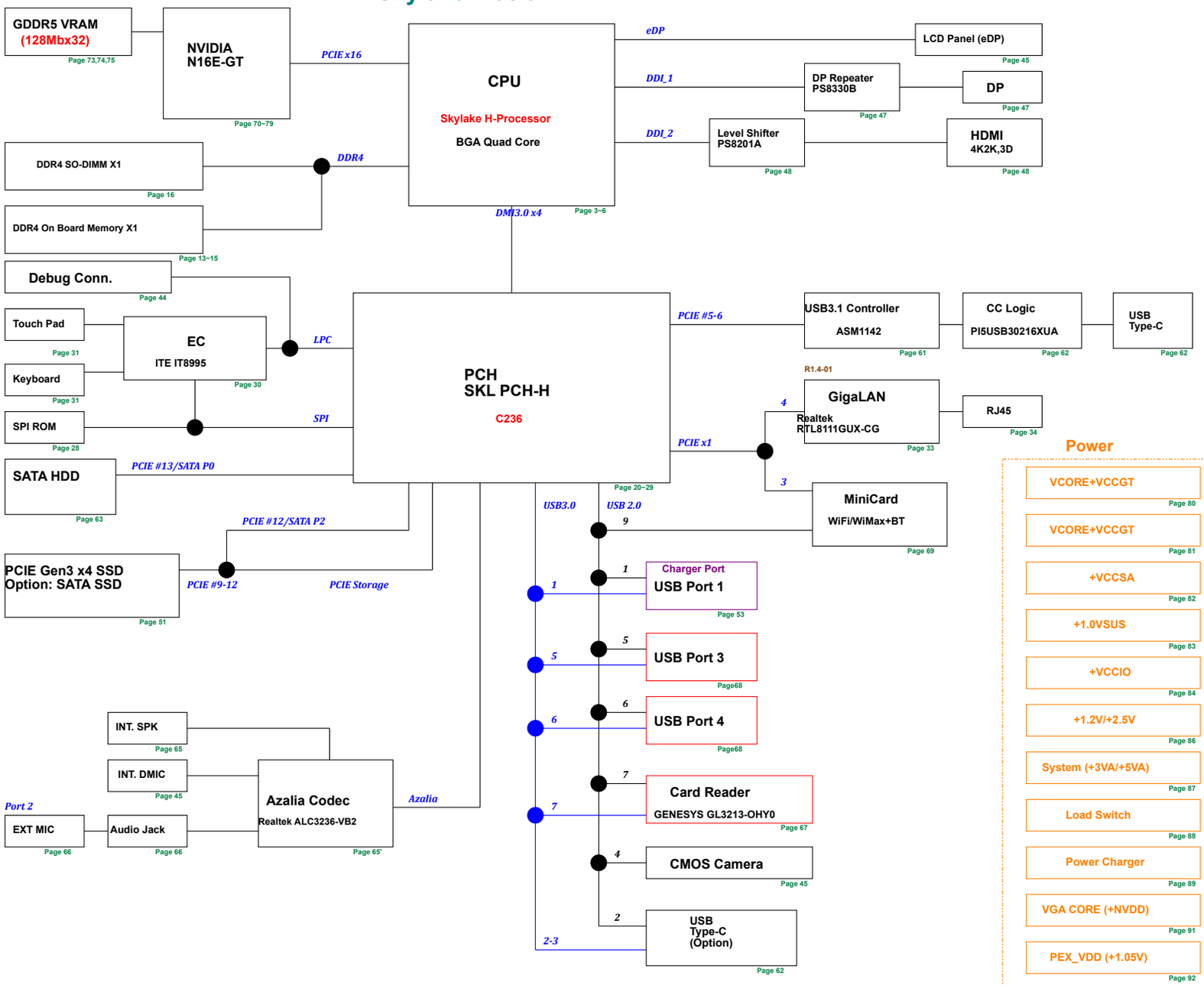
GL502VT Block Diagram

Skylake Platform



Power

- VCORE+VCCGT — Page 80
- VCORE+VCCGT — Page 81
- +VCCSA — Page 82
- +1.0VSUS — Page 83
- +VCCIO — Page 84
- +1.2V/+2.5V — Page 86
- System (+3VA/+5VA) — Page 87
- Load Switch — Page 88
- Power Charger — Page 89
- VGA CORE (+NVDD) — Page 91
- PEX_VDD (+1.05V) — Page 92
- +FBVDDQ — Page 93
- TBT (+VCC12V) — Page 94
- Power OV — Page 97

CPU XDP — Page 7	PWM Fan — Page 50	
PCH XDP — Page 29	LEDs — Page 40	DC & Battery — Page 60
Reset Circuit — Page 32	Discharge Circuit — Page 57	Skew Holes
Thermal Sensor — Page 50	Power Protect — Page 58	EMI Caps

Project Name	GL502VT	Rev	1.0
Title :	Block Diagram		
Size	Custom	Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Marshall Li		
Date:	Friday, December 18, 2015	Sheet	1 of 102

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	BC1B#	Native	BC_1B#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_EBCHIP_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	WE_BusMasterDack		PU 10K(8)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	PCH_GPP_A17			
GPP_A18	GPI	GPI	PCH_GPP_A18			
GPP_A19	GPI	GPI	PCH_GPP_A19			
GPP_A20	GPI	GPI	PCH_GPP_A20			
GPP_A21	GPI	GPI	PCH_GPP_A21			
GPP_A22	GPI	GPI	PCH_GPP_A22			
GPP_A23	GPI	GPI	PCH_GPP_A23			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_FREQ_REQ0# _X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN# _X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT# _X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MSWV_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP914	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPP918	PD		
GPP_B19	GPI	GPO	PCH_GPP919/WT_ON_PCH		PD 10K(8)	
GPP_B20	GPI	GPO	PCH_GPP920/WV_GPO_EVENT#		PU 10K	+3VS
GPP_B21	GPI	GPI	PCH_GPP921/WV_GC6_FB_EN		PD 10K	
GPP_B22	GPO	Strap	PCH_GPP922	PD		
GPP_B23	GPO	GPO	SMLIALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPI	Strap	PCH_GPPC2			
GPP_C3	SMLOCLK	Native	SMLO_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLODATA	Native	SMLO_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		+3VSUS
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SELO		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PD 10K	+3VSUS
GPP_C16	GPO	GPO	AOAC_WLANLED		PU 10K(8)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(8)	+3VS
GPP_C18	GPI	Native	I2C1 _SDA		PU 4.7K	+3VS
GPP_C19	GPI	Native	I2C1 _SCL		PU 4.7K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK			
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 10K(8)	+3VSUS
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT			
GPP_D1	GPO	GPO	GPIO_3 PCH2S_PWR			
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#		PD 100K(8)	
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCH_I2C		PU 10K	
GPP_D10	GPI	Strap	PCH_I2C1		PU 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID		PD 10K(8)	
GPP_D12	GPI	Strap	TOUCH_PANEL_ID		PD 10K(8)	
GPP_D13	GPI	GPI	PCH_GPP_D13		PD 10K(8)	+3VSUS
GPP_D14	GPO	GPO	PCH_GPP_D14/WLAN_LED			
GPP_D15	GPO	GPO	PCH_GPP_D15/WLAN_BT_LED			
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	DIRECT_ESATA_DETECT#		PU 10K(8)	+3VS
GPP_E1	GPI	GPI	SATA_ODD_PRSNT#		PU 10K(8)	+3VS
GPP_E2	GPI	GPI	MSATA_MPCIE_DET#		PU 10K(8)	+3VS
GPP_E3	GPI	GPI	USB31_SW1#		PU 10K	+3V
GPP_E4	GPI	Native	SATAG_HDD_DEVSLP		PU 10K(8)	+3VS
GPP_E5	GPI	Native	M2PF1_DEVSLP		PU 10K(8)	+3VS
GPP_E6	GPI	Native	M2PF2_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	(N.C)			
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	M2PF3_DEVSLP		PU 10K(8)	+3VS
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	L_VDDEN_PCH_X1		PD 100K	
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GPI	Native	L_BKLTCTL_PCH_X1		PD 10K	
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	SATA_ODD_PWRGT			
GPP_G2	GPI	GPI	SATA_HDD_DAP			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_M2PF1# _X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPO	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	WLAN_WAKE_CTRL_CRB			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	DD11_DP_HPD0		PD 100K	
GPP_I1	GPI	Native	DD12_HDMI_HPD1		PD 100K	
GPP_I2	GPI	GPI	DD13_TBT_HPD2			
GPP_I3	GPI	Native	DD1E_VGA_HPD3			
GPP_I4	GPI	Native	EDP_HPD		PD 100K	
GPP_I5	GPI	Native	DDPB_SCL_PCH		PU 2.2K	+3VS
GPP_I6	GPO	Native	DDPB_SDA_PCH	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	DDPC_SCL_PCH		PU 2.2K	+3VS
GPP_I8	GPO	Native	DDPC_SDA_PCH	PD	PU 2.2K	+3VS
GPP_I9	GPI	Native	DDPD_SCL_PCH		PU 2.2K(8)	+3VS
GPP_I10	GPO	Native	DDPD_SDA_PCH	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	PCH_GPD2#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(8)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUS3#		PD 150K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUS5#		PD 150K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(8)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PHYEN		PU 10K(8)	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PU 3M(8)	
GPA1	OD	GPO	CHG_LED#	PU 10K (8)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (8)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN2_PWM		
GPA6	Alt	PWM	PM_LED_PWM		
GPA7	O	GPO	GS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_EC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON		
GPB5	O	GPO	PM_SLP_S03# _WOL		
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (8)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_THRMTRIP#	PU 10K (8)	+3VSUS
GPC4	I	GPI	EC_SATA/CHP1#	PU 10K (8)	+3V
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/WL_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/USB_SS#		
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	EC_GPD7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PU 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PU 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	PCHRSTB# _WOC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PU 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K(8)	+3VA_EC
				PU 1K	+VCCSTG

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VDUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0 CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0 DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_DISACK#		
GPG2	I	GPI	EC_GPG2/PMULIMIT_EC#	PU 100K	+3VA_EC
GPG3	GP2		EC_SCK#/EC_SCK#_PCH	PU 10K (8)	
GPG4	GP2		EC_SI/EC_SI_PCH	PU 10K (8)	
GPG5	GP2		EC_SO/EC_SO_PCH	PU 10K (8)	
GPG6	O	GPO	USB30_5VSUS		
GPG7	GP2		EC_SCK_PCH	PU 10K (8)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3 CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3 DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_SUSWRST#	PU 10K	
GPH4	O	GPO	DPWROK_EC	PU 10K	
GPH5	O	GPO	PM_PWROK	PU 10K	
GPH6	O	GPO	PM_SYSPWROK	PU 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_S0IX#		
GPI1	I	GPI	SYSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP9_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PU 0	+3VACC
GPI7	Alt	AD	WA_MAX_POWER	PU 100K & PU 5401K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB11_5VSUS#		
GPJ1	O	GPO	3VAUSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_USB_STA7#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	EC_SPI0/I2S#	PU 10K (8)	+3V
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EC0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EC01		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EC02		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EC03		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EC0C		CLK_EBCHIP1_PCH		
GPM5	LFRAME#/EC0#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
on board memory CHA	
SO-DIMM B(0)	A4h

EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
VGA Thermal Sensor	90h
CPU Thermal Sensor	98h
Power Thermal Sensor	70h

Device Identification

CPU Thermal Sensor	
1st	0x4d3213b9 / 4CF7FF7U
2nd	

N501VW PCIE & USB Function define

Skylake HM170

XDCI	XDCI Capabilities	Function	SSIC
	PCIEG (From GPU)	dGPU	SSIC0
01	USB3#01	MB USB3.0 (Charger)	
02	USB3#02 / SSIC#01		
03	USB3#03 / SSIC#02	reserve for USB3.1	
04	USB3#04	reserve for USB3.1	
05	USB3#05	USB3.0 IO Port1	
06	USB3#06	USB3.0 IO Port2	
07	USB3#07 / PCIE#01		
08	USB3#08 / PCIE#02	Card reader(PCIE)	SSIC2
09	PCIE#03	WLAN	SSIC3
10	PCIE#04 / GBE	reserve	SSIC4
11	PCIE#05 / GBE		
12	PCIE#06	TBT AR	SSIC5
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE		
16	PCIE#10 / SATA#1	PCIE*4 SSD	SSIC6
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE	HDD (SATA-0B)	
20	PCIE#14 / SATA#1	reserve (SATA-1B)	
21	PCIE#15 / SATA#2	SSD (SATA-2)	
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	reserve for USB3.1
USB2_03	reserve for USB3.1
USB2_04	Camera
USB2_05	USB3.0 IO Port1
USB2_06	USB3.0 IO Port2
USB2_07	
USB2_08	
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	Touchpanel

SKL PCH-H Z170 HSIO

1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7	PCIE #1	x2	x4	NA
8	USB3 #8	PCIE #2			
9	USB3 #9	PCIE #3	x2		
10	USB3 #10	PCIE #4	GbE		
11	PCIE #5		GbE	x2	x4
12	PCIE #6				NA
13	PCIE #7			x2	
14	PCIE #8				
15	PCIE #9	SATA #0	GbE	x2	x4
16	PCIE #10	SATA #1			Intel IRST PCIE Storage Device #1
17	PCIE #11			x2	
18	PCIE #12		GbE		
19	PCIE #13	SATA #0*	GbE	x2	x4
20	PCIE #14	SATA #1*			Intel IRST PCIE Storage Device #2
21	PCIE #15	SATA #2		x2	
22	PCIE #16	SATA #3			
23	PCIE #17	SATA #4		x2	x4
24	PCIE #18	SATA #5			Intel IRST PCIE Storage Device #3
25	PCIE #19	SATA #6		x2	
26	PCIE #20	SATA #7			

SKL PCH-H H170 HSIO

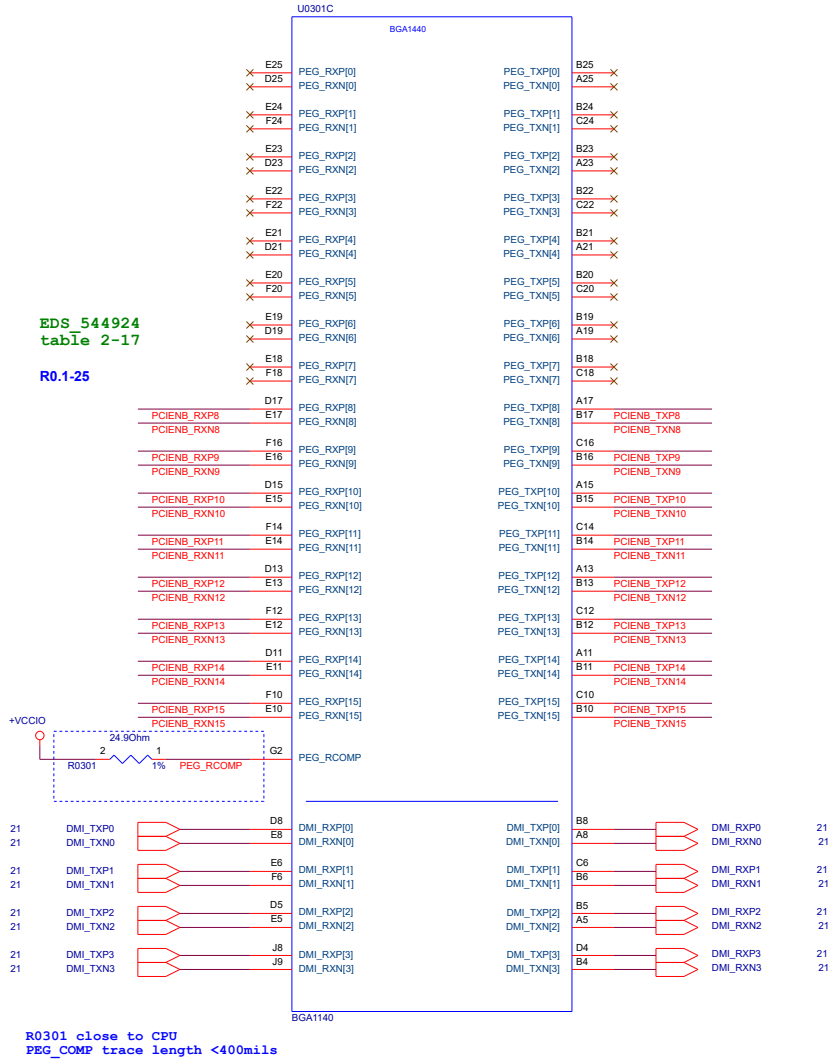
1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7				
8	USB3 #8				
9	PCIE #3		x2	NA	NA
10	PCIE #4		GbE		
11	PCIE #5		GbE	x2	x4
12	PCIE #6				NA
13	PCIE #7			x2	
14	PCIE #8				
15	PCIE #9	SATA #0	GbE	x2	x4
16	PCIE #10	SATA #1			Intel IRST PCIE Storage Device #1
17	PCIE #11			x2	
18	PCIE #12		GbE		
19	PCIE #13	SATA #0*	GbE	x2	x4
20	PCIE #14	SATA #1*			Intel IRST PCIE Storage Device #2
21	PCIE #15	SATA #2		x2	
22	PCIE #16	SATA #3			
23	SATA #4			NA	NA
24	SATA #5				NA
25	PCIE #19			x2	
26	PCIE #20				

SKL PCH-H HM170 HSIO

1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7	PCIE #1	x2	x4	NA
8	USB3 #8	PCIE #2			
9	PCIE #3		x2		
10	PCIE #4		GbE		
11	PCIE #5		GbE	x2	x4
12	PCIE #6				NA
13	PCIE #7			x2	
14	PCIE #8				
15	PCIE #9	SATA #0	GbE	x2	x4
16	PCIE #10	SATA #1			Intel IRST PCIE Storage Device #1
17	PCIE #11			x2	
18	PCIE #12		GbE		
19	PCIE #13	SATA #0*	GbE	x2	x4
20	PCIE #14	SATA #1*			Intel IRST PCIE Storage Device #2
21	PCIE #15	SATA #2		x2	
22	PCIE #16	SATA #3			
23				NA	NA
24					NA
25				x2	
26					

ASUS	Project Name: N501VW		Rev: 1.0
Title : System Setting			
Size: B	Date: Wednesday, 25 April 2018	Engineer: EE	
Sheet 1 of 57			

PCIEG



R0.1-25

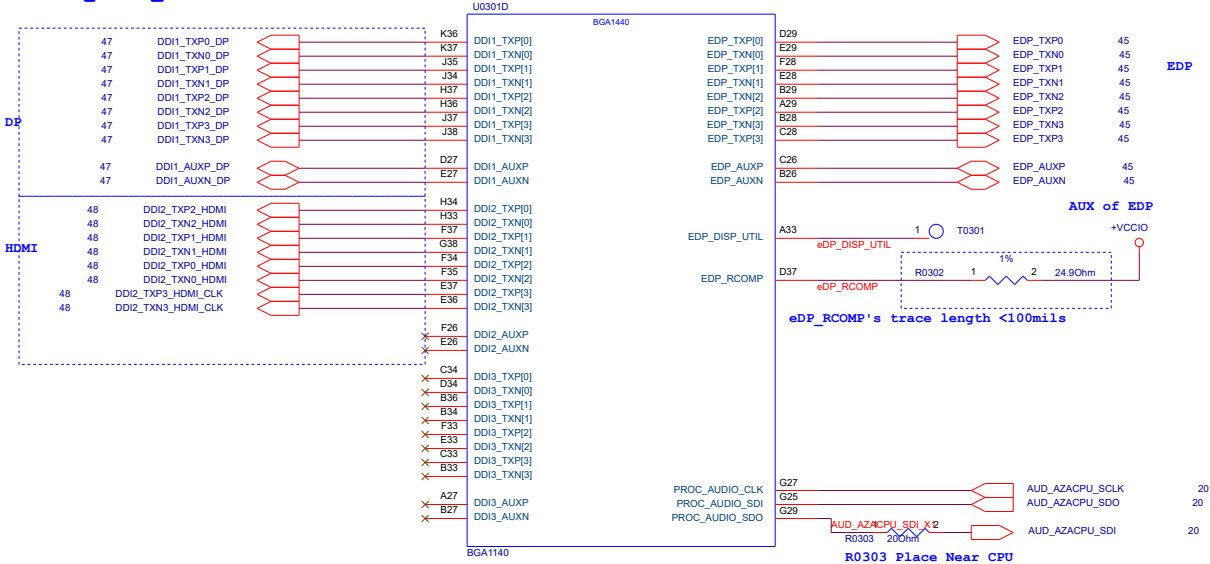
CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8

PCIEG_RXN[7:0] 70
PCIEG_RXP[7:0] 70
PCIENB_RXN[15:8] 70
PCIENB_RXP[15:8] 70

	CX0309			0.22UF/6.3V	
PCIENB_TXN8	CX0310	1	2	0.22UF/6.3V	PCIEG_RXN7
PCIENB_TXN9	CX0311	1	2	0.22UF/6.3V	PCIEG_RXN6
PCIENB_TXN10	CX0312	1	2	0.22UF/6.3V	PCIEG_RXN5
PCIENB_TXN11	CX0313	1	2	0.22UF/6.3V	PCIEG_RXN4
PCIENB_TXN12	CX0314	1	2	0.22UF/6.3V	PCIEG_RXN3
PCIENB_TXN13	CX0315	1	2	0.22UF/6.3V	PCIEG_RXN2
PCIENB_TXN14	CX0316	1	2	0.22UF/6.3V	PCIEG_RXN1
PCIENB_TXN15		1	2		PCIEG_RXN0

	CX0325			0.22UF/6.3V	
PCIENB_TXP8	CX0326	1	2	0.22UF/6.3V	PCIEG_RXP7
PCIENB_TXP9	CX0327	1	2	0.22UF/6.3V	PCIEG_RXP6
PCIENB_TXP10	CX0328	1	2	0.22UF/6.3V	PCIEG_RXP5
PCIENB_TXP11	CX0329	1	2	0.22UF/6.3V	PCIEG_RXP4
PCIENB_TXP12	CX0330	1	2	0.22UF/6.3V	PCIEG_RXP3
PCIENB_TXP13	CX0331	1	2	0.22UF/6.3V	PCIEG_RXP2
PCIENB_TXP14	CX0332	1	2	0.22UF/6.3V	PCIEG_RXP1
PCIENB_TXP15		1	2		PCIEG_RXP0

Display



ASUS	Project Name: N501VW	Rev: 1.0
Title :	CPU_DMI,PEG,FDI,eDP,DDI	
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 3 of 102	

Memory Channel A

U0301A — BGA1440

M_A_DQ[63:0]

M_A_DQ0	BR6	DDR0_DQ[0]
M_A_DQ1	BT6	DDR0_DQ[1]
M_A_DQ2	BP3	DDR0_DQ[2]
M_A_DQ3	BR3	DDR0_DQ[3]
M_A_DQ4	BN5	DDR0_DQ[4]
M_A_DQ5	BP6	DDR0_DQ[5]
M_A_DQ6	BP2	DDR0_DQ[6]
M_A_DQ7	BN3	DDR0_DQ[7]
M_A_DQ8	BL4	DDR0_DQ[8]
M_A_DQ9	BL5	DDR0_DQ[9]
M_A_DQ10	BL2	DDR0_DQ[10]
M_A_DQ11	BM1	DDR0_DQ[11]
M_A_DQ12	BK4	DDR0_DQ[12]
M_A_DQ13	BK5	DDR0_DQ[13]
M_A_DQ14	BK1	DDR0_DQ[14]
M_A_DQ15	BK2	DDR0_DQ[15]
M_A_DQ16	BG4	DDR0_DQ[16]/DDR0_DQ[32]
M_A_DQ17	BG5	DDR0_DQ[17]/DDR0_DQ[33]
M_A_DQ18	BF4	DDR0_DQ[18]/DDR0_DQ[34]
M_A_DQ19	BF5	DDR0_DQ[19]/DDR0_DQ[35]
M_A_DQ20	BG2	DDR0_DQ[20]/DDR0_DQ[36]
M_A_DQ21	BG1	DDR0_DQ[21]/DDR0_DQ[37]
M_A_DQ22	BF1	DDR0_DQ[22]/DDR0_DQ[38]
M_A_DQ23	BF2	DDR0_DQ[23]/DDR0_DQ[39]
M_A_DQ24	BD2	DDR0_DQ[24]/DDR0_DQ[40]
M_A_DQ25	BD1	DDR0_DQ[25]/DDR0_DQ[41]
M_A_DQ26	BC4	DDR0_DQ[26]/DDR0_DQ[42]
M_A_DQ27	BC5	DDR0_DQ[27]/DDR0_DQ[43]
M_A_DQ28	BD5	DDR0_DQ[28]/DDR0_DQ[44]
M_A_DQ29	BD4	DDR0_DQ[29]/DDR0_DQ[45]
M_A_DQ30	BC1	DDR0_DQ[30]/DDR0_DQ[46]
M_A_DQ31	BC2	DDR0_DQ[31]/DDR0_DQ[47]
M_A_DQ32	AB1	DDR0_DQ[32]/DDR1_DQ[0]
M_A_DQ33	AB2	DDR0_DQ[33]/DDR1_DQ[1]
M_A_DQ34	AA4	DDR0_DQ[34]/DDR1_DQ[2]
M_A_DQ35	AA5	DDR0_DQ[35]/DDR1_DQ[3]
M_A_DQ36	AB4	DDR0_DQ[36]/DDR1_DQ[4]
M_A_DQ37	AA2	DDR0_DQ[37]/DDR1_DQ[5]
M_A_DQ38	AA1	DDR0_DQ[38]/DDR1_DQ[6]
M_A_DQ39	V5	DDR0_DQ[39]/DDR1_DQ[7]
M_A_DQ40	V2	DDR0_DQ[40]/DDR1_DQ[8]
M_A_DQ41	U1	DDR0_DQ[41]/DDR1_DQ[9]
M_A_DQ42	U2	DDR0_DQ[42]/DDR1_DQ[10]
M_A_DQ43	V1	DDR0_DQ[43]/DDR1_DQ[11]
M_A_DQ44	V4	DDR0_DQ[44]/DDR1_DQ[12]
M_A_DQ45	U5	DDR0_DQ[45]/DDR1_DQ[13]
M_A_DQ46	U4	DDR0_DQ[46]/DDR1_DQ[14]
M_A_DQ47	R4	DDR0_DQ[47]/DDR1_DQ[15]
M_A_DQ48	P5	DDR0_DQ[48]/DDR1_DQ[32]
M_A_DQ49	R4	DDR0_DQ[49]/DDR1_DQ[33]
M_A_DQ50	P4	DDR0_DQ[50]/DDR1_DQ[34]
M_A_DQ51	R5	DDR0_DQ[51]/DDR1_DQ[35]
M_A_DQ52	P2	DDR0_DQ[52]/DDR1_DQ[36]
M_A_DQ53	R1	DDR0_DQ[53]/DDR1_DQ[37]
M_A_DQ54	P1	DDR0_DQ[54]/DDR1_DQ[38]
M_A_DQ55	M4	DDR0_DQ[55]/DDR1_DQ[39]
M_A_DQ56	M1	DDR0_DQ[56]/DDR1_DQ[40]
M_A_DQ57	L4	DDR0_DQ[57]/DDR1_DQ[41]
M_A_DQ58	L2	DDR0_DQ[58]/DDR1_DQ[42]
M_A_DQ59	M5	DDR0_DQ[59]/DDR1_DQ[43]
M_A_DQ60	M2	DDR0_DQ[60]/DDR1_DQ[44]
M_A_DQ61	L5	DDR0_DQ[61]/DDR1_DQ[45]
M_A_DQ62	L1	DDR0_DQ[62]/DDR1_DQ[46]
M_A_DQ63		DDR0_DQ[63]/DDR1_DQ[47]

BA2		DDR0_ECC[0]
BA1		DDR0_ECC[1]
AY4		DDR0_ECC[2]
AY5		DDR0_ECC[3]
BA5		DDR0_ECC[4]
BA4		DDR0_ECC[5]
AY1		DDR0_ECC[6]
AY2		DDR0_ECC[7]

DDR CHANNEL A

BGA1140

AG1		DDR0_CKP[0]
AG2	M_A_DIM0_CK_DDR0_DP	DDR0_CKN[0]
AK1	M_A_DIM0_CK_DDR0_DN	DDR0_CKN[1]
AK2	M_A_DIM0_CK_DDR1_DN	DDR0_CKP[1]
AL3	M_A_DIM0_CK_DDR1_DP	DDR0_CLKP[2]
AK3		DDR0_CLKN[2]
AL2		DDR0_CLKP[3]
AL1		DDR0_CLKN[3]
AT1		DDR0_CKE[0]
AT2		DDR0_CKE[1]
AT3	M_A_DIM0_CKE1	DDR0_CKE[2]
AT5		DDR0_CKE[3]
AD5		DDR0_CS#[0]
AE2		DDR0_CS#[1]
AD2	M_A_DIM0_CS1#	DDR0_CS#[2]
AE5		DDR0_CS#[3]
AD3		DDR0_ODT[0]
AE4		DDR0_ODT[1]
AE1	M_A_DIM0_ODT1_2DIE	DDR0_ODT[2]
AD4		DDR0_ODT[3]

AH5		DDR0_CAB[4]/DDR0_BA[0]	
AH1		DDR0_CAB[6]/DDR0_BA[1]	
AU1		DDR0_CAA[5]/DDR0_BG[0]	
AH4	M_A_A16	DDR0_CAB[3]/DDR0_MA[16]	
AG4	M_A_A14	DDR0_CAB[2]/DDR0_MA[14]	
AD1	M_A_A15	DDR0_CAB[1]/DDR0_MA[15]	
AH3	M_A_A0	DDR0_CAB[9]/DDR0_MA[0]	
AP4	M_A_A1	DDR0_CAB[8]/DDR0_MA[1]	
AN4	M_A_A2	DDR0_CAB[5]/DDR0_MA[2]	
AP5	M_A_A3	DDR0_MA[3]	
AP2	M_A_A4	DDR0_MA[4]	
AP1	M_A_A5	DDR0_CAA[0]/DDR0_MA[5]	
AP3	M_A_A6	DDR0_CAA[2]/DDR0_MA[6]	
AN1	M_A_A7	DDR0_CAA[4]/DDR0_MA[7]	
AN3	M_A_A8	DDR0_CAA[3]/DDR0_MA[8]	
AT4	M_A_A9	DDR0_CAA[1]/DDR0_MA[9]	
AH2	M_A_A10	DDR0_CAB[7]/DDR0_MA[10]	
AN2	M_A_A11	DDR0_CAA[7]/DDR0_MA[11]	
AU4	M_A_A12	DDR0_CAA[6]/DDR0_MA[12]	
AE3	M_A_A13	DDR0_CAB[0]/DDR0_MA[13]	
AU2	M_A_BG1	DDR0_CAA[9]/DDR0_BG[1]	
AU3	M_A_ACT#	DDR0_CAA[8]/DDR0_ACT#	
AG3	M_A_PARITY	DDR0_PAR	
AU5	M_A_ALERT#	DDR0_ALERT#	

BR5	M_A_DQS#[3:0]	DDR0_DQSN[0]
BL3	M_A_DQS#0	DDR0_DQSN[1]
BG3	M_A_DQS#1	DDR0_DQSN[2]/DDR0_DQSN[4]
BD3	M_A_DQS#2	DDR0_DQSN[3]/DDR0_DQSN[5]
AB3	M_A_DQS#3	DDR0_DQSP[4]/DDR1_DQSP[0]
V3	M_A_DQS4	DDR0_DQSP[5]/DDR1_DQSP[1]
R3	M_A_DQS5	DDR0_DQSP[6]/DDR1_DQSP[4]
M3	M_A_DQS6	DDR0_DQSP[7]/DDR1_DQSP[5]
BP5	M_A_DQS[3:0]	DDR0_DQSP[0]
BK3	M_A_DQS0	DDR0_DQSP[1]
BF3	M_A_DQS1	DDR0_DQSP[2]/DDR0_DQSP[4]
BC3	M_A_DQS2	DDR0_DQSP[3]/DDR0_DQSP[5]
AA3	M_A_DQS3	DDR0_DQSN[4]/DDR1_DQSN[0]
U3	M_A_DQS#4	DDR0_DQSN[5]/DDR1_DQSN[1]
P3	M_A_DQS#5	DDR0_DQSN[6]/DDR1_DQSN[4]
L3	M_A_DQS#6	DDR0_DQSN[7]/DDR1_DQSN[5]
AY3	M_A_DQS#7	DDR0_DQSP[8]
BA3	M_A_DQS#[7:4]	DDR0_DQSN[8]

Memory Channel B

U0301B — BGA1440

M_B_DQ[63:0]

M_B_DQ0	BT11	DDR1_DQ[0]/DDR0_DQ[16]
M_B_DQ1	BR11	DDR1_DQ[1]/DDR0_DQ[17]
M_B_DQ2	BT8	DDR1_DQ[2]/DDR0_DQ[18]
M_B_DQ3	BR8	DDR1_DQ[3]/DDR0_DQ[19]
M_B_DQ4	BP11	DDR1_DQ[4]/DDR0_DQ[20]
M_B_DQ5	BN11	DDR1_DQ[5]/DDR0_DQ[21]
M_B_DQ6	BP8	DDR1_DQ[6]/DDR0_DQ[22]
M_B_DQ7	BN8	DDR1_DQ[7]/DDR0_DQ[23]
M_B_DQ8	BL12	DDR1_DQ[8]/DDR0_DQ[24]
M_B_DQ9	BL11	DDR1_DQ[9]/DDR0_DQ[25]
M_B_DQ10	BL8	DDR1_DQ[10]/DDR0_DQ[26]
M_B_DQ11	BJ8	DDR1_DQ[11]/DDR0_DQ[27]
M_B_DQ12	BJ11	DDR1_DQ[12]/DDR0_DQ[28]
M_B_DQ13	BJ10	DDR1_DQ[13]/DDR0_DQ[29]
M_B_DQ14	BL7	DDR1_DQ[14]/DDR0_DQ[30]
M_B_DQ15	BJ7	DDR1_DQ[15]/DDR0_DQ[31]
M_B_DQ16	BG11	DDR1_DQ[16]/DDR0_DQ[48]
M_B_DQ17	BG10	DDR1_DQ[17]/DDR0_DQ[49]
M_B_DQ18	BG8	DDR1_DQ[18]/DDR0_DQ[50]
M_B_DQ19	BF8	DDR1_DQ[19]/DDR0_DQ[51]
M_B_DQ20	BF11	DDR1_DQ[20]/DDR0_DQ[52]
M_B_DQ21	BF10	DDR1_DQ[21]/DDR0_DQ[53]
M_B_DQ22	BG7	DDR1_DQ[22]/DDR0_DQ[54]
M_B_DQ23	BF7	DDR1_DQ[23]/DDR0_DQ[55]
M_B_DQ24	BB11	DDR1_DQ[24]/DDR0_DQ[56]
M_B_DQ25	BC11	DDR1_DQ[25]/DDR0_DQ[57]
M_B_DQ26	BB8	DDR1_DQ[26]/DDR0_DQ[58]
M_B_DQ27	BC8	DDR1_DQ[27]/DDR0_DQ[59]
M_B_DQ28	BC10	DDR1_DQ[28]/DDR0_DQ[60]
M_B_DQ29	BB10	DDR1_DQ[29]/DDR0_DQ[61]
M_B_DQ30	BC7	DDR1_DQ[30]/DDR0_DQ[62]
M_B_DQ31	BB7	DDR1_DQ[31]/DDR0_DQ[63]
M_B_DQ32	AA11	DDR1_DQ[32]/DDR1_DQ[16]
M_B_DQ33	AA10	DDR1_DQ[33]/DDR1_DQ[17]
M_B_DQ34	AC11	DDR1_DQ[34]/DDR1_DQ[18]
M_B_DQ35	AC10	DDR1_DQ[35]/DDR1_DQ[19]
M_B_DQ36	AA7	DDR1_DQ[36]/DDR1_DQ[20]
M_B_DQ37	AA8	DDR1_DQ[37]/DDR1_DQ[21]
M_B_DQ38	AC8	DDR1_DQ[38]/DDR1_DQ[22]
M_B_DQ39	AC7	DDR1_DQ[39]/DDR1_DQ[23]
M_B_DQ40	W8	DDR1_DQ[40]/DDR1_DQ[24]
M_B_DQ41	W7	DDR1_DQ[41]/DDR1_DQ[25]
M_B_DQ42	V10	DDR1_DQ[42]/DDR1_DQ[26]
M_B_DQ43	V11	DDR1_DQ[43]/DDR1_DQ[27]
M_B_DQ44	W11	DDR1_DQ[44]/DDR1_DQ[28]
M_B_DQ45	W10	DDR1_DQ[45]/DDR1_DQ[29]
M_B_DQ46	V7	DDR1_DQ[46]/DDR1_DQ[30]
M_B_DQ47	V8	DDR1_DQ[47]/DDR1_DQ[31]
M_B_DQ48	R11	DDR1_DQ[48]
M_B_DQ49	P11	DDR1_DQ[49]
M_B_DQ50	P7	DDR1_DQ[50]
M_B_DQ51	R8	DDR1_DQ[51]
M_B_DQ52	R10	DDR1_DQ[52]
M_B_DQ53	P10	DDR1_DQ[53]
M_B_DQ54	R7	DDR1_DQ[54]
M_B_DQ55	P8	DDR1_DQ[55]
M_B_DQ56	L11	DDR1_DQ[56]
M_B_DQ57	M11	DDR1_DQ[57]
M_B_DQ58	L7	DDR1_DQ[58]
M_B_DQ59	M8	DDR1_DQ[59]
M_B_DQ60	L10	DDR1_DQ[60]
M_B_DQ61	M10	DDR1_DQ[61]
M_B_DQ62	M7	DDR1_DQ[62]
M_B_DQ63	L8	DDR1_DQ[63]

AW11		DDR1_ECC[0]
AY11		DDR1_ECC[1]
AY8		DDR1_ECC[2]
AW8		DDR1_ECC[3]
AY10		DDR1_ECC[4]
AW10		DDR1_ECC[5]
AY7		DDR1_ECC[6]
AW7		DDR1_ECC[7]

DDR CHANNEL B

BGA1140

AM9	M_B_CLK_DDR0	DDR1_CKP[0]
AN9	M_B_CLK_DDR#0	DDR1_CKN[0]
AM8	M_B_CLK_DDR#1	DDR1_CKN[1]
AM7	M_B_CLK_DDR1	DDR1_CKP[1]
AM11		DDR1_CLKP[2]
AM10		DDR1_CLKN[2]
AJ10		DDR1_CLKP[3]
AJ11		DDR1_CLKN[3]
AT8	M_B_CKE0	DDR1_CKE[0]
AT10	M_B_CKE1	DDR1_CKE[1]
AT7		DDR1_CKE[2]
AT11		DDR1_CKE[3]
AF11	M_B_CS#0	DDR1_CS#[0]
AE7	M_B_CS#1	DDR1_CS#[1]
AF10		DDR1_CS#[2]
AE10		DDR1_CS#[3]
AF7	M_B_ODT0	DDR1_ODT[0]
AE8	M_B_ODT1	DDR1_ODT[1]
AE9		DDR1_ODT[2]
AE11		DDR1_ODT[3]

AH10		DDR1_CAB[3]/DDR1_MA[16]	DDR1_RAS#
AH11		DDR1_CAB[2]/DDR1_MA[14]	DDR1_WE#
AF8		DDR1_CAB[1]/DDR1_MA[15]	DDR1_CAS#
AH8	M_B_BA0	DDR1_CAB[4]/DDR1_BA[0]	DDR1_BA[0]/
AH9	M_B_BA1	DDR1_CAB[6]/DDR1_BA[1]	DDR1_BA[1]/
AR9	M_B_BG0	DDR1_CAA[5]/DDR1_BG[0]	DDR1_BA[2]/
AJ9	M_B_A[13:0]	DDR1_CAB[9]/DDR1_MA[0]	DDR1_MA[0]/
AK6	M_B_A0	DDR1_CAB[8]/DDR1_MA[1]	DDR1_MA[1]/
AK5	M_B_A1	DDR1_CAB[5]/DDR1_MA[2]	DDR1_MA[2]/
AL5	M_B_A2	DDR1_MA[3]	
AL6	M_B_A3	DDR1_MA[4]	
AM6	M_B_A4	DDR1_CAA[0]/DDR1_MA[5]	DDR1_MA[5]/
AN7	M_B_A5	DDR1_CAA[2]/DDR1_MA[6]	DDR1_MA[6]/
AN10	M_B_A6	DDR1_CAA[4]/DDR1_MA[7]	DDR1_MA[7]/
AN8	M_B_A7	DDR1_CAA[3]/DDR1_MA[8]	DDR1_MA[8]/
AR11	M_B_A8	DDR1_CAA[1]/DDR1_MA[9]	DDR1_MA[9]/
AH7	M_B_A9	DDR1_CAB[7]/DDR1_MA[10]	DDR1_MA[10]/
AN11	M_B_A10	DDR1_CAA[7]/DDR1_MA[11]	DDR1_MA[11]/
AR10	M_B_A11	DDR1_CAA[6]/DDR1_MA[12]	DDR1_MA[12]/
AF9	M_B_A12	DDR1_CAB[0]/DDR1_MA[13]	DDR1_MA[13]/
AR7	M_B_A13	DDR1_CAA[9]/DDR1_BG[1]	DDR1_MA[14]/
AT9	M_B_BG1	DDR1_CAA[8]/DDR1_ACT#	DDR1_MA[15]/
AJ7	M_B_PARITY	DDR1_PAR	
AR8	M_B_ALERT#	DDR1_ALERT#	

BP9	M_B_DQS#[7:0]	DDR1_DQSN[0]/DDR0_DQSN[2]
BL9	M_B_DQS#0	DDR1_DQSN[1]/DDR0_DQSN[3]
BG9	M_B_DQS#1	DDR1_DQSN[2]/DDR0_DQSN[6]
BC9	M_B_DQS#2	DDR1_DQSN[3]/DDR0_DQSN[7]
AC9	M_B_DQS#3	DDR1_DQSN[4]/DDR1_DQSN[2]
W9	M_B_DQS#4	DDR1_DQSN[5]/DDR1_DQSN[3]
R9	M_B_DQS#5	DDR1_DQSN[6]
M9	M_B_DQS#6	DDR1_DQSN[7]
BR9	M_B_DQS[7:0]	DDR1_DQSP[0]/DDR0_DQSP[2]
BJ9	M_B_DQS0	DDR1_DQSP[1]/DDR0_DQSP[3]
BF9	M_B_DQS1	DDR1_DQSP[2]/DDR0_DQSP[6]
BB9	M_B_DQS2	DDR1_DQSP[3]/DDR0_DQSP[7]
AA9	M_B_DQS3	DDR1_DQSP[4]/DDR1_DQSP[2]
V9	M_B_DQS4	DDR1_DQSP[5]/DDR1_DQSP[3]
P9	M_B_DQS5	DDR1_DQSP[6]
L9	M_B_DQS6	DDR1_DQSP[7]
AW9	M_B_DQS7	DDR1_DQSP[8]
AY9		DDR1_DQSN[8]

DDR4 COMPENSATION SIGNALS

R0401	1	2	121Ohm	1%	G1
R0402			75Ohm	1%	H1
R0403	11	2	100Ohm	1%	J2

SM_RCOMP0
SM_RCOMP1
SM_RCOMP2

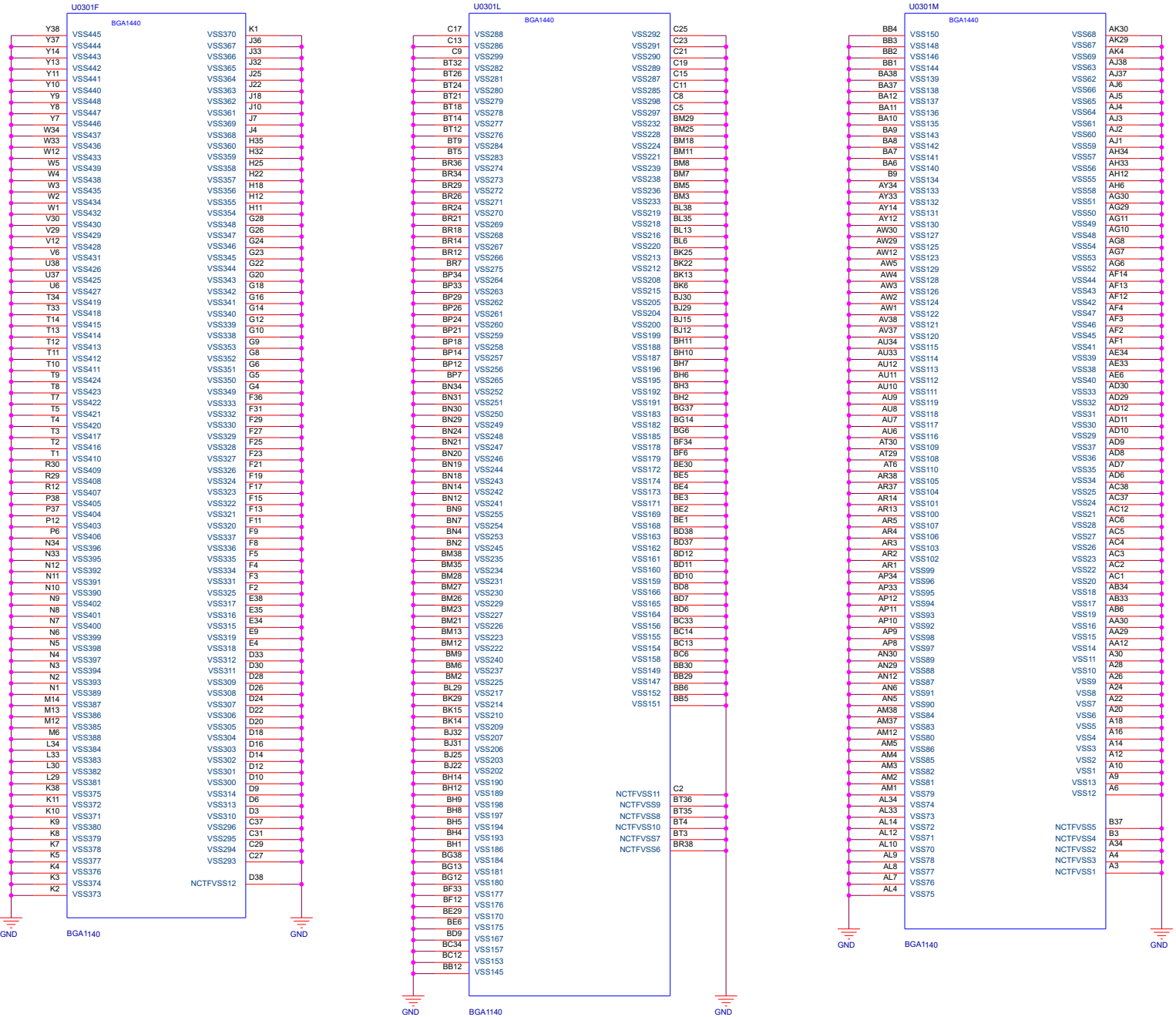
DDR_RCOMP[0]
DDR_RCOMP[1]
DDR_RCOMP[2]

DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ

BN13
BP13
BR13

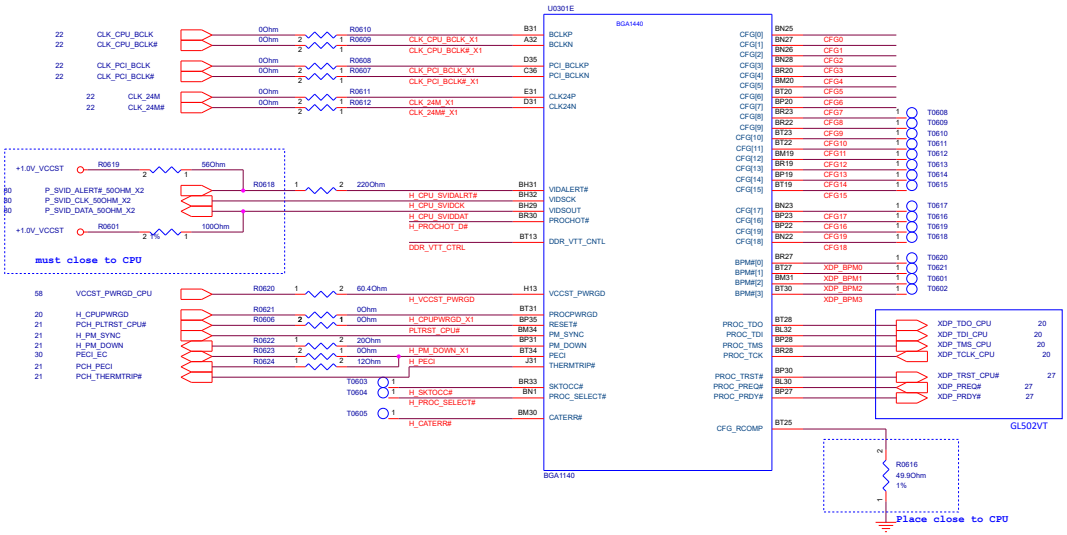
+V_DDR_CA_VREF
SB_DIMM_VREFDQ

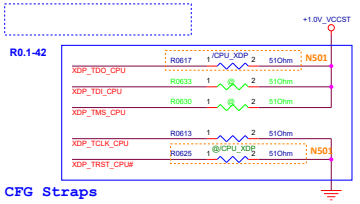
Project Name	N501VW	Rev 1.0
Title :	CPU_DDR4	
Size	Custom	
Dept.:	ASUSTeK COMPUTER	Engineer: EE
Date:	Friday, December 18, 2015	Sheet 4 of 102



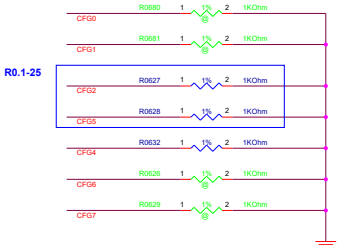
Project Name: N501VW		Rev: 1.0
Title : CPU_CFG,RSVD,GND		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 5 of 102	

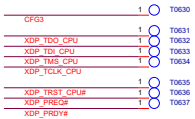
CFG





CFG Straps





CFG Straps for Processor

ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

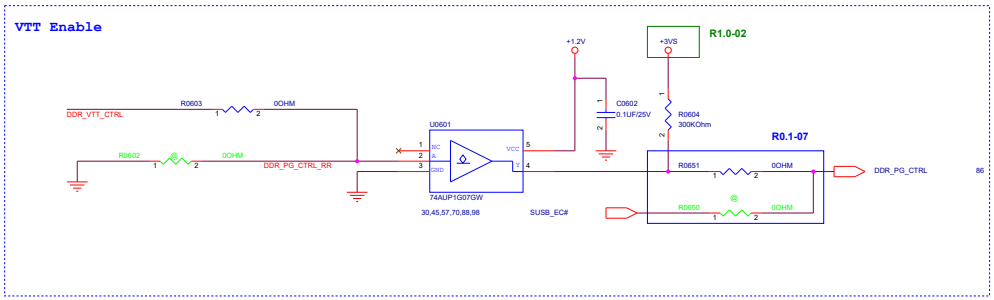
CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

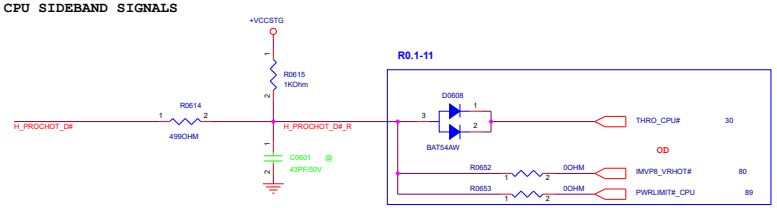
Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121
Richard 2014I209

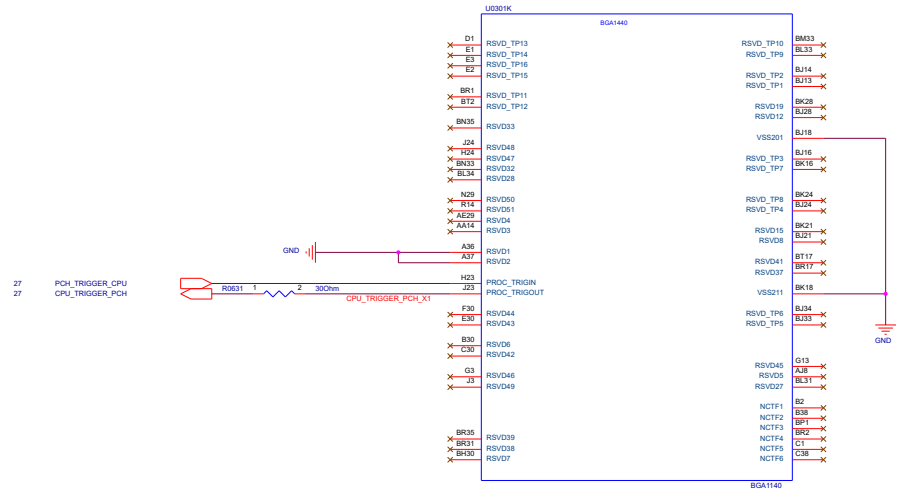
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

VTT Enable



CPU SIDEBAND SIGNALS



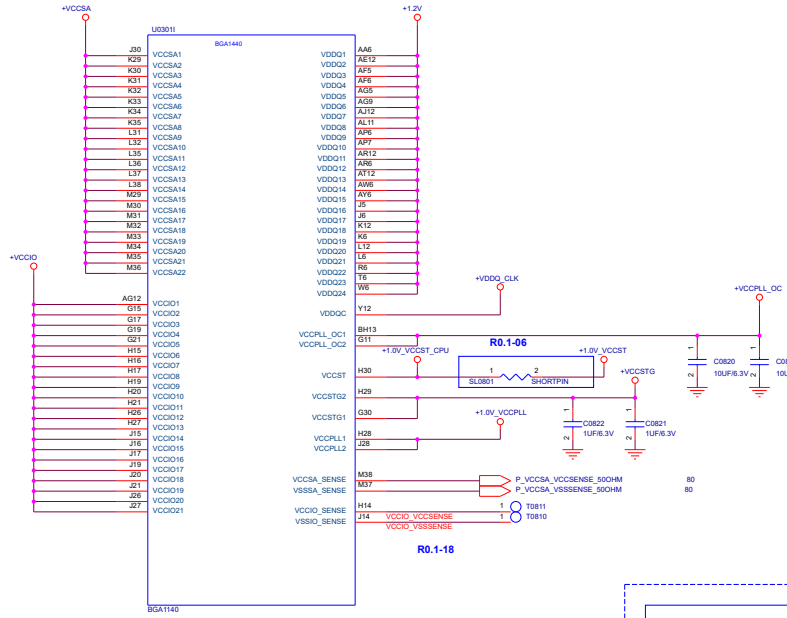


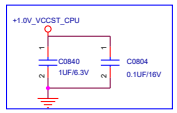
Project Name	N501VW
Rev	1.0
Title :	NB_****
Size	C
Dept.:	ASUSTeK COMPUTER
Engineer:	EE
Date:	Friday, December 18, 2015
Sheet	6 of 102

ASUS	Project Name: N501VW	Rev: 1.0
Title : CPU XDP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 7 of 102	

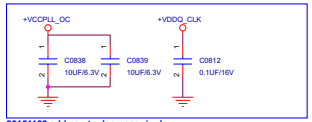
Main Board

OPC Power Rails



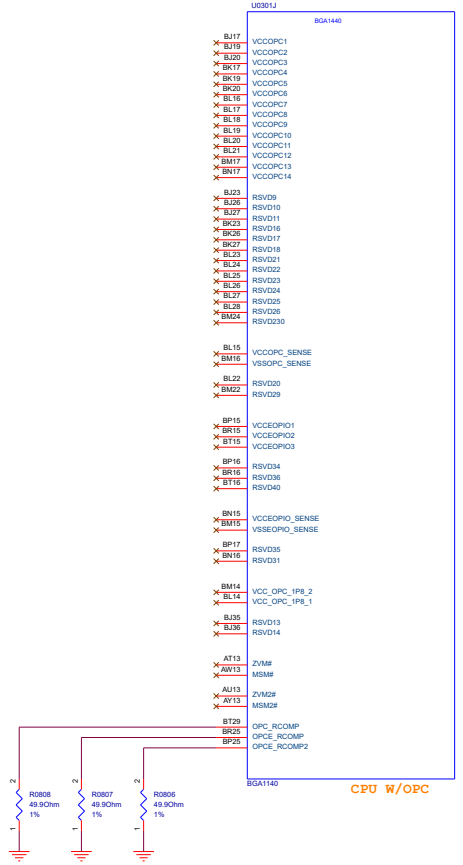


151015 靠近CPU擺放

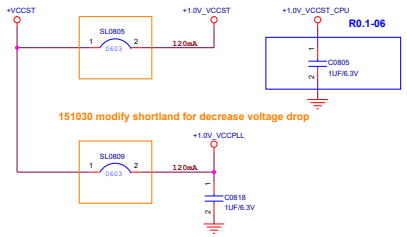


20151102 add cap to decrease ripple

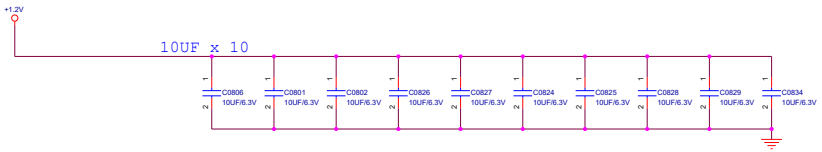
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST
			+1.0V_VCCPLL
	+1.2V	+VDDQ_CPU	+VDDQ_CLK
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	



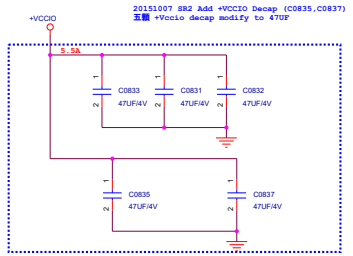
+1.0V_VCCST/+1.0V_VCCPLL DECAPS Place Back Side (TOP)



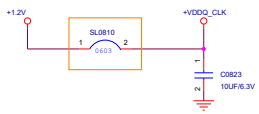
+VDDQ DECAPS Place Back Side (TOP)



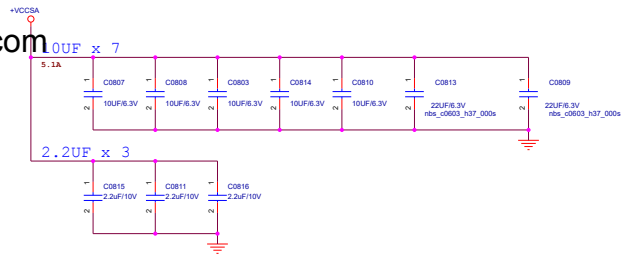
+VCCIO DECAPS Place Back Side (TOP)



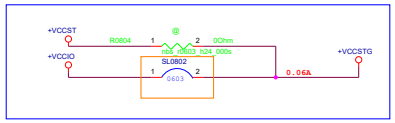
+VDDQ_CLK DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)



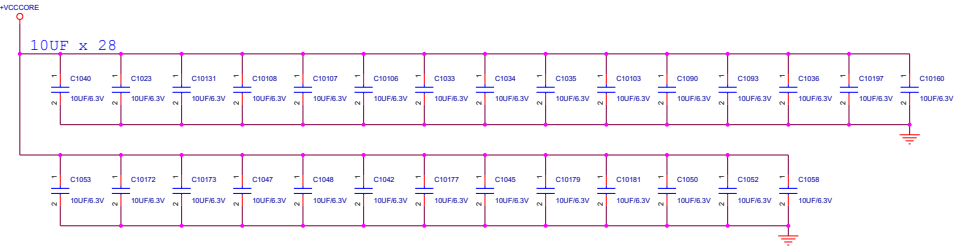
R0.1-06

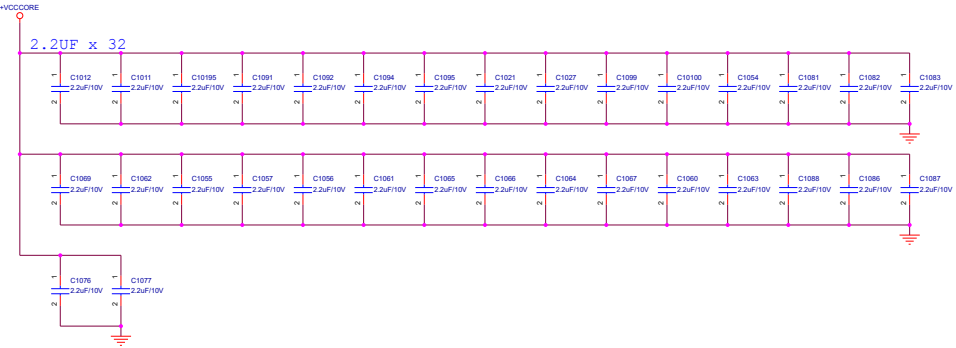


Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)

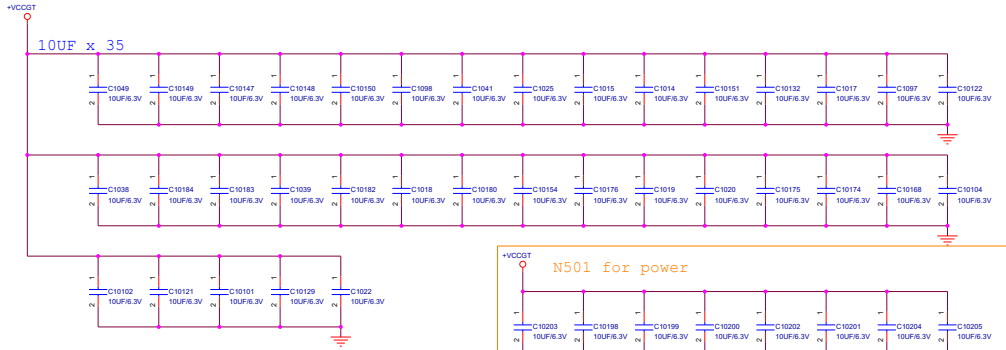
ASUS	Project Name: N501VW		Rev: 1.0
Title : CPU_PWR			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, December 18, 2015	Sheet 8 of 102		

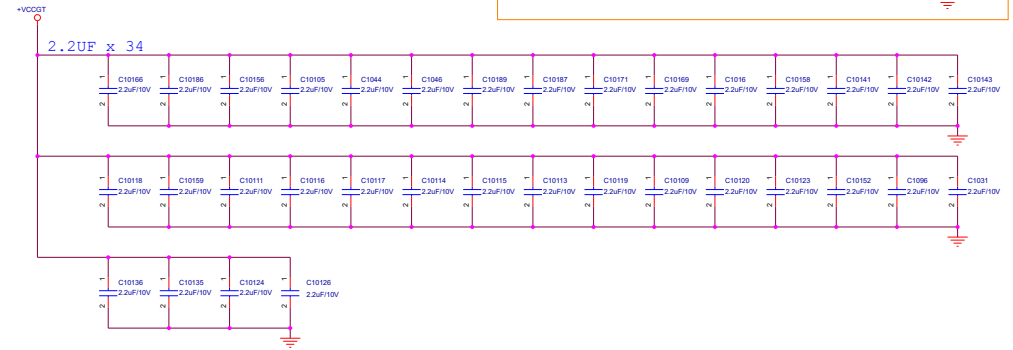
+VCCORE DECAPS Place Back Side (TOP)





+VCCGT DECAPS Place Back Side (TOP)



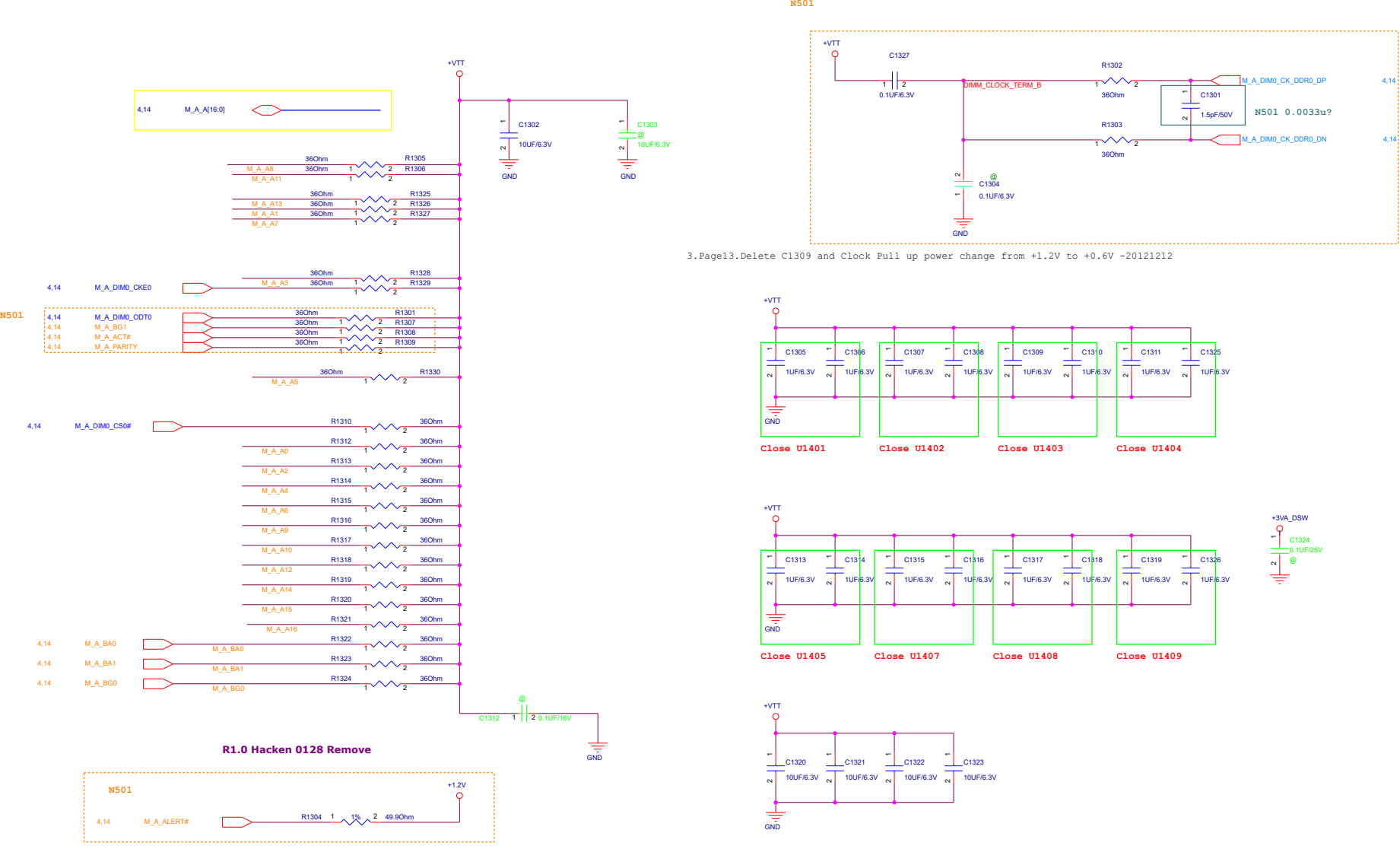


ASUS	Project Name: N501VW	Rev: 1.0
Title :	010_CPU_POWER_CAP	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 10 of 102	

Main Board

Main Board

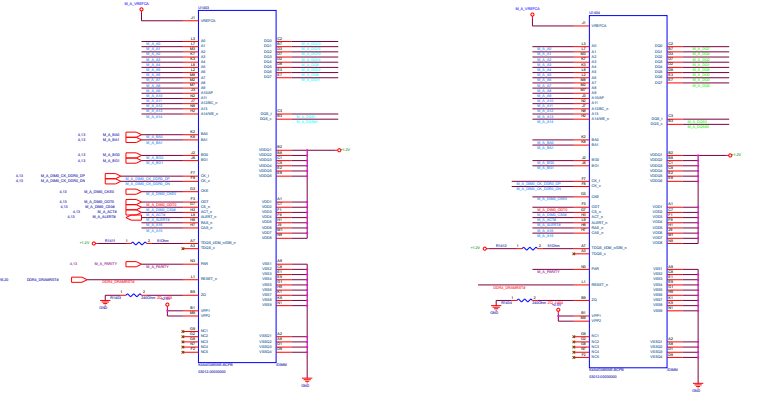
ASUS	Project Name: N501VW	Rev: 1.0
Title : Intel Alpine-Ridge		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, December 18, 2015	Sheet 11 of 102	

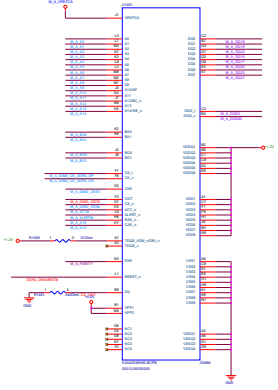


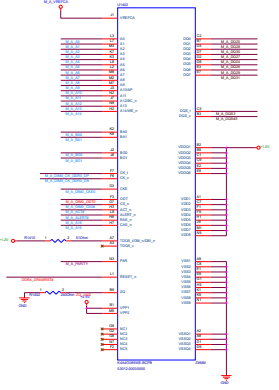
3.Page13.Delete C1309 and Clock Pull up power change from +1.2V to +0.6V -20121212

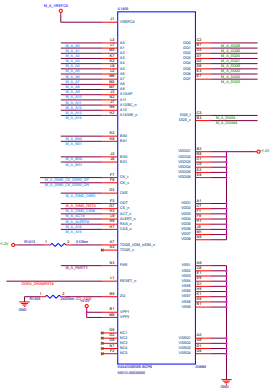
teknisi-indonesia

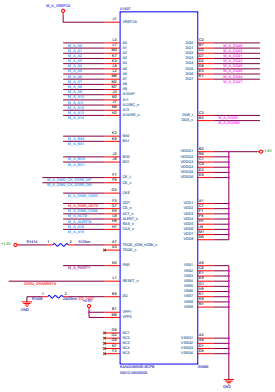
ASUSTeK COMPUTER INC.	Title : DDR4_TERMINATION	
	Engineer: EE	
Size: Custom	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 13 of 102	

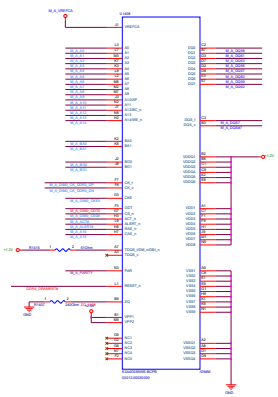


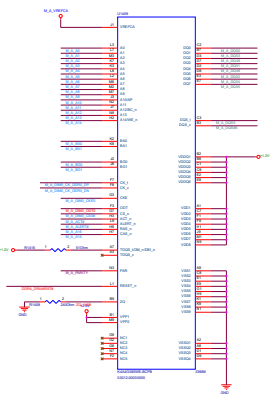


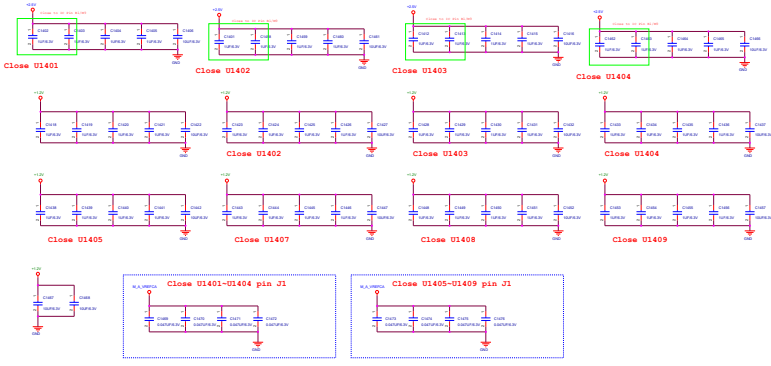








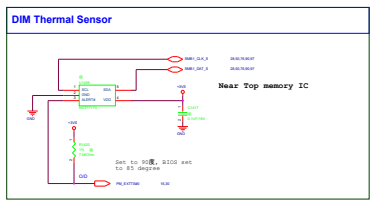


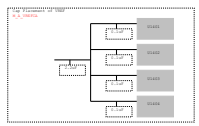

Close U1401
Close U1402
Close U1403
Close U1404

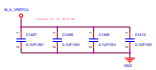
Close U1402
Close U1403
Close U1404

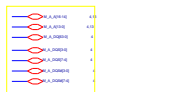
Close U1405
Close U1407
Close U1408
Close U1409

Close U1401~U1404 pin J1
Close U1405~U1409 pin J1


DIM Thermal Sensor
Near Top memory IC
Set to 90度, BIOS set to 85 degree





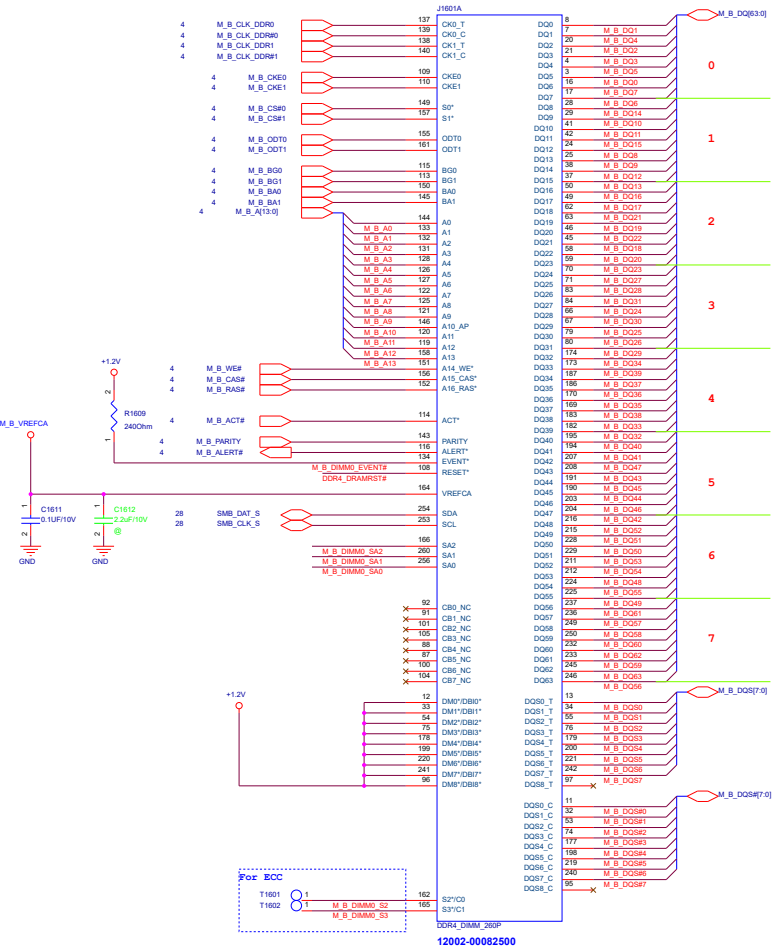


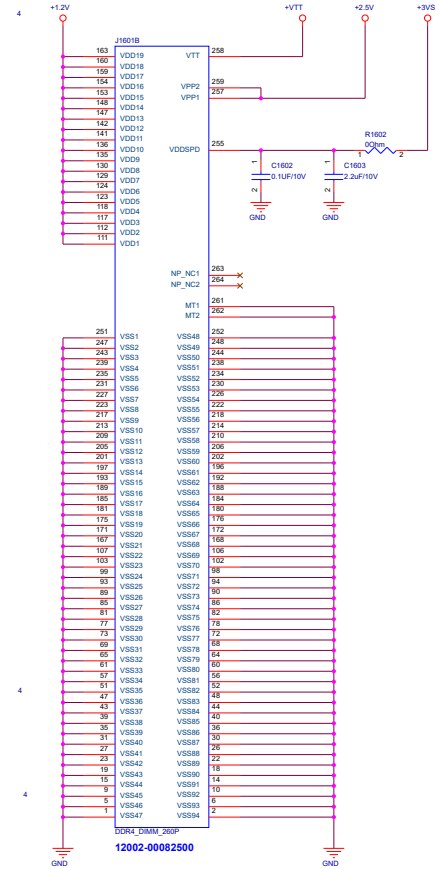
<Variant Name>

ASUSTeK COMPUTER INC.	Title : DDR4_ON-BOARD_A2	
	Engineer: EE	
Size: Custom	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 15 of 102	

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

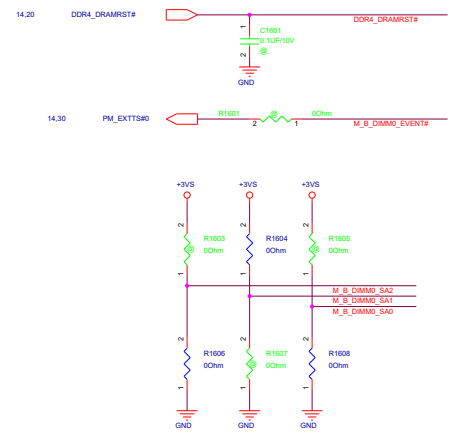
Main Board

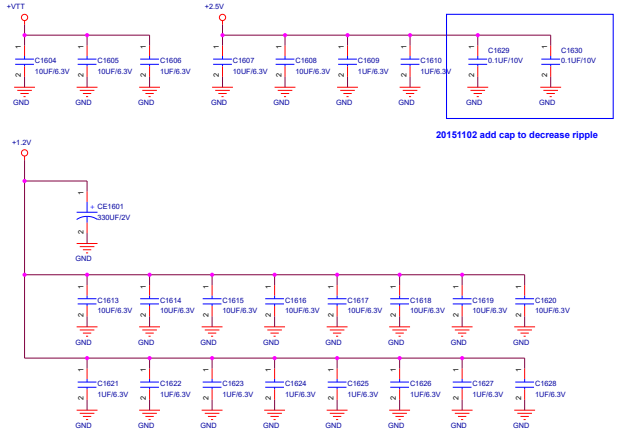




SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



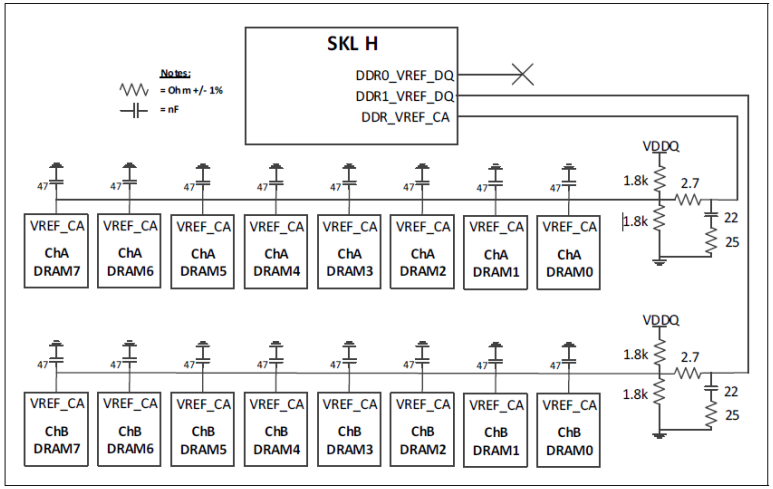


20151102 add cap to decrease ripple

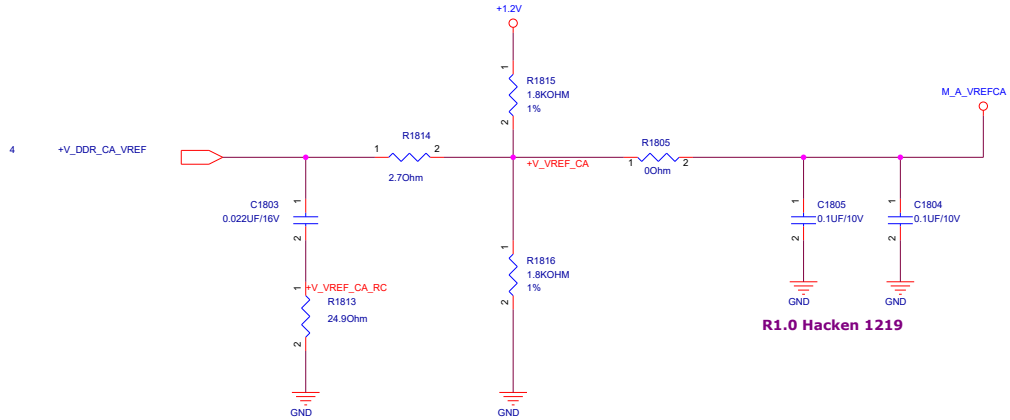
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: EE	
Size: A	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 17 of 102	

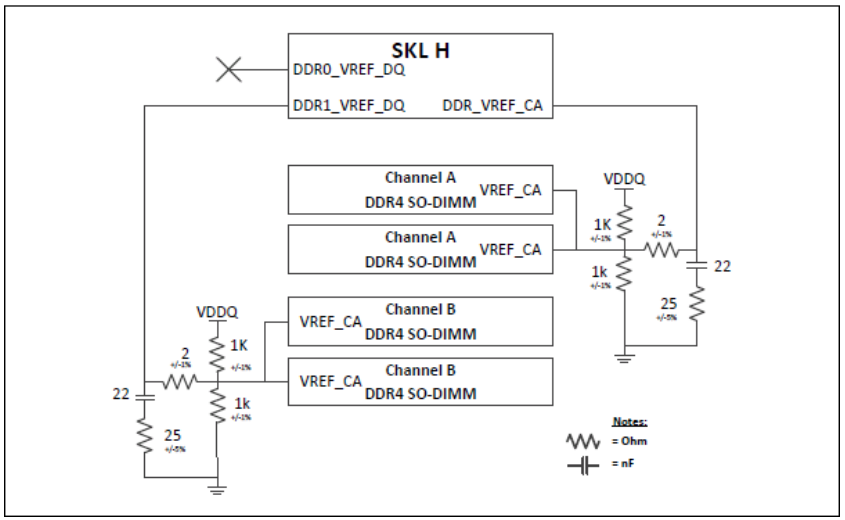
Figure 4-27. SKL H DDR4/DDR4-RS x8 Memory Down V_{REF-CA} Overview



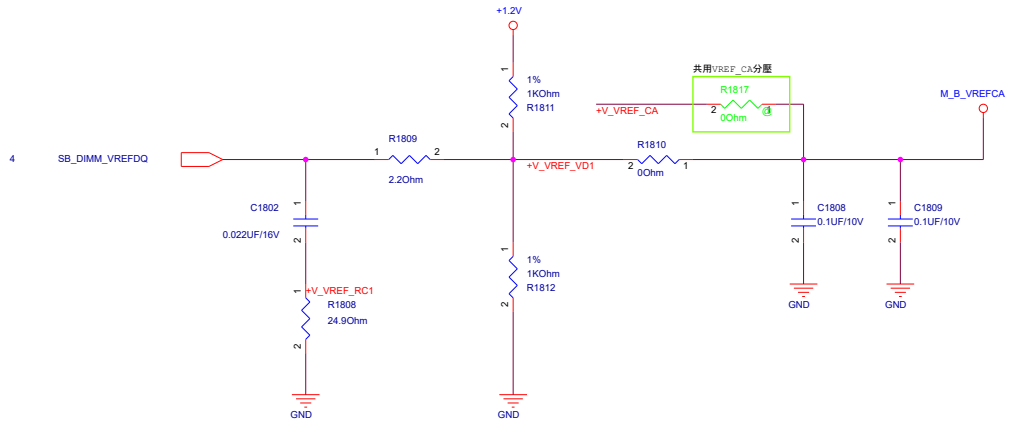
SO-DIMM0 Vref



SKL H DDR4/DDR4-RS SO-DIMM V_{REF-CA} Overview



SO-DIMM1 Vref



Project Name: N501VW		Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 18 of 102	

Title : *****

Engineer: EE

ASUSTeK COMPUTER INC. NB3

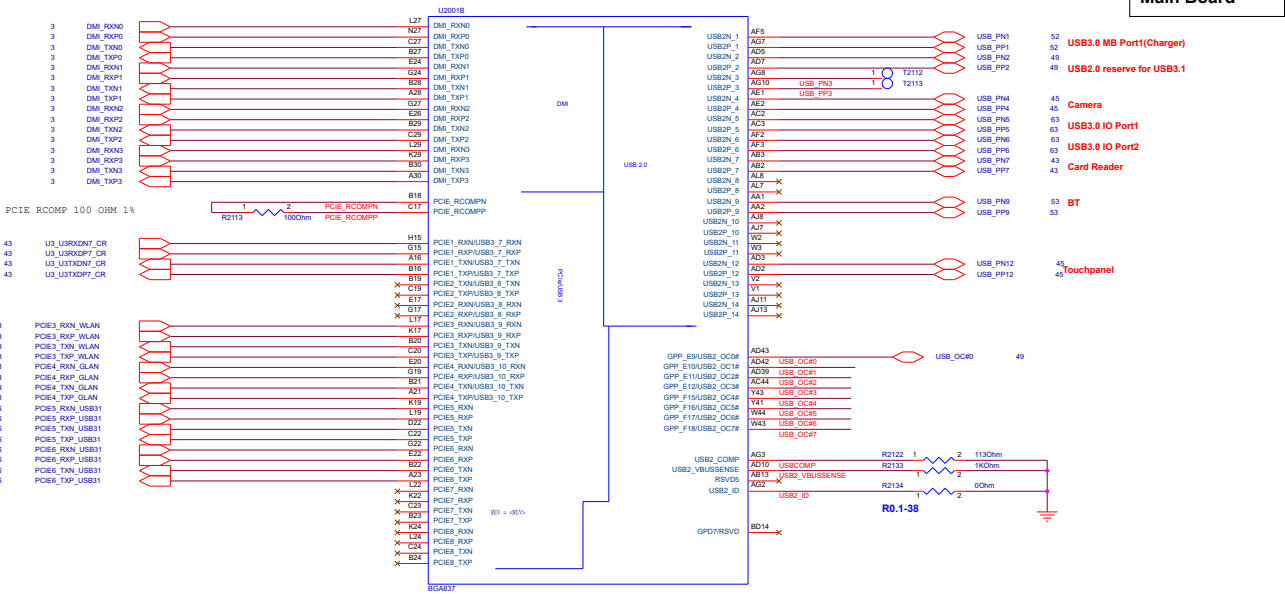
Size	Project Name	Rev
C	N501VW	1.0

Date:	Friday, December 18, 2015	Sheet	19	of	102

PCIE Setting

GL752VW PCIE Function define
Skylake HM170

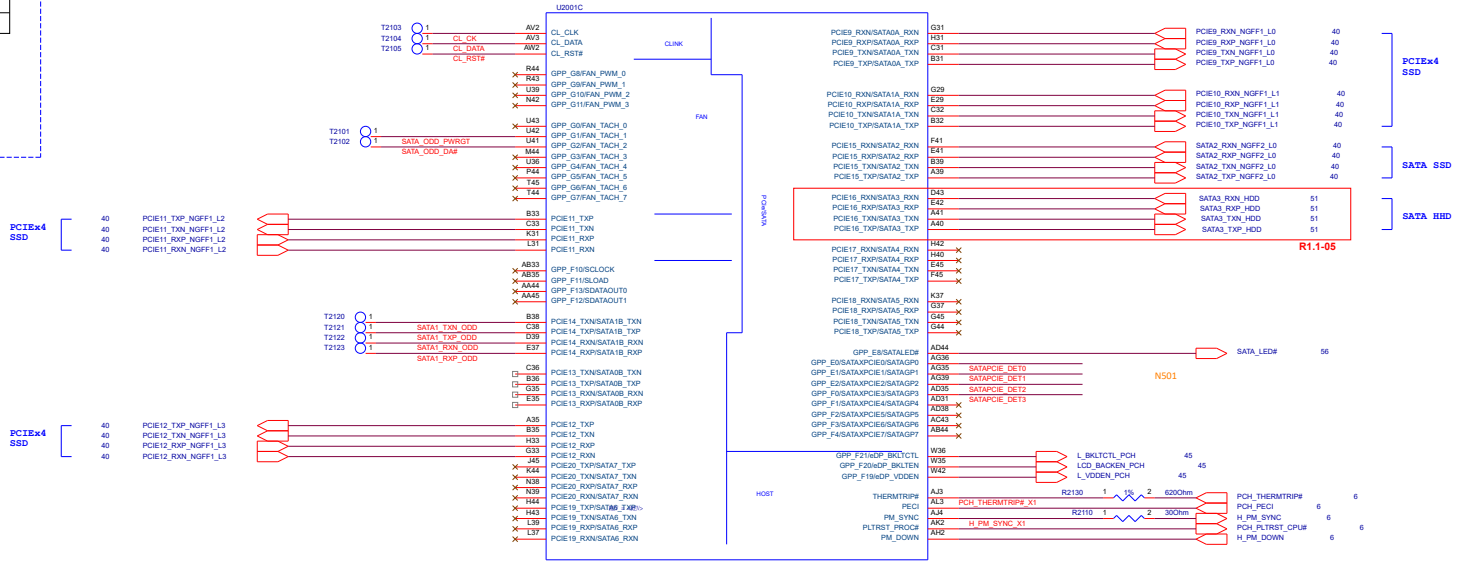
HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01	USB3.0 IO colay USB3.1	
03	USB3#03 / SSIC#02	USB3.0 IO colay USB3.1	
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06	USB3_IO	
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	SRC1
08	USB3#08 / PCIE#02	CardReader_PCIE/802.11AD(RSV)	SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN & CardReader	SRC4
11	PCIE#05 / GBE	USB 3.1	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	PCIE*4 SSD	SRC6
16	PCIE#10 / SATA#1		
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE	1st HDD	
20	PCIE#14 / SATA#1	ODD	
21	PCIE#15 / SATA#2	SATA SSD	
22	PCIE#16 / SATA#3		
23			
24			
25			
26			



USB Setting

N501VW USB Function define
Skylake HM170

USB 2.0	Function	USB 3.0	Function
USB2_01	USB3.0 MB Port1(Charger)	USB3_01	MB USB3.0 (Charger)
USB2_02	reserve for USB3.1	USB3_02	
USB2_03	reserve for USB3.1	USB3_03	
USB2_04	Camera	USB3_04	
USB2_05	USB3.0 IO Port1	USB3_05	USB3.0 IO Port1
USB2_06	USB3.0 IO Port2	USB3_06	USB3.0 IO Port2
USB2_07		USB3_07	
USB2_08		USB3_08	Card reader(PCIE)
USB2_09	BT		
USB2_10			
USB2_11			
USB2_12	Touchpanel		

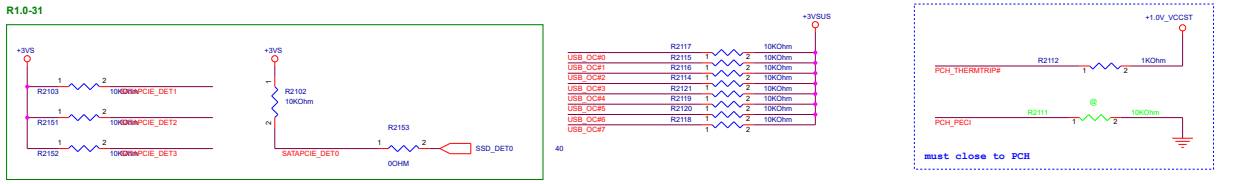


N501VW PCIE/SATA Function define

	Function
PCIE-01	
PCIE-02	Card Reader
PCIE-03	WLAN
PCIE-04	reserve
PCIE-05	TBT AR
PCIE-06	TBT AR
PCIE-07	TBT AR
PCIE-08	TBT AR
PCIE-09 (SATA-0A)	PCIE SSD
PCIE-10 (SATA-1A)	PCIE SSD
PCIE-11	PCIE SSD
PCIE-12	PCIE SSD

	Function
PCIE-13 (SATA-0B)	HDD
PCIE-14 (SATA-1B)	reserve
PCIE-15 (SATA-2)	SSD
PCIE-16 (SATA-3)	
PCIE-17 (SATA-4)	
PCIE-18 (SATA-5)	TBT AR
PCIE-19 (SATA-6)	PCIE SSD
PCIE-20 (SATA-7)	

	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	CR
CLKREQ-3	WLAN
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	



ASUS	Project Name: N501VW		Rev: 1.0
Title : PCH-CPT(2)_PCIE,CLK,USB			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, December 18, 2015	Sheet 21 of 102		

XTAL 24MHz

R1.1-08

C2201 /XTAL 22PF/25V
C2202 /XTAL 22PF/25V
XTAL24_IN_X1
XTAL24_OUT_X1
X2201 24Mhz /XTAL
XTAL 24MHZ 18PF/20PPM 3.2*2.5
R2211 0OHM XTAL24_IN
R2212 1MOhm
R2209 0OHM XTAL24_OUT
GND

RTC CRYSTAL 32.768KHz

C2203 15PF/50V
C2204 15PF/50V
SL2201 0402
X2202 32.768khz
R2210 10MOhm 5%
RTC_X1_X1
RTC_X1
RTC_X2
GND

2015.12.15 change cap base on vendor report

DGPU CLKReq#

+3VSUS
R2203 10KOhm
CLK_PEGA_REQ0#
For Optimus
2N7002K-T1-GE3 Q2201
25,70 DGPU_PWROK
GND

PCH CLKREQ Setting:

+3VSUS
R2214 10KOhm CLK_REQ1#
R2234 10KOhm CLK_REQ1#
R2219 10KOhm CLK_REQ2#
R2215 10KOhm CLKREQ3_WLAN#_X1
R2217 10KOhm CLKREQ4_GLAN#_X1
R2218 10KOhm CLKREQ5_NGFF1#_X1
R2235 10KOhm CLK_REQ7#
R2236 10KOhm CLK_REQ8#
CLK_REQ8#
R2202 10KOhm CLK_PEGA_REQ0#
GND
+3VSUS
R2216 10KOhm
CLKREQ5_USB31#_X1
R2261 10KOhm
GND

U2001G

GPP_A16/CLKOUT_48
T2211
GPP_A16
CLK_24M
CLK_24M#
R2262 0Ohm
R2263 0Ohm
CLK_CPU_BCLK
CLK_CPU_BCLK#
R2264 0Ohm
R2265 0Ohm
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
XTAL24_OUT
XTAL24_IN
+1.0VSUS_PCH
R2213 1% 2.7KOhm
XCLK_BIASREF
RTCX1
RTCX2
RTC_X1
RTC_X2
CLK_PEGA_REQ0#
R2222 0Ohm
CLK_PEGA_REQ0#_X1
CLKREQ3_WLAN#
R2206 0Ohm CLK_REQ2#
CLKREQ4_GLAN#
R2226 0Ohm CLKREQ3_WLAN#_X1
CLKREQ5_USB31#
R2256 0Ohm CLKREQ4_GLAN#_X1
CLKREQ6_NGFF1#
R2255 0Ohm CLKREQ5_USB31#_X1
CLKREQ6_NGFF1#_X1
CLK_REQ7#
CLK_REQ8#
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
CLKOUT_SRC_N15
CLKOUT_SRC_P15
CLKOUT_SRC_N14
CLKOUT_SRC_P14
CLKOUT_SRC_N13
CLKOUT_SRC_P13
CLKOUT_SRC_N12
CLKOUT_SRC_P12
BGA837

CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
CLK_ITP_BCLK_PCH#
CLK_ITP_BCLK_PCH
T2230
T2231
R2259 0Ohm
R2260 0Ohm
CLK_PCI_BCLK#
CLK_PCI_BCLK
PCH XDP 100 MHz

CLKOUT_SRC_N0
CLKOUT_SRC_P0
CLK0_PCIE_PEG#_VGA_X1
CLK0_PCIE_PEG_VGA_X1
R2223 0Ohm
R2224 0Ohm
CLK0_PCIE_PEG#_VGA
CLK0_PCIE_PEG_VGA
VGA 100 MHz

CLKOUT_SRC_N1
CLKOUT_SRC_P1
CLKOUT_SRC_N2
CLKOUT_SRC_P2
CLK2_PCIE_CR#_X1
CLK2_PCIE_CR_X1
T2203
T2204

CLKOUT_SRC_N3
CLKOUT_SRC_P3
CLK3_PCIE_WLAN#_X1
CLK3_PCIE_WLAN_X1
R2204 0Ohm
R2205 0Ohm
CLK3_PCIE_WLAN#
CLK3_PCIE_WLAN
PCIE#3 WLAN

CLKOUT_SRC_N4
CLKOUT_SRC_P4
CLK4_PCIE_GLAN#_X1
CLK4_PCIE_GLAN_X1
R2220 0Ohm
R2221 0Ohm
CLK4_PCIE_GLAN#
CLK4_PCIE_GLAN
PCIE#4 GLAN

CLKOUT_SRC_N5
CLKOUT_SRC_P5
CLK5_PCIE_USB31#_X1
CLK5_PCIE_USB31_X1
R2256 /USB31 0Ohm
R2257 /USB31 0Ohm
CLK5_PCIE_USB31#
CLK5_PCIE_USB31
PCIE#5-6 USB3.1

CLKOUT_SRC_N6
CLKOUT_SRC_P6
CLK6_PCIE_NGFF1#_X1
CLK6_PCIE_NGFF1_X1
R2228 0Ohm
R2229 0Ohm
CLK6_PCIE_NGFF1#
CLK6_PCIE_NGFF1
PCIE#9-12 NGFF1

CLKOUT_SRC_N7
CLKOUT_SRC_P7
CLKOUT_SRC_N8
CLKOUT_SRC_P8
CLKOUT_SRC_N9
CLKOUT_SRC_P9
CLKOUT_SRC_N10
CLKOUT_SRC_P10
CLKOUT_SRC_N11
CLKOUT_SRC_P11

teknisi-indonesia

U2001F

MB USB3.0 (Charger)
USB3.0 Port2 Colay USB3.1
USB3.0 IO Port2
USB3.0 IO Port1
USB3.0 Port2 Colay USB3.1

U3_U3TXDN1 U3_U3TXDP1 U3_U3RXDN1 U3_U3RXDP1
U3_U3TXDN2 U3_U3TXDP2 U3_U3RXDN2 U3_U3RXDP2
U3_U3TXDN6 U3_U3TXDP6 U3_U3RXDN6 U3_U3RXDP6
U3_U3TXDN5 U3_U3TXDP5 U3_U3RXDN5 U3_U3RXDP5
U3_U3TXDP3 U3_U3TXDN3 U3_U3RXDP3 U3_U3RXDN3

USB3_1_TXN USB3_1_TXP USB3_1_RXN USB3_1_RXP
USB3_2_TXN/SSIC_1_TXN USB3_2_TXP/SSIC_1_TXP
USB3_2_RXN/SSIC_1_RXN USB3_2_RXP/SSIC_1_RXP
USB3_6_TXN USB3_6_TXP USB3_6_RXN USB3_6_RXP
USB3_5_TXN USB3_5_TXP USB3_5_RXN USB3_5_RXP
USB3_3_TXP/SSIC_2_TXP USB3_3_TXN/SSIC_2_TXN
USB3_3_RXP/SSIC_2_RXP USB3_3_RXN/SSIC_2_RXN
USB3_4_TXP USB3_4_TXN USB3_4_RXN

GPP_A1/LAD0/ESPI_IO0 GPP_A2/LAD1/ESPI_IO1 GPP_A3/LAD2/ESPI_IO2 GPP_A4/LAD3/ESPI_IO3
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3
GPP_A5/LFRAME#/ESPI_CS0# GPP_A6/SERIRQ/ESPI_CS1#
LPC_FRAME# INT_SERIRQ
GPP_A7/PIRQA#/ESPI_ALERT0# GPP_A0/RCIN#/ESPI_ALERT1#
PCI_INTA# RC_IN#
GPP_A14/SUS_STAT#/ESPI_RESET# PCH_SUS_STAT#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
R2245 22Ohm R2201 22Ohm
CLK_KBCPCI_PCH_X1
CLK_DEBUG_X1
CLK_KBCPCI_PCH
CLK_DEBUG
GPP_G19/SM#
GPP_G18/NM#
T2201 T2202
PCH_GPP_G19
PCH_GPP_G18
GPP_E6/DEVSLP2 GPP_E5/DEVSLP1 GPP_E4/DEVSLP0 GPP_F9/DEVSLP7 GPP_F8/DEVSLP6 GPP_F7/DEVSLP5 GPP_F6/DEVSLP4 GPP_F5/DEVSLP3
NGFF2_DEVSLP SATA1_DEVSLP
NGFF2_DEVSLP NGFF0_DEVSLP
SATA3_HDD_DEVSLP

BGA837

R1.1-05 R0.1-43

SATA3_HDD_DEVSLP R2251 N/A 10KOhm
NGFF2_DEVSLP R2252 N/A 10KOhm
SATA1_DEVSLP R2253 N/A 10KOhm
NGFF0_DEVSLP R2243 N/A 10KOhm
+3VS

PCI_INTA# R2208 10KOhm
INT_SERIRQ R2246 10KOhm
+3VS

Project Name	N501VW	Rev 1.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR	
Size Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 22 of 102	

HPD0 to DP

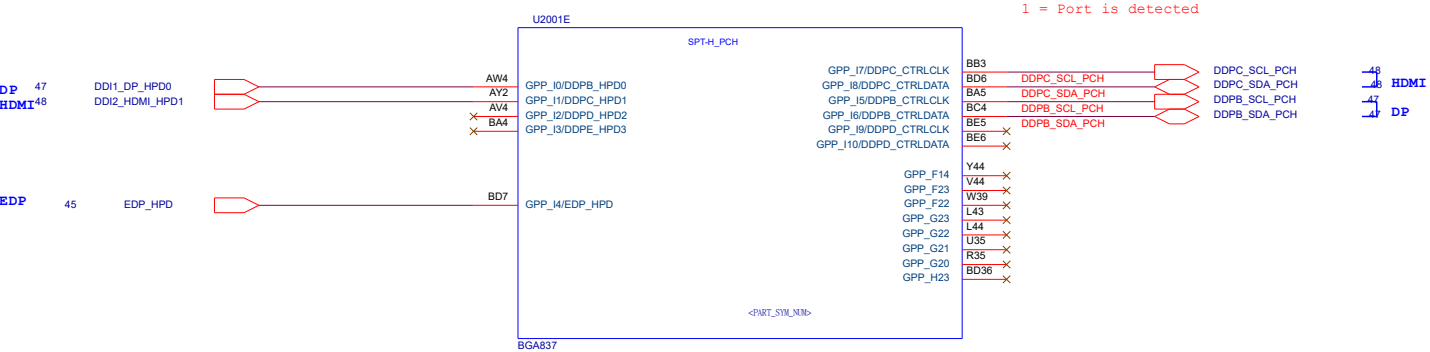
HPD1 to HDMI

HPD2 to TBT

HPD3 to VGA

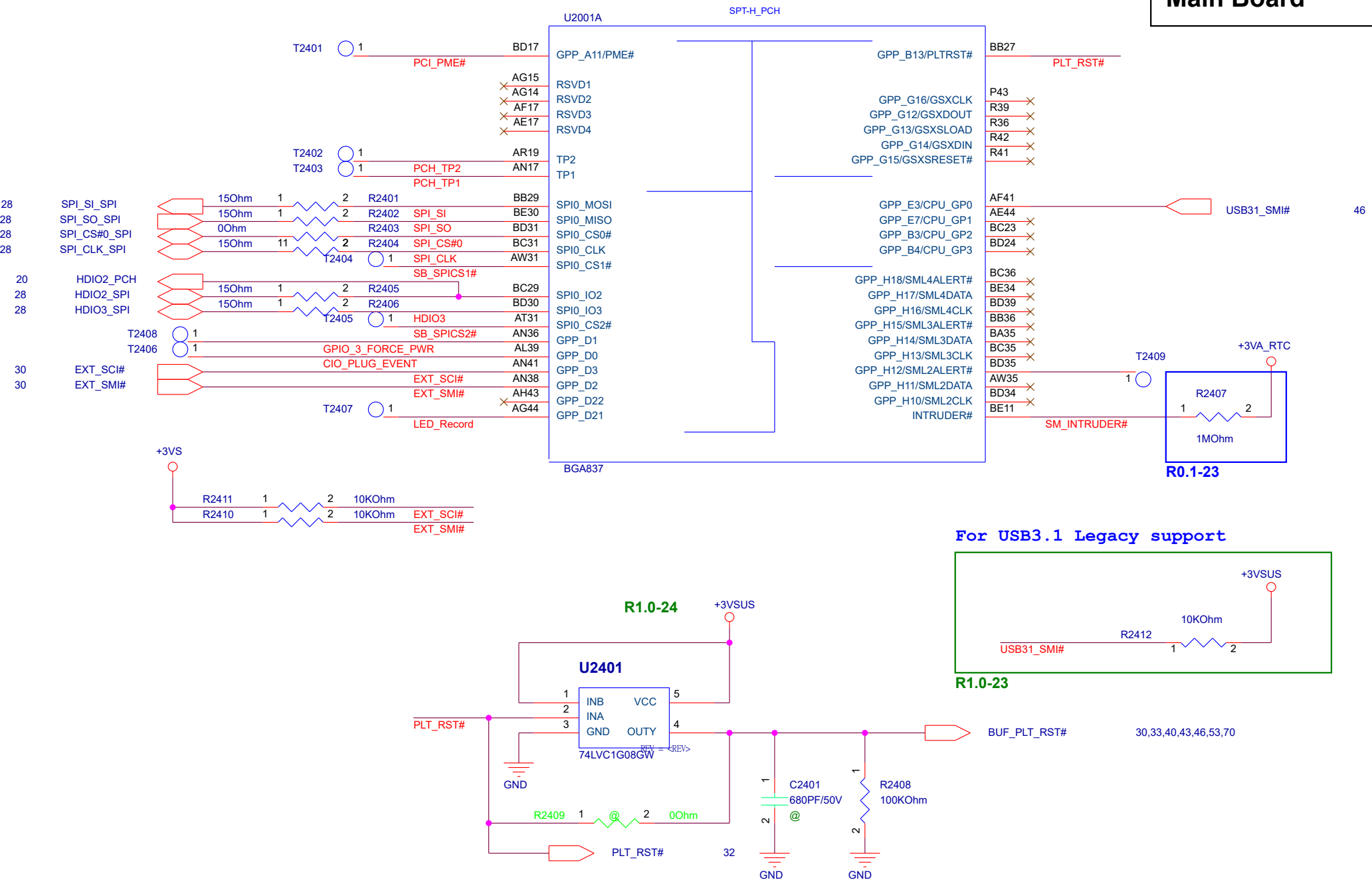
HPD4 to EDP Panel

DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected



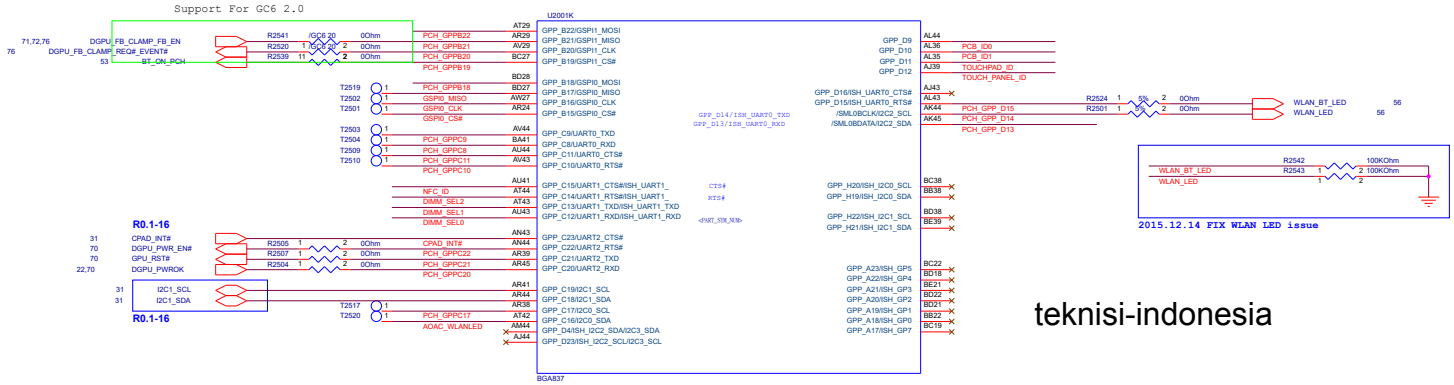
REV = <REV>

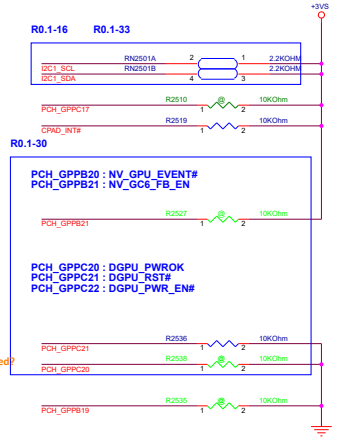
Project Name: N501VW		Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 23 of 102	

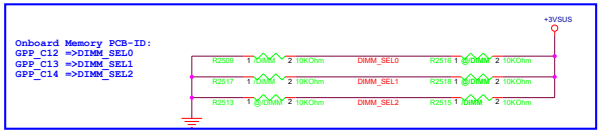


For USB3.1 Legacy support

Project Name: N501VW		Rev: 1.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 24 of 102	

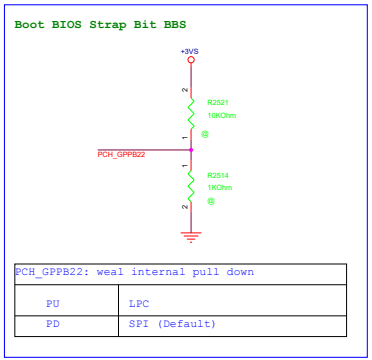


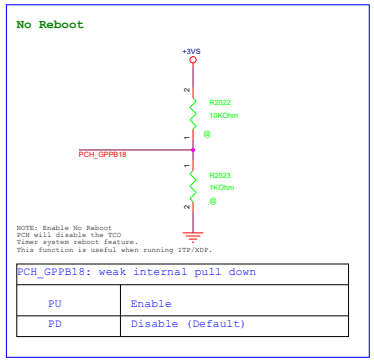




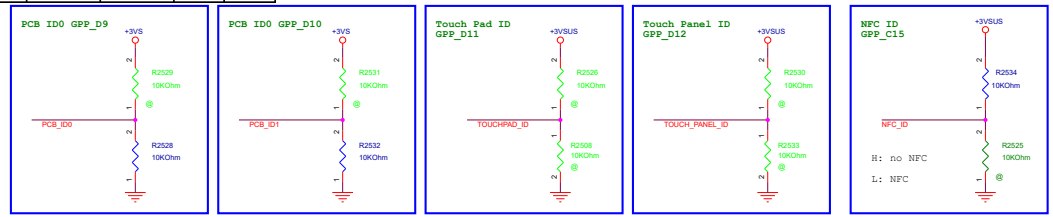
151030 Add new RAM source Micron

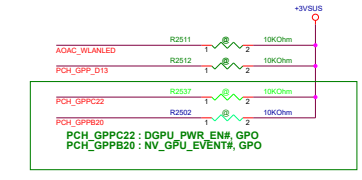
	MIcron (8Gb)	Samsung (8Gb)		
	03012-00030100 DDR4 2400 1024M*8 1.2V MT40A1G8PM-083E:A	03012-00030000 DDR4 2133 1024M*8 1.2V FBGA78 K4A8G085WB-BCPB		
DIMM_SEL0	H	L		
DIMM_SEL1	L	L		
DIMM_SEL2	H	H		





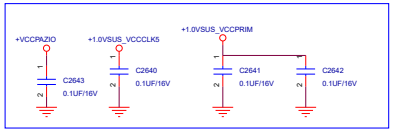
				DIMM_SEL0 (GPP_C12)	DIMM_SEL1 (GPP_C13)	DIMM_SEL2 (GPP_C14)	Stuff	Unstuff
4G	03012-00010100	DDR4 2133 512M*8 1.2V FBGA78	MICRON	L	L	L	R2509	R2516
							R2513	R2518
							R2517	R2515
	03012-00010200	DDR4 2133 512M*8 1.2V FBGA78	SAMSUNG	H	L	L	R2513	R2509
							R2516	R2518
							R2517	R2515
8G	03012-00030000	DDR4 2133 1024M*8 1.2V FBGA78	SAMSUNG	L	L	H	R2509	R2513
							R2515	R2516
							R2517	R2518

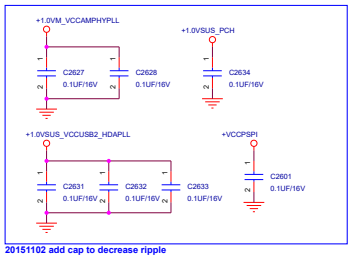




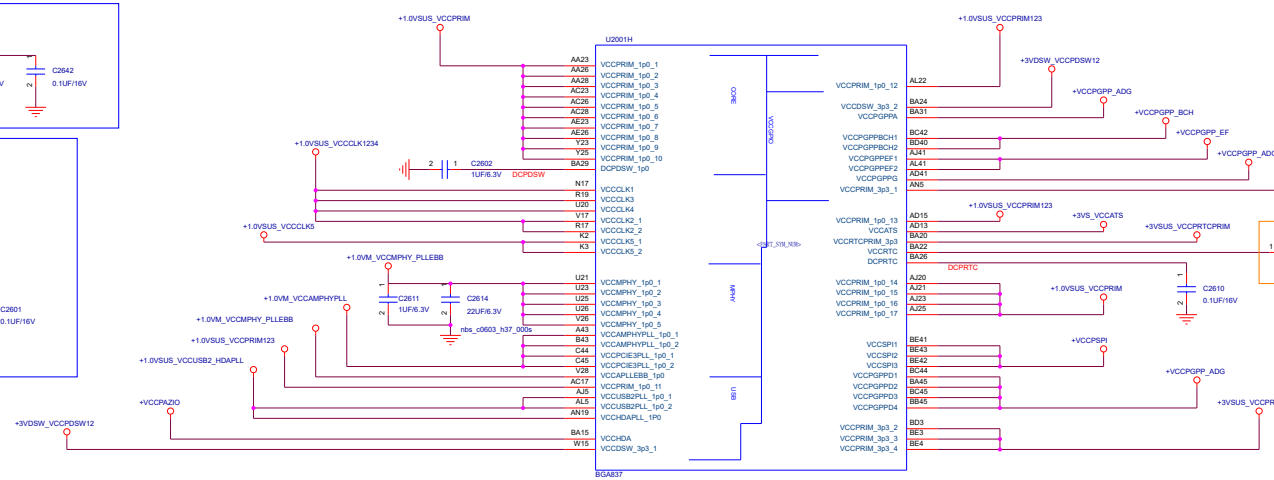
ASUS	Project Name: N501VW	Rev: 1.0
Title :	PCH-CPT(6)_GPIO,MISC	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 25 of 102	

151015 靠近PCH擺放

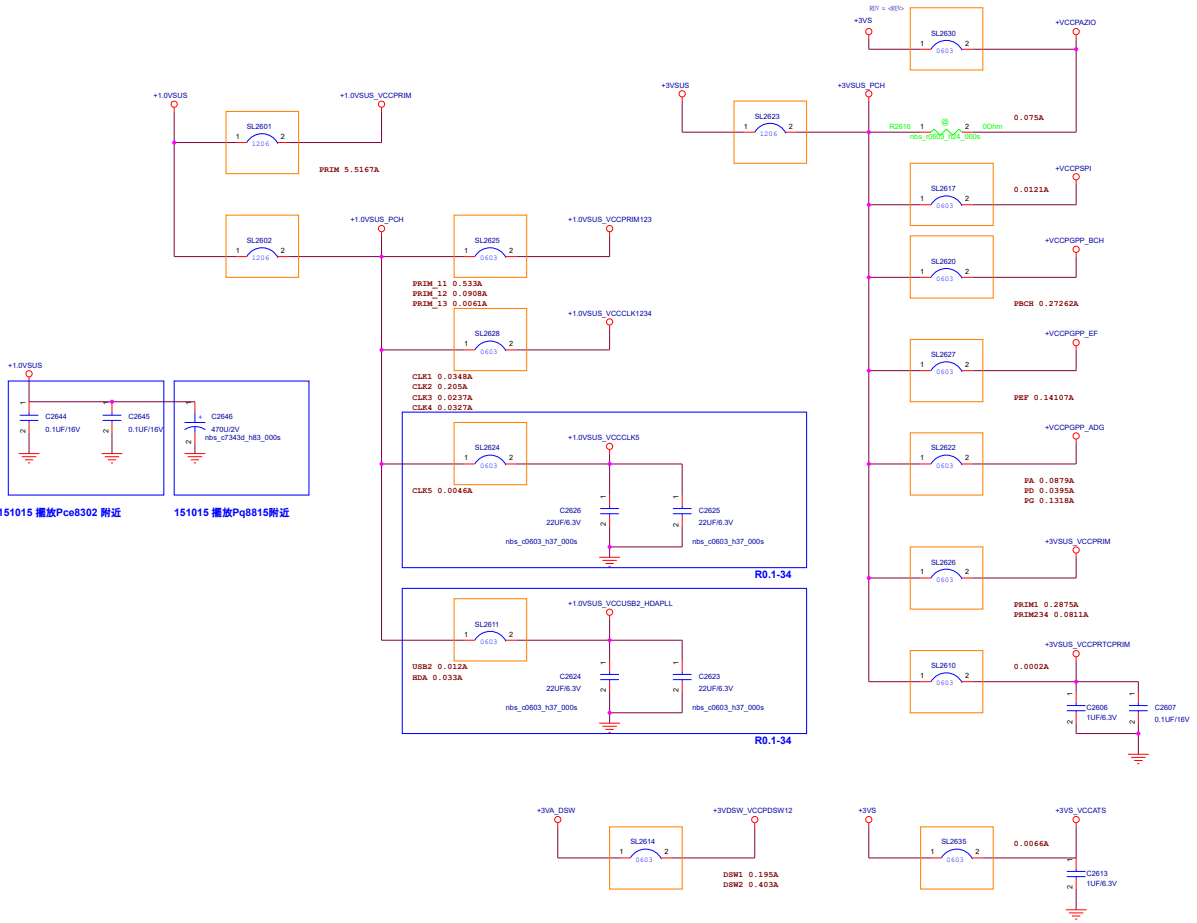




20151102 add cap to decrease ripple

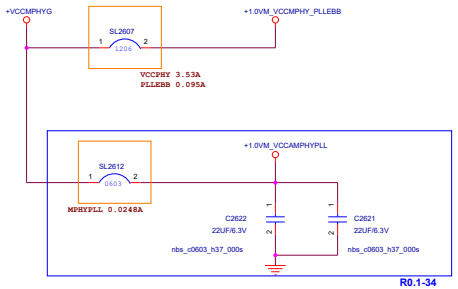


151030 modify shortland for decrease voltage drop



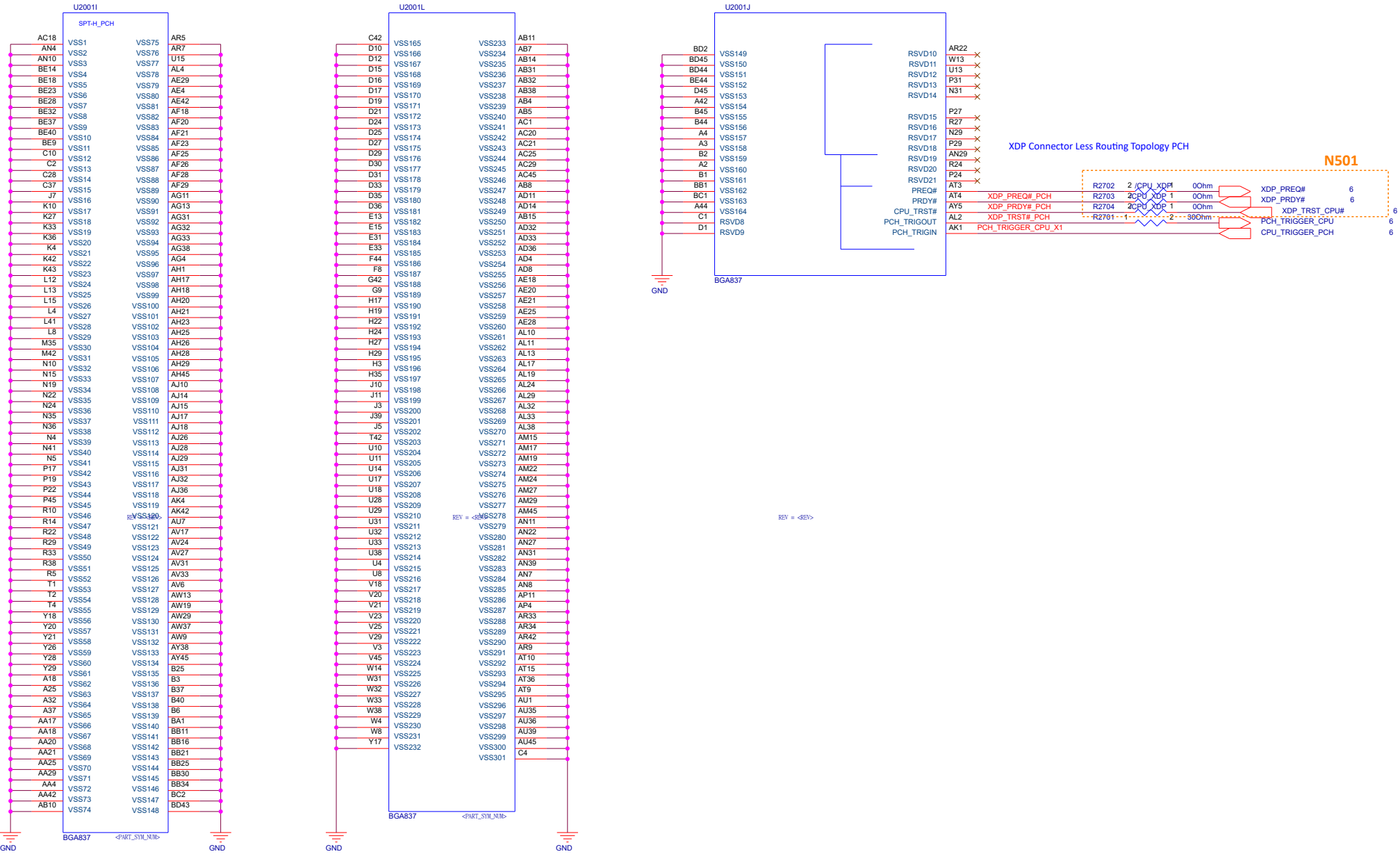
151015 擺放Pce8302 附近

151015 擺放Pq8815附近



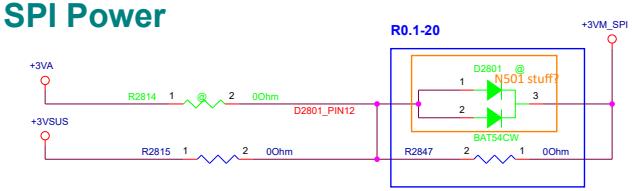
Supply	Value	Quantity	Type	Notes	Placement
VccMPHYPLL & VccPCIE3PLL (Pin A43, B43, C44, C45) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	Recommended to be placed <3 mm from edge of package
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccUSB2PLL & VccHDAPLL (Pin AJ5, AL5, AN19) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccCLK5 (Pin K2, K3) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	

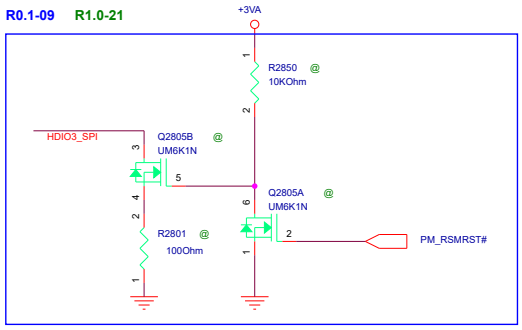
ASUS	Project Name N501VW		Rev 1.0
Title : PCH-CPT(7)_POWER,GND			
Size C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, December 18, 2015	Sheet 26 of 102		



Project Name: N501VW		Rev: 1.0
Title : PCH-CPT(8)_POWER,GND		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 27 of 102	

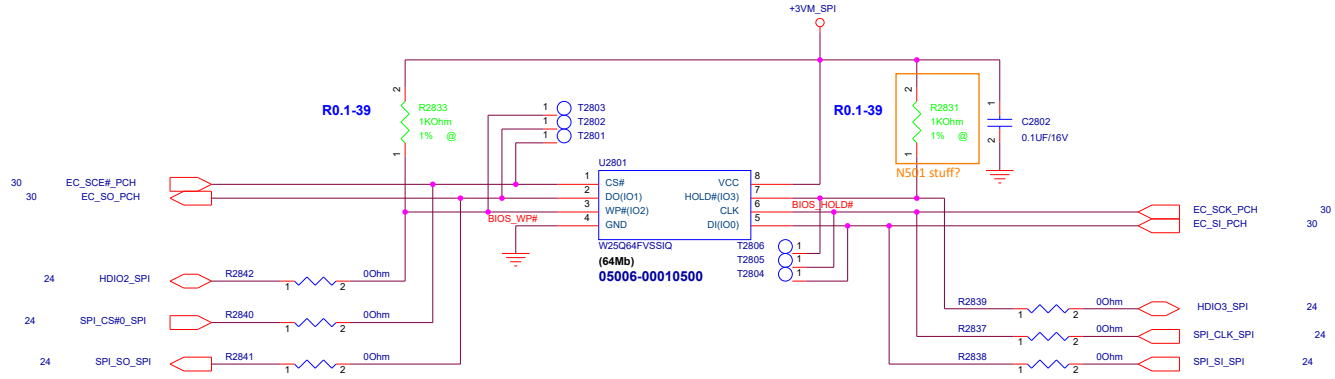
SPI Power



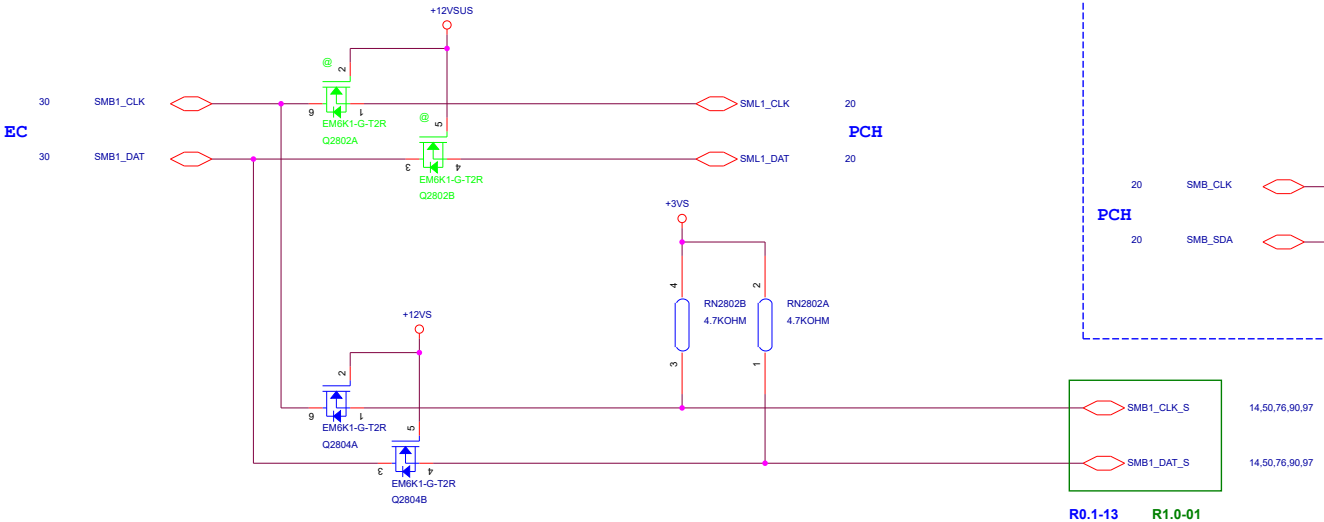


1st SPI ROM

Main: 05006-00010500 (fixed quad bit)



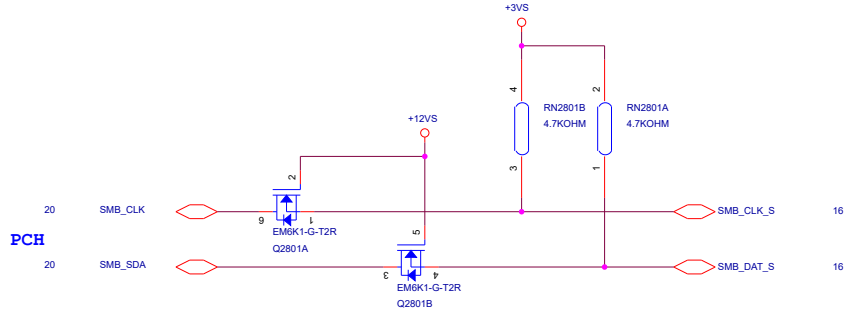
System Management Interface



R0.1-13 R1.0-01

CPU,VGA Thermal Sensor
Power Thermal Sensor

SMBus Interface



Project Name: N501VW		Rev: 1.0
Title : PCH-SPI ROM,OTH		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 28 of 102	

Main Board

ASUS	Project Name: N501VW	Rev: 1.0
Title : PCH-XDP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 29 of 102	

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8995E/AX	06037-00050400

Power

R1.0-29

+3VS, +3VA_EC, +3VPLL, +3VACC, +3VADSW, EC_AGND

C3002 0.1UF/16V
C3051 0.1UF/16V
C3052 0.1UF/16V
C3053 0.1UF/16V
C3054 0.1UF/16V
C3004 0.1UF/16V
C3005 0.1UF/16V
C3007 0.1UF/16V
C3001 0.1UF/16V
C3008 0.1UF/16V
SL3005 1603
SL3006 SHORTPIN
SL3007 SHORTPIN

PU/PD

+3VA

PWR_SW# 100KOhm R3037
AC_IN_OC# 100KOhm R3042
LID_SW# 100KOhm R3063

+3VA_EC

CHG_LED# R3043 10KOhm
CHG_FULL_LED# R3044 10KOhm
PM_EXTTS#0 R3001 10KOhm
THRO_CPU# R3032 10KOhm
PWRLIMIT_EC# R3021 100KOhm

SMB1_DAT RN3001A 4.7KOhm
SMB1_CLK RN3001B 4.7KOhm
P_SMB0_CLK RN3001D 4.7KOhm
P_SMB0_DAT RN3001C 4.7KOhm
P_SMB3_DAT RN3002A 4.7KOhm
P_SMB3_CLK RN3002B 4.7KOhm

3VADSW_ON R3053 100KOhm
5VSUS_ON R3056 1MOhm
VSUS_ON R3030 1MOhm

for load code

ClickPad Schematic

TP_DAT RN3004A 4.7KOhm
TP_CLK RN3004B 4.7KOhm

+3VSUS

PM_PWRBTN# R3041 10KOhm
RC_IN# R3003 10KOhm

N501

BAT1_IN_OC# R3065 100KOhm
R3008 100KOhm

PM_SUSC# R3004 100KOhm
PM_SUSB# R3005 100KOhm
SUSB_EC# R3092 4.7KOhm
SUSC_EC# R3093 4.7KOhm
EC_SCK R3002 10KOhm
EC_SCE# R3011 10KOhm
EC_SO R3007 10KOhm
EC_SI R3013 10KOhm
R3058 10KOhm

R0.1-42

U3001

LCD_BACKOFF# 45

+3VA_EC, +3VPLL, +3VS, +3VACC

IT8995E-128/CX
06037-00050500

LPC: LPC_AD0, LPC_AD1, LPC_AD2, LPC_AD3, CLK_KBCPCI_PCH, LPC_FRAME#, BUF_PLT_RST#, INT_SERIRQ, EXT_SMI#, EXT_SCI#, RC_IN#, EC_RST#

FLASH ROM: DGPU_LIMIT, EC_SCK_PCH, EC_SO_PCH, EC_SI_PCH, EC_SCE#_PCH, PWRLIMIT_EC#

KBMX: KSI0~KSI7, KSO0~KSO15

PSY2: PM_PWRBTN#, PM_SUSC#, 5VSUS_ON, VSUS_ON, P_SMB0_CLK, P_SMB0_DAT, TP_CLK, TP_DAT

SWBAK: PWR_SW#, PS_ON_EC, SMB1_CLK, SMB1_DAT, PECI_EC, PCH_SPI_OV

GPIO: PWR_LED, CHG_LED#, CHG_FULL_LED#, FAN1_PWM, FAN0_PWM, KB_LED_PWM, AC_IN_OC#, LID_SW#, NUM_LED#, PM_EXTTS#0, BAT1_IN_OC#, PCH_SLP_S0#, ME_AC_PRESENT, OP_SD#, FAN0_TACH, FAN1_TACH, SUSB_EC#, SUSC_EC#, 1.2V_ON, PM_SUSB#, CAP_LED#, THRO_CPU#, PCH_SUSACK#, PM_CLKRUN#, PM_RSMRST#, DPWROK_EC, PM_PWROK, PM_SYSPWROK, 3VSUS_PWRGD, ALL_SYSTEM_PWRGD, IMVP8_PWRGD, A/D_MAX_POWER, MB_MAX_POWER, USB31_5VBUS#, 3VADSW_ON, PCH_SUS_STAT#

PM_SLP_SUS# R0.1-41, SUSWARN# R0.1-41

Battery

Thermal sensor

For EMI

2015.08.21 EMI Modify

C3012 EC_RST# 100PF/50V
C3013 PM_SYSPWROK 100PF/50V
C3014 PM_PWROK 100PF/50V
C3015 DPWROK_EC 100PF/50V
C3031 RC_IN# 100PF/50V
C3023 3VSUS_PWRGD 100PF/50V
C3024 KB_LED_PWM 100PF/50V
C3025 CHG_FULL_LED# 100PF/50V
C3026 PWR_LED 100PF/50V
C3027 CHG_LED# 100PF/50V
C3028 NUM_LED# 100PF/50V
C3029 ALL_SYSTEM_PWRGD 100PF/50V
C3030 IMVP8_PWRGD 100PF/50V

For EMI

2015.08.21 EMI Modify

C3019 3VADSW_ON 15PF/50V
C3020 A/D_MAX_POWER 33PF/50V
C3021 MB_MAX_POWER 33PF/50V

Close U3001

C3018 CLK_KBCPCI_PCH 8.2PF/50V
C3011 BAT1_IN_OC# 0.01UF/16V
C3010 PWR_SW# 0.01UF/16V
C3009 BUF_PLT_RST# 0.01UF/16V

R1.0-34

+3VA_DSW, +3VS

R3055 100KOhm
R3054 100KOhm
3VA_DSW_PWRGD
IMVP8_PWRGD
3VA_DSW_PWRGD_EC
R3052 0Ohm

R1.0-25 R1.0-38 To CC logic at p49

INTB# ID# USB31_5VBUS#
EC_GPC4 EC_GPJ6 EC_GPJ0
R3096 R3095 R3061 10KOhm

<Variant Name>

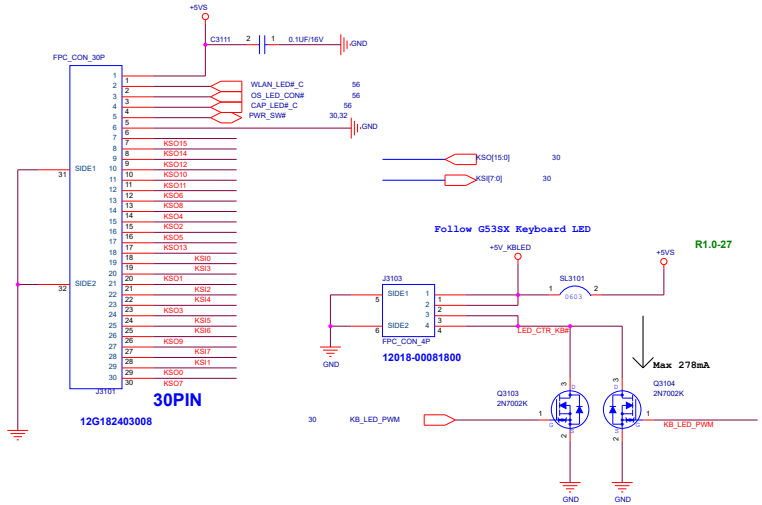
ASUSTeK COMPUTER

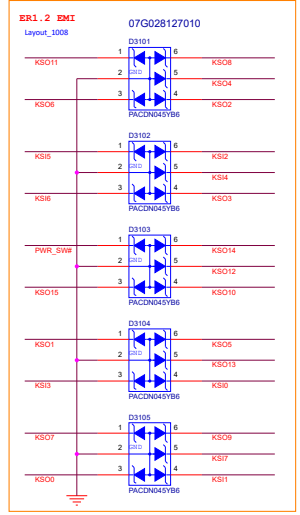
Title : CR_KBC_IT8521
Engineer: EE

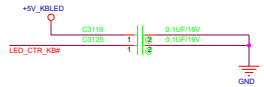
Size	Project Name	Rev
C	N501VW	1.0

Date: Friday, December 18, 2015 Sheet 30 of 102

Keyboard Connector

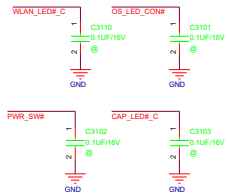




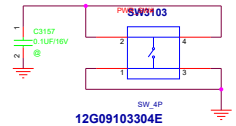


R1.1-4/13-5

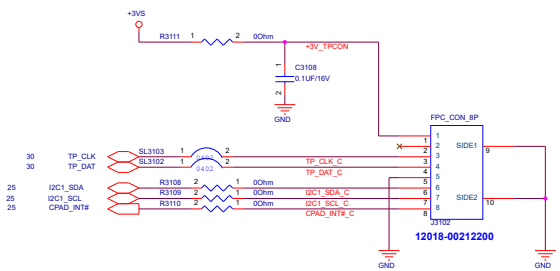
D3102~D317 ESD PROTECTION AZ2115-05C
1st Source: P/N:07G028162010 NXP SOT363
2nd Source: P/N:07G028127010 AMAZING SC70-6L



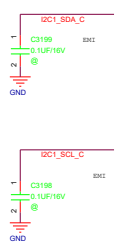
POWER button for SR

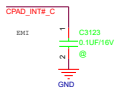


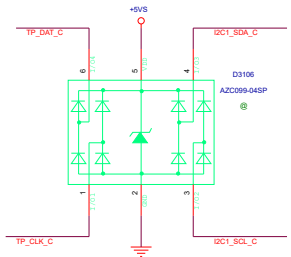
Click touch Pad Connector



Reserved for EMI



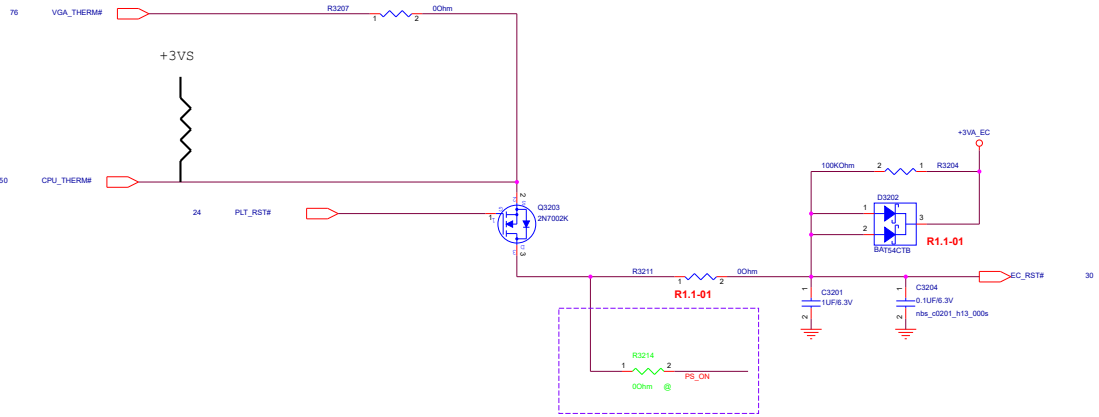




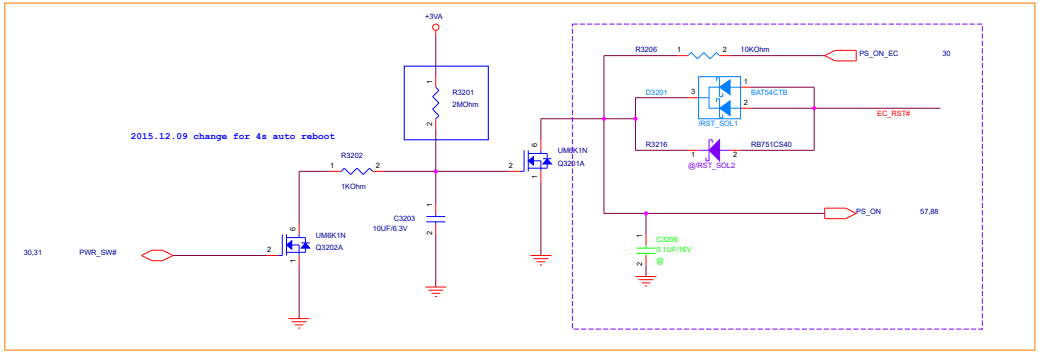
ASUSTeK COMPUTER	Title :	KBC_KB & TP	
	Engineer:	EE	
Size: C	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 31 of 102		

Reset Circuit

Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



Battery embedded (press pwr_sw 10sec, then reset ec)



EC power off solution:
Solution1 Mount R3206, D3201/ Unmount R3216
Solution2 Mount R3206/R3216/ Unmount D3201- for reserved 0402 footprint

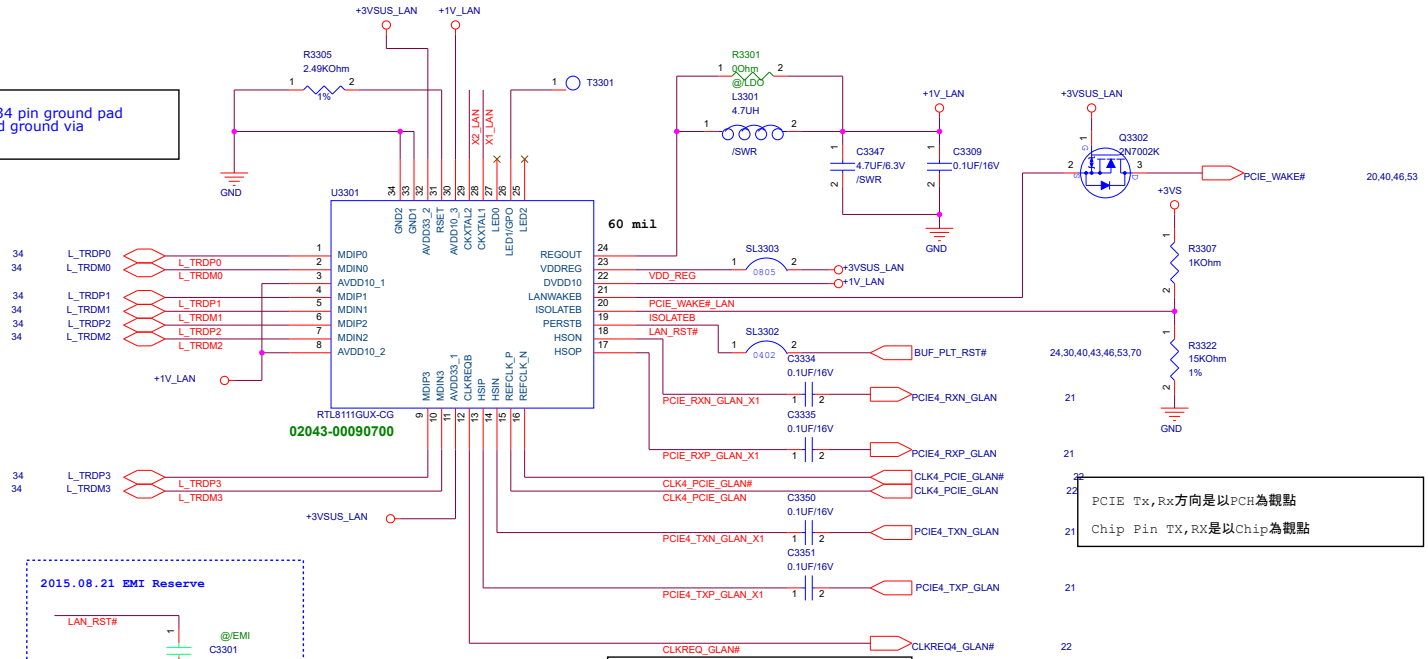
R1.2-65

ASUSTeK COMPUTER	Title :	RST_Reset Circuit	
	Engineer:	EE	
Size: B	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 32 of 102		

The distance from U3301.24 to L3301 within 200 mil.

The distance from L3301 to C3347 within 200 mil.

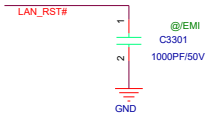
33/34 pin ground pad
need ground via



PCIE Tx,Rx方向是以PCH為觀點

Chip Pin TX,RX是以Chip為觀點

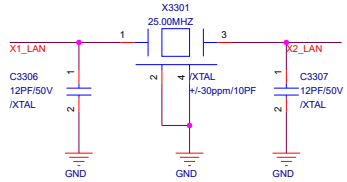
2015.08.21 EMI Reserve



CLKREQ_GLAN#, PCIE_WAKE#
should be PU on the host side

teknisi-indonesia

07G010272501

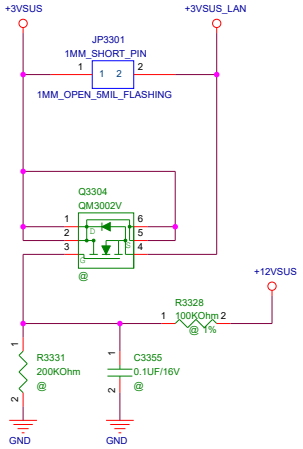


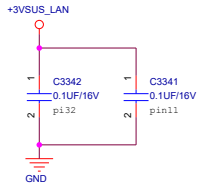
X3301: 25MHZ +/-30ppm/10pF (3225)

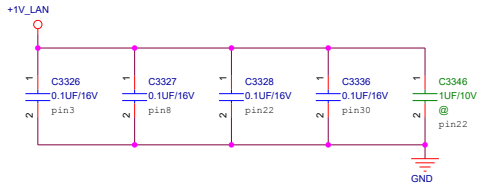
1st: P/N:07G010272501 TXC/7V25000011

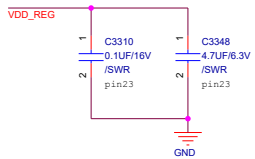
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms



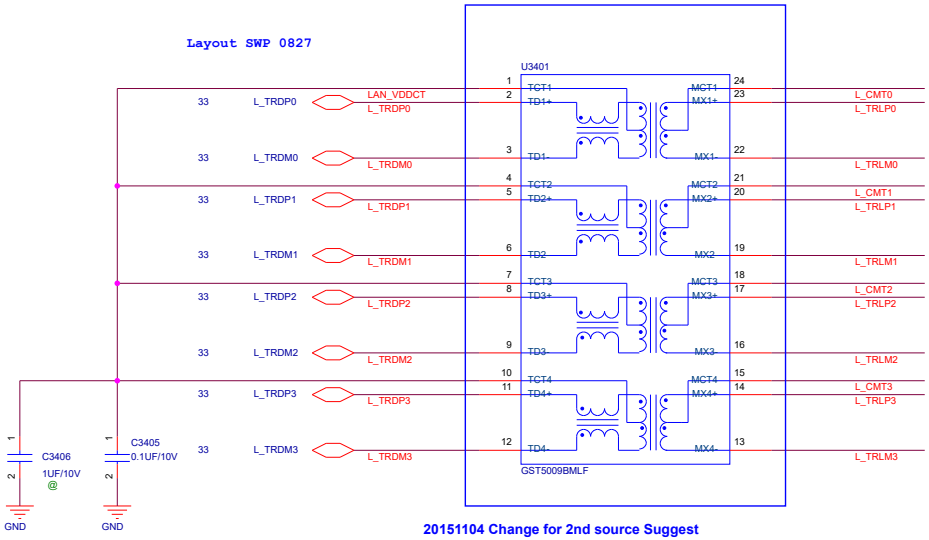






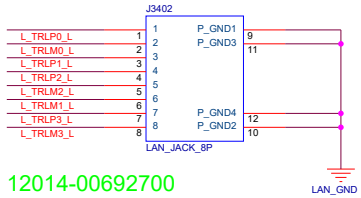
C3348, C3310 close to pin 23
reserved for SWR mode

ASUS	Project Name: GL502VT		Rev: 1.0
Title : LAN RTL8111GUX-CG			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Friday, December 18, 2015		Sheet 33 of 102	



20151104 Change for 2nd source Suggest

LAN Connector



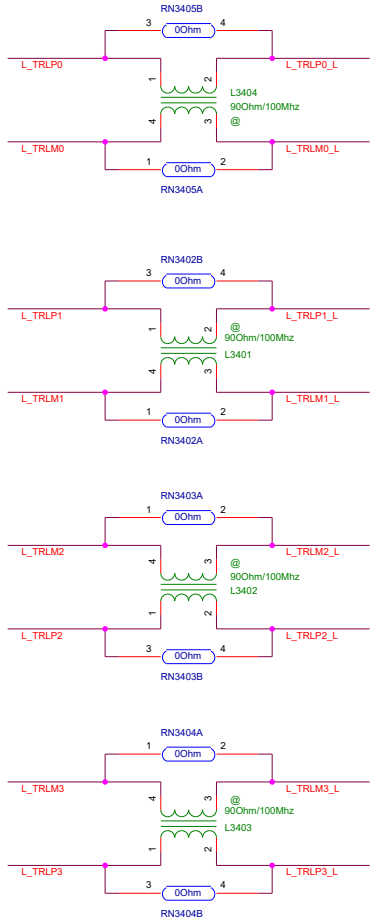
12014-00692700

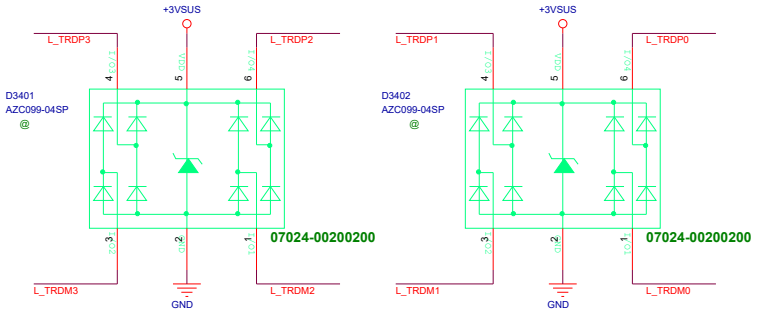
J3402 LAN Jack

1st Source: P/N:12014-00161700 FOXCONN/JM3611-NS640003-7H

2nd Source: P/N:12014-00035500 SINGATRON/2RJ1648-000111F

J3402 SR2
P/N : 12014-00692700

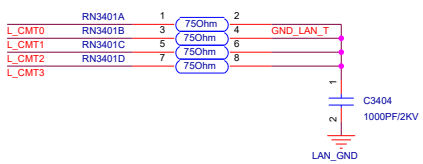




D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

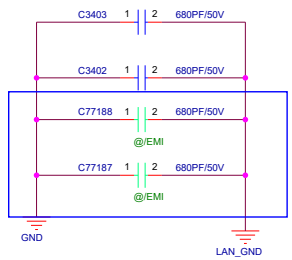
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



GND_LAN_T 上禁止加任何零件

2015.12.16 EMI Reserve

2012/2/16 EMI



Place near chassis GND

Project Name: GL502VT		Rev: 1.0
Title : LAN RJ45 Conn.		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li
Date: Friday, December 18, 2015	Sheet 34 of 102	

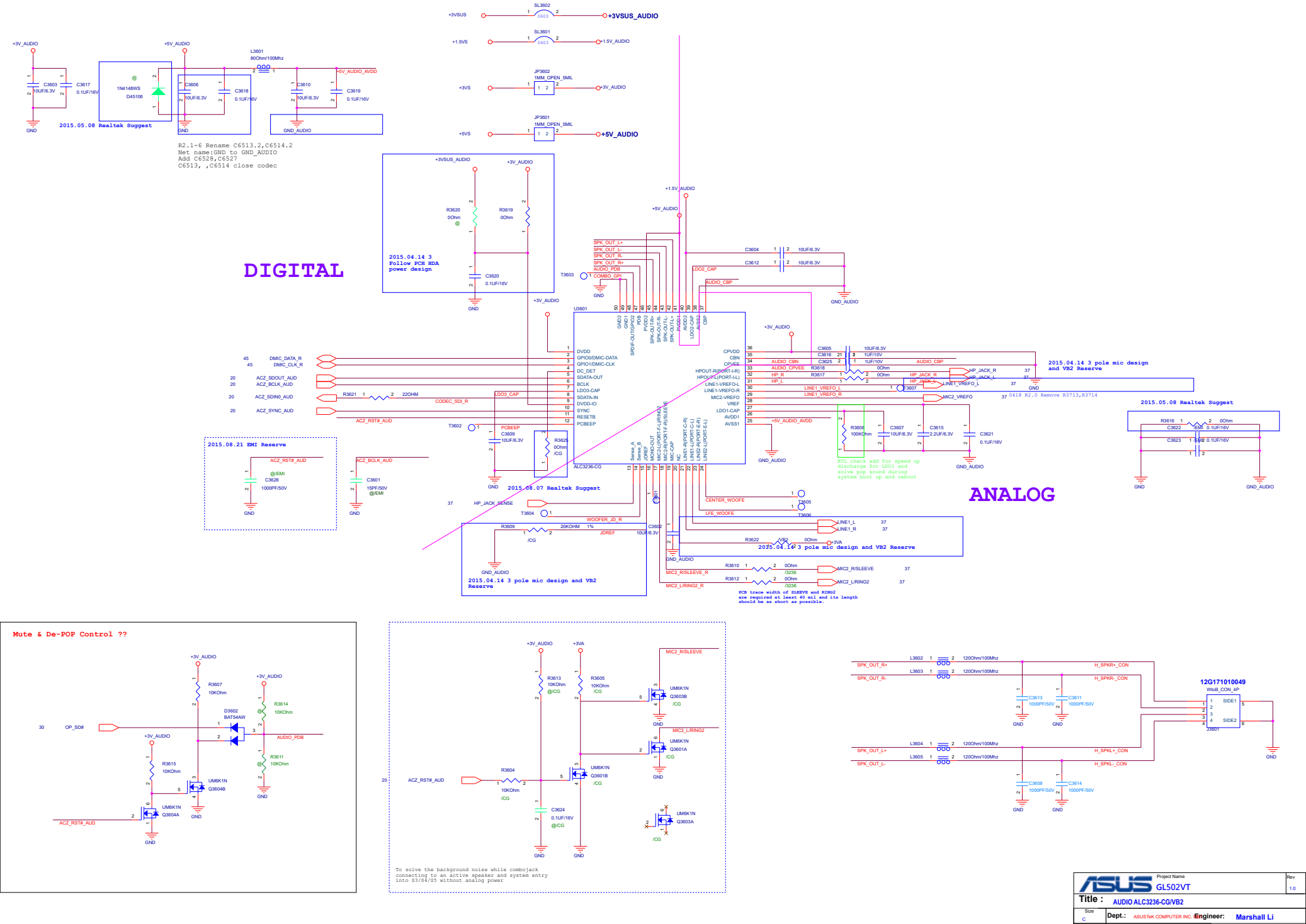
Title : LAN_*****

ASUSTeK COMPUTER INC. NB3

Engineer: EE

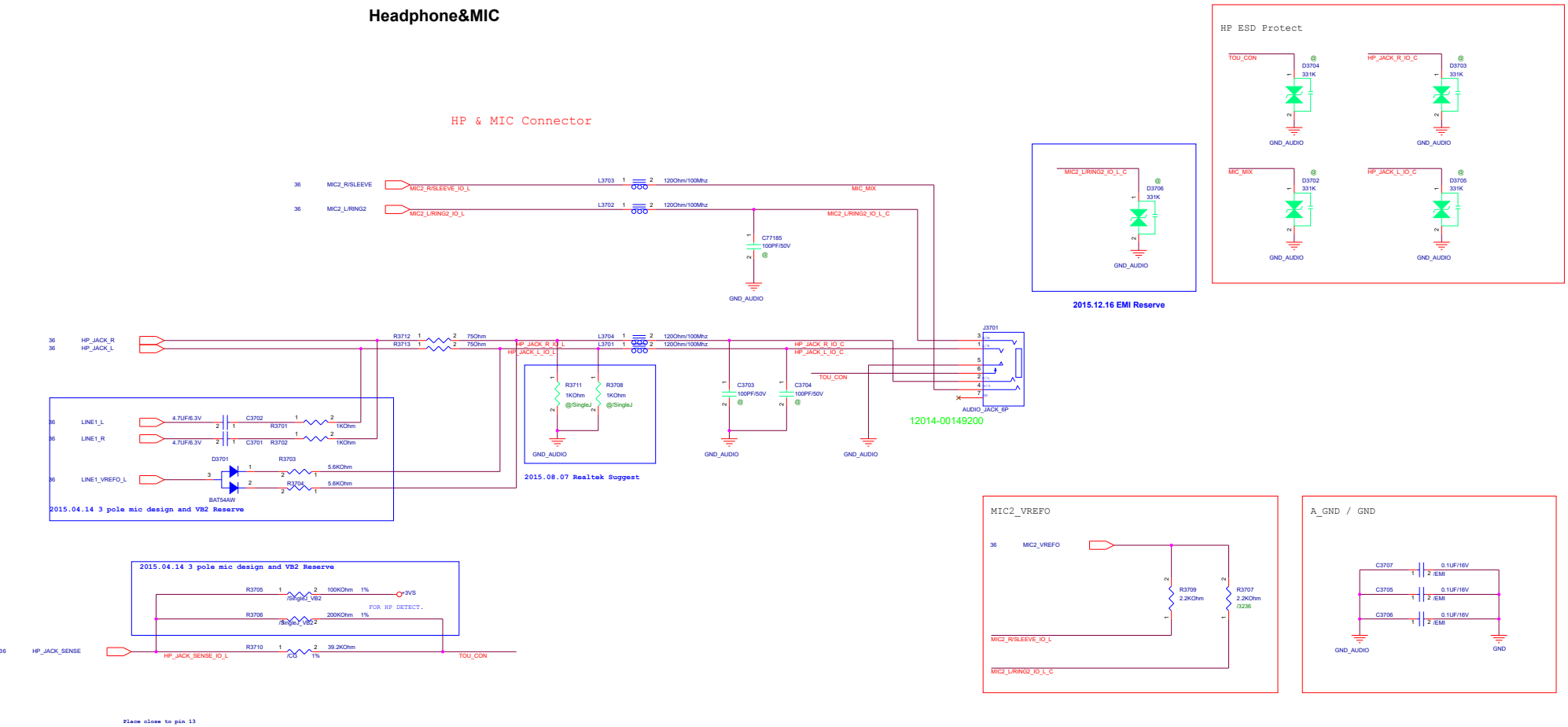
Size	Project Name	Rev
C	N501VW	1.0

Date:	Friday, December 18, 2015	Sheet	35	of	102



ASUS	Project Name: GL502VT		Rev: 1.0
Title : AUDIO ALC3236-CG/VB2			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Friday, December 18, 2015	Sheet 36 of 102		

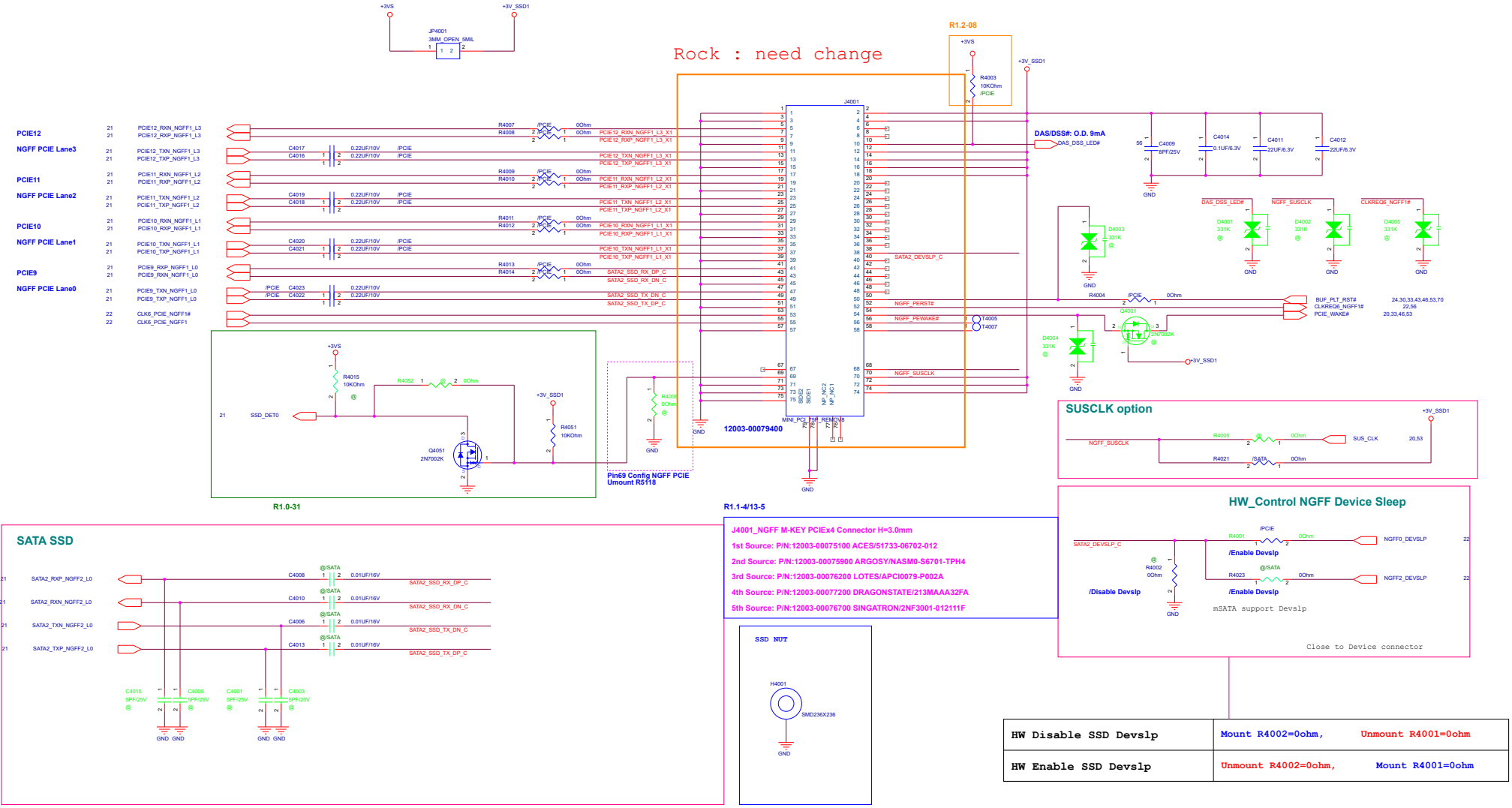
Headphone&MIC



Project Name: GL502VT		Rev: 1.0
Title: AUDIO ALC3236-CG/VB2 Jack		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li
Date: Friday, December 18, 2015	Sheet 37 of 102	

ASUSTeK COMPUTER INC. NB1	Title : Aud_HP Jack, MIC		
	Engineer: EE		
Size: Custom	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 38	of	102

NGFF_SSD



HW Disable SSD Devslp	Mount R4002=0ohm, Unmount R4001=0ohm
HW Enable SSD Devslp	Unmount R4002=0ohm, Mount R4001=0ohm

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : MiniCard_SSD

Engineer: EE

Size	Project Name	Rev
C	N501VW	1.0

Date: Friday, December 18, 2015 Sheet 40 of 102

Title : CB_*****

ASUSTeK COMPUTER INC. NB3

Engineer: EE

Size	Project Name	Rev
A	N501VW	1.0

Date:	Friday, December 18, 2015	Sheet	41	of	102

Title : Card Reader-RTS5226

ASUSTeK COMPUTER INC. NB1

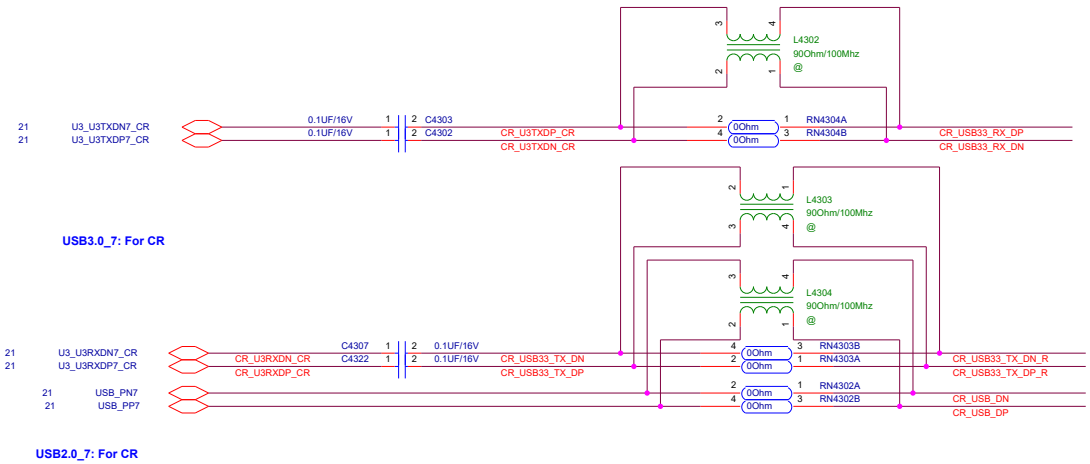
Engineer: EE

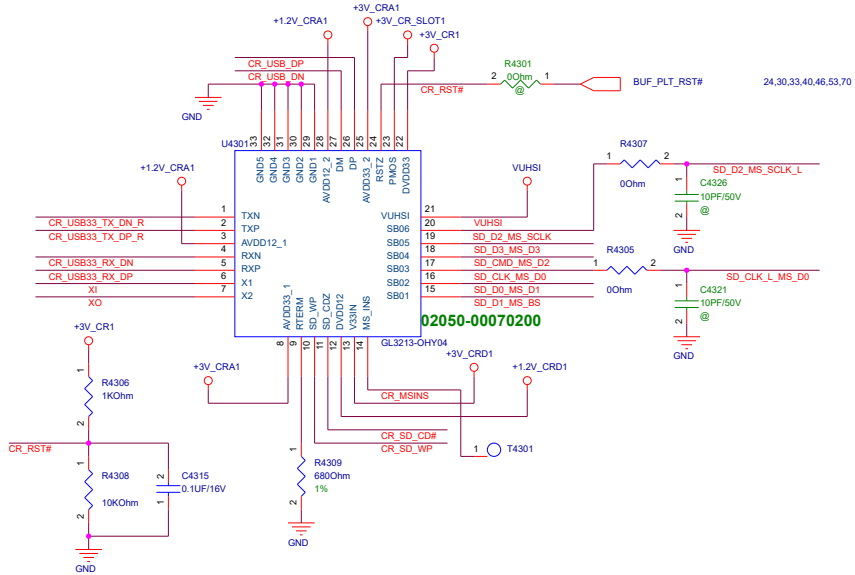
Size	Project Name	Rev
C	N501VW	1.0

Date:	Friday, December 18, 2015	Sheet	42	of	102

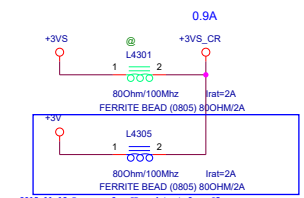
CR I/O Conn. (MB)

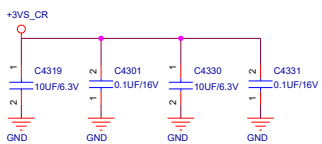
Main Board

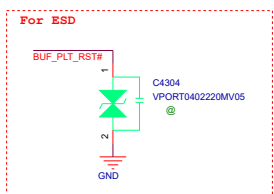


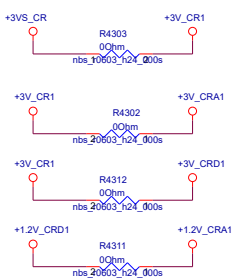


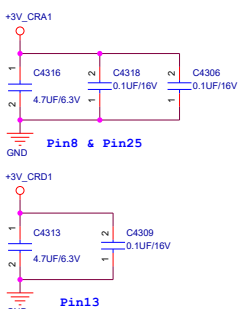
CardReader PWR

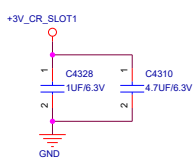




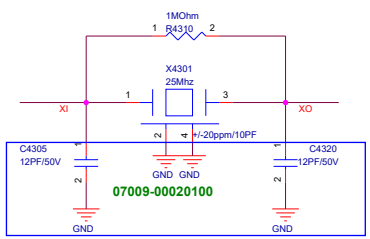








C4214, C4215 close to Pin23



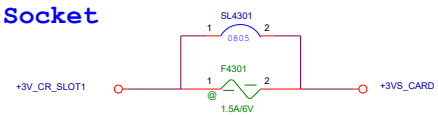
2015.12.15 change cap base on vendor report

X4201: 25MHZ +/-20ppm/10pF (3225)

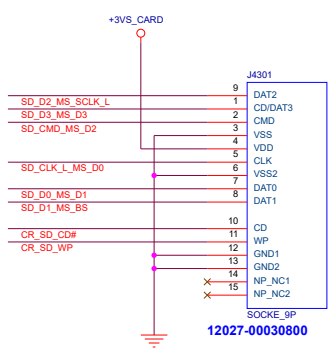
1st: P/N:07009-00020100 EPSON/FA-238G

2nd: P/N:07009-00020800 TXC/7V25000036

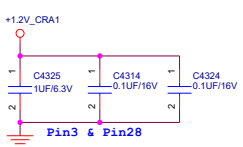
CR Socket

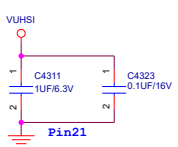


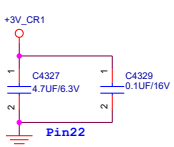
Reserved fuse for safety

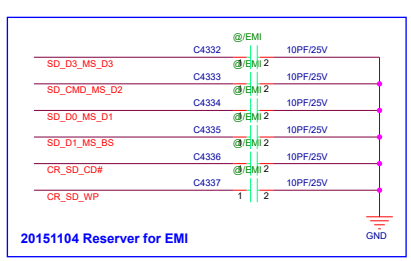


12027-00030800

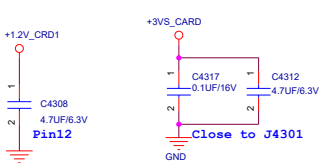








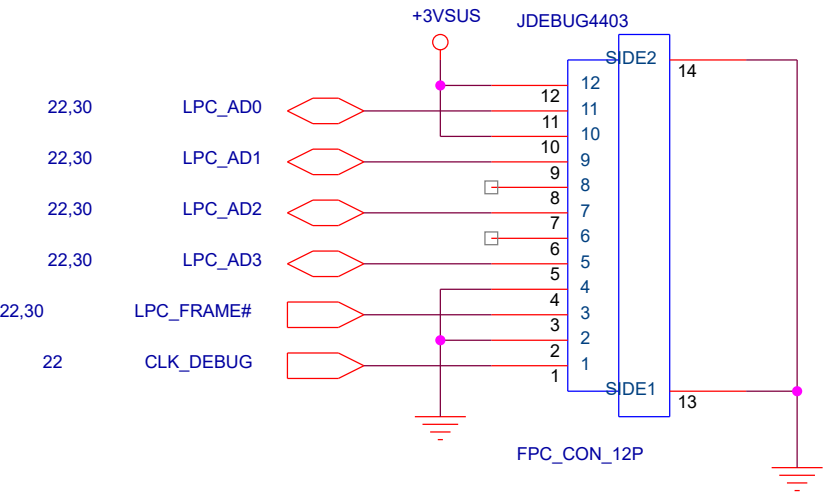
20151104 Reserver for EMI



ASUS	Project Name: GL502VT		Rev: 1.0
Title : CB IO CON			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Friday, December 18, 2015		Sheet 43 of 102	

LPC Debug Port

R1.0-24

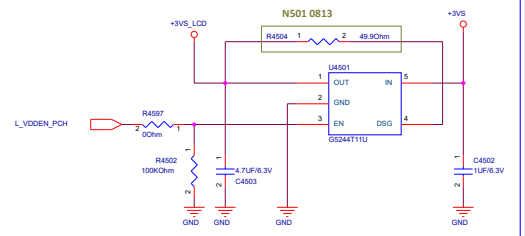


12018-00103200

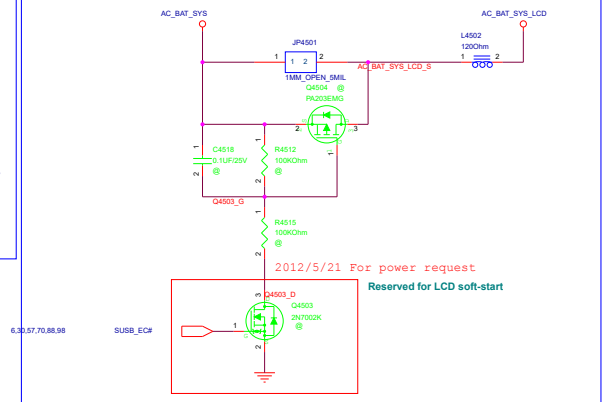
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DEBUG_LPC	
	Engineer: EE	
Size: A	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 44 of 102	

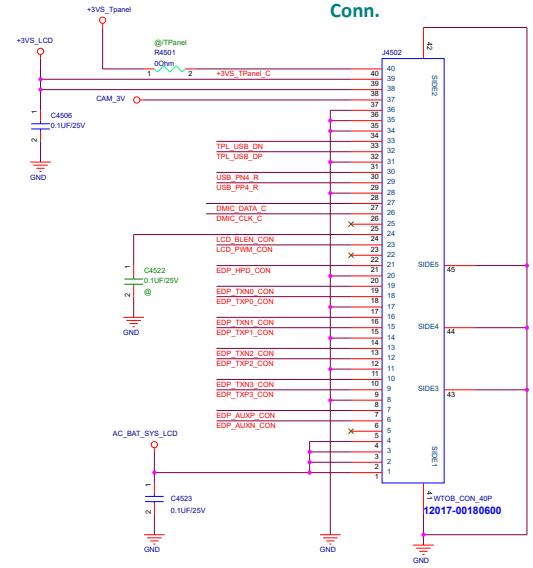
LCD Power switch



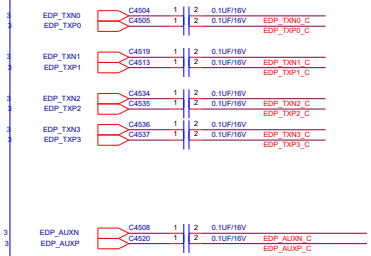
Panel BL Power



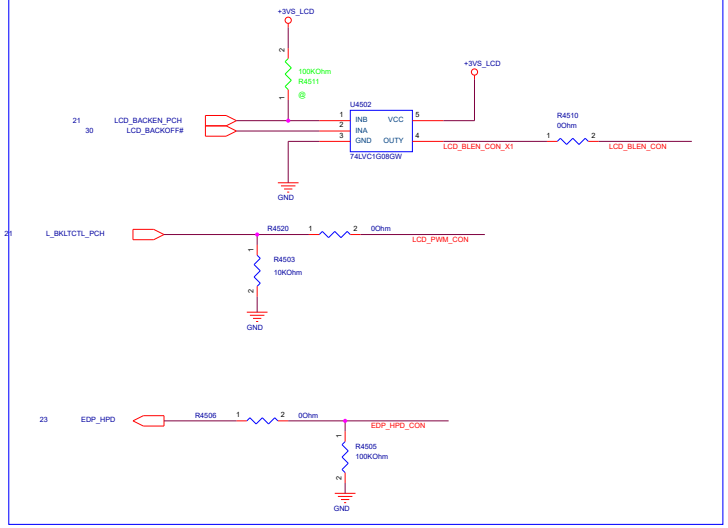
eDP Panel Conn.



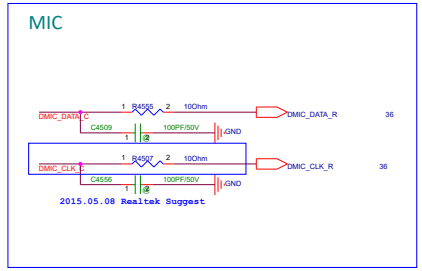
eDP from CPU



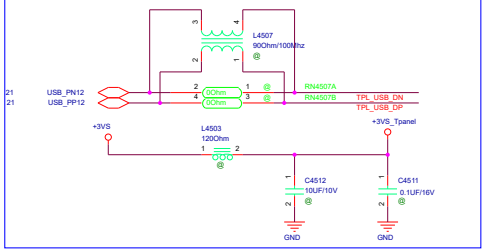
Panel



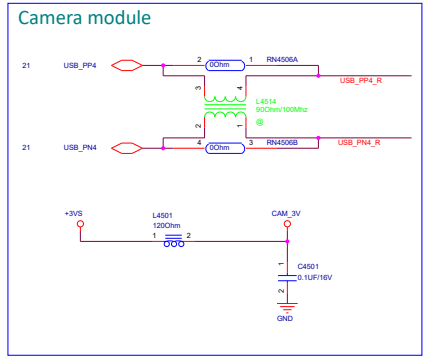
MIC



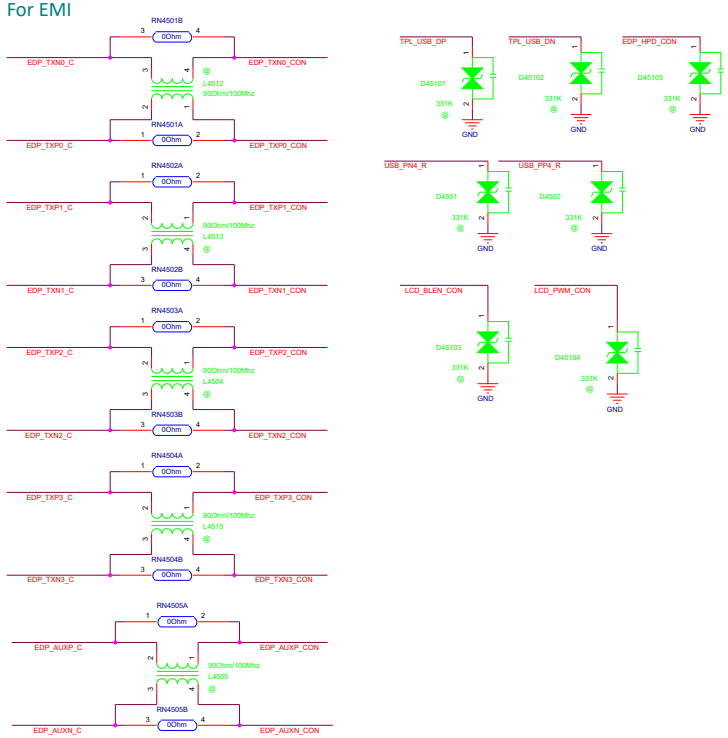
Touch Panel



Camera module



For EMI



<variant_name>

ASUSTeK COMPUTER INC. NB1	Title : CRT_eDP	
	Engineer: EE	
Size: C	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 45 of 102	

R1.1-17

+3V R7917 1 /USB31 2 0Ohm +3VSUS_ASM
nbs_r0603_h24_000s

+1.2V R7918 1 /USB31 2 0Ohm +1.2VSUS_ASM
nbs_r0603_h24_000s

+3VS JP4601 1 2 2 L4601 1 /USB31 2 220Ohm/100Mhz +3V_ASM +3V_ASM_A
1MM_OPEN_5MIL
/USB31

R0.1-40

+1.2V Q4611 PEA28BA /USB31 +1.2V_ASM L4602 1 /USB31 2 220Ohm/100Mhz +1.2V_ASM_A
C4651 0.1UF/25V /USB31
+12VS
P_LS_1.2VS_RC_10 C4652 0.01UF/25V /USB31 R4652 100KOhm /USB31 20,33,40,53 PCIE_WAKE#
+3V_ASM Q4602 2N7002K /USB31 PCIE_WAKE#_USB31

+3V_ASM R4628 4.7KOhm /USB31 +3V_ASM
U4602
U3_SPI_CS# 1 CE# VCC 8
U3_SPI_DI 2 SO(IO1) HOLD#(IO3) 7
3 WP#(IO2) SCK 6
4 GND SI(IO0) 5
U3_SPI_CLK
U3_SPI_DO
PM25LQ512B-SCE
/USB31
GND

20151102 Replace SPI Rom for Factory

reference delay circuit.

+3V_ASM R4608 100KOhm /USB31 +3V_ASM R4609 100KOhm /USB31 +3V_ASM R4614 100KOhm /USB31
Q4601A LM6K1N /USB31 U3_PORST# Q4601B LM6K1N /USB31
C4616 1UF/10V /USB31 C4620 1UF/10V /USB31
GND GND GND GND

-PORST : Vih=0.52xVCC33;Vil=0.3xVCC33 ;base on ASM1142 DC level

2015.12.04 SWAP the USB31 P and N

22 CLK5_PCIE_USB31 48 PECLKP
22 CLK5_PCIE_USB31# 49 PECLKN
/USB31

21 PCIE5_RXP_USB31 C4680 C4681 0.22UF/10V /USB31 PCIE5_RXP_USB31_X1 56 PTX0P
21 PCIE5_RXN_USB31 PCIE5_RXN_USB31_X1 57 PTX0N
/USB31

21 PCIE5_TXP_USB31 C4622 C4623 0.22UF/10V /USB31 PCIE5_TXP_USB31_X1 53 PRX0P
21 PCIE5_TXN_USB31 PCIE5_TXN_USB31_X1 54 PRX0N
/USB31

21 PCIE6_RXP_USB31 C4682 C4683 0.22UF/10V /USB31 PCIE6_RXP_USB31_X1 60 PTX1P
21 PCIE6_RXN_USB31 PCIE6_RXN_USB31_X1 61 PTX1N
/USB31

21 PCIE6_TXP_USB31 C4626 C4627 0.22UF/10V /USB31 PCIE6_TXP_USB31_X1 63 PRX1P
21 PCIE6_TXN_USB31 PCIE6_TXN_USB31_X1 64 PRX1N
/USB31

24,30,33,40,43,53,70 BUF_PLT_RST# R4670 0Ohm /USB31 PE_RST# 30 PE_RST#
PE_WAKE# 25 PE_WAKE#
22 CLKREQ5_USB31# PCIE_WAKE#_USB31 3 PE_CLKREQ#

R4605 1% /USB31 12.1KOHM REXT 59 REXT
GND

49 USB31_01_TXP 49 USB31_01_TXN U3TXP_A 42 U3TXN_A 43
49 USB31_01_U2N 49 USB31_01_U2P U2DM_A 22 U2DP_A 23

R0.1-21

+3V_ASM R4634 4.7KOhm R4633 4.7KOhm
T4605 T4606 USB31_01_PWRON USB31_02_PWRON PRON_A 26 PRON_B 27
49 USB31_01_OCI# 49 USB31_02_OCI# OCI_A# 28 OCI_B# 29

49 USB31_01_RXP 49 USB31_01_RXN U3RXP_A 45 U3RXN_A 46
49 USB31_02_TXP 49 USB31_02_TXN U3TXP_B 39 U3TXN_B 40
49 USB31_02_U2N 49 USB31_02_U2P U2DM_B 18 U2DP_B 19
49 USB31_02_RXP 49 USB31_02_RXN U3RXP_B 36 U3RXN_B 37

T4601 T4602 U3_UART_TX U3_UART_RX UART_TX 11 UART_RX 10

For USB3.1 Legacy support

+3V_ASM R4651 10KOhm /USB31
24 USB31_SMI# /USB31 Q4621 2N7002K SMI# 2 SMI#
U3_SPI_DI 8 SPI_DI
U3_SPI_CS# 5 SPI_CS#
U3_SPI_CLK 7 SPI_CLK
U3_SPI_DO 6 SPI_DO
U3_PORST# 9 PORST#

R1.0-23

X4601 20MHZ /USB31 C4632 10PF/50V /USB31 U3_XI 51 XI
U3_XO 50 XO
U3_TEST_EN 31 TEST_EN
R4612 4.7KOhm /USB31
GND

U4601

VCC_IN 13 VCC_IN R4631 /USB31@ 0Ohm +3V_ASM
PGND 15 PGND R4602 /USB31@ 0Ohm GND +3V_ASM
VCC1 4 VCC2 32 C4601 0.1UF/16V /USB31 C4602 0.1UF/16V /USB31 GND
VCCP1 55 VCCP2 62 VCCU1 38 VCCU2 44 C4603 2.2uF/10V /USB31 C4604 2.2uF/10V /USB31 C4605 2.2uF/10V /USB31 C4606 2.2uF/10V /USB31 +3V_ASM_A GND
EXTL 14 U3_EXTL_O T4609 for 1.05V_ASM
VDD1 1 VDD2 12 VDD3 33 C4607 0.1UF/16V /USB31 C4608 0.1UF/16V /USB31 C4609 0.1UF/16V /USB31 +1.2V_ASM GND
VDDU1 35 VDDU3 47 VDDP1 52 C4610 2.2uF/10V /USB31 C4611 2.2uF/10V /USB31 C4612 2.2uF/10V /USB31 +1.2V_ASM_A GND
VDDP2 58 VDDU2 41 R4606 /USB31 0Ohm R4607 /USB31 0Ohm +1.2V_ASM_A C4621 4.7UF/16V /USB31 C4613 4.7UF/16V /USB31 GND
VCCSUS1 20 VCCSUS2 24 C4614 C4615 0.1UF/16V /USB31 +3VSUS_ASM
VCCSUS_IN 16 U3_VCCSUS_IN R4611 /USB31@ 0Ohm GND
1.05VSUS LDO IN
ASM1142 R05 P.29 3.3VSUS max 5mA
VDDSUS1 21 VDDSUS2 34 C4618 C4619 0.1UF/16V /USB31 +1.2VSUS_ASM
VCCSUS_O 17 U3_VCCSUS_O R4613 /USB31@ 0Ohm GND
1.05VSUS LDO OUT
ASM1142 R05 P.29 1.2VSUS max 5mA

GND1 65 GND2 66 GND
ASM1142
06050-00090100
/USB31

H/W Strapping

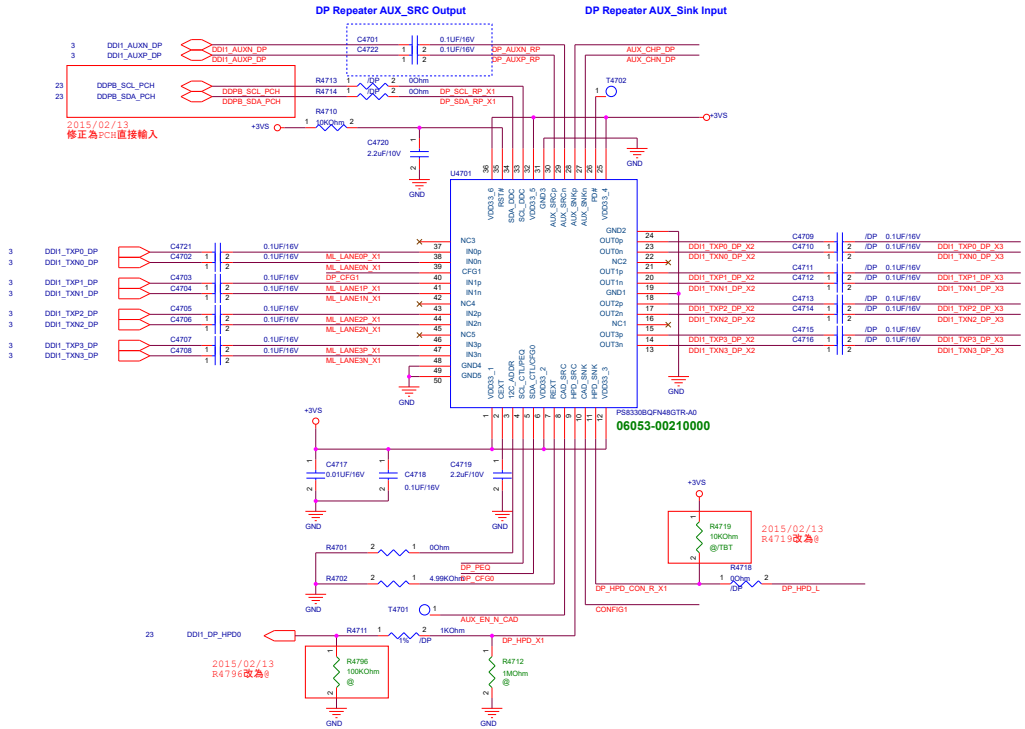
+3V_ASM
U3_SPI_DO R4615 /USB31 4.7KOhm R4616 /USB31@ 4.7KOhm
U3_UART_RX R4617 /USB31 4.7KOhm R4618 /USB31@ 4.7KOhm
U3_UART_TX R4619 /USB31 4.7KOhm R4620 /USB31@ 4.7KOhm
U3_SPI_CLK R4621 /USB31 4.7KOhm R4622 /USB31@ 4.7KOhm
GND

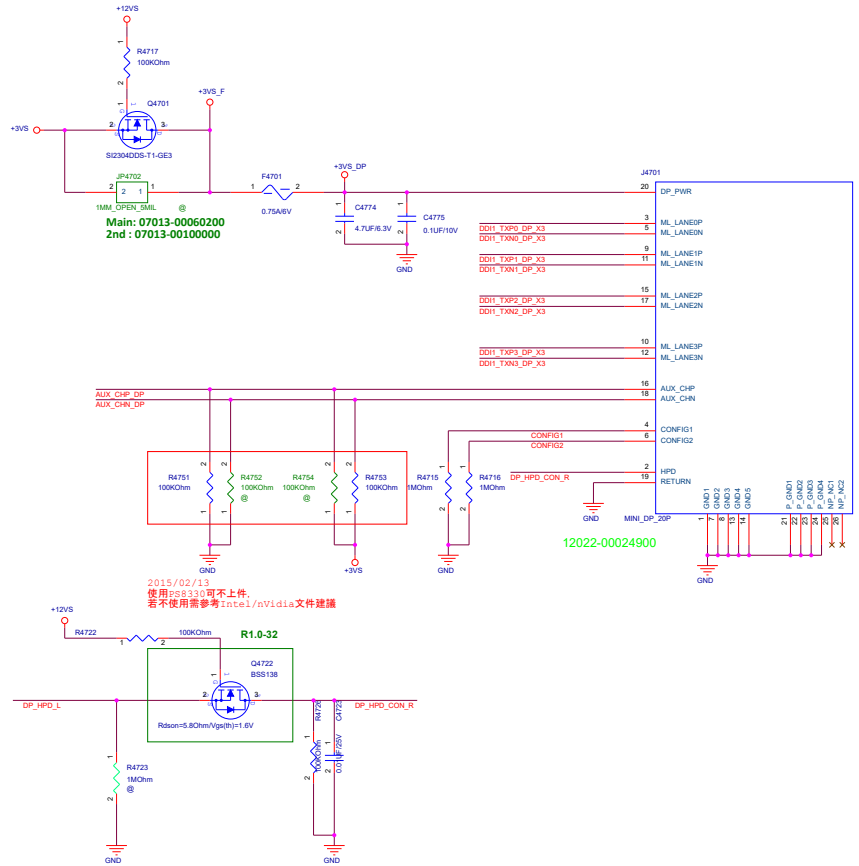
UART[RX:TX] Clock Select
11: Asynchronous mode with External 20MHz Crystal (Default)

SPI_CLK D3cold enable
1: D3cold(Default) 0: D3Hot

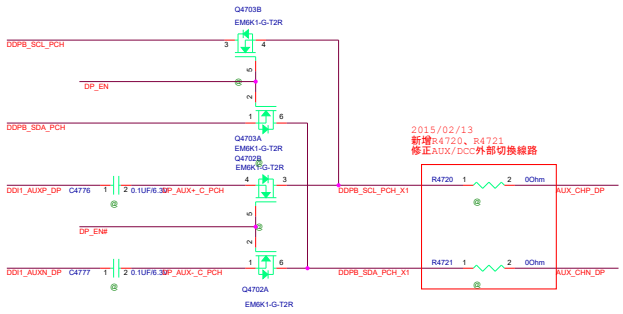
ASUS	Project Name: GL752VW		Rev: 1.0
Title : USB 3.1 ASM1142			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo	
Date: Friday, December 18, 2015	Sheet 46 of 102		

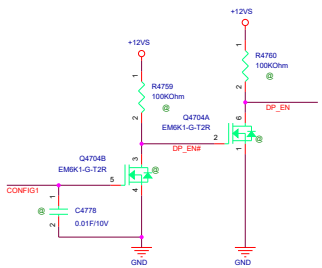
DP Repeater_PS8330B

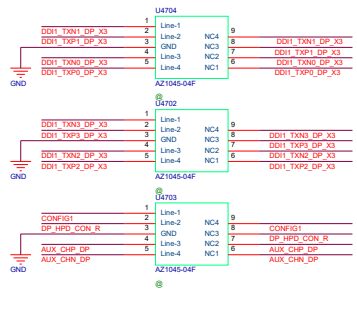


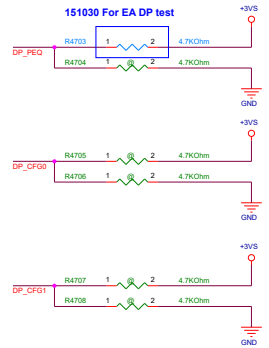


Follow SKL-H PDG 5.4.4 P150
Figure 5-13. DisplayPort*
Auxiliary Channel Dual Mode Support Protection Circuit



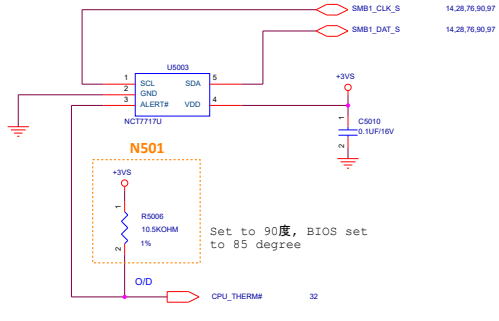






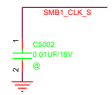
ASUS	Project Name: GL502VT		Rev: 1.0
Title :	Display Port Conn.		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Friday, December 18, 2015	Sheet 47 of 102		

CPU Thermal Sensor

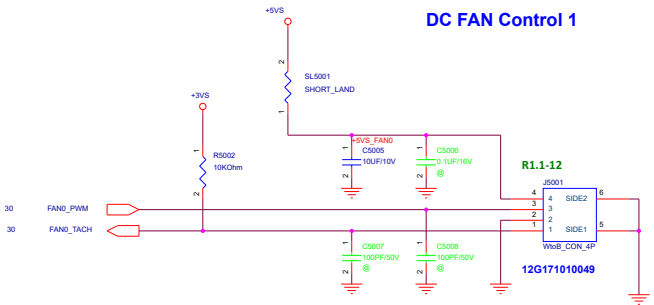


Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

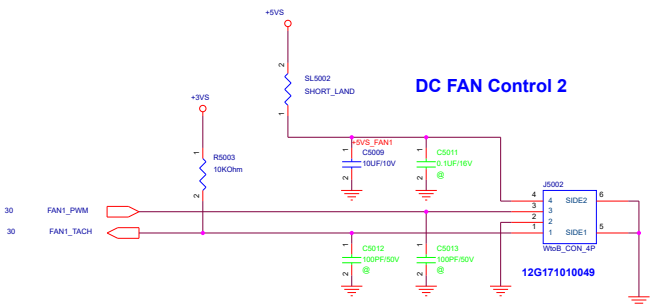
Reserve for
powr noise



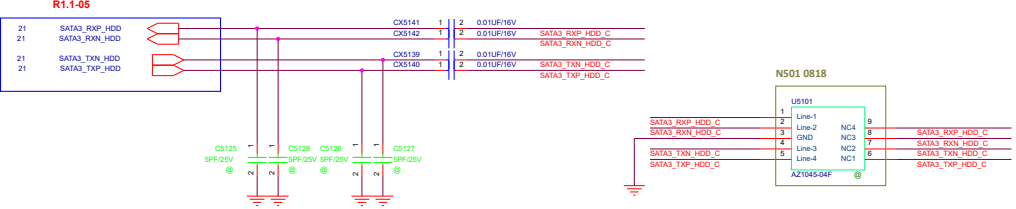
DC FAN Control 1

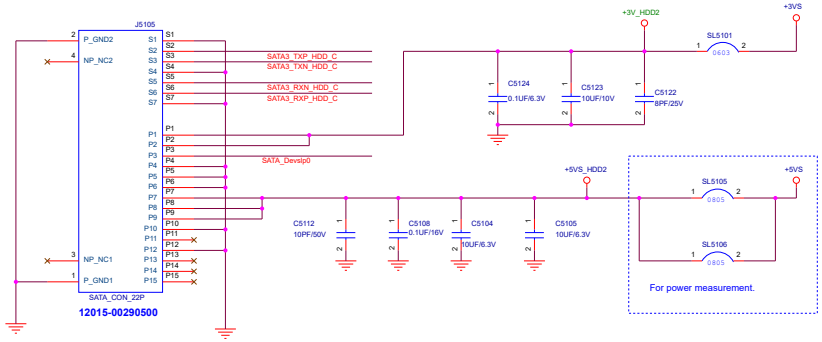


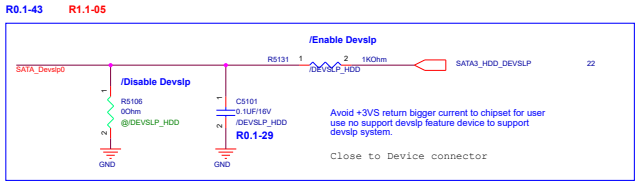
DC FAN Control 2



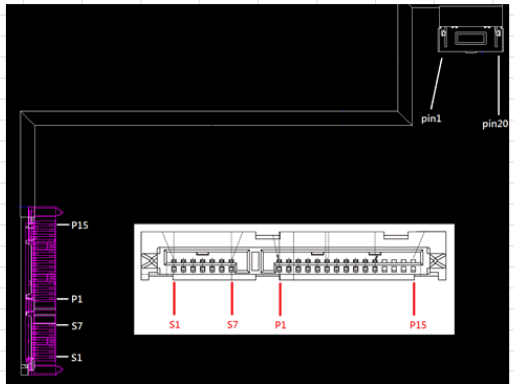
ASUSTeK COMPUTER INC. NB1	Title : FAN_Thermal Sensor & Fan		
	Engineer: EE		
Size: C	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 50 of 102		







SATA Connector		
Pin	net	Note
P15	NC	
P14	NC	
P13	NC	
P12	Ground	
P11	NC	
P10	Ground	
P9	+5V	power
P8	+5V	
P7	+5V	
P6	Ground	
P5	Ground	
P4	Ground	
P3	Devslp	Impedance 50Ω
P2	+3V	power
P1	+3V	
S7	Ground	
S6	SATA_RX_P	Differential Pairs, Impedance 85Ω
S5	SATA_RX_N	Differential Pairs, Impedance 85Ω
S4	Ground	
S3	SATA_TX_N	Differential Pairs, Impedance 85Ω
S2	SATA_TX_P	Differential Pairs, Impedance 85Ω
S1	Ground	



20 pin HDD Board connector		
Pin	net	Note
pin1	Ground	
pin2	NC	
pin3	+5V	power
pin4	+5V	
pin5	+5V	
pin6	+5V	
pin7	NC	
pin8	Ground	
pin9	Devslp	Impedance 50Ω
pin10	NC	
pin11	+3V	power
pin12	+3V	
pin13	NC	
pin14	Ground	
pin15	SATA_RX_P	Differential Pairs, Impedance 85Ω
pin16	SATA_RX_N	Differential Pairs, Impedance 85Ω
pin17	Ground	
pin18	SATA_TX_N	Differential Pairs, Impedance 85Ω
pin19	SATA_TX_P	Differential Pairs, Impedance 85Ω
pin20	Ground	

ASUSTeK COMPUTER INC. NB1

Title : XDD_HDD & ODD CON

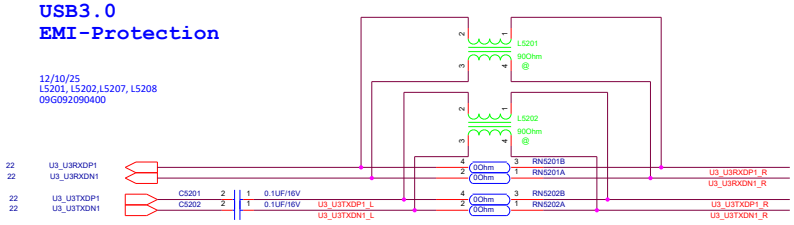
Engineer: EE

Size: C | Project Name: N501VW | Rev: 1.0

Date: Friday, December 18, 2015 | Sheet 51 of 102

USB3.0 EMI-Protection

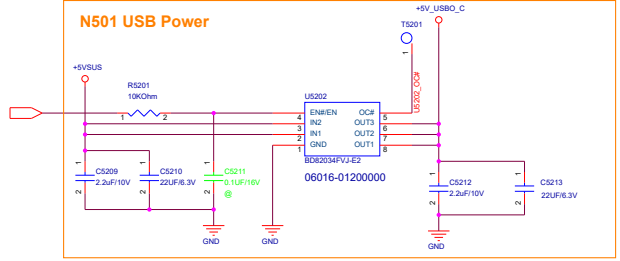
12/10/25
L5201, L5202,L5207, L5208
09G092090400



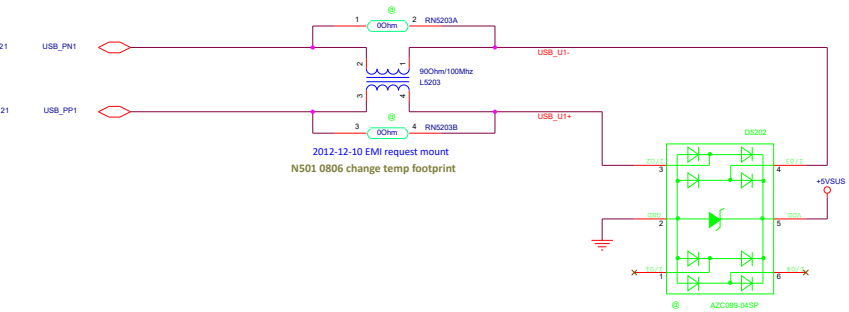
From PCH

30,57,63,88 SUSC_EC#

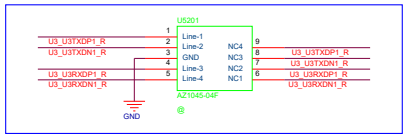
N501 USB Power



USB2.0 EMI-Protection



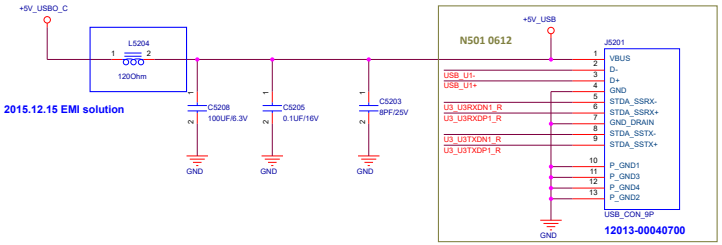
2012-12-10 EMI request mount
N501 0806 change temp footprint



2015.12.16 EMI solution

USB3.0_Port 0

N501 0808 change temp footprint

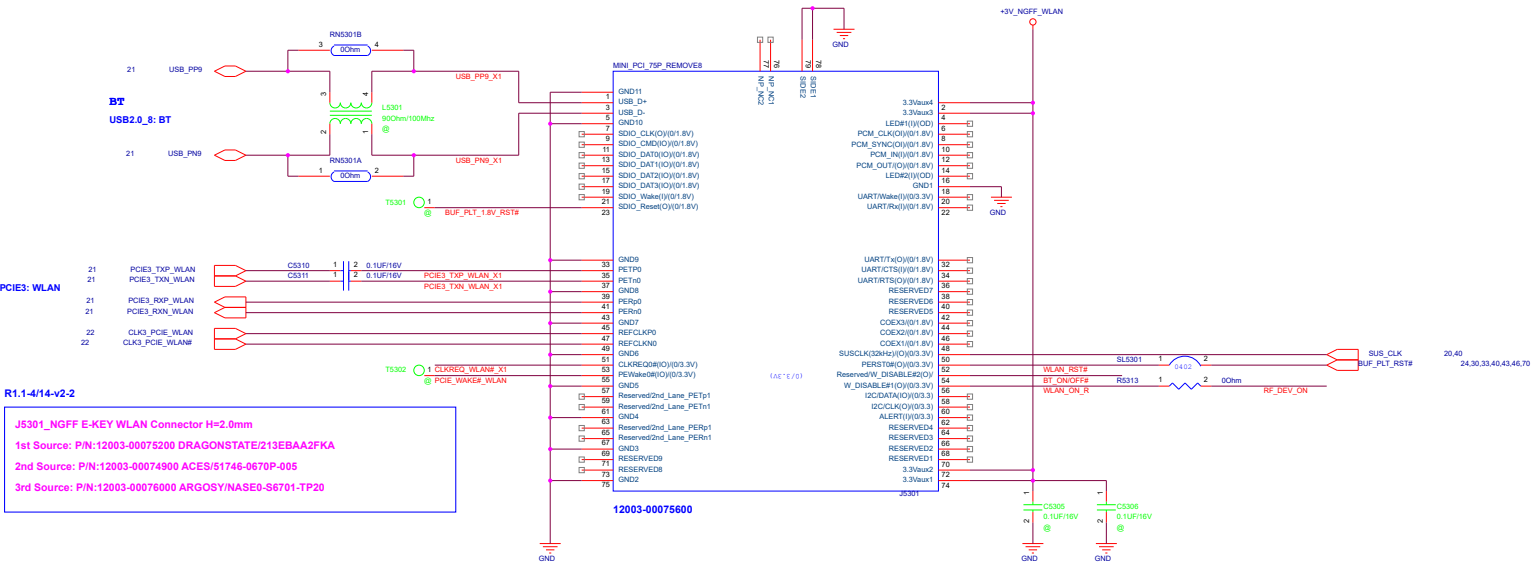


2015.12.15 EMI solution

ASUSTeK COMPUTER INC. NB1	Title : USB Charger		
	Engineer: EE		
Size: Custom	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 52 of 102		

R1.1-02

NGFF M.2 TYPE_E-KEY WIFI

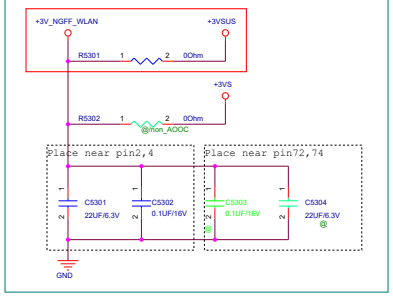


R1.1-4/14-v2-2

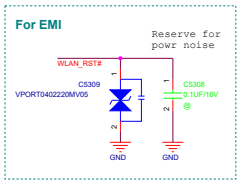
J5301_NGFF E-KEY WLAN Connector H=2.0mm
1st Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FKA
2nd Source: P/N:12003-00074900 ACES/51746-0670P-005
3rd Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

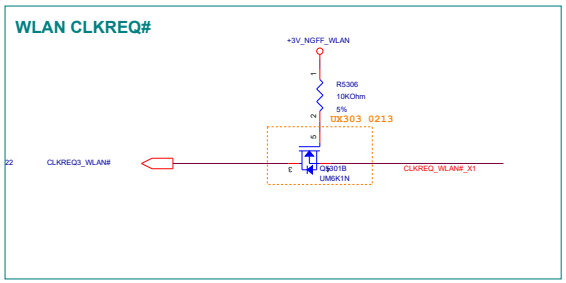
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS



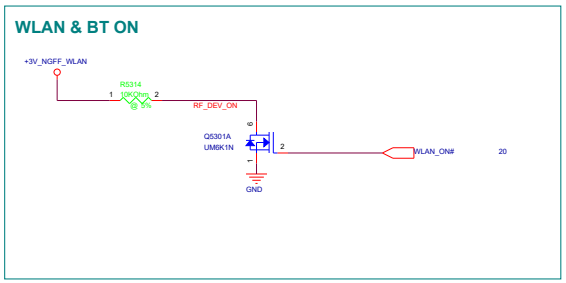
For EMI



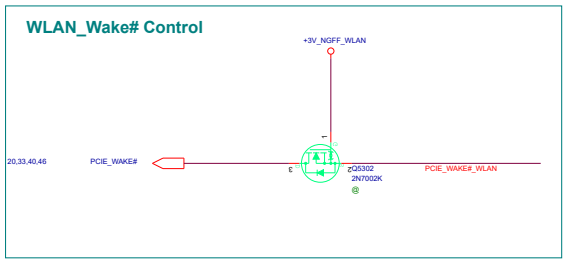
WLAN CLKREQ#

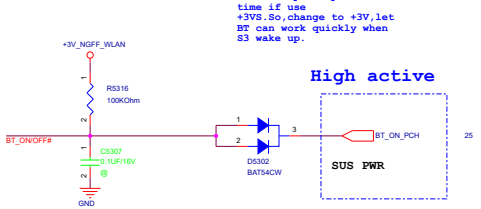


WLAN & BT ON

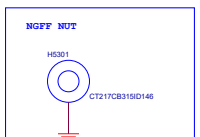


WLAN_Wake# Control





NGFF NUT



74	3.3Vaux	GND	75
72	3.3Vaux	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GND	69
66	RESERVED	Reserved/2nd Lane PERn1	67
64	GPIO0 NFC Reset# (MGPIO7)(O)(0/3.3V)	Reserved/2nd Lane PERp1	65
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	GND	63
60	NFC I2C SM CLK (O)(0/3.3)	Reserved/2nd Lane PETn1	61
58	NFC I2C SM DATA (IO)(0/3.3)	Reserved/2nd Lane PETp1	59
56	W_DISABLE#1 (O)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (?)(0/1.8V)	REFCLKN0	49
46	COEX2(?)(0/1.8V)	REFCLKP0	47
44	COEX3(?)(0/1.8V)	GND	45
42	CLink CLK	PERn0	43
40	CLink DATA	PERp0	41
38	CLink RESET (O)(0/3.3V)	GND	39
36	UART CTS (O)(0/1.8V)	PETn0	37
34	UART RTS (I)(0/1.8V)	PETp0	35
32	UART Tx (O)(0/1.8V)	GND	33
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I)(0/1.8V)	SDIO Reset(O)(0/1.8V)	23
20	UART Wake (I)(0/3.3V)	SDIO Wake(I)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (OI)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (OI)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3Vaux	USB_D-	5
2	3.3Vaux	USB_D+	3
		GND	1

<Variant Name>

ASUSTeK COMPUTER		Title :	WiFi/WiMax
		Engineer:	EE
Size	Project Name		Rev
C	N501VW		1.0
Date: Friday, December 18, 2015		Sheet 53 of 102	

Title : USB3_*****

ASUSTeK COMPUTER INC

Engineer: EE

Size	Project Name	Rev
C	N501VW	1.0

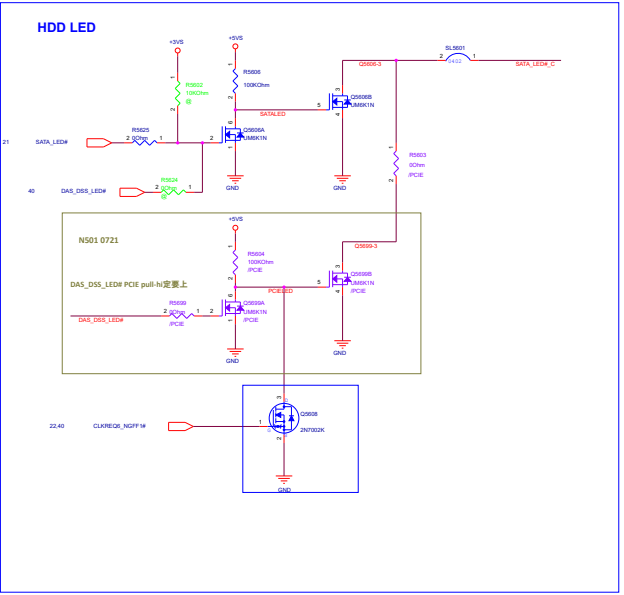
Date: Friday, December 18, 2015 Sheet 54 of 102

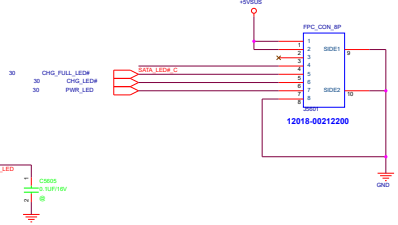
IO Board

ASUSTeK COMPUTER INC. NB1	Title : IO Con. to MB	Engineer: EE	
Size: Custom	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 55 of 102		

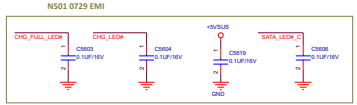
2014/05/29 Add HDD & SSD LED control circuit.

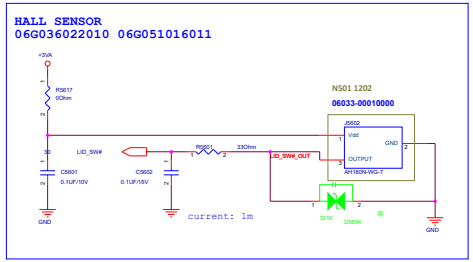
HDD LED



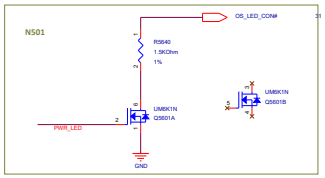


SATA_LED#_C

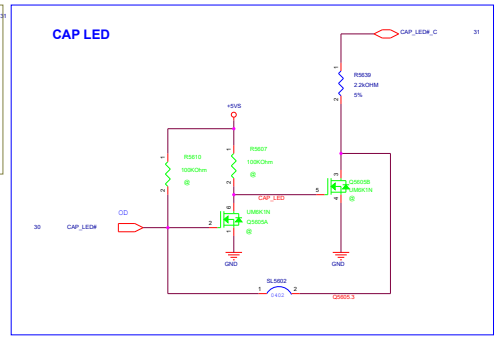




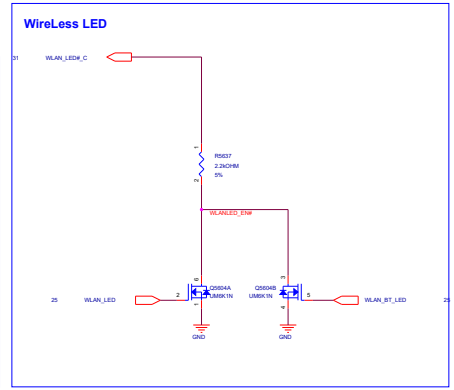
OS LED



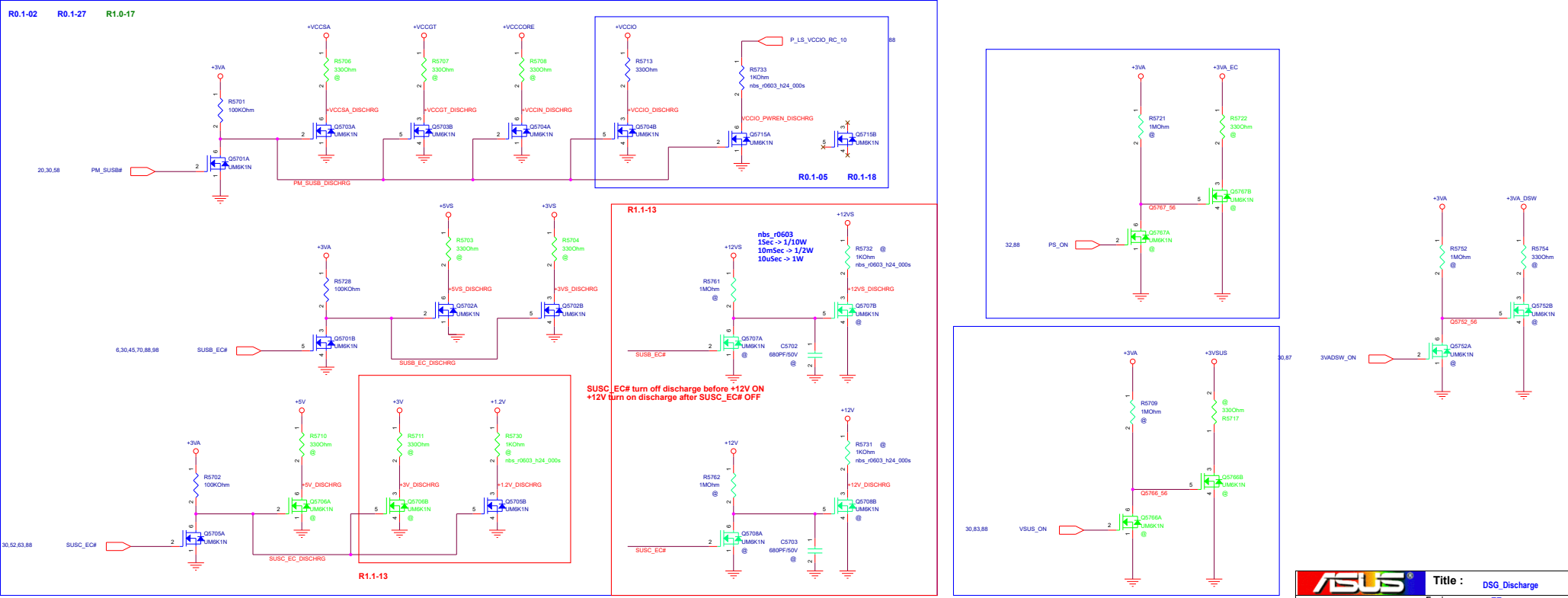
CAP LED



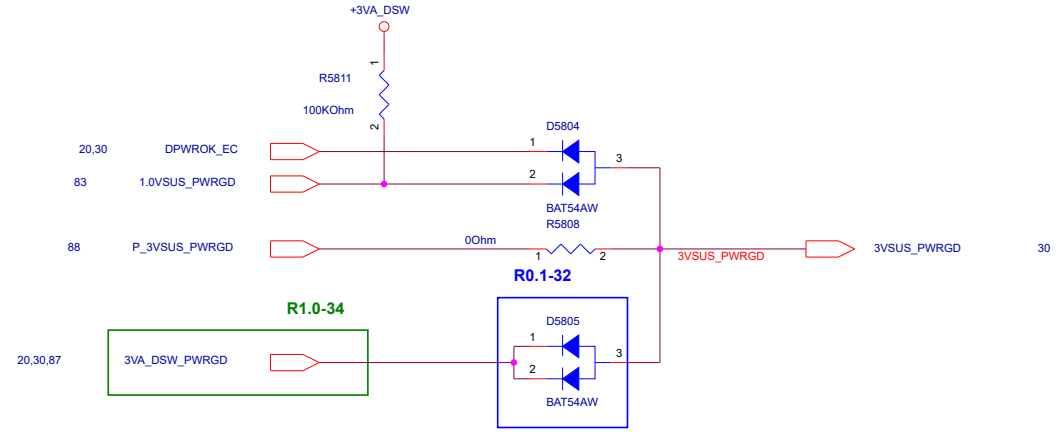
WireLess LED

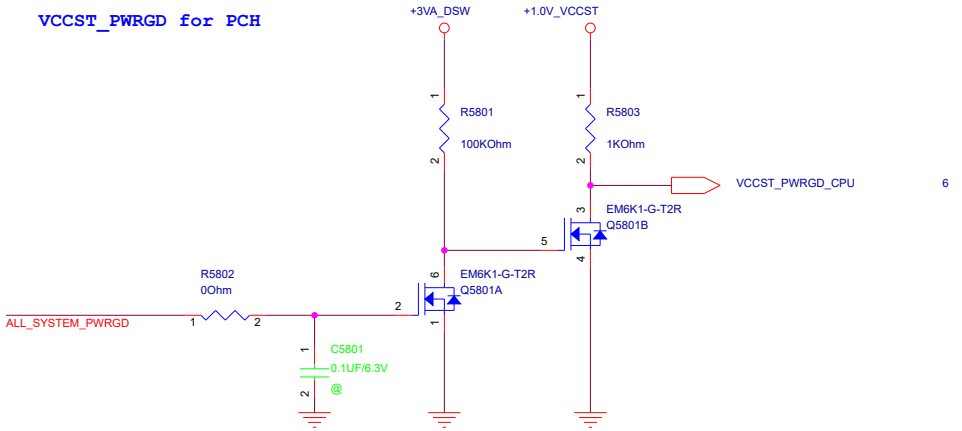


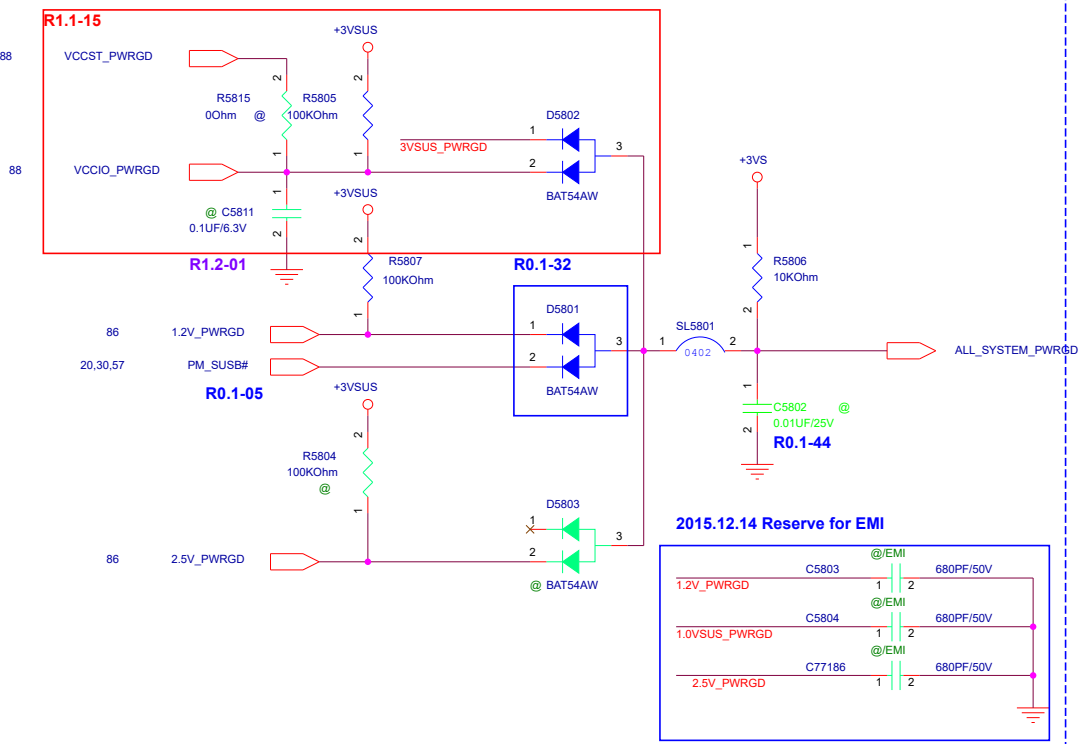
ASUSTeK COMPUTER INC. NB3	Title :	LED & LID
	Engineer:	EE
Size: C	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 56 of 102	



ASUSTeK COMPUTER	Title : DSG_Discharge		
	Engineer: EE		
Size: Custom	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 57 of 102		







<Variant Name>

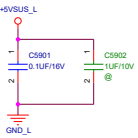
ASUSTeK COMPUTER

Title : Power Protect

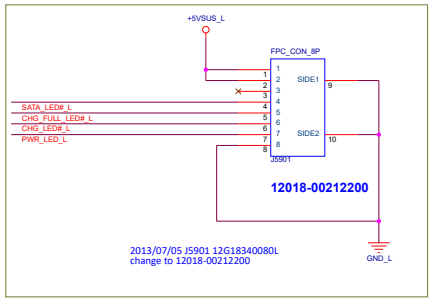
Engineer: EE

Size	Project Name	Rev
Custom	N501VW	1.0

Date: Friday, December 18, 2015 Sheet 58 of 102

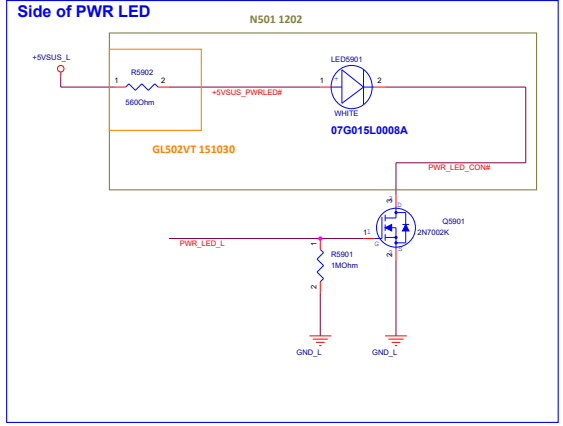


N501 0603

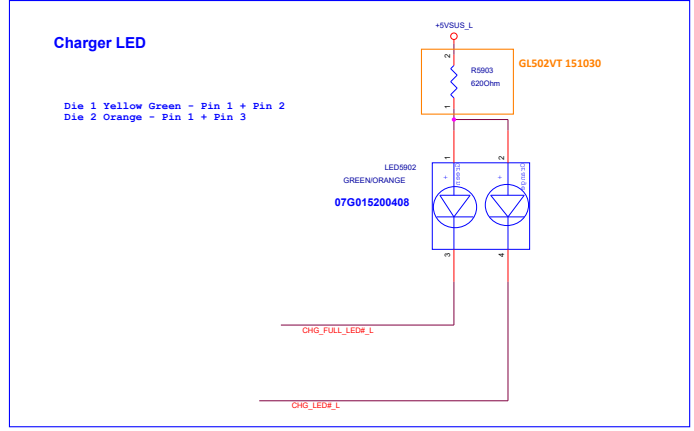


Side of PWR LED

N501 1202

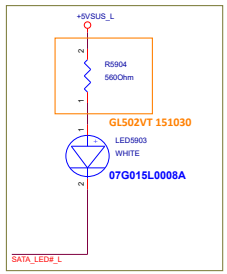


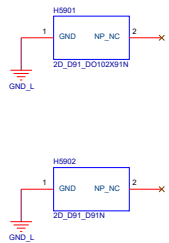
Charger LED

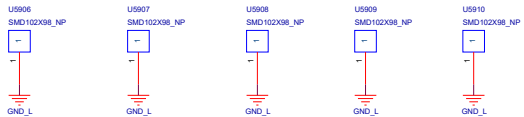


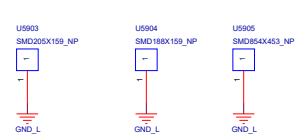
HDD LED

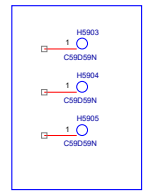
N501 0721



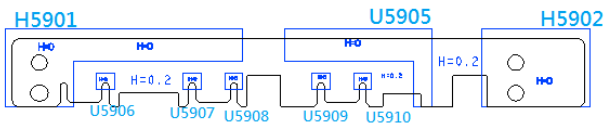


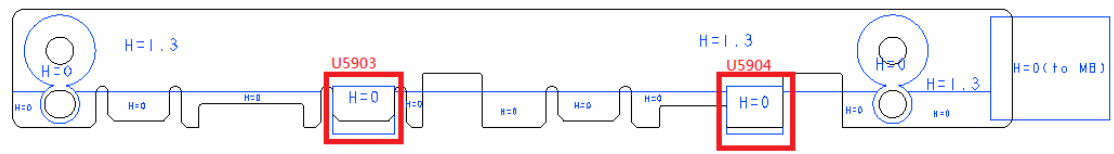






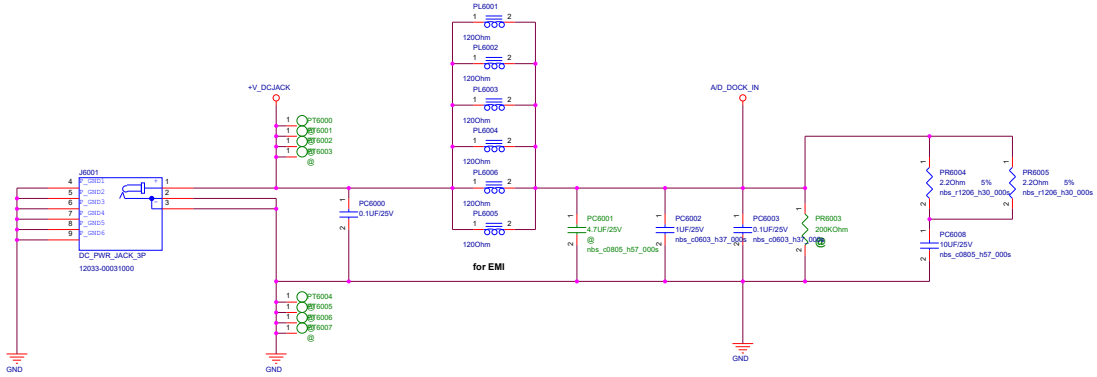
2015.11.05 add by ME



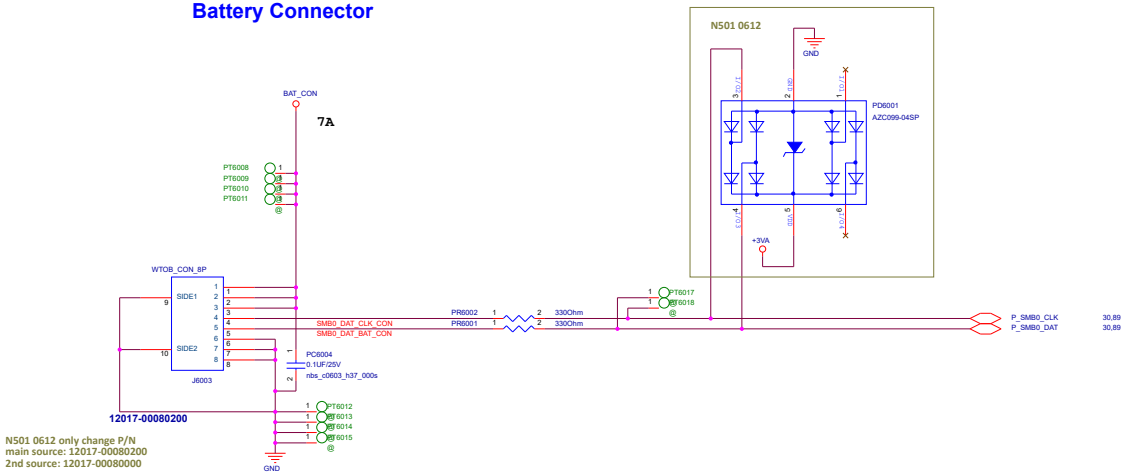


ASUSTeK COMPUTER INC. NB3	Title : I/O_Main board Conn.		
	Engineer: EE		
Size: C	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 59 of 102		

DC-IN Connector



Battery Connector



N501 0612 only change P/N
main source: 12017-00080200
2nd source: 12017-00080000

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN		
	Engineer:		
Size: C	Project Name: N501VW		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 60 of 102		

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : BT_Bluetooth	
	Engineer: EE	
Size: A	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 61 of 102	

Title : I/O board(1-1)_CR_RTS5139

ASUSTeK COMPUTER INC. NB3

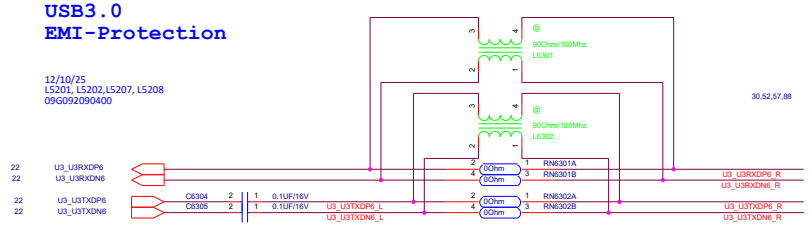
Engineer: EE

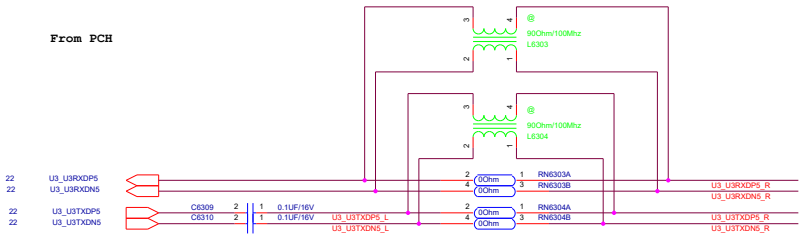
Size	Project Name	Rev
C	N501VW	1.0

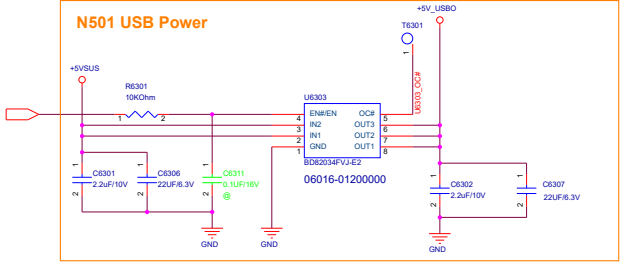
Date: Friday, December 18, 2015 Sheet 62 of 102

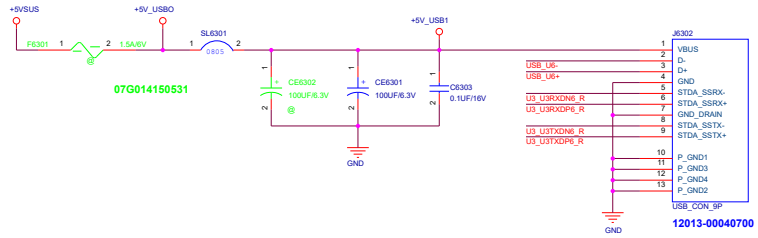
USB3.0 EMI-Protection

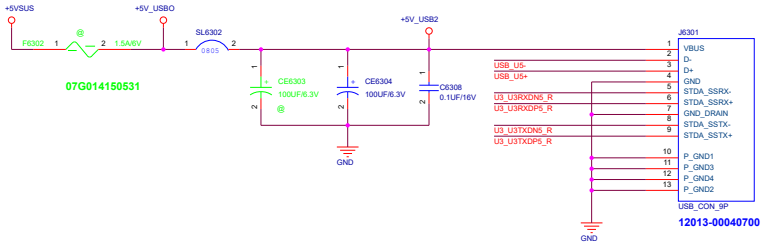
12/10/25
L5201, L5202,L5207, L5208
09G092090400





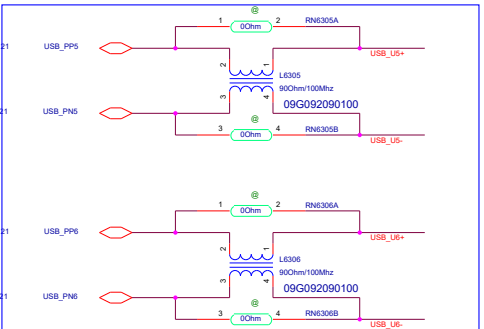






USB2.0 EMI-Protection

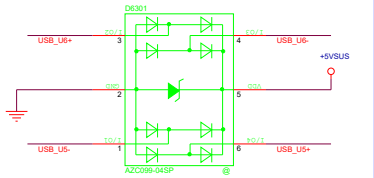
R1.1-4/13-5



L5204 & L5206 C.M. CHOKE(0805)90 OHM/330mA
1st Source: P/N:09G09209011D INPAQ/MCM2012D900FBE
2nd Source: P/N:09G092090300 TAI-TECH/WCM2012F2SF-900T04
3rd Source: P/N:09G092090110 MURATA/DLW21SN900SQ2L
4th Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S
5th Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L

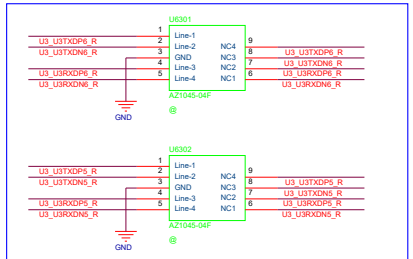
R1.1-4/13-5

D5201 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



USB3.0/USB 2.0 ESD-Protection

R1.1-4/13-5



U5201 & U5203 ESD PROTECTION
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : USB Port	
	Engineer: EE	
Size: C	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 63 of 102	

Main Board

<Variant Name>

Title :

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
A	N501VW	1.0

Date: Friday, December 18, 2015 Sheet 66 of 102

shielding case screw hole

H6701 NOPAD
H6702 NOPAD
H6703 O59X20DO59X20N
H6704 O59X20DO59X20N

PCH NUT

H6731 2D_D94
H6732 GND NP_NC 2D_D110_DO94X106N
H6735 GND NP_NC 2D_D94_D94N
H6736 2D_D110_DO94X106
H6744 CT354CB315D94
H6742 CT256CB315I114D94
H6741 CT256CB315I114D94
H6743 CT256CB315I114D94
H6745 P_GND NP_NC1 NP_NC2 NP_NC3 NP_NC4 NP_NC5 NP_NC6 NP_NC7 NP_NC8 NP_NC9 NP_NC10 NP_NC11 NP_NC12 D94_12D31N
H6733 P_GND1 P_GND2 NP_NC1 NP_NC2 NP_NC3 NP_NC4 NP_NC5 NP_NC6 NP_NC7 NP_NC8 NP_NC9 NP_NC10 NP_NC11 NP_NC12 NP_NC13 15D_D94_D106X94_D31N
H6734 P_GND1 P_GND2 NP_NC1 NP_NC2 NP_NC3 NP_NC4 NP_NC5 NP_NC6 NP_NC7 NP_NC8 NP_NC9 NP_NC10 NP_NC11 NP_NC12 NP_NC13 15D_D110_106X94_D31N

FAN NUT

H6705 CT217CB176D146
H6706 CT217CB176D146
H6707 CT217CB176D146
H6708 CT217CB176D146
H6709 CT217CB176D146
H6710 CT217CB176D146

GPU bracket tooling hole

CPU skrew hole

CPU NUT

H6748 CT217CB176D146
H6749 CT217CB176D146
H6750 CT217CB176D146
H6751 CT217CB176D146

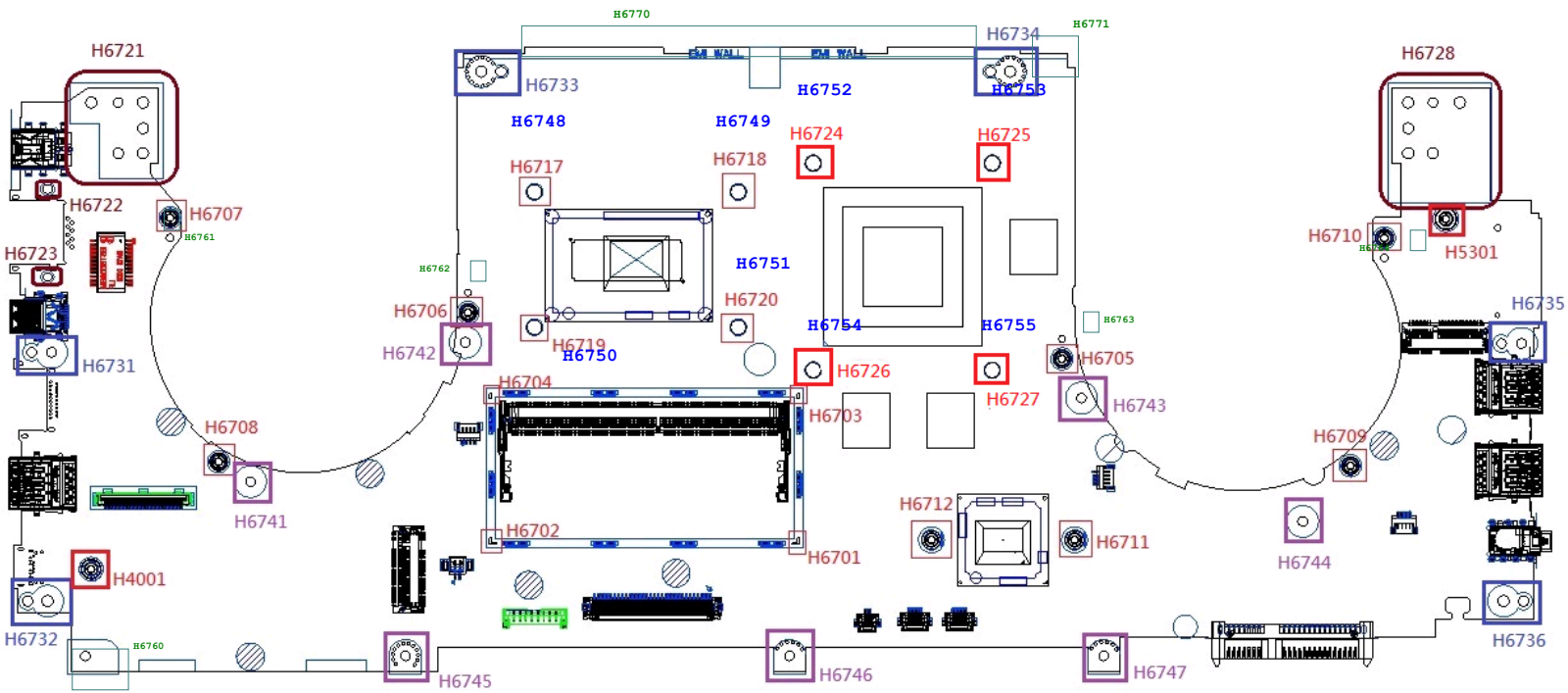
GPU NUT

H6752 U5F-M-EXPREE
H6753 U5F-M-EXPREE
H6754 U5F-M-EXPREE
H6755 U5F-M-EXPREE

H6721 P_GND1 P_GND2 P_GND3 P_GND4 P_GND5 P_GND6 P_NGD7 7D_D104_D110_D114
H6728 P_GND1 P_GND2 P_GND3 P_GND4 P_GND5 P_GND6 P_NGD7 7D_D114_D104_D110

H6722 OT111X99BIDO91X79
H6723 OT111X99BIDO91X79
H6756 OB169X94DO130X55
H6757 OB169X94DO130X55
H6760 CT354CRBI114D94
H6761 O79X67DO79X67N
H6762 C67D67N
H6764 O79X67DO79X67N
H6763 C67D67N
H6746 CT354CRB315x335D94
H6747 CT354CRB315x335D94

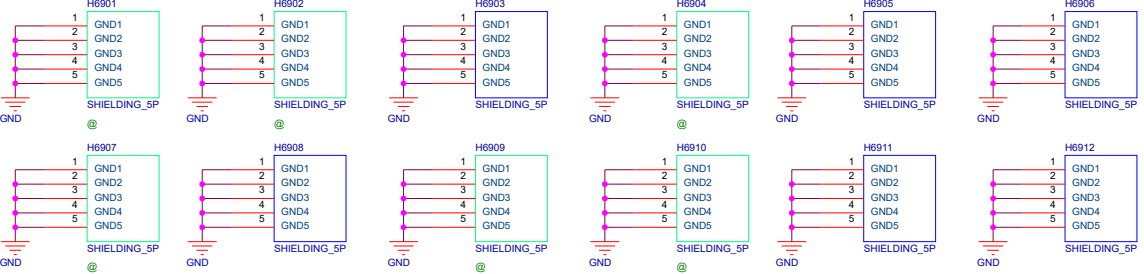
<COMPONMENT BOT>

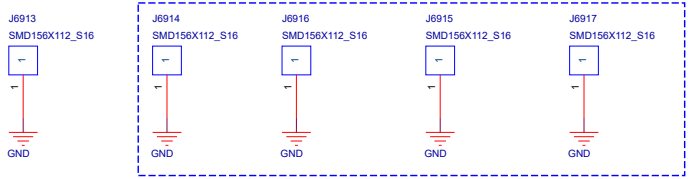


ASUSTeK COMPUTER INC. NB3	Title :	I/O board FUNC key	
	Engineer:	EE	
Size: C	Project Name:	N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet	67 of 102	

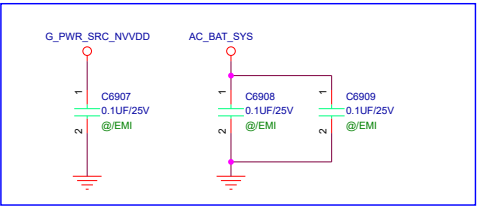
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : OTH_for test only	
	Engineer: EE	
Size: A	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 68 of 102	





2015.10.07 For EMI Request



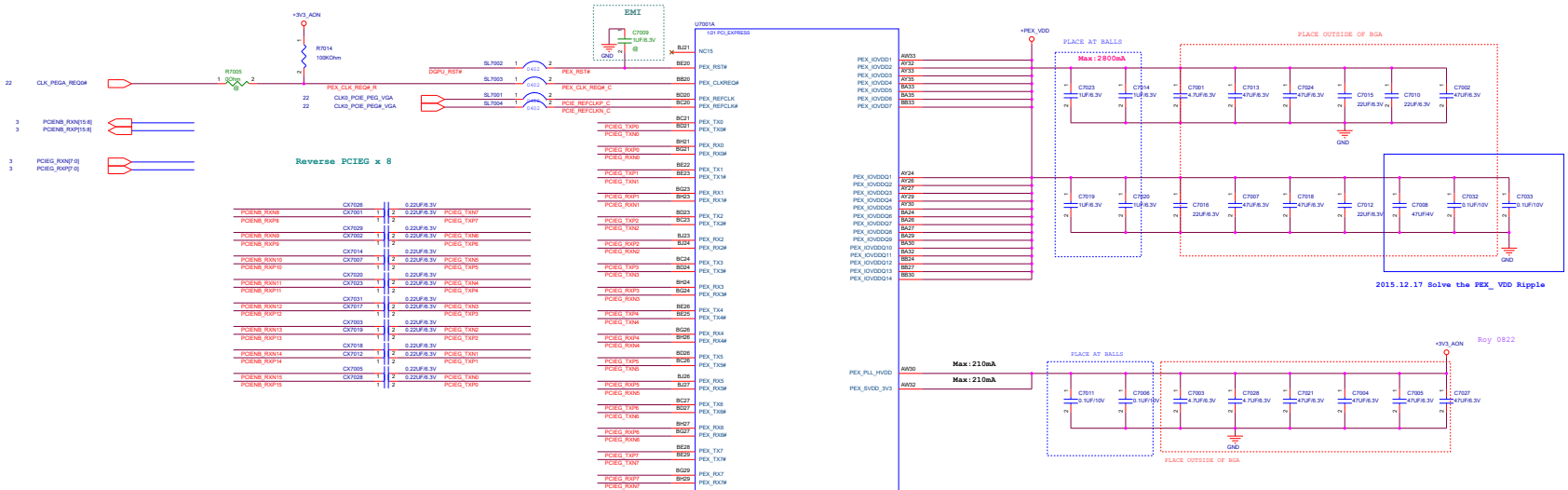
2015.12.16 EMI Reserve

<Variant Name>

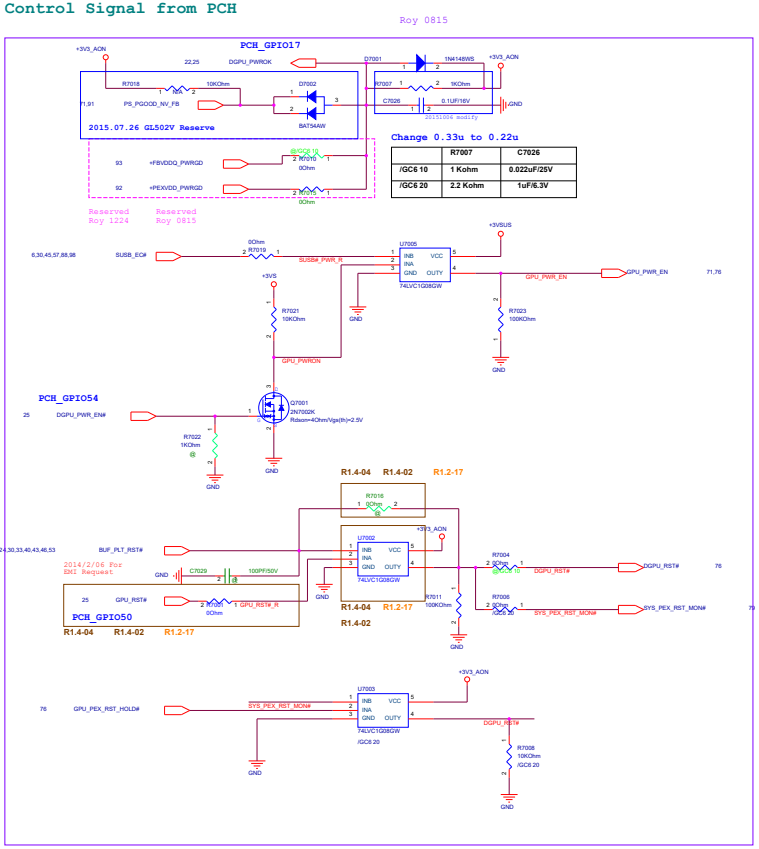
ASUSTeK COMPUTER INC. NB1	Title : OTH_EMI	
	Engineer: EE	
Size: B	Project Name: N501VW	Rev: 1.0
Date: Friday, December 18, 2015	Sheet 69 of 102	

PCI EXPRESS_Graphics

REVERSED Type PCIE X16

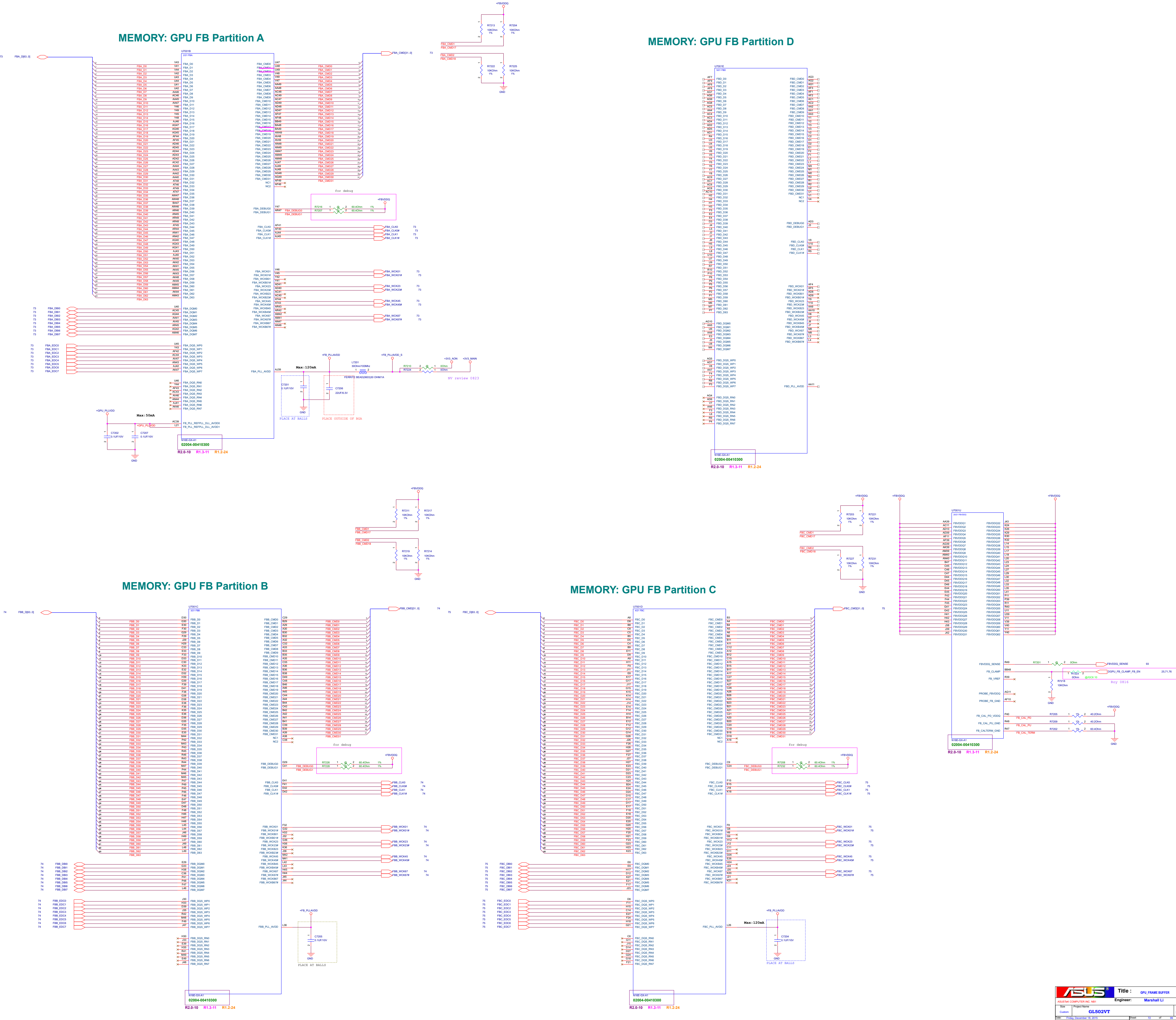


Control Signal from PCH



	R7007	C7026
/GC6 10	1 Kohm	0.022uF/25V
/GC6 20	2.2 Kohm	1uF/6.3V

Main Board


MEMORY: GPU FB Partition A
MEMORY: GPU FB Partition D
MEMORY: GPU FB Partition B
MEMORY: GPU FB Partition C
for debug
PLACE AT BALLS
PLACE OUTSIDE OF BGA
02004-00410300
R2.0-10 R1.3-11 R1.2-24
Title : GPU_FRAME BUFFER
Engineer: Marshall Li
GL502VT

MF=0 Normal

FBB Partition Memory (1 of 2)

GDD5 MODE SELECTION

MODE	MF	EEC1	EDC3
x36	0	0	VDDQ
x32	0	VDDQ	VDDQ
x36 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

CK External Termination

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03000-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03000-00030200 SAMSUNG/K4G4132IFC-HC03 ,Strap: 0x3

3rd: P/N:03000-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

R1.2-02 R1.2-25

03008-00030100

MF=1 Mirror

FBB Partition Memory (2 of 2)

CK External Termination

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03000-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03000-00030200 SAMSUNG/K4G4132IFC-HC03 ,Strap: 0x3

3rd: P/N:03000-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

R1.2-02 R1.2-25

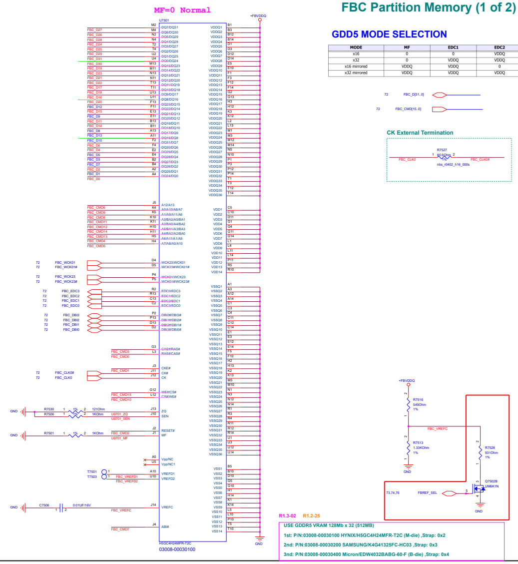
03008-00030100

Title :	VRAM-CHANNEL B		
Engineer:	Marshall Li		
Size	Project name		Rev
Custom	GL502VT		0.1
Date: 2015-09-08	Sheet 4	of 55	

Main Board

FBC Partition Memory (1 of 2)

MF=0 Normal



GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

CK External Termination

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

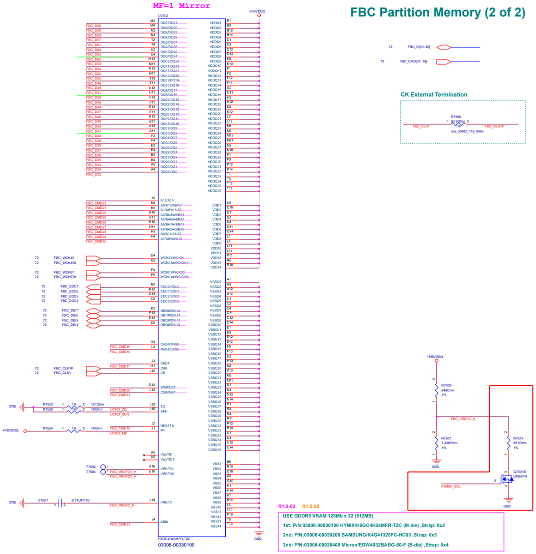
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

FBC Partition Memory (2 of 2)

MF=1 Mirror



CK External Termination

R1.3-02 R1.2-25

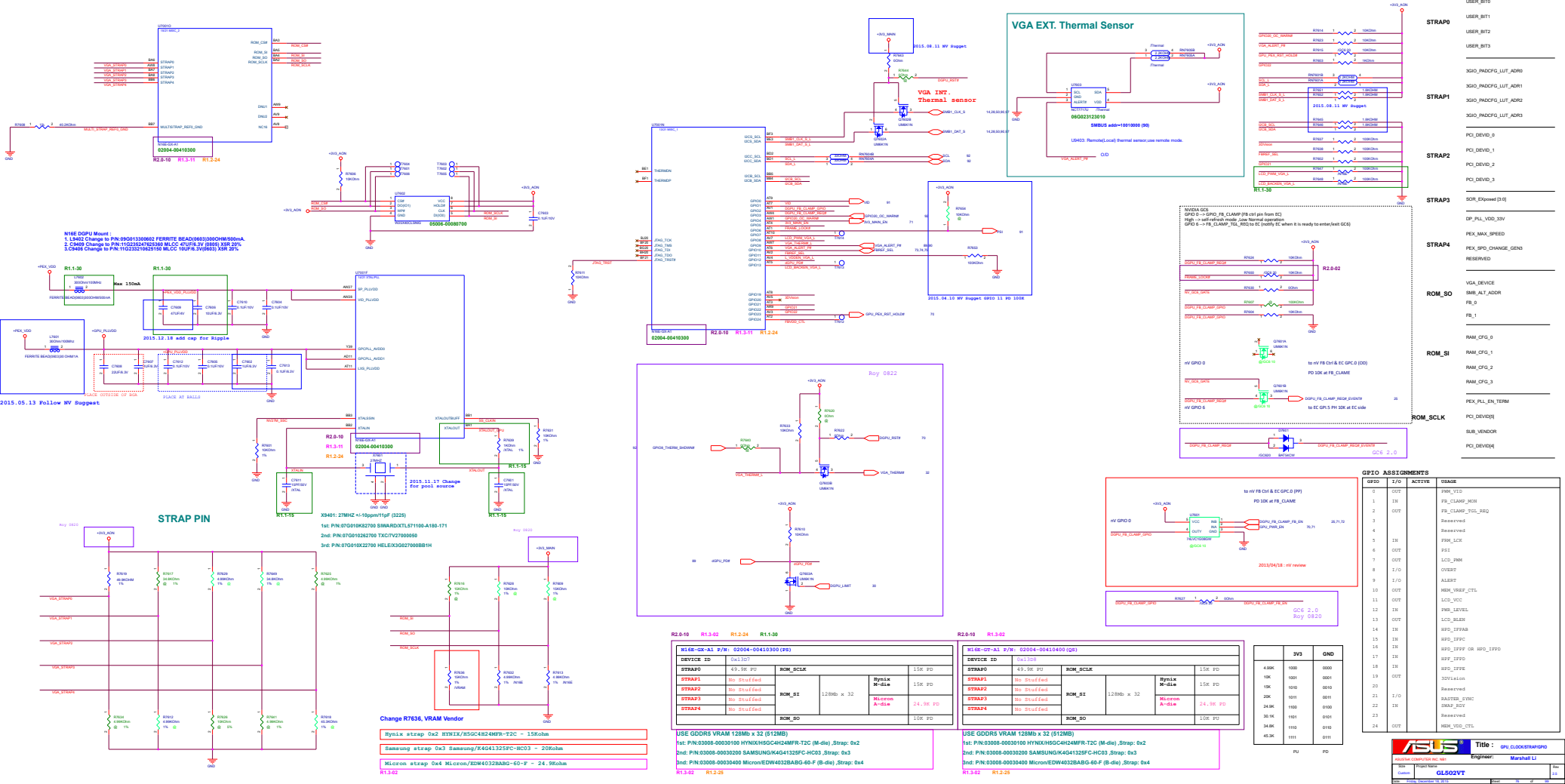
USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

Title :	VRAM-CHANNEL C		
ASUSTeK COMPUTER INC. NB1	Engineer:	Marshall Li	
Size: Custom	Project Name: GL502VT		Rev: 2.5
Date: Friday, December 18, 2015	Sheet 75 of 99		



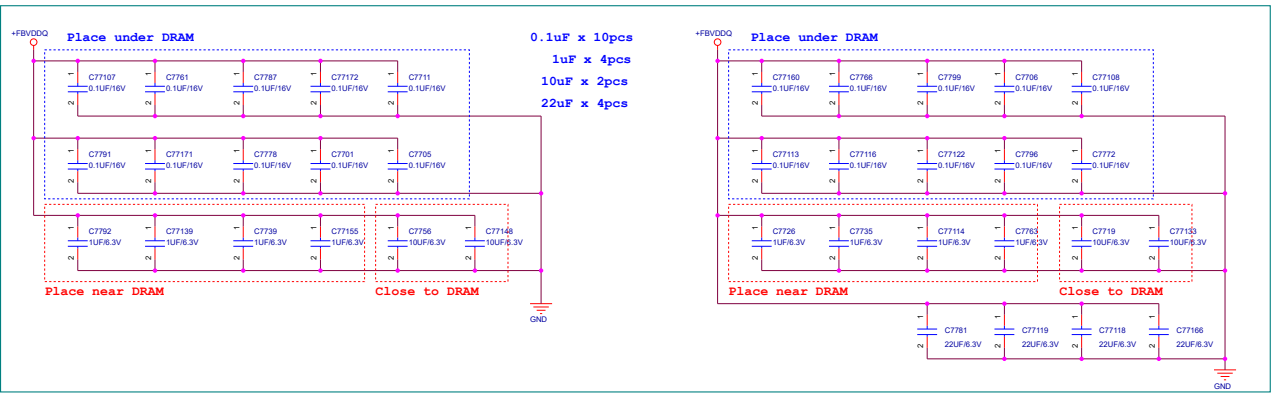
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	OUT		PWM_VID
1	IN		FB_CLAMP_MON
2	OUT		FB_CLAMP_TGL_REQ
3			Reserved
4			Reserved
5	IN		PSM_LCK
6	OUT		PSI
7	OUT		LCD_PWM
8	I/O		CURSEL
9	I/O		ALERT
10	OUT		MEM_VREF_CTL
11	OUT		LCD_VCC
12	IN		PWR_LEVEL
13	OUT		LCD_BLEN
14	IN		HPD_IFPAB
15	IN		HPD_IFPC
16	IN		HPD_IFPF OR HPD_IFPD
17	IN		HPD_IFPD
18	IN		HPD_IFPE
19	OUT		3DVision
20			Reserved
21	I/O		RASTER_SYNC
22	IN		SWAP_RDY
23			Reserved
24	OUT		MEM_VDD_CTL

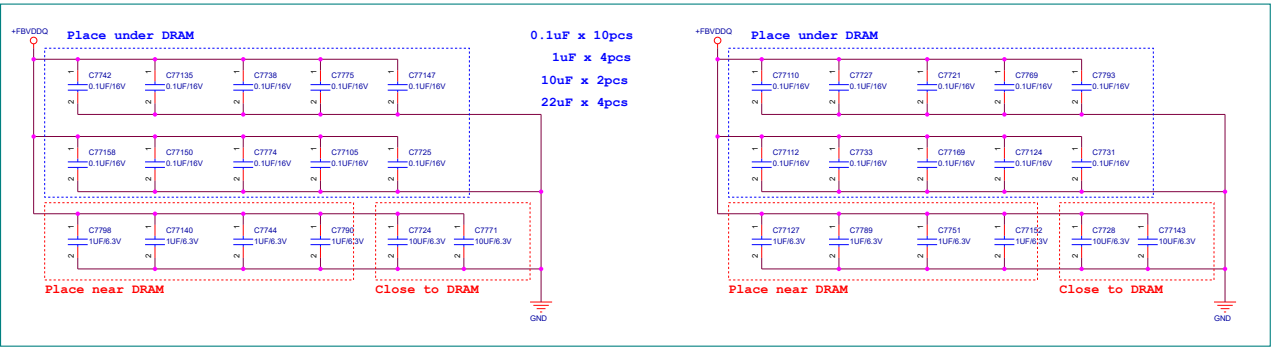
	3V3	GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111
	PU	PD

Title :	GPU_CLOCK/STRAP/GPIO
Engineer:	Marshall Li
Size: Custom	Project Name: GL502VT
Rev: 2.0	
Date: Friday, December 18, 2015	Sheet: 76 of 98

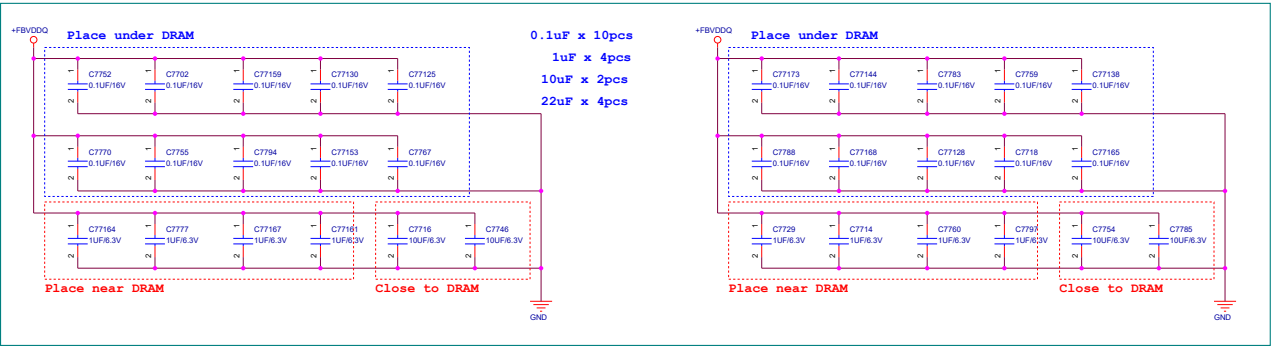
VRAM Chanel A



VRAM Chanel B



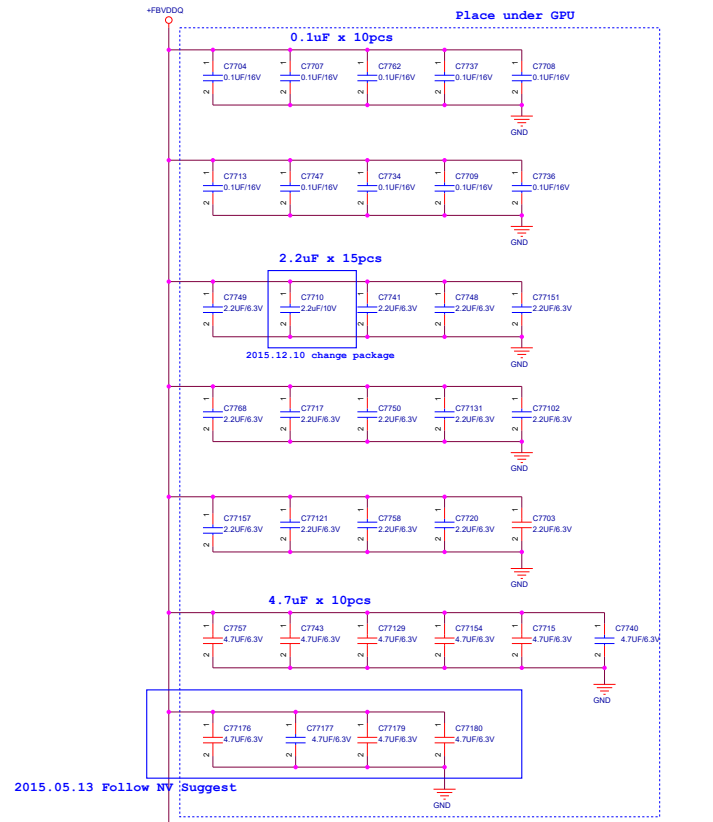
VRAM Chanel C

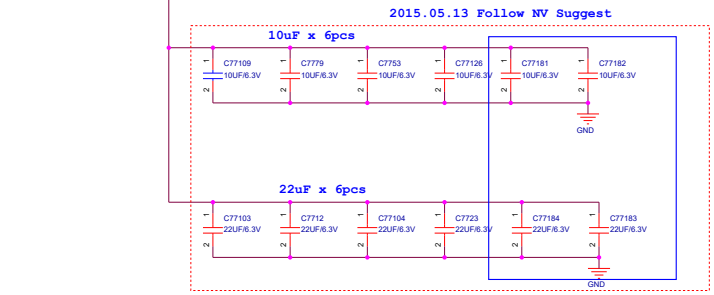


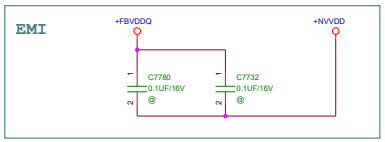
VRAM Chanel D

www.teknisi-indonesia.com

VRAM PWR_FBVDDQ

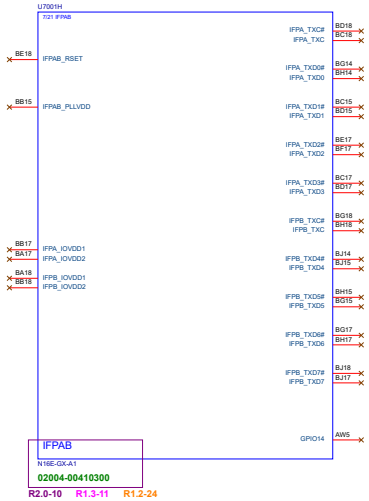


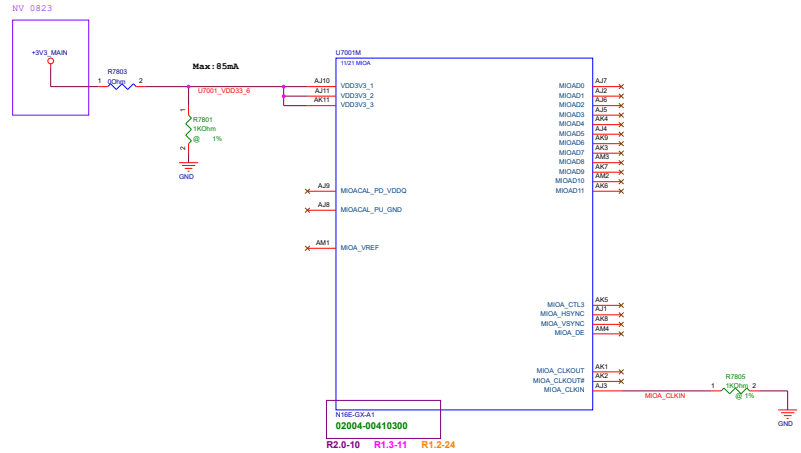


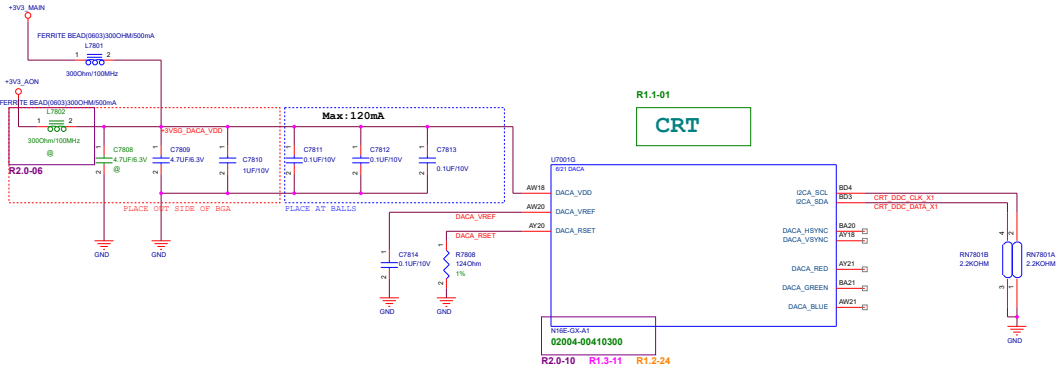


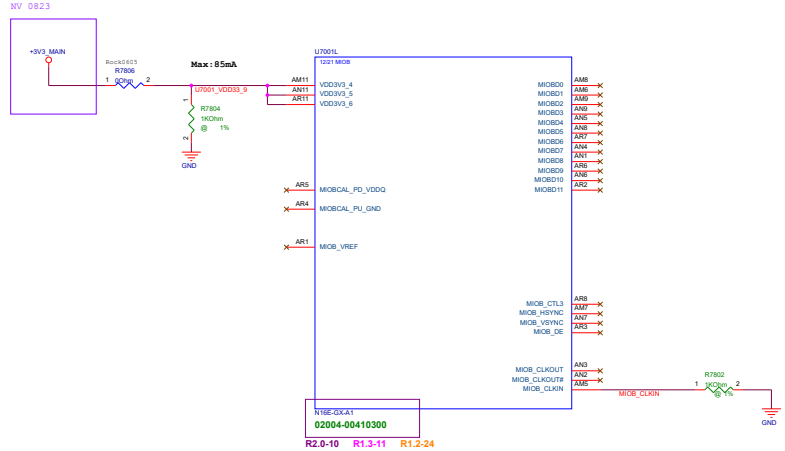
ASUSTeK COMPUTER INC. NB1	Title : VRAM CAP.	
	Engineer: Marshall Li	
Size: Custom	Project Name: GL502VT	Rev: 2.5
Date: Friday, December 18, 2015	Sheet 77 of 99	

LVDS







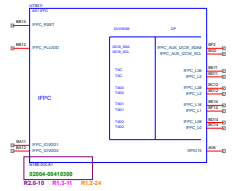


ASUSTeK COMPUTER INC. NB1	Title : GPU_LVDS/ CRT		
	Engineer: Marshall Li		
Size: Custom	Project Name: GL502VT		Rev: 2.5
Date: Friday, December 18, 2015	Sheet 78 of 99		

1.7901 FERISTE BEAD(0603)300OHM/1A
1st Source: P/N:09GD013300800 TAI-TECH/HCB1608KF-301T10
2nd Source: P/N:09GD013308800 MAXECHO/ACMS160808A301 1A

R1.1-01

DP(Intel Thunderbolt)

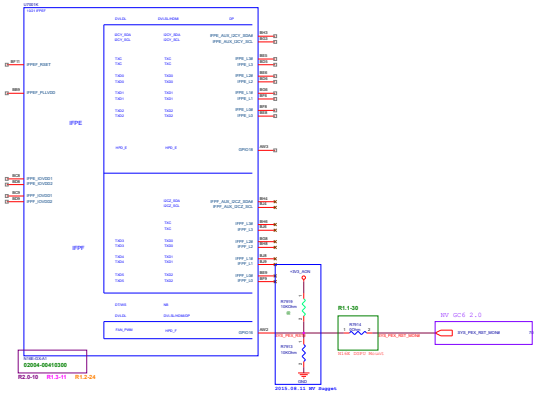


R1.1-01

EDP(2Lane Panel)

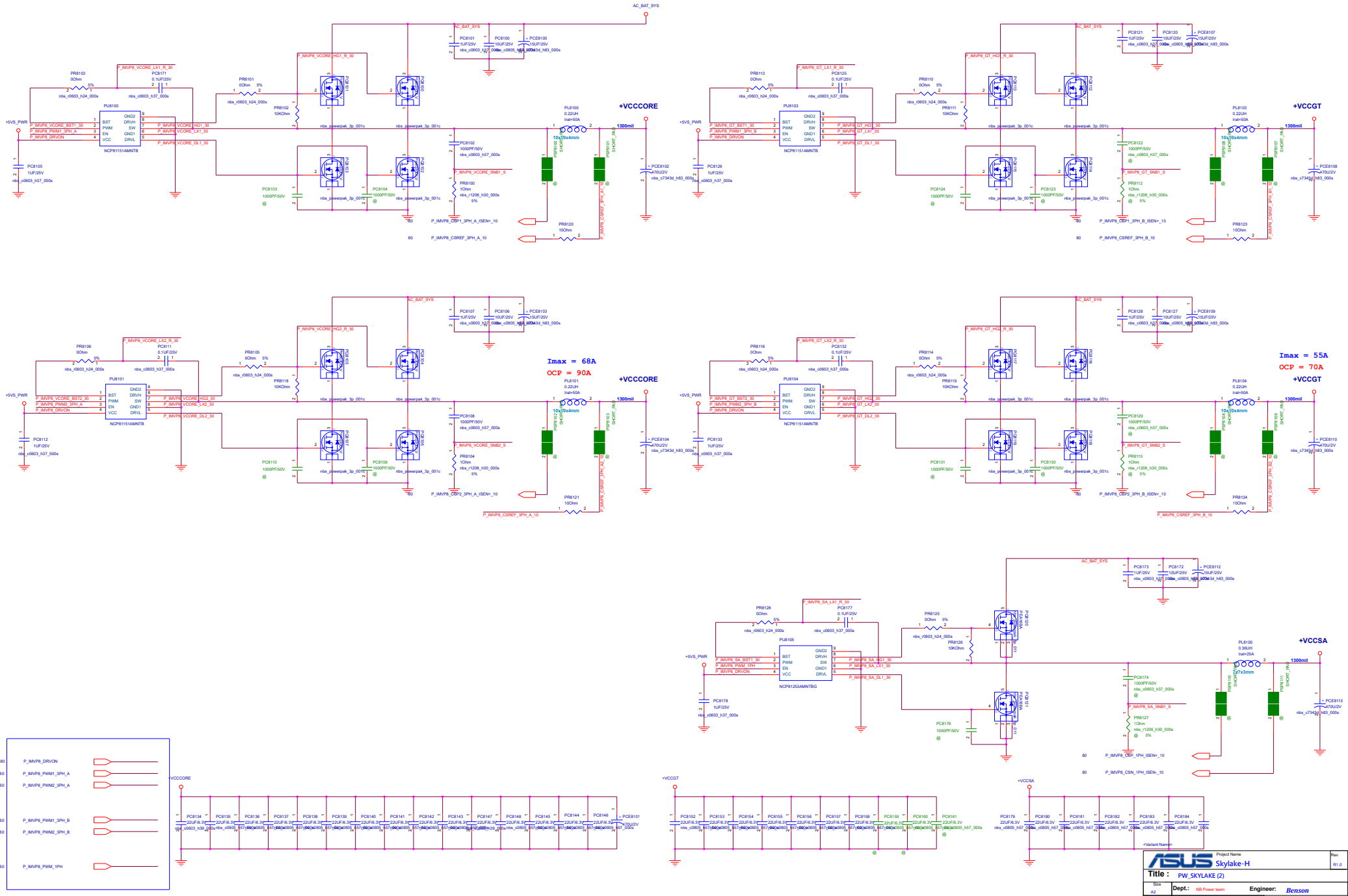
R1.1-01

HDMI



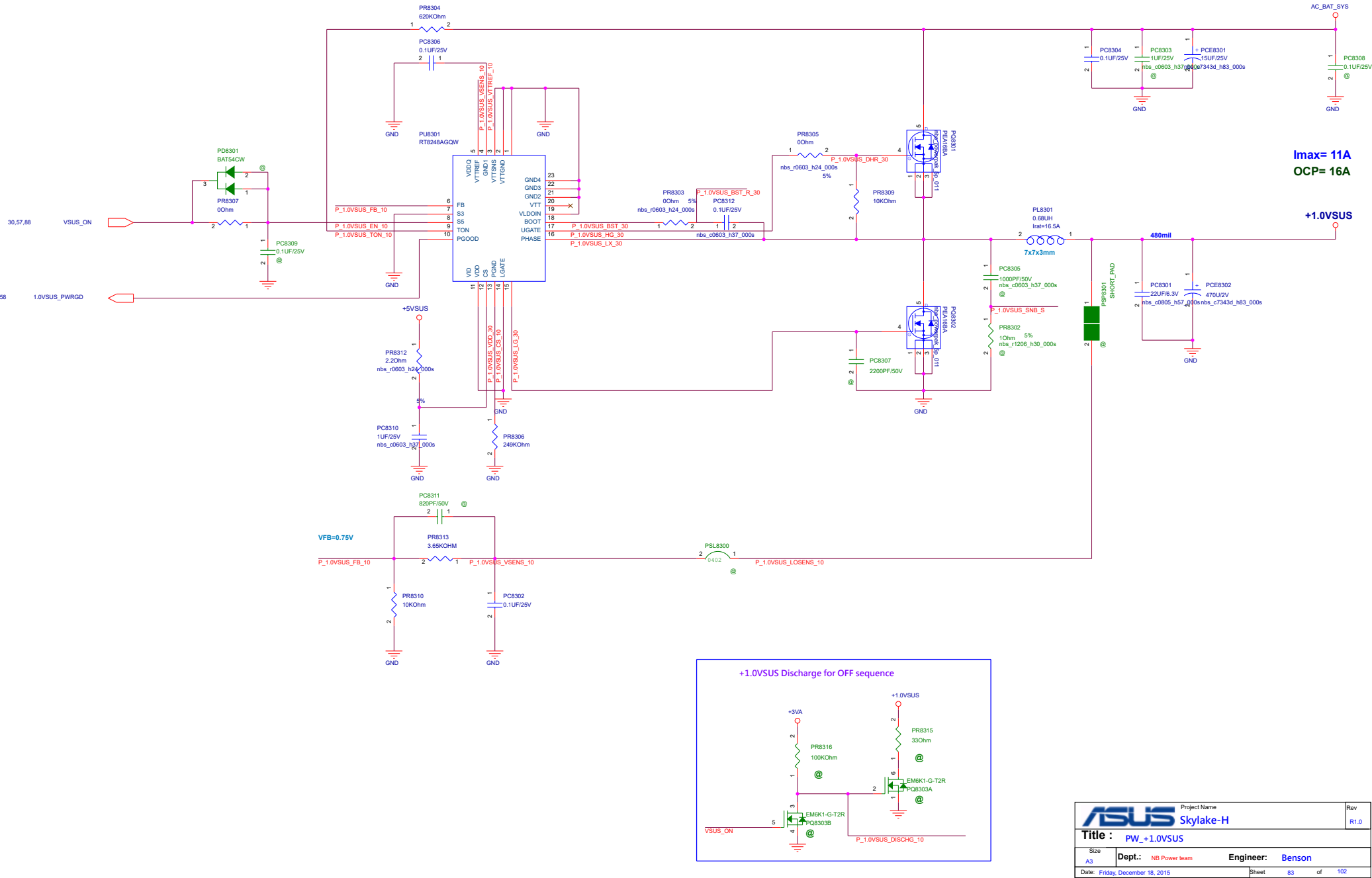
ASUSTeK COMPUTER INC.(MB)	Title :	GPU_SPECIFICNEW	
	Engineer:	Marshall Li	
Size: Custom	Project Name: GL502VT		Rev: 1.0
Date: Friday, December 18, 2015	Sheet 10 of 50		

Skylake IMVP8 Power [For CPU]



Project Name: GL502VT		Rev: 1.0
Title : POWER_+VGFX_CORE		
Size: A	Dept.: NB Power team	Engineer: Marshall Li
Date: Friday, December 18, 2015	Sheet 82 of 102	

+1.0VSUS [For PCH]



Project Name: Skylake-H			Rev: R1.0
Title : PW_+1.0VSUS			
Size: A3	Dept.: NB Power team	Engineer: Benson	
Date: Friday, December 18, 2015	Sheet 83 of 102		

<Variant Name>

	Project Name **Skylake-H**	Rev R1.0

Title : PW_+VCCIO

Size			
A3	**Dept.:** NB Power Team	**Engineer:**	**Benson**

Date: Friday, December 18, 2015	Sheet	84	of	102

Project Name

GL502VT

Rev

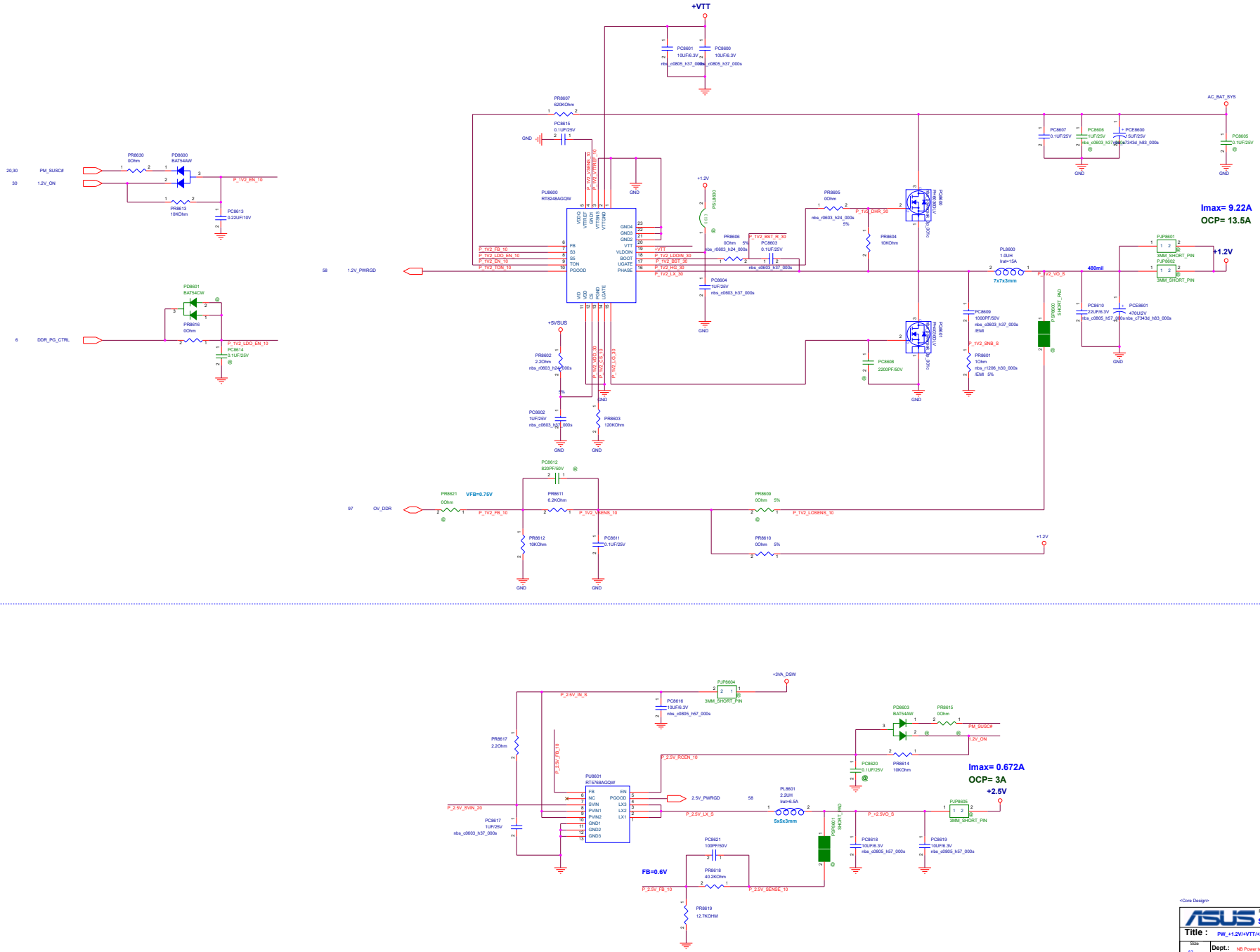
1.0

Title : POWER_+VGFX_CORE

Size	Dept.:	Engineer:
A	NB Power team	Marshall Li

Date:	Sheet		
Friday, December 18, 2015	85	of	102

+1.2V / +VTT / +2.5V[For Memory]

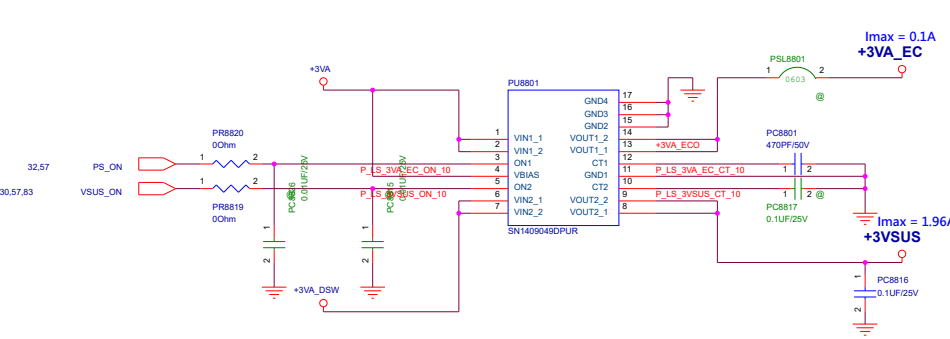


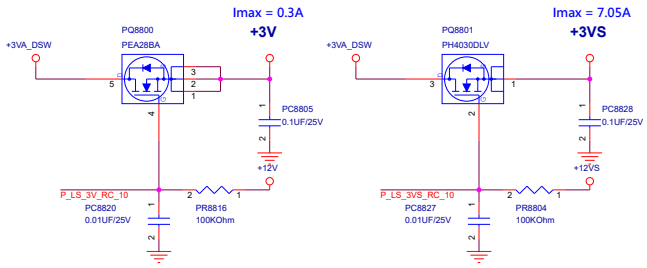
<Core Design>

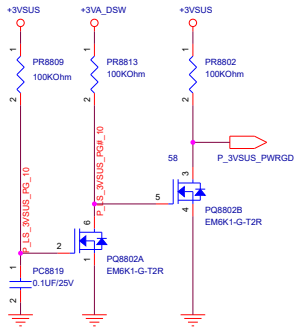
ASUS	Project Name: Skylake-H		Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: Benson	
Date: Friday, December 18, 2015	Sheet: 86 of 105		

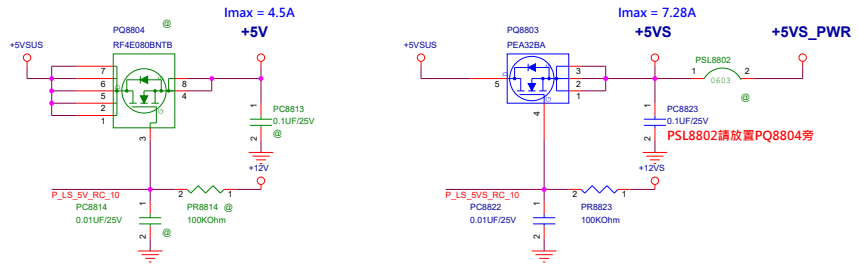
Load Switch

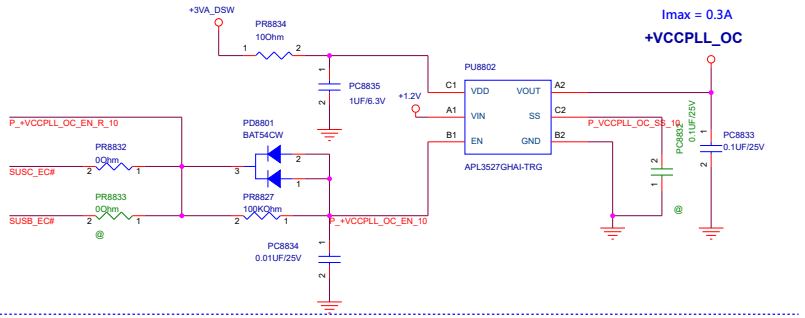
Main Board



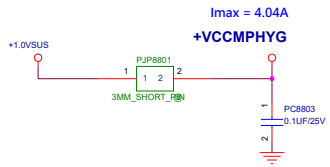


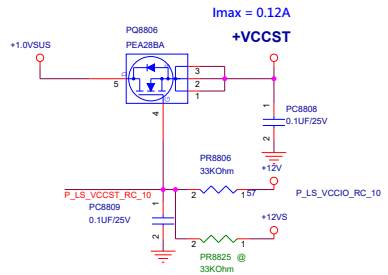


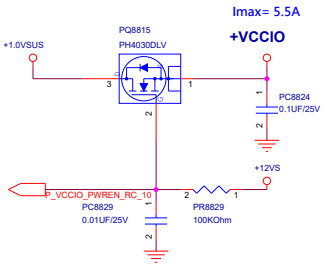


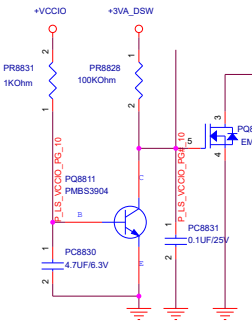


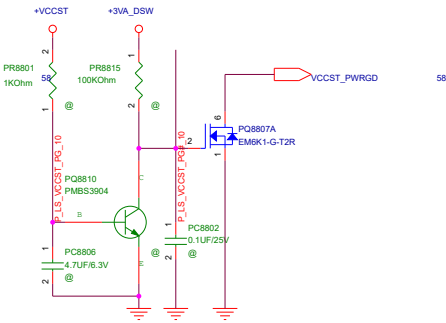
PJP8801 需開鋼板

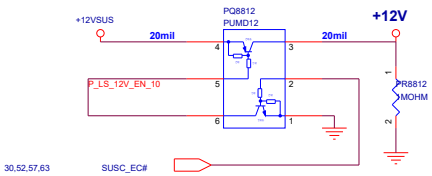


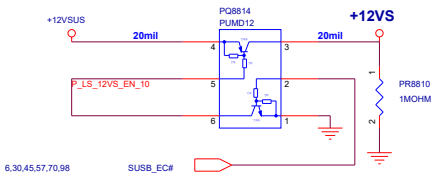




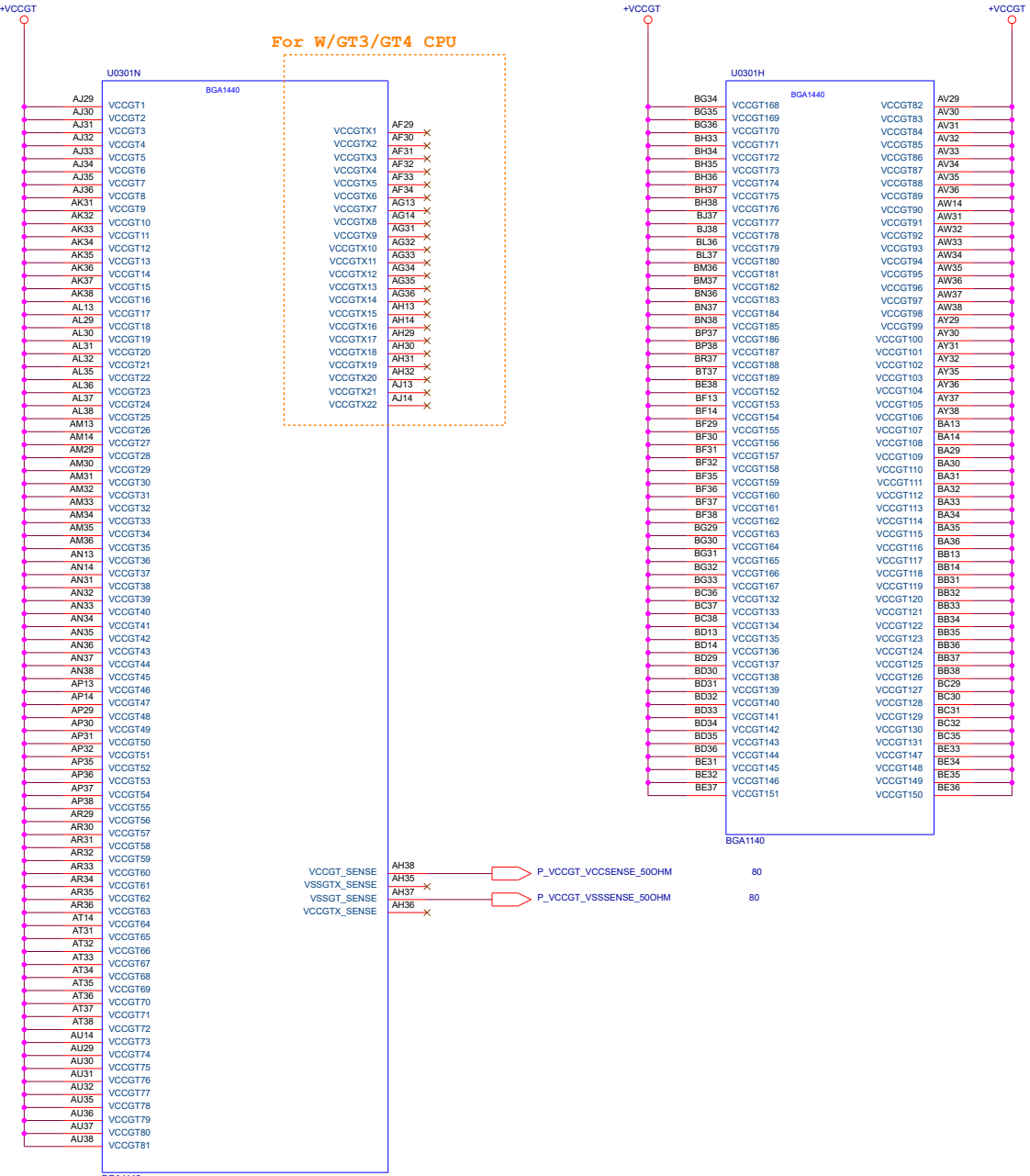








Project Name: Skylake-H			Rev: 1.0
Title: PW_LOAD SWITCH			
Size: A3	Dept.: NB Power team	Engineer: Benson	
Date: Friday, December 18, 2015	Sheet 88 of 102		



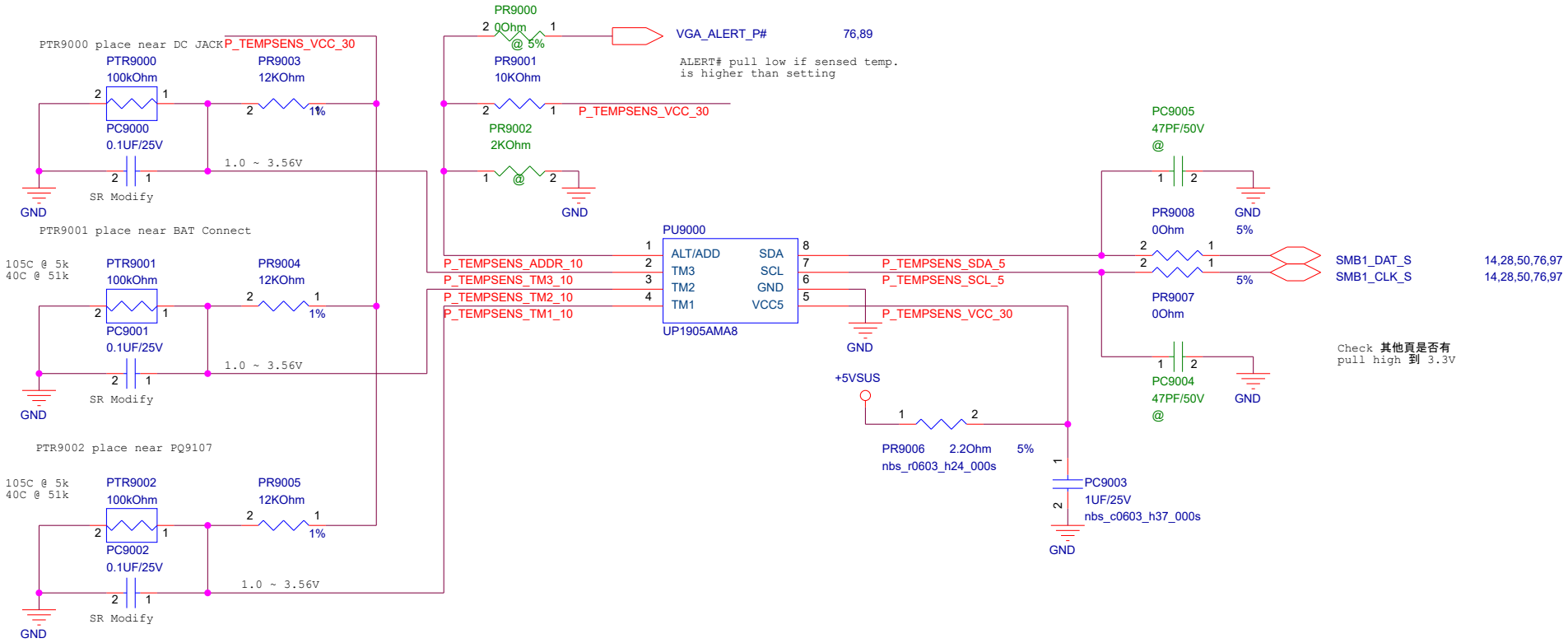
Project Name: N501VW		Rev: 1.0
Title : NB_****		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, December 18, 2015	Sheet 9 of 102	

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

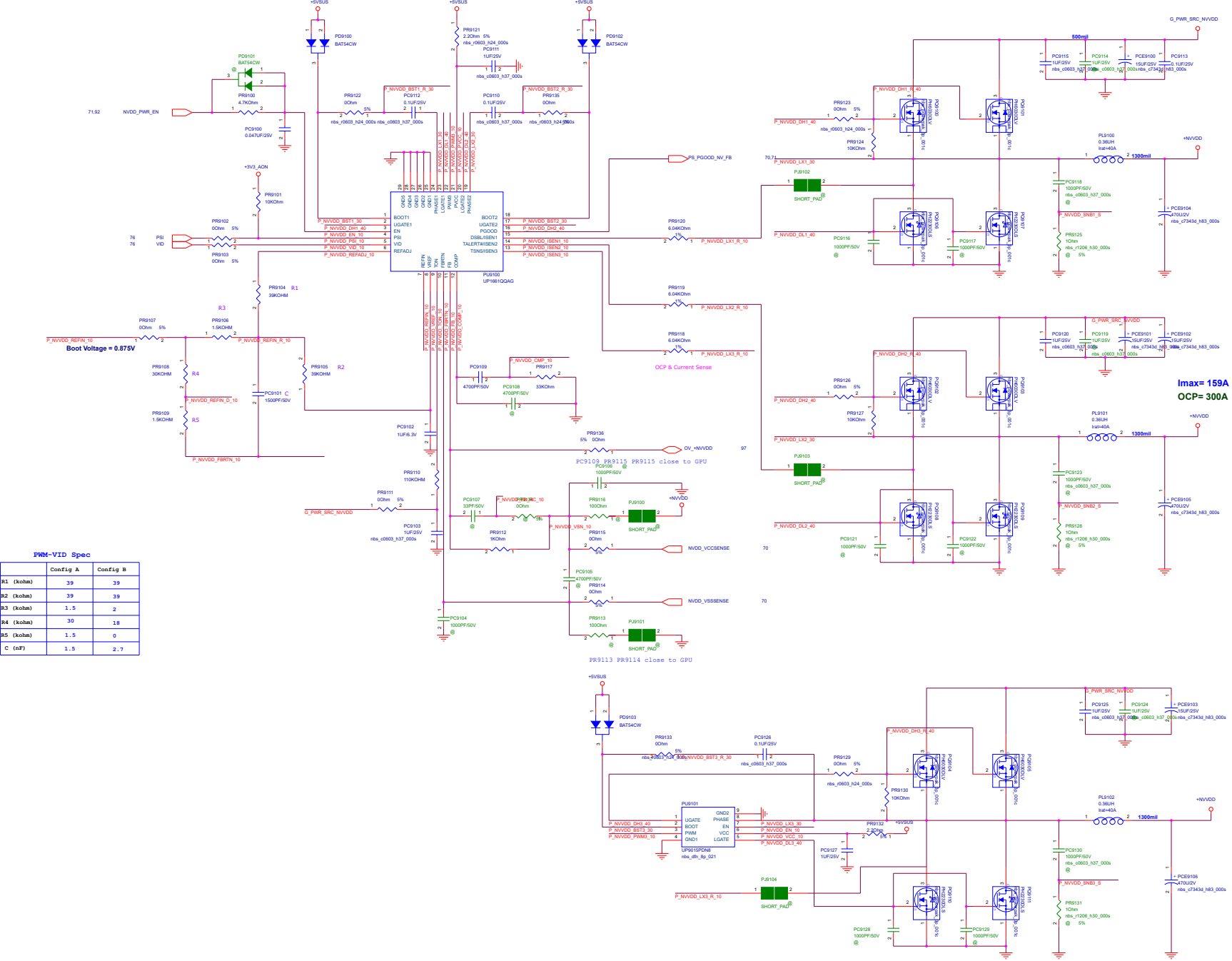
Register Address

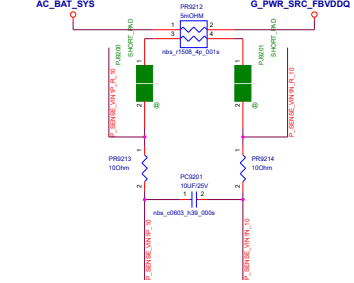
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

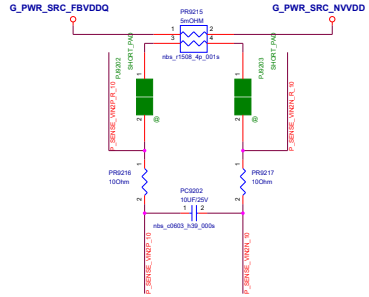


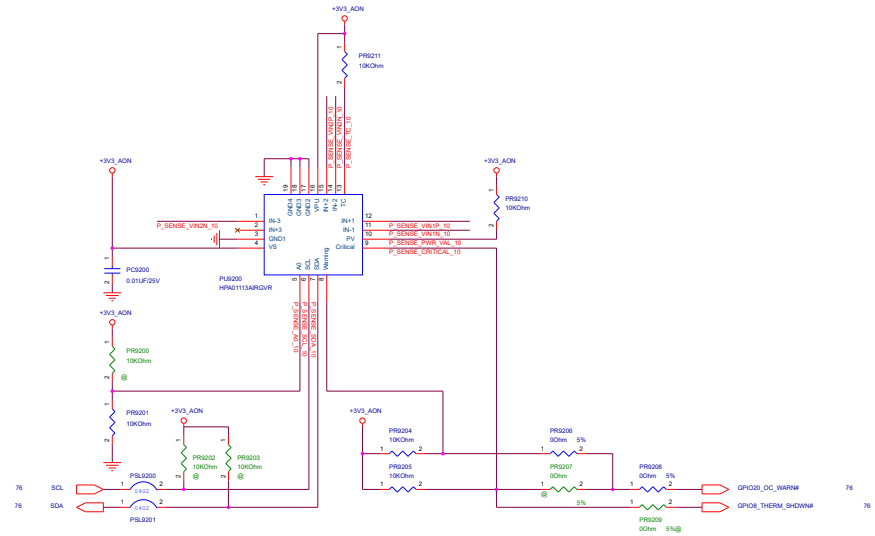
<Variant Name>

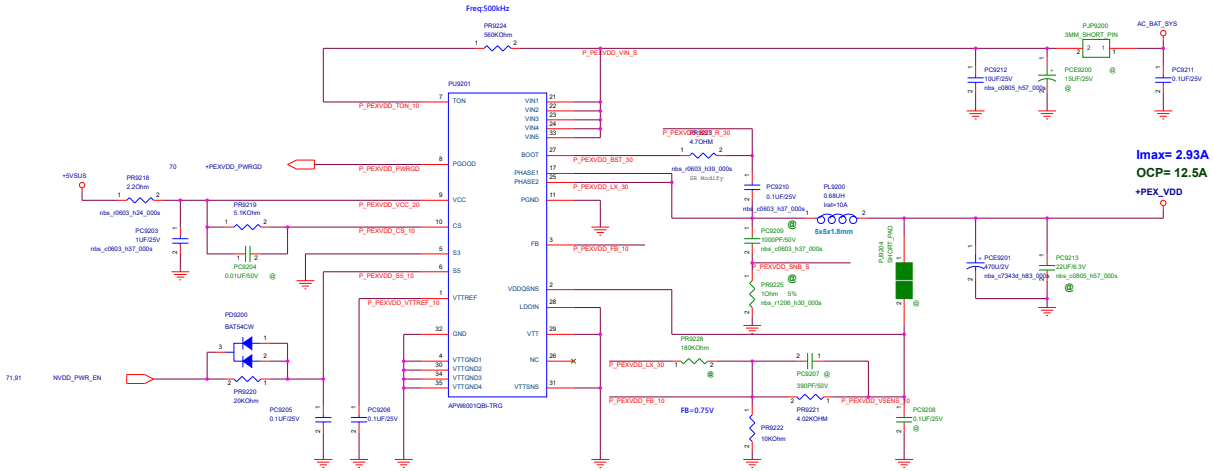
Project Name: Skylake-H		Rev: R1.0
Title : PW_PROTECTION		
Size: A4	Dept.: NB Power Team	Engineer: Benson
Date: Friday, December 18, 2015	Sheet 90 of 102	


Boot Voltage = 0.875V
OCP & Current Sense
Imax= 159A
OCP= 300A
PC9109 PR9115 PR9115 close to GPU
PR9113 PR9114 close to GPU
PWM-VID Spec
Config A
Config B
R1 (kohm) 39 39
R2 (kohm) 39 39
R3 (kohm) 1.5 2
R4 (kohm) 30 18
R5 (kohm) 1.5 0
C (nF) 1.5 2.7
Project Name Skylake-H
Rev R1.0
Title : PW_+NVVDD
Dept.: NB Power Team
Engineer: Benson
Date: Friday, December 18, 2015
Sheet 91 of 102







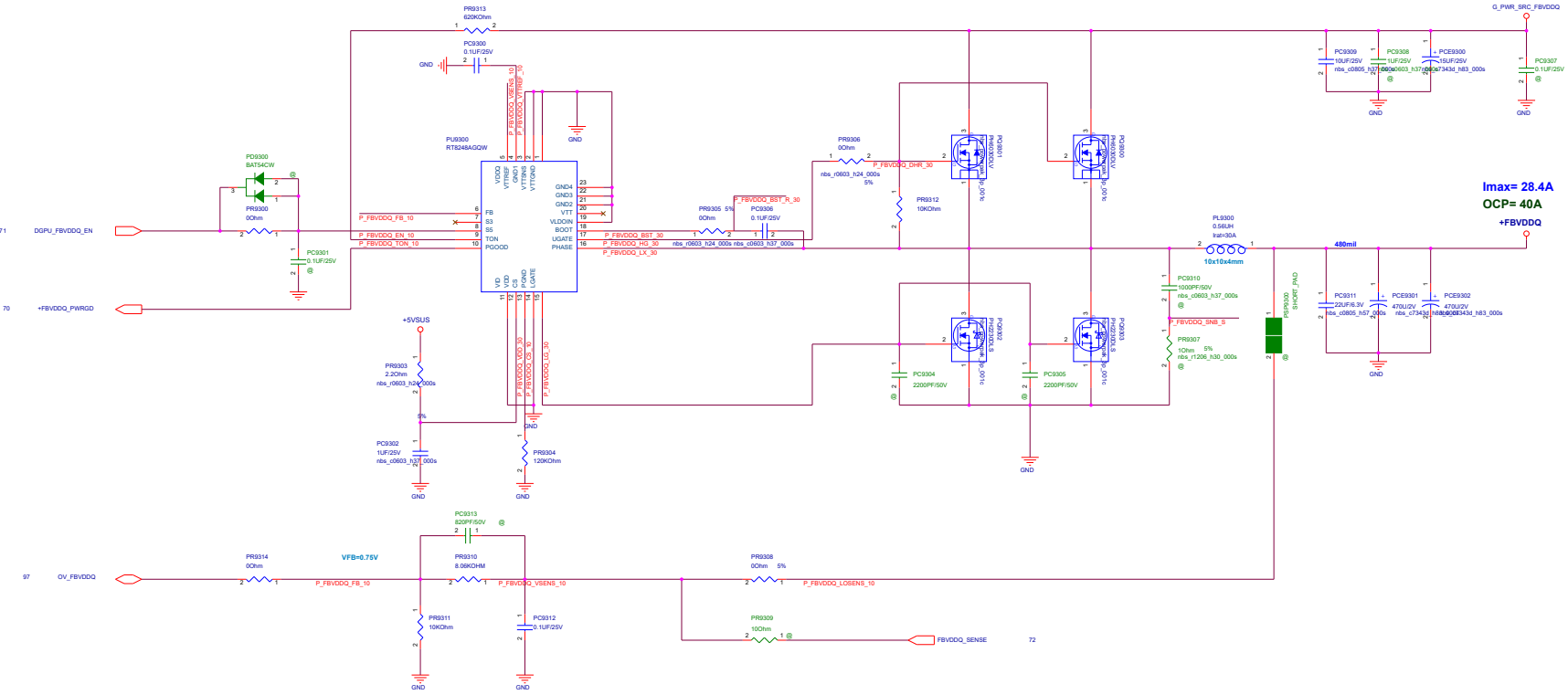


PR9221	APW6001Q_Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

<Variant Name>

ASUS	Project Name: Skylake-H	Rev: R1.0
Title : PW_PEX_VDD/IPC		
Size: A2	Dept.: NB Power Team	Engineer: Benson
Date: Friday, December 18, 2015	Sheet: 92 of 102	

+FBVDDQ [For FRAM]



<Variant Name>

ASUS	Project Name: Skylake-H	Rev: R1.0
Title : PW_+FBVDDQ		
Size: A2	Dept.: NB Power Team	Engineer: Benson
Date: Friday, December 18, 2015	Sheet 93 of 102	

Project Name

GL502VT

Rev

2.3

Title : INPUT SENSE

Size	Dept.:	Engineer:
Custom	ASUS PWR NB1	Marshall Li

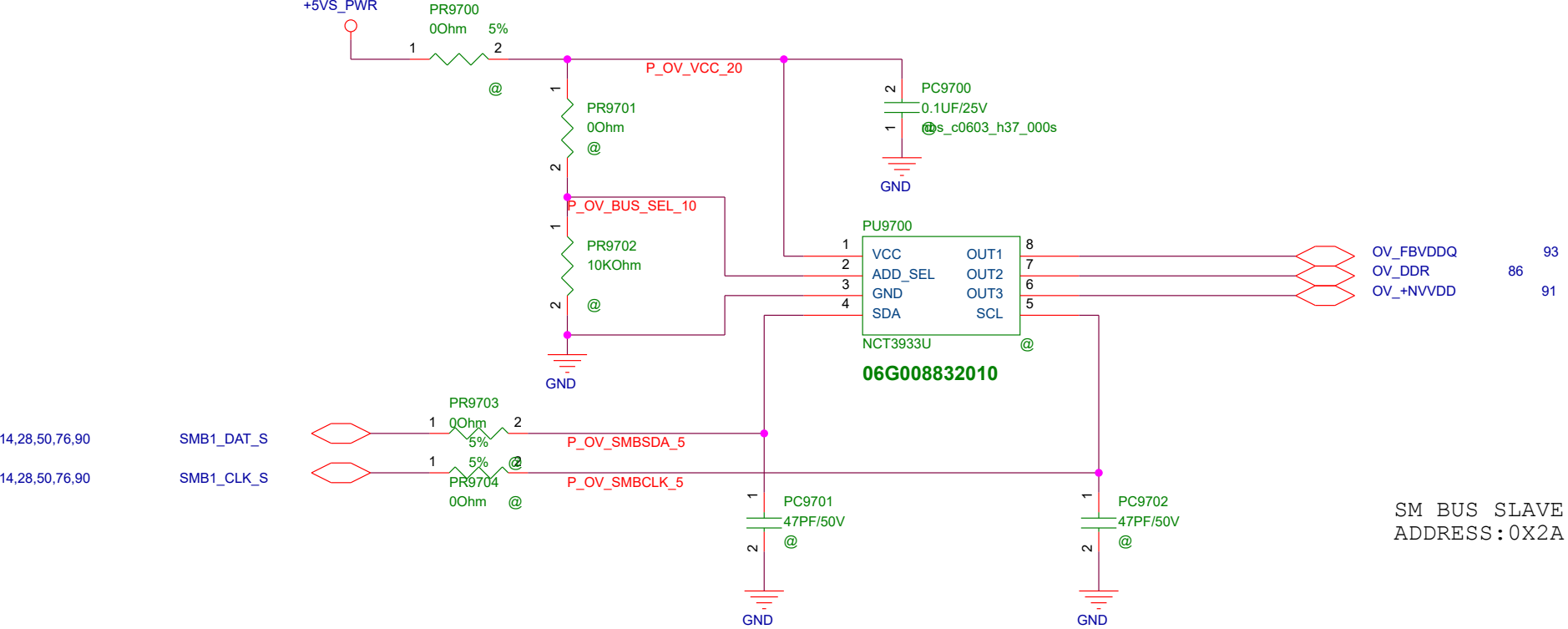
Date:	Sheet	of
Friday, December 18, 2015	94	99

Main Board

ASUS	Project Name: GL502VT	Rev: 1.0
Title :	POWER_+VGFX_CORE	
Size: B	Dept.: NB Power team	Engineer: Marshall Li
Date: Friday, December 18, 2015	Sheet 95 of 102	

Main Board

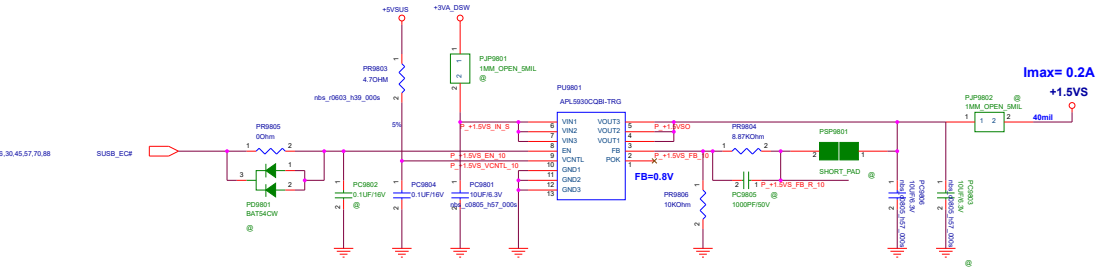
Project Name: GL502VT		Rev: 1.0
Title : POWER_+VGFX_CORE		
Size: B	**Dept.:** NB Power team	**Engineer:** Marshall Li
Date: Friday, December 18, 2015	Sheet 96 of 102	



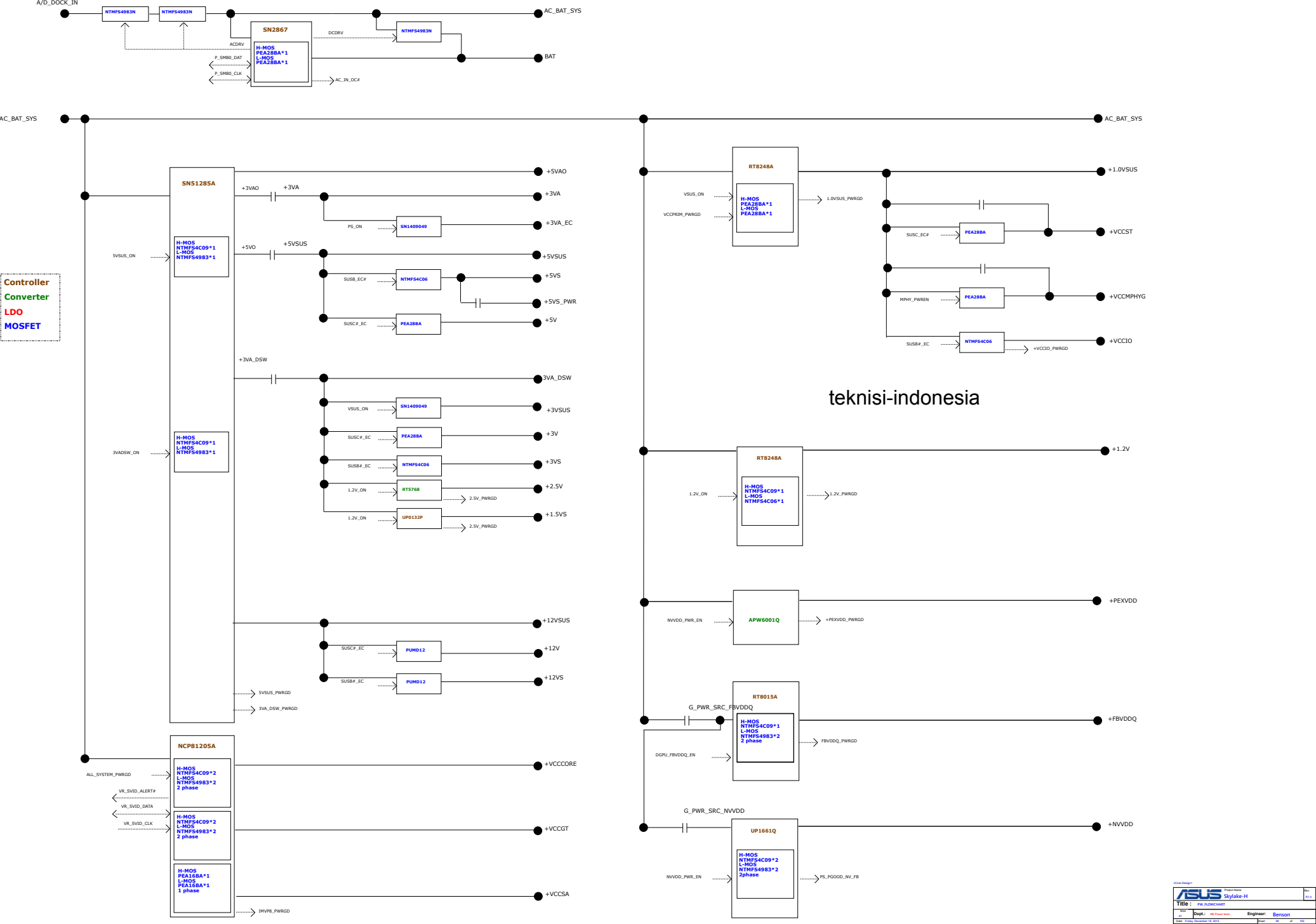
<Variant Name>

Project Name: Skylake-H		Rev: R1.0
Title : PW_OV		
Size: A	Dept.: NB Power team	Engineer: Benson
Date: Friday, December 18, 2015	Sheet 97 of 102	

+1.5VS



ASUS	Project Name: GL502VT		Rev: 1.0
Title : POWER_+V1.5VS			
Size: A4	Dept.: NB Power team	Engineer: Benson	
Date: Friday, December 18, 2015	Sheet 98 of 102		


A/D_DOCK_IN
NTMFS4983N
NTMFS4983N
AC_BAT_SYS
SN2867
DCDRV
NTMFS4983N
ACDRV
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
BAT
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
AC_BAT_SYS
SN51285A
+5VAO
+3VAO
+3VA
+3VA
PS_ON
SN1409049
+3VA_EC
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*1
5VSUS_ON
+5VO
+5VSUS
+5VSUS
SUSB_EC#
NTMFS4C06
+5VS
+5VS_PWR
SUSC#_EC
PEA28BA
+5V
Controller
Converter
LDO
MOSFET
+3VA_DSW
3VA_DSW
VSUS_ON
SN1409049
+3VSUS
SUSC#_EC
PEA28BA
+3V
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*1
3VADSW_ON
SUSB#_EC
NTMFS4C06
+3VS
1.2V_ON
RT5768
+2.5V
2.5V_PWRGD
1.2V_ON
UP0132P
+1.5VS
2.5V_PWRGD
+12VSUS
SUSC#_EC
PUMD12
+12V
SUSB#_EC
PUMD12
+12VS
5VSUS_PWRGD
3VA_DSW_PWRGD
NCP81205A
+VCCCORE
ALL_SYSTEM_PWRGD
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
2 phase
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
2 phase
+VCCGT
H-MOS
PEA16BA*1
L-MOS
PEA16BA*1
1 phase
+VCCSA
IMVP8_PWRGD
AC_BAT_SYS
RT8248A
+1.0VSUS
VSUS_ON
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
1.0VSUS_PWRGD
VCCPRIM_PWRGD
SUSC_EC#
PEA28BA
+VCCST
MPHY_PWREN
PEA28BA
+VCCMPHYG
SUSB#_EC
NTMFS4C06
+VCCIO_PWRGD
+VCCIO
teknisi-indonesia
RT8248A
+1.2V
1.2V_ON
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
1.2V_PWRGD
APW6001Q
+PEXVDD
NVVDD_PWR_EN
+PEXVDD_PWRGD
RT8015A
G_PWR_SRC_FBVDDQ
+FBVDDQ
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*2
2 phase
FBVDDQ_PWRGD
DGPU_FBVDDQ_EN
G_PWR_SRC_NVVDD
+NVVDD
UP1661Q
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
2phase
NVVDD_PWR_EN
PS_PGOOD_NV_FB
ASUS
Project Name
Skylake-H
Rev
0.1
Title :
PW_FLOWCHART
Size
A4
Dept.:
NB Power team
Engineer:
Benson
Date:
Friday, December 14, 2012
Sheet
50
of
100

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(pull up to +3VSUS)

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

T0=20ms (spec.>=10ms)

T1<200ms(check)

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(falling edge)

(to EC) 8 PWR_SW#

T2=50ms

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power)

+1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

T3=2ms (spec.>=1ms)

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

T4=1.25ms

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD

(power to CPU)

GFX_VID

+VGFX_CORE

T5=60us(typ.)

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

T6=110ms (spec.>=99ms)

(EC to power) CPU_VRON

T7=10~100us

19 +VCCIN

CLK_PWRGD

(inversion of CLK_EN#)

T8=3~20ms

(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

T9=10ms

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#

<Variant Name>

ASUSTeK COMPUTER

Title : Power On Timing

Engineer: EE

Size	Project Name	Rev
C	N501VW	1.0

Date: Friday, December 18, 2015 Sheet 100 of 102

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(pull up to +3VSUS)

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

T0=20ms (spec.>=10ms)

T1<200ms(check)

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(falling edge)

(to EC) 8 PWR_SW#

T2=50ms

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power)

+1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

T3=2ms (spec.>=1ms)

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

T4=1.25ms

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD

(power to CPU)

GFX_VID

+VGFX_CORE

T5=60us(typ.)

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

T6=110ms (spec.>=99ms)

(EC to power) CPU_VRON

T7=10~100us

19 +VCCIN

CLK_PWRGD

(inversion of CLK_EN#)

T8=3~20ms

(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

T9=10ms

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#

<Variant Name>

ASUSTeK COMPUTER

Title : Power On Timing

Engineer: EE

Size	Project Name	Rev
C	N501VW	1.0

Date: Friday, December 18, 2015 Sheet 101 of 102

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

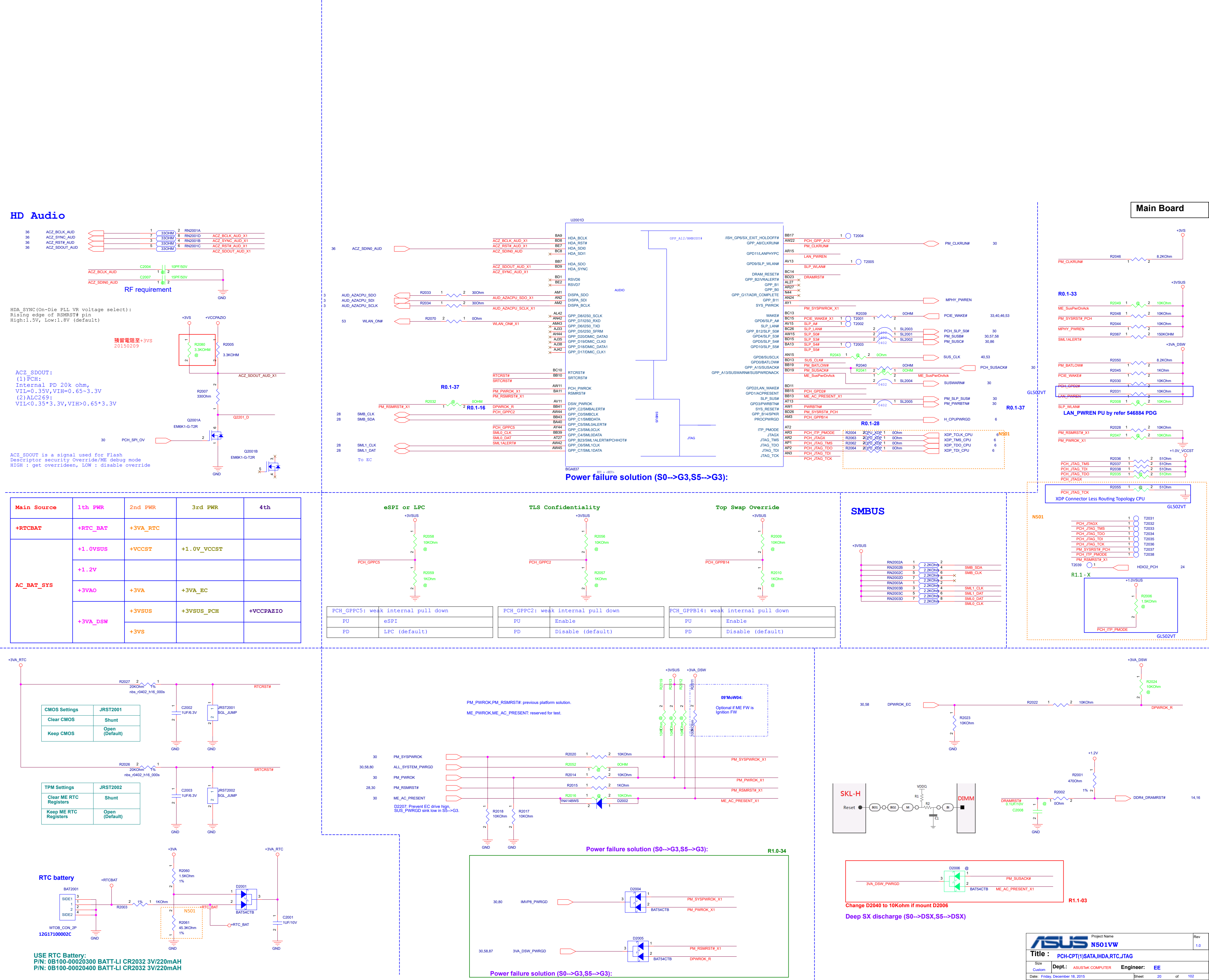
ASUSTeK COMPUTER INC.

Title : Revision History

Engineer: EE

Size: D | Project Name: N501VW | Rev: 1.0

Date: Friday, December 19, 2015 | Sheet 102 of 102



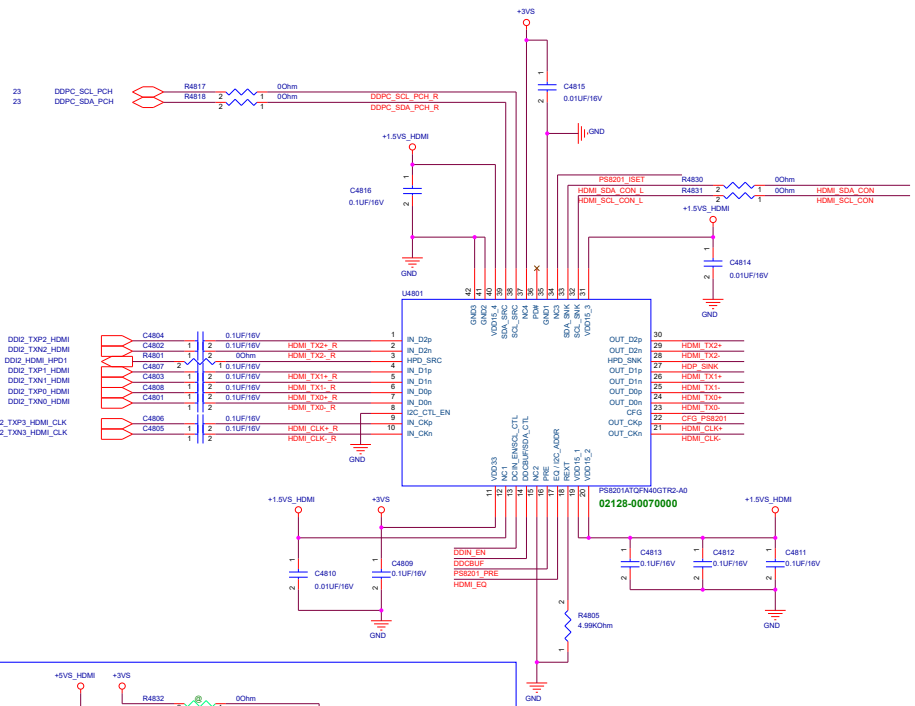
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST	
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+VCCPAZIO
		+3VS		

PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

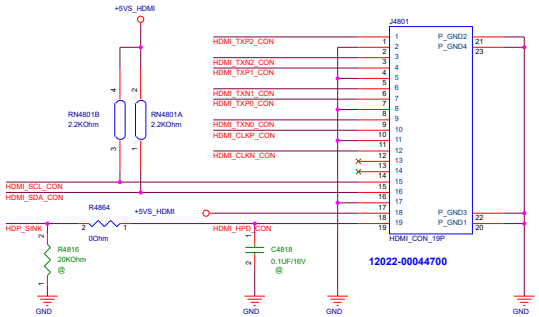
PCH_GPPC2: weak internal pull down	
PU	Enable
PD	Disable (default)

PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

HDMI Active-Level Shift



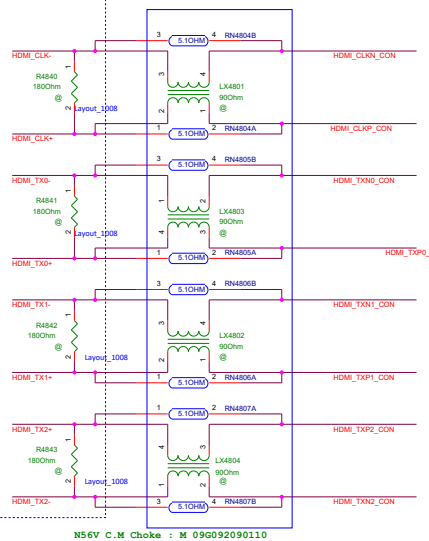
HDMI Conn.



2015.08.26 EMI Reserve

HDMI EMI

2015.12.15 EMI solution



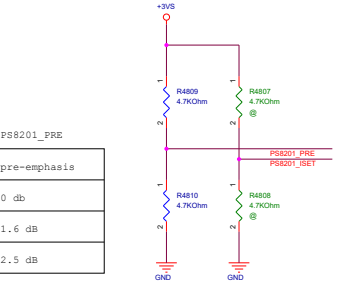
N56V C.M Choke : M 09G092090110

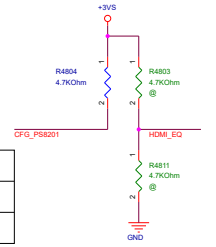
PS8201_PRE

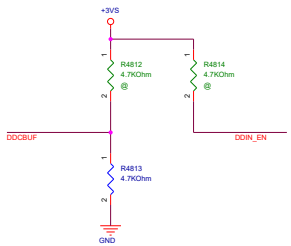
	pre-emphasis
L	0 db
M	1.6 dB
H	2.5 dB

	HDMI_EQ
L	6.5dB@3Gbps
M	3dB@3Gbps
H	9.5dB@3Gbps

	CFG_PS8201
L	HDMI ID disable
H	HDMI ID enable





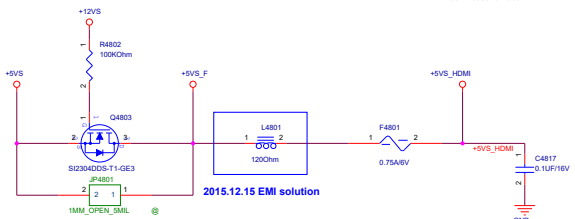


FIX can't read 4K2K HDMI Monitor EDID BUG

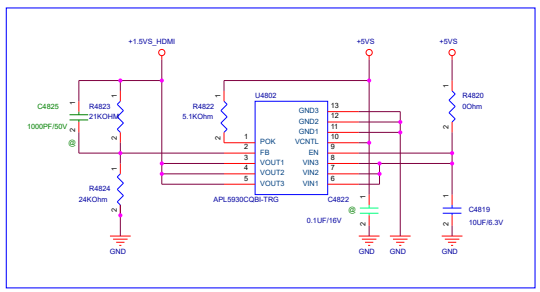
Reverse R4812, Mount R4813 Pull-down

HDMI PWR_+5VS_HDMI

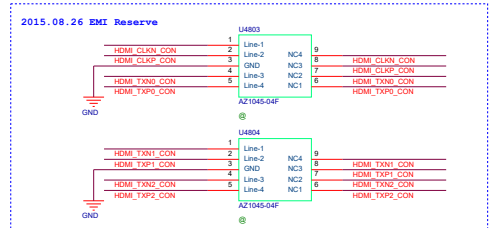
12/21/11
For HDMI Design IP R1.4
Del Q4801
Add Q4803 07G005047212
F4801=>07G014075310
L4802=>09G013120802



HDMI LDO 1.5VS

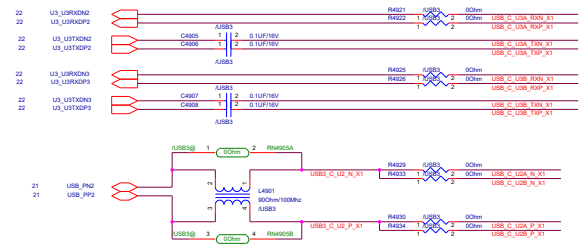


2015.08.26 EMI Reserve

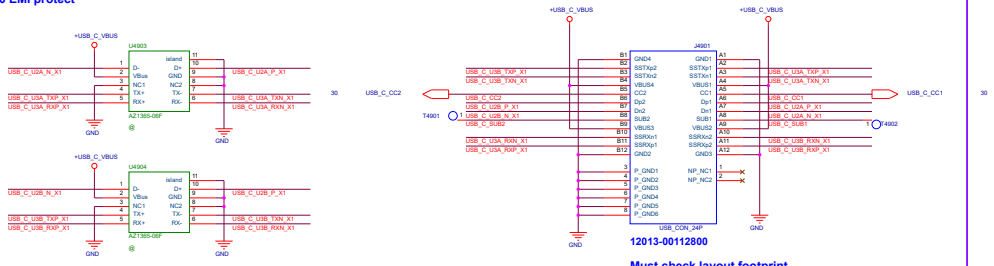


Project Name	GL502VT
Rev	1.0
Title :	HDMI Conn.
Size	C
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Marshall Li
Date:	Friday, December 18, 2015
Sheet	48 of 102

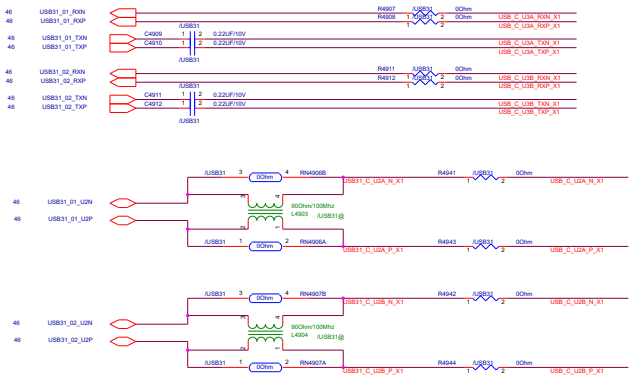
PCH USB3.0



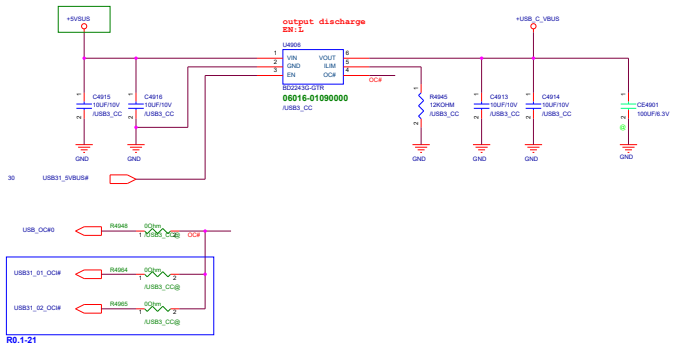
Type C Con. & USB3.0 EMI protect



ASM1142 USB3.1



Type-C CC logic IC PI5USB30216 & VBUS POWER_Switch



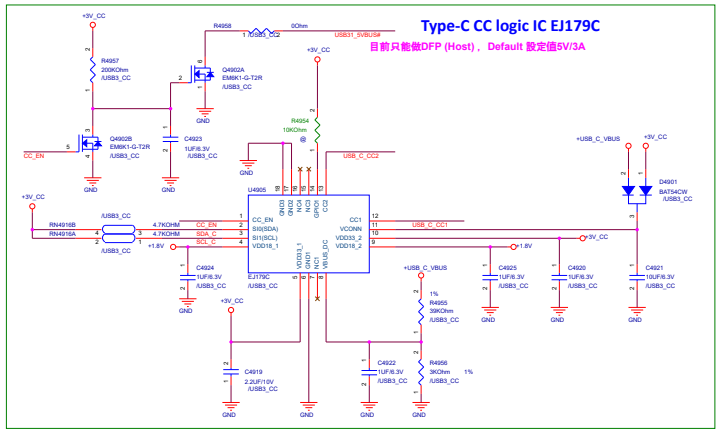
	Min	Typ	Max	R4945
Current Limit Threshold (mA)	112	212	313	100kohm
	911	1028	1145	20kohm
	1566	1696	1826	12kohm

R0.1-21

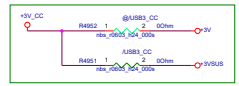
R1.0-38

Type-C CC logic IC EJ179C

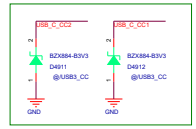
目前只能做DFP (Host)， Default 設定值5V/3A

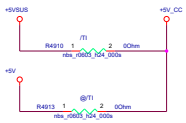


R1.0-30

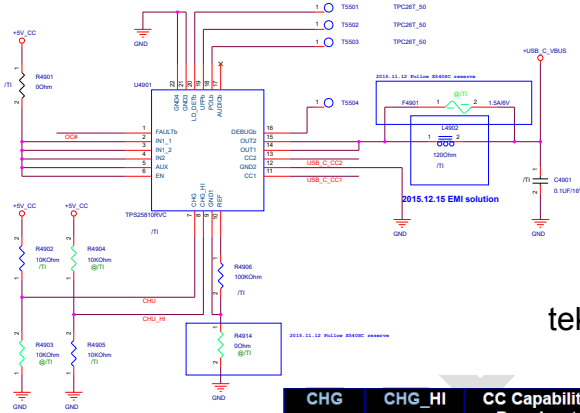


R1.0-16





Set CC
I limit = 3A



teknisi-indonesia

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

Project Name	GL752VW	Rev 1.0
Title :	USB 3.1 MB Type-C	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo
Date: Friday, December 18, 2015	Sheet 49 of 102	

<Variant Name>

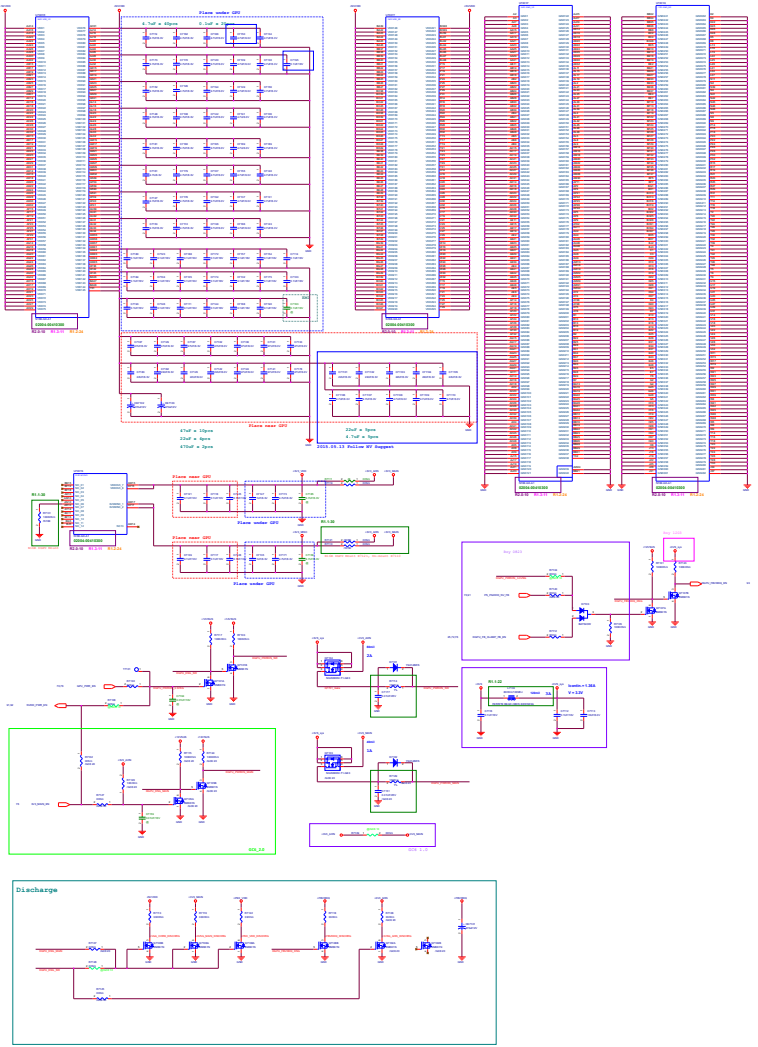
Title : I/O board(1-3)_USB

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
A	N501VW	1.0

Date:	Friday, December 18, 2015	Sheet	64	of	102



Title :	GPU_POWER		
Engineer :	Marshall Li		
Size :	Document Number :	Rev :	
B	0120210YT		
Date :	Sheet of		

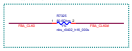
MF=0 Normal

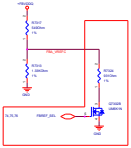
FBA Partition Memory (1 of 2)

GDDS MODE SELECTION

MODE	MF	EEC1	EDC1
x36	0	0	VDDQ
x32	0	VDDQ	VDDQ
x36 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

CK External Termination





R1.2-62 R1.2-25

USE GDDR3 VRAM 128Mb x 32 (512MB)

1st: P/N:03000-00031000 HYNIXH5GC4H24MFR-T2C (M-die) ,Strap: 0x2

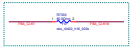
2nd: P/N:03000-00032000 SAMSUNGK4G41325FC-HC03 ,Strap: 0x3

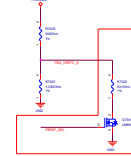
3nd: P/N:03000-00032400 MicronEDW4032BABG-60-F (B-die) ,Strap: 0x4

MF=1 Mirror

FBA Partition Memory (2 of 2)

CK External Termination





R1.2-62 R1.2-25

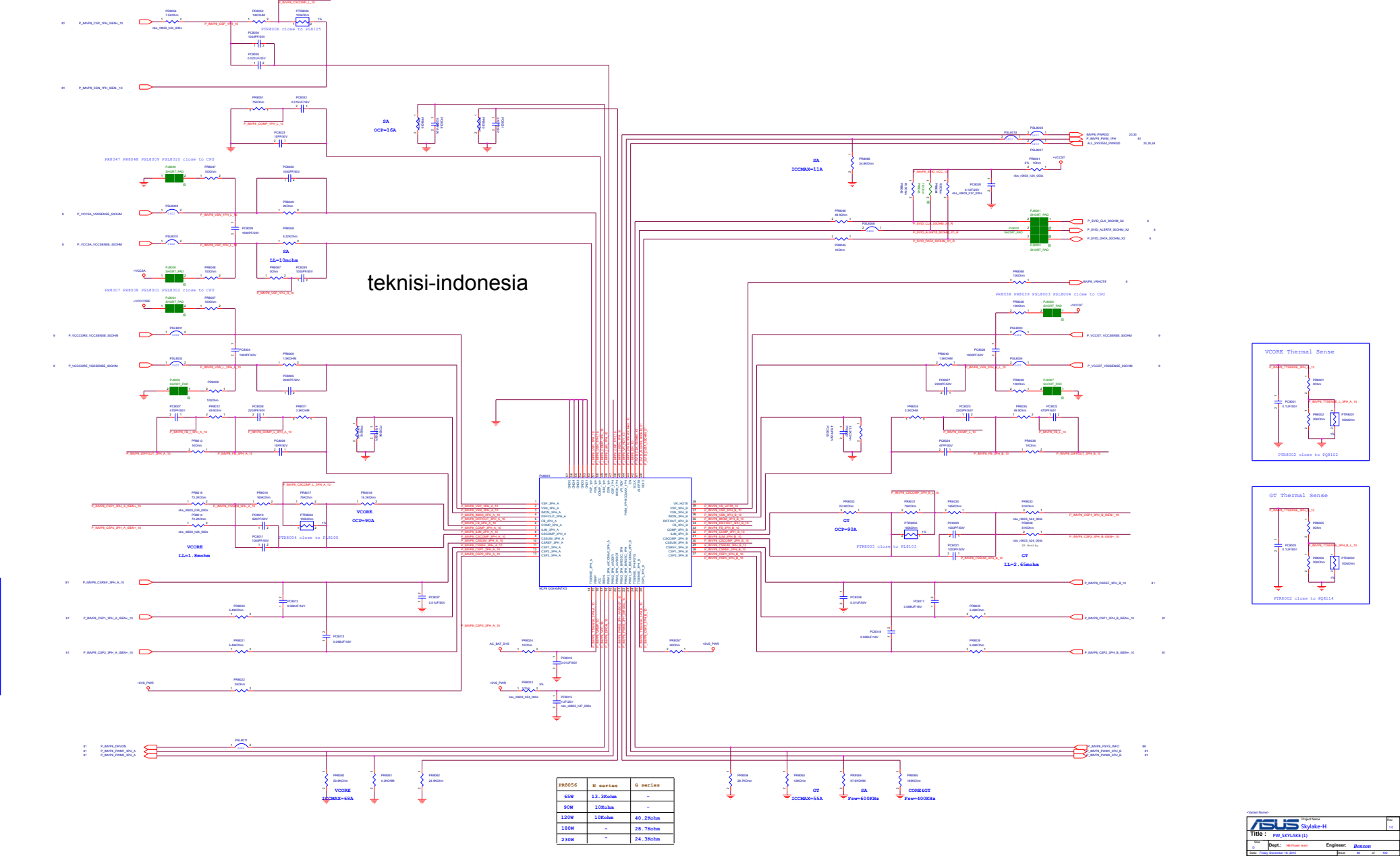
USE GDDR3 VRAM 128Mb x 32 (512MB)

1st: P/N:03000-00031000 HYNIXH5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03000-00032000 SAMSUNGK4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03000-00032400 MicronEDW4032BABG-60-F (B-die) ,Strap: 0x4

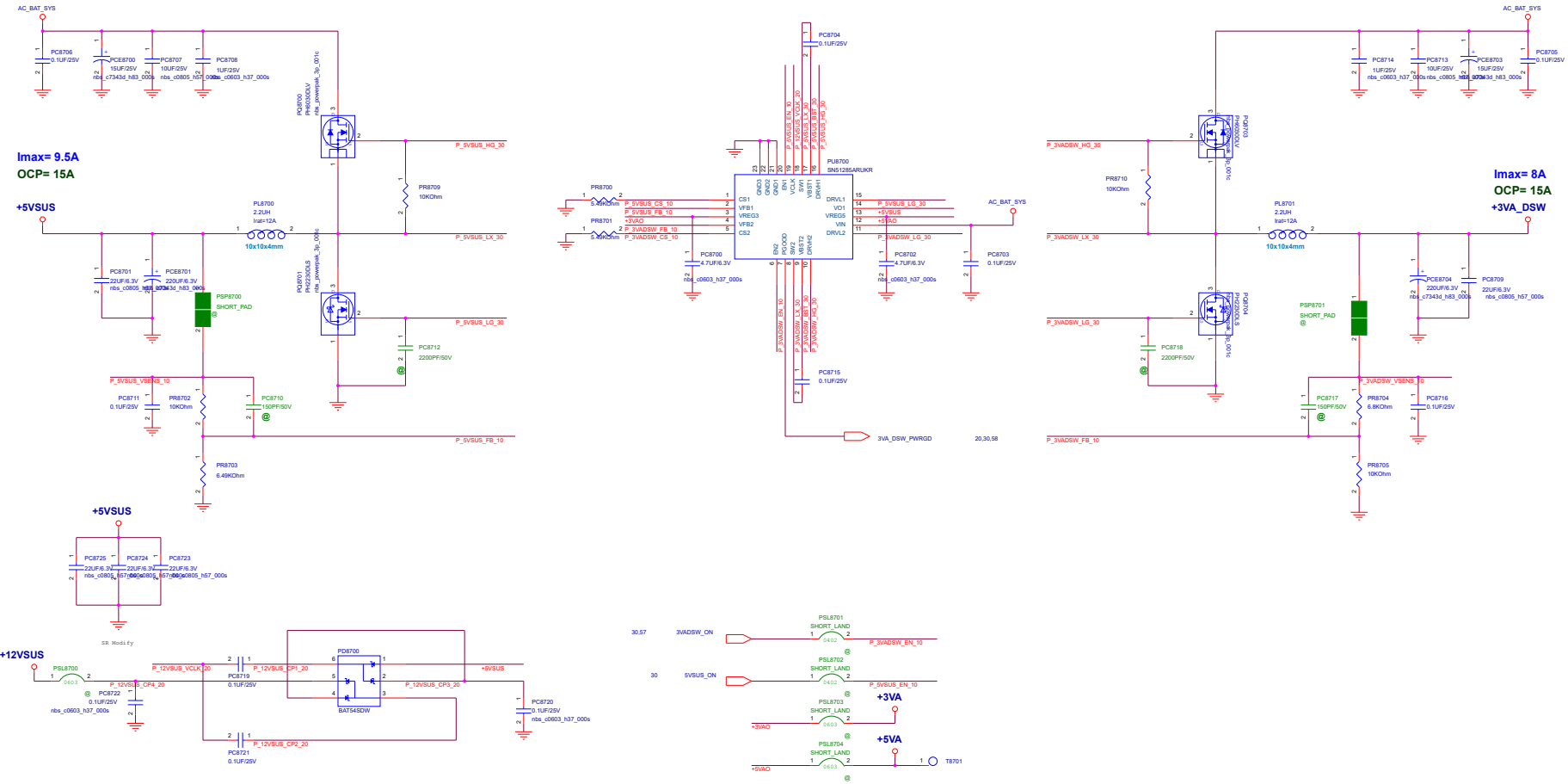
Title :	VRAM-CHANNEL A		
Engineer:	Marshall Li		
Size	Project name	Rev	
Custom	GL502VT		
Date: 2015/08/26 Tue	Sheet 1 of 1		



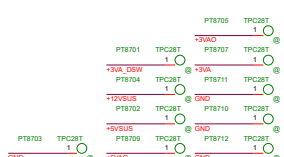
PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

ASUS	Project Name: Skylake-H	Rev: 1.0
Title :	PW_SKYLAKE (1)	
Size: D	Dept.: NB Power team	Engineer: Benson
Date: Friday, December 18, 2015	Sheet 80 of 102	

+3VA_DSW / +5VSUS [System Power]



請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



Adaptor Mode (IMVP8)

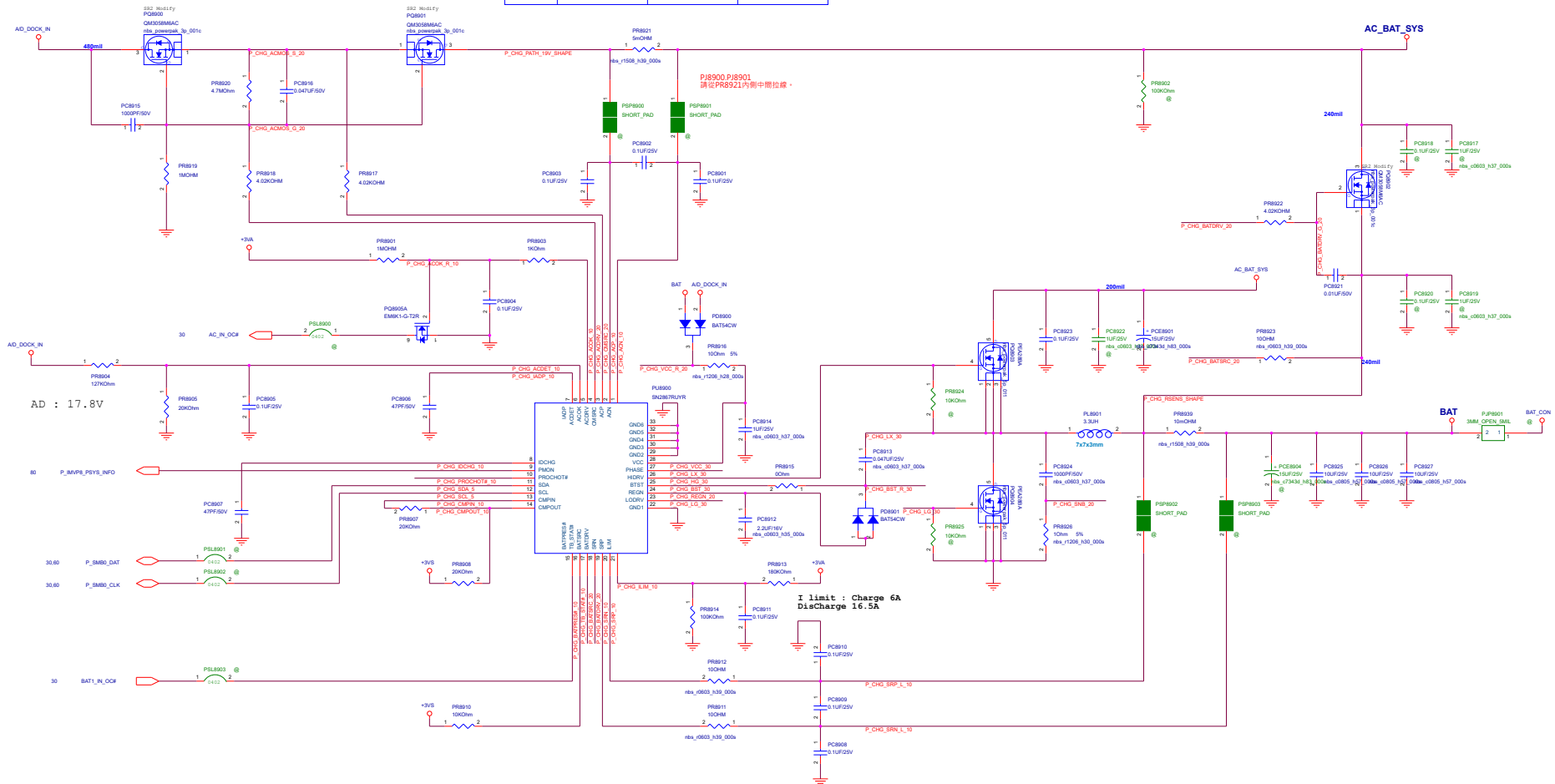
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

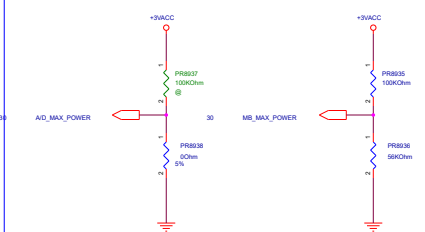
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

<Variant Name>
Project Name: Skylake-H
Rev: R1.0
Title : PW_+3VA_DSW/+5VSUS
Size: A2
Dept.: NB Power team
Engineer: Benson
Date: Friday, December 18, 2015
Sheet 87 of 102

PR8921	<=40W	<=120W	>=120W
	20m	10m	5m
	10125-0004m000	10G21DR01015111	10G21DM00515111



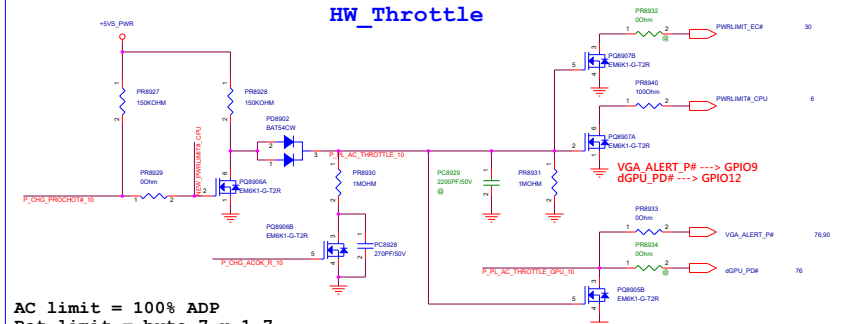
Adaptor select
total power = 90% ADP



Adaptor select

		N Series	G Series
PR8936	PR8921	10m	5m
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle



AC limit = 100% ADP
Bat limit = byte 7 x 1.7

ASUS	Project Name: Skylake-H		Rev: 1.0
Title : PW_CHARGER			
Size: A2	Dept.: NB Power Team	Engineer: Benson	
Date: Friday, December 18, 2015	Sheet 89 of 102		