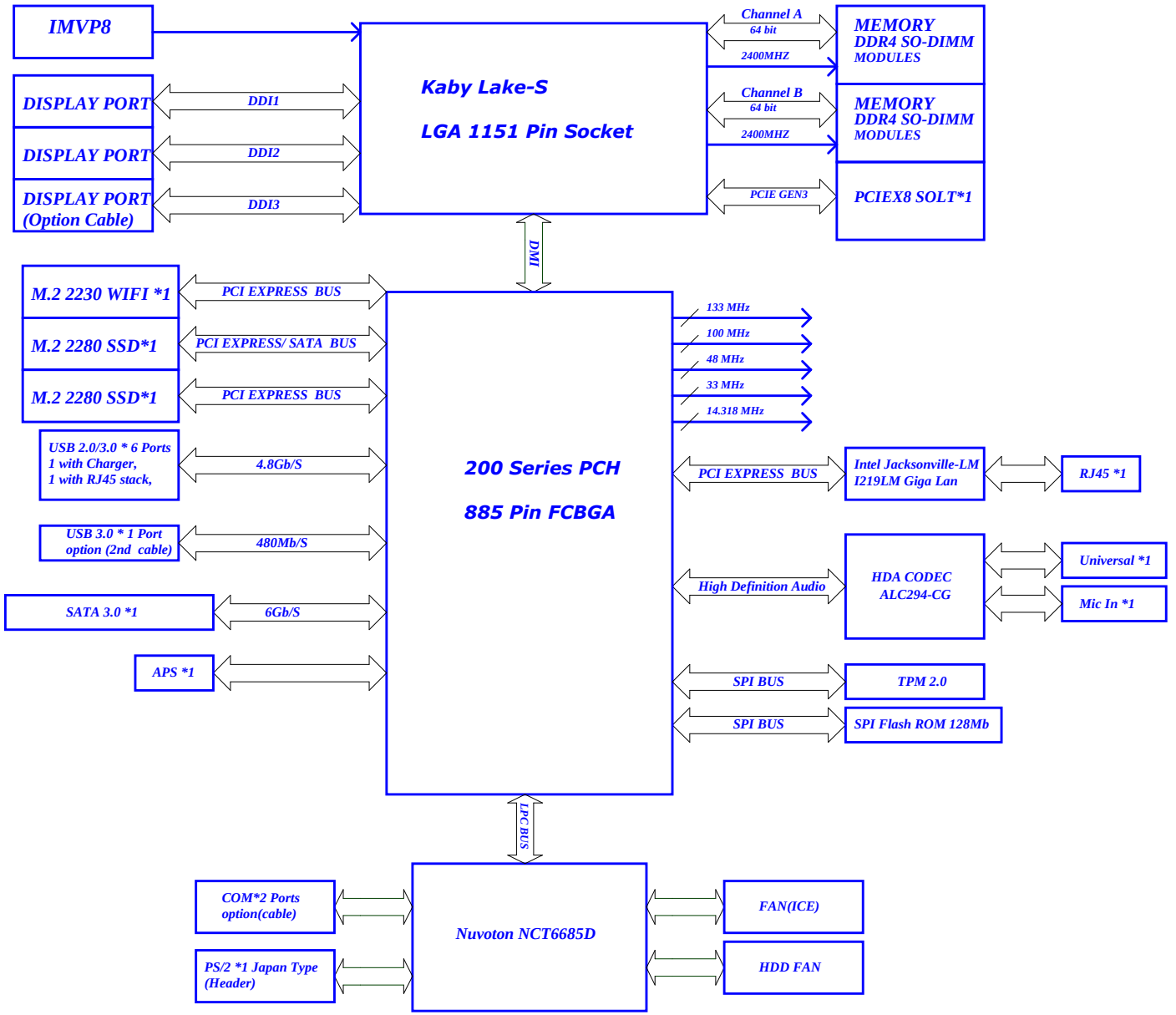
JC113/IQ270IH1

Q270 35W LI SVID/SSID: 17AA/310B
Q270 65W LI SVID/SSID: 17AA/310C
B250 35W LI SVID/SSID: 17AA/3111

X03 : 07/12/2016Y



LITE-ON TECHNOLOGY CORP.

Title: 01. Block Diagram

Size: C | Document Number: JC113 | Rev: X03

Date: Friday, August 26, 2016 | Sheet 1 of 67

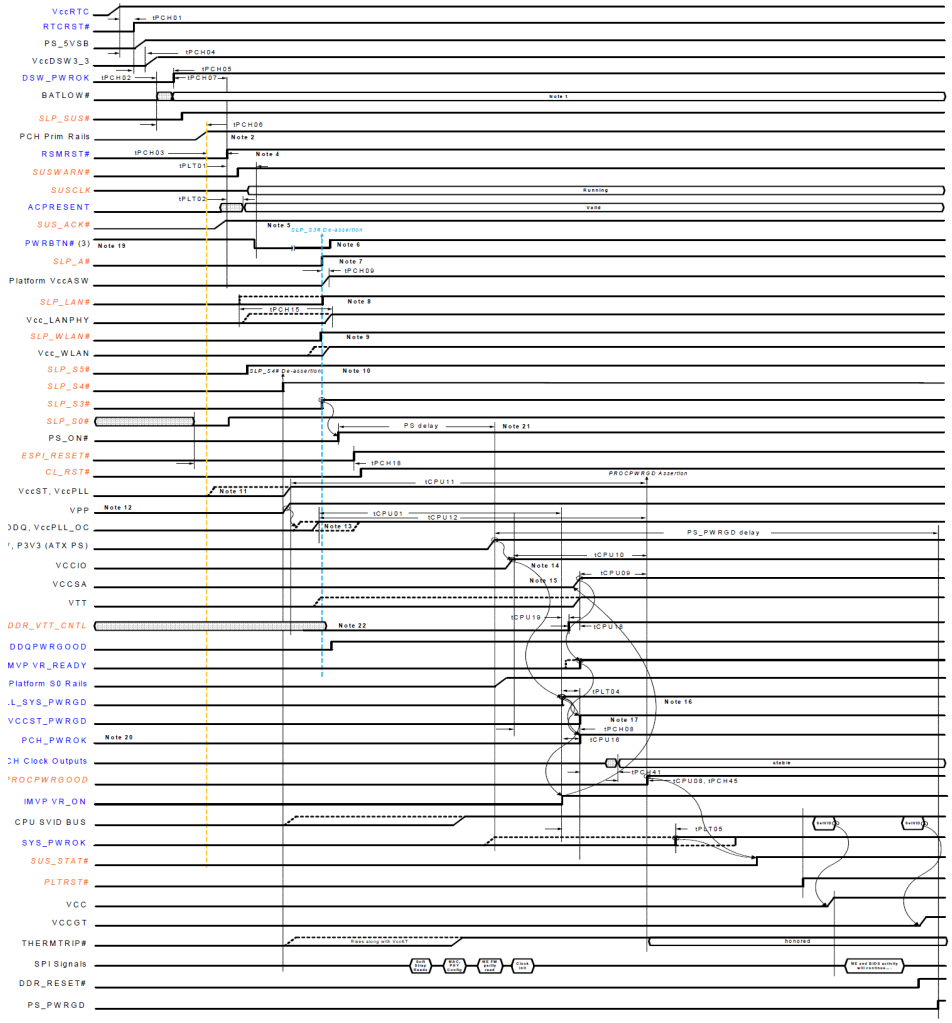


Figure 40-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

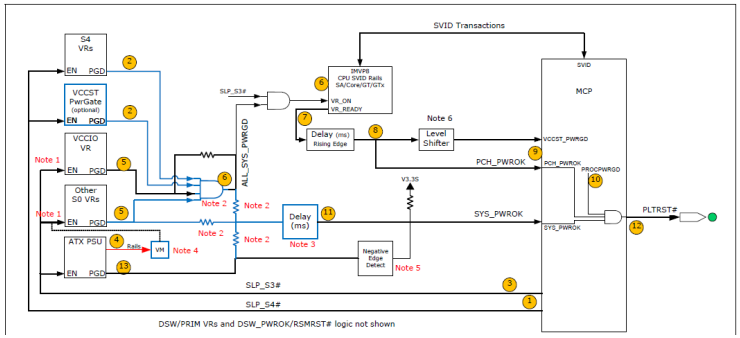


Figure 40-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation

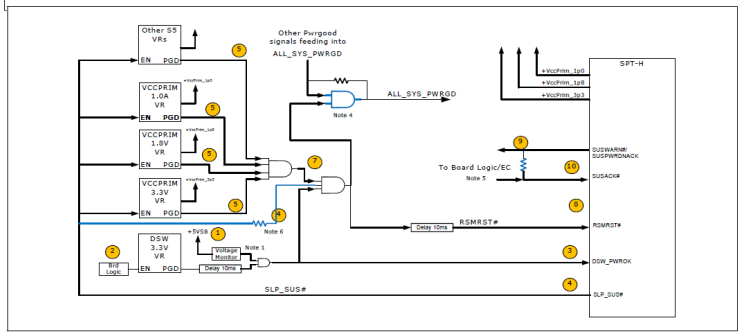


Table 40-3 System with M3 State Supported (Sheet 1 of 2)

Rails	S0/M0	S3/M3	S4/M3	S5/M3	Sx/M-Off	Deep S3	Deep S4/S5	G3[1]
RTC Well	ON	ON	ON	ON	ON	ON	ON	ON
PS_5VSB	ON	ON	ON	ON	ON	ON	ON	ON[14]
3.3V_DSW	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)[12]	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	ON	ON	ON	ON	ON	OFF	OFF	No Power
V3.3A	ON	ON	ON	ON	ON	OFF	OFF	No Power
V1.8A[13]	ON	ON	ON	ON	ON	OFF	OFF	No Power
V1.0A	ON	ON	ON	ON	ON	OFF	OFF	No Power
VCCOPC_1p8	ON	ON[15]	ON[15]	ON[15]	ON[15]	OFF	OFF	No Power
V3.3M[3]	ON	ON[11]	ON[11]	ON[11]	OFF	OFF	OFF	No Power
V1.8M[3]	ON	ON[11]	ON[11]	ON[11]	OFF	OFF	OFF	No Power
VDDQ	ON	ON	OFF	OFF	OFF	ON	OFF	No Power
V1.8U/V2.5U	ON	ON	OFF	OFF	OFF	ON	OFF	No Power
VCCST	ON	ON	OFF[5]	OFF[5]	OFF[5]	OFF	OFF	No Power
VCCPLL	ON	ON[7]	OFF[5]	OFF[5]	OFF[5]	OFF[5]	OFF	No Power
VCCPLL_OC	ON	ON[8]	OFF	OFF	OFF	OFF[8]	OFF	No Power
V3.3S	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V5.0S	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCC	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCGT/VCCGTx	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCIO	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCSA	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCOPC	ON/OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCEOPIO	ON/OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
P12V, P5V, P3V3	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power

LITE-ON TECHNOLOGY CORP.

Title: 02. Power Sequence

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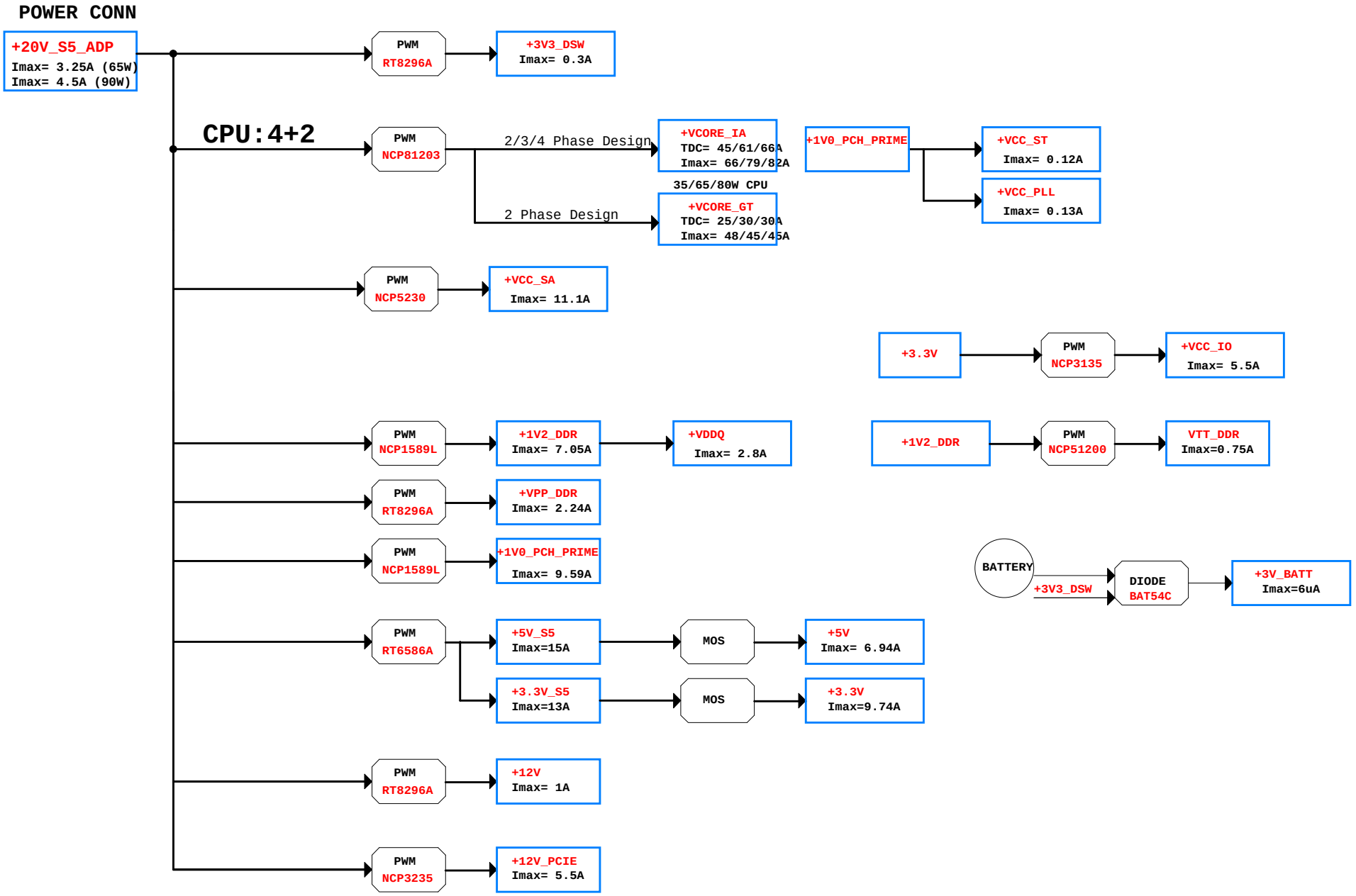

LITE-ON TECHNOLOGY CORP.

Title: 03. Power Delivery Map

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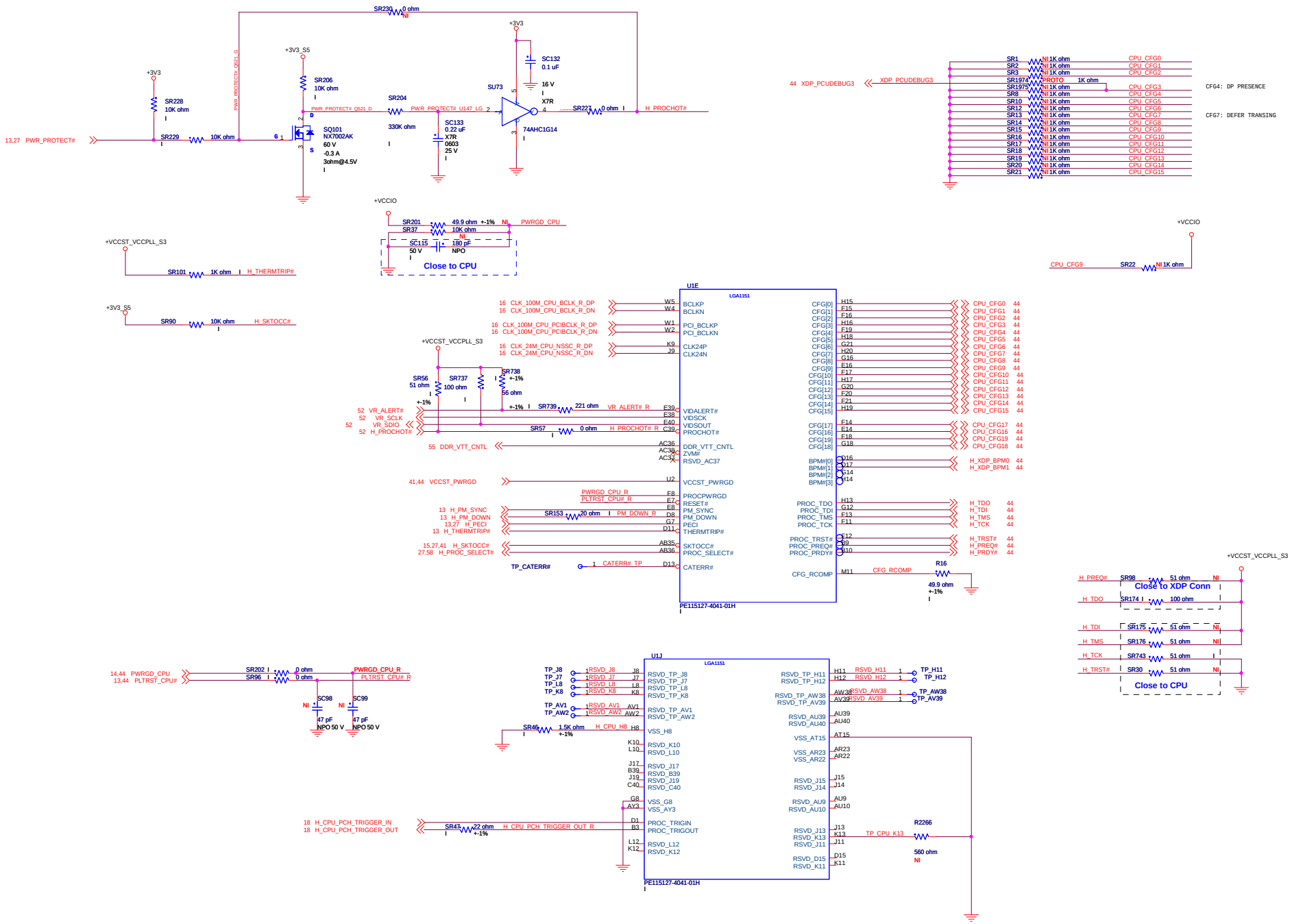
SR230 0 ohm NI
+3V3
+3V3_S5
SR206 10K ohm
SR228 10K ohm
SR229 10K ohm
13,27 PWR_PROTECT#
PWR_PROTECT# Q521_G
PWR_PROTECT# Q521_D
SQ101 NX7002AK 60 V -0.3 A 3ohm@4.5V
SR204 330K ohm
PWR_PROTECT# U147_LG
SC133 0.22 uF X7R 0603 25 V
SU73
74AHC1G14
SC132 0.1 uF 16 V X7R
SR227 0 ohm
H_PROCHOT#
44 XDP_PCUDEBUG3
SR1 NI 1K ohm CPU_CFG0
SR2 NI 1K ohm CPU_CFG1
SR3 NI 1K ohm CPU_CFG2
SR1974 PROTO 1K ohm CPU_CFG3
SR1975 NI 1K ohm CPU_CFG4
SR8 NI 1K ohm CPU_CFG5
SR10 NI 1K ohm CPU_CFG6
SR12 NI 1K ohm CPU_CFG7
SR13 NI 1K ohm CPU_CFG8
SR14 NI 1K ohm CPU_CFG9
SR15 NI 1K ohm CPU_CFG10
SR16 NI 1K ohm CPU_CFG11
SR17 NI 1K ohm CPU_CFG12
SR18 NI 1K ohm CPU_CFG13
SR19 NI 1K ohm CPU_CFG14
SR20 NI 1K ohm CPU_CFG15
SR21 NI 1K ohm
CFG4: DP PRESENCE
CFG7: DEFER TRANSING
+VCCIO
SR201 49.9 ohm +-1% NI PWRGD_CPU
SR37 10K ohm
SC115 180 pF 50 V NPO
Close to CPU
+VCCST_VCCPLL_S3
SR101 1K ohm H_THERMTRIP#
+VCCIO
CPU_CFG9 SR22 NI 1K ohm
+3V3_S5
SR90 10K ohm H_SKTOCC#
U1E
LGA1151
16 CLK_100M_CPU_BCLK_R_DP
16 CLK_100M_CPU_BCLK_R_DN
BCLKP
BCLKN
16 CLK_100M_CPU_PCIBCLK_R_DP
16 CLK_100M_CPU_PCIBCLK_R_DN
PCI_BCLKP
PCI_BCLKN
16 CLK_24M_CPU_NSSC_R_DP
16 CLK_24M_CPU_NSSC_R_DN
CLK24P
CLK24N
+VCCST_VCCPLL_S3
SR56 51 ohm +-1%
SR737 100 ohm +-1%
SR738 56 ohm +-1%
SR739 221 ohm
52 VR_ALERT#
52 VR_SCLK
52 VR_SDIO
52 H_PROCHOT#
VR_ALERT# R
VIDALERT#
VIDSCK
VIDSOUT
PROCHOT#
SR57 0 ohm H_PROCHOT# R
55 DDR_VTT_CNTL
DDR_VTT_CNTL
ZVM#
RSVD_AC37
41,44 VCCST_PWRGD
VCCST_PWRGD
PWRGD_CPU_R
PLTRST_CPU# R
PROCPWRGD
RESET#
13 H_PM_SYNC
13 H_PM_DOWN
13,27 H_PECI
13 H_THERMTRIP#
SR153 20 ohm
PM_DOWN_R
PM_SYNC
PM_DOWN
PECI
THERMTRIP#
15,27,41 H_SKTOCC#
27,58 H_PROC_SELECT#
SKTOCC#
PROC_SELECT#
TP_CATERR#
CATERR# TP
CATERR#
CFG[0] CFG[1] CFG[2] CFG[3] CFG[4] CFG[5] CFG[6] CFG[7] CFG[8] CFG[9] CFG[10] CFG[11] CFG[12] CFG[13] CFG[14] CFG[15]
CPU_CFG0 CPU_CFG1 CPU_CFG2 CPU_CFG3 CPU_CFG4 CPU_CFG5 CPU_CFG6 CPU_CFG7 CPU_CFG8 CPU_CFG9 CPU_CFG10 CPU_CFG11 CPU_CFG12 CPU_CFG13 CPU_CFG14 CPU_CFG15
CFG[17] CFG[16] CFG[19] CFG[18]
CPU_CFG17 CPU_CFG16 CPU_CFG19 CPU_CFG18
BPM#[0] BPM#[1] BPM#[2] BPM#[3]
H_XDP_BPM0 H_XDP_BPM1
PROC_TDO PROC_TDI PROC_TMS PROC_TCK
H_TDO H_TDI H_TMS H_TCK
PROC_TRST# PROC_PREQ# PROC_PRDY#
H_TRST# H_PREQ# H_PRDY#
CFG_RCOMP
R16 49.9 ohm +-1%
PE115127-4041-01H
+VCCST_VCCPLL_S3
H_PREQ# SR98 51 ohm NI
Close to XDP Conn
H_TDO SR174 100 ohm
H_TDI SR175 51 ohm NI
H_TMS SR176 51 ohm NI
H_TCK SR743 51 ohm
H_TRST# SR30 51 ohm NI
Close to CPU
14,44 PWRGD_CPU
13,44 PLTRST_CPU#
SR202 0 ohm
SR96 0 ohm
PWRGD_CPU_R
PLTRST_CPU# R
SC98 NI 47 pF NPO 50 V
SC99 NI 47 pF NPO 50 V
U1J
LGA1151
TP_J8 TP_J7 TP_L8 TP_K8
RSVD_J8 RSVD_J7 RSVD_L8 RSVD_K8
TP_AV1 TP_AW2
RSVD_AV1 RSVD_AW2
SR46 1.5K ohm +-1%
H_CPU_H8
RSVD_TP_J8 RSVD_TP_J7 RSVD_TP_L8 RSVD_TP_K8
RSVD_TP_AV1 RSVD_TP_AW2
VSS_H8
RSVD_K10 RSVD_L10
RSVD_J17 RSVD_B39 RSVD_J19 RSVD_C40
VSS_G8 VSS_AY3
18 H_CPU_PCH_TRIGGER_IN
18 H_CPU_PCH_TRIGGER_OUT
SR47 22 ohm +-1%
H_CPU_PCH_TRIGGER_OUT_R
PROC_TRIGIN PROC_TRIGOUT
RSVD_L12 RSVD_K12
RSVD_TP_H11 RSVD_TP_H12
RSVD_TP_AW38 RSVD_TP_AV39
RSVD_AU39 RSVD_AU40
VSS_AT15
VSS_AR23 VSS_AR22
RSVD_J15 RSVD_J14
RSVD_AU9 RSVD_AU10
RSVD_J13 RSVD_K13 RSVD_J11
RSVD_D15 RSVD_K11
TP_CPU_K13
R2266 560 ohm NI
PE115127-4041-01H
LITE-ON TECHNOLOGY CORP.
Title
04. CPU-1: MSIC
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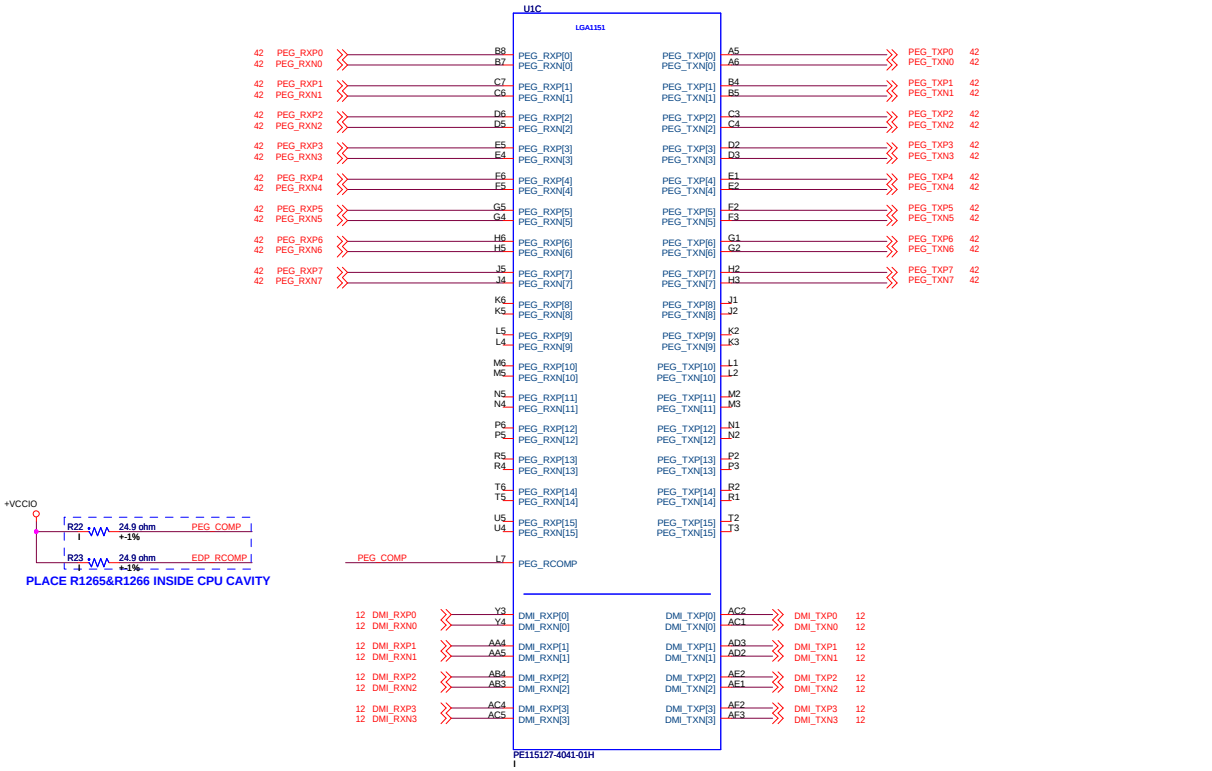
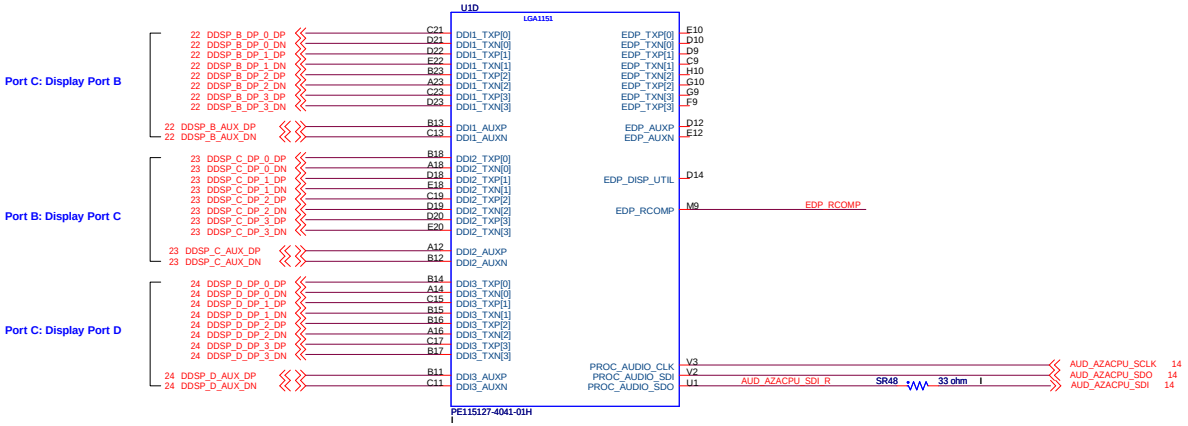
GFX SIGNAL





LITE-ON TECHNOLOGY CORP.		
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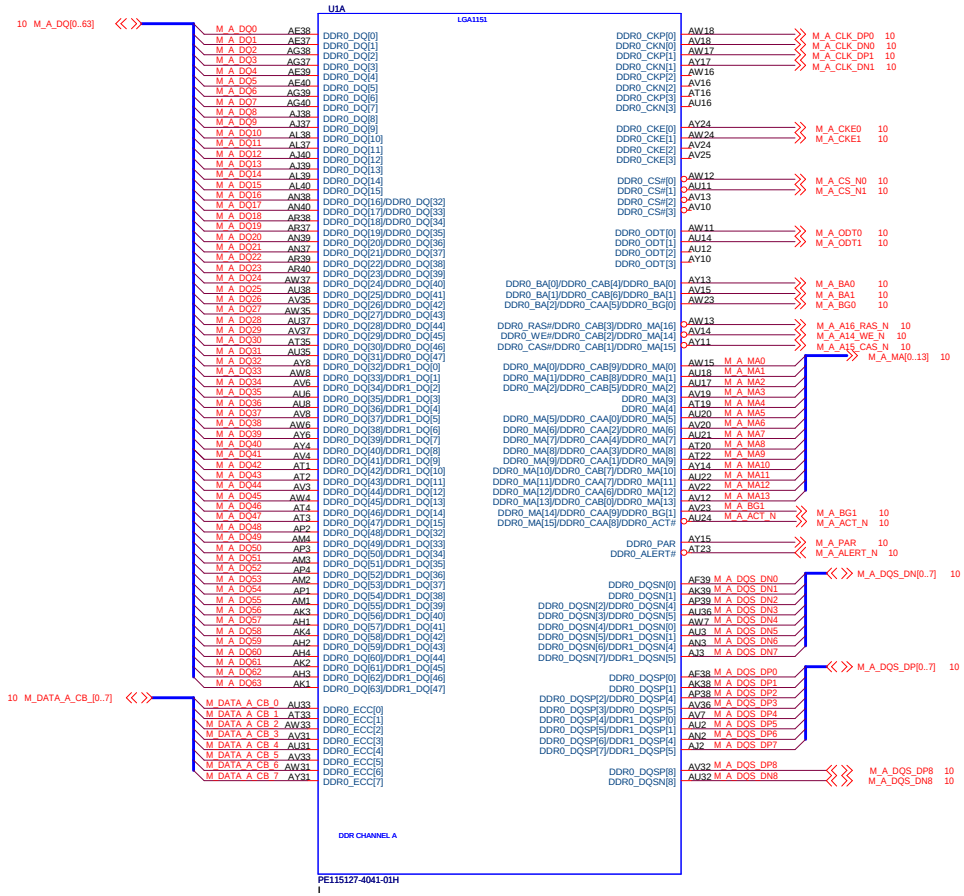
Size C	Document Number JC113	Rev X03
Date: Friday, August 26, 2016	Sheet 5 of 67	



LITE-ON TECHNOLOGY CORP.		
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Size: C	Document Number: JC113	Rev: X03
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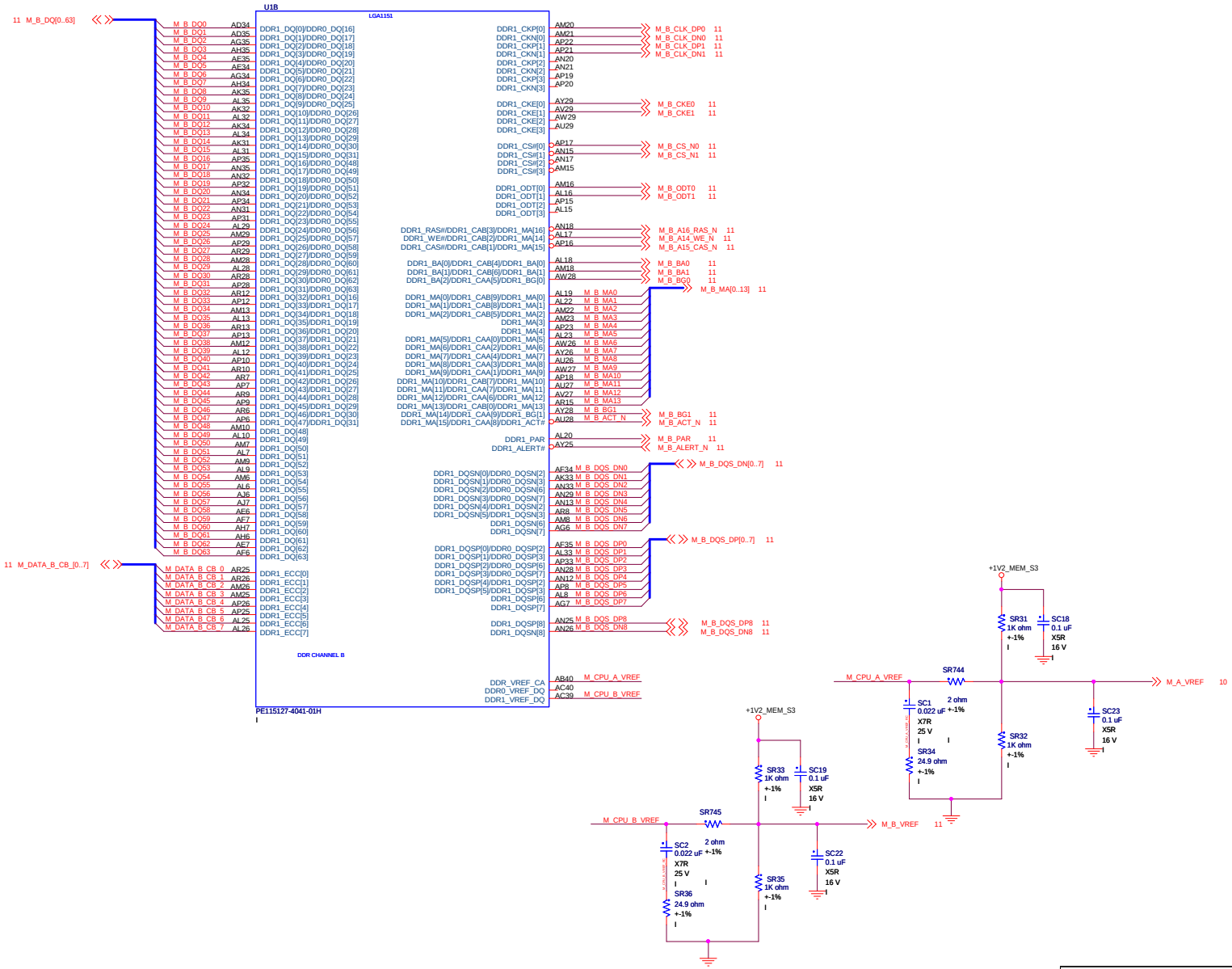

LITE-ON TECHNOLOGY CORP.		
Title	07. CPU-4: DDR4_CHB	
Size C	Document Number JC113	Rev X03
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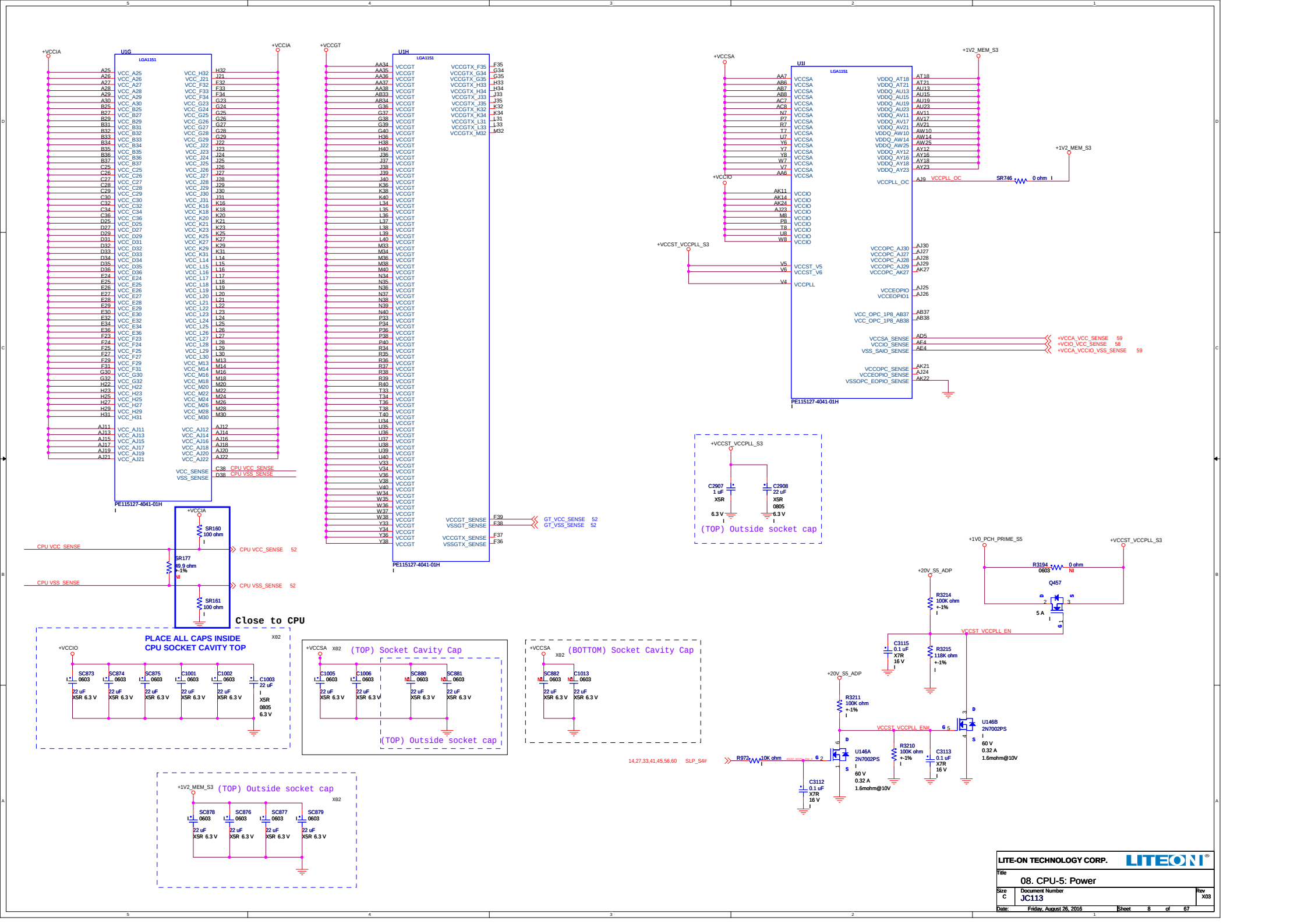
U1G
LGA1151
PE115127-4041-01H
+VCCIA
VCC_A25 VCC_A26 VCC_A27 VCC_A28 VCC_A29 VCC_A30 VCC_B25 VCC_B27 VCC_B29 VCC_B31 VCC_B32 VCC_B33 VCC_B34 VCC_B35 VCC_B36 VCC_B37 VCC_C25 VCC_C26 VCC_C27 VCC_C28 VCC_C29 VCC_C30 VCC_C32 VCC_C34 VCC_C36 VCC_D25 VCC_D27 VCC_D29 VCC_D31 VCC_D32 VCC_D33 VCC_D34 VCC_D35 VCC_D36 VCC_E24 VCC_E25 VCC_E26 VCC_E27 VCC_E28 VCC_E29 VCC_E30 VCC_E32 VCC_E34 VCC_E36 VCC_F23 VCC_F24 VCC_F25 VCC_F27 VCC_F29 VCC_F31 VCC_G30 VCC_G32 VCC_H22 VCC_H23 VCC_H25 VCC_H27 VCC_H29 VCC_H31
VCC_AJ11 VCC_AJ13 VCC_AJ15 VCC_AJ17 VCC_AJ19 VCC_AJ21
VCC_H32 VCC_J21 VCC_F32 VCC_F33 VCC_F34 VCC_G23 VCC_G24 VCC_G25 VCC_G26 VCC_G27 VCC_G28 VCC_G29 VCC_J22 VCC_J23 VCC_J24 VCC_J25 VCC_J26 VCC_J27 VCC_J28 VCC_J29 VCC_J30 VCC_J31 VCC_K16 VCC_K18 VCC_K20 VCC_K21 VCC_K23 VCC_K25 VCC_K27 VCC_K29 VCC_K31 VCC_L14 VCC_L15 VCC_L16 VCC_L17 VCC_L18 VCC_L19 VCC_L20 VCC_L21 VCC_L22 VCC_L23 VCC_L24 VCC_L25 VCC_L26 VCC_L27 VCC_L28 VCC_L29 VCC_L30 VCC_M13 VCC_M14 VCC_M16 VCC_M18 VCC_M20 VCC_M22 VCC_M24 VCC_M26 VCC_M28 VCC_M30
VCC_AJ12 VCC_AJ14 VCC_AJ16 VCC_AJ18 VCC_AJ20 VCC_AJ22
VCC_SENSE C38 CPU VCC_SENSE
VSS_SENSE D38 CPU VSS_SENSE
+VCCIA
SR160 100 ohm
CPU VCC_SENSE
SR177 49.9 ohm +-1% NI
CPU VSS_SENSE
SR161 100 ohm
CPU VCC_SENSE 52
CPU VSS_SENSE 52
Close to CPU
PLACE ALL CAPS INSIDE
CPU SOCKET CAVITY TOP
X82
+VCCIO
SC873 SC874 SC875 C1001 C1002 C1003
0603
22 uF X5R 6.3 V
C1003 22 uF I X5R 0805 6.3 V
U1H
LGA1151
PE115127-4041-01H
+VCCGT
VCCGT
VCCGTX_F35 VCCGTX_G34 VCCGTX_G35 VCCGTX_H33 VCCGTX_H34 VCCGTX_J33 VCCGTX_J35 VCCGTX_K32 VCCGTX_K34 VCCGTX_L31 VCCGTX_L33 VCCGTX_M32
VCCGT_SENSE F39
VSSGT_SENSE F38
VCCGTX_SENSE F37
VSSGTX_SENSE F36
GT_VCC_SENSE 52
GT_VSS_SENSE 52
+VCCSA
(TOP) Socket Cavity Cap
C1005 C1006 SC880 SC881
0603
22 uF X5R 6.3 V
(TOP) Outside socket cap
(BOTTOM) Socket Cavity Cap
SC882 C1013
U1I
LGA1151
PE115127-4041-01H
VCCSA
VDDQ_AT18 VDDQ_AT21 VDDQ_AU13 VDDQ_AU15 VDDQ_AU19 VDDQ_AU23 VDDQ_AV11 VDDQ_AV17 VDDQ_AV21 VDDQ_AW10 VDDQ_AW14 VDDQ_AW25 VDDQ_AY12 VDDQ_AY16 VDDQ_AY18 VDDQ_AY23
+1V2_MEM_S3
VCCPLL_OC
SR746 0 ohm I
+VCCIO
VCCIO
+VCCST_VCCPLL_S3
VCCST_V5 VCCST_V6
VCCPLL
VCCOPC_AJ30 VCCOPC_AJ27 VCCOPC_AJ28 VCCOPC_AJ29 VCCOPC_AK27
VCCEOPIO VCCEOPIO1
VCC_OPC_1P8_AB37 VCC_OPC_1P8_AB38
VCCSA_SENSE VCCIO_SENSE VSS_SAIO_SENSE
+VCCA_VCC_SENSE 59
+VCCIO_VCC_SENSE 58
+VCCA_VCCIO_VSS_SENSE 59
VCCOPC_SENSE VCCEOPIO_SENSE VSSOPC_EOPIO_SENSE
+VCCST_VCCPLL_S3
C2907 1 uF X5R 6.3 V
C2908 22 uF X5R 0805 6.3 V
(TOP) Outside socket cap
+1V0_PCH_PRIME_S5
+VCCST_VCCPLL_S3
R3194 0 ohm 0603 NI
Q457
5 A
+20V_S5_ADP
R3214 100K ohm +-1%
VCCST_VCCPLL_EN
C3115 0.1 uF X7R 16 V
R3215 118K ohm +-1%
R3211 100K ohm +-1%
VCCST_VCCPLL_EN#
U146A 2N7002PS
U146B 2N7002PS
60 V 0.32 A 1.6mohm@10V
R3210 100K ohm +-1%
C3113 0.1 uF X7R 16 V
R972 10K ohm
14,27,33,41,45,56,60 SLP_S4#
C3112 0.1 uF X7R 16 V
+1V2_MEM_S3 (TOP) Outside socket cap
SC878 SC876 SC877 SC879
0603
22 uF X5R 6.3 V
LITE-ON TECHNOLOGY CORP.
Title
08. CPU-5: Power
Size C
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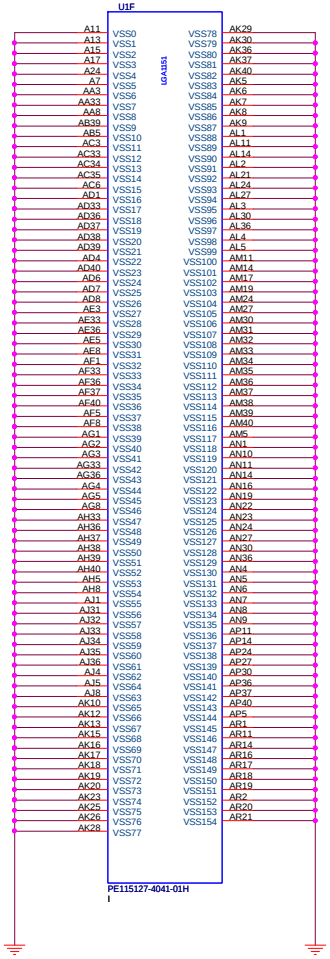

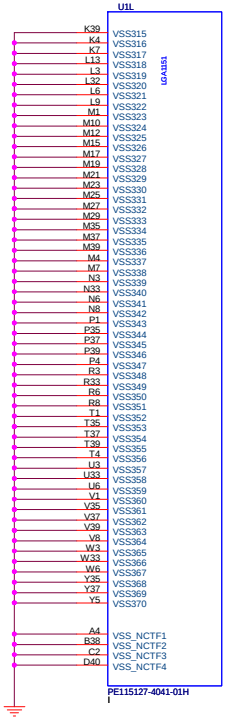

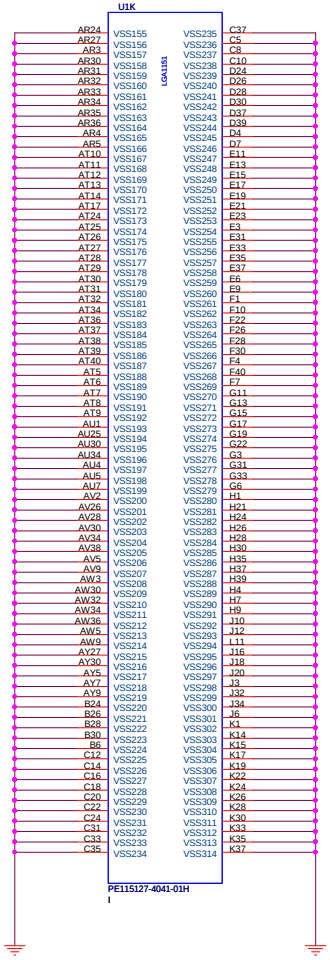

LITE-ON TECHNOLOGY CORP.			
Title: 09. CPU-6: GND			
Size: C	Document Number: JC113		Rev: X03
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PLACE THE CAP WITHIN 200 MILS FROM THE DIMM0

PLACE ALL COMPONENTS ON THIS PAGE CLOSE TO SODIMM

LITE-ON TECHNOLOGY CORP.	
Title	10. DDR4 CHA SO-DIMM1
Size C	Document Number JC113
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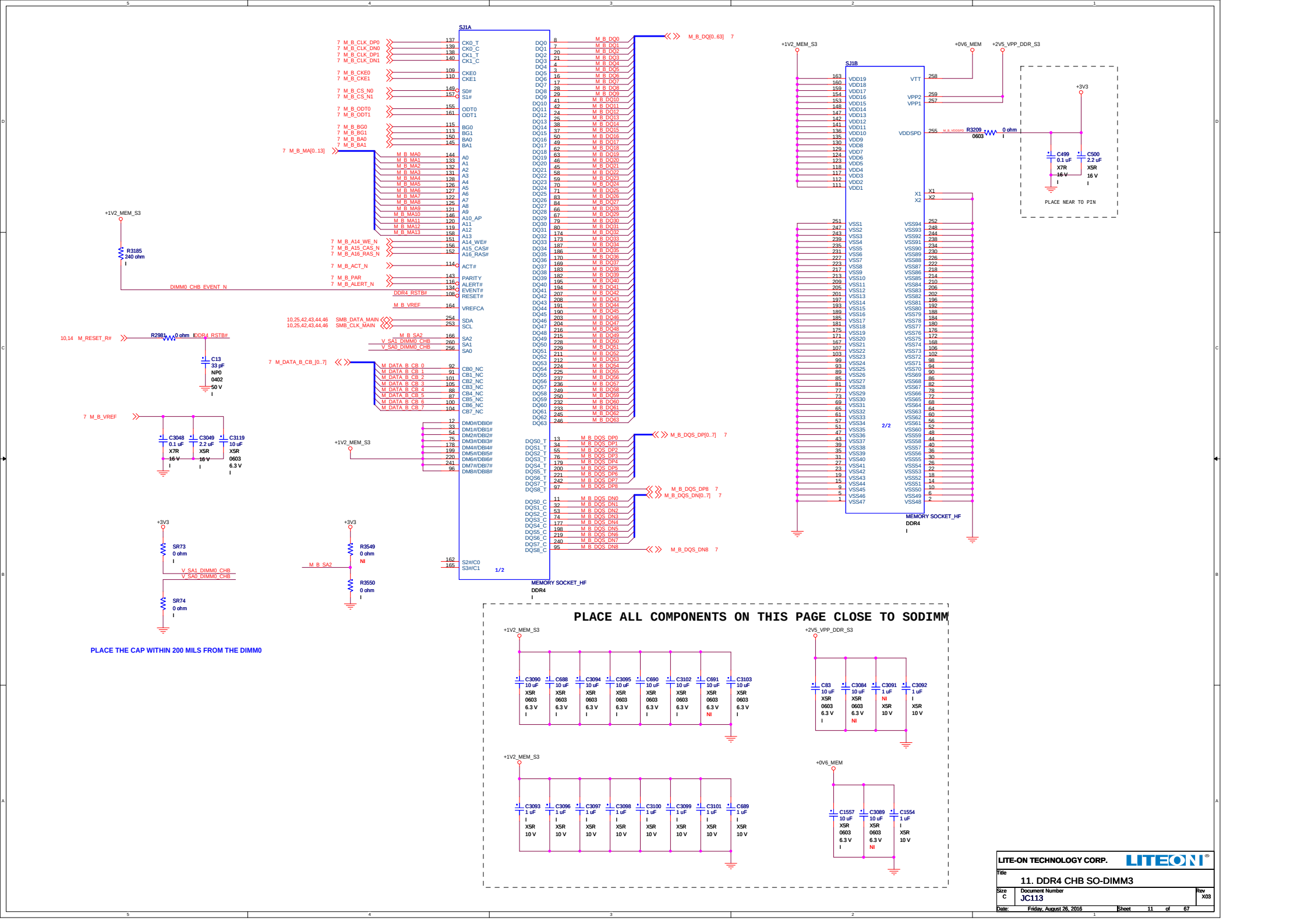
Date: Friday, August 26, 2016	Sheet 10 of 67


SJ1A
SJ1B
MEMORY SOCKET_HF
DDR4
1/2
2/2
+1V2_MEM_S3
+0V6_MEM
+2V5_VPP_DDR_S3
+3V3
R3185 240 ohm
R2981 0 ohm
C13 33 pF NP0 0402 50 V
R3209 0 ohm 0603
C499 0.1 uF X7R 16 V
C500 2.2 uF X5R 16 V
PLACE NEAR TO PIN
C3048 0.1 uF X7R 16 V
C3049 2.2 uF X5R 16 V
C3119 10 uF X5R 0603 6.3 V
SR73 0 ohm
SR74 0 ohm
R3549 0 ohm NI
R3550 0 ohm
PLACE THE CAP WITHIN 200 MILS FROM THE DIMM0
PLACE ALL COMPONENTS ON THIS PAGE CLOSE TO SODIMM
C3090 10 uF X5R 0603 6.3 V
C688 10 uF X5R 0603 6.3 V
C3094 10 uF X5R 0603 6.3 V
C3095 10 uF X5R 0603 6.3 V
C690 10 uF X5R 0603 6.3 V
C3102 10 uF X5R 0603 6.3 V
C691 10 uF X5R 0603 6.3 V NI
C3103 10 uF X5R 0603 6.3 V
C83 10 uF X5R 0603 6.3 V
C3084 10 uF X5R 0603 6.3 V NI
C3091 1 uF NI X5R 10 V
C3092 1 uF X5R 10 V
C3093 1 uF X5R 10 V
C3096 1 uF X5R 10 V
C3097 1 uF X5R 10 V
C3098 1 uF X5R 10 V
C3100 1 uF X5R 10 V
C3099 1 uF X5R 10 V
C3101 1 uF X5R 10 V
C689 1 uF X5R 10 V
C1557 10 uF X5R 0603 6.3 V
C3089 10 uF X5R 0603 6.3 V NI
C1554 1 uF X5R 10 V
LITE-ON TECHNOLOGY CORP.
11. DDR4 CHB SO-DIMM3
Size C
Document Number JC113
Rev X03
Date: Friday, August 26, 2016
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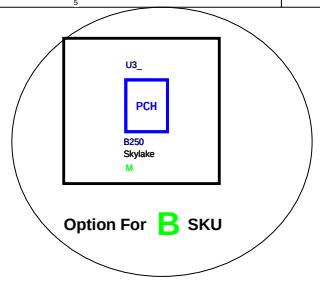


U3B

DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0 DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1 DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2 DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3

PCIE_RCOMPN PCIE_RCOMPP

R41 +-1% 100 ohm

PCIE1_RXN/USB3_7_RXN PCIE1_RXP/USB3_7_RXP PCIE1_TXN/USB3_7_TXN PCIE1_TXP/USB3_7_TXP PCIE2_TXN/USB3_8_TXN PCIE2_TXP/USB3_8_TXP PCIE2_RXN/USB3_8_RXN PCIE2_RXP/USB3_8_RXP PCIE3_RXN/USB3_9_RXN PCIE3_RXP/USB3_9_RXP PCIE3_TXN/USB3_9_TXN PCIE3_TXP/USB3_9_TXP PCIE4_RXN/USB3_10_RXN PCIE4_RXP/USB3_10_RXP PCIE4_TXN/USB3_10_TXN PCIE4_TXP/USB3_10_TXP PCIE5_RXN PCIE5_RXP PCIE5_TXN PCIE5_TXP PCIE6_RXN PCIE6_RXP PCIE6_TXN PCIE6_TXP PCIE7_RXN PCIE7_RXP PCIE7_TXN PCIE7_TXP PCIE8_RXN PCIE8_RXP PCIE8_TXN PCIE8_TXP

USB2N_1 USB2P_1 USB2N_2 USB2P_2 USB2N_3 USB2P_3 USB2N_4 USB2P_4 USB2N_5 USB2P_5 USB2N_6 USB2P_6 USB2N_7 USB2P_7 USB2N_8 USB2P_8 USB2N_9 USB2P_9 USB2N_10 USB2P_10 USB2N_11 USB2P_11 USB2N_12 USB2P_12 USB2N_13 USB2P_13 USB2N_14 USB2P_14

USBP1- USBP1+ — Int USB HDR
USBP3- USBP3+ — M.2 2230 USB 2.0 X 1
USBP5- USBP5+ USBP6- USBP6+ USBP7- USBP7+ USBP8- USBP8+ — Rear USB
USBP11- USBP11+ USBP12- USBP12+ — Front USB

GPP_E9/USB2_OC0# GPP_E10/USB2_OC1# GPP_E11/USB2_OC2# GPP_E12/USB2_OC3# GPP_F15/USB2_OCB_4 GPP_F16/USB2_OCB_5 GPP_F17/USB2_OCB_6 GPP_F18/USB2_OCB_7

OC0#7 OC1#1113 OC2# OC3#8 OC4#5 OC5#1 OC6#6 OC7#

R42 R43 R45 R126 R2888 R53 — 0 ohm

USB_OC0_REAR_7# USB_OC1_FRONT_1113# USB_OC3_REAR_8# USB_OC4_REAR_5# USB_OC5_INT_1# USB_OC6_REAR_6#

USB2_COMP USB2_VBUSSENSE RSVD_3 USB2_ID

PD_USB2_COMP R48 113 ohm +-1%
PD_USB2_VBUSSENSE R3072 1K ohm +-1%
PD_USB2_ID R50 1K ohm +-1%

GPD7/RSVD

2 OF 13

NB/SB Kabylake A0 QL0M Pre-QS Q270

INT USB 3.0 X1

SC86 SC89 0.1 uF USB3_TXN7_C USB3_TXP7_C

M.2_2230_WLAN

PCIE_LAN_RX4N PCIE_LAN_RX4P PCIE_LAN_TX4N_C PCIE_LAN_TX4P_C

PCIE_M.2_WLAN_RXN6 PCIE_M.2_WLAN_RXP6 PCIE_M.2_WLAN_TXN6 PCIE_M.2_WLAN_TXP6

+3V3_S5

OC2# OC7# OC3#8 — 10K ohm — R52 R1633 R3499 R3500 (NI)

U3F

USB3_1_TXN USB3_1_TXP USB3_1_RXN USB3_1_RXP
USB3_2_SSIC_1_TXN USB3_2_SSIC_1_TXP USB3_2_SSIC_1_RXN USB3_2_SSIC_1_RXP
USB3_6_TXN USB3_6_TXP USB3_6_RXN USB3_6_RXP
USB3_5_TXN USB3_5_TXP USB3_5_RXN USB3_5_RXP
USB3_3_SSIC_2_TXP USB3_3_SSIC_2_TXN USB3_3_SSIC_2_RXP USB3_3_SSIC_2_RXN
USB3_4_TXP USB3_4_TXN USB3_4_RXP USB3_4_RXN

GPP_A1/LAD0/ESPI_IO0 GPP_A2/LAD1/ESPI_IO1 GPP_A3/LAD2/ESPI_IO2 GPP_A4/LAD3/ESPI_IO3

LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 — 27,39

GPP_A5/LFRAME#/ESPI_CS0# GPP_A6/SERIRQ/ESPI_CS1# GPP_A7/PIRQA#/ESPI_ALERT0# GPP_A0/RCIN#/ESPI_ALERT1# GPP_A14/SUS_STAT#/ESPI_RESET#

LPC_FRAME# SER_IRQ LPC_DRQ0# KBRST# — 27,39 / 27

GPP_A9/CLKOUT_LPC0/ESPI_CLK GPP_A10/CLKOUT_LPC1

CK_LPC0_24M_R CK_LPC1_24M_R — 16

GPP_G19/SMI# GPP_G18/NMI# — R43 U45 FM_NMI_EVENT# SIO_SCI# 27

GPP_E6/DEVSLP2 GPP_E5/DEVSLP1 GPP_E4/DEVSLP0 GPP_F9/DEVSLP7 GPP_F8/DEVSLP6 GPP_F7/DEVSLP5 GPP_F6/DEVSLP4 GPP_F5/DEVSLP3

HDD_PWRGT 38
SSD_SATA_DEVSLP2 37
SSD_SATA_DEVSLP1 38
TPM_SPI_IRQ# 29

6 OF 13

NB/SB Kabylake A0 QL0M Pre-QS Q270

Rear USB 3.0 — SC1433 SC1432 0.1 uF USB3_TXN1_C USB3_TXP1_C
Rear USB 3.0 — SC82 SC81 0.1 uF USB3_TXN2_C USB3_TXP2_C
Front USB 3.0 — SC1435 SC1434 0.1 uF USB3_TXN6_C USB3_TXP6_C
Front USB 3.0 — SC109 SC110 0.1 uF USB3_TXN5_C USB3_TXP5_C
Rear USB 3.0 — SC1430 SC1431 0.1 uF USB3_TXP3_C USB3_TXN3_C
Rear USB 3.0 — SC1513 SC1514 0.1 uF USB3_TXP4_C USB3_TXN4_C

Rear USB 3.0 *3

+3V3_S5

FM_NMI_EVENT# GPP_A14 TPM_SPI_IRQ# — R651 R3086 R3551 — 10K ohm NI / 4.7K ohm

+3V3

SER_IRQ SIO_SCI# — R3073 R109 — 10K ohm
KBRST# — R3093 — 10K ohm

KBRST# — SC61 — 100 pF NPO 50 V

U3M

PCIE_21_RXN PCIE_21_RXP PCIE_21_TXP PCIE_22_RXN PCIE_22_RXP PCIE_22_TXN PCIE_22_TXP PCIE_23_RXN PCIE_23_RXP PCIE_23_TXN PCIE_23_TXP PCIE_24_RXN PCIE_24_RXP PCIE_24_TXN PCIE_24_TXP

PCIE21_M.2_SSD_RXN PCIE21_M.2_SSD_RXP PCIE21_M.2_SSD_TXN PCIE21_M.2_SSD_TXP PCIE22_M.2_SSD_RXN PCIE22_M.2_SSD_RXP PCIE22_M.2_SSD_TXN PCIE22_M.2_SSD_TXP PCIE23_M.2_SSD_RXN PCIE23_M.2_SSD_RXP PCIE23_M.2_SSD_TXN PCIE23_M.2_SSD_TXP PCIE24_M.2_SSD_RXN PCIE24_M.2_SSD_RXP PCIE24_M.2_SSD_TXN PCIE24_M.2_SSD_TXP — 38

M.2_2280_SSD#2

13 OF 13

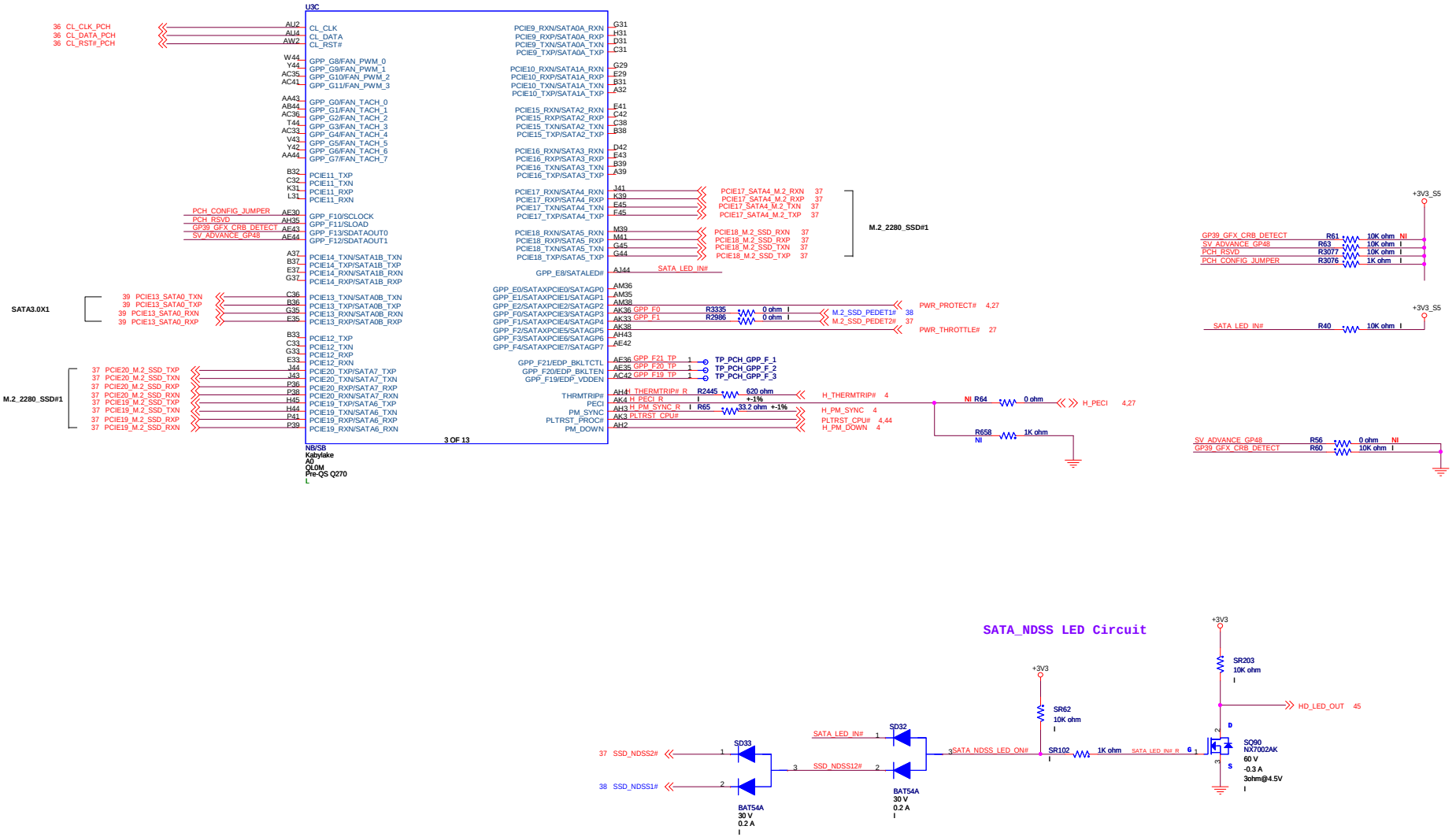
NB/SB Kabylake A0 QL0M Pre-QS Q270

LITE-ON TECHNOLOGY CORP.

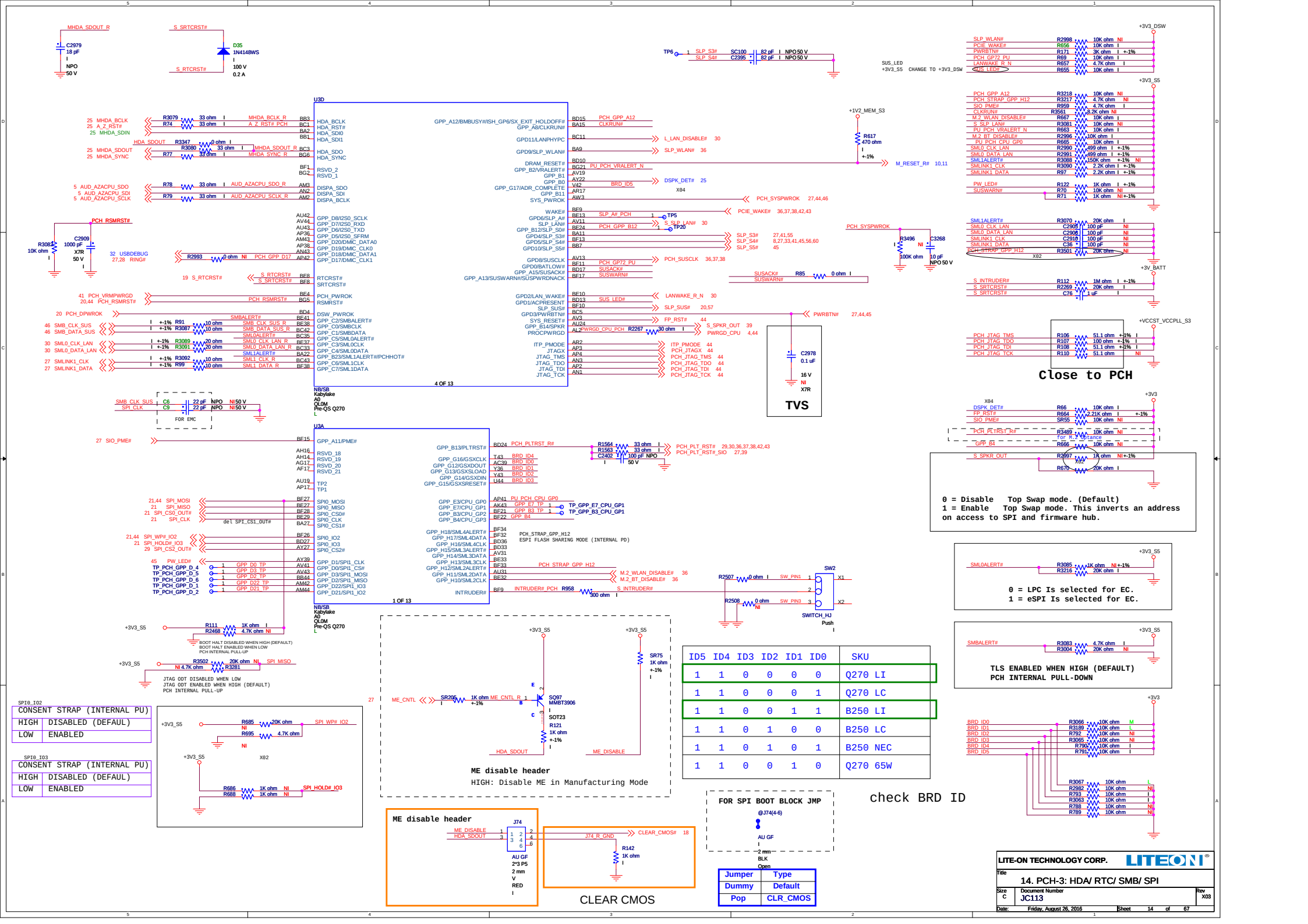
Title: 12. PCH-1: DMI/ USB/ LPC/ PCIe

Size	Document Number	Rev
C	JC113	X03

Date: Friday, August 26, 2016 Sheet 12 of 67



LITE-ON TECHNOLOGY CORP.		
Title	13. PCH-2: PCIe/ SATA/ FAN	
Size C	Document Number JC113	Rev X03
Date: Friday, August 26, 2016	Sheet 13 of 67	

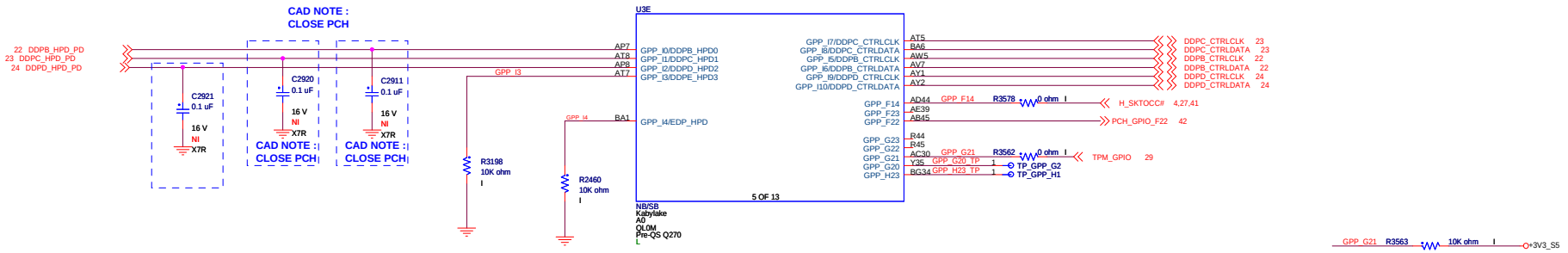


SPI0_IO2	
CONSENT STRAP (INTERNAL PU)	
HIGH	DISABLED (DEFAUL)
LOW	ENABLED

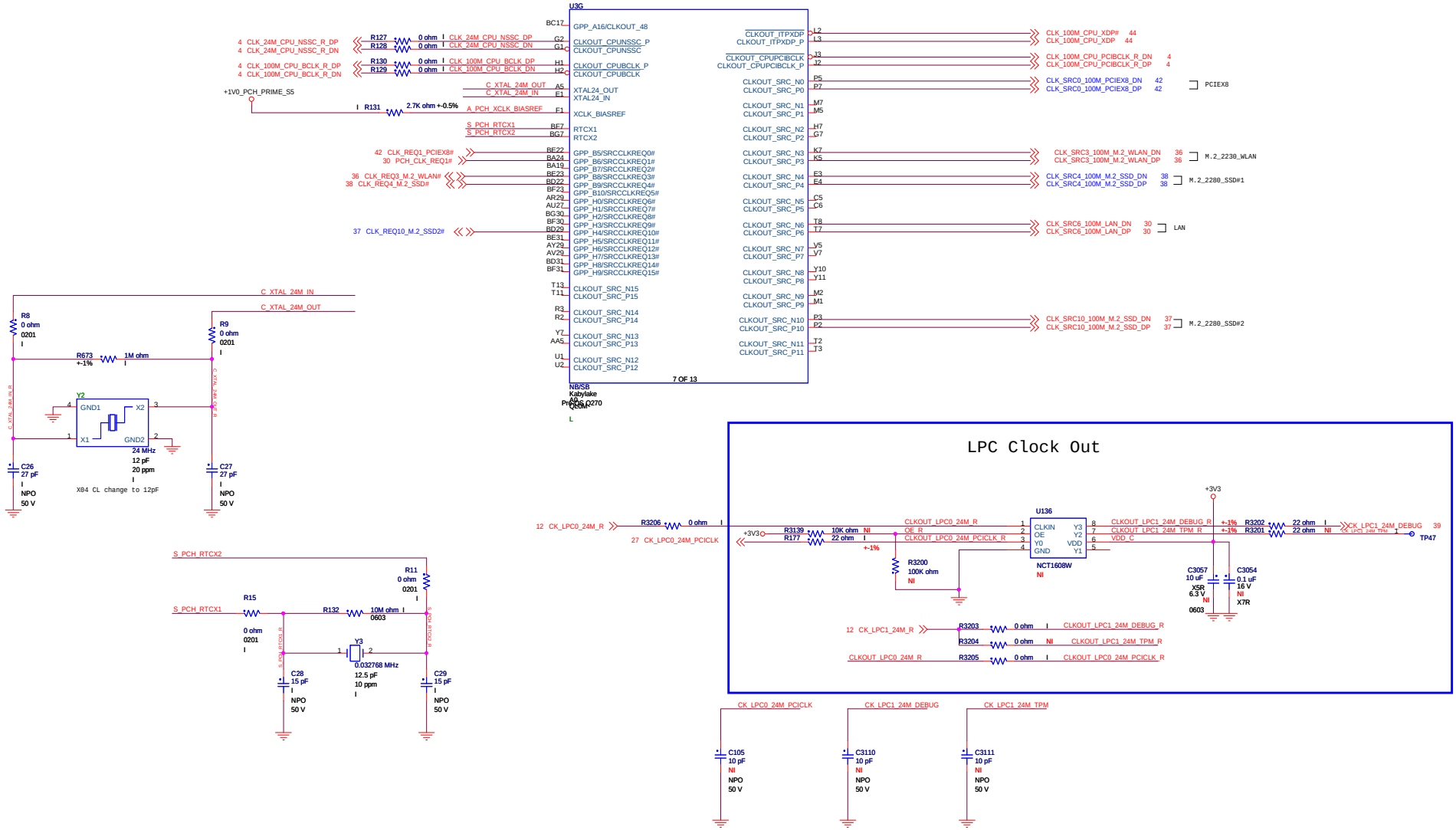
SPI0_IO3	
CONSENT STRAP (INTERNAL PU)	
HIGH	DISABLED (DEFAUL)
LOW	ENABLED

ID5	ID4	ID3	ID2	ID1	ID0	SKU
1	1	0	0	0	0	Q270 LI
1	1	0	0	0	1	Q270 LC
1	1	0	0	1	1	B250 LI
1	1	0	1	0	0	B250 LC
1	1	0	1	0	1	B250 NEC
1	1	0	0	1	0	Q270 65W

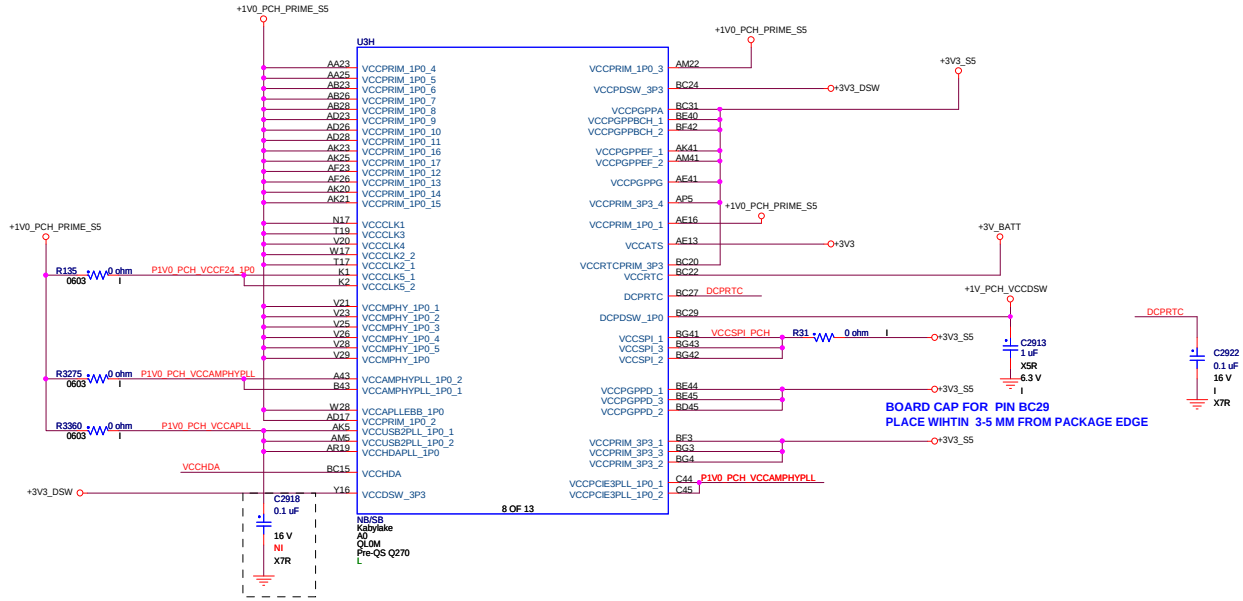
Jumper	Type
Dummy	Default
Pop	CLR_CMOS



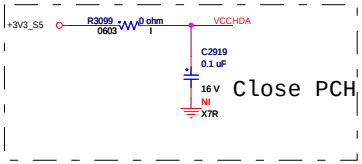
LITE-ON TECHNOLOGY CORP.		
Title: 15. PCH-4: Display		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 15 of 67	



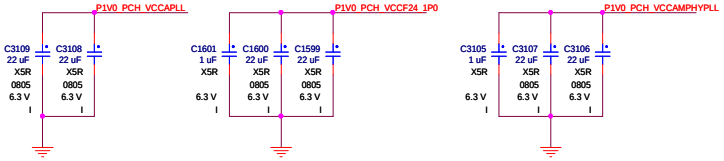
LITE-ON TECHNOLOGY CORP.		
Title: 16. PCH-5: Clock		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 16 of 67	

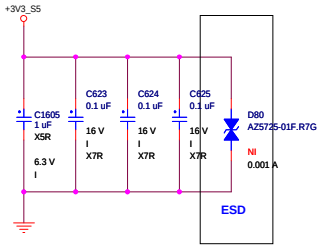


Close AR19 (VCCHDAPLL)



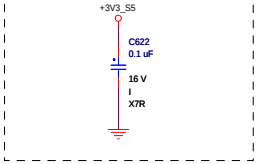
Close PCH





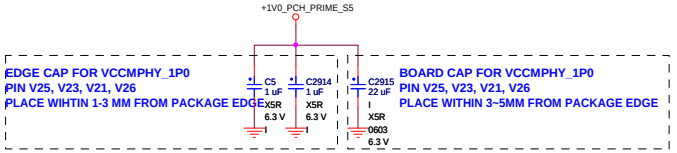
BOARD CAP FOR PIN AE13
PLACE WIHTIN 3-5 MM FROM PACKAGE EDGE

BOARD CAP FOR PIN BE40
PLACE WIHTIN 3-5 MM FROM PACKAGE EDGE



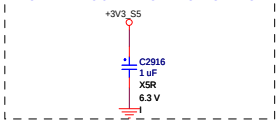
BOARD CAP FOR PIN BC29
PLACE WIHTIN 3-5 MM FROM PACKAGE EDGE

EDGE CAP FOR VCCMPHY_1P0
PIN V25, V23, V21, V26
PLACE WIHTIN 1-3 MM FROM PACKAGE EDGE

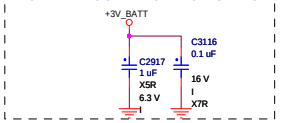


BOARD CAP FOR VCCMPHY_1P0
PIN V25, V23, V21, V26
PLACE WITHIN 3~5MM FROM PACKAGE EDGE

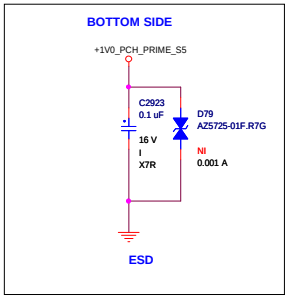
BOARD CAP FOR PIN BC20
PLACE WIHTIN 3-5 MM FROM PACKAGE EDGE



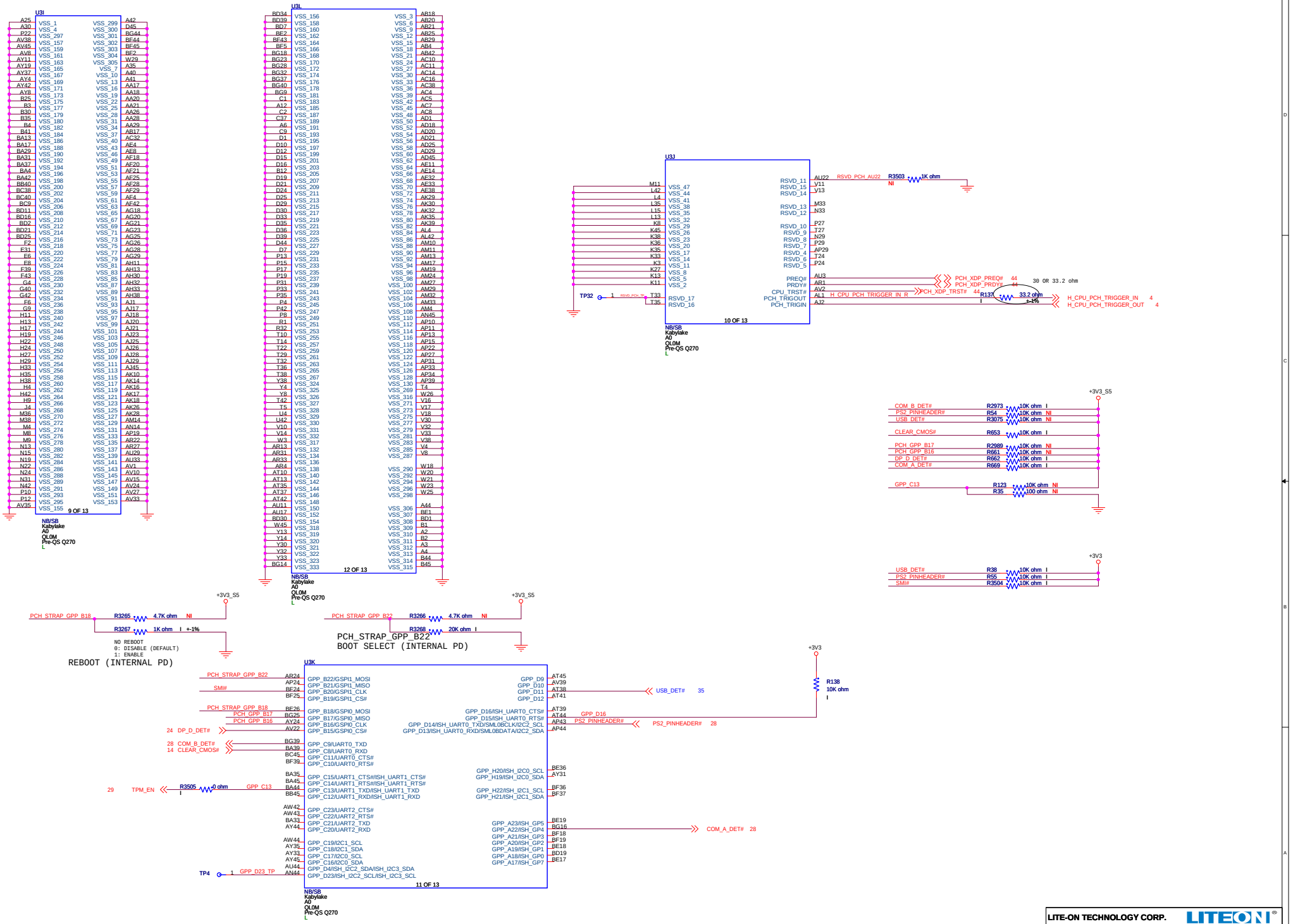
EDGE CAP FOR PIN BC22
PLACE WIHTIN 3-5 MM FROM PACKAGE EDGE



BOTTOM SIDE

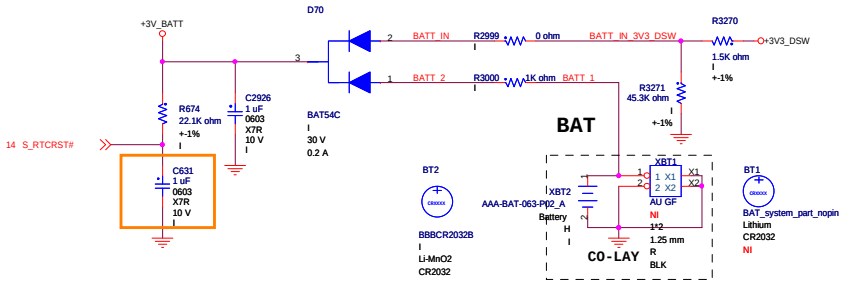


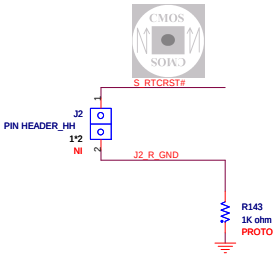
LITE-ON TECHNOLOGY CORP.		LITEON
Title: 17. PCH-6: Power 1		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 17 of 67	



LITE-ON TECHNOLOGY CORP.	LITEON
Title	18. PCH-8: GND
Size C	Document Number JC113
Rev	X03
Date: Friday, August 26, 2016	Sheet 18 of 67

BATTERY CIRCUIT

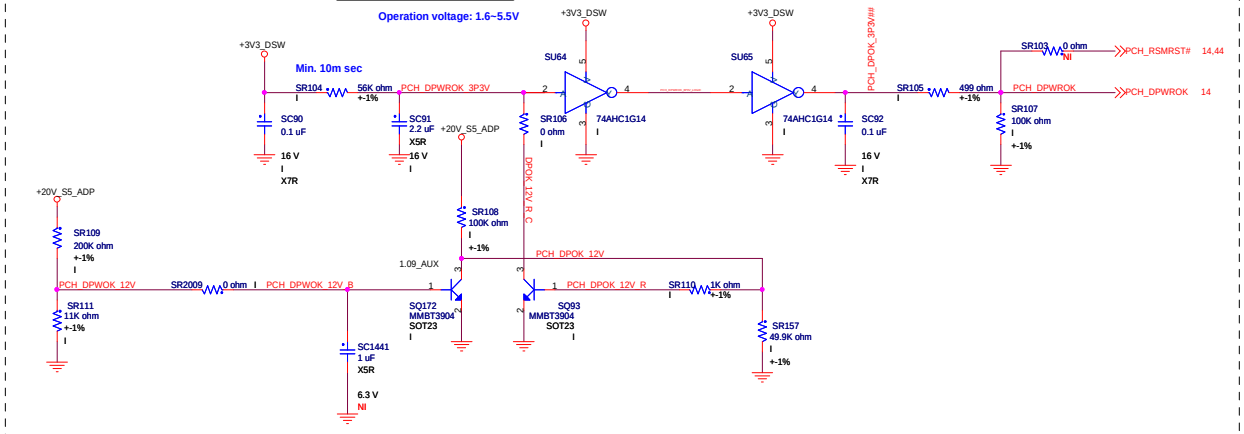


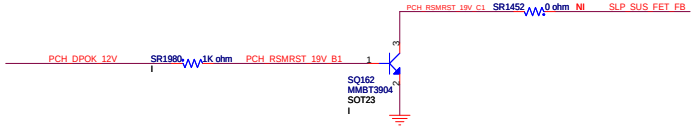


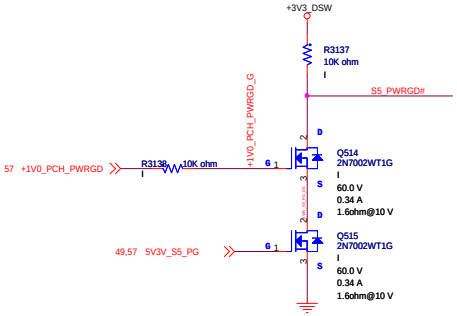
LITE-ON TECHNOLOGY CORP.		
Title: 19. CMOS Clear / Battery		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 19 of 67	

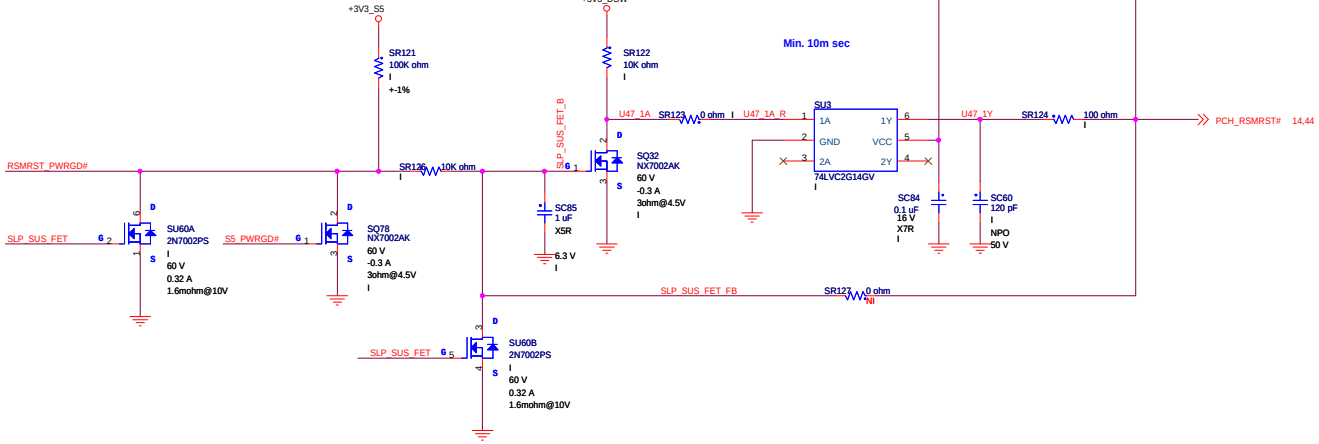
PCH_DPWROK

Operation voltage: 1.6~5.5V

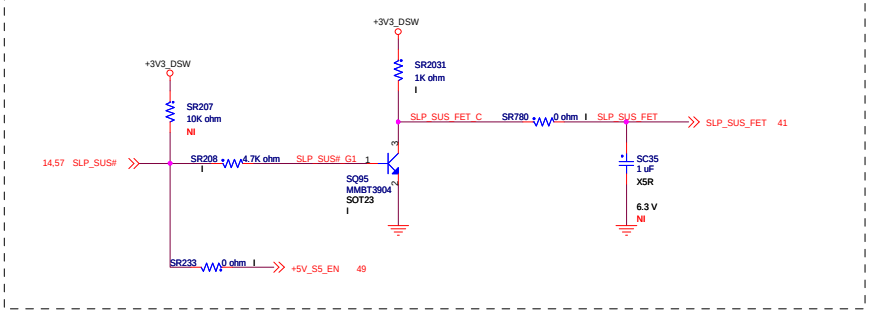




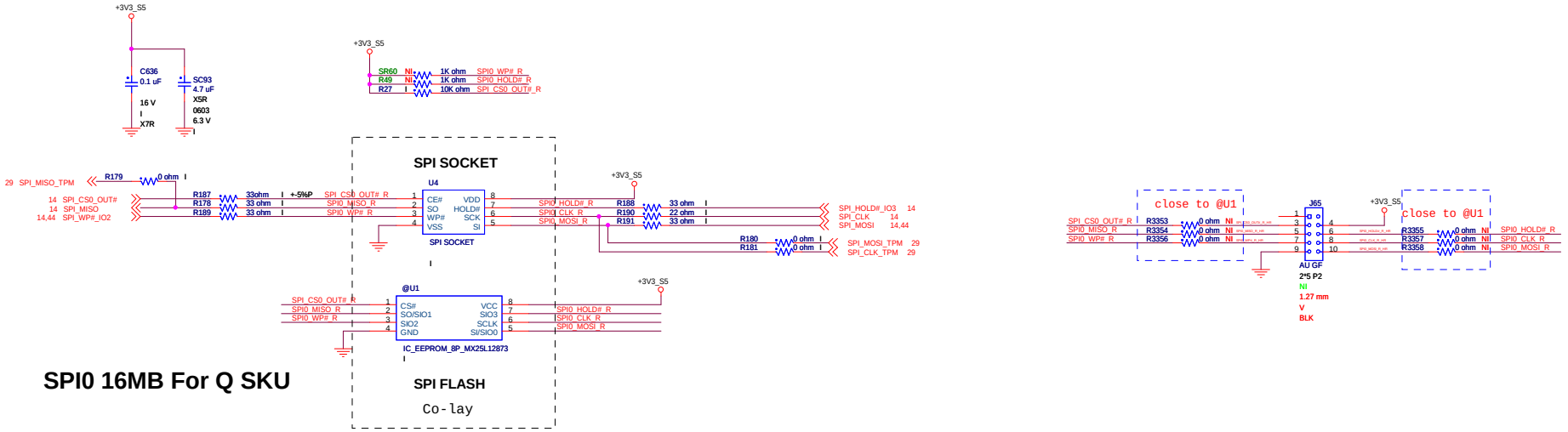




DSW CONTROL SIGNAL

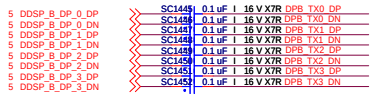


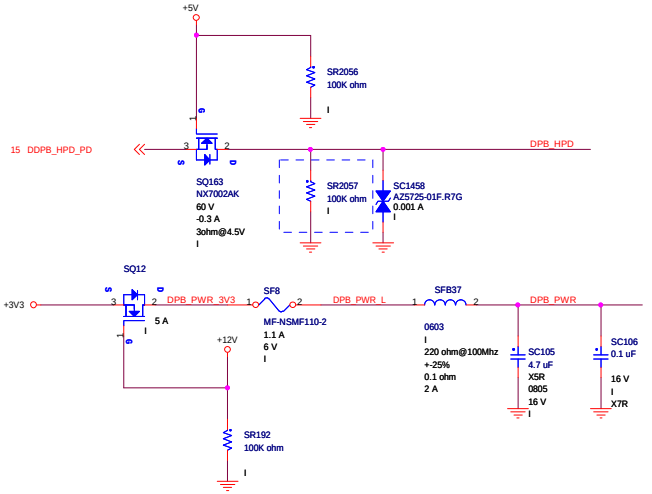
LITE-ON TECHNOLOGY CORP.		
Title: 20. DSW		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 20 of 67	

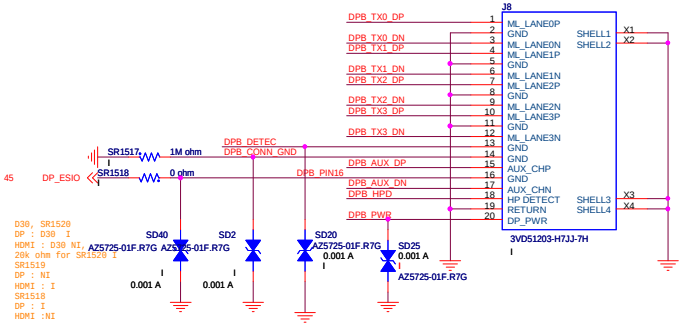


LITE-ON TECHNOLOGY CORP.		
Title: 21. SPI ROM		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 21 of 67	

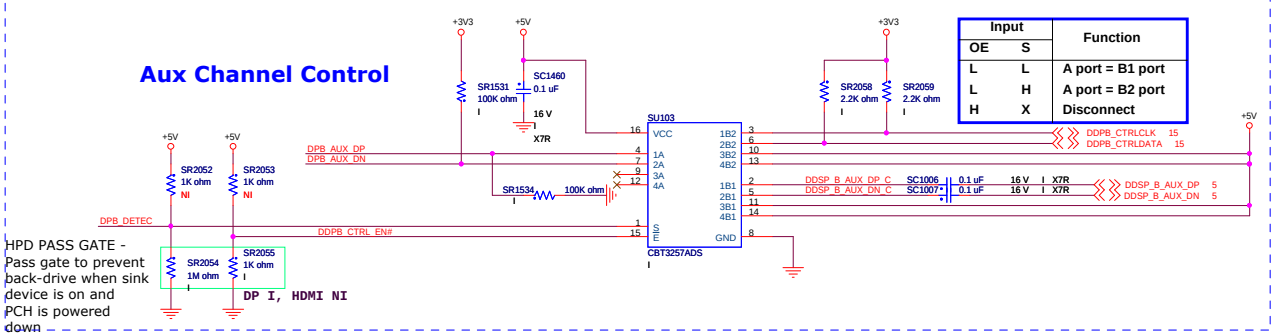
DISPLAY PORT





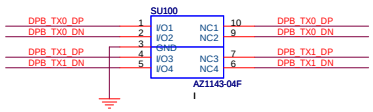


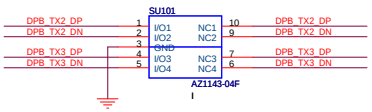
Aux Channel Control

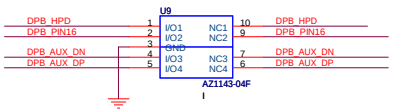


Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

HPD PASS GATE -
Pass gate to prevent back-drive when sink device is on and PCH is powered down



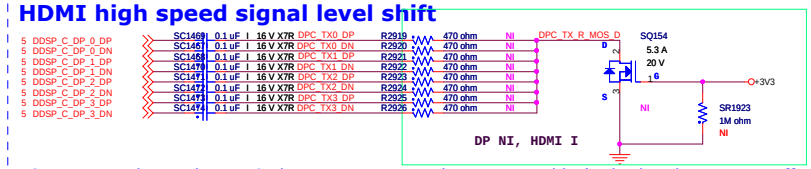




CAD Note : Please place ESD component close to DP connector

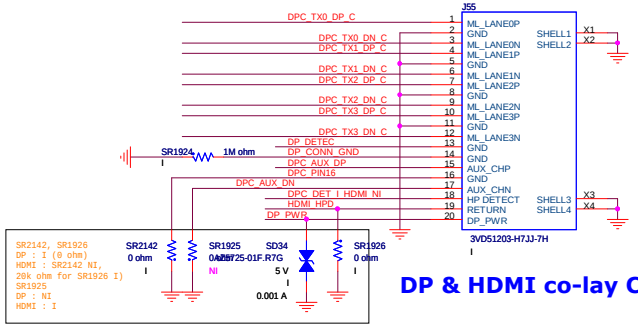
LITE-ON TECHNOLOGY CORP.		
Title: 22. Display Port B		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 22 of 67	

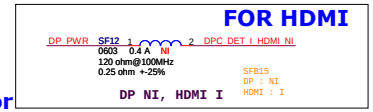
HDMI high speed signal level shift

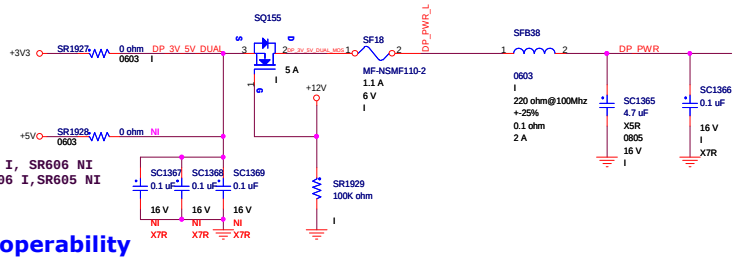


CAD Note : Please place 470 ohm component as short as passable (to bridge the antenna effect)

DP & HDMI co-lay Connector

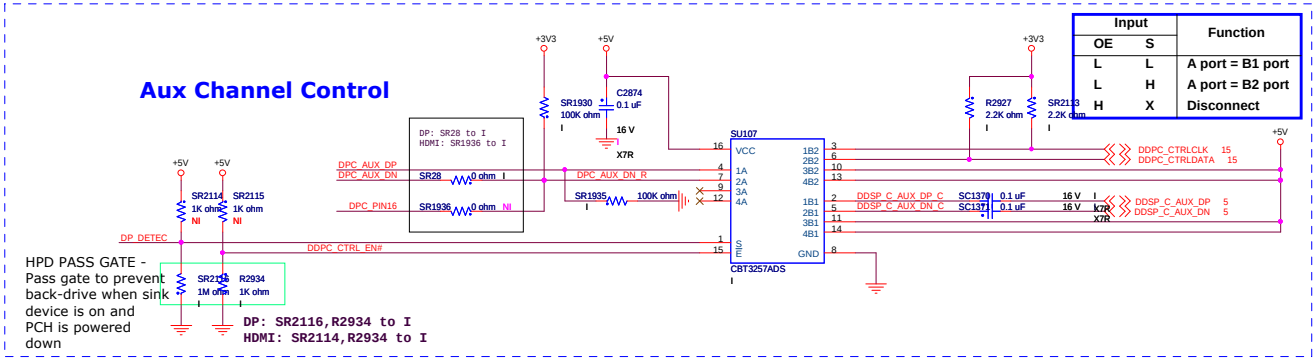




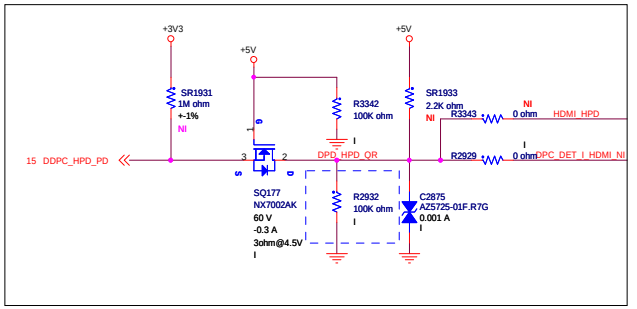


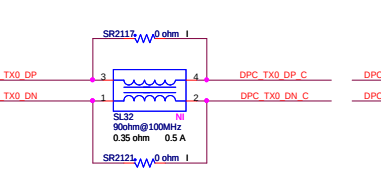
DisplayPort Interoperability

Aux Channel Control

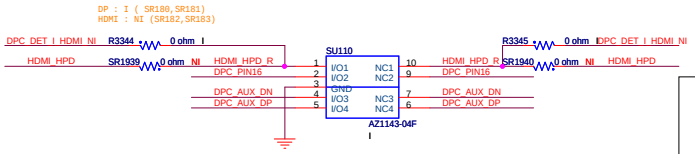


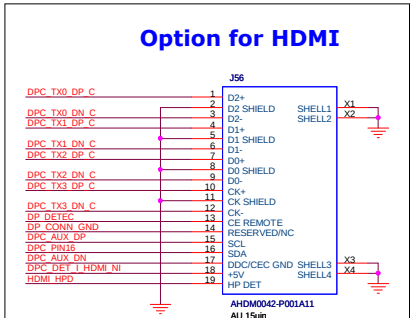
Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect





CAD Note : Please place ESD component close to DP connector





CAD Note : Please place Common Choke component close to DP & HDMI connector

LITE-ON TECHNOLOGY CORP.			
Title: 23. Display Port C			
Size: C	Document Number: JC113		Rev: X03
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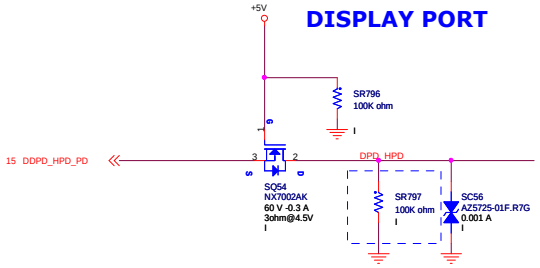
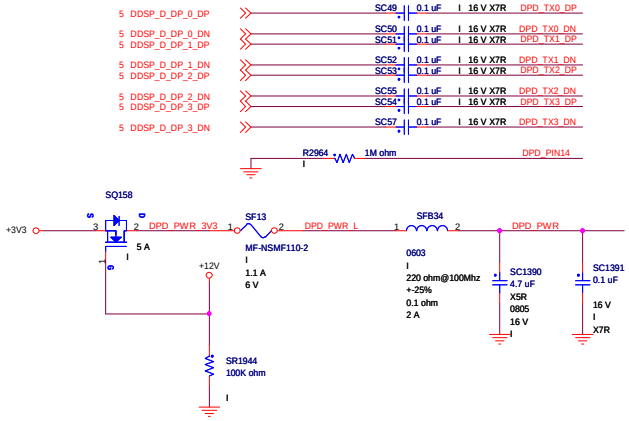
DISPLAY PORT

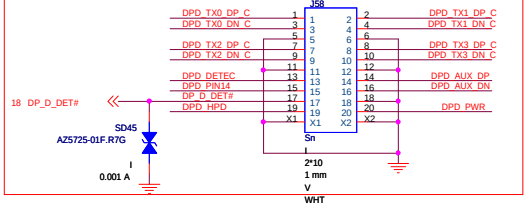


CAD NOTE:
PLACE NEAR CONNECTOR PIN

HPD PASS GATE -
Pass gate to prevent back-drive when sink device is on and PCH is powered down

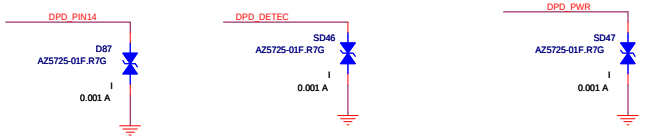


J24 Footprint is special ,for Tiny II only use, other project don't use.

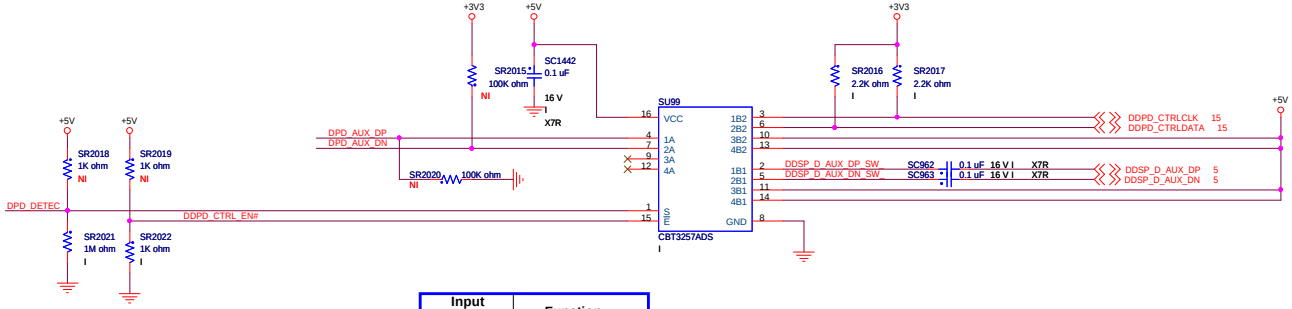


On Cable side Pin17 & Pin 18 need short

DPC_DETEC
L : Connect to Display Port or No Connection
H : Connect to Doungle

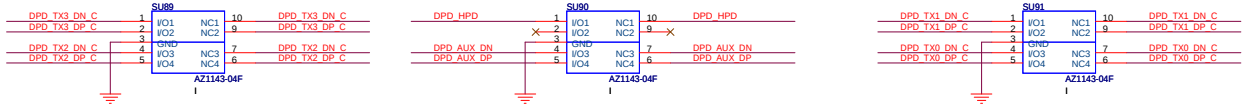


DisplayPort Interoperability



Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

CAD Note : Please place ESD component close to DP connector



DP used 0 ohm
HDMI used Common Choke

DP used 0 ohm
HDMI used Common Choke

DP used 0 ohm
HDMI used Common Choke

DP used 0 ohm
HDMI used Common Choke

CAD Note : Please place Common Choke component close to J9 pinheader

LITE-ON TECHNOLOGY CORP.		
Title	24. Display Port D	
Size C	Document Number JC113	Rev X03
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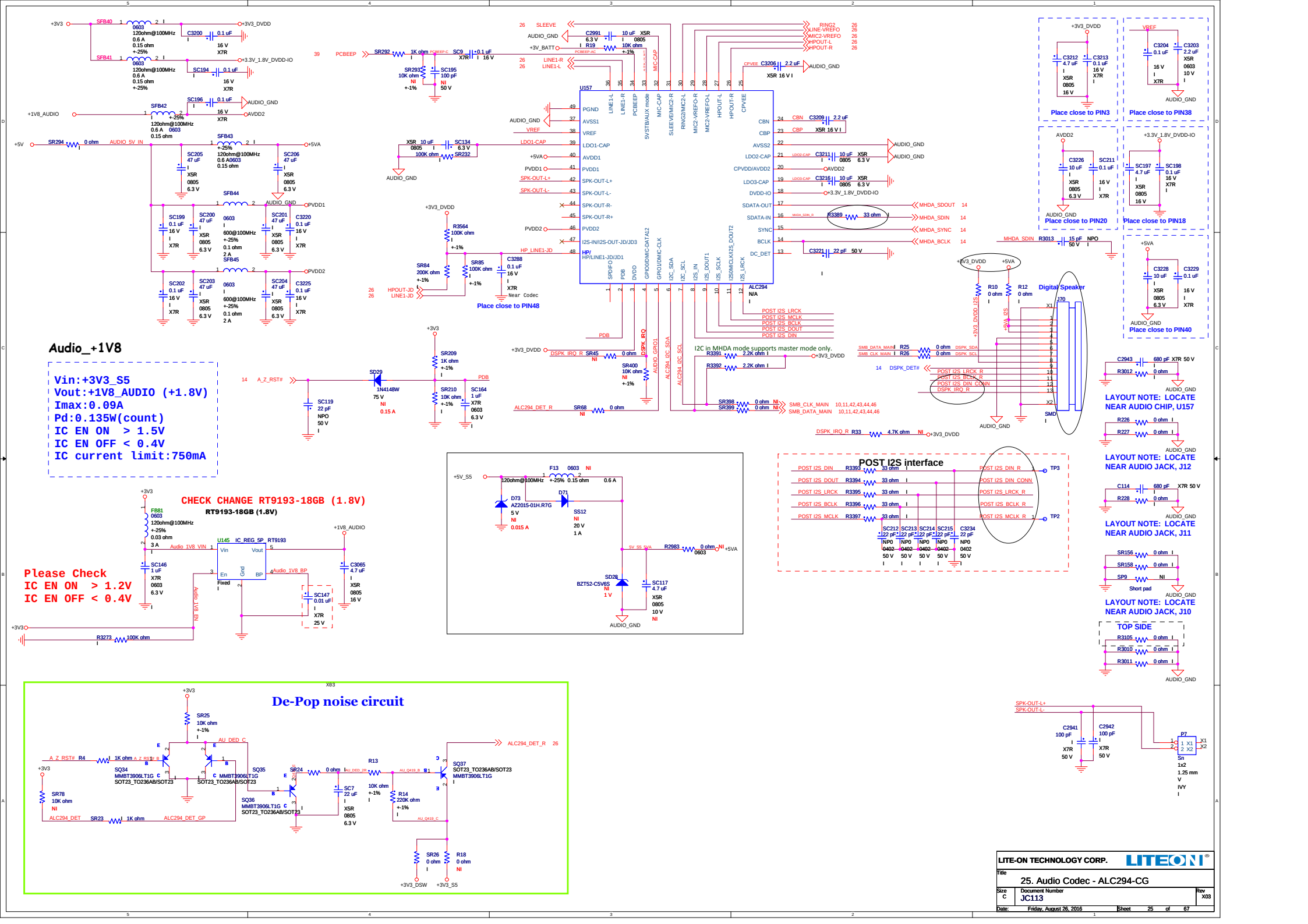
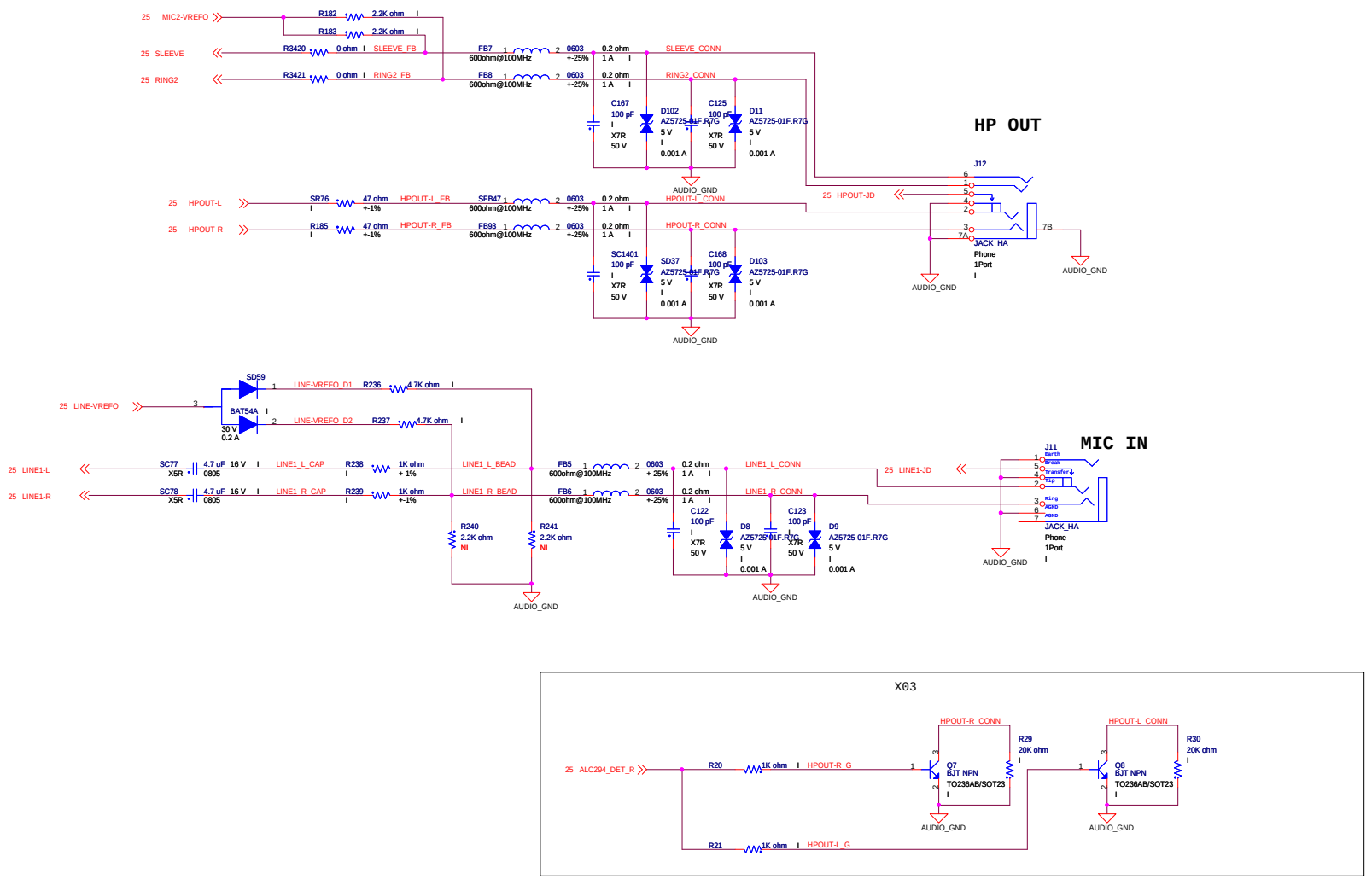
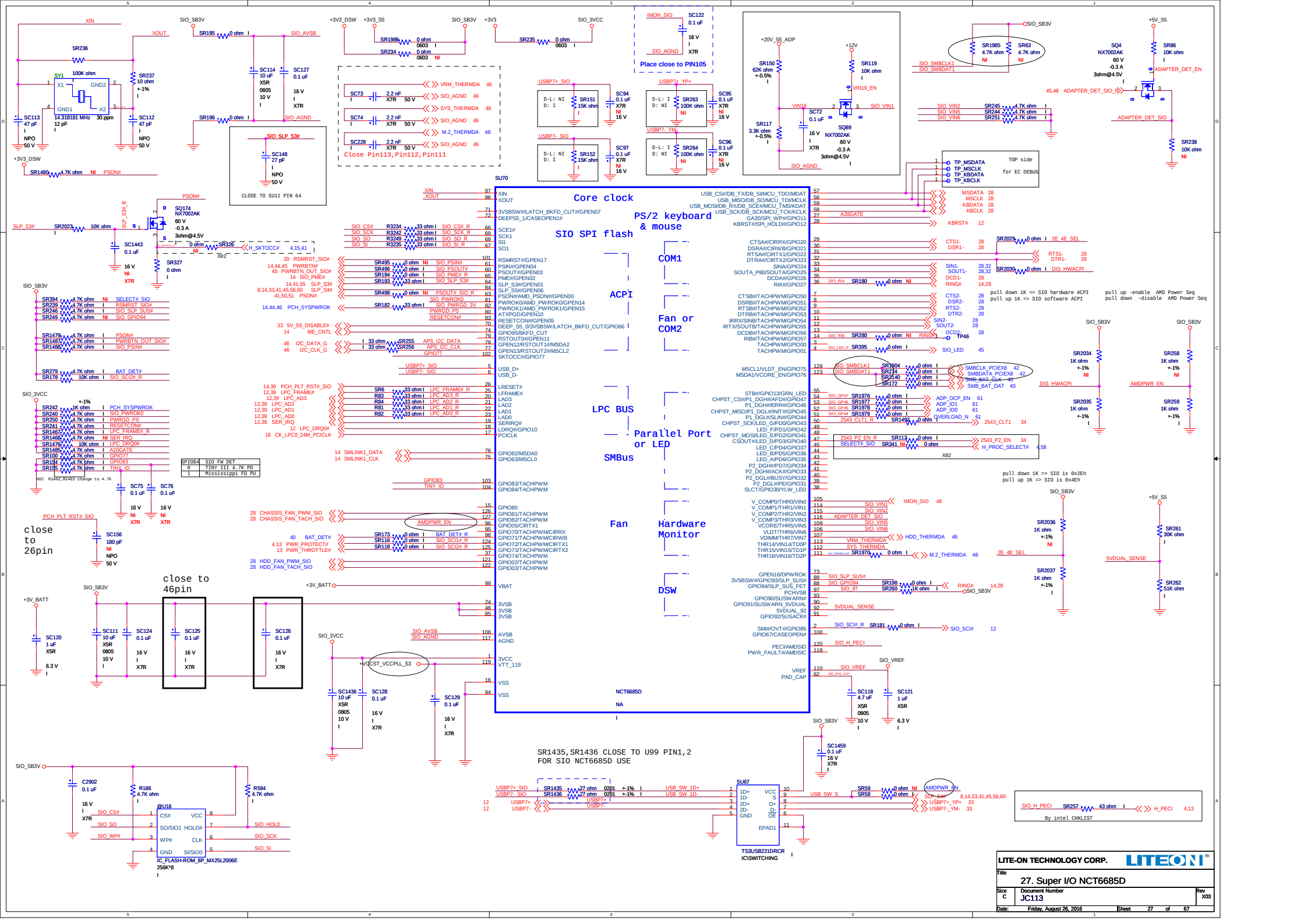

Audio_+1V8
Vin:+3V3_S5
Vout:+1V8_AUDIO (+1.8V)
Imax:0.09A
Pd:0.135W(count)
IC EN ON > 1.5V
IC EN OFF < 0.4V
IC current limit:750mA
CHECK CHANGE RT9193-18GB (1.8V)
RT9193-18GB (1.8V)
Please Check
IC EN ON > 1.2V
IC EN OFF < 0.4V
De-Pop noise circuit
Place close to PIN3
Place close to PIN38
Place close to PIN20
Place close to PIN18
Place close to PIN40
Place close to PIN48
Digital Speaker
I2C in MHDA mode supports master mode only.
POST I2S interface
LAYOUT NOTE: LOCATE NEAR AUDIO CHIP, U157
LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J12
LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J11
LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J10
TOP SIDE
LITE-ON TECHNOLOGY CORP.
25. Audio Codec - ALC294-CG
JC113
Friday, August 26, 2016



LITE-ON TECHNOLOGY CORP.		
Title: 26. Audio Jack_Line I-O/ Mic in		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 26 of 67	


SU70
Core clock
PS/2 keyboard & mouse
SIO SPI flash
COM1
ACPI
Fan or COM2
LPC BUS
Parallel Port or LED
SMBus
Fan
Hardware Monitor
DSW
NCT6685D
NA
close to 26pin
close to 46pin
SR1435,SR1436 CLOSE TO U99 PIN1,2 FOR SIO NCT6685D USE
Close Pin113,Pin112,Pin111
CLOSE TO SU11 PIN 64
Place close to PIN105
TOP side for EC DEBUG
pull down 1K => SIO hardware ACPI
pull up 1K => SIO software ACPI
pull up -enable AMD Power Seq
pull down -disable AMD Power Seq
pull down 1K => SIO is 0x2Eh
pull up 1K => SIO is 0x4Eh
IC_FLASH-ROM_8P_MX25L2006E 256K*8
TS3USB221DRCR IC\SWITCHING
LITE-ON TECHNOLOGY CORP.
27. Super I/O NCT6685D
Size C
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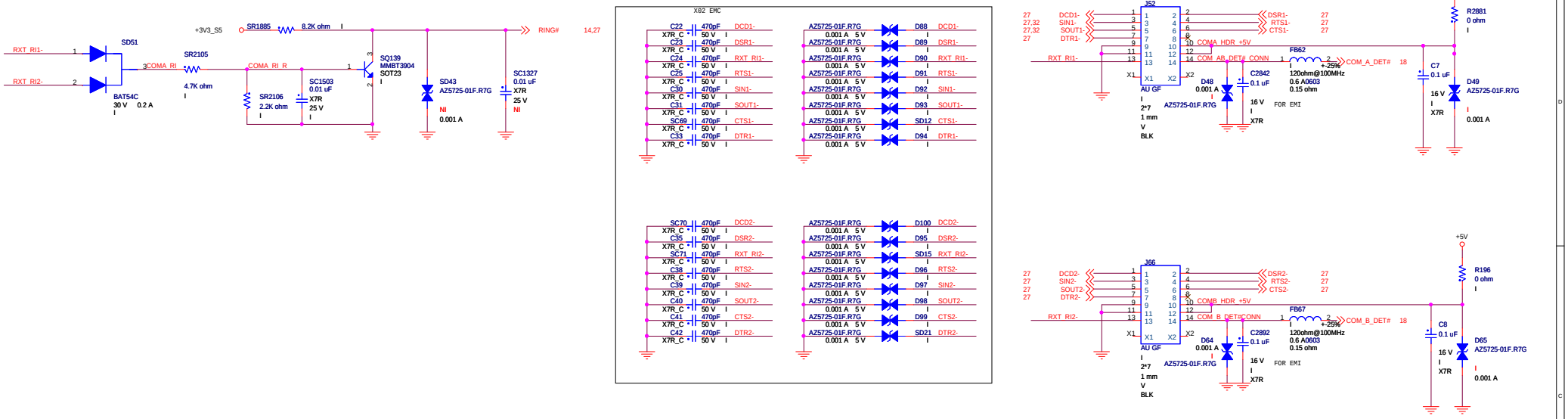
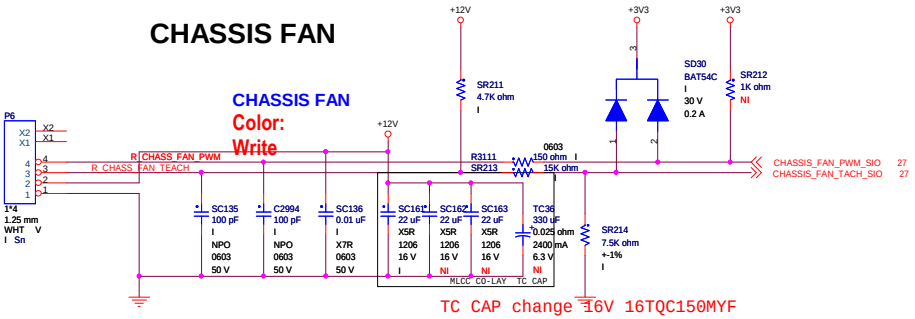
COM PORT HDR x2

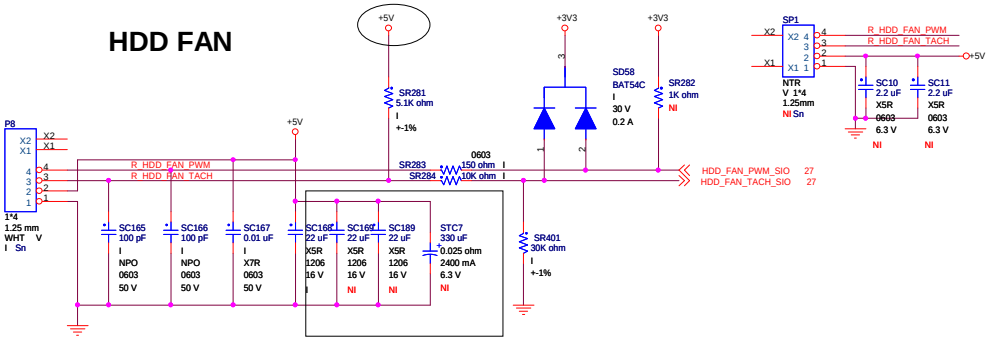


CHASSIS FAN

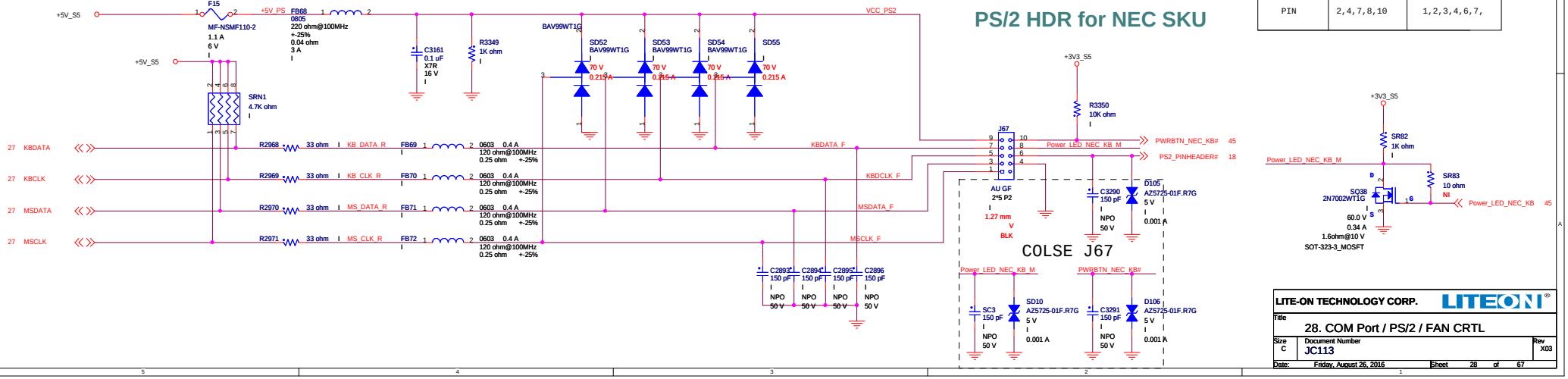


TC CAP change 16V 16TQC150MYF

HDD FAN



M.2 FAN



Function	Mouse	NEC KeyBoard
PIN	2,4,7,8,10	1,2,3,4,6,7,

LITE-ON TECHNOLOGY CORP.

Title: 28. COM Port / PS/2 / FAN CRTL

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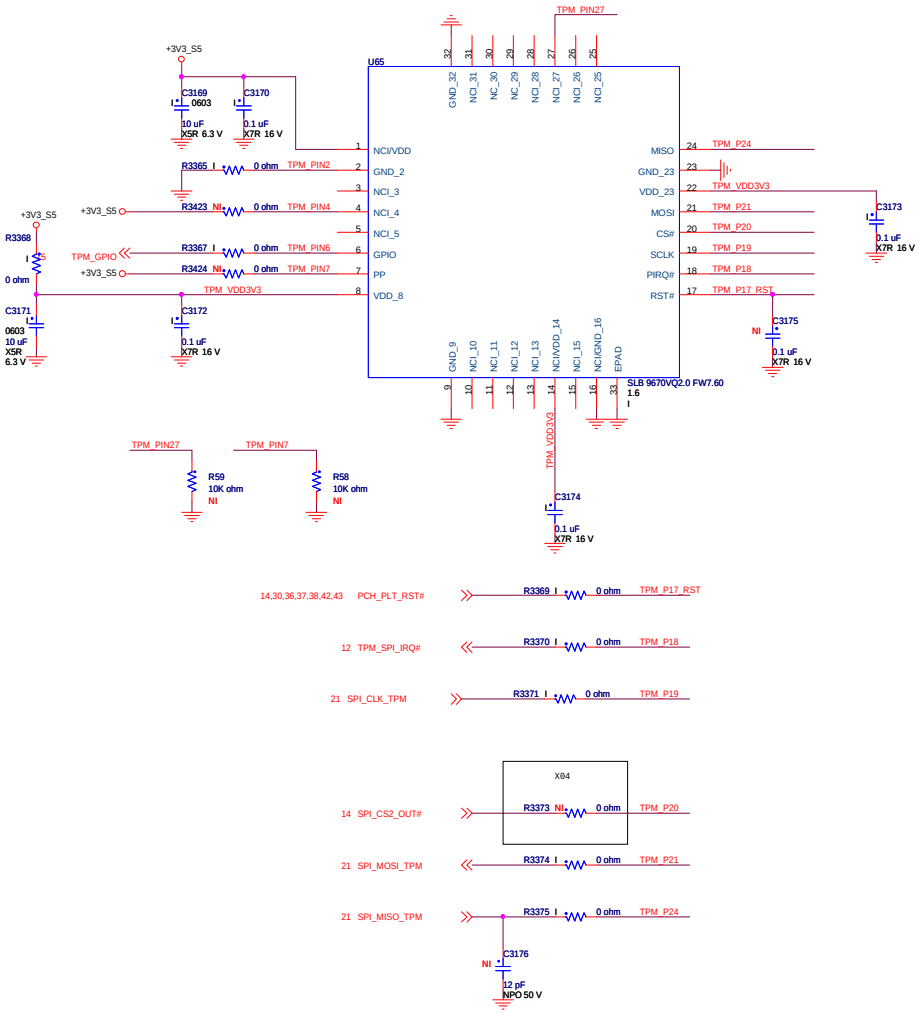

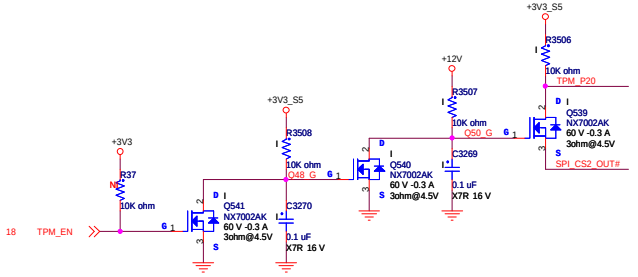

BOM	PIN	NCT650LBAYX(SPI)	BT00012901IB-R SLB9670(SPI)	ST33HTPH2E32AAE8(SPI)
GND	2		R3365	R3365
GPIO	6	R3367	R3367	
CLKRUN	13			
AD3	15			
IRQ#(R1164)/AD2(R628)	18	R3370	R3370	R3370
CLK	19	R3371	R3371	R3371
CS#(R616)/LPC Frame#(R625)	20	R3373	R3373	R3373
MOSI(R617)/AD1(R626)	21	R3374	R3374	R3374
MISO(R615)/AD0(R624)	24	R3375	R3375	R3375

LITE-ON TECHNOLOGY CORP.

Title: 29. TPM - ST ST33ZP24AR28PVSH

Size	Document Number	Rev
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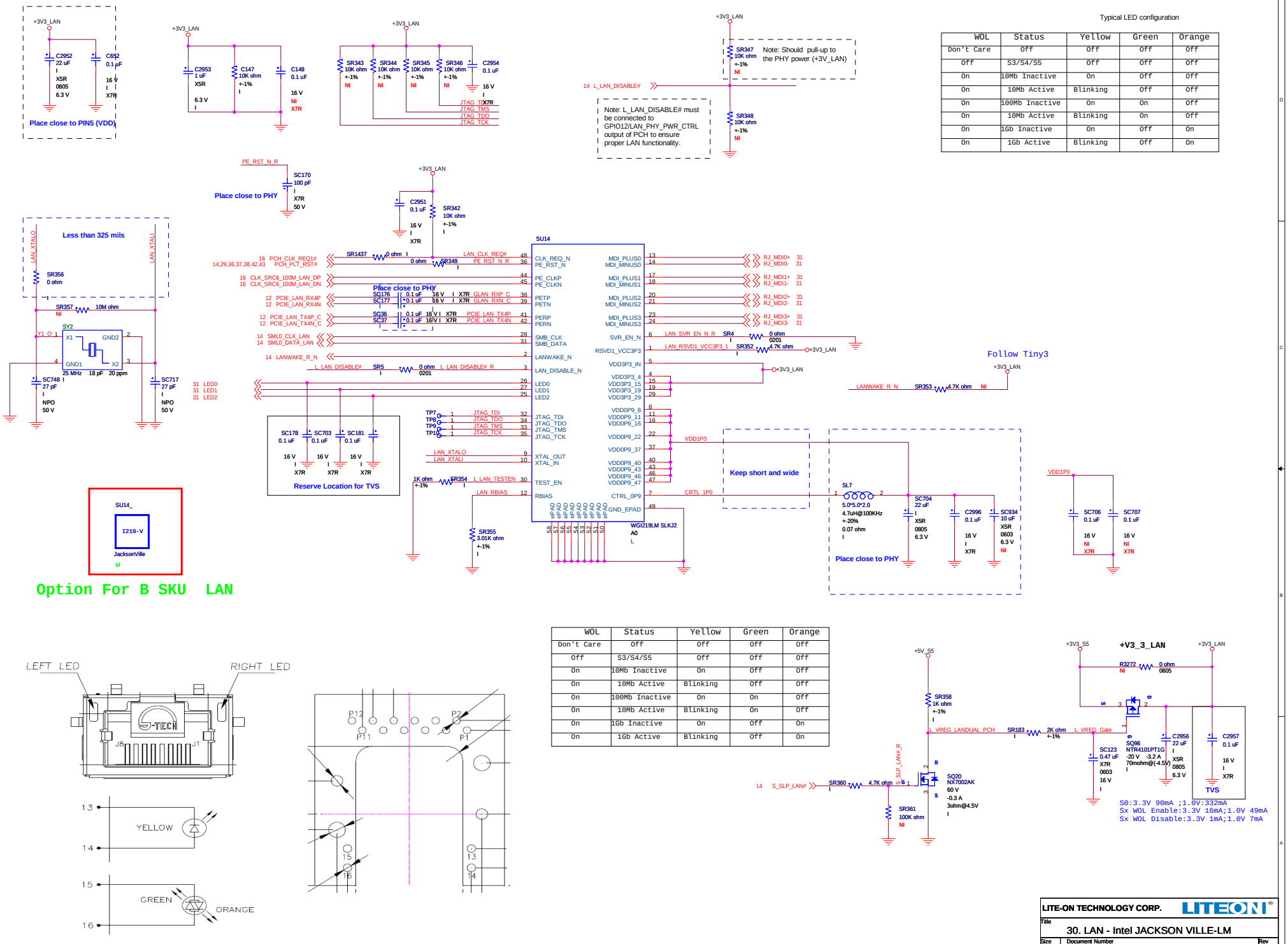

WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	S3/S4/S5	Off	Off	Off
On	10Mb Inactive	On	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	On	On	Off
On	10Mb Active	Blinking	On	Off
On	1Gb Inactive	On	Off	On
On	1Gb Active	Blinking	Off	On

WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	S3/S4/S5	Off	Off	Off
On	10Mb Inactive	On	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	On	On	Off
On	10Mb Active	Blinking	On	Off
On	1Gb Inactive	On	Off	On
On	1Gb Active	Blinking	Off	On

LITE-ON TECHNOLOGY CORP.			
Title	30. LAN - Intel JACKSON VILLE-LM		
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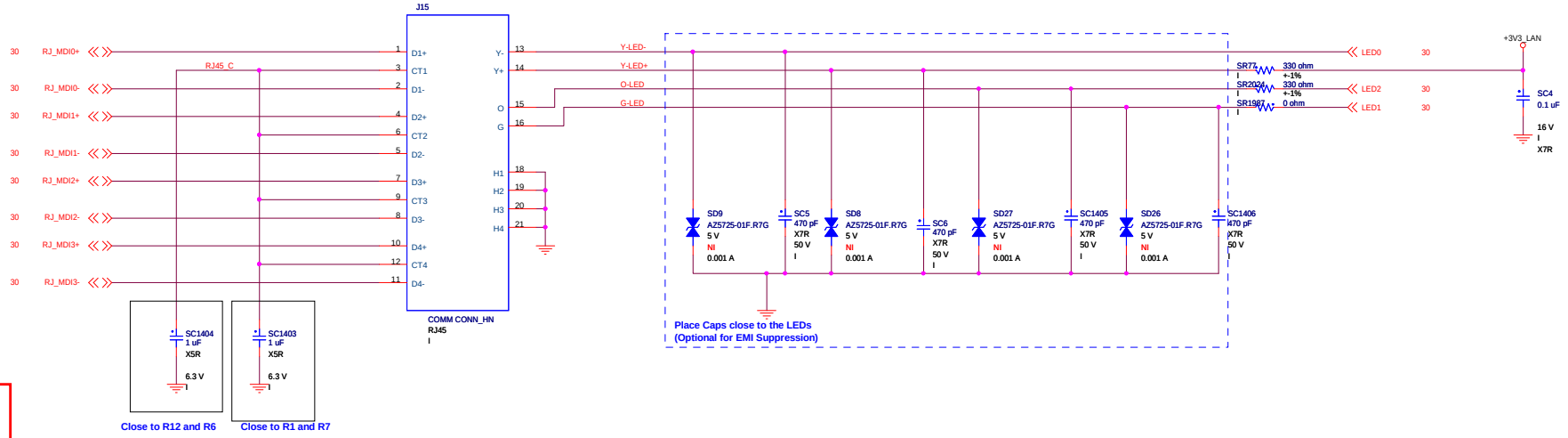
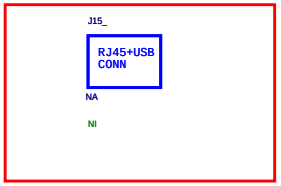
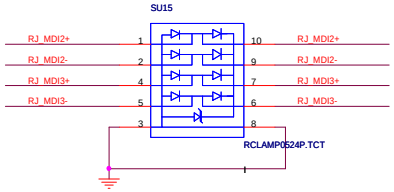
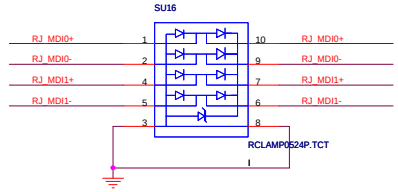




Option For LC SKU





LITE-ON TECHNOLOGY CORP.		
Title: 31. RJ45		
Size: C	Document Number: JC113	Rev: X03
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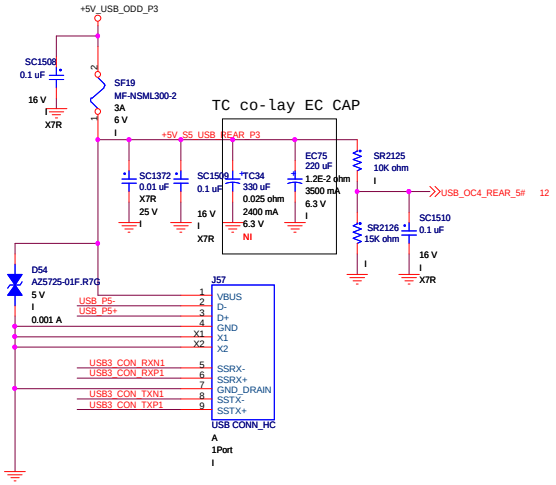
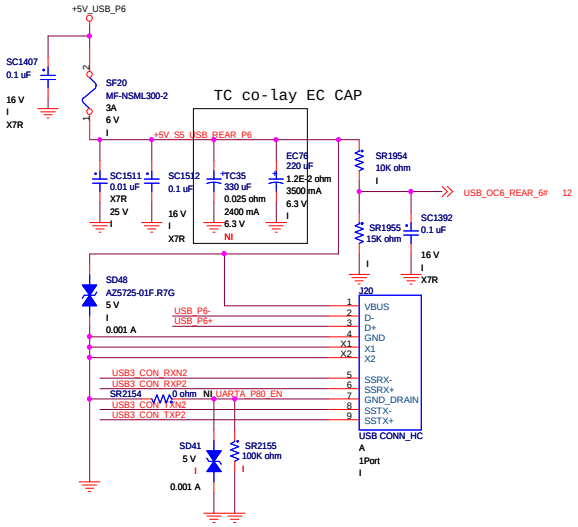
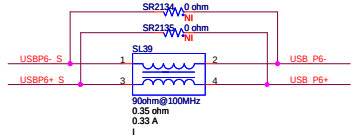
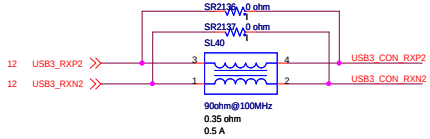
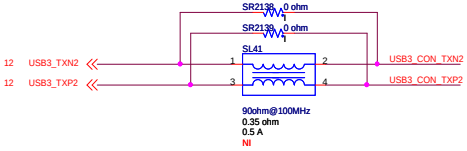
Rear Side USB ODD

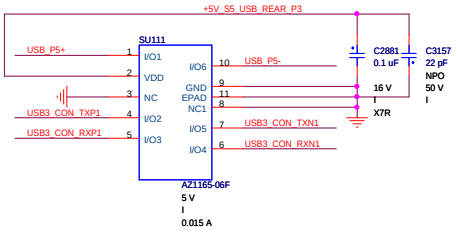


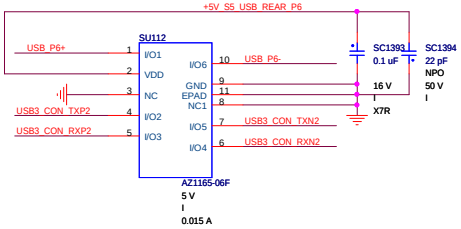


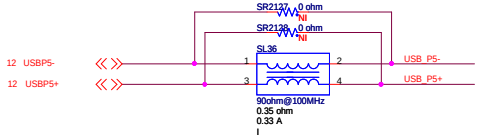


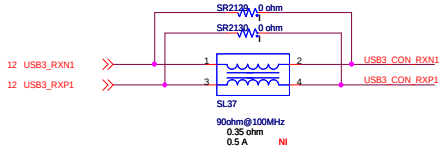


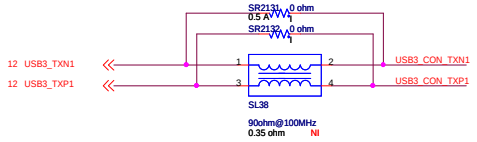




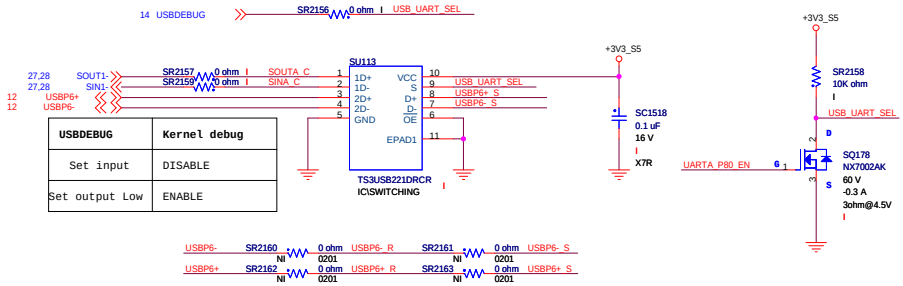








For USB Debug Function



USBDEBUG	Kernel debug
Set input	DISABLE
Set output Low	ENABLE

OE#	S	Function
H	X	Disable
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

UARTA_P80_EN	POST 80
L	DISABLE
H	ENABLE

LITE-ON TECHNOLOGY CORP.

Title: 32. USB3.0 ODD CONN

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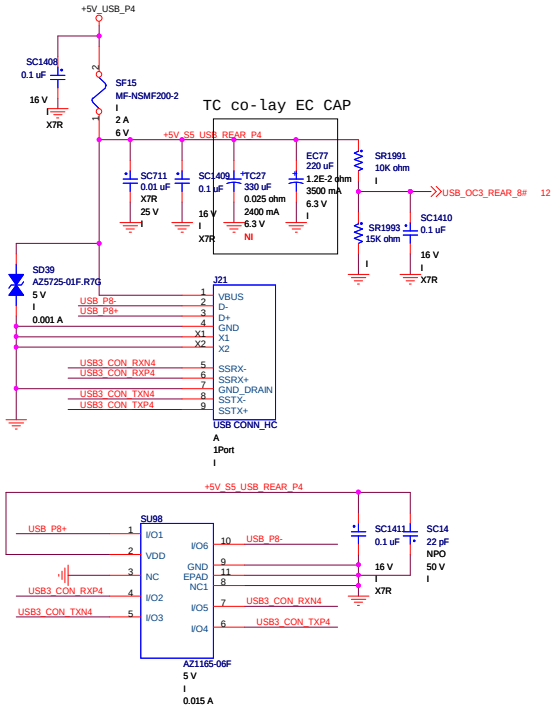
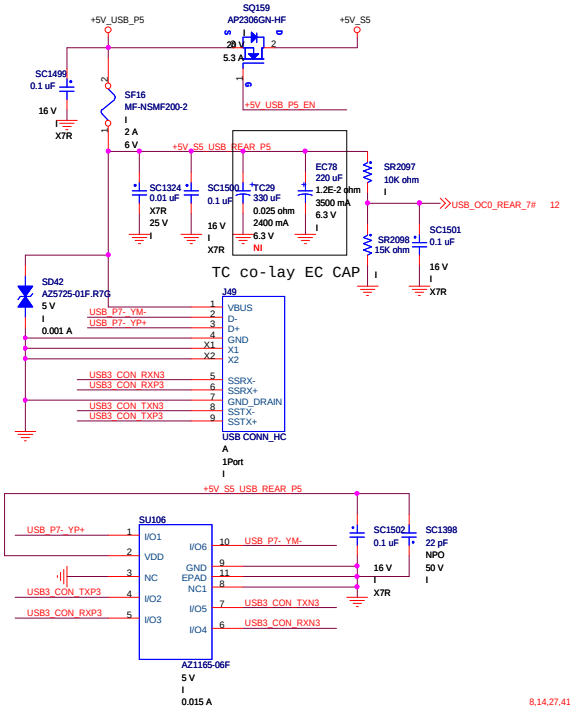
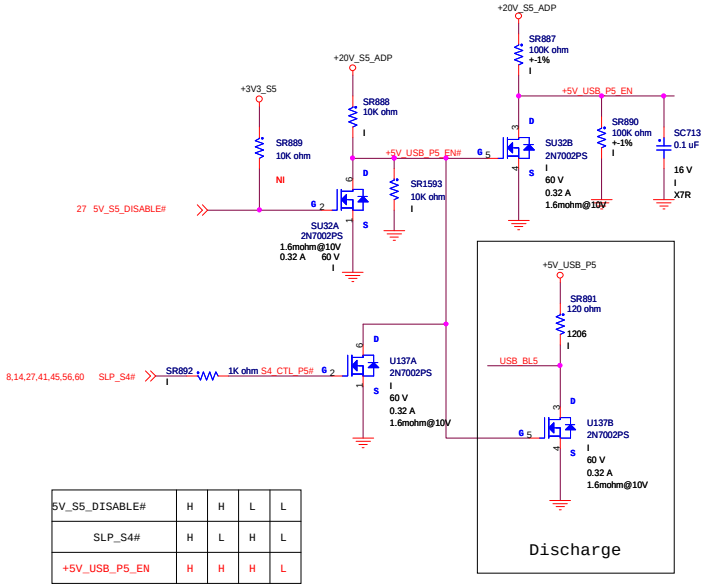
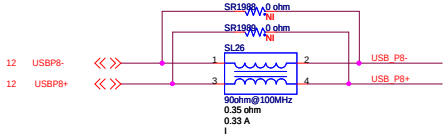
Rear Side USBx2

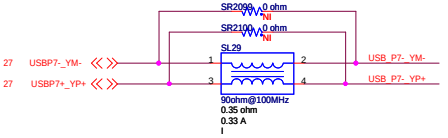


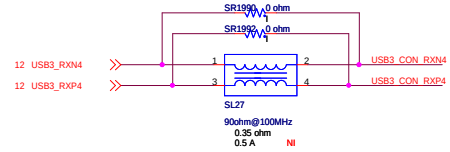


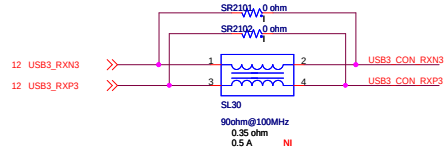


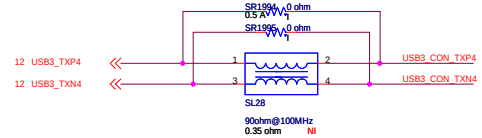
5V_S5_DISABLE#	H	H	L	L
SLP_S4#	H	L	H	L
+5V_USB_P5_EN	H	H	H	L

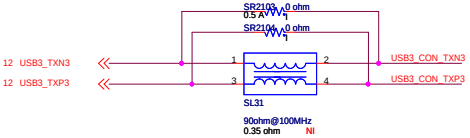












LITE-ON TECHNOLOGY CORP.	LITEON
Title	33. USB3.0 CONN x 2
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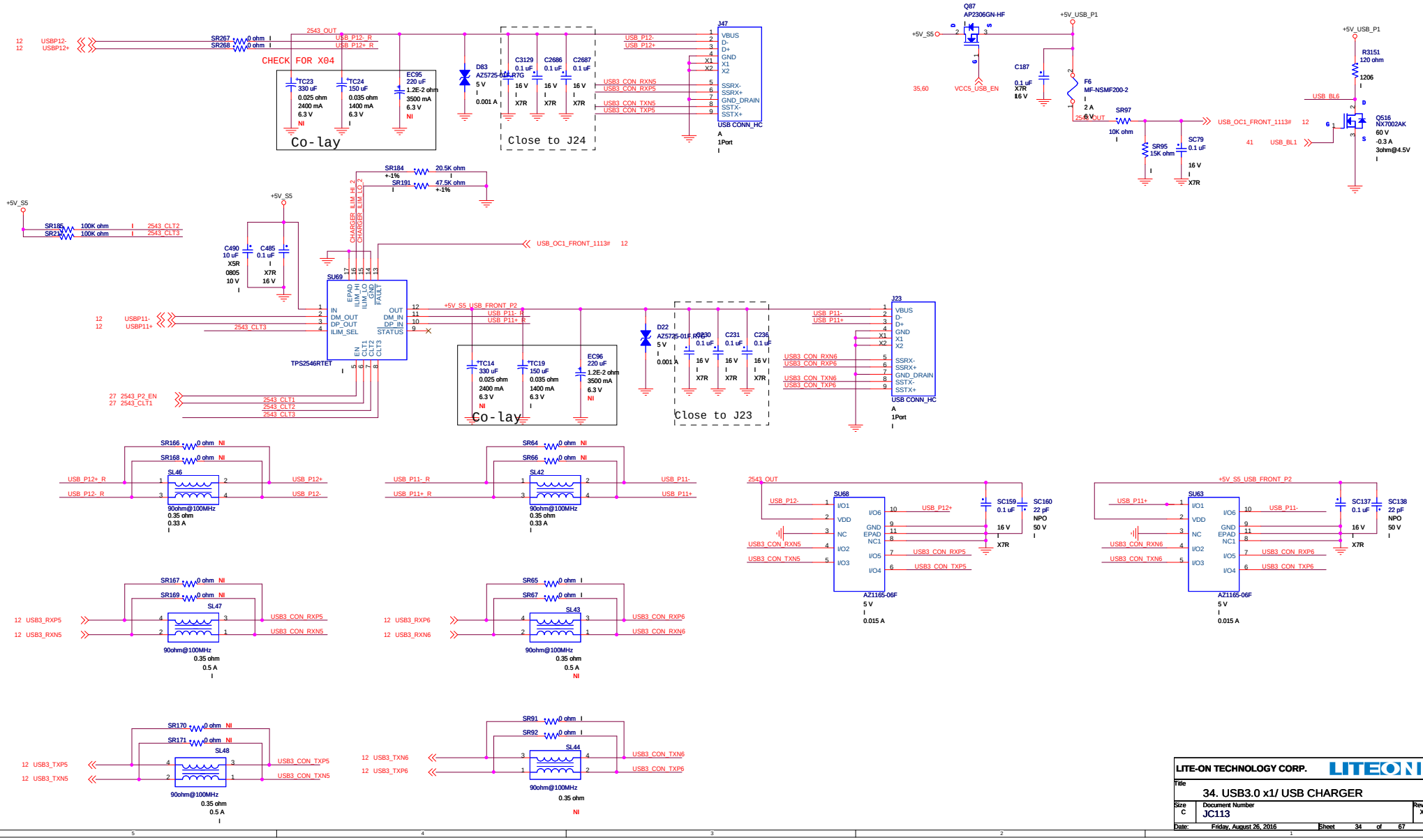
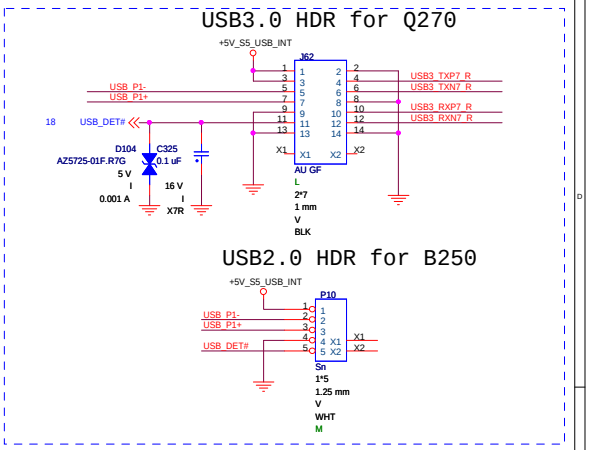
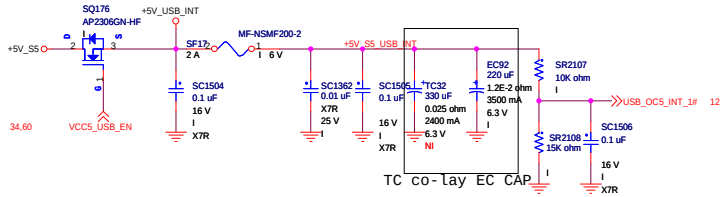
FRONT USB3.0 Charger x 2

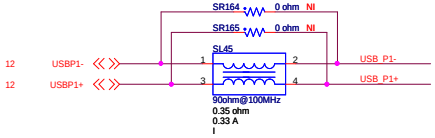
ILIM_HI	20.5K	2.5A	DCP	Tiny S3/S4/S5
			CDP	Tiny S0
ILIM_LO	47.5K	1.1A	SDP	Tiny not support

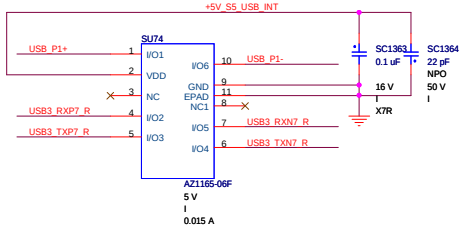
CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
						off
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	I_{OS_PW} & ILIM_HI (1)	DCP load present (2)
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present (3)
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP (4)	ILIM_LO	off
1	1	1	1	CDP (4)	ILIM_HI	CDP load present (3)

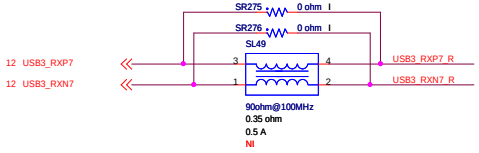


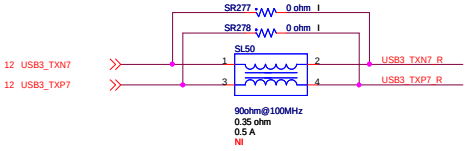










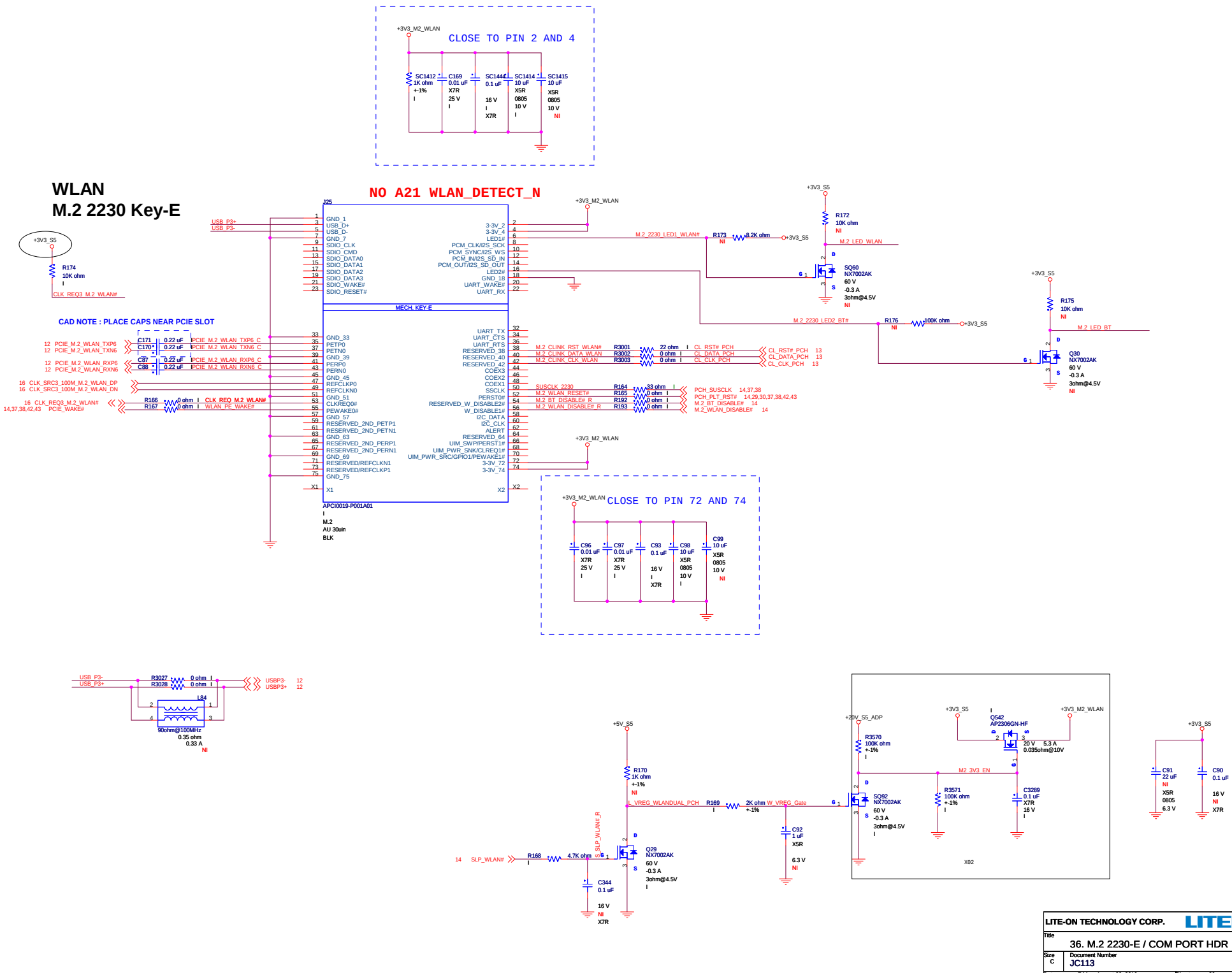


LITE-ON TECHNOLOGY CORP.		
Title: 35. INT USB3.0		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 35 of 67	

WLAN
M.2 2230 Key-E

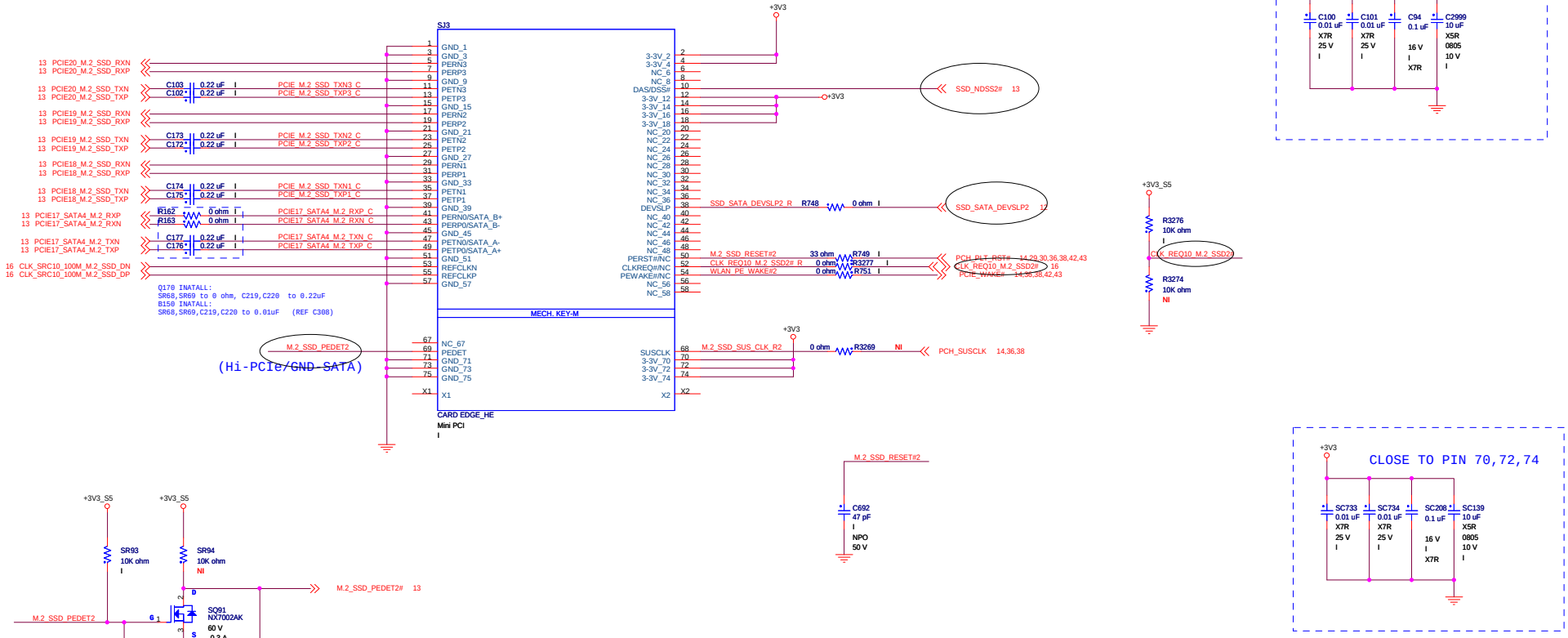
NO A21 WLAN_DETECT_N

CAD NOTE : PLACE CAPS NEAR PCIE SLOT



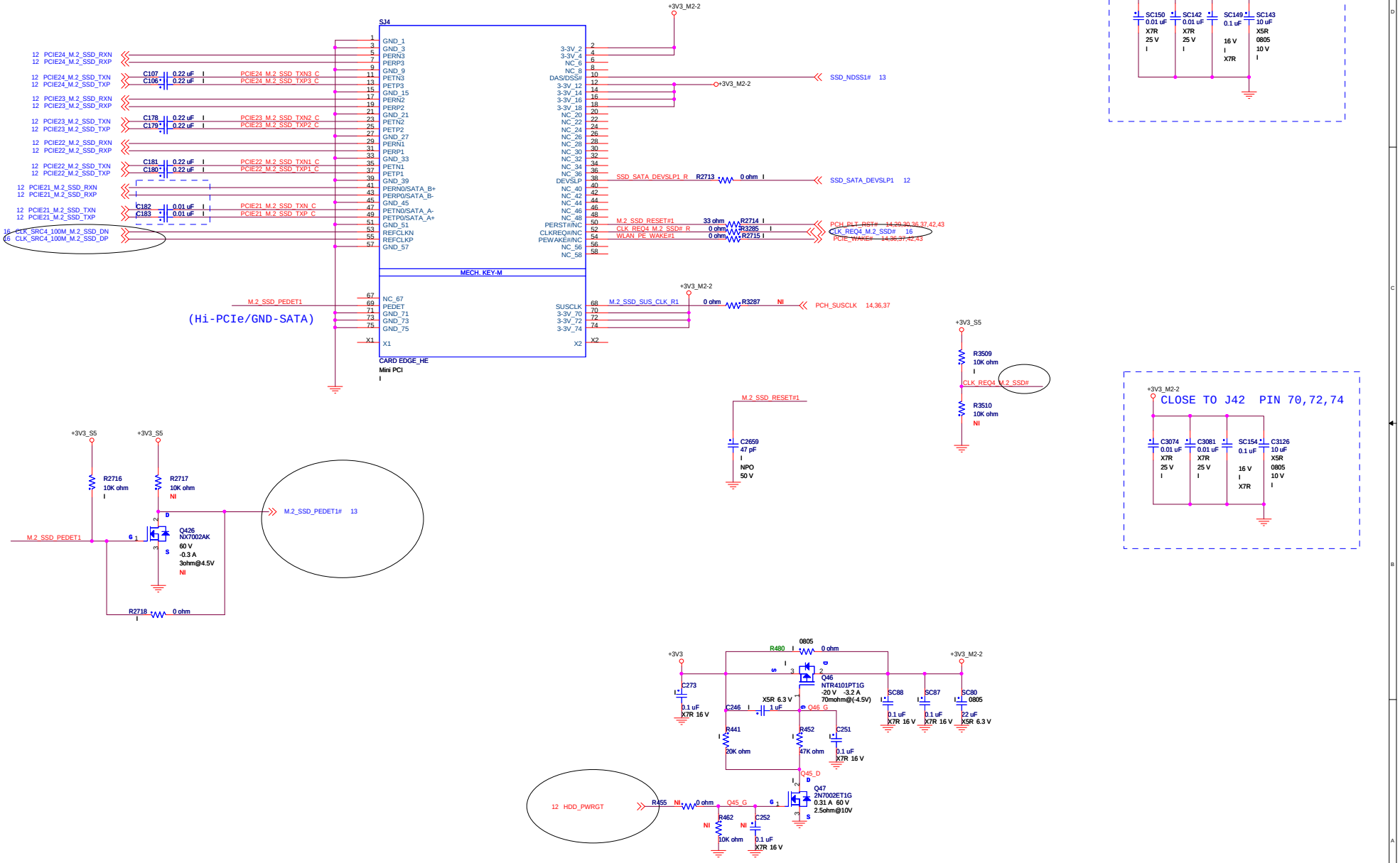
LITE-ON TECHNOLOGY CORP.	LITEON
Title	36. M.2 2230-E / COM PORT HDR
Size C	Document Number JC113
Rev	X03
Date:	Friday, August 26, 2016
Sheet	36 of 67

SSD Card
M.2 2280 Key-M

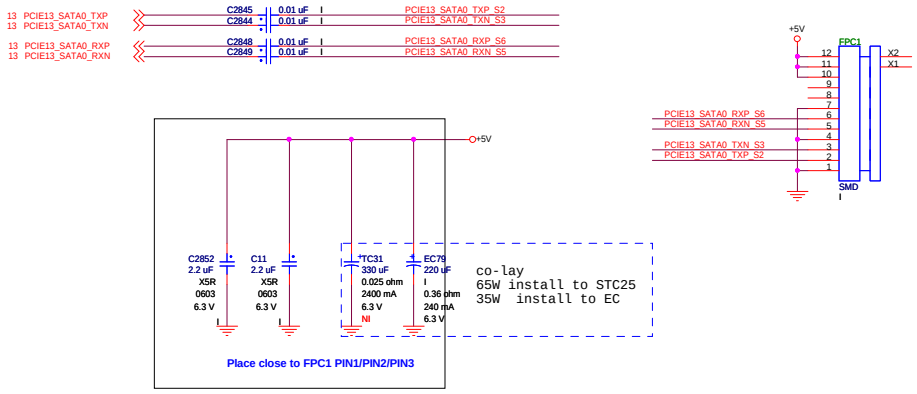


LITE-ON TECHNOLOGY CORP.		
Title: 37. M.2 2280-M		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 37 of 67	

SSD Card
M.2 2280 Key-M



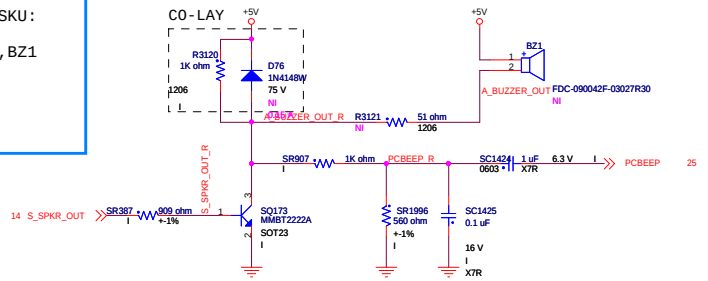
LITE-ON TECHNOLOGY CORP.			
Title: 38. M.2 2280-M			
Size: C	Document Number: JC113		Rev: X03
Date: Friday, August 26, 2016	Sheet 38 of 67		



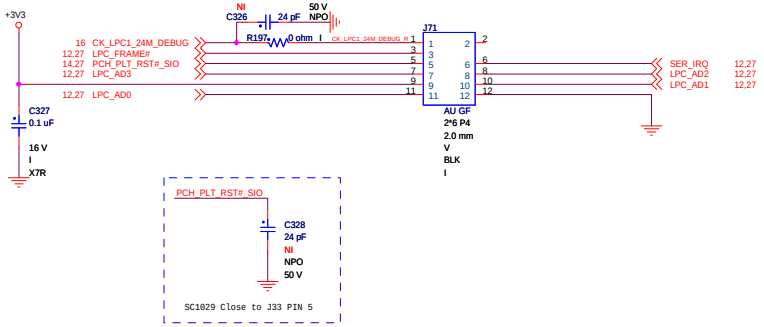
CAD NOTE : PLACE ALL CAPS WITHIN 0.5 INCH OF CONNECTOR

For Google SKU:
Install
SD14 ,SR906,BZ1

Remove
SR905



Debug port



LITE-ON TECHNOLOGY CORP.		
Title: 39. Buzzer/SATA/Debug Port		
Size: C	Document Number: JC113	Rev: X03
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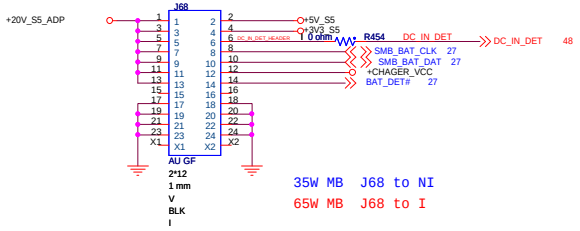
BATTERY/INT PSU Header

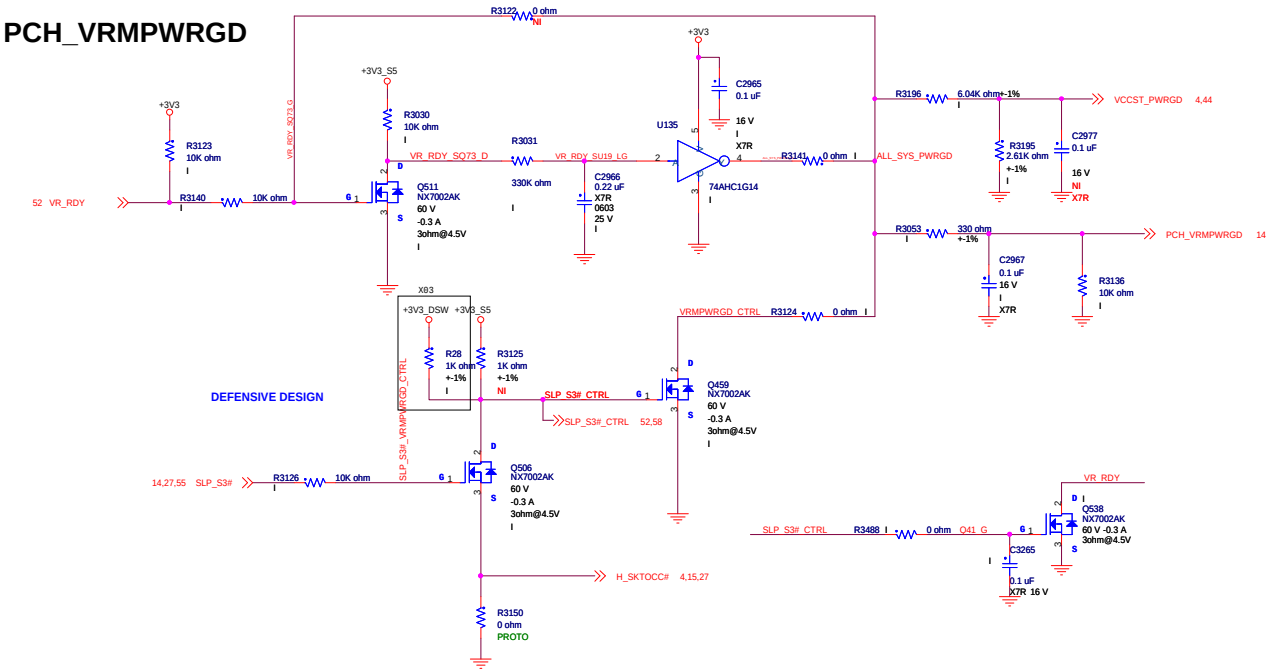


35W MB J68 to NI

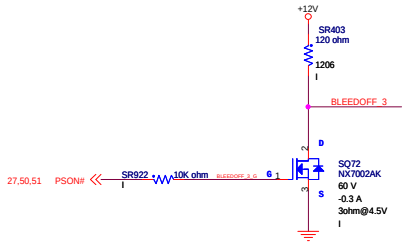
65W MB J68 to I

LITE-ON TECHNOLOGY CORP.		
Title: 40. BATTERY HEADER		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 40 of 67	

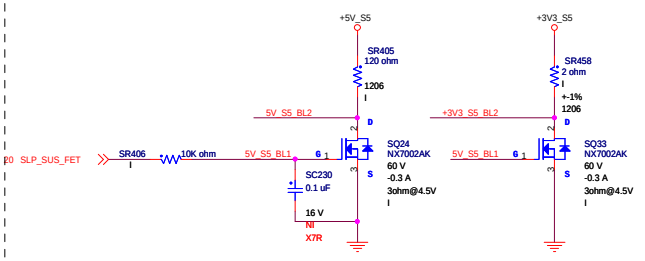
PCH_VRMPWRGD



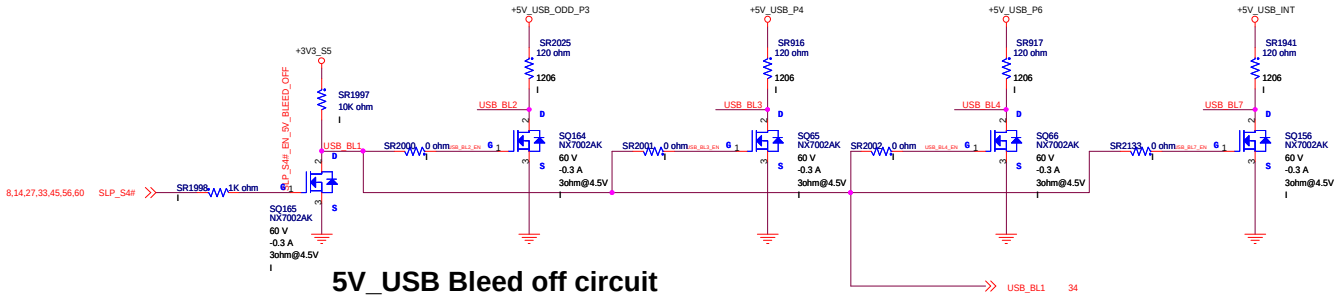
+12V Bleed off circuit



5V_S5 and 3V_S5 Bleed off circuit

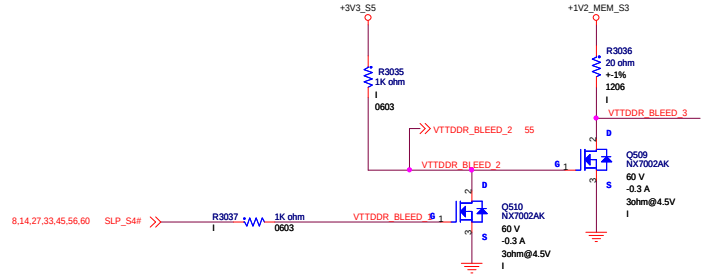


5V_USB Bleed off circuit

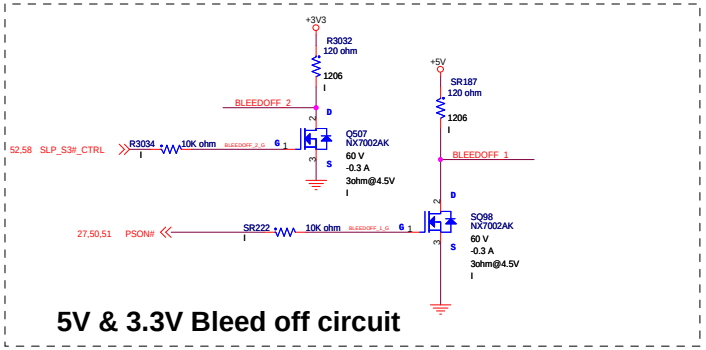


DESIGN NOTE:THESE CIRCUITS ARE USED TO BLEED OFF 1.5V DDR

+1V2_MEM Bleed off circuit



5V & 3.3V Bleed off circuit



LITE-ON TECHNOLOGY CORP.

Title: 41. PWRGD & BLEED OFF

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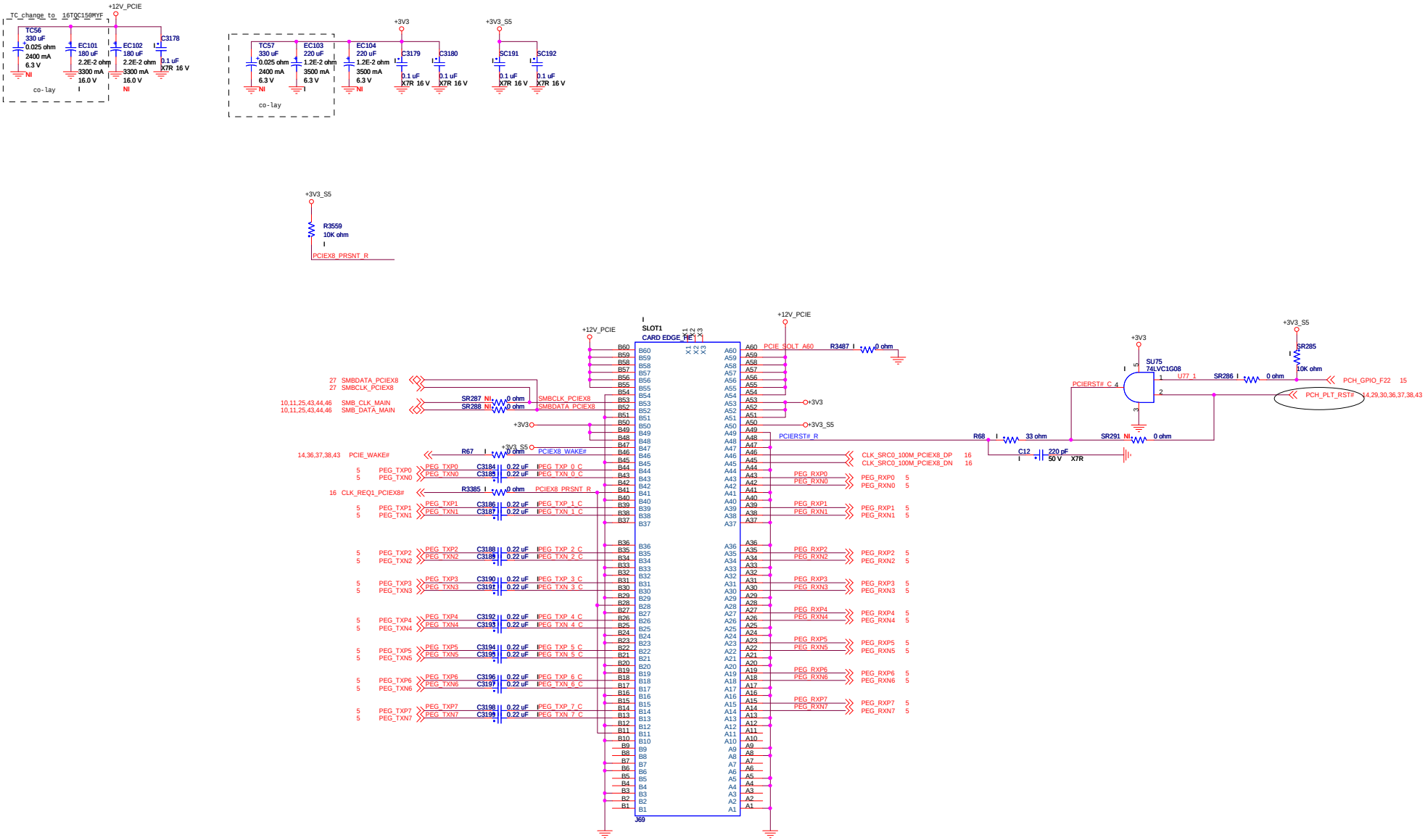

LITE-ON TECHNOLOGY CORP.		
Title	42. PCIEX8	
Size C	Document Number JC113	Rev X03
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LITE-ON TECHNOLOGY CORP.

Title

43. PCIEX8

Size	Document Number	Rev
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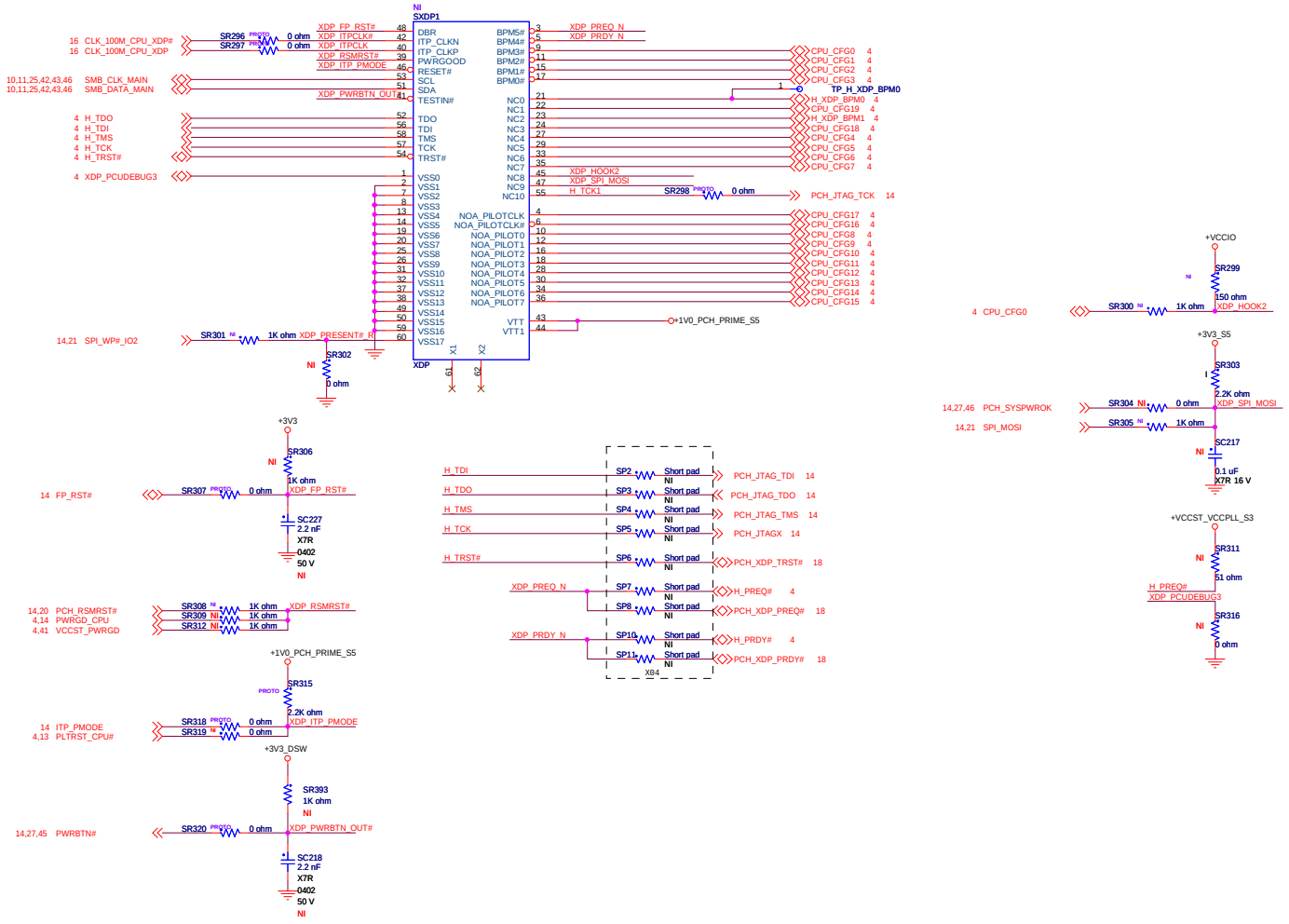
Intel XDP Debugging Connector



LITE-ON TECHNOLOGY CORP.			
Title: 44. XDP			
Size: C	Document Number: JC113		Rev: X03
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CONTROL PANEL / LED CIRCUITRY

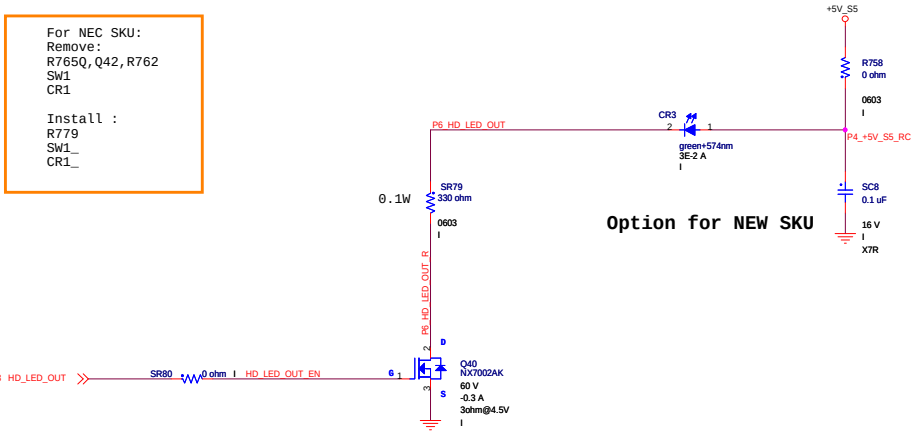
POWER BUTTON & LED

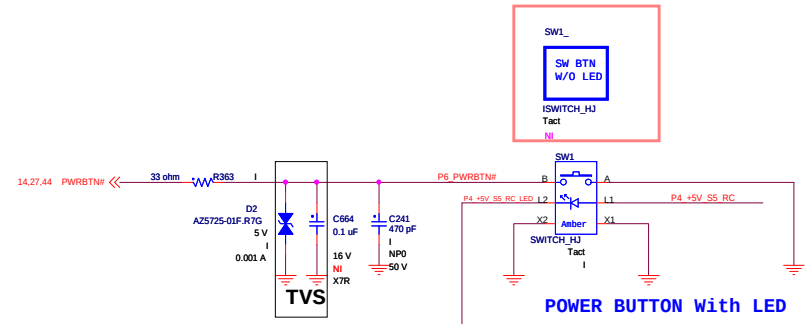
Color	Functoin
G	HDD

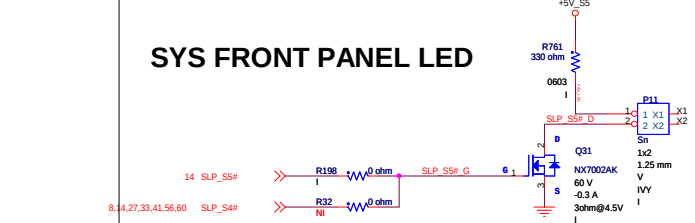
For NEC SKU:
Remove:
R765Q,Q42,R762
SW1
CR1

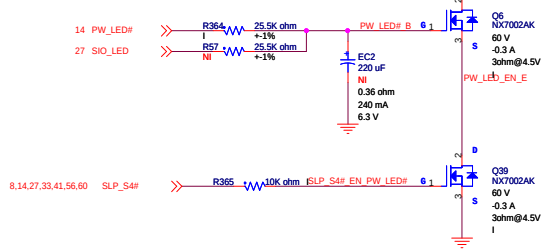
Install :
R779
SW1_
CR1_

Id = 25mA @ 2.8V (SPEC)
Id = (5V-2.8V) / 330ohm = 5mA
5m * 3.2 V = 16 mW
0.1W (For Current limit R)

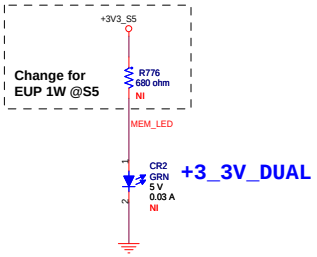


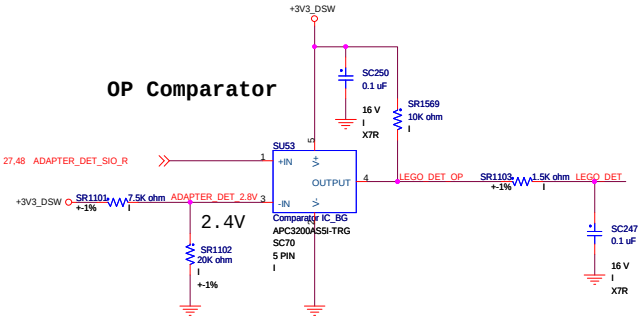


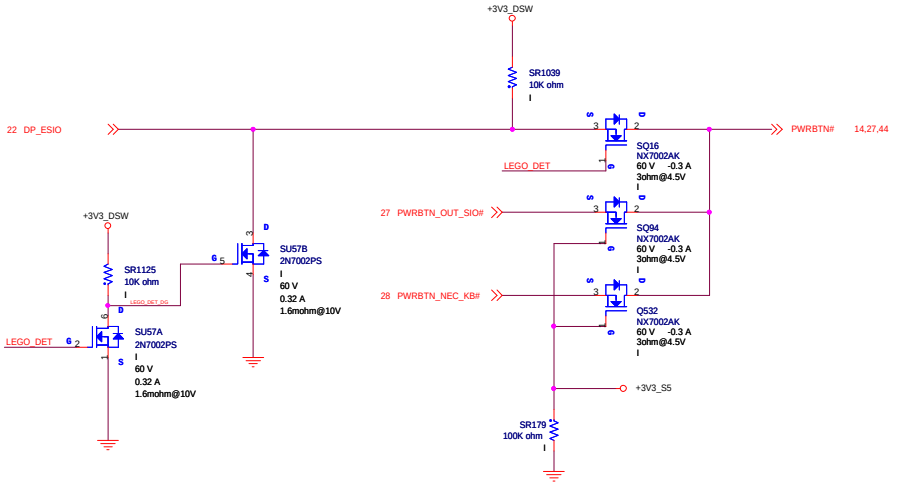




PCA LED CIRCUITS







LITE-ON TECHNOLOGY CORP.

Title: 45. Button/LED

Size: C | Document Number: JC113 | Rev: X03

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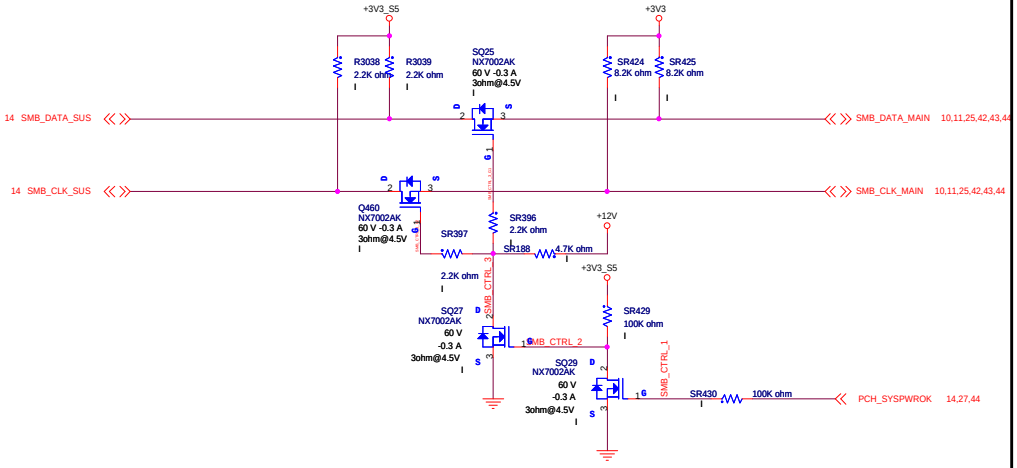
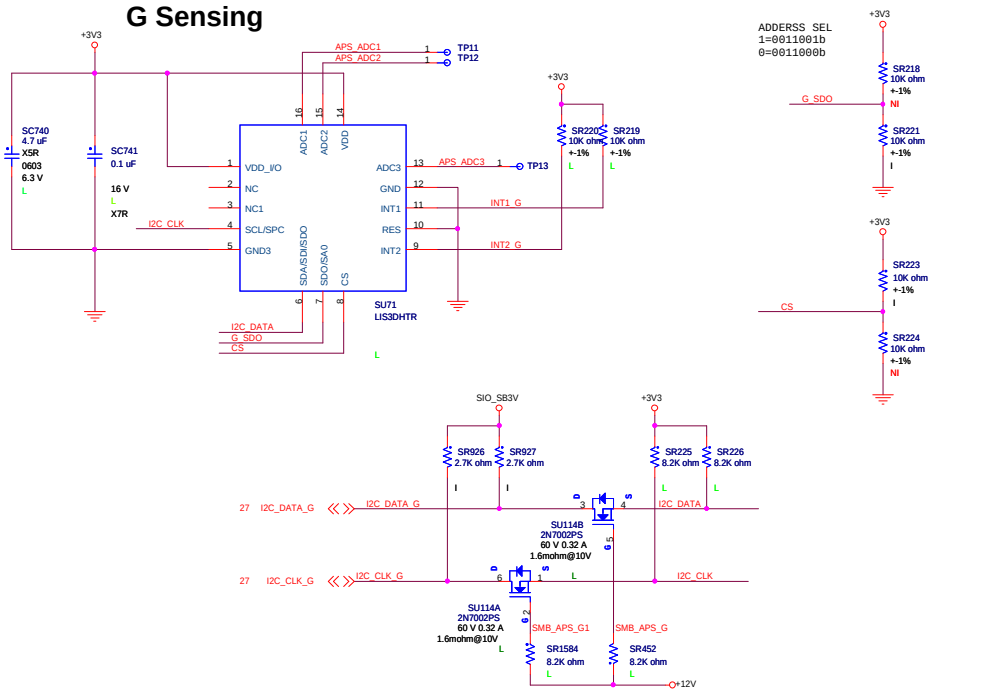
SM Bus



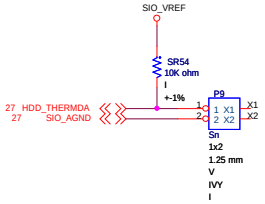
G Sensing

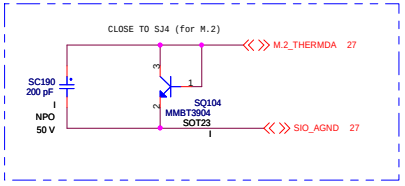


Temperature Sensing

Current Mode

CAD NOTE : Place MLCC Close to Thermal Diode





Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconsuctor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

LITE-ON TECHNOLOGY CORP.		
Title: 46. SM BUS/Thermal Sensing/APS		
Size: C	Document Number: JC113	Rev: X03
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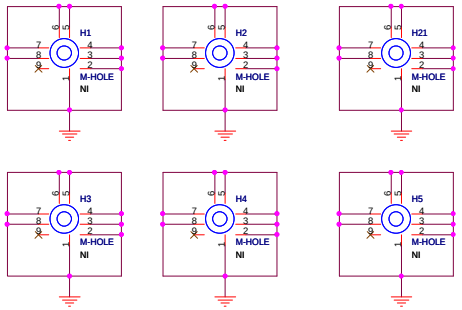
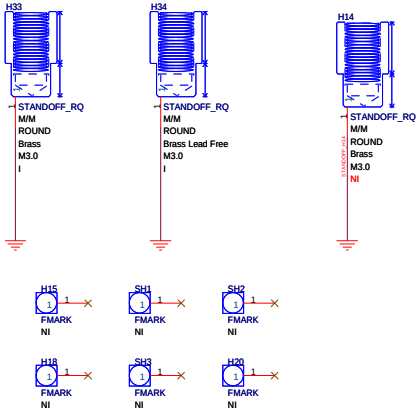
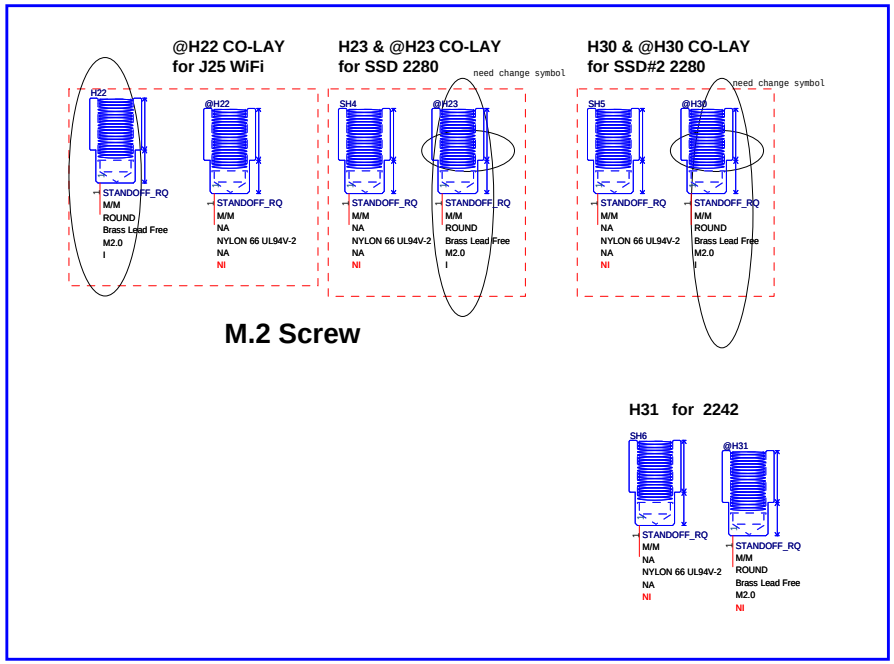
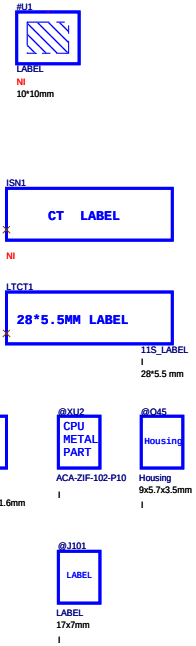


CPU HEATSINK_HOLE







LITE-ON TECHNOLOGY CORP.

Title: 47. Mounting Hole / PCB / Stand Off

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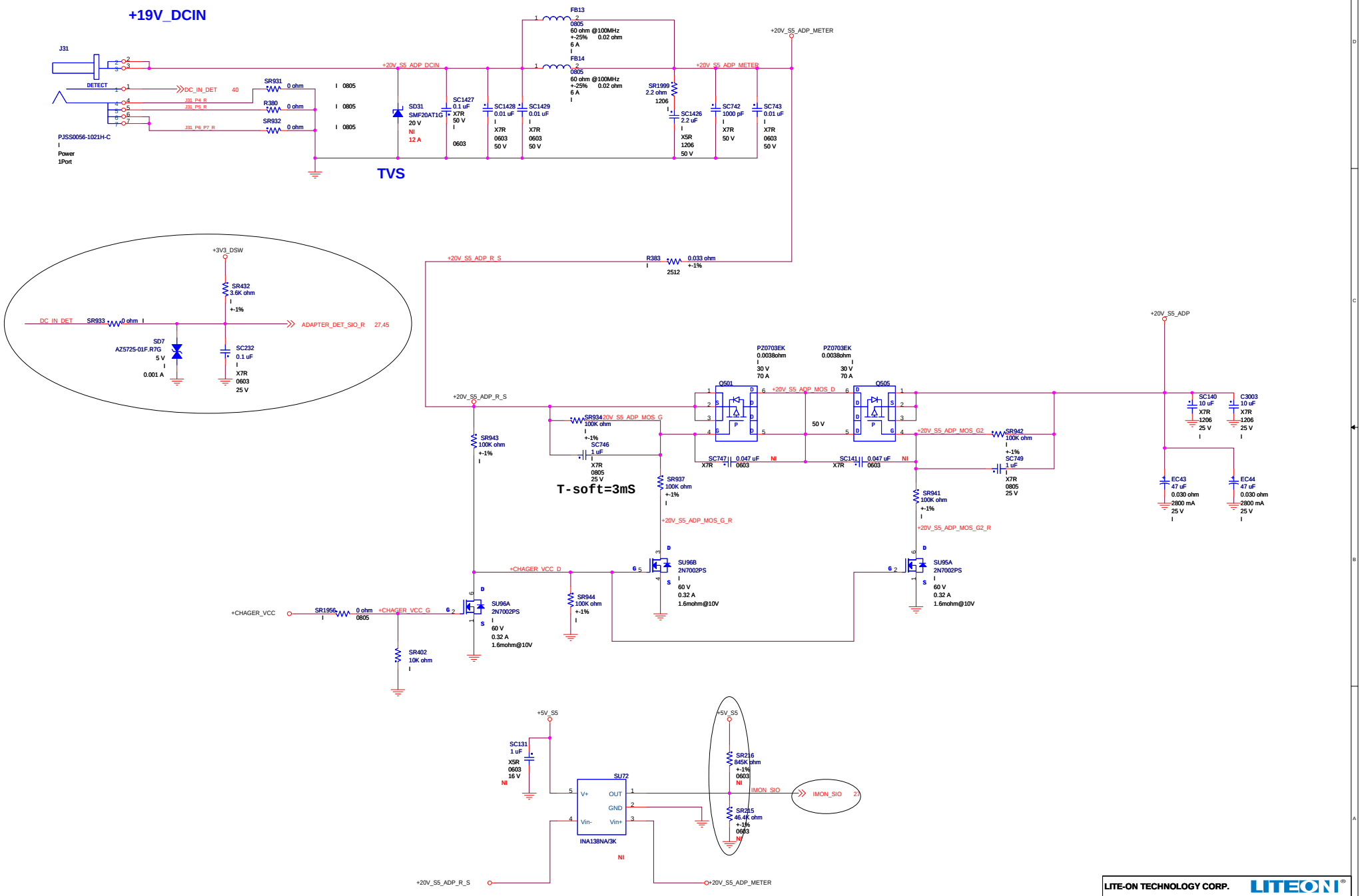


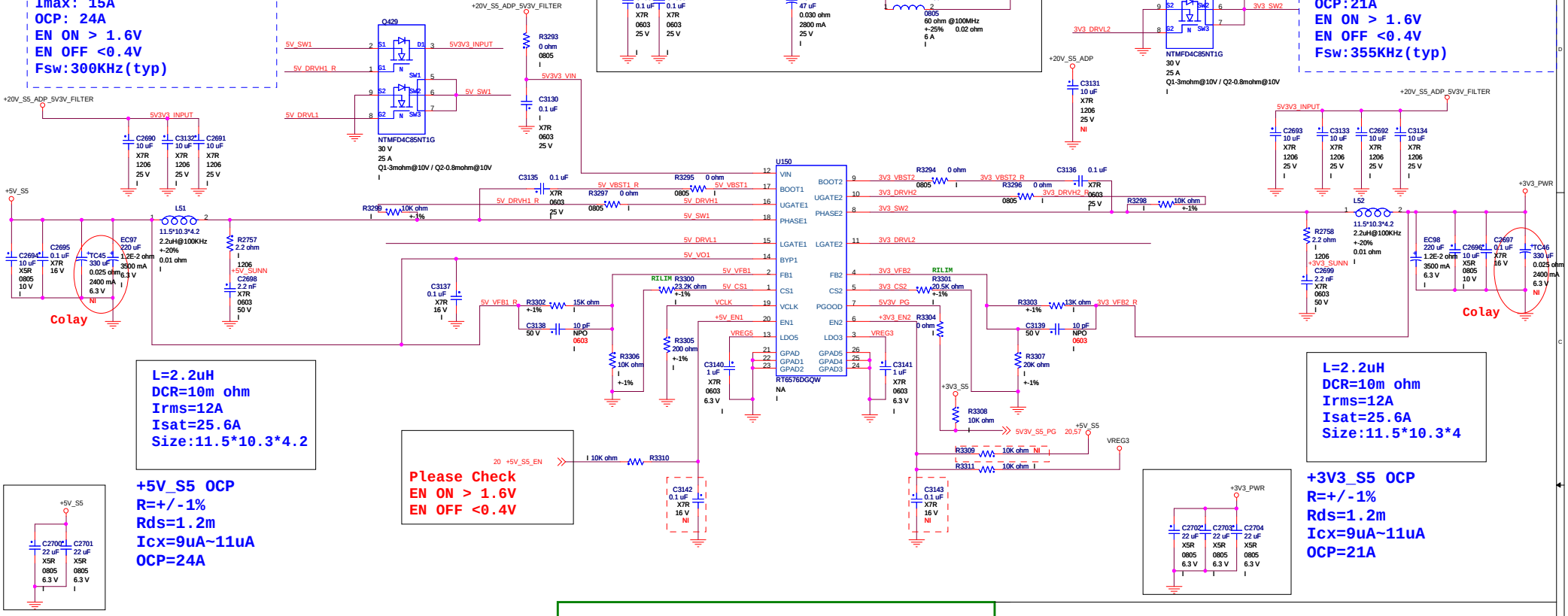
LITE-ON TECHNOLOGY CORP.		
Title: 48.+20V_S5_ADP		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 48 of 67	

+5V_S5

Vin:+20V_S5_ADP_5V3V_FILTER
Vout:+5V
Imax: 15A
OCP: 24A
EN ON > 1.6V
EN OFF <0.4V
Fsw:300KHz(typ)

+3V3_PWR

Vin:+20V_S5_ADP_5V3V_FILTER
Vout:+3V3_S5
Imax:13A
OCP:21A
EN ON > 1.6V
EN OFF <0.4V
Fsw:355KHz(typ)



L=2.2uH
DCR=10m ohm
Irms=12A
Isat=25.6A
Size:11.5*10.3*4.2

L=2.2uH
DCR=10m ohm
Irms=12A
Isat=25.6A
Size:11.5*10.3*4

Please Check
EN ON > 1.6V
EN OFF <0.4V

+5V_S5 OCP
R=+/-1%
Rds=1.2m
Icx=9uA~11uA
OCP=24A

+3V3_S5 OCP
R=+/-1%
Rds=1.2m
Icx=9uA~11uA
OCP=21A

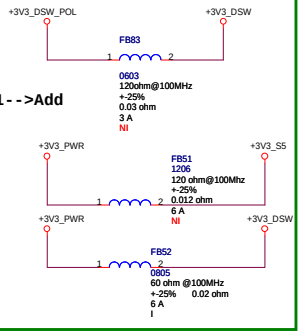
OCP
+3V3_S5
Rlimit=Ilimit*Ron*8/10uA=20.16K
+5V_S5
Rlimit=Ilimit*Ron*8/10uA=23.04K
Ron=1.2m Icx=10uA R=+/-1%

+3V3_S5
ΔIL /2=5.43/2=1.79

+5V_S5
ΔIL /2=5.68/2=2.84

使用RT6576 (+3V3_DSW)
1.SFB17-->NI
2.FB40->NI
3.SR956-->NI
4.SR1516;SR1573,SQ101;FB41-->Add

使用RT8296A (+3V3_DSW)
1.SR1516-->NI
2.FB41-->NI
3.SR1573->NI
4.SQ101-->NI
5.SR1573-->NI

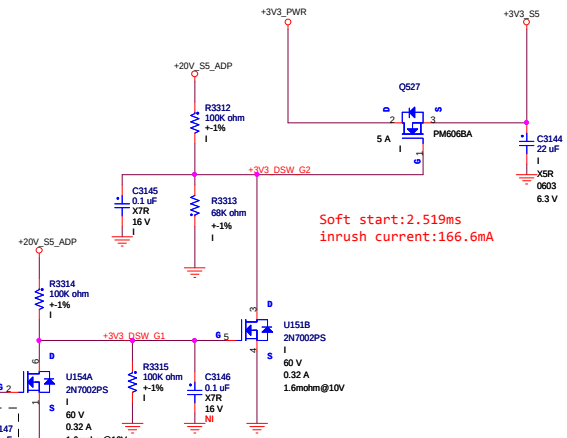


Cin=117uF
ripple current:13.3A

+5V_S5:
Cout=220uF
ripple current:3.5A

+3V3_S5:
Cout=220uF
ripple current:3.5A

+3V3_S5



Soft start:2.519ms
inrush current:166.6mA

LITE-ON TECHNOLOGY CORP.		
Title	49.+5V_S5/+3V3_S5	
Size C	Document Number JC113	Rev X03
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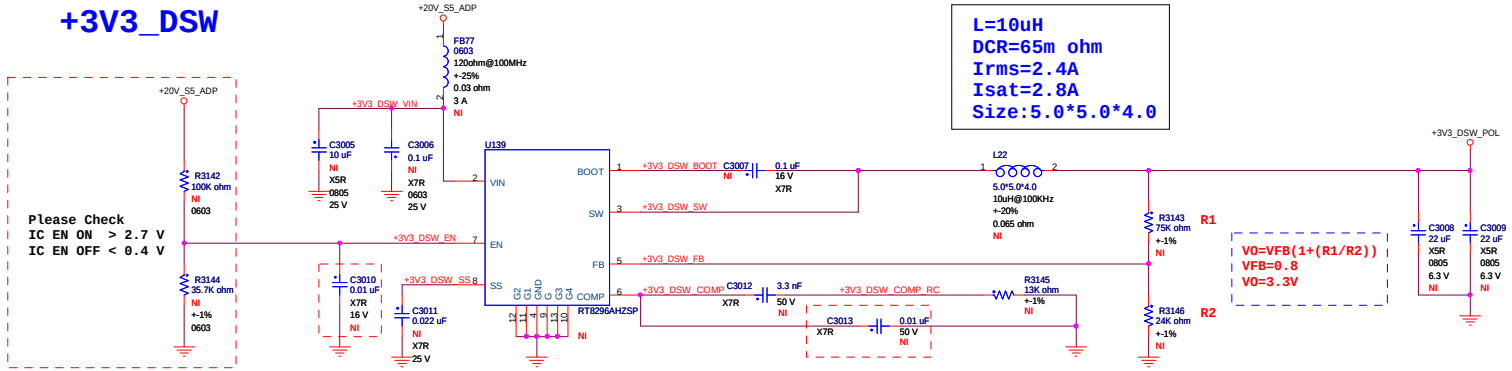
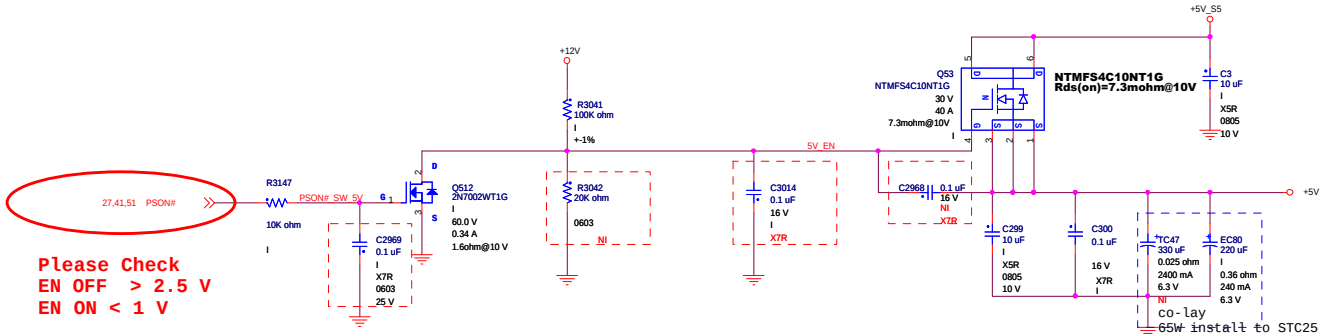
+3V3_DSW



+3V3_DSW_POL
Temp. Max. DC: 0.3A
OCP: 5.1A
IC EN ON > 2.7V
IC EN OFF <0.4V

L=10uH
DCR=65m ohm
Irms=2.4A
Isat=2.8A
Size:5.0*5.0*4.0

+5V

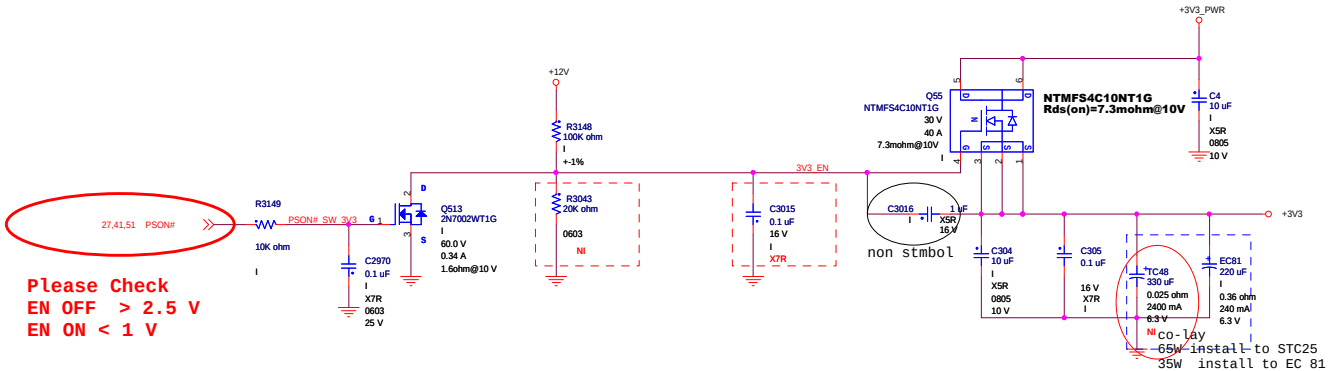


Please Check
EN OFF > 2.5 V
EN ON < 1 V

+5V @Imax 6.94A

SOFT-START
+5V: 5.835mS
+3V3: 3.449mS

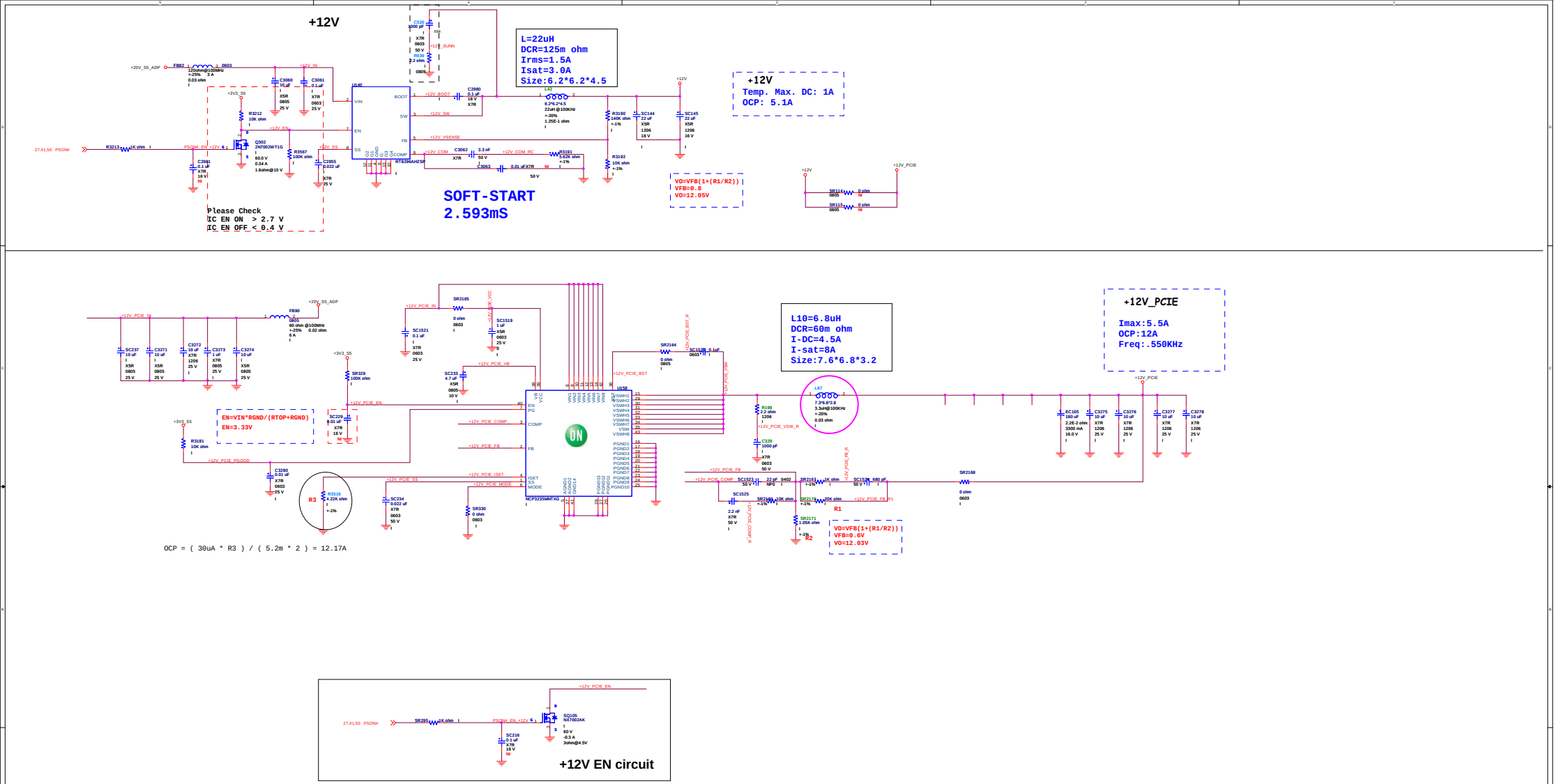
+3V3



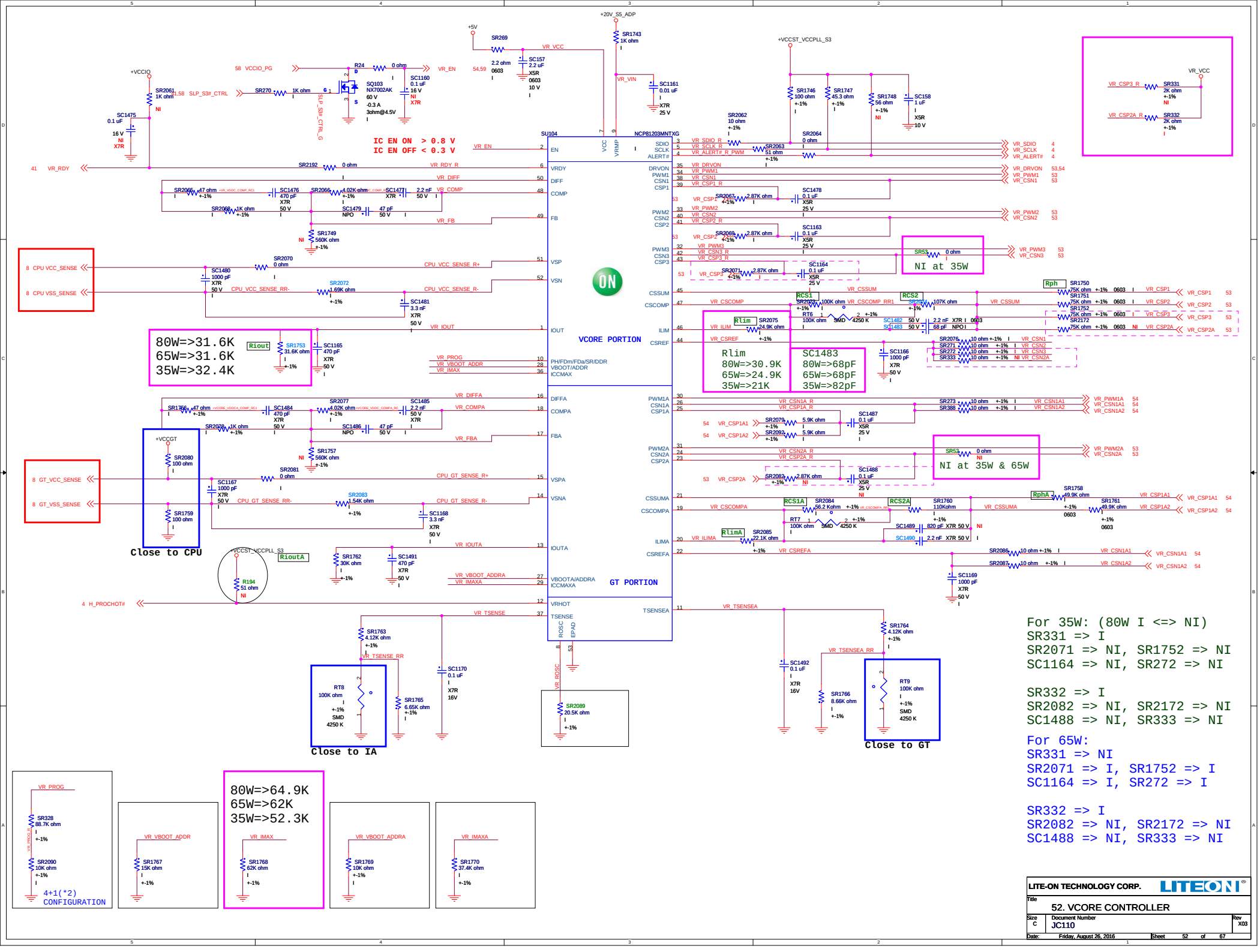
Please Check
EN OFF > 2.5 V
EN ON < 1 V

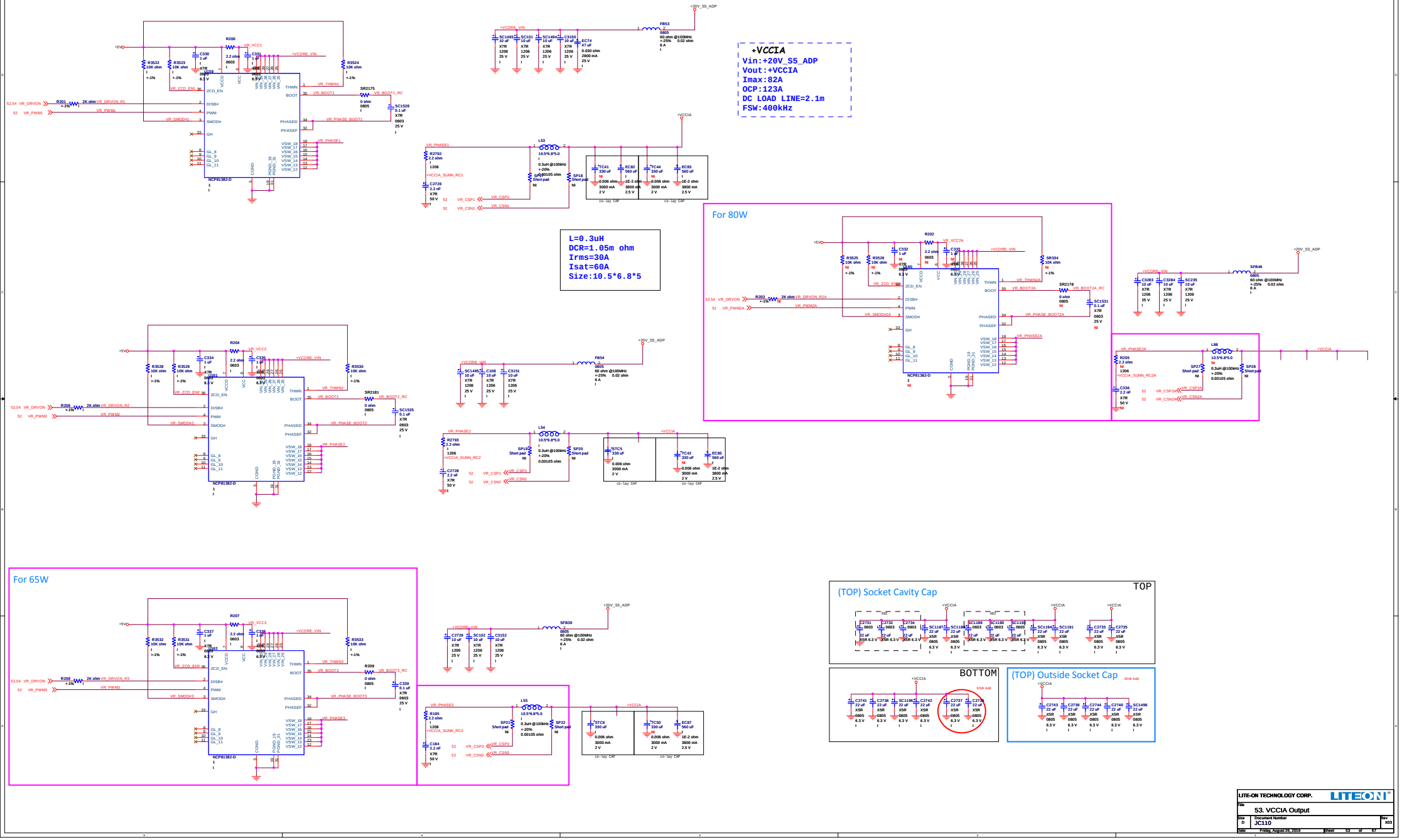
+3V3 @Imax 6.74A

LITE-ON TECHNOLOGY CORP.		
Title: 50. +3V3_DSW/+5V/+3V3		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 50 of 67	

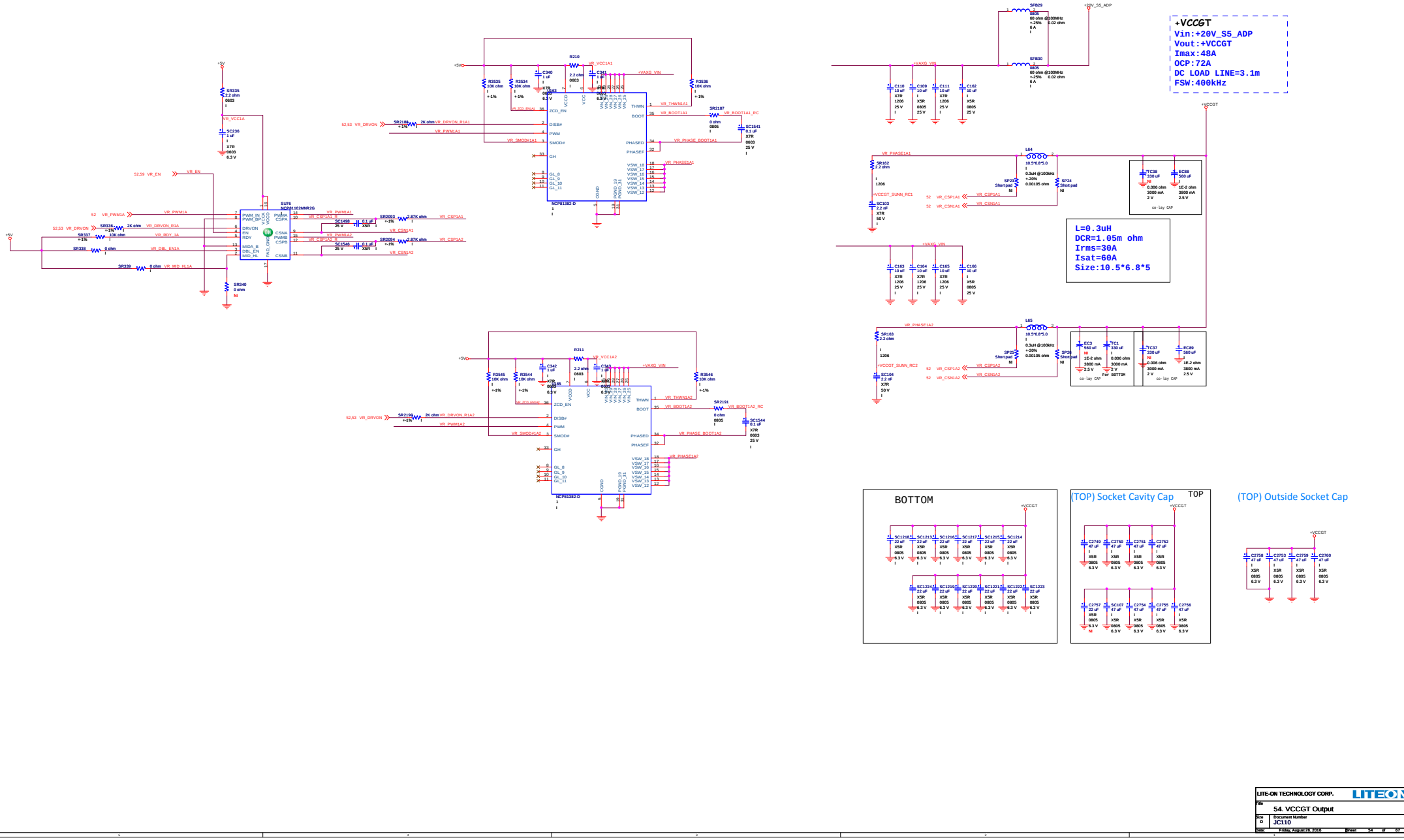


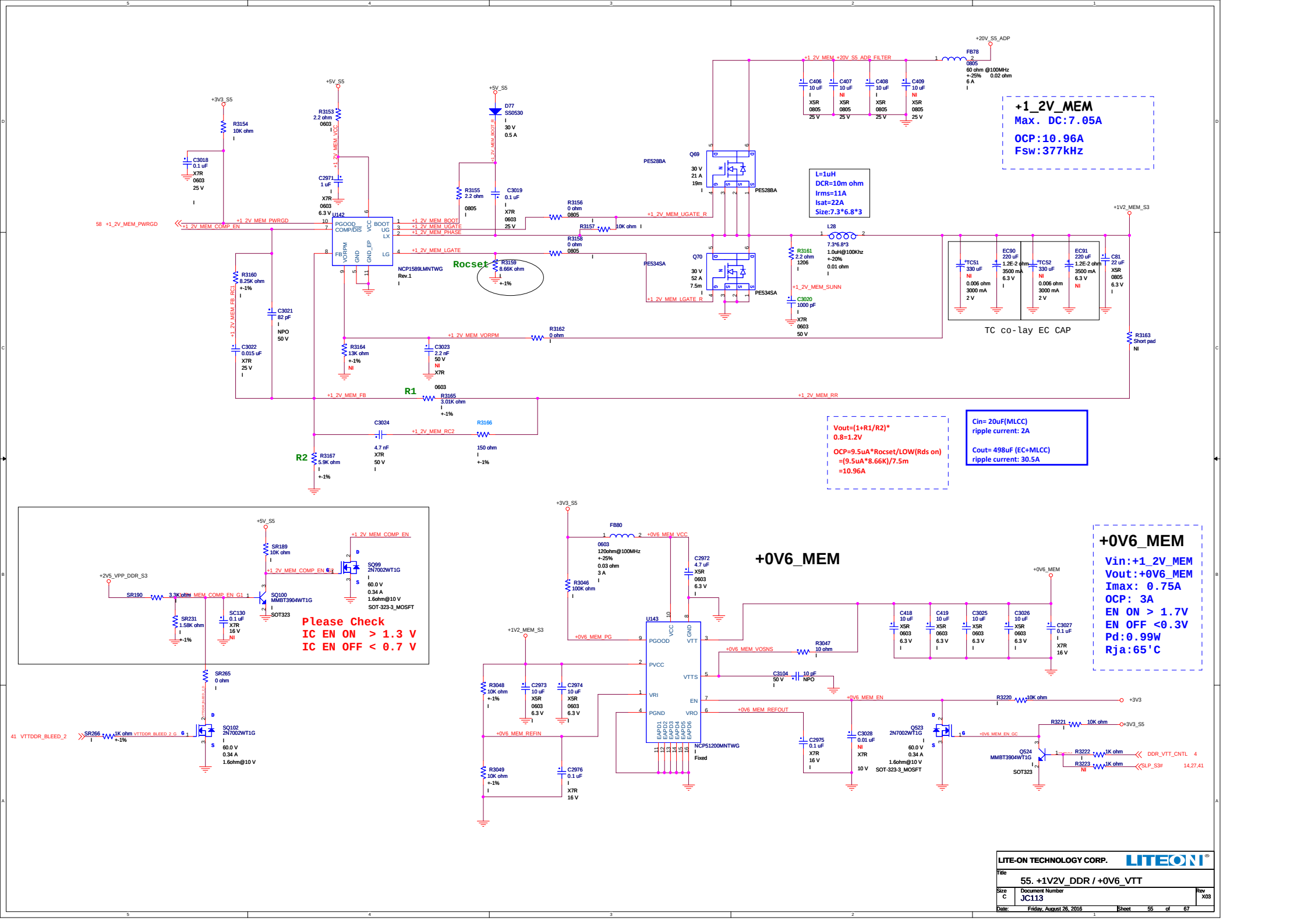
LITE-ON TECHNOLOGY CORP.			
Title: 51. +12V			
Size: D	Document Number: JC113		Rev: X03
Date: Friday, August 26, 2016	Sheet: 51	of: 67	


IC EN ON > 0.8 V
IC EN OFF < 0.3 V
SU104
NCP81203MNTXG
VCORE PORTION
GT PORTION
ON
NI at 35W
NI at 35W & 65W
80W=>31.6K
65W=>31.6K
35W=>32.4K
Riout
Rlim
80W=>30.9K
65W=>24.9K
35W=>21K
SC1483
80W=>68pF
65W=>68pF
35W=>82pF
Close to CPU
Close to IA
Close to GT
RioutA
RlimA
RCS1
RCS2
RCS1A
RCS2A
Rph
RphA
80W=>64.9K
65W=>62K
35W=>52.3K
4+1(*2)
CONFIGURATION
For 35W: (80W I <=> NI)
SR331 => I
SR2071 => NI, SR1752 => NI
SC1164 => NI, SR272 => NI
SR332 => I
SR2082 => NI, SR2172 => NI
SC1488 => NI, SR333 => NI
For 65W:
SR331 => NI
SR2071 => I, SR1752 => I
SC1164 => I, SR272 => I
SR332 => I
SR2082 => NI, SR2172 => NI
SC1488 => NI, SR333 => NI
LITE-ON TECHNOLOGY CORP.
52. VCORE CONTROLLER
JC110
Friday, August 26, 2016
Sheet 52 of 67



LITE-ON TECHNOLOGY CORP.	LITEON
Title	53. VCCIA Output
Size: D	Document Number: JC110
Rev	X03
Date: Friday, August 28, 2015	Sheet 53 of 87


+VCCGT
Vin:+20V_S5_ADP
Vout:+VCCGT
Imax:48A
OCP:72A
DC LOAD LINE=3.1m
FSW:400kHz
L=0.3uH
DCR=1.05m ohm
Irms=30A
Isat=60A
Size:10.5*6.8*5
SU76
NCP81162MNR2G
NCP81382-D
BOTTOM
TOP
(TOP) Socket Cavity Cap
(TOP) Outside Socket Cap
LITE-ON TECHNOLOGY CORP.
54. VCCGT Output
JC110
Friday, August 26, 2016


+1_2V_MEM
Max. DC:7.05A
OCP:10.96A
Fsw:377kHz
L=1uH
DCR=10m ohm
Irms=11A
Isat=22A
Size:7.3*6.8*3
Rocset
Vout=(1+R1/R2)*
0.8=1.2V
OCP=9.5uA*Rocset/LOW(Rds on)
=(9.5uA*8.66K)/7.5m
=10.96A
Cin= 20uF(MLCC)
ripple current: 2A
Cout= 498uF (EC+MLCC)
ripple current: 30.5A
TC co-lay EC CAP
Please Check
IC EN ON > 1.3 V
IC EN OFF < 0.7 V
+0V6_MEM
Vin:+1_2V_MEM
Vout:+0V6_MEM
Imax: 0.75A
OCP: 3A
EN ON > 1.7V
EN OFF <0.3V
Pd:0.99W
Rja:65'C
LITE-ON TECHNOLOGY CORP.
55. +1V2V_DDR / +0V6_VTT
JC113
Friday, August 26, 2016

+2V5_VPP_DDR_S3

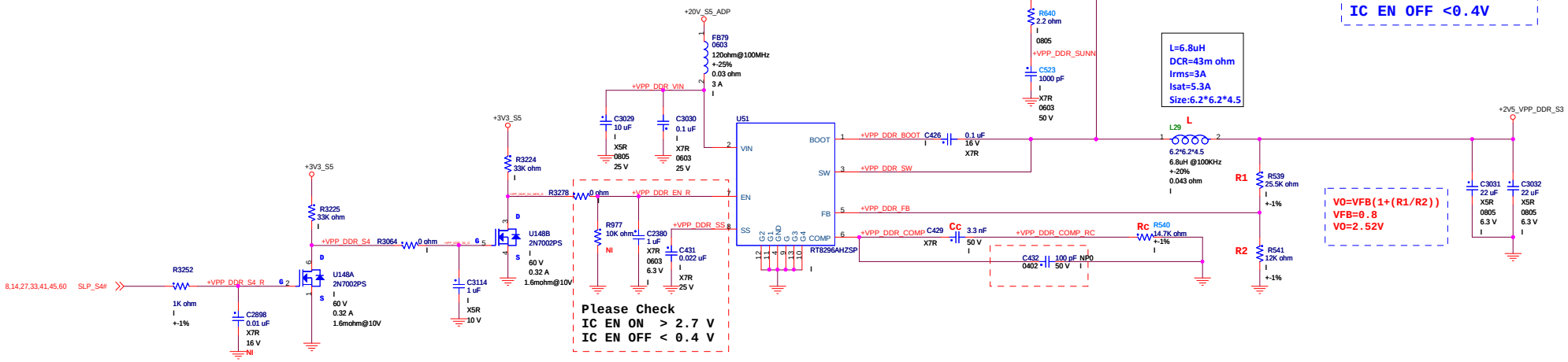
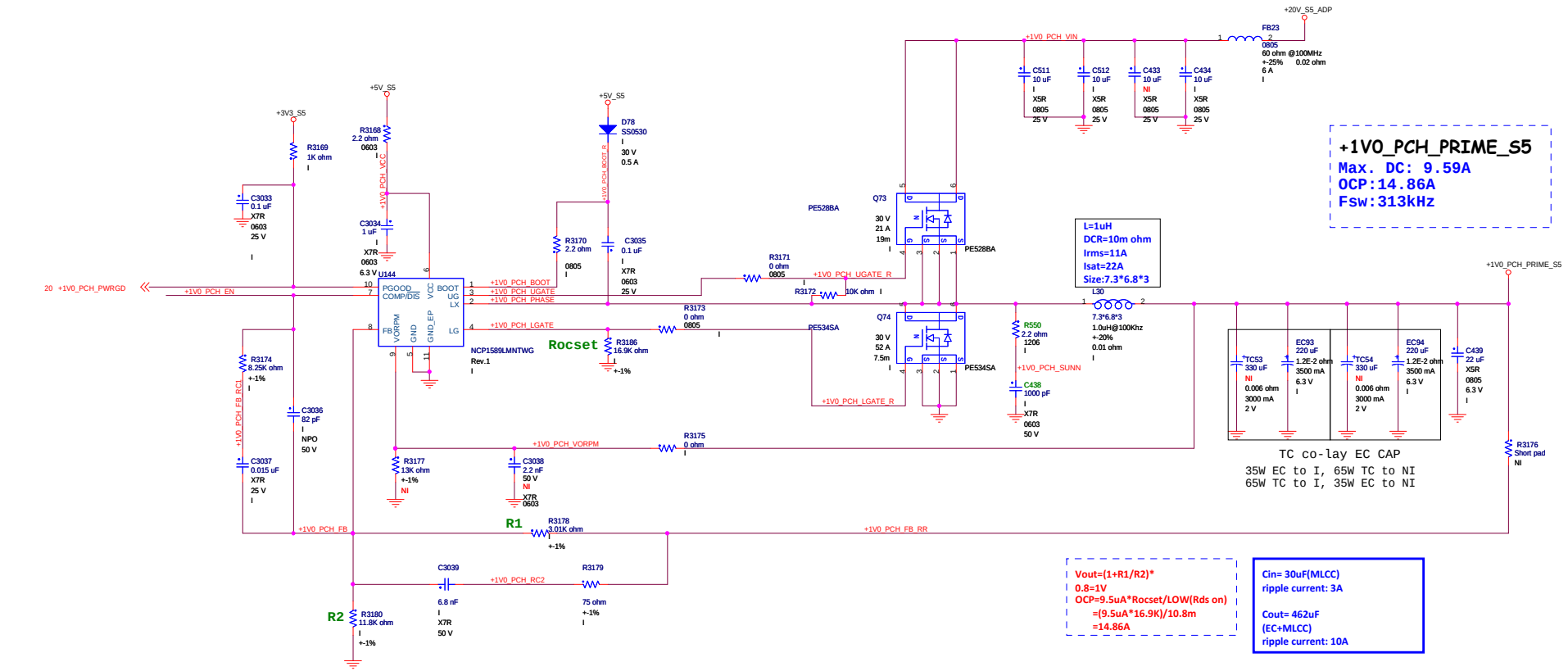


Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	C_C (nF)	L (µH)	C_{OUT} (µF)
8	27	3	33	3.3	22	22 x 2
5	62	11.8	20	3.3	15	22 x 2
3.3	75	24	13	3.3	10	22 x 2
2.5	25.5	12	9.1	3.3	6.8	22 x 2
1.5	10.5	12	5.6	3.3	3.6	22 x 2
1.2	12	24	4.3	3.3	3.6	22 x 2
1	3	12	3.6	3.3	2	22 x 2

LITE-ON TECHNOLOGY CORP.		
Title: 56. +2V5_VPP		
Size: C	Document Number: JC113	Rev: X03
Date: Friday, August 26, 2016	Sheet 56 of 67	



LITE-ON TECHNOLOGY CORP.	
Title	57. +1V0_PCH PRIME
Size C	Document Number JC113
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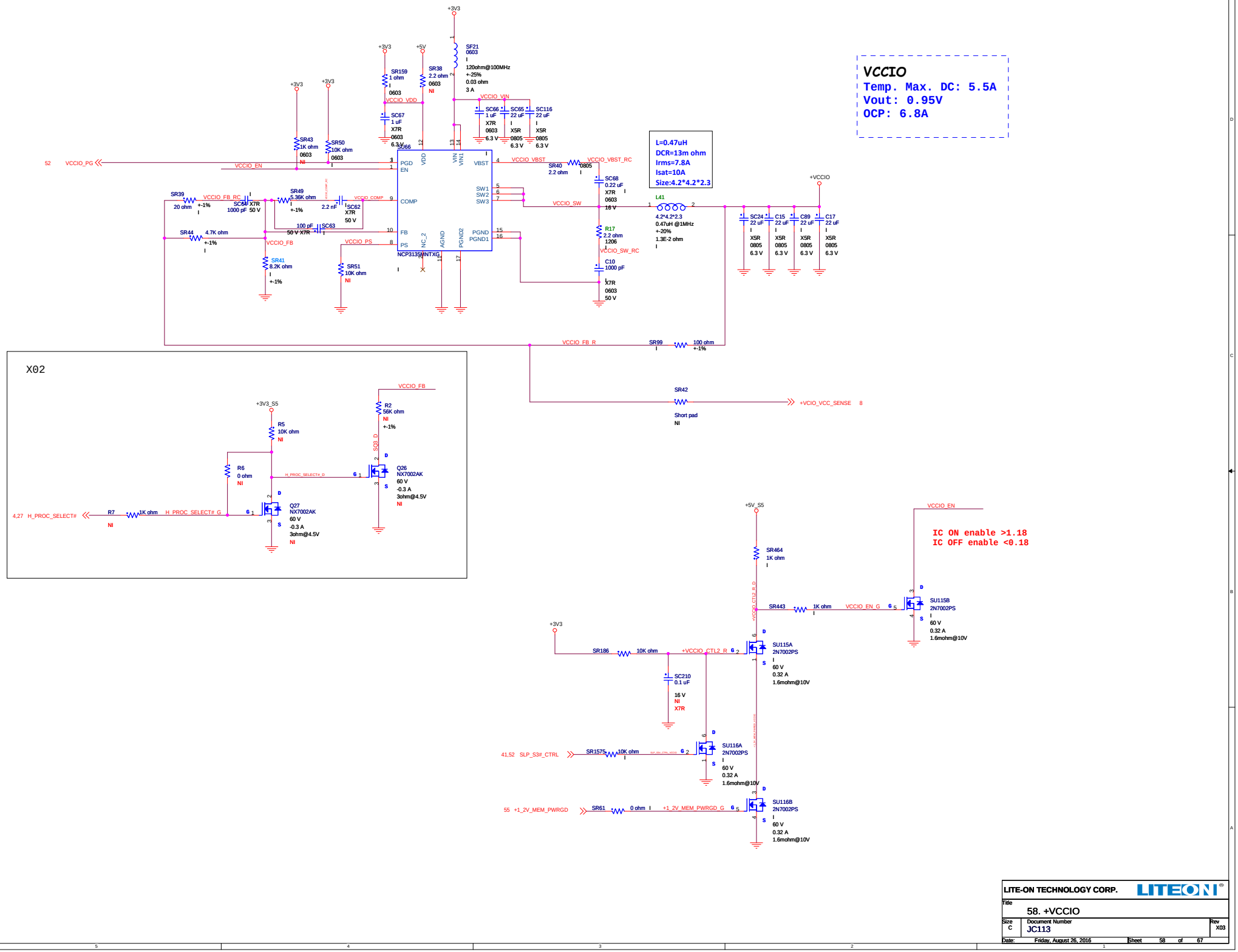
Date: Friday, August 26, 2016	Sheet 57 of 67



LITE-ON TECHNOLOGY CORP.			
Title: 58. +VCCIO			
Size: C	Document Number: JC113		Rev: X03
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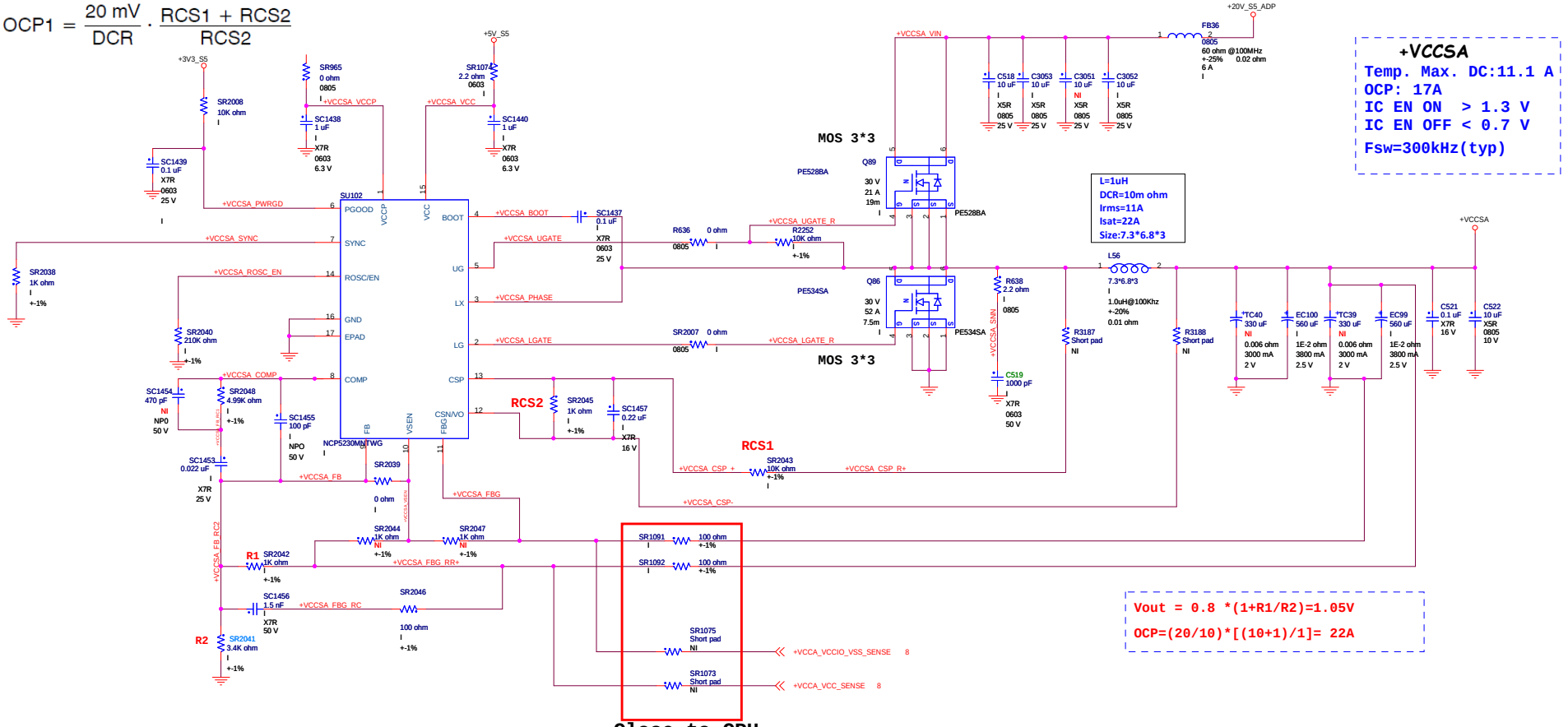
$$OCP1 = \frac{20\ mV}{DCR} \cdot \frac{RCS1 + RCS2}{RCS2}$$



LITE-ON TECHNOLOGY CORP.		
Title	59. +VCCSA	
Size C	Document Number JC110	Rev X03
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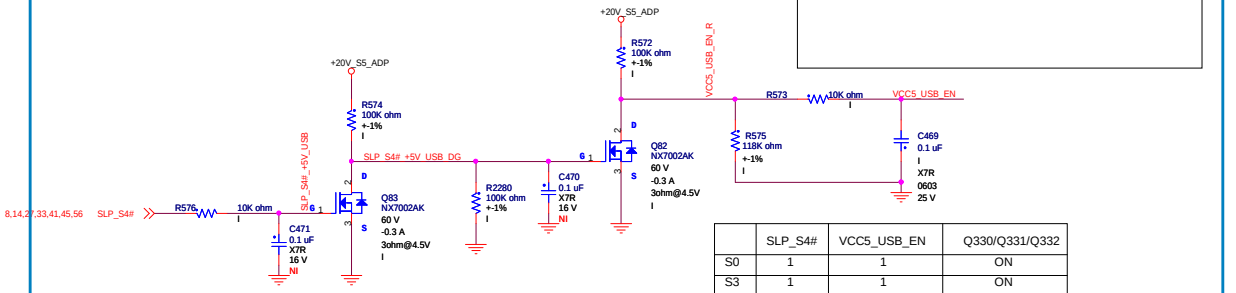
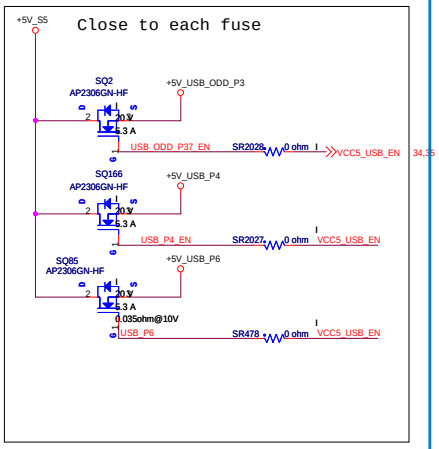
For Goolge SKU
Keep Q79 ,Q80 ,SQ85 then remove Others

+5V_USB





	SLP_S4#	VCC5_USB_EN	Q330/Q331/Q332
S0	1	1	ON
S3	1	1	ON
S4	0	0	OFF
S5	0	0	OFF

LITE-ON TECHNOLOGY CORP.			
Title: 60. +5V_USB			
Size: C	Document Number: JC113		Rev: X03
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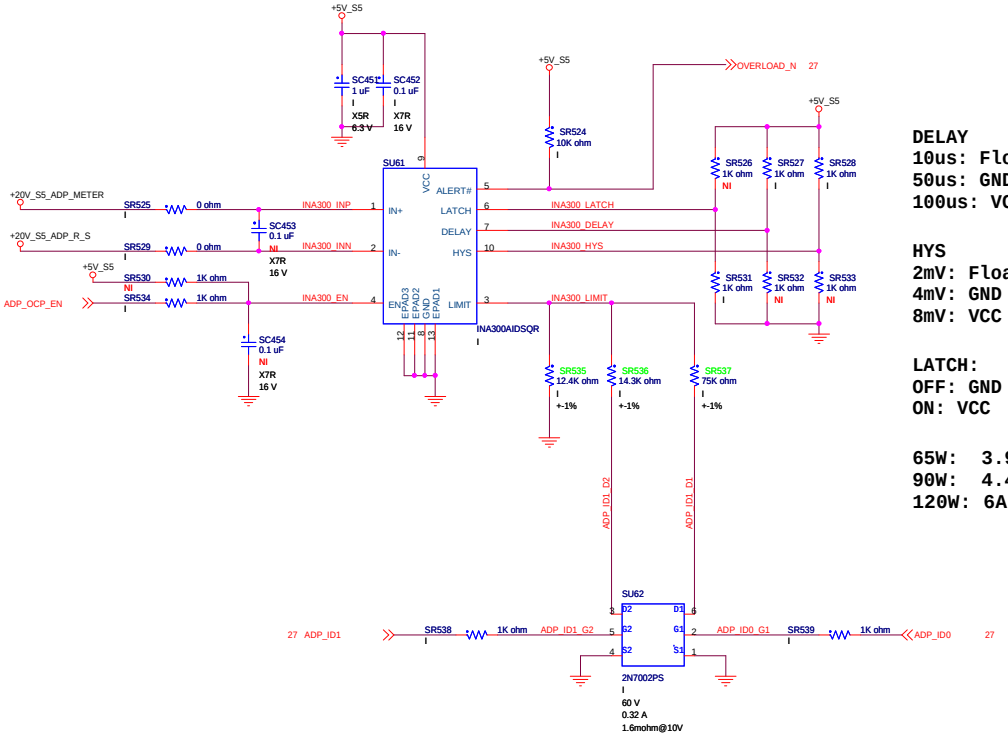
ADP_IN

ADP_OUT

>1.4V: Enable
<0.4V: Disable



DELAY
10us: Float
50us: GND
100us: VCC (default)

HYS
2mV: Float
4mV: GND
8mV: VCC (default)

LATCH:
OFF: GND (default)
ON: VCC

65W: 3.978A 啓動
90W: 4.495A 啓動
120W: 6A 啓動

ADP TYPE
ID1 ID0
0 0: 120W
0 1: 90W
1 0: 65W

LITE-ON TECHNOLOGY CORP.			
Title: 61. INA300			
Size: C	Document Number: JC113		Rev: X03
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GPIO	Signal Name	Power Well	In/Out	Tiny4 Usage	Tiny4 Note
GPP_A0	GPP_A0_RCIN_N_ESPI_ALERT1_N	SB3V	NATIVE	KBRST#	PU 10K +3V3
GPP_A1	GPP_A1_LAD0_ESPI_IO0	SB3V	NATIVE	LPC_AD0	
GPP_A2	GPP_A2_LAD1_ESPI_IO1	SB3V	NATIVE	LPC_AD1	
GPP_A3	GPP_A3_LAD2_ESPI_IO2	SB3V	NATIVE	LPC_AD2	
GPP_A4	GPP_A4_LAD3_ESPI_IO3	SB3V	NATIVE	LPC_AD3	
GPP_A5	GPP_A5_LFRAME_N_ESPI_CS_N	SB3V	NATIVE	LPC_FRAME#	PU 4.7K SIO_3VCC
GPP_A6	GPP_A6_SERIRQ	SB3V	NATIVE	SER_IRQ	PU 10K +3V3
GPP_A7	GPP_A7_PIRQA_N_ESPI_ALERT0_N	SB3V	NATIVE	LPC_DRQ0#	PU 10K +3V3
GPP_A8	GPP_A8_CLKRUN_N	SB3V	NATIVE	CLKRUN#	PU 8.2K(W) +3V3_S5
GPP_A9	GPP_A9_CLKOUT_LPC0_ESPI_CLK	SB3V	NATIVE	CK_LPC0_24M_R	
GPP_A10	GPP_A10_CLKOUT_LPC1	SB3V	NATIVE	CK_LPC1_24M_R	
GPP_A11	GPP_A11_PME_N	SB3V	NATIVE	SIO_PME#	PU 4.7K +3V3_S5
GPP_A12	GPP_A12_BMBUSY_N	SB3V	NATIVE	PCH_GPP_A12	Reserved PU 10K +3V3_S5
GPP_A13	GPP_A13_SUSWARN_N_SUSPWRDNACK	SB3V	NATIVE	SUSWARN#	Reserved PU 10K +3V3_S5
GPP_A14	GPP_A14_SUS_STAT_N_ESPI_RST_N	SB3V	NATIVE	GPP_A14	Reserved PU 10K +3V3_S5
GPP_A15	GPP_A15_SUSACK_N	SB3V	NATIVE	SUSACK#	Reserved PU 10K +3V3_S5
GPP_A16	GPP_A16_CLKOUT_48	SB3V	NATIVE	NC	
GPP_A17	GPP_A17_ISH_GP7	SB3V	OUT	NC	
GPP_A18	GPP_A18_ISH_GP0	SB3V	IN	NC	
GPP_A19	GPP_A19_ISH_GP1	SB3V	NATIVE	NC	
GPP_A20	GPP_A20_ISH_GP2	SB3V	OUT	NC	
GPP_A21	GPP_A21_ISH_GP3	SB3V	IN	NC	
GPP_A22	GPP_A22_ISH_GP4	SB3V	IN	COM_A_DET#	PU 10K +3V3_S5
GPP_A23	GPP_A23_ISH_GP5	SB3V	NATIVE	NC	
GPP_B0	GPP_B0	SB3V	NATIVE	N.C	
GPP_B1	GPP_B1	SB3V	NATIVE	N.C	
GPP_B2	GPP_B2_VRALERT_N	SB3V	NATIVE	PU_PCH_VRALERT_N	PU 10K +3V3_S5
GPP_B3	GPP_B3_CPU_GP2	SB3V	NATIVE	GPP_B3_TP	
GPP_B4	GPP_B4_CPU_GP3	SB3V	NATIVE	GPP_B4	Reserved PU 10K +3V3
GPP_B5	GPP_B5_SRCCLKREQ0_N	SB3V	NATIVE	CLK_REQ1_PCIEX8#	PU 10K +3V3_S5
GPP_B6	GPP_B6_SRCCLKREQ1_N	SB3V	NATIVE	PCH_CLK_REQ1#	Reserved PU 10K +3V3_S5
GPP_B7	GPP_B7_SRCCLKREQ2_N	SB3V	NATIVE	NC	
GPP_B8	GPP_B8_SRCCLKREQ3_N	SB3V	NATIVE	CLK_REQ3_M.2_WLAN#	PU 10K +3V3_S5
GPP_B9	GPP_B9_SRCCLKREQ4_N	SB3V	NATIVE	CLK_REQ4_M.2_SSD#	PU 10K +3V3_S5
GPP_B10	GPP_B10_SRCCLKREQ5_N	SB3V	NATIVE	NC	
GPP_B11	GPP_B11	SB3V	NATIVE	NC	
GPP_B12	GPP_B12_SLP_S0_N	SB3V	NATIVE	PCH_GPP_B12	TP
GPP_B13	GPP_B13_PLTRST_N	SB3V	NATIVE	PCH_PLTRST_R#	Reserved PU 10K +3V3
GPP_B14	GPP_B14_SPKR	SB3V	NATIVE	S_SPKR_OUT	strap PD 20K
GPP_B15	GPP_B15_GSPI0_CS_N	SB3V	NATIVE	DP_D_DET#	PU 10K +3V3_S5
GPP_B16	GPP_B16_GSPI0_CLK	SB3V	NATIVE	PCH_GPP_B16	Reserved PU 10K +3V3_S5
GPP_B17	GPP_B17_GSPI0_MISO	SB3V	NATIVE	PCH_GPP_B17	Reserved PU 10K +3V3_S5
GPP_B18	GPP_B18_GSPI0_MOSI	SB3V	NATIVE	PCH_STRAP_GPP_B18	strap PD 1K
GPP_B19	GPP_B19_GSPI1_CS_N	SB3V	NATIVE	NC	
GPP_B20	GPP_B20_GSPI1_CLK	SB3V	NATIVE	SMI#	PU 10K +3V3
GPP_B21	GPP_B21_GSPI1_MISO	SB3V	NATIVE	NC	
GPP_B22	GPP_B22_GSPI1_MOSI	SB3V	NATIVE	PCH_STRAP_GPP_B22	strap PD 20K
GPP_B23	GPP_B23_SML1ALERT_N_PCHHOT_N	SB3V	NATIVE	SML1ALERT#	strap PU 150K +3V3_S5

GPIO	Signal Name	Power Well	In/Out	Tiny4 Usage	Tiny4 Note
GPP_C0	GPP_C0_SMBCLK	SB3V	NATIVE	SMB_CLK_SUS	PU 2.2K +3V3_S5
GPP_C1	GPP_C1_SMBDATA	SB3V	NATIVE	SMB_DATA_SUS	PU 2.2K +3V3_S5
GPP_C2	GPP_C2_SMBALERT_N	SB3V	NATIVE	SMBALERT#	strap PU 4.7K +3V3_S5
GPP_C3	GPP_C3_SML0CLK	SB3V	NATIVE	SML0_CLK_LAN@10ohm	PU 499 +3V3_S5
GPP_C4	GPP_C4_SML0DATA	SB3V	NATIVE	SML0_DATA_LAN@10ohm	PU 499 +3V3_S5
GPP_C5	GPP_C5_SML0ALERT_N	SB3V	NATIVE	SML0ALERT#	strap
GPP_C6	GPP_C6_SML1CLK	SB3V	NATIVE	SMLINK1_CLK	PU 2.2K +3V3_S5
GPP_C7	GPP_C7_SML1DATA	SB3V	NATIVE	SMLINK1_DATA	PU 1K +3V3_S5
GPP_C8	GPP_C8_UART0_RXD	SB3V	IN	CLEAR_CMOS#	PU 10K +3V3_S5
GPP_C9	GPP_C9_UART0_TXD	SB3V	NATIVE	COM_B_DET#	PU 10K +3V3_S5
GPP_C10	GPP_C10_UART0_RTS	SB3V	INOUT	NC	
GPP_C11	GPP_C11_UART0_CTS_N	SB3V	IN	NC	
GPP_C12	GPP_C12_UART1_RXD_ISH_UART1_RXD	SB3V	IN	NC	
GPP_C13	GPP_C13_UART1_TXD_ISH_UART1_TXD	SB3V	IN	TPM_EN	TPM_Disable PU 10K +3V3_S5
GPP_C14	GPP_C14_UART1_RTS_N_ISH_UART1_RT	SB3V	IN	NC	
GPP_C15	GPP_C15_UART1_CTS_N_ISH_UART1_CT	SB3V	IN	NC	
GPP_C16	GPP_C16_I2C0_SDA	SB3V	NATIVE	NC	
GPP_C17	GPP_C17_I2C0_SCL	SB3V	NATIVE	NC	
GPP_C18	GPP_C18_I2C1_SDA	SB3V	NATIVE	NC	
GPP_C19	GPP_C19_I2C1_SCL	SB3V	NATIVE	NC	
GPP_C20	GPP_C20_UART2_RXD	SB3V	NATIVE	NC	
GPP_C21	GPP_C21_UART2_TXD	SB3V	NATIVE	NC	
GPP_C22	GPP_C22_UART2_RTS_N	SB3V	NATIVE	NC	
GPP_C23	GPP_C23_UART2_CTS_N	SB3V	NATIVE		

GPP_D0	GPP_D0_SPI1_CS_N	SB3V	NATIVE	NC	
GPP_D1	GPP_D1_SPI1_CLK	SB3V	NATIVE	PW_LED#	PU 1K +3V3_S5
GPP_D2	GPP_D2_SPI1_MISO	SB3V	NATIVE	NC,TP	
GPP_D3	GPP_D3_SPI1_MOSI	SB3V	NATIVE	NC,TP	
GPP_D4	GPP_D4_ISH_I2C2_SDA	SB3V	NATIVE	NC	
GPP_D5	GPP_D5_SSP0_SFRM	SB3V	NATIVE	NC	
GPP_D6	GPP_D6_SSP0_TXD	SB3V	NATIVE	NC	
GPP_D7	GPP_D7_SSP0_RXD	SB3V	NATIVE	NC	
GPP_D8	GPP_D8_SSP0_SCLK	SB3V	NATIVE	NC	
GPP_D9	GPP_D9_ISH_SPI_CS_N	SB3V	NATIVE	NC	
GPP_D10	GPP_D10_ISH_SPI_CLK	SB3V	NATIVE	NC	
GPP_D11	GPP_D11_ISH_SPI_MISO	SB3V	IN	USB_DET#	PU 10K +3V3
GPP_D12	GPP_D12_ISH_SPI_MOSI	SB3V	IN	NC	
GPP_D13	GPP_D13_ISH_UART0_RXD	SB3V	IN	NC	
GPP_D14	GPP_D14_ISH_UART0_TXD	SB3V	IN	PS2_PINHEADER#	PU 10K +3V3
GPP_D15	GPP_D15_ISH_UART0_RTS_N	SB3V	IN	GPP_D15	PU 10K +3V3
GPP_D16	GPP_D16_ISH_UART0_CTS_N	SB3V	OUT	NC	
GPP_D17	GPP_D17_DMIC_CLK1	SB3V	IN	RING#	PU 8.2K +3V3_S5
GPP_D18	GPP_D18_DMIC_DATA1	SB3V	NATIVE	USBDEBUG	PU 10K +3V3_S5
GPP_D19	GPP_D19_DMIC_CLK0	SB3V	NATIVE	N.C	
GPP_D20	GPP_D20_DMIC_DATA0	SB3V	NATIVE	N.C	
GPP_D21	GPP_D21_SPI1_IO2	SB3V	NATIVE	N.C	
GPP_D22	GPP_D22_SPI1_IO3	SB3V	NATIVE	N.C	
GPP_D23	GPP_D23_ISH_I2C2_SCL	SB3V	NATIVE	N.C	

GPIO	Signal Name	Power Well	In/Out	Tiny4 Usage	Tiny4 Note
GPP_E0	GPP_E0_SATAXPCIE0_SATAGP0	SB3V	NATIVE	N.C	
GPP_E1	GPP_E1_SATAXPCIE1_SATAGP1	SB3V	NATIVE	N.C	
GPP_E2	GPP_E2_SATAXPCIE2_SATAGP2	SB3V	NATIVE	PWR_PROTECT#	PU 10K +3V3_S5
GPP_E3	GPP_E3_CPU_GP0	SB3V	IN	PU_PCH_CPU_GP0	PU 10K +3V3_S5
GPP_E4	GPP_E4_DEVSLP0	SB3V	IN	N.C	
GPP_E5	GPP_E5_DEVSLP1	SB3V	NATIVE	N.C	
GPP_E6	GPP_E6_DEVSLP2	SB3V	NATIVE	HDD_PWR0T	
GPP_E7	GPP_E7_CPU_GP1	SB3V	NATIVE	GPP_E7_TP	NC
GPP_E8	GPP_E8_SATALED_N	SB3V	OUT	SATA_LED_IN#	PU 10K +3V3
GPP_E9	GPP_E9_USB2_OC0_N	SB3V	IN	USB_OC0_FRONT_12#	Front USB 3.0 X 2
GPP_E10	GPP_E10_USB2_OC1_N	SB3V	IN	USB_OC1_REAR_3#	Rear USB 3.0
GPP_E11	GPP_E11_USB2_OC2_N	SB3V	IN	USB_OC2_REAR_4#	Rear USB 3.0
GPP_E12	GPP_E12_USB2_OC3_N	SB3V	IN	USB_OC3_REAR_5#	Rear USB 3.0

GPIO	Signal Name	Power Well	In/Out	Tiny4 Usage	Tiny4 Note
GPP_F0	GPP_F17_USB2_OCB_6	SB3V	NATIVE	M.2_SSD_PEDET1#	PU 10K +3V3_S5
GPP_F1	GPP_F1_SATAXPCIE1_SATAGP4	SB3V	NATIVE	M.2_SSD_PEDET0#	PU 10K +3V3_S5
GPP_F2	GPP_F2_SATAXPCIE5_SATAGP5	SB3V	NATIVE	PWR_THROTTLE#	PU 10K +3V3_S5
GPP_F3	GPP_F3_SATAXPCIE6_SATAGP6	SB3V	NATIVE	NC	
GPP_F4	GPP_F4_SATAXPCIE7_SATAGP7	SB3V	NATIVE	NC	
GPP_F5	GPP_F5_DEVSLP3	SB3V	NATIVE	TPM_SPI_IRQ#	PU 4.7K +3V3_S5
GPP_F6	GPP_F6_DEVSLP4	SB3V	NATIVE	NC	
GPP_F7	GPP_F7_DEVSLP6	SB3V	NATIVE	SSD_SATA_DEVSLP1	
GPP_F8	GPP_F8_DEVSLP5	SB3V	NATIVE	SSD_SATA_DEVSLP2	
GPP_F9	GPP_F9_DEVSLP7	SB3V	IN	NC	
GPP_F10	GPP_F10_SCLOCK	SB3V	NATIVE	PCH_CONFIG_JUMPER	PU 1K +3V3_S5
GPP_F11	GPP_F11_SLOAD	SB3V	NATIVE	PCH_RSV0	PU 10K +3V3_S5
GPP_F12	GPP_F12_SDATAOUT1	SB3V	NATIVE	SV_ADVANCE_GP48	PU 20K +3V3_S5
GPP_F13	GPP_F13_SDATAOUT0	SB3V	NATIVE	GPS8_GFX_CRB_DETECT	PD 10K
GPP_F14	GPP_F14	SB3V	IN	H_SKTOCC#	PU 10K +3V3_S5
GPP_F15	GPP_F15_USB2_OCB_4	SB3V	NATIVE	USB_OC4_REAR_6#	Rear USB 3.0
GPP_F16	GPP_F16_USB2_OCB_5	SB3V	NATIVE	USB_OC5_INT_7#	Int USB HDR
GPP_F17	GPP_F17_USB2_OCB_6	SB3V	NATIVE	OC6#	PU 8.2K +3V3_S5
GPP_F18	GPP_F18_USB2_OCB_7	SB3V	NATIVE	OC7#	PU 8.2K +3V3_S5
GPP_F19	GPP_F19_EDP_VDDEN	SB3V	NATIVE	N.C	
GPP_F20	GPP_F20_EDP_BKLTEN	SB3V	NATIVE	N.C	
GPP_F21	GPP_F21_EDP_BKLTCTL	SB3V	NATIVE	N.C	
GPP_F22	GPP_F22	SB3V	OUT	PCH_GPIO_F22	PU 10K +3V3_S5
GPP_F23	GPP_F23	SB3V	NATIVE	N.C	

GPP_G0	GPP_G0_FAN_TACH_0	SB3V	IN	N.C	
GPP_G1	GPP_G1_FAN_TACH_1	SB3V	IN	N.C	
GPP_G2	GPP_G2_FAN_TACH_2	SB3V	IN	N.C	
GPP_G3	GPP_G3_FAN_TACH_3	SB3V	OUT	N.C	
GPP_G4	GPP_G4_FAN_TACH_4	SB3V	NATIVE	N.C	
GPP_G5	GPP_G5_FAN_TACH_5	SB3V	NATIVE	N.C	
GPP_G6	GPP_G6_FAN_TACH_6	SB3V	NATIVE	N.C	
GPP_G7	GPP_G7_FAN_TACH_7	SB3V	NATIVE	N.C	
GPP_G8	GPP_G8_FAN_PWM_0	SB3V	NATIVE	N.C	
GPP_G9	GPP_G9_FAN_PWM_1	SB3V	NATIVE	N.C	
GPP_G10	GPP_G10_FAN_PWM_2	SB3V	NATIVE	N.C	
GPP_G11	GPP_G11_FAN_PWM_3	SB3V	IN	N.C	
GPP_G12	GPP_G12_GSXDOUT	SB3V	IN	BRD_ID0	BRD ID_PD 10K
GPP_G13	GPP_G13_GSXSLOAD	SB3V	IN	BRD_ID1	BRD ID_NAL
GPP_G14	GPP_G14_GSXDIN	SB3V	IN	BRD_ID2	BRD ID_PD 10K
GPP_G15	GPP_G15_GSXSRESET_N	SB3V	IN	BRD_ID3	BRD ID_PD 10K
GPP_G16	GPP_G16_GSXCLK	SB3V	IN	BRD_ID4	BRD ID_PU 10K +3V3_S5
GPP_G17	GPP_G17_ADR_COMPLETE	SB3V	IN	BRD_ID5	BRD ID_PU 10K +3V3_S5
GPP_G18	GPP_G18_NMI_N	SB3V	OUT	FM_NMI_EVENT#	PU 10K +3V3_S5
GPP_G19	GPP_G19_SMI_N	SB3V	IN	SIO_SCI#	PU 10K +3V3
GPP_G20	GPP_G20	SB3V	IN	NC	
GPP_G21	GPP_G21	SB3V	IN	TPM_GPIO	PU 10K +3V3_S5
GPP_G22	GPP_G22	SB3V	IN	NC	
GPP_G23	GPP_G23	SB3V	IN	NC	

GPIO	Signal Name	Power Well	In/Out	Tiny4 Usage	Tiny4 Note
GPP_H0	GPP_H0_SRCCLKREQ8_N	SB3V	IN	NC	
GPP_H1	GPP_H1_SRCCLKREQ7_N	SB3V	OUT	NC	
GPP_H2	GPP_H2_SRCCLKREQ6_N	SB3V	IN	NC	
GPP_H3	GPP_H3_SRCCLKREQ9_N	SB3V	OUT	NC	
GPP_H4	GPP_H4_SRCCLKREQ10_N	SB3V	NATIVE	CLK_REQ10_M.2_SSD2#	PU 10K +3V3_S5
GPP_H5	GPP_H5_SRCCLKREQ11_N	SB3V	NATIVE	NC	
GPP_H6	GPP_H6_SRCCLKREQ12_N	SB3V	NATIVE	NC	
GPP_H7	GPP_H7_SRCCLKREQ13_N	SB3V	NATIVE	NC	
GPP_H8	GPP_H8_SRCCLKREQ14_N	SB3V	NATIVE	N.C	
GPP_H9	GPP_H9_SRCCLKREQ15_N	SB3V	NATIVE	N.C	
GPP_H10	GPP_H10_SML2CLK	SB3V	NATIVE	M.2_BT_DISABLE#	PU 10K +3V3_S5
GPP_H11	GPP_H11_SML2DATA	SB3V	NATIVE	M.2_WLAN_DISABLE#	PU 10K +3V3_S5
GPP_H12	GPP_H12_SML2ALERT_N	SB3V	NATIVE	PCH_STRAP_GPP_H12	Strap, Reserve PU 4.7K +3V3_S5 Reserve PD 20K +3V3_S5
GPP_H13	GPP_H13_SML3CLK	SB3V	NATIVE	N.C	
GPP_H14	GPP_H14_SML3DATA	SB3V	NATIVE	N.C	
GPP_H15	GPP_H15_SML3ALERT_N	SB3V	NATIVE	NC	
GPP_H16	GPP_H16_SML4CLK	SB3V	NATIVE	N.C	
GPP_H17	GPP_H17_SML4DATA	SB3V	NATIVE	N.C	
GPP_H18	GPP_H18_SML4ALERT_N	SB3V	NATIVE	N.C	
GPP_H19	GPP_H19_ISH_I2C0_SDA	SB3V	NATIVE	N.C	
GPP_H20	GPP_H20_ISH_I2C0_SCL	SB3V	NATIVE	N.C	
GPP_H21	GPP_H21_ISH_I2C1_SDA	SB3V	NATIVE	N.C	
GPP_H22	GPP_H22_ISH_I2C1_SCL	SB3V	NATIVE	N.C	
GPP_H23	GPP_H23	SB3V	NATIVE	N.C	

GPP_I0	GPP_I0_DDPB_HPD0	SB3V	NATIVE	DDPB_HPD_PD	DDI1_PD 0.1uF
GPP_I1	GPP_I1_DDPC_HPD1	SB3V	NATIVE	DDPC_HPD_PD	DDI2_Reserve PU 1M +3V3 DDI2_PD 0.1uF
GPP_I2	GPP_I2_DDPD_HPD2	SB3V	NATIVE	DDPD_HPD_PD	DDI3_PD 0.1uF
GPP_I3	GPP_I3_DDPE_HPD3	SB3V	NATIVE	DDPE_HPD3	PD 100K
GPP_I4	GPP_I4_EDP_HPD	SB3V	NATIVE	PCH_GPP_I4	PD 100K
GPP_I5	GPP_I5_DDPB_CTRLCLK	SB3V	NATIVE	DDPB_CTRLCLK	PU 2.2K +3V3
GPP_I6	GPP_I6_DDPB_CTRLDATA	SB3V	NATIVE	DDPB_CTRLDATA	PU 2.2K +3V3
GPP_I7	GPP_I7_DDPC_CTRLCLK	SB3V	NATIVE	DDPC_CTRLCLK	PU 2.2K +3V3
GPP_I8	GPP_I8_DDPC_CTRLDATA	SB3V	NATIVE	DDPC_CTRLDATA	PU 2.2K +3V3
GPP_I9	GPP_I9_DDPD_CTRLCLK	SB3V	NATIVE	DDPD_CTRLCLK	PU 2.2K +3V3
GPP_I10	GPP_I10_DDPD_CTRLDATA	SB3V	NATIVE	DDPD_CTRLDATA	PU 2.2K +3V3

GPD0	GPD0_BATLOW_N	SB3V_DSW	NATIVE	PCH_OPT2_PU	PU 10K +3V3_DSW
GPD1	GPD1_ACPRESENT	SB3V_DSW	OUT	SUS_LED#	PU 10K +3V3_DSW
GPD2	GPD2_LAN_WAKE_N	SB3V_DSW	NATIVE	LANWAKE_R_N	PU 4.7K +3V3_DSW
GPD3	GPD3_PWRBTN_N	SB3V_DSW	NATIVE	PWRBTN#	PU 3K +3V3_DSW
GPD4	GPD4_SLP_S3_N	SB3V_DSW	NATIVE	SLP_S3#	
GPD5	GPD5_SLP_S4_N	SB3V_DSW	NATIVE	SLP_S4#	
GPD6	GPD6_SLP_A_	SB3V_DSW	NATIVE	SLP_A#_PCH	TP5
GPD7	GPD7_USB2_WAKEOUT_N	SB3V_DSW	NATIVE	NC	
GPD8	GPD8_SUSCLK	SB3V_DSW	NATIVE	PCH_SUSCLK	
GPD9	GPD9_SLP_WLAN_N	SB3V_DSW	NATIVE	SLP_WLAN#	Reserve PU 10K +3V3_DSW
GPD10	GPD10_SLP_S5_N	SB3V_DSW	NATIVE	SLP_S5#	FAN LED CONTROL
GPD11	GPD11_LANPHYPC	SB3V_DSW	NATIVE	LAN_DISABLE#	Reserve PU 10K +3V3_S5

GPIO	Signal Name	In/Out	Power well	Tiny3	I
GPP_G0	FAN_TACH_0(Serve Only)	GPI		Non Use	
GPP_G1	FAN_TACH_1(Serve Only)	GPI		Non Use	
GPP_G2	FAN_TACH_2(Serve Only)	GPI		Non Use	
GPP_G3	FAN_TACH_3(Serve Only)	GPI		Non Use	
GPP_G4	FAN_TACH_4(Serve Only)	GPI		Non Use	
GPP_G5	FAN_TACH_5(Serve Only)	GPI		Non Use	
GPP_G6	FAN_TACH_6(Serve Only)	GPI		Non Use	
GPP_G7	FAN_TACH_7(Serve Only)	GPI		Non Use	
GPP_G8	FAN_PWM_0(Serve Only)	FAN_PWM_0		Non Use	
GPP_G9	FAN_PWM_1(Serve Only)	FAN_PWM_1		Non Use	
GPP_G10	FAN_PWM_2(Serve Only)	FAN_PWM_2		Non Use	
GPP_G11	FAN_PWM_3(Serve Only)	FAN_PWM_3		Non Use	
GPP_G12	GSXDOUT	GPI	+3V3	BRD_ID0 (PU 10K)	
GPP_G13	GSXSLOAD	GPI	+3V3	BRD_ID1 (PU 10K)	
GPP_G14	GSXDIN	GPI	+3V3	BRD_ID2 (PU 10K)	
GPP_G15	GSXRESET#	GPI	+3V3	BRD_ID3 (PU 10K)	
GPP_G16	GSXCLK	GPI	+3V3	BRD_ID4 (PU 10K)	
GPP_G17	ADR_COMPLETE	GPI	+3V3	BRD_ID5 (PU 10K)	
GPP_G18	NMI#	GPO	+3V3_S5	FM_NMI_EVENT# (PU 10K)	
GPP_G19	SMI#	GPI(SCI)	+3V3	SIO_SCI# (PU 10K)	
GPP_G20	None	GPI		TP	
GPP_G21	None	GPI		TP	
GPP_G22	None	GPI		Non Use	
GPP_G23	None	GPI		Non Use	
GPP_H0	SRCCLKREQ6#	GPI		Non Use	
GPP_H1	SRCCLKREQ7#	GPI		Non Use	
GPP_H2	SRCCLKREQ8#	GPI		Non Use	
GPP_H3	SRCCLKREQ9#	GPI	+3V3	CLK_REQ9_SATAE# (PU 10K)	
GPP_H4	SRCCLKREQ10#	GPI		Non Use	
GPP_H5	SRCCLKREQ11#	GPI		Non Use	
GPP_H6	SRCCLKREQ12#	GPI		Non Use	
GPP_H7	SRCCLKREQ13#	GPI		Non Use	
GPP_H8	SRCCLKREQ14#	GPI		Non Use	
GPP_H9	SRCCLKREQ15#	GPI		Non Use	
GPP_H10	SML2CLK(ServerWS Only)	GPI		Non Use	
GPP_H11	SML2DATA(ServerWS Only)	GPI		Non Use	
GPP_H12	SML2ALERT#(ServerWS Only)	GPO		Non Use	
GPP_H13	SML3CLK(ServerWS Only)	GPI		Non Use	
GPP_H14	SML3DATA(ServerWS Only)	GPI		Non Use	
GPP_H15	SML3ALERT#(ServerWS Only)	GPI		Non Use	
GPP_H16	SML4CLK(ServerWS Only)	GPI		Non Use	
GPP_H17	SML4DATA(ServerWS Only)	GPI		Non Use	
GPP_H18	SML4ALERT#(ServerWS Only)	GPI		Non Use	
GPP_H19	ISH_I2C0_SDA	GPI		LINEOUT-JD	
GPP_H20	ISH_I2C0_SCL	GPI		MIC1-JD	
GPP_H21	ISH_I2C1_SDA	GPO(High)	+5V_S5	2643_P2_EN (PU 100K_NI)	
GPP_H22	ISH_I2C1_SCL	GPI(High)	+5V_S5	2643_EN (PU 100L_NI)	
GPP_H23	None	GPI		TP_GPP_H1	

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62. PCH GPIO TABLE

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PCH STRAPPING PIN

Signal	Usage	When Sampled	Comment
GSPI0_MOSI / GPP_B18	NO REBOOT 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
SMBALERT# / GPP_C2	TLS CONFIDENTIALITY 0: DISABLE 1: ENABLE (DEFAULT)	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
GSPI1_MOSI / GPP_B22	BOOT BIOS STRAP 0: SPI (DEFAULT) 1: ESPI/LPC	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap Bit 10 Boot BIOS Destination 0 SPI 1 LPC
SML0ALERT# / GPP_C5	ESPI ENABLE STRAP 0: LPC (Default) 1: ESPI	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.
SML1ALERT#/ PCHHOT#/ GPP_B23	EXI BOOT STALLBYPASS STRAP 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H12/ SML2ALERT#	ESPI FLASH SHARING MODE STRAP 0: DISABLE (DEFAULT) 1: SLAVE ATTACHED FLASH SHARING	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	JTAG ODT DISABLE STRAP(DFX) 0: DISABLE 1: ENABLE(DEFAULT)	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
SPI0_MOSI	BOOT HALF STRAP(DFX) 0: ENABLE 1: DISABLE (PCH INT PULL-UP)(DEFAULT)	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
SPI0_IO2	CONSENT STRAP(DXF) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
SPI0_IO3	PERSONALITY STRAP(DXF) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPIO Group	GPIO	SIO PIN#	In/Out	PWR well	Signal PIN	External PU / PD
GPIO-0	00	3				
	01	4	Native		SIO_LED	
	02	121	Native		HDD_FAN_PWM_SIO	+3V3
	03	122	Native		HDD_FAN_TACH_SIO	+3V3
	05	96				
GPIO-1	10	18	Native		LPC_DRQ0#	PU 10K to SIO_3VCC
	11	27	?		A20GATE	
	12	28	Native		KBRST#	
	13	55				
GPIO-2	20	29	Native		CTS1-	
	21	30	Native		DSR1-	
	22	31	Native		RTS1-	
	23	32	Native		DTR1-	
	24	33	Native		SIN1-	
	25	34	Native		SOUT1-	
	26	35	Native		DCD1-	
	27	36	Native		SIO_RIA	
GPIO-3	30	38			NC	
	31	39			NC	
	32	40			NC	
	33	41			NC	
	34	42			NC	
	35	43			NC	
	36	44			NC	
	37	45	GPIO		H_PROC_SELECT#(NI)	PU 4.7K to SIO_SB3V(NI)
GPIO-4	40	47	GPIO		2543_P2_EN	PU 100K to +5V_S5(NI)
	41	48	GPIO		2543_CLT3(NI)	PU 100K to +5V_S5
	42	49	GPIO		2543_EN	
	43	50	GPIO		2543_CLT1	
	44	51	GPIO		OVERLOAD_N	PU 10K to +5V_S5
	45	52	??		ADP_ID0	
	46	53	??		ADP_ID1	
	47	54	GPIO		ADP_OCP_EN	PU1K to 5V_S5(NI)
GPIO-5	50	7	Native		CTS2-	
	51	8	Native		DSR2-	
	52	9	Native		RTS2-	
	53	10	Native		DTR2-	
	54	11	Native		SIN2-	
	55	12	Native		SOUT2-	
	56	13	Native		DCD2-	
	57	14	Native		SIO_RIB	

GPIO Group	GPIO	SIO PIN#	In/Out	PWR well	Signal PIN	External PU / PD
GPIO-6	62	76	Native		SMLINK1_DATA	PU 2.2K to +3V3_S5
	63	75	Native		SMLINK1_CLK	PU 2.2K to +3V3_S5
	66	70	GPIO		5V_S5_DISABLE#	PU 10K to +3V3_S5(NI)
	67	100			NC	
GPIO-7	70	95			NC	
	71	98	GPIO		BAT_DET#	PU 4.7K to SIO_SB3V
	72	124	GPIO		PWR_PROTECT#	PU 10K to +3V3
	73	125	GPIO		PWR_THROTTLE#	PU 10K to SIO_SB3V
	74	37			NC	
	75	128	Native		SMB_BAT_CLK	PU 4.7K to SIO_SB3V(NI)
	76	123	Native		SMB_BAT_DAT	PU 4.7K to SIO_SB3V(NI)
	77	102			GPIO77	PD 4.7K
GPIO-8	80	15			NC	
	81	126	Native		CHASSIS_FAN_PWM_SIO	+3V3
	82	127	Native		CHASSIS_FAN_TACH_SIO	+3V3
	83	103			GPIO83	PD 4.7K
	84	104			TINY_ID	PD 4.7K
	85	2	GPIO		SIO_SCI#	PU 10K to +3V3
GPIO-9	90	93	Native		SUSWARN#(NI)	PU 10K to +3V3_S5(NI)
	91	90			NC	
	92	91	Native		SUSACK#(NI)	PU 10K to +3V3_S5(NI)
	93	89	Native		SLP_SUS#(NI)	PU 4.7K to SIO_SB3V
	94	88			RING#	PU 4.7K to SIO_SB3V(NI)
	95	74	GPIO		ME_CNTL	
GPIO-EN0	00	63	Native		PSON#(NI)	PU 4.7K to SIO_SB3V
	01	64	Native		SLP_S3#	
	02	65	?		SIO_PME#	PU 4.7K to SIO_SB3V(NI)
	03	60			PWRBTN_OUT_SIO#	PU 4.7K to SIO_SB3V
	04	61	GPIO		PWRBTN# (NI)	PU 4.7K to SIO_SB3V
	05	83	GPIO		RESETCON#	PU 4.7K to SIO_3VCC
	06	84	Native		SLP_S4#	
	07	71	GPIO		DP_ESIO(NI)	PU 4.7K to SIO_SB3V
GPIO-EN1	10	80	GPIO		PWRGD_PS	PU 4.7K to SIO_3VCC
	11	79			NC	
	12	78	Native		I2C_DATA_G	PU 2.7K to SIO_SB3V
	13	77	Native		I2C_CLK_G	PU 2.7K to SIO_SB3V
	14	81	GPIO		SIO_PWROK0	PU 4.7K to SIO_3VCC
	15	82	GPIO		PCH_SYSPWROK	PU 4.7K to SIO_3VCC
	16	73	GPIO		PCH_DPWROK(NI)	PU 2.7K to SIO_SB3V
	17	101	Native		RSMRST_SIO#	PU 4.7K to SIO_SB3V

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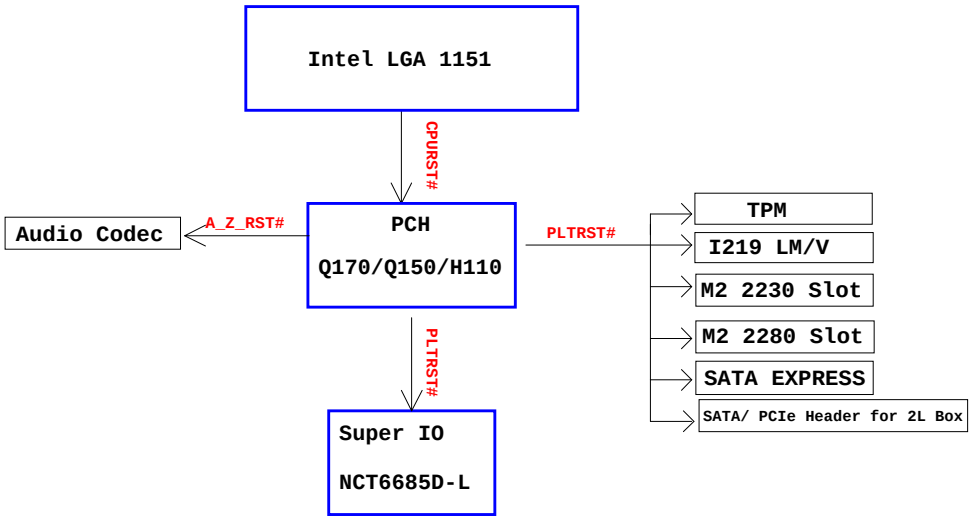
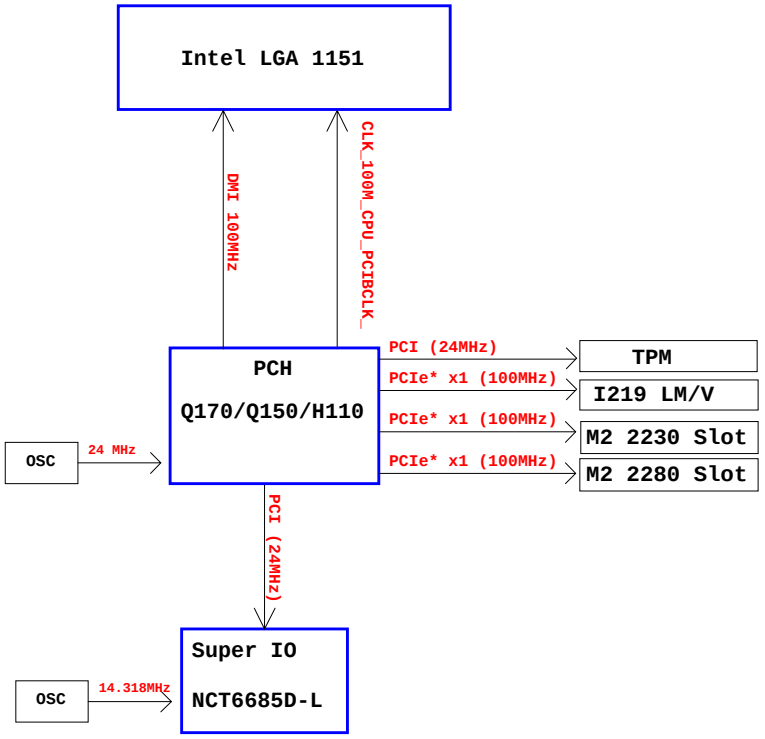
RESET MAP



CLOCK DIAGRAM



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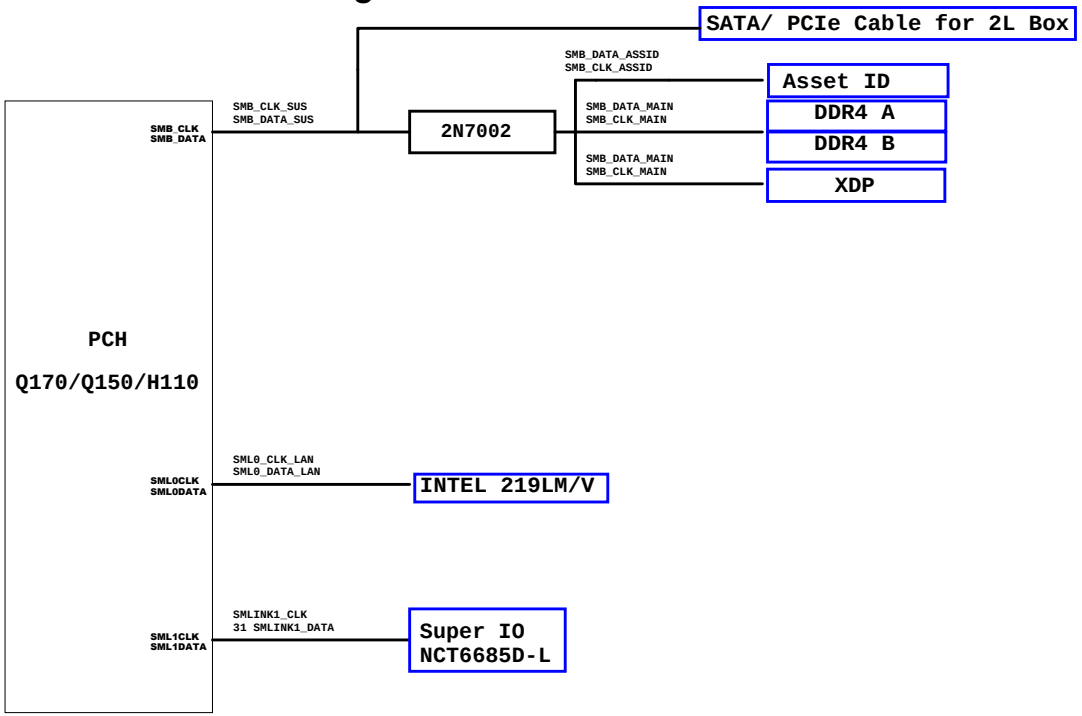
SMBUS Block Diagram



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X03

(1) Add P25,P26 ADD De-Pop noise circuit.

(2) P10,V_SA1_DIMM0_CHA & V_SA0_DIMM0_CHA add 0ohm to GND

(3) P74 PCIE X8 swap pin

(4) P14,combine CLS_COMS & ME DIS 2*5 Header, P19 S_RTCRST# header change 1*2 to NI

(5) Power:
P52:
SR2072 => 1.69K
SR1753 => 31.6K
SR2083 => 1.54K
SR2074 => 113K
SR2075 BOM
SC1482 => 2200pF (0603)
SC1483 => 68pF
SC1489 => NI
SC1490 =>2200pF

P54:
Botton MLCC => I

P58:
SR41 => 8.2K

P59:
SR2041 => 3.4K

(6) P37, Del C3000,C95,C104
P38, Del SC151,SC152,SC153

X03 0712

(7) P16, ADD R8,R9,R11,R15 0ohm for DCL2.7
P30 ADD SR5 L_LAN_DISABLE# AND ADD SR4 PD to GND for DCL2.7

(8) P47, H33,H34 Symbol change

(9) P39, Debug header symbol from 2*9 cjhange to 2*6

(10) P28,F15 symbol change to1206 size

(11) P52, SR2060 RENAME TO R24

(12) P42, PCIEX8 MLCC change to X7R

(13) USB3.0 connector Housing Color change to BLACK

X03 0713

(14) P10,P11 add C2 ,C13 for DDR4_RST have monotonic at power down

(15) P26 Q7,Q8,SQ6,SQ8 change to symbol

(16) P40, J68 2*17 header change to 2*12 header

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