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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

APUS_KL

ACER KBL R + MX13

AX2 BUILD

2018.06.15

DATE	CHANGE NO.	REV
21-OCT-2002		A

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK	BRYAN_CHIOU		
APPROVAL	TICKY_TSAI		
FILE NAME	R10_TOPAZ_WS		
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

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16 VCORE
17 VCCGT
18 VCCSA
19 ENABLE PIN
2 SYSTEM POWER
21 PCB SCREW
22 DDR4-DIMM
23 DDR4-DIMM1
24 CPU-DDR
25 CPU-LPC, SPI, SMBUS, CLINK
26 GPIO2
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37 KB CONN
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39 LEDS
4 FAN CONN
41 CODEC ALC255
42 SPEAKER & JACK
43 SATA HDD
44 WLAN/BT
45 LAN
46 TRANSFOMER
47 NGFF M.2 SSD
48 SD CARD READER
49 USB3. REDRIVER 1& 2
5 USB3. PORT 1&2
51 USB3. PORT 3
52 TYPEC ADP IN
53 TYPEC USB REDRIVER
54 USB TYPE C CONTROLLER
55 USB TYPEC CONN
56 EDP CONN
57 DP MUX
58 DP2HDMI CONVERTER
59 HDMI.2. CONN
6 DP2VGA CONVERTER
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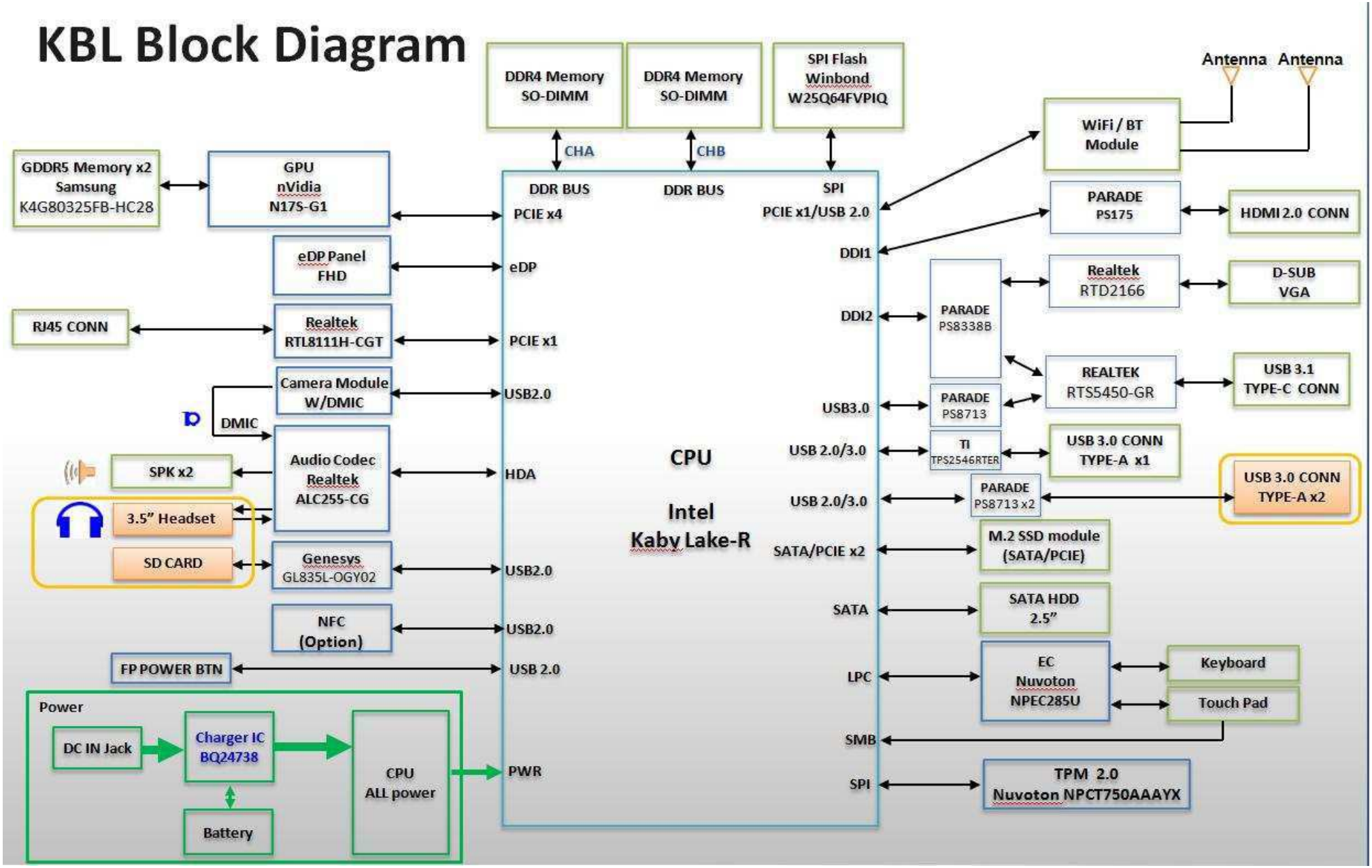
7e2 6 f 91126 1d7 3a62b79 361

KBL Block Diagram



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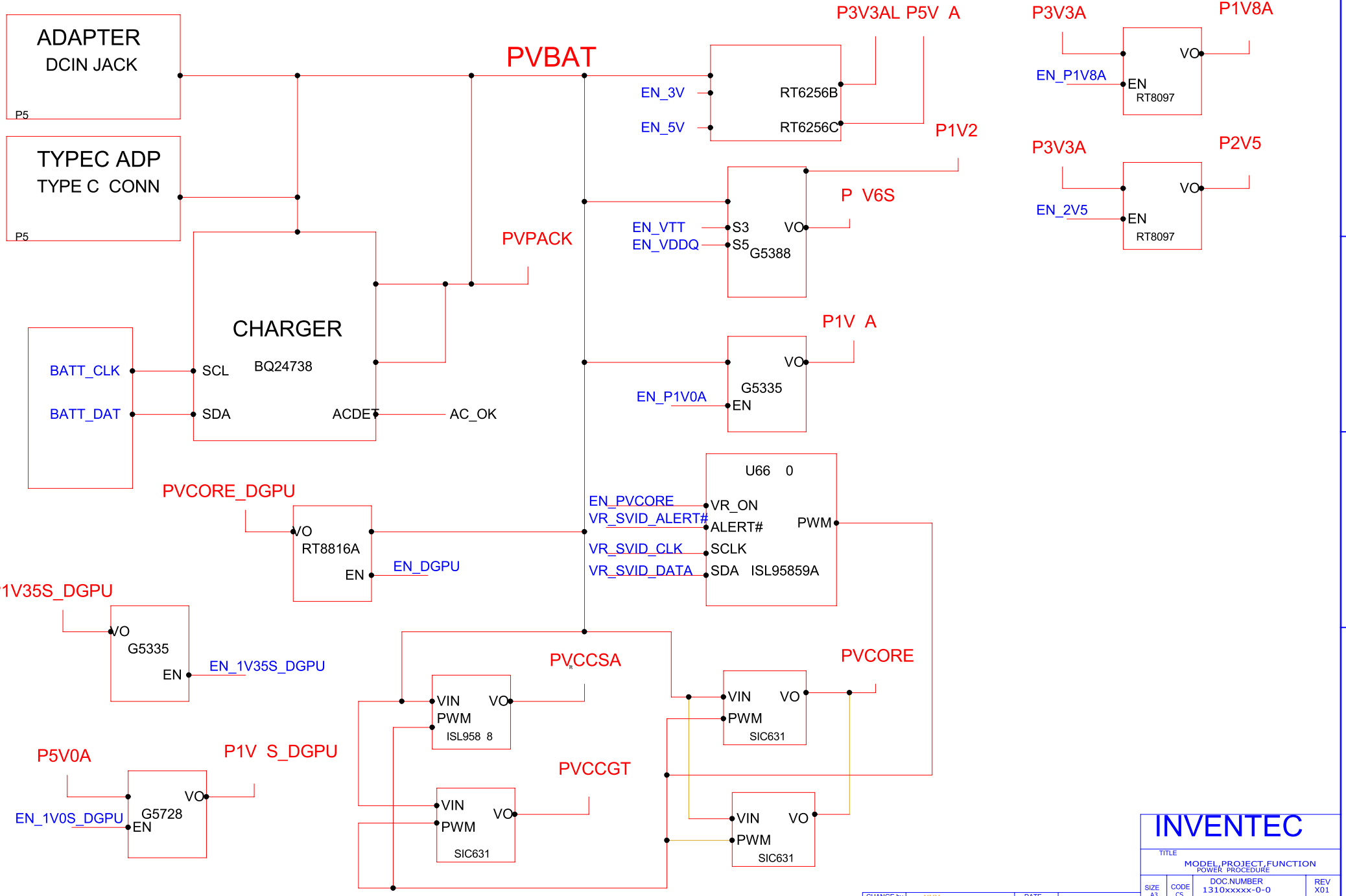

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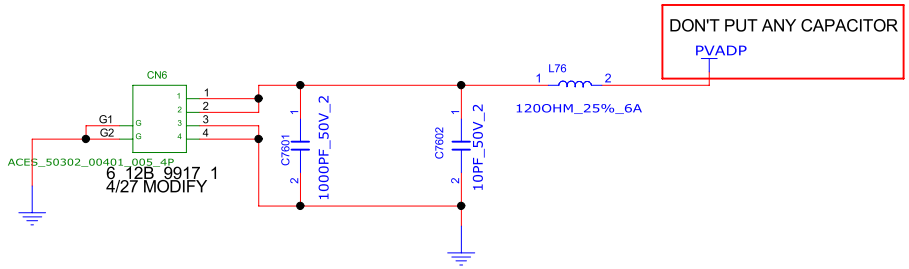

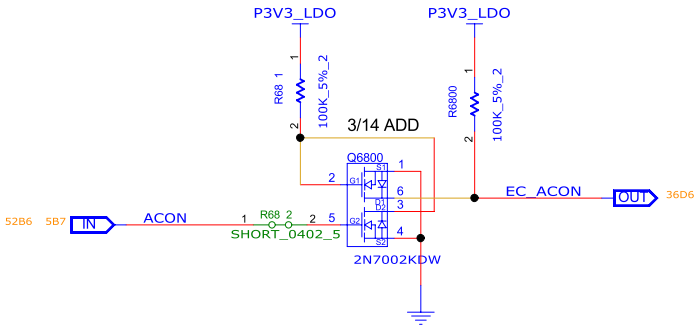

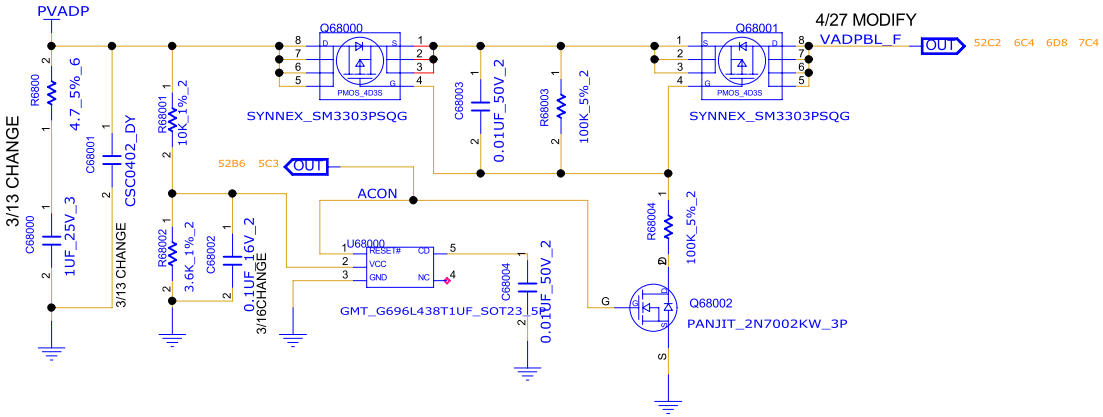

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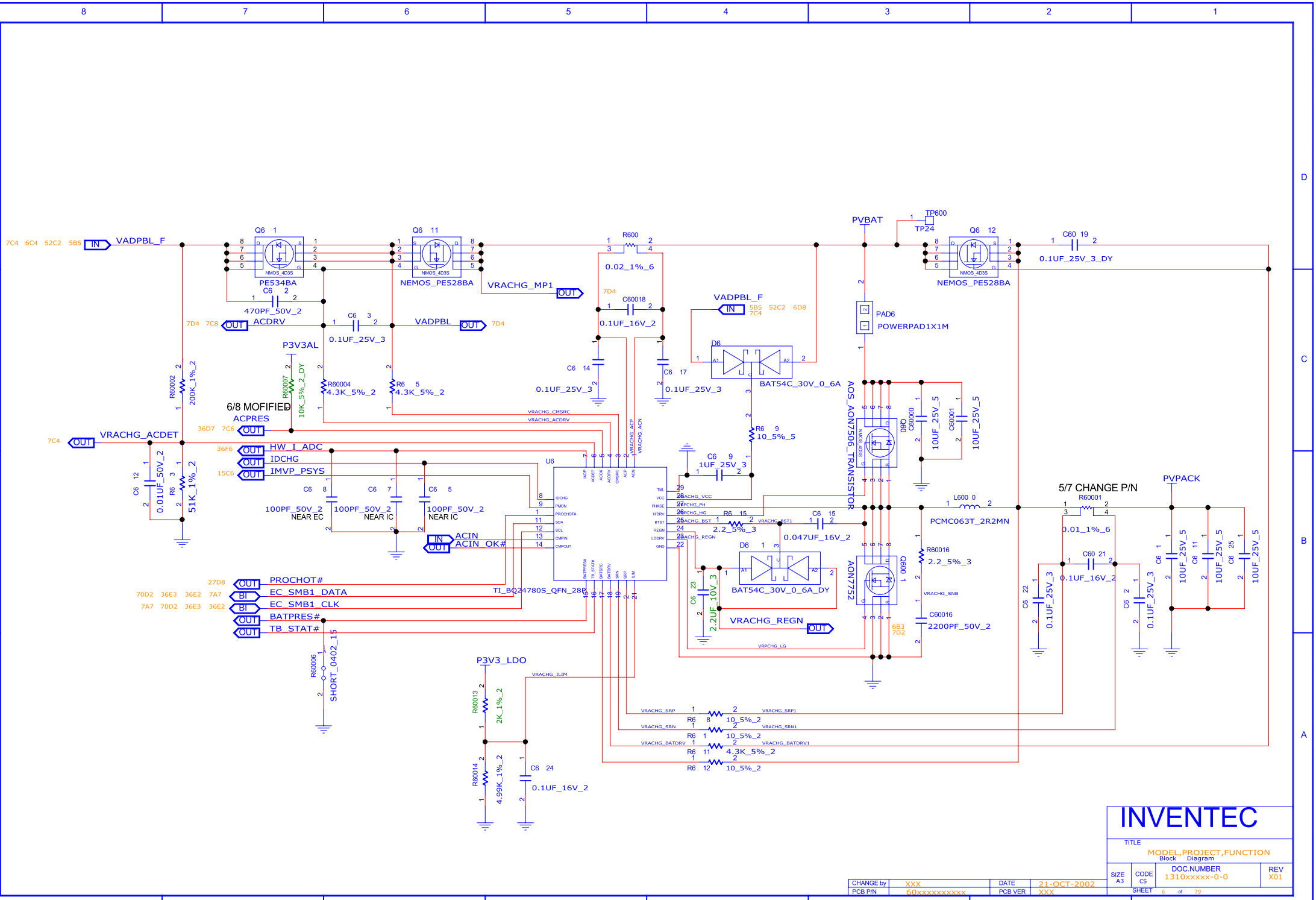
VADPBL_F
IN
PE534BA
NEMOS_PE528BA
470PF_50V_2
ACDRV
OUT
VADPBL
0.1UF_25V_3
P3V3AL
R60002
200K_1%_2
R60007
10K_5%_2_DY
R60004
4.3K_5%_2
R6 5
4.3K_5%_2
6/8 MOFIFIED
ACPRES
VRACHG_ACDET
0.01UF_50V_2
51K_1%_2
HW_I_ADC
IDCHG
IMVP_PSYS
100PF_50V_2
NEAR EC
NEAR IC
ACIN
ACIN_OK#
PROCHOT#
EC_SMB1_DATA
EC_SMB1_CLK
BATPRES#
TB_STAT#
R60006
SHORT_0402_15
TI_BQ24780S_QFN_28P
VRACHG_MP1
R600
0.02_1%_6
C60018
0.1UF_16V_2
0.1UF_25V_3
BAT54C_30V_0_6A
R6 9
10_5%_5
VRACHG_CMSRC
VRACHG_ACDRV
VRACHG_ACP
VRACHG_ACN
1UF_25V_3
R6 15
2.2_5%_3
0.047UF_16V_2
VRACHG_BST1
VRACHG_REGN
2.2UF_10V_3
PVBAT
TP600
TP24
NEMOS_PE528BA
0.1UF_25V_3_DY
PAD6
POWERPAD1X1M
AOS_AON7506_TRANSISTOR
10UF_25V_5
L600 0
PCMC063T_2R2MN
R60016
2.2_5%_3
C60016
2200PF_50V_2
AON7752
5/7 CHANGE P/N
R60001
0.01_1%_6
C60 21
0.1UF_16V_2
PVPACK
0.1UF_25V_3
P3V3_LDO
VRACHG_ILIM
R60013
2K_1%_2
R60014
4.99K_1%_2
C6 24
0.1UF_16V_2
VRACHG_SRP
VRACHG_SRP1
VRACHG_SRN
VRACHG_SRN1
VRACHG_BATDRV
VRACHG_BATDRV1
R6 8
10_5%_2
R6 1
10_5%_2
R6 11
4.3K_5%_2
R6 12
10_5%_2
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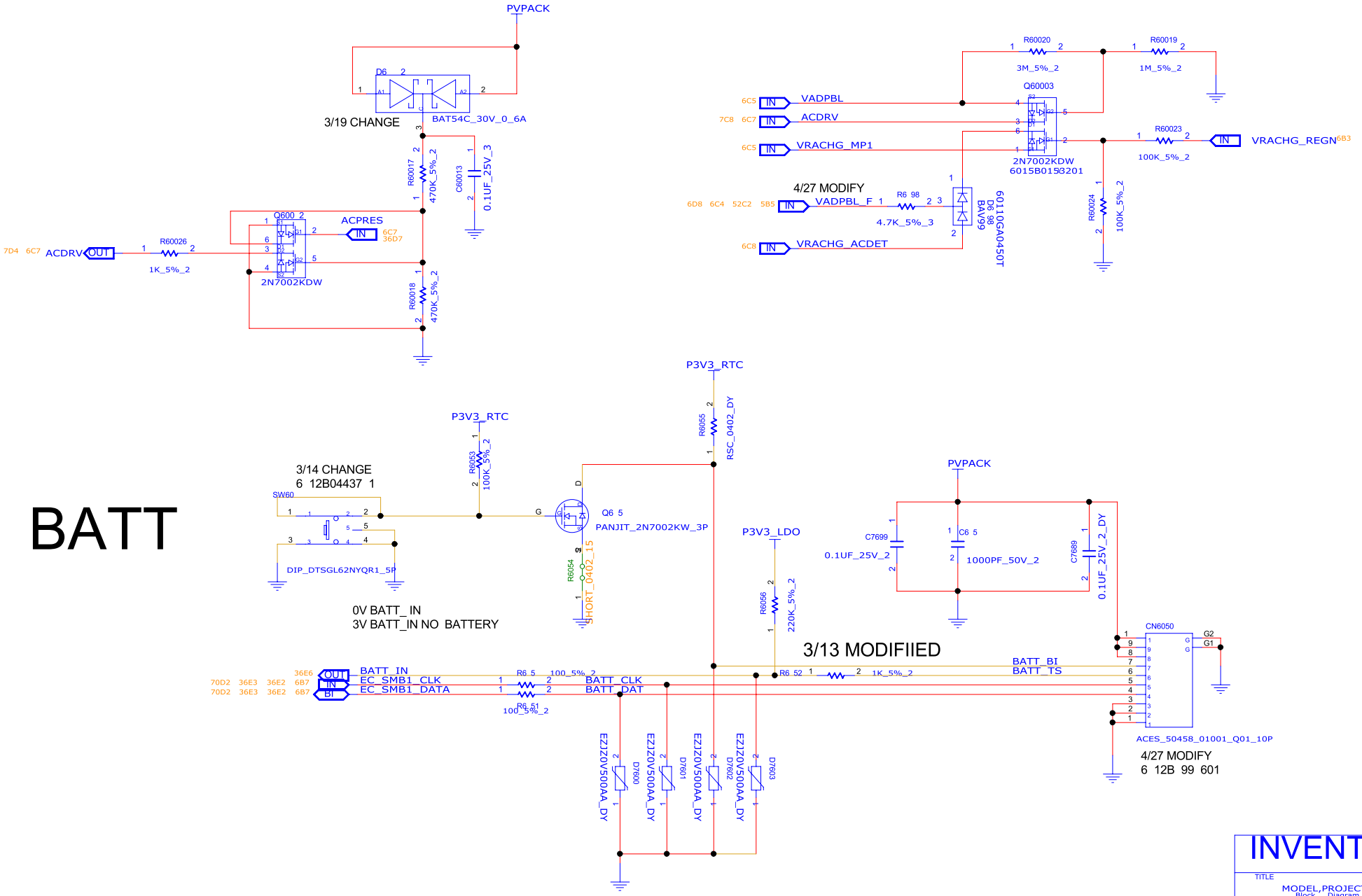
BATT



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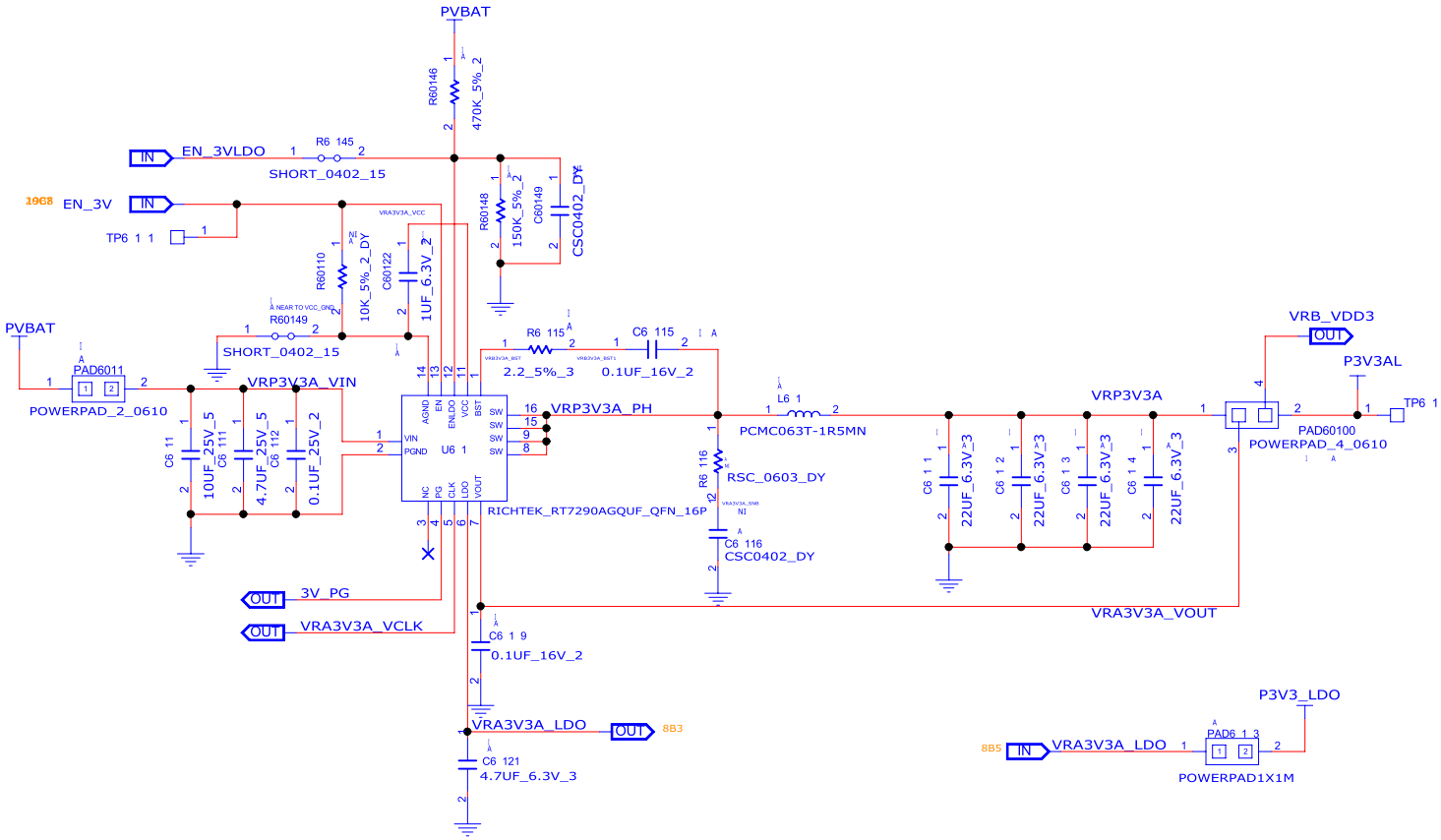

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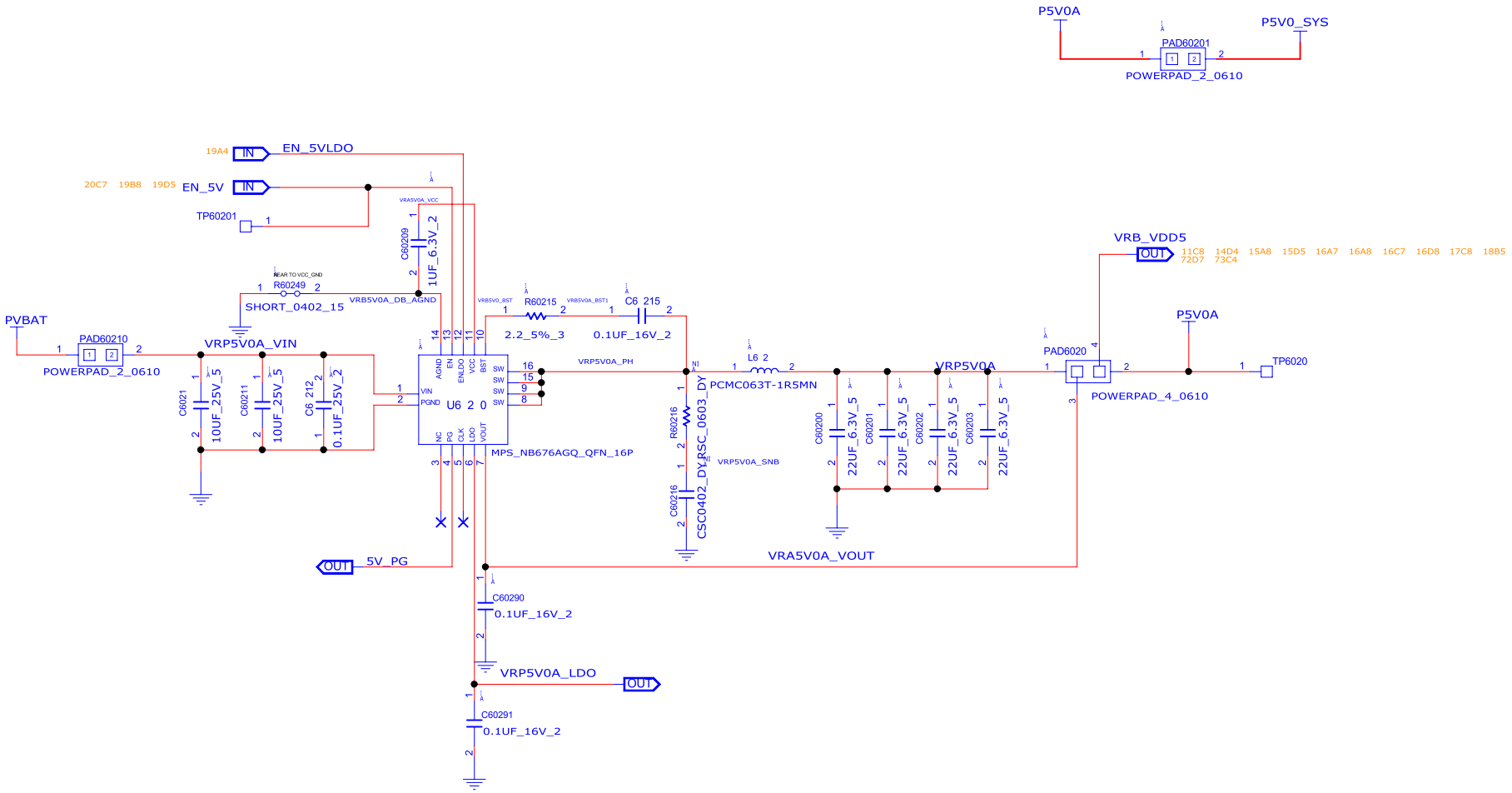

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7e2 6 f 91126 1d7 3a62b79 361

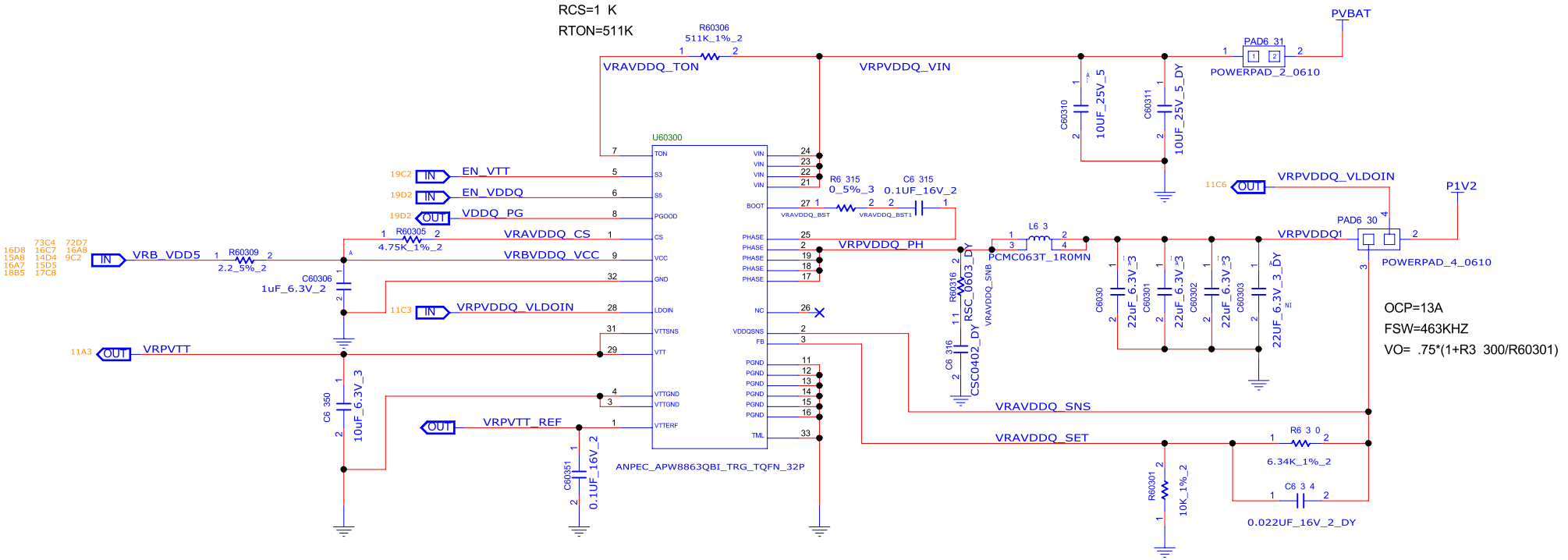

Table 2. S3 and S5 Control Table

STATE	S3	S5	VTT	VTTREF
Normal	Hi	Hi	VTTREF	VDDQSNS/2
Standby	Lo	Hi	OFF (High-Z)	VDDQSNS/2
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)

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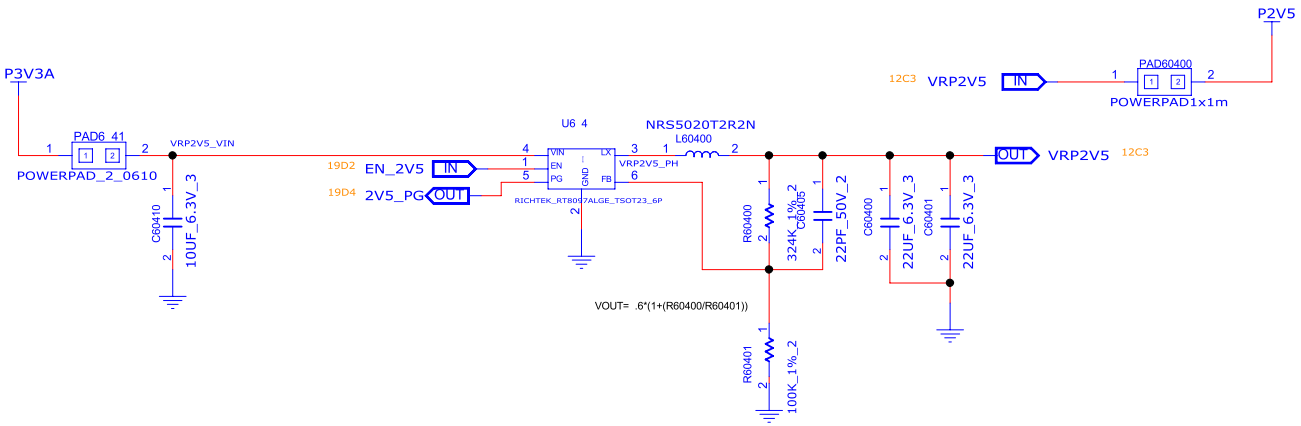

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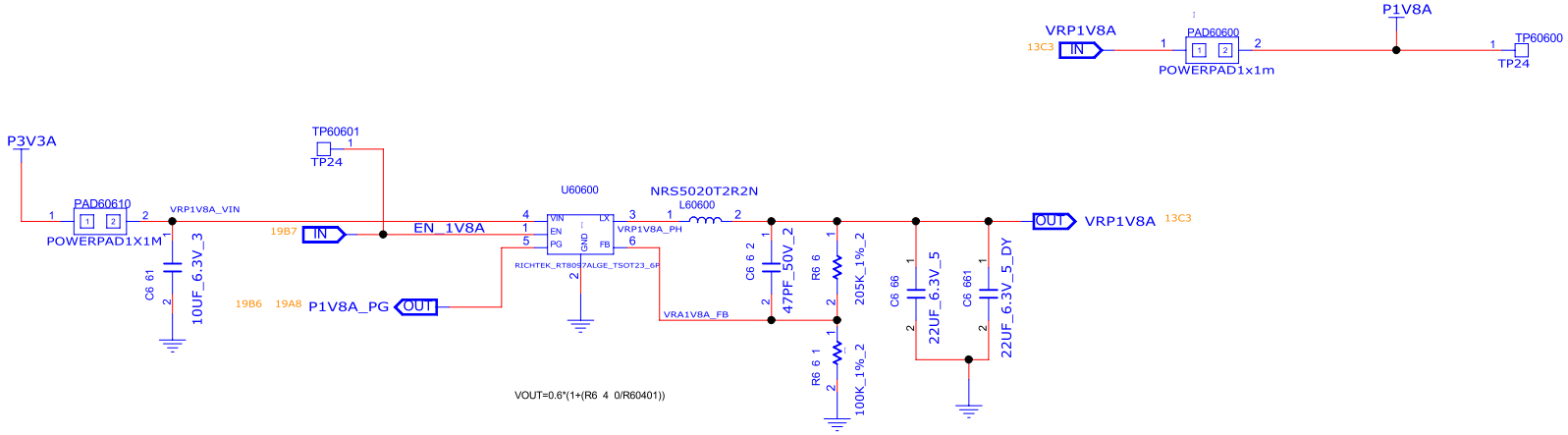

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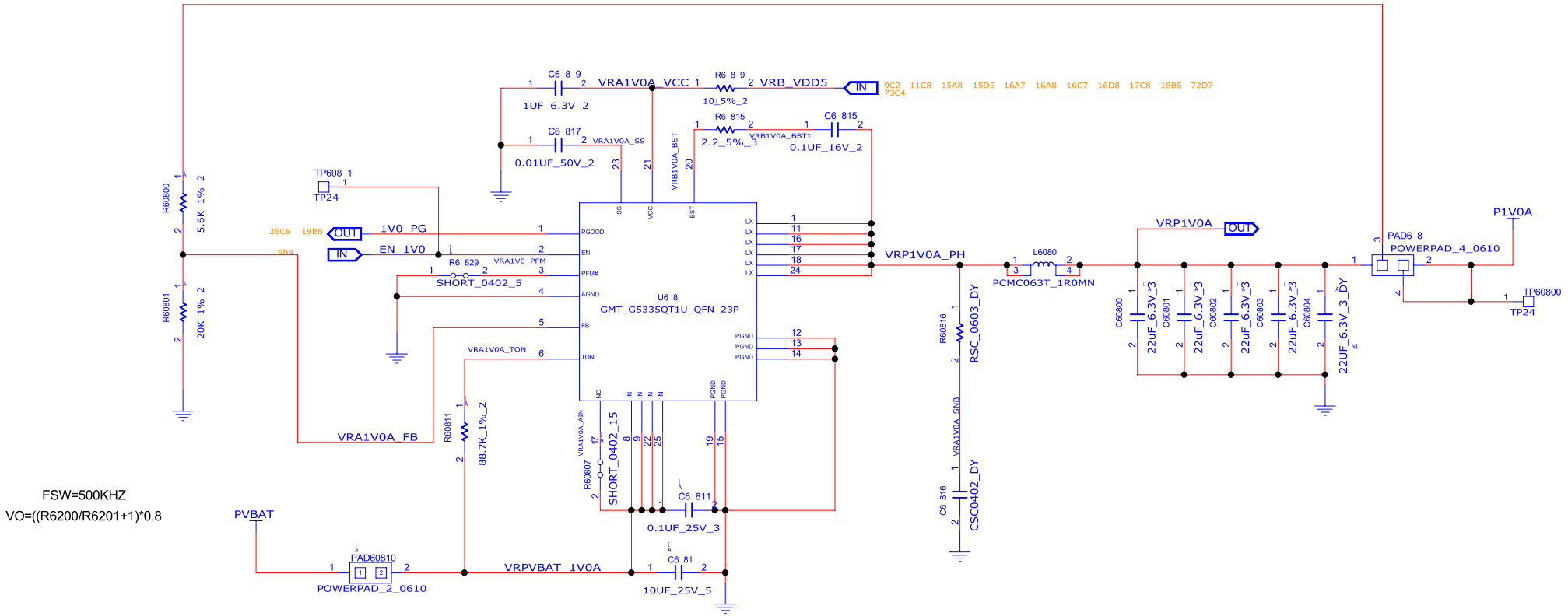

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FOR KBL-R U42
VCCIA: MAX CURRENT=64A; LOADLINE=2.4MV/A
VCCGT: MAX CURRENT=28A; LOADLINE=3.1MV/A
VCCSA: MAX CURRENT=5A; LOADLINE=10.3MV/A
FOR KBL U22 (GT1/GT2)
VCCIA: MAX CURRENT=29/32A; LOADLINE=2.4MV/A
VCCGT: MAX CURRENT=31A; LOADLINE=3.1MV/A
VCCSA: MAX CURRENT=4.5A; LOADLINE=10.3MV/A

INTERSIL_ISL95859AHRTZ_TQFN_40P
6019B1485801
U66

CLOSE TO IA DRMOS
CLOSE TO IA CHOKE
CLOSE TO SA CHOKE
CLOSE TO GT CHOKE
CLOSE TO GT DRMOS
3/20 MODIFIED
3/2 MODIFIED
5/8 CHANGE

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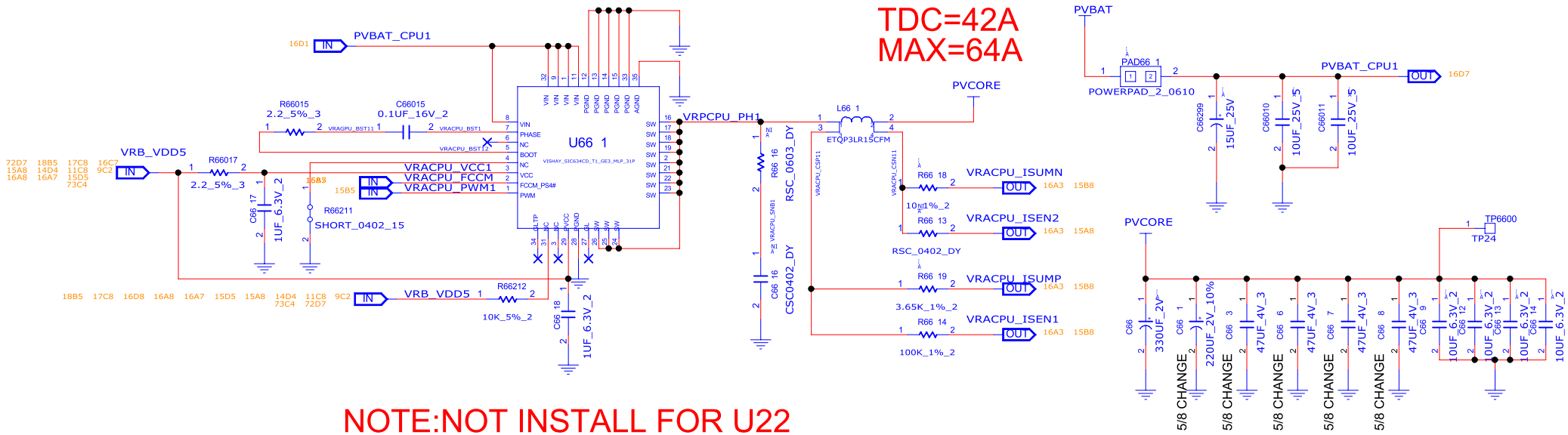
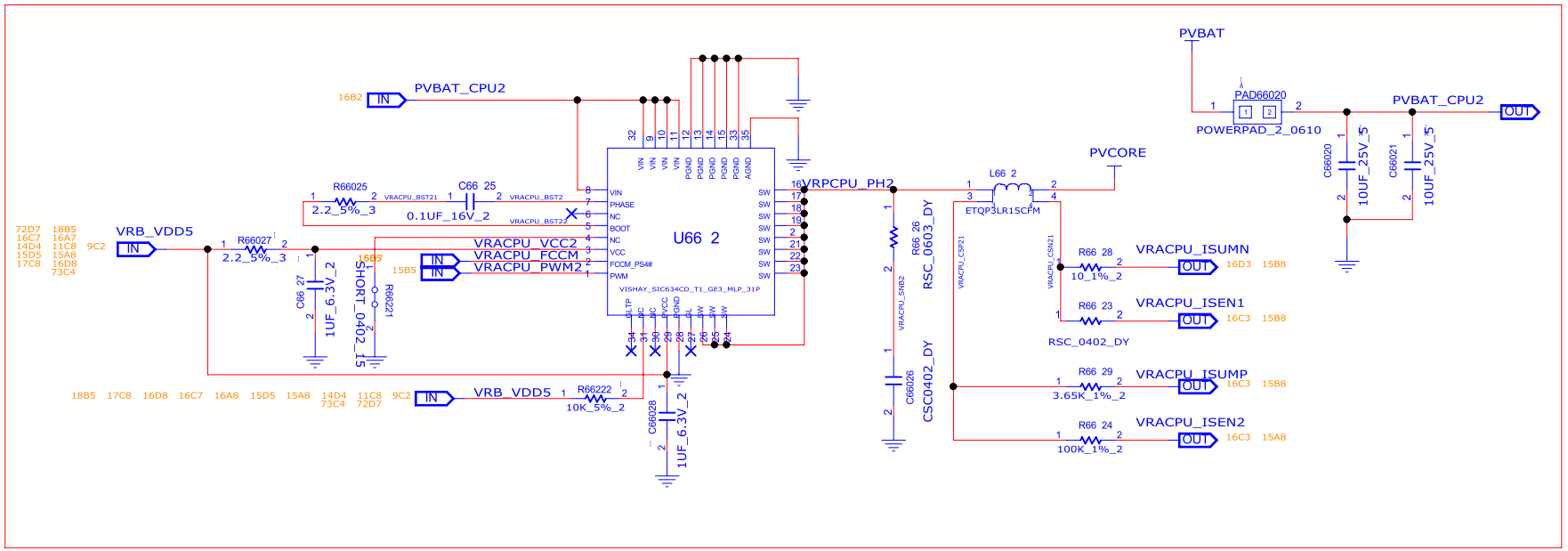
NOTE:ONE PHASE FOR U22

TDC=42A
MAX=64A



NOTE:NOT INSTALL FOR U22



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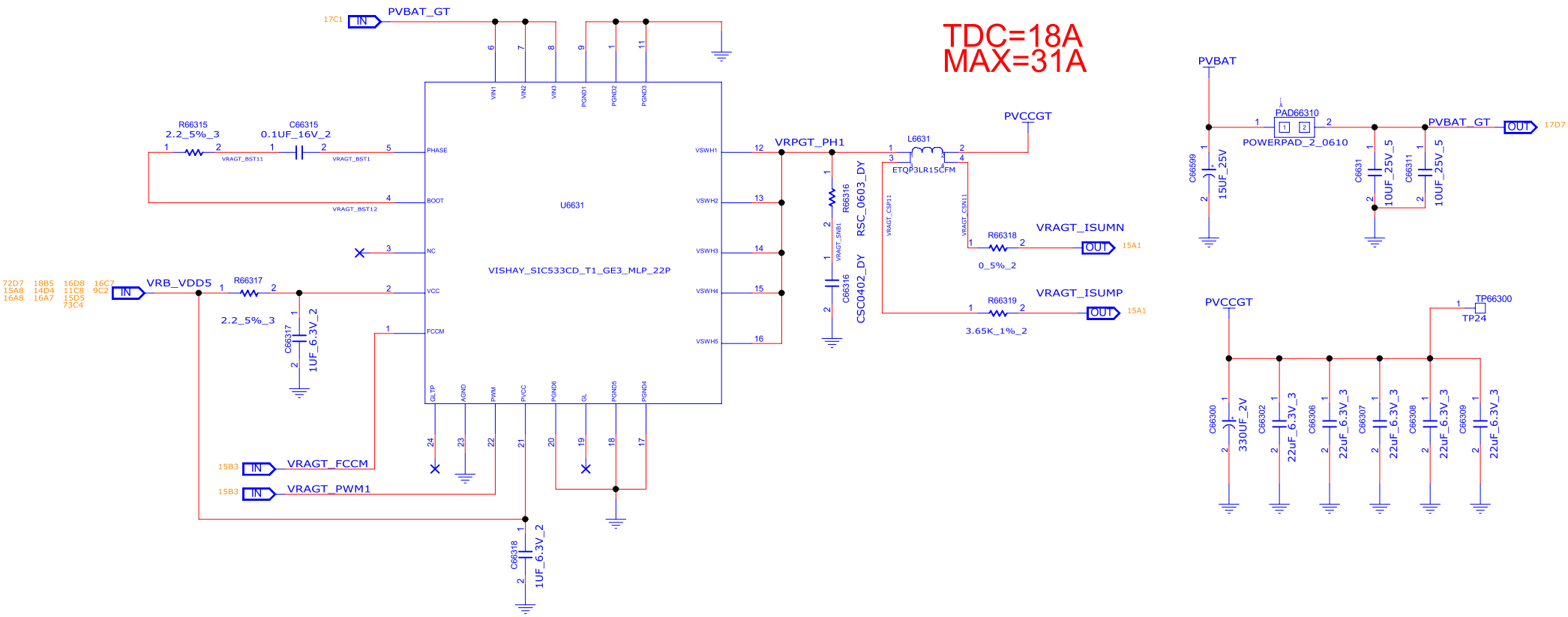

3/2 CHANGE

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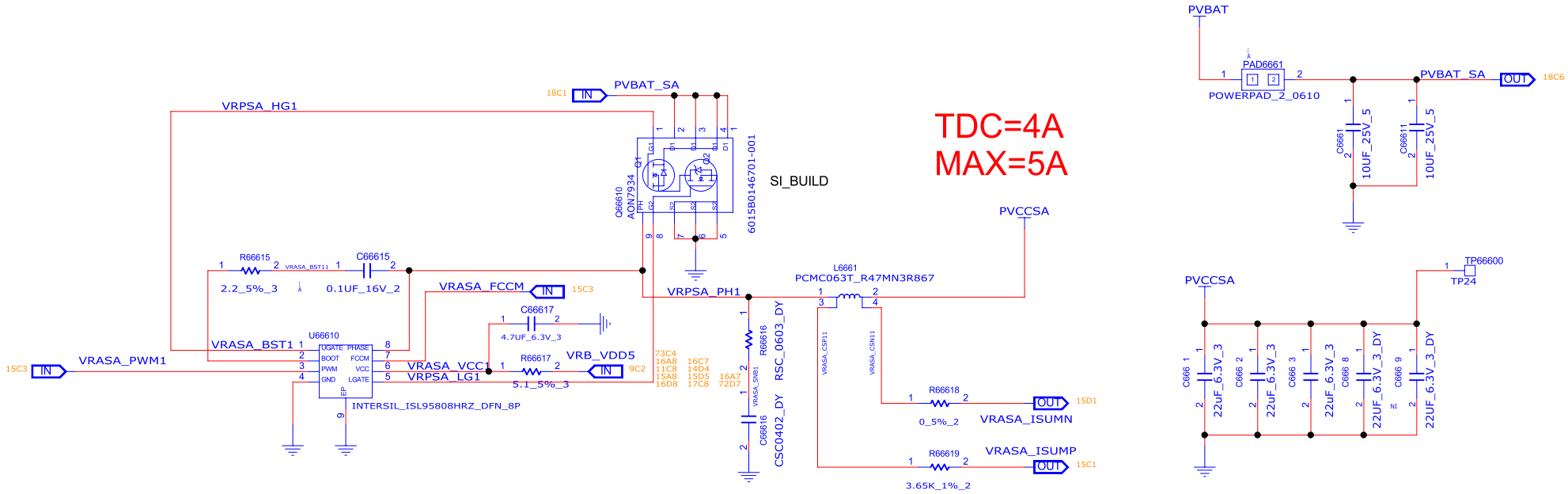

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3V & 5V

P3V3_LDO
R7 10K_5%_2
R7 01 SHORT_0402_5
EN_5V OUT 9C6 19B8 20C7
36D6 IN EC_PW_ON# G Q7000 PANJIT_2N7002KW_3P
R7019 100K_5%_2
D7 00 60110GA0367T DIODE-BAT54-TAP-PHP
6/13 ADD
IN P5VAUXON R7 9 1K_5%_2
D7002 60110GA0367T DIODE-BAT54-TAP-PHP
P3V3_LDO
R7 02 10K_5%_2
R70 5_2 10K_5%_2
EN_3V OUT
6/15 MODIFIED
C71 6 0.1UF_16V_2
IN AOAC_ON# R70 8 0_5%_2 G Q7001 PANJIT_2N7002KW_3P
6/13 ADD
R7 3 100K_5%_2
R7 6 0_5%_2

DDR

D70 1 DIODE-BAT54-TAP-PHP
R7017 100_5%_2
EN_2V5 OUT 12C5
IN SLP_S4#_3R R7012 330K_5%_2
C7003 0.22UF_6.3V_2
P3V3A
R7121 10K_5%_2_DY
IN 2V5_PG R7118 SHORT_0402_5
EN_VDDQ OUT 11C6
IN SLP_S4#_3R R7018 10K_5%_2
IN SLP_S3#_3R R7 23 47K_5%_2_DY
EN_VTT OUT 11C6
C7009 CSC0402_DY
IN DDR_VTT_PG_CTR R7 07 47K_5%_2
P3V3A
R7 13 10K_5%_2
11C6 IN VDDQ_PG OUT

P1V8A

9C6 IN EN_5V R7021 47K_5%_2_DY
EN_1V8A OUT 13C6
8C7 IN EN_3V R7037 47K_5%_2
C7 2 0.1UF_16V_2
EN5V CHANGE TO EN3V
6/14 CHANGE
P3V3A
R7 25 10K_5%_2
19B6 13B6 19A8 IN P1V8A_PG P1V8A_PG OUT

P1V A

31B2 IN EXT_PWR_GATE# R7 24 0_5%_2_DY
13B6 19A8 IN P1V8A_PG R7 22 SHORT_0402_5
EN_1V0 OUT 14C7
C7 21 CSC0402_DY
P3V3A
R7020 10K_5%_2
19B6 14C7 36C6 IN 1V0_PG 1V0_PG OUT

PVCORE

EN_PVCORE IN 36E6 31D7
R66000 SHORT_0402_5
VRAVR_ON OUT 15C6
R66001 RSC_0402_DY
P3V3S
R660 2 10K_5%_2
PVCORE_PG OUT 40C4 15C6 31A8

EC POWER CONTROL
THERMAL SHUTDOWN

6/15 MODIFIED

P3V3_LDO
R7 29 10K_5%_2
Q7 05 Q7 03
TO EC POWER
P3V3_LDO_EC OUT 36E1 36E8
DIODES_DMP2305U_SOT25_3P
C7 11 CSC0402_DY
6/15 ADD
P5VAUXON_MOS
PANJIT_2N7002KW_3P
D7003 DIODE-BAT54-TAP-PHP
P5VAUXON IN 36D6 19D8
R7015 51K_1%_2
C7010 0.022UF_16V_2
9C6 IN EN_5VLDO R7041 SHORT_0402_15
TP700

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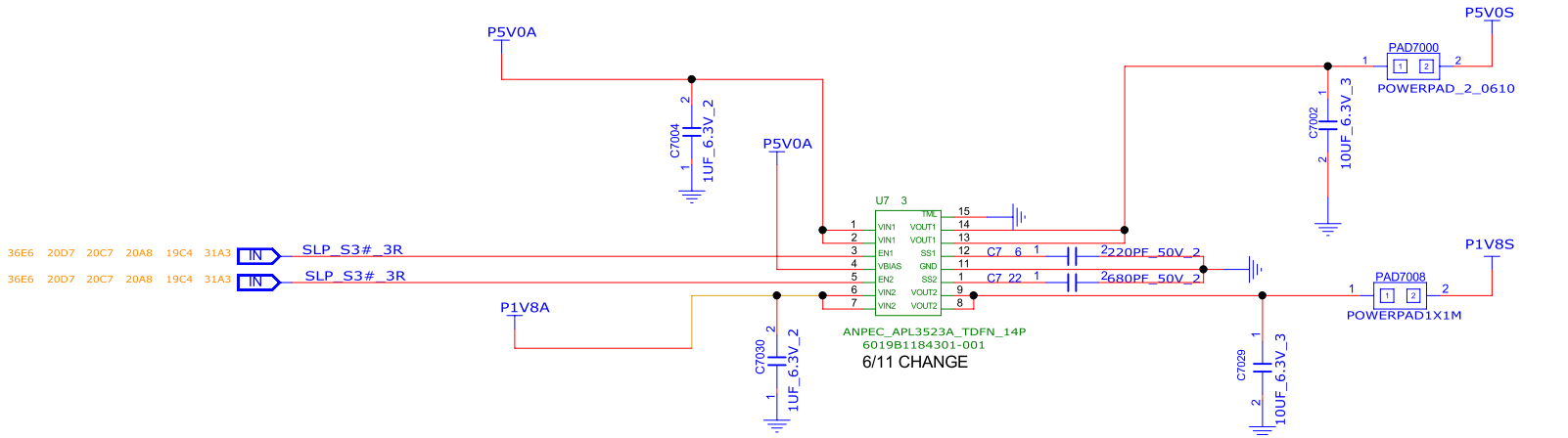

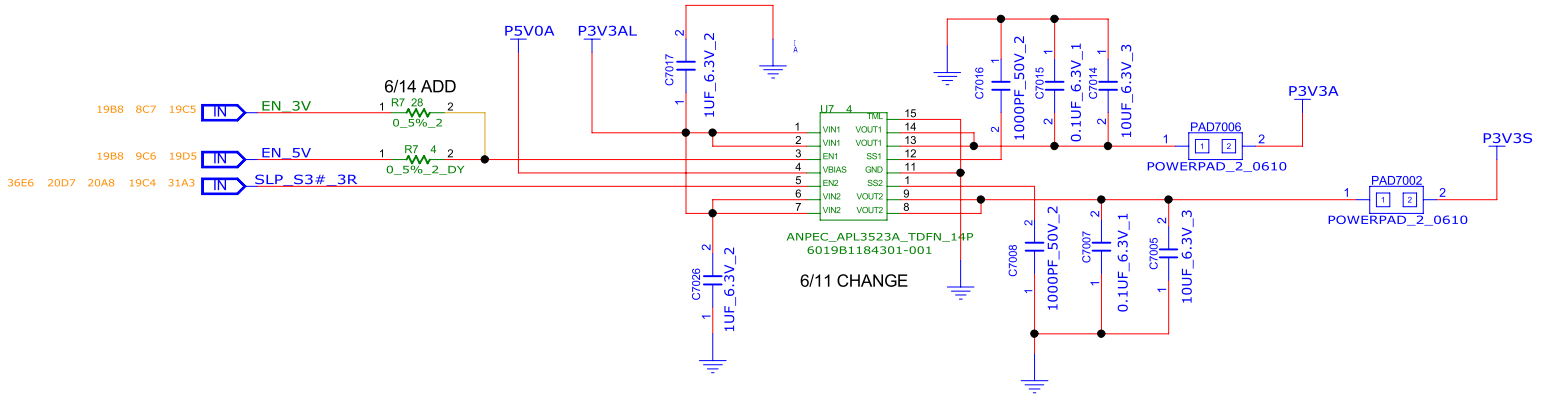

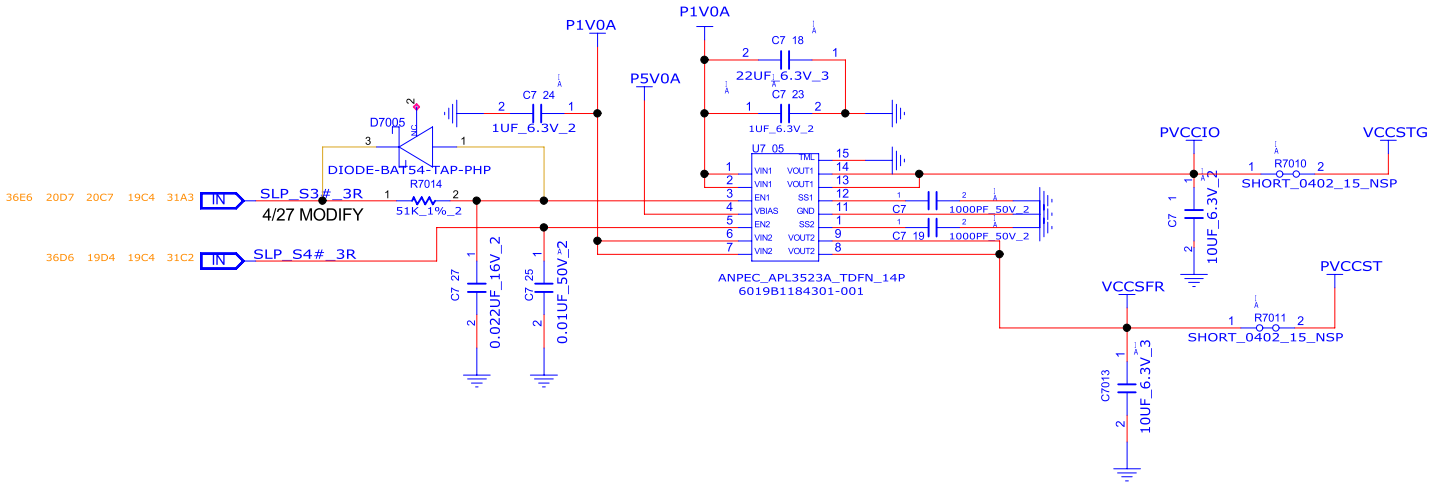

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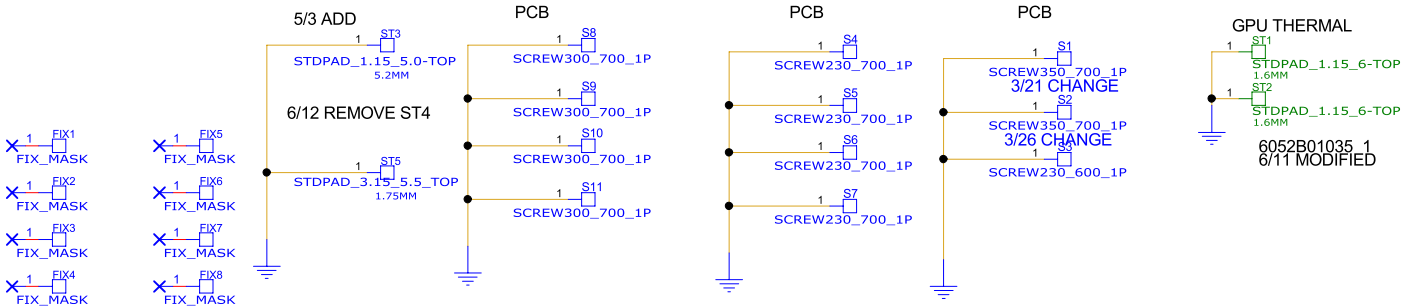
REFERENCE 0~49(PCB SCREW)



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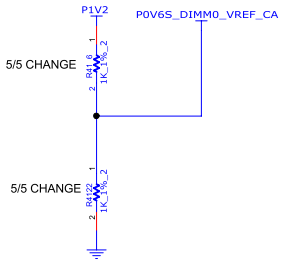
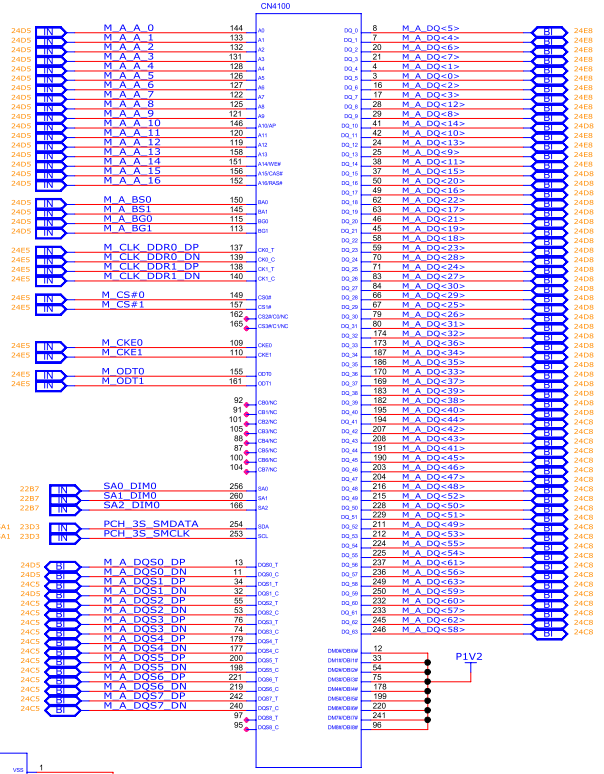
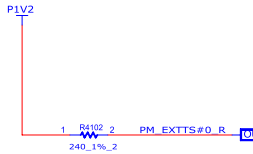
REFERENCE 4100~4299(DDR)

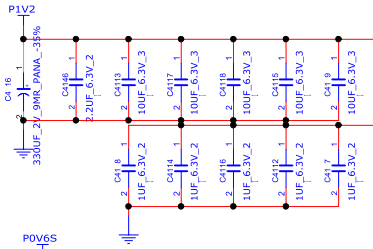
CHA SODIMM H=4.15MM

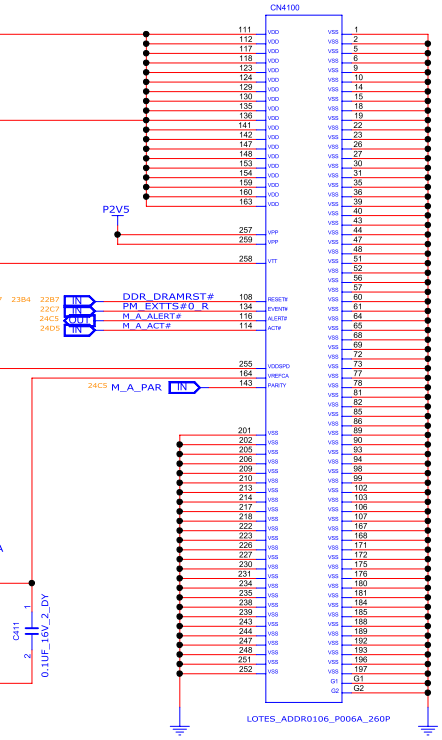


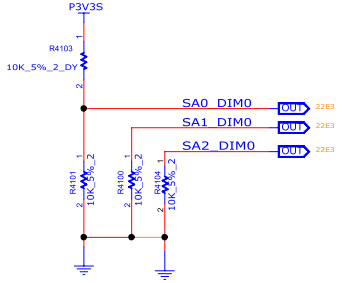


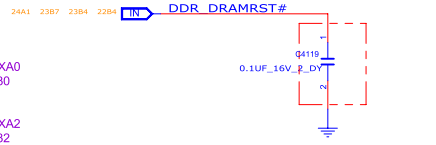
BOM USE 6026B 333201
6/11 CHANGE



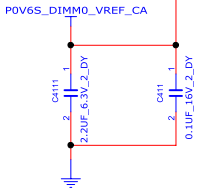








PLACE C4119 WITHIN 2 MILS
FROM THE SODIMM - (CN41)



NOTE:

IF SA _DIM0= , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30

IF SA _DIM0=1 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

REFERENCE NUMBER:4100~4199

INVENTEC

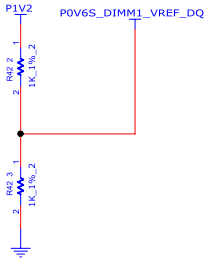
MODEL,PROJECT,FUNCTION
Block Diagram

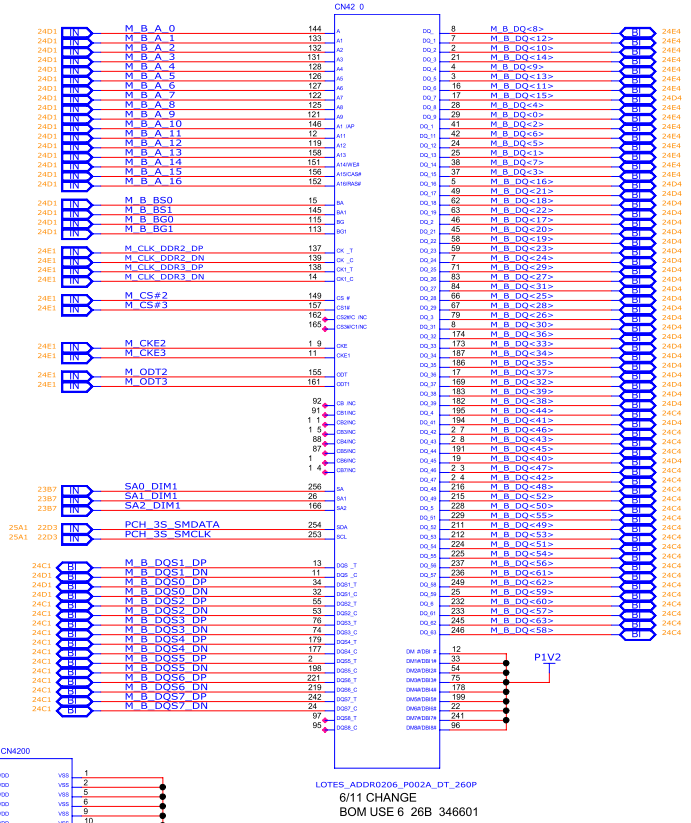
CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

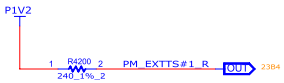
SHEET 22 of 79

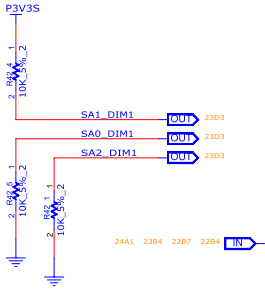
CHB SODIMM 1 H=4.15MM

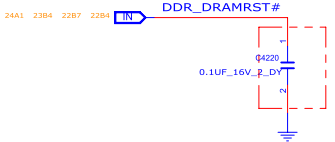




6/11 CHANGE
BOM USE 6 26B 346601

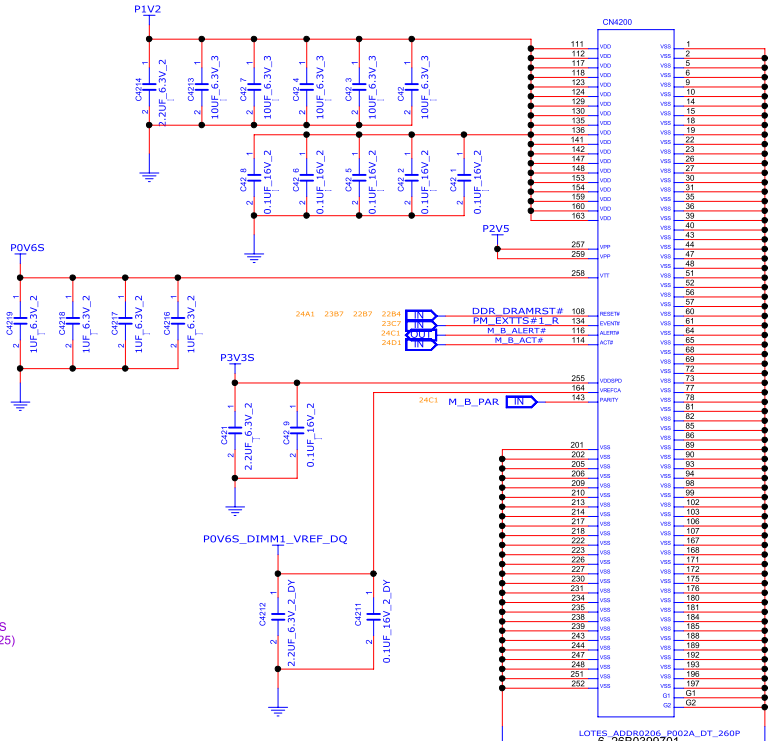






NOTE:
SO-DIMMB SPD ADDRESS IS 0XA4
SO-DIMMB TS ADDRESS IS 0X34

PLACE C4120 WITHIN 200 MILS
FROM THE SODIMM - 1 (CN4125)



6 26B0339701
3/13 CHECK

REFERENCE NUMBER:42 ~4299

INVENTEC

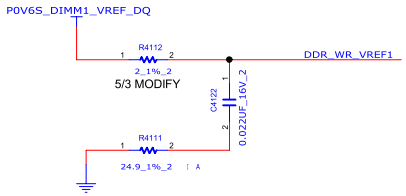
MODEL,PROJECT,FUNCTION
Block Diagram

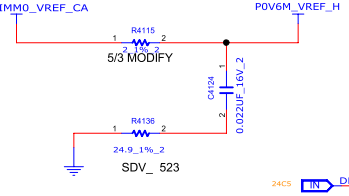
CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

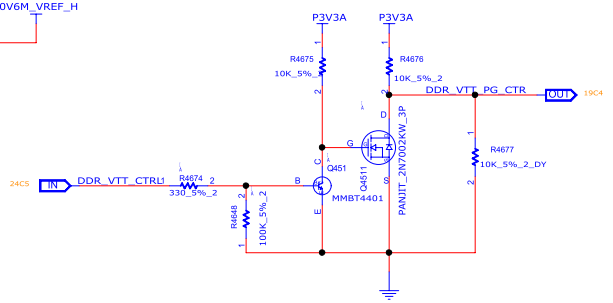
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

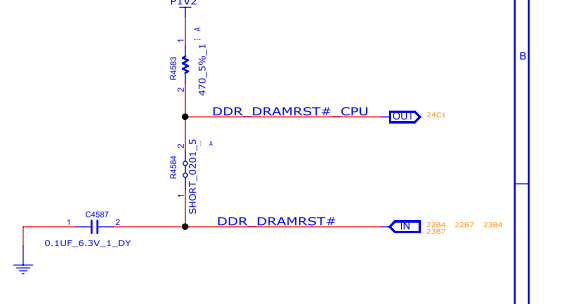
SHEET 22 of 29

REFERENCE:45 ~4949









INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

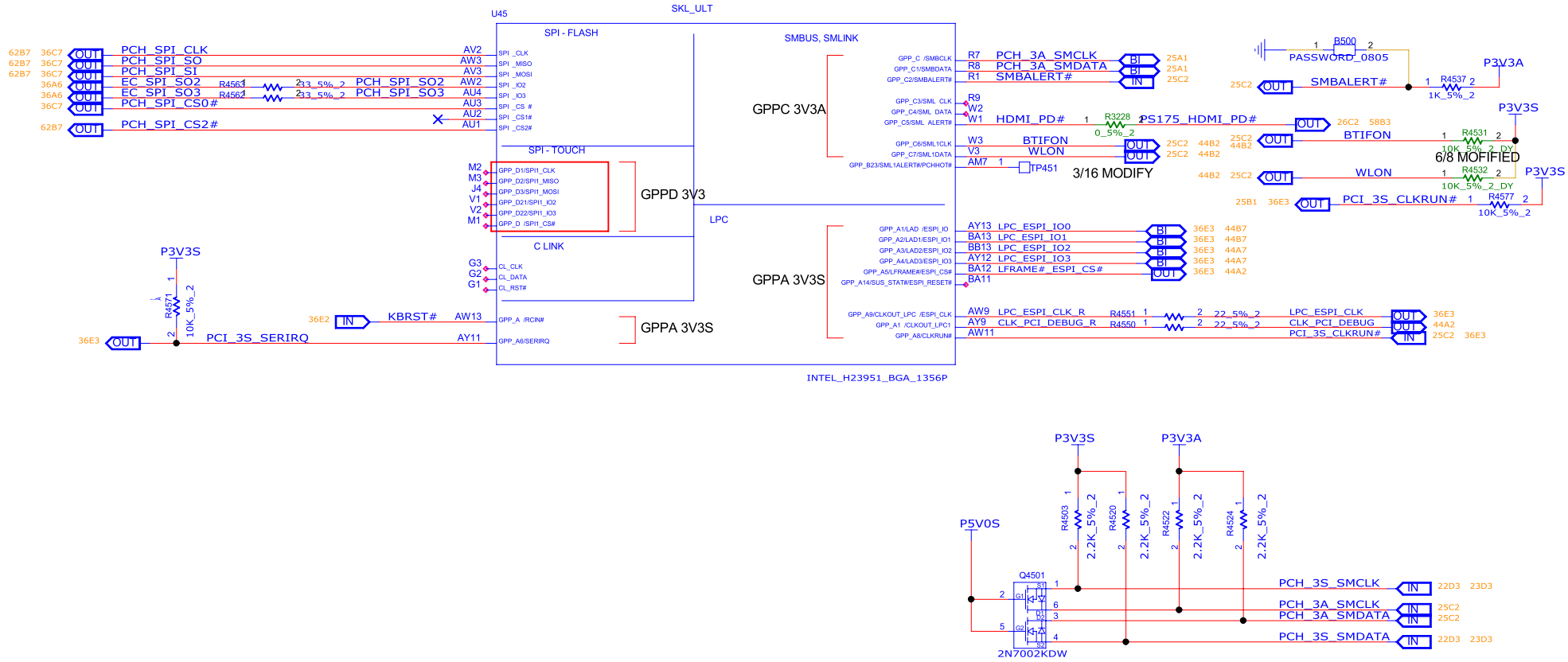
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

CHANGE N	XXX	DATE	
PCB P/N	60.xxxxx.xxxx	PCB VER 2	

SHEET of

7e2 6 f 91126 1d7 3a62b79 361

543016 6 .3.31: ALL UNUSED GPIOS (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION



CHANGE by	XENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XVER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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7e2 6 f 91126 1d7 3a62b79 361

7e2 6 f 91126 1d7 3a62b79 361

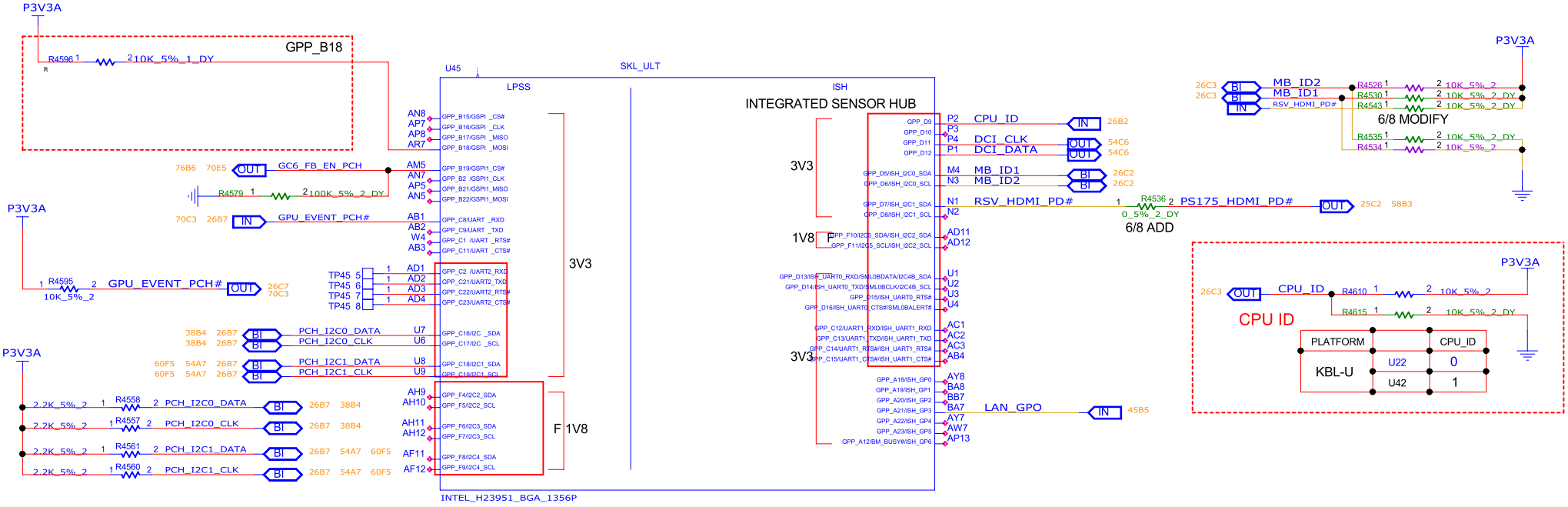
REFERENCE 4700~4949(PCH)

REFERENCE 4700~4949(PCH)

543 16 6 .3.31: ALL UNUSED GPIOS (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

543016 60.3.31: ALL UNUSED GPIOS (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

MB_ID	MB_ID2	MB_ID1
X01	0	0
AX1	0	1
AX2	1	0
MP	1	1



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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7e2 6 f 91126 1d7 3a62b79 361

543016 60.3.31: ALL UNUSED GPIOS (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

3/21 MODIFIED

INTEL_H23951_BGA_1356P

INTEL_H23951_BGA_1356P

GPP_B

DGPU PRSNT#

	DGPU_PRSNT#
DIS	0
UMA	1

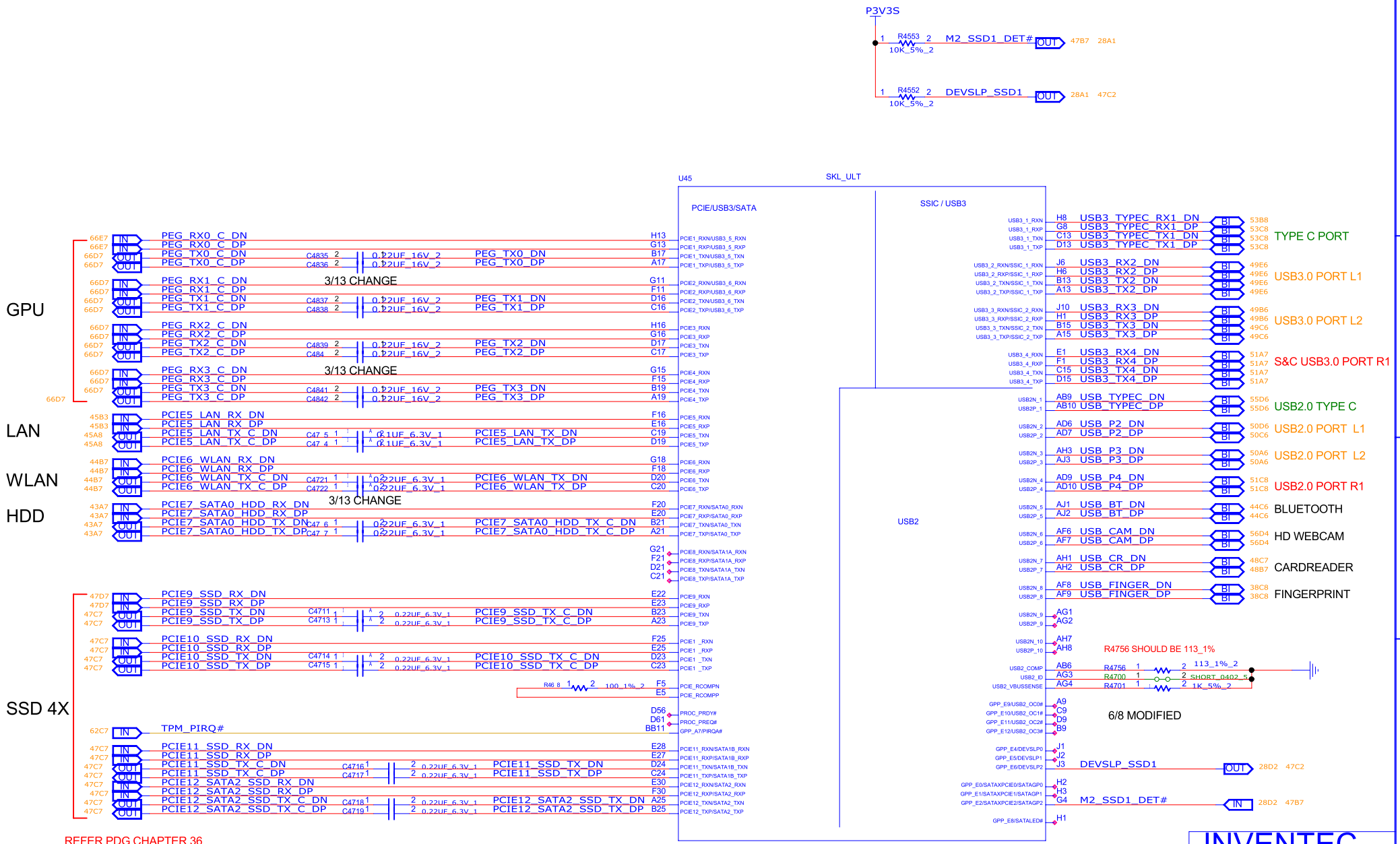
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 27 of 79


P3V3S
R4553 2 M2_SSD1_DET# OUT 47B7 28A1
10K_5%_2
R4552 2 DEVSLP_SSD1 OUT 28A1 47C2
10K_5%_2
U45
SKL_ULT
PCIE/USB3/SATA
SSIC / USB3
USB2
INTEL_H23951_BGA_1356P
GPU
LAN
WLAN
HDD
SSD 4X
3/13 CHANGE
PEG_RX0_C_DN
PEG_RX0_C_DP
PEG_TX0_C_DN
PEG_TX0_C_DP
PEG_RX1_C_DN
PEG_RX1_C_DP
PEG_TX1_C_DN
PEG_TX1_C_DP
PEG_RX2_C_DN
PEG_RX2_C_DP
PEG_TX2_C_DN
PEG_TX2_C_DP
PEG_RX3_C_DN
PEG_RX3_C_DP
PEG_TX3_C_DN
PEG_TX3_C_DP
PCIE5_LAN_RX_DN
PCIE5_LAN_RX_DP
PCIE5_LAN_TX_C_DN
PCIE5_LAN_TX_C_DP
PCIE6_WLAN_RX_DN
PCIE6_WLAN_RX_DP
PCIE6_WLAN_TX_C_DN
PCIE6_WLAN_TX_C_DP
PCIE7_SATA0_HDD_RX_DN
PCIE7_SATA0_HDD_RX_DP
PCIE7_SATA0_HDD_TX_DN
PCIE7_SATA0_HDD_TX_DP
PCIE9_SSD_RX_DN
PCIE9_SSD_RX_DP
PCIE9_SSD_TX_DN
PCIE9_SSD_TX_DP
PCIE10_SSD_RX_DN
PCIE10_SSD_RX_DP
PCIE10_SSD_TX_DN
PCIE10_SSD_TX_DP
PCIE11_SSD_RX_DN
PCIE11_SSD_RX_DP
PCIE11_SSD_TX_C_DN
PCIE11_SSD_TX_C_DP
PCIE12_SATA2_SSD_RX_DN
PCIE12_SATA2_SSD_RX_DP
PCIE12_SATA2_SSD_TX_C_DN
PCIE12_SATA2_SSD_TX_C_DP
TPM_PIRQ#
USB3_TYPEC_RX1_DN
USB3_TYPEC_RX1_DP
USB3_TYPEC_TX1_DN
USB3_TYPEC_TX1_DP
TYPE C PORT
USB3_RX2_DN
USB3_RX2_DP
USB3_TX2_DN
USB3_TX2_DP
USB3.0 PORT L1
USB3_RX3_DN
USB3_RX3_DP
USB3_TX3_DN
USB3_TX3_DP
USB3.0 PORT L2
USB3_RX4_DN
USB3_RX4_DP
USB3_TX4_DN
USB3_TX4_DP
S&C USB3.0 PORT R1
USB_TYPEC_DN
USB_TYPEC_DP
USB2.0 TYPE C
USB_P2_DN
USB_P2_DP
USB2.0 PORT L1
USB_P3_DN
USB_P3_DP
USB2.0 PORT L2
USB_P4_DN
USB_P4_DP
USB2.0 PORT R1
USB_BT_DN
USB_BT_DP
BLUETOOTH
USB_CAM_DN
USB_CAM_DP
HD WEBCAM
USB_CR_DN
USB_CR_DP
CARDREADER
USB_FINGER_DN
USB_FINGER_DP
FINGERPRINT
R4756 SHOULD BE 113_1%
R4756 113_1%_2
R4700 SHORT_0402_5
R4701 1K_5%_2
6/8 MODIFIED
DEVSLP_SSD1
M2_SSD1_DET#
REFER PDG CHAPTER 36
DESIGN CONSTRAINT: FOR PCIE* GEN 3/ SATA MULTIPLEXED CONFIGURATION, MOTHERBOARD TX REQUIRES A 220 NF
AC CAPACITOR AND NO AC CAPACITOR IS REQUIRED FOR MOTHERBOARD RX CHANNEL
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 28 of 79
CHANGE by <XXXG>
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx
PCB VER <XXXR>

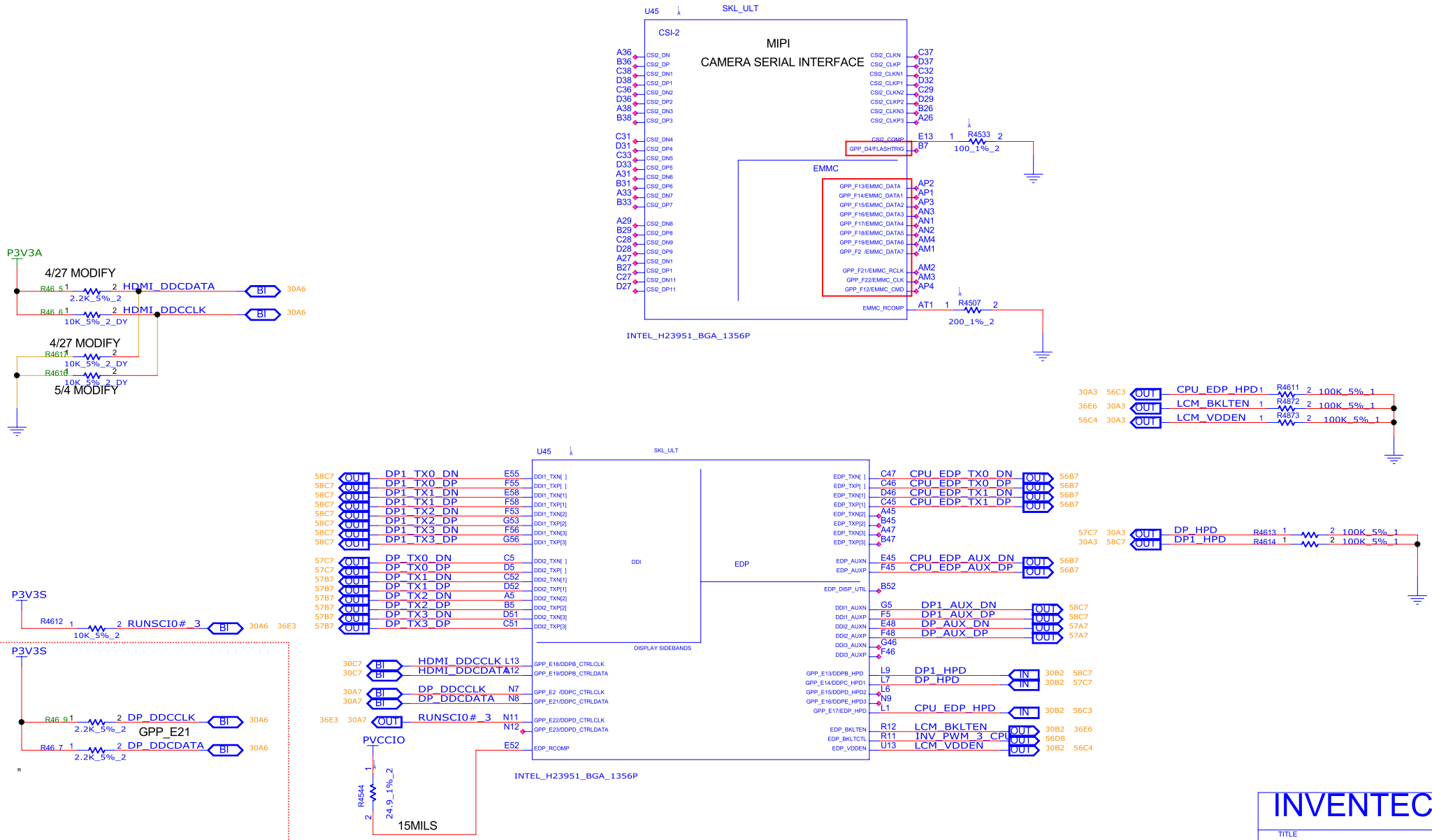
7e2 6 f 91126 1d7 3a62b79 361

RTC

P3V3S
P3V3S_WLAN
P3V3A_LAN
P3V3_LDO
P3V3AL
P3V3_RTC
P1V0A
U4500 SKL_ULT
CLOCK SIGNALS
INTEL_H23951_BGA_1356P
CLK_PEG_DN
CLK_PEG_DP
CLKREQ_GPU#
CLK_PCIE_SSD1_DN
CLK_PCIE_SSD1_DP
CLKREQ_SSD1#
CLK_LAN_DN
CLK_LAN_DP
CLKREQ_LAN#
CLK_PCIE_WLAN_DN
CLK_PCIE_WLAN_DP
CLKREQ_WLAN#
R4708 1.5K_5%_2
R4703 1.5K_5%_2_DY
6/14 MODIFIED
R4723 45.3K_1%_2
D475 BAT54C_30V_0_6A
3/19 CHANGE
R4834 20K_1%_1
R4845 20K_1%_1
R4832 1K_5%_2
CN4700 P3V3_RTC_BATTERY
LOTES_AAA_BAT_054_P04_2P
6_26B_0_8801
4/27 MODIFY
FOR U2+2 CPU
SUSCLK32_WLAN
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
RTCX1
RTCX2
SRTC_RST#
RTC_RST#
RTCRST#_0603
1UF_6.3V_1
THE 24 MHZ (50 OHM ESR) XTAL USED FOR SKYLAKE-U.
U4500 SKL_ULT
RESERVED SIGNALS-1
CFG<0>
CFG<1>
CFG<2>
CFG<3>
CFG<4>
CFG<5>
CFG<6>
CFG<7>
CFG<8>
STRAPPING:
DP ENABLE/DISABLE
: ENABLED
R4523 1K_5%_1
R4519 49.9K_1%_2
R4841 1.5K_5%_2
TD_IREF
CFG_RCOMP
ITP_PMODE
RCOMP NEED CLOSED TO CPU AT 5 MIL
R4513 SHORT_0402_15
INTEL_H23951_BGA_1356P
FOR U22
BOM CHANGE
R4899 33_5%_2_DY
R4897 33_5%_2_DY
R4898 1M_5%_2_DY
X4751 24MHZ_12PF_DY
C4828 15PF_50V_2_DY
C4826 15PF_50V_2_DY
R4862 10M_5%_2
X4750 32.768KHZ_12.5PF
C4788 15PF_50V_2
C4767 15PF_50V_2
SRCCLKRQ[5:0]# CAN BE ASSIGNED TO DIFFERENT SRC CLOCKS USING FW SETTINGS AND MAY NOT NECESSARILY CORRESPOND TO THE SAME PCI EXPRESS CLOCK NUMBER
ROOT PORTS WHILE USING ANY OF THE CLKOUT_SRC_P/NDIFFERENTIAL PAIRS.
REFERENCE:4500~4949

INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET of 29 79
CHANGE by XXX
PCB P/N 6MB0xxxxxxxx
DATE
PCB VER XVER
OCT-2002

7e2 6 f 91126 1d7 3a62b79 361



CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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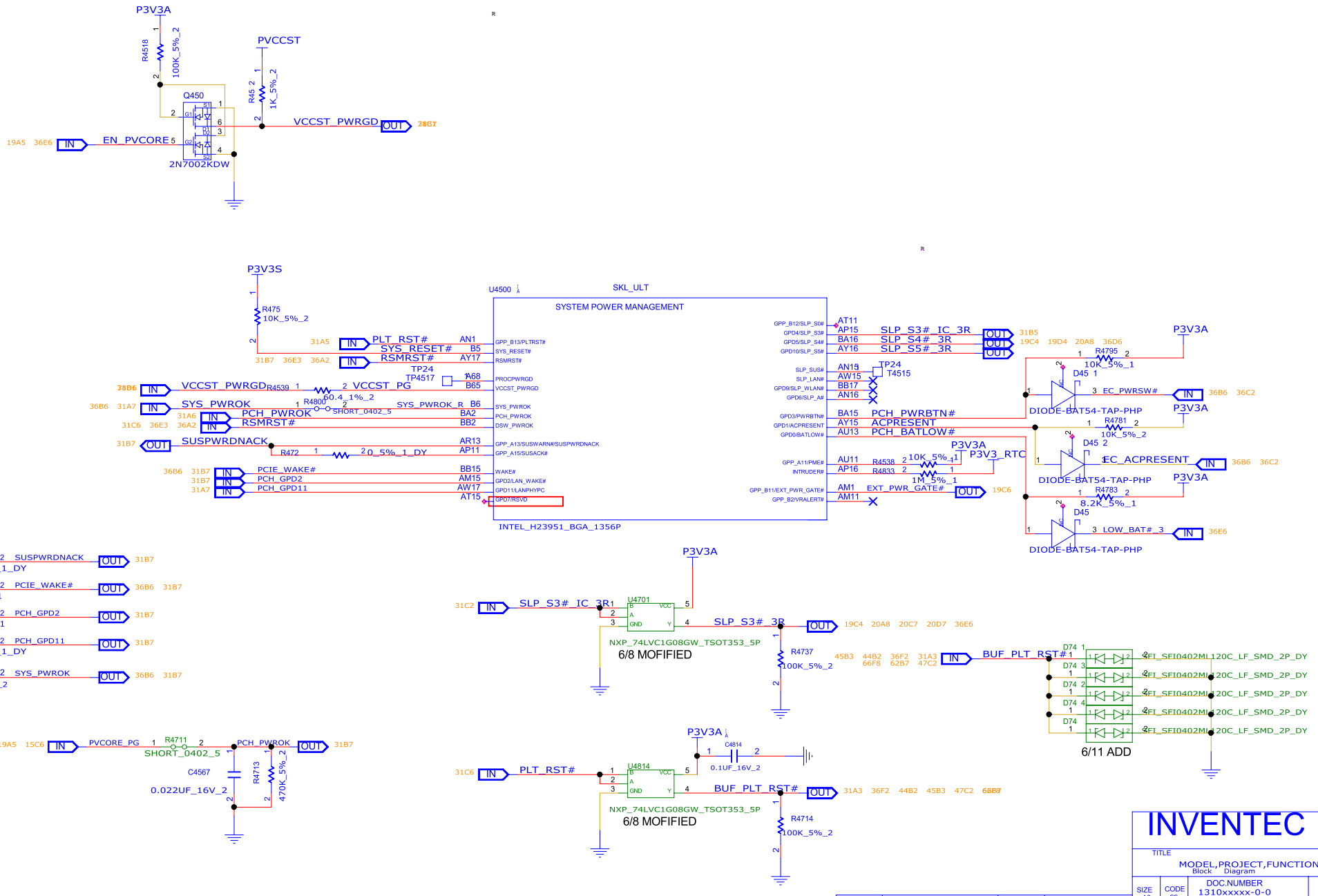


CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

INVENTEC

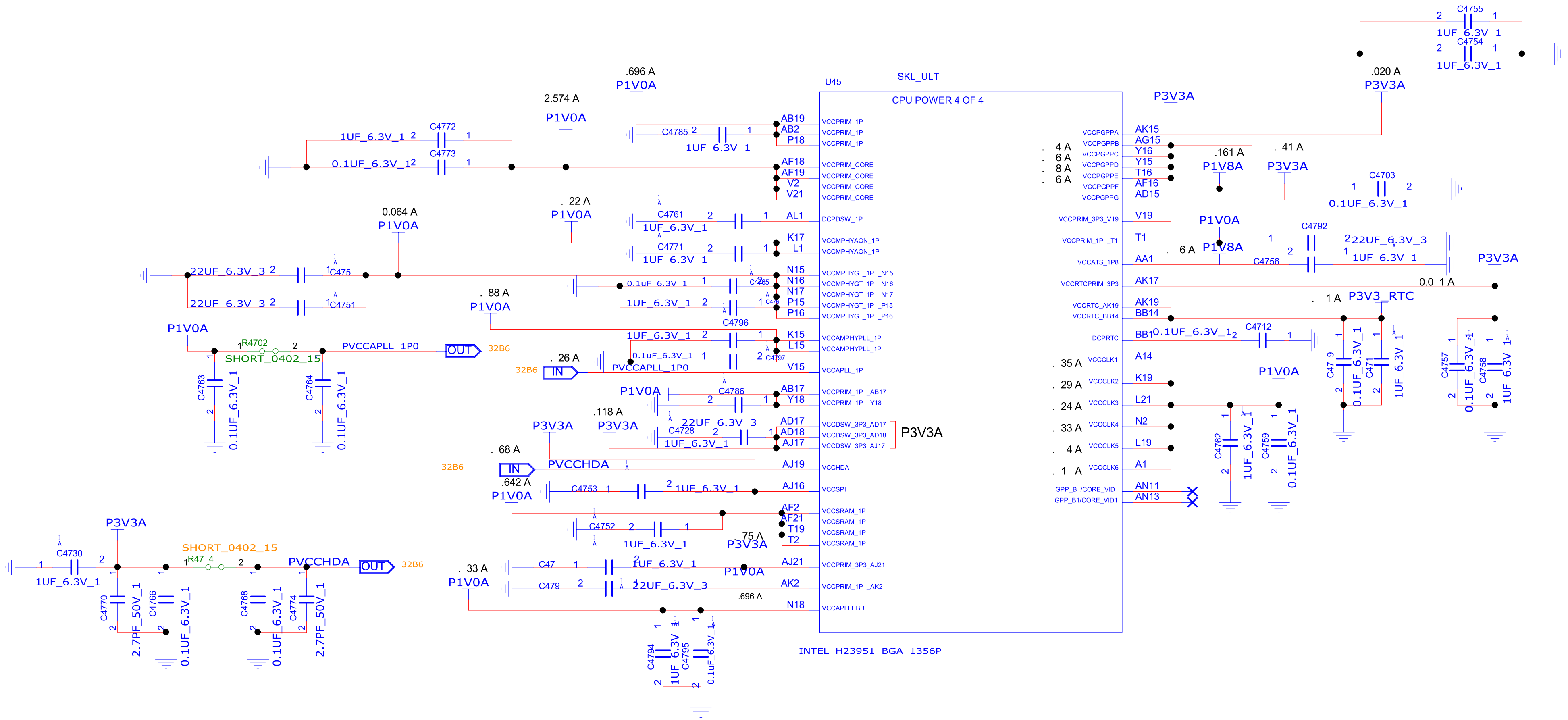
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 31 of 79

7e2 6 f 91126 1d7 3a62b79 361

REFERENCE 47 ~4949(PCH)



CHANGE by	XXX	DATE	
PCB P/N	6QNSxxxxxxxxx	PCB VER	X/ER... OCT-2002

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 32 of 79

7e2 6 f 91126 1d7 3a62b79 361

32 A
PVCORE

PVCORE

SI 12 2

U45 SKL_ULT
CPU POWER 1 OF 4
INTEL_H23951_BGA_1356P

SDV_ 523

2.2UF 0402 * 1 PCS
PVCORE

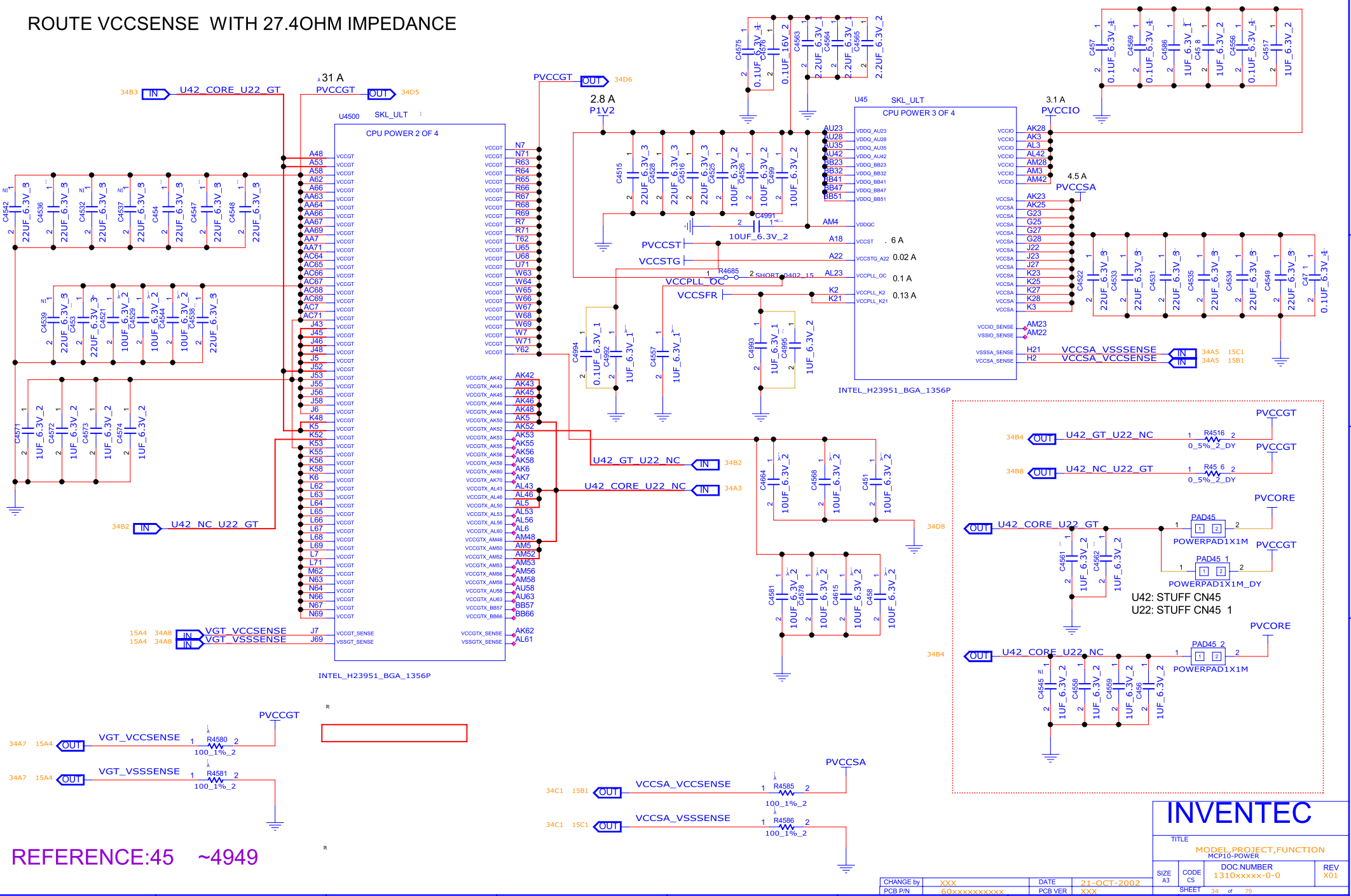
2.2UF 402 * 1 PCS
PVCCSA

2.2UF 4 2 * 1 PCS
PVCORE

2.2UF 402 * 1 PCS
PVCCGT

PVCCST
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
VCCSENSE
VSSSENSE
VCCSTG

ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
MCP10-POWER

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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7e2 6 f 91126 1d7 3a62b79 361

SKL_ULT U4500

GND 1 OF 3

A5 A67 A70 A2 A4 AA65 AA68 AB15 AB16 AB18 AB21 AB8 AD13 AD16 AD19 AD20 AD21 AD62 AD8 AE64 AE65 AE66 AE67 AE68 AE69 AF1 AF10 AF15 AF17 AF2 AF4 AF63 AG16 AG17 AG18 AG19 AG20 AG21 AG71 AH13 AH6 AH63 AH64 AH67 AJ15 AJ18 AJ20 AJ4 AK11 AK16 AK18 AK21 AK22 AK27 AK63 AK68 AK69 AK8 AL2 AL28 AL32 AL35 AL38 AL4 AL45 AL48 AL52 AL55 AL58 AL64

AL65 AL66 AM13 AM21 AM25 AM27 AM43 AM45 AM46 AM55 AM60 AM61 AM68 AM71 AM8 AN20 AN23 AN28 AN30 AN32 AN33 AN35 AN37 AN38 AN40 AN42 AN58 AN63 AP10 AP18 AP20 AP23 AP28 AP32 AP35 AP38 AP42 AP58 AP63 AP68 AP70 AR11 AR15 AR16 AR20 AR23 AR28 AR35 AR42 AR43 AR45 AR46 AR48 AR5 AR50 AR52 AR53 AR55 AR58 AR63 AR8 AT2 AT20 AT23 AT28 AT35 AT4 AT42 AT56 AT58

INTEL_H23951_BGA_1356P

SKL_ULT U4500

GND 2 OF 3

AT63 AT68 AT71 AU10 AU15 AU20 AU32 AU38 AV1 AV68 AV69 AV70 AV71 AW10 AW12 AW14 AW16 AW18 AW21 AW23 AW26 AW28 AW30 AW32 AW34 AW36 AW38 AW41 AW43 AW45 AW47 AW49 AW51 AW53 AW55 AW57 AW6 AW60 AW62 AW64 AW66 AW8 AY66 B10 B14 B18 B22 B30 B34 B39 B44 B48 B53 B58 B62 B66 B71 BA1 BA10 BA14 BA18 BA2 BA23 BA28 BA32 BA36 F68 BA45

BA49 BA53 BA57 BA6 BA62 BA66 BA71 BB18 BB26 BB30 BB34 BB38 BB43 BB55 BB6 BB60 BB64 BB67 BB7 C1 C25 C5 D10 D11 D14 D18 D22 D25 D26 D30 D34 D39 D44 D45 D47 D48 D53 D58 D6 D62 D66 D69 E11 E15 E18 E21 E46 E50 E53 E56 E6 E65 E71 F1 F13 F2 F22 F23 F27 F28 F32 F33 F35 F37 F38 F4 F40 F42 BA41

INTEL_H23951_BGA_1356P

SKL_ULT U4500

GND 3 OF 3

F8 G10 G22 G43 G45 G48 G5 G52 G55 G58 G6 G60 G63 G66 H15 H18 H71 J11 J13 J25 J28 J32 J35 J38 J42 J8 K16 K18 K22 K61 K63 K64 K65 K66 K67 K68 K70 K71 L11 L16 L17

L18 L2 L20 L4 L8 N10 N13 N19 N21 N6 N65 N68 P17 P19 P20 P21 R13 R6 T15 T17 T18 T2 T21 T4 U10 U63 U64 U66 U67 U69 U70 V16 V17 V18 W13 W6 W9 Y17 Y19 Y20 Y21

INTEL_H23951_BGA_1356P

ST4412 STDPAD_1.15_6-TOP 1.6MM

ST4411 STDPAD_1.15_6-TOP 1.6MM

ST4413 STDPAD_1.15_6-TOP 1.6MM

ST4414 STDPAD_1.15_6-TOP 1.6MM

6_52B0103501
6/11 MODIFIED

35A6 OUT XTAL24_OUT_U42

U4500 SKL_ULT SPARE

AW69 AW68 AU56 AW48 C7 U12 U11 H11

RSVD_AW69 RSVD_AW68 RSVD_AU56 RSVD_AW48 RSVD_C7 RSVD_U12 RSVD_U11 RSVD_H11

RSVD_F6 RSVD_E3 RSVD_C11 RSVD_B11 RSVD_A11 RSVD_D12 RSVD_C12 RSVD_F52

F6 E3 C11 B11 A11 D12 C12 F52

XTAL24_IN_U42 IN 35A6

INTEL_H23951_BGA_1356P

For I²C Control Mode only(I2C_EN=H)

ADDR: I²C control bus address LSB. Internally pull down at 150kΩ, 3.3V I/O.

[ADDR] =

L: 0x20/0x21

H: 0x22/0x23

35B1 OUT XTAL24_IN_U42 R4895 33_5%_2

35A4 IN XTAL24_OUT_U42 R4896 33_5%_2

R4501 1M_5%_2

X4500 24MHZ_12PF 6018B0059001

C4579 15PF_50V_2

C4582 15PF_50V_2

FOR U4+2 CPU

BOM CHANGE

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION

Block Diagram

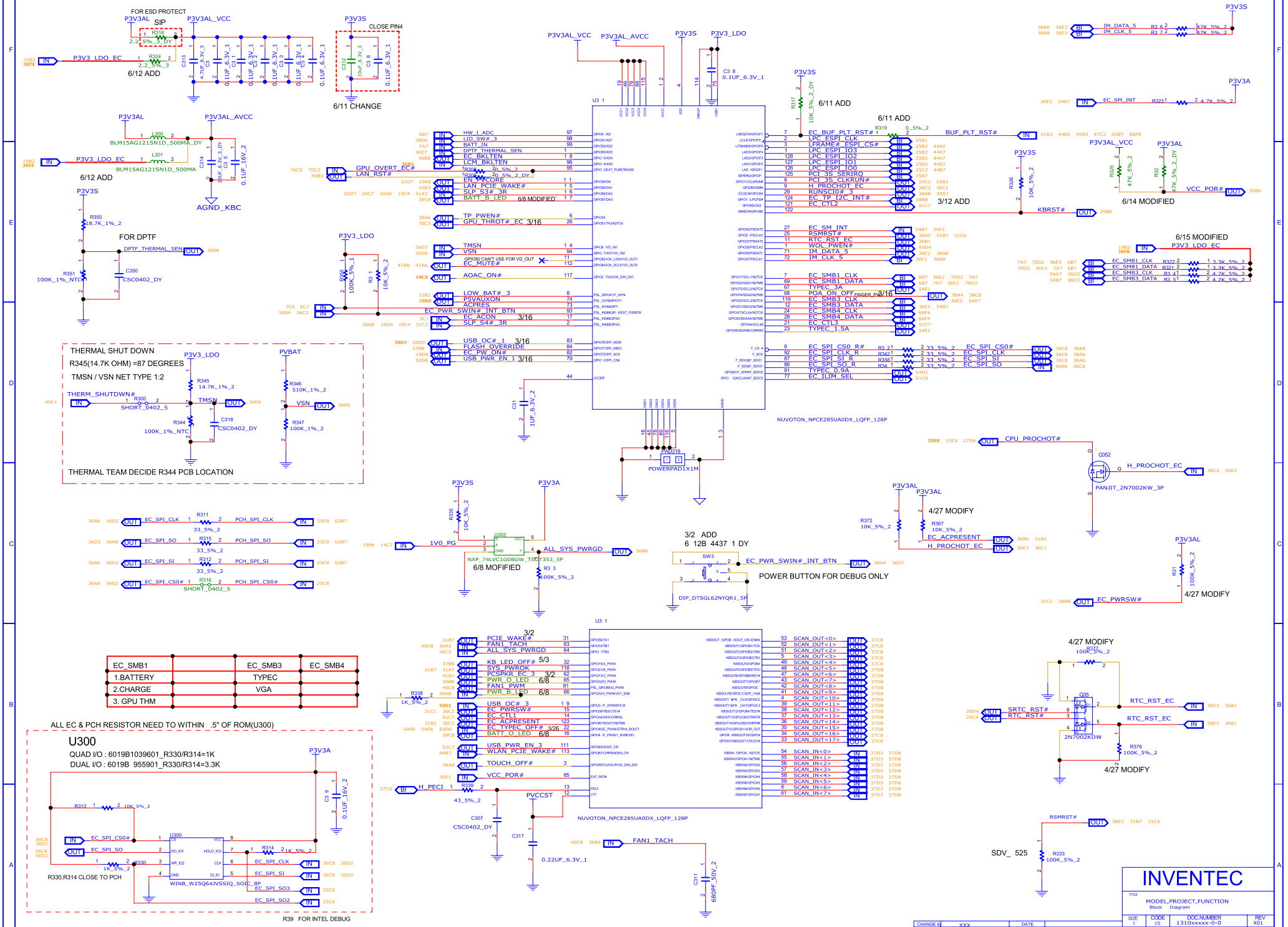
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 35 of 79

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

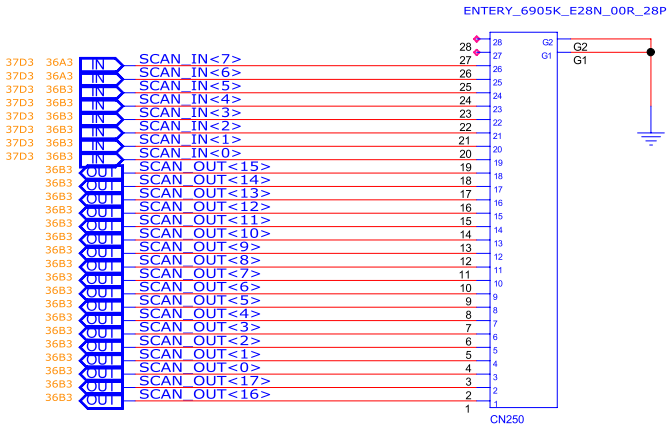
7e2 6 f 91126 1d7 3a62b79 361

REFERENCE 300~389(KBC)

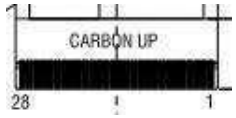


REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)

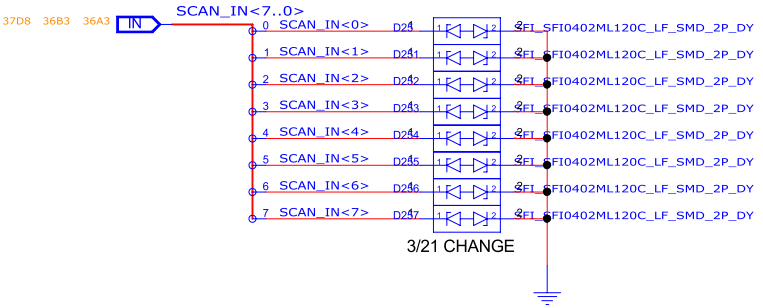
KEYBOARD CONN



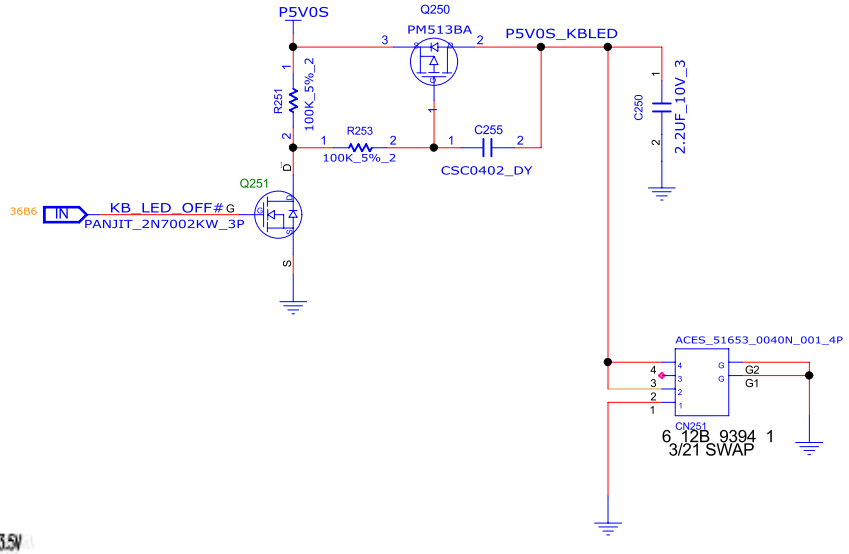
NEE TO CHANGE 6012B1002701
5/2 REVERSE



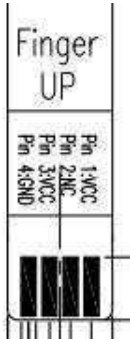
	14"
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



3/21 CHANGE



6_12B_9394_1
3/21 SWAP



VCC : +5V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

KEYBOARD LED CONN

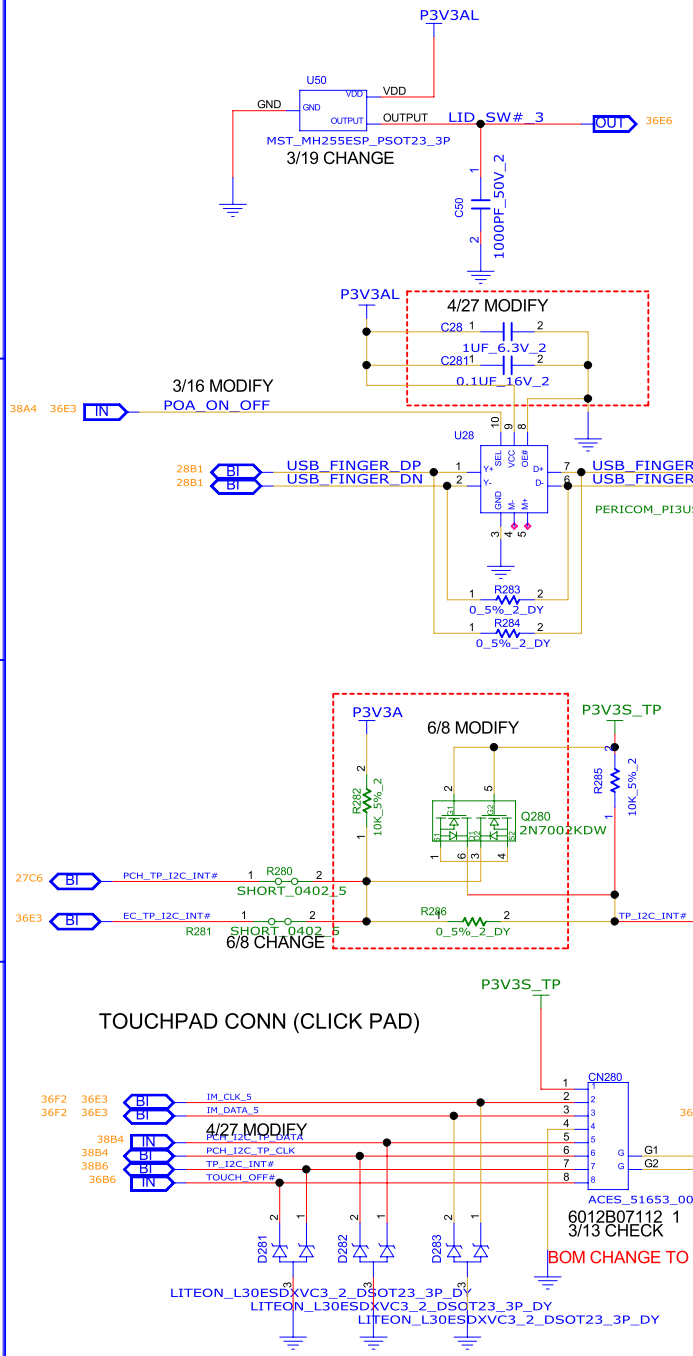
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	
PCB P/N	6PNG	PCB VER	XXX-OCT-2002

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET of 37 79



Signal Name	Active H/L	Direction	Description
POA_EN#	Low	Host to FPR	to activate the POA functionality
POA_POWERREQ	High	FPR to Host	To request additional power while acquiring/matching fingerprint
PWR_INT#	Low	FPR to Host	trigger power on event to EC
Auth_ERR	High	FPR to Host	to notify EC to error pattern LED or message
USB_SW_EN	High		Enable USB LS SW
FP_PWREN	High		control FP switch power enable

Truth Table

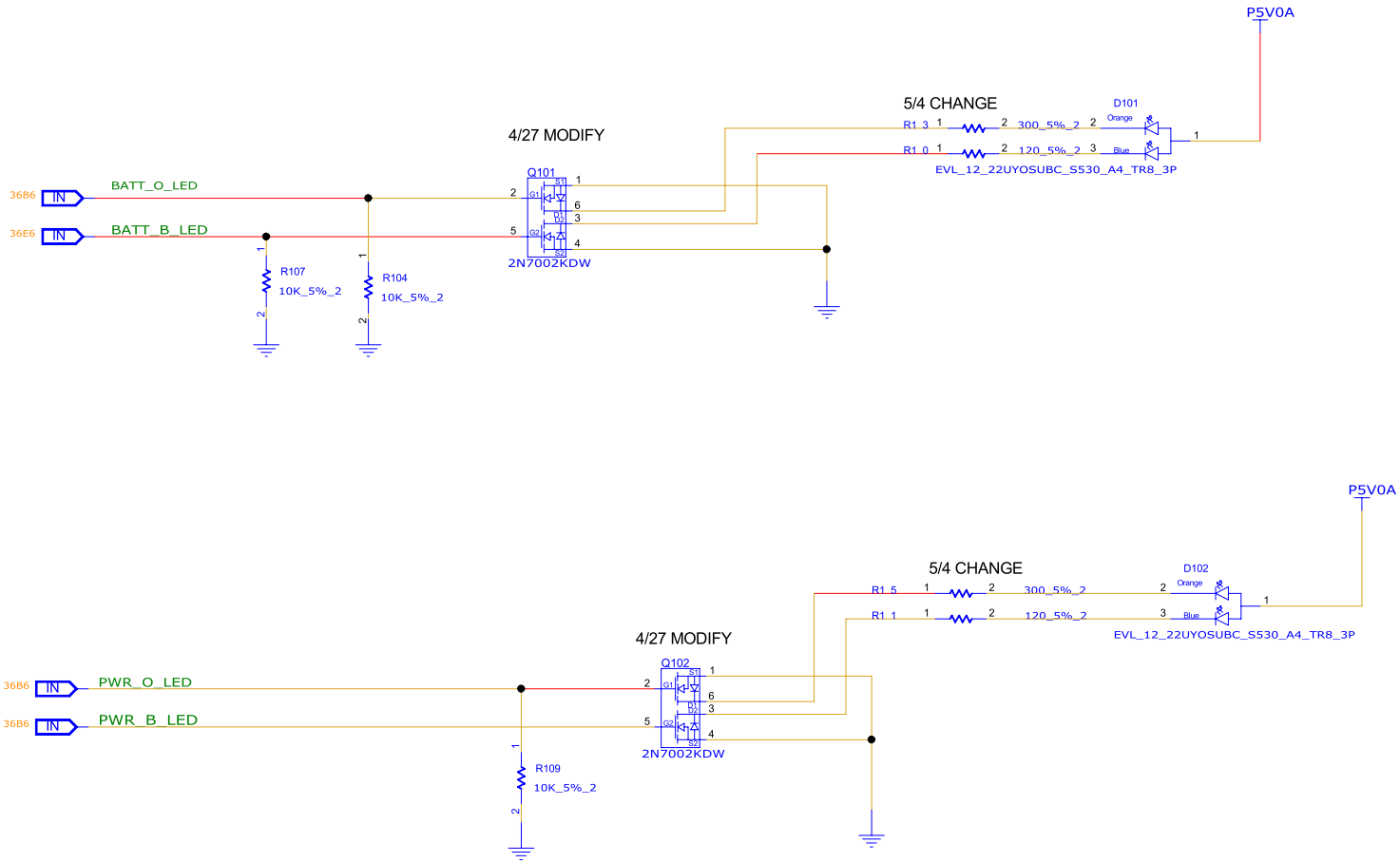
SEL	$\overline{OE}$	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

Pin Number	Pin Definition
1	+FP_VCC
2	USBP
3	USBN
4	GND
5	POA_EN
6	PWR_INT#
7	AUTH_ERR
8	POA_POWERREQ

Pin	Name	IO	Active	Description
1	VCC	POWER		Power Supply for this module
2	D+	I/O		USB data+
3	D-	I/O		USB data-
4	GND	GND		Ground
5	INT_BTN	O	Low	Button interrupt trigger; Short pulse in duration of 100 msec +/- 5%
6	Power_Notify	I		EC Power On/Off Notification; High: Power On, Low: Power Off
7	LED1	O		LED for R/G/B (optional)
8	LED2	O		LED for R/G/B (optional)

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 38 of 79			
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE		SIZE A3	DOC.NUMBER 1310xxxxx-0-0
PCB P/N	6PNGxxxxxxxx	PCB VER	XXX-OCT-2002	CODE CS	REV X01
				SHEET	of 39 79

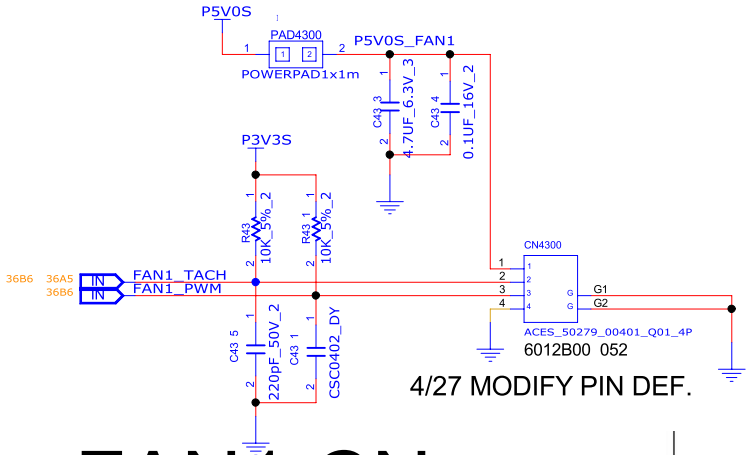
7e2 6 f 91126 1d7 3a62b79 361

REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)

NOTES :

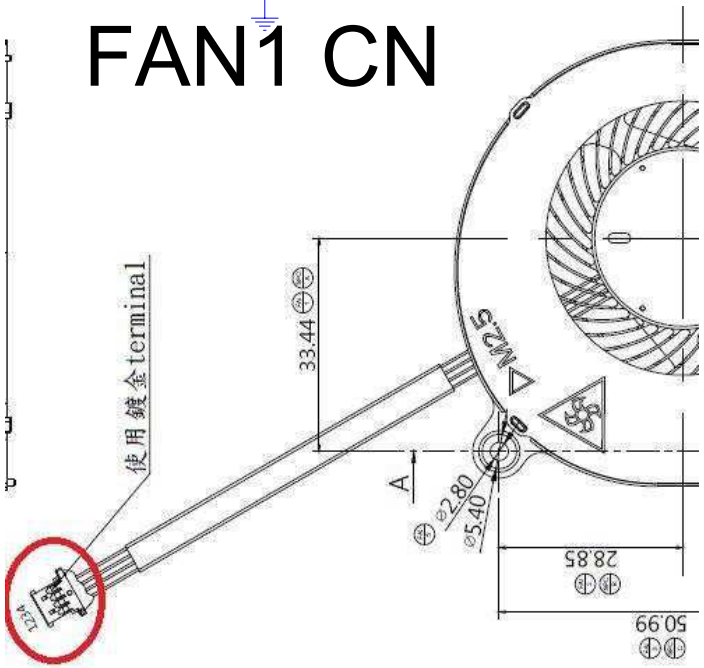
1. LEAD WIRE: UL10064 AWG#32 OD: 0.38±0.05mm(OR EQUIVALENT MATERIAL)
   PIN 1: RED WIRE -----(+)
   PIN 2: YELLOW WIRE -----(FG)
   PIN 3: BROWN WIRE -----(PWM)
   PIN 4: BLACK WIRE -----(-)

HOL
DIMS

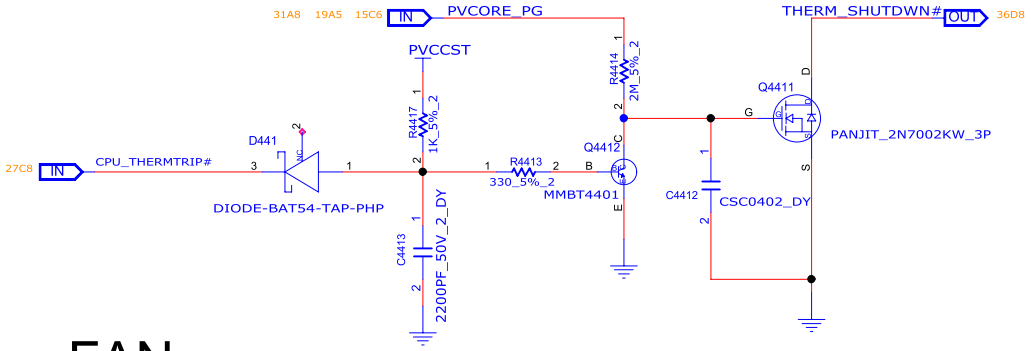


4/27 MODIFY PIN DEF.

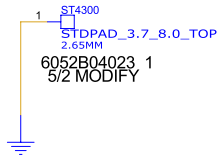
FAN1 CN



REFERENCE NUMBER:4411~4449



FAN



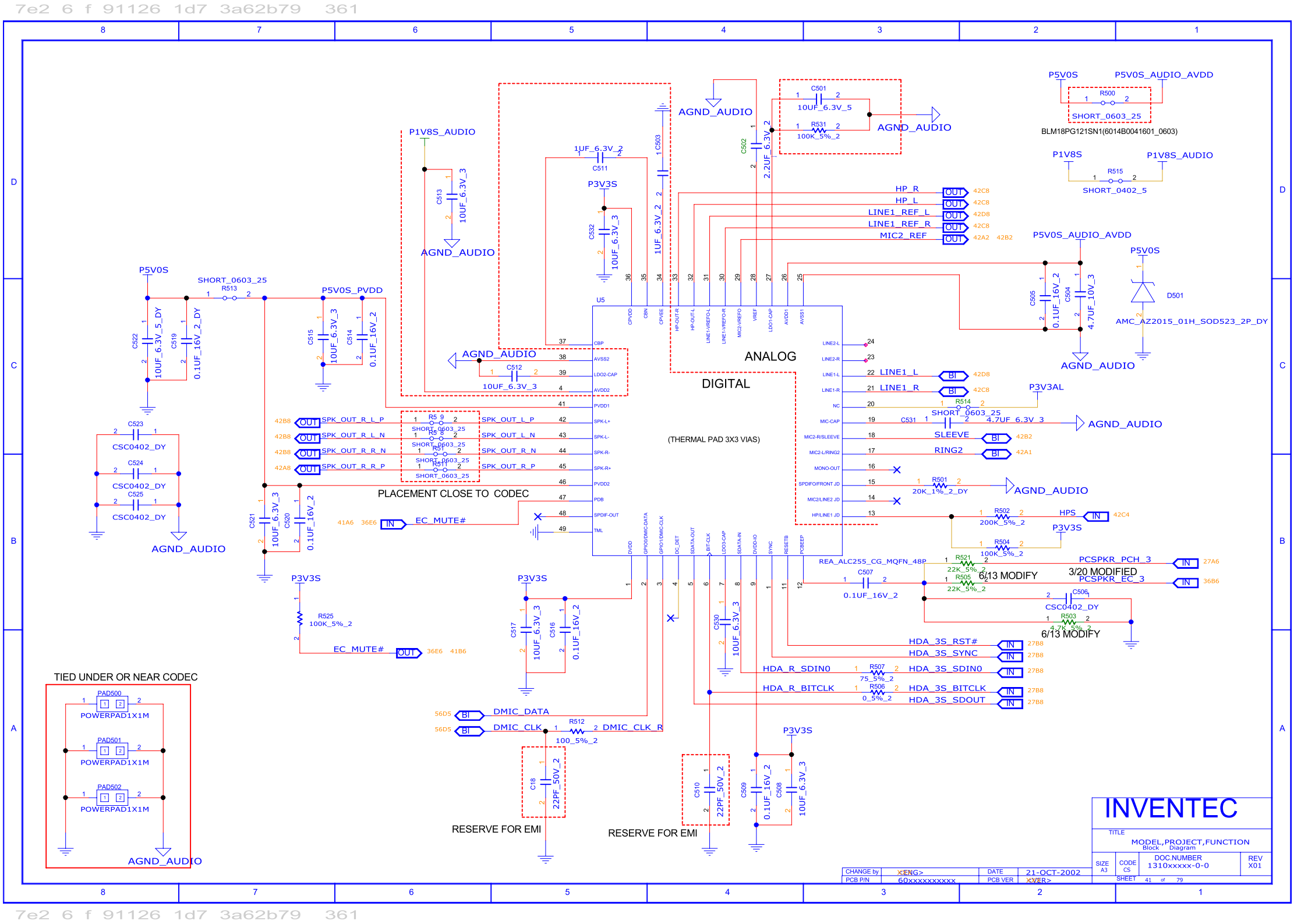
6052B04023 1
5/2 MODIFY

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
	SHEET	of 40 79	

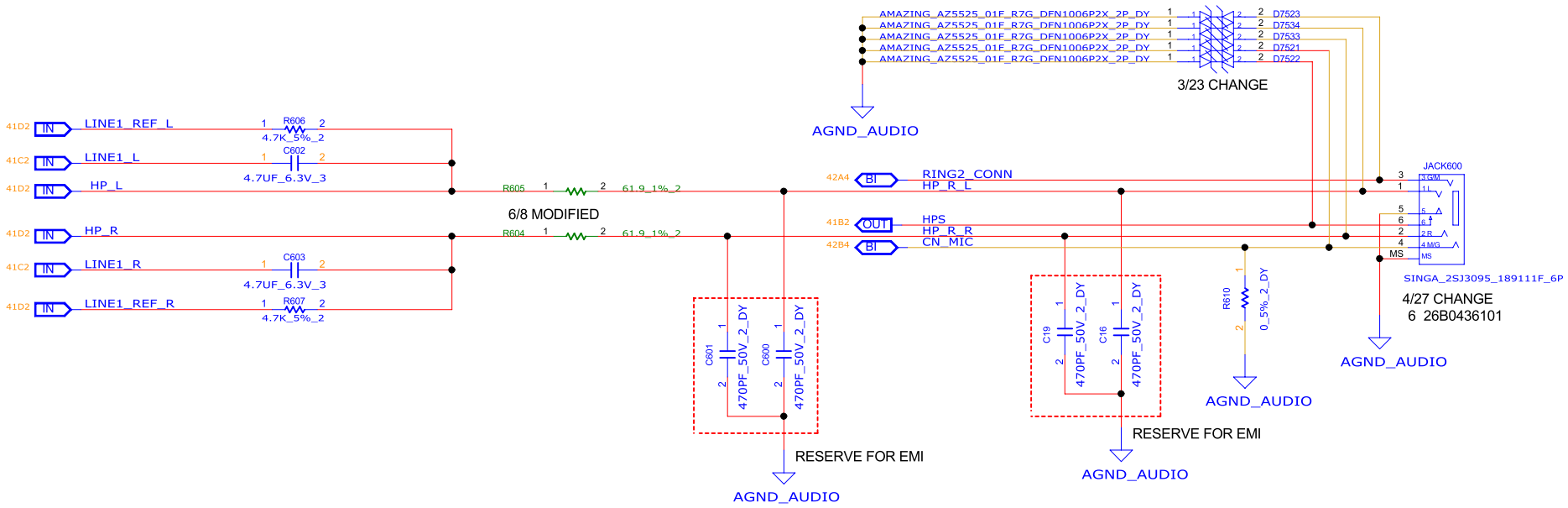
CHANGE by	XXX	DATE	
PCB P/N	PNG-xxxxxxx	PCB VER	XXX-OCT-2002

7e2 6 f 91126 1d7 3a62b79 361


ANALOG
DIGITAL
(THERMAL PAD 3X3 VIAS)
REA_ALC255_CG_MQFN_48P
PLACEMENT CLOSE TO CODEC
TIED UNDER OR NEAR CODEC
RESERVE FOR EMI
RESERVE FOR EMI
6/13 MODIFY
3/20 MODIFIED
6/13 MODIFY
BLM18PG121SN1(6014B0041601_0603)
AMC_AZ2015_01H_SOD523_2P_DY
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
SHEET
41 of 79
CHANGE by
<ENG>
DATE
21-OCT-2002
PCB P/N
60xxxxxxxxxx
PCB VER
<VER>

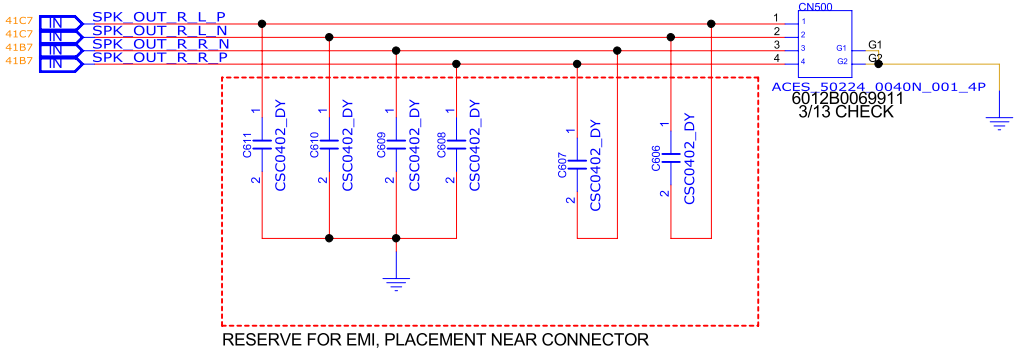
REFERCE 600~649(JACK/MIC/SPEAKER)

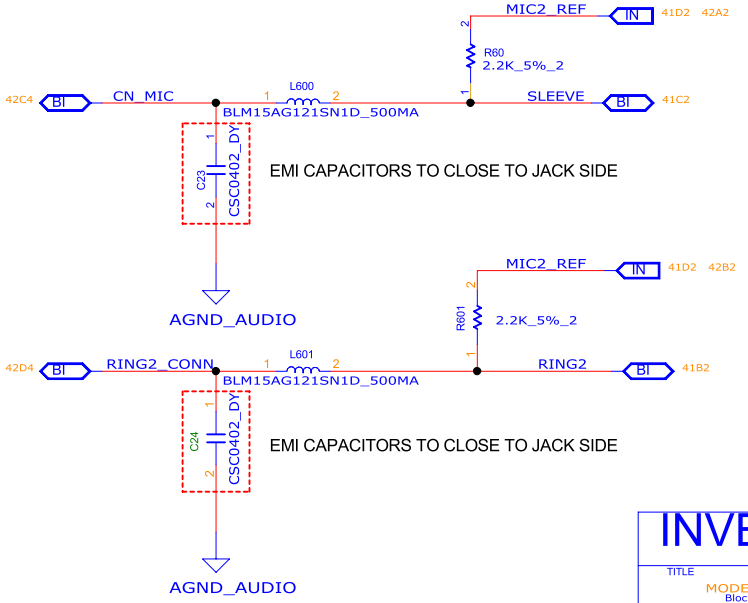
AUDIO JACKS



INTERNAL SPEAKERS1

NOTE:SPK TRACE SHOULD 3 ~40 MILS WIDTH





INVENTEC

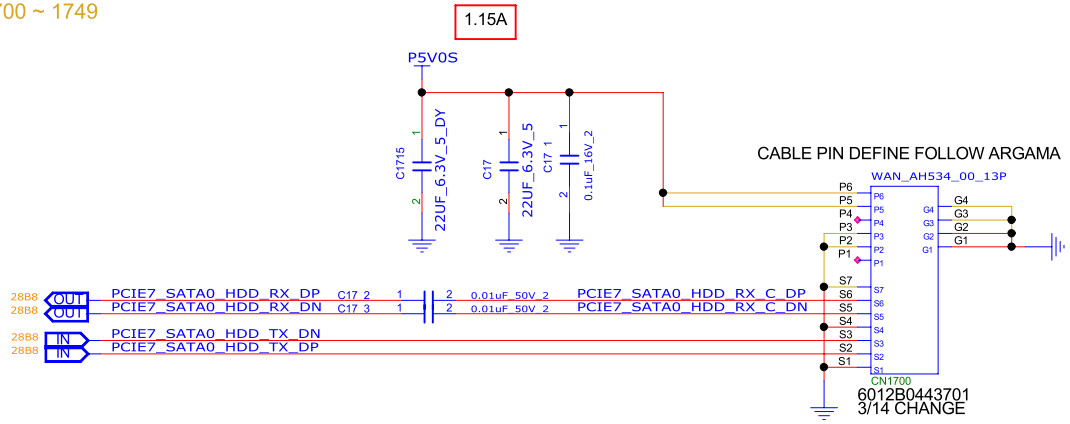
TITLE	MODEL,PROJECT,FUNCTION		
	Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 42 of 79	
PCB P/N 60xxxxxxxxx	PCB VER XXX		

7e2 6 f 91126 1d7 3a62b79 361

SATA HDD CABLE CONN on MB

SATA HDD

Lo ation 1700 ~ 1749



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 43 of 79			

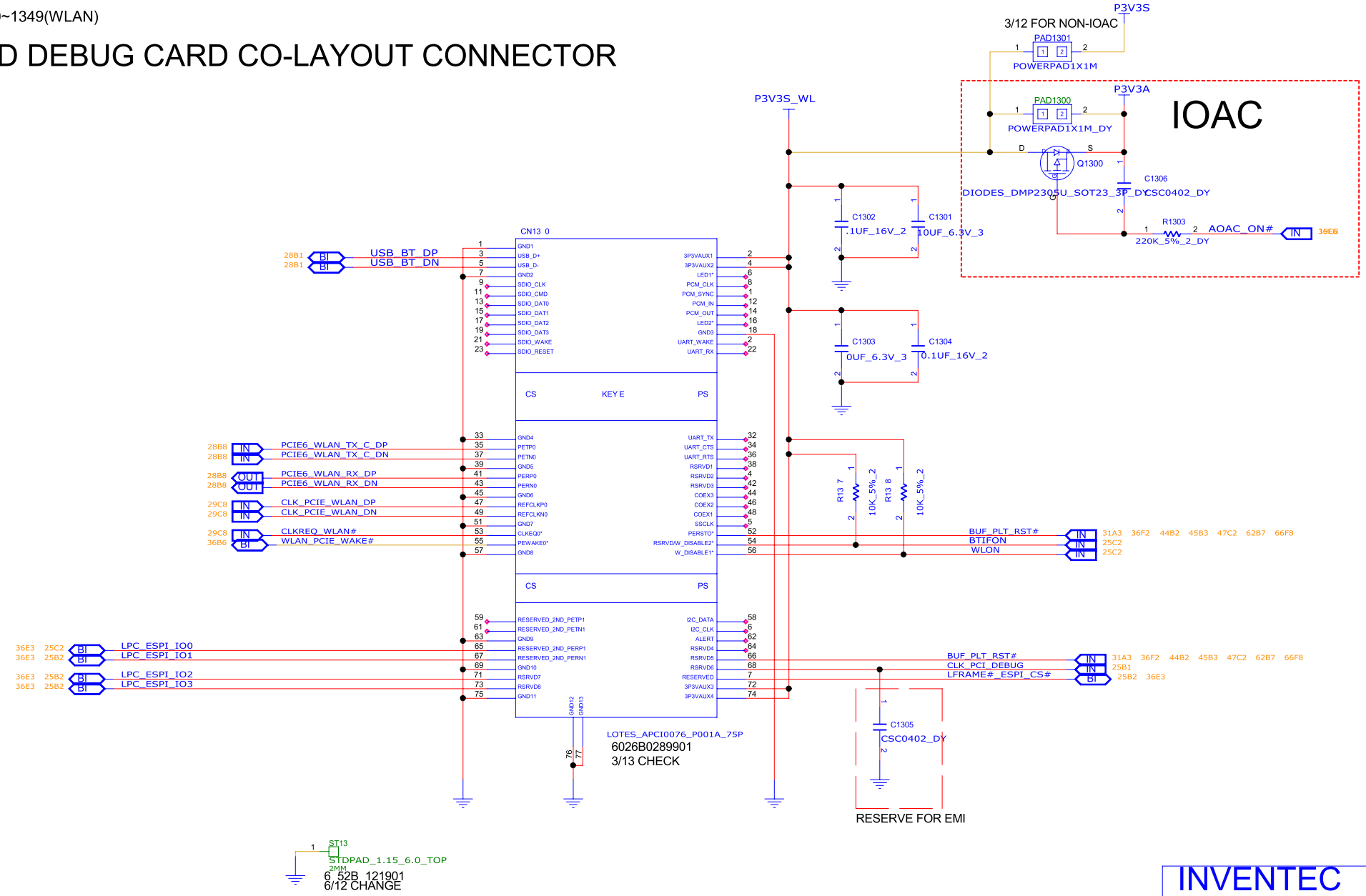
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

7e2 6 f 91126 1d7 3a62b79 361

7e2 6 f 91126 1d7 3a62b79 361

REFERENCE 1300~1349(WLAN)

WIFI AND DEBUG CARD CO-LAYOUT CONNECTOR



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

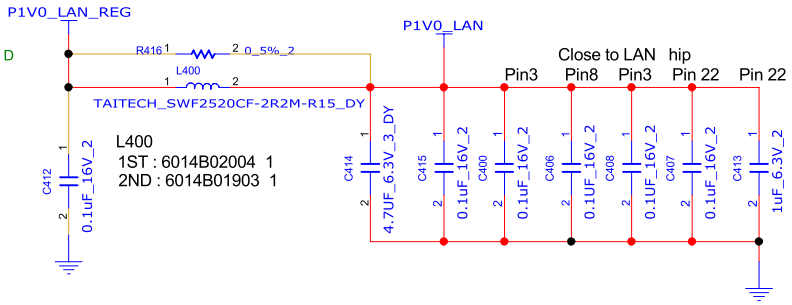
SHEET 44 of 79

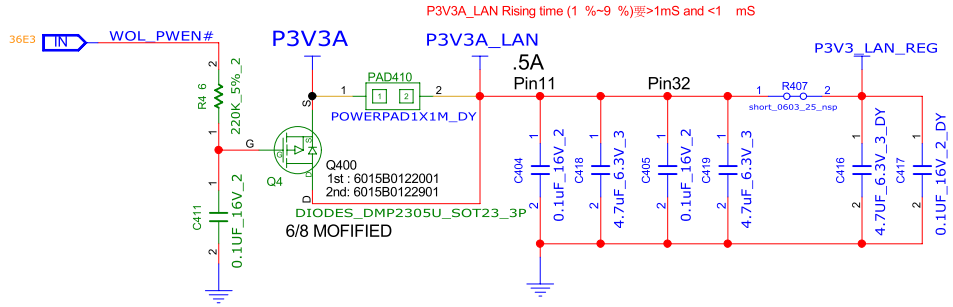
7e2 6 f 91126 1d7 3a62b79 361

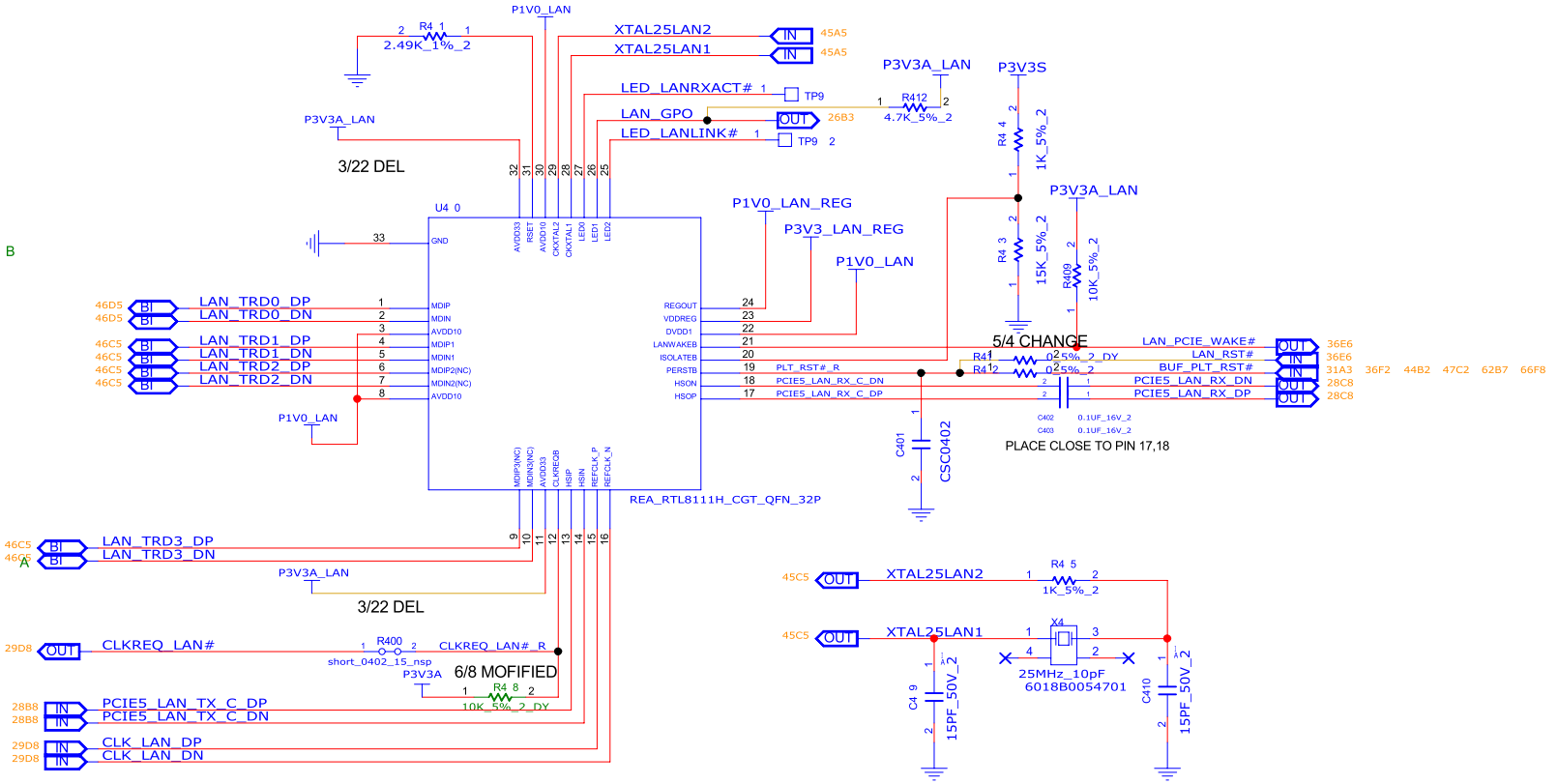
LAN (Controller)

Location 4 ~ 469
Ver. 3_21 120807

The schematic check had some item must modify as below.
01. 請註記 P3V3A_LAN **Rising time (10%~90%)要>0.5mS and <100mS.**
02. LAN power Noise P3V3A_LAN < 200mV Vpeak to Vpeak.
03. LAN power Noise P1_LAN < 100mV Vpeak to Vpeak.







INVENTEC

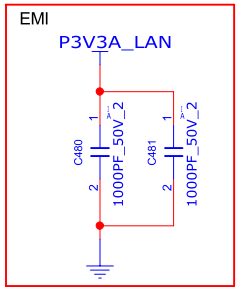
TITLE	MODEL,PROJECT,FUNCTION		
	Block Diagram		
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 45 of 79			

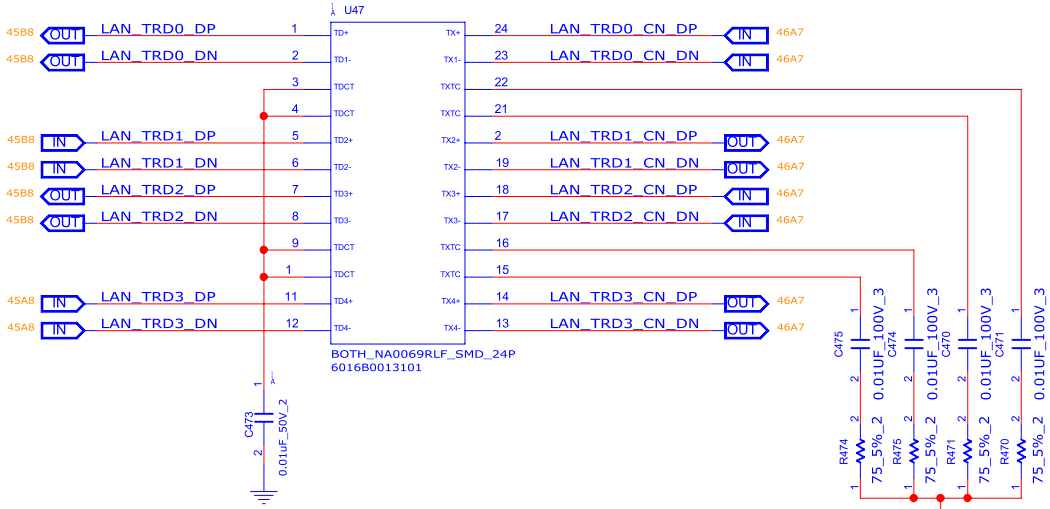
e2 6 f 91126 1d7 3a62b79 361

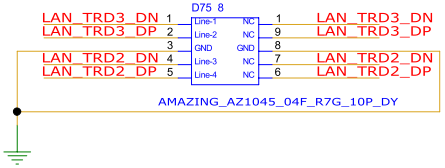
LAN (Transformer & RJ45)

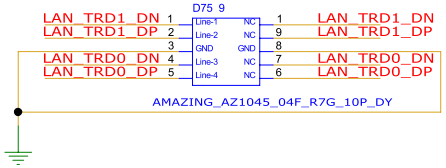
Location 470 ~ 499

Ver.01_20120801

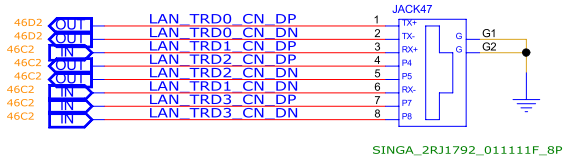








RJ-45



4/27 MODIFY

6 26B 4357 1

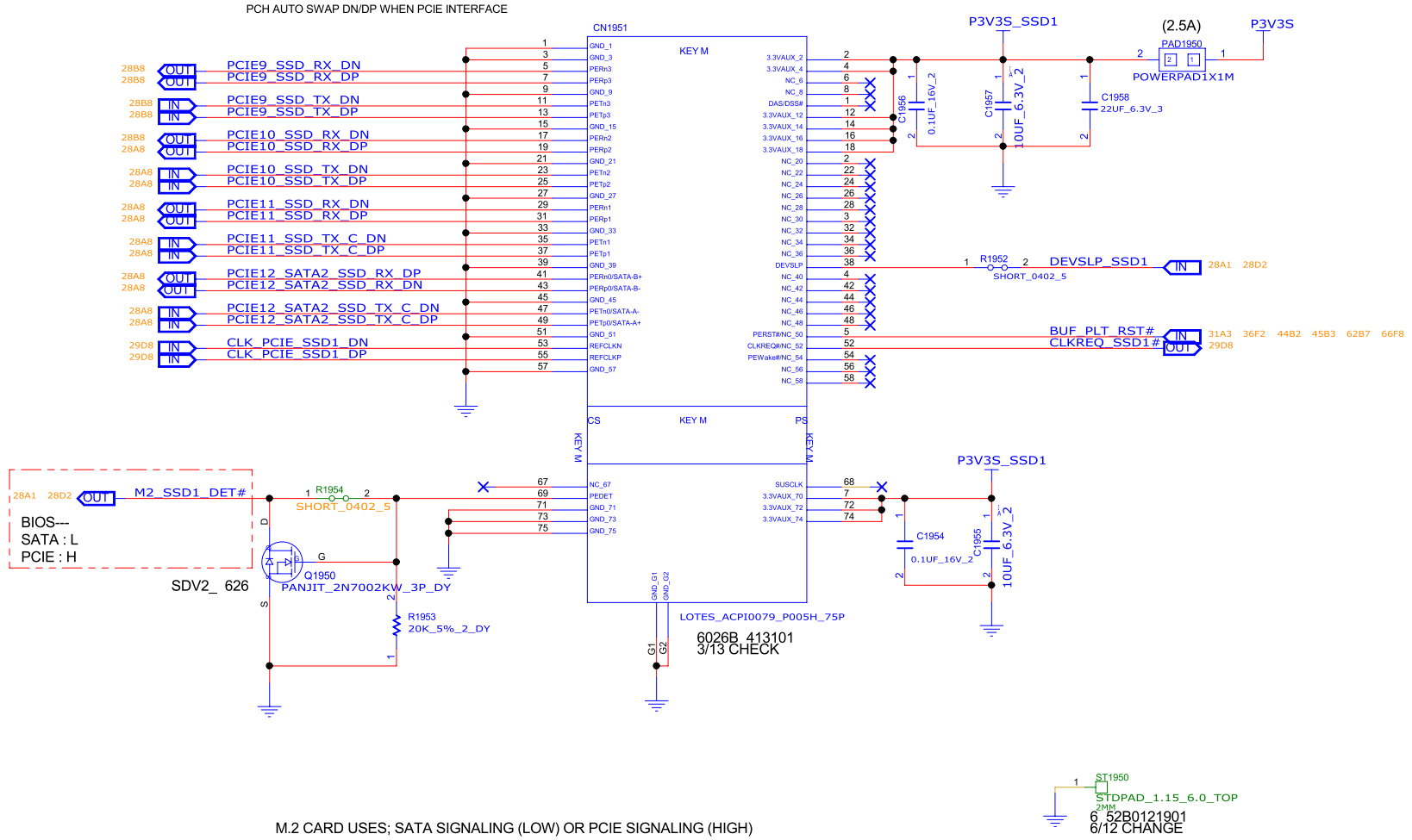
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 46 of 79	
PCB P/N 60xxxxxxxxxx	PCB VER XXX		

e2 6 f 91126 1d7 3a62b79 361

7e2 6 f 91126 1d7 3a62b79 361

NGFF SSD(PCIE/SATA 4X)



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

REFERENCE NUMBER:195 ~1999

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

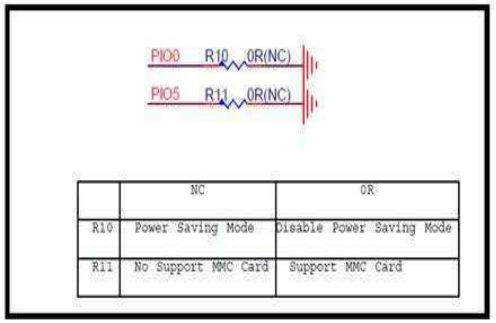
SHEET 47 of 79

7e2 6 f 91126 1d7 3a62b79 361

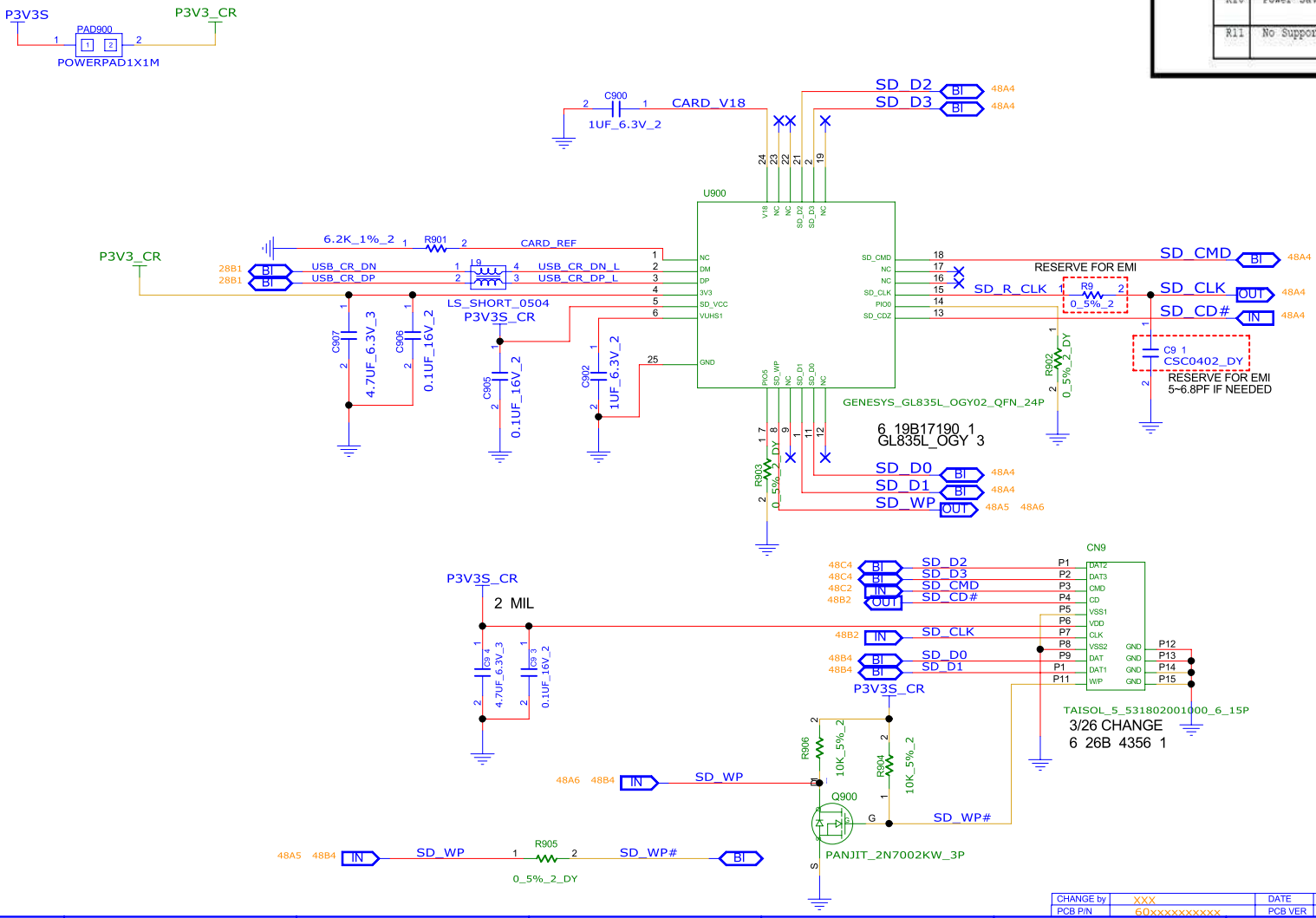
7e2 6 f 91126 1d7 3a62b79 361

REFERNCE 9 0~999(CARDREADER)

CARD READER



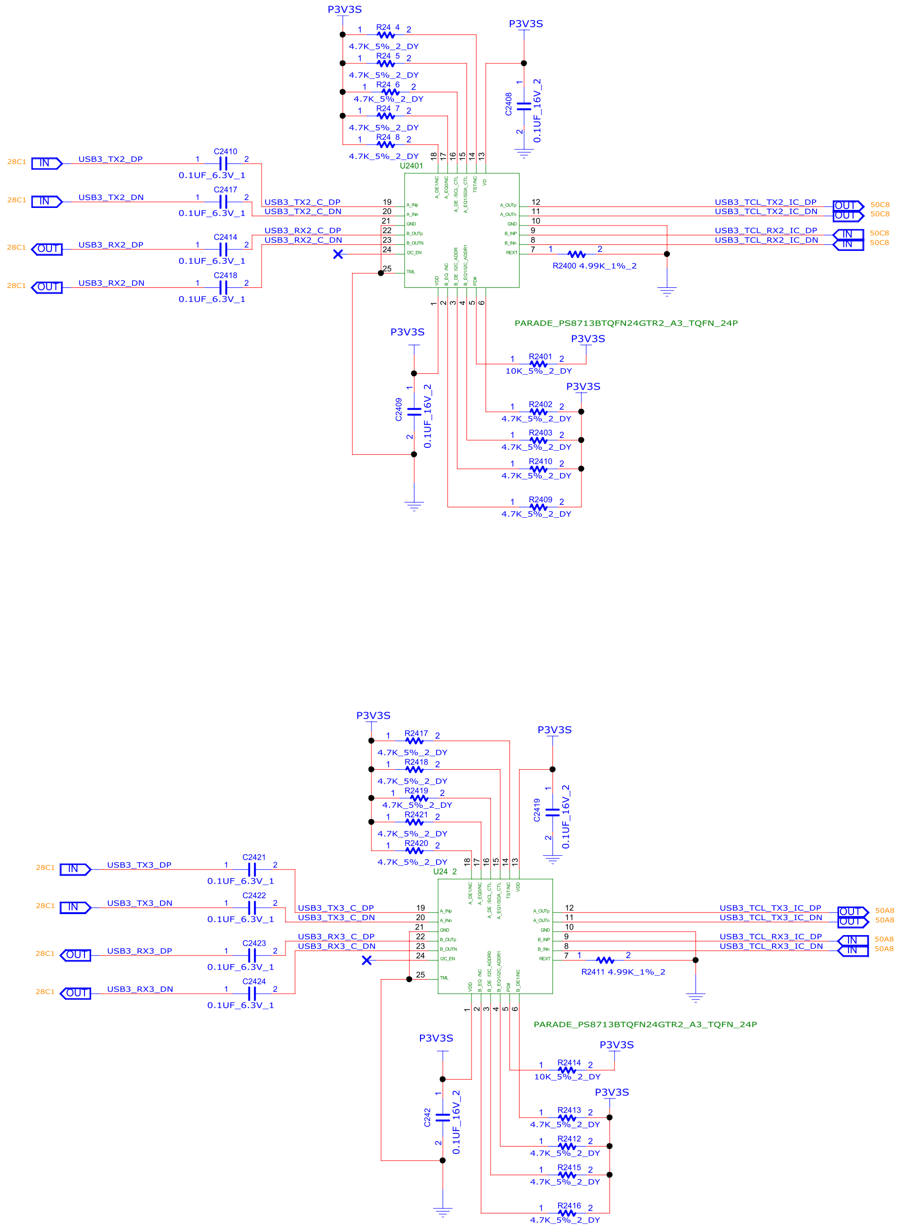
	NC	0R
R10	Power Saving Mode	Disable Power Saving Mode
R11	No Support MMC Card	Support MMC Card



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION CARD READER
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	48 of 79
CHANGE by	XXX
PCB P/N	60xxxxxxxxx
DATE	21-OCT-2002
PCB VER	XXX

7e2 6 f 91126 1d7 3a62b79 361



INVENTEC

TITLE MODEL,PROJECT,FUNCTION

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002

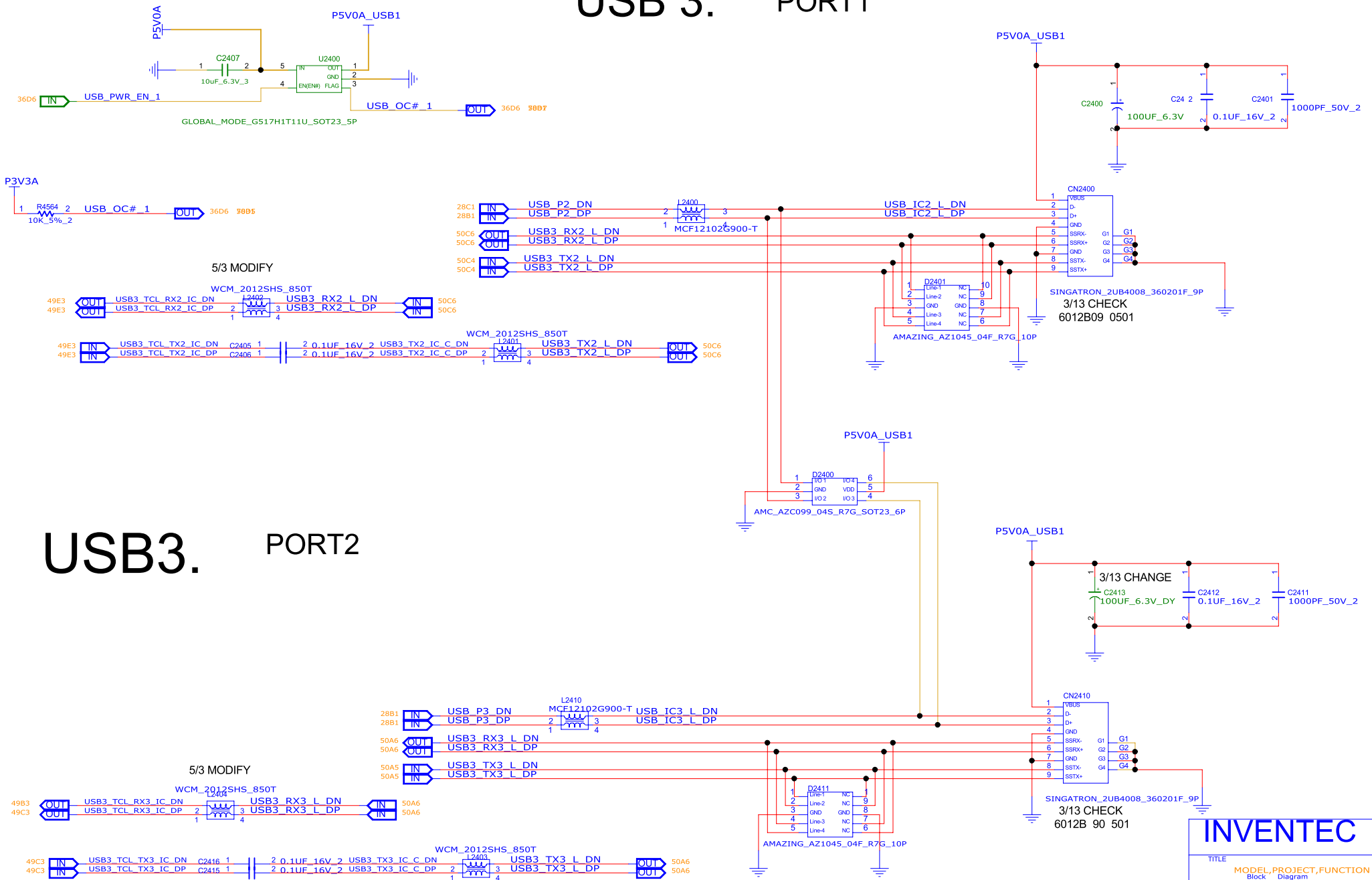
PCB P/N 60xxxxxxxxxx PCB VER <VER>

SHEET 49 of 79

7e2 6 f 91126 1d7 3a62b79 361

REFERENCE 24 0~2450(USB3.)

USB 3. PORT1



USB3. PORT2

INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

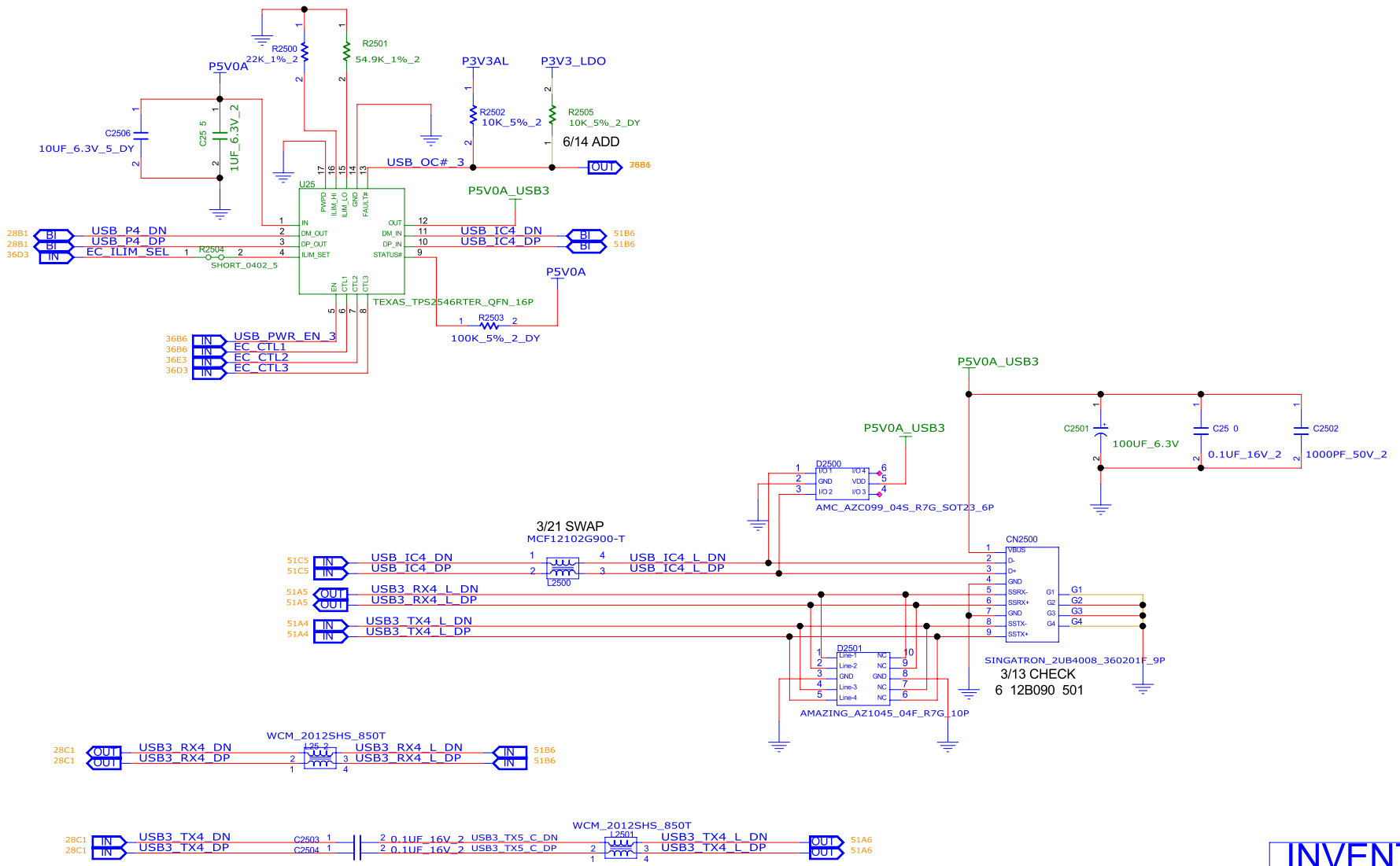
SHEET 50 of 79

7e2 6 f 91126 1d7 3a62b79 361

7e2 6 f 91126 1d7 3a62b79 361

REFERENCE 2500(USB3.)

USB 3. PORT3



INVENTEC

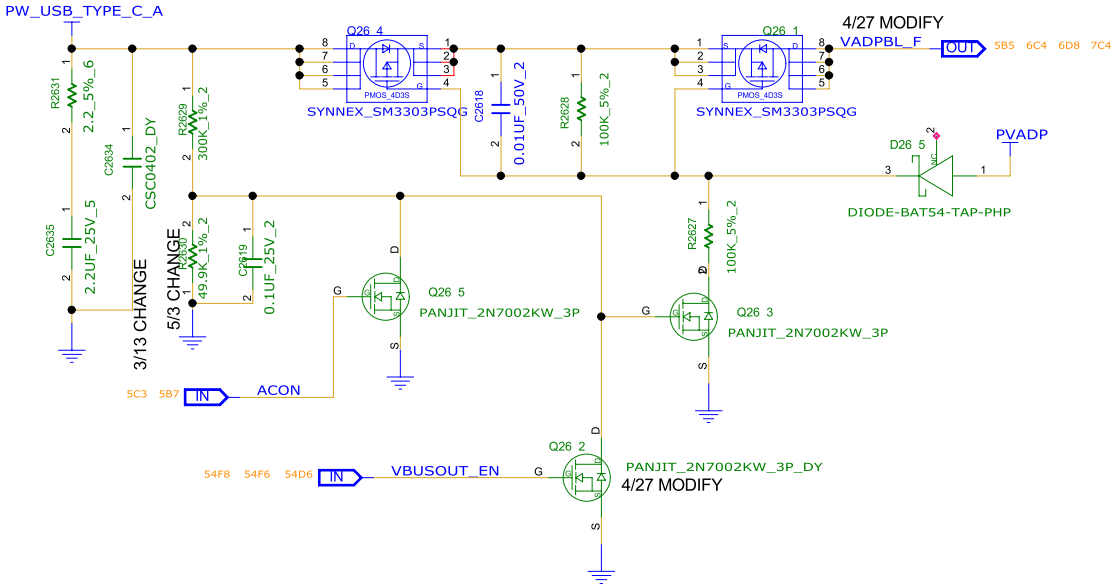
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 51 of 79

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

7e2 6 f 91126 1d7 3a62b79 361



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TITLE
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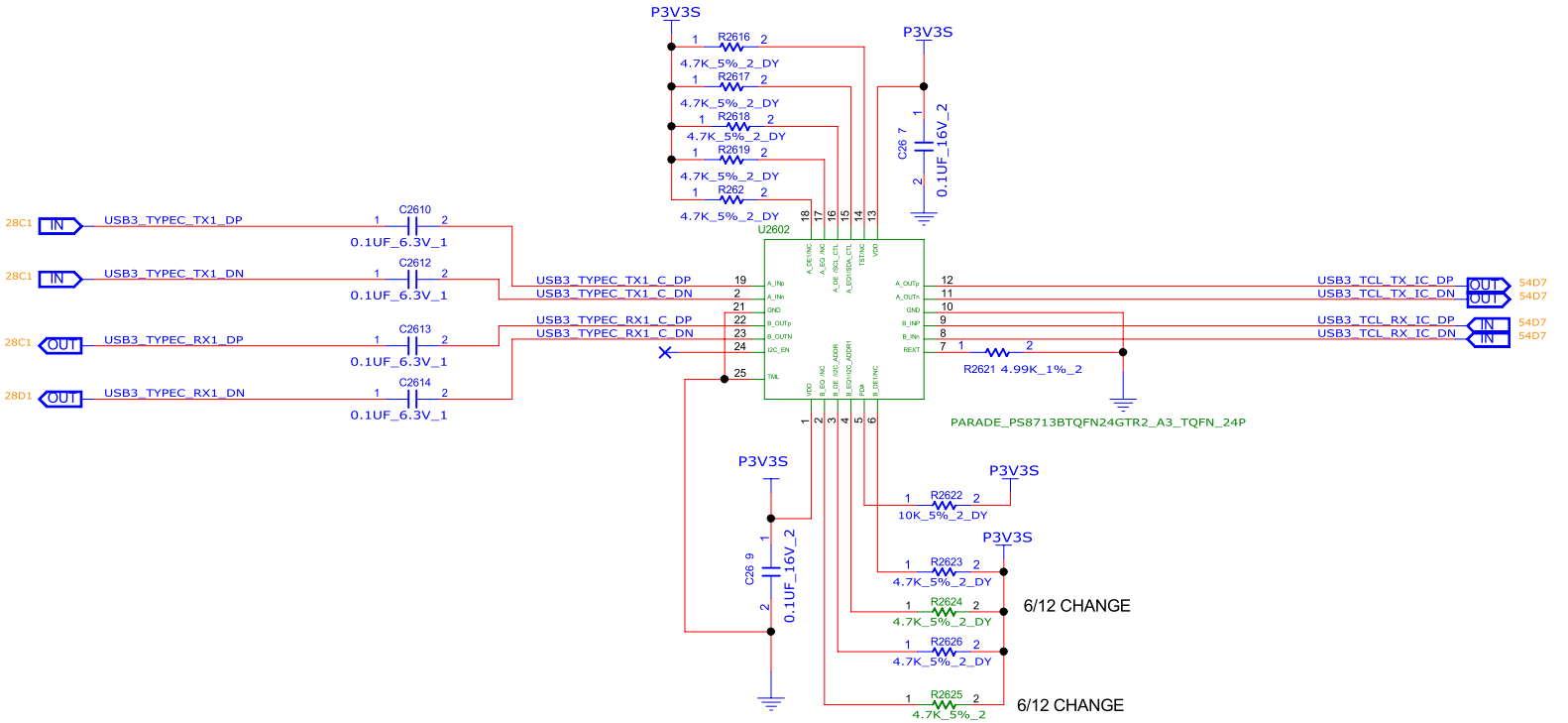
USB3 REDRIVER

REFERENCE 2600~2699(USB RESERVE)



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PCB P/N	60xxxxxxxxx	PCB VER	XXX

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Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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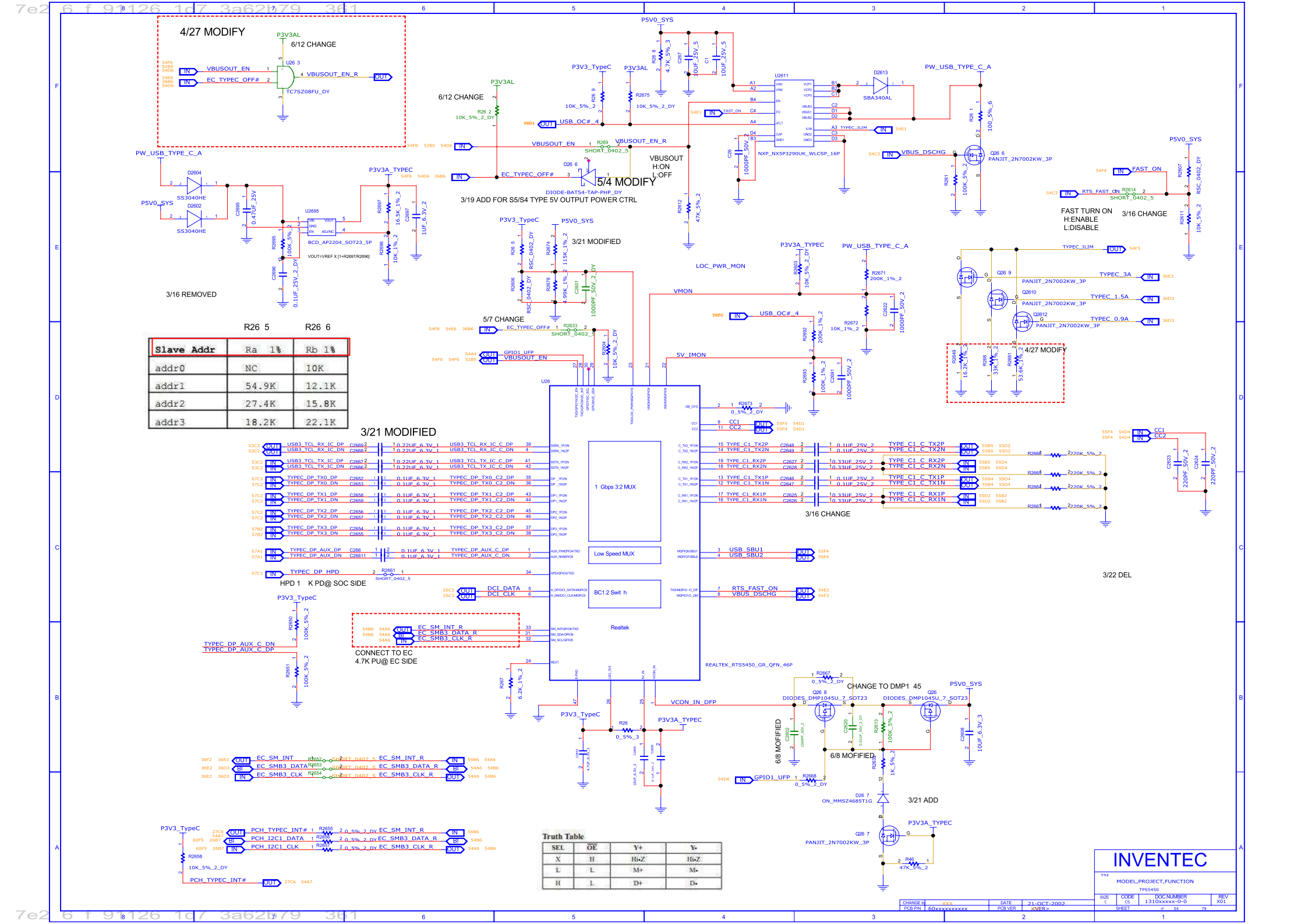
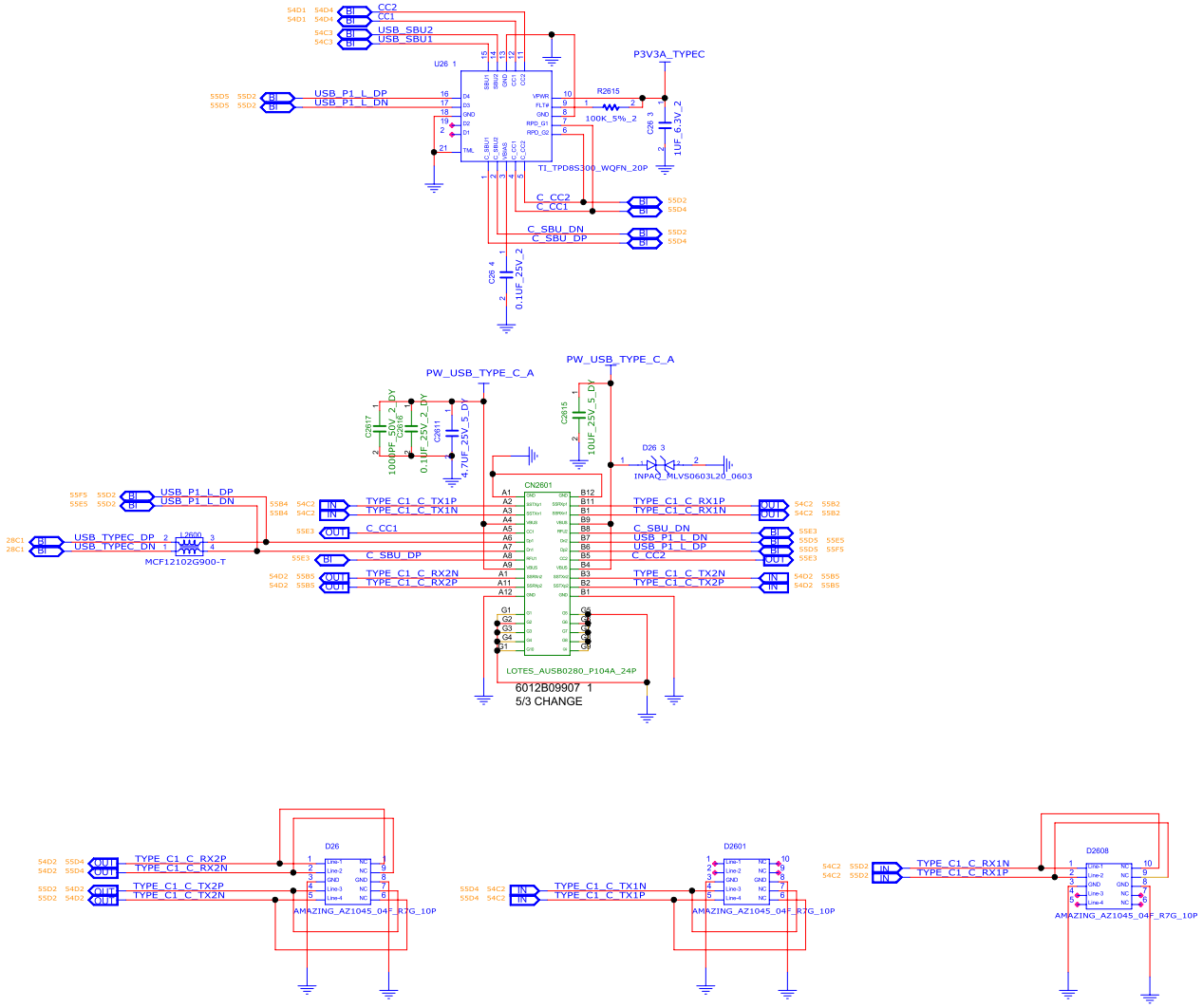


R26 5 R26 6

Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



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TITLE: MODEL,PROJECT,FUNCTION

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	X.XER>

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01
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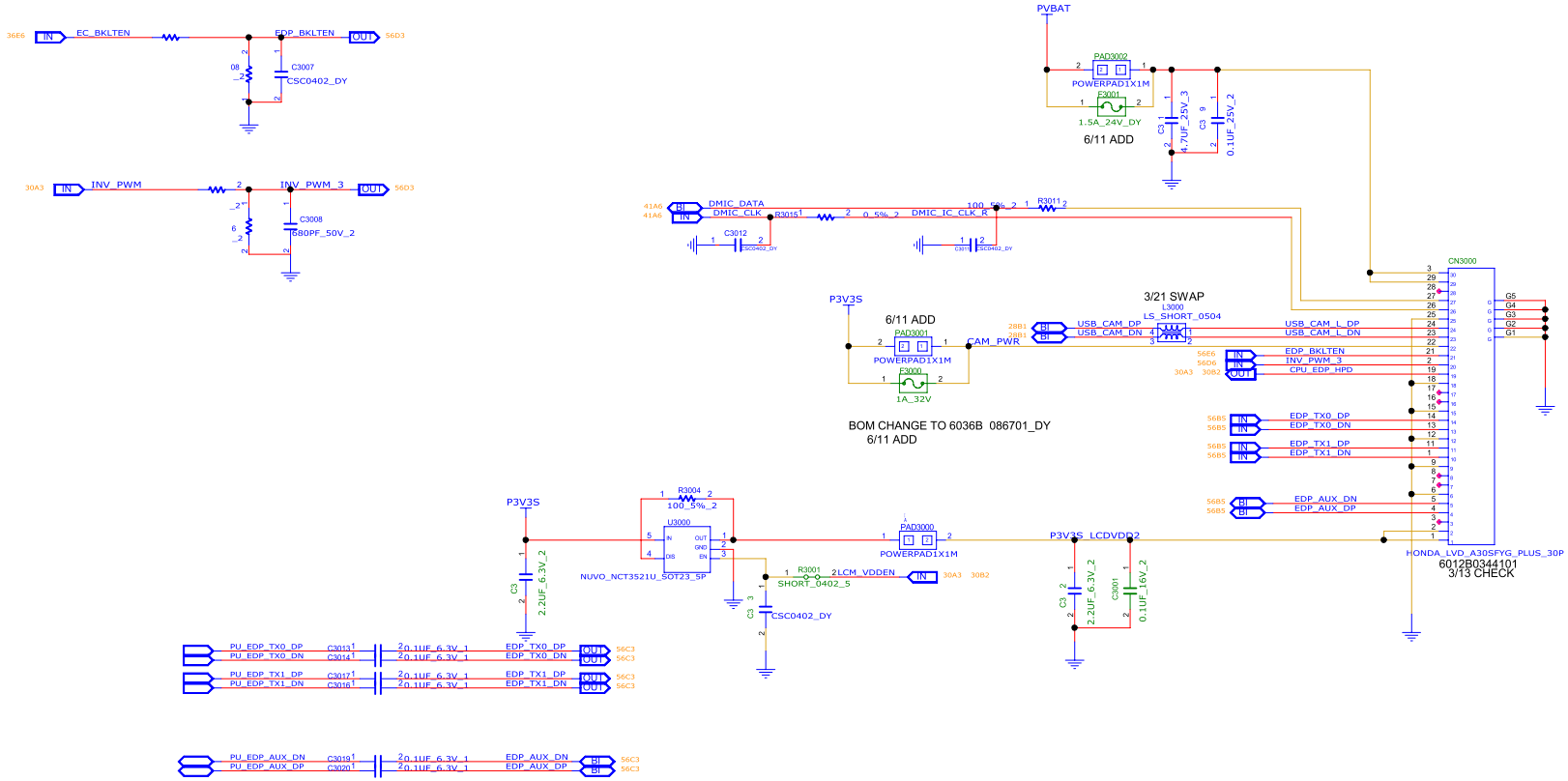
REFFE E 3 00~3 49(LCM)

EDP CONN



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TITLE: MODEL, PROJECT, FUNCTION
Block Diagram

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SIZE	CODE	DOC NUMBER	REV
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4-LANE DP1.2 DEMUX

PCy0 (3 level input)	I	AUX interception disable for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V I/O; PCy0 = L: AUX interception enable, driver configuration is set by link training (default) H: AUX interception disable, driver output with fixed 800mV and 0dB M: AUX interception disable, driver output with fixed 400mV and 0dB ***Overwritten by I2C register in I2C Control Mode***
PCy1 (3 level input)	I	Output swing adjustment for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V I/O; PCy0 = L: default H: +20% M: -16.7% ***Overwritten by I2C register in I2C Control Mode***

3/12 ADD
3/2 MODIFIED
3/2 MODIFIED
3/2 MODIFIED
3/2 MODIFIED
4/27 MODIFY
4/27 MODIFY
PORT 2 PRIORITY
FROM CPU DDI2
TYPE C DP PORT
VGA DP PORT
6019B1031701
PARADE_PS8338BQFN60GTR_QFN_60P

REFERENCE NUMBER:54 1~5499

INVENTEC

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Block Diagram

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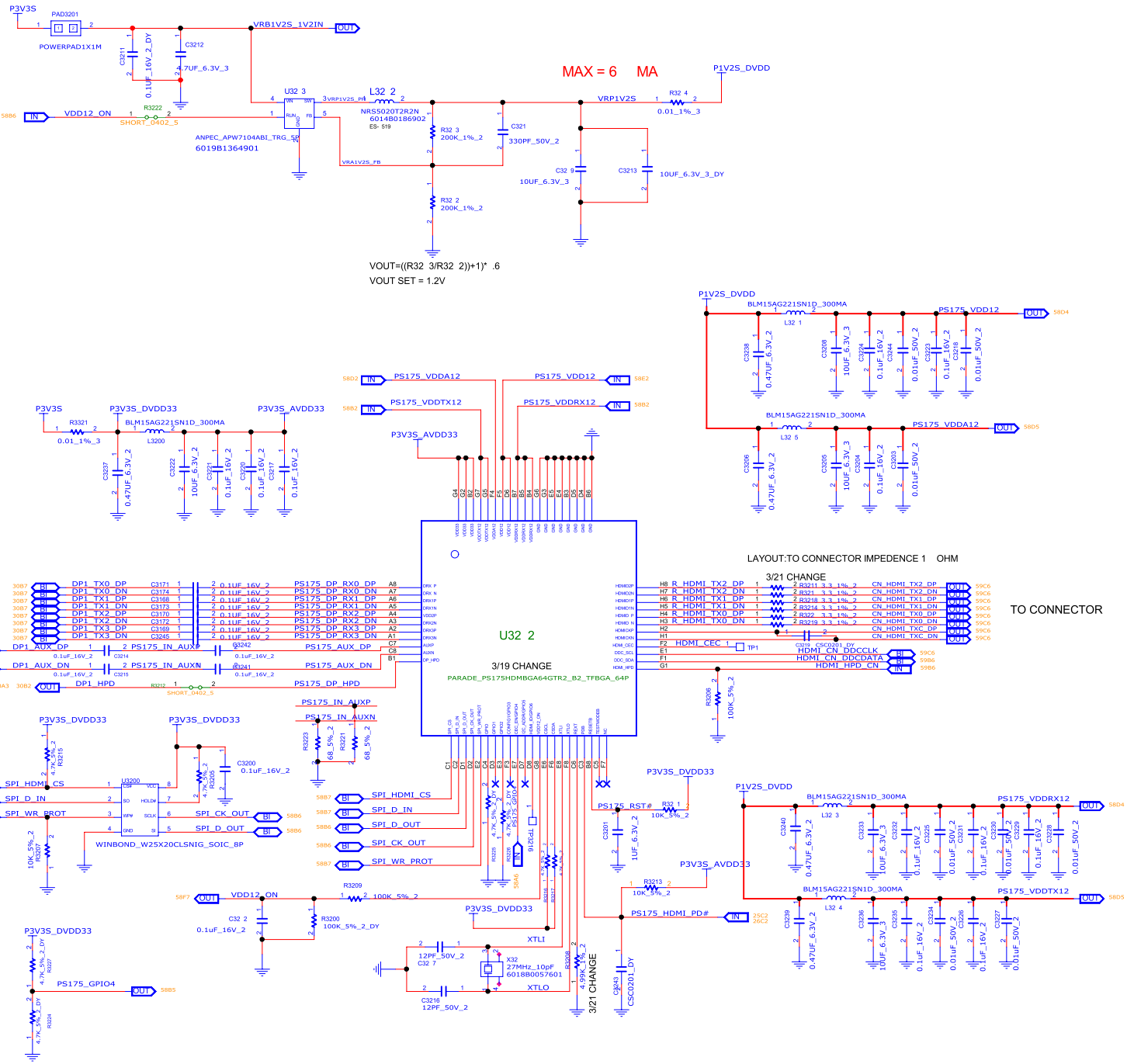
HDMI2.

REFERENCE 3200~3299(HDMI IC)

PS175



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MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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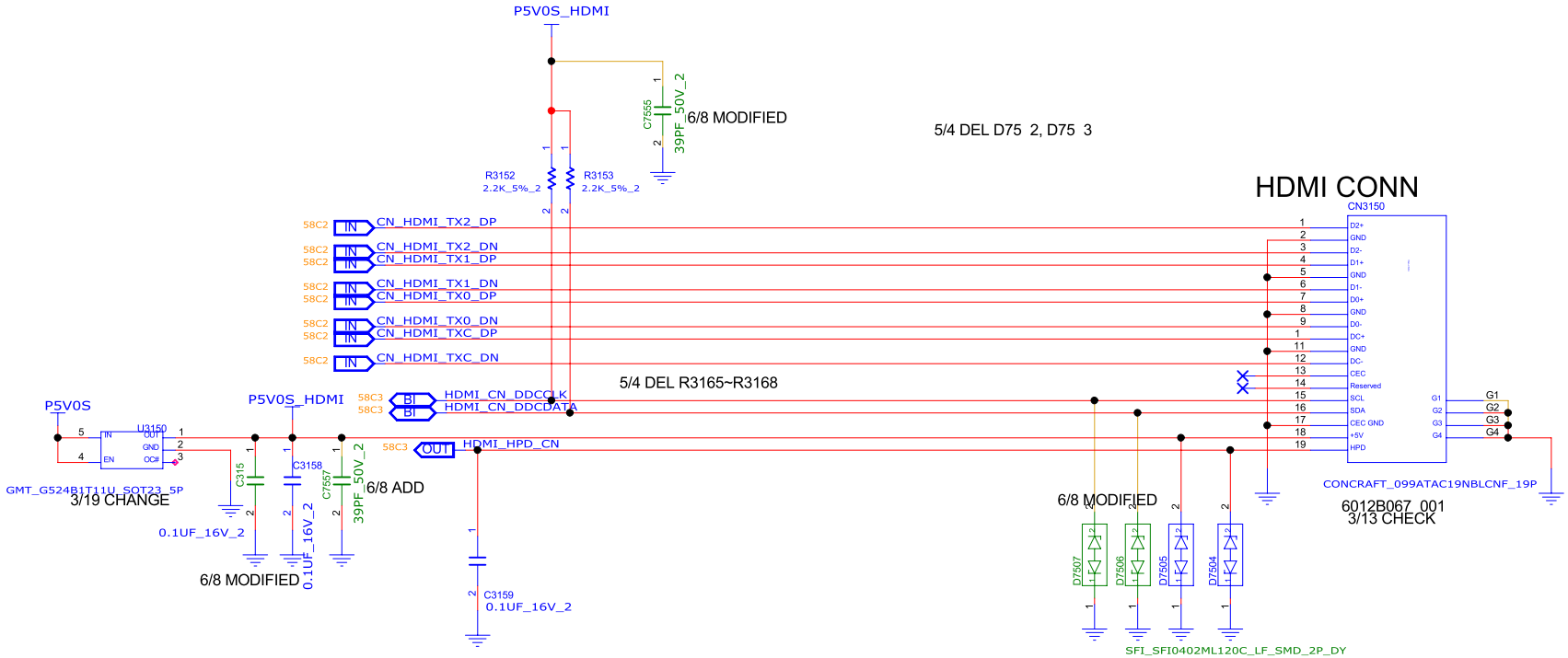

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TITLE
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CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	DOC.NUMBER 1310xxxxx-0-0
PCB P/N	60xxxxxxxxx	PCB VER	XXX	CODE CS	REV X01
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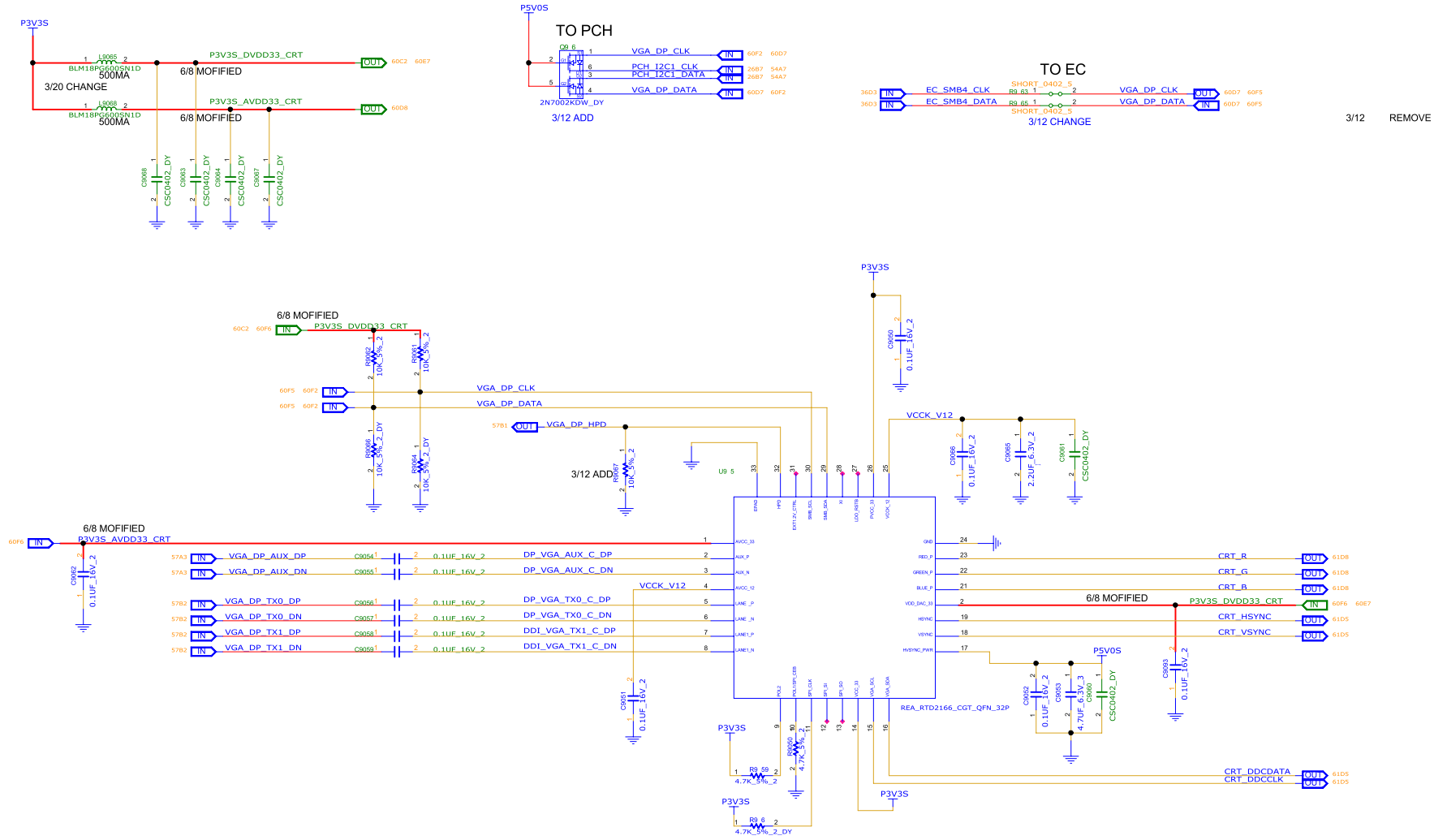

REFERENCE NUMBER:9 5 ~9 99

CHANGE NO	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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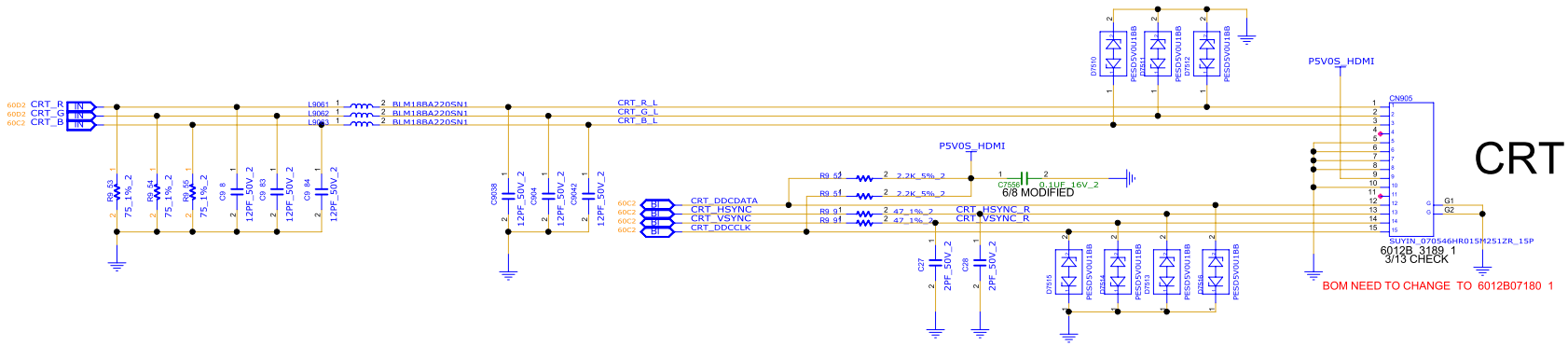

CRT CONN

REFERENCE NUMBER:9 5 ~9 99

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SIZE	CODE	DOC NUMBER	REV
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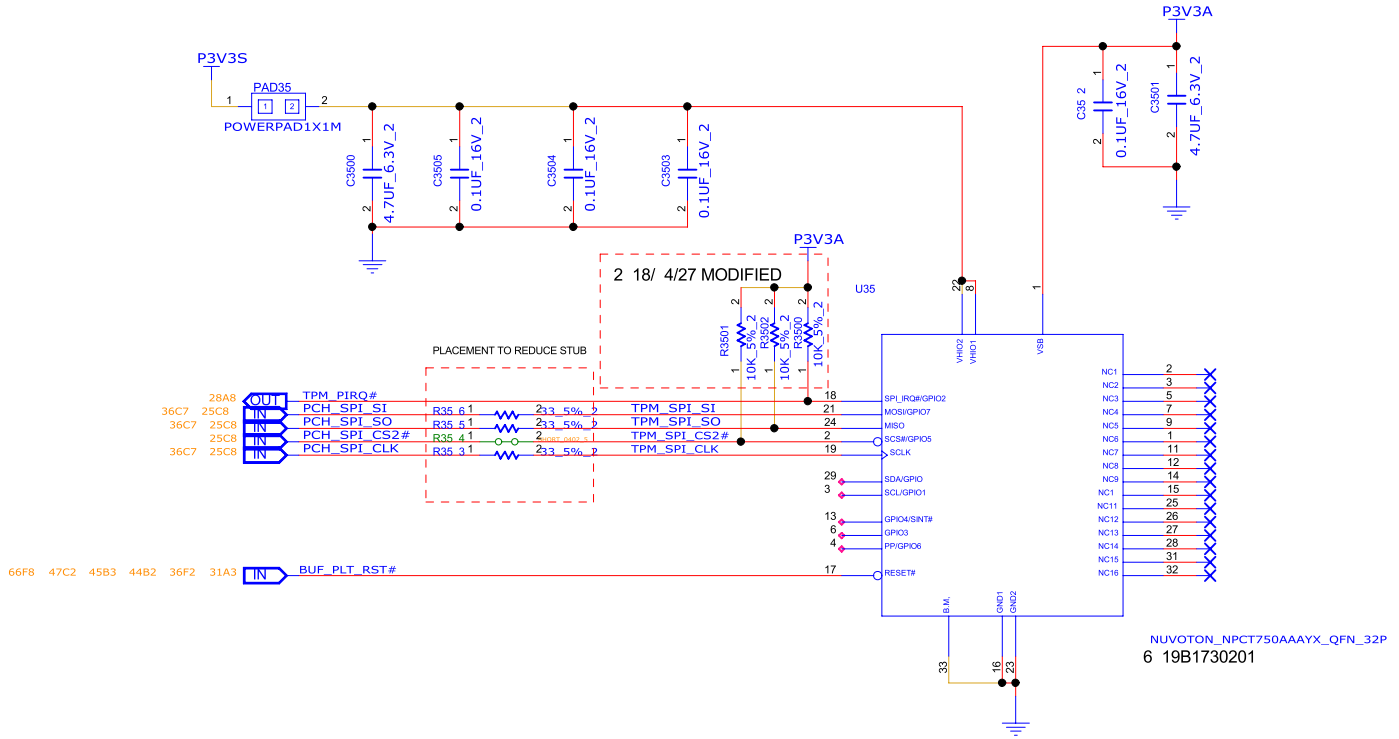

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

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Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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7e2 6 f 91126 1d7 3a62b79 361

8	7	6	5	4	3	2	1

F E D C B A

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TPS5450

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C	05	1310xxxxx-0-0	X01

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7e2 6 f 91126 1d7 3a62b79 361

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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

MX130

GDDR5 23X23

6 19B1722 1 N16S-GTR-S-A2
6 19B172 4 1 MT51J256M32HF-7 (MICRON)
6 19B172 5 1 H5GC8H24AJR-R0C (HYNIX)

2018.03.20

DATE	CHANGE NO.	REV
21-OCT-2002		A

	Chan, Shane Huang, Vens	Shiu, Vivi	
DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			A01
FILE NAME			
PCB P/N	6-71NOSxxxxxx	PCB VER	XXX

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TITLE MODEL,PROJECT,FUNCTION

SIZE	CODE	DOC.NUMBER	REV
J	CS	1310xxxxx-0-0	X01

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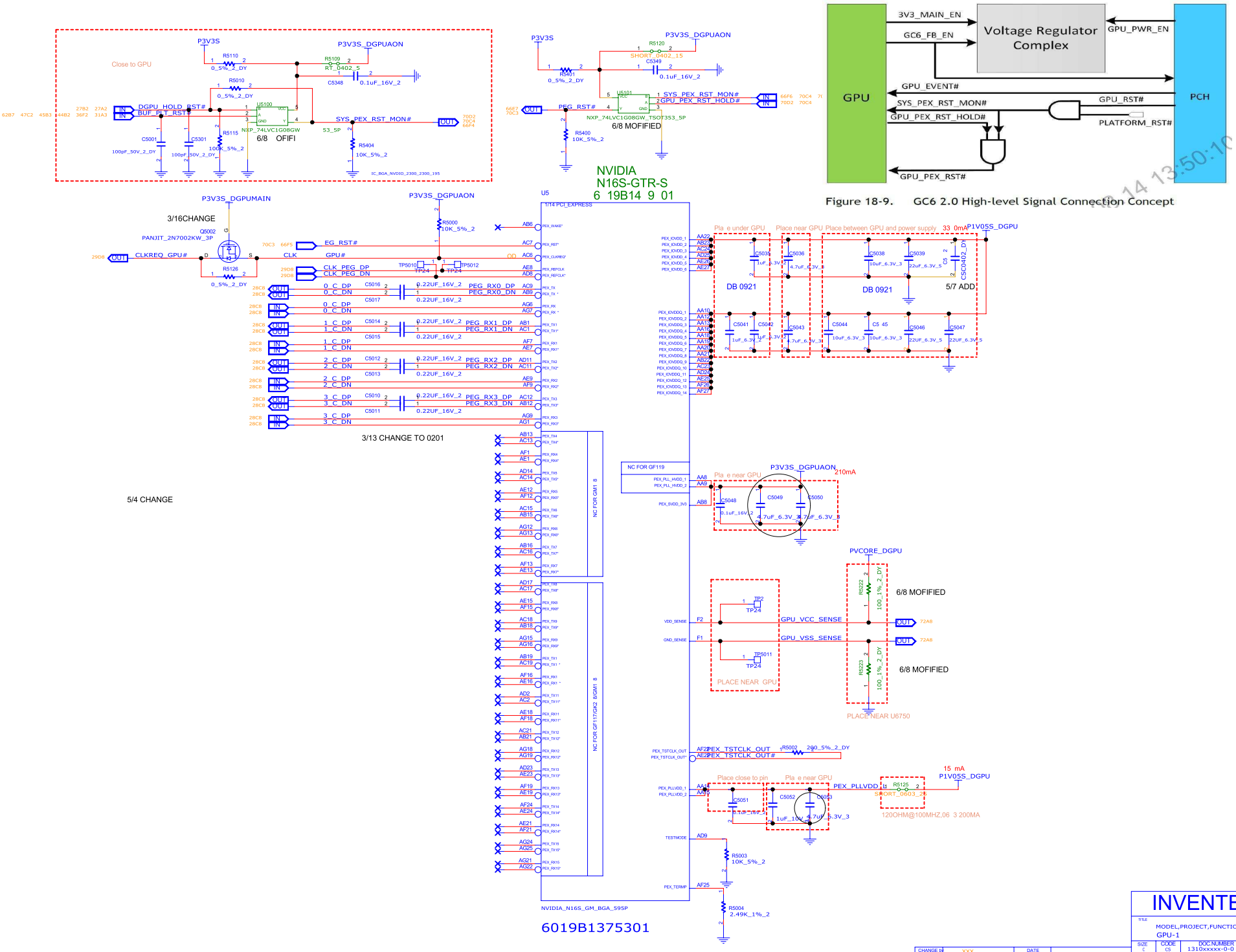
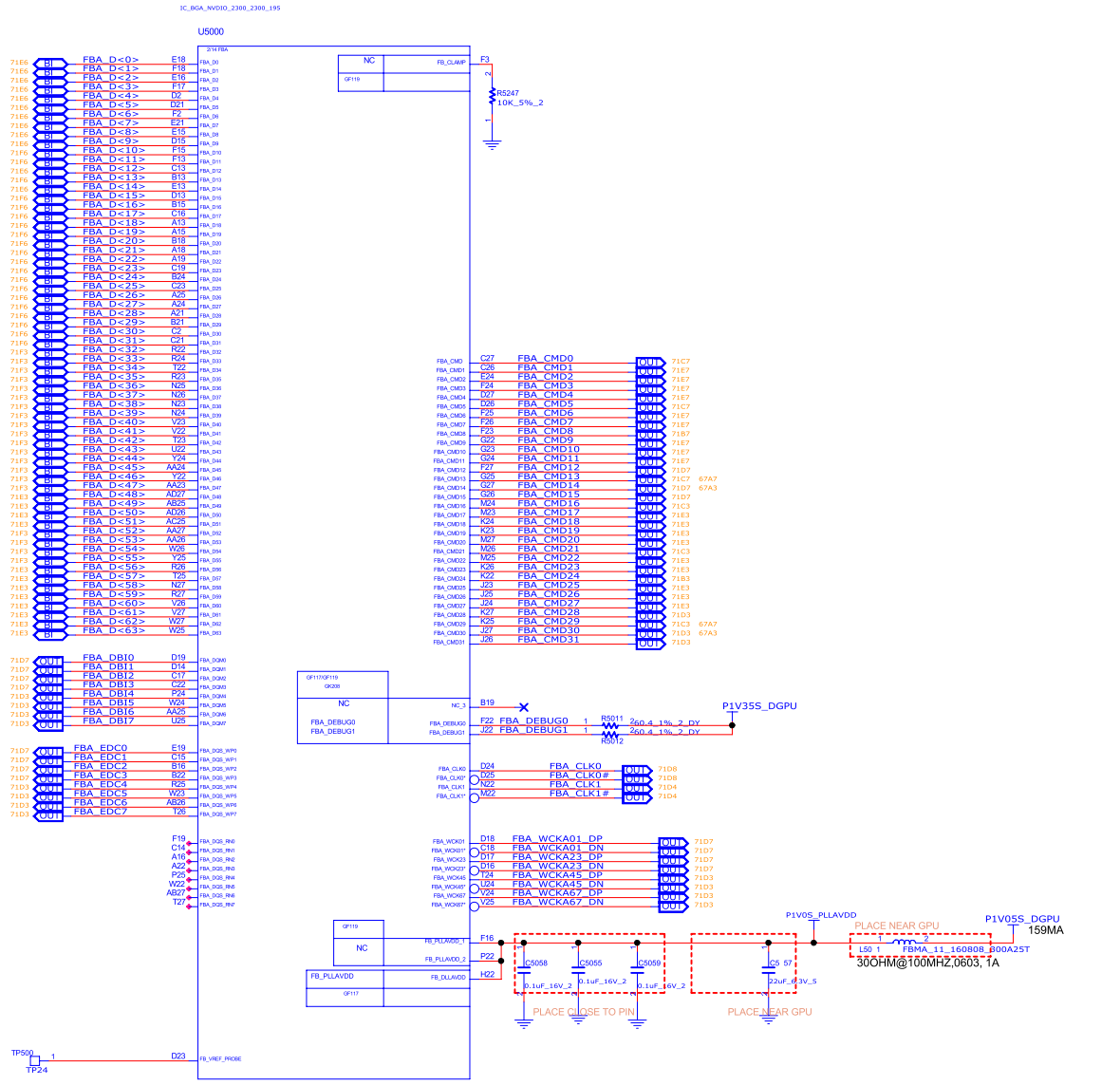


Figure 18-9. GC6 2.0 High-level Signal Connection Concept



N14x DDR3 mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6

NVIDIA Confidential 2012.07.1

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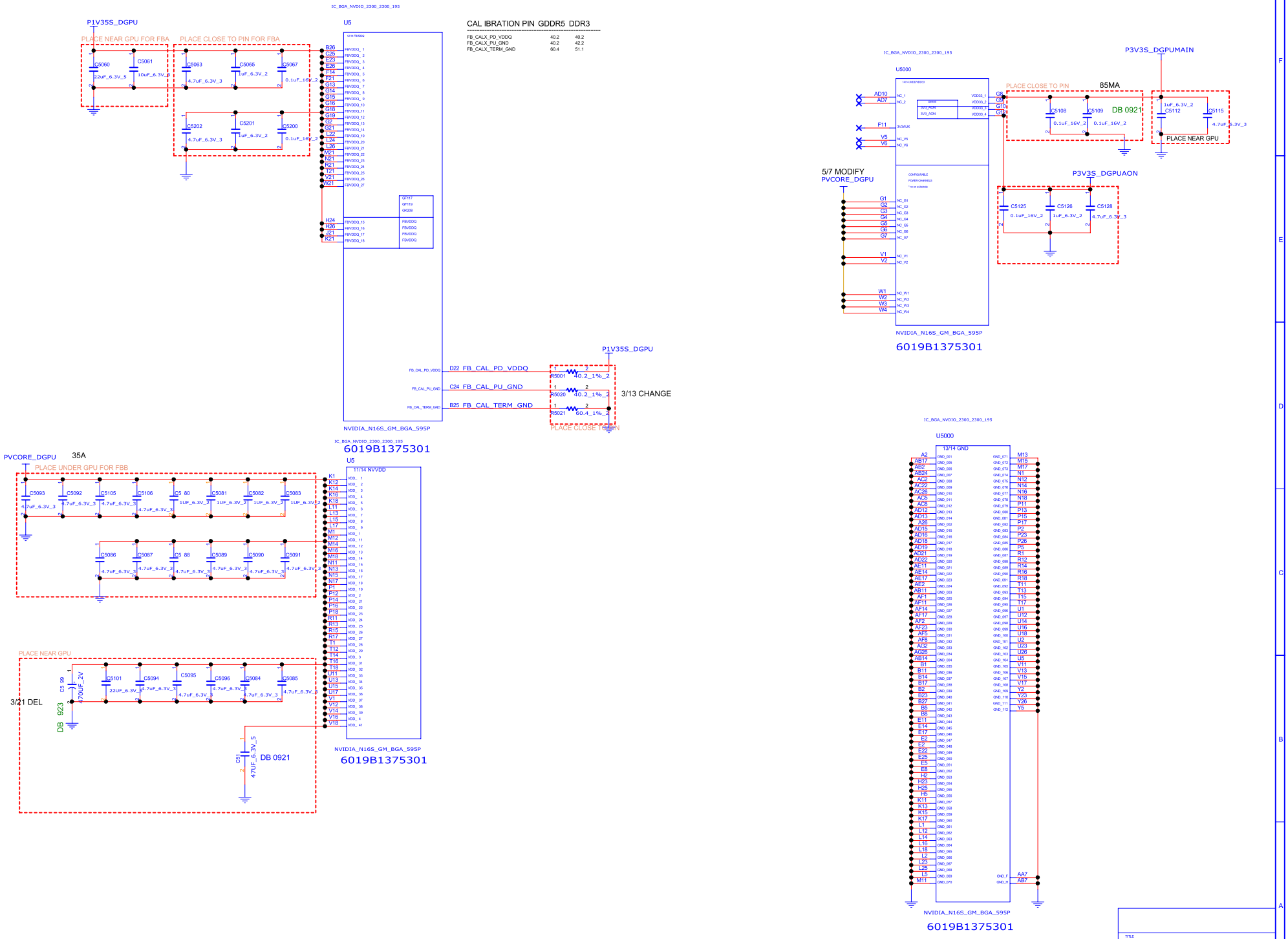
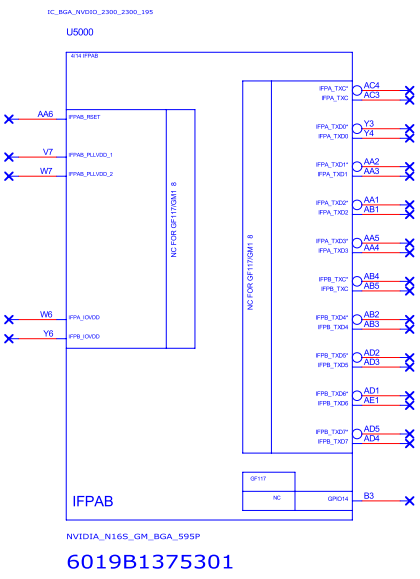
Block Diagram

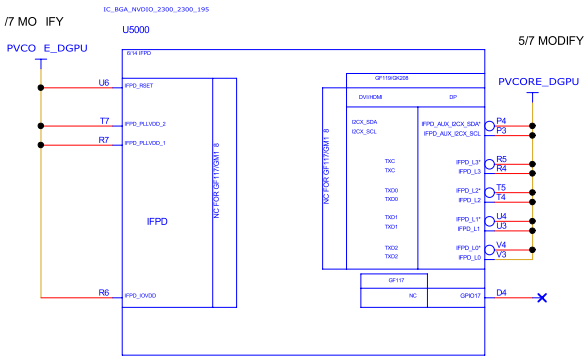
7e2 6 f 91126 1d7 3a62b79 3b1



7e2 6 f 91126 1d7 3a62b79 3b1



6019B1375301



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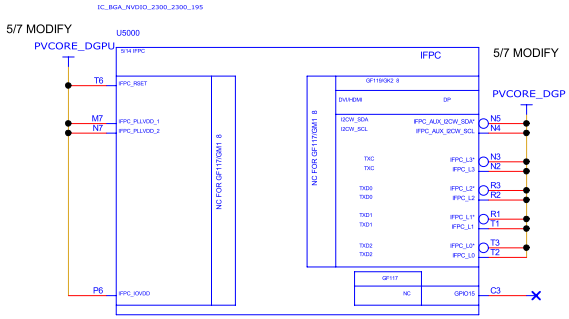

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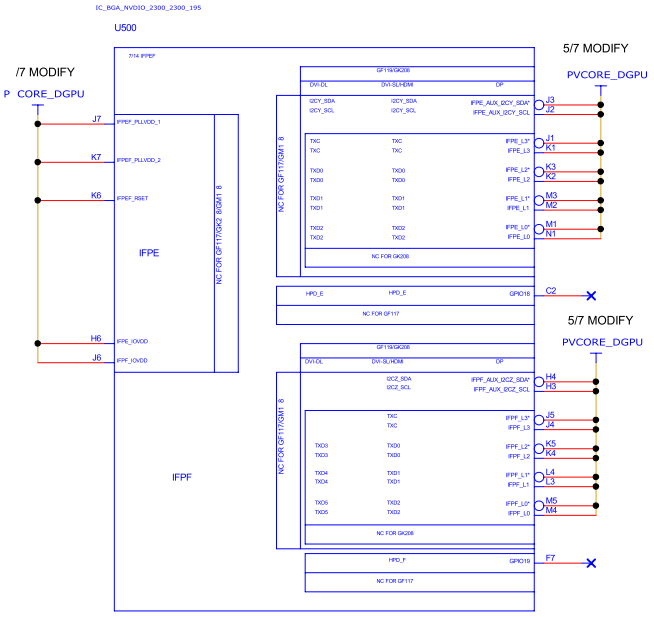

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TITLE
MODEL,PROJECT,FUNCTION
GPU-4

SIZE	CODE	DOC NUMBER	REV
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Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	N15S-GV	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	N15S-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	All GB2-64 N14 and GB2B-64 N15	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	N15S-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	N15S-GM/-GT	DEVID_SEL	PCIE_CFG		
STRAP0	N15S-GV	USER[3]	USER[2]	USER[1]	USER[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)			
STRAP1	N15S-GV	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP2	N15S-GV	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP3	N15S-GV	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	N15S-GV	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

15.5.14 DEVID_SEL Strap

This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVID straps. This strap only exists in the GB2B-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* for the latest configuration.

15.5.15 PCIE_CFG Strap

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing 3GIO_PADCFG. This strap only exists in the GB2B-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* for the latest configuration.

15.5.6 SMB_ALT_ADDR Strap

This strap is used to configure the I2CS address of a GPU or the I2CS slave address.

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

15.5.5 VGA_DEVICE Strap

The VGA_DEVICE strap is used to identify the device type (or class code) of the GPU within the PCI configuration space. Set 3D Acceleration Device for GPU in Optimus configuration or secondary GPU in SLI configuration.

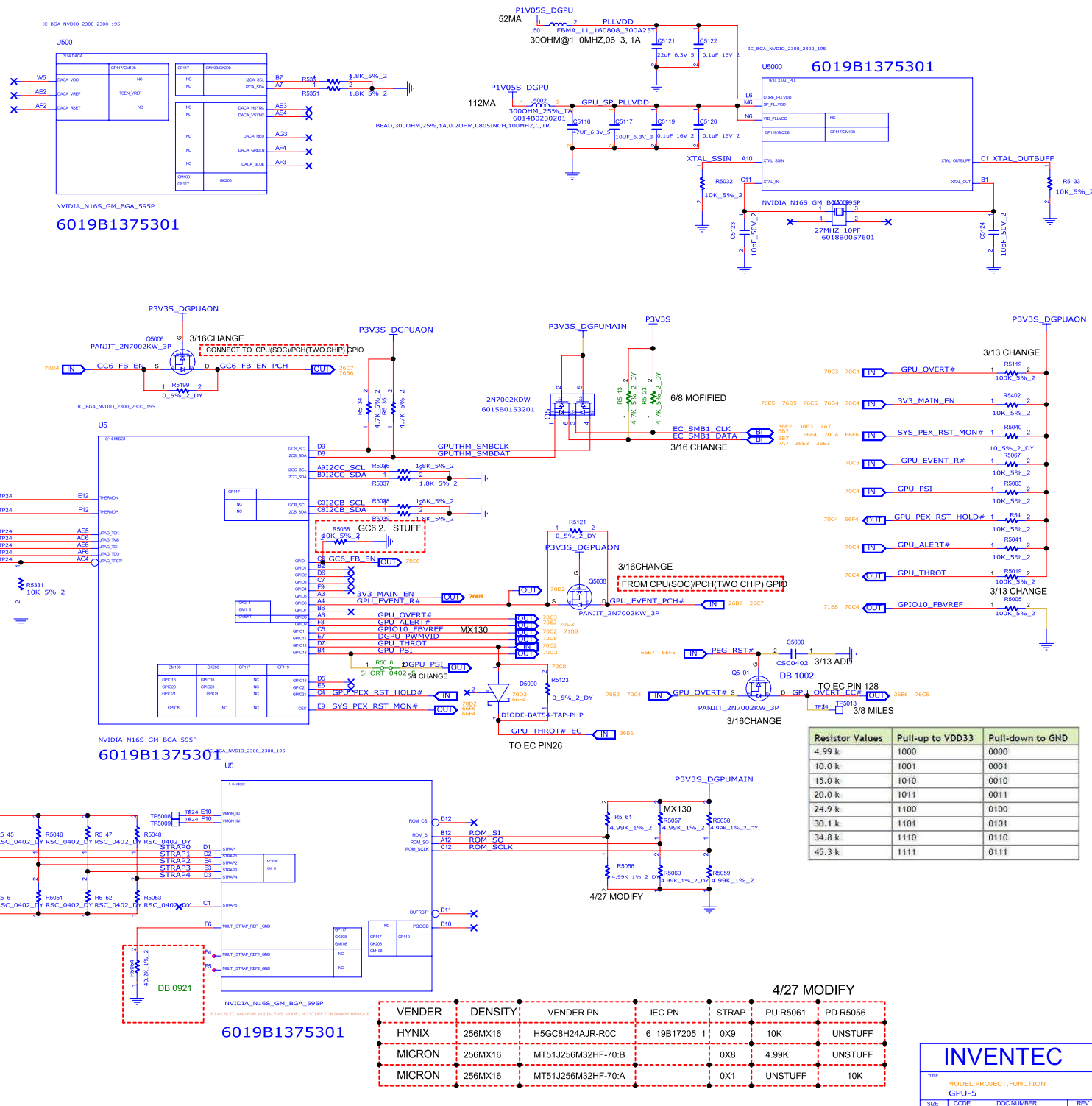
Table 15-7. VGA_DEVICE Settings

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device (Class Code 0302h)
1	Primary Display or VGA Device (Class Code 0300h)

Table 15-15. SORx_EXPOSED - Display Link to Usage Bit Mapping

Displays		HDMI/DP	DVI	LVDS	eDP	Not in Use
Standard Mode	FPAB		SOR0_EXP = 1	SOR0_EXP = 0		SOR0_EXP = 0
	FPC	SOR1_EXP = 1				SOR1_EXP = 0
	FPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	FPEF	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
Split Mode AB	FPA	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	FPB	SOR0_EXP = 1	SOR0_EXP = 1			SOR0_EXP = 0
	FPC	SOR1_EXP = 1				SOR1_EXP = 0
	FPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	FPEF	SOR3_EXP = 1				SOR3_EXP = 0
Split Mode EF	FPAB					
	FPC	SOR1_EXP = 1				SOR1_EXP = 0
	FPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	FPE	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	FPF	SOR0_EXP = 1	SOR0_EXP = 1		SOR0_EXP = 0	SOR0_EXP = 0

Note: GB2B-64 package GPUs are configured with no display output so all links are considered Not in Use.



Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

VENDER	DENSITY	VENDER PN	IEC PN	STRAP	PU R5061	PD R5056
HYNIX	256MX16	H5GC8H24AJR-R0C	6 19B17205 1	0X9	10K	UNSTUFF
MICRON	256MX16	MT51J256M32HF-70:B		0X8	4.99K	UNSTUFF
MICRON	256MX16	MT51J256M32HF-70:A		0X1	UNSTUFF	10K

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GPU-5

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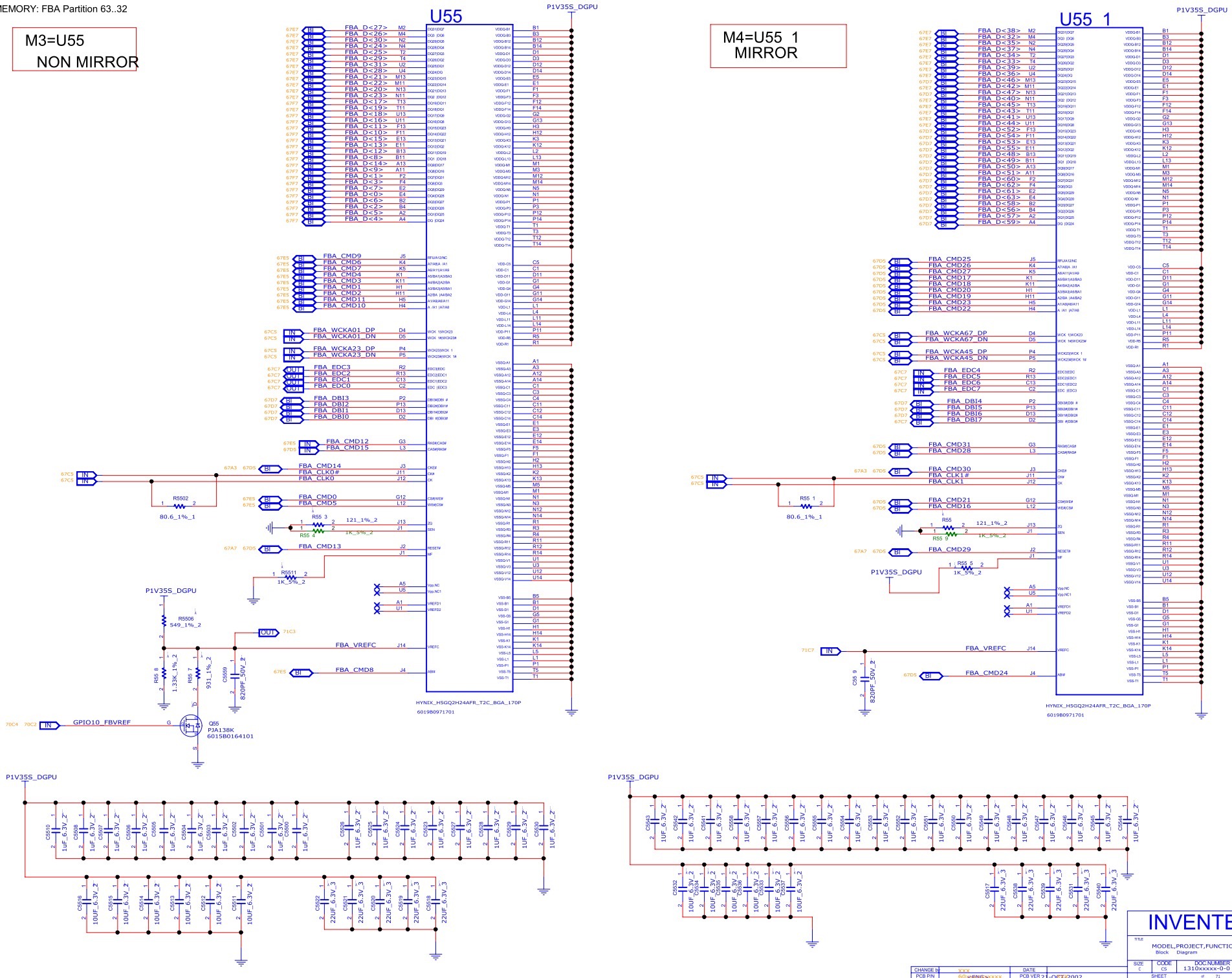
MEMORY: FBA Partition 31..
MEMORY: FBA Partition 63..32

M3=U55
NON MIRROR

M4=U55_1
MIRROR



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VMAX=1.2V BY PWM D=100%
VMIN=0.6V PWM D= %
VBOOT=0.875~0.9V BY PWM TRISTATE
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=9 US

5/ 4 CHANGE

PVBAT
PVBAT_PVCORE_DGPU1
PAD67010
POWERPAD_2_0610
PVCORE_DGPU
PVCORE_DGPU_SENSE
PVBAT_PVCORE_DGPU2
PAD67_11
VRB_VDD5
DGPU_PG
EN_DGPU
DGPU_PSI
DGPU_PWMVID
VRAPVCORE_DGPU_EN
VRAPVCORE_DGPU_PSI
VRAPVCORE_DGPU_VID6
U67
RICHTEK_RT8812AGQW_QFN_20P
Q67010
Q67020
ALPHA_AON6994_8P
L67 1
L67 2
PCME063T-R24MS1R195
VRBPVCORE_DGPU_GND
GPU_VSS_SENSE
GPU_VCC_SENSE
5/8 CHANGE

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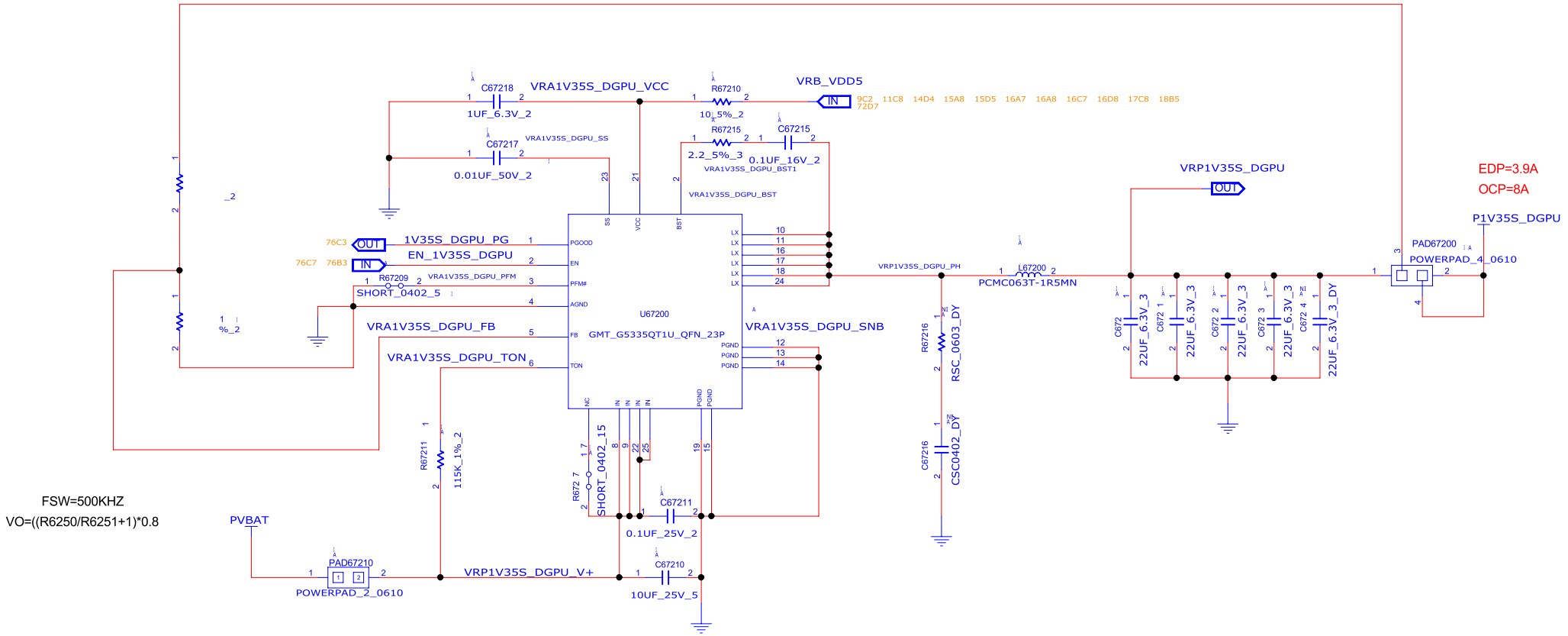

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

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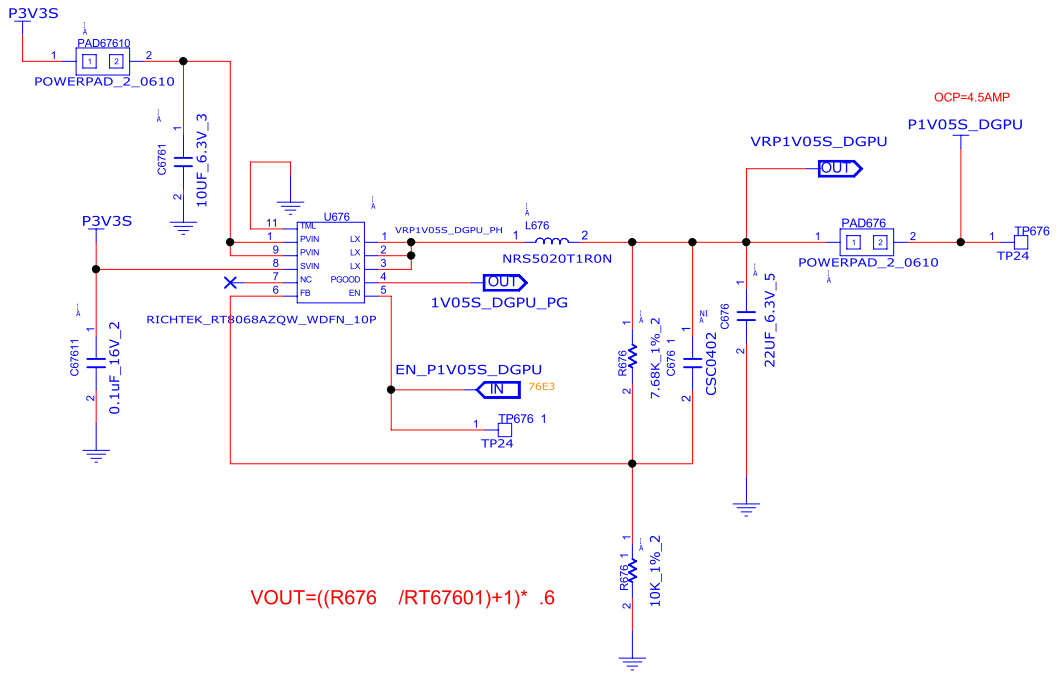

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MODEL,PROJECT,FUNCTION
Block Diagram

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PCB P/N	60xxxxxxxxx	PCB VER	XXX	CODE CS	REV X01
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

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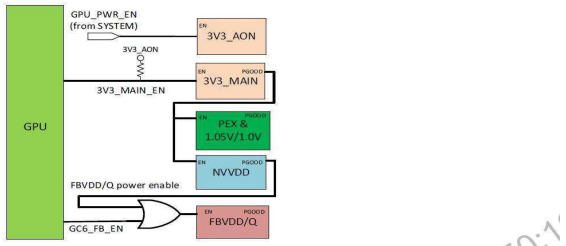
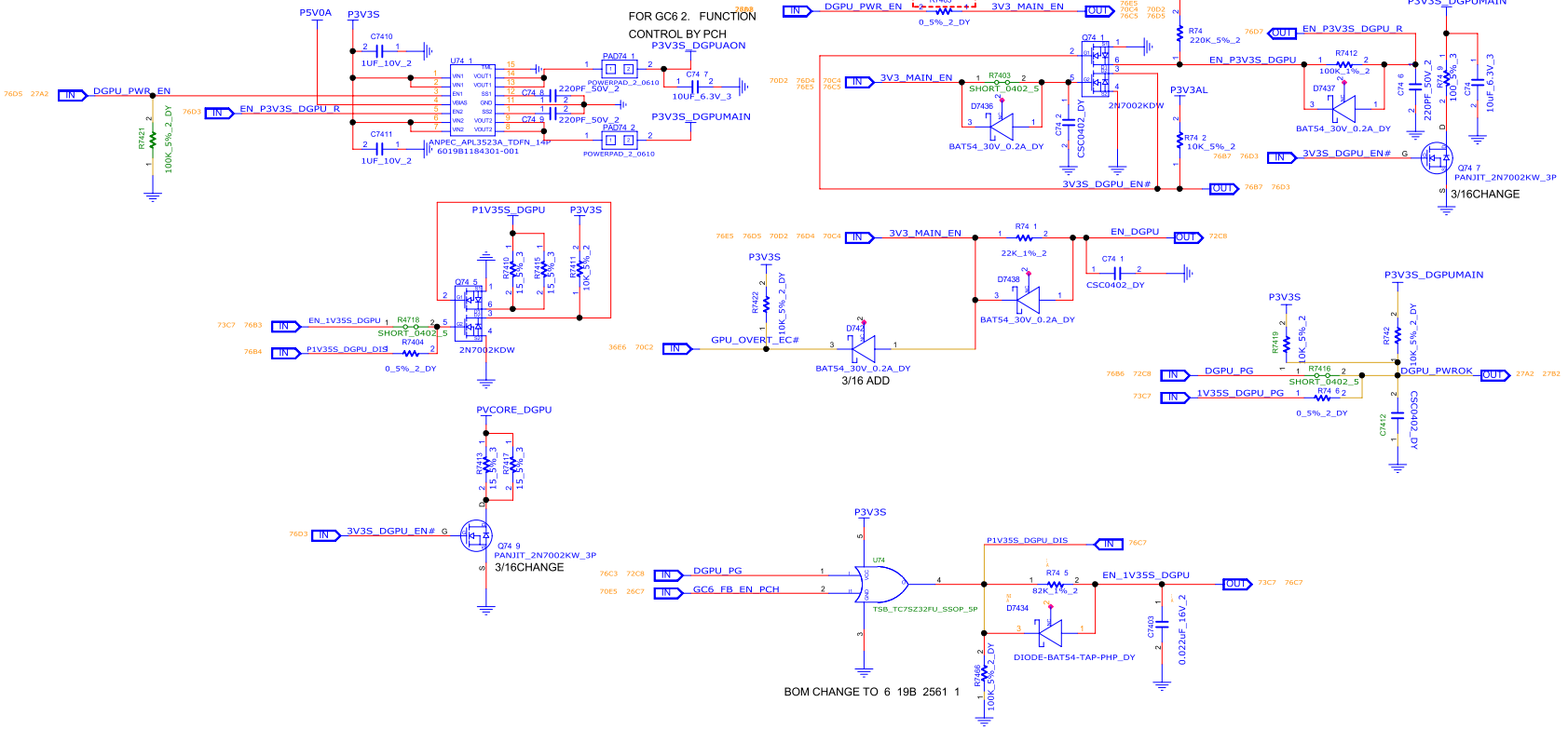


Figure 18-8. GC6 2.0 Voltage Regulator Complex Signal Connection

- **Cold boot/Optimus:** 3V3_AON & 3V3_MAIN → NVVDD → PEX_VDD → FBVDD/Q
- **GC6 2.0 Exit:** 3.3V_MAIN → NVVDD → PEX_VDD



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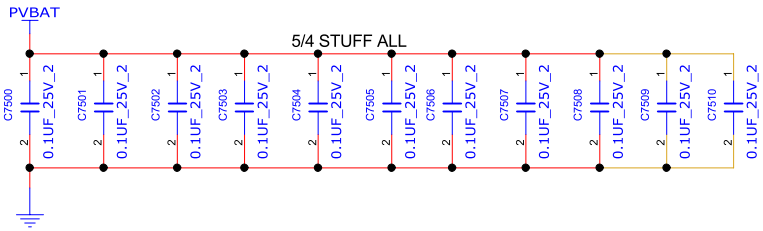

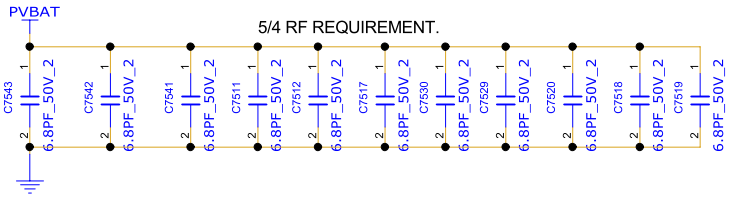

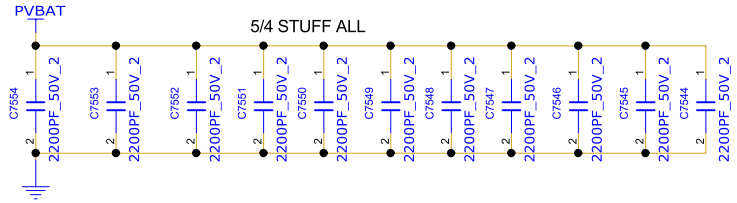

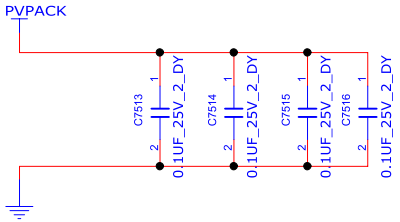

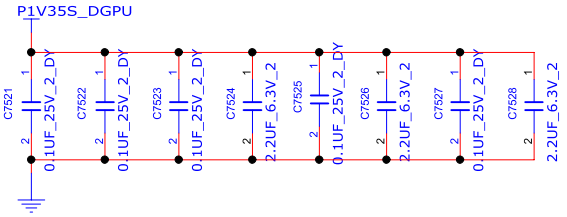

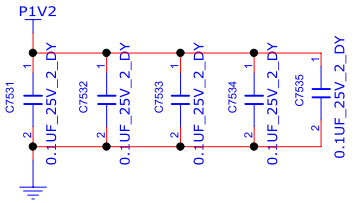

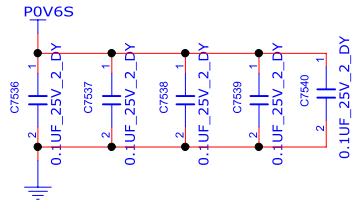

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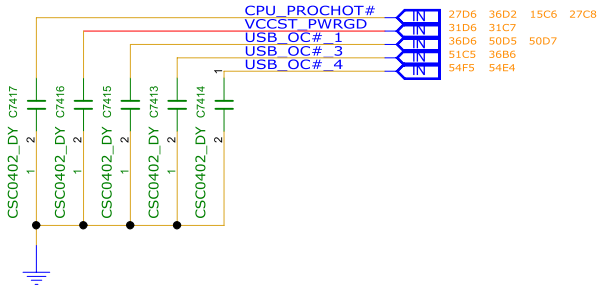

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