1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J70 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0002721096	PRODUCTION RELEASED	2014-04-15

LAST_MODIFIED=Tue Apr 15 17:23:51 2014

DRAWING
TITLE=J16 MLB_IG
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 15 17:23:51 2014

DRAWING TITLE: SCHEM,MLB,J70

Apple Inc.

DRAWING NUMBER: 051-1407 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 123
SHEET: 1 OF 81

Schematic / PCB #’s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-1407	1	SCH,MLB,J70	SCH	CRITICAL	
820-4668	1	PCBF,MLB,J70	PCB	CRITICAL	
685-1351	1	PCBA,MLB,J70,COMMON PARTS	CMNPTS		MLB_CMNPTS

Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-1058	PCBA,MLB,DEV,J70	DEVELOPMENT,J70_DEVEL
939-00046	PCBA,MLB,DEV,J70,CPU_INT	MLB_CMNPTS,ALTERNATE,CPU:SOCKET,DDR3:HYNIX_4GB_29nm,SSD:Y
639-6212	PCBA,MLB,J70,HY_4GB_38nm,HDD	MLB_CMNPTS,CPU:ULT,DDR3:HYNIX_4GB_38nm,SSD:N
639-6213	PCBA,MLB,J70,EL_4GB_38nm,HDD	MLB_CMNPTS,CPU:ULT,DDR3:ELPIDA_4GB_38nm,SSD:N
639-6214	PCBA,MLB,J70,HY_4GB_38nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_4GB_38nm,SSD:Y
639-6215	PCBA,MLB,J70,EL_4GB_38nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_4GB_38nm,SSD:Y
639-6216	PCBA,MLB,J70,HY_8GB_38nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_8GB_38nm,SSD:Y
639-6217	PCBA,MLB,J70,EL_8GB_38nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_8GB_38nm,SSD:Y
639-6218	PCBA,MLB,J70,HY_4GB_29nm,HDD	MLB_CMNPTS,CPU:ULT,DDR3:HYNIX_4GB_29nm,SSD:N
639-6219	PCBA,MLB,J70,EL_4GB_25nm,HDD	MLB_CMNPTS,CPU:ULT,DDR3:ELPIDA_4GB_25nm,SSD:N
639-6220	PCBA,MLB,J70,HY_4GB_29nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_4GB_29nm,SSD:Y
639-6221	PCBA,MLB,J70,EL_4GB_25nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_4GB_25nm,SSD:Y
639-6222	PCBA,MLB,J70,HY_8GB_29nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_8GB_29nm,SSD:Y
639-6223	PCBA,MLB,J70,EL_8GB_25nm,SSD	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_8GB_25nm,SSD:Y
685-1351	PCBA,MLB,J70,COMMON PARTS	J70_COMMON

BOM Groups

BOM GROUP	BOM OPTIONS
J70_COMMON	COMMON,ALTERNATE,J70_PROGPARTS,SMCREG:DIV,XDP,TEMPSNSDEV,SMBUS0:ISOL,SMBUS1:ISOL,AUDIO:I2S,RTCRST:Y
J70_PROGPARTS	SMC:PROG,BOOTROM:PROG,CAMROM:PROG,TBTROM:PROG,ENETROM:PROG
J70_DEVEL	XDP_CONN,LPCPLUS,TEMPSNSDEV

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00011	1	IC,CPU,HSW,SR16T,PRQ,1.4,15W,2+3,3M,BGA	U0500	CRITICAL	CPU:ULT
998-7866	1	INTERPOSER,BGA1168,SINGLE SIDE	U0500	CRITICAL	CPU:SOCKET

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1273	1	IC,TBT,RR-4C,A0,PRQ,CIO,FCBGA,288,T&R	U2800	CRITICAL	
343S0616	1	IC,BCM57766A,CIV+,A0,8x8	U3900	CRITICAL	

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB_38nm	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB_38nm
DDR3:HYNIX_8GB_38nm	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB_38nm
DDR3:ELPIDA_4GB_38nm	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB_38nm
DDR3:ELPIDA_8GB_38nm	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB_38nm
DDR3:HYNIX_4GB_29nm	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_4GB_29nm
DDR3:HYNIX_8GB_29nm	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:HYNIX_8GB_29nm
DDR3:ELPIDA_4GB_25nm	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_4GB_25nm
DDR3:ELPIDA_8GB_25nm	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:ELPIDA_8GB_25nm
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,38nm,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB_38nm
333S0681	4	IC,SDRAM,38nm,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB_38nm
333S0678	4	IC,SDRAM,38nm,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB_38nm
333S0666	4	IC,SDRAM,38nm,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB_38nm
333S0787	4	IC,SDRAM,29nm,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB_29nm
333S0785	4	IC,SDRAM,29nm,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB_29nm
333S0793	4	IC,SDRAM,25nm,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB_25nm
333S0791	4	IC,SDRAM,25nm,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB_25nm
333S0676	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0680	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00053	1	IC,EFI,V0174,J70	U5210	CRITICAL	BOOTROM:PROG
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S00050	1	IC,SMC-B1,EXTERNAL,V2.21F70,PVT,J70	U5000	CRITICAL	SMC:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50MIPS,SCPL FW,1578GA	U5000	CRITICAL	SMC:BLANK
341S3778	1	IC,CAMERA,FLASH,V7230,J16	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S00048	1	IC,EPROM,T29,REDWOOD RDG,V30.8,J70	U2890	CRITICAL	TBTROM:PROG
335S0915	1	IC,FLASH,SPI,4MBIT,50MHZ	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET SPI ROM,NYMONYX,V1.15,J16/J16G/J17	U3990	CRITICAL	ENETROM:PROG
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	ENETROM:BLANK

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0155	377S0104		ALL	USB3 diodes
377S0124	377S0057		ALL	TVS
376S1218	376S1081		ALL	P/NCh dual FET
155S0578	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uf 805 alt
197S0479	197S0478		ALL	12 MHz Cam. Xtal
197S0486	197S0478		ALL	12 MHz Cam. Xtal
107S0251	107S0249		ALL	Sense resistor
197S0481	197S0480		ALL	25MHz Xtal
197S0343	197S0480		ALL	25MHz Xtal
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
378S0391	378S0390		ALL	Debug LEDs
341S00016	341S3912		ALL	ENET ROM,ADESTO,V1.15
138S0747	138S0773		ALL	1uF,X6S,402
197S0542	197S0544		ALL	24 MHz PCH Xtal
197S0545	197S0544		ALL	24 Mhz PCH XTal
376S1217	376S0855		ALL	Dual N-Ch FET
376S1129	376S0855		ALL	Dual N-Ch FET
376S0572	376S0659		ALL	Single P-Ch FET
376S0972	376S1017		ALL	Single N-Ch FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1089	376S1128		ALL	Dual N-Ch FET
155S0660	155S0513		ALL	22OHM EMI BEAD
155S0694	155S0387		ALL	470OHM EMI BEAD
127S0164	127S0162		ALL	1UF 25V TANT
376S1217	376S0855	SSD:Y	ALL	Dual N-Ch FET
376S1129	376S0855	SSD:Y	ALL	Dual N-Ch FET
197S0369	197S0392		ALL	32 KHz PCH Xtal
197S0399	197S0392		ALL	32 KHz PCH Xtal
311S0649	311S0541		ALL	Single AND Gate
107S0375	107S0151		ALL	DDR Sense Res
107S0372	107S0181		ALL	CPU VR Sense Res

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
N/A	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

SYNC_MASTER=J70 TONY SYNC_DATE=11/06/2013

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

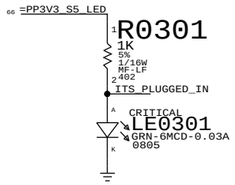
REVISION A.0.0

BRANCH

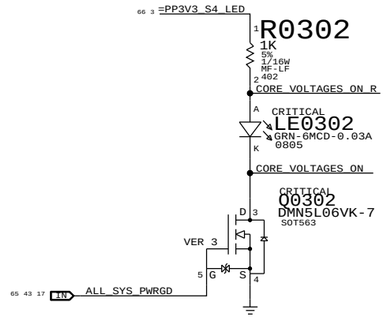
PAGE 2 OF 123

SHEET 2 OF 81

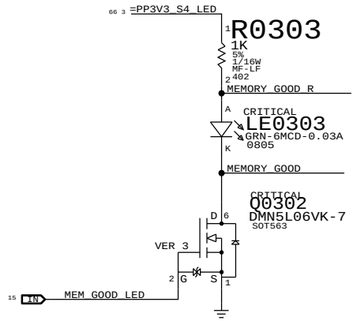
S5 Led



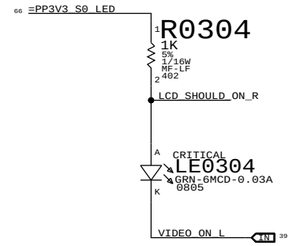
ALL_SYS_PWRGD Led



MEM_GOOD Led



VIDEO ON Led



SYNC_MASTER=J70 GAREN SYNC_DATE=10/22/2013

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

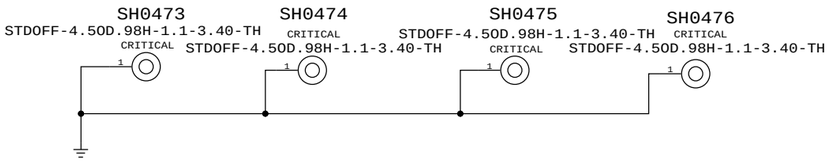
REVISION: A.0.0

BRANCH:

PAGE: 3 OF 123

SHEET: 3 OF 81

CPU HEATSINK MOUNTING FEATURES

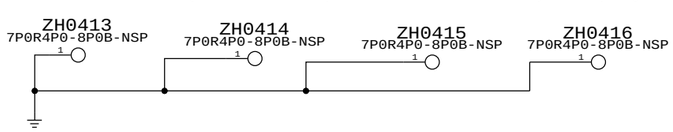


HEATSINK STABILITY MOUNTING FEATURES

APN:860-1532

Rear Cover

APN:998-4559 (Plated holes, 4mm inner diameter, 8mm pad)

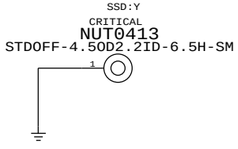


WIRELESS CARD MTG HOLES

APN:998-4938 (Plated holes, 1.9mm inner diameter, 4.3mm pad)

SSD STANDOFF

APN: 860-1624



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 4 OF 123

SHEET: 4 OF 81

DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 1 OF 19

DDI

DP_TBTSNK0_ML_C_N<0>	C54	DDI1_TXN0		EDP_TXN0	C45	DP_INT_ML_N<0>	40 80
DP_TBTSNK0_ML_C_P<0>	C55	DDI1_TXP0		EDP_TXP0	B46	DP_INT_ML_P<0>	40 80
DP_TBTSNK0_ML_C_N<1>	B58	DDI1_TXN1		EDP_TXN1	A47	DP_INT_ML_N<1>	40 80
DP_TBTSNK0_ML_C_P<1>	C58	DDI1_TXP1		EDP_TXP1	B47	DP_INT_ML_P<1>	40 80
DP_TBTSNK0_ML_C_N<2>	B55	DDI1_TXN2		EDP_TXN2	C47	DP_INT_ML_N<2>	40
DP_TBTSNK0_ML_C_P<2>	A55	DDI1_TXP2		EDP_TXP2	C46	DP_INT_ML_P<2>	40
DP_TBTSNK0_ML_C_N<3>	A57	DDI1_TXN3		EDP_TXN3	A49	DP_INT_ML_N<3>	40
DP_TBTSNK0_ML_C_P<3>	B57	DDI1_TXP3		EDP_TXP3	B49	DP_INT_ML_P<3>	40
DP_TBTSNK1_ML_C_N<0>	C51	DDI2_TXN0					
DP_TBTSNK1_ML_C_P<0>	C50	DDI2_TXP0					
DP_TBTSNK1_ML_C_N<1>	C53	DDI2_TXN1		EDP_AUXN	A45	DP_INT_AUX_N	40 80
DP_TBTSNK1_ML_C_P<1>	B54	DDI2_TXP1		EDP_AUXP	B45	DP_INT_AUX_P	40 80
DP_TBTSNK1_ML_C_N<2>	C49	DDI2_TXN2					
DP_TBTSNK1_ML_C_P<2>	B50	DDI2_TXP2					
DP_TBTSNK1_ML_C_N<3>	A53	DDI2_TXN3		EDP_RCOMP	D20	MCP_EDP_RCOMP	71
DP_TBTSNK1_ML_C_P<3>	B53	DDI2_TXP3		EDP_DISP_UTIL	A43	TP_EDP_DISP_UTIL	

eDP Port Assignment:

Internal panel

PPVCOMP_S0_CPU

R0530
24.9
1%
1/20W
MF
201
PLACE_NEAR=U0500.D20:12.7mm

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 17 OF 19

	NO_TEST				NO_TEST		
MCP_DC_AW2_AY2	TRUE	AY2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A3	TRUE	MCP_DC_A3_B3
MCP_DC_AW3_AY3	TRUE	AY3	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A4		MCP_DC_A4 → TP0500
MCP_DC_AY60		AY60	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A60		MCP_DC_A60 → TP0510
MCP_DC_AW61_AY61	TRUE	AY61	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A61	TRUE	MCP_DC_A61_B61
MCP_DC_AW62_AY62	TRUE	AY62	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A62		MCP_DC_A62 → TP0511
MCP_DC_B2		B2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AV1		MCP_DC_AV1 → TP0520
MCP_DC_A3_B3	TRUE	B3	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW1		MCP_DC_AW1 → TP0521
MCP_DC_A61_B61	TRUE	B61	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW2	TRUE	MCP_DC_AW2_AY2
MCP_DC_B62_B63	TRUE	B62	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW3	TRUE	MCP_DC_AW3_AY3
		B63	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW61	TRUE	MCP_DC_AW61_AY61
MCP_DC_C1_C2	TRUE	C1	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW62	TRUE	MCP_DC_AW62_AY62
		C2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW63		MCP_DC_AW63 → TP0530

TP0531 (TP-P6)
TP0501 (TP-P6)

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 18 OF 19
SPARE

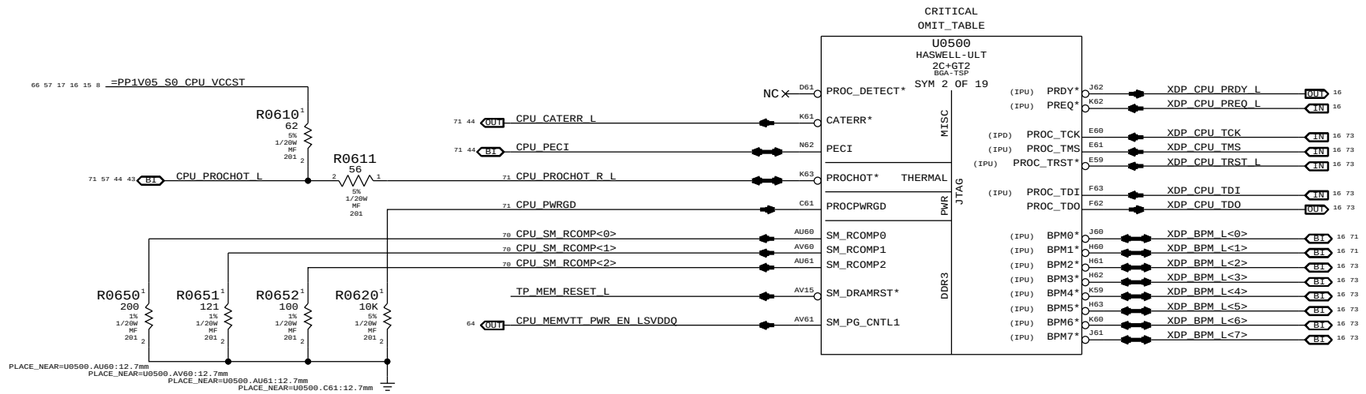
NC	AT2	RSVD	N23 NC
NC	AU44	RSVD	R23 NC
NC	AV44	RSVD	T23 NC
NC	D15	RSVD	U10 NC
NC	F22	RSVD	AL1 NC
NC	H22	RSVD	AM11 NC
NC	J21	RSVD	AP7 NC
		RSVD	AU10 NC
		RSVD	AU15 NC
		RSVD	AW14 NC
		RSVD	AY14 NC

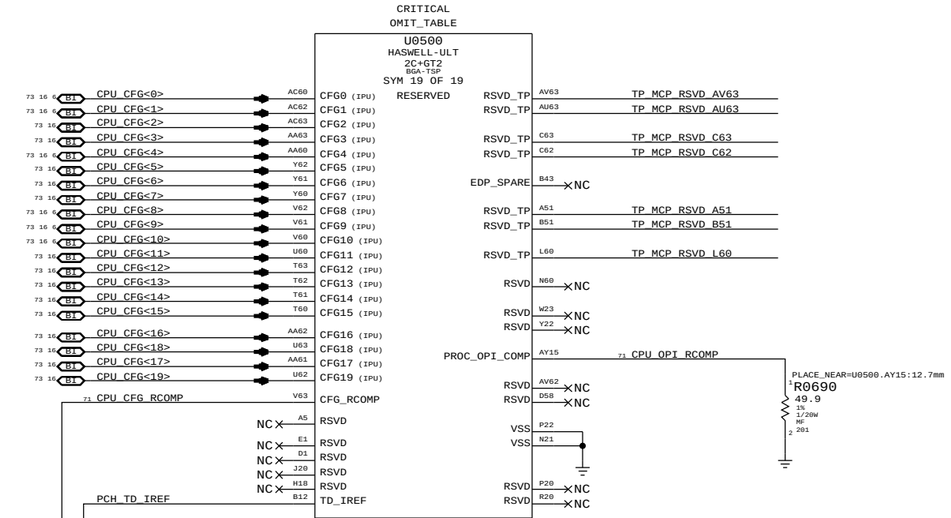
SYNC_MASTER=J70_TONY SYNC_DATE=09/11/2013

PAGE TITLE
CPU GFX/NCTF/RSVD

Apple Inc.

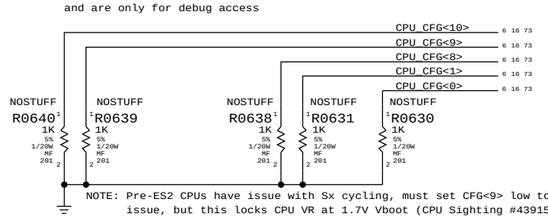
DRAWING NUMBER 051-1407
SIZE D
REVISION A.0.0
BRANCH
PAGE 5 OF 123
SHEET 5 OF 81



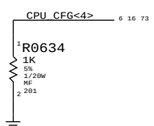


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



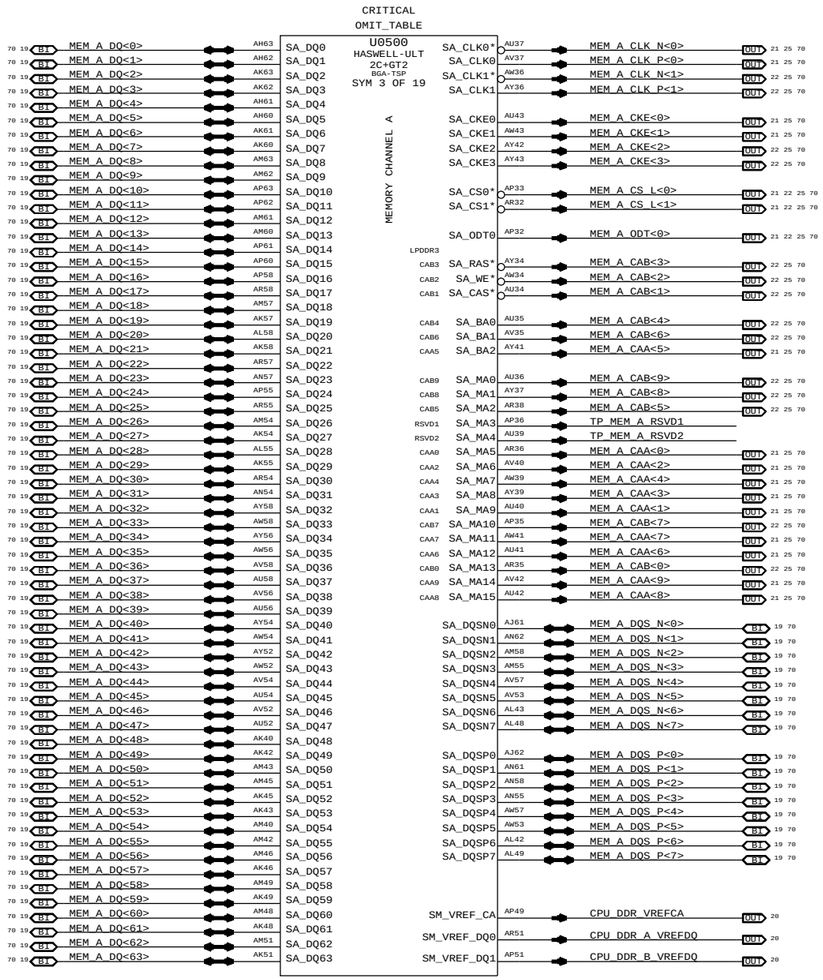
SYNC MASTER=J70 TONY
SYNC DATE=09/24/2013

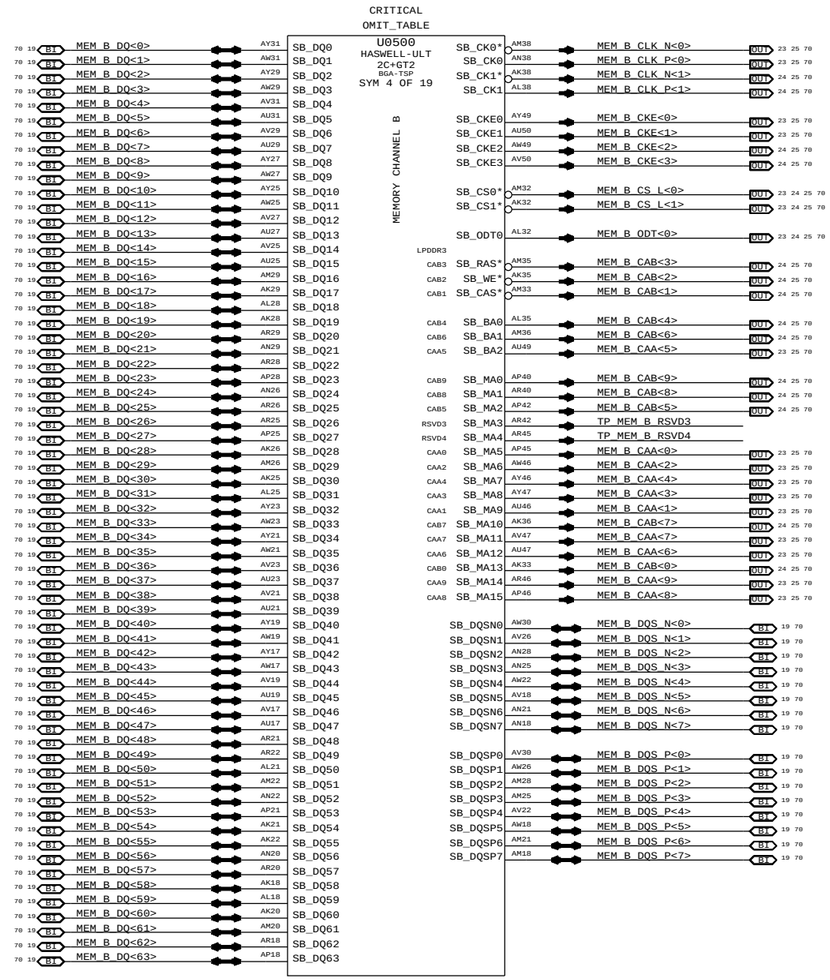
PAGE TITLE

CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER 051-1407
SIZE D
REVISION A.0.0
BRANCH
PAGE 6 OF 123
SHEET 6 OF 81





SYNC_MASTER=J70 DINI SYNC_DATE=09/23/2013

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

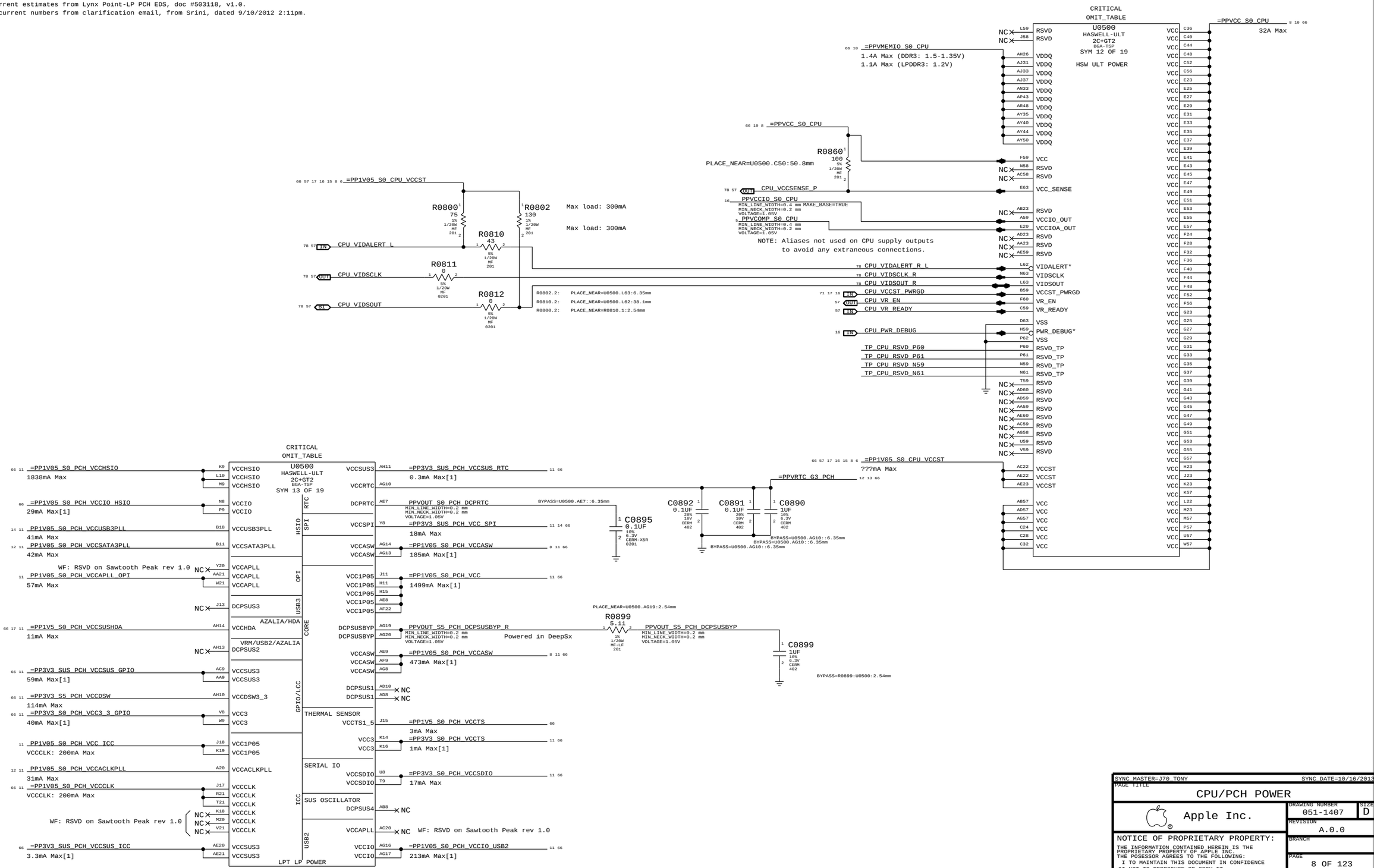
REVISION A.0.0

BRANCH

PAGE 7 OF 123

SHEET 7 OF 81

HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J70_TONY	SYNC_DATE=10/16/2013
PAGE TITLE	CPU/PCH POWER
Apple Inc.	DRAWING NUMBER 051-1407 · SIZE D · REVISION A.0.0 · BRANCH · PAGE 8 OF 123 · SHEET 8 OF 81

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N → OUT 57 78

R0960
100
5%
1/20W
MF
201
PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J41_MLB SYNC_DATE=08/27/2013

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

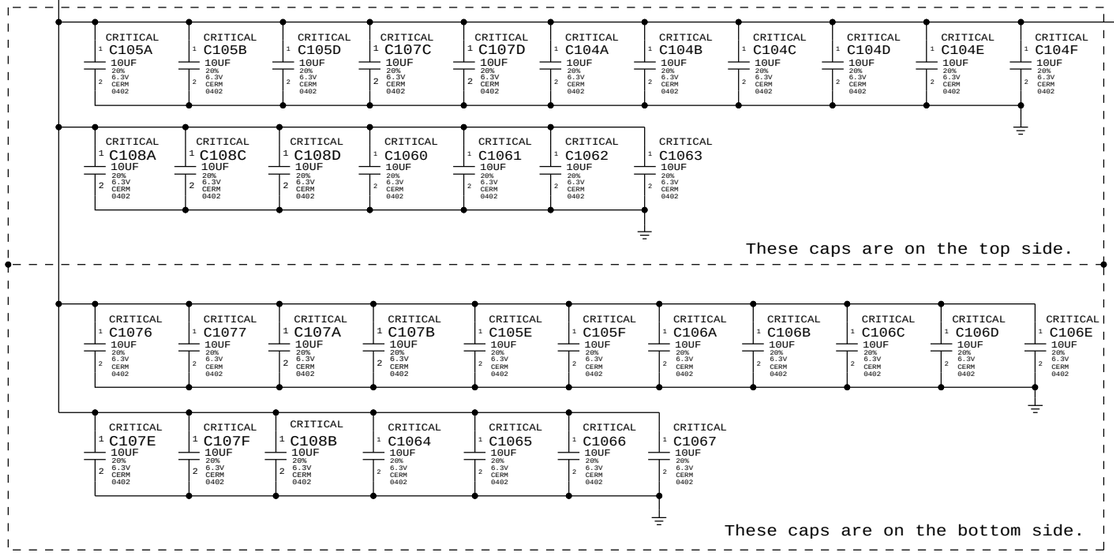
DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 9 OF 123
SHEET 9 OF 81

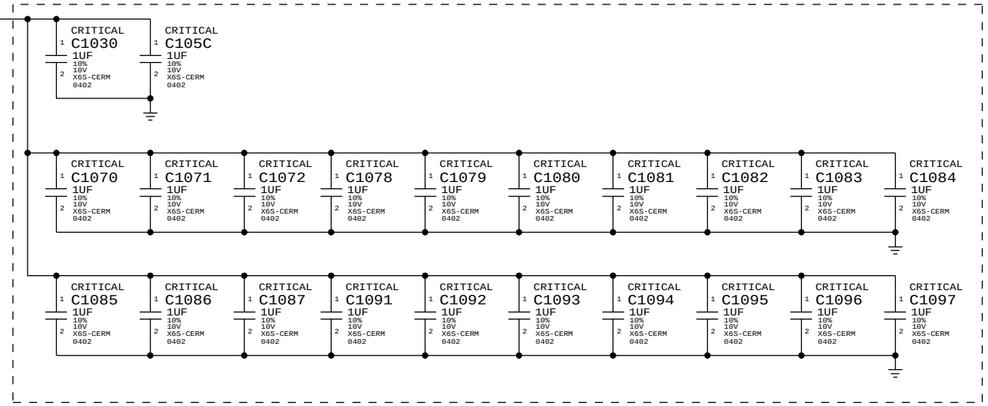
All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff
J70 implementation : 18x 10uF 0402 mirrored stuff, 32x 10uF single sided no stuff

66 8 =PPVCC_S0_CPU

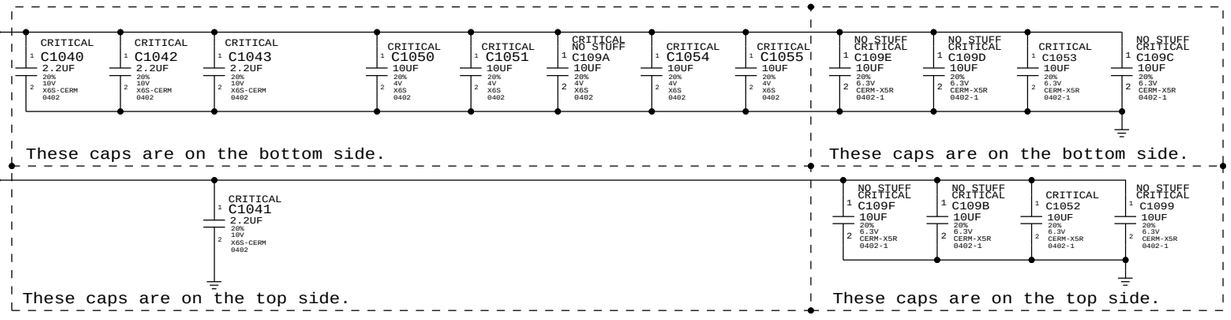




CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 6x 10uF no stuff, 1x 270 uF Bulk

66 8 =PPVMEMIO_S0_CPU



CRITICAL C1056 270UF-0.006OHM 20% 2V TANT CASE-D2

SYNC_MASTER=J70_TONY SYNC_DATE=11/14/2013

PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 10 OF 123
SHEET 10 OF 81

PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
66 8 =PP3V3_S5_PCH_VCCDSW
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
66 14 8 =PP3V3_SUS_PCH_VCC_SPI
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500.Y8::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
66 8 =PP3V3_SUS_PCH_VCCSUS_GPIO
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9::12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
66 8 =PP3V3_SUS_PCH_VCCSUS_RTC
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11::6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V SDIO PWR)
66 8 =PP3V3_S0_PCH_VCCSDIO
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 1.5V HDA PWR)
66 17 8 =PP1V5_S0_PCH_VCCSUSHDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
66 8 =PP3V3_S0_PCH_VCC3_3_GPIO
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8::12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
66 8 =PP3V3_S0_PCH_VCCTS
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.K14::6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
66 8 =PP1V05_S0_PCH_VCCASW
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9::12.7mm
BYPASS=U0500.AE9::6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
66 8 =PP1V05_S0_PCH_VCC
C1255 10UF 20% 6.3V CERM-X5R 0402-1
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11::12.7mm
BYPASS=U0500.J11::6.35mm
BYPASS=U0500.AE8::6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
66 8 =PP1V05_S0_PCH_VCCHSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9::6.35mm
BYPASS=U0500.L10::6.35mm
BYPASS=U0500.M9::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
66 8 =PP1V05_S0_PCH_VCCIO_USB2
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
66 8 =PP1V05_S0_PCH_VCCCLK
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17::6.35mm
BYPASS=U0500.R21::6.35mm

66 =PP1V05_S0_PCH_PLLFILTERS
R1270 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402-1
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::6.35mm
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max 8 12

R1275 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402-1
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::6.35mm
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max 8

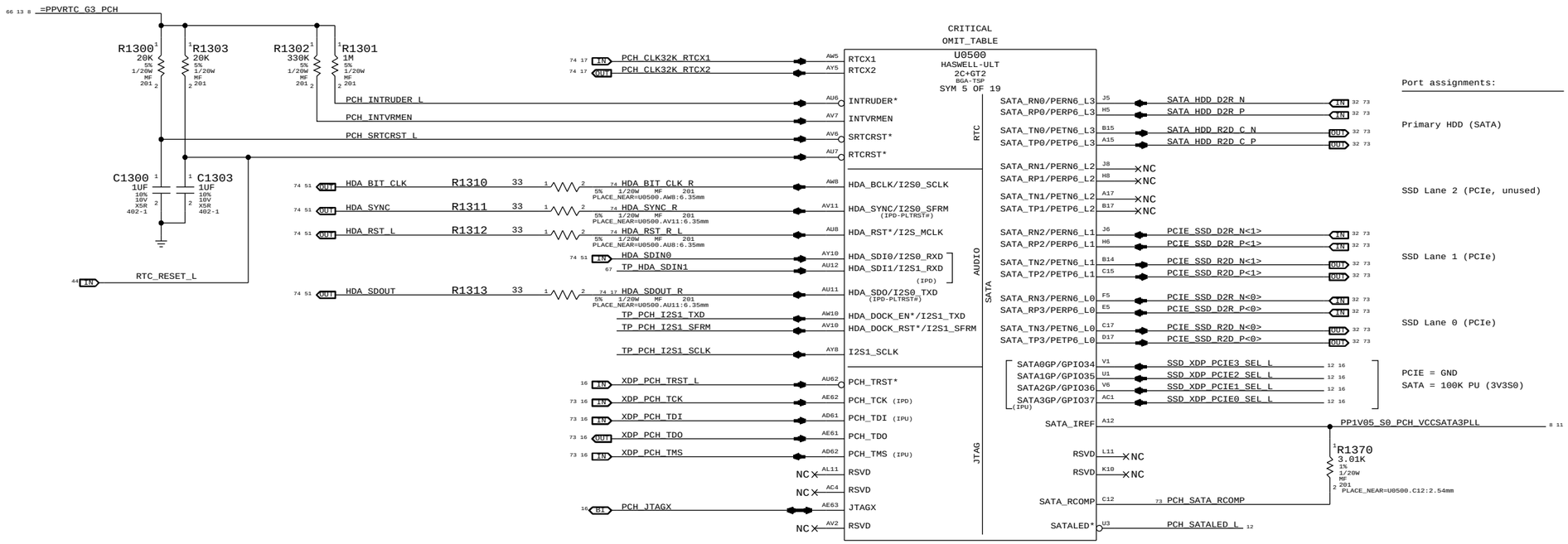
R1280 0 5% 1/10W MF-LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
C1280 47UF 20% 4V CERM-X5R 0805-1
C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402-1
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::6.35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max 8

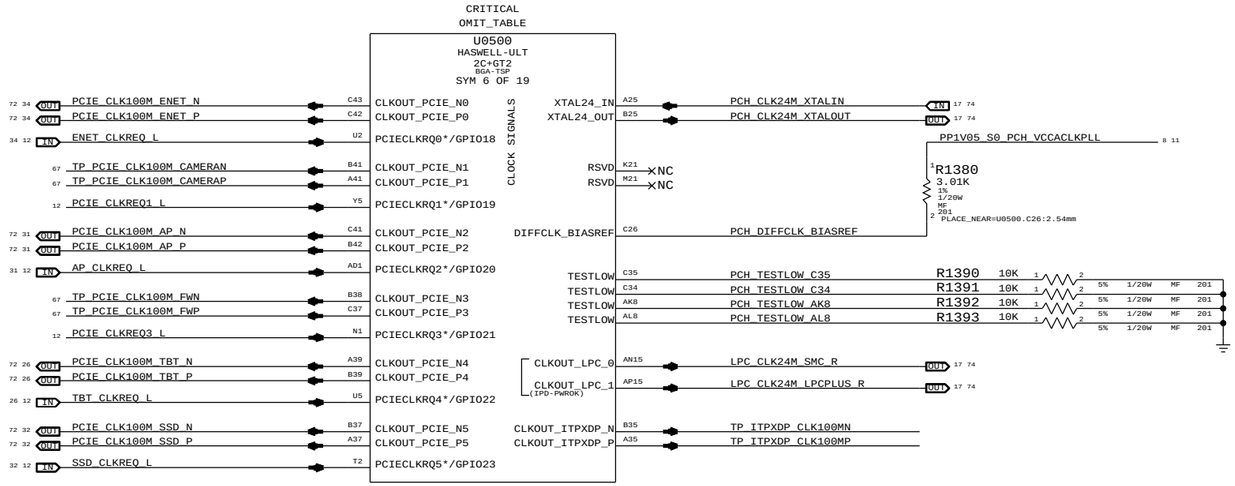
66 =PP1V05_S0_PCH_VCCPLL_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
C1290 47UF 20% 4V CERM-X5R 0805-1
C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402-1
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::6.35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max 8 12

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
C1295 47UF 20% 4V CERM-X5R 0805-1
NO STUFF
C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402-1
BYPASS=U0500.B18::12.7mm
BYPASS=U0500.B18::12.7mm
BYPASS=U0500.B18::6.35mm
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max 8 14

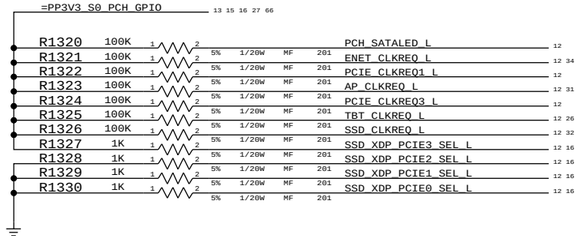
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J41_MLB SYNC_DATE=08/27/2013
PAGE TITLE
PCH Decoupling
Apple Inc.
DRAWING NUMBER 051-1407
SIZE D
REVISION A.0.0
BRANCH
PAGE 12 OF 123
SHEET 11 OF 81





NOTE: Haswell ULT requires that CLQREQ_n be mapped to ROOT_PORT_n+1 to properly support CLKREQs for PCIE devices.

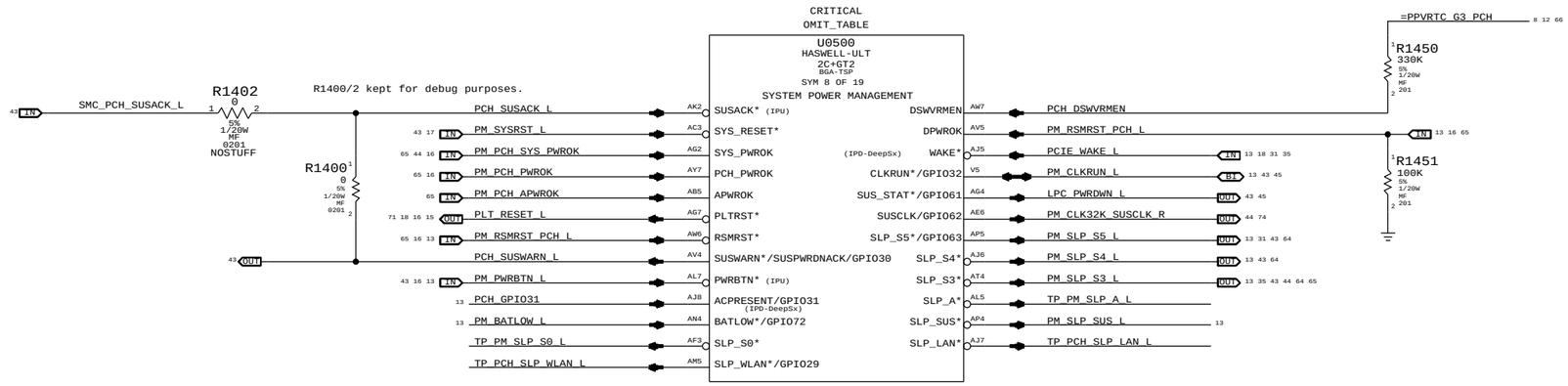


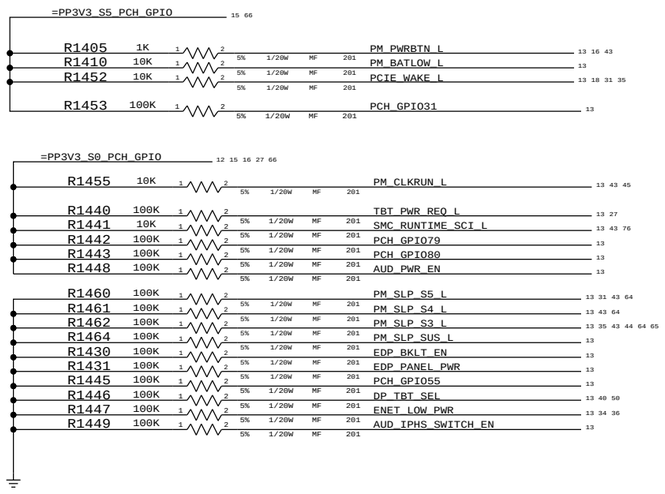
SYNC MASTER=J70 GAREN | SYNC DATE=01/30/2014

PAGE TITLE: PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER: 051-1407 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 13 OF 123
SHEET: 12 OF 81





SYNC_MASTER=J70_NICK	SYNC_DATE=11/20/2013
PAGE TITLE	PCH PM/PCI/GFX
Apple Inc.	DRAWING NUMBER 051-1407 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 14 OF 123
	SHEET 13 OF 81

PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Ethernet

USB3 Port Assignments:

Ext C (SS)

Ext D (SS)

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 11 OF 19

72 26 IN	PCIE_TBT_D2R_N<0>	F10	PERN5_L0
72 26 IN	PCIE_TBT_D2R_P<0>	E10	PERP5_L0
72 26 OUT	PCIE_TBT_R2D_C_N<0>	C23	PETN5_L0
72 26 OUT	PCIE_TBT_R2D_C_P<0>	C22	PETP5_L0
72 26 IN	PCIE_TBT_D2R_N<1>	F8	PERN5_L1
72 26 IN	PCIE_TBT_D2R_P<1>	E8	PERP5_L1
72 26 OUT	PCIE_TBT_R2D_C_N<1>	B23	PETN5_L1
72 26 OUT	PCIE_TBT_R2D_C_P<1>	A23	PETP5_L1
72 26 IN	PCIE_TBT_D2R_N<2>	H10	PERN5_L2
72 26 IN	PCIE_TBT_D2R_P<2>	G10	PERP5_L2
72 26 OUT	PCIE_TBT_R2D_C_N<2>	B21	PETN5_L2
72 26 OUT	PCIE_TBT_R2D_C_P<2>	C21	PETP5_L2
72 26 IN	PCIE_TBT_D2R_N<3>	E6	PERN5_L3
72 26 IN	PCIE_TBT_D2R_P<3>	F6	PERP5_L3
72 26 OUT	PCIE_TBT_R2D_C_N<3>	B22	PETN5_L3
72 26 OUT	PCIE_TBT_R2D_C_P<3>	A21	PETP5_L3
72 31 IN	PCIE_AP_D2R_N	G11	PERN3
72 31 IN	PCIE_AP_D2R_P	F11	PERP3
72 31 OUT	PCIE_AP_R2D_C_N	C29	PETN3
72 31 OUT	PCIE_AP_R2D_C_P	B30	PETP3
72 34 IN	PCIE_ENET_D2R_N	F13	PERN4
72 34 IN	PCIE_ENET_D2R_P	G13	PERP4
72 34 OUT	PCIE_ENET_R2D_C_N	B29	PETN4
72 34 OUT	PCIE_ENET_R2D_C_P	A29	PETP4
75 42 IN	USB3_EXTC_D2R_N	G17	PERN1/USB3RN2
75 42 IN	USB3_EXTC_D2R_P	F17	PERP1/USB3RP2
75 42 OUT	USB3_EXTC_R2D_CF_N	C30	PETN1/USB3TN2
75 42 OUT	USB3_EXTC_R2D_CF_P	C31	PETP1/USB3TP2
75 42 IN	USB3_EXTD_D2R_N	F15	PERN2/USB3RN3
75 42 IN	USB3_EXTD_D2R_P	G15	PERP2/USB3RP3
75 42 OUT	USB3_EXTD_R2D_CF_N	B31	PETN2/USB3TN3
75 42 OUT	USB3_EXTD_R2D_CF_P	A31	PETP2/USB3TP3
NC		E15	RSVD
NC		E13	RSVD
72	PCH_PCIE_RCOMP	A27	PCIE_RCOMP
		B27	PCIE_IREF

PCI-E / USB

USB2N0	AN8	USB_EXTA_0_N	B! 41 75
USB2P0	AM8	USB_EXTA_0_P	B! 41 75
USB2N1	AR7	USB_EXTB_1_N	B! 41 75
USB2P1	AT7	USB_EXTB_1_P	B! 41 75
USB2N2	AR8	USB_EXTC_2_N	B! 42 75
USB2P2	AP8	USB_EXTC_2_P	B! 42 75
USB2N3	AR10	USB_EXTD_3_N	B! 42 75
USB2P3	AT10	USB_EXTD_3_P	B! 42 75
USB2N4	AM15	USB_CAMERA_N	B! 37 75
USB2P4	AL15	USB_CAMERA_P	B! 37 75
USB2N5	AM13	USB_BT_N	B! 31 75
USB2P5	AN13	USB_BT_P	B! 31 75
USB2N6	AP11	NC	
USB2P6	AN11	NC	
USB2N7	AR13	NC	
USB2P7 (IPD)	AP13	NC	
USB3RN0	G20	USB3_EXTA_D2R_N	IN 41 75
USB3RP0	H20	USB3_EXTA_D2R_P	IN 41 75
USB3TN0	C33	USB3_EXTA_R2D_CF_N	OUT 41 75
USB3TP0	B34	USB3_EXTA_R2D_CF_P	OUT 41 75
USB3RN1	E18	USB3_EXTB_D2R_N	IN 41 75
USB3RP1	F18	USB3_EXTB_D2R_P	IN 41 75
USB3TN1	B33	USB3_EXTB_R2D_CF_N	OUT 41 75
USB3TP1	A33	USB3_EXTB_R2D_CF_P	OUT 41 75
USBRBIAS*	AJ10	75 PCH_USB_RBIAS	
USBRBIAS	AJ11		
RSVD	AN10	NC	
RSVD	AM10	NC	
OC0*/GPIO40	AL3	XDP_USB_EXTA_OC_L	IN 14 16
OC1*/GPIO41	AT1	XDP_USB_EXTB_OC_L	IN 14 16
OC2*/GPIO42	AH2	XDP_USB_EXTC_OC_L	IN 14 16
OC3*/GPIO43	AV3	XDP_USB_EXTD_OC_L	IN 14 16

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

Ext C (LS/FS/HS)

Ext D (LS/FS/HS)

Camera

BT

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

11 8 PP1V05_S0_PCH_VCCUSB3PLL

R1500 1
3.01K
1% 1/20W MF 201
PLACE_NEAR=U0500.A27:6.35mm

R1570 1
22.6
1% 1/20W MF 201
PLACE_NEAR=U0500.AJ10:6.35mm

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 7 OF 19

74 45 43 B!	LPC_AD<0>	R1540 33	AU14	LAD0 (IPU)
74 45 43 B!	LPC_AD<1>	R1541 33	AW12	LAD1
74 45 43 B!	LPC_AD<2>	R1542 33	AY12	LAD2
74 45 43 B!	LPC_AD<3>	R1543 33	AW11	LAD3
74 45 43 OUT	LPC_FRAME_L	R1544 33	AV12	LFRAME*
74 45 OUT	SPI_CLK_R		AA3	SPI_CLK (IPU)
74 45 OUT	SPI_CS0_R_L		Y7	SPI_CS0* (IPU)
	TP_SPI_CS1_L		Y4	SPI_CS1* (IPU)
	TP_SPI_CS2_L		AC2	SPI_CS2* (IPU)
74 45 B!	SPI_MOSI_R		AA2	SPI_MOSI (IPU/IPD)
74 45 B!	SPI_MISO		AA4	SPI_MISO (IPU)
14	SPI_IO<2>		Y6	SPI_IO2 (IPU)
14	SPI_IO<3>		AF1	SPI_IO3 (IPU)

74 45 43 B! LPC_AD_R<0> … LPC_AD_R<3>
74 45 43 OUT LPC_FRAME_R_L

LPC / SMBUS / SPI / C-LINK

SMBALERT*/GPIO11	AN2	PCH_SMBALERT_L	14
SMBCLK	AP2	SMBUS_PCH_CLK	OUT 46 76
SMBDATA	AH1	SMBUS_PCH_DATA	B! 46 76
SML0ALERT*/GPIO60	AL2	WOL_EN	OUT 14 35
SML0CLK	AN1	SML_PCH_0_CLK	OUT 46 76
SML0DATA	AK1	SML_PCH_0_DATA	B! 46 76
SML1ALERT*/PCHHOT*/GPIO73	AU4	PCH_SML1ALERT_L	14
SML1CLK_GPIO75	AU3	SML_PCH_1_CLK	OUT 46
SML1DATA/GPIO74	AH3	SML_PCH_1_DATA	B! 46
(IPU/IPD) CL_CLK	AF2	TP_CLINK_CLK	
(IPU/IPD) CL_DATA	AD2	TP_CLINK_DATA	
CL_RST*	AF4	TP_CLINK_RESET_L	

=PP3V3_SUS_PCH_GPIO 66

R1579	100K	PCH_SML1ALERT_L	14
R1580	100K	XDP_USB_EXTA_OC_L	14 16
R1581	100K	XDP_USB_EXTB_OC_L	14 16
R1582	100K	XDP_USB_EXTC_OC_L	14 16
R1583	100K	XDP_USB_EXTD_OC_L	14 16
R1590	100K	PCH_SMBALERT_L	14

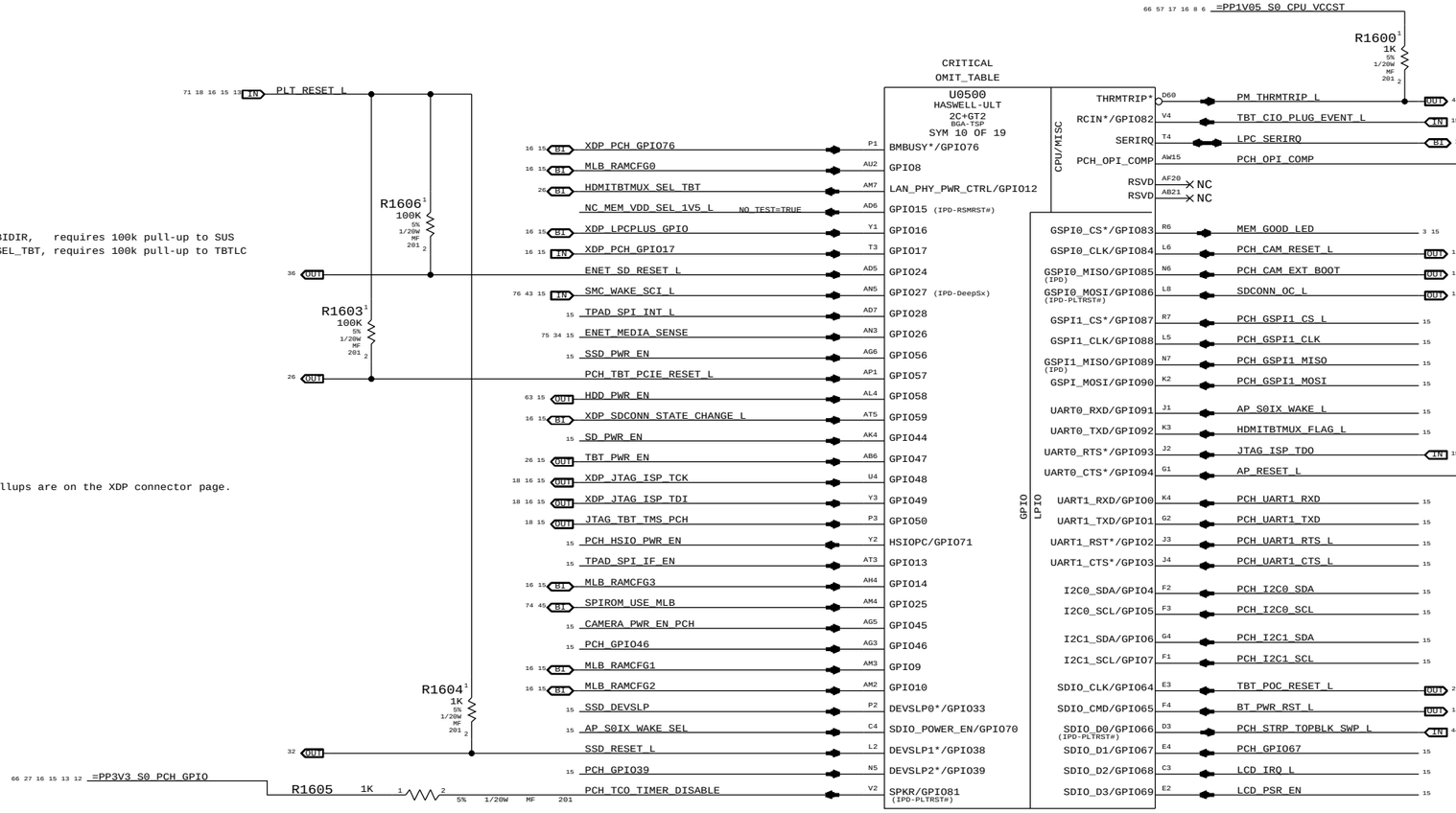
=PP3V3_SUS_PCH_VCC_SPI 8 11 66

R1548	1K	SPI_IO<2>	14
R1549	1K	SPI_IO<3>	14

R1591 100K WOL_EN 14 35

5% 1/20W MF 201

SYNC_MASTER=J70_TONY	SYNC_DATE=10/15/2013
PAGE TITLE	PCH PCIe/USB/LPC/SPI/SMBus
Apple Inc.	DRAWING NUMBER 051-1407
	SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 15 OF 123
	SHEET 14 OF 81


CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 10 OF 19
CPU/MISC
GPIO LPIO
=PP1V05_S0_CPU_VCCST
R1600 1K 5% 1/20W MF 201
PLT_RESET_L
R1606 100K
R1603 100K
R1604 1K
R1605 1K
=PP3V3_S0_PCH_GPIO
THRMTRIP* PM_THRMTRIP_L
RCIN*/GPIO82 TBT_CIO_PLUG_EVENT_L
SERIRQ LPC_SERIRQ
PCH_OPI_COMP PCH_OPI_COMP
RSVD NC
RSVD NC
R1601 49.9 1% 1/20W MF 201
PLACE_NEAR=U0500.AW15:12.7mm
GSPI0_CS*/GPIO83 MEM_GOOD_LED
GSPI0_CLK/GPIO84 PCH_CAM_RESET_L
GSPI0_MISO/GPIO85 PCH_CAM_EXT_BOOT
GSPI0_MOSI/GPIO86 SDCONN_OC_L
GSPI1_CS*/GPIO87 PCH_GSPI1_CS_L
GSPI1_CLK/GPIO88 PCH_GSPI1_CLK
GSPI1_MISO/GPIO89 PCH_GSPI1_MISO
GSPI_MOSI/GPIO90 PCH_GSPI1_MOSI
UART0_RXD/GPIO91 AP_S0IX_WAKE_L
UART0_TXD/GPIO92 HDMITBTMUX_FLAG_L
UART0_RTS*/GPIO93 JTAG_ISP_TDO
UART0_CTS*/GPIO94 AP_RESET_L
R1602 100K
UART1_RXD/GPIO0 PCH_UART1_RXD
UART1_TXD/GPIO1 PCH_UART1_TXD
UART1_RST*/GPIO2 PCH_UART1_RTS_L
UART1_CTS*/GPIO3 PCH_UART1_CTS_L
I2C0_SDA/GPIO4 PCH_I2C0_SDA
I2C0_SCL/GPIO5 PCH_I2C0_SCL
I2C1_SDA/GPIO6 PCH_I2C1_SDA
I2C1_SCL/GPIO7 PCH_I2C1_SCL
SDIO_CLK/GPIO64 TBT_POC_RESET_L
SDIO_CMD/GPIO65 BT_PWR_RST_L
SDIO_D0/GPIO66 PCH_STRP_TOPBLK_SWP_L
SDIO_D1/GPIO67 PCH_GPIO67
SDIO_D2/GPIO68 LCD_IRQ_L
SDIO_D3/GPIO69 LCD_PSR_EN
BMBUSY*/GPIO76 XDP_PCH_GPIO76
GPIO8 MLB_RAMCFG0
LAN_PHY_PWR_CTRL/GPIO12 HDMITBTMUX_SEL_TBT
GPIO15 (IPD-RSMRST#) NC_MEM_VDD_SEL_1V5_L
GPIO16 XDP_LPCPLUS_GPIO
GPIO17 XDP_PCH_GPIO17
GPIO24 ENET_SD_RESET_L
GPIO27 (IPD-DeepSx) SMC_WAKE_SCI_L
GPIO28 TPAD_SPI_INT_L
GPIO26 ENET_MEDIA_SENSE
GPIO56 SSD_PWR_EN
GPIO57 PCH_TBT_PCIE_RESET_L
GPIO58 HDD_PWR_EN
GPIO59 XDP_SDCONN_STATE_CHANGE_L
GPIO44 SD_PWR_EN
GPIO47 TBT_PWR_EN
GPIO48 XDP_JTAG_ISP_TCK
GPIO49 XDP_JTAG_ISP_TDI
GPIO50 JTAG_TBT_TMS_PCH
HSIOPC/GPIO71 PCH_HSIO_PWR_EN
GPIO13 TPAD_SPI_IF_EN
GPIO14 MLB_RAMCFG3
GPIO25 SPIROM_USE_MLB
GPIO45 CAMERA_PWR_EN_PCH
GPIO46 PCH_GPIO46
GPIO9 MLB_RAMCFG1
GPIO10 MLB_RAMCFG2
DEVSLP0*/GPIO33 SSD_DEVSLP
SDIO_POWER_EN/GPIO70 AP_S0IX_WAKE_SEL
DEVSLP1*/GPIO38 SSD_RESET_L
DEVSLP2*/GPIO39 PCH_GPIO39
SPKR/GPIO81 (IPD-PLTRST#) PCH_TCO_TIMER_DISABLE
Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).
Pull-up on TBT page
Requires connection to SMC via 1K series R
GPIO12:
CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC
Required JTAG pullups are on the XDP connector page.
=PP3V3_S5_PCH_GPIO
=PP3V3_S4_PCH_GPIO
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_CAMPWREN
R1628 100K CAMERA_PWR_EN_PCH
R1624 100K JTAG_TBT_TMS_PCH
R1634 100K JTAG_ISP_TDO
R1609 100K TBT_CIO_PLUG_EVENT_L
R1610 100K XDP_PCH_GPIO76
R1611 100K XDP_LPCPLUS_GPIO
R1617 100K SSD_PWR_EN
R1618 100K HDD_PWR_EN
R1621 100K TBT_PWR_EN
R1625 100K PCH_HSIO_PWR_EN
R1629 100K PCH_GPIO46
R1632 100K PCH_GPIO39
R1633 10K LPC_SERIRQ
R1635 100K BT_PWR_RST_L
R1637 100K LCD_IRQ_L
R1615 100K TPAD_SPI_INT_L
R1619 100K XDP_SDCONN_STATE_CHANGE_L
R1620 100K SD_PWR_EN
R1614 100K SMC_WAKE_SCI_L
R1616 100K PCH_GPIO67
R1612 100K XDP_PCH_GPIO17
R1622 100K XDP_JTAG_ISP_TCK
R1623 100K XDP_JTAG_ISP_TDI
R1626 100K TPAD_SPI_IF_EN
R1630 100K SSD_DEVSLP
R1631 100K AP_S0IX_WAKE_SEL
R1636 100K ENET_MEDIA_SENSE
R1638 100K LCD_PSR_EN
TBTLC for CR, S0 for RR
RAM Configuration Straps
For chip-down RAM systems
=PP3V3_S0_PCH_GPIO
RAMCFG3:H R1680 100K
RAMCFG2:H R1681 100K
RAMCFG1:H R1682 100K
RAMCFG0:H R1683 100K
MLB_RAMCFG0
MLB_RAMCFG1
MLB_RAMCFG2
MLB_RAMCFG3
RAMCFG3:L R1684 10K
RAMCFG2:L R1685 10K
RAMCFG1:L R1686 10K
RAMCFG0:L R1687 10K
=PP3V3_S0_PCH_GPIO
PCH_GSPI1_CS_L R1654 47K
PCH_GSPI1_MOSI R1653 100K
SDCONN_OC_L R1657 200K
AP_S0IX_WAKE_L R1658 100K
HDMITBTMUX_FLAG_L R1659 100K
PCH_UART1_RXD R1660 100K
PCH_UART1_TXD R1661 100K
PCH_UART1_RTS_L R1662 100K
PCH_UART1_CTS_L R1663 100K
PCH_I2C0_SDA R1664 100K
PCH_I2C0_SCL R1665 100K
PCH_I2C1_SDA R1666 100K
PCH_I2C1_SCL R1667 100K
MEM_GOOD_LED R1650 100K
PCH_GSPI1_CLK R1651 47K
PCH_GSPI1_MISO R1652 47K
PCH_CAM_RESET_L NOSTUFF R1668 100K
PCH_CAM_EXT_BOOT NOSTUFF R1669 100K
SYNC_MASTER=J70_DINI
SYNC_DATE=01/21/2014
PAGE TITLE
PCH GPIO/MISC/LPIO
Apple Inc.
DRAWING NUMBER 051-1407
SIZE D
REVISION A.0.0
BRANCH
PAGE 16 OF 123
SHEET 15 OF 81
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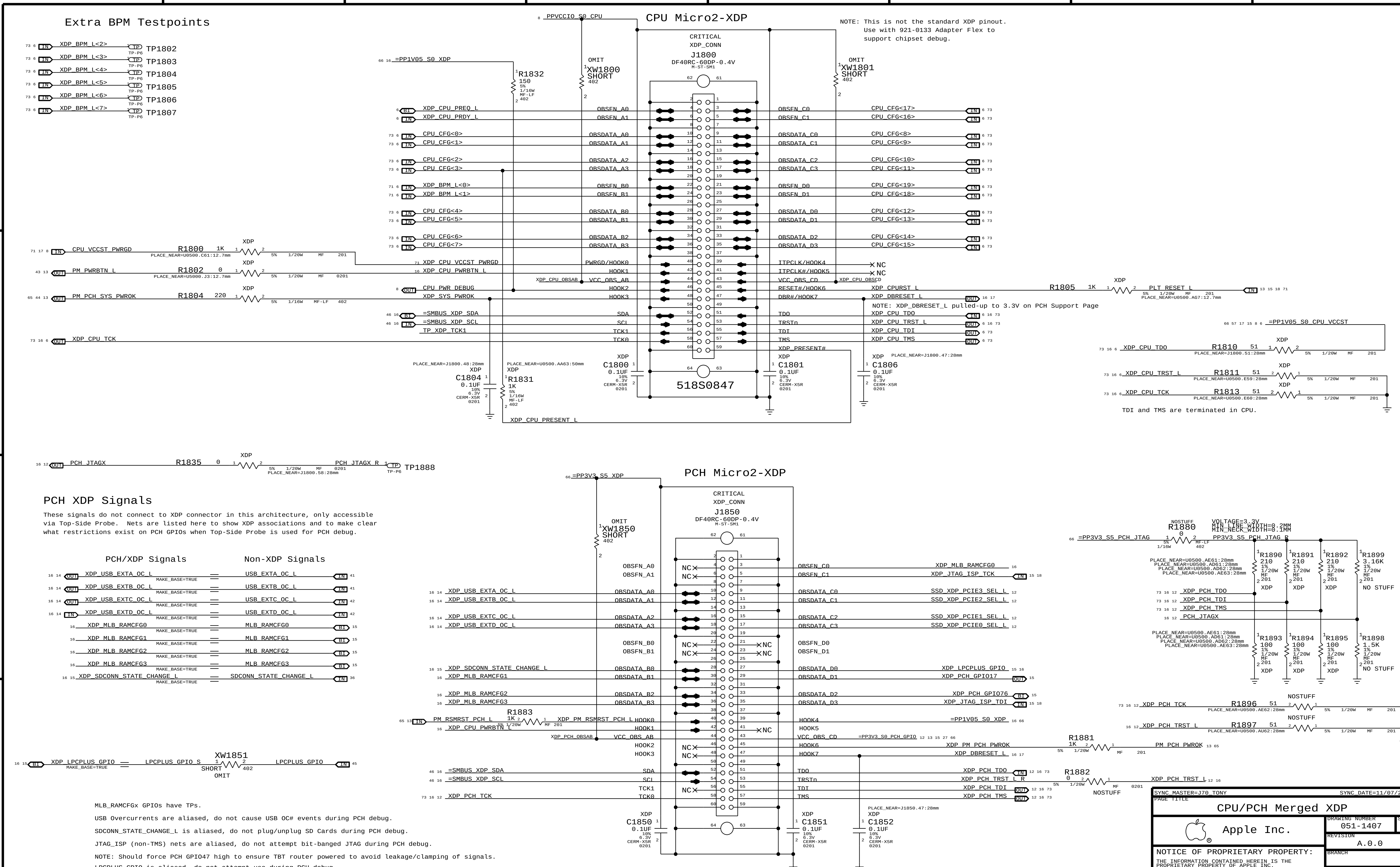

Extra BPM Testpoints
XDP_BPM_L<2> TP1802
XDP_BPM_L<3> TP1803
XDP_BPM_L<4> TP1804
XDP_BPM_L<5> TP1805
XDP_BPM_L<6> TP1806
XDP_BPM_L<7> TP1807
CPU Micro2-XDP
NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.
PPVCCIO_S0_CPU
=PP1V05_S0_XDP
R1832 150 5% 1/16W MF-LF 402
OMIT XW1800 SHORT 402
OMIT XW1801 SHORT 402
CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
XDP_BPM_L<0>
XDP_BPM_L<1>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
OBSFN_A0
OBSFN_A1
OBSDATA_A0
OBSDATA_A1
OBSDATA_A2
OBSDATA_A3
OBSFN_B0
OBSFN_B1
OBSDATA_B0
OBSDATA_B1
OBSDATA_B2
OBSDATA_B3
PWRGD/HOOK0
HOOK1
VCC_OBS_AB
HOOK2
HOOK3
SDA
SCL
TCK1
TCK0
OBSFN_C0
OBSFN_C1
OBSDATA_C0
OBSDATA_C1
OBSDATA_C2
OBSDATA_C3
OBSFN_D0
OBSFN_D1
OBSDATA_D0
OBSDATA_D1
OBSDATA_D2
OBSDATA_D3
ITPCLK/HOOK4
ITPCLK#/HOOK5
VCC_OBS_CD
RESET#/HOOK6
DBR#/HOOK7
TDO
TRSTn
TDI
TMS
XDP_PRESENT#
CPU_CFG<17>
CPU_CFG<16>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<19>
CPU_CFG<18>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
NC
CPU_VCCST_PWRGD R1800 1K XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.C61:12.7mm
PM_PWRBTN_L R1802 0 XDP 5% 1/20W MF 0201 PLACE_NEAR=U5000.J3:12.7mm
PM_PCH_SYS_PWROK R1804 220 XDP 5% 1/16W MF-LF 402
XDP_CPU_VCCST_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_OBSAB
XDP_CPU_OBSCD
CPU_PWR_DEBUG
XDP_SYS_PWROK
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
TP_XDP_TCK1
XDP_CPU_TCK
XDP_CPURST_L
R1805 1K XDP PLT_RESET_L 5% 1/20W MF 201 PLACE_NEAR=U0500.AG7:12.7mm
XDP_DBRESET_L
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page
XDP_CPU_TDO
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS
=PP1V05_S0_CPU_VCCST
XDP_CPU_TDO R1810 51 XDP 5% 1/20W MF 201 PLACE_NEAR=J1800.51:28mm
XDP_CPU_TRST_L R1811 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.E59:28mm
XDP_CPU_TCK R1813 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.E60:28mm
TDI and TMS are terminated in CPU.
PLACE_NEAR=J1800.48:28mm XDP C1804 0.1UF 10% 6.3V CERM-X5R 0201
PLACE_NEAR=U0500.AA63:50mm XDP R1831 1K 5% 1/16W MF-LF 402
XDP C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
XDP C1806 0.1UF 10% 6.3V CERM-X5R 0201 PLACE_NEAR=J1800.47:28mm
XDP_CPU_PRESENT_L
PCH_JTAGX R1835 0 XDP 5% 1/20W MF 0201 PCH_JTAGX_R TP1888 PLACE_NEAR=J1800.58:28mm
PCH XDP Signals
These signals do not connect to XDP connector in this architecture, only accessible
via Top-Side Probe. Nets are listed here to show XDP associations and to make clear
what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.
PCH/XDP Signals
Non-XDP Signals
XDP_USB_EXTA_OC_L = USB_EXTA_OC_L
XDP_USB_EXTB_OC_L = USB_EXTB_OC_L
XDP_USB_EXTC_OC_L = USB_EXTC_OC_L
XDP_USB_EXTD_OC_L = USB_EXTD_OC_L
XDP_MLB_RAMCFG0 = MLB_RAMCFG0
XDP_MLB_RAMCFG1 = MLB_RAMCFG1
XDP_MLB_RAMCFG2 = MLB_RAMCFG2
XDP_MLB_RAMCFG3 = MLB_RAMCFG3
XDP_SDCONN_STATE_CHANGE_L = SDCONN_STATE_CHANGE_L
MAKE_BASE=TRUE
XDP_LPCPLUS_GPIO = LPCPLUS_GPIO_S XW1851 SHORT OMIT 402 LPCPLUS_GPIO
PCH Micro2-XDP
=PP3V3_S5_XDP
OMIT XW1850 SHORT 402
CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM1
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3
PM_RSMRST_PCH_L R1883 1K 1/20W MF 201 XDP_PM_RSMRST_PCH_L
XDP_CPU_PWRBTN_L
XDP_PCH_OBSAB
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_PCH_TCK
XDP_MLB_RAMCFG0
XDP_JTAG_ISP_TCK
SSD_XDP_PCIE3_SEL_L
SSD_XDP_PCIE2_SEL_L
SSD_XDP_PCIE1_SEL_L
SSD_XDP_PCIE0_SEL_L
XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17
XDP_PCH_GPIO76
XDP_JTAG_ISP_TDI
=PP1V05_S0_XDP
=PP3V3_S0_PCH_GPIO
XDP_PM_PCH_PWROK
XDP_DBRESET_L
XDP_PCH_TDO
XDP_PCH_TRST_L_R
XDP_PCH_TDI
XDP_PCH_TMS
R1881 1K 5% 1/20W MF 201 PM_PCH_PWROK
R1882 0 5% 1/20W MF 0201 NOSTUFF XDP_PCH_TRST_L
XDP C1850 0.1UF 10% 6.3V CERM-X5R 0201
XDP C1851 0.1UF 10% 6.3V CERM-X5R 0201
PLACE_NEAR=J1850.47:28mm XDP C1852 0.1UF 10% 6.3V CERM-X5R 0201
=PP3V3_S5_PCH_JTAG NOSTUFF R1880 0 5% 1/16W MF-LF 402 PP3V3_S5_PCH_JTAG_R
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
R1890 210 1% 1/20W MF 201 XDP
R1891 210 1% 1/20W MF 201 XDP
R1892 210 1% 1/20W MF 201 XDP
R1899 3.16K 1% 1/20W MF 201 NO STUFF
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
PCH_JTAGX
R1893 100 1% 1/20W MF 201 XDP
R1894 100 1% 1/20W MF 201 XDP
R1895 100 1% 1/20W MF 201 XDP
R1898 1.5K 1% 1/20W MF 201 NO STUFF
XDP_PCH_TCK R1896 51 NOSTUFF 5% 1/20W MF 201 PLACE_NEAR=U0500.AE62:28mm
XDP_PCH_TRST_L R1897 51 NOSTUFF 5% 1/20W MF 201 PLACE_NEAR=U0500.AU62:28mm

MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

SYNC_MASTER=J70_TONY SYNC_DATE=11/07/2013

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

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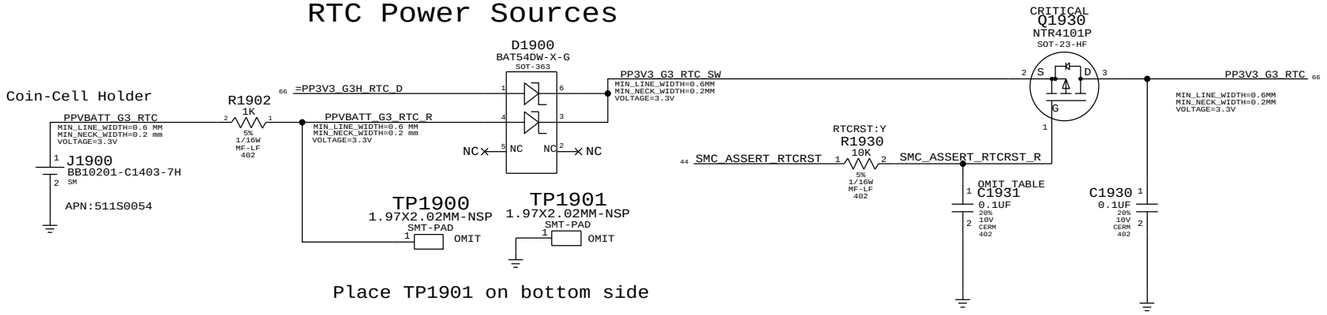
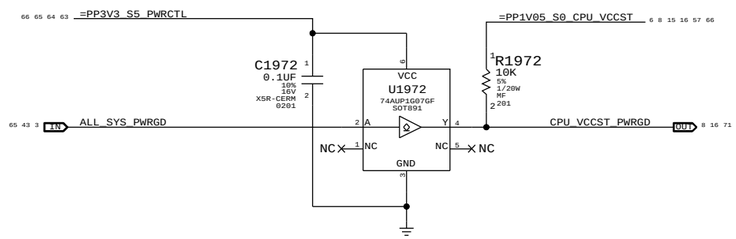
RTC Power Sources



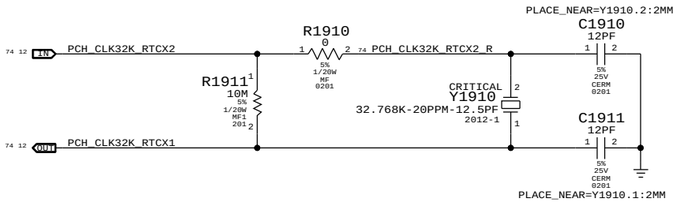
Place TP1901 on bottom side

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1059	1	CAP,0.1 UF,402	C1931	RTCRST:Y
116S0090	1	RES,10K OHM,402	C1931	RTCRST:N

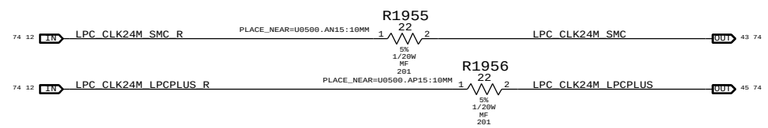
ALL_SYS_PWRGD/CPU_VCCST_PWRGD Level-Shifter



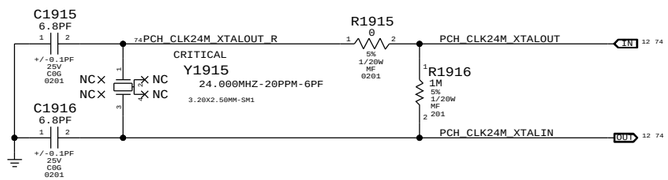
PCH RTC Crystal



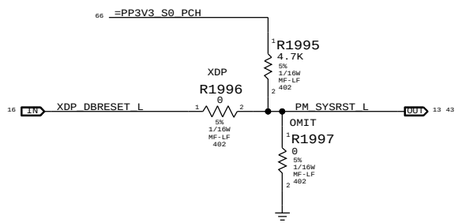
Clock series termination



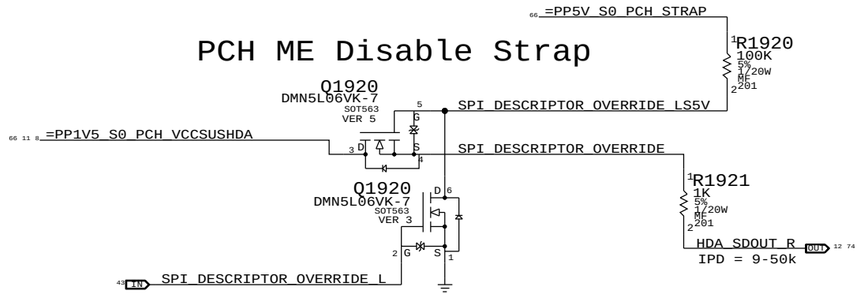
PCH 24MHz Crystal



PCH Reset Button



PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

SYNC_MASTER=J70_NICK SYNC_DATE=02/25/2014

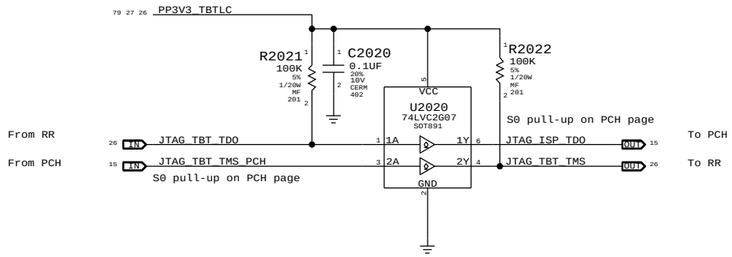
PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 19 OF 123
SHEET: 17 OF 81

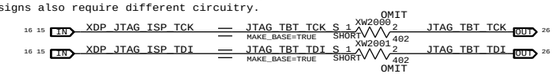
Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

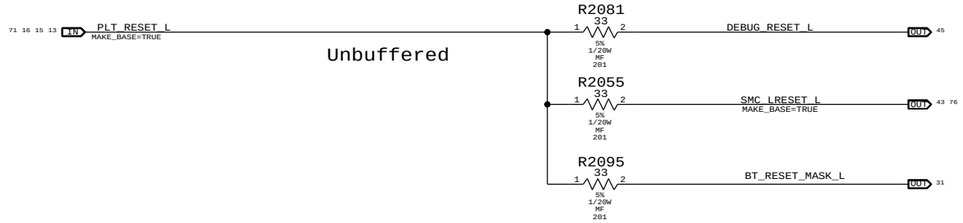


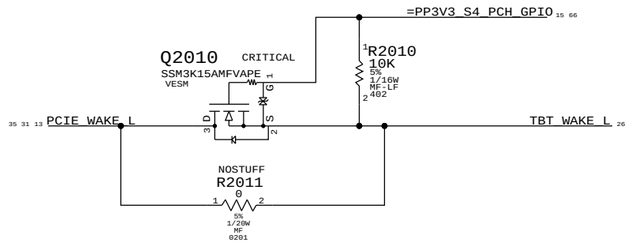
NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.



Platform Reset Connections





SYNC_MASTER=J70_NICK SYNC_DATE=11/20/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 20 OF 123
SHEET: 18 OF 81

Memory Bit/Byte Swizzle

MAKE_BASE

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MAKE_BASE

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

DDR3 Signal Aliases

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

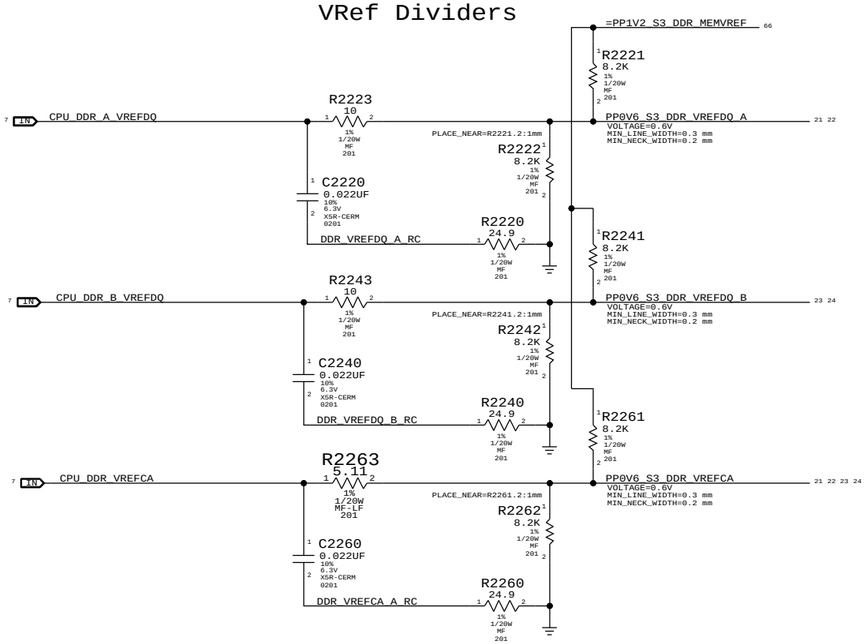
REVISION A.0.0

BRANCH

PAGE 21 OF 123

SHEET 19 OF 81

VRef Dividers



SYNC_MASTER=J70_GAREN SYNC_DATE=10/24/2013

PAGE TITLE

DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

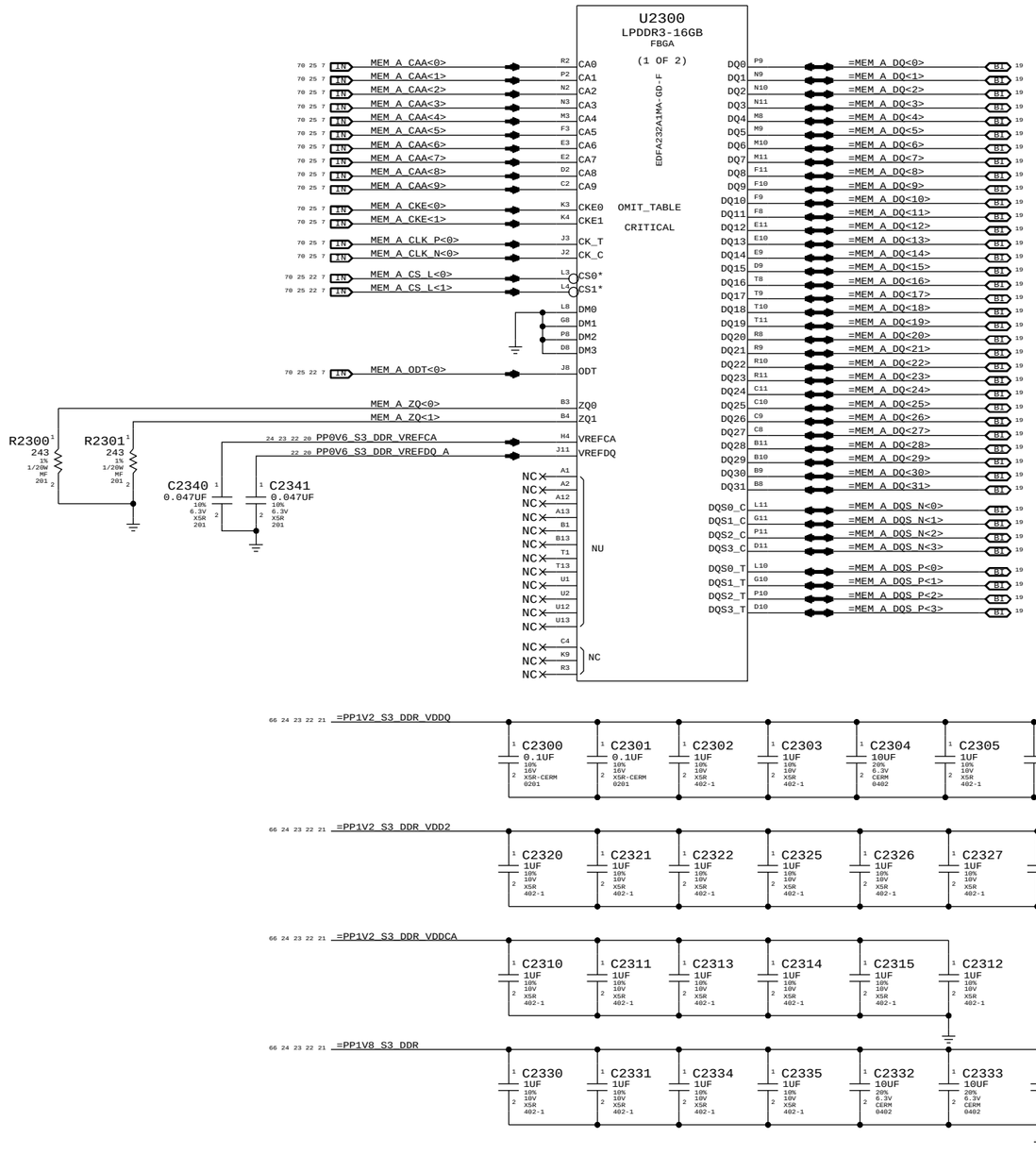
REVISION A.0.0

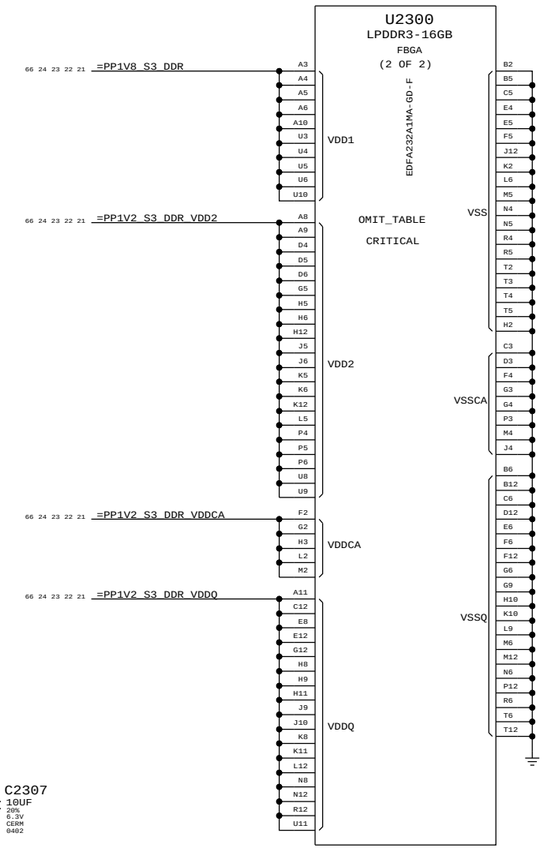
BRANCH

PAGE 22 OF 123

SHEET 20 OF 81

LPDDR3 CHANNEL A (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

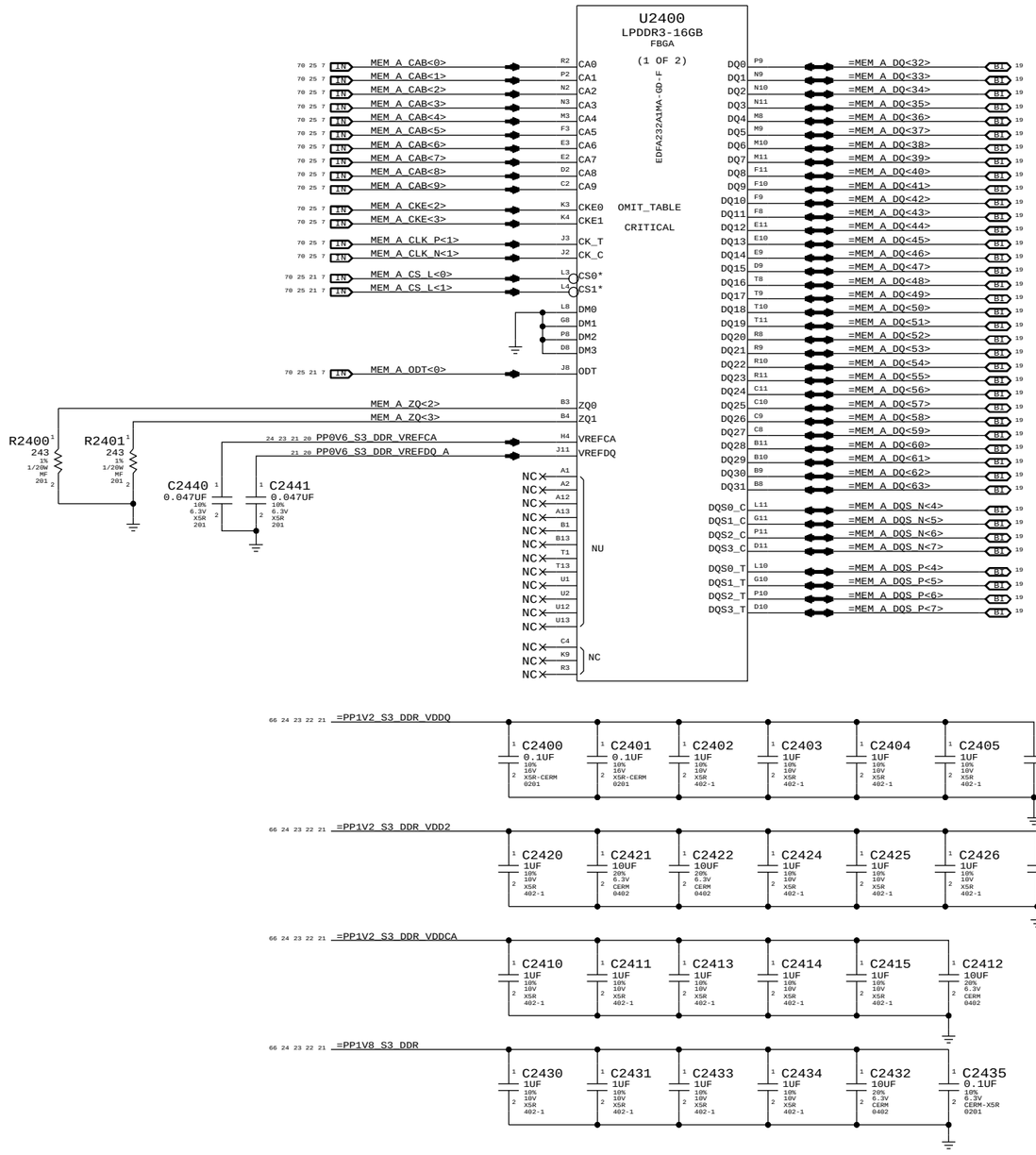
SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

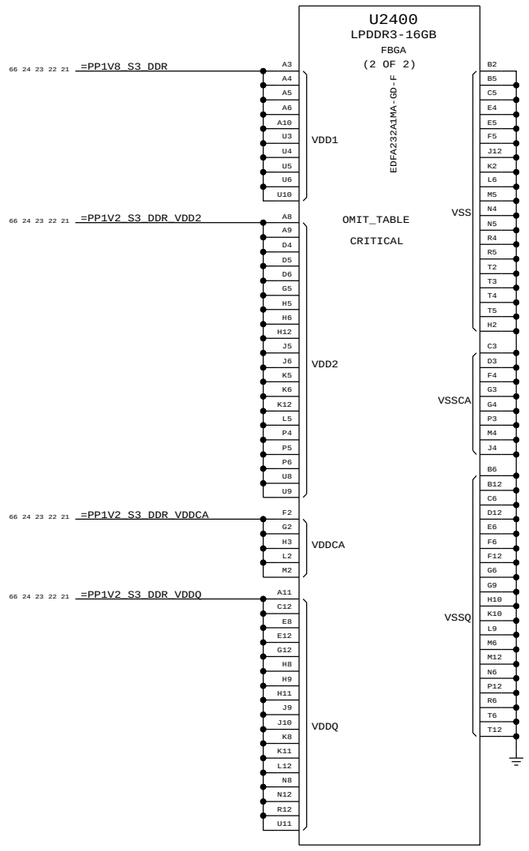
PAGE TITLE: LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 23 OF 123
SHEET: 21 OF 81

LPDDR3 CHANNEL A (32-63)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

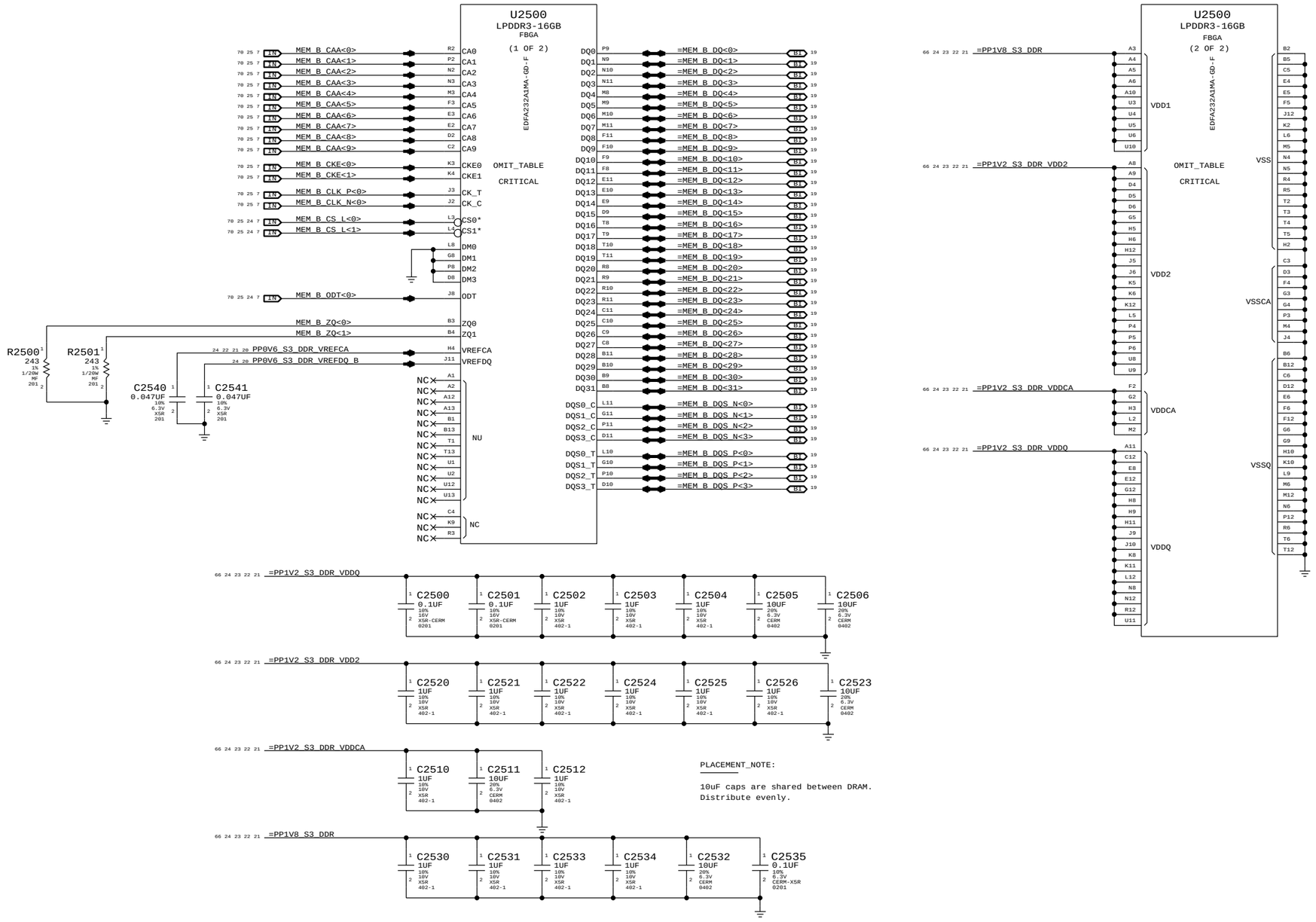
SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 24 OF 123
SHEET 22 OF 81

LPDDR3 CHANNEL B (0-31)



SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

LPDDR3 DRAM Channel B (0-31)

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

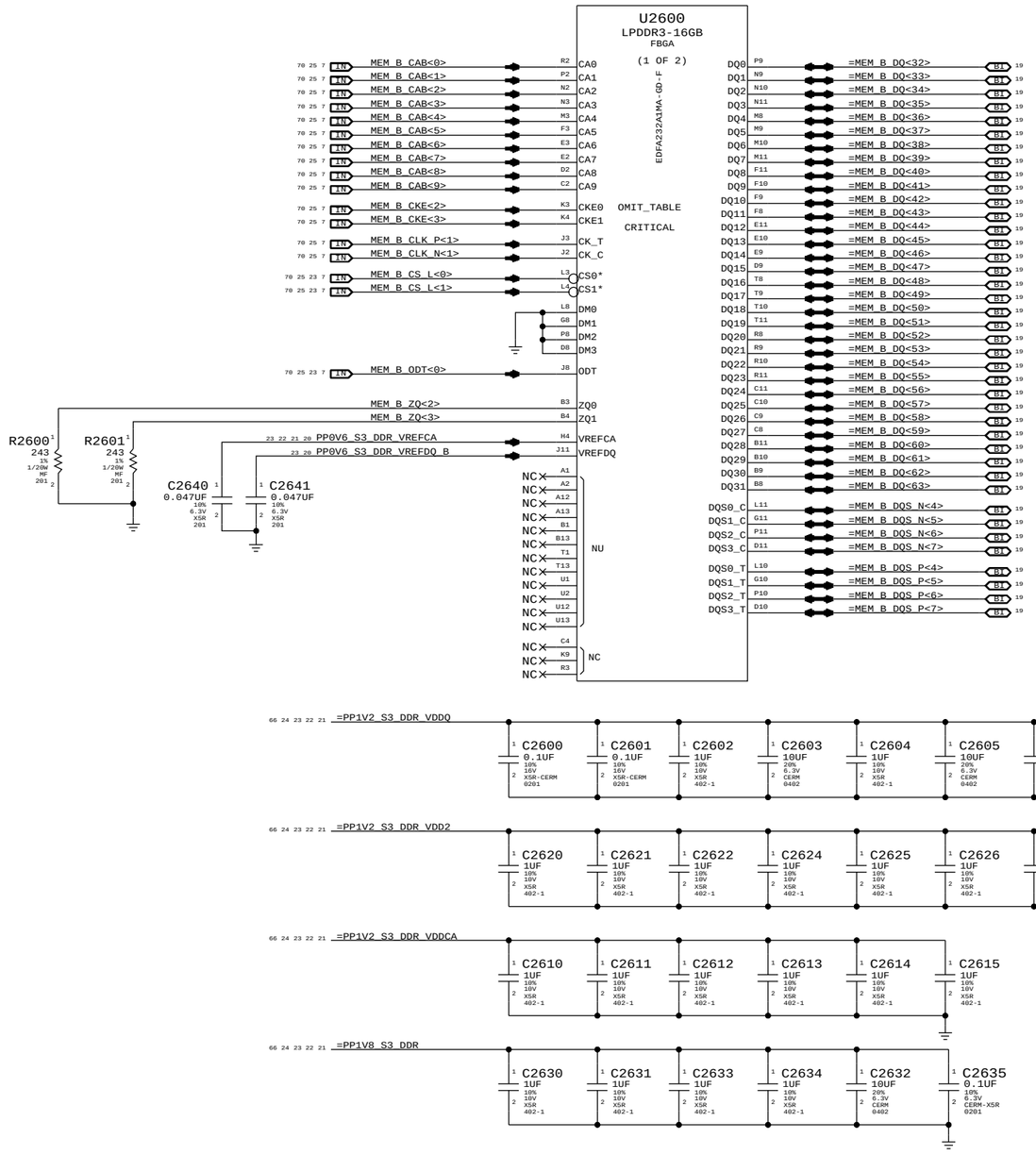
REVISION A.0.0

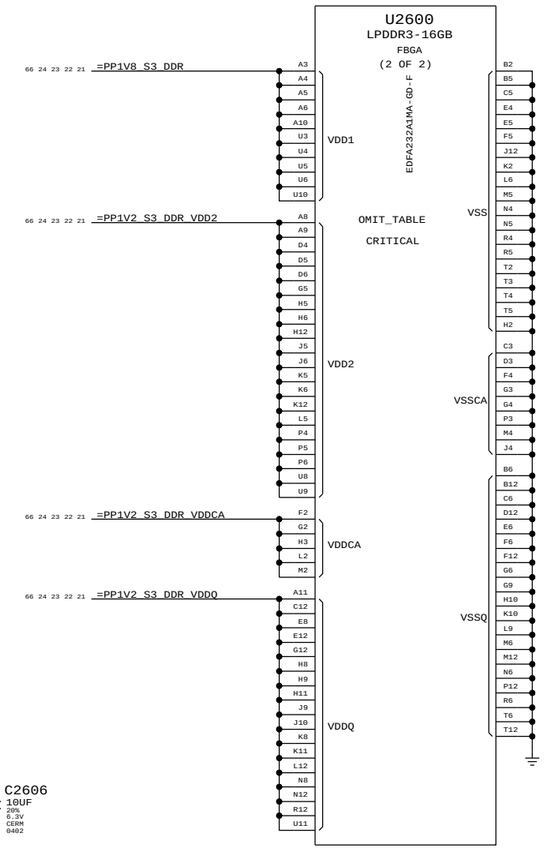
BRANCH

PAGE 25 OF 123

SHEET 23 OF 81

LPDDR3 CHANNEL B (32-63)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER 051-1407
SIZE D
REVISION A.0.0
BRANCH
PAGE 26 OF 123
SHEET 24 OF 81

Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

66 =PP0V6_S3_DDRVTT_A

70 21 7	MEM_A_CAA<9>	RP2701	56	4	5	5% 1/32W	4X0201-HF	
70 21 7	MEM_A_CAA<8>	RP2701	56	3	6	5% 1/32W	4X0201-HF	
70 21 7	MEM_A_CAA<6>	RP2701	56	2	7	5% 1/32W	4X0201-HF	
70 21 7	MEM_A_CAA<7>	RP2701	56	1	8	5% 1/32W	4X0201-HF	
70 21 7	MEM_A_CAA<5>	R2700	56	1	2	5% 1/32W	4X0201-HF	
70 21 7	MEM_A_CLK_P<0>	R2701	39	1	2	5% 1/20W	201 MF	
70 21 7	MEM_A_CLK_N<0>	R2702	39	1	2	5% 1/20W	201 MF	
70 21 7	MEM_A_CKE<1>	R2703	82	1	2	5% 1/20W	201 MF	
70 21 7	MEM_A_CKE<0>	R2704	82	1	2	5% 1/20W	201 MF	
70 21 7	MEM_A_CAA<4>	R2705	56	1	2	5% 1/20W	201 MF	
70 21 7	MEM_A_CAA<3>	R2706	56	1	2	5% 1/20W	201 MF	
70 21 7	MEM_A_CAA<2>	RP2703	56	4	5	5% 1/32W	4X0201-HF	
70 21 7	MEM_A_CAA<1>	RP2703	56	3	6	5% 1/32W	4X0201-HF	
70 21 7	MEM_A_CAA<0>	RP2703	56	2	7	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CAB<9>	R2725	56	1	2	5% 1/20W	201 MF	
70 22 7	MEM_A_CAB<8>	RP2707	56	4	5	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CAB<6>	RP2707	56	3	6	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CAB<7>	RP2707	56	2	7	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CAB<5>	RP2707	56	1	8	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CLK_P<1>	R2707	39	1	2	5% 1/20W	201 MF	
70 22 7	MEM_A_CLK_N<1>	R2708	39	1	2	5% 1/20W	201 MF	
70 22 7	MEM_A_CKE<2>	R2709	82	1	2	5% 1/20W	201 MF	
70 22 7	MEM_A_CKE<3>	R2720	82	1	2	5% 1/20W	201 MF	
70 22 7	MEM_A_CAB<4>	R2721	56	1	2	5% 1/20W	201 MF	
70 22 7	MEM_A_CAB<2>	RP2704	56	4	5	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CAB<3>	RP2704	56	3	6	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CAB<1>	RP2704	56	2	7	5% 1/32W	4X0201-HF	
70 22 7	MEM_A_CAB<0>	RP2704	56	1	8	5% 1/32W	4X0201-HF	
70 22 21 7	MEM_A_CS_L<0>	R2722	82	1	2	5% 1/20W	201 MF	
70 22 21 7	MEM_A_CS_L<1>	R2723	82	1	2	5% 1/20W	201 MF	
70 22 21 7	MEM_A_ODT<0>	R2724	82	1	2	5% 1/20W	201 MF	

C2700 0.47UF 20% 4V CERM-X5R-1 201
C2701 0.47UF 20% 4V CERM-X5R-1 201
C2702 0.47UF 20% 4V CERM-X5R-1 201
C2703 0.47UF 20% 4V CERM-X5R-1 201
C2704 0.47UF 20% 4V CERM-X5R-1 201
C2705 0.47UF 20% 4V CERM-X5R-1 201
C2706 0.47UF 20% 4V CERM-X5R-1 201
C2707 0.47UF 20% 4V CERM-X5R-1 201
C2708 0.47UF 20% 4V CERM-X5R-1 201
C2709 0.47UF 20% 4V CERM-X5R-1 201

CRITICAL
C2720 22UF 20% 6.3V X5R-CERM-1 603

PLACE_NEAR=RP2701.5:4mm

Spare
RP2703
56
NC 1 8 NC
5% 1/32W 4X0201-HF

66 =PP0V6_S3_DDRVTT_B

70 23 7	MEM_B_CAA<9>	RP2712	56	4	5	5% 1/32W	4X0201-HF	
70 23 7	MEM_B_CAA<8>	RP2712	56	3	6	5% 1/32W	4X0201-HF	
70 23 7	MEM_B_CAA<7>	RP2712	56	2	7	5% 1/32W	4X0201-HF	
70 23 7	MEM_B_CAA<6>	RP2712	56	1	8	5% 1/32W	4X0201-HF	
70 23 7	MEM_B_CAA<5>	R2710	56	1	2	5% 1/32W	4X0201-HF	
70 23 7	MEM_B_CLK_P<0>	R2711	39	1	2	5% 1/20W	201 MF	
70 23 7	MEM_B_CLK_N<0>	R2712	39	1	2	5% 1/20W	201 MF	
70 23 7	MEM_B_CKE<1>	R2713	82	1	2	5% 1/20W	201 MF	
70 23 7	MEM_B_CKE<0>	R2714	82	1	2	5% 1/20W	201 MF	
70 23 7	MEM_B_CAA<4>	R2715	56	1	2	5% 1/20W	201 MF	
70 23 7	MEM_B_CAA<2>	R2716	56	1	2	5% 1/20W	201 MF	
70 23 7	MEM_B_CAA<3>	RP2713	56	4	5	5% 1/32W	4X0201-HF	
70 23 7	MEM_B_CAA<1>	RP2713	56	3	6	5% 1/32W	4X0201-HF	
70 23 7	MEM_B_CAA<0>	RP2713	56	2	7	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CAB<9>	R2735	56	1	2	5% 1/20W	201 MF	
70 24 7	MEM_B_CAB<8>	RP2717	56	4	5	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CAB<7>	RP2717	56	3	6	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CAB<6>	RP2717	56	2	7	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CAB<5>	RP2717	56	1	8	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CLK_N<1>	R2717	39	1	2	5% 1/20W	201 MF	
70 24 7	MEM_B_CLK_P<1>	R2718	39	1	2	5% 1/20W	201 MF	
70 24 7	MEM_B_CKE<2>	R2719	82	1	2	5% 1/20W	201 MF	
70 24 7	MEM_B_CKE<3>	R2730	82	1	2	5% 1/20W	201 MF	
70 24 7	MEM_B_CAB<4>	R2731	56	1	2	5% 1/20W	201 MF	
70 24 7	MEM_B_CAB<2>	RP2714	56	4	5	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CAB<3>	RP2714	56	3	6	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CAB<1>	RP2714	56	2	7	5% 1/32W	4X0201-HF	
70 24 7	MEM_B_CAB<0>	RP2714	56	1	8	5% 1/32W	4X0201-HF	
70 24 23 7	MEM_B_CS_L<0>	R2732	82	1	2	5% 1/20W	201 MF	
70 24 23 7	MEM_B_CS_L<1>	R2733	82	1	2	5% 1/20W	201 MF	
70 24 23 7	MEM_B_ODT<0>	R2734	82	1	2	5% 1/20W	201 MF	

C2710 0.47UF 20% 4V CERM-X5R-1 201
C2711 0.47UF 20% 4V CERM-X5R-1 201
C2712 0.47UF 20% 4V CERM-X5R-1 201
C2713 0.47UF 20% 4V CERM-X5R-1 201
C2714 0.47UF 20% 4V CERM-X5R-1 201
C2715 0.47UF 20% 4V CERM-X5R-1 201
C2716 0.47UF 20% 4V CERM-X5R-1 201
C2717 0.47UF 20% 4V CERM-X5R-1 201
C2718 0.47UF 20% 4V CERM-X5R-1 201
C2719 0.47UF 20% 4V CERM-X5R-1 201

CRITICAL
C2740 22UF 20% 6.3V X5R-CERM-1 603

PLACE_NEAR=RP2714.8:4.5mm

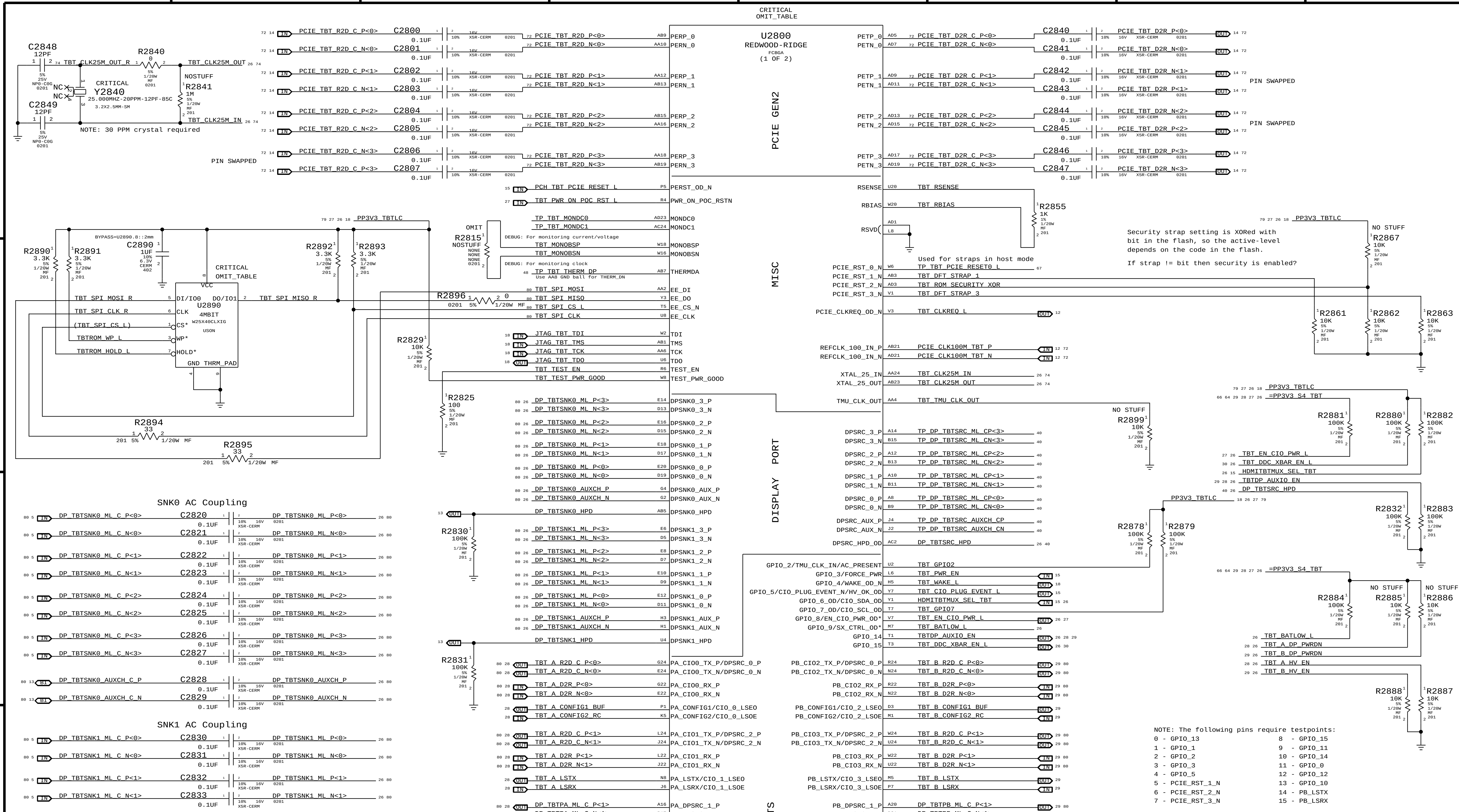
Spare
RP2713
56
NC 1 8 NC
5% 1/32W 4X0201-HF

SYNC MASTER=J41_MLB SYNC DATE=09/03/2013

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 27 OF 123
SHEET 25 OF 81



CRITICAL
OMIT_TABLE
U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)
PCIE GEN2
MISC
DISPLAY PORT
PORTS
C2848
12PF
R2840
TBT_CLK25M_OUT_R
TBT_CLK25M_OUT
NOSTUFF
R2841
1M
CRITICAL
Y2840
25.000MHZ-20PPM-12PF-85C
3.2X2.5MM-SM
C2849
12PF
TBT_CLK25M_IN
NOTE: 30 PPM crystal required
PIN SWAPPED
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
C2800
C2801
C2802
C2803
C2804
C2805
C2806
C2807
0.1UF
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
C2840
C2841
C2842
C2843
C2844
C2845
C2846
C2847
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCH_TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
PERST_OD_N
PWR_ON_POC_RSTN
TBT_RSENSE
TBT_RBIAS
R2855
1K
PP3V3_TBTLC
OMIT
R2815
NOSTUFF
TP_TBT_MONDC0
TP_TBT_MONDC1
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TP_TBT_THERM_DP
Use AA8 GND ball for THERM_DN
THERMDA
BYPASS=U2890.8::2mm
R2890
R2891
C2890
1UF
R2892
R2893
3.3K
CRITICAL
OMIT_TABLE
U2890
4MBIT
W25X40CLXIG
USON
TBT_SPI_MOSI_R
TBT_SPI_CLK_R
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
TBT_SPI_MISO_R
R2896
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
R2829
10K
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
R2825
100
R2894
33
R2895
33
Used for straps in host mode
TP_TBT_PCIE_RESET0_L
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
TBT_CLK25M_IN
TBT_CLK25M_OUT
TBT_TMU_CLK_OUT
Security strap setting is XORed with
bit in the flash, so the active-level
depends on the code in the flash.
If strap != bit then security is enabled?
NO STUFF
R2867
10K
R2861
R2862
R2863
=PP3V3_S4_TBT
R2881
R2880
R2882
100K
NO STUFF
R2899
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
R2832
R2883
R2878
R2879
R2884
NO STUFF
R2885
NO STUFF
R2886
TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R2888
R2887
SNK0 AC Coupling
SNK1 AC Coupling
C2820
C2821
C2822
C2823
C2824
C2825
C2826
C2827
C2828
C2829
C2830
C2831
C2832
C2833
C2834
C2835
C2836
C2837
C2838
C2839
R2830
100K
R2831
100K
TBT_GPIO2
TBT_PWR_EN
TBT_WAKE_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SYNC_MASTER=J70_NICK SYNC_DATE=01/27/2014

PAGE TITLE

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

BRANCH

PAGE 28 OF 123

SHEET 26 OF 81

U2950

Part	SLG5AP304V
Type	Load Switch
R(on) @ 1.05V	7.8 mOhm Typ 9.6 mOhm Max

Max Current = 4A (85C)

1.05V TBT "CIO" Switch

Internal switch not functional on RR.

66 64 29 28 27 26 =PP3V3_S4_TBT

C2940 1.0UF 20% 6.3V X5R 0201-1

27 PP1V05_TBT

U2940 SLG5AP304V TDFN CRITICAL

VDD, D, S, CAP, ON, GND

7 TBT_CIO_FET_CAP

2 TBT_EN_CIO_PWR

PP3V3_TBTLC 18 26 27 79

R2945 100K 5% 1/20W MF 201

C2941 0.0022UF 10% 50V CERM 402

Q2945 DMN5L06VK-7 SOT563 VER 3

66 27 16 15 13 12 =PP3V3_S0_PCH_GPIO

VER 5

13 OUT TBT_PWR_REQ_L

Pull-up (S0) on PCH page

TBT_EN_CIO_PWR_L IN 26

Q2945 DMN5L06VK-7 SOT563

CRITICAL

U2800 REDWOOD-RIDGE FCBGA (2 OF 2)

PP1V05_TBTRDV MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=1.05V

700 mA EDP

C2900 C2901 C2902 C2903 C2904 C2905 C2906 1.0UF 20% 6.3V X5R 0201-1

VCC1P0_RDV_DECAP

VCC1P0_CIO

PP1V05_TBTCIO MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V

1200 mA EDP

C2930 C2931 C2932 1.0UF 20% 6.3V X5R 0201-1

VCC

SVR input to RR - 1100 mA EDP

POC input to RR - 150 mA EDP

Isolated to reduce noise from SVR

VCC3P3

PP1V05_TBT MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=1.05V

C2910 C2911 1.0UF 20% 6.3V X5R 0201-1

SVR_VCC1P0

VCC3P3_LC

PP3V3_TBTLC MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.15 MM VOLTAGE=3.3V

100 mA EDP

C2970 1.0UF 20% 6.3V X5R 0201-1

=PP3V3_S4_TBT 26 27 28 29 64 66

3.1 W (Dual-Port)

2.4 W (Single-Port)

EDP: 1.25 A

PLACE_NEAR=C2952.1:3mm

C2950 C2951 C2952 C2953 10UF 20% 6.3V CERM-X5R 0402-1

XW2960 SM

CRITICAL L2920 680NH-30%-3.6A-35MOHM SM

1900 mA EDP

C2923 C2922 C2921 C2920 10UF 20% 6.3V CERM-X5R 0402-1

P1V05TBT_SW MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM DIDT=TRUE SWITCH_NODE=TRUE

SVR_IND0

NC

SVR_AMON

CRITICAL D2920 SOD-323 NSR1020MW2T1G

VCC3P3_RDV_DECAP

PP3V3_TBTRDV MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V

25 mA EDP

C2980 C2981 1.0UF 20% 6.3V X5R 0201-1

PP3V3_S4_TBT_F MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V

C2960 C2961 1.0UF 20% 6.3V X5R 0201-1

GND

VSS

A2, B1, and C2 are the ground current pins for A4, A6, and B3.
They should be routed as a shape to the annode of D2920.

TBT "POC" Power-up Reset

66 64 29 28 27 26 =PP3V3_S4_TBT

65 44 43 IN SMC_DELAYED_PWRGD

66 27 16 15 13 12 =PP3V3_S0_PCH_GPIO

R2995 100K 5% 1/20W MF 201

Q2995 DMN32D2LFB4 DFN1006H4-3

SYM_VER_3

15 IN TBT_POC_RESET_L

R2990 100K 5% 1/20W MF 201

R2992 100K 5% 1/20W MF 201

CRITICAL

U2990 TPS3895ADRY USON

VCC, ENABLE, SENSE, SENSE_OUT, CT, GND

TBTPOCRST_MR_L

TBTPOCRST_SENSE

TBTPOCRST_CT

C2990 0.1UF 10% 25V X5R 402

Push-pull output

TBT_PWR_ON_POC_RST_L OUT 26

C2995 330PF 10% 16V X7R 0201

R2991 24.9K 1% 1/20W MF 201

C2991 0.001UF 10% 50V X7R-CERM 0402

Vth = 2.508V nominal

Delay = 4.04ms nominal

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=J70_NICK SYNC_DATE=01/12/2014

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 29 OF 123

SHEET: 27 OF 81

3.3V/HV Power MUX

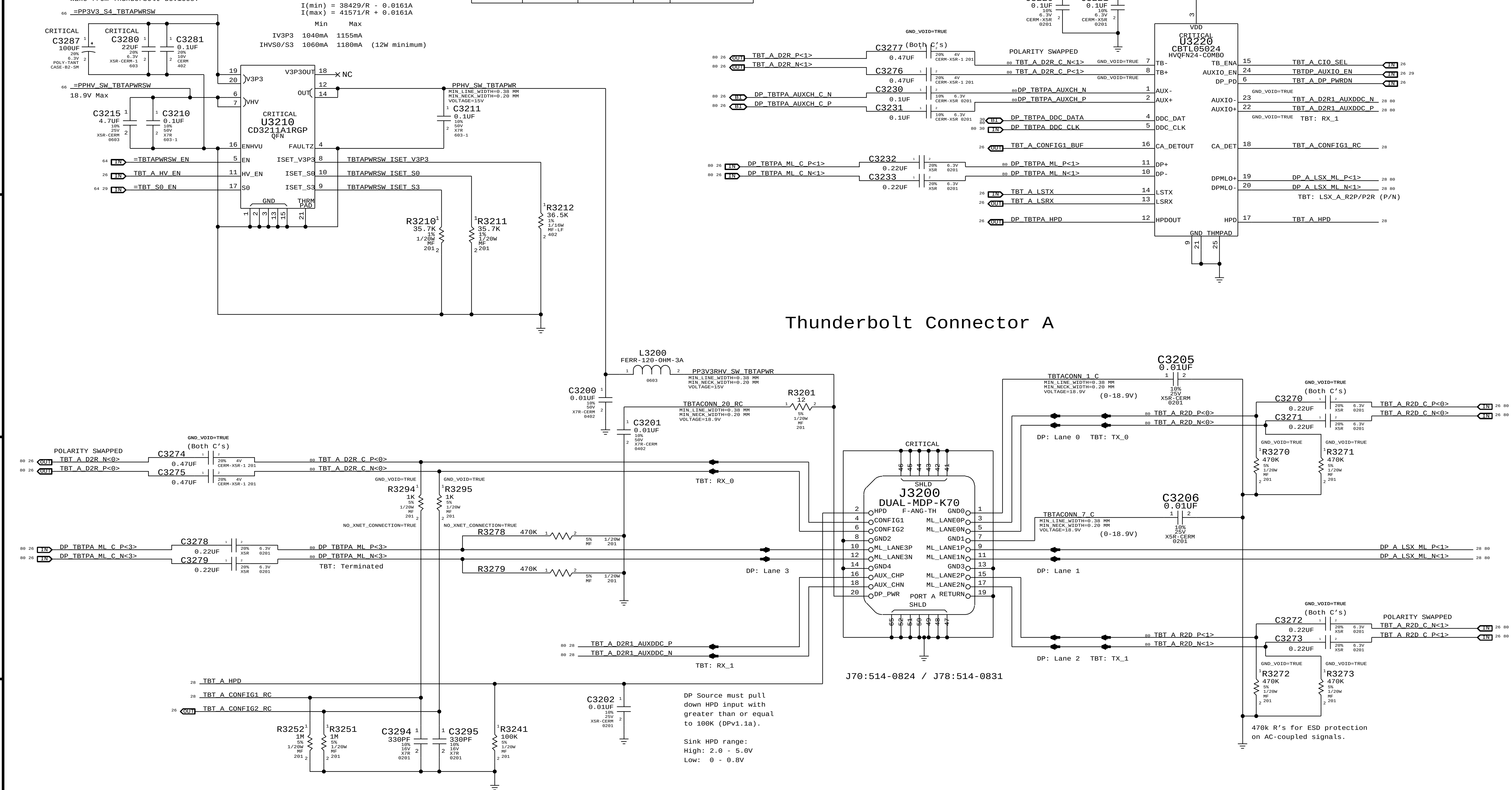
V3P3 must be S4 to support
wake from Thunderbolt devices.

For 12V systems:
I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A

	Min	Max	
IV3P3	1040mA	1155mA	
IHVS0/S3	1060mA	1180mA	(12W minimum)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0398	128S0220		ALL	3.3V INPUT CAP

Thunderbolt Connector A



=PP3V3_S4_TBTAPWRSW
=PPHV_SW_TBTAPWRSW
18.9V Max
CRITICAL
C3287 100UF
C3280 22UF
C3281 0.1UF
C3215 4.7UF
C3210 0.1UF
CRITICAL
U3210
CD3211A1RGP
QFN
V3P3
VHV
V3P3OUT
NC
OUT
ENHVU
EN
HV_EN
S0
ISET_V3P3
ISET_S0
ISET_S3
FAULTZ
GND
THRM PAD
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3211 0.1UF
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
R3210 35.7K
R3211 35.7K
R3212 36.5K
=PP3V3_S4_TBT
C3220 0.1UF
C3221 0.1UF
GND_VOID=TRUE
(Both C's)
POLARITY SWAPPED
C3277 0.47UF
C3276 0.47UF
C3230 0.1UF
C3231 0.1UF
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
VDD
CRITICAL
U3220
CBTL05024
HVQFN24-COMBO
TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
HPDOUT
TB_ENA
AUXIO_EN
DP_PD
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND THMPAD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
C3232 0.22UF
C3233 0.22UF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
L3200
FERR-120-OHM-3A
PP3V3RHV_SW_TBTAPWR
C3200 0.01UF
C3201 0.01UF
TBTACONN_20_RC
R3201 12
C3205 0.01UF
TBTACONN_1_C
(0-18.9V)
C3206 0.01UF
TBTACONN_7_C
CRITICAL
SHLD
J3200
DUAL-MDP-K70
F-ANG-TH
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
PORT A
SHLD
J70:514-0824 / J78:514-0831
C3274 0.47UF
C3275 0.47UF
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT: RX_0
R3294 1K
R3295 1K
NO_XNET_CONNECTION=TRUE
C3278 0.22UF
C3279 0.22UF
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Terminated
R3278 470K
R3279 470K
DP: Lane 3
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT: RX_1
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M
R3251 1M
C3294 330PF
C3295 330PF
R3241 100K
C3202 0.01UF
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
DP: Lane 0 TBT: TX_0
C3270 0.22UF
C3271 0.22UF
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R3270 470K
R3271 470K
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
DP: Lane 1
C3272 0.22UF
C3273 0.22UF
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
DP: Lane 2 TBT: TX_1
R3272 470K
R3273 470K
470k R's for ESD protection
on AC-coupled signals.

SYNC_MASTER=J70_NICK SYNC_DATE=10/16/2013

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

For 12V systems:

I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A

	Min	Max
IV3P3	1040mA	1155mA
IHVS0/S3	1060mA	1180mA (12W minimum)

66 =PP3V3_S4_TBTBPWRSW

CRITICAL C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM

CRITICAL C3380 22UF 20% 6.3V X5R-CERM-1 603

C3381 0.1UF 20% 10V CERM 402

66 =PPHV_SW_TBTBPWRSW
18.9V Max

C3315 4.7UF 10% 25V X5R-CERM 0603

C3310 0.1UF 10% 50V X7R 603-1

CRITICAL U3310 CD3211A1RGP QFN

19 V3P3
20 V3P3
6 VHV
7 VHV
16 ENHVU
5 EN
11 HV_EN
17 S0
V3P3OUT 18 NC
OUT 12 14
FAULTZ 4
ISET_V3P3 8
ISET_S0 10
ISET_S3 9
GND THRM PAD 1 2 3 13 15 21

PPHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C3311 0.1UF 10% 50V X7R 603-1

64 IN =TBTBPWRSW_EN
26 IN TBT_B_HV_EN
64 28 IN =TBT_S0_EN

TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3

R3310 35.7K 1% 1/20W MF 201

R3311 35.7K 1% 1/20W MF 201

R3312 36.5K 1% 1/16W MF-LF 402

66 64 28 27 26 =PP3V3_S4_TBT

C3320 0.1UF 10% 6.3V CERM-X5R 0201

C3321 0.1UF 10% 6.3V CERM-X5R 0201

GND_VOID=TRUE (Both C's)

80 26 OUT TBT_B_D2R_P<1>
80 26 OUT TBT_B_D2R_N<1>

C3377 0.47UF 20% 4V CERM-X5R-1 201

C3376 0.47UF 20% 4V CERM-X5R-1 201

POLARITY SWAPPED

80 TBT_B_D2R_C_N<1> GND_VOID=TRUE
80 TBT_B_D2R_C_P<1> GND_VOID=TRUE

80 26 OUT DP_TBTPB_AUXCH_C_N
80 26 OUT DP_TBTPB_AUXCH_C_P

C3330 0.1UF 10% 6.3V CERM-X5R 0201

C3331 0.1UF 10% 6.3V CERM-X5R 0201

80 DP_TBTPB_AUXCH_N
80 DP_TBTPB_AUXCH_P

80 30 IN DP_TBTPB_DDC_DATA
80 30 IN DP_TBTPB_DDC_CLK

26 OUT TBT_B_CONFIG1_BUF

80 26 IN DP_TBTPB_ML_C_P<1>
80 26 IN DP_TBTPB_ML_C_N<1>

C3332 0.22UF 20% 6.3V X5R 0201

C3333 0.22UF 20% 6.3V X5R 0201

80 DP_TBTPB_ML_P<1>
80 DP_TBTPB_ML_N<1>

26 IN TBT_B_LSTX
26 OUT TBT_B_LSRX

26 OUT DP_TBTPB_HPD

VDD
CRITICAL U3320 CBTL05024 HVQFN24-COMBO

TB- 7
TB+ 8
AUX- 1
AUX+ 2
DDC_DAT 4
DDC_CLK 5
CA_DETOUT 16
DP+ 11
DP- 10
LSTX 14
LSRX 13
HPDOUT 12

TB_ENA 15 TBT_B_CIO_SEL IN 26
AUXIO_EN 24 TBTDP_AUXIO_EN IN 26 28
DP_PD 6 TBT_B_DP_PWRDN IN 26
GND_VOID=TRUE
AUXIO- 23 TBT_B_D2R1_AUXDDC_N 29 80
AUXIO+ 22 TBT_B_D2R1_AUXDDC_P 29 80
GND_VOID=TRUE TBT: RX_1
CA_DET 18 TBT_B_CONFIG1_RC 29
HPD 17 TBT_B_HPD 29

GND THMPAD 9 21 25

DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>

DP_B_LSX_ML_P<1> 29 80
DP_B_LSX_ML_N<1> 29 80
TBT: LSX_B_R2P/P2R (P/N)

Thunderbolt Connector B

L3300 FERR-120-OHM-3A 0603

PP3V3RHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C3300 0.01UF 10% 50V X7R-CERM 0402

C3301 0.01UF 10% 50V X7R-CERM 0402

TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V

R3301 12 5% 1/20W MF 201

C3305 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)

80 TBT_B_R2D_P<0>
80 TBT_B_R2D_N<0>

DP: Lane 0 TBT: TX_0

GND_VOID=TRUE (Both C's)

C3370 0.22UF 20% 6.3V X5R 0201

C3371 0.22UF 20% 6.3V X5R 0201

TBT_B_R2D_C_P<0> IN 26 80
TBT_B_R2D_C_N<0> IN 26 80

GND_VOID=TRUE R3370 470K 5% 1/20W MF 201

GND_VOID=TRUE R3371 470K 5% 1/20W MF 201

CRITICAL J3200 DUAL-MDP-K70

SHLD 58 57 56 55 54 53

22	HPD	F-ANG-TH	GND0 21
24	CONFIG1	ML_LANE0P	23
26	CONFIG2	ML_LANE0N	25
28	GND2	GND1	27
30	ML_LANE3P	ML_LANE1P	29
32	ML_LANE3N	ML_LANE1N	31
34	GND4	GND3	33
36	AUX_CHP	ML_LANE2P	35
38	AUX_CHN	ML_LANE2N	37
40	DP_PWR	RETURN	39

PORT B SHLD 65 64 63 62 61 60 59

C3306 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)

DP: Lane 1

DP_B_LSX_ML_P<1> 29 80
DP_B_LSX_ML_N<1> 29 80

80 TBT_B_R2D_P<1>
80 TBT_B_R2D_N<1>

DP: Lane 2 TBT: TX_1

GND_VOID=TRUE (Both C's)

C3372 0.22UF 20% 6.3V X5R 0201

C3373 0.22UF 20% 6.3V X5R 0201

POLARITY SWAPPED
TBT_B_R2D_C_N<1> IN 26 80
TBT_B_R2D_C_P<1> IN 26 80

GND_VOID=TRUE R3372 470K 5% 1/20W MF 201

GND_VOID=TRUE R3373 470K 5% 1/20W MF 201

470k R's for ESD protection
on AC-coupled signals.

J70:514-0824 / J78:514-0831

GND_VOID=TRUE
(Both C's)

POLARITY SWAPPED

C3374 0.47UF 20% 4V CERM-X5R-1 201

C3375 0.47UF 20% 4V CERM-X5R-1 201

80 26 OUT TBT_B_D2R_N<0>
80 26 OUT TBT_B_D2R_P<0>

80 TBT_B_D2R_C_P<0>
80 TBT_B_D2R_C_N<0>

TBT: RX_0

GND_VOID=TRUE R3394 1K 5% 1/20W MF 201

GND_VOID=TRUE R3395 1K 5% 1/20W MF 201

NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE

R3378 470K 5% 1/20W MF 201

R3379 470K 5% 1/20W MF 201

POLARITY SWAPPED

C3379 0.22UF 20% 6.3V X5R 0201

C3378 0.22UF 20% 6.3V X5R 0201

80 26 IN DP_TBTPB_ML_C_N<3>
80 26 IN DP_TBTPB_ML_C_P<3>

80 DP_TBTPB_ML_P<3>
80 DP_TBTPB_ML_N<3>

TBT: Terminated

DP: Lane 3

80 29 TBT_B_D2R1_AUXDDC_P
80 29 TBT_B_D2R1_AUXDDC_N

TBT: RX_1

29 TBT_B_HPD
29 TBT_B_CONFIG1_RC
26 OUT TBT_B_CONFIG2_RC

R3352 1M 5% 1/20W MF 201

R3351 1M 5% 1/20W MF 201

C3394 330PF 10% 16V X7R 0201

C3395 330PF 10% 16V X7R 0201

R3341 100K 5% 1/20W MF 201

C3302 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J70_NICK SYNC_DATE=10/16/2013

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 33 OF 123
SHEET 29 OF 81

DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.

DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

66 39 =PP3V3_S0_DP

R3485 100K 5% 1/20W MF 201

C3480 0.1UF 20% 10V CERM 402

U3400
TS3DS10224
QFN
CRITICAL

80 28 OUT DP_TBTPA_DDC_CLK
80 28 BI DP_TBTPA_DDC_DATA
80 29 OUT DP_TBTPB_DDC_CLK
80 29 BI DP_TBTPB_DDC_DATA
TBT_DDC_XBAR_EN

SAI/SBI = 1: INA == OUTA0, INB == OUTB0
SAI/SBI = 0: INA == OUTB0, INB == OUTA0

Q3400
DMN3202LFB4
DFN1006H4-3
SYM_VER_2

26 IN TBT_DDC_XBAR_EN_L

R3451 R3452 R3453 R3454
2.2K 1% 1/20W MF 201

DP_TBTSNK1_DDC_CLK IN 13 80
DP_TBTSNK1_DDC_DATA BI 13 80
DP_TBTSNK0_DDC_CLK IN 13 80
DP_TBTSNK0_DDC_DATA BI 13 80

SYNC_MASTER=J70_TONY SYNC_DATE=09/13/2017

PAGE TITLE: DDC Crossbar

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 34 OF 123
SHEET: 30 OF 81

AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22966
AP SLEW RATE	1185 us
BT SLEW RATE	1185 us
Equation	0.32*Ct + 13.7

CRITICAL
U3500
TPS22966
DPU

=PP3V3_G3H_BT → VIN1
BT_PWR_EN → ON1
BT_PWR_RAMP → CT1
=PP3V3_G3H_BT → VBIAS
=PP3V3_S4_AP → VIN2
AP_PWR_EN → ON2
AP_PWR_RAMP → CT2
VOUT1 → PP3V3_S4_AP_FET
VOUT2 → PP3V3_G3H_BT_FET
GND, THRM PAD

SMC_G3_WAKESRC_EN → R3542 10K 5% 1/16W MF-LF 402

C3541 0.001UF 10% 50V X7R-CERM 0402
C3542 0.1UF 10% 16V X7R-CERM 0402
C3543 0.001UF 10% 50V X7R-CERM 0402

BT_RESET_MASK_L
BT_RESET_MASK_L GATES BT_PWR_RST_L until after S0 GPIO is guranteed stable

BT_PWR_RST_L → CRITICAL Q3540 DMC2400UV SOT563

BT_PWR_RST → CRITICAL Q3540 DMC2400UV SOT563

R3543 10K 5% 1/16W MF-LF 402
C3540 0.01UF 20% 16V CERM 402

PP3V3_S4_AP_FET → CRITICAL L3502 FERR-220-OHM-2.5A 0603 → PP3V3_S4_AP_FLT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603

PCIE_AP_R2D_C_P → C3505 0.1UF 10% 6.3V CERM-X5R 0201 → PCIE_AP_R2D_P
PCIE_AP_R2D_C_N → C3506 0.1UF 10% 6.3V CERM-X5R 0201 → PCIE_AP_R2D_N
PLACE_NEAR=J3500.4:7mm
PLACE_NEAR=J3500.5:7mm

PP3V3_G3H_BT_FET → CRITICAL L3501 FERR-220-OHM-2.5A 0603 → PP3V3_G3H_BT_FLT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603

514S0335
CRITICAL
J3500
SSD-K99
F-RT-SM1

POLARITY SWAPPED

AP_EVENT_L
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L
USB_BT_MUX_N
USB_BT_MUX_P

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L → CRITICAL Q3501 SSM3K15AMFVAPE VESM

=PP3V3_G3H_BT → C3500 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
U3501
USB3740
DFN

USB_BT_N → DP_2
USB_BT_P → DM_2
USB_BT_WAKEN → DP_1
NC → DM_1
PM_SLP_S5_L → OE*
S → GND
DP → USB_BT_MUX_N
DM → USB_BT_MUX_P

SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

R3501 15K 1% 1/20W MF 201

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT → R3530 100K 1% 1/16W MF-LF 402
PP3V3_S4_AP_FLT → R3531 232K 1% 1/16W MF-LF 402
P3V3AP_VMON

CRITICAL
U3530
SLG4AP041V
TDFN

VDD, SENSE, VREF, DLY, RESET*, MR*, EN, IN, OUT (OD), THRM PAD, GND

=PP3V3_S4_AP → C3530 0.1UF 20% 16V CERM 402

AP_RESET_CONN_L → AP_RESET_L
AP_CLKREQ_Q_L → AP_CLKREQ_L
AP_PWR_EN

R3532 100K 1% 1/16W MF-LF 402

PP3V3_S4_AP_FLT → R3570 10K 5% 1/16W MF-LF 402 → Q3570 CRITICAL SSM3K15AMFVAPE VESM → AP_WAKE_L
PCIE_WAKE_L

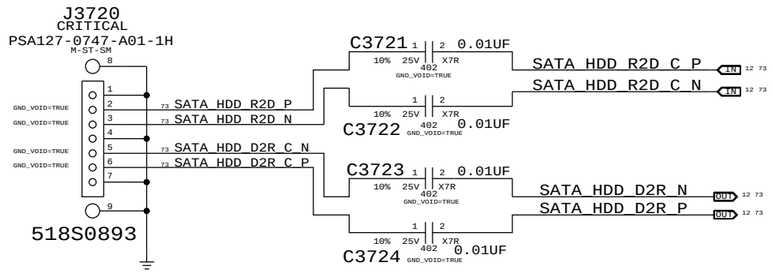
SYNC_MASTER=J70_DINI SYNC_DATE=10/08/2013

PAGE TITLE: AIRPORT/BT

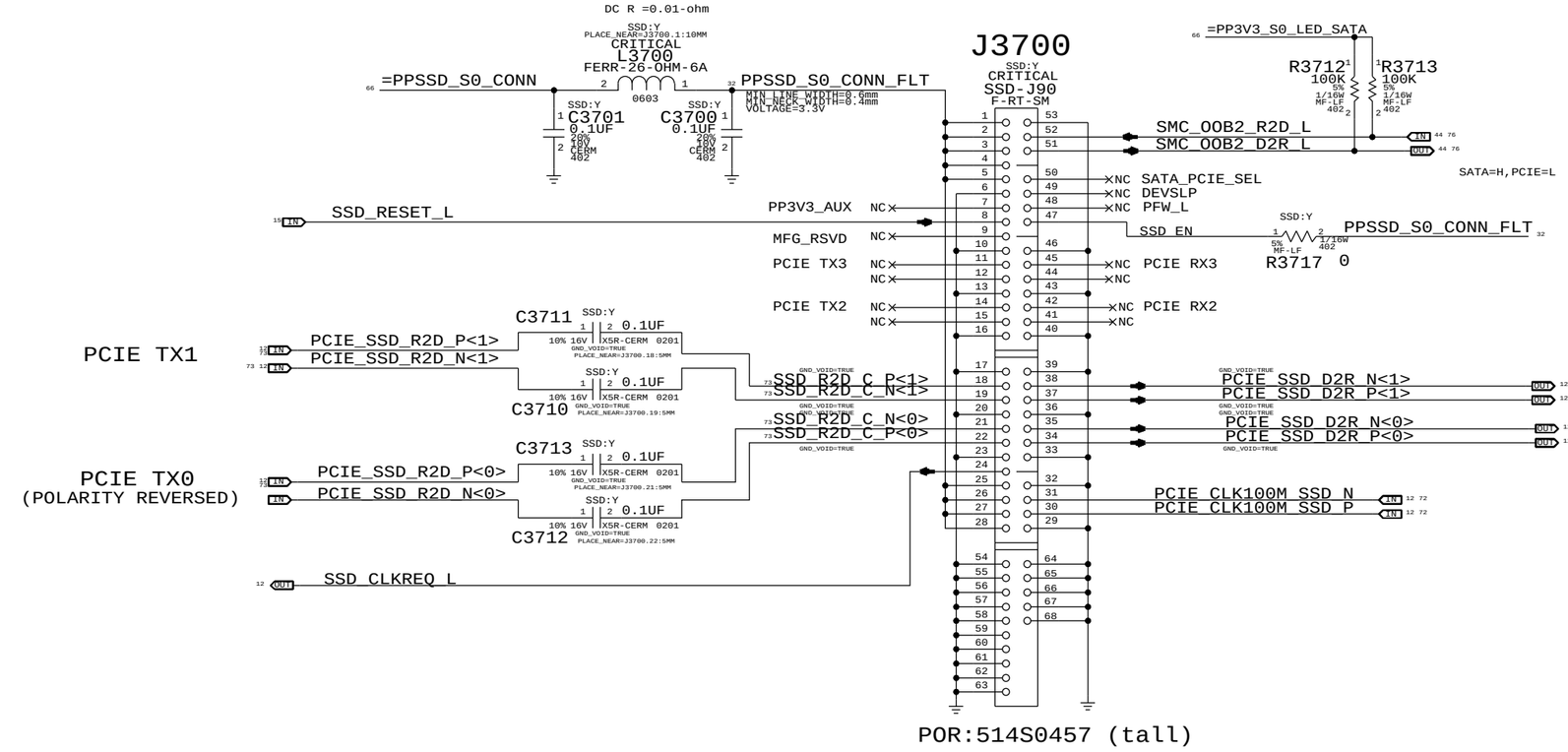
Apple Inc.

DRAWING NUMBER: 051-1407
SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 35 OF 123
SHEET: 31 OF 81

HDD SIGNAL CONNECTOR



GS3 SSD



Note:Bead Probes needed

PCIE RX1

PCIE RX0

PCIEx2 SSD requires AC coupling caps on TX side

SYNC_MASTER=J70_DINI SYNC_DATE=10/14/2013

PAGE TITLE
SATA/SSD Connectors

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

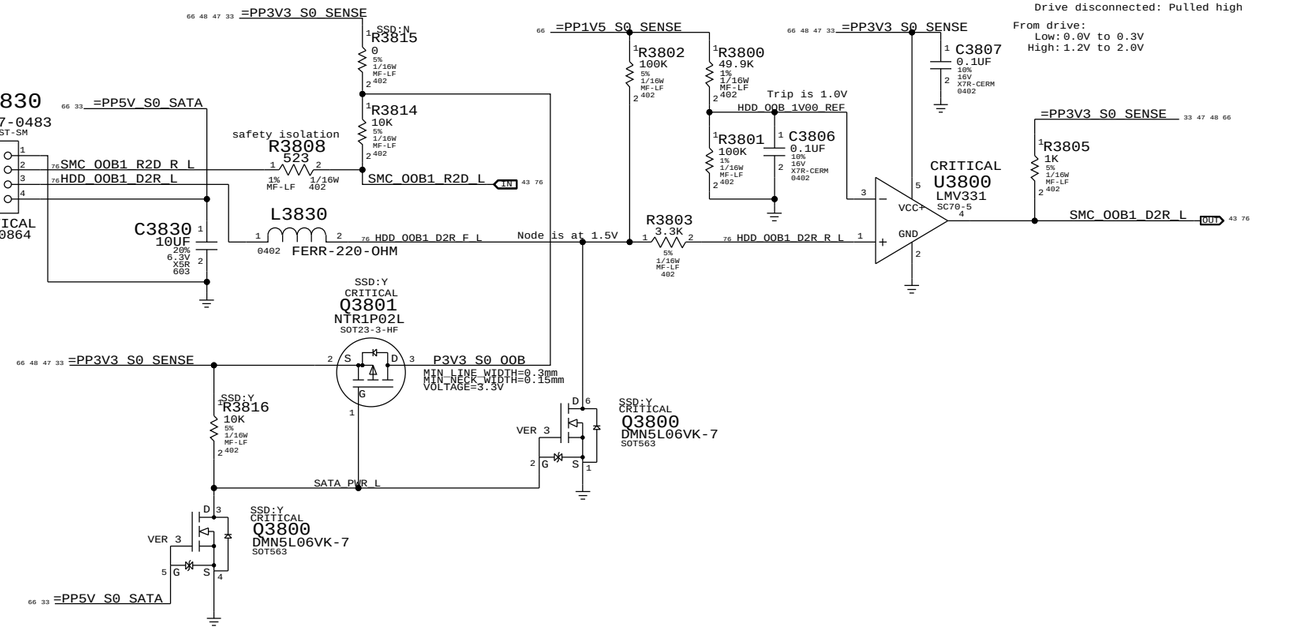
BRANCH

PAGE 37 OF 123

SHEET 32 OF 81

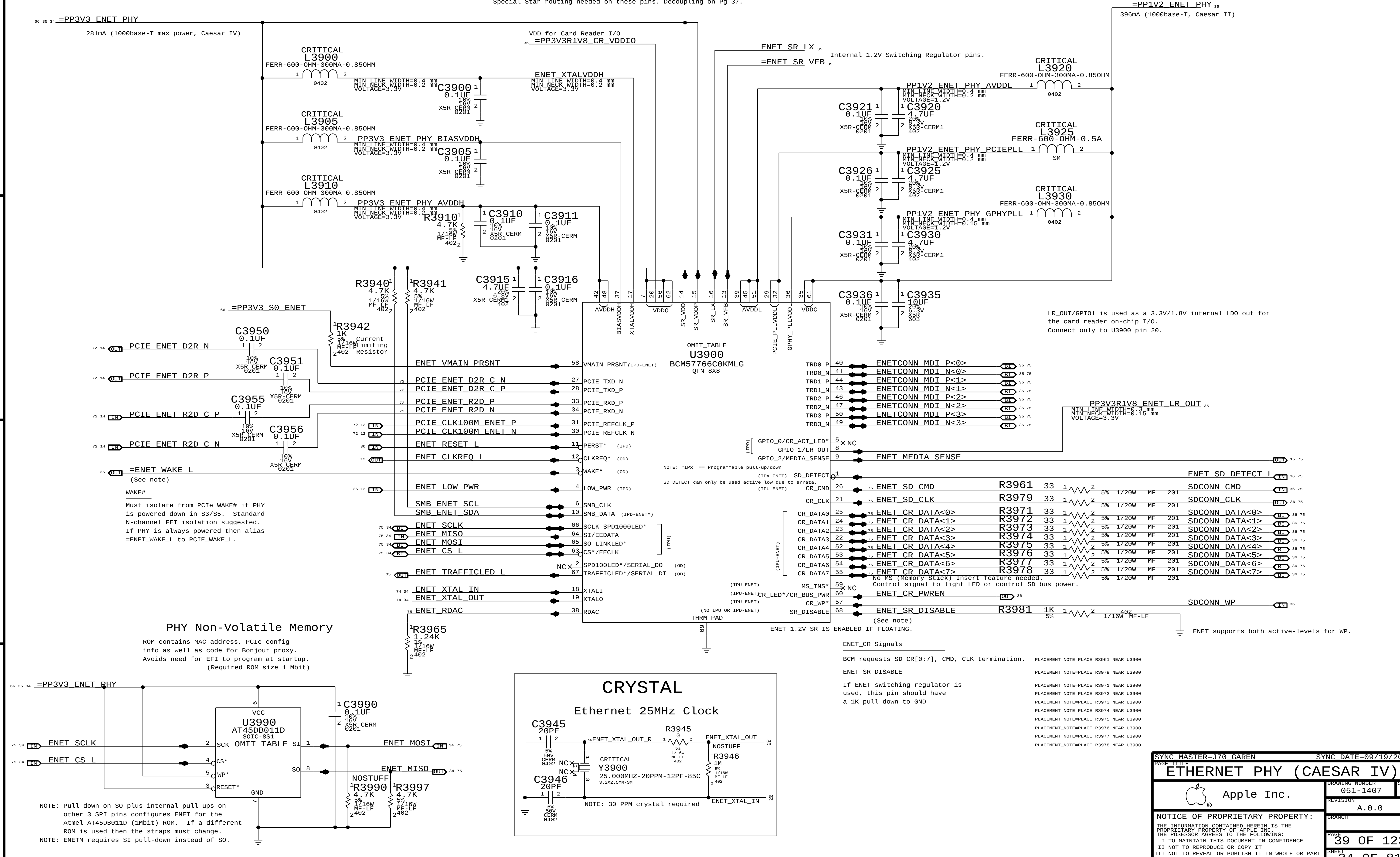
HDD POWER/OOB CONNECTOR

HDD Out-of-Band Temperature Sensing



SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE: HDD Connector	
Apple Inc.	DRAWING NUMBER: 051-1407 · SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 38 OF 123
	SHEET: 33 OF 81

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.



=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)
VDD for Card Reader I/O
=PP3V3R1V8_CR_VDDIO
=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)
ENET_SR_LX
=ENET_SR_VFB
Internal 1.2V Switching Regulator pins.
CRITICAL
L3900
FERR-600-OHM-300MA-0.85OHM
ENET_XTALVDDH
C3900
0.1UF
L3905
PP3V3_ENET_PHY_BIASVDDH
C3905
L3910
PP3V3_ENET_PHY_AVDDH
R3910
4.7K
C3910
C3911
L3920
PP1V2_ENET_PHY_AVDDL
C3921
C3920
4.7UF
L3925
FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926
C3925
L3930
PP1V2_ENET_PHY_GPHYPLL
C3931
C3930
C3936
C3935
10UF
R3940
R3941
C3915
C3916
=PP3V3_S0_ENET
R3942
1K
Current Limiting Resistor
LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.
OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8
PCIE_ENET_D2R_N
C3950
PCIE_ENET_D2R_P
C3951
PCIE_ENET_R2D_C_P
C3955
PCIE_ENET_R2D_C_N
C3956
=ENET_WAKE_L
(See note)
WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.
ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
ENET_TRAFFICLED_L
ENET_XTAL_IN
ENET_XTAL_OUT
ENET_RDAC
R3965
1.24K
ENETCONN_MDI_P<0>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<2>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
PP3V3R1V8_ENET_LR_OUT
ENET_MEDIA_SENSE
ENET_SD_DETECT_L
NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.
ENET_SD_CMD
R3961
SDCONN_CMD
ENET_SD_CLK
R3979
SDCONN_CLK
ENET_CR_DATA<0>
ENET_CR_DATA<1>
ENET_CR_DATA<2>
ENET_CR_DATA<3>
ENET_CR_DATA<4>
ENET_CR_DATA<5>
ENET_CR_DATA<6>
ENET_CR_DATA<7>
R3971
R3972
R3973
R3974
R3975
R3976
R3977
R3978
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.
ENET_CR_PWREN
SDCONN_WP
ENET_SR_DISABLE
R3981
1K
(See note)
ENET 1.2V SR IS ENABLED IF FLOATING.
ENET supports both active-levels for WP.
ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.
ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND
PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900
PHY Non-Volatile Memory
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)
U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE
C3990
R3990
R3997
NOSTUFF
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.
CRYSTAL
Ethernet 25MHz Clock
C3945
20PF
R3945
ENET_XTAL_OUT_R
CRITICAL
Y3900
25.000MHZ-20PPM-12PF-85C
R3946
1M
C3946
NOTE: 30 PPM crystal required

SYNC_MASTER=J70_GAREN SYNC_DATE=09/19/2013

PAGE TITLE: ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

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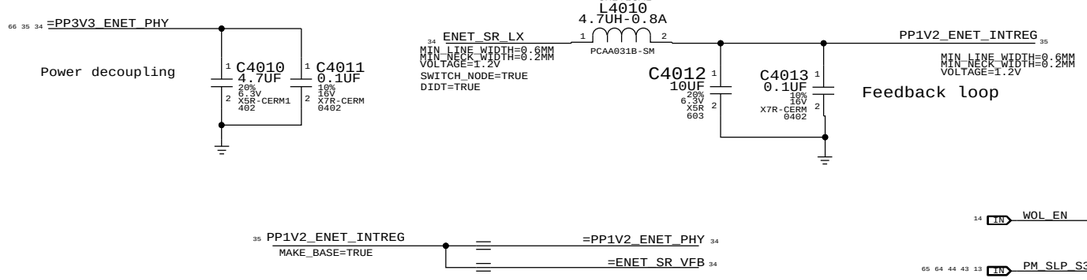
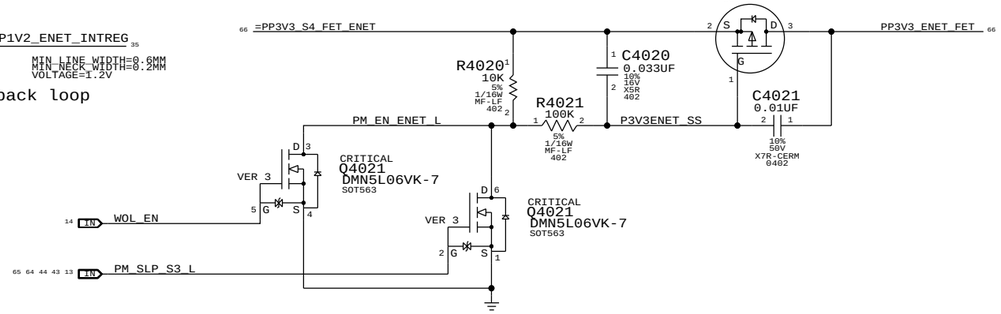
CAESAR IV 1.2V INT.VR CMPTS

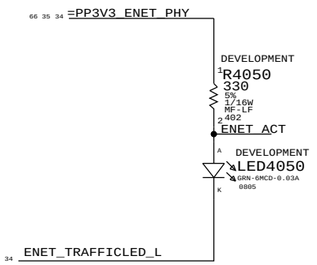


ENET Enable Generation

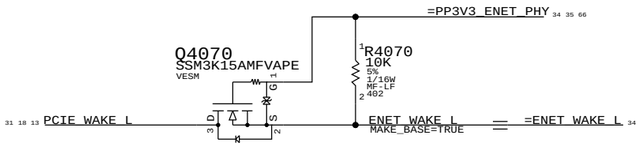
"ENET" = "S0" || ("S4" && "WOL_EN")

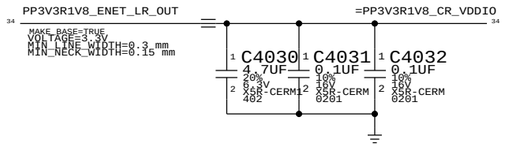


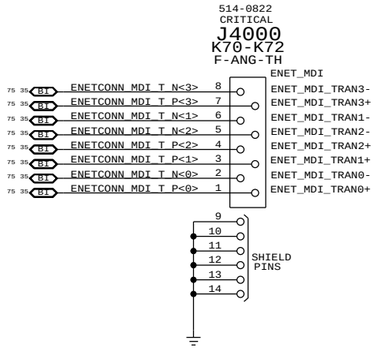
CAESAR IV ACTIVITY LED



CAESAR IV WAKE# ISOLATION







SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE

Ethernet Support & Connector

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

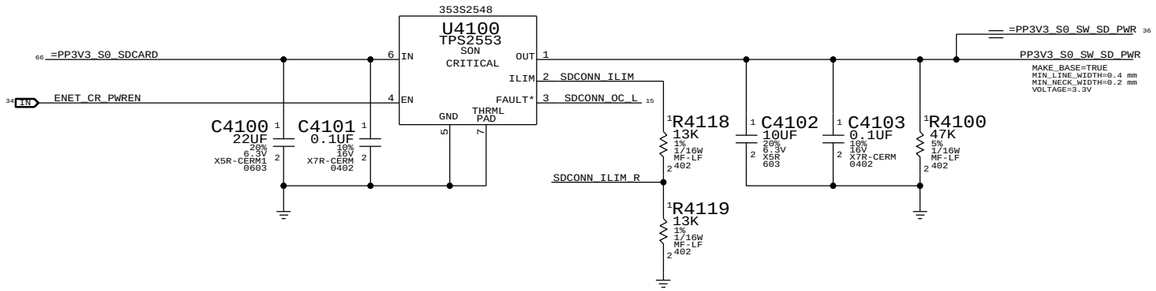
REVISION A.0.0

BRANCH

PAGE 40 OF 123

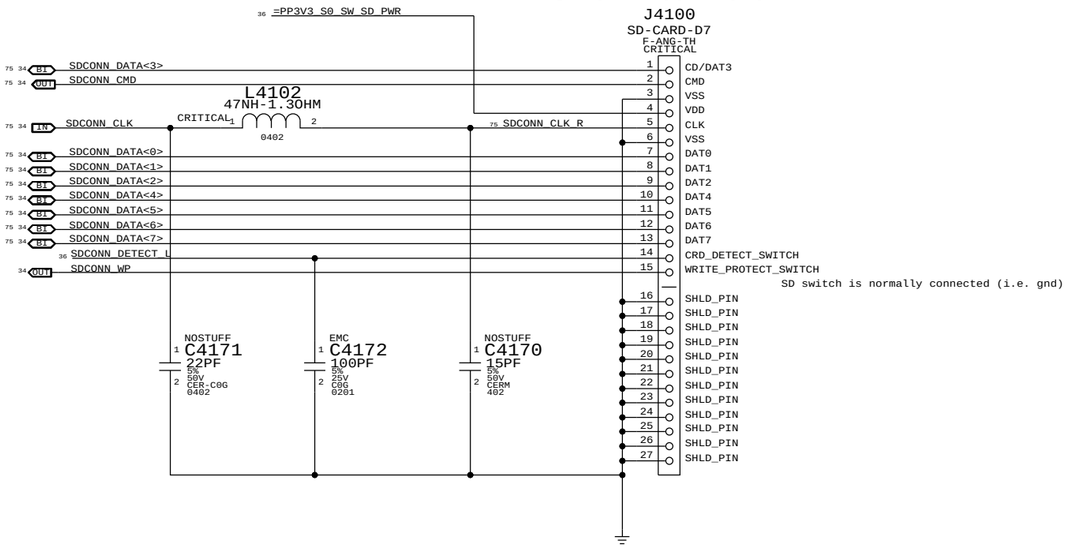
SHEET 35 OF 81

SD CARD 3.3V OVERCURRENT PROTECTION CHIP

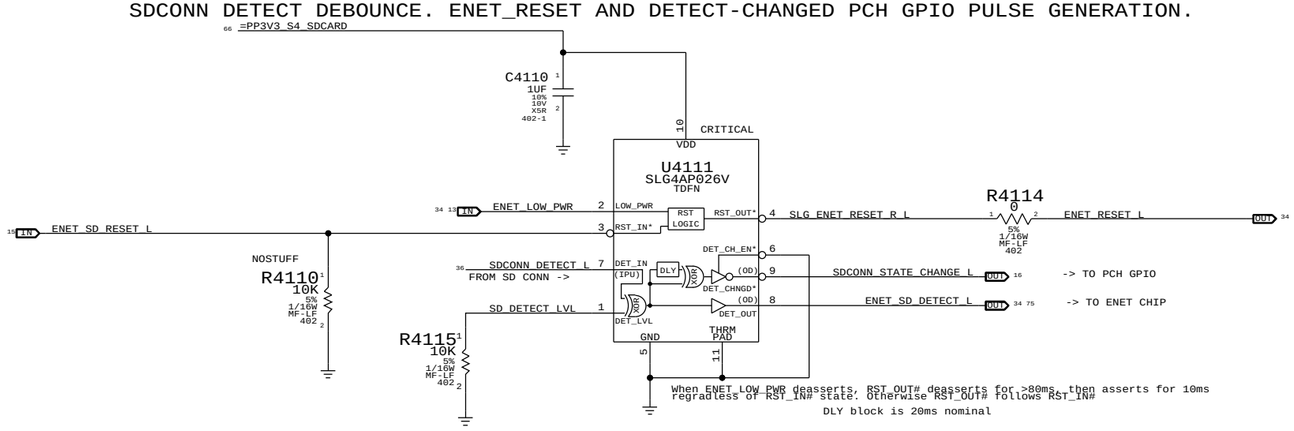


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



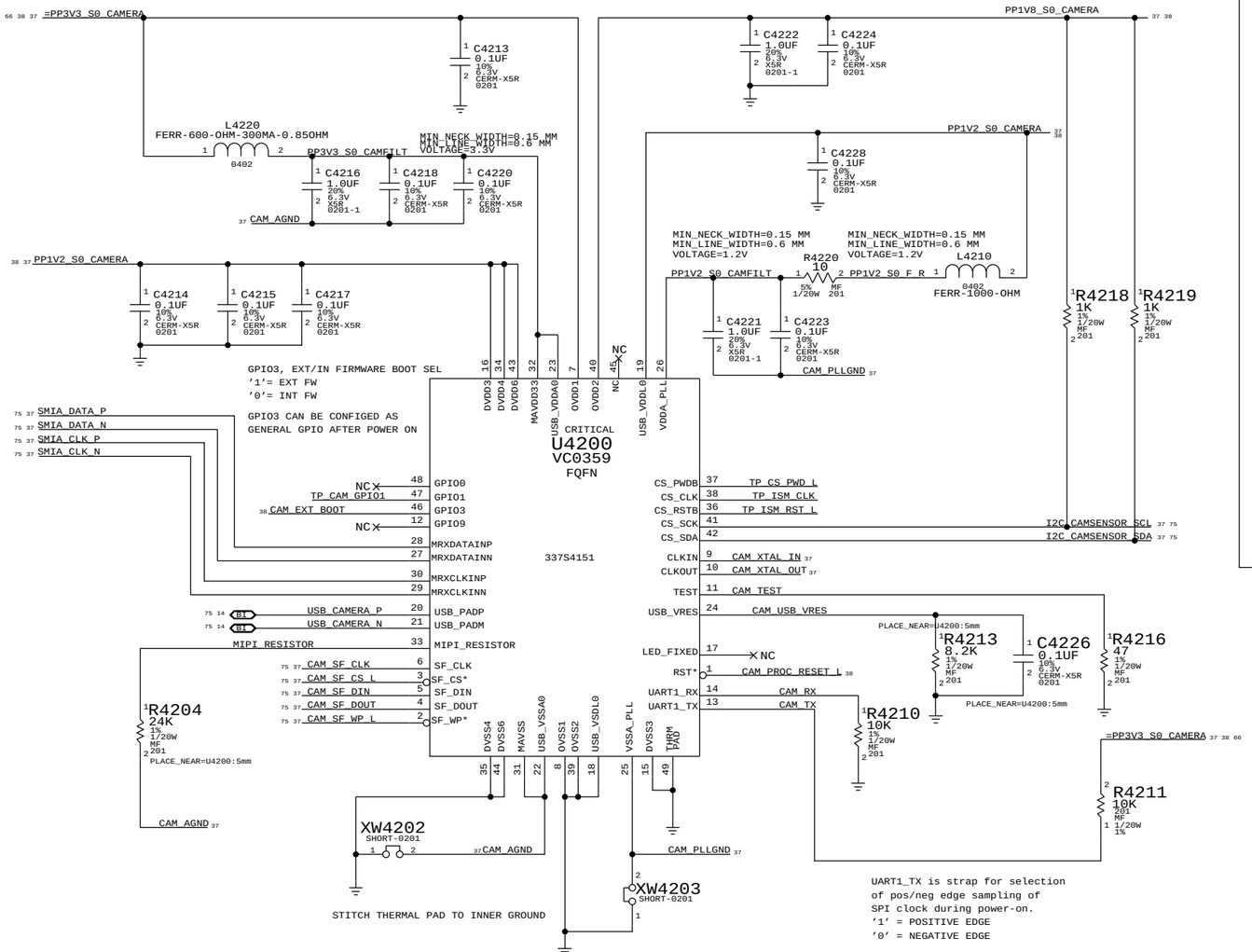
SYNC_MASTER=J70 GAREN SYNC_DATE=09/23/2013

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

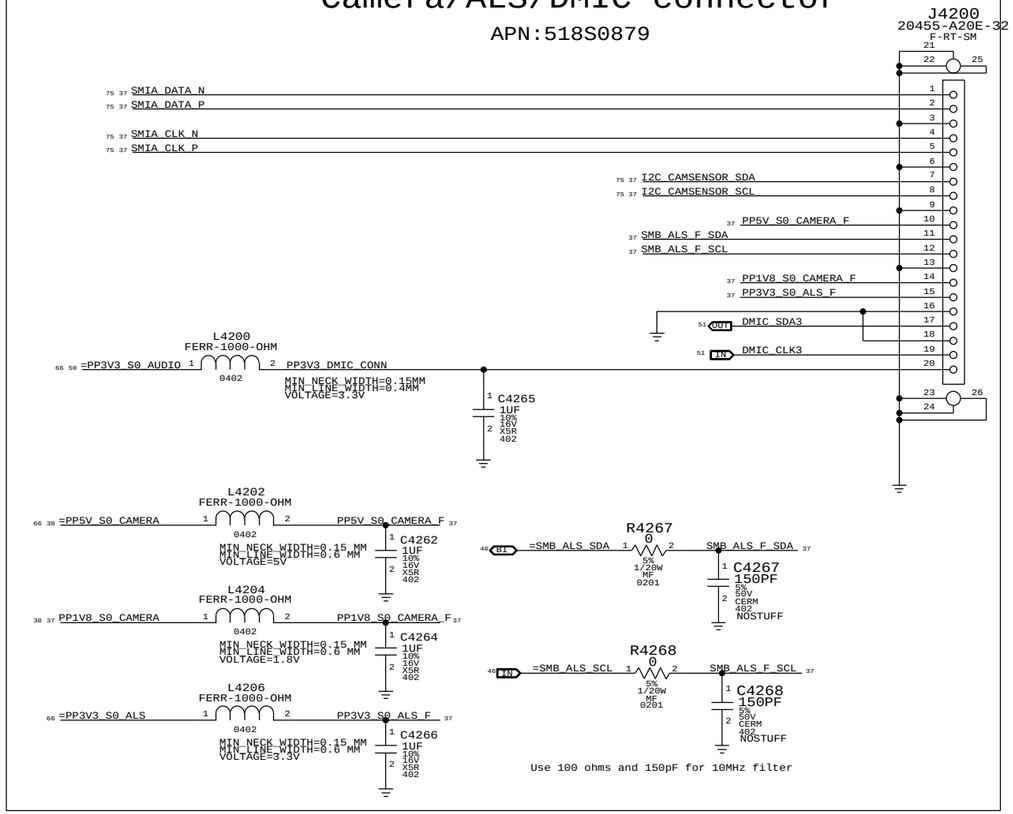
DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 41 OF 123
SHEET 36 OF 81

USB CAMERA CONTROLLER

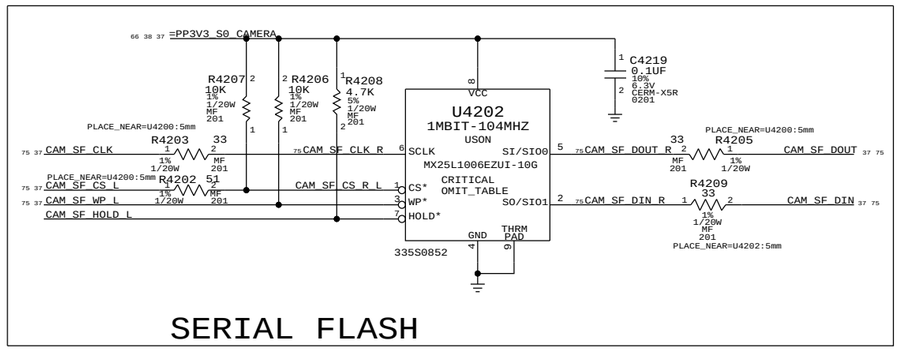


Camera/ALS/DMIC connector

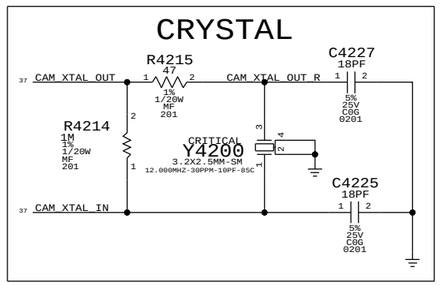
APN:518S0879



SERIAL FLASH



CRYSTAL



SYNC_MASTER=J70_GAREN SYNC_DATE=02/05/2014

PAGE TITLE: Camera Controller

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

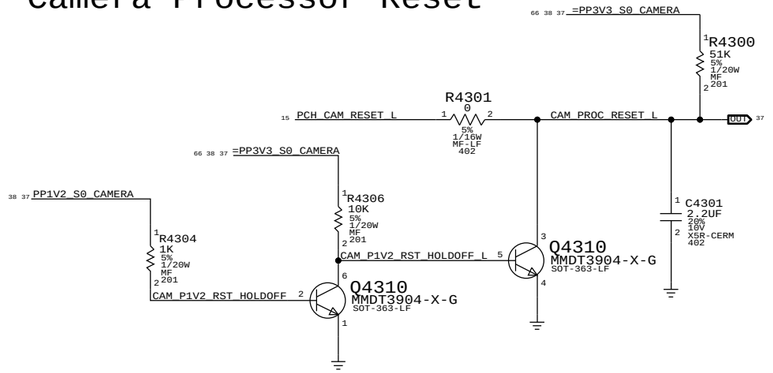
REVISION: A.0.0

BRANCH:

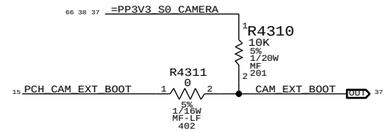
PAGE: 42 OF 123

SHEET: 37 OF 81

Camera Processor Reset



Camera Processor ExtBoot Cntl



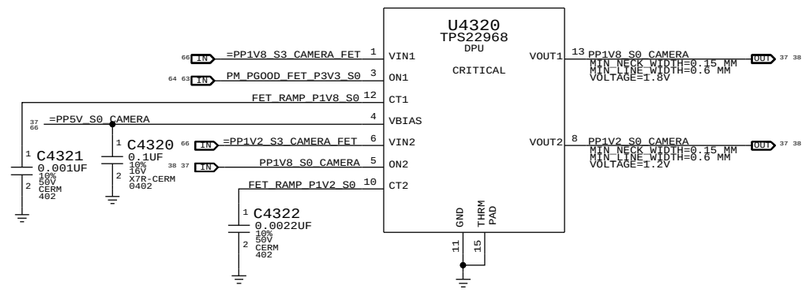
1.8V S0 and 1.2V S0 Load Switch

POWER SEQUENCE

3.3V => 1.8V => 1.2V

Enable 1.8V camera rail when 3.3V S0 rail is on

Enable 1.2V camera rail when 1.8V S0 rail is on



Capacitor Values Found Using
Slew Rate(us/V) = 0.32*CT(pF) + 13.7

Rise Times:
1.8V S0 -- 1000 pF -- 600 us
1.2V S0 -- 2200 pF -- 881 us

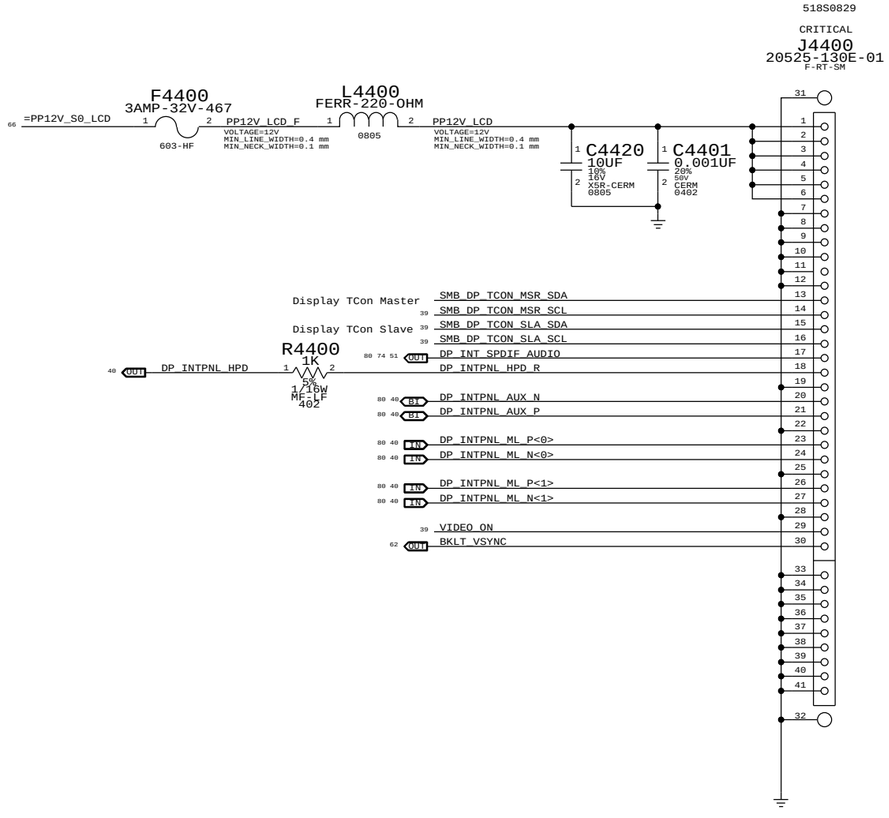
SYNC_MASTER=J70_GAREN SYNC_DATE=10/24/2013

PAGE_TITLE
Camera Controller Support

Apple Inc.

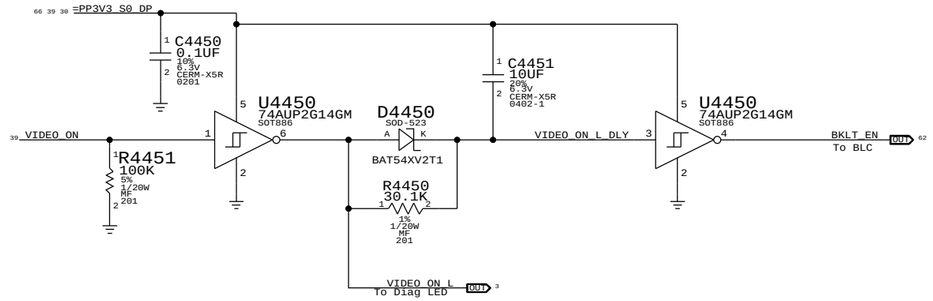
DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 43 OF 123
SHEET 38 OF 81

Internal DP Connector



Backlight Control

Delay applies only on a L->H transition on VIDEO_ON. This guarantees video is valid before the backlight is enabled.
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video

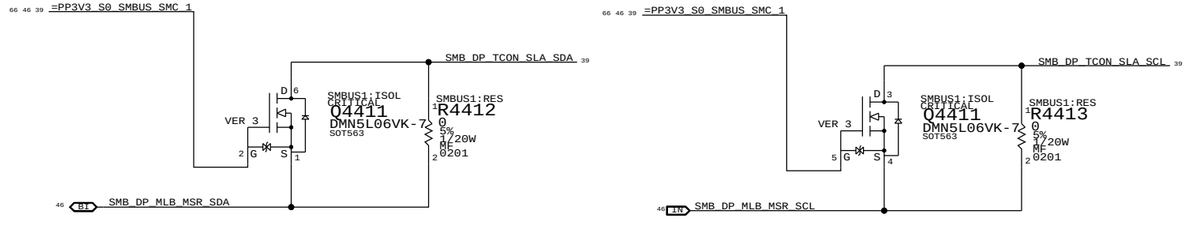


SMBus Isolation

TCON Master

Active switch used on TCON Master I2C bus to ensure integrity of 400 kHz transactions on powerup

MLB Master



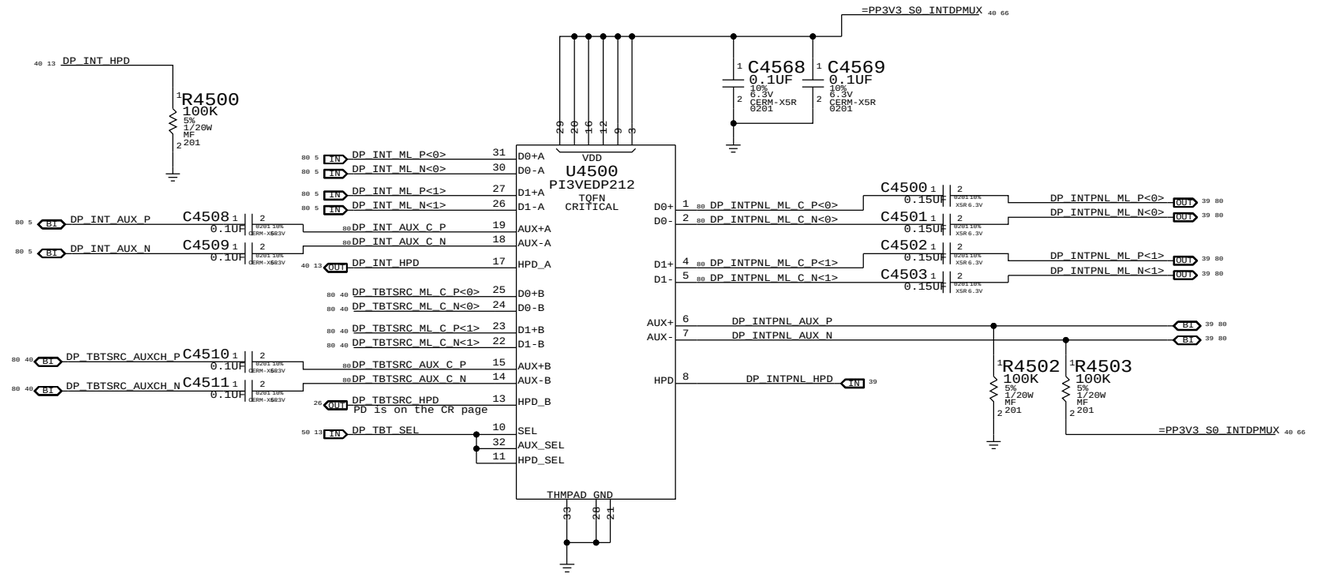
SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE: Internal DP Support	
Apple Inc.	DRAWING NUMBER: 051-1407 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 44 OF 123
	SHEET: 39 OF 81

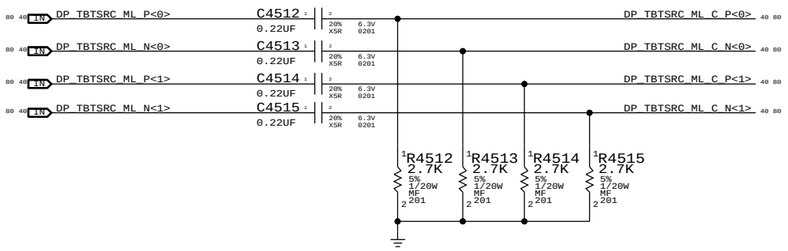
TP to DP aliases

26 IN TP_DP_TBTSRC_ML_CP<0> — DP_TBTSRC_ML_P<0> 40 80 MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<0> — DP_TBTSRC_ML_N<0> 40 80 MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CP<1> — DP_TBTSRC_ML_P<1> 40 80 MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<1> — DP_TBTSRC_ML_N<1> 40 80 MAKE_BASE=TRUE
26 BI TP_DP_TBTSRC_AUXCH_CP — DP_TBTSRC_AUXCH_P 40 80 MAKE_BASE=TRUE
26 BI TP_DP_TBTSRC_AUXCH_CN — DP_TBTSRC_AUXCH_N 40 80 MAKE_BASE=TRUE

NC aliases

26 IN TP_DP_TBTSRC_ML_CP<2> — NC_DP_TBTSRC_ML_P<2> NO_TEST=TRUE MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<2> — NC_DP_TBTSRC_ML_N<2> NO_TEST=TRUE MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CP<3> — NC_DP_TBTSRC_ML_P<3> NO_TEST=TRUE MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<3> — NC_DP_TBTSRC_ML_N<3> NO_TEST=TRUE MAKE_BASE=TRUE
5 IN DP_INT_ML_P<2> — NC_DP_INT_ML_P<2> NO_TEST=TRUE MAKE_BASE=TRUE
5 IN DP_INT_ML_N<2> — NC_DP_INT_ML_N<2> NO_TEST=TRUE MAKE_BASE=TRUE
5 IN DP_INT_ML_P<3> — NC_DP_INT_ML_P<3> NO_TEST=TRUE MAKE_BASE=TRUE
5 IN DP_INT_ML_N<3> — NC_DP_INT_ML_N<3> NO_TEST=TRUE MAKE_BASE=TRUE



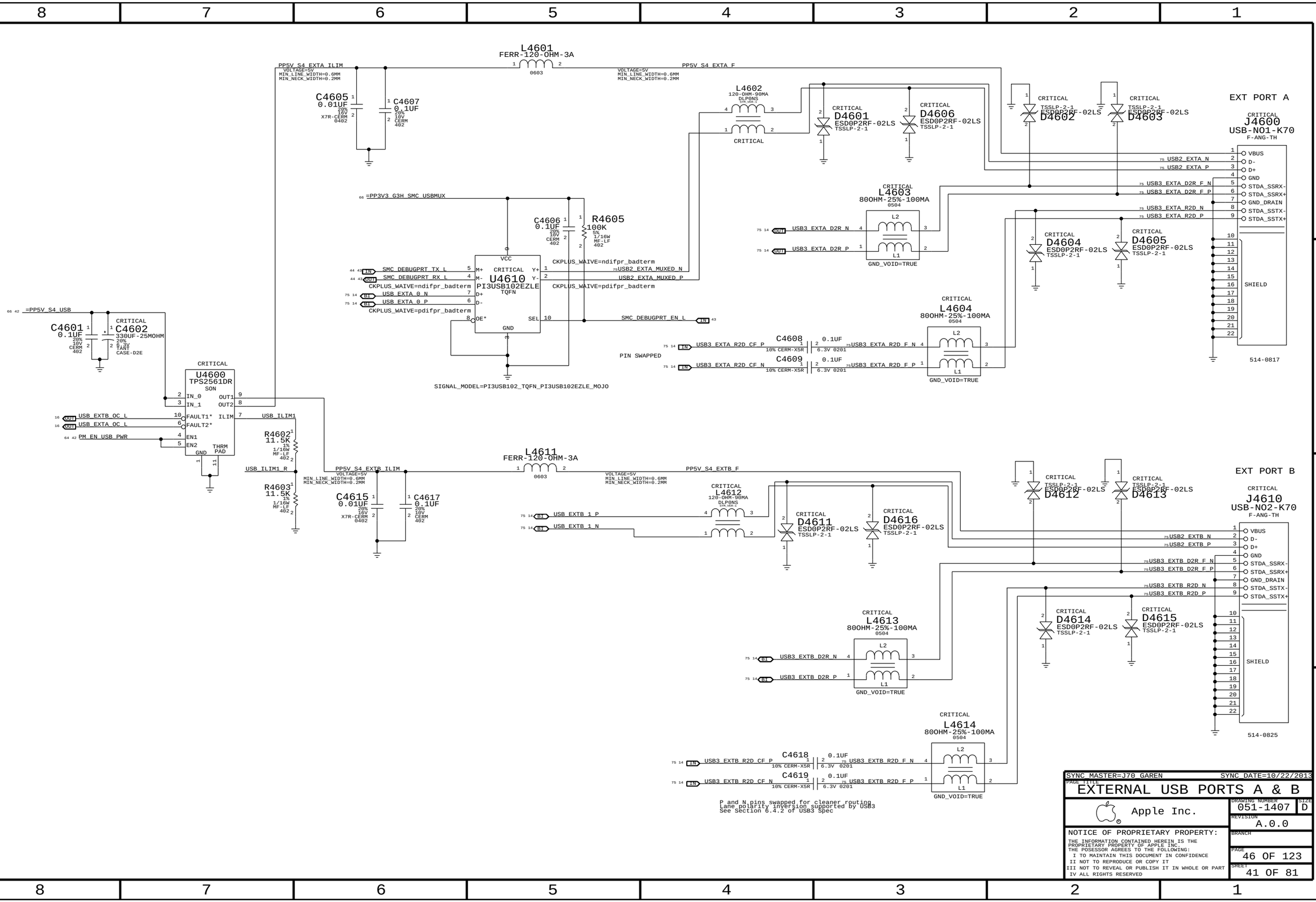


SYNC_MASTER=J70_TONY SYNC_DATE=09/05/2013

PAGE TITLE: Internal DP MUXing

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 45 OF 123
SHEET: 40 OF 81


L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
C4605
0.01UF
20%
16V
X7R-CERM
0402
C4607
0.1UF
20%
10V
CERM
402
PP5V_S4_EXTA_F
L4602
120-OHM-90MA
DLP0NS
CRITICAL
D4601
ESD0P2RF-02LS
TSSLP-2-1
D4606
ESD0P2RF-02LS
TSSLP-2-1
D4602
ESD0P2RF-02LS
TSSLP-2-1
D4603
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT A
J4600
USB-NO1-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0817
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_D2R_F_N
USB3_EXTA_D2R_F_P
USB3_EXTA_R2D_N
USB3_EXTA_R2D_P
=PP3V3_G3H_SMC_USBMUX
C4606
0.1UF
R4605
100K
5%
1/16W
MF-LF
402
U4610
PI3USB102EZLE
TQFN
VCC
GND
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
USB_EXTA_0_N
USB_EXTA_0_P
CKPLUS_WAIVE=ndifpr_badterm
CKPLUS_WAIVE=pdifpr_badterm
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
SEL
SMC_DEBUGPRT_EN_L
SIGNAL_MODEL=PI3USB102_TQFN_PI3USB102EZLE_MOJO
L4603
80OHM-25%-100MA
0504
L2
L1
GND_VOID=TRUE
L4604
80OHM-25%-100MA
0504
C4608
C4609
0.1UF
10% CERM-X5R
6.3V 0201
PIN SWAPPED
D4604
ESD0P2RF-02LS
TSSLP-2-1
D4605
ESD0P2RF-02LS
TSSLP-2-1
=PP5V_S4_USB
C4601
0.1UF
C4602
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
U4600
TPS2561DR
SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
ILIM
THRM PAD
GND
OUT1
OUT2
USB_EXTB_OC_L
USB_EXTA_OC_L
PM_EN_USB_PWR
USB_ILIM1
R4602
11.5K
1%
1/16W
MF-LF
402
USB_ILIM1_R
R4603
11.5K
C4615
0.01UF
C4617
0.1UF
L4611
FERR-120-OHM-3A
0603
L4612
120-OHM-90MA
DLP0NS
D4611
ESD0P2RF-02LS
TSSLP-2-1
D4616
ESD0P2RF-02LS
TSSLP-2-1
D4612
ESD0P2RF-02LS
TSSLP-2-1
D4613
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT B
J4610
USB-NO2-K70
F-ANG-TH
USB_EXTB_1_P
USB_EXTB_1_N
L4613
80OHM-25%-100MA
0504
L4614
80OHM-25%-100MA
0504
C4618
C4619
0.1UF
10% CERM-X5R
6.3V 0201
D4614
ESD0P2RF-02LS
TSSLP-2-1
D4615
ESD0P2RF-02LS
TSSLP-2-1
514-0825
P and N pins swapped for cleaner routing
Lane polarity inversion supported by USB3
See Section 6.4.2 of USB3 Spec
SYNC_MASTER=J70_GAREN
SYNC_DATE=10/22/2013
PAGE TITLE
EXTERNAL USB PORTS A & B
Apple Inc.
DRAWING NUMBER
051-1407
SIZE
D
REVISION
A.0.0
BRANCH
PAGE
46 OF 123
SHEET
41 OF 81
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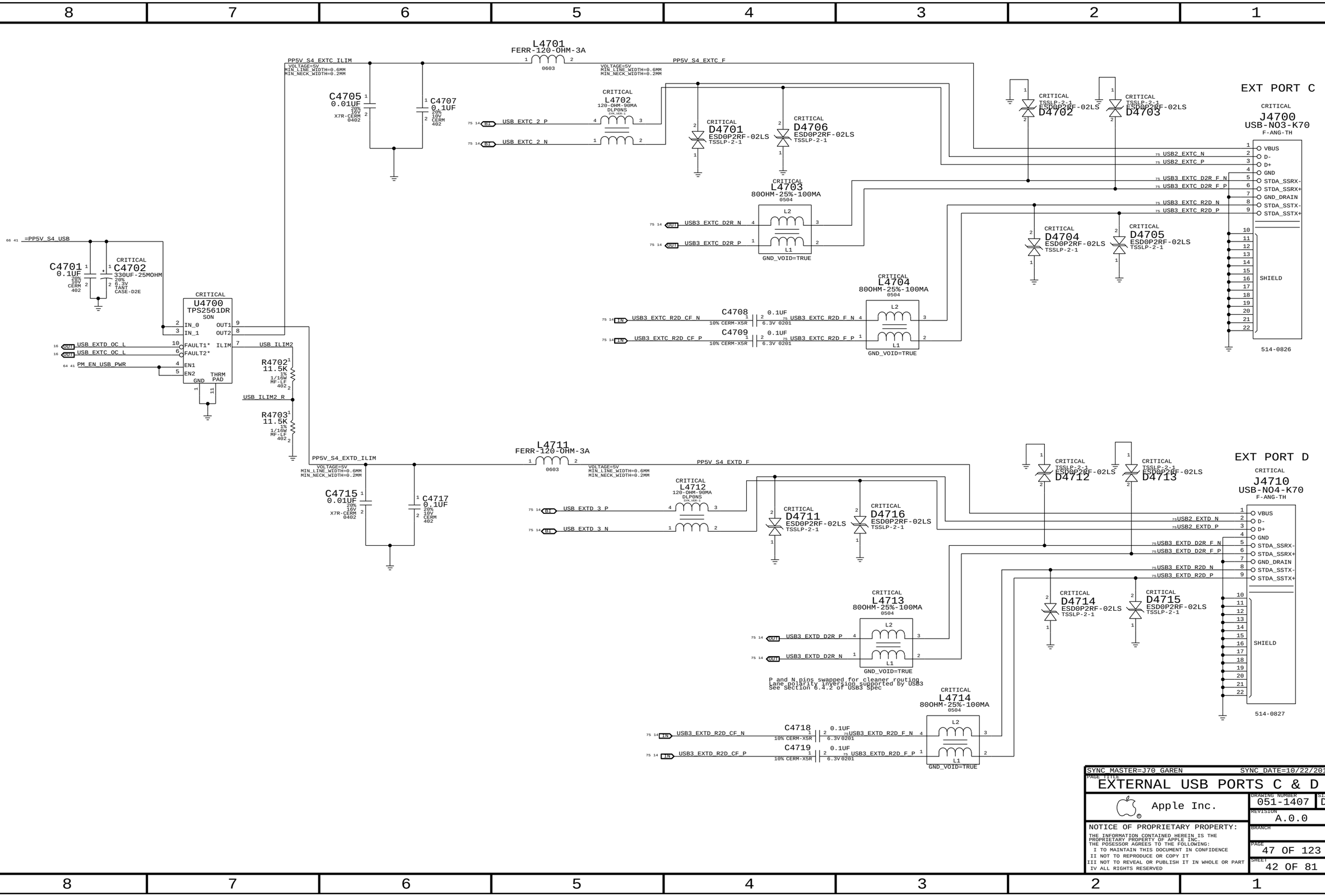


SYNC_MASTER=J70_GAREN SYNC_DATE=10/22/2013

PAGE TITLE

EXTERNAL USB PORTS C & D

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

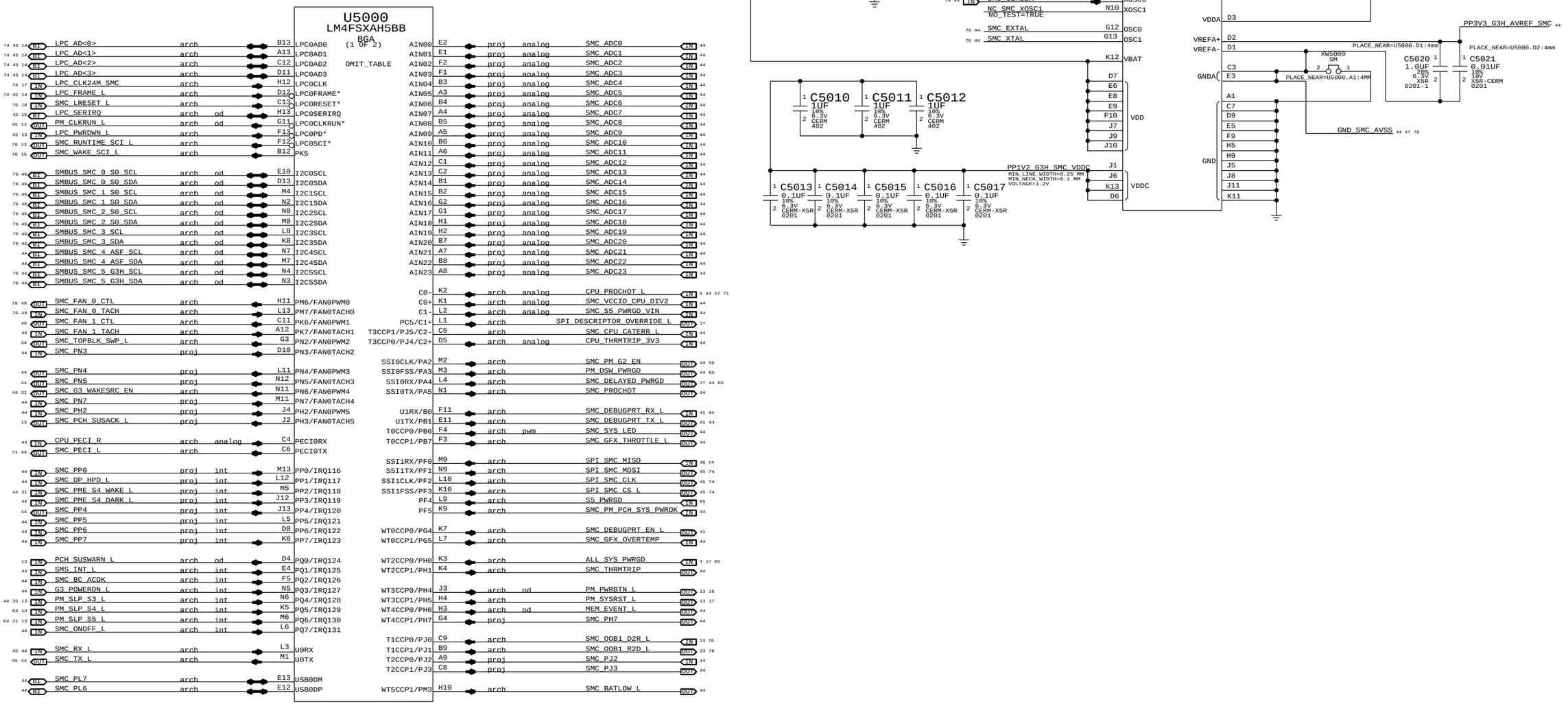
REVISION A.0.0

BRANCH

PAGE 47 OF 123

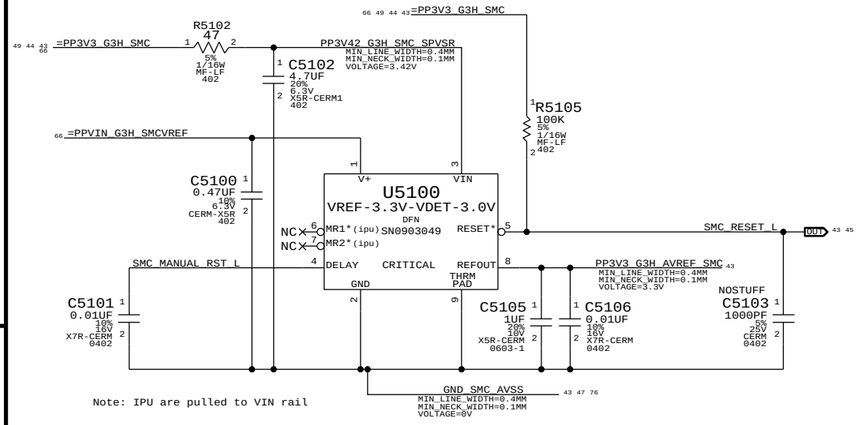
SHEET 42 OF 81

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SYNC_MASTER=J70_NICK	SYNC_DATE=09/24/2013
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER 051-1407
	SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 50 OF 123
	SHEET 43 OF 81

SMC Supervisor and AVREF Supply



Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC6	VSNS_P1V2_S3_DDR	MAKE_BASE=TRUE
SMC_ADC7	ISNS_P1V2_S3_DDR	MAKE_BASE=TRUE
SMC_ADC10	VSNS_CPUVCC	MAKE_BASE=TRUE
SMC_ADC11	ISNS_CPUVCC	MAKE_BASE=TRUE
SMC_ADC20	VSNS_P3V3_SSD	MAKE_BASE=TRUE
SMC_ADC21	ISNS_SSDS0	MAKE_BASE=TRUE

Unused ADC Channels

SMC_PH3	NC_SMC_PH3	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC2	NC_VSNS_P12VS0_GPUCORE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC3	NC_ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC4	NC_VSNS_PVDDQS0	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC5	NC_ISNS_PVDDQS0	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC8	NC_VSNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC9	NC_ISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC12	NC_VSNS_GPUCORE_ALT	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC13	NC_ISNS_GPUCORE_ALT	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC14	NC_VSNS_HDDS0	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC15	NC_ISNS_HDDS0	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC16	NC_SMC_ADC16	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC17	NC_SMC_ADC17	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC18	NC_VSNS_P1V05S0_PCH	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC19	NC_ISNS_P3V3S4_AP	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC23	NC_SMC_ADC23	MAKE_BASE=TRUE NO_TEST=TRUE

Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE
SMC_PL6	SMC_WIFI_PWR_EN	MAKE_BASE=TRUE

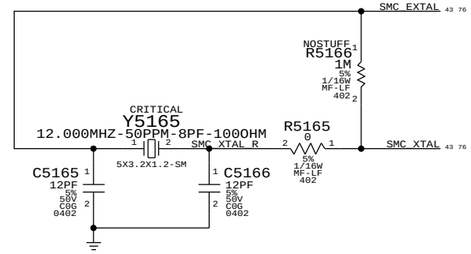
Unused Project-specific

SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PL7	NC_SMC_PL7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN4	NC_SMC_PN4	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE NO_TEST=TRUE
TP for access if ZPB re-intstated		
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_BATLOW_L	NC_SMC_BATLOW_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE NO_TEST=TRUE
MEM_EVENT_L	NC_MEM_EVENT_L	MAKE_BASE=TRUE NO_TEST=TRUE

SMC 32KHz Clock

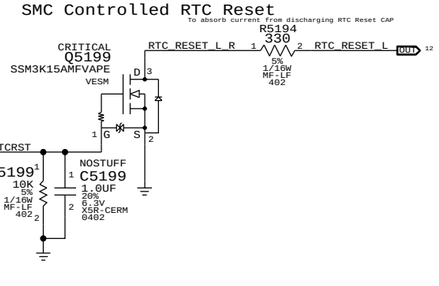
SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal

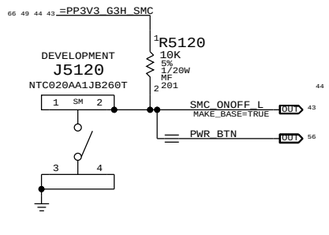


SMC Controlled RTC Reset

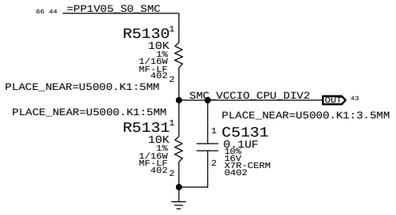
To absorb current from discharging RTC Reset CAP



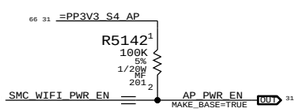
Power Button



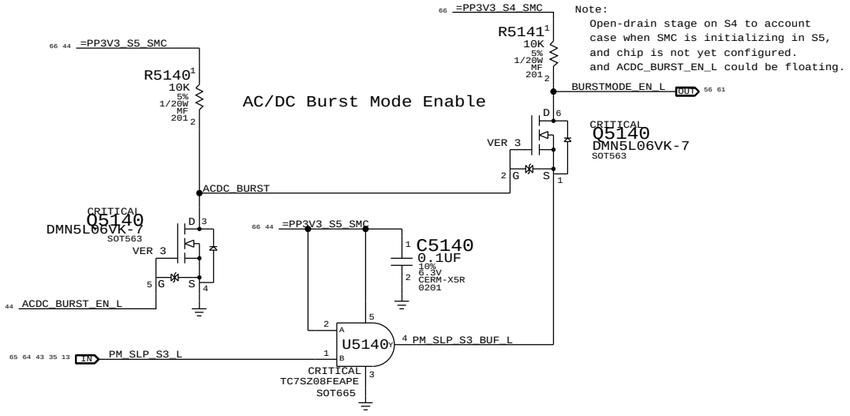
Comparator Reference



SMC control for AirPort power



AC/DC Burst Mode Enable



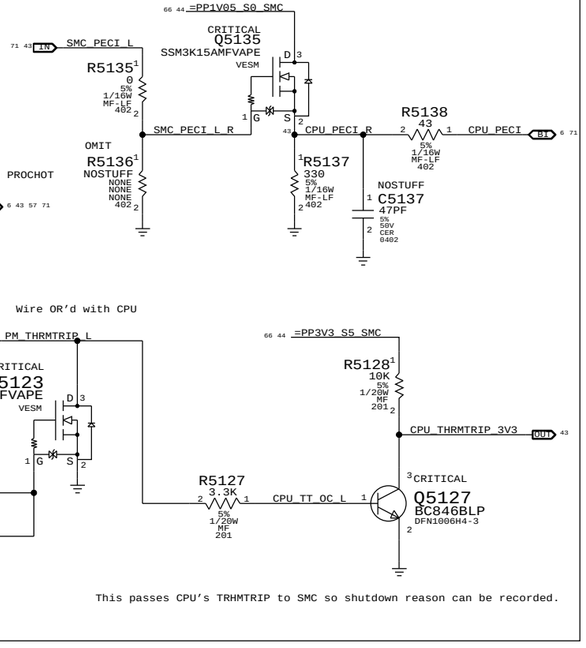
Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

Platform Thermal Control

PECI Support

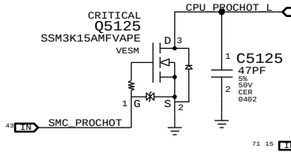
Level-shifter that allows SMC to drive PECI

Place this circuit near the Tee point to minimize reflections



PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT



Wire OR'd with CPU

This passes CPU's TRHMTRIP to SMC so shutdown reason can be recorded.

Arch Pull Up/Down

SMC_TOPBLK_SWP_L	R5171	1K	5% 1/20W MF 201 =PP3V3_S0_SMC
G3_POWERON_L	R5176	10K	5% 1/20W MF 201 =PP3V3_G3H_SMC
SMC_BC_ACOK	R5178	100K	5% 1/20W MF 201
SMC_SYS_LED NOSTUFF	R5179	100K	5% 1/20W MF 201
SMS_INT_L	R5180	10K	5% 1/20W MF 201
SMC_PME_S4_WAKE_L	R5181	10K	5% 1/20W MF 201
AP_EVENT_L	R5185	10K	5% 1/20W MF 201 PP3V3_S4_AP_FET
SMC_G3_WAKESRC_EN	R5118	100K	5% 1/20W MF 201
SMC_DELAYED_PWRGD	R5186	100K	5% 1/16W MF-LF 402
PM_DSW_PWRGD	R5184	100K	5% 1/16W MF-LF 402
SMC_PM_G2_EN	R5187	100K	5% 1/20W MF 201

Note:

Serial/JTAG Interface Pull-ups

SMC_TX_L	R5190	10K	5% 1/20W MF 201 =PP3V3_G3H_SMC
SMC_RX_L	R5191	100K	5% 1/20W MF 201
SMC_DEBUGPRT_TX_L	R5192	20K	5% 1/20W MF 201
SMC_DEBUGPRT_RX_L	R5193	20K	5% 1/20W MF 201
SMC_TCK	R5195	10K	5% 1/20W MF 201
SMC_TDI	R5196	10K	5% 1/20W MF 201
SMC_TDO	R5197	10K	5% 1/20W MF 201
SMC_TMS	R5198	10K	5% 1/20W MF 201

SYNC_MASTER=J70_NICK SYNC_DATE=01/15/2014

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

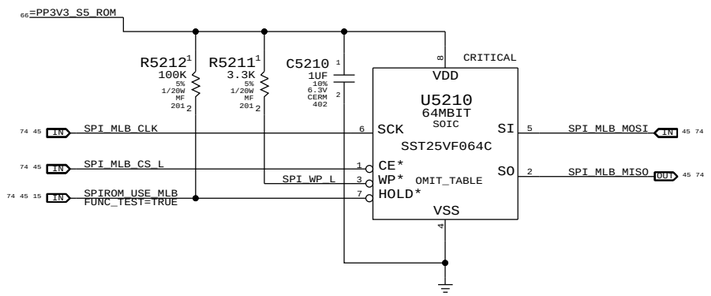
REVISION: A.0.0

BRANCH:

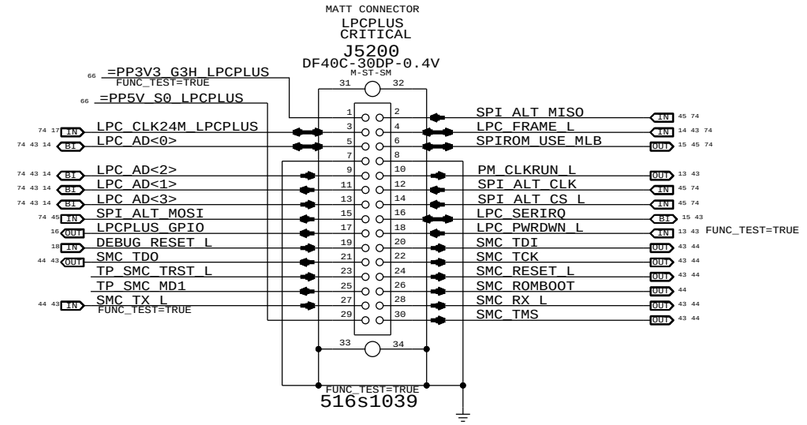
PAGE: 51 OF 123

SHEET: 44 OF 81

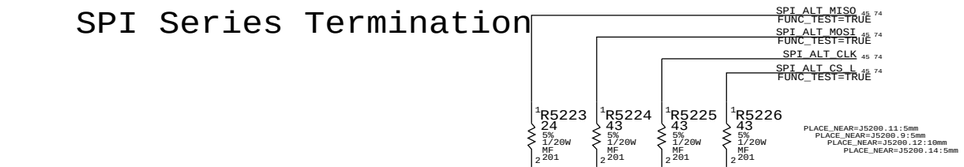
SPI BootROM

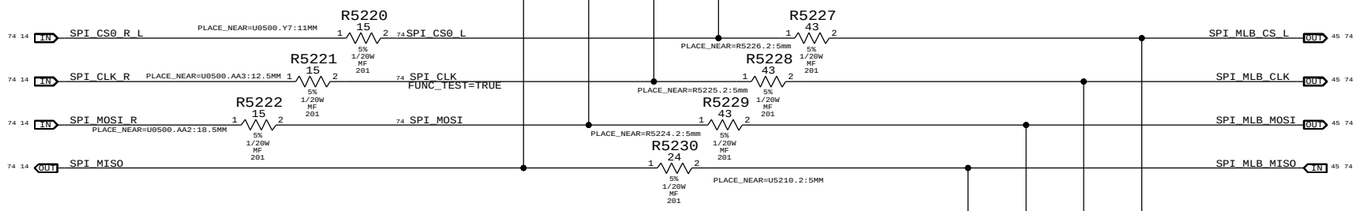


LPC+SPI Connector

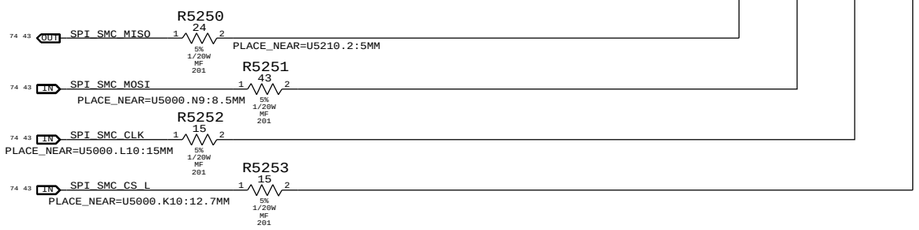


SPI Series Termination





SMC SPI Support



SYNC_MASTER=J70_TONY SYNC_DATE=09/24/2013

PAGE TITLE

SPI and Debug Connector

Apple Inc.

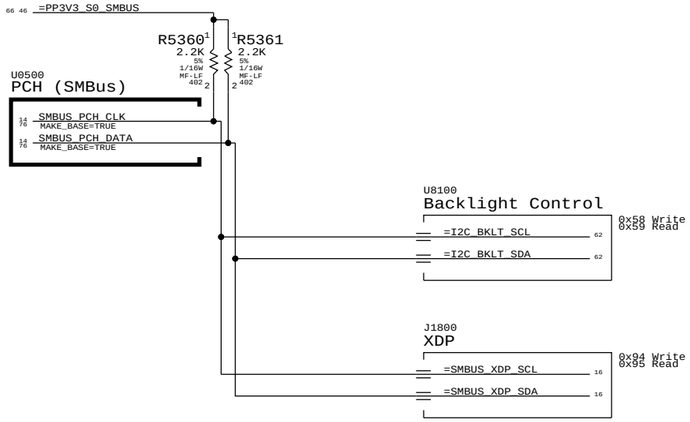
DRAWING NUMBER 051-1407 SIZE D

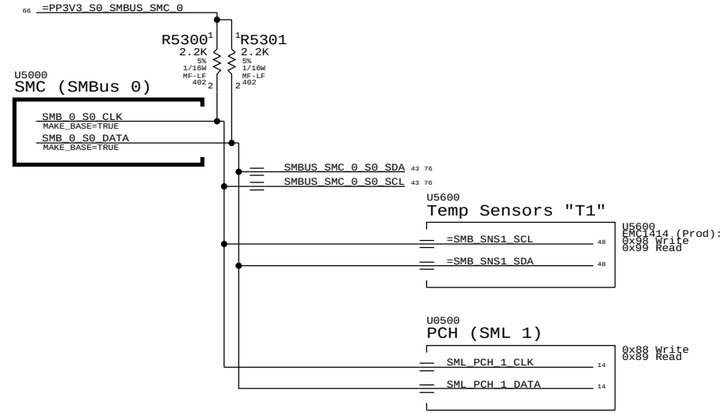
REVISION A.0.0

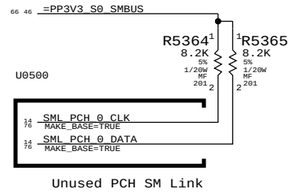
BRANCH

PAGE 52 OF 123

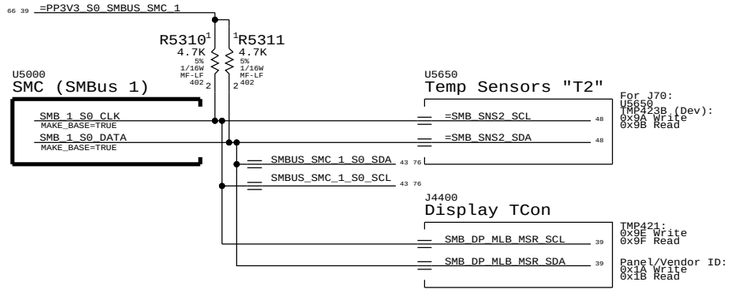
SHEET 45 OF 81

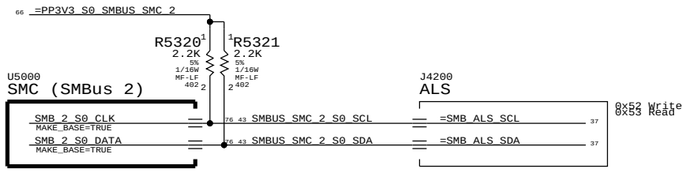


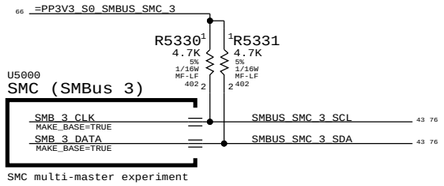




Unused PCH SM Link







SMC multi-master experiment

Line Legend
- Master
- Slave
- Mux

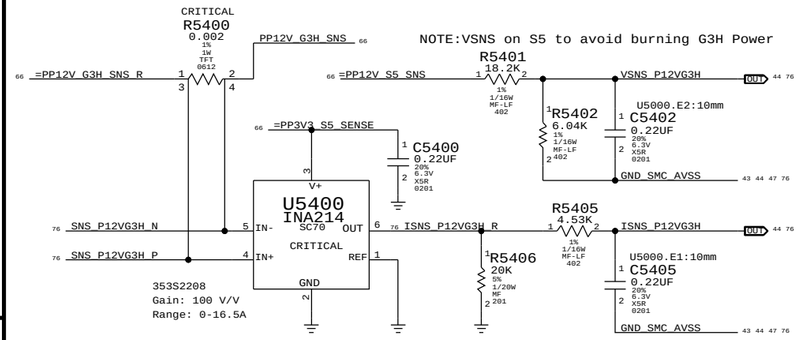
SYNC_MASTER=J70_NICK SYNC_DATE=02/14/2014

PAGE TITLE
SMBus Connections

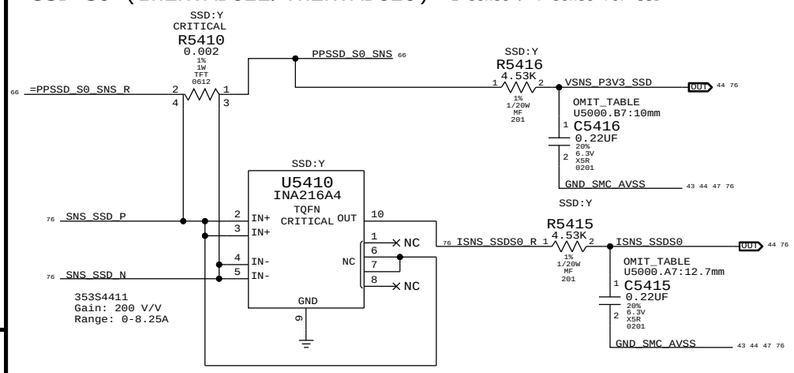
Apple Inc.

DRAWING NUMBER 051-1407
SIZE D
REVISION A.0.0
BRANCH
PAGE 53 OF 123
SHEET 46 OF 81

12V G3H (VD2R:ADC0/ID2R:ADC1) AC/DC lowside sense (System total)



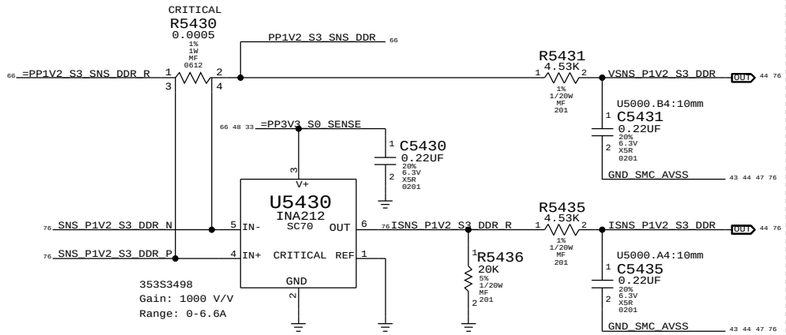
SSD S0 (IH1R:ADC21/VH1R:ADC20) I-sense / V-sense for SSD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5415,C5416	SSD:Y
117S0201	2	RES,0 OHM,201	C5415,C5416	SSD:N

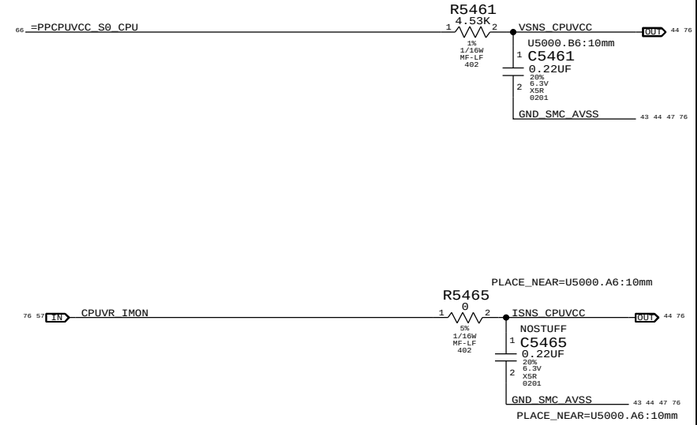
VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for DDR



CPU Core (VC0C:ADC10/IC0C:ADC11)

Voltage sense and IMON amp (VC0C, IC0C)



SYNC_MASTER=J70_NICK SYNC_DATE=11/05/2013

PAGE TITLE: I and V Sense

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

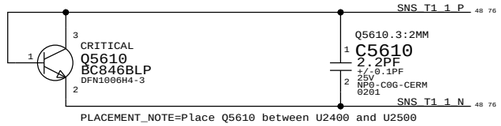
BRANCH:

PAGE: 54 OF 123

SHEET: 47 OF 81

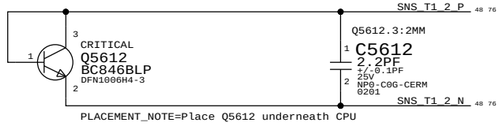
Temperature Sensor T1

LPDDR3 Proximity



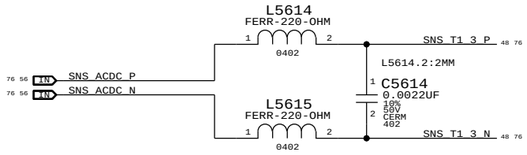
PLACEMENT_NOTE=Place Q5610 between U2400 and U2500

CPU Proximity

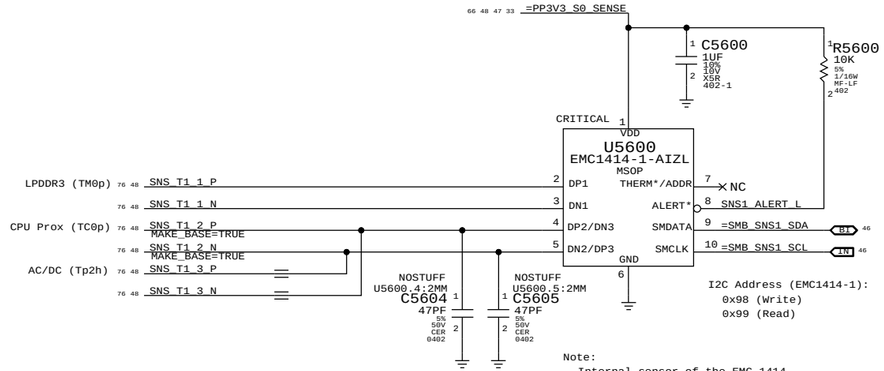


PLACEMENT_NOTE=Place Q5612 underneath CPU

AC/DC Diode on supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

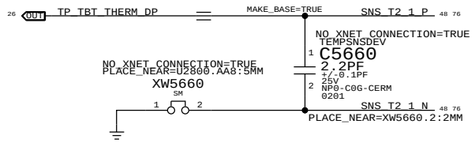


Filter Caps: Stuff if needed for PSU sensor SI

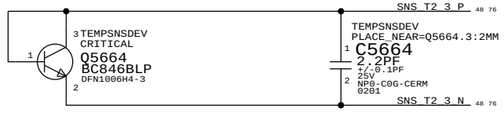
Note:
Internal sensor of the EMC 1414 will be used as the ambient sensor. Place U5600 at the coolest location on the MLB.

Temperature Sensor T2

TBT On Die

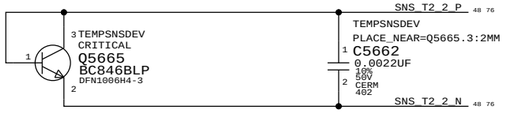


BLC Proximity

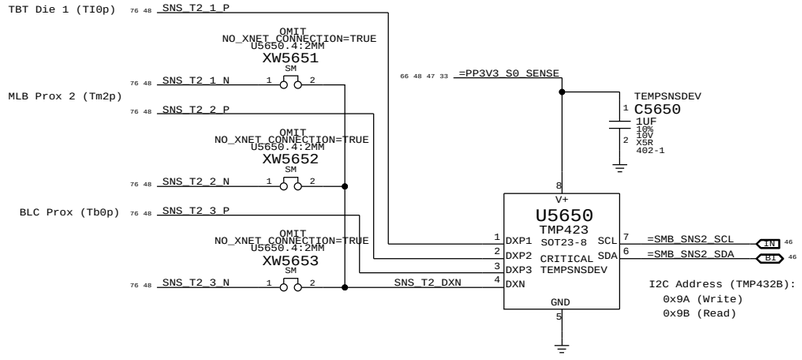


PLACEMENT_NOTE=Place Q5664 near BLC controller

MLB Misc 0



PLACEMENT_NOTE=PLACE Q5665 near CPU



SYNC_MASTER=J70_NICK SYNC_DATE=11/05/2013

PAGE TITLE
Temperature Sensors

Apple Inc.

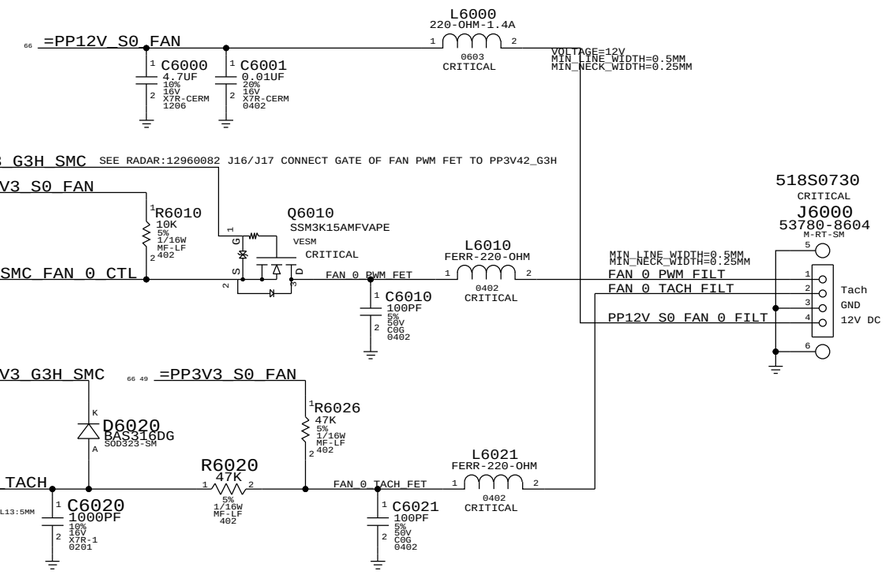
DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 56 OF 123
SHEET 48 OF 81

SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

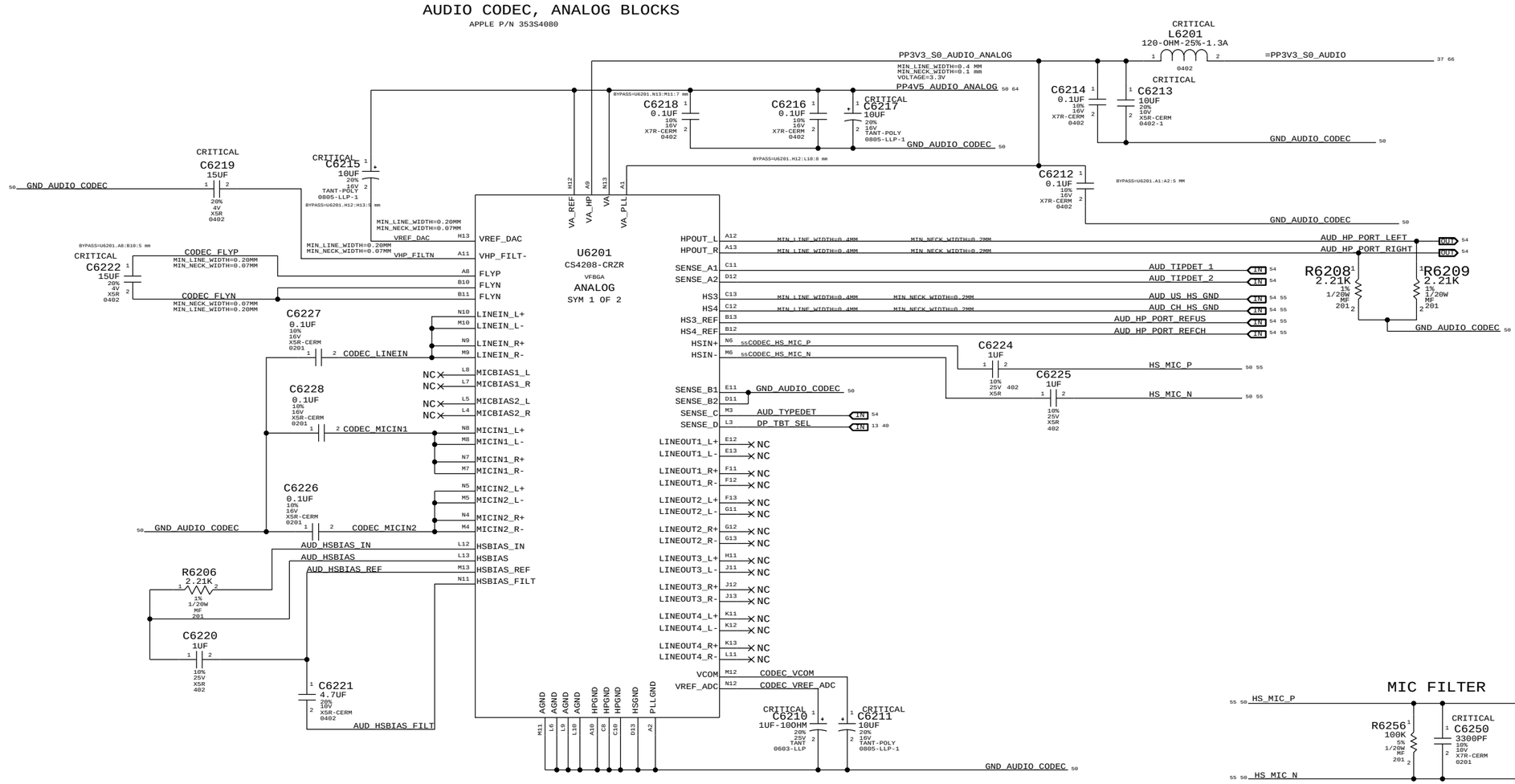
PAGE TITLE
System Fan

Apple Inc.

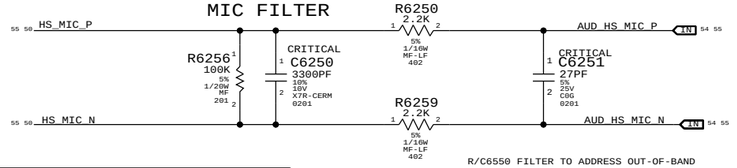
DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 60 OF 123
SHEET 49 OF 81

AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



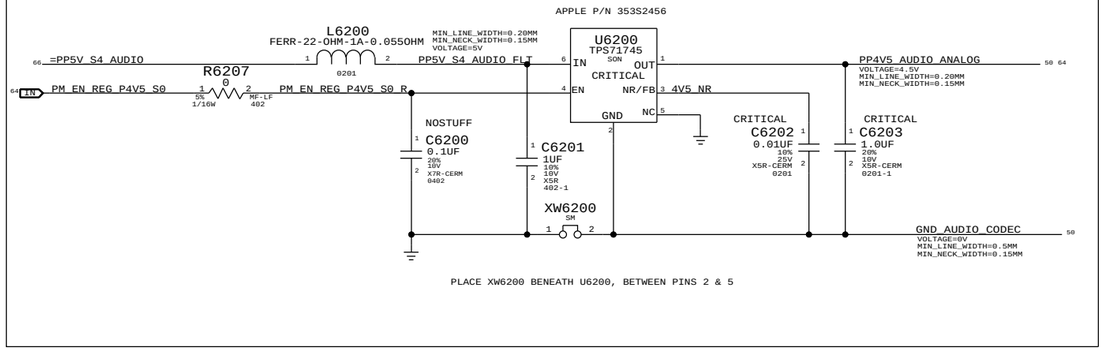
MIC FILTER



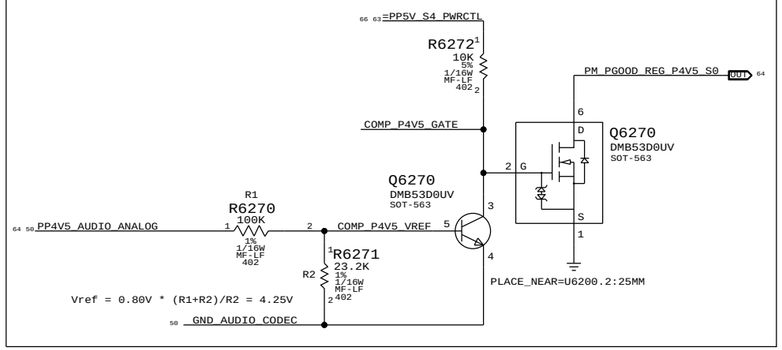
R/C6550 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)

4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



4.5V COMPARATOR



SYNC_MASTER=J70_GAREN SYNC_DATE=12/17/2013

PAGE TITLE: AUDIO:CODEC ANALOG

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

BRANCH

PAGE 62 OF 123

SHEET 50 OF 81

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.055OHM
0201

=PP1V5_S0_AUDIO_DIG
PP1V5_S0_AUDIO_DIG_FILT
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.07MM
VOLTAGE=1.5V

C6300 4.7UF 20% 4V X5R-1 402
C6301 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.J2:J1:13 mm
C6302 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.E1:F1:11 mm

=PP3V3_S0_AUDIO_DIG
BYPASS=U6201.G1:F1:12 mm
C6303 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U6201.K1:K3:6 mm
C6304 0.1UF 10% 6.3V CERM-X5R 0201
C6305 10UF 20% 10V X5R-CERM 0402-1
C6306 10UF 20% 10V X5R-CERM 0402-1
BYPASS=U6201.A7:E3:6 mm
C6307 0.1UF 10% 6.3V CERM-X5R 0201

=PP3V3_S0_AUDIO_DIG
R6358 1K 1% 1/16W MF-LF 402
R6359 1K 1% 1/16W MF-LF 402
R6324 100K 5% 1/20W MF 201
R6325 100K 5% 1/20W MF 201
R6326 47.0K 1% 1/16W MF-LF 402
R6327 47.0K 1% 1/16W MF-LF 402

CODEC_SDA
CODEC_SCL

SPKR_AMP_SD
SPKR_AMP_FAULT
AUD_CONN_SPKR_VENDOR_ID_LEFT
AUD_CONN_SPKR_VENDOR_ID_RIGHT
DFET_OPENUS
DFET_OPENCH

R6340 0 5% 1/20W MF 0201
HDA_BIT_CLK
HDA_BIT_CLK_PORT
R6341 0 5% 1/20W MF 0201
HDA_SYNC
HDA_SYNC_PORT
R6342 22 5% 1/20W MF 201
HDA_SDIN0
CS4208_HDA_SDOUT0_R
TP_CS4208_HDA_SDOUT1
R6343 0 5% 1/20W MF 0201
HDA_SDOUT
HDA_SDOUT_PORT
HDA_RST_L

U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

GPIO0 H3
GPIO1 H2
GPIO2 H1
GPIO3 C4
GPIO4 C5
GPIO5 C7
GP00 C9
GPO1 B9
BCLK F2
SYNC E2
SDI0 D1
SDI1 C1
SDO0 D2
SDO1 C2
SDO2 C3
SDO3 B1
RST* D3
MCLK_A A5
SCLK_A B2
LRCK_A B4
SDOUT_A A3
SDIN_A B3
MCLK_B A6
SCLK_B B6
LRCK_B B5
SDOUT_B B8
SDIN_B A4
SDA C6
SCL B7

VD_J2
VL_HD E1
VL_SP A7
VL_LF G1
VL_DM K1

DGND J1
LGND F1
LGND E3
LGND F3
LGND J3
LGND K3

SPDIF_IN G3
SPDIF_OUT G2
CS4208_SPDIF_IN
CS4208_SPDIF_OUT
DMIC_SDA0 N3
DMIC_SCL0 N2
DMIC_SDA1 N1
DMIC_SCL1 M1
DMIC_SDA2 M2
DMIC_SCL2 L1
DMIC_SDA3 K2
DMIC_SCL3 L2
NC F6
NC F7
NC F8
NC G6
NC G7
NC G8
NC H6
NC H7
NC H8

R6302 0 5% 1/20W MF 0201
DP_INT_SPDIF_AUDIO
R6330 33 5% 1/10W MF-LF 402
SPDIF_OUT_JACK
R6333 0 5% 1/20W MF 0201
DMIC_SDA3_R
DMIC_SDA3
R6332 75 1% 1/10W MF-LF 402
DMIC_CLK3_R
DMIC_CLK3

R6350 33 1% 1/20W MF 201
R6351 33 1% 1/20W MF 201
R6352 33 1% 1/20W MF 201
R6353 33 1% 1/20W MF 201
MCLKA_SPKR_LEFT
SCLKA_SPKR_LEFT
LRCLKA_SPKR_LEFT
SDOUTA_SPKR_LEFT

AUDIO:TDM R6354 33 1% 1/20W MF 201
AUDIO:TDM R6355 33 1% 1/20W MF 201
AUDIO:TDM R6356 33 1% 1/20W MF 201
AUDIO:TDM R6357 33 1% 1/20W MF 201
AUDIO:I2S R6360 33 1% 1/20W MF 201
AUDIO:I2S R6361 33 1% 1/20W MF 201
AUDIO:I2S R6362 33 1% 1/20W MF 201
AUDIO:I2S R6363 33 1% 1/20W MF 201
MCLKB_SPKR_RIGHT
SCLKB_SPKR_RIGHT
LRCLKB_SPKR_RIGHT
SDOUTB_SPKR_RIGHT

MCLKA_SPKR_LEFT_R
SCLKA_SPKR_LEFT_R
LRCLKA_SPKR_LEFT_R
SDOUTA_SPKR_LEFT_R
MCLKB_SPKR_RIGHT_R
SCLKB_SPKR_RIGHT_R
LRCLKB_SPKR_RIGHT_R
SDOUTB_SPKR_RIGHT_R

SYNC_MASTER=J70_GAREN	SYNC_DATE=01/30/2013
PAGE TITLE	AUDIO:CODEC, DIGITAL
Apple Inc.	DRAWING NUMBER 051-1407
	SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 63 OF 123
	SHEET 51 OF 81

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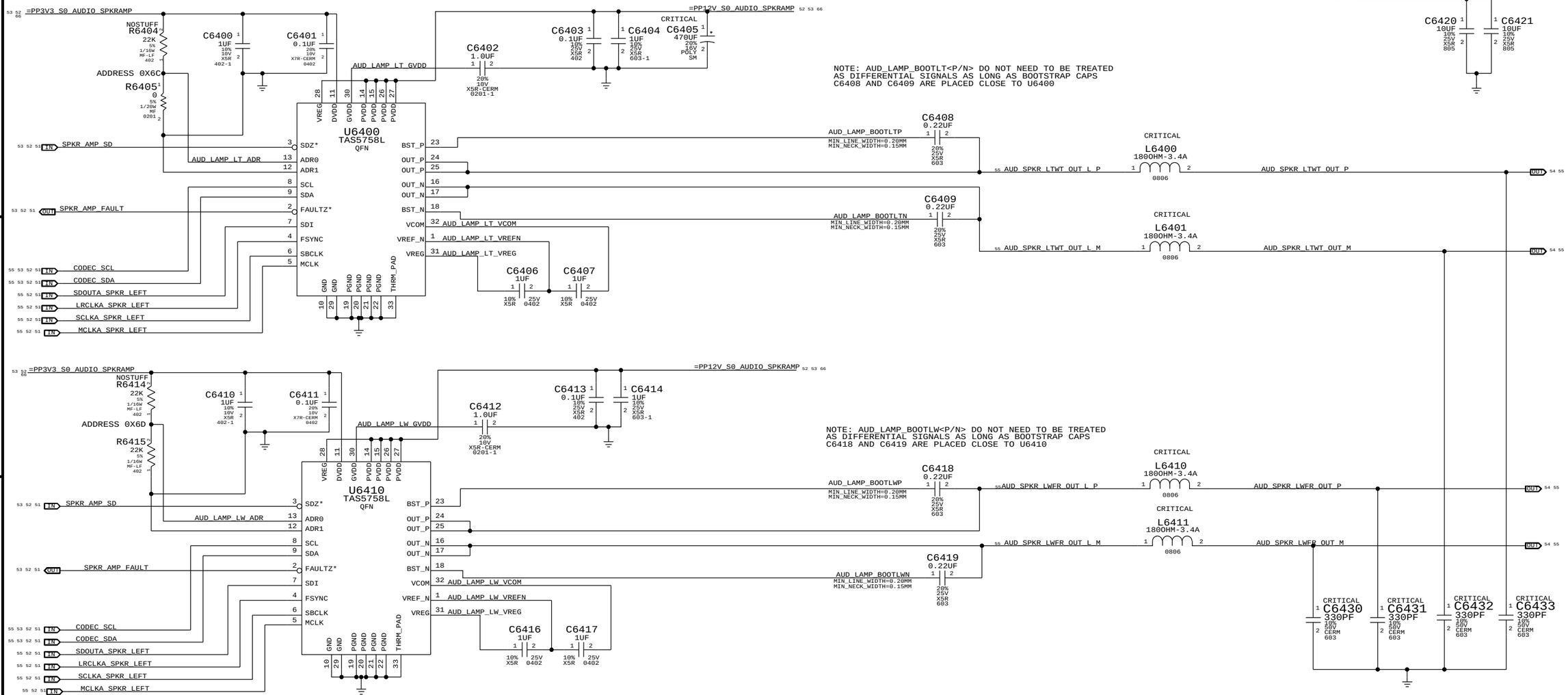
2X MONO SPEAKER AMPLIFIERS (TAS5758L)

APN: TBD

GAIN = TBD

SPEAKER AMPLIFIERS - LEFT CHANNEL



SYNC_MASTER=J70_GAREN SYNC_DATE=03/07/2014

PAGE TITLE

AUDIO: SPEAKER AMP, LEFT CHANNEL

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

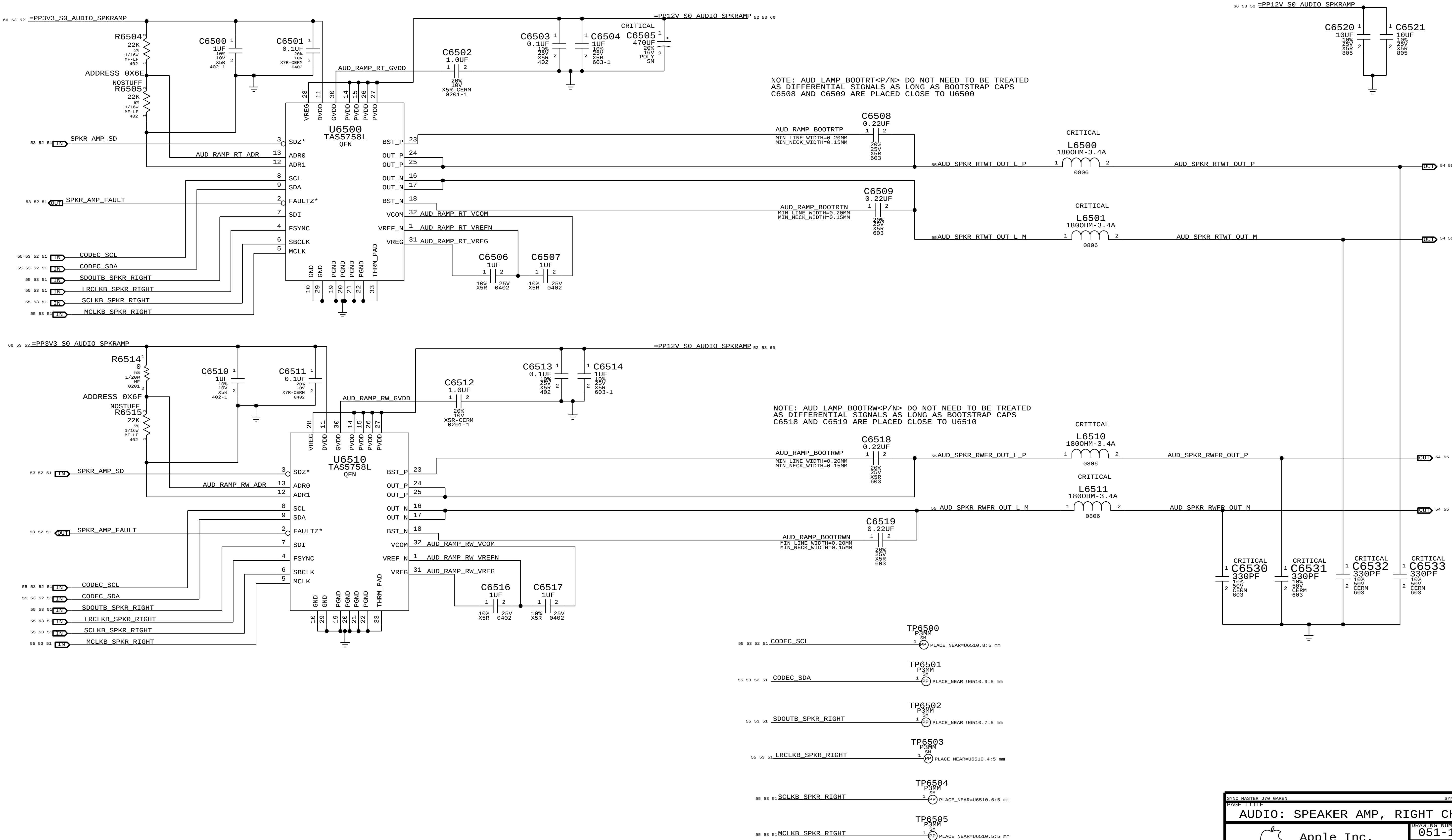
BRANCH

PAGE 64 OF 123

SHEET 52 OF 81

2X MONO SPEAKER AMPLIFIERS (TAS5758L)   APN: TBD   GAIN = TBD

SPEAKER AMPLIFIERS - RIGHT CHANNEL



=PP3V3_S0_AUDIO_SPKRAMP
=PP12V_S0_AUDIO_SPKRAMP
U6500
TAS5758L
QFN
U6510
TAS5758L
QFN
ADDRESS 0X6E
ADDRESS 0X6F
NOSTUFF
R6504 22K
R6505 22K
R6514 0
R6515 22K
C6500 1UF
C6501 0.1UF
C6502 1.0UF
C6503 0.1UF
C6504 1UF
CRITICAL C6505 470UF
C6506 1UF
C6507 1UF
C6508 0.22UF
C6509 0.22UF
C6510 1UF
C6511 0.1UF
C6512 1.0UF
C6513 0.1UF
C6514 1UF
C6516 1UF
C6517 1UF
C6518 0.22UF
C6519 0.22UF
C6520 10UF
C6521 10UF
CRITICAL C6530 330PF
CRITICAL C6531 330PF
CRITICAL C6532 330PF
CRITICAL C6533 330PF
CRITICAL L6500 180OHM-3.4A 0806
CRITICAL L6501 180OHM-3.4A 0806
CRITICAL L6510 180OHM-3.4A 0806
CRITICAL L6511 180OHM-3.4A 0806
SPKR_AMP_SD
SPKR_AMP_FAULT
CODEC_SCL
CODEC_SDA
SDOUTB_SPKR_RIGHT
LRCLKB_SPKR_RIGHT
SCLKB_SPKR_RIGHT
MCLKB_SPKR_RIGHT
AUD_RAMP_RT_GVDD
AUD_RAMP_RT_ADR
AUD_RAMP_RT_VCOM
AUD_RAMP_RT_VREFN
AUD_RAMP_RT_VREG
AUD_RAMP_BOOTRTP
AUD_RAMP_BOOTRTN
AUD_RAMP_RW_GVDD
AUD_RAMP_RW_ADR
AUD_RAMP_RW_VCOM
AUD_RAMP_RW_VREFN
AUD_RAMP_RW_VREG
AUD_RAMP_BOOTRWP
AUD_RAMP_BOOTRWN
MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.15MM
AUD_SPKR_RTWT_OUT_L_P
AUD_SPKR_RTWT_OUT_L_M
AUD_SPKR_RTWT_OUT_P
AUD_SPKR_RTWT_OUT_M
AUD_SPKR_RWFR_OUT_L_P
AUD_SPKR_RWFR_OUT_L_M
AUD_SPKR_RWFR_OUT_P
AUD_SPKR_RWFR_OUT_M
NOTE: AUD_LAMP_BOOTRT<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6508 AND C6509 ARE PLACED CLOSE TO U6500
NOTE: AUD_LAMP_BOOTRW<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6518 AND C6519 ARE PLACED CLOSE TO U6510
TP6500 P3MM SM PLACE_NEAR=U6510.8:5 mm
TP6501 P3MM SM PLACE_NEAR=U6510.9:5 mm
TP6502 P3MM SM PLACE_NEAR=U6510.7:5 mm
TP6503 P3MM SM PLACE_NEAR=U6510.4:5 mm
TP6504 P3MM SM PLACE_NEAR=U6510.6:5 mm
TP6505 P3MM SM PLACE_NEAR=U6510.5:5 mm

SYNC_MASTER=J70_GAREN   SYNC_DATE=03/07/2014

PAGE TITLE

AUDIO: SPEAKER AMP, RIGHT CHANEL

Apple Inc.

DRAWING NUMBER 051-1407   SIZE D

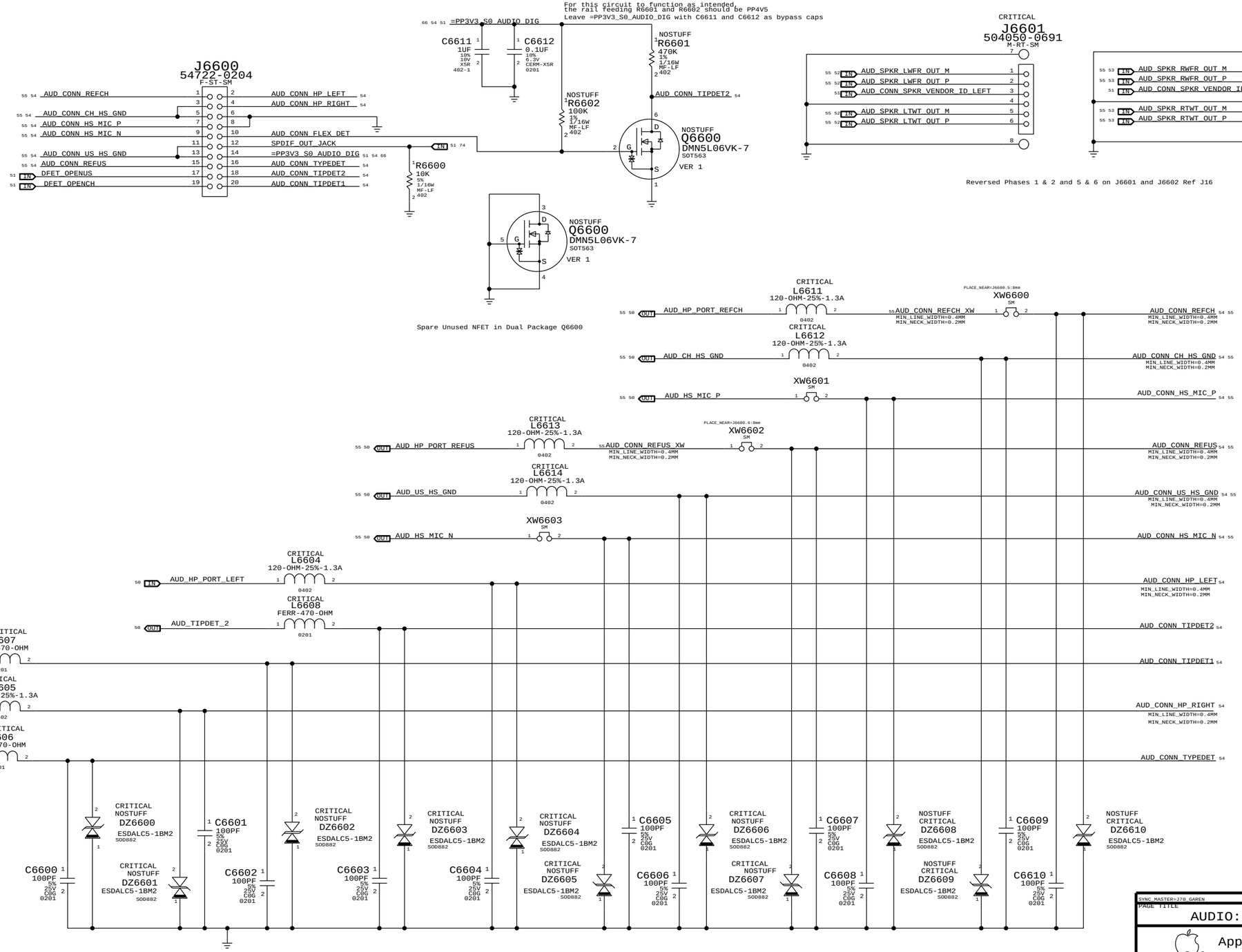
REVISION A.0.0

BRANCH

PAGE 65 OF 123

SHEET 53 OF 81

SPEAKER CONNECTOR



SYNC_MASTER=J70_GAREN SYNC_DATE=03/11/2014

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

BRANCH

PAGE 66 OF 123

SHEET 54 OF 81

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0x12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO_ISO	*	0.1 MM	?
SPKROUT_ISO	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
AUDIODIFF_2MM	*	Y	0.2 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	AUDIO_ISO
SPKROUT	*	*	SPKROUT_ISO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SPEAKER OUTPUTS				
H20 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	53 54
H21 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_M	53 54
H22	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_P	53
H23	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_M	53
H32 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	53 54
H33 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_M	53 54
H35	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_P	53
H34	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_M	53
H37 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	52 54
H38 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_M	52 54
H39	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_P	52
H40	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_M	52
H42 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	52 54
H43 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_M	52 54
H45	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_P	52
H44	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_M	52
HEADSET MIC				
H14 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_CONN_HS_MIC_P	54
H15 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_CONN_HS_MIC_N	54
F25 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	50 54
F25 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	50 54
H12 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_P	50
H13 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_N	50
F16 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CODEC_HS_MIC_P	50
H42 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CODEC_HS_MIC_N	50
H54		AUDIO	AUD_CONN_CH_HS_GND	54
H55		AUDIO	AUD_CONN_US_HS_GND	54
H60		AUDIO	AUD_CH_HS_GND	50 54
H60		AUDIO	AUD_US_HS_GND	50 54
H56		AUDIO	AUD_CONN_REFCH	54
H57		AUDIO	AUD_CONN_REFUS	54
H27		AUDIO	AUD_CONN_REFCH_XW	54
H70		AUDIO	AUD_CONN_REFUS_XW	54
G72		AUDIO	AUD_HP_PORT_REFCH	50 54
G72		AUDIO	AUD_HP_PORT_REFUS	50 54
LINEOUT				
H46	AUDIODIFF	AUDIO	LINEOUT2_LEFT_P	
H47	AUDIODIFF	AUDIO	LINEOUT2_LEFT_N	
H48	AUDIODIFF	AUDIO	LINEOUT2_RIGHT_P	
H49	AUDIODIFF	AUDIO	LINEOUT2_RIGHT_N	
H50	AUDIODIFF	AUDIO	LINEOUT3_LEFT_P	
H51	AUDIODIFF	AUDIO	LINEOUT3_LEFT_N	
H53	AUDIODIFF	AUDIO	LINEOUT3_RIGHT_P	
H52	AUDIODIFF	AUDIO	LINEOUT3_RIGHT_N	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CODEC SCL & SDA				
H58			CODEC_SCL	51 52 53
H59			CODEC_SDA	51 52 53
TDM				
H56		HDA	MCLKA_SPKR_LEFT	51 52
H54		HDA	SCLKA_SPKR_LEFT	51 52
F89		HDA	LRCLKA_SPKR_LEFT	51 52
H55		HDA	SDOUTA_SPKR_LEFT	51 52
H72			MCLKA_SPKR_LEFT_R	51
F72			SCLKA_SPKR_LEFT_R	51
H72			LRCLKA_SPKR_LEFT_R	51
F72			SDOUTA_SPKR_LEFT_R	51
H56		HDA	MCLKB_SPKR_RIGHT	51 53
F89		HDA	SCLKB_SPKR_RIGHT	51 53
H57		HDA	LRCLKB_SPKR_RIGHT	51 53
H56		HDA	SDOUTB_SPKR_RIGHT	51 53
F72			MCLKB_SPKR_RIGHT_R	51
H37			SCLKB_SPKR_RIGHT_R	51
H38			LRCLKB_SPKR_RIGHT_R	51
F88			SDOUTB_SPKR_RIGHT_R	51

SYNC_MASTER=J70 GAREN SYNC_DATE=03/07/2014

PAGE TITLE

AUDIO: Speaker ID

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

BRANCH

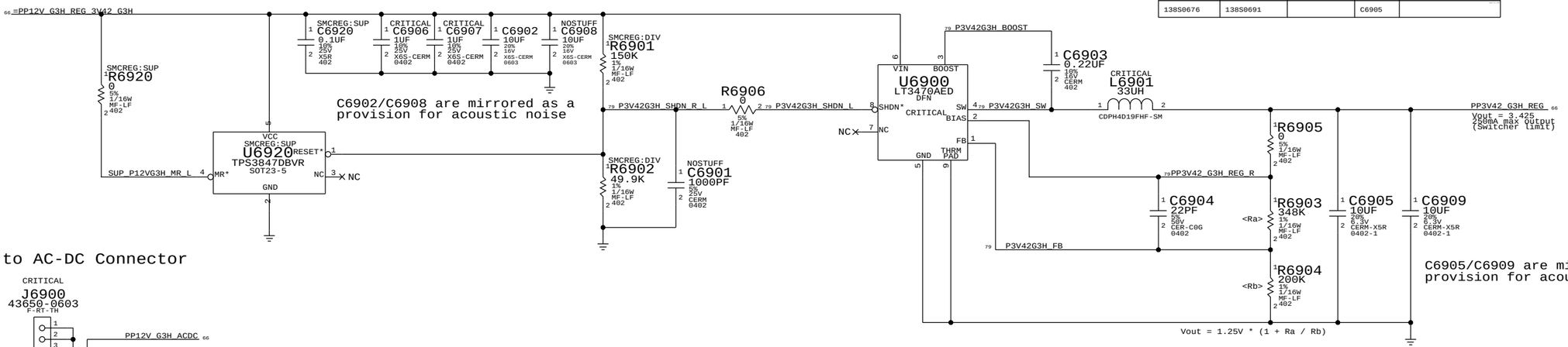
PAGE 68 OF 123

SHEET 55 OF 81

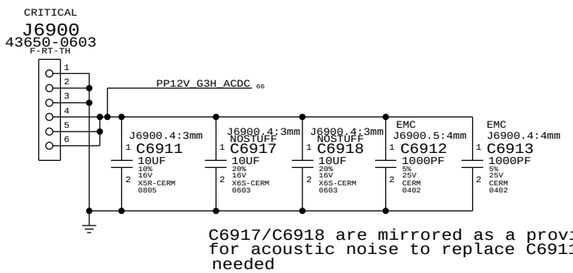
3.425V "G3Hot" Regulator

Switching freq: 409 kHz = $\frac{13.5}{L6901}$

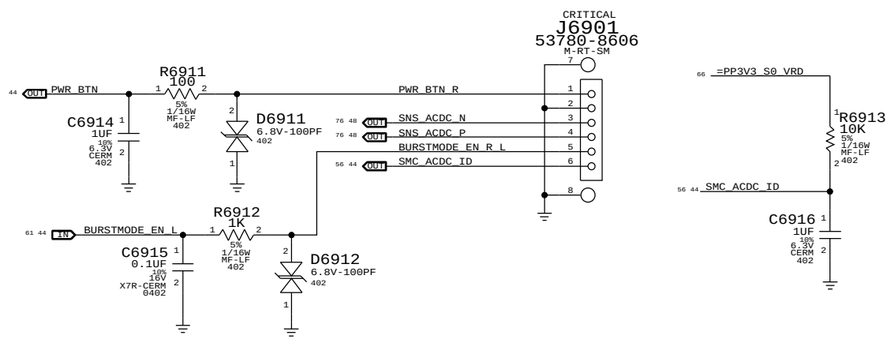
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6905	



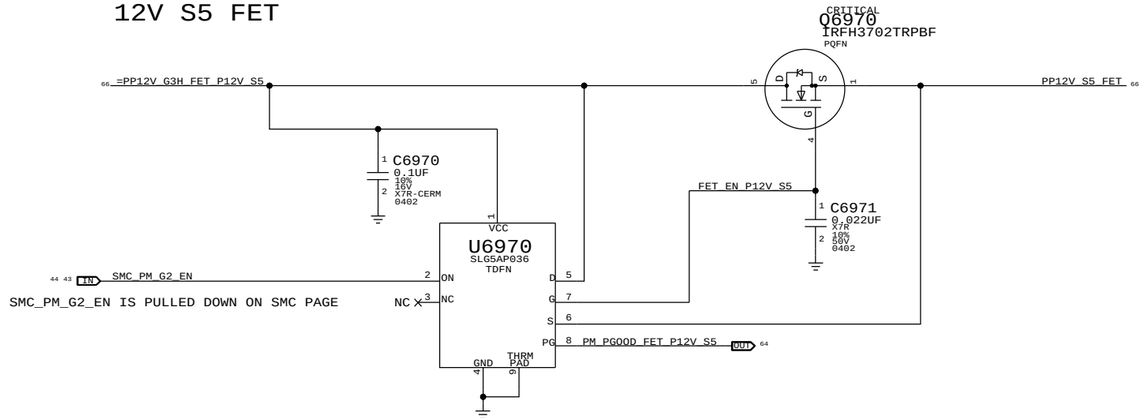
MLB to AC-DC Connector



MLB to AC-DC Supplemental Signal Connector



12V S5 FET



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Power Connectors / VReg G3Hot

Apple Inc.

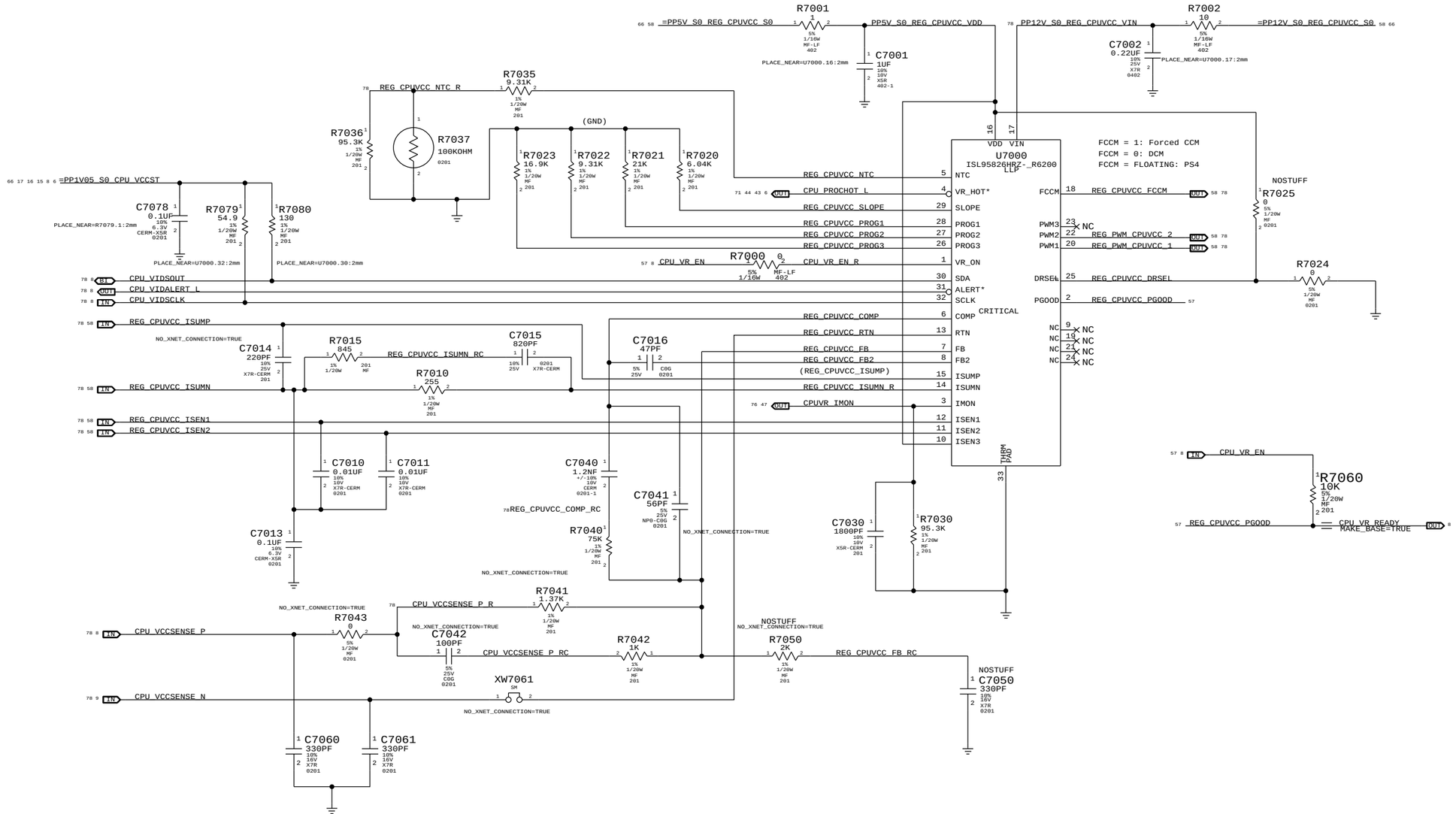
DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

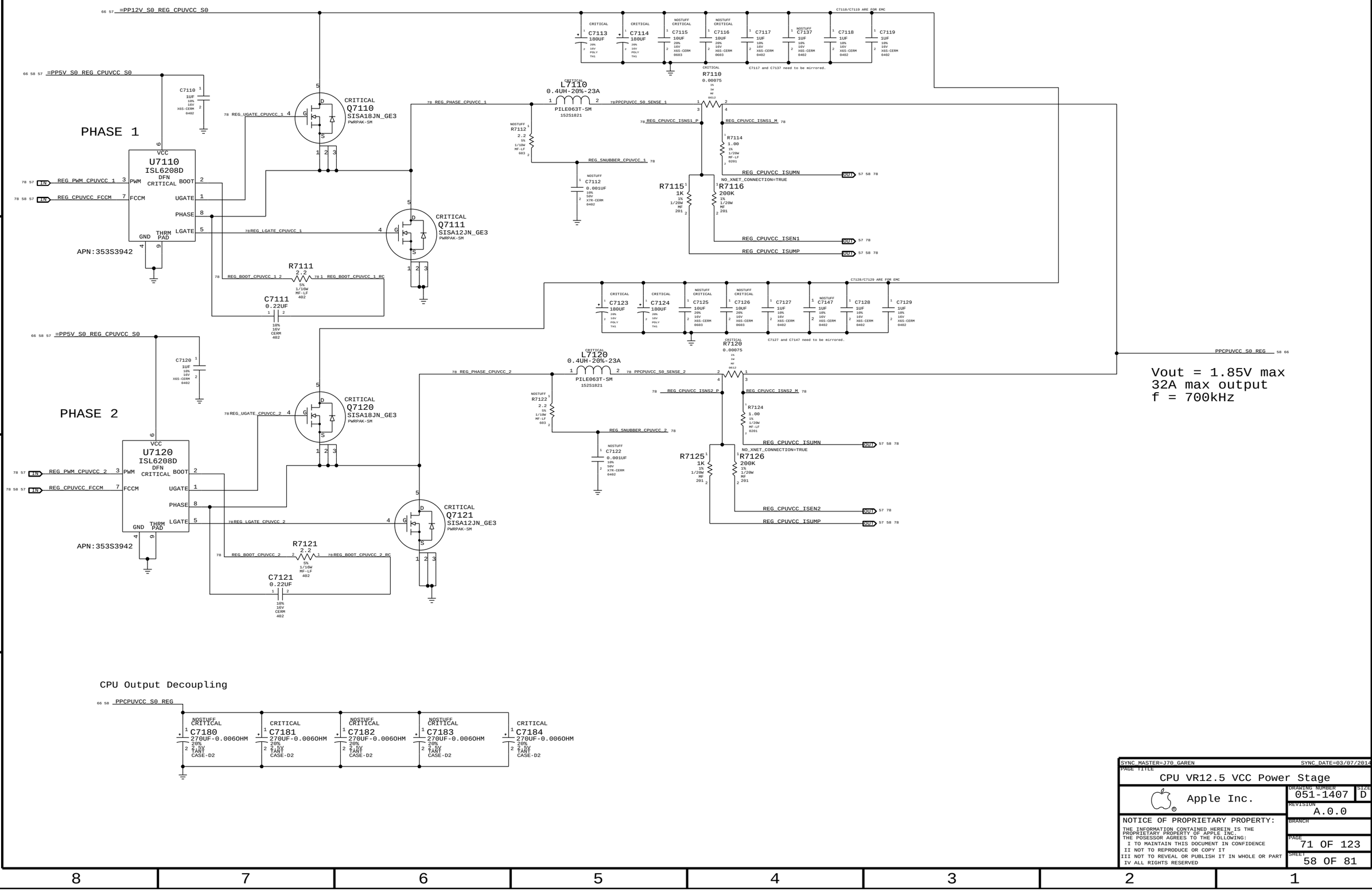
BRANCH:

PAGE: 69 OF 123

SHEET: 56 OF 81



SYNC_MASTER=J70_ROSSANA	SYNC_DATE=09/17/2013
PAGE TITLE	CPU VR12.6 VCC Regulator IC
Apple Inc.	DRAWING NUMBER 051-1407 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 70 OF 123
	SHEET 57 OF 81



SYNC_MASTER=J70_GAREN SYNC_DATE=03/07/2014

PAGE TITLE: CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 71 OF 123

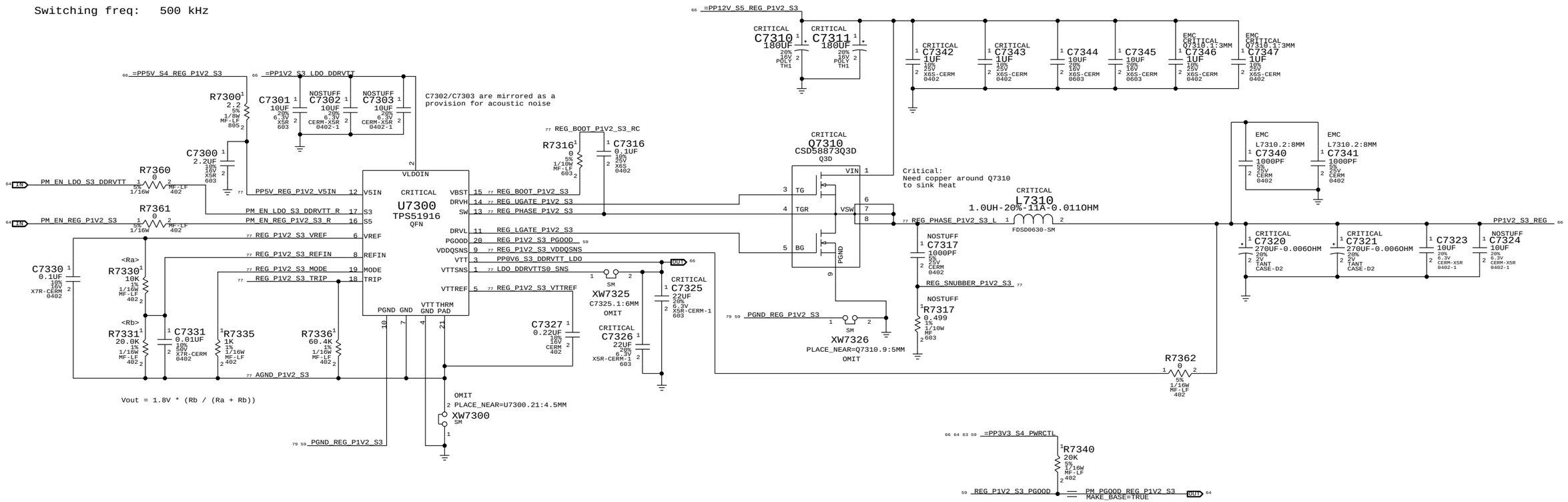
SHEET: 58 OF 81

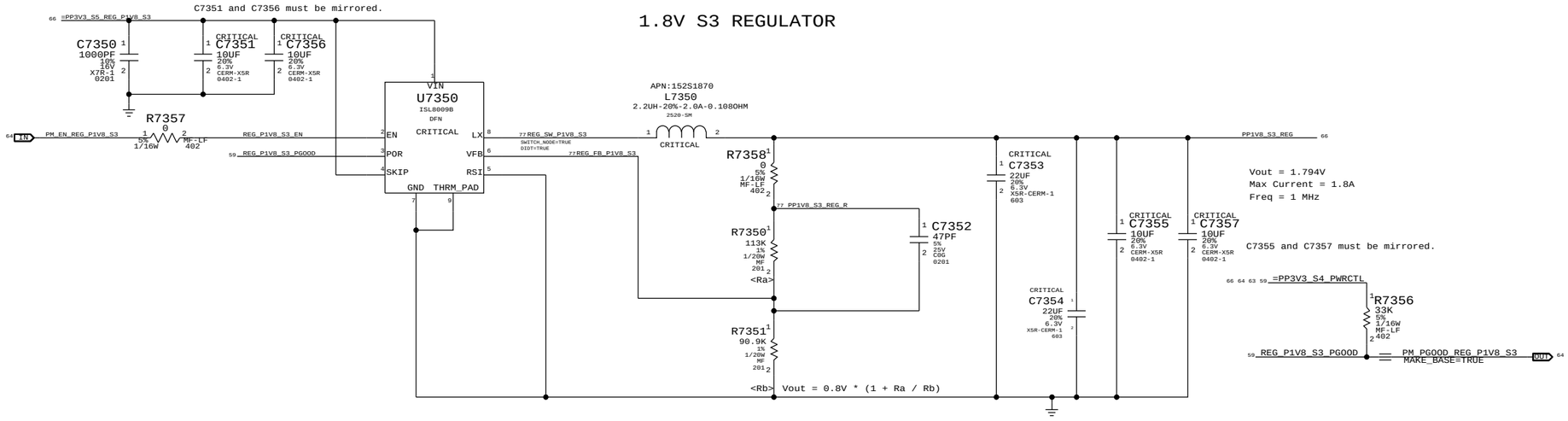
VDDQ 1.2V S3 Regulator

OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5\ *\ Rds(Q7310)} + \frac{0.65625}{L7310\ *\ f(switch)}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz





SYNC_MASTER=J70_ROSSANA SYNC_DATE=09/12/2013

PAGE TITLE: VReg VDDQ S3 / 1.8V S3

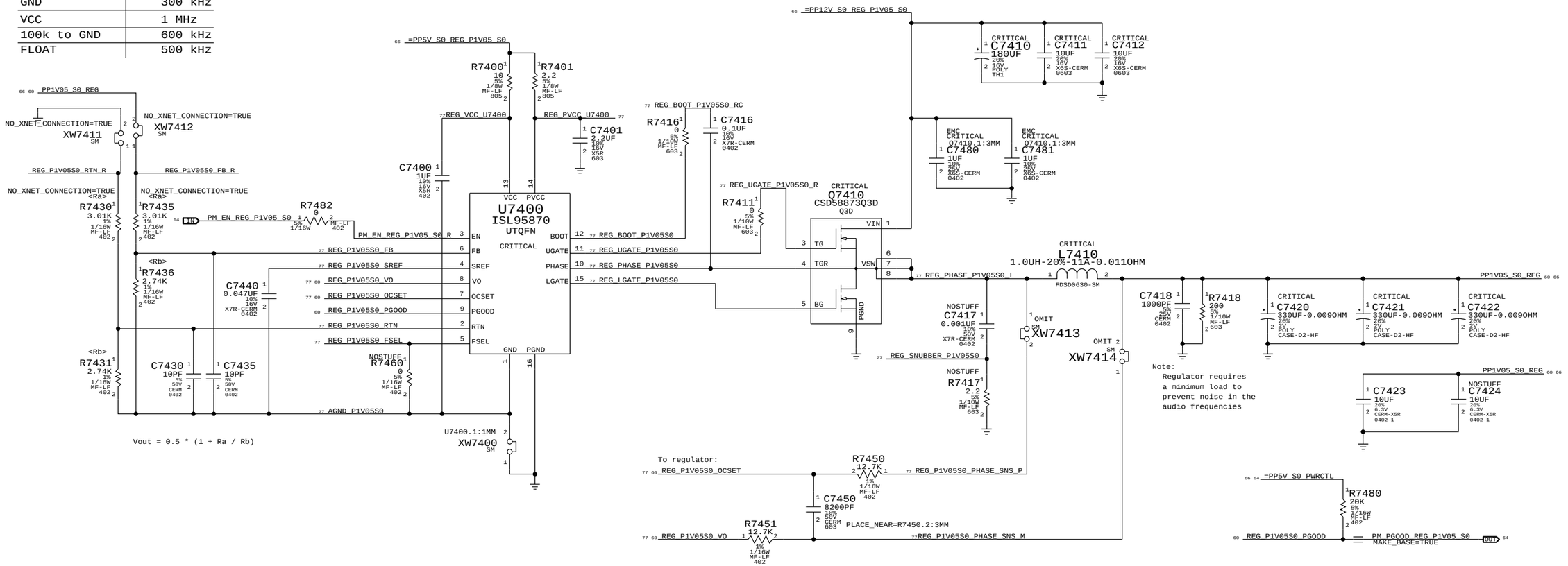
Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 73 OF 123
SHEET: 59 OF 81

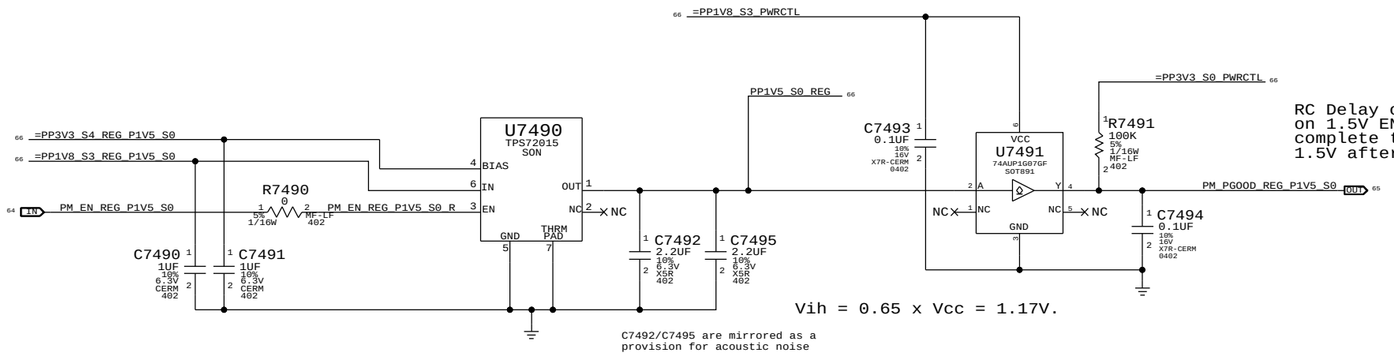
PCH (1.05V) S0 REGULATOR

Switching freq: 500 kHz OC trip point: 12.4 A = $\frac{\text{R7450} * 8.5\ \text{E-6}}{\text{DCR(L7410)}}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



1.5V S0 REGULATOR



RC Delay on 1.5V PGOOD must be longer than delay on 1.5V EN. This allows for rail voltage to complete transition from Vih min (1.17V) to 1.5V after output shifts to OD.

SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE	VREG 1V05 S0 / 1V5 S0
Apple Inc.	DRAWING NUMBER 051-1407 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 74 OF 123
	SHEET 60 OF 81

3.3V S5 Regulator

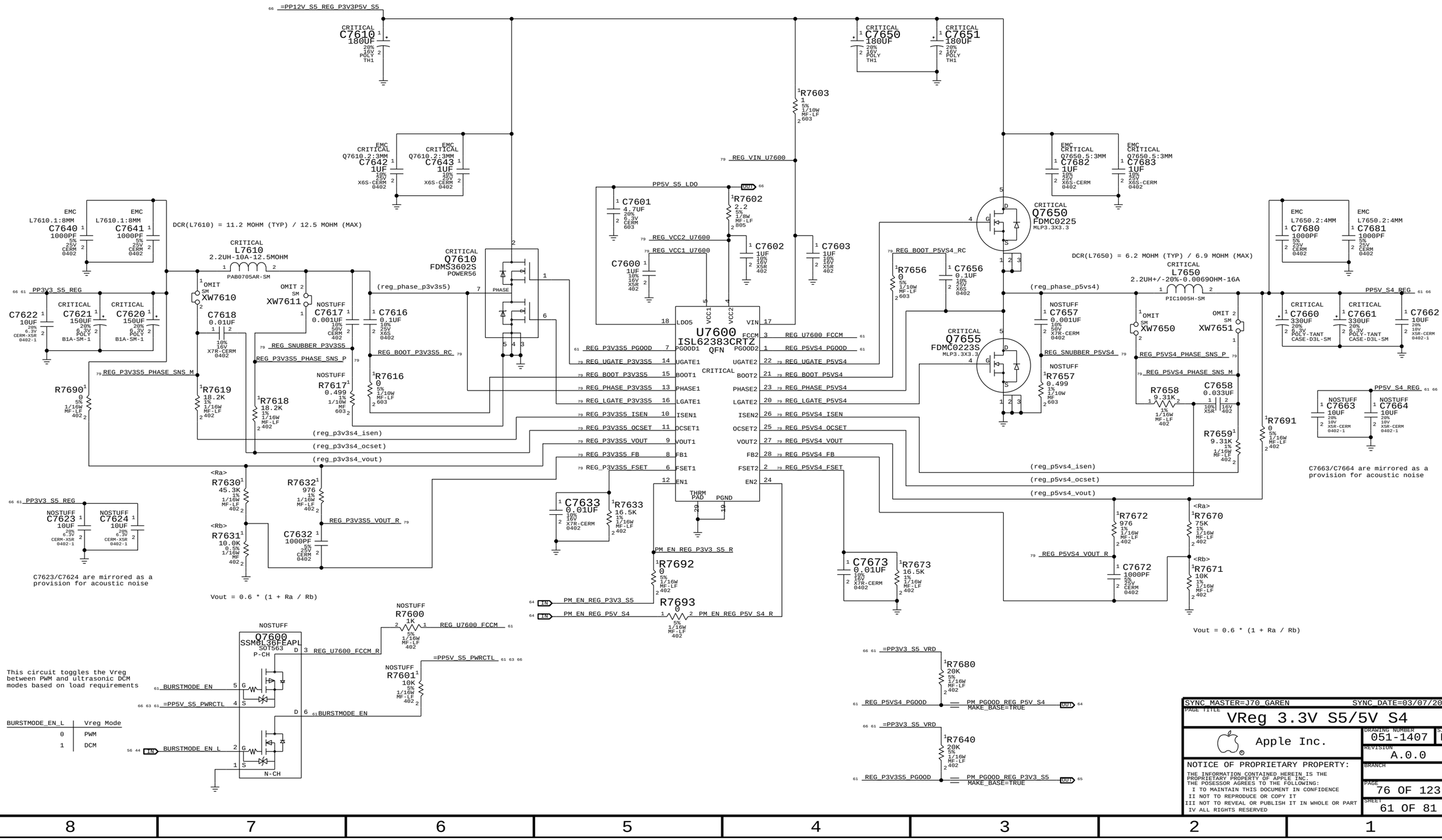
OC trip point: 12.5 A = $\frac{\text{R7618 * 10 E-6}}{\text{DCR(L7610)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7633}}$

5V S4 Regulator

OC trip point: 14.1 A = $\frac{\text{R7658 * 10 E-6}}{\text{DCR(L7650)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7673}}$



SYNC_MASTER=J70_GAREN SYNC_DATE=03/07/2014

PAGE TITLE: VReg 3.3V S5/5V S4

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 76 OF 123

SHEET: 61 OF 81

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0648	371S0694		D8100	BLC Switch Diode

ACOUSTICS E-NOISE COMPONENTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0810	138S1078		2.2UF_CAP	BLC OUTPUT CAPS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0748	371S0731		D8101	INPUT DIODE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1071	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8100 to FB8107

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1116		Q8102	BLC Inrush FET
740S0145	740S0146		F8100	BLC Fuse

SYNC_MASTER=J70_GAREN SYNC_DATE=03/07/2014

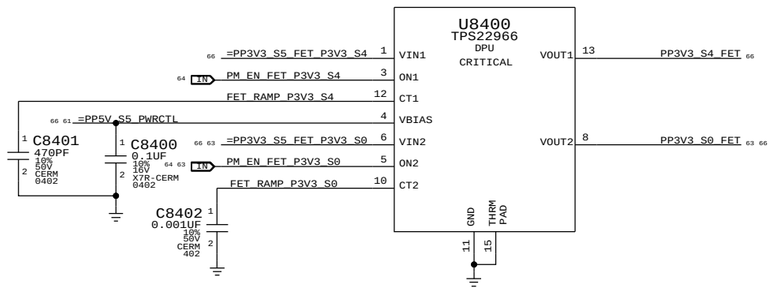
PAGE TITLE

LCD Backlight Driver (LP8561)

Apple Inc.

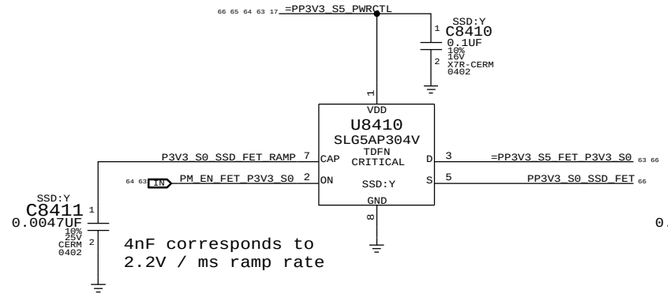
DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 81 OF 123
SHEET 62 OF 81

3.3V S4/S0 FET



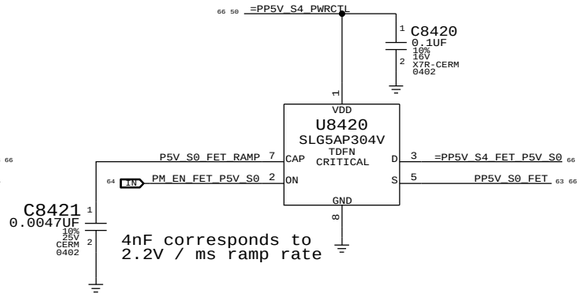
Rise Time For VD = 3.3V:
470 pF -- 603 us
1000 pF -- 1185 us

3V3 S0 SSD



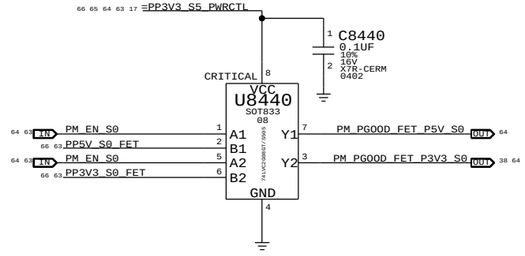
4nF corresponds to
2.2V / ms ramp rate

5V S0 FET

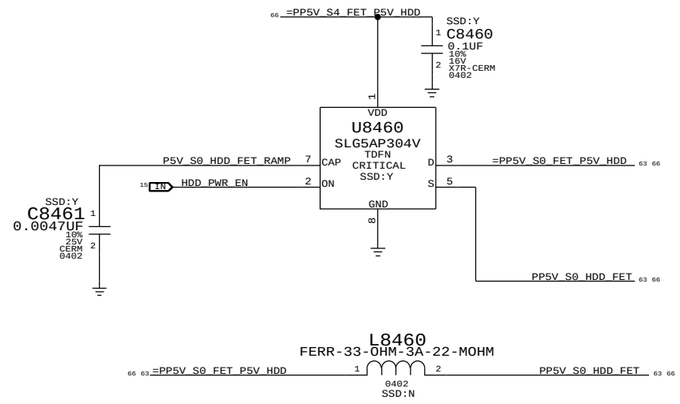


4nF corresponds to
2.2V / ms ramp rate

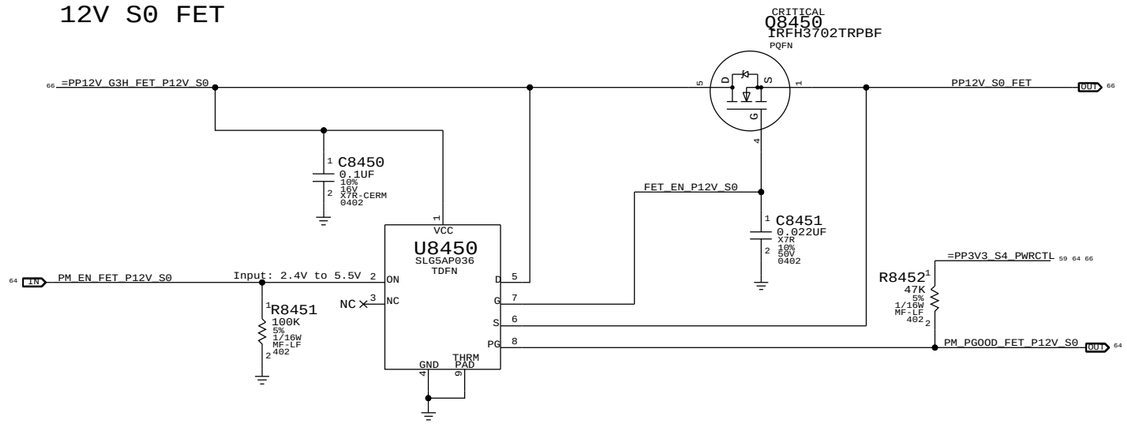
5V / 3V3 S0 PGOODs



5V HDD FET

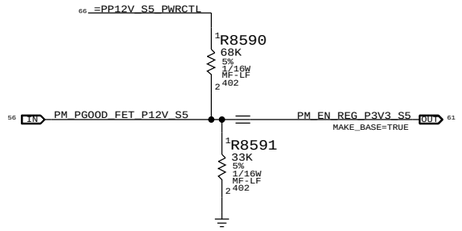


12V S0 FET

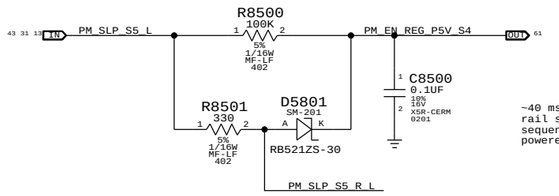


SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE: FET-Controlled S0 and S4	
Apple Inc.	DRAWING NUMBER: 051-1407 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 84 OF 123
	SHEET: 63 OF 81

S5 Enable

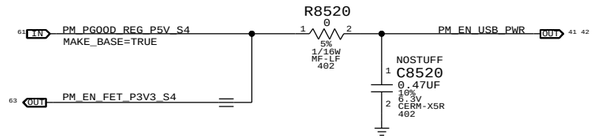


S4 Enables



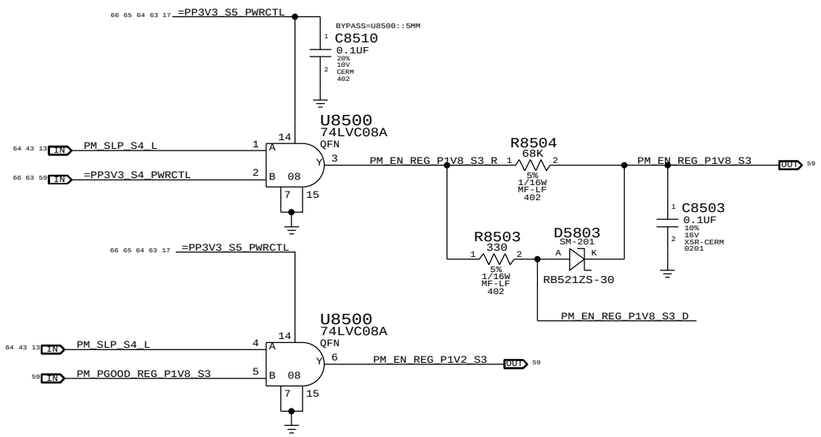
~40 ms RC delay added to ensure that 5V S4 rail stays up at least as long as the S0 sequencing holds in order to keep 5V S0 powered.

S4 USB Enable

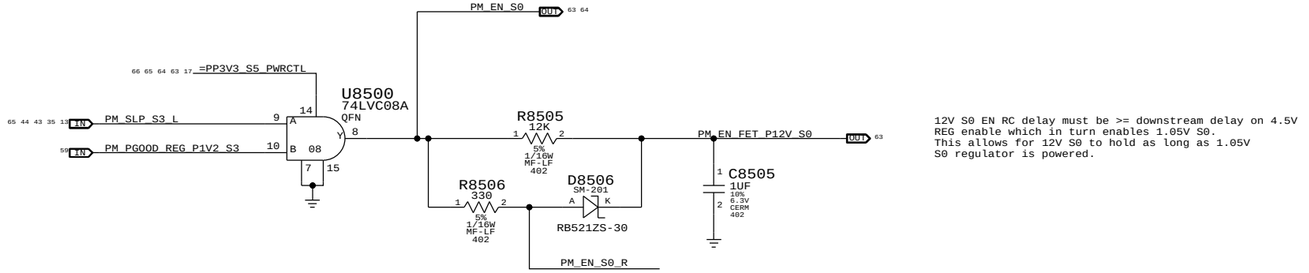


S4 TBT Port Enable

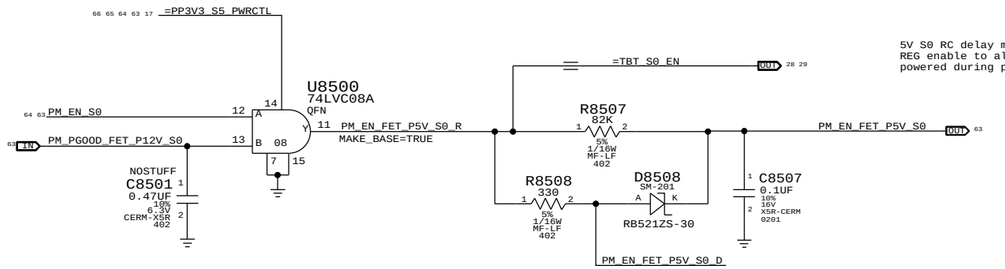
S3 Enables



S0 Enables

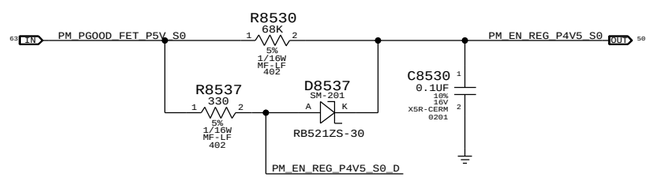


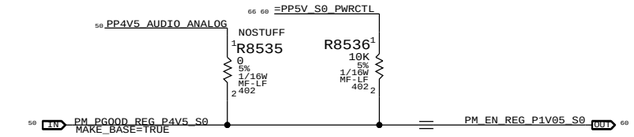
12V S0 EN RC delay must be >= downstream delay on 4.5V REG enable which in turn enables 1.05V S0. This allows for 12V S0 to hold as long as 1.05V S0 regulator is powered.



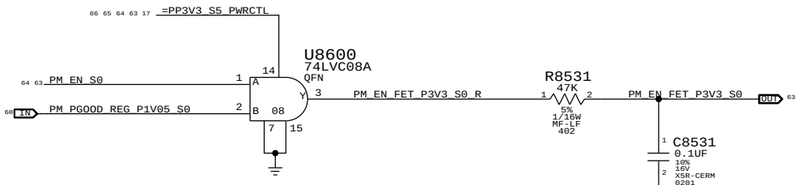
5V S0 RC delay must be >= downstream delay on 4.5V REG enable to allow for 4.5V regulator to remain powered during power down sequence.

Audio + PCH Sequencing Requirements:
4.5V -> 1.05V -> 3.3V -> 1.5V -> ALL SYS GOOD

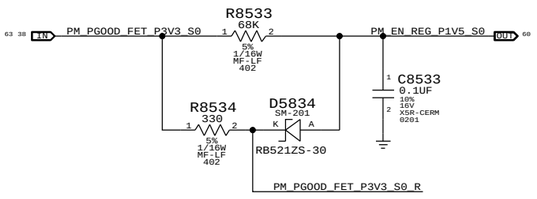




NOSTUFF resistor added in case of using 4.5V rail as the PGOOD itself directly.

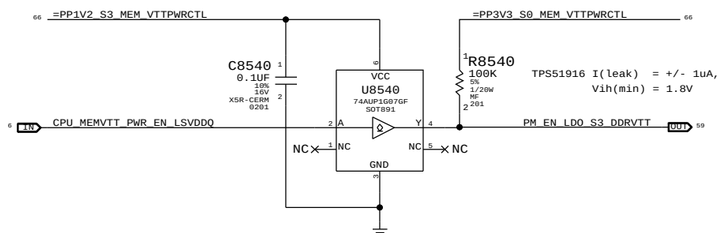


No bypass diode added across 3.3V S0 EN RC delay to mitigate possible glitching from PGOOD pullup to 5V S0 on 1.05V VR page competing with logic turn on time.



Memory VTT Enable Level-Shifter

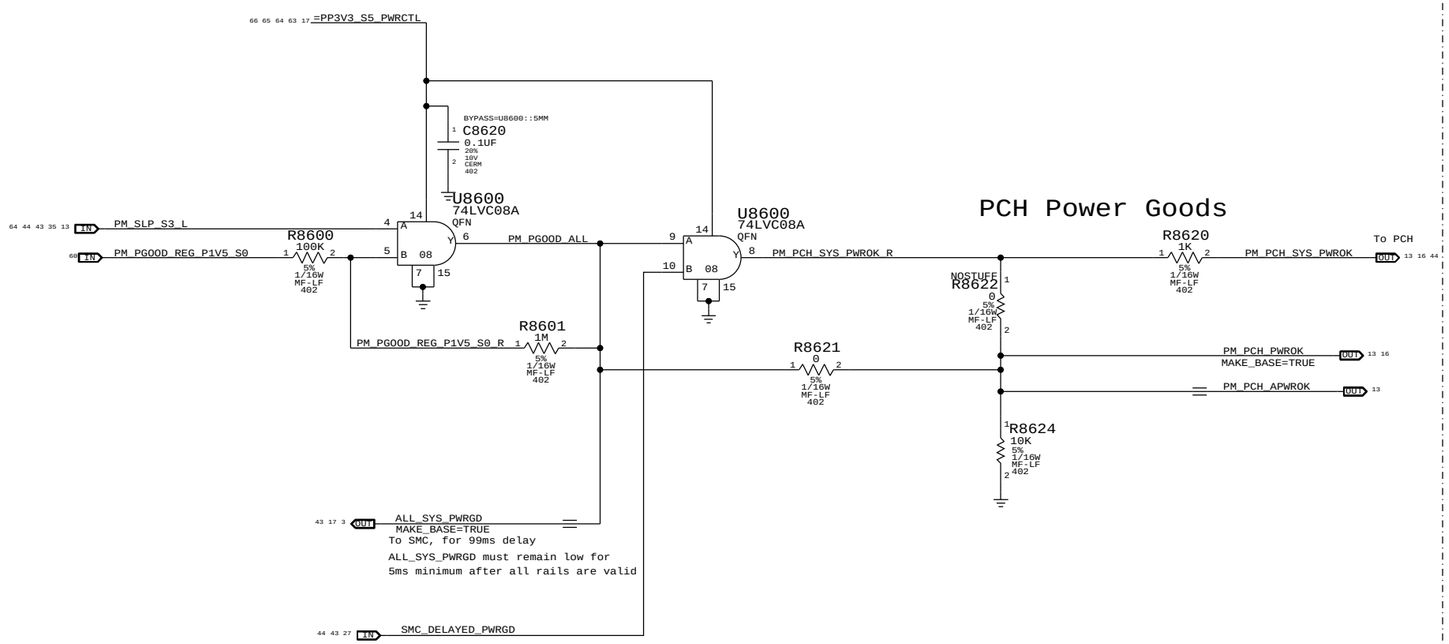
CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).



TPS51916 I(leak) = +/- 1uA,
Vih(min) = 1.8V

SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE: PM Regulator Enables	
Apple Inc.	DRAWING NUMBER: 051-1407 SIZE: D
	REVISION: A.0.0
	BRANCH
	PAGE: 85 OF 123
	SHEET: 64 OF 81

ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation



Resume Reset

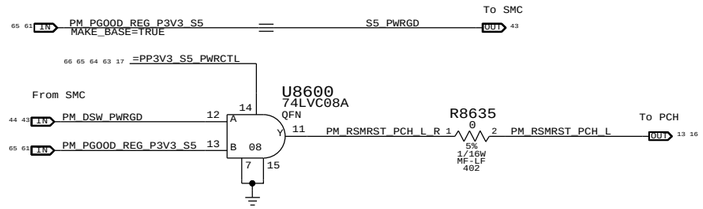
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J70 design does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



Rail definitions

Platform: All processor non-Core and non-Graphics (5V, 3.3V, 1.5V, 1.05V for PCH/TBT/GPU)
Uncore: 1.8V and 1.2V for DDR3

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

SYNC_MASTER=J70_TONY SYNC_DATE=10/10/2013

PAGE TITLE: PM Power Good

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 86 OF 123
SHEET: 65 OF 81

G3 Rails

Always on: Keeps the PCH RTC alive

79 PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC 17
- =PPVRTC_G3_PCH 8 12 13

G3H Rails

79 PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC 56
- =PP12V_G3H_SNS_R 47

79 PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS 47
- =PP12V_G3H_REG_3V42_G3H 56
- =PP12V_G3H_FET_P12V_S5 56
- =PP12V_G3H_FET_P12V_S0 63

79 PP3V42_G3H (MAKE_BASE=TRUE)
- PP3V42_G3H_REG 56
- =PP3V3_G3H_BT 31
- =PP3V3_G3H_SMC 43 44 49
- =PP3V3_G3H_RTC_D 17
- =PPVIN_G3H_SMCVREF 44
- =PP3V3_G3H_SMC_USBMUX 41
- =PP3V3_G3H_LPCPLUS 45

Ground/Common

GND (MAKE_BASE=TRUE)

S5 Rails

Enabled when system has AC and is in S5

79 PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET 56
- =PP12V_S5_REG_P3V3P5V_S5 61
- =PP12V_S5_REG_P1V2_S3 59
- =PPHV_SW_TBTAPWRSW 28
- =PPHV_SW_TBTBPWRSW 29
- =PP12V_S5_SNS 47
- =PP12V_S5_PWRCTL 64

79 PP5V_S5 (MAKE_BASE=TRUE)
- PP5V_S5_LDO 61
- =PP5V_S5_PWRCTL 61 63

79 PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_REG 61
- =PP3V3_S5_FET_P3V3_S4 63
- =PP3V3_S5_FET_P3V3_S0 63
- =PP3V3_S5_PWRCTL 17 63 64 65
- =PP3V3_S5_VRD 61
- =PP3V3_S5_LED 3
- =PP3V3_SUS_PCH_VCCSUS_GPIO 8 11
- =PP3V3_S5_PCH_VCCDSW 8 11
- =PP3V3_SUS_PCH_VCC_SPI 8 11 14
- =PP3V3_SUS_PCH_VCCSUS_RTC 8 11
- =PP3V3_SUS_PCH_VCCSUS_ICC 8
- =PP3V3_S5_ROM 45
- =PP3V3_S5_SENSE 47
- =PP3V3_S5_SMC 44
- =PP3V3_S4_TBTAPWRSW 28
- =PP3V3_S4_TBTBPWRSW 29
- =PP3V3_SUS_PCH_GPIO 14
- =PP3V3_S5_PCH_GPIO 13 15
- =PP3V3_S5_PCH_JTAG 16
- =PP3V3_S5_REG_P1V8_S3 59
- =PP3V3_S5_XDP 16

S4 Rails

Enabled when system has AC and is in run or sleep

79 PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_REG 61
- =PP5V_S4_REG_P1V2_S3 59
- =PP5V_S4_FET_P5V_S0 63
- =PP5V_S4_PWRCTL 50 63
- =PP5V_S4_USB 41 42
- =PP5V_S4_AUDIO 50
- =PP5V_S4_FET_P5V_HDD 63

79 PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET 63
- =PP3V3_S4_FET_ENET 35
- =PP3V3_S4_PWRCTL 59 63 64
- =PP3V3_S4_LED 3
- =PP3V3_S4_PCH_GPIO 15 18
- =PP3V3_S4_SDCARD 36
- =PP3V3_S4_SMC 44
- =PP3V3_S4_TBT 26 27 28 29 64
- =PP3V3_S4_AP 31 44
- =PP3V3_S4_DP 39
- =PP3V3_S4_REG_P1V5_S0 60

S3 Rails

Enabled when system is in run or sleep

79 PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET 35
- =PP3V3_ENET_PHY 34 35

77 PP1V8_S3 (MAKE_BASE=TRUE)
- PP1V8_S3_REG 59
- =PP1V8_S3_DDR 21 22 23 24
- =PP1V8_S3_CAMERA_FET 38
- =PP1V8_S3_PWRCTL 60
- =PP1V8_S3_REG_P1V5_S0 60

77 PP1V2_S3 (MAKE_BASE=TRUE)
- PP1V2_S3_REG 59
- =PP1V2_S3_SNS_DDR_R 47

77 PP1V2_S3_DDR (MAKE_BASE=TRUE)
- PP1V2_S3_SNS_DDR 47
- =PP1V2_S3_LDO_DDRVTT 59
- =PP1V2_S3_DDR_MEMVREF 20
- =PP1V2_S3_DDR_VDD2 21 22 23 24
- =PP1V2_S3_DDR_VDDCA 21 22 23 24
- =PP1V2_S3_DDR_VDDQ 21 22 23 24
- =PP1V2_S3_MEM_VTTPWRCTL 64
- =PPVMEMIO_S0_CPU 8 10
- =PP1V2_S3_CAMERA_FET 38

77 PP0V6_S3_DDRVTT (MAKE_BASE=TRUE)
- PP0V6_S3_DDRVTT_LDO 59
- =PP0V6_S3_DDRVTT_A 25
- =PP0V6_S3_DDRVTT_B 25

S0 Rails

Enabled when system is in run

79 PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET 63
- =PP12V_S0_REG_CPUVCC_S0 57 58
- =PP12V_S0_REG_P1V05_S0 60
- =PP12V_S0_AUDIO_SPKRAMP 52 53
- =PP12V_S0_BKLT 62
- =PP12V_S0_FAN 49
- =PP12V_S0_LCD 39

79 PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET 63
- =PP5V_S0_REG_CPUVCC_S0 57 58
- =PP5V_S0_REG_P1V05_S0 60
- =PP5V_S0_LPCPLUS 45
- =PP5V_S0_BKLT 62
- =PP5V_S0_FET_P5V_HDD 63
- =PP5V_S0_CAMERA 37 38
- =PP5V_S0_PCH_STRAP 17
- =PP5V_S0_PWRCTL 60 64

79 PP5V_S0_HDD (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET 63
- =PP5V_S0_SATA 33

79 PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET 63
- =PP3V3_S0_VRD 56
- =PP3V3_S0_AUDIO 37 50
- =PP3V3_S0_AUDIO_DIG 51 54
- =PP3V3_S0_AUDIO_SPKRAMP 52 53
- =PP3V3_S0_DP 30 39
- =PP3V3_S0_ENET 34
- =PP3V3_S0_FAN 49
- =PP3V3_S0_INTDPMUX 40
- =PP3V3_S0_LED 3
- =PP3V3_S0_LED_SATA 32
- =PP3V3_S0_PCH 17
- =PP3V3_S0_PCH_VCC3_3_GPIO 8 11
- =PP3V3_S0_PCH_VCCTS 8 11
- =PP3V3_S0_PCH_VCCSDIO 8 11
- =PP3V3_S0_CAMPWREN 15
- =PP3V3_S0_SDCARD 36
- =PP3V3_S0_SENSE 33 47 48
- =PP3V3_S0_SMBUS 46
- =PP3V3_S0_SMBUS_SMC_0 46
- =PP3V3_S0_SMBUS_SMC_1 39 46
- =PP3V3_S0_SMBUS_SMC_2 46
- =PP3V3_S0_SMBUS_SMC_3 46
- =PP3V3_S0_SMC 44
- =PP3V3_S0_BKLT_VDDIO 62
- =PP3V3_S0_PCH_GPIO 12 13 15 16 27
- =PP3V3_S0_CAMERA 37 38
- =PP3V3_S0_ALS 37
- =PP3V3_S0_MEM_VTTPWRCTL 64
- =PP3V3_S0_PWRCTL 60

79 PP3V3_S0_SSD (MAKE_BASE=TRUE)
- PP3V3_S0_SSD_FET 63
- =PPSSD_S0_SNS_R 47

79 PPSSD_S0 (MAKE_BASE=TRUE)
- PPSSD_S0_SNS 47
- =PPSSD_S0_CONN 32

79 PP1V5_S0 (MAKE_BASE=TRUE)
- PP1V5_S0_REG 60
- =PP1V5_S0_SENSE 33
- =PP1V5_S0_PCH_VCCTS 8
- =PP1V5_S0_AUDIO_DIG 51
- =PP1V5_S0_PCH_VCCSUSHDA 8 11 17

77 PP1V05_S0 (MAKE_BASE=TRUE)
- PP1V05_S0_REG 60
- =PP1V05_S0_PCH_VCC 8 11
- =PP1V05_S0_PCH_VCCASW 8 11
- =PP1V05_S0_PCH_VCCCLK 8 11
- =PP1V05_S0_PCH_VCCIO_USB2 8 11
- =PP1V05_S0_PCH_VCCHSIO 8 11
- =PP1V05_S0_PCH_VCCIO_HSIO 8
- =PP1V05_S0_PCH_PLLFILTERS 11
- =PP1V05_S0_SMC 44
- =PP1V05_S0_XDP 16
- =PP1V05_S0_CPU_VCCST 6 8 15 16 17 57
- =PP1V05_S0_PCH_VCCPLL_HSIO 11

78 PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)
- PPCPUVCC_S0_REG 58
- =PPCPUVCC_S0_CPU 47
- =PPVCC_S0_CPU 8 10

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Power Aliases

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 100 OF 123
SHEET: 66 OF 81

PCH Miscellaneous

12 TP_HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=TRUE

12 TP_PCIE_CLK100M_CAMERAP — NC_PCIE_CLK100M_CAMERAP
MAKE_BASE=TRUE NO_TEST=TRUE

12 TP_PCIE_CLK100M_CAMERAN — NC_PCIE_CLK100M_CAMERAN
MAKE_BASE=TRUE NO_TEST=TRUE

12 TP_PCIE_CLK100M_FWP — NC_PCIE_CLK100M_FWP
MAKE_BASE=TRUE NO_TEST=TRUE

12 TP_PCIE_CLK100M_FWN — NC_PCIE_CLK100M_FWN
MAKE_BASE=TRUE NO_TEST=TRUE

Unused Thunderbolt Aliases

26 TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE
Unused Signal Aliases

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DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 104 OF 123
SHEET 67 OF 81

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE

Functional / ICT Test

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DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

BRANCH

PAGE 105 OF 123

SHEET 68 OF 81

J70 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	0.145 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.092 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.150 MM	0.076 MM	=STANDARD	0.120 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.174 MM	0.085 MM	=STANDARD	0.120 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	*	Y	0.141 MM	0.076 MM	=STANDARD	0.130 MM	0.1 MM
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.120 MM	0.076 MM	=STANDARD	0.140 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.108 MM	0.076 MM	=STANDARD	0.150 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.099 MM	0.076 MM	=STANDARD	0.170 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.085 MM	=STANDARD	0.175 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.076 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.085 MM	=STANDARD	0.210 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.070 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

Top	Signal	1/3 OZ (CU PLATED)	
	Prepreg	0.070 MM	
2	Plane	1/3 OZ (CU PLATED)	
	Prepreg	0.070 MM	
3	Signal	0.5 OZ	
	Prepreg	0.435 MM	
4	Plane	1 OZ	
	Core	0.152 MM	
5	Plane	1 OZ	
	Prepreg	0.435 MM	
6	Signal	0.5 OZ	
	Prepreg	0.070 MM	
2	Plane	1/3 OZ (CU PLATED)	
	Prepreg	0.070 MM	
Btm	Signal	1/3 OZ (CU PLATED)	

SYNC_MASTER=J70_NICK SYNC_DATE=09/12/2013

PAGE TITLE: J70 RULE DEFINITIONS

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DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 110 OF 123

SHEET: 69 OF 81

DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
DDR_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_70D
DDR_CTRL_PHY	*	DDR_40S
DDR_CMD_PHY	*	DDR_40S
DDR_DQ_PHY	*	DDR_40S
DDR_DQS_PHY	*	DDR_70D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=4:1_SPACING	?
DDR_STROBE_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.381 MM	?

Main Segment Min Spacing Rules (mils) (HSW U/Y PDG, Intel Doc# 502636)

Table	Trace	Design	Iso	Design	Comments
6-14	4	(diff)	16	19.69	CLK trace spacing controlled by =70_OHM_DIFF.
6-14	7.5	7.87	12	13.78	
6-14	7.5	7.87	12	13.78	
6-14	7.5	7.87	16	11.81	DQ to other signals not in the same bytelane (but not ch)
			12	11.81	DQS to other signals of the same channel
			7.5	7.87	DQ to DQ in the same bytelane of the same channel
			12	11.81	DQ to DQS in the same bytelane of the same channel
			16	11.81	DQ or DQS in different bytelanes of the same channel
			?	25.59	DQ or DQS in different channels. ISO RULE NOT IN PDG
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_STROBE_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_STROBE_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
U17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<0>	7 21 25
U17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<0>	7 21 25
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1>	7 22 25
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1>	7 22 25
T26 DDR_A_CS0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<0>	7 21 22 25
T18 DDR_A_CS1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1>	7 21 22 25
T18 DDR_A_ODT	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<0>	7 21 22 25
T18 DDR_A_CKE0	DDR_CMD_PHY	DDR_CMD	MEM_A_CKE<1..0>	7 21 25
T24 DDR_A_CKE1	DDR_CMD_PHY	DDR_CMD	MEM_A_CKE<3..2>	7 22 25
T18 DDR_A_CMD0	DDR_CMD_PHY	DDR_CMD	MEM_A_CAA<15..0>	7 21 25
T18 DDR_A_CMD1	DDR_CMD_PHY	DDR_CMD	MEM_A_CAB<15..0>	7 22 25
T18 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	7 19
T18 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	7 19
T19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	7 19
T19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	7 19
T17 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	7 19
T17 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	7 19
T19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	7 19
T19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	7 19
T18 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	7 19
T18 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	7 19
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	7 19
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	7 19
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	7 19
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	7 19
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	7 19
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	7 19
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	7 19
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	7 19
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	7 19
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	7 19
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	7 19
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	7 19
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	7 19
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	7 19
Channel B				
T17 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<0>	7 23 25
T17 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<0>	7 23 25
T26 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1>	7 24 25
T26 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1>	7 24 25
T26 DDR_B_CS0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<0>	7 23 24 25
T21 DDR_B_CS1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1>	7 23 24 25
T21 DDR_B_ODT	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<0>	7 23 24 25
T21 DDR_B_CKE0	DDR_CMD_PHY	DDR_CMD	MEM_B_CKE<1..0>	7 23 25
T25 DDR_B_CKE1	DDR_CMD_PHY	DDR_CMD	MEM_B_CKE<3..2>	7 24 25
T17 DDR_B_CMD0	DDR_CMD_PHY	DDR_CMD	MEM_B_CAA<15..0>	7 23 25
T21 DDR_B_CMD1	DDR_CMD_PHY	DDR_CMD	MEM_B_CAB<15..0>	7 24 25
T22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	7 19
T22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	7 19
T22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	7 19
T22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	7 19
T22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	7 19
T22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	7 19
T22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	7 19
T22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	7 19
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	7 19
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	7 19
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	7 19
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	7 19
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	7 19
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	7 19
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	7 19
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	7 19
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	7 19
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	7 19
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	7 19
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	7 19
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	7 19
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	7 19
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	7 19
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	7 19
SM COMP				
T25	DDR_COMP_PHY	DDR_COMP	CPU_SM_RCOMP<0..2>	6

SYNC_MASTER=J70_NICK SYNC_DATE=09/30/2013

PAGE TITLE: DDR3 Constraints

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 111 OF 123
SHEET: 70 OF 81

PCI Express

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP
CPU_ASYNC_PHY	*	CPU_50S

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?
CPU_ASYNC_ISO	*	=3:1_SPACING	?
CPU_MS_ISO	TOP,BOTTOM	=4.5:1_SPACING	?
CPU_MS_ISO	*	=3:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
CPU_ASYNC	*	*	CPU_ASYNC_ISO
CPU_ASYNC_MS	*	*	CPU_MS_ISO

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

CPU ASYNCHRONOUS

Electrical Contraint Set	Physical	Spacing		
U67	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L	6 43 44 57
U67	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L	6
U67 PECI	CPU_ASYNC_PHY	CPU_ASYNC_MS	CPU_PECI	6 44
U67	CPU_ASYNC_PHY	CPU_ASYNC_MS	SMC_PECI_L	43 44
U67	CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERR_L	6 44
U67	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD	6
U68	CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L	15 44
U68	CPU_ASYNC_PHY	CPU_ASYNC	CPU_VCCST_PWRGD	8 16 17
U68	CPU_ASYNC_PHY	CPU_ASYNC	XDP_CPU_VCCST_PWRGD	16
U68	CPU_ASYNC_PHY	CPU_ASYNC	PLT_RESET_L	13 15 16 18
U68 XDP_BPM_L	CPU_ASYNC_PHY	CPU_ASYNC	XDP_BPM_L<1..0>	6 16

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
CPU OPI Compensation				
U67	COMP_PCIE_PHY	COMP_PCIE	CPU_OPI_RCOMP	6
CPU eDP Compensation				
U67	COMP_PCIE_PHY	COMP_PCIE	MCP_EDP_RCOMP	5
U67	COMP_PCIE_PHY	COMP_PCIE	CPU_CFG_RCOMP	6

SYNC_MASTER=J70_NICK SYNC_DATE=09/12/2013

PAGE TITLE: CPU CONSTRAINTS

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 112 OF 123

SHEET: 71 OF 81

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=5X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
1436 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	12 26
1434 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	12 26
1432 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<2..0>	26
1433 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<2..0>	26
1429	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<2..0>	14 26
1431	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<2..0>	14 26
1427 PCIE_GEN2_R2D_RVSD	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3>	26
1428 PCIE_GEN2_R2D_RVSD	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3>	26
1426	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3>	14 26
1424	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3>	14 26
1423 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<0>	14 26
1421 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<0>	14 26
1419	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<0>	26
1420	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<0>	26
1422 PCIE_GEN2_D2R_RVSD	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<2..1>	14 26
1424 PCIE_GEN2_D2R_RVSD	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<2..1>	14 26
1418	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<2..1>	26
1416	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<2..1>	26
1417 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3>	14 26
1415 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3>	14 26
1414	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3>	26
1412	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3>	26
x1 AirPort				
1440 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	31
1441 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	31
1442	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	14 31
1443	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	14 31
1444 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	14 31
1445 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	14 31
1438 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	12 31
1439 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	12 31
x1 Caesar IV				
1446 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	34
1447 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	34
1448	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	14 34
1449	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	14 34
1450 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	14 34
1451 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	14 34
1452	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	34
1453	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	34
1435 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	12 34
1437 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	12 34
x2 SSD				
1377 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	12 32
1379 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	12 32
PCH PCIE Compensation				
1470	COMP_PCIE_PHY	COMP_PCIE	PCH_PCIE_RCOMP	14

SYNC_MASTER=J70_DINI SYNC_DATE=10/28/2013

PAGE TITLE
PCH PCIe/DMI Constaints

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 113 OF 123
SHEET 72 OF 81

SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	SATA_50S
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
I90 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_P	32
I92 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_N	32
I89	SATA_PHY_90	SATA	SATA_HDD_R2D_C_P	12 32
I91	SATA_PHY_90	SATA	SATA_HDD_R2D_C_N	12 32
I84 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_P	12 32
I85 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_N	12 32
I81	SATA_PHY_90	SATA	SATA_HDD_D2R_C_P	32
I83	SATA_PHY_90	SATA	SATA_HDD_D2R_C_N	32
PCH SATA Port 1 (SSD)				
I96 SATA_SSD_R2D	SATA_PHY	SATA	PCIE_SSD_R2D_P<0..1>	12 32
I98 SATA_SSD_R2D	SATA_PHY	SATA	PCIE_SSD_R2D_N<0..1>	12 32
H114 SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_P<0..1>	32
H116 SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_N<0..1>	32
H103 SATA_SSD_D2R	SATA_PHY	SATA	PCIE_SSD_D2R_P<0..1>	12 32
H102 SATA_SSD_D2R	SATA_PHY	SATA	PCIE_SSD_D2R_N<0..1>	12 32
PCH SATA Compensation				
H104	COMP_SATA_PHY	COMP_SATA	PCH_SATA_RCOMP	12

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
I37 XDP_BPM_L	XDP_PHY	XDP	XDP_BPM_L<7..2>	6 16
I38 XDP_CPU_CFG_PD	XDP_PHY	XDP	CPU_CFG<0>	6 16
I152 XDP_CPU_CFG1_PD	XDP_PHY	XDP	CPU_CFG<1>	6 16
I153 XDP_CPU_CFG	XDP_PHY	XDP	CPU_CFG<2>	6 16
I154 XDP_CPU_CFG3	XDP_PHY	XDP	CPU_CFG<3>	6 16
I155 XDP_CPU_CFG_PD	XDP_PHY	XDP	CPU_CFG<4>	6 16
I156 XDP_CPU_CFG	XDP_PHY	XDP	CPU_CFG<7..5>	6 16
I157 XDP_CPU_CFG_PD	XDP_PHY	XDP	CPU_CFG<10..8>	6 16
I158 XDP_CPU_CFG	XDP_PHY	XDP	CPU_CFG<19..11>	6 16
I45 XDP_CPU_TCK	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	6 16
I46 XDP_CPU_TMS	XDP_PHY	XDP	XDP_CPU_TMS	6 16
I47	XDP_PHY	XDP	XDP_CPU_TDI	6 16
I48	XDP_PHY	XDP	XDP_CPU_TDO	6 16
I44 XDP_CPU_TRST_L	XDP_PHY	XDP	XDP_CPU_TRST_L	6 16
PCH XDP				
I49	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	12 16
I50	XDP_PHY	XDP	XDP_PCH_TMS	12 16
I51	XDP_PHY	XDP	XDP_PCH_TDI	12 16
I52	XDP_PHY	XDP	XDP_PCH_TDO	12 16

SYNC_MASTER=J70_TONY SYNC_DATE=10/23/2013

PAGE TITLE
SATA/FDI/XDP Constraints

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 114 OF 123
SHEET 73 OF 81

PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH_ISO	*	=4:1_SPACING	?
COMP_PCH_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCH	*	*	CLK_PCH_ISO
COMP_PCH	*	*	COMP_PCH_ISO

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC_ISO	*	=1.5:1_SPACING	?
CLK_LPC_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LPC	*	*	LPC_ISO
CLK_LPC	*	*	CLK_LPC_ISO

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA_ISO	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	HDA_ISO

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL_ISO	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XTAL	*	*	XTAL_ISO

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
H33C	LPC_55S	LPC	LPC_AD<3..0>	14 43 45
H33D	LPC_55S	LPC	LPC_AD_R<3..0>	14
H33E	LPC_55S	LPC	LPC_FRAME_L	14 43 45
H33F	LPC_55S	LPC	LPC_FRAME_R_L	14
LPC Clocks				
H33G	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_LPCPLUS	17 45
H44C	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	12 17
H34J	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_SMC	17 43
H34K	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_SMC_R	12 17

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
T41F	CLK_XTAL	XTAL	PCH_CLK24M_XTALIN	12 17
T41G	CLK_XTAL	XTAL	PCH_CLK24M_XTALOUT	12 17
T43G	CLK_XTAL	XTAL	PCH_CLK24M_XTALOUT_R	17
PCH RTC 32K				
H44J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	12 17
H44H	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	12 17
H45Y	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	17
SMC 32K				
H24C	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	13 44
F45C	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	43 44

25 MHz XTALS

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
H42C	CLK_XTAL	XTAL	TBT_CLK25M_IN	26
H43C	CLK_XTAL	XTAL	TBT_CLK25M_OUT	26
H43D	CLK_XTAL	XTAL	TBT_CLK25M_OUT_R	26
F43C	CLK_XTAL	XTAL	ENET_XTAL_IN	34
H43C	CLK_XTAL	XTAL	ENET_XTAL_OUT	34
H43D	CLK_XTAL	XTAL	ENET_XTAL_OUT_R	34

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
H43G HDA_CLK	HDA_55S	HDA	HDA_BIT_CLK	12 51
H44D	HDA_55S	HDA	HDA_BIT_CLK_R	12
H43C HDA_RST	HDA_55S	HDA	HDA_RST_L	12 51
H43C	HDA_55S	HDA	HDA_RST_R_L	12
H44C HDA_OUT	HDA_55S	HDA	HDA_SDOUT	12 51
H43C	HDA_55S	HDA	HDA_SDOUT_R	12 17
H43C HDA_SYNC	HDA_55S	HDA	HDA_SYNC	12 51
H43C	HDA_55S	HDA	HDA_SYNC_R	12
H43C HDA_IN	HDA_55S	HDA	HDA_SDIN0	12 51
H43C	HDA_55S	HDA	AUD_SDI_R	
SPDIF				
H47C	HDA_55S	HDA	DP_INT_SPDIF_AUDIO	39 51 80
H47J	HDA_55S	HDA	SPDIF_OUT_JACK	51 54
H42C	HDA_55S	HDA	CS4208_SPDIF_IN	51
H42F	HDA_55S	HDA	CS4208_SPDIF_OUT	51

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
H49J	SPI_50S	SPI	SPI_CLK_R	14 45
H49C	SPI_50S	SPI	SPI_CLK	45
H49K	SPI_50S	SPI	SPI_ALT_CLK	45
H48C	SPI_50S	SPI	SPI_SMC_CLK	43 45
H48F	SPI_50S	SPI	SPI_MLB_CLK	45
H49E	SPI_50S	SPI	SPI_CS0_R_L	14 45
H49D	SPI_50S	SPI	SPI_CS0_L	45
H49G	SPI_50S	SPI	SPI_ALT_CS_L	45
H48G	SPI_50S	SPI	SPI_SMC_CS_L	43 45
H49F	SPI_50S	SPI	SPI_MLB_CS_L	45
H49B	SPI_50S	SPI	SPI_MOSI_R	14 45
H48C	SPI_50S	SPI	SPI_MOSI	45
H48J	SPI_50S	SPI	SPI_ALT_MOSI	45
H43K	SPI_50S	SPI	SPI_SMC_MOSI	43 45
H48K	SPI_50S	SPI	SPI_MLB_MOSI	45
H48B	SPI_50S	SPI	SPI_MISO	14 45
H48C	SPI_50S	SPI	SPI_ALT_MISO	45
H43K	SPI_50S	SPI	SPI_SMC_MISO	43 45
H43C	SPI_50S	SPI	SPI_MLB_MISO	45
H49G	SPI_50S	SPI	SPIROM_USE_MLB	15 45

SYNC_MASTER=J70_NICK SYNC_DATE=10/15/2013

PAGE TITLE: PCH and BR Constraints

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 115 OF 123

SHEET: 74 OF 81

USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions
Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

Constraints
Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor’s SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor’s SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
J42C USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_D2R_P	14 41
J42A USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_D2R_N	14 41
J43B	USB3_PHY	USB3	USB3_EXTA_D2R_F_P	41
J43D	USB3_PHY	USB3	USB3_EXTA_D2R_F_N	41
J41A USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTA_R2D_P	41
J41C USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTA_R2D_N	41
J43A	USB3_PHY	USB3	USB3_EXTA_R2D_F_P	41
J43C	USB3_PHY	USB3	USB3_EXTA_R2D_F_N	41
J49A	USB3_PHY	USB3	USB3_EXTA_R2D_CF_P	14 41
J49C	USB3_PHY	USB3	USB3_EXTA_R2D_CF_N	14 41
J41E USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_P	14 41
J41G USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_N	14 41
J41B	USB2_PHY	USB2	USB2_EXTA_MUXED_P	41
J42E	USB2_PHY	USB2	USB2_EXTA_MUXED_N	41
J49E	USB2_PHY	USB2	USB2_EXTA_P	41
J49C	USB2_PHY	USB2	USB2_EXTA_N	41
External Port B (J4610)				
J42J USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_D2R_P	14 41
J42L USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_D2R_N	14 41
J42F	USB3_PHY	USB3	USB3_EXTB_D2R_F_P	41
J42K	USB3_PHY	USB3	USB3_EXTB_D2R_F_N	41
J42G USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTB_R2D_P	41
J42H USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTB_R2D_N	41
J42D	USB3_PHY	USB3	USB3_EXTB_R2D_F_P	41
J42E	USB3_PHY	USB3	USB3_EXTB_R2D_F_N	41
J49G	USB3_PHY	USB3	USB3_EXTB_R2D_CF_P	14 41
J49E	USB3_PHY	USB3	USB3_EXTB_R2D_CF_N	14 41
J43E USB2_CONN	USB2_PHY	USB2	USB_EXTB_1_P	14 41
J43G USB2_CONN	USB2_PHY	USB2	USB_EXTB_1_N	14 41
J43J	USB2_PHY	USB2	USB2_EXTB_P	41
J43H	USB2_PHY	USB2	USB2_EXTB_N	41
External Port C (J4700)				
J43K USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_D2R_P	14 42
J43M USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_D2R_N	14 42
J43L	USB3_PHY	USB3	USB3_EXTC_D2R_F_P	42
J44C	USB3_PHY	USB3	USB3_EXTC_D2R_F_N	42
J44J USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_R2D_P	42
J44L USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_R2D_N	42
J44E	USB3_PHY	USB3	USB3_EXTC_R2D_F_P	42
J44G	USB3_PHY	USB3	USB3_EXTC_R2D_F_N	42
J49K	USB3_PHY	USB3	USB3_EXTC_R2D_CF_P	14 42
J49M	USB3_PHY	USB3	USB3_EXTC_R2D_CF_N	14 42
J44E USB2_CONN	USB2_PHY	USB2	USB_EXTC_2_P	14 42
J44G USB2_CONN	USB2_PHY	USB2	USB_EXTC_2_N	14 42
J43C	USB2_PHY	USB2	USB2_EXTC_P	42
J43F	USB2_PHY	USB2	USB2_EXTC_N	42
External Port D (J4710)				
J45K USB3_RX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTD_D2R_P	14 42
J45M USB3_RX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTD_D2R_N	14 42
J45C	USB3_PHY	USB3	USB3_EXTD_D2R_F_P	42
J45E	USB3_PHY	USB3	USB3_EXTD_D2R_F_N	42
J45F USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_R2D_P	42
J45H USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_R2D_N	42
J46C	USB3_PHY	USB3	USB3_EXTD_R2D_F_P	42
J45G	USB3_PHY	USB3	USB3_EXTD_R2D_F_N	42
J49B	USB3_PHY	USB3	USB3_EXTD_R2D_CF_P	14 42
J49D	USB3_PHY	USB3	USB3_EXTD_R2D_CF_N	14 42
J46E USB2_CONN	USB2_PHY	USB2	USB_EXTD_3_P	14 42
J46G USB2_CONN	USB2_PHY	USB2	USB_EXTD_3_N	14 42
J46B	USB2_PHY	USB2	USB2_EXTD_P	42
J46D	USB2_PHY	USB2	USB2_EXTD_N	42
Camera (J3510)				
H2C USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_P	14 37
H2E USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_N	14 37
PCH USB Compensation				
H8E	PCH_55S	COMP_PCH	PCH_USB_RBIAS	14

RMH Love

Electrical Contraint Set	Physical	Spacing		
J49D USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_P	14 31
J41C USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_N	14 31
J45D USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_P	31
J45C USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_N	31

Et tu Brute?

Electrical Contraint Set	Physical	Spacing		
Ethernet				
J47C ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	34 35
J47E ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	34 35
J47G	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	35
J47J	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	35
J51C		ENET_TRANS	ENETCONN_MCT0	35
J52C		ENET_TRANS	ENETCONN_MCT1	35
J52A		ENET_TRANS	ENETCONN_MCT2	35
J52J		ENET_TRANS	ENETCONN_MCT3	35
J52E		ENET_TRANS	ENETCONN_MCT_BS	35
J47K	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	34
SD				
J47A SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0>	34
J48C	SD_PHY	SD	SDCONN_DATA<7..0>	34 36
J48L SD_CMD	SD_PHY	SD	ENET_SD_CMD	34
J48J	SD_PHY	SD	SDCONN_CMD	34 36
J48A SD_CLK	SD_PHY	SD	ENET_SD_CLK	34
J48E	SD_PHY	SD	SDCONN_CLK	34 36
J48G	SD_PHY	SD	SDCONN_CLK_R	36
J48N	SD_PHY	SD	ENET_MEDIA_SENSE	15 34
J48N	SD_PHY	SD	ENET_SD_DETECT_L	34 36
CIV SPI				
J49C	CIV_SPI	SPI	ENET_SCLK	34
J48C	CIV_SPI	SPI	ENET_MISO	34
J49J	CIV_SPI	SPI	ENET_MOSI	34
J49J	CIV_SPI	SPI	ENET_CS_L	34

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing		
H5B SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	37
H5D SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	37
H5A SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	37
H5C SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	37
H6B	SPI_50S	SPI	CAM_SF_CLK	37
H6D	SPI_50S	SPI	CAM_SF_CLK_R	37
H6C	SPI_50S	SPI	CAM_SF_DIN	37
H5E	SPI_50S	SPI	CAM_SF_DIN_R	37
H5J	SPI_50S	SPI	CAM_SF_CS_L	37
H5L	SPI_50S	SPI	CAM_SF_WP_L	37
H5G	SPI_50S	SPI	CAM_SF_DOUT	37
H5E	SPI_50S	SPI	CAM_SF_DOUT_R	37
H5K	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	37
H5H	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	37

SYNC_MASTER=J70_DINI SYNC_DATE=10/28/2013

PAGE TITLE
USB/Ethernet/SD Constraints

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 116 OF 123
SHEET 75 OF 81

SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=1.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMC Generic Control Line Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMC_ISO	*	=1:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO

SMC Generic Control Line Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMC_GEN	*	SMC_50S

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
I3		SENSE	GND_SMC_AVSS	43 44 47
12V S5 (System Total)				
I4 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	47
I5 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	47
I6		SENSE	ISNS_P12VG3H_R	47
I7		SENSE	ISNS_P12VG3H	44 47
I8		SENSE	VSNS_P12VG3H	44 47
SSD				
I85 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	47
I87 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	47
I86		SENSE	ISNS_SSDS0_R	47
I88		SENSE	ISNS_SSDS0	44 47
I89		SENSE	VSNS_P3V3_SSD	44 47
VDDQ S3 (DDR)				
I33 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V2_S3_DDR_P	47
I32 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V2_S3_DDR_N	47
I35		SENSE	ISNS_P1V2_S3_DDR_R	47
I34		SENSE	ISNS_P1V2_S3_DDR	44 47
I26		SENSE	VSNS_P1V2_S3_DDR	44 47
CPU Core				
I42		SENSE	CPUVR_IMON	47 57
I45		SENSE	ISNS_CPUVCC	44 47
I46		SENSE	VSNS_CPUVCC	44 47

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
I81	CLK_XTAL	XTAL	SMC_XTAL	43 44
I82	CLK_XTAL	XTAL	SMC_EXTAL	43 44
I91	SMC_GEN	SMC_CTRL	SMC_LRESET_L	18 43
I90	SMC_GEN	SMC_CTRL	SMC_RUNTIME_SCI_L	13 43
I92	SMC_GEN	SMC_CTRL	SMC_WAKE_SCI_L	15 43
I93	SMC_GEN	SMC_CTRL	SMC_FAN_0_CTL	43 49
I94	SMC_GEN	SMC_CTRL	SMC_FAN_0_TACH	43 49

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
I10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	43 46
I9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	43 46
I11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	43 46
I12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	43 46
I13	SMB_PHY	SMB	SMBUS_SMC_2_S0_SCL	43 46
I14	SMB_PHY	SMB	SMBUS_SMC_2_S0_SDA	43 46
I15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	43 46
I16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	43 46
I19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	43 44
I20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	43 44
PCH				
I51	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_CLK	14 46
I52	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_DATA	14 46
I53	SMB_PHY	SMB	SML_PCH_0_CLK	14 46
I54	SMB_PHY	SMB	SML_PCH_0_DATA	14 46
Display TCon				
I55	SMB_PHY	SMB	SMB_DP_TCON_SCL	
I56	SMB_PHY	SMB	SMB_DP_TCON_SDA	

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
I67 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	48
I68 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	48
I69 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_P	48
I68 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_N	48
I65 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	48 56
I66 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	48 56
I42	SNS_DIFF_PHY	SENSE	SNS_T1_2_P	48
I42	SNS_DIFF_PHY	SENSE	SNS_T1_2_N	48
TMP423 (Development)				
I67 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	48
I68 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	48
I69 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	48
I70 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	48
I71 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	48
I72 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	48
HDD Out-of-Band				
I73		SENSE	HDD_OOB1_D2R_L	33
I74		SENSE	HDD_OOB1_D2R_F_L	33
I75		SENSE	HDD_OOB1_D2R_R_L	33
I83		SENSE	SMC_OOB1_D2R_L	33 43
I76		SENSE	SMC_OOB1_R2D_L	33 43
I81		SENSE	SMC_OOB1_R2D_R_L	33
SSD Out-of-Band				
I77		SENSE	SMC_OOB2_R2D_L	32 44
I78		SENSE	SMC_OOB2_D2R_L	32 44

SYNC_MASTER=J70_NICK SYNC_DATE=10/15/2013

PAGE TITLE
SMBus/Sensor Constraints

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D

REVISION A.0.0

BRANCH

PAGE 117 OF 123

SHEET 76 OF 81

DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

VDDQ (1.2V)/VTT (0.6V) S3

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I43	POWER	POWER	5V			PP5V_REG_P1V2_V5IN 59 77
Local Ground						
I44	GND	GND	0V			AGND_P1V2_S3 59 77
VDDQ S3						
I45	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V2_S3 59
I47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V2_S3_L 59
I46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V2_S3 59
I48	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V2_S3_RC 59
I49	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V2_S3 59
I50	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V2_S3_R
I52	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V2S3
I51	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V2_S3 59
I53	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_VDDQSNS 59
I55	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_VREF 59
I56	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_REFIN 59
I57	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_MODE 59
I58	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_TRIP 59
I59	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS 59
I61	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_VTTREF 59
Output Bus						
I60	POWER	POWER	1.2V			PP1V2_S3 66
I62	POWER_DDR	POWER_DDR	0.6V			PP0V6_S3_DDRVTT 66
Sensed						
I54	POWER	POWER	1.2V			PP1V2_S3_DDR 66

PCH 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I1	POWER	POWER	5V			REG_VCC_U7400 60
I2	POWER	POWER	5V			REG_PVCC_U7400 60
Local Ground						
I3	GND	GND	0V			AGND_P1V05S0 60
1.05V S0						
I5	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0 60
I4	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L 60
I7	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0 60
I6	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0_RC 60
I8	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0 60
I9	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R 60
I10	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0 60
I12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0 60
I11	VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET 60
I14	VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO 60
I86	SNS_CURRENT	SNS_DIFF_PHY	SENSE			REG_P1V05S0_PHASE_SNS_P 60
I85	SNS_CURRENT	SNS_DIFF_PHY	SENSE			REG_P1V05S0_PHASE_SNS_M 60
I16		SENSE				REG_P1V05S0_FB 60
I15		SENSE				REG_P1V05S0_RTN 60
I21	VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF 60
I20	VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL 60
Output Bus						
I22	POWER	POWER	1.05V			PP1V05_S0 66

1.8V S3

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I67	POWER	POWER	5V			PP5V_REG_P1V2_V5IN 59 77
Local Ground						
I68	GND	GND	0V			AGND_P1V2_S3 59 77
Switch						
I69	VR_DIDT_PHY	VR_SWITCH	3.3V	TRUE		REG_SW_P1V8_S3 59
I70	VR_DIDT_PHY	VR_SWITCH	3.3V	TRUE		REG_FB_P1V8_S3 59
Output Bus						
I83	POWER	POWER	1.8V			PP1V8_S3_REG_R 59
I84	POWER	POWER	1.8V			PP1V8_S3 66

SYNC_MASTER=J70 GAREN SYNC_DATE=03/07/2014

PAGE TITLE: VReg Constraints

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 118 OF 123

SHEET: 77 OF 81

CPU VCC Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H126	POWER	POWER	12V			PP12V_S0_REG_CPUVCC_VIN 57
H118	POWER	POWER	5V			PP5V_S0_REG_CPUVCC_VDD 57
Local Ground						
H126	GND	GND	0V			AGND_CPU
Phase 1						
H89	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1 57 58
H93	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_1 58
H88	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1 58
H86	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1_RC 58
H92	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_1 58
H90	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_1 58
H87	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_1 58
H97	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1 58
H85 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS1_M 58
H95 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS1_P 58
H84		SENSE				REG_CPUVCC_ISEN1 57 58
H122		SENSE				REG_CPUVCC_ISUMN 57 58
H127		SENSE				REG_CPUVCC_ISUMP 57 58
Phase 2						
H116	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2 57 58
H113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_2 58
H114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2 58
H115	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2_RC 58
H117	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_2 58
H119	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_2 58
H120	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_2 58
H106	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2 58
H105 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS2_M 58
H103 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS2_P 58
H110		SENSE				REG_CPUVCC_ISEN2 57 58

CPU VCC Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL95826HRZ						
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FCCM 57 58
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DRSEL 57
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP 57
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP_RC 57
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB 57
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB_RC 57
H103	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB2 57
H101 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_P 8 57
H104 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_N 9 57
H101		SENSE				CPU_VCCSENSE_P_R 57
H103		SENSE				CPU_VCCSENSE_P_RC 57
H103		SENSE				REG_CPUVCC_ISUMN_RC 57
H101		SENSE				REG_CPUVCC_ISUMN_R 57
H103		SENSE				REG_CPUVCC_RTN 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NTC 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NTC_R 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_SLOPE 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG1 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG2 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG3 57
H100 CPU_VIDSCLK	VR_VID_PHY	VR_VID				CPU_VIDSCLK 8 57
H100	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R 8
H100 CPU_VIDALERT_L	VR_VID_PHY	VR_VID				CPU_VIDALERT_L 8 57
H100	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L 8
H100 CPU_VIDSOUT	VR_VID_PHY	VR_VID				CPU_VIDSOUT 8 57
H100	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R 8
Output Bus						
H108	POWER	POWER	1.8V			PPCPUVCC_S0_CPU 66

SYNC_MASTER=J70_GAREN SYNC_DATE=03/07/2014

PAGE TITLE: CPU VReg Constraints

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 119 OF 123

SHEET: 78 OF 81

12V

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H45	POWER	POWER	12V			PP12V_ACDC 66
FET Switched						
H46	POWER	POWER	12V			PP12V_S5 66
H45	POWER	POWER	12V			PP12V_S0 66
Sensed						
H45	POWER	POWER	12V			PP12V_G3H 66

3.42V G3H

	Physical	Spacing	Voltage	DIDT	NO_TEST	
3.42V G3H						
H45	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_BOOST 56
H45	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_SW 56
H45	VR_CTL_PHY	VR_CTL				P3V42G3H_FB 56
H46	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L 56
H45	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_R_L 56
Output Bus						
H45	POWER	POWER	3.425V			PP3V42_G3H 66
H45	POWER	POWER	3.425V			PP3V42_G3H_REG_R 56

3.3V G3

	Physical	Spacing	Voltage	DIDT	NO_TEST	
H57	POWER	POWER	3.3V			PP3V3_G3 66

3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H45	POWER	POWER	12V			REG_VIN_U7600 61
H42	POWER	POWER	5V			REG_VCC1_U7600 61
H42	POWER	POWER	5V			REG_VCC2_U7600 61
3.3V S5						
H46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5 61
H47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5 61
H84	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5_RC 61
H46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5 61
H86	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5 61
H85	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5 61
H87	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN 61
H87	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET 61
H87	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET 61
H60	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT 61
H87	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R 61
H87	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB 61
5V S4						
H11	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4 61
H11	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4 61
H11	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4_RC 61
H11	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4 61
H11	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4 61
H11	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4 61
H11	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN 61
H11	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET 61
H11	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET 61
H11	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT 61
H11	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R 61
H11	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB 61
Output Bus						
H11	POWER	POWER	5V			PP5V_S5 66
H11	POWER	POWER	5V			PP5V_S4 66
H12	POWER	POWER	3.3V			PP3V3_S5 66
FET Switched						
H12	POWER	POWER	5V			PP5V_S0 66
H12	POWER	POWER	3.3V			PP3V3_S4 66
H12	POWER	POWER	3.3V			PP3V3_S0 66
H14	POWER	POWER	3.3V			PP3V3_S0_SSD 66
H12	POWER	POWER	3.3V			PP3V3_ENET 66
H38	POWER	POWER	3.3V			PP3V3_TBTLC 18 26 27
Sensed						
H44	POWER	POWER	3.3V			PPSSD_S0 66

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
FET Switched						
H45	POWER	POWER	5V			PP5V_S0_HDD 66

1V5 S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
OUTPUT BUS						
H47	POWER	POWER	1.5V			PP1V5_S0 66
H48	VR_CTL_PHY	VR_CTL				REG_P1V5S0_SS
H48	VR_CTL_PHY	VR_CTL				REG_P1V5S0_ISET
H48	VR_CTL_PHY	VR_CTL				REG_P1V5S0_ADJ

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Common						
H35	GND	GND	0V			GND
H49	GND	GND	0V			PGND_REG_P1V2_S3 59

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
H46	SNS_CURRENT	SNS_DIFF_PHY	SENSE			REG_P3V3S5_PHASE_SNS_P 61
H46	SNS_CURRENT	SNS_DIFF_PHY	SENSE			REG_P3V3S5_PHASE_SNS_M 61
H45	SNS_CURRENT	SNS_DIFF_PHY	SENSE			REG_P5VS4_PHASE_SNS_P 61
H45	SNS_CURRENT	SNS_DIFF_PHY	SENSE			REG_P5VS4_PHASE_SNS_M 61

SYNC_MASTER=J70_GAREN SYNC_DATE=03/07/2014

PAGE TITLE
Platform VReg Constraints

Apple Inc.

DRAWING NUMBER 051-1407 SIZE D
REVISION A.0.0
BRANCH
PAGE 120 OF 123
SHEET 79 OF 81

Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C_ISO	*	=2x_DIELECTRIC	?
TBT_SPI_ISO	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP	*	*	TBTDP_ISO
TBT_SPI	*	*	TBT_SPI_ISO
TBT_I2C	*	*	TBT_I2C_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_ISO

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
I651	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 26
I651	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 26
I652 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	26
I654 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	26
I636	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	13 26
I651	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	13 26
I653 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	26
I651 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	26
I635	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 26
H621	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 26
H620 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	26
H622 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	26
H622	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	13 26
H624	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	13 26
H626 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	26
H624 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	26
I680 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	40
I682 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	40
I681 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	40
I683 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	40
H692 DP_TNTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	40
H693 DP_TNTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	40
I660	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	40
I662	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	40
I653 TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	26
I654 TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	26
I656 TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	26
I657 TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	26

*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
I642 DP_INTPNL_IG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_ML_P<1..0>	5 40
I644 DP_INTPNL_IG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_ML_N<1..0>	5 40
I646 DP_INTPNL_IG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	5 40
I645 DP_INTPNL_IG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	5 40
I646	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	40
I647	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	40
Internal Panel				
I688	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	40
I690	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	40
I687 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	39 40
I689 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	39 40
I686 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	39 40
I691 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	39 40
Internal DP SPDIF				
I631		HDA	DP_INT_SPDIF_AUDIO	39 51 74
DDC				
I692	TBT_I2C_55S	TBT_I2C	DP_TBTSNK0_DDC_CLK	13 30
I693	TBT_I2C_55S	TBT_I2C	DP_TBTSNK0_DDC_DATA	13 30
I694	TBT_I2C_55S	TBT_I2C	DP_TBTSNK1_DDC_CLK	13 30
I695	TBT_I2C_55S	TBT_I2C	DP_TBTSNK1_DDC_DATA	13 30
I698	TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_CLK	28 30
I699	TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_DATA	28 30
I697	TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_CLK	29 30
I696	TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_DATA	29 30

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
I641 TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	26 28
I642 TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	26 28
I643	TBTDP_90D	TBTDP	TBT_A_R2D_P<1>	28
I644	TBTDP_90D	TBTDP	TBT_A_R2D_N<1>	28
I745 TBT_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	26 28
I746 TBT_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	26 28
I747	TBTDP_90D	TBTDP	TBT_A_R2D_P<0>	28
I748	TBTDP_90D	TBTDP	TBT_A_R2D_N<0>	28
I650 DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	26 28
I650 DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	26 28
I648	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	28
I647	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	28
I680 DP_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	26 28
I681 DP_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	26 28
I679	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	28
I678	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	28
I646 DP_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	28
I645 DP_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	28
I5C0 TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	26 28
I5C1 TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	26 28
I731	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1>	28
I730	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1>	28
I6F6 TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	26 28
I6F5 TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	26 28
I649	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<0>	28
I650	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<0>	28
I6D0 TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	28
I6D1 TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	28
I650 TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	26 28
I660 TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	26 28
I650	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	28
I650	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	28
Port B				
I655 TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	26 29
I655 TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	26 29
I656	TBTDP_90D	TBTDP	TBT_B_R2D_P<1>	29
I654	TBTDP_90D	TBTDP	TBT_B_R2D_N<1>	29
I7D6 TBT_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	26 29
I7D5 TBT_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	26 29
I7A9	TBTDP_90D	TBTDP	TBT_B_R2D_P<0>	29
I7A8	TBTDP_90D	TBTDP	TBT_B_R2D_N<0>	29
I669 DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	26 29
I669 DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	26 29
I668	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	29
I667	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	29
I669 DP_ML3_RVSD	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	26 29
I669 DP_ML3_RVSD	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	26 29
I66A	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	29
I66B	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	29
I666 DP_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	29
I667 DP_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	29
I5C6 TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	26 29
I5C4 TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	26 29
I7A6	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1>	29
I7A5	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1>	29
I7F6 TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	26 29
I7F7 TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	26 29
I6C1	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<0>	29
I6C0	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<0>	29
I7F1 TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	29
I7F0 TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	29
I660 TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	26 29
I667 TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	26 29
I666	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	29
I670	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	29

SYNC_MASTER=J70_NICK SYNC_DATE=10/22/2013

PAGE TITLE: TBT/DP Constraints

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 121 OF 123
SHEET: 80 OF 81

Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H38	POWER	POWER	12V			PP12V_BKLT_SNS	62
H40	POWER	POWER	12V			PP12V_BKLT_FUSED	62
H46	POWER	POWER	12V			PP12V_S0_BKLT_FILT	62
H72	POWER	POWER	12V			PP12V_S0_BKLT_PWR	62
H94	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R	62
H96	POWER	POWER	5V			PP5V_S0_BKLT_R	62
H62	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO_R	62
Local Ground							
H34	BLC_CTL_PHY	BLC_PHASE	0V			PGND_BKLT	62
H70	BLC_CTL_PHY	BLC_PHASE	0V			DGND_BKLT	62
H88	BLC_CTL_PHY	BLC_PHASE	0V			LGND_BKLT	62
Backlight							
H76	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE	62
H36	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE	62
H54	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE_R	62
H78	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_SNUBBER	62
H52	BLC_CTL_PHY	BLC_PHASE	12V	TRUE		BKLT_SW_R	62
H50	BLC_CTL_PHY	BLC_CTL				BKLT_ISET	62
H74	BLC_CTL_PHY	BLC_CTL				BKLT_FLT	62
H48	BLC_CTL_PHY	BLC_CTL				BKLT_FLT_RC	62
H32	SNS_DIFF_PHY	SENSE				BKLT_SW_P	62
H30	SNS_DIFF_PHY	SENSE				BKLT_SW_M	62
H42		SENSE				BKLT_FB	62
H80		BLC_HV	67V			BKLT_FB_XW	62
H44		BLC_HV	67V			BKLT_FB_R	62
H27	POWER_BLC_RET	BLC_CTL				BKLT_ISEN1	62
H29	POWER_BLC_RET	BLC_CTL				BKLT_ISEN2	62
H31	POWER_BLC_RET	BLC_CTL				BKLT_ISEN3	62
H33	POWER_BLC_RET	BLC_CTL				BKLT_ISEN4	62
H35	POWER_BLC_RET	BLC_CTL				BKLT_ISEN5	62
H37	POWER_BLC_RET	BLC_CTL				BKLT_ISEN6	62
H26	POWER_BLC_RET	BLC_HV				BKLT_ISEN1_R	62
H28	POWER_BLC_RET	BLC_HV				BKLT_ISEN2_R	62
H30	POWER_BLC_RET	BLC_HV				BKLT_ISEN3_R	62
H32	POWER_BLC_RET	BLC_HV				BKLT_ISEN4_R	62
H34	POWER_BLC_RET	BLC_HV				BKLT_ISEN5_R	62
H36	POWER_BLC_RET	BLC_HV				BKLT_ISEN6_R	62
H38	POWER_BLC_RET	BLC_HV				LED_RETURN_1	62
H40	POWER_BLC_RET	BLC_HV				LED_RETURN_2	62
H42	POWER_BLC_RET	BLC_HV				LED_RETURN_3	62
H44	POWER_BLC_RET	BLC_HV				LED_RETURN_4	62
H46	POWER_BLC_RET	BLC_HV				LED_RETURN_5	62
H48	POWER_BLC_RET	BLC_HV				LED_RETURN_6	62
Output Bus							
H24	POWER_BLC	BLC_HV	67V			BKLT_BOOST	62
H22	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1	62
H20	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2	62

Cello Miscellaneous

	Electrical Contraint Set	Physical	Spacing		
SPI					
H66		SMB_PHY	SMB	BKLT_SCL	62
H68		SMB_PHY	SMB	BKLT_SDA	62

SYNC_MASTER=J70_GAREN SYNC_DATE=03/07/2014

PAGE TITLE: BLC Constraints

Apple Inc.

DRAWING NUMBER: 051-1407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 123 OF 123

SHEET: 81 OF 81