PCB Stackups

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : PWR
LAYER 6 : BOT

15.6" Discrete Block Diagram

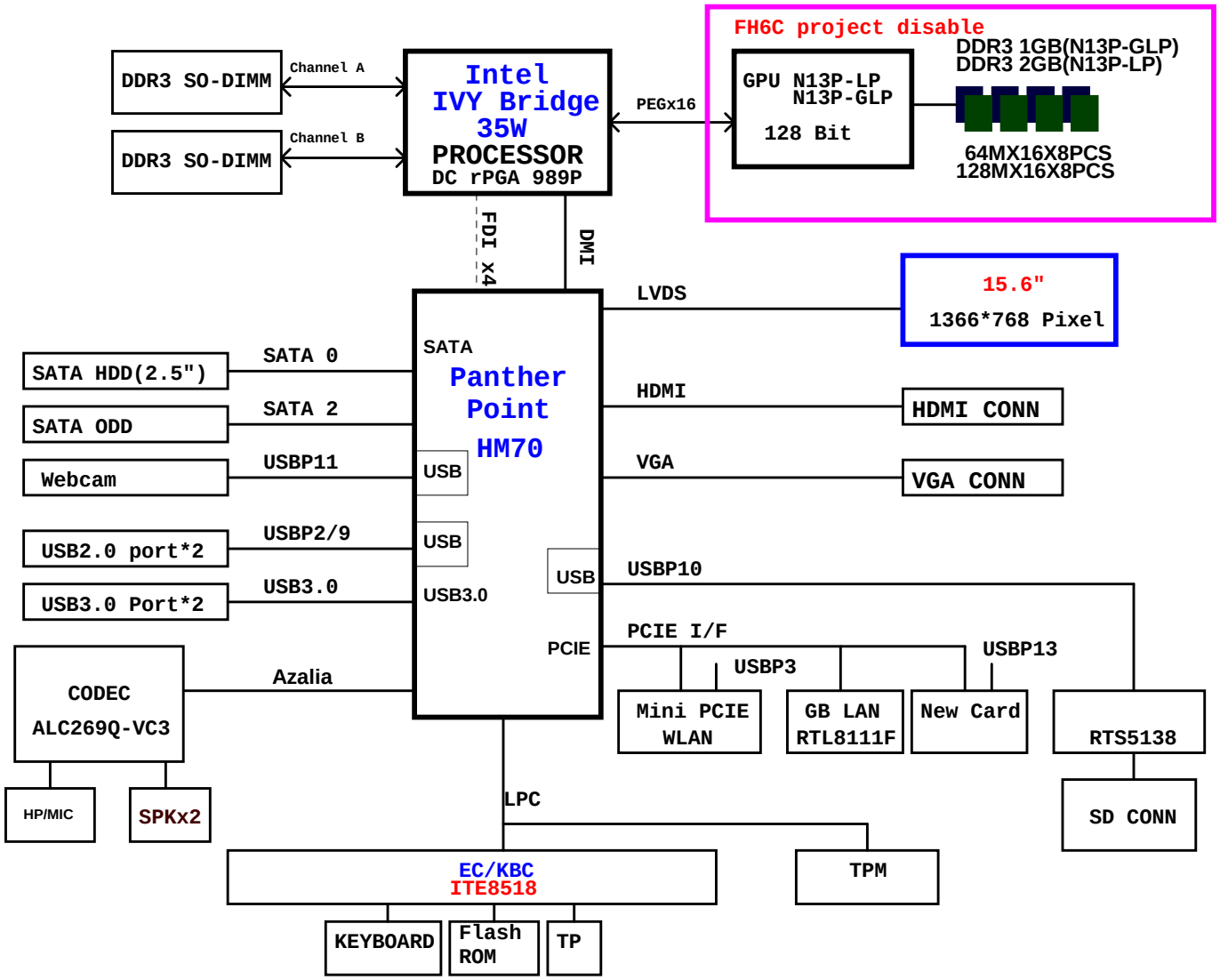

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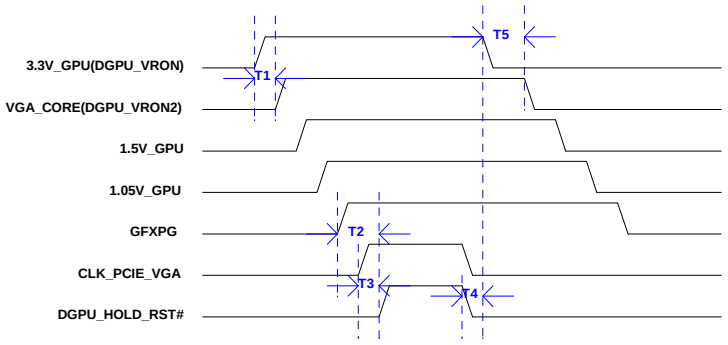
Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
3V_RTC	+3.0V~+3.3V		S0~G3
3V_S0	+3.3V	S0_ON1	S0
3V_S5	+3.3V	EC	S0~S5
3V_AUX	+3.3V	AC/DC Insert enable	AWLAYS
5V_S0	+5V	S0_ON1	S0
5V_S3	+5V	S3_ON	S0~S3
5V_S5	+5V	EC	S0~S5
5V_AUX	+5V	AC/DC Insert enable	AWLAYS
1.8V_S0	+1.8V	S0_ON2	S0
1.5V_S0	+1.5V	S0_ON2	S0
1.5V_S3	+1.5V	S3_ON	S0~S3
1.05V_S0	+1.05V	S0_ON2	S0
VCCSA	By VID	S0_ON2	S0
CPU_CORE	By VID	VR_ON	S0
VCC_AXG	By VID	VR_ON	S0
3V_LAN	+3.3V	LAN_ON	S0~S5(By WOL)
3V_GPU	+3.3V	DGPU_VRON	Optimus
1.5V_GPU	+1.5V	DGFX_VR_PWRGD	Optimus
1.05V_GPU	+1.05V	DGFX_VR_PWRGD	Optimus
VGA_CORE	By VID	DGPU_VRON1	Optimus

N13P-LP Power ON/OFF Sequence



BIOS/ EC control:
T1:DGPU_VRON to DGPU_VRON2 = 500us
T2:GFXPG to DGPU_HOLD_RST# = 5ms
T3:CLK_PCIE_VGA to DGPU_HOLD_RST# >100us(Spec)
T4:DGPU_HOLD_RST# to DGPU_VRON = 5ms
Note: Clock must be shutdown before 3.3V_GPU
T5:DGPU_VRON to DGPU_VRON2 = 500us

N13P-LP & N13P-GLP Table

	N13P-GLP	N13P-LP
VL3	BLM18P121SN (CX8PG121009)	0ohm_0603 (CS00003J951)

	N13P-GLP	N13P-LP
VR111	NA	10Kohm_0402 (CS31002FB26)

	N13P-GLP	N13P-LP
VR62	10Kohm_0402 (CS31002FB26)	NA

ID2	ID1	ID0	Model PU/PD RES P/N:CS31002JB28
0-R435	0-R438	0-R437	FJ8 UMA
0-R435	0-R438	1-R430	FJ8 Discrete
0-R435	1-R382	0-R437	FH6 UMA(Consumer)
0-R435	1-R382	1-R430	FH6 UMA(Commercial)
1-R384	0-R438	0-R437	FH6 N13P-LP
1-R384	0-R438	1-R430	FH6 N13P-GLP
1-R384	1-R382	0-R437	TBD
1-R384	1-R382	1-R430	TBD

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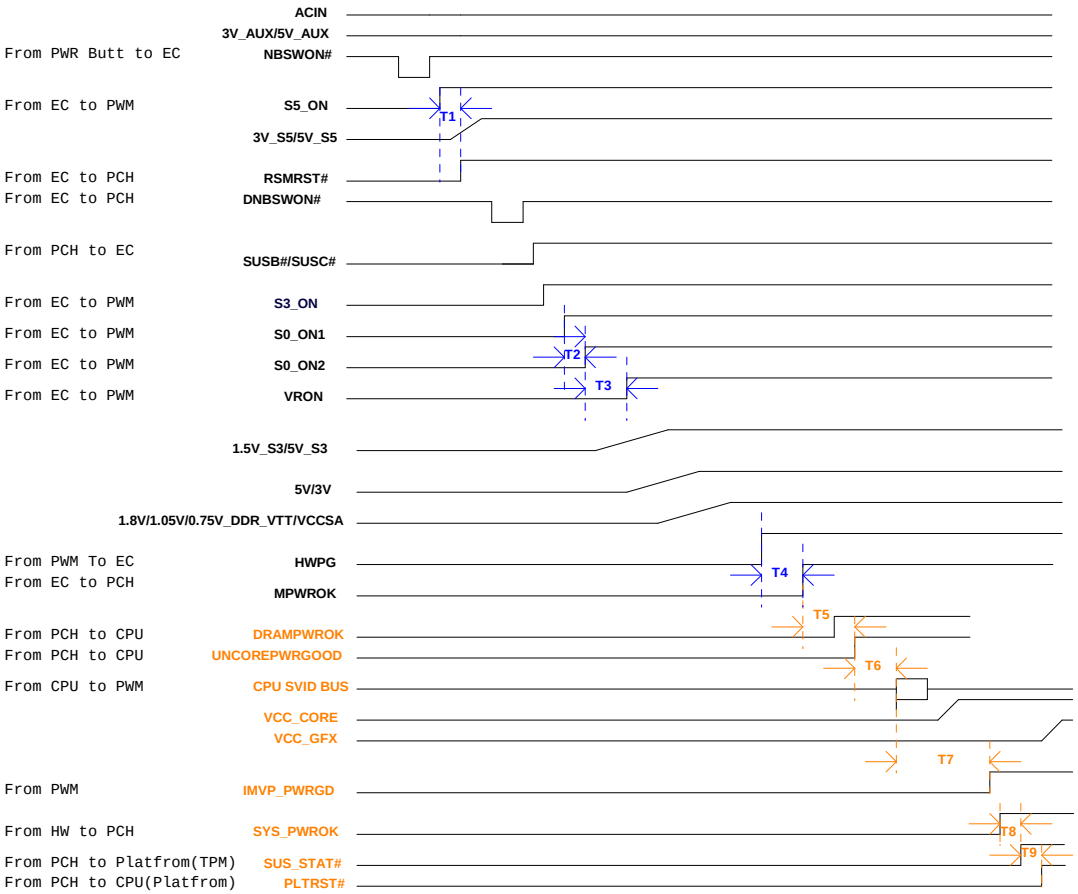
		GLP 1GB HYN	GLP 1GB SAM	GLP 2GB HYN	GLP 2GB SAM	LP 2GB HYN	LP 2GB SAM
ROM_SCLK	VR44 VR54	NA CS31502FB24	NA CS31502FB24	NA CS31502FB24	NA CS31502FB24	CS24992FB26 NA	CS24992FB26 NA
ROM_SI	VR41 VR52	NA CS31502FB24	NA CS32002FB29	NA CS33012FB18	NA CS34532FB18	NA CS33012FB18	NA CS34532FB18
ROM_SO	VR43 VR53	NA CS31002FB26	NA CS31002FB26	NA CS31002FB26	NA CS31002FB26	CS31002FB26 NA	CS31002FB26 NA
STRAP0	VR51 VR55	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA
STRAP1	VR46 VR56	NA CS34532FB18	NA CS34532FB18	NA CS34532FB18	NA CS34532FB18	NA CS24992FB26	NA CS24992FB26
STRAP2	VR47 VR57	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	NA CS32002FB29	NA CS32002FB29
STRAP3	VR48 VR58	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26
STRAP4	VR50 VR59	NA NA	NA NA	NA NA	NA NA	NA CS34532FB18	NA CS34532FB18

System Power-ON Sequence



System Power Sequence

EC Control:
T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)
T2: S0_ON1 TO S0_ON2 = 500us
T3: S0_ON2 TO VRON = 10ms
T4: HWPG TO MPWROK = 110ms (spec:mini 99ms)
Note:HWPG NEED TO BE HIGH at that time

System:
T5: MPWROK to UNCOREPWRGOOD =2ms(Min)
T6: UNCOREPWRGOOD to SVID Packet =500us(Max)
T7: SVID Packet to IMVP_PWRGD =5ms(Max)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9:SUS_STAT# to PLTRST# =60us(Min)

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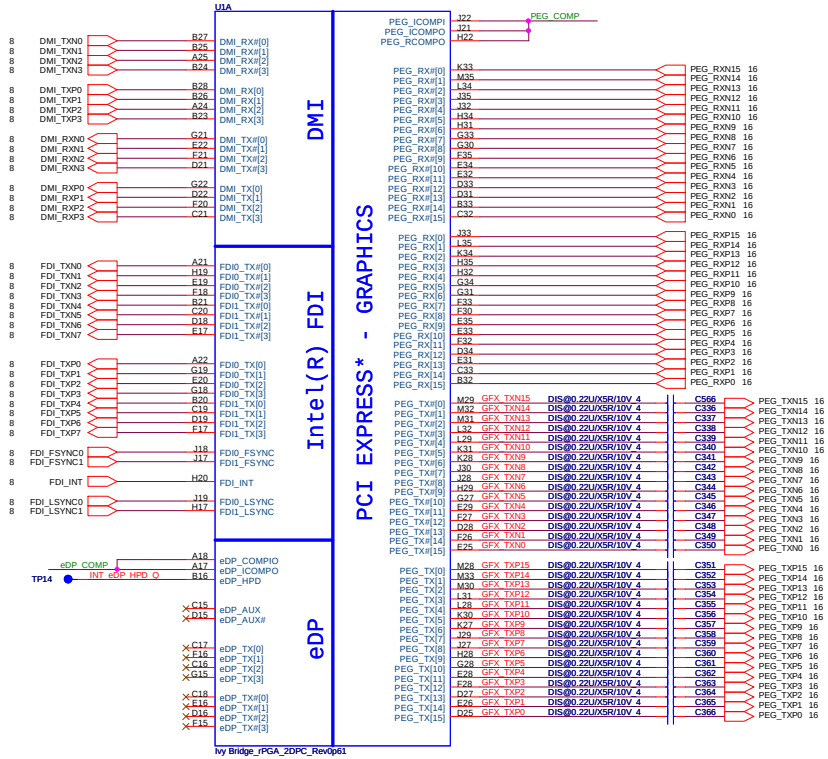
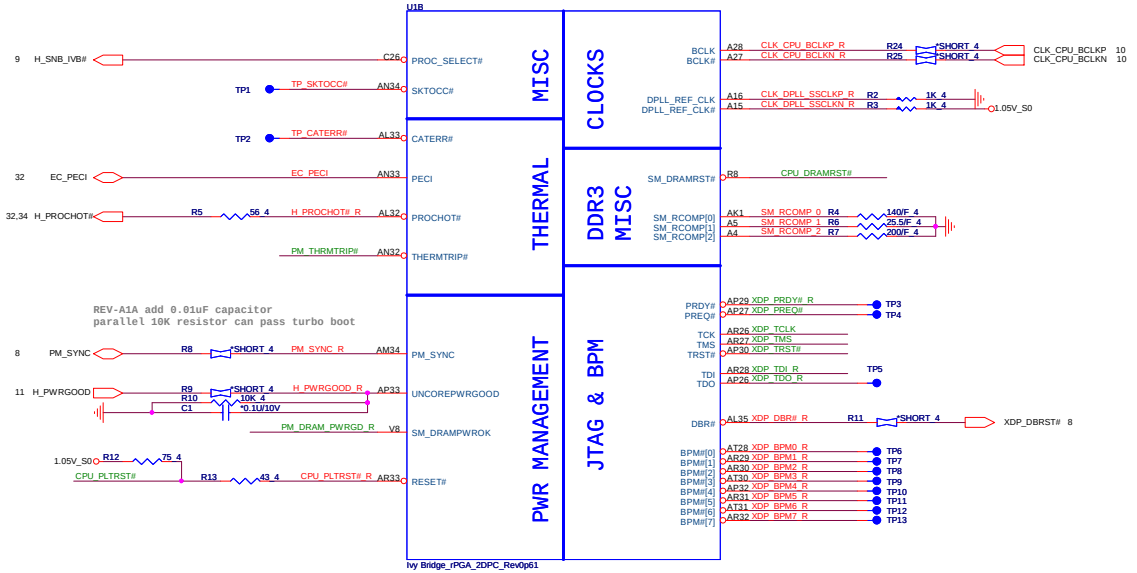
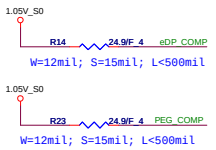
Ivy Bridge Processor (DMI,PEG,FDI)



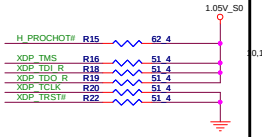
Ivy Bridge Processor (CLK,MISC,JTAG)



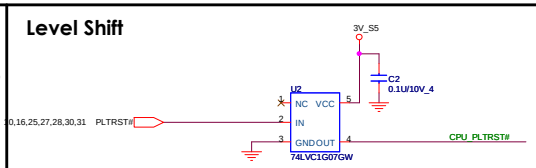
DP & PEG Compensation



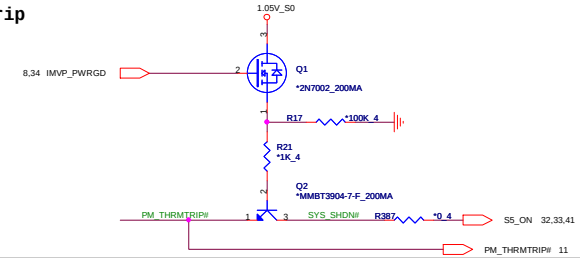
Processor pull-up



Level Shift



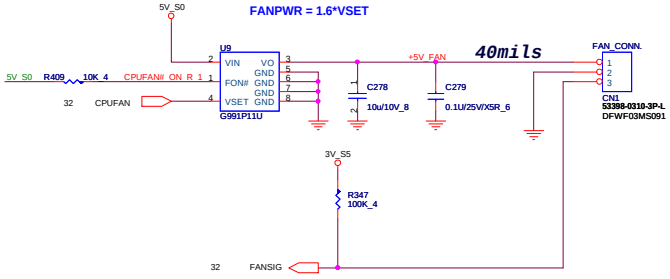
Thermal Trip



FAN Control-->For one FAN solution

VSET >= 1V, Enable

FANPWR = 1.6*VSET



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Ivy Bridge Processor (DDR3)

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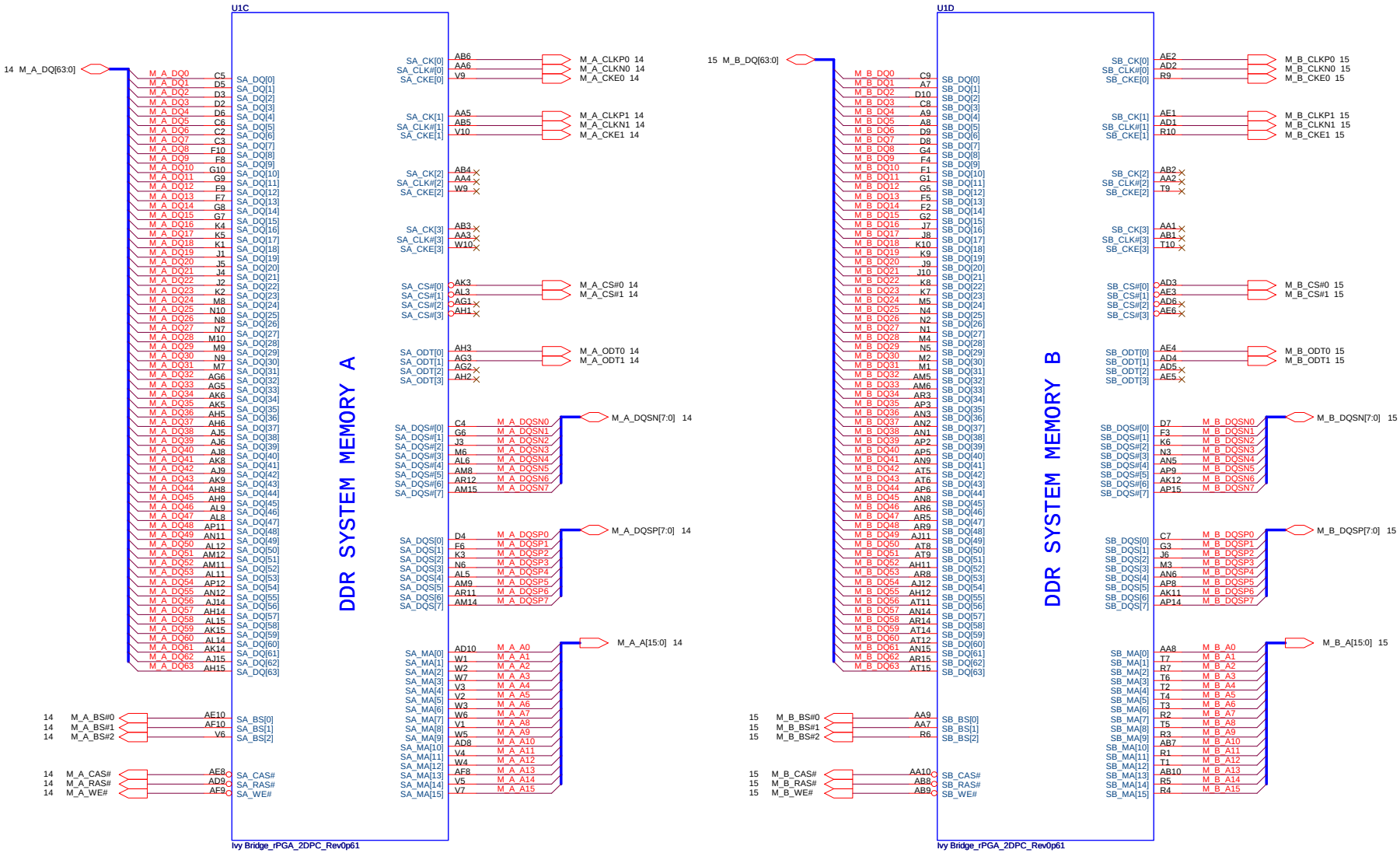

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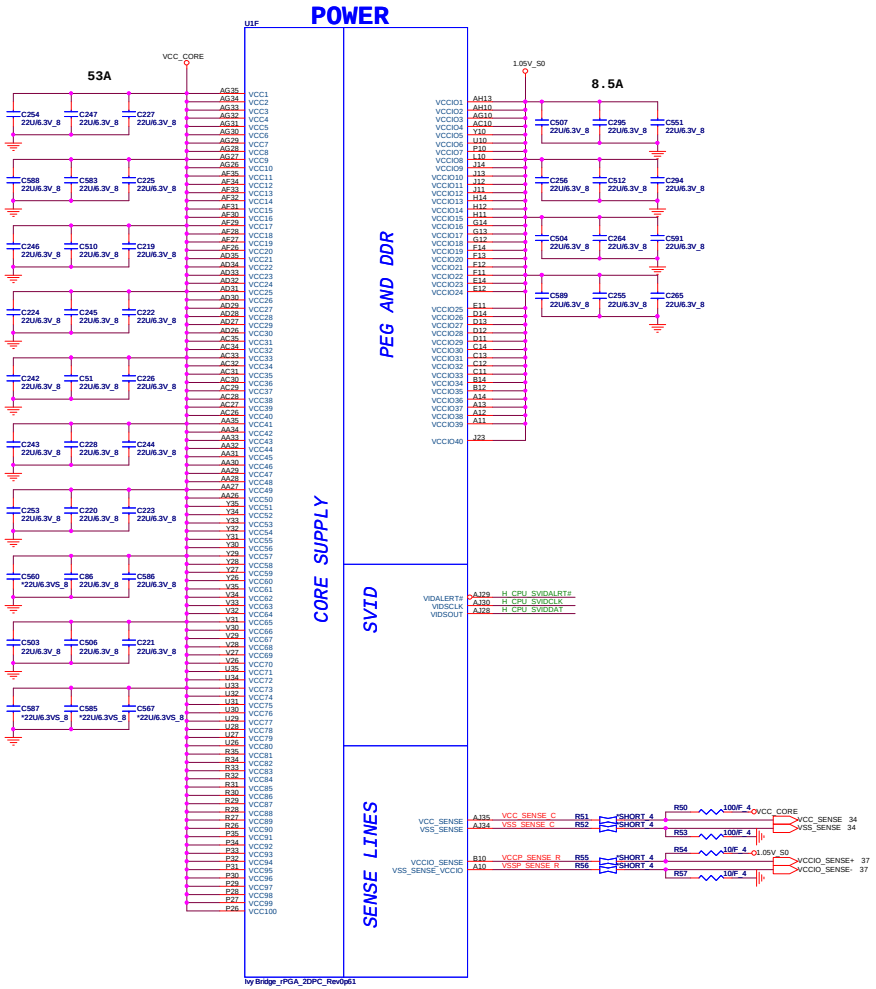
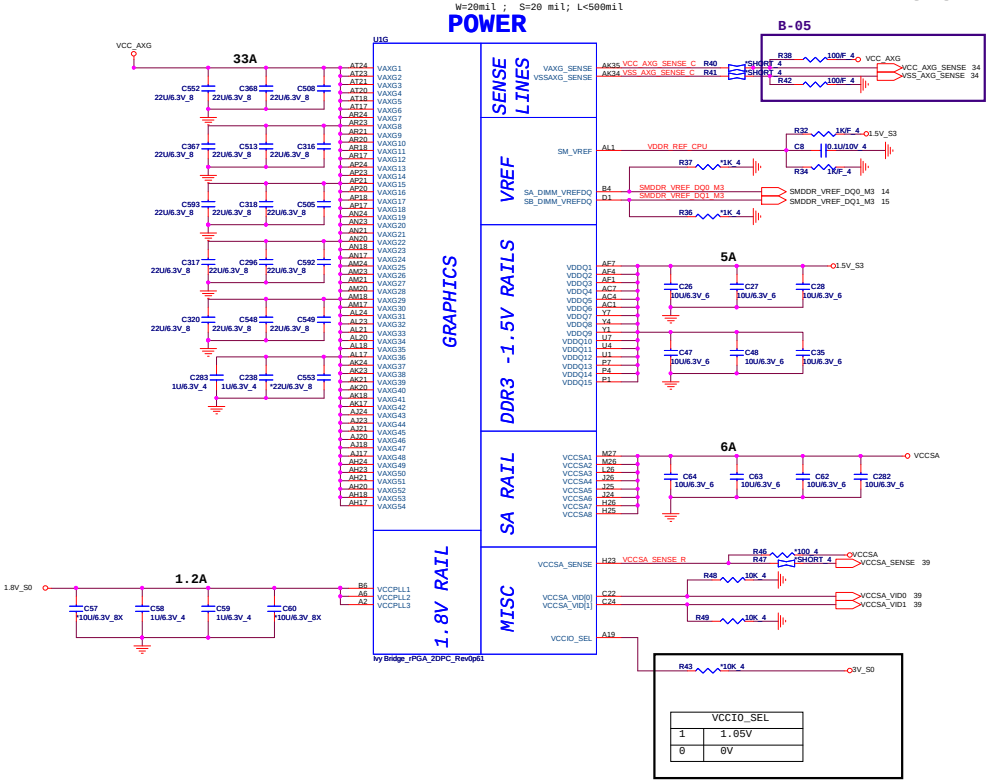
Ivy Bridge Processor (POWER)



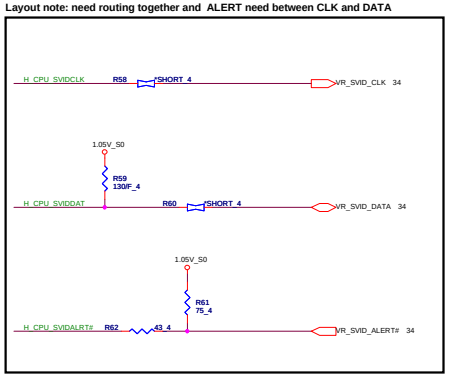
Ivy Bridge Processor (GRAPHIC POWER)

W=20mil ; S=20 mil; L<500mil



VCCIO_SEL	
1	1.05V
0	0V

Layout note: need routing together and ALERT need between CLK and DATA



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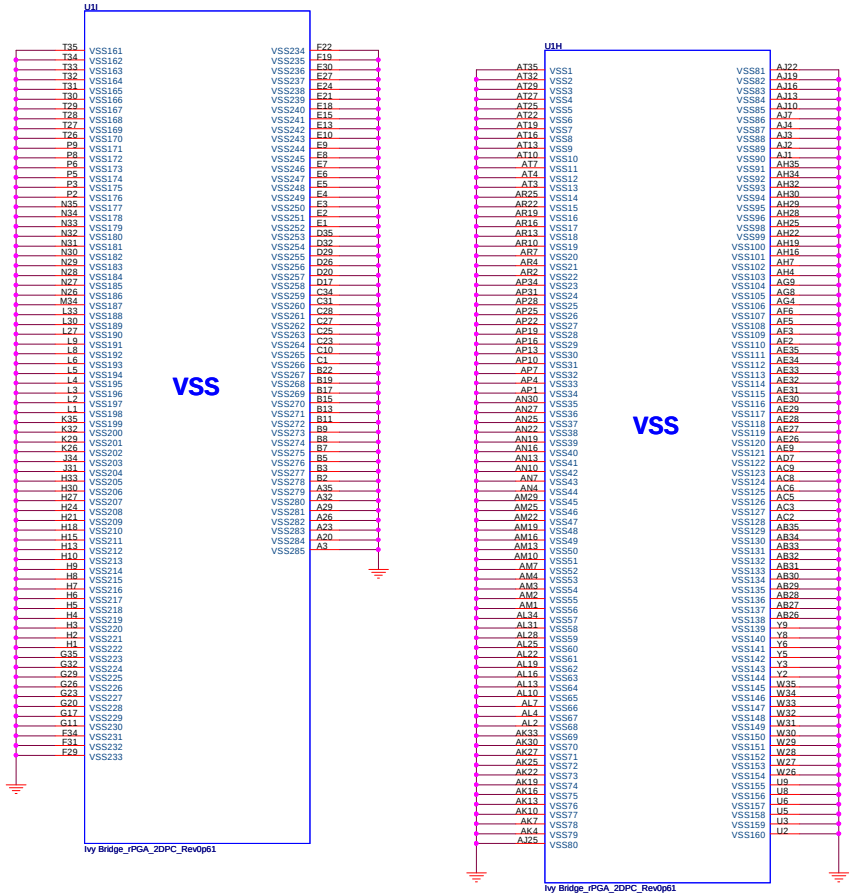
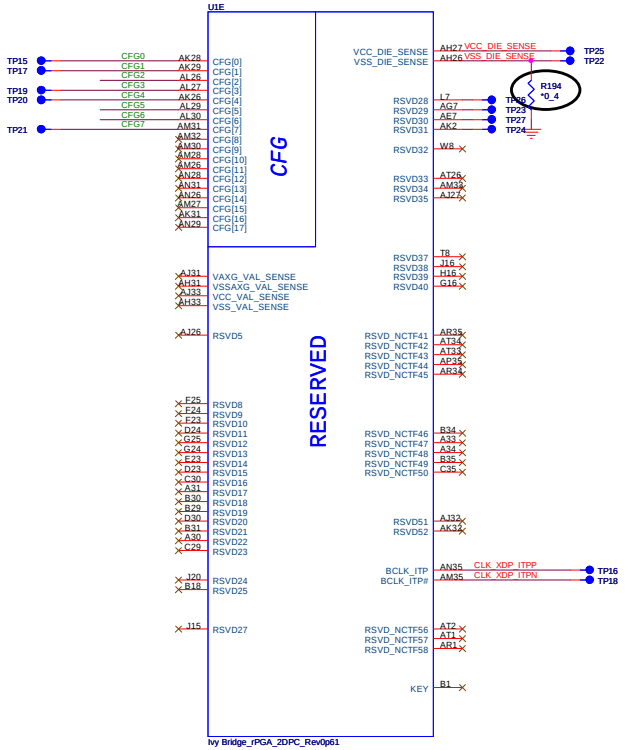
Ivy Bridge Processor (GND)

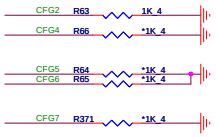


Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

CFG2	0	PCIe X16 LANE Reversed
	1	Normal Operation
CFG3	0	PCIe X4 LANE Reversed
	1	Normal Operation
CFG4	0	Enable; An ext DP device is connected to eDP
	1	Disable; No physical DP attached to eDP
CFG(5:6)	00	1 x 8 , 2 x 4 PCIe
	01	Reserve
	10	2 x 8 PCIe
	11	1 x 16 PCIe
CFG7	0	PEG Wait for BIOS for training
	1	PEG Train immediately following PLT_RST#



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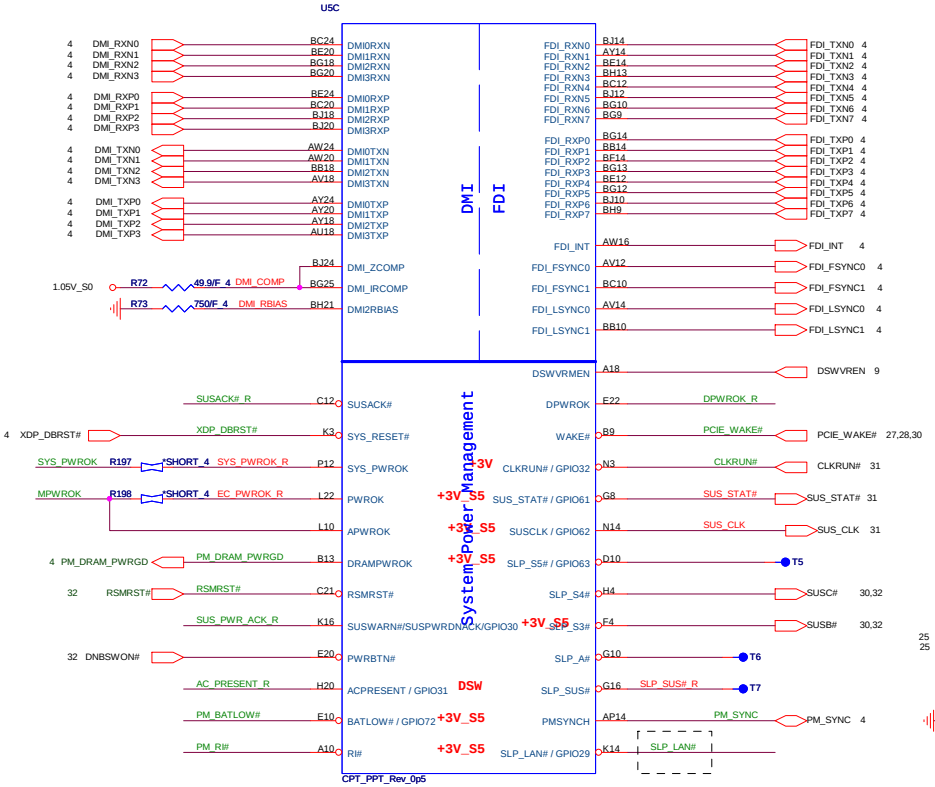
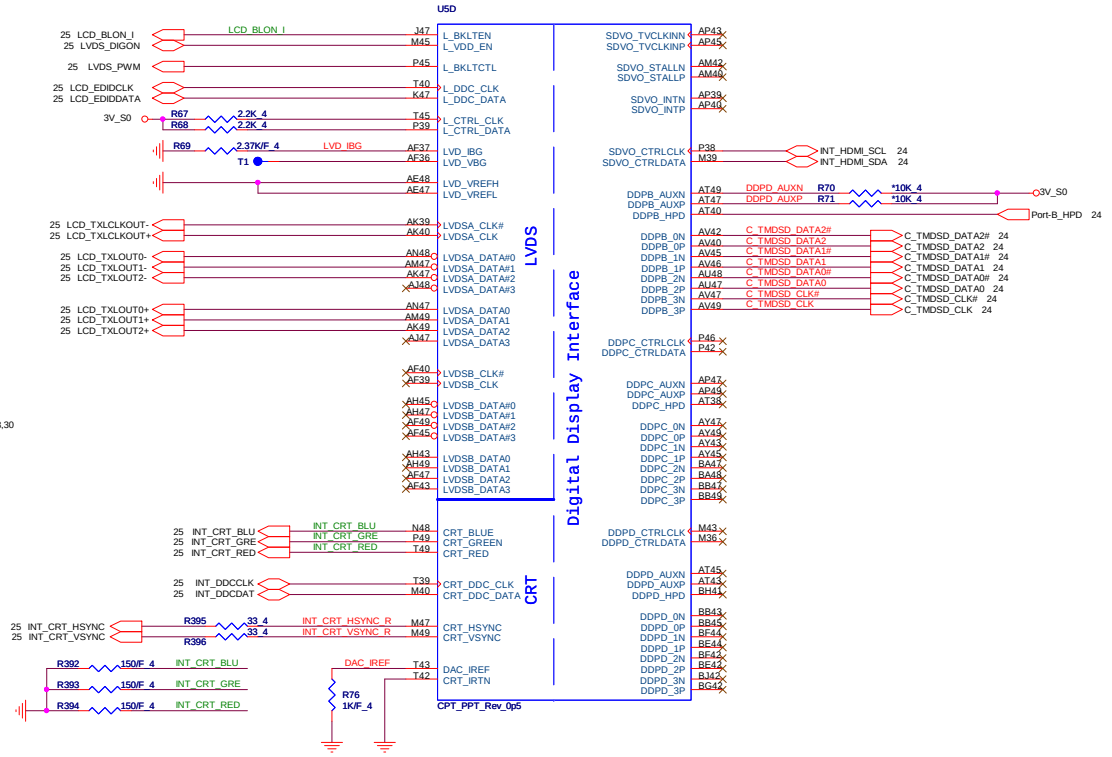
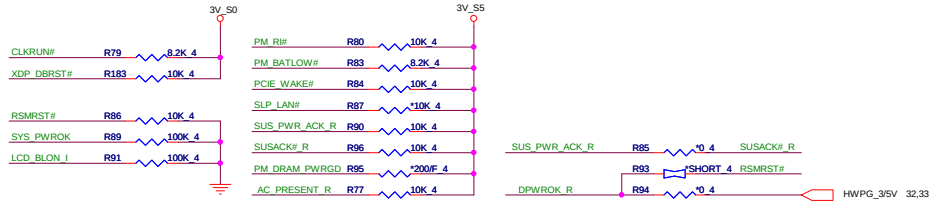
Panther Point (DMI,FDI,PM)



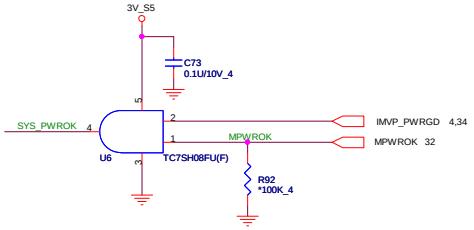
Panther Point (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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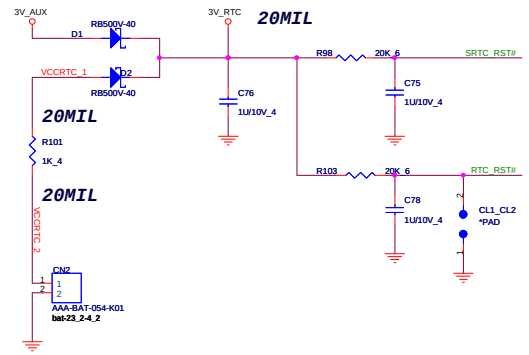
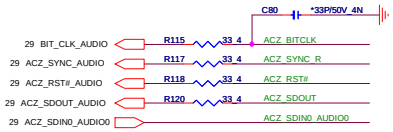
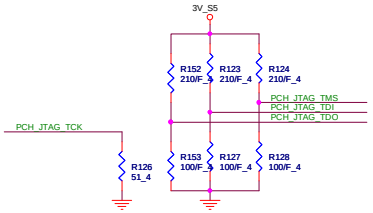
RTC Circuit



HDA Bus



PCH JTAG Debug



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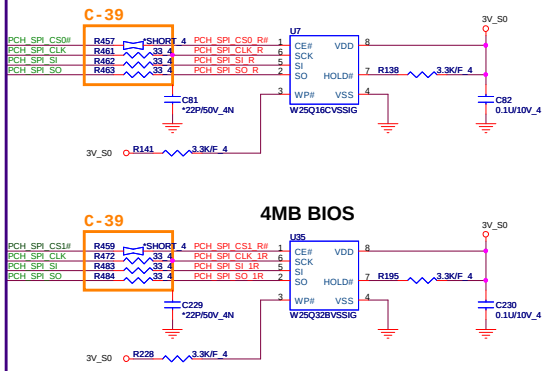
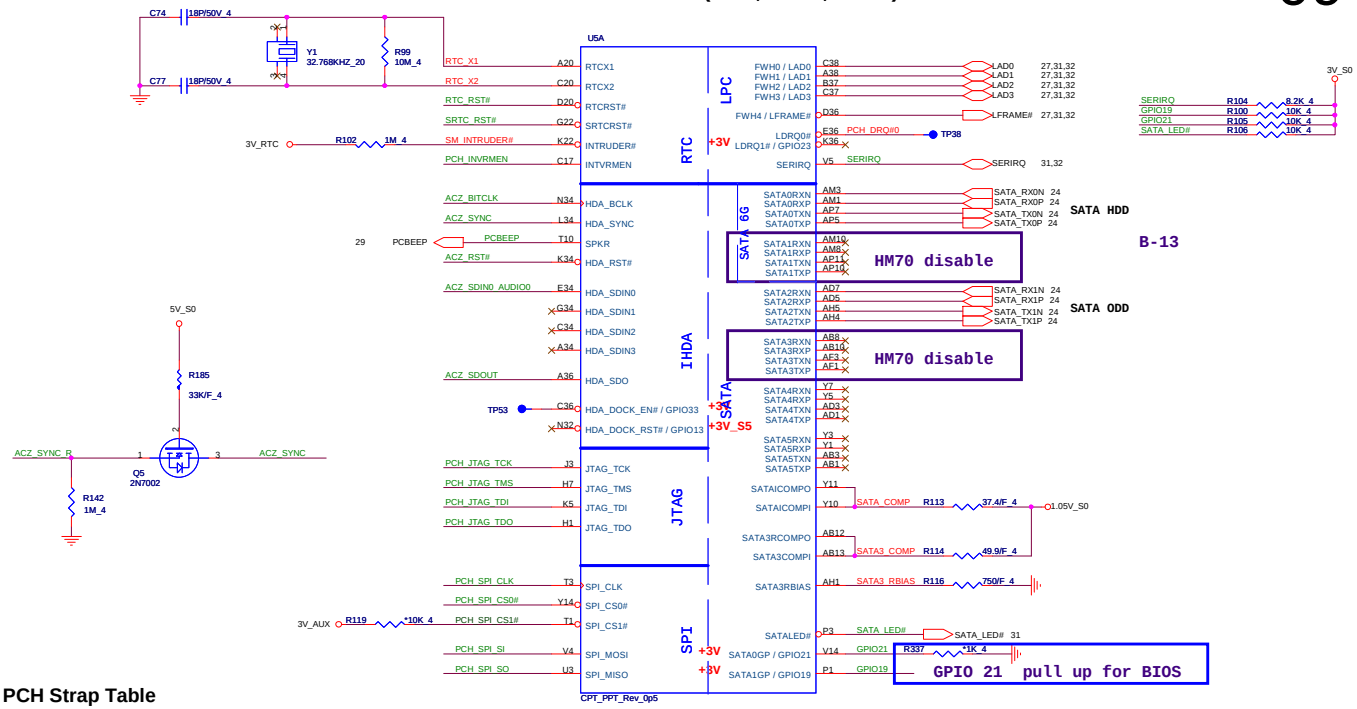
PCH Dual SPI Change from 8MB to 2MB for ME



PCH2

Panther Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V_S0 R121 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R122 *1K_4 PCI_GNT3# 10
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V_RTC R125 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI 0 / 0 / LPC	R129 *1K_4 GNT1# 10 R130 *1K_4 GPIO19
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	1 = Override 0 = Default (weak PD 20K)	3V_S0 R131 *1K_4 ACZ_SDOUT ACZ_SDOUT 32
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R132 2.2K_4 R133 1K_4 1.8V_S0 DF_TVS 11 H_SNB_IVB# 4
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3V_AUX R134 *10K_4 R135 *1K_4 PLL_ODVR_EN 11
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R136 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	3V_S5 R137 *1K_4 GPIO15 11
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN 8 3V_RTC R139 330K_4 R140 *330K_4
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**

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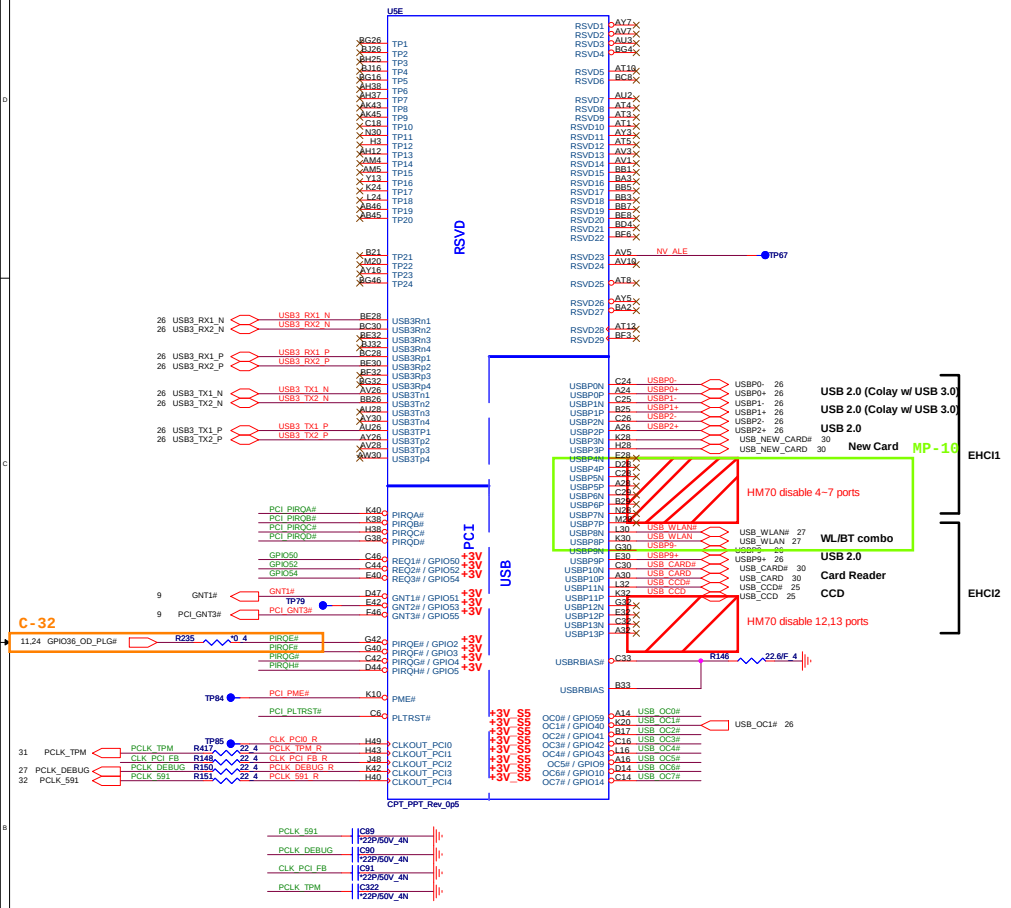
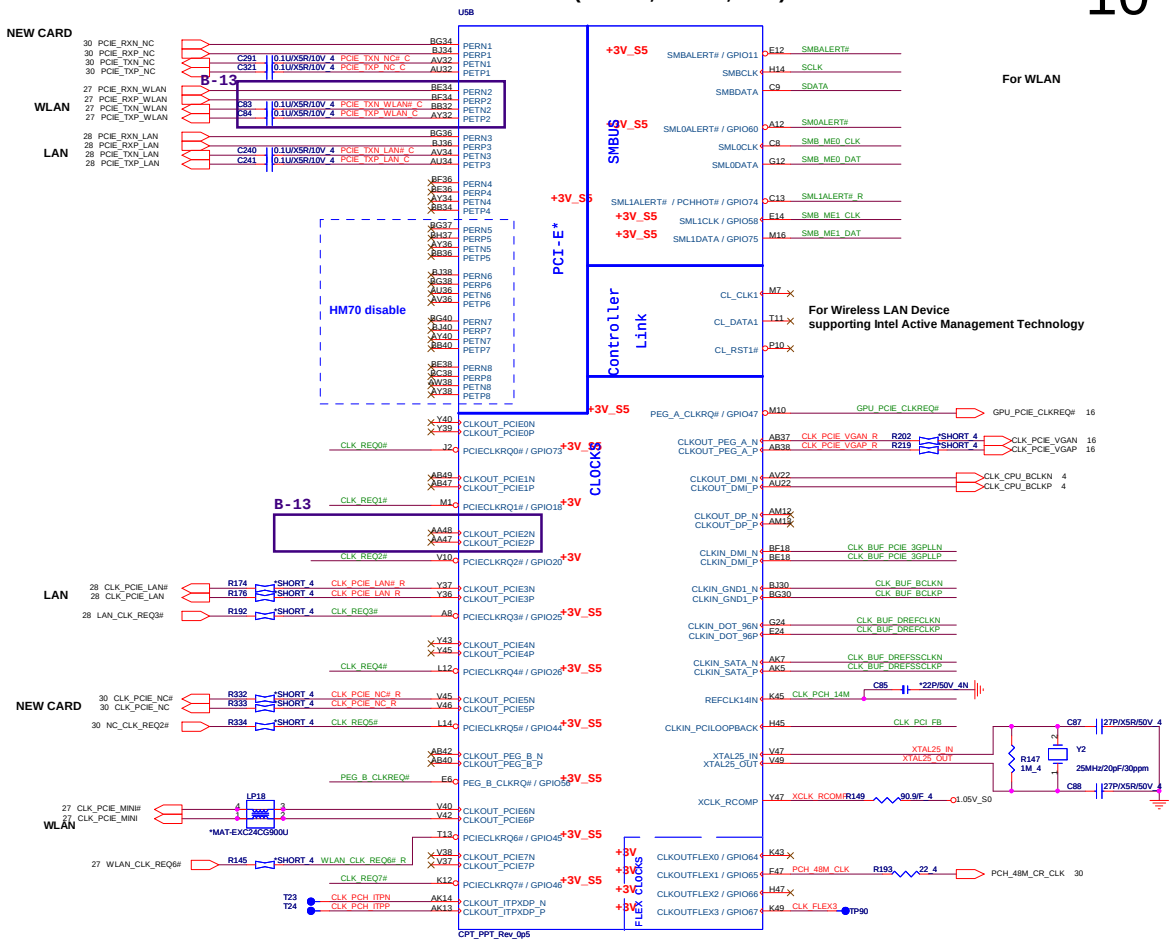
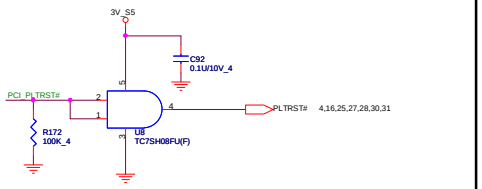
Panther Point-M (PCI,USB,NVRAM)



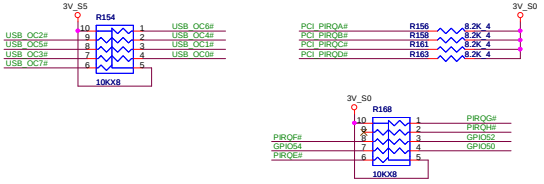
Panther Point-M (PCI-E,SMBUS,CLK)



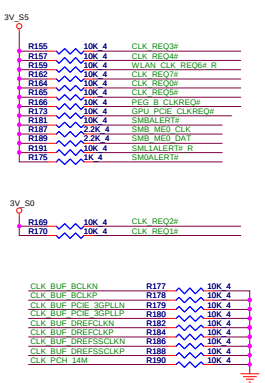
PLTRST#



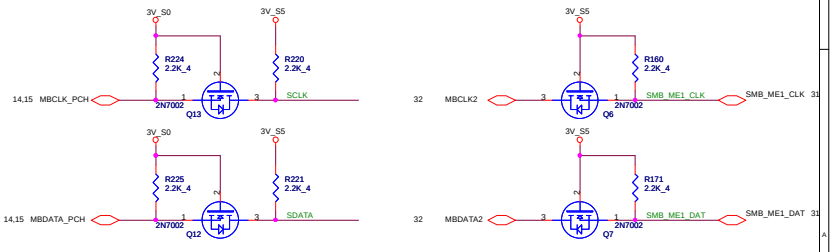
PCI/USBOC# PU



System PU



SMBUS Level Shift



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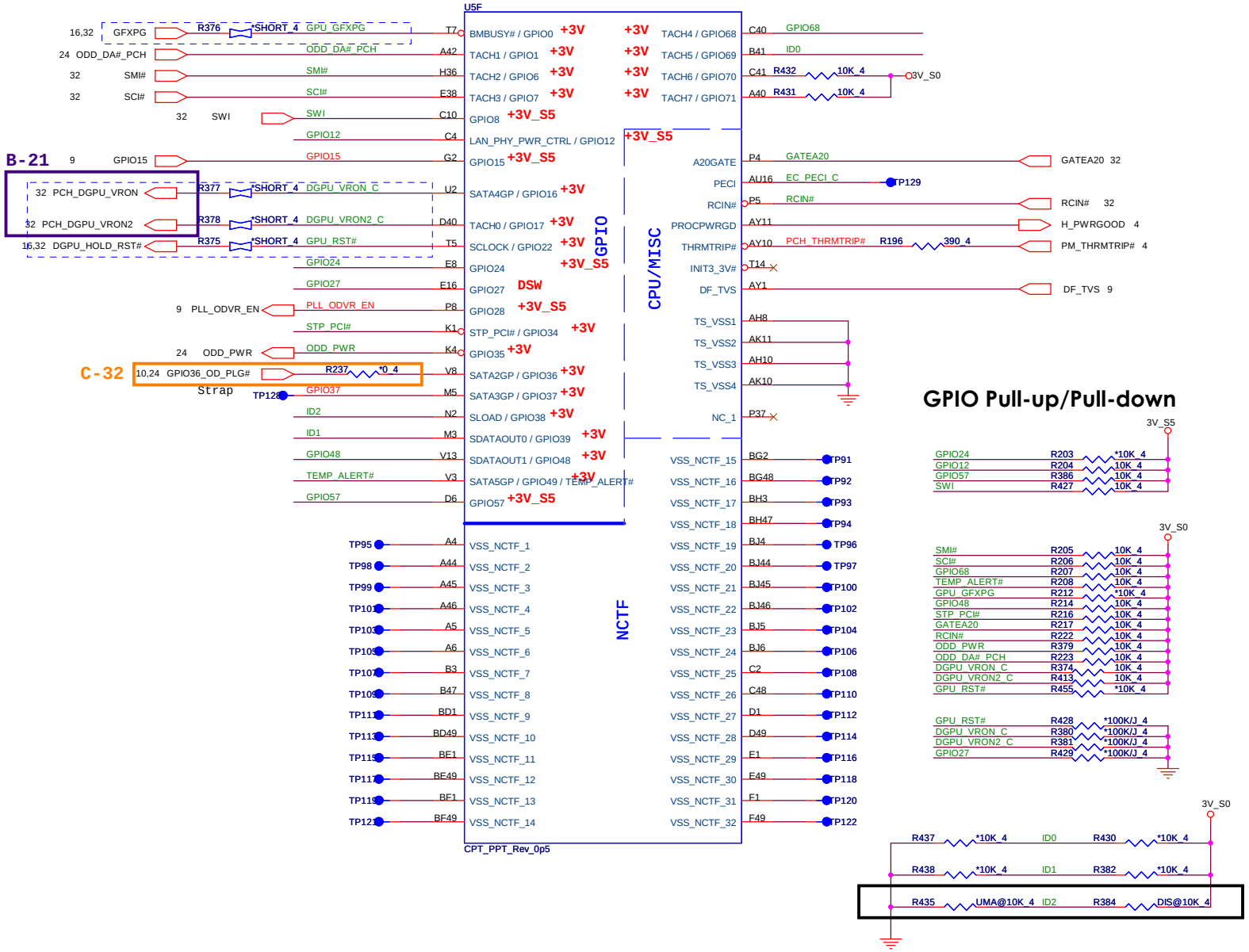
Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down

ID2	ID1	ID0	Model
0	0	0	FJ8 UMA
0	0	1	FJ8 Discrete
0	1	0	FH6 UMA(Consumer)
0	1	1	FH6 UMA(Commercial)
1	0	0	FH6 N13P-LP
1	0	1	FH6 N13P-GLP
1	1	0	TBD
1	1	1	TBD

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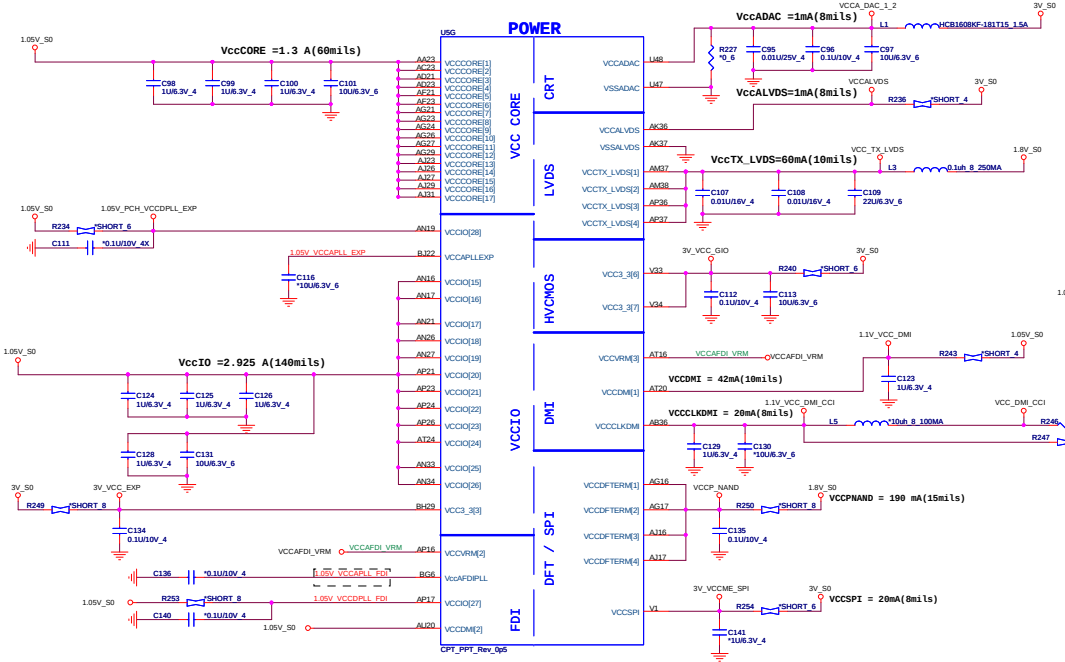
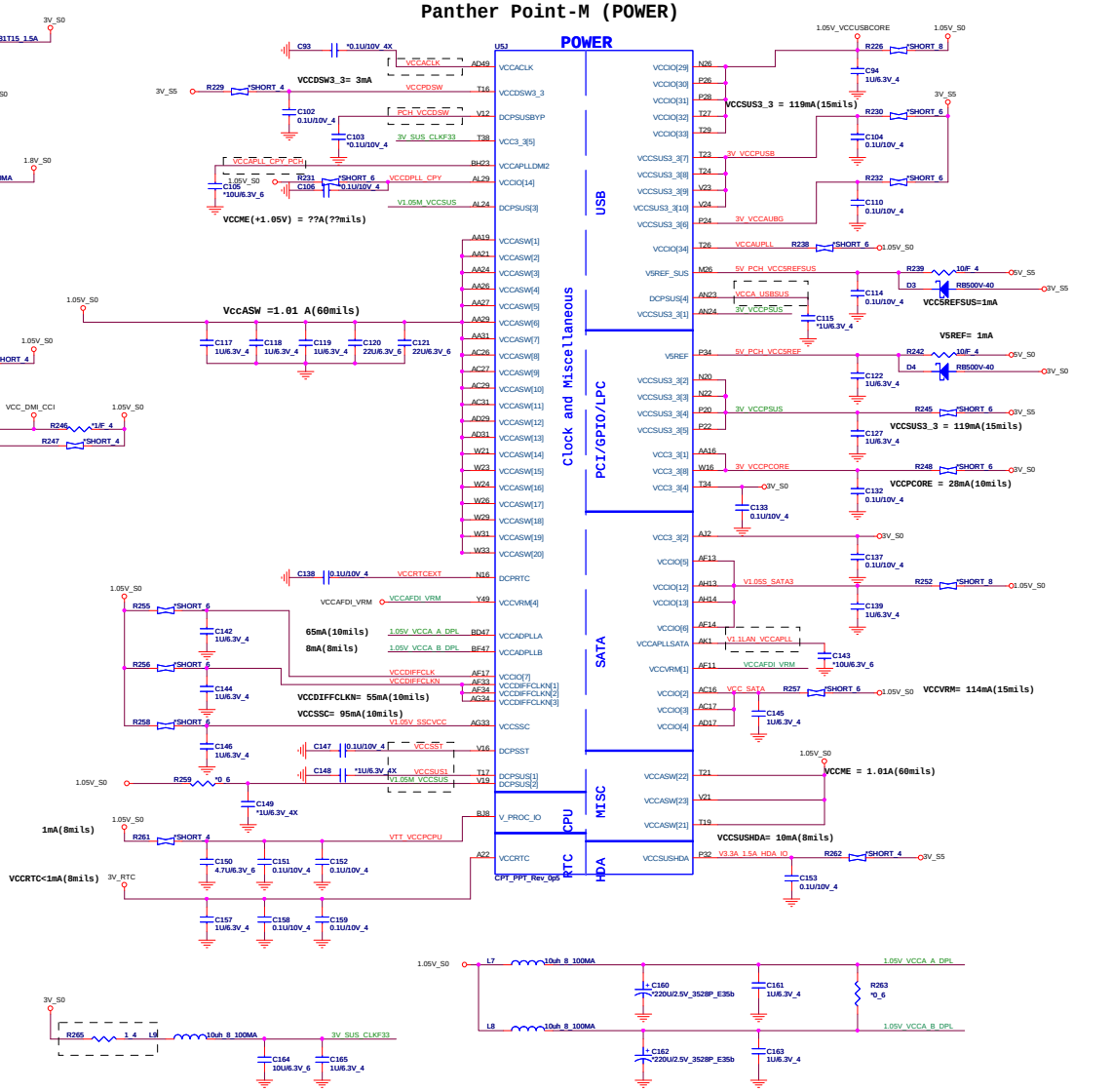
Panther Point (POWER)



Panther Point-M (POWER)



Quanta Computer Inc.
PROJECT : FH6C_HM70

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	Panther Point 5/6	B
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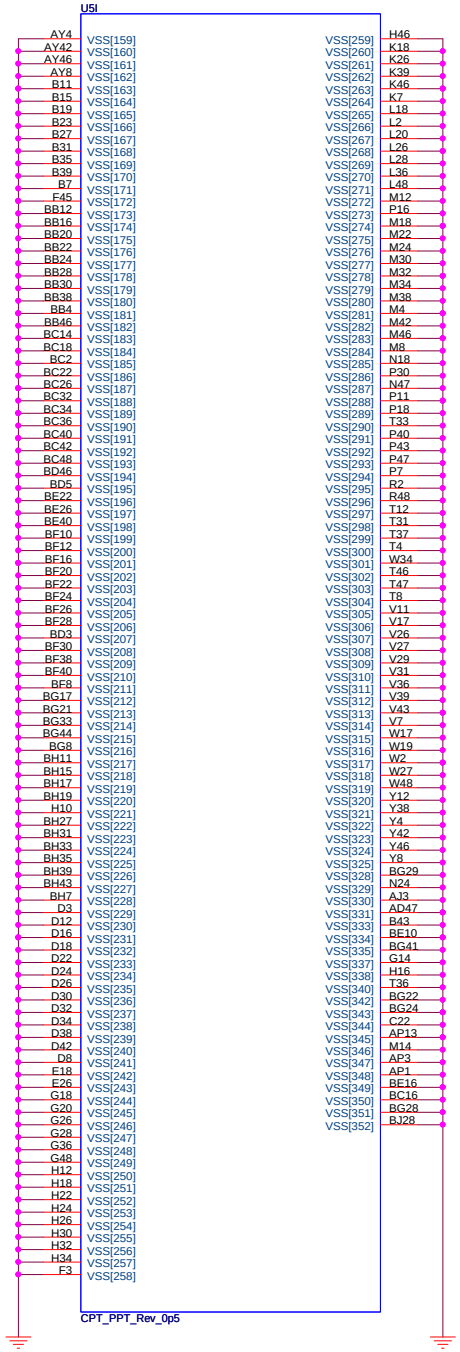
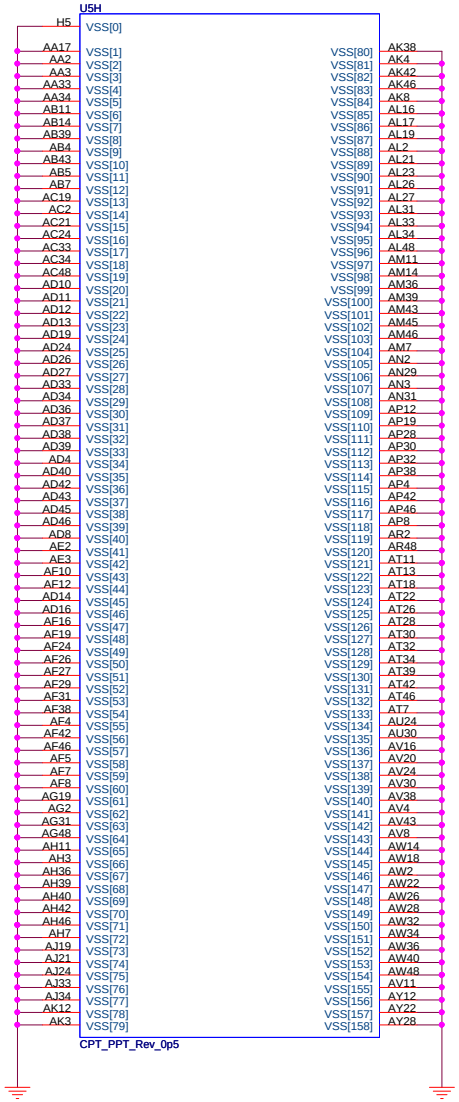
IBEX PEAK-M (GND)





Quanta Computer Inc.

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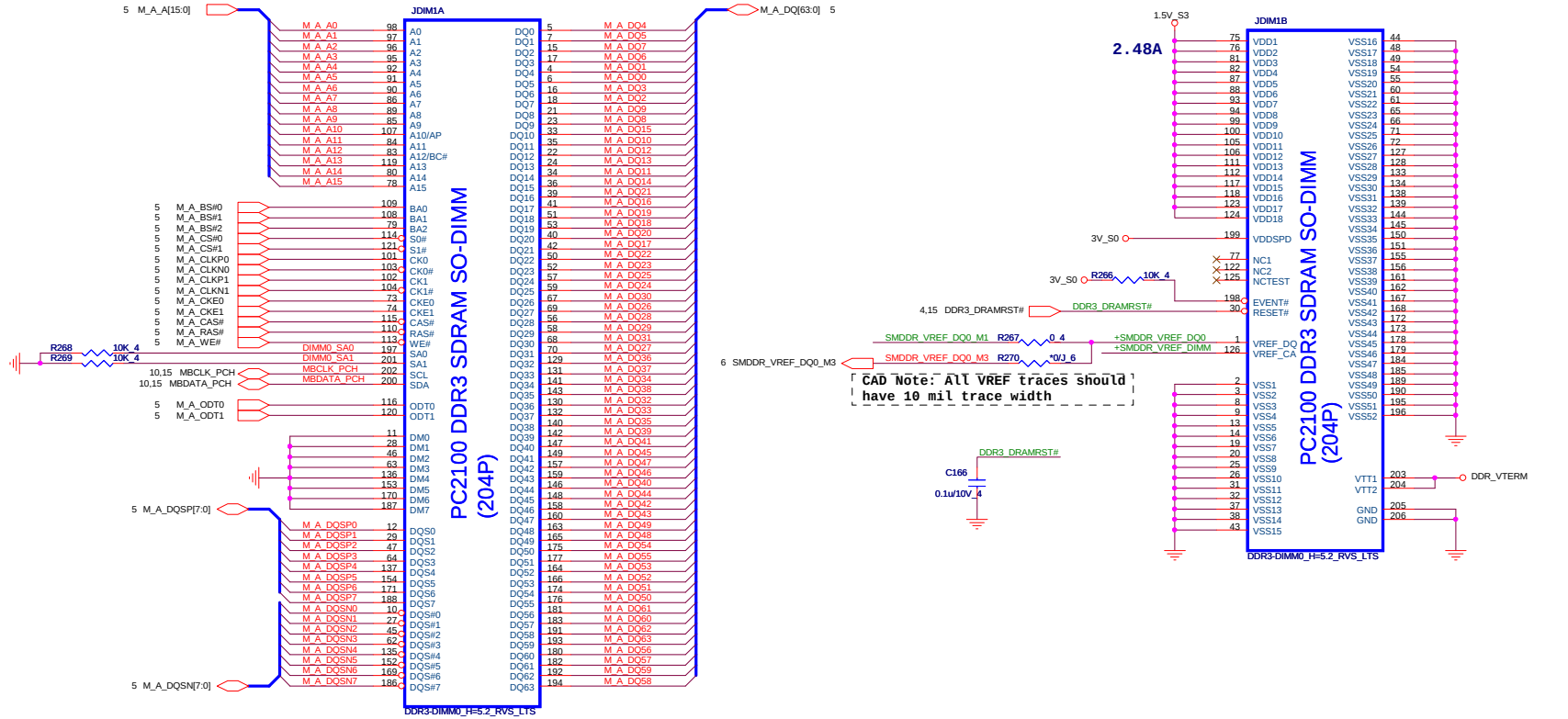
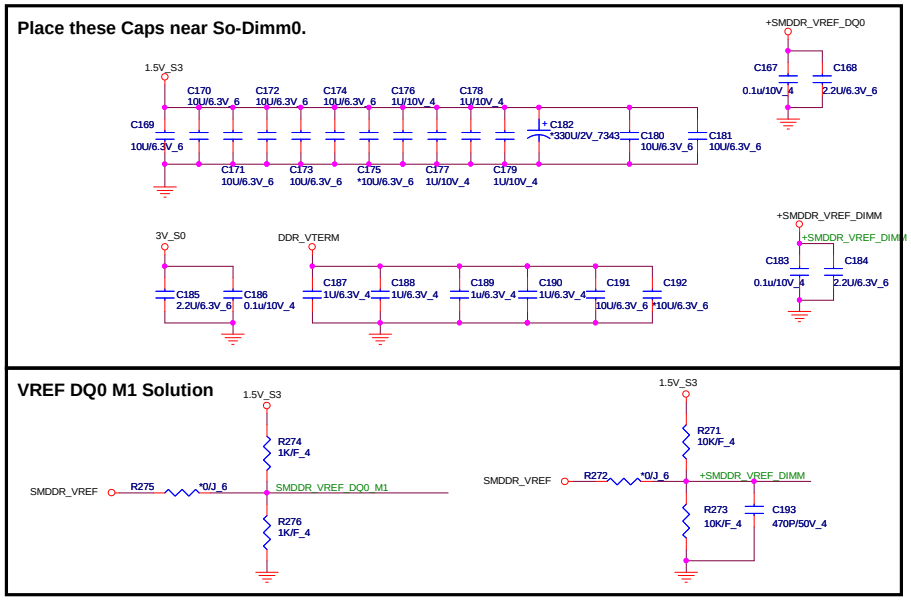
DDR_STD(DDR)





Quanta Computer Inc.

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	DDRIII SO-DIMM-0	B

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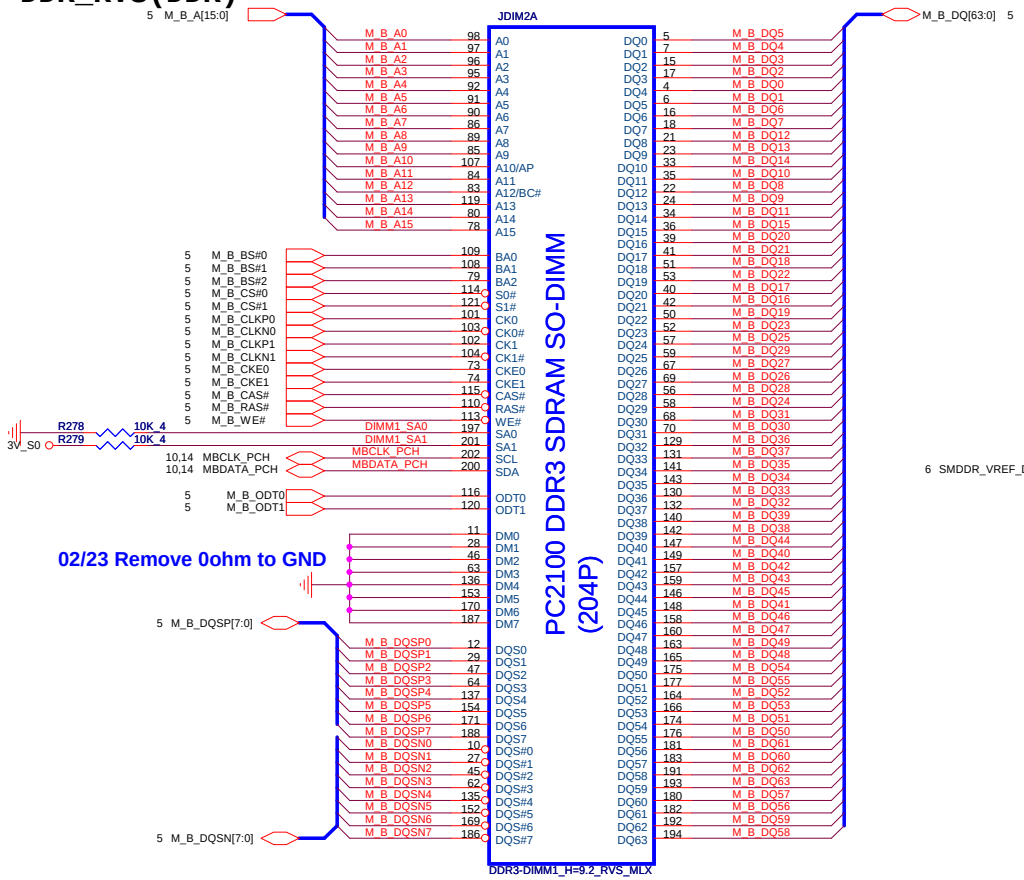
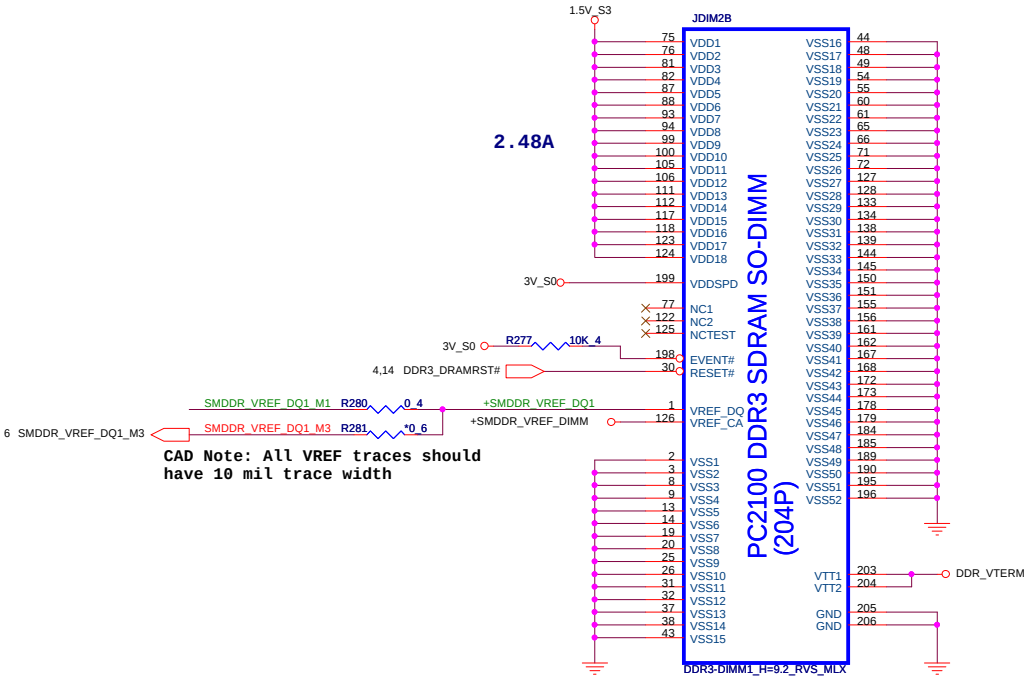
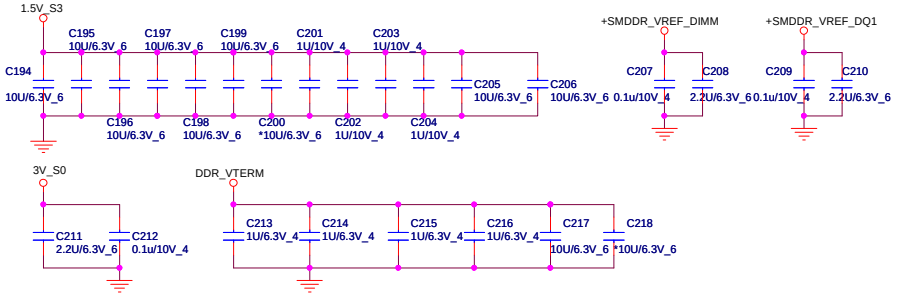
DDR_RVS(DDR)

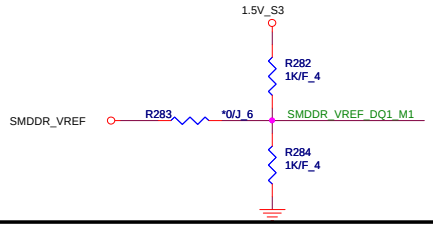




Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



Quanta Computer Inc.		
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Size	Document Number: DDRIII SO-DIMM-1	Rev: B
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U10A
bga908-nvidia-n13p-gs-a1
COMMON
1/19 PCI_EXPRESS

VT1 — PEX_WAKE AJ11
PLTRST_DIS# — PEX_RST AJ12
PCIE_CLKREQ_PEG# O — PEX_CLKREQ AK12
10 CLK_PCIE_VGAP — PEX_REFCLK AL13
10 CLK_PCIE_VGAN — PEX_REFCLK# AK13

4 PEG_RXP0	VC9	DIS@0.22U/x5R/10V_4	GFX_RXP0_C	AK14	PEX_TX0
4 PEG_RXN0	VC10	DIS@0.22U/x5R/10V_4	GFX_RXN0_C	AJ14	PEX_TX0#
4 PEG_TXP0				AN12	PEX_RX0
4 PEG_TXN0				AM12	PEX_RX0#
4 PEG_RXP1	VC13	DIS@0.22U/x5R/10V_4	GFX_RXP1_C	AH14	PEX_TX1
4 PEG_RXN1	VC4	DIS@0.22U/x5R/10V_4	GFX_RXN1_C	AG14	PEX_TX1#
4 PEG_TXP1				AN14	PEX_RX1
4 PEG_TXN1				AM14	PEX_RX1#
4 PEG_RXP2	VC6	DIS@0.22U/x5R/10V_4	GFX_RXP2_C	AK15	PEX_TX2
4 PEG_RXN2	VC16	DIS@0.22U/x5R/10V_4	GFX_RXN2_C	AJ15	PEX_TX2#
4 PEG_TXP2				AP14	PEX_RX2
4 PEG_TXN2				AP15	PEX_RX2#
4 PEG_RXP3	VC20	DIS@0.22U/x5R/10V_4	GFX_RXP3_C	AL16	PEX_TX3
4 PEG_RXN3	VC22	DIS@0.22U/x5R/10V_4	GFX_RXN3_C	AK16	PEX_TX3#
4 PEG_TXP3				AN15	PEX_RX3
4 PEG_TXN3				AM15	PEX_RX3#
4 PEG_RXP4	VC23	DIS@0.22U/x5R/10V_4	GFX_RXP4_C	AK17	PEX_TX4
4 PEG_RXN4	VC24	DIS@0.22U/x5R/10V_4	GFX_RXN4_C	AJ17	PEX_TX4#
4 PEG_TXP4				AN17	PEX_RX4
4 PEG_TXN4				AM17	PEX_RX4#
4 PEG_RXP5	VC25	DIS@0.22U/x5R/10V_4	GFX_RXP5_C	AH17	PEX_TX5
4 PEG_RXN5	VC26	DIS@0.22U/x5R/10V_4	GFX_RXN5_C	AG17	PEX_TX5#
4 PEG_TXP5				AP17	PEX_RX5
4 PEG_TXN5				AP18	PEX_RX5#
4 PEG_RXP6	VC28	DIS@0.22U/x5R/10V_4	GFX_RXP6_C	AK18	PEX_TX6
4 PEG_RXN6	VC30	DIS@0.22U/x5R/10V_4	GFX_RXN6_C	AJ18	PEX_TX6#
4 PEG_TXP6				AN18	PEX_RX6
4 PEG_TXN6				AM18	PEX_RX6#
4 PEG_RXP7	VC32	DIS@0.22U/x5R/10V_4	GFX_RXP7_C	AL19	PEX_TX7
4 PEG_RXN7	VC33	DIS@0.22U/x5R/10V_4	GFX_RXN7_C	AK19	PEX_TX7#
4 PEG_TXP7				AN20	PEX_RX7
4 PEG_TXN7				AM20	PEX_RX7#
4 PEG_RXP8	VC34	DIS@0.22U/x5R/10V_4	GFX_RXP8_C	AK20	PEX_TX8
4 PEG_RXN8	VC35	DIS@0.22U/x5R/10V_4	GFX_RXN8_C	AJ20	PEX_TX8#
4 PEG_TXP8				AP20	PEX_RX8
4 PEG_TXN8				AP21	PEX_RX8#
4 PEG_RXP9	VC36	DIS@0.22U/x5R/10V_4	GFX_RXP9_C	AH20	PEX_TX9
4 PEG_RXN9	VC37	DIS@0.22U/x5R/10V_4	GFX_RXN9_C	AG20	PEX_TX9#
4 PEG_TXP9				AN21	PEX_RX9
4 PEG_TXN9				AM21	PEX_RX9#
4 PEG_RXP10	VC39	DIS@0.22U/x5R/10V_4	GFX_RXP10_C	AK21	PEX_TX10
4 PEG_RXN10	VC40	DIS@0.22U/x5R/10V_4	GFX_RXN10_C	AJ21	PEX_TX10#
4 PEG_TXP10				AN23	PEX_RX10
4 PEG_TXN10				AM23	PEX_RX10#
4 PEG_RXP11	VC42	DIS@0.22U/x5R/10V_4	GFX_RXP11_C	AL22	PEX_TX11
4 PEG_RXN11	VC43	DIS@0.22U/x5R/10V_4	GFX_RXN11_C	AK22	PEX_TX11#
4 PEG_TXP11				AP23	PEX_RX11
4 PEG_TXN11				AP24	PEX_RX11#
4 PEG_RXP12	VC44	DIS@0.22U/x5R/10V_4	GFX_RXP12_C	AK23	PEX_TX12
4 PEG_RXN12	VC46	DIS@0.22U/x5R/10V_4	GFX_RXN12_C	AJ23	PEX_TX12#
4 PEG_TXP12				AN24	PEX_RX12
4 PEG_TXN12				AM24	PEX_RX12#
4 PEG_RXP13	VC51	DIS@0.22U/x5R/10V_4	GFX_RXP13_C	AH23	PEX_TX13
4 PEG_RXN13	VC52	DIS@0.22U/x5R/10V_4	GFX_RXN13_C	AG23	PEX_TX13#
4 PEG_TXP13				AN26	PEX_RX13
4 PEG_TXN13				AM26	PEX_RX13#
4 PEG_RXP14	VC56	DIS@0.22U/x5R/10V_4	GFX_RXP14_C	AK24	PEX_TX14
4 PEG_RXN14	VC57	DIS@0.22U/x5R/10V_4	GFX_RXN14_C	AJ24	PEX_TX14#
4 PEG_TXP14				AP26	PEX_RX14
4 PEG_TXN14				AP27	PEX_RX14#
4 PEG_RXP15	VC58	DIS@0.22U/x5R/10V_4	GFX_RXP15_C	AL25	PEX_TX15
4 PEG_RXN15	VC59	DIS@0.22U/x5R/10V_4	GFX_RXN15_C	AK25	PEX_TX15#
4 PEG_TXP15				AN27	PEX_RX15
4 PEG_TXN15				AM27	PEX_RX15#

PEX_IOVDD AG19, AG21, AG22, AG24, AH21, AH25 — 1.05V_GPU
VC1 DIS@1U/10V_4; VC7 DIS@1U/10V_4; VC8 DIS@4.7U/6.3V_6; VC2 DIS@10U/6.3V_6; VC3 DIS@10U/6.3V_6; VC11 DIS@22U/6.3V_6; VC12 DIS@22U/6.3V_6

PEX_IOVDD AG13, AG15, AG16, AG18, AG25, AH15, AH18, AH26, AH27, AJ27, AK27, AL27, AM28, AN28 — 1.05V_GPU
VC14 DIS@1U/10V_4; VC5 DIS@1U/10V_4; VC15 DIS@4.7U/6.3V_6; VC17 DIS@10U/6.3V_6; VC18 DIS@10U/6.3V_6; VC19 DIS@22U/6.3V_6; VC21 DIS@22U/6.3V_6

B-18
PEX_PLL_HVDD AH12 — VR22 LP@0R_6 — 3V_GPU
PEX_SVDD_3V3 AG12 — 3V_GPU
VC27 DIS@0.1u/10V_4; VC29 DIS@4.7U/6.3V_6; VC31 DIS@4.7U/6.3V_6

VDD_SENSE L4 — VDD_SENSE 40
GND_SENSE L5 — GND_SENSE 40
3V3AUX_NC P8 — VT2

PEX_TSTCLK_OUT AJ26 — VR2 *DIS@200/F_4 — PEX_TSTCLK_OUT AK26

VL3 DIS@BLM18P121SN — 1.05V_GPU
PEX_PLLVDD AG25 — VC53 DIS@0.1u/10V_4; VC54 DIS@1U/6.3V_4; VC55 DIS@4.7U/6.3V_6

TESTMODE AK11 — VR5 DIS@10K/F_4

PEX_TERMP AP29 — VR7 DIS@2.49K/F_4

1.05V_GPU — VL1 *SHORT_6 — VC38 DIS@0.1u/10V_4; VC41 DIS@22U/6.3V_6

U10O
bga908-nvidia-n13p-gs-a1
COMMON
12/19 XTAL_PLL

1.05V_GPU — VL2 *SHORT_6 — VC45 DIS@0.1u/10V_4; VC47 DIS@0.1u/10V_4; VC48 DIS@1U/6.3V_4; VC49 DIS@4.7U/6.3V_6; VC50 DIS@22U/6.3V_6

AD8 PLLVDD; AE8 SP_PLLVDD; AD7 VID_PLLVDD; NC; GF108/GKx; GF117

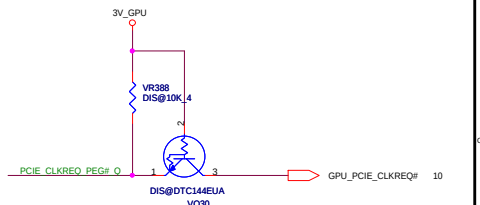
H1 XTALSSIN — VR3 DIS@10K/F_4
H3 XTALIN — VR6 DIS@0_4
XTALOUTBUFF J4 — VR4 DIS@10K/F_4
XTALOUT H2
VY1 1 2 DIS@27MHZ/20ppm

B-17
VC60 DIS@27P/X5R/50V_4; VC61 DIS@27P/X5R/50V_4

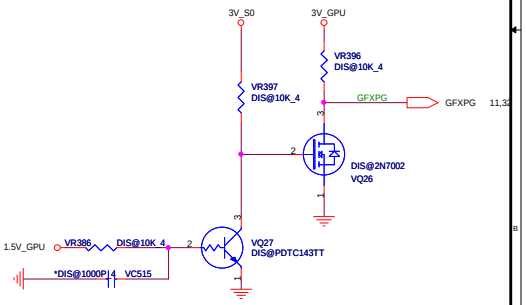
	N13P-GLP	N13P-LP
VL3	BLM18P121SN (CX8PG121009)	0ohm_0603 (CS00003J951)

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

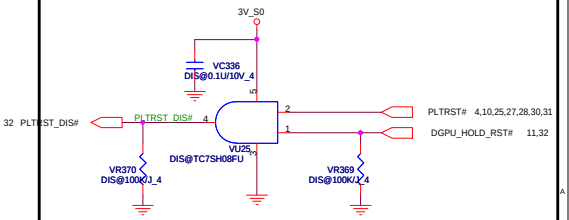
CLK REQ



GPU all PWROK



GPU RST#



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Size	Document Number	Rev
	N13P PCIE	B
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22 FBA_DQ[0..63]
22 FBA_DQM[0..7]
22 FBA_WDQSP[0..7]
22 FBA_RDQSN[0..7]
22 FBA_CMD[0..31]

23 FBB_DQ[0..63]
23 FBB_DQM[0..7]
23 FBB_WDQSP[0..7]
23 FBB_RDQSN[0..7]
23 FBB_CMD[0..31]

U10B
bga908-nvidia-n13p-gs-a1
COMMON
2/19 FBA

U10C
bga908-nvidia-n13p-gs-a1
COMMON
3/19 FBB

	N13P-GLP	N13P-LP
VR111	NA	10Kohm_0402 (CS31002FB26)

VR111 LP@10K_4

FB_CLAMP E1
FB_DLL_AVDD K27 FBA_PLL_AVDD
VC62 DIS@0.1u/10V_4

FBA_DQ0 L28 FBA_D0
FBA_DQ1 M29 FBA_D1
FBA_DQ2 L29 FBA_D2
FBA_DQ3 M28 FBA_D3
FBA_DQ4 N31 FBA_D4
FBA_DQ5 P29 FBA_D5
FBA_DQ6 R29 FBA_D6
FBA_DQ7 P28 FBA_D7
FBA_DQ8 J28 FBA_D8
FBA_DQ9 H29 FBA_D9
FBA_DQ10 J29 FBA_D10
FBA_DQ11 H28 FBA_D11
FBA_DQ12 G29 FBA_D12
FBA_DQ13 E31 FBA_D13
FBA_DQ14 E32 FBA_D14
FBA_DQ15 F30 FBA_D15
FBA_DQ16 C34 FBA_D16
FBA_DQ17 D32 FBA_D17
FBA_DQ18 B33 FBA_D18
FBA_DQ19 C33 FBA_D19
FBA_DQ20 F33 FBA_D20
FBA_DQ21 F32 FBA_D21
FBA_DQ22 H33 FBA_D22
FBA_DQ23 H32 FBA_D23
FBA_DQ24 P34 FBA_D24
FBA_DQ25 P32 FBA_D25
FBA_DQ26 P31 FBA_D26
FBA_DQ27 P33 FBA_D27
FBA_DQ28 L31 FBA_D28
FBA_DQ29 L34 FBA_D29
FBA_DQ30 L32 FBA_D30
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FBA_DQ33 AF29 FBA_D33
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FBA_DQ36 AD30 FBA_D36
FBA_DQ37 AD29 FBA_D37
FBA_DQ38 AC29 FBA_D38
FBA_DQ39 AD28 FBA_D39
FBA_DQ40 AJ29 FBA_D40
FBA_DQ41 AK29 FBA_D41
FBA_DQ42 AJ30 FBA_D42
FBA_DQ43 AK28 FBA_D43
FBA_DQ44 AM29 FBA_D44
FBA_DQ45 AM31 FBA_D45
FBA_DQ46 AN29 FBA_D46
FBA_DQ47 AM30 FBA_D47
FBA_DQ48 AN31 FBA_D48
FBA_DQ49 AN32 FBA_D49
FBA_DQ50 AP30 FBA_D50
FBA_DQ51 AP32 FBA_D51
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FBA_DQ58 AC30 FBA_D58
FBA_DQ59 AD33 FBA_D59
FBA_DQ60 AF31 FBA_D60
FBA_DQ61 AG34 FBA_D61
FBA_DQ62 AG32 FBA_D62
FBA_DQ63 AG33 FBA_D63

FBA_DQM0 P30 FBA_DQM0
FBA_DQM1 F31 FBA_DQM1
FBA_DQM2 F34 FBA_DQM2
FBA_DQM3 M32 FBA_DQM3
FBA_DQM4 AD31 FBA_DQM4
FBA_DQM5 AL29 FBA_DQM5
FBA_DQM6 AM32 FBA_DQM6
FBA_DQM7 AF34 FBA_DQM7

FBA_WDQSP0 M31 FBA_DQS_WP0
FBA_WDQSP1 G31 FBA_DQS_WP1
FBA_WDQSP2 E33 FBA_DQS_WP2
FBA_WDQSP3 M33 FBA_DQS_WP3
FBA_WDQSP4 AE31 FBA_DQS_WP4
FBA_WDQSP5 AK30 FBA_DQS_WP5
FBA_WDQSP6 AN33 FBA_DQS_WP6
FBA_WDQSP7 AF33 FBA_DQS_WP7

FBA_RDQSN0 M30 FBA_DQS_RN0
FBA_RDQSN1 H30 FBA_DQS_RN1
FBA_RDQSN2 E34 FBA_DQS_RN2
FBA_RDQSN3 M34 FBA_DQS_RN3
FBA_RDQSN4 AF30 FBA_DQS_RN4
FBA_RDQSN5 AK31 FBA_DQS_RN5
FBA_RDQSN6 AM34 FBA_DQS_RN6
FBA_RDQSN7 AF32 FBA_DQS_RN7

H26 FB_VREF

FBA_CMD0 U30 FBA_CMD0
FBA_CMD1 T31 FBA_CMD1 — VT3
FBA_CMD2 U29 FBA_CMD2
FBA_CMD3 R34 FBA_CMD3
FBA_CMD4 R33 FBA_CMD4
FBA_CMD5 U32 FBA_CMD5
FBA_CMD6 U33 FBA_CMD6
FBA_CMD7 U28 FBA_CMD7
FBA_CMD8 V28 FBA_CMD8
FBA_CMD9 V29 FBA_CMD9
FBA_CMD10 V30 FBA_CMD10
FBA_CMD11 U34 FBA_CMD11
FBA_CMD12 U31 FBA_CMD12
FBA_CMD13 V34 FBA_CMD13
FBA_CMD14 V33 FBA_CMD14
FBA_CMD15 V32 FBA_CMD15
FBA_CMD16 AA31 FBA_CMD16
FBA_CMD17 AA29 FBA_CMD17 — VT5
FBA_CMD18 AA28 FBA_CMD18
FBA_CMD19 AC34 FBA_CMD19
FBA_CMD20 AC33 FBA_CMD20
FBA_CMD21 AA32 FBA_CMD21
FBA_CMD22 AA33 FBA_CMD22
FBA_CMD23 Y28 FBA_CMD23
FBA_CMD24 Y29 FBA_CMD24
FBA_CMD25 W31 FBA_CMD25
FBA_CMD26 Y30 FBA_CMD26
FBA_CMD27 AA34 FBA_CMD27
FBA_CMD28 Y31 FBA_CMD28
FBA_CMD29 Y34 FBA_CMD29
FBA_CMD30 Y33 FBA_CMD30
FBA_CMD31 V31 FBA_CMD31 — VT7

FBA_CMD_RFU0 R32 — VT9
FBA_CMD_RFU1 AC32 — VT10

FBA_CMD2 VR8 DIS@10K_4 FBA_ODT_L
FBA_CMD18 VR10 DIS@10K_4 FBA_ODT_H
FBA_CMD3 VR12 DIS@10K_4 FBA_CKE_L
FBA_CMD19 VR14 DIS@10K_4 FBA_CKE_H
FBA_CMD5 VR16 DIS@10K_4 FBA_RST#

Debug
1.5V_GPU
FBA_DEBUG0 R28 FBA_DEBUG0 — VR18 *DIS@60.4/F_4
FBA_DEBUG1 AC28 FBA_DEBUG1 — VR19 *DIS@60.4/F_4

FBA_CLK0 R30 — FBA_CLK0 22
FBA_CLK0 R31 — FBA_CLK#0 22
FBA_CLK1 AB31 — FBA_CLK1 22
FBA_CLK1 AC31 — FBA_CLK#1 22

FBA_WCK01 K31
FBA_WCK01 L30
FBA_WCK23 H34
FBA_WCK23 J34
FBA_WCK45 AG30
FBA_WCK45 AG31
FBA_WCK67 AJ34
FBA_WCK67 AK34

FBA_WCKB01 J30
FBA_WCKB01 J31
FBA_WCKB23 J32
FBA_WCKB23 J33
FBA_WCKB45 AH31
FBA_WCKB45 AJ31
FBA_WCKB67 AJ32
FBA_WCKB67 AJ33

FBA_PLL_AVDD U27 FBA_PLL_AVDD — VL4 *SHORT_6 — 1.05V_GPU
VC64 DIS@0.1u/10V_4
VC65 DIS@22u/6.3V_6

B-07

FBB_DQ0 G9 FBB_D0
FBB_DQ1 E9 FBB_D1
FBB_DQ2 G8 FBB_D2
FBB_DQ3 F9 FBB_D3
FBB_DQ4 E11 FBB_D4
FBB_DQ5 G11 FBB_D5
FBB_DQ6 F12 FBB_D6
FBB_DQ7 G12 FBB_D7
FBB_DQ8 G6 FBB_D8
FBB_DQ9 F5 FBB_D9
FBB_DQ10 E6 FBB_D10
FBB_DQ11 F6 FBB_D11
FBB_DQ12 F4 FBB_D12
FBB_DQ13 G4 FBB_D13
FBB_DQ14 E2 FBB_D14
FBB_DQ15 F3 FBB_D15
FBB_DQ16 C2 FBB_D16
FBB_DQ17 D4 FBB_D17
FBB_DQ18 D3 FBB_D18
FBB_DQ19 C1 FBB_D19
FBB_DQ20 B3 FBB_D20
FBB_DQ21 C4 FBB_D21
FBB_DQ22 B5 FBB_D22
FBB_DQ23 C5 FBB_D23
FBB_DQ24 A11 FBB_D24
FBB_DQ25 C11 FBB_D25
FBB_DQ26 D11 FBB_D26
FBB_DQ27 B11 FBB_D27
FBB_DQ28 D8 FBB_D28
FBB_DQ29 A8 FBB_D29
FBB_DQ30 C8 FBB_D30
FBB_DQ31 B8 FBB_D31
FBB_DQ32 F24 FBB_D32
FBB_DQ33 G23 FBB_D33
FBB_DQ34 E24 FBB_D34
FBB_DQ35 G24 FBB_D35
FBB_DQ36 D21 FBB_D36
FBB_DQ37 E21 FBB_D37
FBB_DQ38 G21 FBB_D38
FBB_DQ39 F21 FBB_D39
FBB_DQ40 G27 FBB_D40
FBB_DQ41 D27 FBB_D41
FBB_DQ42 G26 FBB_D42
FBB_DQ43 E27 FBB_D43
FBB_DQ44 E29 FBB_D44
FBB_DQ45 F29 FBB_D45
FBB_DQ46 E30 FBB_D46
FBB_DQ47 D30 FBB_D47
FBB_DQ48 A32 FBB_D48
FBB_DQ49 C31 FBB_D49
FBB_DQ50 C32 FBB_D50
FBB_DQ51 B32 FBB_D51
FBB_DQ52 D29 FBB_D52
FBB_DQ53 A29 FBB_D53
FBB_DQ54 C29 FBB_D54
FBB_DQ55 B29 FBB_D55
FBB_DQ56 B21 FBB_D56
FBB_DQ57 C23 FBB_D57
FBB_DQ58 A21 FBB_D58
FBB_DQ59 C21 FBB_D59
FBB_DQ60 B24 FBB_D60
FBB_DQ61 C24 FBB_D61
FBB_DQ62 B26 FBB_D62
FBB_DQ63 C26 FBB_D63

FBB_DQM0 E11 FBB_DQM0
FBB_DQM1 E3 FBB_DQM1
FBB_DQM2 A3 FBB_DQM2
FBB_DQM3 C9 FBB_DQM3
FBB_DQM4 F23 FBB_DQM4
FBB_DQM5 F27 FBB_DQM5
FBB_DQM6 C30 FBB_DQM6
FBB_DQM7 A24 FBB_DQM7

FBB_WDQSP0 D10 FBB_DQS_WP0
FBB_WDQSP1 D5 FBB_DQS_WP1
FBB_WDQSP2 C3 FBB_DQS_WP2
FBB_WDQSP3 B9 FBB_DQS_WP3
FBB_WDQSP4 E23 FBB_DQS_WP4
FBB_WDQSP5 E28 FBB_DQS_WP5
FBB_WDQSP6 B30 FBB_DQS_WP6
FBB_WDQSP7 A23 FBB_DQS_WP7

FBB_RDQSN0 D9 FBB_DQS_RN0
FBB_RDQSN1 E4 FBB_DQS_RN1
FBB_RDQSN2 B2 FBB_DQS_RN2
FBB_RDQSN3 A9 FBB_DQS_RN3
FBB_RDQSN4 D22 FBB_DQS_RN4
FBB_RDQSN5 D28 FBB_DQS_RN5
FBB_RDQSN6 A30 FBB_DQS_RN6
FBB_RDQSN7 B23 FBB_DQS_RN7

FBB_CMD0 D13 FBB_CMD0
FBB_CMD1 E14 FBB_CMD1 — VT4
FBB_CMD2 E14 FBB_CMD2
FBB_CMD3 A12 FBB_CMD3
FBB_CMD4 B12 FBB_CMD4
FBB_CMD5 C14 FBB_CMD5
FBB_CMD6 B14 FBB_CMD6
FBB_CMD7 G15 FBB_CMD7
FBB_CMD8 F15 FBB_CMD8
FBB_CMD9 E15 FBB_CMD9
FBB_CMD10 D15 FBB_CMD10
FBB_CMD11 A14 FBB_CMD11
FBB_CMD12 D14 FBB_CMD12
FBB_CMD13 A15 FBB_CMD13
FBB_CMD14 B15 FBB_CMD14
FBB_CMD15 C17 FBB_CMD15
FBB_CMD16 D18 FBB_CMD16
FBB_CMD17 E18 FBB_CMD17 — VT6
FBB_CMD18 F18 FBB_CMD18
FBB_CMD19 A20 FBB_CMD19
FBB_CMD20 B20 FBB_CMD20
FBB_CMD21 C18 FBB_CMD21
FBB_CMD22 B18 FBB_CMD22
FBB_CMD23 G18 FBB_CMD23
FBB_CMD24 G17 FBB_CMD24
FBB_CMD25 E17 FBB_CMD25
FBB_CMD26 D16 FBB_CMD26
FBB_CMD27 A18 FBB_CMD27
FBB_CMD28 D17 FBB_CMD28
FBB_CMD29 A17 FBB_CMD29
FBB_CMD30 B17 FBB_CMD30
FBB_CMD31 E17 FBB_CMD31 — VT8

FBB_CMD_RFU0 C12 — VT11
FBB_CMD_RFU1 C20 — VT12

FBB_CMD2 VR9 DIS@10K_4 FBB_ODT_L
FBB_CMD18 VR11 DIS@10K_4 FBB_ODT_H
FBB_CMD3 VR13 DIS@10K_4 FBB_CKE_L
FBB_CMD19 VR15 DIS@10K_4 FBB_CKE_H
FBB_CMD5 VR17 DIS@10K_4 FBB_RST#

Debug
1.5V_GPU
FBB_DEBUG0 G14 FBB_DEBUG0 — VR20 *DIS@60.4/F_4
FBB_DEBUG1 G20 FBB_DEBUG1 — VR21 *DIS@60.4/F_4

FBB_CLK0 D12 — FBB_CLK0 23
FBB_CLK0 E12 — FBB_CLK#0 23
FBB_CLK1 E20 — FBB_CLK1 23
FBB_CLK1 F20 — FBB_CLK#1 23

FBB_WCK01 F8
FBB_WCK01 E8
FBB_WCK23 A5
FBB_WCK23 A6
FBB_WCK45 D24
FBB_WCK45 D25
FBB_WCK67 B27
FBB_WCK67 C27

FBB_WCKB01 D6
FBB_WCKB01 D7
FBB_WCKB23 C6
FBB_WCKB23 B6
FBB_WCKB45 F26
FBB_WCKB45 E26
FBB_WCKB67 A26
FBB_WCKB67 A27

FBB_PLL_AVDD H17 FBA_PLL_AVDD
VC63 LP@0.1u/10V_4

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	N13P MEM I/F	B

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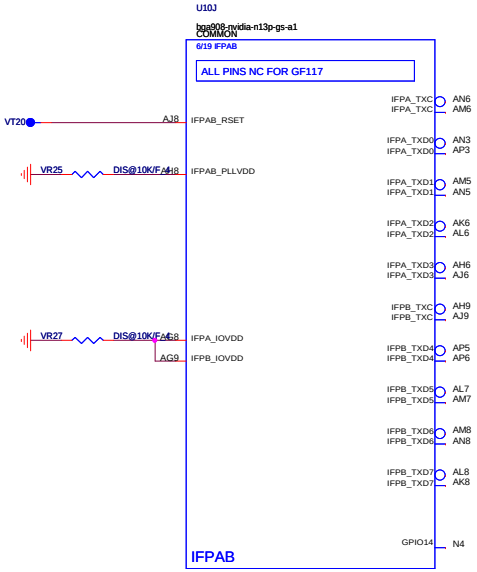

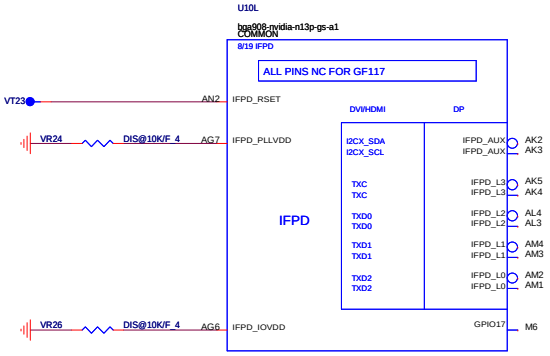

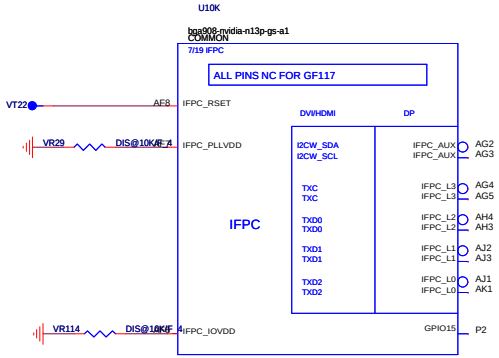

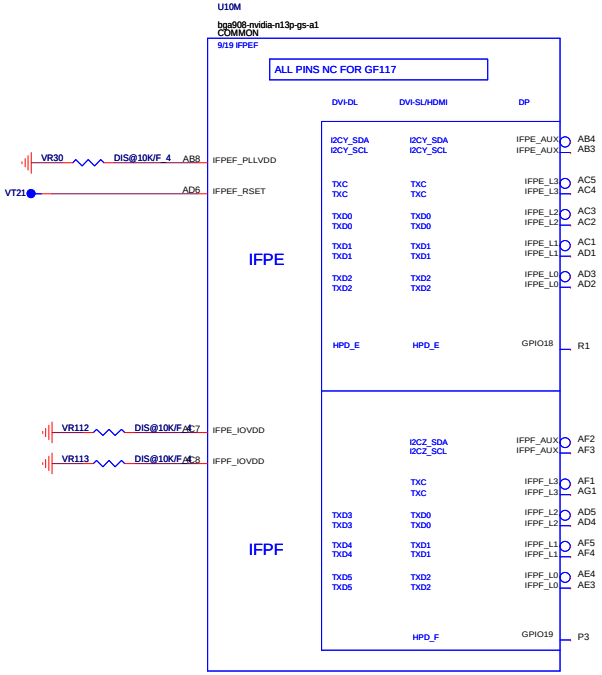

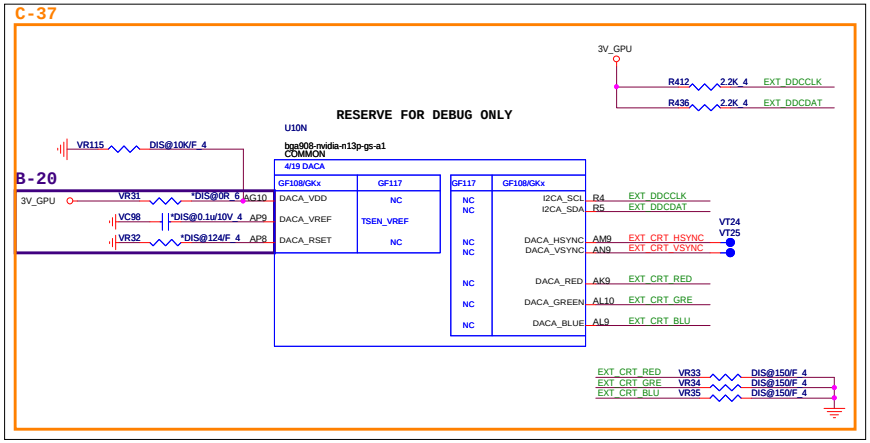

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2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	N13P DISPLAY	B
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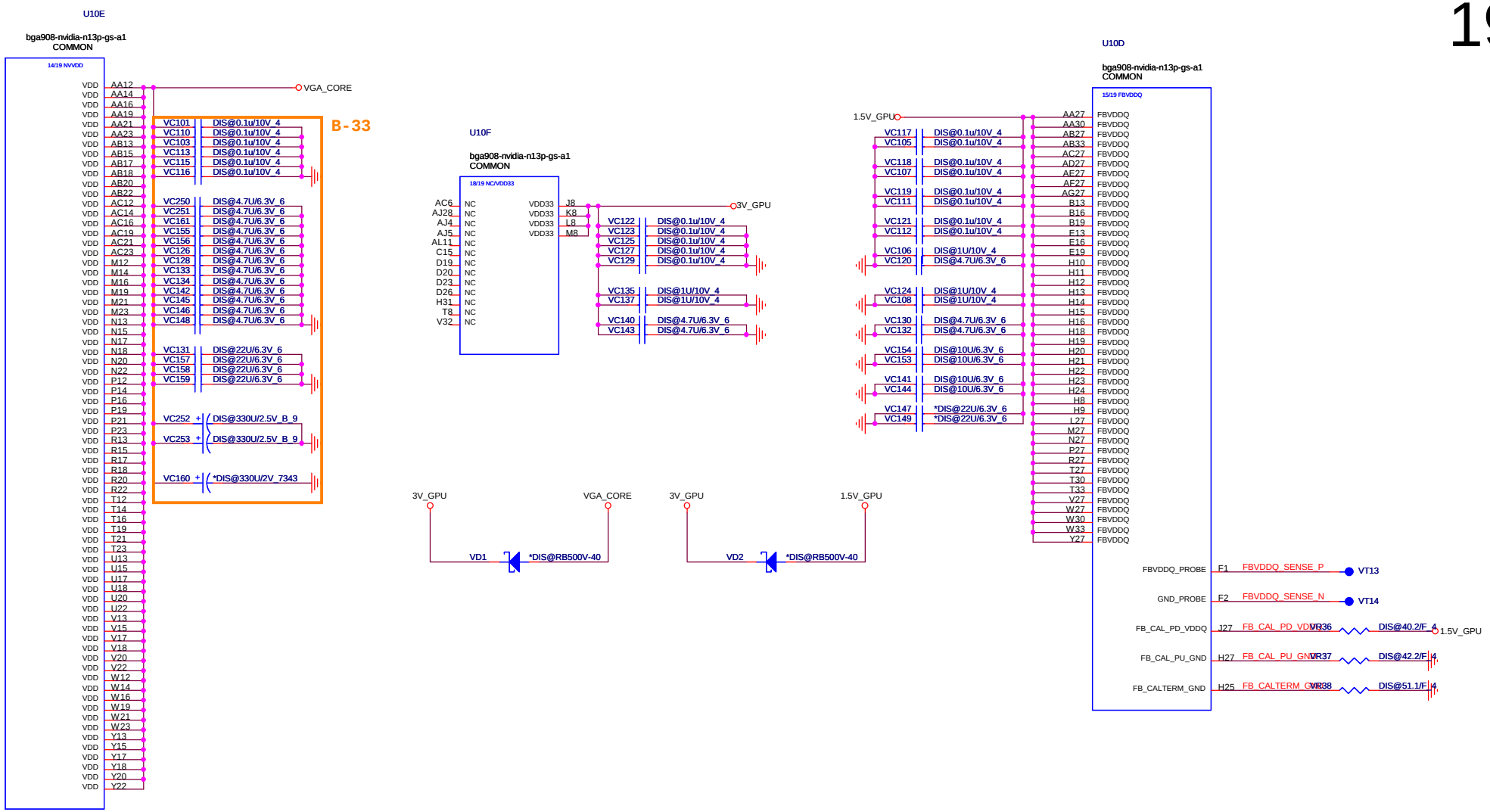

Quanta Computer Inc.

PROJECT : FH6C_HM70

Size	Document Number	Rev
	N13P POWER	B

Date: Tuesday, May 22, 2012 Sheet 19 of 45

U10G

bga908-nvidia-n13p-gs-a1
COMMON

16/19 GND_1/2

A2	GND	GND	AM25
AA17	GND	GND	AN1
AA18	GND	GND	AN10
AA20	GND	GND	AN13
AA22	GND	GND	AN16
AB12	GND	GND	AN19
AB14	GND	GND	AN22
AB16	GND	GND	AN25
AB19	GND	GND	AN30
AB2	GND	GND	AN34
AB21	GND	GND	AN4
A33	GND	GND	AN7
AB23	GND	GND	AP2
AB28	GND	GND	AP33
AB30	GND	GND	B1
AB32	GND	GND	B10
AB5	GND	GND	B22
AB7	GND	GND	B25
AC13	GND	GND	B28
AC15	GND	GND	B31
AC17	GND	GND	B34
AC18	GND	GND	B4
AA13	GND	GND	B7
AC20	GND	GND	C10
AC22	GND	GND	C13
AE2	GND	GND	C19
AE28	GND	GND	C22
AE30	GND	GND	C25
AE32	GND	GND	C28
AE33	GND	GND	C7
AE5	GND	GND	D2
AE7	GND	GND	D31
AH10	GND	GND	D33
AA15	GND	GND	E10
AH13	GND	GND	E22
AH16	GND	GND	E25
AH19	GND	GND	E5
AH2	GND	GND	E7
AH22	GND	GND	E28
AH24	GND	GND	F7
AH28	GND	GND	G10
AH29	GND	GND	G13
AH30	GND	GND	G16
AH32	GND	GND	G19
AH33	GND	GND	G2
AH5	GND	GND	G22
AH7	GND	GND	G25
AJ7	GND	GND	G28
AK10	GND	GND	G3
AK7	GND	GND	G30
AL12	GND	GND	G32
AL14	GND	GND	G33
AL15	GND	GND	G5
AL17	GND	GND	G7
AL18	GND	GND	K2
AL2	GND	GND	K28
AL20	GND	GND	K30
AL21	GND	GND	K32
AL23	GND	GND	K33
AL24	GND	GND	K5
AL26	GND	GND	K7
AL28	GND	GND	M13
AL30	GND	GND	M15
AL32	GND	GND	M17
AL33	GND	GND	M18
AL5	GND	GND	M20
AM13	GND	GND	M22
AM16	GND	GND	N12
AM19	GND	GND	N14
AM22	GND	GND	N16

U10I

bga908-nvidia-n13p-gs-a1
COMMON

17/19 GND_2/2

N19	GND	GND	T28
N2	GND	GND	T32
N21	GND	GND	T5
N23	GND	GND	T7
N28	GND	GND	U12
N30	GND	GND	U14
N32	GND	GND	U16
N33	GND	GND	U19
N5	GND	GND	U21
N7	GND	GND	U23
P13	GND	GND	V12
P15	GND	GND	V14
P17	GND	GND	V16
P18	GND	GND	V19
P20	GND	GND	V21
P22	GND	GND	V23
R12	GND	GND	W13
R14	GND	GND	W15
R16	GND	GND	W17
R19	GND	GND	W18
R21	GND	GND	W20
R23	GND	GND	W22
T13	GND	GND	W28
T15	GND	GND	Y12
T17	GND	GND	Y14
T18	GND	GND	Y16
T2	GND	GND	Y19
T20	GND	GND	Y21
T22	GND	GND	Y23
AG11	GND	GND	AH11
	GND_OPT	GND_OPT	C16
	GND_OPT	GND_OPT	W32

Optional CMD GNDs (2)
NC for 4-Lyr cards

U10H

bga908-nvidia-n13p-gs-a1
COMMON

10/19 XVDD

CONFIGURABLE
POWER
CHANNELS

XVDD	U1	
XVDD	U2	
XVDD	U3	
XVDD	U4	
XVDD	U5	
XVDD	U6	
XVDD	U7	
XVDD	U8	
XVDD	V1	
XVDD	V2	
XVDD	V3	
XVDD	V4	
XVDD	V5	
XVDD	V6	
XVDD	V7	
XVDD	V8	
XVDD	W2	
XVDD	W3	
XVDD	W4	
XVDD	W5	
XVDD	W7	
XVDD	W8	
XVDD	Y1	
XVDD	Y2	
XVDD	Y3	
XVDD	Y4	
XVDD	Y5	
XVDD	Y6	
XVDD	Y7	
XVDD	Y8	
XVDD	AA1	
XVDD	AA2	
XVDD	AA3	
XVDD	AA4	
XVDD	AA5	
XVDD	AA6	
XVDD	AA7	
XVDD	AA8	

To be configured as needed on the PCB

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	N13P GND	B
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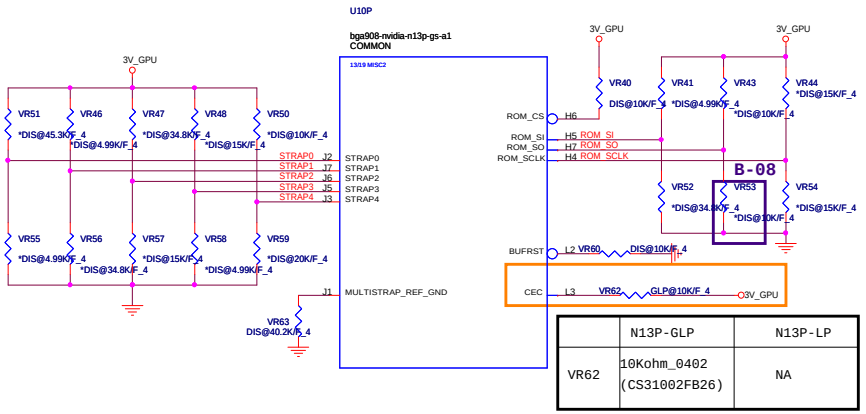
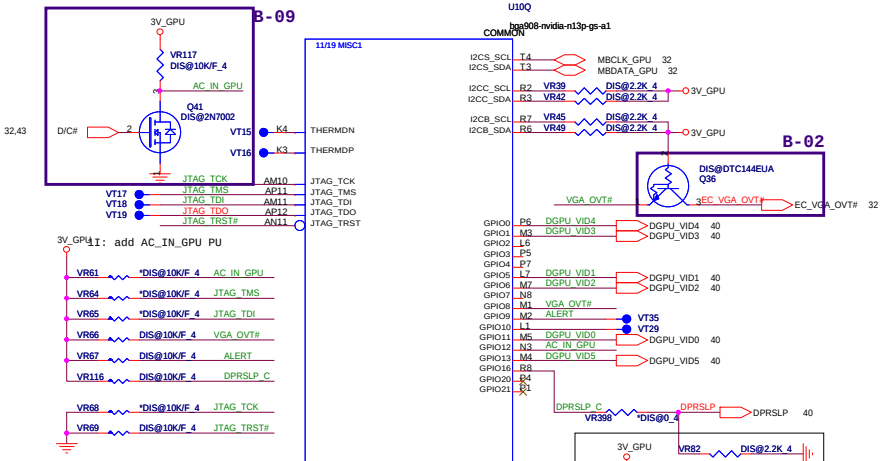


	N13P-GLP	N13P-LP
VR62	10Kohm_0402 (CS31002FB26)	NA

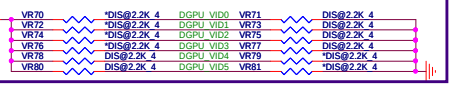


1I: add AC_IN_GPU PU

VR61 *DIS@10K/F_4 AC_IN_GPU
VR64 *DIS@10K/F_4 JTAG_TMS
VR65 *DIS@10K/F_4 JTAG_TDI
VR66 DIS@10K/F_4 VGA_OVT#
VR67 DIS@10K/F_4 ALERT
VR116 DIS@10K/F_4 DPRSLP_C
VR68 *DIS@10K/F_4 JTAG_TCK
VR69 DIS@10K/F_4 JTAG_TRST#

C-33 For IVMP 6.5(GPU)

Default:0.9V (0110000) N13P-GLP/LP
Note:VID6 PD in VR Side



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Logical Strap Bit Mapping

Value	PU-VDD	PD	QCI PN(0402)
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB22
45.3K	1111	0111	CS34532FB18

VRAM(DDR3) Configuration Table

RAMCFG [3:0]	DESCRIPTION (Vendor P/N)	Vendor	QCI P/N	ROM_SI
0111	128*16-900MHz K4W2G1646C-HC11	Samsung	AKD5MGWT500	PD 45.3K
0110	128*16-900MHz H5TQ2G63BFR-11C	Hinyx	AKD5MGWTW00	PD 35K
0010	64*16-900MHz H5TQ1G63DFR-11C	Hinyx	AKD5LZWTW02	PD 15K
0011	64*16-900MHz K4W1G1646G-BC11	Samsung	AKD5EGGT500	PD 20K

B-29

		GLP 1GB HYN	GLP 1GB SAM	GLP 2GB HYN	GLP 2GB SAM	LP 2GB HYN	LP 2GB SAM
ROM_SCLK	VR44 VR54	NA CS31502FB24	NA CS31502FB24	NA CS31502FB24	NA CS31502FB24	CS24992FB26 NA	CS24992FB26 NA
ROM_SI	VR41 VR52	NA CS31502FB24	NA CS32002FB29	NA CS33012FB18	NA CS34532FB18	NA CS33012FB18	NA CS34532FB18
ROM_SO	VR43 VR53	NA CS31002FB26	NA CS31002FB26	NA CS31002FB26	NA CS31002FB26	CS31002FB26 NA	CS31002FB26 NA
STRAP0	VR51 VR55	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA
STRAP1	VR46 VR56	NA CS34532FB18	NA CS34532FB18	NA CS34532FB18	NA CS34532FB18	NA CS24992FB26	NA CS24992FB26
STRAP2	VR47 VR57	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	NA CS32002FB29	NA CS32002FB29
STRAP3	VR48 VR58	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26	NA CS24992FB26
STRAP4	VR50 VR59	NA NA	NA NA	NA NA	NA NA	NA CS34532FB18	NA CS34532FB18

N13P-LP (GK107-ESP)	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG-GLP PCI_DEVIDE[5]-LP	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	XCLK_417 FB[1]-LP	FB_0_BAR_SIZE FB[0]-LP	SMB_ALT_ADDR I2CS ADDR:0X9E	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	Reserve PCIE_SPEED-LP	PCIE_MAX_SPEED	DP_PLL_VDD3V

Value	Note
1000	LP:ES Samples 5K PU(0X0FDB)
0010	GLP:ES Samples 15K PD(0X0DFE)
0110	LP H5TQ2G63BFR-11C :35K PD
0111	LP K4W2G1646C-HC11 45.3K PD
0010	GLP H5TQ1G63DFR-11C :15K PD
0011	GLP K4W1G1646G-BC11 :20K PD
1001	10K PU
0001	10K PD
1111	EDID is used :45K PU
0000	LP:notebook default:35K PD
0111	GLP: Reserve:45.3K PD
0011	LP ES Samples:20K PU(0X0FDB)
1000	GLP ES Samples:45.3K PU(0X0DEF)
0000	Not in use :5K PD
0111	LP:10K PD GLP: NA

B-08

*LP QS Samples:5K PU(0X0FD3)
*GLP MP Samples 15K PD(0X0DE8)
*H5TQ2G63DFR-11C: 30.1K PD(0X5)

C-48

*LP QS Samples: 4.99K PD(0X0)
*LP QS Samples: 20K PD(0X0FD3)
*GLP MP Samples: 5K PU(0X0DE8)
*LP QS Samples: 45K PD(0X111)

GPIO ASSIGNMENTS

GPIO	I/O	USAGE	
0	OUT	Y	NVVDD VID4
1	OUT	Y	NVVDD VID3
2	OUT	N	PANEL BACKLIGHT PWM
3	OUT	N	PANEL POWER ENABLE
4	OUT	N	PANEL BACKLIGHT ENABLE
5	OUT	Y	NVVDD VID1
6	OUT	Y	NVVDD VID2
7	OUT	N	3D STEREO
8	I/O	Y	GPU Overtemp
9	I/O	Y	GPU ALERT
10	OUT	N	FB Vref Control
11	OUT	Y	NVVDD VID0
12	IN	N	PWR_Level AC Detect
13	OUT	Y	NVVDD VID5
14	IN	N	HPD for IFP AB
15	IN	N	HPD for IFP C
16	OUT	N	DPRSLP(Default) or PSI#
17	OUT	N	HPD for IFP D
18	OUT	N	HPD for IFP E
19	OUT	N	HPD for IFP F
20	OUT	N	
21	OUT	N	

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PROJECT : FH6C_HM70

Size	Document Number	Rev
	N13P STRAP/GPIO	B

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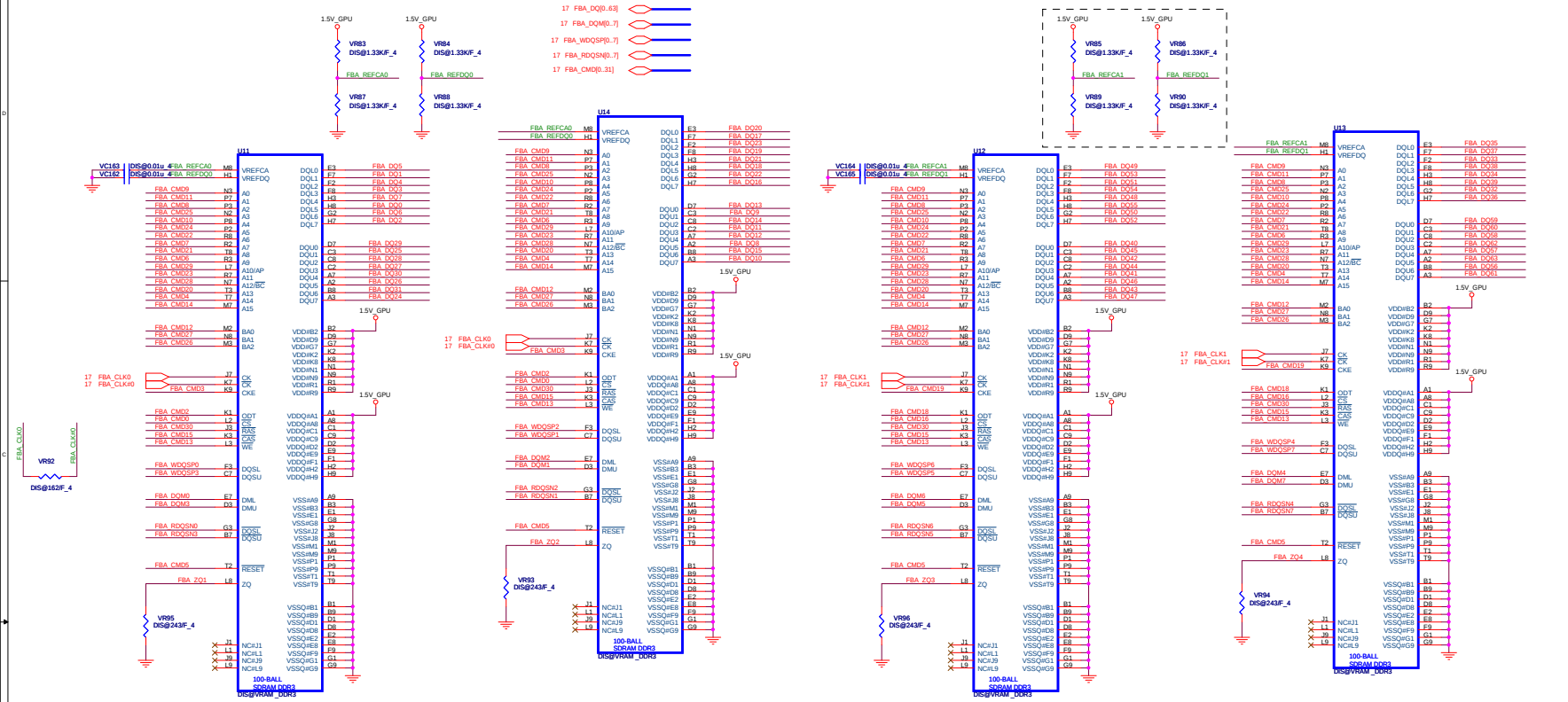

	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	N/A	CKE
CMD21	ODT	N/A
CMD22	N/A	ODT
CMD23	CS*	N/A
CMD24	N/A	CS*
CMD25	RAS*	RAS*
CMD26	CAS*	CAS*
CMD27	WE*	WE*
CMD28	RST	RST
CMD29	N/A	N/A
CMD30	N/A	N/A
CMD31	N/A	N/A

IN USE ON VU? - VU?

	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	N/A	CKE
CMD20	CKE	N/A
CMD21	N/A	ODT
CMD22	ODT	N/A
CMD23	N/A	CS*
CMD24	CS*	N/A
CMD25	RAS*	RAS*
CMD26	CAS*	CAS*
CMD27	WE*	WE*
CMD28	RST	RST
CMD29	N/A	N/A
CMD30	N/A	N/A
CMD31	N/A	N/A

IN USE ON VU? - VU?

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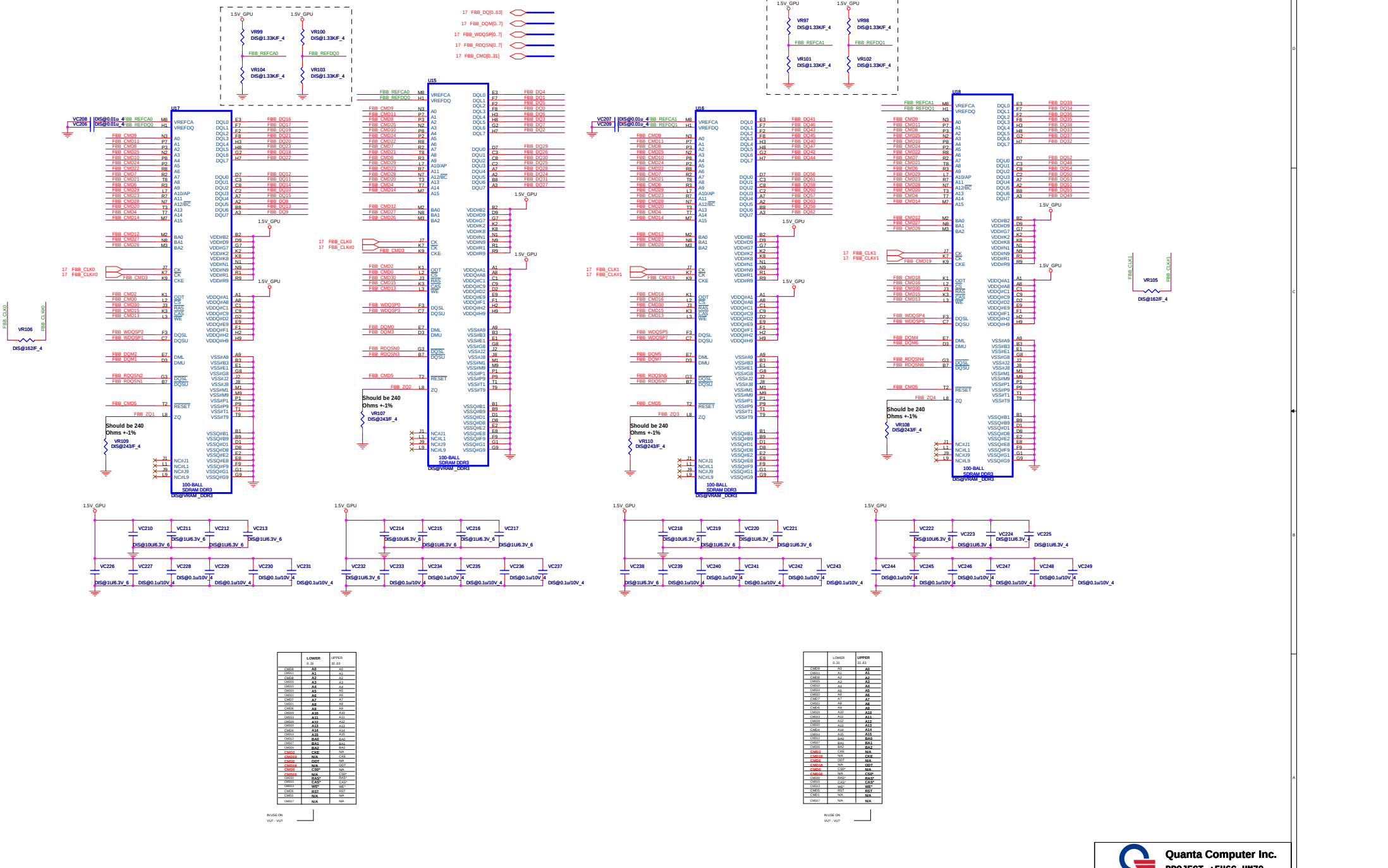
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	N13P VRAM-A DDR3	B
Date: Tuesday, May 22, 2012	Sheet 22 of 45	



	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	ODT	N/A
CMD21	CS#	N/A
CMD22	RAS#	CKE
CMD23	CAS#	ODT
CMD24	WE#	CS#
CMD25	RST	RAS#
CMD26	N/A	CAS#
CMD27	N/A	WE#
		RST
		N/A

IN USE ON VU7 - VU7

	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	ODT	N/A
CMD21	CS#	N/A
CMD22	RAS#	CKE
CMD23	CAS#	ODT
CMD24	WE#	CS#
CMD25	RST	RAS#
CMD26	N/A	CAS#
CMD27	N/A	WE#
		RST
		N/A

IN USE ON VU7 - VU7

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
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	N13P VRAM-B DDR3	B

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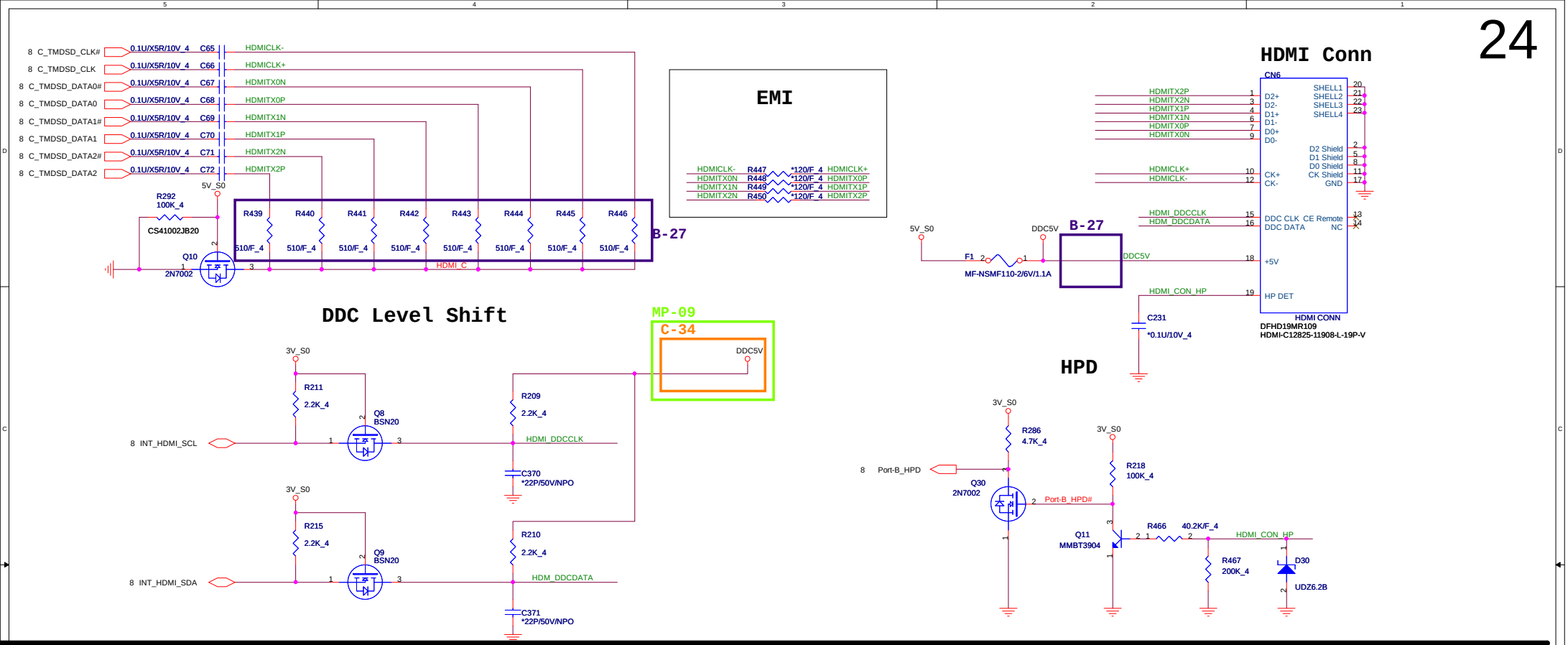

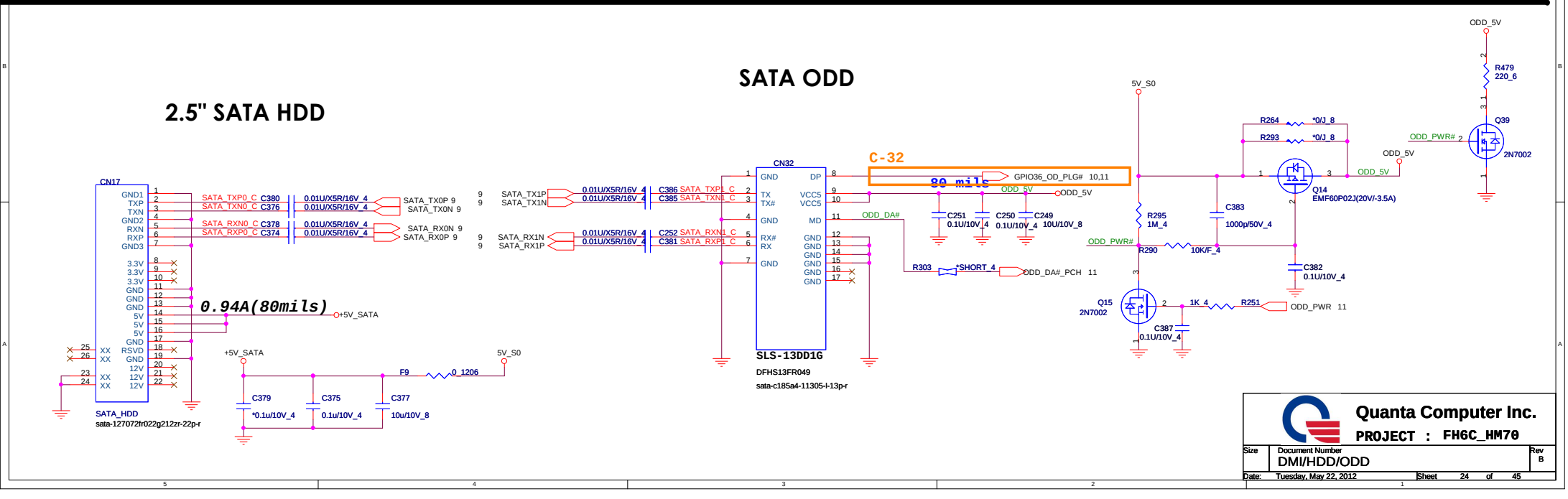

Quanta Computer Inc.
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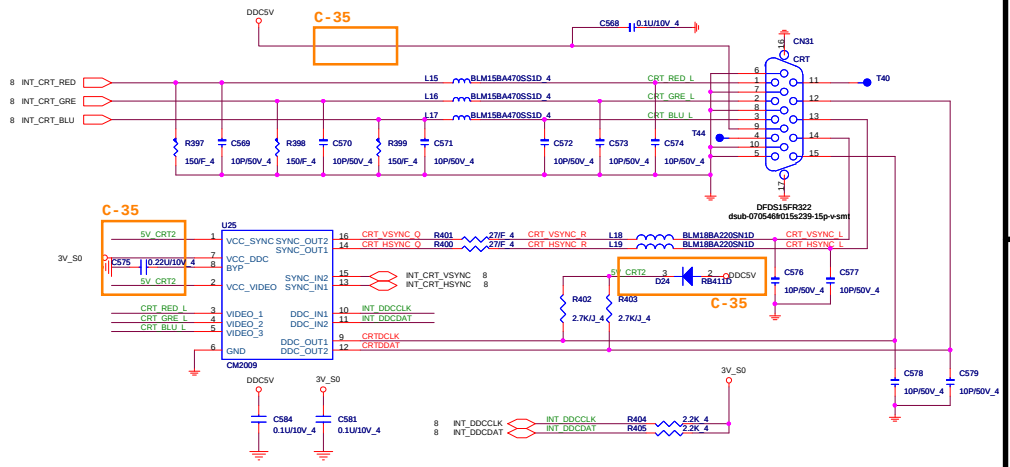
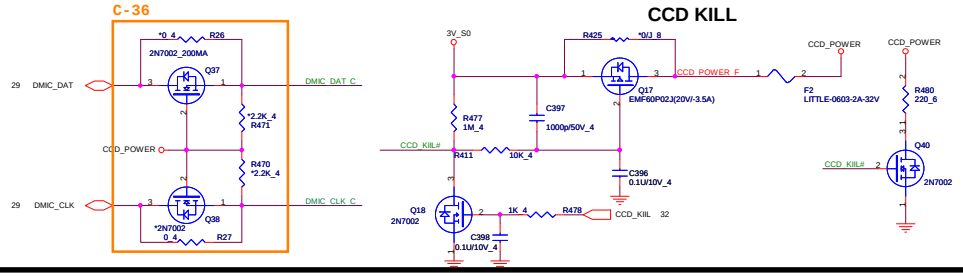
CRT CONN/DDC LEVEL SHIFT

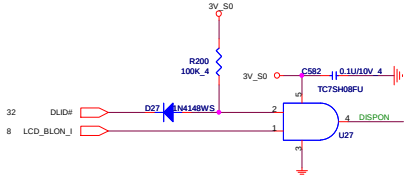


C-37

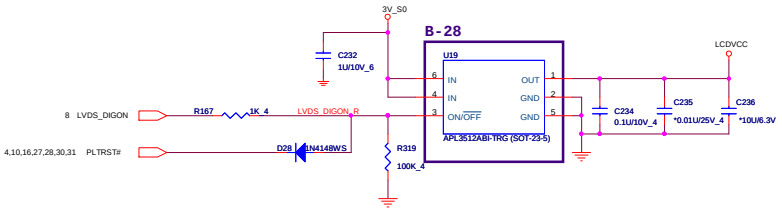
CCD KILL



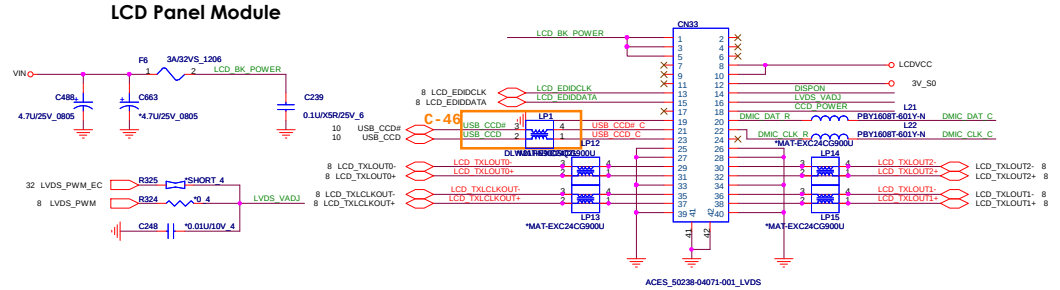
PANEL BACKLIGHT CONTROL



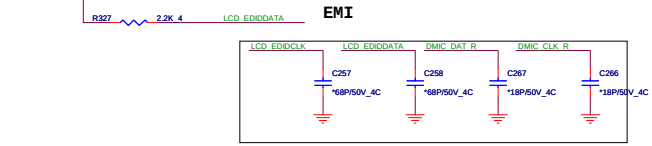
LCD POWER SWITCH



LCD Panel Module



EMI



Quanta Computer Inc.

PROJECT : FH6C_HM70

Size	Document Number	Rev
	LVDS/CCD/CRT	B

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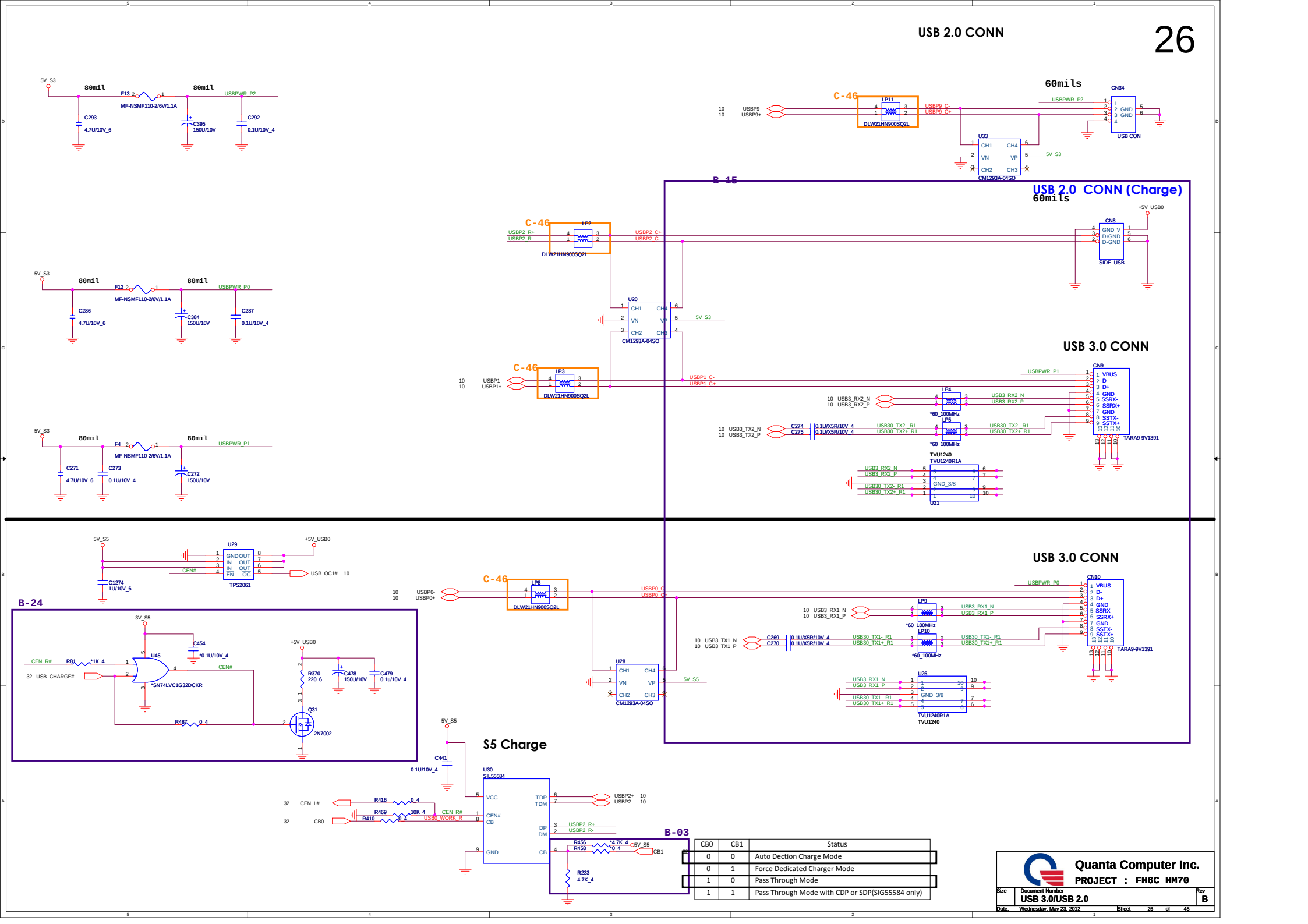

CB0	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP or SDP(SIG55584 only)

Quanta Computer Inc.

PROJECT : FH6C_HM70

Size	Document Number	Rev
	USB 3.0/USB 2.0	B

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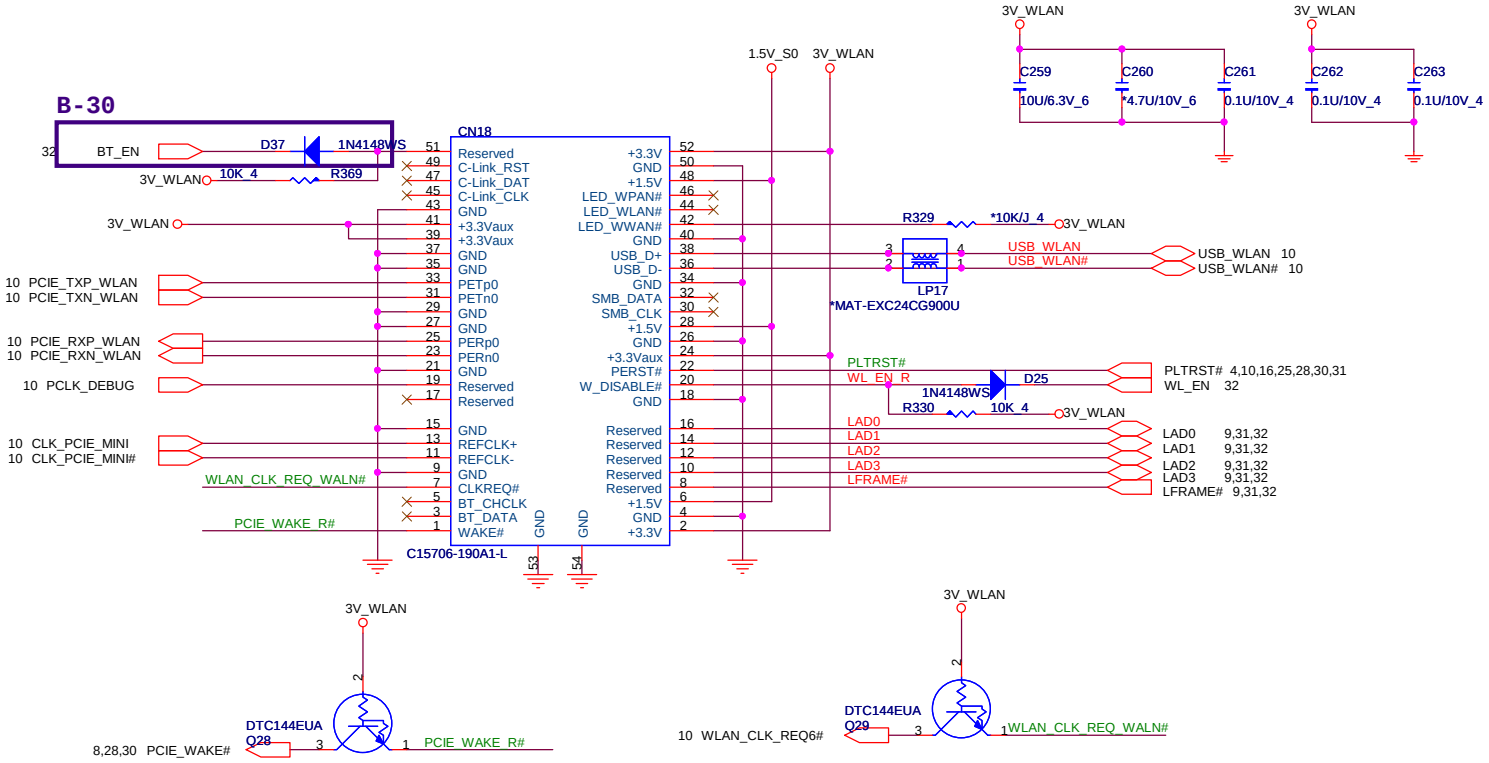
Wireless/BT COMBO



Quanta Computer Inc.		
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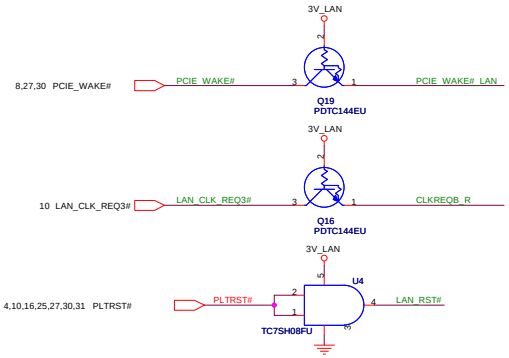

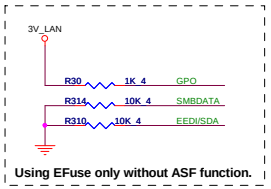

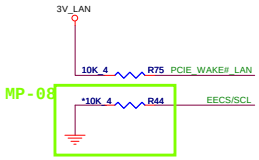

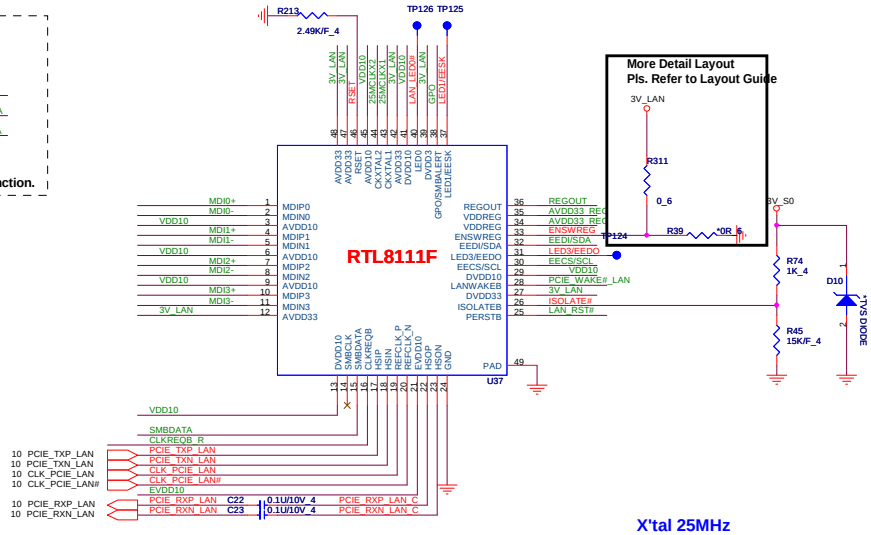

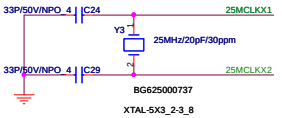

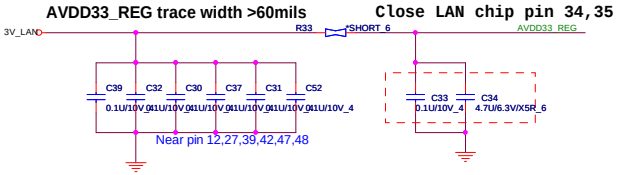

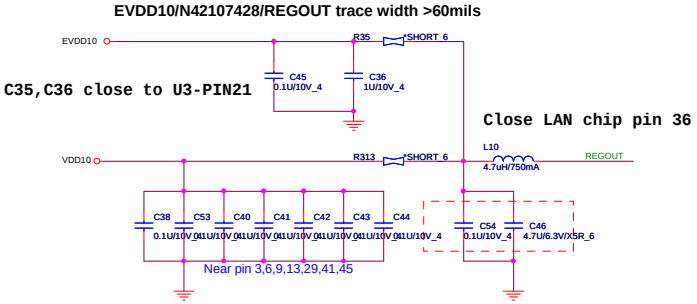

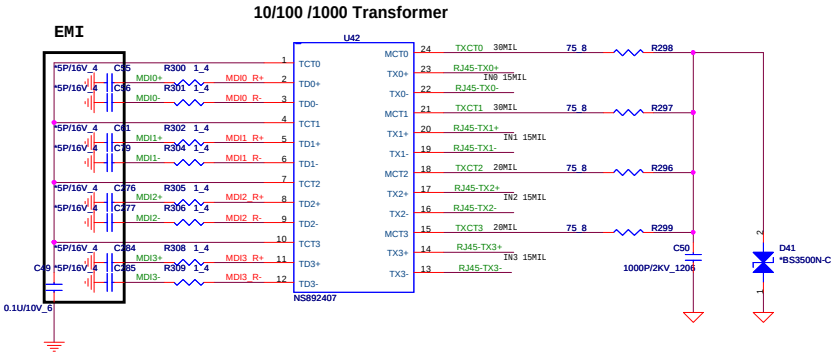

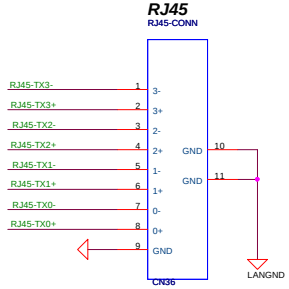

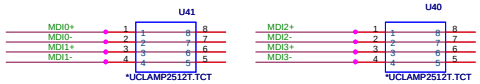

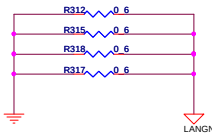

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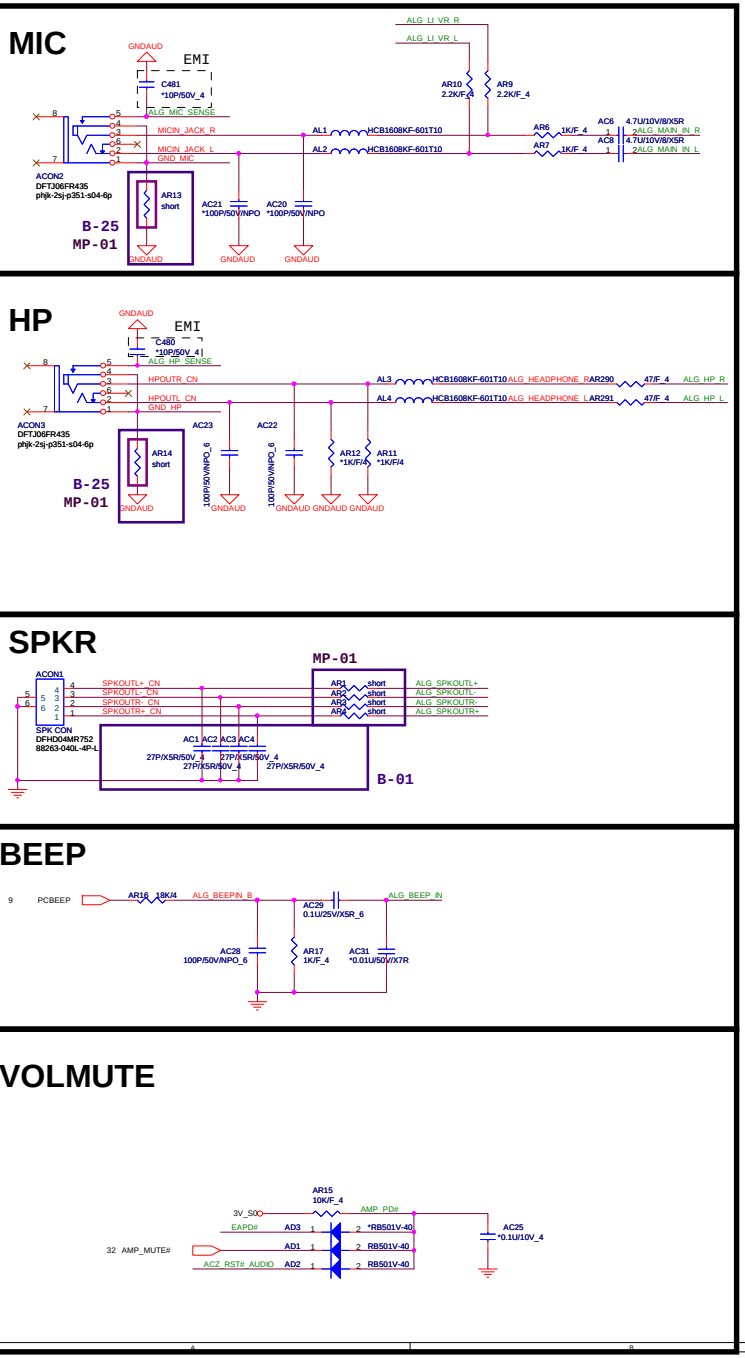
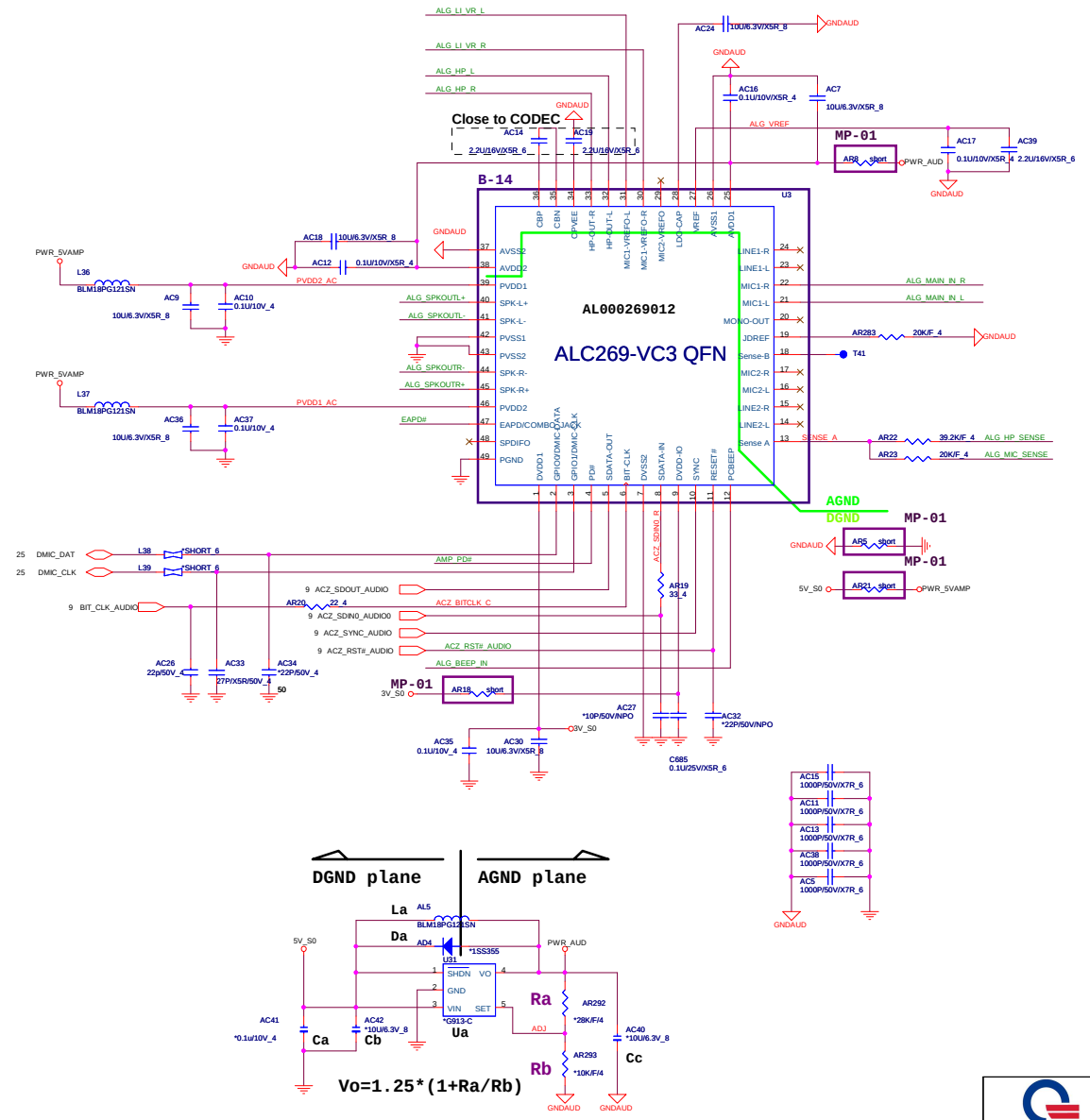
Codec ALC269-VC3





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	CODEC (ALC269Q-VC3)		B
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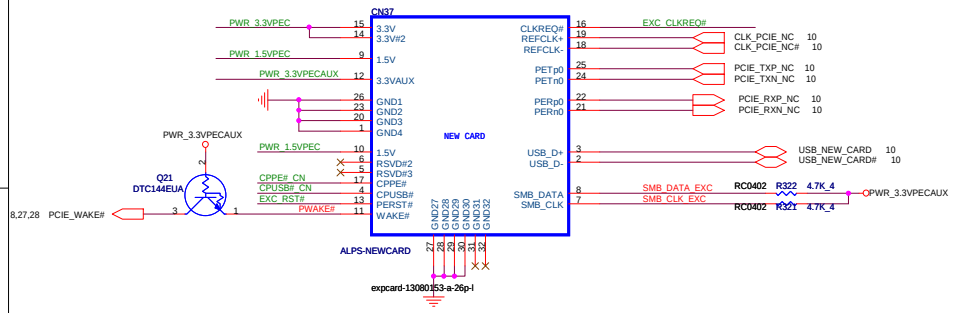
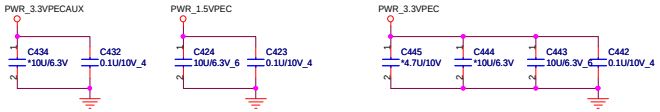
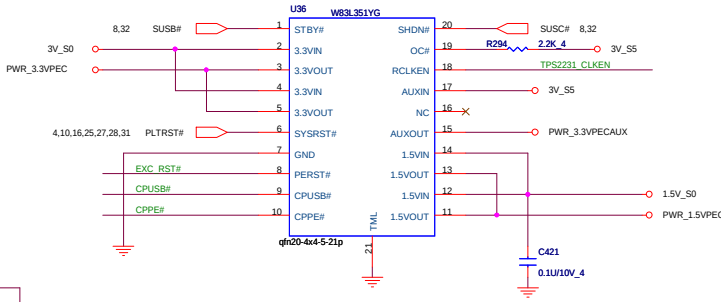
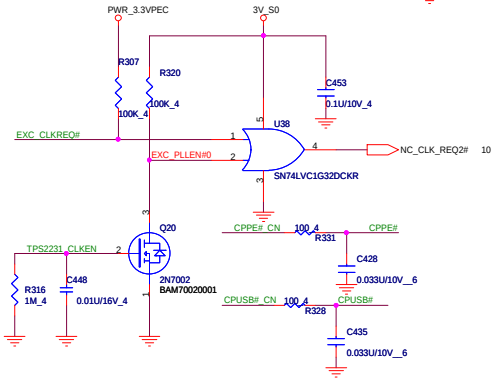
NEW CARD

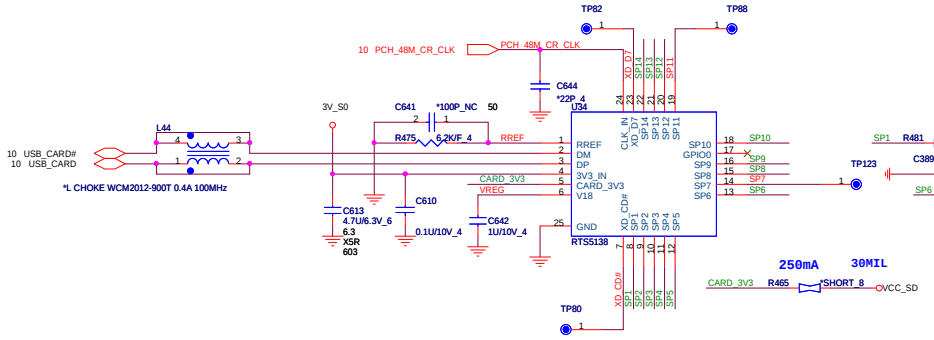


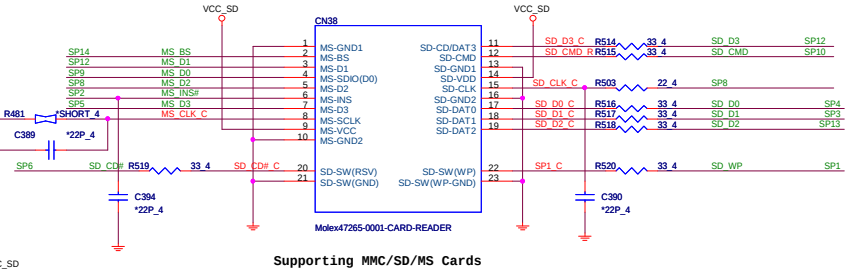


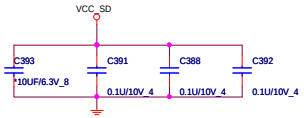


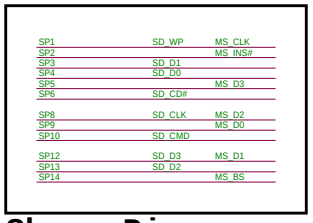


Card reader RTS5138









Share Pin

Quanta Computer Inc.
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	NEW CARD/CARD READER	B
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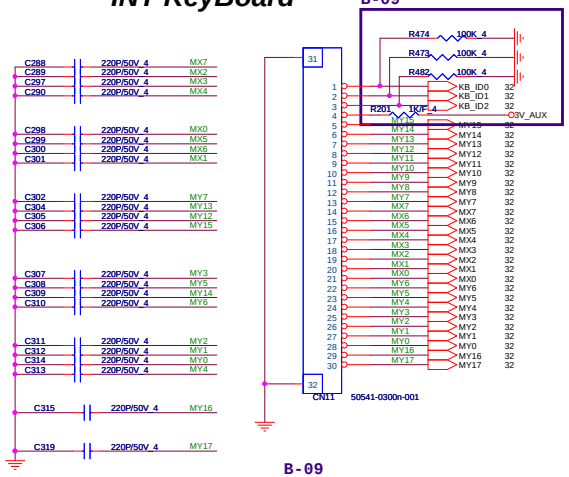
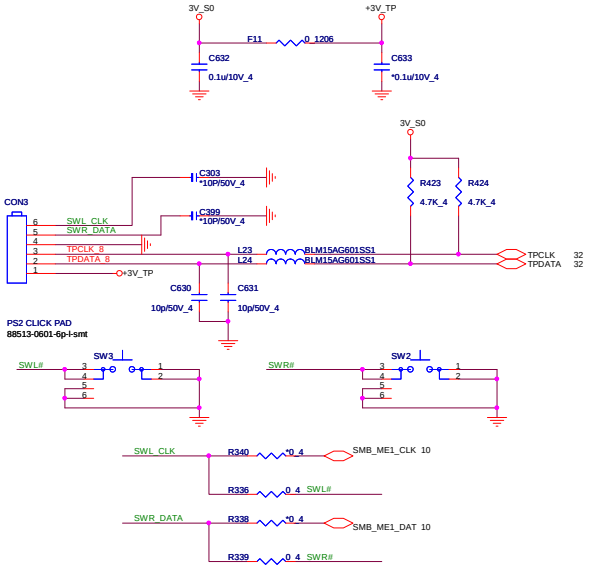
INT KeyBoard



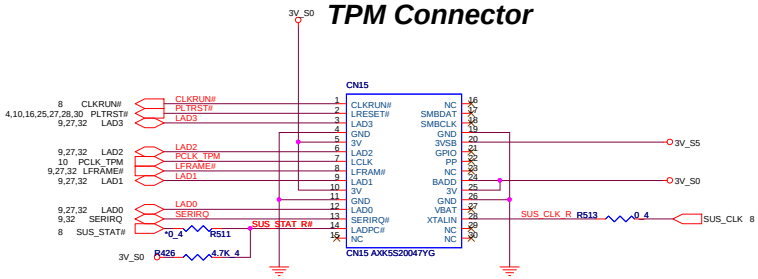
B-09

	ID0	ID1	ID2		KB_ID
			CHO	ISO	
UK	1	0	0	1	1
US	0	1	0	1	1
JP	1	1	0	1	1

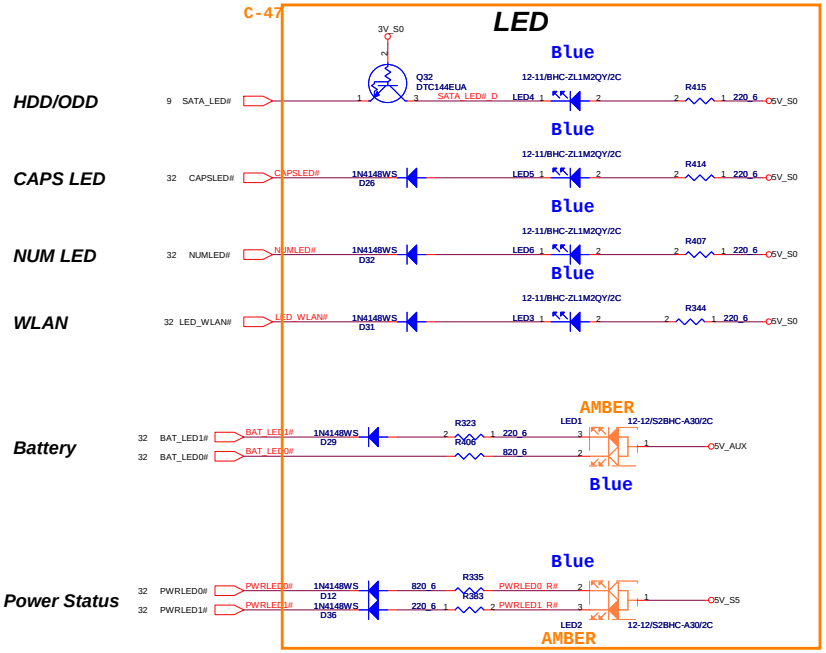
Touch Pad SMBUS CLICK PAD reserve



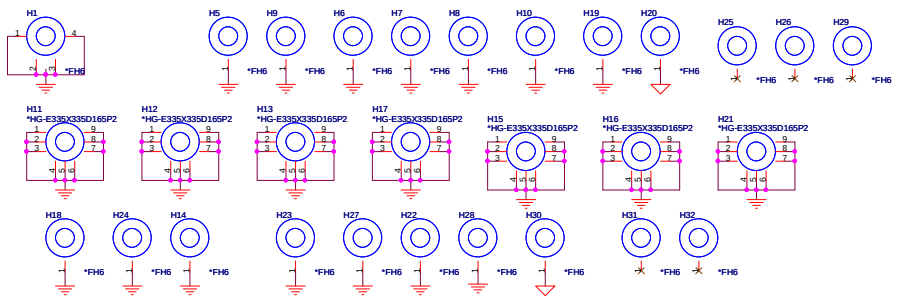
TPM Connector



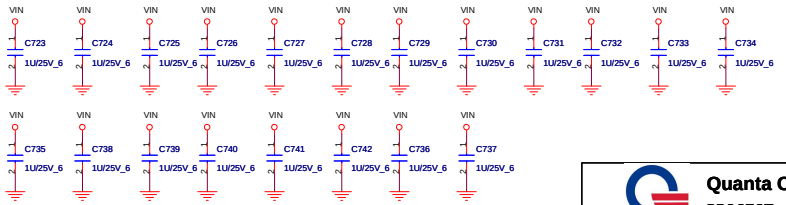
LED



HOLE



Decaupling Cap



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	TPM/KB/TP/LED/HOLE	B

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EC_ITE8519

Close EC Side

3V_AUX — C326 *10U/6.3V_6 — C327 *10U/6.3V_6 — C328 *10U/6.3V_6 — C329 0.1U/10V_4 — C330 0.1U/10V_4 — C331 0.1U/10V_4

3V_RTC — VBAT — R452 0_4 — R453 *0_4

AVCC_EC — C323 1000P/50V_4 — C324 0.1U/10V_4 — C325 0.1U/10V_4 — L14 BK1608HS121-T/0.5A_6 — 3V_AUX

3V_S0 — C332 0.1U/10V_4

S5_ON — S3_ON — S0_ON1 — S0_ON2

11 PCH_DGPU_VRON — S5_ON 4,33,41 — S3_ON 36,41 — S0_ON1 41 — S0_ON2 36,37,38,39,41

T43 — R97 UMA@100K_4 — R108 DIS@100K_4 — SUSB# — SUSB# 8,30 — KB_ID2 31 — SUSC# — SUSC# 8,30

B-23 — B-09

	UMA	DIS
R97	CS41002JB20	NA
R108	NA	CS41002JB20

B-21

3V_S5 — C233 0.1U/10V_4 — PCH_DGPU_VRON — EC_DGPU_VRON_R — U43 TC7SH08FU(F) — DGPU_VRON 41

3V_S5 — C237 0.1U/10V_4 — 11 PCH_DGPU_VRON2 — PCH_DGPU_VRON2 — EC_DGPU_VRON2_R — U44 TC7SH08FU(F) — DGPU_VRON2 40

IT8518

U23

LAD0 LAD1 LAD2 LAD3 — CB0 — PCLK_591 — LFRAME# — LED_WLAN# — GATEA20 — SERIRQ — SMI# — SCI# — PCURST# — RCIN# — BAT_LED0#

LPC

D16 1N4148WS — D17 1N4148WS — D14 1N4148WS — D15 1N4148WS

GA20/GPB5(X) SERIRQ/GPM6(X) ECSMI#/GPD4(Up) ECSCI#/GPD3(Up) WRST# KBRST#/GPB6(X) PWUREQ#/BBO/SMCLK2ALT/GPC7(Up)

LPCPD#/WUI6/GPE6(Dn) LFRAME#/GPM5(X) LPCRST#/WUI4/GPD2(Up) LPCCLK/GPM4(X)

GPIO

EGCLK/WUI27/GPE3(Dn) EGCS#/WUI26/GPE2(Dn) EGAD/WUI25/GPE1(Dn) L80HLATCH/WUI24/GPE0(Dn) L80LLATCH/WUI7/GPE7(Up) HMOSI/GPH6/ID6(Dn) HMISO/GPH5/ID5(Dn) HSCK/GPH4/ID4(Dn) HSCE#/WUI18/GPH3/ID3(Dn) CLKRUN#/WUI16/GPH0/ID0(Dn)

SM BUS — SMCLK0/GPB3(X) SMDAT0/GPB4(X) SMCLK1/GPC1(X) SMDAT1/GPC2(X) SMCLK2/WUI22/GPF6(Up) SMDAT2/WUI23/GPF7(Up)

PS/2 — PS2CLK0/TMB0/GPF0(Up) PS2DAT0/TMB1/GPF1(Up) PS2CLK2/WUI20/GPF4(Up) PS2DAT2/WUI21/GPF5(Up)

MBCLK1 MBDATA1 MBCLK2 MBDATA2 EC_PECI R 43_4 R355 WL_EN — TPCLK TPDATA CAPSLED# NUMLED#

B-21 — MPWROK — EC_DGPU_VRON_R R389 SHORT_4 — EC_DGPU_VRON 123

CIR — CRX0/GPC0(Dn) CTX0/TMA0/GPB2(Dn)

PWM — PWM0/GPA0(Up) PWM1/GPA1(Up) PWM2/GPA2(Up) PWM3/GPA3(Up) PWM4/GPA4(Up) PWM5/GPA5(Up)

LAN_ON LVDS_PWM_EC CB1 BT_EN AMP_MUTE#

TACH0A/GPD6(Dn) TACH1A/TMA1/GPD7(Dn) — DNBSWON_R# D13 1N4148WS — FANSIG — B-04

TMRI0/WUI2/GPC4(Dn) TMRI1/WUI3/GPC6(Dn) — VRON — D/C#

DLID# — RSMRST# — PWRLED2# — HWPG — H_PROCHOT_EC — BAT_LED1# — LID# — KB_ID0 — KB_ID1 — PCUHOLD# — PWRLED1# — SWI — ACZ_SDOUT — WLAN_ON — 1N4148WS D39 — 1N4148WS D33 — SWI_EC — ME_Security — B-04

DAC4/DCD0#/GPJ4(X) DSR0#/GPG6(X) GINT/CTS0#/GPD5(Up) PS2DAT1/RTS0#/GPF3(Up) DAC5/RIG0#/GPJ5(X) PS2CLK1/DTR0#/GPF2(Up) TXD/SOUT0/GPB1(Up) RXD/SIN0/GPB0(Up)

UART port

ADC5/DCD1#/WUI29/GPI5(X) ADC6/DSR1#/WUI30/GPI6(X) ADC7/CTS1#/WUI31/GPI7(X) RTS1#/WUI5/GPE5(Dn) PWM7/RIG1#/GPA7(Up) DTR1#/SBUSY/GPG1/ID7(Dn) CTX1/WUI18/SOUT1/GPH2/SMDAT3/ID2(Dn) CRX1/WUI17/SIN1/SMCLK3/GPH1/ID1(Dn)

WAKE UP

PWRSW/GPE4(Up) RI1#/WUI0/GPD0(Up) RI2#/WUI1/GPD1(Up) — NBSWON# — ACIN — USB_CHARGE# 26 — ACIN 43

RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7(Dn) — EC_DGPU_VRON2 — EC_DGPU_VRON2_R R390 SHORT_4 — B-21

8518_SCK 8518_SCE# 8518_SI 8518_SO — EXTERNAL SERIAL FLASH

FSCK FSCE# FMOSI FMISO

R363 *100K/F_4 — 3V_AUX

A/D D/A

ADC0/GPI0(X) ADC1/GPI1(X) ADC2/GPI2(X) ADC3/GPI3(X) ADC4/WUI28/GPI4(X) — ICM — EC_VGA_OVT# — EC_GFXPG R388 *SHORT_4 — PLTRST_DIS_R# R454 *SHORT_4

TEMP_MBAT 43 — ICM 43 — EC_VGA_OVT# 21 — GFXPG 11,16 — PLTRST_DIS# 16

TACH2/GPJ0(X) GPJ1(X) DAC2/TACH0B/GPJ2(X) DAC3/TACH1B/GPJ3(X) — CEN_L# — CCD_KILL — CPUFAN

CEN_L# 26 — CCD_KILL 25 — CPUFAN 4

SSCE#/GPG2(X) SSCE1#/GPG0(X) — SPI ENABLE

PWRLED0# — KSO16/SMOSI/GPC3(Dn) KSO17/SMISO/GPC5(Dn) PWM6/SSCK/GPA6(Up)

KBMX

KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15

MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15

MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7

KSI0/KSTB# KSI1/ATB# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7

CLOCK — CK32KE/GPJ7(X) CK32K/GPJ6(X) — T39 — R367 *SHORT_4

ITE-IT8518E

VSS VCORE AVSS

C335 0.1U/10V_4

3V_AUX — R356 100K_4 — PCURST# — C333 1U/X7R/10V_6

3V_AUX — MBCLK1 R349 3.9K_4 — MBDATA1 R350 3.9K_4 — NBSWON# R351 10K_4 — MBCLK2 R352 4.7K_4 — MBDATA2 R353 4.7K_4 — WL_EN R433 *4.7K_4 — BT_EN R434 *4.7K_4 — LID# R451 100K_4 — EC_VGA_OVT# R199 10K_4

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

For Debug

SW4 — NBSWON# — *MSK-NTC016-AA1G-A160T

3V_AUX — Q33 DTA124EUA — NBSWON# — SUSB# — D34 1N4148WS — PCUHOLD# — R476 100K_4

PWR BOARD CON

5V_S3 — PWRLED2# — LID# — 3V_AUX — NBSWON# — B-22

C400 0.1U/10V_4 — C401 0.1U/10V_4 — C405 0.1U/10V_4 — C406 0.1U/10V_4 — C407 0.1U/10V_4

CN39 — PWR CN 88513-0601-6p-l-smt

GPU Thermal

3V_GPU — R372 2.2K_4 — MBCLK1 — Q27 2N7002 — MBCLK_GPU 21

3V_GPU — R373 2.2K_4 — MBDATA1 — Q26 2N7002 — MBDATA_GPU 21

1MB ROM

B-11

3V_AUX — 0.025A(20mils) — R357 10K_4

8518_SO R358 33_4 8518_SO_R — 8518_SI R359 33_4 8518_SI_R — 8518_SCK R361 33_4 8518_SCK_R — 8518_SCE# — R364 10K_4 — C372 *0.1U/10V_4

U24 SO VDD SI HOLD SCK WP CE VSS — W25Q80BVSSIG — C334 0.1U/10V_4

Intel Turbo mode only <CPU>

H_PROCHOT# 4,34 — H_PROCHOT_EC — R366 100K_4 — Q25 2N7002

HWPG circuit

3V_S0 — R368 10K_6

34 HWPG_VAXG — D18 *BAS316

37,39 HWPG_VTT — D19 BAS316

39 HWPG_VCCSA — D20 BAS316

38 HWPG_1.8V — D21 BAS316 — HWPG

8,33 HWPG_3/5V — D22 BAS316

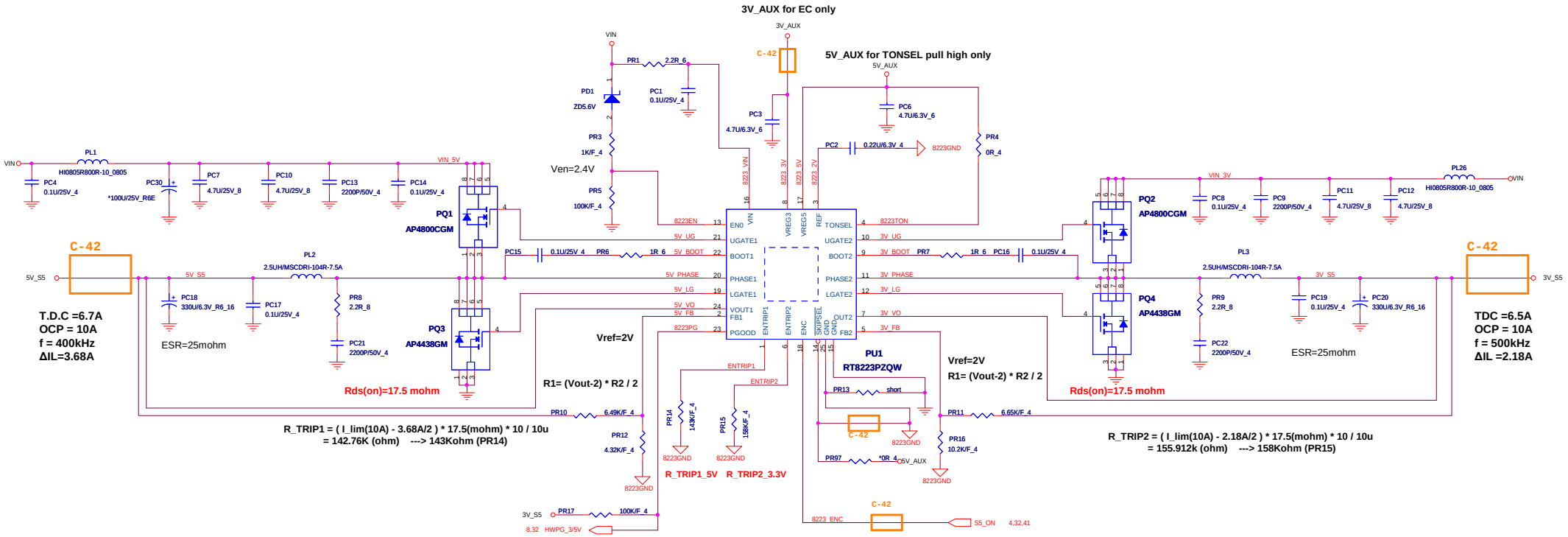
36 HWPG_1.5V — D23 BAS316

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	EC_ITE8518	B

Date: Tuesday, May 22, 2012 — Sheet 32 of 45

System 3V_S5 and 5V_S5 (RT8223PZQW)



Iripple=(Vin-Vout)*Vout/(Vin*L*f)

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	17.5m_Max	10	3.68	400	2.5uH	143K
3.3V	17.5m_Max	10	2.18	500	2.5uH	158K

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
Si4134DY	SO-8	9.9A/14A	17.5m
AO4712	SO-8	10A/11.2A	18.0m
AO4710	SO-8	11A/12.7A	14.2m
AP4438GSM	SO-8	7A/11.7A	18.0m
DMG4812	SO-8	9.6A/10.7A	18.5m
AON7702	DFN3x3	11A/20A	14.0m

Power On sequencing

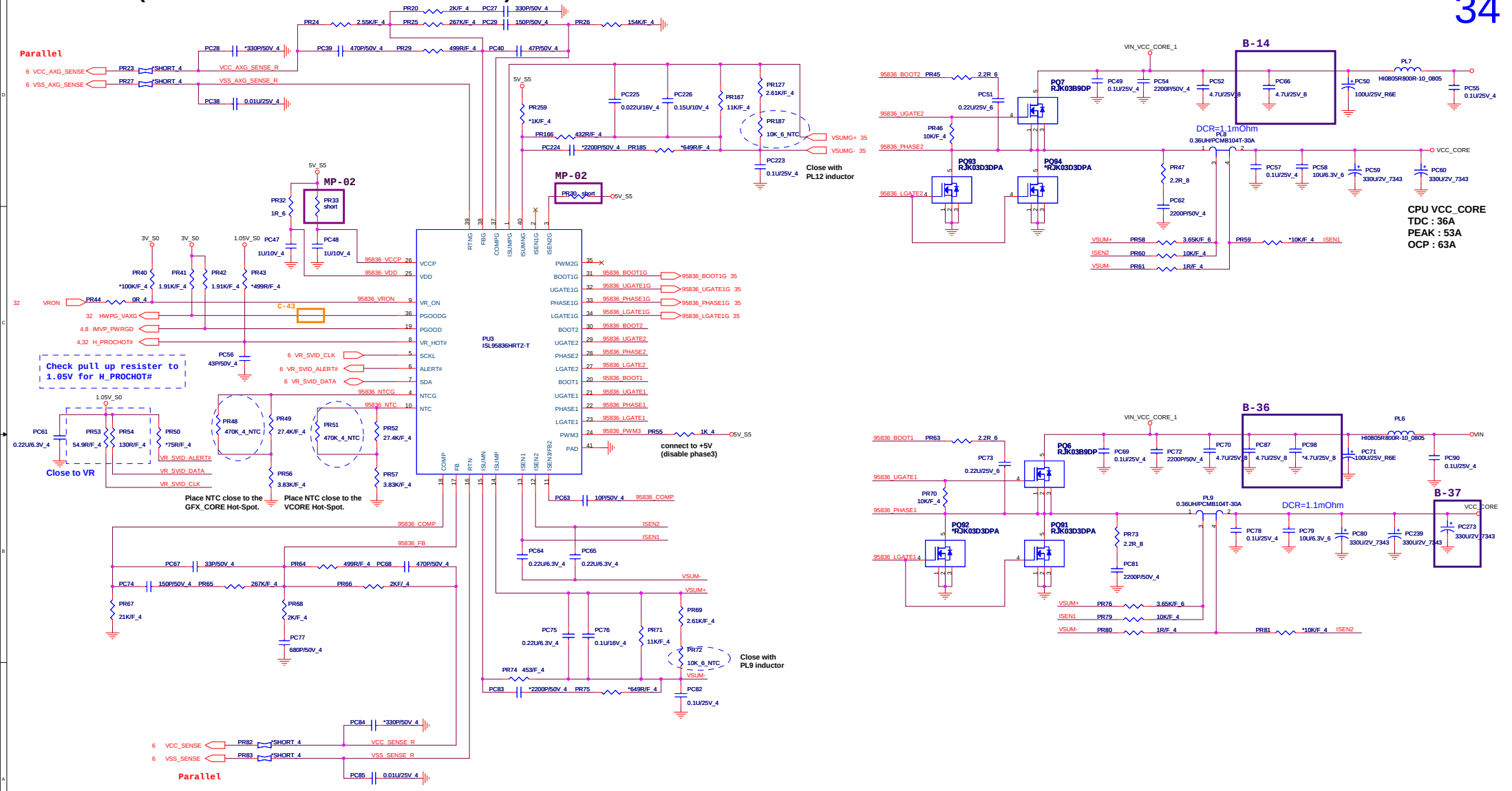
EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	System 3V_S5 and 5V_S5 (RT8223PZQW)	B

Date: Tuesday, May 22, 2012 Sheet 33 of 45

CPU VCORE (ISL95836HRTZ-T and ISL6208CRZ-T)



Inductor information

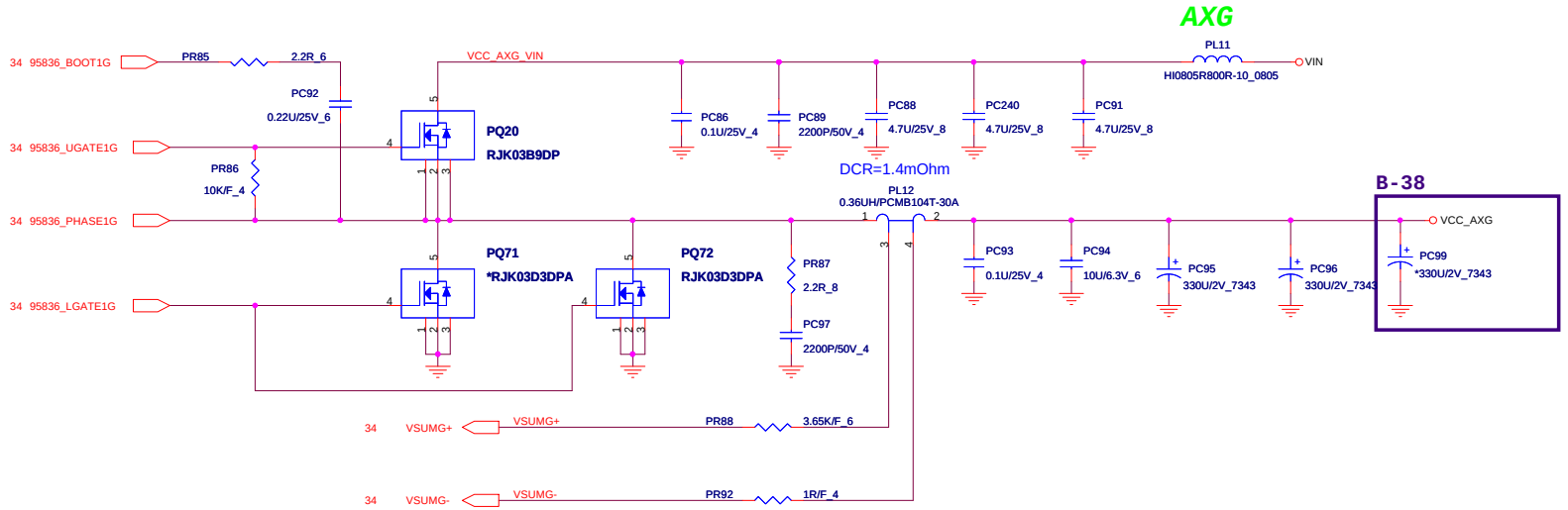
Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	CYN	CV+36V0MZ13	30	50	1.4m Max.	10x10x4	PCMB104T-R36MT
0.36uH 20%	Panasonic	CV+18V0MZ04	30	34	1.4m Max.	10x10x4	ETQP4LR36WFC

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	CPU_CORE (ISL95836HRTZ-T and ISL6208CRZ-T)	S

Date: Tuesday, May 22, 2012 Sheet 34 of 45

VCC_AXG (ISL95836HRTZ-T)



CPU VCC_AXG
TDC : 21.5A
PEAK :33A
OCP : 39A
Width : 1400mil

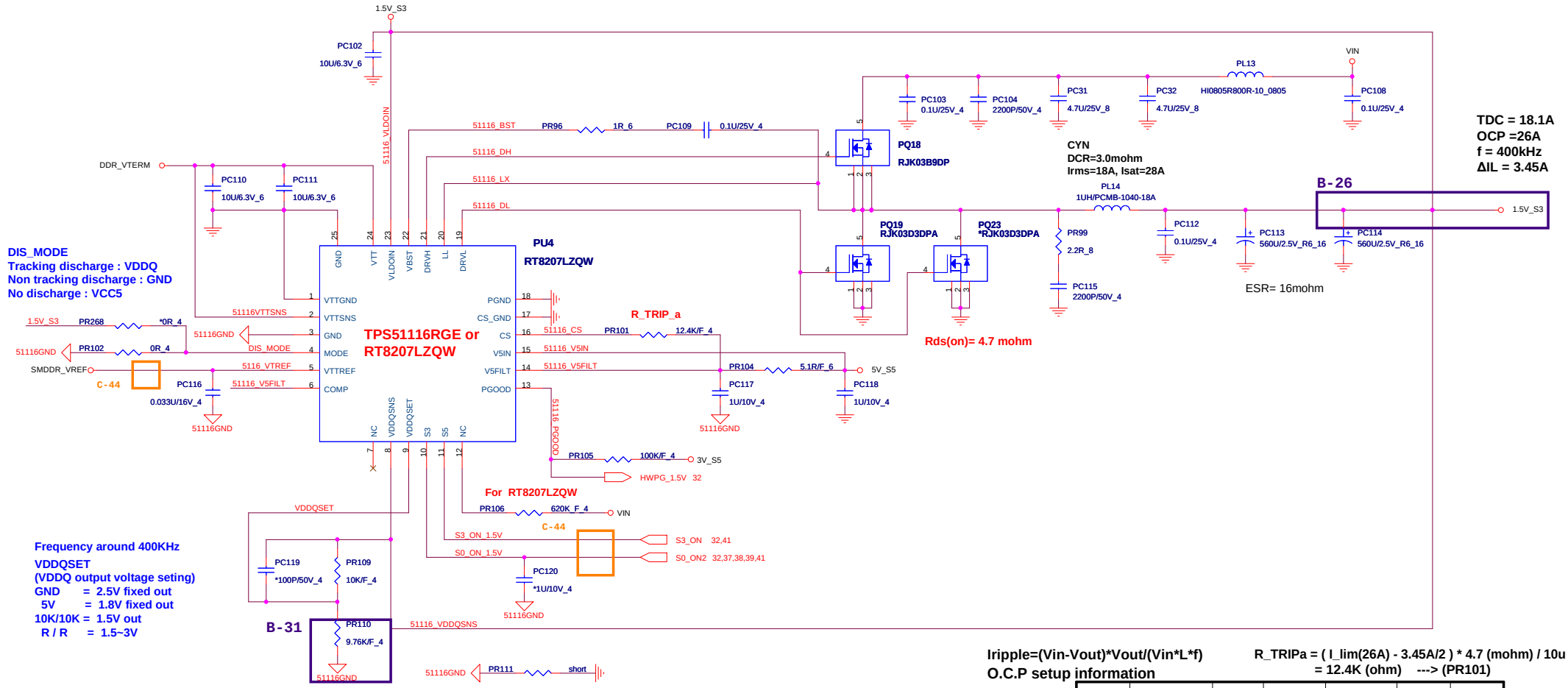
L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	Panasonic	CV+36Q0MZ00	20	25	1.4m Max.	7X7X4	ETQP4LR36AFM

DDR3 1.5V_S3 (TPS51116RGE or RT8207LZQW)



Iripple=(Vin-Vout)*Vout/(Vin*L*f)

R_TRIPa = (I_lim(26A) - 3.45A/2) * 4.7 (mohm) / 10u
= 12.4K (ohm) ---> (PR101)

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	4.7m_Max	26	3.45	400	1uH	12.4K

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	DDR3 1.5V_S3 (RT8207LZQW)	B

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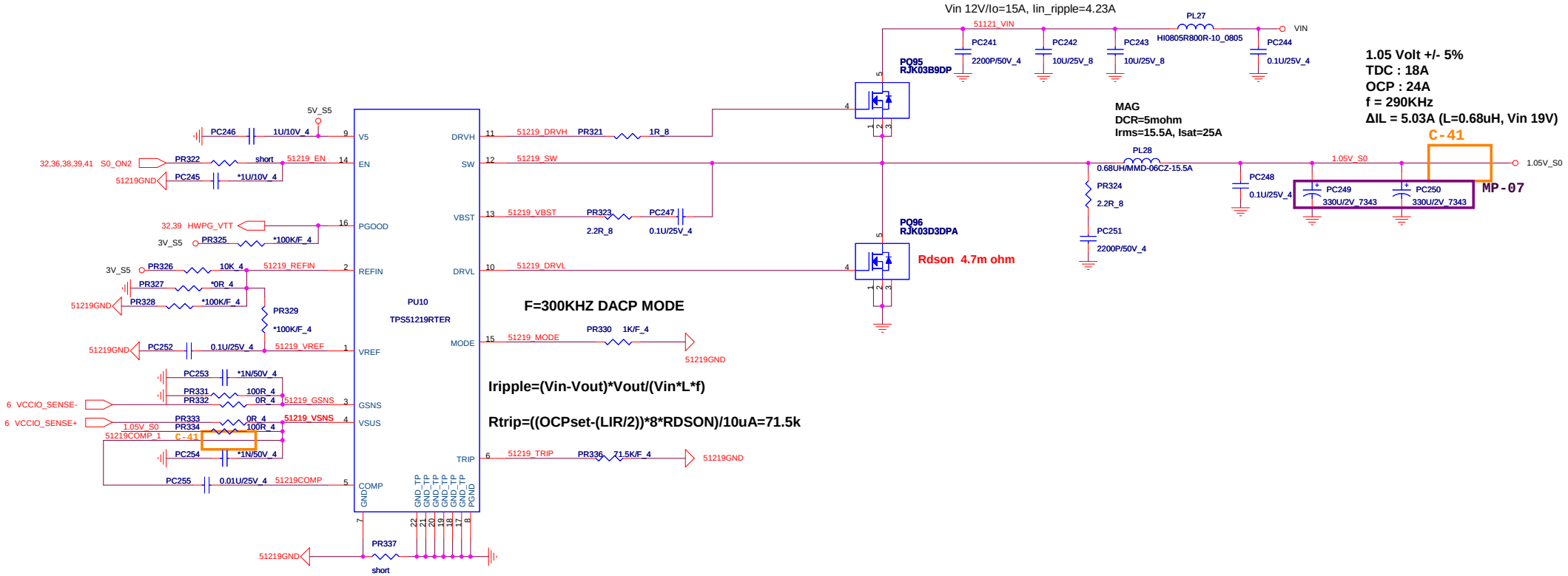
VCCIO and 1.05V_PCH (TPS51219RTER)



VCCIO_SENSE- connect to the GND sense point of the load
VCCIO_SENSE+ connect to the load voltage sense point.

Output Voltage Selection

RFIN=3.3V	output voltage=1.05V
RFIN=GND	output voltage=1.00V
Resister Divider	Adjutable from VREF

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.05V	4.3m_Max	24	3.306	300	1uH	56.2K

Quanta Computer Inc.
PROJECT : FH6C_HM70

Size	Document Number	Rev
	VCCIO and 1.05V_PCH (TPS51219RTER)	B

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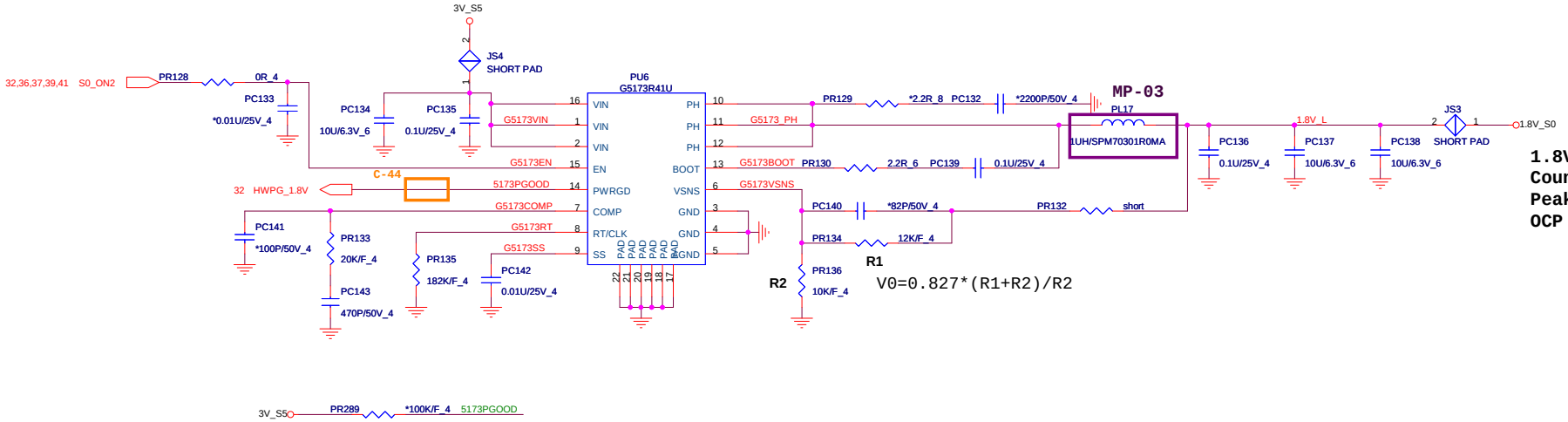
1.8V_S0(G5173R41U)



1.8V_S0 +/- 5%
Countinue current:1.4A
Peak current:3A
OCP minimum 4.5A

Quanta Computer Inc.		
PROJECT : FH6C_HM70		
Size	Document Number	Rev
	1.8V_S0(G5173R41U)	B
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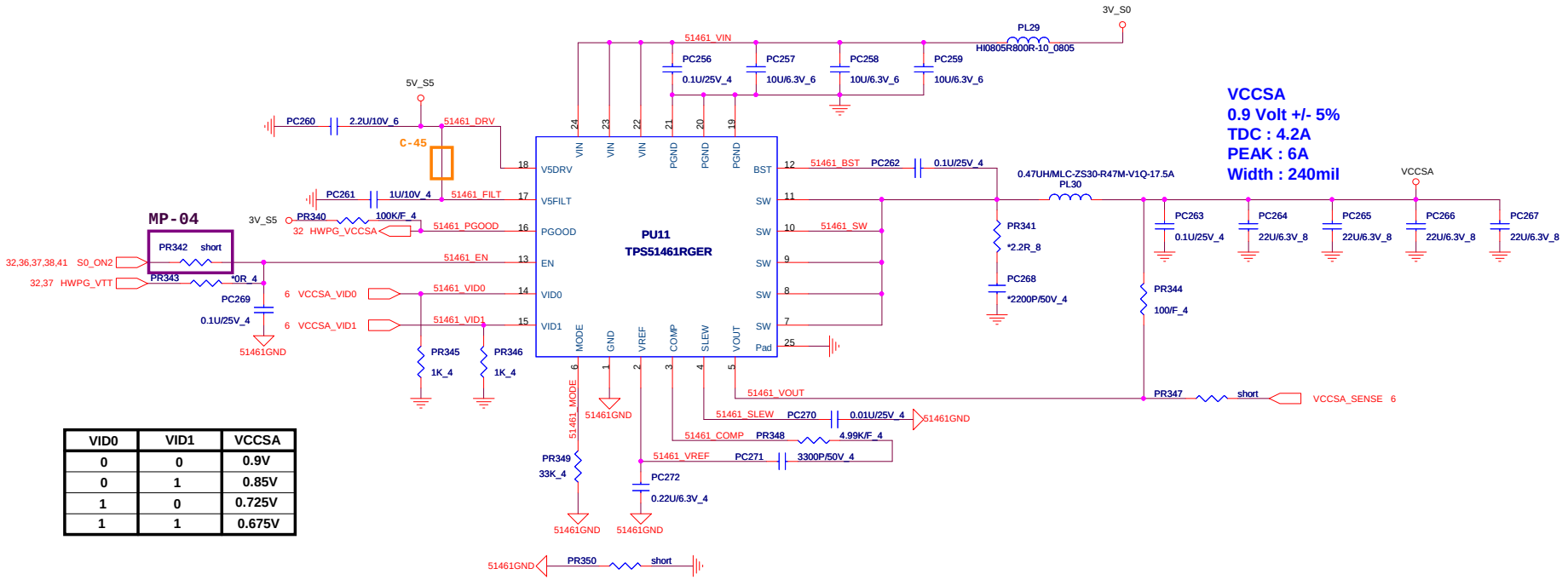
VCCSA (TPS51461RGER)



VID0	VID1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.725V
1	1	0.675V

Quanta Computer Inc.

PROJECT : FH6C_HM70

Size	Document Number	Rev
	VCCSA (TPS51461RGER)	B

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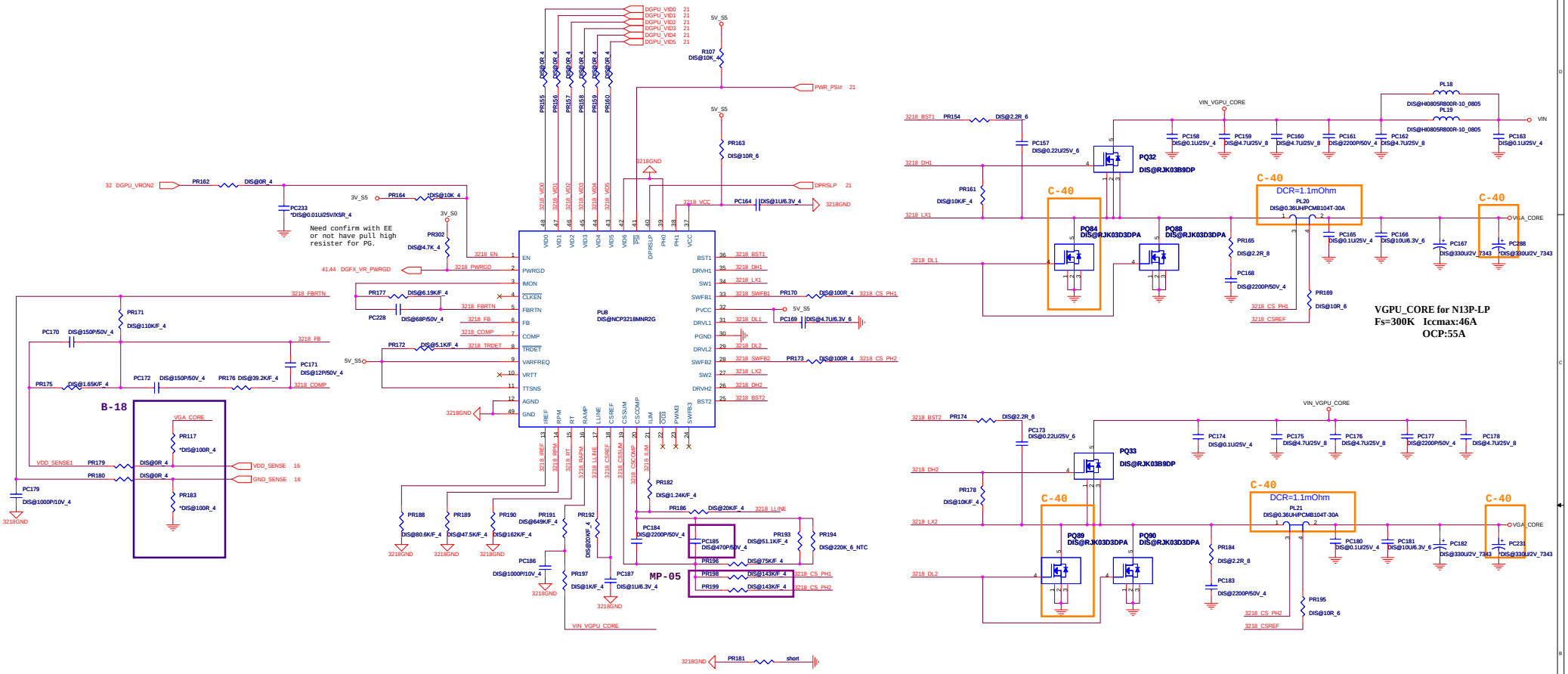
VGA_CORE (NCP3218MNR2G)



L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	CYN	CV+36V0MZ13	20	25	1.2m Max.	7x7x3	PCMB104T-R36MT
0.36uH 20%	Panasonic	CV+36Q0MZ00	20	25	1.4m Max.	7x7x3	ETQP4LR36AFM

Quanta Computer Inc.
PROJECT : FH6C_HM70
VGA_CORE (NCP3218MNR2G)
Size: Document Number: Rev: B
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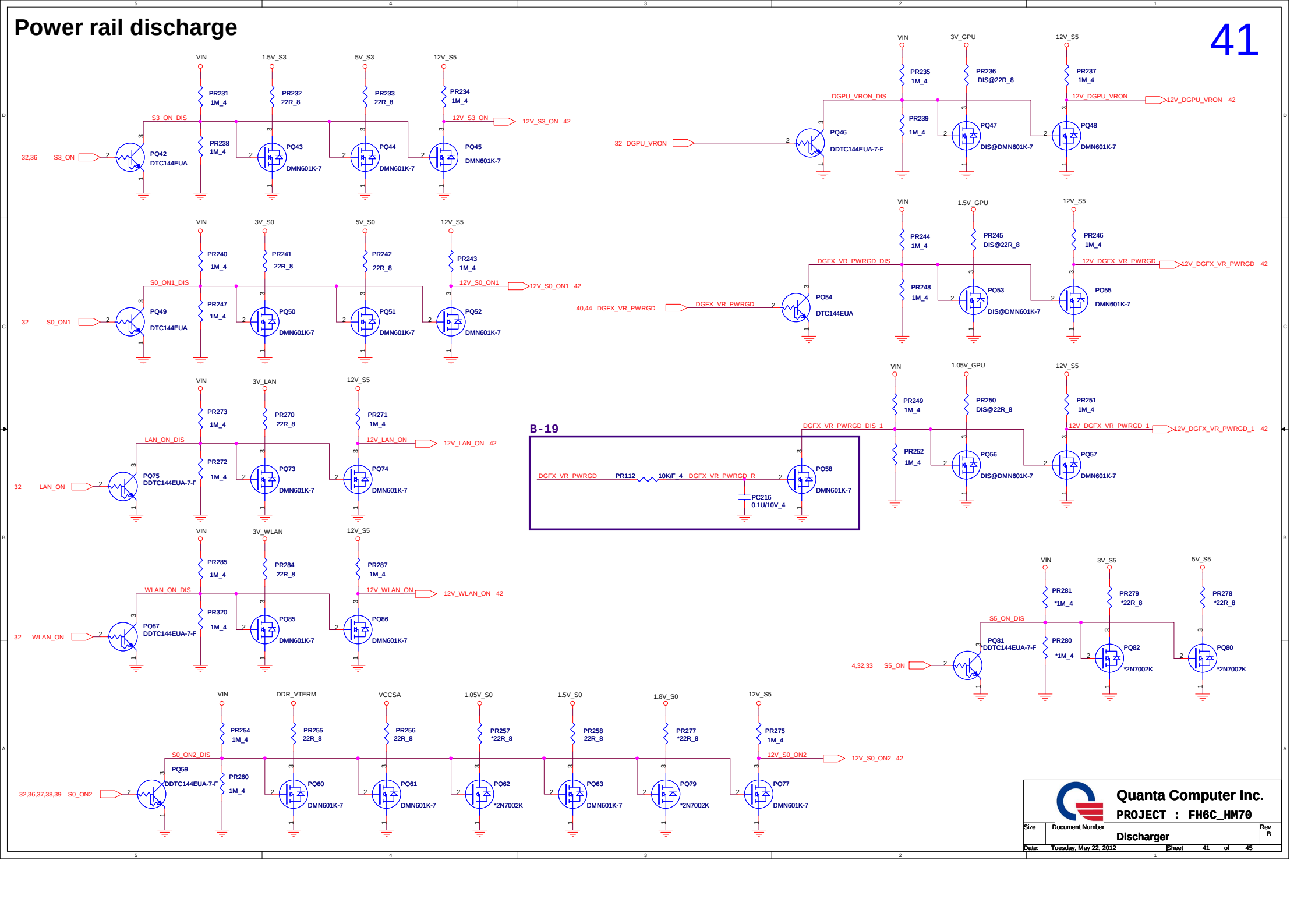
Power rail discharge



Quanta Computer Inc.		
PROJECT : FH6C_HM70		
Size	Document Number: Discharger	Rev: B
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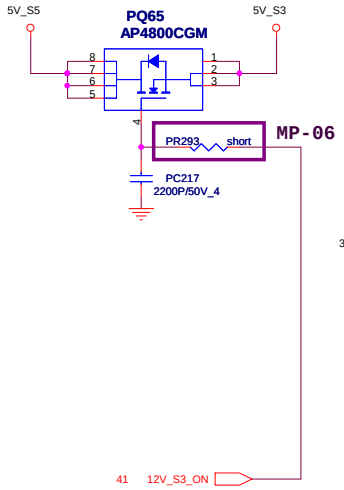
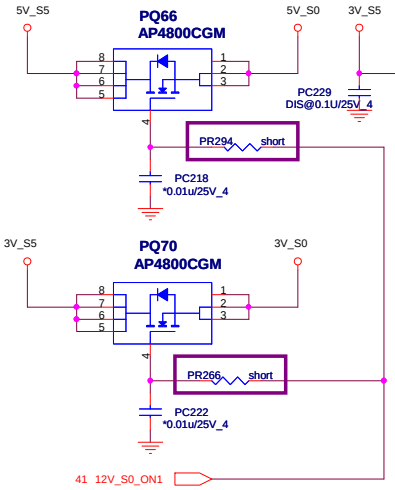
Load Switch

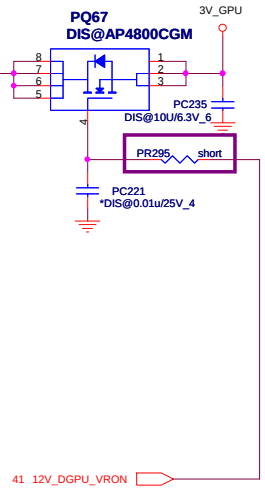
S3 ON Load SW



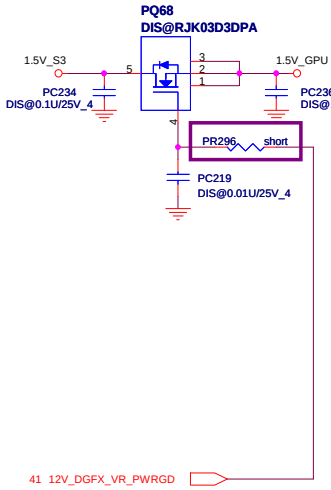
S0 ON1 Load SW



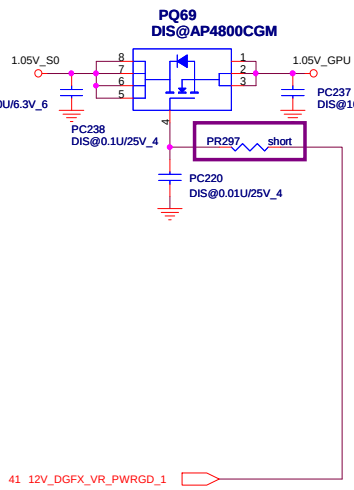
DGPU VRON Load SW



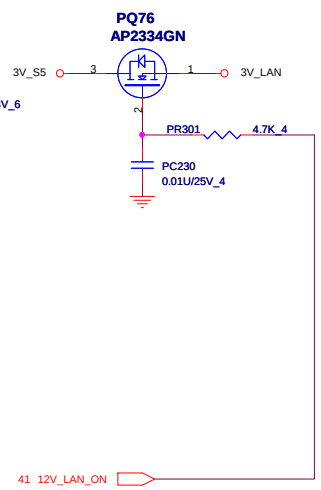
DGFX_VR_PWRGD Load SW



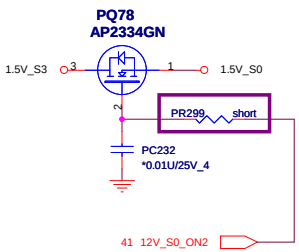
DGFX_VR_PWRGD_1 Load SW



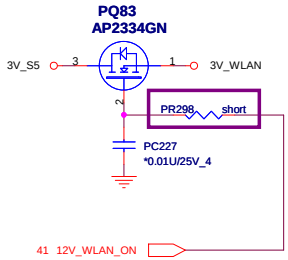
LAN_ON Load SW



S0 ON2 Load SW



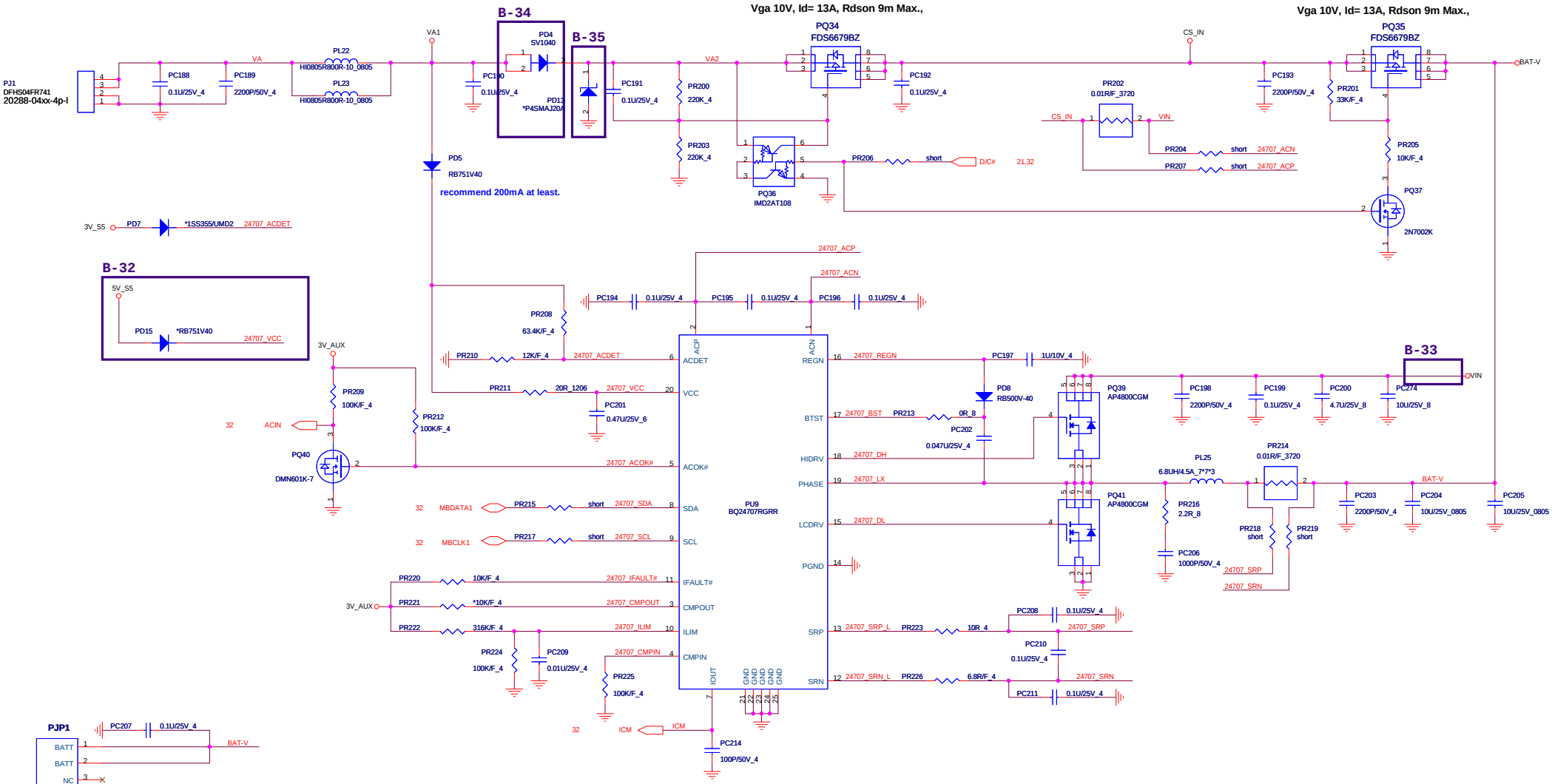
WLAN_ON Load SW



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO4468	SO-8	8.4A/10.4A	22m	+/- 20V
AP4800CGM	SO-8	7.5A/10.4A	22m	+/- 20V
Si4128DY	SO-8	7.0A/10.9A	30m	+/- 20V
Si4134DY	SO-8	7.0A/14A	17.5m	+/- 20V
ME3424D	TSOP-6	5.0A/6.7A	42m	+/- 20V
AP2334GN	SOT-23	4.5A/5.0A	42m	+/- 20V
AO3404	SOT-23	5.0A/5.8A	43m	+/- 20V

Adapter/Battery input & Charger



H/L side Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
AO4468	SO-8	10A/11.6A	22m	NO
AO4712	SO-8	10A/11.2A	18.0m	YES
Si4128DY	SO-8	7.0A/10.9A	30m	NO
Si4134DY	SO-8	7.0A/14A	17.5m	NO
AP4800CGM	SO-8	7.5A/10.4A	22m	NO

Quanta Computer Inc.
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Size	Document Number	Rev
	Charger (BQ24707RGRR)	B

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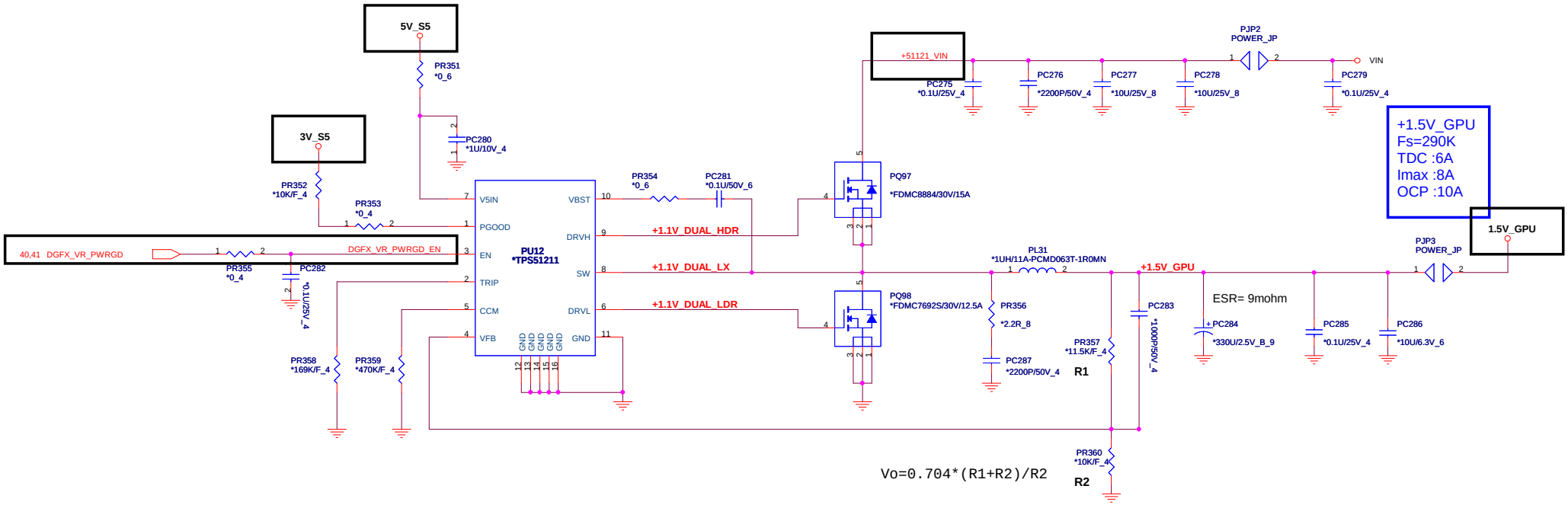

Quanta Computer Inc.		
PROJECT : FH6C_HM70		
Size	Document Number: +1.5V_GPU	Rev: B
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FH6C Mother Board Schematics Revision History

PCB Rev	Sch Rev	BOM Rev	DATE	Change List & Description
B	B		0426	USB S5 Charge U30.2.3 from USBP0_R-, USBP0_R+ to USBP2_R-, USBP2_R+
B	B		0426	USB S5 Charge U30.7.8 from USBP0-, USBP0+ to USBP2-, USBP2+
B	B		0426	CN8.1 USBPWR_P0 swap to CN10.1 +5V_USB0
B	B		0426	Change CON3 from 12Pin to 6Pin 1.0 pitch connector for factoryRequirements

Quanta Computer Inc.
PROJECT : FH6C_HM70
Size | Document Number: Change List | Rev: B
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