MS-7507

Version 1.0

CPU:

- Intel Prescott (L2=2MB) - 3.4G & Above
- Intel Cendar Mill (65nm) - 3.73G & Above
- Intel Smithfield (90nm Dual core)
- Intel Conroe (65W Dual core)

System Chipset:

- Intel Lakeport - MCH (North Bridge)
- Intel ICH7R (South Bridge)

On Board Chipset:

- BIOS -- SPI
- HD -- ALC888
- LPC Super I/O -- F71882FG
- LAN-- REALTEK RTL8111C Co-lay RTL8101E
- CLOCK -- RTM876-660

Main Memory:

- DDR II *2 (Max 2GB)

Expansion Slots:

- PCI2.3 SLOT * 2
- PCI EXPRESS X1 SLOT
- PCI EXPRESS X16 SLOT

ST PWM:

- Controller: 3 PHASES

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MS-7507

Size: Custom | Document Description: Cover Sheet | Rev: 0A

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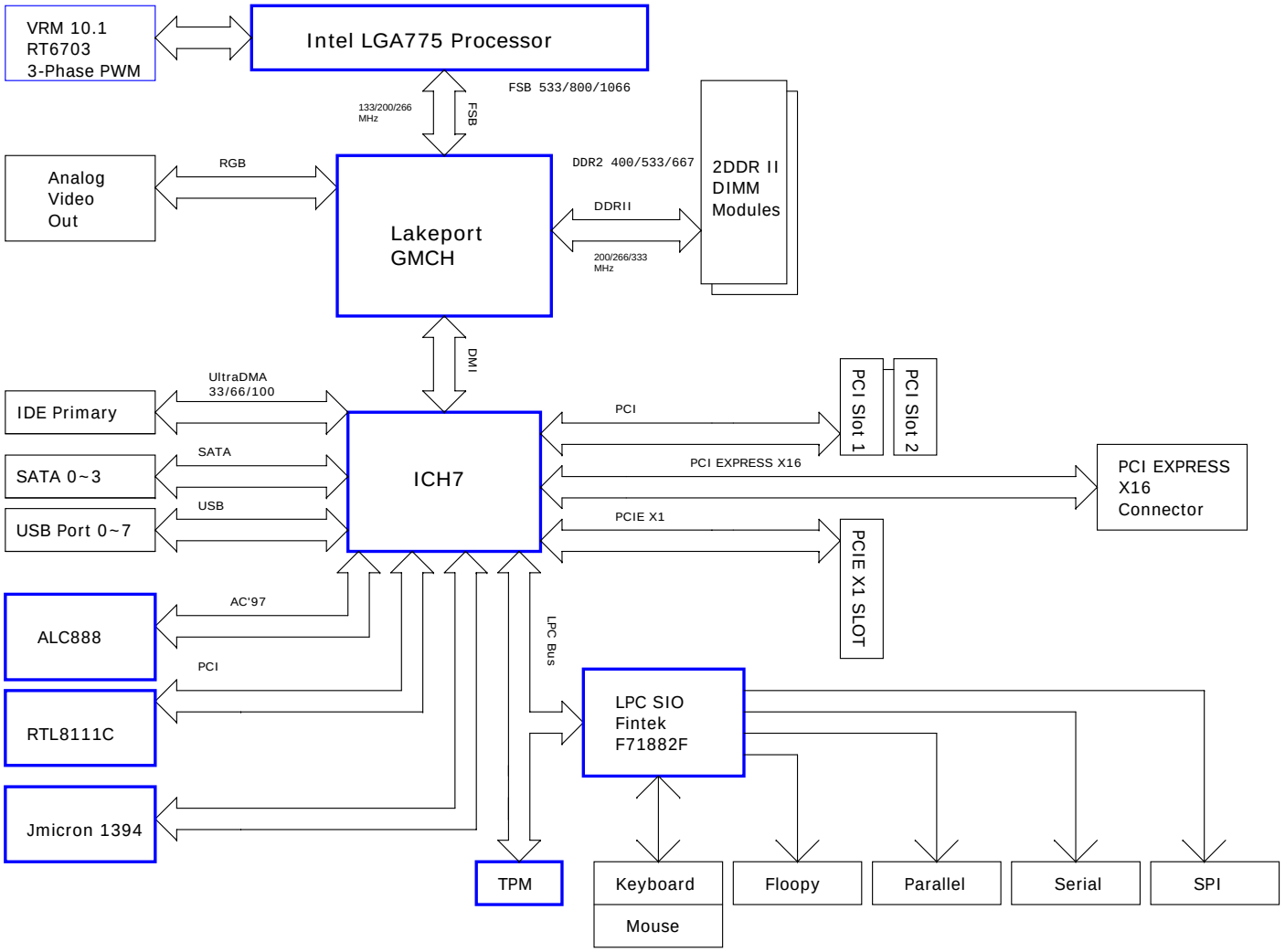
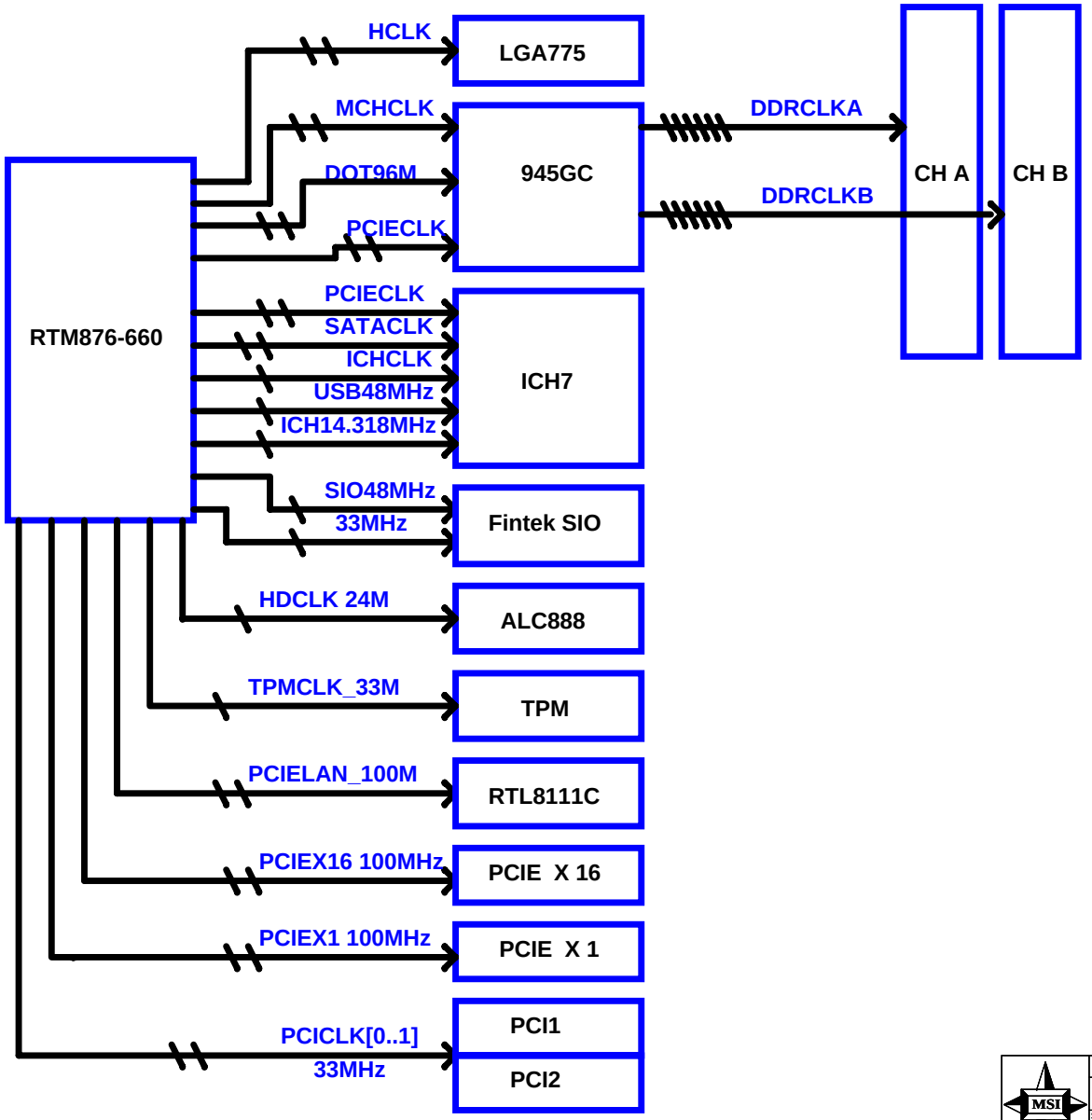
Block Diagram



MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 0A
Date: Wednesday, October 10, 2007	Sheet 2 of 34	

CLOCK MAP



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MS-7507		
Size: Custom	Document Description: CLOCK MAP	Rev: 0A
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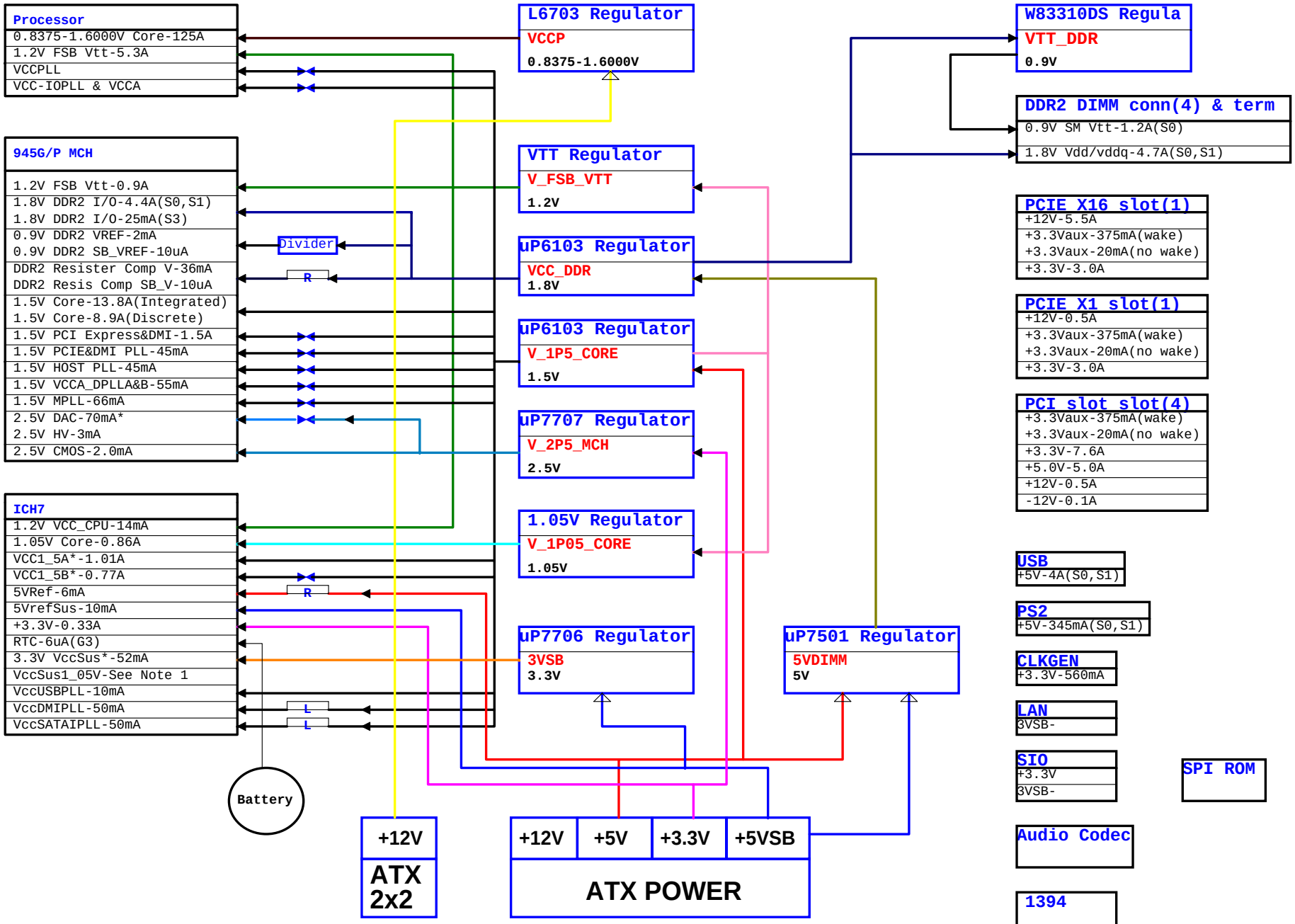

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MS-7507

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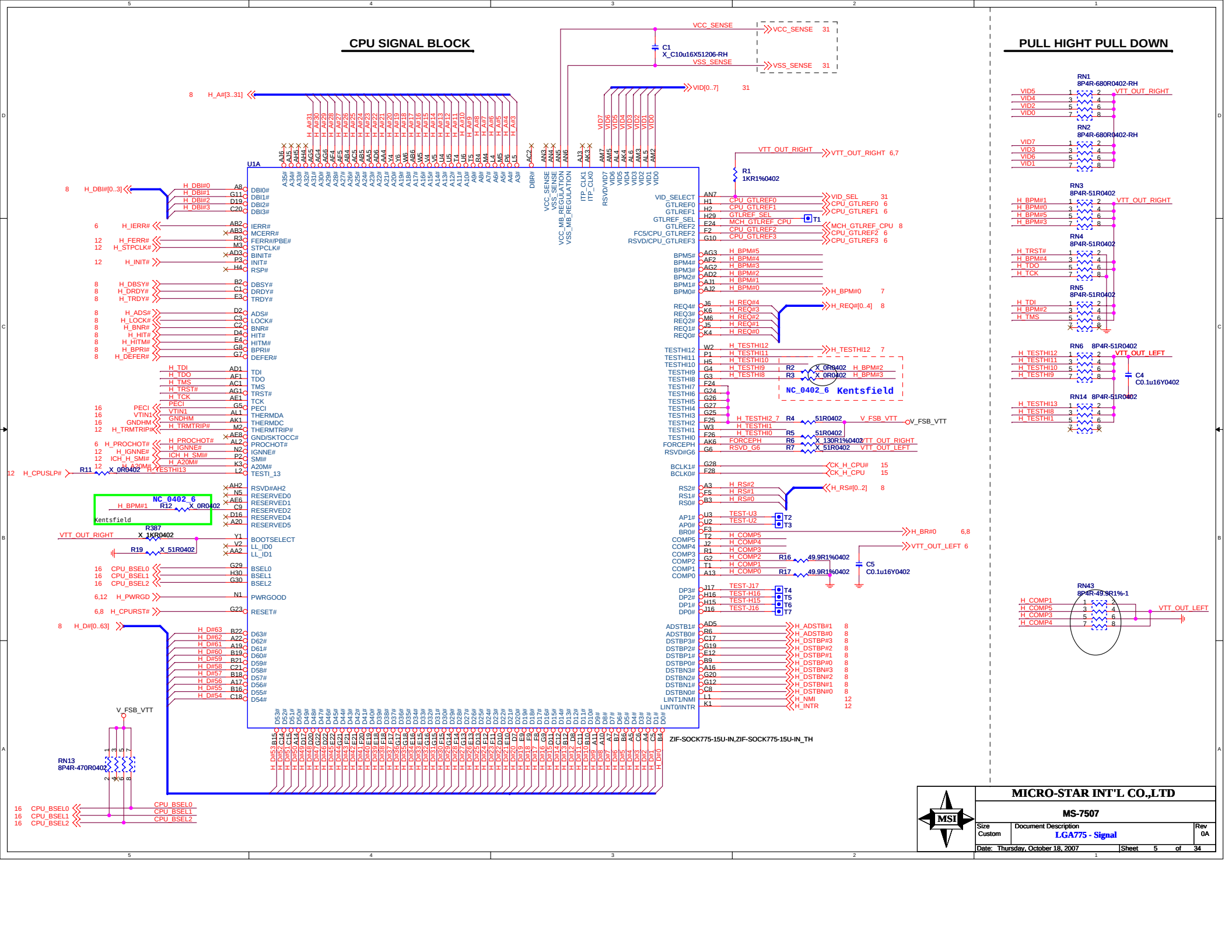
CPU SIGNAL BLOCK
PULL HIGHT PULL DOWN
U1A
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
NC_0402_6
Kentsfield
MICRO-STAR INT'L CO.,LTD
MS-7507
LGA775 - Signal
Date: Thursday, October 18, 2007
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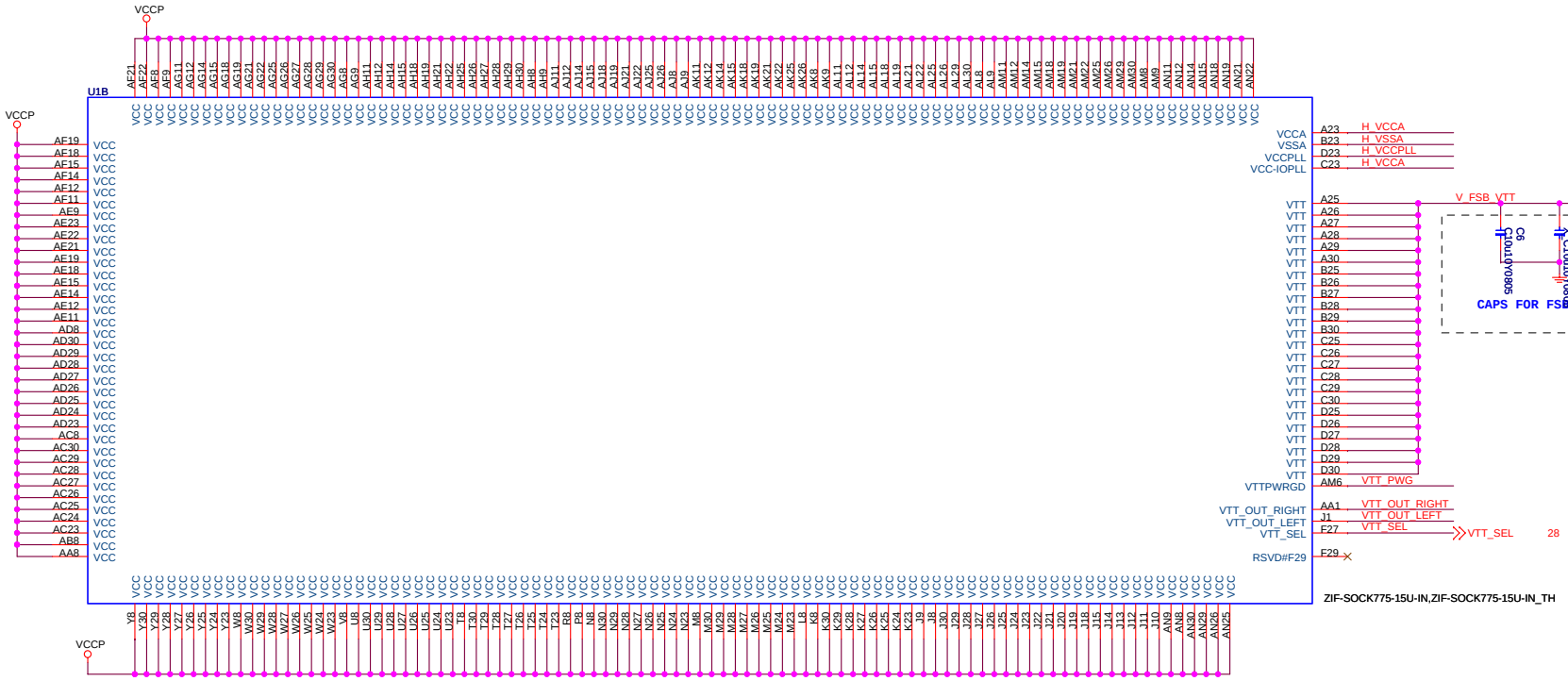
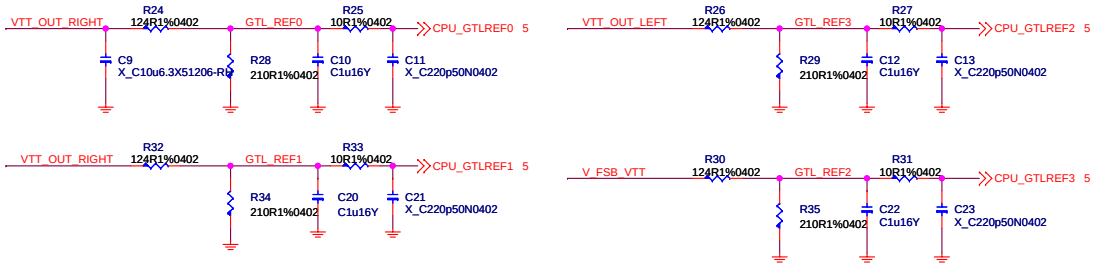
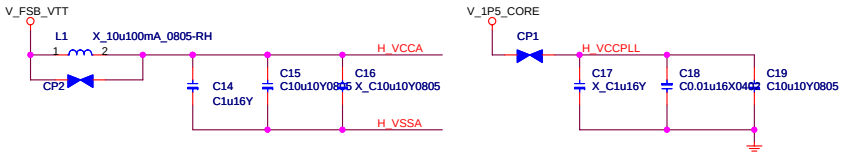


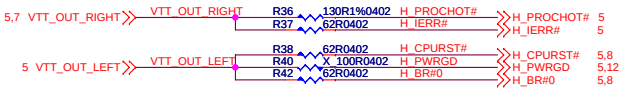
*GTLREF VOLTAGE SHOULD BE 0.67 * VTT = 0.8V (At VTT=1.2V)



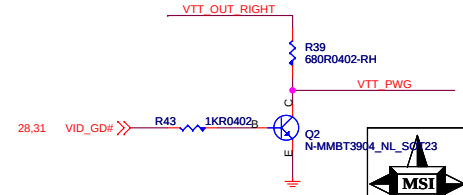
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



VTT_PWRGOOD



VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: LGA775 - Power	Rev: 0A
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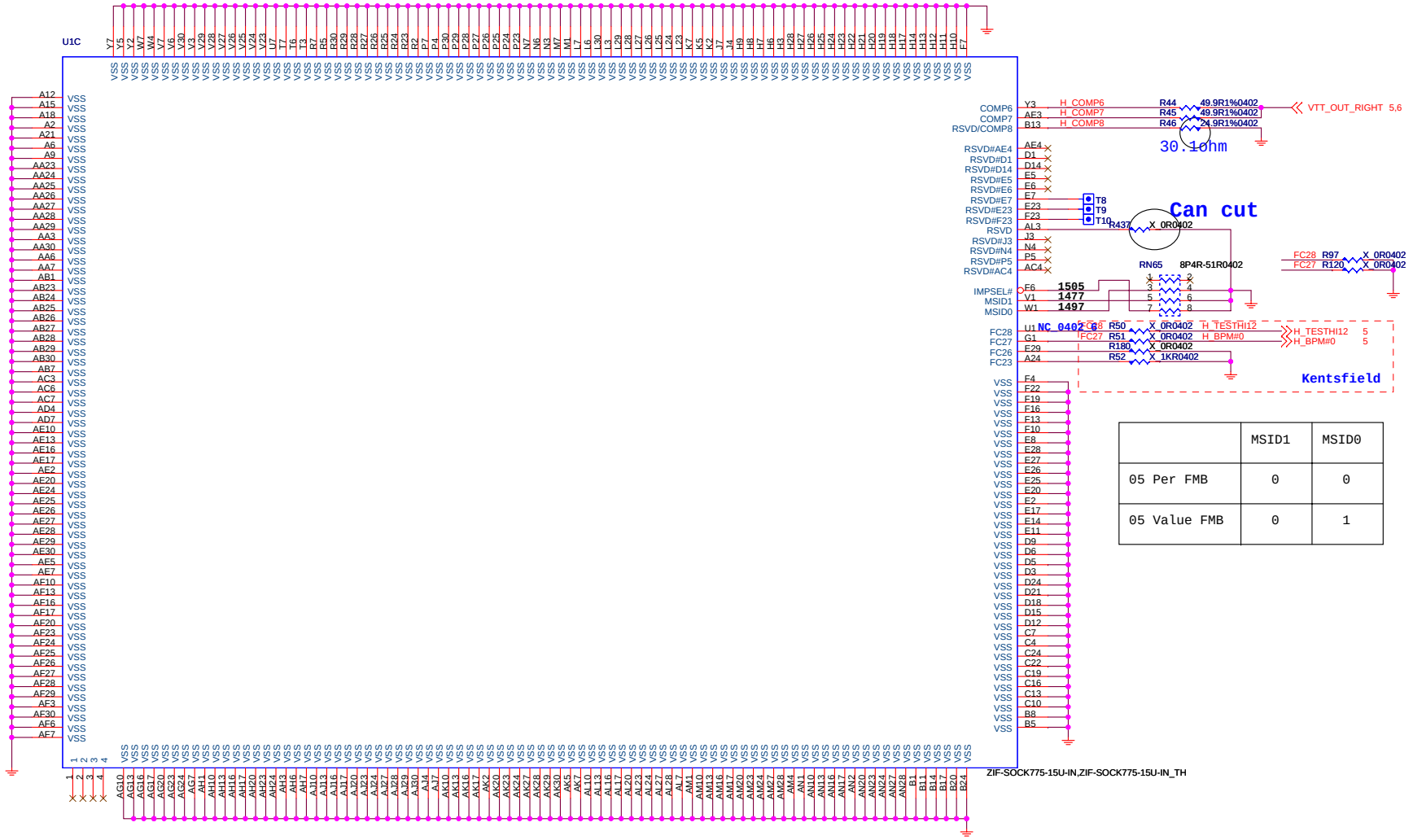
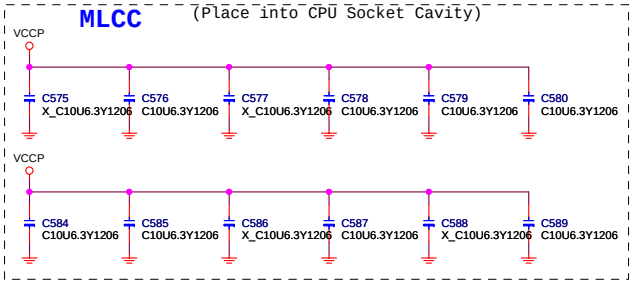


	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1



MICRO-STAR INT'L CO.,LTD

MS-7507

Size	Document Description	Rev
Custom	LGA775 - GND	0A

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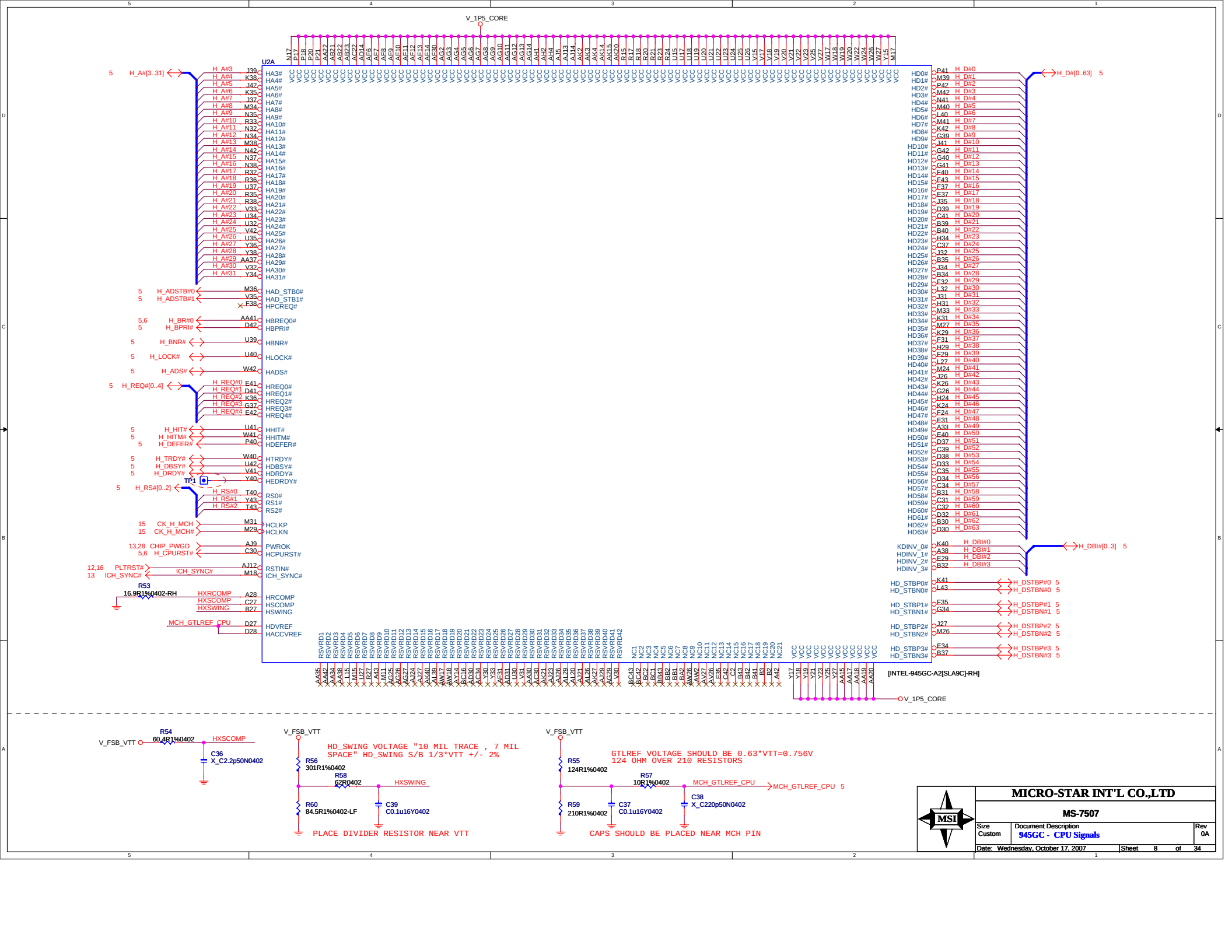
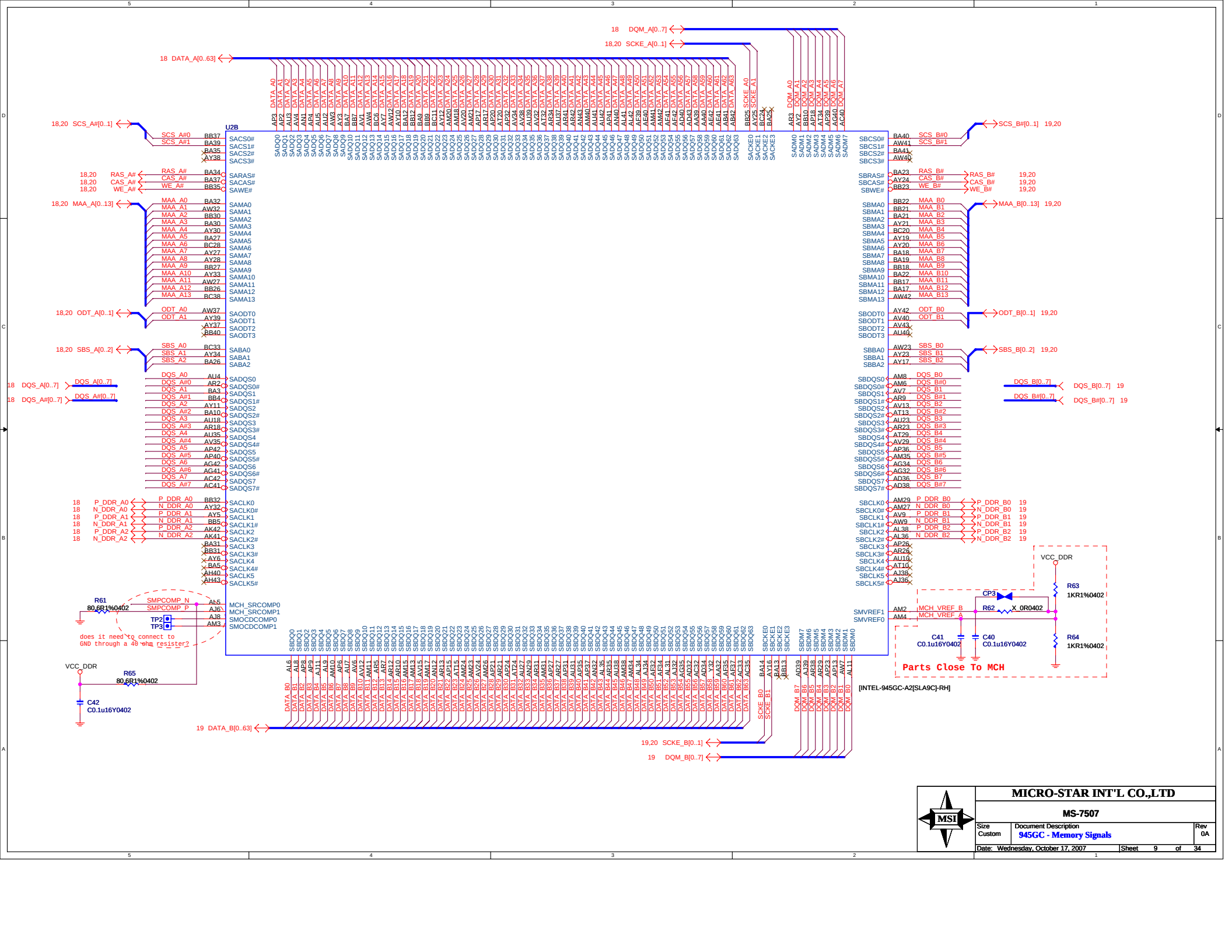

V_1P5_CORE
U2A
[INTEL-945GC-A2[SLA9C]-RH]
R53
16.9R1%0402-RH
R54
60.4R1%0402
C36
X_C2.2p50N0402
V_FSB_VTT
HD_SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD_SWING S/B 1/3*VTT +/- 2%
R56
301R1%0402
R58
62R0402
R60
84.5R1%0402-LF
C39
C0.1u16Y0402
PLACE DIVIDER RESISTOR NEAR VTT
GTLREF VOLTAGE SHOULD BE 0.63*VTT=0.756V
124 OHM OVER 210 RESISTORS
R55
124R1%0402
R57
10R1%0402
R59
210R1%0402
C37
C0.1u16Y0402
C38
X_C220p50N0402
CAPS SHOULD BE PLACED NEAR MCH PIN
MICRO-STAR INT'L CO.,LTD
MS-7507
945GC - CPU Signals
Wednesday, October 17, 2007
Sheet 8 of 34



MICRO-STAR INT'L CO.,LTD			
MS-7507			
Size: Custom	Document Description: 945GC - Memory Signals		Rev: 0A
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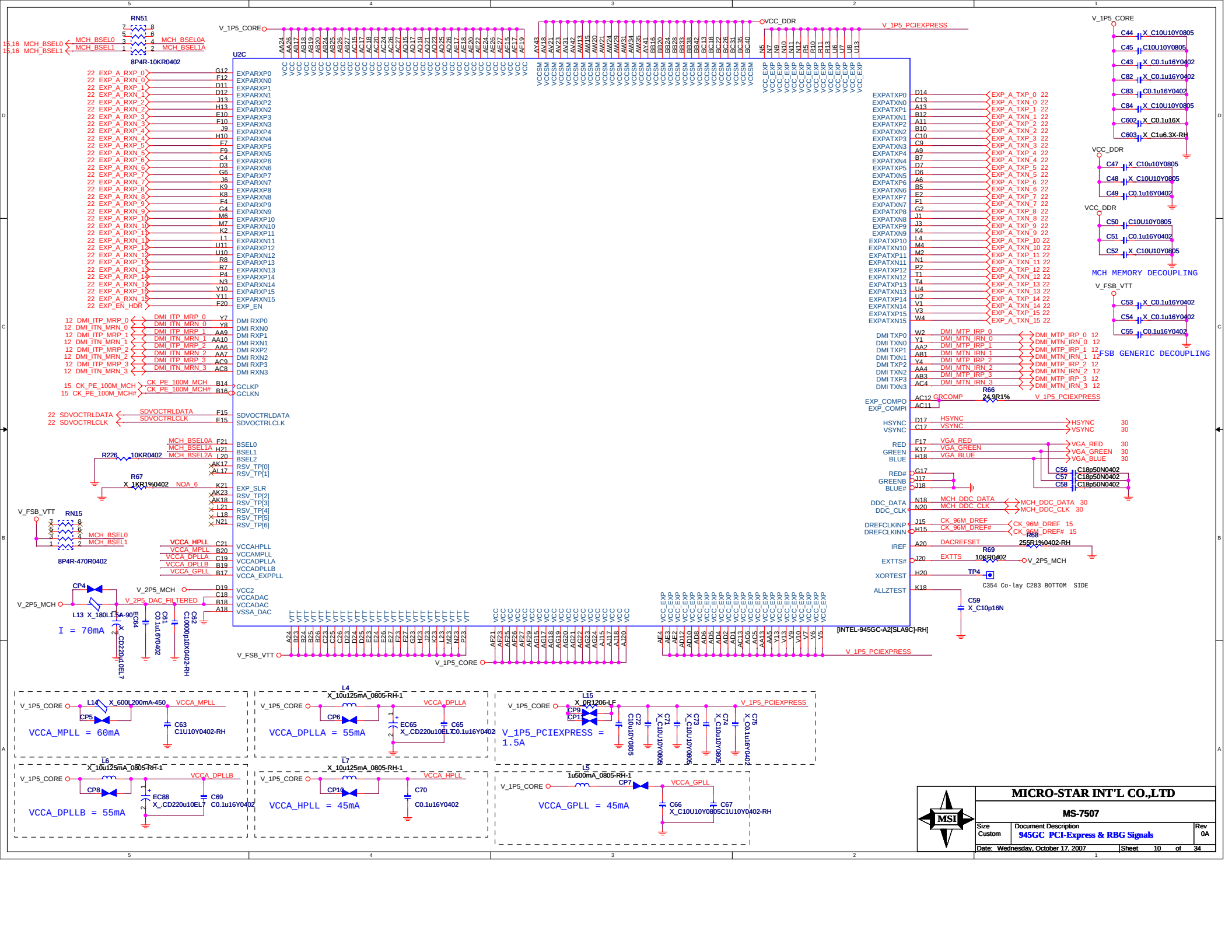
RN51
8P4R-10KR0402
U2C
[INTEL-945GC-A2[SLA9C]-RH]
MCH MEMORY DECOUPLING
FSB GENERIC DECOUPLING
R66
24.9R1%
R67
X_1KR1%0402
R226
10KR0402
RN15
8P4R-470R0402
R69
10KR0402
R68
255R1%0402-RH
TP4
C354 Co-lay C283 BOTTOM SIDE
C59
X_C10p16N
L13
X_180LL15A-90
I = 70mA
L4
X_10u125mA_0805-RH-1
L15
X_0R1206-LF
L6
L7
L5
1u500mA_0805-RH-1
VCCA_MPLL = 60mA
VCCA_DPLLA = 55mA
V_1P5_PCIEXPRESS = 1.5A
VCCA_DPLLB = 55mA
VCCA_HPLL = 45mA
VCCA_GPLL = 45mA
MICRO-STAR INT'L CO.,LTD
MS-7507
945GC PCI-Express & RBG Signals
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Rev 0A
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MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: Intel .945GC - GND	Rev: 0A
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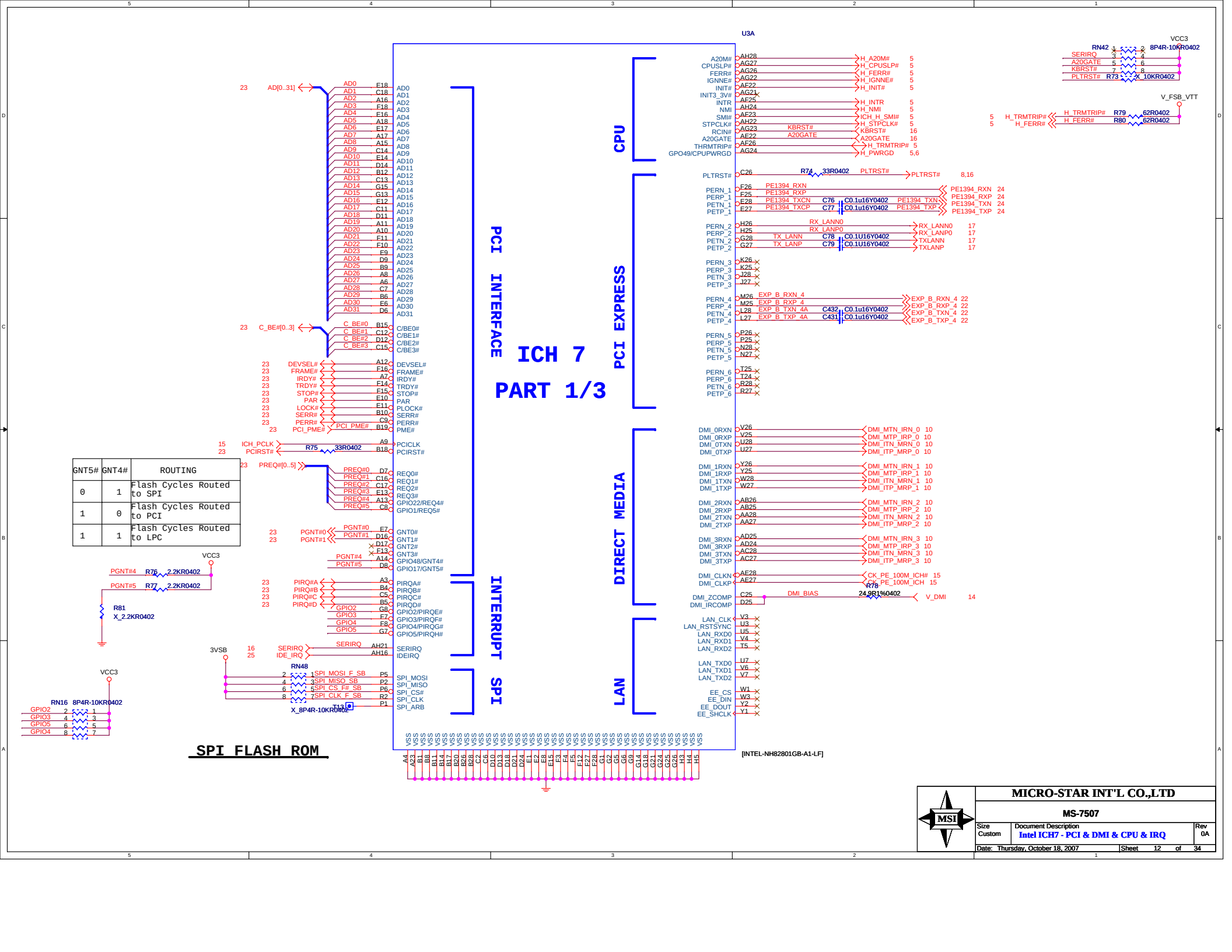
ICH 7
PART 1/3
PCI INTERFACE
PCI EXPRESS
DIRECT MEDIA
CPU
INTERRUPT
SPI
LAN
U3A
SPI FLASH ROM
[INTEL-NH82801GB-A1-LF]
GNT5# GNT4# ROUTING
0 1 Flash Cycles Routed to SPI
1 0 Flash Cycles Routed to PCI
1 1 Flash Cycles Routed to LPC
MICRO-STAR INT'L CO.,LTD
MS-7507
Intel ICH7 - PCI & DMI & CPU & IRQ
Rev 0A
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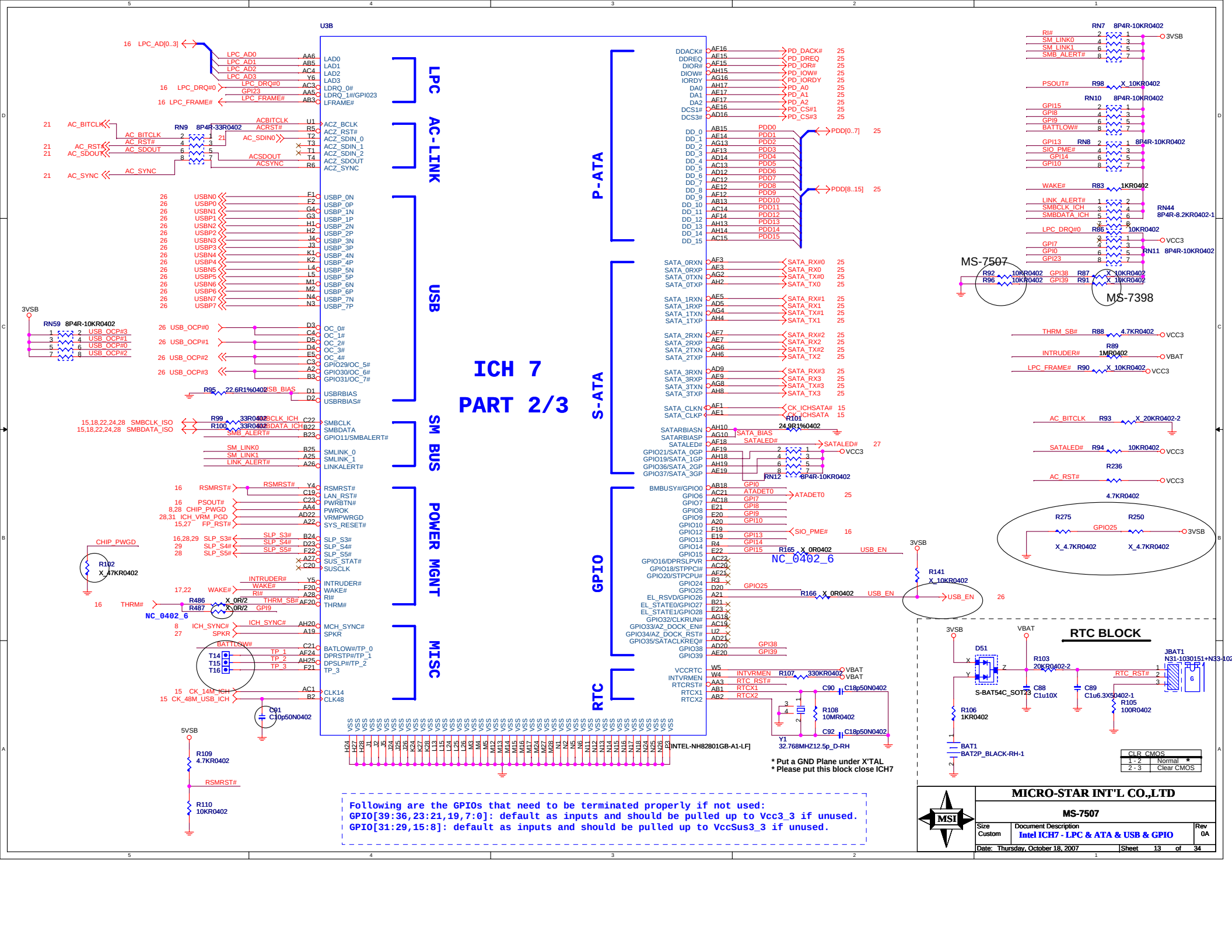
U3B
ICH 7
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
INTEL-NH82801GB-A1-LF]
RTC BLOCK
MS-7507
MS-7398
NC_0402_6
* Put a GND Plane under X'TAL
* Please put this block close ICH7
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
MICRO-STAR INT'L CO.,LTD
MS-7507
Intel ICH7 - LPC & ATA & USB & GPIO
Date: Thursday, October 18, 2007
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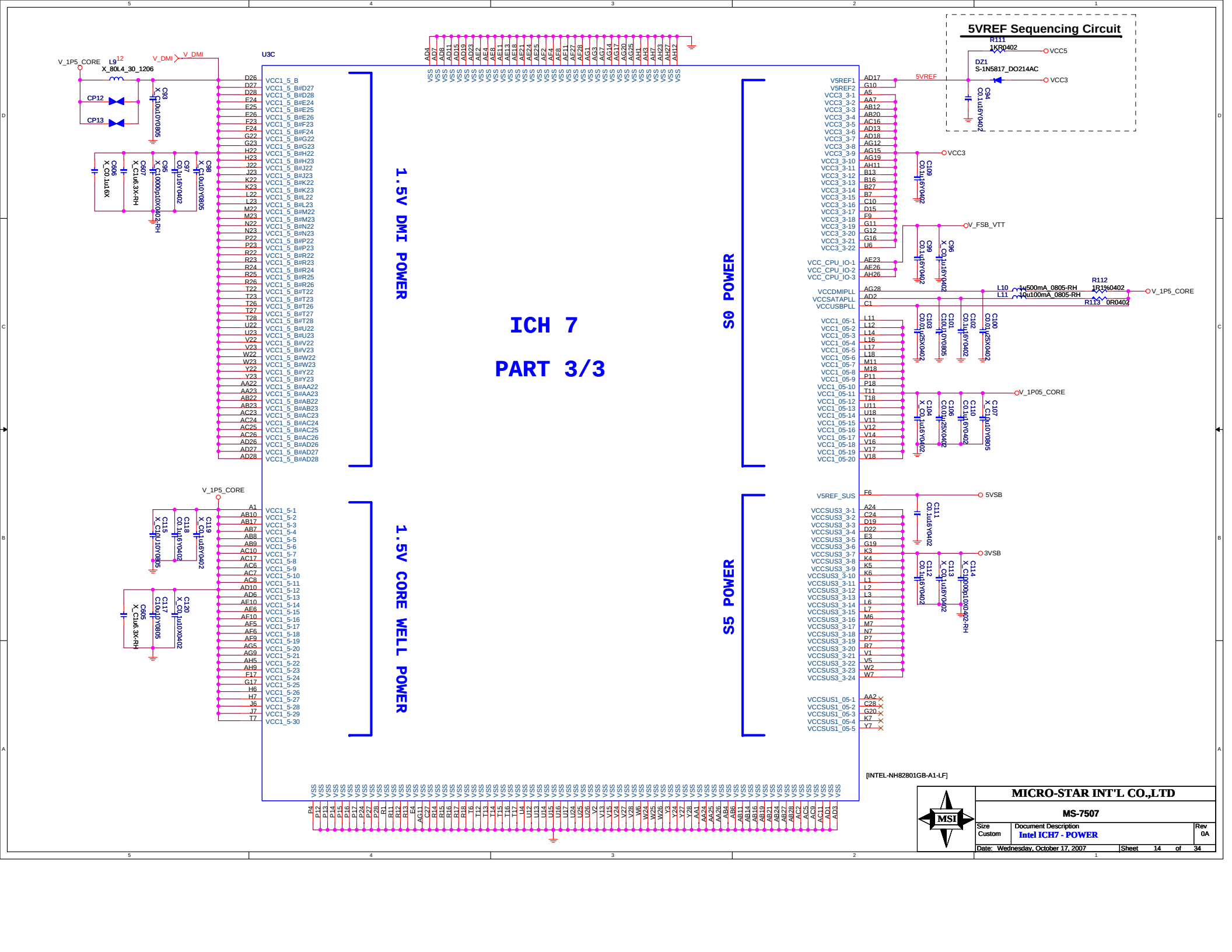
ICH 7
PART 3/3
1.5V DMI POWER
1.5V CORE WELL POWER
S0 POWER
S5 POWER
U3C
5VREF Sequencing Circuit
R111 1KR0402
VCC5
DZ1 S-1N5817_DO214AC
VCC3
C94 C0.1u16Y0402
5VREF
V_1P5_CORE
L9 X_80L4_30_1206
V_DMI
CP12
CP13
C93 X_C10u10Y0805
C606 X_C0.1u16X
C607 X_C1u6.3X-RH
C95 X_C1000p10X0402-RH
C97 C0.1u16Y0402
C98 X_C10u10Y0805
C109 C0.1u16Y0402
V_FSB_VTT
C99 C0.1u16Y0402
C96 X_C0.1u16Y0402
L10 1u500mA_0805-RH
L11 10u100mA_0805-RH
R112 1R1%0402
R113 0R0402
V_1P5_CORE
C103 C0.01u25X0402
C101 C10u10Y0805
C102 C0.1u16Y0402
C100 C0.01u25X0402
V_1P05_CORE
C104 X_C0.1u16Y0402
C106 C0.01u25X0402
C110 C0.1u16Y0402
C107 X_C10u10Y0805
5VSB
C111 C0.1u16Y0402
3VSB
C112 C0.1u16Y0402
C113 X_C0.1u16Y0402
C114 X_C1000p10X0402-RH
V_1P5_CORE
C115 X_C10u10Y0805
C118 C0.1u16Y0402
C119 X_C0.1u16Y0402
C805 X_C1u6.3X-RH
C117 C10u10Y0805
C120 X_C0.1u10X0402
[INTEL-NH82801GB-A1-LF]
MICRO-STAR INT'L CO.,LTD
MS-7507
Size Custom
Document Description Intel ICH7 - POWER
Rev 0A
Date: Wednesday, October 17, 2007
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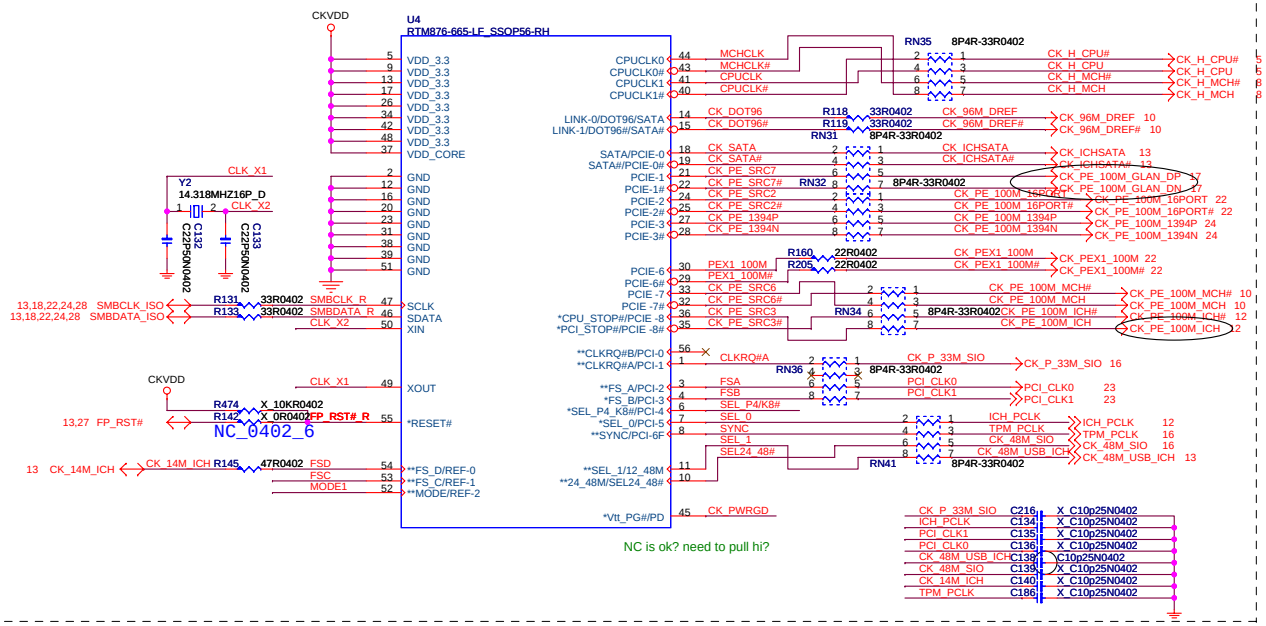
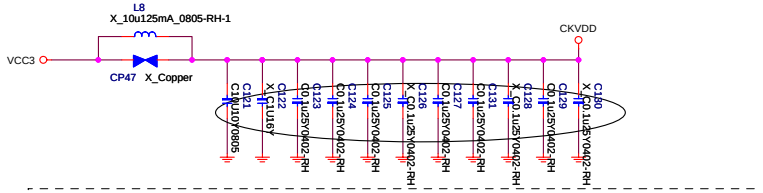
Clock Generator - RTM876-665





STRAPPING RESISTOR

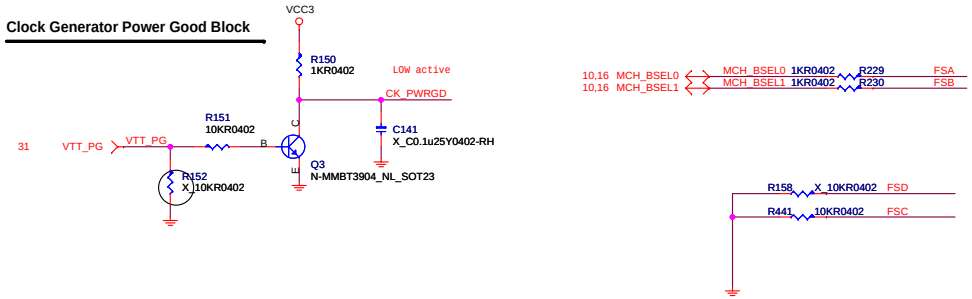
SEL_1	SEL_0	Chipset Support
0	0	SIS
1	0	VIA
0	1	Intel W/GFX
1	1	Intel

SEL_P4/K8#	PIN#40,41,43,44
0	K8 3.3V swing
1	P4 0.8V swing

MODE	PIN#35/36
0	PCIE-8 T/C
1	PCI_STOP#/CPU_STOP#

SEL24_48#	Pin#10
0	48Mhz
1	24Mhz

Clock Generator Power Good Block



CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid

MICRO-STAR INT'L CO.,LTD			
MS-7507			
Size: Custom	Document Description: CLK-RTM 876-660		Rev: 0A
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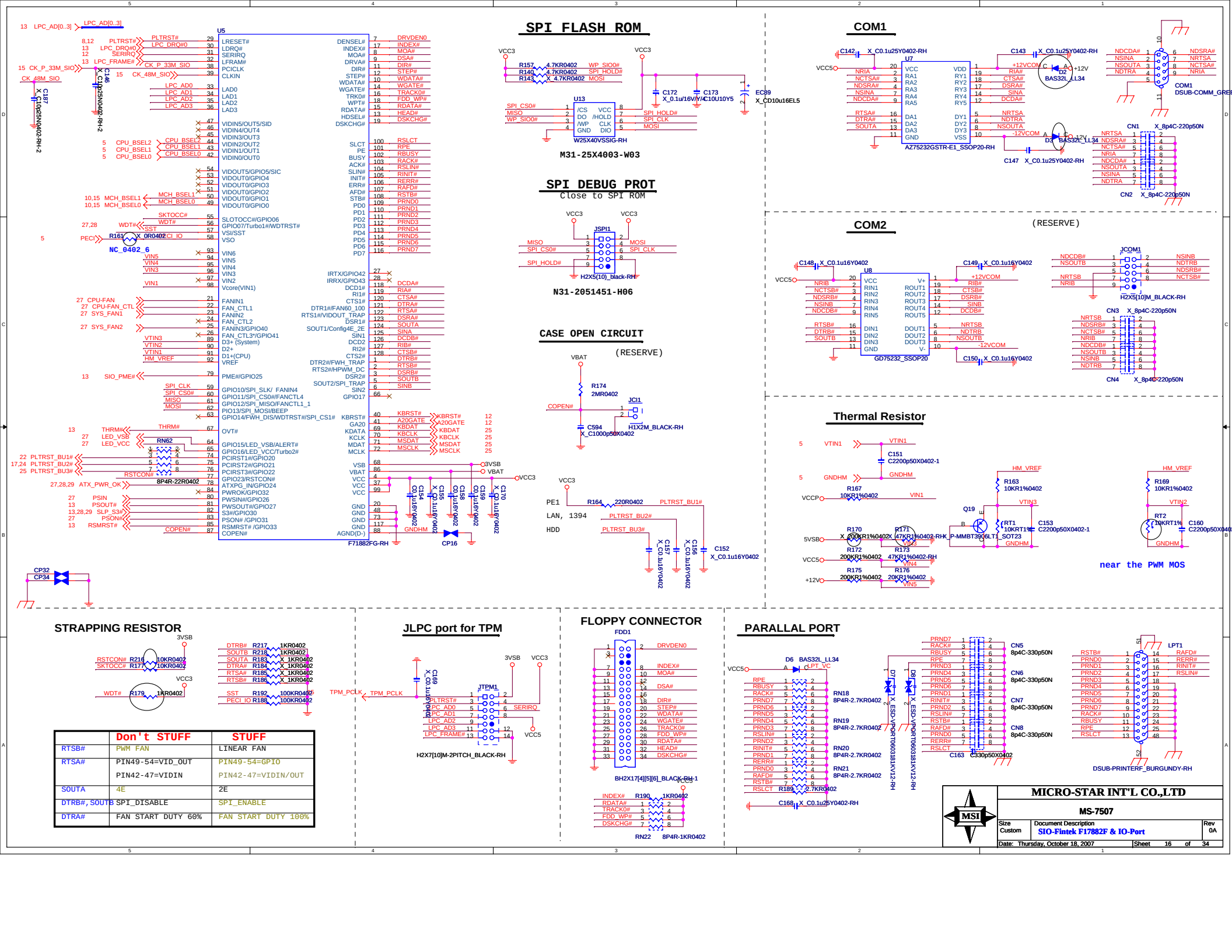
SPI FLASH ROM
M31-25X4003-W03
SPI DEBUG PROT
Close to SPI ROM
N31-2051451-H06
CASE OPEN CIRCUIT
(RESERVE)
COM1
COM2
(RESERVE)
Thermal Resistor
near the PWM MOS
STRAPPING RESISTOR
JLPC port for TPM
FLOPPY CONNECTOR
PARALLAL PORT
Don't STUFF
STUFF
RTSB#
PWM FAN
LINEAR FAN
RTSA#
PIN49-54=VID_OUT
PIN42-47=VIDIN
PIN49-54=GPIO
PIN42-47=VIDIN/OUT
SOUTA
4E
2E
DTRB#, SOUTB
SPI_DISABLE
SPI_ENABLE
DTRA#
FAN START DUTY 60%
FAN START DUTY 100%
MICRO-STAR INT'L CO.,LTD
MS-7507
Size
Custom
Document Description
SIO-Fintek F71882F & IO-Port
Rev
0A
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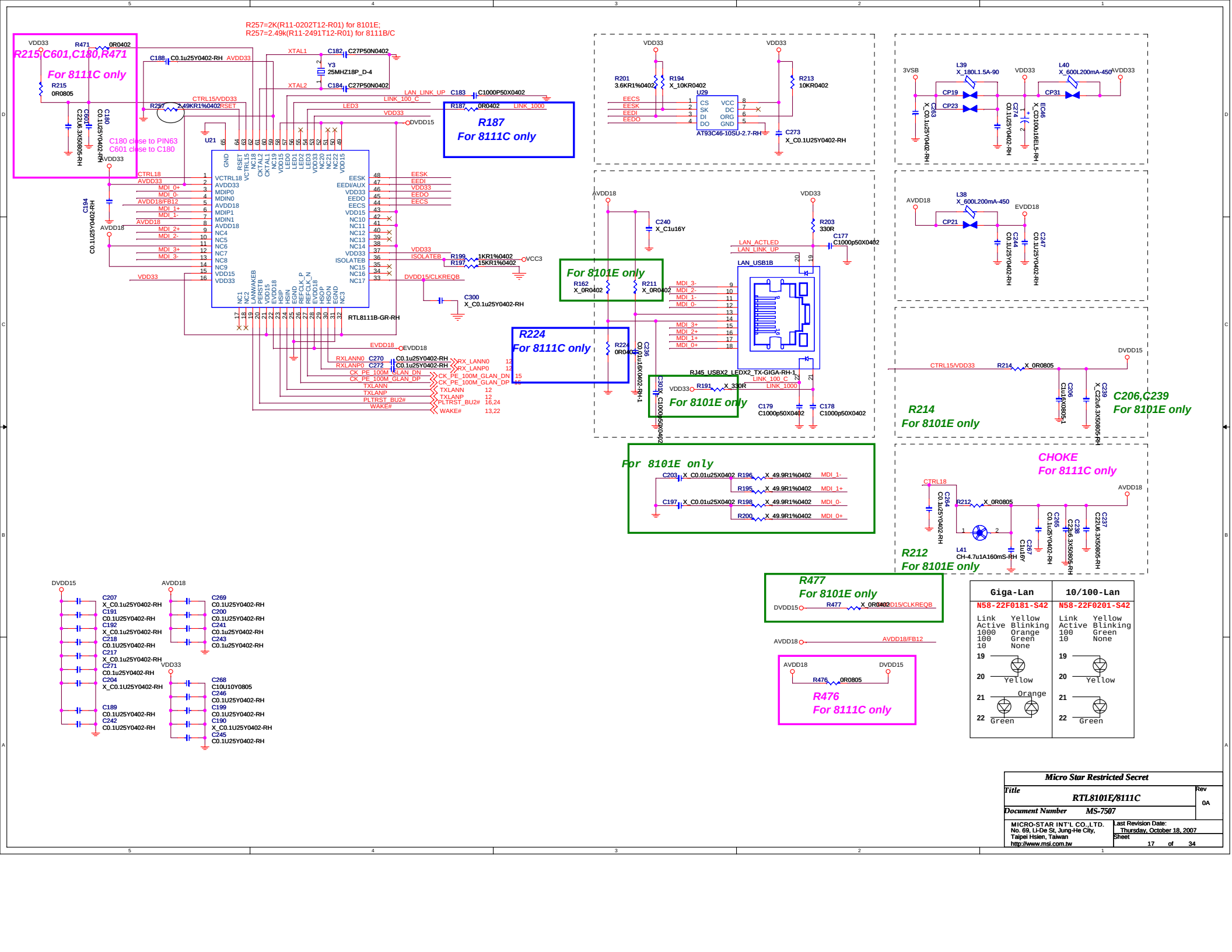
R257=2K(R11-0202T12-R01) for 8101E;
R257=2.49k(R11-2491T12-R01) for 8111B/C
R215,C601,C180,R471
For 8111C only
C180 close to PIN63
C601 close to C180
R187
For 8111C only
R224
For 8111C only
For 8101E only
For 8101E only
For 8101E only
For 8101E only
C206,C239
For 8101E only
R214
For 8101E only
CHOKE
For 8111C only
R212
For 8101E only
R477
For 8101E only
R476
For 8111C only
RTL8111B-GR-RH
AT93C46-10SU-2.7-RH
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
Giga-Lan
N58-22F0181-S42
Link Yellow
Active Blinking
1000 Orange
100 Green
10 None
10/100-Lan
N58-22F0201-S42
Link Yellow
Active Blinking
100 Green
10 None
Micro Star Restricted Secret
Title
RTL8101E/8111C
Rev
0A
Document Number
MS-7507
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Thursday, October 18, 2007
Sheet
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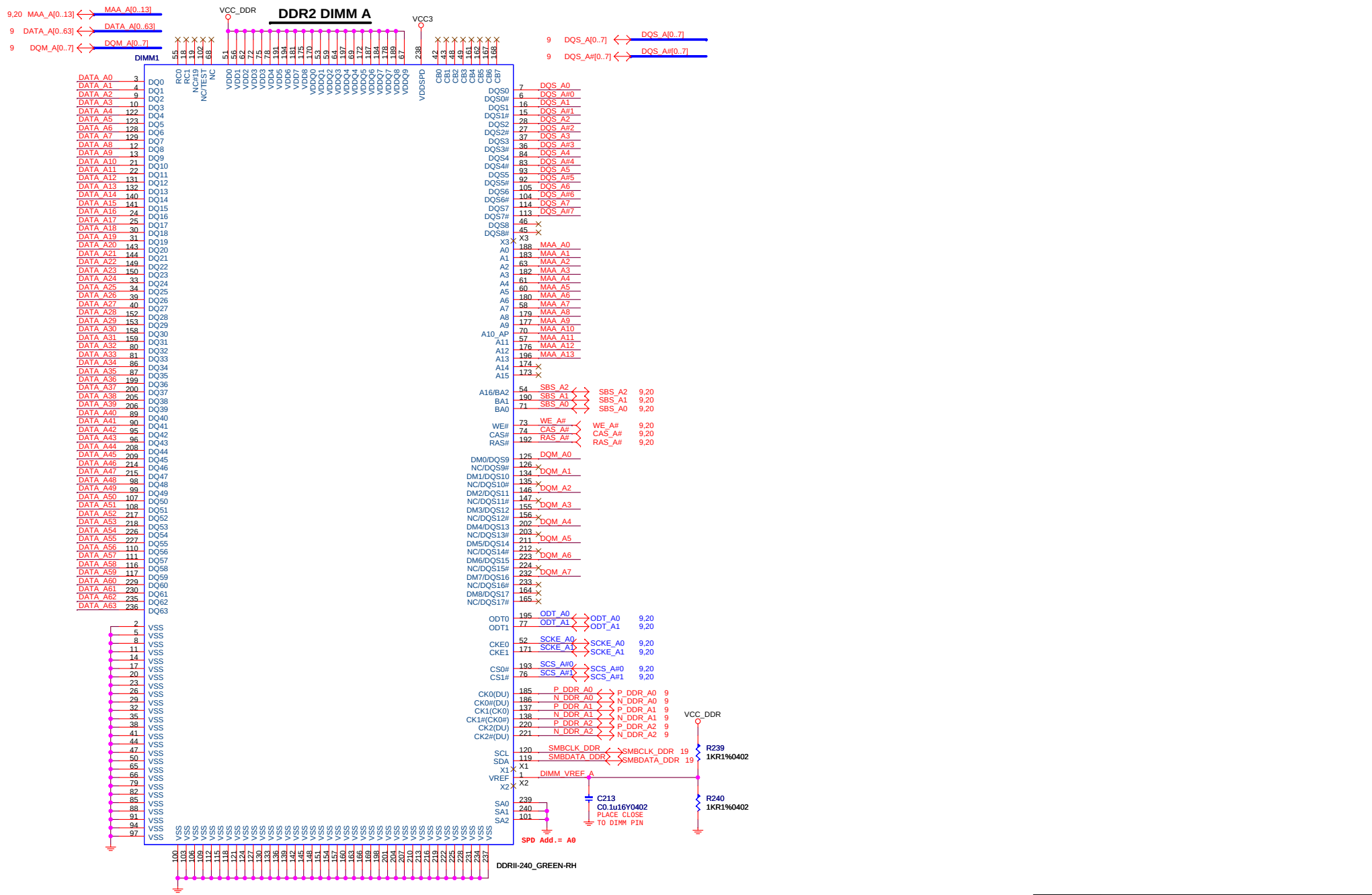

MICRO-STAR INT'L CO.,LTD	
MS-7507	
Size: Custom	Document Description: DDR II DIMM A & B
Rev: 0A	
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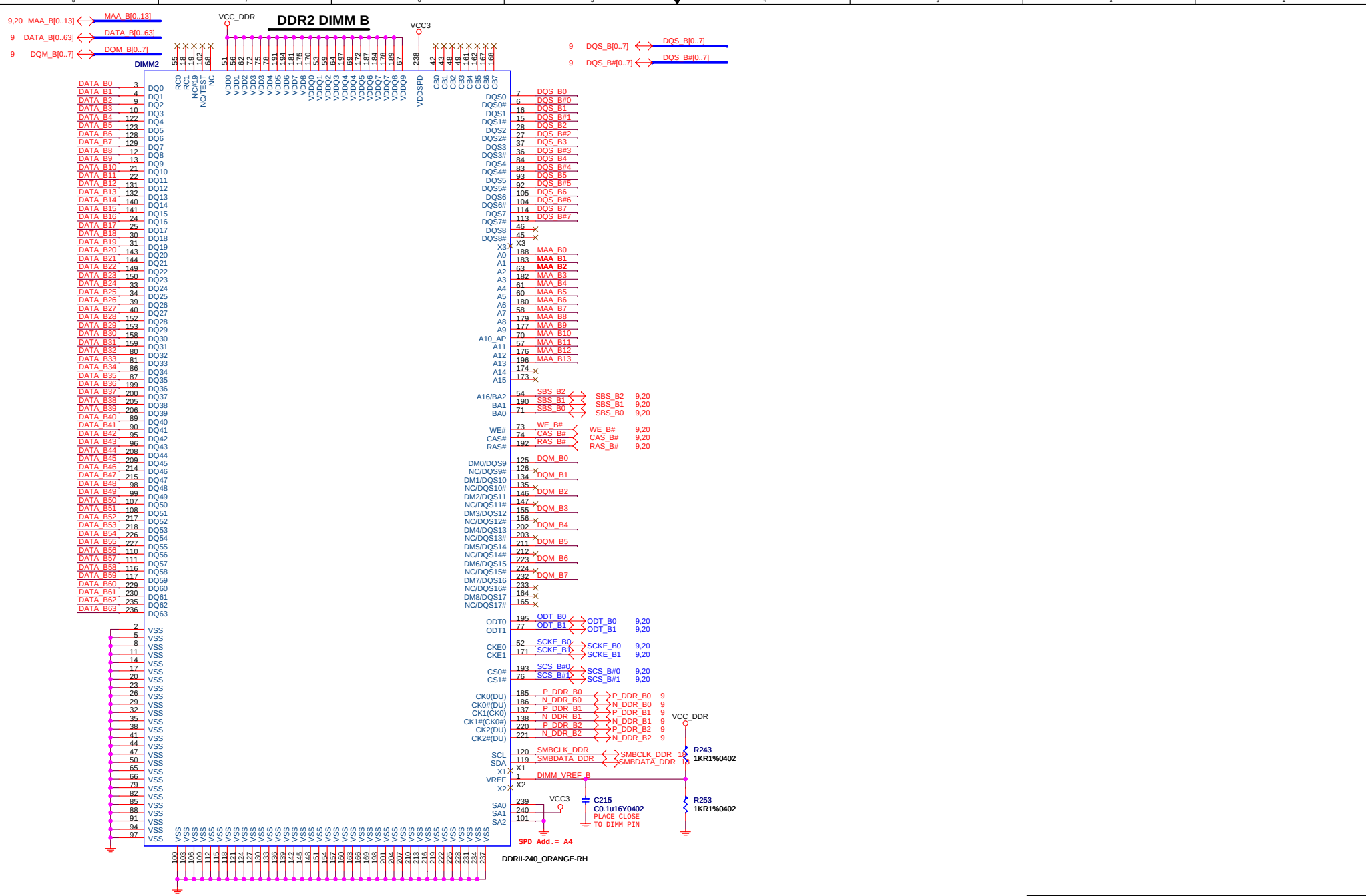

MICRO-STAR INT'L CO.,LTD	
MS-7507	
Size: Custom	Document Description: DDR II DIMM A & B
Rev: 0A	
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CHANNEL A V_SM_VTT DECOUPLING CAPS

VTT_DDR

C224 C4.7u6.3X5
C226 X_C4.7u6.3X5

VTT_DDR

C229 C0.1u16Y0402
C231 C0.1u16Y0402
C233 X_C0.1u16Y0402
C234 X_C0.1u16Y0402

CHANNEL B V_SM_VTT DECOULPING CAPS

VTT_DDR

C220 X_C4.7u6.3X5
C222 C4.7u6.3X5

VTT_DDR

C223 X_C0.1u16Y0402
C225 X_C0.1u16Y0402
C227 X_C0.1u16Y0402
C228 C0.1u16Y0402

VTT_DDR

RN23 8P4R-33R0402
MAA_A4
MAA_A3
MAA_A2
MAA_A1
MAA_A9
RN25 8P4R-33R0402
MAA_A5
MAA_A8
MAA_A6
SBS_A2
RN27 8P4R-33R0402
MAA_A12
MAA_A11
MAA_A7
RAS_A# 9,18
WE_A# 9,18
CAS_A# 9,18
RN46 8P4R-33R0402
MAA_A13
RN47 8P4R-33R0402
MAA_A0
MAA_A10
SBS_A0
SBS_A1
RN60 8P4R-43R0402
ODT_A1
SCS_A#1
ODT_A0
SCS_A#0
change RN
SCKE_A0 R227 43R0402
SCKE_A1 R228 43R0402

9,18 MAA_A[0..13]
9,18 SBS_A[0..2]
9,18 SCS_A#[0..1]
9,18 SCKE_A[0..1]
9,18 ODT_A[0..1]

VTT_DDR

RN24 8P4R-33R0402
MAA_B4
MAA_B3
MAA_B2
MAA_B1
SBS_B2
RN26 8P4R-33R0402
MAA_B12
MAA_B11
MAA_B7
MAA_B9
RN28 8P4R-33R0402
MAA_B5
MAA_B8
MAA_B6
WE_B# 9,19
RAS_B# 9,19
CAS_B# 9,19
RN29 8P4R-33R0402
MAA_B13
RN30 8P4R-33R0402
MAA_B10
MAA_B0
SBS_B0
SBS_B1
RN61 8P4R-43R0402
ODT_B1
SCS_B#1
ODT_B0
SCS_B#0
change RN
SCKE_B0 R231 43R0402
SCKE_B1 R232 43R0402

9,19 MAA_B[0..13]
9,19 SBS_B[0..2]
9,19 SCS_B#[0..1]
9,19 SCKE_B[0..1]
9,19 ODT_B[0..1]

VCC_DDR

C248 C1U10Y0402-RH
C249 C1U10Y0402-RH
C250 C1U10Y0402-RH
C251 X_C1U10Y0402-RH
C252 X_C1U10Y0402-RH
C253 C1U10Y0402-RH
C254 C1U10Y0402-RH
C255 X_C1U10Y0402-RH

VCC_DDR

C256 C1U10Y0402-RH
C257 X_C1U10Y0402-RH
C258 X_C1U10Y0402-RH
C259 X_C1U10Y0402-RH
C260 X_C1U10Y0402-RH
C261 C1U10Y0402-RH
C266 X_C1U10Y0402-RH
C262 X_C1U10Y0402-RH

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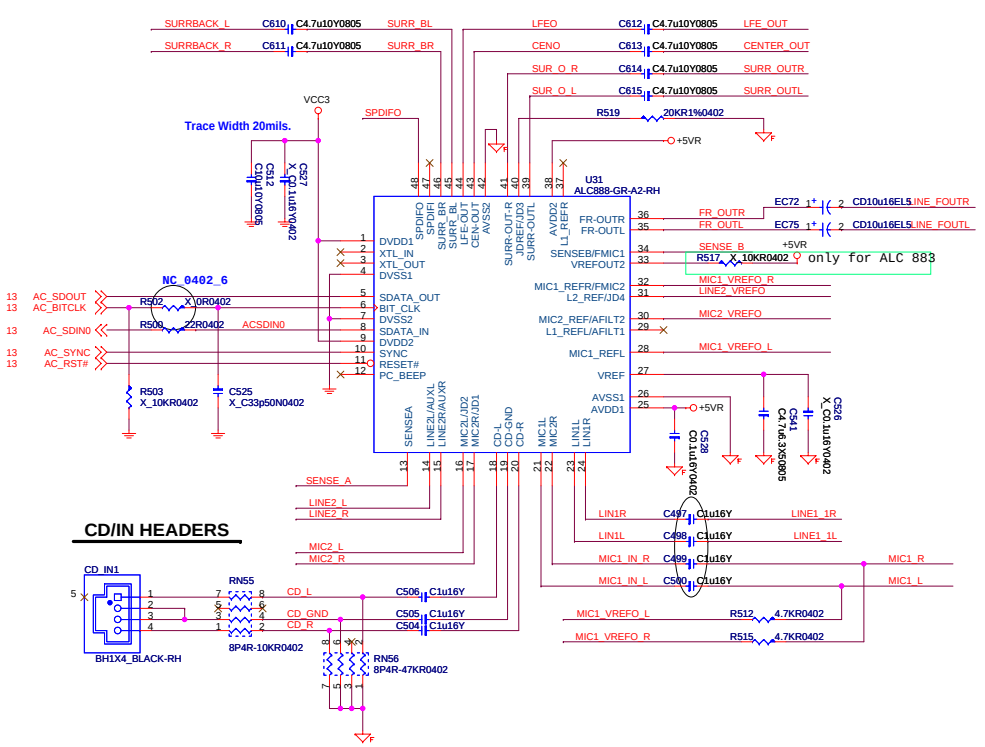
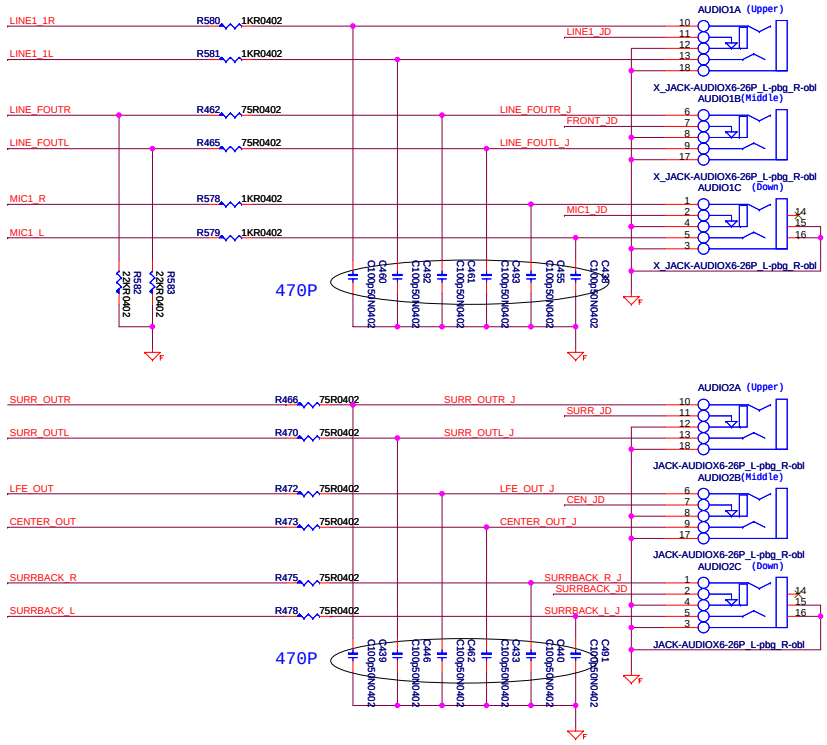
ALC888 CODEC

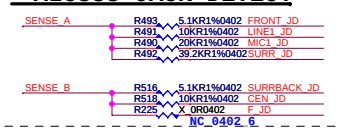


CD/IN HEADERS

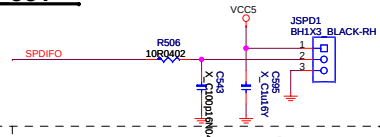
ALC888 JACK



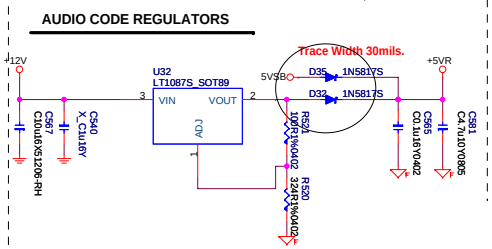
ALC883 JACK DETECT



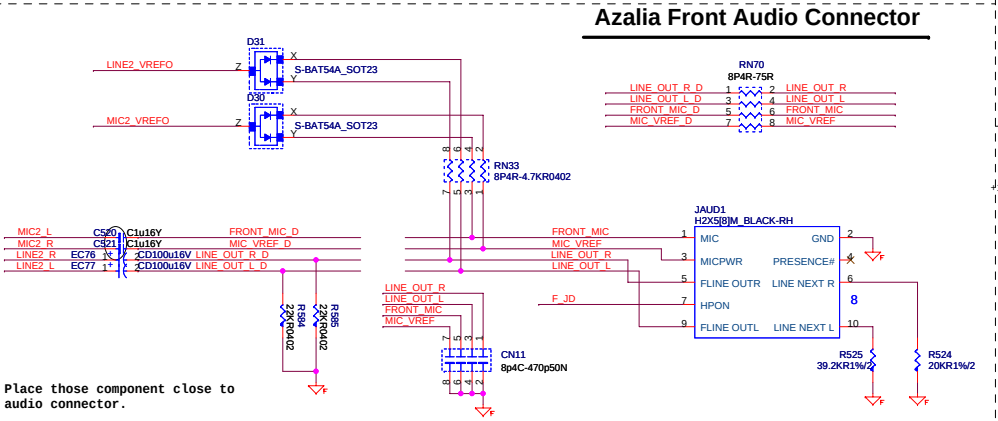
SPDIF OUT



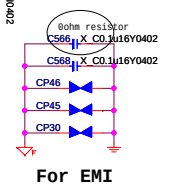
AUDIO CODE REGULATORS



Azalia Front Audio Connector



Place those component close to audio connector.



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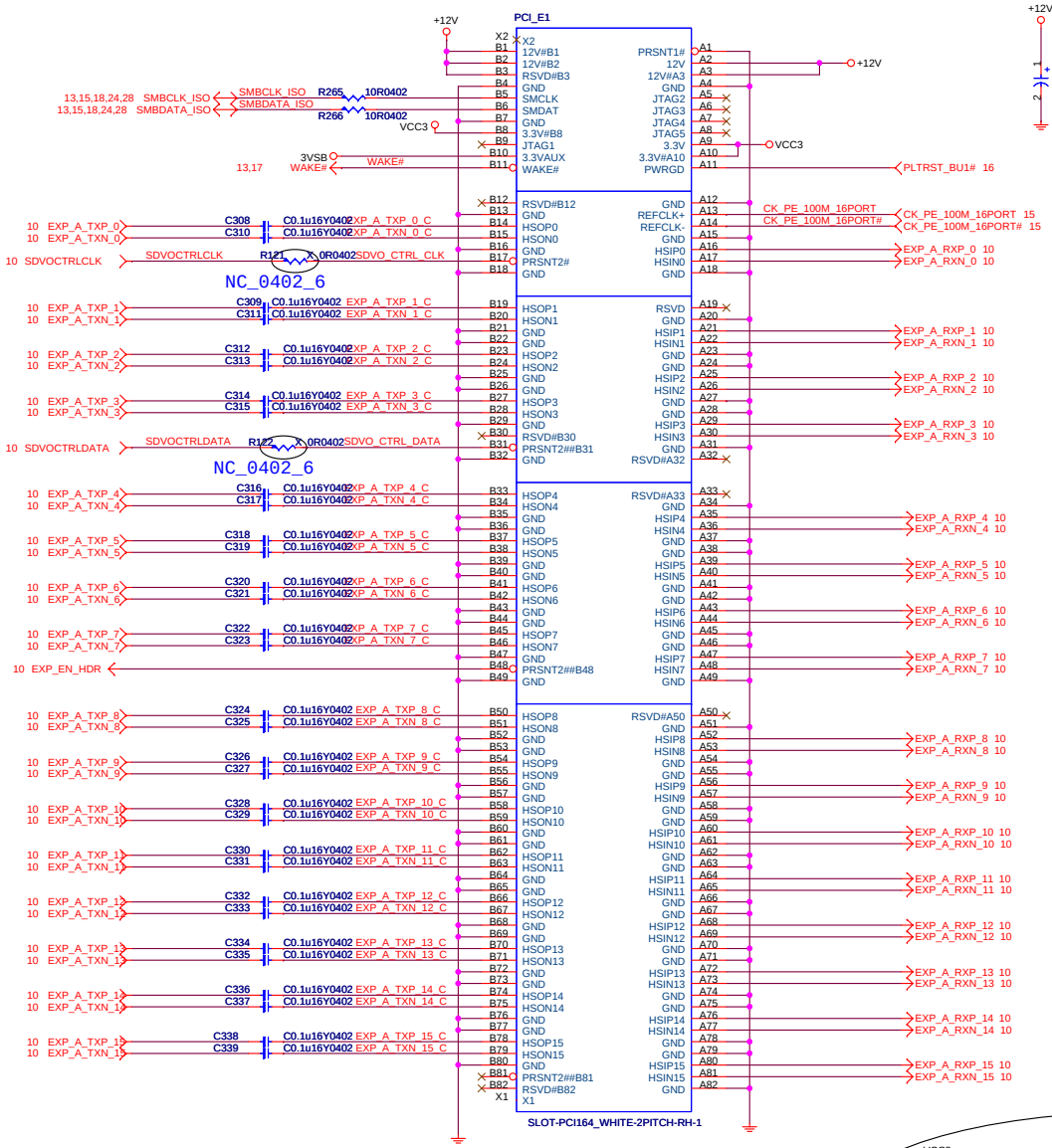
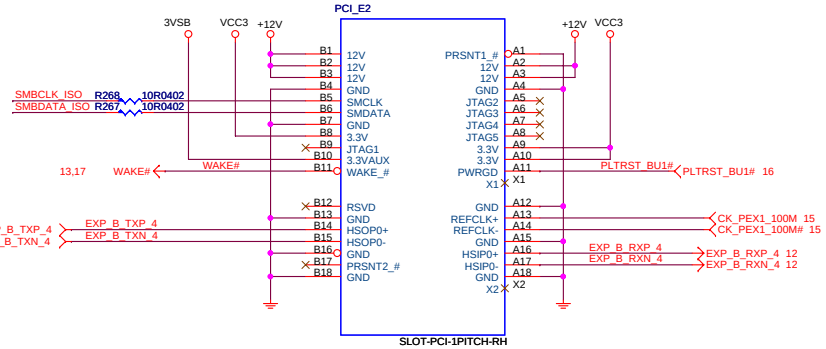
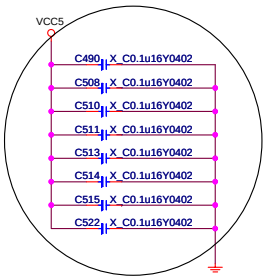
PCIE X16 PORT

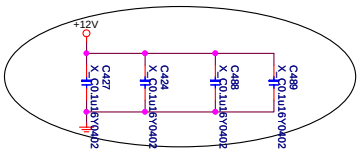


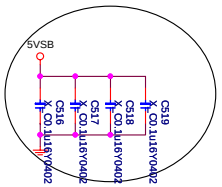
PCIE X1 PORT

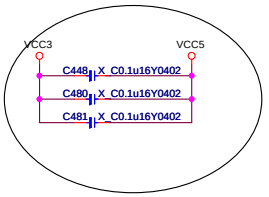


EMI

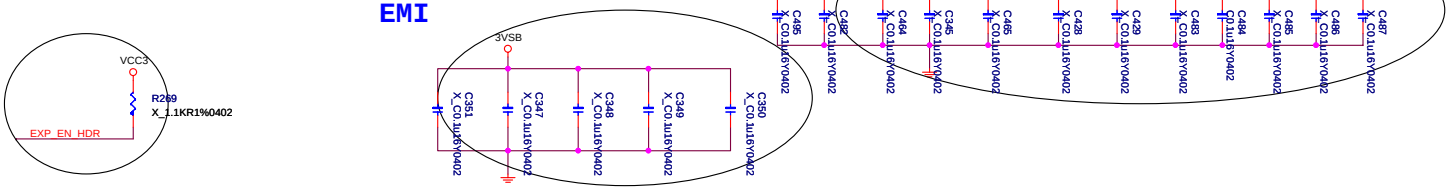








EMI



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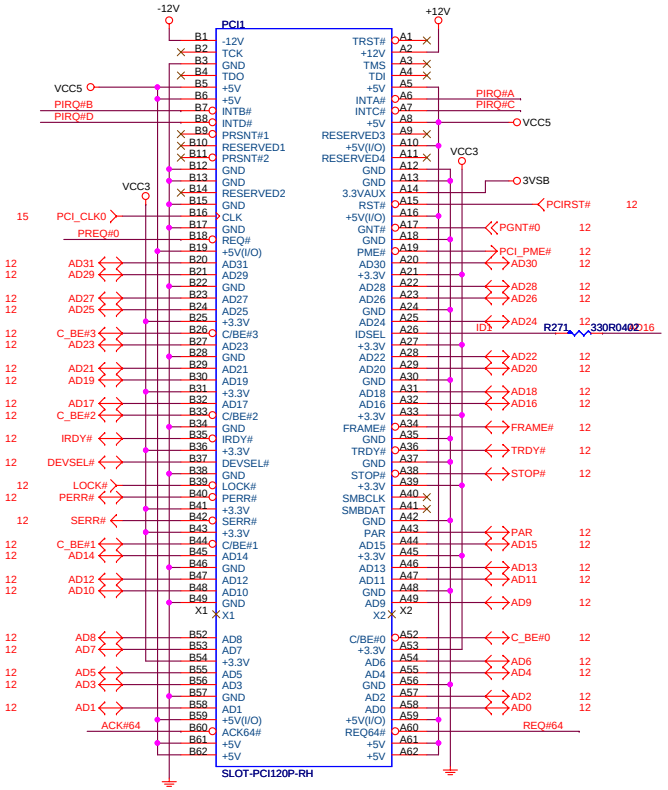
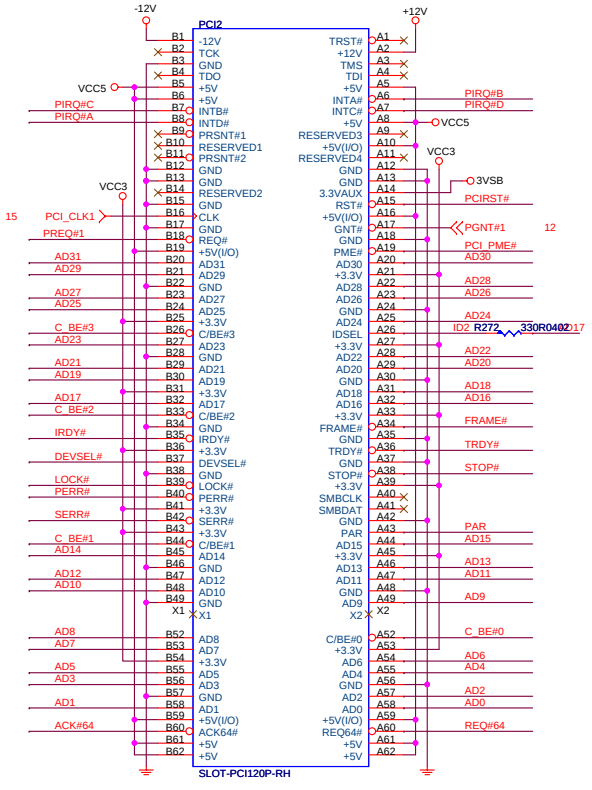
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



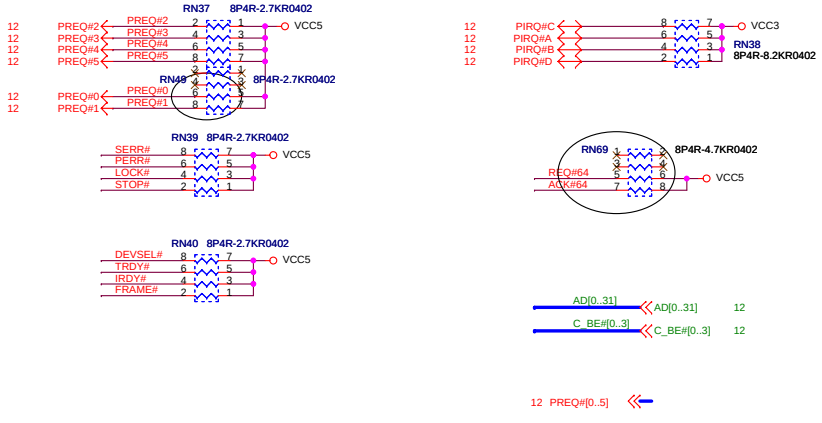
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

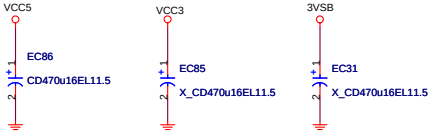
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS





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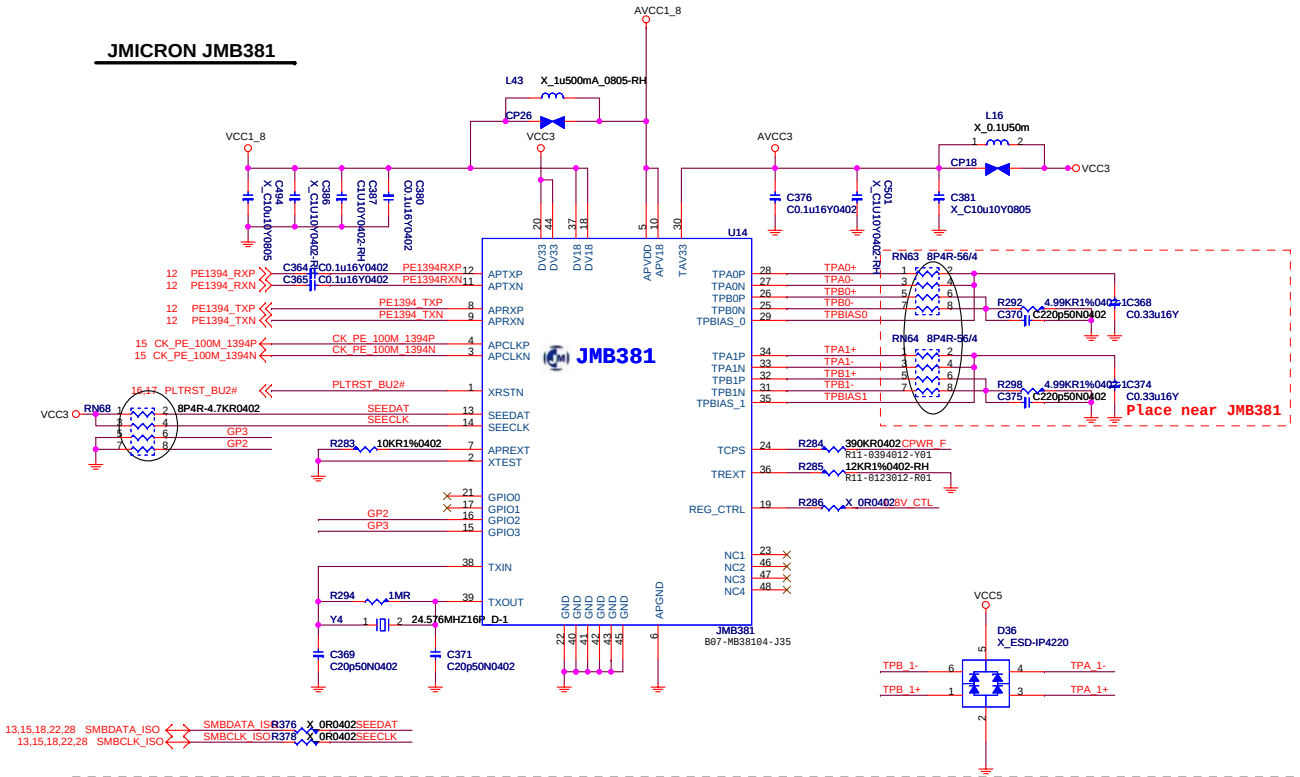
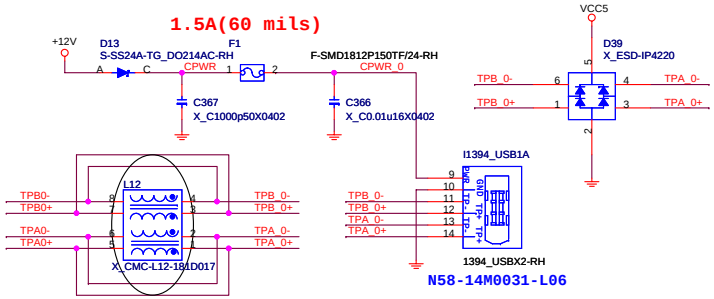
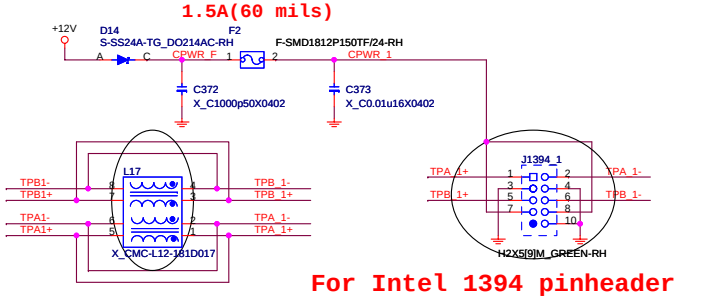
JMICRON JMB381

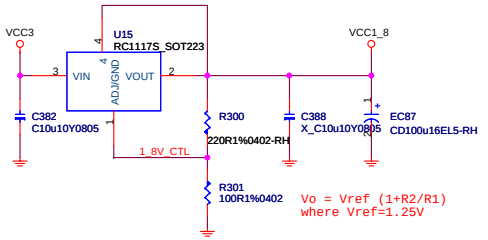


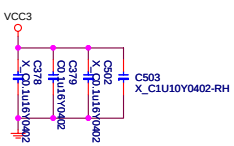
Rear 1394 port

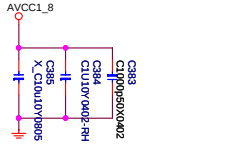


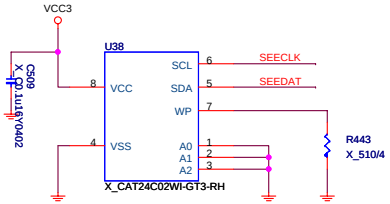
Front 1394 pin header











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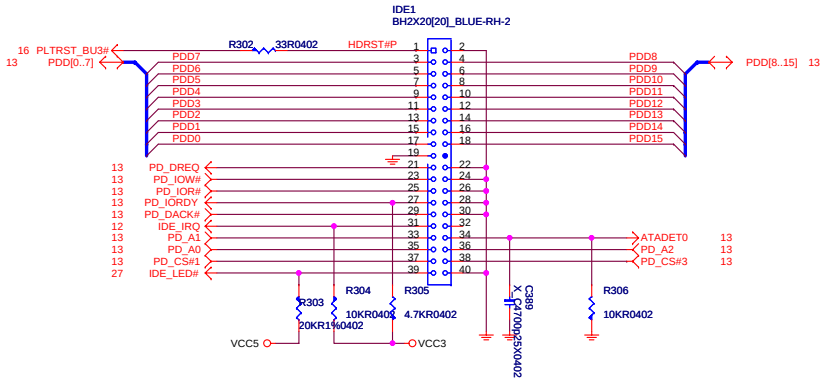
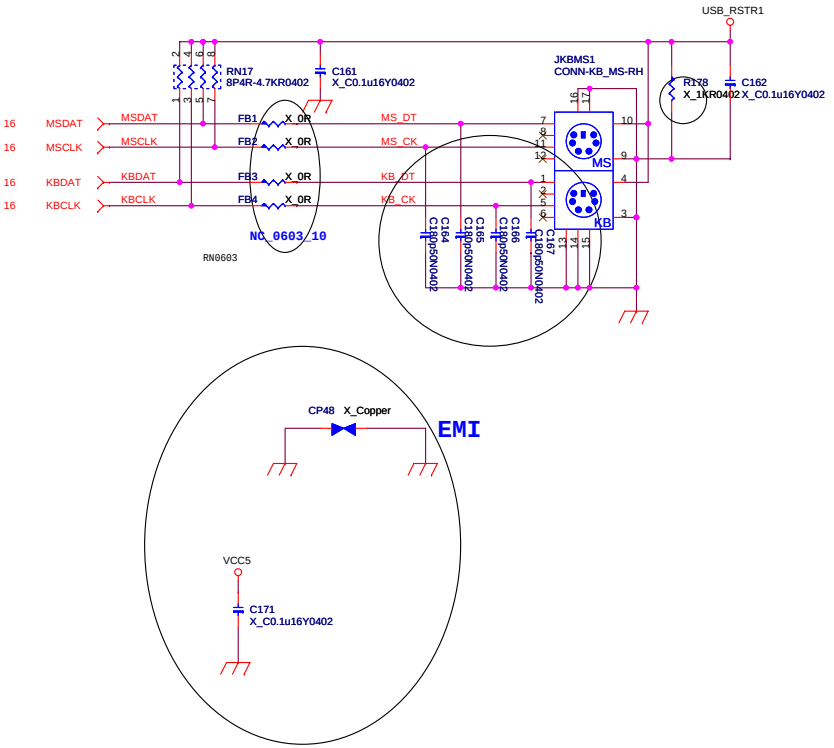
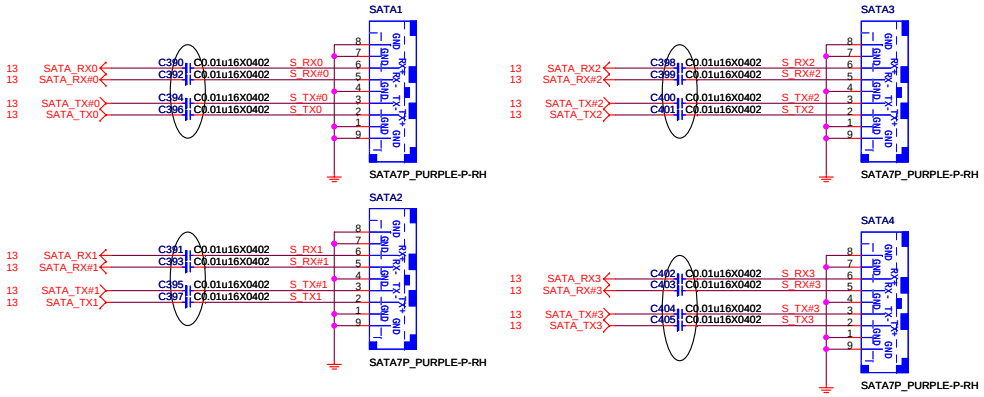
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK



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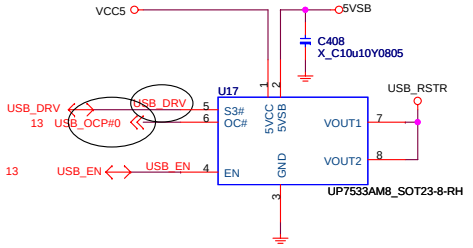
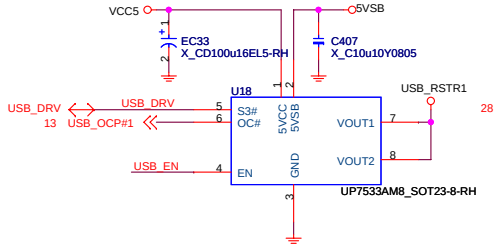
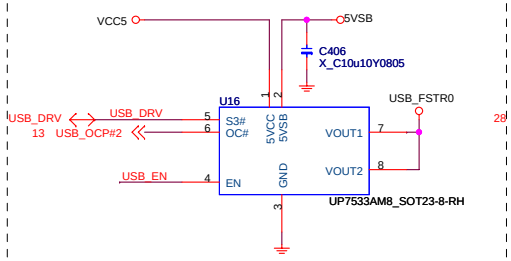
POWER CIRCUIT FOR USB PORT 0,1



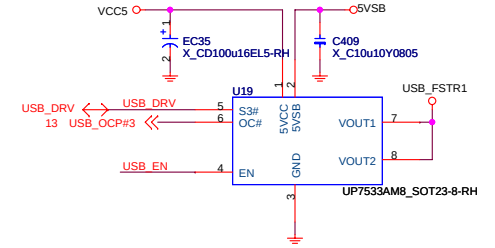
POWER CIRCUIT FOR USB PORT 2,3



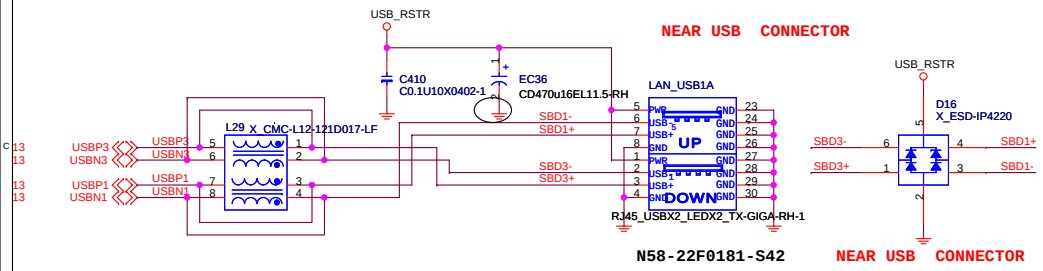
POWER CIRCUIT FOR USB PORT 4,5



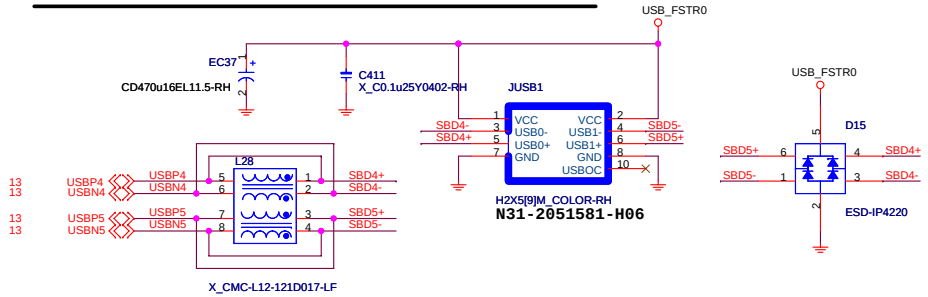
POWER CIRCUIT FOR USB PORT 6,7



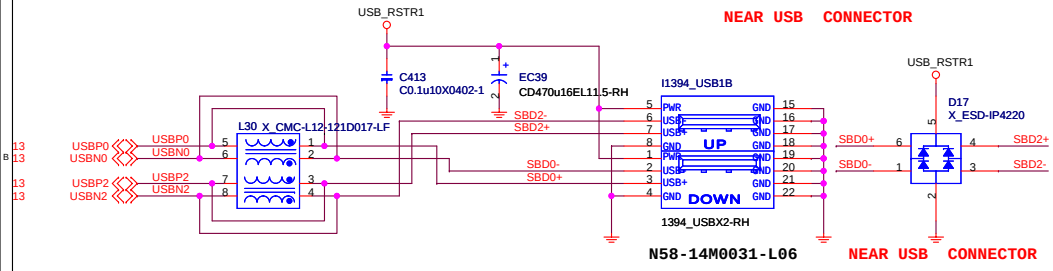
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



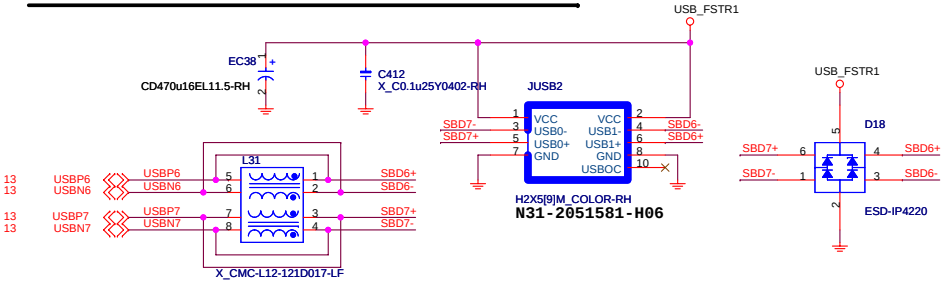
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



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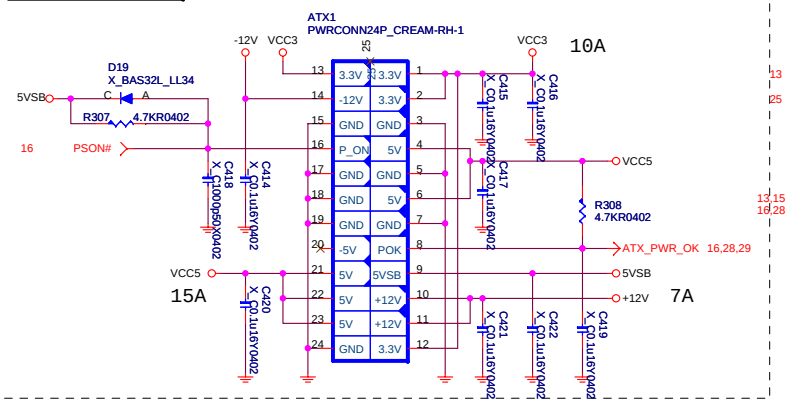
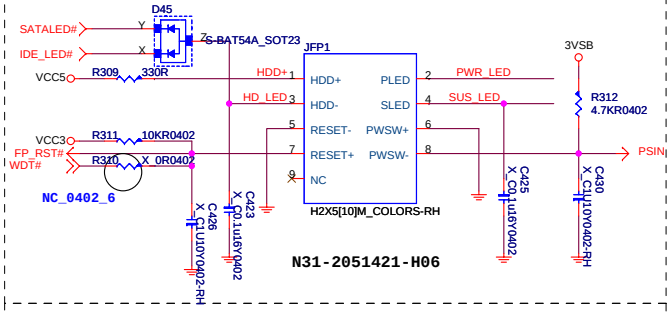
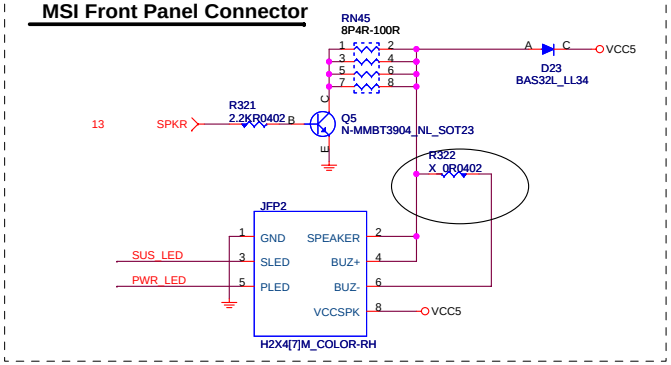
ATX Connector



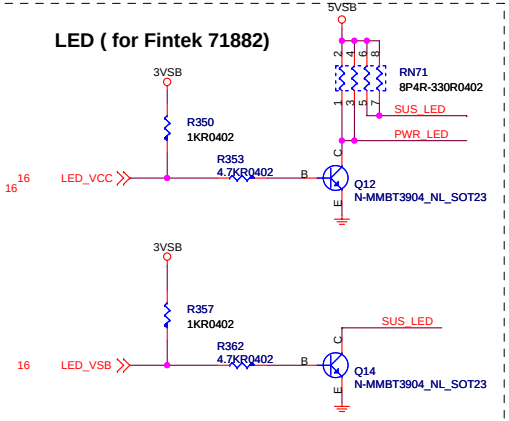
INTEL/PB Front Panel Connector



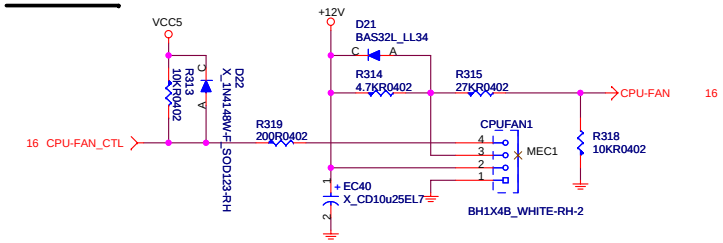
MSI Front Panel Connector



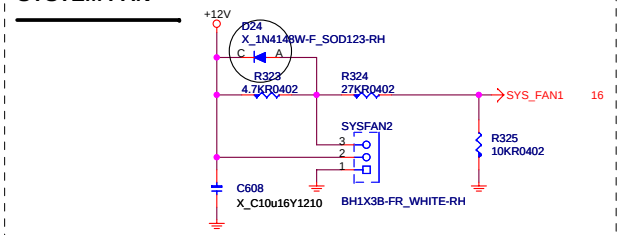
LED (for Fintek 71882)



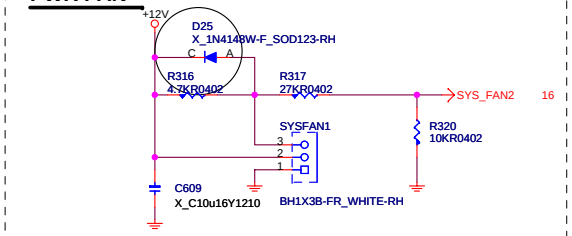
CPU FAN



SYSTEM FAN



PWR FAN



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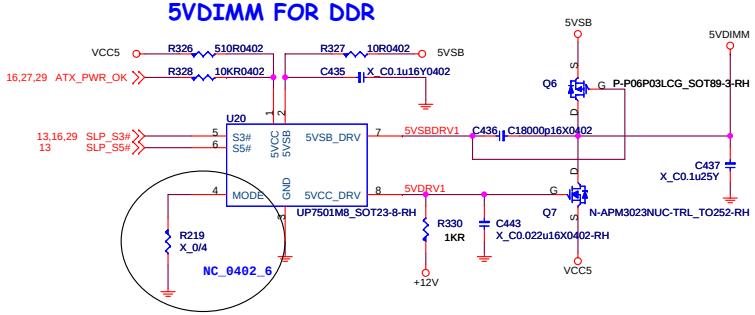
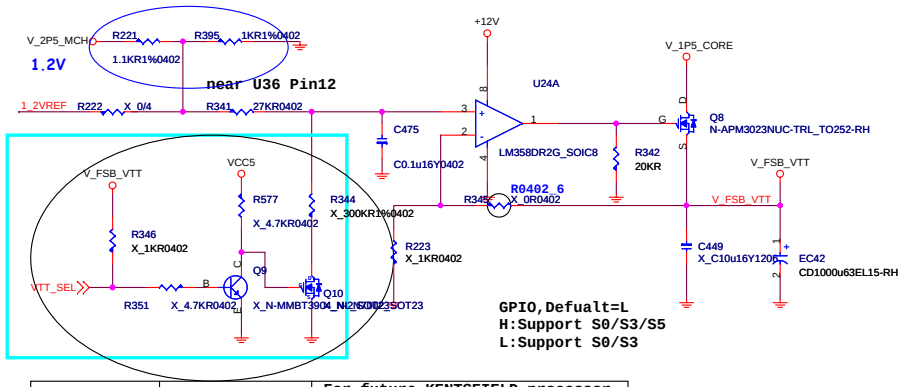
5VDIMM FOR DDR

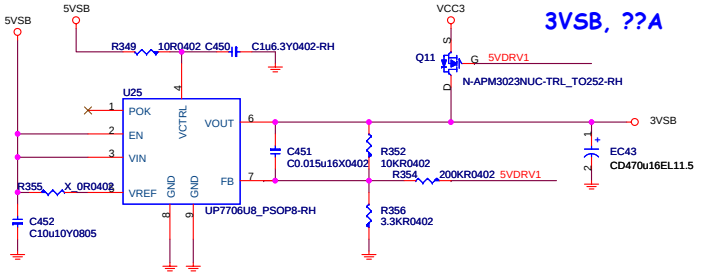


1.2V

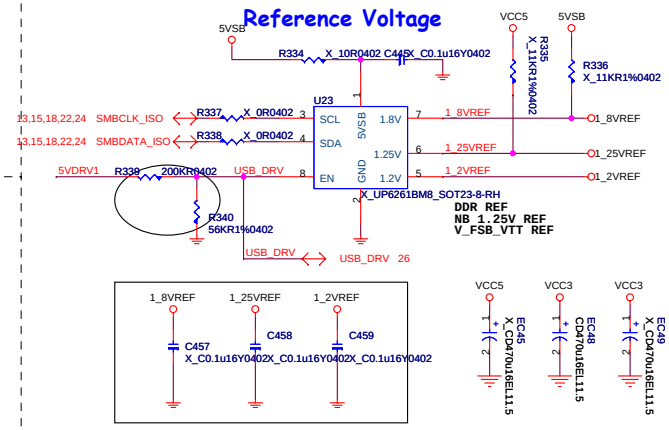


VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

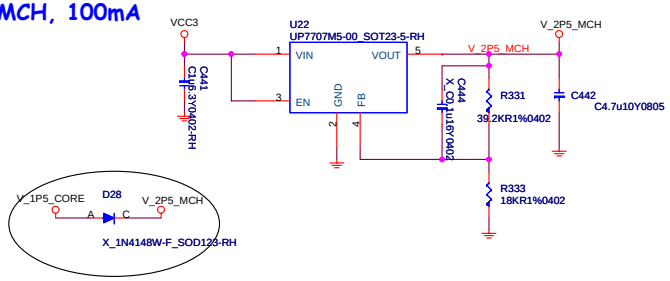
3VSB, ??A



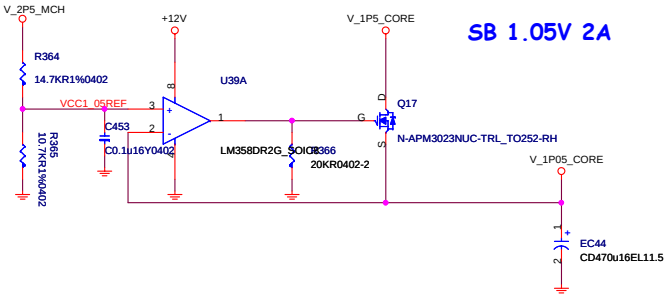
Reference Voltage

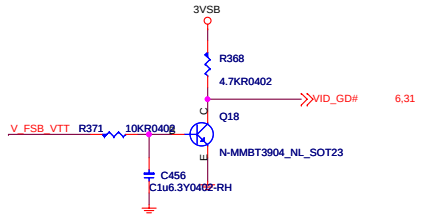


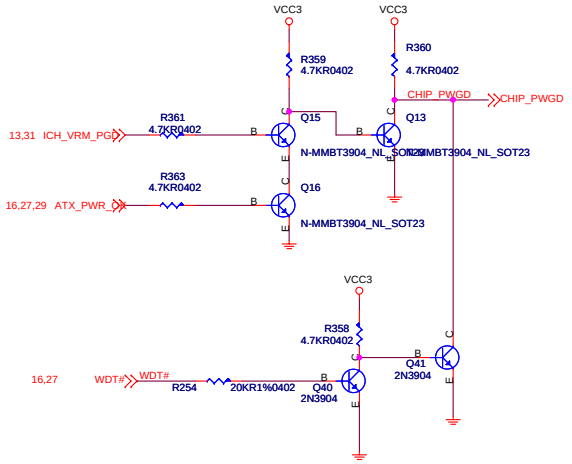
V_2P5_MCH, 100mA



SB 1.05V 2A







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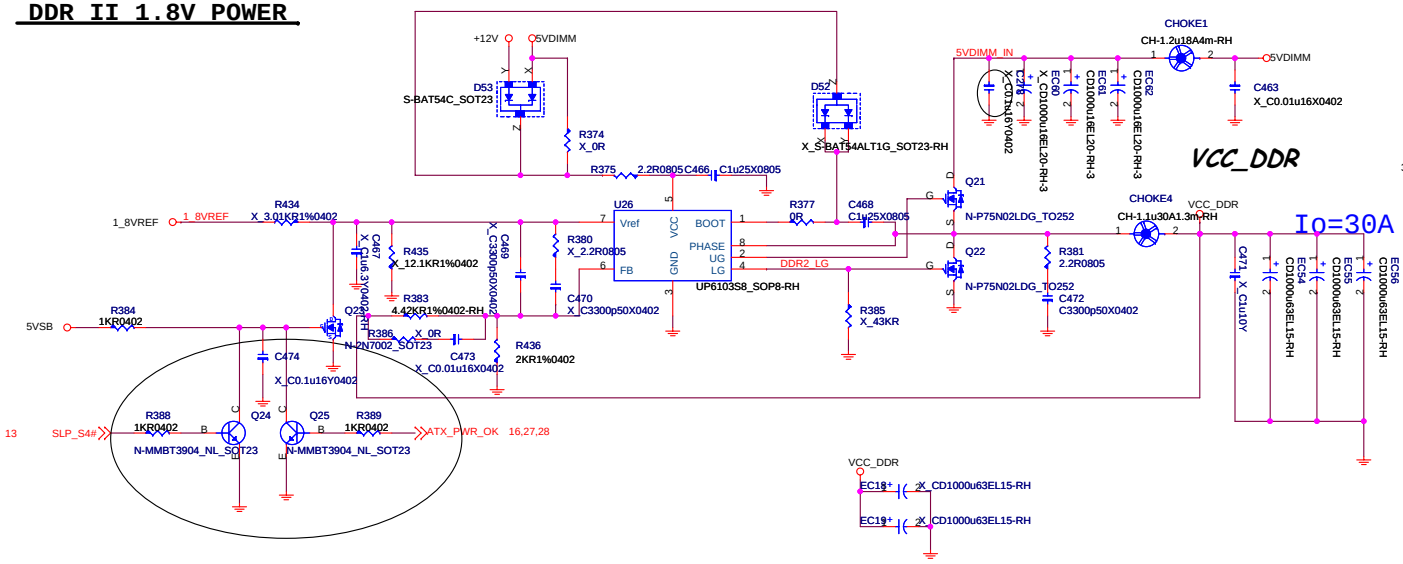
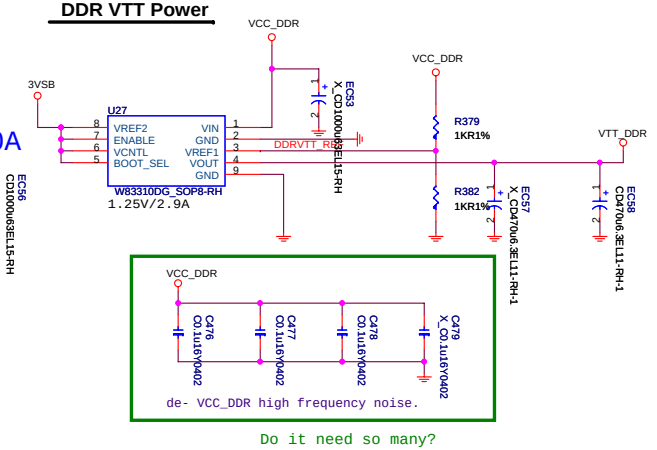
DDR II 1.8V POWER



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

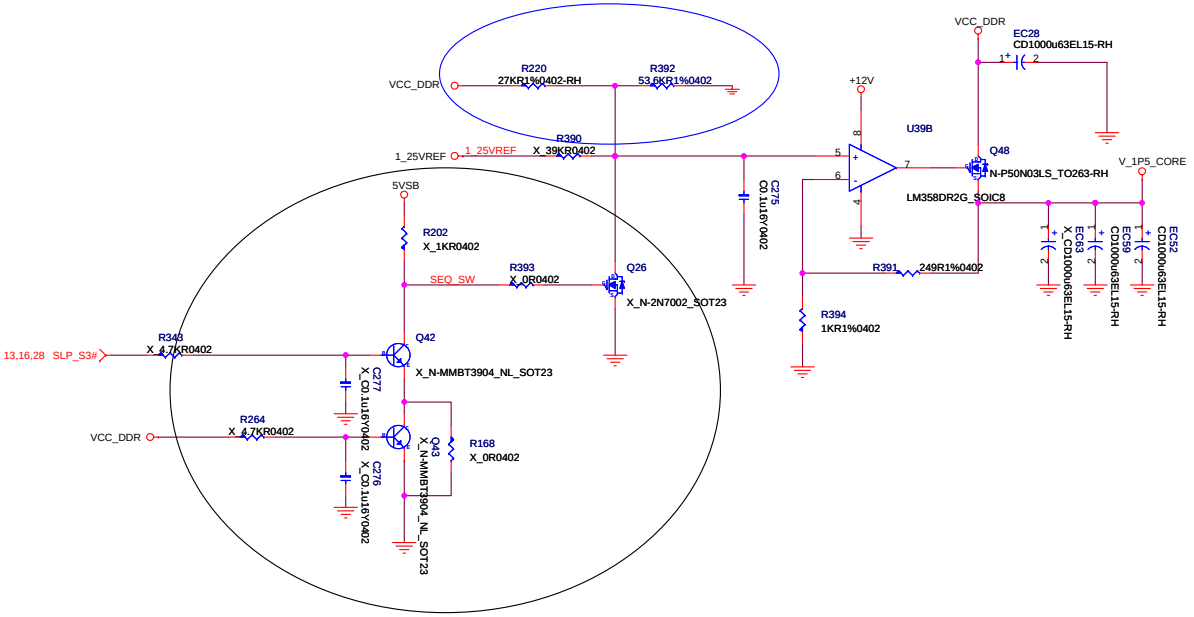
DDR VTT Power



Do it need so many?

1.5V Core

For cost down



Io=22.8A

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7507	
Size: Custom	Document Description: NB Core Power & DDR Power	Rev: 0A
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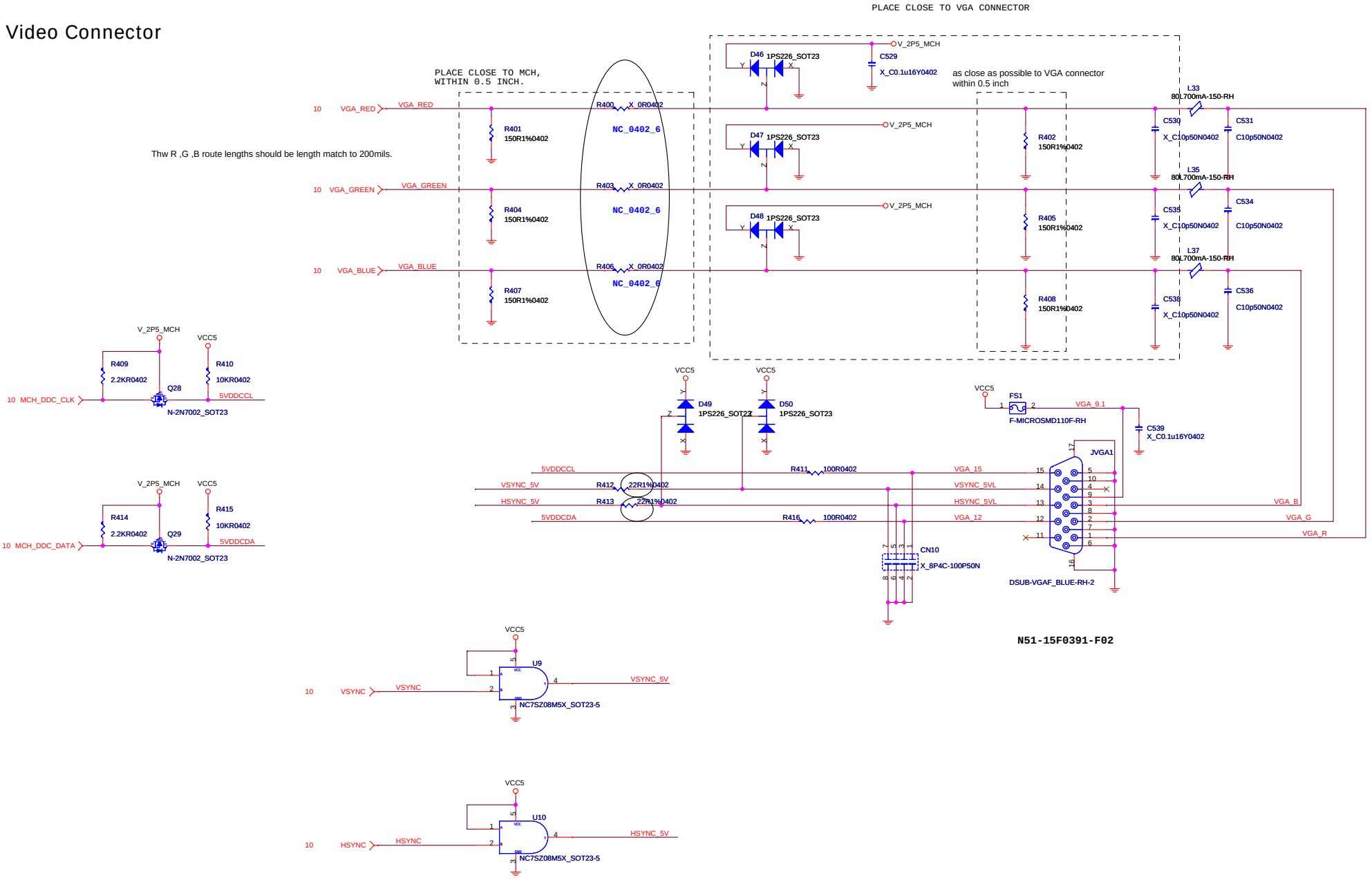
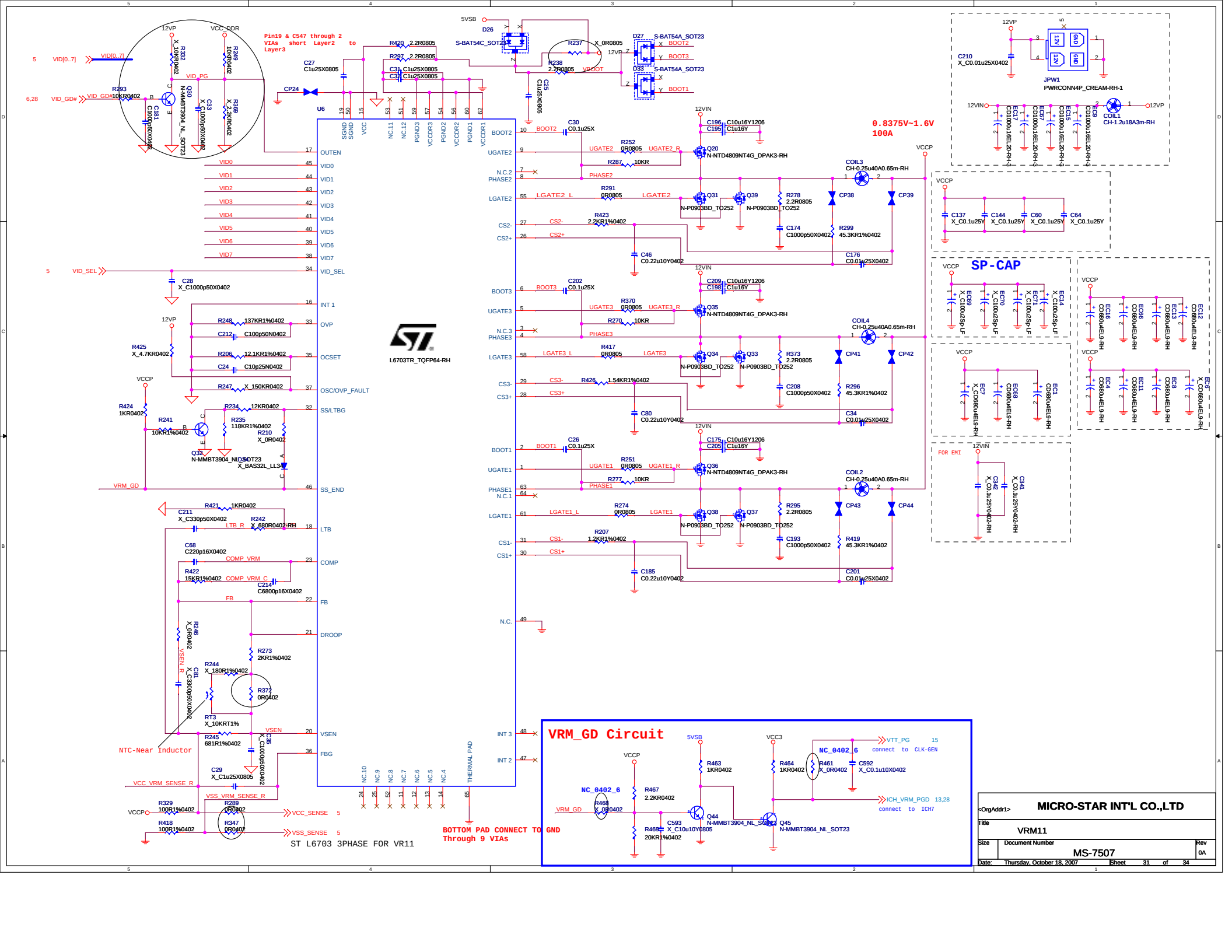
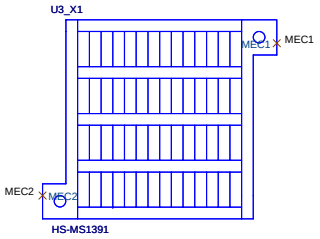
Video Connector



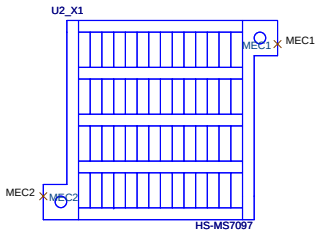
MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: VGA Connector	Rev: 0A
Date: Wednesday, October 17, 2007	Sheet 30 of 34	


Pin19 & C547 through 2 VIAs short Layer2 to Layer3
L6703TR_TQFP64-RH
0.8375V~1.6V 100A
SP-CAP
VRM_GD Circuit
NTC-Near Inductor
BOTTOM PAD CONNECT TO GND Through 9 VIAs
ST L6703 3PHASE FOR VR11
MICRO-STAR INT'L CO.,LTD
VRM11
MS-7507
Thursday, October 18, 2007

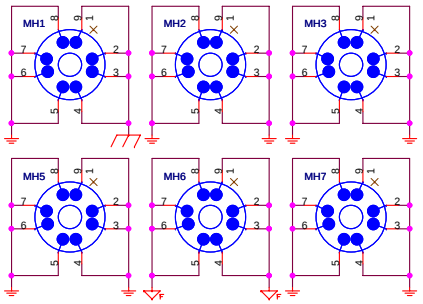
ICH7 HEATSINK



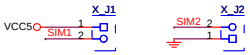
MCH HEATSINK



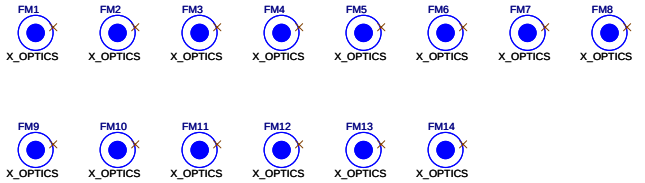
Mounting Holes



Simulation



Optics Orientation Holes



MICRO-STAR INT'L CO.,LTD		
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1.link CIS library
2.change lan whole page circuit
3.move SPI rom and header connector to SB
4.modify SMB on CLKGEN
5.change R363 to 4.7K
6.add SIO_PWROK to circuit
7.SIO 57pin(SST) pull-low use 100K
8.add VCC3 sense on SIO
9.reserve Q19 for VTIN3
10.change com port,KBMS and parallel port ground(GND) to PGND
11.delete Mounting Holes pin4 and pin5 connecting
12.delete two Mounting Holes
13.Change two Mounting Holes ground(GNDF) to AGND
14.change SIO and Chassis intrusion power VBAT0 to VBAT
15.add beep function for SIO
16.Pull-high SIO 77pin to 3VSB
17.modify PSOUT# pull-high to 3VSB
18.reserve R223 for V_FSB_VTT FB
19.Change KB&MS 0ohm series resistor to L
20.delete OC# signal on JUSB1&2
21.reserve C30 for LAN connector
22.Delete DDR2 two DIMMs
23.delete PCI SLOT3
24.fang sir help to adjust 1394 and USB page
25.add PCIE X1 Connector
26.change VRM circuit
27.modify VCC5_SB to 5VSB in VRM page
28.add GND_USB,add coppers connect to GND_VGA and to GND
29.change audio whole page circuit
30.change AGND to GNDF
31.modify 1394 circuit using EMI solution
32.modify diode footprint for layout
33.change CPU footprint
34.add reserved D52,D54 for uPI power solution
35.delete CPU three Address traces
36.add some reserve pull-low resistors at CLKGEN page
37.modify frequence latch circuit
38.modify audio 6 of DIP caps to SMT cap
39.add GPI9 for throttle function
40.modify 1394 circuit
41.modify USB power circuit
42.modify frequence latch circuit
43.remove GPIO24 pull-low/pull-high
44.modify VGA circuit follow EMI solution
45.delete 2.5V control circuit
46.change 1.5V_Core ragulator
47.change front audio detect mode
48.Change ACPI circuit for cost down

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ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPI0(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OOD12t	
GPIO6	SLOTOCC#	55	GPO	I/OOD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OOD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OOD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OOD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OOD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OOD12t	

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JCI1	*Chassis Intrusion*
Open	Normal
(1-2)	Chassis Open

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

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