P53 N19E Schematic Page Number

Nighthawk - 14L

Project Code: FP530
14L NM-C261 Rev : 1.0
NV N19E-Qx

Project Name	*Nighthawk-1*	
Rev 1.0	Title	TITLE PAGE
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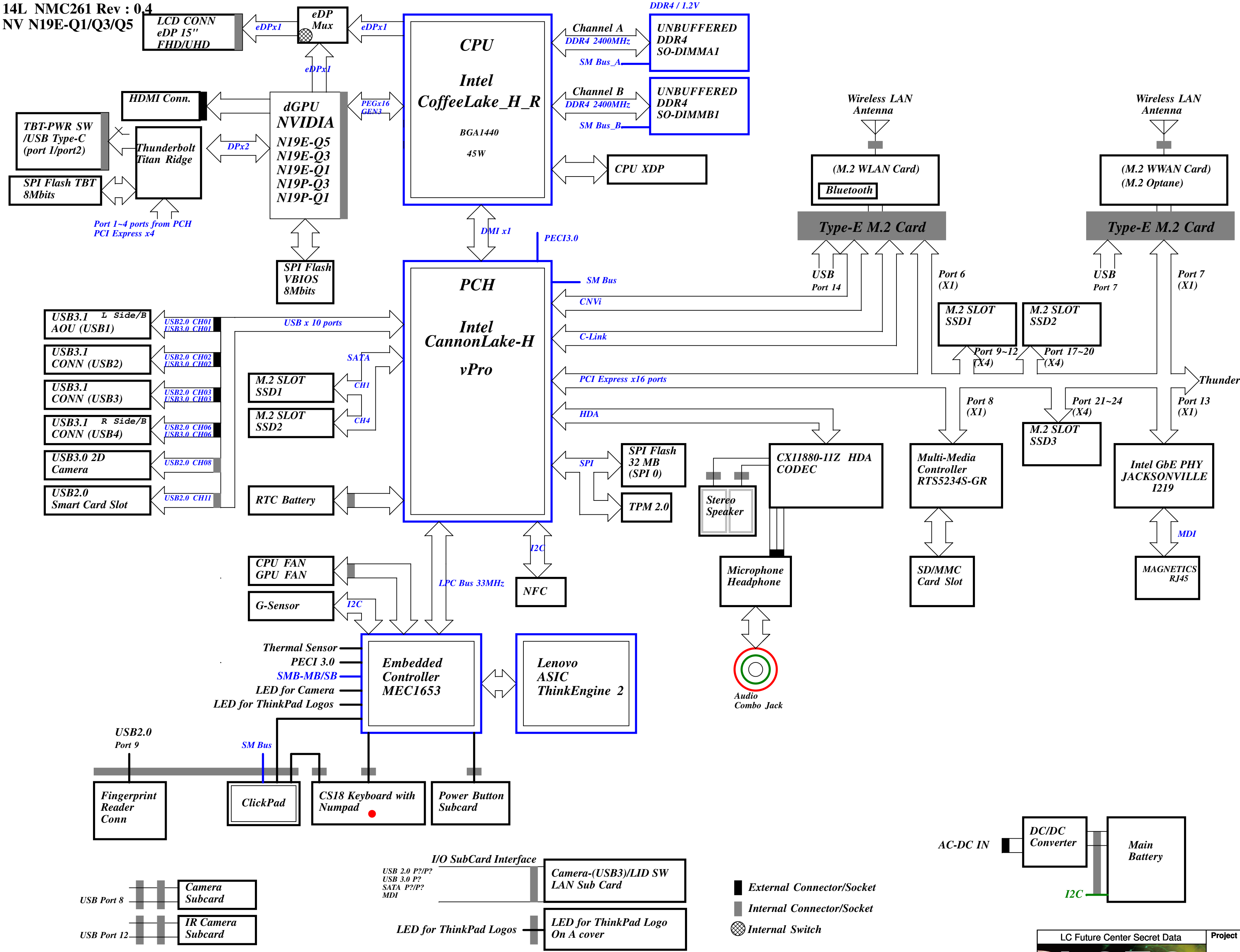
Nighthawk - Block Diagram

Project Code: FP530

14L NMC261 Rev : 0.4

NV N19E-Q1/Q3/Q5



PCB Layer Stackup

- L1:TOP
- L2:GND1
- L3:Signal 1
- L4:GND 2
- L5:Signal 2
- L6:GND3
- L7:VCC1
- L8:Signal 3
- L9:VCC2
- L10:Signal 4
- L11:GND4
- L12:BOTTOM

Battery Charger

BQ24780SRUYR

INPUTS	OUTPUTS
BAT-PWR12	M-BAT-PWR

System DC/DC

TPS51285B-1RUKR

VINT20	VCC5M VCC3M

CPU DC/DC

M: NCP81215MNTXG
S: NCP302045MNTWG

VINT20	VCCCPUCORE VCCGFXCORE_I VCCSA

VCCCPUIO

NB694GD-Z

VINT20	VCCCPUIO

VCC1R05_SUS

NB693GQ-Z

VCC5M	VCC1R0_SUS

VCC1R2A/VCC0R6B

TPS51716RUKR

VINT20	VCC0R6B VCC1R2A

VCC1R8_SUS

NB694GD-Z

VCC5M	VCC1R8_SUS

VCC2R5A

NB695GD-Z

VCC5M	VCC2R5A

GFXCORE_D

NCP81276MNTXG

VINT20	VCCGFXCORE_D

VCC1R35VIDEO

TPS51219RTER

VCC5M	VCC1R35VIDEO

VCC1R0VIDEO

NB695GD-Z

VCC5M	VCC1R0VIDEO

TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	Suspend-to-Disk (STD)
	Deep S4	M-OFF	ON	ON	OFF	OFF	OFF	OFF		
G2	S5	M3	ON	ON	ON	ON	OFF	OFF	Hibernation or Shutdown	Soft Off
	Deep S5	M-OFF	ON	ON	OFF	OFF	OFF	OFF		
	S5 EC OFF	M-OFF	OFF	OFF	OFF	OFF	OFF	OFF		
G3	---	---	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off

EC SMBus1 address

Device	Address
G-Senor (BMA255)	0011 000Xb
G-Senor (KX022-1020)	0011 110Xb

EC SMBus2 address

Device	Address
Smart Battery	0001 0110 b
Charge Controller	0001 0010 b

EC SMBus3 address

Device	Address
PCH	0x96h
USB Re-driver	0x20h / 0x21h (Reserve)
USB Re-driver(AUO)	0x52h / 0x53h (Reserve)

EC SMBus4 address

Device	Address
DGPU	0x9Eh

EC SMBus5 address

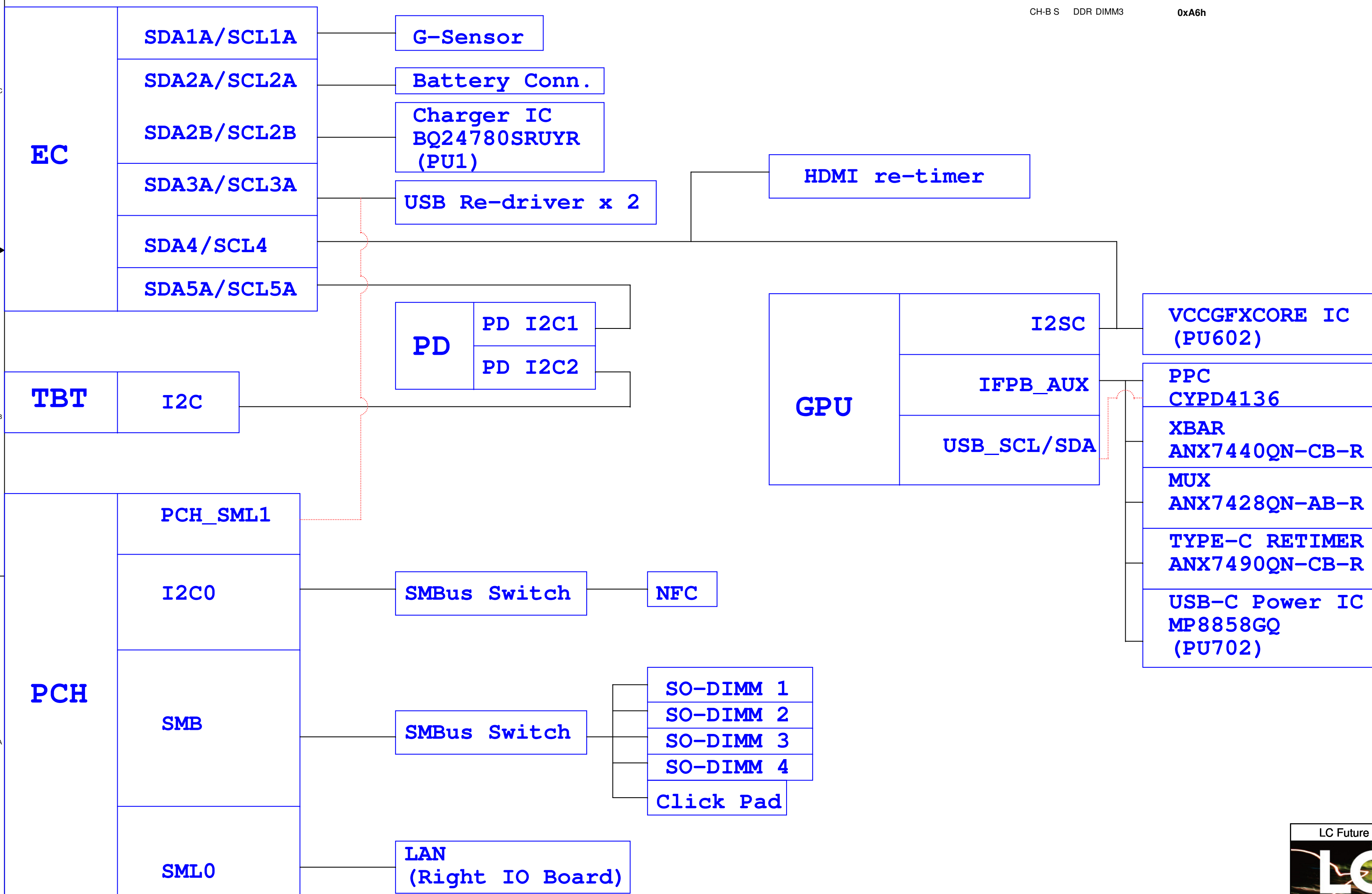
Device	Address
Power Delivery	01001 XXXXb

PCH SM Bus address

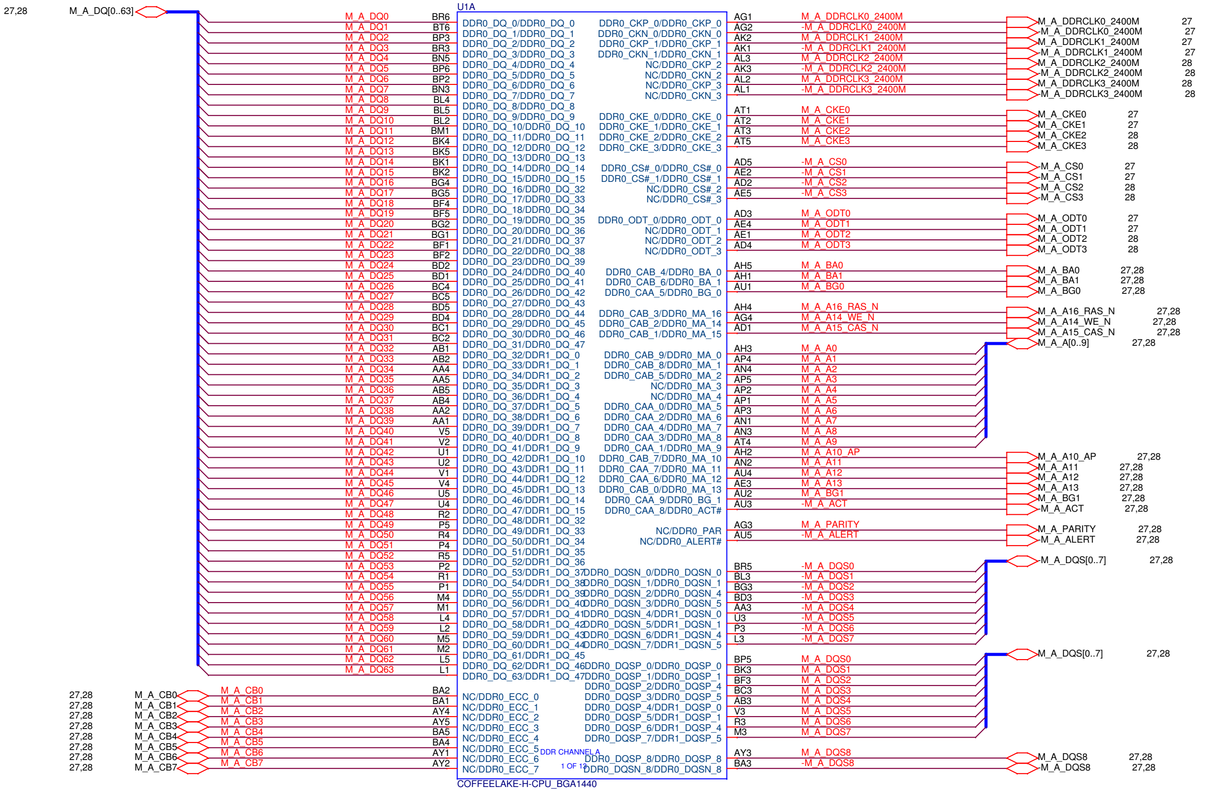
Device		Address
CH-A P	DDR DIMM0	0xA0h
CH-A S	DDR DIMM1	0xA2h
CH-B P	DDR DIMM2	0xA4h
CH-B S	DDR DIMM3	0xA6h

PCH SM Bus0 address

Device	Address
Intel Lan_I219	0XC8h

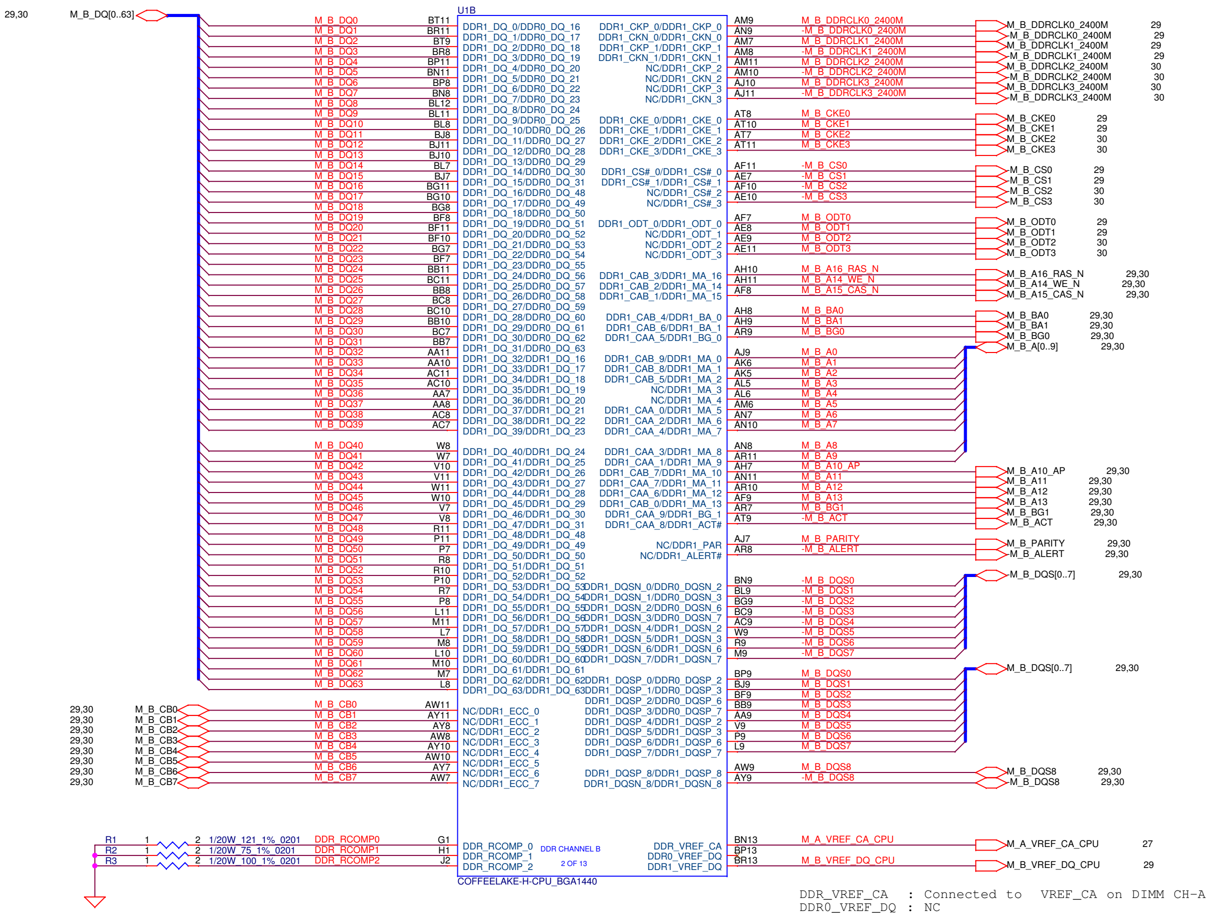


CPU



DDR4 INTERLEAVE IMPLEMENTATION

CPU



DDR_VREF_CA : Connected to VREF_CA on DIMM CH-A
DDR0_VREF_DQ : NC
DDR1_VREF_DQ : Connected to VREF_CA on DIMM CH-B

CPU

31 PEG_RXP[15:0]
31 PEG_RXN[15:0]
PEG_TXP[15:0] 31
PEG_TXN[15:0] 31
U1C
PEG_RXP15 E25 PEG_RXP_0 PEG_TXP_0 B25 PEG_TXP15_C C1 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP15
PEG_RXN15 D25 PEG_RXN_0 PEG_TXN_0 A25 PEG_TXN15_C C2 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN15
PEG_RXP14 E24 PEG_RXP_1 PEG_TXP_1 B24 PEG_TXP14_C C3 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP14
PEG_RXN14 F24 PEG_RXN_1 PEG_TXN_1 C24 PEG_TXN14_C C4 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN14
PEG_RXP13 E23 PEG_RXP_2 PEG_TXP_2 B23 PEG_TXP13_C C5 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP13
PEG_RXN13 D23 PEG_RXN_2 PEG_TXN_2 A23 PEG_TXN13_C C6 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN13
PEG_RXP12 E22 PEG_RXP_3 PEG_TXP_3 B22 PEG_TXP12_C C7 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP12
PEG_RXN12 F22 PEG_RXN_3 PEG_TXN_3 C22 PEG_TXN12_C C8 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN12
PEG_RXP11 E21 PEG_RXP_4 PEG_TXP_4 B21 PEG_TXP11_C C9 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP11
PEG_RXN11 D21 PEG_RXN_4 PEG_TXN_4 A21 PEG_TXN11_C C10 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN11
PEG_RXP10 E20 PEG_RXP_5 PEG_TXP_5 B20 PEG_TXP10_C C11 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP10
PEG_RXN10 F20 PEG_RXN_5 PEG_TXN_5 C20 PEG_TXN10_C C12 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN10
PEG_RXP9 E19 PEG_RXP_6 PEG_TXP_6 B19 PEG_TXP9_C C13 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP9
PEG_RXN9 D19 PEG_RXN_6 PEG_TXN_6 A19 PEG_TXN9_C C14 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN9
PEG_RXP8 E18 PEG_RXP_7 PEG_TXP_7 B18 PEG_TXP8_C C15 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP8
PEG_RXN8 F18 PEG_RXN_7 PEG_TXN_7 C18 PEG_TXN8_C C16 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN8
PEG_RXP7 D17 PEG_RXP_8 PEG_TXP_8 A17 PEG_TXP7_C C17 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP7
PEG_RXN7 E17 PEG_RXN_8 PEG_TXN_8 B17 PEG_TXN7_C C18 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN7
PEG_RXP6 F16 PEG_RXP_9 PEG_TXP_9 C16 PEG_TXP6_C C19 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP6
PEG_RXN6 E16 PEG_RXN_9 PEG_TXN_9 B16 PEG_TXN6_C C20 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN6
PEG_RXP5 D15 PEG_RXP_10 PEG_TXP_10 A15 PEG_TXP5_C C21 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP5
PEG_RXN5 E15 PEG_RXN_10 PEG_TXN_10 B15 PEG_TXN5_C C22 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN5
PEG_RXP4 F14 PEG_RXP_11 PEG_TXP_11 C14 PEG_TXP4_C C23 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP4
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PEG_RXP3 D13 PEG_RXP_12 PEG_TXP_12 A13 PEG_TXP3_C C25 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP3
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PEG_RXP2 F12 PEG_RXP_13 PEG_TXP_13 C12 PEG_TXP2_C C27 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP2
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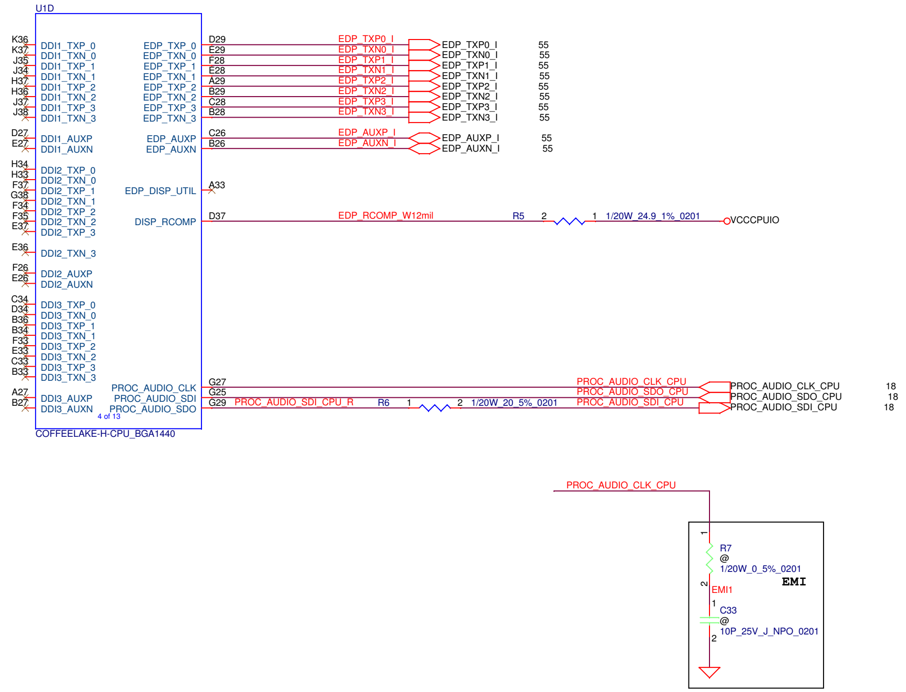
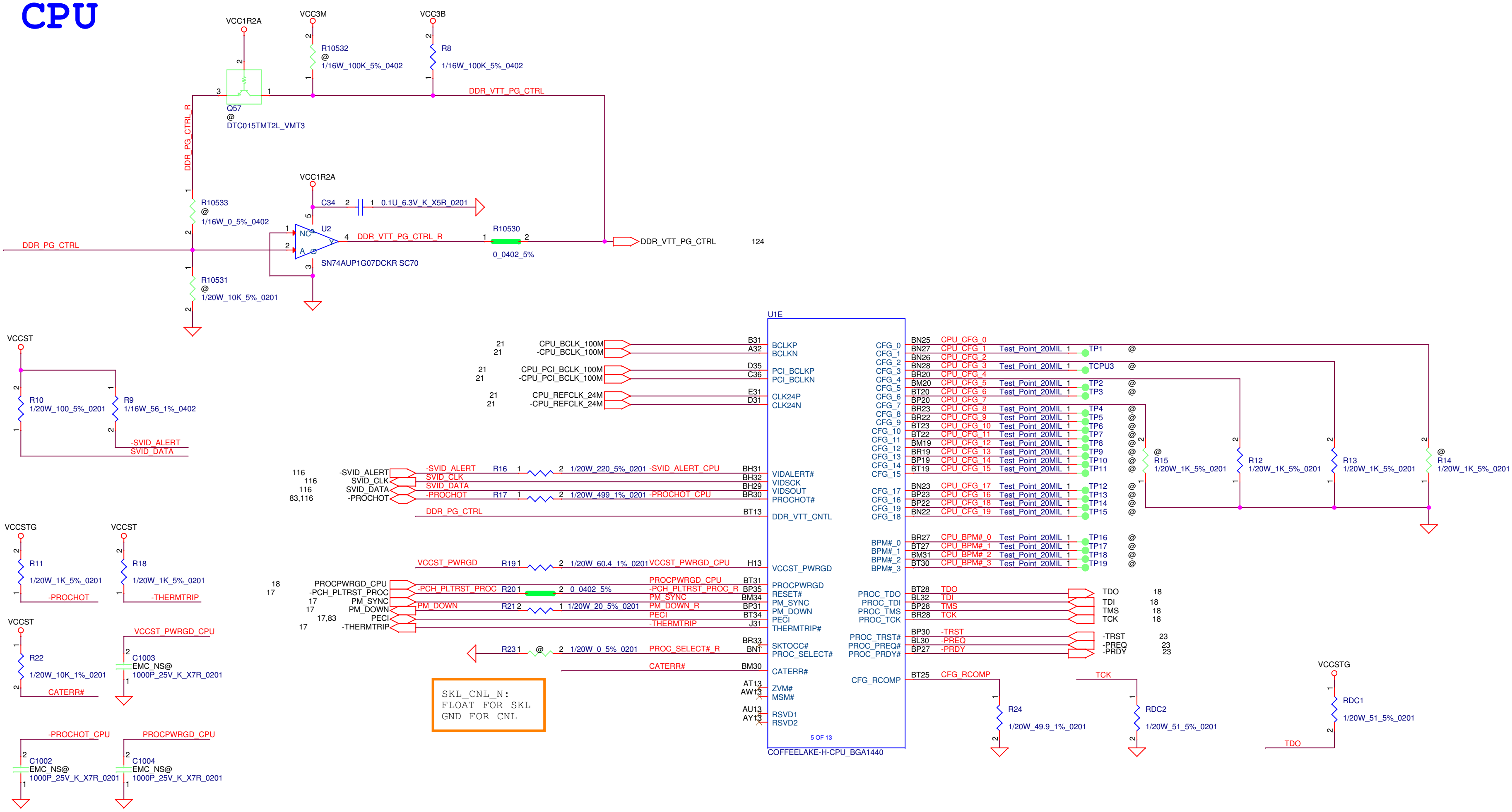
PEG_RXN1 E11 PEG_RXN_14 PEG_TXN_14 B11 PEG_TXN1_C C30 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN1
PEG_RXP0 F10 PEG_RXP_15 PEG_TXP_15 C10 PEG_TXP0_C C31 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXP0
PEG_RXN0 E10 PEG_RXN_15 PEG_TXN_15 B10 PEG_TXN0_C C32 1 2 0.22U_6.3V_K_X5R_0201 PEG_TXN0
VCCCPUIO R4 1 2 1/20W_24.9_1%_0201 PEG_COMP_W12mil G2 PEG_RCOMP
16 DMI_TXP0 DMI_TXP0 D8 DMI_RXP_0 DMI_TXP_0 B8 DMI_RXP0 DMI_RXP0 16
16 DMI_TXN0 DMI_TXN0 E8 DMI_RXN_0 DMI_TXN_0 A8 DMI_RXN0 DMI_RXN0 16
16 DMI_TXP1 DMI_TXP1 E6 DMI_RXP_1 DMI_TXP_1 C6 DMI_RXP1 DMI_RXP1 16
16 DMI_TXN1 DMI_TXN1 F6 DMI_RXN_1 DMI_TXN_1 B6 DMI_RXN1 DMI_RXN1 16
16 DMI_TXP2 DMI_TXP2 D5 DMI_RXP_2 DMI_TXP_2 B5 DMI_RXP2 DMI_RXP2 16
16 DMI_TXN2 DMI_TXN2 E5 DMI_RXN_2 DMI_TXN_2 A5 DMI_RXN2 DMI_RXN2 16
16 DMI_TXP3 DMI_TXP3 J8 DMI_RXP_3 DMI_TXP_3 D4 DMI_RXP3 DMI_RXP3 16
16 DMI_TXN3 DMI_TXN3 J9 DMI_RXN_3 DMI_TXN_3 B4 DMI_RXN3 DMI_RXN3 16
3 OF 13
COFFEELAKE-H-CPU_BGA1440

CPU



U1D
K36 DDI1_TXP_0
K37 DDI1_TXN_0
J35 DDI1_TXP_1
J34 DDI1_TXN_1
H37 DDI1_TXP_2
H36 DDI1_TXN_2
J37 DDI1_TXP_3
J38 DDI1_TXN_3
D27 DDI1_AUXP
E27 DDI1_AUXN
H34 DDI2_TXP_0
H33 DDI2_TXN_0
F37 DDI2_TXP_1
G38 DDI2_TXN_1
F34 DDI2_TXP_2
F35 DDI2_TXN_2
E37 DDI2_TXP_3
E36 DDI2_TXN_3
F26 DDI2_AUXP
E26 DDI2_AUXN
C34 DDI3_TXP_0
D34 DDI3_TXN_0
B36 DDI3_TXP_1
B34 DDI3_TXN_1
F33 DDI3_TXP_2
E33 DDI3_TXN_2
C33 DDI3_TXP_3
B33 DDI3_TXN_3
A27 DDI3_AUXP
B27 DDI3_AUXN
EDP_TXP_0 D29 EDP_TXP0_I EDP_TXP0_I 55
EDP_TXN_0 E29 EDP_TXN0_I EDP_TXN0_I 55
EDP_TXP_1 F28 EDP_TXP1_I EDP_TXP1_I 55
EDP_TXN_1 E28 EDP_TXN1_I EDP_TXN1_I 55
EDP_TXP_2 A29 EDP_TXP2_I EDP_TXP2_I 55
EDP_TXN_2 B29 EDP_TXN2_I EDP_TXN2_I 55
EDP_TXP_3 C28 EDP_TXP3_I EDP_TXP3_I 55
EDP_TXN_3 B28 EDP_TXN3_I EDP_TXN3_I 55
EDP_AUXP C26 EDP_AUXP_I EDP_AUXP_I 55
EDP_AUXN B26 EDP_AUXN_I EDP_AUXN_I 55
EDP_DISP_UTIL A33
DISP_RCOMP D37 EDP_RCOMP_W12mil R5 2 1 1/20W_24.9_1%_0201 VCCCPUIO
PROC_AUDIO_CLK G27 PROC_AUDIO_CLK_CPU PROC_AUDIO_CLK_CPU 18
PROC_AUDIO_SDI G25 PROC_AUDIO_SDO_CPU PROC_AUDIO_SDO_CPU 18
PROC_AUDIO_SDO G29 PROC_AUDIO_SDI_CPU_R R6 1 2 1/20W_20_5%_0201 PROC_AUDIO_SDI_CPU PROC_AUDIO_SDI_CPU 18
4 of 13
COFFEELAKE-H-CPU_BGA1440
PROC_AUDIO_CLK_CPU
R7
@
1/20W_0_5%_0201
EMI
EMI1
C33
@
10P_25V_J_NPO_0201

CPU



If VCCSTG is used instead of VCC1R05_SUS,
VCCST_PWRGD will be off in Sleep S0 because
VCCSTG may be turned off when in Sleep S0.
Currently, VCCSTG is still on in Sleep S0
but we may change logic to turn off VCCSTG in sleep S0.
(CT_20141216)

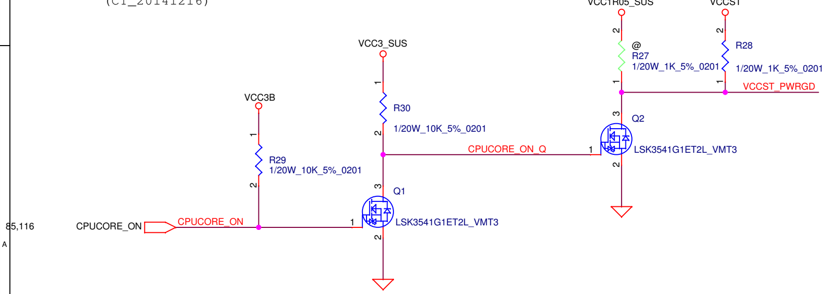


TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:
1 : No Stall <------------ LOGIC
0 : Stall

CFG[2] : PEG Static Lane Reversal
1 : Normal Operation
0 : Lane Reversal <------------ LOGIC

CFG[4] : eDP enable
1 : Disabled
0 : Enabled <------------ LOGIC

CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0
11 : 1x16 <------------ LOGIC

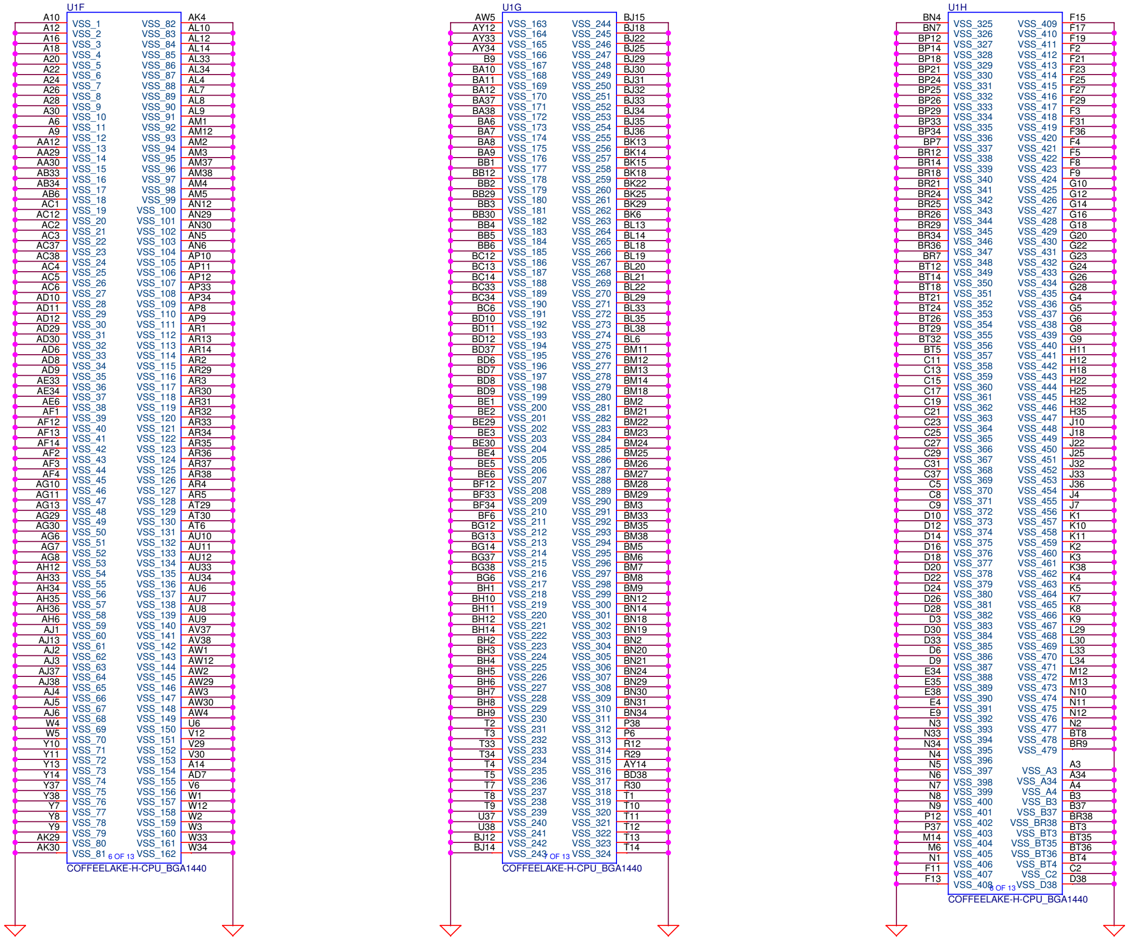
CFG[7] : PEG Training
1 : PEG Train immediately following RESET# deassertion <------------ LOGIC
0 : PEG Wait for BIOS for training

CFG[19:8] : Reserved

For x16 Reversal Lanes - CFG[6/5/2] setting is 110
For x4 Reversal Lanes - CFG[6/5/2] setting is 000

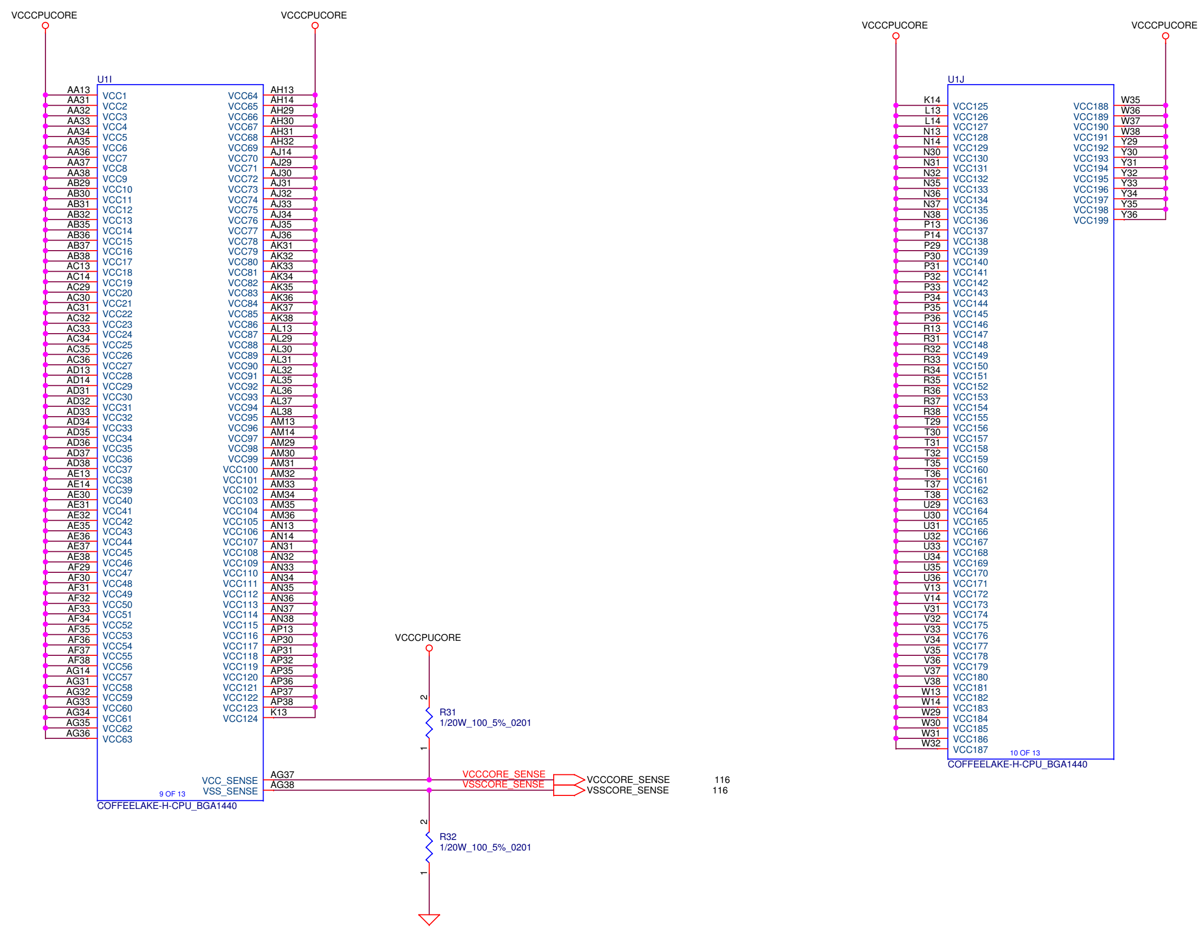
VCCST_PWRGD requirements
1) Indication that the VCCST\VDDQ power supplies are stable and within specification
2) VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
3) VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

CPU



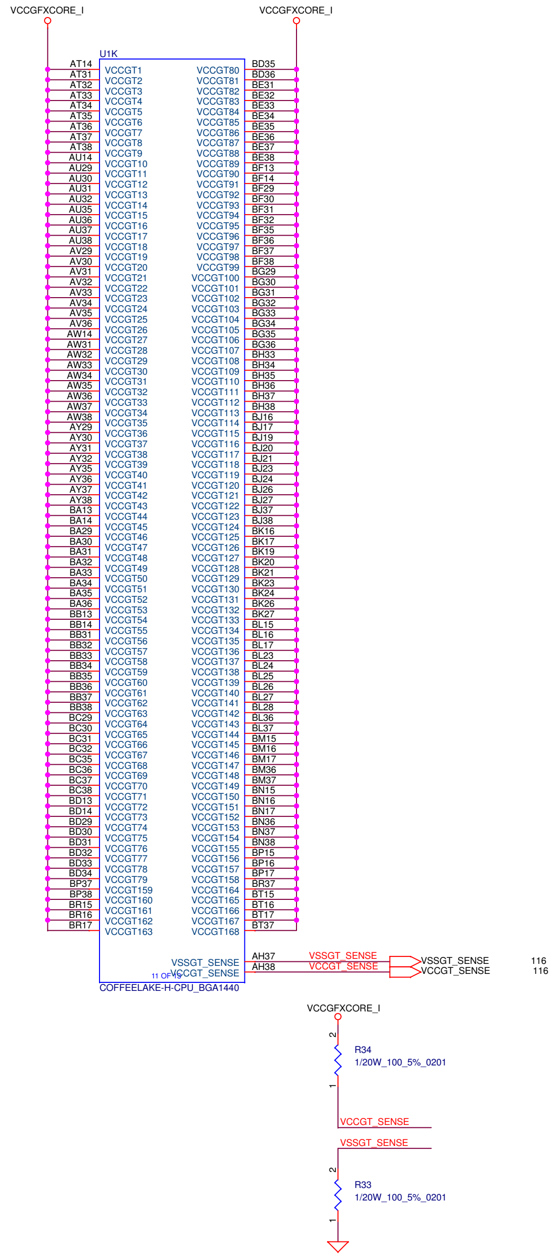
U1F
6 OF 13
COFFEELAKE-H-CPU_BGA1440
U1G
7 OF 13
COFFEELAKE-H-CPU_BGA1440
U1H
8 OF 13
COFFEELAKE-H-CPU_BGA1440

CPU



Project Name: Nighthawk-1
Rev 1.0
Title: CPU
Date: Monday, April 29, 2019

CPU



LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev: 1.0 | Title: CPU

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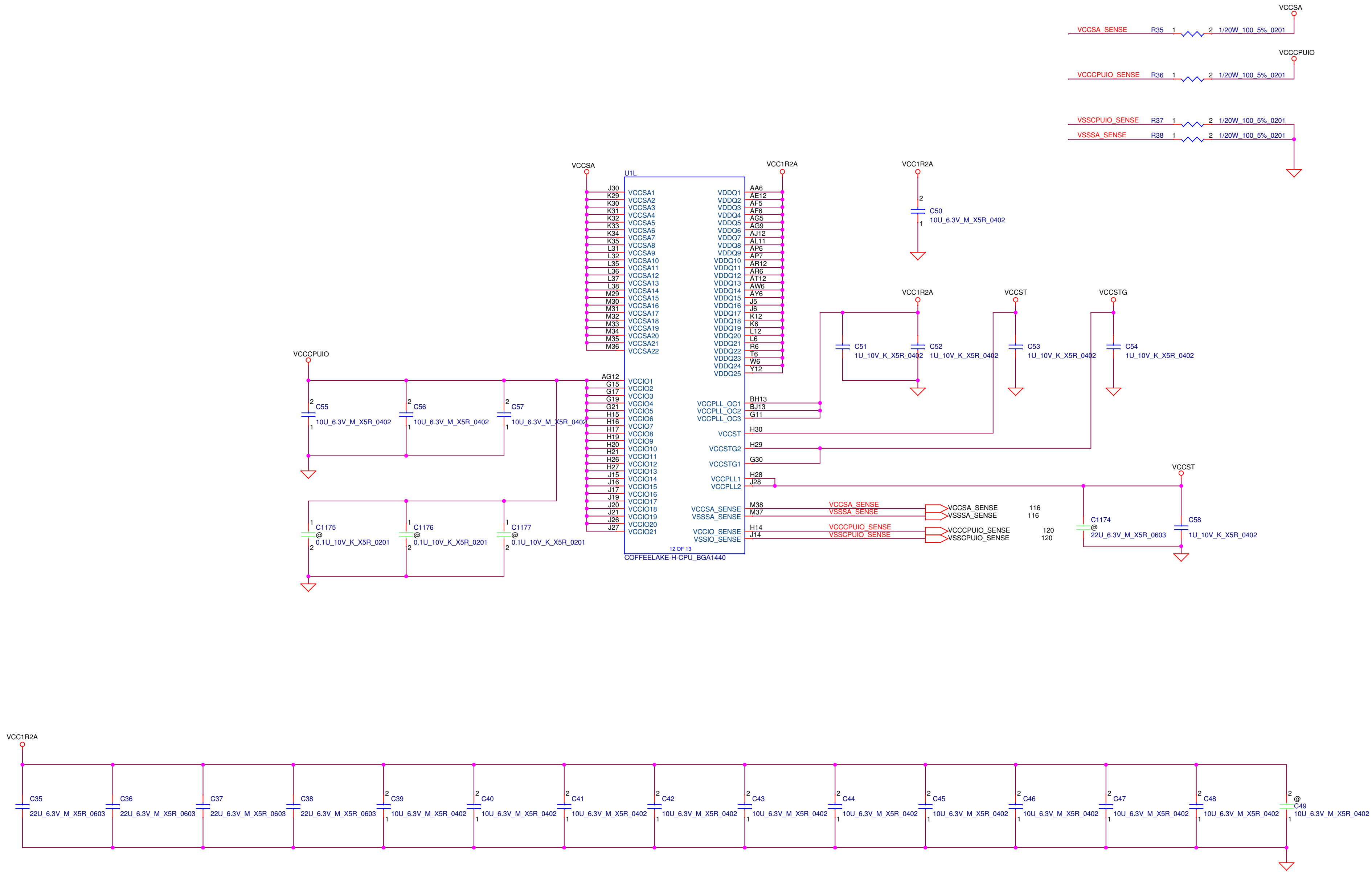
CPU



LC Future Center Secret Data

Project Name: **Nighthawk-1**

Rev 1.0 | Title: **CPU**

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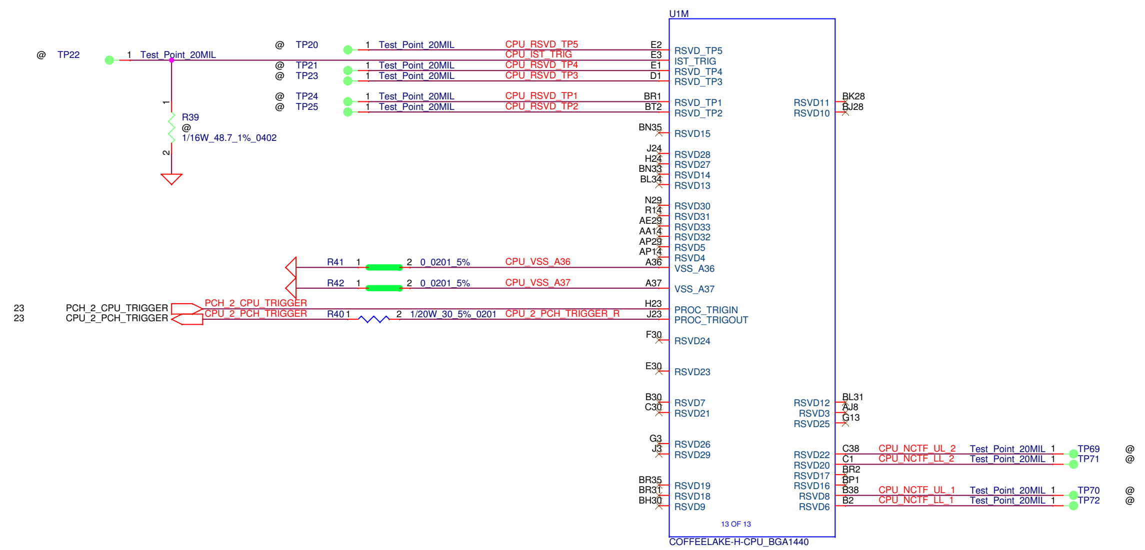
CPU



LC Future Center Secret Data	Project Name
LCFC	Nighthawk-1
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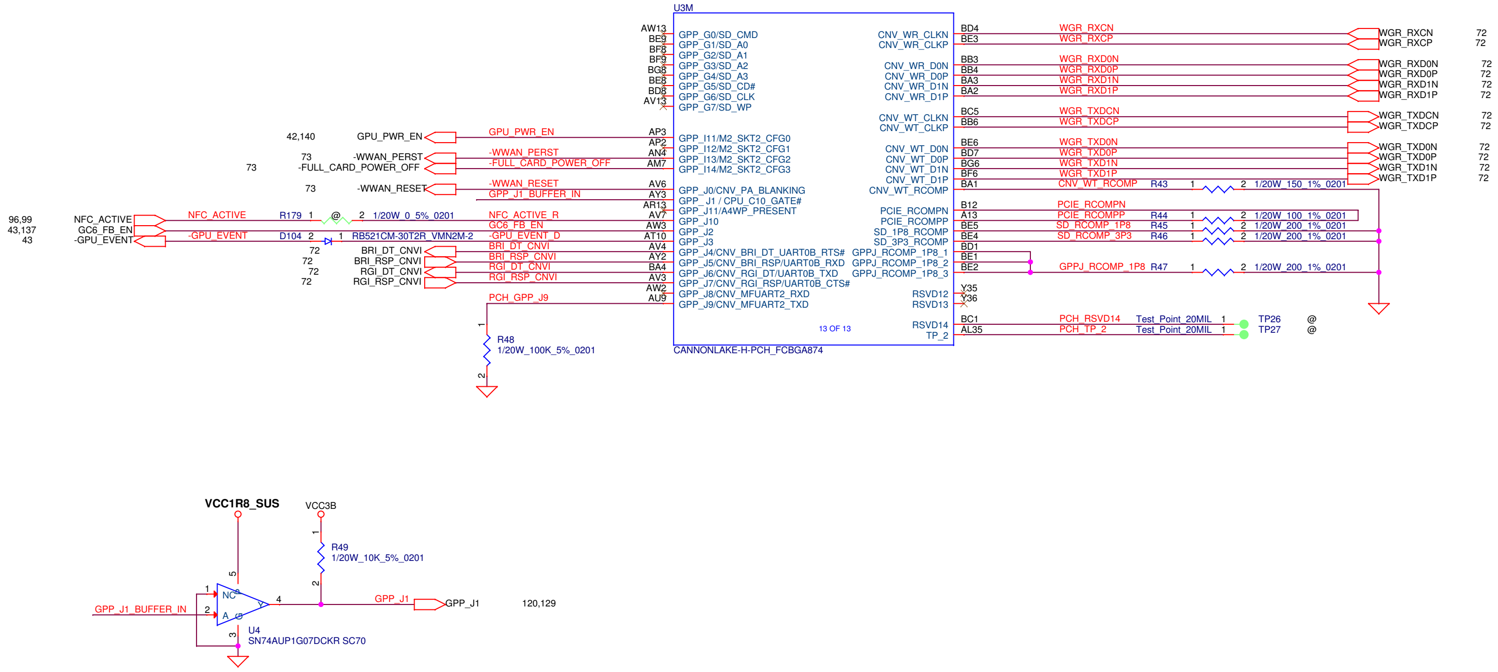
PCH



LC Future Center Secret Data

LCFC

Project Name	Nighthawk-1
Rev 1.0	Title PCH
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PCH

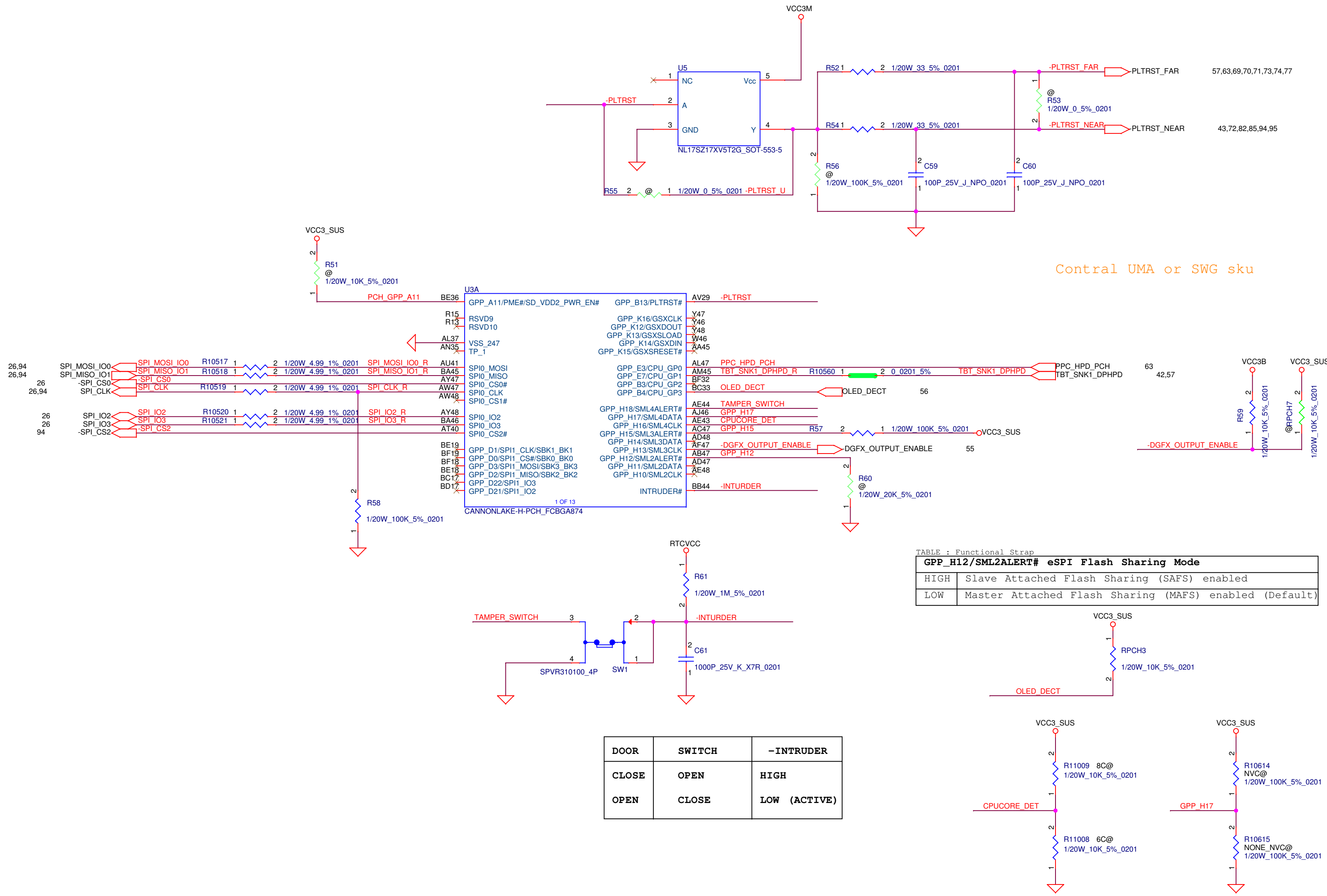


TABLE : Functional Strap

GPP_H12/SML2ALERT#	eSPI Flash Sharing Mode
HIGH	Slave Attached Flash Sharing (SAFS) enabled
LOW	Master Attached Flash Sharing (MAFS) enabled (Default)

DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE)

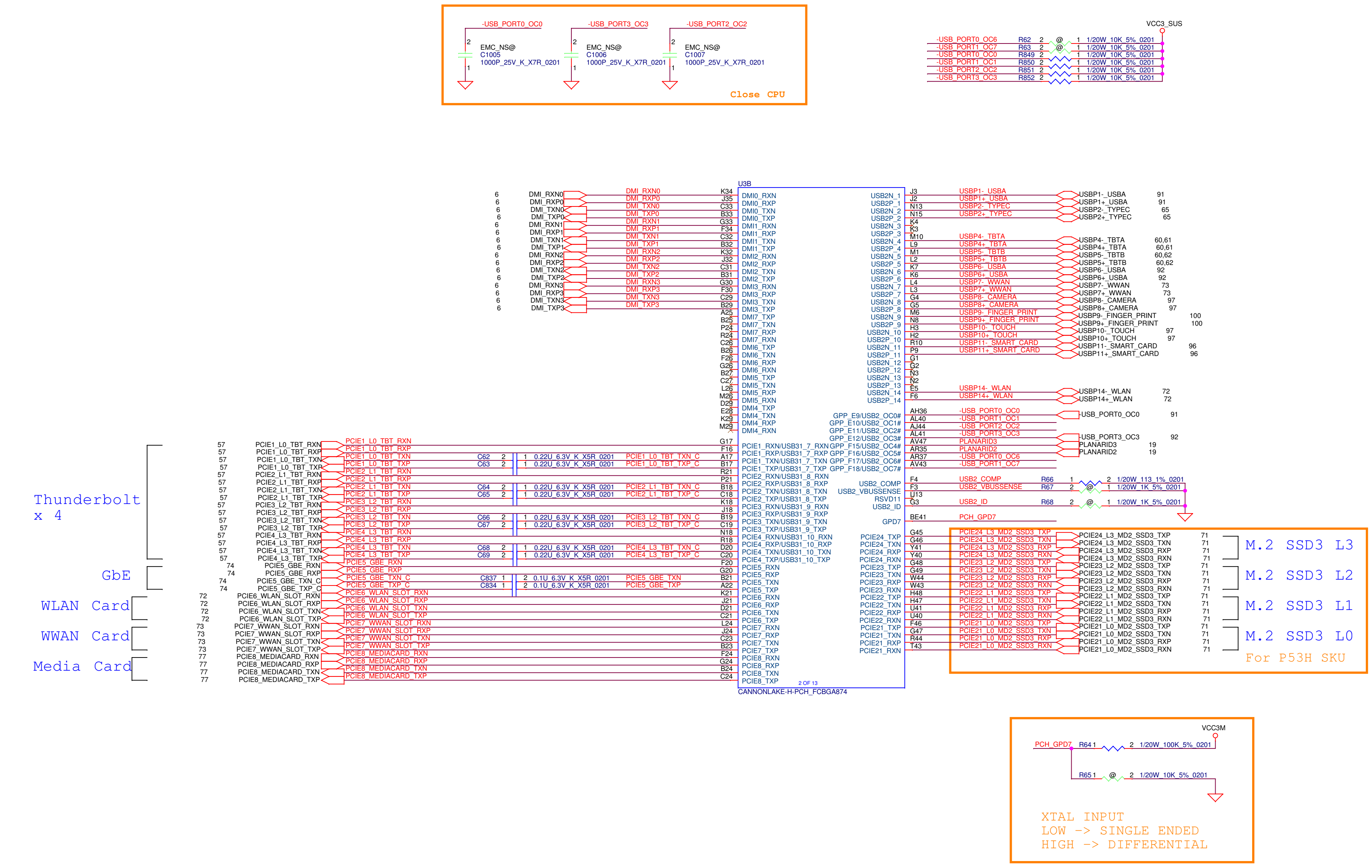
CPUCORE_DET	HIGH	LOW
	8C@	6C@

LC Future Center Secret Data

Project Name: Nighthawk-1

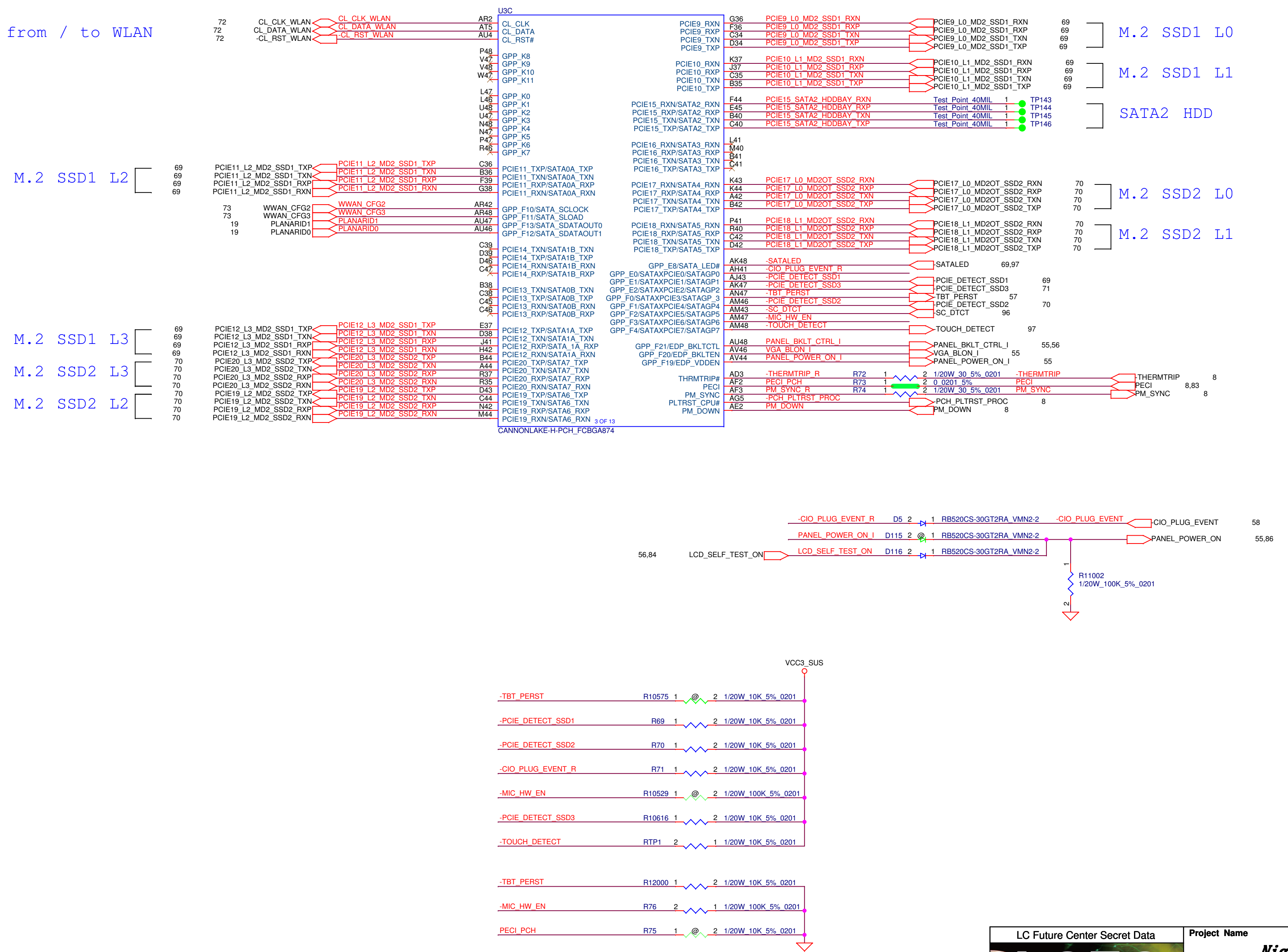
Rev 1.0 | Title: PCH

PCH



Close CPU
VCC3_SUS
U3B
CANNONLAKE-H-PCH_FCBGA874
Thunderbolt x 4
GbE
WLAN Card
WWAN Card
Media Card
M.2 SSD3 L3
M.2 SSD3 L2
M.2 SSD3 L1
M.2 SSD3 L0
For P53H SKU
VCC3M
XTAL INPUT
LOW -> SINGLE ENDED
HIGH -> DIFFERENTIAL

PCH



LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0 | Title: PCH

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PCH

TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.

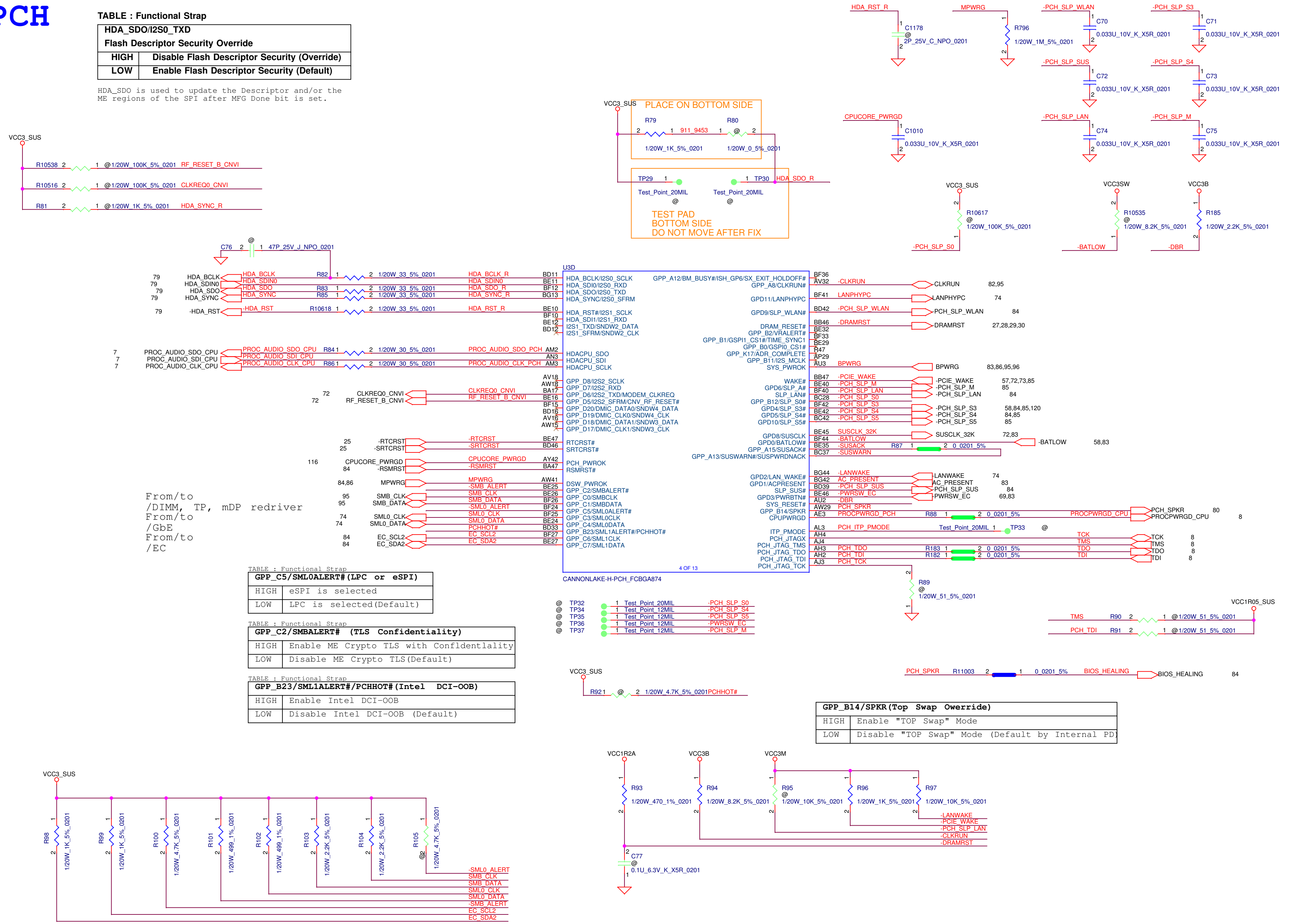


TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

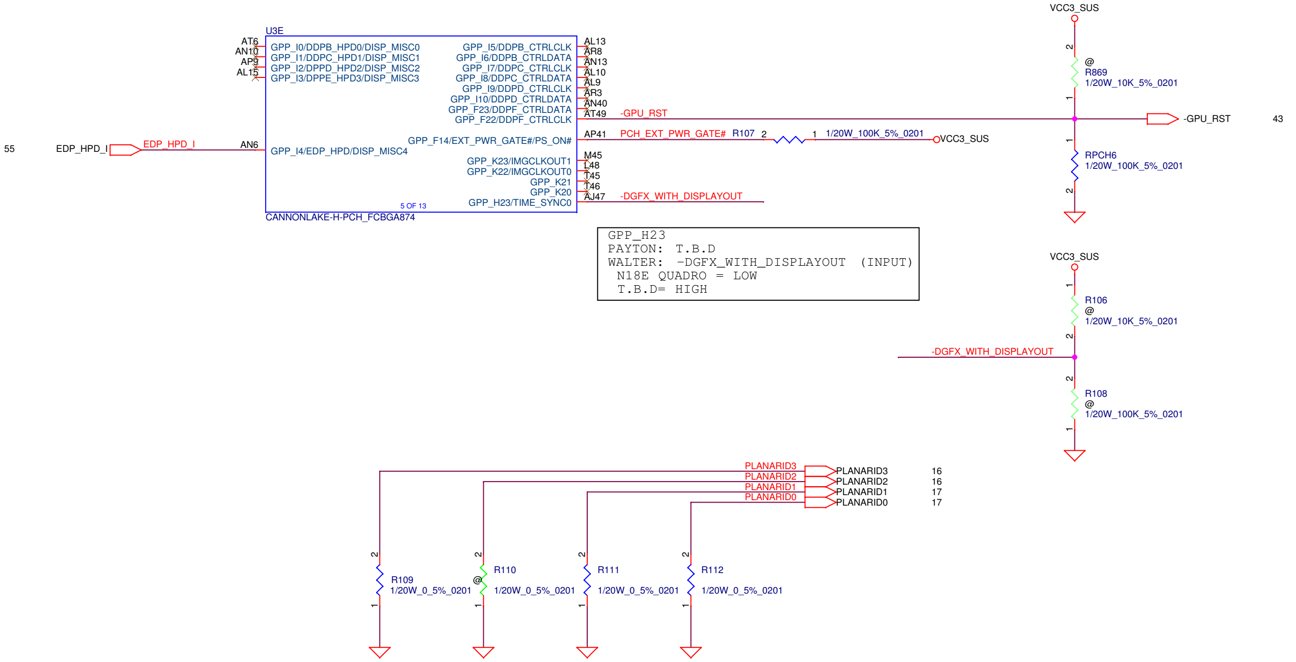
GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confldentlality
LOW	Disable ME Crypto TLS(Default)

TABLE : Functional Strap

GPP_B23/SML1ALERT#/PCHHOT#(Intel DCI-OOB)	
HIGH	Enable Intel DCI-OOB
LOW	Disable Intel DCI-OOB (Default)

GPP_B14/SPKR(Top Swap Override)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

PCH



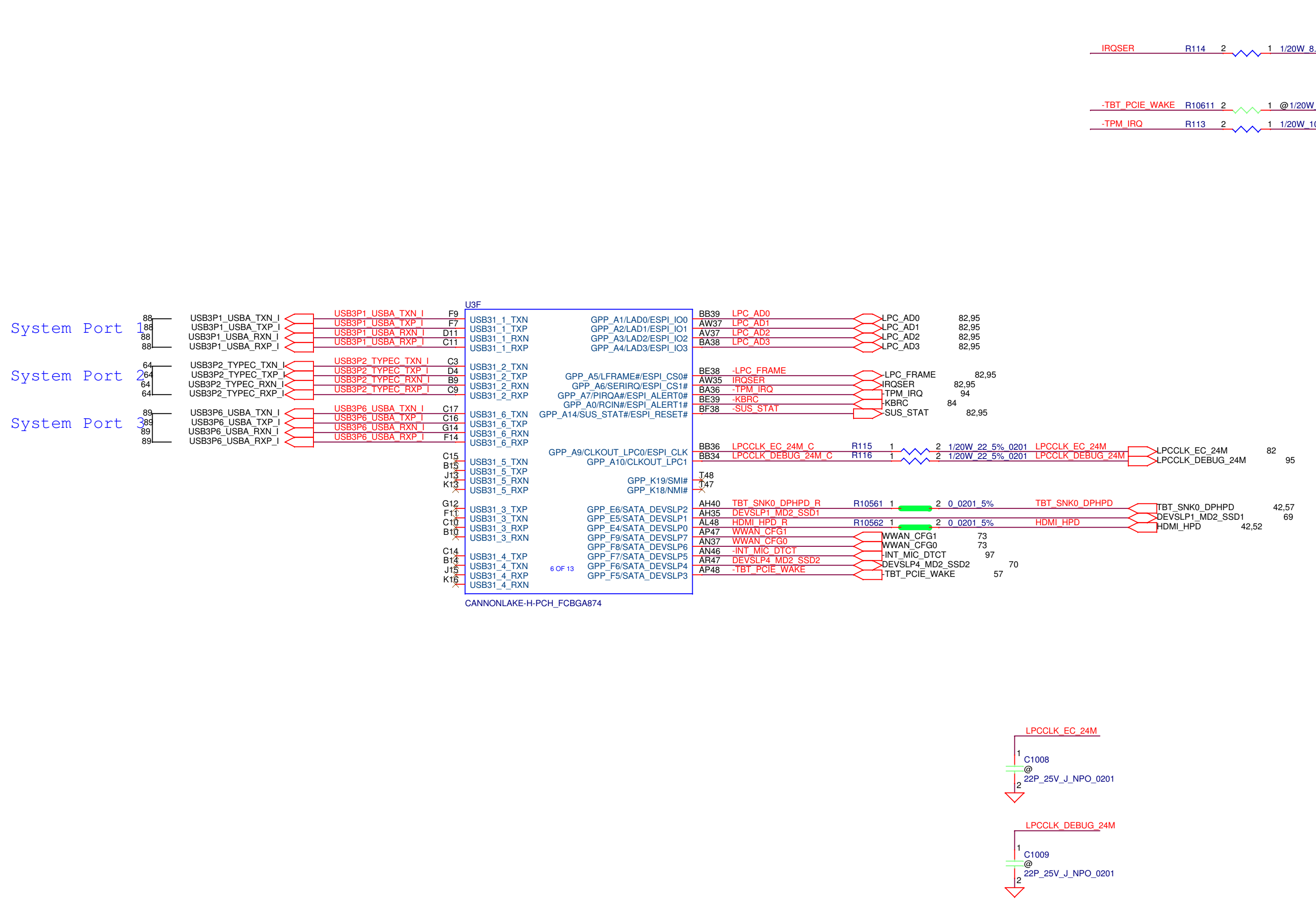
TABLE

	PLANAR ID			
	3	2	1	0
	R109	R110	R111	R112
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3..0]	CPU	PCH
PDV	--------	--------	--------
EVT	0001b	ES	ES
FVT	0010b	ES	ES
SIT	0011b	QS	QS
SVT	0100b	QS	QS

PCH



LC Future Center Secret Data	Project Name: Nighthawk-1
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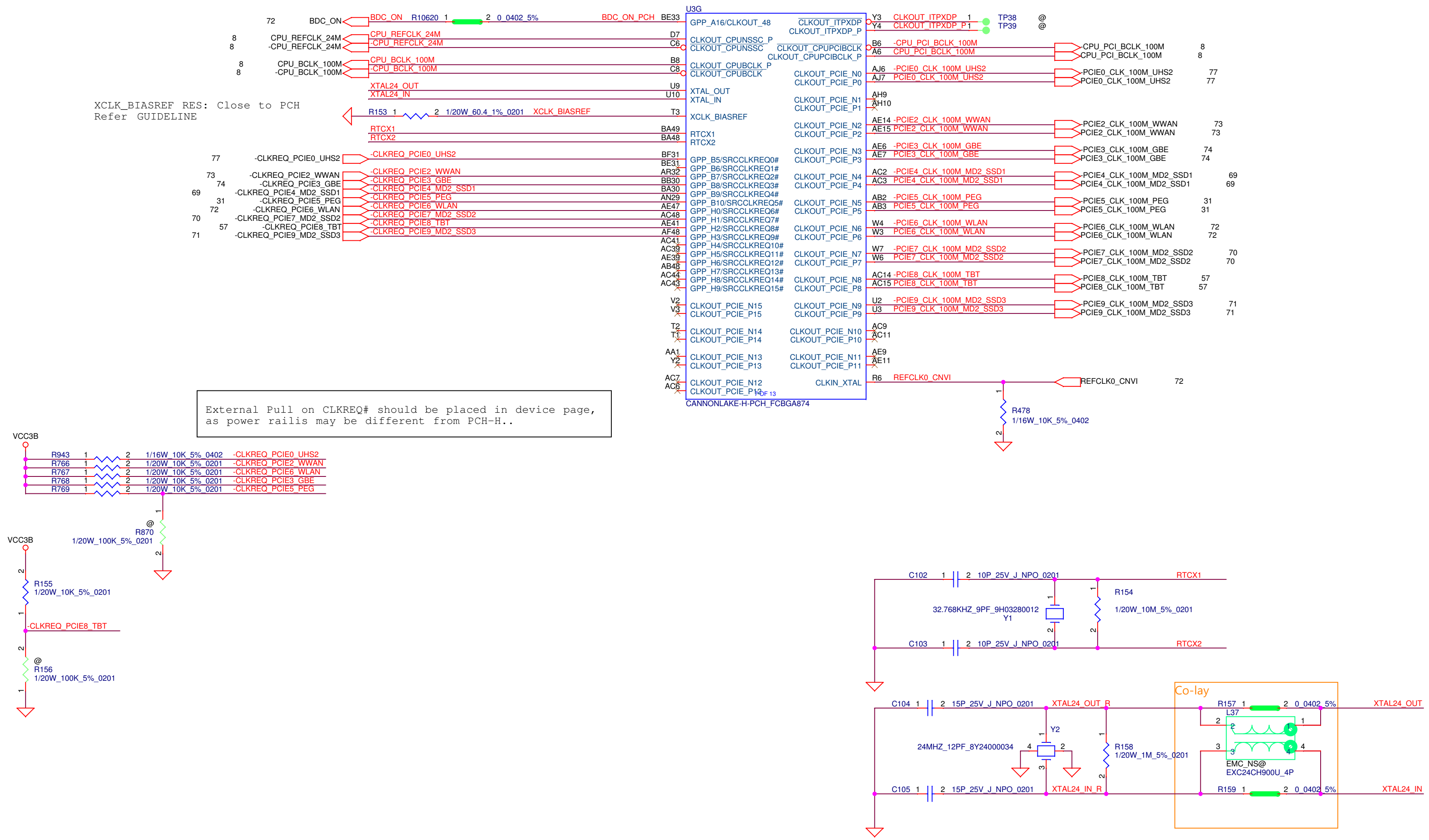
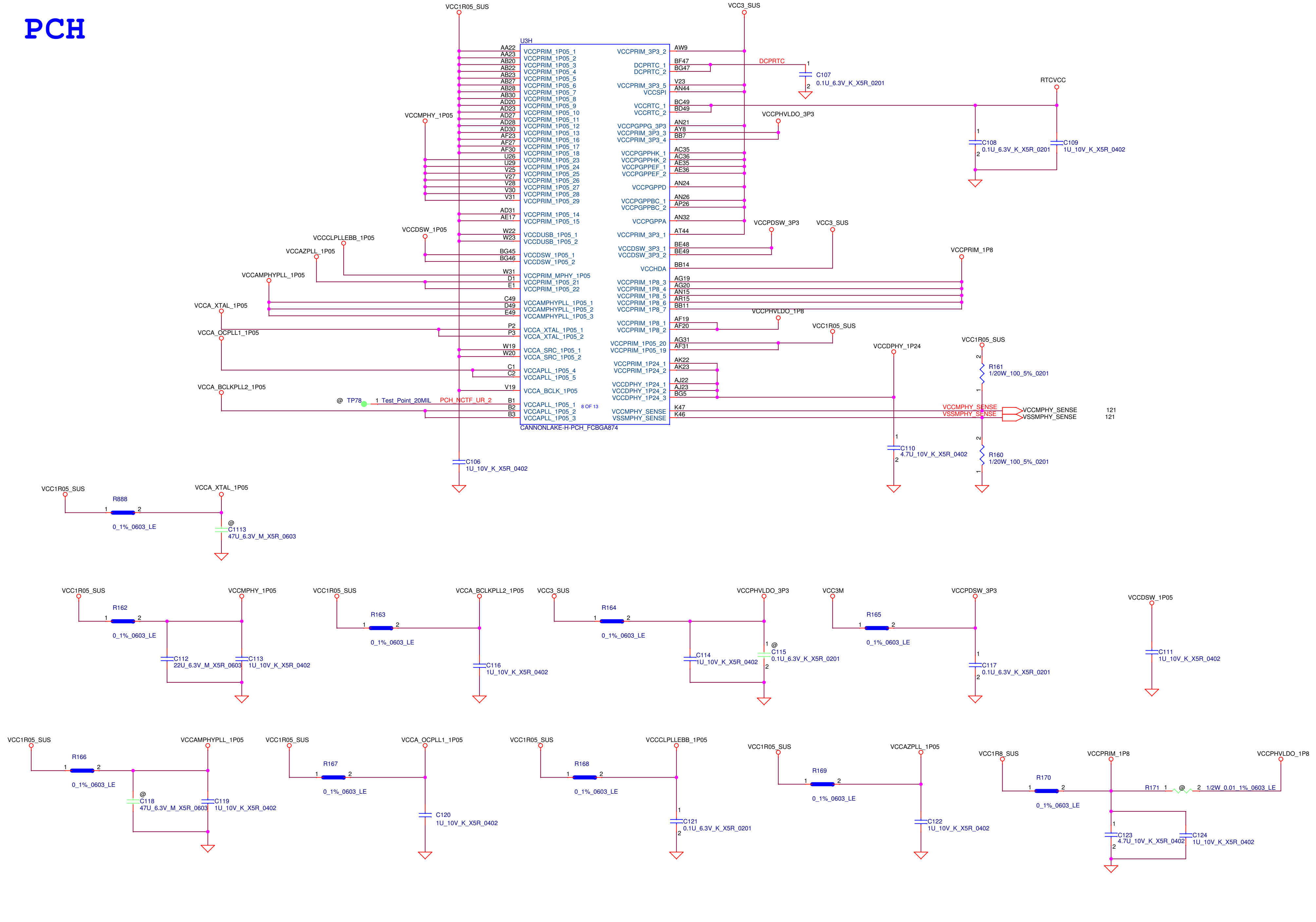
PCH



U3G
CANNONLAKE-H-PCH_FCBGA874
BDC_ON
R10620 0_0402_5%
BDC_ON_PCH
CPU_REFCLK_24M
-CPU_REFCLK_24M
CPU_BCLK_100M
-CPU_BCLK_100M
XTAL24_OUT
XTAL24_IN
XCLK_BIASREF RES: Close to PCH
Refer GUIDELINE
R153 1/20W_60.4_1%_0201
XCLK_BIASREF
RTCX1
RTCX2
-CLKREQ_PCIE0_UHS2
-CLKREQ_PCIE2_WWAN
-CLKREQ_PCIE3_GBE
-CLKREQ_PCIE4_MD2_SSD1
-CLKREQ_PCIE5_PEG
-CLKREQ_PCIE6_WLAN
-CLKREQ_PCIE7_MD2_SSD2
-CLKREQ_PCIE8_TBT
-CLKREQ_PCIE9_MD2_SSD3
GPP_A16/CLKOUT_48
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK
XTAL_OUT
XTAL_IN
XCLK_BIASREF
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK
CLKOUT_CPUPCIBCLK_P
CLKOUT_PCIE_N0 … CLKOUT_PCIE_P11
CLKIN_XTAL
CLKOUT_ITPXDP TP38
CLKOUT_ITPXDP_P TP39
CPU_PCI_BCLK_100M
-CPU_PCI_BCLK_100M
PCIE0_CLK_100M_UHS2
PCIE2_CLK_100M_WWAN
PCIE3_CLK_100M_GBE
PCIE4_CLK_100M_MD2_SSD1
PCIE5_CLK_100M_PEG
PCIE6_CLK_100M_WLAN
PCIE7_CLK_100M_MD2_SSD2
PCIE8_CLK_100M_TBT
PCIE9_CLK_100M_MD2_SSD3
REFCLK0_CNVI
R478 1/16W_10K_5%_0402
External Pull on CLKREQ# should be placed in device page, as power railis may be different from PCH-H..
VCC3B
R943 1/16W_10K_5%_0402 -CLKREQ_PCIE0_UHS2
R766 1/20W_10K_5%_0201 -CLKREQ_PCIE2_WWAN
R767 1/20W_10K_5%_0201 -CLKREQ_PCIE6_WLAN
R768 1/20W_10K_5%_0201 -CLKREQ_PCIE3_GBE
R769 1/20W_10K_5%_0201 -CLKREQ_PCIE5_PEG
R870 1/20W_100K_5%_0201
R155 1/20W_10K_5%_0201
-CLKREQ_PCIE8_TBT
R156 1/20W_100K_5%_0201
C102 10P_25V_J_NPO_0201
RTCX1
32.768KHZ_9PF_9H03280012
Y1
R154 1/20W_10M_5%_0201
C103 10P_25V_J_NPO_0201
RTCX2
Co-lay
C104 15P_25V_J_NPO_0201
XTAL24_OUT_R
Y2
24MHZ_12PF_8Y24000034
R158 1/20W_1M_5%_0201
C105 15P_25V_J_NPO_0201
XTAL24_IN_R
R157 0_0402_5%
L37
EMC_NS@
EXC24CH900U_4P
R159 0_0402_5%
XTAL24_OUT
XTAL24_IN

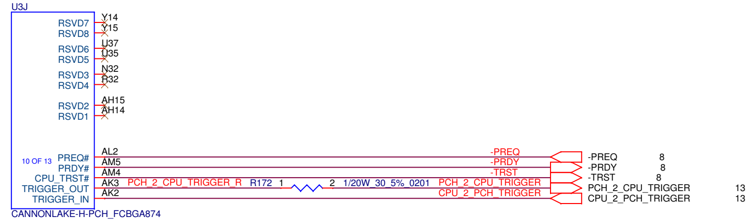
PCH

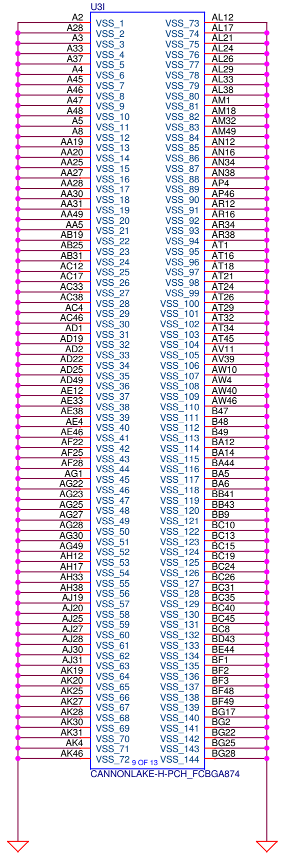


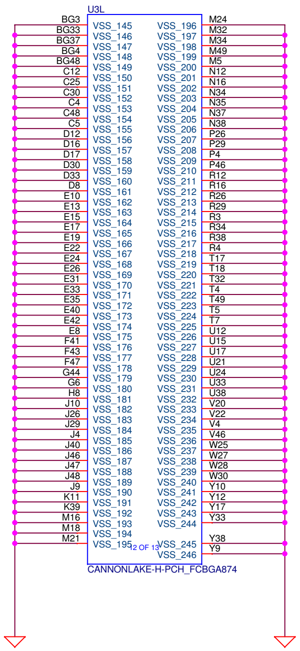
LC Future Center Secret Data

Project Name	Nighthawk-1
Rev 1.0	Title: PCH
Date: Monday, April 29, 2019	Sheet 22 of 142

PCH







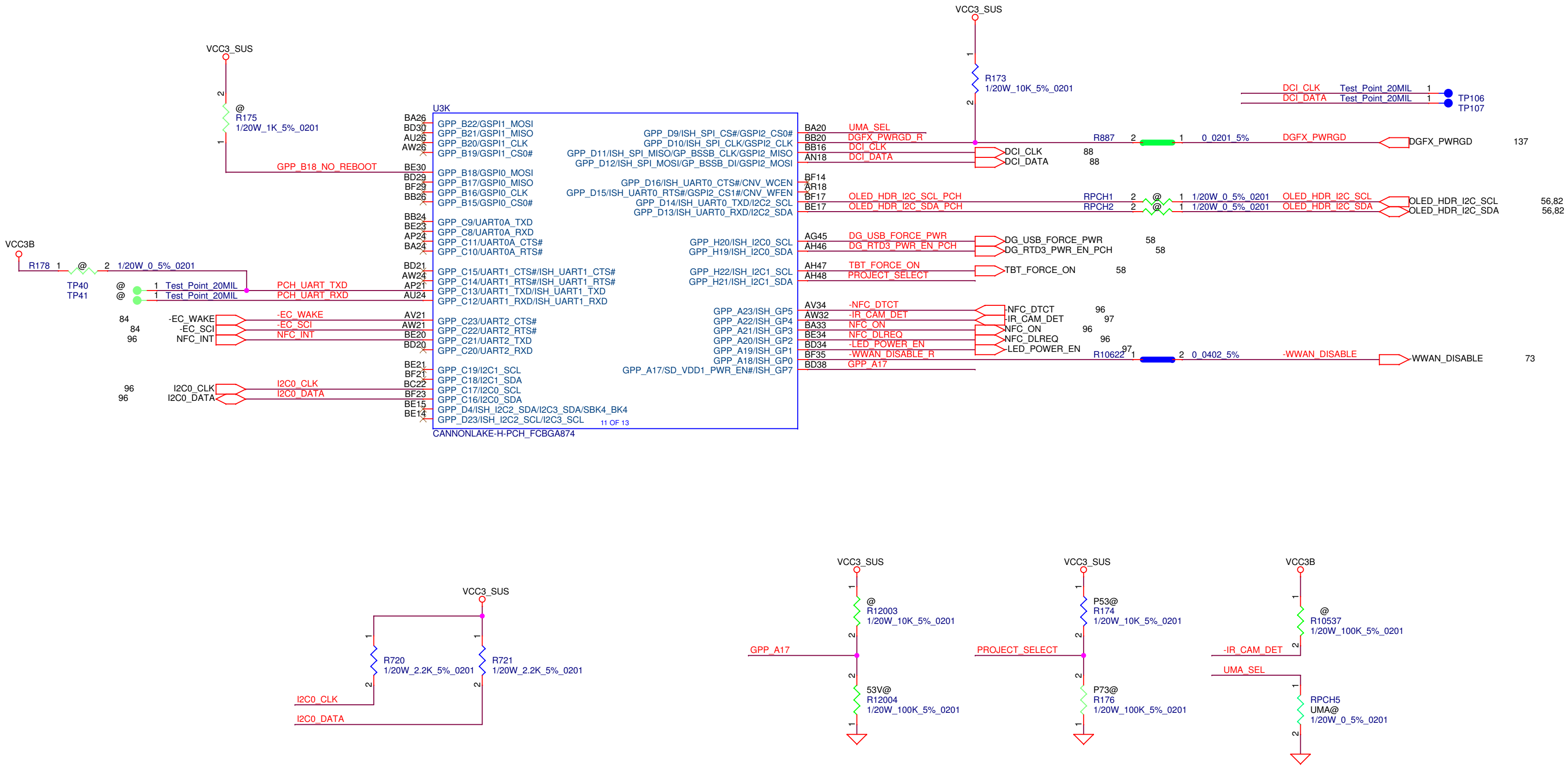
LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 · Title: PCH
	Date: Monday, April 29, 2019 · Sheet 23 of 142

PCH

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		PCHR96
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

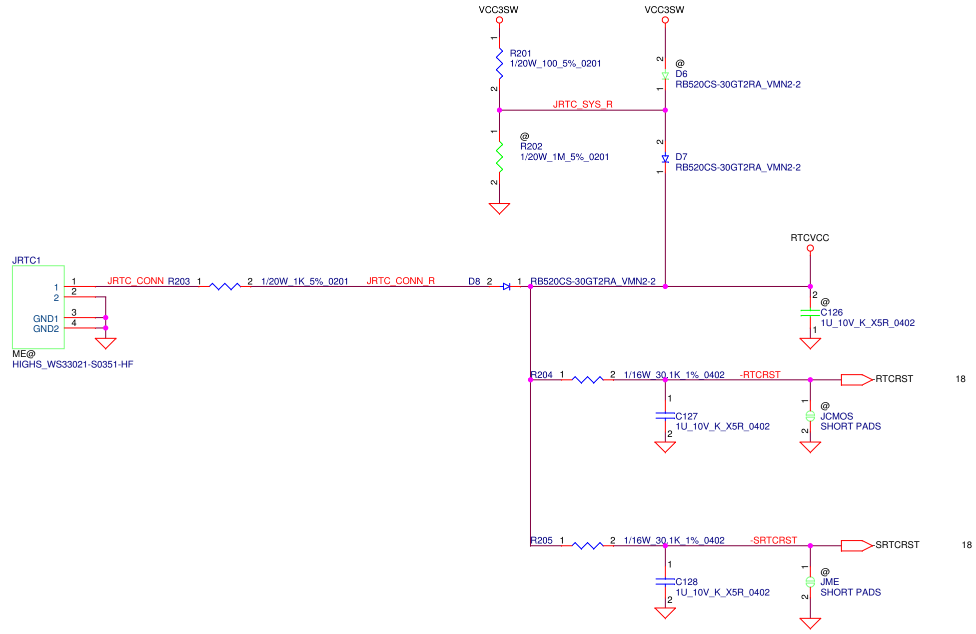
LOGIC



GPP_A17 need BIOS internal PU

	GPP_A17	PROJECT_SELECT
Chiron-2	HIGH	Low
Nighthawk	HIGH	HIGH
Apache	Low	X

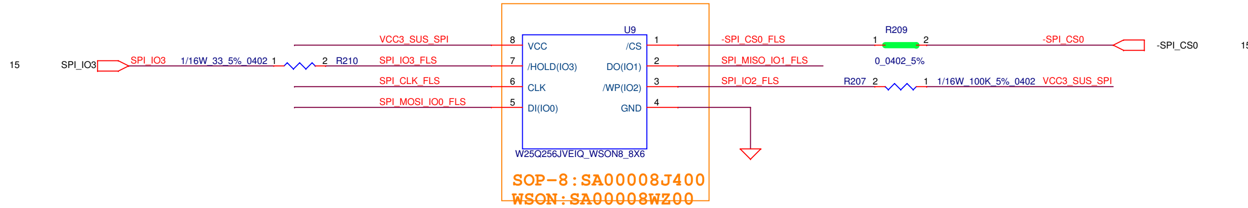
RTC



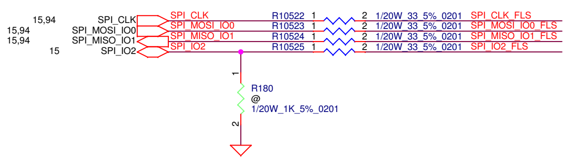
LC Future Center Secret Data

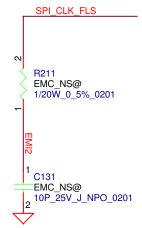
Project Name	Nighthawk-1
Rev 1.0	Title: RTC BATTERY
Date: Monday, April 29, 2019	Sheet 25 of 142

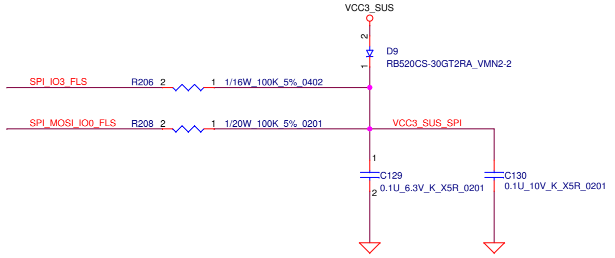
SPI FLASH

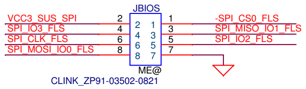


W25Q256JV have PGND in body
for co-lay use, footprint and symbol did't have PGND
confirm with vender PGND just for soldering,
not really need connect to GND.
when WSON8 package popular.
please modify footprint and symbol.
2017/10/27

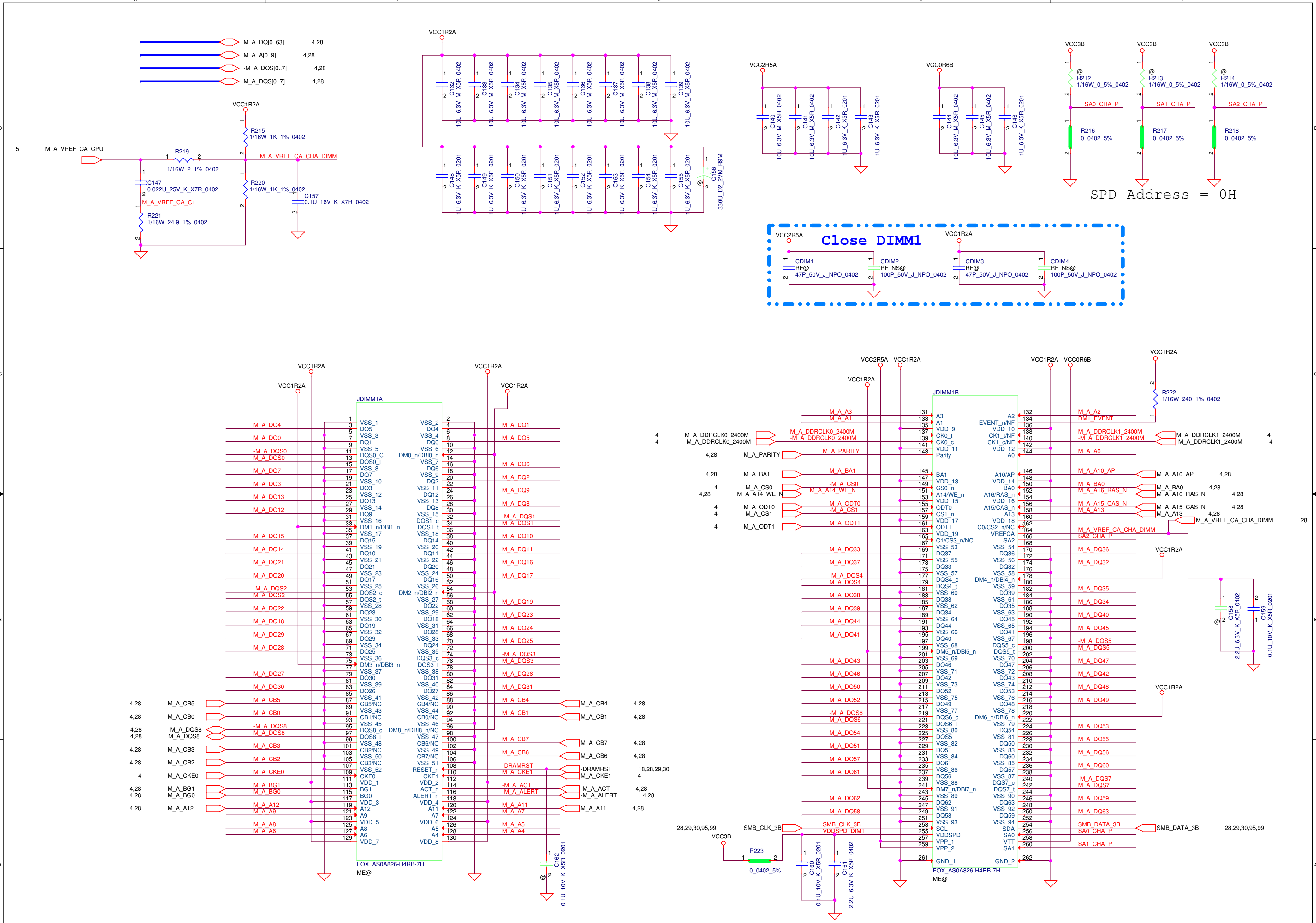






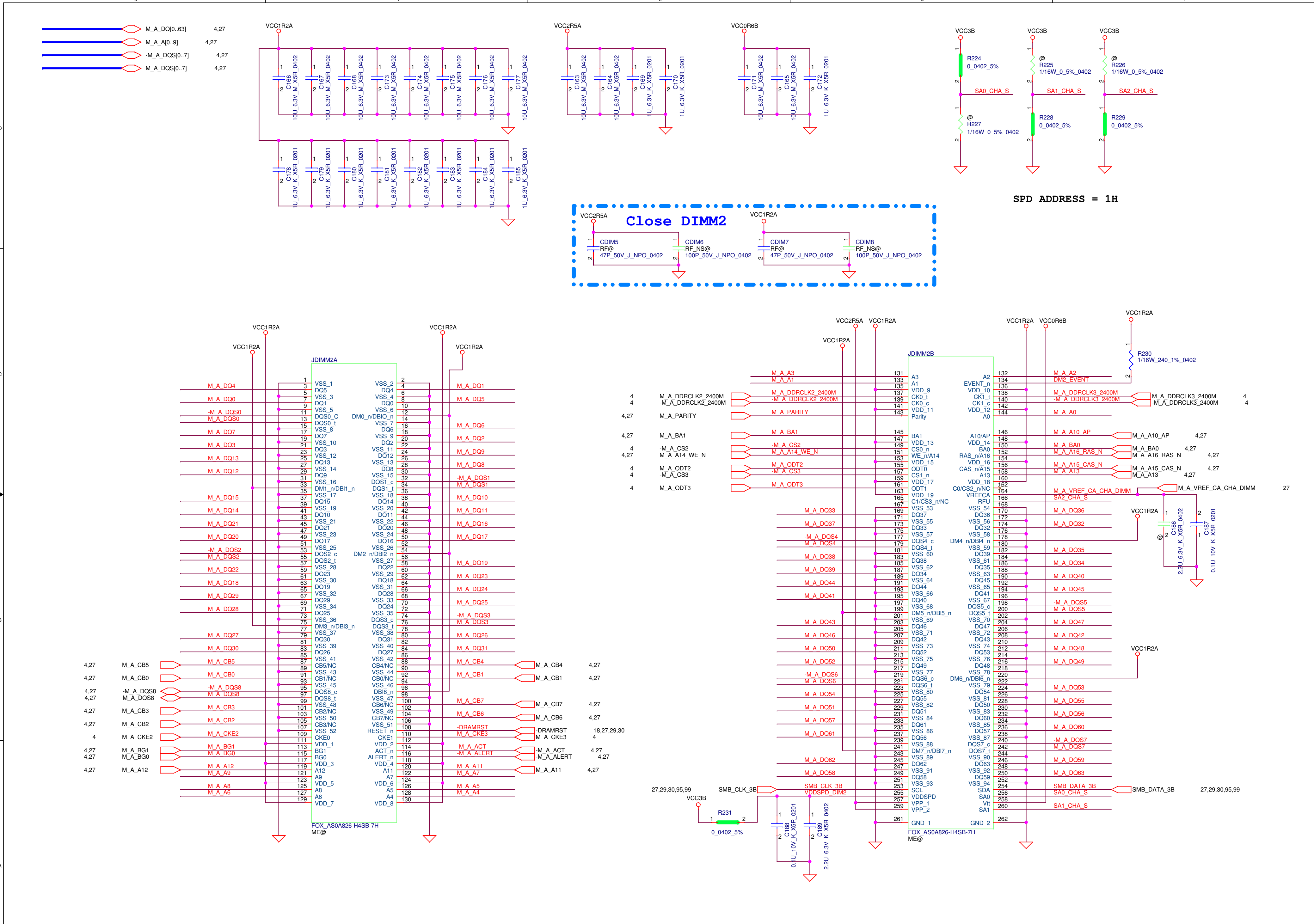


LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 — Title: SPI
	Date: Monday, April 29, 2019 — Sheet 26 of 142



LC Future Center Secret Data

Project Name	Nighthawk-1
Rev 1.0	Title: DDR
Date: Monday, April 29, 2019	Sheet 27 of 142



LC Future Center Secret Data

LCFC

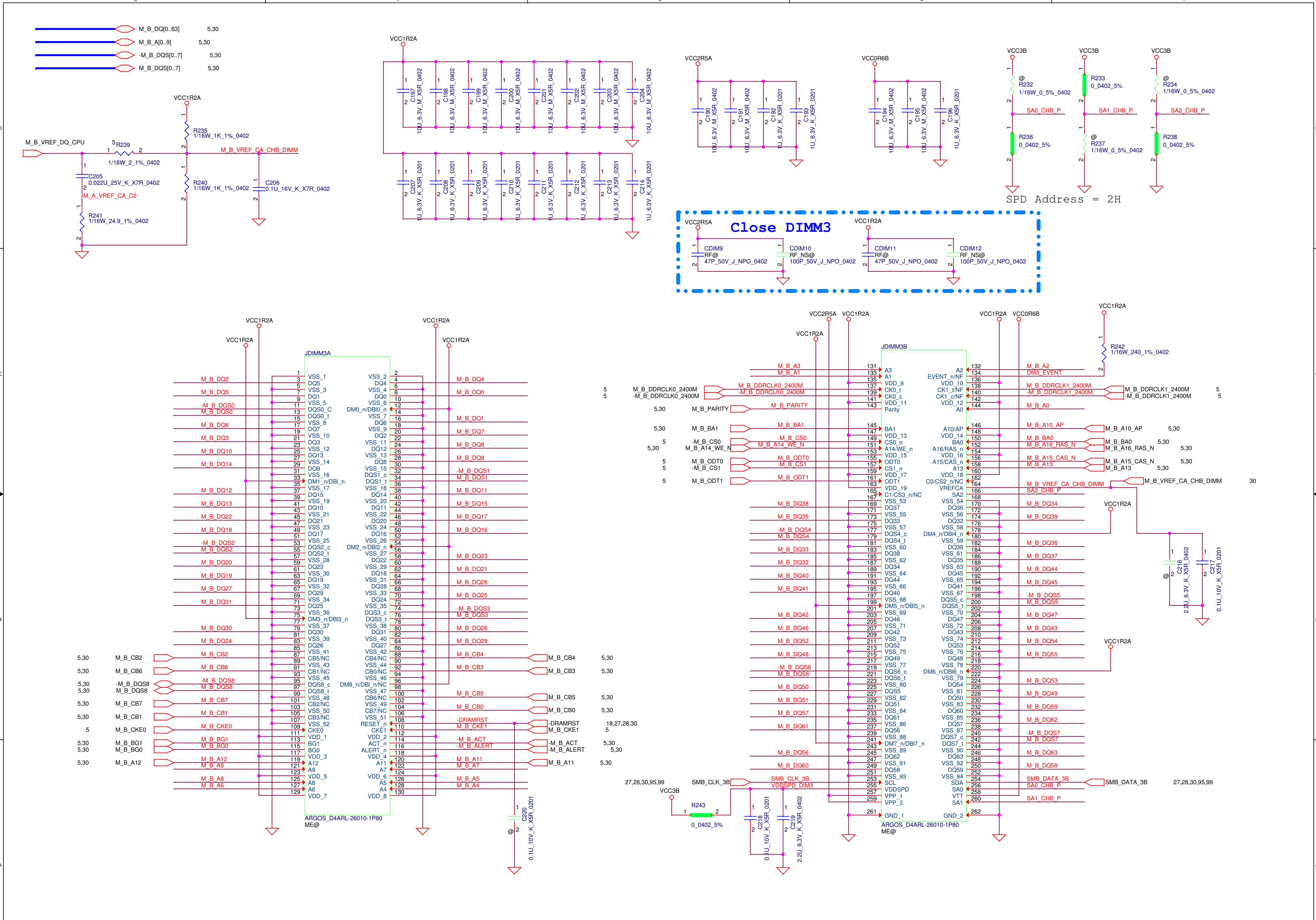
Project Name: Nighthawk-1

Rev 1.0

Title: DDR

Date: Monday, April 29, 2019

Sheet 28 of 142

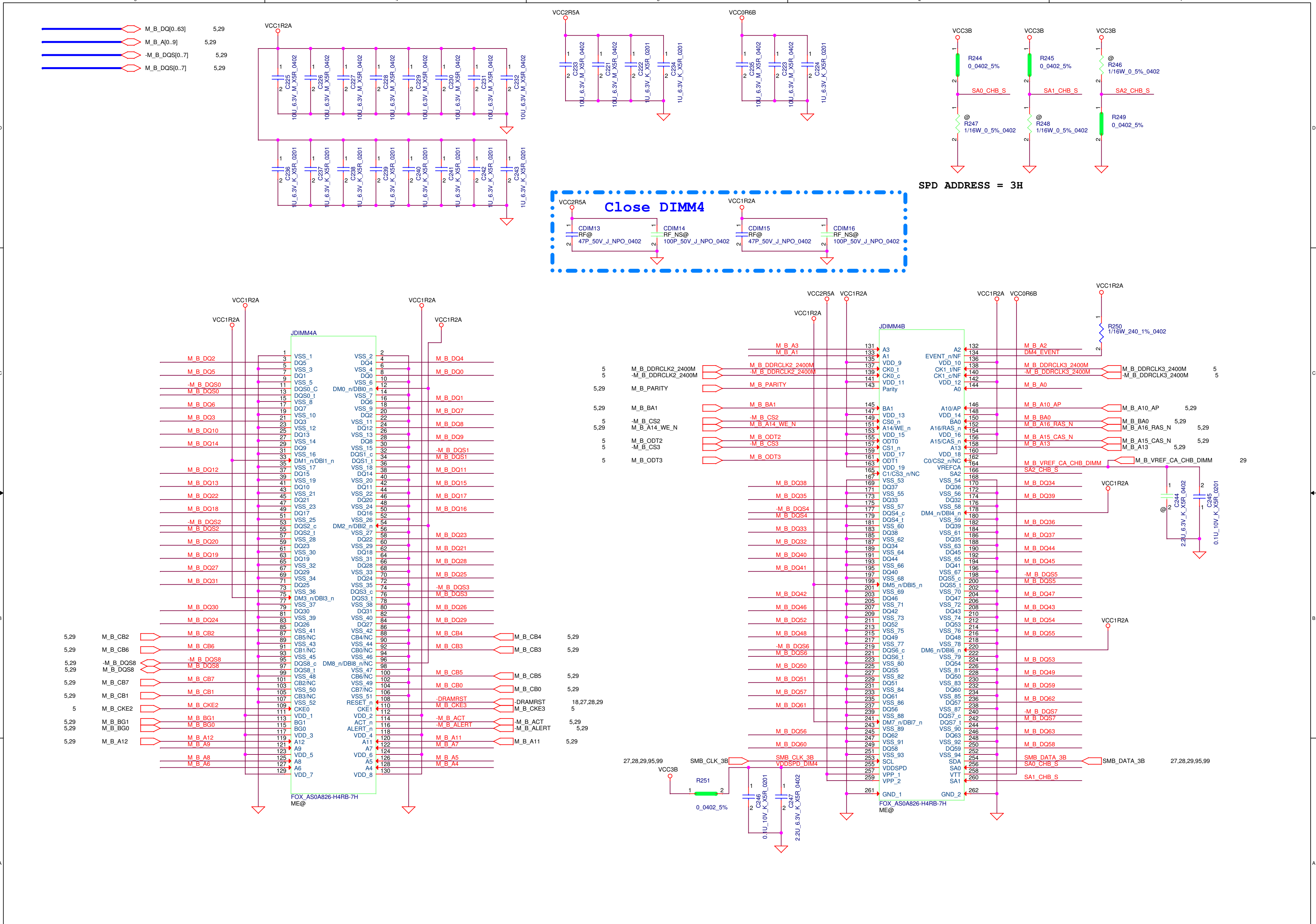


LC Future Center Secret Data

Project Name: **Nighthawk-1**

Rev 1.0 | Title: **DDR**

Date: Monday, April 29, 2019 | Sheet 29 of 142



LC Future Center Secret Data

Project Name: Nighthawk-1

Rev: 1.0

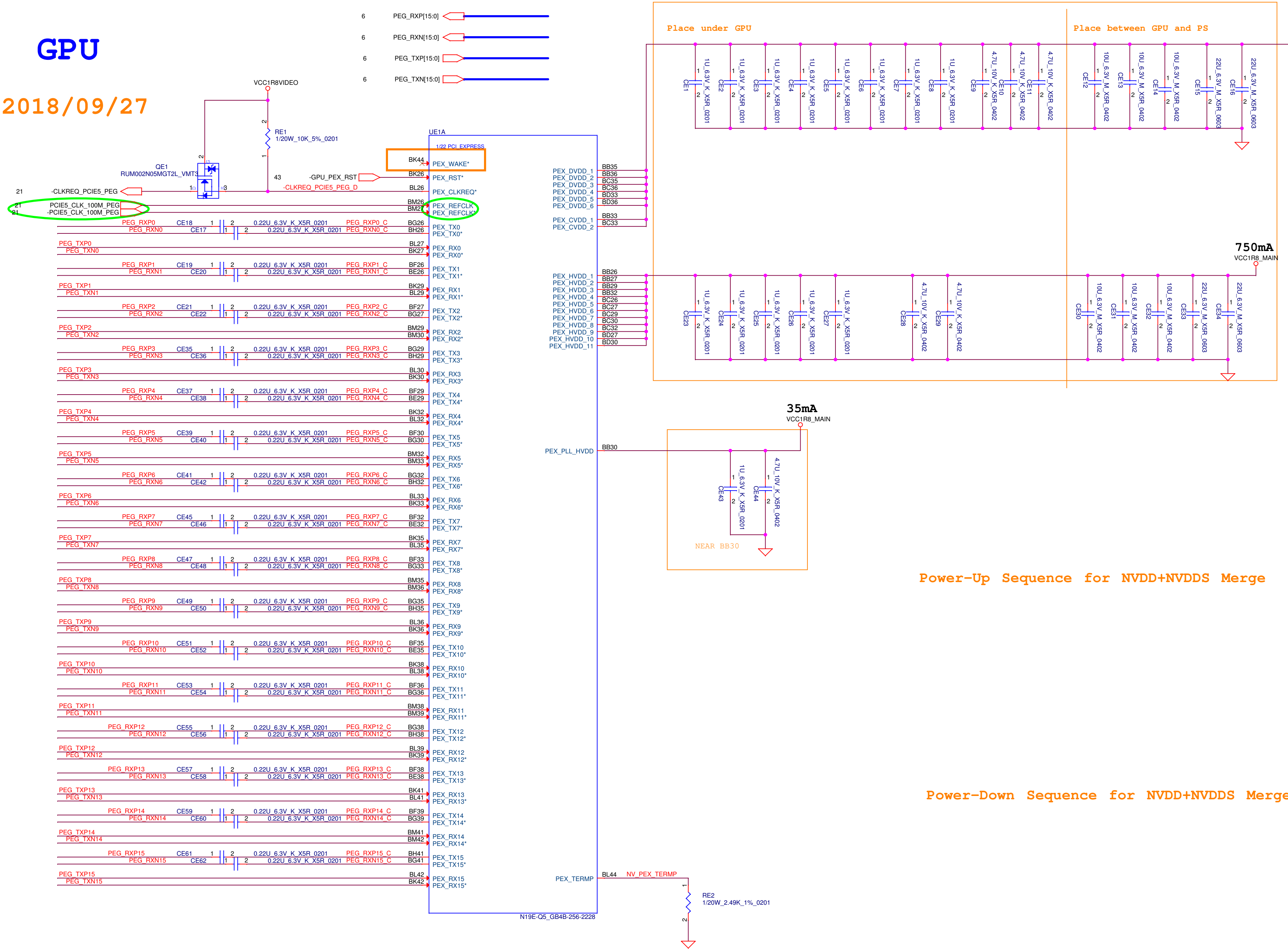
Title: DDR

Date: Monday, April 29, 2019

Sheet 30 of 142

GPU

2018/09/27

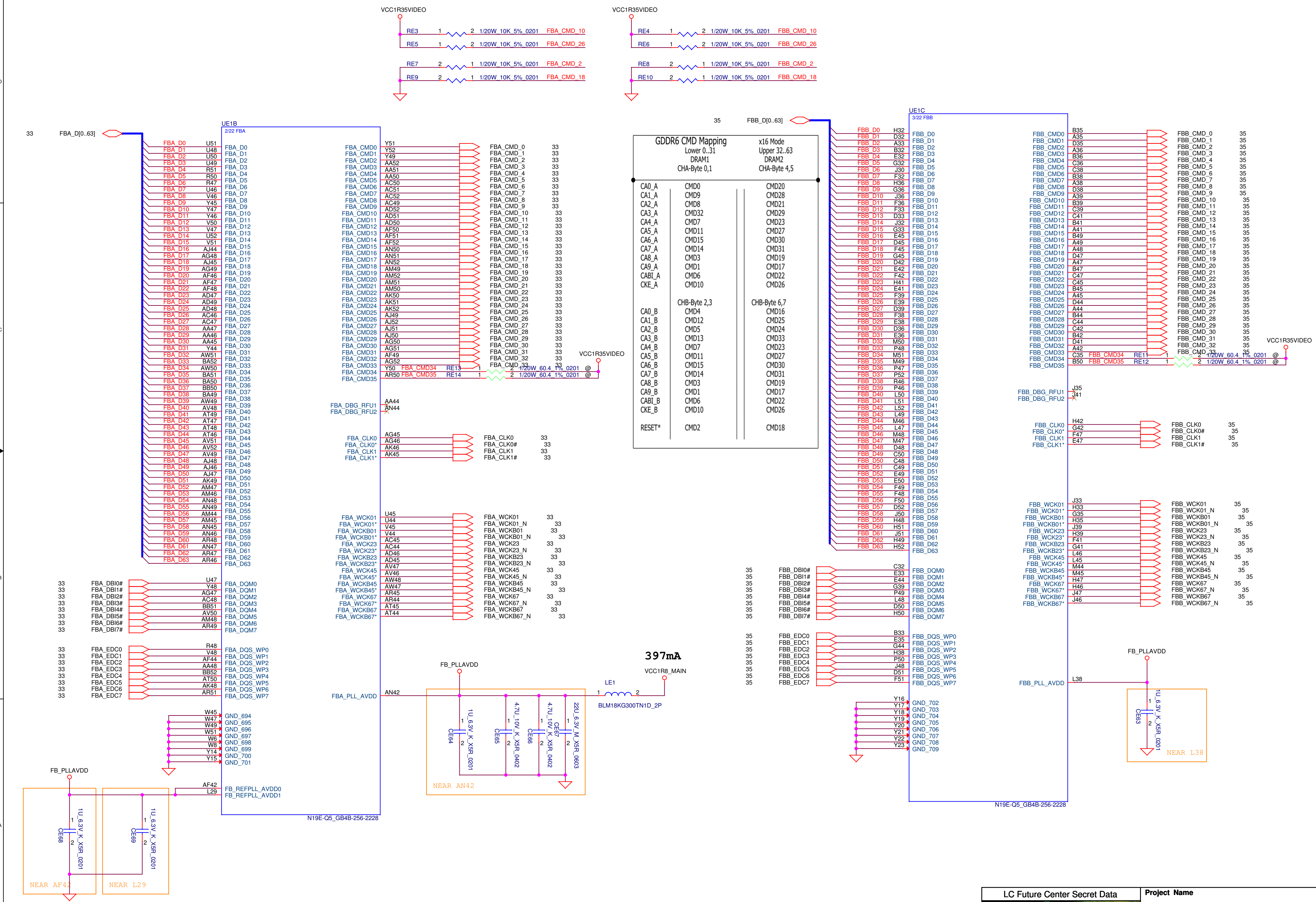


Power-Up Sequence for NVDD+NVDDS Merge

Power-Down Sequence for NVDD+NVDDS Merge

LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 — Title: N19E : PCI EXPREX
	Date: Monday, April 29, 2019 — Sheet 31 of 142

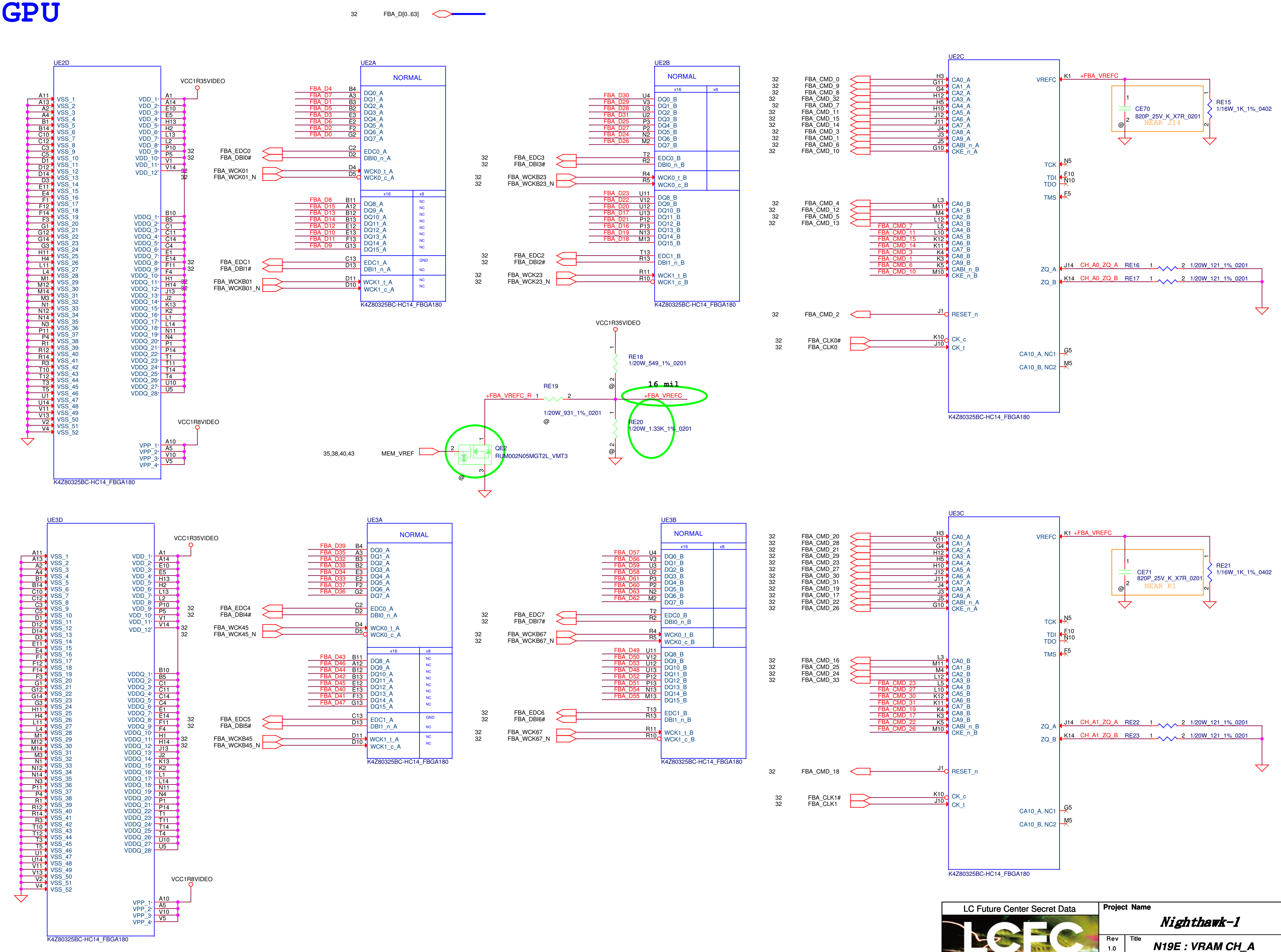
GPU



GDDR6 CMD Mapping

	x16 Mode Lower 0..31 DRAM1	Upper 32..63 DRAM2
	CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

GPU



LC Future Center Secret Data

LCFC

Project Name: Nighthawk-1

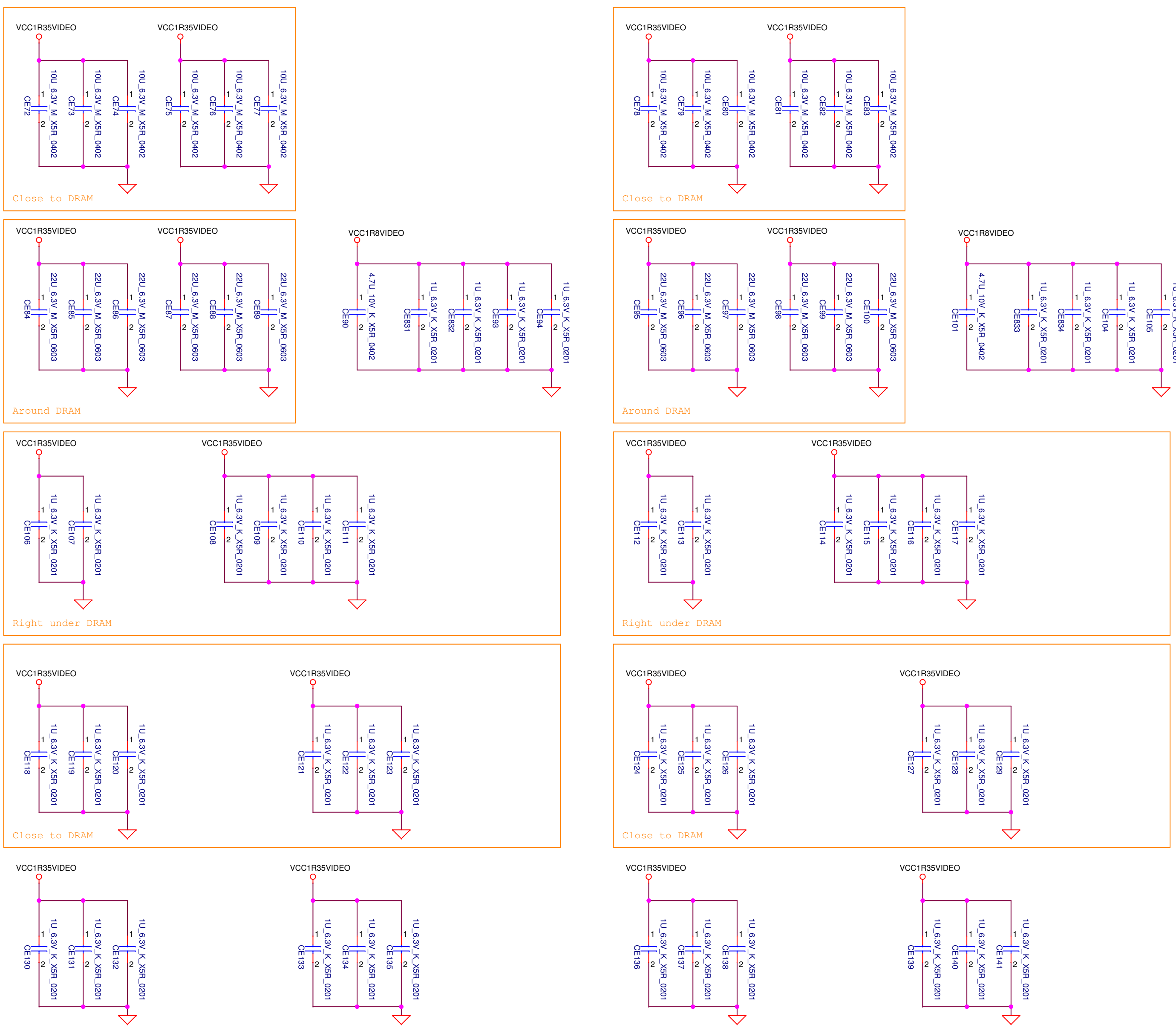
Rev 1.0

Title: N19E : VRAM CH_A

Date: Monday, April 29, 2019

Sheet 33 of 142

GPU



LC Future Center Secret Data

LCFC

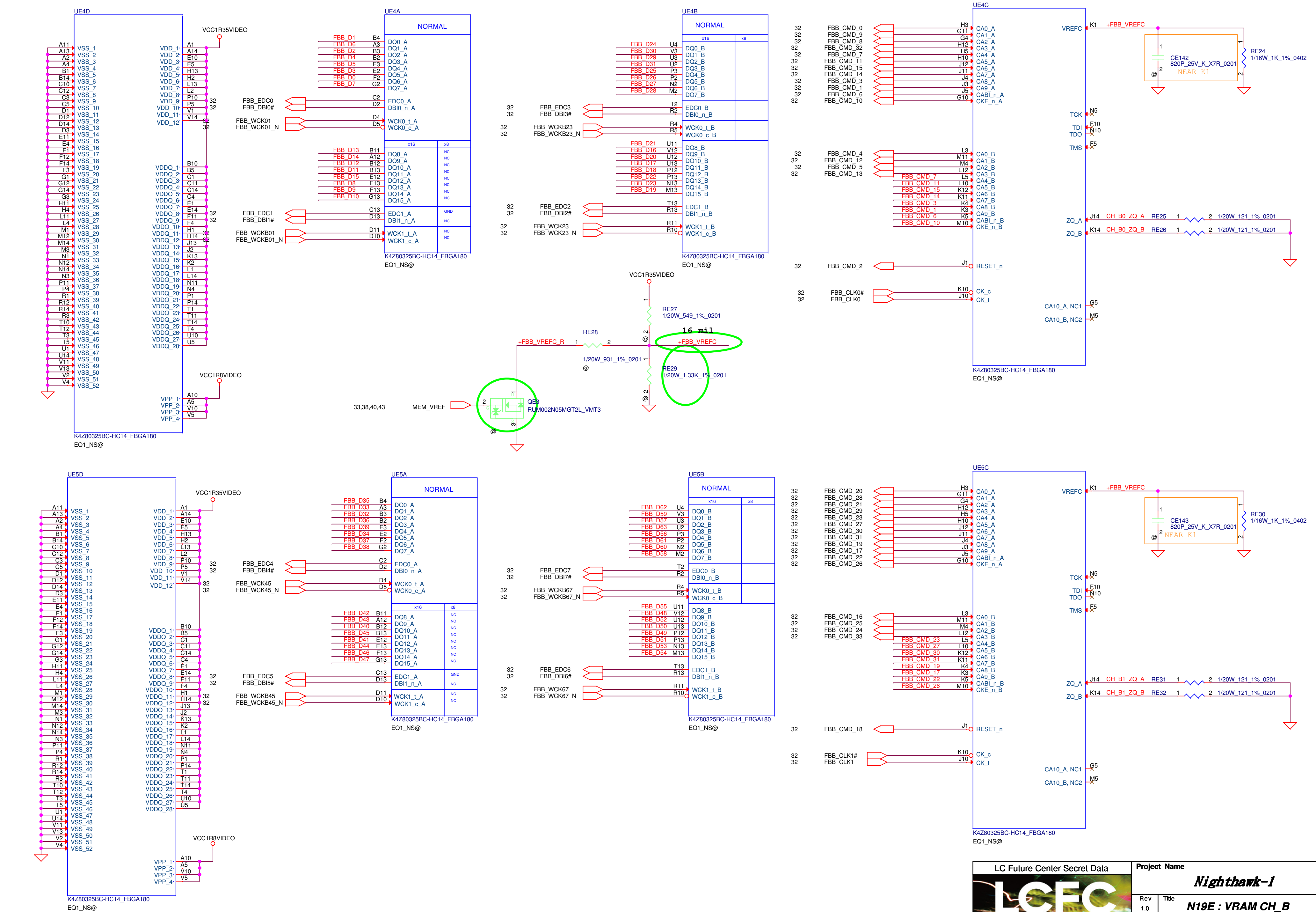
Project Name: Nighthawk-1

Rev: 1.0

Title: N19E : VRAM CH_A_CAP

Date: Monday, April 29, 2019

GPU



LC Future Center Secret Data

Project Name: *Nighthawk-1*

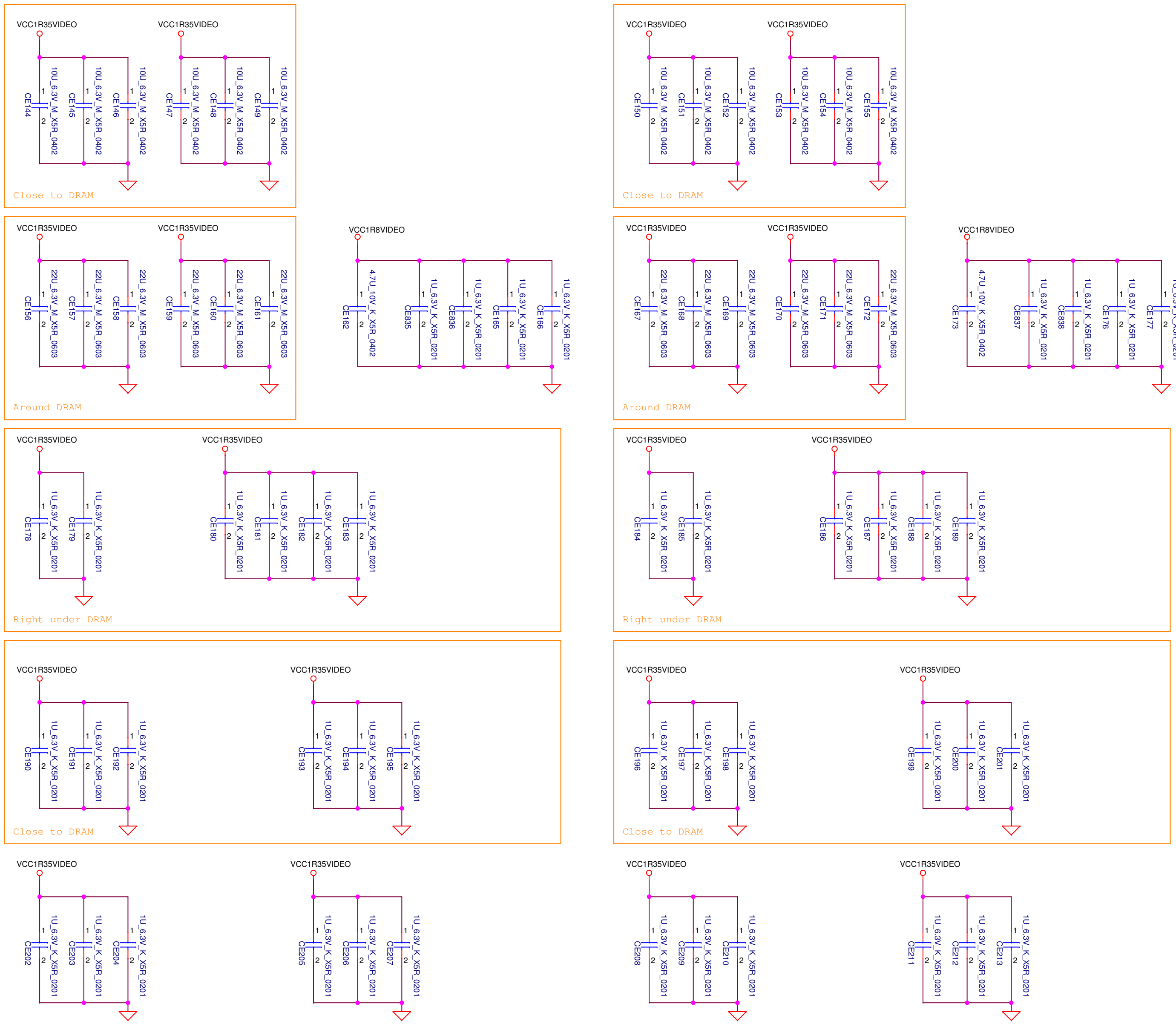
Rev 1.0

Title: N19E : VRAM CH_B

Date: Monday, April 29, 2019

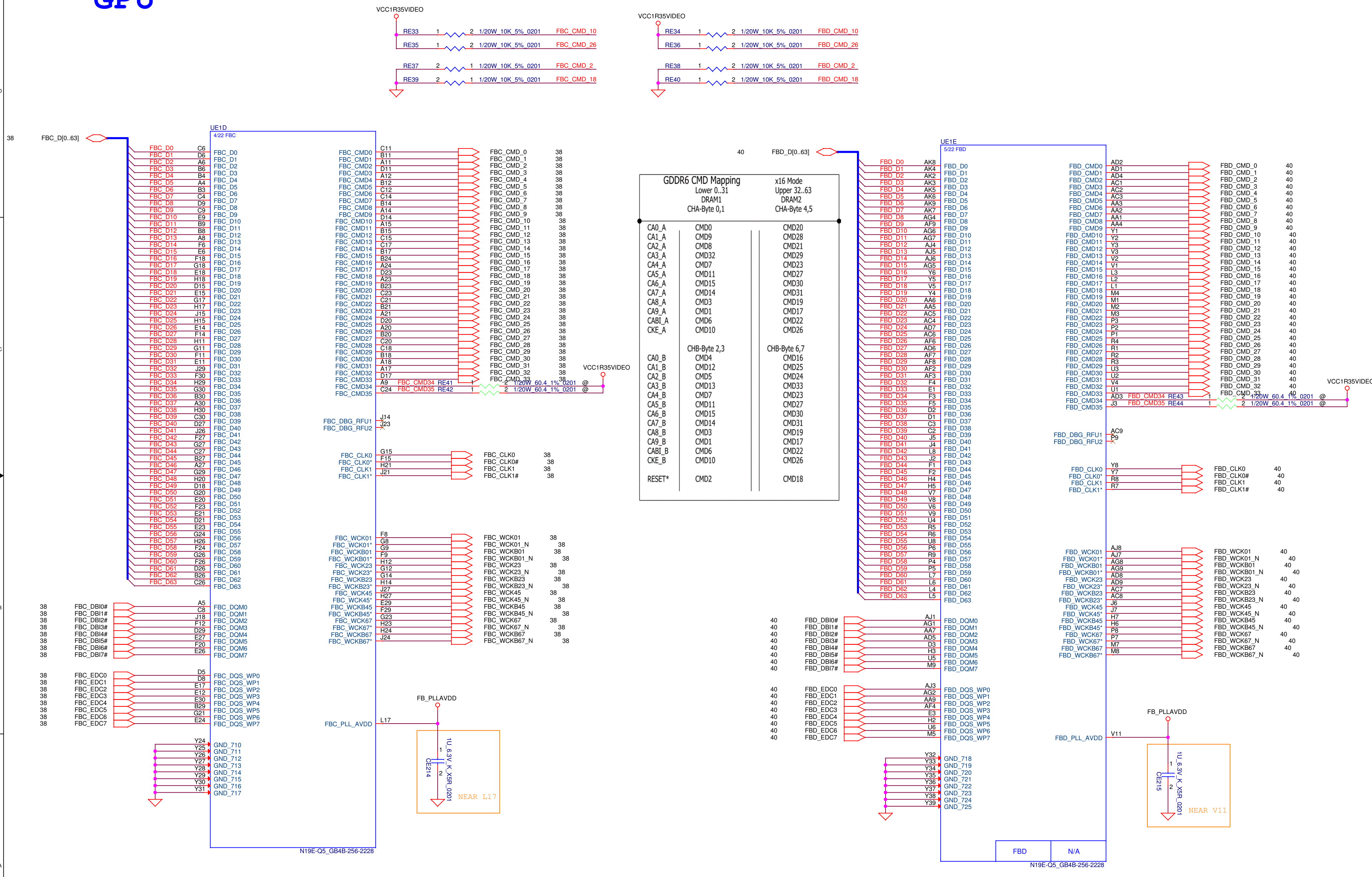
Sheet 35 of 142

GPU



LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 — Title: N19E : VRAM CH_B_CAP
	Date: Monday, April 29, 2019 — Sheet 36 of 142

GPU

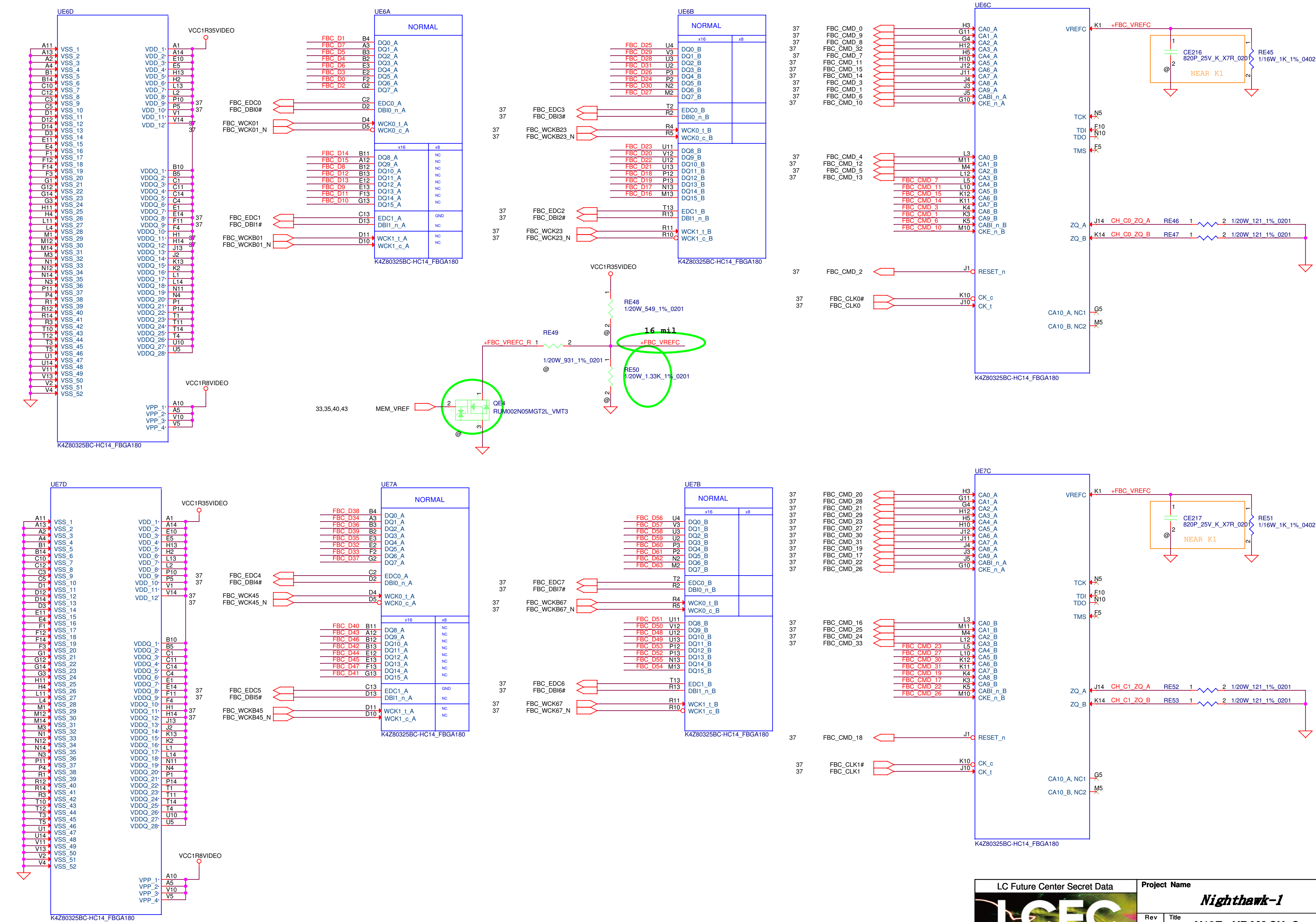


GDDR6 CMD Mapping — x16 Mode

	Lower 0..31 DRAM1 CHA-Byte 0,1	Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

GPU

37 FBC_D[0..63]



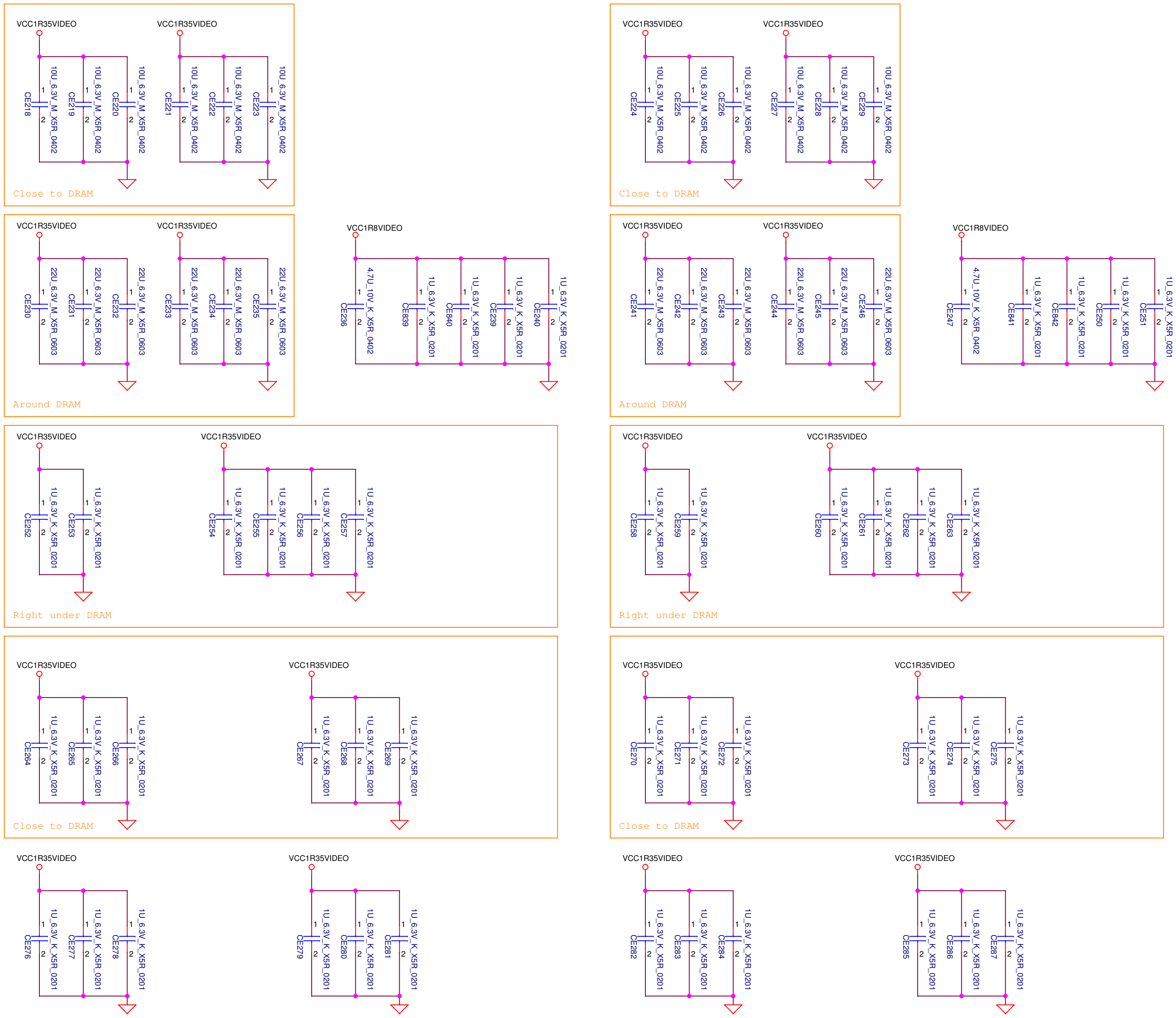
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0 | Title: N19E : VRAM CH_C

Date: Monday, April 29, 2019 | Sheet 38 of 142

GPU



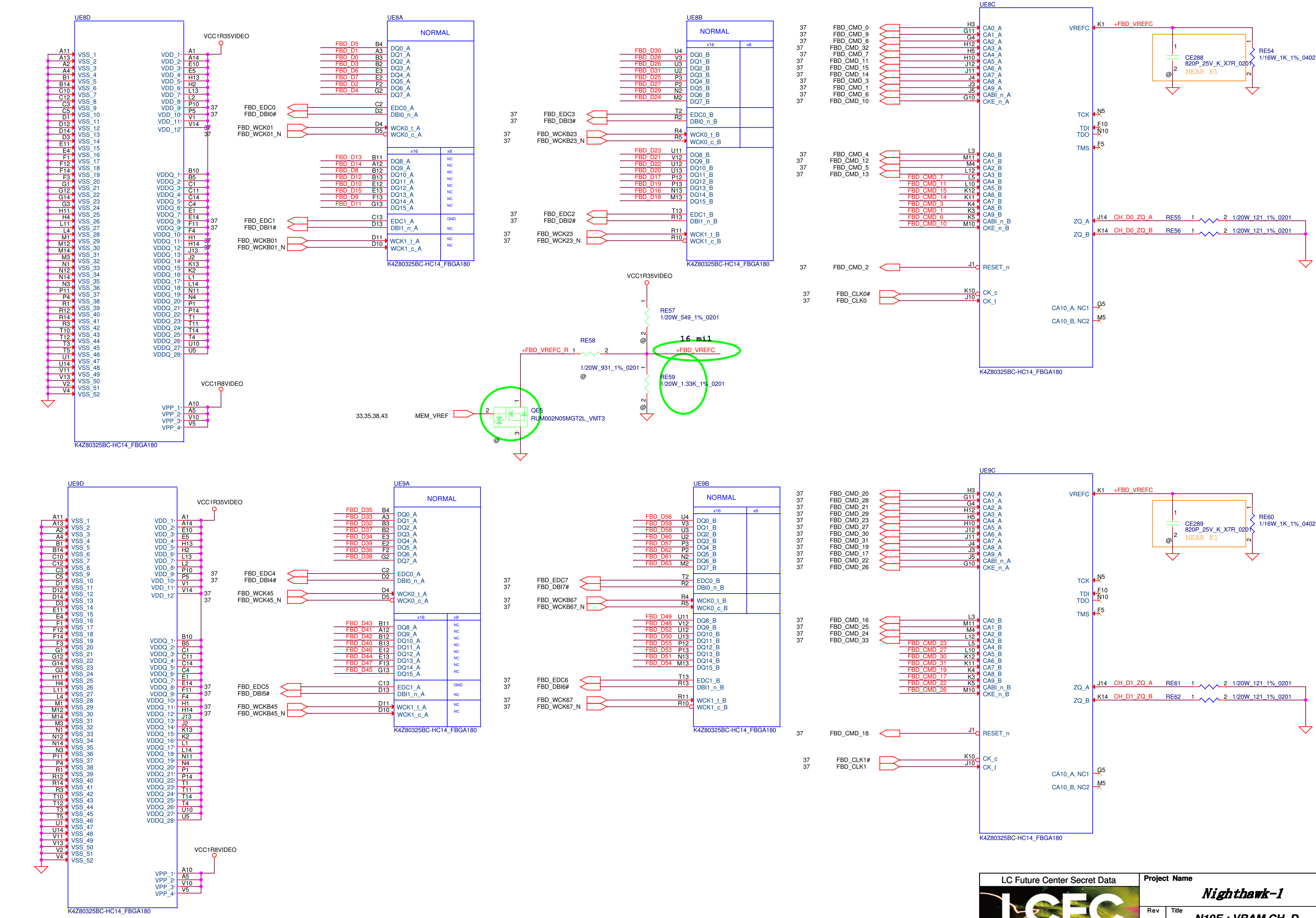
LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev 1.0 | Title: **N19E : VRAM CH_C_CAP**

Date: Monday, April 29, 2019 | Sheet 39 of 142

GPU



LC Future Center Secret Data

Project Name: Nighthawk-1

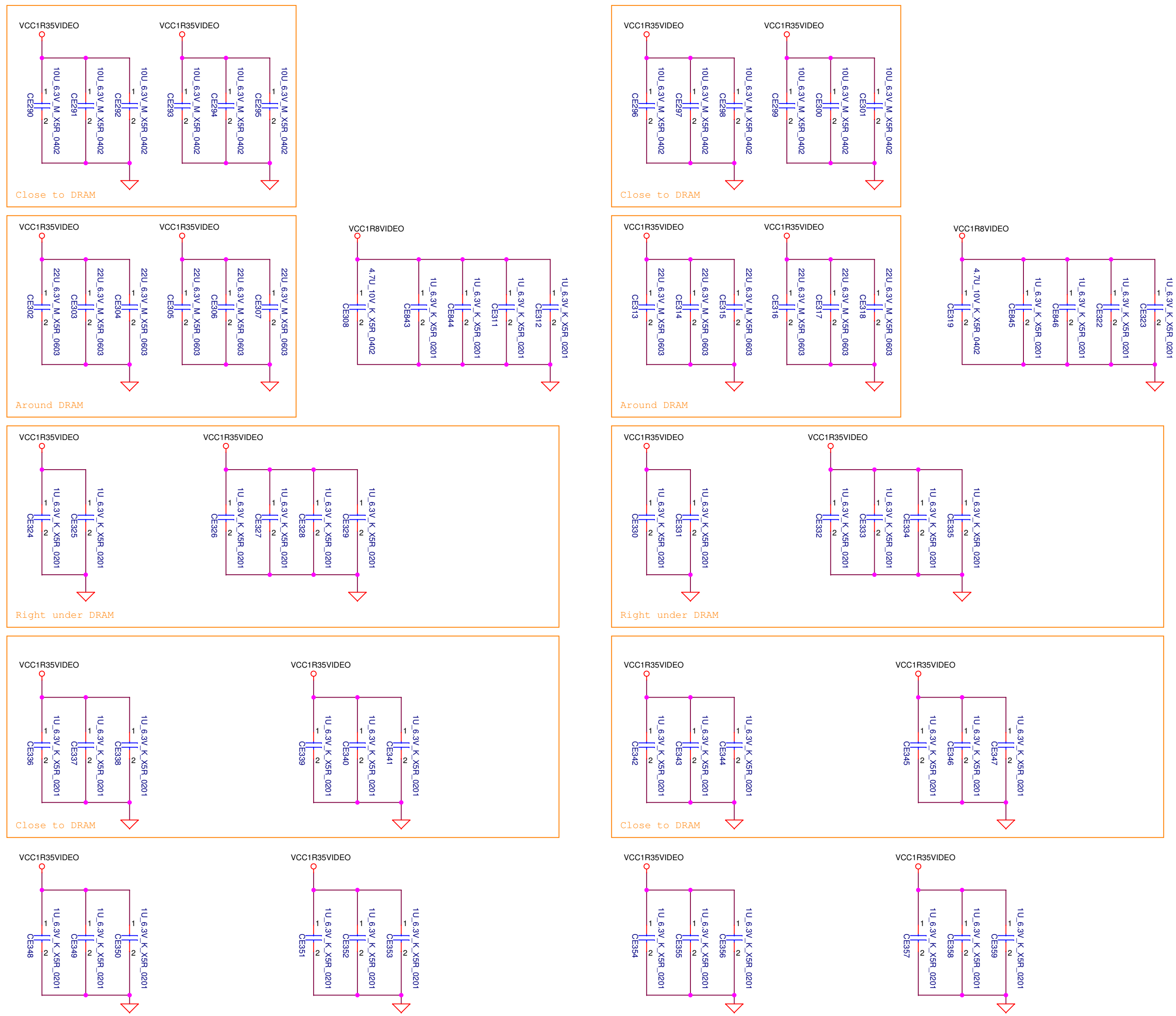
Rev 1.0

Title: N19E : VRAM CH_D

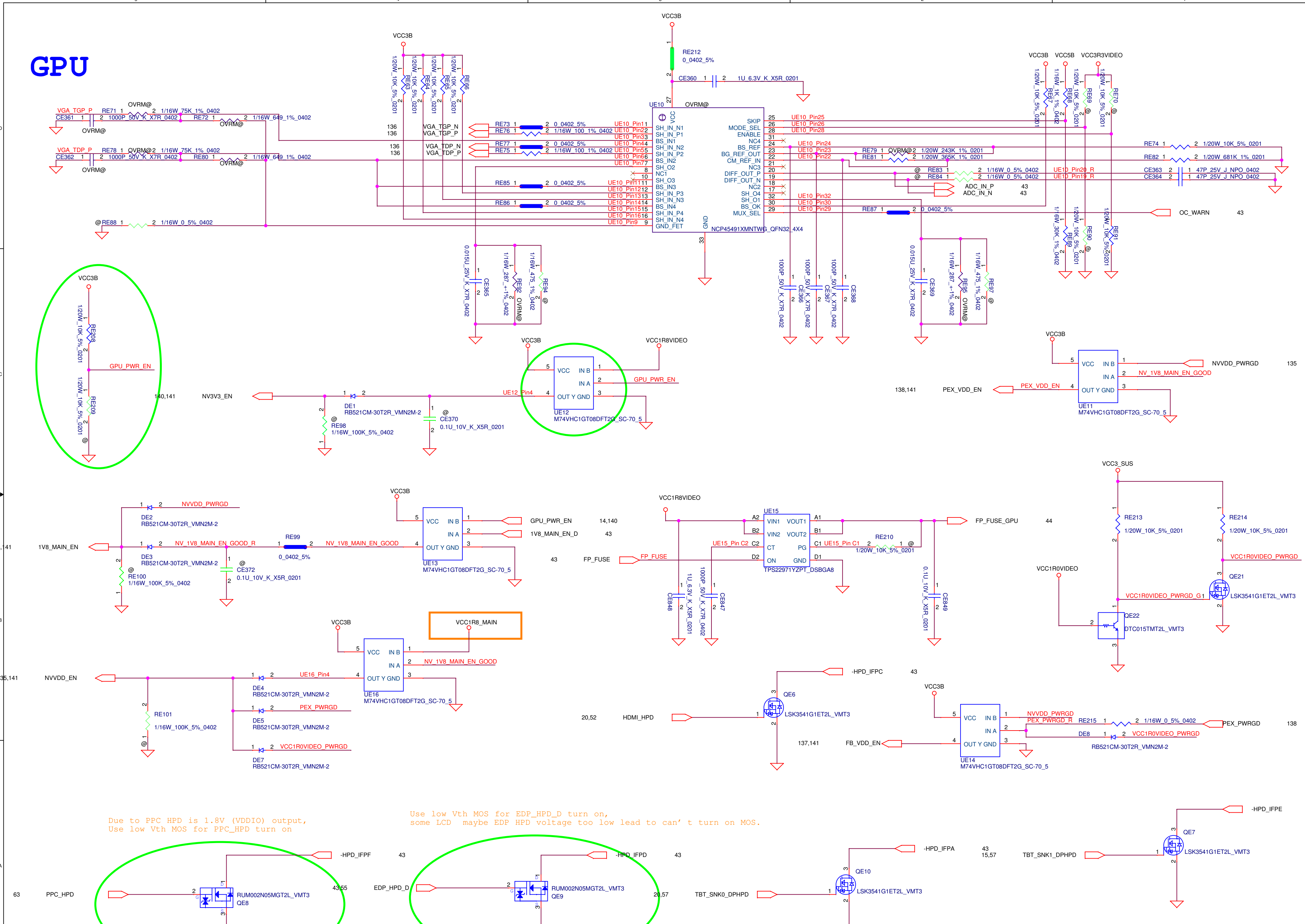
Date: Monday, April 29, 2019

Sheet 40 of 142

GPU



LC Future Center Secret Data	Project Name	*Nighthawk-1*
	Rev 1.0	Title: **N19E : VRAM CH_D_CAP**
	Date: Monday, April 29, 2019	Sheet 41 of 142



LC Future Center Secret Data

LCFC

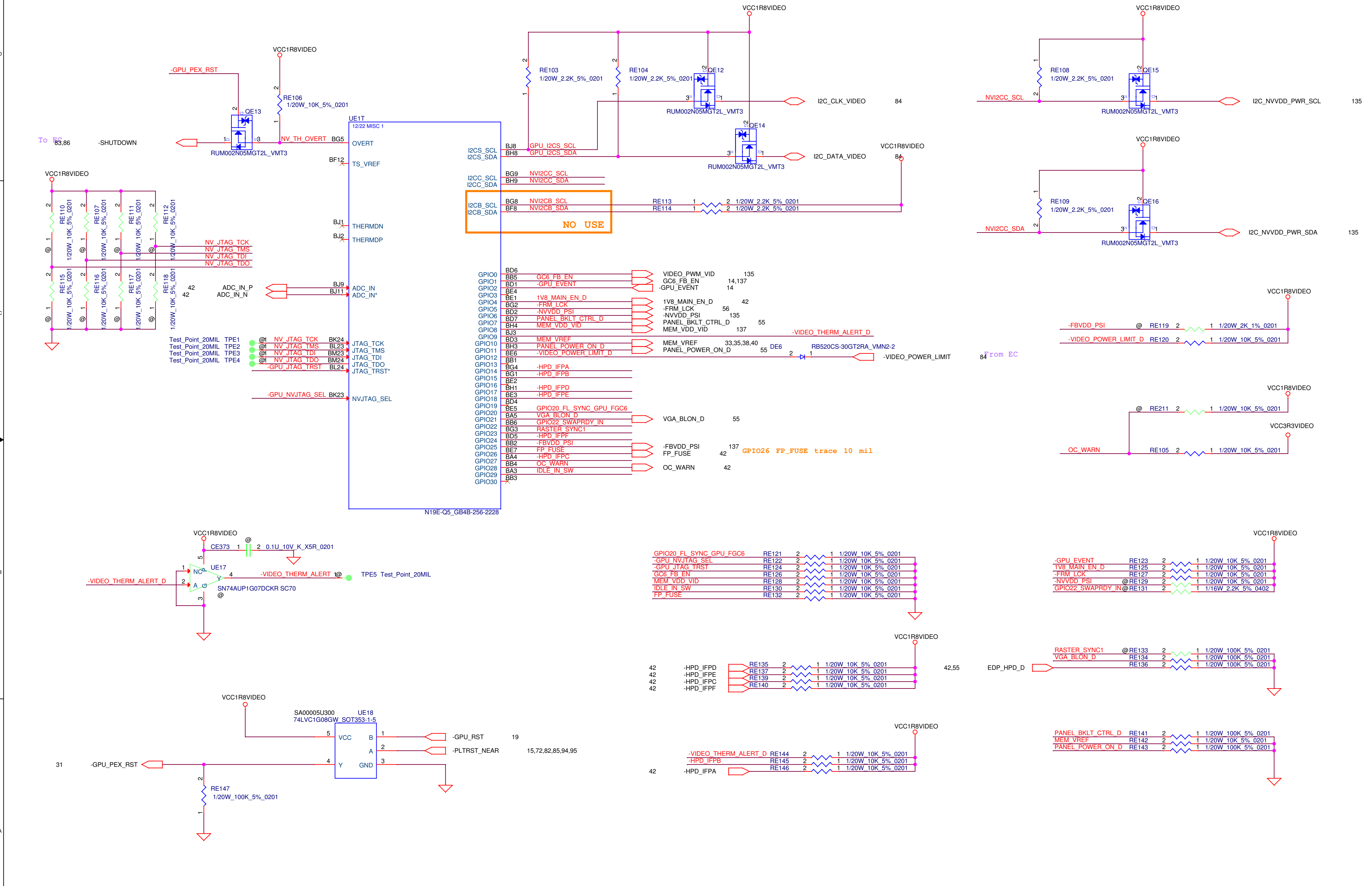
Project Name: Nighthawk-1

Rev 1.0

Title: N19E : NCP45491

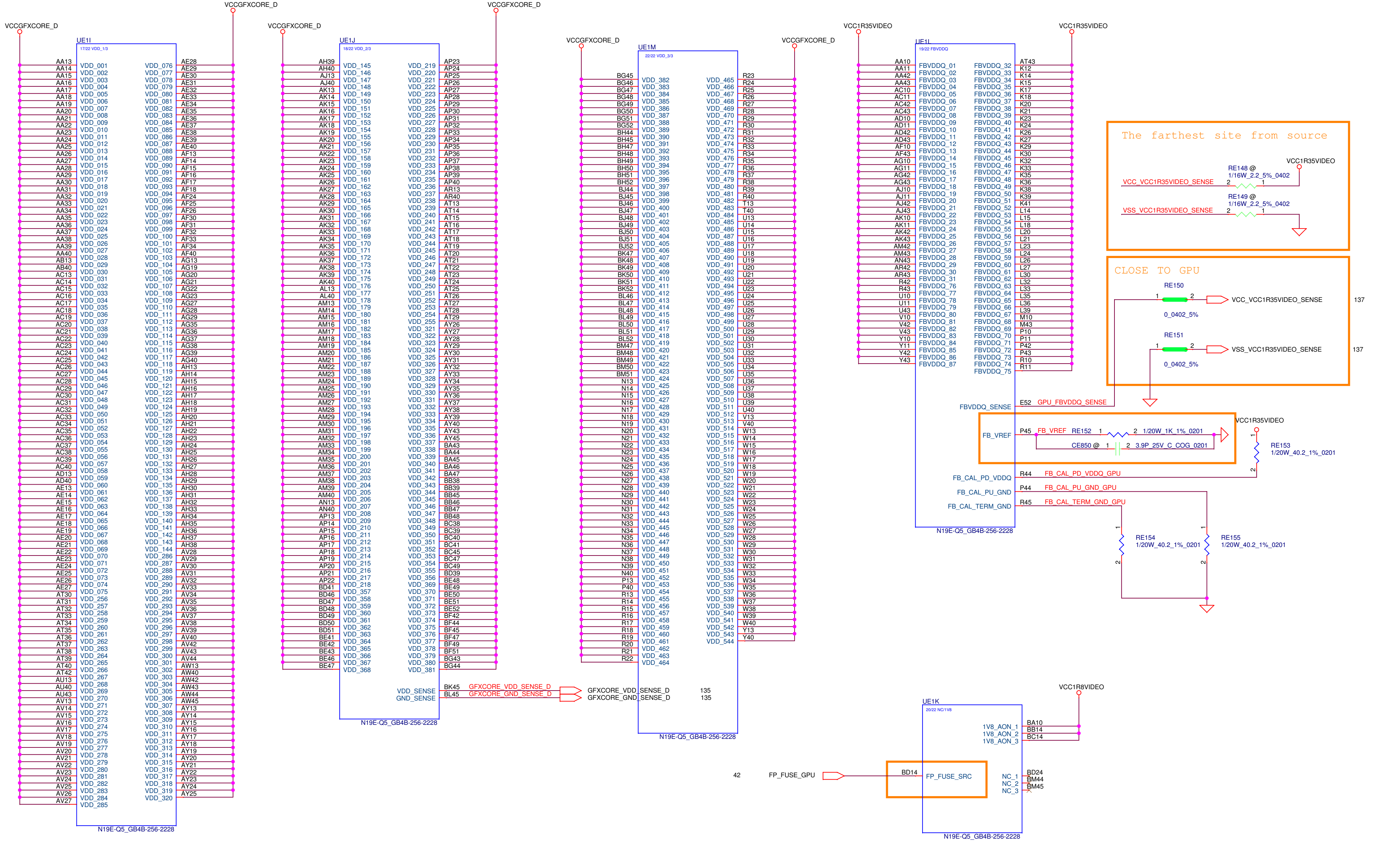
Date: Monday, April 29, 2019 Sheet 42 of 142

GPU



LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 · Title: N19E : GPIO and I2C
	Date: Monday, April 29, 2019 · Sheet 43 of 142

GPU



LC Future Center Secret Data

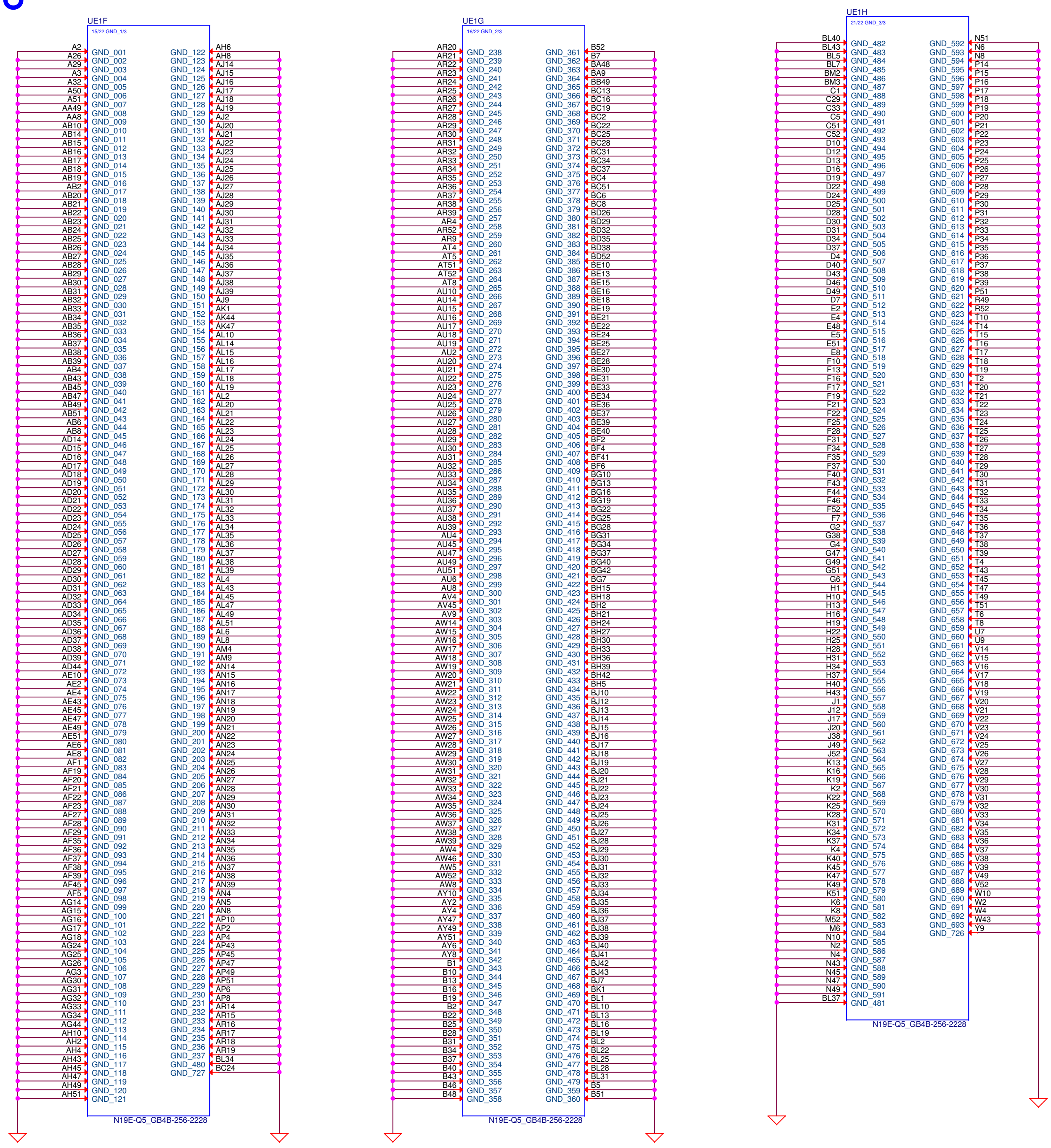
Project Name: *Nighthawk-1*

Rev 1.0

Title: N19E : POWER

Date: Monday, April 29, 2019 | Sheet 44 of 142

GPU

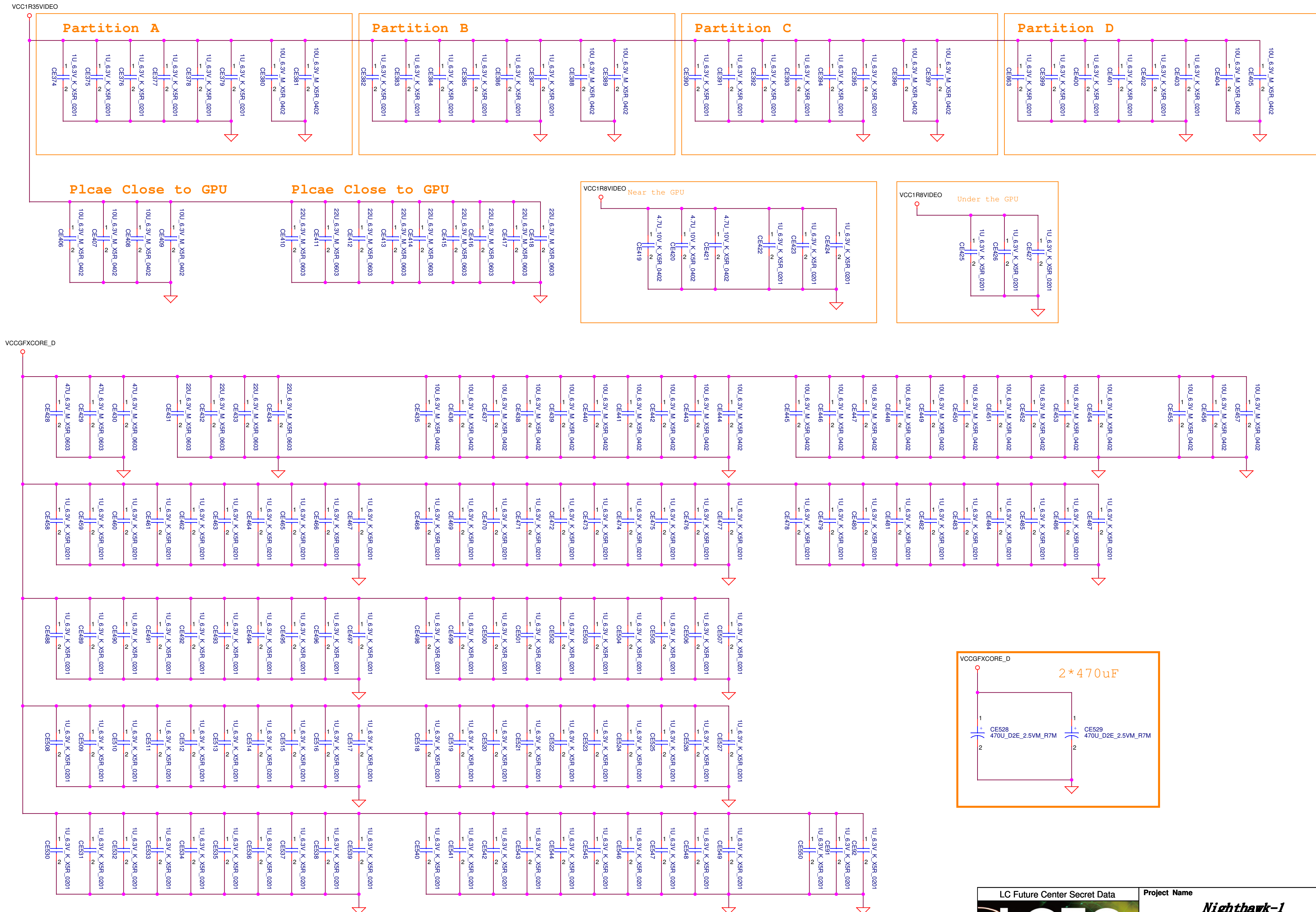


LC Future Center Secret Data

Project Name *Nighthawk-1*

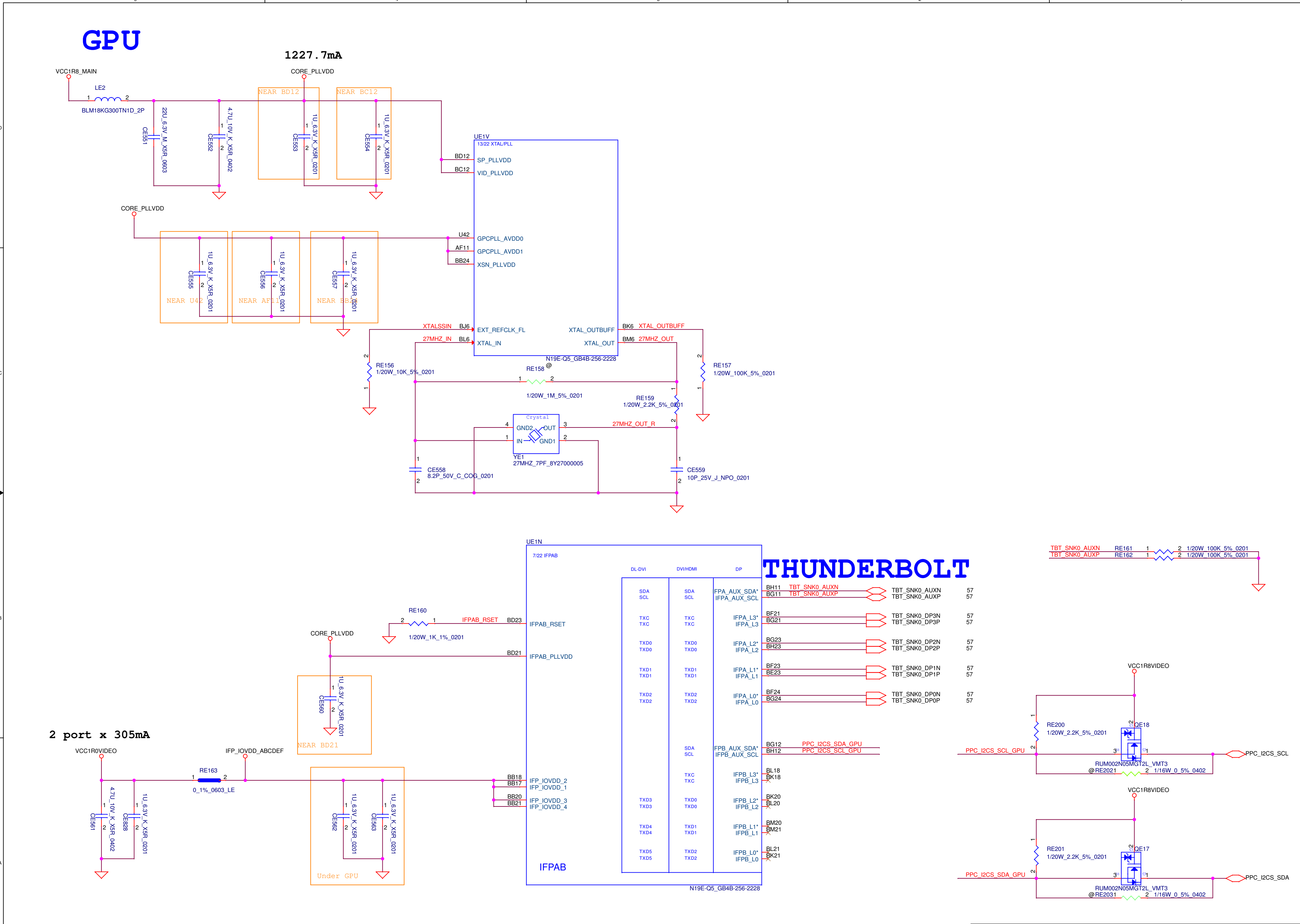
Rev	Title
1.0	N19E : GND

GPU


VCC1R35VIDEO
Partition A
Partition B
Partition C
Partition D
Plcae Close to GPU
Plcae Close to GPU
VCC1R8VIDEO
Near the GPU
VCC1R8VIDEO
Under the GPU
VCCGFXCORE_D
VCCGFXCORE_D
2*470uF
CE528
470U_D2E_2.5VM_R7M
CE529
470U_D2E_2.5VM_R7M

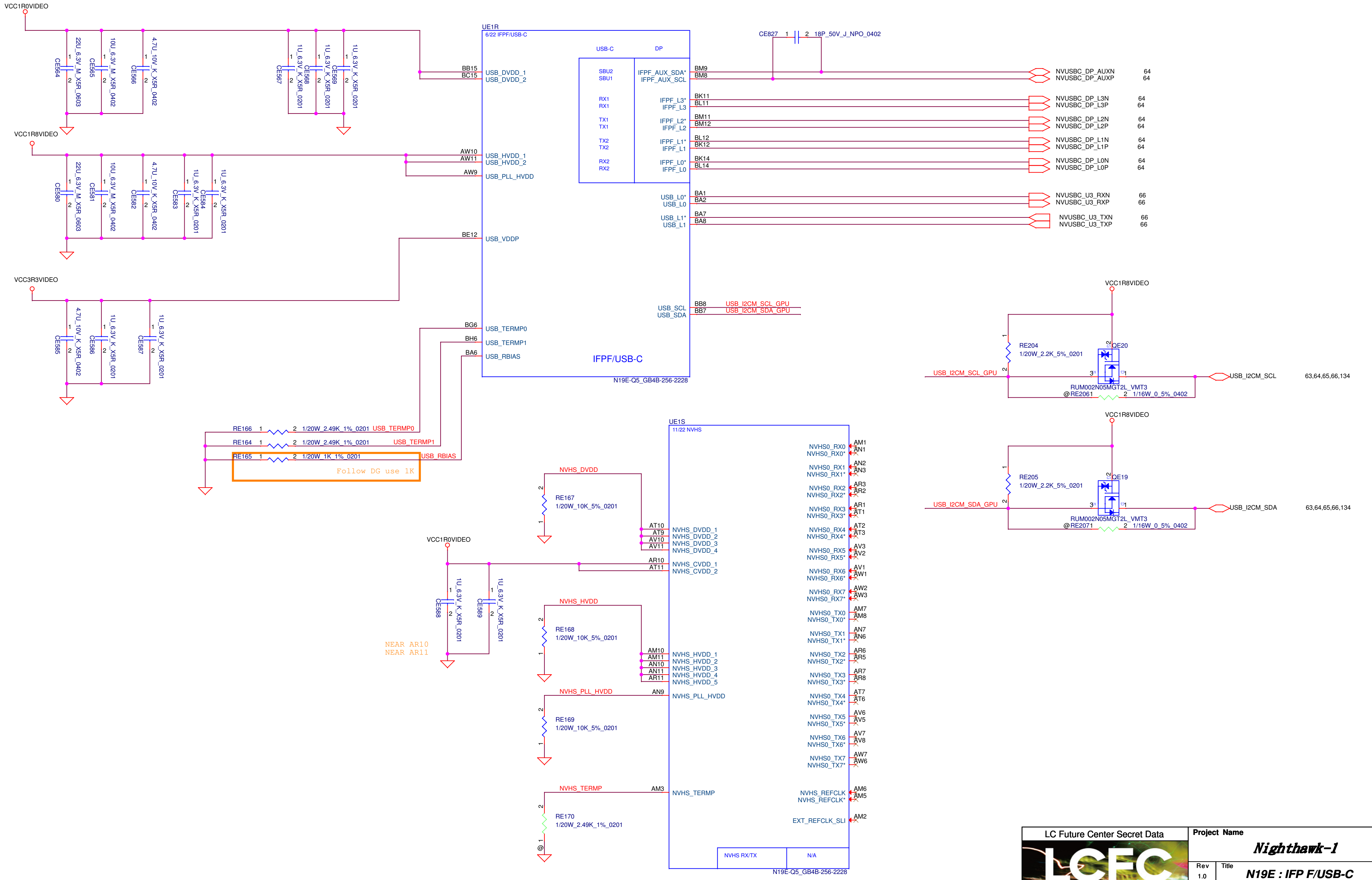
GPU

EMPTY



LC Future Center Secret Data	Project Name	Nighthawk-1
LCFC	Rev 1.0	Title: N19E : IFP A/B and XTAL
	Date: Monday, April 29, 2019	Sheet 48 of 142

GPU



LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0

Title: N19E : IFP F/USB-C

Date: Monday, April 29, 2019

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GPU

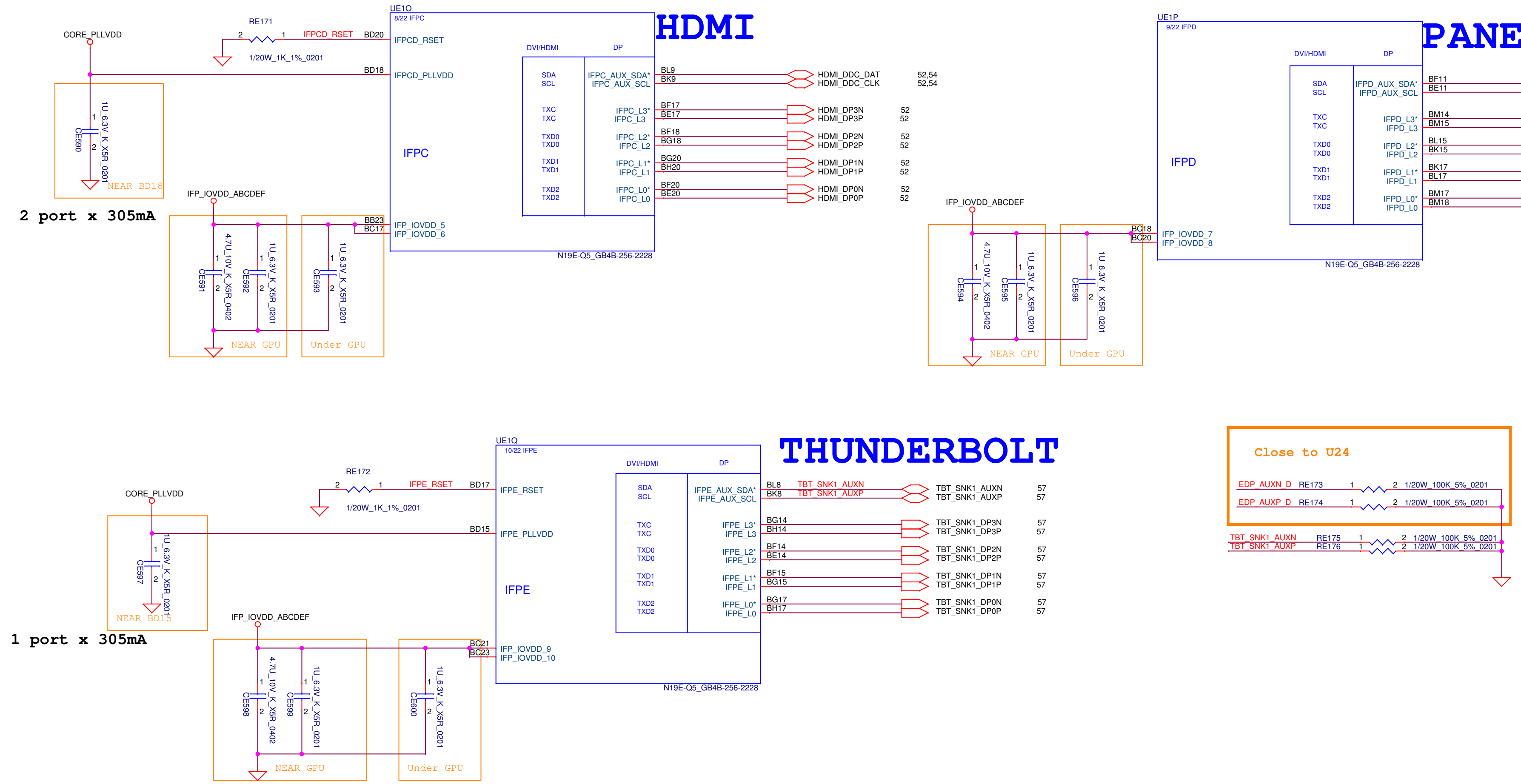


Table 10.1 Digital Display Link Summary

Digital Display Link	Dual-Link DVI	HDMI	DisplayPort
IFPA (Link A)	✓(Dual Link with IFPB)	✓	✓
IFPB (Link B)	✓(Dual Link with IFPA)	✓	✓
IFPC (Link C)	✓(Dual Link with IFPD)	✓	✓
IFPD (Link D)	(not supported)	(not supported)	eDP Only (no ext. display)
IFPE (Link E)	✓(Dual Link with IFPF)	✓	✓
IFPF (Link F)	✓(Dual Link with IFPE)	✓	✓

GPU

Strap table				STRAP 0		STRAP 1		STRAP 2	
				STRAP0_H@	STRAP0_L@	STRAP1_H@	STRAP1_L@	STRAP2_H@	STRAP2_L@
GPU	Vendor	DIE Rev	Strap	RE177	RE187	RE178	RE188	RE179	RE189
N19E-Q5	Samsung	M	0x6	NO ASM	ASM	ASM	NO ASM	ASM	NO ASM
N19E-Q3	Micron	A	0x1	ASM	NO ASM	NO ASM	ASM	NO ASM	ASM
N19E-Q1	Samsung	C	0x0	NO ASM	ASM	NO ASM	ASM	NO ASM	ASM

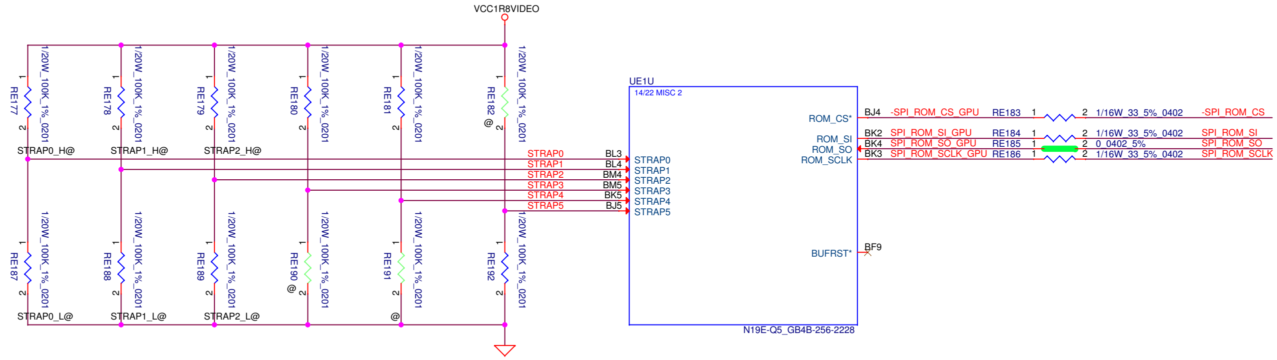
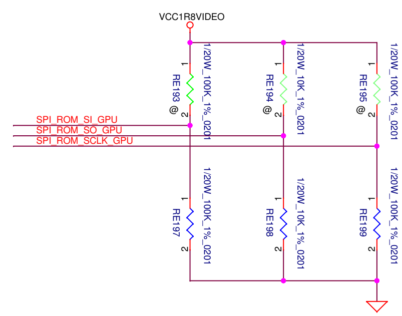
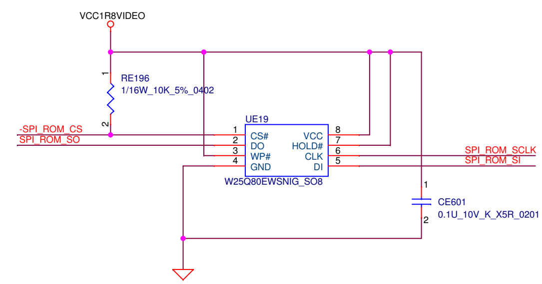


Table 5.3 RAMCFG

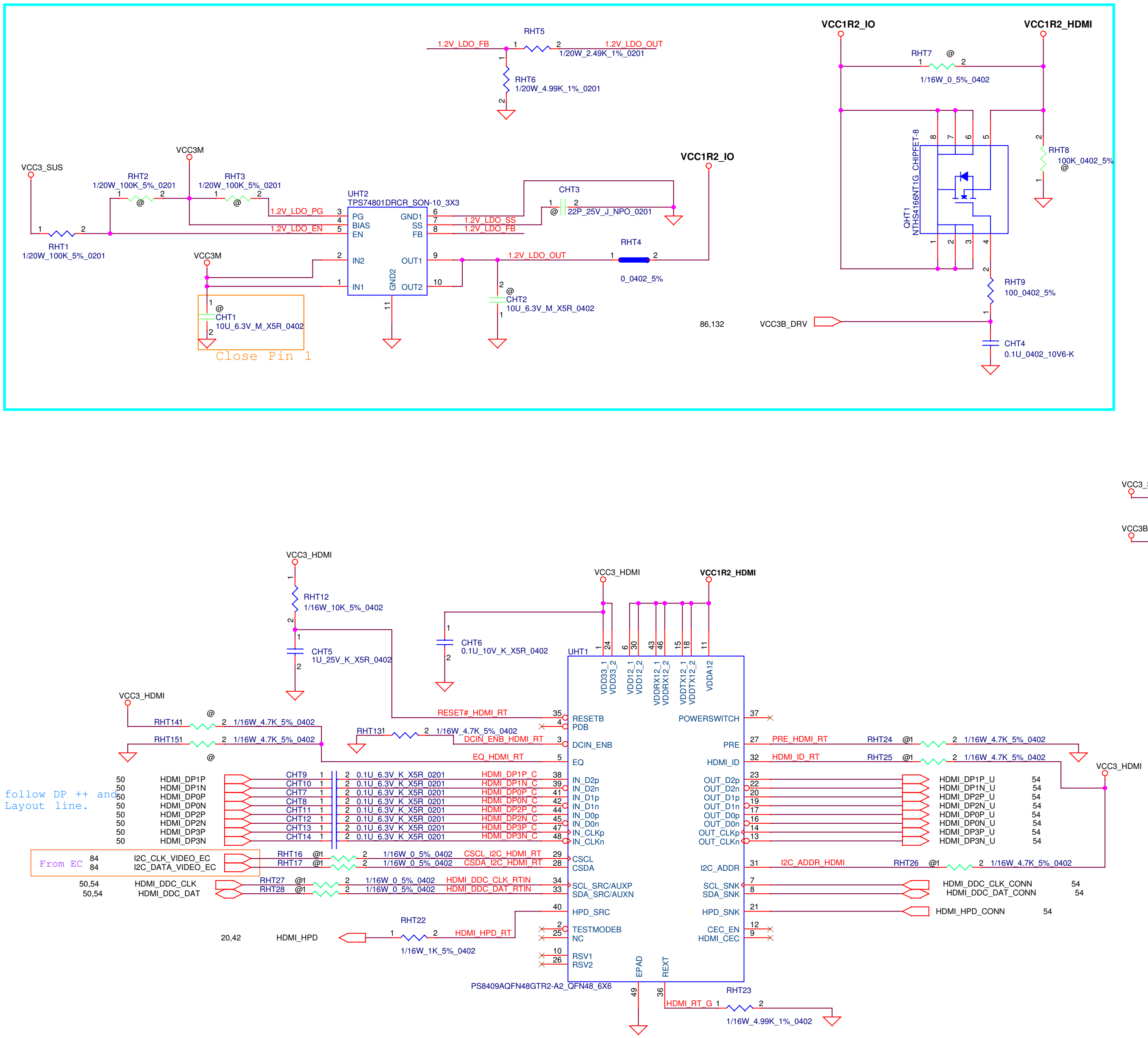
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Note: The ternary strap pins listed in the STRAP columns must be pulled to one of three voltage levels. "L" means Low level (GND). "M" means middle level (0.9V). "H" means High level (1.8V).





HDMI Re-Timer



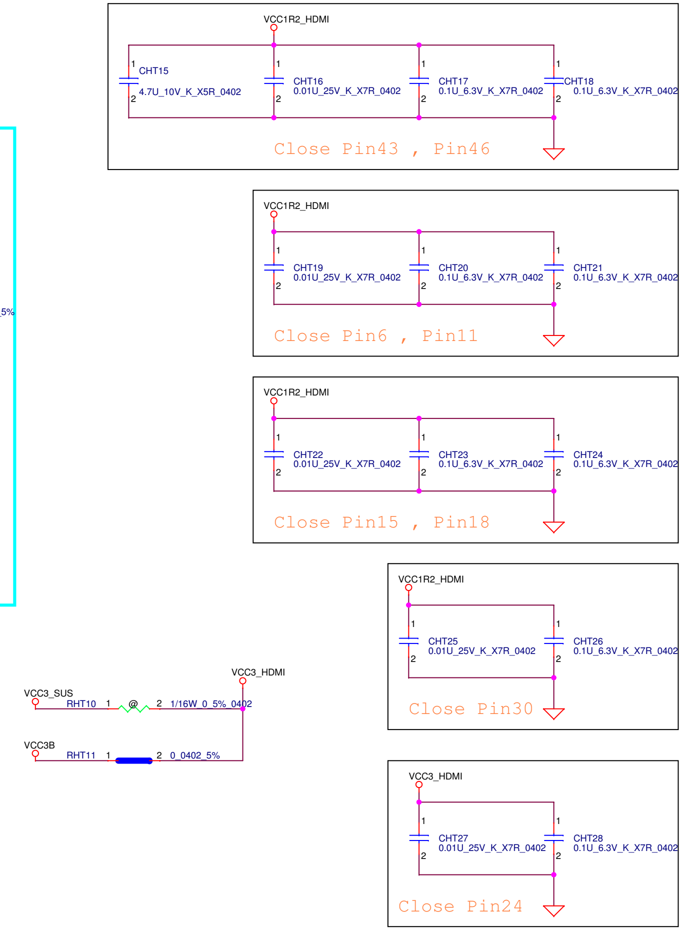


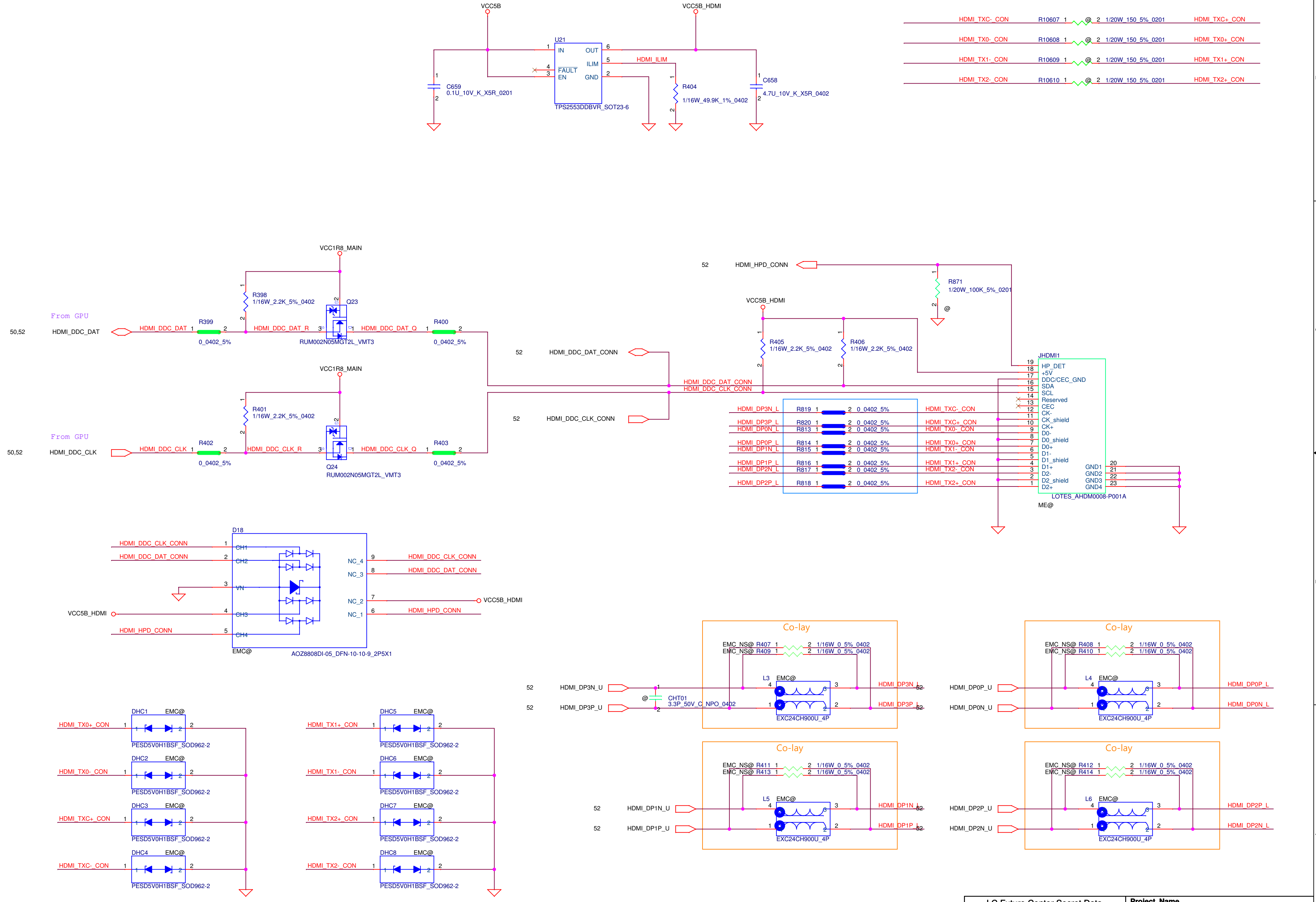
Table 9.12 Display Connector with DVI/HDMI Dongle Support

DP Connector Pin	DisplayPort Signal	DVI/HDMI Signal
1	Main Link Lane 0 +	TX Data 2 +
2	GND	GND
3	Main Link Lane 0 -	TX Data 2 -
4	Main Link Lane 1 +	TX Data 1 +
5	GND	GND
6	Main Link Lane 1 -	TX Data 1 -
7	Main Link Lane 2 +	TX Data 0 +
8	GND	GND
9	Main Link Lane 2 -	TX Data 0 -
10	Main Link Lane 3 +	Clock +
11	GND	GND
12	Main Link Lane 3 -	Clock -
13	CONFIG1 (Connected to GND)	DP_MODE
14	CONFIG1 (Connected to GND)	CEC
15	AUX CH +	SCL (DDC Clock)
16	GND	GND
17	AUX CH -	SDA (DDC Data)
18	Hot Plug Detect	Hot Plug Detect
19	GND Return	GND Return
20	PWR (3.3V)	PWR (3.3V)

HDMI LSPCON

BLANK

HDMI



LC Future Center Secret Data

LCFC

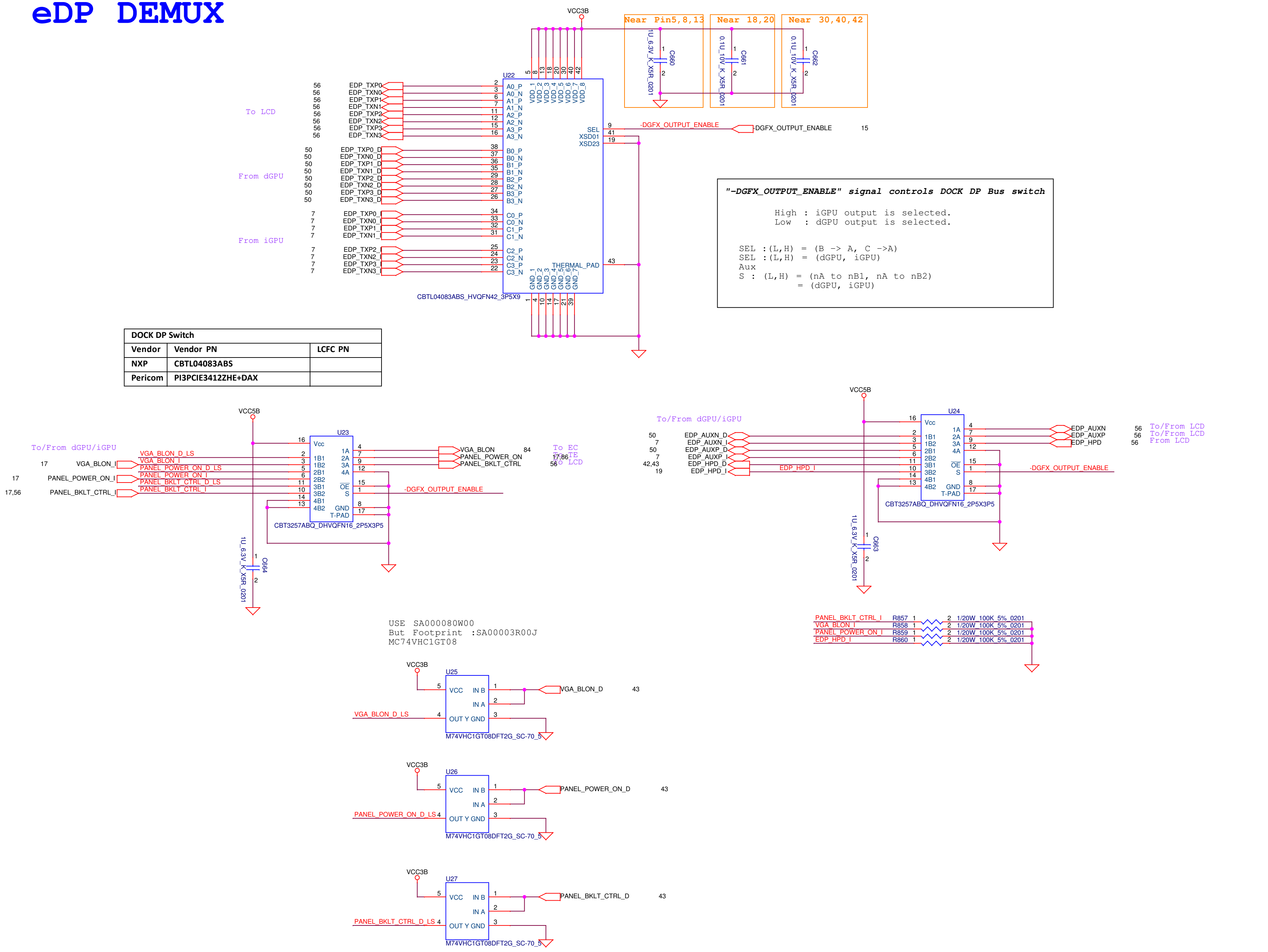
Project Name: *Nighthawk-1*

Rev: 1.0

Title: **HDMI CONNECTOR**

Date: Monday, April 29, 2019 | Sheet 54 of 142

eDP DEMUX



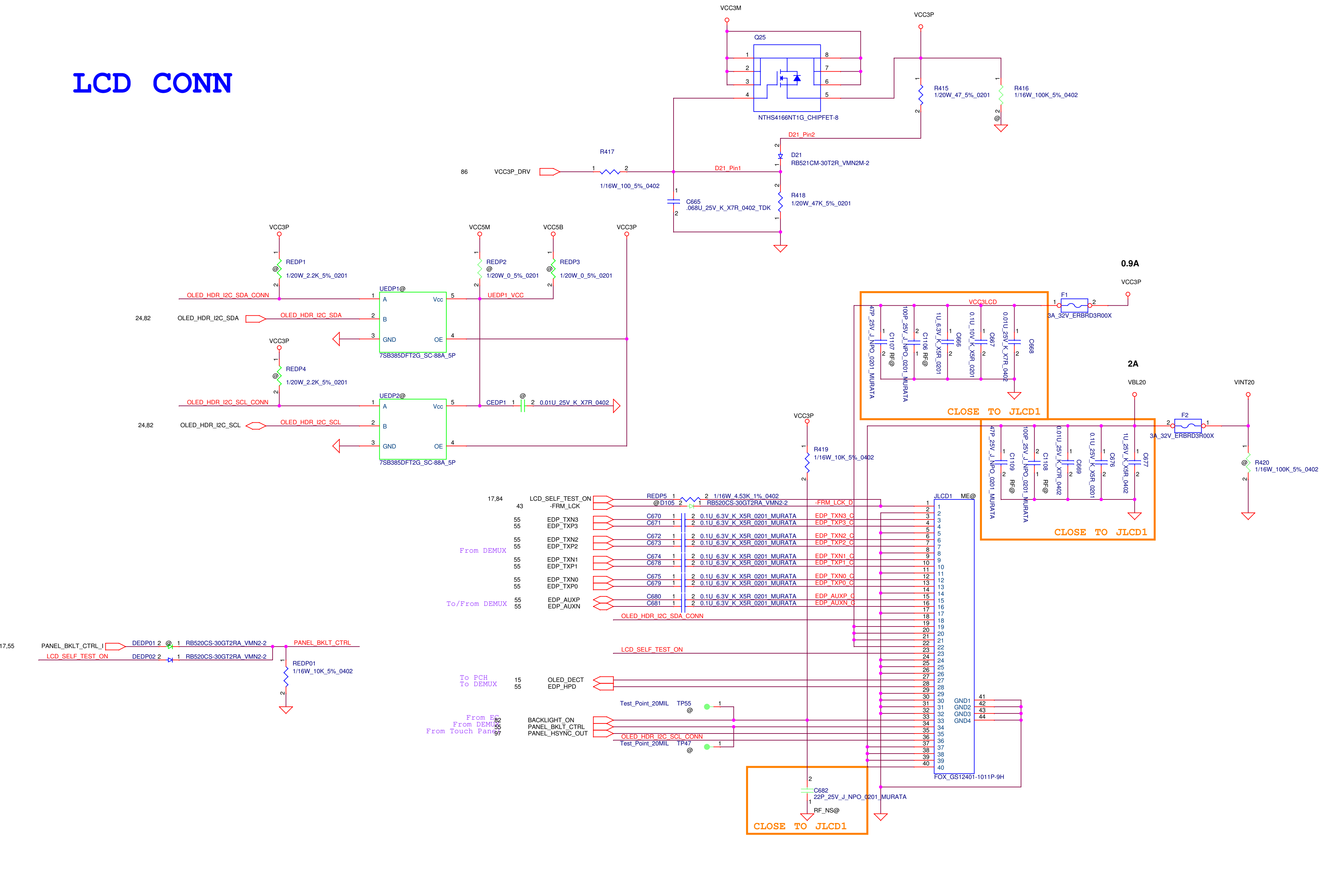
"-DGFX_OUTPUT_ENABLE" signal controls DOCK DP Bus switch

High : iGPU output is selected.
Low : dGPU output is selected.

SEL :(L,H) = (B -> A, C ->A)
SEL :(L,H) = (dGPU, iGPU)
Aux
S : (L,H) = (nA to nB1, nA to nB2)
= (dGPU, iGPU)

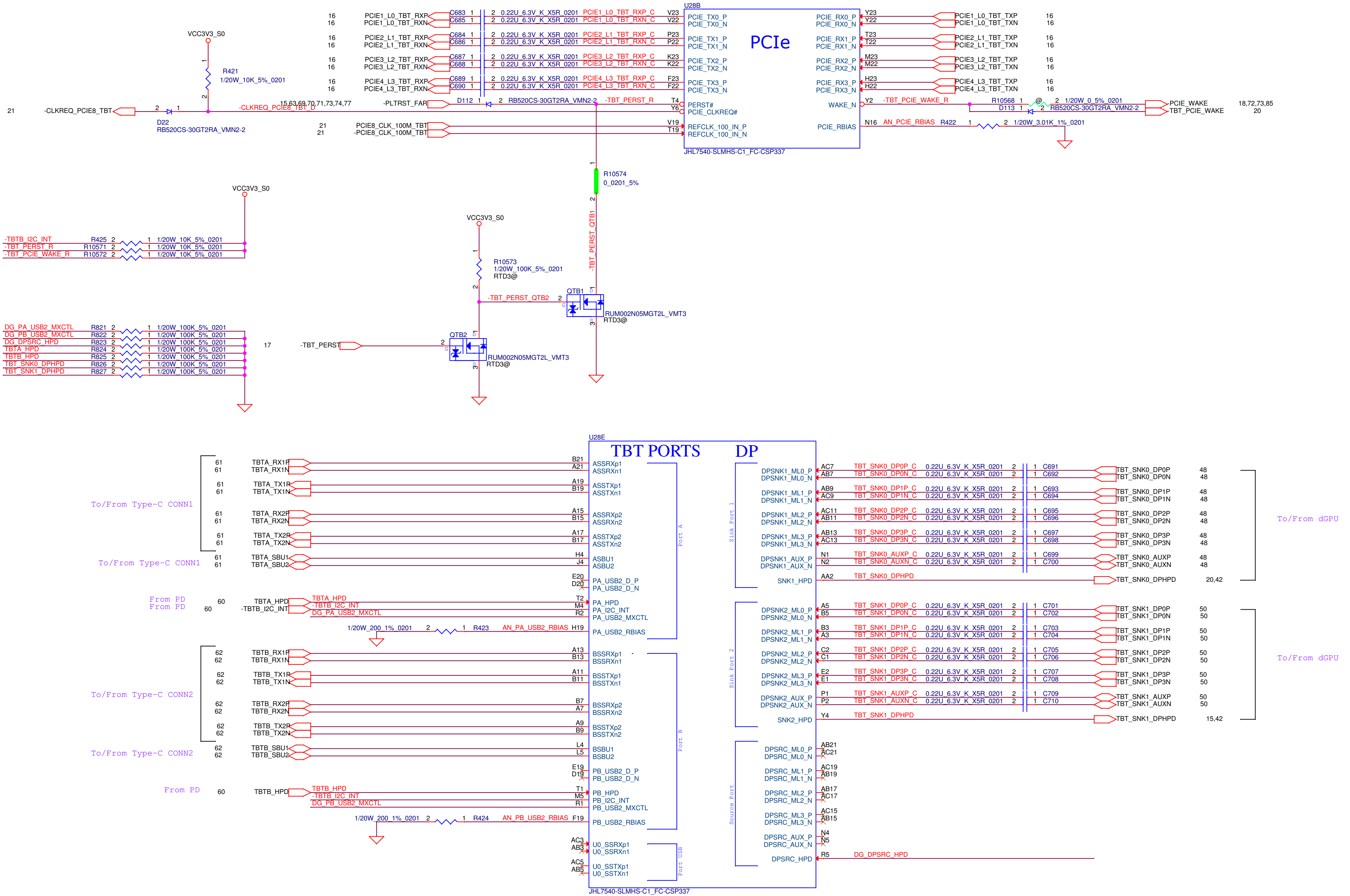
DOCK DP Switch		
Vendor	Vendor PN	LCFC PN
NXP	CBTL04083ABS	
Pericom	PI3PCIE3412ZHE+DAX	

LCD CONN



VCC3M
Q25
NTHS4166NT1G_CHIPFET-8
VCC3P
R415
1/20W_47_5%_0201
R416
1/16W_100K_5%_0402
D21_Pin2
D21
RB521CM-30T2R_VMN2M-2
R417
86
VCC3P_DRV
1/16W_100_5%_0402
D21_Pin1
C665
.068U_25V_K_X7R_0402_TDK
R418
1/20W_47K_5%_0201
VCC3P
VCC5M
VCC5B
REDP1
1/20W_2.2K_5%_0201
REDP2
1/20W_0_5%_0201
REDP3
1/20W_0_5%_0201
OLED_HDR_I2C_SDA_CONN
UEDP1@
UEDP1_VCC
24,82
OLED_HDR_I2C_SDA
7SB385DFT2G_SC-88A_5P
REDP4
1/20W_2.2K_5%_0201
OLED_HDR_I2C_SCL_CONN
UEDP2@
CEDP1
0.01U_25V_K_X7R_0402
24,82
OLED_HDR_I2C_SCL
7SB385DFT2G_SC-88A_5P
0.9A
VCC3P
VCC3LCD
F1
3A_32V_ERBRD3R00X
47P_25V_J_NPO_0201_MURATA
C1107 RF@
100P_25V_J_NPO_0201_MURATA
C1106 RF@
1U_6.3V_K_X5R_0201
C666
0.1U_10V_K_X5R_0201
C667
0.01U_25V_K_X7R_0402
C668
CLOSE TO JLCD1
2A
VBL20
VINT20
F2
3A_32V_ERBRD3R00X
R420
1/16W_100K_5%_0402
C1109 RF@
C1108 RF@
0.01U_25V_K_X7R_0402
C669
0.1U_25V_K_X5R_0201
C676
1U_25V_K_X5R_0402
C677
CLOSE TO JLCD1
VCC3P
R419
1/16W_10K_5%_0402
17,84
LCD_SELF_TEST_ON
43
-FRM_LCK
REDP5
1/16W_4.53K_1%_0402
@D105
RB520CS-30GT2RA_VMN2-2
-FRM_LCK_D
JLCD1
ME@
From DEMUX
EDP_TXN3
EDP_TXP3
EDP_TXN2
EDP_TXP2
EDP_TXN1
EDP_TXP1
EDP_TXN0
EDP_TXP0
To/From DEMUX
EDP_AUXP
EDP_AUXN
0.1U_6.3V_K_X5R_0201_MURATA
EDP_TXN3_C
EDP_TXP3_C
EDP_TXN2_C
EDP_TXP2_C
EDP_TXN1_C
EDP_TXP1_C
EDP_TXN0_C
EDP_TXP0_C
EDP_AUXP_C
EDP_AUXN_C
OLED_HDR_I2C_SDA_CONN
17,55
PANEL_BKLT_CTRL_I
DEDP01
RB520CS-30GT2RA_VMN2-2
PANEL_BKLT_CTRL
LCD_SELF_TEST_ON
DEDP02
REDP01
1/16W_10K_5%_0402
LCD_SELF_TEST_ON
To PCH
To DEMUX
OLED_DECT
EDP_HPD
Test_Point_20MIL
TP55
From EC
From DEMUX
From Touch Panel
BACKLIGHT_ON
PANEL_BKLT_CTRL
PANEL_HSYNC_OUT
OLED_HDR_I2C_SCL_CONN
TP47
GND1
GND2
GND3
GND4
FOX_GS12401-1011P-9H
C682
22P_25V_J_NPO_0201_MURATA
RF_NS@
CLOSE TO JLCD1

TUNDERBOLT



LC Future Center Secret Data	Project Name
LCFC	*Nighthawk-1*
Rev 1.0	Title: *Titan Ridge (1/3)*
Date: Monday, April 29, 2019	Sheet 57 of 142

TUNDERBOLT

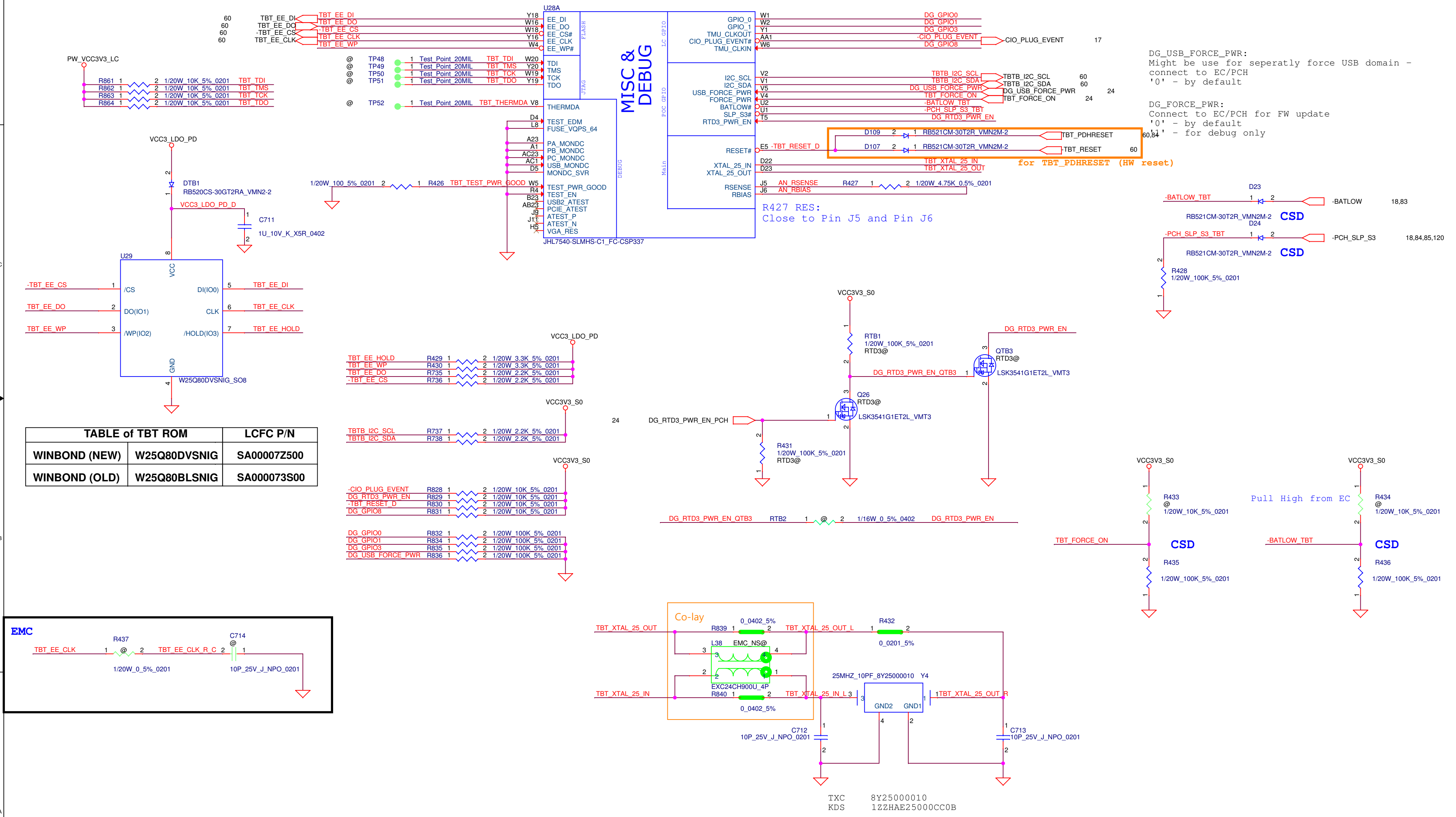


TABLE of TBT ROM		LCFC P/N
WINBOND (NEW)	W25Q80DVSNIG	SA00007Z500
WINBOND (OLD)	W25Q80BLSNIG	SA000073S00

LC Future Center Secret Data

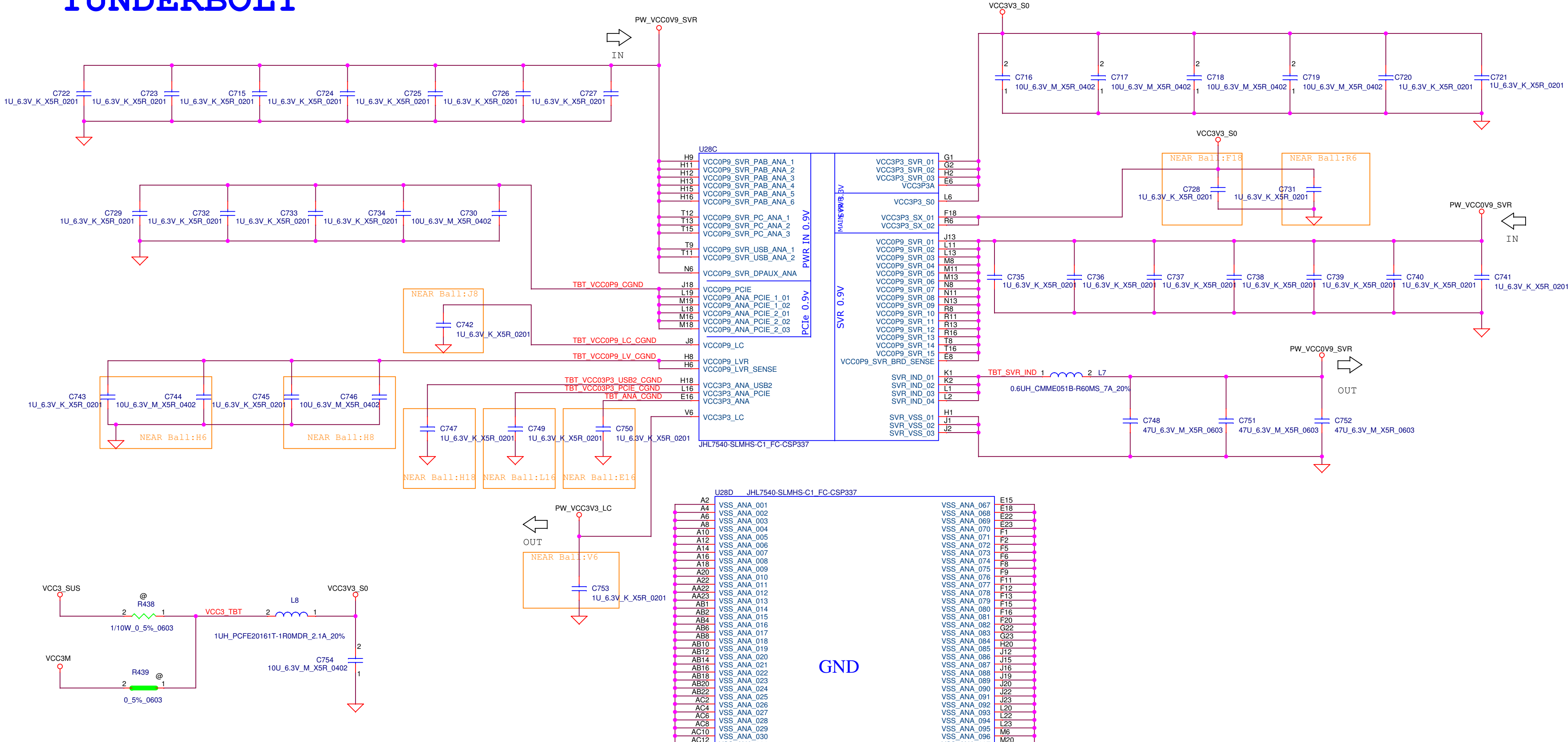
Project Name: Nighthawk-1

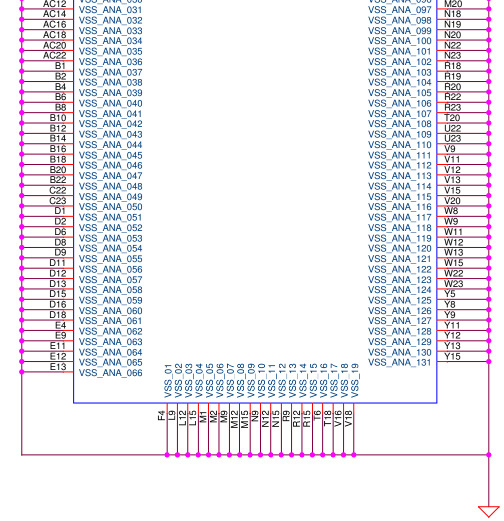
Rev 1.0

Title: Titan Ridge (2/3)

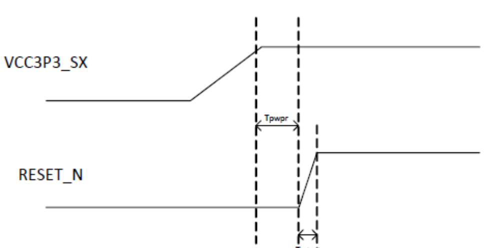
Date: Monday, April 29, 2019

TUNDERBOLT





Power On Sequence



Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

POWER DELIVERY

ADCIN1 BUS POWER CONFIGURATION

DIV = PDR3 / (PDR1 + PDR3)		CONFIGURATION
DIV MIN	DIV MAX	
0.00	0.18	BP_NoResponse
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

← LOGIC

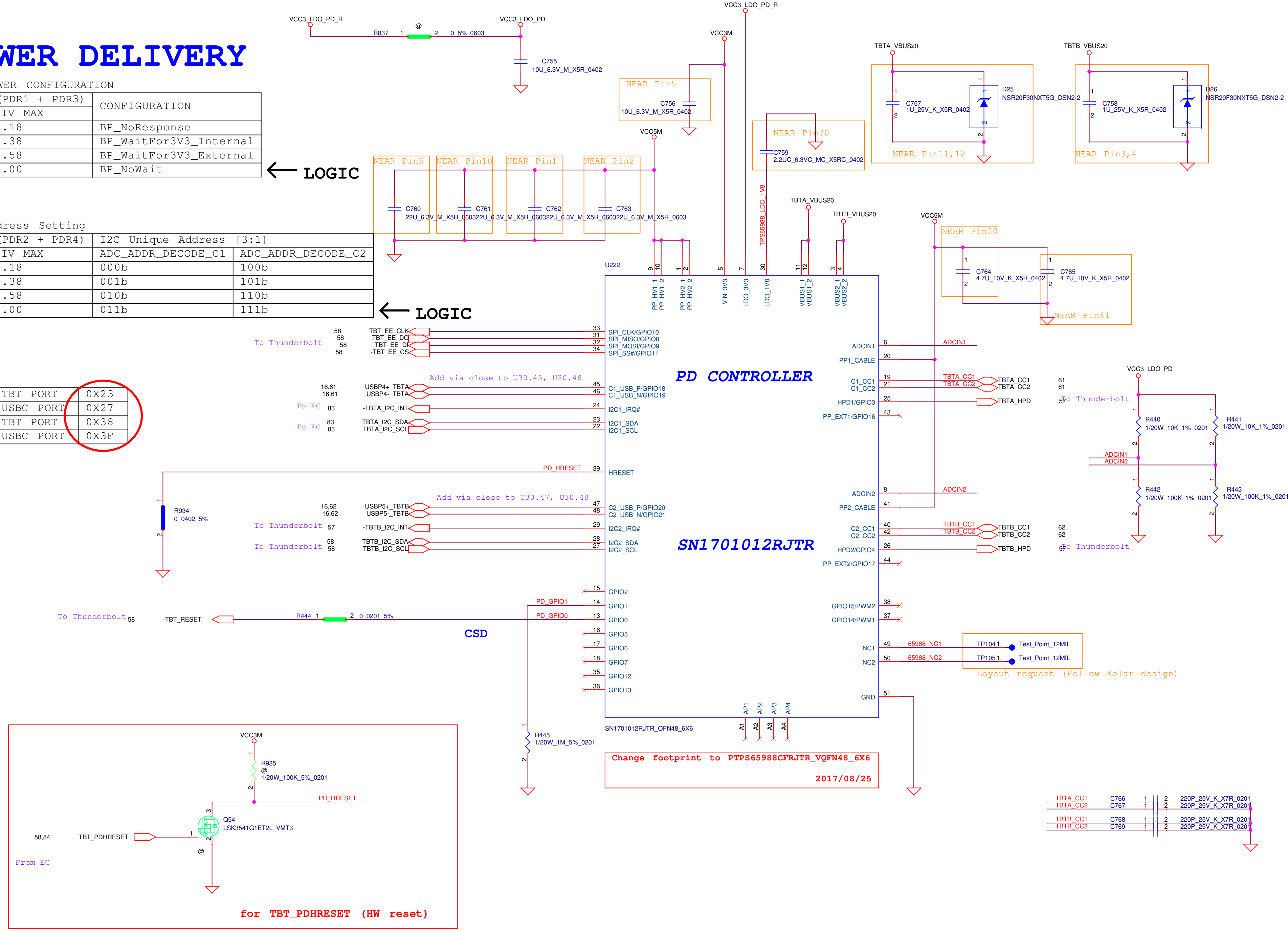
ADCIN2 I2C Address Setting

DIV = PDR4 / (PDR2 + PDR4)		I2C Unique Address [3:1]	
DIV MIN	DIV MAX	ADC_ADDR_DECODE_C1	ADC_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

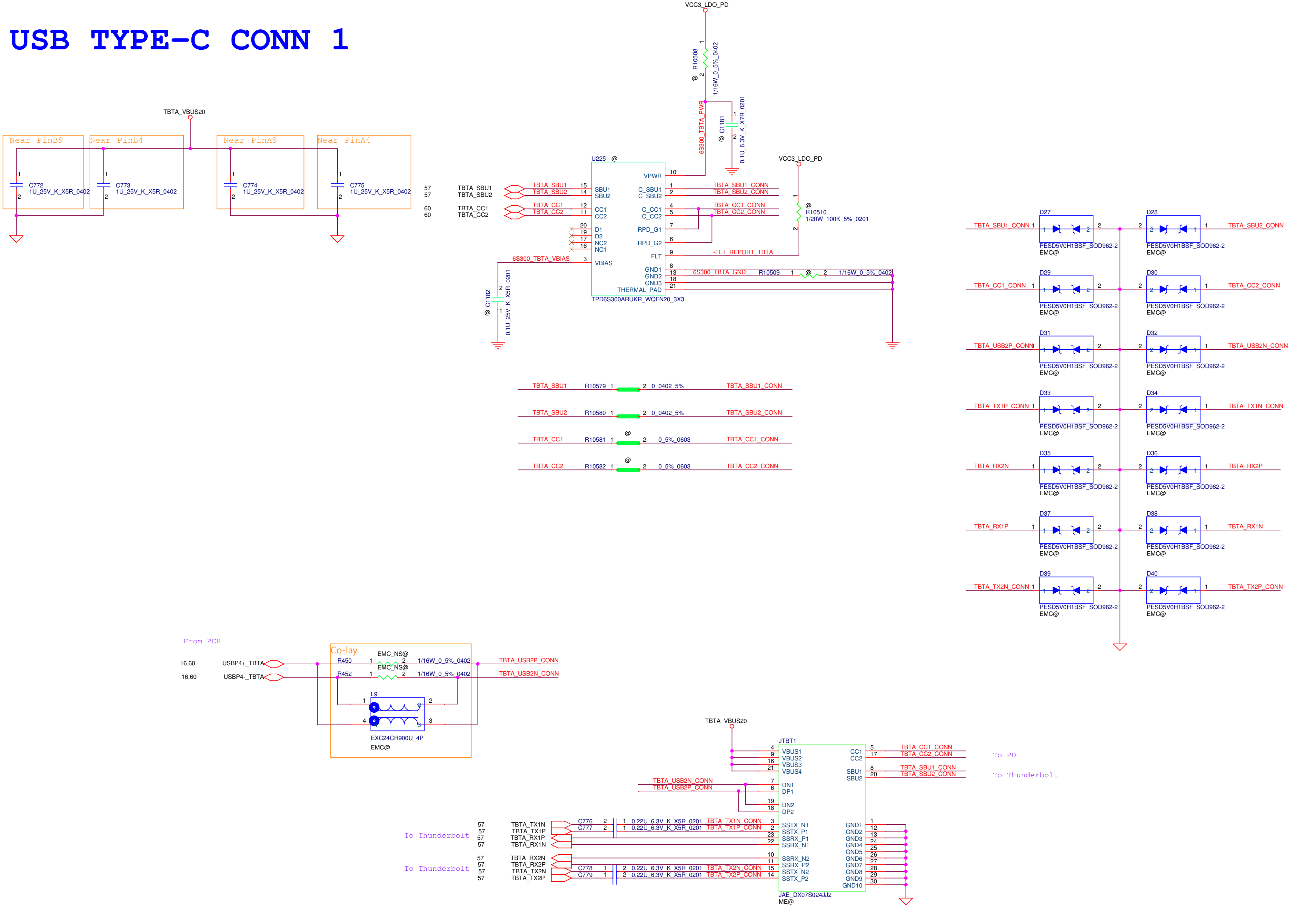
← LOGIC

I2C Address

I2C1 (to EC)	TBT PORT	0X23
	USBC PORT	0X27
I2C2 (to TR)	TBT PORT	0X38
	USBC PORT	0X3F



USB TYPE-C CONN 1



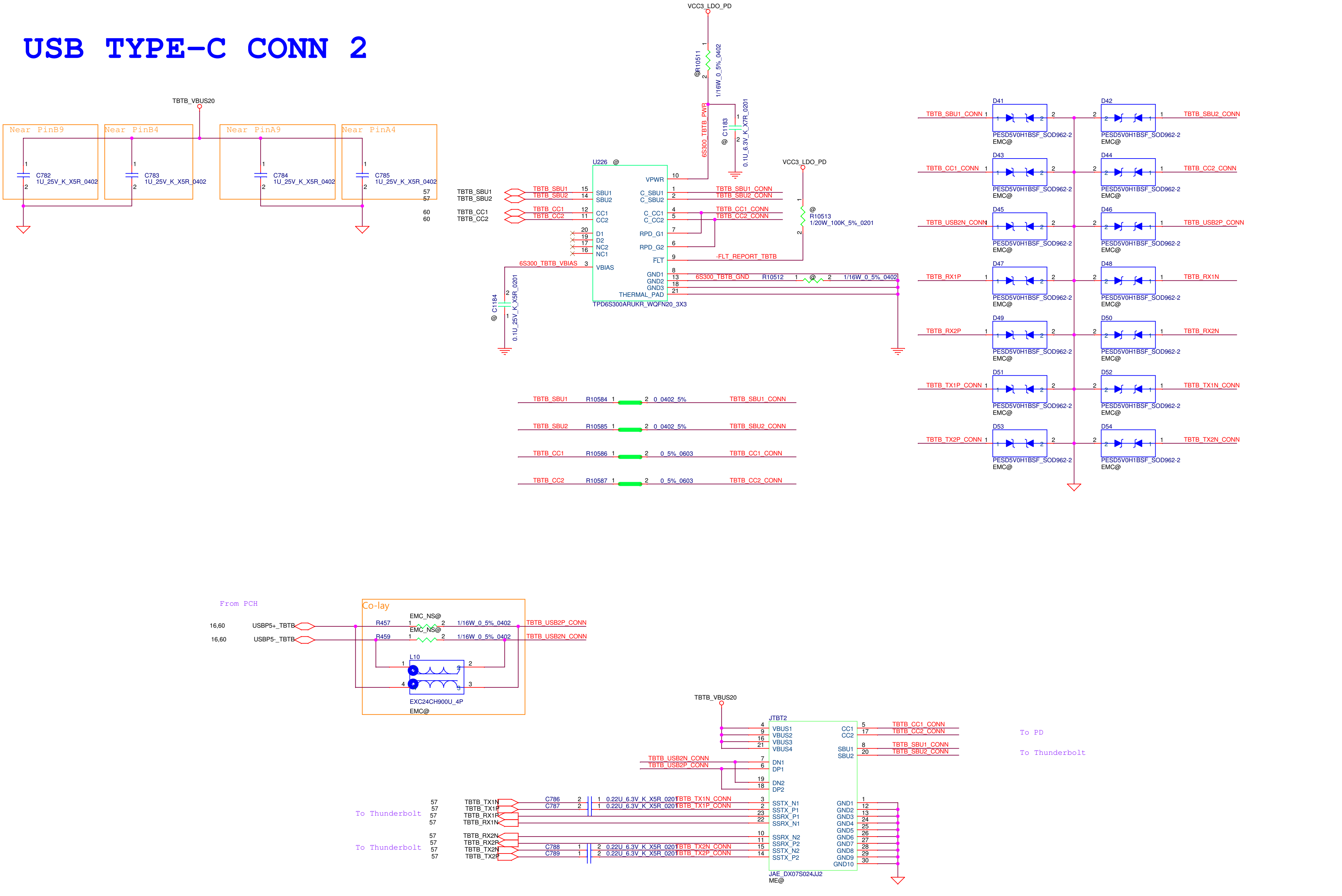
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0 | Title: USB TYPE-C CONNECTOR(1/2)

Date: Monday, April 29, 2019 | Sheet 61 of 142

USB TYPE-C CONN 2



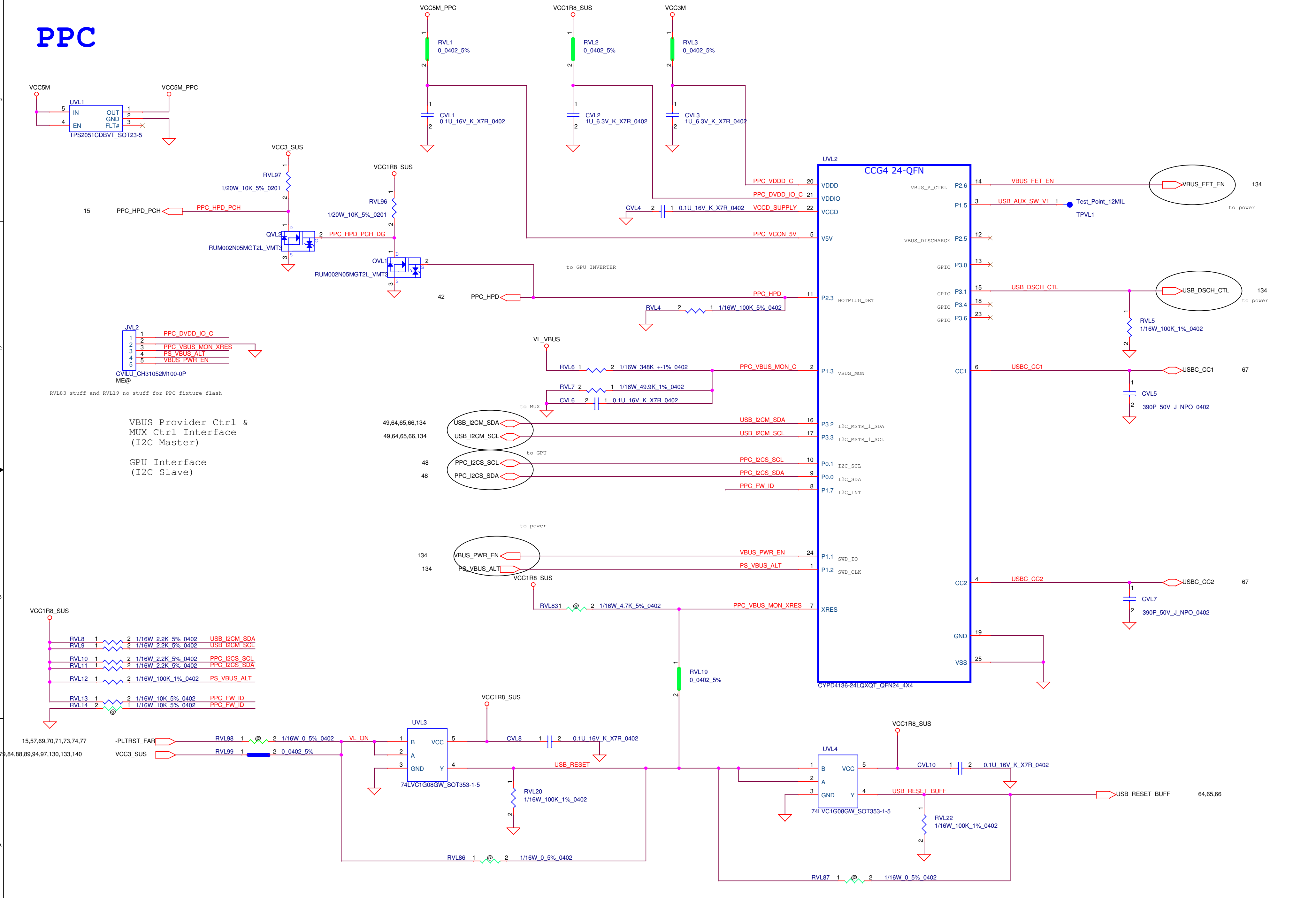
LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev 1.0 | Title: USB TYPE-C CONNECTOR(2/2)

Date: Monday, April 29, 2019 | Sheet 62 of 142

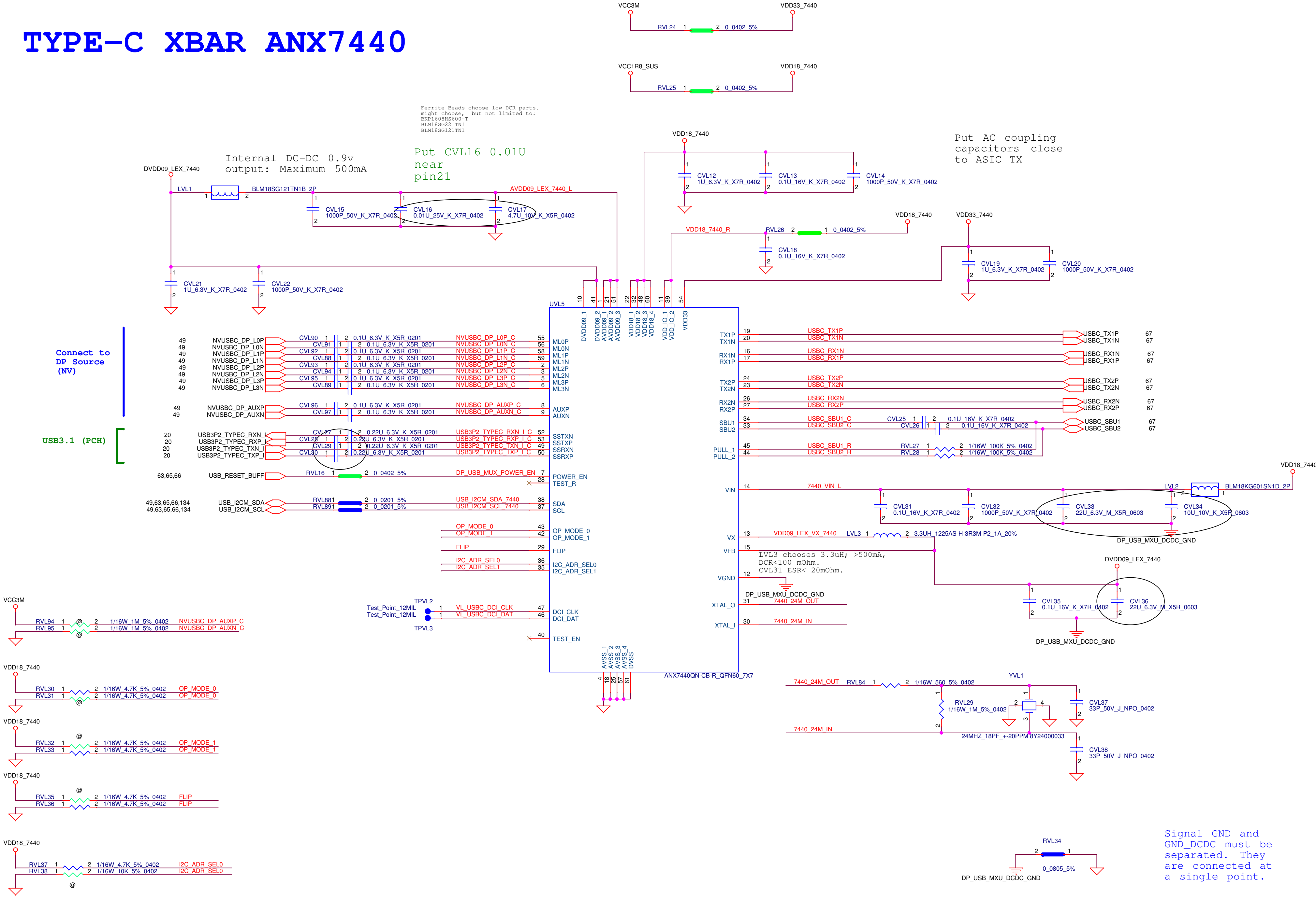
PPC



LC Future Center Secret Data

Project Name	Nighthawk-1
Rev 1.0	Title PPC
Date: Monday, April 29, 2019	Sheet 63 of 142

TYPE-C XBAR ANX7440



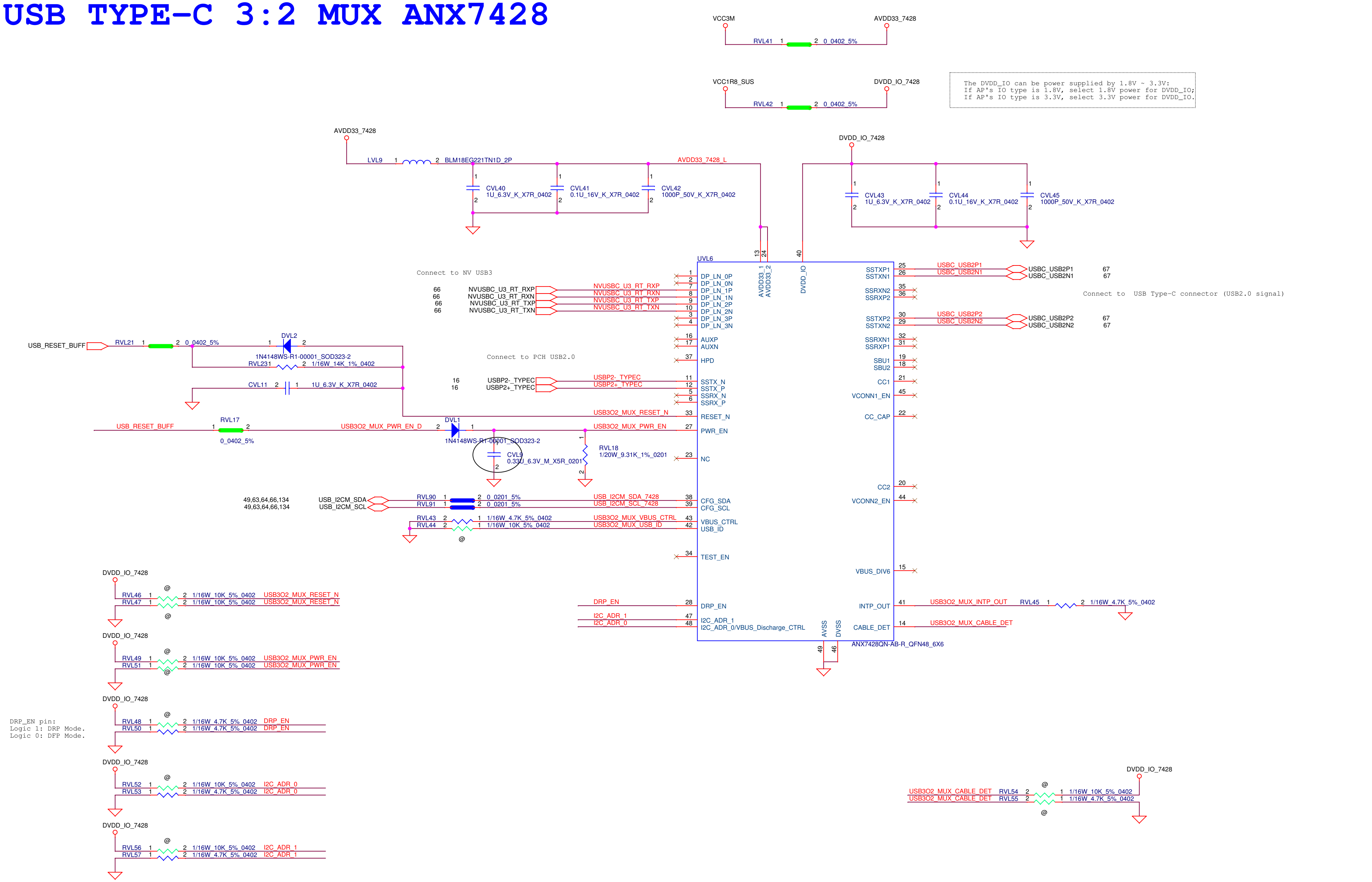
OP_MODE_I/O	MODE
00	Disabled
01	USB3
10	DP
11	USB3 + DP

FLIP:
USB Typc-C Orientation:
0=normal, 1=flipped

CC1 detection is normal
or
CC2 detection is flipped

USB TYPE-C 3:2 MUX ANX7428

The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.



DRP_EN pin:
Logic 1: DRP Mode.
Logic 0: DFP Mode.

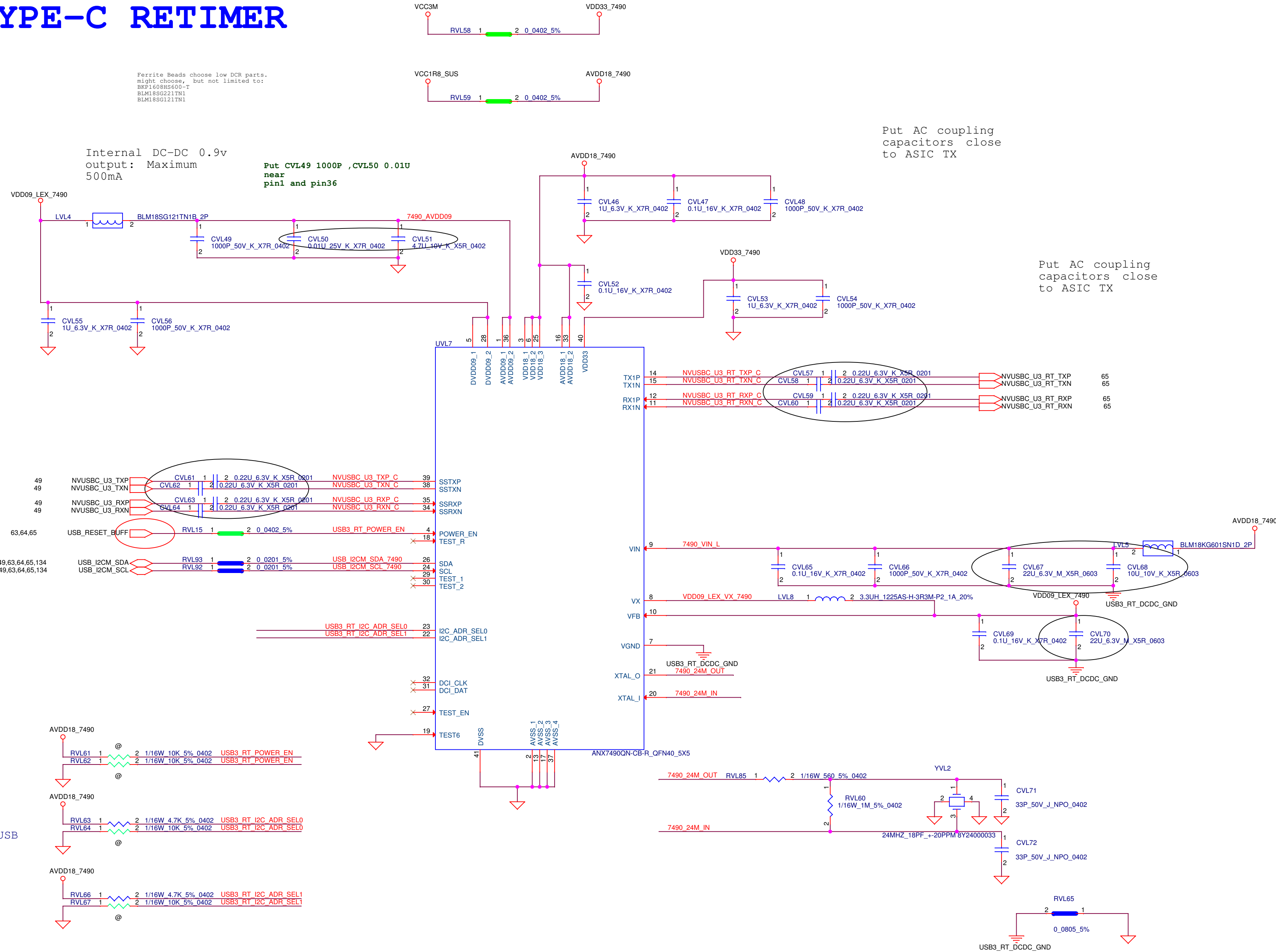
I2C Address Selection:

I2C_ADR_1	I2C_ADR_0	I2C Addr
Logic 0(R19=DNP)	Logic 0(R20=DNP, R38=0R, R40=4.7K, R39=DNP, Q11=DNP)	0x50
Logic 0(R19=DNP)	Logic 1(R20=4.7K, R38=DNP, R40=DNP, R39=4.7K, Q11=FDV301N)	0x72
Logic 1(R19=4.7K)	Logic 0(R20=DNP, R38=0R, R40=4.7K, R39=DNP, Q11=DNP)	0x7c
Logic 1(R19=4.7K)	Logic 1(R20=4.7K, R38=DNP, R40=DNP, R39=4.7K, Q11=FDV301N)	0x80

I2C_ADR_1 and I2C_ADR_0 pin:
1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

Project Name: Nighthawk-1
Rev 1.0
Title: USB-C 3:2 MUX
Date: Monday, April 29, 2019

NV USB TYPE-C RETIMER



Put AC coupling capacitors close to SSTXP/N pins

Assume connection to a USB Micro B receptacle

If ANX7490 is on host motherboard, then
USB3.1_SSTX+/- connect to chipset SSRX,
USB3.1_SSRX+/- connect to chipset SSTX

Note:
Both SSTx and SSRx between USB host and ANX7490 need AC capacitors.
USB host SSTx connects to ANX7490 SSRx.
USB host SSRx connects to ANX7490 SSTx.
The capacitors should be placed near SSTx pin.

Signal GND and GND_DCDC must be separated. They are connected at a single point.

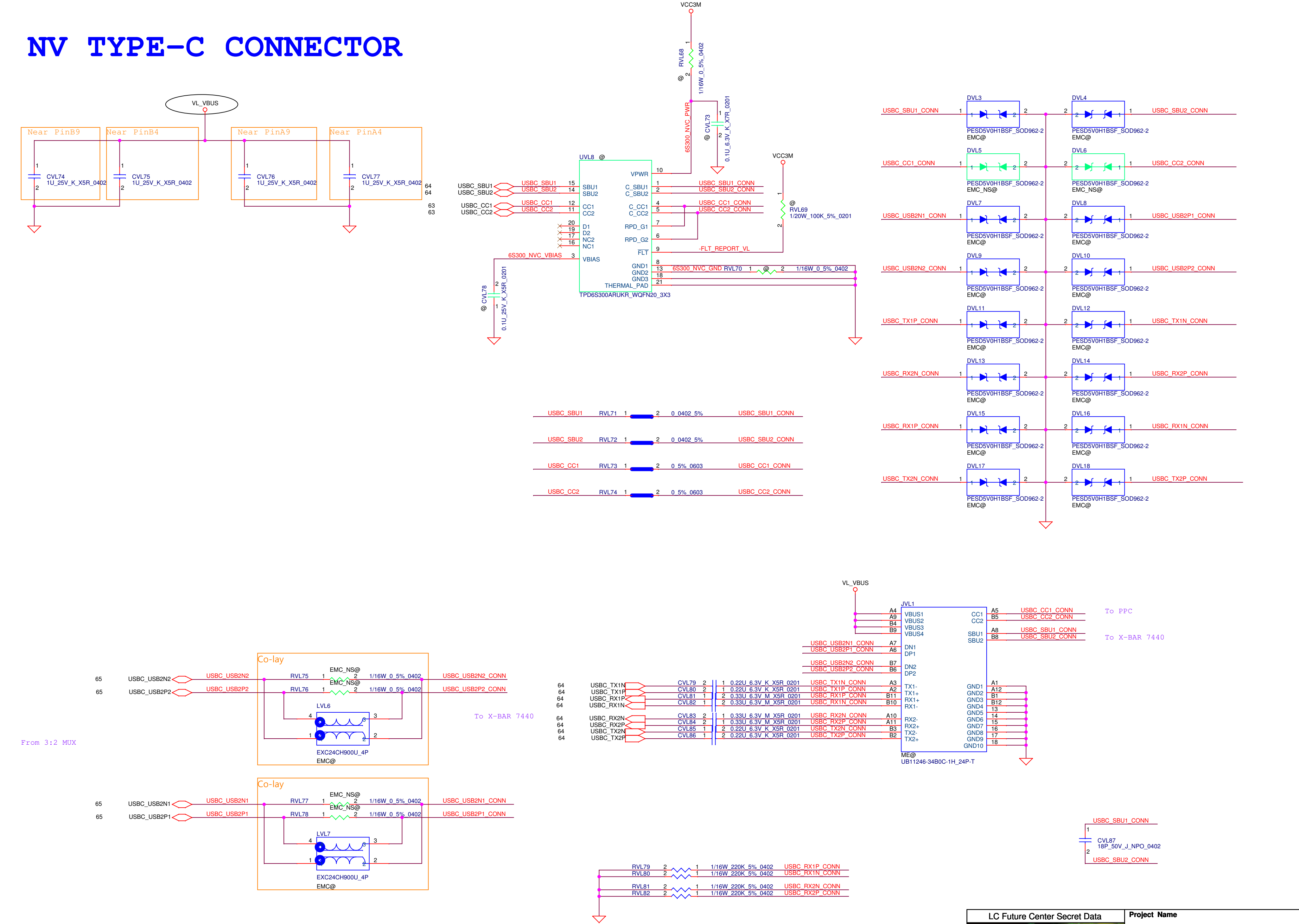
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0 | Title: NV USB TYPE-C RETIMER

Date: Monday, April 29, 2019 | Sheet 66 of 142

NV TYPE-C CONNECTOR



LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0

Title: NV TYPE-C CONNECTOR

Date: Monday, April 29, 2019

5 4 3 2 1

D C B A

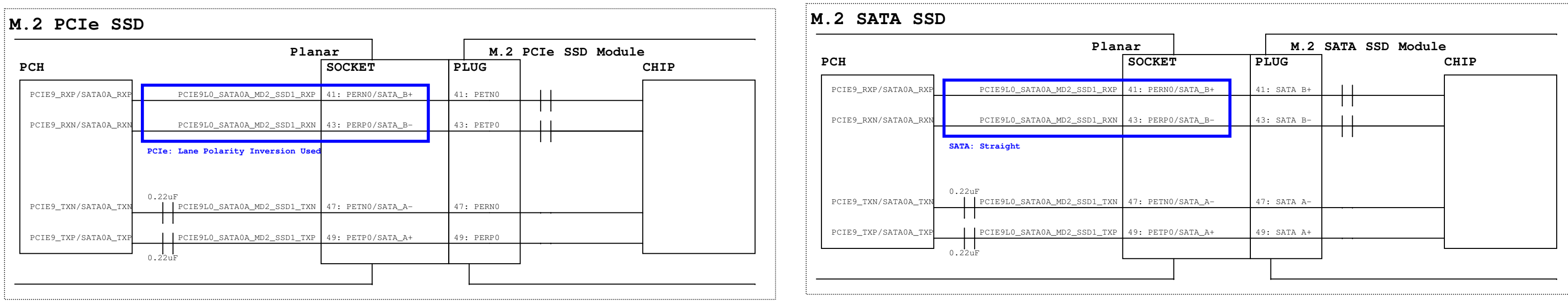
BLANK

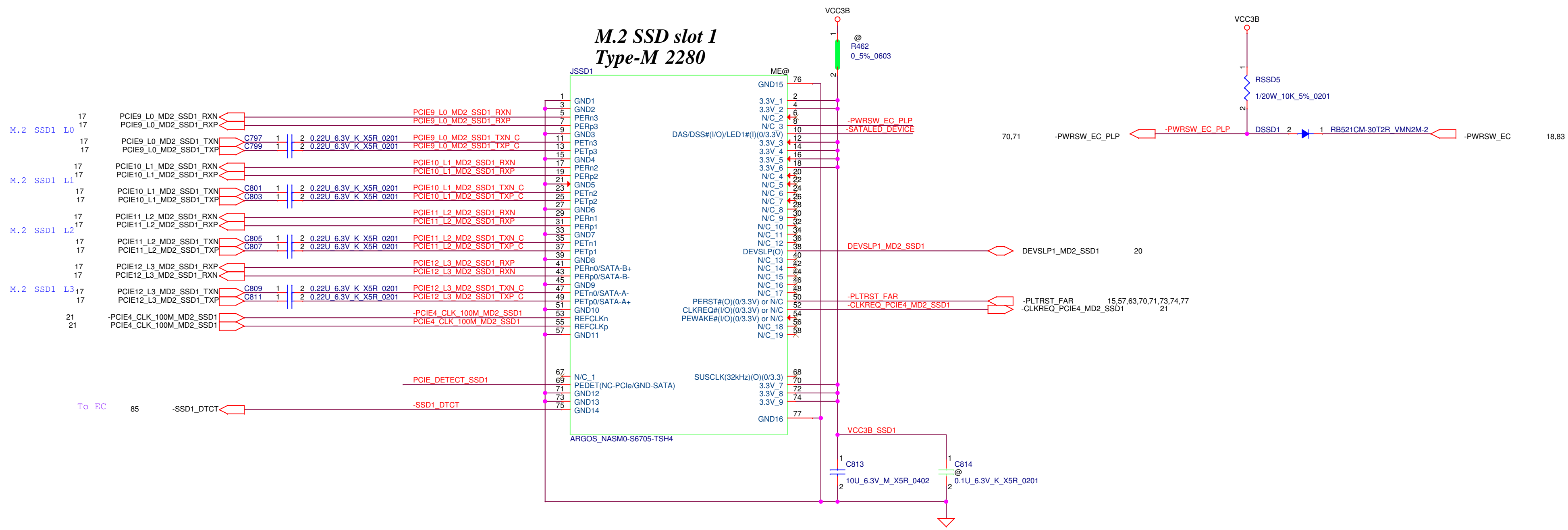
LC Future Center Secret Data

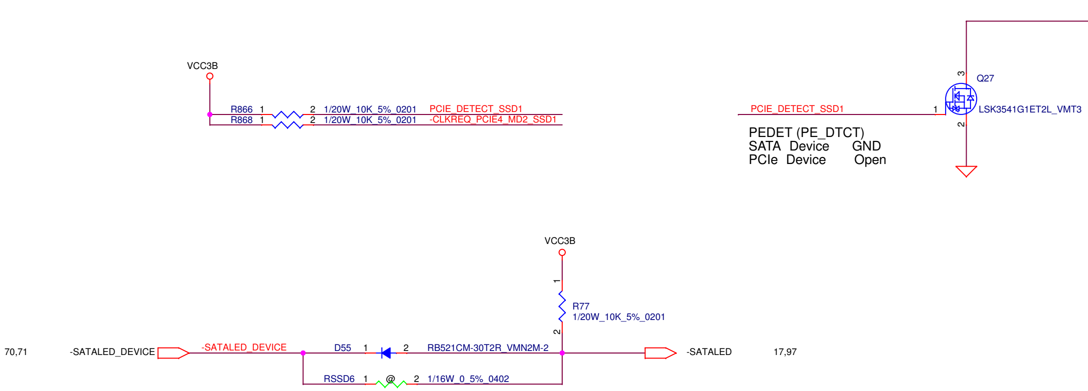
LCFC

Project Name		
Nighthawk-1		
Rev 1.0	Title **BLANK**	
Date: Monday, April 29, 2019	Sheet 68 of 142	

M.2 SSD







-PCIE_DETECT_SSD1 17

TABLE

-PCIE_DETECT_SSD1	Device
High	SATA SSD
LOW	PCIe SSD

LC Future Center Secret Data

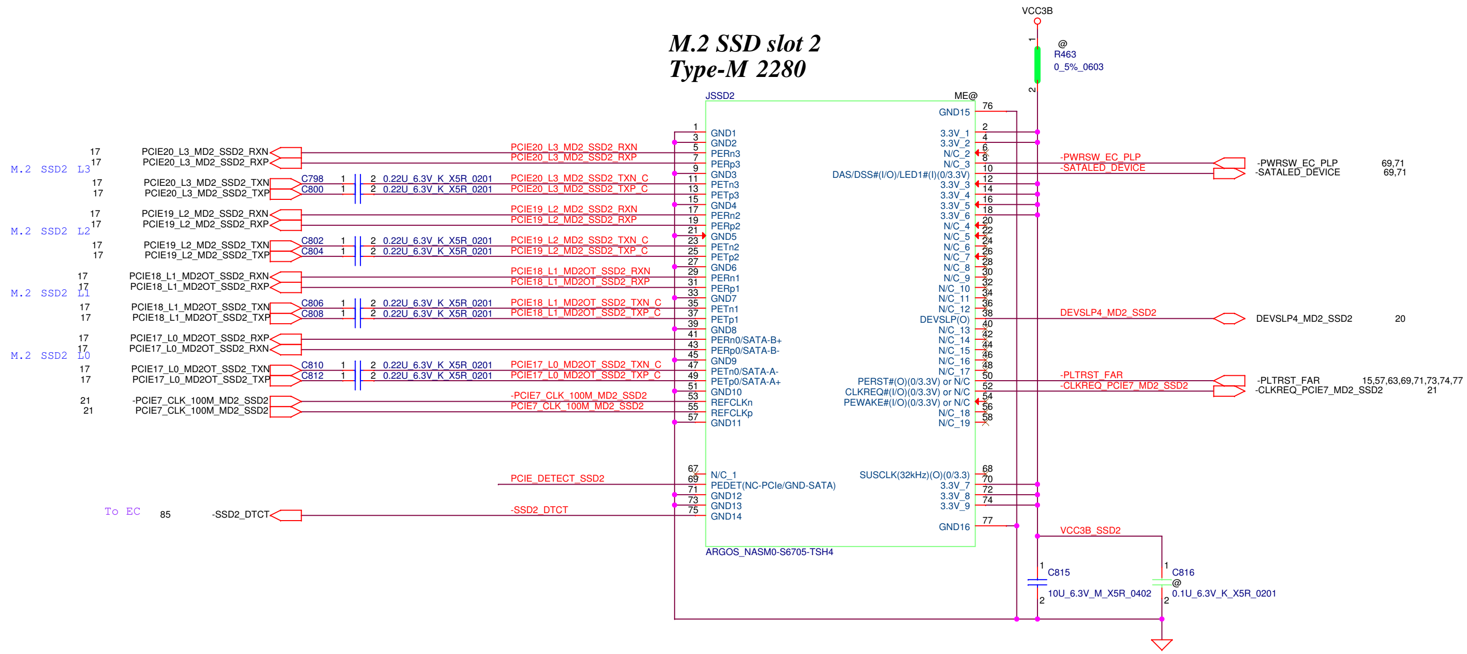
Project Name: Nighthawk-1

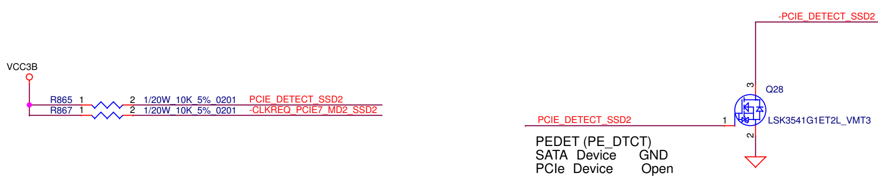
Rev 1.0

Title: M.2 SATA/PCIE SSD SLOT_1

Date: Monday, April 29, 2019

M.2 SSD





TABLE

-PCIE_DETECT_SSD2	Device
High	SATA SSD
LOW	PCIe SSD

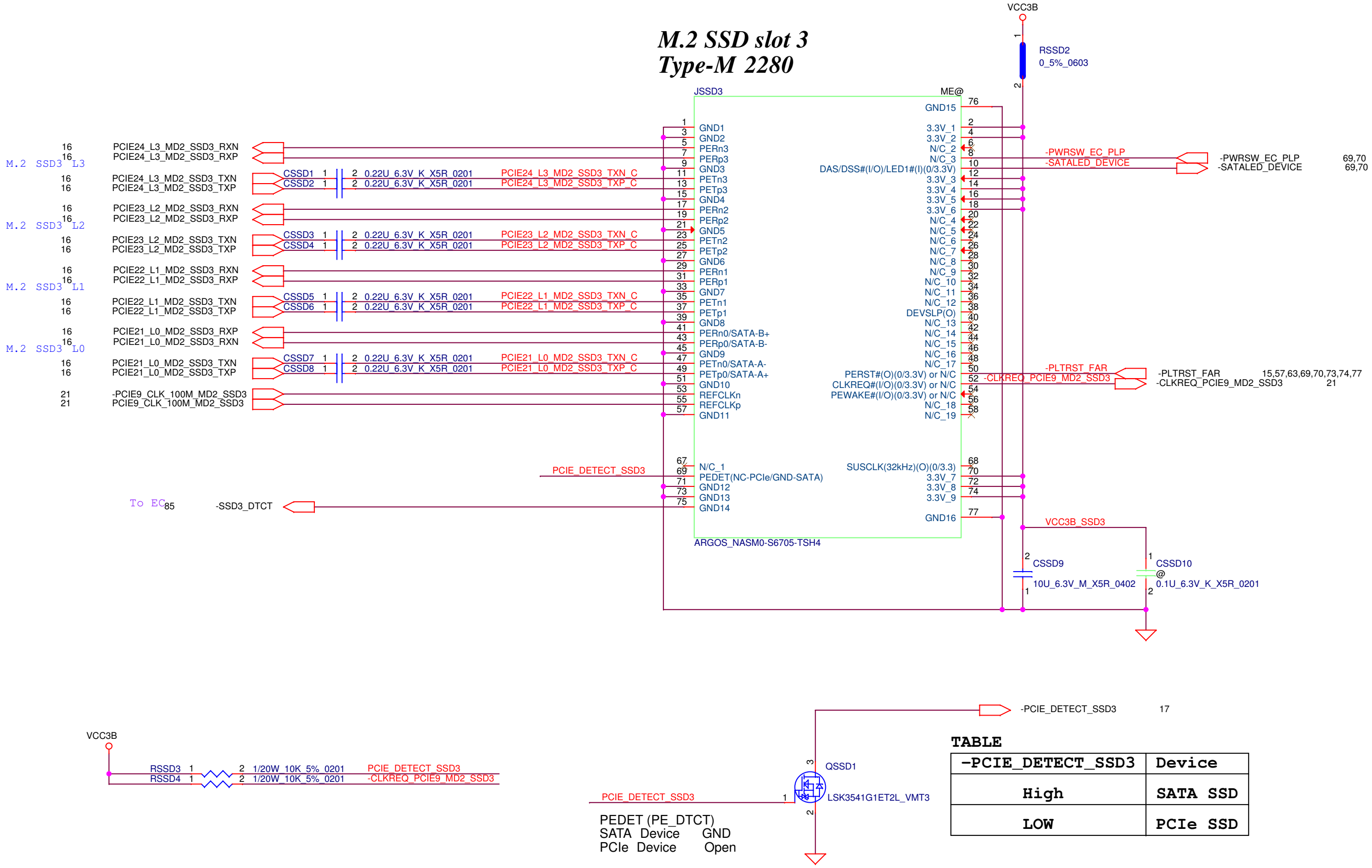
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0 | Title: M.2 SATA/PCIE SSD SLOT_2

Date: Monday, April 29, 2019 | Sheet 70 of 142

M.2 SSD



TABLE

-PCIE_DETECT_SSD3	Device
High	SATA SSD
LOW	PCIe SSD

LC Future Center Secret Data

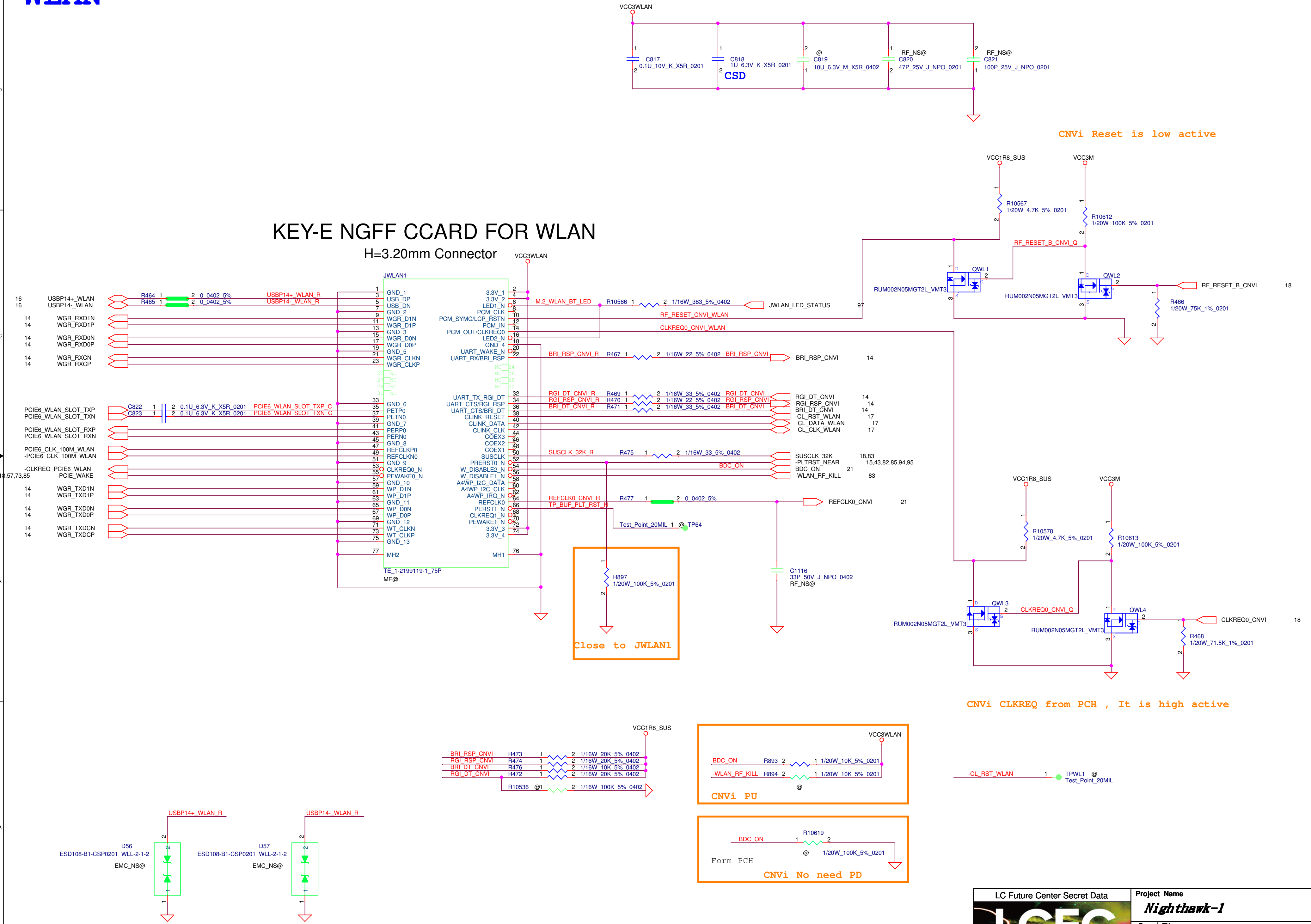
Project Name: Nighthawk-1

Rev 1.0

Title: M.2 SATA/PCIE SSD SLOT_3

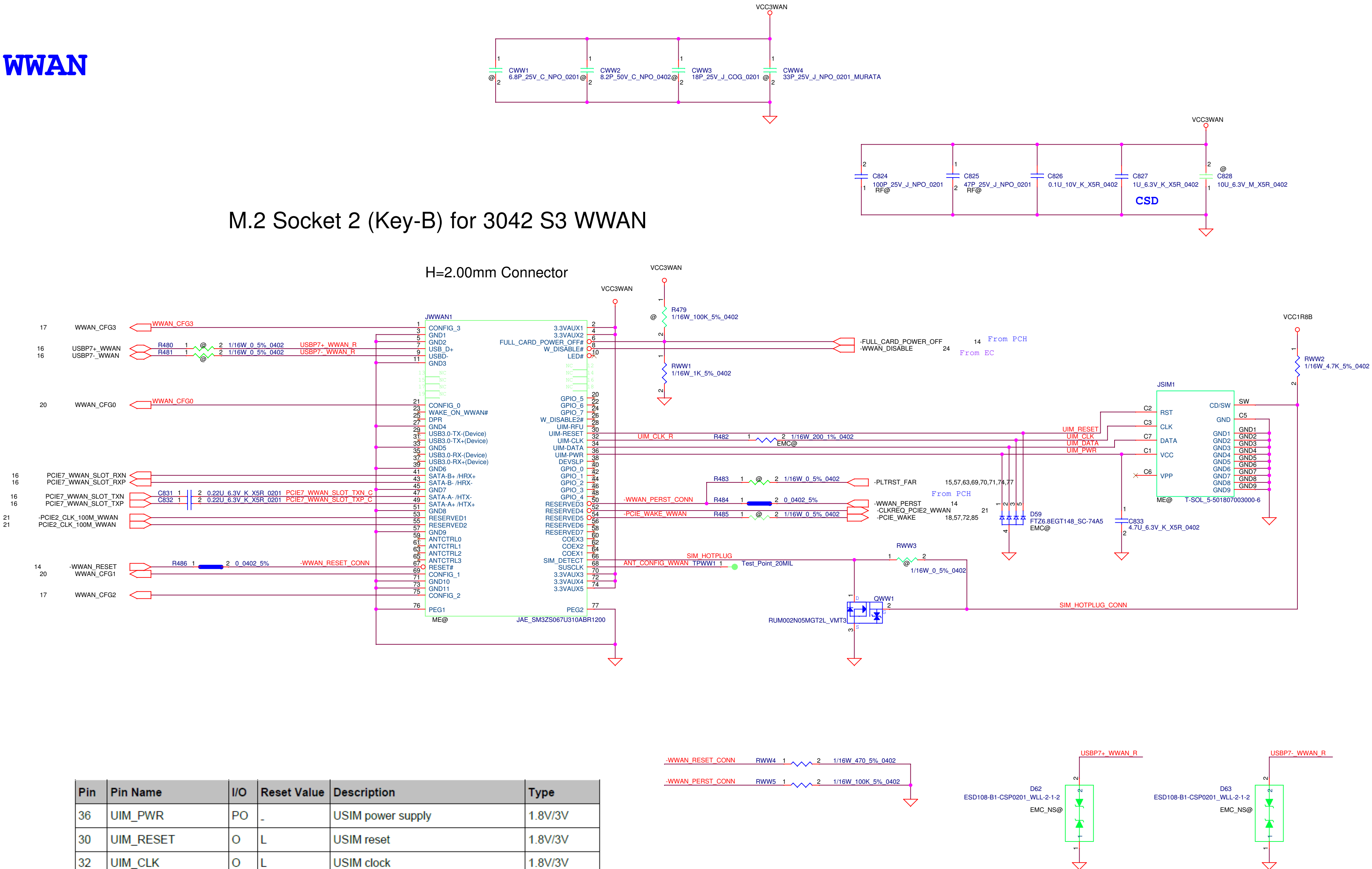
Date: Monday, April 29, 2019

WLAN



LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 — Title: M.2 WLAN CARD SLOT
	Date: Monday, April 29, 2019 — Sheet 72 of 142

WWAN



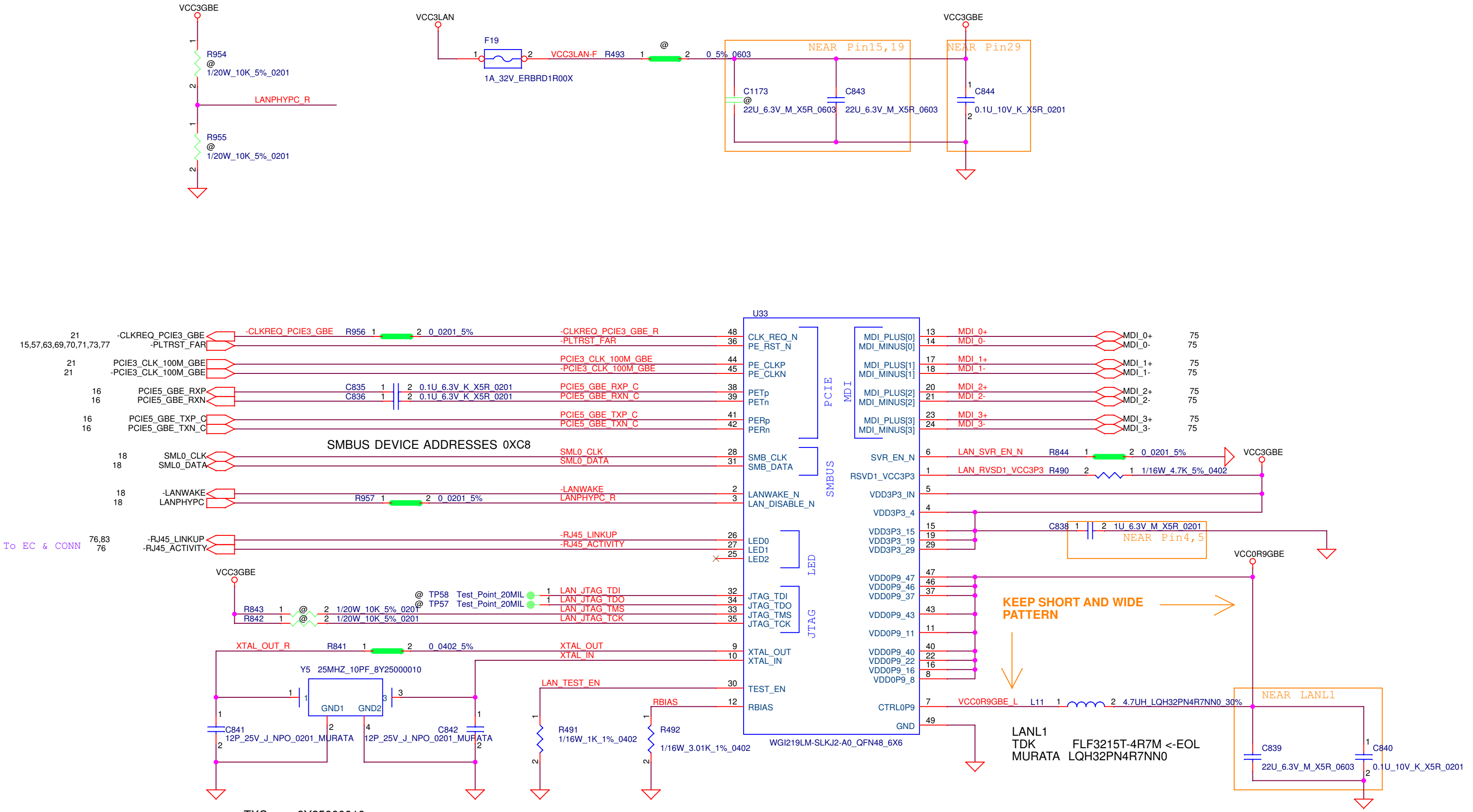
Pin	Pin Name	I/O	Reset Value	Description	Type
36	UIM_PWR	PO	_	USIM power supply	1.8V/3V
30	UIM_RESET	O	L	USIM reset	1.8V/3V
32	UIM_CLK	O	L	USIM clock	1.8V/3V
34	UIM_DATA	I/O	L	USIM data, internal pull up(4.7KΩ)	1.8V/3V
66	SIM_DETECT	I	PD	USIM card detect, internal 390K pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached.	1.8V

TABLE

	CONFIG 0	CONFIG 3	CONFIG 2	CONFIG 1
Fibocom L850-GL	GND	N.C.	GND	GND

LC Future Center Secret Data	Project Name: Nighthawk-1
Rev 1.0	Title: M.2 WWAN CARD SLOT
Date: Monday, April 29, 2019	Sheet 73 of 142

LAN



TXC 8Y25000010
KDS 1ZZHAE25000CC0B

LANU1 GBE PHY

vPRO Model	Non-vPRO Model
I219LM	I219V

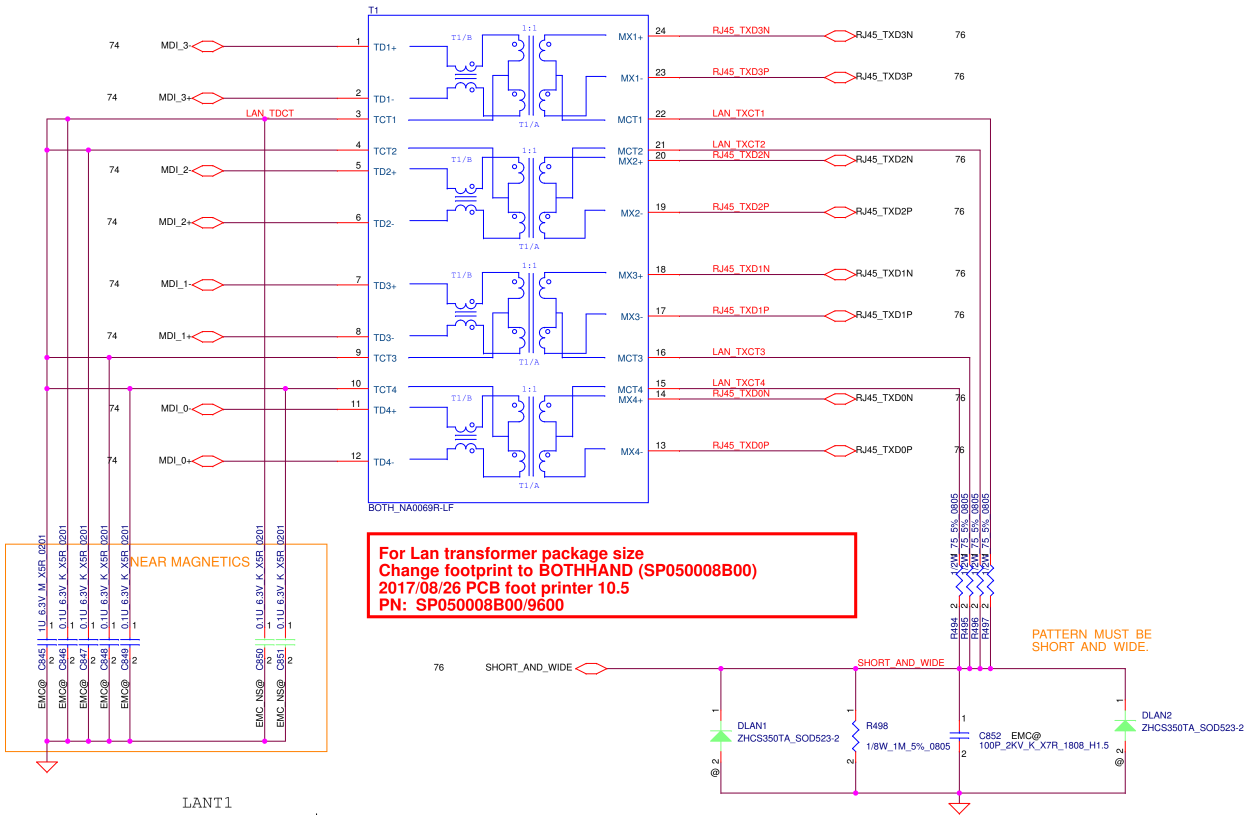
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0

Title: GBE JACKSONVILLE

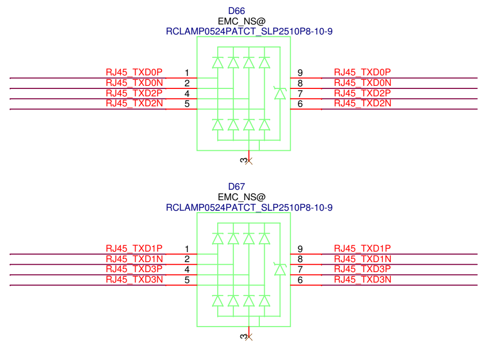
LAN



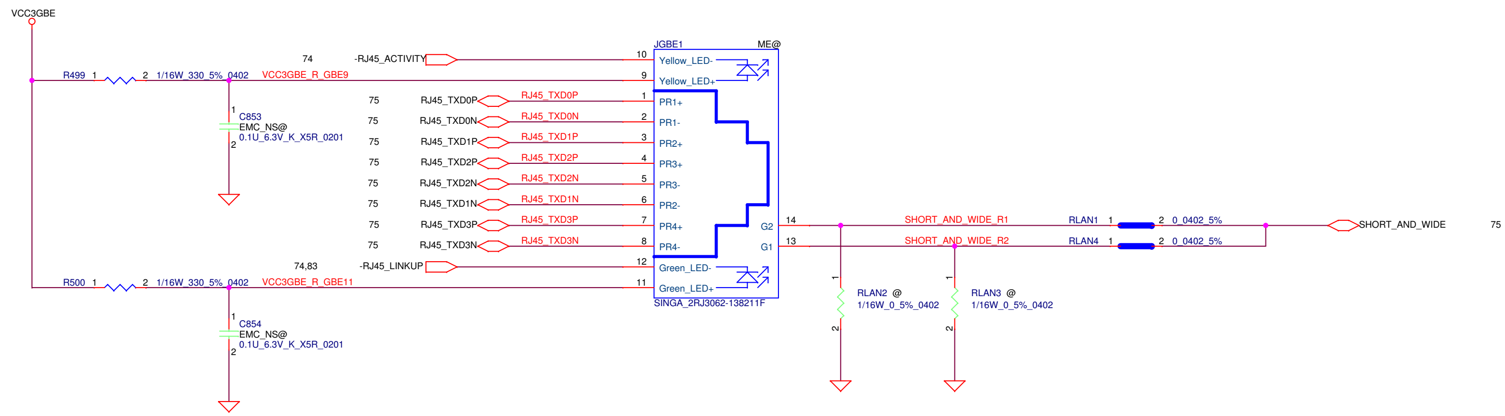
LANT1

Vendor	P/N
Bothhand	SP050008B00 NA69LF
TAIMAG	SP050009J00 IH-189-F LAN

LAN



D66,D67	1st:Semtech RCLAMP0524PATCT (SC300000T0J) 2nd:LittelFuse SP3012-04UTG-1 MO-229 (SC300003900) 3th:LittelFuse SP3012-04UTG UDFN (SC300003800)



LC Future Center Secret Data

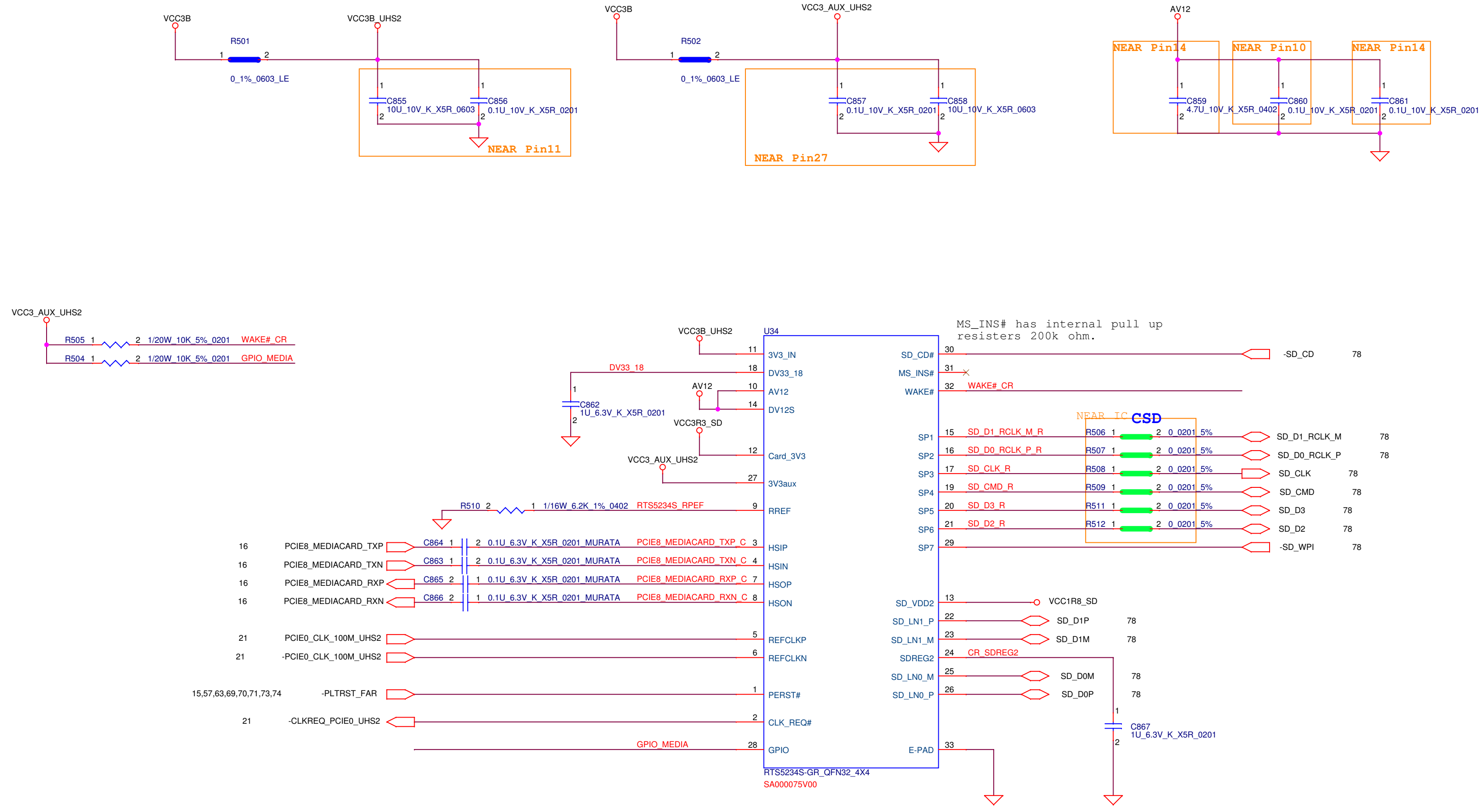
Project Name: Nighthawk-1

Rev: 1.0

Title: GBE_RJ45 CONNECTOR

Date: Monday, April 29, 2019

Card Reader



LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev: 1.0

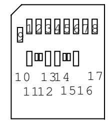
Title: MEDIACARD UHS-II

Date: Monday, April 29, 2019

Card Reader

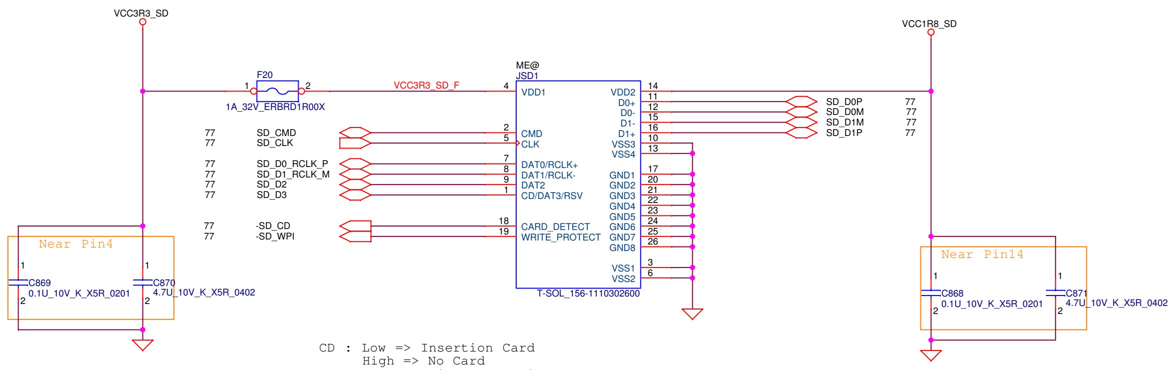
Normal type Pin No	UHS-II SD Slot SD Mode	UHS II Mode
1	CD/DAT3	
2	CMD	
3	VSS1	
4	VDD	VDD1
5	CLK	
6	VSS2	
7	DAT0	RCLKP
8	DAT1	RCLKM
9	DAT2	
10		VSS3
11		D0P
12		D0M
13		VSS4
14		VDD2
15		D1M
16		D1P
17		VSS5
CD	CARD DETECT	
WP	WRITE PROTECT	

Bottom View



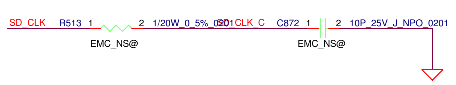
UHS II Interface
4 VDD1 3.3V
7 RCLKP
8 RCLKM
10 VSS3
11 D0P
12 D0M
13 VSS4
14 VDD2 1.8V
15 D1M
16 D1P
17 VSS5

UHS I Inteface
1 CD/DAT3
2 CMD
3 VSS1
4 VDD 3.3V
5 CLK
6 VSS2
7 DAT0
8 DAT1
9 DAT2



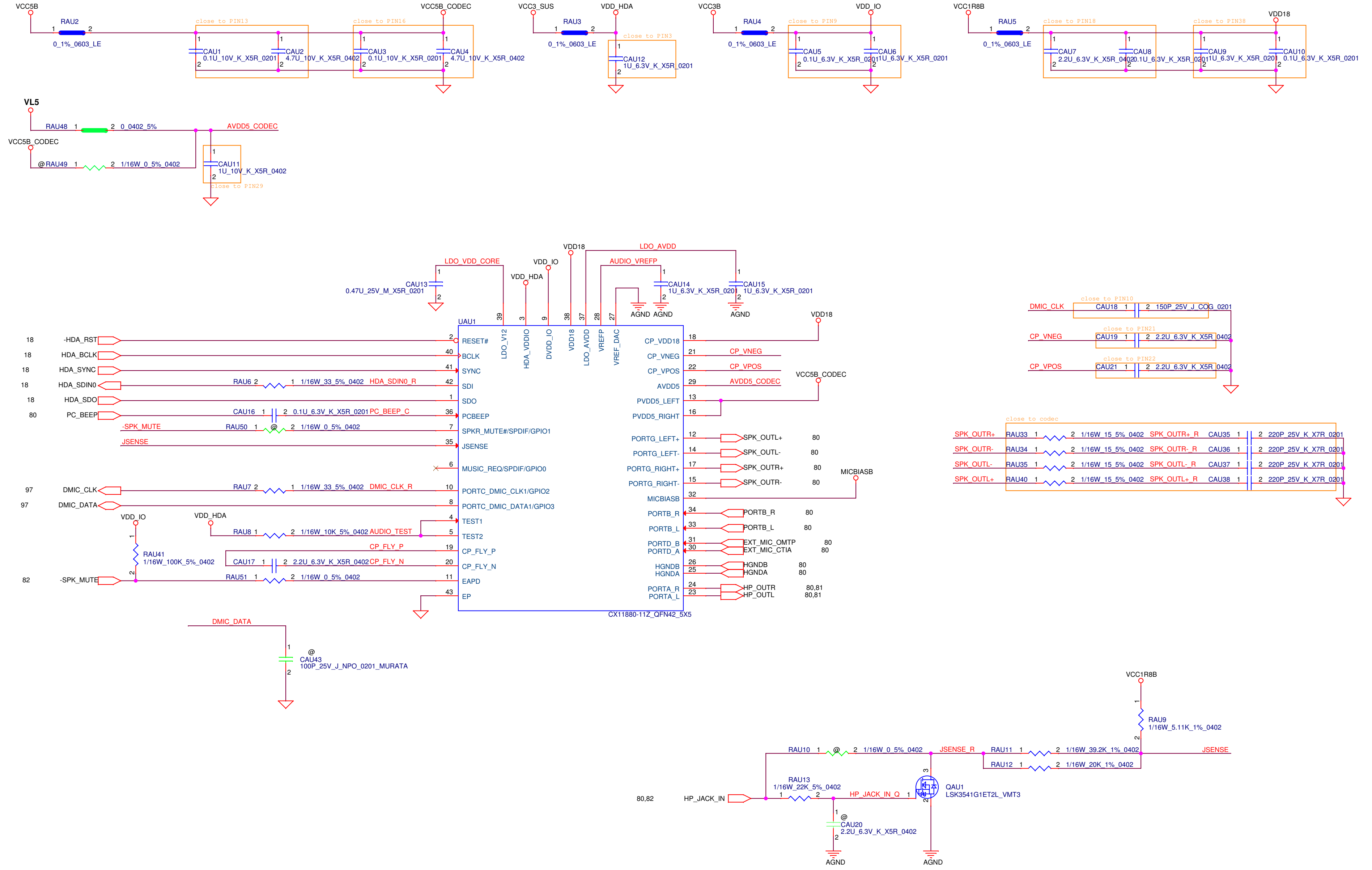
CD : Low => Insertion Card
High => No Card
WP : Low => Write Protection on
High => Write Protection off or No Card

EMC



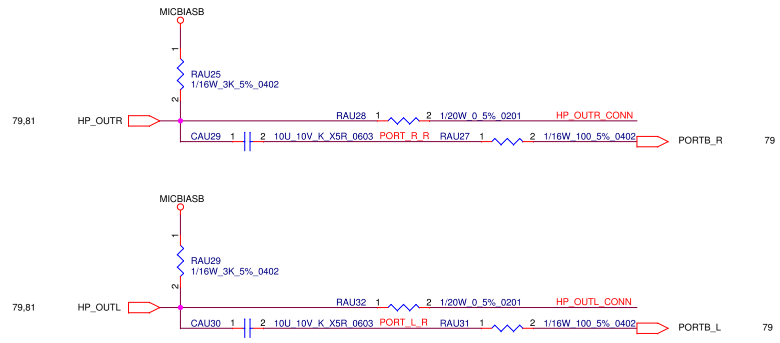
LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 — Title: MEDIA CARD INTERFACE UHS-II
	Date: Monday, April 29, 2019 — Sheet 78 of 142

AUDIO CODEC

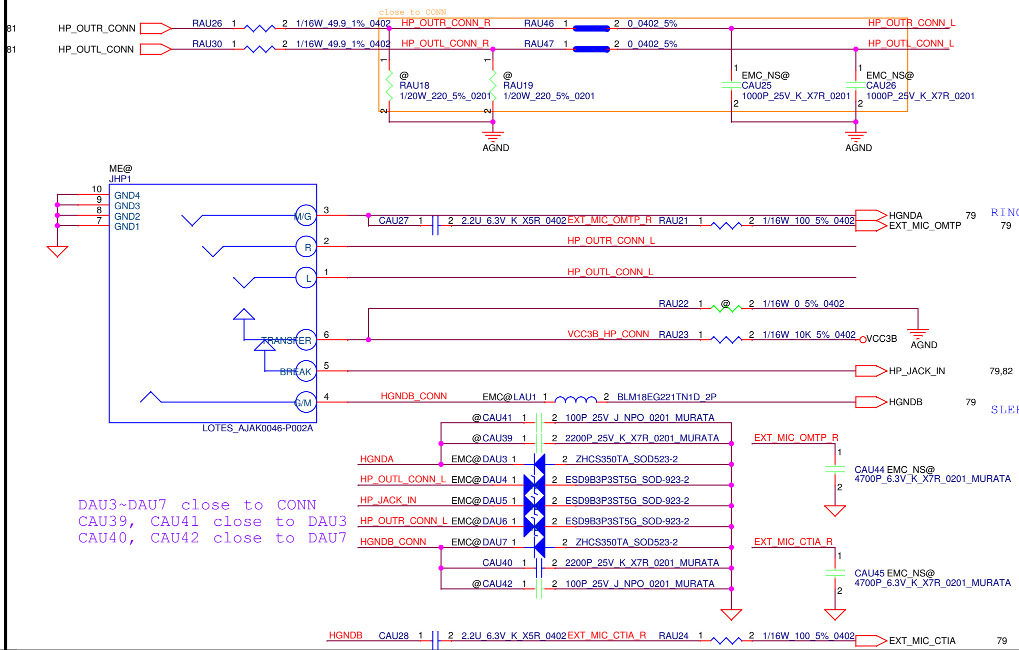


LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 — Title: AUDIO CX11880
	Date: Monday, April 29, 2019 — Sheet 79 of 142

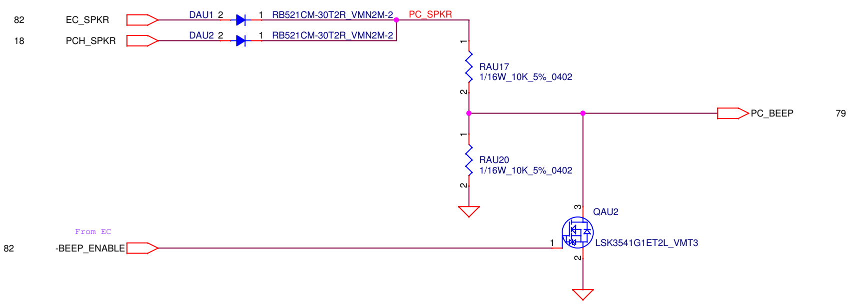
HEAD PHONE/LINE OUT



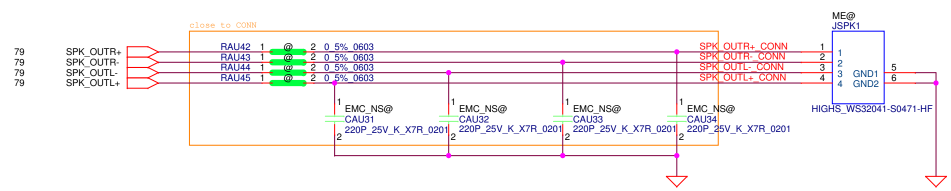
AUDIO JACK/EXT. MIC/LINE IN



PC BEEP



SPEAKER



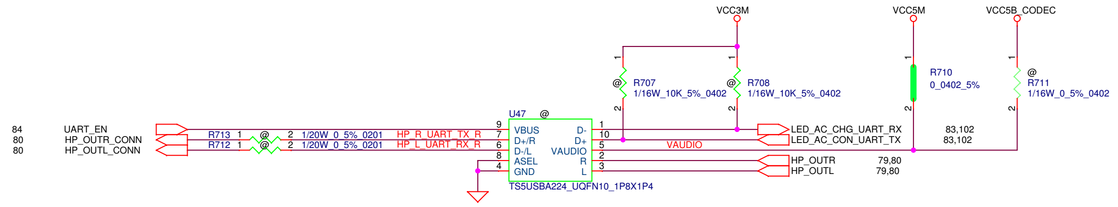
LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev 1.0 | Title: AUDIO CX11880

Date: Monday, April 29, 2019 | Sheet 80 of 142

AUDIO DEBUG PORT



LC Future Center Secret Data	Project Name	Nighthawk-1
LCFC	Rev 1.0	Title AUDIO DEBUG
	Date: Monday, April 29, 2019	Sheet 81 of 142

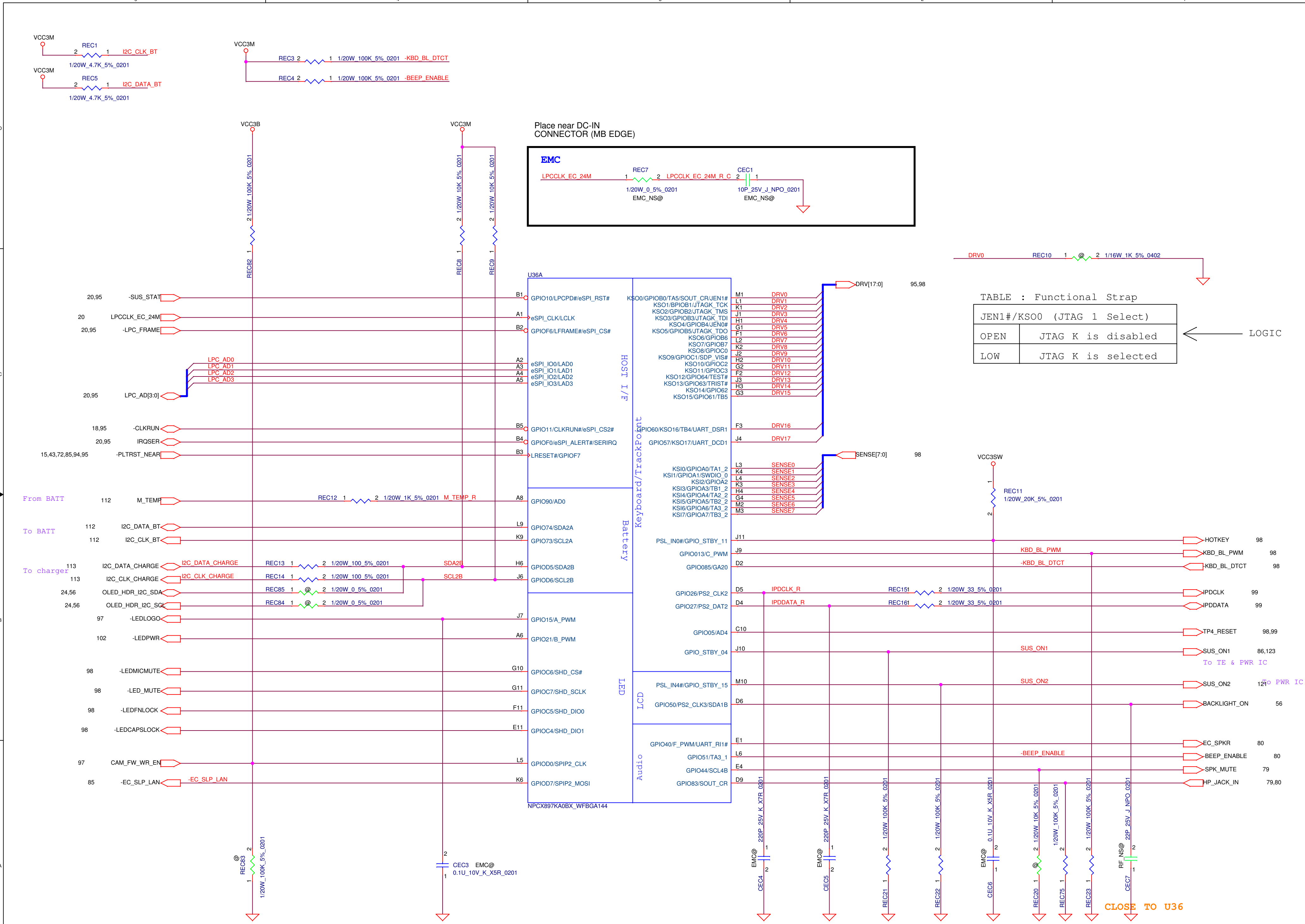


TABLE : Functional Strap

JEN1#/KSO0 (JTAG 1 Select)	
OPEN	JTAG K is disabled
LOW	JTAG K is selected

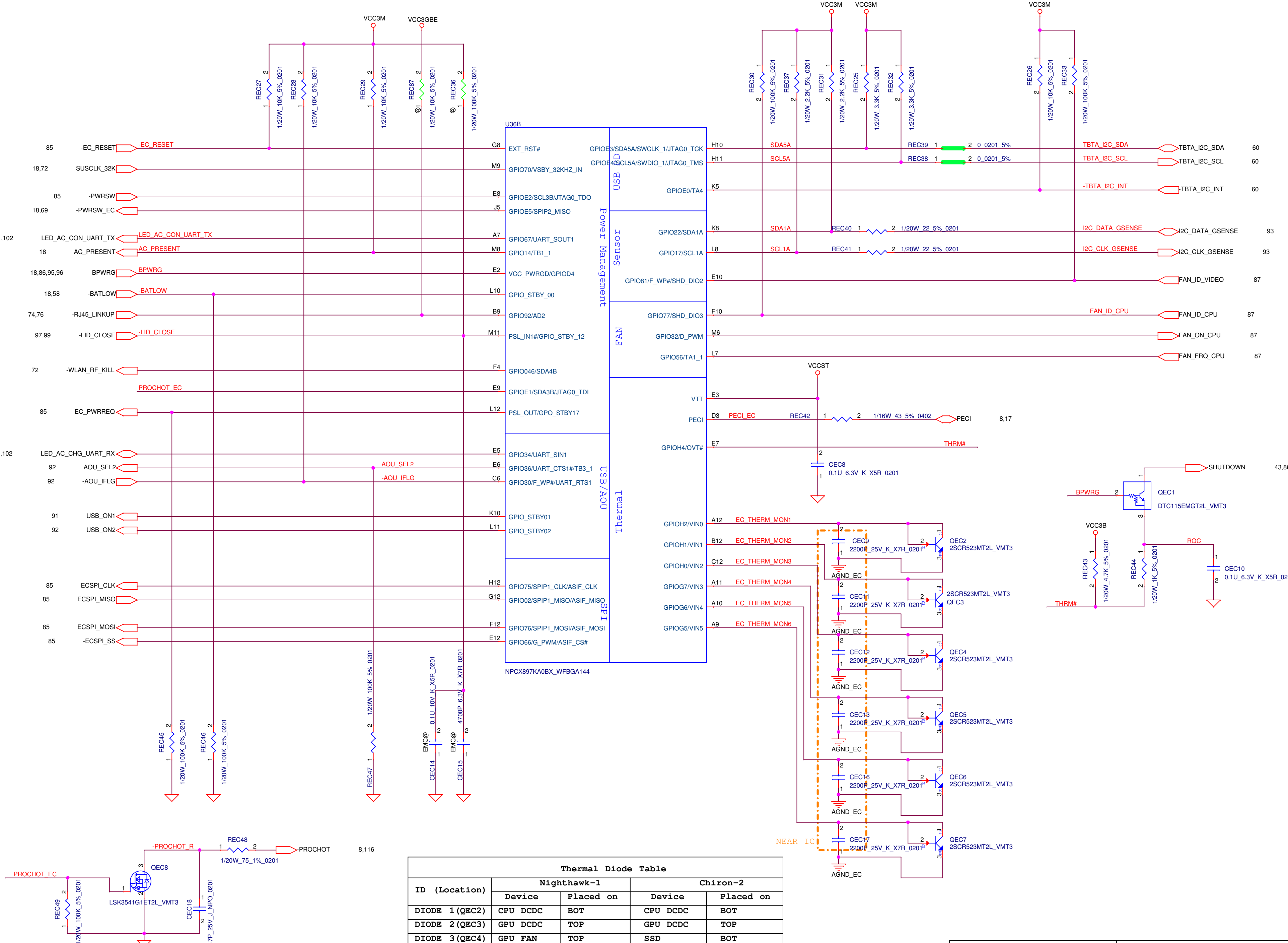
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0

Title: NPCX897KA0BX(1/3)

Date: Monday, April 29, 2019 | Sheet 82 of 142



Thermal Diode Table

ID (Location)	Nighthawk-1		Chiron-2	
	Device	Placed on	Device	Placed on
DIODE 1(QEC2)	CPU DCDC	BOT	CPU DCDC	BOT
DIODE 2(QEC3)	GPU DCDC	TOP	GPU DCDC	TOP
DIODE 3(QEC4)	GPU FAN	TOP	SSD	BOT
DIODE 4(QEC5)	CPU FAN	TOP	GPU FAN	TOP
DIODE 5(QEC6)	DDR DCDC	TOP	CPU FAN	TOP
DIODE 6(QEC7)	SSD	BOT	DIMM	TOP

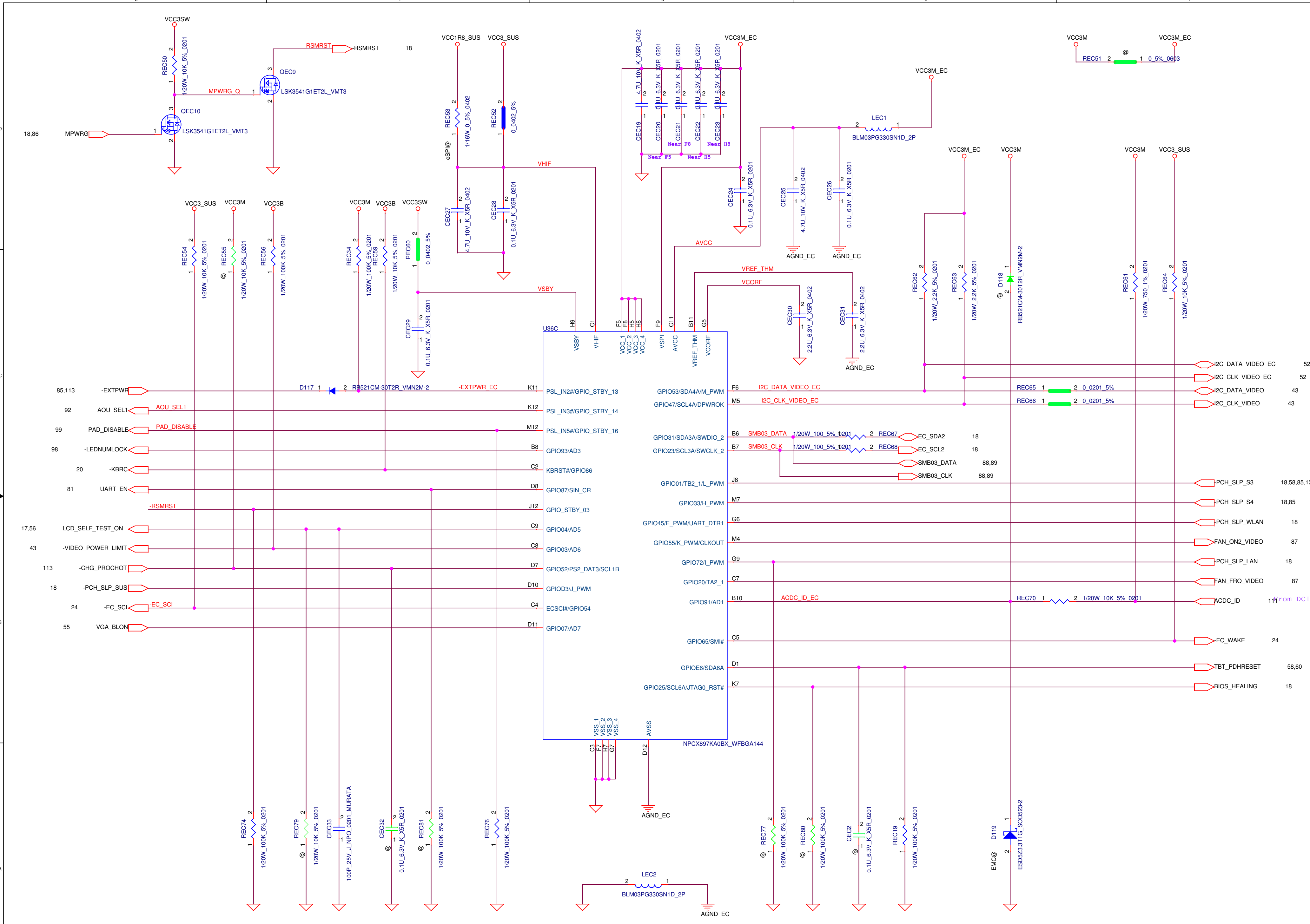
LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev 1.0

Title: NPCX897KA0BX(2/3)

Date: Monday, April 29, 2019



LC Future Center Secret Data

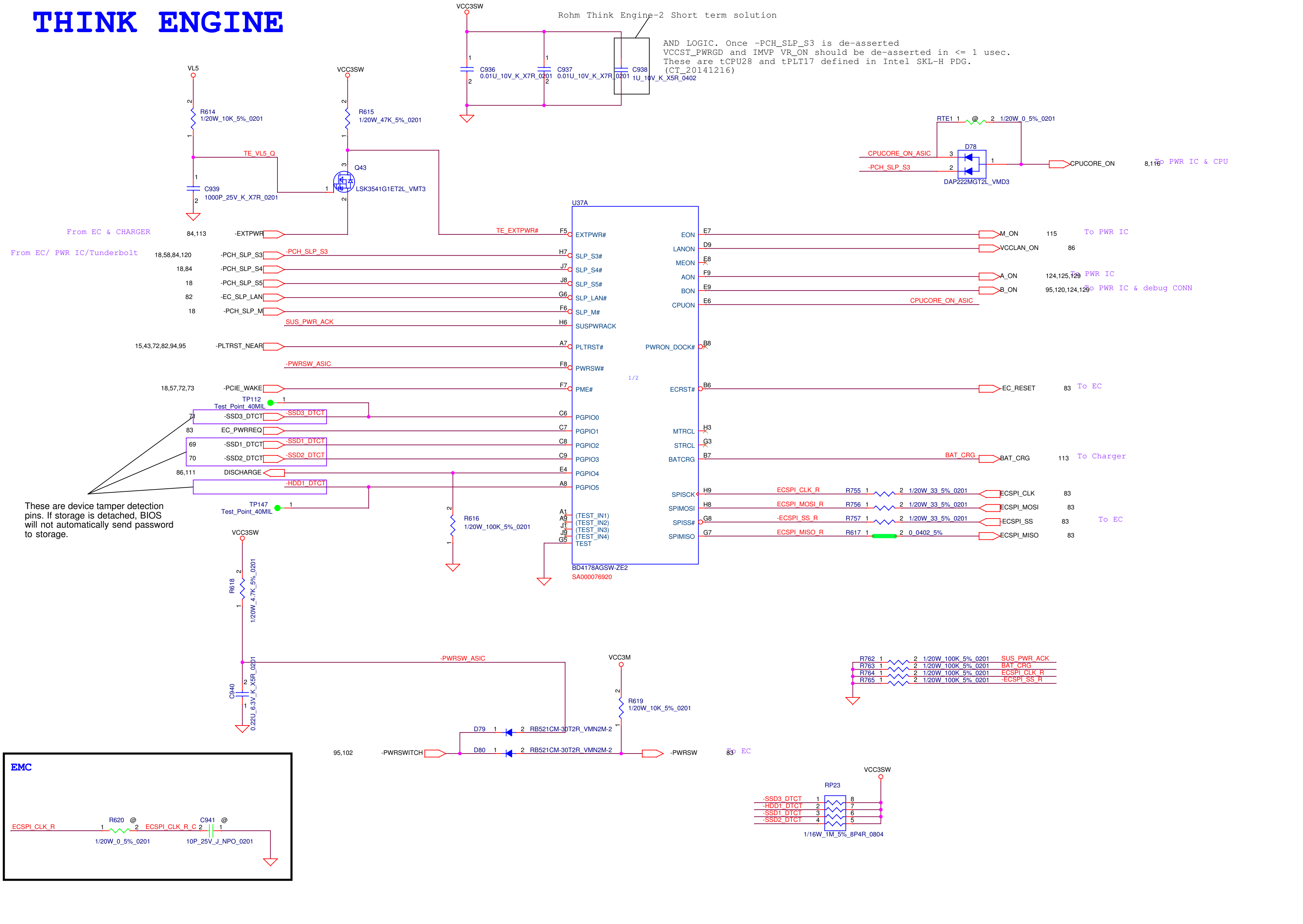
Project Name: Nighthawk-1

Rev 1.0

Title: NPCX897KA0BX(3/3)

Date: Monday, April 29, 2019

THINK ENGINE



LC Future Center Secret Data

LCFC

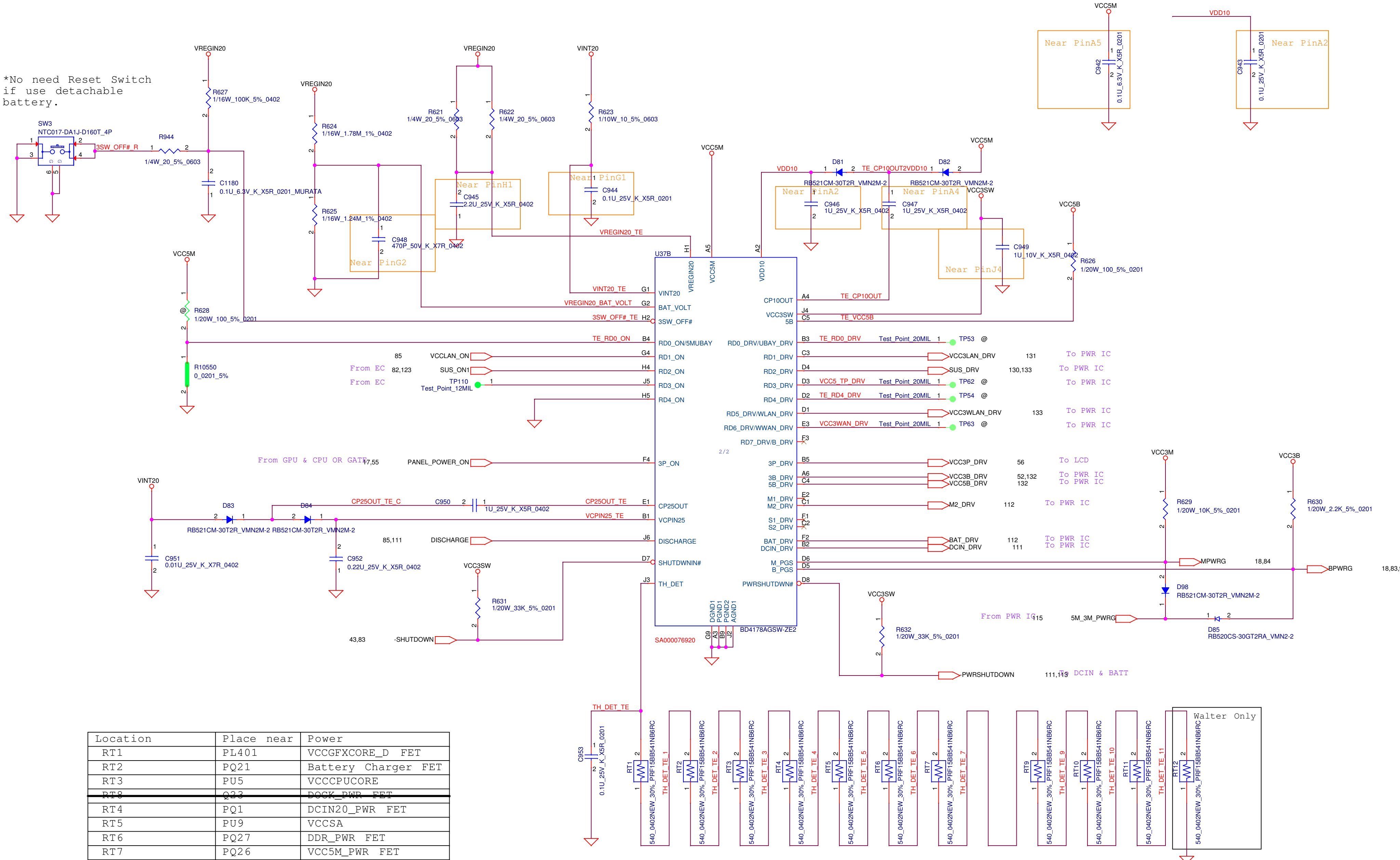
Project Name: Nighthawk-1

Rev 1.0

Title: THINK ENGINE 2(1/2)

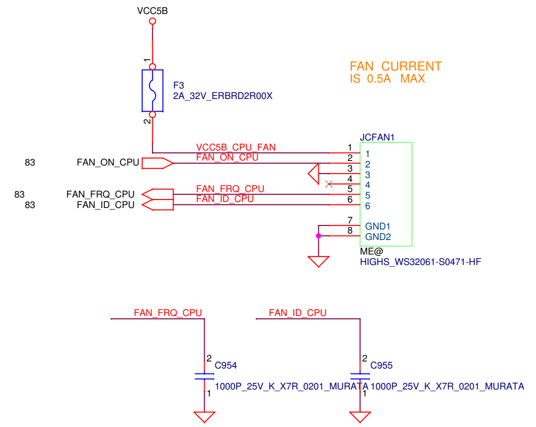
Date: Monday, April 29, 2019

THINK ENGINE

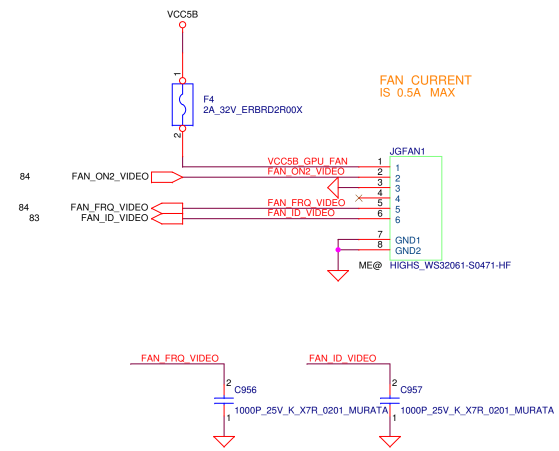


Location	Place near	Power
RT1	PL401	VCCGFXCORE_D FET
RT2	PQ21	Battery Charger FET
RT3	PU5	VCCCPUCORE
~~RT8~~	~~Q23~~	~~DOCK_PWR FET~~
RT4	PQ1	DCIN20_PWR FET
RT5	PU9	VCCSA
RT6	PQ27	DDR_PWR FET
RT7	PQ26	VCC5M_PWR FET
RT9	PQ51	VCC3M_PWR FET
RT10	PQ10	M_BAT_PWR FET
RT11	PU7	VCCGFXCORE_I
RT12	PQ9	Charge FET
~~PRT1(BAT_FET_HOT)~~	~~PQ11~~	~~BAT_IN~~

CPU FAN

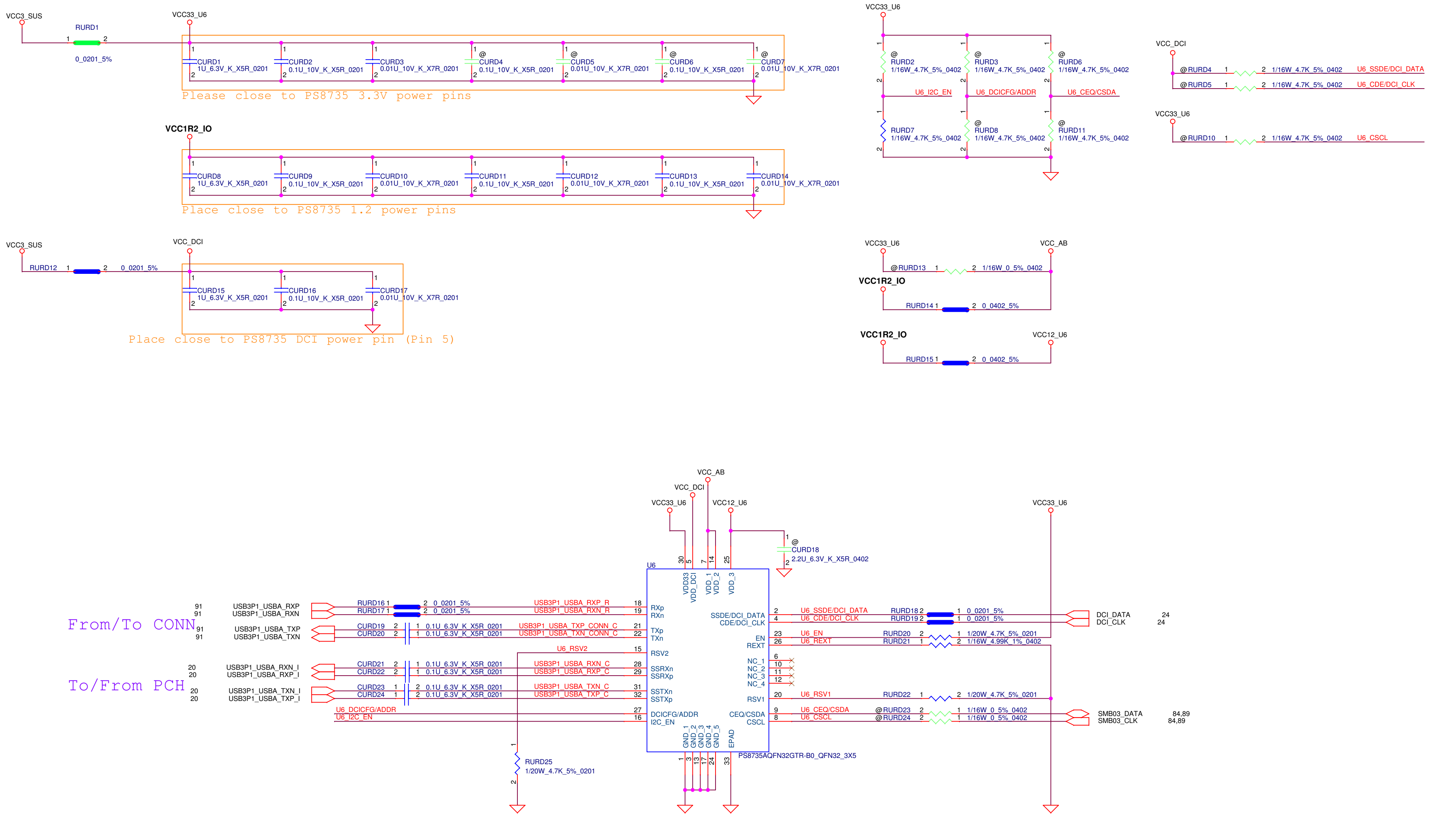


GPU FAN



Project Name	Nighthawk-1
Rev 1.0	Title: FAN CONNECTOR
Date: Monday, April 29, 2019	Sheet 87 of 142

USB3.1 Redriver



LC Future Center Secret Data

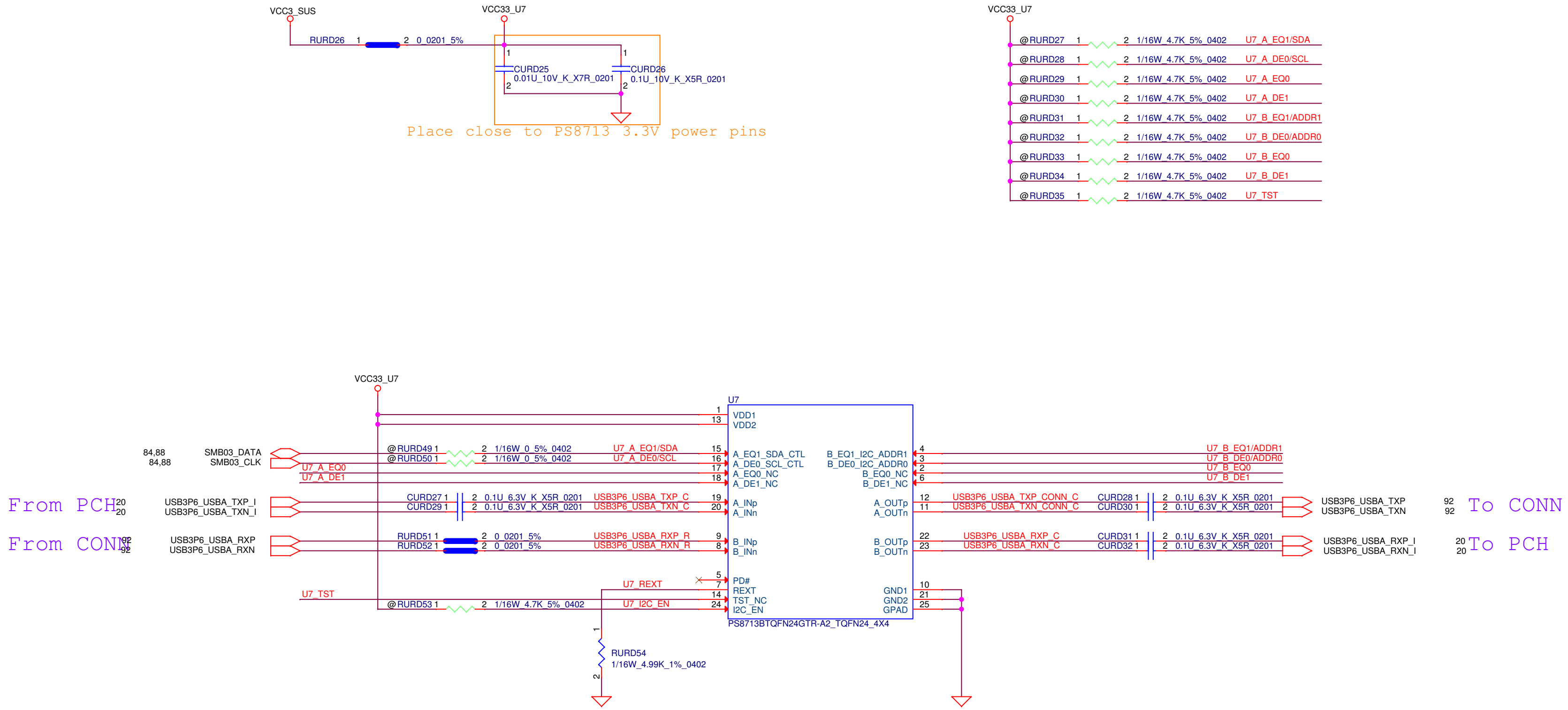
Project Name: Nighthawk-1

Rev 1.0

Title: USB REDRIVER (2/2)

Date: Monday, April 29, 2019

USB3.1 Redriver



LC Future Center Secret Data

Project Name	Nighthawk-1
Rev 1.0	Title: USB REDRIVER (1/2)
Date: Monday, April 29, 2019	Sheet 89 of 142

BLANK

USB3.1 CONN

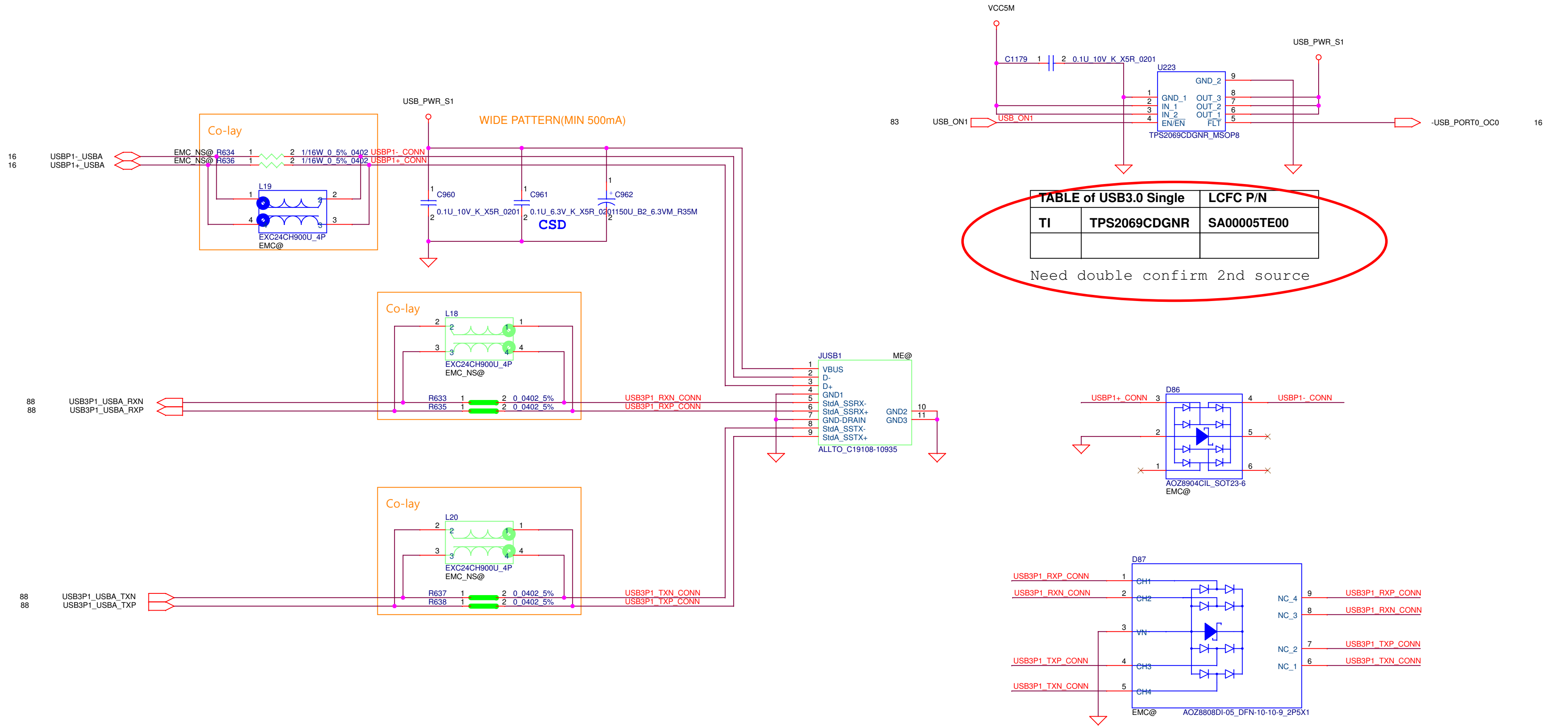


TABLE of USB3.0 Single		LCFC P/N
TI	TPS2069CDGNR	SA00005TE00

Need double confirm 2nd source

D87	1st:Semtech AOZ8808DI-05 DFN-10 (SC300003H00) 2nd:LittelFuse 3th:LittelFuse

LC Future Center Secret Data

Project Name: Nighthawk-1

Rev 1.0

Title: USB POWER/CONNECTOR_1

Date: Monday, April 29, 2019

USB Charger IC

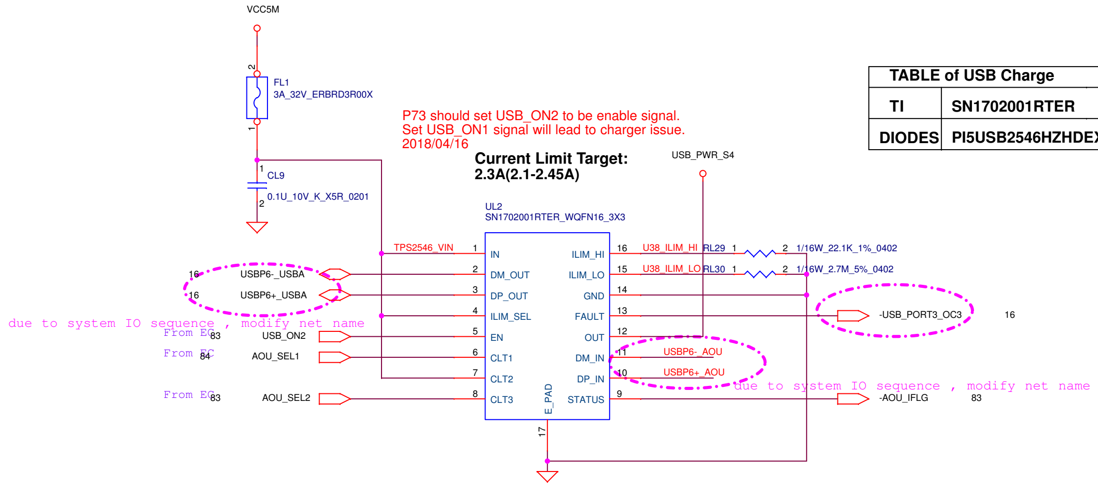
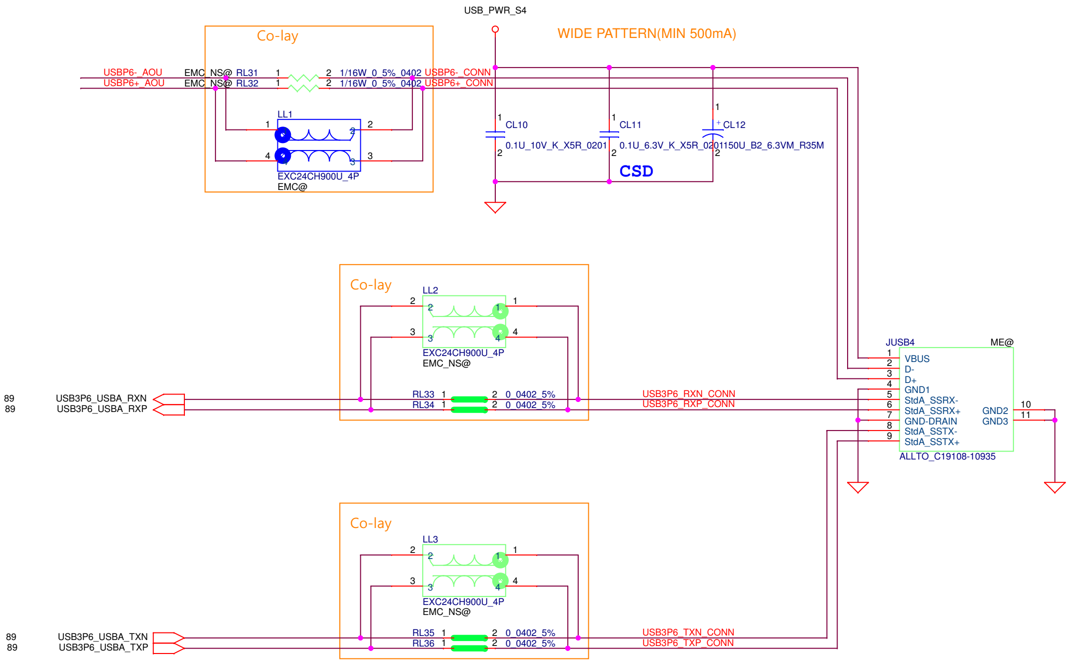
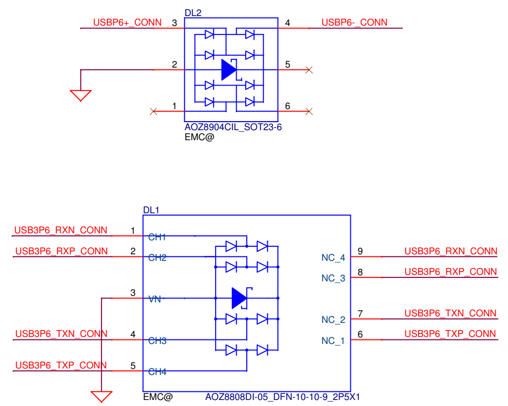


TABLE of USB Charge		LCFC P/N
TI	SN1702001RTER	SA00008HF00
DIODES	PI5USB2546HZHDEX	SA00009D800

USB3.0 CONN





DL1	1st:Semtech AOZ8808DI-05 DFN-10 (SC300003H00) 2nd:LittelFuse 3th:LittelFuse

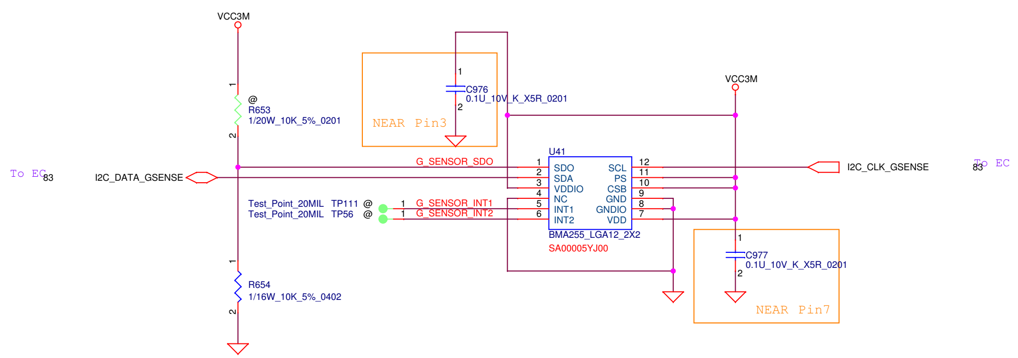
G-SENSOR

TABLE

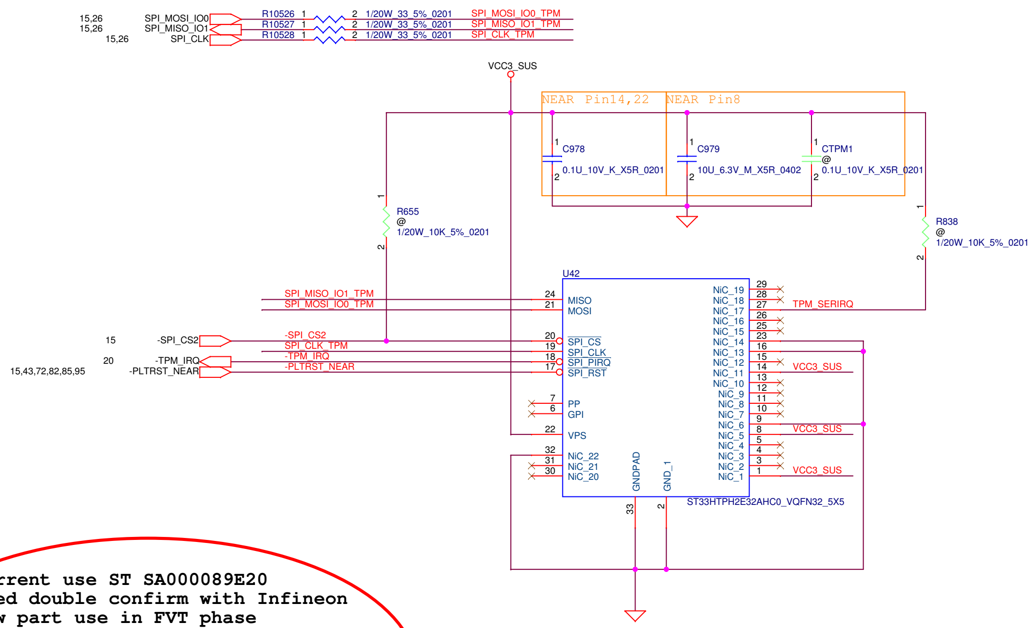
P/N	ADDR_SEL	Address
BMA255	H L	30h (W) & 31h (R) 32h (W) & 33h (R)
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

TABLE of G-Sersor (GSU1)

Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00



TPM



Current use ST SA000089E20
Need double confirm with Infineon
new part use in FVT phase

TABLE of TPM (U42)

Vendor	P/N	LCFC P/N	Valid through
Infineon	SLB9670VQ2.0FW7.85	SA000075L90	
ST Micro	ST33HTPH2E32AHC0	SA000089E20	2020/Apr/01

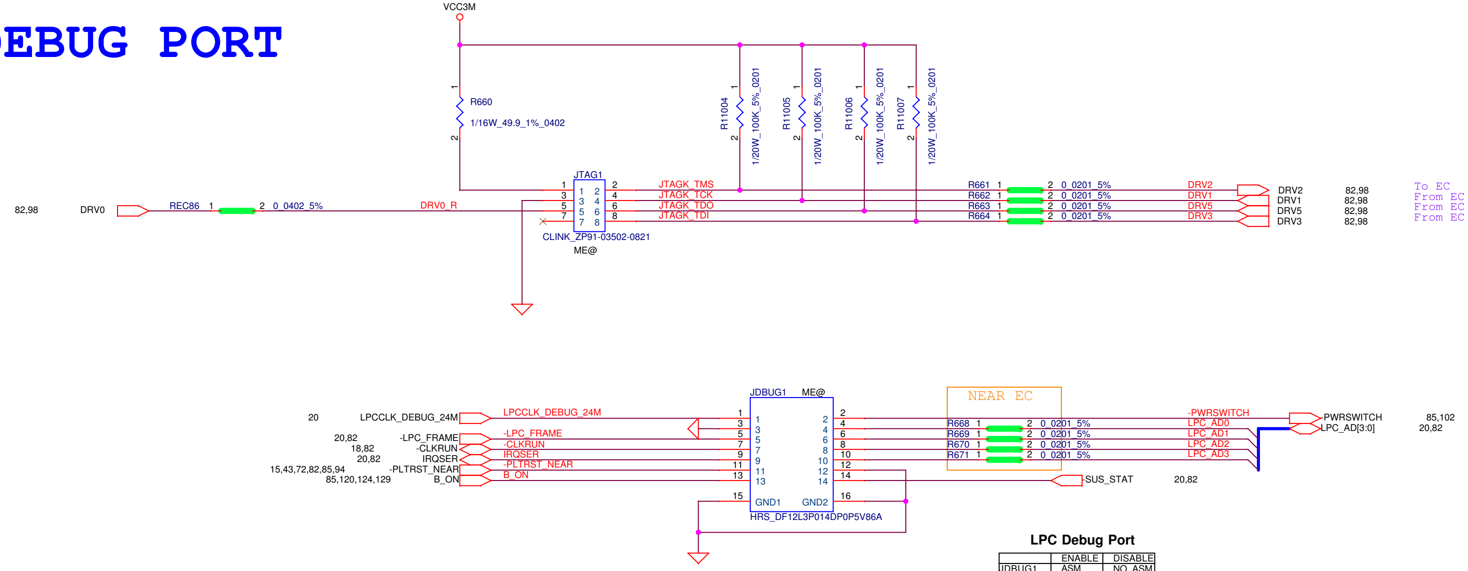
TABLE

Pin No	TCG PTP Spec (v38)	Main Source: Infineon SLB9670VQ2.0FW7.63 SA000075L50	2nd Source: ST Micro ST33HTPH2E32AHB4 SA000089E10
1	VDD	VDD	NC
2	GND	GND	GND
3	GPIO	NC	NC
4	GPIO	NC	PP
5	NC	NC	NC
6	VNC/GPIO	GPIO	NC
7	GPIO/VDD	PP	GPIO
8	VDD	VDD	NC
9	GND	GND	NC
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	VNC/GPIO	NC	NC
14	VDD	NC	NC
15	NC	NC	NC
16	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	VNC/GPIO	NC	NC
30	VNC/GPIO	NC	NC
31	VNC	NC	NC
32	GND	GND	NC

EMC

LC Future Center Secret Data
Project Name: Nighthawk-1
Rev 1.0
Title: DISCRETE TPM 2.0
Date: Monday, April 29, 2019
Sheet 94 of 142

LPC DEBUG PORT

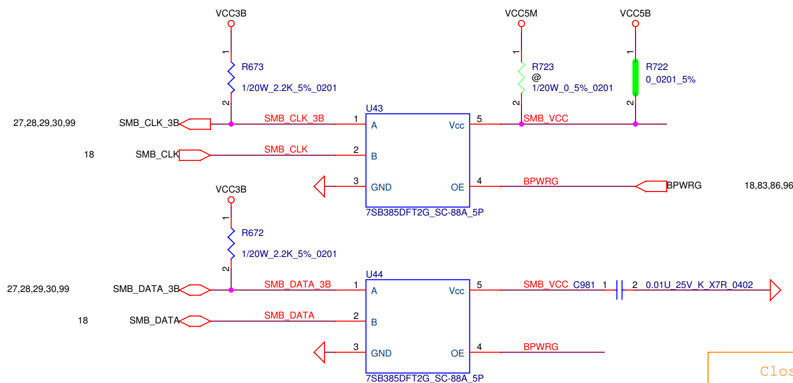


LPC Debug Port

	ENABLE	DISABLE
JDBUG1	ASM	NO_ASM
DBUGR8	ASM	NO_ASM
DBUGR9	ASM	NO_ASM
DBUGR10	ASM	NO_ASM
DBUGR11	ASM	NO_ASM

LOGIC

SMBUS SWITCH



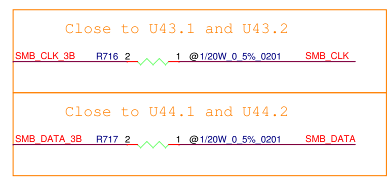
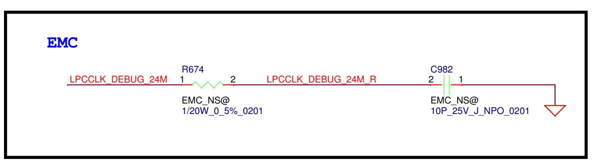


TABLE of U43/U44

Vendor	P/N	LCFC P/N
~~TOSHIBA~~	~~TC7SB385FU~~	~~SA00005US0L~~
ON	7SB385DFT2G	SA00007CW00



LC Future Center Secret Data	Project Name: Nighthawk-1
Rev 1.0	Title: SMBUS SWITCH/LPC DEBUG PORT
Date: Monday, April 29, 2019	Sheet 95 of 142

NFC

SMART CARD

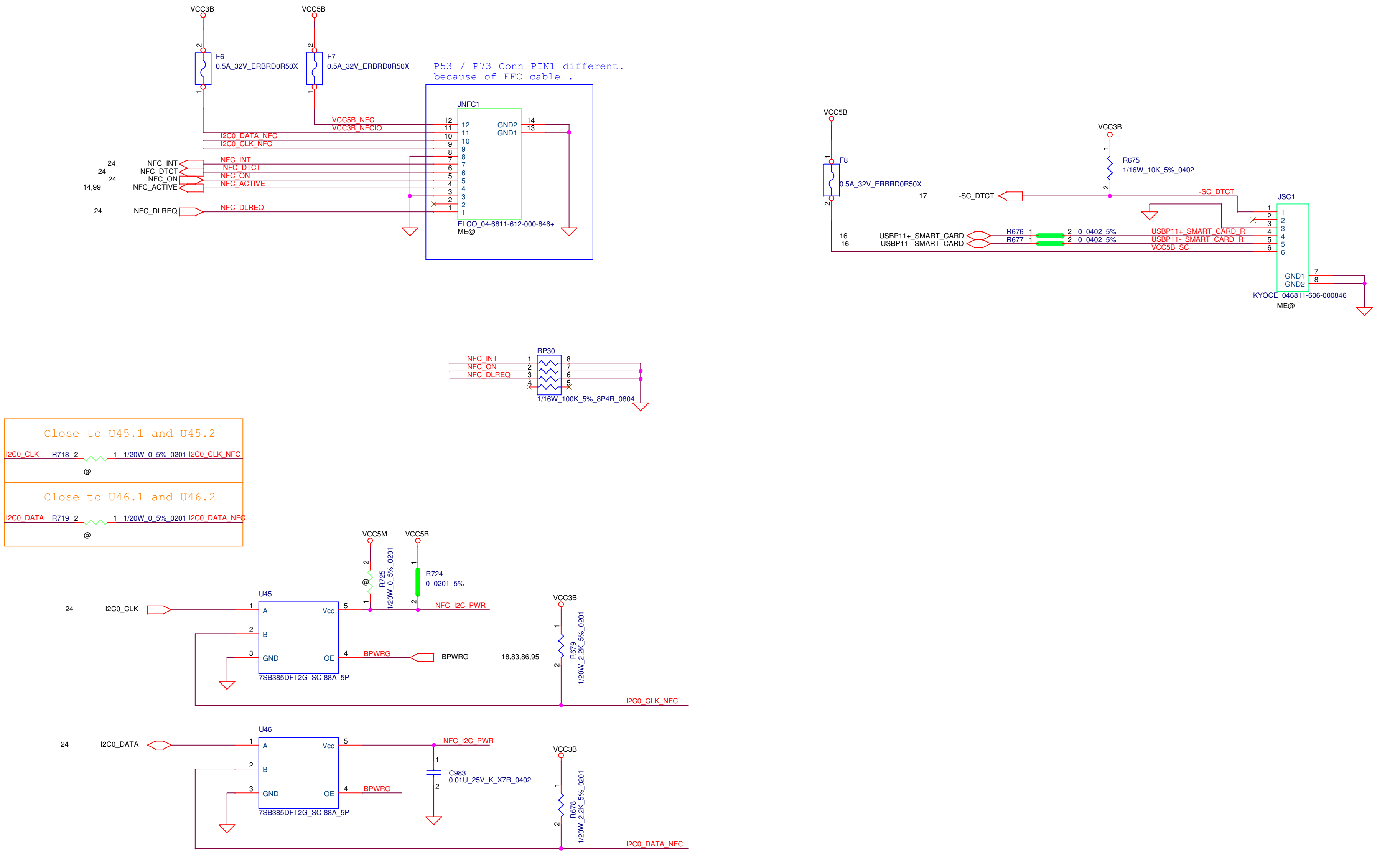


TABLE of U45/U46		
Vendor	P/N	LCFC P/N
~~TOSHIBA~~	~~TC7SB385FU~~	~~SA00005US0J~~
ON	7SB385DFT2G	SA00007CW00

U45, U46 Symbol : SA00005US0J

LC Future Center Secret Data

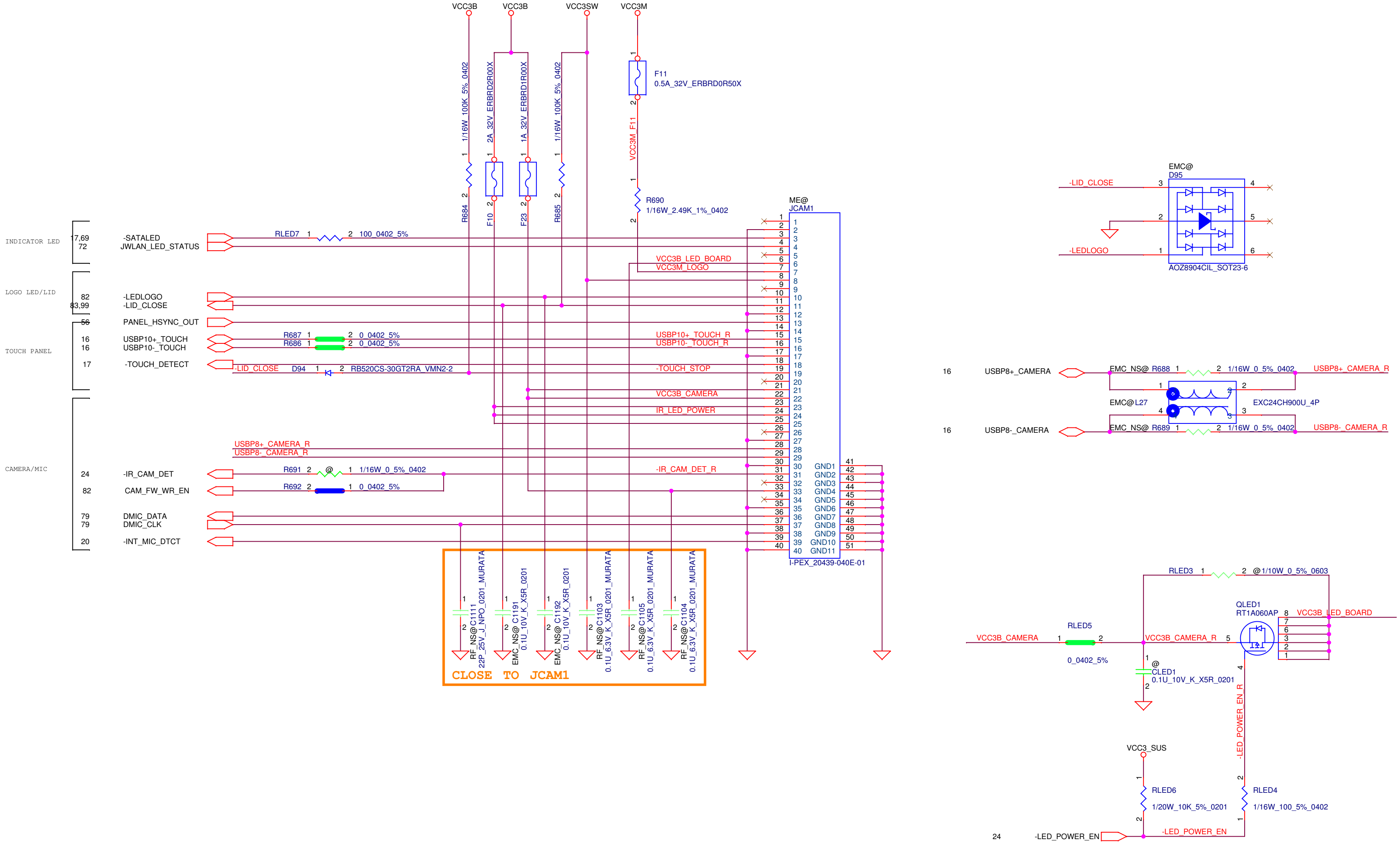
Project Name: *Nighthawk-1*

Rev 1.0

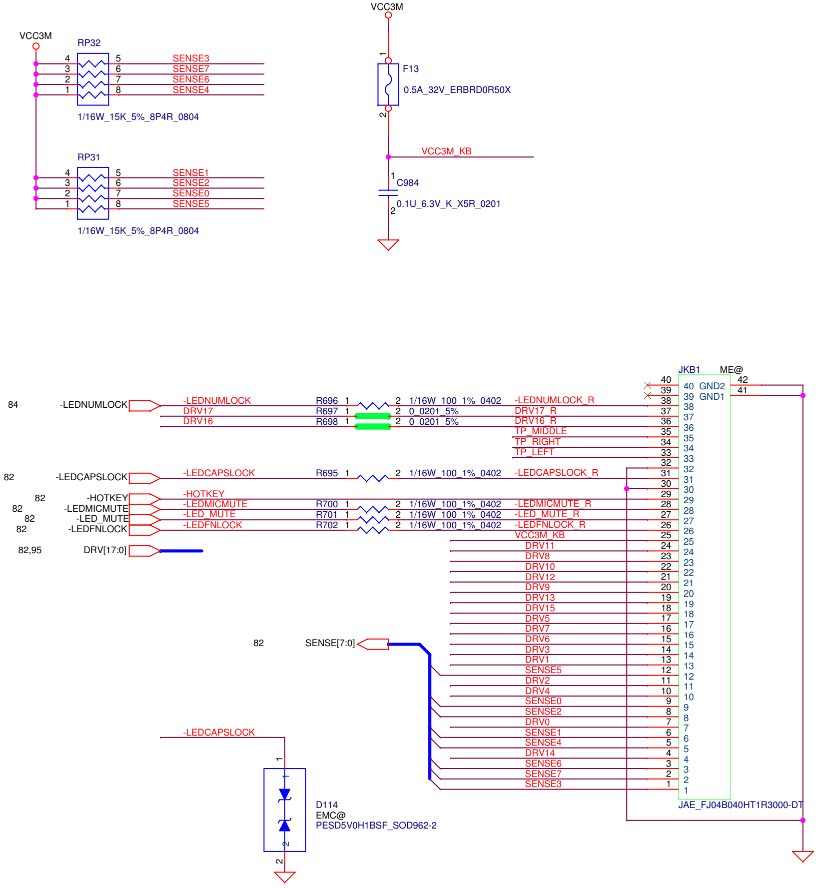
Title: *SMART CARD/NFC/Color Conn*

Date: Monday, April 29, 2019 Sheet 96 of 142

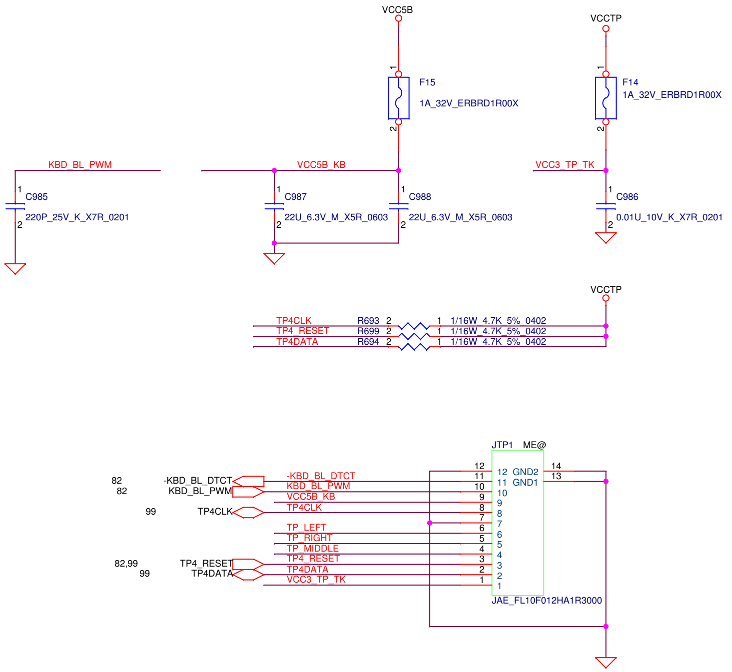
CAMERA/TOUCH



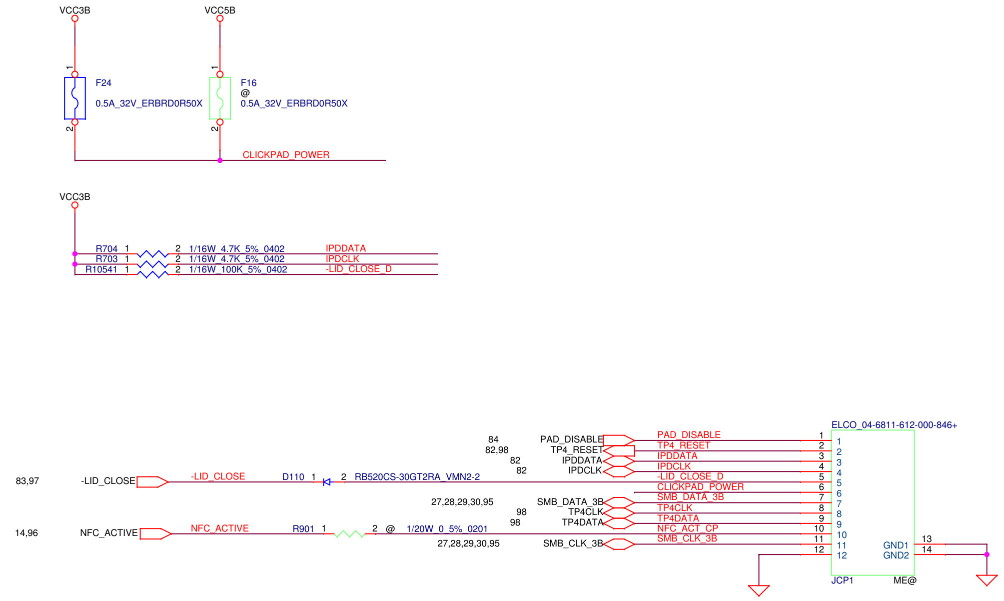
KEYBOARD



TRACK POINT



CLICK PAD



LC Future Center Secret Data

Project Name

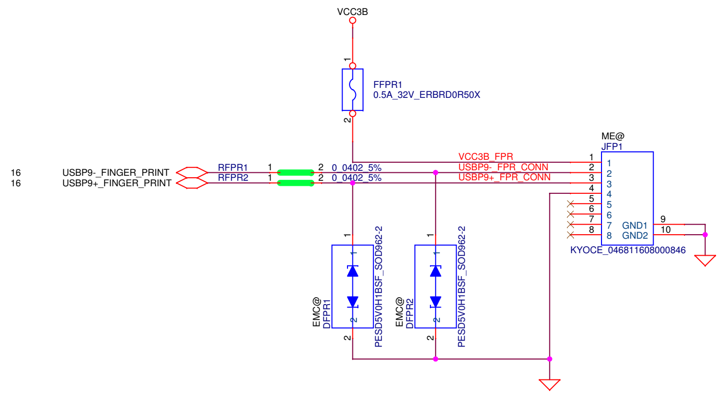
Nighthawk-1

Rev 1.0

Title **CLICK PAD**

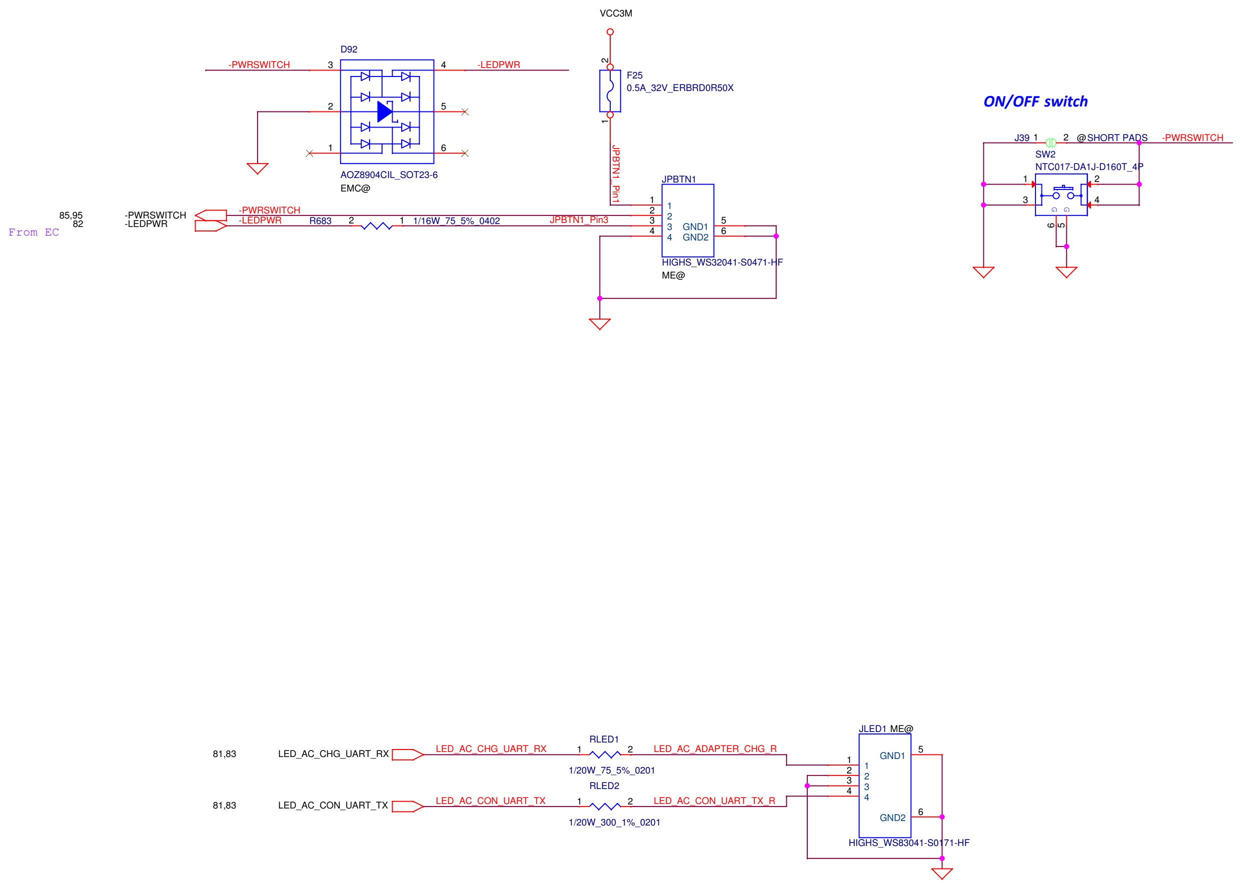
Date: Monday, April 29, 2019

FINGERPRINT



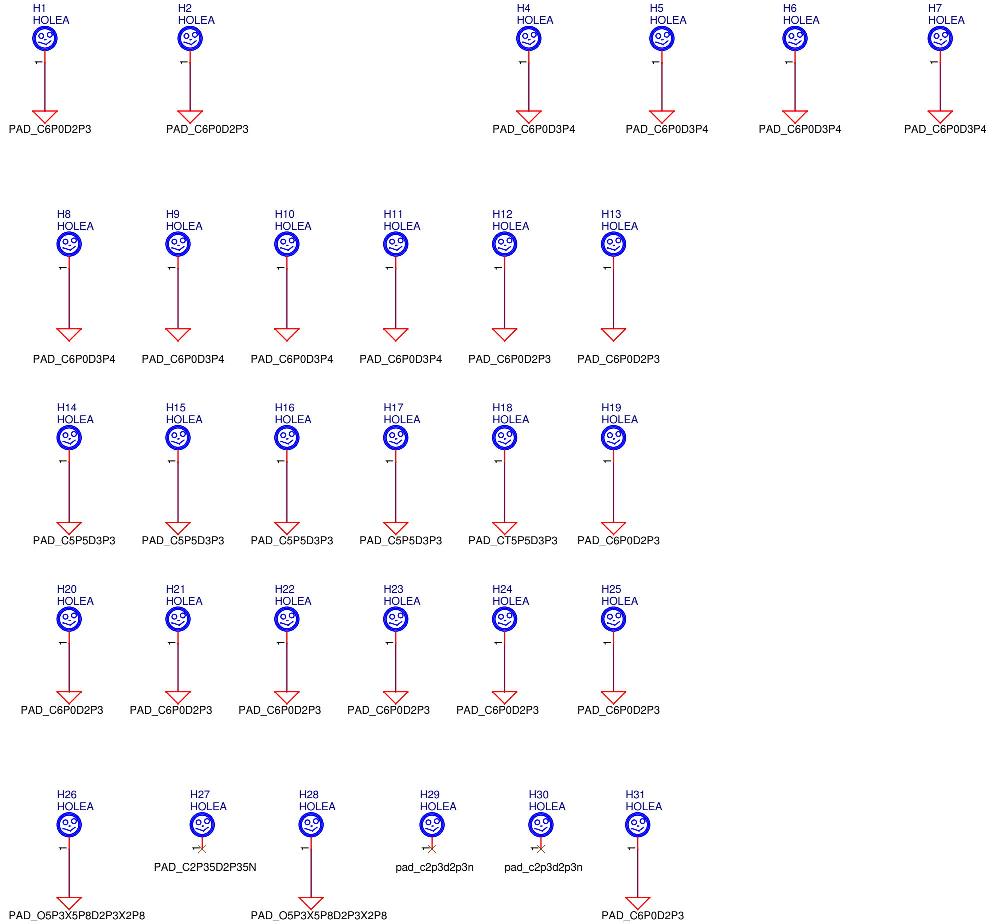
LC Future Center Secret Data

Project Name	Nighthawk-1
Rev 1.0	Title: FINGERPRINT
Date: Monday, April 29, 2019	Sheet 100 of 142

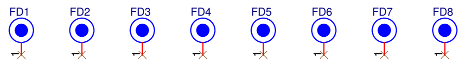


LC Future Center Secret Data	Project Name	Nighthawk-1
LCFC	Rev 1.0	Title P53 IO BOARD CONN
	Date: Monday, April 29, 2019	Sheet 102 of 142

Nighthawk Unique



PCB Fedical Mark PAD



LC Future Center Secret Data

Project Name

Nighthawk-1

Rev 1.0

Title

BLANK

Date: Monday, April 29, 2019

5 4 3 2 1

D

C

B

A

LC Future Center Secret Data	Project Name: Nighthawk-1
LCFC	Rev 1.0 · Title: BLANK
	Date: Monday, April 29, 2019 · Sheet 106 of 142

LC Future Center Secret Data

Project Name

Nighthawk-1

Rev 1.0

Title **BLANK**

Date: Monday, April 29, 2019

LC Future Center Secret Data	Project Name	
LCFC	Nighthawk-1	
	Rev 1.0	Title BLANK
	Date: Monday, April 29, 2019	Sheet 108 of 142

LC Future Center Secret Data

Project Name

Nighthawk-1

Rev	Title
1.0	**BLANK**

Date: Monday, April 29, 2019

5 4 3 2 1

D

C

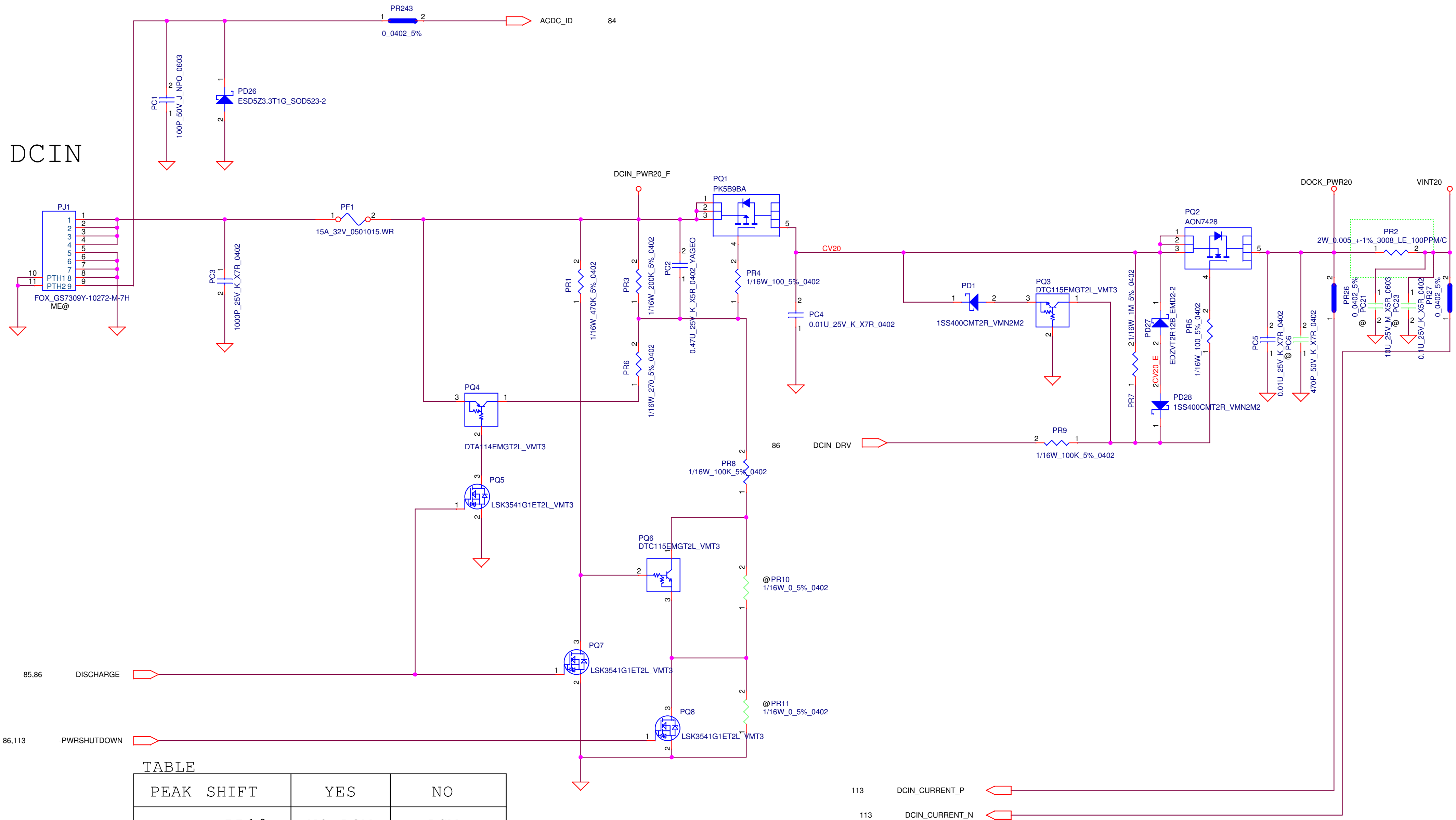
B

A

LC Future Center Secret Data	Project Name: *Nighthawk-1*
LCFC	Rev 1.0 — Title: **BLANK**
	Date: Monday, April 29, 2019 — Sheet 110 of 142

5 4 3 2 1

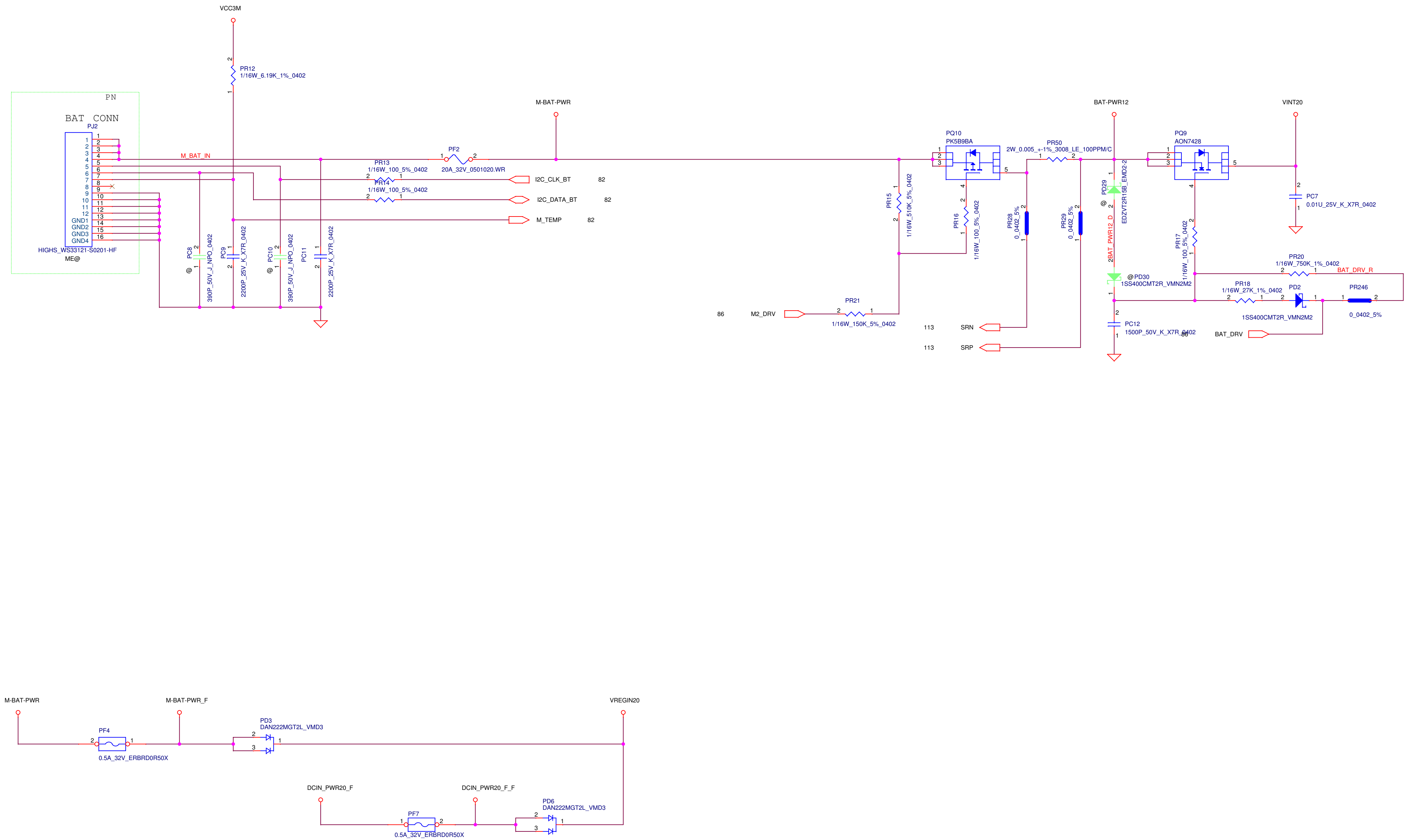
DCIN



TABLE

PEAK SHIFT	YES	NO
PR10	NO-ASM	ASM
PR1	ASM	NO-ASM
PQ6	ASM	NO-ASM
PQ7	ASM	NO-ASM

↑
LOGIC



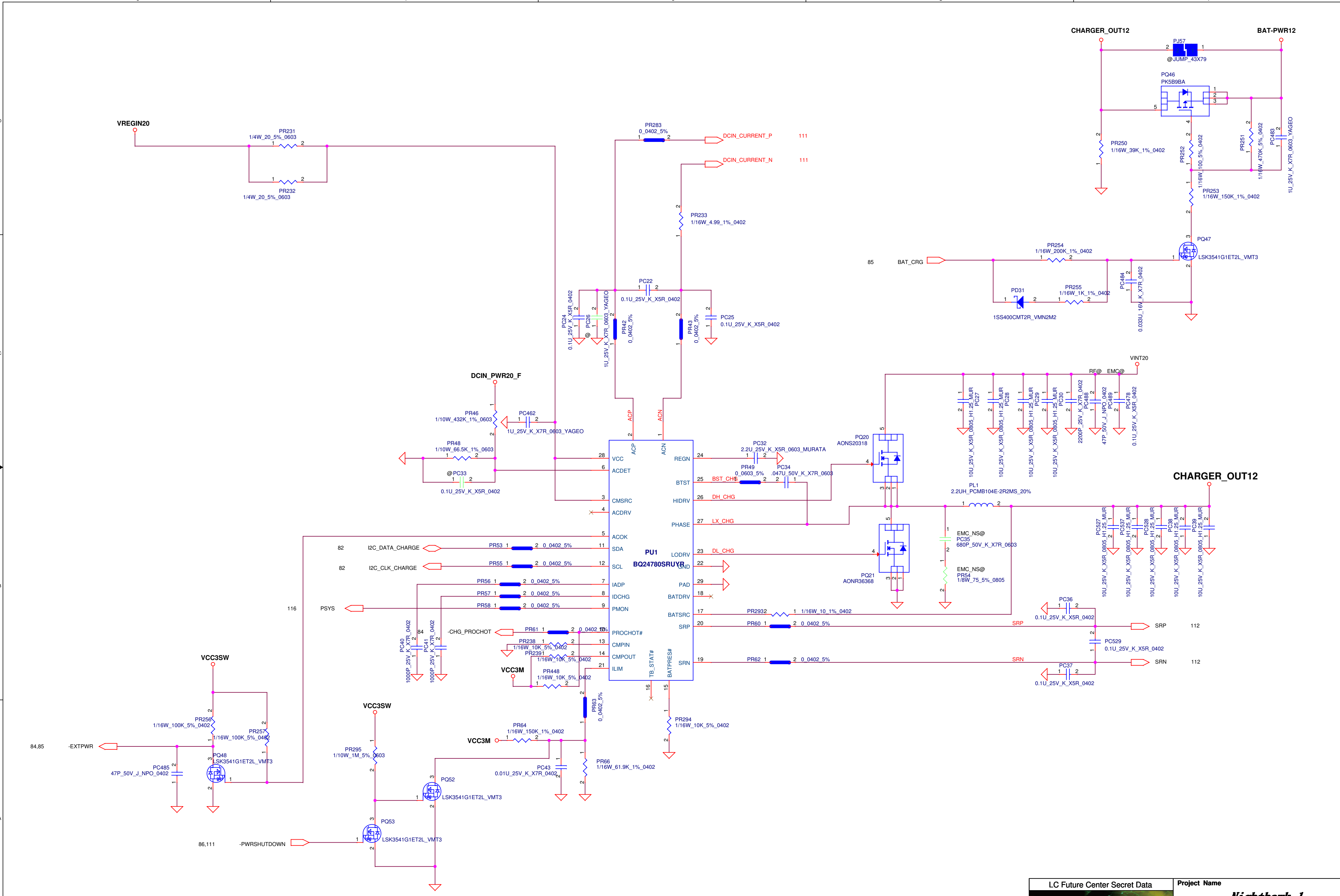
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev: 0.1

Title: BATTERY INPUT

Date: Monday, April 29, 2019



LC Future Center Secret Data

LCFC

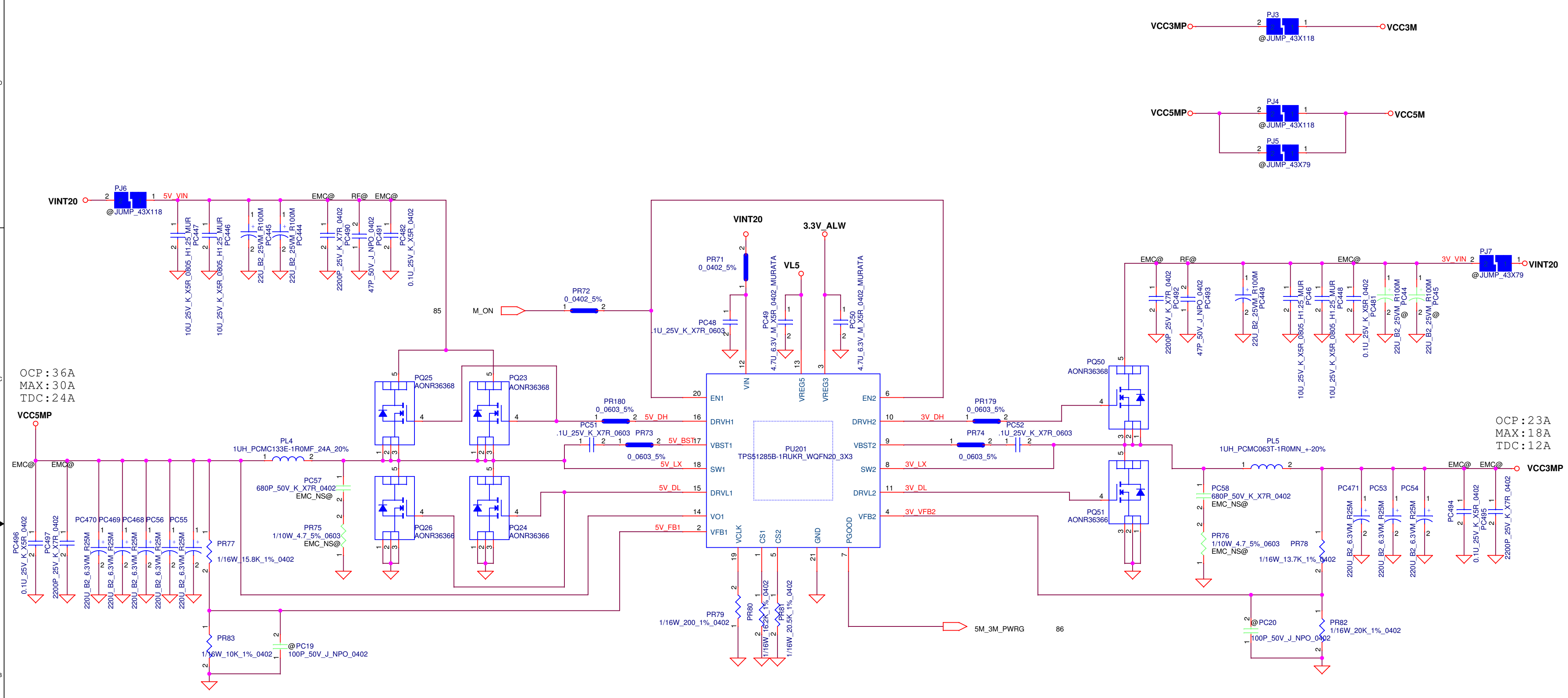
Project Name: Nighthawk-1

Rev 0.1

Title: BATTERY CHARGER

Date: Monday, April 29, 2019

BLANK



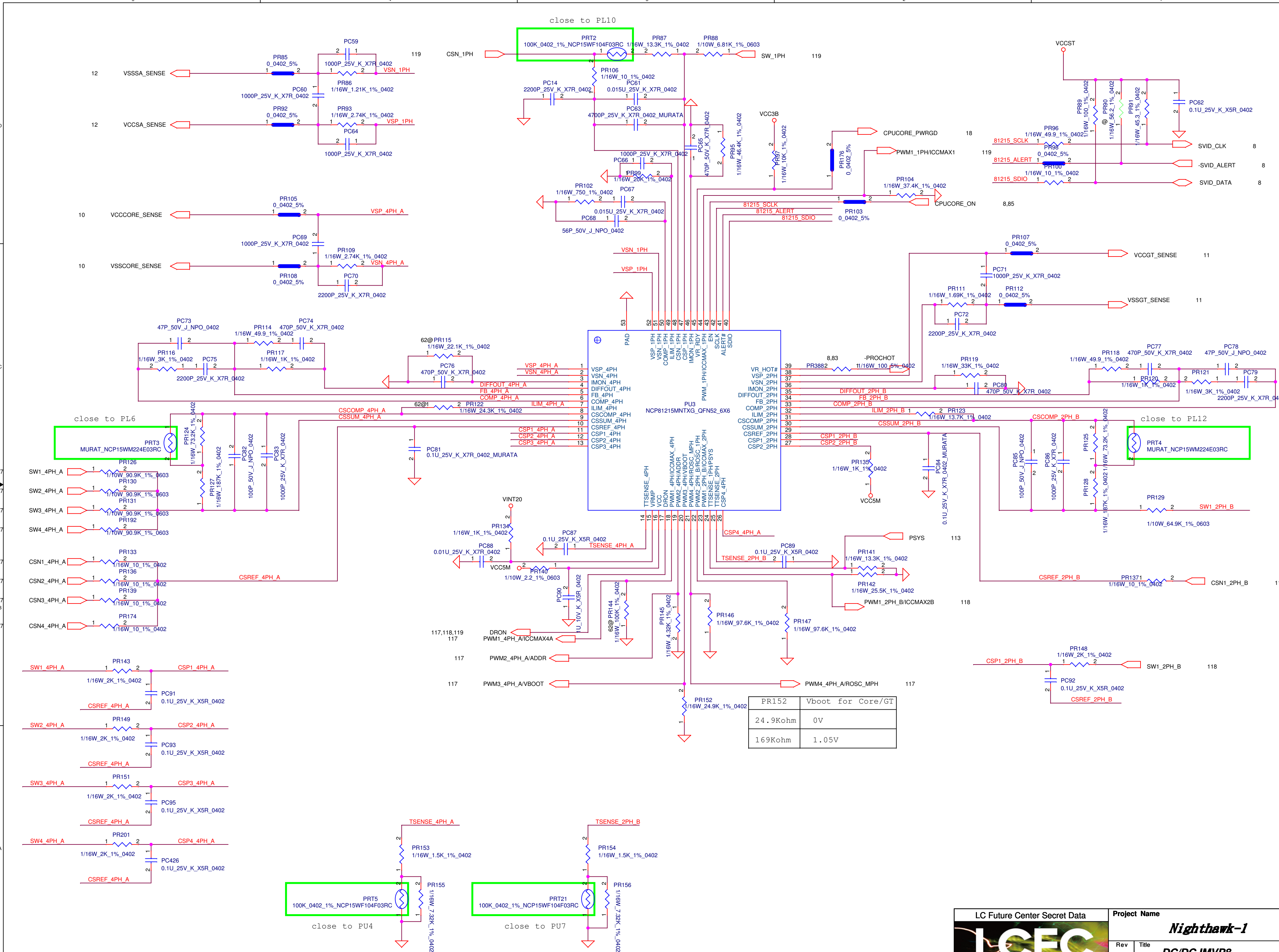
LC Future Center Secret Data

Project Name: Nighthawk-1

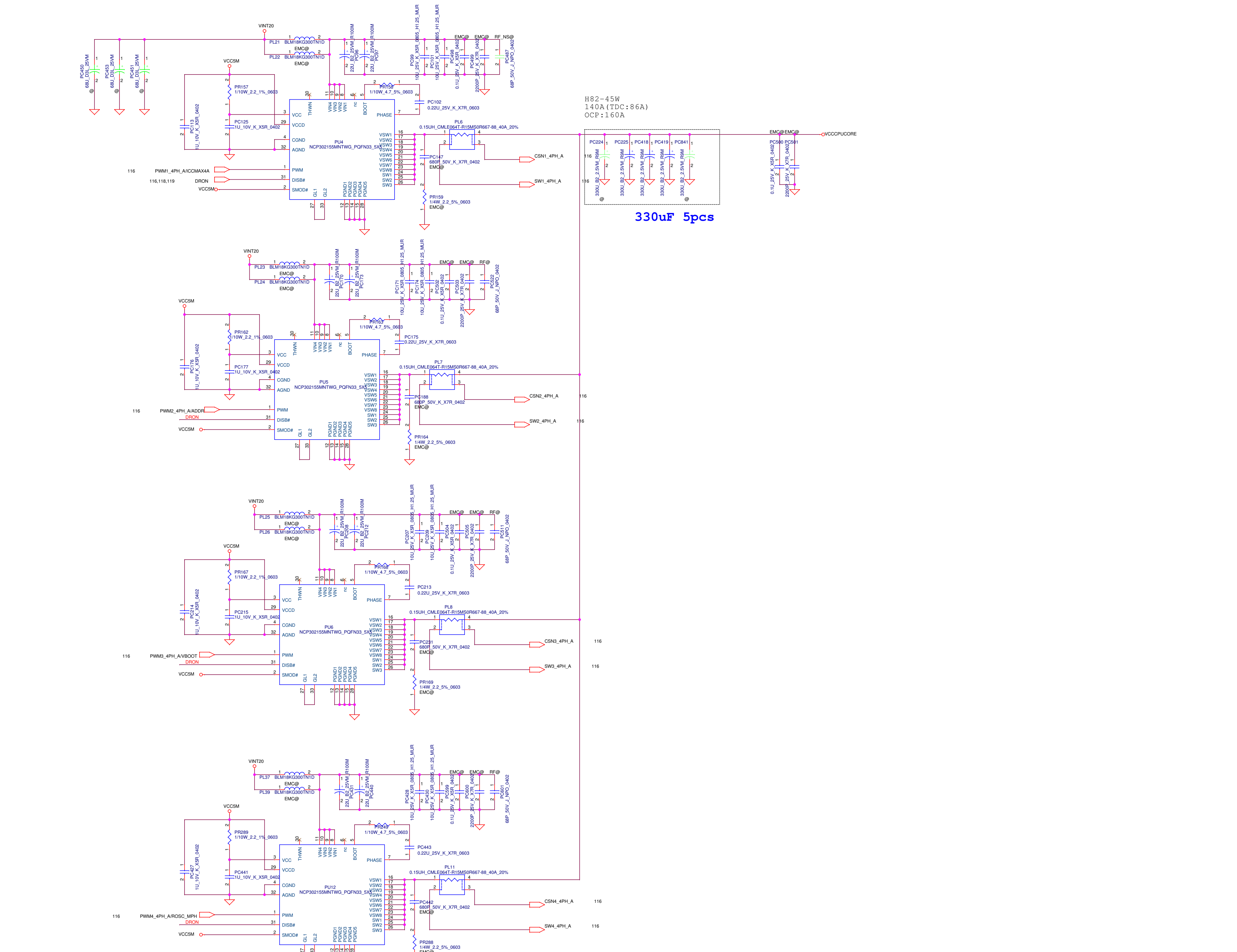
Rev 0.1

Title: DC/DC VCC5M/VCC3M

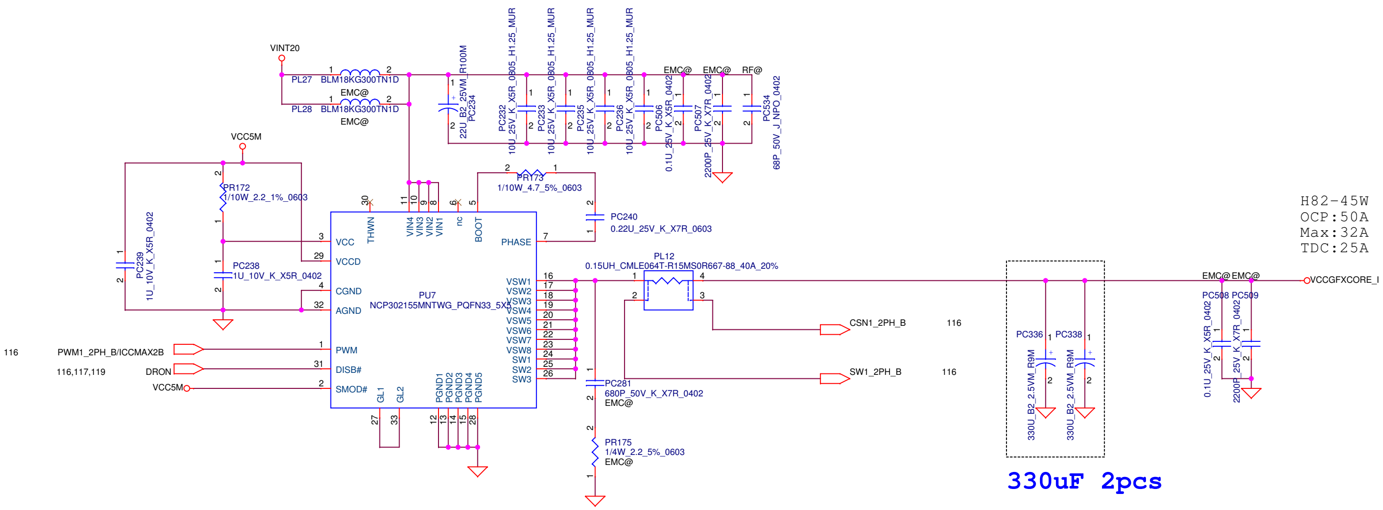
Date: Monday, April 29, 2019



PR152	Vboot for Core/GT
24.9Kohm	0V
169Kohm	1.05V



LC Future Center Secret Data	Project Name	Nighthawk-1
Rev 0.1	Title	DC/DC VCCPUCORE
Date: Monday, April 29, 2019	Sheet 117 of 142	



LC Future Center Secret Data

LCFC

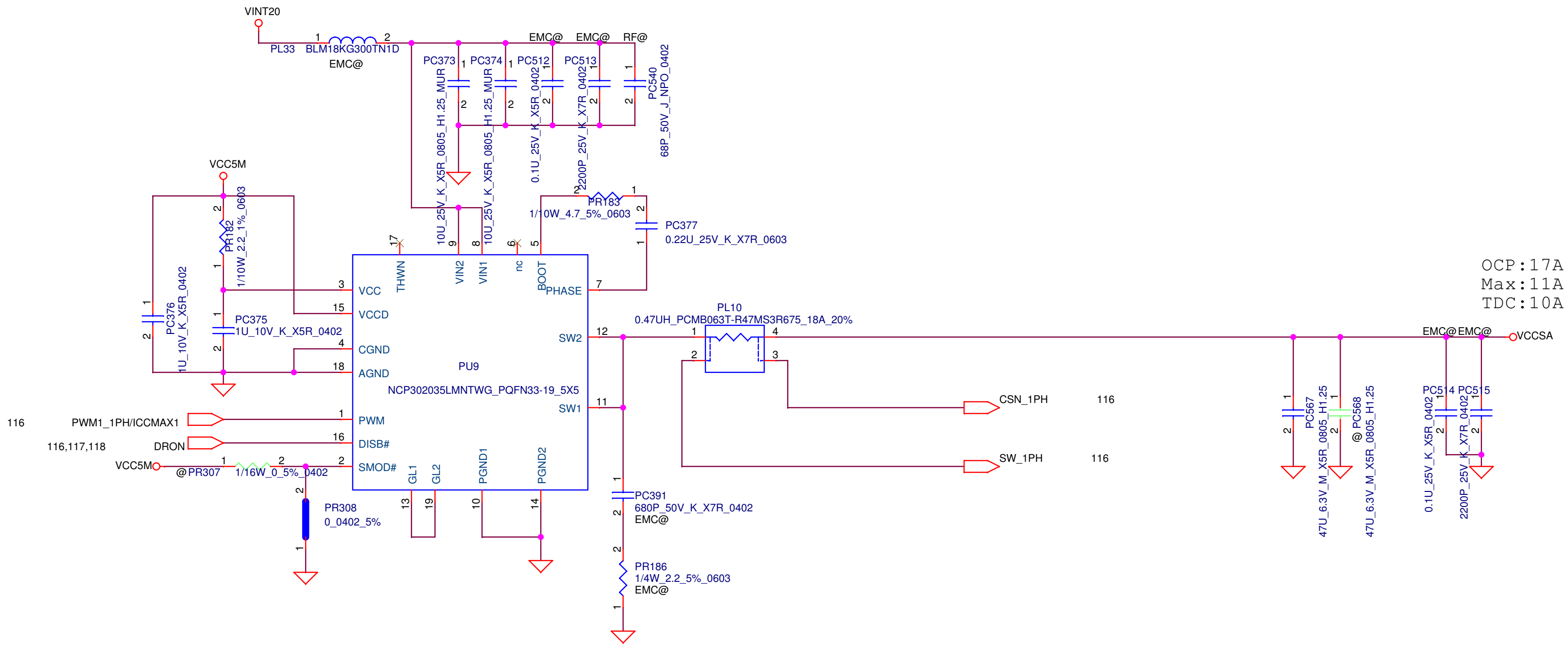
Project Name: Nighthawk-1

Rev: 0.1

Title: DC/DC VCCGFXCORE_I

Date: Monday, April 29, 2019

Sheet 118 of 142



LC Future Center Secret Data

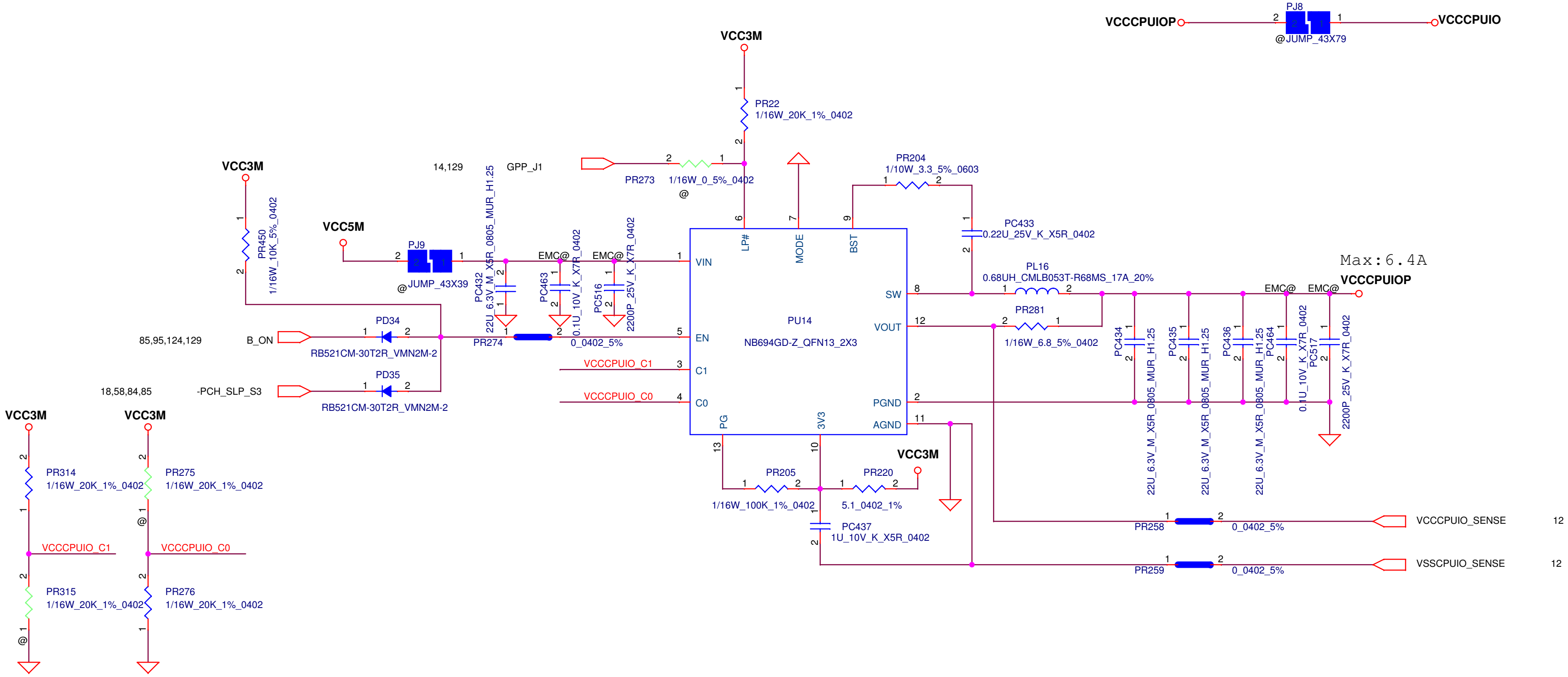
Project Name: Nighthawk-1

Rev: 0.1

Title: DC/DC VCCSA

Date: Monday, April 29, 2019

Sheet 119 of 142



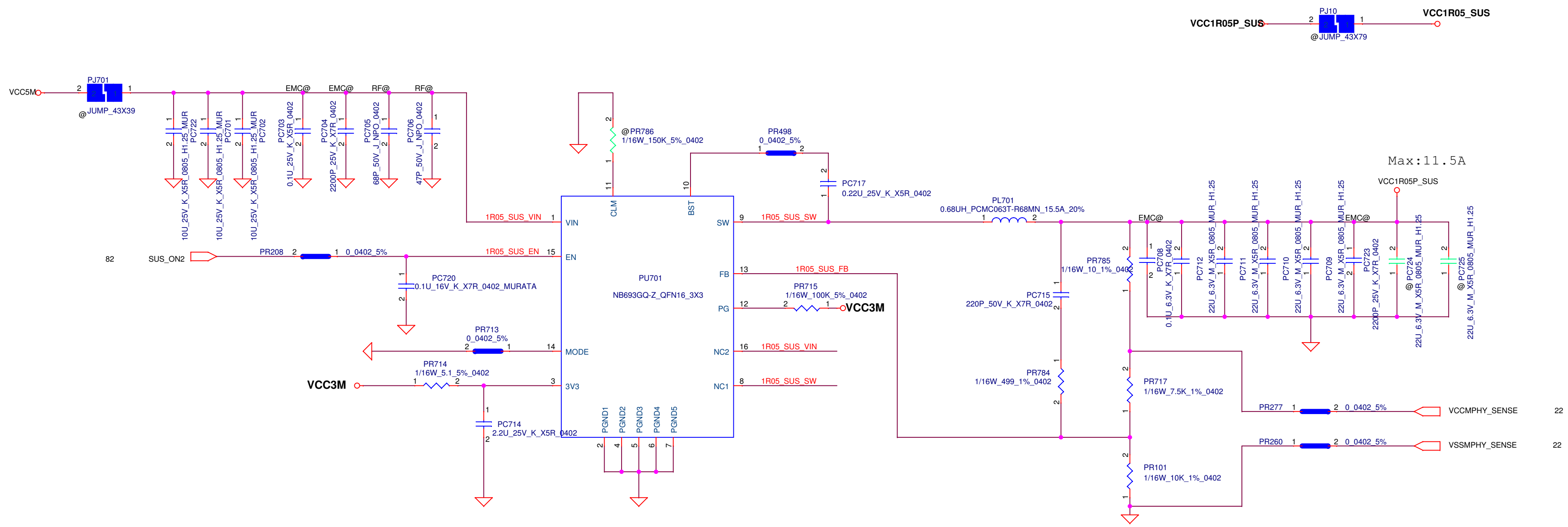
Control Bit Definitions

LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

Project Name: Nighthawk-1

Rev 0.1

Title: DC/DC VCCCPUIO



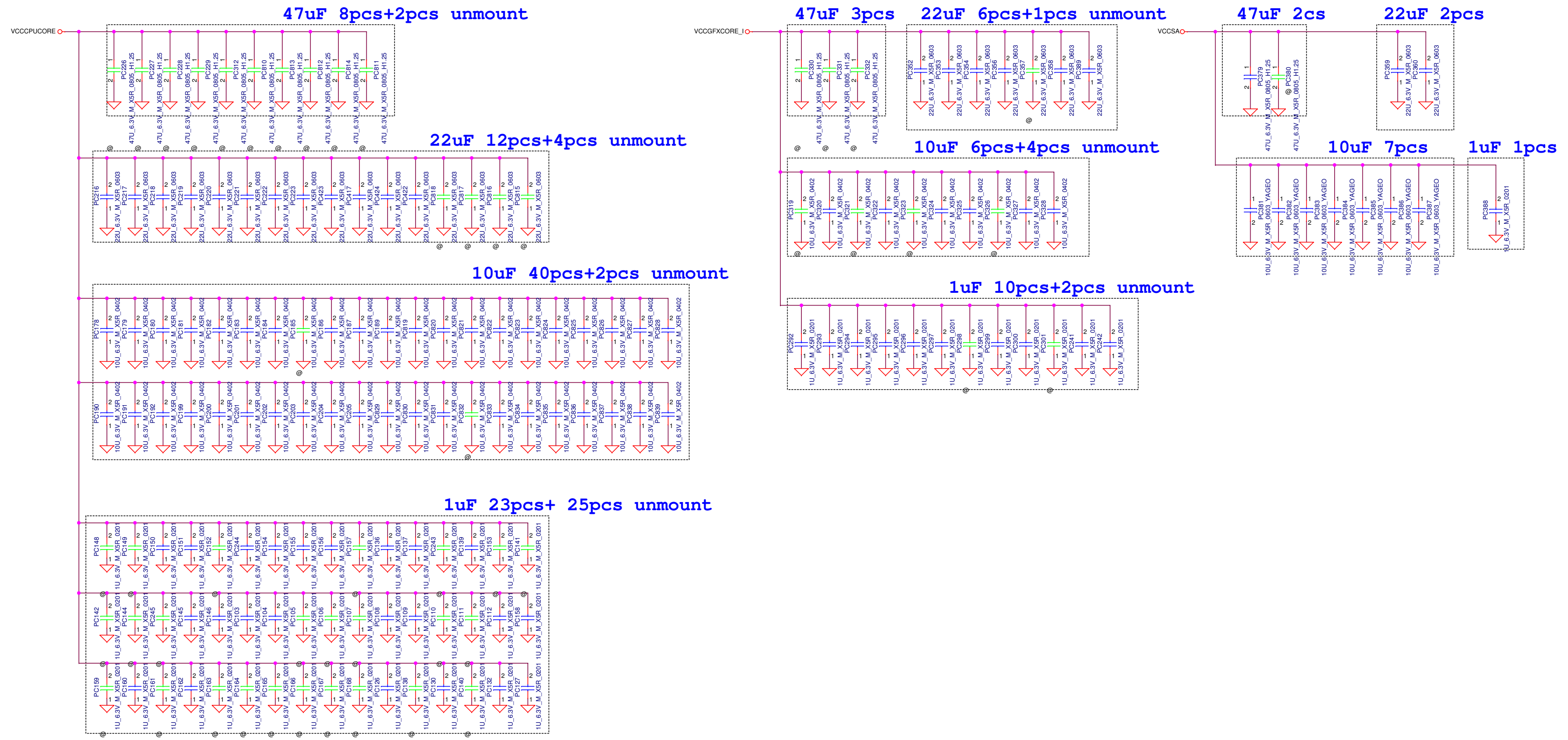
LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev: 0.1

Title: **DC/DC VCC1R05_SUS**

Date: Monday, April 29, 2019



LC Future Center Secret Data

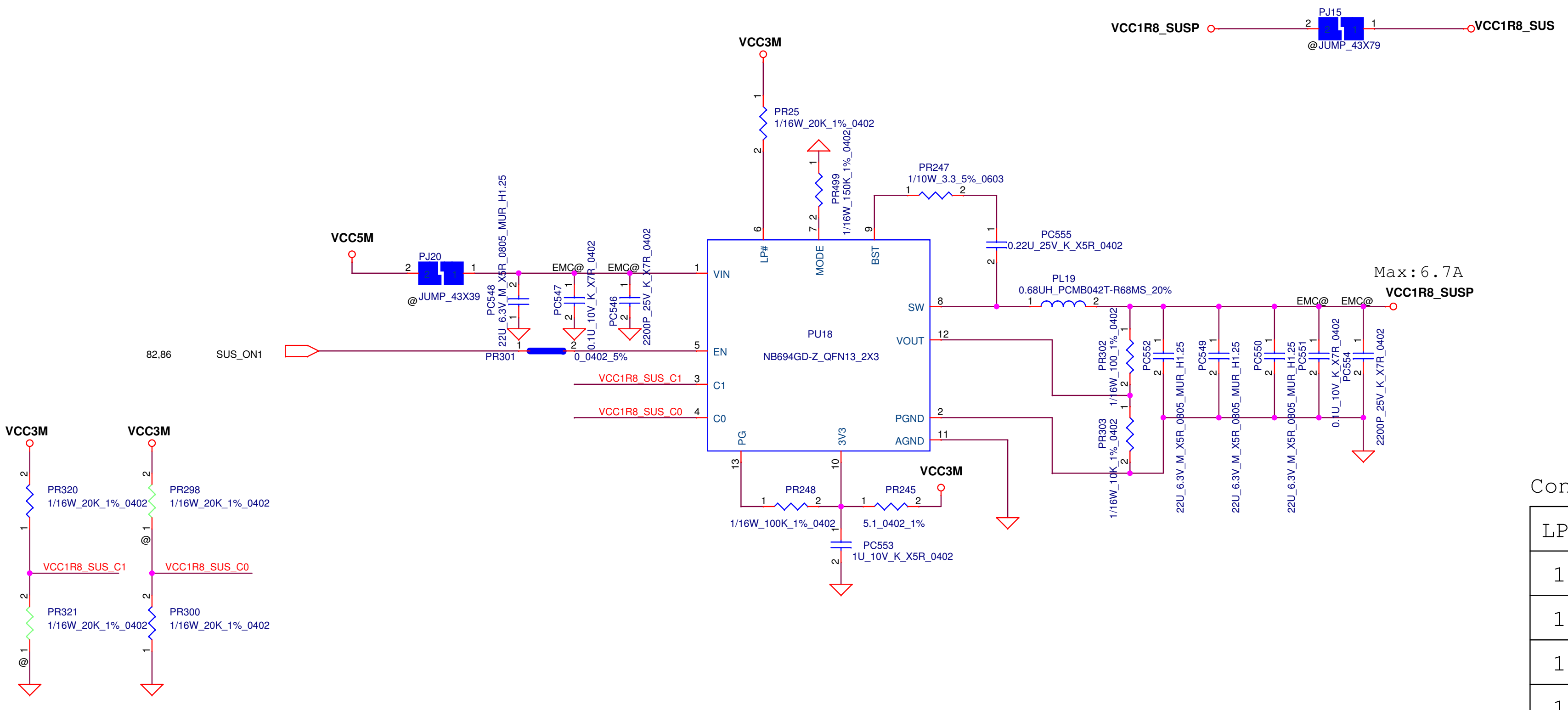
Project Name: Nighthawk-1

Rev: 0.1

Title: VCCCPUCORE DECOUPLING

Date: Monday, April 29, 2019

Sheet 122 of 142



Control Bit Definitions

LP#	C1	C0	VOUT(V)
1	0	0	1.2
1	0	1	1.5
1	1	0	1.8
1	1	1	2.5

LCFC

Project Name: Nighthawk-1

Rev: 0.1

Title: DC/DC VCC1R8_SUS

Date: Monday, April 29, 2019

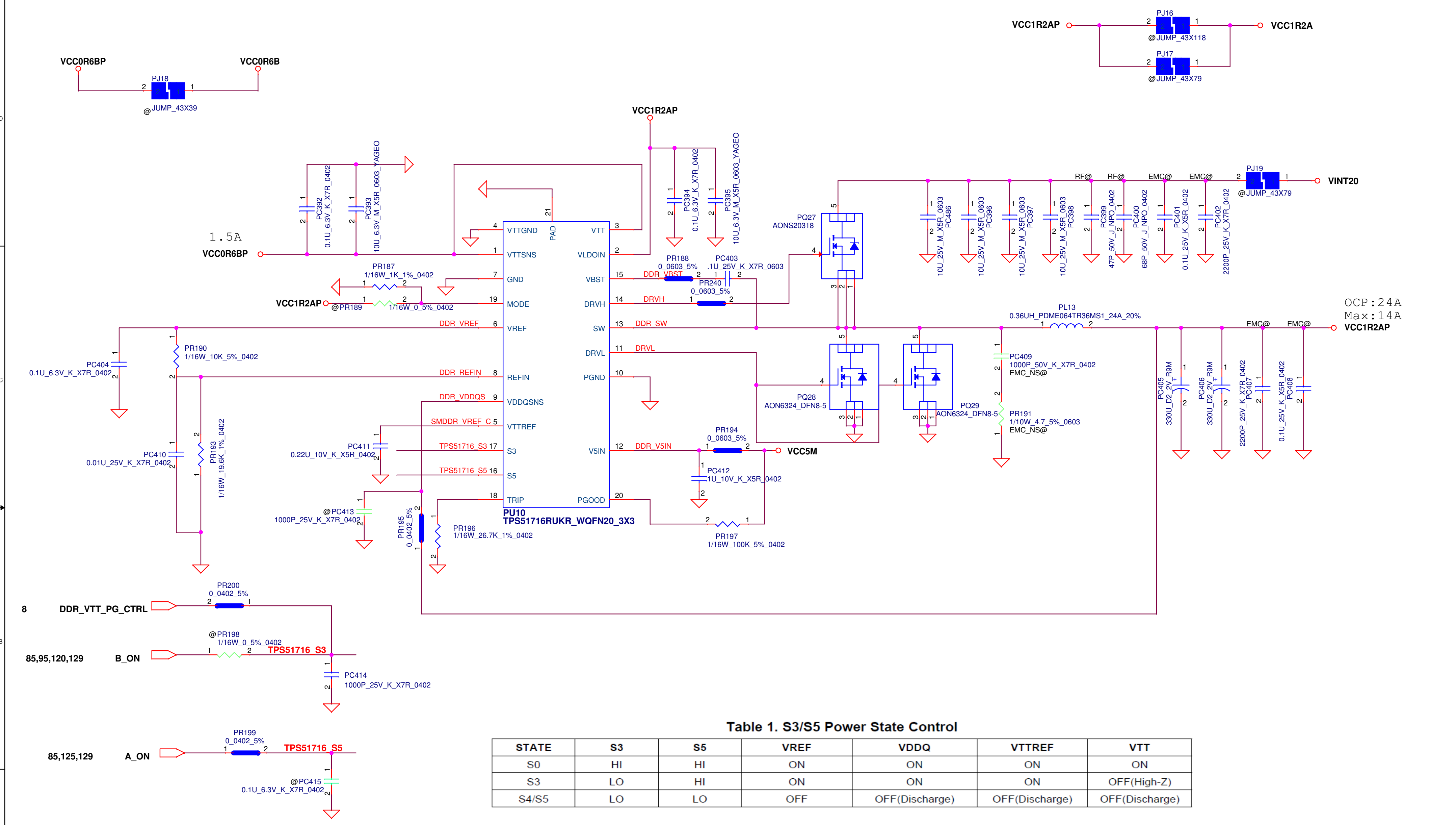
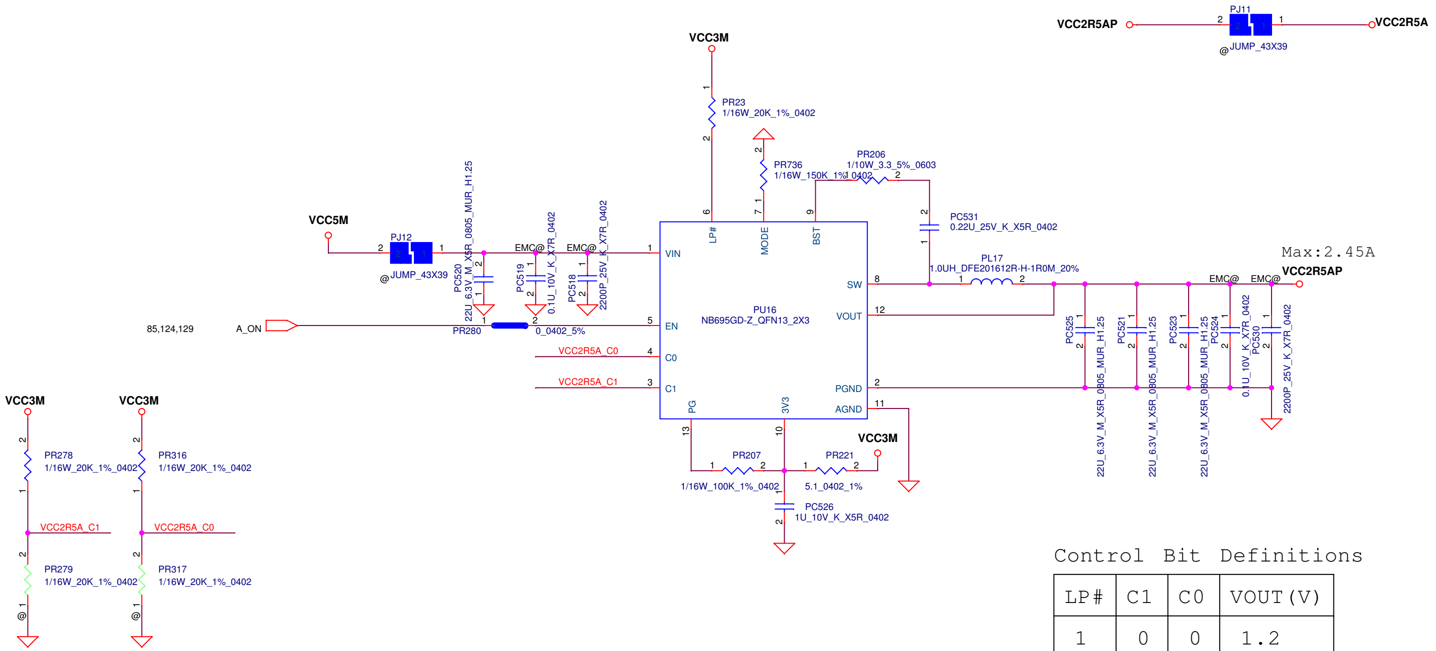


Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)



Control Bit Definitions

LP#	C1	C0	VOUT(V)
1	0	0	1.2
1	0	1	1.5
1	1	0	1.8
1	1	1	2.5

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LC Future Center Secret Data	Project Name	*Nighthawk-1*
LCFC	Rev 0.1	Title **BLANK**
	Date: Monday, April 29, 2019	Sheet 127 of 142

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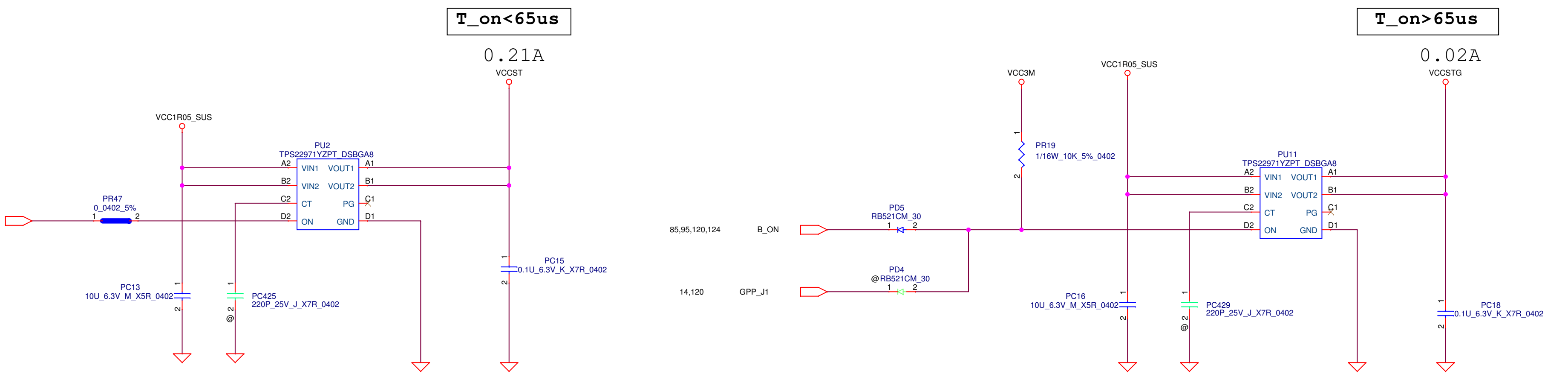
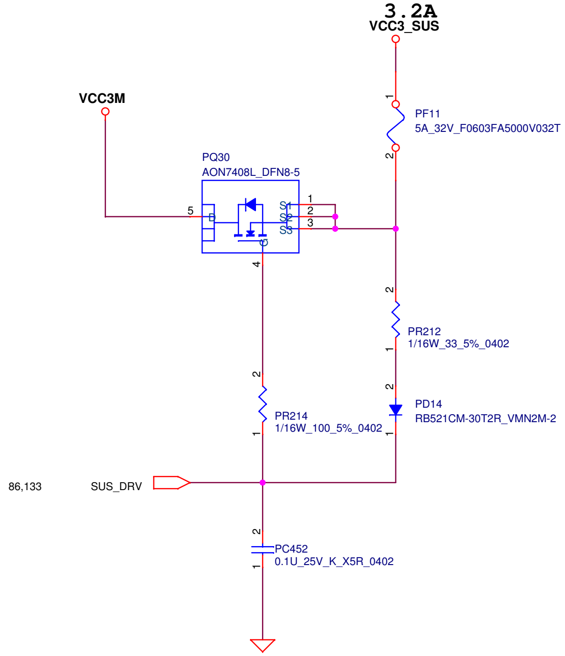
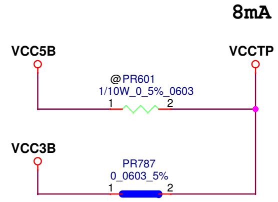


LC Future Center Secret Data	Project Name	Nighthawk-1
	Rev 0.1	Title LOAD SW VCCST/VCCSTG
	Date: Monday, April 29, 2019	Sheet 129 of 142





LC Future Center Secret Data

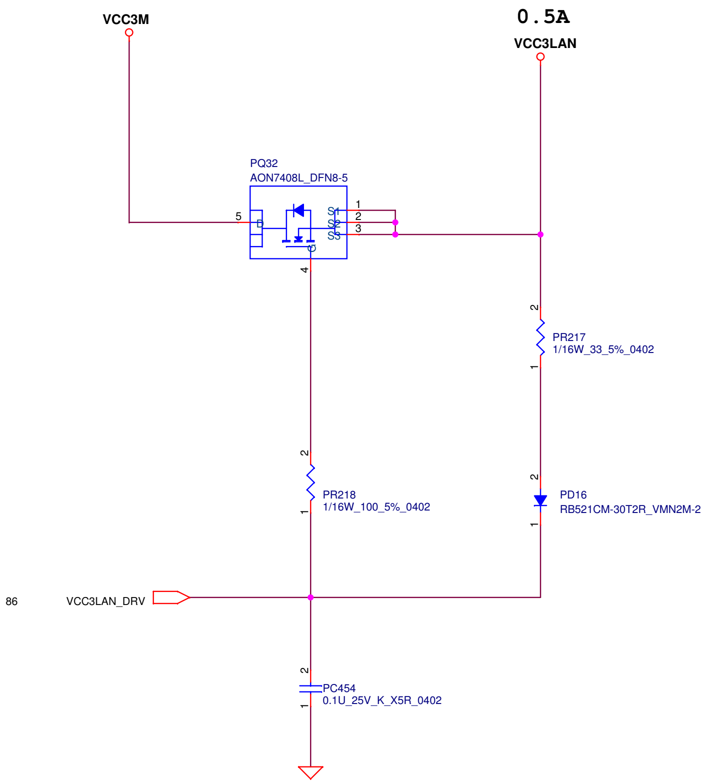
LCFC

Project Name

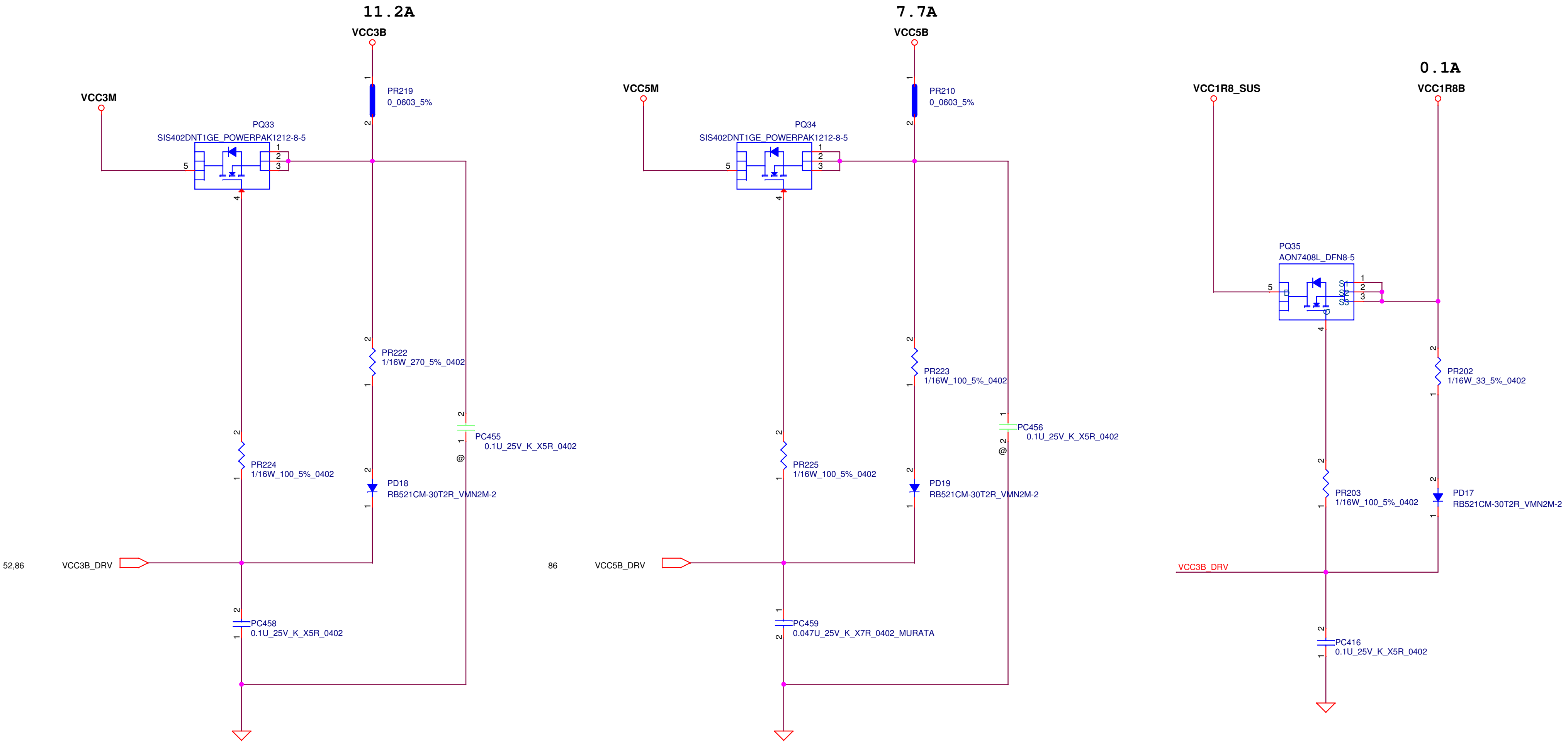
Nighthawk-1

Rev	Title
0.1	*LOAD SW LOAD SW PCH SUS/TP*

Date: Monday, April 29, 2019 | Sheet 130 of 142



LC Future Center Secret Data	Project Name: Nighthawk-1
	Rev: 0.1 — Title: LOAD SW LAN
	Date: Monday, April 29, 2019 — Sheet 131 of 142



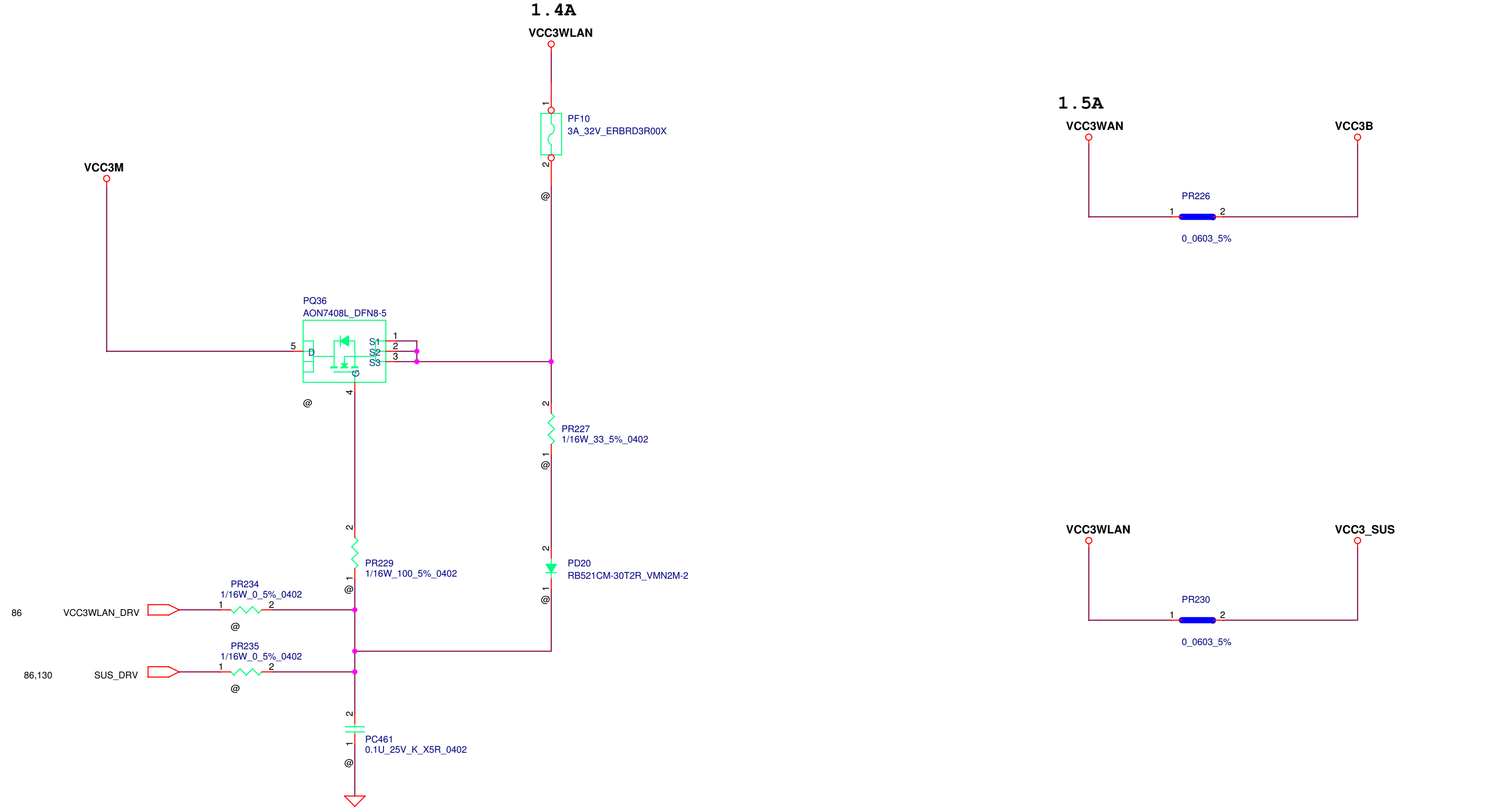
LC Future Center Secret Data

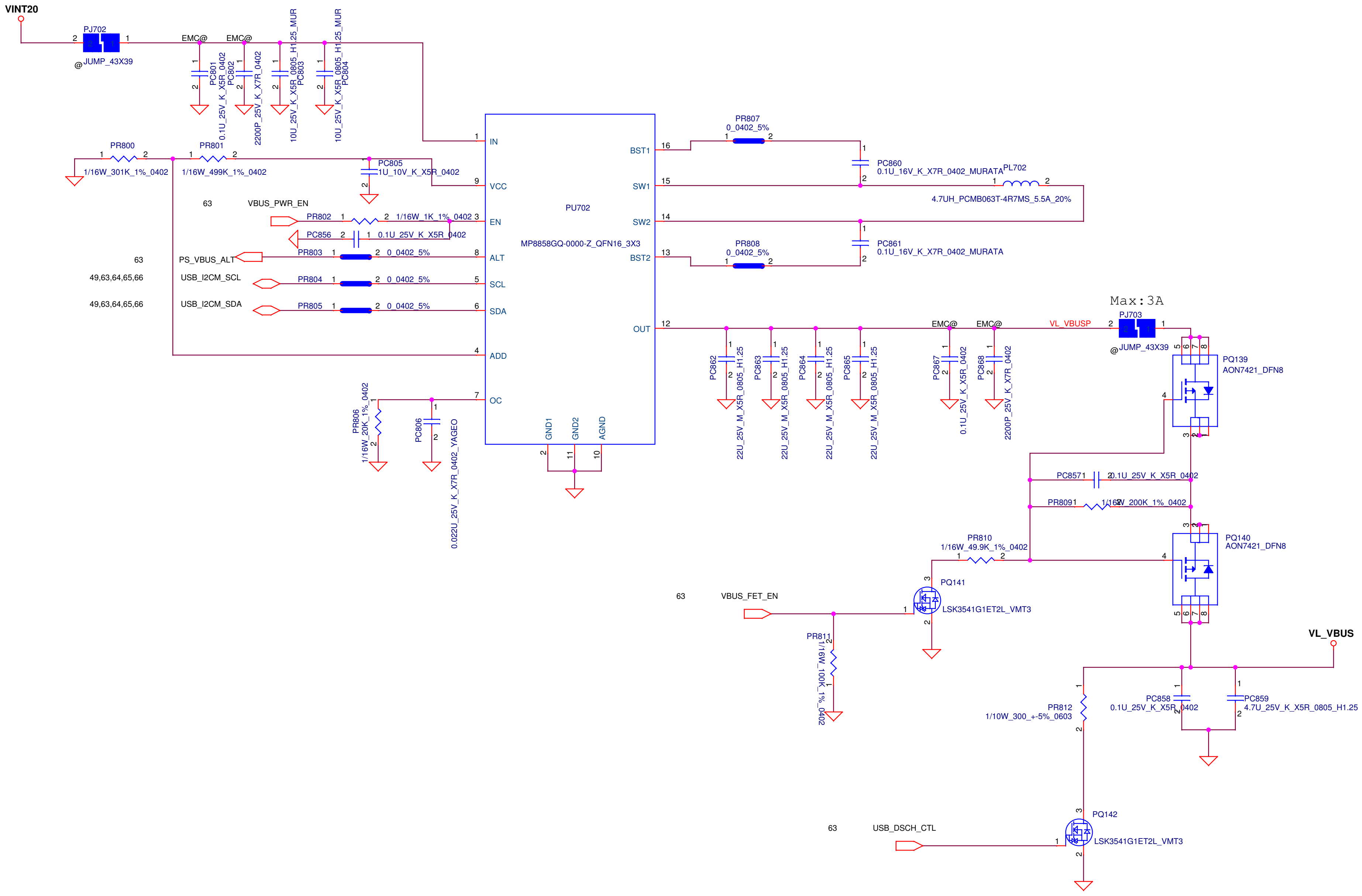
Project Name: Nighthawk-1

Rev: 0.1

Title: LOAD SW B

Date: Monday, April 29, 2019


1.4A
VCC3WLAN
PF10
3A_32V_ERBRD3R00X
VCC3M
PQ36
AON7408L_DFN8-5
D
S1
S2
S3
G
PR227
1/16W_33_5%_0402
PR229
1/16W_100_5%_0402
PD20
RB521CM-30T2R_VMN2M-2
PR234
1/16W_0_5%_0402
86
VCC3WLAN_DRV
PR235
1/16W_0_5%_0402
86,130
SUS_DRV
PC461
0.1U_25V_K_X5R_0402
1.5A
VCC3WAN
VCC3B
PR226
0_0603_5%
VCC3WLAN
VCC3_SUS
PR230
0_0603_5%



LC Future Center Secret Data

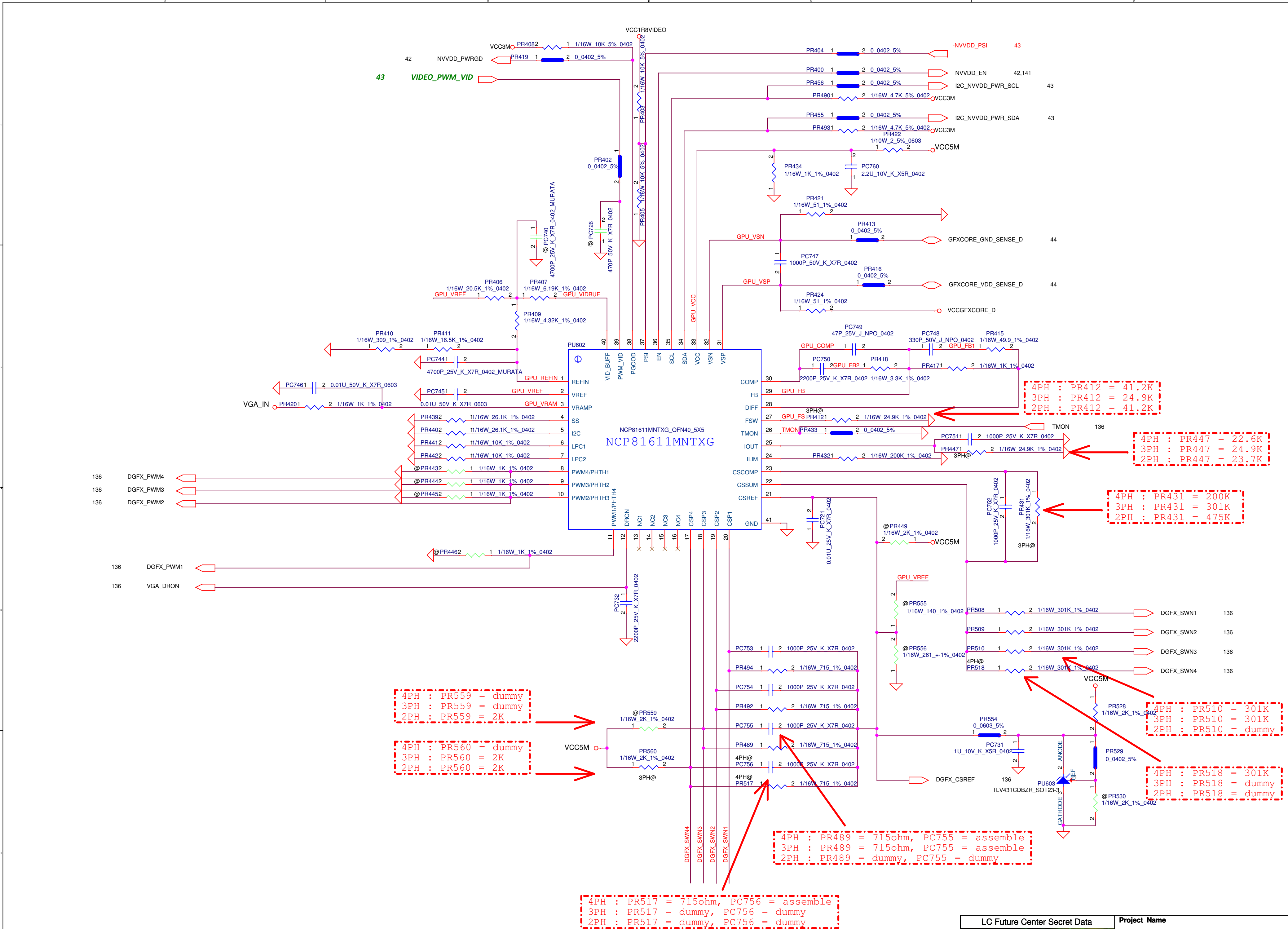
LCFC

Project Name: Nighthawk-1

Rev: 0.1

Title: DC/DC USBC

Date: Monday, April 29, 2019



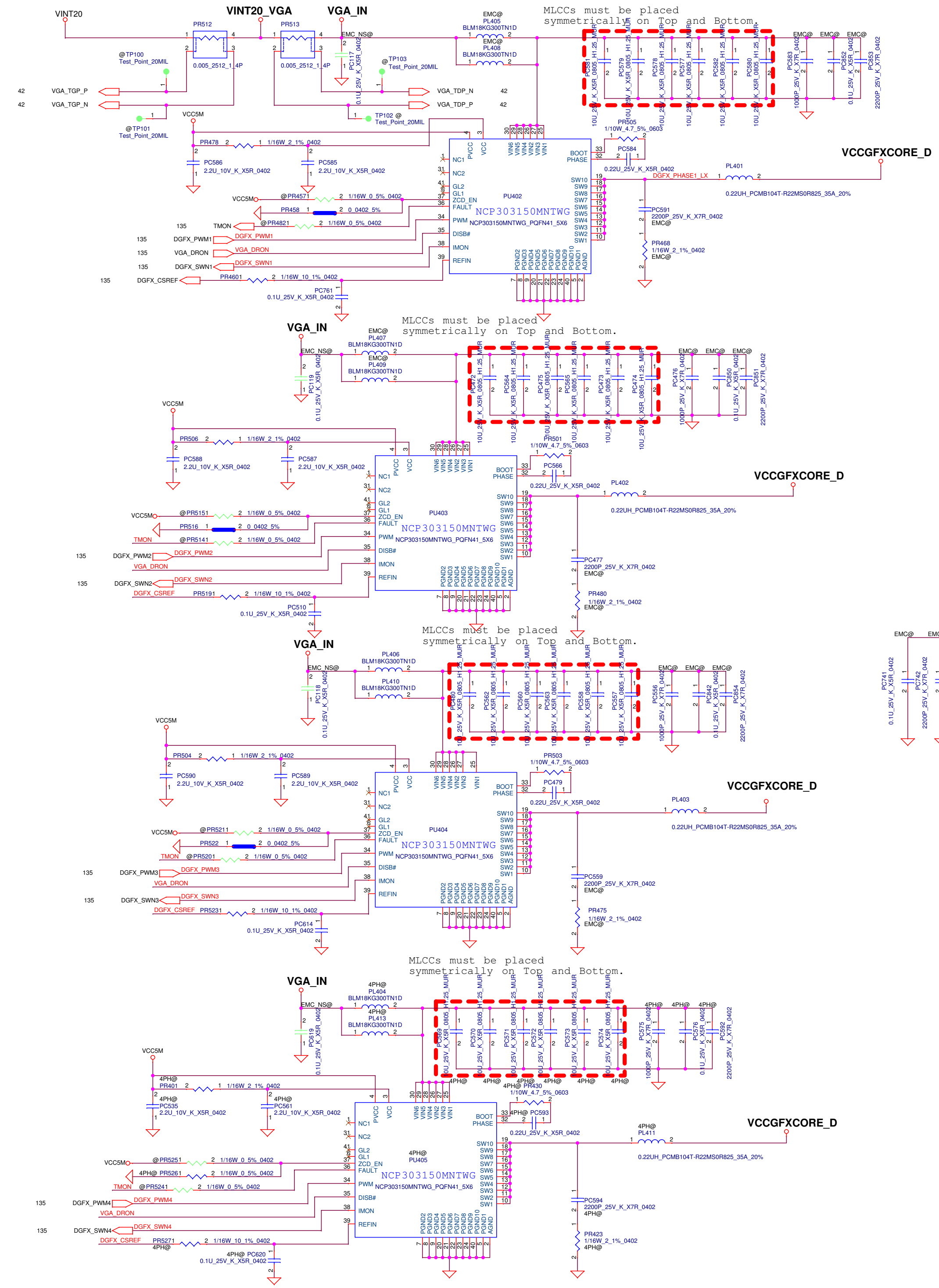
LC Future Center Secret Data

Project Name: Nighthawk-1

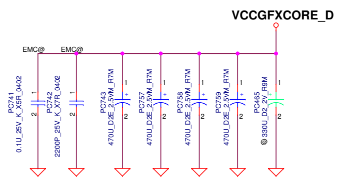
Rev: 0.1

Title: VCCGFXCORE_D IC

Date: Monday, April 29, 2019



	EDP-continue	EDP-Peak	EDPe	OCP
N19E-Q5 (max-Q)	84A	300A	61A	320A
N19E-Q3 (MAX-Q)	84A	300A	60A	320A
N19E-Q1 (MAX-P)	90A	225A	57A	240A
N19P-Q3 (MAX-P)	55A	150A	TBD	160A
N19P-Q1 (MAX-P)	45A	150A	TBD	160A



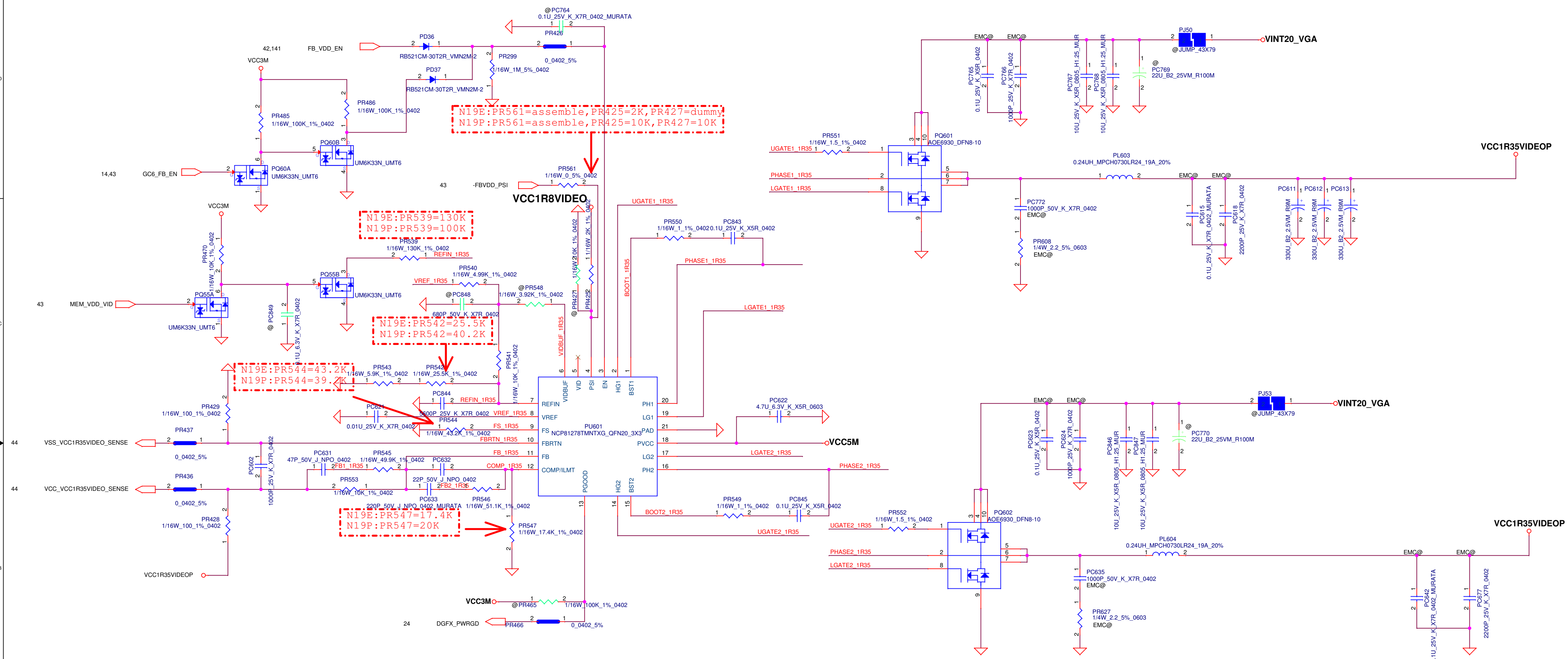
LC Future Center Secret Data

Project Name: Nighthawk-1

Rev: 0.1

Title: VCCGFXCORE_D

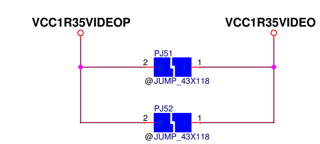
Date: Monday, April 29, 2019

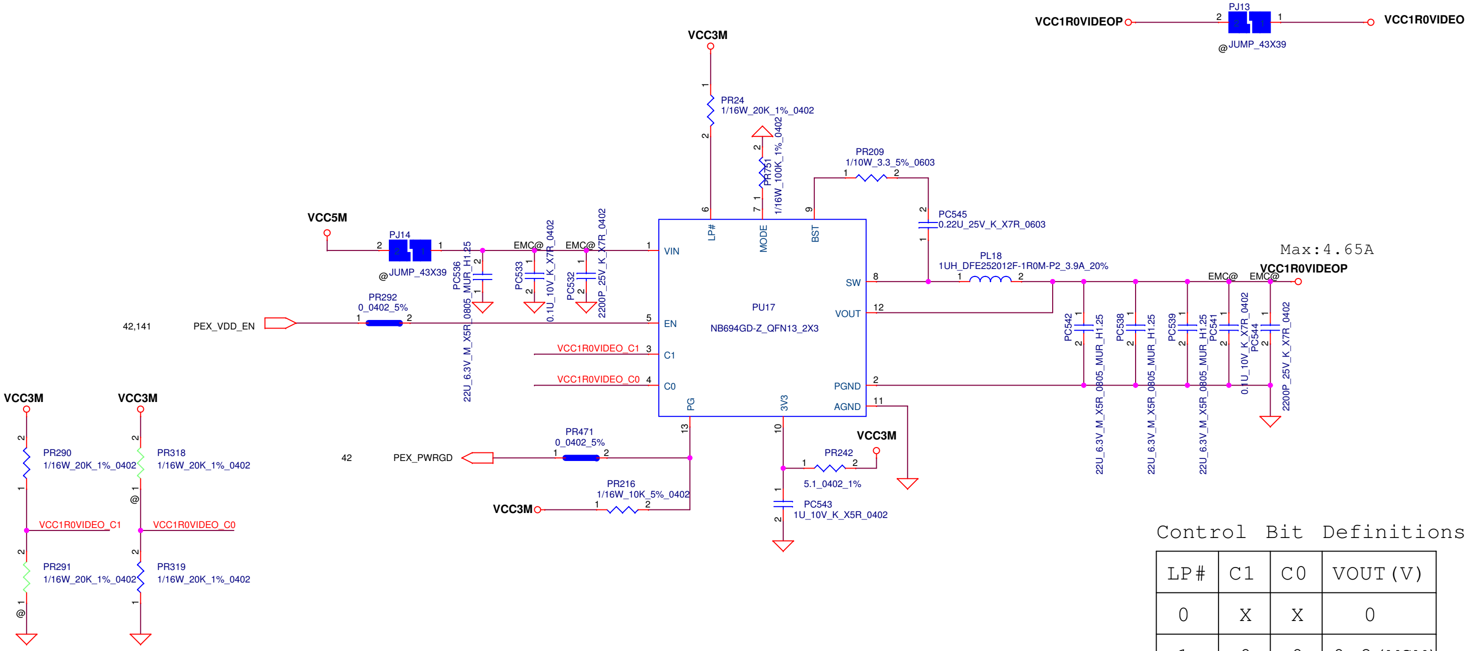


N19E (1.25V/1.35V)				
MEM_VDD_VID	Vref(V)	PR539	PR542	VCC1R35VIDEO
L	2	130K	25.5K	1.25V
H	2	130K	25.5K	1.35V

N19P (1.35V/1.5V)				
MEM_VDD_VID	Vref(V)	PR539	PR542	VCC1R35VIDEO
L	2	100K	40.2K	1.35V
H	2	100K	40.2K	1.5V

	EDP-continue	EDP-Peak	OCP
N19E-Q5/Q3 (max-Q)	40A	54A	70A
N19E-Q1	35A	46A	70A
N19P-Q3/Q1	14A	20A	30A





Control Bit Definitions

LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.8(MSM)
1	0	1	0.95
1	1	0	1
1	1	1	1.05

LCFC

Project Name: *Nighthawk-1*

Rev 0.1

Title: DC/DC VCC1R0VIDEO

Date: Monday, April 29, 2019

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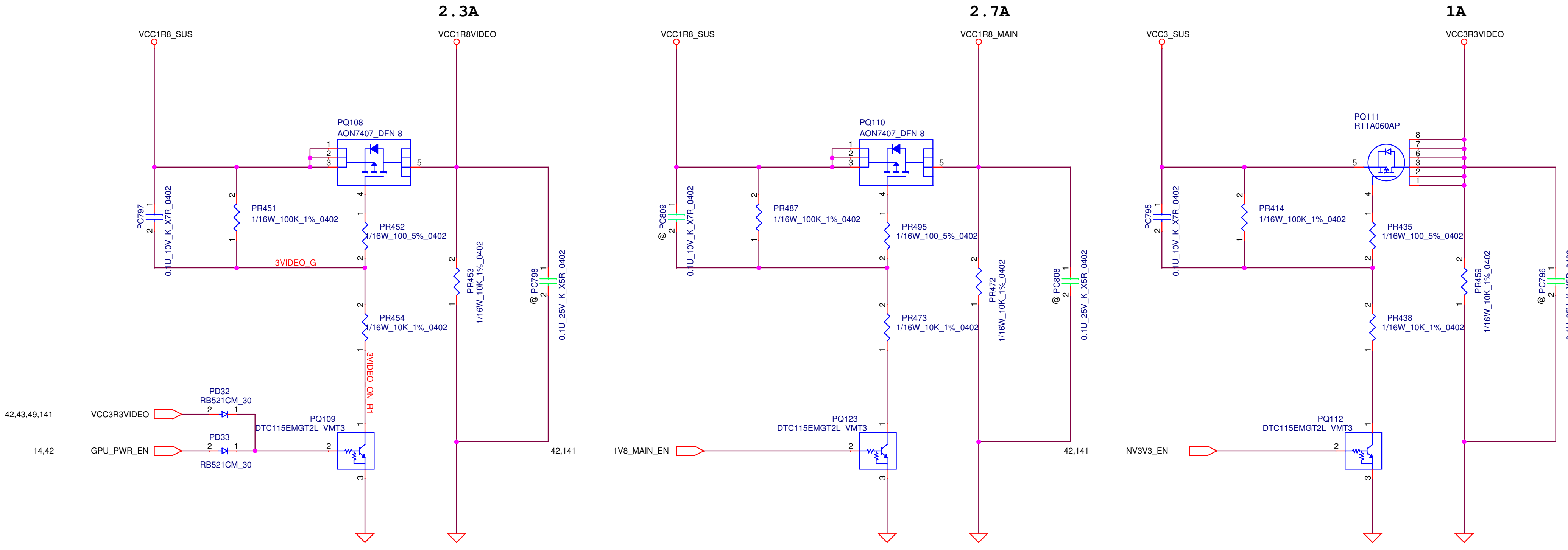


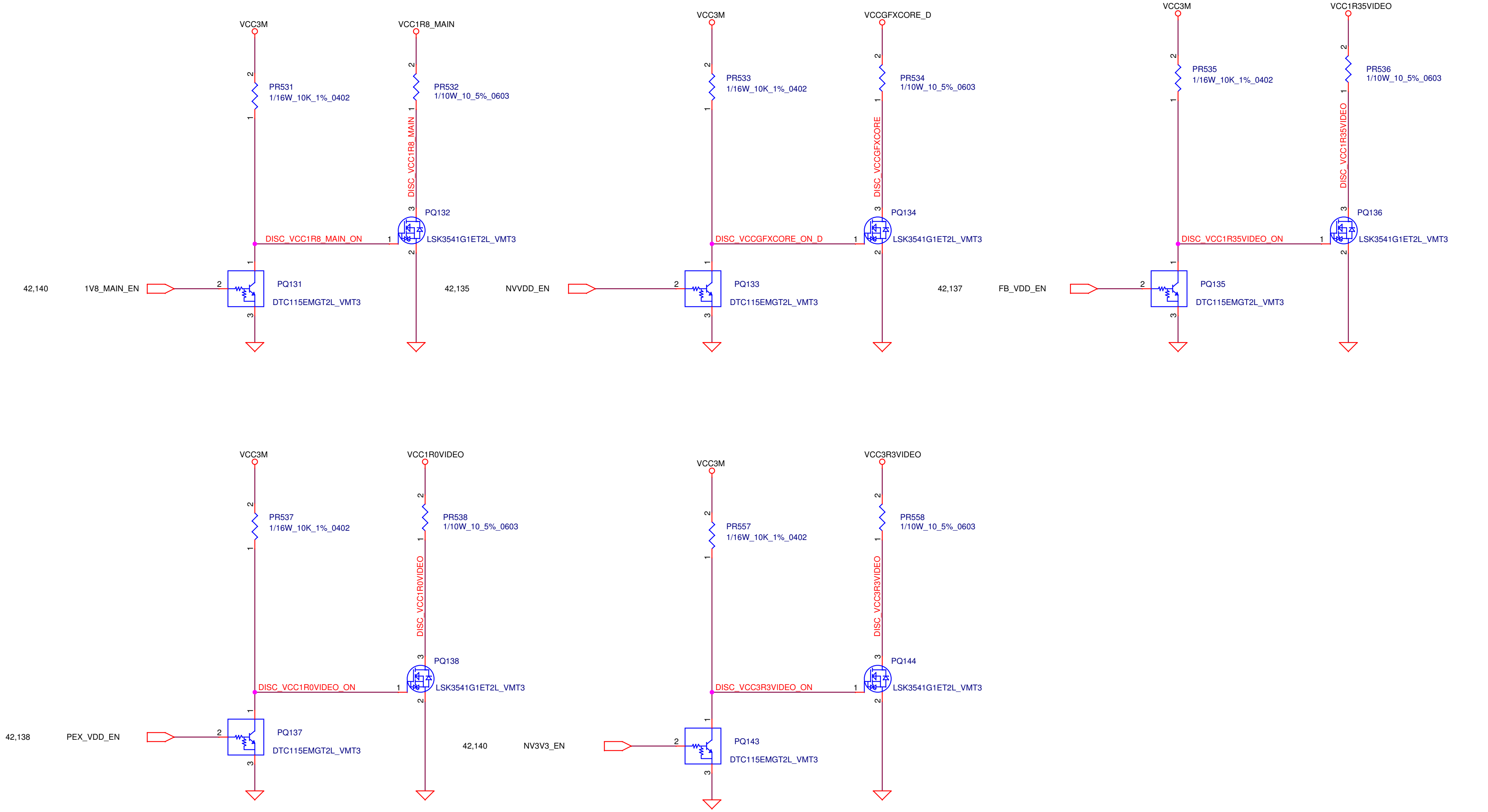
LC Future Center Secret Data

Project Name: *Nighthawk-1*

Rev: 0.1

Title: **LOAD SW VIDEO**

Date: Monday, April 29, 2019



LC Future Center Secret Data

Project Name

Nighthawk-1

Rev 0.1

Title

DISCHARGE CIRCUIT VIDEO

Date: Monday, April 29, 2019

PR431
4PH@
1/16W_200K_1%_0402

PR447
4PH@
1/16W_22.6K_1%_0402

PR412
4PH@
1/16W_41.2K_1%_0402

PR115
82@
1/16W_25.5K_1%_0402

PR122
82@
1/16W_30.1K_1%_0402

PR144
82@
1/16W_110K_1%_0402

3PH@ comment

4PH@ comment

82@ comment