GAMING

Gaming (Skylake-H) Revision_1.00_2015/03/10

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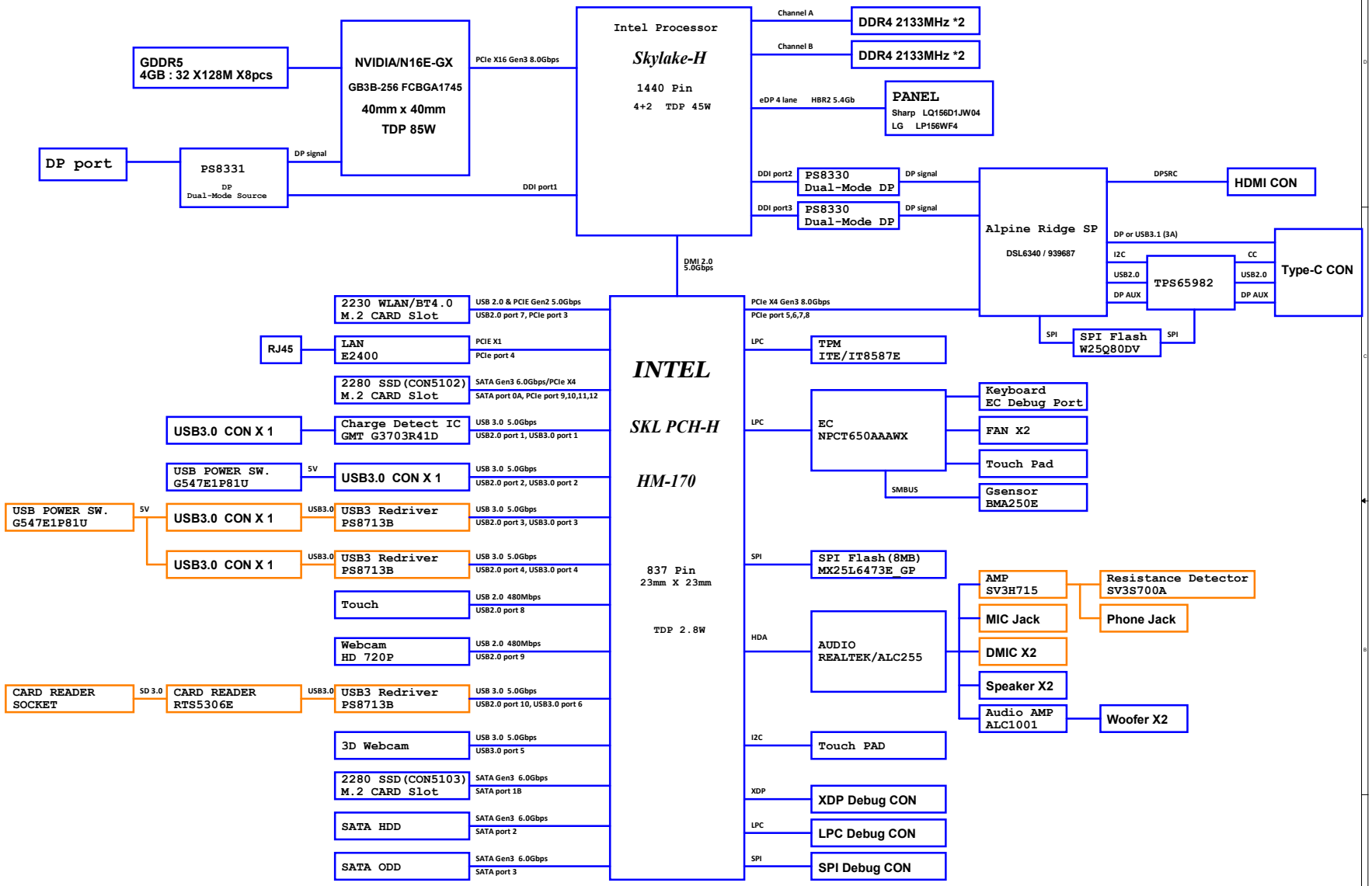
SO-DIMM (Max Memory 64GB)



Note:
Default component footprint is
SMD 0402, Y5V, 5% type.
Difference footprint show on schematics.

Property: BOM
I = Installed Part.
NI = Not Installed Part.
PROTO = PROTO Phase Only.
VP = Virtual Part.
NOBOM = Symbol only.

VP = Virtual Part.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BLOCK DIAGRAM
Pegatron Corp. Engineer: Leon_Lu
Size: Custom | Project Name: P5NCN/P7NCN MAIN BOARD | Rev: A01
Date: Monday, September 07, 2015 | Sheet 1 of A01

I2C_Port	Module	DEVICE	7-bit addr
I2C_0	TOUCH PAD		0X2C
I2C_1	TOUCH PANEL		
SMBUS	DDR Channel A(CON1600)		
	DDR Channel A(CON1601)		
	DDR Channel B(CON1700)		
	DDR Channel B(CON1701)		
	Resistance Detector	SV3S700A	0X73
SMBUS0 (EC)	BATTERY		0X0B
	CHARGE IC	BQ24735RGRR	0X09
SMBUS1 (EC)	G-SENSOR	BMA250E	0X1D
	THERMAL-SENSOR	G781P8F	0X4C
	LED DRIVER	TLC59116IPWR	0X68
	GPU	N16E-GX	0X4B

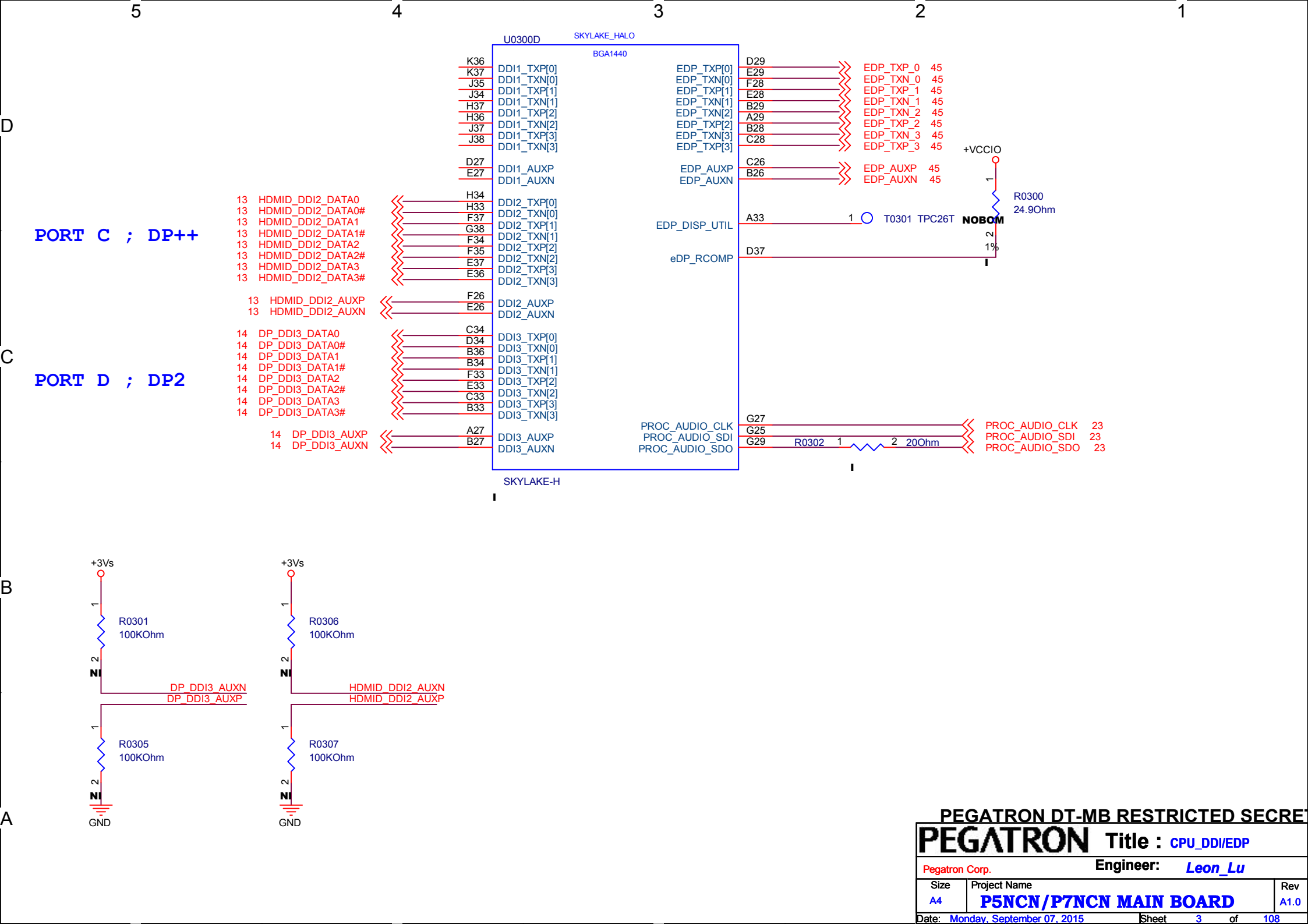
<Variant Name>

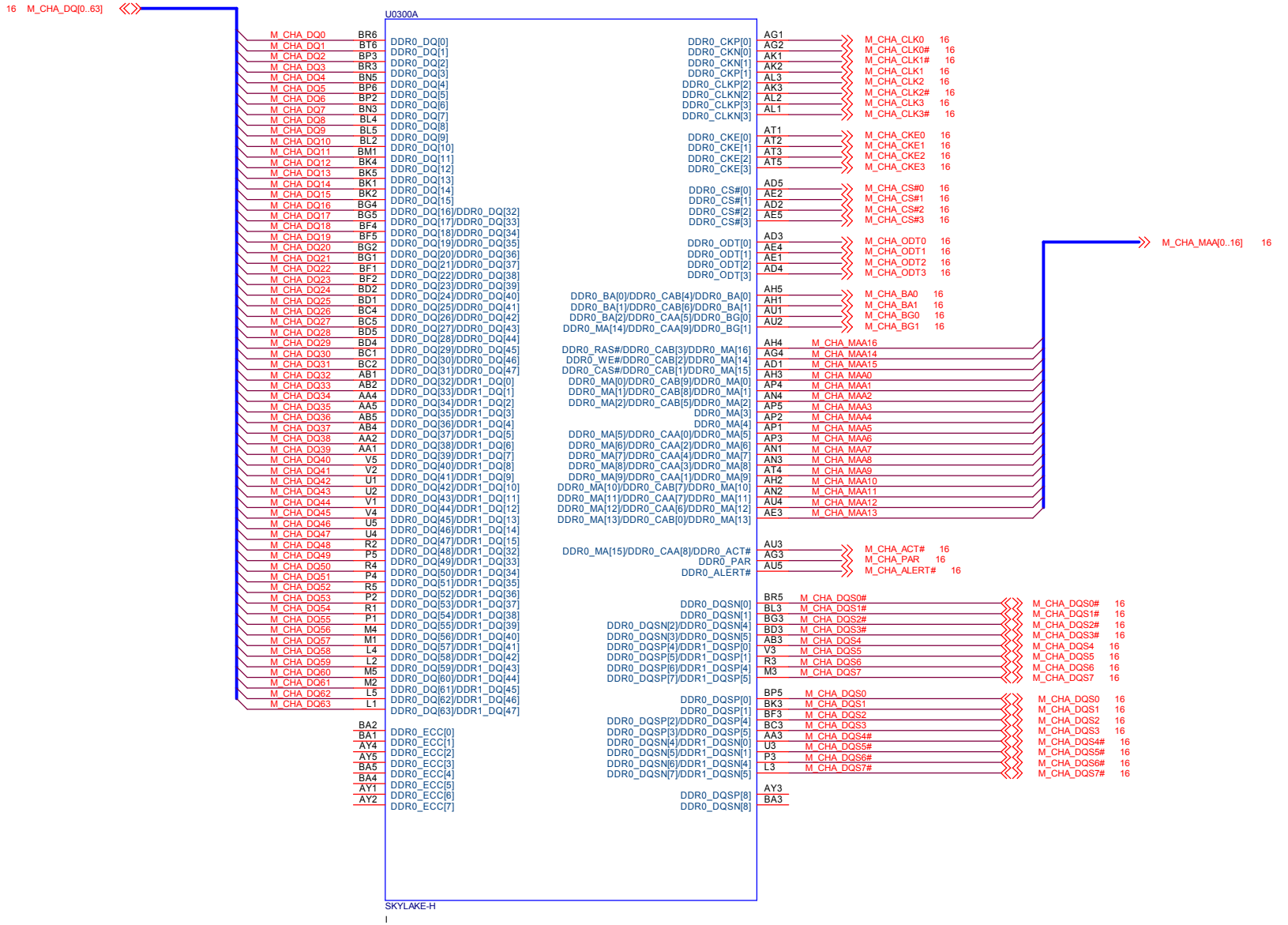
PEGATRON Title : I2C MAP

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A00

Date: Monday, September 07, 2015 Sheet 2 of A02


5
4
3
2
1
D
C
B
A
U0300D
SKYLAKE_HALO
BGA1440
SKYLAKE-H
PORT C ; DP++
PORT D ; DP2
DDI1_TXP[0]
DDI1_TXN[0]
DDI1_TXP[1]
DDI1_TXN[1]
DDI1_TXP[2]
DDI1_TXN[2]
DDI1_TXP[3]
DDI1_TXN[3]
DDI1_AUXP
DDI1_AUXN
DDI2_TXP[0]
DDI2_TXN[0]
DDI2_TXP[1]
DDI2_TXN[1]
DDI2_TXP[2]
DDI2_TXN[2]
DDI2_TXP[3]
DDI2_TXN[3]
DDI2_AUXP
DDI2_AUXN
DDI3_TXP[0]
DDI3_TXN[0]
DDI3_TXP[1]
DDI3_TXN[1]
DDI3_TXP[2]
DDI3_TXN[2]
DDI3_TXP[3]
DDI3_TXN[3]
DDI3_AUXP
DDI3_AUXN
13 HDMID_DDI2_DATA0
13 HDMID_DDI2_DATA0#
13 HDMID_DDI2_DATA1
13 HDMID_DDI2_DATA1#
13 HDMID_DDI2_DATA2
13 HDMID_DDI2_DATA2#
13 HDMID_DDI2_DATA3
13 HDMID_DDI2_DATA3#
13 HDMID_DDI2_AUXP
13 HDMID_DDI2_AUXN
14 DP_DDI3_DATA0
14 DP_DDI3_DATA0#
14 DP_DDI3_DATA1
14 DP_DDI3_DATA1#
14 DP_DDI3_DATA2
14 DP_DDI3_DATA2#
14 DP_DDI3_DATA3
14 DP_DDI3_DATA3#
14 DP_DDI3_AUXP
14 DP_DDI3_AUXN
EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXN[2]
EDP_TXP[2]
EDP_TXN[3]
EDP_TXP[3]
EDP_AUXP
EDP_AUXN
EDP_DISP_UTIL
eDP_RCOMP
EDP_TXP_0 45
EDP_TXN_0 45
EDP_TXP_1 45
EDP_TXN_1 45
EDP_TXN_2 45
EDP_TXP_2 45
EDP_TXN_3 45
EDP_TXP_3 45
EDP_AUXP 45
EDP_AUXN 45
+VCCIO
R0300
24.9Ohm
1%
NOBOM
T0301 TPC26T
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
R0302 20Ohm
PROC_AUDIO_CLK 23
PROC_AUDIO_SDI 23
PROC_AUDIO_SDO 23
+3Vs
R0301
100KOhm
R0305
100KOhm
R0306
100KOhm
R0307
100KOhm
DP_DDI3_AUXN
DP_DDI3_AUXP
HDMID_DDI2_AUXN
HDMID_DDI2_AUXP
GND
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : CPU_DDI/EDP
Pegatron Corp.
Engineer: Leon_Lu
Size A4
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 3 of 108



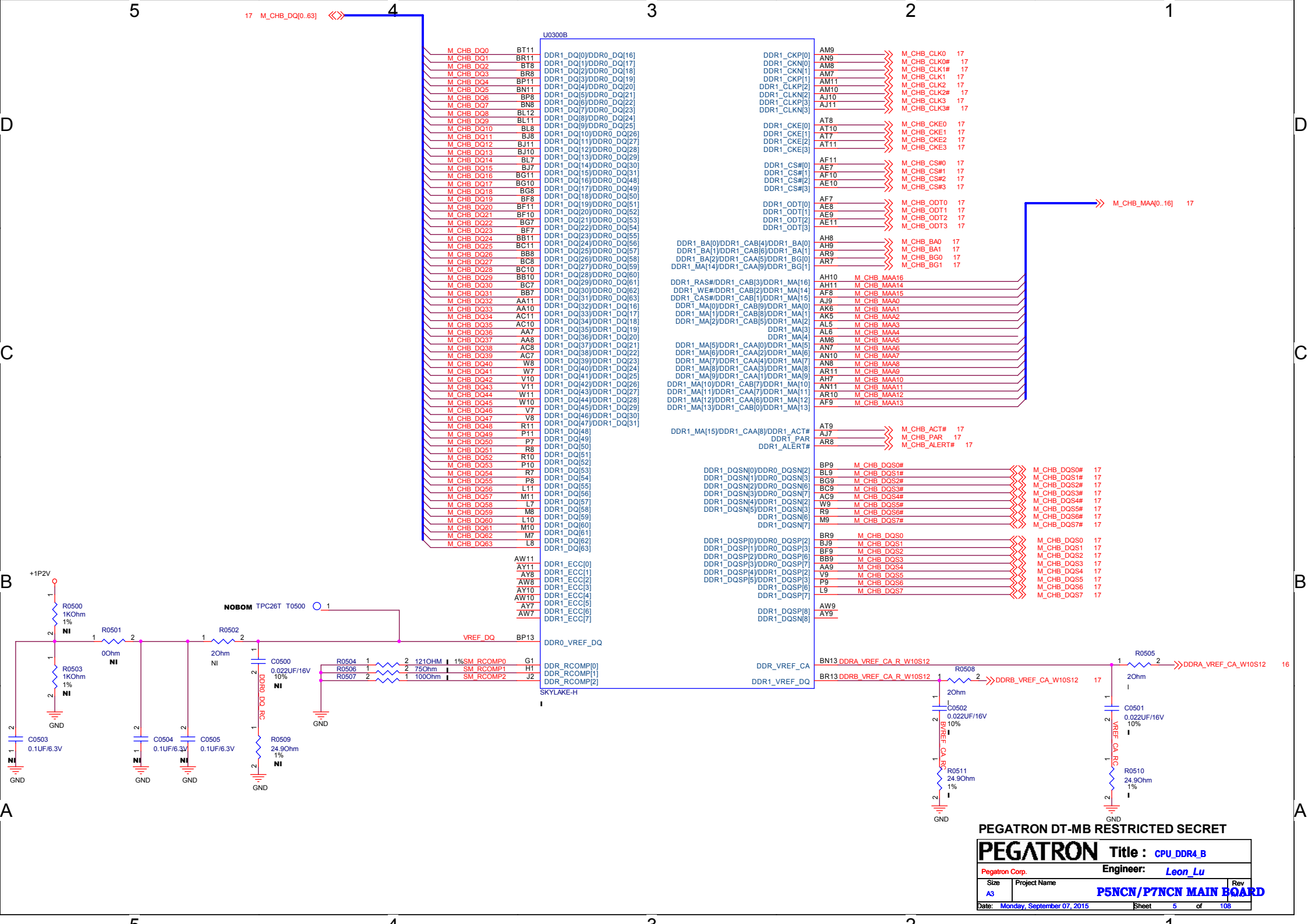
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_DDR4_A

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 4 of 108



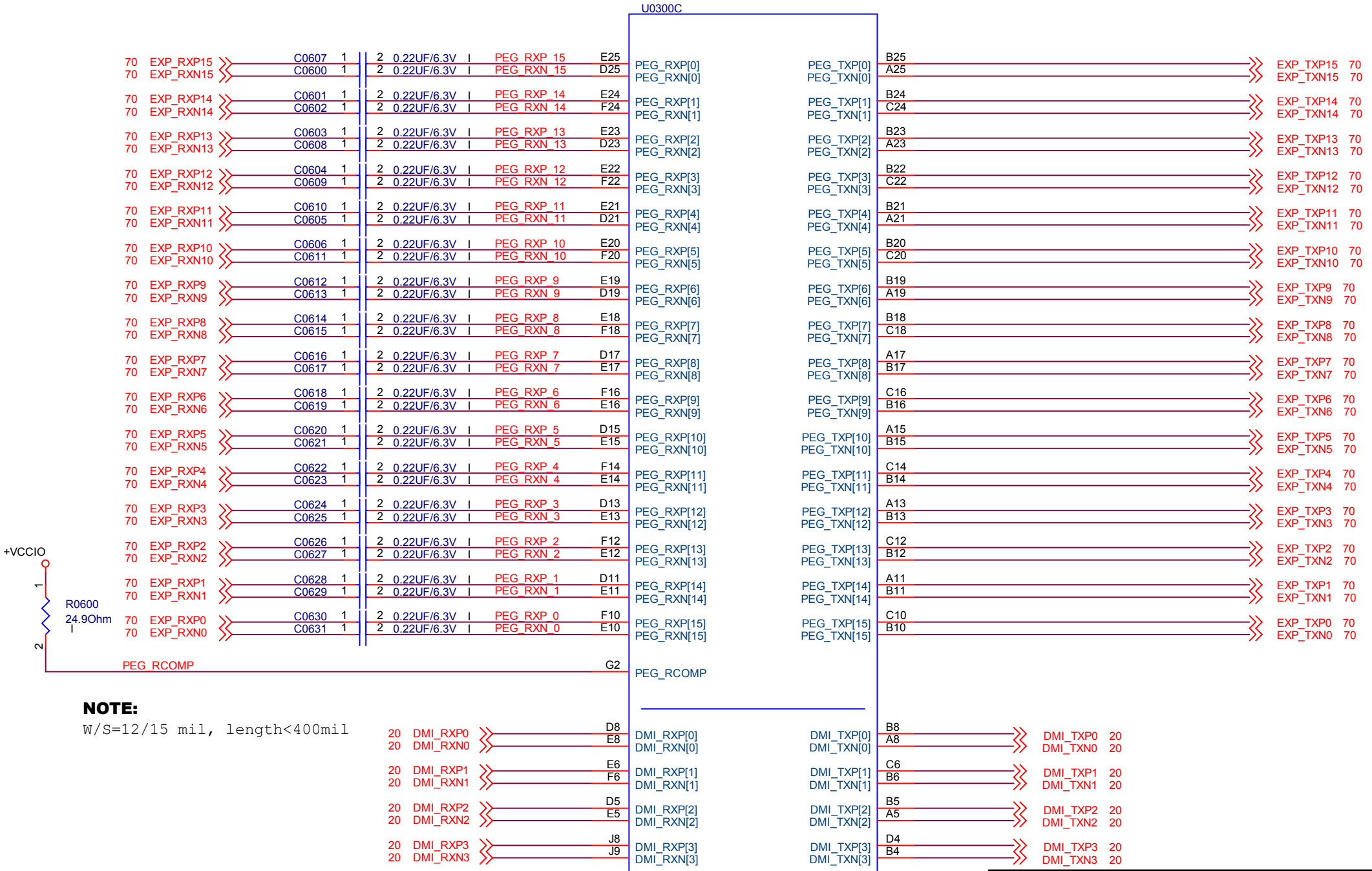
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_DDR4_B

Pegatron Corp. Engineer: Leon_Lu

Size A3 | Project Name P5NCN/P7NCN MAIN BOARD | Rev

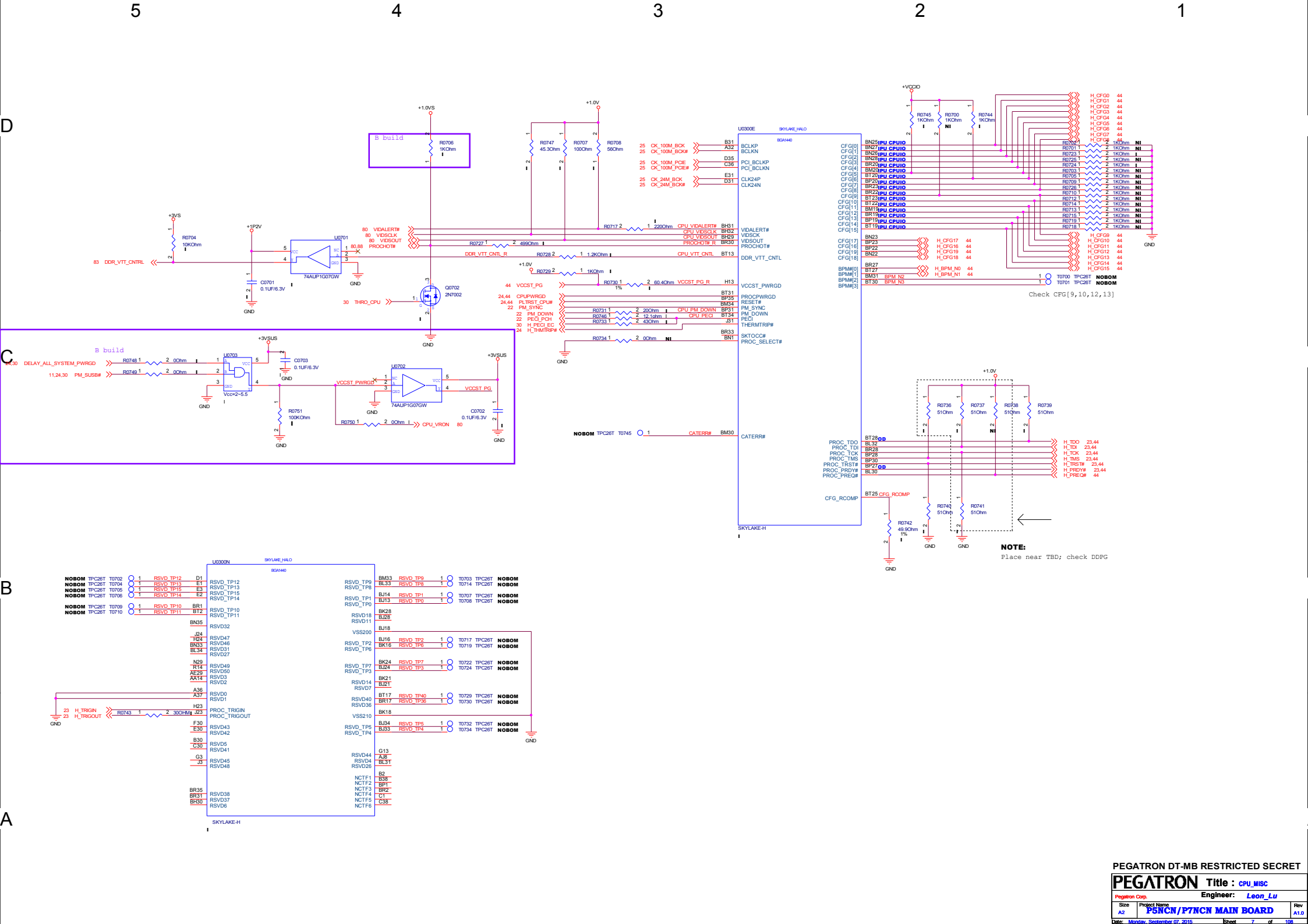
Date: Monday, September 07, 2015 Sheet 5 of 108



NOTE:

W/S=12/15 mil, length<400mil

PEGATRON	Title : CPU_DMI	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 6 of 108	



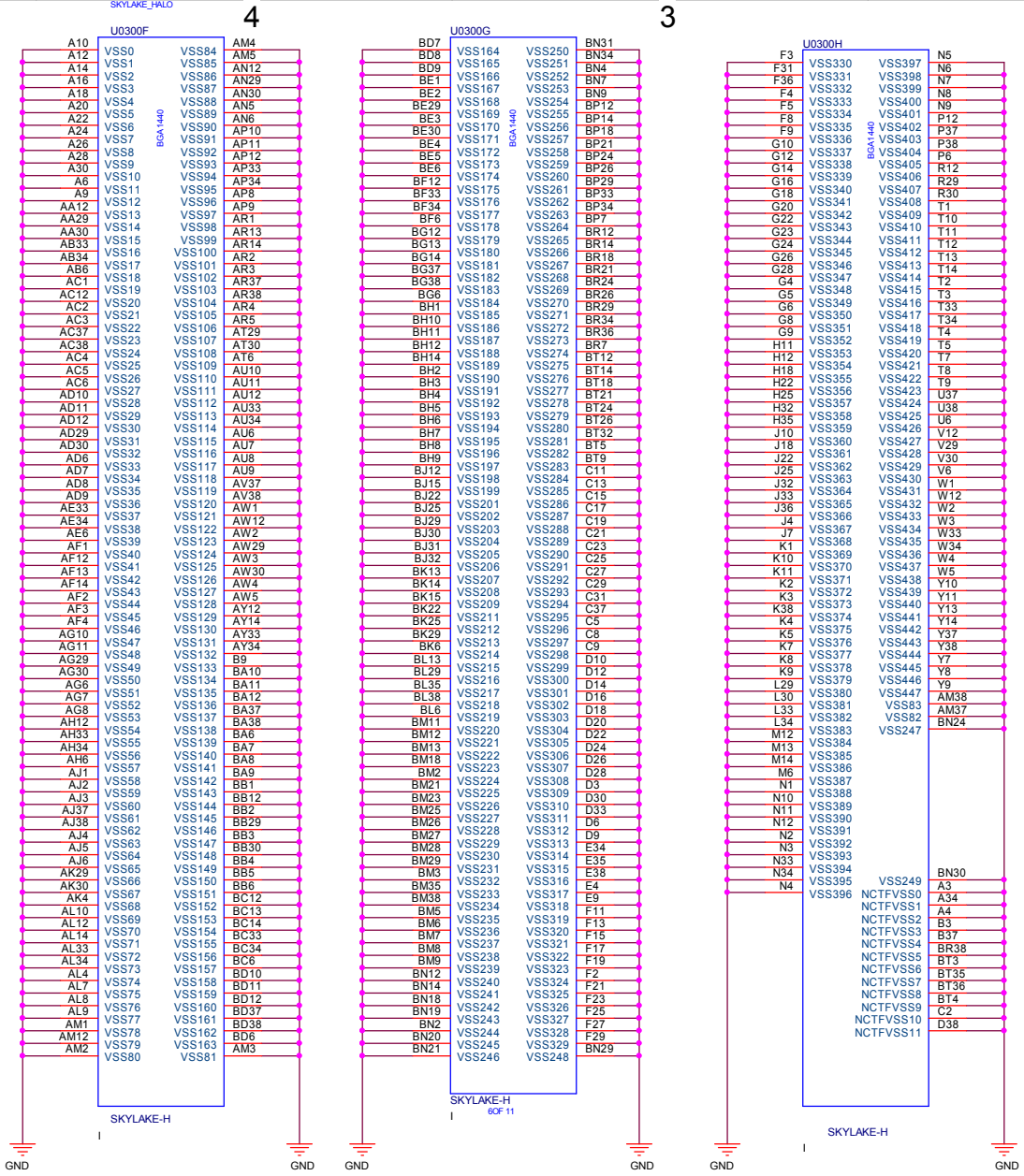
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_MISC

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 7 of 108



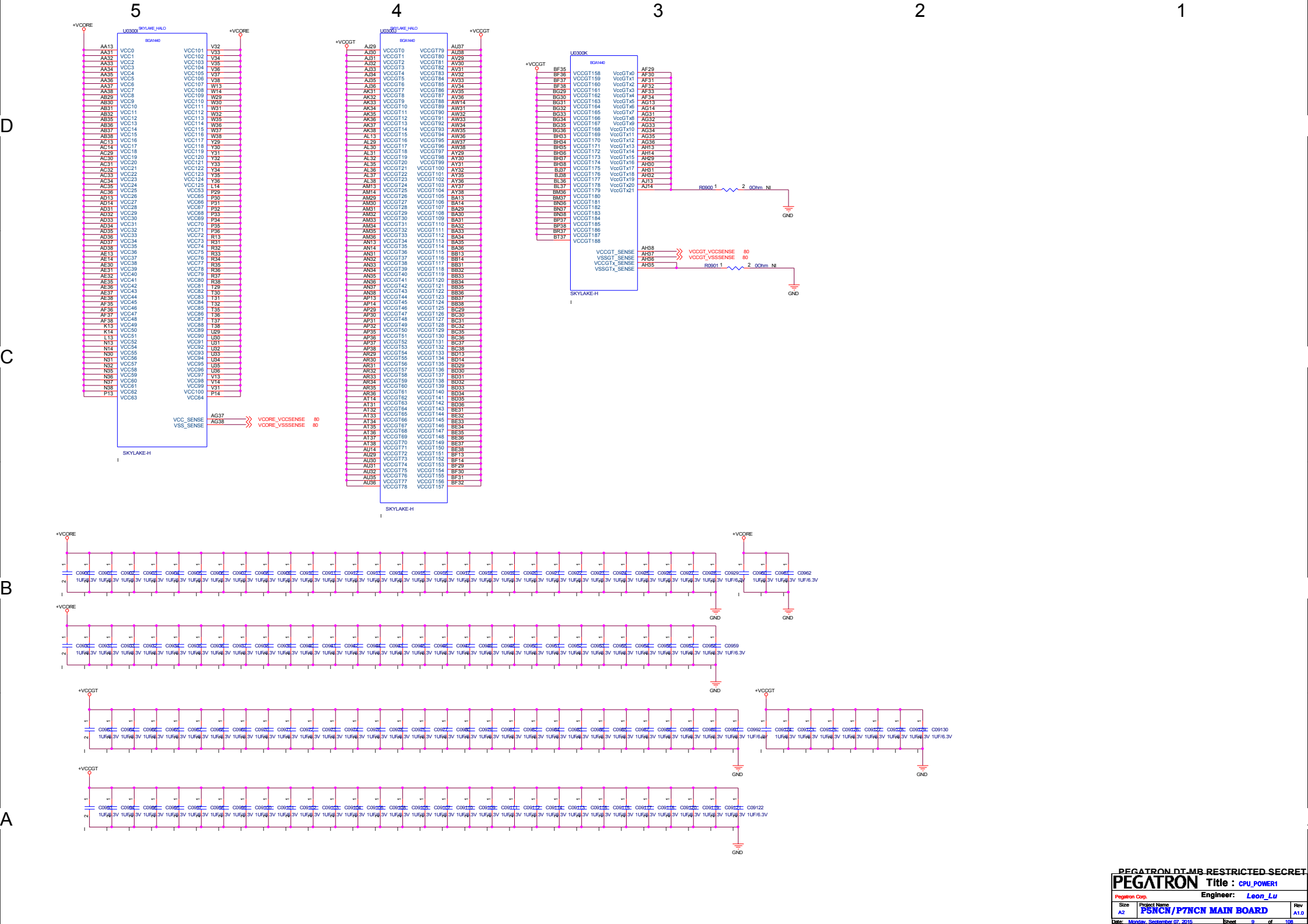
PEGATRON DT-MB RESTRICTED SECRET

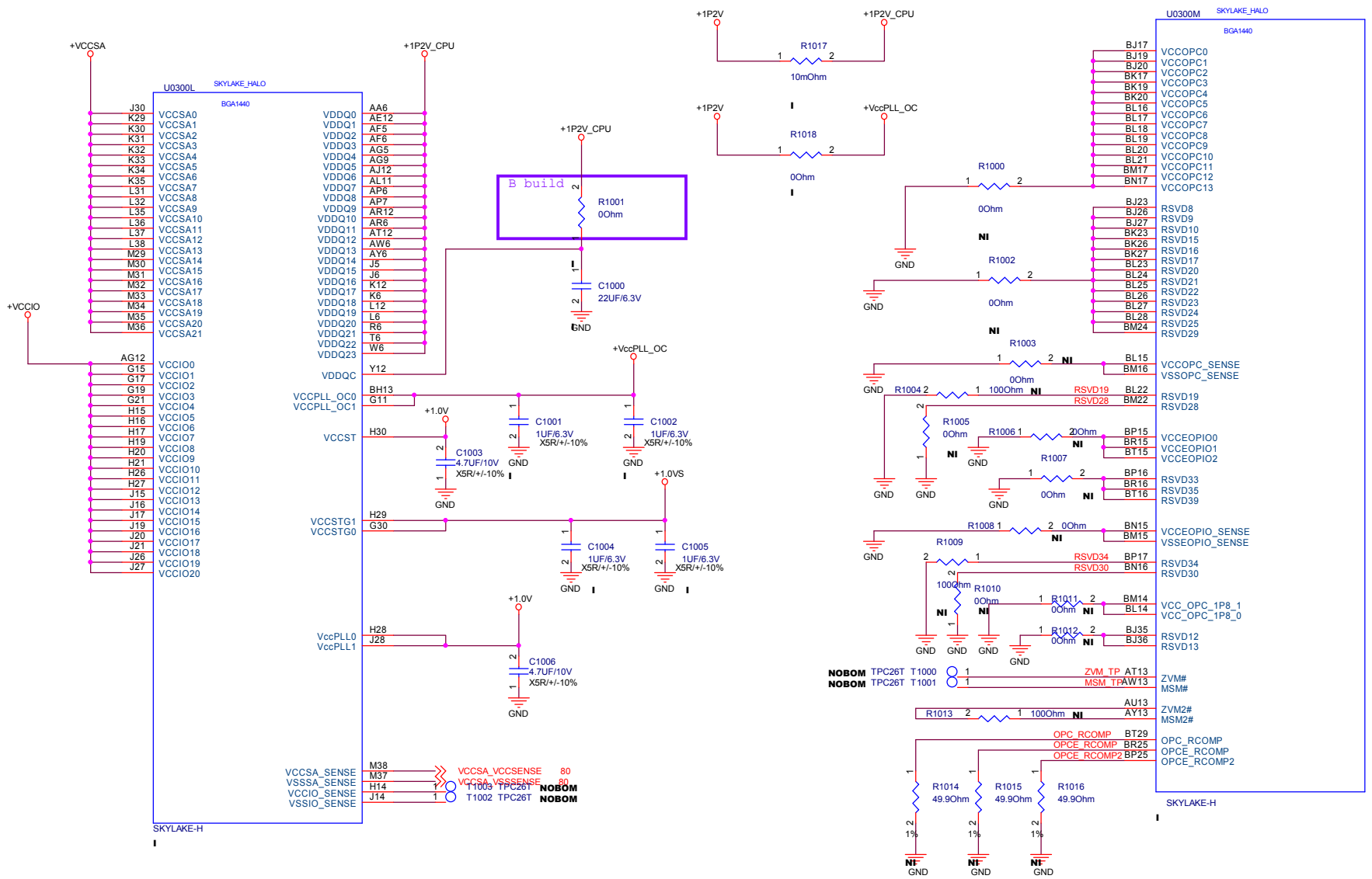
PEGATRON Title : CPU_VSS

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

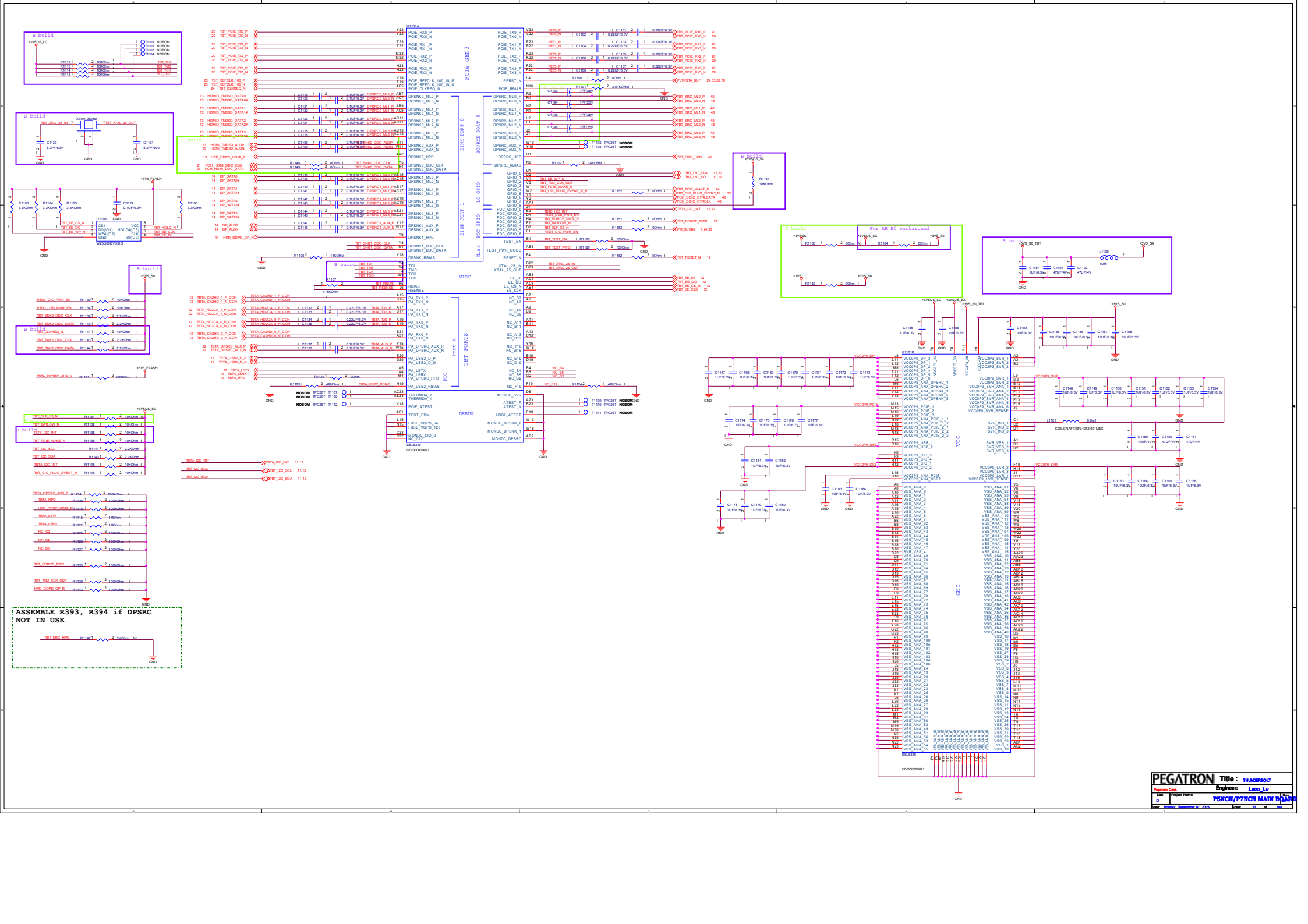
Date: Monday, September 07, 2015 Sheet 8 of 108

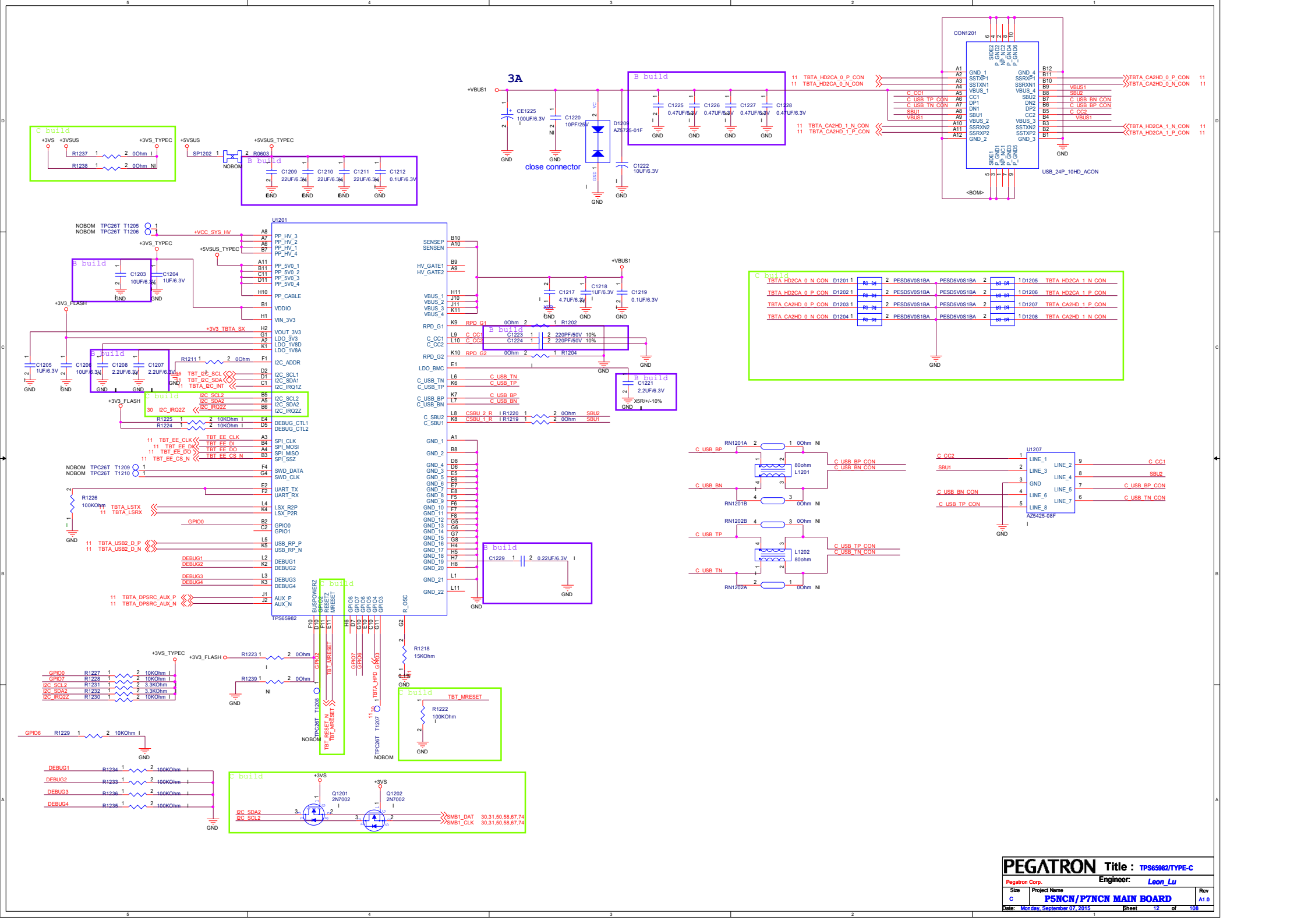

5
4
3
2
1
D
C
B
A
U0300I
SKYLAKE_HALO
BGA1440
SKYLAKE-H
U0300J
U0300K
+VCORE
+VCCGT
GND
VCC_SENSE
VSS_SENSE
VCORE_VCCSENSE
VCORE_VSSSENSE
VCCGT_SENSE
VSSGT_SENSE
VCCGTx_SENSE
VSSGTx_SENSE
VCCGT_VCCSENSE
VCCGT_VSSSENSE
R0900
R0901
0Ohm_NI
PEGATRON DT MB RESTRICTED SECRET
PEGATRON
Title : CPU_POWER1
Pegatron Corp.
Engineer: Leon_Lu
Size A2
Project Name PSNCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 9 of 108

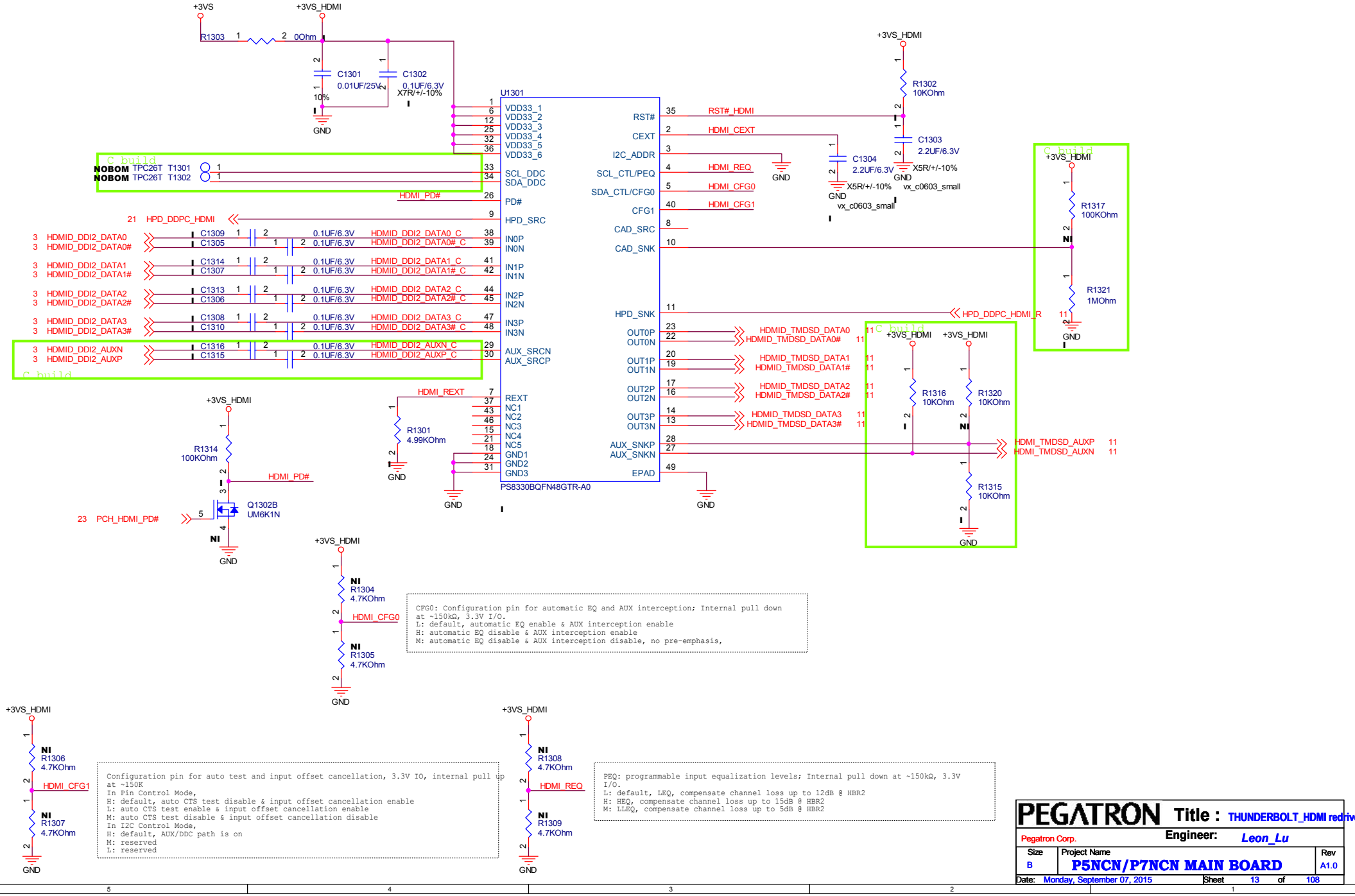


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CPU_POWER2	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A3	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 10 of 108	


B build
C build
J1901A
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
LC GPIO
SINK PORT 1
POC GPIO
Misc
MISC
TBT PORTS
Port A
POC
DEBUG
For AR B0 workaround
ASSEMBLE R393, R394 if DPSRC NOT IN USE
PEGATRON
Title : THUNDERBOLT
Engineer: Leon_Lu
P5NCK/P7NCN MAIN BOARD
Date: Monday, September 07, 2015


3A
close connector
CON1201
USB_24P_10HD_ACON
U1201
TPS65982
U1207
AZ5425-08F
Q1201 2N7002
Q1202 2N7002
PESD5V0S1BA
B build
C build
NOBOM
<BOM>
PEGATRON
Title : TPS65982/TYPE-C
Pegatron Corp.
Engineer: Leon_Lu
Size C
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 12 of 108

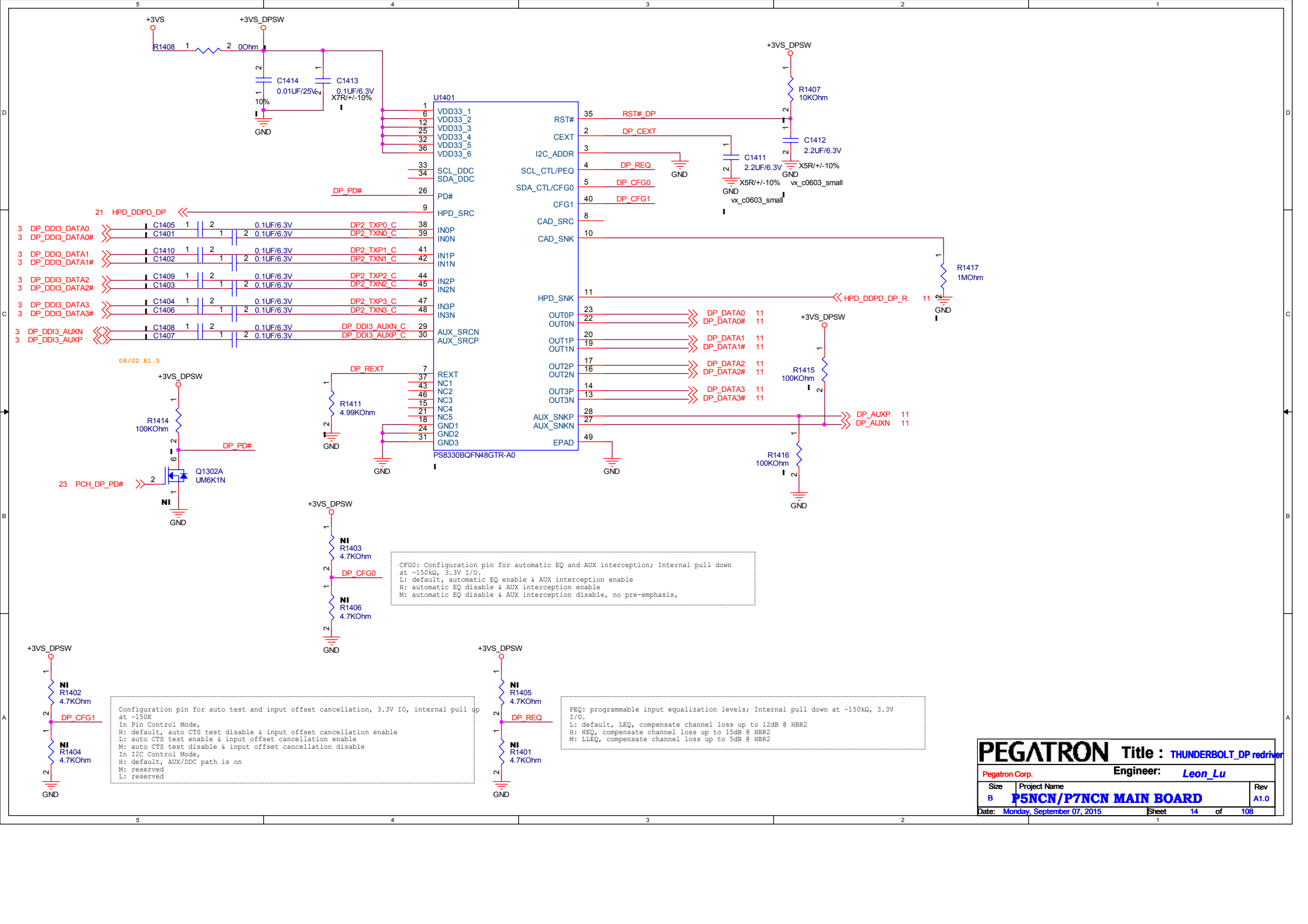


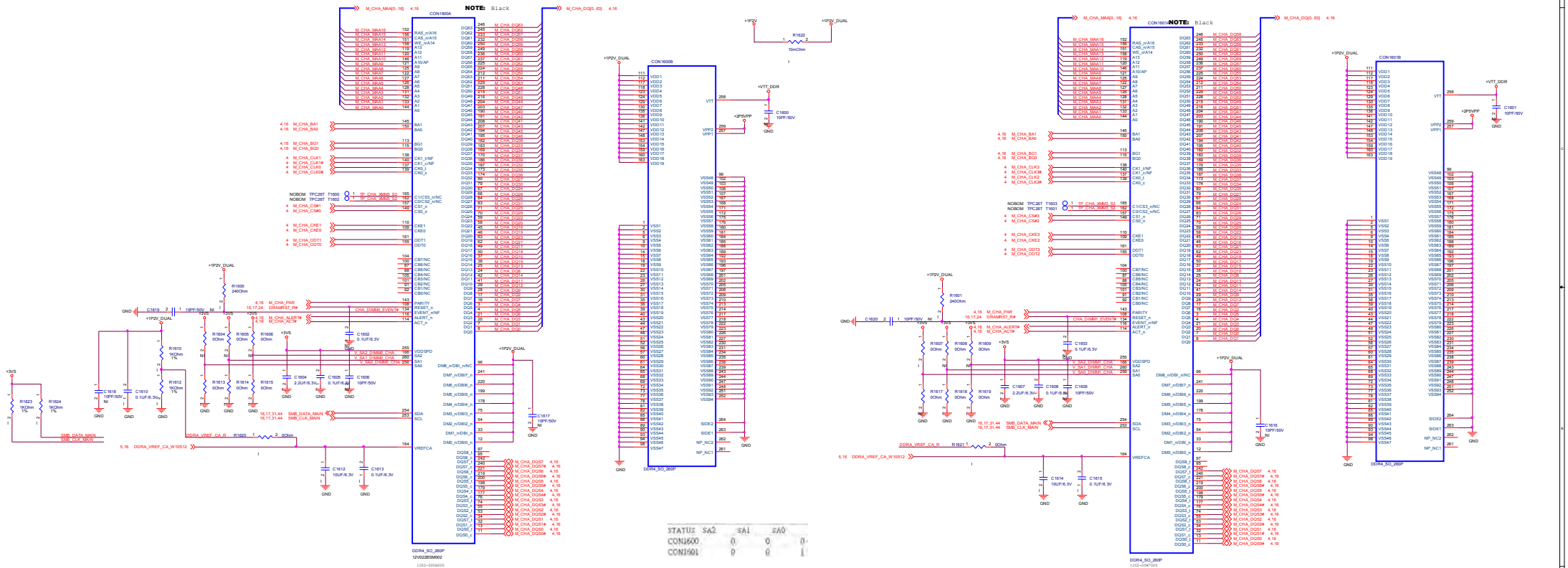
PEGATRON Title : THUNDERBOLT_HDMI redriver

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
B	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 13 of 108


+3VS
+3VS_DPSW
R1408 1 2 0Ohm
C1414 0.01UF/25V 10%
C1413 0.1UF/6.3V X7R/+/-10%
GND
U1401
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
VDD33_6
SCL_DDC
SDA_DDC
PD#
HPD_SRC
IN0P
IN0N
IN1P
IN1N
IN2P
IN2N
IN3P
IN3N
AUX_SRCN
AUX_SRCP
REXT
NC1
NC2
NC3
NC4
NC5
GND1
GND2
GND3
PS8330BQFN48GTR-A0
RST#
CEXT
I2C_ADDR
SCL_CTL/PEQ
SDA_CTL/CFG0
CFG1
CAD_SRC
CAD_SNK
HPD_SNK
OUT0P
OUT0N
OUT1P
OUT1N
OUT2P
OUT2N
OUT3P
OUT3N
AUX_SNKP
AUX_SNKN
EPAD
DP_PD#
DP_REXT
DP_RST#
DP_CEXT
DP_REQ
DP_CFG0
DP_CFG1
HPD_DDPD_DP
HPD_DDPD_DP_R
DP_DATA0
DP_DATA0#
DP_DATA1
DP_DATA1#
DP_DATA2
DP_DATA2#
DP_DATA3
DP_DATA3#
DP_AUXP
DP_AUXN
DP_DDI3_AUXN_C
DP_DDI3_AUXP_C
DP_TXP0_C
DP_TXN0_C
DP_TXP1_C
DP_TXN1_C
DP_TXP2_C
DP_TXN2_C
DP_TXP3_C
DP_TXN3_C
R1407 10KOhm
C1412 2.2UF/6.3V X5R/+/-10%
C1411 2.2UF/6.3V X5R/+/-10%
vx_c0603_small
R1417 1MOhm
R1415 100KOhm
R1416 100KOhm
R1414 100KOhm
R1411 4.99KOhm
Q1302A UM6K1N
PCH_DP_PD#
08/02 R1.5
R1403 4.7KOhm
R1406 4.7KOhm
R1402 4.7KOhm
R1404 4.7KOhm
R1405 4.7KOhm
R1401 4.7KOhm
NI
CFG0: Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis,
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
In Pin Control Mode,
H: default, auto CTS test disable & input offset cancellation enable
L: auto CTS test enable & input offset cancellation enable
M: auto CTS test disable & input offset cancellation disable
In I2C Control Mode,
H: default, AUX/DDC path is on
M: reserved
L: reserved
PEQ: programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2
PEGATRON
Title : THUNDERBOLT_DP redriver
Pegatron Corp.
Engineer: Leon_Lu
Size B
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 14 of 108



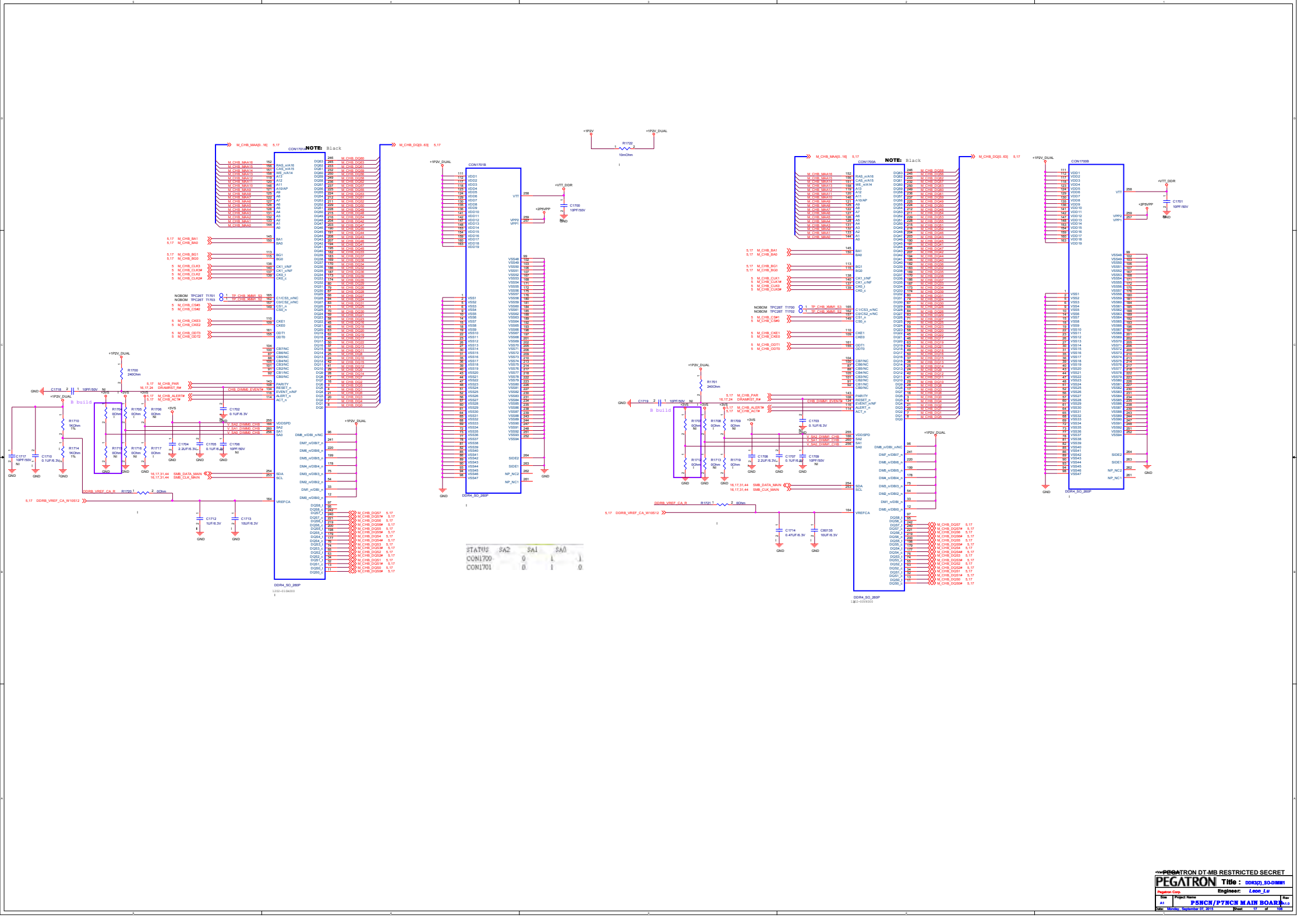
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3(I)_SO-DIMM0

Pegatron Corp. Engineer: Leon_Li

Size	Project Name	Rev
A1	P5NCN/P7NCN MAIN BOARD	1.0

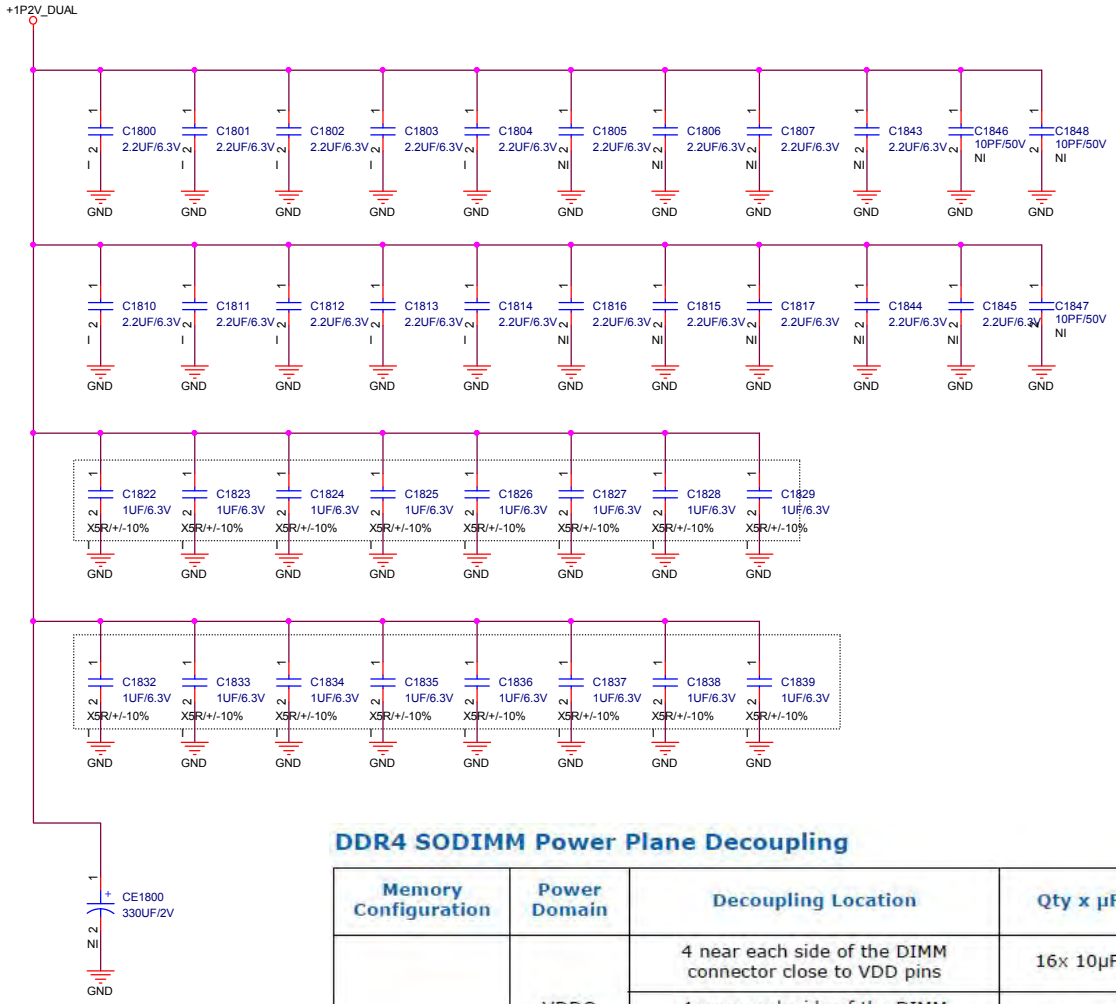
Date: Monday, September 07, 2015 Sheet 16 of 108



PEGATRON DT-MB RESTRICTED SECRET

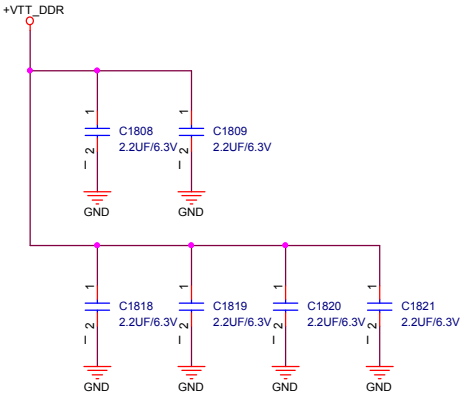
PEGATRON Corp.	Title : DDR3(2)_SO-DIMM1		
	Engineer: Leon_Lu		
Size: A1	Project Name: P5NCN/P7NCN MAIN BOARD		Rev: 1.0
Date: Monday, September 07, 2015	Sheet 17 of 108		

Need to check SODIMM DDR4 Termination Cap.



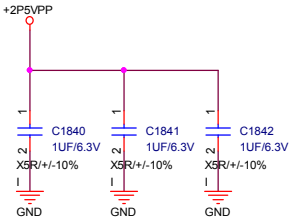
NOTE:
Place those cap close to CH A DIMM

NOTE:
Place those cap close to CH B DIMM



NOTE:
Place those cap close to CH A DIMM

NOTE:
Place those cap close to CH B DIMM



DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 22µF (0402)	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 TERMINATION A&B

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 18 of 108

NOTE:

PCH EDS 0.7

NOTE:

Lynx Point: USB2[0:13]

Sunrise Point PCH-H: USB2[1:14]

U2000A

DMI

6 DMI_TXP0	N27	DMI_RXP0
6 DMI_TXN0	L27	DMI_RXN0
6 DMI_RXP0	B27	DMI_TXP0
6 DMI_RXN0	C27	DMI_TXN0
6 DMI_TXP1	G24	DMI_RXP1
6 DMI_TXN1	E24	DMI_RXN1
6 DMI_RXP1	A28	DMI_TXP1
6 DMI_RXN1	B28	DMI_TXN1
6 DMI_TXP2	E26	DMI_RXP2
6 DMI_TXN2	G27	DMI_RXN2
6 DMI_RXP2	C29	DMI_TXP2
6 DMI_RXN2	B29	DMI_TXN2
6 DMI_TXP3	K29	DMI_RXP3
6 DMI_TXN3	L29	DMI_RXN3
6 DMI_RXP3	A30	DMI_TXP3
6 DMI_RXN3	B30	DMI_TXN3

PCIE/USB/ SATA

USB2.0

USB2P_1	AG7	IPD 14~24KOHM	USBP1 52	OC0
USB2N_1	AF5	IPD 14~24KOHM	USBN1 52	
USB2P_2	AD7	IPD 14~24KOHM	USBP2 55	OC2
USB2N_2	AD5	IPD 14~24KOHM	USBN2 55	
USB2P_3	AG10	IPD 14~24KOHM	USBP3 67	OC1
USB2N_3	AG8	IPD 14~24KOHM	USBN3 67	
USB2P_4	AE2	IPD 14~24KOHM	USBP4 67	
USB2N_4	AE1	IPD 14~24KOHM	USBN4 67	
USB2P_5	AC3	IPD 14~24KOHM		
USB2N_5	AC2	IPD 14~24KOHM		
USB2P_6	AF3	IPD 14~24KOHM		
USB2N_6	AF2	IPD 14~24KOHM		
USB2P_7	AB2	IPD 14~24KOHM	USBP7 53	
USB2N_7	AB3	IPD 14~24KOHM	USBN7 53	
USB2P_8	AL7	IPD 14~24KOHM	USBP8 43	
USB2N_8	AL8	IPD 14~24KOHM	USBN8 43	
USB2P_9	AA2	IPD 14~24KOHM	USBP9 45	
USB2N_9	AA1	IPD 14~24KOHM	USBN9 45	
USB2P_10	AJ7	IPD 14~24KOHM	USBP10 67	
USB2N_10	AJ8	IPD 14~24KOHM	USBN10 67	
USB2P_11	W3	IPD 14~24KOHM		
USB2N_11	W2	IPD 14~24KOHM		
USB2P_12	AD2	IPD 14~24KOHM		
USB2N_12	AD3	IPD 14~24KOHM		
USB2P_13	V1	IPD 14~24KOHM		
USB2N_13	V2	IPD 14~24KOHM		
USB2P_14	AJ13	IPD 14~24KOHM		
USB2N_14	AJ11	IPD 14~24KOHM		

LEFT USB3.0

SMALL CARD USB3.0

M.2 BT

TOUCH

WEBCAM

CARD READER

C build

3D CAMERA

43 USB3_TX_P5	B16	PCIE1_TXP/USB3_7_TXP
43 USB3_TX_N5	A16	PCIE1_TXN/USB3_7_TXN
43 USB3_RX_P5	G15	PCIE1_RXP/USB3_7_RXP
43 USB3_RX_N5	H15	PCIE1_RXN/USB3_7_RXN
	C19	PCIE2_TXP/USB3_8_TXP
	B19	PCIE2_TXN/USB3_8_TXN
	G17	PCIE2_RXP/USB3_8_RXP
	E17	PCIE2_RXN/USB3_8_RXN

M.2 WLAN

53 PCIE_TXP7_WLAN	C2020 1	2 0.1UF/6.3V	PCIE_TXP7_WLAN_C	C20
53 PCIE_TXN7_WLAN	C2021 1	2 0.1UF/6.3V	PCIE_TXN7_WLAN_C	B20
53 PCIE_RXP7_WLAN				K17
53 PCIE_RXN7_WLAN				L17
				PCIE3_TXP/USB3_9_TXP
				PCIE3_TXN/USB3_9_TXN
				PCIE3_RXP/USB3_9_RXP
				PCIE3_RXN/USB3_9_RXN

LAN RTL8111H

33 LAN_TXP	C2012 1	2 0.1UF/6.3V	PCIE_LAN_TXP	A21
33 LAN_TXN	C2013 1	2 0.1UF/6.3V	PCIE_LAN_TXN	B21
33 LAN_RXP				G19
33 LAN_RXN				E20
				PCIE4_TXP/USB3_10_TXP
				PCIE4_TXN/USB3_10_TXN
				PCIE4_RXP/USB3_10_RXP
				PCIE4_RXN/USB3_10_RXN

Thunderbolt

11 TBT_PCIE_TX0_P	C2000 1	2 0.1UF/6.3V	TBT_PCIE_TX0_P_C	C22
11 TBT_PCIE_TX0_N	C2001 1	2 0.1UF/6.3V	TBT_PCIE_TX0_N_C	D22
11 TBT_PCIE_RX0_P				L19
11 TBT_PCIE_RX0_N				K19
				PCIE5_TXP
				PCIE5_TXN
				PCIE5_RXP
				PCIE5_RXN
11 TBT_PCIE_TX1_P	C2015 1	2 0.1UF/6.3V	TBT_PCIE_TX1_P_C	A23
11 TBT_PCIE_TX1_N	C2014 1	2 0.1UF/6.3V	TBT_PCIE_TX1_N_C	B22
11 TBT_PCIE_RX1_P				E22
11 TBT_PCIE_RX1_N				G22
				PCIE6_TXP
				PCIE6_TXN
				PCIE6_RXP
				PCIE6_RXN
11 TBT_PCIE_TX2_P	C2017 1	2 0.1UF/6.3V	TBT_PCIE_TX2_P_C	B23
11 TBT_PCIE_TX2_N	C2016 1	2 0.1UF/6.3V	TBT_PCIE_TX2_N_C	C23
11 TBT_PCIE_RX2_P				K22
11 TBT_PCIE_RX2_N				L22
				PCIE7_TXP
				PCIE7_TXN
				PCIE7_RXP
				PCIE7_RXN
11 TBT_PCIE_TX3_P	C2019 1	2 0.1UF/6.3V	TBT_PCIE_TX3_P_C	B24
11 TBT_PCIE_TX3_N	C2018 1	2 0.1UF/6.3V	TBT_PCIE_TX3_N_C	C24
11 TBT_PCIE_RX3_P				L24
11 TBT_PCIE_RX3_N				K24
				PCIE8_TXP
				PCIE8_TXN
				PCIE8_RXP
				PCIE8_RXN

SATA Port1 (SSD)

51 PCIE_SATA_TXP0	B31	PCIE9_TXP/SATA0A_TXP
51 PCIE_SATA_TXN0	C31	PCIE9_TXN/SATA0A_TXN
51 PCIE_SATA_RXP0	H31	PCIE9_RXP/SATA0A_RXP
51 PCIE_SATA_RXN0	G31	PCIE9_RXN/SATA0A_RXN

SATA Port1 (SSD)

51 PCIE_SATA_TXP1	B32	PCIE10_TXP/SATA1A_TXP
51 PCIE_SATA_TXN1	C32	PCIE10_TXN/SATA1A_TXN
51 PCIE_SATA_RXP1	E29	PCIE10_RXP/SATA1A_RXP
51 PCIE_SATA_RXN1	G29	PCIE10_RXN/SATA1A_RXN

SATA Port1 (SSD)

51 PCIE_SATA_TXP2	B33	PCIE11_TXP
51 PCIE_SATA_TXN2	C33	PCIE11_TXN
51 PCIE_SATA_RXP2	K31	PCIE11_RXP
51 PCIE_SATA_RXN2	L31	PCIE11_RXN

SATA Port1 (SSD)

51 PCIE_SATA_TXP3	A35	PCIE12_TXP
51 PCIE_SATA_TXN3	B35	PCIE12_TXN
51 PCIE_SATA_RXP3	H33	PCIE12_RXP
51 PCIE_SATA_RXN3	G33	PCIE12_RXN

USB3.0

USB3_1_TXP	B11			
USB3_1_TXN	C11			
USB3_1_RXP	A7			
USB3_1_RXN	B7			
USB3_2_TXP/SSIC_1_TXP	A12	USB3_TX_P2_C	C2004 1 2 0.1UF/6.3V	USB3_TX_P2 55
USB3_2_TXN/SSIC_1_TXN	B12	USB3_TX_N2_C	C2005 1 2 0.1UF/6.3V	USB3_TX_N2 55
USB3_2_RXP/SSIC_1_RXP	B8			USB3_RX_P2 55
USB3_2_RXN/SSIC_1_RXN	C8			USB3_RX_N2 55
USB3_3_TXP/SSIC_2_TXP	D13	USB3_TX_P3_C	C2006 1 2 0.1UF/6.3V	USB3_TX_P3 67
USB3_3_TXN/SSIC_2_TXN	C13	USB3_TX_N3_C	C2007 1 2 0.1UF/6.3V	USB3_TX_N3 67
USB3_3_RXP/SSIC_2_RXP	A9			USB3_RX_P3 67
USB3_3_RXN/SSIC_2_RXN	B10			USB3_RX_N3 67
USB3_4_TXP	B13	USB3_TX_P4_C	C2009 1 2 0.1UF/6.3V	USB3_TX_P4 67
USB3_4_TXN	A14	USB3_TX_N4_C	C2011 1 2 0.1UF/6.3V	USB3_TX_N4 67
USB3_4_RXP	G11			USB3_RX_P4 67
USB3_4_RXN	E11			USB3_RX_N4 67
USB3_5_TXP	C14	USB3_TX_P1_C	C2002 1 2 0.1UF/6.3V	USB3_TX_P1 55
USB3_5_TXN	B14	USB3_TX_N1_C	C2003 1 2 0.1UF/6.3V	USB3_TX_N1 55
USB3_5_RXP	H13			USB3_RX_P1 55
USB3_5_RXN	G13			USB3_RX_N1 55
USB3_6_TXP	C15			USB3_TX_P6 67
USB3_6_TXN	B15			USB3_TX_N6 67
USB3_6_RXP	K13			USB3_RX_P6 67
USB3_6_RXN	K15			USB3_RX_N6 67

LEFT USB3.0(SIDE)

USB3.0

C build

LEFT USB3.0(SIDE)

USB3.0 CARD

USB2_ID	AG2	IWPU	USB2_ID
USB2_VBUSSENSE	AD10		USB2_VBUSSENSE

R2000 1KOhm

R2001 0Ohm

GND GND

SKYLAKE_PCH Rev 0.9

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_DMI/PCIE

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 20 of 108

NOTE:
Check PU/PD

NOTE:
CPU_GP can be used from external sensors for the thermal management.

NOTE:
Check real OC# application

NOTE:
NI SR39(POLYSWITCH)
I SR39(POWER SWITCH)

STATUS	CTL1	CTL2	CTL3	ILIM_SEL
S0(CDP)	1	1	1	1
S3(CDP)	1	1	1	1
S4(DCP)	0	0	1	0
S5(DCP)	0	0	1	0

NOTE:
GPP_F[11:10] for SWITCH#0 to select source from ISH or HOST

NOTE:

SATAXPCIE[0:7]	SATA/PCIE
SATAXPCIE0	SATA0A/PCIE9 SATA0B/PCIE13
SATAXPCIE1	SATA1A/PCIE10 SATA1B/PCIE14
SATAXPCIE2	SATA2/PCIE15
SATAXPCIE3	SATA3/PCIE16
SATAXPCIE4	SATA4/PCIE17
SATAXPCIE5	SATA5/PCIE18
SATAXPCIE6	SATA5/PCIE19
SATAXPCIE7	SATA7/PCIE20

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_SATA/PCIE

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 21 of 108

NOTE:
eSPI operates at 1.8V

NOTE:
Check SERIRQ & PIRQA volt level

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

NOTE:
Check GPP_A0 power well

NOTE:
ESPI_ALERT[0:1]# & ESPI_CS1# are Server Only
ESPI interface are Primary Well

NOTE:
Check PCA spec for specific implementation

NOTE:
CLKOUT_LPC[0:1] are 24MHz(TBD) with Rs=22ohm
ESPI_CLK is xxHz with Rs=15ohm

NOTE:
Check PCA spec SIO_SMI# to GPIO or SMI#?

NOTE:
TBD; Check ISH GPIO[0:7]
PU/PD and power rail

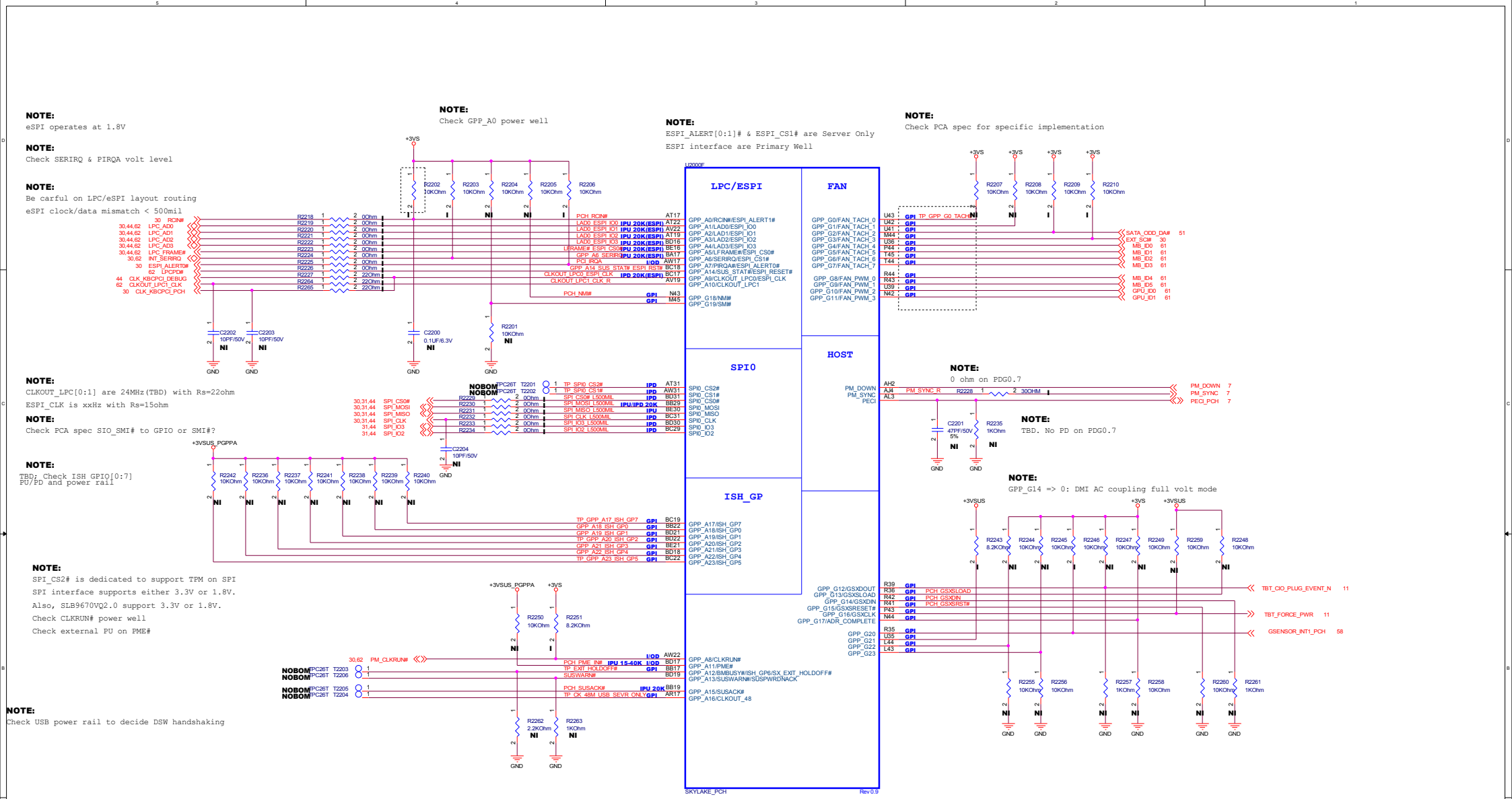
NOTE:
SPI_CS2# is dedicated to support TPM on SPI
SPI interface supports either 3.3V or 1.8V.
Also, SLB9670VQ2.0 support 3.3V or 1.8V.
Check CLKRUN# power well
Check external PU on PME#

NOTE:
Check USB power rail to decide DSW handshaking

NOTE:
0 ohm on PDG0.7

NOTE:
TBD. No PD on PDG0.7

NOTE:
GPP_G14 => 0: DMI AC coupling full volt mode



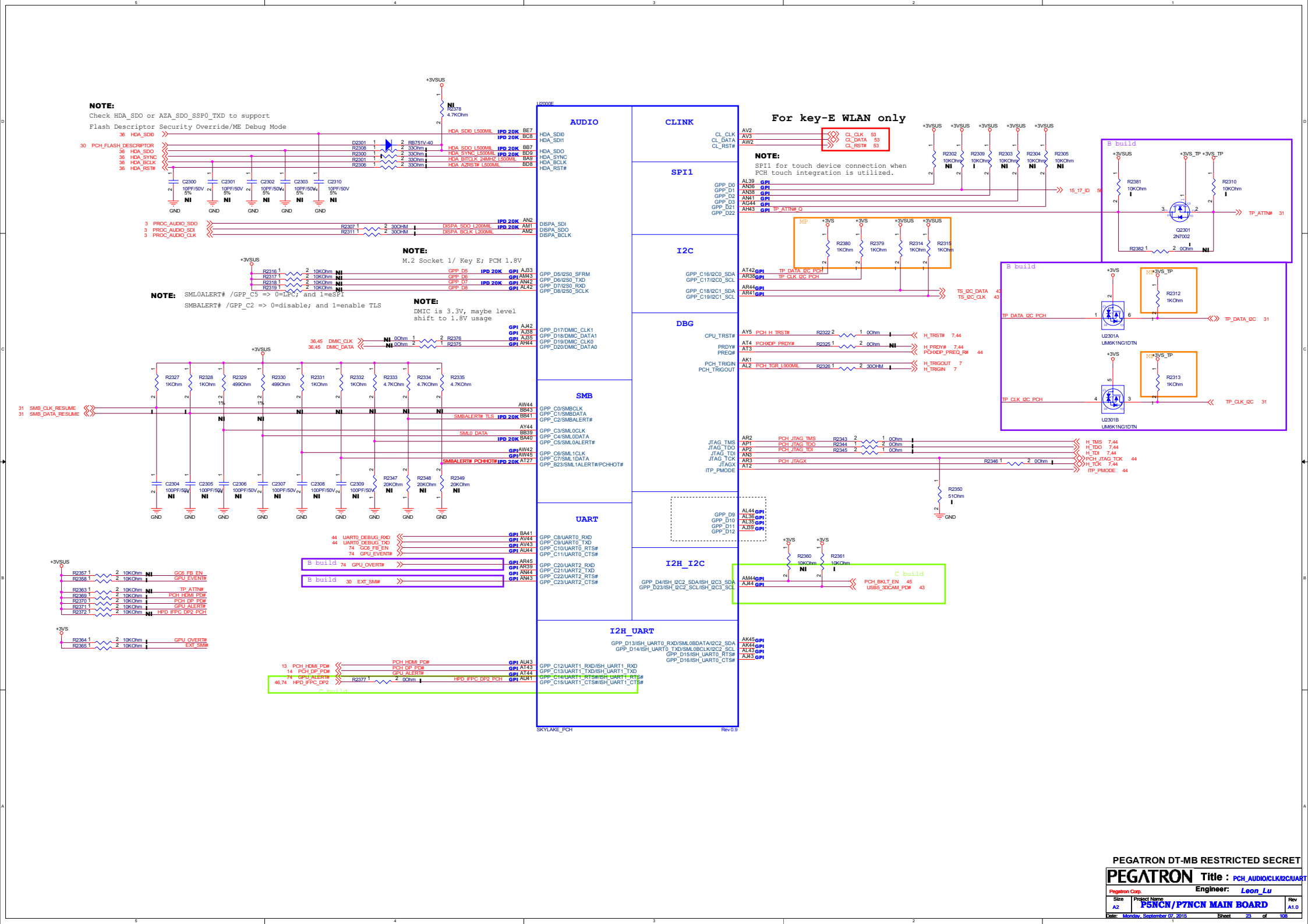
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_ESPI/SPI/FAN/HOST

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 22 of 108


NOTE:
Check HDA_SDO or AZA_SDO_SSP0_TXD to support
Flash Descriptor Security Override/ME Debug Mode
NOTE:
M.2 Socket 1/ Key E; PCM 1.8V
NOTE:
SML0ALERT# /GPP_C5 => 0=LPC; and 1=eSPI
SMBALERT# /GPP_C2 => 0=disable; and 1=enable TLS
NOTE:
DMIC is 3.3V, maybe level shift to 1.8V usage
For key-E WLAN only
NOTE:
SPI1 for touch device connection when PCH touch integration is utilized.
AUDIO
CLINK
SPI1
I2C
DBG
SMB
UART
I2H_I2C
I2H_UART
B build
C build
MP
SKYLAKE_PCH
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCH_AUDIO/CLK/I2C/UART
Engineer: Leon_Lu
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Monday, September 07, 2015
Sheet 23 of 108

NOTE:
GPP_B22/GSPI1_MOSI

Offset 3410h:Bit 10
0: SPI
1: LPC

NOTE:
GSPI is not the same as SPI

It's used mainly for sensor

NOTE:
GSPI0_MOSI/GPP_B18

0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

NOTE:
HP PCA spec request probe points

NOTE:
1.DRAM_RESET# used on DDR3L, DDR4. Not applicable to LPDDR3

2.Check PCA spec if we need isolation CKT

since DRAM_RESET# is changed from SHB processor to SKL PCH assertion

3.Also be careful while changing push-pull to OD

4. PU 475ohm on Zumba Beach CRB 0.5

NOTE:
PCH_PWROK and VCCST_PWRGD
have the same timing

NOTE:
Check PCH PLL VSB(PRIM) and GPIO PU(GPO) MAIN power W/O IPD 20Kohm.

Ex: GPP_B11

NOTE:
GPD7/RSVD

NOTE:
SPKR/GPP_B14

0 = Disable "Top Swap" mode.(Default)
1 = Enable "Top Swap" mode

NOTE:
SML[2:4] are
Server Only

SYS_PWROK for PCH

U2000D

GSPI

ISH_I2C

SKYLAKE_PCH

Rev 0.9

PEGATRON DT MB RESTRICTED SECRET

PEGATRON Title : PCH_SML

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 24 of 108

NOTE:

CRB: 2.71Kohm

Refer to GND; NOT near switching noise; spacing 3x

Add a GND shield(Width>4 mils)

between XCLK_BIASREF and adjacent IO signals

U2000C

CLOCK

7 CK_100M_BCK — R2500 — CK_100M_85OHM_BCK — G2 — CLKOUT_CPUBCLK_P
7 CK_100M_BCK# — R2501 — CK_100M_85OHM_BCK# — H2 — CLKOUT_CPUBCLK_N

7 CK_24M_BCK — R2503 — CK_24M_85OHM_BCK — G1 — CLKOUT_CPUNSSC_P
7 CK_24M_BCK# — R2505 — CK_24M_85OHM_BCK# — F1 — CLKOUT_CPUNSSC_N

7 CK_100M_PCIE — R2510 — CK_100M_85OHM_PCIE — J2 — CLKOUT_CPUPCIBCLK_P
7 CK_100M_PCIE# — R2511 — CK_100M_85OHM_PCIE# — J1 — CLKOUT_CPUPCIBCLK_N

44 CK_100M_CPUXDP — R2507 — CK_100M_85OHM_CPUXDP — L2 — CLKOUT_ITPXDP_P
44 CK_100M_CPUXDP# — R2508 — CK_100M_85OHM_CPUXDP# — L1 — CLKOUT_ITPXDP_N

All resistors: 0Ohm, 1%

+1.0VSUS — R2512 2.7KOhm — XCLK_BIASREF — E1 — XCLK_BIASREF

R2516 100Ohm — PCIE_RCOMPP — C17 — PCIE_RCOMPP
PCIE_RCOMPN — B18 — PCIE_RCOMPN

NOBOM TPC26T T2500 — TP_PCH_RSVD_BD1 — BD1
NOBOM TPC26T T2501 — TP_PCH_RSVD_BE2 — BE2

AN17 TP1
AR19 TP2

RSVD3 N29
RSVD4 N31
RSVD5 P24
RSVD6 P27
RSVD7 P29
RSVD8 P31
RSVD9 R24
RSVD10 R27
RSVD11 U13
RSVD12 W13
RSVD13 AB13
RSVD14 AE17
RSVD15 AF17
RSVD16 AG14
RSVD17 AG15
RSVD18 AN29
RSVD19 AR22
RSVD20 BD1
RSVD21 BE2

CLKOUT_PCIE_P0 — N8 — CK_100M_PE0_R — R2509 — CK_100M_PE0 53 — M2 WLAN
CLKOUT_PCIE_N0 — N7 — CK_100M_PE0#_R — R2502 — CK_100M_PE0# 53 — M2 WLAN
CLKOUT_PCIE_P1 — L5
CLKOUT_PCIE_N1 — L7
CLKOUT_PCIE_P2 — F2
CLKOUT_PCIE_N2 — D3
CLKOUT_PCIE_P3 — G4 — TBT_REFCLK_100_P_R — R2527 — TBT_REFCLK_100_P 11 — Thunderbolt
CLKOUT_PCIE_N3 — E5 — TBT_REFCLK_100_N_R — R2528 — TBT_REFCLK_100_N 11 — Thunderbolt
CLKOUT_PCIE_P4 — E6
CLKOUT_PCIE_N4 — D5
CLKOUT_PCIE_P5 — D7
CLKOUT_PCIE_N5 — D8
CLKOUT_PCIE_P6 — R7
CLKOUT_PCIE_N6 — R8
CLKOUT_PCIE_P7 — U7
CLKOUT_PCIE_N7 — U5
CLKOUT_PCIE_P8 — W11 — CK_100M_PE8_R — R2515 — CK_100M_PE8 51 — M2 SSD
CLKOUT_PCIE_N8 — W10 — CK_100M_PE8#_R — R2517 — CK_100M_PE8# 51 — M2 SSD
CLKOUT_PCIE_P9 — N2 — PCIE_CLK_P_GPU_R — R2518 — PCIE_CLK_P_GPU 70 — GPU
CLKOUT_PCIE_N9 — N3 — PCIE_CLK_N_GPU_R — R2519 — PCIE_CLK_N_GPU 70 — GPU
CLKOUT_PCIE_P10 — P2 — CK_100M_LAN_R — R2520 — CK_100M_LAN 33 — LAN
CLKOUT_PCIE_N10 — P3 — CK_100M_LAN#_R — R2521 — CK_100M_LAN# 33 — LAN
CLKOUT_PCIE_P11 — R4
CLKOUT_PCIE_N11 — R3
CLKOUT_PCIE_P12 — U3
CLKOUT_PCIE_N12 — U2
CLKOUT_PCIE_P13 — Y5
CLKOUT_PCIE_N13 — W7
CLKOUT_PCIE_P14 — R2
CLKOUT_PCIE_N14 — P1
CLKOUT_PCIE_P15 — R11
CLKOUT_PCIE_N15 — R13

All resistors: 0Ohm, 1%

NOTE:

RVP 10 CRB 0.5 use 30.1K ohm on RTCRST#

28 RTCRST# — BC10 — RTCRST#

RTCX1_NO_IO — BC9 — RTCX1
RTCX2_NO_IO — BD10 — RTCX2

R2523 10MOhm
R2525 0Ohm
Y2500 32.768KHZ — Y5_R
C2500 18PF/50V
C2501 18PF/50V
GND

NOTE:

Be careful on RTC crystal(routing and test point) on AiO

Instead of DIP to SMD if possible

Reduce trace length mismatch between RTCX1 & RTCX2

Do NOT route High Speed or GPIO(tie to header/connector) near X'tal region

SKYLAKE_PCH
02V000000020
Rev 0.9

NOTE:

Check 24MHz crystal spec

XTAL24_IN — A6 — XTAL24_IN_R — R2522 — XTAL24_IN_NO_IO
XTAL24_OUT — A5 — XTAL24_OUT_NO_IO

USB2_COMP — AG3 — USB2_COMP

RSVD1 — C1 — PCH_C1 — T2502 TPC26T
RSVD2 — D1 — PCH_D1 — T2503 TPC26T
NOBOM NOBOM

R2526 113Ohm
R2524 1MOhm
Y2501 24MHZ
C2502 27PF/50V
C2503 27PF/50V
C build
GND

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_CLOCK

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

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NOTE:
Add 2x 22uF(instead of 47uF) 0603 caps
on 3.3V/1.8V/1.0V plane at PCH
Check 22uF qty on power CKT

NOTE:
Check real GPIO implementation to decide VccGPIO rail is 3.3V or 1.8V

U2000G

PRIMARY
VCCPRIM_1p0_17
VCCPRIM_1p0_13
VCCPRIM_1p0_14
VCCPRIM_1p0_15
VCCPRIM_1p0_16
VCCPRIM_1p0_6
VCCPRIM_1p0_10
VCCPRIM_1p0_2
VCCPRIM_1p0_1
VCCPRIM_1p0_4
VCCPRIM_1p0_3
VCCPRIM_1p0_5
VCCPRIM_1p0_9
VCCPRIM_1p0_12
VCCPRIM_1p0_11
VCCPRIM_1p0_8
VCCPRIM_1p0_7

CLOCK
VCCCLK5_1
VCCCLK5_2
VCCCLK1
VCCCLK3
VCCCLK4
VCCCLK2_2
VCCCLK2_1

MPHY
VCCMPHY_1p0_1
VCCMPHY_1p0_2
VCCMPHY_1p0_3
VCCMPHY_1p0_4
VCCMPHY_1p0_5

VCCAMPHYPLL_1p0_1
VCCAMPHYPLL_1p0_2
VCCPCIE3PLL_1p0_1
VCCPCIE3PLL_1p0_2

VCCAPLLEBB_1p0
VCCUSB2PLL_1p0_1
VCCUSB2PLL_1p0_2
VCCHDAPLL_1P0

DCPDSW_1p0
DCPRTC

SKYLAKE_PCH
02V000000020
Rev 0.9

VCCGPIO
VCCPGPPA
VCCPGPPBCH1
VCCPGPPBCH2
VCCPGPPEF1
VCCPGPPEF2
VCCPGPPG
VCCPGPPD3
VCCPGPPD1
VCCPGPPD4
VCCPGPPD2

SPI
VCCSPI1
VCCSPI3
VCCSPI2

PRIMARY
VCCPRIM_3p3_2
VCCPRIM_3p3_3
VCCPRIM_3p3_4
VCCPRIM_3p3_1
VCCRTCPRIM_3p3

VCCATS
VCCDSW_3p3_2
VCCDSW_3p3_1
VCCHDA
VCCRTC

+1.0VSUS
R2613 1 2 10mOhm +1V_PRIM_W12MIL
Icc(max):6.01A
C2600 22UF/6.3V
C2601 22UF/6.3V
GND

R2604 0Ohm
Icc(max):0.006A
+V1P0A_VCCF24_W15MIL
C2605 22UF/6.3V
C2606 22UF/6.3V NI
C2607 1UF/6.3V
Icc(max):0.232A

NOTE:
Reserve 0 ohm/0603 for 2.2uH Series Inductor

Icc(max):0.08A
C2608 22UF/6.3V
C2609 1UF/6.3V

R2606 0Ohm
Icc(max):0.08A
+V1P0A_VCCAMPHYPLL_W25MIL
C2613 22UF/6.3V
C2614 22UF/6.3V NI
C2615 1UF/6.3V

NOTE:
Place to U3.U21
PDG request 22uF 0805

NOTE:
Place to U3.A43

R2607 0Ohm
Icc(max):0.045A
+V1P0A_VCCAPLL_W15MIL
Icc(max):0.03A
C2618 22UF/6.3V
C2619 22UF/6.3V NI

+1V_DCPDSW
DCPRTC
C2622 1UF/6.3V
C2623 0.1UF/6.3V

+3VSUS_PGPPA
Icc(max):0.082A
B build
SP2601 1 2 R0603
NOBOM

Icc(max):0.408A
B build
C2601 0.1UF/6.3V
C2602 0.1UF/6.3V
C2603 0.1UF/6.3V
C2604 0.1UF/6.3V
R2615 1 2 0Ohm +3VSUS

NOTE:
Place 0.1uF near U3.BC42/ AJ41/ AD41 pins

NOTE:
Add 2x 22uF(instead of 47uF) 0603 caps
on 3.3V/1.8V/1.0V plane at PCH
Check 22uF qty on power CKT

Icc(max):0.078A
+VCCPGPPCD_W15MIL
R2603 0Ohm +3VSUS

NOTE:

GPIO Group	Power Pins	Voltage
Primary Well Group A(GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B(GPP_B) Primary Well Group C(GPP_C) Primary Well Group H(GPP_H)	VCCPGPPBCH	1.8V or 3.3V
Primary Well Group D(GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E(GPP_E) Primary Well Group F(GPP_F)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group G(GPP_G)	VCCPGPPG	1.8V or 3.3V
Primary Well Group I(GPP_I)	VCCPRIM_3P3	3.3V
Deep Sleep Well Group(GPD)	VCCDSW_3P3	3.3V

B build
Icc(max):0.029A
R2616 1 2 0Ohm +3VSUS +3VA
R2619 1 2 0Ohm NI

NOTE:
1.8V SPI(with Quad IO) is expensive than 3.3V part.

Icc(max):0.117A
+VCCPFUSE_W20MIL
R2605 2 1 0Ohm +3VSUS
C2610 0.1UF/6.3V NI
C2611 22UF/6.3V
C2612 22UF/6.3V
Icc(max):0.001A
C2616 0.1UF/6.3V NI
C2617 1UF/6.3V

NOTE:
Place 0.1uF near U3.AN5

Icc(max):0.007A
R2618 1 2 0Ohm +3VS
Icc(max):0.195A
R2617 1 2 0Ohm +3VSUS
C2621 1UF/6.3V
C2620 1UF/6.3V

NOTE:
Place 1uF near U3.W15

Icc(max):0.06A
+DVDDIO_AUDIO_W10MIL
R2608 2 1 0Ohm +3VSUS
Icc(max):0.001A
+VCCRTC_W8MIL
R2609 2 1 0Ohm +VCC_RTC
C2629 0.1UF/6.3V
C2624 0.1UF/6.3V NI
C2625 1UF/6.3V

PEGATRON Title : PCH_VCC
Pegatron Corp. Engineer: Leon_Lu
Size A3 | Project Name P5NCN/P7NCN MAIN BOARD | Rev A1.0
Date: Monday, September 07, 2015 Sheet 26 of 108

PEGATRON

Title : PCH_VSS

Pegatron Corp.

Engineer: Leon_Lu

Size	Project Name	Rev
A4	P5NCN/P7NCN MAIN BOARD	A1.0

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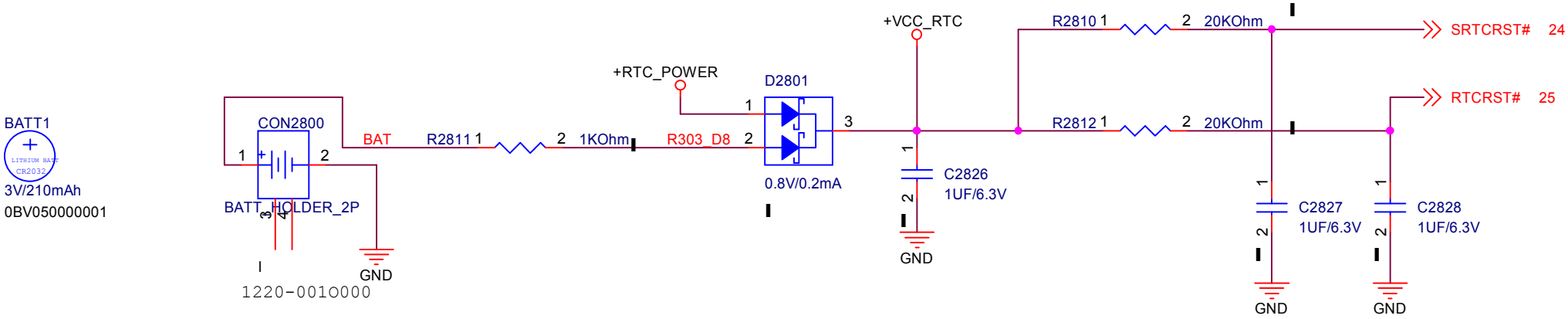
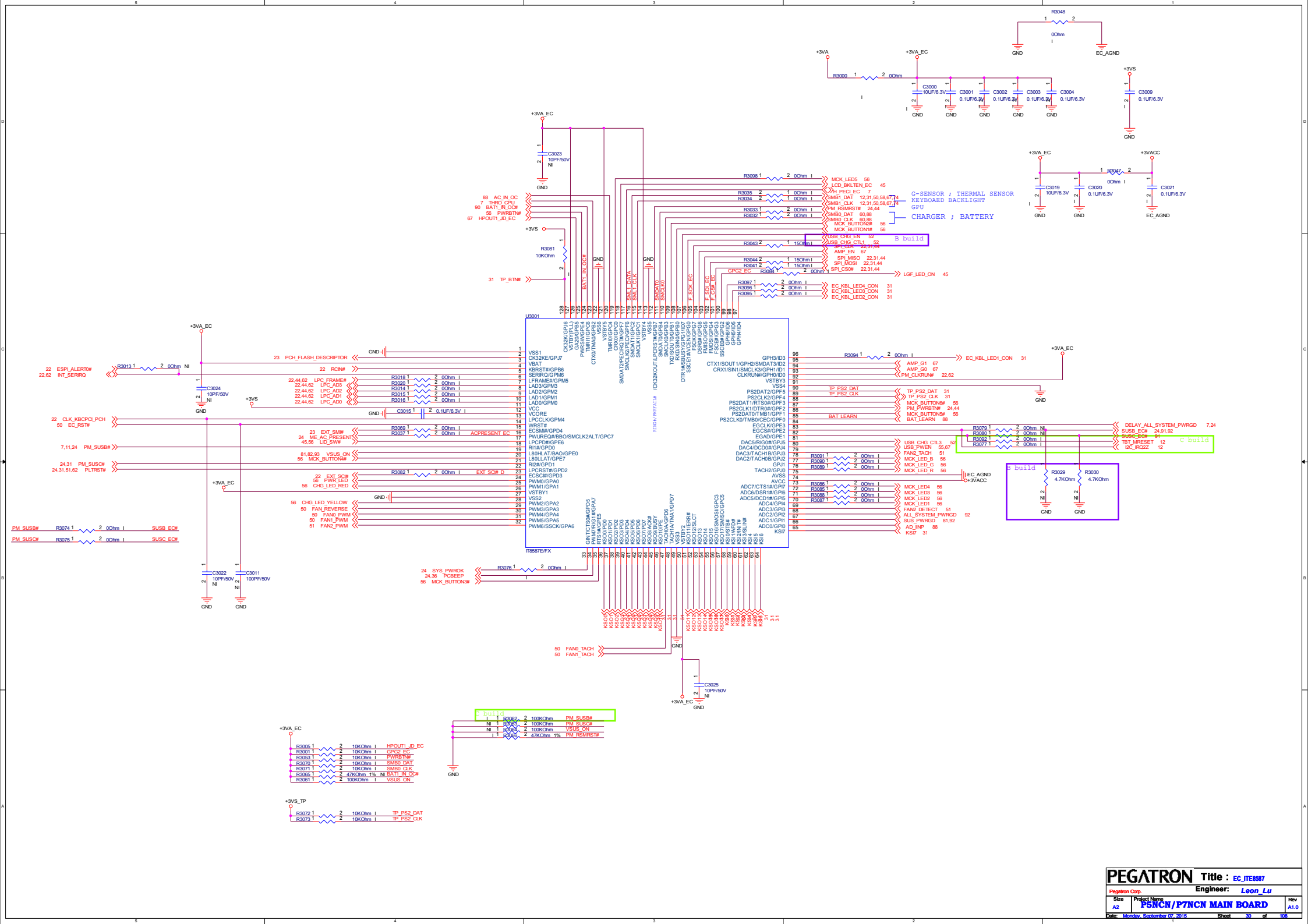
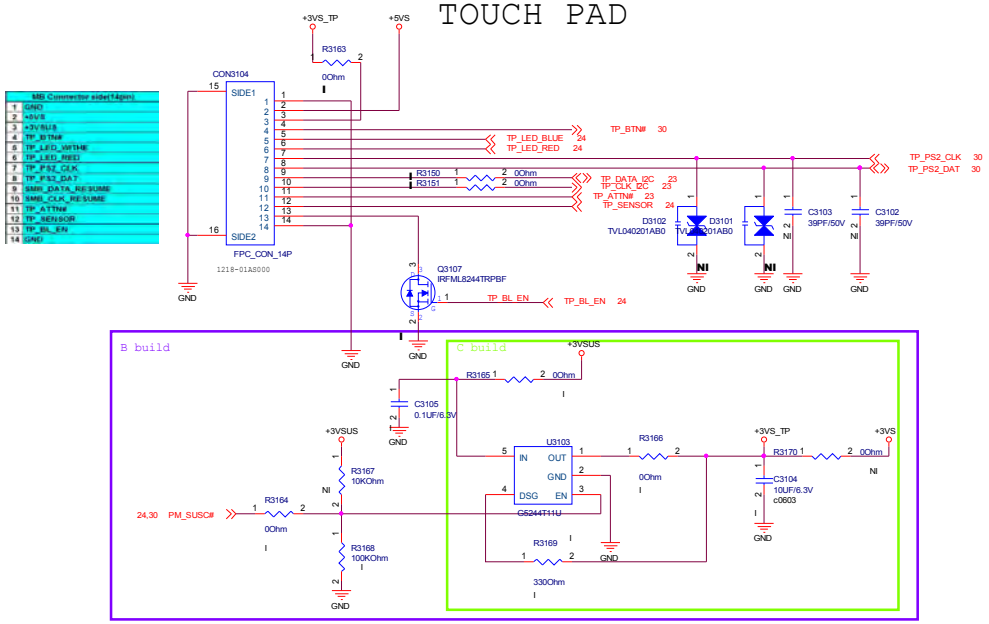
RTC



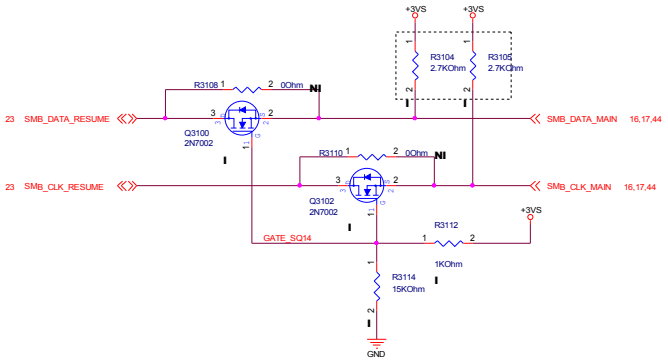
PEGATRON	Title : RTC	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 28 of 108	


U3001
IT8587E/FX
G-SENSOR ; THERMAL SENSOR
KEYBOAED BACKLIGHT
GPU
CHARGER ; BATTERY
B build
C build
PEGATRON
Title : EC_ITE8587
Engineer: Leon_Lu
Pegatron Corp.
Project Name
P5NCN/P7NCN MAIN BOARD
Size
A2
Rev
A1.0
Date: Monday, September 07, 2015
Sheet 30 of 108

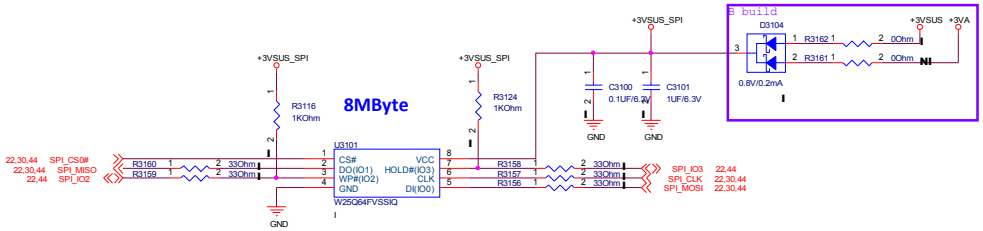
TOUCH PAD



Avoid leakage in S5

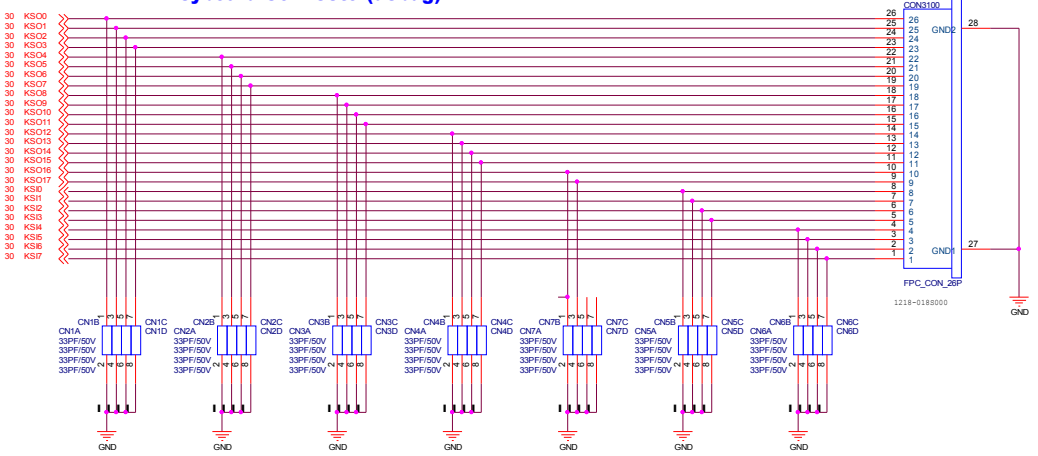


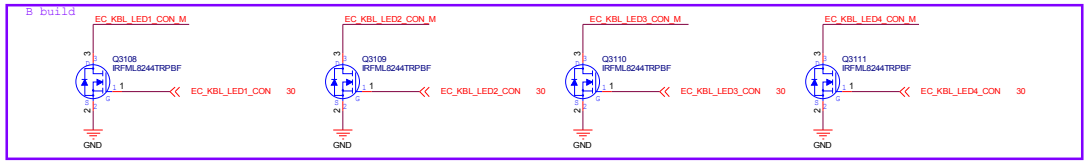
SPI ROM (Quad I/O Supported)



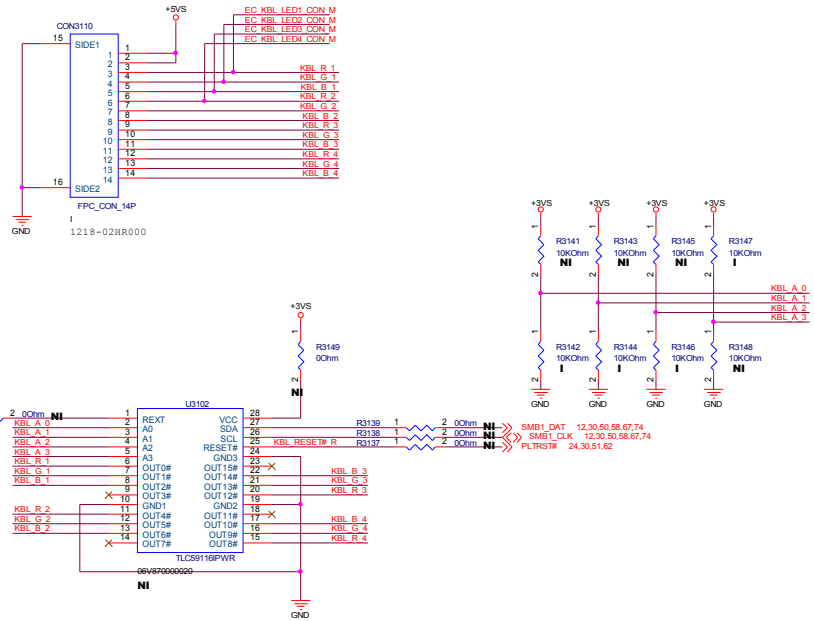
NOTE:
Making use of WP* and HOLD* for Quad I/O support

Keyboard Connector(debug)

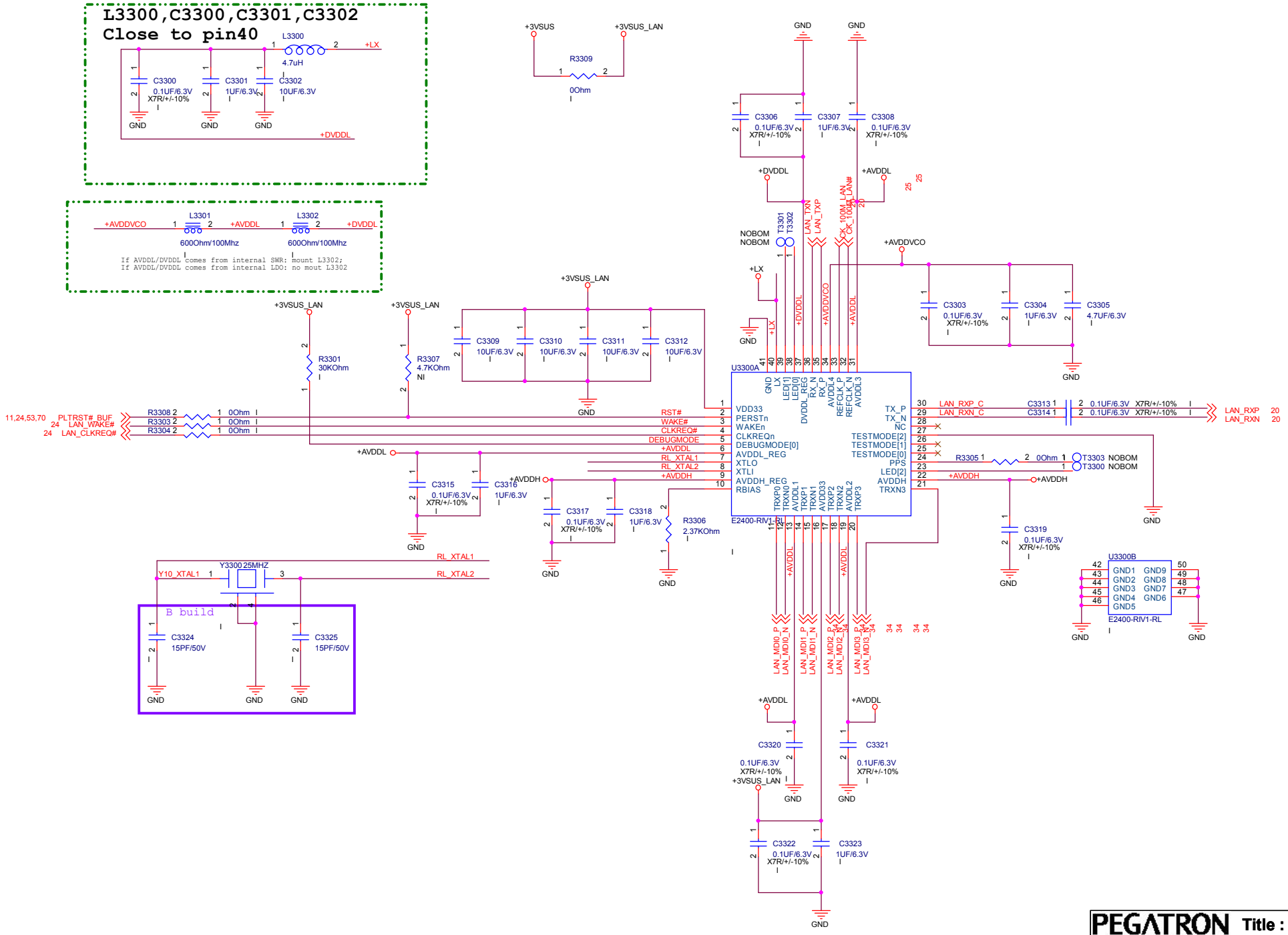




KB(Backlight)

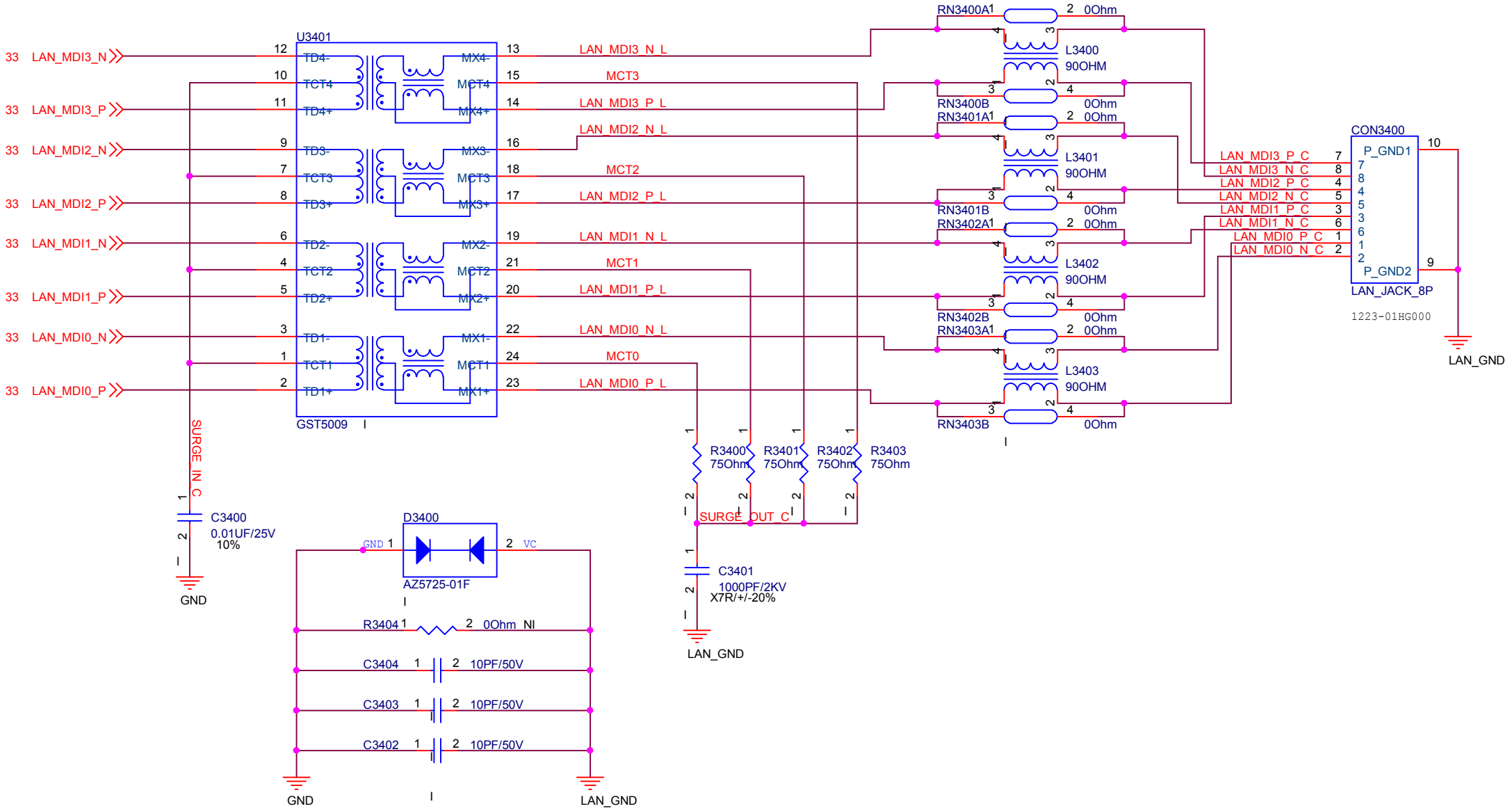


PEGATRON	Title : KB/TP/SPI		
Pegatron Corp.	Engineer: Leon_Lu		
Size: A2	Project Name: P5NCN/P7NCN MAIN BOARD		Rev: A1.0
Date: Monday, September 07, 2015	Sheet 31 of 108		



PEGATRON	Title : LAN_E2400	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A3	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 33 of 108	

SURGE

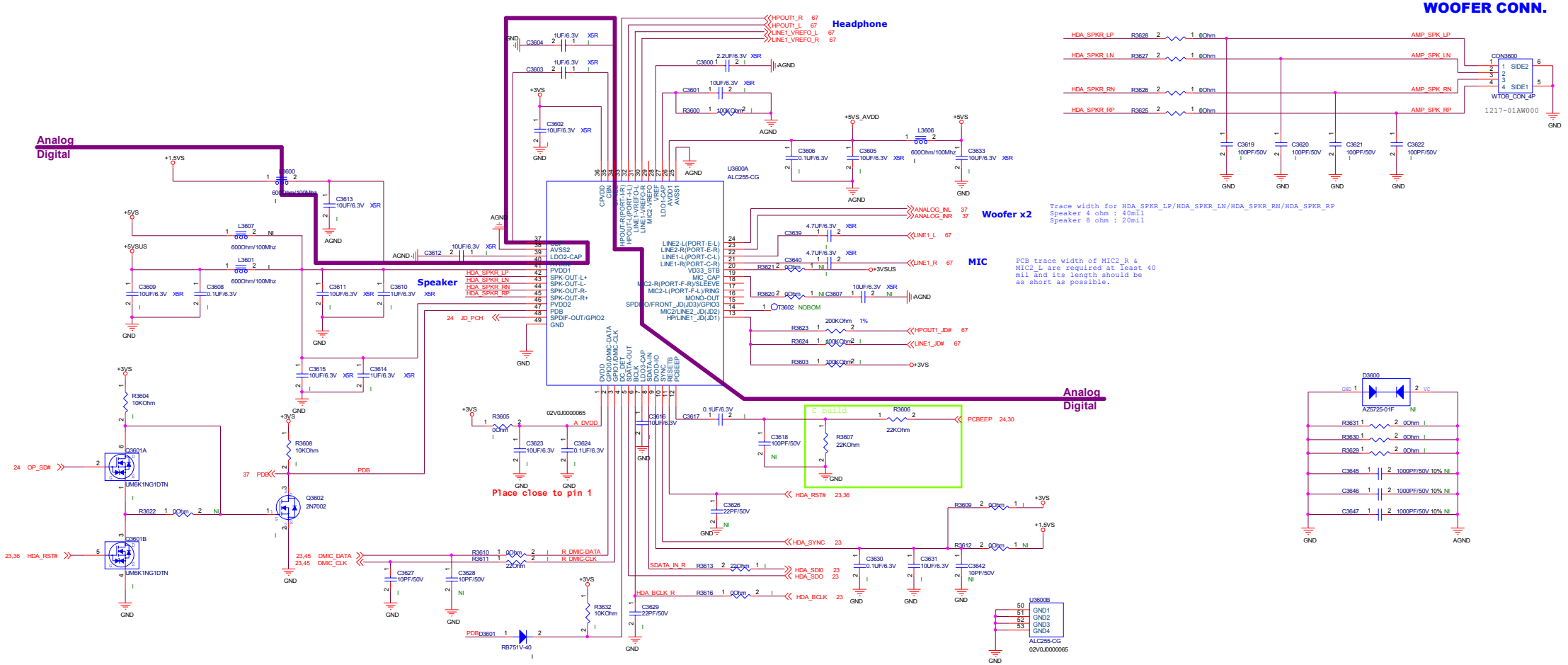


PEGATRON DT-MB RESTRICTED SECRET

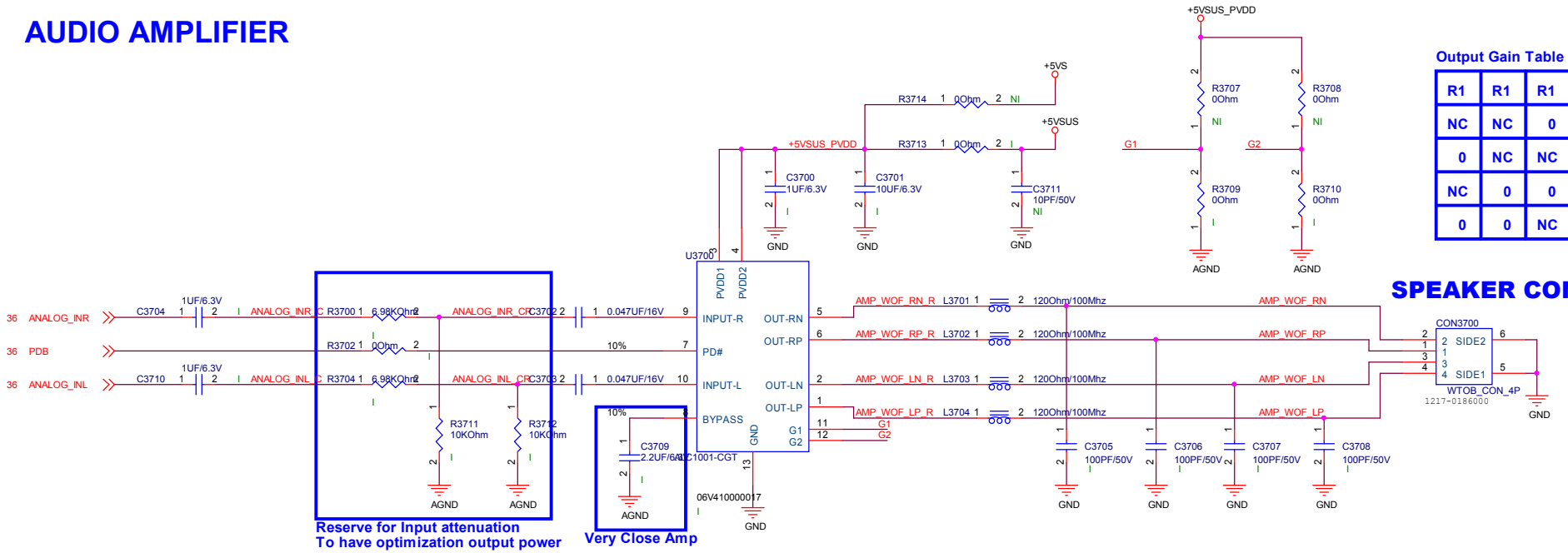
<Variant Name>

PEGATRON	Title : RJ45 CONN.	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 34 of 108	

ALC255 CODEC



AUDIO AMPLIFIER



Reserve for Input attenuation
To have optimization output power

Very Close Amp

SPEAKER CONN.

Output Gain Table

R1	R1	R1	R1	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

<Variant Name>

PEGATRON Title : SPEAKER & SIDE MIC1

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

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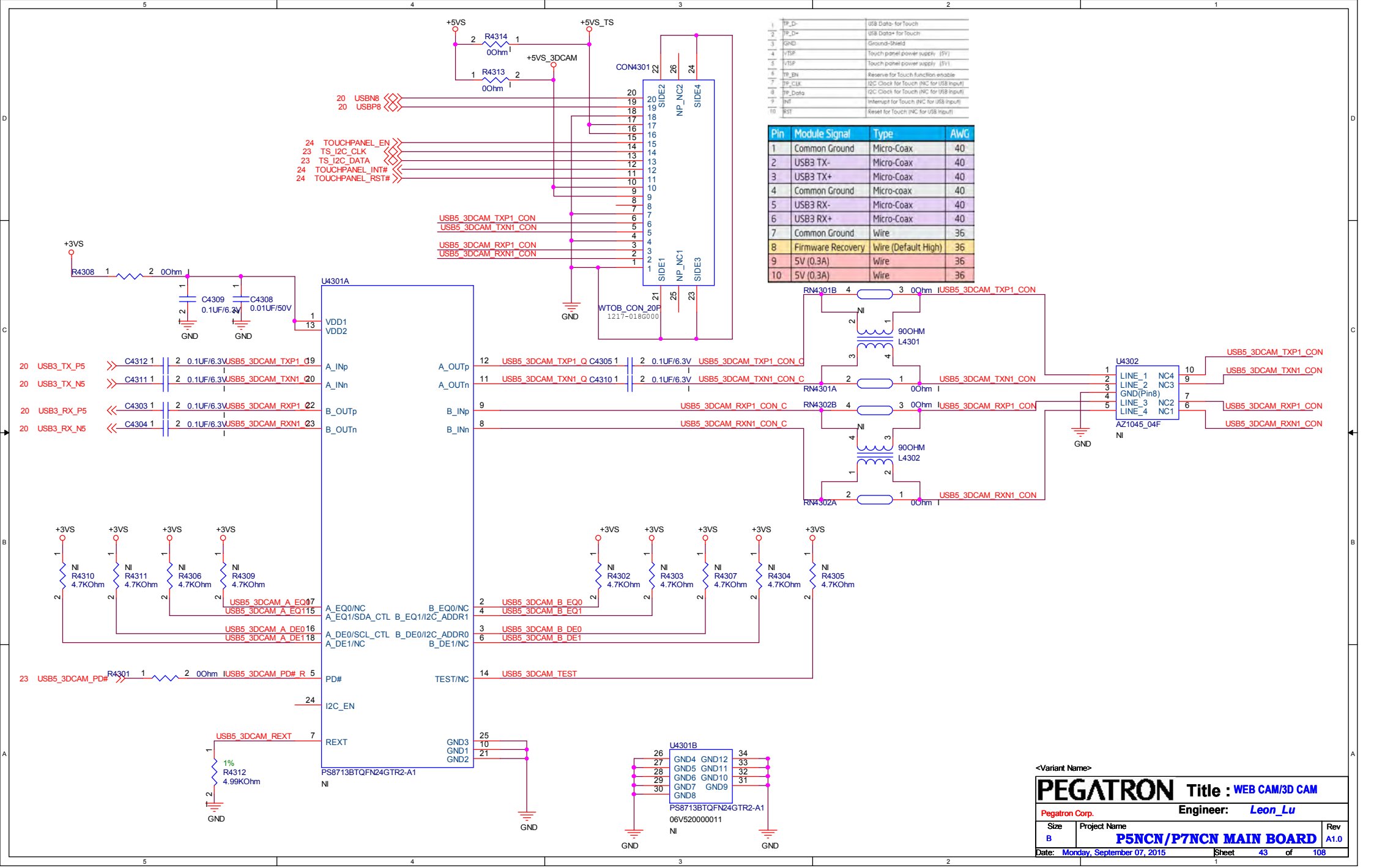


Pin	Module Signal	Type	AWG
1	Common Ground	Micro-Coax	40
2	USB3 TX-	Micro-Coax	40
3	USB3 TX+	Micro-Coax	40
4	Common Ground	Micro-coax	40
5	USB3 RX-	Micro-Coax	40
6	USB3 RX+	Micro-Coax	40
7	Common Ground	Wire	36
8	Firmware Recovery	Wire (Default High)	36
9	5V (0.3A)	Wire	36
10	5V (0.3A)	Wire	36

1	TP_D-	USB Data- for Touch
2	TP_D+	USB Data+ for Touch
3	GND	Ground-Shield
4	VTSP	Touch panel power supply (5V)
5	VTSP	Touch panel power supply (5V)
6	TP_EN	Reserve for Touch function enable
7	TP_CLK	I2C Clock for Touch (NC for USB input)
8	TP_Data	I2C Clock for Touch (NC for USB input)
9	INT	Interrupt for Touch (NC for USB input)
10	RST	Reset for Touch (NC for USB input)

<Variant Name>

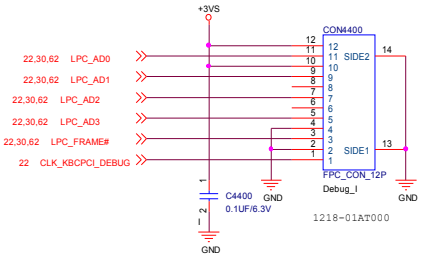
PEGATRON Title : WEB CAM/3D CAM

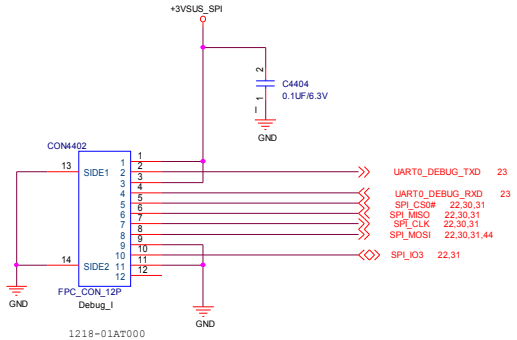
Pegatron Corp. Engineer: Leon_Lu

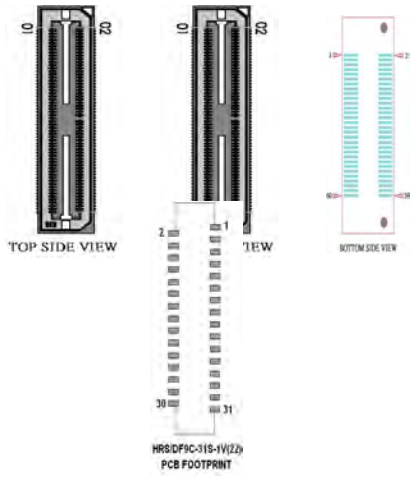
Size	Project Name	Rev
B	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 43 of 108

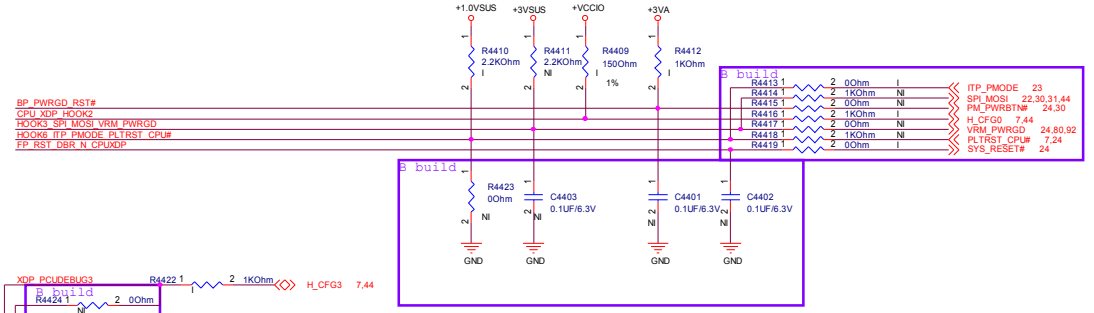
LPC DEBUG SMD

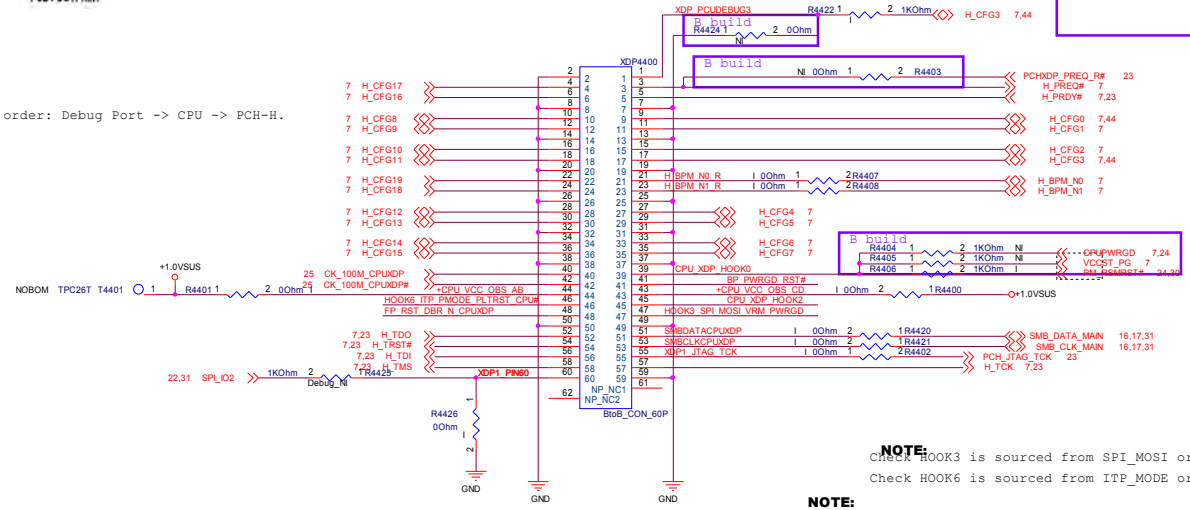






INTEL CPU XDP DEBUG PORT





NOTE: PREQ# and PRDY#
MUST be routed in this order: Debug Port -> CPU -> PCH-H.

NOTE:
CHECK HOOK3 is sourced from SPI_MOSI or VRM_PWRGD?
Check HOOK6 is sourced from ITP_MODE or PLTRST_CPU#?

NOTE:
XDP_PRESENT#(PIN 60) to enable +1V_ST for Sx debug purpose

NOTE:
Place SPI_IO2 0 ohm near PCH

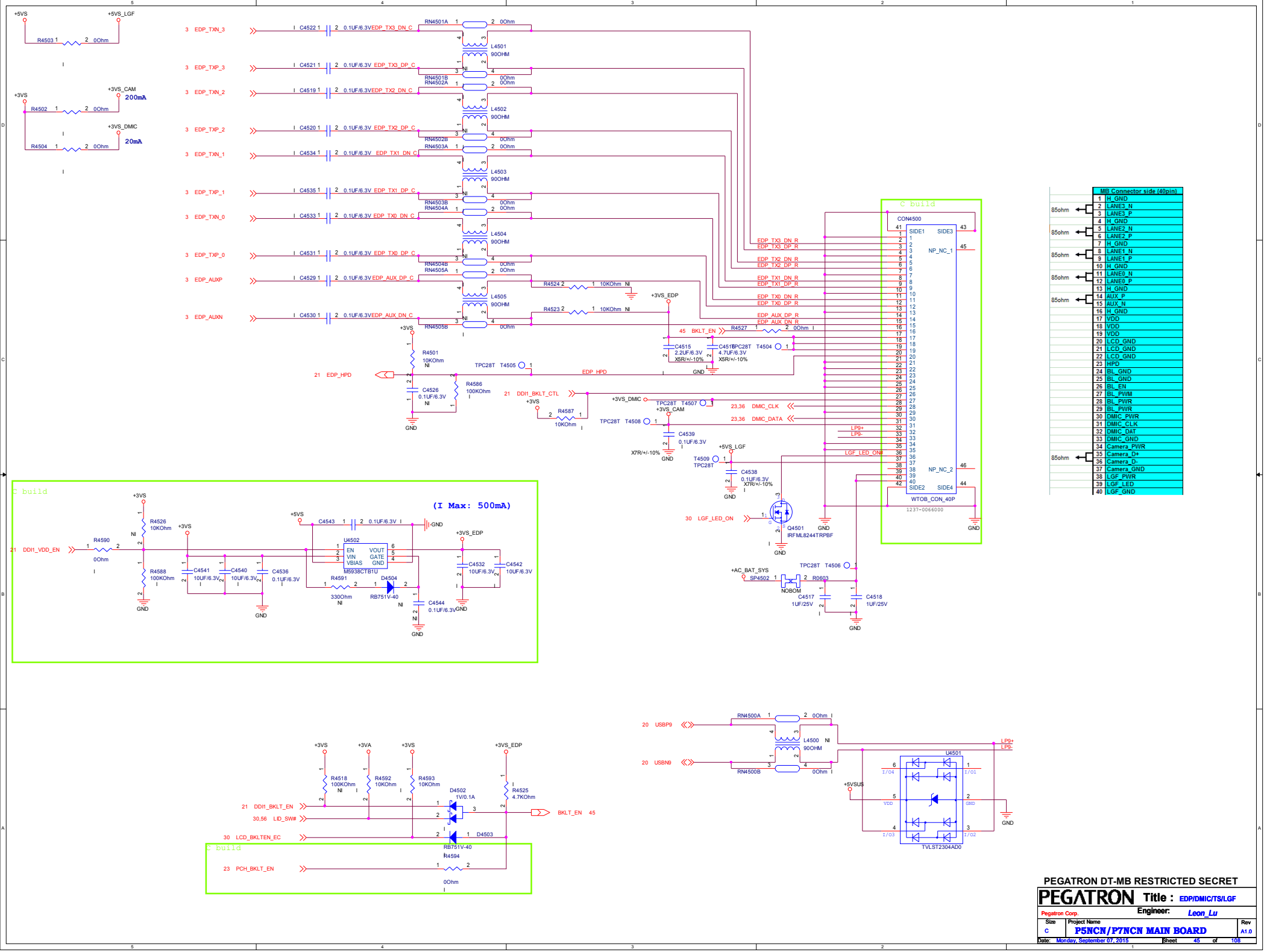
<Variant Name>

PEGATRON Title : DEBUG CON

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
C	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Thursday, September 10, 2015 Sheet 44 of 108



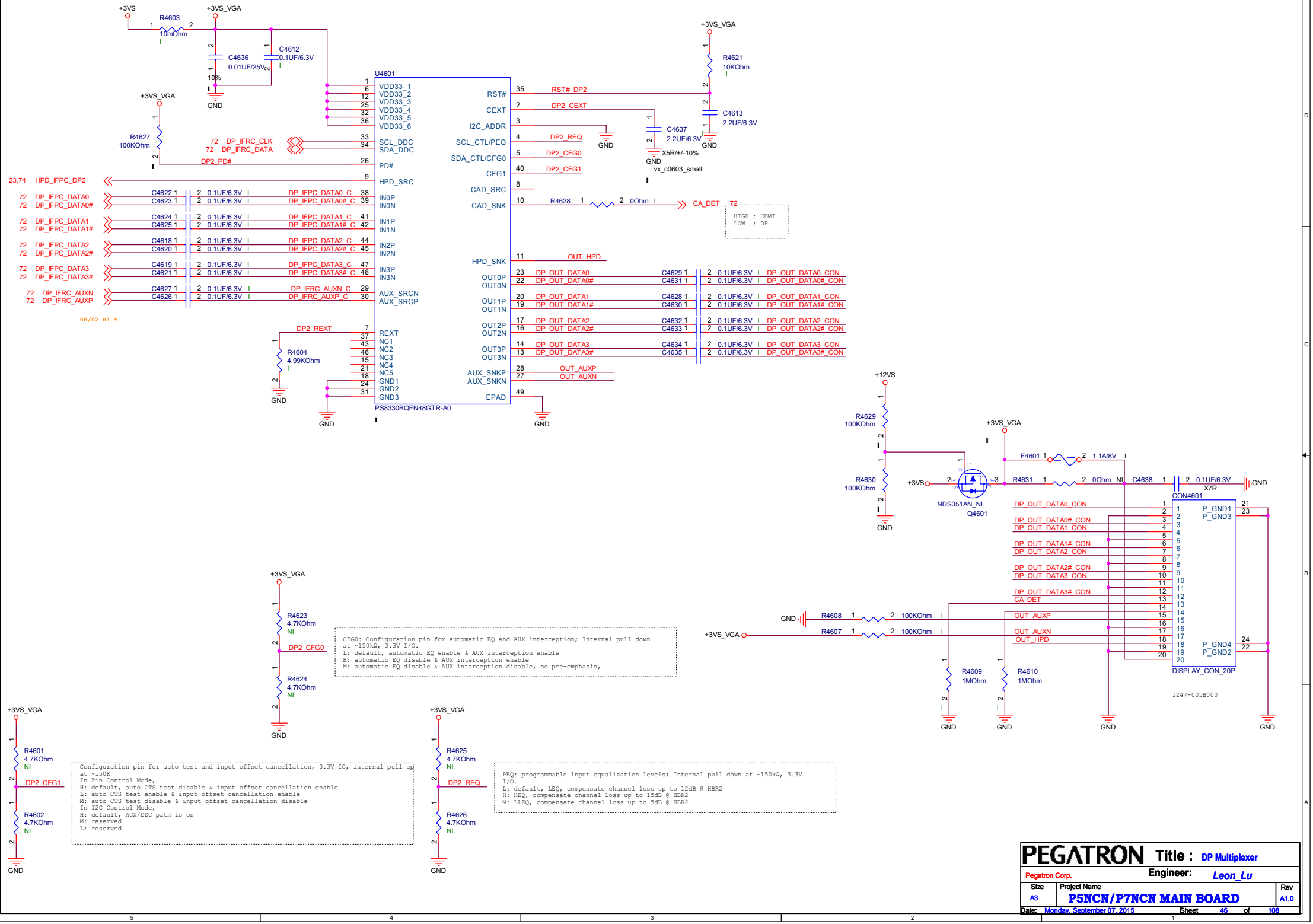
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : EDP/DMIC/TS/LGF

Pegatron Corp. Engineer: Leon_Lu

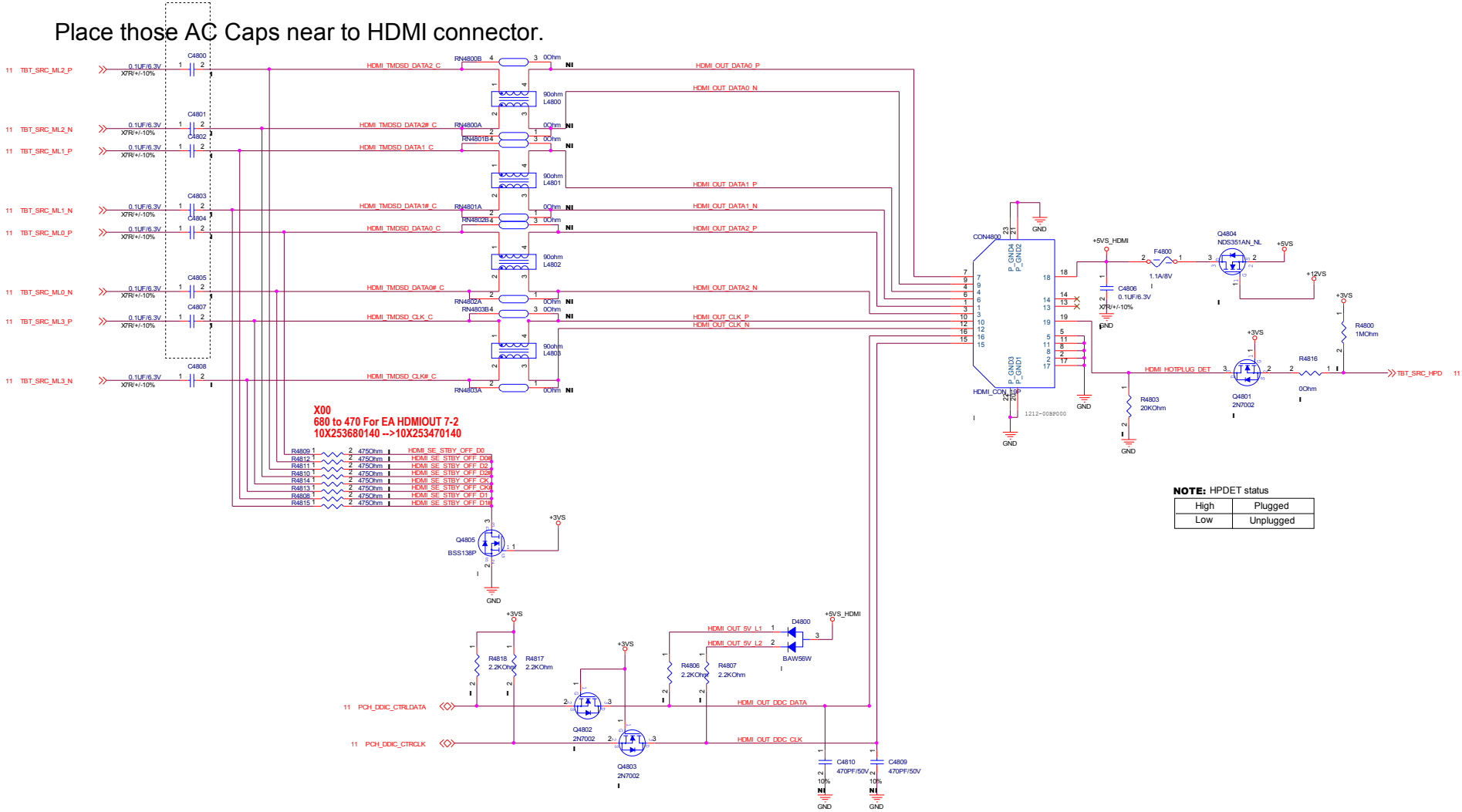
Size	Project Name	Rev
C	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 45 of 108



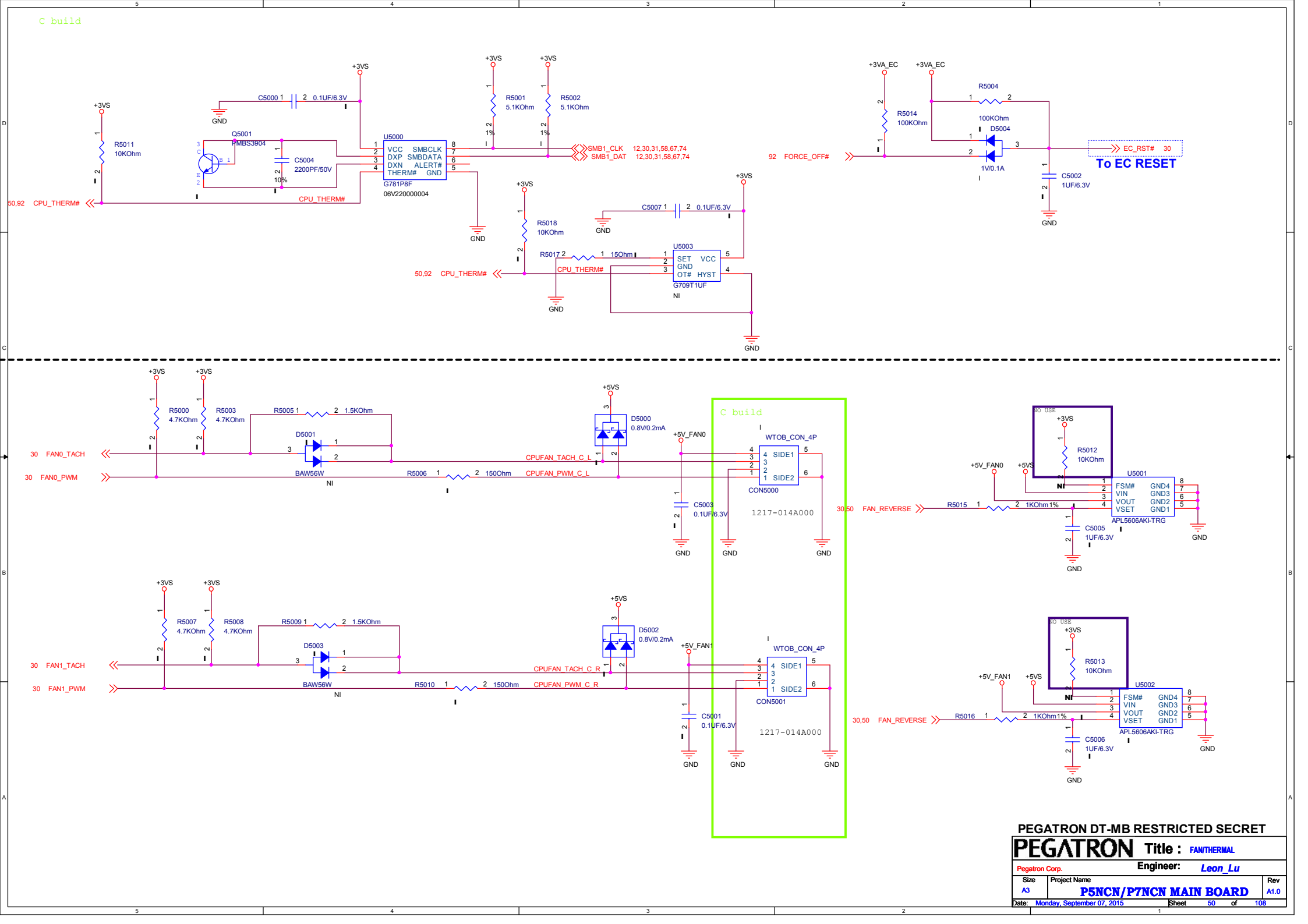
PEGATRON	Title : DP Multiplexer	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A3	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 46 of 108	

Place those AC Caps near to HDMI connector.



NOTE: HPDET status

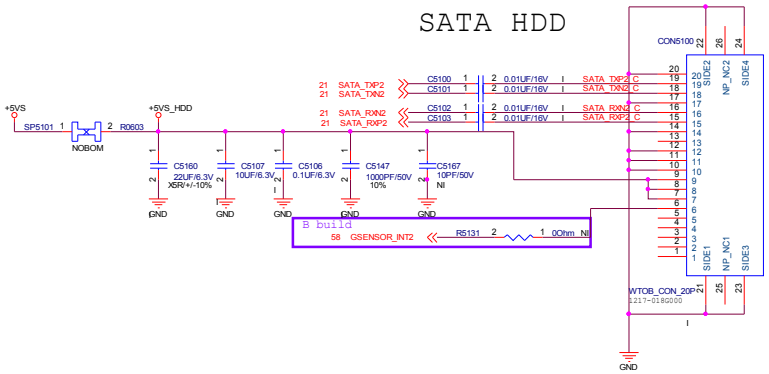
High	Plugged
Low	Unplugged



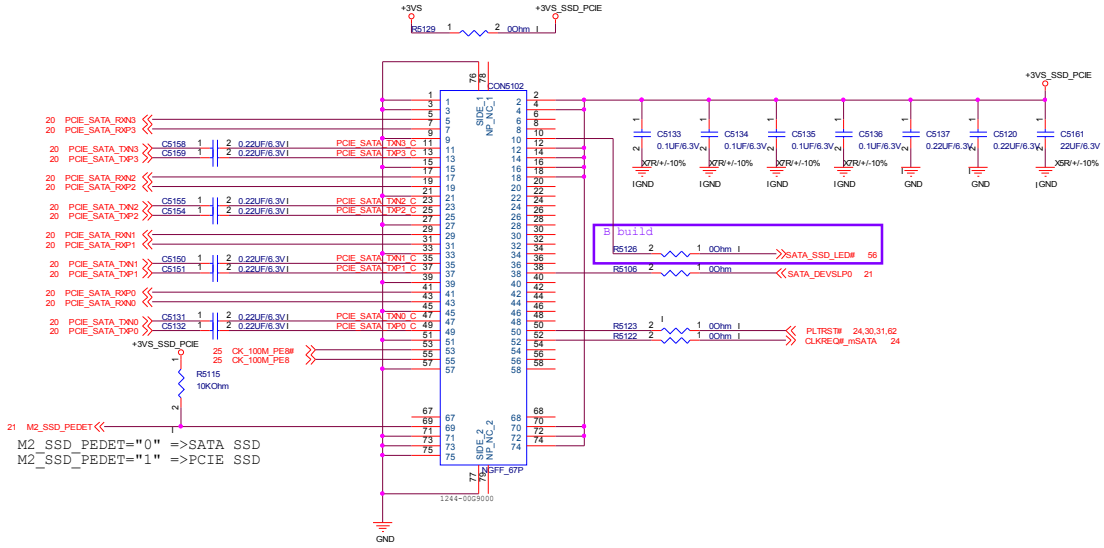
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : FAN/THERMAL	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A3	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 50 of 108	

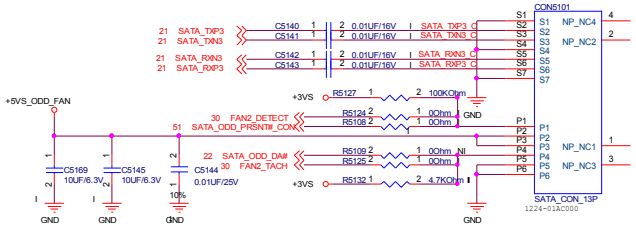
SATA HDD

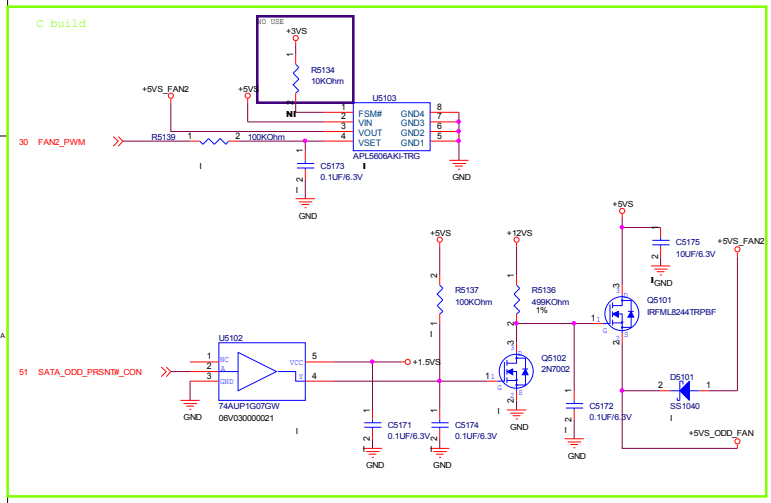


PCIE & SATA SSD

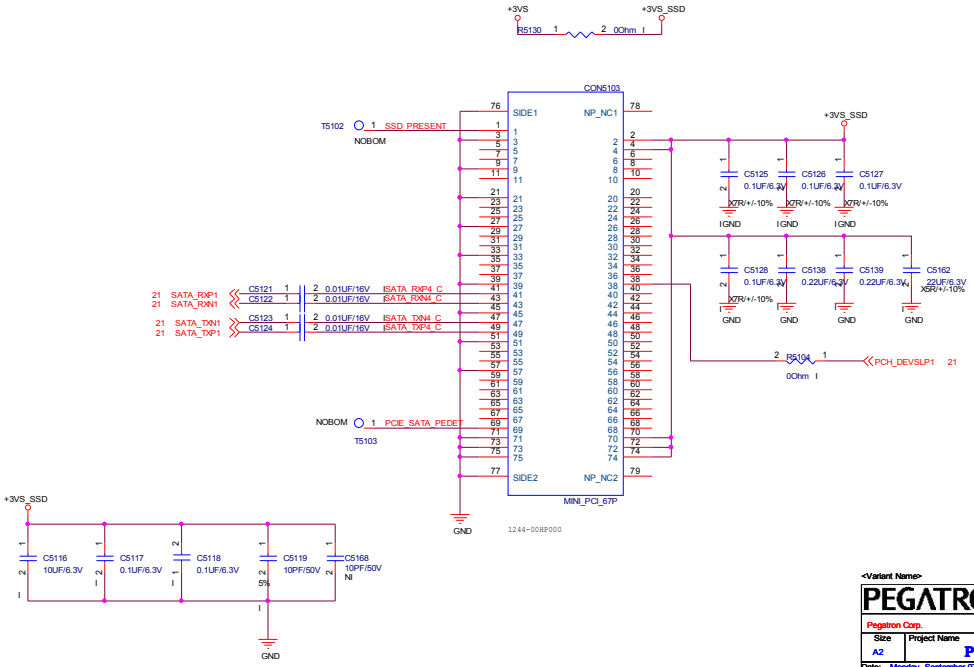


SATA ODD & 3'TH FAN





SATA SSD



<Variant Name>

PEGATRON Title : SATA/ODD/SSD

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	1.0

Date: Monday, September 07, 2015 Sheet 51 of 108

STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: -0.3 to 7v.
STATUS#, FAULT# Continuous output sink current:25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.

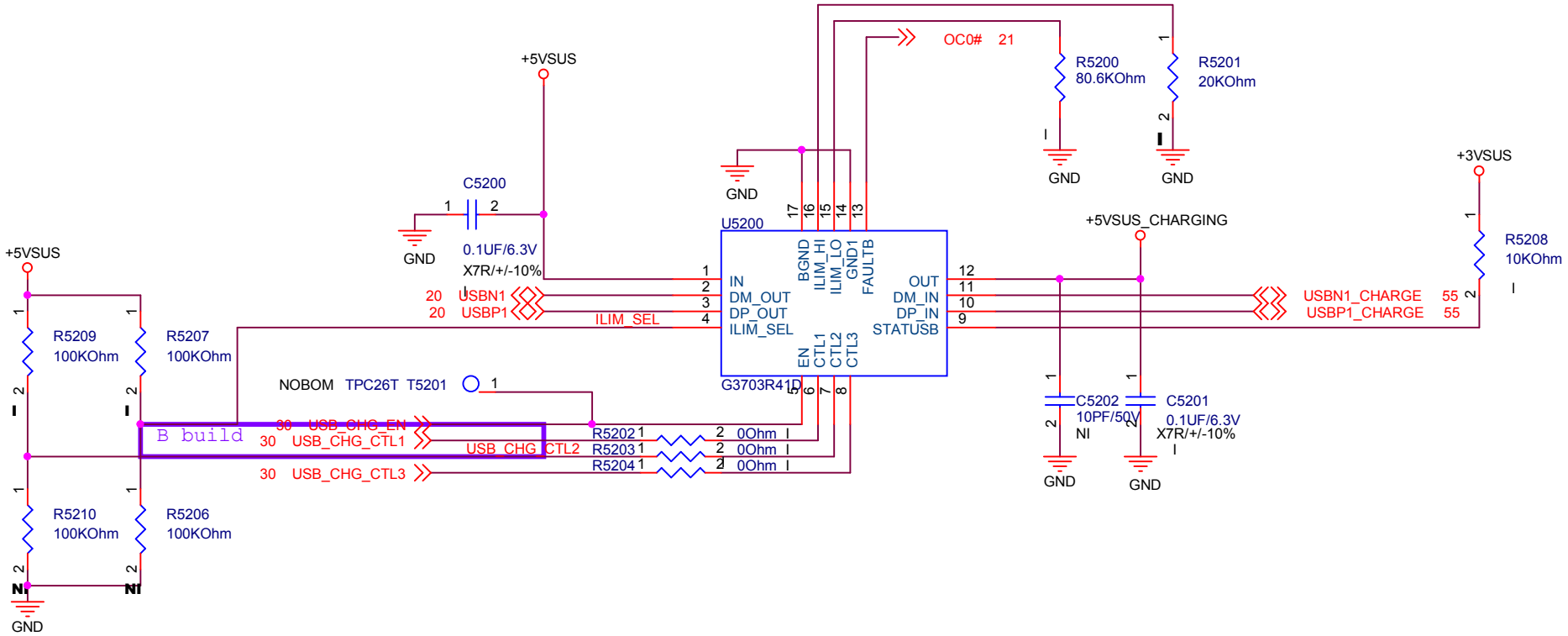


Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_ SEL	MODE	Current Limit Setting	Status Output	Notice
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A4	P5NCN/P7NCN MAIN BOARD	A1.0

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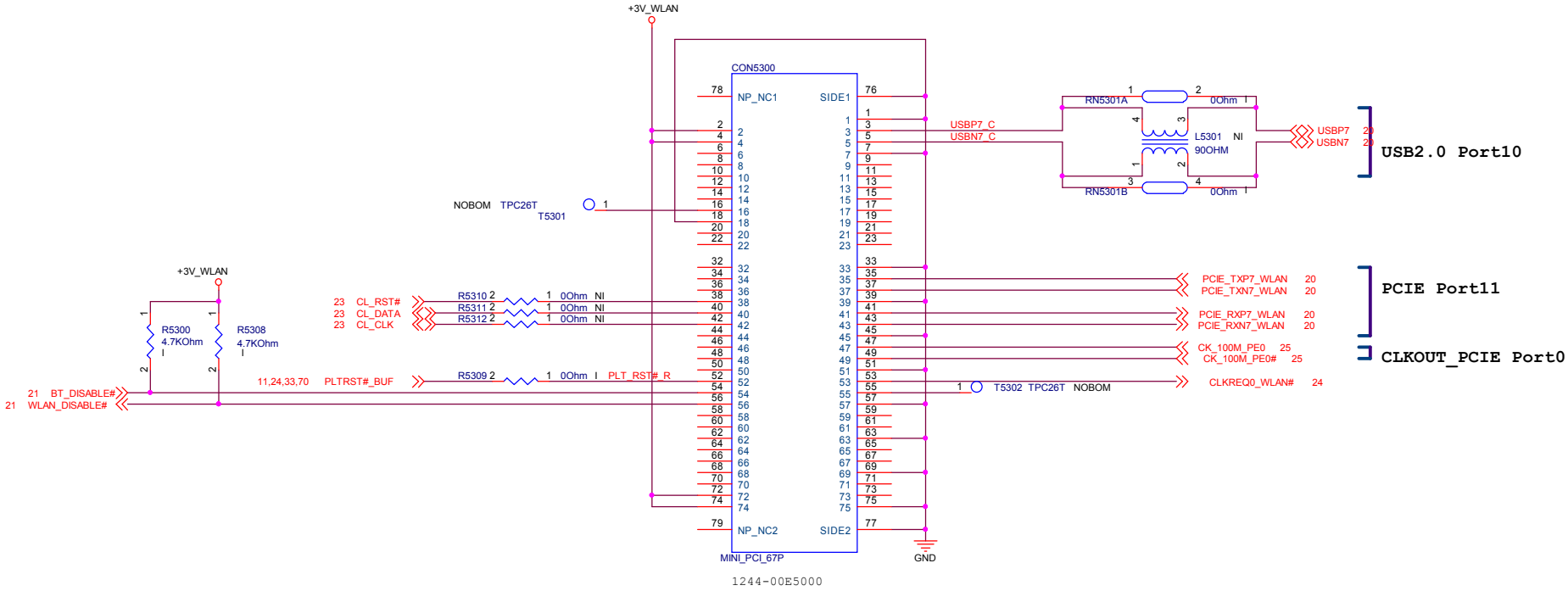
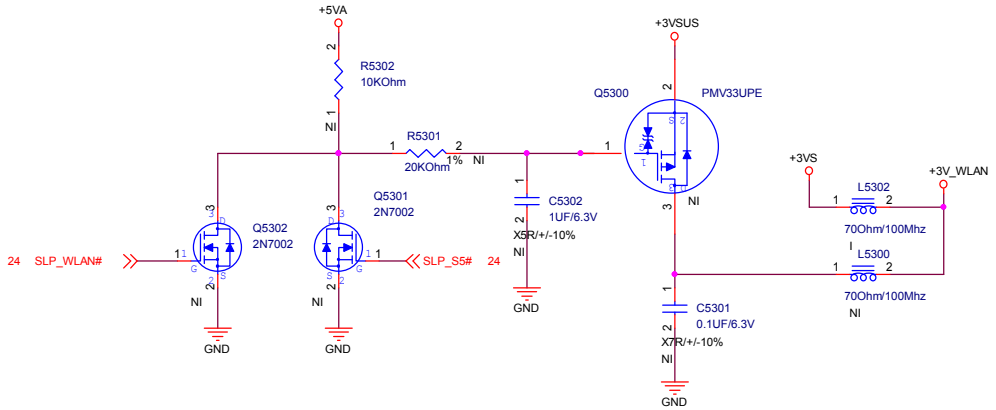
WLAN

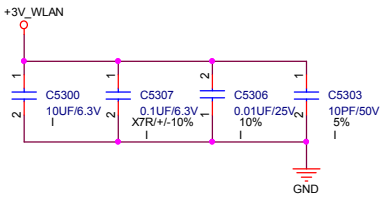


1244-00E5000

+3P3V_MINI1
Imax=2A /TDC=1.4A

Vdroop: 1.4A*65mohm=91mV >3.3*0.95





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : NGFF_WLAN

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

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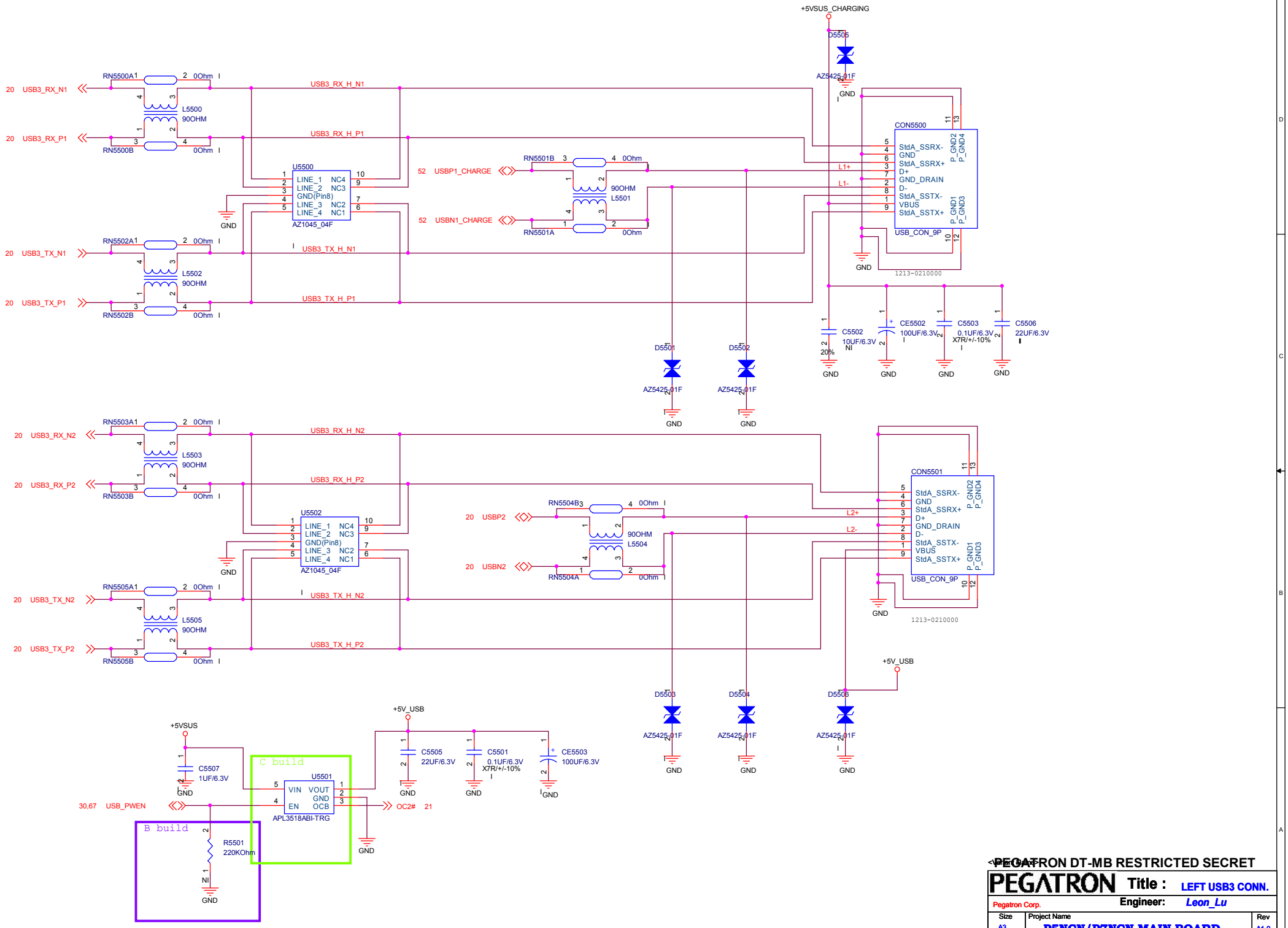
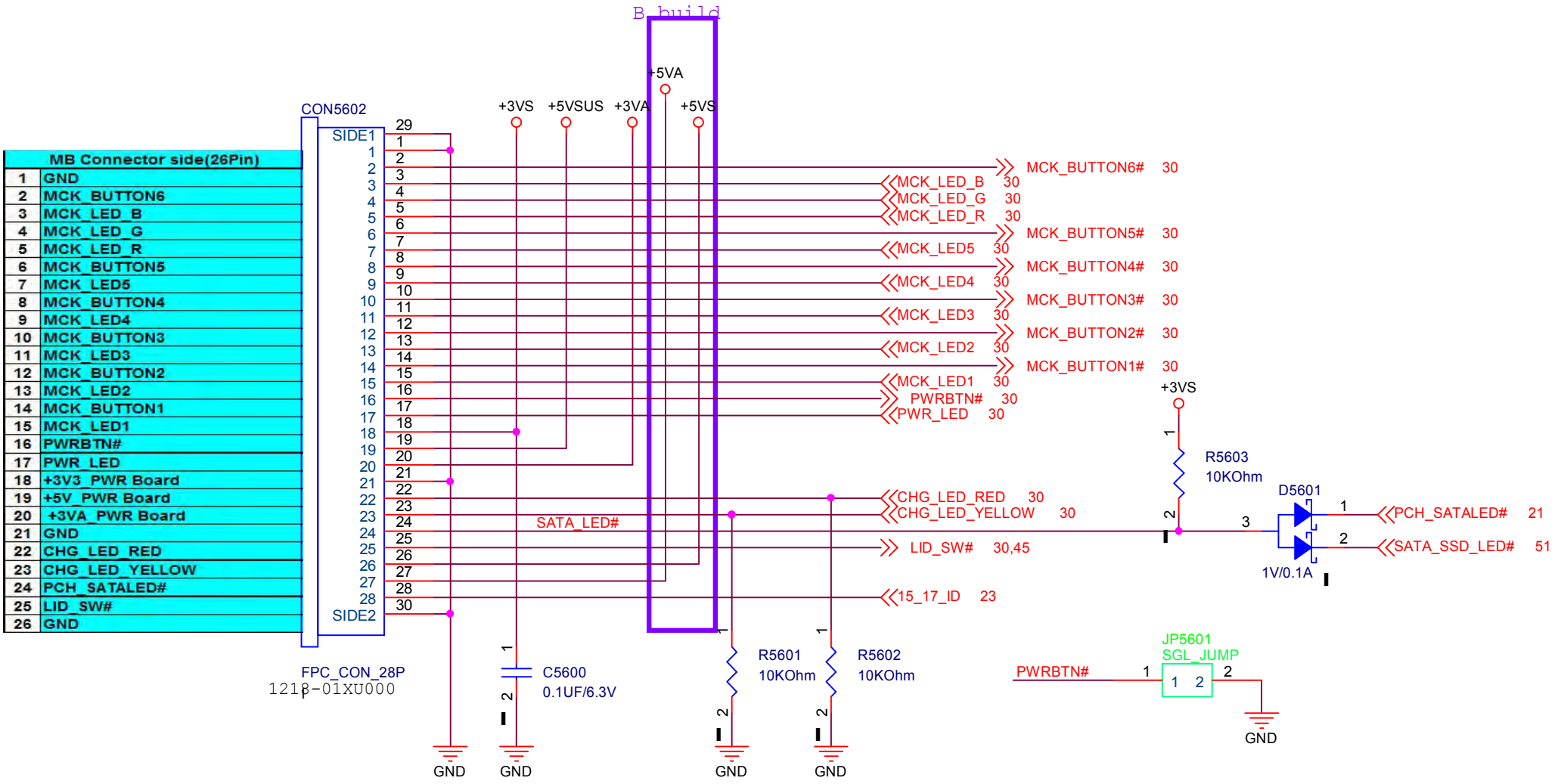


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	LEFT USB3 CONN.
Pegatron Corp.	Engineer:	Leon_Lu
Size: A3	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 55 of 108	



<Variant Name>

PEGATRON

Title : PWR BOARD CON

Pegatron Corp.

Engineer: Leon_Lu

Size	Project Name	Rev
A	P5NCN/P7NCN MAIN BOARD	A1.0

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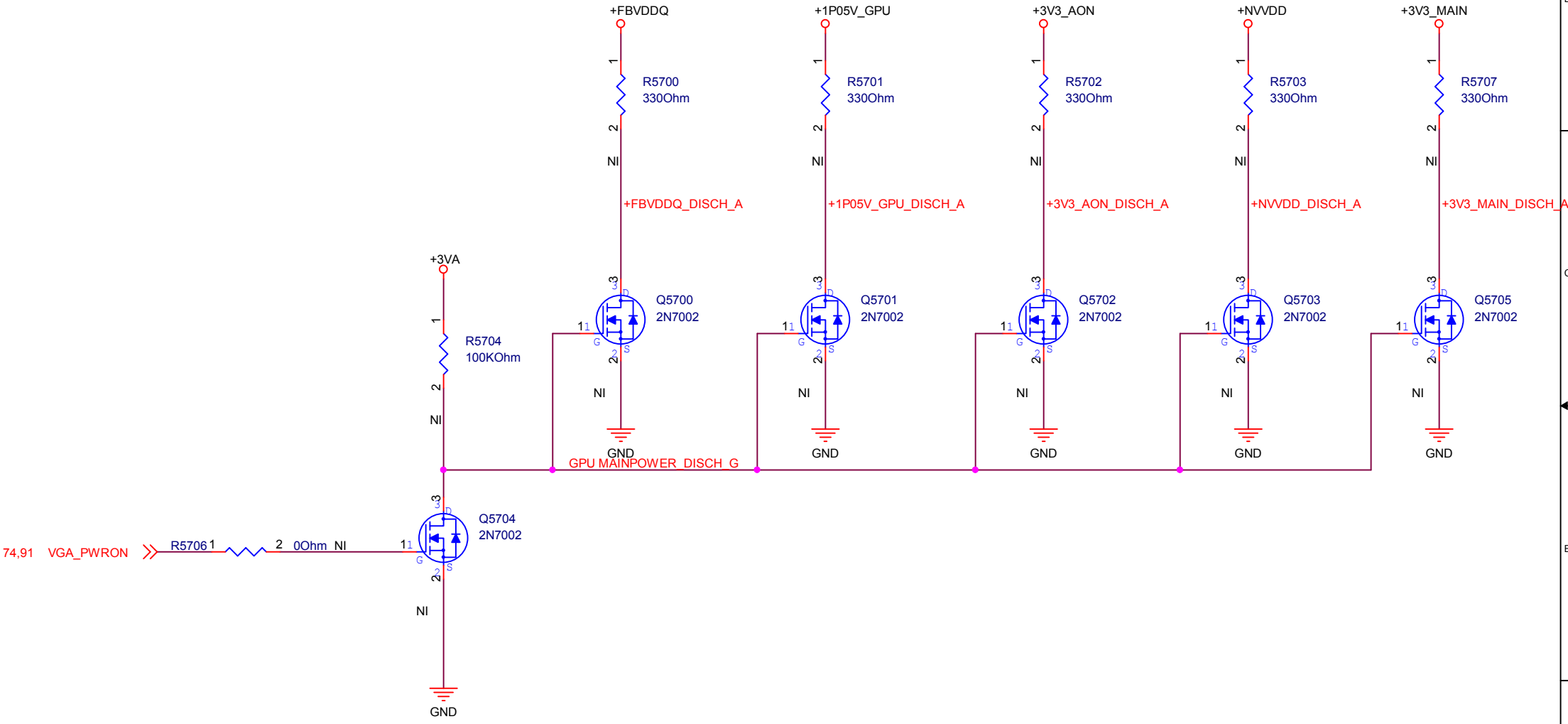
NV GPU POWER DISCHARGE

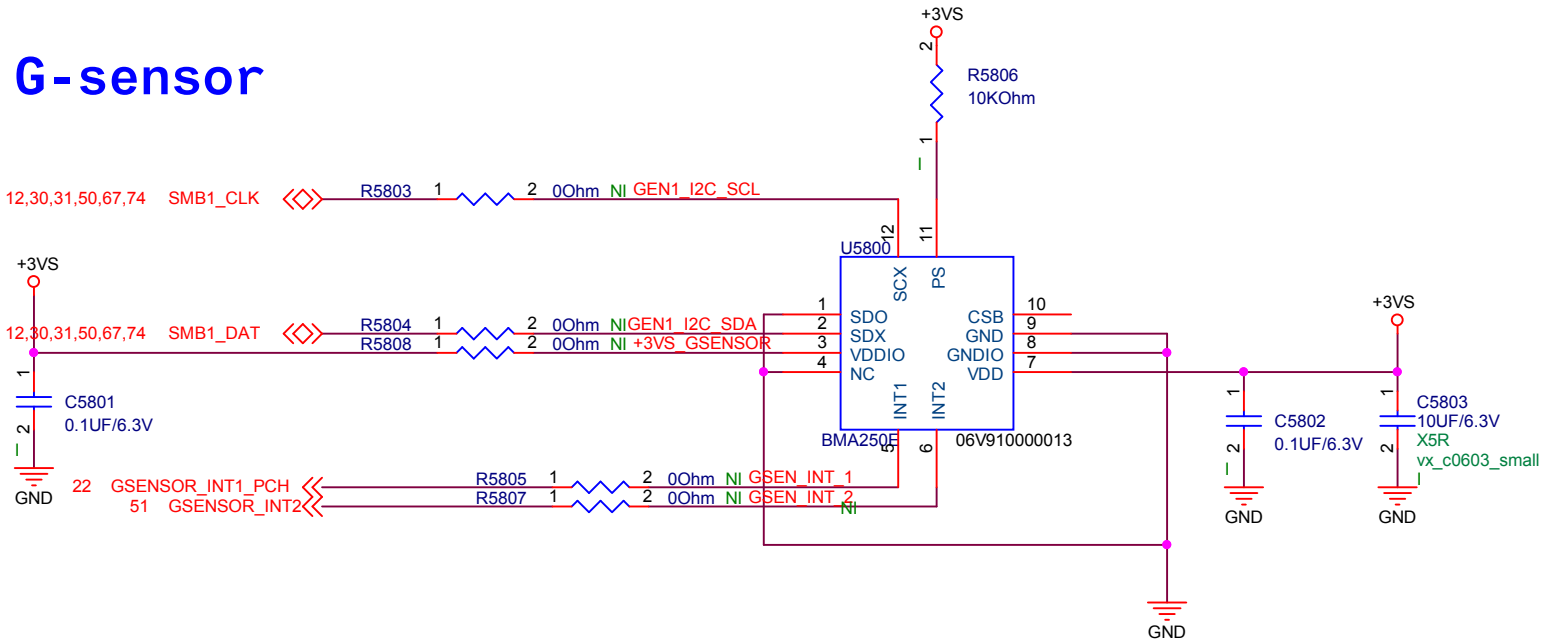


PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>

PEGATRON	Title : GPU PWR discharge	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 57 of 108	

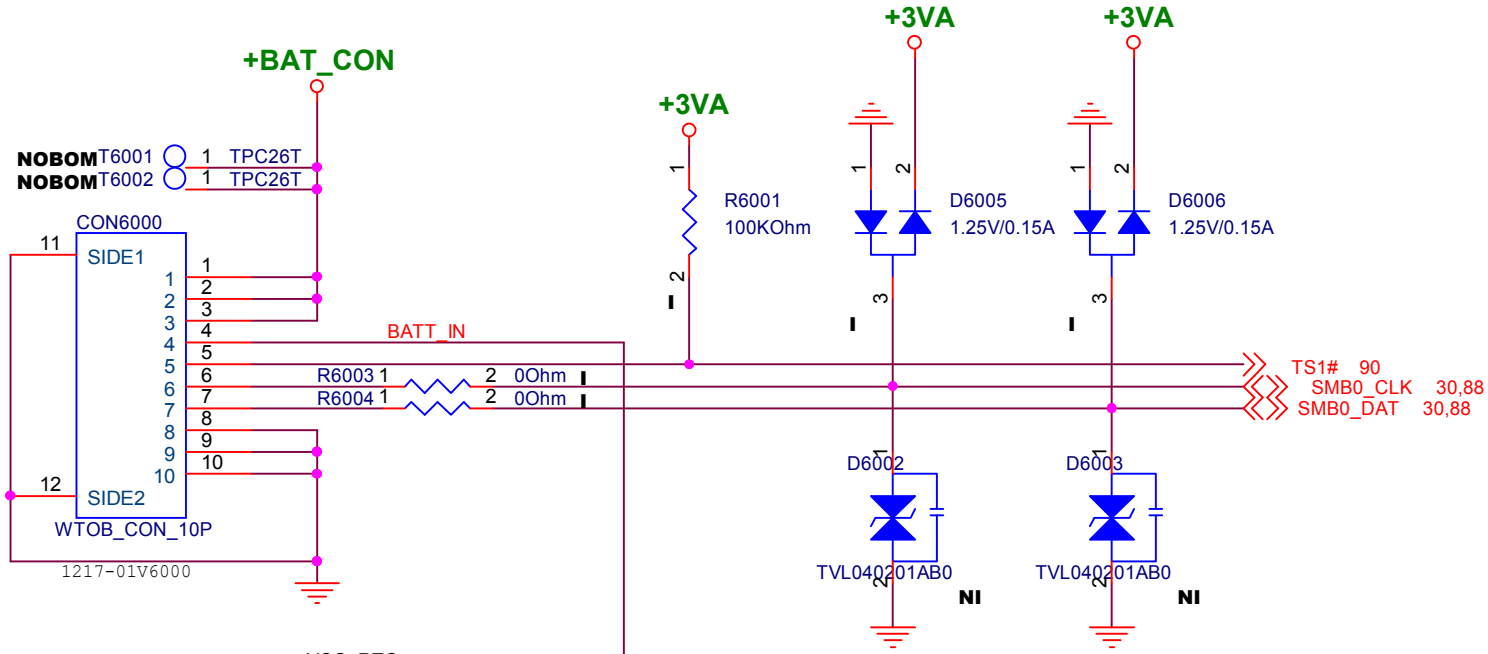
G-sensor

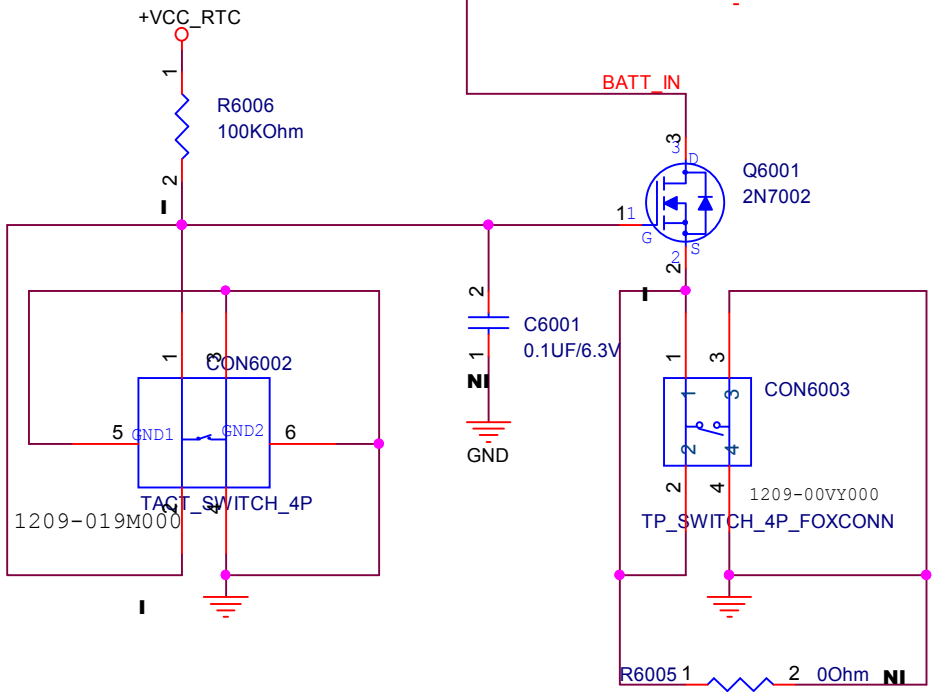


<Variant Name>

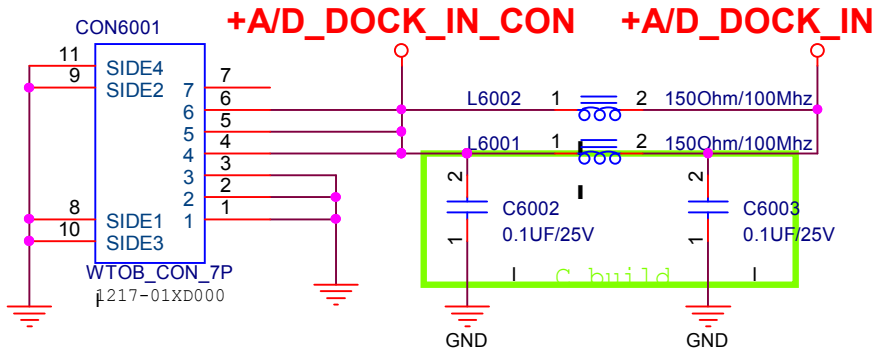
PEGATRON	Title : G-sensor	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 58 of 108	

BATTERY CONNECTOR

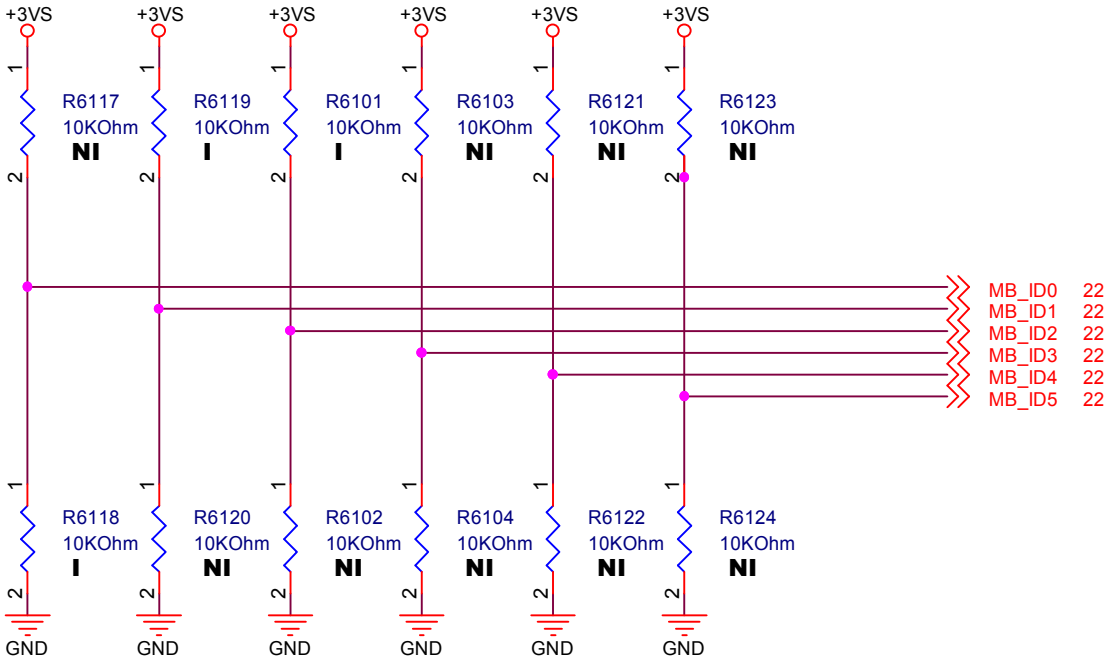


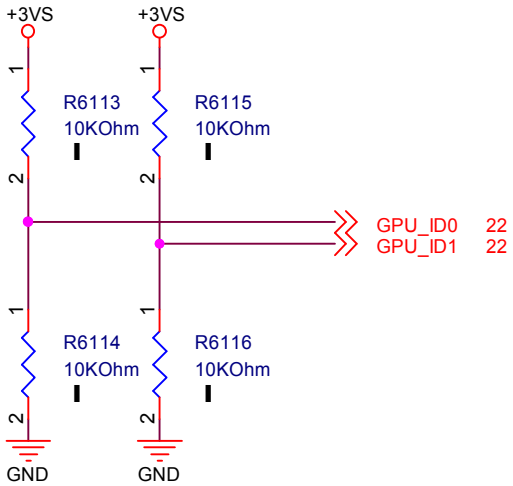


AC IN CONNECTOR



PEGATRON	Title : BATT CON/AC IN	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 60 of 108	





	ID2	ID1	ID0
1.0	0	0	0
1.1	0	0	1
1.2	0	0	1
1.3	0	1	0
1.4	0	1	1
1.5/1.6	1	0	0
1.5/1.6 C8	1	0	1
2	1	1	0

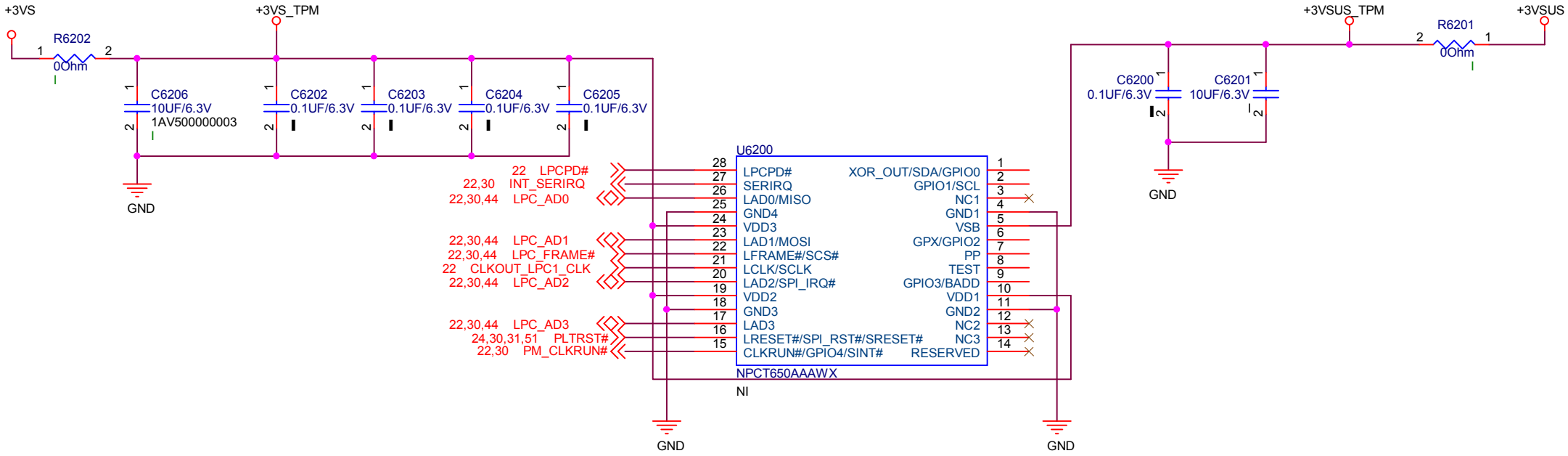
PEGATRON Title : BOARD ID

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A	P5NCN/P7NCN MAIN BOARD	A1.0

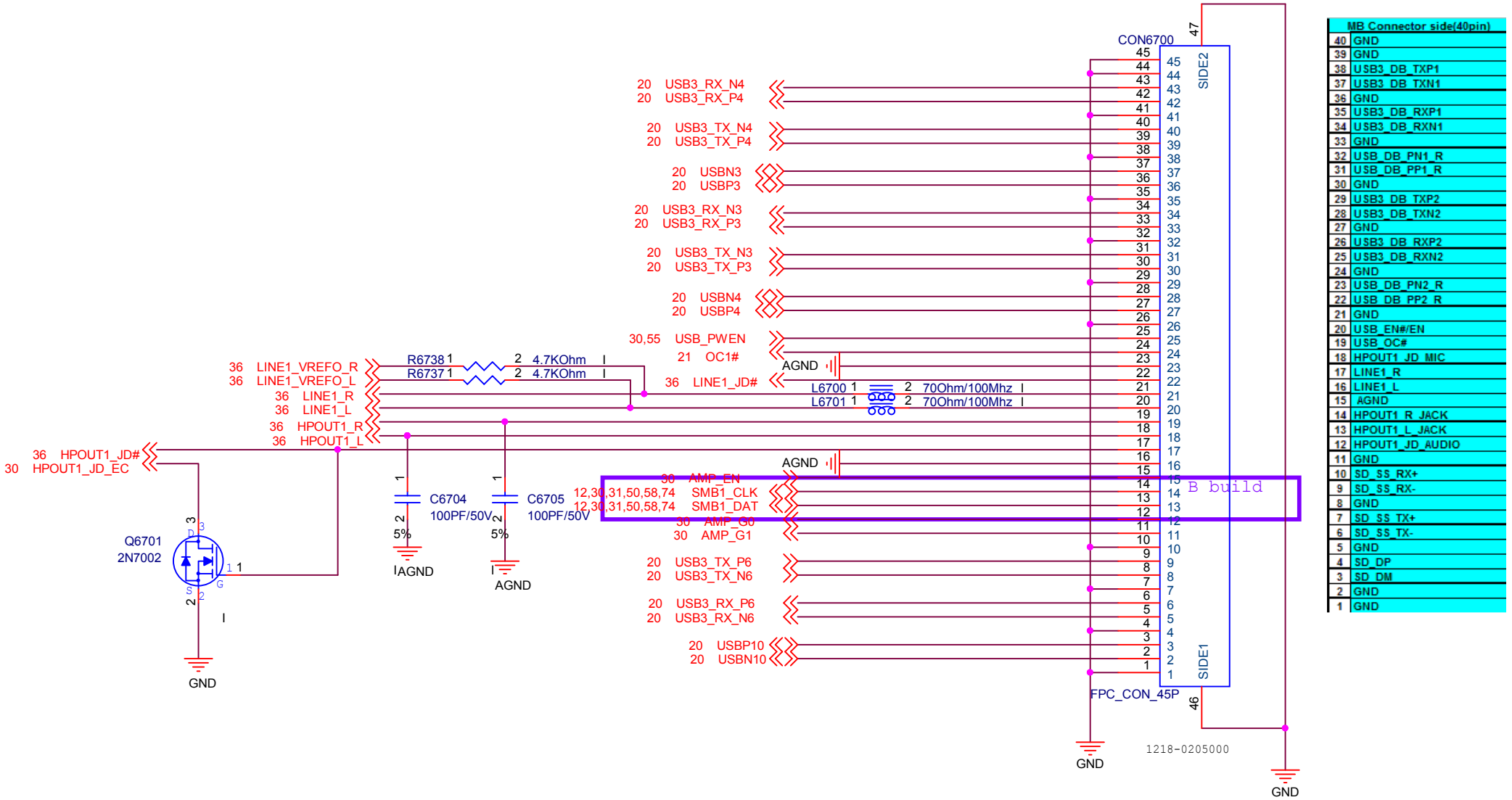
Date: Monday, September 07, 2015 Sheet 61 of 108

NPCT650

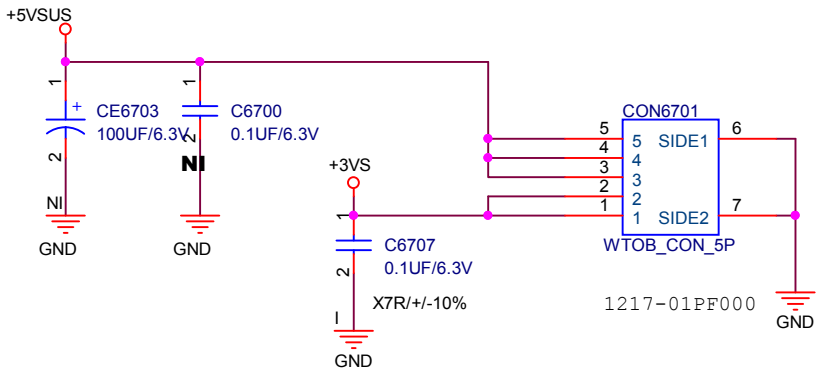


<Variant Name>

PEGATRON	Title : TPM	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 62 of 108	



MB Connector side(40pin)	
40	GND
39	GND
38	USB3_DB_TXP1
37	USB3_DB_TXN1
36	GND
35	USB3_DB_RXP1
34	USB3_DB_RXN1
33	GND
32	USB_DB_PN1_R
31	USB_DB_PP1_R
30	GND
29	USB3_DB_TXP2
28	USB3_DB_TXN2
27	GND
26	USB3_DB_RXP2
25	USB3_DB_RXN2
24	GND
23	USB_DB_PN2_R
22	USB_DB_PP2_R
21	GND
20	USB_EN#/EN
19	USB_OC#
18	HPOUT1_JD_MIC
17	LINE1_R
16	LINE1_L
15	AGND
14	HPOUT1_R_JACK
13	HPOUT1_L_JACK
12	HPOUT1_JD_AUDIO
11	GND
10	SD_SS_RX+
9	SD_SS_RX-
8	GND
7	SD_SS_TX+
6	SD_SS_TX-
5	GND
4	SD_DP
3	SD_DM
2	GND
1	GND



MB Connector side(5pin)	
1	+3VS_DB
2	+3VS_DB
3	+5V_POWER
4	+5V_POWER
5	+5V_POWER

PEGATRON DT-MB RESTRICTED SECRET

Variant Name:

PEGATRON Title : IO BOARD CON

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A4	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 67 of 108

H31
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H33
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H34
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H36
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H54
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H53
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H56
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H11
RT419X335B335D118
GND

H21
RT335X350CBD118
GND

H32
RT335X315B315D118
GND

H35
RT335X315B315D118
GND

H51
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H52
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H55
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

CPU NUT

H61
CT256BD146

H64
CT256BD146

H66
CT256BD146

GND

GPU NUT

H60
CT256BD146

H63
CT256BD146

H65
CT256BD146

GND

U6901
SV-11A1M
GND

U6902
SV-11A1M
GND

H6901
O122X102DO122X102N
NOBOM

H6902
C102D102N
NOBOM

H6903
O122X102DO122X102N
NOBOM

PCH NUT

H68
CT256SB315D146
GND

H69
CT256BD146
GND

H62
CT256BD146
GND

<Variant Name>

~~PEGATRON RT MB RESTRICTED SECRET~~

PEGATRON Title : Screw hole

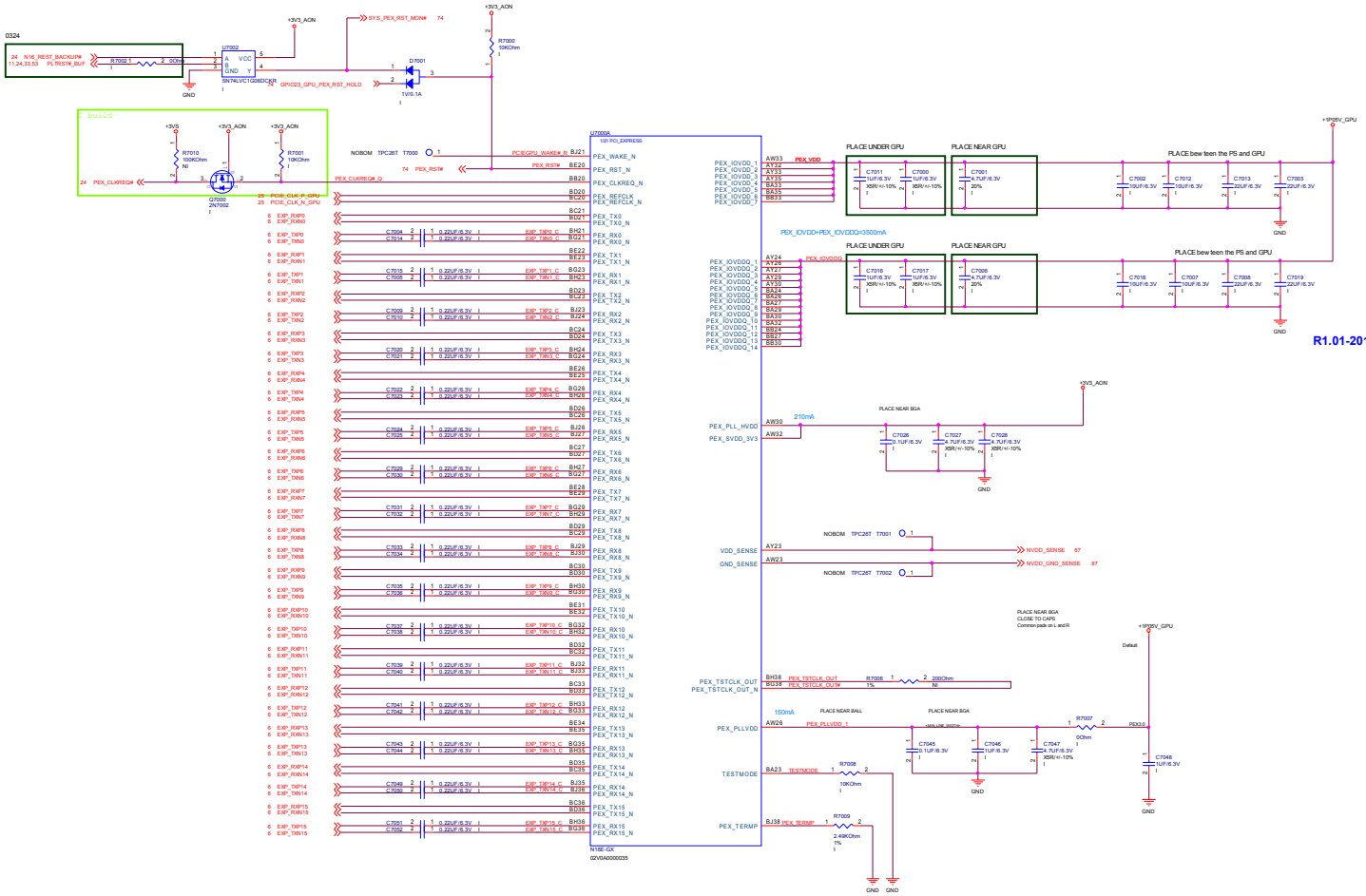
Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A4	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 69 of 108

PCI-Express Gen2 x 8 Interface

R1.01-2012/09/26:add C9972 220pf "NI" for GPU "PCIE_RST#"
R1.01-2012/09/28: For GPU PCIE_WAKE#,Add NR132 0ohm for switch.

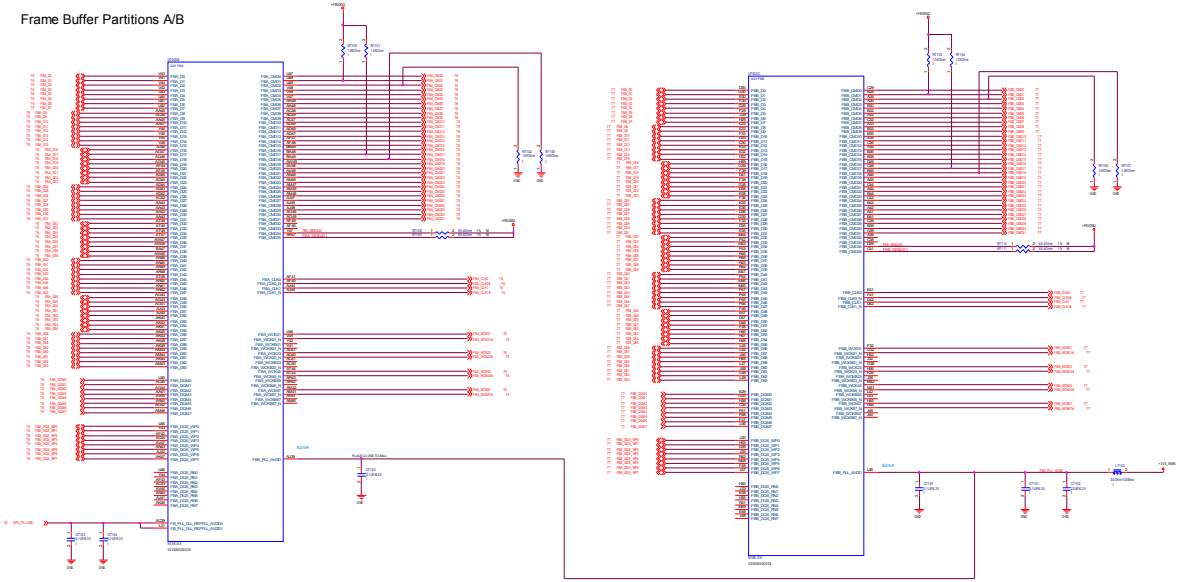


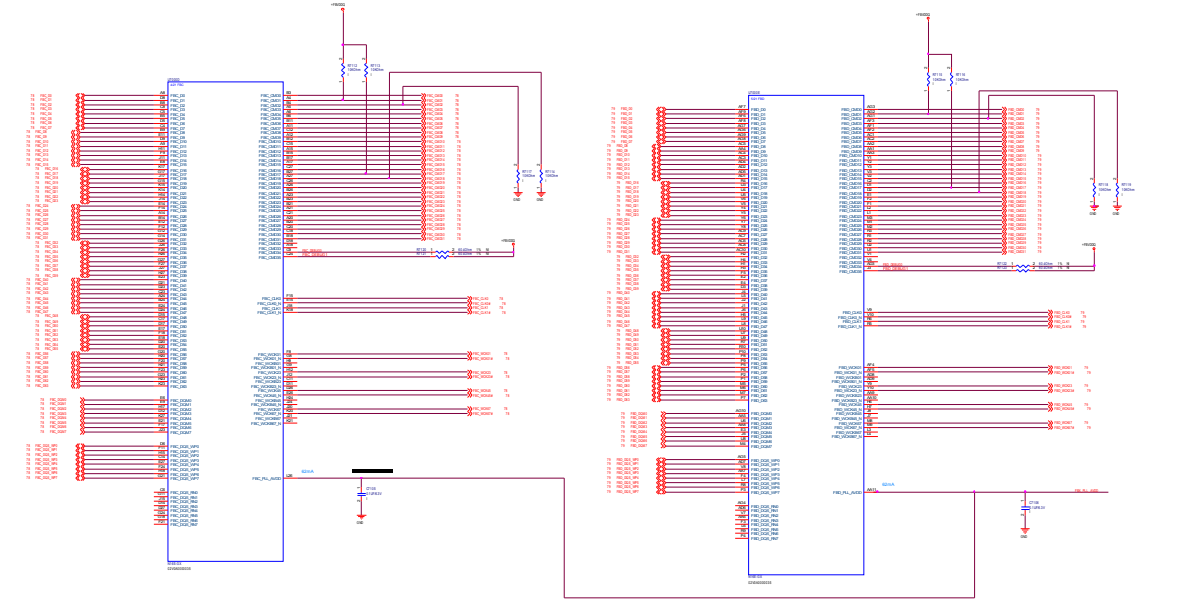
R1.01-2012/09/28: Change CE1 for +1P05V_GPU

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	NVDIAPCIE
Pegatron Corp.	Engineer:	Allens_Hsu
Size: D	Project Name:	P5NCN/P7NCN MAIN BOARD
Date: Monday, September 07, 2015	Sheet	78 of 104

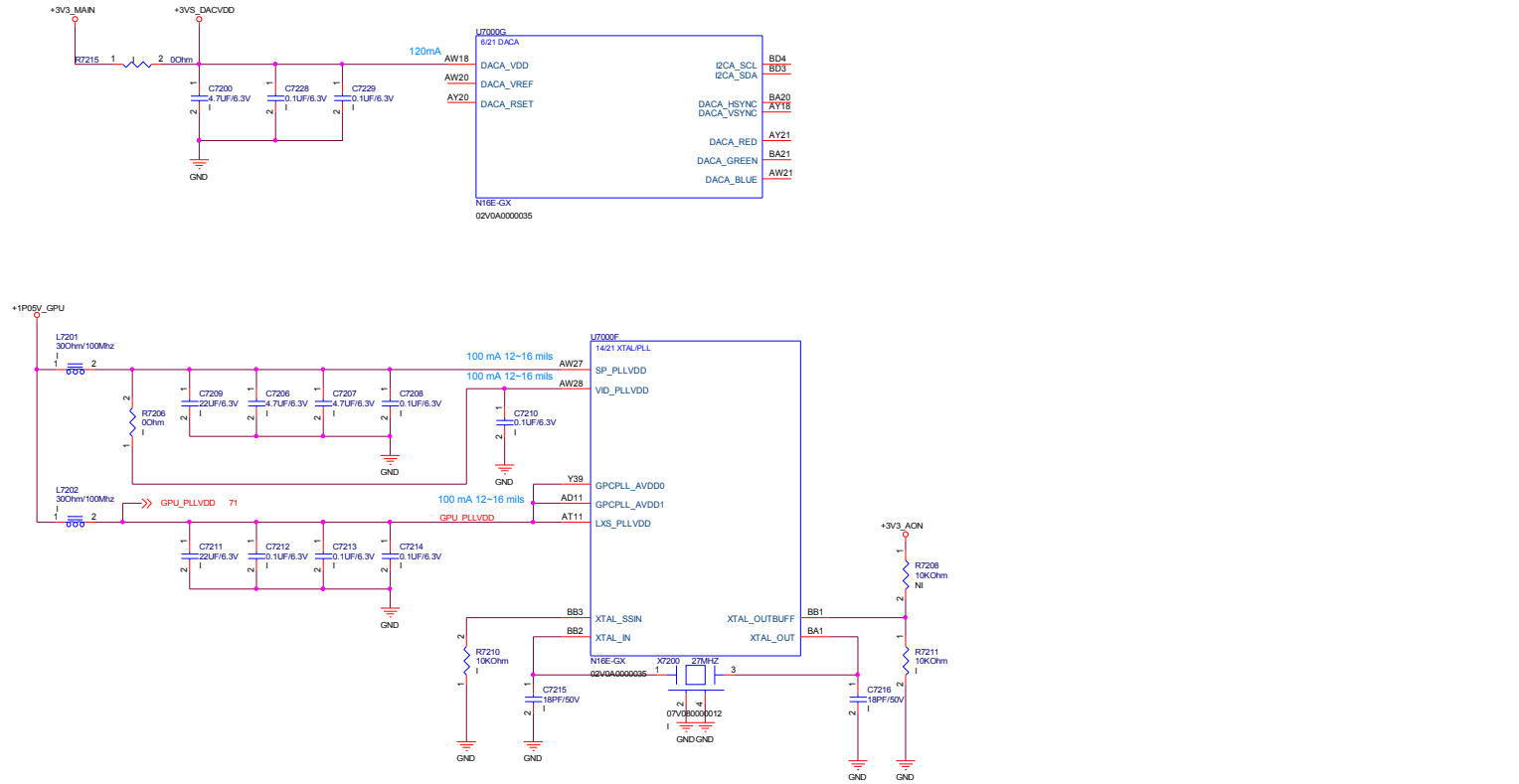
Frame Buffer Partitions A/B





PEGATRON Title : NVDIA/BUFFERAB
Engineer: Athena_Xiao
PSRCH/PTRCH MAIN BOARD

Power/Decoupling: +NVVDD,3V3_NV,GRND,and Optional



<variant_name>

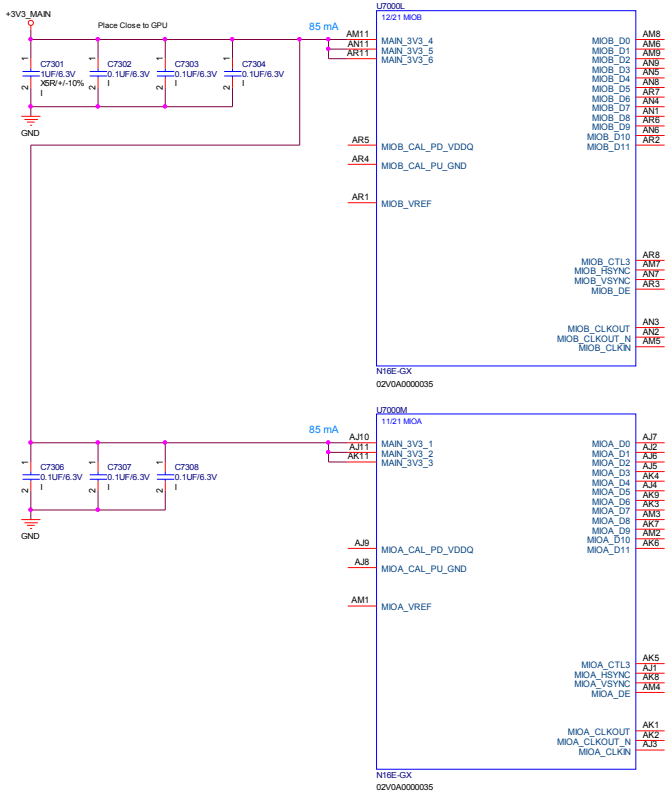
PEGATRON Title : NVDIA/DACA/XTAL

Pegatron Corp. Engineer: Aliens_Hsu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

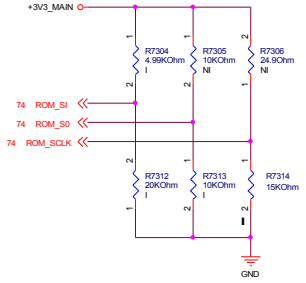
Date: Monday, September 07, 2015 Sheet 72 of 104

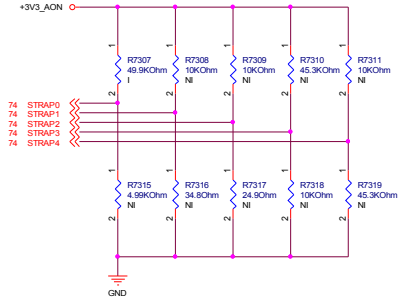
BIOS, External SS, and Mechanical Components



ROM_SI RAM CONFIG

```
Hynix(H5GC4H24AJR)  128Mx32  -> ram_cfg = 0x8      4.99K PU
Samsung 128Mx32 -> ram_cfg = 0x3                    20K PD
```





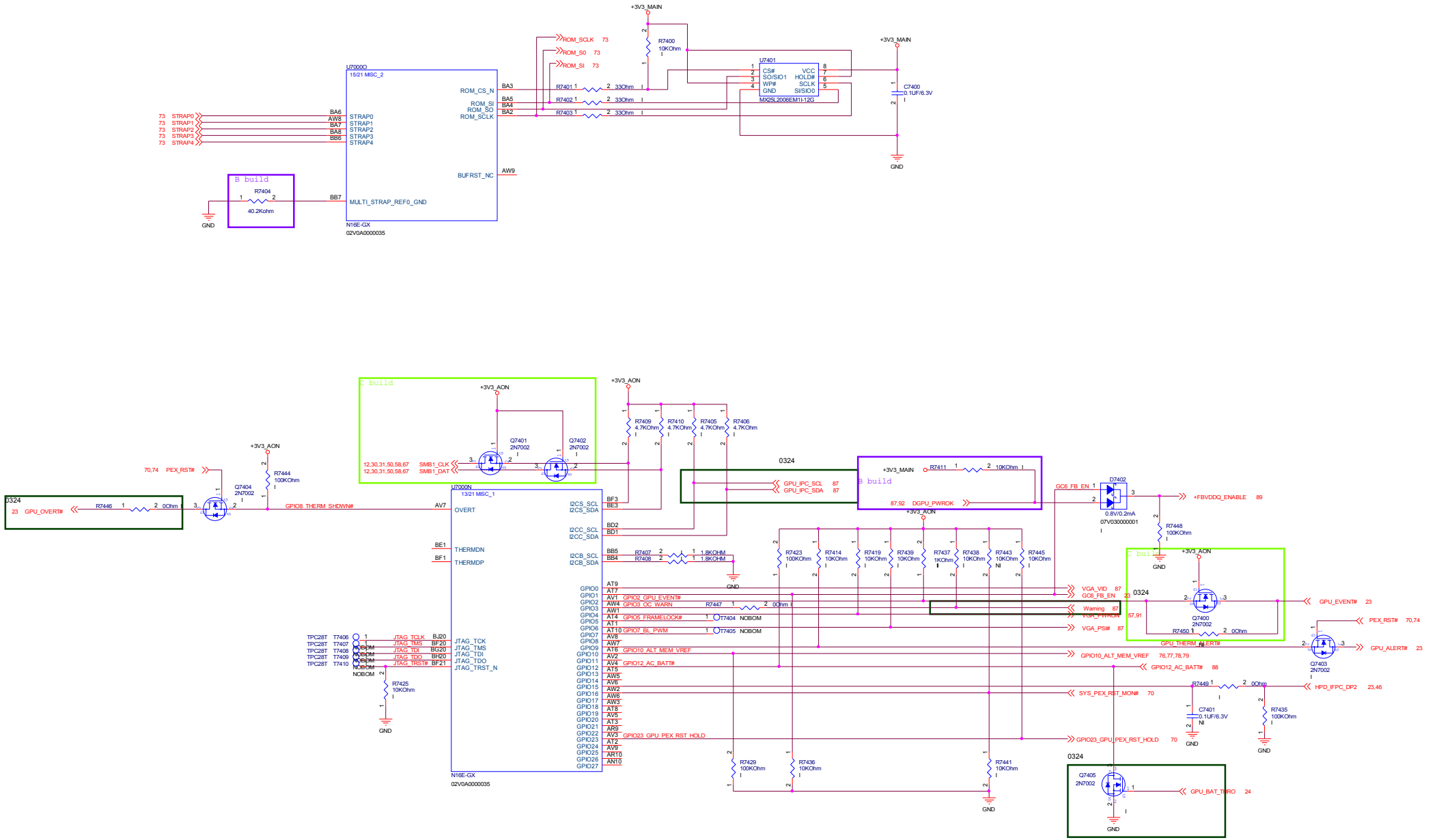
<Variant Name>

PEGATRON Title : NVDIA/Multi-use IO

Pegatron Corp. Engineer: Aliens_Hsu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 73 of 104



PEGATRON DT-MB RESTRICTED SECRET

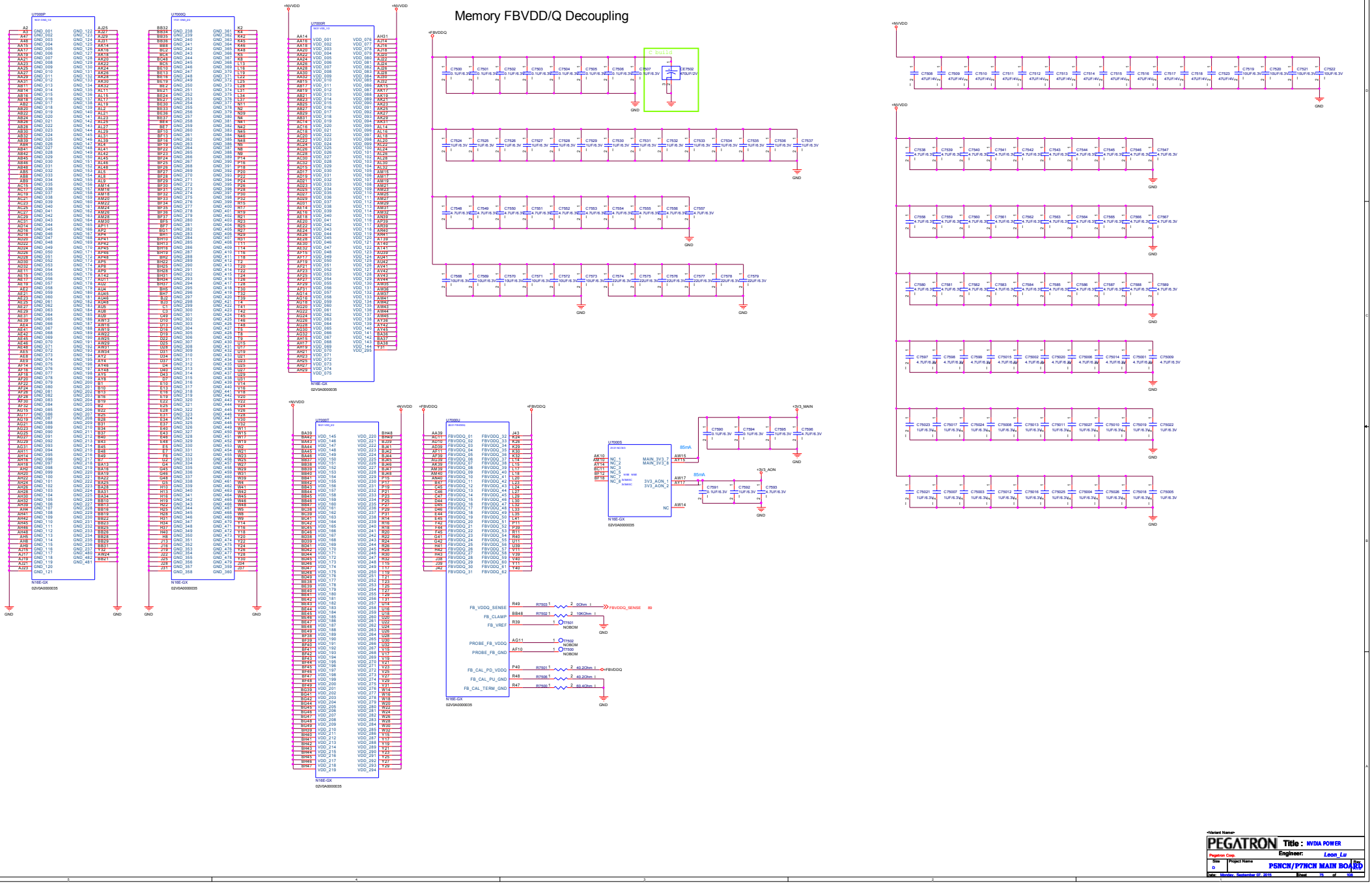
PEGATRON Title : NVDIA MISC/GPIO

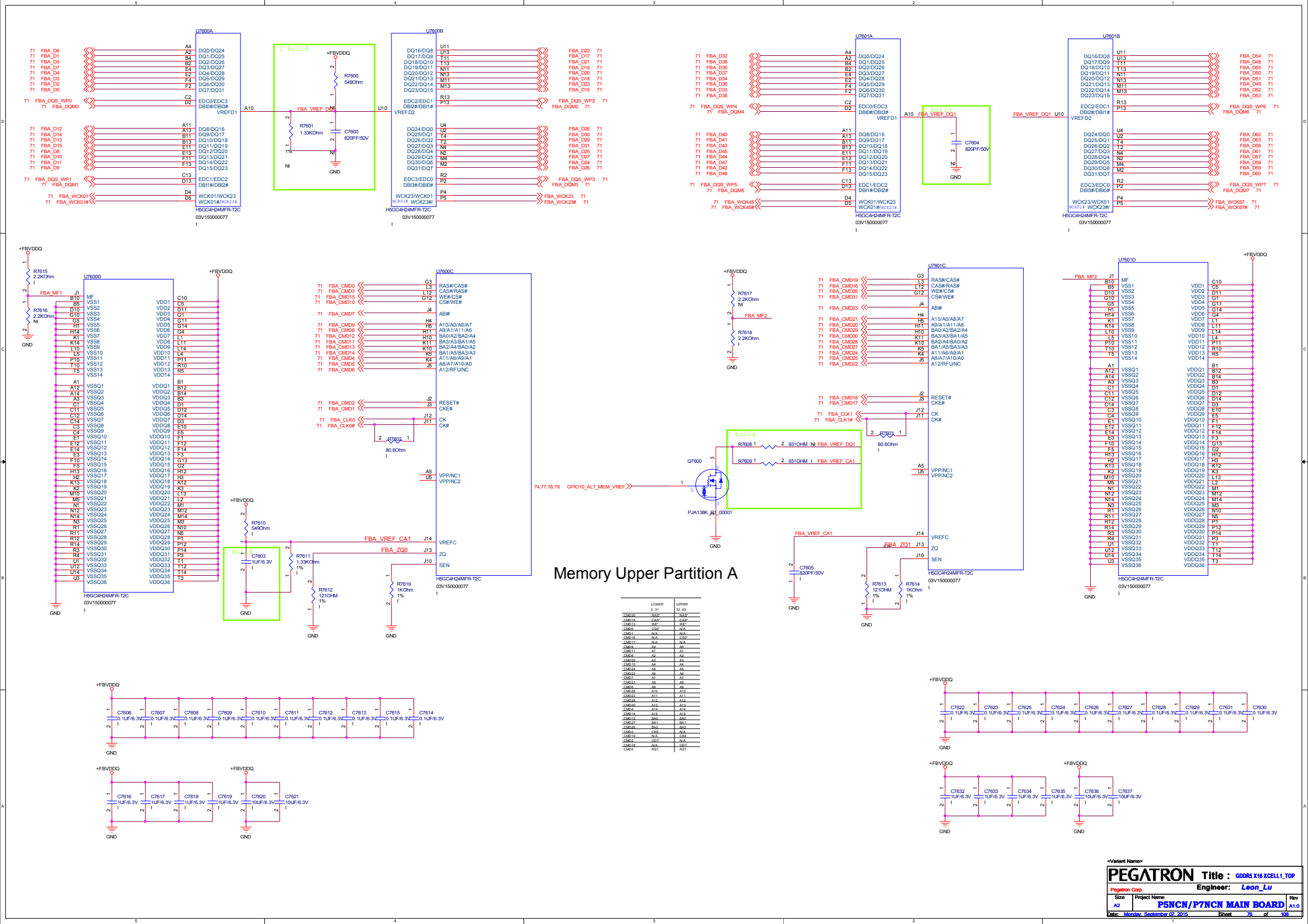
Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 74 of 108

Memory FBVDD/Q Decoupling





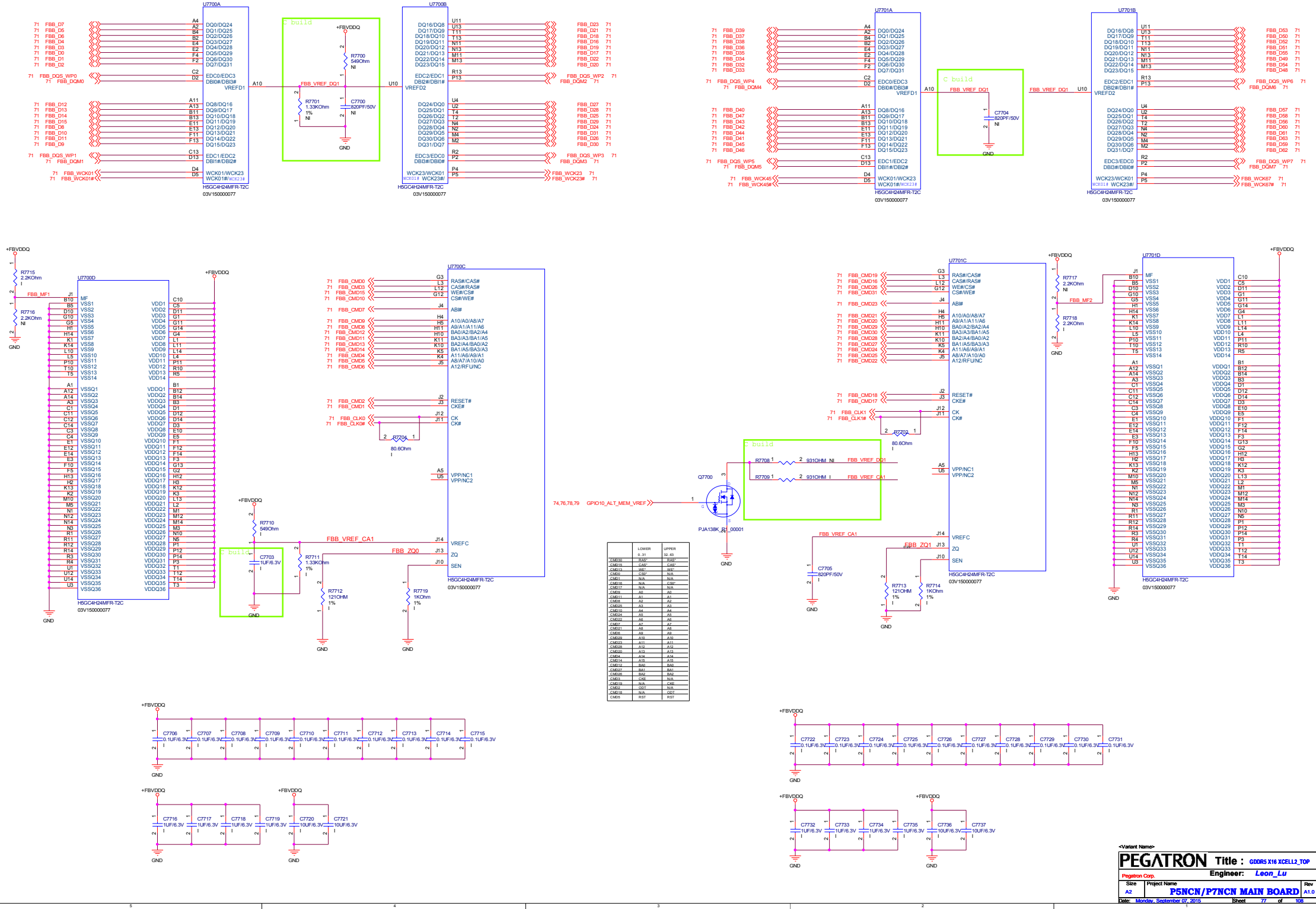
<variant_name>

PEGATRON Title : GDDR5 X16 XCELL1_TOP

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 78 of 108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U7700B
U7701A
U7701B
U7700C
U7700D
U7701C
U7701D
H5GC4H24MFR-T2C
03V150000077
C build
+FBVDDQ
GND
FBB_VREF_DQ1
FBB_VREF_CA1
FBB_ZQ0
FBB_ZQ1
FBB_MF1
FBB_MF2
R7700 549Ohm NI
R7701 1.33KOhm 1% NI
C7700 820PF/50V NI
C7704 820PF/50V NI
R7705 820PF/50V
R7715 2.2KOhm
R7716 2.2KOhm NI
R7717 2.2KOhm NI
R7718 2.2KOhm
R7702 80.6Ohm
R7708 931OHM NI
R7709 931OHM
Q7700
PJA138K_R1_00001
R7710 549Ohm
R7711 1.33KOhm 1%
R7712 121OHM 1%
R7719 1KOhm 1%
R7713 121OHM 1%
R7714 1KOhm 1%
C7703 1UF/6.3V
C7706 0.1UF/6.3V
C7707 0.1UF/6.3V
C7708 0.1UF/6.3V
C7709 0.1UF/6.3V
C7710 0.1UF/6.3V
C7711 0.1UF/6.3V
C7712 0.1UF/6.3V
C7713 0.1UF/6.3V
C7714 0.1UF/6.3V
C7715 0.1UF/6.3V
C7716 1UF/6.3V
C7717 1UF/6.3V
C7718 1UF/6.3V
C7719 1UF/6.3V
C7720 10UF/6.3V
C7721 10UF/6.3V
C7722 0.1UF/6.3V
C7723 0.1UF/6.3V
C7724 0.1UF/6.3V
C7725 0.1UF/6.3V
C7726 0.1UF/6.3V
C7727 0.1UF/6.3V
C7728 0.1UF/6.3V
C7729 0.1UF/6.3V
C7730 0.1UF/6.3V
C7731 0.1UF/6.3V
C7732 1UF/6.3V
C7733 1UF/6.3V
C7734 1UF/6.3V
C7735 1UF/6.3V
C7736 10UF/6.3V
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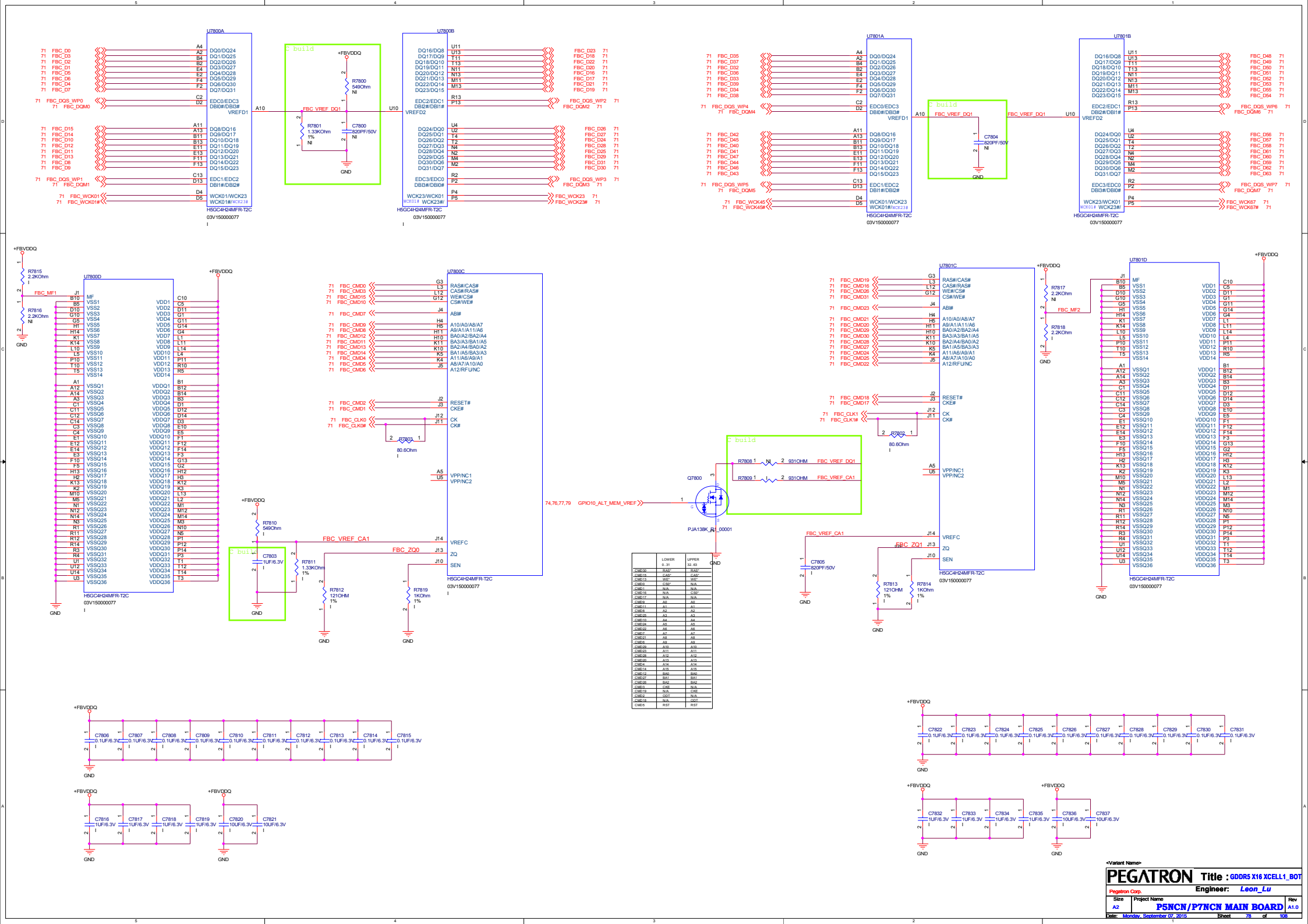
74,76,78,79 GPIO10_ALT_MEM_VREF
LOWER 0..31
UPPER 32..63
<Variant Name>
PEGATRON
Title : GDDR5 X16 XCELL2_TOP
Pegatron Corp.
Engineer: Leon_Lu
Size A2
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 77 of 108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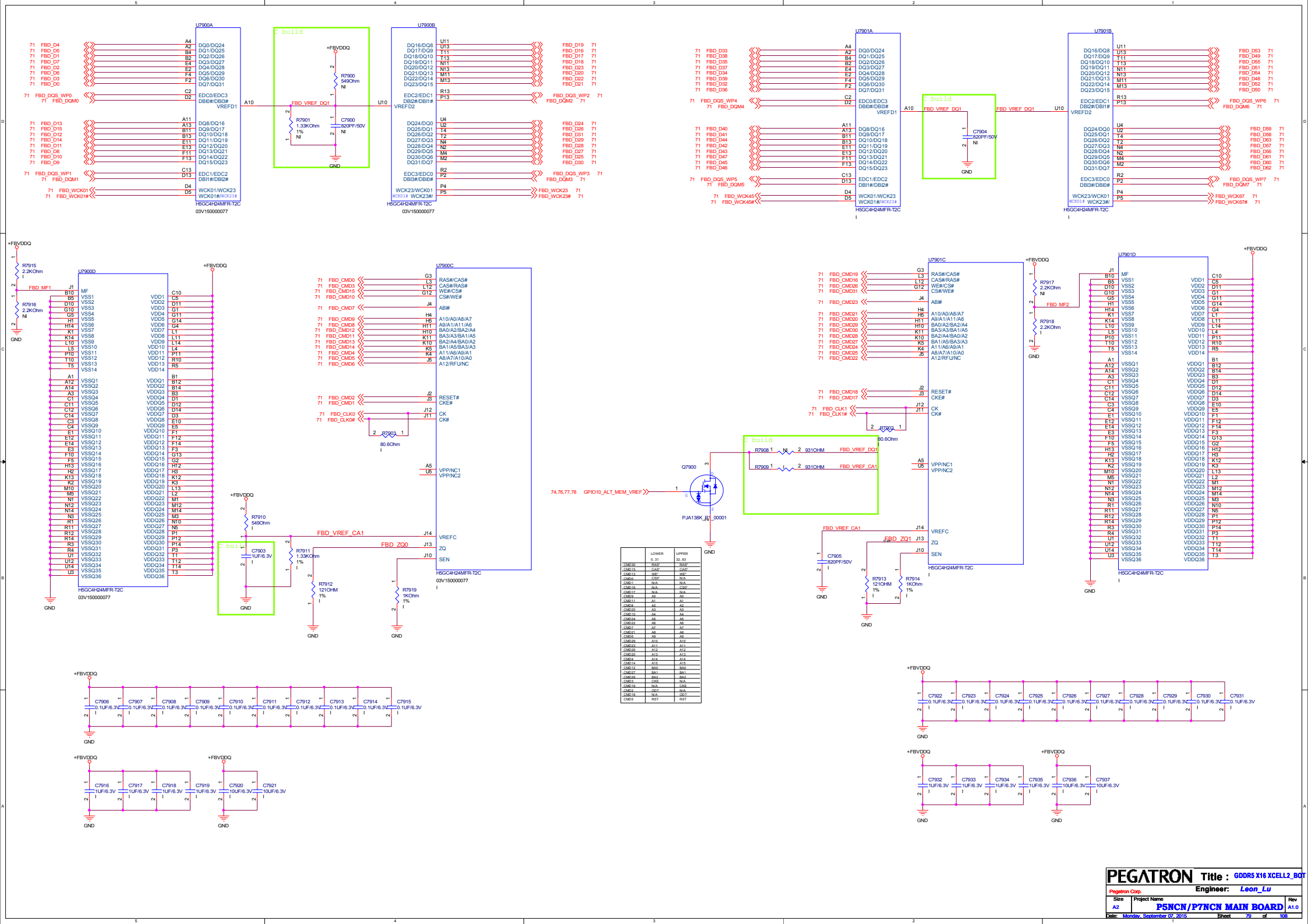
U7800B
U7801A
U7801B
U7800C
U7800D
U7801C
U7801D
H5GC4H24MFR-T2C
03V150000077
C build
+FBVDDQ
GND
FBC_VREF_DQ1
FBC_VREF_CA1
FBC_ZQ0
FBC_MF1
FBC_MF2
R7800 549Ohm NI
R7801 1.33KOhm 1%
C7800 820PF/50V NI
R7802 80.6Ohm
R7803 80.6Ohm
R7804 820PF/50V NI
R7805 820PF/50V
R7807 931OHM
R7808 931OHM
R7809 931OHM
R7810 549Ohm
R7811 1.33KOhm 1%
R7812 121OHM 1%
R7813 121OHM 1%
R7814 1KOhm 1%
R7815 2.2KOhm
R7816 2.2KOhm NI
R7817 2.2KOhm NI
R7818 2.2KOhm
R7819 1KOhm 1%
Q7800
PJA138K_R1_00001
GPIO10_ALT_MEM_VREF
C7803 1UF/6.3V
C7806 0.1UF/6.3V
C7807 0.1UF/6.3V
C7808 0.1UF/6.3V
C7809 0.1UF/6.3V
C7810 0.1UF/6.3V
C7811 0.1UF/6.3V
C7812 0.1UF/6.3V
C7813 0.1UF/6.3V
C7814 0.1UF/6.3V
C7815 0.1UF/6.3V
C7816 1UF/6.3V
C7817 1UF/6.3V
C7818 1UF/6.3V
C7819 1UF/6.3V
C7820 10UF/6.3V
C7821 10UF/6.3V
C7822 0.1UF/6.3V
C7823 0.1UF/6.3V
C7824 0.1UF/6.3V
C7825 0.1UF/6.3V
C7826 0.1UF/6.3V
C7827 0.1UF/6.3V
C7828 0.1UF/6.3V
C7829 0.1UF/6.3V
C7830 0.1UF/6.3V
C7831 0.1UF/6.3V
C7832 1UF/6.3V
C7833 1UF/6.3V
C7834 1UF/6.3V
C7835 1UF/6.3V
C7836 10UF/6.3V
C7837 10UF/6.3V
LOWER 0..31
UPPER 32..63
<Variant Name>
PEGATRON
Title : GDDR5 X16 XCELL1_BOT
Pegatron Corp.
Engineer: Leon_Lu
Size A2
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 78 of 108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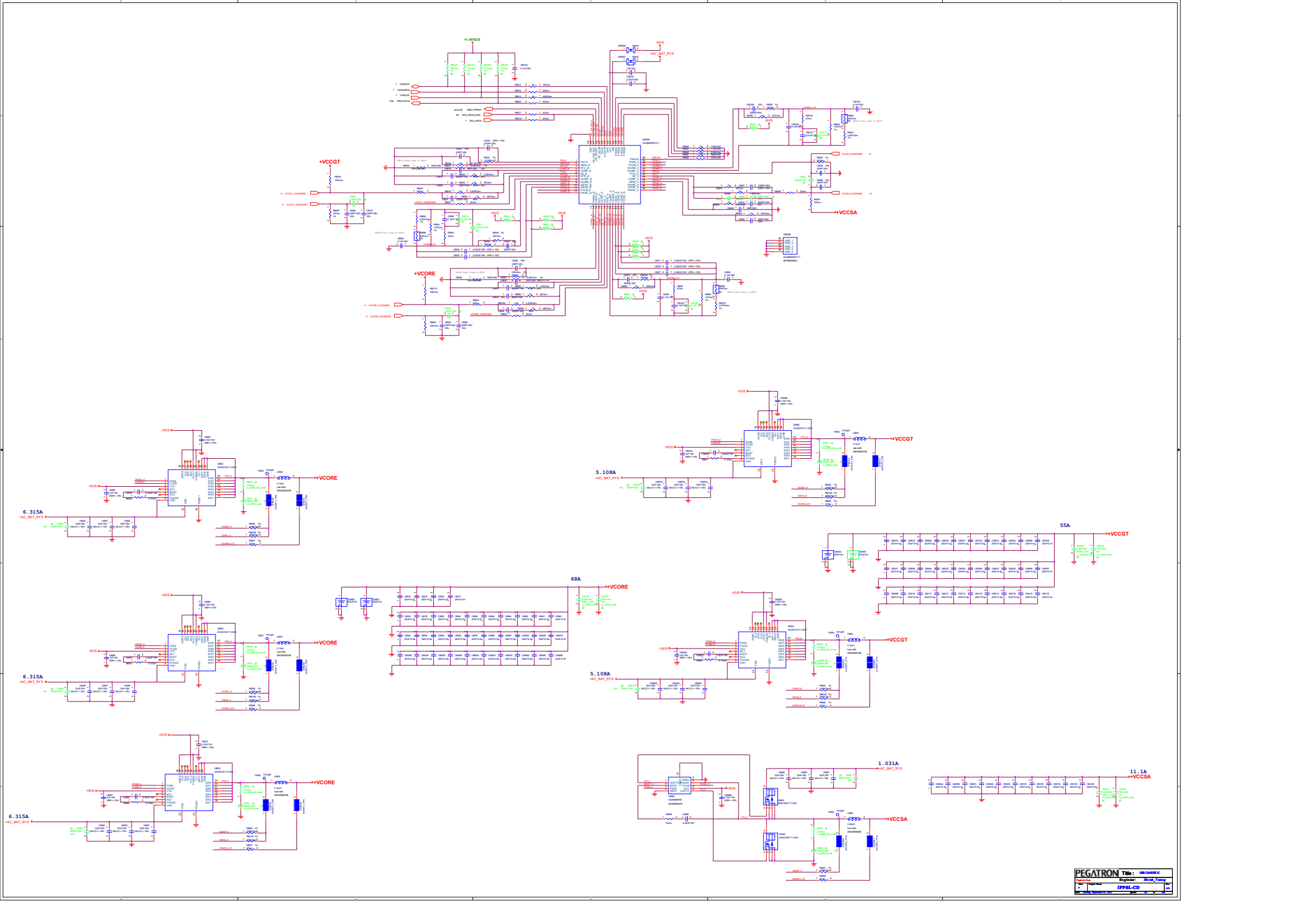
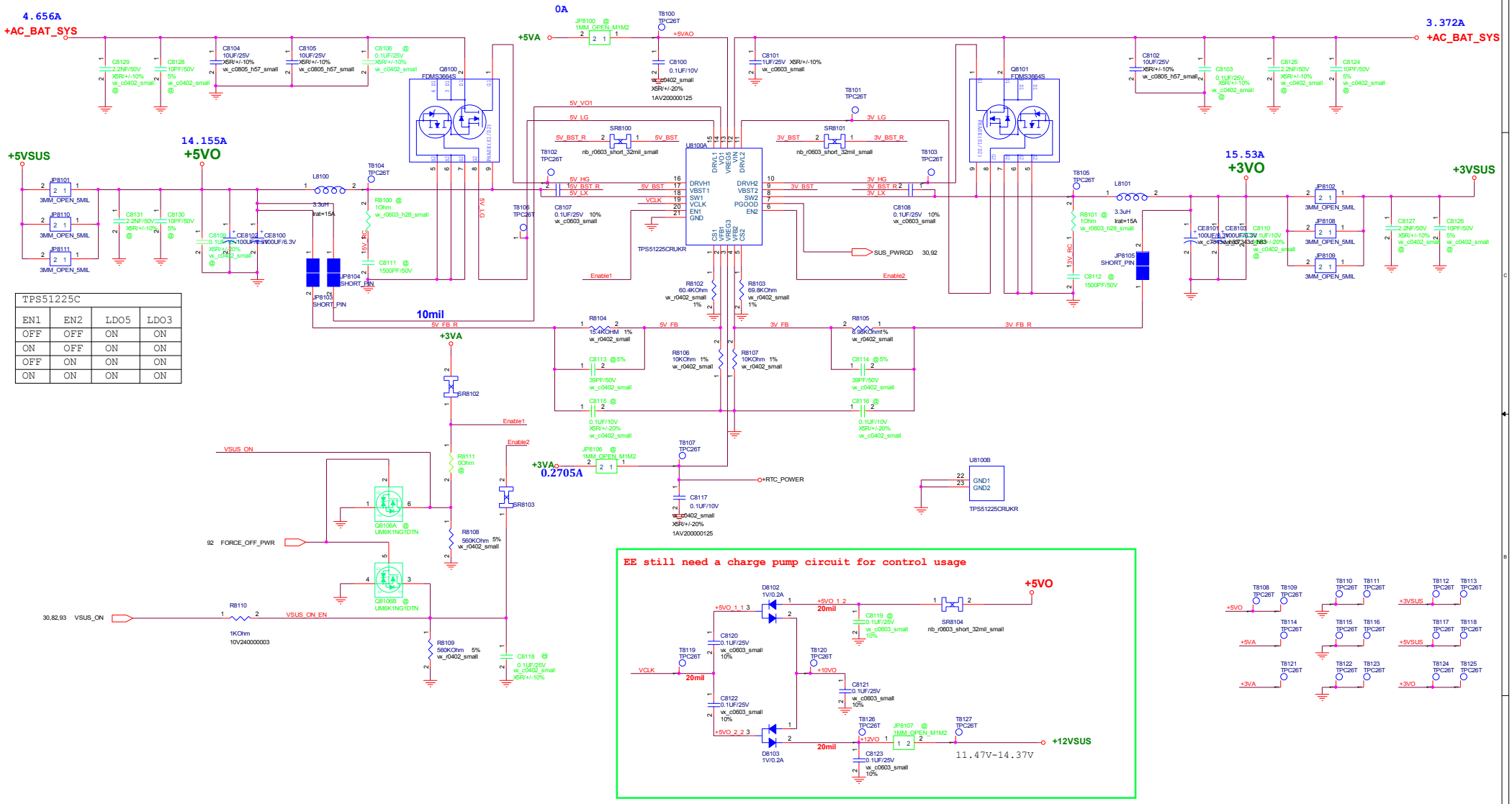
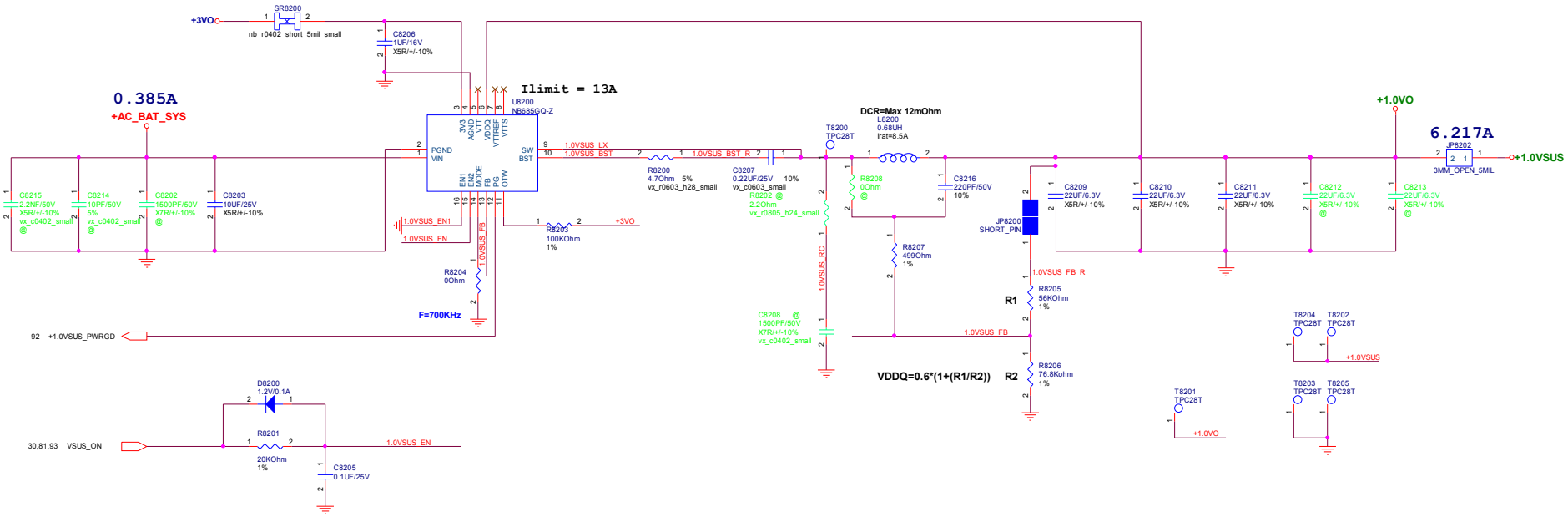
U7900B
U7901A
U7901B
U7900D
U7900C
U7901C
U7901D
H5GC4H24MFR-T2C
03V150000077
+FBVDDQ
GND
C build
R7900 549Ohm NI
R7901 1.33KOhm 1% NI
C7900 820PF/50V NI
C7904 820PF/50V NI
R7915 2.2KOhm NI
R7916 2.2KOhm NI
R7917 2.2KOhm NI
R7918 2.2KOhm NI
R7902 80.6Ohm
R7903 80.6Ohm
R7908 931OHM
R7909 931OHM
Q7900 PJA138K_R1_00001
R7910 549Ohm
C7903 1UF/6.3V
R7911 1.33KOhm 1%
R7912 121OHM 1%
R7919 1KOhm 1%
C7905 820PF/50V
R7913 121OHM 1%
R7914 1KOhm 1%
C7906 C7907 C7908 C7909 C7910 C7911 C7912 C7913 C7914 C7915 0.1UF/6.3V
C7916 C7917 C7918 C7919 1UF/6.3V
C7920 C7921 10UF/6.3V
C7922 C7923 C7924 C7925 C7926 C7927 C7928 C7929 C7930 C7931 0.1UF/6.3V
C7932 C7933 C7934 C7935 1UF/6.3V
C7936 C7937 10UF/6.3V
FBD_VREF_DQ1
FBD_VREF_CA1
FBD_ZQ0
FBD_ZQ1
FBD_MF1
FBD_MF2
74,76,77,78 GPIO10_ALT_MEM_VREF
PEGATRON
Title : GDDR5 X16 XCELL2_BOT
Pegatron Corp.
Engineer: Leon_Lu
Size A2
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 79 of 108


+1.05VSUS
+VCCGT
+VCCSA
+VCORE
+5VS
+AC_BAT_SYS
6.315A
5.108A
68A
55A
1.031A
11.1A
PEGATRON
Title : USB CHARGE IC
Engineer: Brad_Tseng
IPP81_CD

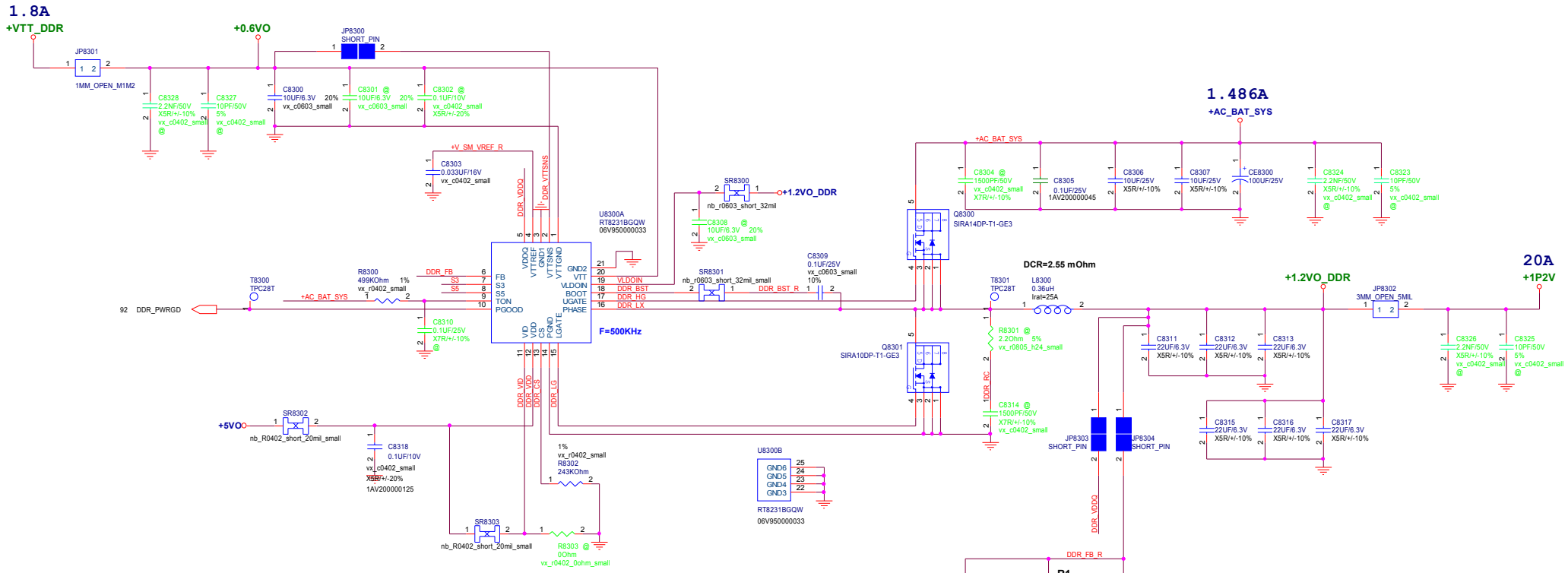
+5VO & +3VO POWER SUPPLY





PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 82 of 108		

DDR & VTT POWER SUPPLY

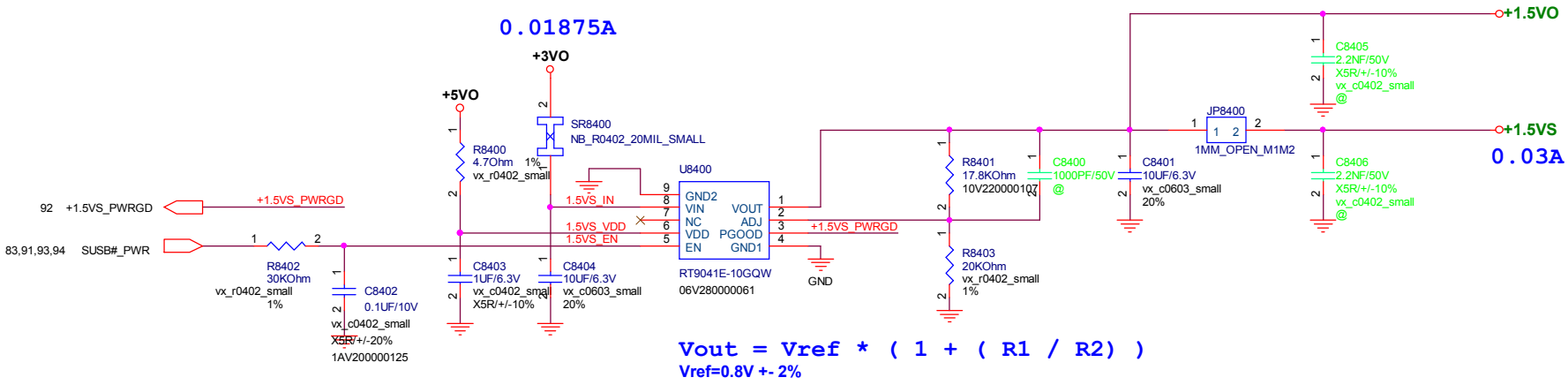


VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 83 of 108		

1.5V POWER SUPPLY



PEGATRON	Title : USB CHARGE IC		
Pegatron Corp.	Engineer: Shrek_Tseng		
Size: B	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 84 of 108		

PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
Custom	IPPSL-CD	A00

Date: Monday, September 07, 2015 Sheet 85 of 108

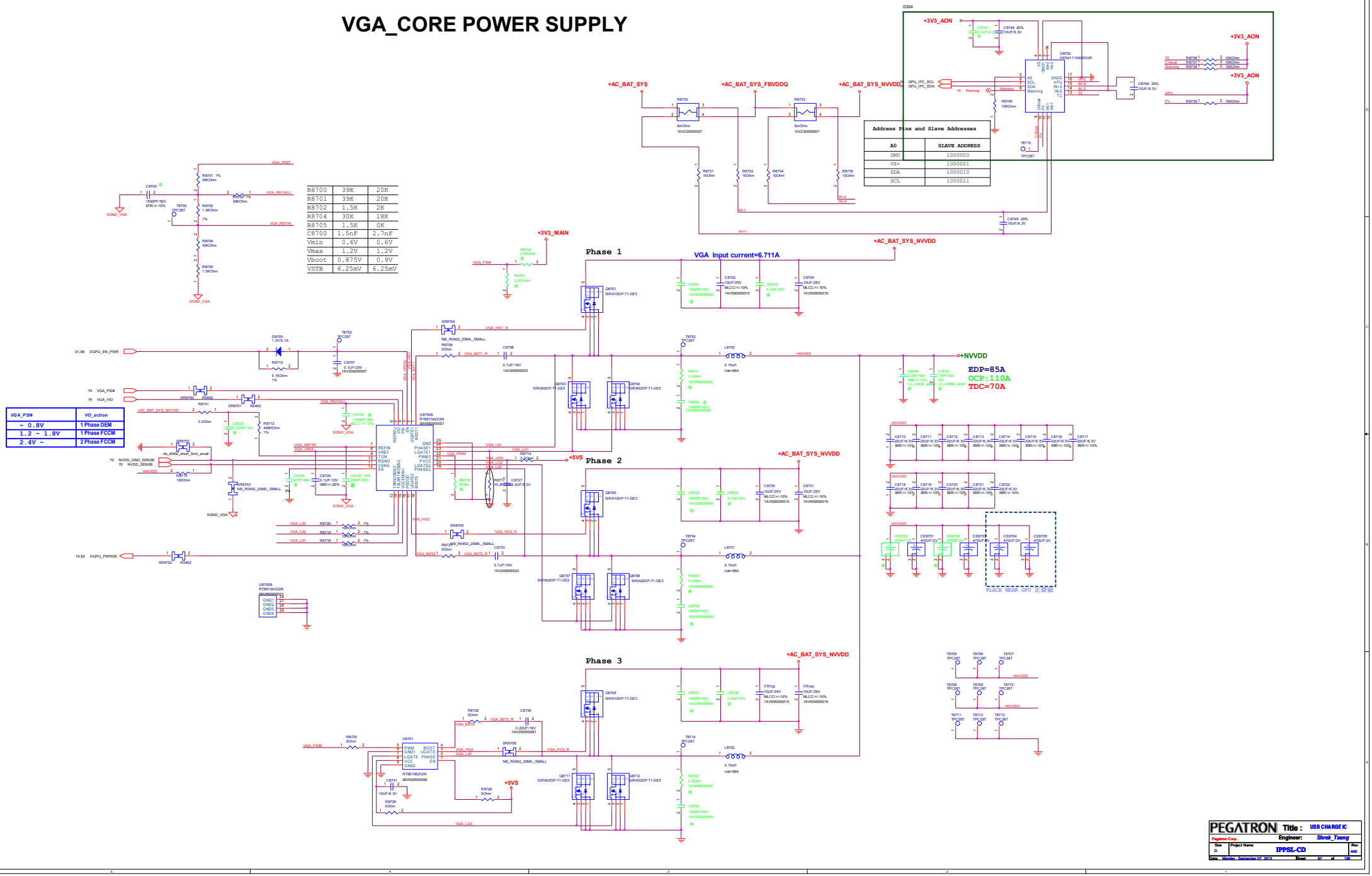
PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
Custom	IPPSL-CD	A00

Date: Monday, September 07, 2015 Sheet 86 of 108

VGA_CORE POWER SUPPLY



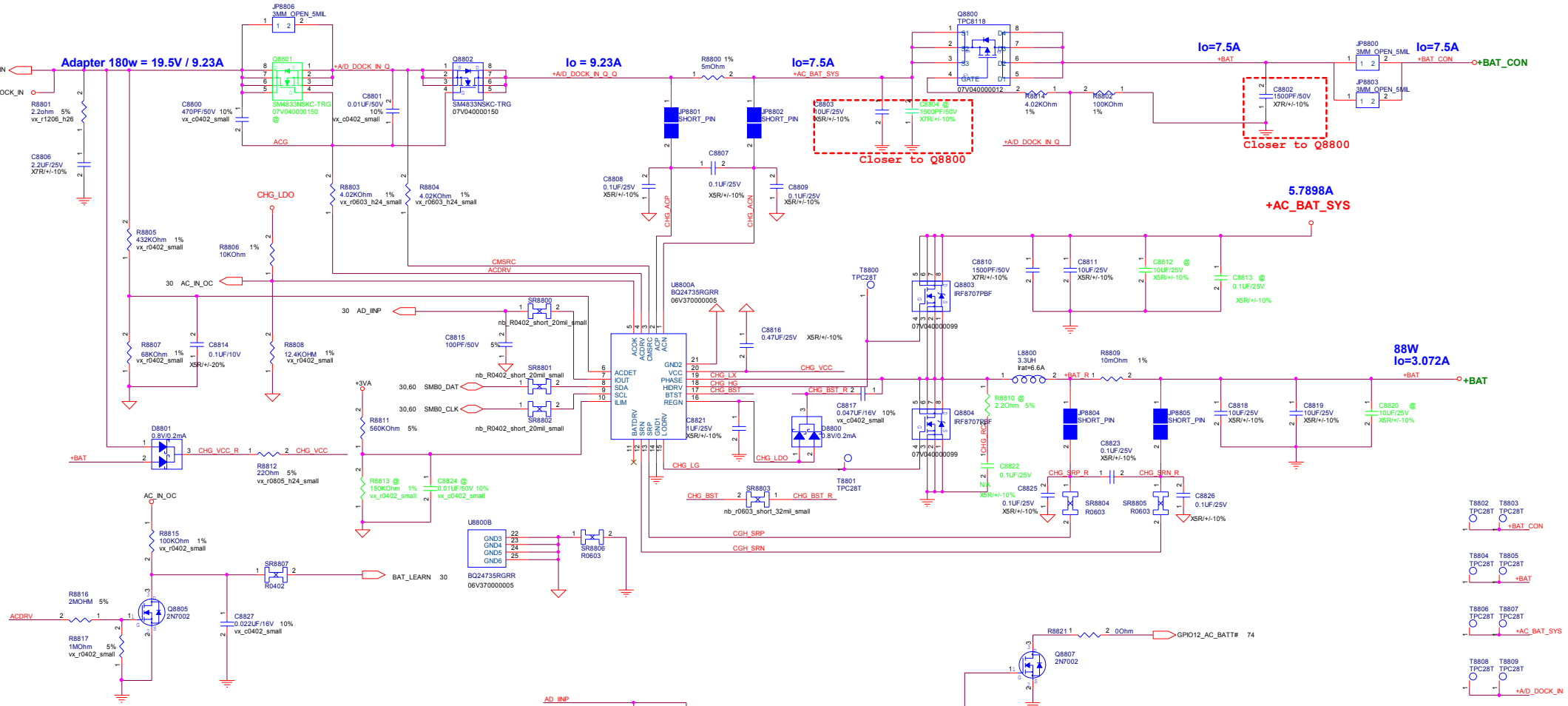
PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Shrek_Tseng

Size D | Project Name IPPSL-CD | Rev A00

Date: Monday, September 07, 2015 Sheet 87 of 106

BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24735RGRR
Support Hybrid Boost?	YES
Adapter capacity	180W
Active/Release Point (Hybrid Boost)	Active - 163.7W Release - 142.3W
Enable condition Disable condition	RSOC>40% RSOC<30%

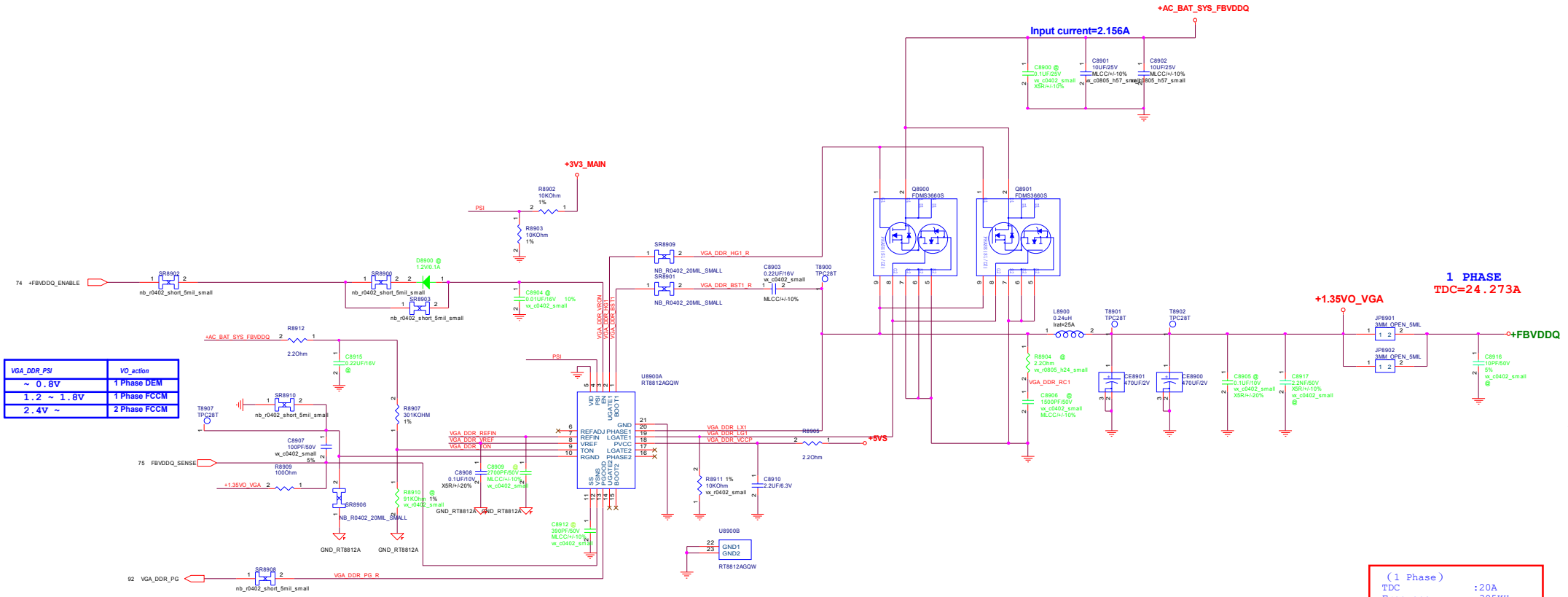
PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
Custom	IPPSL-CD	A00

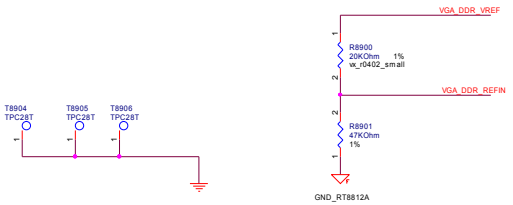
Date: Monday, September 07, 2015 Sheet 88 of 108

+FBVDDQ POWER SUPPLY



VGA_DDR_PSI	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

Vout = Vref (2V) * (R8901/(R8900+R8901))

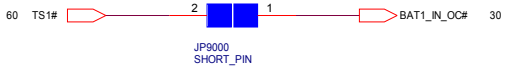


(1 Phase)

TDC	:20A
Frequency	:305KHz
PWR Cap.	:940uF
EE Cap.	:139.5uF
Total Cap.	:1079.5uF
ESR	:3mOHM

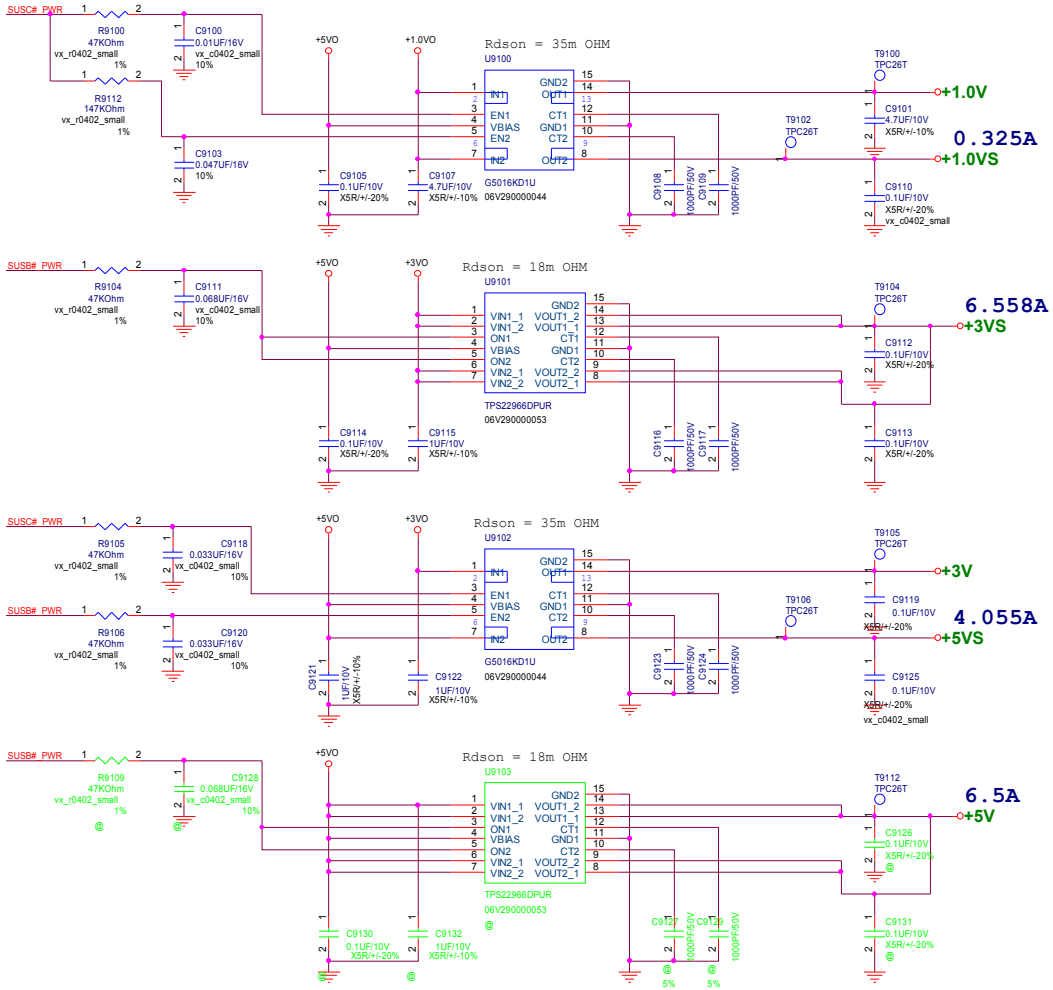
PEGATRON Corp.	Title : USB CHARGE IC	
	Engineer: Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD	Rev: A00
Date: Monday, September 07, 2015	Sheet 89 of 108	

BATTERY IN DETECT

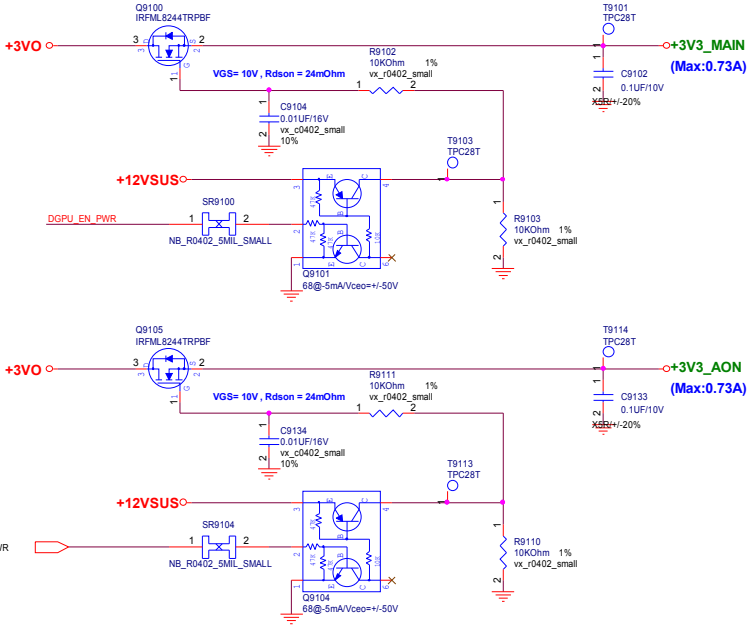


PEGATRON	Title : USB CHARGE IC		
Pegatron Corp.	Engineer: Shrek_Tseng		
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 90 of 108		

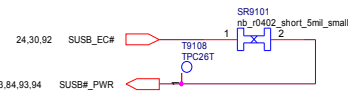
SUSB#_PWR POWER



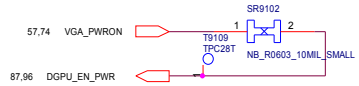
SUSC#_PWR POWER



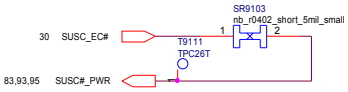
SUSB#_PWR POWER Control



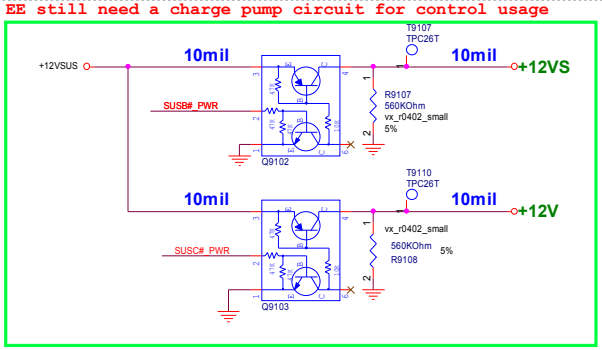
DSC_VGA_PWR POWER Control



SUSC#_PWR POWER Control

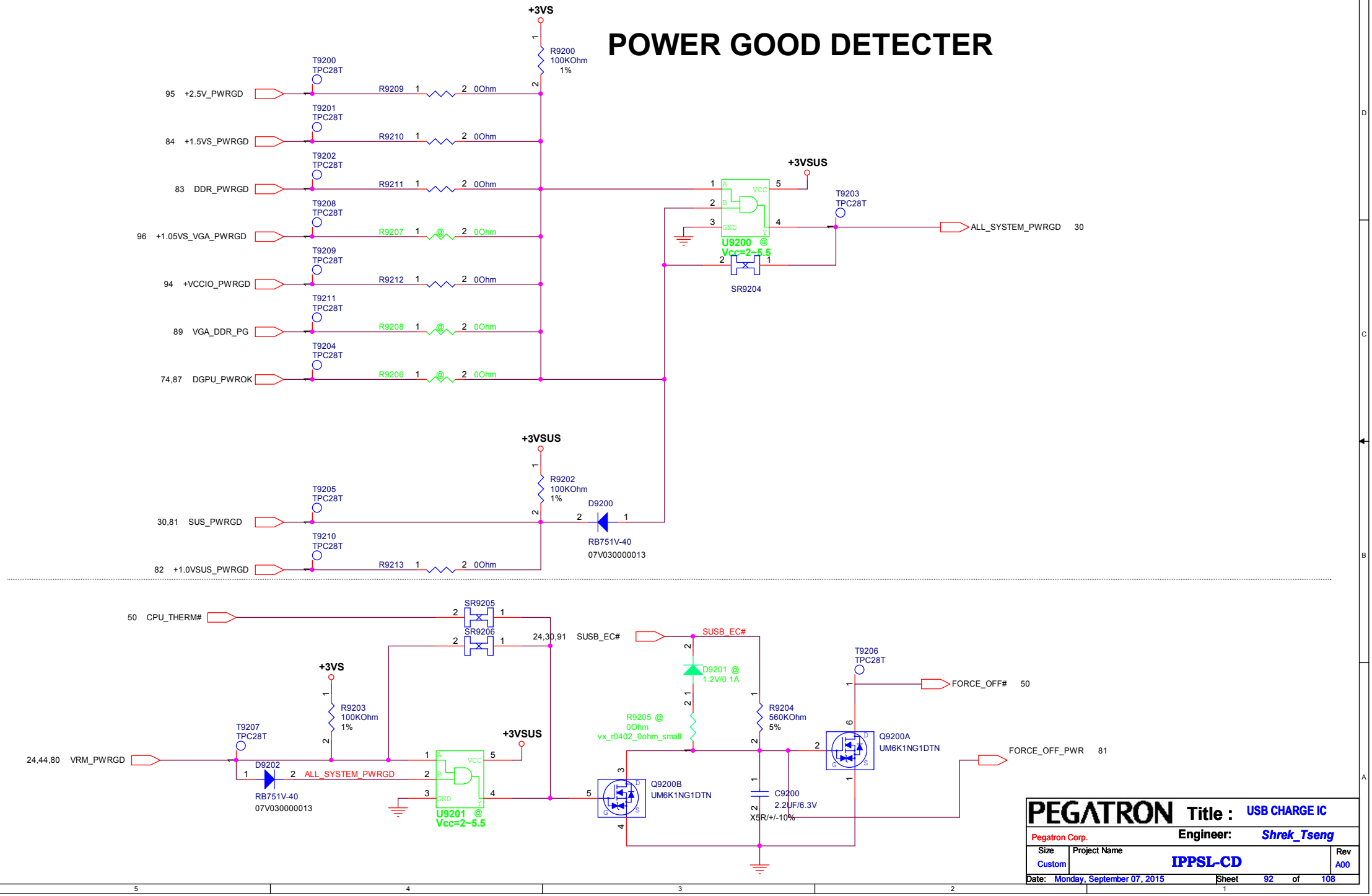


EE still need a charge pump circuit for control usage



PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 91 of 108		

POWER GOOD DETECTER



PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 92 of 108		

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,87,88,94,95,96

+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 53,56,81

+3VA → +3VA 26,30,31,44,45,56,57,60,81,88

+5VO → +5VO 81,83,84,88,91

+3VO → +3VO 81,82,84,91,94

+1.5VO → +1.5VO 84

+5VSUS → +5VSUS 12,36,37,45,52,55,56,67,81

+3VSUS → +3VSUS 7,11,12,21,22,23,24,26,31,33,36,44,52,53,62,81,92

+3V → +3V 91

+5VS → +5VS 31,36,37,43,45,48,50,51,56,80,87,89,91

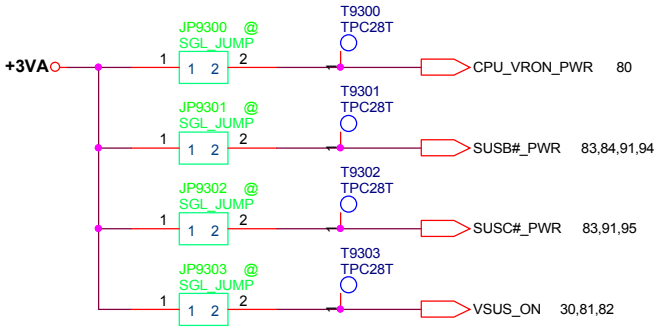
+3VS → +3VS 3,7,11,12,13,14,16,17,21,22,23,24,26,30,31,36,43,44,45,46,48,50,51,53,56,58,61,62,67,70,91,92

+1.5VS → +1.5VS 36,51,84

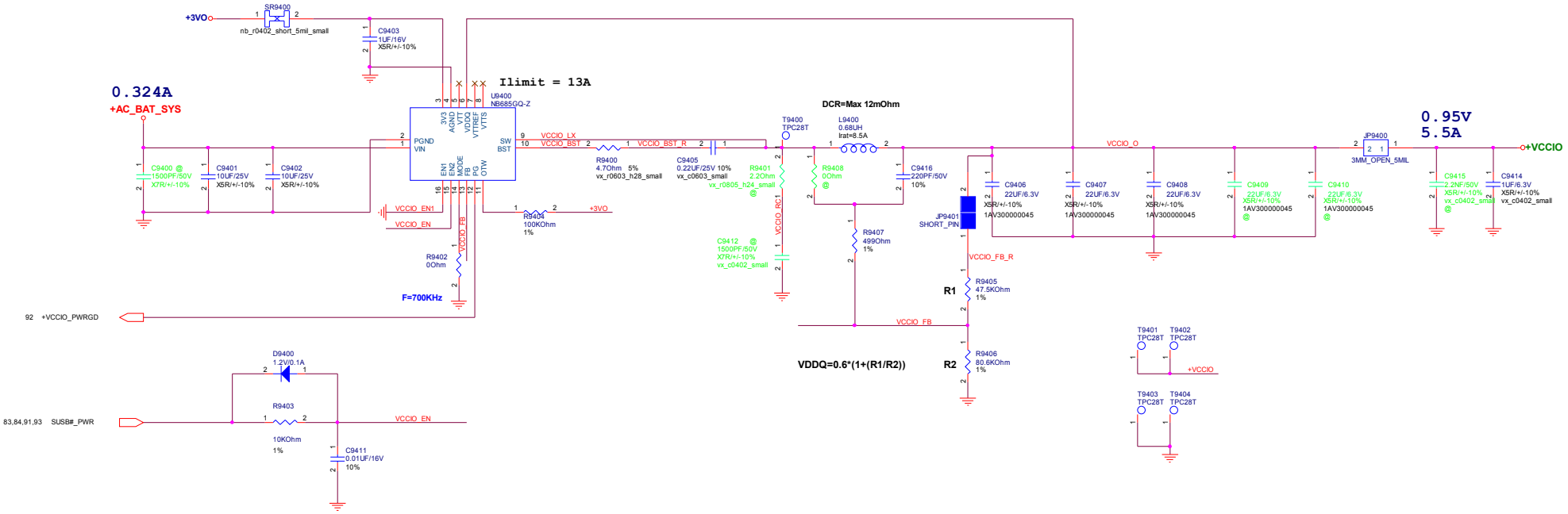
+VCORE → +VCORE 9,80

+VCCIO → +VCCIO 3,6,7,10,44,94

FOR POWER TEST

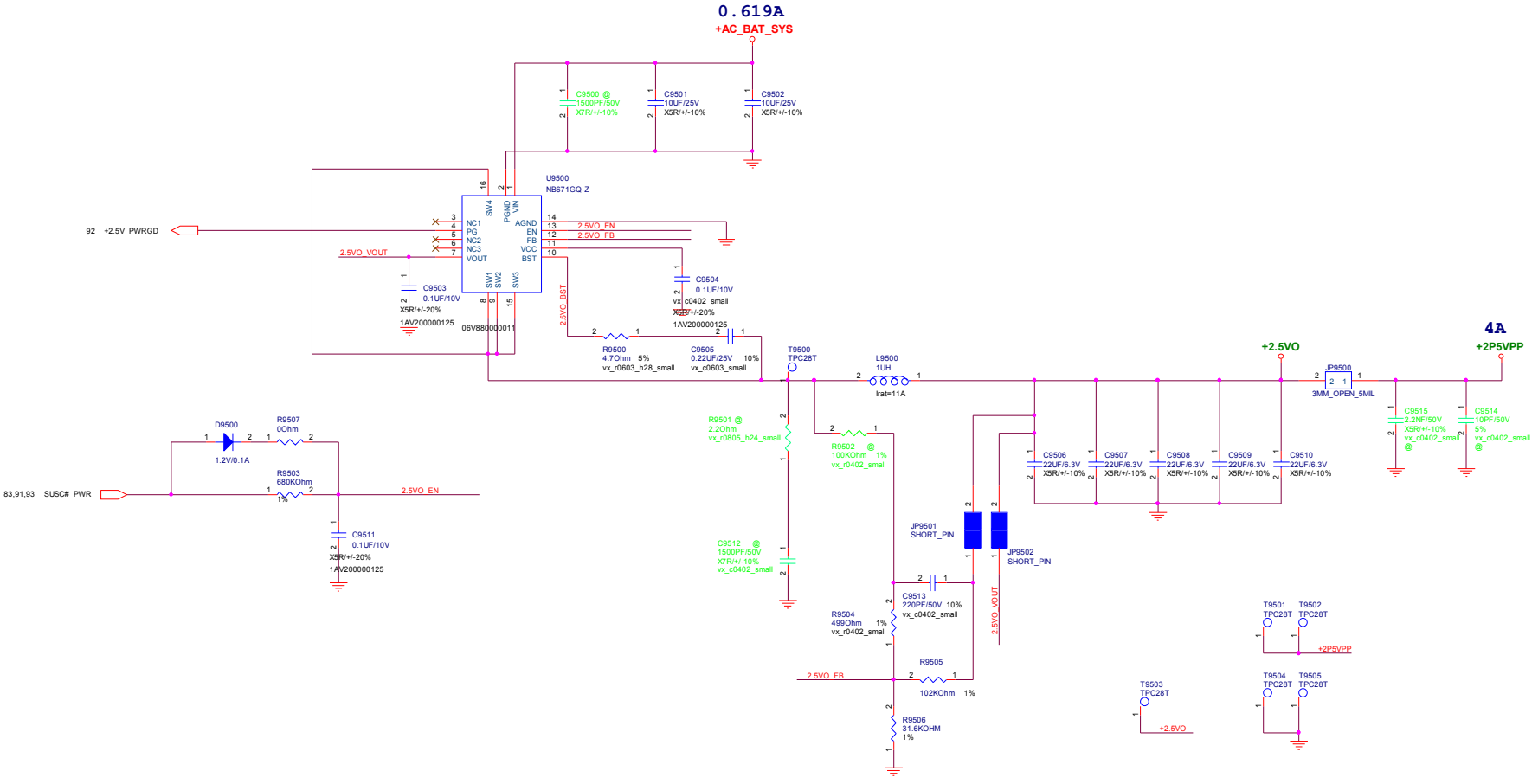


PEGATRON	Title :	USB CHARGE IC
Pegatron Corp.	Engineer:	Shrek_Tseng
Size: Custom	Project Name: IPPSL-CD	Rev: A00
Date: Monday, September 07, 2015	Sheet 93 of 108	



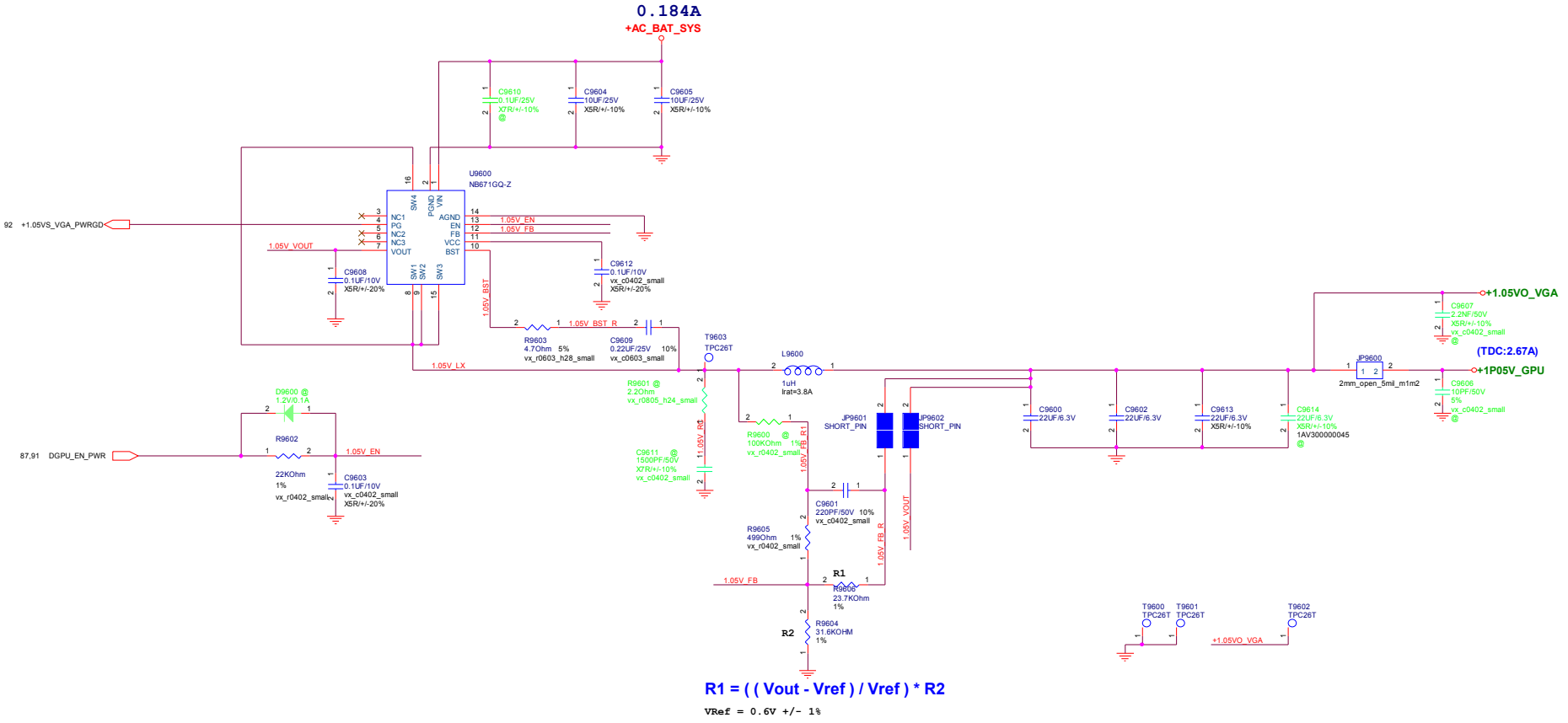
PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 94 of 108		

+2.5V POWER SUPPLY



PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 95 of 108		

1.05VS_VGA POWER SUPPLY



PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 96 of 108		

modify notice

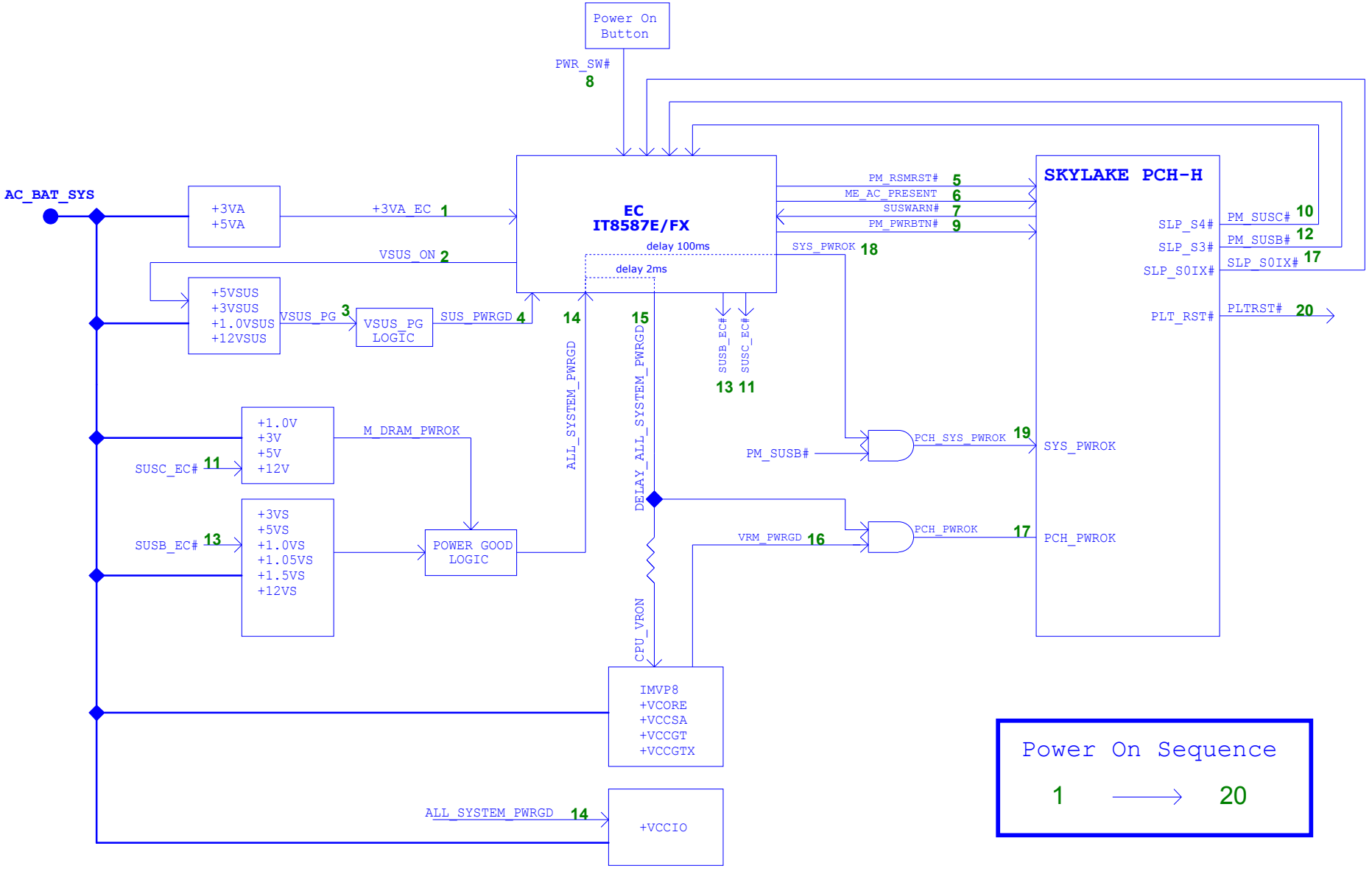
Version	Date	Description

PEGATRON Title : USB CHARGE IC

Engineer: Shrek_Tseng

IPPSL-CD

Power On Sequence Diagram G3-S0 R0.1(non-Deep Sx)



Title	<Title>	
Size C	Document Number PSNCNP7NCN MAIN BOARD	Rev A00
Date: Monday, September 07, 2015	Sheet 99 of 108	

Intel SharkBay and DSW supported

LAN RTL8151GD-CG
RESET#

GPU SUN XT
RESET#

Mini Express x 1 (Half Card)
PERST#

CARDER READER RTS5209-GR
RESET#

Mini Express x 1 (Full Card)
PERST#

RESET_SWITCH

LYNXPOINT PCH

HASWELL PROCESSOR

AUDIO ALC3661-CG
RESET#

POWER_SWITCH
PWRBTN

Fintek SIO F71808AU

<5> PWRBTN#
PSIN#
PCIRST2#
PCIRST1#
<23> PCIE_RST#
LRESET#
<22> PLTRST#
KBRST#
RST_KB#
RSMRST#
<8> RSMRST#
PSOUT#
<5> SB_PWRBTN#
<14> PSON#
PSON#
S3#
<13> SLP_S3#
S4#
<11> SLP_S4#
SUS_WARN#
<9> SUS_WARN#
SUS_ACK#
<10> SUS_ACK#
DPWROK
<4> PCH_DPWROK
PWROK
<16> PWROK
<6> SLP_SUS#

HDA_RST#
AZ_RST#
SYS_RESET#
SYS_RESET#
DBR#
PLTRST#
RCIN#
DRAMPWROK
<17> PM_DRAM_PWRGD
SM_DRAMPWROK
RSMRST#
PWRBTN#
PROCPWRGD
<18> H_CPUPWRGD
PWRGOOD
SLP_S3#
PLTRST_PROC#
<22> PLTRST_CPU#
SLP_S4#
PLTRSTIN#
SLP_A#
SLP_LAN#
RTCRST#
<1> RTCRST#
BATTERY
<16~18> SVIDs
<19> LOAD SVIDs
SUS_WARN#
VIDSOUT/VIDSCLK
SUS_ACK#
VCORE
DPWROK
PWROK
APWROK
SLP_SUS#
SYS_PWROK

MAIN POWER
<15> +19V
+5V
+3P3V
+1P5V
+1P2V
+1P05V

DUAL POWER
<12> +5V_DUAL
+1P35V_DUAL

ALWAYS POWER
<3> +5VA
+3VA

STANDBY POWER
<7> +5VSB
+3VSB

<2> +19VA
+19V Adapter PSU

Vcore Controller
VDIO/VCLK
VCORE
<20> +VCORE
<21> VRM_PWRGD
VR_RDY
EN
<15> +3P3V
TPS51631RSM

MAIN POWER
+3P3V

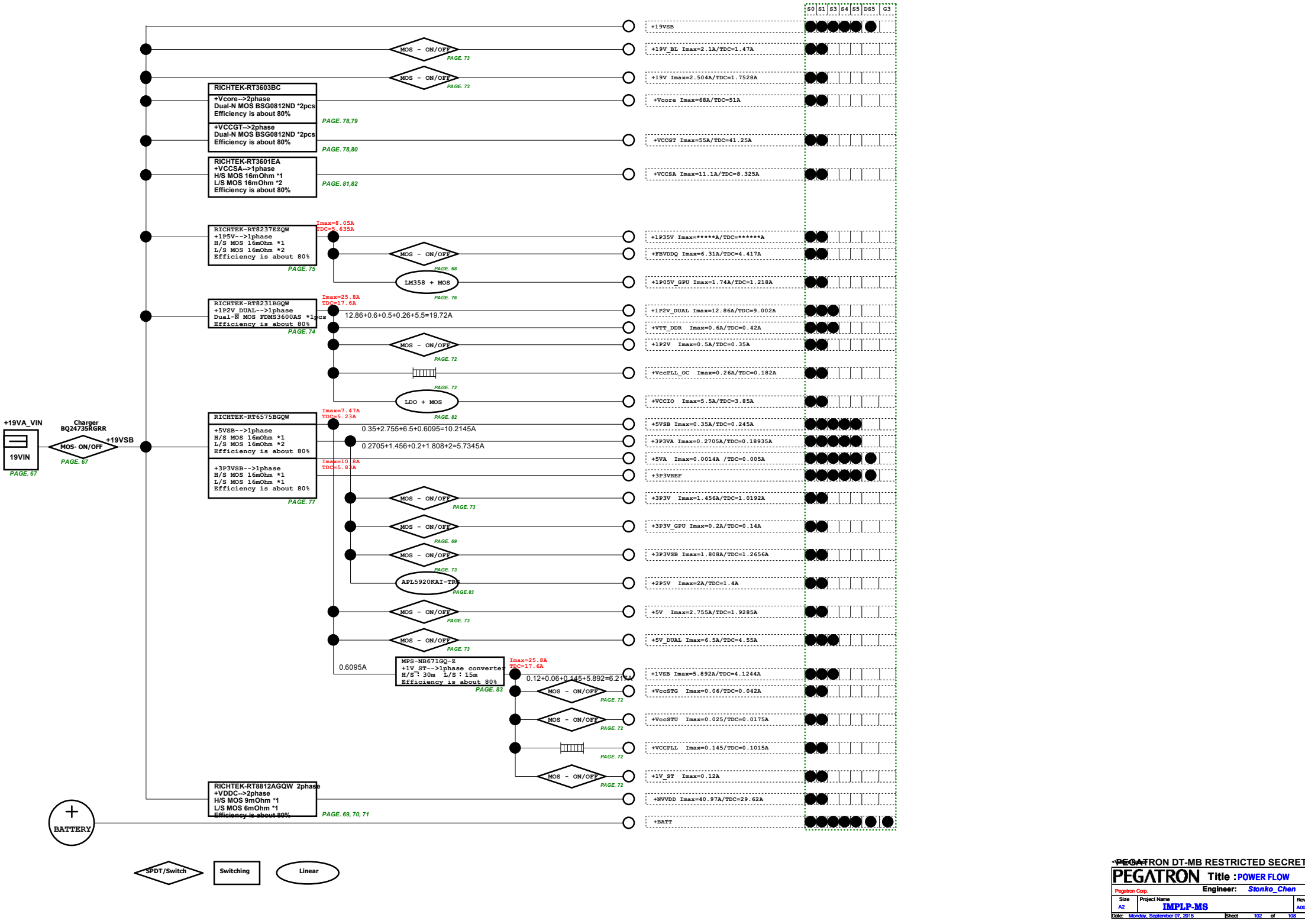
ONBOARD POWER
CHIP
SOCKET or SLOT

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER ON CHART
Pegatron Corp. Engineer: Stonko_Chen
Size A3 | Project Name IMPLP-MS | Rev A00
Date: Monday, September 07, 2015 | Sheet 100 of 108

Schematics Change History

Version	Date	Description	Comments
1.00			



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER FLOW

Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A2	IMPLP-MS	A00

Date: Monday, September 07, 2015 Sheet 102 of 108

Intel Haswell CPU			
	I(max) (A)	TDC (A)	Wattage(W)
+VCORE	85	27	47
+1P35V_DUAL	4.2	2.94	5.67

Intel PCH - Lynx Point HM87			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3V	0.202	0.141	0.67
+3P3VSB	0.293	0.205	0.97
+3VA	0.015	0.011	0.05
+1P5V	0.253	0.177	0.38
+1P05V_PCH	5.921	4.1447	6.22

AMD GPU - SUN-XT (64bit)			
	I(max) (A)	TDC (A)	Wattage(W)
+VDDC(1.125V)	37.5	25	49.19
+VDDCI(0.95V)	9	6	8.55
+3P3V_GPU	0.086	0.06	0.283
+1P8V_MXM	0.53	0.35	0.954
+1P35V_GPU	1.5	1	2.025
+0P95V_GPU	6.03	4.02	5.73

GDDR5 - 2GB			
	I(max) (A)	TDC (A)	Wattage(W)
+1P35V_GPU	5.43	3.8	7.33

SO - DIMM x 2 (DDR3L)			
	I(max) (A)	TDC (A)	Wattage(W)
+1P35V_DUAL	5.12	3.584	6.912
+VTT_DDR	1.43	1	0.97

Scalar - MSTAR TSUMU88BDC2-1			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3V	0.5	0.35	1.65
+1P26V	0.5	0.35	0.6

LOM - Realtek RTL8151GD			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3VSB	0.1	0.07	0.33

Audio - Realtek ALC3661-CG			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3V	0.071	0.05	0.236
+5VSB	0.5	0.35	2.5

Audio AMP - TPA3110D2PWPR			
	I(max) (A)	TDC (A)	Wattage(W)
+19V	0.58	0.404	11.97

SIO - Fintek F71808AU			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3V	0.011	0.008	0.38
+3P3VSB	0.0014	0.001	0.005
+5VA	0.0014	0.001	0.005

Card Reader - Realtek RTS5209-GR			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3V	1.71	1.2	5.66

SATA 3.0 (1-Port for 2.5" HDD)			
	I(max) (A)	TDC (A)	Wattage(W)
+5V	1.57	1.1	7.86

mini_PCIE (Half card)			
	I(max) (A)	TDC (A)	Wattage(W)
+1P5V	0.5	0.375	0.5
+3P3VSB	2.75	1.1	9.075

mini_PCIE (Full card)			
	I(max) (A)	TDC (A)	Wattage(W)
+1P5V	0.5	0.375	0.5
+3P3VSB	2.75	1.1	9.075

USB3.0 (6-Ports)			
	I(max) (A)	TDC (A)	Wattage(W)
+5V_DUAL	5.4	3.78	27

Webcam			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3V	0.323	0.226	1.065

Touch			
	I(max) (A)	TDC (A)	Wattage(W)
+5V_DUAL	1.57	1.1	7.86

HDMI			
	I(max) (A)	TDC (A)	Wattage(W)
+5V	0.055	0.039	0.275

FAN			
	I(max) (A)	TDC (A)	Wattage(W)
+5V	0.5	0.35	2.5

SPI			
	I(max) (A)	TDC (A)	Wattage(W)
+3P3V	0.03	0.03	0.099

PANEL			
	I(max) (A)	TDC (A)	Wattage(W)
+19V_BL	2.1	1.47	39.9
+5V_LCD	1.1	0.8	0.5

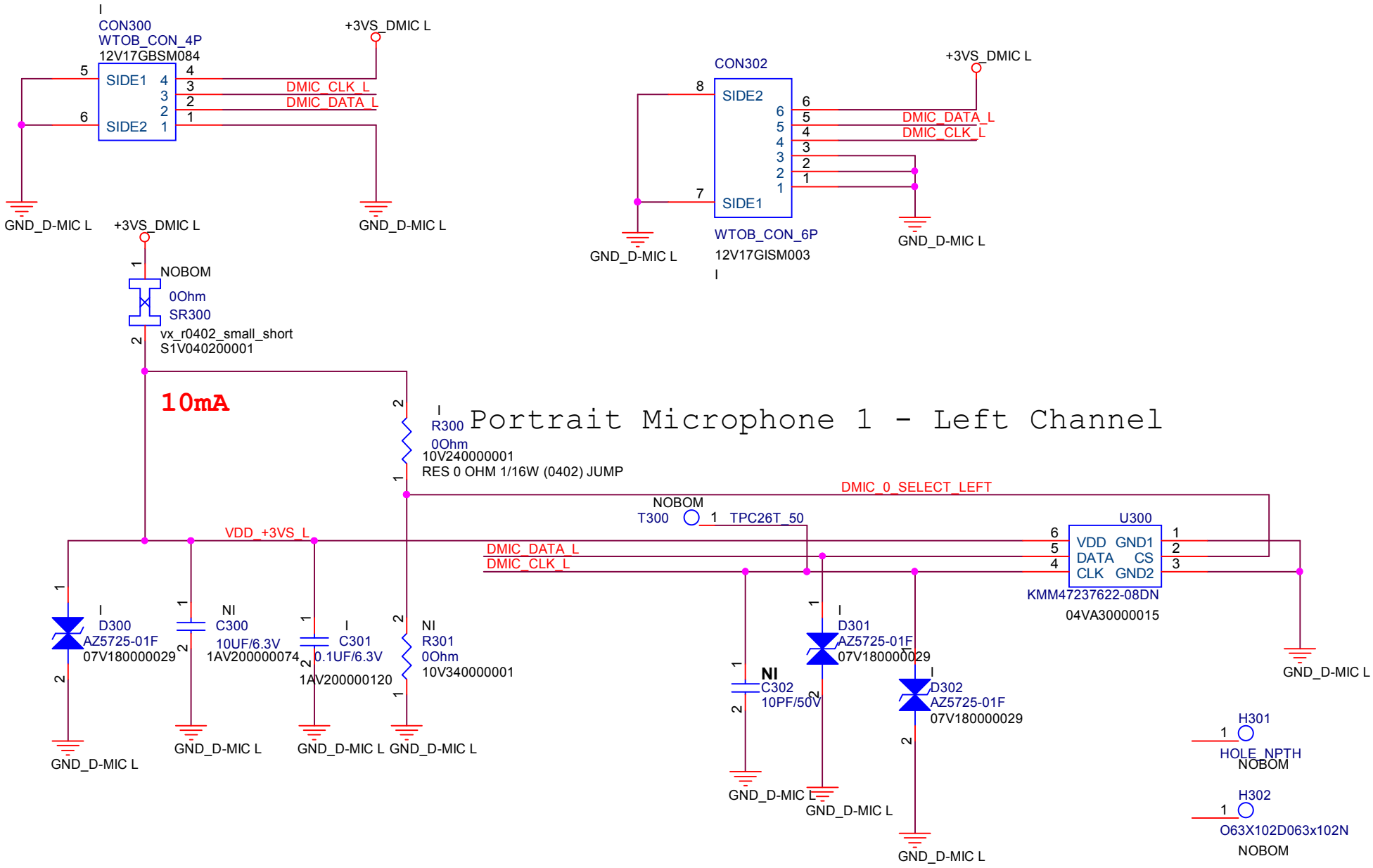
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER DISTRIBUTION

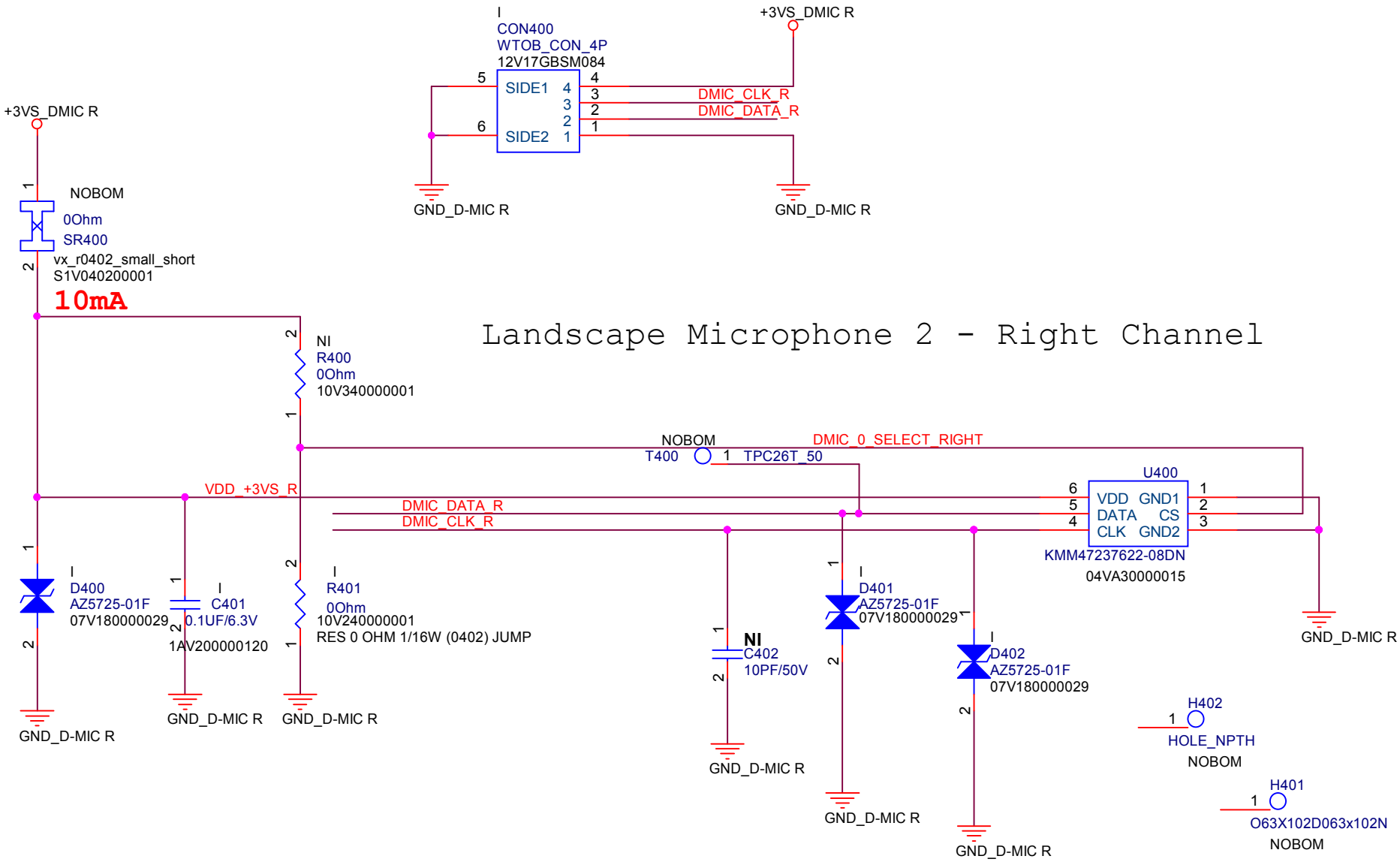
Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00

Date: Monday, September 07, 2015 Sheet 103 of 108

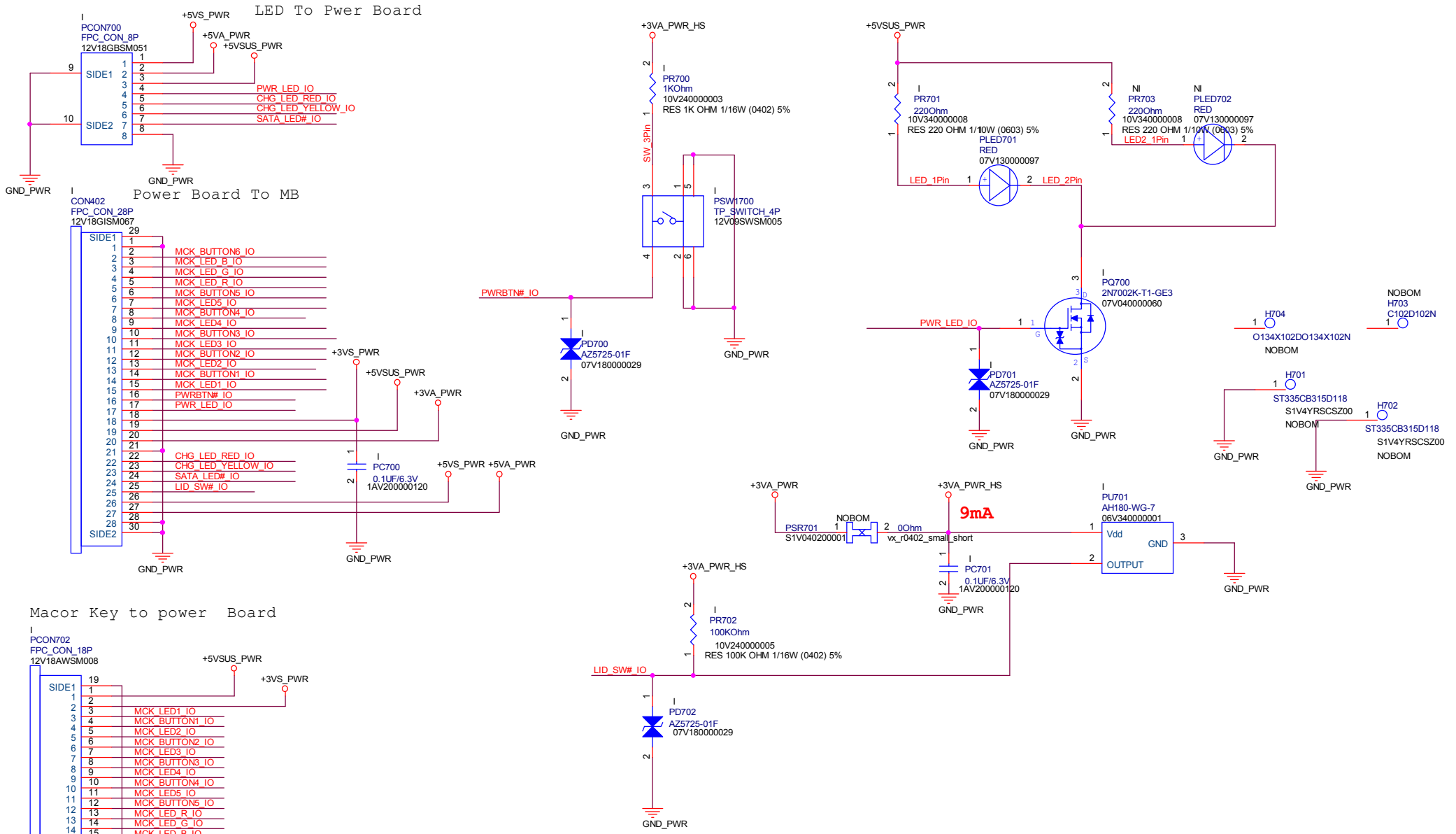

I
CON300
WTOB_CON_4P
12V17GBSM084
SIDE1
SIDE2
+3VS_DMIC L
DMIC_CLK_L
DMIC_DATA_L
GND_D-MIC L
CON302
WTOB_CON_6P
12V17GISM003
NOBOM
0Ohm
SR300
vx_r0402_small_short
S1V040200001
10mA
Portrait Microphone 1 - Left Channel
R300
0Ohm
10V240000001
RES 0 OHM 1/16W (0402) JUMP
DMIC_0_SELECT_LEFT
T300
TPC26T_50
VDD_+3VS_L
U300
VDD GND1
DATA CS
CLK GND2
KMM47237622-08DN
04VA30000015
D300
AZ5725-01F
07V180000029
NI
C300
10UF/6.3V
1AV200000074
C301
0.1UF/6.3V
1AV200000120
R301
0Ohm
10V340000001
C302
10PF/50V
D301
D302
H301
HOLE_NPTH
H302
O63X102D063x102N
<Variant Name>
PEGATRON
Title : D-MIC L BOARD.
Pegatron Corp.
Engineer: Aliens_Hsu
Size A
Project Name IP5NCN/P7NCN DB
Rev A00
Date: Monday, September 07, 2015
Sheet 105 of 108

Landscape Microphone 2 - Right Channel



<Variant Name>

PEGATRON	Title : D-MIC R BOARD.	
Pegatron Corp.	Engineer: Aliens_Hsu	
Size: A	Project Name: IP5NCN/P7NCN DB	Rev: A00
Date: Monday, September 07, 2015	Sheet 106 of 108	



<Variant Name>

PEGATRON Title : POWER BOARD.

Pegatron Corp. Engineer: Aliens_Hsu

Size	Project Name	Rev
B	IP5NCN/P7NCN DB	A00

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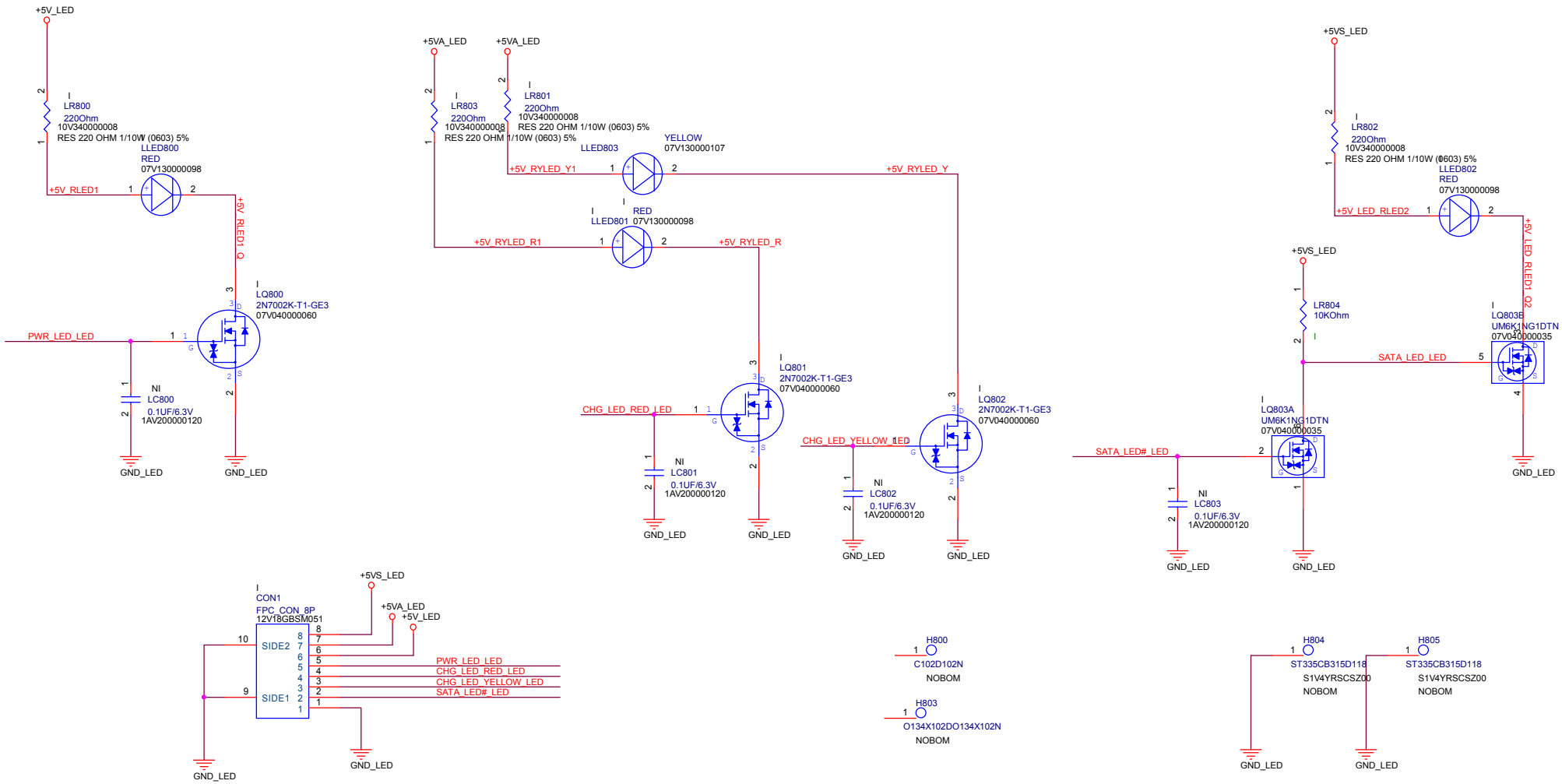

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PEGATRON **Title :** LED BOARD.

Pegatron Corp. **Engineer:** *Aliens_Hsu*

Size	Project Name	Rev
A3	IP5NCN/P7NCN DB	A00

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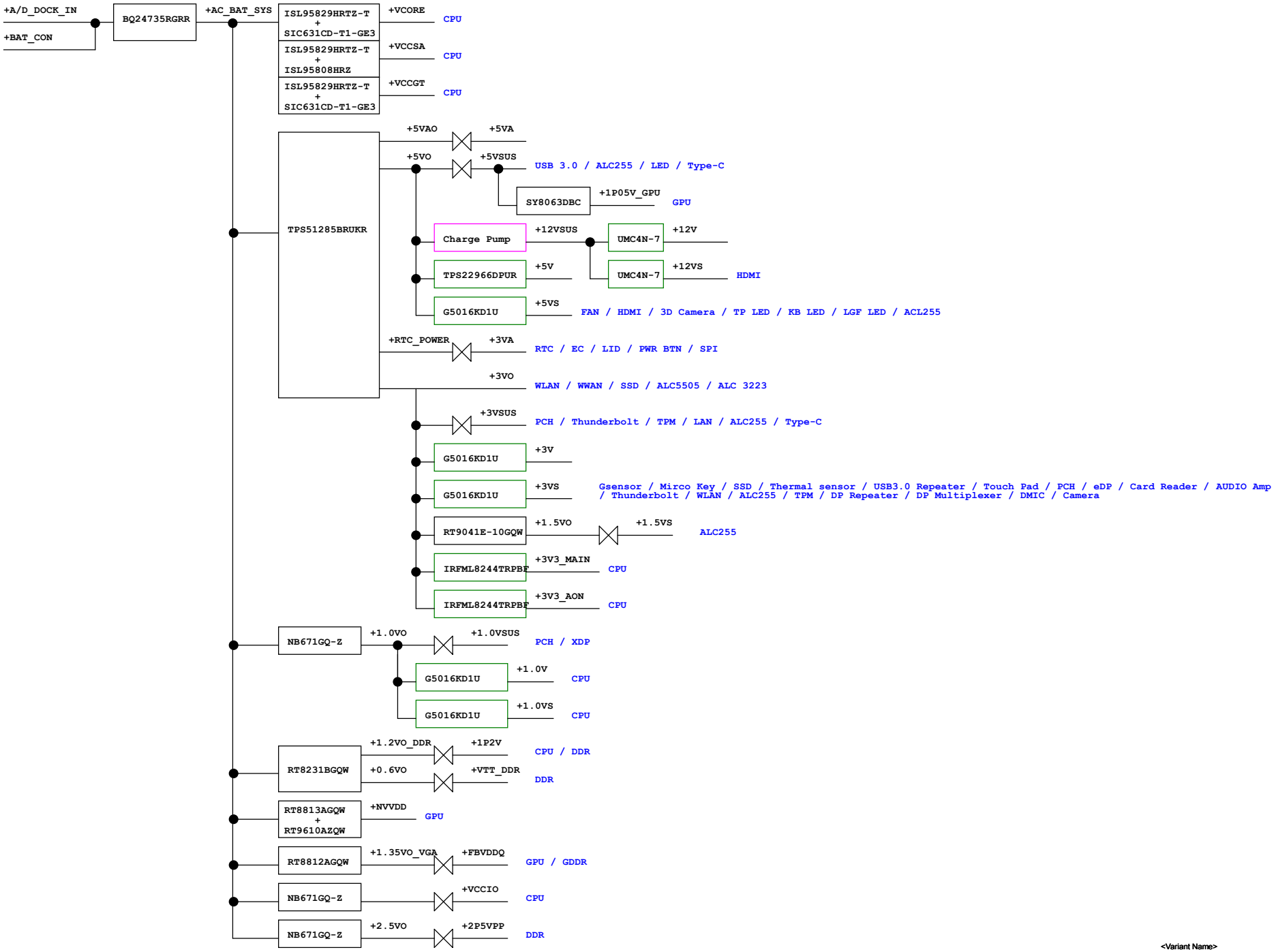

<Variant Name>

PEGATRON

Title : POWER TREE

PEGATRON CORPORATION

Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A00

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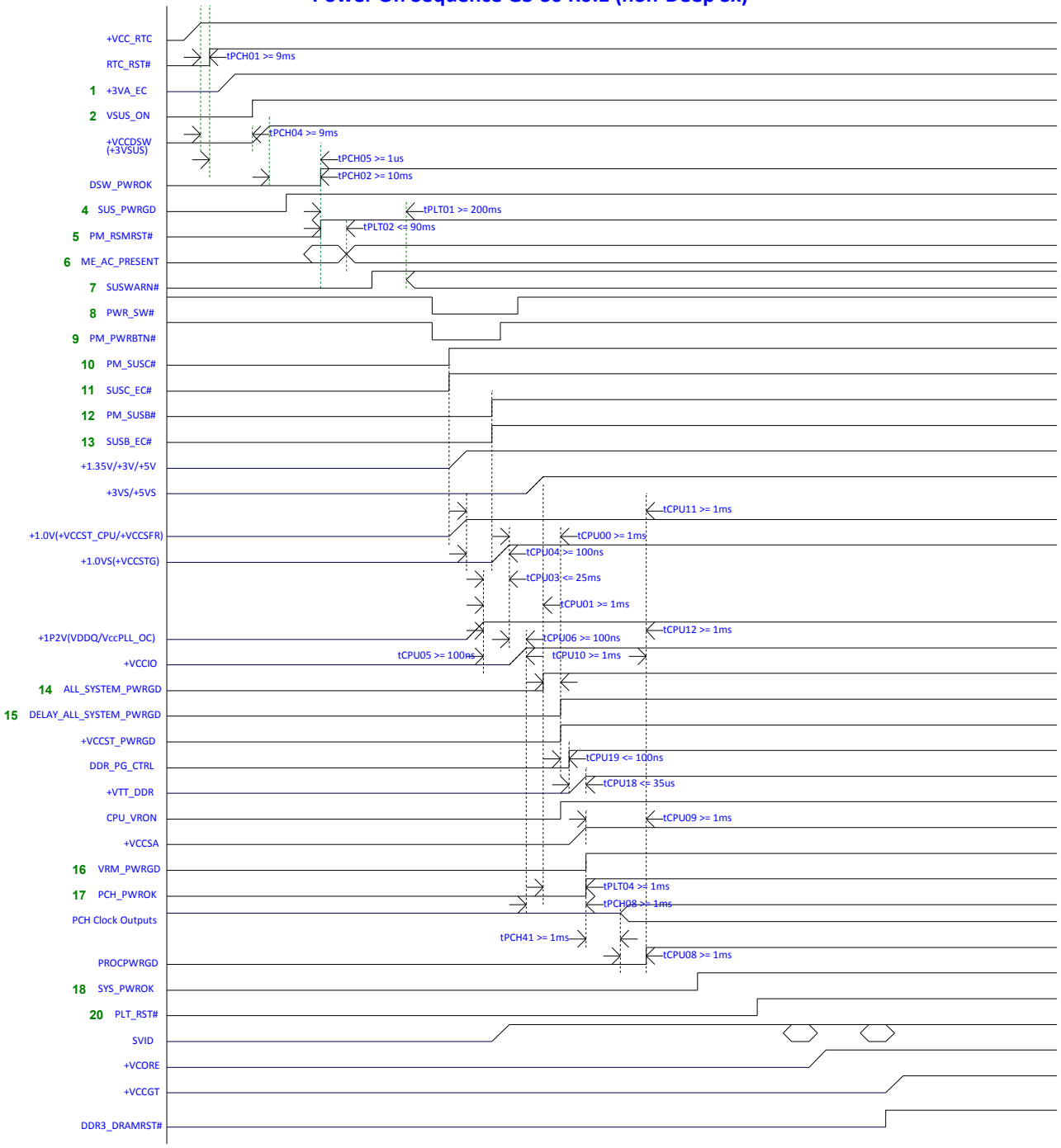
Power On Sequence G3-S0 R0.1 (non-Deep Sx)



<Variant Name>

PEGATRON Title : POWER SEQUENCE Timing

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
C	P5NCN/P7NCN MAIN BOARD	A00

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