Compal Confidential

CFL-H MB Schematic Document

LA-G132P

Rev: 2.0

2018.11.30

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Title: Cover Sheet

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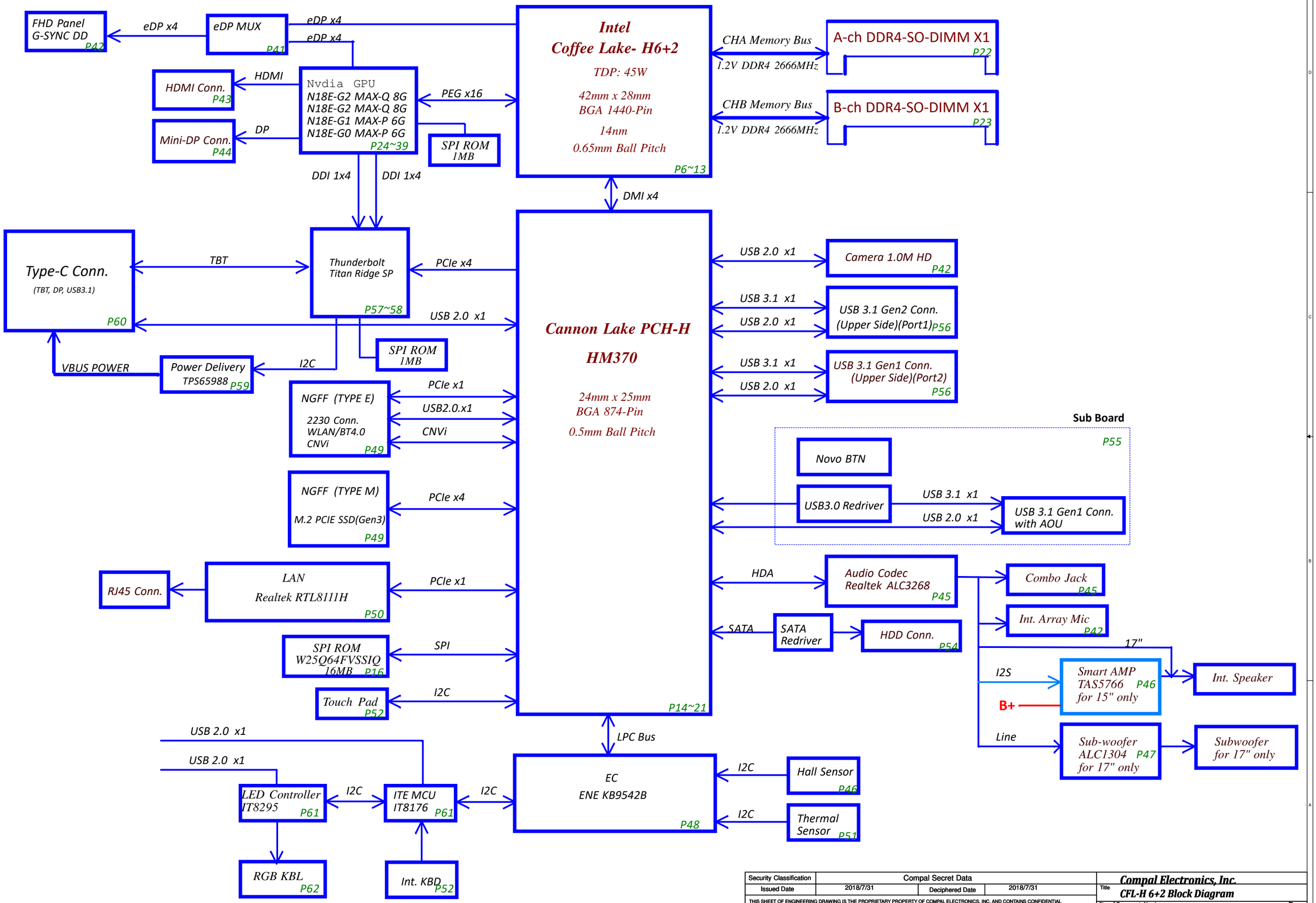
Coffee Lake H Block Diagram



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Title	CFL-H 6+2 Block Diagram		
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	0		0 V	0.300 V	0x00 - 0x13
1 --> 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E
2 --> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3 --> 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4 --> 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5 --> 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6 --> 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7 --> 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8 --> 0.9	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9 --> 1.0	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10 --> 1.1	130K +/- 1%	1.849 V	1.865 V	1.881V	0x88 - 0x96
11 --> 1.2	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12 --> 1.3	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13 --> 1.4	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14 --> 1.5	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15 --> 1.6	330K +/- 1%	2.521 V	2.533V	2.544 V	0xC0 - 0xC9
16 --> 1.7	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17 --> 1.8	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18 --> 1.9	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19 --> 2.0	NC	3.000 V	3.000 V		0xF1 - 0xFF

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	NA		NA
DDI2	NA		NA
DDI3	NA		NA
eDP	Embedded Display		EDP_HPD

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM3	0X52	0XA4	0XA3
PCH_SML0CLK PCH_SML0DATA	+3VS	NA			
PCH_SML1CLK PCH_SML1DATA	+3VS	EC	TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1 EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		TBT	Reserved	TBC	TBC
SMBUS Port2 EC_SMB_CK2 EC_SMB_DA2	+3VS	Current Mon 1	0x41	0x82	0x83
		Current Mon 2	0x40	0x80	0x81
		PCH	TBC		
		GPU	0x9E/0x9F	TBC	TBC
		Smart Amp	0x4C	0x98	0x99
		THERMAL	0x4D	0x9A	0x9B
		USB3.1 re-driver	0x29	0x52	0x53
SMBUS Port4 EC_SMB_CK4 EC_SMB_DA4	+3VS	G-sensor	0x1F	0x3E	0X3F
		Ant i-ghost	TBC		

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3VS				
		EC KB9542	TBC	TBC	TBC
I2C_1_SCL I2C_1_SDA	+3VS	Touch Pad	0x15	TBC	TBC

Voltage Rails

Power Plane	Descript i on	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Bat t ery po wer supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or bat t ery po wer rail f or po wer circ uit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

BOM Structure Table (1/2)

Funct i on	Stuff	Note
Unit SKU	UMA@	
	DIS@	
Project SKU	15@	
	17@	
CFL-H SKU	CPU1@	i5-8300H-R1
	CPU2@	i7-8750H-R1
	CPU3@	i5-8300H
	CPU4@	i7-8750H
	CPU5@	i5-8300H-R3
	CPU6@	i7-8750H-R3
DGPU SKU	N18G0@	
	N18G1@	
	N18G2@	
	N18G3@	
PCH SKU HM370	PCH1@	SR40B-R1
	PCH2@	QNYF
	PCH3@	SR40B-R3
N18 x SKU	GPU1@	2060-G1-R1
	GPU2@	2070-G2-R1
	GPU3@	2080-G3-R1
	GPU4@	2060-G1-R3
	GPU5@	2070-G2-R3
	GPU6@	2080-G3-R3
VRAM 8G	M8G@	X7678038L51
	S8G@	X7678038L52
	H8G@	X7678038L53
VRAM 6G	M8G@	X7678038L56
	S8G@	X7678038L57
	H8G@	X7678038L58
EC		
eSPI I/F	ESPI@	
	LPC@	
Debug	CMC@	
	DCI@	
Panel SKU	GSYNC@	
	NOGSYNC@	
Intel TBT TR	TBT@	
Intel CNVi	CNVI@	
LAN Mode	8111H_SW@	
	8111H_LDO@	
FIN FPC	FIN1@	Y730 FIN
	FIN2@	Y740 FIN
OVRM	ON@	NCP45491
	UPI@	US5650PQKI
ME Connector	ME@	
EMI Components	EMI@	@EMI@
	EMI15@	
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@

HSIO Port Table(PCH) HM370

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1(OTG)	1			**USB3.1 PORT 1**		**Lef t Back**
1	USB3.1_2	2			**USB3.1 PORT 2**		**Right Back**
2	USB3.1_3	3			**USB3.1 PORT 3**		**Right Fornt**
3	USB3.1_4	4					
4	USB3.1_5	5					
5	USB3.1_6	6					
6	USB3.1_7	7					
7	USB3.1_8	8					
8							
9							
10							
11							
12							
13							
14	PCIE_9 / GbE		9				
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0	**HDD**		
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	**LAN**	CLK2 & & CLKREQ#2	
19	PCIE_14 / SATA_1B		14	1	**WLAN+BT NGFF**	CLK3 & & CLKREQ#3	
20	PCIE_15 / SATA_2		15	2			
21	PCIE_16 / SATA_3		16	3			
22	PCIE_17 / SATA_4		17	4	**NGFF SSD**	CLK1 & & CLKREQ#1	Support SATA funct i on on SATA#4
23	PCIE_18 / SATA_5		18	5			
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21		**Thunderbolt Intel Titan Ridge SP**	CLK0 & & CLKREQ#0	
27	PCIE_22		22				
28	PCIE_23		23				
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	**USB3.1 PORT 1**
2	**USB3.1 PORT 2**
3	**USB3.1 PORT 3**
4	**Anti-ghost IT8176**
5	**TBT TYPE-C**
6	**LED Controller IT8295**
7	**Camera**
8	
9	**Tobii**
10	
11	
12	
13	
14	**WLAN+BT NGFF**

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Title: Notes List

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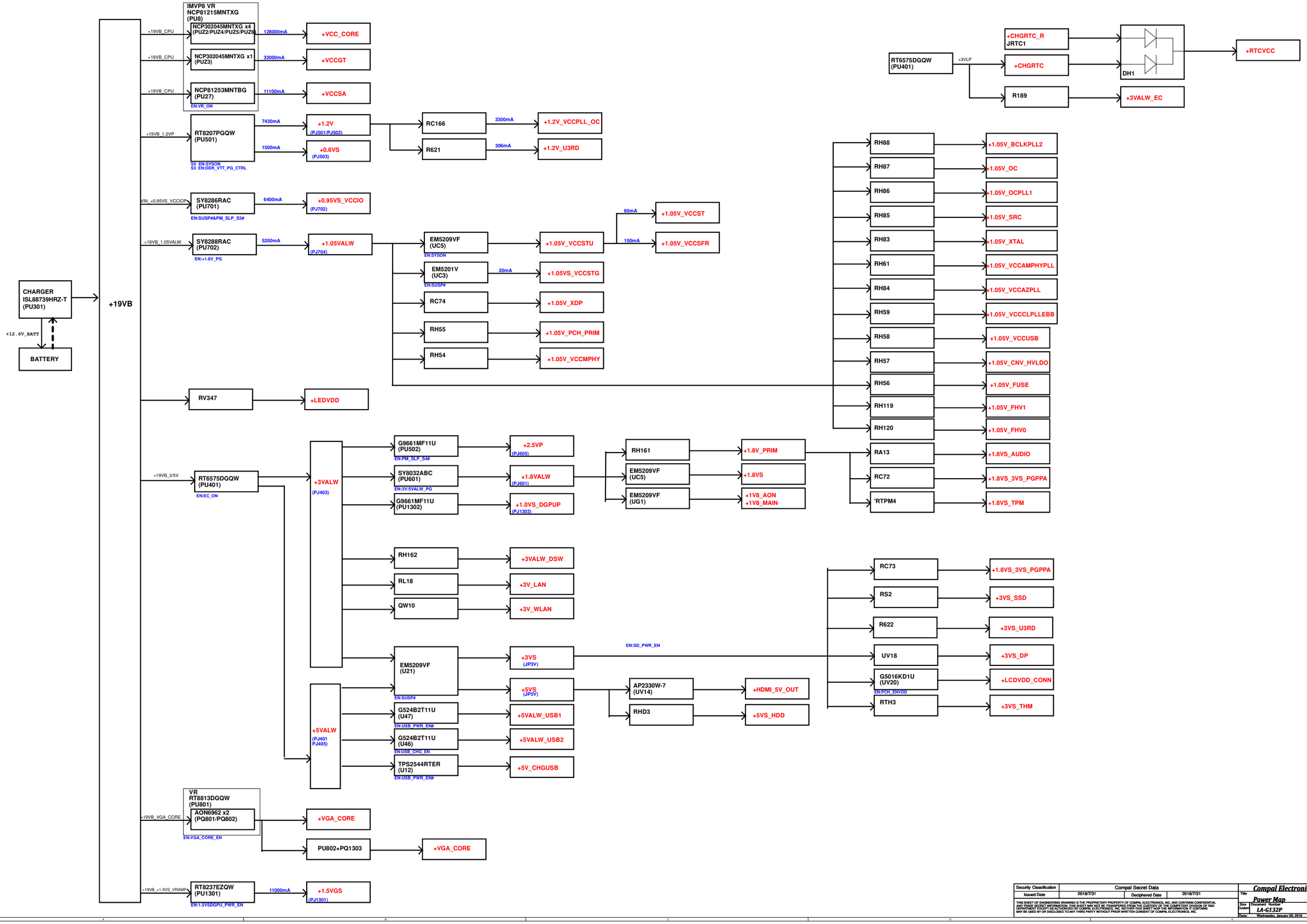

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Title: **Power Map**

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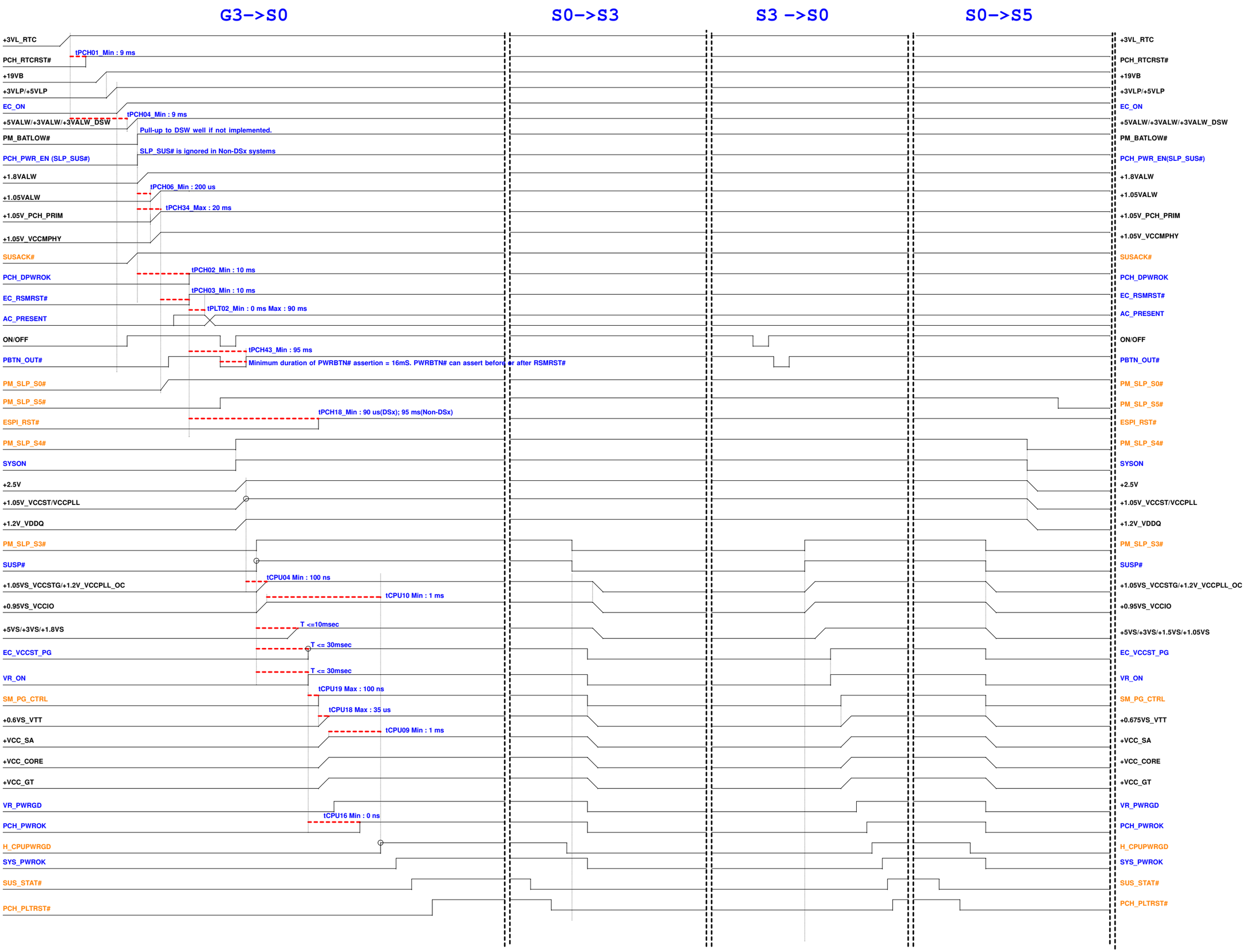
[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



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Title: Power Sequence			
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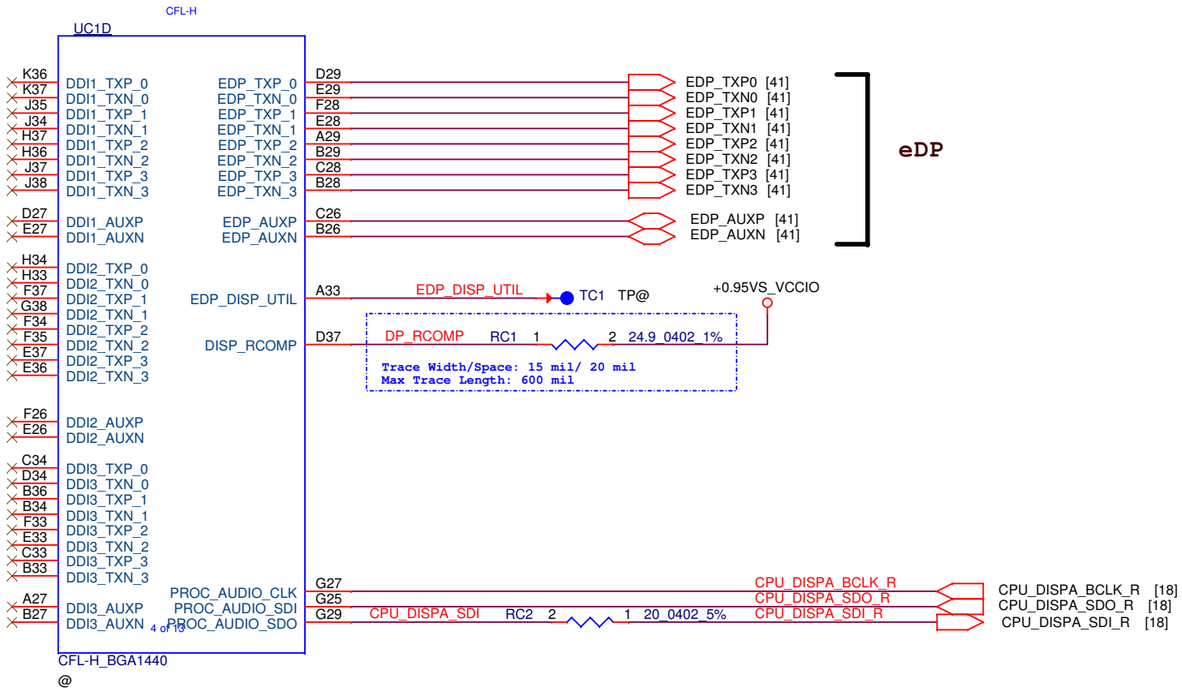

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Title: CFL-H(1/8)DDI/eDP			
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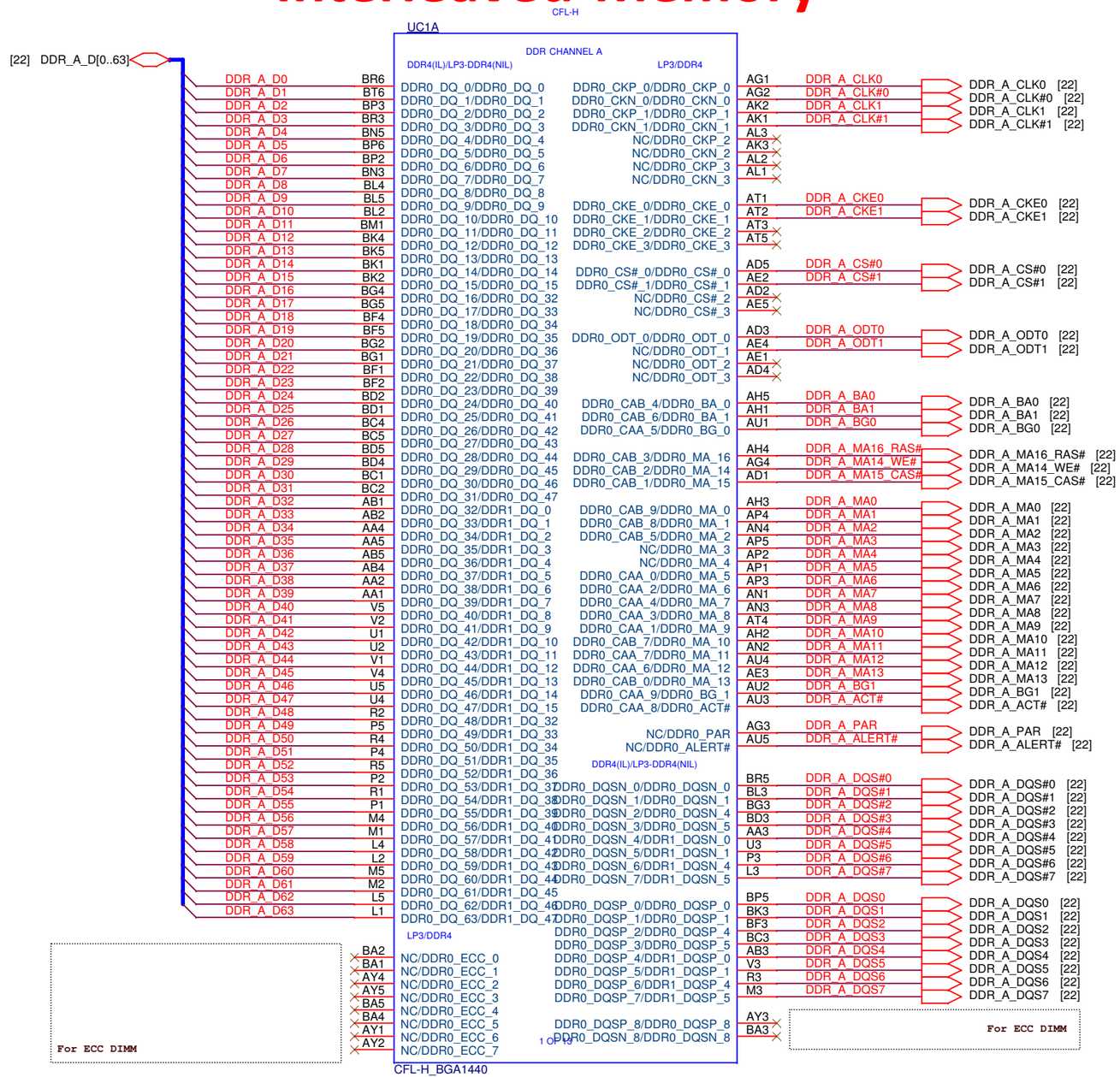
CHANNEL-A

Interleaved Memory



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Compal Electronics, Inc.			
Title	CFL-H(2/8)DIMMA		
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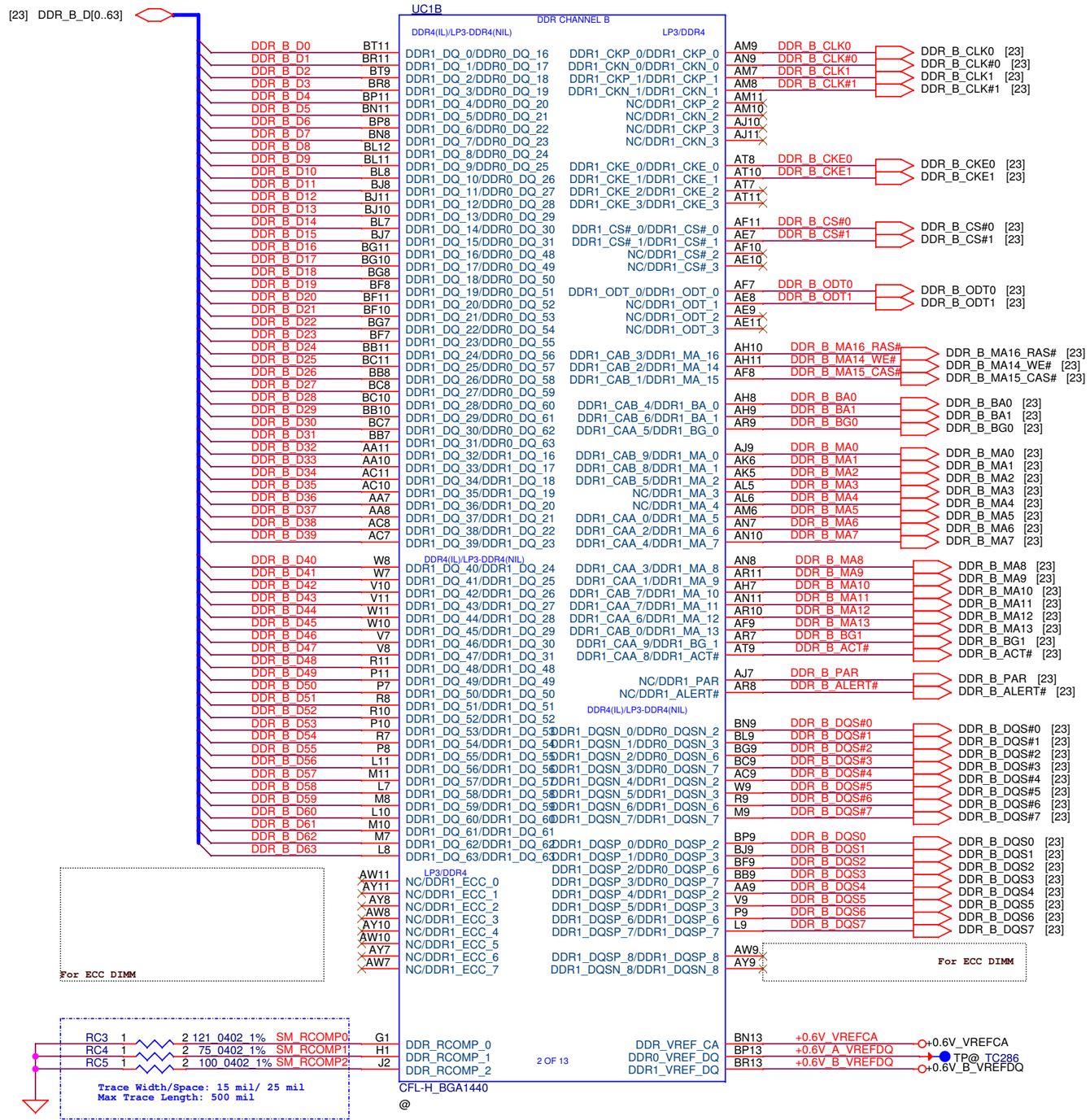
CHANNEL-B

Interleaved Memory



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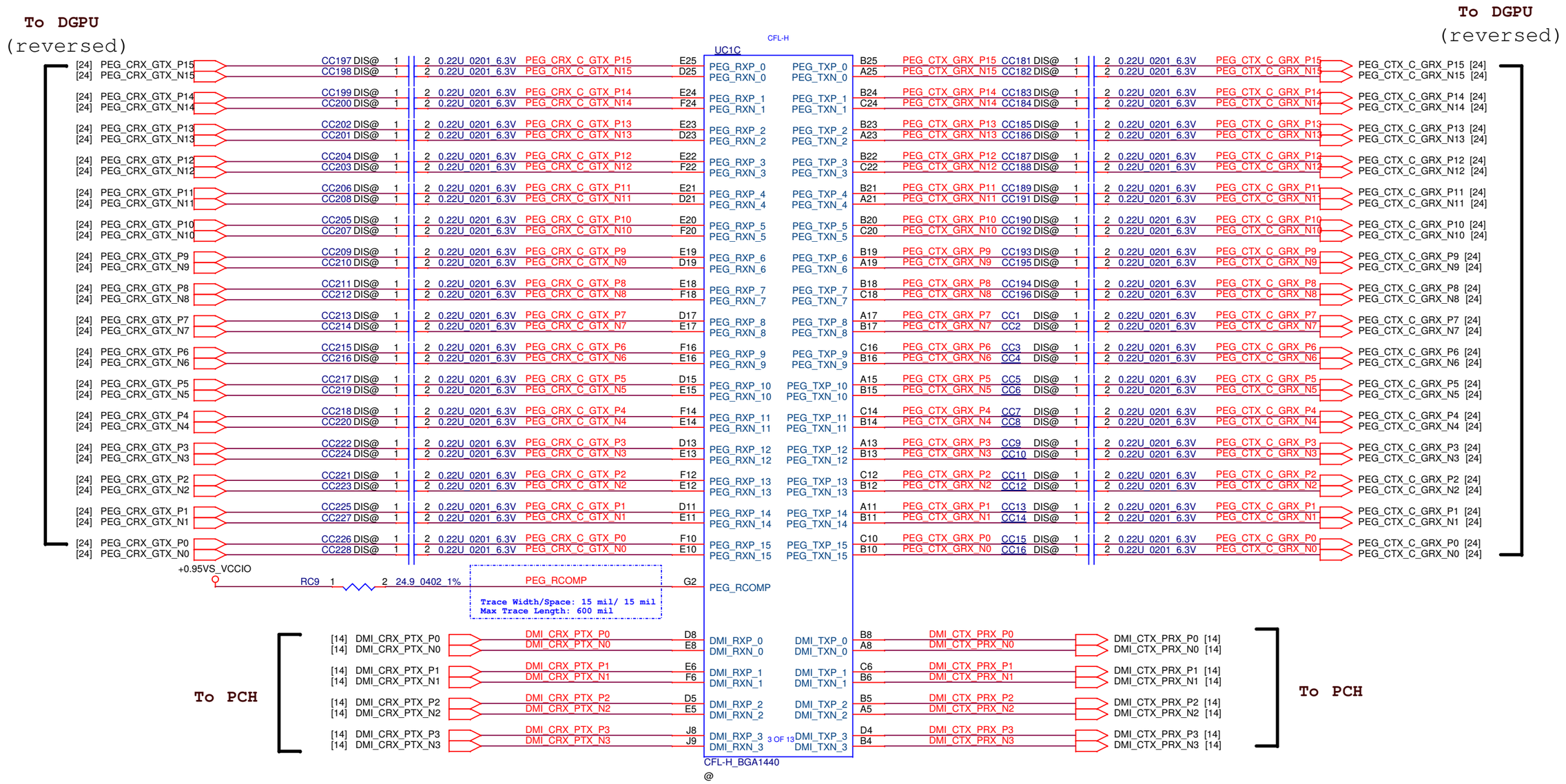
PEG&DMI



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Title: PEG/DMI		
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CFL-H

UC1E

[15] PCH_CPU_BCLK_P — PCH_CPU_BCLK_P — B31 — BCLKP
[15] PCH_CPU_BCLK_N — PCH_CPU_BCLK_N — A32 — BCLKN

[15] PCH_CPU_PCIBCLK_P — PCH_CPU_PCIBCLK_P — D35 — PCI_BCLKP
[15] PCH_CPU_PCIBCLK_N — PCH_CPU_PCIBCLK_N — C36 — PCI_BCLKN

[15] PCH_CPU_24M_CLK_P — PCH_CPU_24M_CLK_P — E31 — CLK24P
[15] PCH_CPU_24M_CLK_N — PCH_CPU_24M_CLK_N — D31 — CLK24N

CPU_SVID_ALERT# — BH31 — VIDALERT#
CPU_SVID_CLK — BH32 — VIDSCK
CPU_SVID_DAT — BH29 — VIDSOUT
Sensitive — H_PROCHOT#_R — BR30 — PROCHOT#

DDR_PG_CTRL — BT13 — DDR_VTT_CNTL

Sensitive — EC_VCCST_PG — H13 — VCCST_PWRGD

[18] H_CPUPWRGD — H_CPUPWRGD — BT31 — PROCPWRGD
[17] H_PLTRST_CPU# — H_PLTRST_CPU# — BP35 — RESET#
[17] H_PM_SYNC_R — H_PM_SYNC_R — BM34 — PM_SYNC
[17] H_PM_DOWN_R — H_PM_DOWN_R — H_PM_DOWN — RC22 1 2 20_0402_5% — BP31 — PM_DOWN
[17,48] H_PECI — BT34 — PECI
[17] PCH_THERMTRIP#_R — H_THERMTRIP# — RC45 1 @ 2 0_0402_5% — J31 — THERMTRIP#

pulled high in PCH side

TP@ TC102 — SKTOCC# — BR33 — SKTOCC#
TP@ TC97 — PROC_SELECT# — BN1 — PROC_SELECT#

TP@ TC96 — CATERR# — BM30 — CATERR#

AT13 — ZVM#
AW13 — MSM#

TP@ TC94 — AU13 — RSVD1
TP@ TC95 — AY13 — RSVD2

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CFL-H_BGA1440

@

CFG_0 — BN25 — CFG0
CFG_1 — BN27
CFG_2 — BN26 — CFG2
CFG_3 — BN28
CFG_4 — BR20 — CFG4
CFG_5 — BM20 — CFG5
CFG_6 — BT20 — CFG6
CFG_7 — BP20 — CFG7
CFG_8 — BR23
CFG_9 — BR22
CFG_10 — BT23
CFG_11 — BT22
CFG_12 — BM19
CFG_13 — BR19
CFG_14 — BP19
CFG_15 — BT19
CFG_17 — BN23
CFG_16 — BP23
CFG_19 — BP22
CFG_18 — BN22

BPM#_0 — BR27 — XDP_BPM#0 — TC98 TP@
BPM#_1 — BT27 — XDP_BPM#1 — TC99 TP@
BPM#_2 — BM31 — XDP_BPM#2 — TC101 TP@
BPM#_3 — BT30 — XDP_BPM#3 — TC100 TP@

PROC_TDO — BT28 — CPU_XDP_TDO — CPU_XDP_TDO [18]
PROC_TDI — BL32 — CPU_XDP_TDI — CPU_XDP_TDI [18]
PROC_TMS — BP28 — CPU_XDP_TMS — CPU_XDP_TMS [18]
PROC_TCK — BR28 — CPU_XDP_TCK0 — CPU_XDP_TCK0 [18]

PROC_TRST# — BP30 — CPU_XDP_TRST#
PROC_PREQ# — BL30 — XDP_PREQ# — XDP_PREQ# [21]
PROC_PRDY# — BP27 — XDP_PRDY# — XDP_PRDY# [21]

CFG_RCOMP — BT25 — CFG_RCOMP 1 RC19 2 49.9_0402_1%

Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

XDP_PREQ# — T37 @
XDP_PRDY# — T394@

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width 0:1:0	0:1:1	0:1:2	CFG Signals CFG [6]	CFG [5]	CFG [2]	Lanes 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

CFG0 — RC31 1 @ 2 1K_0402_5%
CFG2 — RC32 1 2 1K_0402_5%
CFG4 — RC33 1 2 1K_0402_5%
CFG5 — RC36 1 @ 2 1K_0402_5%
CFG6 — RC34 1 @ 2 1K_0402_5%
CFG7 — RC35 1 @ 2 1K_0402_5%

@RF@
10P_0402_50V8J2 — CC155 — CPU_SVID_CLK
03/14 From RF Team Request

ESD@
100P_0402_50V8J1 — CC156 — VCCST_PWRGD
ESD@
100P_0402_50V8J1 — CC157 — H_CPUPWRGD
Near CPU side
From ESD Team Request

+1.05V_VCCST — RC20 1K_0402_5% — VCCST_PWRGD
[48] VCCST_PWRGD — VCCST_PWRGD — RC2521 2 60.4_0402_1% — EC_VCCST_PG

+1.05VS_VCCSTG — RC18 1K_0402_5% — H_PROCHOT#
[48] H_PROCHOT# — H_PROCHOT# — RC42 2 1 499_0402_1% — H_PROCHOT#_R

TMS/TDI pin CPU on-die termination

Place to PCH side

+1.05VS_VCCSTG
CPU_XDP_TMS — 51_0402_5% 1 CMC@ 2 — RC255
CPU_XDP_TDI — 51_0402_5% 1 CMC@ 2 — RC254
CPU_XDP_TDO — 100_0402_1% 2 DCI@ 1 — RC253

Place to CPU side

CPU_XDP_TCK0 — 51_0402_5% 1 DCI@ 2 — RC256

If need debug with INTEL. this cmc@ need pop

CPU_XDP_TRST# — R387 1 @ 2 0_0402_5% — PCH_XDP_TRST# [21]

SVID ALERT

+1.05V_VCCST — RC40 56_0402_1%
[70] VR_SVID_ALERT# — RC39 1 2 220_0402_5% — CPU_SVID_ALERT#

SVID DATA

+1.05V_VCCST — RC41 100_0402_5%
[70] VR_SVID_SDIO — RC38 1 @ 2 0_0402_5% — CPU_SVID_DAT

SVID CLK

[70] VR_SVID_SCLK — RC37 1 @ 2 0_0402_5% — CPU_SVID_CLK

571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

+1.2V — CC41 0.1U_0201_10V6K — UC2 VCC
+3VS — RC43 100K_0402_5%
DDR_PG_CTRL — UC2 A
UC2 NC
UC2 GND
UC2 Y — DDR_VTT_PG_CTRL
74AUP1G07GW_TSSOP5
DDR_VTT_PG_CTRL [67]

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.
Title: CFL-H(5/8)CFG,SVID
Size: Custom | Document Number: LA-G132P | Rev: 1.0
Date: Wednesday, January 09, 2019 | Sheet 10 of 81

GT
32000mA(Hexa Core GT2)

+VCCGT

CFL-H

UC1K

AT14	VCCGT1	VCCGT80	BD35
AT31	VCCGT2	VCCGT81	BD36
AT32	VCCGT3	VCCGT82	BE31
AT33	VCCGT4	VCCGT83	BE32
AT34	VCCGT5	VCCGT84	BE33
AT35	VCCGT6	VCCGT85	BE34
AT36	VCCGT7	VCCGT86	BE35
AT37	VCCGT8	VCCGT87	BE36
AT38	VCCGT9	VCCGT88	BE37
AU14	VCCGT10	VCCGT89	BE38
AU29	VCCGT11	VCCGT90	BF13
AU30	VCCGT12	VCCGT91	BF14
AU31	VCCGT13	VCCGT92	BF29
AU32	VCCGT14	VCCGT93	BF30
AU35	VCCGT15	VCCGT94	BF31
AU36	VCCGT16	VCCGT95	BF32
AU37	VCCGT17	VCCGT96	BF35
AU38	VCCGT18	VCCGT97	BF36
AV29	VCCGT19	VCCGT98	BF37
AV30	VCCGT20	VCCGT99	BF38
AV31	VCCGT21	VCCGT100	BG29
AV32	VCCGT22	VCCGT101	BG30
AV33	VCCGT23	VCCGT102	BG31
AV34	VCCGT24	VCCGT103	BG32
AV35	VCCGT25	VCCGT104	BG33
AV36	VCCGT26	VCCGT105	BG34
AW14	VCCGT27	VCCGT106	BG35
AW31	VCCGT28	VCCGT107	BG36
AW32	VCCGT29	VCCGT108	BH33
AW33	VCCGT30	VCCGT109	BH34
AW34	VCCGT31	VCCGT110	BH35
AW35	VCCGT32	VCCGT111	BH36
AW36	VCCGT33	VCCGT112	BH37
AW37	VCCGT34	VCCGT113	BH38
AW38	VCCGT35	VCCGT114	BJ16
AY29	VCCGT36	VCCGT115	BJ17
AY30	VCCGT37	VCCGT116	BJ19
AY31	VCCGT38	VCCGT117	BJ20
AY32	VCCGT39	VCCGT118	BJ21
AY35	VCCGT40	VCCGT119	BJ23
AY36	VCCGT41	VCCGT120	BJ24
AY37	VCCGT42	VCCGT121	BJ26
AY38	VCCGT43	VCCGT122	BJ27
BA13	VCCGT44	VCCGT123	BJ37
BA14	VCCGT45	VCCGT124	BJ38
BA29	VCCGT46	VCCGT125	BK16
BA30	VCCGT47	VCCGT126	BK17
BA31	VCCGT48	VCCGT127	BK19
BA32	VCCGT49	VCCGT128	BK20
BA33	VCCGT50	VCCGT129	BK21
BA34	VCCGT51	VCCGT130	BK23
BA35	VCCGT52	VCCGT131	BK24
BA36	VCCGT53	VCCGT132	BK26
BB13	VCCGT54	VCCGT133	BK27
BB14	VCCGT55	VCCGT134	BL15
BB31	VCCGT56	VCCGT135	BL16
BB32	VCCGT57	VCCGT136	BL17
BB33	VCCGT58	VCCGT137	BL23
BB34	VCCGT59	VCCGT138	BL24
BB35	VCCGT60	VCCGT139	BL25
BB36	VCCGT61	VCCGT140	BL26
BB37	VCCGT62	VCCGT141	BL27
BB38	VCCGT63	VCCGT142	BL28
BC29	VCCGT64	VCCGT143	BL36
BC30	VCCGT65	VCCGT144	BL37
BC31	VCCGT66	VCCGT145	BM15
BC32	VCCGT67	VCCGT146	BM16
BC35	VCCGT68	VCCGT147	BM17
BC36	VCCGT69	VCCGT148	BM36
BC37	VCCGT70	VCCGT149	BM37
BC38	VCCGT71	VCCGT150	BN15
BD13	VCCGT72	VCCGT151	BN16
BD14	VCCGT73	VCCGT152	BN17
BD29	VCCGT74	VCCGT153	BN36
BD30	VCCGT75	VCCGT154	BN37
BD31	VCCGT76	VCCGT155	BN38
BD32	VCCGT77	VCCGT156	BP15
BD33	VCCGT78	VCCGT157	BP16
BD34	VCCGT79	VCCGT158	BP17
BP37	VCCGT159	VCCGT164	BR37
BP38	VCCGT160	VCCGT165	BT15
BR15	VCCGT161	VCCGT166	BT16
BR16	VCCGT162	VCCGT167	BT17
BR17	VCCGT163	VCCGT168	BT37

11 OF 13 VSSGT_SENSE AH37
VCCGT_SENSE AH38

CFL-H_BGA1440
@

+VCCGT
RC12 2 1 100_0402_1%
VSSGT_SENSE [70]
VCCGT_SENSE [70]
RC13 1 2 100_0402_1%

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

+VCCCORE

CFL-H

UC1I

AA13	VCC1	VCC64	AH13
AA31	VCC2	VCC65	AH14
AA32	VCC3	VCC66	AH29
AA33	VCC4	VCC67	AH30
AA34	VCC5	VCC68	AH31
AA35	VCC6	VCC69	AH32
AA36	VCC7	VCC70	AJ14
AA37	VCC8	VCC71	AJ29
AA38	VCC9	VCC72	AJ30
AB29	VCC10	VCC73	AJ31
AB30	VCC11	VCC74	AJ32
AB31	VCC12	VCC75	AJ33
AB32	VCC13	VCC76	AJ34
AB35	VCC14	VCC77	AJ35
AB36	VCC15	VCC78	AJ36
AB37	VCC16	VCC79	AK31
AB38	VCC17	VCC80	AK32
AC13	VCC18	VCC81	AK33
AC14	VCC19	VCC82	AK34
AC29	VCC20	VCC83	AK35
AC30	VCC21	VCC84	AK36
AC31	VCC22	VCC85	AK37
AC32	VCC23	VCC86	AK38
AC33	VCC24	VCC87	AL13
AC34	VCC25	VCC88	AL29
AC35	VCC26	VCC89	AL30
AC36	VCC27	VCC90	AL31
AD13	VCC28	VCC91	AL32
AD14	VCC29	VCC92	AL35
AD31	VCC30	VCC93	AL36
AD32	VCC31	VCC94	AL37
AD33	VCC32	VCC95	AL38
AD34	VCC33	VCC96	AM13
AD35	VCC34	VCC97	AM14
AD36	VCC35	VCC98	AM29
AD37	VCC36	VCC99	AM30
AD38	VCC37	VCC100	AM31
AE13	VCC38	VCC101	AM32
AE14	VCC39	VCC102	AM33
AE30	VCC40	VCC103	AM34
AE31	VCC41	VCC104	AM35
AE32	VCC42	VCC105	AM36
AE35	VCC43	VCC106	AN13
AE36	VCC44	VCC107	AN14
AE37	VCC45	VCC108	AN31
AE38	VCC46	VCC109	AN32
AF29	VCC47	VCC110	AN33
AF30	VCC48	VCC111	AN34
AF31	VCC49	VCC112	AN35
AF32	VCC50	VCC113	AN36
AF33	VCC51	VCC114	AN37
AF34	VCC52	VCC115	AN38
AF35	VCC53	VCC116	AP13
AF36	VCC54	VCC117	AP30
AF37	VCC55	VCC118	AP31
AF38	VCC56	VCC119	AP32
AG14	VCC57	VCC120	AP35
AG31	VCC58	VCC121	AP36
AG32	VCC59	VCC122	AP37
AG33	VCC60	VCC123	AP38
AG34	VCC61	VCC124	K13
AG35	VCC62		
AG36	VCC63		

9 OF 13 VCC_SENSE AG37
VSS_SENSE AG38

CFL-H_BGA1440
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128000mA(Hexa Core GT2)

+VCCCORE
RC10 2 1 100_0402_1%
VCCCORE_SENSE [70]
VSSCORE_SENSE [70]
RC11 1 2 100_0402_1%

1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU

+VCCCORE

CFL-H

UC1J

K14	VCC1	VCC64	W35
L13	VCC2	VCC65	W36
L14	VCC3	VCC66	W37
N13	VCC4	VCC67	W38
N14	VCC5	VCC68	Y29
N30	VCC6	VCC69	Y30
N31	VCC7	VCC70	Y31
N32	VCC8	VCC71	Y32
N35	VCC9	VCC72	Y33
N36	VCC10	VCC73	Y34
N37	VCC11	VCC74	Y35
N38	VCC12	VCC75	Y36
P13	VCC13		
P14	VCC14		
P29	VCC15		
P30	VCC16		
P31	VCC17		
P32	VCC18		
P33	VCC19		
P34	VCC20		
P35	VCC21		
P36	VCC22		
R13	VCC23		
R31	VCC24		
R32	VCC25		
R33	VCC26		
R34	VCC27		
R35	VCC28		
R36	VCC29		
R37	VCC30		
R38	VCC31		
T29	VCC32		
T30	VCC33		
T31	VCC34		
T32	VCC35		
T35	VCC36		
T36	VCC37		
T37	VCC38		
T38	VCC39		
U29	VCC40		
U30	VCC41		
U31	VCC42		
U32	VCC43		
U33	VCC44		
U34	VCC45		
U35	VCC46		
U36	VCC47		
V13	VCC48		
V14	VCC49		
V31	VCC50		
V32	VCC51		
V33	VCC52		
V34	VCC53		
V35	VCC54		
V36	VCC55		
V37	VCC56		
V38	VCC57		
W13	VCC58		
W14	VCC59		
W29	VCC60		
W30	VCC61		
W31	VCC62		
W32	VCC63		

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CFL-H_BGA1440
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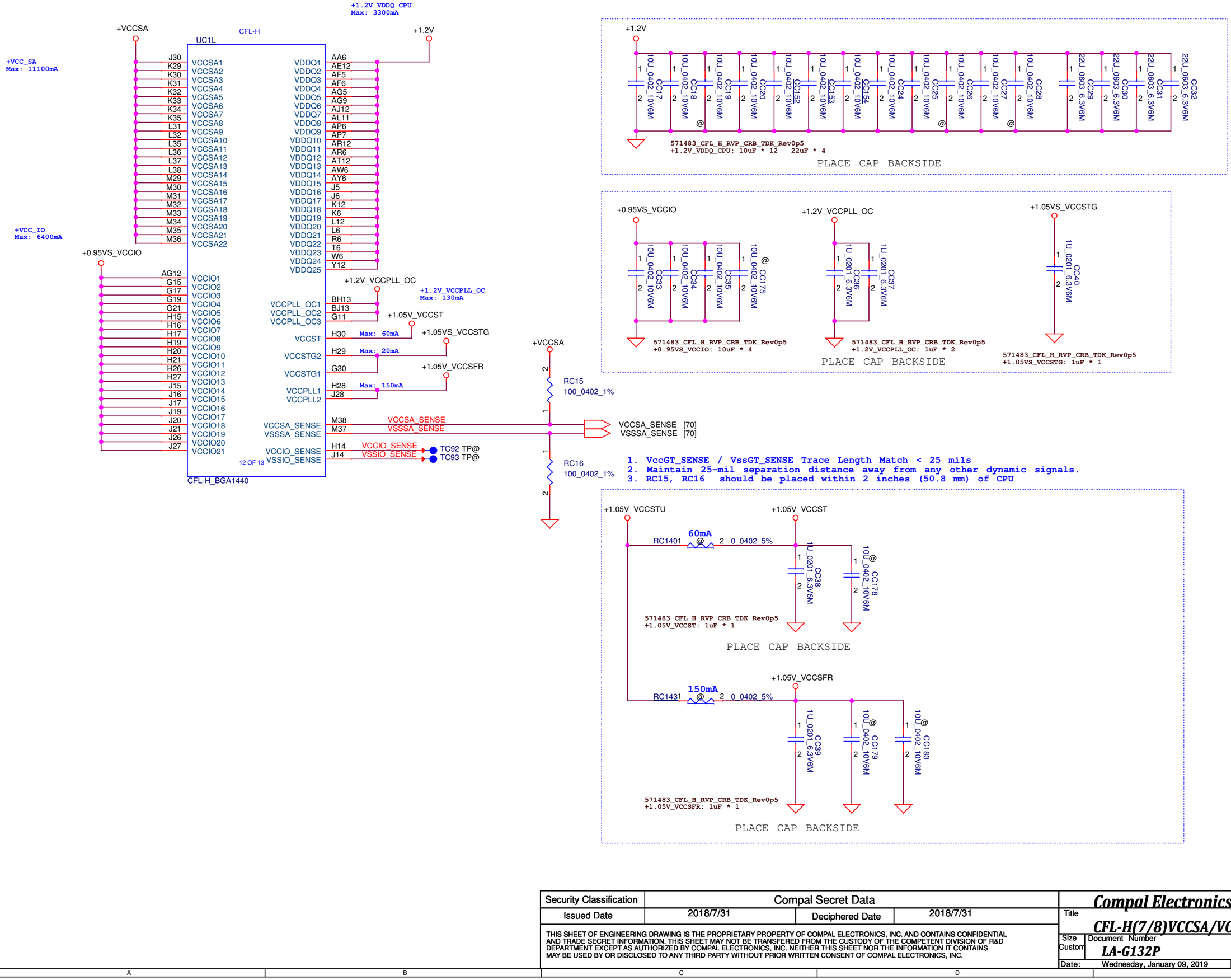
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: CFL-H(6/8)VCC CORE/GT

Size	Document Number	Rev
Custom	LA-G132P	1.0

Date: Wednesday, January 09, 2019 Sheet 11 of 81



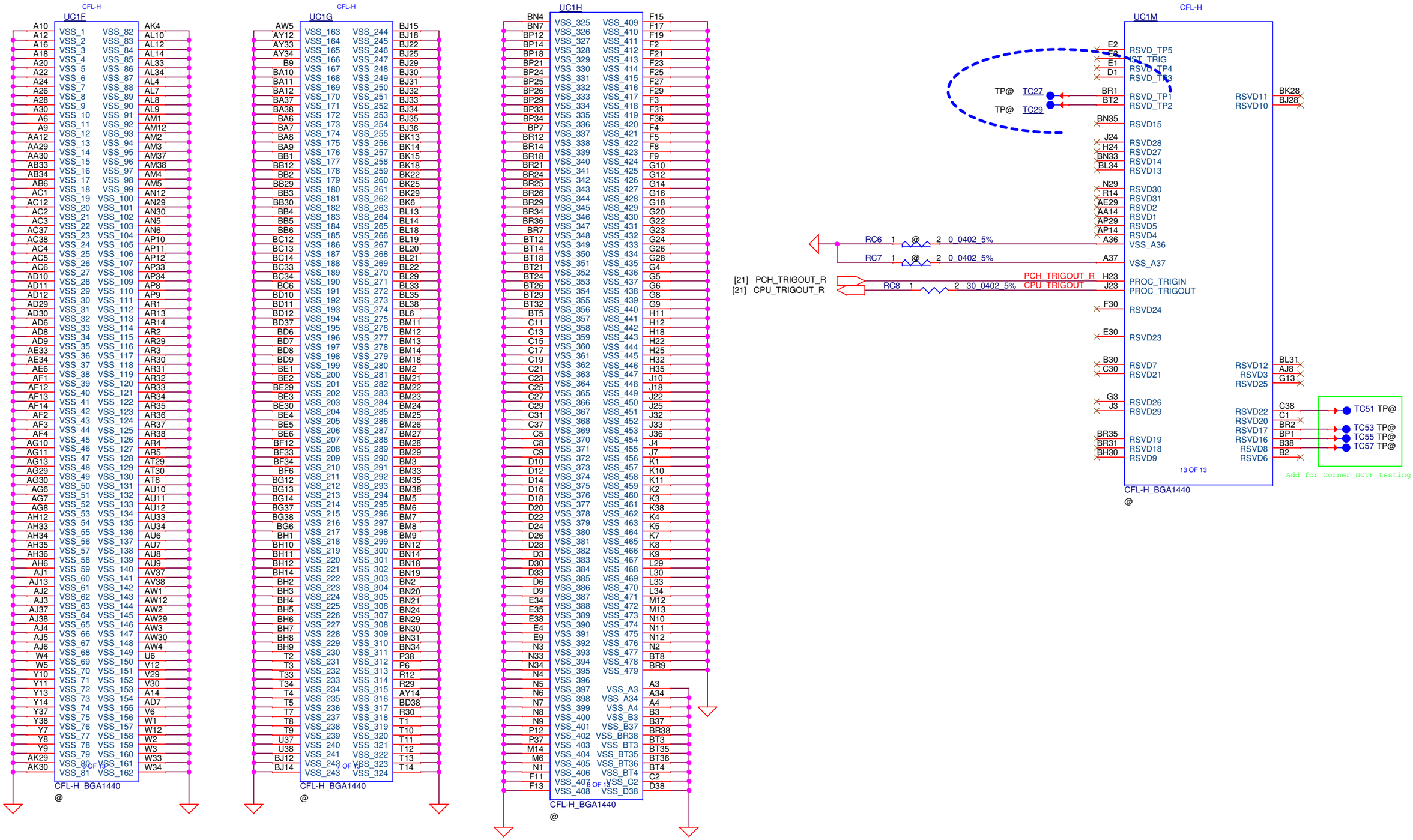
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

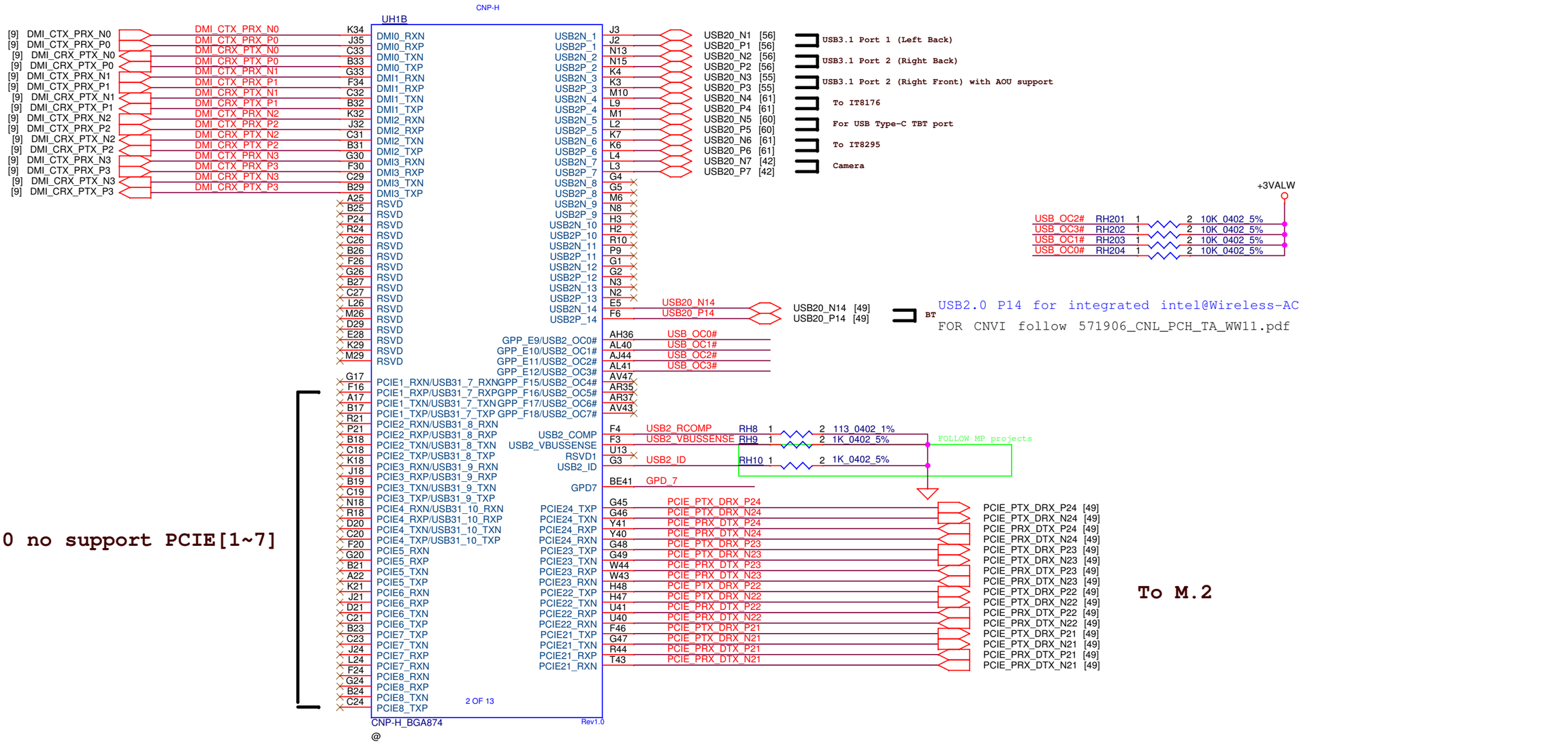
Size	Document Number	Rev
Custom	LA-G132P	1.0

Date: Wednesday, January 09, 2019 Sheet 12 of 81



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

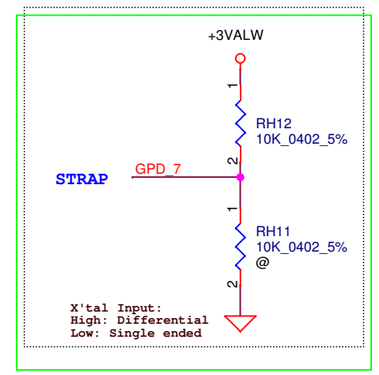
Compal Electronics, Inc.			
Title	CFL-H(8/8)GND/RSVD		
Size: Custom	Document Number: LA-G132P		Rev: 1.0
Date: Wednesday, January 09, 2019	Sheet 13 of 81		



Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7 / PCIe* #1	USB3.1 #8 / PCIe* #2	USB3.1 #9 / PCIe* #3	USB3.1 #10 / PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11 / SATA 0a	PCIe* #12 / SATA 1a	PCIe* #13 / SATA 0b	PCIe* #14 / SATA 1b	PCIe* #15 / SATA 2	PCIe* #16 / SATA 3	PCIe* #17 / SATA 4	PCIe* #18 / SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
											GbE				GbE		GbE	GbE	GbE											
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
XA maximum of 16 PCIe* Ports (or devices) can be enabled
E When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
X PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
X A maximum of 6 SATA Ports (or devices) can be enabled
X SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
X SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
X A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
X A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
X x2 and x4 PCIe* NVMe SSD
X x2 IntelR Optane? Memory Device
X See the PCI Express* (PCIe*) chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



check its function

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title	PCH(1/8)DMI/PCIE/USB2		
Size: Custom	Document Number: LA-G132P		Rev: 1.0
Date: Wednesday, January 09, 2019	Sheet 14 of 81		

PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT RH17 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_OUT_R
XTAL_24M_PCH_IN RH18 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_IN_R

RH16 1 2 1M_0402_5%
24MHZ_18PF_XRCGB24M000F2P51R0
YH1 SJ10000TP00
NC NC
TXC SJ10000UJ00
Murata SJ10000UJ00
27P_0402_50V8J CH4
27P_0402_50V8J CH5

RH20 1 2 60.4_0402_1% XCLK_BIASREF
XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

PCH_RTCX1
PCH_RTCX2
RH19 1 2 10M_0402_5%
YH2
32.768KHZ_9PF_X1A000141000200
EPSON SJ10000PW00
TXC SJ10000Q400
10P_0402_50V8J CH6
10P_0402_50V8J CH7
Trace Space: 15 mil
Max Trace Length: 1000 mil

+3VS
RH205 1 2 10K_0402_5% TBT_CLKREQ0#
RH206 1 2 10K_0402_5% SSD_CLKREQ1#
RH207 1 2 10K_0402_5% LAN_CLKREQ2#
RH208 1 2 10K_0402_5% WLAN_CLKREQ3#
RH189 2 DIS@ 1 GPU_CLKREQ4# 10K_0402_5%

For DDX03 R02

+1.8V_PRIM
XTAL Frequency Select
RH26 1 2 4.7K_0402_5% CNV_BRI_PTX_DRX STRAP
This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+1.8V_PRIM
VCCPSPI Select
RH93 1 @ 2 4.7K_0402_5% GPP_J9 STRAP
The signal has a weak internal pull-down 20K
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a 1 for the proper functionality of the SPI (Flash) I/Os

+1.8V_PRIM
M.2 CNV Mode Select
RH167 2 1 10K_0402_5% CNV_RGI_PTX_DRX STRAP
RH168 2 @ 1 10K_0402_5%
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

CNP-H
UH1G
CNP-H_BGA874
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Rev1.0
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TH74 TP@
BE33 GPP_A16/CLKOUT_48

[10] PCH_CPU_24M_CLK_P D7 CLKOUT_CPUNSSC_P
[10] PCH_CPU_24M_CLK_N C6 CLKOUT_CPUNSSC#
CLKOUT_ITPXDP# Y3 TP@ TH73
CLKOUT_ITPXDP_P Y4 TP@ TH72

[10] PCH_CPU_BCLK_P B8 CLKOUT_CPUBCLK_P CLKOUT_CPUPCIBCLK#
[10] PCH_CPU_BCLK_N C8 CLKOUT_CPUBCLK# CLKOUT_CPUPCIBCLK_P
B6 PCH_CPU_PCIBCLK_N → PCH_CPU_PCIBCLK_N [10]
A6 PCH_CPU_PCIBCLK_P → PCH_CPU_PCIBCLK_P [10]

XTAL_24M_PCH_OUT_R U9 XTAL_OUT
XTAL_24M_PCH_IN_R U10 XTAL_IN
CLKOUT_PCIE_N0 AJ6 → CLK_PCIE_N0 [57]
CLKOUT_PCIE_P0 AJ7 → CLK_PCIE_P0 [57] Thunderbolt

XCLK_BIASREF T3
CLKOUT_PCIE_N1 AH9 → CLK_PCIE_N1 [49]
CLKOUT_PCIE_P1 AH10 → CLK_PCIE_P1 [49] NGFF SSD

PCH_RTCX1 BA49 RTCX1
PCH_RTCX2 BA48 RTCX2
CLKOUT_PCIE_N2 AE14 → CLK_PCIE_N2 [50]
CLKOUT_PCIE_P2 AE15 → CLK_PCIE_P2 [50] LAN

[57] TBT_CLKREQ0# BF31 GPP_B5/SRCCLKREQ0#
[49] SSD_CLKREQ1# BE31 GPP_B6/SRCCLKREQ1#
[50] LAN_CLKREQ2# AR32 GPP_B7/SRCCLKREQ2#
[49] WLAN_CLKREQ3# BB30 GPP_B8/SRCCLKREQ3#
[24] GPU_CLKREQ4# BA30 GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N3 AE6 → CLK_PCIE_N3 [49]
CLKOUT_PCIE_P3 AE7 → CLK_PCIE_P3 [49] WLAN

AN29 GPP_B10/SRCCLKREQ5#
CLKOUT_PCIE_N4 AC2 → CLK_PEG_N4 [24]
CLKOUT_PCIE_P4 AC3 → CLK_PEG_P4 [24] GPU

AE47 GPP_H0/SRCCLKREQ6#
AC48 GPP_H1/SRCCLKREQ7#
AE41 GPP_H2/SRCCLKREQ8#
CLKOUT_PCIE_N5 AB2
CLKOUT_PCIE_P5 AB3

AF48 GPP_H3/SRCCLKREQ9#
AC41 GPP_H4/SRCCLKREQ10#
AC39 GPP_H5/SRCCLKREQ11#
CLKOUT_PCIE_N6 W4
CLKOUT_PCIE_P6 W3

AE39 GPP_H6/SRCCLKREQ12#
AB48 GPP_H7/SRCCLKREQ13#
AC44 GPP_H8/SRCCLKREQ14#
CLKOUT_PCIE_N7 W7
CLKOUT_PCIE_P7 W6

AC43 GPP_H9/SRCCLKREQ15#
CLKOUT_PCIE_N8 AC14
CLKOUT_PCIE_P8 AC15

V2 CLKOUT_PCIE_N15
V3 CLKOUT_PCIE_P15
CLKOUT_PCIE_N9 U2
CLKOUT_PCIE_P9 U3

T2 CLKOUT_PCIE_N14
T1 CLKOUT_PCIE_P14
CLKOUT_PCIE_N10 AC9
CLKOUT_PCIE_P10 AC11

AA1 CLKOUT_PCIE_N13
Y2 CLKOUT_PCIE_P13
CLKOUT_PCIE_N11 AE9
CLKOUT_PCIE_P11 AE11

AC7 CLKOUT_PCIE_N12
AC6 CLKOUT_PCIE_P12
CLKIN_XTAL R6 → REFCLK_CNV [49] 1V@38.4MHZ

RH173 10K_0402_5%

CNP-H
UH1M
CNP-H_BGA874
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Rev1.0
13 OF 13

AW13 GPP_G0/SD_CMD
BE9 GPP_G1/SD_DATA0
BF8 GPP_G2/SD_DATA1
BF9 GPP_G3/SD_DATA2
BG8 GPP_G4/SD_DATA3
BE8 GPP_G5/SD_CD#
BD8 GPP_G6/SD_CLK
AV13 GPP_G7/SD_WP

AP3 GPP_I11/M2_SKT2_CFG0
AP2 GPP_I12/M2_SKT2_CFG1
AN4 GPP_I13/M2_SKT2_CFG2
AM7 GPP_I14/M2_SKT2_CFG3
3.3V

AV6 GPP_J0/CNV_PA_BLANKING
AY3 GPP_J1/CPU_C10_GATE#
AR13 GPP_J11/A4WP_PRESENT
AV7 GPP_J10
AW3 GPP_J_2
AT10 GPP_J_3
1.8V

[49] CNV_BRI_PTX_DRX CNV_BRI_PTX_DRX AV4 GPP_J4/CNV_BRI_DT/UART0B_RTS#
[49] CNV_BRI_PRX_DTX CNV_BRI_PRX_DTX AY2 GPP_J5/CNV_BRI_RSP/UART0B_RXD
[49] CNV_RGI_PTX_DRX CNV_RGI_PTX_DRX BA4 GPP_J6/CNV_RGI_DT/UART0B_TXD
[49] CNV_RGI_PRX_DTX CNV_RGI_PRX_DTX AV3 GPP_J7/CNV_RGI_RSP/UART0B_CTS#
AW2 GPP_J8/CNV_MFUART2_RXD
VCCPSPI Select GPP_J9 AU9 GPP_J9/CNV_MFUART2_TXD

CNV_WR_CLKN BD4 CLK_CNV_PRX_DTX_N → CLK_CNV_PRX_DTX_N [49]
CNV_WR_CLKP BE3 CLK_CNV_PRX_DTX_P → CLK_CNV_PRX_DTX_P [49]
CNV_WR_D0N BB3 CNV_PRX_DTX_N0 → CNV_PRX_DTX_N0 [49]
CNV_WR_D0P BB4 CNV_PRX_DTX_P0 → CNV_PRX_DTX_P0 [49]
CNV_WR_D1N BA3 CNV_PRX_DTX_N1 → CNV_PRX_DTX_N1 [49]
CNV_WR_D1P BA2 CNV_PRX_DTX_P1 → CNV_PRX_DTX_P1 [49]
CNV_WT_CLKN BC5 CLK_CNV_PTX_DRX_N → CLK_CNV_PTX_DRX_N [49]
CNV_WT_CLKP BB6 CLK_CNV_PTX_DRX_P → CLK_CNV_PTX_DRX_P [49]
CNV_WT_D0N BE6 CNV_PTX_DRX_N0 → CNV_PTX_DRX_N0 [49]
CNV_WT_D0P BD7 CNV_PTX_DRX_P0 → CNV_PTX_DRX_P0 [49]
CNV_WT_D1N BG6 CNV_PTX_DRX_N1 → CNV_PTX_DRX_N1 [49]
CNV_WT_D1P BF6 CNV_PTX_DRX_P1 → CNV_PTX_DRX_P1 [49]
CNV_WT_RCOMP BA1 CNV_WT_RCOMP RH25 1 2 150_0402_1%

PCIE_RCOMPN B12 PCIE_RCOMPN RH21 1 2 100_0402_1%
PCIE_RCOMPP A13 PCIE_RCOMPP
SD_1P8_RCOMP BE5 SD_RCOMP_1P8 RH22 1 2 200_0402_1%
SD_3P3_RCOMP BE4 SD_RCOMP_3P3 RH23 1 2 200_0402_1%
GPPJ_RCOMP_1P81 BD1
GPPJ_RCOMP_1P82 BE1 GPPJ_RCOMP_1P8 RH24 1 2 200_0402_1%
GPPJ_RCOMP_1P83 BE2

RSVD2 Y35
RSVD3 Y36
RSVD1 BC1
TP AL35 TP@ TH101
#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

+1.8V_PRIM
RH1811 2 20K_0402_1% CNV_BRI_PRX_DTX
RH1821 2 20K_0402_1% CNV_RGI_PRX_DTX

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

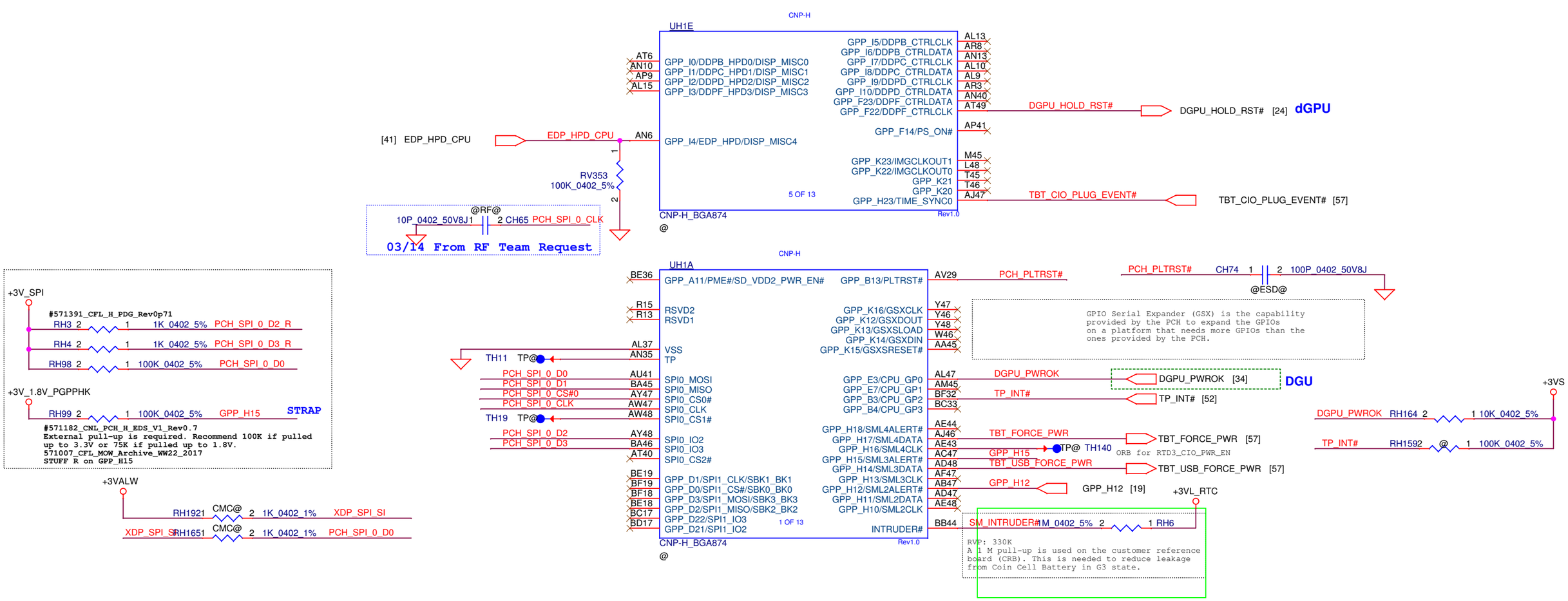
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

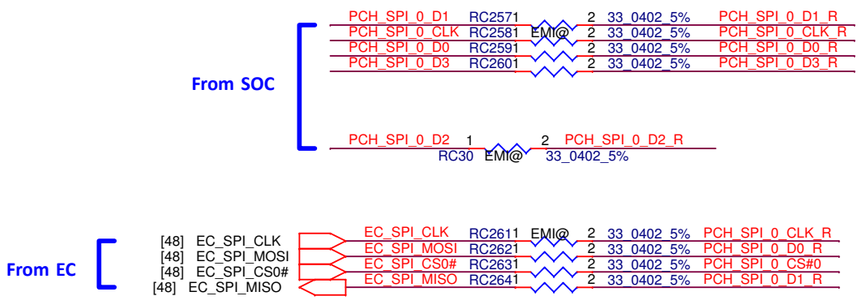
Compal Electronics, Inc.

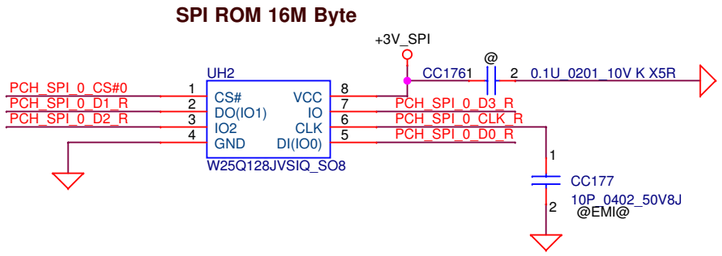
Title: PCH(2/8)CLK/CNVI/SD

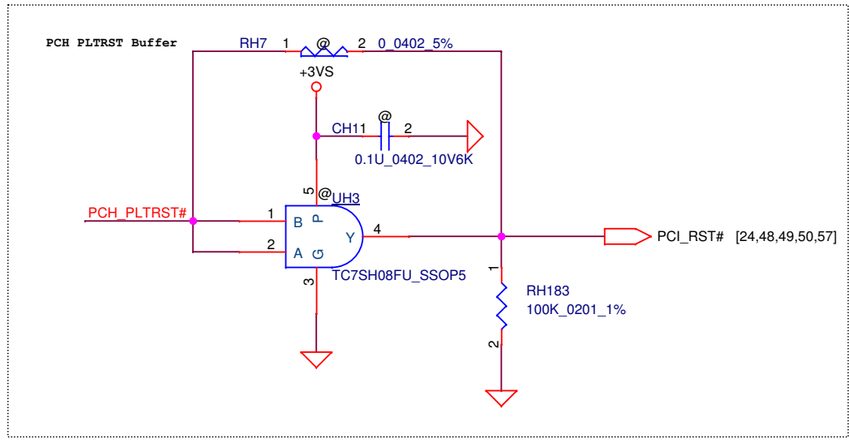
Size: Custom | Document Number: LA-G132P | Rev: 1.0

Date: Wednesday, January 09, 2019 | Sheet 15 of 81



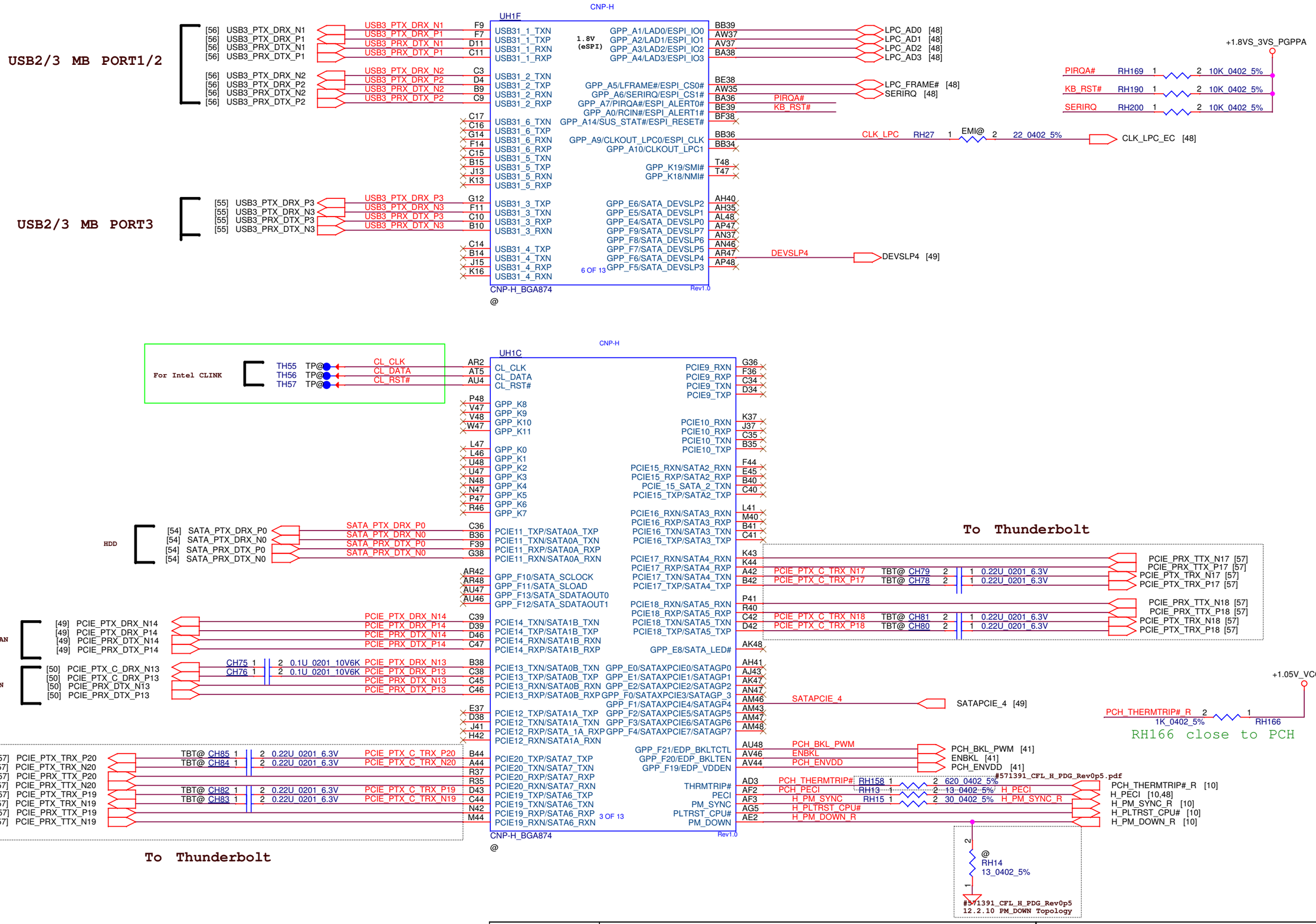






Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title	PCH(3/8)DDC/SPI		
Size: Custom	Document Number: LA-G132P		Rev: 1.0
Date: Wednesday, January 09, 2019	Sheet 16 of 81		



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: PCIE/SATA/USB3/eSPI			
Size: Custom	Document Number: LA-G132P		Rev: 1.0
Date: Wednesday, January 09, 2019	Sheet 17 of 81		

[45] HDA_RST#_R
[45] HDA_BIT_CLK_R
[45] HDA_SDOUT_R
[45] HDA_SYNC_R

HDA_RST# R — RH2091 @ 2 33_0402_5% — HDA_RST#
HDA_BIT_CLK_R — RH2101 2 33_0402_5% — HDA_BIT_CLK
HDA_SDOUT_R — RH2111 2 33_0402_5% — HDA_SDOUT
HDA_SYNC_R — RH2121 2 33_0402_5% — HDA_SYNC

@RF@ 2 HDA_BIT_CLK_R
CH66 2.2P_0402_50V8C
@RF@ 2 HDA_SYNC_R
CH67 2.2P_0402_50V8C
@RF@ 2 HDA_SDOUT_R
CH68 2.2P_0402_50V8C
@RF@ 2 HDA_RST#_R
CH69 2.2P_0402_50V8C

3/16 From RF Team Request

CNP-H
UH1D

[45] HDA_SDIN0
[19] HDA_SDOUT

HDA_BIT_CLK — BD11 — HDA_BCLK/I2S0_SCLK
HDA_SDIN0 — BE11 — HDA_SDI0/I2S0_RXD
HDA_SDOUT — BF12 — HDA_SDO/I2S0_TXD
HDA_SYNC — BG13 — HDA_SYNC/I2S0_SFRM
HDA_RST# — BE10 — HDA_RST#/I2S1_SCLK
BF10 — HDA_SDI1/I2S1_RXD
BE12 — I2S1_TXD/SNDW2_DATA
BD12 — I2S1_SFRM/SNDW2_CLK

[6] CPU_DISPA_SDO_R — CPU_DISPA_SDO_R RH28 1 2 30_0402_5% CPU_DISPA_SDO — AM2 — HDACPU_SDO
[6] CPU_DISPA_SDI_R — CPU_DISPA_SDI_R — AN3 — HDACPU_SDI
[6] CPU_DISPA_BCLK_R — CPU_DISPA_BCLK_R RH29 1 2 30_0402_5% CPU_DISPA_BCLK — AM3 — HDACPU_SCLK

FOR Jefferson Peak RESET pin is glitch free,it is recommended that a pull-down resistor of 75K ohm on GPP_D5(CNV_RF_RESET#)

[49] CLKREQ_CNV#
[49] CNV_RF_RESET#

CLKREQ_CNV# — AV18 — GPP_D8/I2S2_SCLK
CNV_RF_RESET# — AW18 — GPP_D7/I2S2_RXD
BA17 — GPP_D6/I2S2_TXD/MODEM_CLKREQ
BE16 — GPP_D5/I2S2_SFRM/CNV_RF_RESET#
BF15 — GPP_D20/DMIC_DATA0/SNDW4_DATA
BD16 — GPP_D19/DMIC_CLK0/SNDW4_CLK
AV16 — GPP_D18/DMIC_DATA1/SNDW3_DATA
AW15 — GPP_D17/DMIC_CLK1/SNDW3_CLK

1.8V

+3VL_RTC
RH31 1 2 20K_0402_1% PCH_SRTCRST#
CH9 1 2 1U_0201_6.3V6M
RH32 1 2 20K_0402_1% EC_CLEAR_CMOS#
CH10 1 2 1U_0201_6.3V6M
CLRP2 1 2 SHORT PADS
ECLR CMOS Delay 18~25 ms
modified in 2017/12/03

[48] EC_CLEAR_CMOS# — BE47 — RTCRST#
PCH_SRTCRST# — BD46 — SRTCRST#

[48] PCH_PWROK — PCH_PWROK — AY42 — PCH_PWROK
[48] EC_RSMRST# — EC_RSMRST# — BA47 — RSMRST#

PCH_DPWROK — AW41 — DSW_PWROK

SMB (Link to DDR)
[19] SMBALERT# — SMBALERT# — BE25 — GPP_C2/SMBALERT#
[22,23] PCH_SMBCLK — PCH_SMBCLK — BE26 — GPP_C0/SMBCLK
[22,23] PCH_SMBDATA — PCH_SMBDATA — BF26 — GPP_C1/SMBDATA
[19] PCH_SML0ALERT# — PCH_SML0ALERT# — BF24 — GPP_C5/SML0ALERT#
PCH_SML0CLK — BF25 — GPP_C3/SML0CLK
PCH_SML0DATA — BE24 — GPP_C4/SML0DATA
[19] PCH_SML1ALERT# — PCH_SML1ALERT# — BD33 — GPP_B23/SML1ALERT#/PCHHOT#

SML1 (Link to EC,DGPU)
[25,41,46,48,51] EC_SMB_CK2 — EC_SMB_CK2 — BF27 — GPP_C6/SML1CLK
[25,41,46,48,51] EC_SMB_DA2 — EC_SMB_DA2 — BE27 — GPP_C7/SML1DATA

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Rev1.0
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GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF# — BF36
GPP_A8/CLKRUN# — AV32 — PM_CLKRUN# — PM_CLKRUN# [48]
GPD11/LANPHYPC — BF41
GPD9/SLP_WLAN# — BD42
DRAM_RESET# — BB46 — DDR_DRAMRST#
GPP_B2/VRALERT# — BE32
GPP_B1/GSPI1_CS1#/TIME_SYNC1 — BF33
GPP_B0/GSPI0_CS1# — BE29
GPP_K17/ADR_COMPLETE — R47
GPP_B11/I2S_MCLK — AP29
SYS_PWROK — AU3 — SYS_PWROK — SYS_PWROK [48]
WAKE# — BB47 — TBT_WAKE# — TBT_WAKE# [57]
GPD6/SLP_A# — BE40
SLP_LAN# — BF40
GPP_B12/SLP_S0# — BC28
GPD4/SLP_S3# — BF42 — PM_SLP_S3# — PM_SLP_S3# [48,68]
GPD5/SLP_S4# — BE42 — PM_SLP_S4# — PM_SLP_S4# [48,65,67]
GPD10/SLP_S5# — BC42 — PM_SLP_S5#
GPD8/SUSCLK — BE45 — SUSCLK — SUSCLK [49]
GPD0/BATLOW# — BF44 — PM_BATLOW# — PM_BATLOW# [57]
GPP_A15/SUSACK# — BE35 — SUSACK# R
GPP_A13/SUSWARN#/SUSPWRDNACK — BC37 — SUSWARN#
GPD2/LAN_WAKE# — BG44 — LAN_WAKE#
GPD1/ACPRESENT — BG42
SLP_SUS# — BD39 — SLP_SUS#
GPD3/PWRBTN# — BE46 — PBTN_OUT# R — RH48 1 @ 2 0_0402_5% PBTN_OUT# — PBTN_OUT# [48]
SYS_RESET# — AU2 — SYS_RESET#
GPP_B14/SPKR — AW29 — SPKR — SPKR [19,45]
CPUPWRGD — AE3 — H_CPUPWRGD — H_CPUPWRGD [10]
ITP_PMODE — AL3 — XDP_ITP_PMODE
PCH_JTAGX — AH4 — CPU_XDP_TCK0 — CPU_XDP_TCK0 [10]
PCH_JTAG_TMS — AJ4 — CPU_XDP_TMS — CPU_XDP_TMS [10]
PCH_JTAG_TDO — AH3 — CPU_XDP_TDO — CPU_XDP_TDO [10]
PCH_JTAG_TDI — AH2 — CPU_XDP_TDI — CPU_XDP_TDI [10]
PCH_JTAG_TCK — AJ3 — PCH_JTAG_TCK1 — TP@ T398

+1.2V
RH39 470_0402_1%
DDR_DRAMRST# [22,23]
CH11 100P_0402_50V8J @ESD@
Near PCH

TP@ T415
TP@ T397
TP@ T372
TP@ T371
TP@ T373
AC_PRESENT [48]
PBTN_OUT# [48]
No Support Deep Sx

Connect CPU & PCH

+3VALW
RH1712 @ 1 1K_0402_5% TBT_WAKE#
RH41 2 1 8.2K_0402_5% PM_BATLOW#
RH45 2 @ 1 100K_0402_5% AC_PRESENT
RH47 2 @ 1 100K_0402_5% PBTN_OUT#_R

+1.8VS_3VS_PGPPA
RH44 2 LPC@ 1 100K_0402_5% PM_CLKRUN#
10k pull up

+3VS
RH213 1 2 1K_0402_5% PCH_SML0CLK
RH214 1 2 1K_0402_5% PCH_SML0DATA
RH215 1 2 1K_0402_5% EC_SMB_CK2
RH216 1 2 1K_0402_5% EC_SMB_DA2

+3VALW
RH217 1 2 1K_0402_5% PCH_SMBCLK
RH218 1 2 1K_0402_5% PCH_SMBDATA

+1.05VALW
RH191 2 CMC@ 1 1K_0402_5% XDP_ITP_PMODE

+3VALW +3VALW
RH219 1 2 10K_0402_5% PCH_PWROK
RH220 1 2 10K_0402_5% LAN_WAKE#
RH221 1 2 10K_0402_5% EC_RSMRST#
RH222 1 2 10K_0402_5% SYS_RESET#

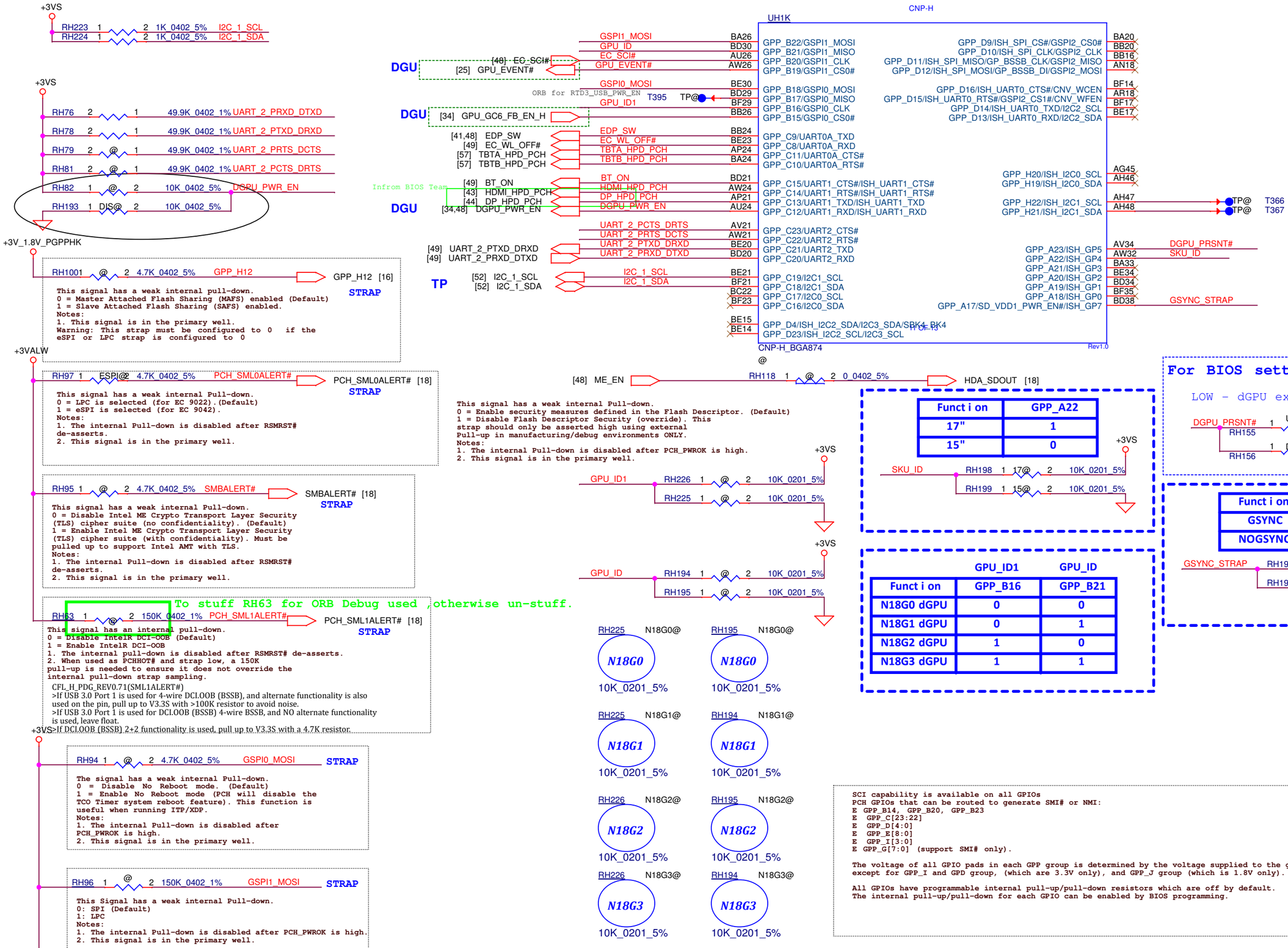
EC_RSMRST# RH52 2 @ 1 0_0402_5% PCH_DPWROK
100K_0402_5% 1 @ 2 RH50 PCH_DPWROK

@ESD@ 100P_0402_50V8J 1 2 CH71 SYS_RESET#
@ESD@ 100P_0402_50V8J 1 2 CH72 SYS_PWROK
@ESD@ 100P_0402_50V8J 1 2 CH73 PCH_PWROK
Near PCH side
From ESD Team Request

SYS_PWROK
RH188 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.
Title: PCH(5/8)PMU/HDA/SMBUS/DMIC
Size: Custom | Document Number: LA-G132P | Rev: 1.0
Date: Wednesday, January 09, 2019 | Sheet 18 of 81



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Title	Compal Electronics, Inc.		
	PCH(6/8)GPIO/I2C/UART/STRAP		
Size	Document Number		Rev
Custom	LA-G132P		1.0
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GPIO Group	Voltage
GPPA	LPC: 3.3V eSPI: 1.8V *
GPPB GPPC	3.3V
GPPD	1.8V for SOC_DMIC * 3.3V for IR_DMIC
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

+1.05VALW
5.95A
close to VCCPRIM balls
1U_0201_6.3V6M CH62
6.6A
close to VCCPRIM balls
22U_0603_6.3V6M CH12
1U_0201_6.3V6M CH13
PLACE 3-5MM FROM PACKAGE EDGE

+3VS
RC73 1 @ 2 0_0603_5%
+1.8VS_3VS_PGPPA

+1.05VALW
UH1H
CNP-H
HSIO for DMIU/USB3.1/PCIE=4162mA
5.95A AA22 VCCPRIM_1P051
AA23 VCCPRIM_1P052
AB20 VCCPRIM_1P053
AB22 VCCPRIM_1P054
AB23 VCCPRIM_1P055
AB27 VCCPRIM_1P056
AB28 VCCPRIM_1P057
AB30 VCCPRIM_1P058
AD20 VCCPRIM_1P059
AD23 VCCPRIM_1P0510
AD27 VCCPRIM_1P0511
AD28 VCCPRIM_1P0512
AD30 VCCPRIM_1P0513
AF23 VCCPRIM_1P0516
AF27 VCCPRIM_1P0517
AF30 VCCPRIM_1P0518
+1.05VALW
6.6A U26 VCCPRIM_1P0523
U29 VCCPRIM_1P0524
V25 VCCPRIM_1P0525
V27 VCCPRIM_1P0526
V28 VCCPRIM_1P0527
V30 VCCPRIM_1P0528
V31 VCCPRIM_1P0529
+1.05V_FUSE
0.0012A AD31 VCCPRIM_1P0514
+1.05V_CNV_HVLDO
0.2A AE17 VCCPRIM_1P0515
+1.05V_VCCUSB
0.42A W22 VCCDUSB_1P051
+1.05V_VCCDSW W23 VCCDUSB_1P052
+1.05V_VCCCLPLLEBB
+1.05V_VCCDSW BG45 VCCDSW_1P051
BG46 VCCDSW_1P052
0.109A W31 VCCPRIM_MPHY_1P05
+1.05V_VCCAZPLL
0.015A D1 VCCPRIM_1P0521
E1 VCCPRIM_1P0522
0.213A C49 VCCAMPHYPLL_1P051
+1.05V_VCCAMPHYPLL D49 VCCAMPHYPLL_1P052
+1.05V_XTAL E49 VCCAMPHYPLL_1P053
0.00428A P2 VCCA_XTAL_1P051
+1.05V_SRC P3 VCCA_XTAL_1P052
0.169A W19 VCCA_SRC_1P051
+1.05V_OCPLL1 W20 VCCA_SRC_1P052
+1.05V_OC
0.0198A C1 VCCAPLL_1P054
C2 VCCAPLL_1P055
0.0085A V19 VCCA_BCLK_1P05
+1.05V_BCLKPLL2
0.021A B1 VCCAPLL_1P051
B2 VCCAPLL_1P052
B3 VCCAPLL_1P053
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Rev1.0
@

VCCPRIM_3P32 AW9 0.182A
+3V_PHVC
DCPRTC1 BF47
DCPRTC2 BG47
+VCCRTCEXT
+VCCRTCEXT
+3V_USB2
VCCPRIM_3P35 V23 0.095A
+3V_SPI
VCCSPI AN44 0.042A
VCCRTC1 BC49
VCCRTC2 BD49
+3VL_RTC
+3VALW
VCCPGPPG_3P3 AN21 0.195A
VCCPRIM_3P33 AY8
+3V_PHVLDO
VCCPRIM_3P34 BB7 0.97A
+3V_1.8V_PGPPHK
VCCPGPPHK1 AC35 0.262A
VCCPGPPHK2 AC36
+3VALW
VCCPGPPEF1 AE35 0.174A
VCCPGPPEF2 AE36
+3V_1.8V_PGPPD
VCCPGPPD AN24 0.14A
VCCPGPPBC1 AN26
VCCPGPPBC2 AP26 0.334A
+3V_1.8V_PGPPA
VCCPGPPA AN32 0.101A
+3VALW
VCCPRIM_3P31 AT44 0.106A
VCCDSW_3P31 BE48
VCCDSW_3P32 BE49 0.113A
+3VALW
+3VALW_HDA
VCCHDA BB14 0.00767A
VCCPRIM_1P83 AG19
VCCPRIM_1P84 AG20
VCCPRIM_1P85 AN15
VCCPRIM_1P86 AR15
VCCPRIM_1P87 BB11 0.766A
+1.8V_PRIM
VCCPRIM_1P81 AF19 0.882A
+1.8V_PHVLDO
VCCPRIM_1P82 AF20 +1.8V_PHVLDO RH1721 @ 2 0.01_0402_1% +1.8V_PRIM
VCCPHVLDO_1P8
(External VRM mode RH172 unmount)
VCCPRIM_1P0520 AG31 0.193A
VCCPRIM_1P0519 AF31 0.0895A
VCCPRIM_1P241 AK22
VCCPRIM_1P242 AK23
+1.05V_FHV1
+1.05V_FHV0
+1.24V_VCCLDOSRAM_IN
VCCDPHY_1P241 AJ22
VCCDPHY_1P242 AJ23
VCCDPHY_1P243 BG5
Internal LDO
+1.24V_PRIM_DPHY
Short pins AJ22,AJ23,AK22,AK23 together at surface layer from PDG Rev0.71
+1.24V_PRIM_MAR
VCCMPHY_SENSE K47
VSSMPHY_SENSE K46
TP@ TH139 +1.24V_VCCLDOSRAM_IN
TP@ TH138
+1.24V_PRIM_DPHY
RH174 1 @ 2 0_0402_5%
RH174 for 571391_CFL_H_PDG_Rev0p71.pdf

+VCCRTCEXT
0.1U_0402_10V6K CH25 @

+1.8V_PRIM
4.7U_0402_6.3V6M CH35 @
1U_0201_6.3V6M CH28
Close to BB11

For DDX03 R02
+1.24V_PRIM_MAR
4.7U_0402_6.3V6M CH36

+1.05V_VCCDSW
1U_0201_6.3V6M @ CH16

+1.05VALW
RH56 1 @ 2 0_0603_5%
+1.05V_FUSE
+1.05V_CNV_HVLDO
RH57 1 @ 2 0_0603_5%
+1.05V_VCCUSB
RH58 1 @ 2 0_0603_5%
0.1U_0402_10V6K CH14 @
+1.05V_VCCCLPLLEBB
RH59 1 @ 2 0_0603_5%
0.1U_0201_10V6K CH15
+1.05V_VCCAZPLL
RH84 1 @ 2 0_0603_5%
1P_0402_50V8 CH24 @
1P_0402_50V8 CH17 @
+1.05V_VCCAMPHYPLL
RH61 1 @ 2 0_0603_5%
22U_0603_6.3V6M @ CH18
1U_0201_6.3V6M CH19
+1.05V_XTAL
RH83 1 @ 2 0_0603_5%
22U_0603_6.3V6M @ CH20

+1.05VALW
+1.05V_SRC
RH85 1 @ 2 0_0603_5%
+1.05V_OCPLL1
RH86 1 @ 2 0_0603_5%
1U_0201_6.3V6M CH21
+1.05V_OC
RH87 1 @ 2 0_0603_5%
0.1U_0402_10V6K CH22 @
+1.05V_BCLKPLL2
RH88 1 @ 2 0_0603_5%
1U_0201_6.3V6M CH23
+1.05V_FHV1
RH119 1 @ 2 0_0603_5%
+1.05V_FHV0
RH120 1 @ 2 0_0603_5%

+3VALW
+3V_PHVC
RH90 1 @ 2 0_0603_5%
+3V_USB2
RH91 1 @ 2 0_0603_5%
+3V_SPI
RH138 1 @ 2 0_0603_5%
+3V_PHVLDO
RH125 1 @ 2 0_0603_5%
1U_0201_6.3V6M CH31
0.1U_0402_10V6K CH30 @
+3VALW
0.1U_0201_10V6K CH34
+1.8VALW
+1.8V_PRIM
RH161 1 @ 2 0_0603_5%

+3VALW
+3V_1.8V_PGPPHK
+1.8V_PRIM
RH139 1 @ 2 0_0603_5%
RH146 1 @ 2 0_0402_5%
0.1U_0402_10V6K CH32 @
+3VALW
0.1U_0402_10V6K CH33 @
+3V_1.8V_PGPPD
RH141 1 @ 2 0_01_0402_1%
RH1481 @ 2 0_0402_5%
+3V_1.8V_PGPPA
RH143 1 @ 2 0_0603_5%
+3VALW_HDA
RH187 1 @ 2 0_0603_5%
1P_0402_50V8 CH64 @
1P_0402_50V8 CH63 @

+3VL_RTC
W=20mils
+RTCVCC
RH1861 @ 2 0_0402_5%
1U_0201_6.3V6M CH27

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

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Title: PCH(7/8)Power

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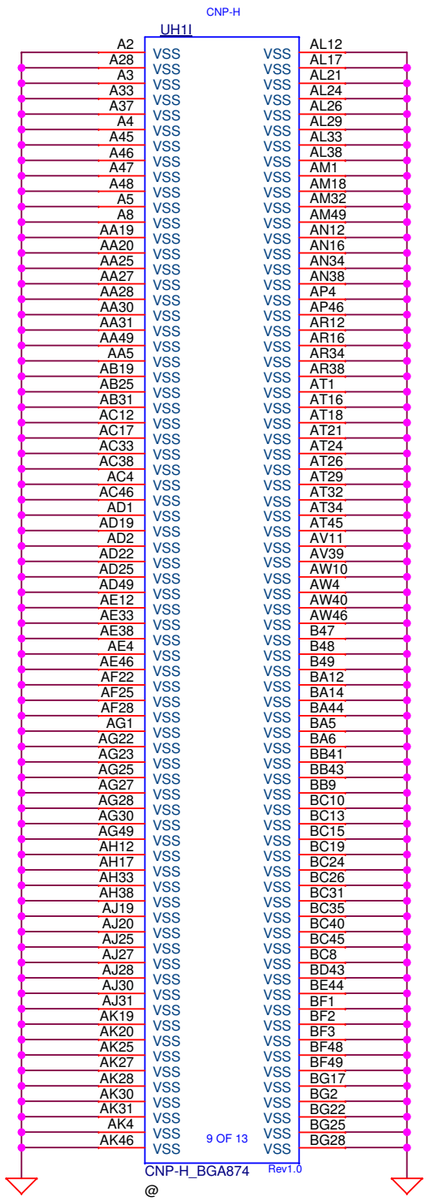

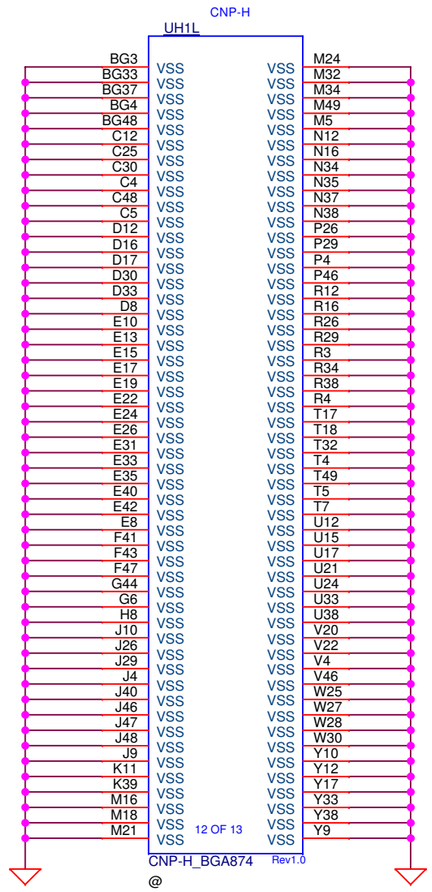

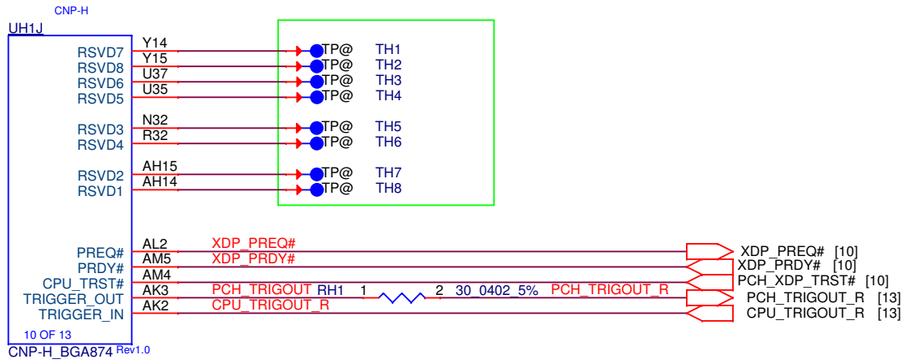

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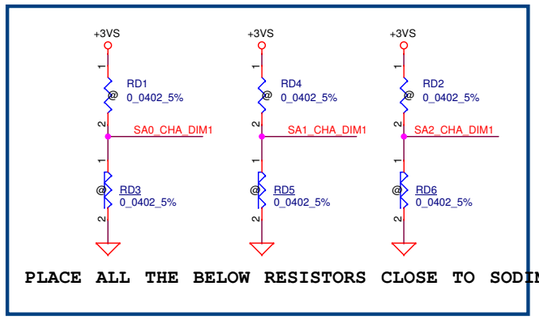
CHANNEL-A

BOT REVERSE TYPE (4 mm)

Interleaved Memory

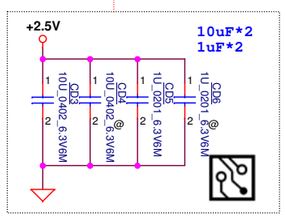
TOP: JDIMM1 CONN Non-ECC DIMM



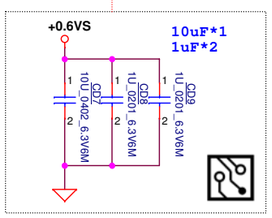
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

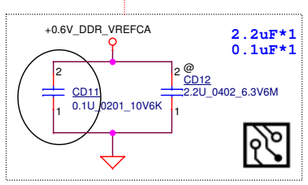
Layout Note:
Place near JDIMM1.257,259



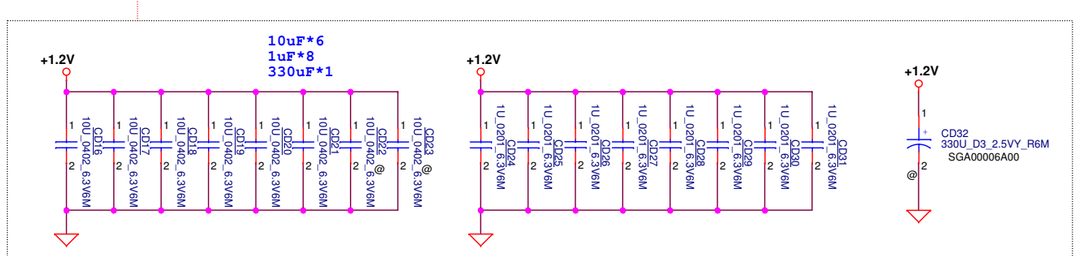
Layout Note:
Place near JDIMM1.258

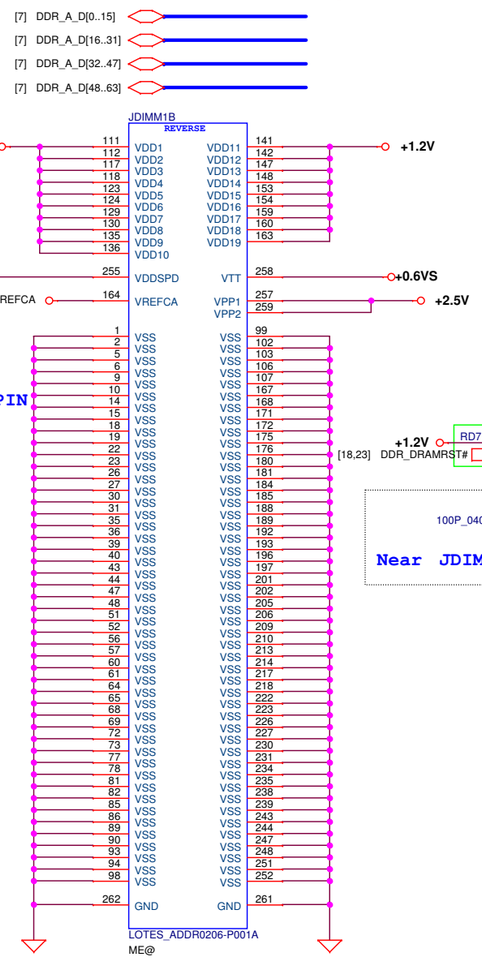


Layout Note:
PLACE THE CAP near JDIMM1. 164



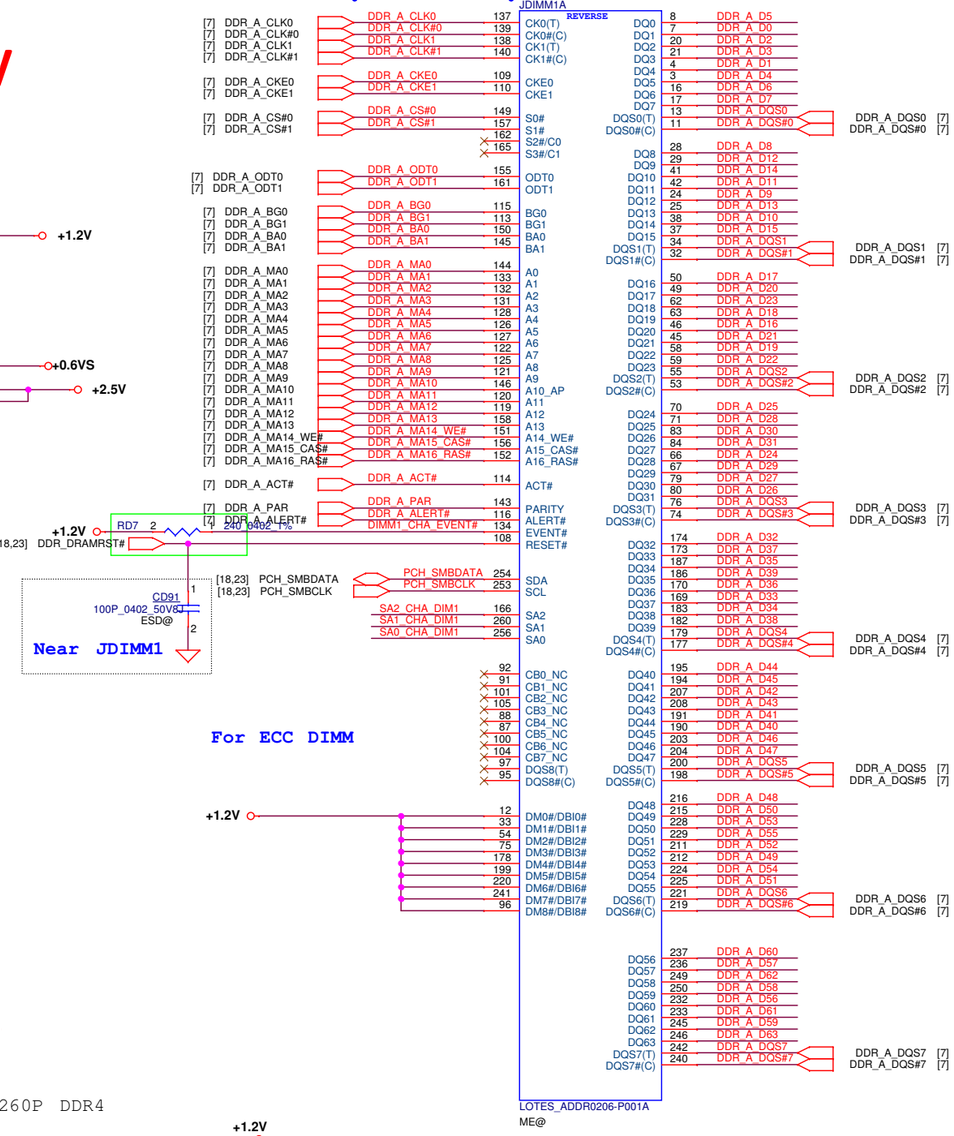
Layout Note:
Place near JDIMM1

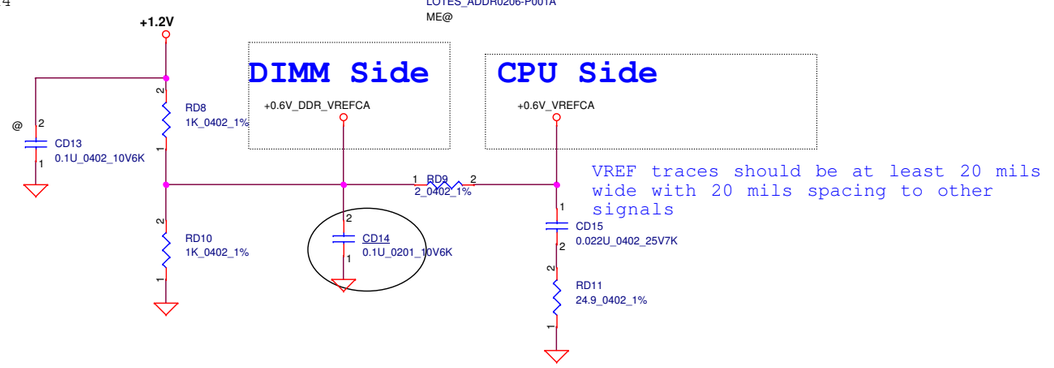




PLACE NEAR TO PIN

Part Number:SP07001FYH0
Part Value:S SOCKET FOX_AS0A826-H4RB-7H 260P DDR4





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Title	DDRIV_CHA: DIMM0
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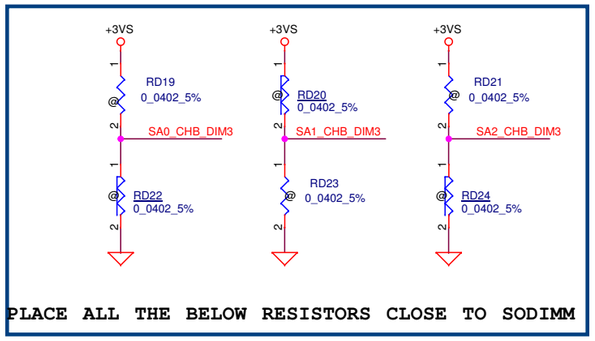
CHANNEL-B

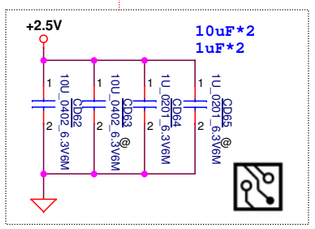
TOP: JDIMM3 CONN Non-ECC DIMM



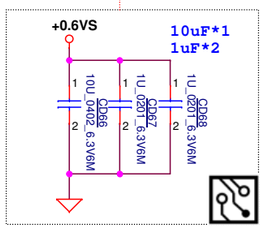
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

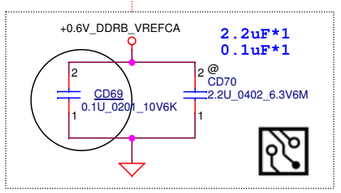
Layout Note:
Place near JDIMM3.257,259



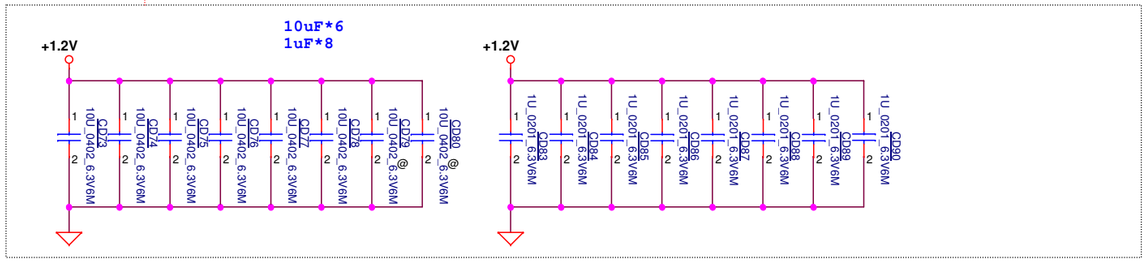
Layout Note:
Place near JDIMM3.258



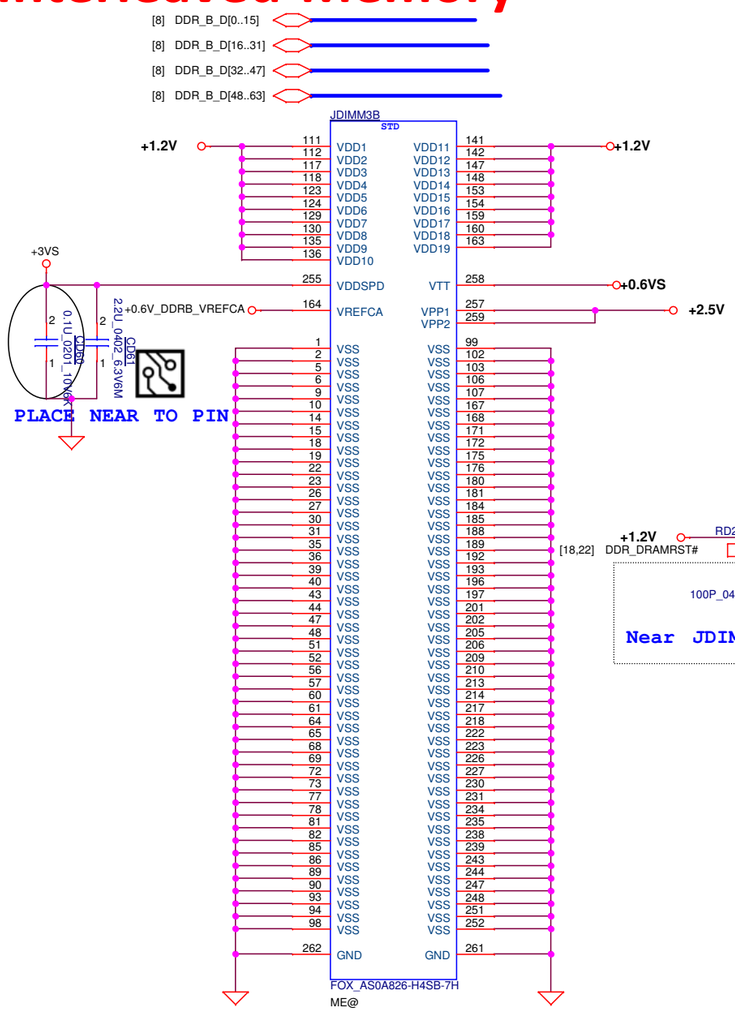
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3



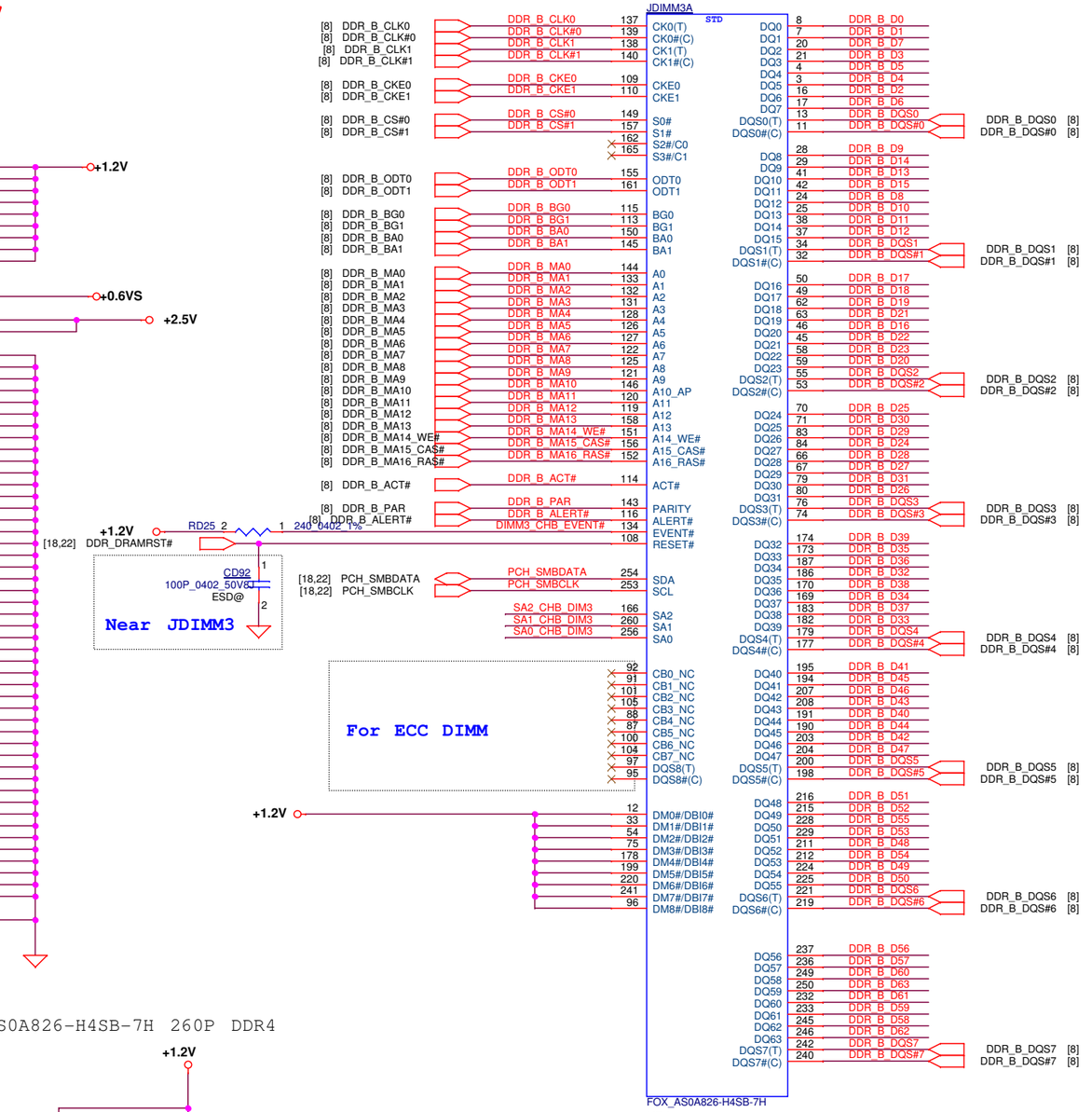
Layout Note:
Place near JDIMM3

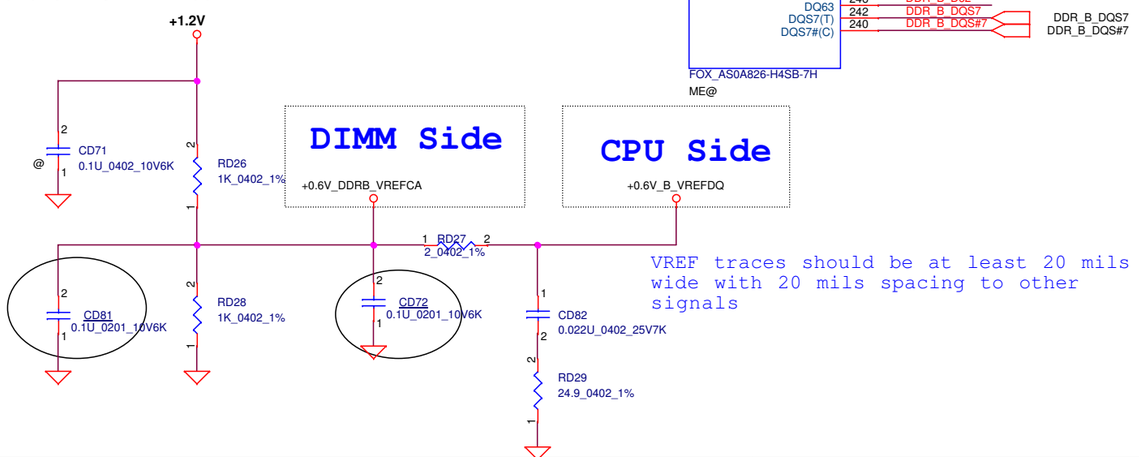


Interleaved Memory



Part Number:SP07001CEA0
Part Value:S SOCKET FOX_AS0A826-H4SB-7H 260P DDR4





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Title: **DDRIV_CHB: DIMM0**

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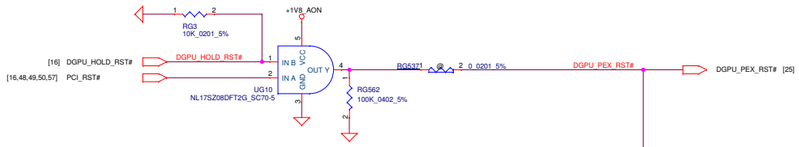
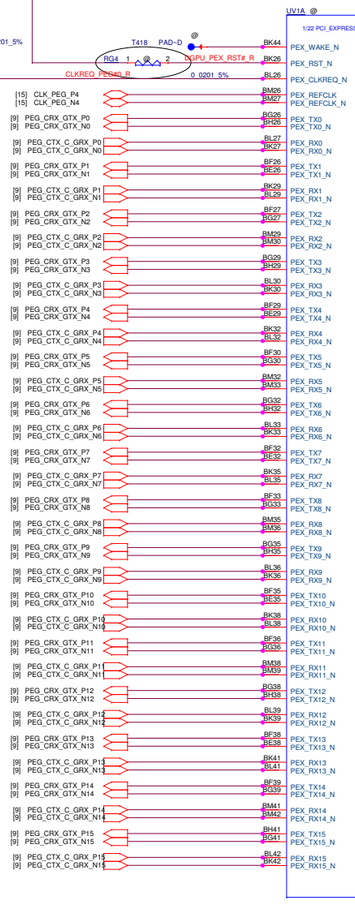
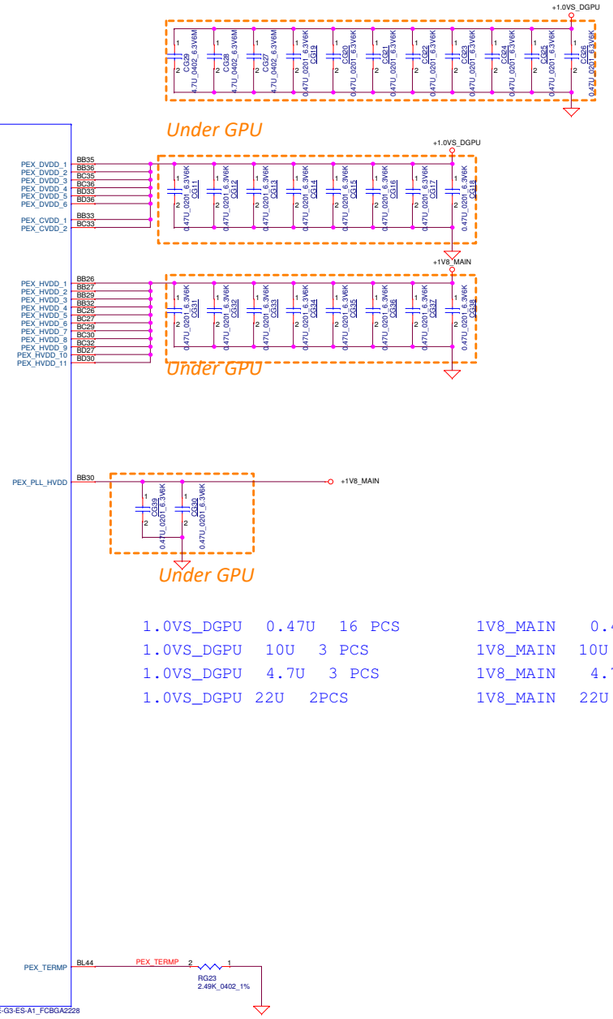
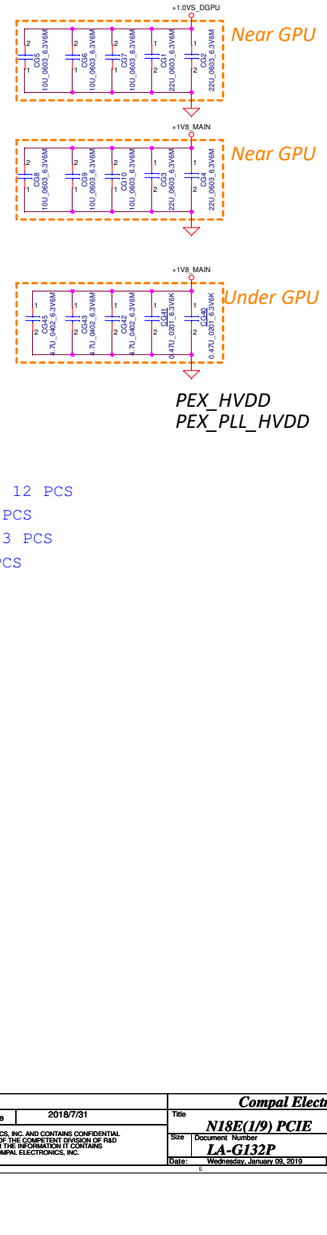
GC OFF 1.0 GPU Power ON/OFF





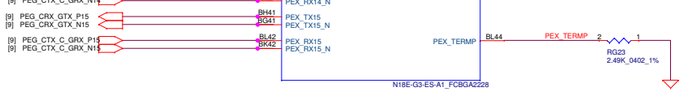




PEX_DVDD
PEX_CVDD

PEX_HVDD
PEX_PLL_HVDD

1.0VS_DGPU	0.47U	16 PCS	1V8_MAIN	0.47U	12 PCS
1.0VS_DGPU	10U	3 PCS	1V8_MAIN	10U	3 PCS
1.0VS_DGPU	4.7U	3 PCS	1V8_MAIN	4.7U	3 PCS
1.0VS_DGPU	22U	2PCS	1V8_MAIN	22U	2PCS



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Title	N18E(1/9) PCIE		
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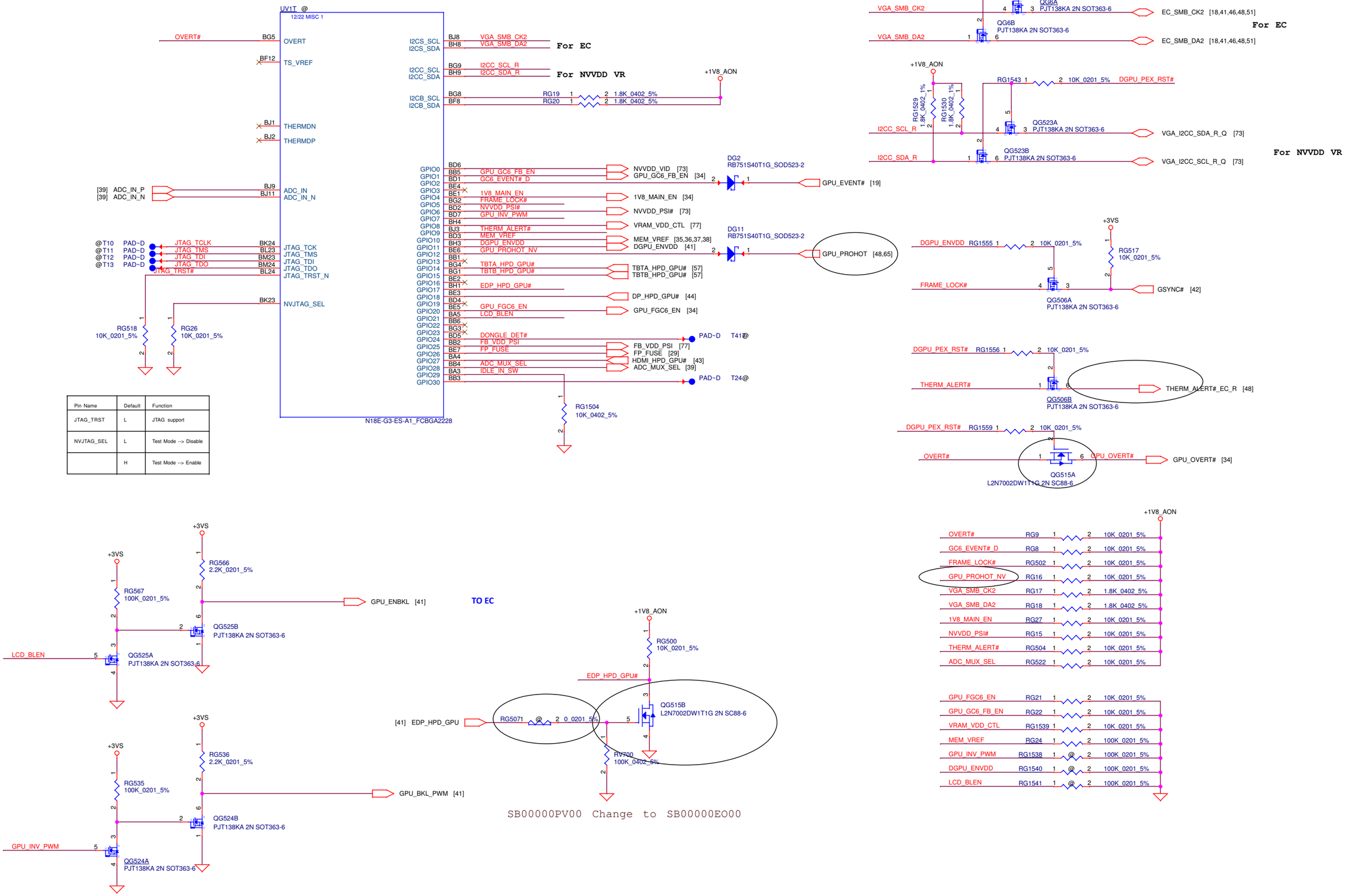

Pin Name	Default	Function
JTAG_TRST	L	JTAG support
NVJTAG_SEL	L	Test Mode --> Disable
	H	Test Mode --> Enable

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: N18E(2/9) GPIO

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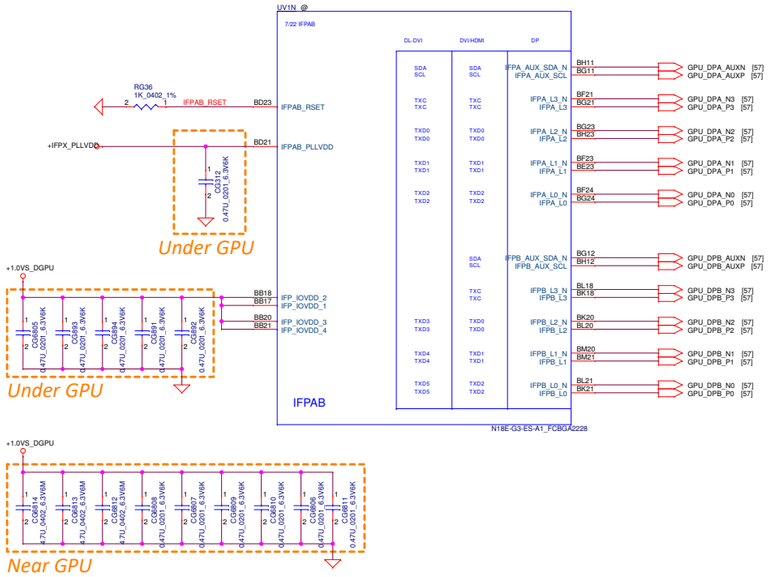


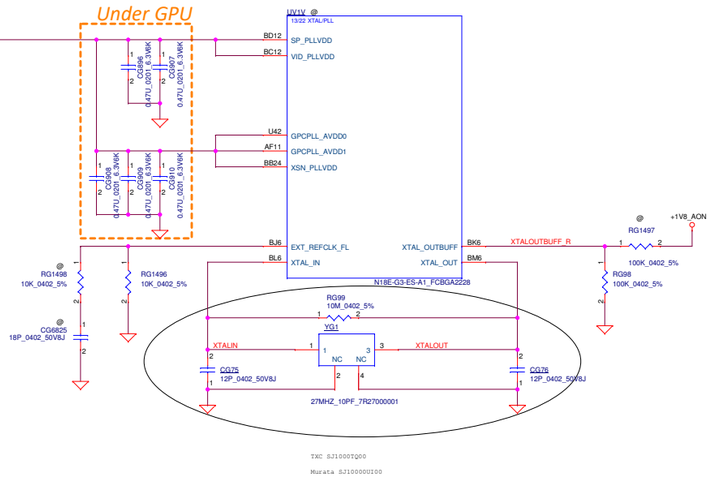
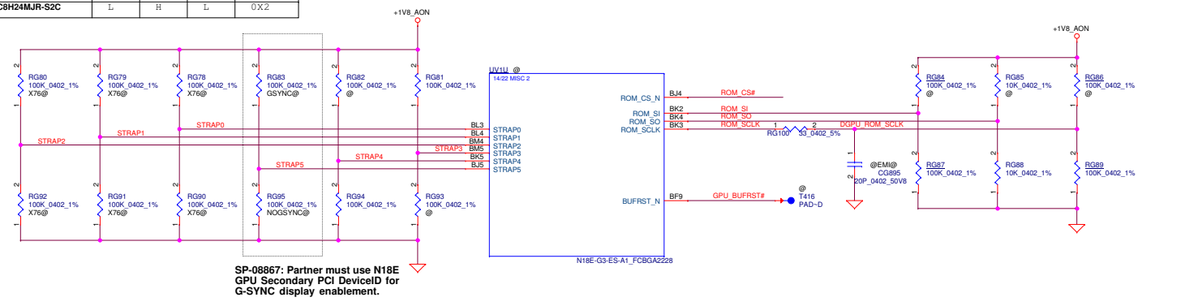


Table 11.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)

GDDR6 VRAM	Strap2	Strap1	Strap0	RAMCFG
Samsung , K4ZB80325BC-HC14	L	L	L	0X0
Micron , MT61K256M32JE-14:A	L	L	H	0X1
Hynix , H56C8H24MJR-S2C	L	H	L	0X2



SP-08867: Partner must use N18E GPU Secondary PCI DeviceID for G-SYNC display enablement.

Table 11.4 FS_OVERT* Strap Enablement

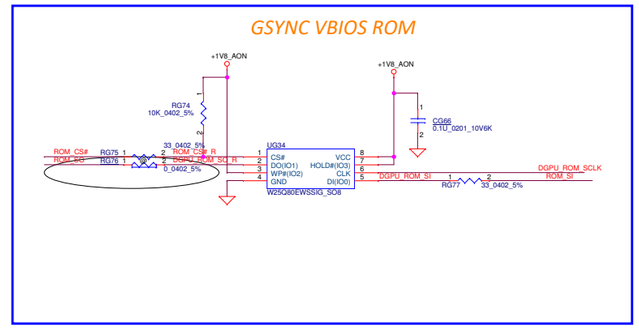
Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note that configurations other than the two listed in Table 11.4 must be avoided, as otherwise damage to strap inputs may result.

Table 11.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0

- **SMB_ALT_ADDR Enable**. This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits.
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG**: This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N18x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits (consult NVIDIA for details on proper bit setting for MS-Hybrid solutions).



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/7/31	Deciphered Date 2018/7/31	Title N18E(3/9) Strap, XTAL, IFP
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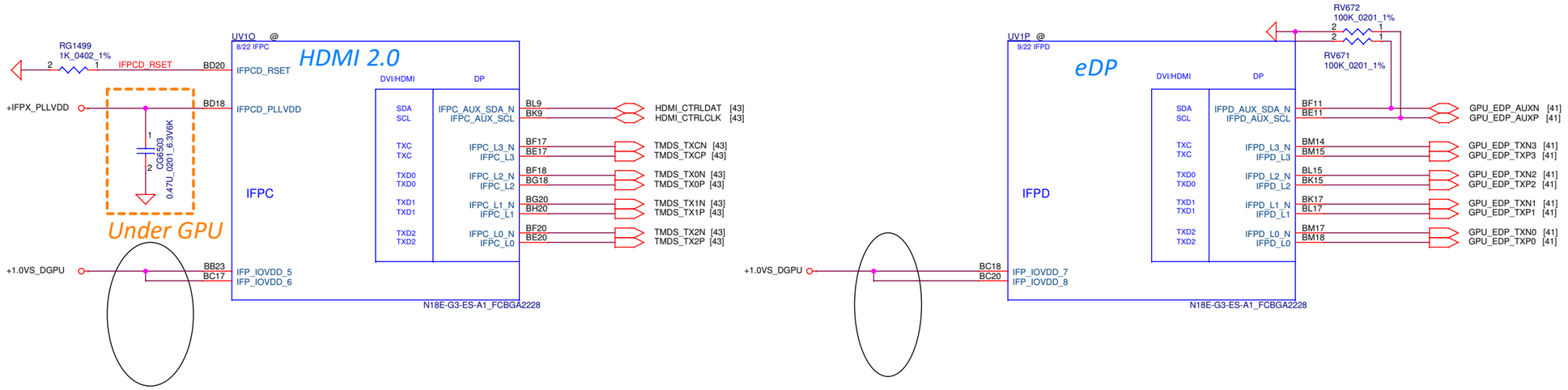

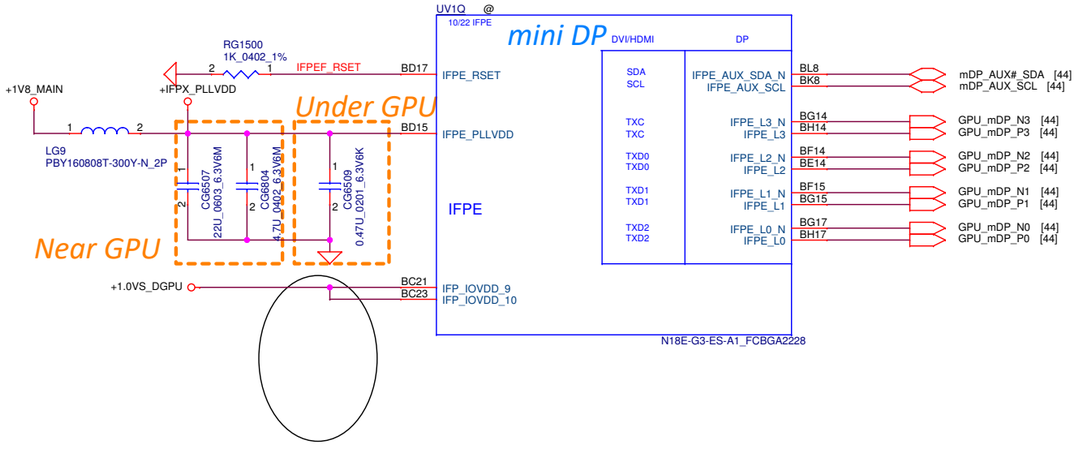

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Title: **N18E(4/9) eDP, HDMI, DP**

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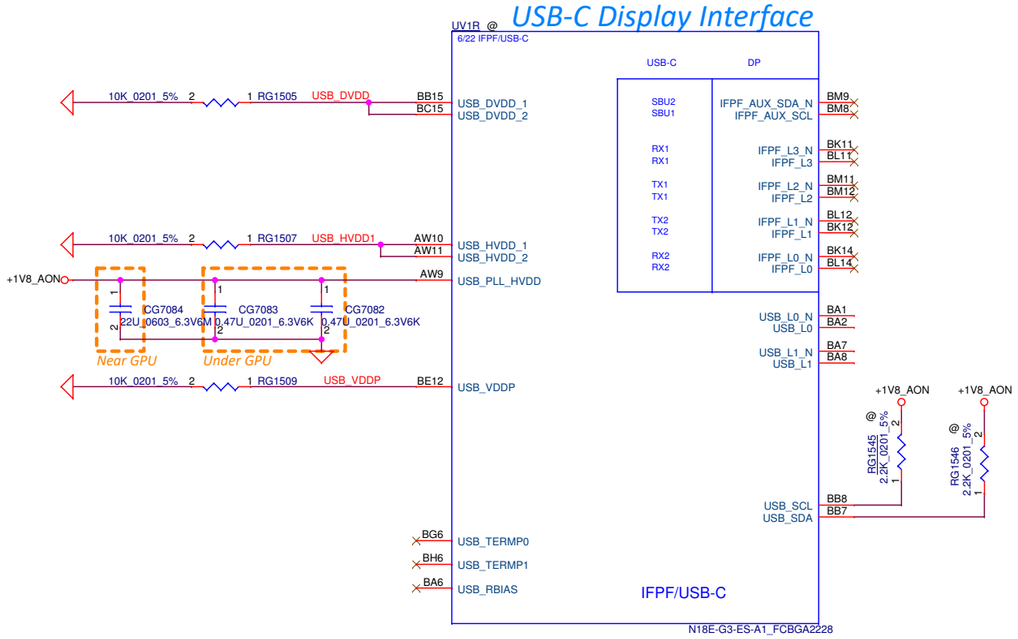
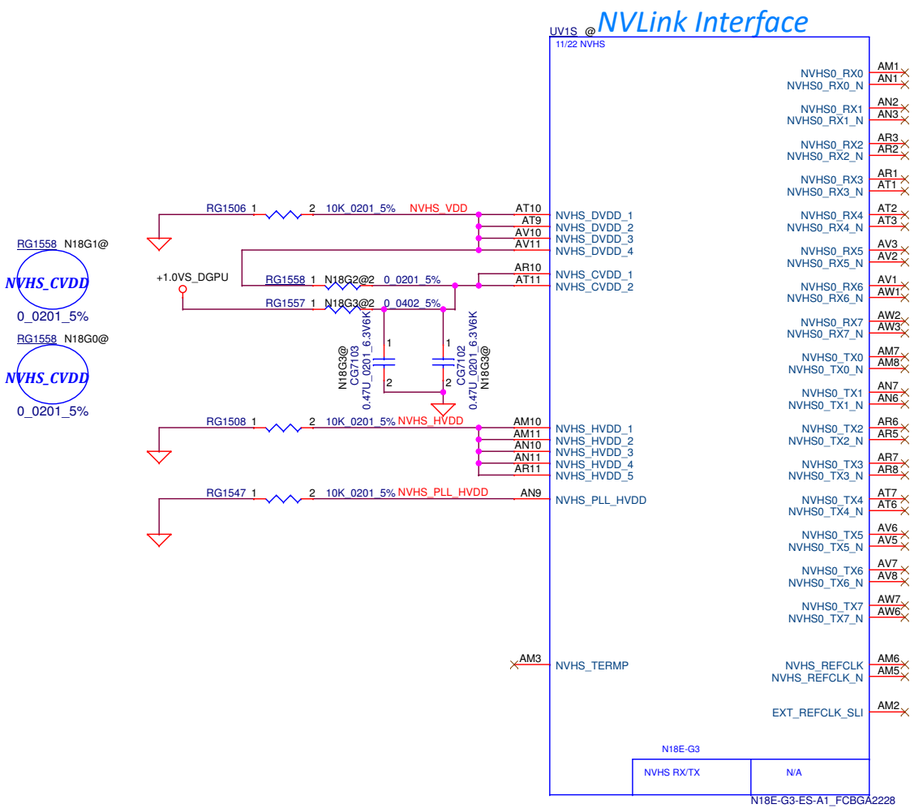
USB-C Display Interface



NVLink Interface



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: N18E(5/9) USB-C, NVLink			
Size	Document Number: LA-G132P		Rev: 1.0
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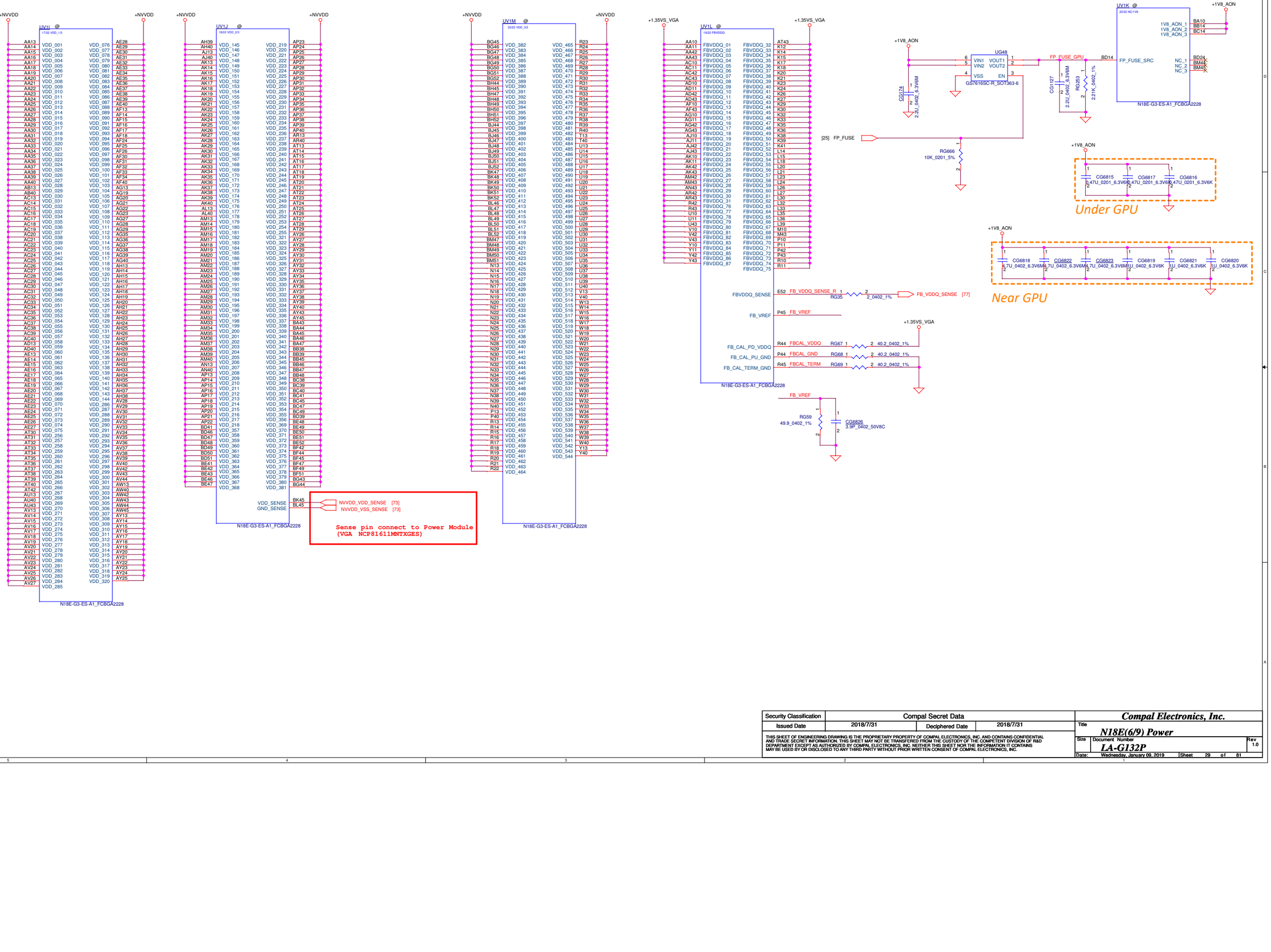

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

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Title: *N18E(6/9) Power*

Size: | Document Number: *LA-G132P* | Rev: 1.0

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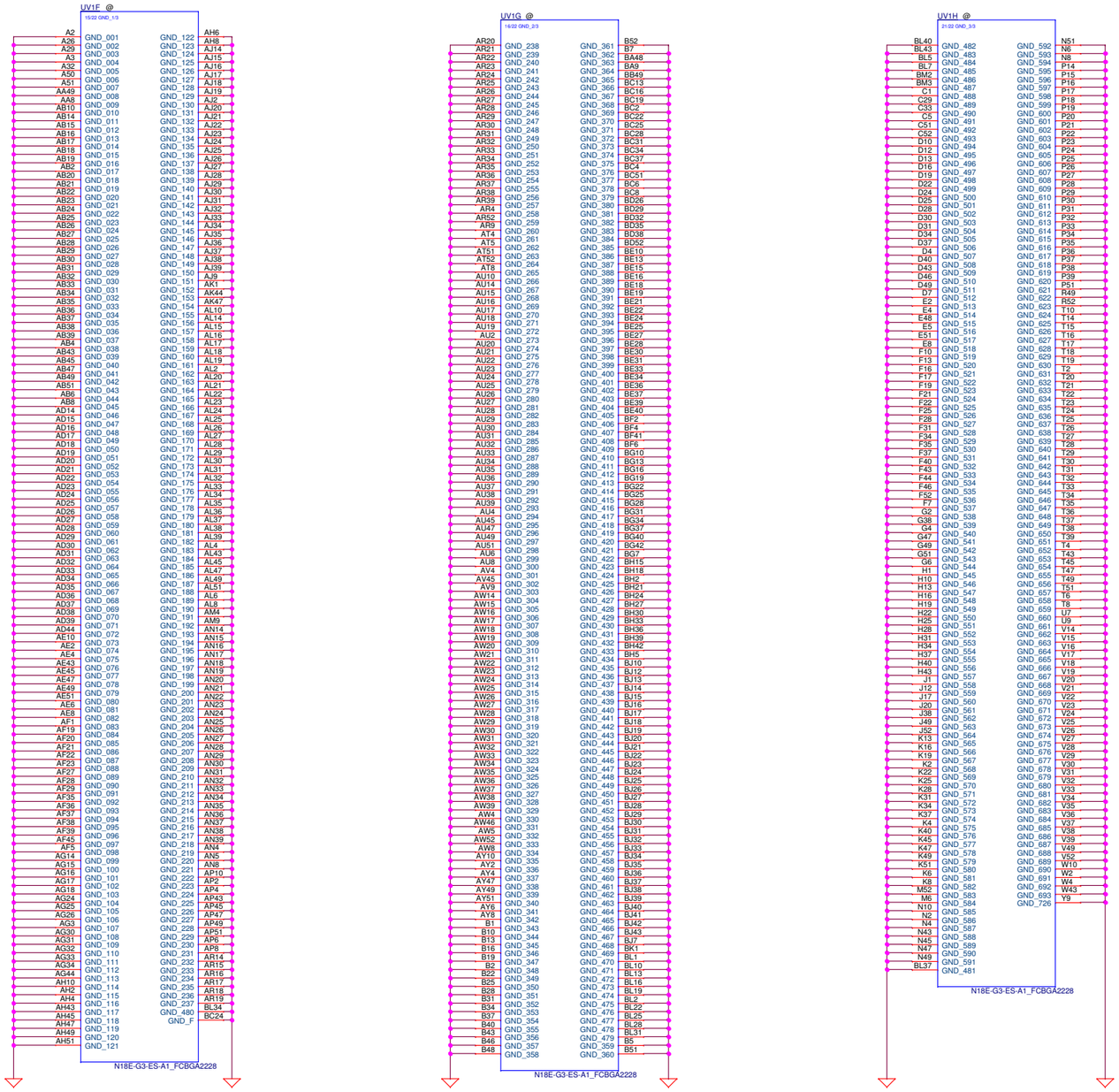

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

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Title: **N18E(7/9) GND**

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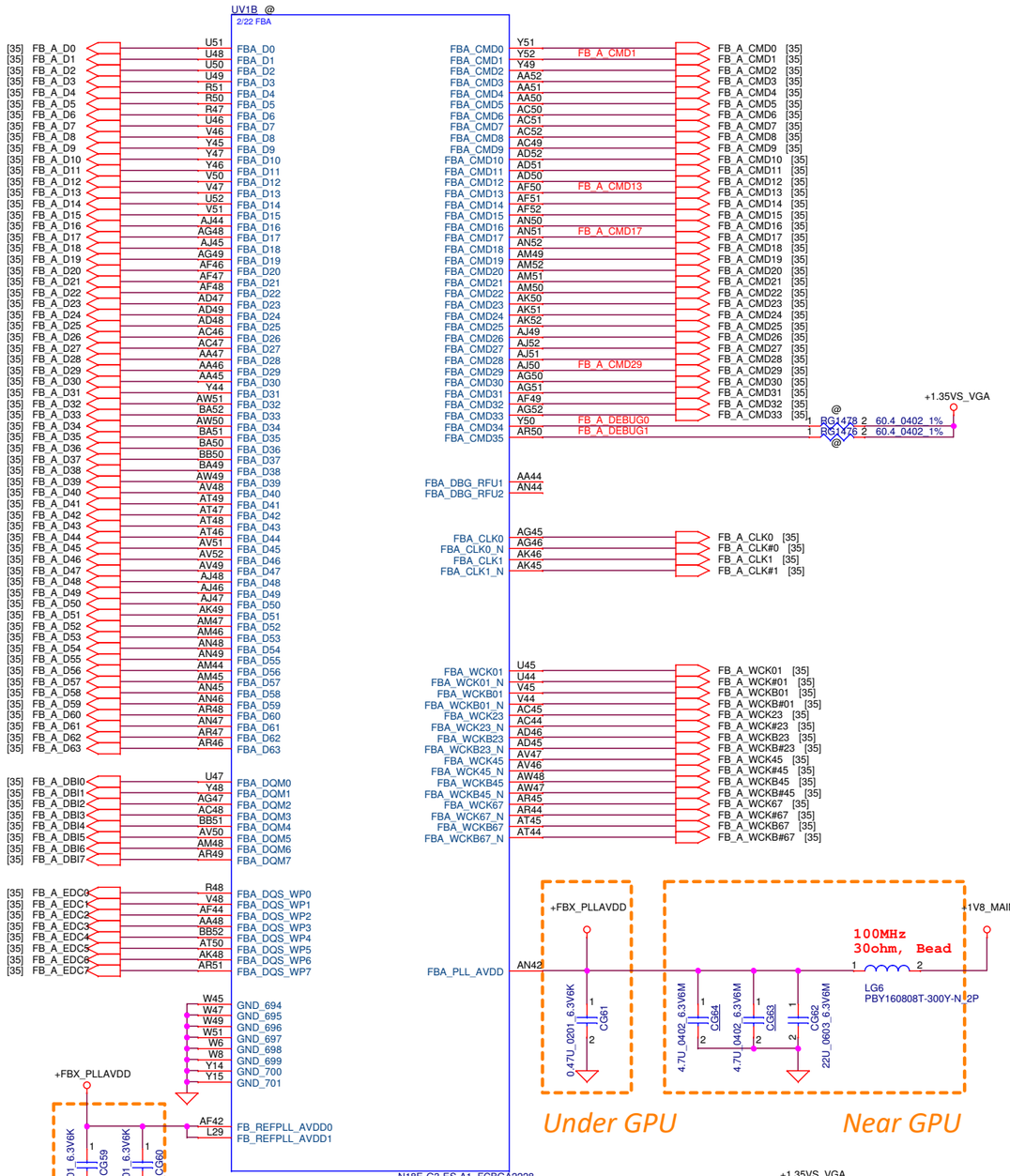

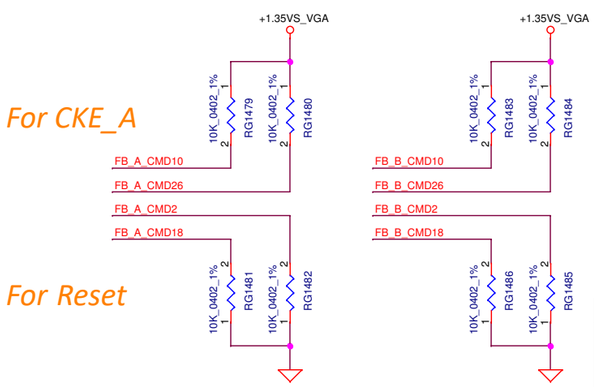

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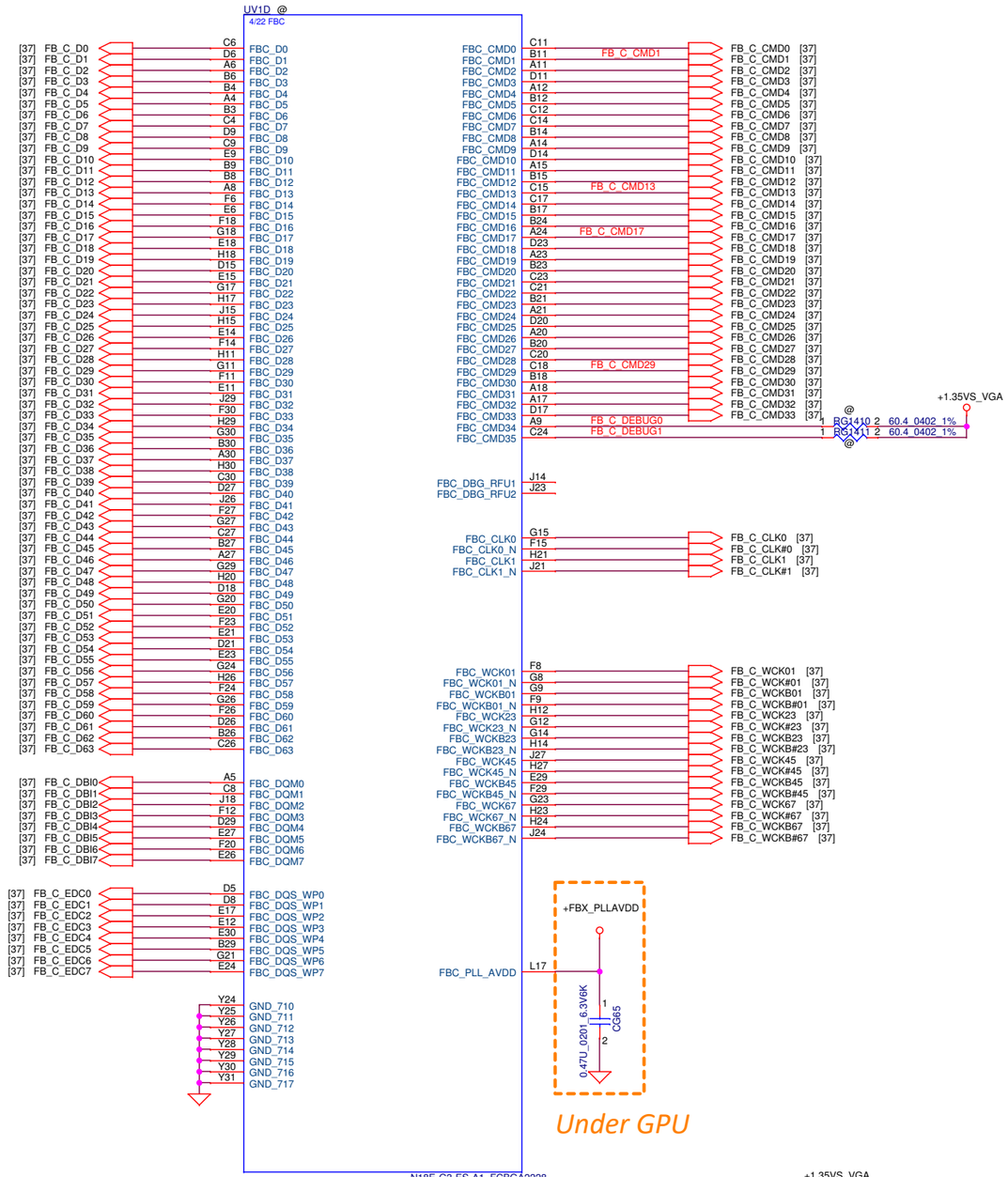
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: N18E(8/9) MEM Interface_AB			
Size	Document Number: LA-G132P		Rev: 1.0
Date: Wednesday, January 09, 2019	Sheet 31 of 81		



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Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: N18E(9/9) MEM Interface_CD			
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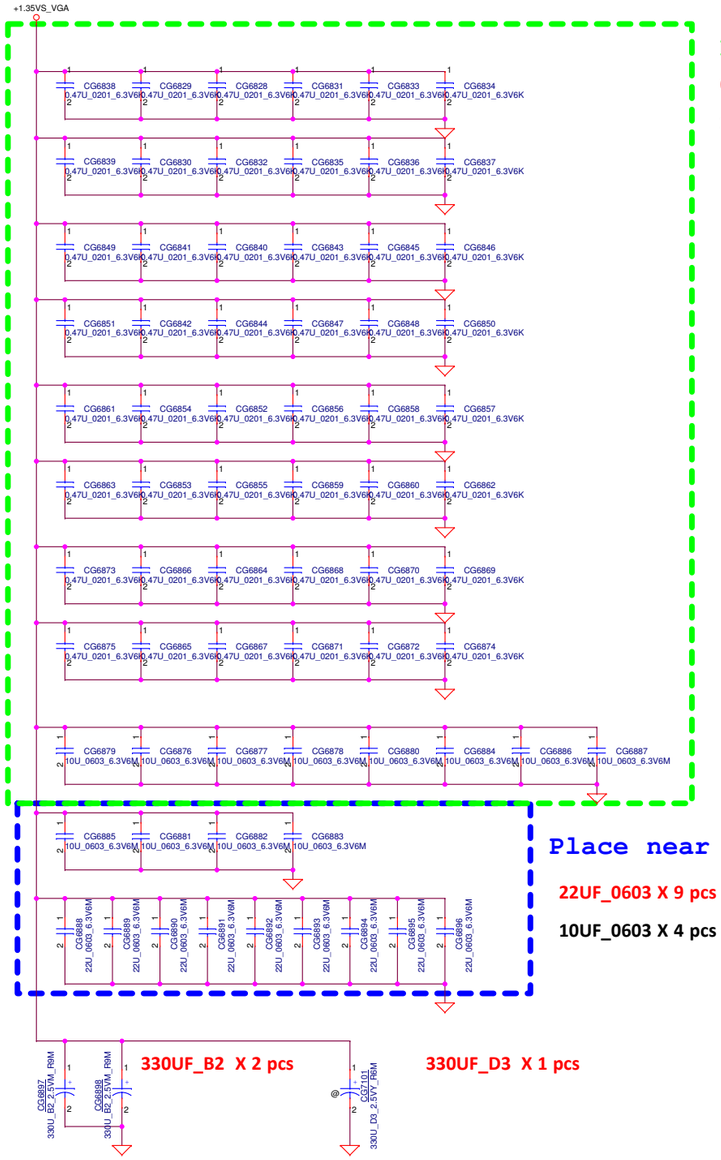
GPU Decoupling - NV Spec Recommendation

FBVDDQ_GPU



Place under GPU

0.47UF_0201 X 48 pcs

10UF_0603 X 8 pcs

Place near GPU

22UF_0603 X 9 pcs

10UF_0603 X 4 pcs

330UF_B2 X 2 pcs

330UF_D3 X 1 pcs

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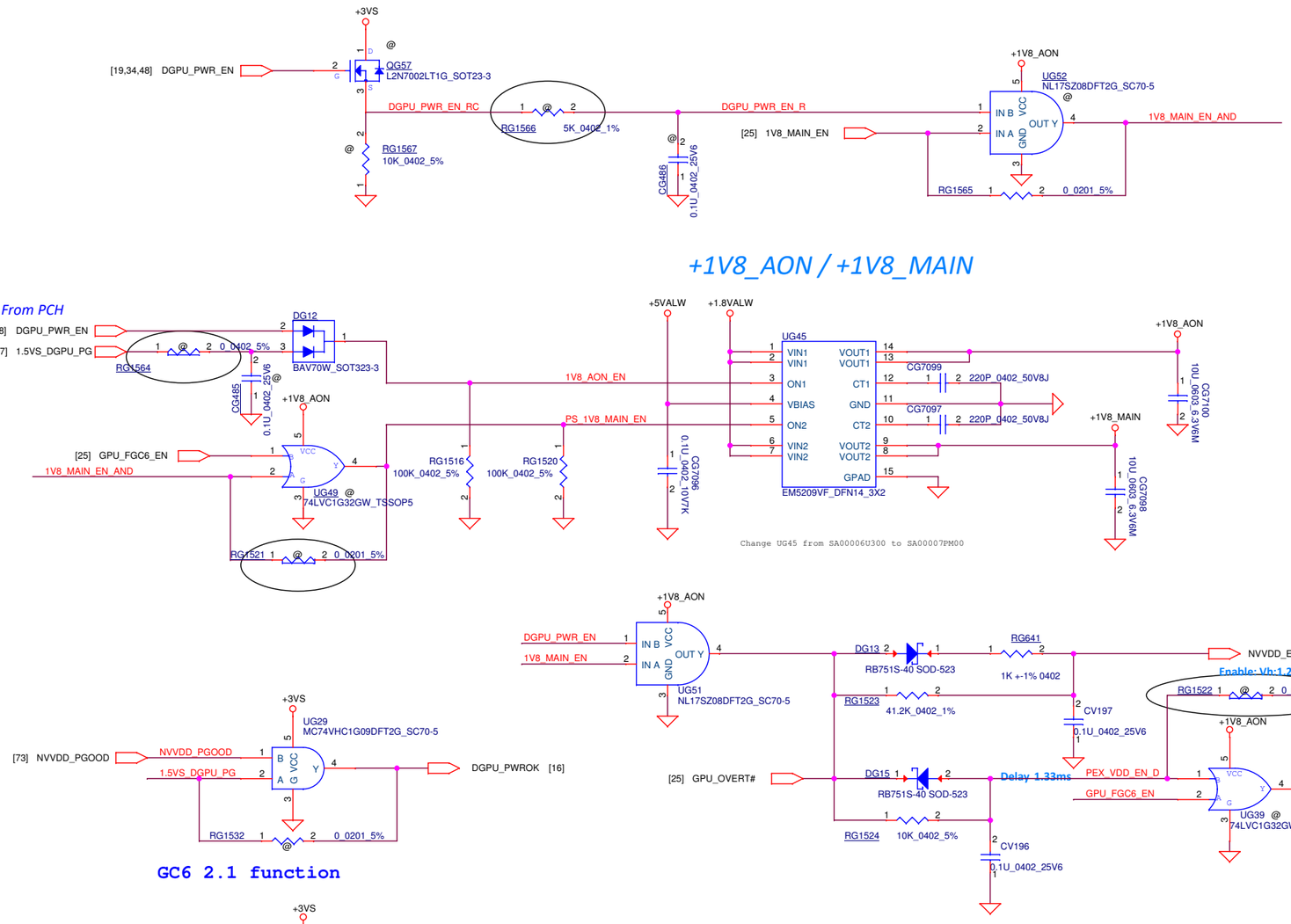
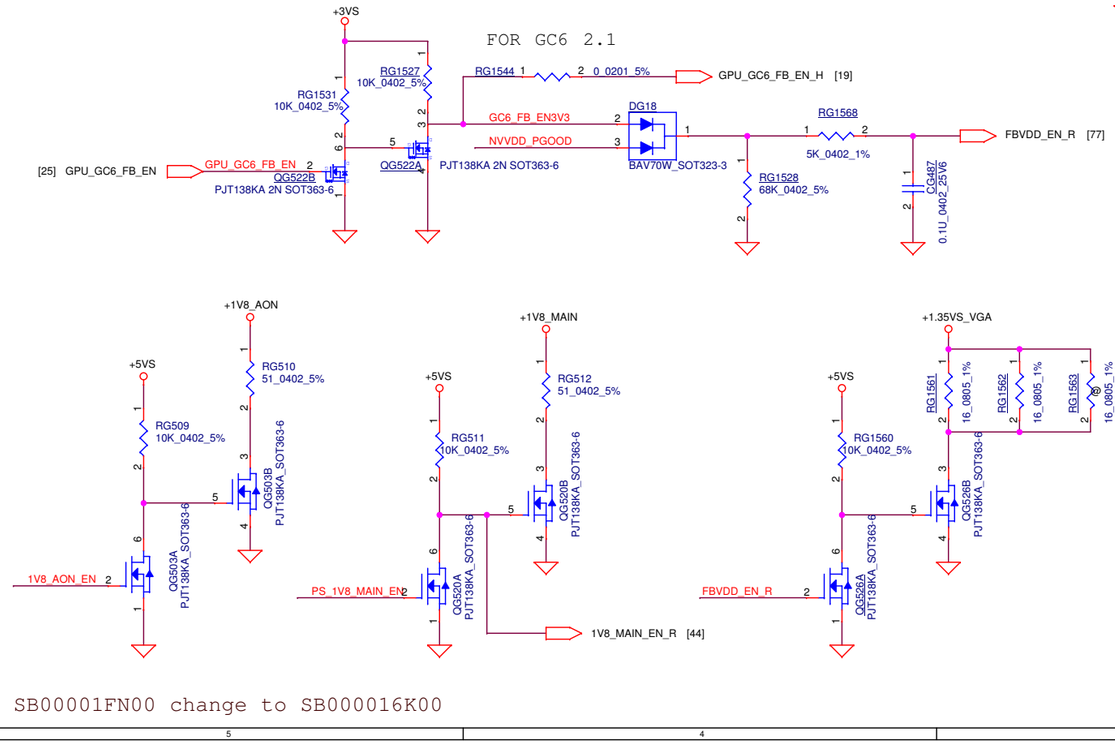


+1V8_AON / +1V8_MAIN



SB00001FN00 change to SB000016K00

	1V8_AON	1V8_MAIN	NVVDD	PEXVDD	FBVDD
GC6 2.1	ON	OFF	OFF	OFF	ON
FGC6	ON	ON	OFF	ON	ON

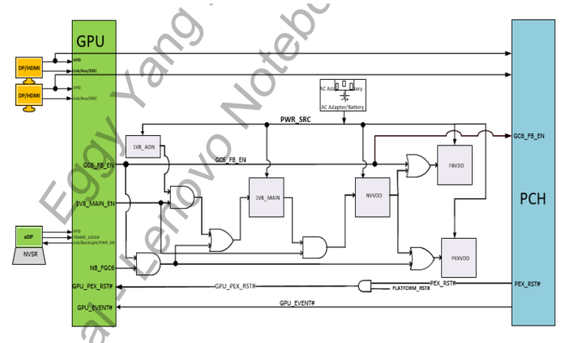


Figure 6.11 FGC6 Block Diagram

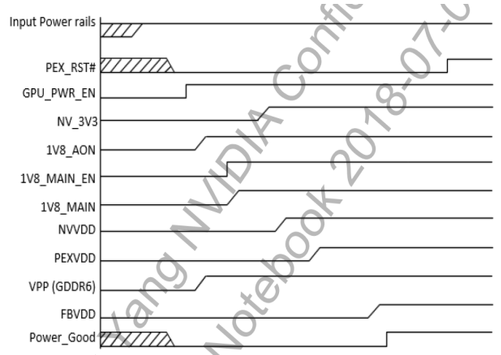


Figure 5.6 Power-Up Sequence

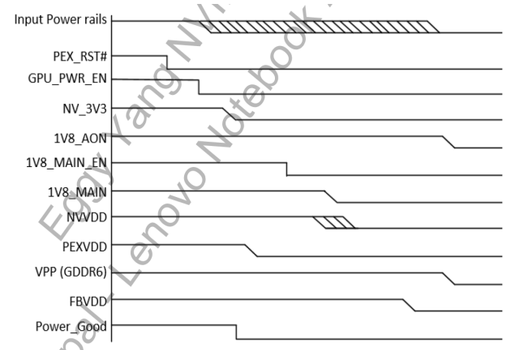
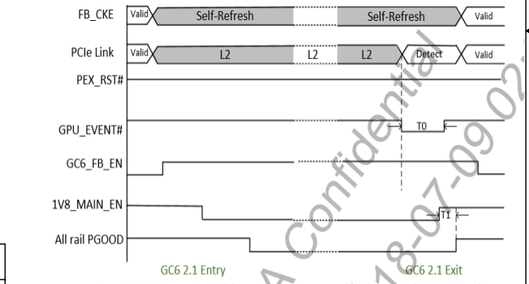


Figure 5.7 Power-Down Sequence



Note 1: GPU_EVENT# assertion and de-assertion event is required for GPU initiated GC6 2.1 Exit only.

Figure 6.12 GC6 2.1 Entry/Exit Sequence Timing Diagram

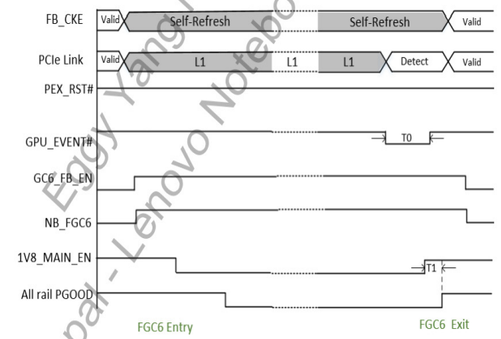


Figure 6.13 FGC6 Entry /Exit Timing Diagram

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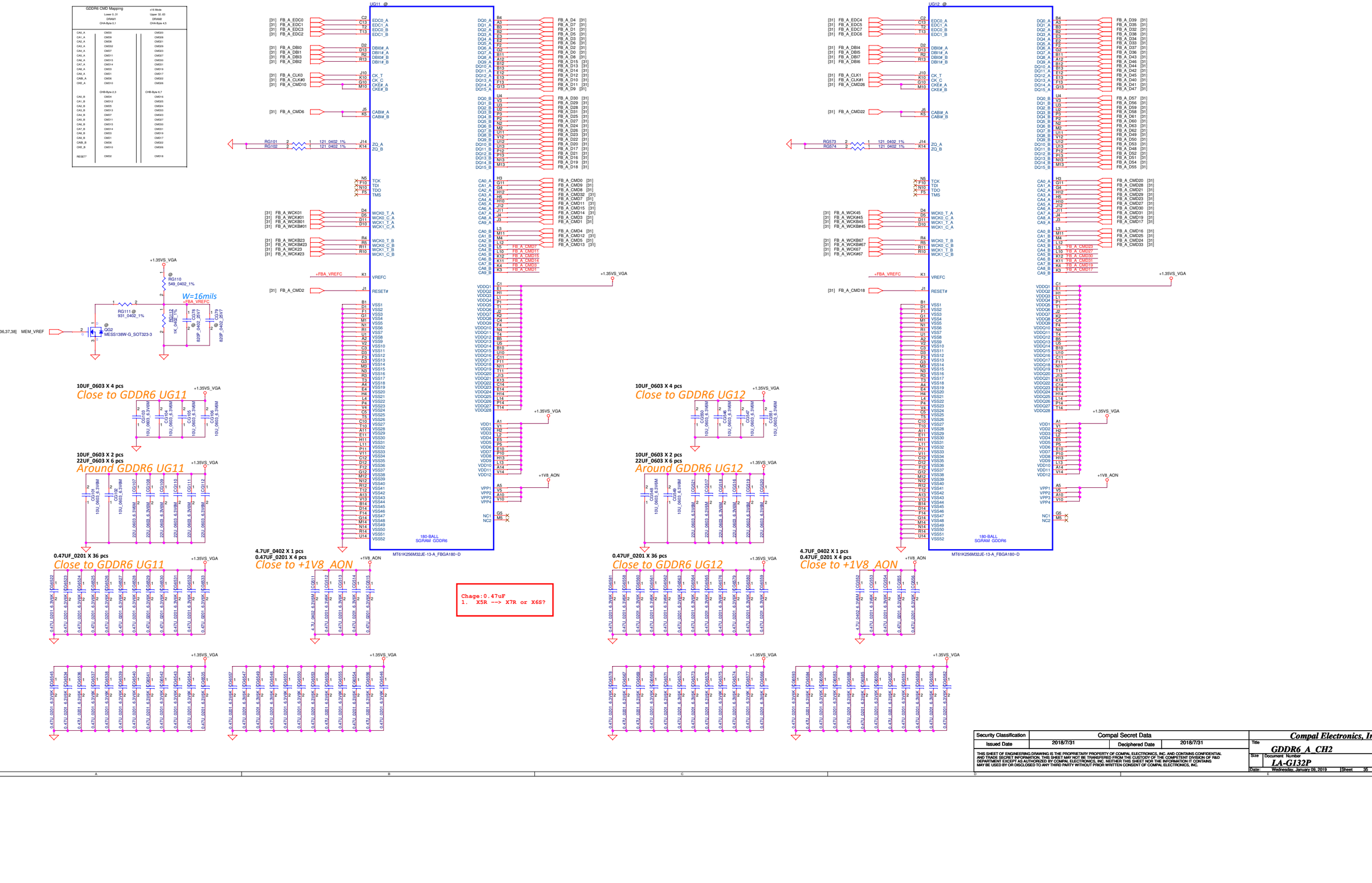
VRAM A

GDDR6 CMD Mapping		x16 Mode	
	Lower 8..31		Upper 32..63
	DRAM1		DRAM2
	CHA-Byte 0,1		CHA-Byte 4,5
CA0_A	CMD0		CMD20
CA1_A	CMD9		CMD28
CA2_A	CMD8		CMD21
CA3_A	CMD32		CMD29
CA4_A	CMD7		CMD23
CA5_A	CMD11		CMD27
CA6_A	CMD10		CMD30
CA7_A	CMD14		CMD31
CA8_A	CMD3		CMD19
CA9_A	CMD1		CMD17
CABI_A	CMD6		CMD22
CKE_A	CMD15		CMD26
	CHB-Byte 2,3		CHB-Byte 6,7
CA0_B	CMD4		CMD16
CA1_B	CMD12		CMD25
CA2_B	CMD5		CMD24
CA3_B	CMD13		CMD33
CA4_B	CMD7		CMD27
CA5_B	CMD11		CMD30
CA6_B	CMD10		CMD31
CA7_B	CMD14		CMD19
CA8_B	CMD3		CMD17
CA9_B	CMD1		CMD22
CABI_B	CMD6		CMD26
CKE_B	CMD15		CMD18
RESET*	CMD2		CMD18



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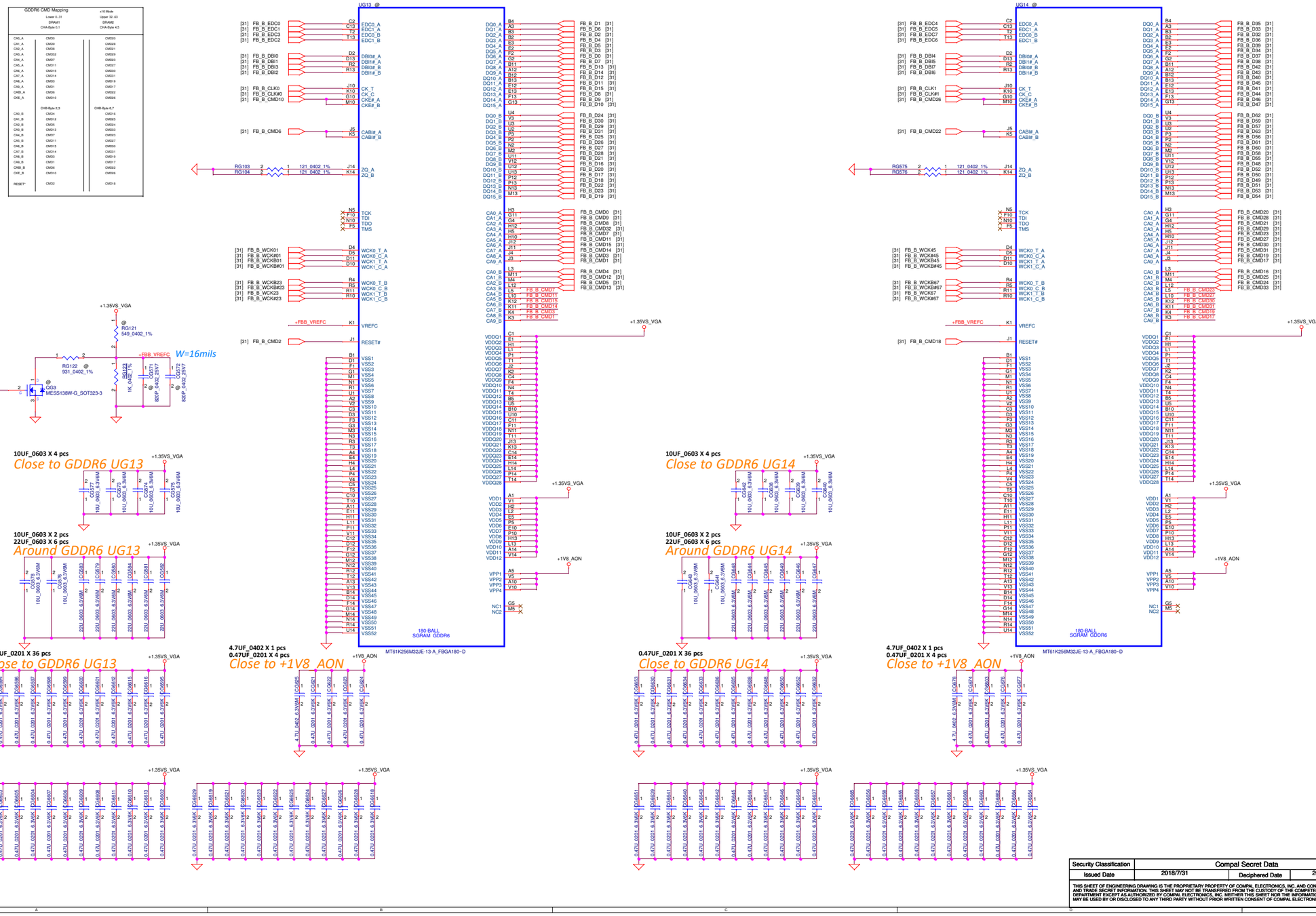
VRAM B



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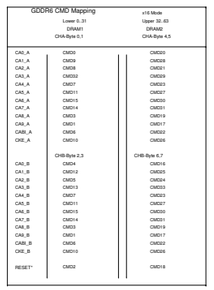
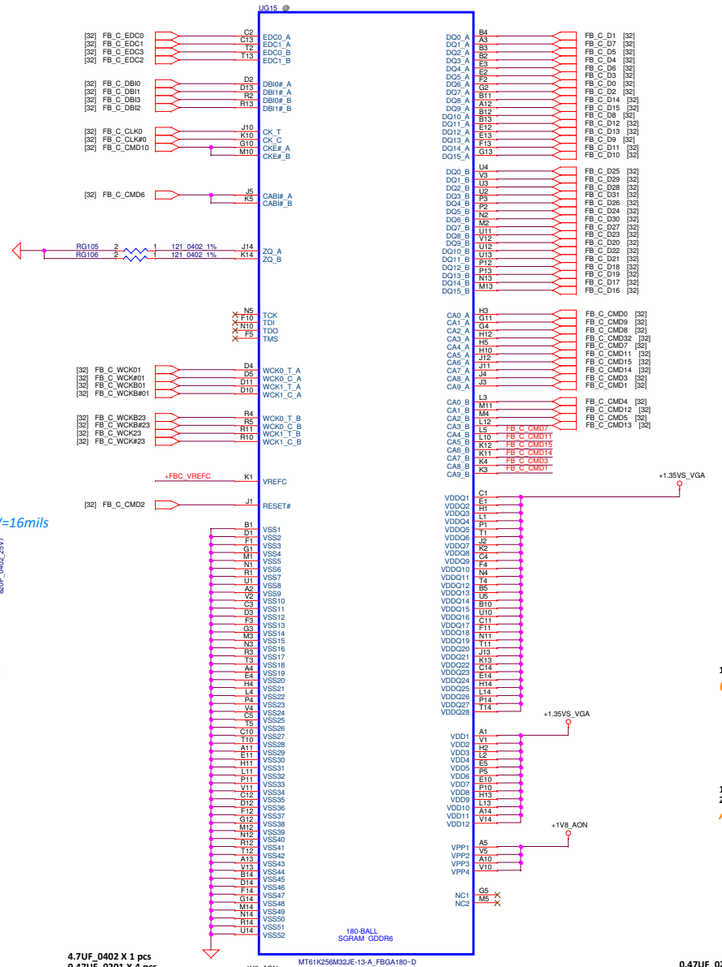
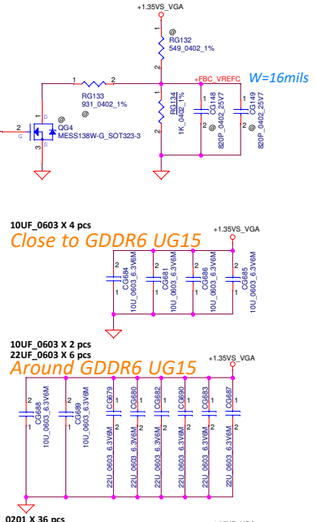
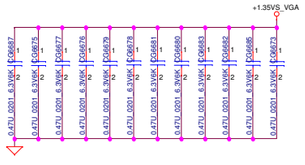
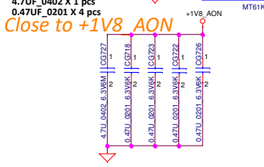
VRAM C

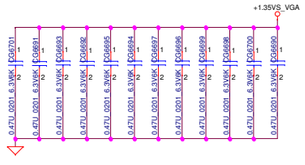


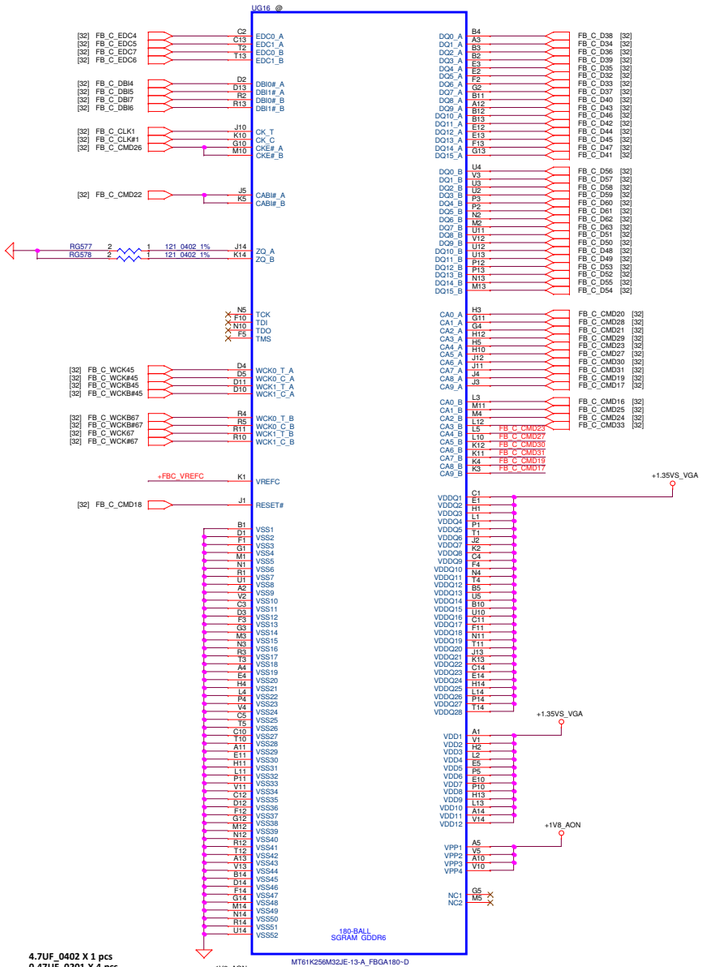


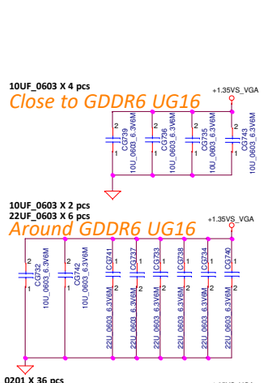


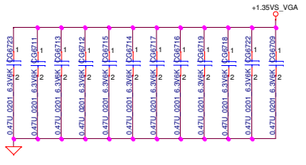












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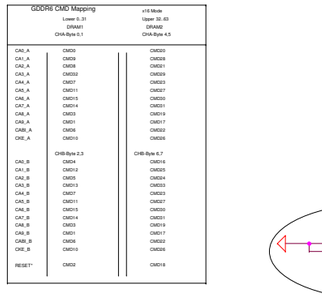
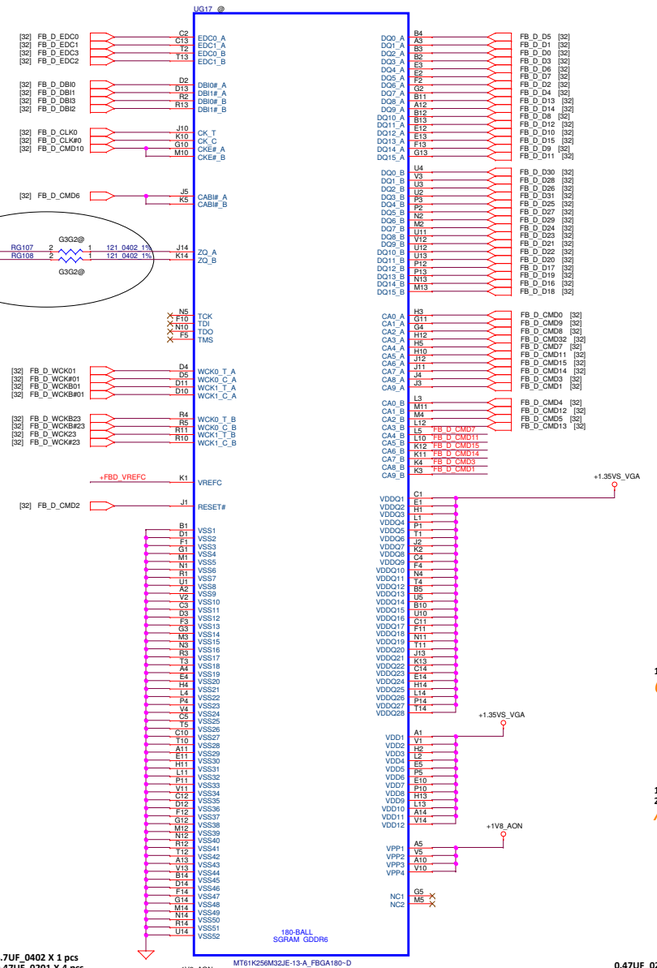
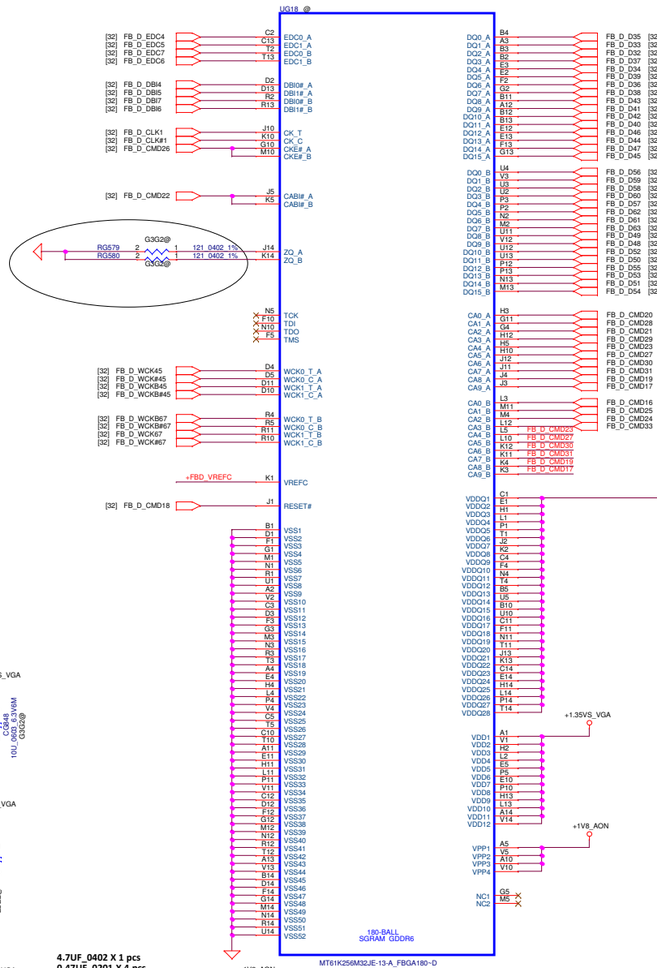
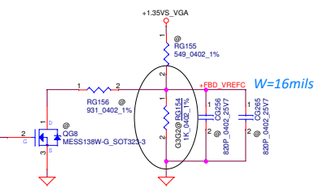
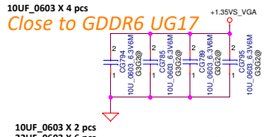
VRAM D (N18G1,N18G0 No Need)

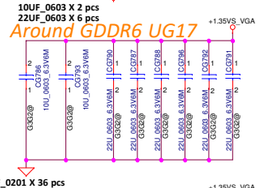


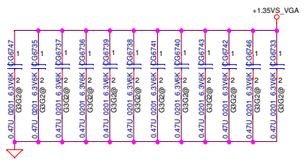




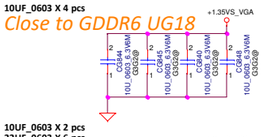


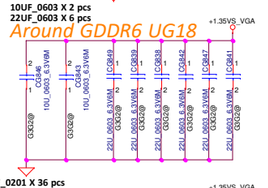


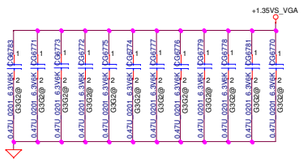


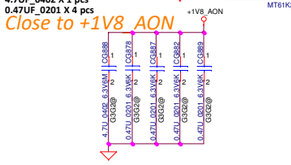


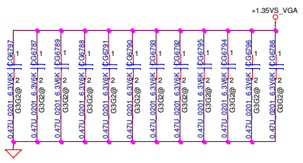
Chage:0.47uF
1. 0401 --> 0201
2. X5R --> X7R or X6S











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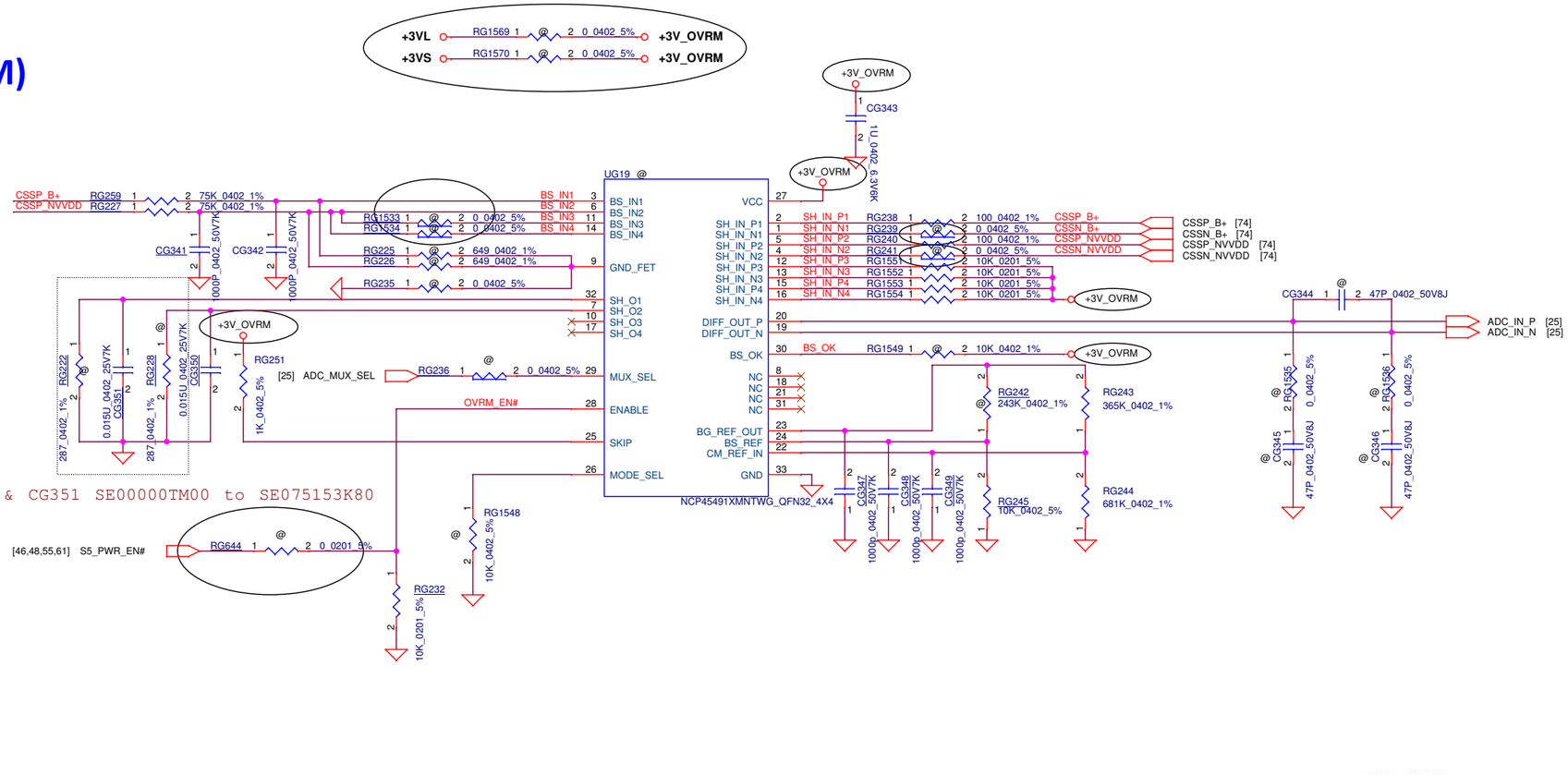
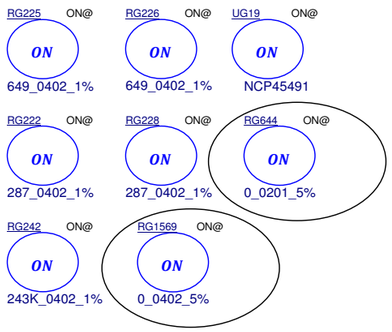
Power Monitor(OVR-M)



OVR-M(OnSemi)



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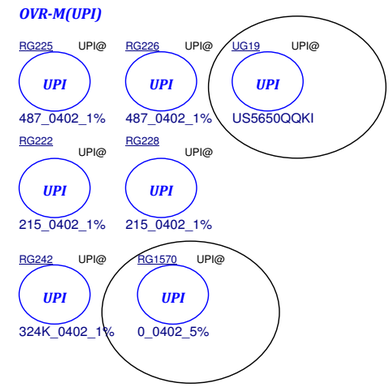

Table 13. Power Monitoring with OnSemi OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
115W to 130W	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
100W to 110W	649 Ω	221 Ω	243 kΩ	75 kΩ	1.0 nF
75W to 90W	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
70W or lower	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF

NV location	R954, R924	R977, R923	R950	R953, R952	C841, C836
Y740 location	RG225, RG226	RG222, RG228	RG242	RG259, RG227	CG341, CG342

ON (X7678038L59)		
UG19	SA0000C9Q00	S IC NCP45491XMNTWG QFN 32P MONITOR
RG225, RG226	SD000008O80	S RES 1/16W 649 +-1% 0402
RG222, RG228	SD034287080	S RES 1/16W 287 +-1% 0402
RG242	SD000004200	S RES 1/16W 243K +-1% 0402

Table 14. Power Monitoring with uPI OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	487 Ω	127 Ω	324 kΩ	75 kΩ	1.0 nF
115W to130W	487 Ω	143 Ω	324 kΩ	75 kΩ	1.0 nF
100W to 110W	487 Ω	165 Ω	324 kΩ	75 kΩ	1.0 nF
75W to 90W	487 Ω	215 Ω	324 kΩ	75 kΩ	1.0 nF
70W or lower	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF

NV location	R954, R924	R977, R923	R950	R953, R952	C841, C836
Y740 location	RG225, RG226	RG222, RG228	RG242	RG259, RG227	CG341, CG342

uPI (X7678038L60)		
UG19	SA0000CEV00	S IC US5650PQKI WQFN 32P POWER MONITOR
RG225, RG226	SD00000EL80	S RES 1/16W 487 +-1% 0402
RG222, RG228	SD000000180	S RES 1/16W 215 +-1% 0402
RG242	SD034324380	S RES 1/16W 324K +-1% 0402

Reference ORB R997 ,R923

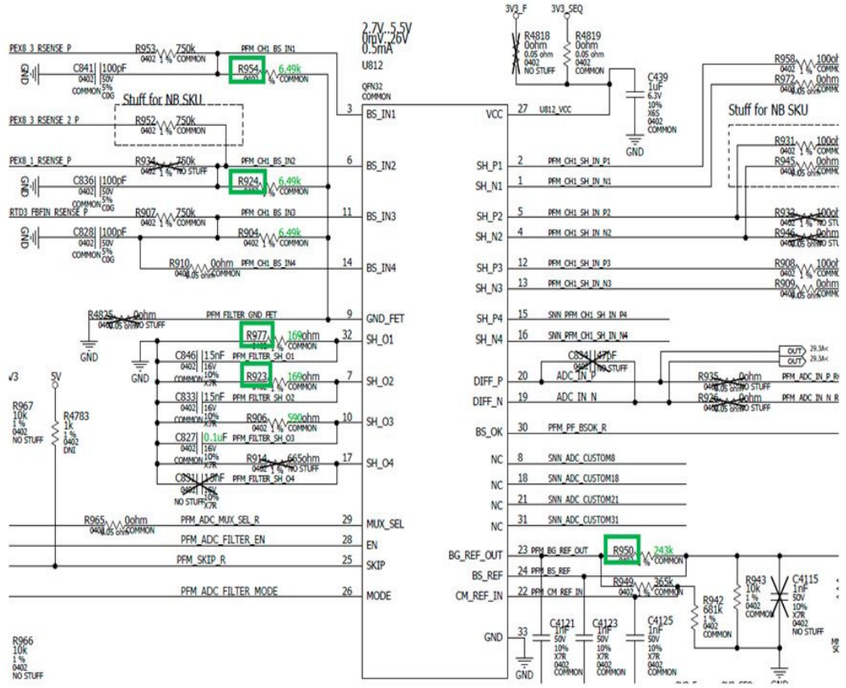

Figure 1. Power Monitoring with OVR-M

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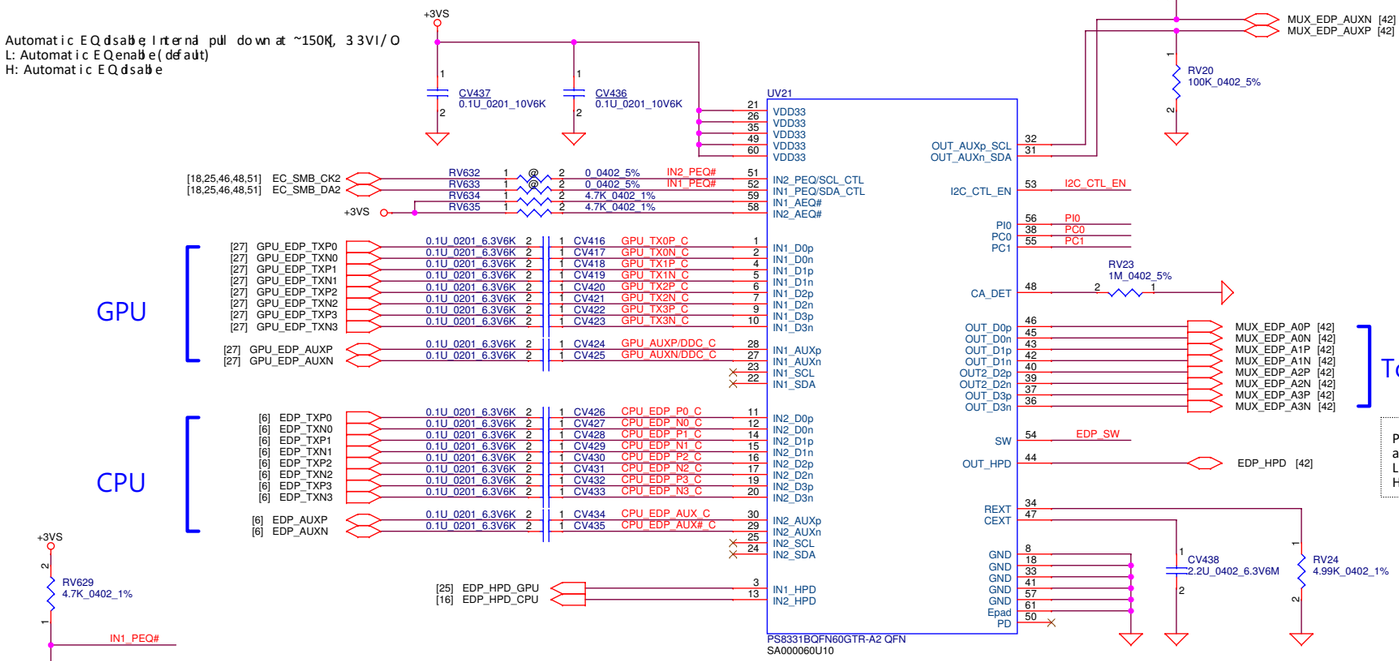
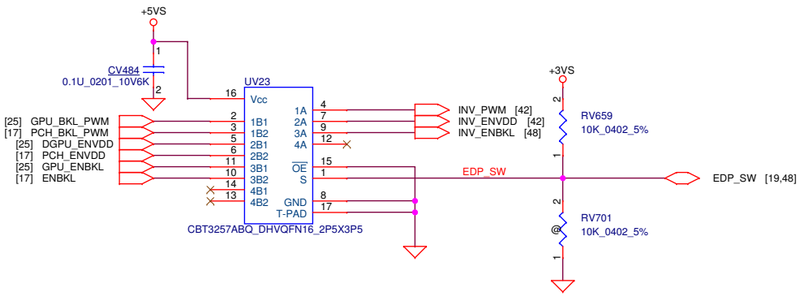
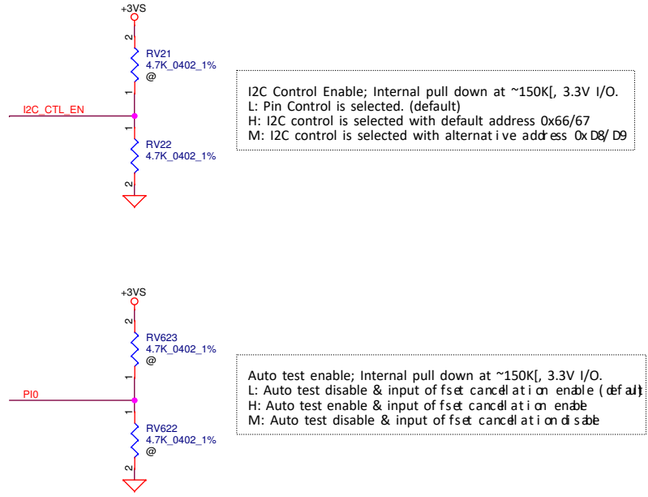
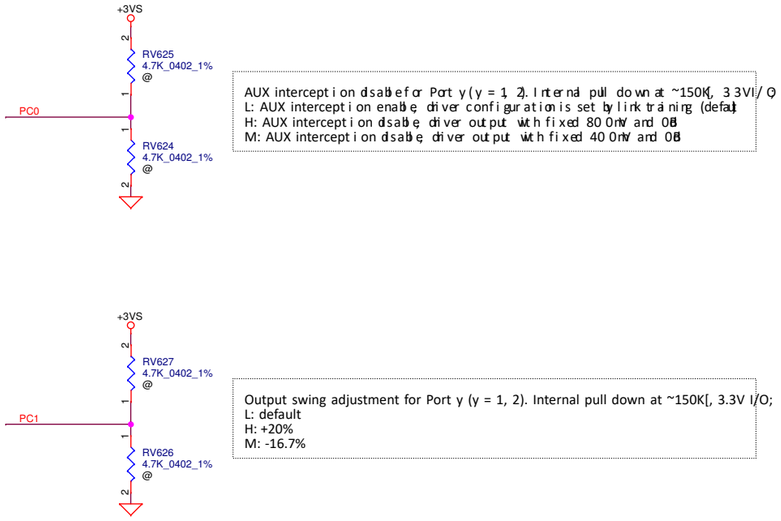


Programmable input equalization levels; Internal pull down at ~150K[, 3.3VI/O
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2



S1	OE	output	function
L	L	A=B1	DGPU
H	L	A=B2	IGPU
X	H		





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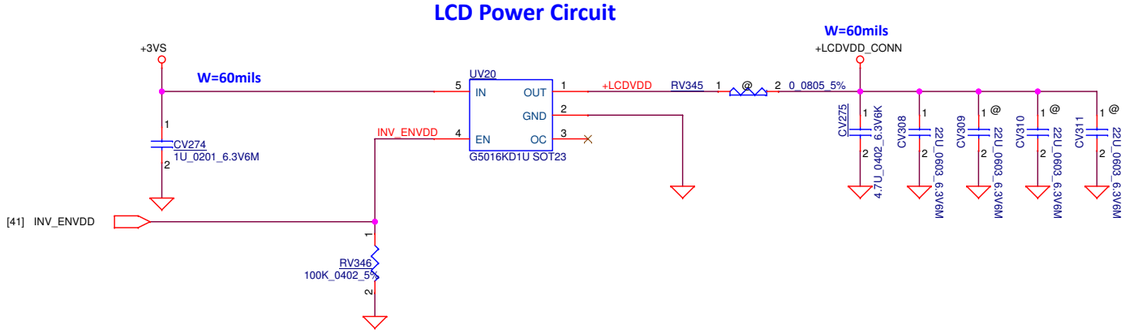
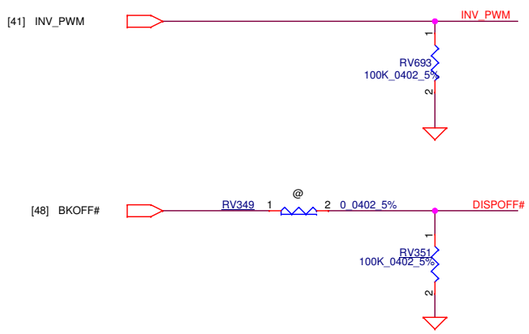
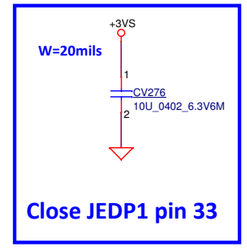
LCD Power Circuit

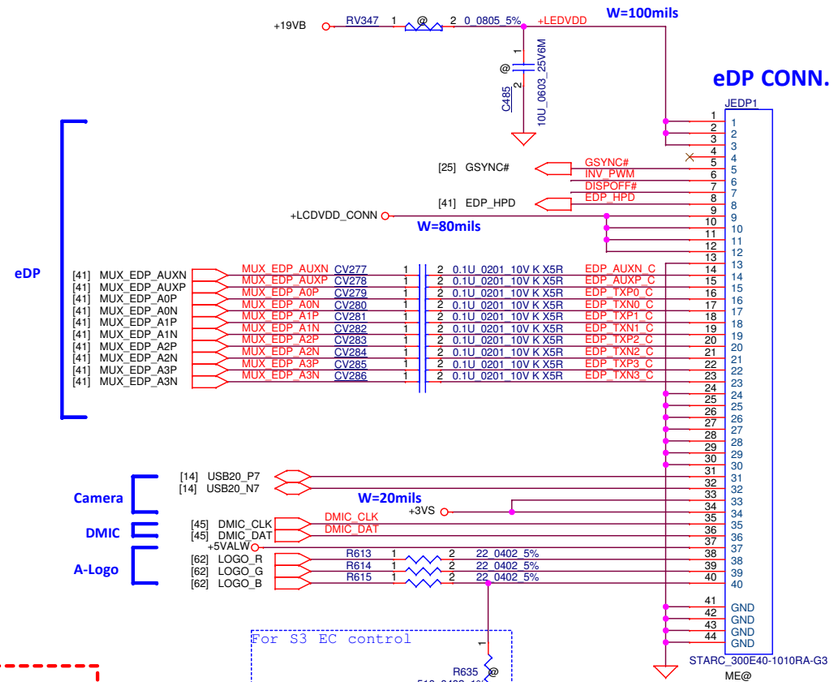




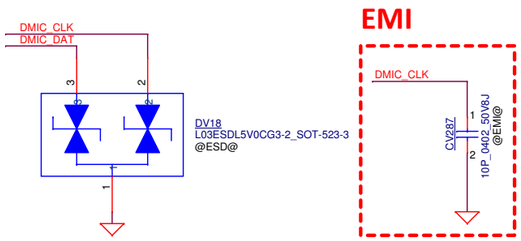
Camera

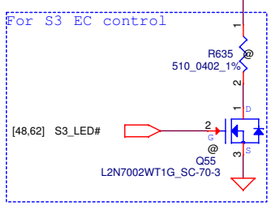


eDP CONN.



EMI





Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **eDP / Camera**

Size	Document Number	Rev
C	LA-G132P	1.0

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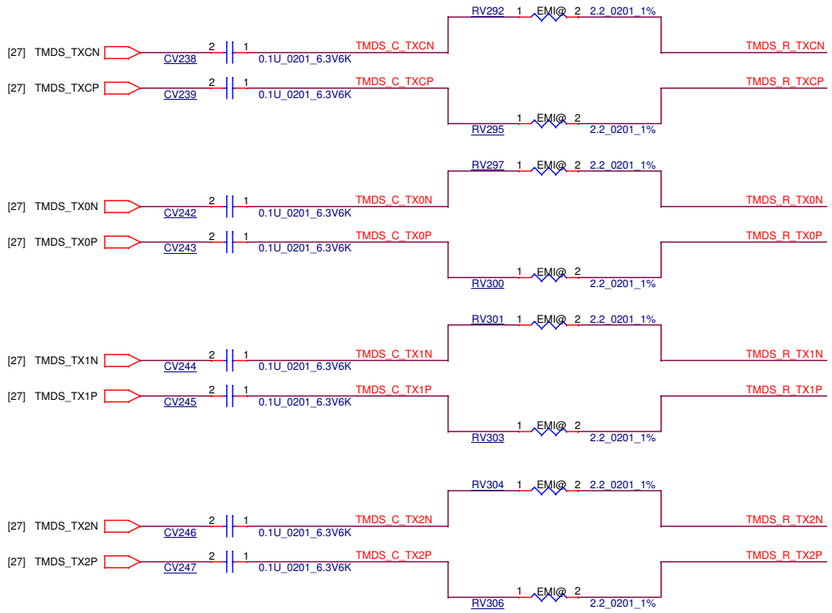

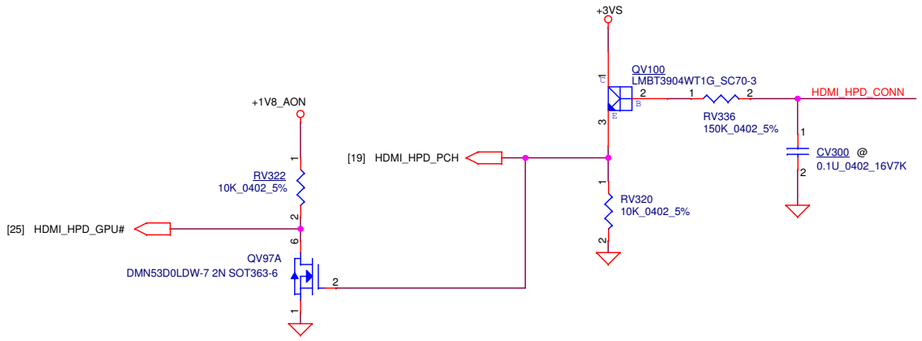

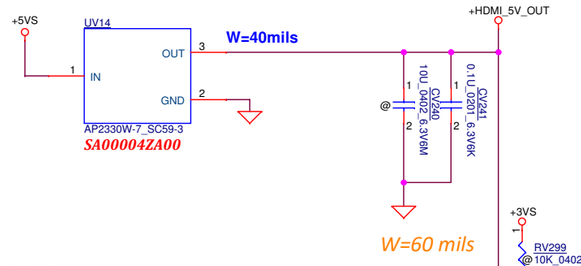

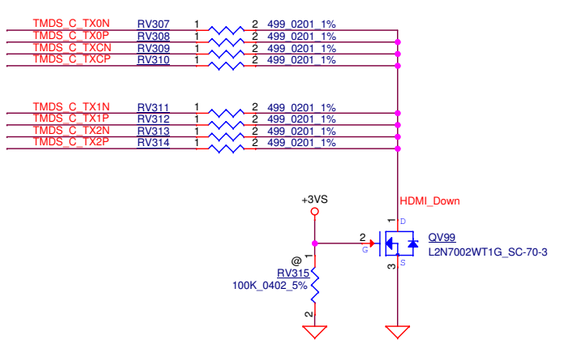

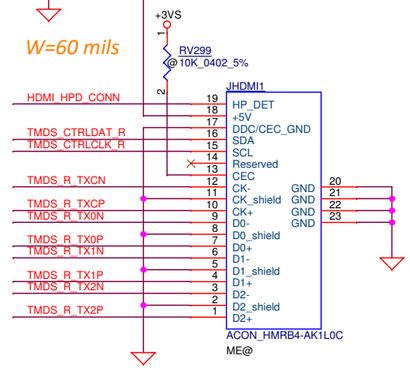

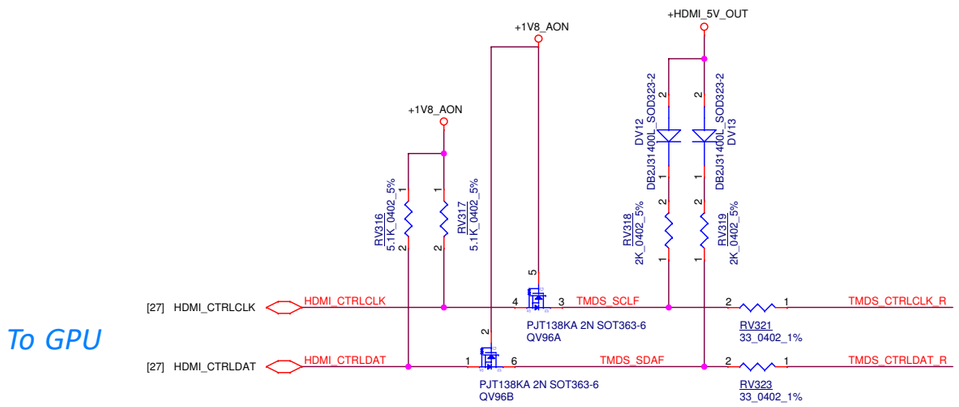

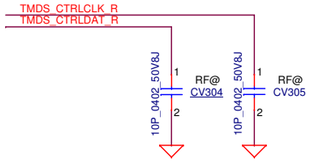

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.	
Title	HDMI
Size	Document Number: LA-G132P
Rev	1.0
Date:	Wednesday, January 09, 2019
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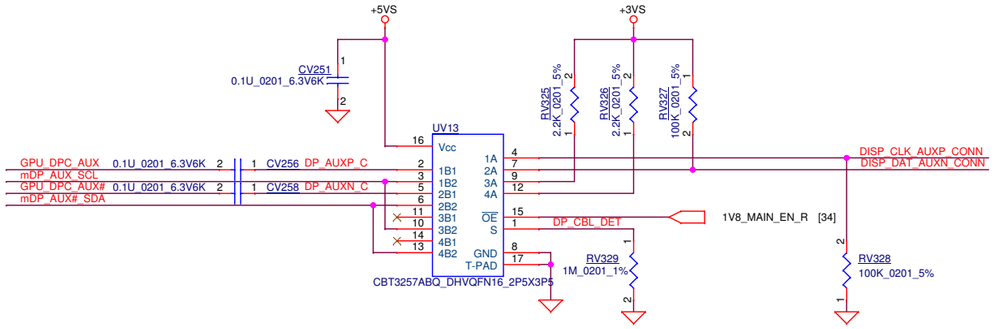

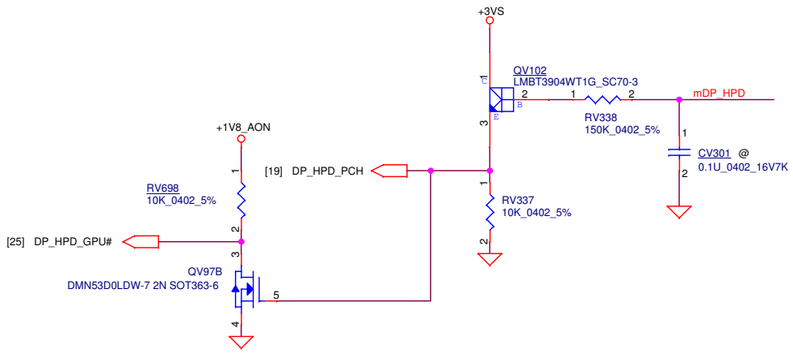

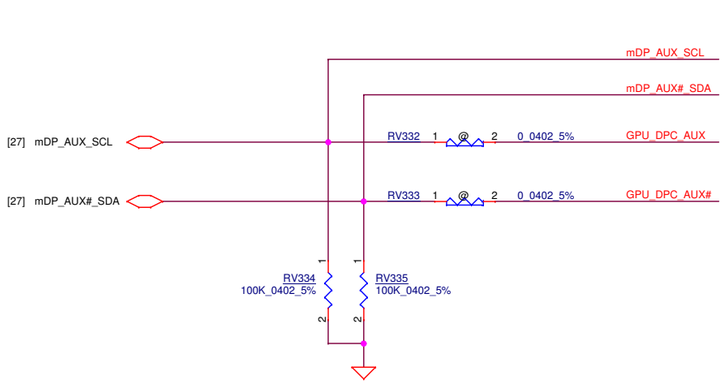

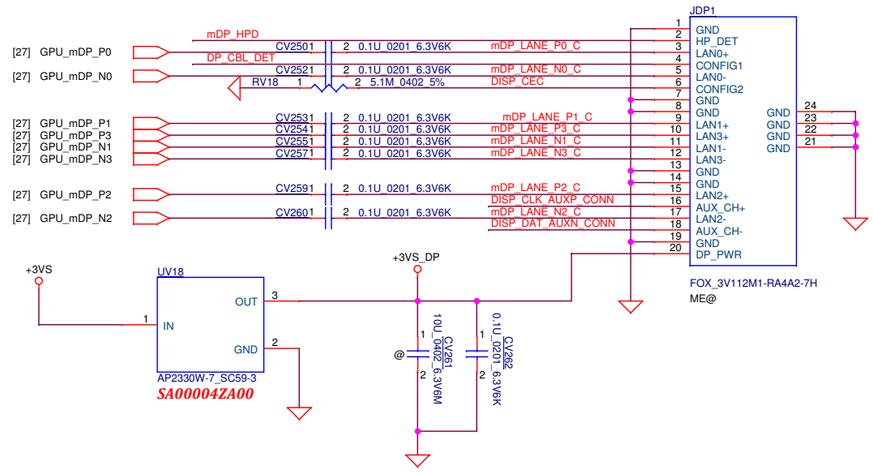

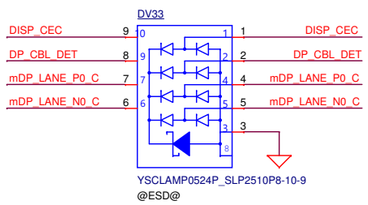

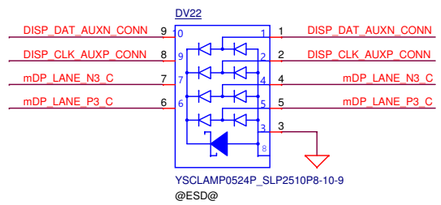

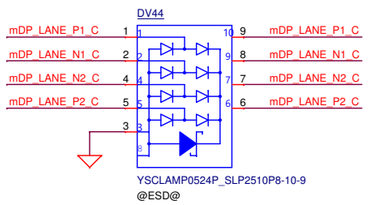

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: miniDP			
Size	Document Number: LA-G132P		Rev: 1.0
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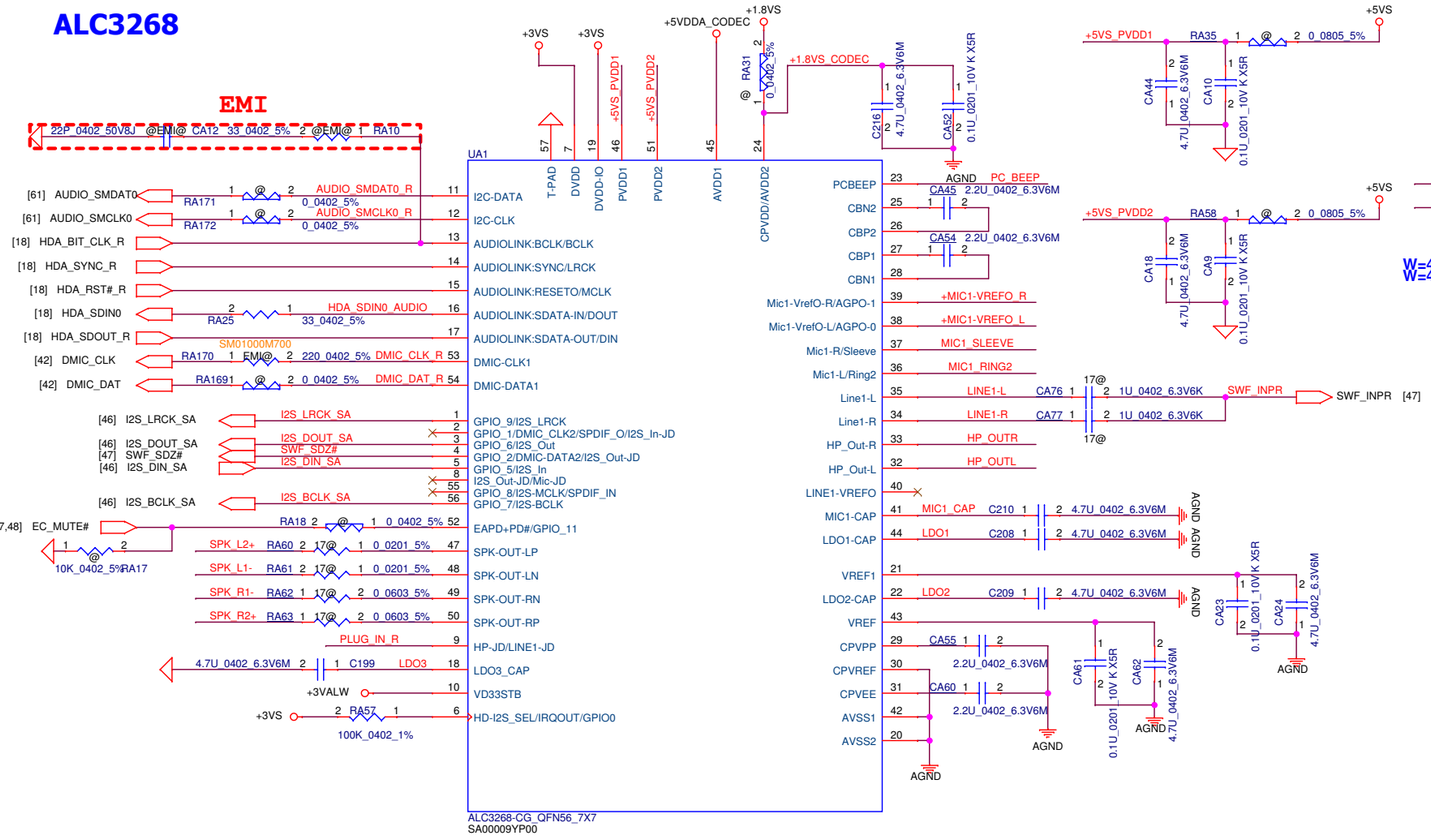
ALC3268



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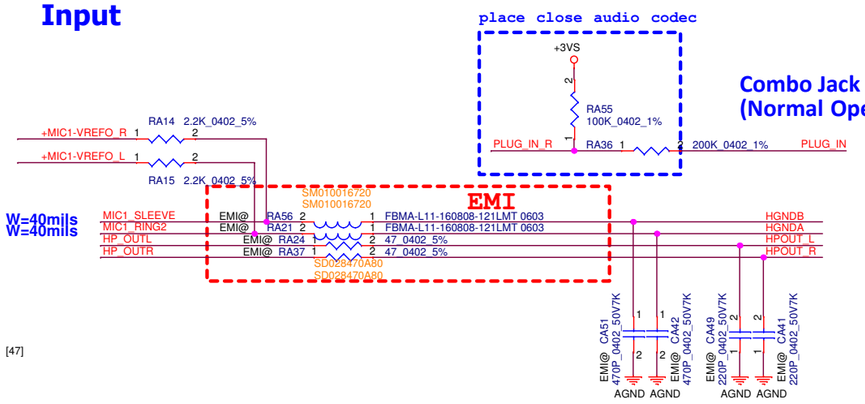
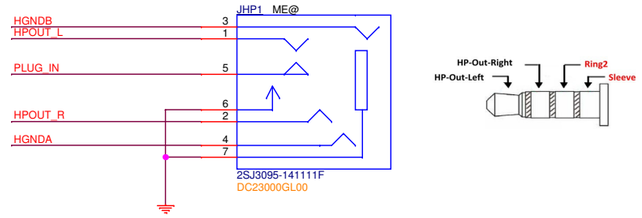
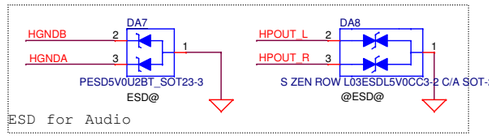
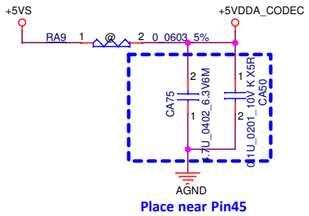


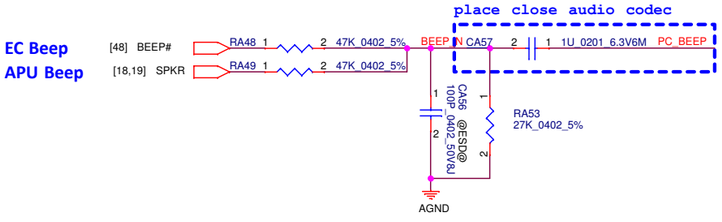




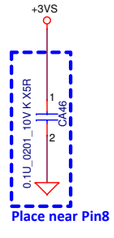
Change SCA00002900 to SCA00000T00

+5VS for +5VDDA_CODEC

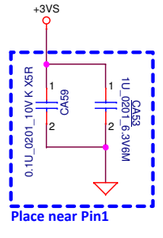


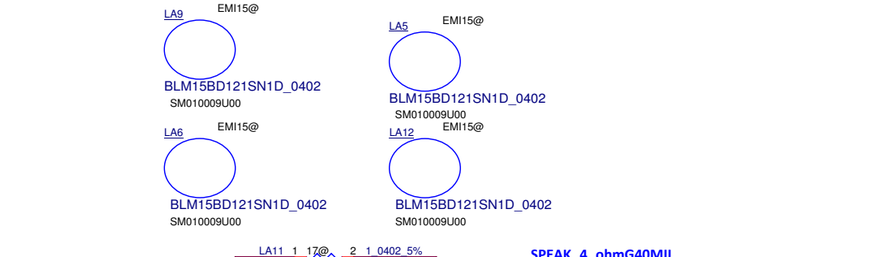


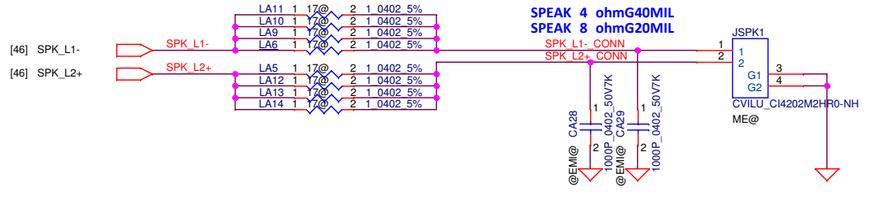
+3VS for +IOVDD_CODEC



+3VS for +3VDD_CODEC







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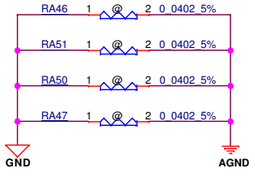
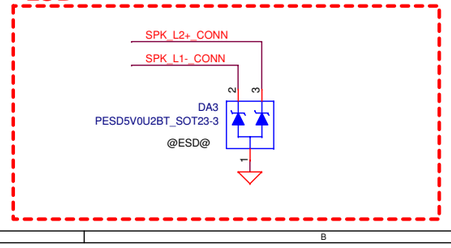
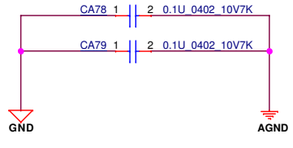
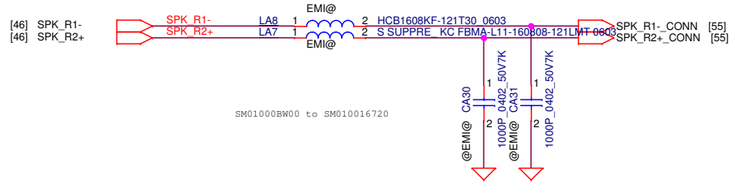


ESD







Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title	HD Audio Codec_ALC3268		
Size C	Document Number LA-G132P		Rev 1.0
Date: Wednesday, January 09, 2019	Sheet 45 of 81		

TAS5766 Smart Amp for 15" only

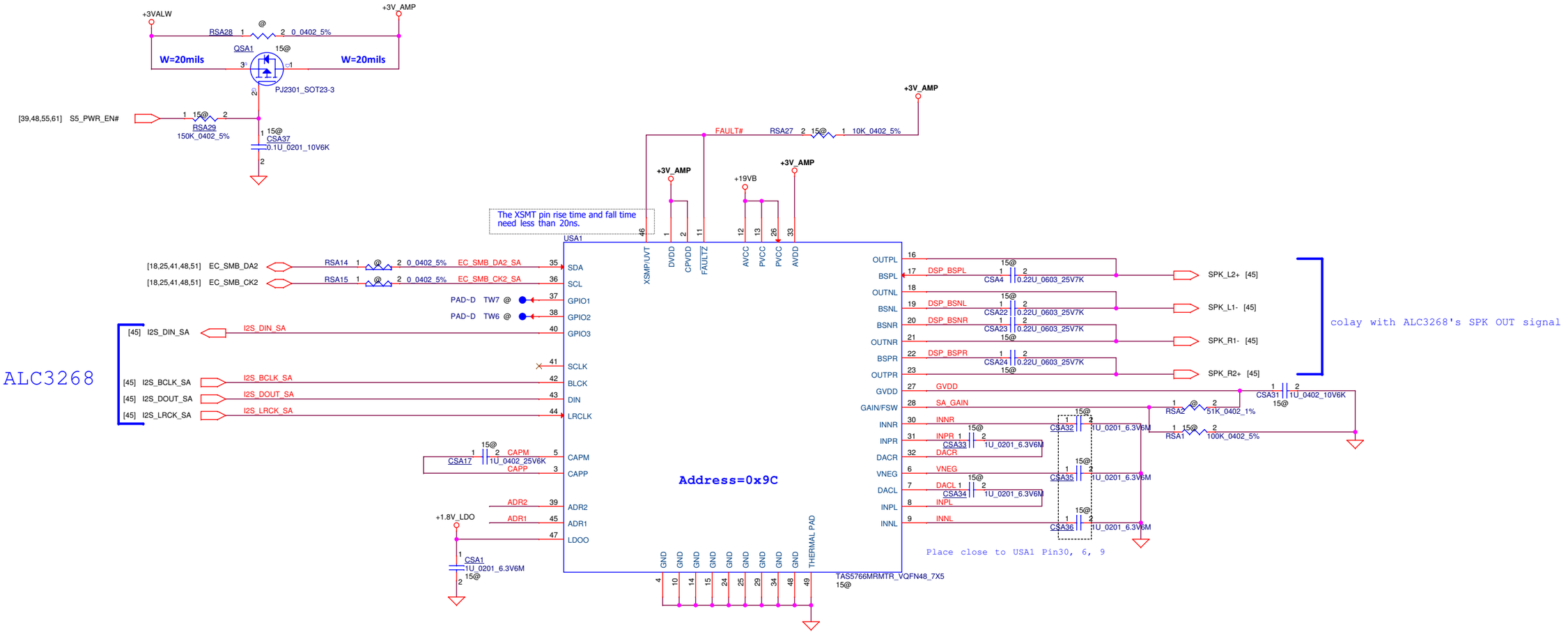


Table 22. Gain and FSW

Ra (to GND)	Rb (to GVDD)	INPUT IMPEDANCE	GAIN	FSW – RATIO TO LRCLK	FSW w. 44.1 kHz	FSW w. 48 kHz
10 0kΩ	OPEN	120 kΩ	14 dB	8	353 kHz	384 kHz
20 kΩ	100 kΩ	120 kΩ	14 dB	10	441 kHz	480 kHz
38 kΩ	100 kΩ	120 kΩ	14 dB	12	529 kHz	576 kHz
47 kΩ	75 kΩ	120 kΩ	14 dB	16	706 kHz	768 kHz
51 kΩ	51 kΩ	60 kΩ	20 dB	8	353 kHz	384 kHz
75 kΩ	47 kΩ	60 kΩ	20 dB	10	441 kHz	480 kHz
100 kΩ	39 kΩ	60 kΩ	20 dB	12	529 kHz	576 kHz
100 kΩ	20 kΩ	60 kΩ	20 dB	16	706 kHz	768 kHz

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.	
Title	Smart Amp TAS5766
Size / Document Number	LA-G132P
Rev	1.0
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ALC1304 Subwoofer Amp for 17" only

Gain/SLV Setting			
Master Mode	Gain	RSWF4	RSWF8
	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	15dB	55K	35K

SDZ Control	
Low	Power down
High	Normal

Mute Control	
Low	Normal
High	Mute

AM Avoidance Setting		
PWM Fsw	AM0	AM1
400KHz	L	L
500KHz	H	L
600KHz	L	H
1000KHz	H	H

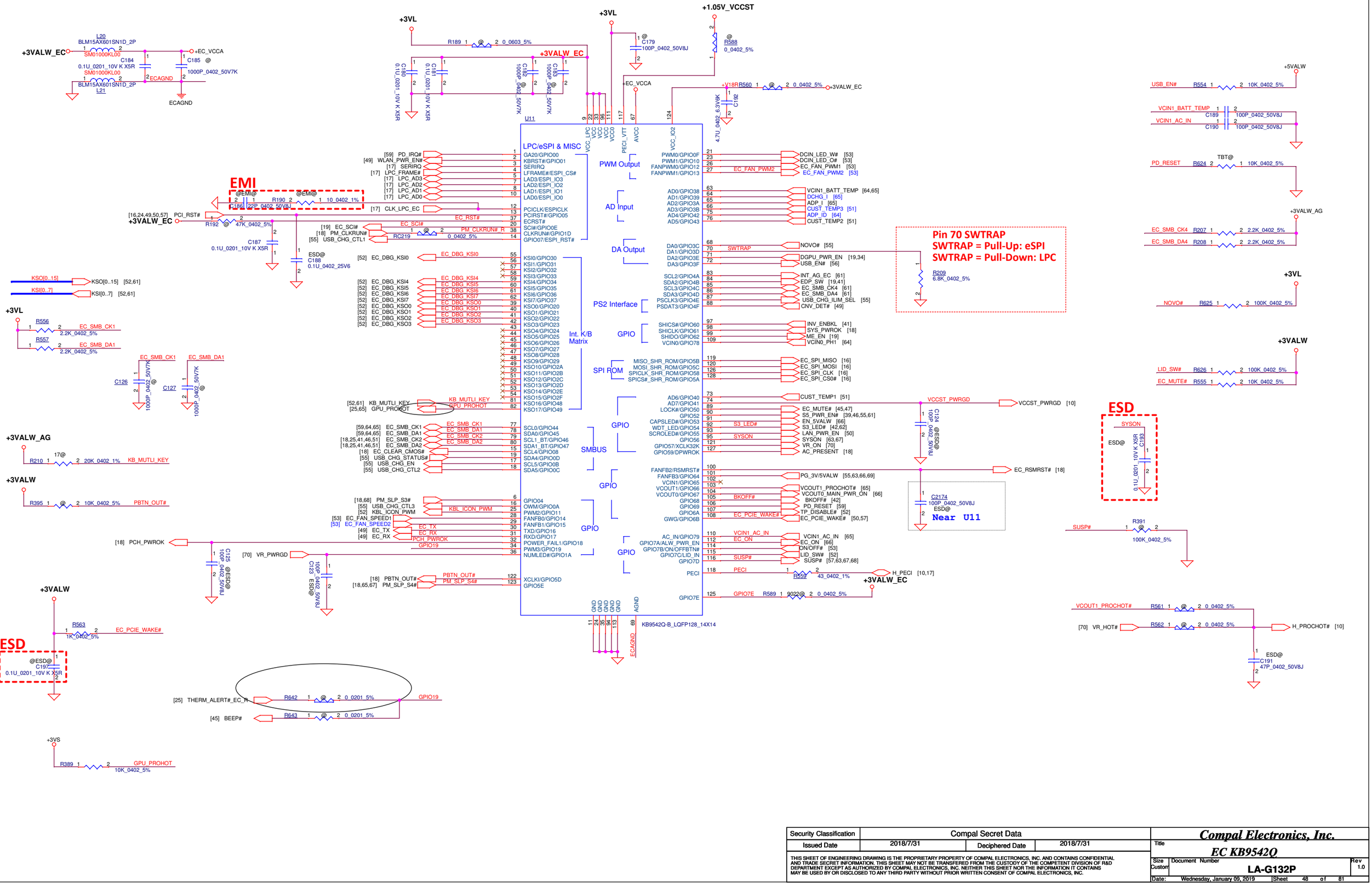
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: Subwoofer ALC1304

Size | Document Number: LA-G132P | Rev: 1.0

Date: Wednesday, January 09, 2019 | Sheet 47 of 81



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

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Compal Electronics, Inc.

Title: **EC KB9542Q**

Size	Document Number	Rev
Custom	LA-G132P	1.0

Date: Wednesday, January 09, 2019 | Sheet 48 of 81

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]

Jefferson Peak:1360mA@peak current
Thunder_Peak_2:1100mA@peak current

For Power consumption Measurement

422.18mA

W=20mils W=20mils

RW40 0_0603_5% CW10 CNVI@ PJ2301_SOT23-3 RW41 150K_0402_5% CW9 0.1U_0201_10V6K CW12 0.1U_0201_10V6K CW11 10U_0402_6.3V6M

[48] WLAN_PWR_EN#

The connectivity module power supply pin shall be connected directly to thr rail DSW.
From 567240_Intel_Wireless_AC_9560_Jefferson_Peak_EPS_Rev1.1

10K_0402_5% RW42 CNV_DET#
10K_0402_5% RW18 EC_WL_OFF#_R
10K_0402_5% RW21 BT_ON_R
10K_0402_5% RW23 EC_WL_WAKE#
71.5K_0402_1% RW39 CLKREQ_CNV#
100K_0402_5% RW24 EC_TX

USB2 P14 (For Bluetooth)
[14] USB20_P14
[14] USB20_N14

CNVi Rx
[15] CNV_PRX_DTX_N1
[15] CNV_PRX_DTX_P1
[48] CNV_DET#
[15] CNV_PRX_DTX_N0
[15] CNV_PRX_DTX_P0
[15] CLK_CNV_PRX_DTX_N
[15] CLK_CNV_PRX_DTX_P

PCIe X1 (link to PICe Port 14)
[17] PCIE_PTX_DRX_P14
[17] PCIE_PRX_DTX_N14

PCIe CLK (From PCH CLKOUT3)
[15] CLK_PCIE_P3
[15] CLK_PCIE_N3
[15] WLAN_CLKREQ3#

CNVi Tx
[15] CNV_PTX_DRX_N1
[15] CNV_PTX_DRX_P1
[15] CNV_PTX_DRX_N0
[15] CNV_PTX_DRX_P0
[15] CLK_CNV_PTX_DRX_N
[15] CLK_CNV_PTX_DRX_P

KEY E

JWLAN1 — LOTES_APCI0128-P005A — ME@

1 GND		2 3.3VAUX	
3 USB_D+ / RSVD		4 3.3VAUX	
5 USB_D- / RSVD		6 LED1#	@TW1 PAD-D
7 GND		8 PCM_CLK / RSVD	
9 SIDO_CLK / WGR_D1N		10 PCM_SYNC / LCP_RSTN	CNV_RF_RESET#_R — RW6 1 @ 2 0_0201_5% — CNV_RF_RESET# [18]
11 SDIO_CMD / WGRD1P		12 PCM_IN / RSVD	CLKREQ_CNV#_R — RW8 1 @ 2 0_0201_5% — CLKREQ_CNV# [18]
13 SDO_DAT0 / RSVD		14 PCM_OUT / CLKREQ0	
15 SDO_DAT1 / WGR_D0N		16 LED2#	@ TW2 PAD-D
17 SDO_DAT2 / WGR_D0P		18 GND	
19 SDO_DAT3 / RSVD		20 UART_WAKE# / RSVD	RW12 1 CNVI@ 2 0_0402_5% — CNV_BRI_PRX_DTX [15]
21 SDIO_WAKE# / WGR_CLKN		22 UART_RX / BRI_RSP	CNV_BRI_PRX_R_DTX — RW35 1 2 0_0402_5% — UART_2_PRXD_DTXD [19]
23 SDIO_RESET# / WGR_CLKP			DBG@ RW36 1 2 0_0402_5% — UART_2_PTXD_DRXD [19]
		32 UART_TX / RGI_DT	CNV_RGI_PTX_R_DRX — RW16 1 CNVI@ 2 0_0402_5% — CNV_RGI_PRX_DRX [15]
		34 UART_CTS / RGI_RSP	CNV_RGI_PRX_R_DTX — RW17 1 2 0_0201_5% — CNV_RGI_PRX_DTX [15]
		36 UART_RTS / BRI_DT	CNV_BRI_PTX_R_DRX — RW19 1 2 0_0201_5% — CNV_BRI_PTX_DRX [15]
		38 RSVD	RW20 1 @ 2 0_0402_5% EC_TX — EC_TX [48]
		40 RSVD	RW22 1 @ 2 0_0402_5% EC_RX — EC_RX [48]
		42 RSVD	
		44 RSVD	
		46 COEX3 / RSVD	@ TW3 PAD-D
		48 COEX2 / RSVD	@ TW4 PAD-D
		50 COEX1 / RSVD	@ TW5 PAD-D
		52 SUSCLK	RW251 1 @ 2 0_0402_5% SUSCLK — SUSCLK [18]
		54 PERST0# / RSVD	WL_RST#_R — RW26 1 @ 2 0_0402_5% — PCI_RST# [16,24,48,50,57]
		56 W_DISABLE2#	BT_ON_R — RW37 1 @ 2 0_0402_5% — BT_ON [19]
		58 W_DISABLE1#	EC_WL_OFF#_R — RW38 1 @ 2 0_0402_5% — EC_WL_OFF# [19]
		60 I2C_DATA	
		62 I2C_CLK	
		64 ALERT / I2C_IRQ#	REFCLK_CNV_R — RW29 1 @ 2 0_0201_5% — REFCLK_CNV [15]
		66 RSVD / REFCLK0	
		68 RSVD	
		70 RSVD	
		72 3.3VAUX	
		74 3.3VAUX	
77 MTG77		76 MTG76	

422.18mA +3V_WLAN

Close to KEY E pin2,4
CW1 @ 4.7U_0402_6.3V6K CW2 @ 0.1U_0201_10V6K CW3 @ 0.01U_0402_16V7K

RW4 75K_0402_1% CNVI@

1.8V

Close to KEY E pin72,74
CW6 4.7U_0402_6.3V6K CW7 0.1U_0201_10V6K CW8 0.01U_0402_16V7K

For CNVi Feature

Follow 566468_CNL_UY_PDG_Rev0p73.pdf

Need to stuff for CNVi power sequence control

Imax : 2.0 A

+3VS_WLAN

UC13 EM5203AJ-20 SOT23-5 (VIN, VOUT, GND, EN, /OC)

CW3861 1U_0201_6.3V6M
CW3863 0.1U_0201_10V6K
CW3864 1U_0201_6.3V6M

WLAN_PWR_EN# — RW3937 — WLAN_PWR_EN#_R — RW3943 1 @ 2 10K_0402_5%

I (Max) : 2.0 A(+3VS_WLAN)
RDS(Typ) : 70 mohm
V drop : 0.14 V

Note : footprint not update, Please use low active load swtich footprint(SA00009XD00)

NGFF SSD1 (KEY M)

PCIE X4 (link to PICE Port 17~20)

PCIE CLK (From PCH CLKOUT1)
[15] CLK_PCIE_N1
[15] CLK_PCIE_P1

RS2 1 @ 2 0_0603_5%

For Power consumption Measurement

KEY M for 15" only SSD

JSSD1

1 GND		2 3P3VAUX	
3 GND		4 3P3VAUX	
5 PERn3	[14] PCIE_PRX_DTX_N24	6 NC	
7 PERp3	[14] PCIE_PRX_DTX_P24	8 NC	
9 GND		10 DAS/DSS#	TP@ TS1
11 PETn3	[14] PCIE_PTX_DRX_N24 — CS5 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_N24	12 3P3VAUX	
13 PETp3	[14] PCIE_PTX_DRX_P24 — CS6 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_P24	14 3P3VAUX	
15 GND		16 3P3VAUX	
17 PERn2	[14] PCIE_PRX_DTX_N23	18 3P3VAUX	
19 PERp2	[14] PCIE_PRX_DTX_P23	20 NC	
21 GND		22 NC	
23 PETn2	[14] PCIE_PTX_DRX_N23 — CS7 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_N23	24 NC	
25 PETp2	[14] PCIE_PTX_DRX_P23 — CS8 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_P23	26 NC	
27 GND		28 NC	
29 PERn1	[14] PCIE_PRX_DTX_N22	30 NC	
31 PERp1	[14] PCIE_PRX_DTX_P22	32 NC	
33 GND		34 NC	
35 PETn1	[14] PCIE_PTX_DRX_N22 — CS9 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_N22	36 NC	
37 PETp1	[14] PCIE_PTX_DRX_P22 — CS10 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_P22	38 NC	DEVSLP4_SSD_RS8 1 @ 2 0_0402_5% — DEVSLP4 [17]
39 GND		40 DEVSLP	
41 PERn0/SATA-B+	[14] PCIE_PRX_DTX_P21	42 NC	
43 PERp0/SATA-B-	[14] PCIE_PRX_DTX_N21	44 NC	
45 GND		46 NC	
47 PETn0/SATA-A-	[14] PCIE_PTX_DRX_N21 — CS11 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_N21	48 NC	
49 PETp0/SATA-A+	[14] PCIE_PTX_DRX_P21 — CS12 15@ 0.22U_0201_6.3V — PCIE_PTX_C_DRX_P21	50 NC	PCI_RST#
51 GND		52 PERST#	
53 REFCLKN	[15] CLK_PCIE_N1	54 CLKREQ#	TP@ TS2 — SSD_CLKREQ1# [15]
55 REFCLKP	[15] CLK_PCIE_P1	56 PEWake#	
57 GND		58 NC	
67 NC		68 SUSCLK(32kHz)	SUSCLK
69 NC		70 3P3VAUX	
71 PEDET(NC-PCIE/GND-SATA)		72 3P3VAUX	
73 GND		74 3P3VAUX	
75 GND		76 GND1	
		77 GND2	

LOTES_APCI0079-P005A

+3VS_SSD

CS2 4.7U_0402_6.3V6K CS4 0.1U_0201_10V6K CS3 0.01U_0402_16V7K

Close to JSSD1 KEY M pin2,4

RS12 10K_0402_5% — SATAPCIE_4 — [17] SATAPCIE_4

PEDET	Module Type
0	SATA
1	PCIE

1129 symbol changed

for 17" SSD

JSSD2

1 GND		2 3P3VAUX	
3 GND		4 3P3VAUX	
5 PERn3	PCIE_PRX_DTX_N24 — RHD19 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_N24_R	6 NC	
7 PERp3	PCIE_PRX_DTX_P24 — RHD20 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_P24_R	8 NC	
9 GND		10 DAS/DSS#	TP@ TS3
11 PETn3	PCIE_PTX_DRX_N24 — 17@CS13 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_N24	12 3P3VAUX	
13 PETp3	PCIE_PTX_DRX_P24 — 17@CS14 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_P24	14 3P3VAUX	
15 GND		16 3P3VAUX	
17 PERn2	PCIE_PRX_DTX_N23 — RHD23 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_N23_R	18 3P3VAUX	
19 PERp2	PCIE_PRX_DTX_P23 — RHD24 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_P23_R	20 NC	
21 GND		22 NC	
23 PETn2	PCIE_PTX_DRX_N23 — 17@CS15 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_N23	24 NC	
25 PETp2	PCIE_PTX_DRX_P23 — 17@CS16 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_P23	26 NC	
27 GND		28 NC	
29 PERn1	PCIE_PRX_DTX_N22 — RHD27 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_N22_R	30 NC	
31 PERp1	PCIE_PRX_DTX_P22 — RHD28 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_P22_R	32 NC	
33 GND		34 NC	
35 PETn1	PCIE_PTX_DRX_N22 — 17@CS17 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_N22	36 NC	
37 PETp1	PCIE_PTX_DRX_P22 — 17@CS18 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_P22	38 NC	DEVSLP4_SSD
39 GND		40 DEVSLP	
41 PERn0/SATA-B+	PCIE_PRX_DTX_P21 — RHD31 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_P21_R	42 NC	
43 PERp0/SATA-B-	PCIE_PRX_DTX_N21 — RHD32 2 17@ 1 0_0201_5% — PCIE_PRX_DTX_N21_R	44 NC	
45 GND		46 NC	
47 PETn0/SATA-A-	PCIE_PTX_DRX_N21 — 17@CS19 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_N21	48 NC	
49 PETp0/SATA-A+	PCIE_PTX_DRX_P21 — 17@CS20 1 2 0.22U_0201_6.3V — PCIE_PTX_17C_DRX_P21	50 NC	PCI_RST#
51 GND		52 PERST#	SSD_CLKREQ1#
53 REFCLKN	CLK_PCIE_N1 — RHD35 2 17@ 1 0_0201_5% — CLK_PCIE_N1_R	54 CLKREQ#	TP@ TS4
55 REFCLKP	CLK_PCIE_P1 — RHD36 2 17@ 1 0_0201_5% — CLK_PCIE_P1_R	56 PEWake#	
57 GND		58 NC	
67 NC		68 SUSCLK(32kHz)	SUSCLK
69 NC		70 3P3VAUX	
71 PEDET(NC-PCIE/GND-SATA)		72 3P3VAUX	
73 GND		74 3P3VAUX	
75 GND		76 GND1	
		77 GND2	

SATAPCIE_4

LOTES_APCI0079-P005A

CS23 CS22 CS21 17@ 0.1U_0201_10V6K

Close to JSSD2 KEY M pin2,4

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

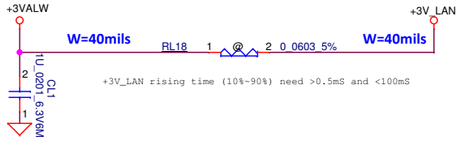
Compal Electronics, Inc.

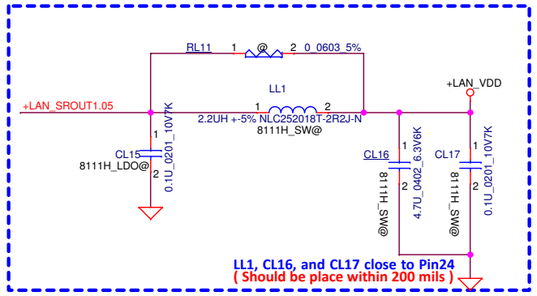
Title: WLAN(KEY E)/SSD(KEY M)

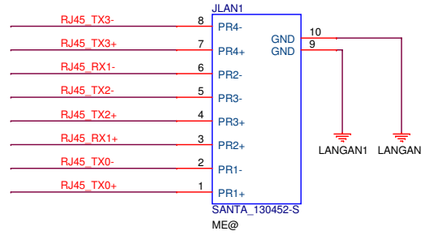
Size: | Document Number: LA-G132P | Rev: 1.0

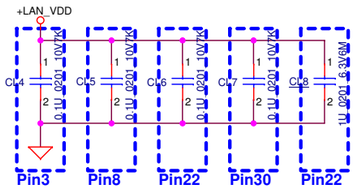
Date: Wednesday, January 09, 2019 | Sheet 49 of 81

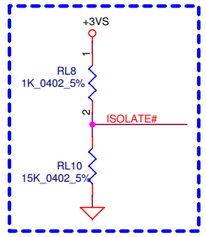
RJ-45 CONN.

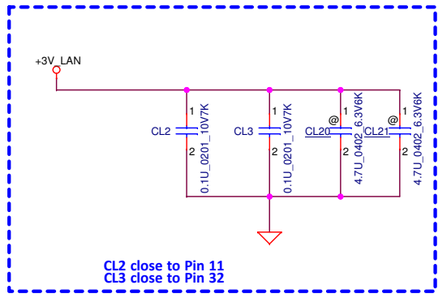


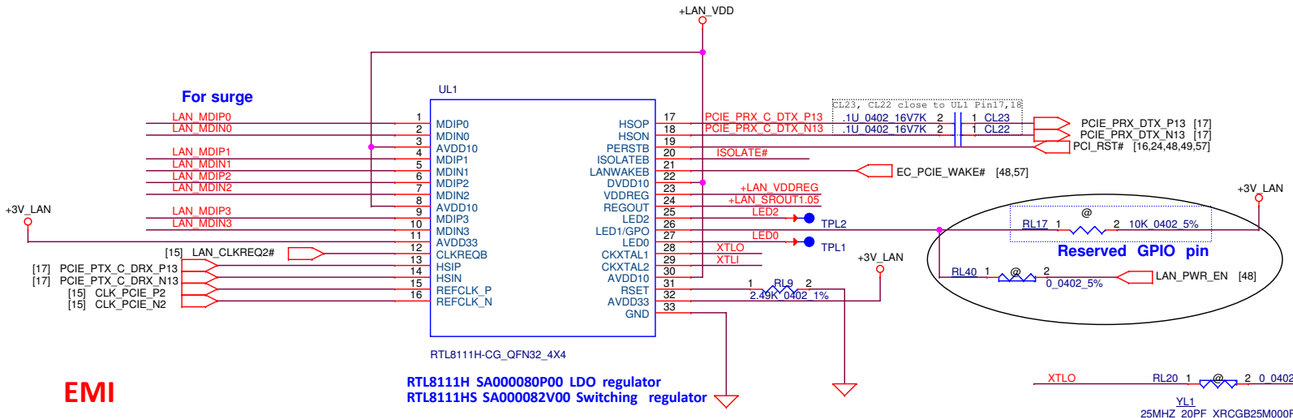


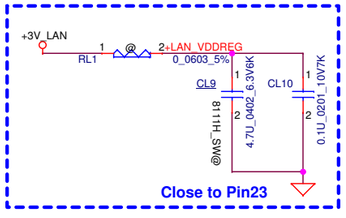


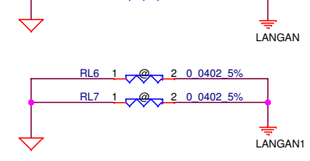


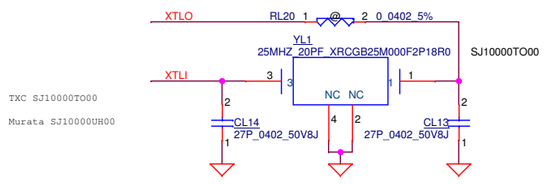


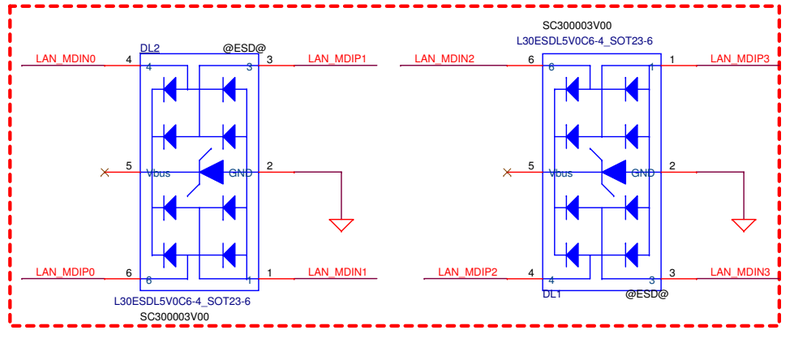


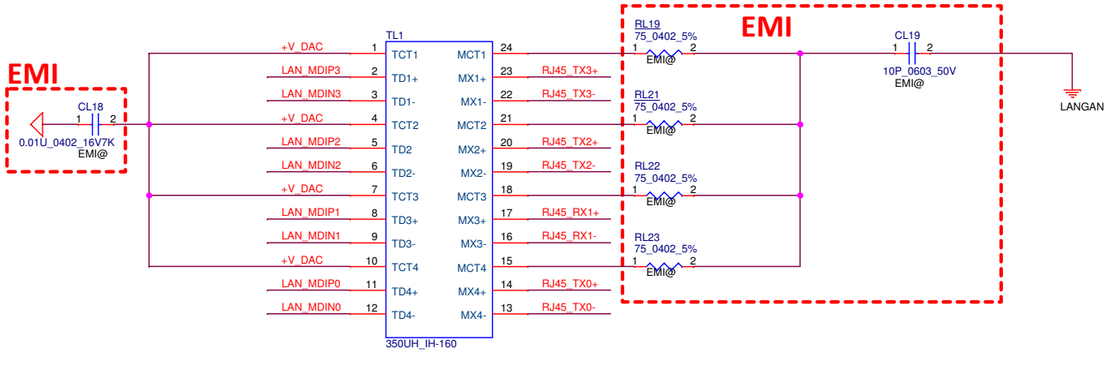












Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: LAN_RTL8111H/RTL8107E

Size: C | Document Number: LA-G132P | Rev: 1.0

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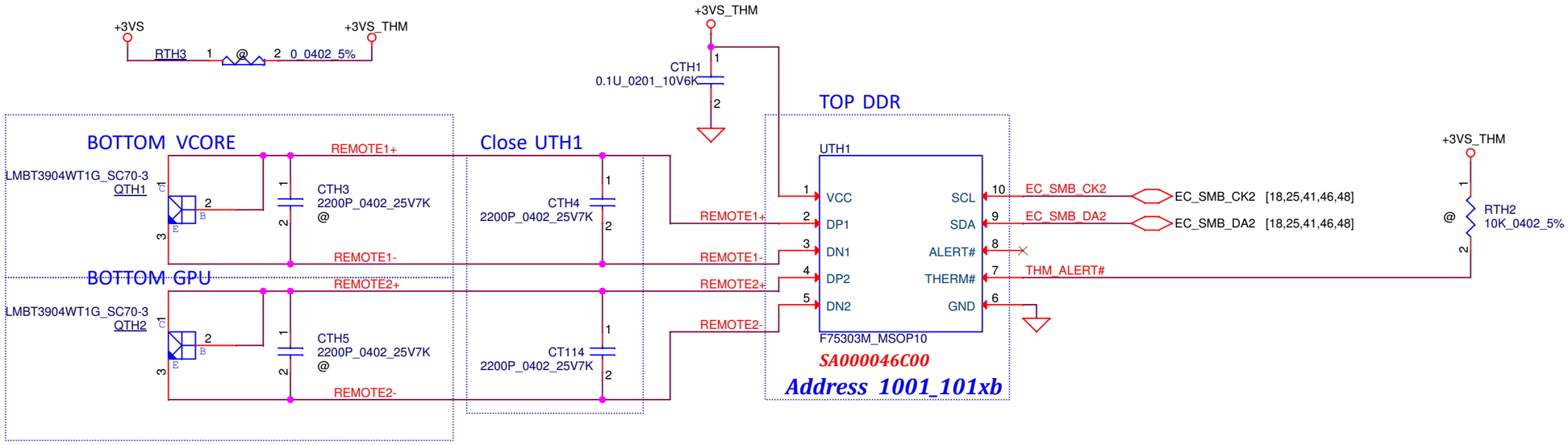
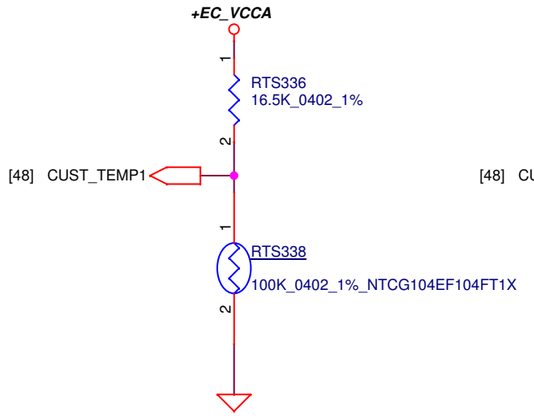
THERMAL SENSOR

For Smart Performance

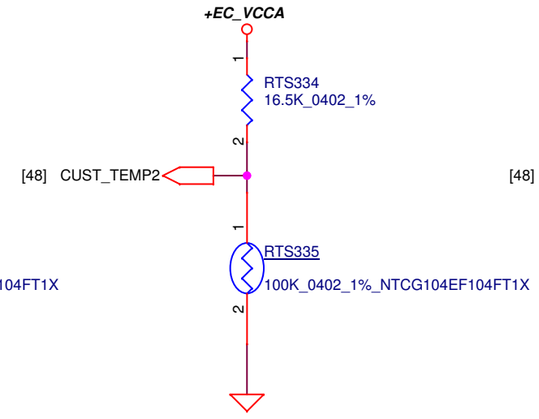


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

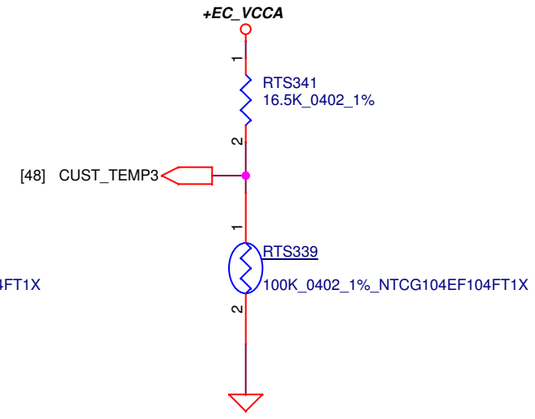
GPU Fan



CPU Fan



SSD



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: Thermal Sensor

Size	Document Number	Rev
B	LA-G132P	1.0

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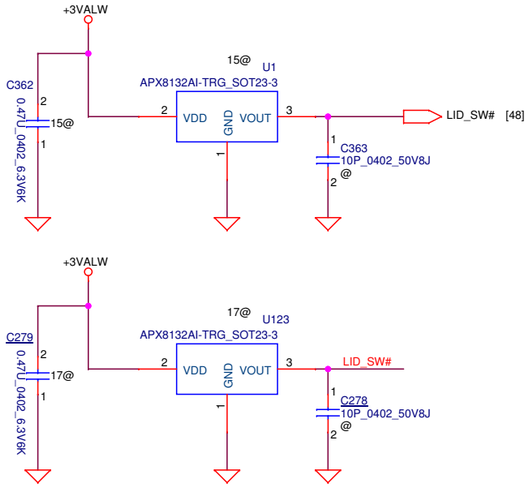
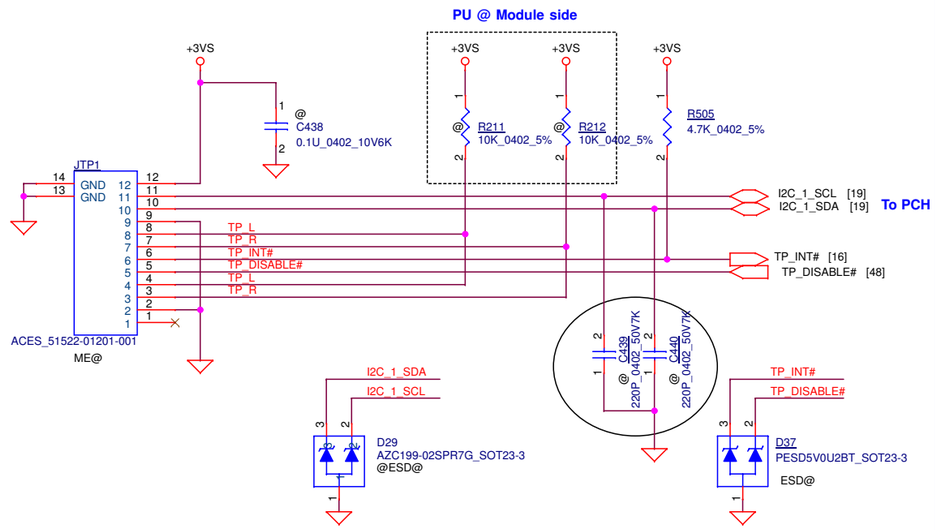
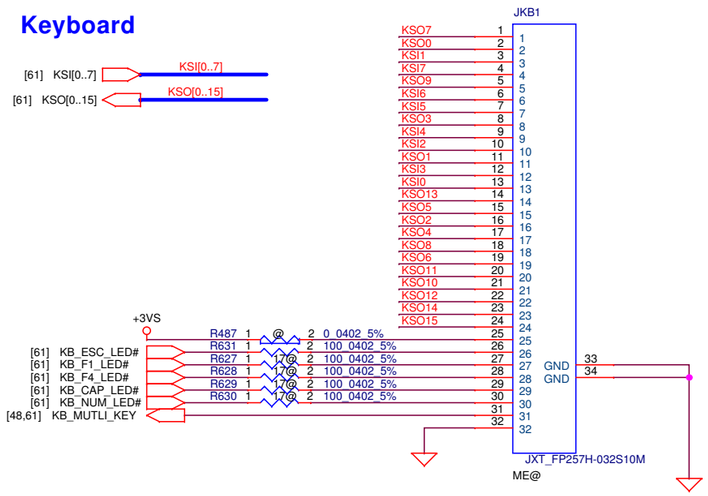
Lid Switch

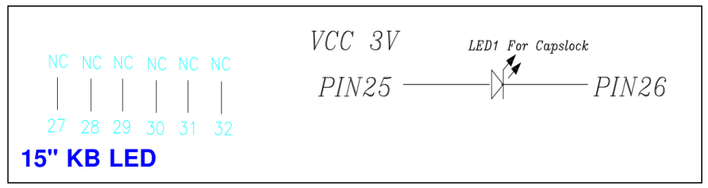


Touch Pad

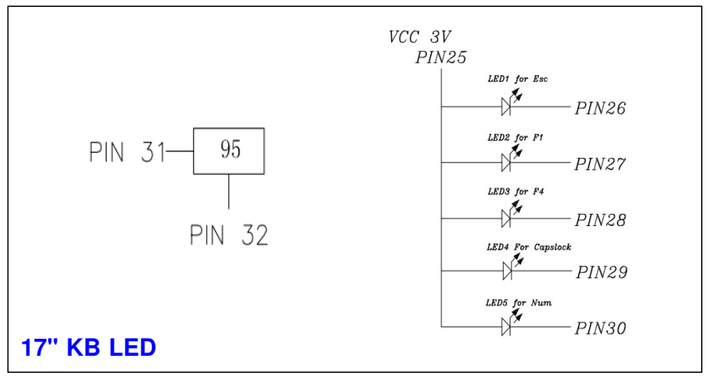


Keyboard





15" KB LED



17" KB LED

Bom Structure

VRAM 8G

M8G@	S8G@	H8G@
MT61K256M32JE-14:A	K4Z80325BC-HC14	H56C8H24MJR-S2C
X7678038L51	X7678038L52	X7678038L53

M6G@	S6G@	H6G@
MT61K256M32JE-14:A	K4Z80325BC-HC14	H56C8H24MJR-S2C
X7678038L56	X7678038L57	X7678038L58

Coffee Lake-H CPU SKU

CPU1@	CPU5@	CPU3@
MP-R1	MP-R3	ES-8+2
CFL-H_i5-8300H	CFL-H_i5-8300H	CFL-R 8C 2.1G ES
SA0000BPJ20	SA0000BPJ60	SA0000CDU00

CPU2@	CPU6@	CPU4@
MP-R1	MP-R3	ES-6+2
CFL-H_i7-8750H	CFL-H_i7-8750H	CFL-R 6C 2.4G ES
SA0000BPZ20	SA0000BPZ60	SA0000CDV00

Refresh

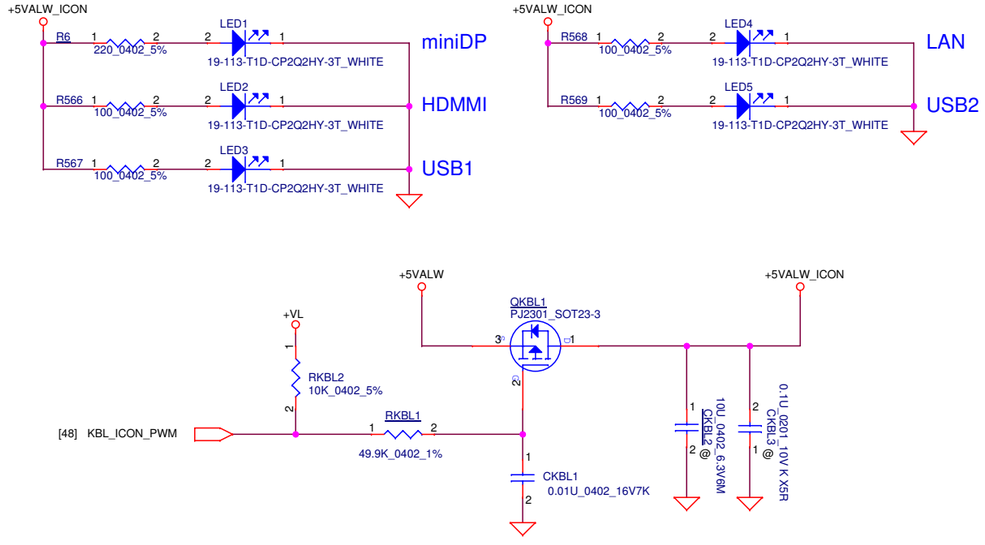
Cannn Lake PCH HM370

PCH1@	PCH3@
MP-R1	MP-R3
HM370 SR40B	HM370 SR40B
SA0000BVP00	SA0000BVP30

Refresh

PCH4@
ES
962361/QP21 ES
SA0000B4I20

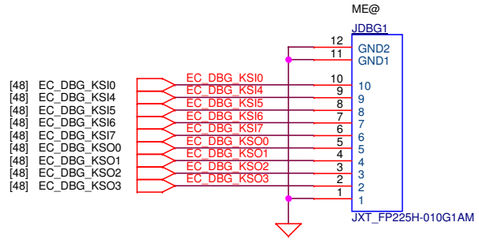
Icon LED



Nvidia GPU SKU

GPU1@	GPU2@	GPU3@	GPU4@	GPU5@	GPU6@
2060-G1-R1	2070-G2-R1	2080-G3-R1	2060-G1-MP	2070-G2-MP	2080-G3-MP
N18E-G1-A1	N18E-G2-A1	N18E-G3-A1	N18E-G1-A1	N18E-G2-A1	N18E-G3-A1
SA0000CFC00	SA0000CCX00	SA0000CD500	SA0000CFC40	SA0000CCX40	SA0000CD550

GPU7@	GPU8@
2050-G0-R1	2050-G0-MP
N18E-G0-A1	N18E-G0-A1
SA0000CK400	SA0000CK420



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: KB/TP/LID/BOM S.

Size | Document Number: LA-G132P | Rev: 1.0

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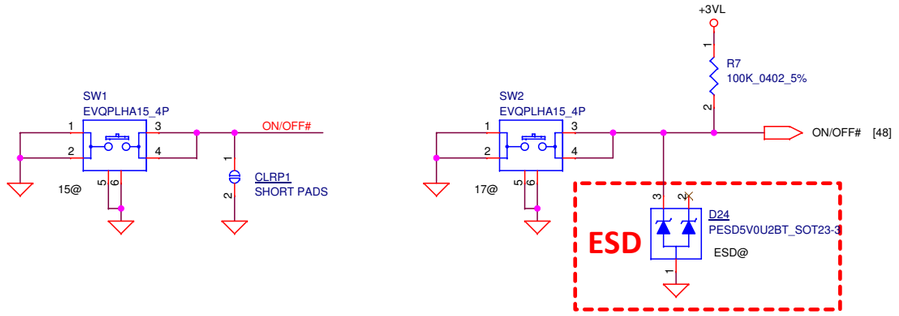
Power BTN

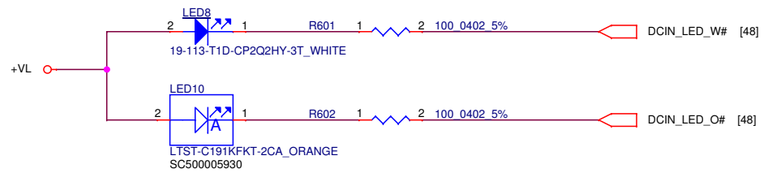


For 15"

For 17"

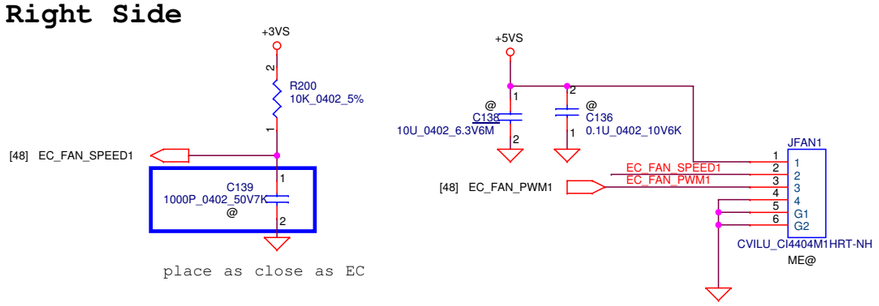
Change SCA00002900 to SCA00000T00

DCIN LED



CPU Fan Control Circuit

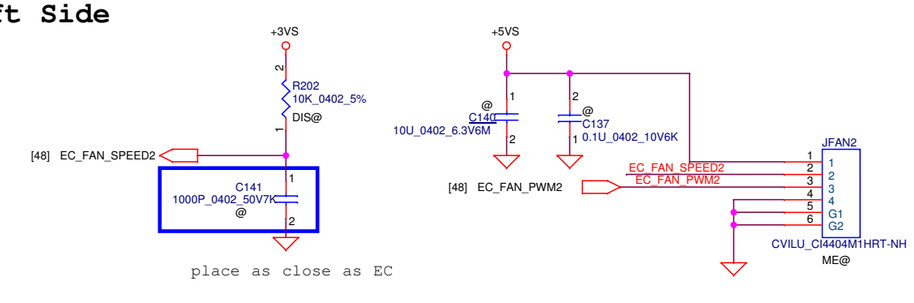
Right Side



place as close as EC

GPU Fan Control Circuit

Left Side



place as close as EC

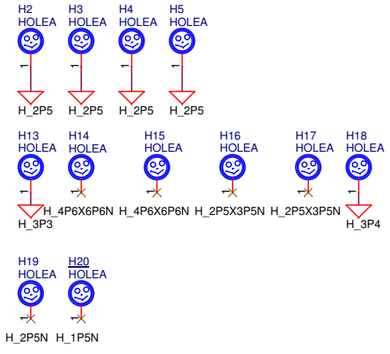
PCB

ZZZ

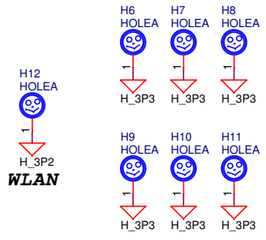
LA-G132P

DAB00032000

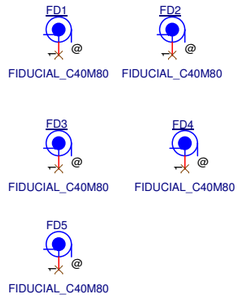
Screw Hole



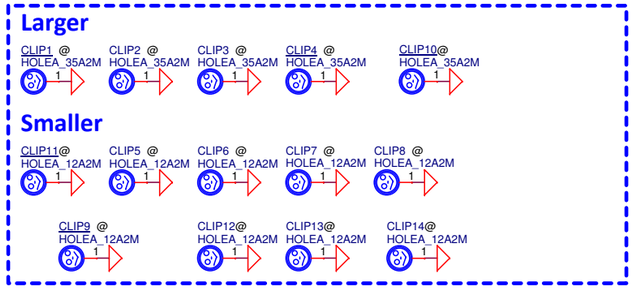
CPU/GPU Thermal Standoff



Fiducial Mark



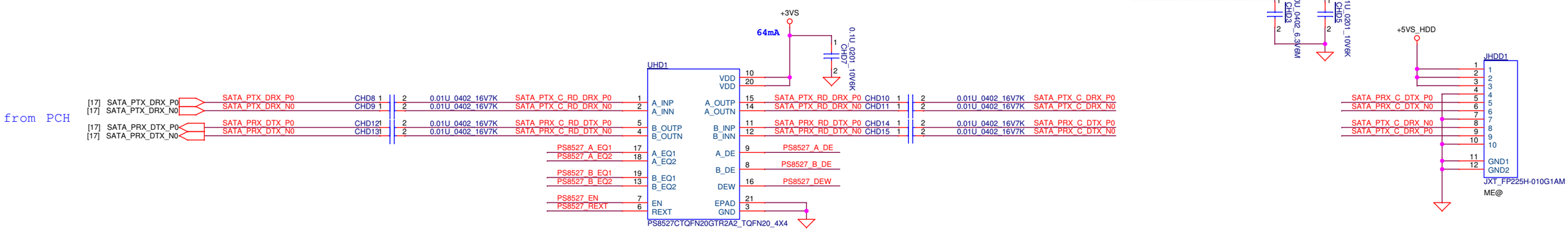
DDR Shielding Clip



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: FAN/LED/PBTN/PCB PN/SCREWS			
Size	Document Number: LA-G132P		Rev: 1.0
Date: Wednesday, January 09, 2019	Sheet 53 of 81		

SATA HDD



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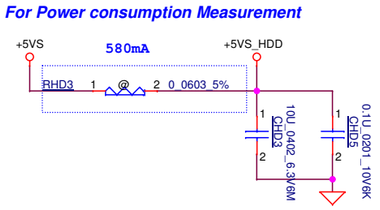
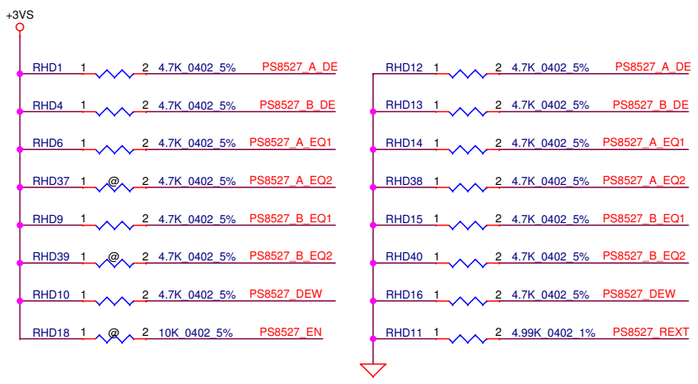




Equalizer control and program for channel A.

Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.

Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Programmable output de-emphasis level setting for channel A.

Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.

Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

De-emphasis width setting for channel A& B .

Internally tied to VDD/2(M status).

DEW	DE pulse duration optimized for
M	SATA 6Gbp/s(default)
L	SATA 6Gbp/s
H	SATA 3Gbp/s

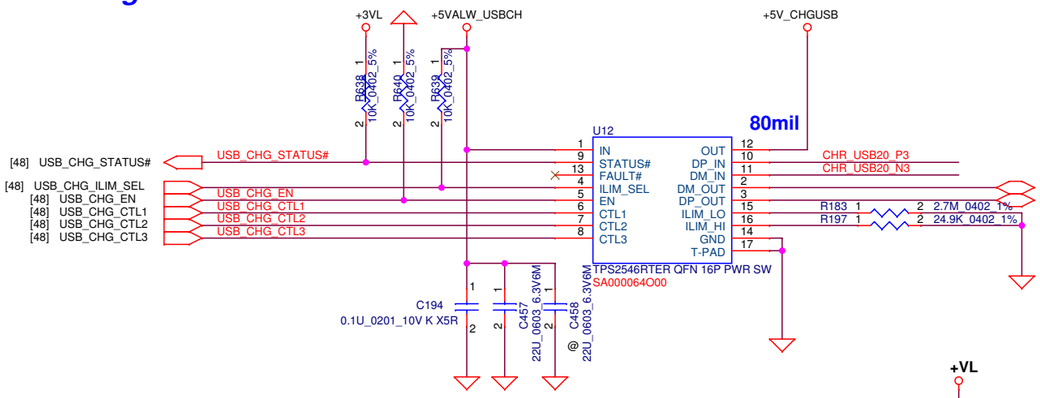
Compal Electronics, Inc.

Title: HDD Connector

Size | Document Number: LA-G132P | Rev: 1.0

Date: Wednesday, January 09, 2019 | Sheet 54 of 81

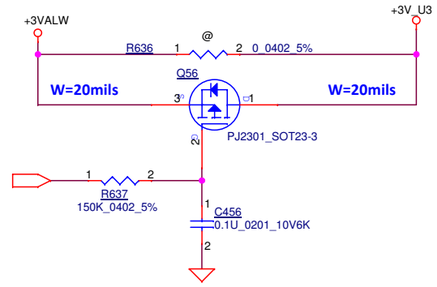
USB Charger from YOGA730 15



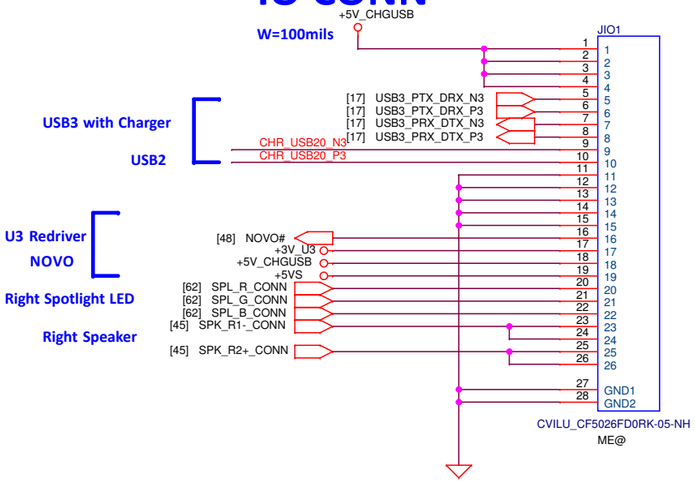
USB3.0 With USB2.0 For Charge

Right Spotlight LED

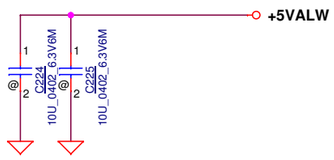
Right Speaker

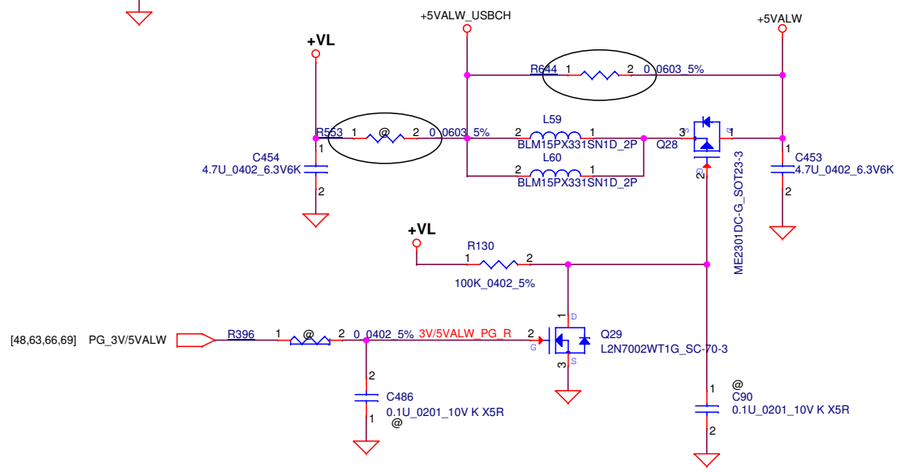


IO CONN



Down USB charger Iout ripple
must under 20mA on DC S5





Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: USB3 Port 3 CONN.			
Size	Document Number: LA-G132P		Rev: 1.0
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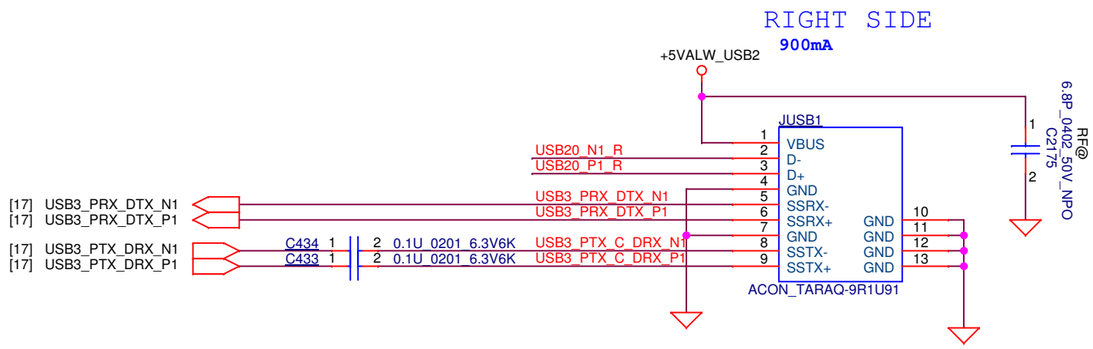
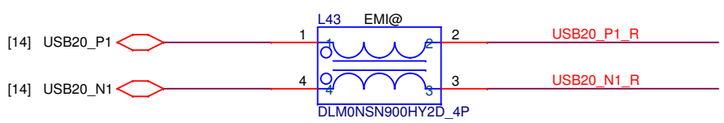
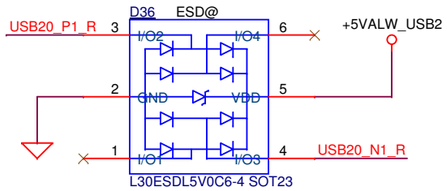
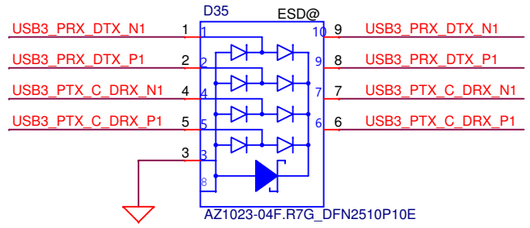
MB_USB3.1 Conn. (Port 1)



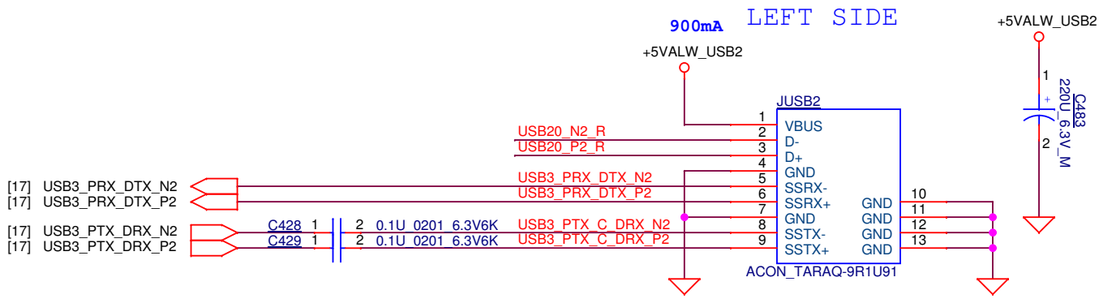


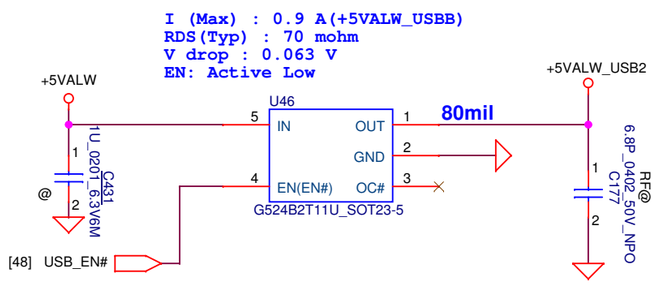


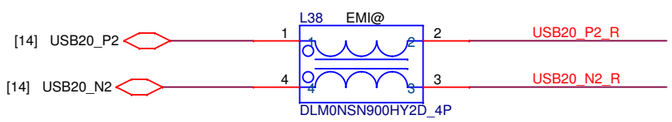
SC300004W00 change to SC300006000

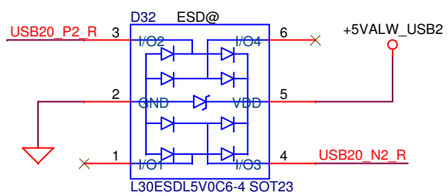


MB_USB3.1 Conn. (Port 2)

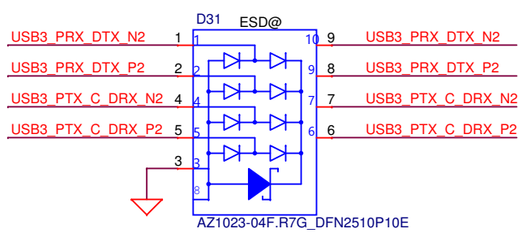








SC300004W00 change to SC300006000



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: USB3 Port1/2 Conn.			
Size	Document Number: LA-G132P		Rev: 1.0
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Titan Ridge SP - High Speed (CIO, USB and PCIe) Parts

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface,
please leave pins open. No need for termination.

TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used

From PCH PCIe TX

To SoC PCIe RX

From GPU DDI

Follow TR_DP_TI_PD_HOST_REF_DESIGN_R0V95
PE isn't POR -
Please don't use

JTAG

SPI ROM

25M XTAL

Must use Metal shielded crystal for better noise immunity.
(Recommended: FL2500123Z by Pericom)

TBT_GPIO_8
'0' - Unsecure mode
'1' - Secure mode

PCIE RBIAS
Place as close as possible to pins

DG_FORCE_PWR:
'0' - Regular Mode, Force Power is disabled (Default)
'1' - Force Power Mode is enabled

DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain - connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

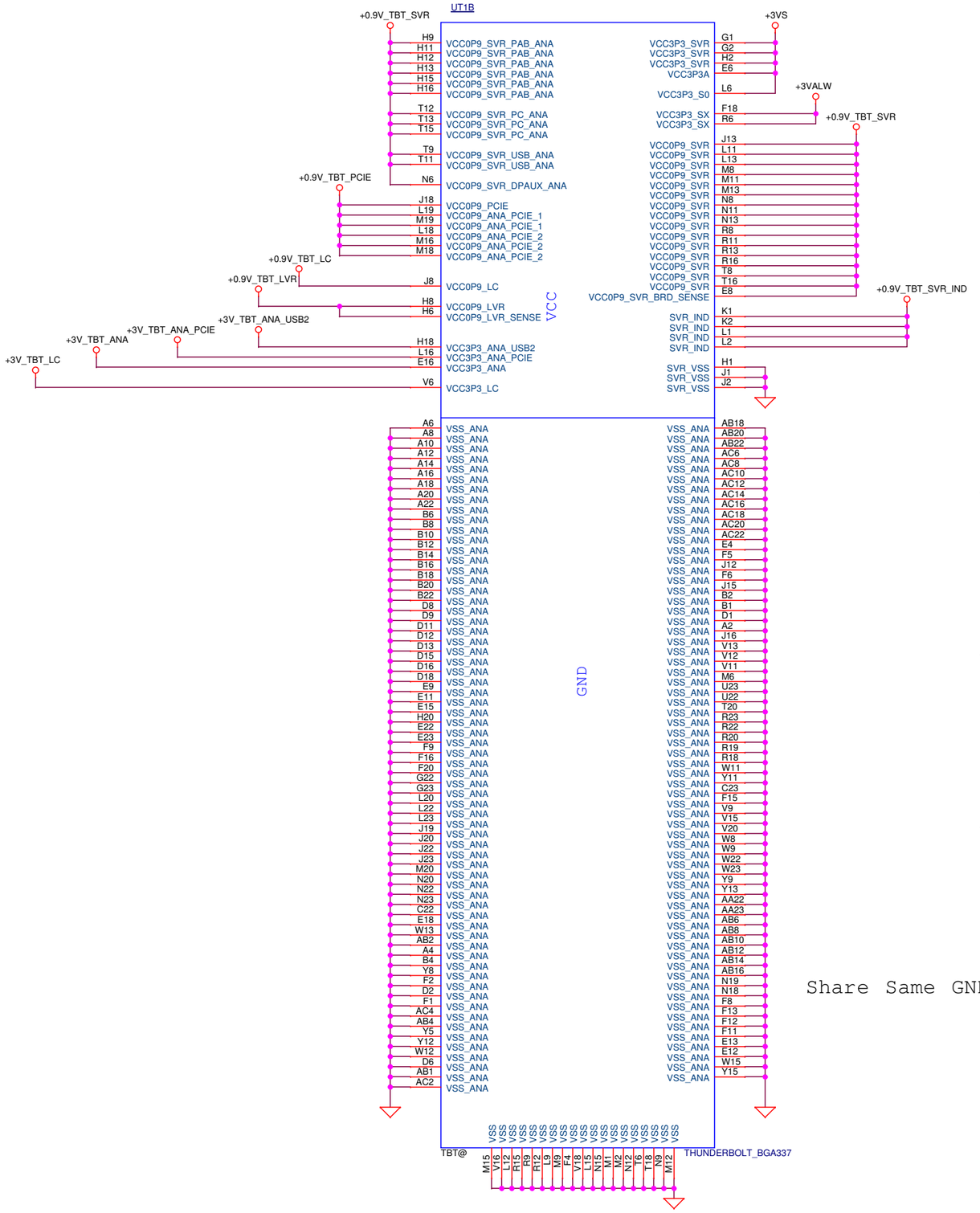
DG_CIO_PLUG_EVENT# should be conncted to PCH SCI GPIO

Place as close as possible to pins

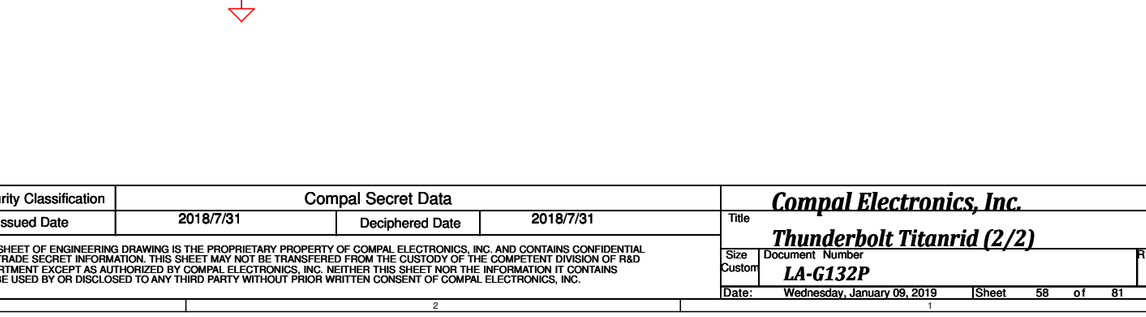
USB2 Rbias Place as close as possible to pins

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title: Thunderbolt Titanrid (1/2)			
Size: Custom	Document Number: LA-G132P		Rev: 1.0
Date: Wednesday, January 09, 2019	Sheet 57 of 81		



Share Same GND plane



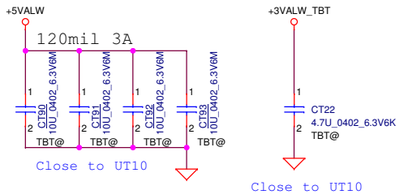
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

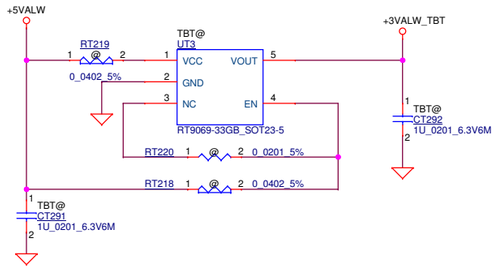
Compal Electronics, Inc.

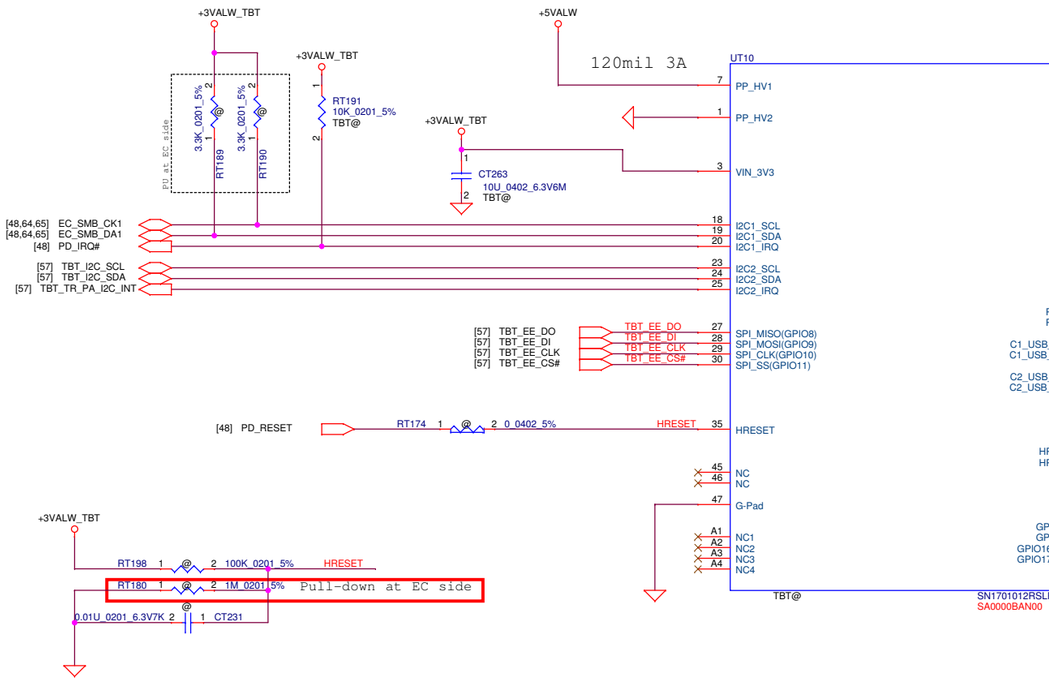
Title: **Thunderbolt Titanrid (2/2)**

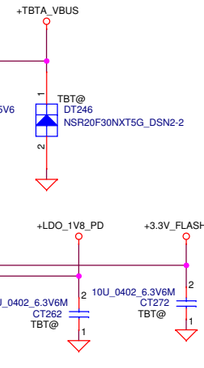
Size	Document Number	Rev
Custom	LA-G132P	1.0

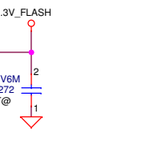
Date: Wednesday, January 09, 2019 Sheet 58 of 81

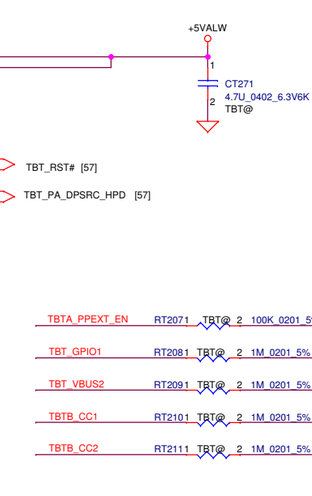


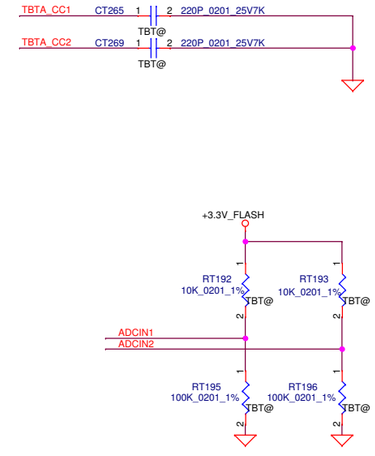












Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title	CC_TPS65988		
Size	Document Number LA-G132P		Rev 1.0
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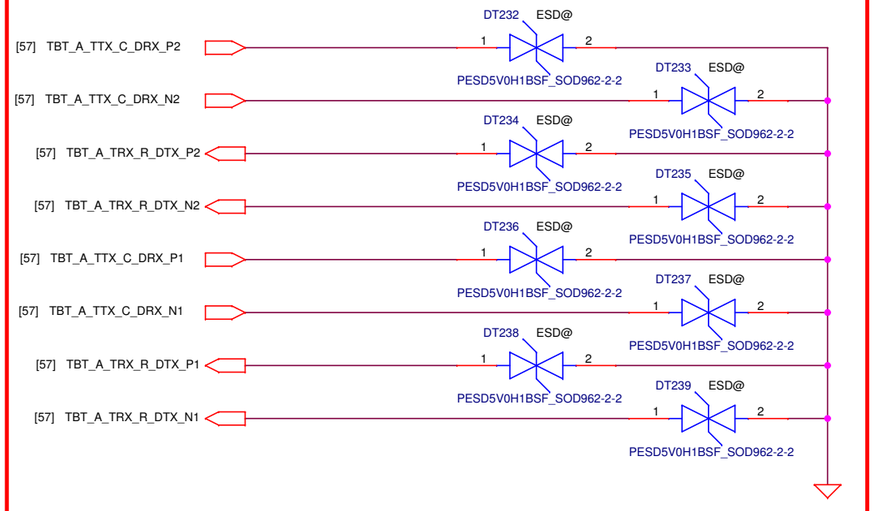
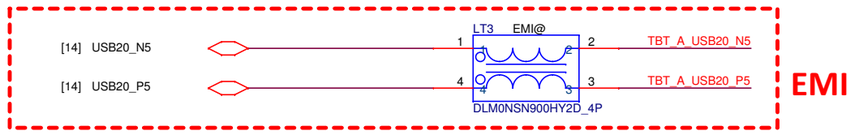
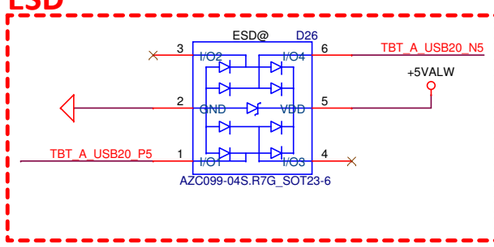
Main source:SC40000AT00
Foorprint: ESD8011MUT5G_X3DFN2-2(SC40000AR00 Footprint)



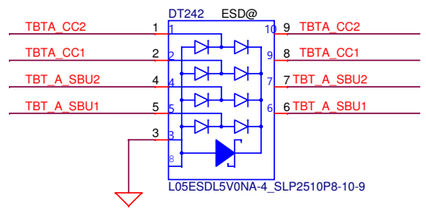


different from USB3.0 port's ESD

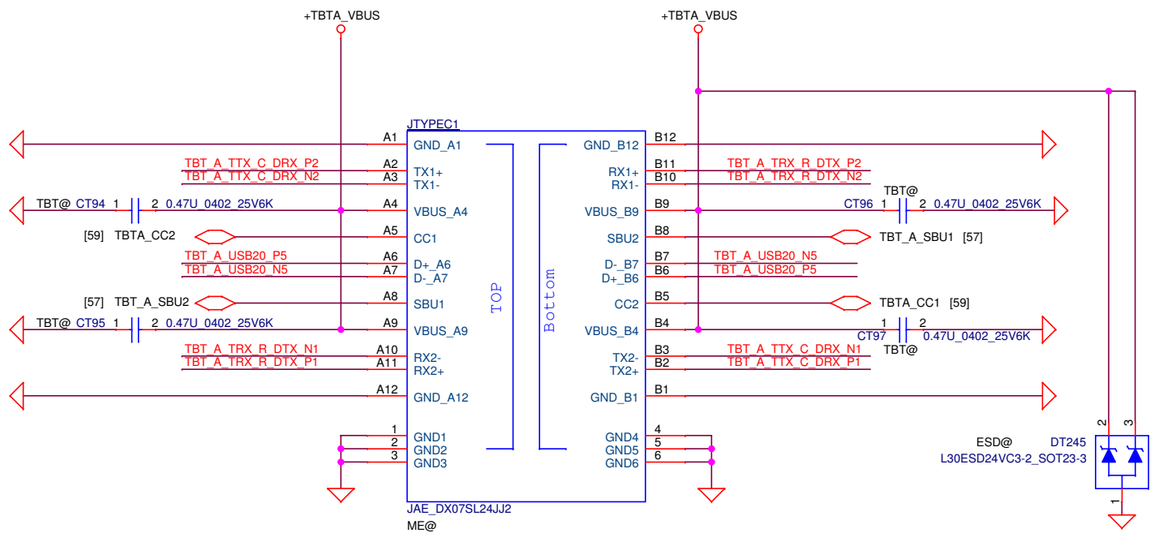
ESD



ESD Diode for CC1 CC2



SC300001G00 change to SC300006000



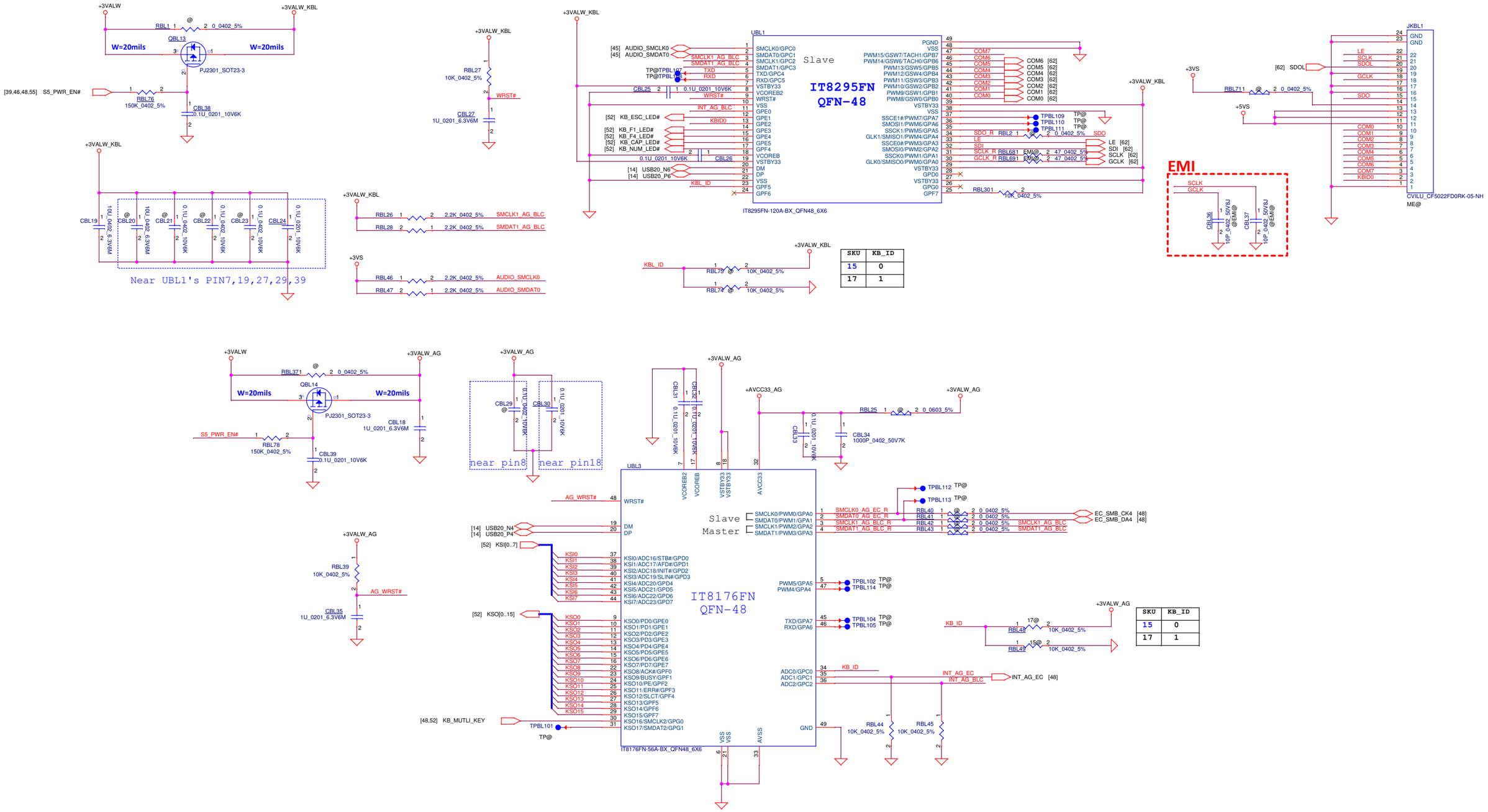
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **USB3.1 TypeC Conn**

Size | Document Number: **LA-G132P** | Rev: 1.0

Date: Wednesday, January 09, 2019 | Sheet 60 of 81



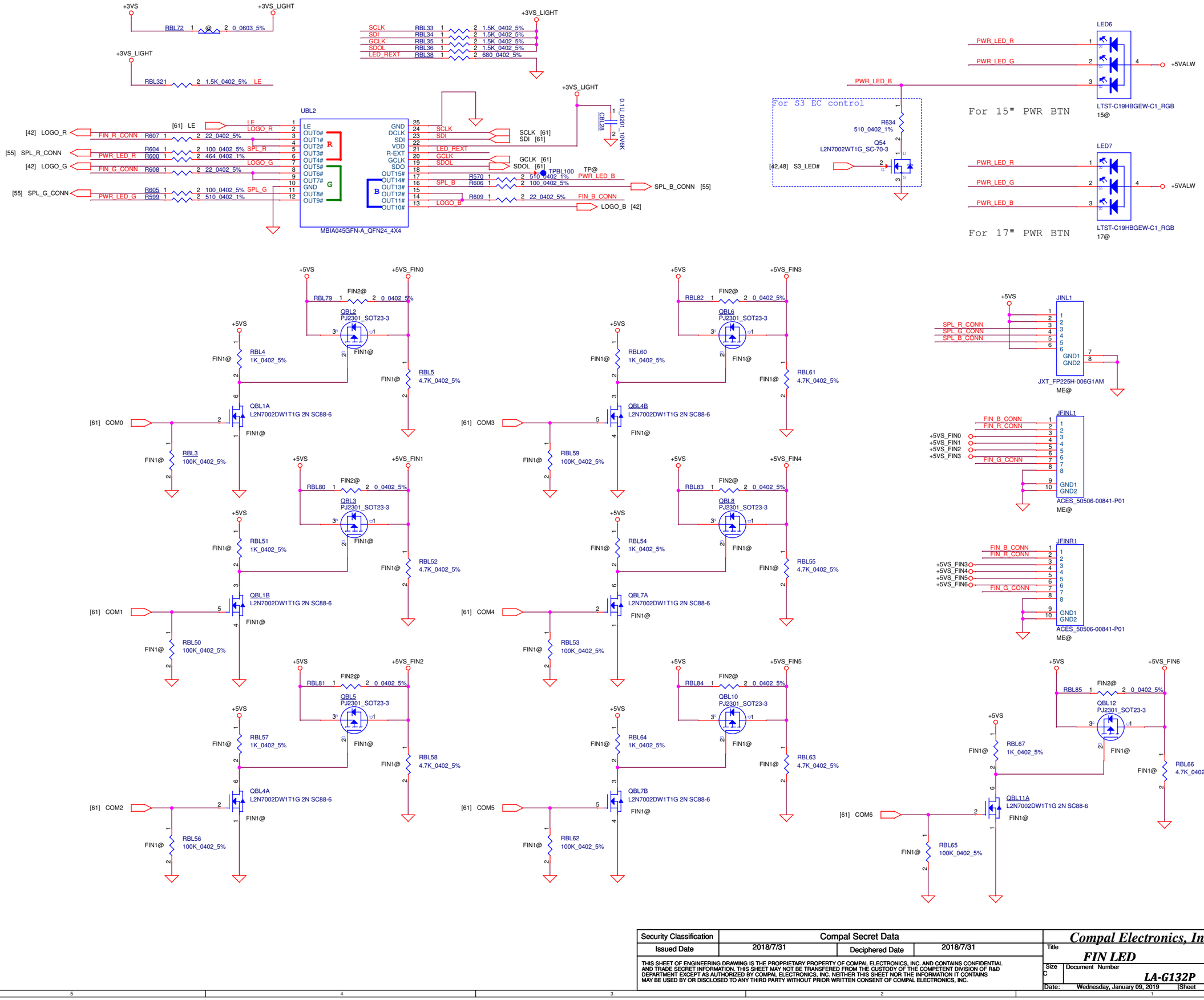
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **KB LED IT8176**

Size: Custom | Document Number: **LA-G132P** | Rev: 1.0

Date: Wednesday, January 09, 2019 | Sheet 61 of 81



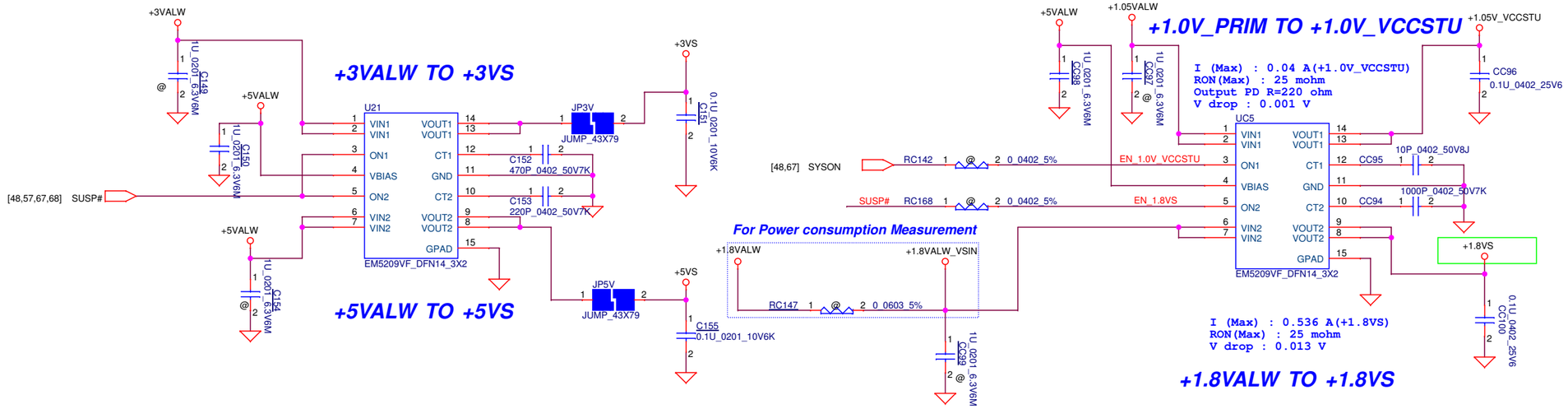
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

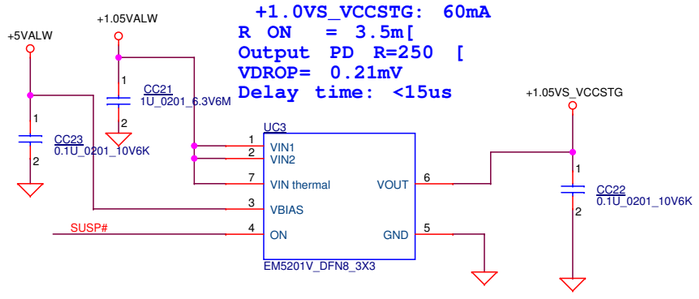
Title: **FIN LED**

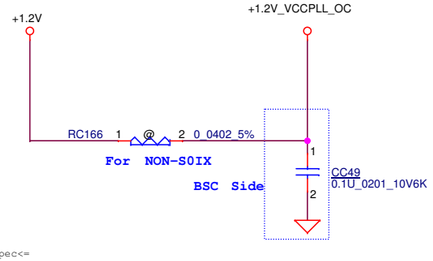
Size	Document Number	Rev
C	LA-G132P	1.0

Date: Wednesday, January 09, 2019 Sheet 62 of 81

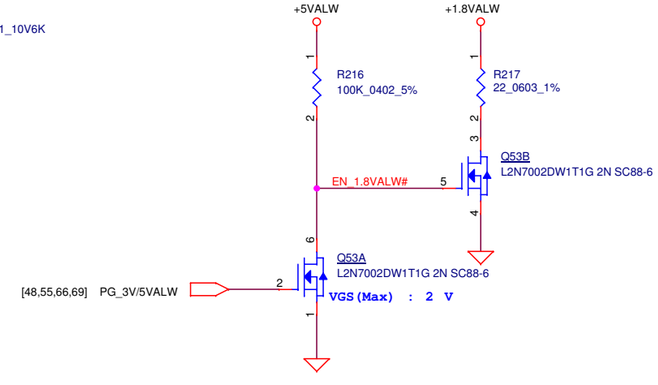


+1.05VALW TO +1.05VS_VCCSTG





+ 1.2V_VCCSFR_OC Load switch timing meet intel spec<= 240gs



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

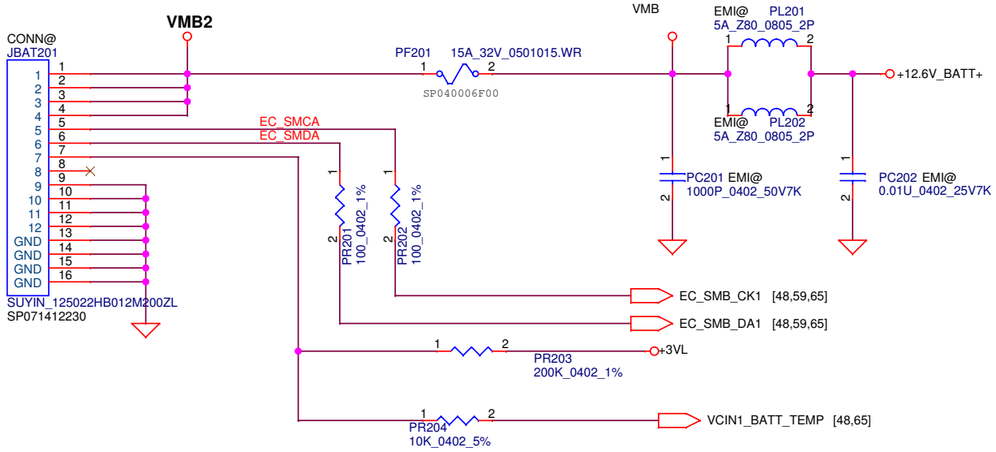
Compal Electronics, Inc.

Title: DC INTERFACE

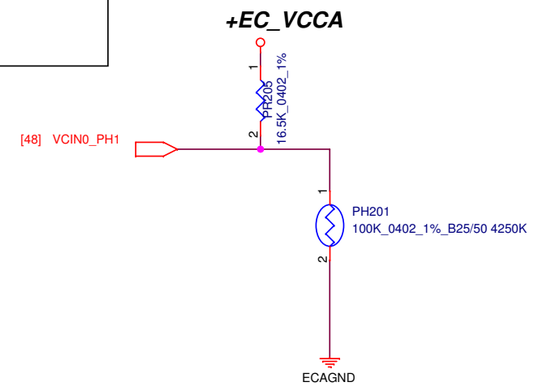
Size | Document Number: LA-G132P | Rev: 1.0

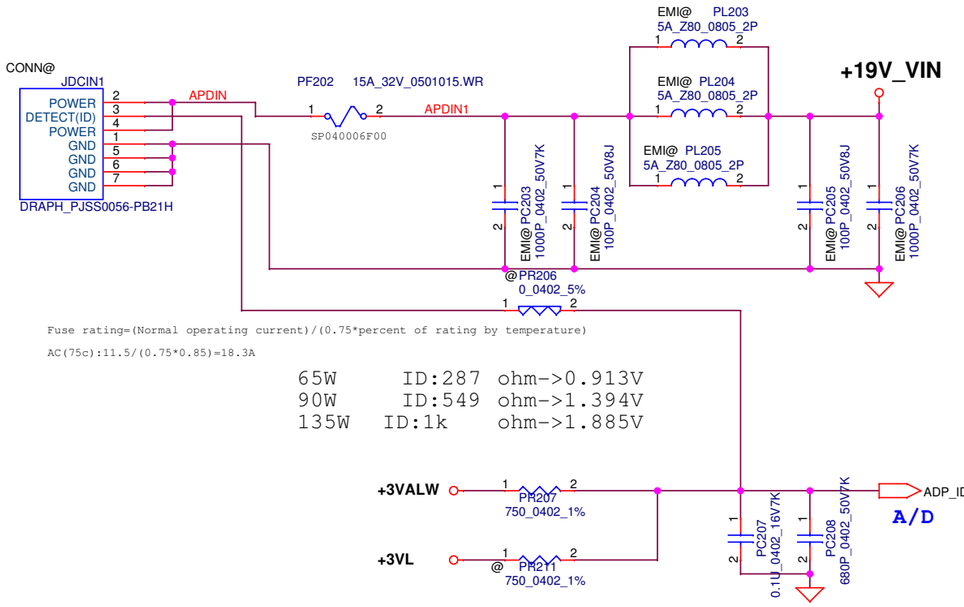
Date: Wednesday, January 09, 2019 | Sheet 63 of 81

Fuse rating=(Normal operating current)/(0.75*percent of rating by temperature)
BATT(95c):8A/(0.75*0.8)=13.3A



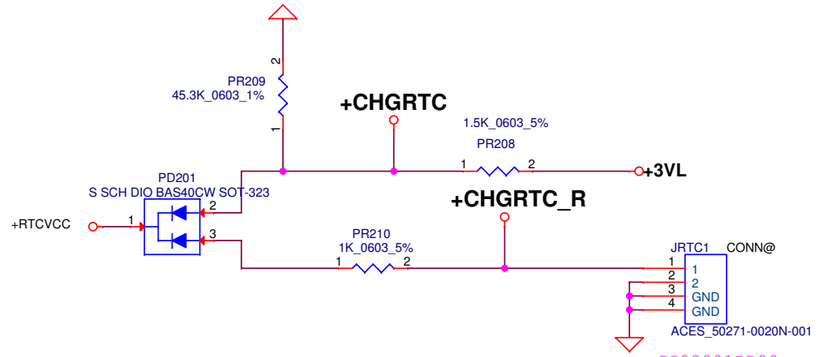
PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C





Fuse rating=(Normal operating current)/(0.75*percent of rating by temperature)
AC(75c):11.5/(0.75*0.85)=18.3A

```
65W      ID:287  ohm->0.913V
90W      ID:549  ohm->1.394V
135W   ID:1k     ohm->1.885V
```

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	Y740	0.1

Date: Wednesday, January 09, 2019 | Sheet 64 of 81

Module model information

ISL95520A_Hybrid_Boost_V2.mdd

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ302 2N7002KW_SOT323-3
PR301 1M_0402_1%
PR302 3M_0402_5%

+19V_P1
+19V_P2
PQ310 AON7380_DFN3X3-8-5
PQ303 AON7380_DFN3X3-8-5
ASGATE_CHG_R

PQ301 EMP21N03HC_N_DFN56-8-5
PQ316 EMP21N03HC_N_DFN56-8-5
ASGATE_CHG_R

Need check the SOA for inrush
+19V_VIN

PR303 0.005_1206_1%
@PJP301 JUMP_43X118
Co-lay jump and ISN choke.
Isat: 10A
DCR: 14mohm

+19VB
+19VB_CHG
PC302 10U_0603_25V6M
PC303 10U_0603_25V6M
PC304 @EMI@ 0.1U_0402_25V7K
PC305 EMI@ 2200P_0402_25V7K

@ PQ311 AON7380_DFN3X3-8-5
BGATE_CHG
PQ304 AON7380_DFN3X3-8-5
Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)

PR304 1_0402_5%
PR305 2_0402_5%
CSIP_CHG_R
CSIN_CHG_R

PR306 392K_0402_1%
PC1813 0.033U_0402_25V7K
PC301 0.1U_0402_25V6
@ PC1814 0.1U_0402_25V6

PR307 4.02K_0402_1%
PR308 4.02K_0402_1%
ASGATE_CHG_R

PR729 and PR732 are ACDET set ting base on your project to set
ACDET= 18.09V

PR309 100_0402_1%
+12.6V_BATT+

CMSRC_CHG
ASGATE_CHG
PC307 0.22U_0603_25V7K
@PC308 0.1U_0402_25V7K

PR310 48.7K_0402_1%
PC306 2200P_0402_50V7K

0x3CH <BIT9> PSYS current gain
Rs1 = 10m[and Rs2 = 5m[or Rs1 = 10m[and Rs2 = 10m[
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
==========
Rs1 = 20m[and Rs2 = 10m[or Rs1 = 20m[and Rs2 = 20m[
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

support Turbo boost : 2200P
no support Turbo boost : 0.1u

Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)

PQ305 AON7408L_DFN8-5
7X7X3
Isat: 6.5A
DCR: 28mohm

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

PR311 100K_0402_1%
VDD_CHG
ACIN_CHG
[48] VCIN1_AC_IN
PR314 158K_0402_1%

PU301 ISL95521BHRZ-T_QFN32_4X4

32	CSIP	ACIN	1
31	CSIN	ACOK	2
30	ASGATE	SDA	3
29	CMSRC	SCL	4
28	OPCN	PROCHOT#	5
27	OPCP	AMON	6
26	VBAT	BMON	7
25	BGATE	NC	8
24	BOOT	AGND	33
23	UGATE	PROG	9
22	PHASE	COMP	10
21	LGATE	CCLIM	11
20	VDDP	FSET	12
19	VDD	BATGONE	13
18	DCIN	CSON	14
17	NTC	CSOP	15
		ACLIM	16

[48,59,64] EC_SMB_DA1 — PR312 0_0402_5%
[48,59,64] EC_SMB_CK1 — PR316 0_0402_5%
[48] VCOUT1_PROCHOT# — PR317 0_0402_5%
[48] ADP_I — PR319 10K_0402_1% — AMON_ISL95520
[48] DCHG_I — PR321 10K_0402_1% — BMON_ISL95520
[70] PSYS_CPU — Close to EC.

PR313 0_0603_5%
PC309 0.47U_0603_25V7K
BST_CHG
BST_CHG_R
UG_CHG
LX_CHG
LG_CHG
VDDP_CHG
VDD_CHG

PR320 4.7_0402_5%
PC313 1U_0402_16V6K
PC314 1U_0402_16V6K
PR322 100K_0402_1%
PC318 1U_0603_25V6

PR324 10_1206_5%
PD301 S SCH DIO BAS40CW SOT323
+19V_VIN
BA
VF = 0.38V
A31 connect to BA
Other team connect to bat t conn

PL302 4.7UH_5.5A_20%_7X7X3_M
+17.4V_BATT_CHG
PR315 0.005_1206_1%
+12.6V_BATT+

RF@ PR318 4.7_1206_5%
RF@ PC315 680P_0402_50V7K
PQ306 AON7506_DFN3X3-8-5

PC310 10U_0603_25V6M
PC311 10U_0603_25V6M
PC312 10U_0603_25V6M

PC316 0.1U_0402_25V6
PC317 0.1U_0402_25V6
Close to EC.
Follow adapter and battery wattage in Vsys current source Base on CPU Core VR design.
The resistor is pop on CPU VR schematic.

@ PR323 10K_0402_1%

VDD=5V
PR326 200K_0402_1%
PR327 200K_0402_1%
PR335 200K_0402_1%
PR334 150K_0402_1%
@ PR329 76.8K_0402_1%
@ PQ309 L2N7002WT1G_SC70-3
VCIN1_AC_IN

CCLIM_CHG
ACLIM_CHG
PROG_CHG
COMP_CHG
FSET_CHG
PR325 10K_0402_1%

CSOP_CHG
PR328 2_0402_5%
PC319 0.1U_0402_25V6
CSON_CHG
PR333 0_0402_5%
CSOP_CHG_R
CSON_CHG_R

Fs=729KHZ ~ +/- 15%

PR332 150K_0402_1%
PC320 560P_0402_50V7K
PR330 100_0402_1%
PR331 0_0402_5%
PC321 0.033U_0402_25V7K

VCIN1_BATT_TEMP [48,64]
BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

Hybrid boost power mode
Cell = 4s

Battery current limimed by CCLIm ~ 15A.
Adapter current limimed by ACLIm ~ 13A.
(PR779 and PQ741 are for change ACLIm when AC in)
ACLIM setting at 10A, (5/295.3)*95.3/32/0.005=10A

+3VS
PR340 @VGA@ 0_0402_5%
PR338 10K_0402_5% VGA@
PR339 10K_0402_0402_5% @VGA@
[25,48] GPU_PROHOT
VCOUT1_PROCHOT#
VGA@ PQ315A 2N7002KDW_SOT363-6
VGA@ PQ314 SSM3K35MFV 1N VESM
VCIN1_AC_IN
VGA@ PQ315B 2N7002KDW_SOT363-6

PQ307 LMUN5113T1G_SOT323-3
[18,48,67] PM_SLP_S4#
PQ308 LMUN5236T1G_NPN_SOT323-3
BA

For A31 only.
Turn off Charger IC on battery only.
Depend on customer design for system power consumption.

(Rs1 = 10m[and Rs2 = 5m[or Rs1 = 20m[and Rs2 = 10m[).
CC_LIM = VccLIM / 64 x Rs2
==========
(Rs1 = 10m[and Rs2 = 10m[or Rs1 = 20m[and Rs2 = 20m[).
CC_LIM = VccLIM / 32 x Rs2
==========
AC_LIM = Vac_LIM / 32 x Rs1

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title	PWR_CHARGER		
Size	Document Number		Rev 0.1
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Module model information

RT6575D_DMOS_single_V2.mdd
RT6575D_DMOS_dual_V2.mdd

(Common Part)
Choke 4.7uH SH00000YC00

+3VLP

PC402 1U_0603_10V6K

@ PC403 100P_0402_50V8J

PR401 13.7K_0402_1%

VFB=2V

@PC404 100P_0402_50V8J

PR402 30.9K_0402_1%

VFB=2V

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

RLIMIT = (ILIMIT x RDS(ON)) x 8 / 10gA

PR403 20K_0402_1%

PR404 20K_0402_1%

POK need pull high, it will pull high on VS transfer circuit

EMI@ PL401 5A_Z80_0805_2P

+19VB

EMI@ PL411 5A_Z80_0805_2P

+12.6VB_3/5V

@EMI@ PC401 0.1U_0402_25V6

EMI@ PC406 2200P_0402_50V7K

PC407 10U_0603_25V6M

PC418 10U_0603_25V6M

[48,55,63,69] PG_3V/5VALW

+3VL

PR617 100K_0402_5%

PR405 100K_0402_1%

PR406 34K_0402_1%

PU401 RT6575DGQW(2)_WQFN20_3X3

CS2_3V FB_3V FB_5V CS1_5V

CS2 FB2 LDO3 FB1 CS1 GND

EN_3V EN2 EN1 EN_5V

PGOOD VCLK

PHASE2 PHASE1 LX_5V

BOOT2 BOOT1 BST_5V

UGATE2 UGATE1 UG_5V

LGATE2 VIN LDO5 BYP1 LGATE1

LG_3V LG_5V

VIN_3/5V

+12.6VB_3/5V

PC405 10U_0603_25V6M

PC417 10U_0603_25V6M

UG_3V

LX_3V

PL402 3.3UH_6.3A_20%_7X7X3_M

+3VALWP

PC408 0.1U_0402_25V6

PR407 2.2_0603_5%

2BST_3V_R1

2BST_3V

PR408 2.2_0603_5%

PC409 0.1U_0402_25V6

2BST_5V_R1

PQ401 AONH36334_DFN3X3A8-10

PQ402 AON6962_DFN5X6D-8-7

(Common Part)
Choke 4.7uH SH00000YC00

PL403 3.3UH_TMPA1004S-3R3MN-D__10A_20%

+5VALWP

PR409 4.7_1206_5%

RF@ PR410 4.7_1206_5%

RF@ PC413 680P_0402_50V7K

PC410 220U_6.3V_ESR18M_6.3X4.5

PC411 220U_6.3V_ESR18M_6.3X4.5

PC412 RF@ 680P_0402_50V7K

+5VLP

PR411 2.2_1206_1%

+12.6VB_3/5V

@ PC414 1U_0603_25V6K

PC415 1U_0603_10V6K

+5VALWP

+5VLP

3.4V
FSW=355kHz
COP: 11.95A

Vout2=2V*(1+13.7k/20k)= 3.4V

OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

Vos= SQU(Vomax)+L*SQU(I)/C)

5.09V
FSW=300kHz
COP: 18.89A

Vout1=2V*(1+30.9k/20k)=5.09V

EN
Rising=1.6~0.3V

Need inform HW to change NET NAME

[48] VCOUT0_MAIN_PWR_ON

[48] EC_ON

EN_5V PR412 0_0402_5%

EN_3V PR413 0_0402_5%

PR414 0_0402_5%

2.2K_0402_5% PR415

EN_5V3V

@PR421 0_0402_5%

PR420 0_0402_5%

@ PR422 100K_0402_5%

PR423 0_0402_5%

PR424 100K_0402_5%

EN_5VALW [48]

@ PR416 402K_0402_1%

PC416 4.7U_0603_25V6K

@ PJ401 JUMP_43X118

@ PJ405 JUMP_43X118

@ PJ403 JUMP_43X118

@ PJ402 JUMP_43X39

@ PJ404 JUMP_43X39

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 0.1

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Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Vout=0.75V(1+6.04k/10k) =1.205V
OCP= A

Vout=0.8V* (1+Rup/Rdown)

Down size

Down size

Down size

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

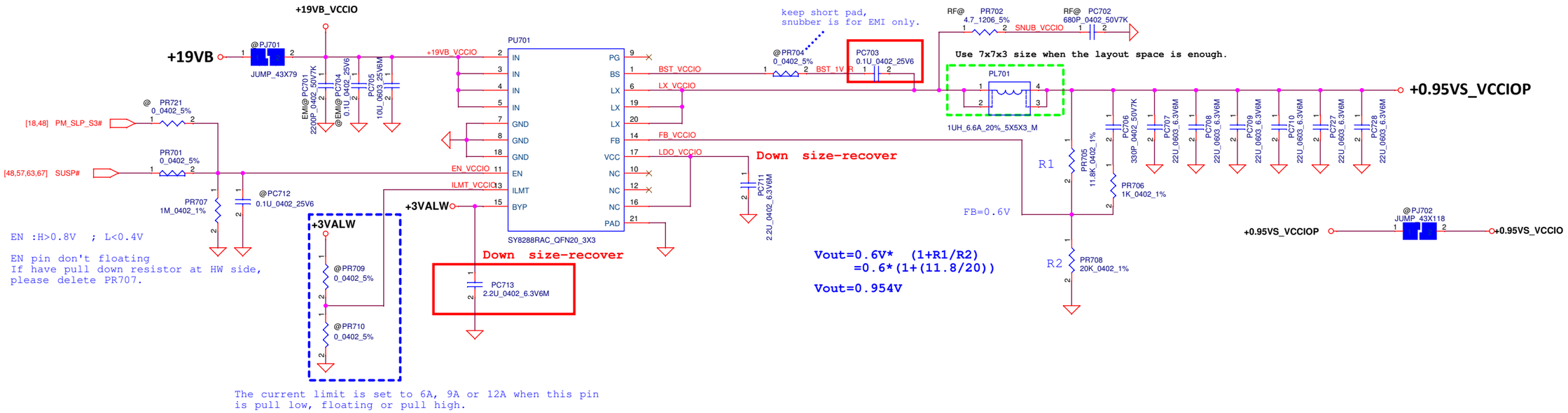
Title: RT8207P

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, January 09, 2019 | Sheet 67 of 81

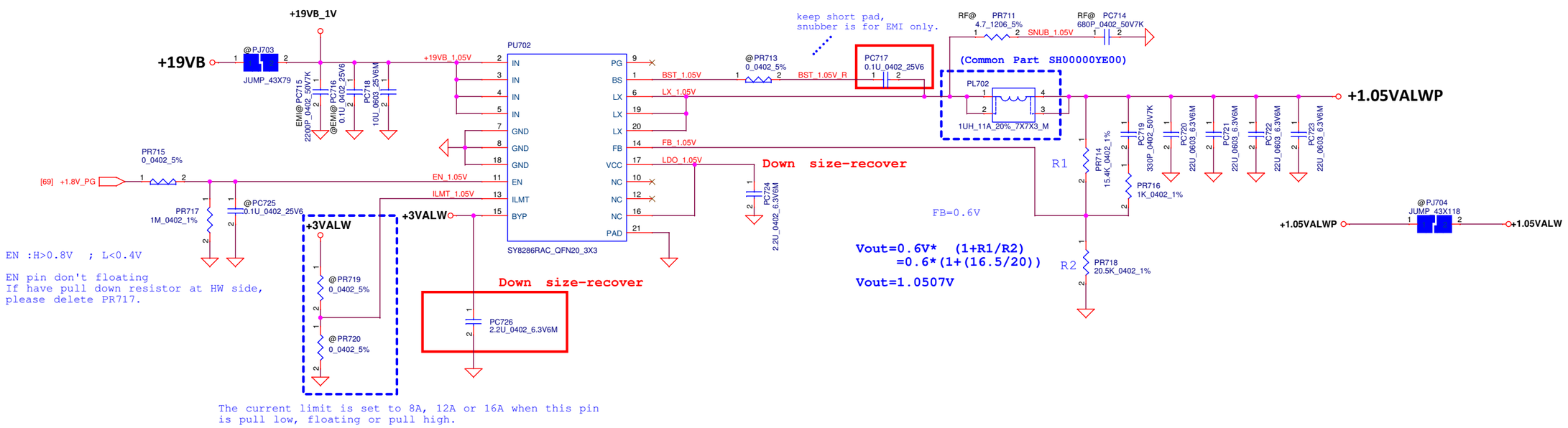
Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



Module model information

SY8288_V2_single.mdd
SY8288_V2_dual.mdd



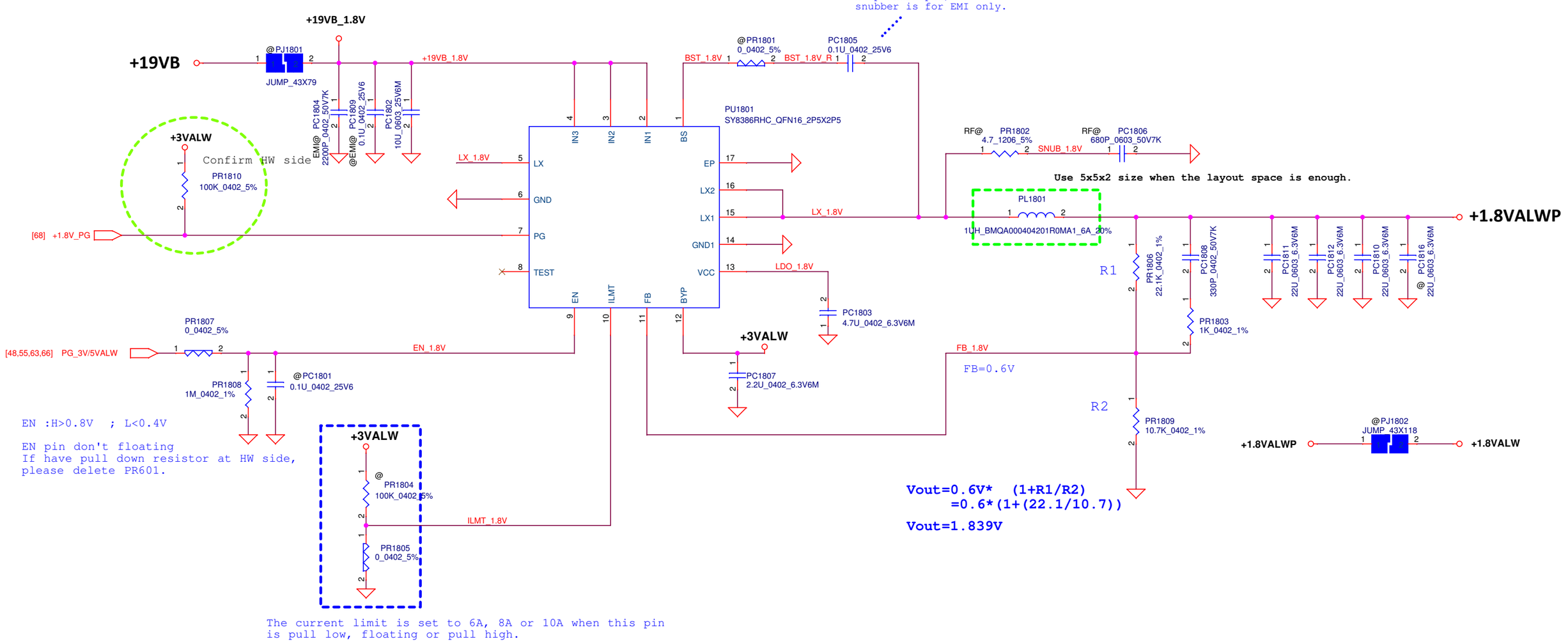
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: SY8286

Size	Document Number	Rev
C		0.1

Date: Wednesday, January 09, 2019 Sheet 68 of 81



Compal Electronics, Inc.

Title: APL5930

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, January 09, 2019 | Sheet 69 of 81

Module model information

NCP81205_H42_V6A.mdd for IC portion

NCP81205_H42_V6B.mdd for SW portion

SKL +Hone	H42(45W)	
TDC@VCORE	56A	
IccMax@VCORE	68A	
OCP@VCORE	75A	
TDC@VGT	39A	
IccMax@VGT	54A	
OCP@VGT	61A	
TDC@VCCSA	10A	
IccMax@VCCSA	11A	
OCP@VCCSA	16.5A	
Fsw	600KHz	
DCR	0.9mohm +/-7%	

VCCSA:

H42: IccMAX@SA= 11A RIccMAX@SA= 34.8K ---> PR109

RIccMAX@SA= IccMAX*2V/10uA/64A

H42: IOUTSP@SA= 11A RIOUTSP@SA=19.6K ---> PR102

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR/(RPHSP+Rth+RCSSP))

H42: OCP@SA= 16.5A RLIMSP@SA=8.45K ---> PR101

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR/(RPHSP+Rth+RCSSP))

Load line@SA= 9.1m

RDRPSP@SA=1.4K ---> PR95

RDRPSP= Load line*(RPHSP+Rth+RCSSP)/(gm * DCR) /(Rth+RCSSP)

CFL-H62 (45W)

IA: Max current=128A, loadline=1.8mohm,

GT: 0~1.52V, Max current=32A, loadline=2.7mohm

SA: 0~1.52V, Max current=11A, loadline=10.3mohm

OCP

IA: 154A

GT: 38.4A

SA: 16.5A

OVP

DAC+370mV

VCCCORE:

H42 OCP@Vcore= 75A RLIM@VCORE=13.7K ---> PR129

RLIM= IoutLIMIT * Load line/10

H42 IccMAX@Vcore= 68A RIccMAX2ph= 52.3K ---> PR154

RIccMAX2ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@Vcore= 68A RIOUT@Vcore=22.6K ---> PR120

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

H42 Load line@VCORE= 1.8m RPH@Vcore=113K ---> PR135,PR137,PR140

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

VCCGT:

H42 OCP@GT= 61A RLIM@GT=16.2K ---> PR130

RLIM= IoutLIMIT * Load line/10

H42 IccMAX@GT= 54A RIccMAX2ph= 42.2K ---> PR150

RIccMAX2ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@GT= 54A RIOUT@GT=24.9K ---> PR126

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

H42 Load line@GT= 2.65m RPH@GT=75K ---> PR139,PR141,PR144

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

Security Classification	Compal Secret Data		
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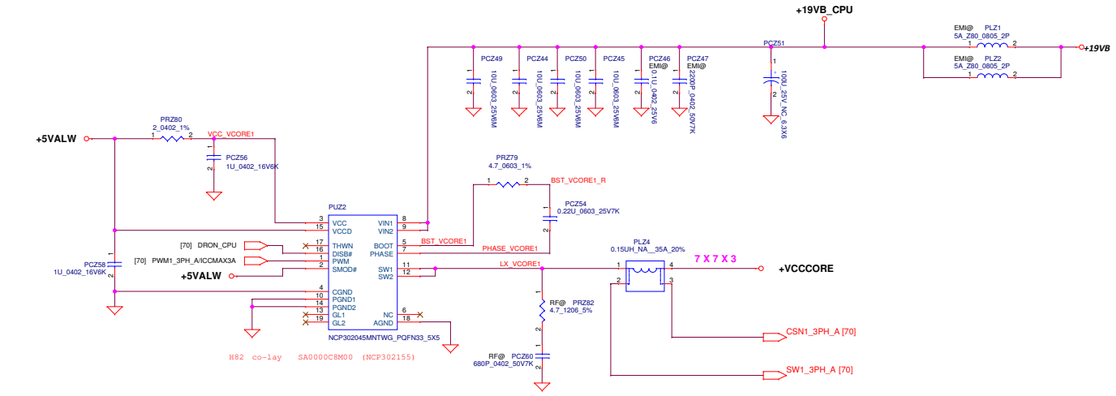
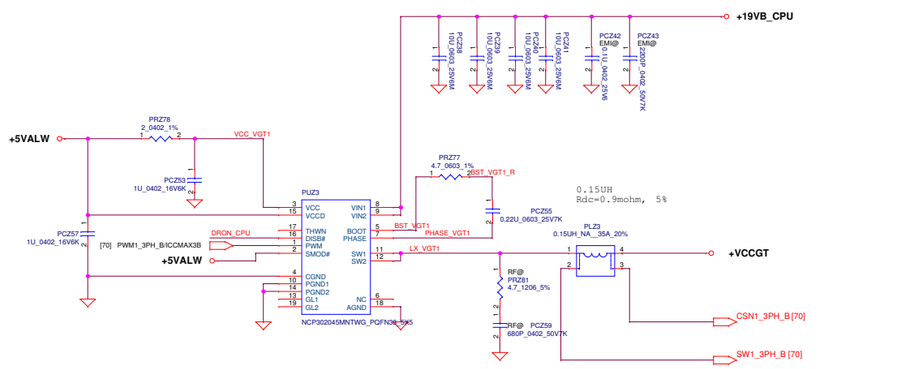
Compal Electronics, Inc.

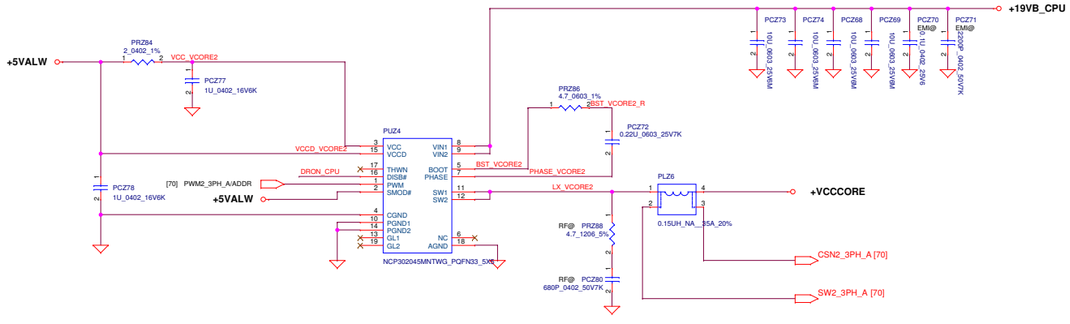
Title: NCP81205 H42

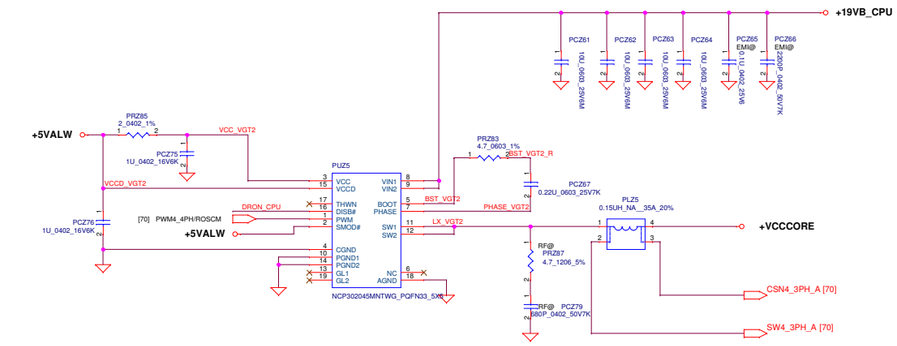
Size: Custom | Document Number | Rev 0.1

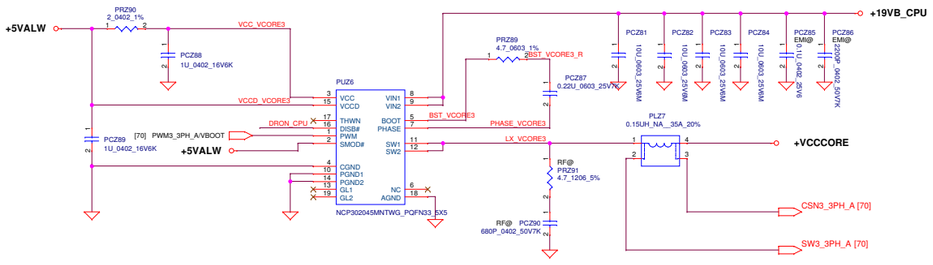
Date: Wednesday, January 09, 2019 | Sheet 70 of 81











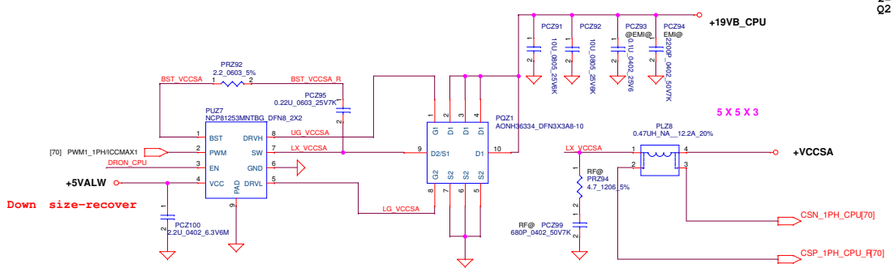
VCC_CORE(3 phase)
TDC 56A(Dual-MOS)
Peak Current 67A
OCP current > 60A
Load line -1.6mV/A (SKL H-44e)
FSW=600kHz
DCR 0.9mohm +/-5%

	TYP	MAX
Q1 Rds(on)	:6.8mohm ,	8.6mohm
Q2 Rds(on)	:2.0mohm ,	2.5mohm

VCCGT(2phase)
TDC 80A(Dual-MOS)
Peak Current 109A
OCP current > 109A
Load line -1.4mV/A (SKL H-44e)

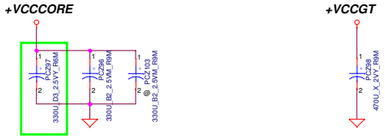
FSW=600kHz
DCR 0.9mohm +/-5%

	TYP	MAX
Q1 Rds(on)	:6.8mohm ,	8.6mohm
Q2 Rds(on)	:2.0mohm ,	2.5mohm



VCCSA
Load line -9.1mV/A
FSW=600kHz
DCR = 6.2 mohm +/- 5%

	TYP	MAX
Q1 Rds(on)	:12.4mohm ,	15.8mohm
Q2 Rds(on)	:9.1mohm ,	11.6mohm



Must review KBL SA rating.

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.
Title: NCP81205_PowerStage
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VCC_CORE Place on CPU Back Side @ V09
22U_0603 *23 pcs+ 1U_0201*30 pcs

SIT(Y730)
22U_0603 *12 pcs+ 1U_0201*48 pcs

Y740 H82
22U_0603 *18 pcs+ 1U_0201*48 pcs
10U_0402 * 42 pcs

+VCCCORE

PC900 22U_0603_6.3V6M @
PC901 22U_0603_6.3V6M
PC902 22U_0603_6.3V6M @
PC903 22U_0603_6.3V6M
PC904 22U_0603_6.3V6M
PC905 22U_0603_6.3V6M
PC906 22U_0603_6.3V6M H82@
PC907 22U_0603_6.3V6M H82@
PC908 22U_0603_6.3V6M H82@
PC909 22U_0603_6.3V6M @
PC910 22U_0603_6.3V6M @
PC911 22U_0603_6.3V6M
PC912 22U_0603_6.3V6M
PC913 22U_0603_6.3V6M @
PC914 22U_0603_6.3V6M H82@
PC1081 22U_0603_6.3V6M @
PC1082 22U_0603_6.3V6M @
PC1083 22U_0603_6.3V6M @

PC930 22U_0603_6.3V6M @
PC931 22U_0603_6.3V6M
PC932 22U_0603_6.3V6M @
PC933 22U_0603_6.3V6M
PC934 22U_0603_6.3V6M
PC935 22U_0603_6.3V6M
PC936 22U_0603_6.3V6M
PC938 22U_0603_6.3V6M @
PC939 22U_0603_6.3V6M @
PC940 22U_0603_6.3V6M
PC942 22U_0603_6.3V6M @
PC943 22U_0603_6.3V6M @
PC944 22U_0603_6.3V6M @
PC937 22U_0603_6.3V6M H82@
PC947 22U_0603_6.3V6M H82@

PC376 1U_0201_6.3V6M
PC977 1U_0201_6.3V6M
PC978 1U_0201_6.3V6M
PC979 1U_0201_6.3V6M
PC980 1U_0201_6.3V6M
PC981 1U_0201_6.3V6M
PC982 1U_0201_6.3V6M
PC983 1U_0201_6.3V6M
PC984 1U_0201_6.3V6M
PC985 1U_0201_6.3V6M
PC986 1U_0201_6.3V6M
PC987 1U_0201_6.3V6M
PC988 1U_0201_6.3V6M
PC989 1U_0201_6.3V6M
PC990 1U_0201_6.3V6M
PC1166 1U_0201_6.3V6M
PC1164 1U_0201_6.3V6M
PC1165 1U_0201_6.3V6M
PC1162 1U_0201_6.3V6M
PC1163 1U_0201_6.3V6M

PC991 1U_0201_6.3V6M
PC992 1U_0201_6.3V6M
PC993 1U_0201_6.3V6M
PC994 1U_0201_6.3V6M
PC995 1U_0201_6.3V6M
PC996 1U_0201_6.3V6M
PC997 1U_0201_6.3V6M
PC998 1U_0201_6.3V6M
PC999 1U_0201_6.3V6M
PC1000 1U_0201_6.3V6M
PC1001 1U_0201_6.3V6M
PC1002 1U_0201_6.3V6M
PC1003 1U_0201_6.3V6M
PC1004 1U_0201_6.3V6M
PC1005 1U_0201_6.3V6M
PC1161 1U_0201_6.3V6M
PC1159 1U_0201_6.3V6M
PC1160 1U_0201_6.3V6M
PC1157 1U_0201_6.3V6M
PC1158 1U_0201_6.3V6M

PC1152 1U_0201_6.3V6M
PC1151 1U_0201_6.3V6M
PC1156 1U_0201_6.3V6M
PC1155 1U_0201_6.3V6M
PC1153 1U_0201_6.3V6M
PC1154 1U_0201_6.3V6M
PC1149 1U_0201_6.3V6M
PC1150 1U_0201_6.3V6M

PC1107 10U_0402_6.3V6M H82@
PC1108 10U_0402_6.3V6M H82@
PC1109 10U_0402_6.3V6M H82@
PC1110 10U_0402_6.3V6M H82@
PC1111 10U_0402_6.3V6M H82@
PC1112 10U_0402_6.3V6M H82@
PC1113 10U_0402_6.3V6M H82@
PC1114 10U_0402_6.3V6M H82@
PC1115 10U_0402_6.3V6M H82@
PC1116 10U_0402_6.3V6M H82@
PC1117 10U_0402_6.3V6M H82@
PC1118 10U_0402_6.3V6M H82@
PC1119 10U_0402_6.3V6M H82@
PC1120 10U_0402_6.3V6M H82@
PC1121 10U_0402_6.3V6M H82@
PC1122 10U_0402_6.3V6M H82@
PC1123 10U_0402_6.3V6M H82@
PC1124 10U_0402_6.3V6M H82@
PC1125 10U_0402_6.3V6M H82@
PC1126 10U_0402_6.3V6M H82@

PC1127 10U_0402_6.3V6M H82@
PC1128 10U_0402_6.3V6M H82@
PC1129 10U_0402_6.3V6M H82@
PC1130 10U_0402_6.3V6M H82@
PC1131 10U_0402_6.3V6M H82@
PC1132 10U_0402_6.3V6M H82@
PC1133 10U_0402_6.3V6M H82@
PC1134 10U_0402_6.3V6M H82@
PC1135 10U_0402_6.3V6M H82@
PC1136 10U_0402_6.3V6M H82@
PC1137 10U_0402_6.3V6M H82@
PC1139 10U_0402_6.3V6M H82@
PC1138 10U_0402_6.3V6M H82@
PC1140 10U_0402_6.3V6M H82@
PC1141 10U_0402_6.3V6M H82@
PC1142 10U_0402_6.3V6M H82@
PC1144 10U_0402_6.3V6M H82@
PC1143 10U_0402_6.3V6M H82@
PC1145 10U_0402_6.3V6M H82@
PC1146 10U_0402_6.3V6M H82@

PC1147 10U_0402_6.3V6M H82@
PC1148 10U_0402_6.3V6M H82@

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 16 pcs +1U_0201* 20pcs

+VCCGT

PC915 22U_0603_6.3V6M
PC916 22U_0603_6.3V6M @
PC917 22U_0603_6.3V6M
PC918 22U_0603_6.3V6M
PC919 22U_0603_6.3V6M @
PC920 22U_0603_6.3V6M @
PC921 22U_0603_6.3V6M
PC922 22U_0603_6.3V6M @
PC923 22U_0603_6.3V6M
PC924 22U_0603_6.3V6M
PC925 22U_0603_6.3V6M
PC926 22U_0603_6.3V6M @
PC927 22U_0603_6.3V6M @
PC928 22U_0603_6.3V6M @
PC929 22U_0603_6.3V6M @

PC945 22U_0603_6.3V6M
PC946 22U_0603_6.3V6M
PC947 22U_0603_6.3V6M
PC948 22U_0603_6.3V6M
PC949 22U_0603_6.3V6M @
PC950 22U_0603_6.3V6M @
PC951 22U_0603_6.3V6M
PC952 22U_0603_6.3V6M @
PC953 22U_0603_6.3V6M

PC961 1U_0201_6.3V6M
PC962 1U_0201_6.3V6M
PC963 1U_0201_6.3V6M
PC964 1U_0201_6.3V6M
PC965 1U_0201_6.3V6M
PC966 1U_0201_6.3V6M
PC967 1U_0201_6.3V6M
PC968 1U_0201_6.3V6M
PC969 1U_0201_6.3V6M
PC970 1U_0201_6.3V6M
PC971 1U_0201_6.3V6M
PC972 1U_0201_6.3V6M
PC973 1U_0201_6.3V6M
PC974 1U_0201_6.3V6M
PC975 1U_0201_6.3V6M

PC1006 1U_0201_6.3V6M
PC1007 1U_0201_6.3V6M
PC1008 1U_0201_6.3V6M
PC1009 1U_0201_6.3V6M
PC1010 1U_0201_6.3V6M

VCC_SA Place on CPU Back Side @ V09
22U_0603 *7pcs +1U_0201* 3pcs

+VCCSA

PC1084 22U_0603_6.3V6M
PC1085 22U_0603_6.3V6M
PC1086 22U_0603_6.3V6M
PC1087 22U_0603_6.3V6M @
PC1088 22U_0603_6.3V6M
PC1089 22U_0603_6.3V6M
PC1090 22U_0603_6.3V6M
PC1091 22U_0603_6.3V6M
PC1092 22U_0603_6.3V6M @
PC1093 22U_0603_6.3V6M @
PC1094 22U_0603_6.3V6M @
PC1095 22U_0603_6.3V6M @
PC1096 1U_0201_6.3V6M
PC1097 1U_0201_6.3V6M
PC1098 1U_0201_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

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Title: PWR-PROCESSOR_DECOUPLING

Size: C | Document Number | Rev: 0.1

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Config	
Vmin	0.3
Vmax	1.3
Vboot	0.8
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	309
C	4.7n

Place close to GPU pins

1M ohm for OCP=80A

Security Classification	Compal Secret Data
Issued Date	2018/7/31
Deciphered Date	2018/7/31

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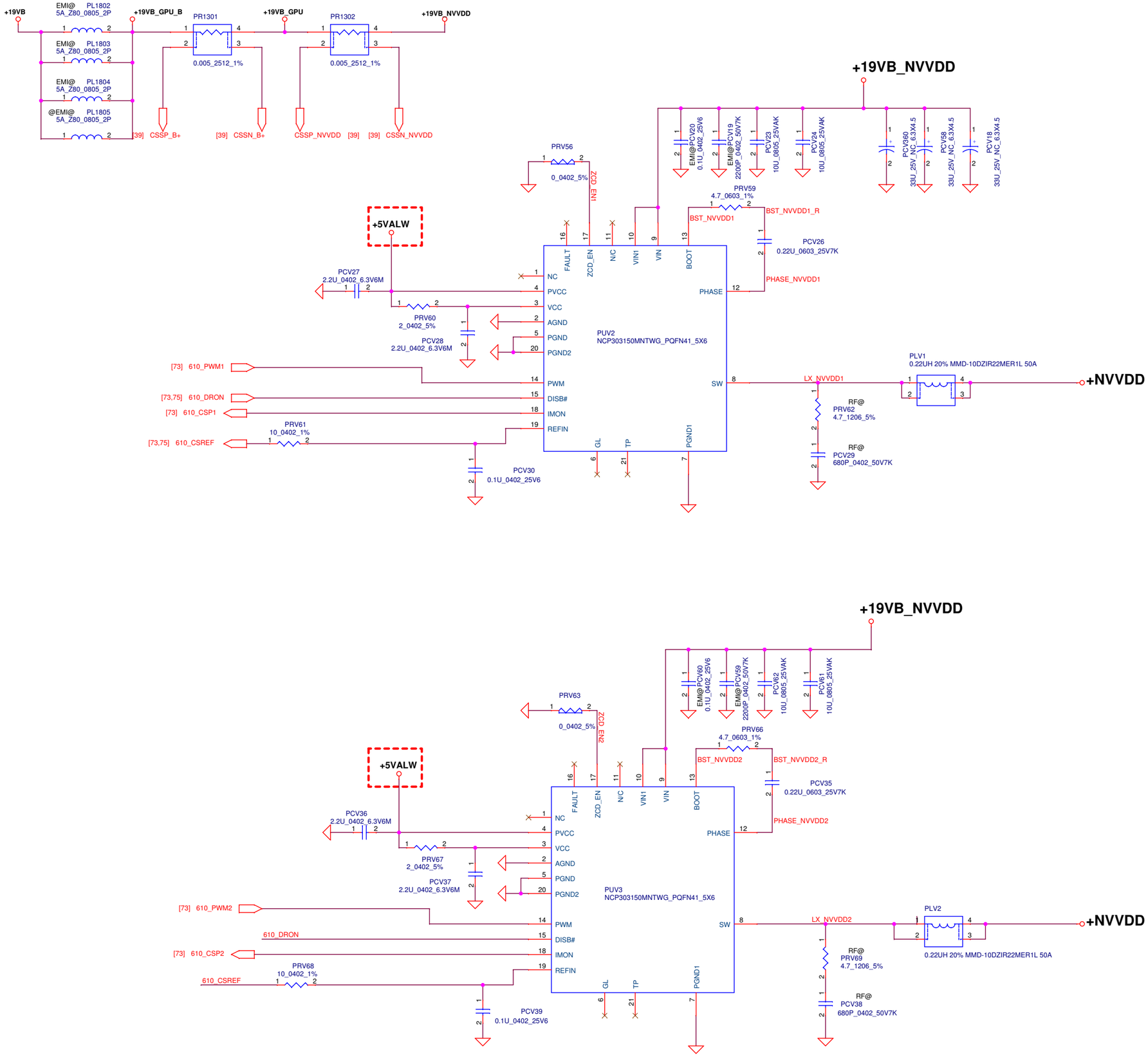
Compal Electronics, Inc.

Title: **VGA CORE**

Size	Document Number	Rev
		0.1

Date: Wednesday, January 09, 2019 Sheet 73 of 81



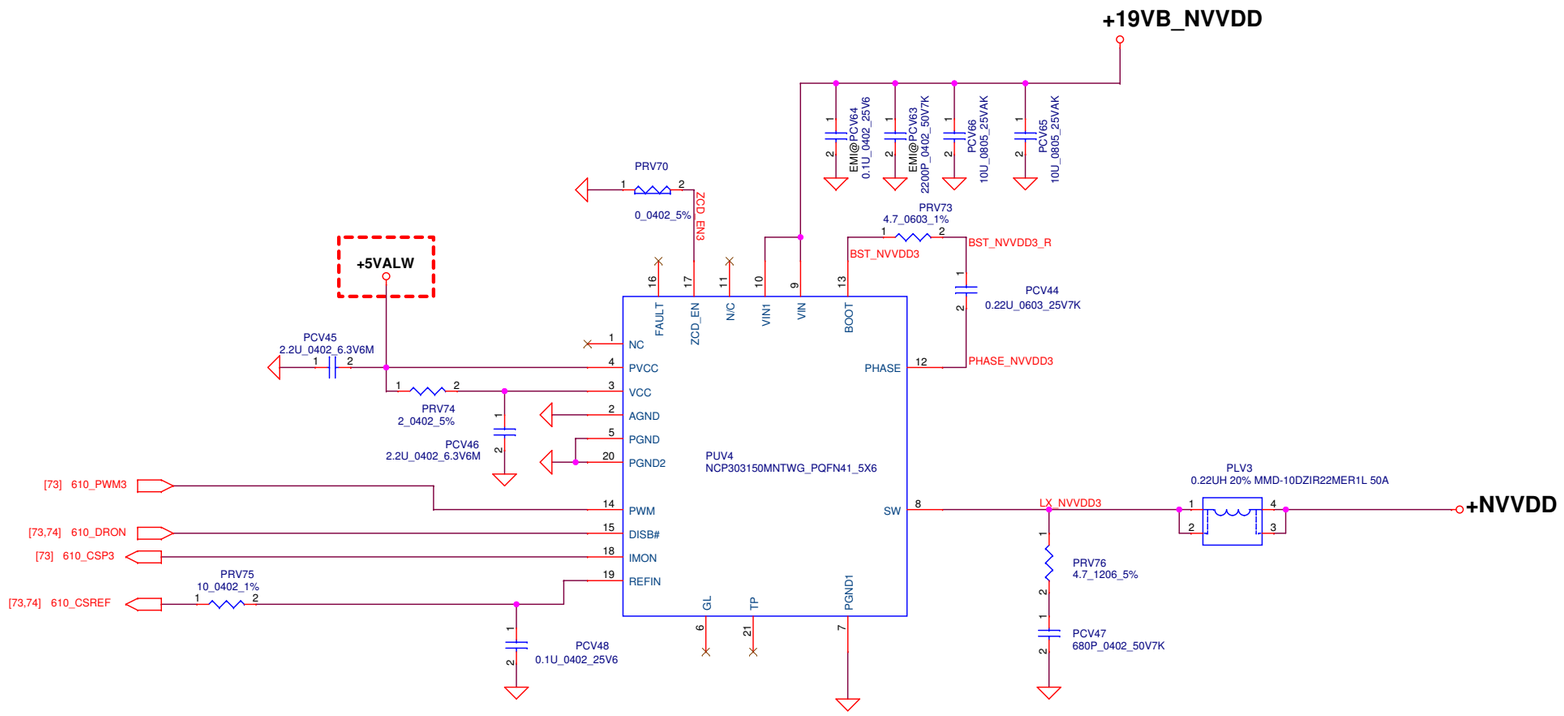
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
		0.1

Date: Wednesday, January 09, 2019 | Sheet 74 of 81



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: ***PWR_+NVVDD1***

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Place near GPU

+NVVDD

D2 B2 D3

470U_D2_2VM_R4.5M PCV135
470U_D2_2VM_R4.5M PCV137
470U_D2_2VM_R4.5M @ PCV136
330U_B2_2.5VM_R9M PCV138
330U_B2_2.5VM_R9M PCV358
330U_B2_2.5VM_R9M PCV359
330U_D3_2.5VY_R6M PCV401
330U_D3_2.5VY_R6M PCV402
330U_D3_2.5VY_R6M PCV403

N18E-G2
+NVVDD
470uF X 2
330uF X 6
47uF_0603 X 3
22uF_0603 X 4 +7
10uF_0402X 22
1uF_0201 X 94 +17
10uF_0603 X 3

Reserve

N17E-G3
+NVVDD
470uF X 11
47uF_0805 X 3
10uF_0603X 27
4.7uF_0603 X 11
1uF_0402 X 65

Place under GPU

PCV251 PCV140 PCV141 PCV142 PCV143 PCV144 PCV145 PCV146 PCV147 PCV148 PCV149 PCV150 PCV152 PCV153 PCV154 PCV157 PCV158
PCV159 PCV160 PCV161 PCV162 PCV163 PCV164 PCV165 PCV166 PCV167 PCV168 PCV170 PCV169 PCV172 PCV171 PCV173 PCV175 PCV174 PCV177 PCV176 PCV178
PCV179 PCV180 PCV181 PCV182 PCV183 PCV184 PCV185 PCV186 PCV187 PCV188 PCV190 PCV189 PCV193 PCV191 PCV192 PCV194 PCV195 PCV196 PCV197 PCV198
PCV199 PCV201 PCV200 PCV203 PCV202 PCV204 PCV205 PCV206 PCV207 PCV208 PCV209 PCV210 PCV211 PCV212 PCV213 PCV214 PCV235 PCV236 PCV237 PCV238
PCV252 PCV253 PCV254 PCV256 PCV257 PCV258 PCV259 PCV260 PCV261 PCV262 PCV263 PCV264 PCV265 PCV266
PCV410 PCV411 PCV412 PCV413 PCV414

All 1U_0201_6.3V6M

+NVVDD

PCV215 PCV216 PCV217 PCV218 PCV219 PCV220 PCV221 PCV222 PCV223 PCV224 PCV225 PCV226 PCV227 PCV229 PCV228 PCV230 PCV231 PCV232 PCV233 PCV234
All 10U_0402_6.3V6M

PCV239 PCV240 PCV241 PCV242 PCV243 PCV244 PCV245 PCV246 PCV247 PCV248
10U_0402_6.3V6M; 47U_0603_6.3V6M; 22U_0603_6.3V6M

PCV404 PCV405 PCV406 PCV407 PCV408 PCV409
22U_0603_6.3V6M

PCV415 PCV416 PCV417
10U_0402_6.3V6M; 22U_0603_6.3V6M

PCV418 PCV419 PCV420 PCV421 PCV422 PCV423 PCV424 PCV425 PCV426 PCV427 PCV428 PCV429
1U_0201_6.3V6M

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side)[1]		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

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Title: PWR_VGA DECOUPLING

Size: | Document Number: LA-G132P | Rev: 0.1

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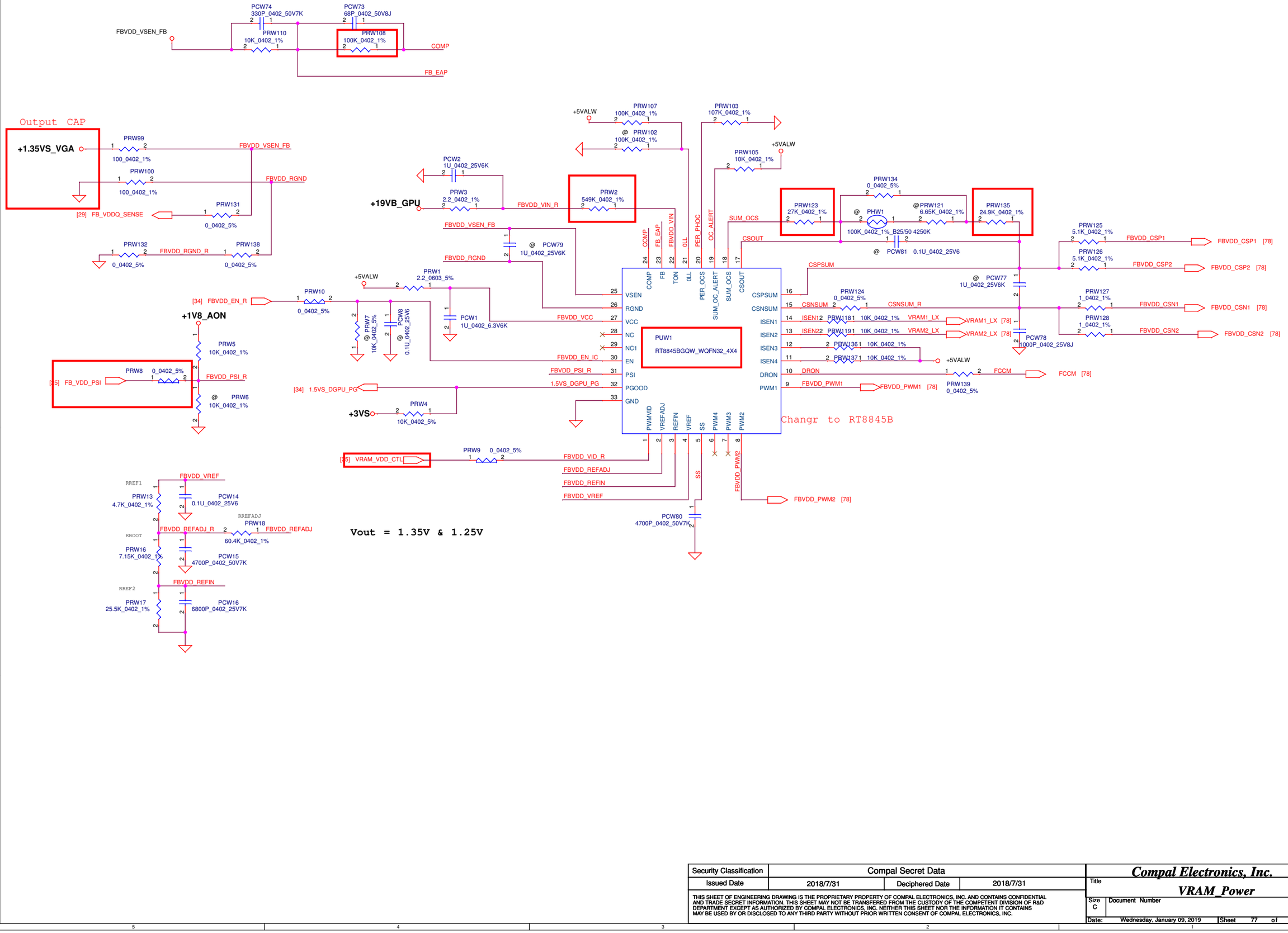

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **VRAM_Power**

Size	Document Number	Rev
C		0.1

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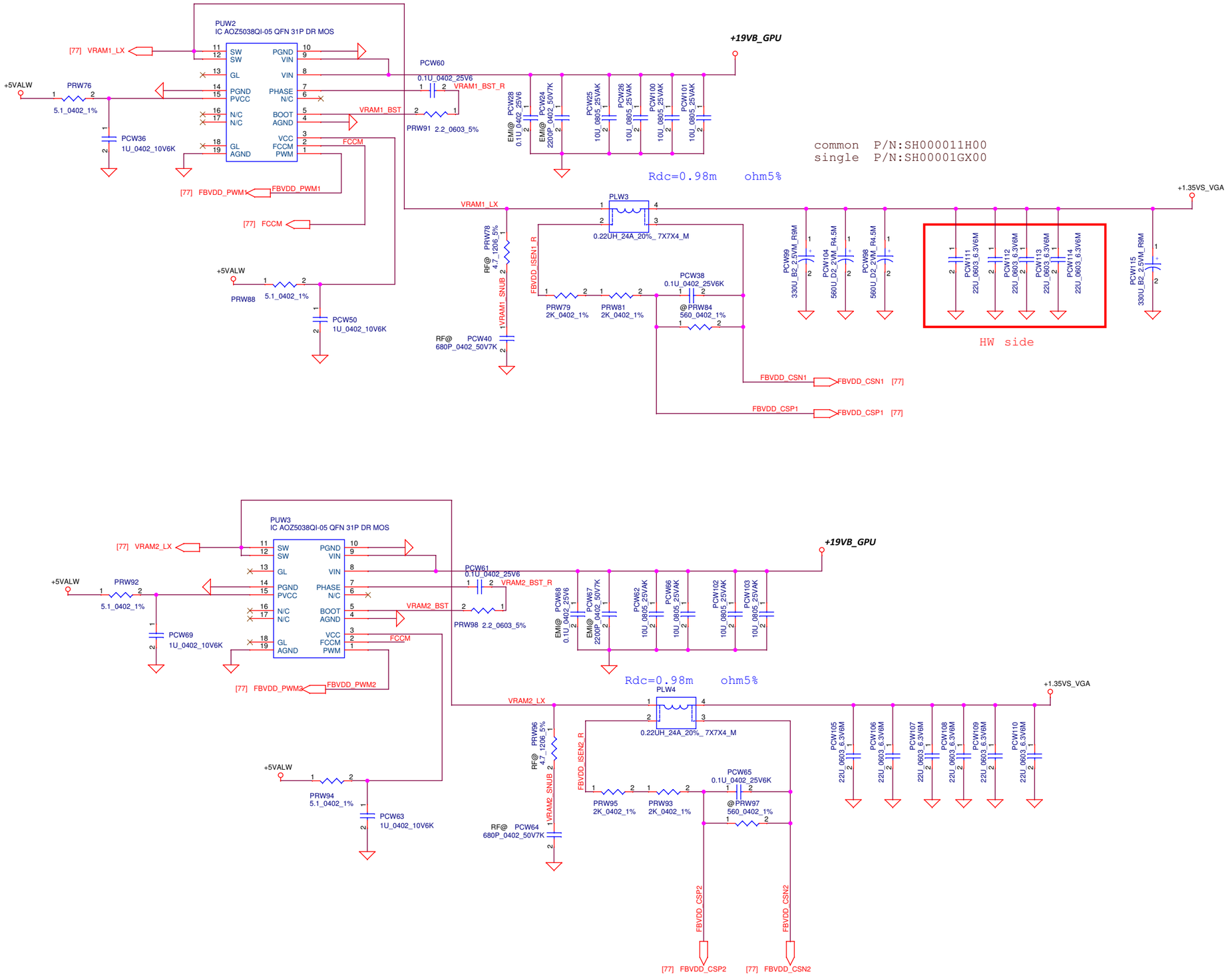

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **VRAM_Power**

Size	Document Number	Rev
C		0.1

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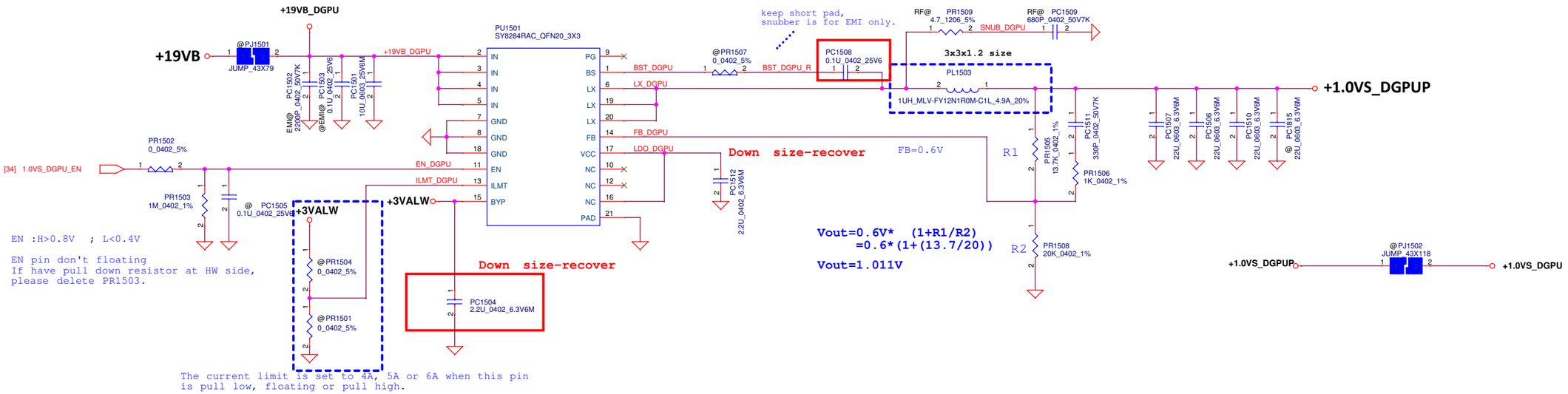
Module model information

SY8288_V2_single.mdd
SY8288_V2_dual.mdd



Compal Electronics, Inc.

Title: **PWR_+1.55VRAM**

Size	Document Number	Rev
		0.1

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	FAE Suggest	74,75	PRV56, PRV63 , PRV70 , PRV77 PIN1 from +5VALW change to GND.	8/28	SDV2
2	NVIDIA Suggest	76	Add PCV404 , PCV405 , PCV406 , PCV407 , PCV408 , PCV409 (22U_0603)	8/28	SDV2
3	Power Design	78	Reserved PCW104 (560U_D2) Add PCW105 ,PCW106, PCW107 ,PCW108 ,PCW109 , PCW110 (22u_0603)	9/05	SDV2
4	Power Design	77	Add PRW138 , 0_0402	9/05	SDV2
5	SDV1 fine tuning ,FAE Suggest	73	Reserved PR1052, PR1057,PR1059 , PR1055 ,PC1019 ,PU1001	9/05	SDV2
6	NVIDIA Suggest	76	Add PCV410,PCV411,PCV412,PCV413,PCV414 (1U_0201) , PCV415,PCV416 PCV146 (10U_0402), PCV417 (22U_0603)	9/06	SDV2
7	NVIDIA Suggest,For better power stability.	78	PCW104 & PCW98 From 330U_D2 change to 560U_D2. PCV135 & PCV137 From 470U_D2 change to 560U_D2.	9/07	SDV2
8	Sourcer Suggest	56,67,77	PC505 from SE00000W210 (0.1U 25V K X7R 0402) change to SE00000G880 (0.1U 25V K X5R 0402) PCW78 from SE00000H180 (1000P 50V J NPO 0402) change to SE068102J80 (1000P 25V J NPO 0402) PC309 from 0.22 change to SE00000HQ00 (0.47U 25V K X7R 0603)	9/10	SDV2
9	Power Design	78	PLW3 & PLW4 From 0.15uH change to 0.24uH PRW125, PRW126 From 5k change to 4.02k PRW123 From 5.76k change to 37.4k	9/10	SDV2
10	FAE Suggest	73	Mount PR1052 ,PR1057,PR1055,PC1019,PU1001. Unmount PRV85 ,PRV86 PRV39 , PRV40 ,PRV42 ,PRV44 From 309 change to 715 ohm PCV13, PCV14 ,PCV16 , PCV17 From 100P change to 47P PRV43 , PRV45 ,PRV47 ,PRV49 From 110k change to 301k PRV31 From 280k change to 261k, PRV29 From 17.4k change to 21.5k, PRV30 From 76.8k change to 200k.	9/10	SDV2
11	Power Design for GPU PDN	76	PCV410 , PCV411 ,PCV412 , PCV413, PCV414 From 1u_0201 change to 4700P_0201	9/14	SDV2
12	HW Suggest	77	PRW10 From 0_0402 change to 5k_0402, 9 /25 change to R-short for SIT	9/21	SDV2
13	HW Suggest	77	change net name : FBVDD_EN_R change to FBVDD_EN_IC , FBVDD_EN change to FBVDD_EN_R	9/25	SIT
14	FAE Suggest	73	PCW10 From 3300P_0402 change to 0.01U_0402_50V7K	9/25	SIT
15	For GPU PI simulation	76	Add location PCV418-PCV429 (4700P_0201_6.3V7K)	10/04	SIT
16	For Auto-PSI	73	Add location PRV87-90 (Reserved)	10/04	SIT
17	Power Design	64	Add location PR211 (Reserved)	10/04	SIT
18	Power Design	73	PCV225,PCV228,PCV232 change to 0603size	10/04	SIT
19	Power Design	74,75,78	PLW3 & PLW4 From 0.24uH (7x7x3) change to 0.22uH (7x7x4) PLV1,PLV2,PLV3,PLV4 From 0.15UH change to 0.22UH (10x10x4) PRW125, PRW126 change to 5.1k PRW123 change to 27k	10/04	SIT
20	EMI Suggest	78	Mount PCW68, PCW28	10/04	SIT
21	EMI Suggest	73	Add PRV91 , PRV94 , PRV95 , PRV96 , PR6108 (Reserved)	10/08	SIT
22	Psys setting	70	PR151 From 12.7k change to 11.5k	10/09	SIT
23	CPU Test results , FAE Suggest	70	PR126 From 26.7k change to 28k	10/09	SIT
24	CPU Test results , FAE Suggest	76	PCV410-PCV414 & PCV418-PCV429 from 4700P_0202 change to 1u_0201	10/11	SIT
25	PJE	74,75	PUV2,PUV3,PUV4,PUV5 From SA0000CAD00 (NCP303150) change to SA0000C6900 (NCP303151) PL1801 From SH00001T800 change to SH00001A200	10/12	SIT
26	For GPU FAE Suggest	74,75	UnmountPRV10	10/12	SIT
27	Power Design, FAE Suggest	65	PR310 from 49.9k change to 48.7k	10/30	SVT
28	Power Design, FAE Suggest	77	Unmount PCW77 PCW74 from 270P change to 330P ,PCW73 from 150P change to 68P PCW16 from 4700P change to 6800P,PRW108 from 53.6k change to 100k PRW135 from 36k change to 24.9k	10/30	SIT MEMO SVT
29	Power Design, FAE Suggest	77	Remove PRW117,PQW1,PRW116&PCW76 Add PRW139 PCW16 from SE00000UL80 change to SE075682K80	11/06	SVT
30	Power Design R-short		PR701,PR715,PR1807,PR1502,PRV11,PRV1,PRV7,PRV7,PRV9,PRV14,PRW8,PRW9 ,PRV56,PRV63,PRV70,PRV77,PR420,PR423Change to R-short	11/14	SVT
31	Power Design,for FBVDD Transient	77	Add PCW111,PCW112,PCW113,PCW114 Add PCW115 PRW16 from 7.87K change to 7.15K	11/16	SVT
32	NV Suggest.	69	PR1806 change to 22.1K,PR1809 change to 10.7K	11/16	SVT
33					
34					

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Title: **PIR (PWR)**

Size	Document Number	Rev
Custom		0.1

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Follow NV review result	27,29,31	Change 4.7u 0603 to 0402	2018/08/20	SDV2
2		25	Add 10K Ohm serial resistor ahead of QG515 gate pin	2018/08/20	SDV2
3		24	Change 1U 0201 to 0.47U 0201	2018/08/20	SDV2
4		24	Add 1.0VS_DGPU,1V8_MAIN 0.47U 0201	2018/08/20	SDV2
5	Follow NV review result	33	Add 0.47U 0201	2018/08/23	SDV2
6	Add the BOM Structure	39	Add OVR-M N18G2@ , N18G0@	2018/09/05	SDV2
7	Follow NV review result	33	Add 330U B2,D3 reserve	2018/09/06	SDV2
8	Change the BOM Structure	38	Change the BOM Structure NOG3G2@ chamge to G3G2@ for N18G1,N18G0	2018/09/27	SIT
9	Follow NV review result	39	Change OVR-M BOM(RG222,RG228,RG225,RG226,RG227,RG259,CG341,CG342)	2018/09/27	SIT
10	Change GPU_ID1,ID for N18G0,G1,G2,G3	19	RH225,RH226,RH195,RH194	2018/10/01	SIT
11	Down size 0402 to 0201	10,20,22 23,62,63	CD1,CD11,CD14,CD60,CD69,CD72,CD81,CH15,CH34,CH75,CH76,C151,C155,CBL28	2018/10/03	SIT
12	Down size 0603 to 0402	59	CT260	2018/10/03	SIT
13	0 ohm change R-SHORT	24,25,39,50	RG236,RG507,RG537,RL18	2018/10/03	SIT
14	Change the BOM Structure	32	For N18G0,G1(G3G2@) RG236,RG507,RG537,RL18	2018/10/03	SIT
15	Add GPIO19 for THERM_ALERT#_EC_R ,BEEP#	48	R642,R643	2018/10/03	SIT
16	0 ohm change to R-Short	24,26,34 39,48,50	RL40,R642,RG4,RG76,RG644,RG1521,RG1522,RG239,RG241,RG1533,RG1534,RG1564	2018/11/13	SVT
17	Add 0 ohm for +3V_OVRM	39	RG1569,RG1570	2018/12/3	SOVP

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Title: **PIR (EE)**

Size	Document Number	Rev
Custom		1.0

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