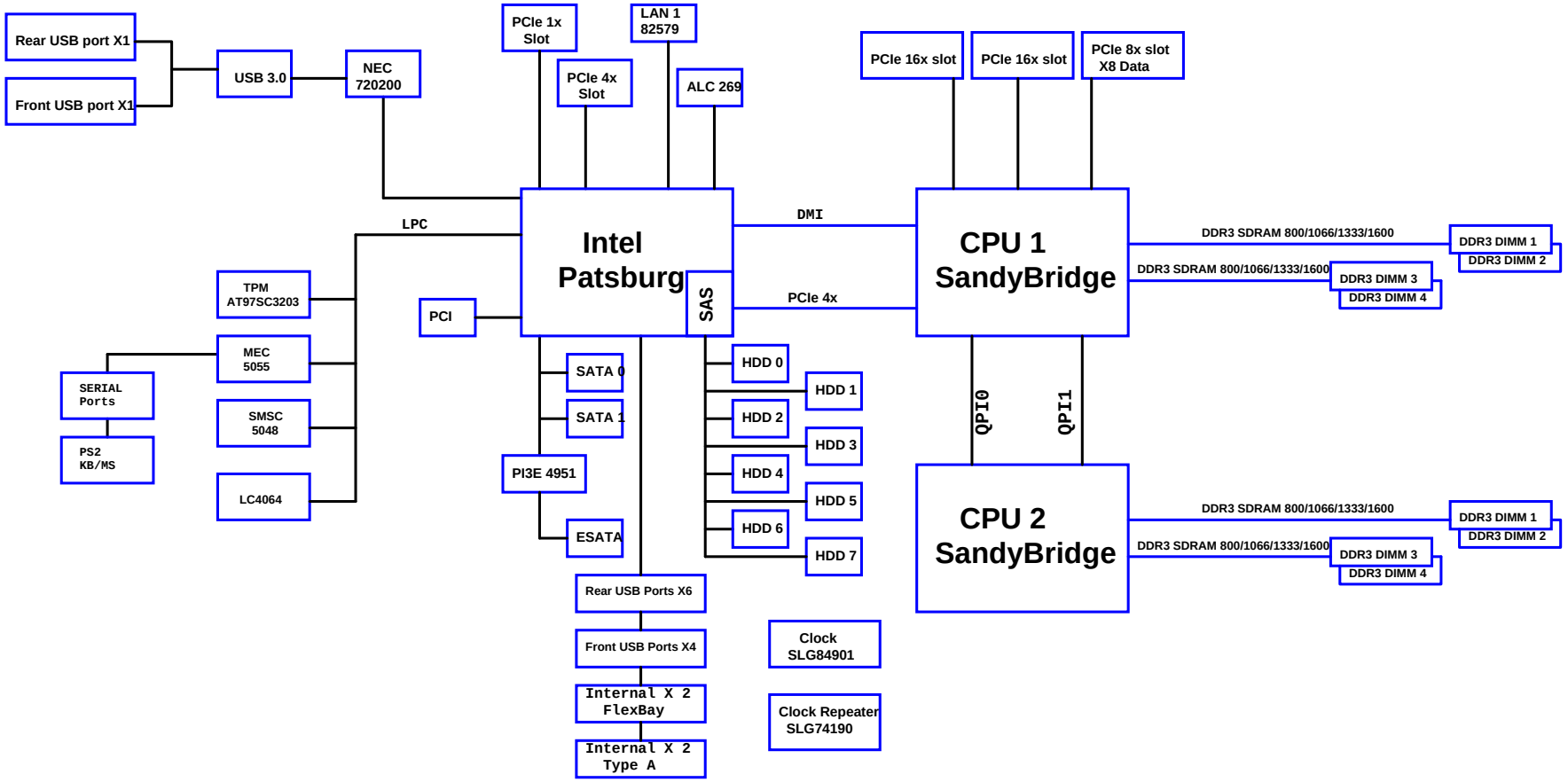
Little Sur



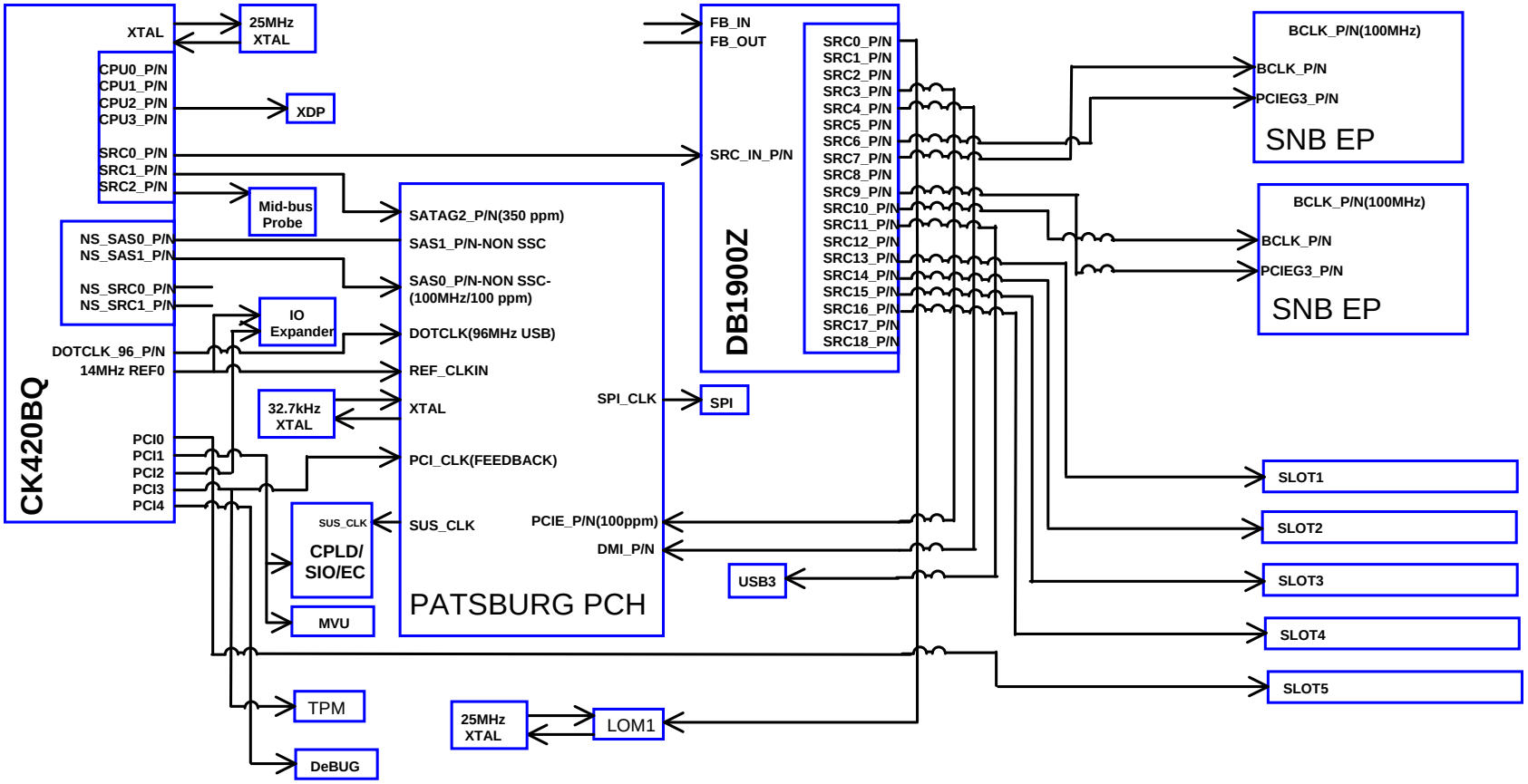
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 1 of 96



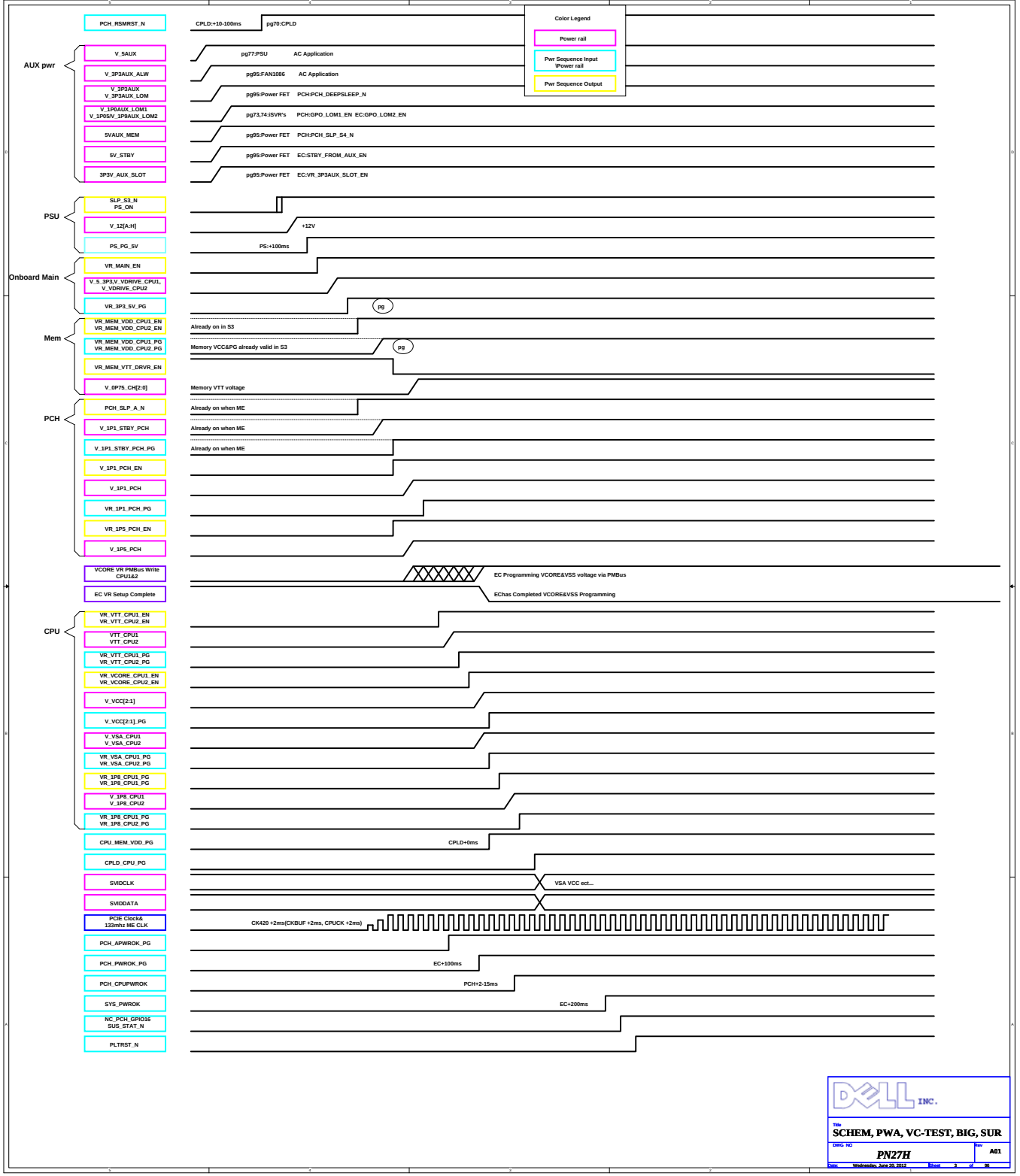
DELL INC.

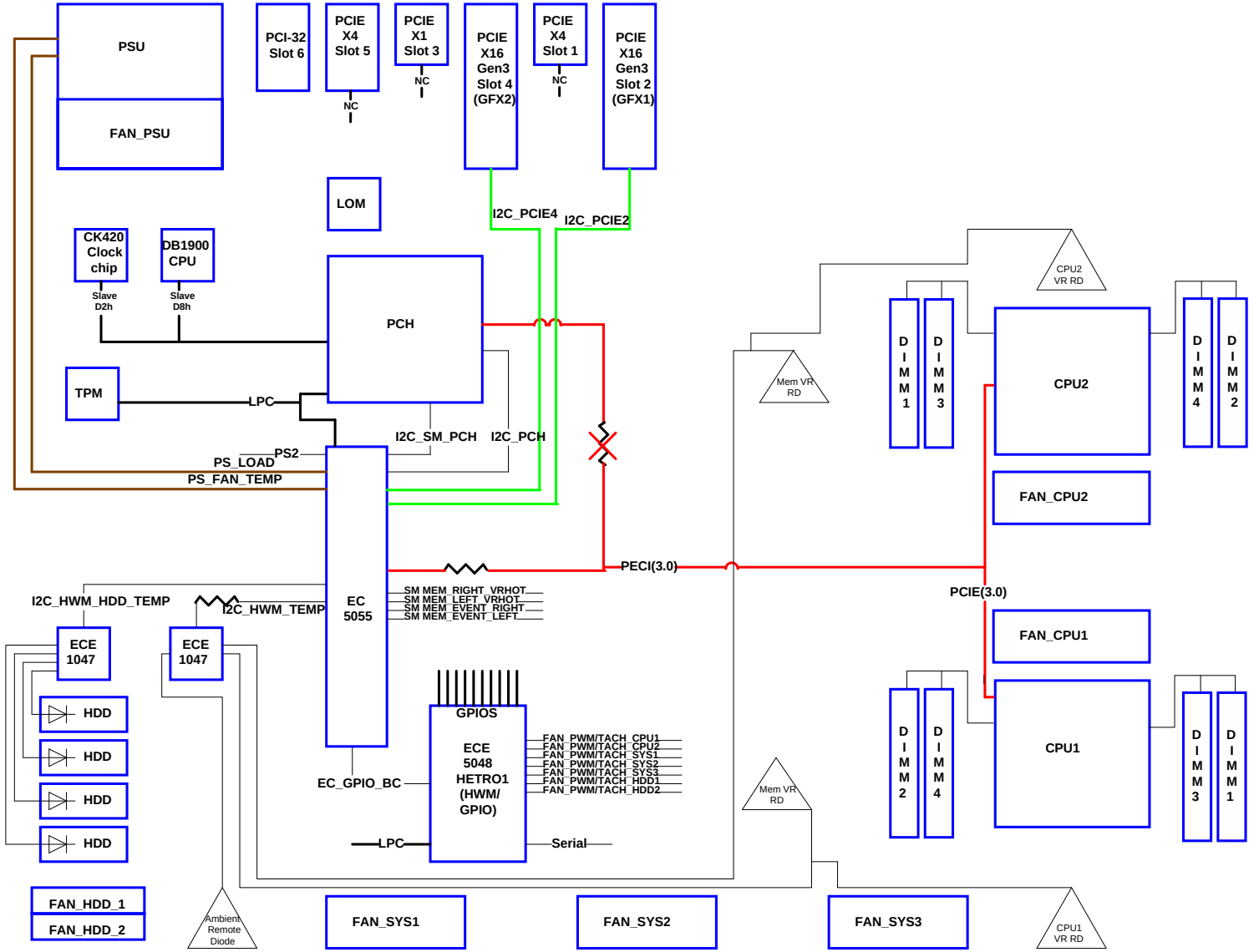
Title
SCHEM, PWA, VC-TEST, BIG, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 2 of 96


PCH_RSMRST_N
CPLD:+10-100ms
pg70:CPLD
Color Legend
Power rail
Pwr Sequence Input \Power rail
Pwr Sequence Output
AUX pwr
V_5AUX
V_3P3AUX_ALW
V_3P3AUX V_3P3AUX_LOM
V_1P0AUX_LOM1 V_1P05/V_1P8AUX_LOM2
5VAUX_MEM
5V_STBY
3P3V_AUX_SLOT
pg77:PSU AC Application
pg95:FAN1086 AC Application
pg95:Power FET PCH:PCH_DEEPSLEEP_N
pg73,74:iSVR's PCH:GPO_LOM1_EN EC:GPO_LOM2_EN
pg95:Power FET PCH:PCH_SLP_S4_N
pg95:Power FET EC:STBY_FROM_AUX_EN
pg95:Power FET EC:VR_3P3AUX_SLOT_EN
PSU
SLP_S3_N PS_ON
V_12[A:H]
PS_PG_5V
+12V
PS:+100ms
Onboard Main
VR_MAIN_EN
V_S_3P3,V_VDRIVE_CPU1, V_VDRIVE_CPU2
VR_3P3_5V_PG
pg
Mem
VR_MEM_VDD_CPU1_EN VR_MEM_VDD_CPU2_EN
VR_MEM_VDD_CPU1_PG VR_MEM_VDD_CPU2_PG
VR_MEM_VTT_DRVR_EN
V_0P75_CH[2:0]
Already on in S3
Memory VCC&PG already valid in S3
pg
Memory VTT voltage
PCH
PCH_SLP_A_N
V_1P1_STBY_PCH
V_1P1_STBY_PCH_PG
V_1P1_PCH_EN
V_1P1_PCH
VR_1P1_PCH_PG
VR_1P5_PCH_EN
V_1P5_PCH
Already on when ME
Already on when ME
Already on when ME
VCORE VR PMBus Write CPU1&2
EC VR Setup Complete
EC Programming VCORE&VSS voltage via PMBus
EChas Completed VCORE&VSS Programming
CPU
VR_VTT_CPU1_EN VR_VTT_CPU2_EN
VTT_CPU1 VTT_CPU2
VR_VTT_CPU1_PG VR_VTT_CPU2_PG
VR_VCORE_CPU1_EN VR_VCORE_CPU2_EN
V_VCC[2:1]
V_VCC[2:1]_PG
V_VSA_CPU1 V_VSA_CPU2
VR_VSA_CPU1_PG VR_VSA_CPU2_PG
VR_1P8_CPU1_PG VR_1P8_CPU1_PG
V_1P8_CPU1 V_1P8_CPU2
VR_1P8_CPU1_PG VR_1P8_CPU2_PG
CPU_MEM_VDD_PG
CPLD_CPU_PG
SVIDCLK
SVIDDATA
PCIE Clock& 133mhz ME CLK
PCH_APWROK_PG
PCH_PWROK_PG
PCH_CPUPWROK
SYS_PWROK
NC_PCH_GPIO16 SUS_STAT_N
PLTRST_N
CPLD+0ms
VSA VCC ect...
CK420 +2ms(CKBUF +2ms, CPUCK +2ms)
EC+100ms
PCH+2-15ms
EC+200ms
DELL INC.
Title
SCHEM, PWA, VC-TEST, BIG, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 3 of 96



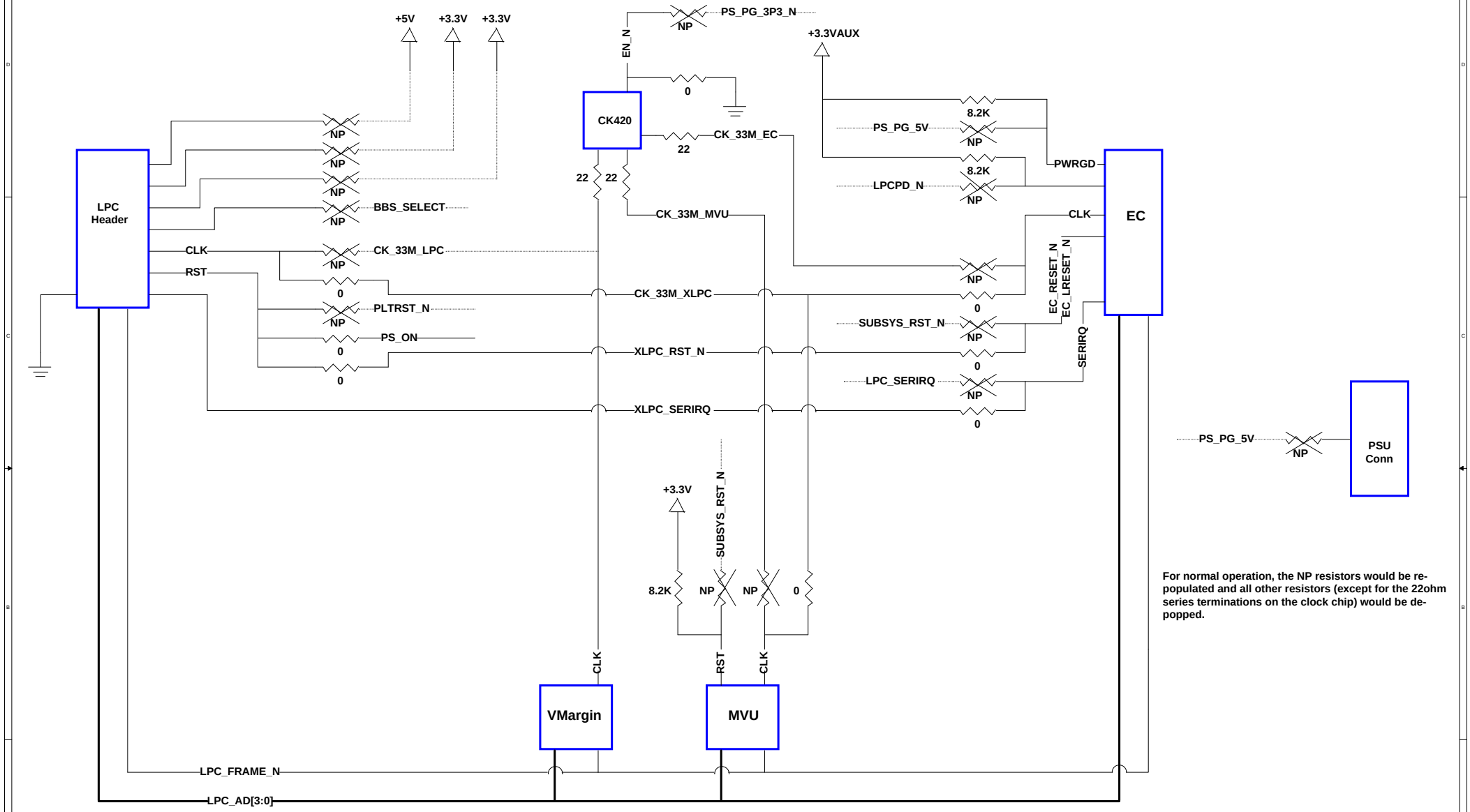
DELL INC.

Title
SCHEM, PWA, VC-TEST, BIG, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 4 of 96



For normal operation, the NP resistors would be re-populated and all other resistors (except for the 22ohm series terminations on the clock chip) would be de-popped.

DELL INC.

Title
SCHEM, PWA, VC-TEST, BIG, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 5 of 96

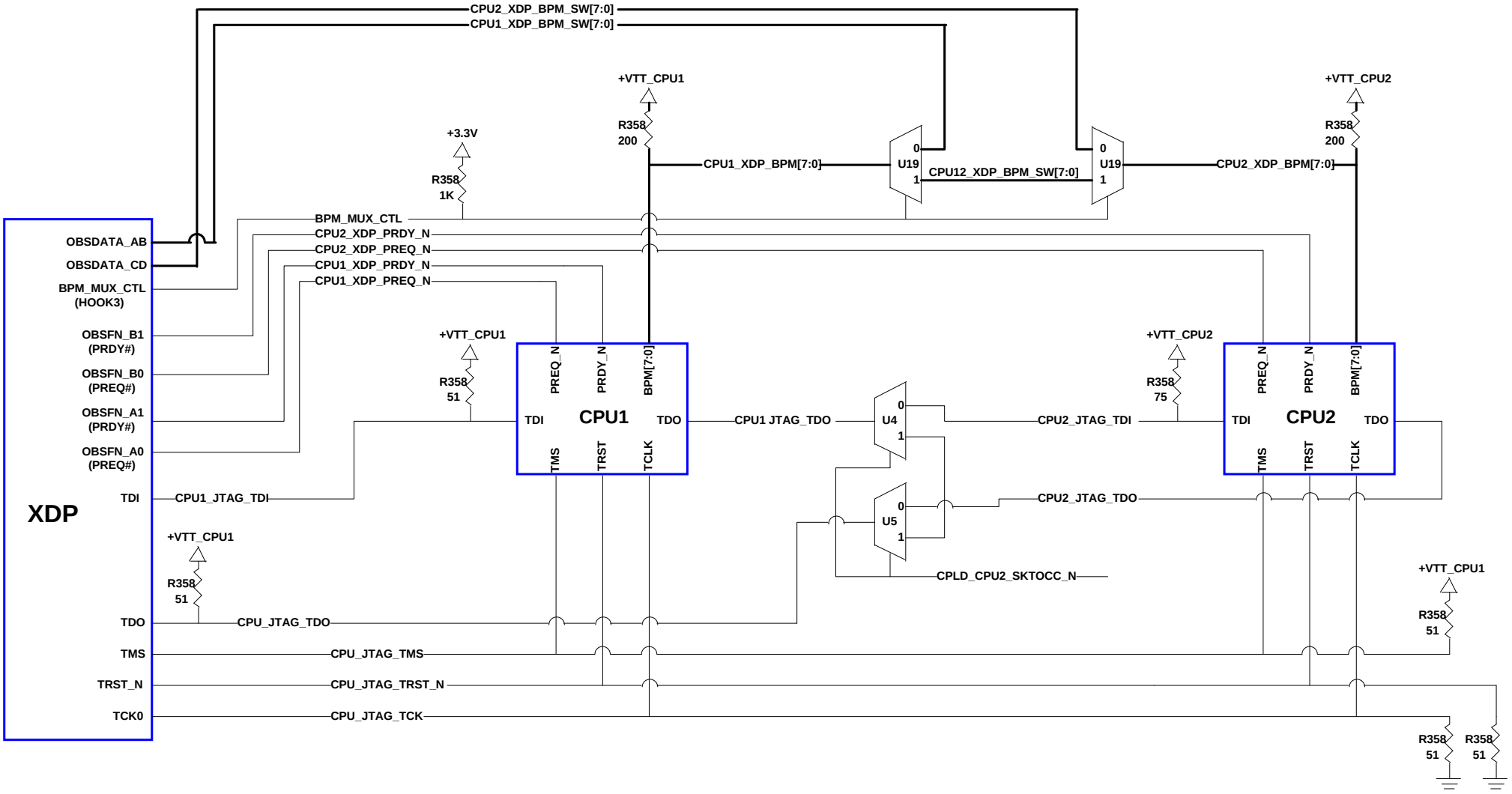
DELL INC.

Title
SCHEM, PWA, VC-TEST, BIG, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 6 of 96



Debug Port Design Guide 0.95 Routing Guidelines:

- TCK/TMS max trace length = 1.5ns
- PREQ#/PRDY# max trace length = 1.5ns
- BPM max trace length between MUX and CPU =10"
- BPM max trace length between MUXes = 8ns
- All BPM net lengths should match as a group to within +/-50ps
- All BPM nets must have 200ohm VTT terminations near CPU

Default settings:

- CPU1 always in scan chain
- CPU2 in scan chain if present, bypassed if not present
- PCH in separate scan chain

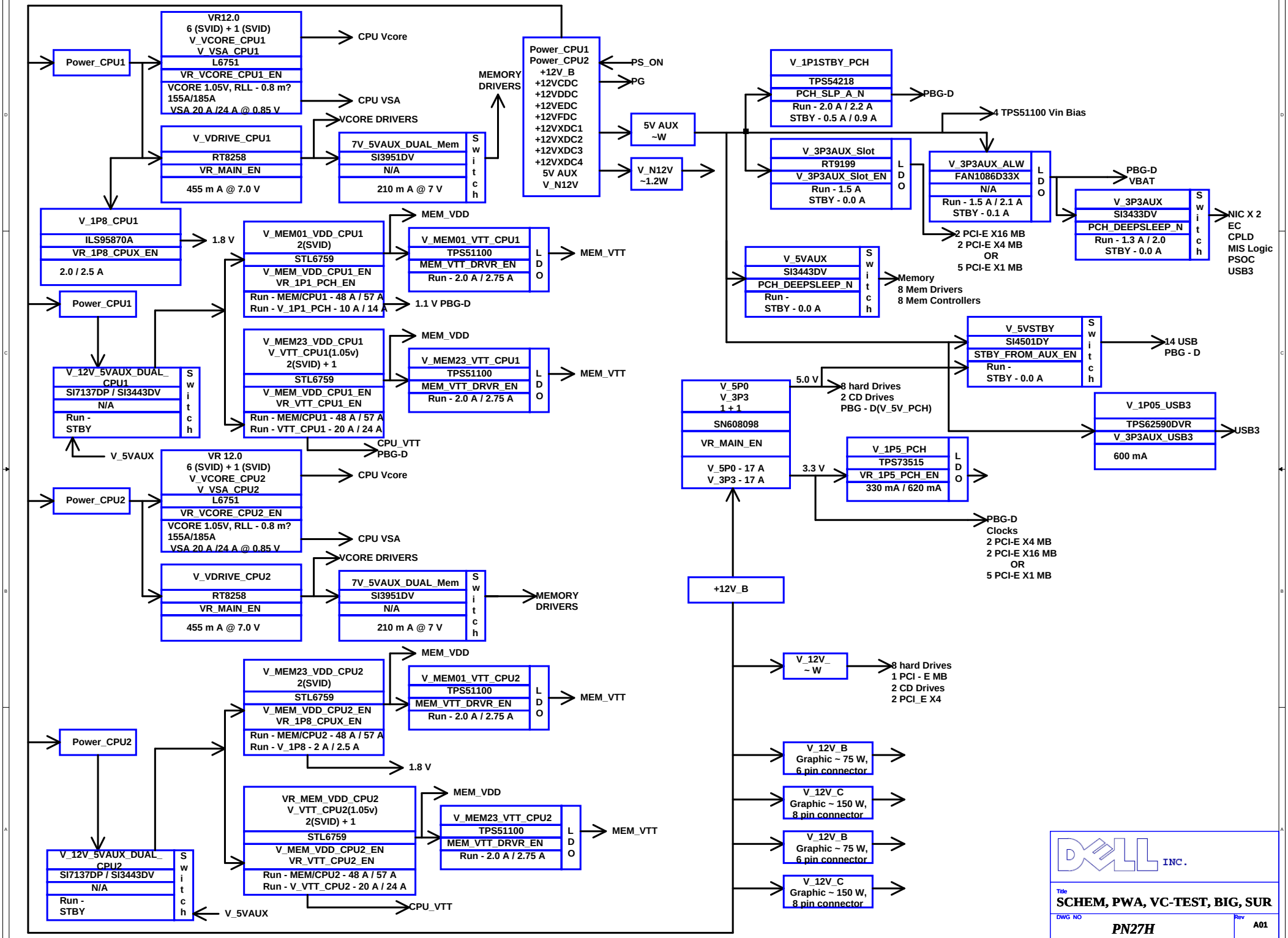
DELL INC.

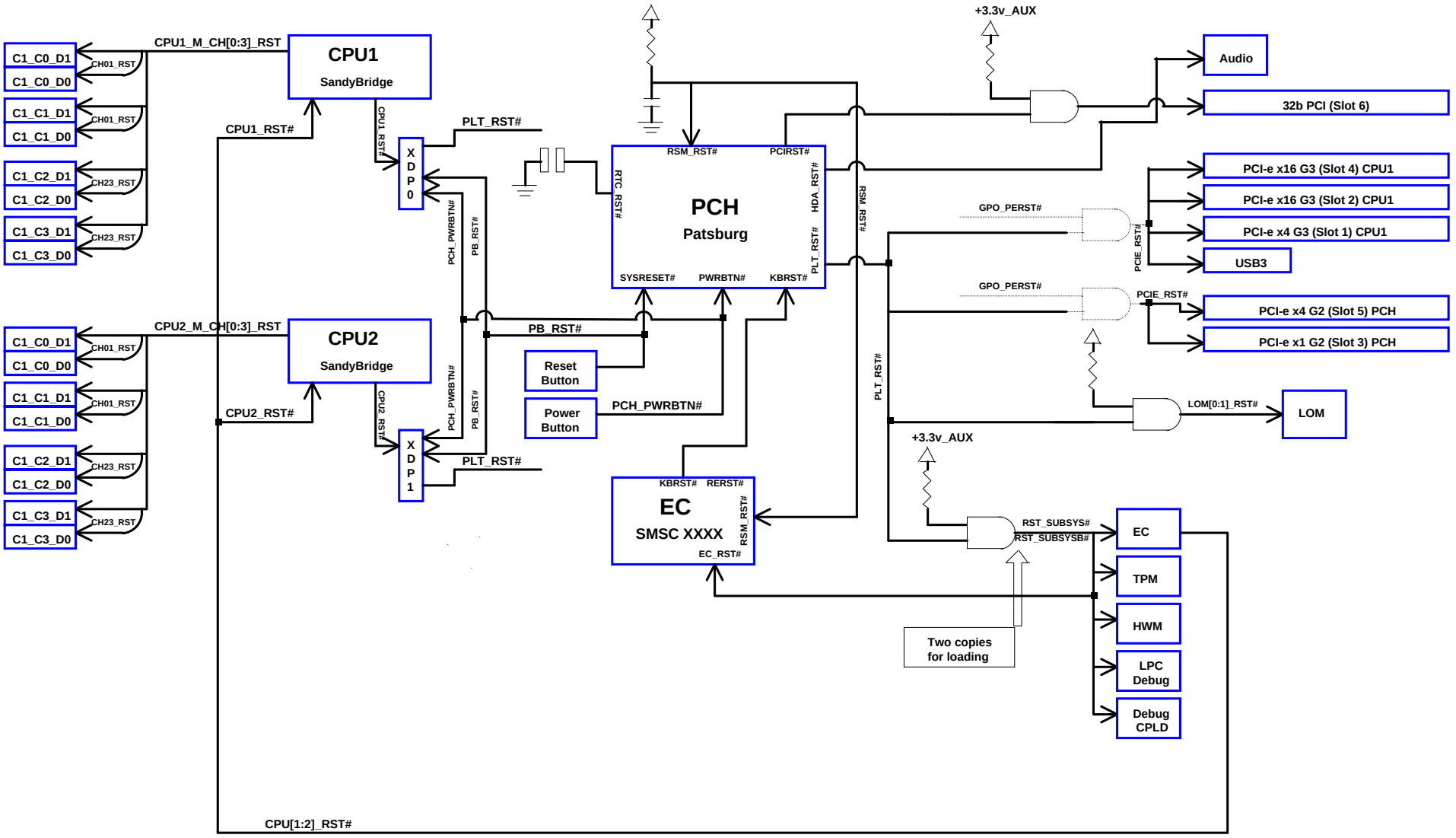
Title: SCHEM, PWA, VC-TEST, BIG, SUR

DWG NO: PN27H

Rev: A01

Date: Wednesday, June 20, 2012 Sheet 7 of 96


Power_CPU1
VR12.0
6 (SVID) + 1 (SVID)
V_VCORE_CPU1
V_VSA_CPU1
L6751
VR_VCORE_CPU1_EN
VCORE 1.05V, RLL - 0.8 m?
155A/185A
VSA 20 A /24 A @ 0.85 V
CPU Vcore
CPU VSA
VCORE DRIVERS
V_VDRIVE_CPU1
RT8258
VR_MAIN_EN
455 m A @ 7.0 V
7V_5VAUX_DUAL_Mem
SI3951DV
N/A
210 m A @ 7 V
Switch
MEMORY DRIVERS
Power_CPU1
Power_CPU2
+12V_B
+12VCDC
+12VDDC
+12VEDC
+12VFDC
+12VXDC1
+12VXDC2
+12VXDC3
+12VXDC4
5V AUX
V_N12V
PS_ON
PG
5V AUX ~W
V_N12V ~1.2W
V_1P8_CPU1
ILS95870A
VR_1P8_CPUX_EN
2.0 / 2.5 A
1.8 V
V_MEM01_VDD_CPU1
2(SVID)
STL6759
V_MEM_VDD_CPU1_EN
VR_1P1_PCH_EN
Run - MEM/CPU1 - 48 A / 57 A
Run - V_1P1_PCH - 10 A / 14 A
MEM_VDD
1.1 V PBG-D
V_MEM01_VTT_CPU1
TPS51100
MEM_VTT_DRVR_EN
Run - 2.0 A / 2.75 A
LDO
MEM_VTT
V_MEM23_VDD_CPU1
V_VTT_CPU1(1.05v)
2(SVID) + 1
STL6759
V_MEM_VDD_CPU1_EN
VR_VTT_CPU1_EN
Run - MEM/CPU1 - 48 A / 57 A
Run - VTT_CPU1 - 20 A / 24 A
MEM_VDD
V_MEM23_VTT_CPU1
TPS51100
MEM_VTT_DRVR_EN
Run - 2.0 A / 2.75 A
LDO
MEM_VTT
CPU_VTT
PBG-D
V_12V_5VAUX_DUAL_CPU1
SI7137DP / SI3443DV
N/A
Run - STBY
Switch
V_5VAUX
Power_CPU2
VR 12.0
6 (SVID) + 1 (SVID)
V_VCORE_CPU2
V_VSA_CPU2
L6751
VR_VCORE_CPU2_EN
VCORE 1.05V, RLL - 0.8 m?
155A/185A
VSA 20 A /24 A @ 0.85 V
CPU Vcore
CPU VSA
VCORE DRIVERS
V_VDRIVE_CPU2
RT8258
VR_MAIN_EN
455 m A @ 7.0 V
7V_5VAUX_DUAL_Mem
SI3951DV
N/A
210 m A @ 7 V
Switch
MEMORY DRIVERS
V_MEM23_VDD_CPU2
2(SVID)
STL6759
V_MEM_VDD_CPU2_EN
VR_1P8_CPUX_EN
Run - MEM/CPU2 - 48 A / 57 A
Run - V_1P8 - 2 A / 2.5 A
MEM_VDD
V_MEM01_VTT_CPU2
TPS51100
MEM_VTT_DRVR_EN
Run - 2.0 A / 2.75 A
LDO
MEM_VTT
1.8 V
VR_MEM_VDD_CPU2
V_VTT_CPU2(1.05v)
2(SVID) + 1
STL6759
V_MEM_VDD_CPU2_EN
VR_VTT_CPU2_EN
Run - MEM/CPU2 - 48 A / 57 A
Run - V_VTT_CPU2 - 20 A / 24 A
MEM_VDD
V_MEM23_VTT_CPU2
TPS51100
MEM_VTT_DRVR_EN
Run - 2.0 A / 2.75 A
LDO
MEM_VTT
CPU_VTT
V_12V_5VAUX_DUAL_CPU2
SI7137DP / SI3443DV
N/A
Run - STBY
Switch
V_5VAUX
V_1P1STBY_PCH
TPS54218
PCH_SLP_A_N
Run - 2.0 A / 2.2 A
STBY - 0.5 A / 0.9 A
PBG-D
4 TPS51100 Vin Bias
V_3P3AUX_Slot
RT9199
V_3P3AUX_Slot_EN
Run - 1.5 A
STBY - 0.0 A
LDO
V_3P3AUX_ALW
FAN1086D33X
N/A
Run - 1.5 A / 2.1 A
STBY - 0.1 A
LDO
PBG-D
VBAT
2 PCI-E X16 MB
2 PCI-E X4 MB
OR
5 PCI-E X1 MB
V_3P3AUX
SI3433DV
PCH_DEEPSLEEP_N
Run - 1.3 A / 2.0
STBY - 0.0 A
Switch
NIC X 2
EC
CPLD
MIS Logic
PSOC
USB3
V_5VAUX
SI3443DV
PCH_DEEPSLEEP_N
Run -
STBY - 0.0 A
Switch
Memory
8 Mem Drivers
8 Mem Controllers
V_5VSTBY
SI4501DY
STBY_FROM_AUX_EN
Run -
STBY - 0.0 A
Switch
14 USB
PBG - D
V_5P0
V_3P3
1 + 1
SN608098
VR_MAIN_EN
V_5P0 - 17 A
V_3P3 - 17 A
5.0 V
8 hard Drives
2 CD Drives
PBG - D(V_5V_PCH)
3.3 V
V_1P5_PCH
TPS73515
VR_1P5_PCH_EN
330 mA / 620 mA
LDO
PBG-D
Clocks
2 PCI-E X4 MB
2 PCI-E X16 MB
OR
5 PCI-E X1 MB
V_1P05_USB3
TPS62590DVR
V_3P3AUX_USB3
600 mA
USB3
+12V_B
V_12V_ ~ W
8 hard Drives
1 PCI - E MB
2 CD Drives
2 PCI_E X4
V_12V_B
Graphic ~ 75 W,
6 pin connector
V_12V_C
Graphic ~ 150 W,
8 pin connector
V_12V_B
Graphic ~ 75 W,
6 pin connector
V_12V_C
Graphic ~ 150 W,
8 pin connector
DELL INC.
Title
SCHEM, PWA, VC-TEST, BIG, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 8 of 96



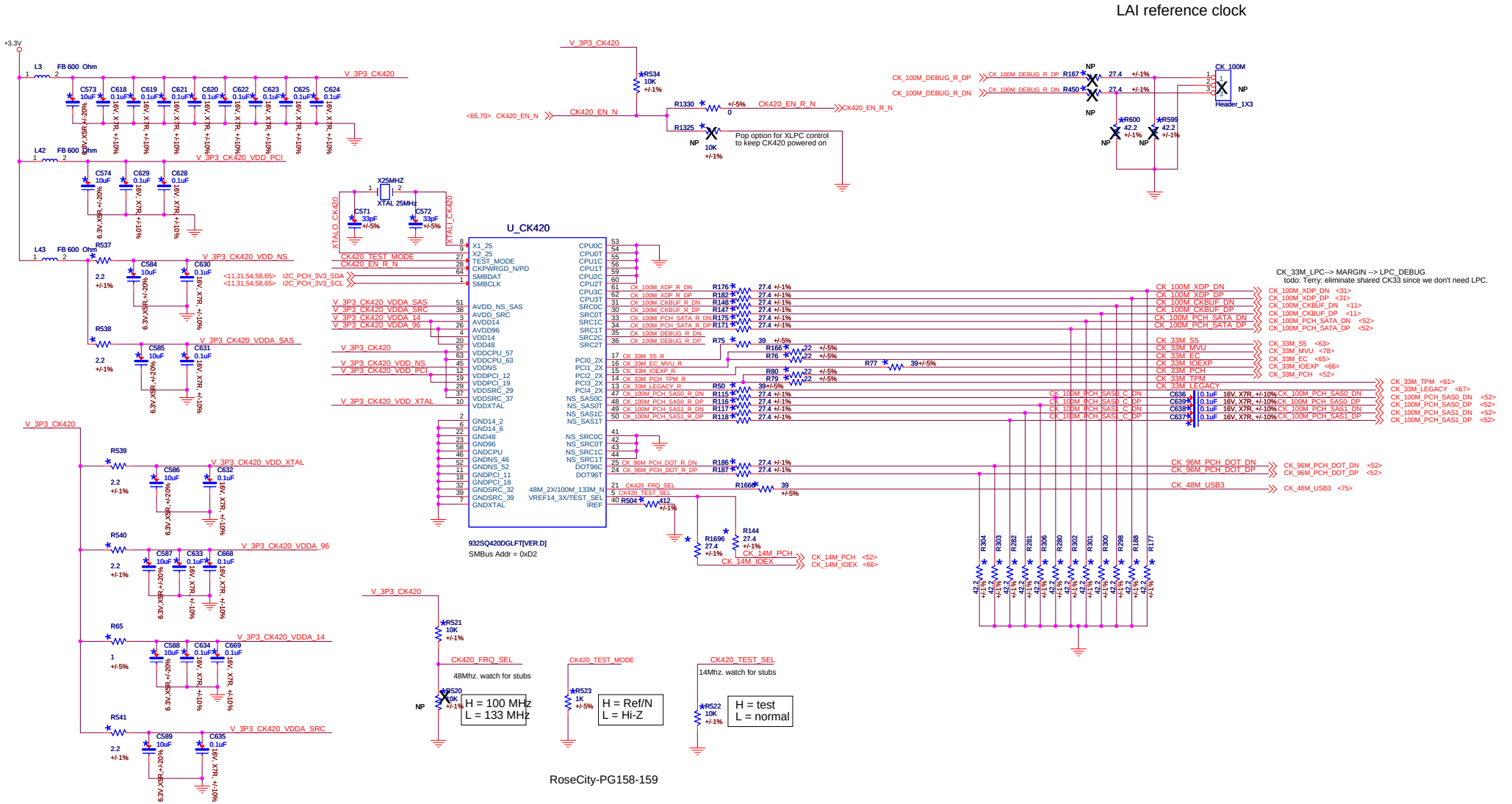
DELL INC.

Title
SCHEM, PWA, VC-TEST, BIG, SUR

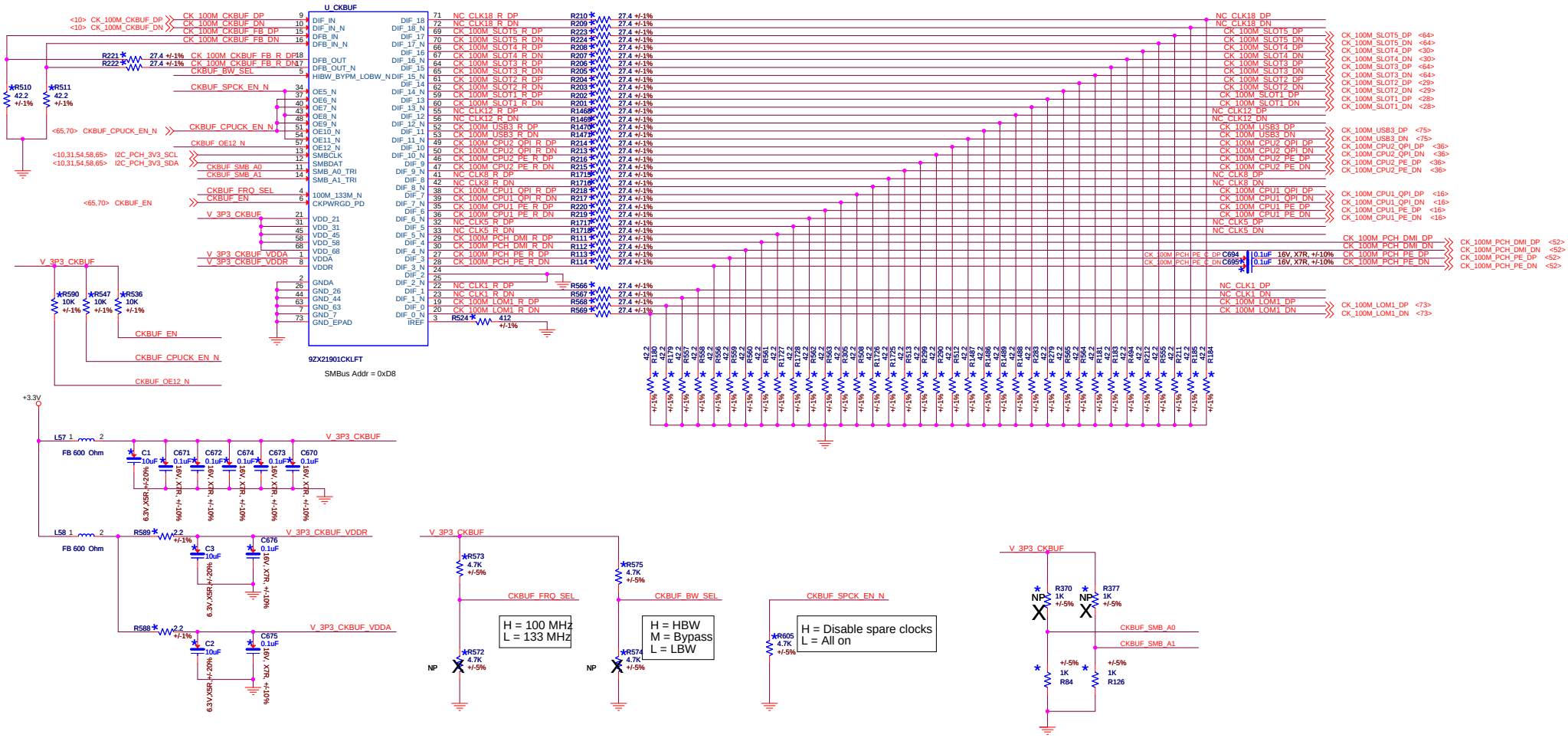
DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 9 of 96



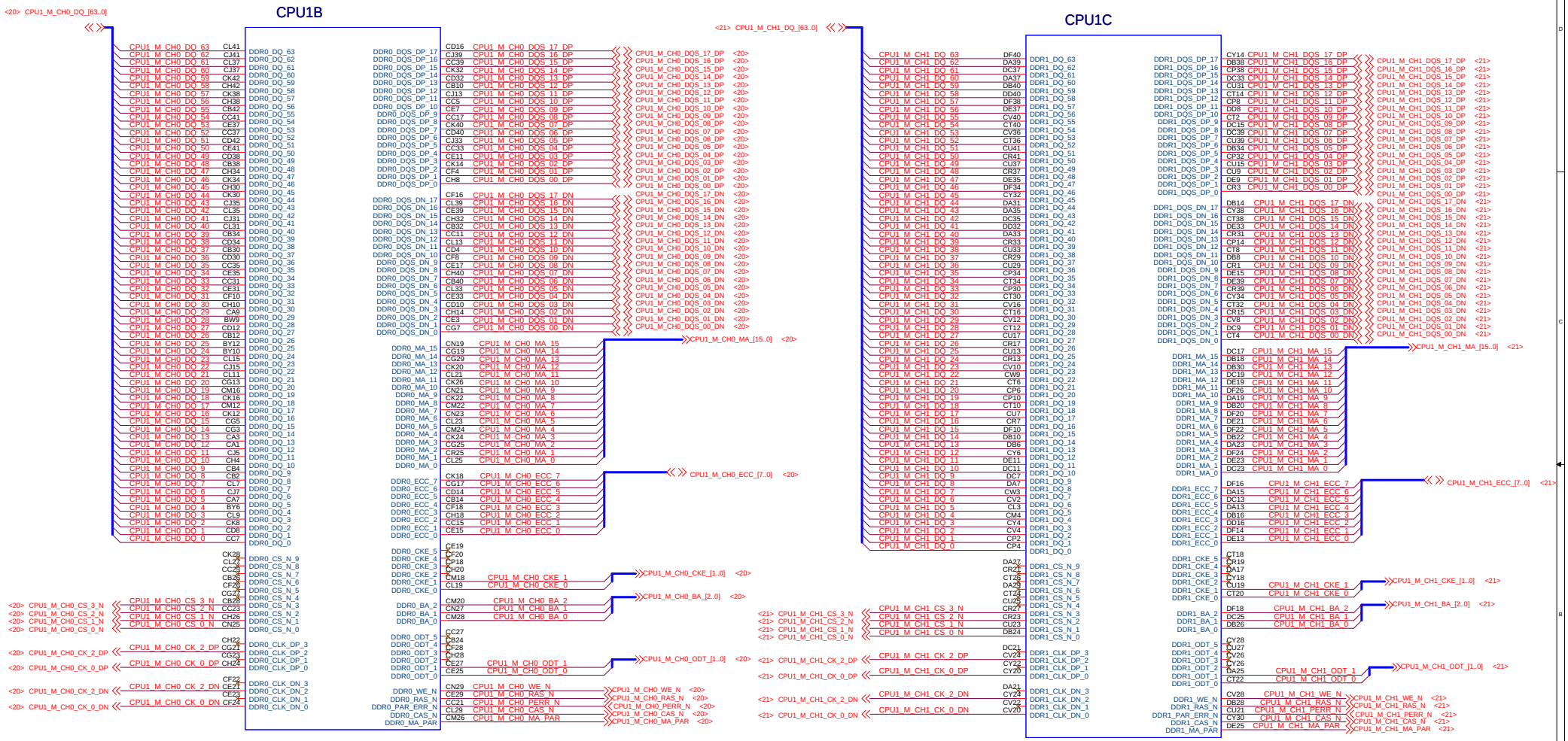
Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	10 of 96



Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	11 of 96

DDR_CH0

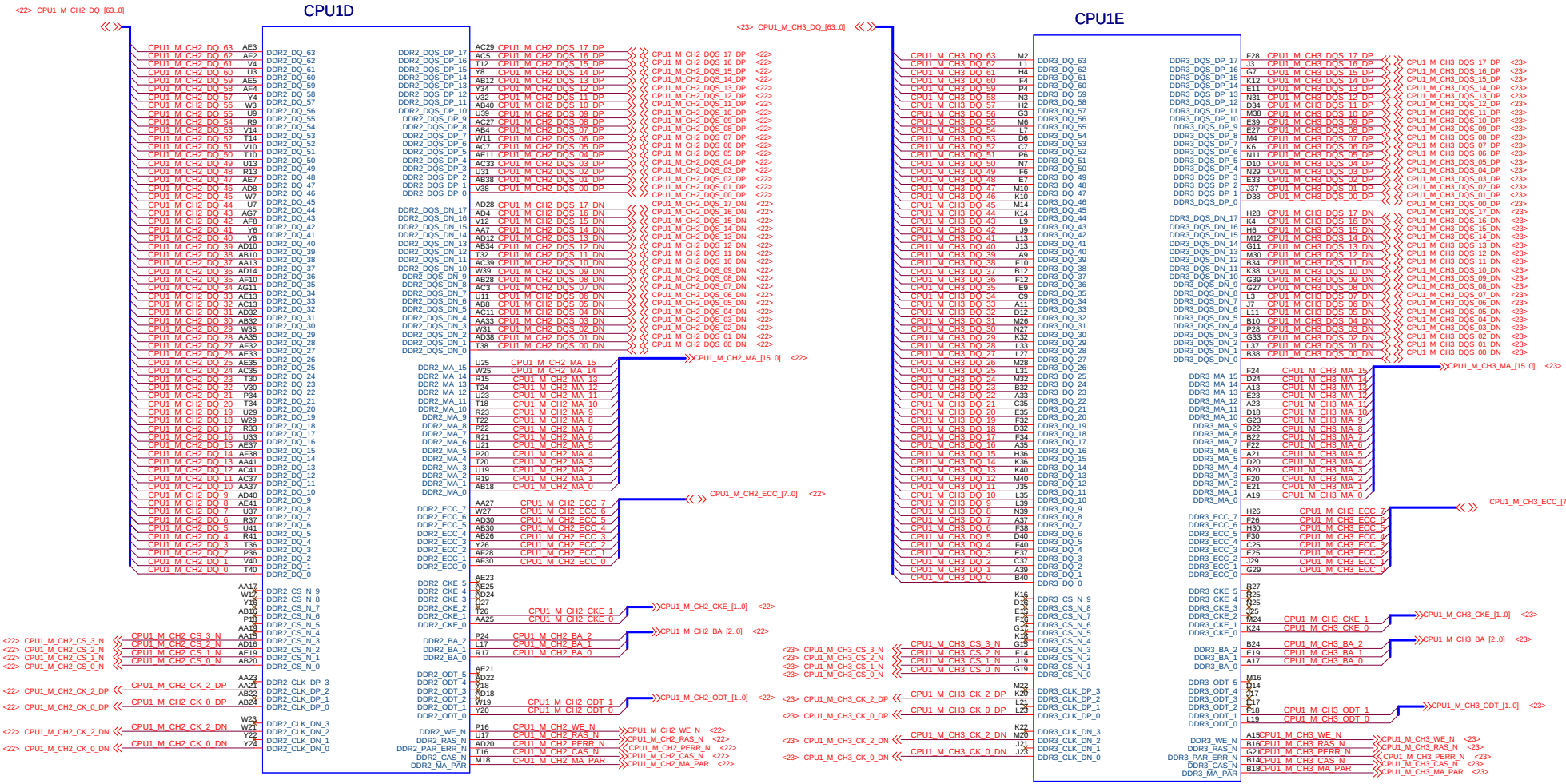
DDR_CH1



Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	12 of 96

DDR_CH2

DDR_CH3



Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	13 of 96

SandyBridge_EPEX_EDS_Vol1_26601,0.5.pvd Figure 1-3 pg.16

Port0	Port1	Port2	Port3
DMI	PE1[A:B]	PE2[A:B:C:D]	PE3[A:B:C:D]
IOU2---IOU2		IOU0	IOU1
DMI to PCH	X4 slot X4 to PCH	X16 slot	X16 slot

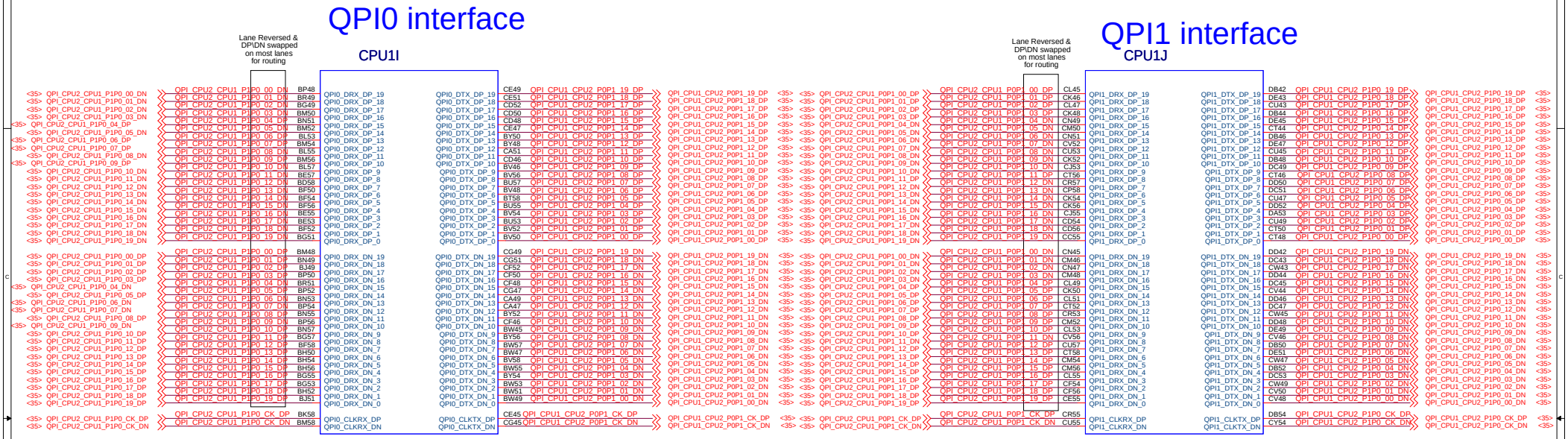
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

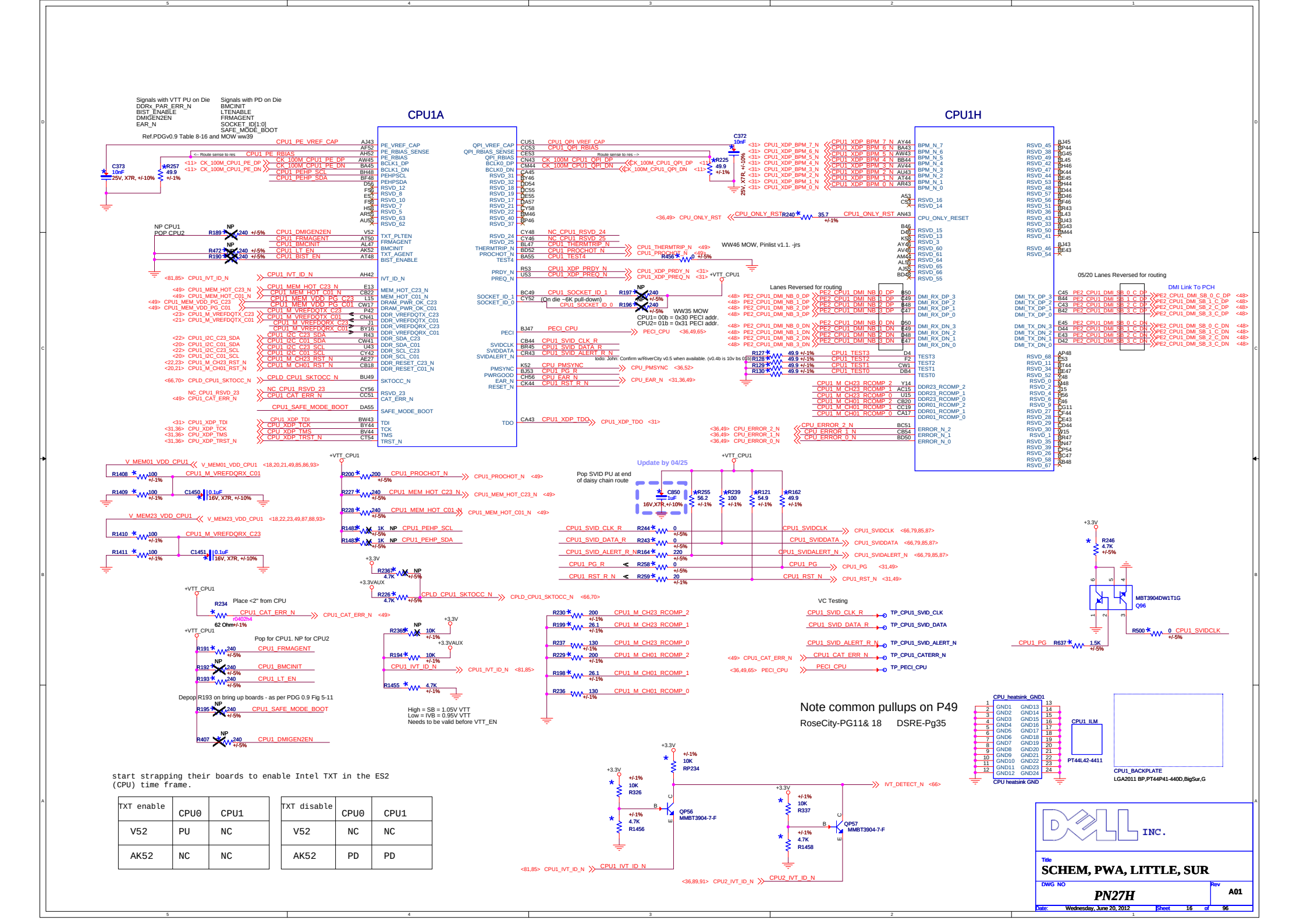
DWG NO
PN27H

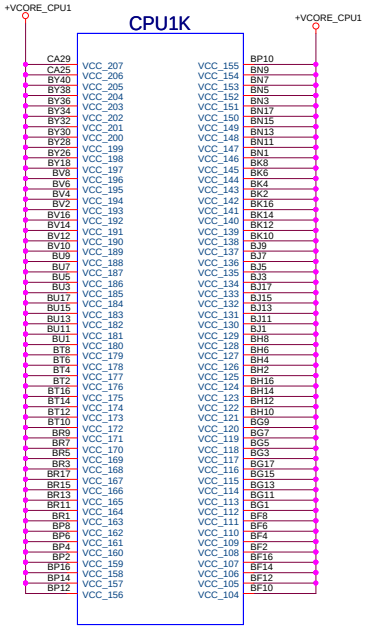
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 14 of 96

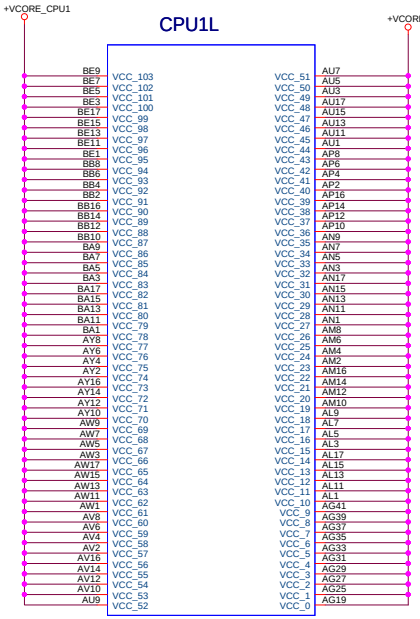


Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	15 of 96


CPU1A
CPU1H
Signals with VTT PU on Die
DDRx_PAR_ERR_N
BIST_ENABLE
DMIGEN2EN
EAR_N
Signals with PD on Die
BMCINIT
LTENABLE
FRMAGENT
SOCKET_ID[1:0]
SAFE_MODE_BOOT
Ref.PDGv0.9 Table 8-16 and MOW ww39
WW46 MOW, Pinlist v1.1. -jrs
WW35 MOW
CPU1= 00b = 0x30 PECI addr.
CPU2= 01b = 0x31 PECI addr.
Lanes Reversed for routing
05/20 Lanes Reversed for routing
DMI Link To PCH
Update by 04/25
Pop SVID PU at end of daisy chain route
VC Testing
Note common pullups on P49
RoseCity-PG11& 18 DSRE-Pg35
Pop for CPU1. NP for CPU2
Depop R193 on bring up boards - as per PDG 0.9 Fig 5-11
High = SB = 1.05V VTT
Low = IVB = 0.95V VTT
Needs to be valid before VTT_EN
start strapping their boards to enable Intel TXT in the ES2 (CPU) time frame.
TXT enable | CPU0 | CPU1
V52 | PU | NC
AK52 | NC | NC
TXT disable | CPU0 | CPU1
V52 | NC | NC
AK52 | PD | PD
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 16 of 96

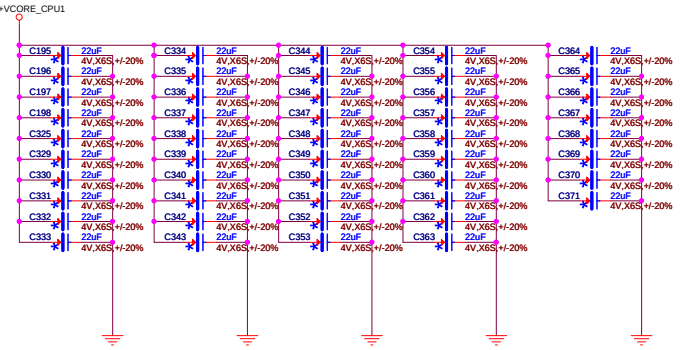


RoseCity-PG31



RoseCity-PG31

Hight Temp X6S Caps. Place in CPU cavity



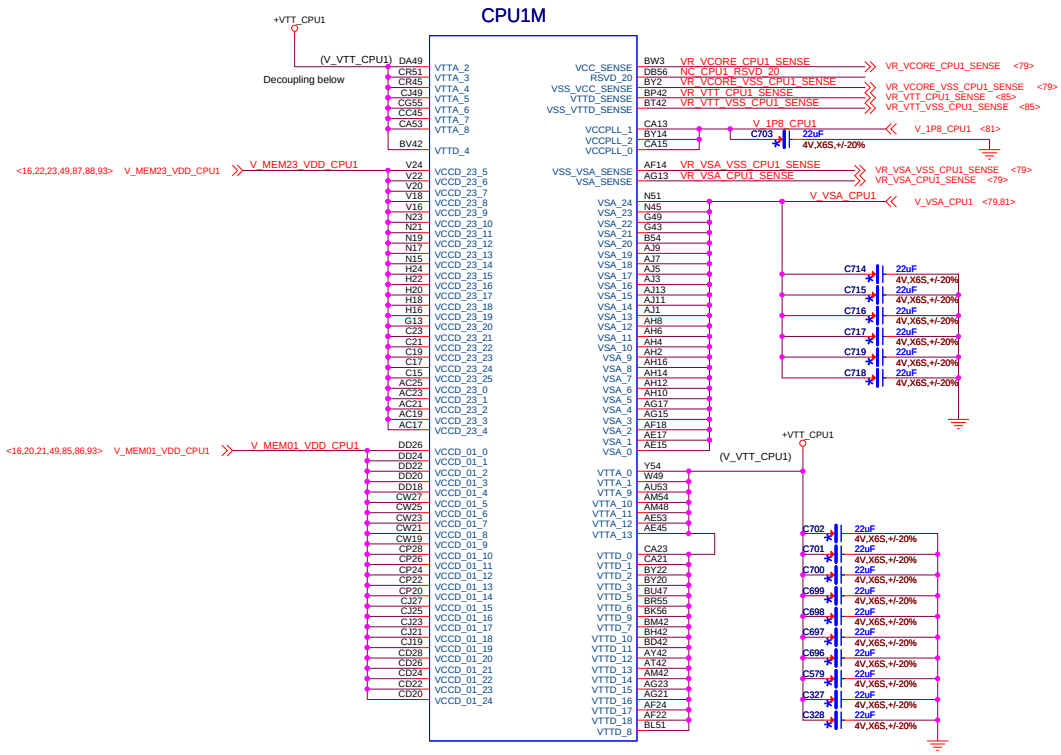
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 17 of 96



RoseCity-PG32

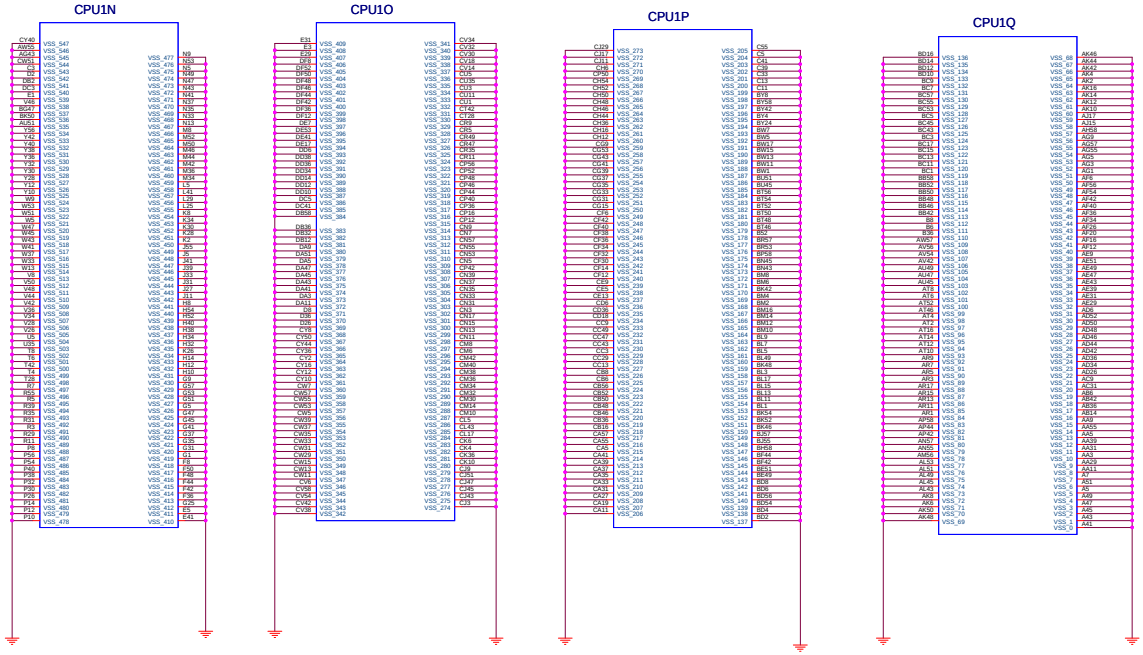
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

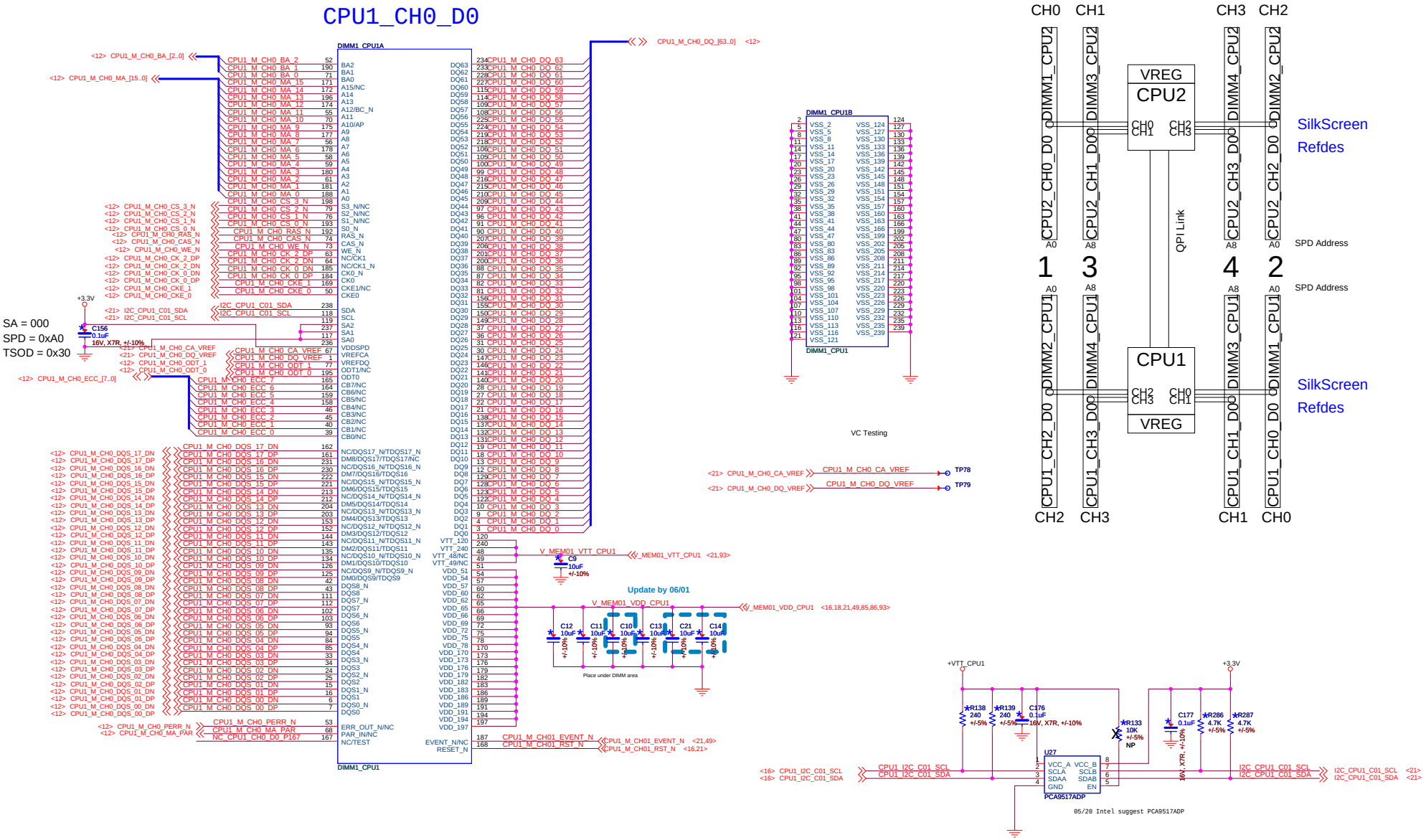
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 18 of 96



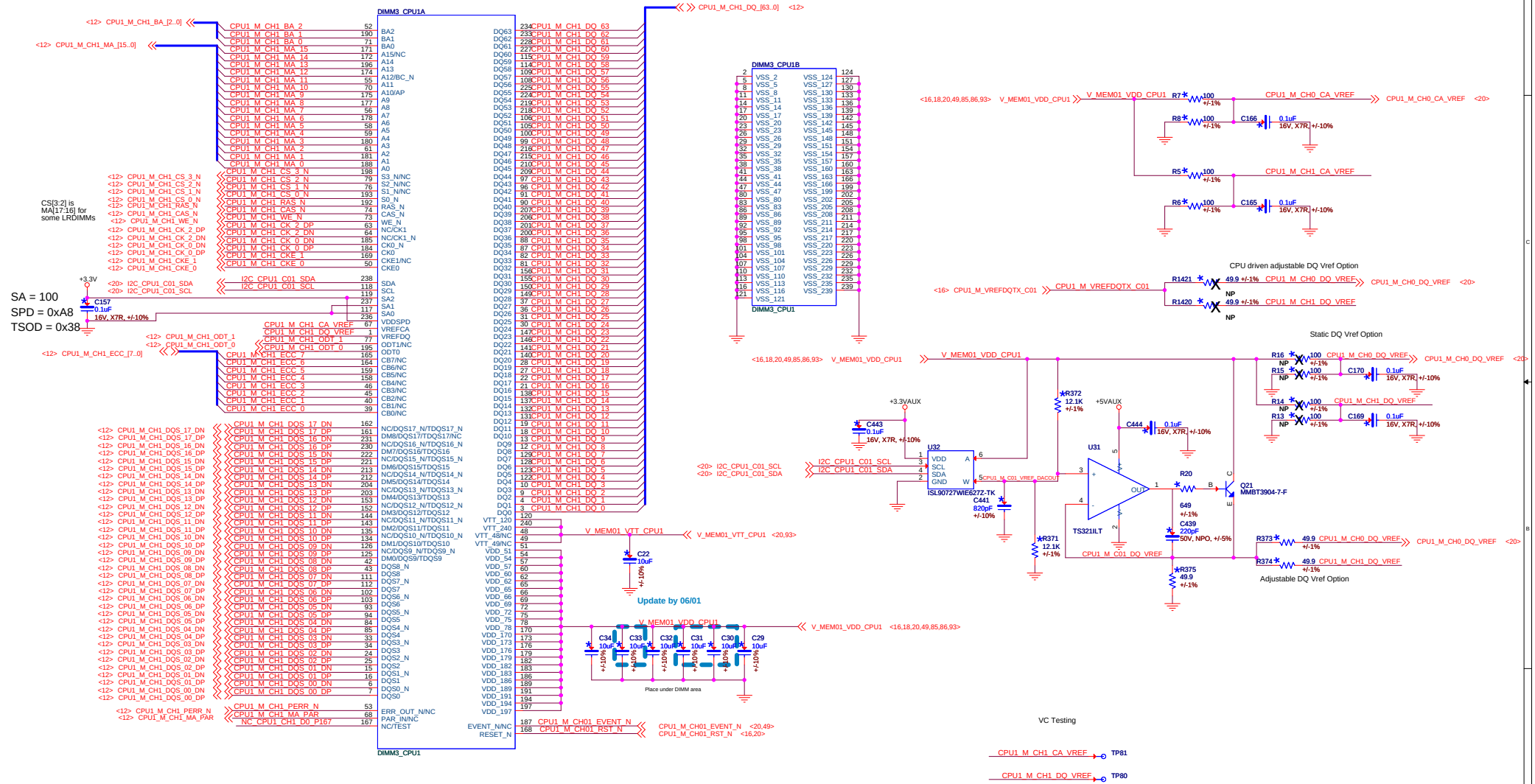
Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date	Wednesday, June 20, 2012
Sheet	19 of 96

CPU1_CH0_D0



Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	20 of 96

CPU1_CH1_D0



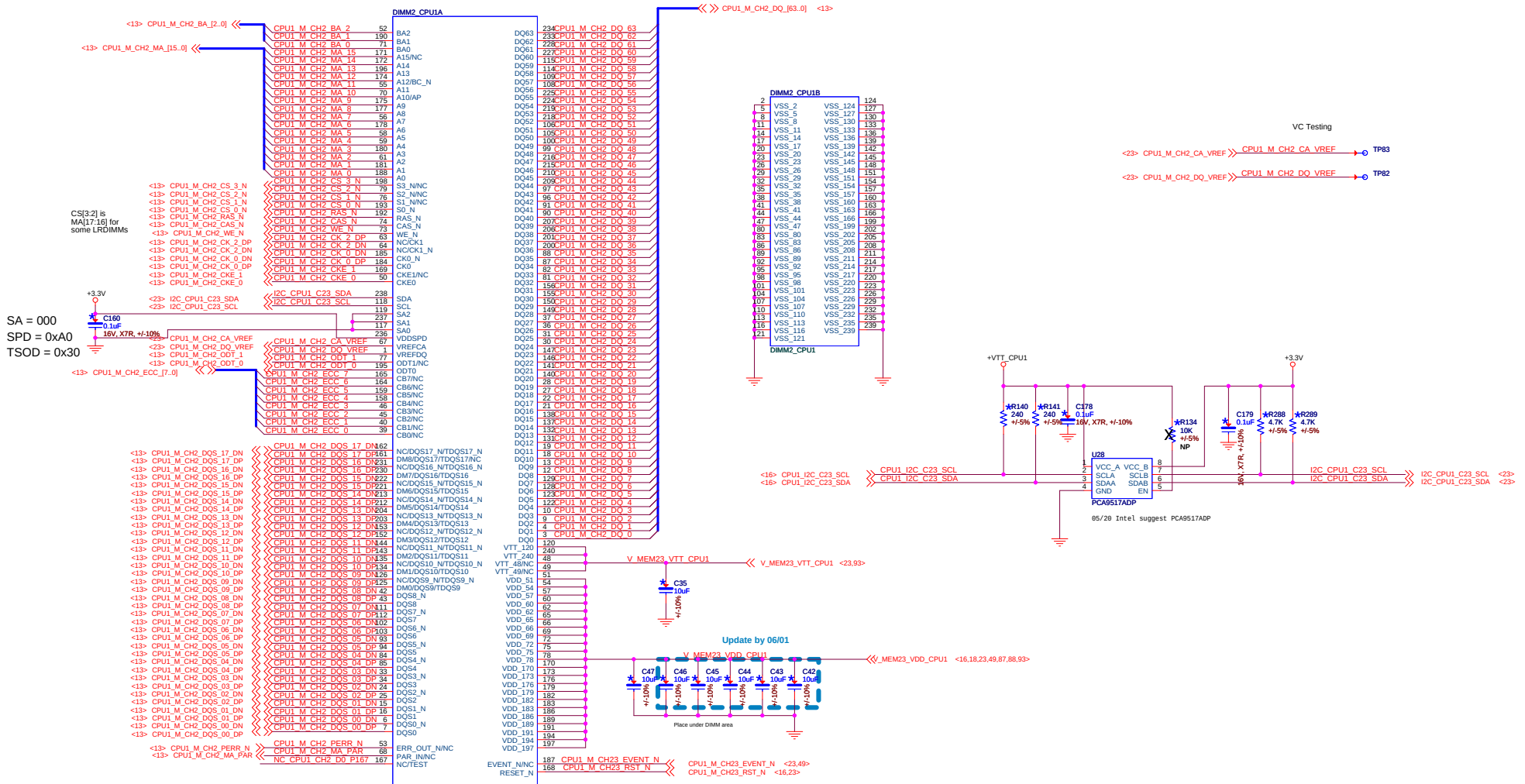
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

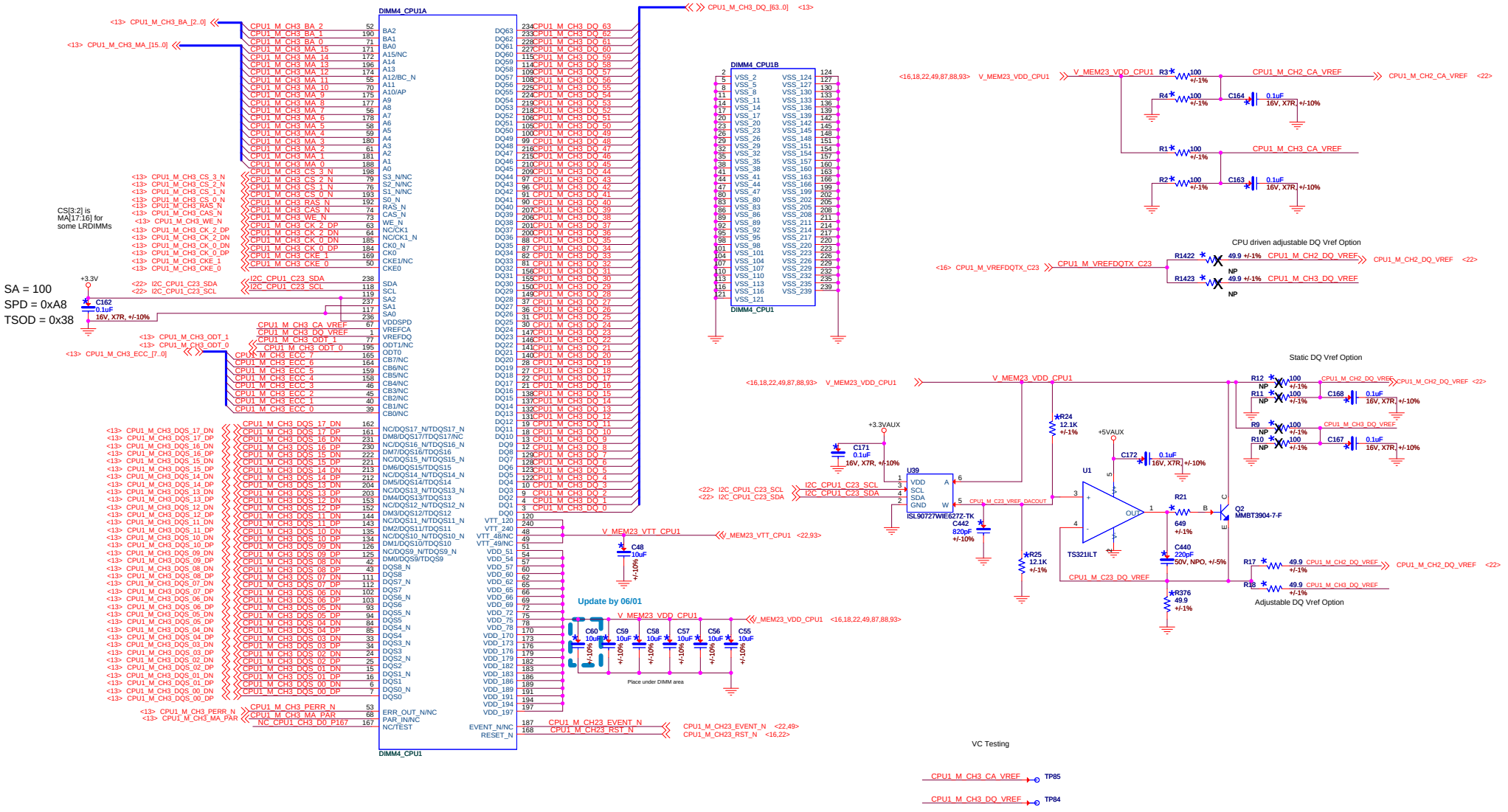
Date: Wednesday, June 20, 2012 Sheet 21 of 96

CPU1_CH2_D0

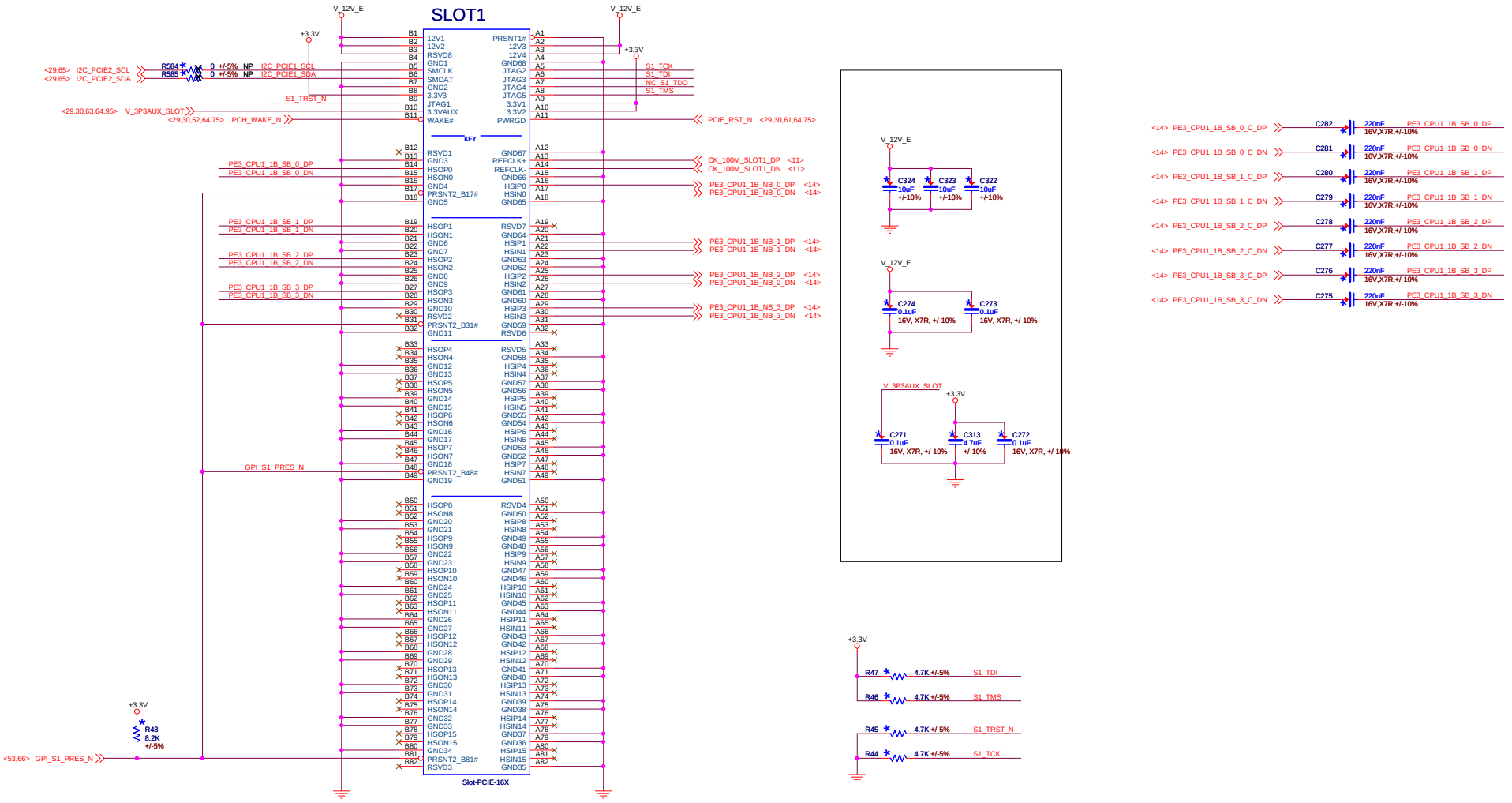


Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	22 of 96

CPU1_CH3_D0



Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	23 of 96



DELL INC.

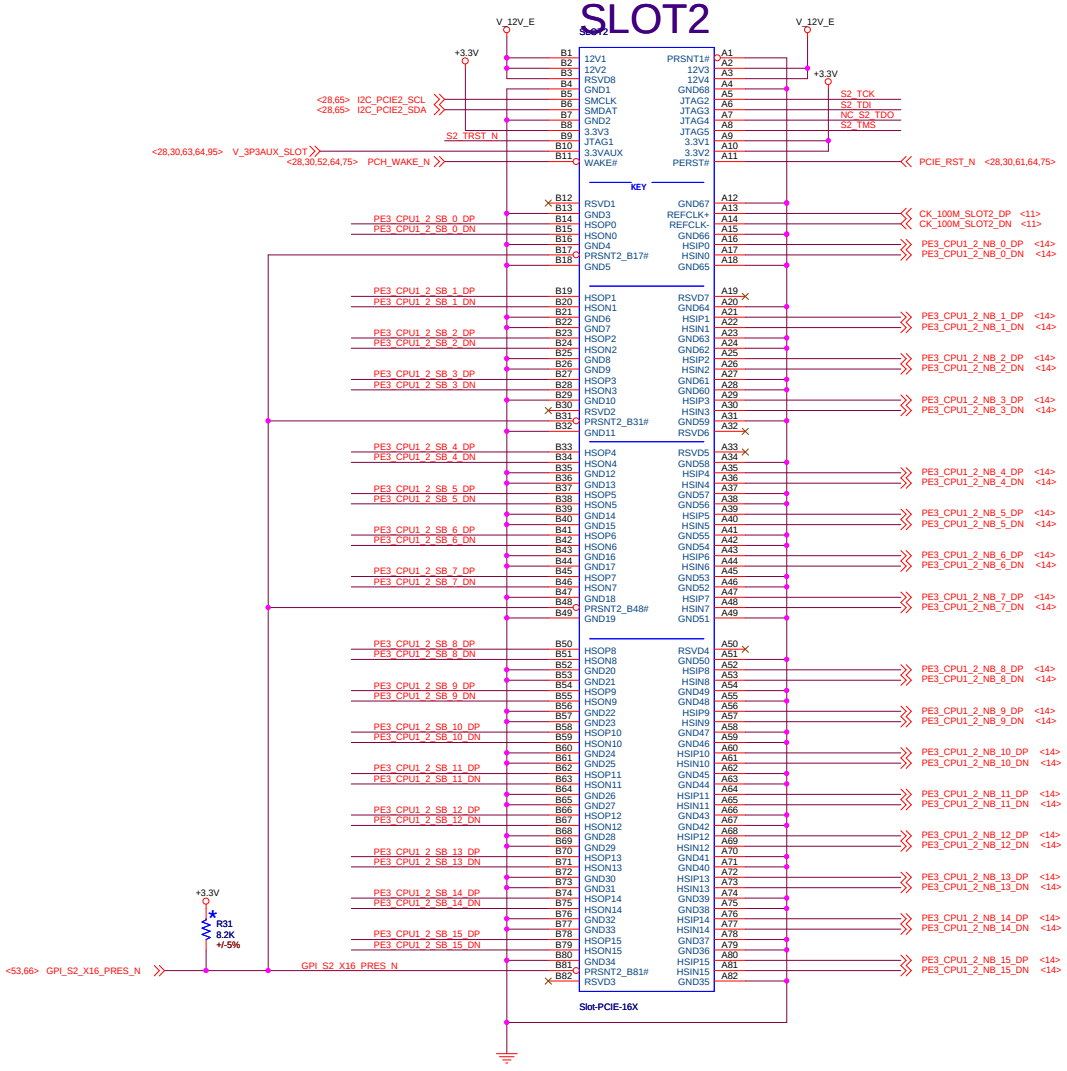
Title
SCHEM, PWA, LITTLE, SUR

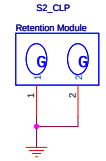
DWG NO
PN27H

Rev
A01

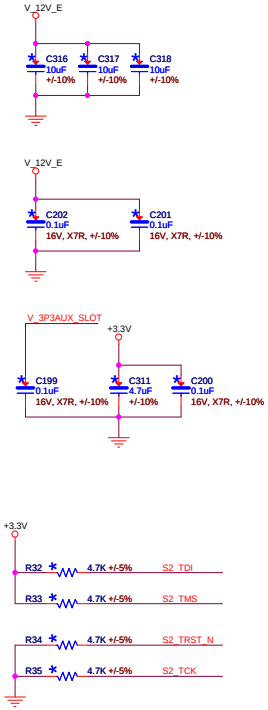
Date: Wednesday, June 20, 2012 Sheet 28 of 96

SLOT2





PCI-E x16 slot decoupling



NOTE: PCIE naming convention is:
EXP_[UpstreamDevice]_[Port]_[NV|SB]_[LANE]_[C]_[DP|DN]

Placed by SLOT

<14> PE3_CPU1_2_SB_0_C_DP	C203	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_0_DP
<14> PE3_CPU1_2_SB_0_C_DN	C204	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_0_DN
<14> PE3_CPU1_2_SB_1_C_DP	C205	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_1_DP
<14> PE3_CPU1_2_SB_1_C_DN	C206	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_1_DN
<14> PE3_CPU1_2_SB_2_C_DP	C207	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_2_DP
<14> PE3_CPU1_2_SB_2_C_DN	C208	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_2_DN
<14> PE3_CPU1_2_SB_3_C_DP	C209	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_3_DP
<14> PE3_CPU1_2_SB_3_C_DN	C210	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_3_DN
<14> PE3_CPU1_2_SB_4_C_DP	C211	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_4_DP
<14> PE3_CPU1_2_SB_4_C_DN	C212	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_4_DN
<14> PE3_CPU1_2_SB_5_C_DP	C213	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_5_DP
<14> PE3_CPU1_2_SB_5_C_DN	C214	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_5_DN
<14> PE3_CPU1_2_SB_6_C_DP	C215	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_6_DP
<14> PE3_CPU1_2_SB_6_C_DN	C216	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_6_DN
<14> PE3_CPU1_2_SB_7_C_DP	C217	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_7_DP
<14> PE3_CPU1_2_SB_7_C_DN	C218	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_7_DN
<14> PE3_CPU1_2_SB_8_C_DP	C219	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_8_DP
<14> PE3_CPU1_2_SB_8_C_DN	C220	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_8_DN
<14> PE3_CPU1_2_SB_9_C_DP	C221	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_9_DP
<14> PE3_CPU1_2_SB_9_C_DN	C222	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_9_DN
<14> PE3_CPU1_2_SB_10_C_DP	C223	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_10_DP
<14> PE3_CPU1_2_SB_10_C_DN	C224	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_10_DN
<14> PE3_CPU1_2_SB_11_C_DP	C225	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_11_DP
<14> PE3_CPU1_2_SB_11_C_DN	C226	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_11_DN
<14> PE3_CPU1_2_SB_12_C_DP	C227	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_12_DP
<14> PE3_CPU1_2_SB_12_C_DN	C228	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_12_DN
<14> PE3_CPU1_2_SB_13_C_DP	C229	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_13_DP
<14> PE3_CPU1_2_SB_13_C_DN	C230	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_13_DN
<14> PE3_CPU1_2_SB_14_C_DP	C231	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_14_DP
<14> PE3_CPU1_2_SB_14_C_DN	C232	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_14_DN
<14> PE3_CPU1_2_SB_15_C_DP	C233	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_15_DP
<14> PE3_CPU1_2_SB_15_C_DN	C234	220nF 16V,X7R,+/-10%	PE3_CPU1_2_SB_15_DN

DELL INC.

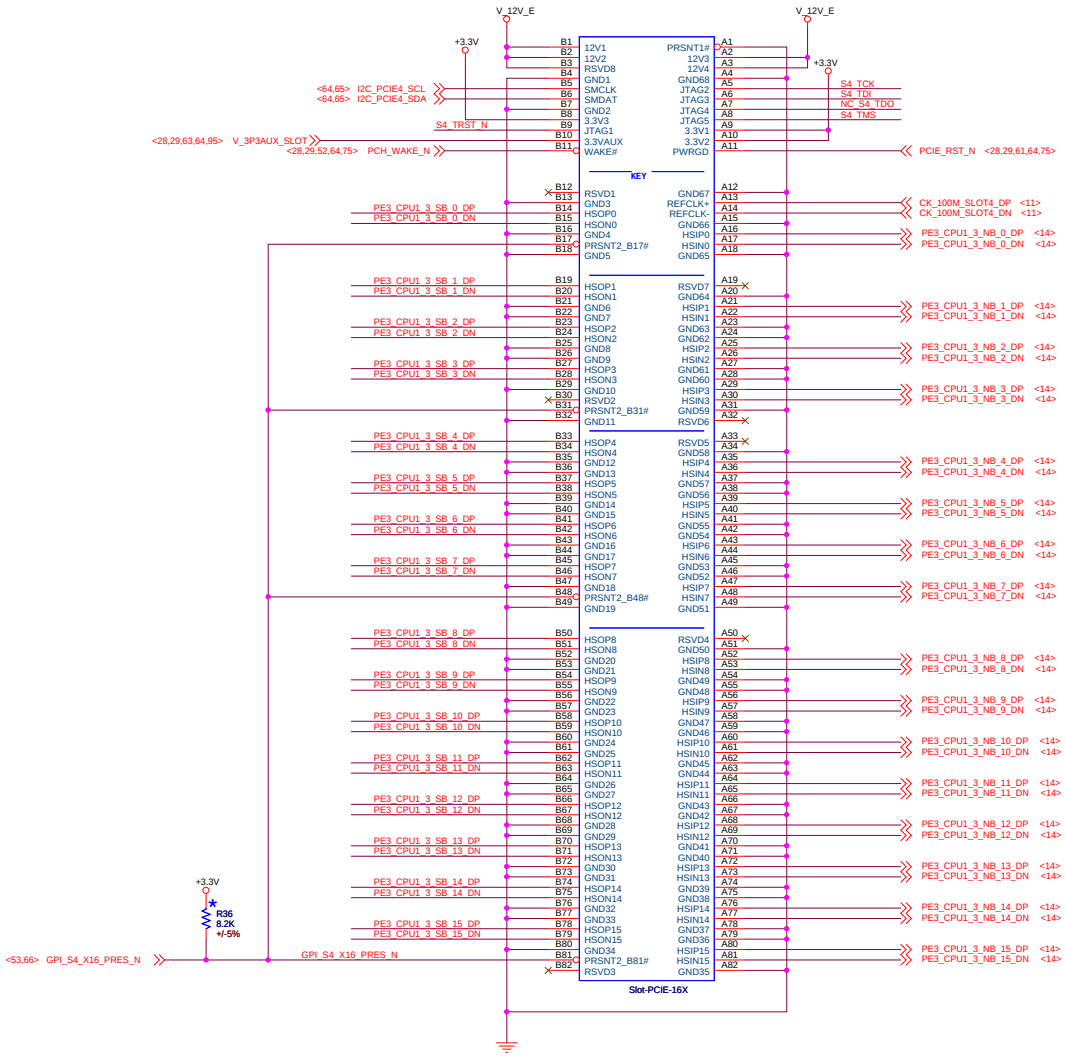
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 29 of 96

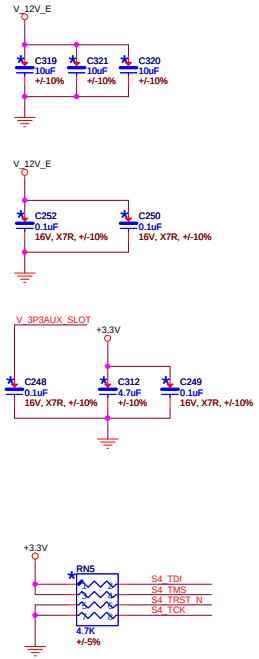
SLOT4



S4_CLP

Retention Module

PCI-E x16 slot decoupling



NOTE: PCIE naming convention is:
EXP_[UpstreamDevice]_[Port]_[NV|SB]_[LANE]_[C]_[DP|DN]

Placed by SLOT

<14> PE3_CPU1_3_SB_0_C_DP	C253	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_0_DP
<14> PE3_CPU1_3_SB_0_C_DN	C264	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_0_DN
<14> PE3_CPU1_3_SB_1_C_DP	C263	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_1_DP
<14> PE3_CPU1_3_SB_1_C_DN	C262	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_1_DN
<14> PE3_CPU1_3_SB_2_C_DP	C261	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_2_DP
<14> PE3_CPU1_3_SB_2_C_DN	C259	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_2_DN
<14> PE3_CPU1_3_SB_3_C_DP	C258	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_3_DP
<14> PE3_CPU1_3_SB_3_C_DN	C257	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_3_DN
<14> PE3_CPU1_3_SB_4_C_DP	C256	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_4_DP
<14> PE3_CPU1_3_SB_4_C_DN	C255	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_4_DN
<14> PE3_CPU1_3_SB_5_C_DP	C254	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_5_DP
<14> PE3_CPU1_3_SB_5_C_DN	C251	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_5_DN
<14> PE3_CPU1_3_SB_6_C_DP	C247	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_6_DP
<14> PE3_CPU1_3_SB_6_C_DN	C246	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_6_DN
<14> PE3_CPU1_3_SB_7_C_DP	C245	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_7_DP
<14> PE3_CPU1_3_SB_7_C_DN	C244	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_7_DN
<14> PE3_CPU1_3_SB_8_C_DP	C243	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_8_DP
<14> PE3_CPU1_3_SB_8_C_DN	C242	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_8_DN
<14> PE3_CPU1_3_SB_9_C_DP	C241	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_9_DP
<14> PE3_CPU1_3_SB_9_C_DN	C240	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_9_DN
<14> PE3_CPU1_3_SB_10_C_DP	C239	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_10_DP
<14> PE3_CPU1_3_SB_10_C_DN	C238	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_10_DN
<14> PE3_CPU1_3_SB_11_C_DP	C237	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_11_DP
<14> PE3_CPU1_3_SB_11_C_DN	C236	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_11_DN
<14> PE3_CPU1_3_SB_12_C_DP	C235	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_12_DP
<14> PE3_CPU1_3_SB_12_C_DN	C270	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_12_DN
<14> PE3_CPU1_3_SB_13_C_DP	C269	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_13_DP
<14> PE3_CPU1_3_SB_13_C_DN	C268	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_13_DN
<14> PE3_CPU1_3_SB_14_C_DP	C267	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_14_DP
<14> PE3_CPU1_3_SB_14_C_DN	C266	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_14_DN
<14> PE3_CPU1_3_SB_15_C_DP	C265	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_15_DP
<14> PE3_CPU1_3_SB_15_C_DN	C260	220nF 16V,X7R,+/-10%	PE3_CPU1_3_SB_15_DN

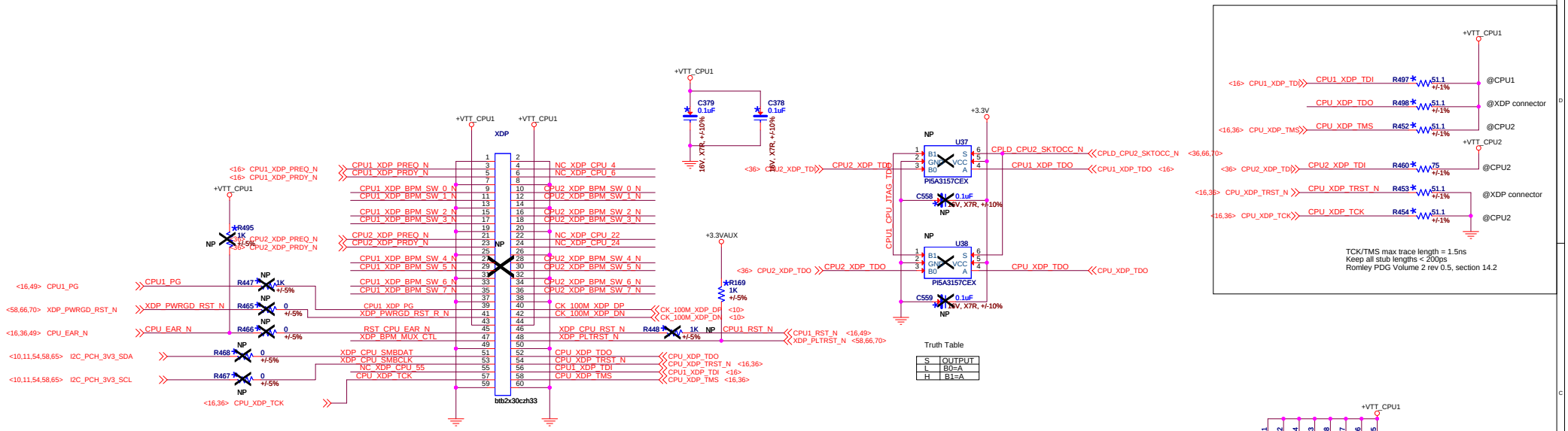
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

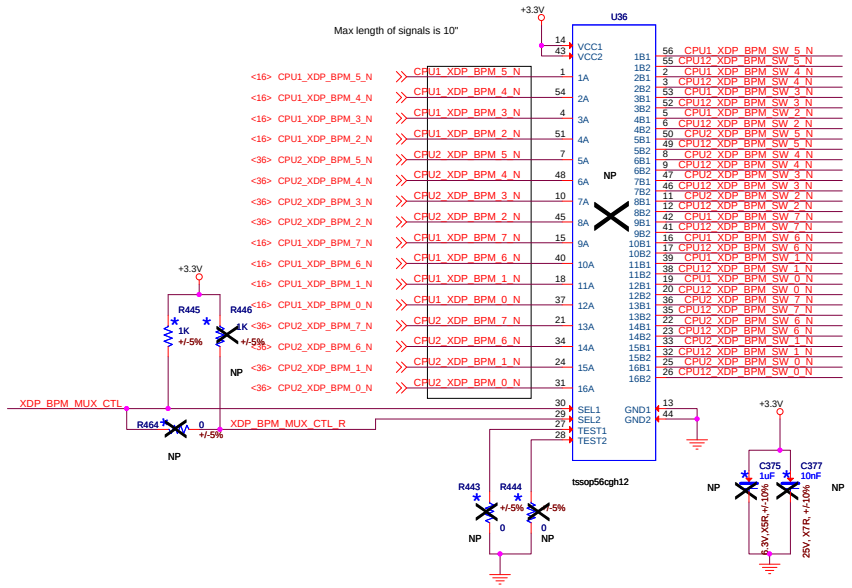
DWG NO
PN27H

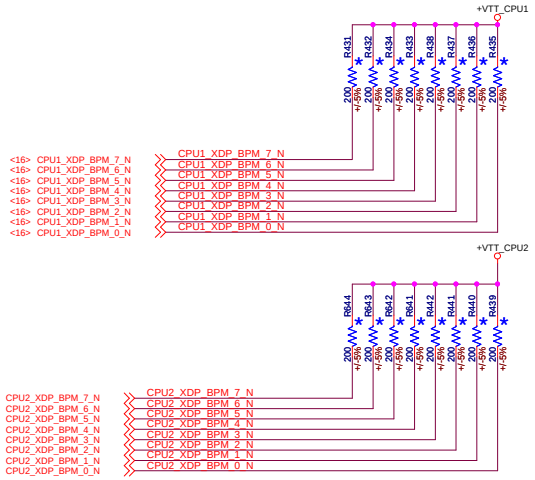
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 30 of 96

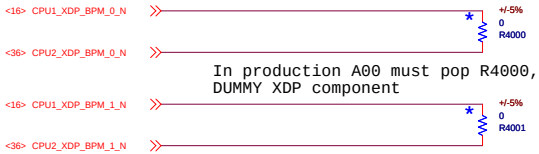


Each group of signals to or from the mux must be length-matched to within 50ps





BPM terminations should be placed near each processor



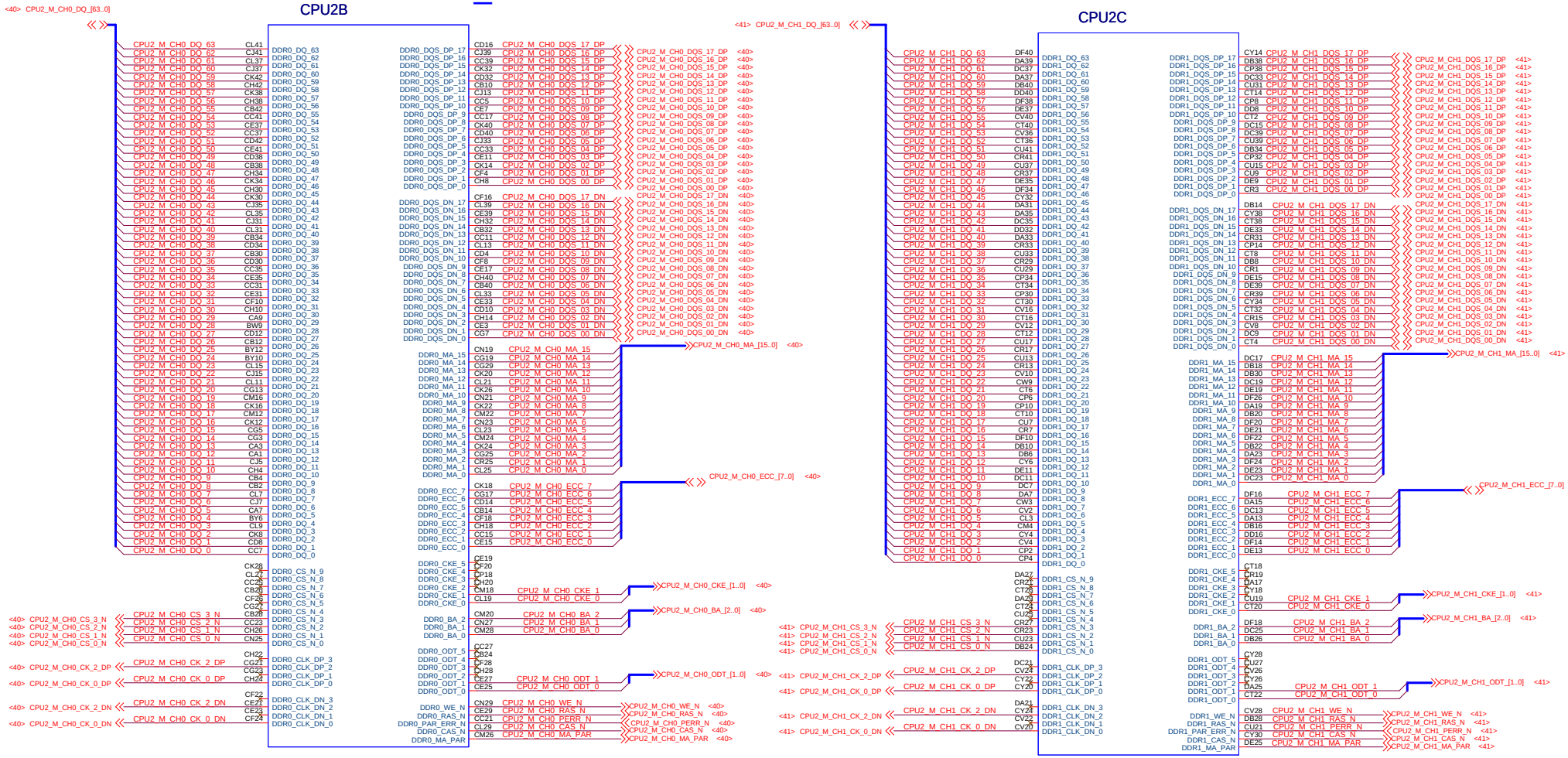
Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	31 of 96

DDR_CH0

DDR_CH1

CPU2B

CPU2C



RoseCity-PG35

RoseCity-PG36

DELL INC.

Title

SCHEM, PWA, LITTLE, SUR

DWG NO

PN27H

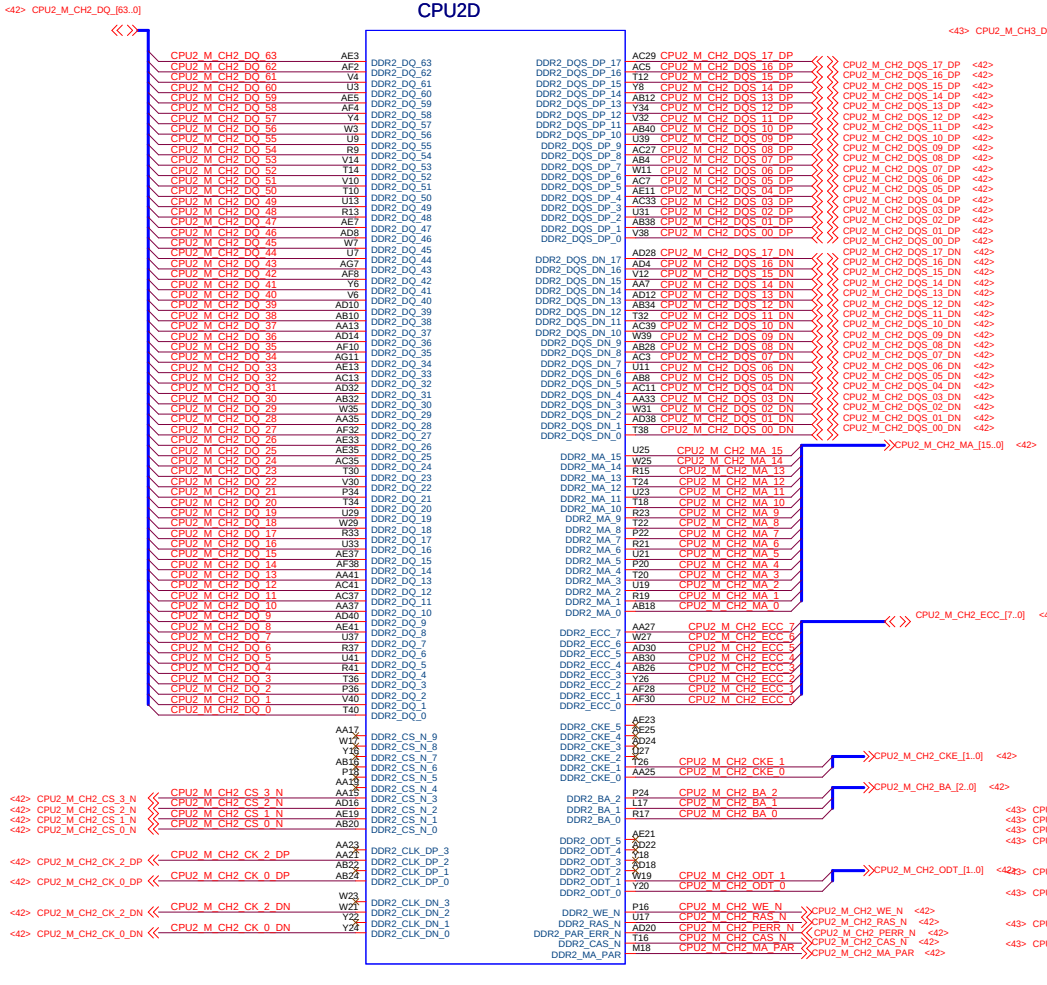
Rev

A01

Date: Wednesday, June 20, 2012 Sheet 32 of 96

DDR_CH2

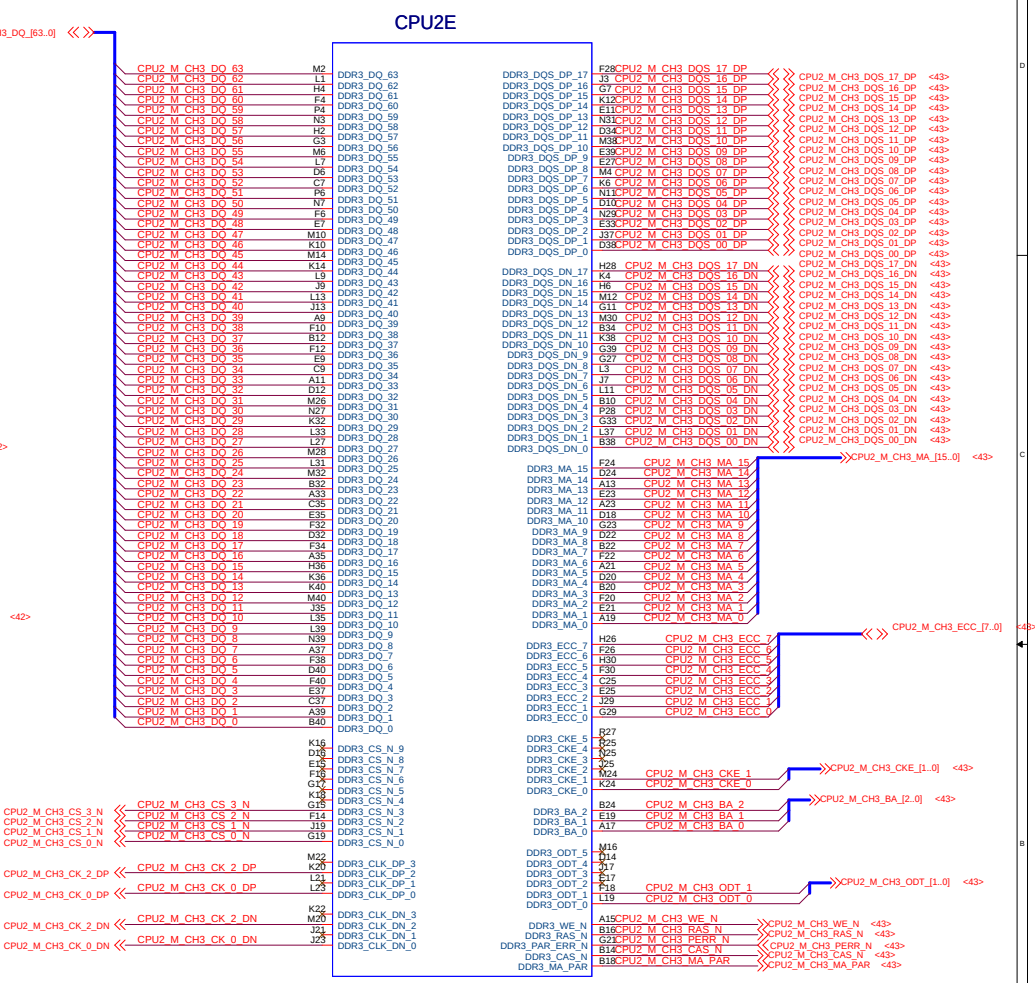
CPU2D



RoseCity-PG37

DDR_CH3

CPU2E



RoseCity-PG38

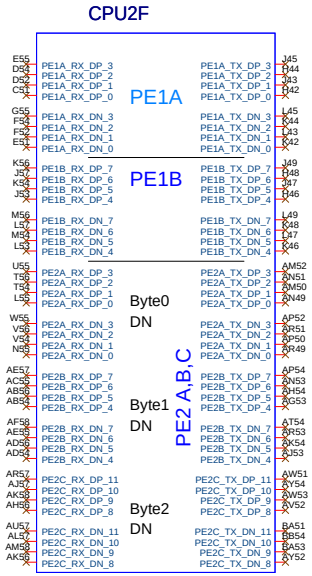
DELL INC.

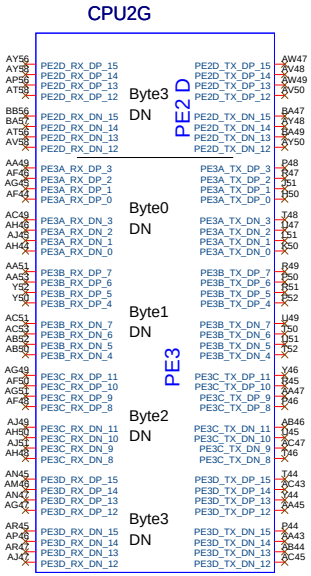
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 33 of 96





SandyBridge_EPEX_EDS_Vol1_26601,0.5.pvd Figure 1-3 pg.16

Port0	Port1	Port2	Port3
DMI	PE1[A:B]	PE2[A:B:C:D]	PE3[A:B:C:D]
IOU2---IOU2		IOU0	IOU1
Unused	Unused	X16 slot	X16 slot

DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

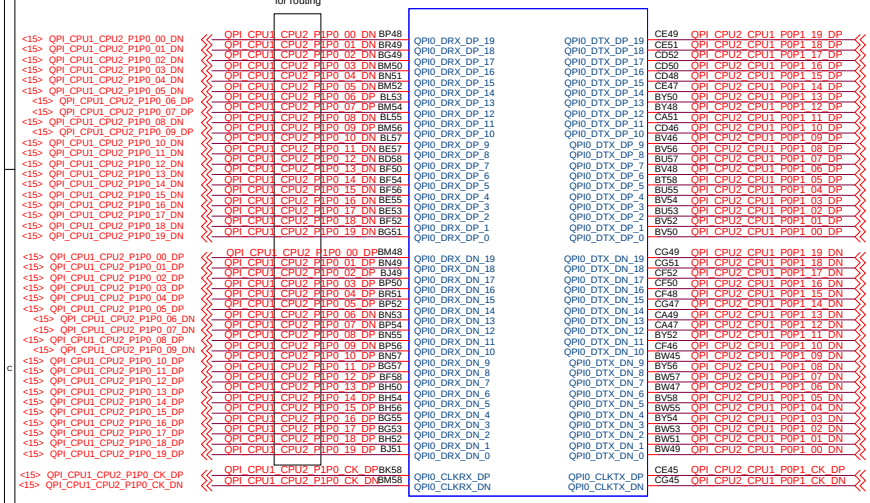
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 34 of 96

QPI0 interface

Lane Reversed & DP\DN swapped on most lanes for routing

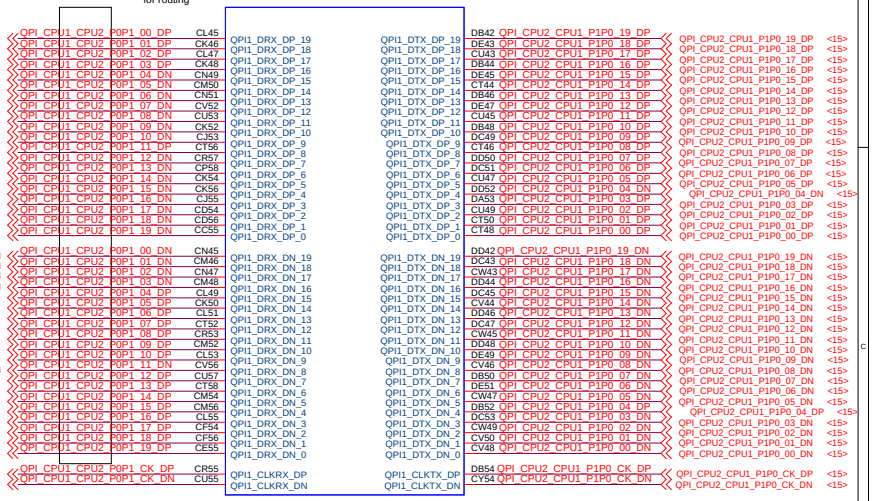
CPU2I



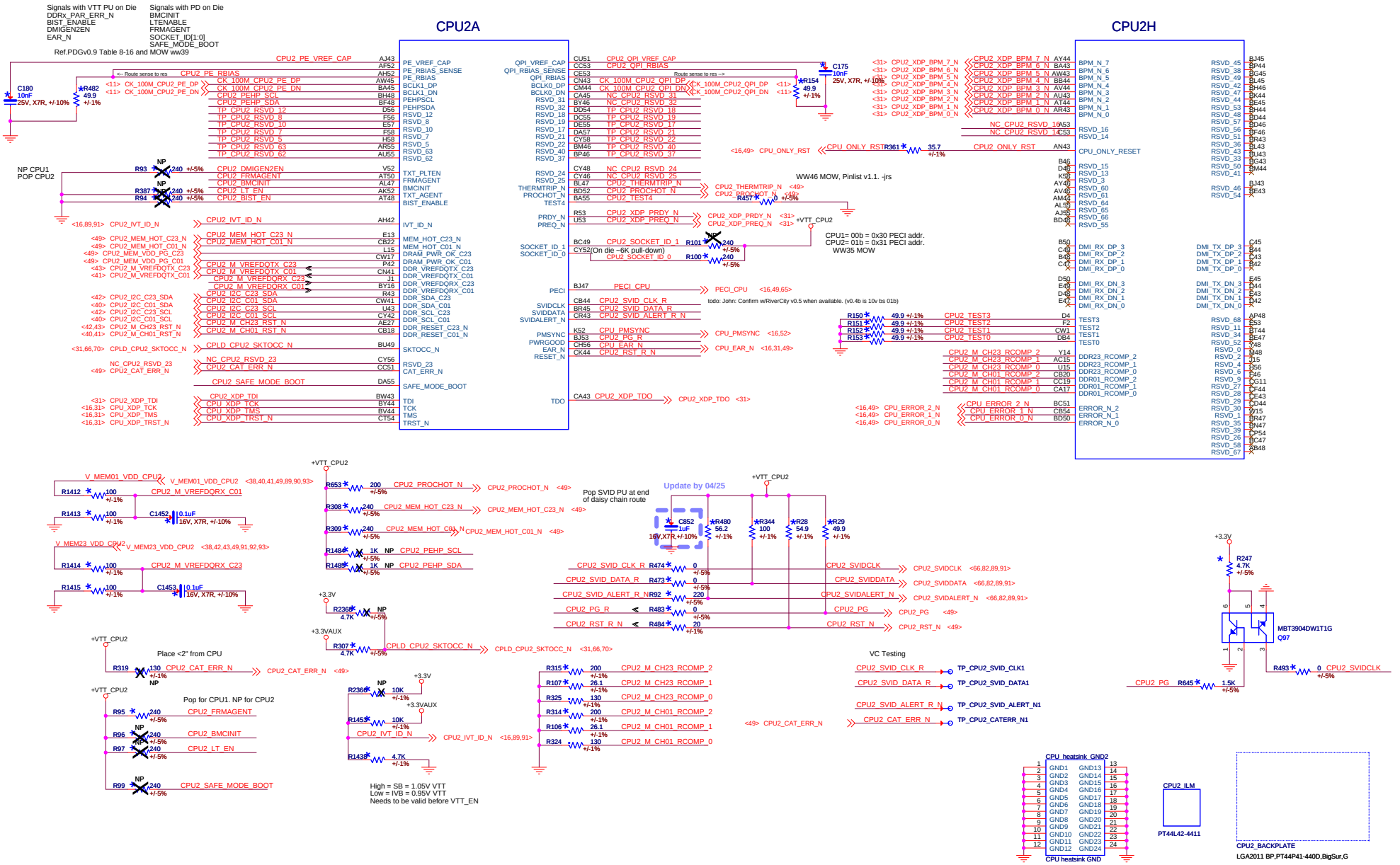
QPI1 interface

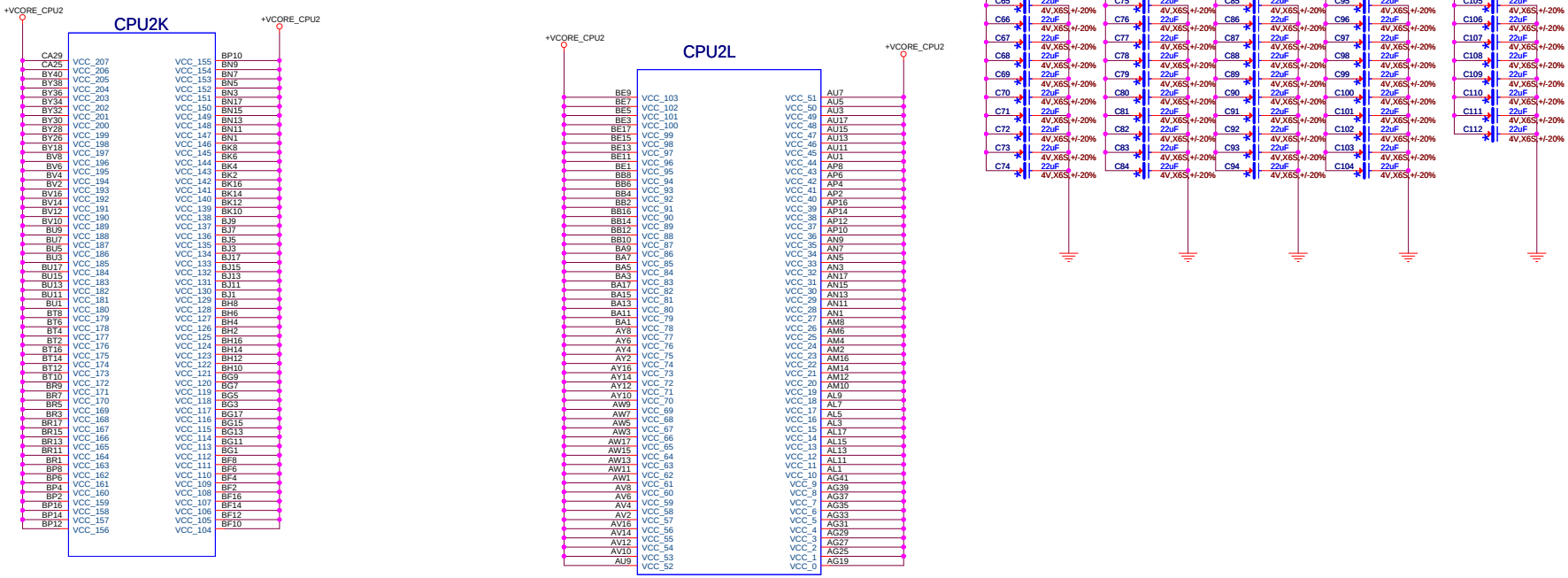
Lane Reversed & DP\DN swapped on most lanes for routing

CPU2J



Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	35 of 96


Signals with VTT PU on Die
DDRx_PAR_ERR_N
BIST_ENABLE
DMIGEN2EN
EAR_N
Signals with PD on Die
BMCINIT
LTENABLE
FRMAGENT
SOCKET_ID[1:0]
SAFE_MODE_BOOT
Ref.PDGv0.9 Table 8-16 and MOW ww39
CPU2A
CPU2H
CPU2_PE_VREF_CAP
CPU2_PE_RBIAS
CK_100M_CPU2_PE_DP
CK_100M_CPU2_PE_DN
CPU2_PEHP_SCL
CPU2_PEHP_SDA
TP_CPU2_RSVD_12
TP_CPU2_RSVD_8
TP_CPU2_RSVD_10
TP_CPU2_RSVD_7
TP_CPU2_RSVD_5
TP_CPU2_RSVD_63
TP_CPU2_RSVD_62
CPU2_DMIGEN2EN
CPU2_FRMAGENT
CPU2_BMCINIT
CPU2_LT_EN
CPU2_BIST_EN
CPU2_IVT_ID_N
CPU2_MEM_HOT_C23_N
CPU2_MEM_HOT_C01_N
CPU2_M_VREFDQTX_C23
CPU2_M_VREFDQTX_C01
CPU2_M_VREFDQRX_C23
CPU2_M_VREFDQRX_C01
CPU2_I2C_C23_SDA
CPU2_I2C_C01_SDA
CPU2_I2C_C23_SCL
CPU2_I2C_C01_SCL
CPU2_M_CH23_RST_N
CPU2_M_CH01_RST_N
CPLD_CPU2_SKTOCC_N
NC_CPU2_RSVD_23
CPU2_CAT_ERR_N
CPU2_SAFE_MODE_BOOT
CPU2_XDP_TDI
CPU_XDP_TCK
CPU_XDP_TMS
CPU_XDP_TRST_N
QPI_VREF_CAP
QPI_RBIAS
QPI_RBIAS_SENSE
CK_100M_CPU2_QPI_DP
CK_100M_CPU2_QPI_DN
NC_CPU2_RSVD_31
NC_CPU2_RSVD_32
TP_CPU2_RSVD_18
TP_CPU2_RSVD_19
TP_CPU2_RSVD_17
TP_CPU2_RSVD_21
TP_CPU2_RSVD_22
TP_CPU2_RSVD_40
TP_CPU2_RSVD_37
NC_CPU2_RSVD_24
NC_CPU2_RSVD_25
CPU2_THERMTRIP_N
CPU2_PROCHOT_N
CPU2_TEST4
CPU2_XDP_PRDY_N
CPU2_XDP_PREQ_N
CPU2_SOCKET_ID_1
CPU2_SOCKET_ID_0
PECI_CPU
CPU2_SVID_CLK_R
CPU2_SVID_DATA_R
CPU2_SVID_ALERT_R_N
CPU_PMSYNC
CPU_PG_R
CPU_EAR_N
CPU2_RST_R_N
CPU2_XDP_TDO
CPU_ONLY_RST
WW46 MOW, Pinlist v1.1. -jrs
CPU1= 00b = 0x30 PECI addr.
CPU2= 01b = 0x31 PECI addr.
WW35 MOW
todo: John: Confirm w/RiverCity v0.5 when available. (v0.4b is 10v bs 01b)
CPU2_TEST3
CPU2_TEST2
CPU2_TEST1
CPU2_TEST0
CPU2_M_CH23_RCOMP_2
CPU2_M_CH23_RCOMP_1
CPU2_M_CH23_RCOMP_0
CPU2_M_CH01_RCOMP_2
CPU2_M_CH01_RCOMP_1
CPU2_M_CH01_RCOMP_0
CPU_ERROR_2_N
CPU_ERROR_1_N
CPU_ERROR_0_N
CPU2_XDP_BPM_7_N
CPU2_XDP_BPM_6_N
CPU2_XDP_BPM_5_N
CPU2_XDP_BPM_4_N
CPU2_XDP_BPM_3_N
CPU2_XDP_BPM_2_N
CPU2_XDP_BPM_1_N
CPU2_XDP_BPM_0_N
NC_CPU2_RSVD_16
NC_CPU2_RSVD_14
CPU2_ONLY_RST
DMI_RX_DP_3
DMI_RX_DP_2
DMI_RX_DP_1
DMI_RX_DP_0
DMI_RX_DN_3
DMI_RX_DN_2
DMI_RX_DN_1
DMI_RX_DN_0
DMI_TX_DP_3
DMI_TX_DP_2
DMI_TX_DP_1
DMI_TX_DP_0
DMI_TX_DN_3
DMI_TX_DN_2
DMI_TX_DN_1
DMI_TX_DN_0
Update by 04/25
Pop SVID PU at end of daisy chain route
Pop for CPU1. NP for CPU2
Place <2" from CPU
High = SB = 1.05V VTT
Low = IVB = 0.95V VTT
Needs to be valid before VTT_EN
VC Testing
TP_CPU2_SVID_CLK1
TP_CPU2_SVID_DATA1
TP_CPU2_SVID_ALERT_N1
TP_CPU2_CATERR_N1
MBT3904DW1T1G
Q97
CPU heatsink GND
CPU2_ILM
PT44L42-4411
CPU2_BACKPLATE
LGA2011 BP,PT44P41-440D,BigSur,G
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 36 of 96



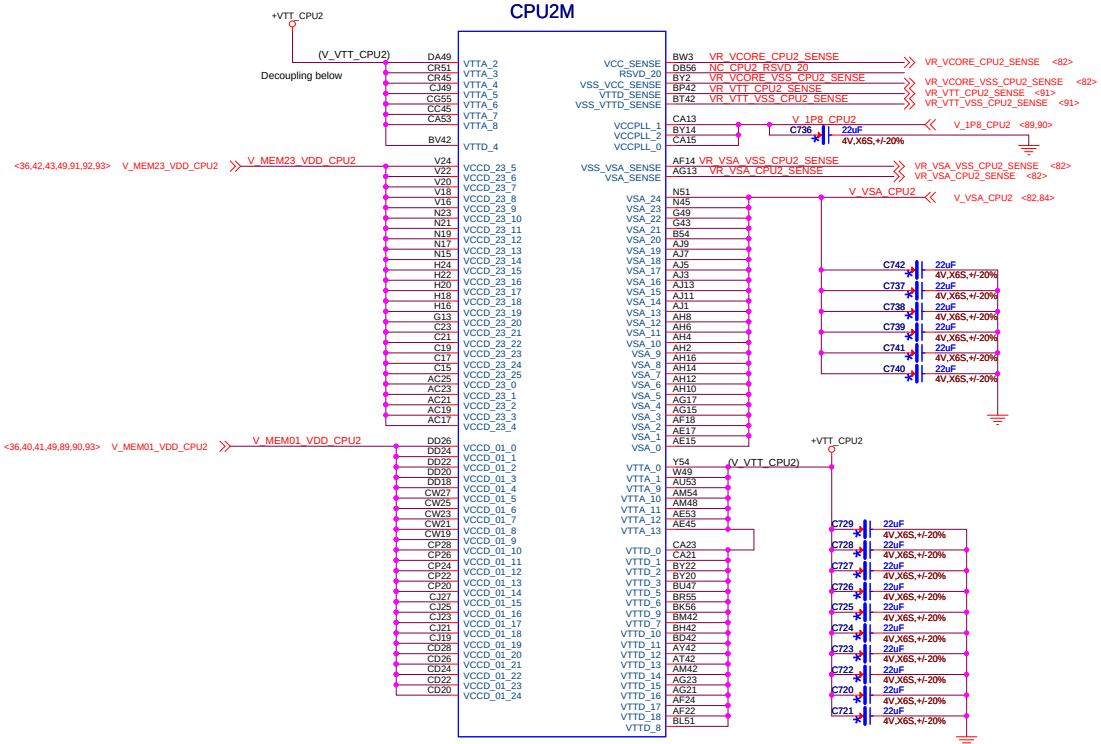
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 37 of 96



RoseCity-PG45

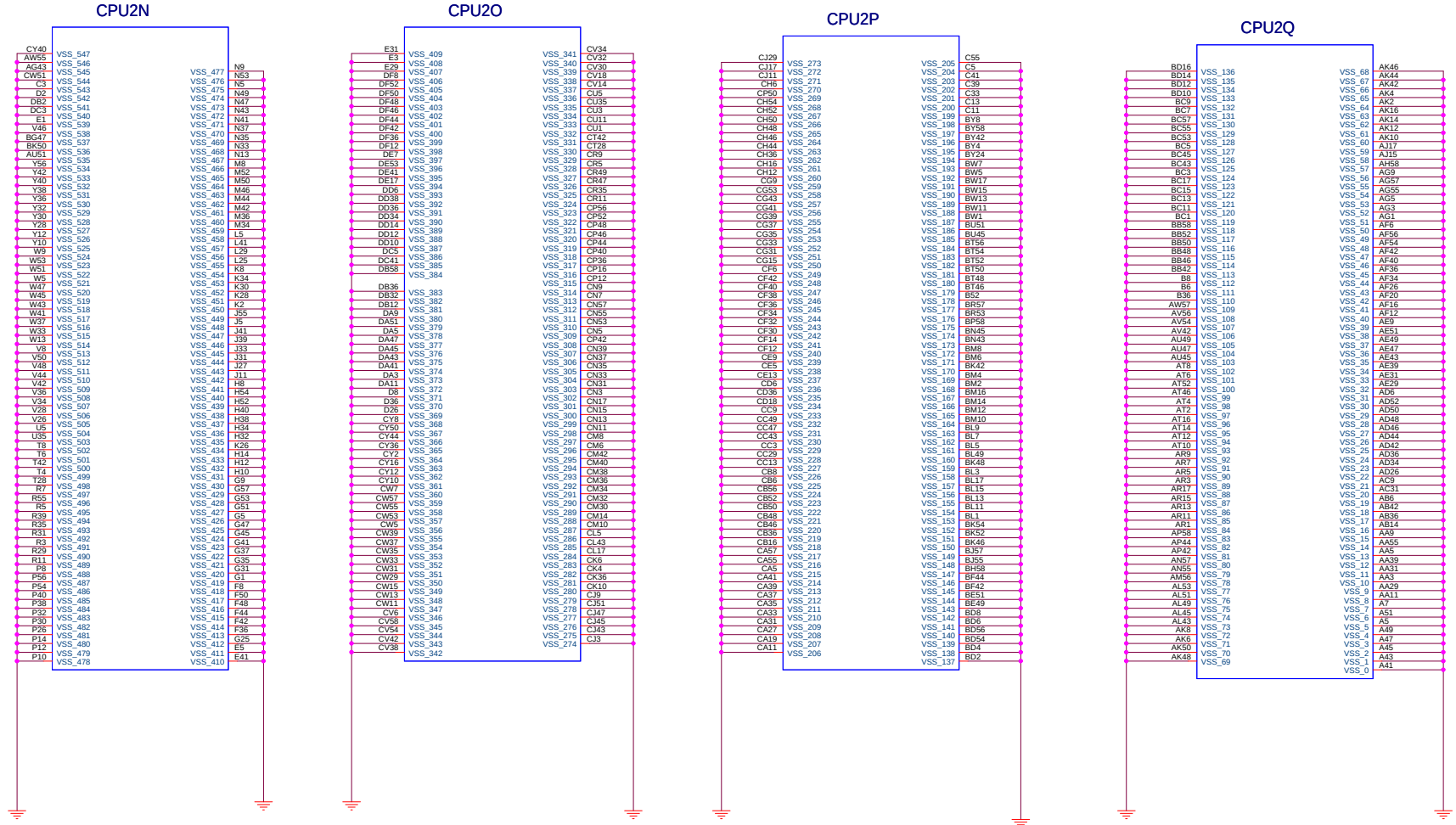
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 38 of 96



DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

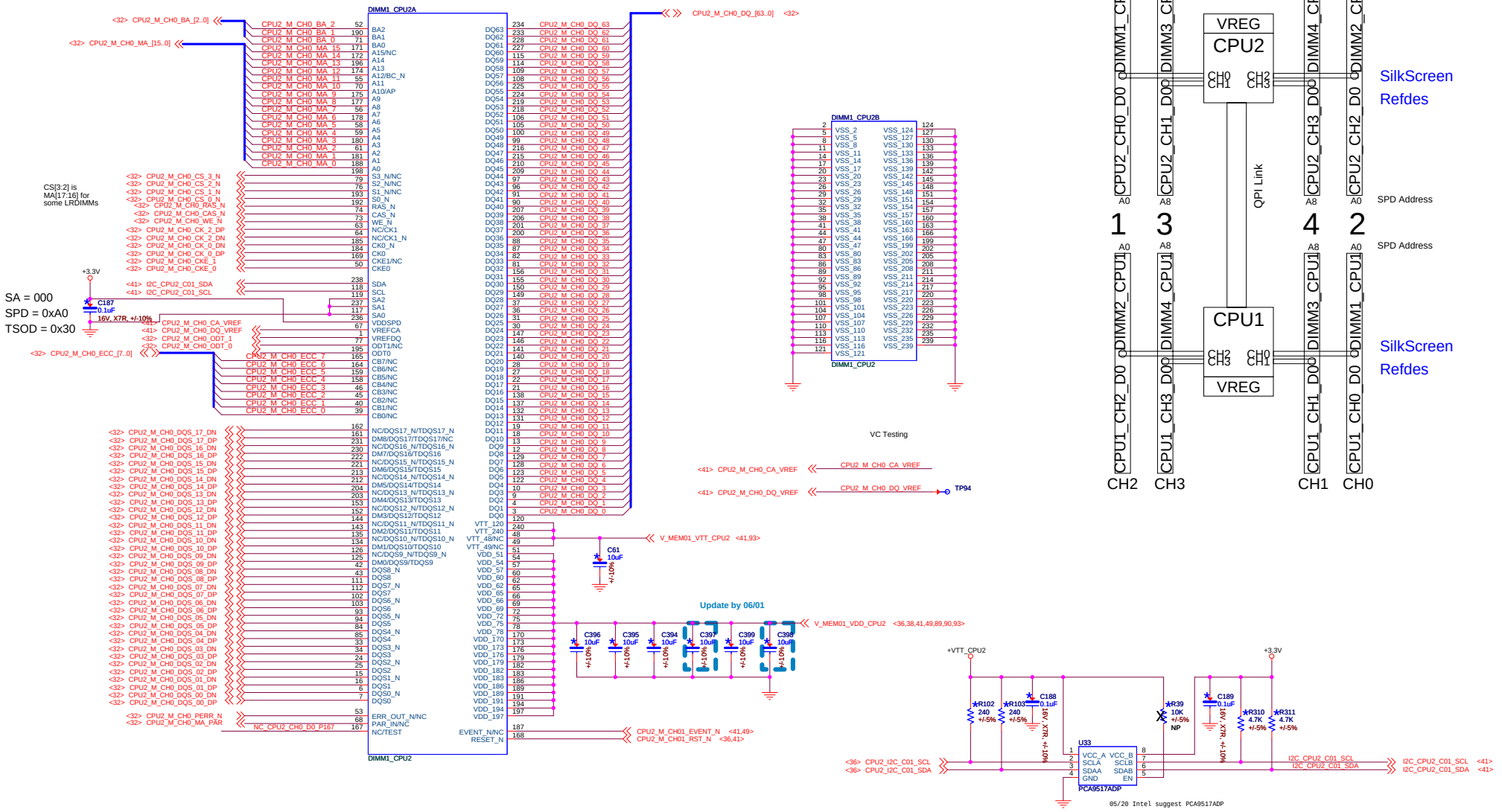
DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012

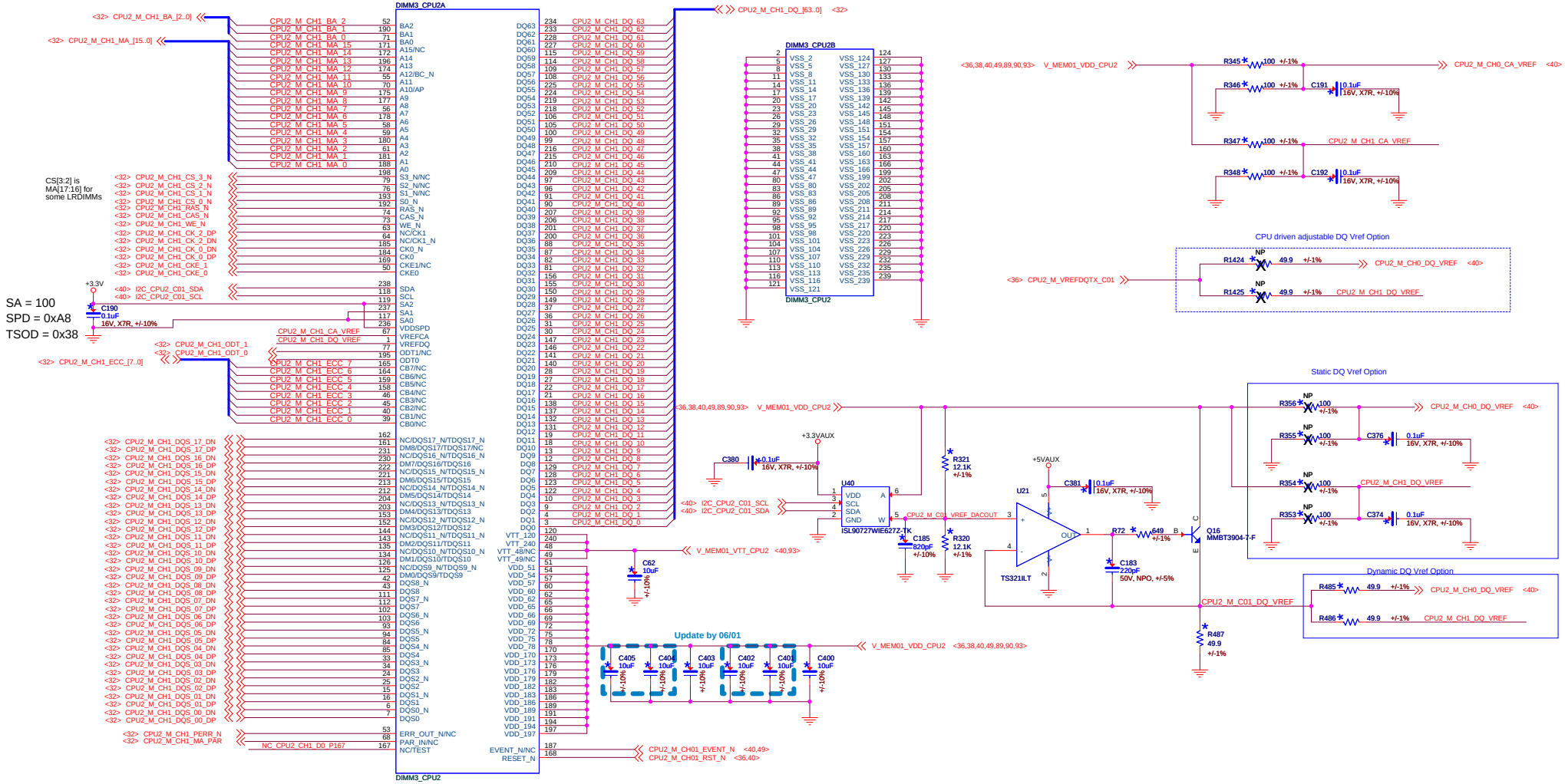
Sheet 39 of 96

CPU2_CH0_D0



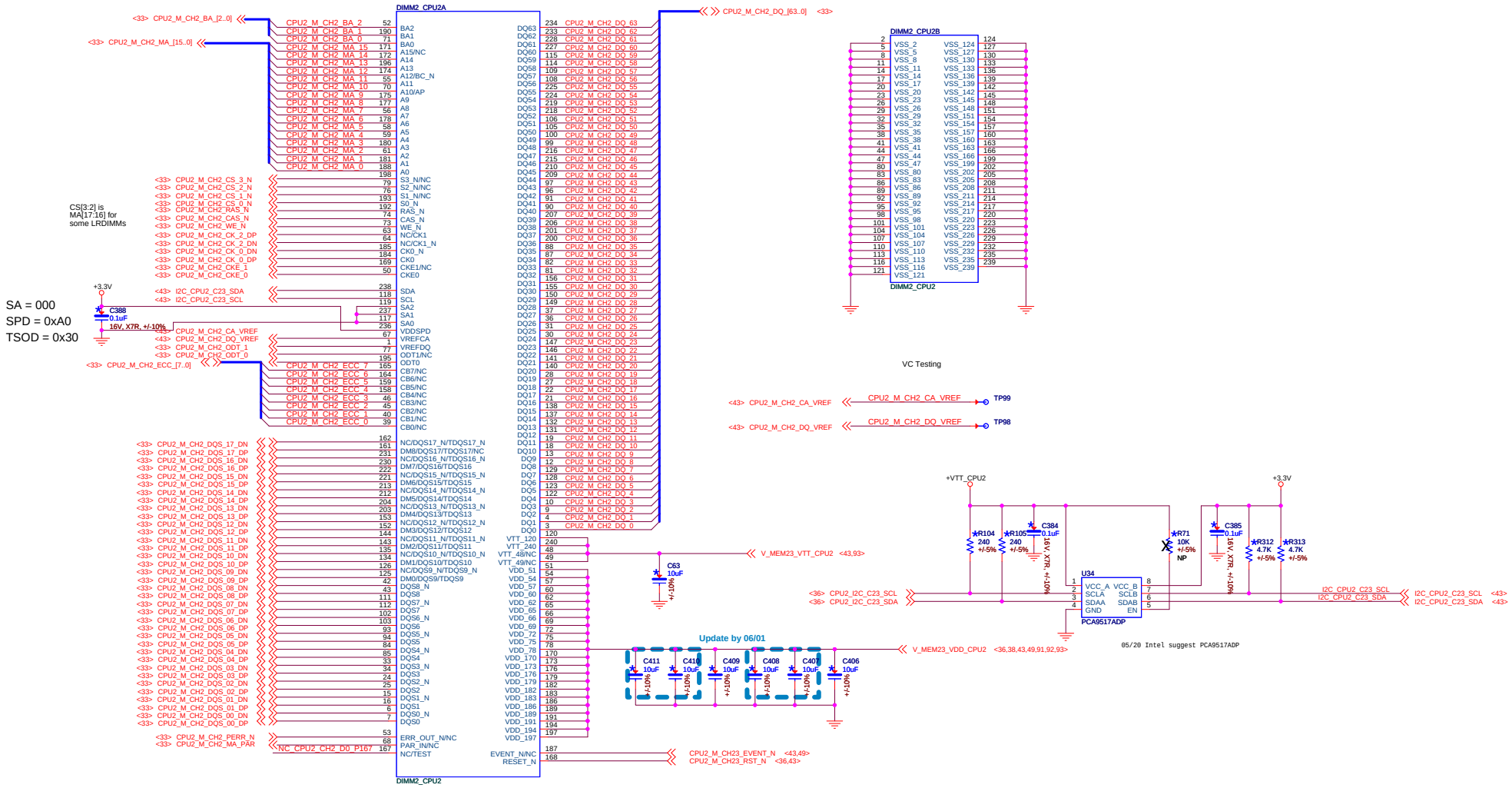
Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	40 of 96

CPU2_CH1_D0


DIMM3_CPU2A
DIMM3_CPU2B
DIMM3_CPU2
CPU2_M_CH1_BA_[2..0]
CPU2_M_CH1_MA_[15..0]
CPU2_M_CH1_DQ_[63..0]
CS[3:2] is MA[17:16] for some LRDIMMs
SA = 100
SPD = 0xA8
TSOD = 0x38
CPU2_M_CH1_ECC_[7..0]
V_MEM01_VDD_CPU2
V_MEM01_VTT_CPU2
CPU2_M_CH1_CA_VREF
CPU2_M_CH1_DQ_VREF
CPU2_M_VREFDQTX_C01
CPU driven adjustable DQ Vref Option
Static DQ Vref Option
Dynamic DQ Vref Option
Update by 06/01
ISL90727WIE627Z-TK
TS321ILT
MMBT3904-7-F
VC Testing
CPU2_M_CH1_CA_VREF
CPU2_M_CH1_DQ_VREF

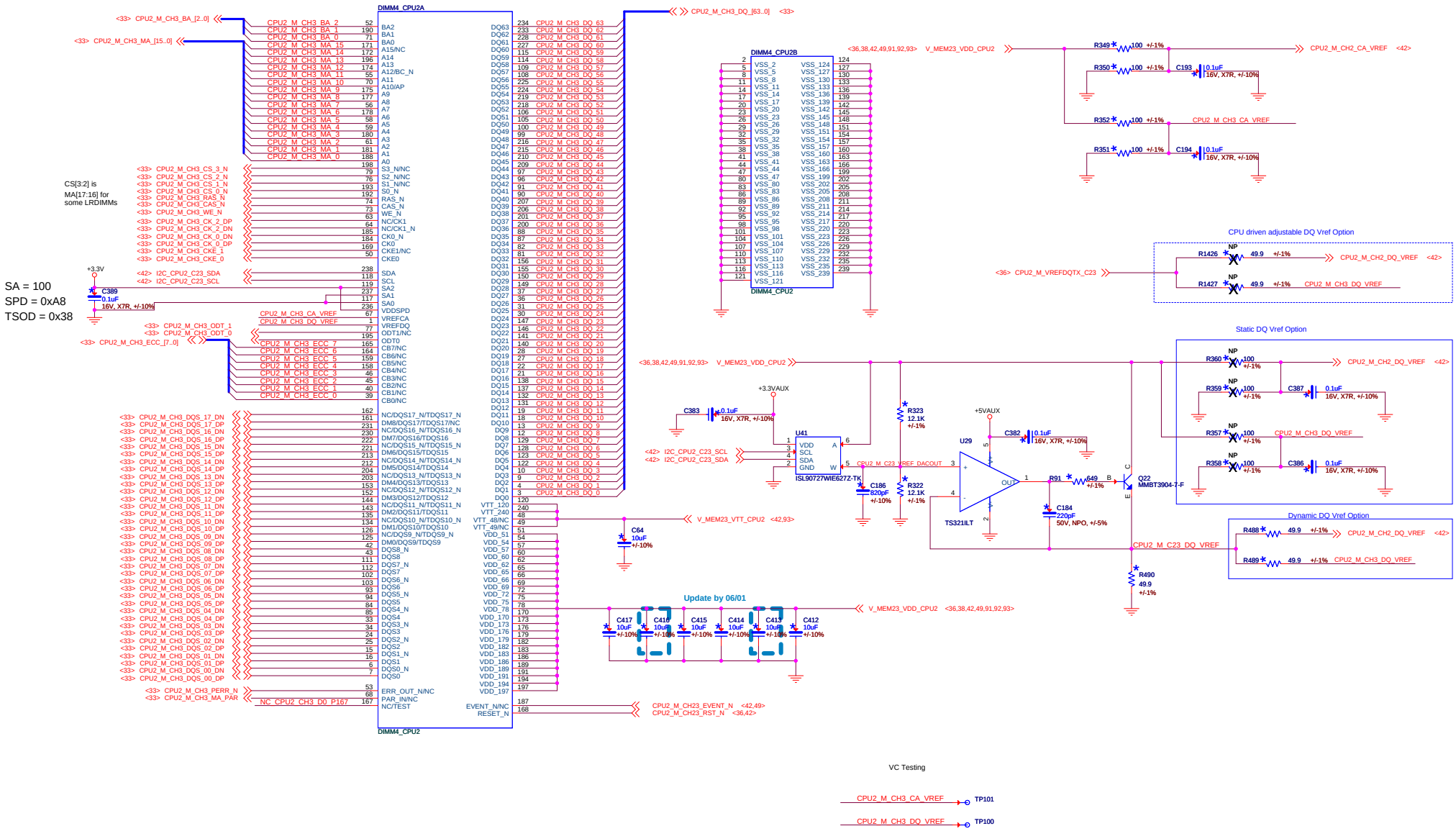
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 41 of 96

CPU2_CH2_D0



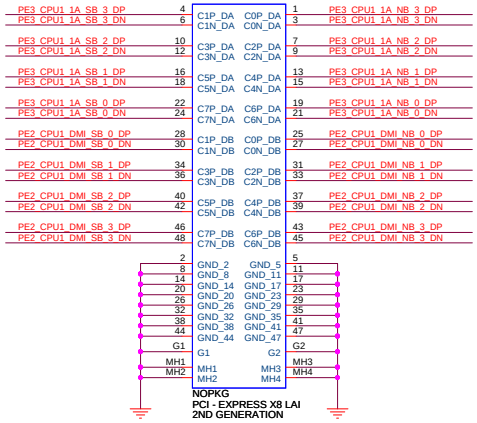
Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	42 of 96

CPU2_CH3_D0



Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	43 of 96

LAI_DMI_PCIE



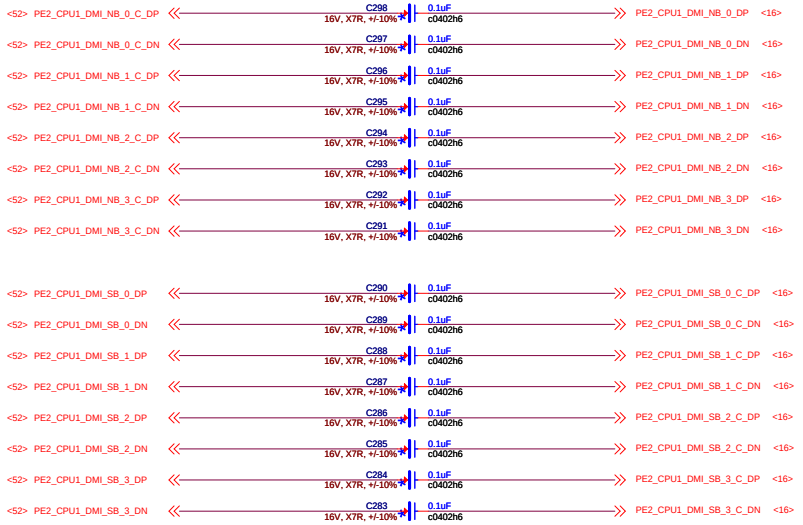
On SandyBridge side caps. Verify w/SI & layout

PCIe x4 Uplink port on CPU1/PCH

See Romley_PDG_Vol2_27178,0.5.pvd Table 14-28
Polarity (DP/DN) may be swapped.
Entire link assignment may be reversed:

SB_0 --> SB_3
SB_1 --> SB_2
SB_2 --> SB_1
SB_3 --> SB_0

To DMI on PCH



To X4 on PCH

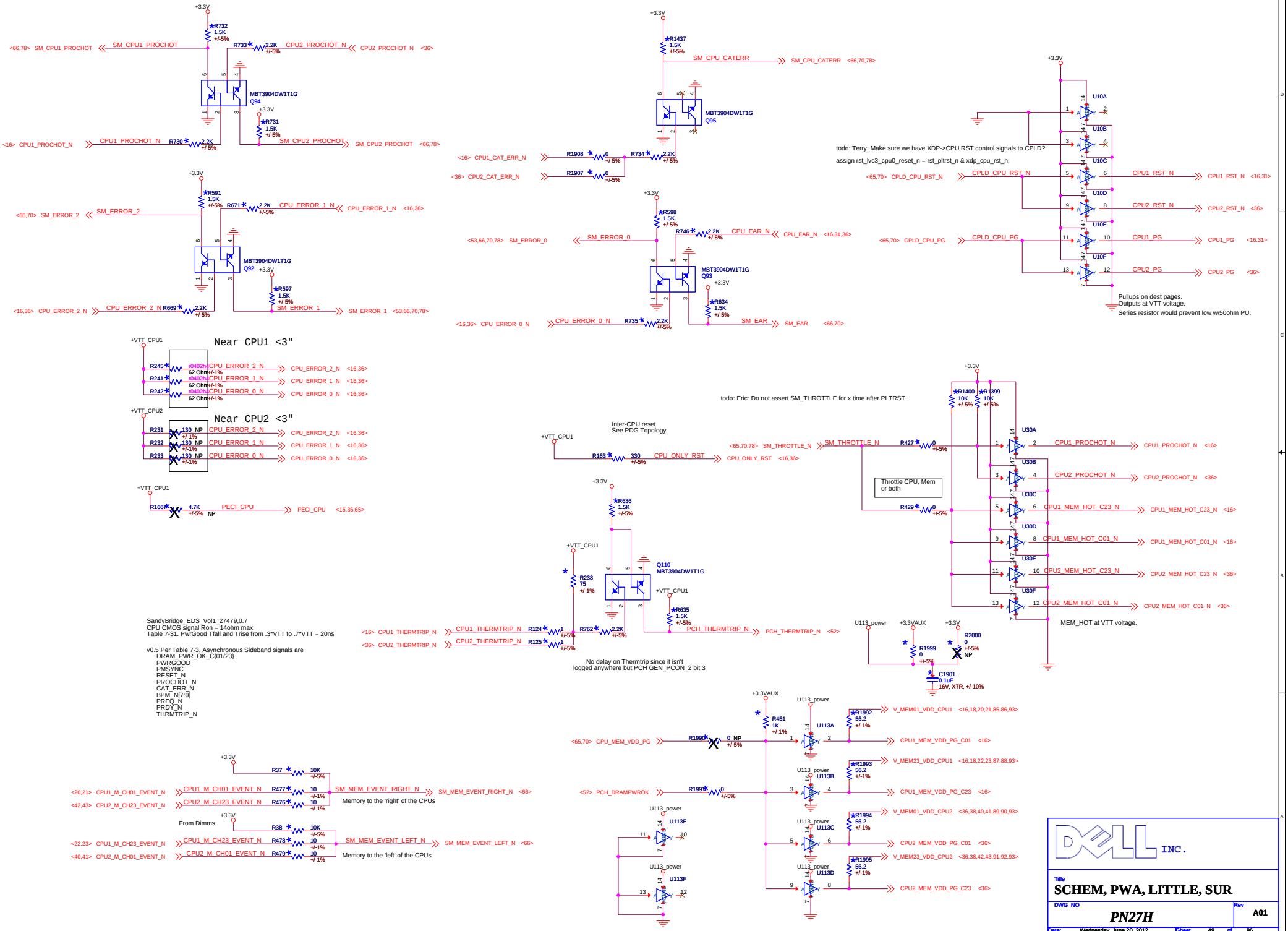
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 48 of 96


+3.3V
R732 1.5K +/-5%
<66,78> SM_CPU1_PROCHOT
SM_CPU1_PROCHOT
R733 2.2K +/-5%
CPU2_PROCHOT_N
CPU2_PROCHOT_N <36>
MBT3904DW1T1G
Q94
R731 1.5K +/-5%
<16> CPU1_PROCHOT_N
CPU1_PROCHOT_N
R730 2.2K +/-5%
SM_CPU2_PROCHOT
SM_CPU2_PROCHOT <66,78>
R1437 1.5K +/-5%
SM_CPU_CATERR
SM_CPU_CATERR <66,70,78>
MBT3904DW1T1G
Q95
<16> CPU1_CAT_ERR_N
R1908 0 +/-5%
R734 2.2K +/-5%
<36> CPU2_CAT_ERR_N
R1907 0 +/-5%
todo: Terry: Make sure we have XDP->CPU RST control signals to CPLD?
assign rst_lvc3_cpu0_reset_n = rst_pltrst_n & xdp_cpu_rst_n;
U10A
U10B
U10C
U10D
U10E
U10F
<65,70> CPLD_CPU_RST_N
CPLD_CPU_RST_N
CPU1_RST_N
CPU1_RST_N <16,31>
CPU2_RST_N
CPU2_RST_N <36>
<65,70> CPLD_CPU_PG
CPLD_CPU_PG
CPU1_PG
CPU1_PG <16,31>
CPU2_PG
CPU2_PG <36>
Pullups on dest pages.
Outputs at VTT voltage.
Series resistor would prevent low w/50ohm PU.
R591 1.5K +/-5%
<66,70> SM_ERROR_2
SM_ERROR_2
R671 2.2K +/-5%
CPU_ERROR_1_N
CPU_ERROR_1_N <16,36>
MBT3904DW1T1G
Q92
R597 1.5K +/-5%
<16,36> CPU_ERROR_2_N
CPU_ERROR_2_N
R669 2.2K +/-5%
SM_ERROR_1
SM_ERROR_1 <53,66,70,78>
R598 1.5K +/-5%
<53,66,70,78> SM_ERROR_0
SM_ERROR_0
R746 2.2K +/-5%
CPU_EAR_N
CPU_EAR_N <16,31,36>
MBT3904DW1T1G
Q93
R634 1.5K +/-5%
<16,36> CPU_ERROR_0_N
CPU_ERROR_0_N
R735 2.2K +/-5%
SM_EAR
SM_EAR <66,70>
+VTT_CPU1
Near CPU1 <3"
R245 r0402hi 62 Ohm +/-1%
R241 r0402hi 62 Ohm +/-1%
R242 r0402hi 62 Ohm +/-1%
CPU_ERROR_2_N
CPU_ERROR_1_N
CPU_ERROR_0_N
CPU_ERROR_2_N <16,36>
CPU_ERROR_1_N <16,36>
CPU_ERROR_0_N <16,36>
+VTT_CPU2
Near CPU2 <3"
R231 130 NP +/-1%
R232 130 NP +/-1%
R233 130 NP +/-1%
R166 4.7K +/-5% NP
PECI_CPU
PECI_CPU <16,36,65>
todo: Eric: Do not assert SM_THROTTLE for x time after PLTRST.
Inter-CPU reset
See PDG Topology
R163 330 +/-5%
CPU_ONLY_RST
CPU_ONLY_RST <16,36>
<65,70,78> SM_THROTTLE_N
SM_THROTTLE_N
R427 0 +/-5%
R429 0 +/-5%
Throttle CPU, Mem or both
R1400 10K +/-5%
R1399 10K +/-5%
U30A
U30B
U30C
U30D
U30E
U30F
CPU1_PROCHOT_N
CPU1_PROCHOT_N <16>
CPU2_PROCHOT_N
CPU2_PROCHOT_N <36>
CPU1_MEM_HOT_C23_N
CPU1_MEM_HOT_C23_N <16>
CPU1_MEM_HOT_C01_N
CPU1_MEM_HOT_C01_N <16>
CPU2_MEM_HOT_C23_N
CPU2_MEM_HOT_C23_N <36>
CPU2_MEM_HOT_C01_N
CPU2_MEM_HOT_C01_N <36>
MEM_HOT at VTT voltage.
R636 1.5K +/-5%
R238 75 +/-1%
Q110
MBT3904DW1T1G
R635 1.5K +/-5%
<16> CPU1_THERMTRIP_N
CPU1_THERMTRIP_N
R124 1 +/-5%
R762 2.2K +/-5%
<36> CPU2_THERMTRIP_N
CPU2_THERMTRIP_N
R125 1 +/-5%
PCH_THERMTRIP_N
PCH_THERMTRIP_N <52>
No delay on Thermtrip since it isn't
logged anywhere but PCH GEN_PCON_2 bit 3
U113_power
+3.3VAUX
R1999 0 +/-5%
R2000 0 +/-5% NP
C1901 0.1uF 16V, X7R, +/-10%
SandyBridge_EDS_Vol1_27479,0.7
CPU CMOS signal Ron = 14ohm max
Table 7-31. PwrGood Tfall and Trise from .3*VTT to .7*VTT = 20ns
v0.5 Per Table 7-3. Asynchronous Sideband signals are
DRAM_PWR_OK_C{01/23}
PWRGOOD
PMSYNC
RESET_N
PROCHOT_N
CAT_ERR_N
BPM_N[7:0]
PREQ_N
PRDY_N
THRMTRIP_N
R37 10K +/-5%
<20,21> CPU1_M_CH01_EVENT_N
CPU1_M_CH01_EVENT_N
R477 10 +/-1%
<42,43> CPU2_M_CH23_EVENT_N
CPU2_M_CH23_EVENT_N
R476 10 +/-1%
SM_MEM_EVENT_RIGHT_N
SM_MEM_EVENT_RIGHT_N <66>
Memory to the 'right' of the CPUs
From Dimms
R38 10K +/-5%
<22,23> CPU1_M_CH23_EVENT_N
CPU1_M_CH23_EVENT_N
R478 10 +/-1%
<40,41> CPU2_M_CH01_EVENT_N
CPU2_M_CH01_EVENT_N
R479 10 +/-1%
SM_MEM_EVENT_LEFT_N
SM_MEM_EVENT_LEFT_N <66>
Memory to the 'left' of the CPUs
+3.3VAUX
R451 1K +/-1%
<65,70> CPU_MEM_VDD_PG
R1998 0 NP +/-5%
<52> PCH_DRAMPWROK
R1997 0 +/-5%
U113A
U113B
U113C
U113D
U113E
U113F
R1992 56.2 +/-1%
V_MEM01_VDD_CPU1 <16,18,20,21,85,86,93>
CPU1_MEM_VDD_PG_C01 <16>
R1993 56.2 +/-1%
V_MEM23_VDD_CPU1 <16,18,22,23,87,88,93>
CPU1_MEM_VDD_PG_C23 <16>
R1994 56.2 +/-1%
V_MEM01_VDD_CPU2 <36,38,40,41,89,90,93>
CPU2_MEM_VDD_PG_C01 <36>
R1995 56.2 +/-1%
V_MEM23_VDD_CPU2 <36,38,42,43,91,92,93>
CPU2_MEM_VDD_PG_C23 <36>
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 49 of 96

DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 50 of 96

DELL INC.

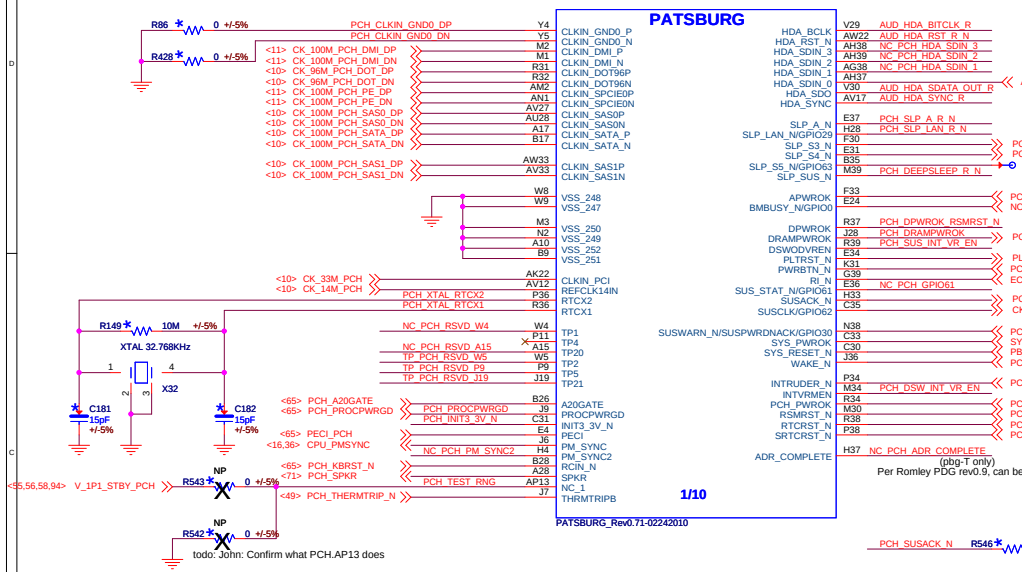
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

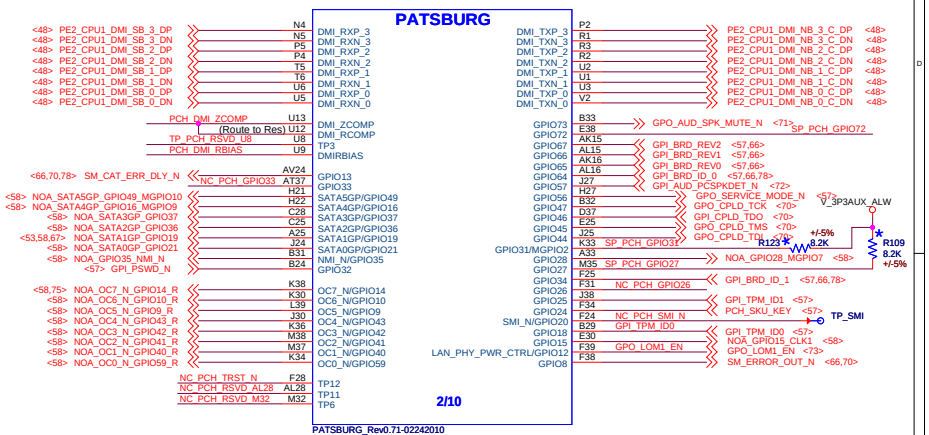
Rev
A01

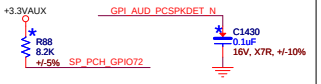
Date: Wednesday, June 20, 2012 Sheet 51 of 96

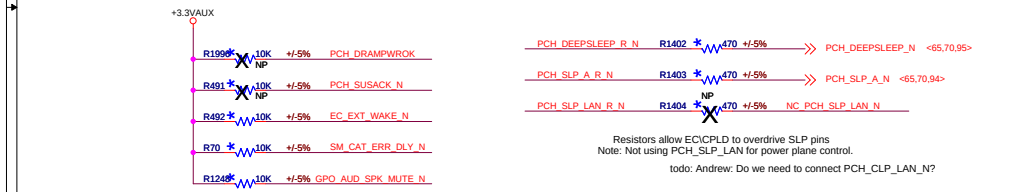
U_PCH

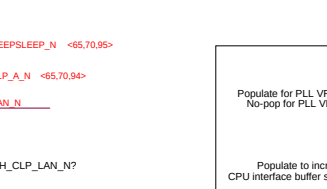


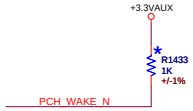
U_PCH

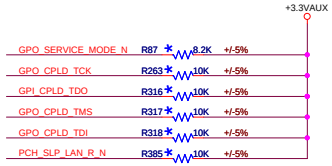




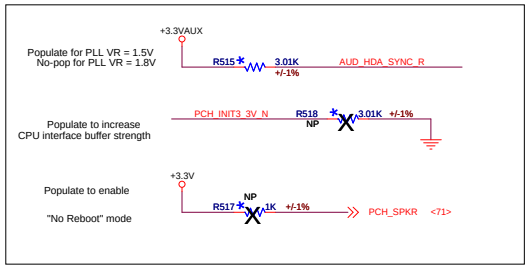


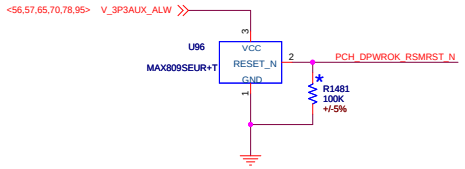


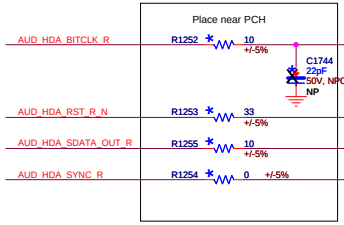


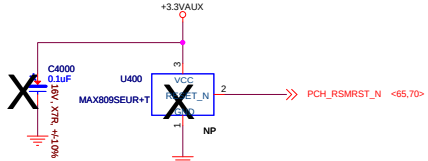


See PCH Section 2.28.1 on Functional Straps









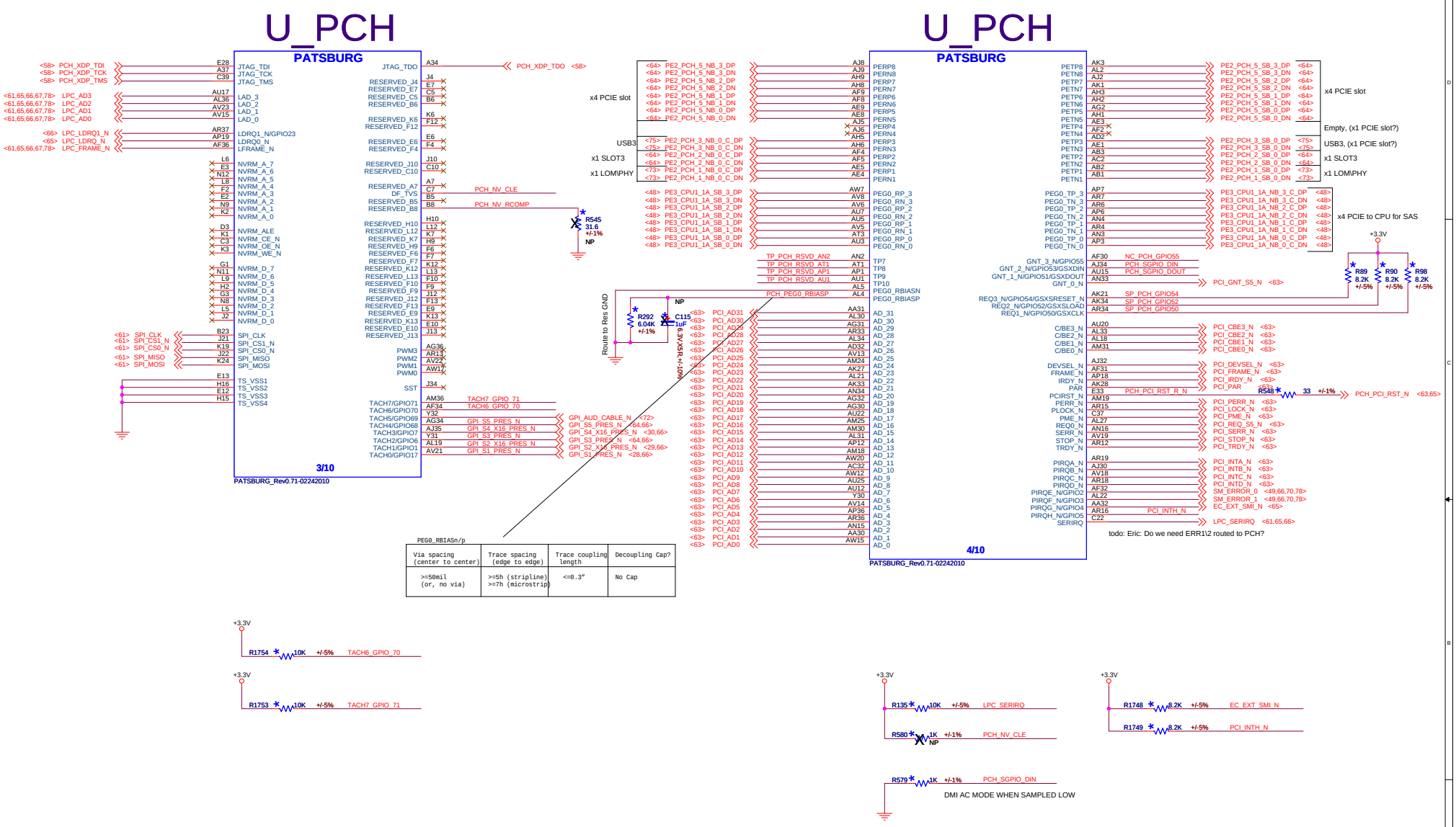
DELL INC.

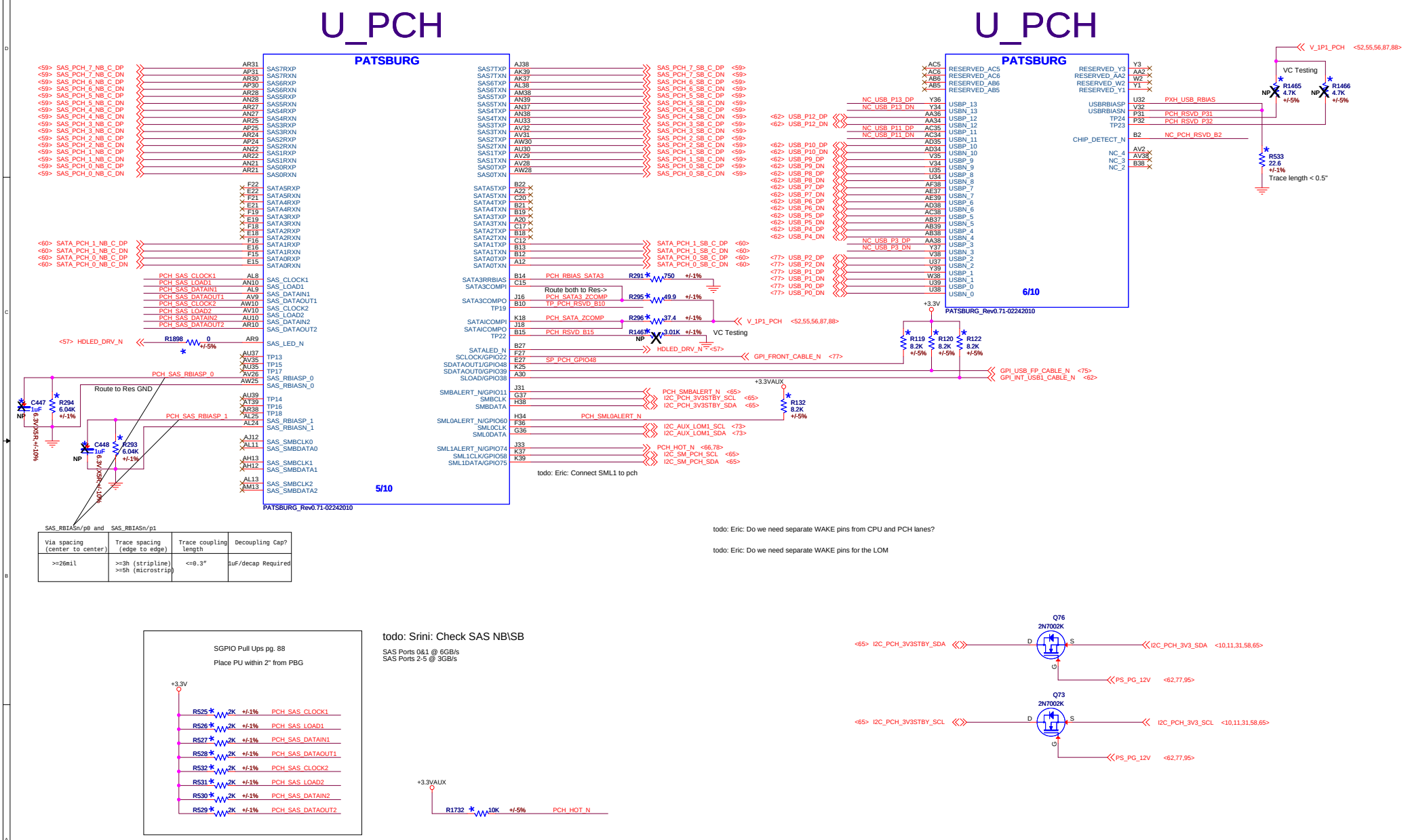
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

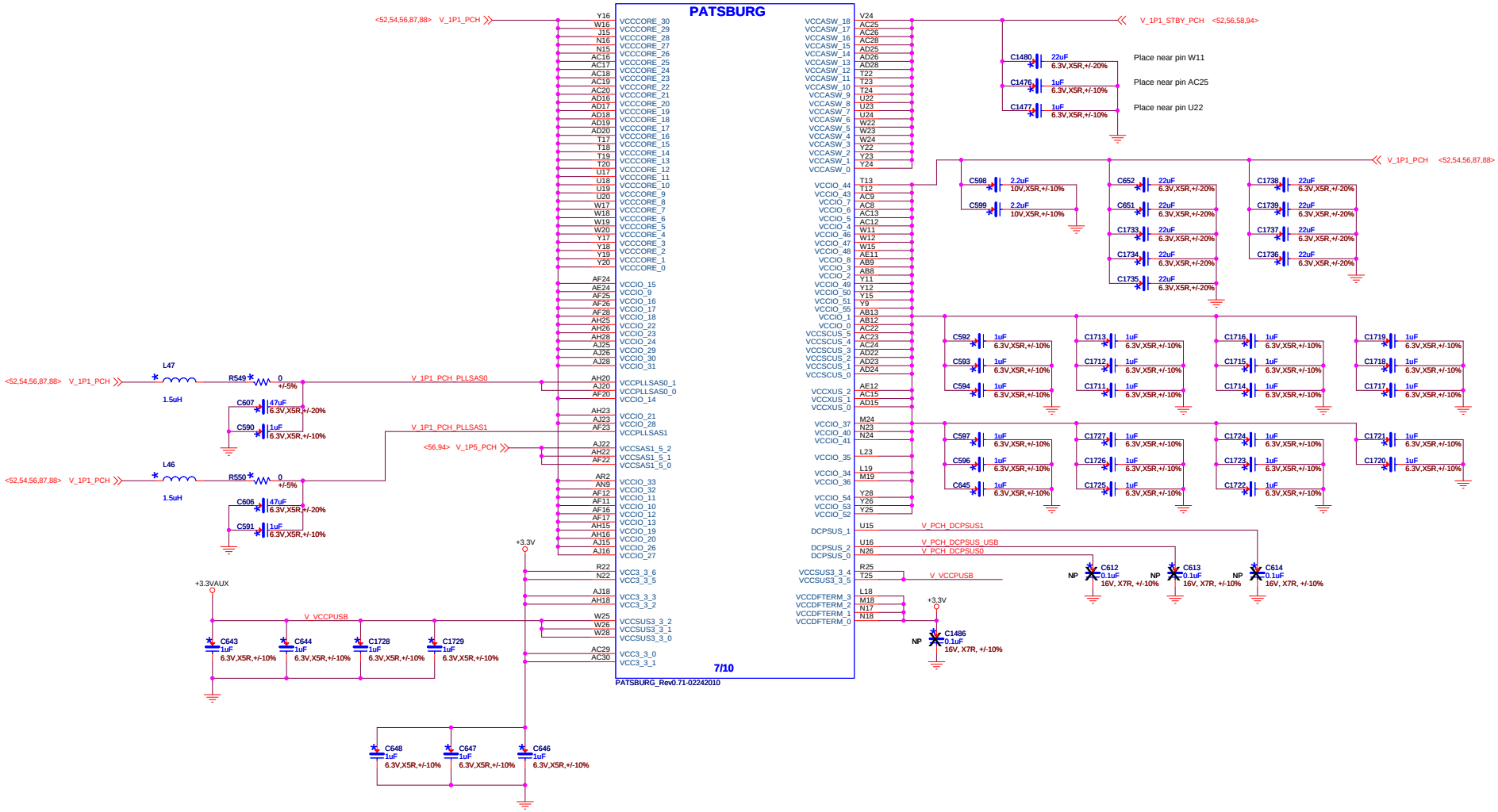
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 52 of 96


U_PCH
PATSBURG
3/10
PATSBURG_Rev0.71-02242010
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
PCH_XDP_TDO
LAD_3
LAD_2
LAD_1
LAD_0
LDRQ1_N/GPIO23
LDRQ0_N
LFRAME_N
NVRM_A_7
NVRM_A_6
NVRM_A_5
NVRM_A_4
NVRM_A_3
NVRM_A_2
NVRM_A_1
NVRM_A_0
NVRM_ALE
NVRM_CE_N
NVRM_OE_N
NVRM_WE_N
NVRM_D_7
NVRM_D_6
NVRM_D_5
NVRM_D_4
NVRM_D_3
NVRM_D_2
NVRM_D_1
NVRM_D_0
SPI_CLK
SPI_CS1_N
SPI_CS0_N
SPI_MISO
SPI_MOSI
TS_VSS1
TS_VSS2
TS_VSS3
TS_VSS4
PCH_NV_CLE
PCH_NV_RCOMP
R545
31.6
+/-1%
NP
TACH7_GPIO_71
TACH6_GPIO_70
GPI_AUD_CABLE_N
GPI_S5_PRES_N
GPI_S4_X16_PRES_N
GPI_S3_PRES_N
GPI_S2_X16_PRES_N
GPI_S1_PRES_N
x4 PCIE slot
USB3
x1 SLOT3
x1 LOM\PHY
PEG0_RBIASP
PEG0_RBIASN
TP_PCH_RSVD_AN2
TP_PCH_RSVD_AT1
TP_PCH_RSVD_AP1
TP_PCH_RSVD_AU1
Route to Res GND
R292
6.04K
+/-1%
C115
1uF
6.3V
X5R
+/-10%
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
PEG0_RBIASn/p
Via spacing (center to center)
>=50mil (or, no via)
Trace spacing (edge to edge)
>=5h (stripline) >=7h (microstrip)
Trace coupling length
<=0.3"
Decoupling Cap?
No Cap
+3.3V
R1754
10K
+/-5%
TACH6_GPIO_70
R1753
TACH7_GPIO_71
BOOT BIOS STRAPS
DEFAULT 1,1: Weak PCH Interal PU
PCH_SGPIO_DOUT
SATA1GP_GPIO19
0 0 LPC
0 1 NAND
1 0 PCI
1 1 SPI
R577
1K
PCH_SGPIO_DOUT <67>
R578
NOA_SATA1GP_GPIO19 <52,58,67>
U_PCH
PATSBURG
4/10
PATSBURG_Rev0.71-02242010
PE2_PCH_5_NB_3_DP
PE2_PCH_5_NB_3_DN
PE2_PCH_5_NB_2_DP
PE2_PCH_5_NB_2_DN
PE2_PCH_5_NB_1_DP
PE2_PCH_5_NB_1_DN
PE2_PCH_5_NB_0_DP
PE2_PCH_5_NB_0_DN
PE2_PCH_3_NB_0_C_DP
PE2_PCH_3_NB_0_C_DN
PE2_PCH_2_NB_0_C_DP
PE2_PCH_2_NB_0_C_DN
PE2_PCH_1_NB_0_C_DP
PE2_PCH_1_NB_0_C_DN
PE3_CPU1_1A_SB_3_DP
PE3_CPU1_1A_SB_3_DN
PE3_CPU1_1A_SB_2_DP
PE3_CPU1_1A_SB_2_DN
PE3_CPU1_1A_SB_1_DP
PE3_CPU1_1A_SB_1_DN
PE3_CPU1_1A_SB_0_DP
PE3_CPU1_1A_SB_0_DN
PE2_PCH_5_SB_3_DP
PE2_PCH_5_SB_3_DN
PE2_PCH_5_SB_2_DP
PE2_PCH_5_SB_2_DN
PE2_PCH_5_SB_1_DP
PE2_PCH_5_SB_1_DN
PE2_PCH_5_SB_0_DP
PE2_PCH_5_SB_0_DN
PE2_PCH_3_SB_0_DP
PE2_PCH_3_SB_0_DN
PE2_PCH_2_SB_0_DP
PE2_PCH_2_SB_0_DN
PE2_PCH_1_SB_0_DP
PE2_PCH_1_SB_0_DN
PE3_CPU1_1A_NB_3_C_DP
PE3_CPU1_1A_NB_3_C_DN
PE3_CPU1_1A_NB_2_C_DP
PE3_CPU1_1A_NB_2_C_DN
PE3_CPU1_1A_NB_1_C_DP
PE3_CPU1_1A_NB_1_C_DN
PE3_CPU1_1A_NB_0_C_DP
PE3_CPU1_1A_NB_0_C_DN
x4 PCIE slot
Empty, (x1 PCIE slot?)
USB3, (x1 PCIE slot?)
x1 SLOT3
x1 LOM\PHY
x4 PCIE to CPU for SAS
+3.3V
R89
R90
R98
8.2K
+/-5%
GNT_3_N/GPIO55
GNT_2_N/GPIO53/GSXDIN
GNT_1_N/GPIO51/GSXDOUT
GNT_0_N
PCI_GNT_S5_N <63>
REQ3_N/GPIO54/GSXSRESET_N
REQ2_N/GPIO52/GSXSLOAD
REQ1_N/GPIO50/GSXCLK
SP_PCH_GPIO54
SP_PCH_GPIO52
SP_PCH_GPIO50
NC_PCH_GPIO55
PCH_SGPIO_DIN
PCH_SGPIO_DOUT
C/BE3_N
C/BE2_N
C/BE1_N
C/BE0_N
DEVSEL_N
FRAME_N
IRDY_N
PAR
PCIRST_N
PERR_N
PLOCK_N
PME_N
REQ0_N
SERR_N
STOP_N
TRDY_N
PIRQA_N
PIRQB_N
PIRQC_N
PIRQD_N
PIRQE_N/GPIO2
PIRQF_N/GPIO3
PIRQG_N/GPIO4
PIRQH_N/GPIO5
SERIRQ
PCI_CBE3_N
PCI_CBE2_N
PCI_CBE1_N
PCI_CBE0_N
PCI_DEVSEL_N
PCI_FRAME_N
PCI_IRDY_N
PCI_PAR
PCH_PCI_RST_R_N
R548
33
+/-1%
PCH_PCI_RST_N <63,65>
PCI_PERR_N
PCI_LOCK_N
PCI_PME_N
PCI_REQ_S5_N
PCI_SERR_N
PCI_STOP_N
PCI_TRDY_N
PCI_INTA_N
PCI_INTB_N
PCI_INTC_N
PCI_INTD_N
SM_ERROR_0 <49,66,70,78>
SM_ERROR_1 <49,66,70,78>
EC_EXT_SMI_N <65>
PCI_INTH_N
LPC_SERIRQ <61,65,66>
todo: Eric: Do we need ERR1\2 routed to PCH?
R135
10K
+/-5%
LPC_SERIRQ
R580
1K
+/-1%
PCH_NV_CLE
R579
PCH_SGPIO_DIN
DMI AC MODE WHEN SAMPLED LOW
R1748
8.2K
EC_EXT_SMI_N
R1749
PCI_INTH_N
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 53 of 96


U_PCH
PATSBURG
5/10
PATSBURG_Rev0.71-02242010
U_PCH
PATSBURG
6/10
PATSBURG_Rev0.71-02242010
SAS_RBIASN/p0 and SAS_RBIASn/p1
Via spacing (center to center)
Trace spacing (edge to edge)
Trace coupling length
Decoupling Cap?
>=26mil
>=3h (stripline) >=5h (microstrip)
<=0.3"
1uF/decap Required
Route to Res GND
Route both to Res->
VC Testing
Trace length < 0.5"
todo: Eric: Connect SML1 to pch
todo: Eric: Do we need separate WAKE pins from CPU and PCH lanes?
todo: Eric: Do we need separate WAKE pins for the LOM
SGPIO Pull Ups pg. 88
Place PU within 2" from PBG
todo: Srini: Check SAS NB\SB
SAS Ports 0&1 @ 6GB/s
SAS Ports 2-5 @ 3GB/s
2N7002K
INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 54 of 96

U_PCH



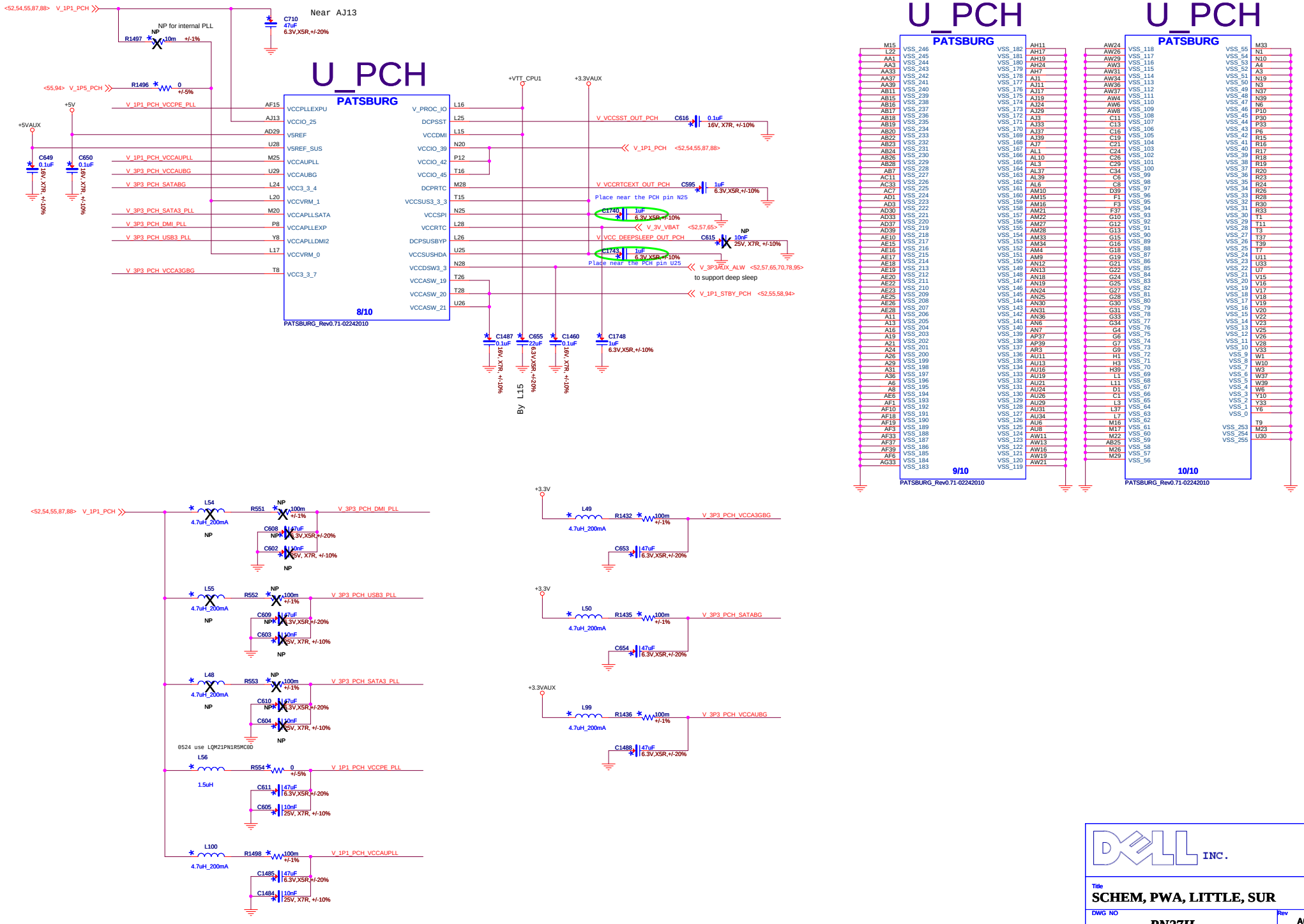
DELL INC.

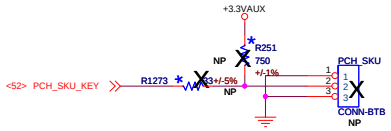
Title
SCHEM, PWA, LITTLE, SUR

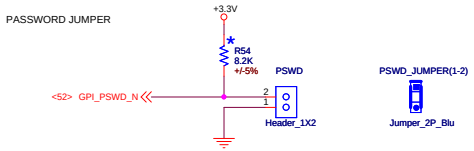
DWG NO
PN27H

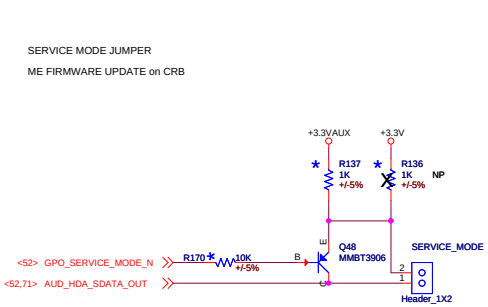
Rev
A01

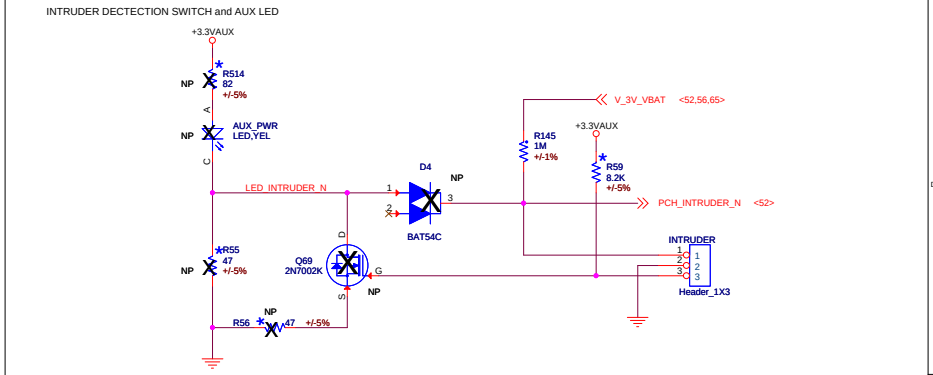
Date: Wednesday, June 20, 2012 Sheet 55 of 96

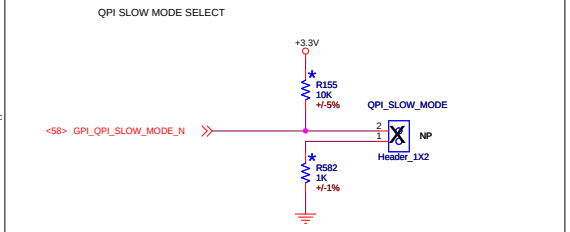

U_PCH
PATSBURG
8/10
PATSBURG_Rev0.71-02242010
Near AJ13
NP for internal PLL
By L15
U_PCH
PATSBURG
9/10
PATSBURG_Rev0.71-02242010
U_PCH
PATSBURG
10/10
PATSBURG_Rev0.71-02242010
0524 use LQM21PN1R5MC0D
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 56 of 96

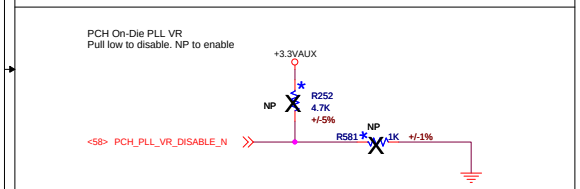


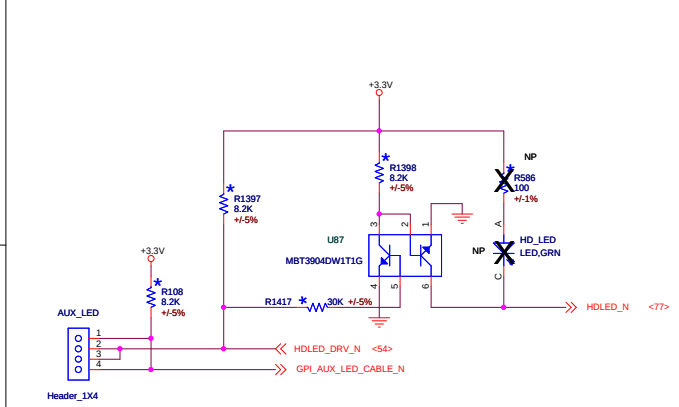


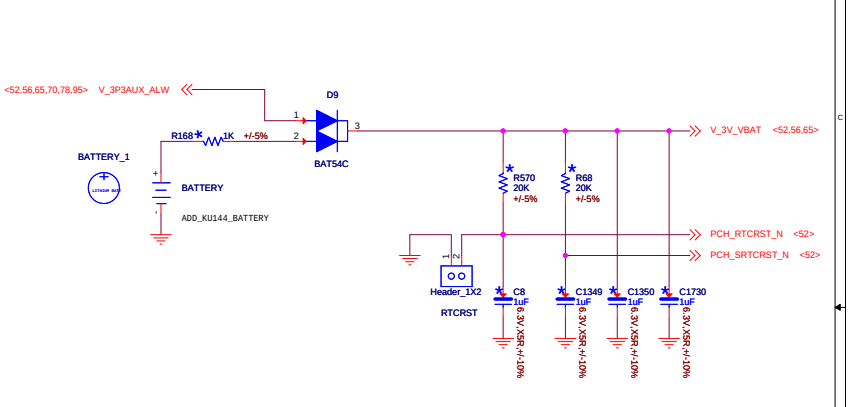


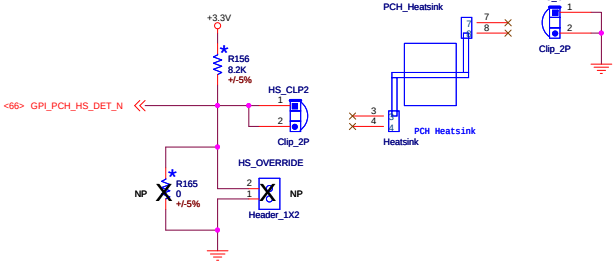


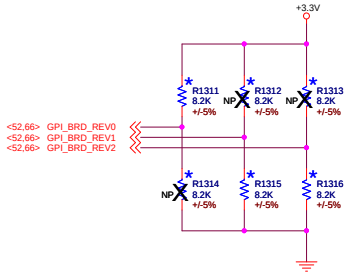




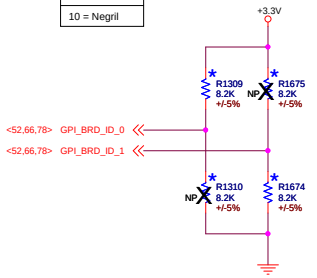




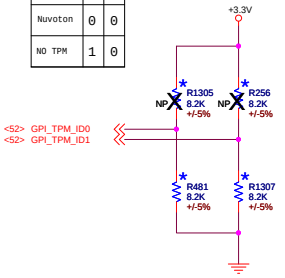




00 = Big Sur
01 = Little Sur
10 = Negril



Vendor	ID	
	0	1
Nuvoton	0	0
NO TPM	1	0



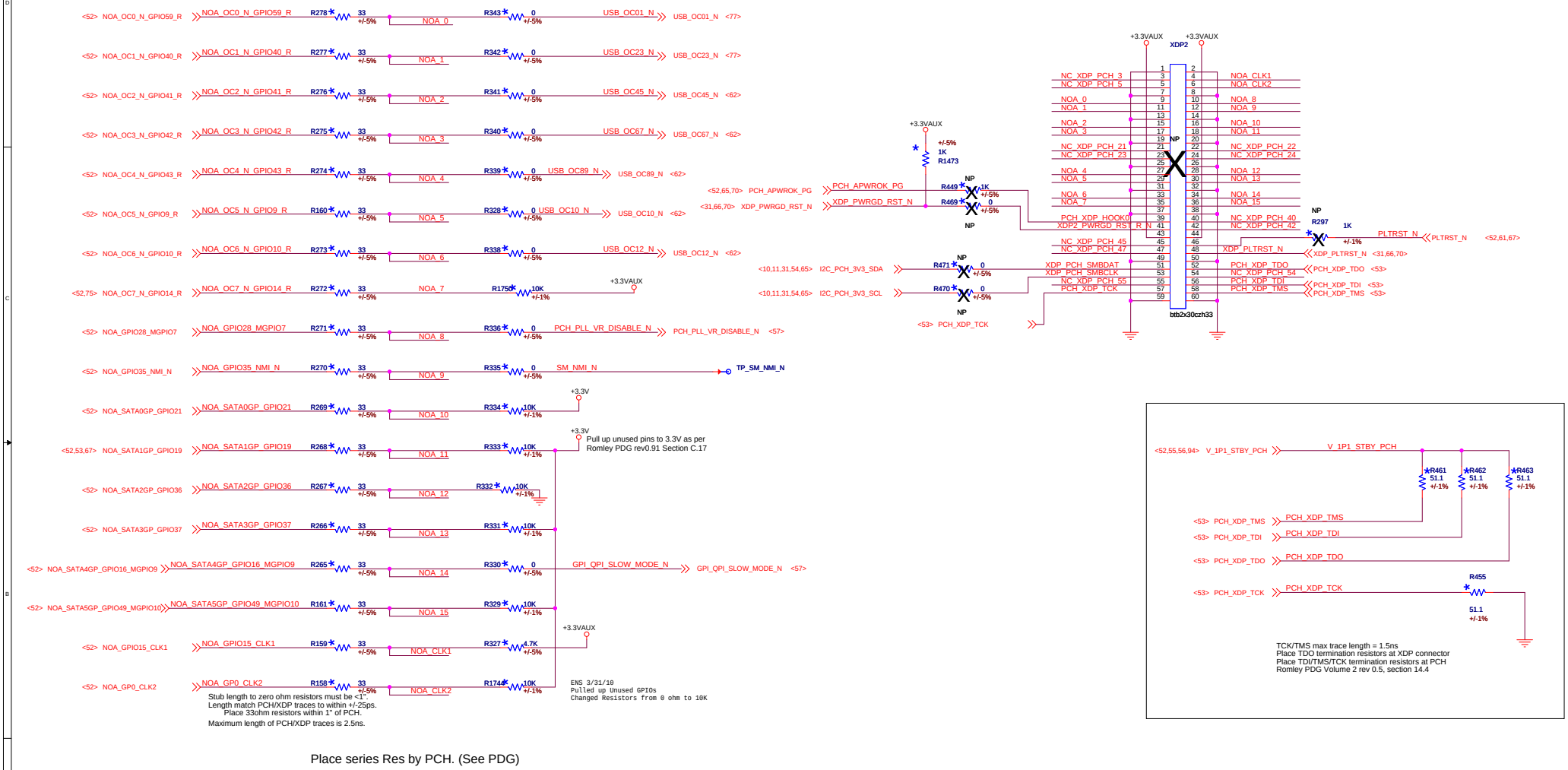
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 57 of 96



Place series Res by PCH. (See PDG)

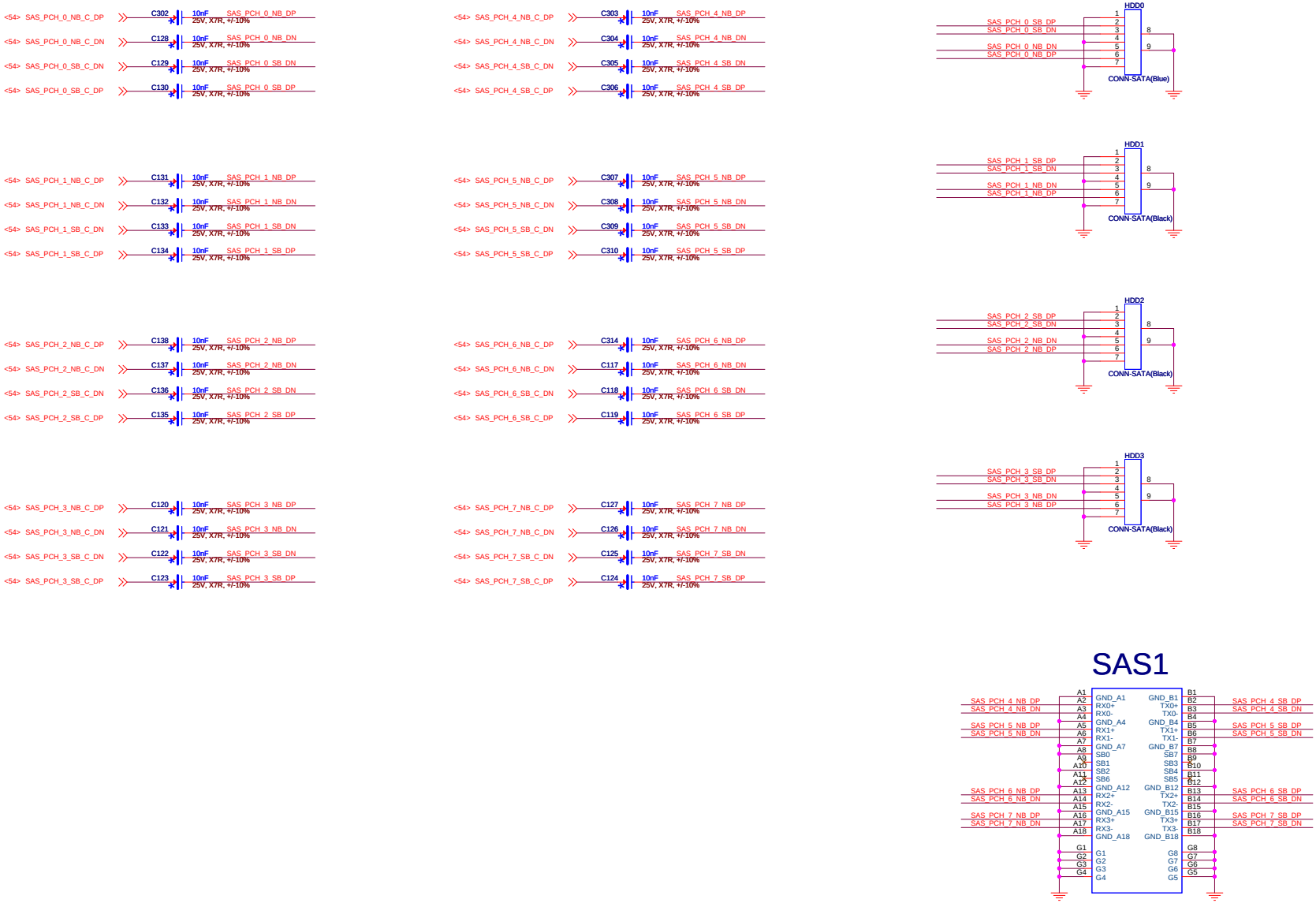
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 58 of 96



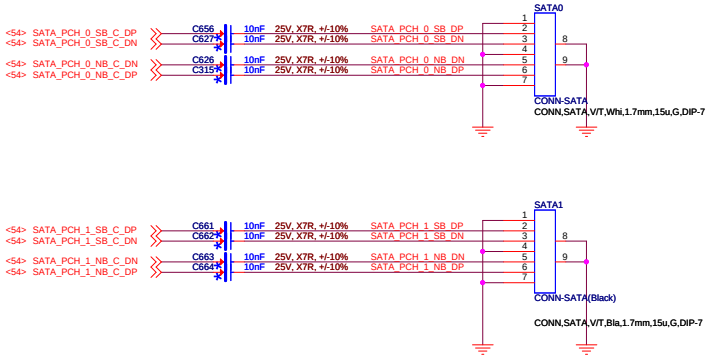
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 59 of 96



SATA 6G connector
LE18077-A50D-4F
LE18077-W50D-4F
LE18077-Z50D-4F

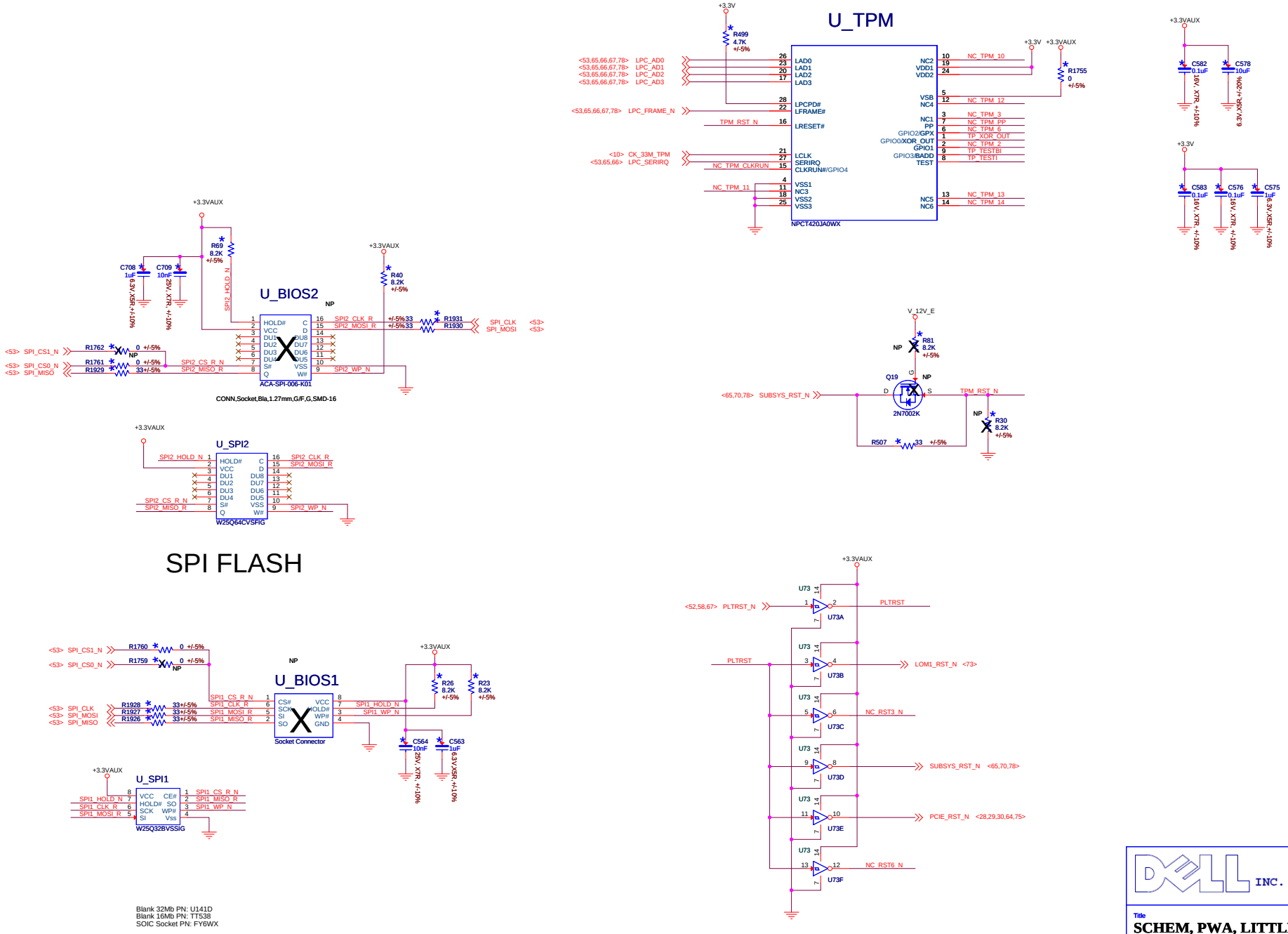
DELL INC.

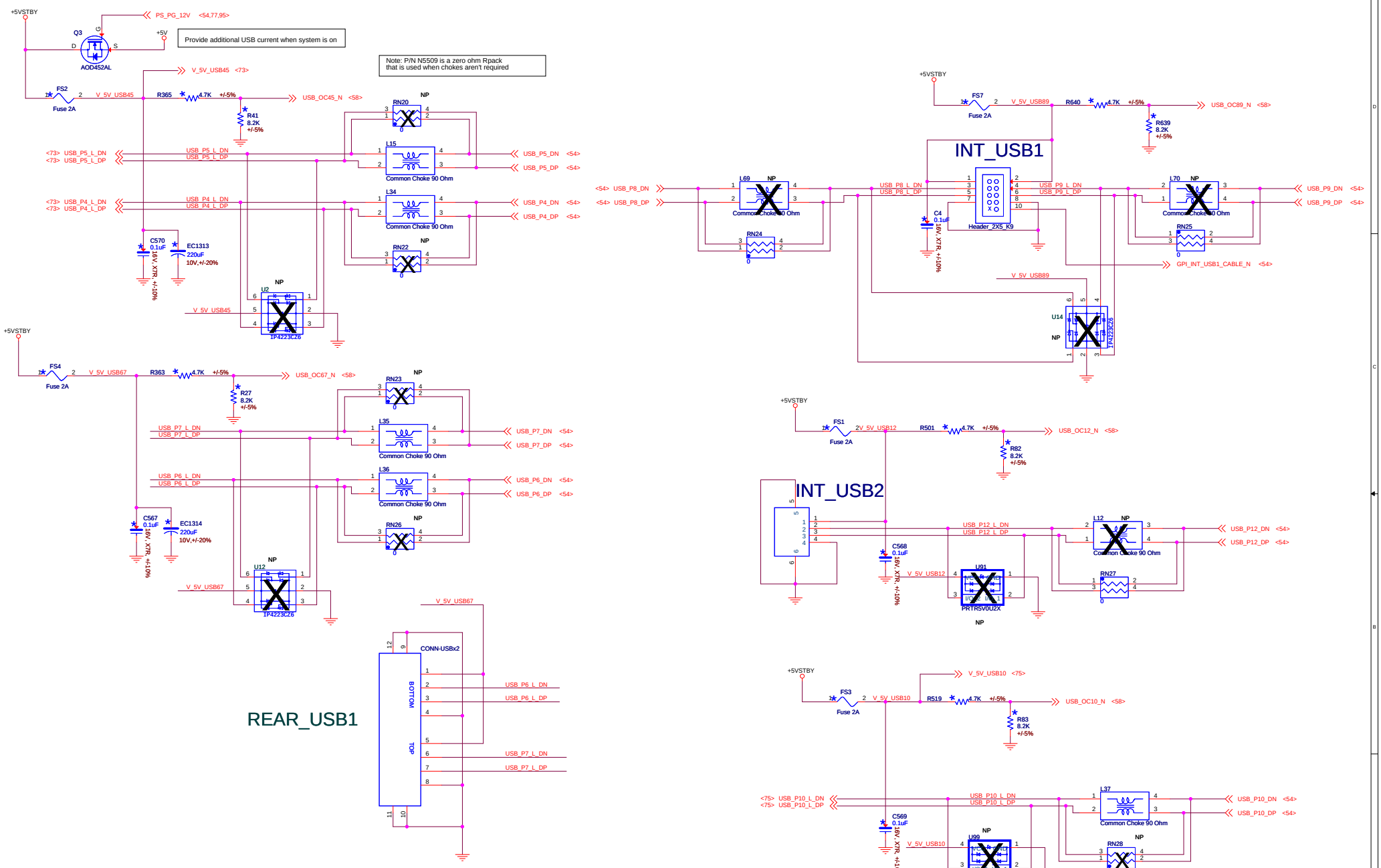
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 60 of 96


U_TPM
NPCT420JA0WX
U_BIOS2
ACA-SPI-006-K01
CONN,Socket,Bla,1.27mm,G/F,G,SMD-16
U_SPI2
W25Q64CVSFIG
SPI FLASH
U_BIOS1
Socket Connector
U_SPI1
W25Q32BVSSIG
Blank 32Mb PN: U141D
Blank 16Mb PN: TT538
SOIC Socket PN: FY6WX
INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 61 of 96

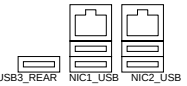


USB PORTS TABLE

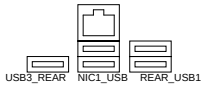
Port	Location
0 - 3	Front USB (pg77)
4 - 5	Rear NIC1_USB x2
6 - 7	Rear NIC2_USB x2 (BigSur) Rear_USB1 x2 (LittleSur)
8 - 9	INT_USB1 (Flexbay)
10	USB3_REAR
12	INT_USB2 (Internal USB)

Ports 1 and 9 are USB debug ports

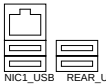
BIGSUR REAR USB PORTS



LITTLESUR REAR USB PORTS



NEGRIL REAR USB PORTS



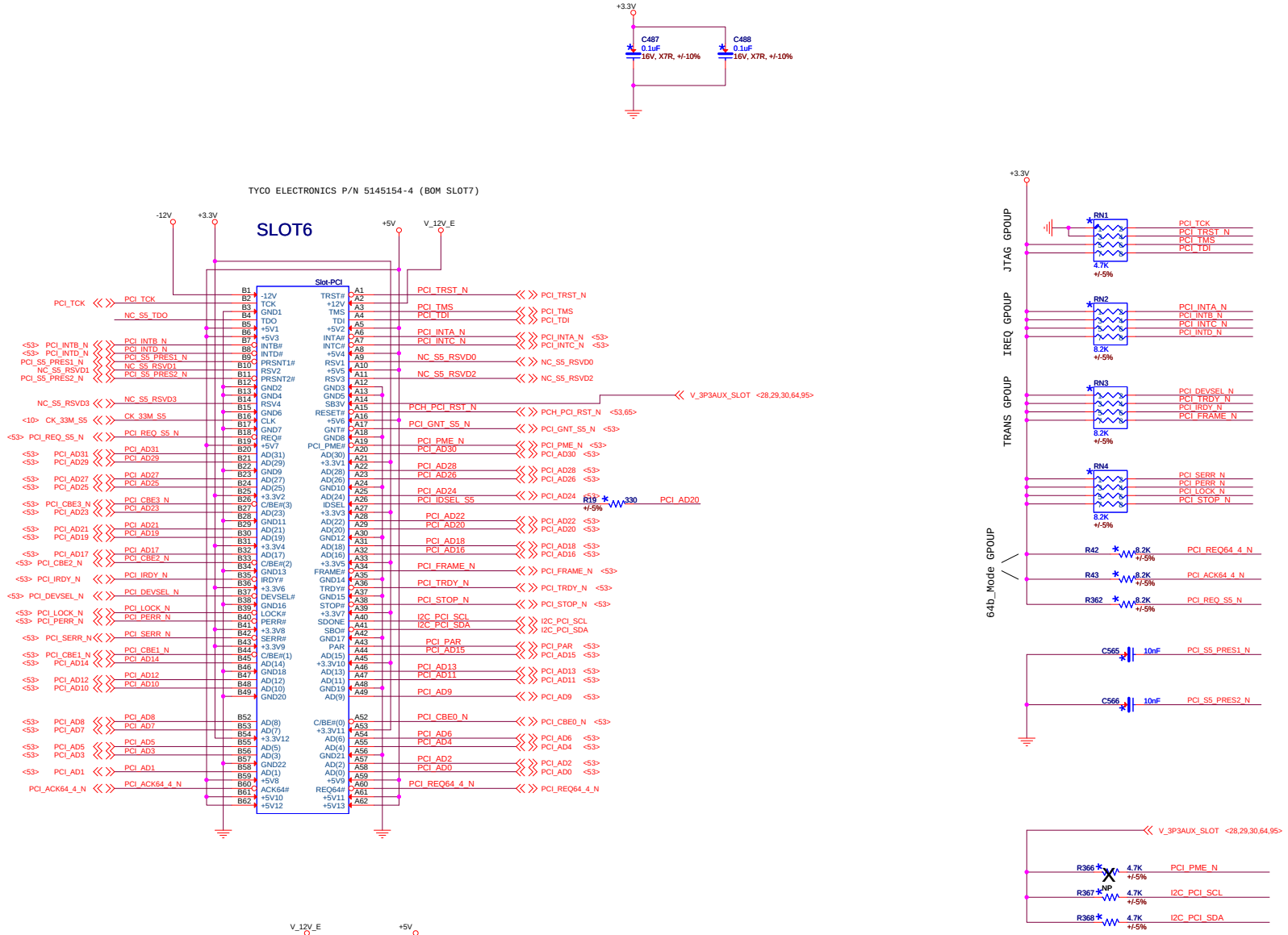
DELL INC.

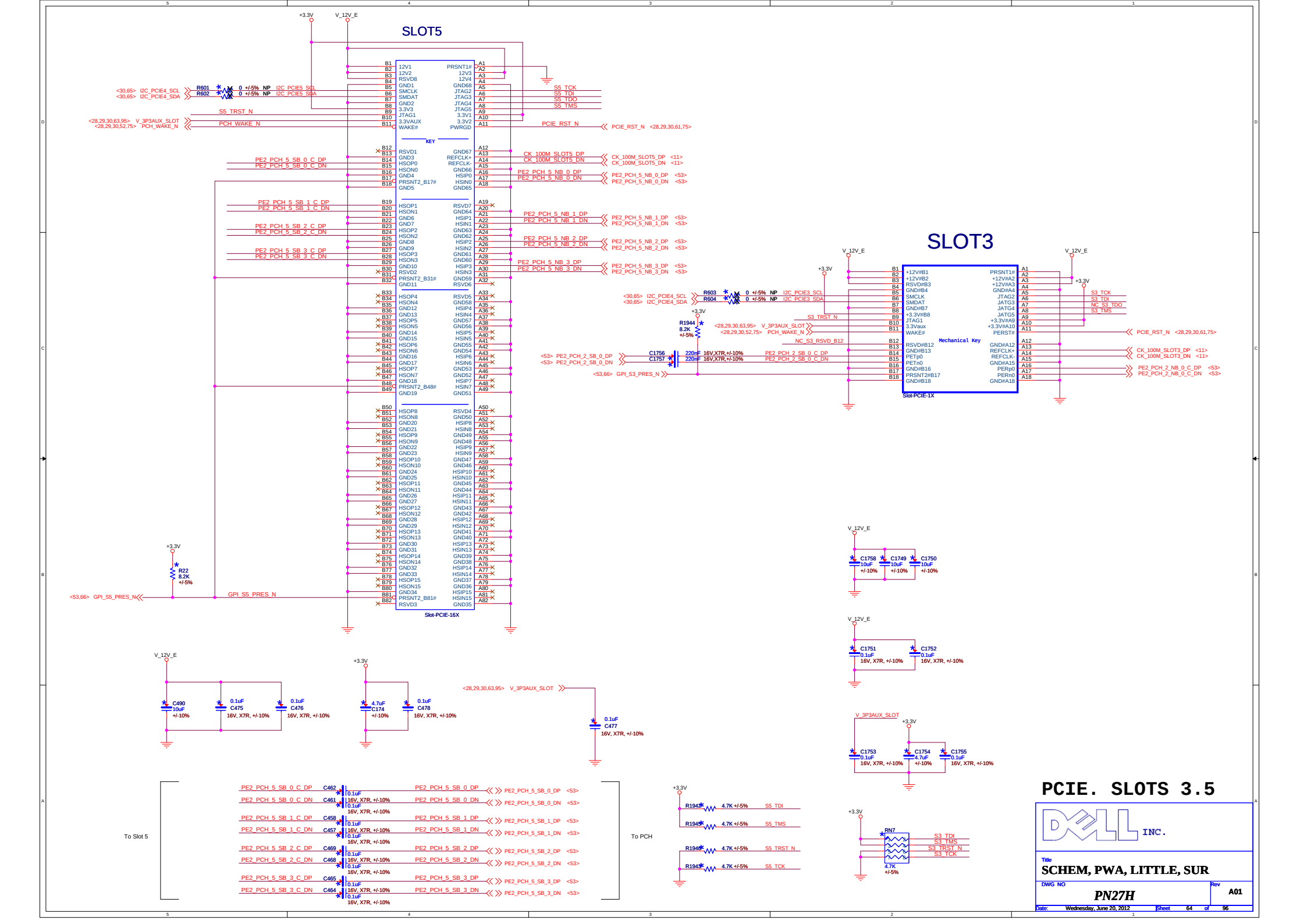
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 62 of 96


TYCO ELECTRONICS P/N 5145154-4 (BOM SLOT7)
SLOT6
Slot-PCI
JTAG GPOUP
IREQ GPOUP
TRANS GPOUP
64b_Mode GPOUP
PCI32 SLOT
DELL INC.
SCHEM, PWA, LITTLE, SUR
PN27H
A01
Wednesday, June 20, 2012
63 of 96


SLOT5
SLOT3
Slot-PCIE-16X
Slot-PCIE-1X
Mechanical Key
KEY
PCIE. SLOTS 3.5
DELL INC.
SCHEM, PWA, LITTLE, SUR
PN27H
A01
Wednesday, June 20, 2012
64 of 96
To Slot 5
To PCH

Change PCH SMBus to SML1 instead of SML0

U_EC

MEC5055-LZY-SUR01_A

PS/2 INTERFACE
JTAG INTERFACE
FAN PWM & TACH
BC-LINK
HOST INTERFACE
MASTER CLOCK
MISC INTERFACE
GENERAL PURPOSE I/O
SMBUS INTERFACE
DELL PWR SW INF

Place close to the pin A11,A22,B35,A41,A58,A52,B3,A26

For SMbus overshoot undershoot reserved

EMBEDDED SM CONTROLLER

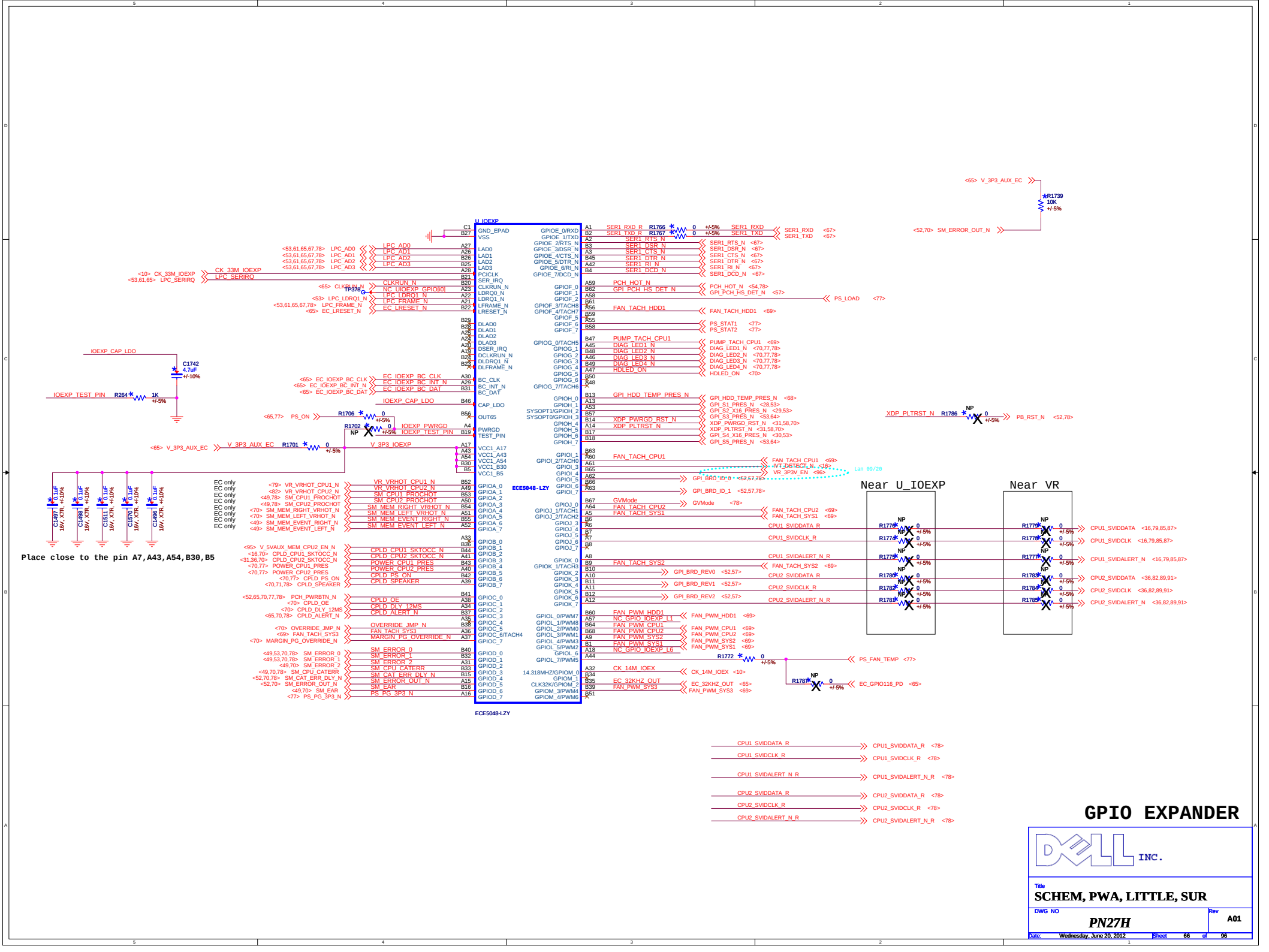
DELL INC.

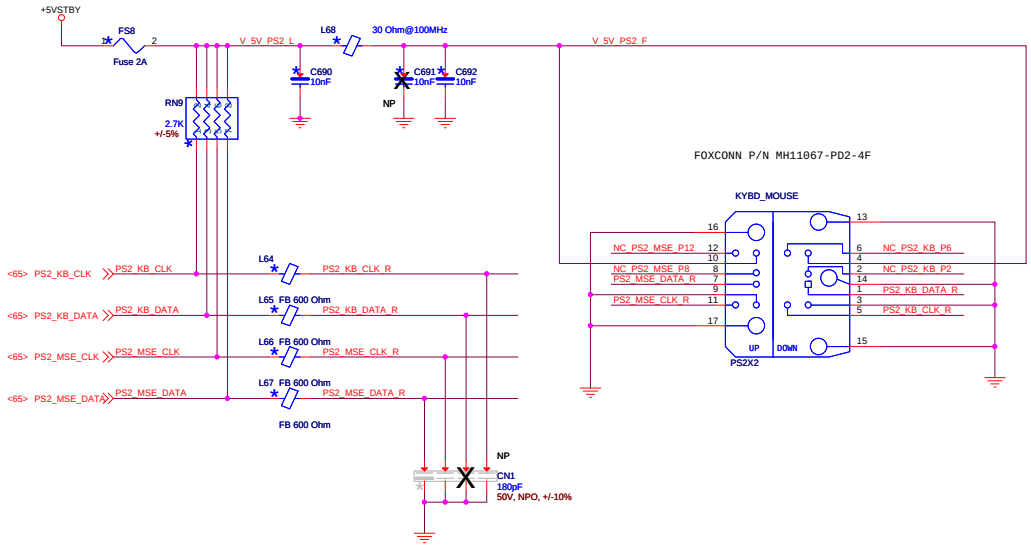
Title: SCHEM, PWA, LITTLE, SUR

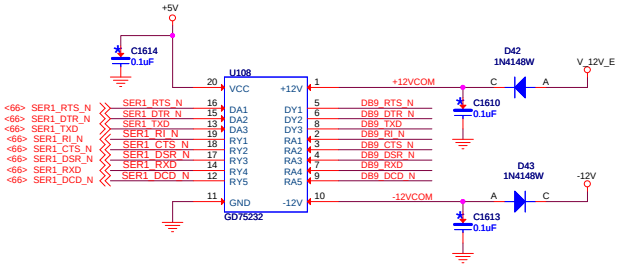
DWG NO: PN27H

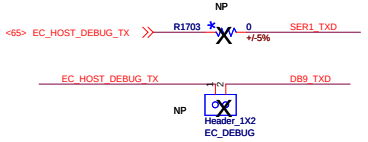
Rev: A01

Date: Wednesday, June 20, 2012 Sheet 65 of 96

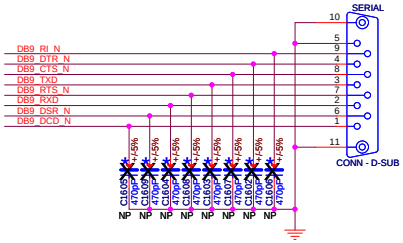

U_IOEXP
ECE5048-LZY
GPIO EXPANDER
Near U_IOEXP
Near VR
Place close to the pin A7,A43,A54,B30,B5
SCHEM, PWA, LITTLE, SUR
PN27H
A01
Wednesday, June 20, 2012





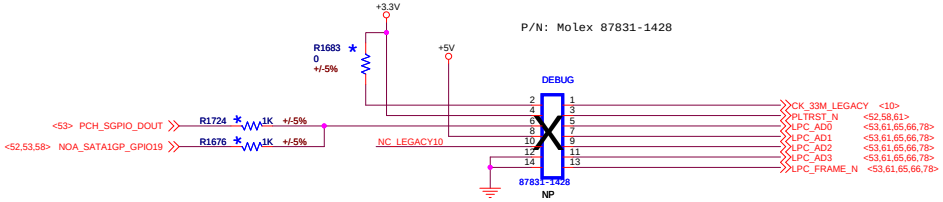


P/N: Foxconn DT10127-82N3-4F



LEGACY IO Connector

see BigSur pg53 for boot bios strapping options
also acts as LPC Debug connector
populate



KYBD\MOUSE,SERIAL

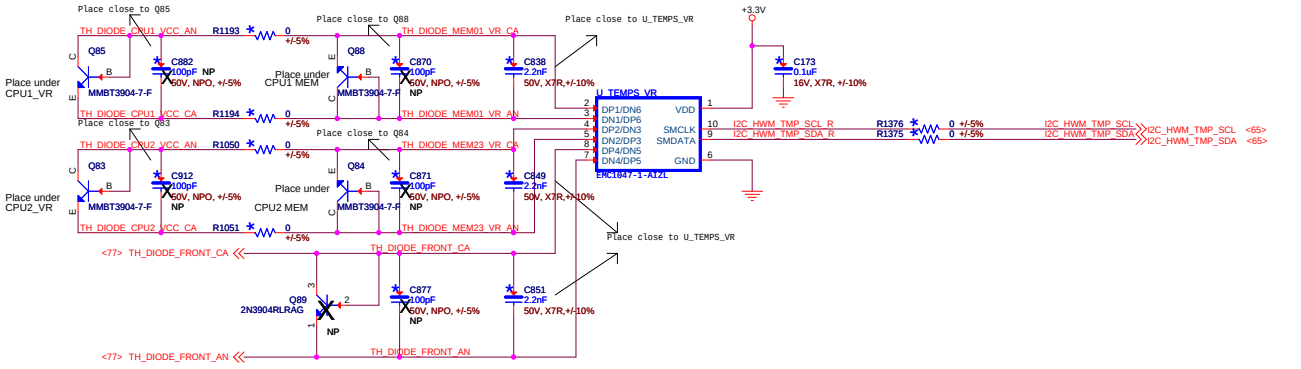
DELL INC.

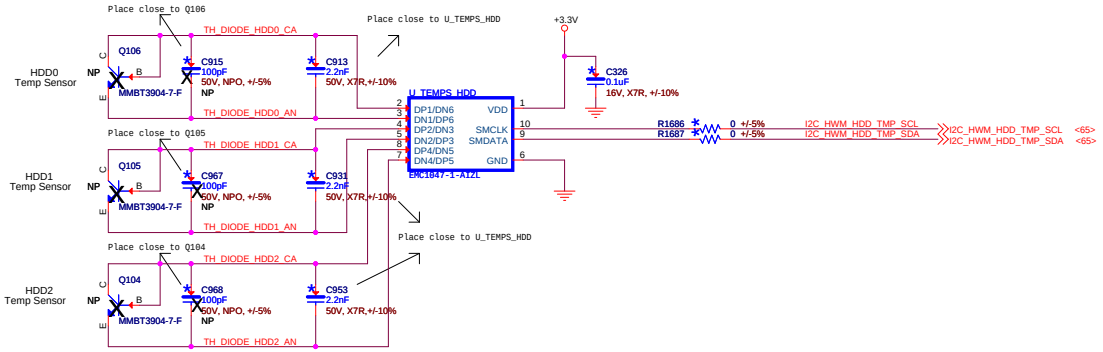
Title
SCHEM, PWA, LITTLE, SUR

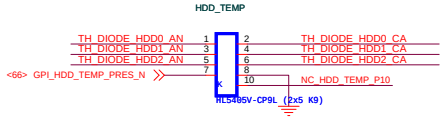
DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 67 of 96







34064WH00-600-G

HW MONITOR

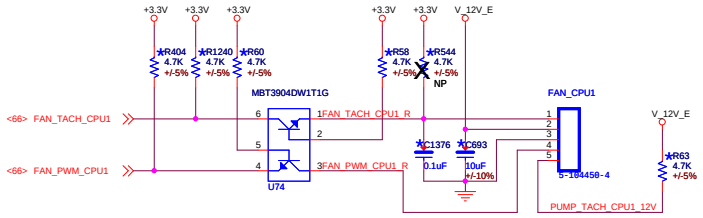
DELL INC.

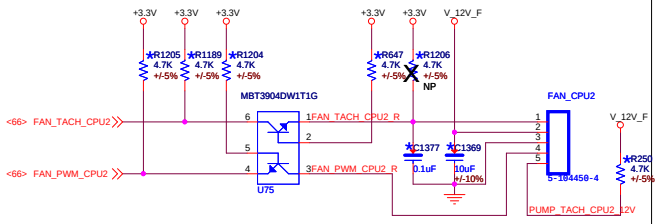
Title
SCHEM, PWA, LITTLE, SUR

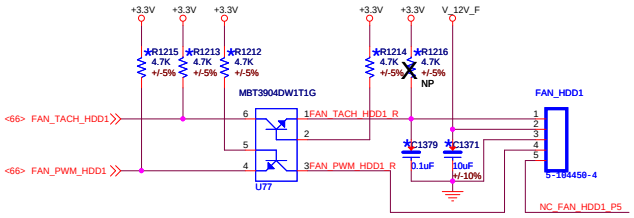
DWG NO
PN27H

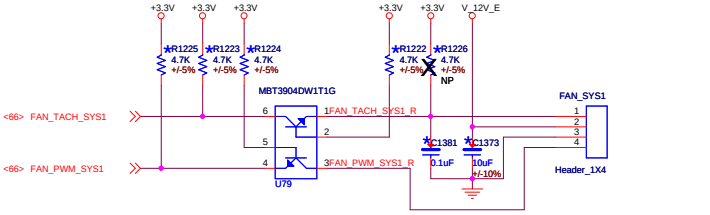
Rev
A01

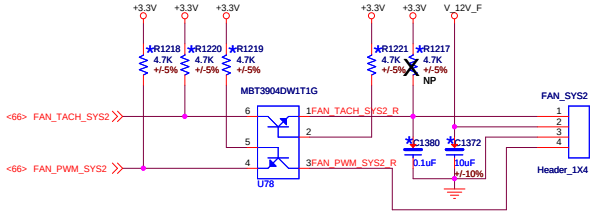
Date: Wednesday, June 20, 2012 Sheet 68 of 96

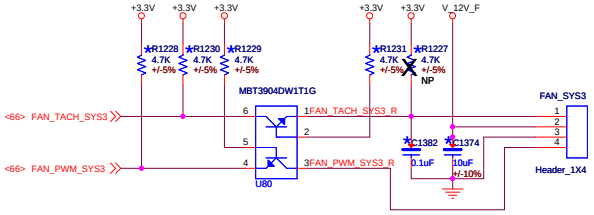






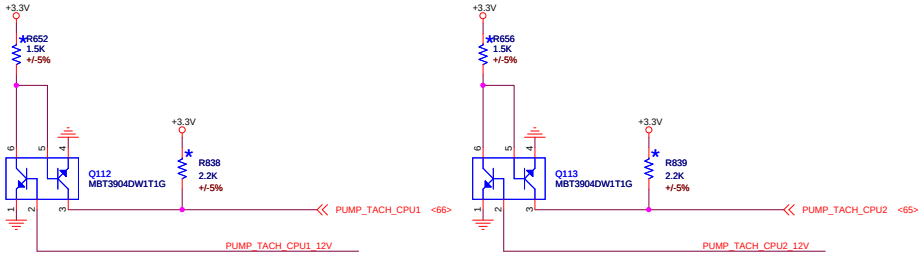






Fan Matrix

	5048 PWM/TACH 0	5048 PWM/TACH 1	5048 PWM/TACH 2	5048 PWM/TACH 3	5048 PWM/TACH 4	5048 PWM/TACH 6
Little Sur	CPU1 Fan	CPU2 Fan	SYS1 FAN	SYS2 FAN	SYS3 FAN	HDD1 FAN



FAN CONNECTOR

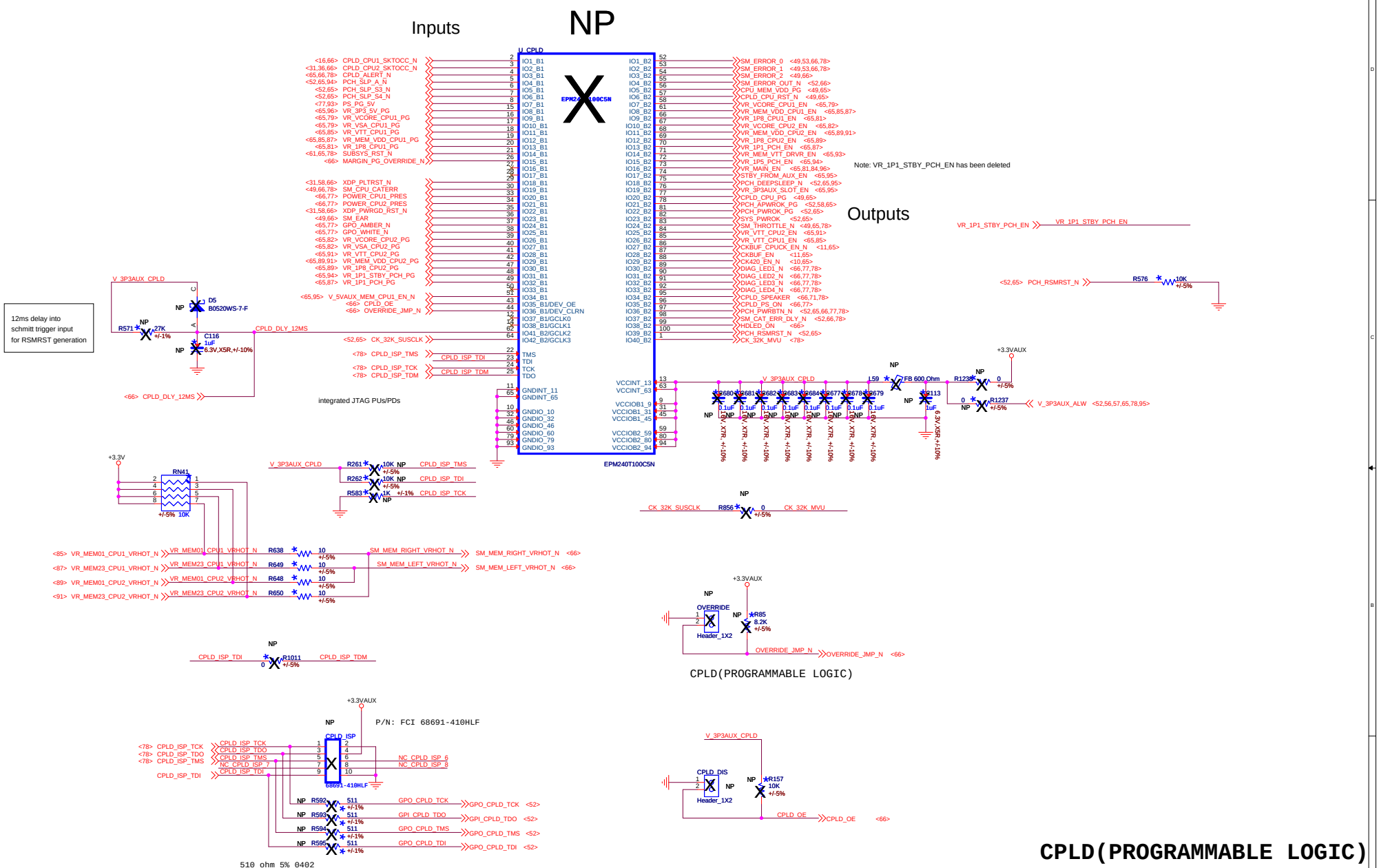
DELL INC.

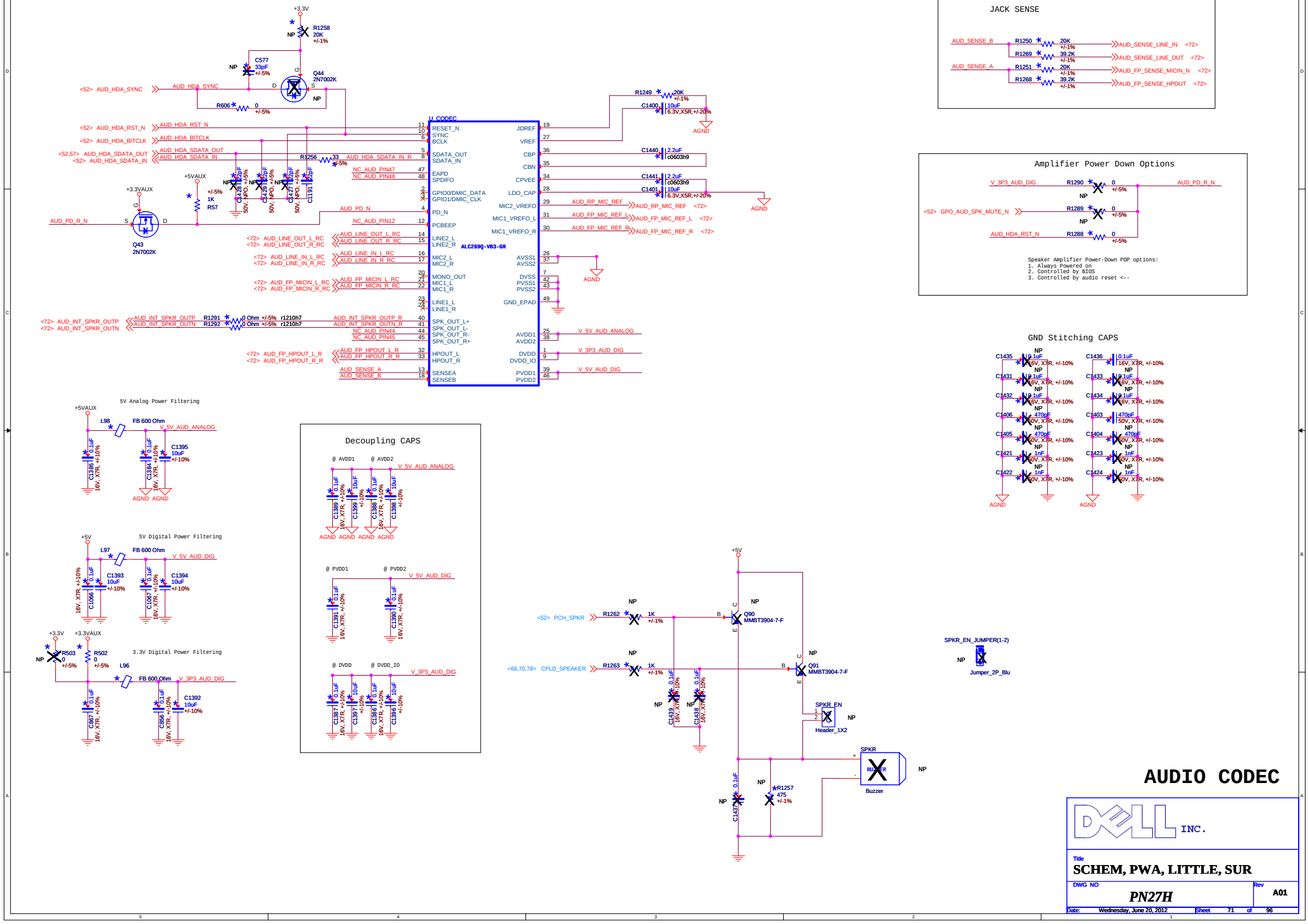
Title
SCHEM, PWA, LITTLE, SUR

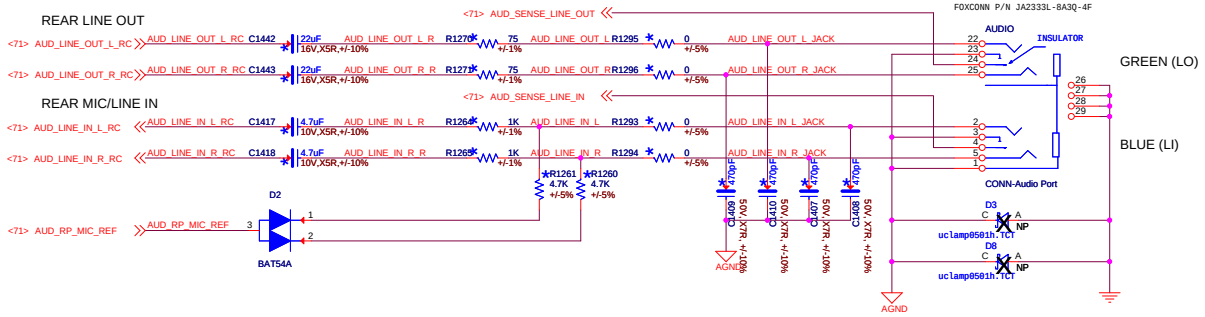
DWG NO
PN27H

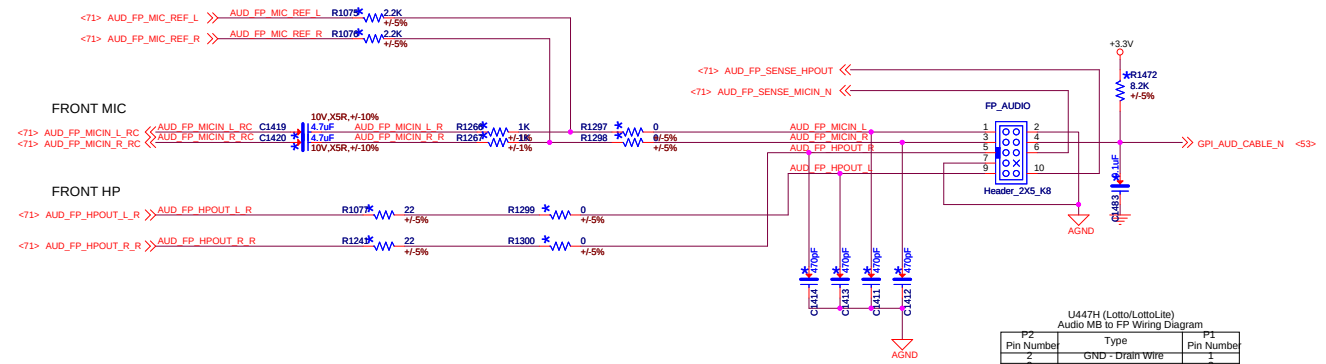
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 69 of 96


Inputs
NP
U_CPLD
EPM240T100C5N
Outputs
Note: VR_1P1_STBY_PCH_EN has been deleted
12ms delay into schmitt trigger input for RSMRST generation
integrated JTAG PUs/PDs
CPLD(PROGRAMMABLE LOGIC)
P/N: FCI 68691-410HLF
510 ohm 5% 0402
CPLD(PROGRAMMABLE LOGIC)
SCHEM, PWA, LITTLE, SUR
PN27H
A01
Wednesday, June 20, 2012
70
96

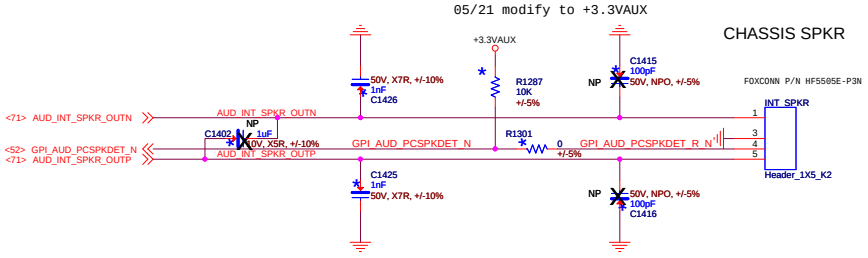

JACK SENSE
AUD_SENSE_B
R1250 20K +/-1%
R1269 39.2K +/-1%
AUD_SENSE_LINE_IN <72>
AUD_SENSE_LINE_OUT <72>
AUD_SENSE_A
R1251 20K +/-1%
R1268 39.2K +/-1%
AUD_FP_SENSE_MICIN_N <72>
AUD_FP_SENSE_HPOUT <72>
Amplifier Power Down Options
V_3P3_AUD_DIG
R1290 0 +/-5% NP
AUD_PD_R_N
<52> GPO_AUD_SPK_MUTE_N
R1289 0 +/-5% NP
AUD_HDA_RST_N
R1288 0 +/-5%
Speaker Amplifier Power-Down POP options:
1. Always Powered on
2. Controlled by BIOS
3. Controlled by audio reset <--
GND Stitching CAPS
Decoupling CAPS
5V Analog Power Filtering
5V Digital Power Filtering
3.3V Digital Power Filtering
U_CODEC
ALC269Q-VB3-GR
RESET_N
SYNC
BCLK
SDATA_OUT
SDATA_IN
EAPD
SPDIFO
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD_N
PCBEEP
LINE2_L
LINE2_R
MIC2_L
MIC2_R
MONO_OUT
MIC1_L
MIC1_R
LINE1_L
LINE1_R
SPK_OUT_L+
SPK_OUT_L-
SPK_OUT_R-
SPK_OUT_R+
HPOUT_L
HPOUT_R
SENSEA
SENSEB
JDREF
VREF
CBP
CBN
CPVEE
LDO_CAP
MIC2_VREFO
MIC1_VREFO_L
MIC1_VREFO_R
AVSS1
AVSS2
DVSS
PVSS1
PVSS2
GND_EPAD
AVDD1
AVDD2
DVDD
DVDD_IO
PVDD1
PVDD2
Q43 2N7002K
Q44 2N7002K
Q90 MMBT3904-7-F
Q91 MMBT3904-7-F
SPKR_EN_JUMPER(1-2)
Jumper_2P_Blu
SPKR_EN
Header_1X2
SPKR
Buzzer
AUDIO CODEC
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 71 of 96





U447H (Lotto/LottoLite)
Audio MB to FP Wiring Diagram

P2 Pin Number	Type	P1 Pin Number
2	GND - Drain Wire	1
9	Twisted Pair	2
10		3
5	Twisted Pair	4
7		5
1	Twisted Pair	6
7		7
3	Twisted Pair	8
6		9
4	Cable Detect	10



AUDIO FILTER AND CONNS

DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 72 of 96

LOM1_ACTLED_N R397 330 +/-5% LOM1_ACTLED_R_N

<77> LOM1_LINK_10/1000_N LOM1_LINK_10/1000_N R398 330 +/-5% LOM1_LED_GRN_N

<77> LOM1_LINK_100/1000_N LOM1_LINK_100/1000_N R399 330 +/-5% LOM1_LED_ORG_N

LOM1 LED Current limiting resistors
adjust resistors for LED brightness

<53> PE2_PCH_1_NB_0_C_DP C523 0.1uF PE2_PCH_1_NB_0_DP

<53> PE2_PCH_1_NB_0_C_DN C524 0.1uF PE2_PCH_1_NB_0_DN

<53> PE2_PCH_1_SB_0_DP C526 0.1uF PE2_PCH_1_SB_0_C_DP

<53> PE2_PCH_1_SB_0_DN C525 0.1uF PE2_PCH_1_SB_0_C_DN

To LOM1

[0412] Add 4.7k PU on nets
I2C_AUX_LOM1_SCL/SDA

+3.3VAUX_LOM

R1741 2.2K +/-5%

R1740 2.2K +/-5%

<54> I2C_AUX_LOM1_SCL

<54> I2C_AUX_LOM1_SDA

+3.3VAUX_LOM

R409 3.01K +/-1%

R410 3.01K +/-1%

R459 10K +/-1%

V_1P0_LOM1_CORE_VDD L11 4.7uH

C517 0.1uF 16V, X7R, +/-10%

C508 22uF 6.3V,X5R,+/-20%

LOM1_LAN_DISABLE_N

U_LOM1

82579LM

CLKREQ_N
CTRL10
GPIO_0
GPIO_1
LAN_DISABLE_N
MDI_N0
MDI_N1
MDI_N2
MDI_N3
MDI_P0
MDI_P1
MDI_P2
MDI_P3
PE_CLK_N
PE_CLK_P
PE_RN
PE_RP
PE_RST_N
RBIAS
SMB_CLK
SMB_DATA
LED_0
LED_1
LED_2
PE_TN
PE_TP
TCK
TDI
TDO
TEST_ENABLE
TMS
XTLI
XTLO
COREVDD_11
COREVDD_16
COREVDD_22
COREVDD_37
COREVDD_40
COREVDD_43
COREVDD_46
COREVDD_47
COREVDD_8
INVDD_15
INVDD_19
INVDD_29
OUTVDD
VDD3P3
RSVD_NC
EPAD_GND

ETH_LOM1_0_DN
ETH_LOM1_1_DN
ETH_LOM1_2_DN
ETH_LOM1_3_DN
ETH_LOM1_0_DP
ETH_LOM1_1_DP
ETH_LOM1_2_DP
ETH_LOM1_3_DP

<11> CK_100M_LOM1_DN
<11> CK_100M_LOM1_DP
PE2_PCH_1_SB_0_C_DN
PE2_PCH_1_SB_0_C_DP

<61> LOM1_RST_N R1920 0 +/-5%

<54> I2C_AUX_LOM1_SCL
<54> I2C_AUX_LOM1_SDA

R408 3.01K +/-1%

todo: Vaibhav: Add 4.7k PU to SMBus

LOM1_ACTLED_N
LOM1_LINK_100/1000_N
LOM1_LINK_10/1000_N
PE2_PCH_1_NB_0_DN
PE2_PCH_1_NB_0_DP
LOM1_TEST_ENABLE
TP_LOM1_TMS
TP_LOM1_TCK
TP_LOM1_TDI
TP_LOM1_TDO
LOM1_XTAL_IN
LOM1_XTAL_OUT

+3.3VAUX_LOM

NP R458 10K +/-1%

NP R430 10K +/-1%

R379 1K +/-5%

R1919 0 +/-5%

V_1P0_LOM1_CORE_VDD

X25MHZ_LOM1

XTAL 25MHz

C512 33pF +/-5%

C513 33pF +/-5%

C510 6.3V,X5R,+/-10% 1uF

+3.3VAUX_LOM

NC_LOM1_P6

C557 0.1uF 16V, X7R, +/-10%

C556 22uF 6.3V,X5R,+/-20%

C560 10uF +/-10% NP

Intel Lewisville LOM

+3.3VAUX_LOM

R396 10K +/-1%

<52> GPO_LOM1_EN R403 0 +/-5%

LOM1_LAN_DISABLE_N

R395 10K +/-1% NP

+3.3VAUX_LOM

C518 0.1uF NP

C501 470pF

C499 470pF NP

C498 470pF NP

P/N JFM38U1C-L1U1W CE team
recommend use DELL commercial P/N-->
JFM38U1C-L1T1-4F(34040VK00-600-G)

NIC1_USB

LOM1_LED_GRN_N
LOM1_LED_ORG_N

ETH_LOM1_0_DP
ETH_LOM1_0_DN
ETH_LOM1_1_DP
ETH_LOM1_1_DN
ETH_LOM1_2_DP
ETH_LOM1_2_DN
ETH_LOM1_3_DP
ETH_LOM1_3_DN

C509 1uF +/-10%

+3.3VAUX_LOM

R411 49.9 +/-1% NP

R412 49.9 +/-1% NP

R413 49.9 +/-1% NP

R414 49.9 +/-1% NP

R415 49.9 +/-1% NP

R416 49.9 +/-1% NP

R417 49.9 +/-1% NP

R418 49.9 +/-1% NP

C522 0.1uF NP

C521 0.1uF NP

C520 0.1uF NP

C519 0.1uF NP

LOM1_ACTLED_R_N

C500 470pF NP

V_5V_USB45 <62>

USB_P5_L_DN
USB_P4_L_DN <62>

USB_P5_L_DP
USB_P4_L_DP <62>

CONN - USBX2_RJ45

LOM1

DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 73 of 96

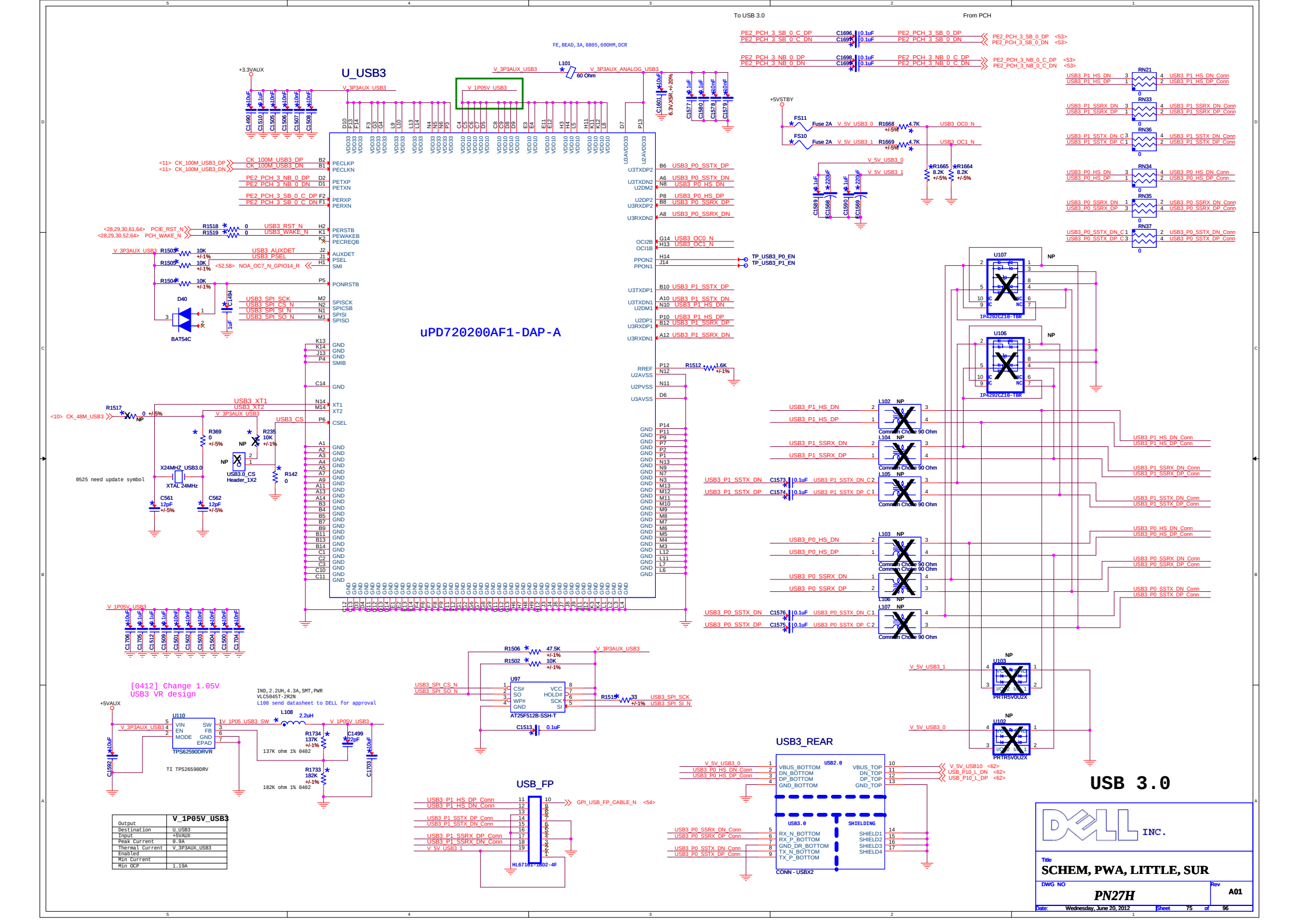
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 74 of 96


To USB 3.0
From PCH
U_USB3
uPD720200AF1-DAP-A
USB3_REAR
USB_FP
USB 3.0
[0412] Change 1.05V
USB3 VR design
TPS62590DRVR
AT25F512B-SSH-T
HL67101-1002-4F
CONN - USBX2
PRTR5V0U2X
IP4292CZ10-TBR
Common Choke 90 Ohm
V_1P05V_USB3
Output
Destination
Input
Peak Current
Thermal Current
Enabled
Min Current
Min OCP
U_USB3_
+5VAUX
1.19A
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date:
Wednesday, June 20, 2012
Sheet
75
of
96

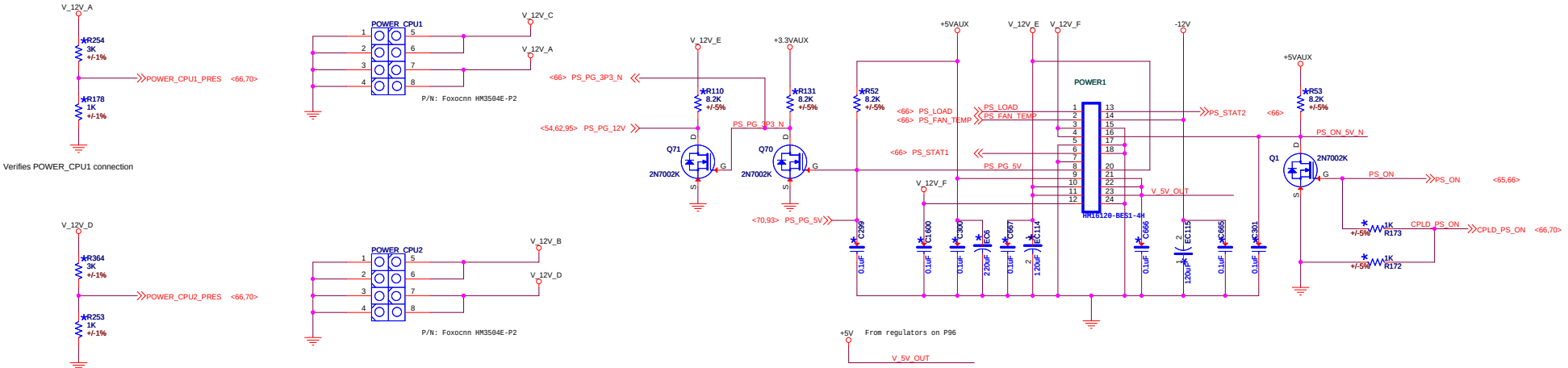
DELL INC.

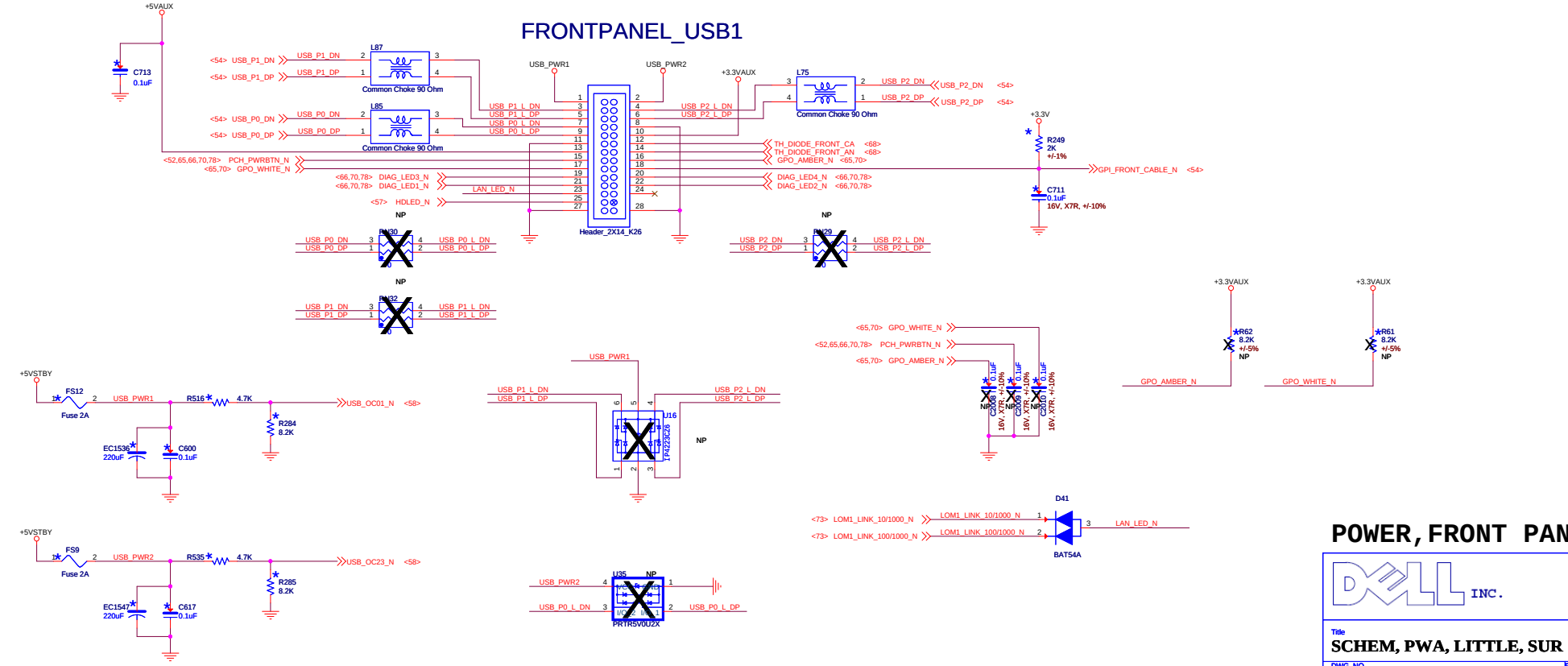
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 76 of 96





POWER, FRONT PANEL

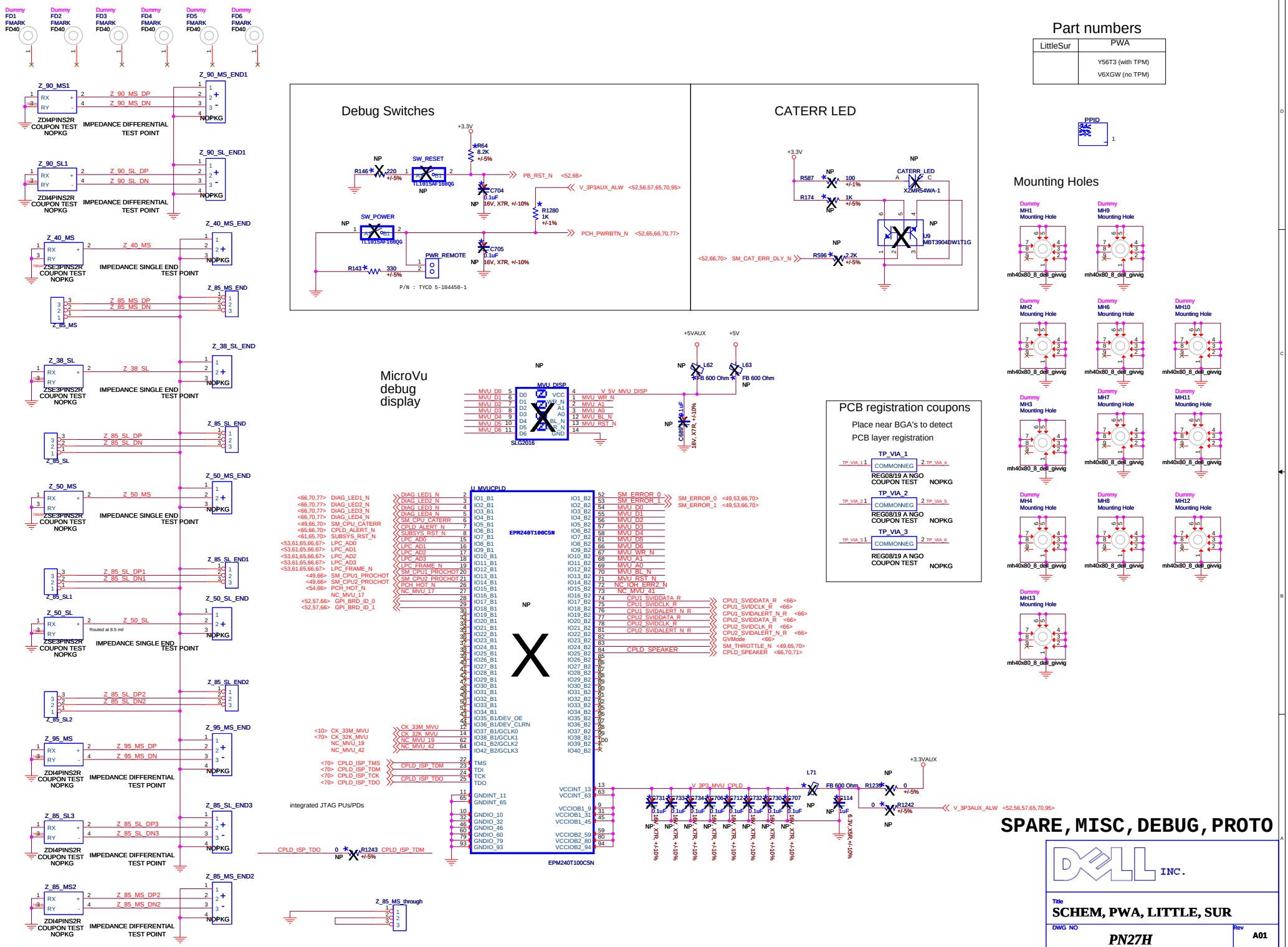
DELL INC.

Title: SCHEM, PWA, LITTLE, SUR

DWG NO: PN27H

Rev: A01

Date: Wednesday, June 20, 2012 Sheet 77 of 96



Part numbers

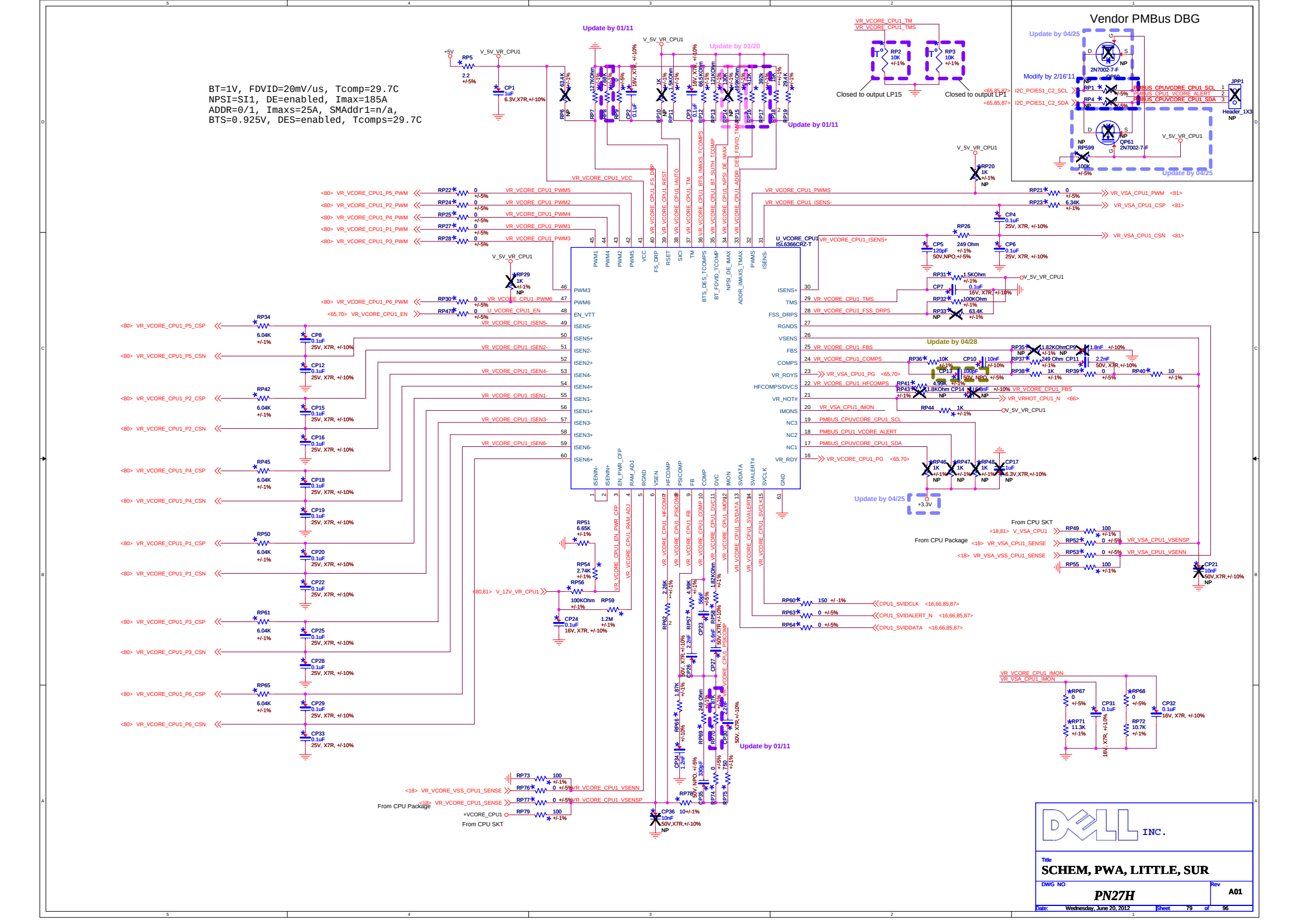
LittleSur	PWA
	Y56T3 (with TPM) V6XGW (no TPM)

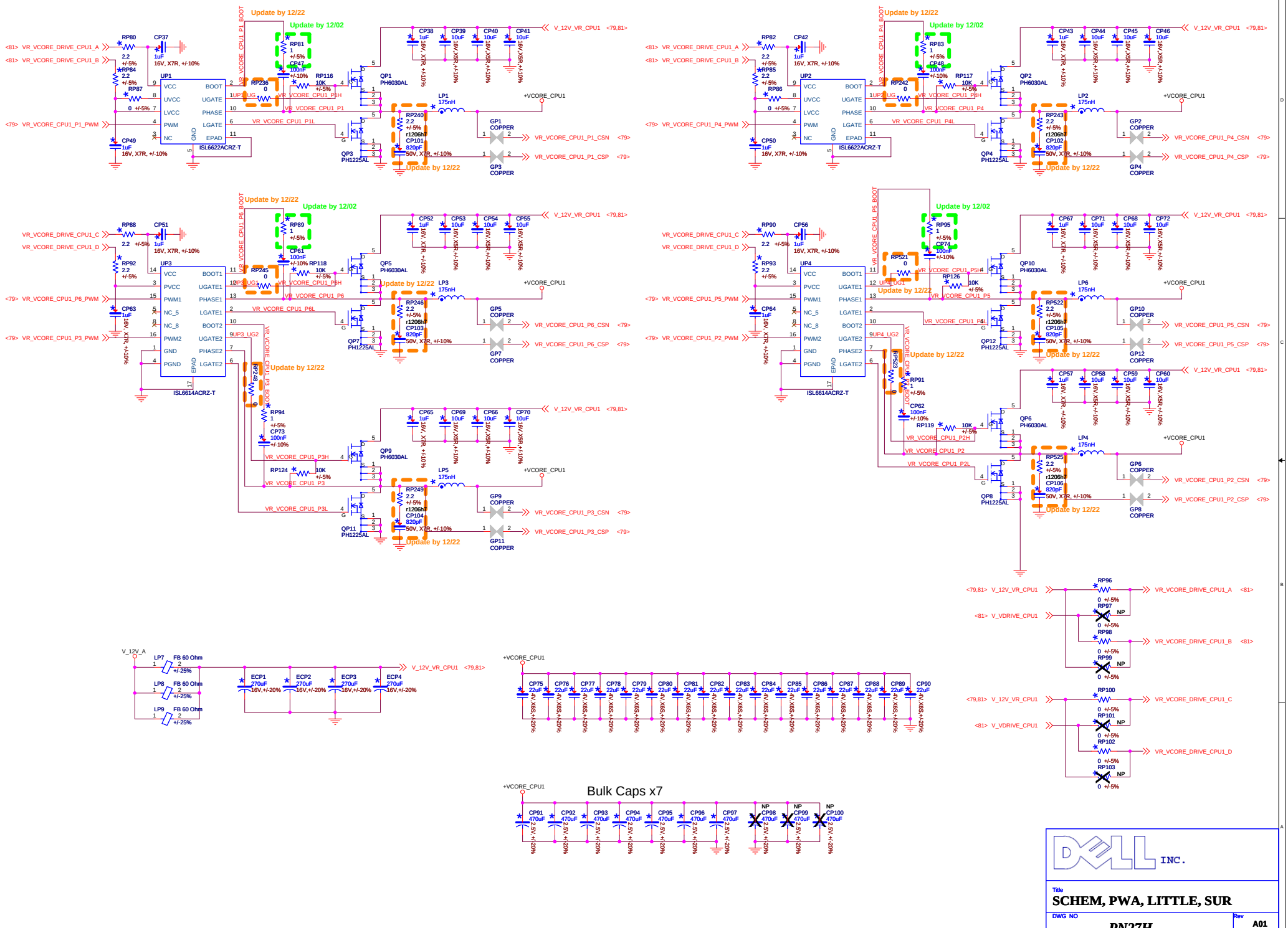
DELL INC.

Title: **SCHEM, PWA, LITTLE, SUR**

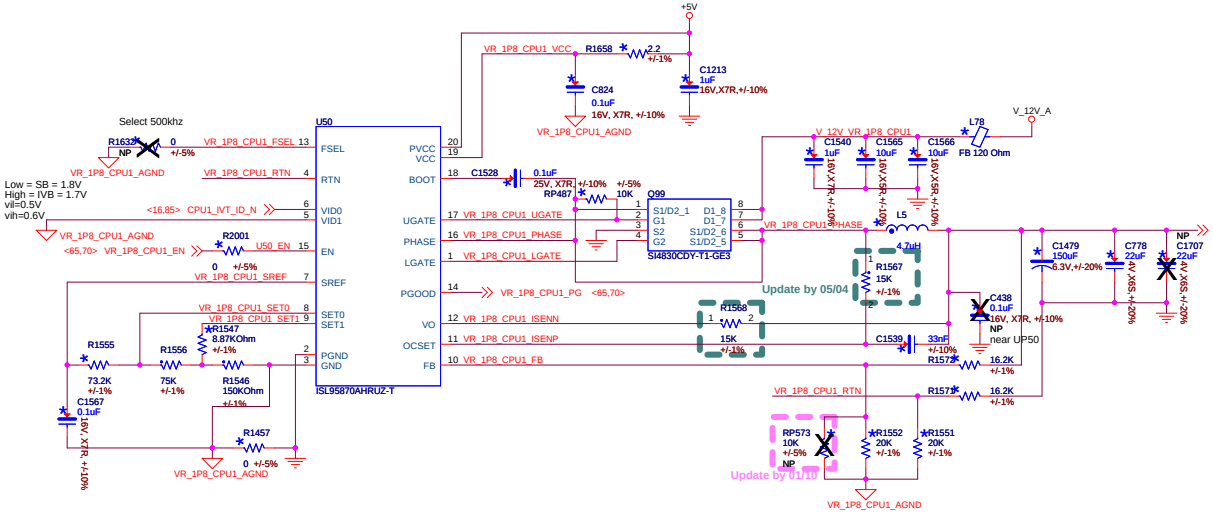
DWG NO: ***PN27H*** Rev: **A01**

Date: Wednesday, June 20, 2012 Sheet 78 of 96

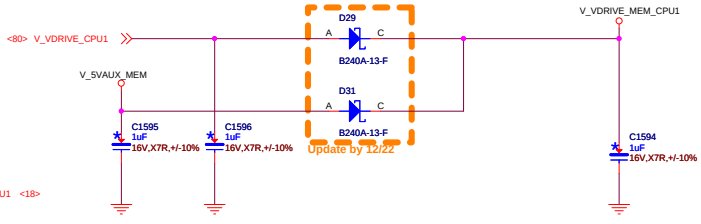

BT=1V, FDVID=20mV/us, Tcomp=29.7C
NPSI=SI1, DE=enabled, Imax=185A
ADDR=0/1, Imaxs=25A, SMAddr1=n/a,
BTS=0.925V, DES=enabled, Tcomps=29.7C
Vendor PMBus DBG
Update by 04/25
Modify by 2/16'11
Update by 01/11
Update by 01/20
Update by 04/28
Closed to output LP15
Closed to output LP1
U_VCORE_CPU1
ISL6366CRZ-T
From CPU SKT
From CPU Package
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 79 of 96


Update by 12/22
Update by 12/02
UP1
ISL6622ACRZ-T
UP2
ISL6622ACRZ-T
UP3
ISL6614ACRZ-T
UP4
ISL6614ACRZ-T
Bulk Caps x7
DELL INC.
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 80 of 96

Output	V_1P8_CPU1
Destination	CPU1 PLL Voltage
Input	12V
Peak Current	2.5A
Thermal Current	2.0A
Enabled	
Min Current	500mA

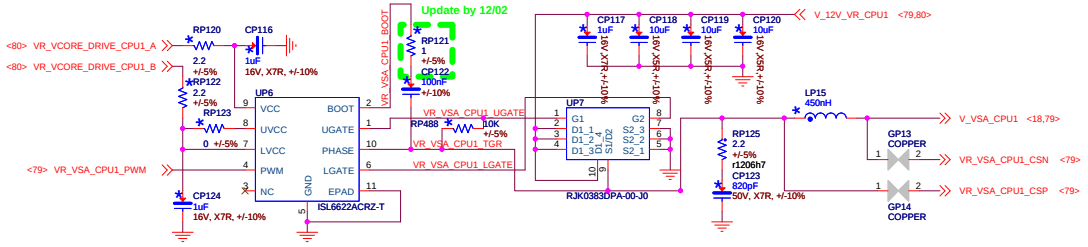


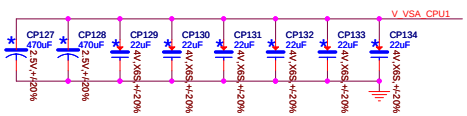
Run the Memory regulator drivers from ~7v when the system is on and 5vAUX when system is in S3.



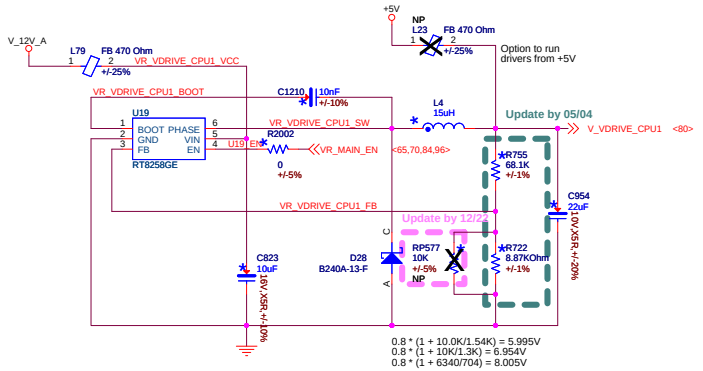
todo: After placement try and combine VDRIVE circuits from CPU1 and CPU2 to save cost

Output	V_VSA_CPU1
Destination	CPU1 VSA rail
Input	12V
Peak Current	VSA 20 A/24 A @ 0.85 V
Thermal Current	tbd
Enabled	





Output	V_VDRIVE_CPU1
Destination	CPU1 vcore regulator drivers
Input	12V
Peak Current	1.0A
Thermal Current	390mA
Enabled	
Min Current	120mA
Min OCP	1.6A



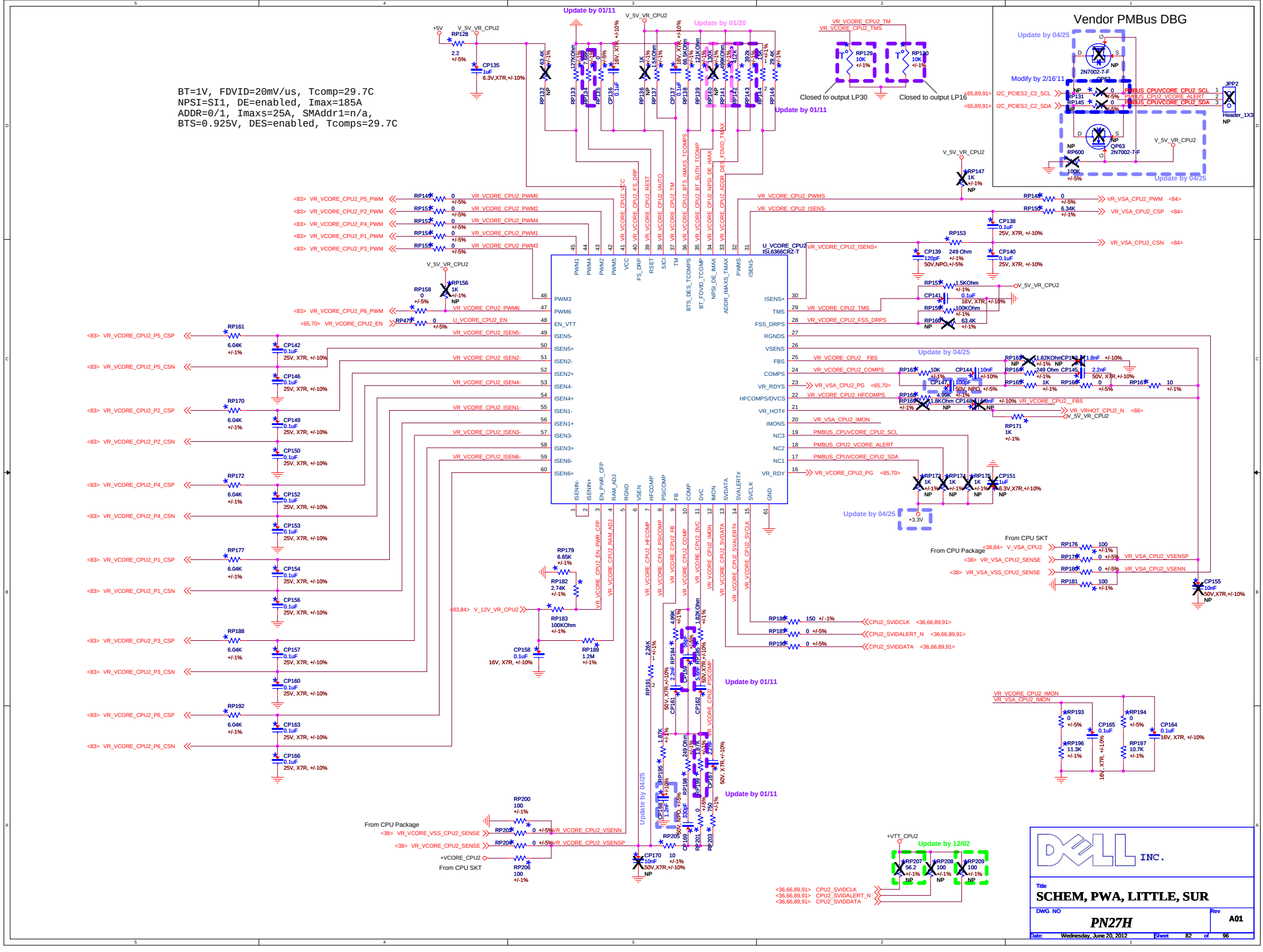
DELL INC.

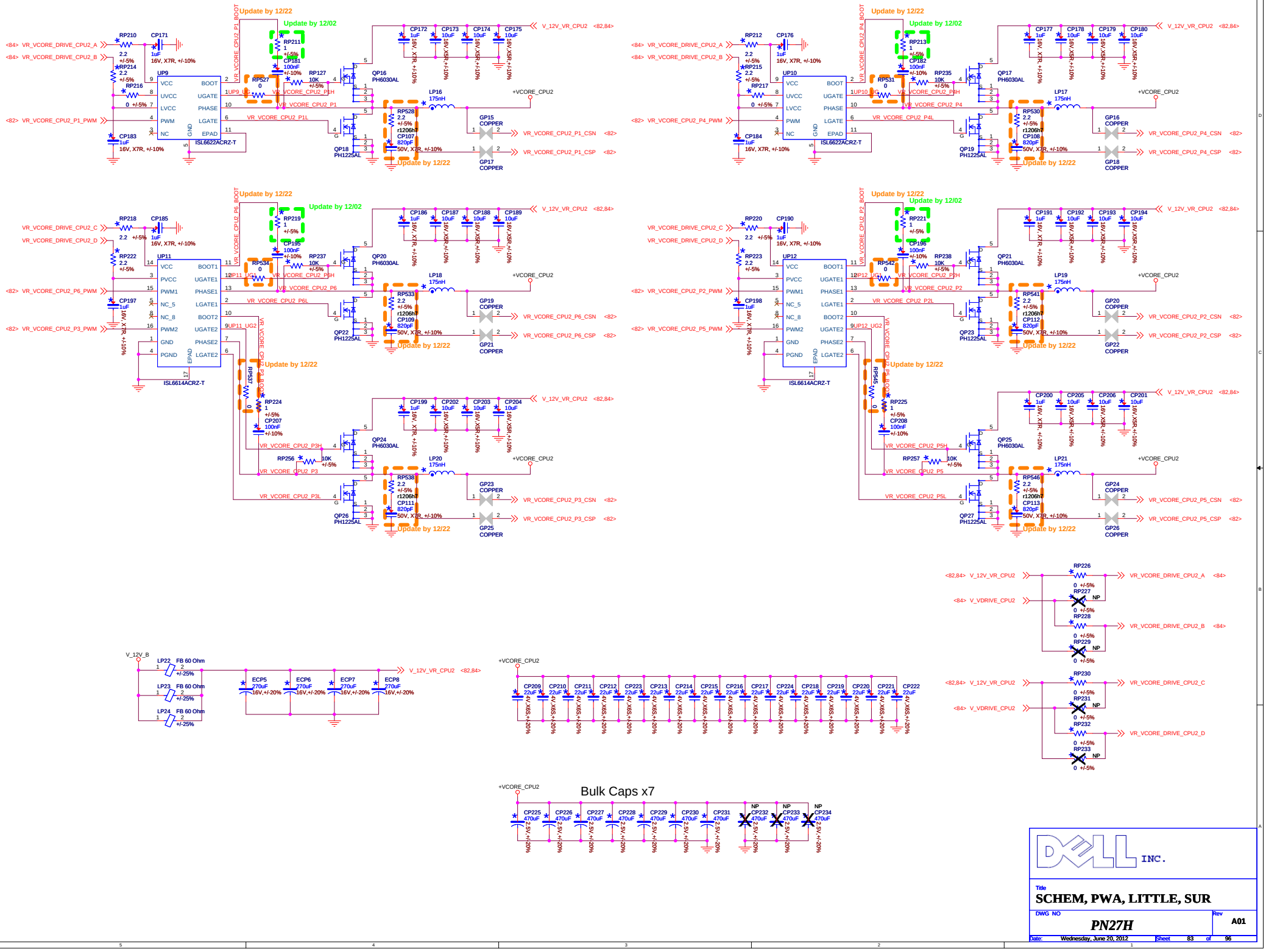
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 81 of 96


BT=1V, FDVID=20mV/us, Tcomp=29.7C
NPSI=SI1, DE=enabled, Imax=185A
ADDR=0/1, Imaxs=25A, SMAddr1=n/a,
BTS=0.925V, DES=enabled, Tcomps=29.7C
Vendor PMBus DBG
Update by 04/25
Modify by 2/16'11
Update by 01/11
Update by 01/20
Update by 12/02
Closed to output LP30
Closed to output LP16
U_VCORE_CPU2
ISL6366CRZ-T
Header_1X3
2N7002-7-F
From CPU SKT
From CPU Package
+VCORE_CPU2
+VTT_CPU2
V_5V_VR_CPU2
V_12V_VR_CPU2
Title
SCHEM, PWA, LITTLE, SUR
DWG NO
PN27H
Rev
A01
Date: Wednesday, June 20, 2012
Sheet 82 of 96

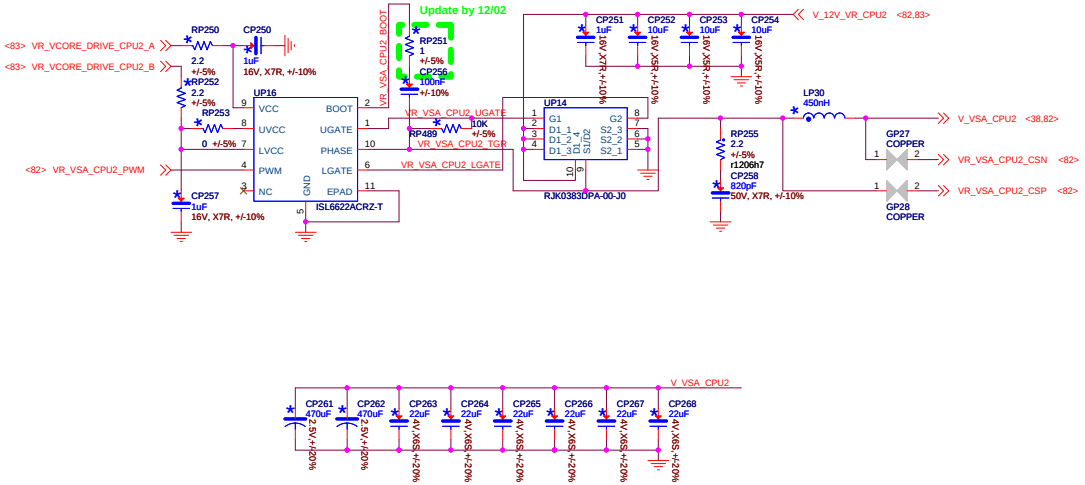


Title	SCHEM, PWA, LITTLE, SUR
DWG NO	PN27H
Rev	A01
Date:	Wednesday, June 20, 2012
Sheet	83 of 96

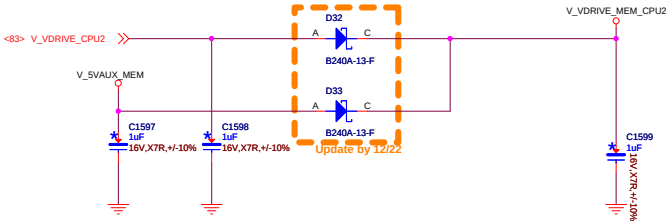
Add by Bob 12/25

Dummy all parts
Ronnie Update by 04/20
Del this schematic 05/04

Output	V_VSA_CPU2
Destination	CPU2 VSA rail
Input	12V
Peak Current	VSA 20 A/24 A @ 0.85 V
Thermal Current	tbd
Enabled	

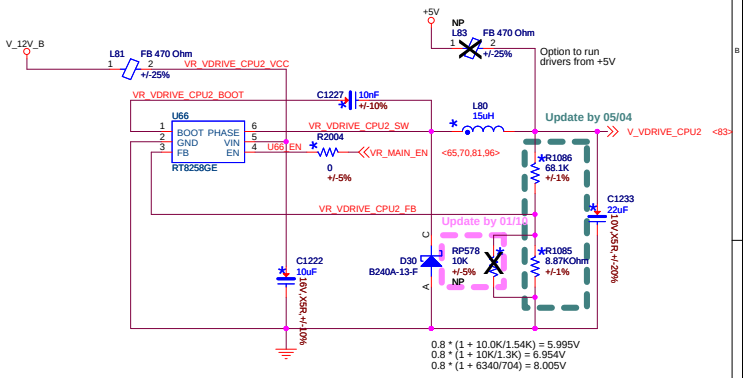


Run the Memory regulator drivers from ~7v when the system is on and 5vAUX when system is in S3.



todo: After placement try and combine VDRIVE circuits from CPU1 and CPU2 to save cost

Output	V_VDRIVE_CPU2
Destination	CPU2 vcore regulator drivers
Input	12V
Peak Current	1.0A
Thermal Current	390mA
Enabled	
Min Current	120mA
Min OCP	1.6A



DELL INC.

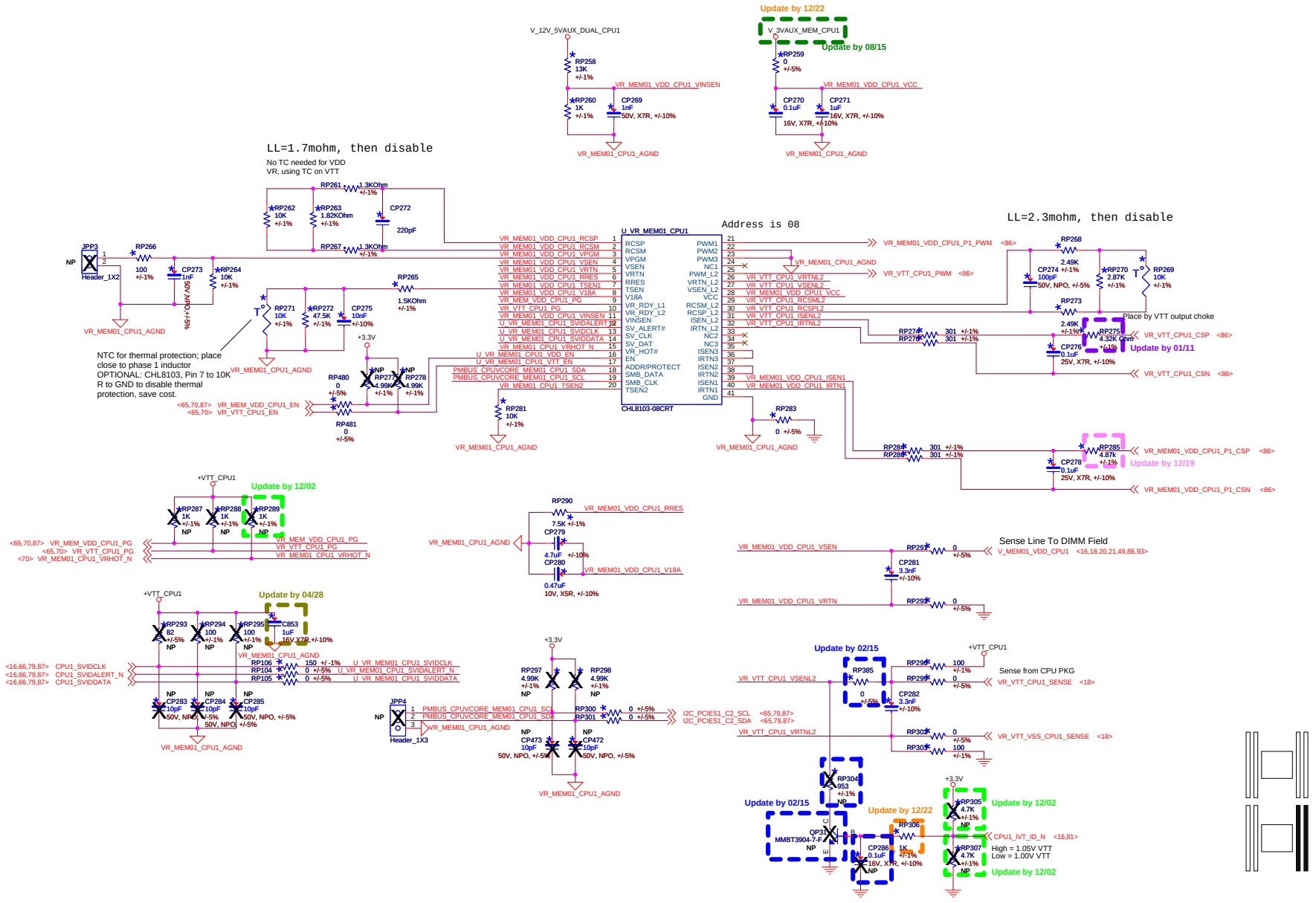
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 84 of 96

CPU1 MEM01- CHIL CHL8103



DELL INC.

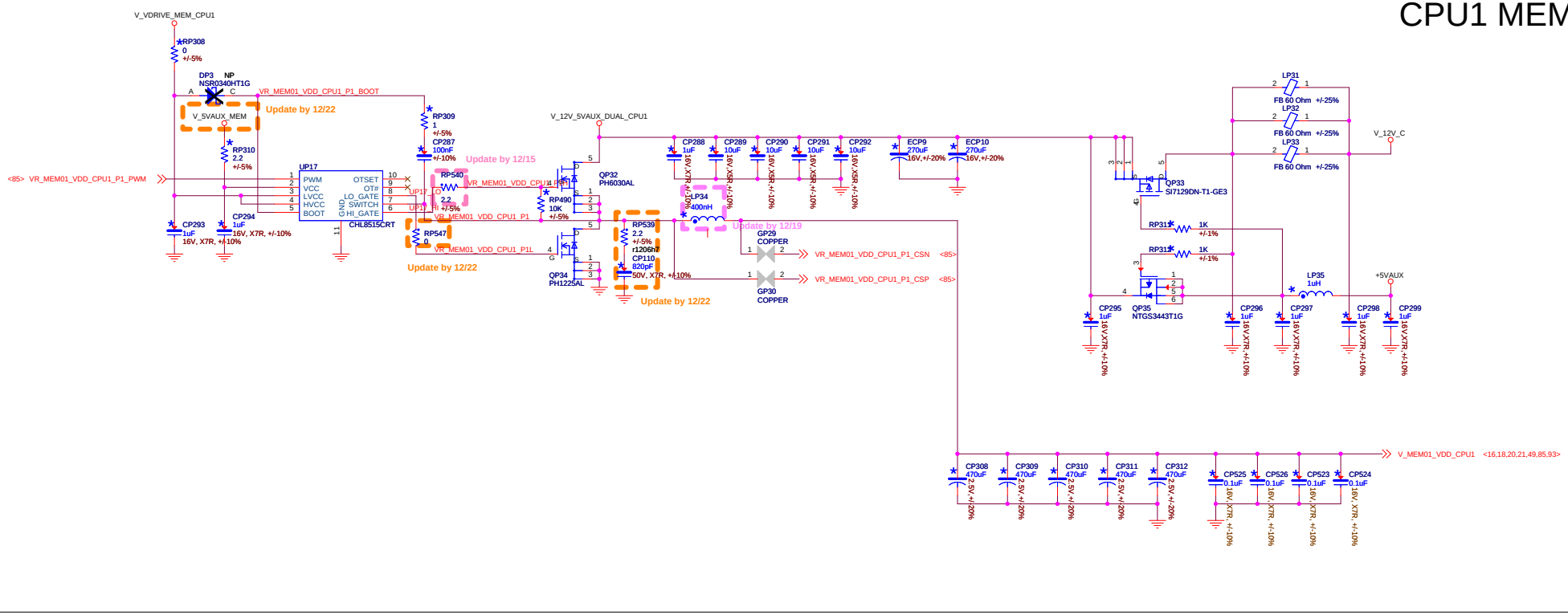
Title
SCHEM, PWA, LITTLE, SUR

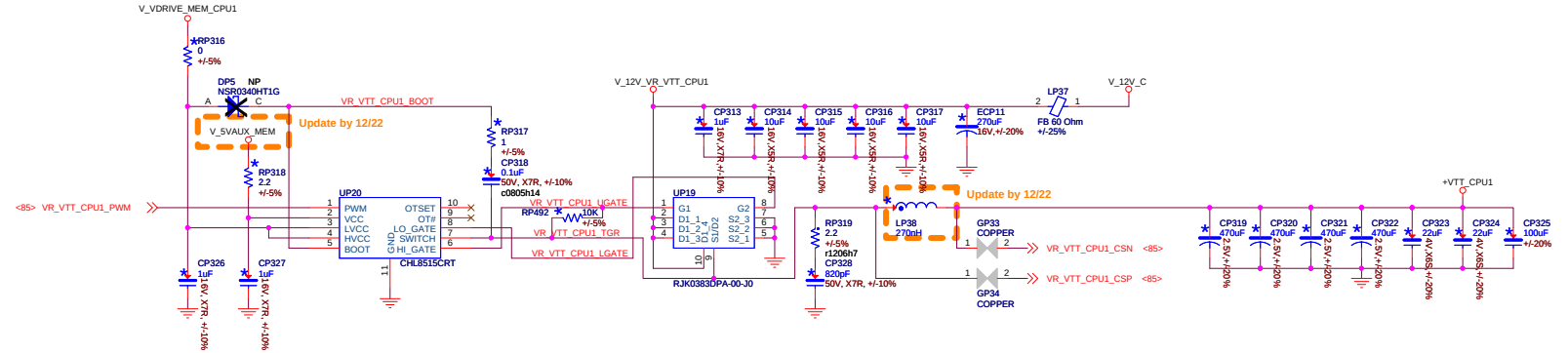
DWG NO
PN27H

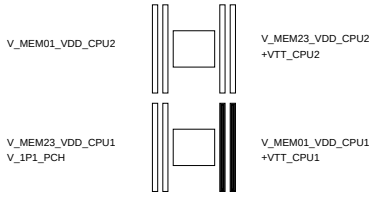
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 85 of 96

CPU1 MEM01







DELL INC.

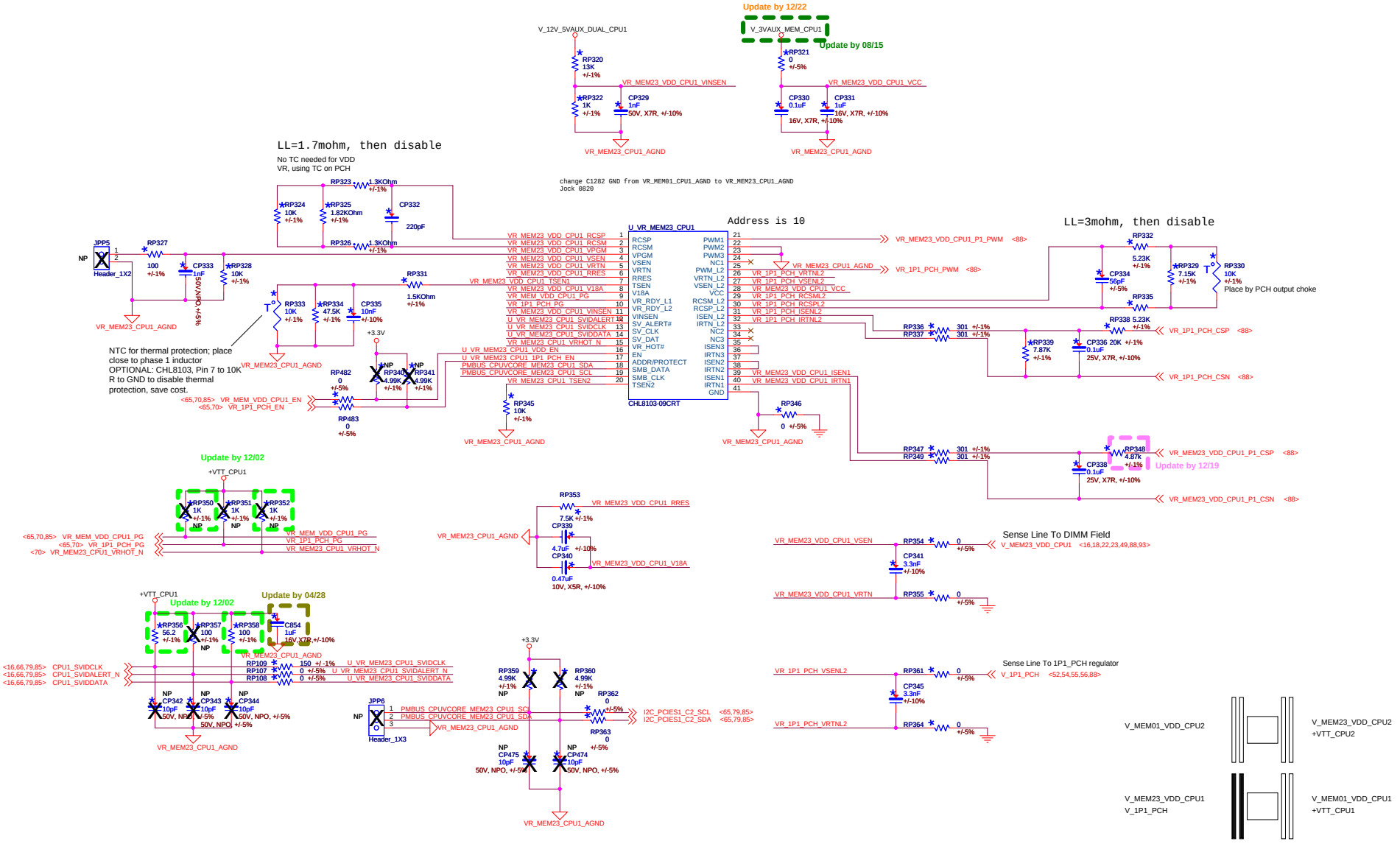
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 86 of 96

CPU1 MEM23- CHIL CHL8103



DELL INC.

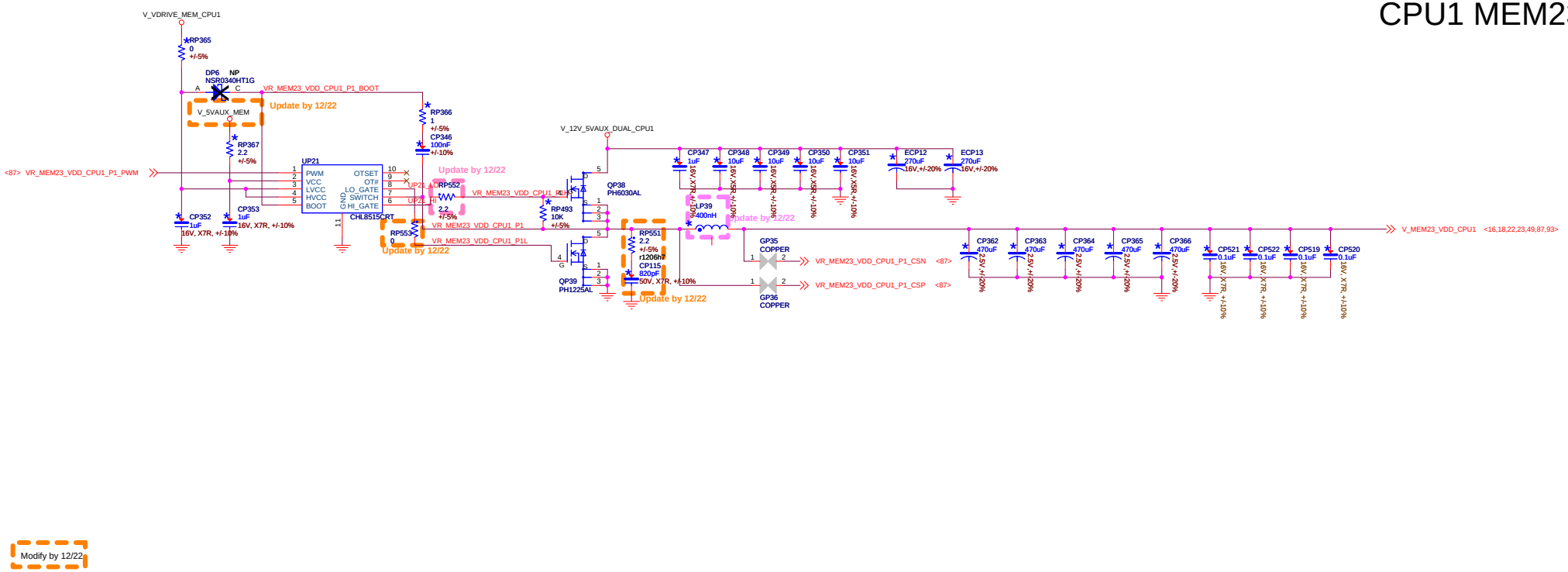
Title
SCHEM, PWA, LITTLE, SUR

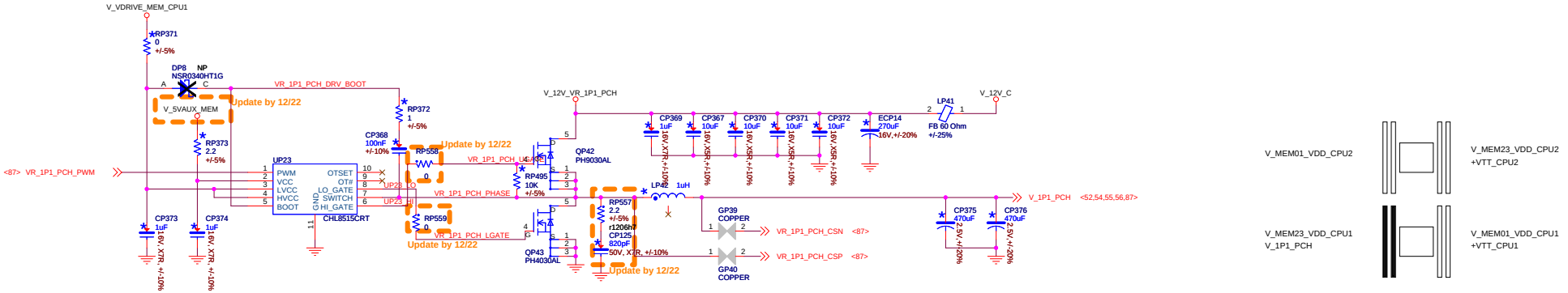
DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 87 of 96

CPU1 MEM23





DELL INC.

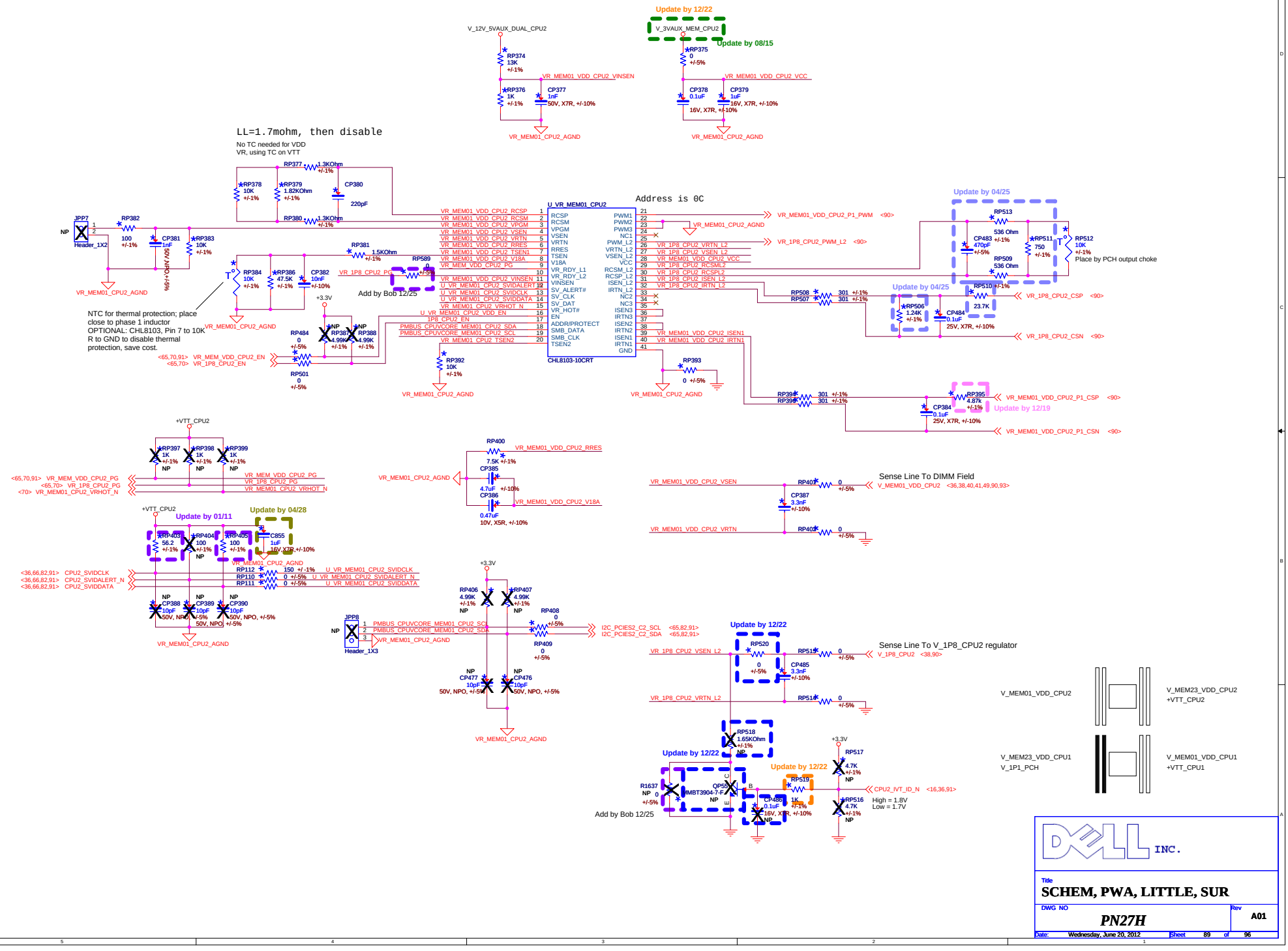
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 88 of 96

CPU2 MEM01- CHIL CHL8103



DELL INC.

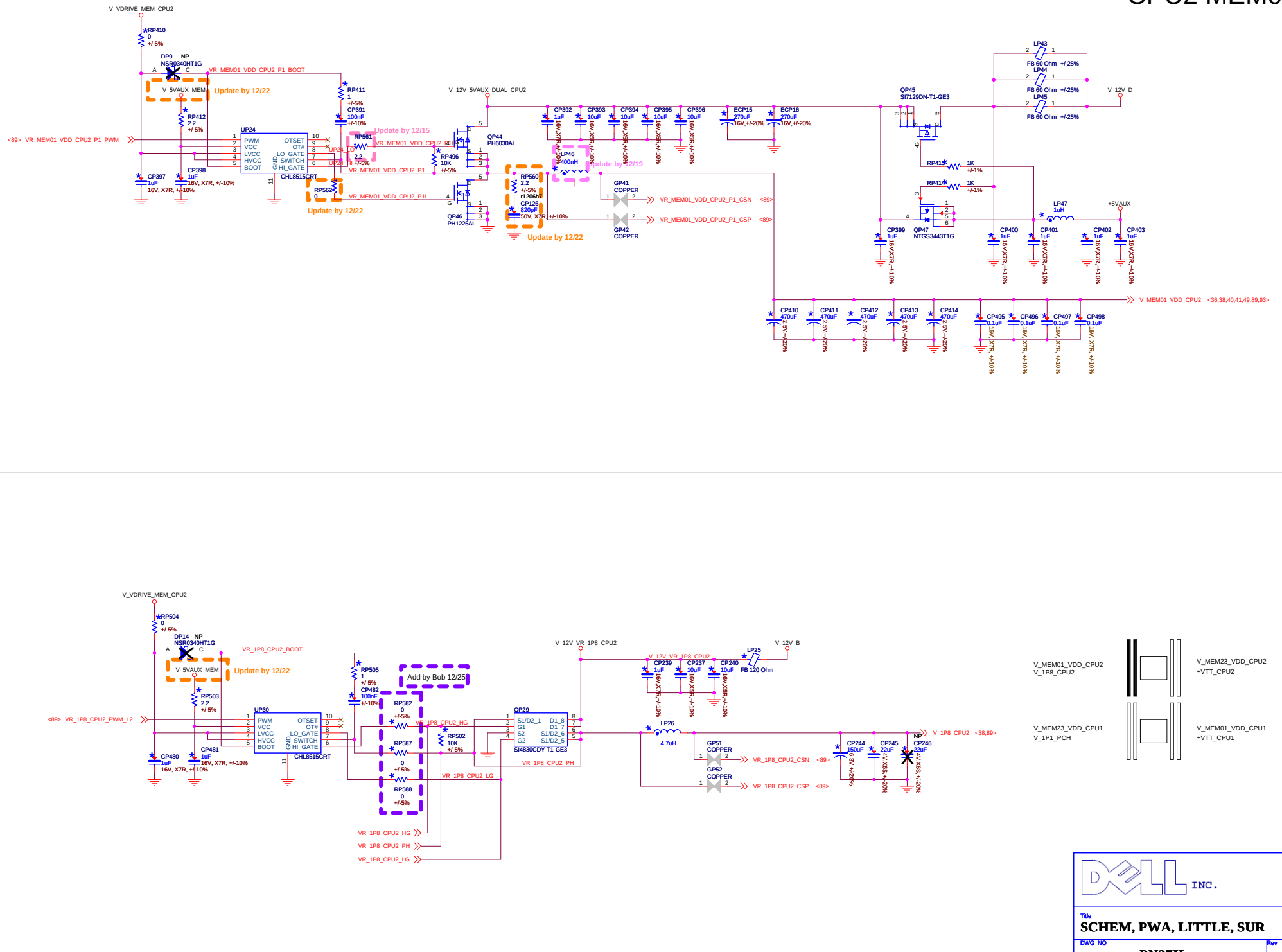
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 89 of 96

CPU2 MEM01



DELL INC.

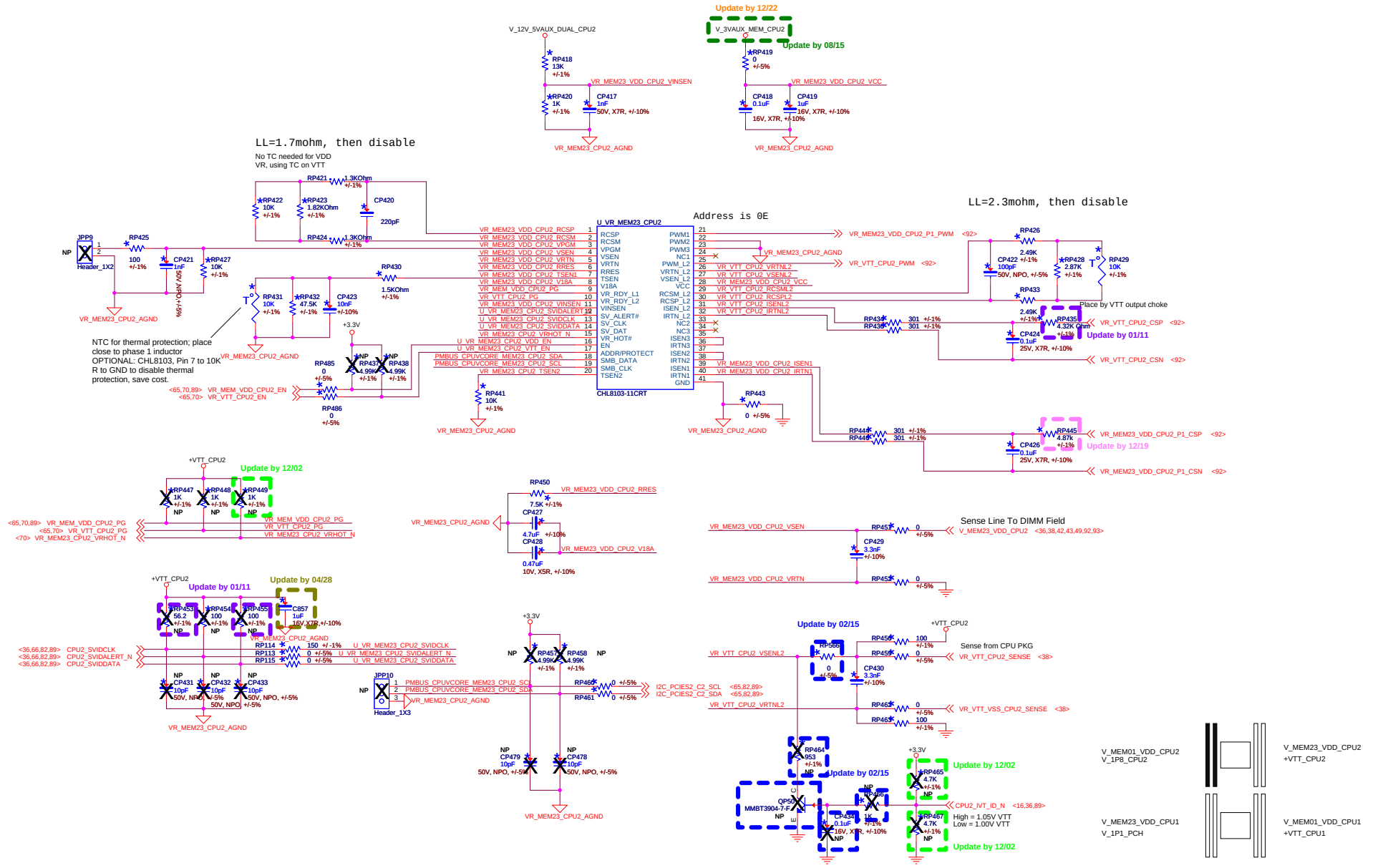
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

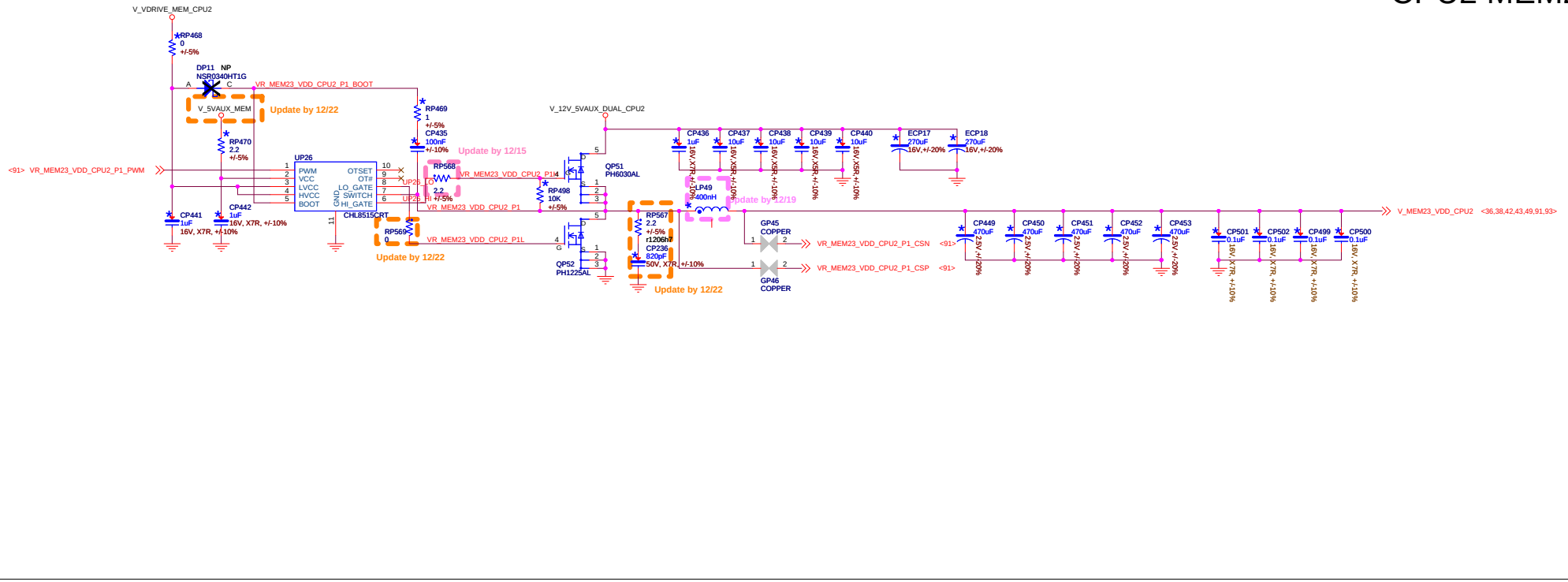
Rev
A01

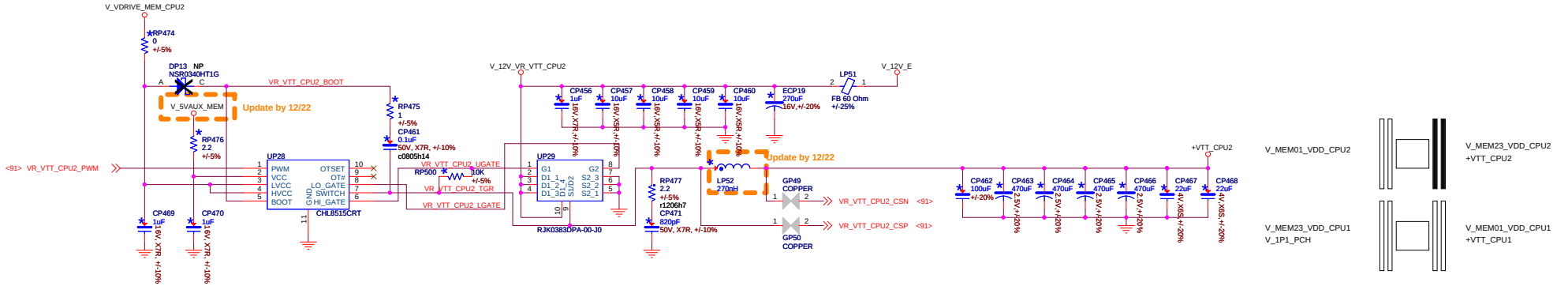
Date: Wednesday, June 20, 2012 Sheet 90 of 96

CPU2 MEM23- CHIL CHL8103



CPU2 MEM23





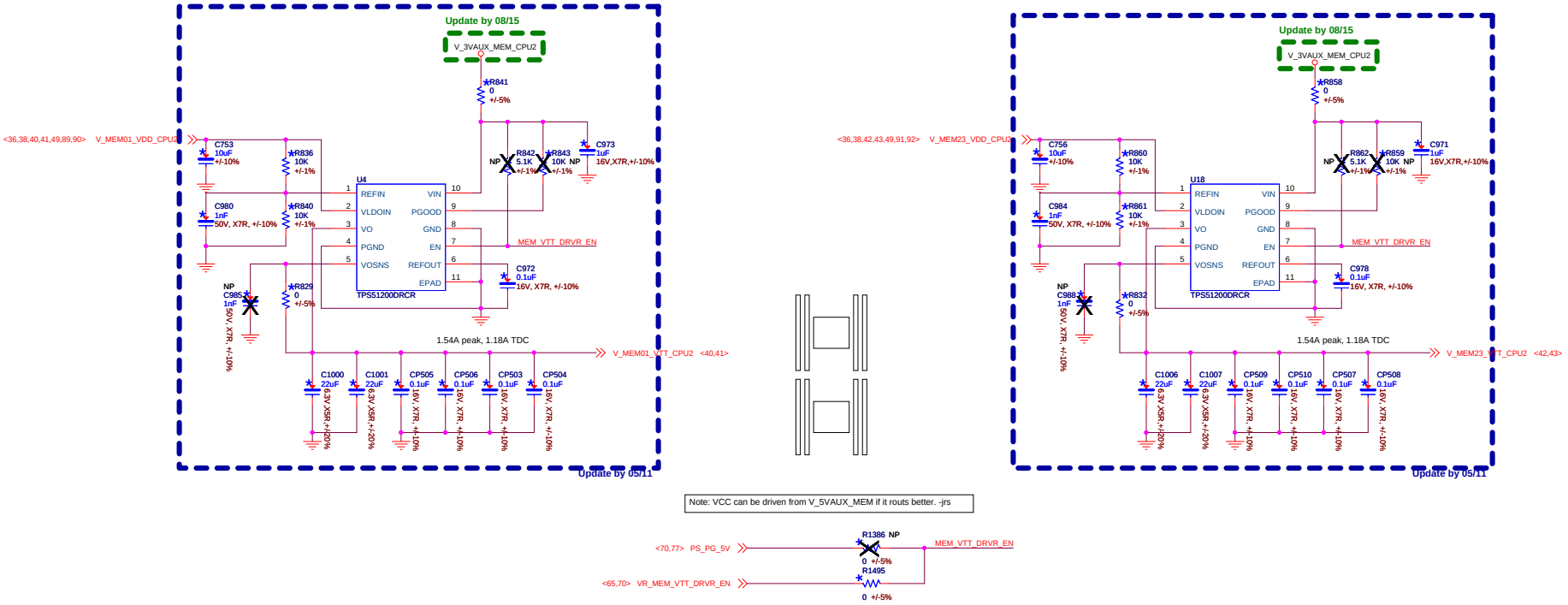
DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 92 of 96



DELL INC.

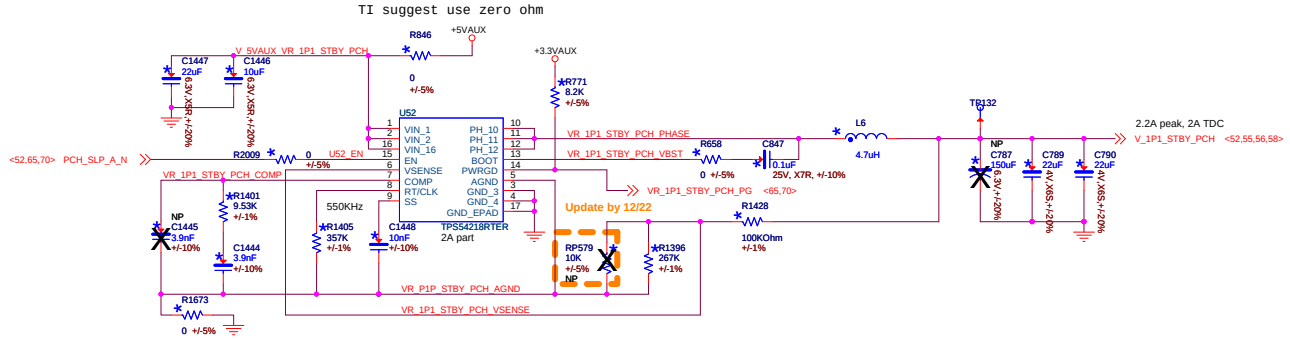
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

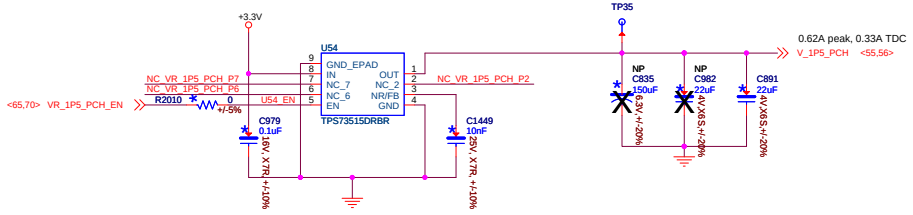
Rev
A01

Date: Wednesday, June 20, 2012 Sheet 93 of 96

Output	V_1P1_STBY_PCH
Destination	PCH
Intput	+5VAUX
Output	1.1V
tdc Current	2.0A
Max Current	2.4A
Min Load	
Min OCP	2.9A



Output	V_1P5_PCH
Destination	PCH
Intput	3.3v
Peak Current	620mA
TDP Current	330mA
OCP	800mA
Enabled	



DELL INC.

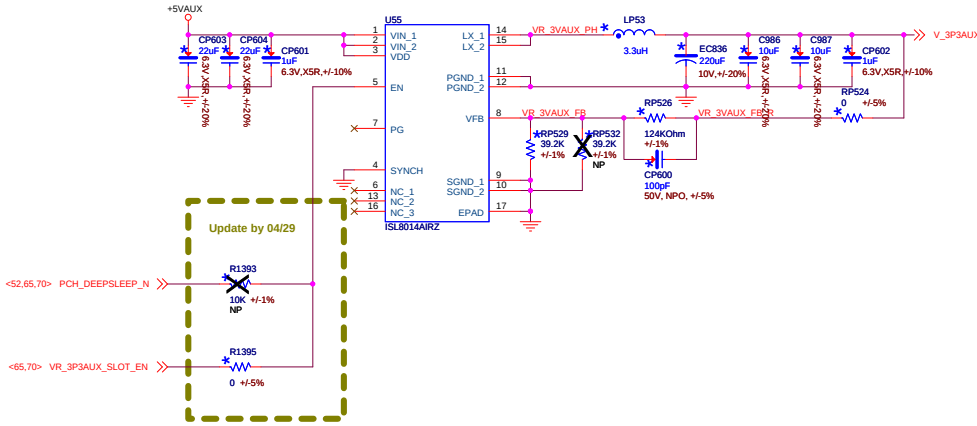
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

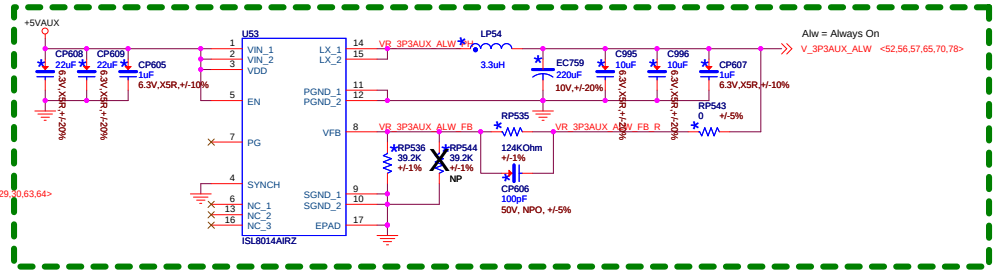
Rev
A01

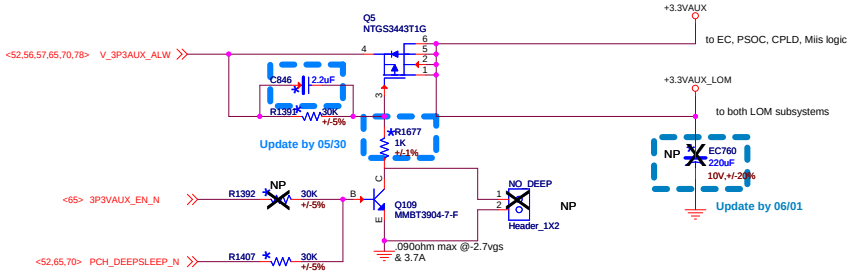
Date: Wednesday, June 20, 2012 Sheet 94 of 96

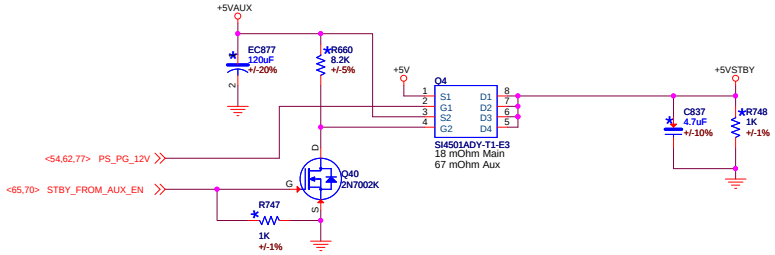
Output	V_3P3AIUX
Destination	
Intput	+5VAUX
Peak Current	TBD
Thermal Current	TBD
Enabled	

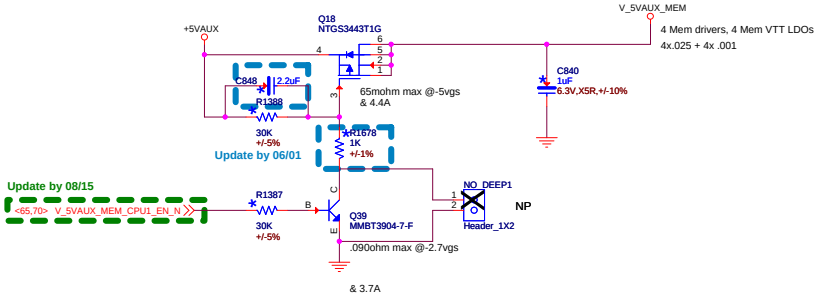


Update by 08/15

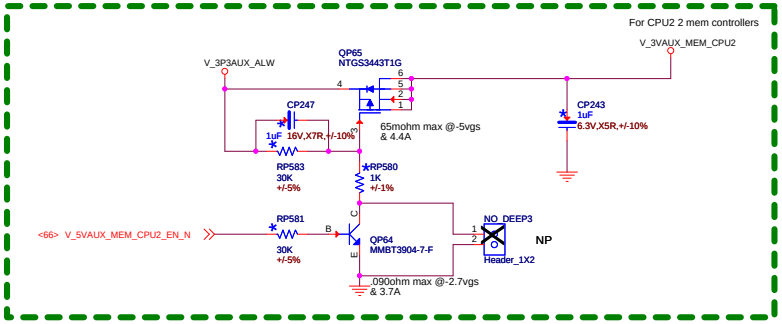




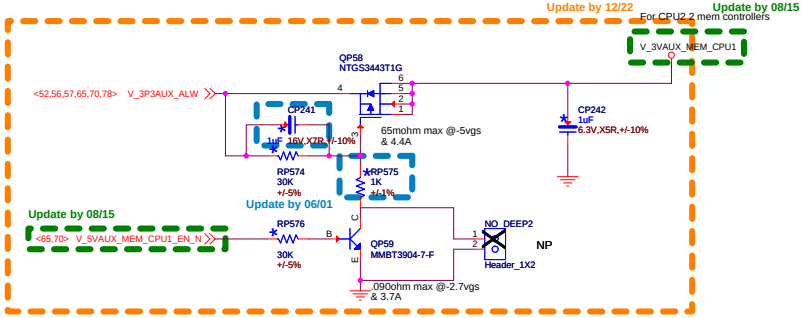




Update by 08/15



Update by 12/22 Update by 08/15



DELL INC.

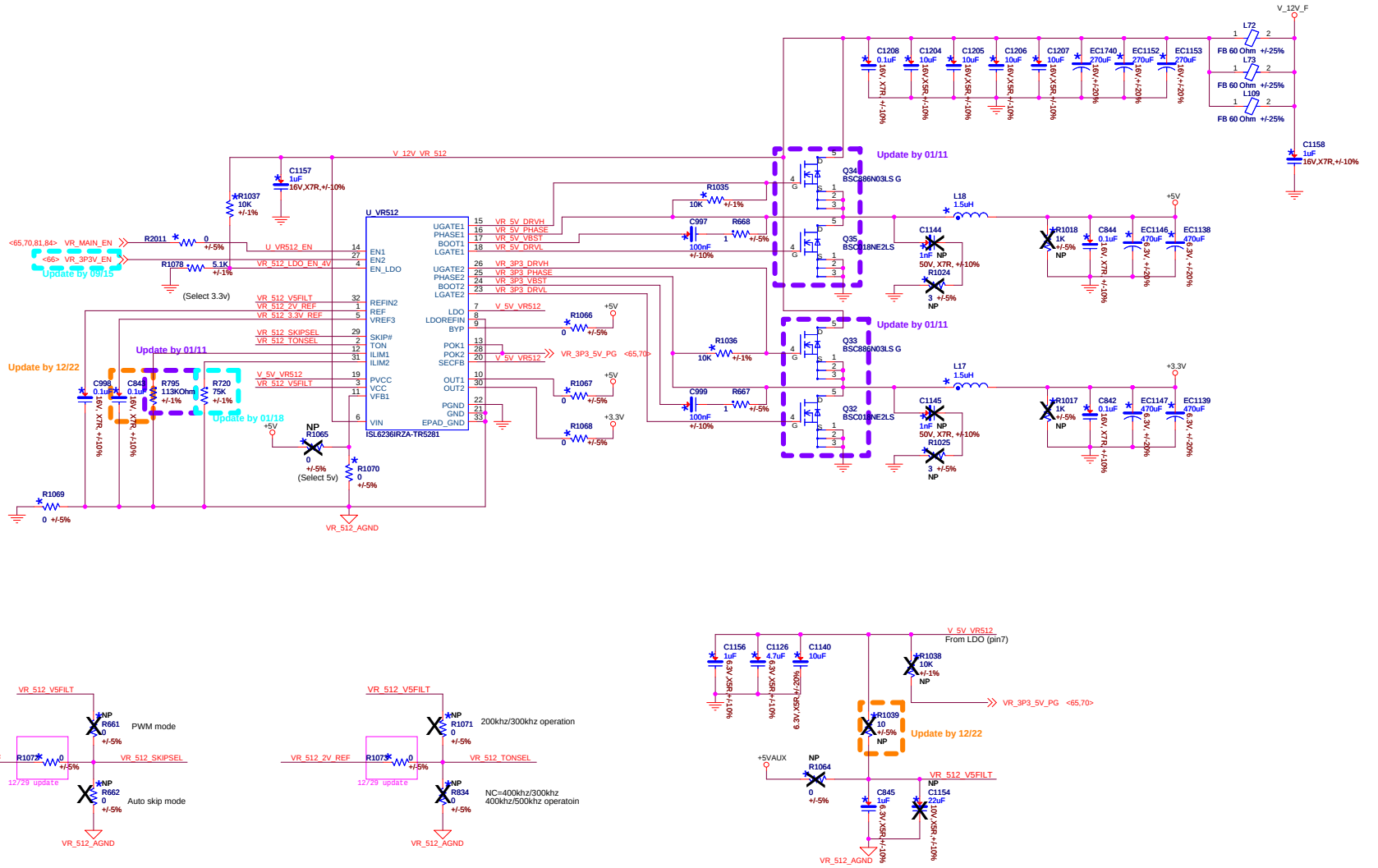
Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 95 of 96

0506 Change to V_12V_F for X00 board with new PSU's



DELL INC.

Title
SCHEM, PWA, LITTLE, SUR

DWG NO
PN27H

Rev
A01

Date: Wednesday, June 20, 2012 Sheet 96 of 96