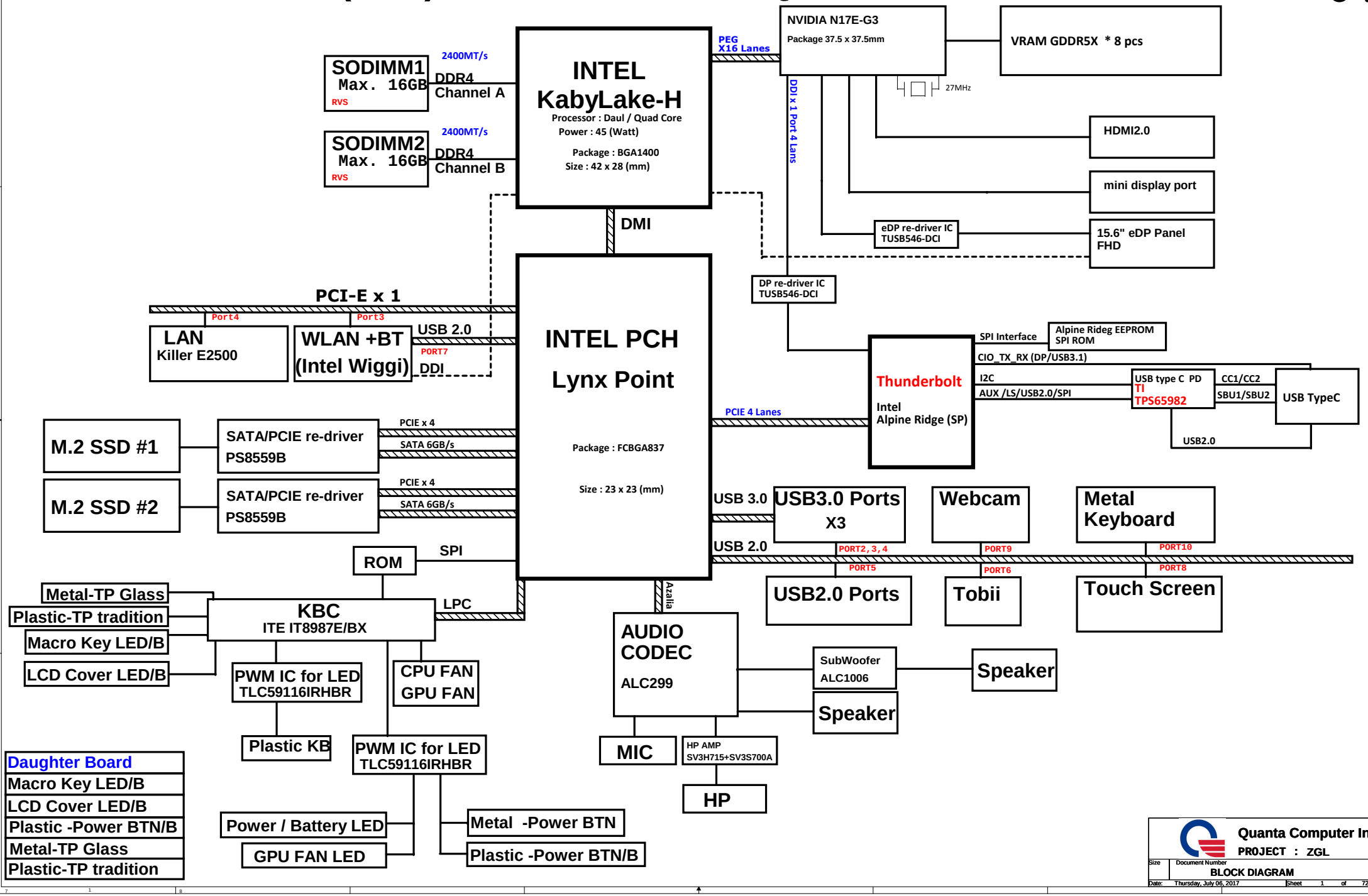
Falcon(ZGL) KBL-H +1080MAX Q SYSTEM DIAGRAM

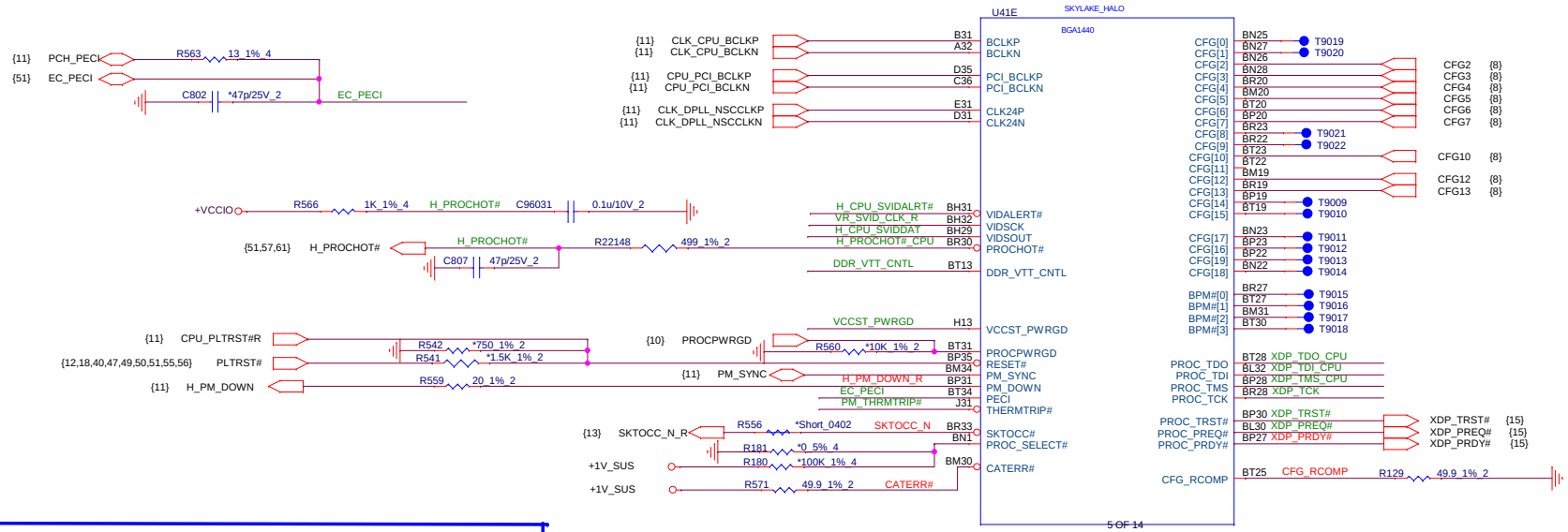
01



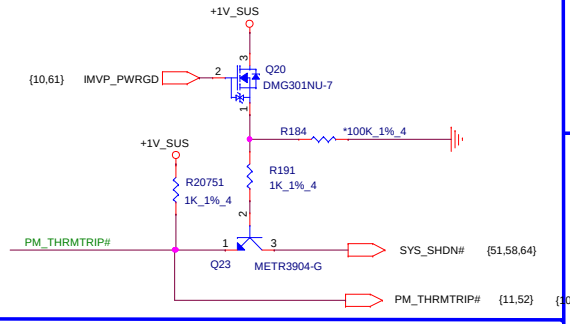
Quanta Computer Inc.
PROJECT : ZGL

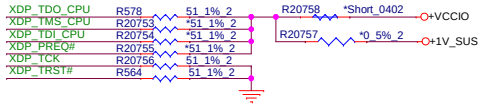
Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Thursday, July 06, 2017 Sheet 1 of 72

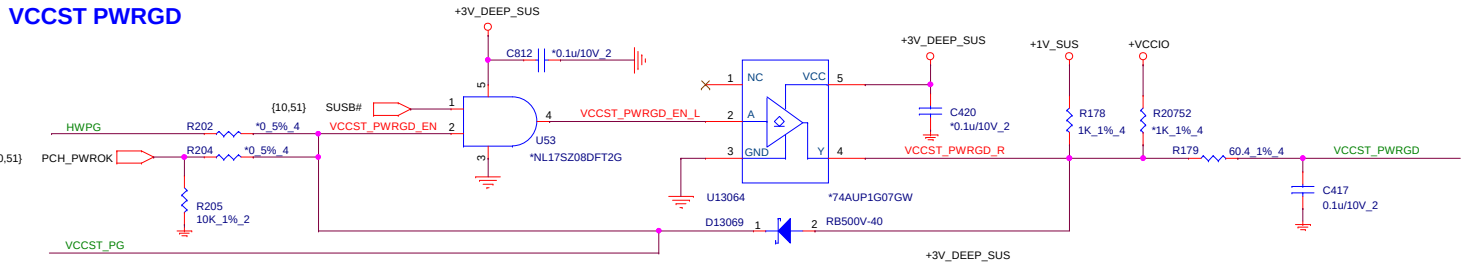


CPU thermal trip

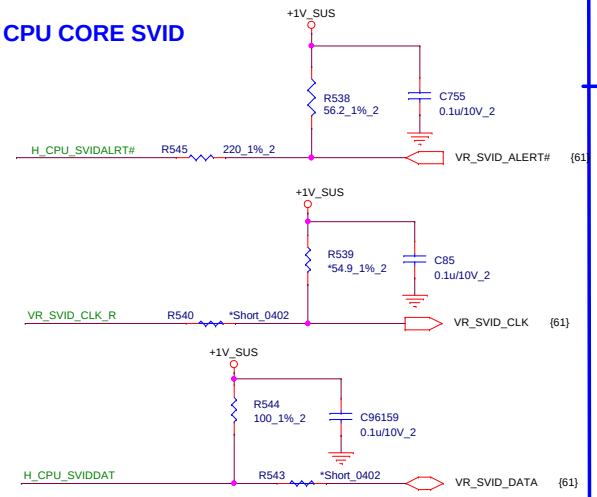


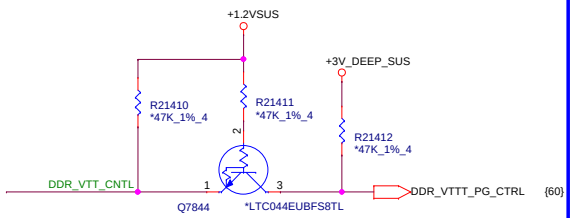


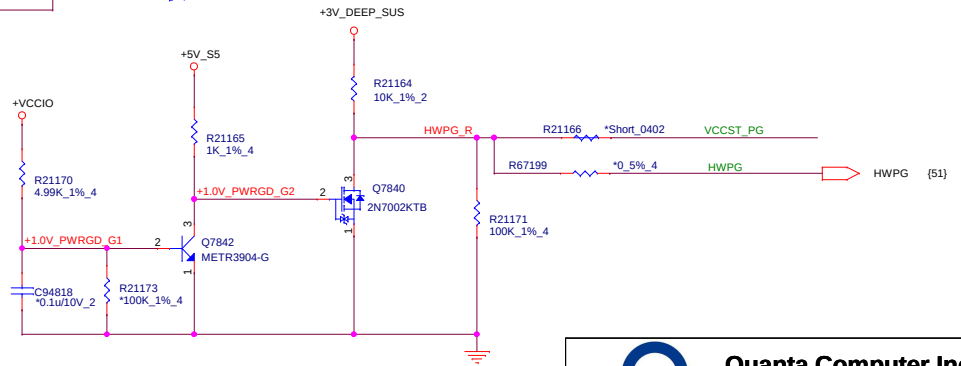
VCCST PWRGD



CPU CORE SVID







Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	02 -- Kabylake 1/7 (eDP/DDI)	1A
Date: Thursday, July 06, 2017	Sheet 2 of 72	

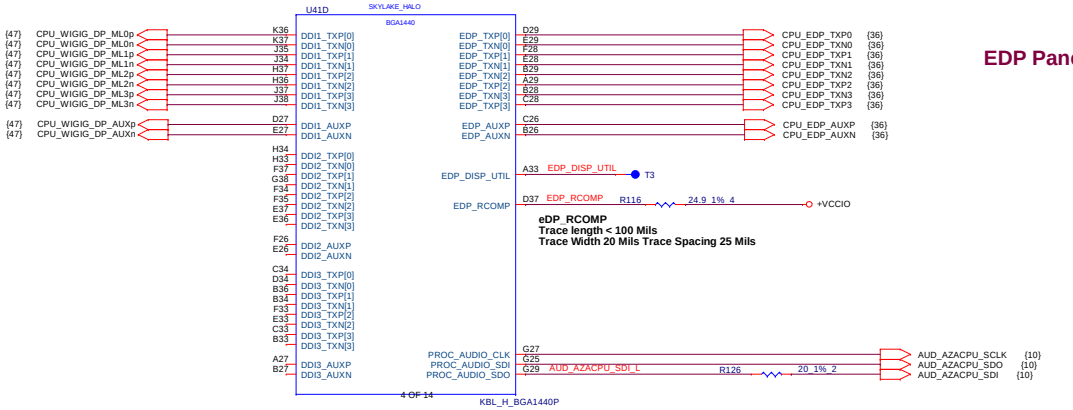
dGPU PEG*16
Lane Reversed

dGPU PEG*16
Lane Reversed

DMI

DMI

Intel Wigig

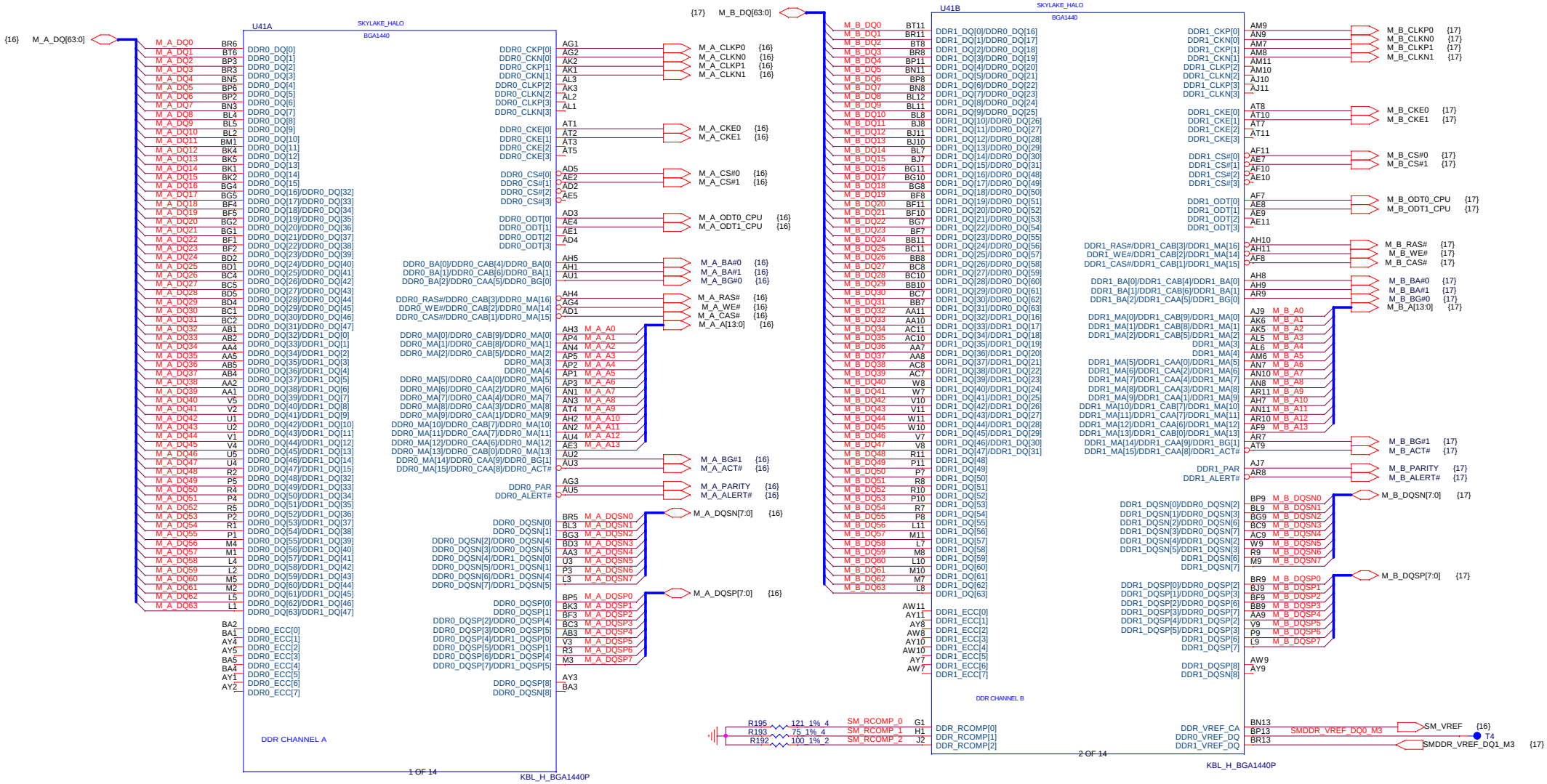


EDP Panel

eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

Quanta Computer Inc.
PROJECT : ZGL

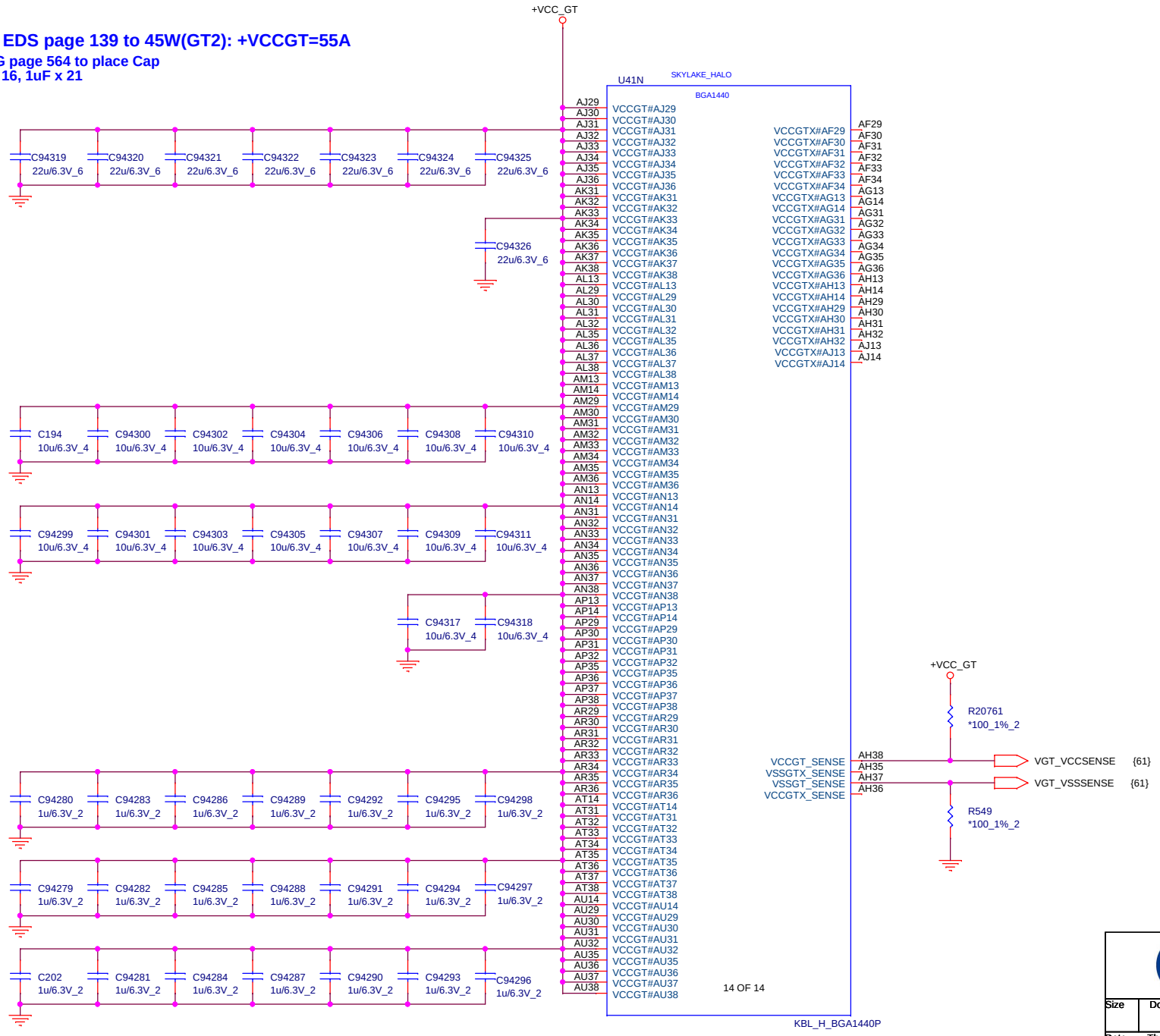
Size	Document Number	Rev
	Kabylake 2/7 (PCIE&DMI&FDI)	1A
Date: Thursday, July 06, 2017	Sheet 3 of 72	



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Kabylake 3/7 (DDR3 I/F)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 4 of 72	

Follow KBL H EDS page 139 to 45W(GT2): +VCCGT=55A

Follow KBL H DG page 564 to place Cap
22uF x 8, 10uF x 16, 1uF x 21



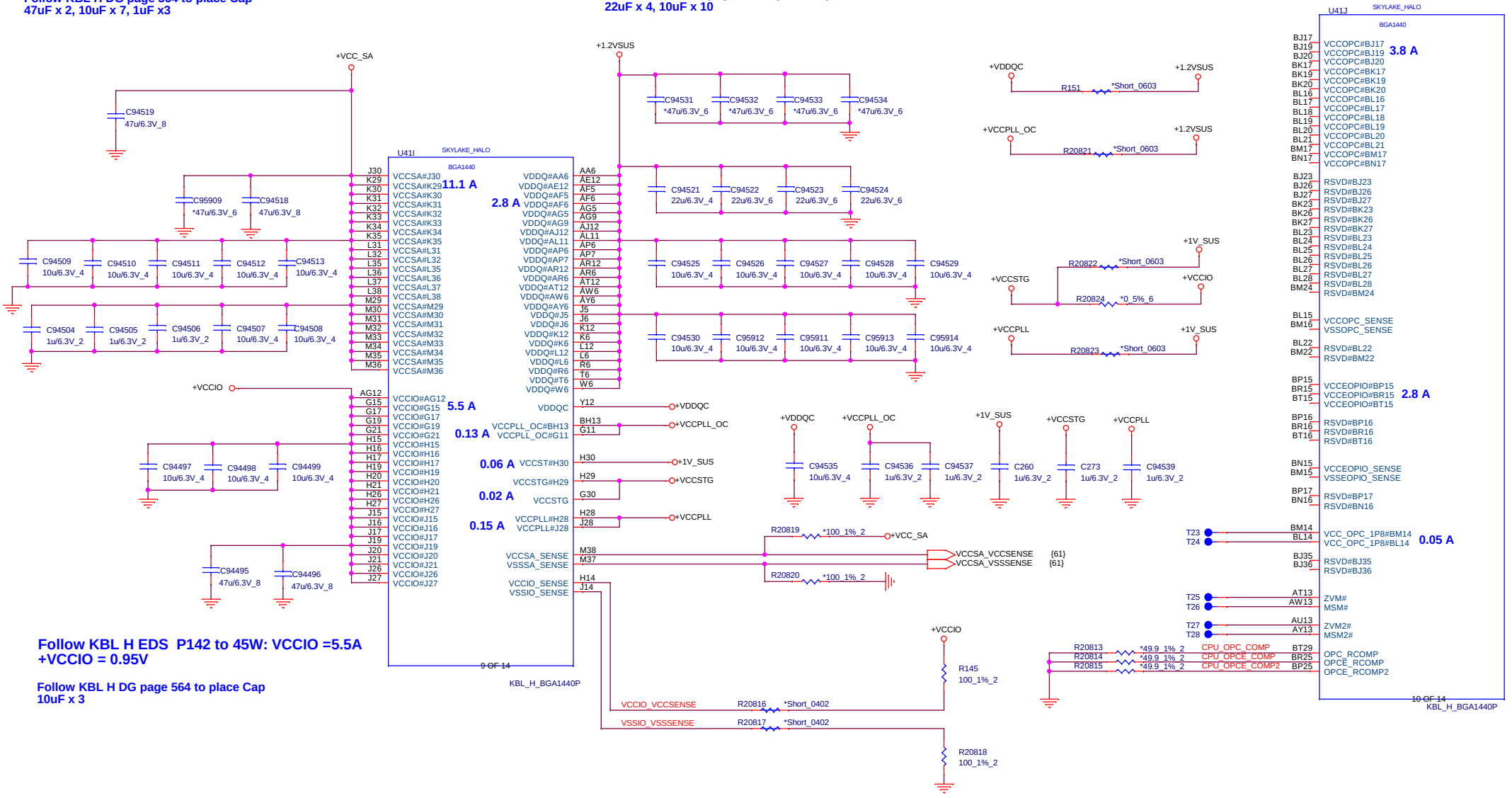
Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Kabylake 4/7 (POWER)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 5 of 72	

Follow KBL H EDS page 141 to 45W(GT2): VCCSA=11.1A

Follow KBL H DG page 564 to place Cap
47uF x 2, 10uF x 7, 1uF x3

Follow KBL H EDS page 141 45W: VDDQ=2.8A

Follow KBL H DG page 564 to place Cap
22uF x 4, 10uF x 10



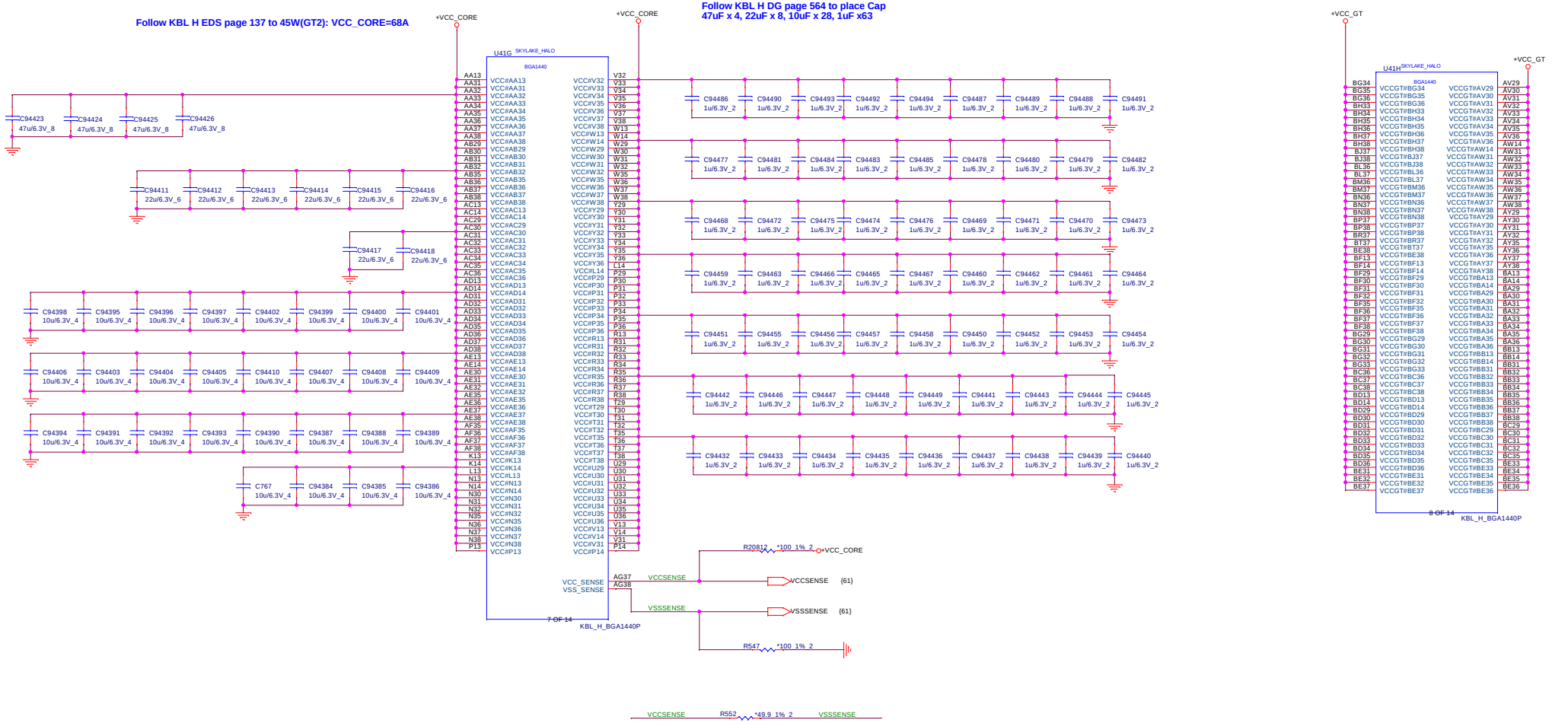
Follow KBL H EDS P142 to 45W: VCCIO =5.5A
+VCCIO = 0.95V

Follow KBL H DG page 564 to place Cap
10uF x 3

Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Kabylake 5/7 (POWER & GND)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 6 of 72	

Follow KBL H EDS page 137 to 45W(GT2): VCC_CORE=68A

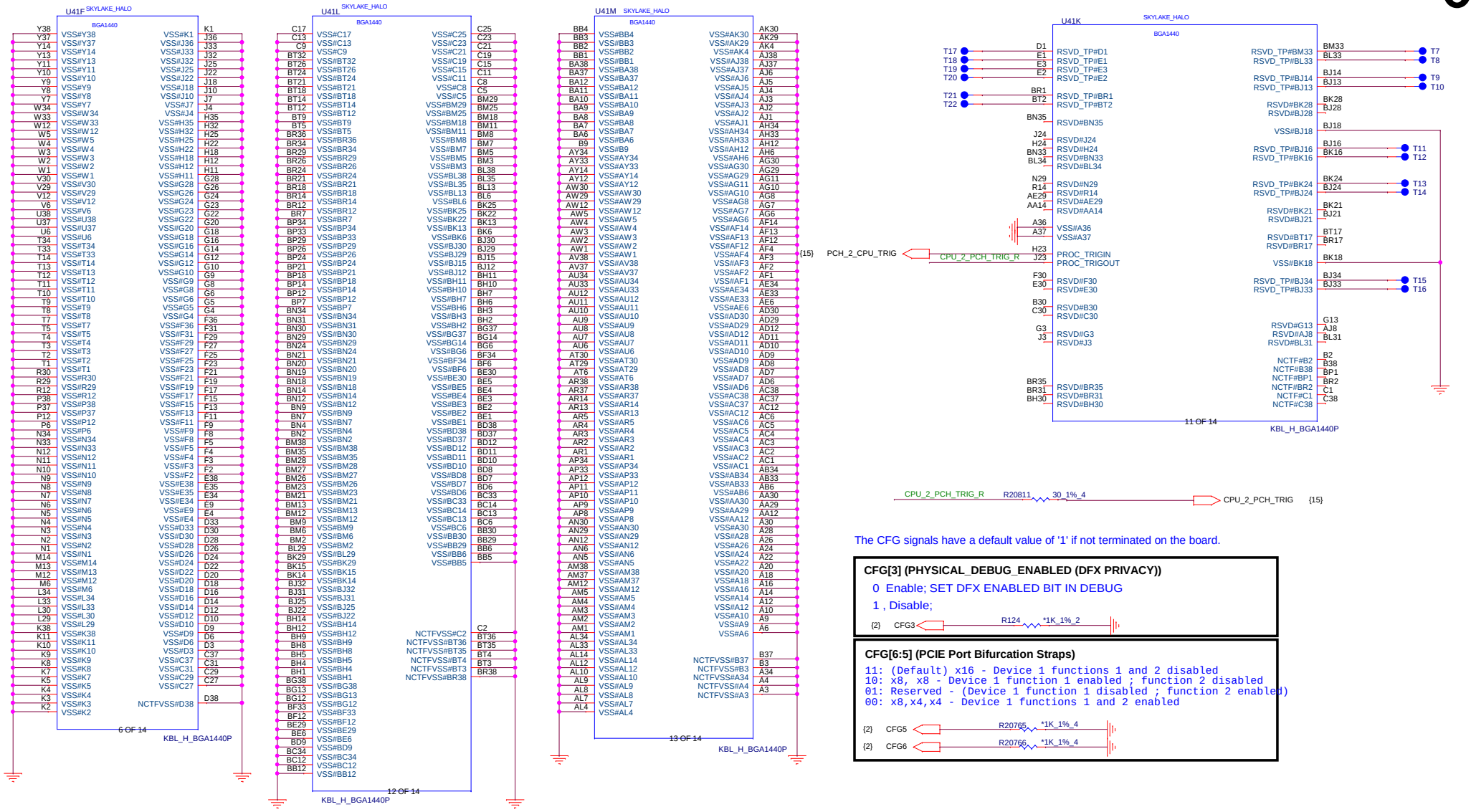
Follow KBL H DG page 564 to place Cap
47uF x 4, 22uF x 8, 10uF x 28, 1uF x63



Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	Kabylake 6/7 (POWER & GND)	1A

Date: Thursday, July 06, 2017 Sheet 7 of 72



The CFG signals have a default value of '1' if not terminated on the board.

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

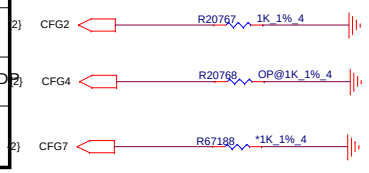
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

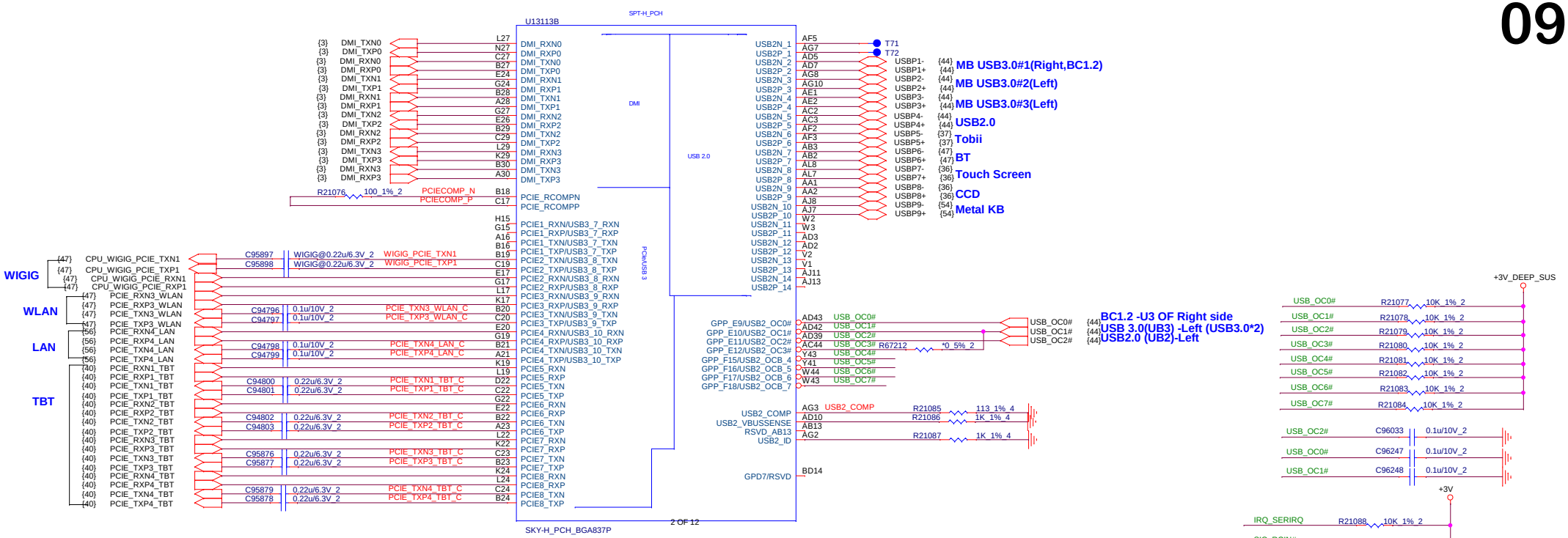
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Training)	PEG train immediately following xxRESETB de assertion (Default)	PEG wait for BIOS training

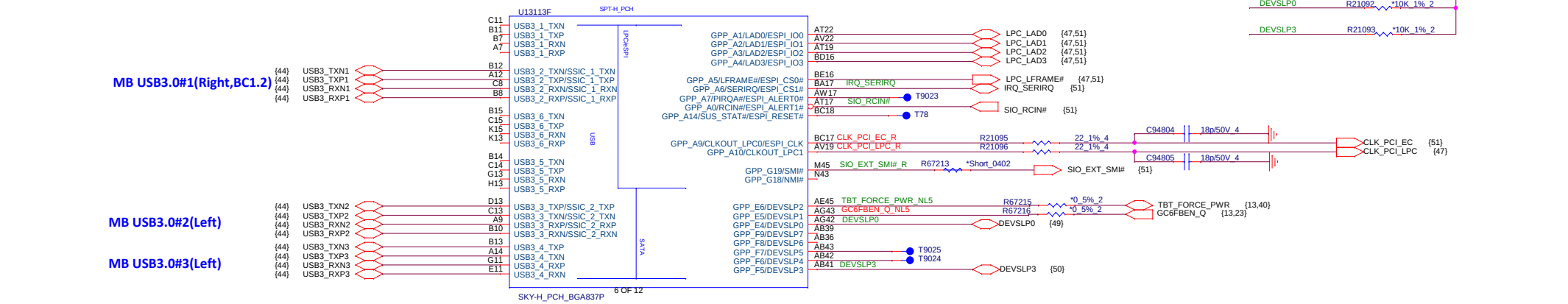


Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	Kabylake 7/7 (GND)	1A

Date: Thursday, July 06, 2017 Sheet 8 of 72





Quanta Computer Inc.	
PROJECT : ZGL	
Size	Document Number: PCH 1/7 (DMI/FDI/VIDEO) — Rev: 1A
Date: Thursday, July 06, 2017	Sheet 9 of 72

HDA Bus(CLG)

0 = *Enable security in the Flash Description (iPD 20K)
1 = Disable Flash Descriptor Security (Override)

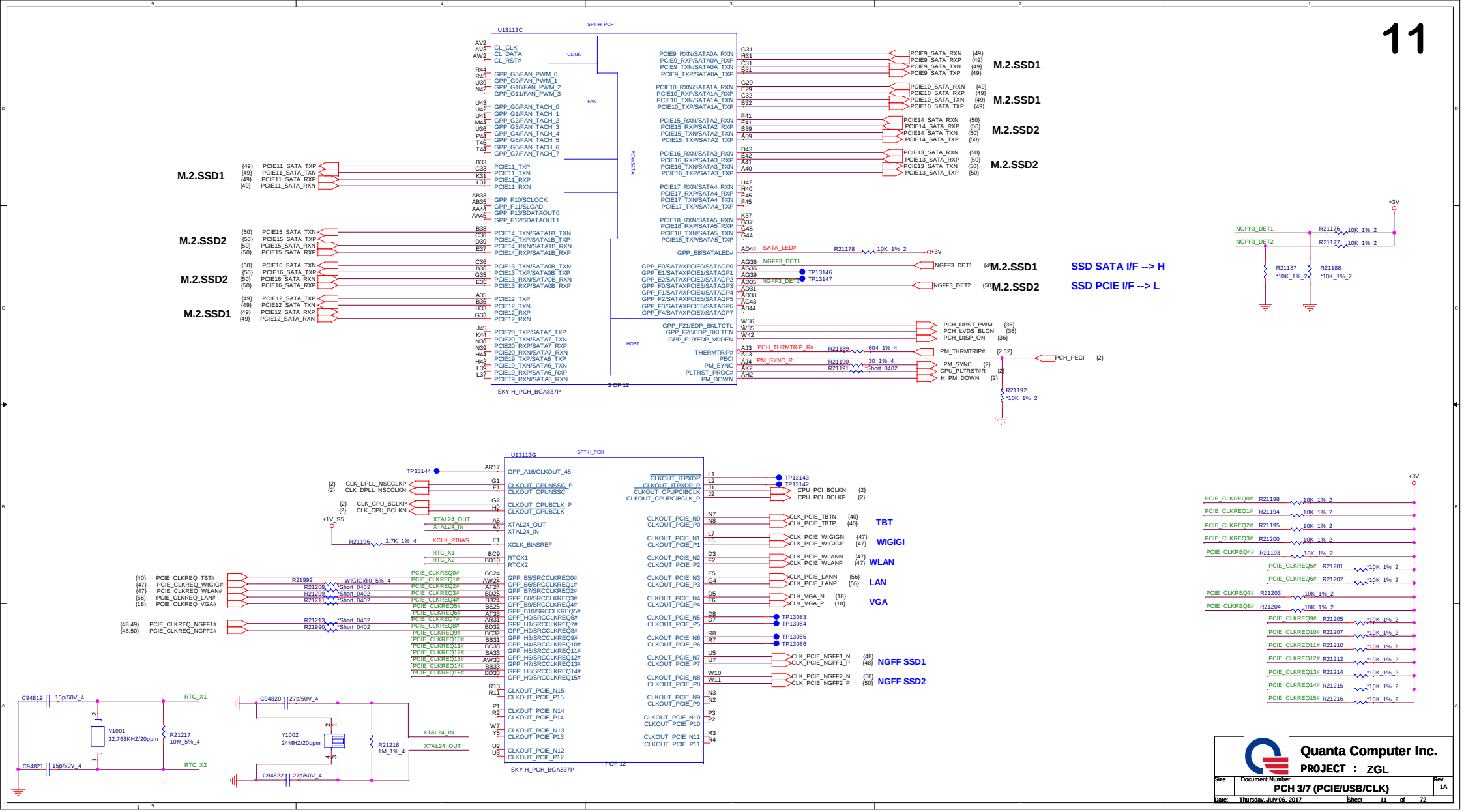
EC reset RTC

RTC Circuitry (RTC)

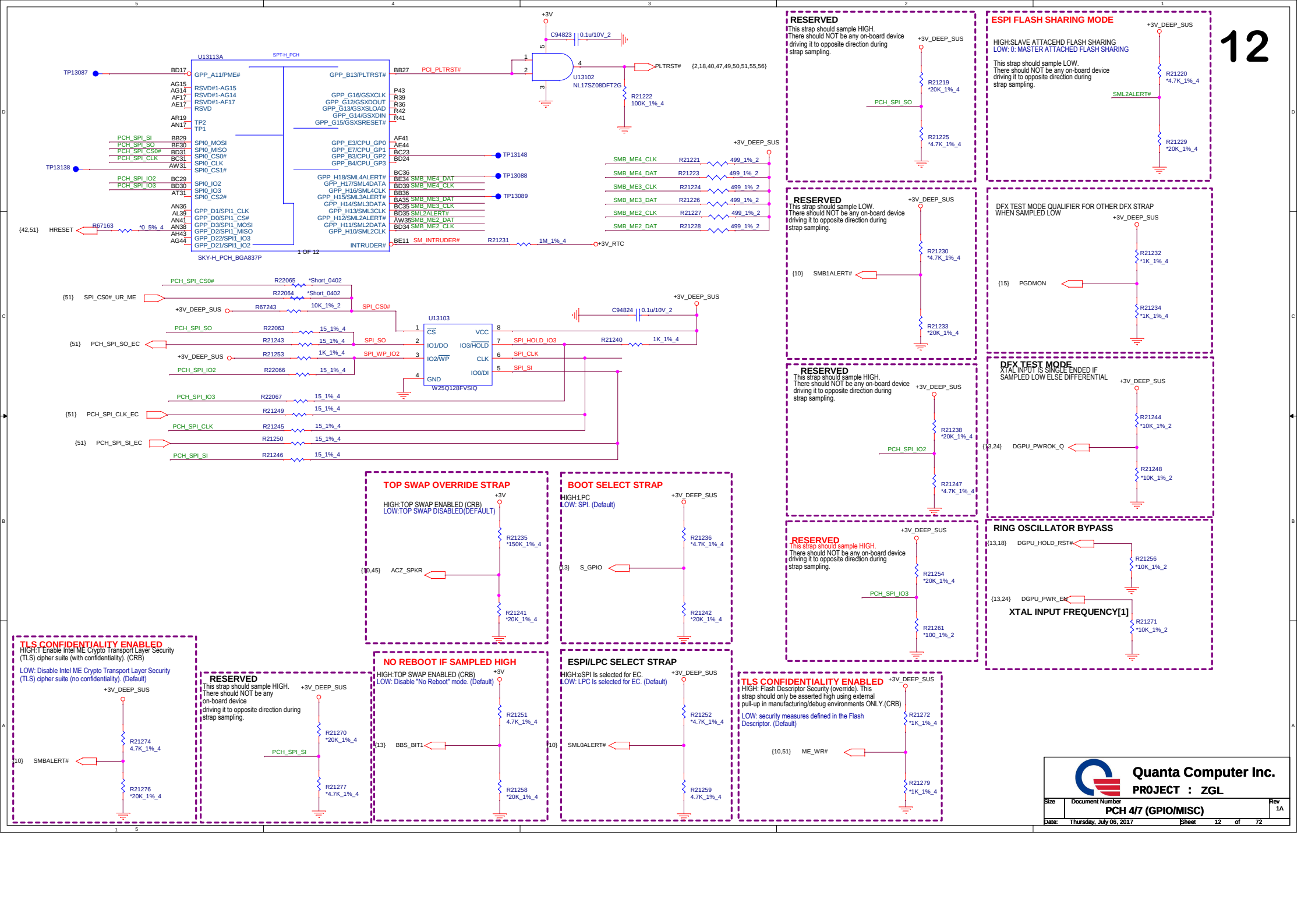
On SKL voltage at VCCRTC does not exceed 3.2V

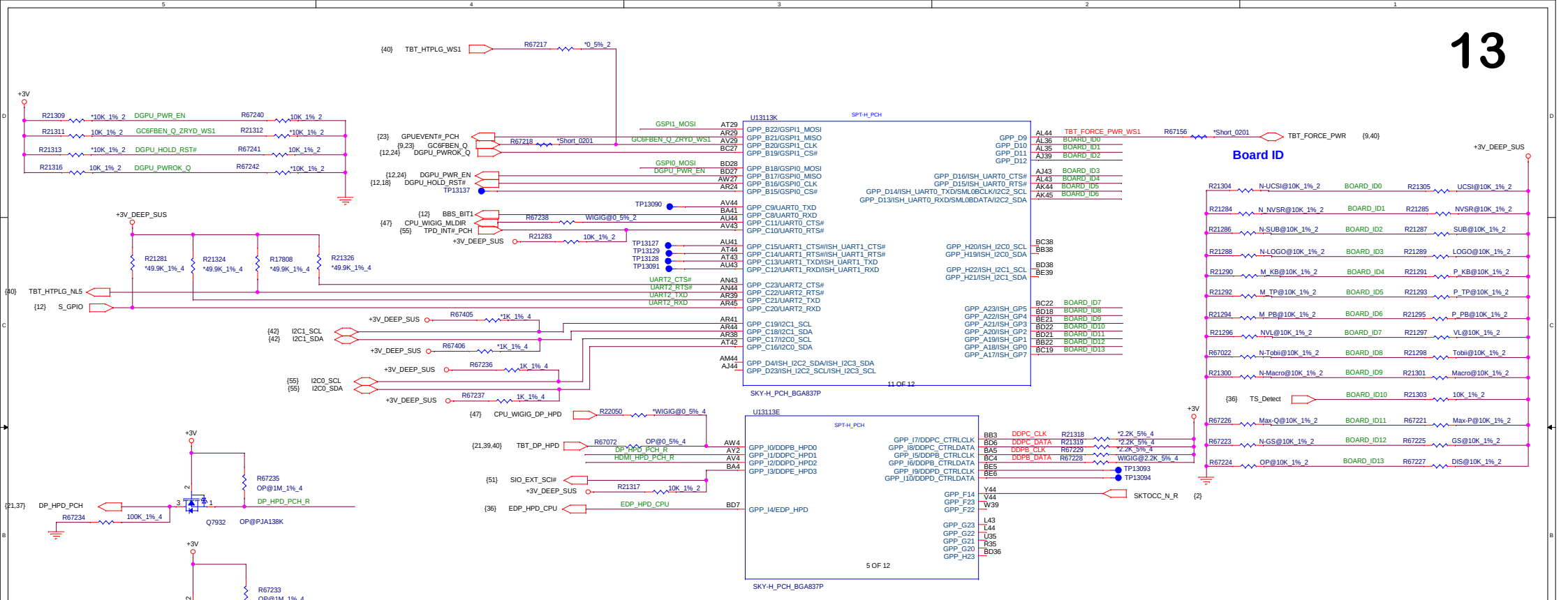
SYSPWOK

Quanta Computer Inc.
PROJECT : ZGL
Size | Document Number: PCH 2/7 (SATA/HDA/SPI) | Rev 1A
Date: Thursday, July 06, 2017 | Sheet 10 of 72



Quanta Computer Inc.	
PROJECT : ZGL	
Size	Document Number: PCH 3/7 (PCIE/USB/CLK) — Rev: 1A
Date: Thursday, July 06, 2017	Sheet 11 of 72


12
U13113A
SPT-H_PCH
SKY-H_PCH_BGA837P
1 OF 12
TP13087
TP13138
{42,51} HRESET
R67163 *0_5%_4
PCH_SPI_SI
PCH_SPI_SO
PCH_SPI_CS0#
PCH_SPI_CLK
PCH_SPI_IO2
PCH_SPI_IO3
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_A11/PME#
RSVD#1-AG15
RSVD#1-AG14
RSVD#1-AF17
RSVD
TP2
TP1
GPP_D1/SPI1_CLK
GPP_D0/SPI1_CS#
GPP_D3/SPI1_MOSI
GPP_D2/SPI1_MISO
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
GPP_B13/PLTRST#
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXSRESET#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
BB27 PCI_PLTRST#
PLTRST# {2,18,40,47,49,50,51,55,56}
U13102
NL17SZ08DFT2G
C94823 0.1u/10V_2
R21222 100K_1%_4
TP13148
TP13088
TP13089
BE11 SM_INTRUDER#
R21231 1M_1%_4
+3V_RTC
+3V_DEEP_SUS
SMB_ME4_CLK R21221 499_1%_2
SMB_ME4_DAT R21223 499_1%_2
SMB_ME3_CLK R21224 499_1%_2
SMB_ME3_DAT R21226 499_1%_2
SMB_ME2_CLK R21227 499_1%_2
SMB_ME2_DAT R21228 499_1%_2
PCH_SPI_CS0# R22065 *Short_0402
{51} SPI_CS0#_UR_ME R22064 *Short_0402
+3V_DEEP_SUS R67243 10K_1%_2
SPI_CS0#
U13103
W25Q128FVSIQ
C94824 0.1u/10V_2
PCH_SPI_SO R22063 15_1%_4
{51} PCH_SPI_SO_EC R21243 15_1%_4
SPI_SO
+3V_DEEP_SUS R21253 1K_1%_4
SPI_WP_IO2
PCH_SPI_IO2 R22066 15_1%_4
R21240 1K_1%_4
SPI_HOLD_IO3
SPI_CLK
SPI_SI
PCH_SPI_IO3 R22067 15_1%_4
{51} PCH_SPI_CLK_EC R21249 15_1%_4
PCH_SPI_CLK R21245 15_1%_4
{51} PCH_SPI_SI_EC R21250 15_1%_4
PCH_SPI_SI R21246 15_1%_4
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.
R21219 *20K_1%_4
R21225 *4.7K_1%_4
ESPI FLASH SHARING MODE
HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.
SML2ALERT#
R21220 *4.7K_1%_4
R21229 *20K_1%_4
RESERVED
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.
{10} SMB1ALERT#
R21230 *4.7K_1%_4
R21233 *20K_1%_4
DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW
{15} PGDMON
R21232 *1K_1%_4
R21234 *1K_1%_4
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.
PCH_SPI_IO2
R21238 *20K_1%_4
R21247 *4.7K_1%_4
DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL
{13,24} DGPU_PWROK_Q
R21244 *10K_1%_2
R21248 *10K_1%_2
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.
PCH_SPI_IO3
R21254 *20K_1%_4
R21261 *100_1%_2
RING OSCILLATOR BYPASS
{13,18} DGPU_HOLD_RST#
R21256 *10K_1%_2
{13,24} DGPU_PWR_EN
XTAL INPUT FREQUENCY[1]
R21271 *10K_1%_2
TOP SWAP OVERRIDE STRAP
HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)
{10,45} ACZ_SPKR
R21235 *150K_1%_4
R21241 *20K_1%_4
BOOT SELECT STRAP
HIGH:LPC
LOW: SPI. (Default)
{13} S_GPIO
R21236 *4.7K_1%_4
R21242 *20K_1%_4
TLS CONFIDENTIALITY ENABLED
HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
{10} SMBALERT#
R21274 4.7K_1%_4
R21276 *20K_1%_4
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.
PCH_SPI_SI
R21270 *20K_1%_4
R21277 *4.7K_1%_4
NO REBOOT IF SAMPLED HIGH
HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)
{13} BBS_BIT1
R21251 4.7K_1%_4
R21258 *20K_1%_4
ESPI/LPC SELECT STRAP
HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)
{10} SML0ALERT#
R21252 *4.7K_1%_4
R21259 4.7K_1%_4
TLS CONFIDENTIALITY ENABLED
HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)
LOW: security measures defined in the Flash Descriptor. (Default)
{10,51} ME_WR#
R21272 *1K_1%_4
R21279 *1K_1%_4
Quanta Computer Inc.
PROJECT : ZGL
Size
Document Number
PCH 4/7 (GPIO/MISC)
Rev 1A
Date: Thursday, July 06, 2017
Sheet 12 of 72



ID.NO	Function	Low	High
BOARD_ID11	PCB	MAXQ	MAXP
BOARD_ID12	G-SYNC	Non-GS	GS
BOARD_ID13	VGA	Optimus	d-VGA

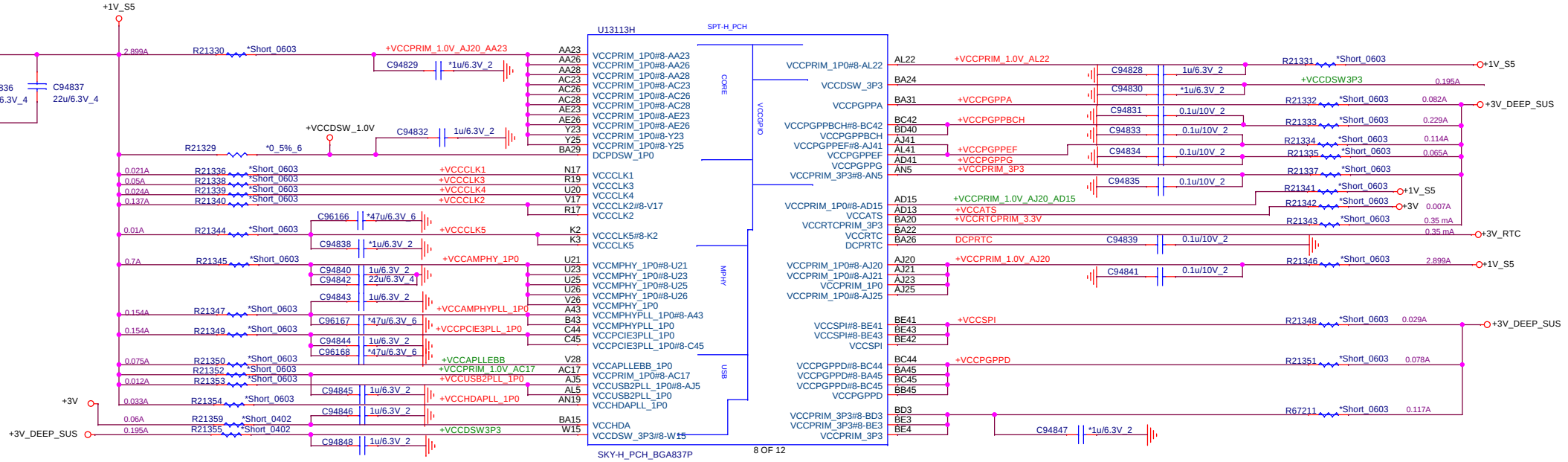
ID.NO	Function	Low	High
BOARD_ID8	EYE Trace	NO	YES
BOARD_ID9	Macro/K	NO	YES
BOARD_ID10	Touch Panel	YES	NO

ID.NO	Function	Low	High
BOARD_ID4	Keyboard	Metal	Plastic
BOARD_ID5	Touch PAD	Metal	Plastic
BOARD_ID6	Power Button	Metal	Plastic
BOARD_ID7	Battery Vin Boost	NO	YES

ID.NO	Function	Low	High
BOARD_ID0	UCSI	No	YES
BOARD_ID1	NVSR	No	YES
BOARD_ID2	Sub-Woofer	No	YES
BOARD_ID3	A-Cover LED	No	YES

Pin Name	Strap description	Sampled	Configuration	note
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R21327 *1K_1%_4 GSPI0_MOSI
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R21328 *1K_1%_4 GSPI1_MOSI

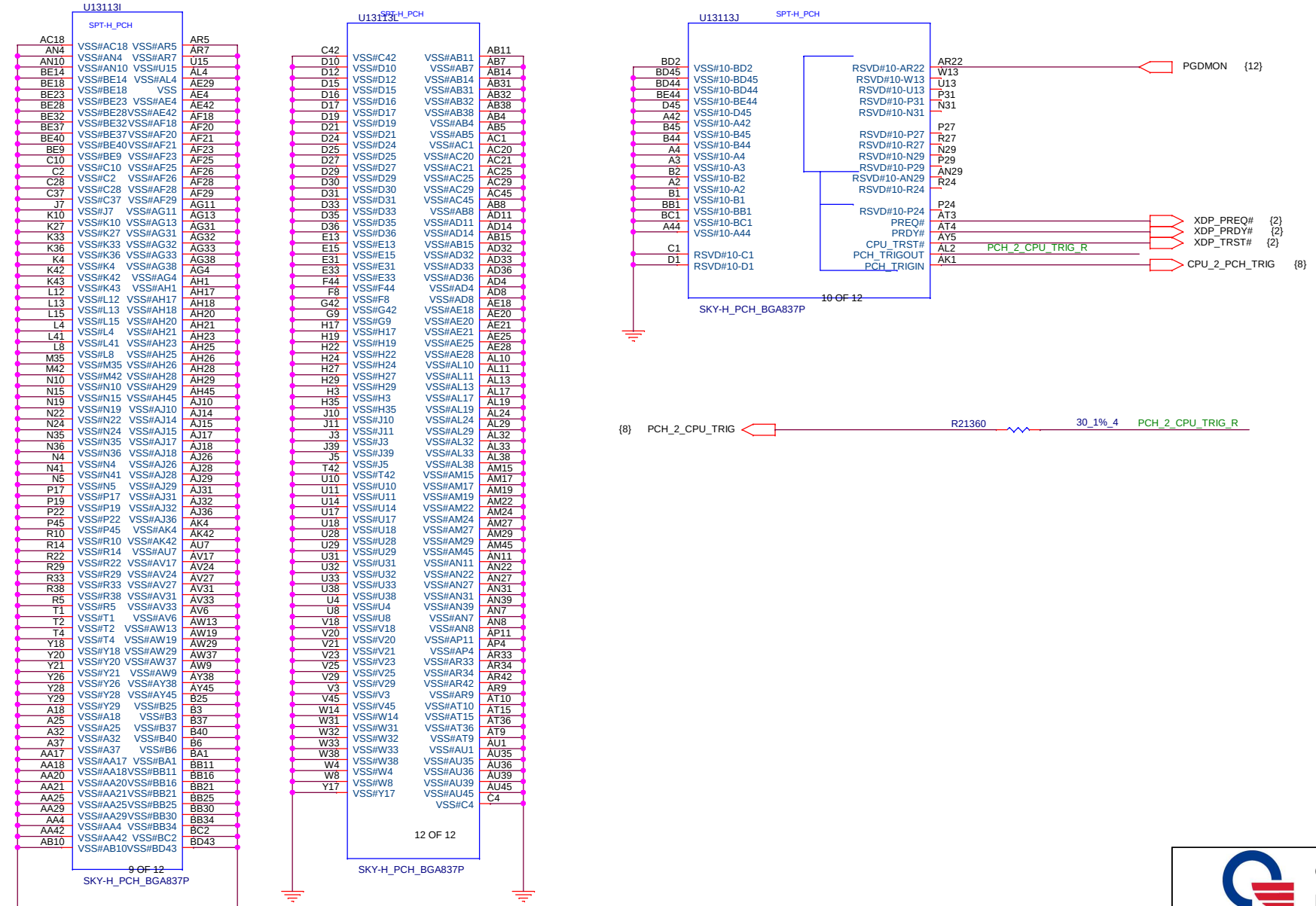
Quanta Computer Inc.
PROJECT : ZGL
Size | Document Number: PCH 5/7 (GPIO/MISC) | Rev: 1A
Date: Monday, July 10, 2017 | Sheet 13 of 72



Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	PCH 6/7 (POWER)	1A

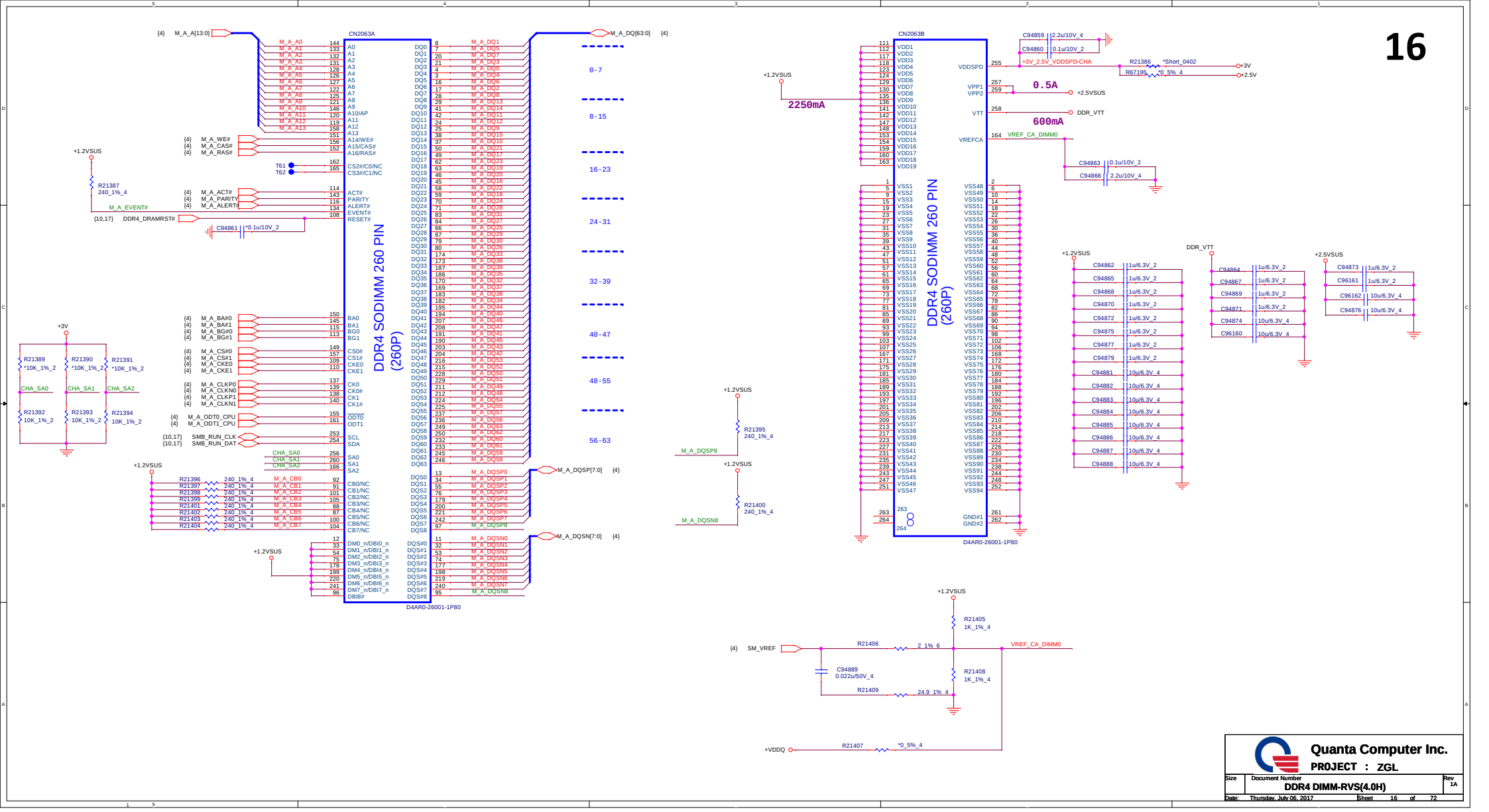
Date: Thursday, July 06, 2017 Sheet 14 of 72



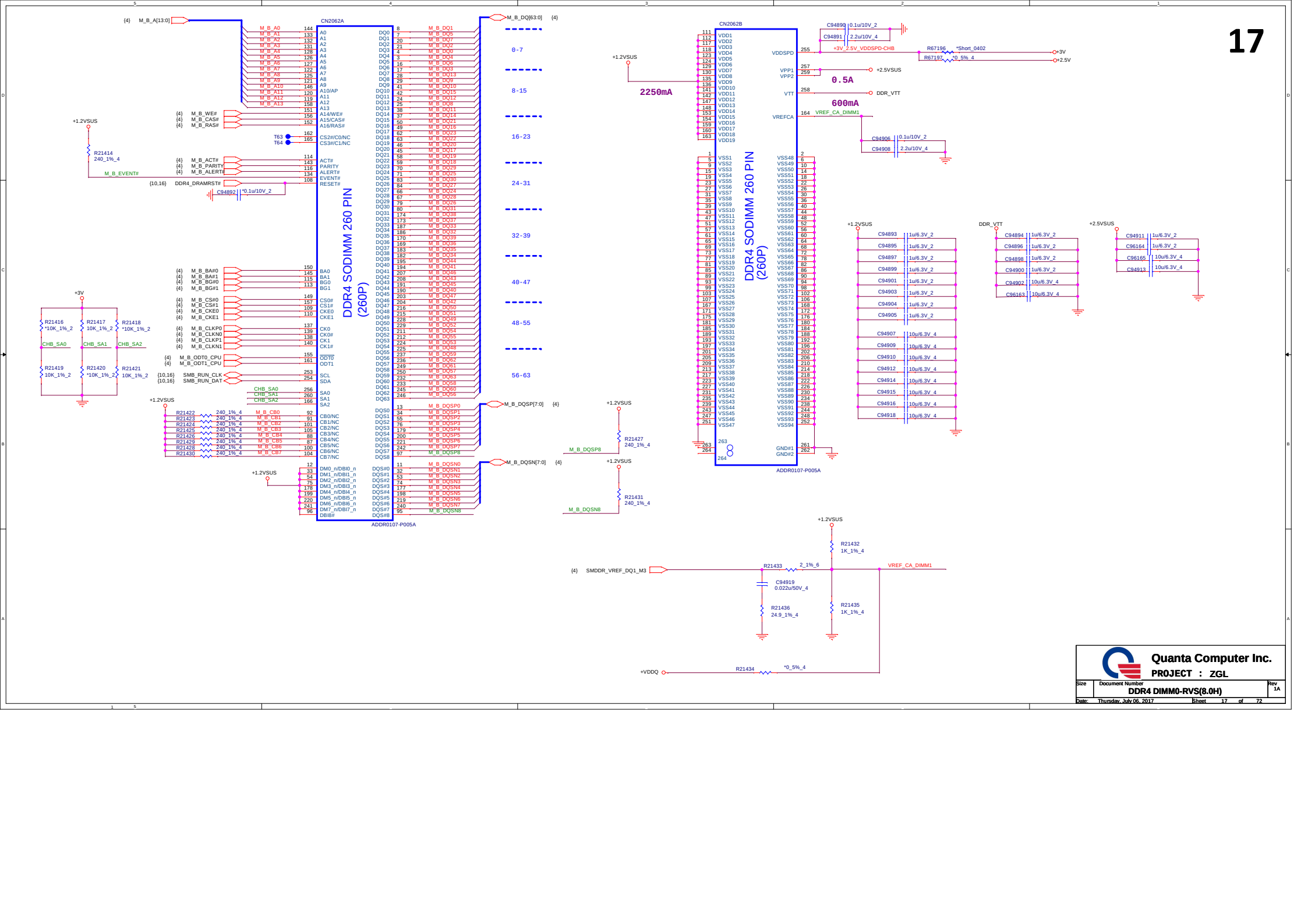
Quanta Computer Inc.

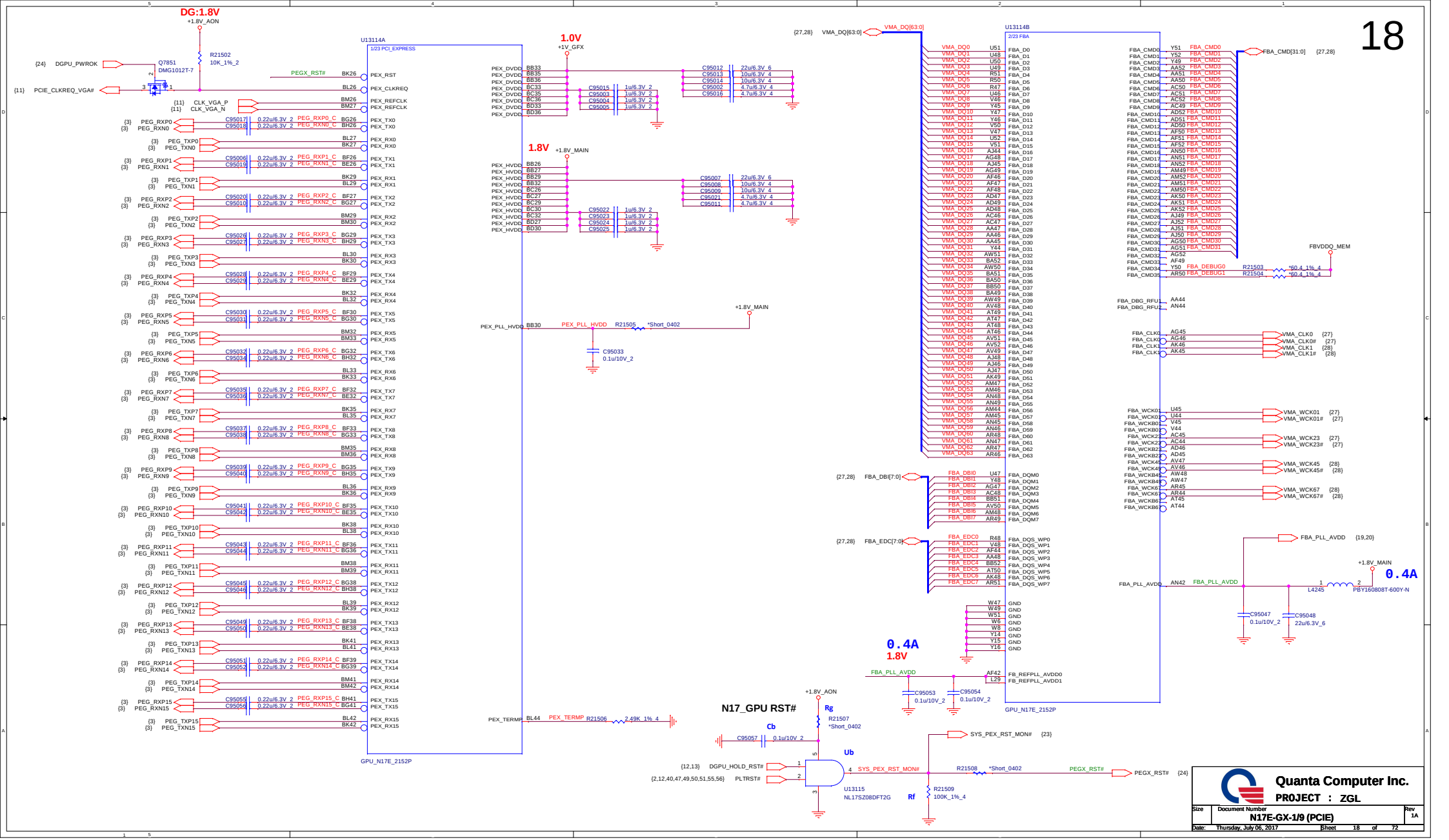
PROJECT : ZGL

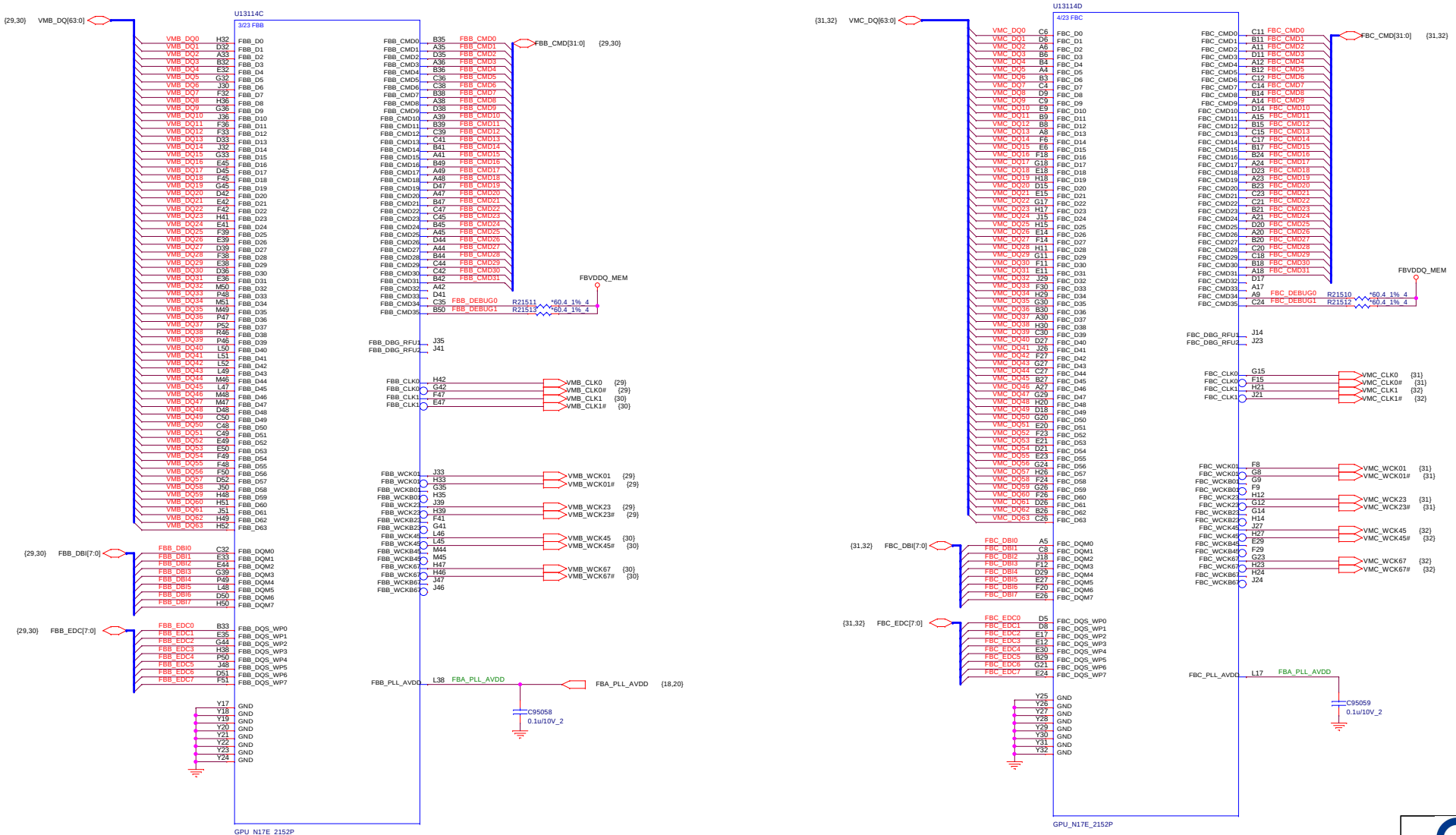
Size	Document Number	Rev
	PCH 7/7 (GND)	1A
Date: Thursday, July 06, 2017	Sheet 15 of 72	



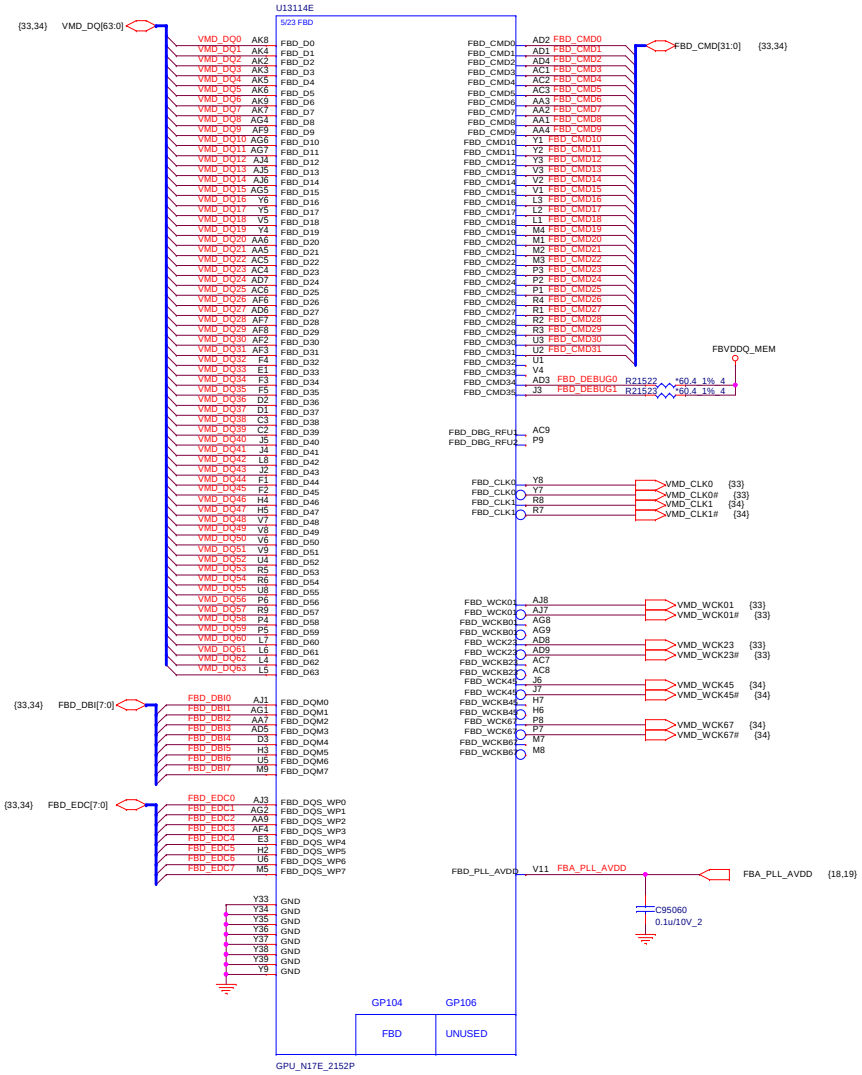
Quanta Computer Inc.			
PROJECT : ZGL			
Size	Document Number		Rev
	DDR4 DIMM-RVS(4.0H)		1A
Date: Thursday, July 06, 2017	Sheet 16 of 72		


CN2062A
DDR4 SODIMM 260 PIN (260P)
ADDR0107-P005A
CN2062B
DDR4 SODIMM 260 PIN (260P)
ADDR0107-P005A
2250mA
0.5A
600mA
0-7
8-15
16-23
24-31
32-39
40-47
48-55
56-63
Quanta Computer Inc.
PROJECT : ZGL
DDR4 DIMM0-RVS(8.0H)
Thursday, July 06, 2017
17


DG:1.8V
+1.8V_AON
R21502
10K_1%_2
{24} DGPU_PWROK
Q7851
DMG1012T-7
{11} PCIE_CLKREQ_VGA#
PEGX_RST#
{11} CLK_VGA_P
{11} CLK_VGA_N
U13114A
1/23 PCI_EXPRESS
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK
PEX_TX0
PEX_RX0
PEX_TX1
PEX_RX1
PEX_TX2
PEX_RX2
PEX_TX3
PEX_RX3
PEX_TX4
PEX_RX4
PEX_TX5
PEX_RX5
PEX_TX6
PEX_RX6
PEX_TX7
PEX_RX7
PEX_TX8
PEX_RX8
PEX_TX9
PEX_RX9
PEX_TX10
PEX_RX10
PEX_TX11
PEX_RX11
PEX_TX12
PEX_RX12
PEX_TX13
PEX_RX13
PEX_TX14
PEX_RX14
PEX_TX15
PEX_RX15
GPU_N17E_2152P
1.0V
+1V_GFX
1.8V
+1.8V_MAIN
PEX_PLL_HVDD
R21505
*Short_0402
C95033
0.1u/10V_2
PEX_TERMP
R21506
2.49K_1%_4
N17_GPU RST#
Rg
R21507
*Short_0402
Cb
C95057
0.1u/10V_2
Ub
U13115
NL17SZ08DFT2G
Rf
R21509
100K_1%_4
{12,13} DGPU_HOLD_RST#
{2,12,40,47,49,50,51,55,56} PLTRST#
SYS_PEX_RST_MON#
{23}
R21508
*Short_0402
PEGX_RST#
{4}
{27,28} VMA_DQ[63:0]
U13114B
2/23 FBA
{27,28} FBA_DBI[7:0]
{27,28} FBA_EDC[7:0]
0.4A
1.8V
FBA_PLL_AVDD
C95053
0.1u/10V_2
C95054
0.1u/10V_2
GPU_N17E_2152P
FBA_CMD[31:0]
{27,28}
FBVDDQ_MEM
R21503
*60.4_1%_4
R21504
*60.4_1%_4
FBA_DBG_RFU1
FBA_DBG_RFU2
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
VMA_CLK0 {27}
VMA_CLK0# {27}
VMA_CLK1 {28}
VMA_CLK1# {28}
FBA_WCK01
FBA_WCK01#
FBA_WCK23
FBA_WCK23#
FBA_WCK45
FBA_WCK45#
FBA_WCK67
FBA_WCK67#
VMA_WCK01 {27}
VMA_WCK01# {27}
VMA_WCK23 {27}
VMA_WCK23# {27}
VMA_WCK45 {28}
VMA_WCK45# {28}
VMA_WCK67 {28}
VMA_WCK67# {28}
FBA_PLL_AVDD {19,20}
+1.8V_MAIN
0.4A
L4245
PBY160808T-600Y-N
C95047
0.1u/10V_2
C95048
22u/6.3V_6
Quanta Computer Inc.
PROJECT : ZGL
Size
Document Number
N17E-GX-1/9 (PCIE)
Rev
1A
Date: Thursday, July 06, 2017
Sheet 18 of 72



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: N17E-GX-2/9 (Memory)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 19 of 72	



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: N17E-GX-3/9 (Memory)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 20 of 72	

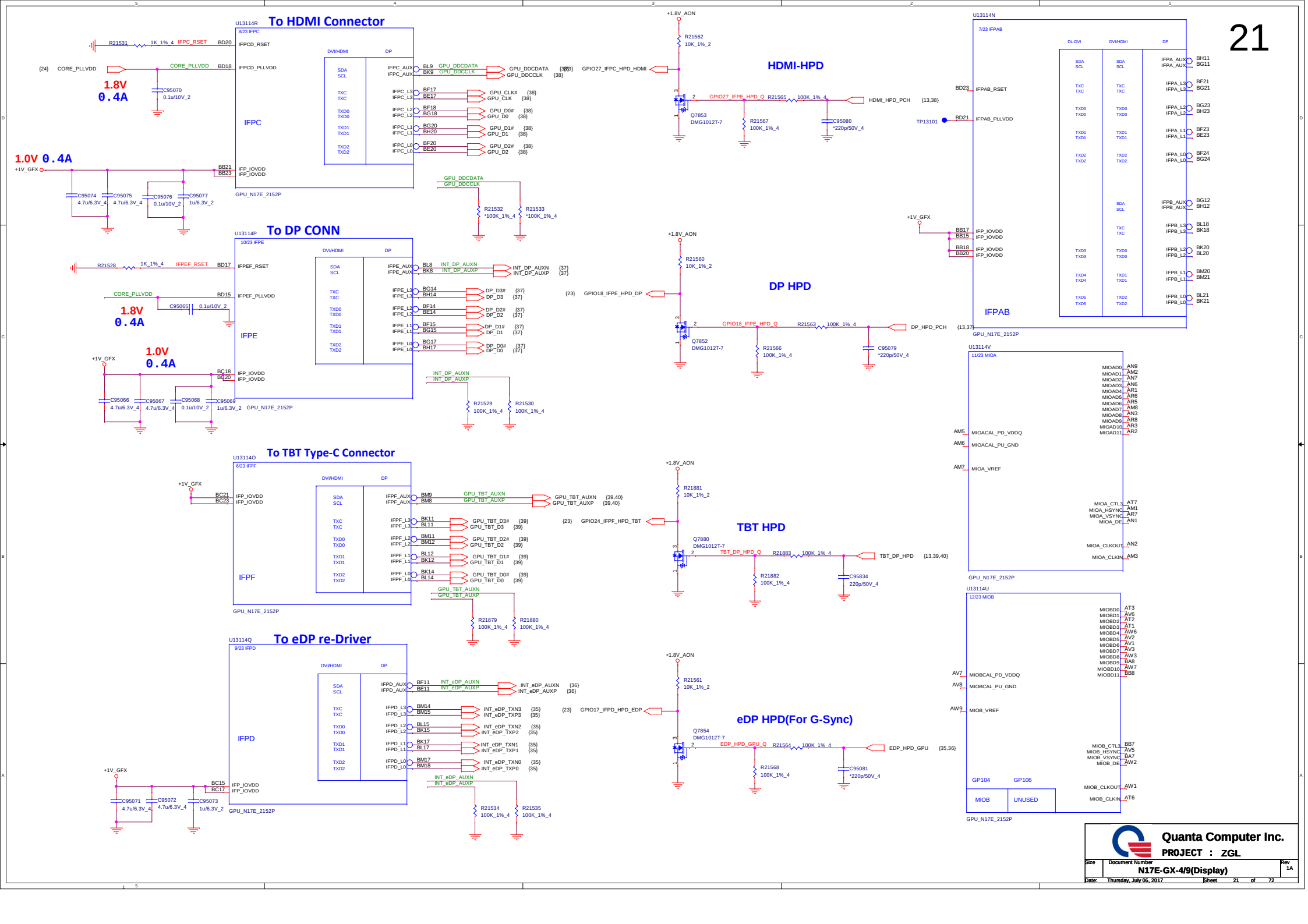

To HDMI Connector
U13114R
8/23 IFPC
IFPC
GPU_N17E_2152P
1.8V 0.4A
1.0V 0.4A
HDMI-HPD
U13114N
7/23 IFPAB
IFPAB
To DP CONN
U13114P
10/23 IFPE
IFPE
DP HPD
To TBT Type-C Connector
U13114O
6/23 IFPF
IFPF
TBT HPD
To eDP re-Driver
U13114Q
9/23 IFPD
IFPD
eDP HPD(For G-Sync)
U13114V
11/23 MIOA
U13114U
12/23 MIOB
GP104
GP106
MIOB
UNUSED

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

VRAM Table

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x0	GDDR5X 256Mx32 8 GHz	Micron A die	MT58k256M32-100:A			

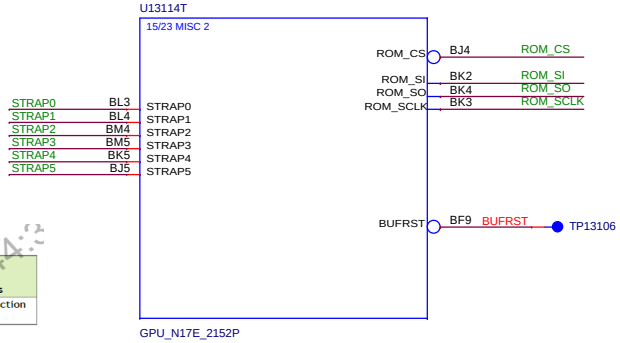
Table 4. N17E-G3 GDDR5X Recommended Memories

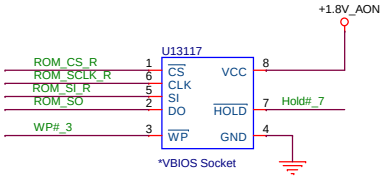
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Micron	MT58K256M32 -100:A	A-die	0x0	10 Gbps	N/A	Full	Production ready

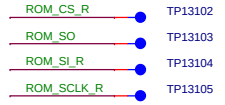
Table 1. N17E-G1/-G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production candidate

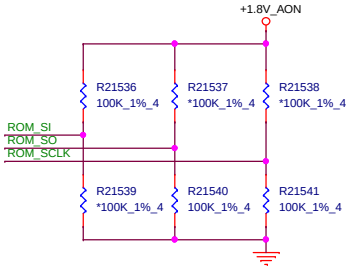
Notes:
1. For N17E-Gx, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

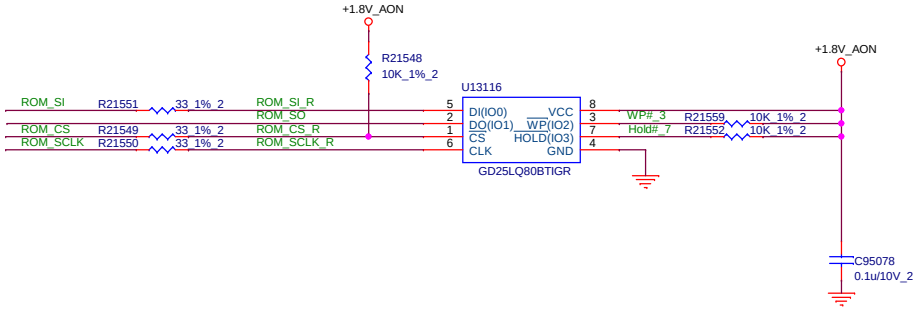


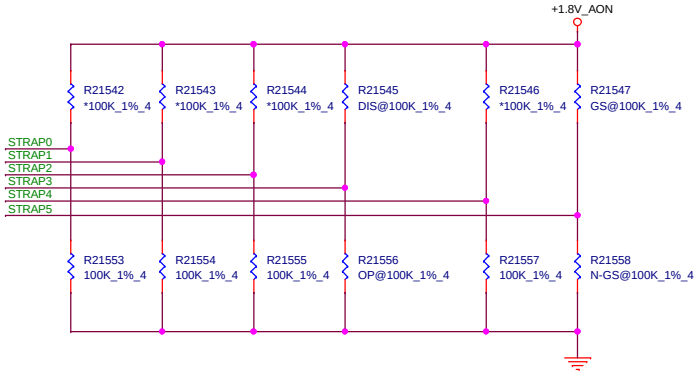




For ICT test



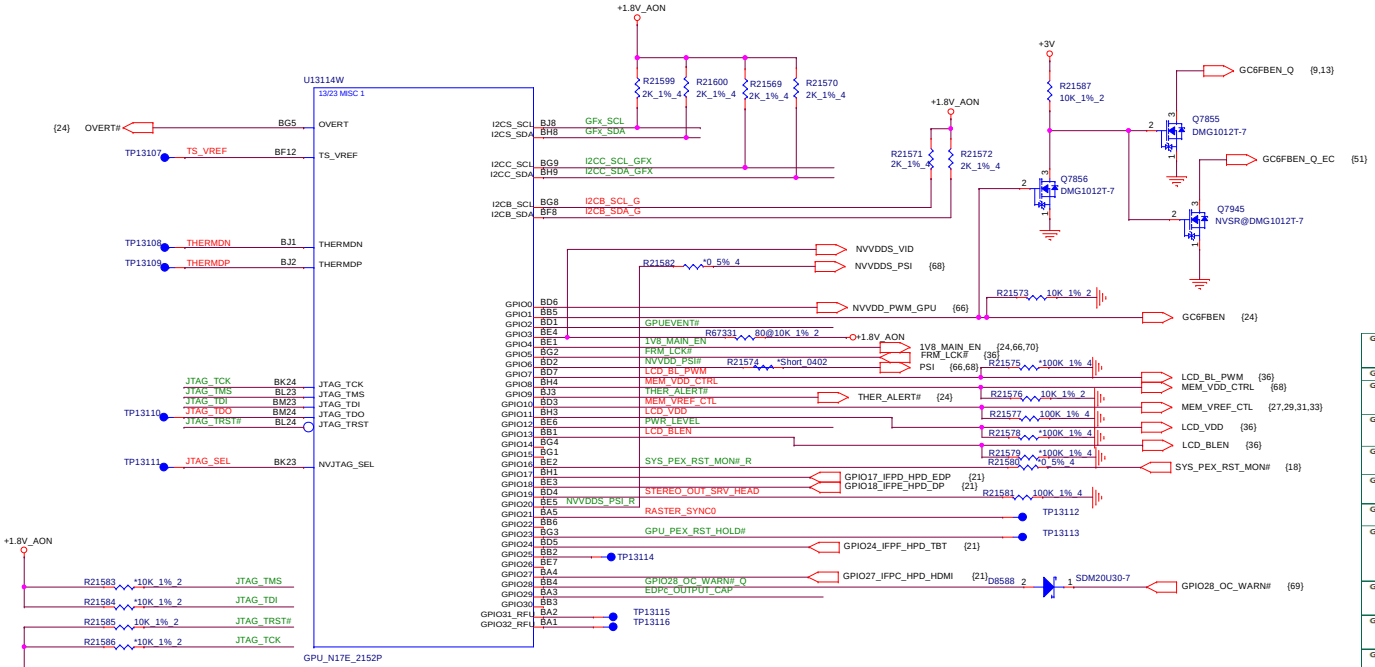


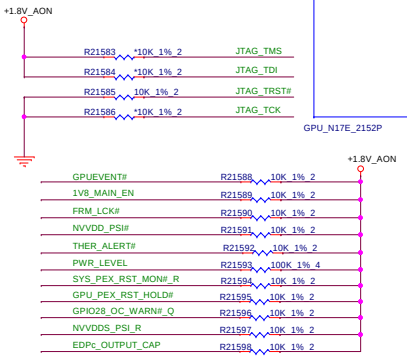


	STRAP5
G-SYNC	100K PU
None G-SYNC	100K PD

Quanta Computer Inc.
PROJECT : ZGL

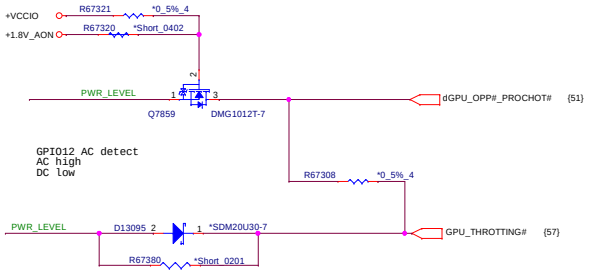
Size	Document Number	Rev
	N17E-GX-5/9(STRAP)	1A
Date: Thursday, July 06, 2017	Sheet 22 of 72	

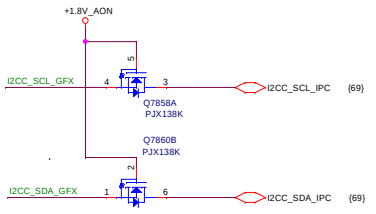




Event

Throttle





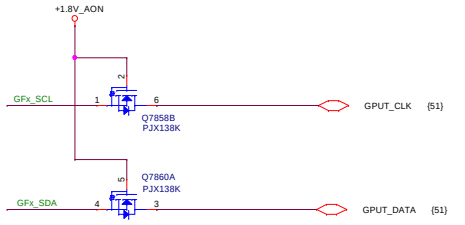


Table 14.3 GPIO Descriptions for GB4-256 Packages

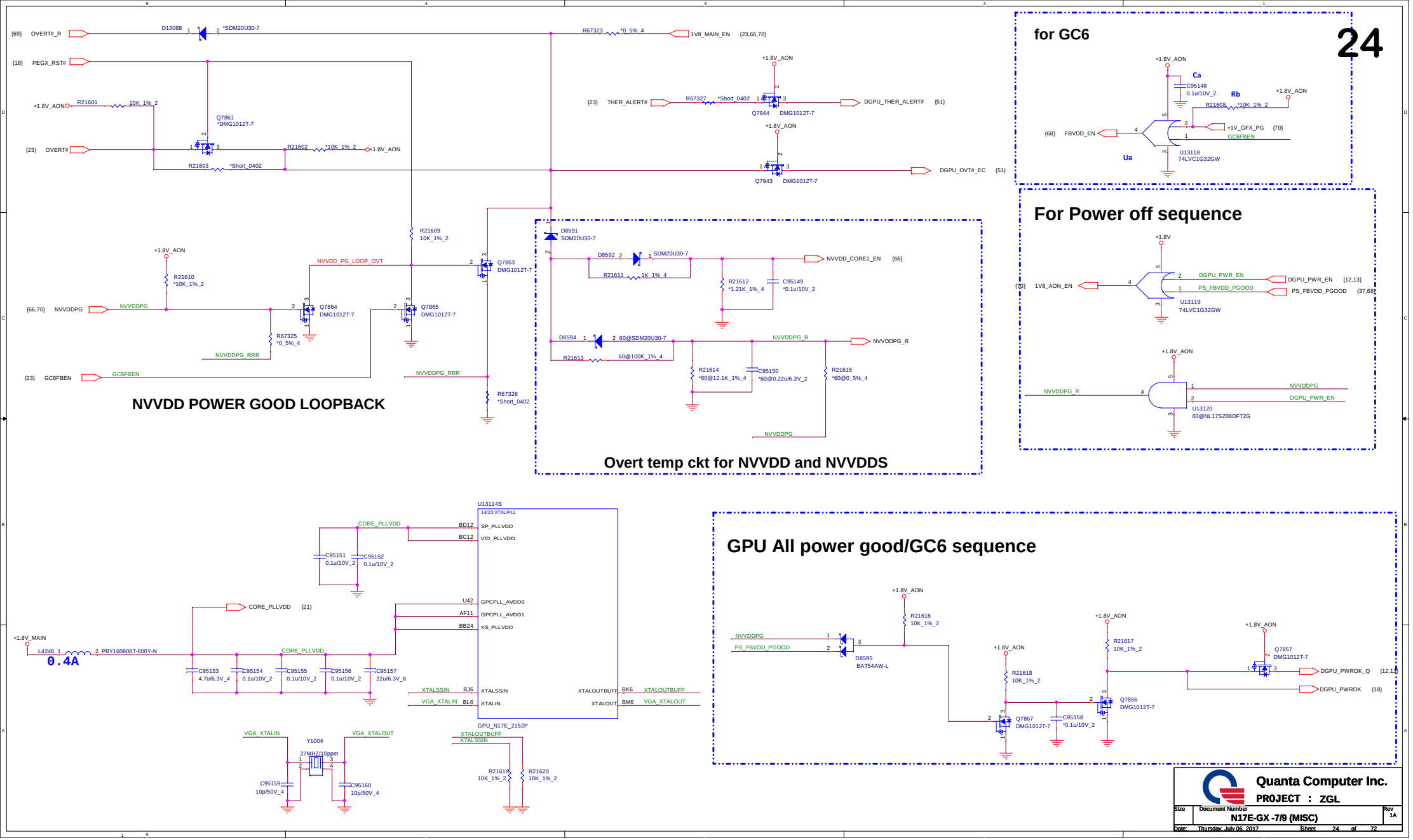
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AOH
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable Control signal to turn on a logo LED	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Turn on heat sink logo LED when present Panel Power enable	10K pull-up to a gated 3V3 100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight EnableFan Tachometer; see Section 14.3.9.	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	PWM output used to control Fan Speed see Section 14.3.9 for definitionSystem side PCIe reset monitor	10K pull-up to a gated 3V3 10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision/STEREO	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	NVVDDS_PSI GC5_MODE			
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI SWAP READY OUT	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset controlInput when master GPU or Output when Slave GPU (SLI with more than 2 boards only)	Open Drain 10 kΩ pull-up to a gated 3V/3100K pull-down
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10kΩ pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	UNUSED	I/O		

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

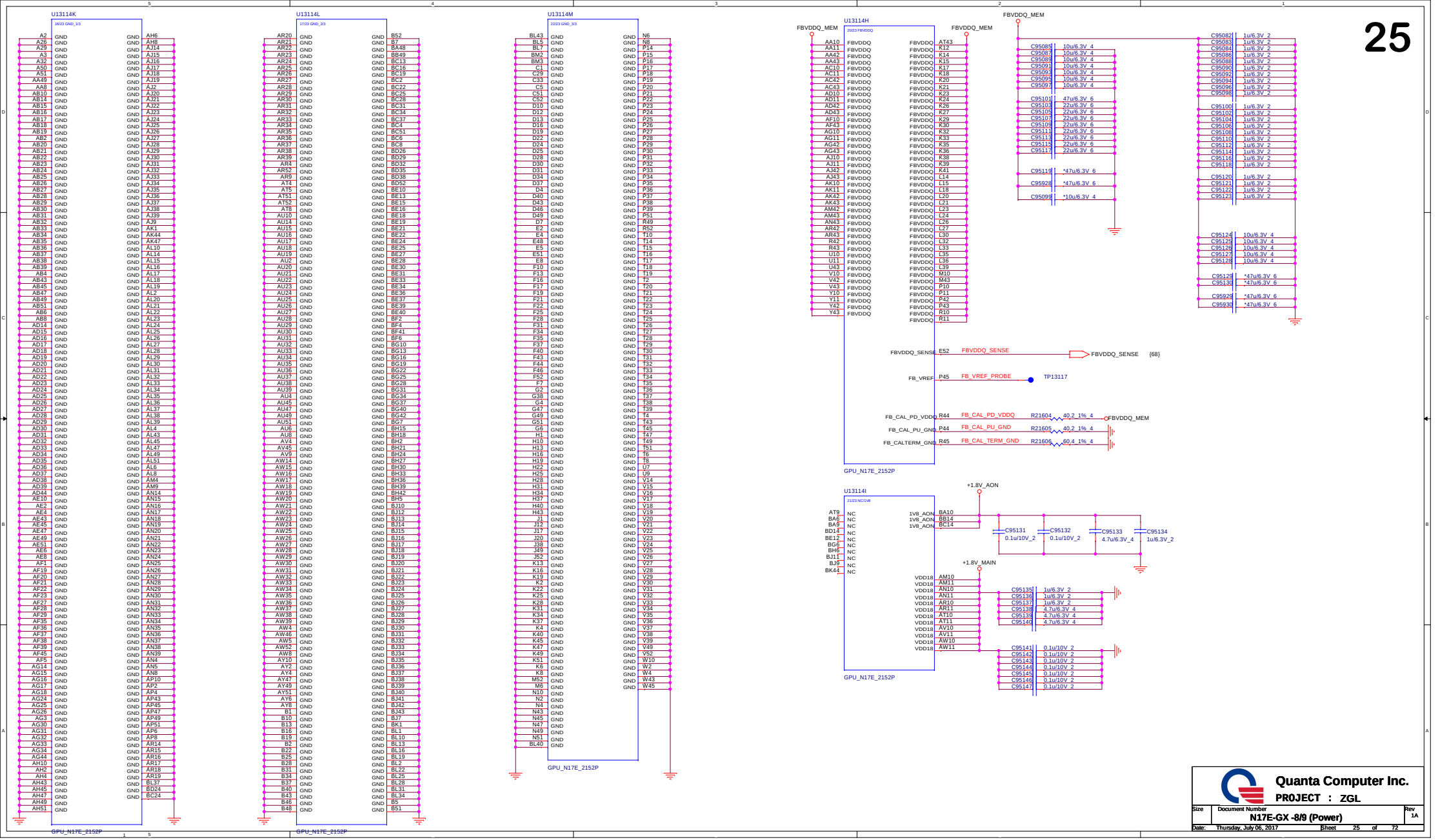
Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX-6/9(GPIO)	1A

Date: Thursday, July 06, 2017 Sheet 23 of 72



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number	Rev
	N17E-GX -7/9 (MISC)	1A
Date: Thursday, July 06, 2017	Sheet 24 of 72	



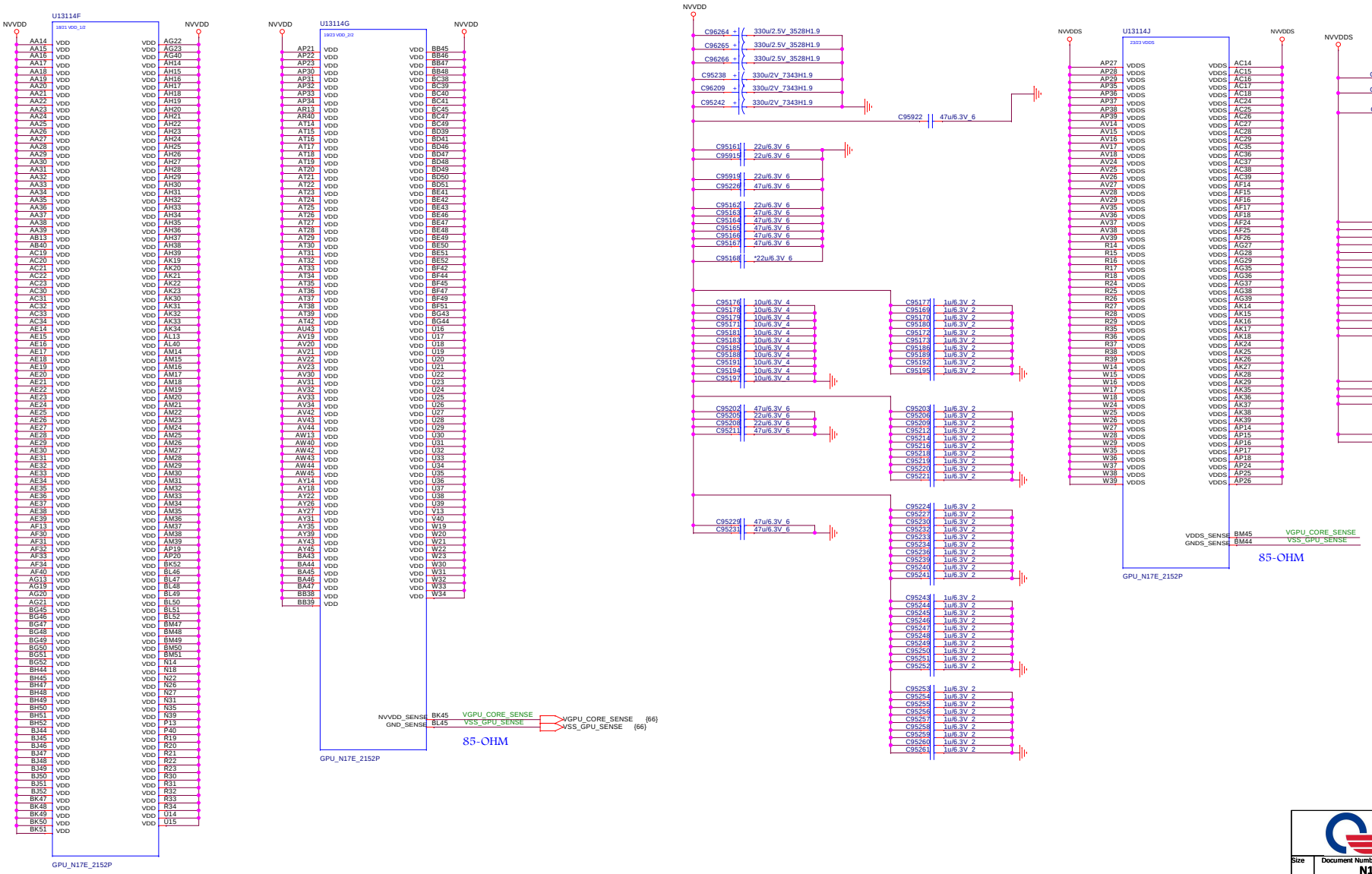
25

Quanta Computer Inc.

PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX -8/9 (Power)	1A

Date: Thursday, July 06, 2017 Sheet 25 of 72



Quanta Computer Inc.	
PROJECT : ZGL	
Size	Document Number: N17E-GX-9/9 (Power) — Rev: 1A
Date: Thursday, July 06, 2017	Sheet 26 of 72

CHANNEL A: GDDR5x (FBA 0-31)

MF=1 mirrored

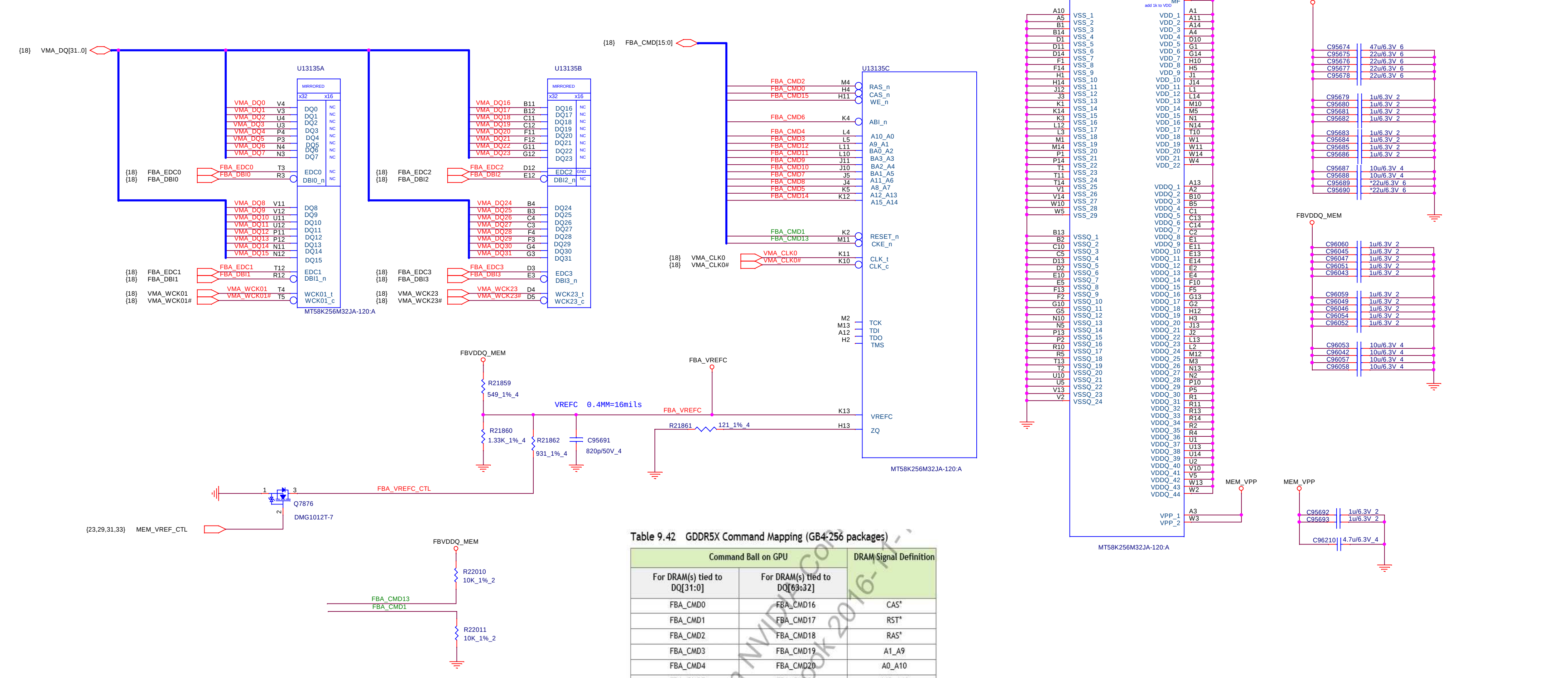


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

Quanta Computer Inc.

PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX-1080-GDDR5X-FBA 0-31	1A

CHANNEL A: GDDR5x (FBA 32-63)

MF=0 Normal

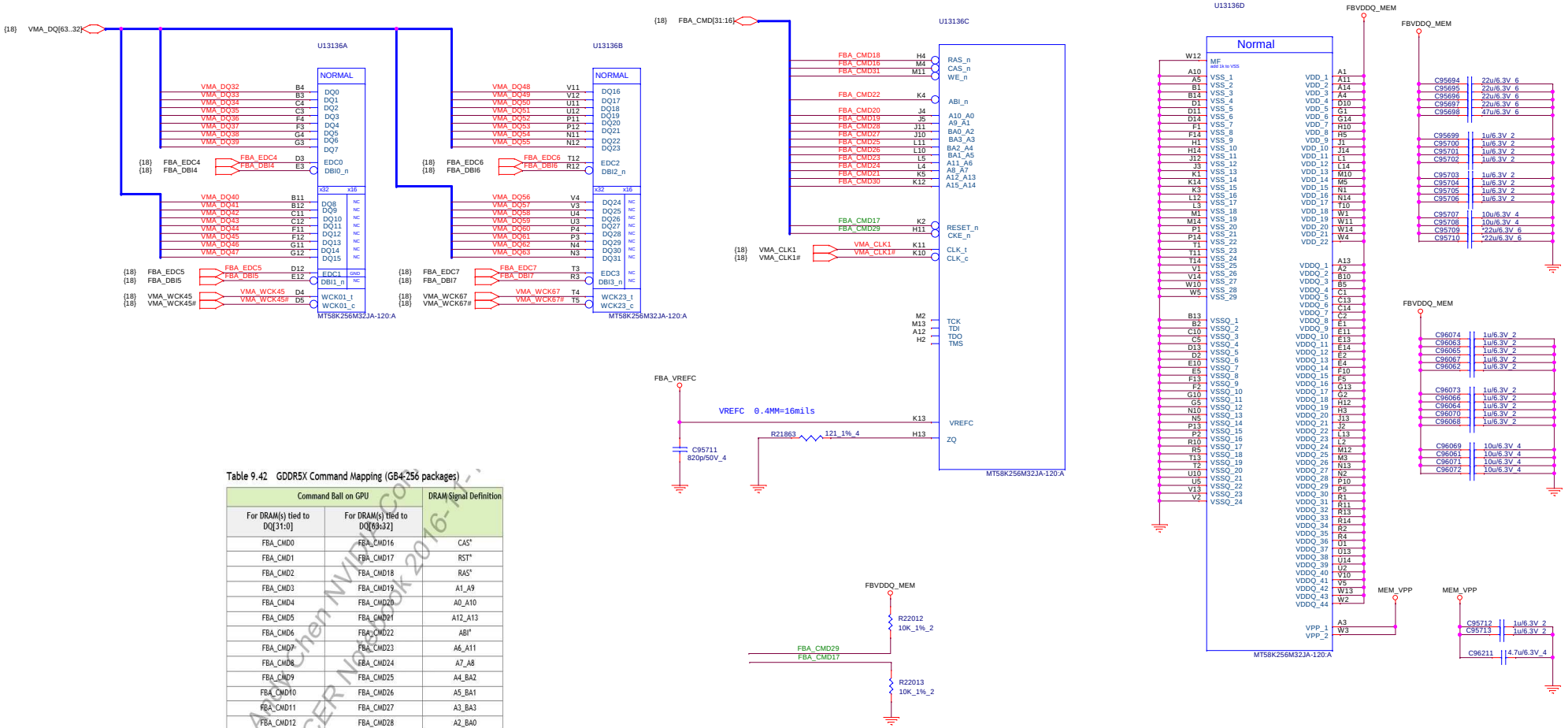


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX-1080-GDDR5X-FBA 32-63	1A

Date: Thursday, July 06, 2017 Sheet 28 of 72

CHANNEL B: GDDR5x (FBB 0-31)

MF=1 mirrored

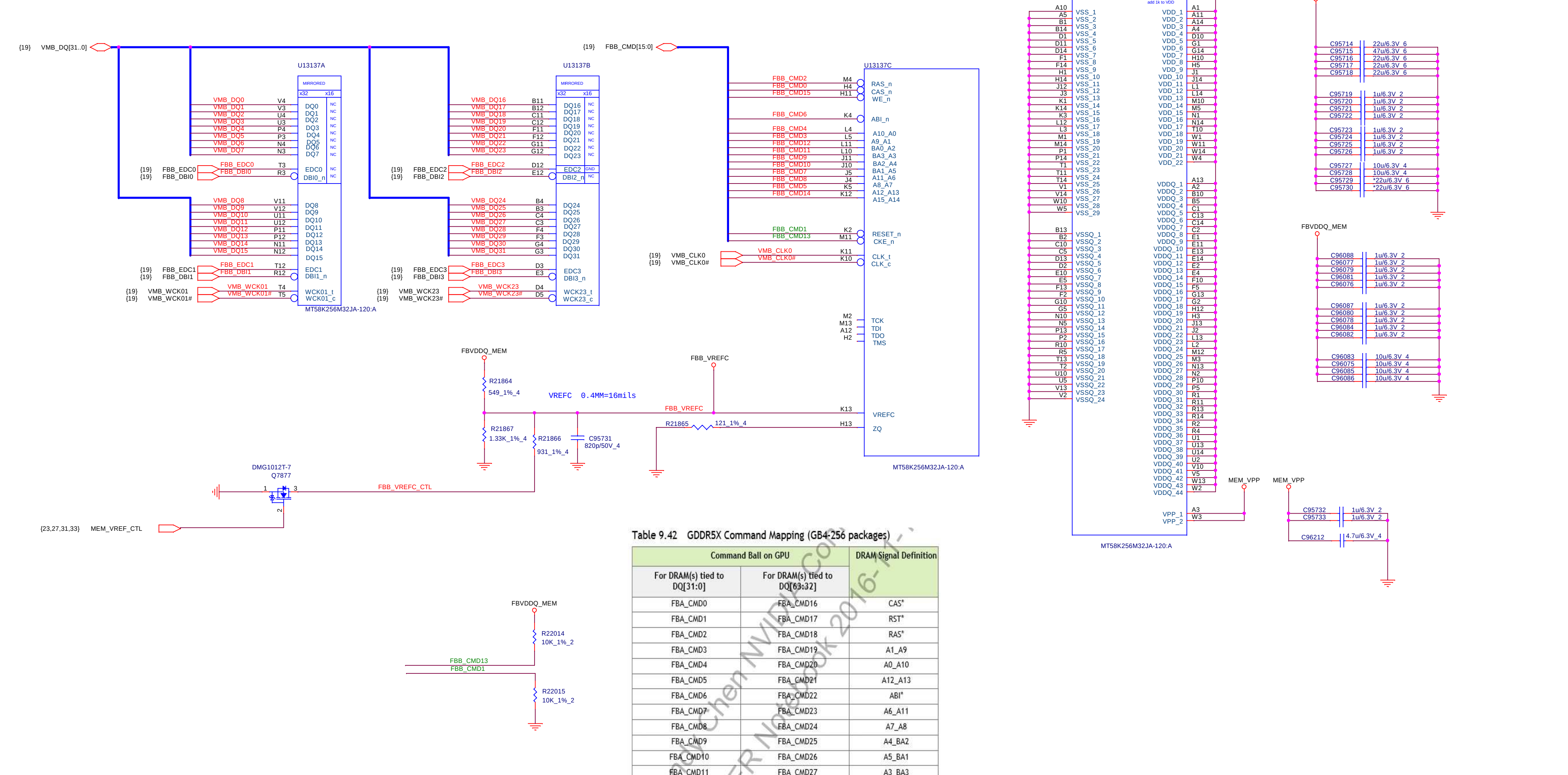


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

Quanta Computer Inc.

PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX-1080-GDDR5X-FBB 0-31	1A

CHANNEL B: GDDR5x (FBB 32-63)

MF=0 Normal

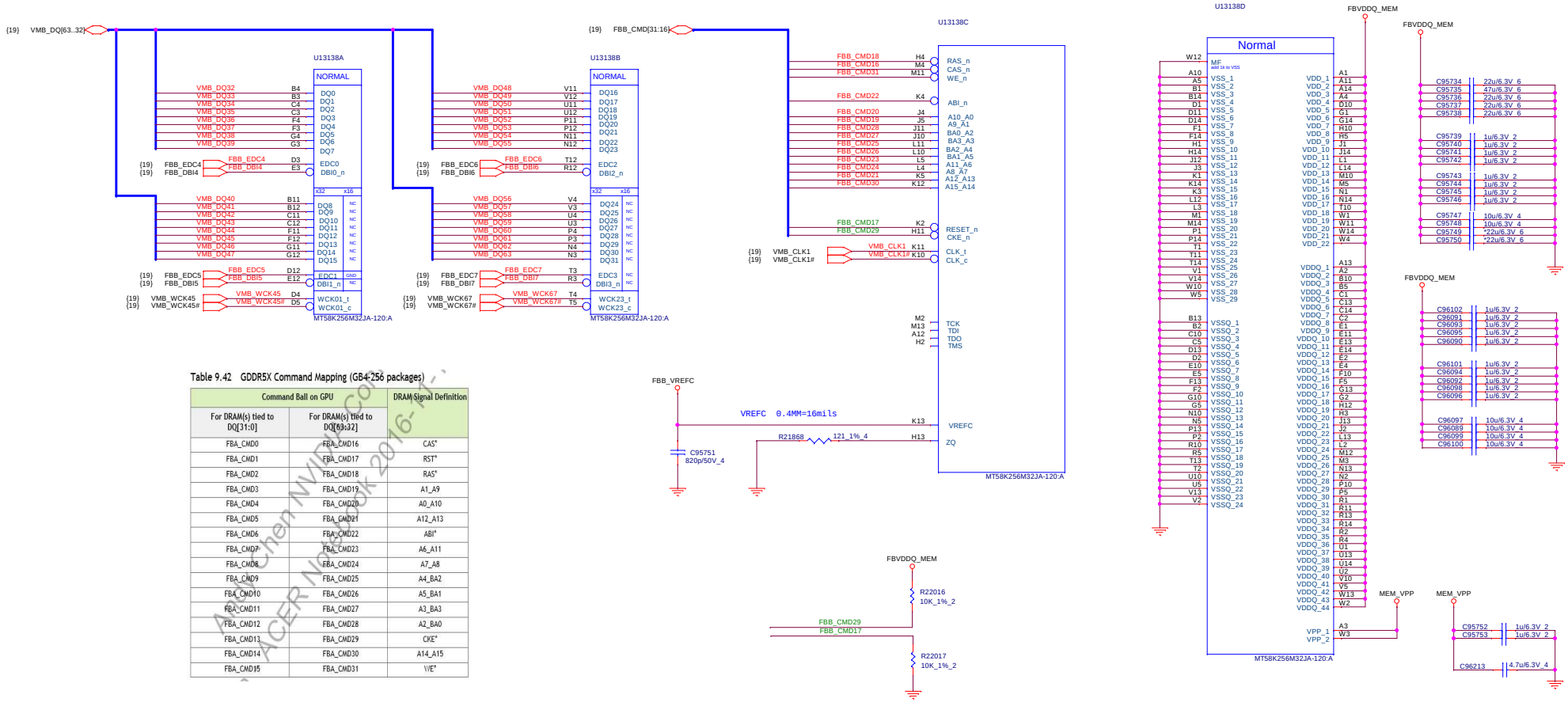


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX-1080-GDDR5X-FBB 32-63	1A

Date: Thursday, July 06, 2017 Sheet 30 of 72

CHANNEL C: GDDR5x (FBB 0-31)

MF=1 mirrored

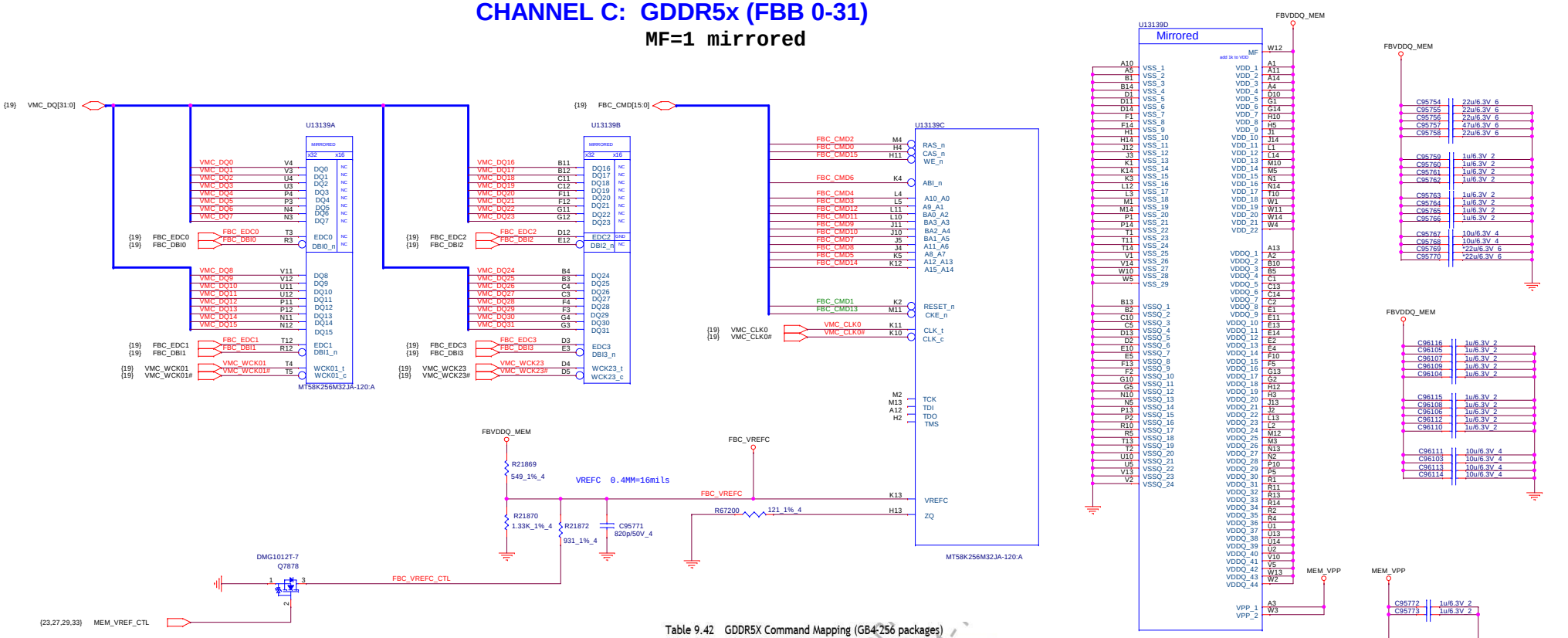


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

Quanta Computer Inc.	
PROJECT : ZGL	
Size	Document Number: N17E-GX-1080-GDDR5X-FBC 0-31 — Rev: 1A
Date: Thursday, July 06, 2017	Sheet 31 of 72

CHANNEL C: GDDR5x (FBC 32-63)

MF=0 Normal

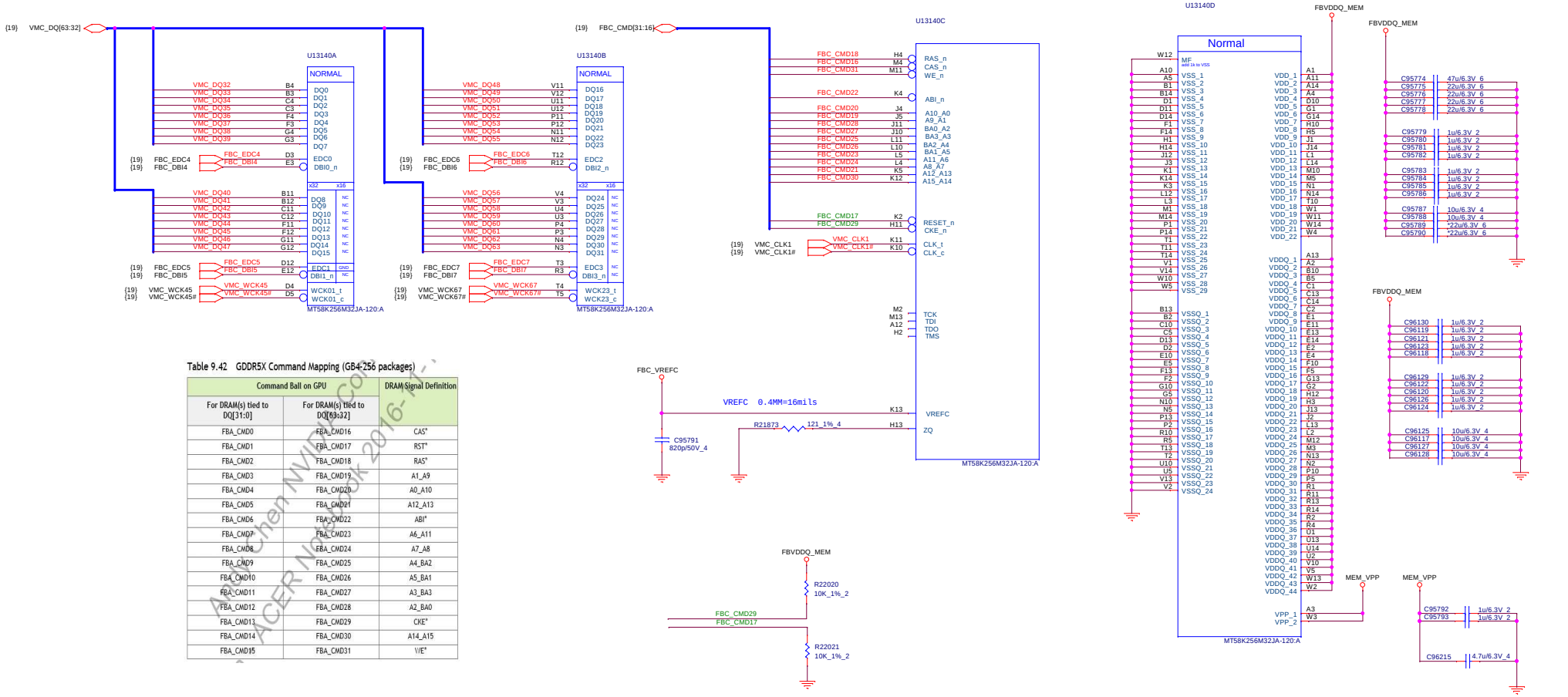


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number	Rev
	N17E-GX-1080-GDDR5X-FBC 32-63	1A
Date: Thursday, July 06, 2017	Sheet 32 of 72	

CHANNEL D: GDDR5x (FBD 0-31)

MF=1 mirrored

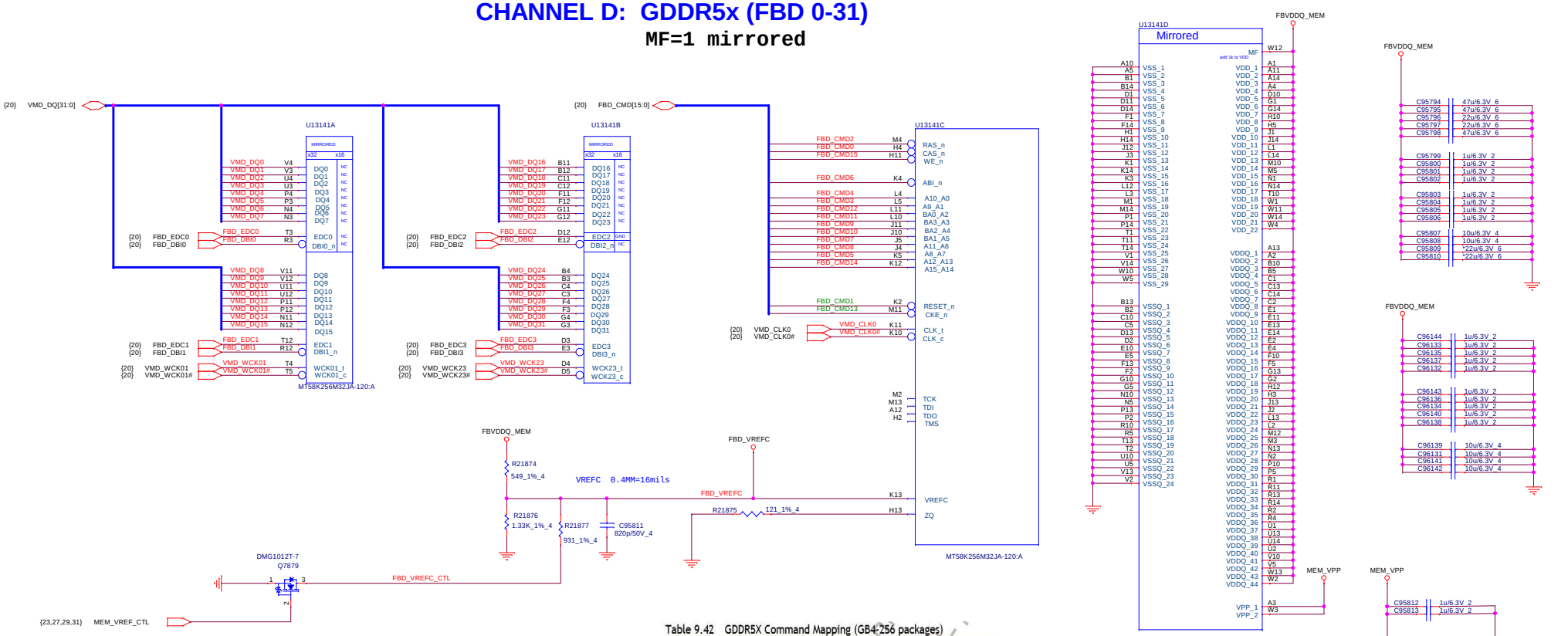


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

Quanta Computer Inc.	
PROJECT : ZGL	
Size	Document Number: N17E-GX-1080-GDDR5X-FBD 0-31 — Rev: 1A
Date: Thursday, July 06, 2017	Sheet 33 of 72

CHANNEL D: GDDR5x (FBD 32-63)

MF=0 Normal

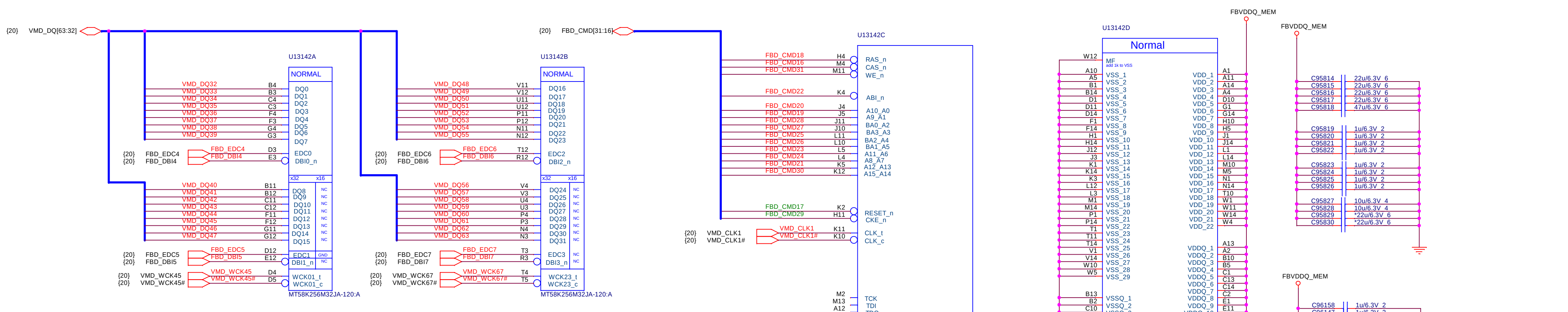
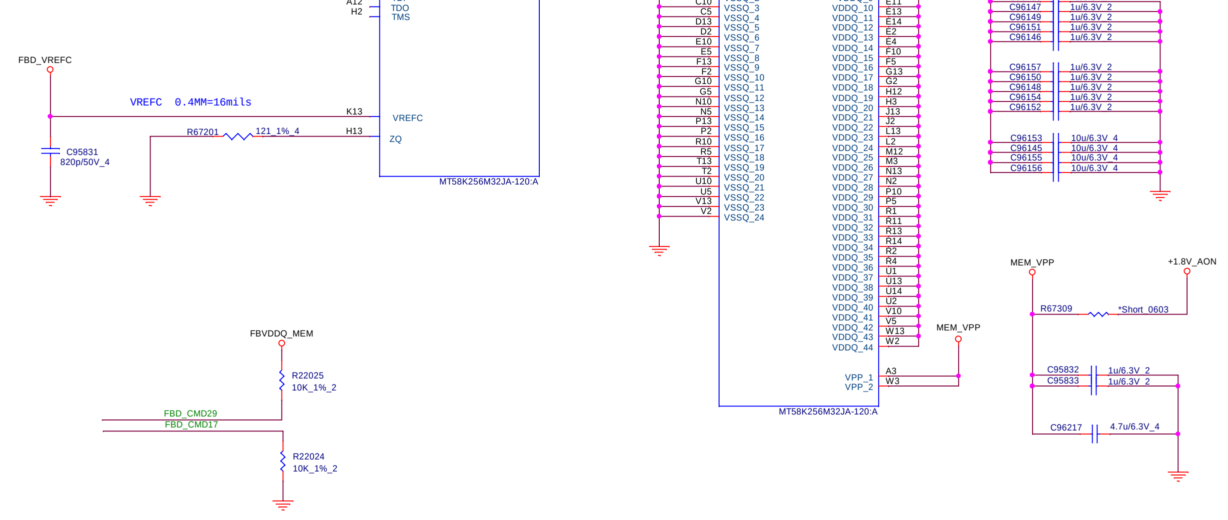


Table 9.42 GDDR5X Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	RST*
FBA_CMD2	FBA_CMD18	RAS*
FBA_CMD3	FBA_CMD19	A1_A9
FBA_CMD4	FBA_CMD20	A0_A10
FBA_CMD5	FBA_CMD21	A12_A13
FBA_CMD6	FBA_CMD22	ABI*
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	A7_A8
FBA_CMD9	FBA_CMD25	A4_BA2
FBA_CMD10	FBA_CMD26	A5_BA1
FBA_CMD11	FBA_CMD27	A3_BA3
FBA_CMD12	FBA_CMD28	A2_BA0
FBA_CMD13	FBA_CMD29	CKE*
FBA_CMD14	FBA_CMD30	A14_A15
FBA_CMD15	FBA_CMD31	WE*

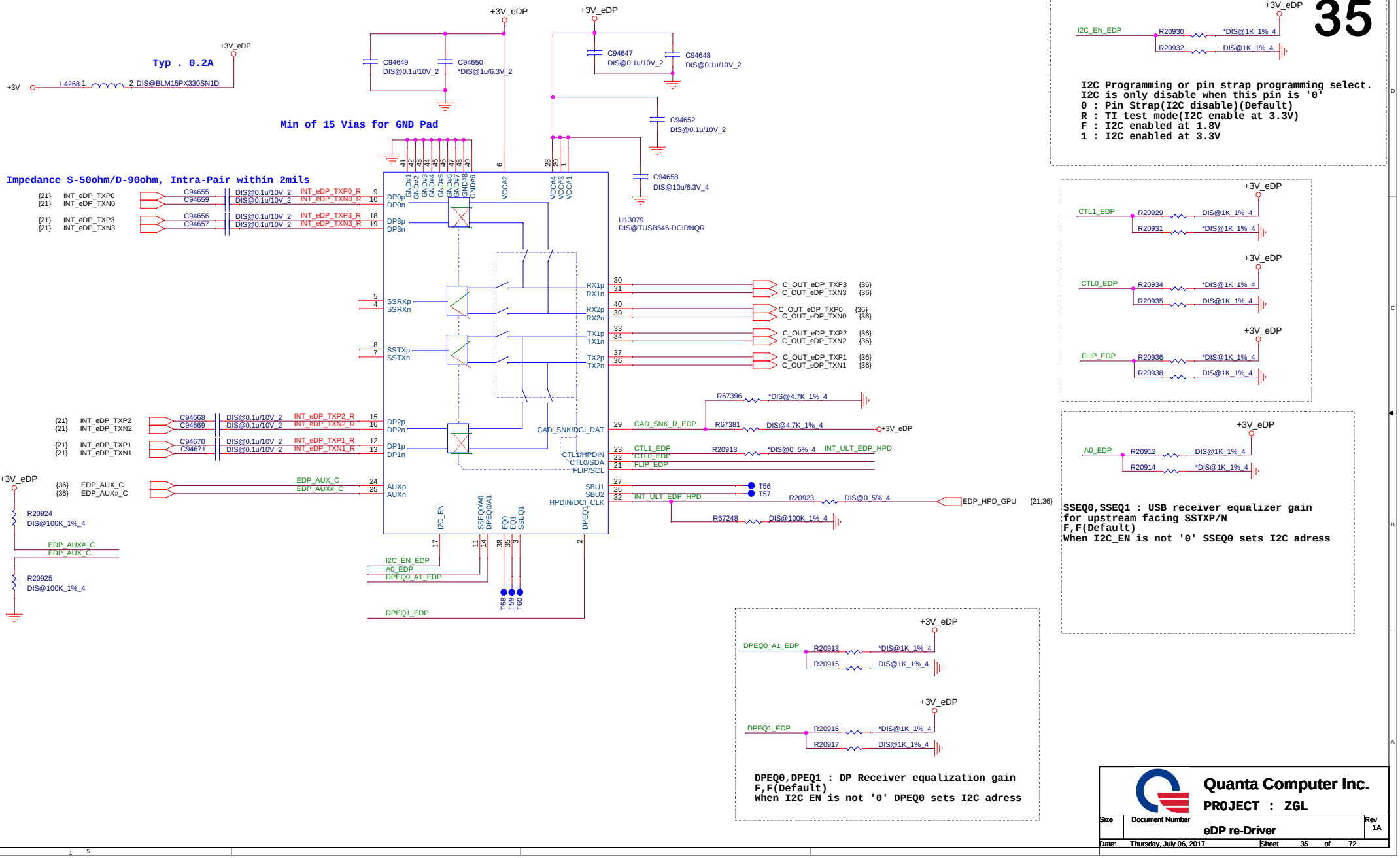


Quanta Computer Inc.

PROJECT : ZGL

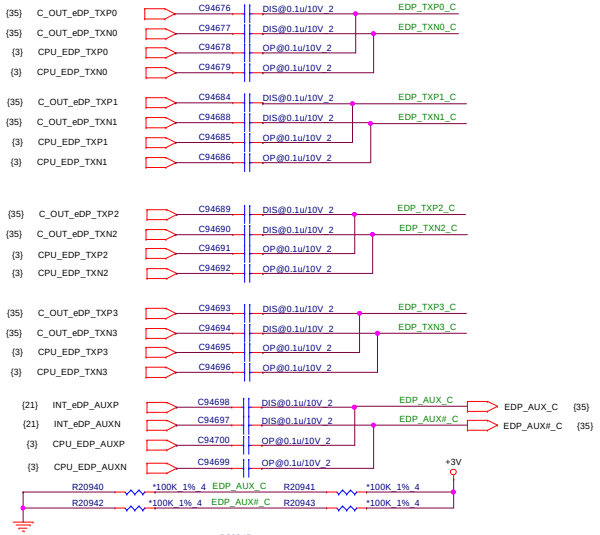
Size	Document Number	Rev
	N17E-GX-1080-GDDR5X-FBD 32-63	1A

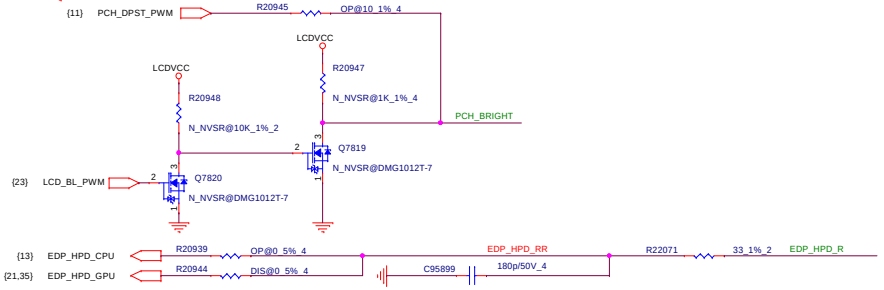
Date: Thursday, July 06, 2017 Sheet 34 of 72



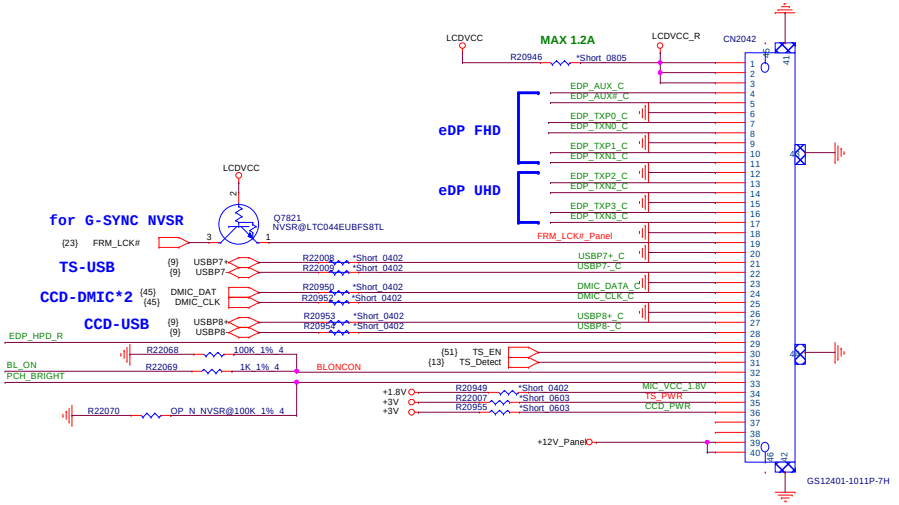
Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number	Rev
	eDP re-Driver	1A
Date: Thursday, July 06, 2017	Sheet 35 of 72	

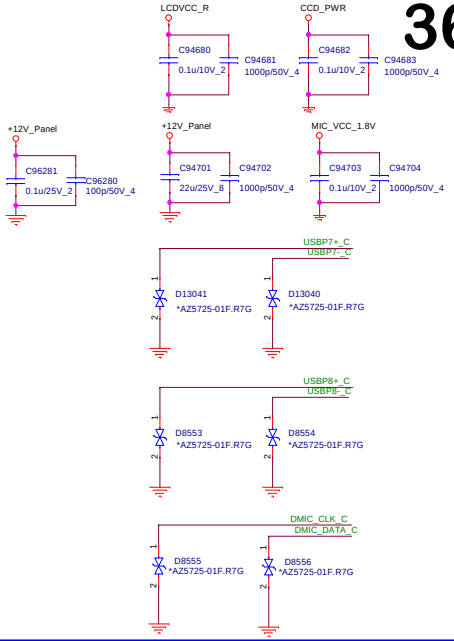
EDP Optimus/Discrete



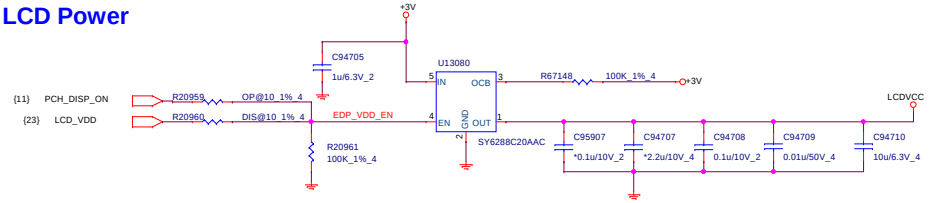


LCD CONNECTOR

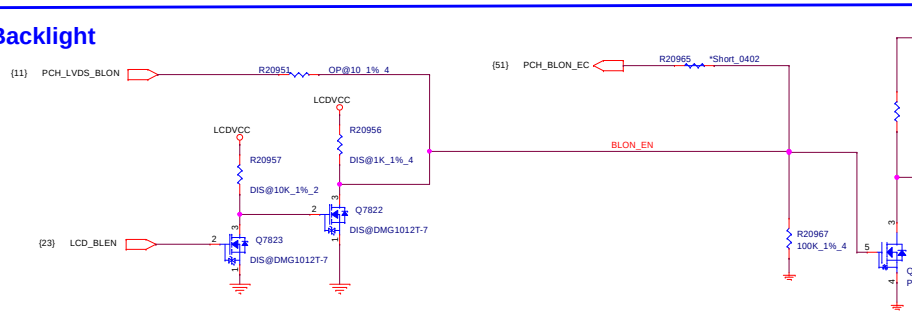


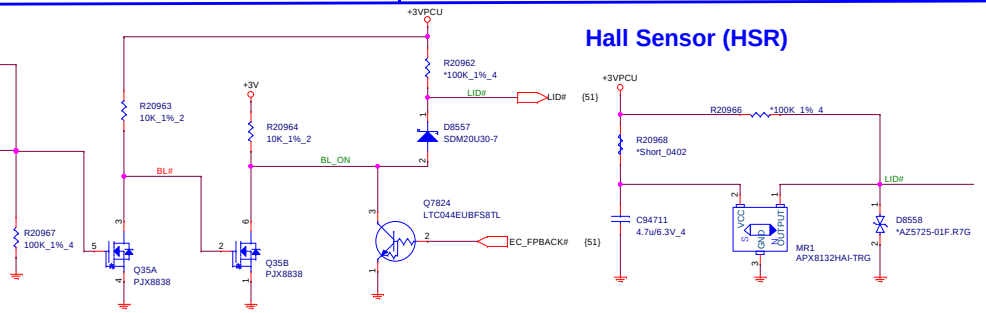


LCD Power



Backlight



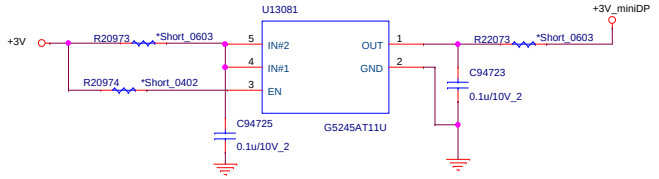


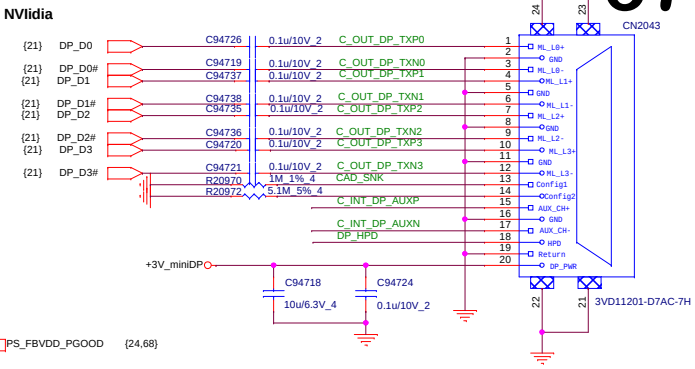
Hall Sensor (HSR)

Quanta Computer Inc.
PROJECT : ZGL

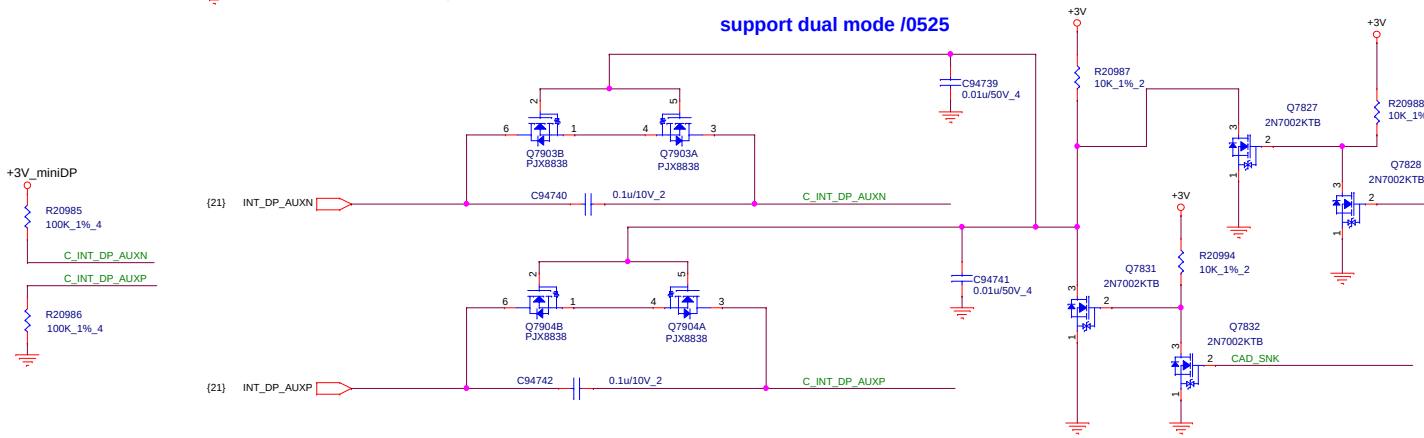
Size	Document Number	Rev
	eDP Panel/CCD/Hall Sensor	1A

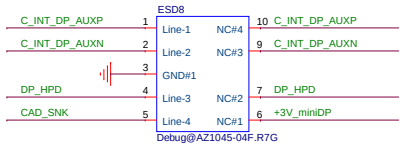
Date: Tuesday, July 11, 2017 Sheet 36 of 72

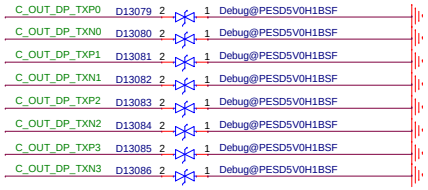




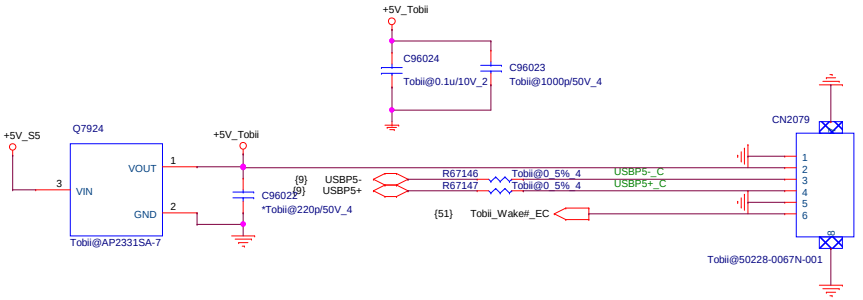
support dual mode /0525

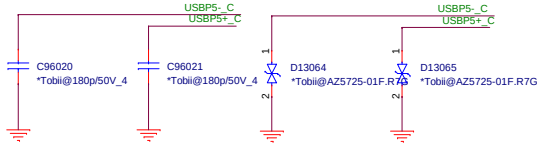






Tobii





Quanta Computer Inc.

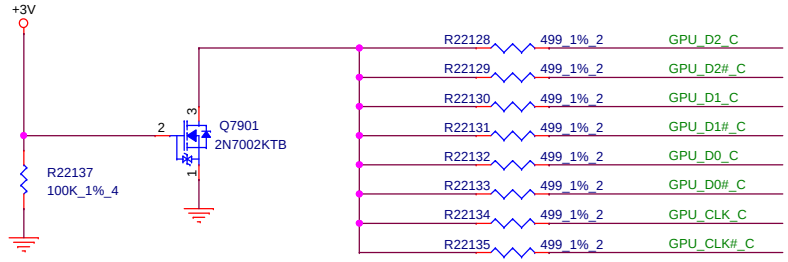
PROJECT : ZGL

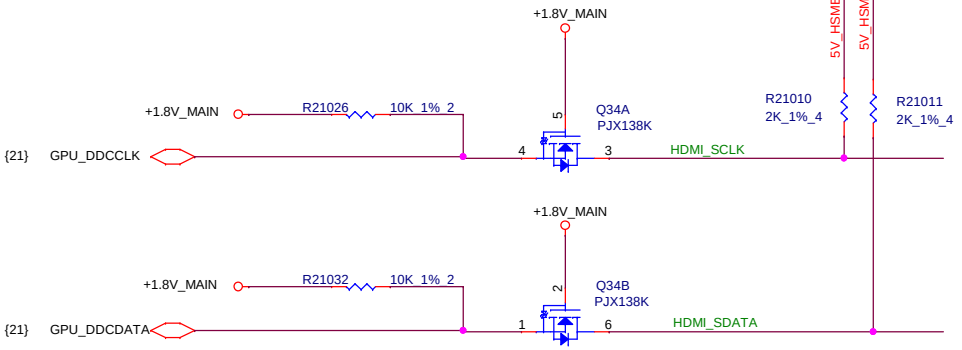
Size	Document Number	Rev
	Display Port/Tobii	1A

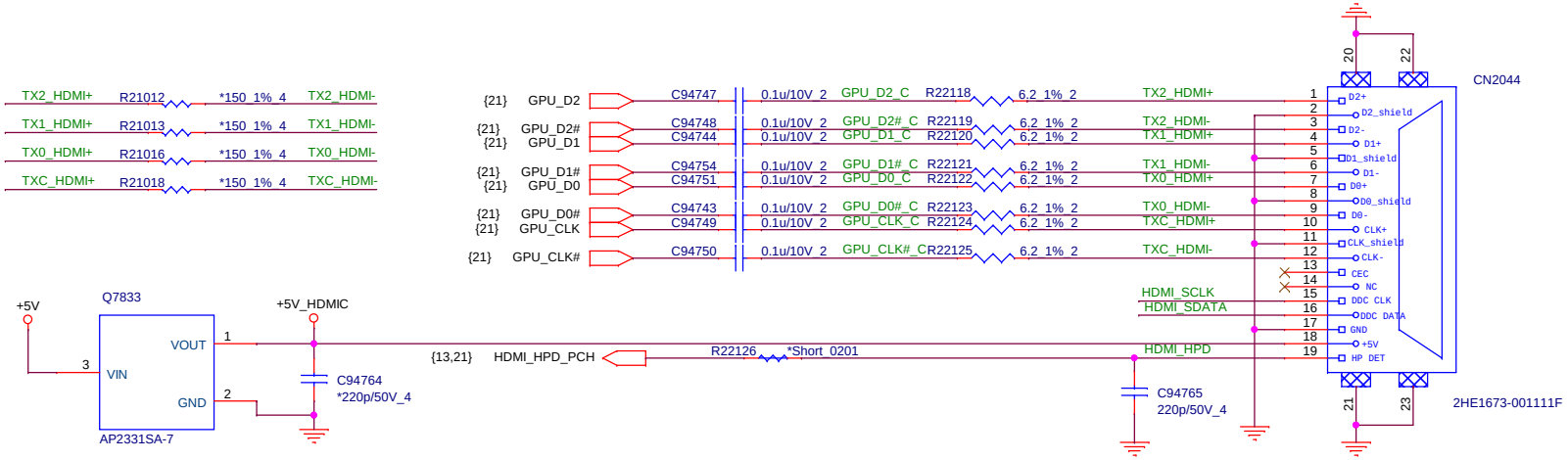
Date: Thursday, July 06, 2017 Sheet 37 of 72

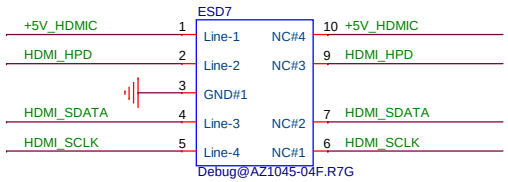
HDMI

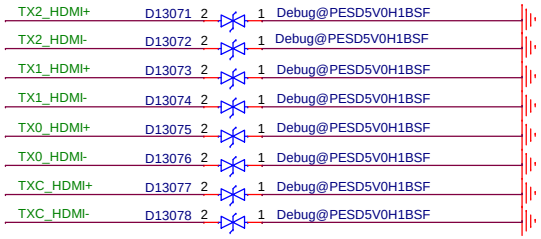
HDMI LEVEL SHIFT







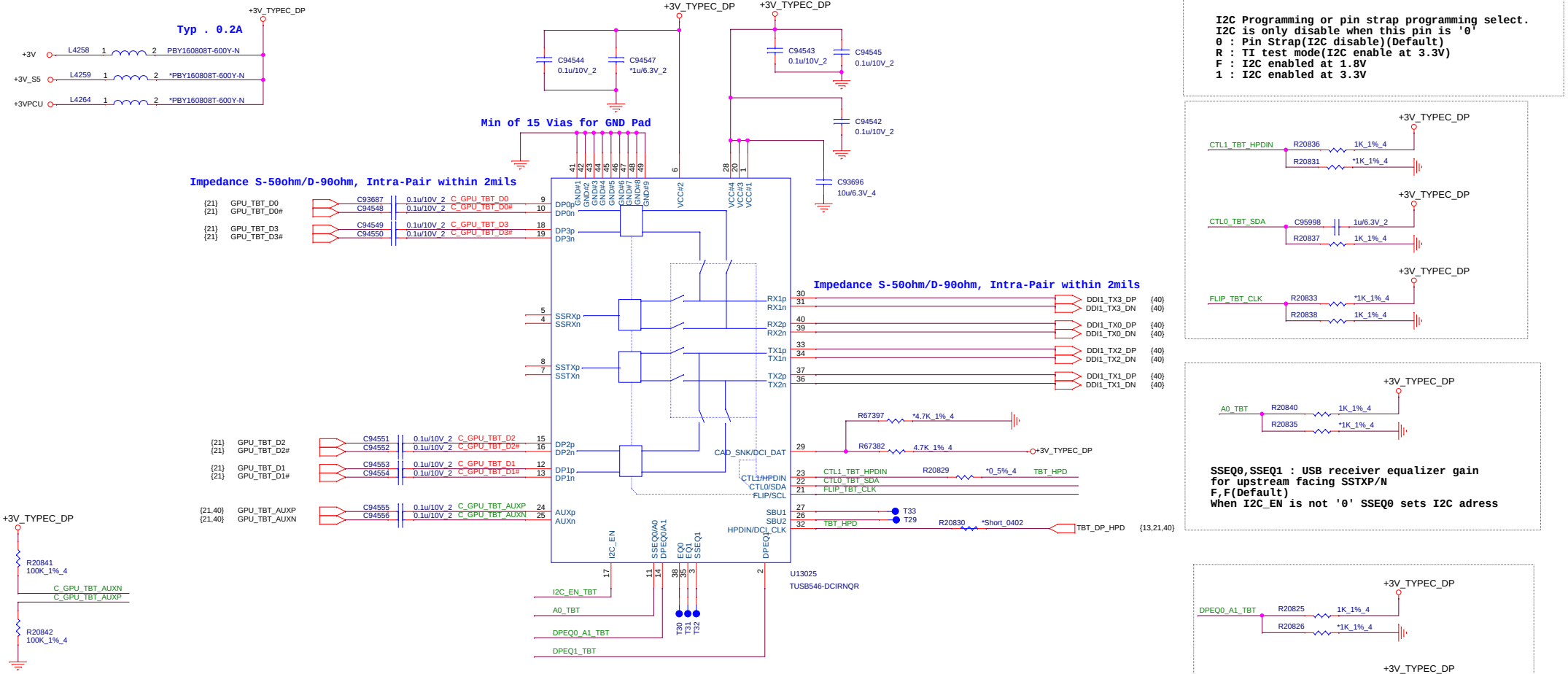


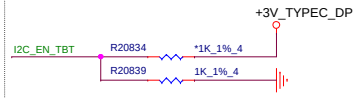


Quanta Computer Inc.

PROJECT : ZGL

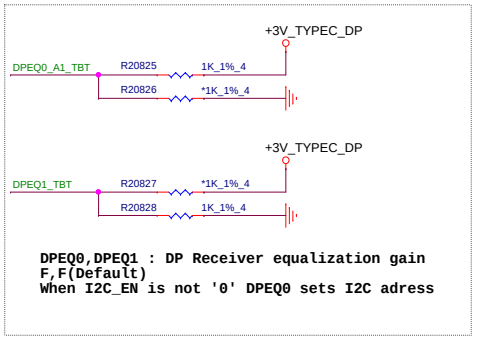
Size	Document Number	Rev
	HDMI	1A
Date: Thursday, July 06, 2017	Sheet 38 of 72	





I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

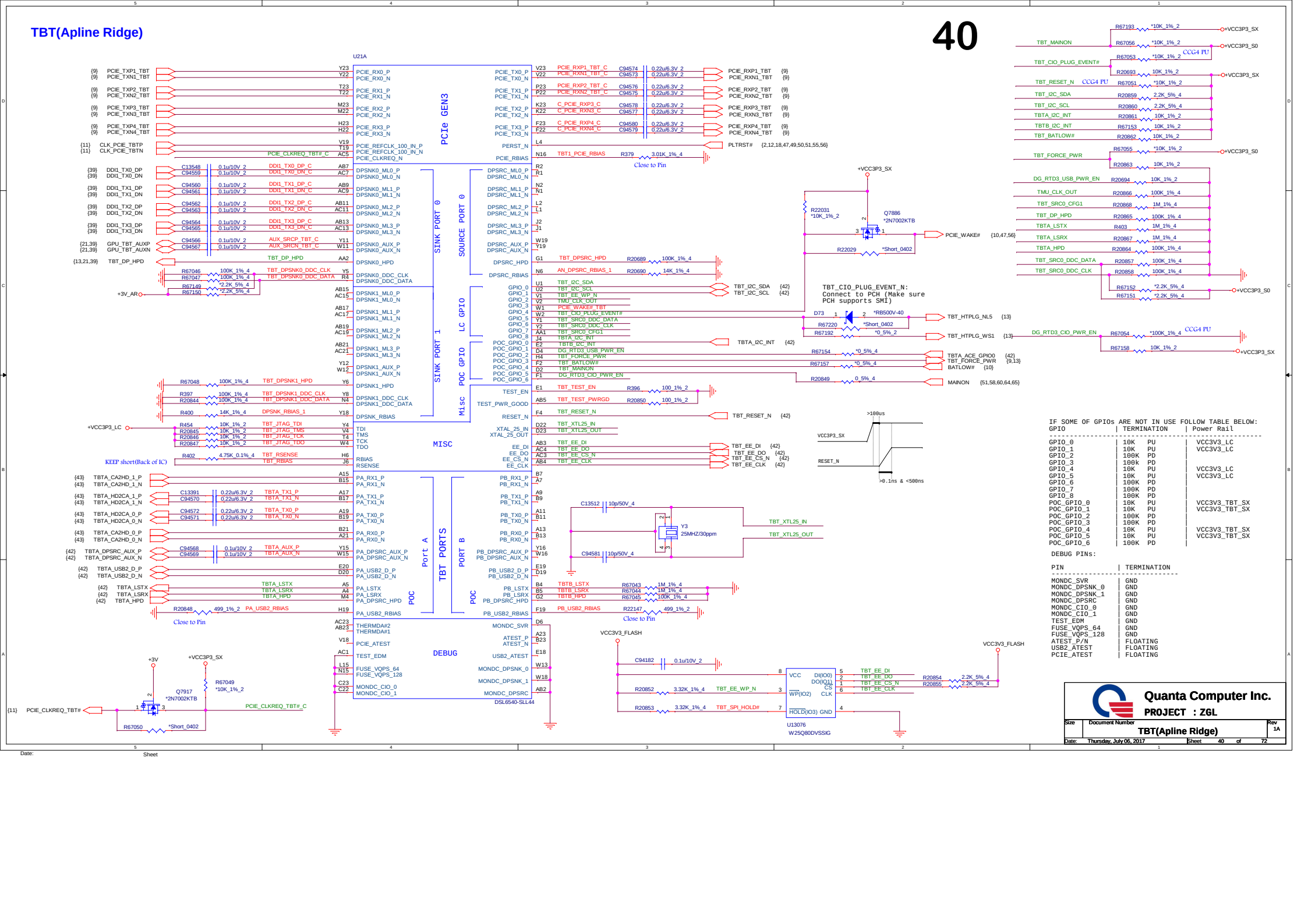
SSEQ0,SSEQ1 : USB receiver equalizer gain
for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress



DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Type C DP re-Driver	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 39 of 72	

TBT(Apline Ridge)



IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100k PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

DEBUG PINs:

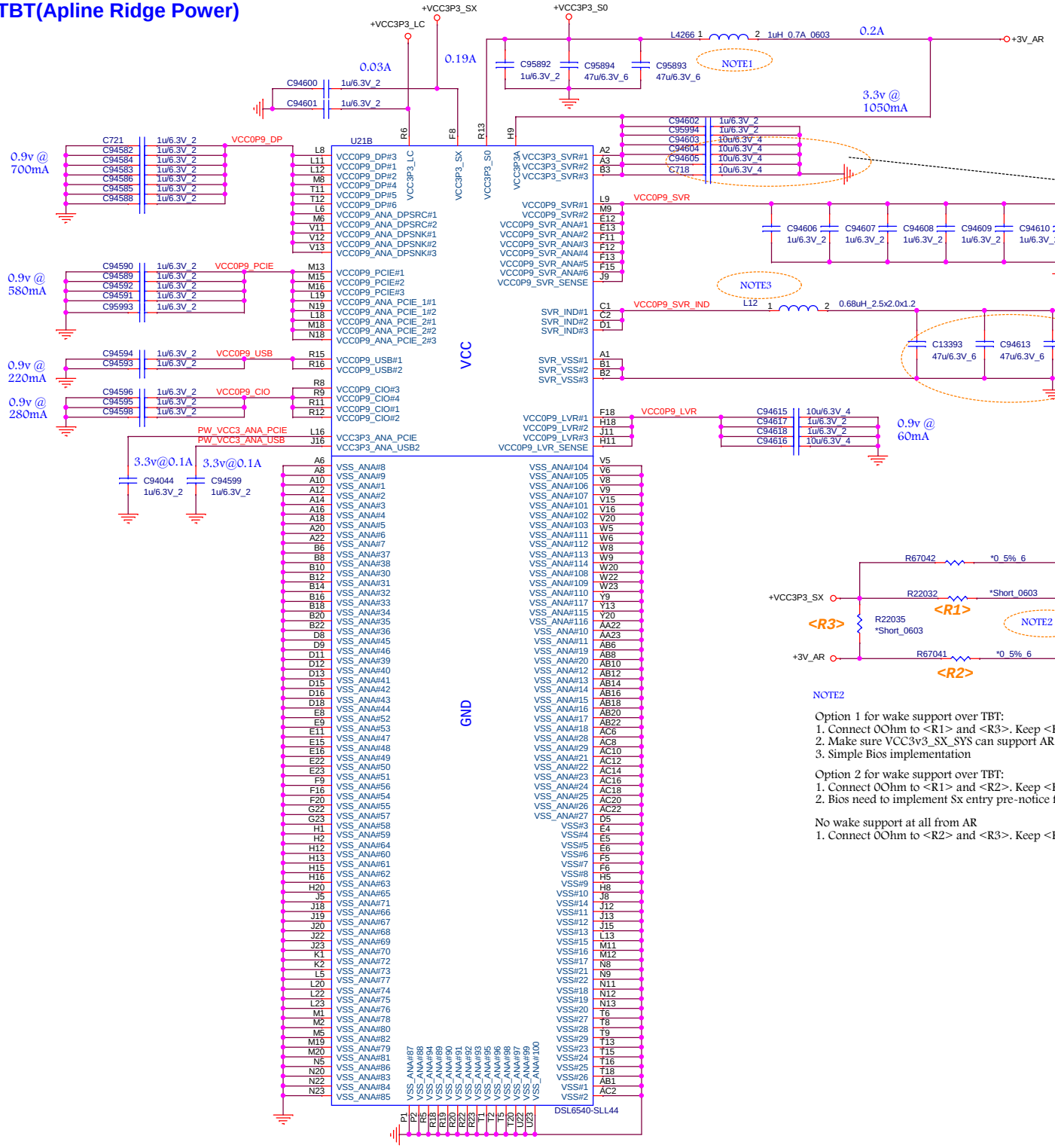
PIN	TERMINATION
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
USB2_ATEST	FLOATING
PCIE_ATEST	FLOATING

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	TBT(Apline Ridge)	1A
Date: Thursday, July 06, 2017	Sheet 40 of 72	

Date:
Sheet

TBT(Apline Ridge Power)



NOTE1

40KHz LC Filter to reduce VCC3v3_S0_TBT ripple

L (LQM18PN1R0MFHD):
RDC < 0.2Ohm
IDC > 0.2A

C (GRM188R60J476ME15):
Need to notice the capacitance at 3.3 Vdc

NOTE3

Share Same GND plane with SVR_VSS of AR

NOTE3

Inductor value should be 0.6uH or 0.68uH
DCR should be as low as possible; 20mΩ – 25mΩ or lower
Saturation current should be above 5A

NOTE2

Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
2. Make sure VCC3v3_SX_SYS can support AR maximum power consumption.
3. Simple Bios implementation

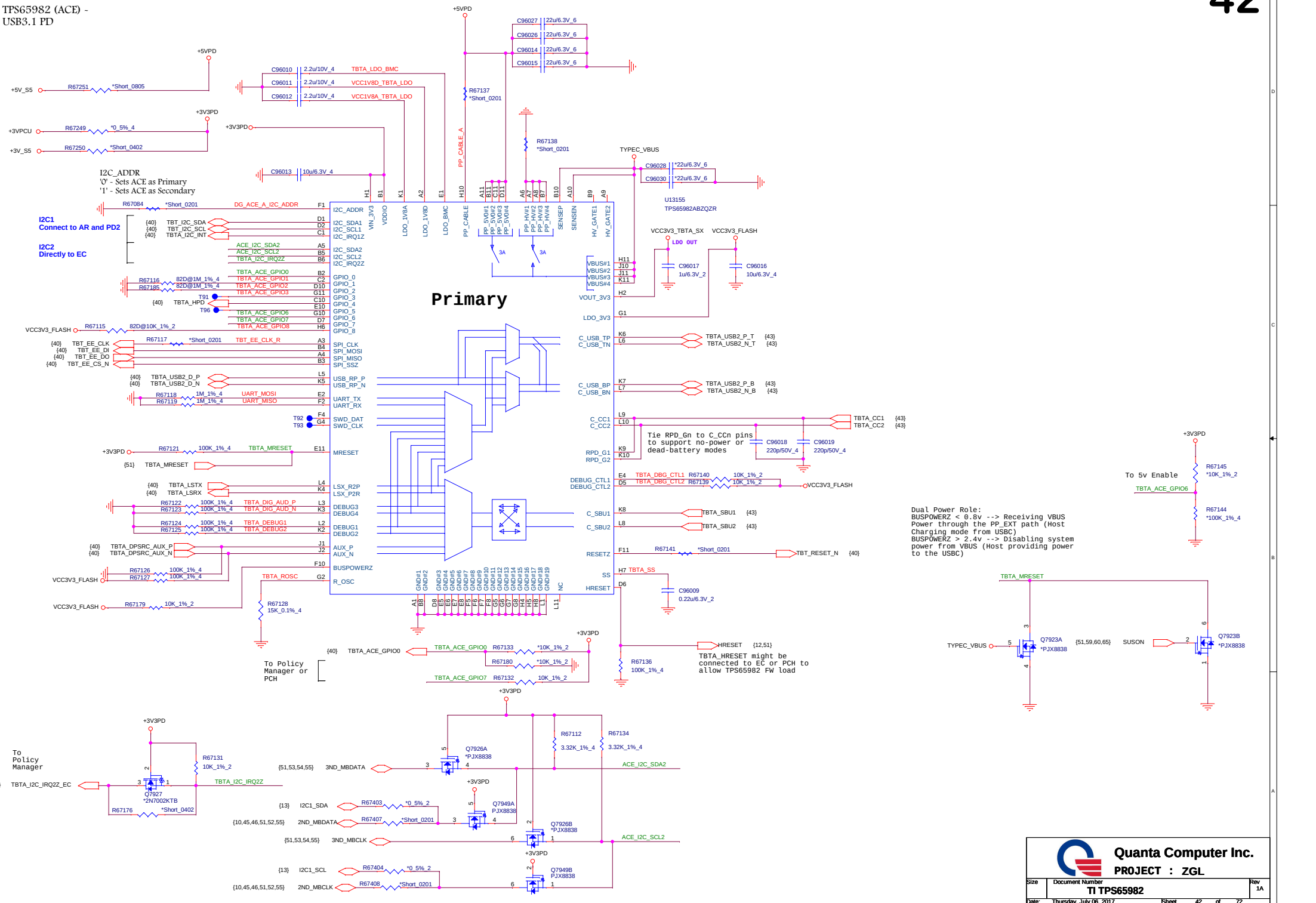
Option 2 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R2>. Keep <R3> empty.
2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from AR
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

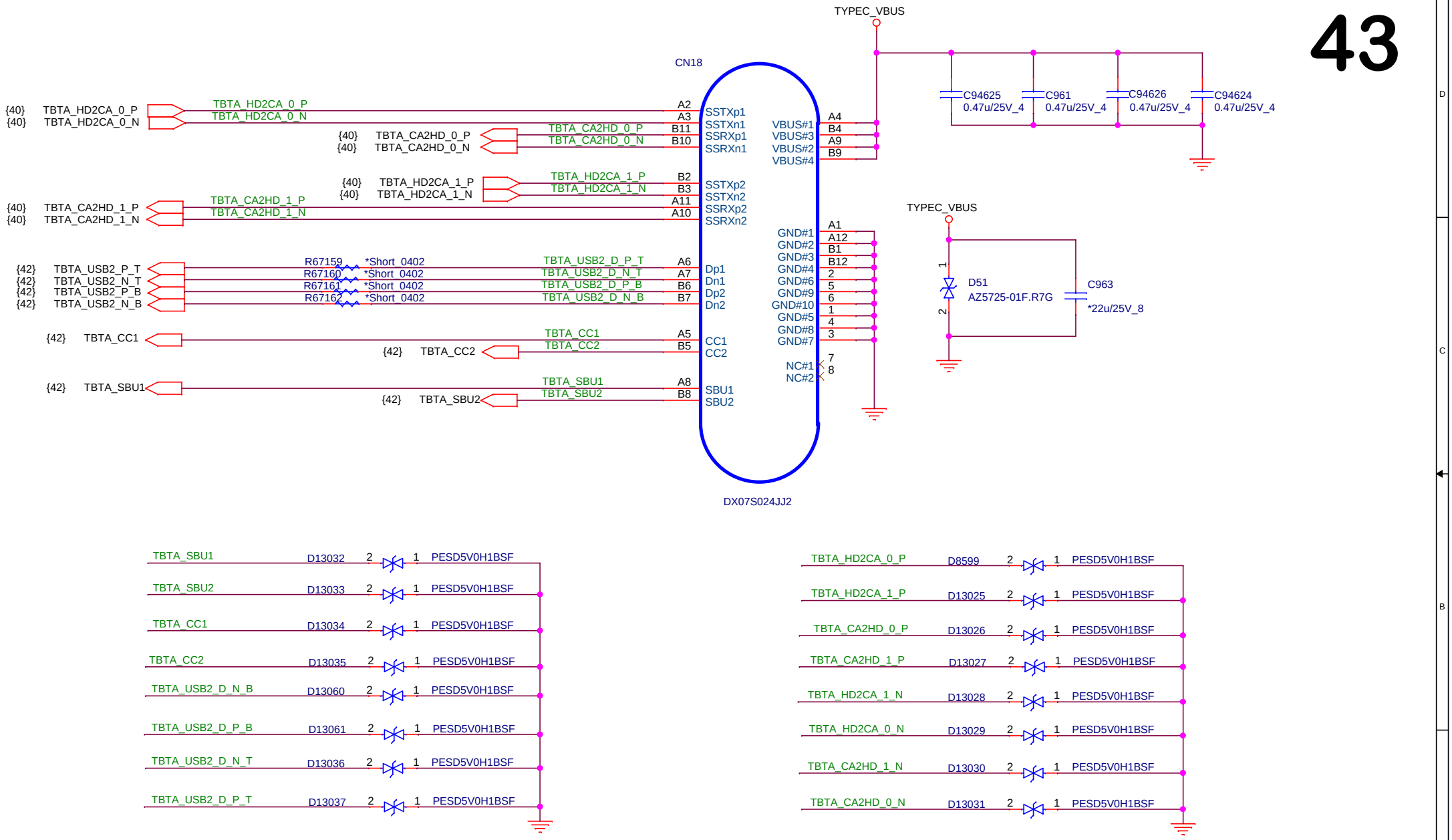
Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: TBT(Apline Ridge Power)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 41 of 72	

Port A Controller - ACE

TPS65982 (ACE) -
USB3.1 PD



Quanta Computer Inc.			
PROJECT : ZGL			
Size	Document Number		Rev
	TI TPS65982		1A
Date: Thursday, July 06, 2017		Sheet 42 of 72	



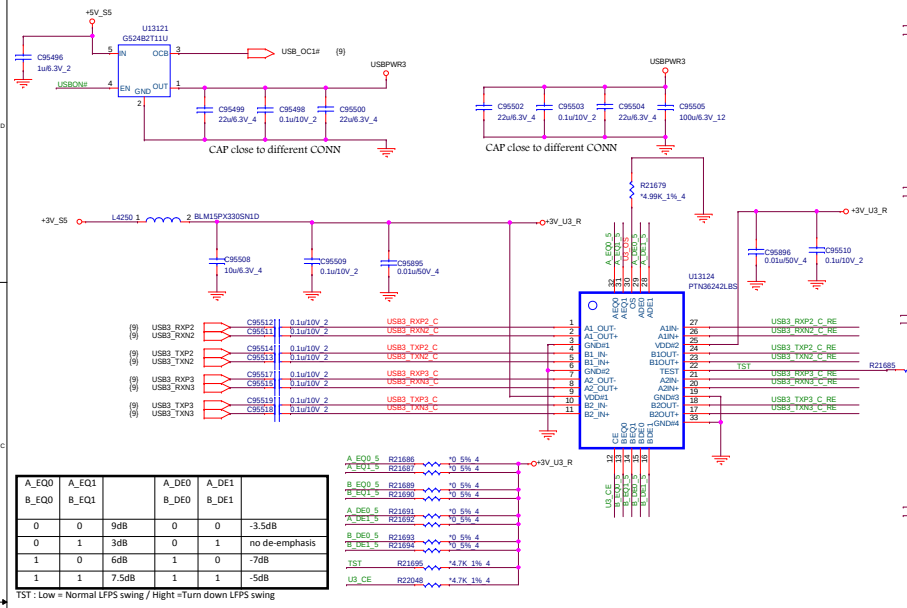
Quanta Computer Inc.

PROJECT : ZGL

Size	Document Number	Rev
	Type C(USB3.1/DP) *1	1A

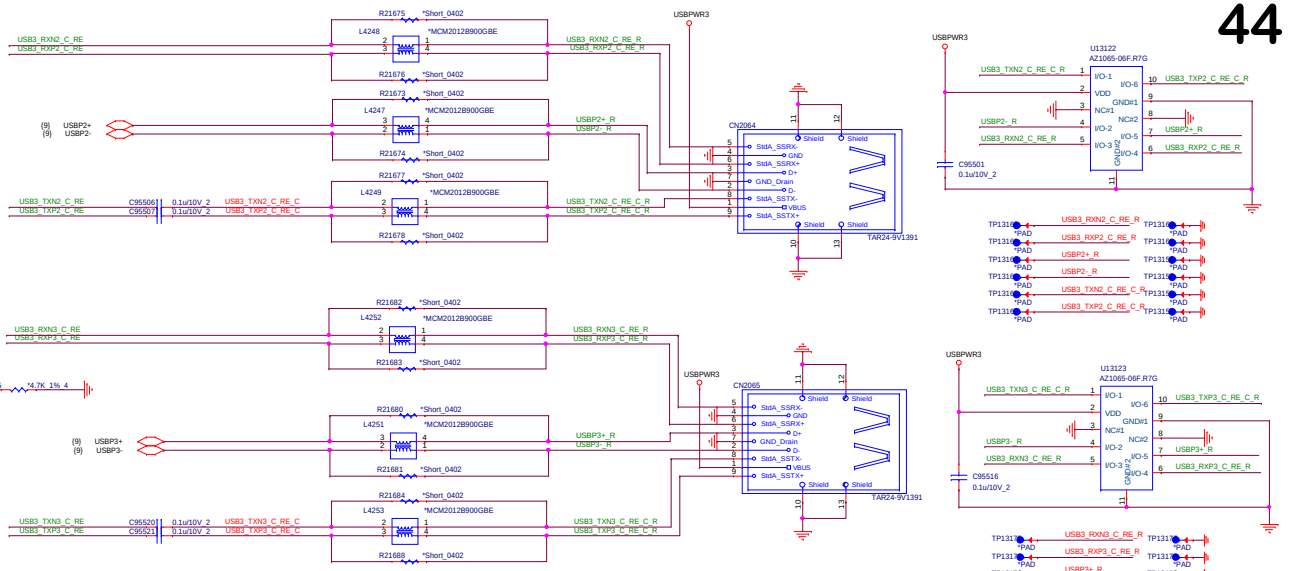
Date: Thursday, July 06, 2017 Sheet 43 of 72

USB 3.0(UB3) -Left

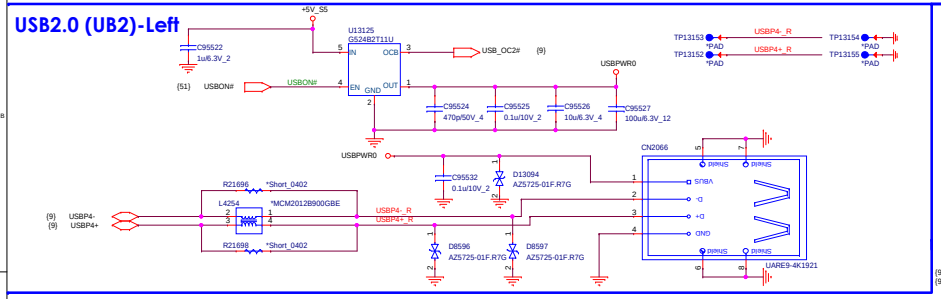


A_EQ0 / B_EQ0	A_EQ1 / B_EQ1		A_DE0 / B_DE0	A_DE1 / B_DE1	
0	0	9dB	0	0	-3.5dB
0	1	3dB	0	1	no de-emphasis
1	0	6dB	1	0	-7dB
1	1	7.5dB	1	1	-5dB

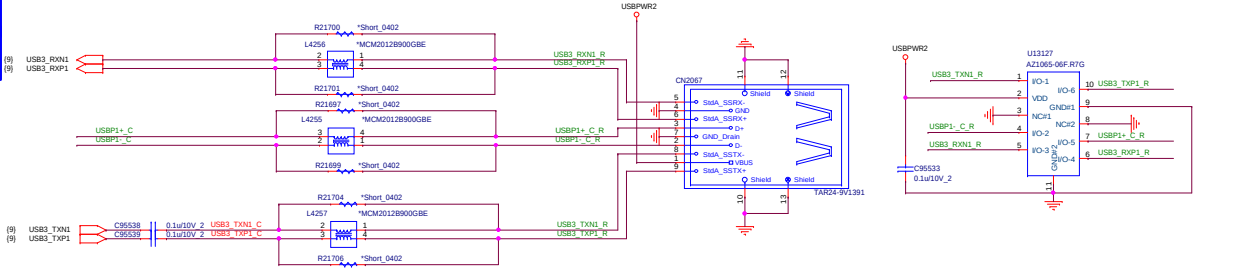
TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing



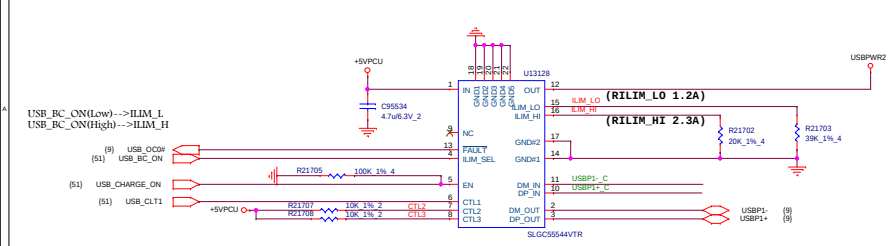
USB2.0 (UB2)-Left



USB 3.0(UB3) -Right



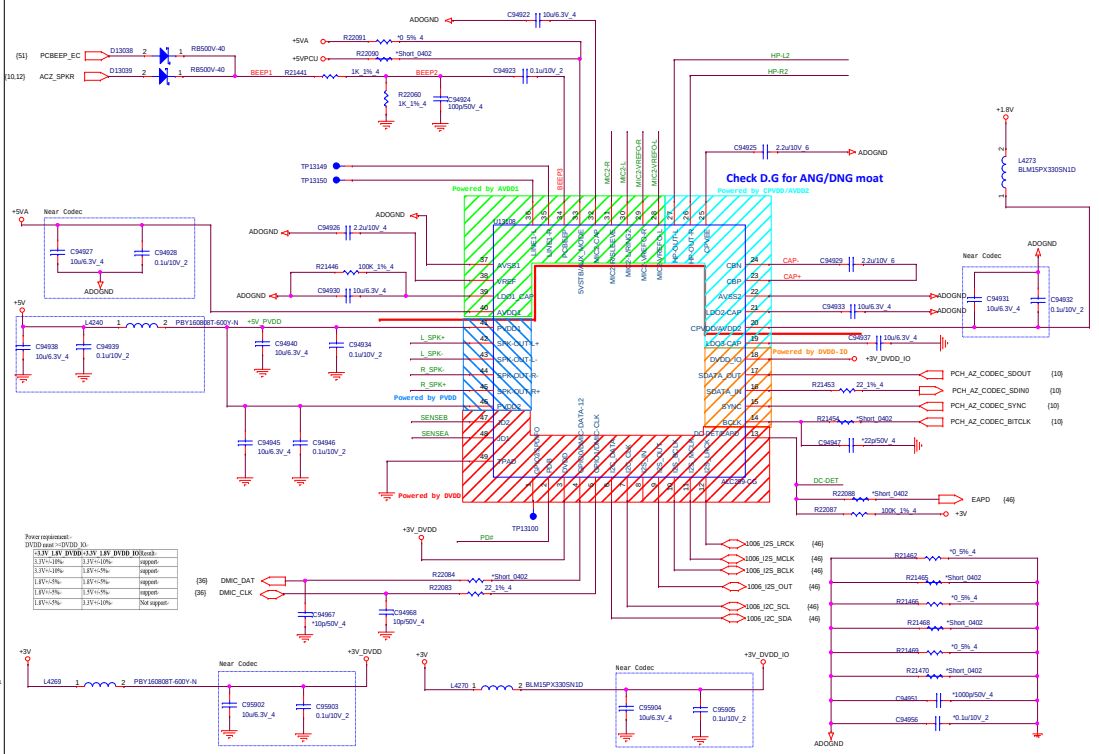
BC1.2 -U3 OF Right side



Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	USB2.0*1/USB3.0*3/BC1.2	1A
Date: Thursday, July 06, 2017	Sheet 44 of 72	

Codec

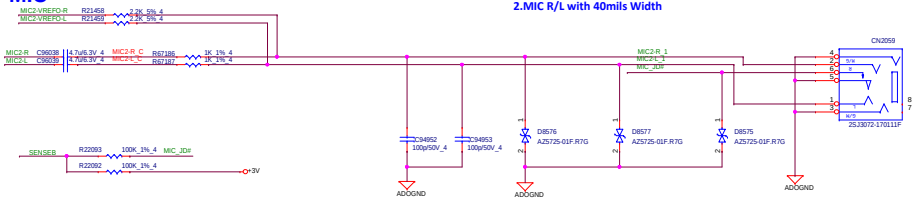


Power requirement :
DVDD must >=DVDD_IO.

+3.3V_LAV_DVDD	+1.8V_LAV_DVDD_IO	Result
3.3V+/-10%	1.8V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	1.3V+/-10%	Not support

MIC

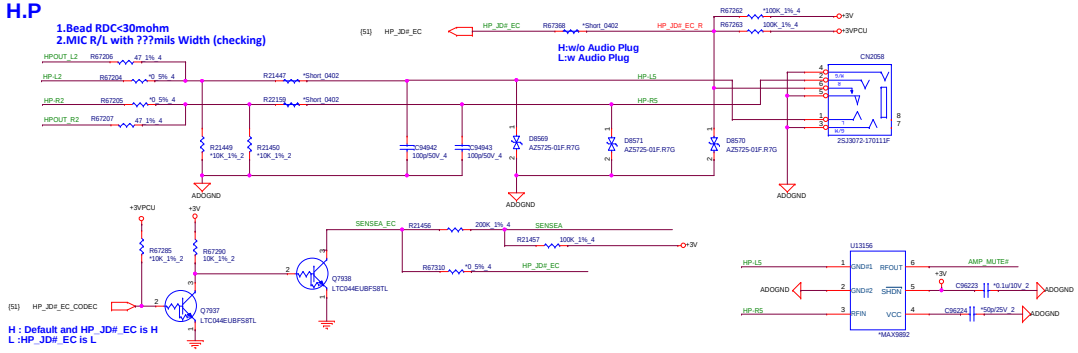
1.Bead RDC<30mohm
2.MIC R/L with 40mils Width



H.P

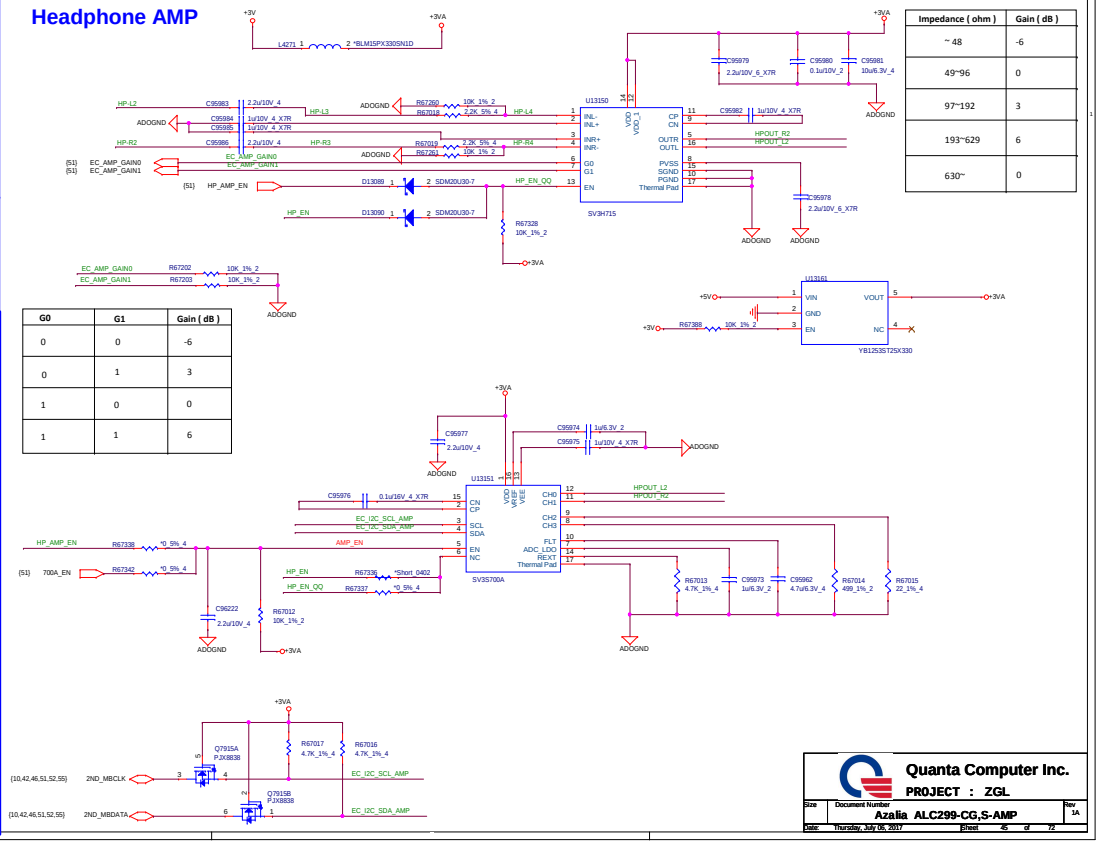
1.Bead RDC<30mohm
2.MIC R/L with ???mils Width (checking)

H:w/o Audio Plug
L:w Audio Plug



H : Default and HP_JD#_EC is H
L :HP_JD#_EC is L

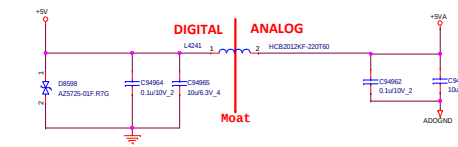
Headphone AMP



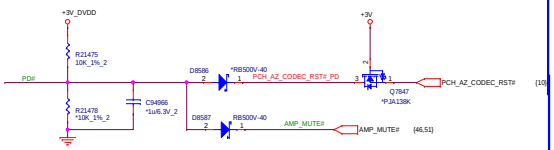
Impedance (ohm)	Gain (dB)
~ 48	-6
49~96	0
97~192	3
193~629	6
630~	0

G0	G1	Gain (dB)
0	0	-6
0	1	3
1	0	0
1	1	6

Codec PWR 5V(ADO)

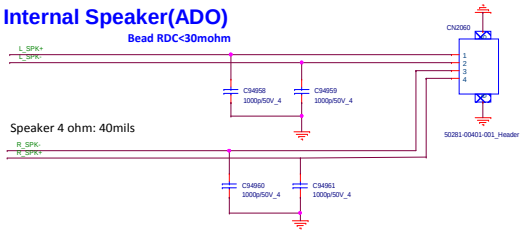


Mute(ADO)



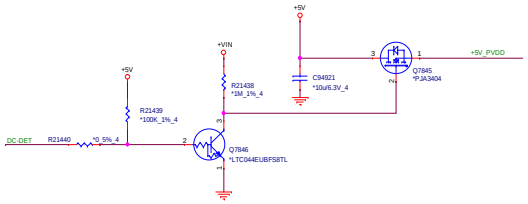
Internal Speaker(ADO)

Bead RDC<30mohm



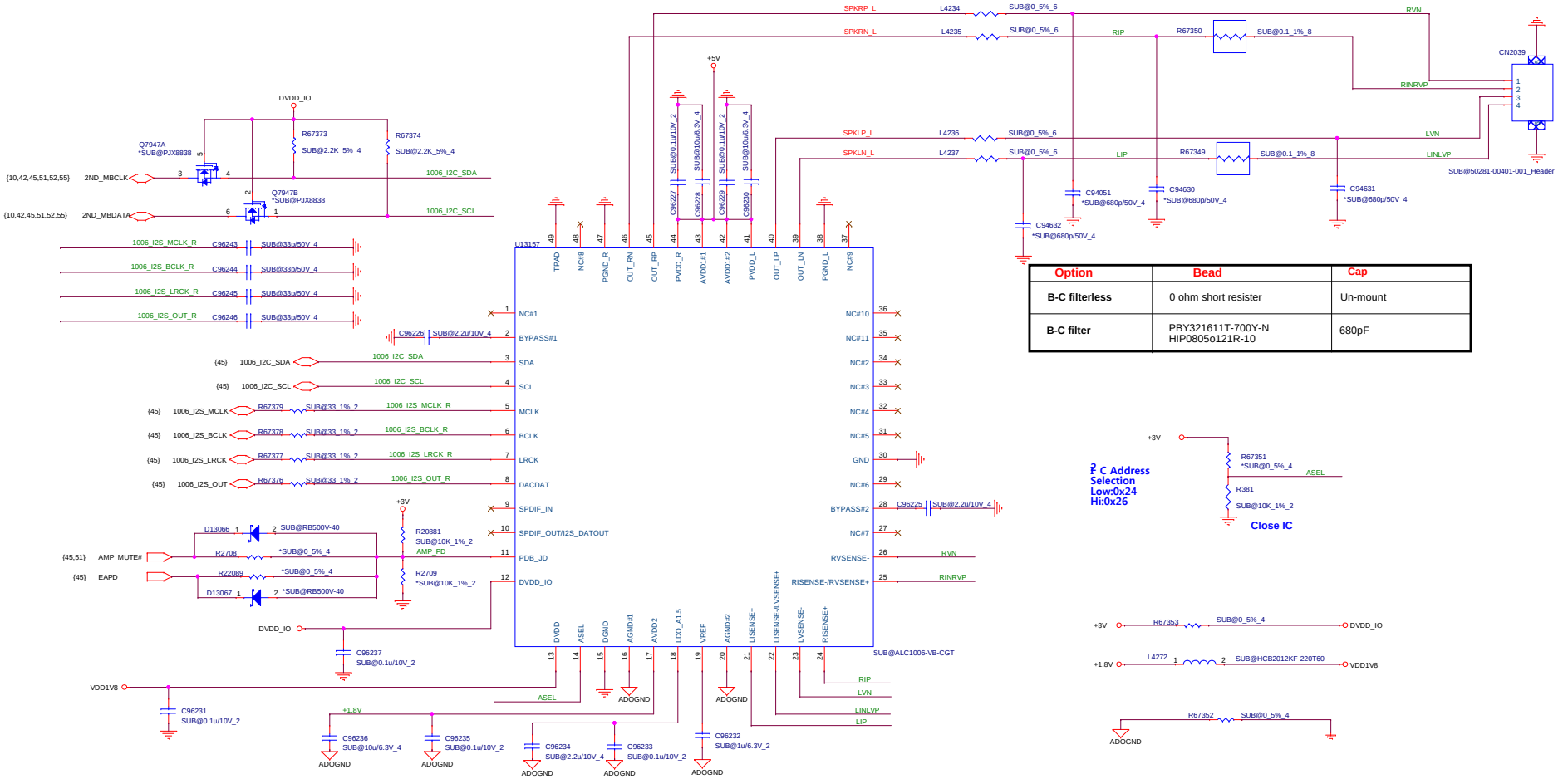
Speaker 4 ohm: 40mils

DC-DET circuit(ADO)



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Azalia ALC299-CG,S-AMP	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 45 of 72	

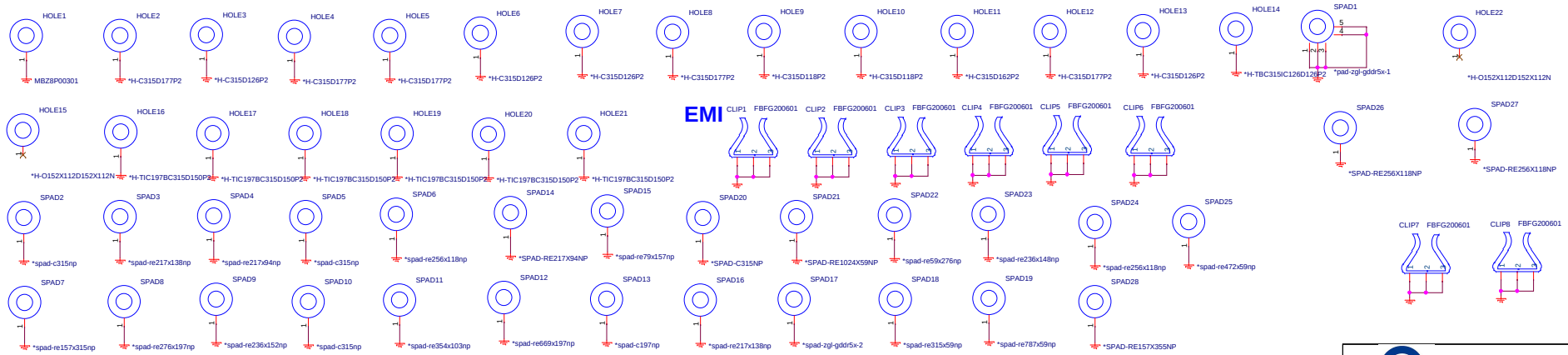
SubWoofer



Option	Bead	Cap
B-C filterless	0 ohm short resister	Un-mount
B-C filter	PBY321611T-700Y-N HIP0805o121R-10	680pF

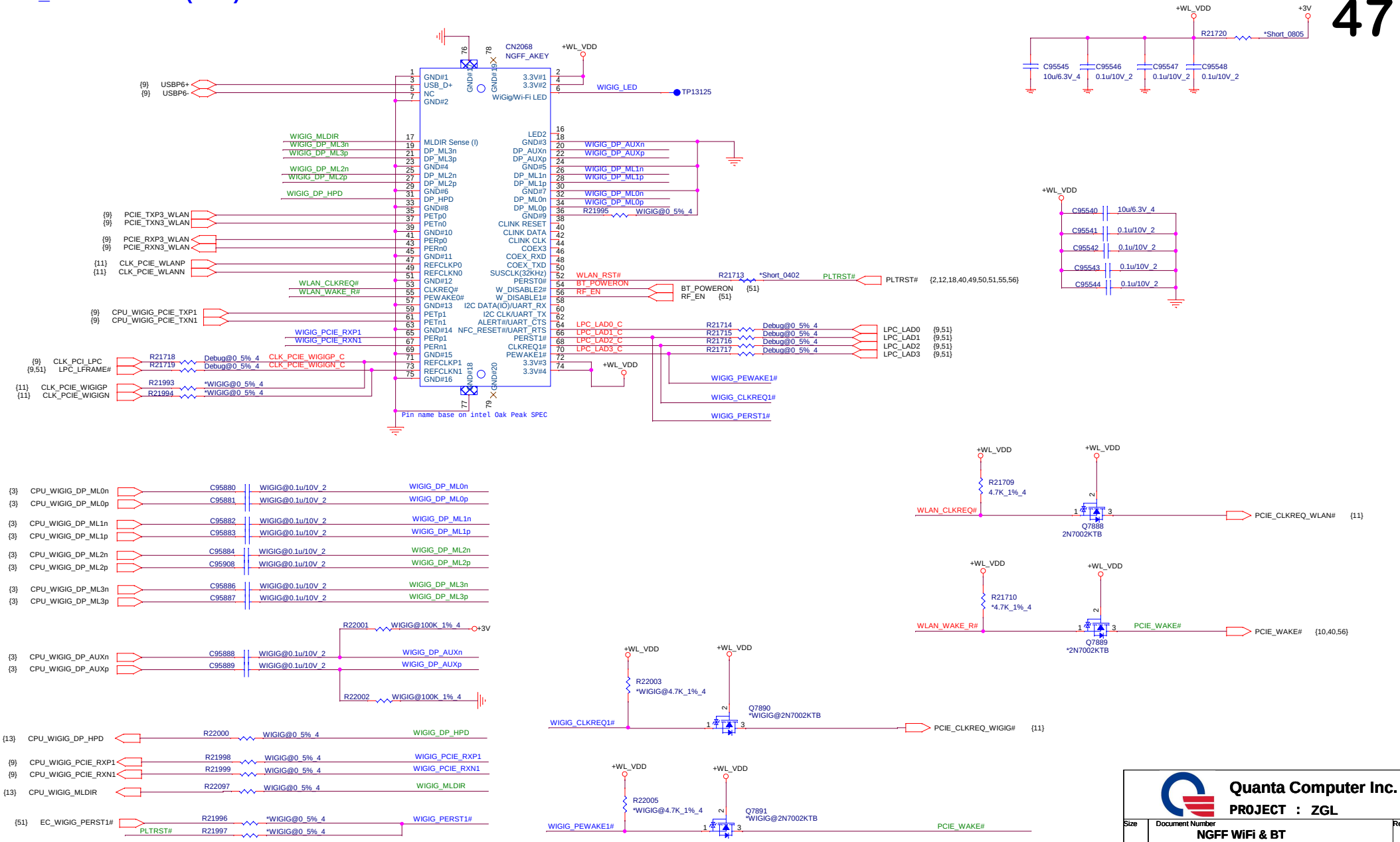
I²C Address Selection
Low:0x24
Hi:0x26

Hole



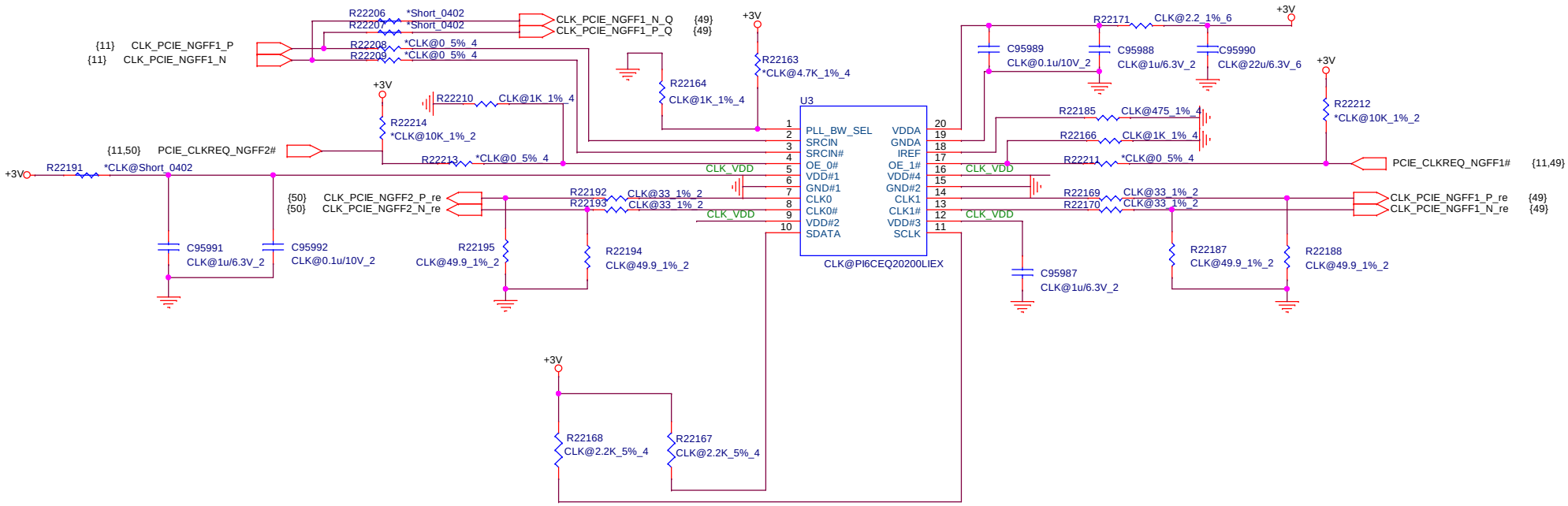
Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Subwoofer(ALC105)/HOL/EMI	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 46 of 72	

NGFF_M.2 WiFi & BT (NGF)



Quanta Computer Inc.	
PROJECT : ZGL	
Size	Document Number: NGFF WiFi & BT — Rev: 1A
Date: Thursday, July 06, 2017	Sheet 47 of 72

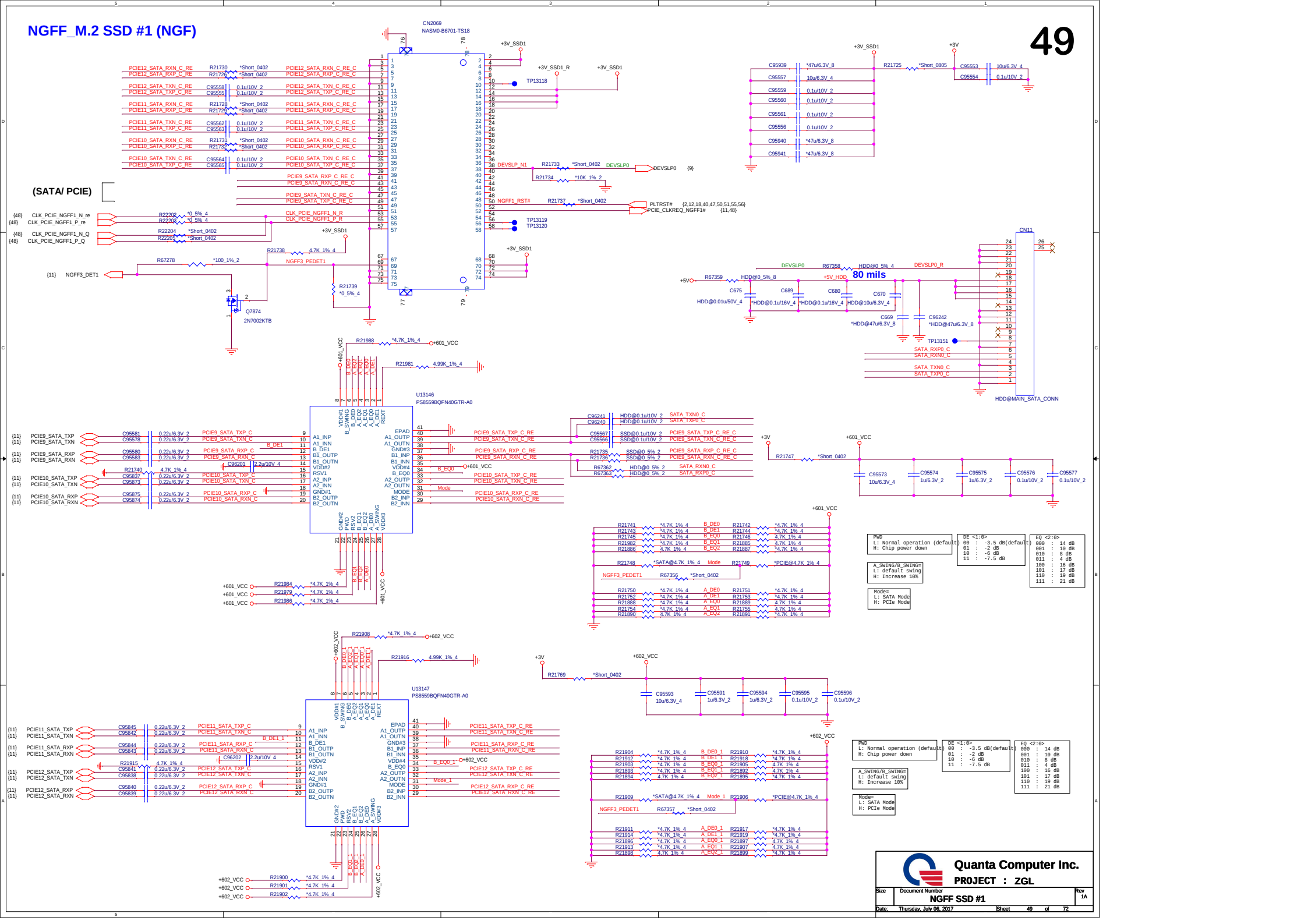
NGFF_M.2 SSD #1 #2 (NGF)



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: SSD Clock re-Driver	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 48 of 72	

NGFF_M.2 SSD #1 (NGF)

(SATA/ PCIE)



Quanta Computer Inc.			
PROJECT : ZGL			
Size	Document Number		Rev
	NGFF SSD #1		1A
Date: Thursday, July 06, 2017	Sheet 49 of 72		

NGFF_M.2 SSD #2 (NGF)

(SATA/ PCIE)

CN2070
NASM0-B6701-TS18

U13149
PS8559BQFN40GTR-A0

U13148
PS8559BQFN40GTR-A0

Q7875
2N7002KTB

PWD
L: Normal operation (default)
H: Chip power down

A_SWING/B_SWING=
L: default swing
H: Increase 10%

Mode=
L: SATA Mode
H: PCIe Mode

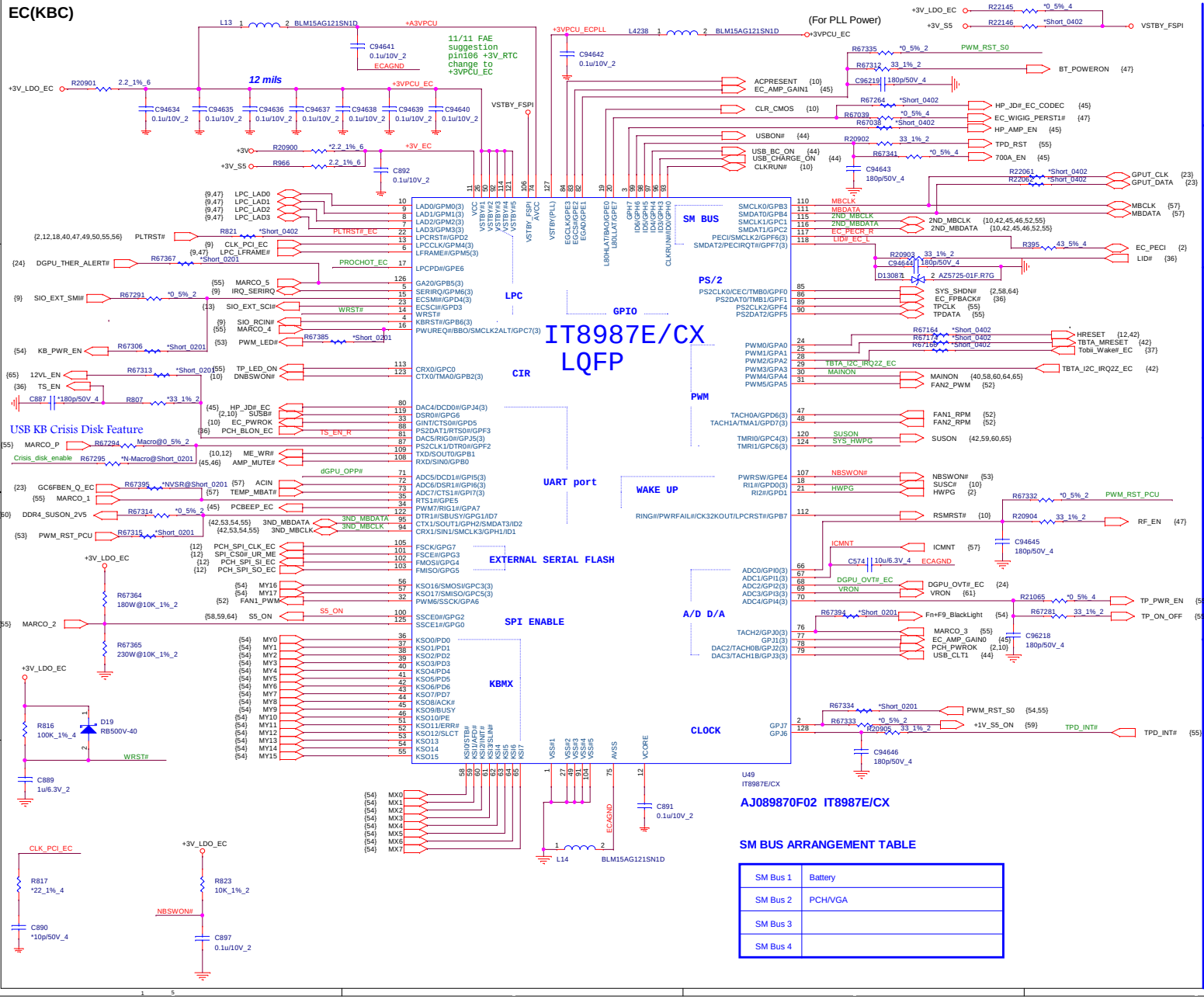
DE <1:0>
00 : -3.5 dB(default)
01 : -2 dB
10 : -6 dB
11 : -7.5 dB

EQ <2:0>
000 : 14 dB
001 : 10 dB
010 : 8 dB
011 : 4 dB
100 : 16 dB
101 : 17 dB
110 : 19 dB
111 : 21 dB

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	NGFF SSD #2	1A
Date: Thursday, July 06, 2017	Sheet 50 of 72	

EC(KBC)

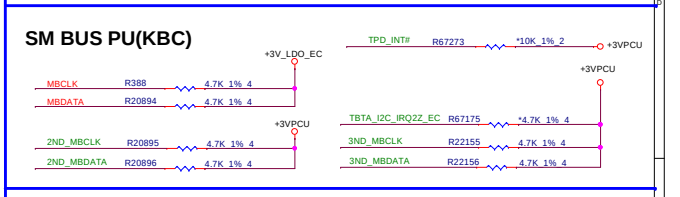


AJ089870F02 IT8987E/CX

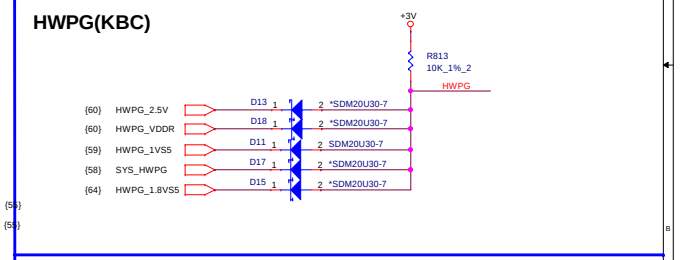
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

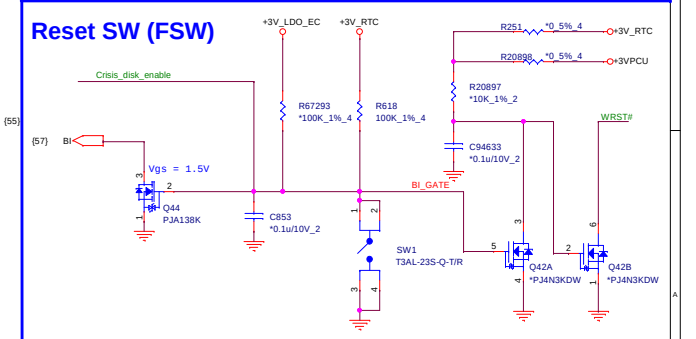
SM BUS PU(KBC)



HWPG(KBC)

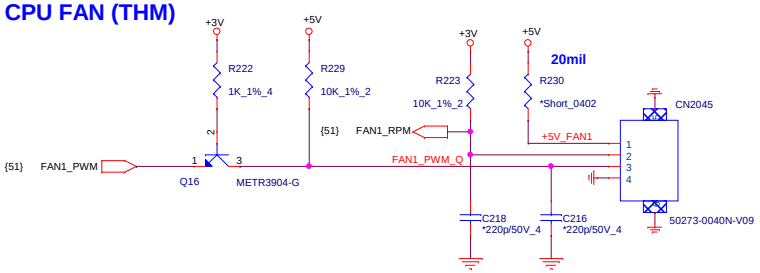


Reset SW (FSW)

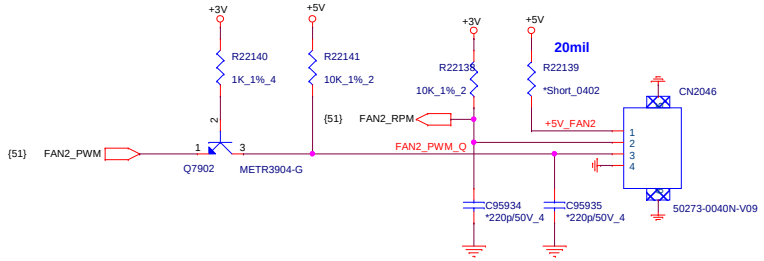


Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: KBC IT8987	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 51 of 72	

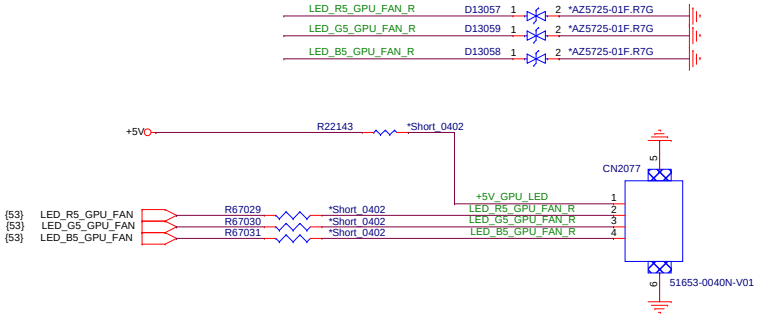
CPU FAN (THM)



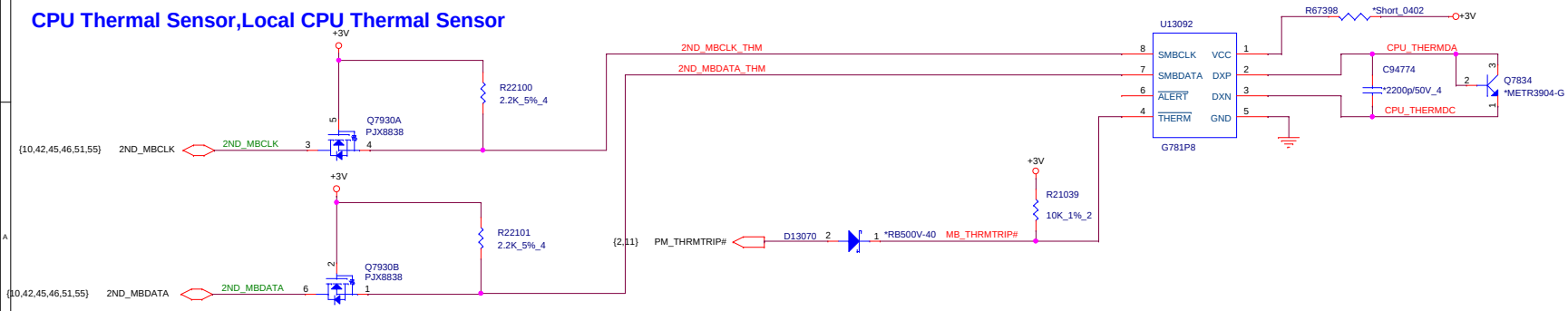
GPU FAN (THM)



GPU FAN LED



CPU Thermal Sensor,Local CPU Thermal Sensor

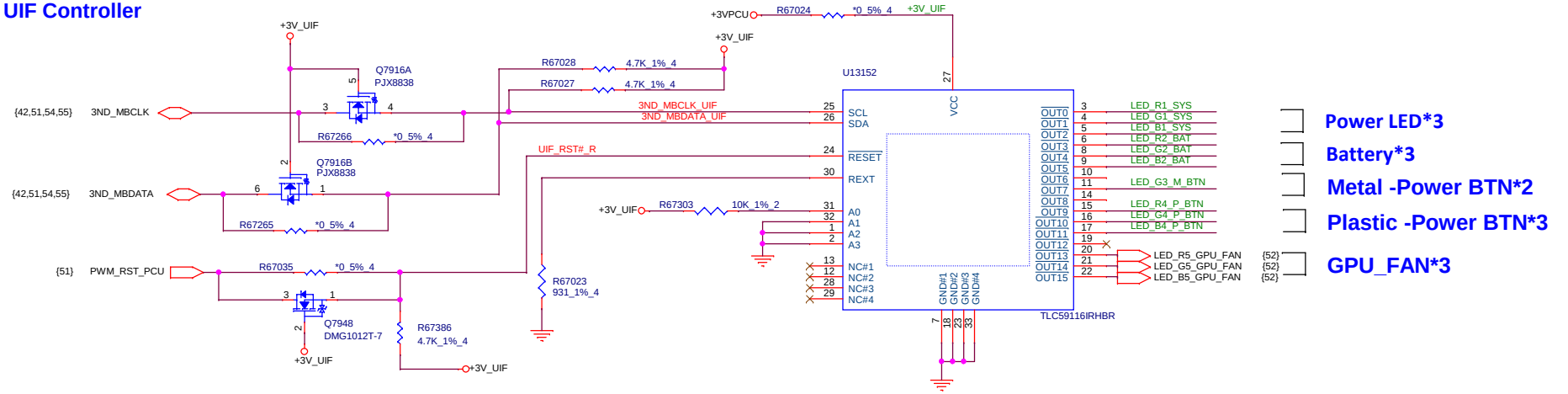


Quanta Computer Inc.

PROJECT : ZGL

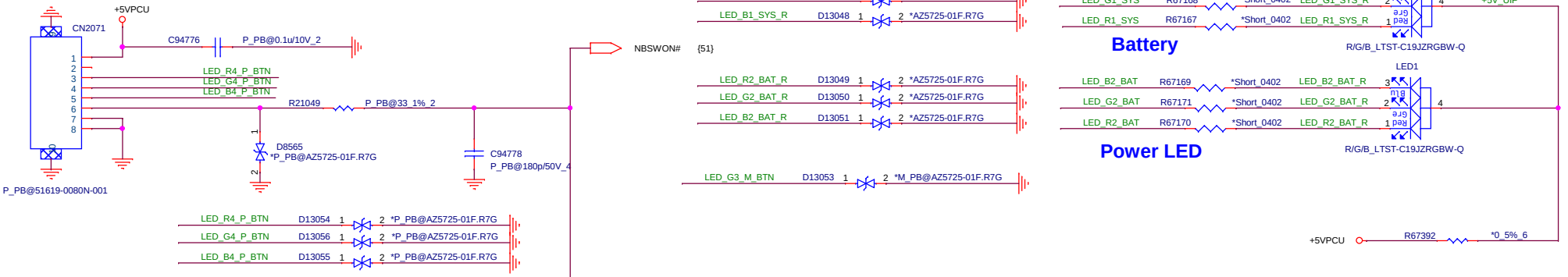
Size	Document Number	Rev
	FAN,Thermal,FAN LED	1A
Date: Thursday, July 06, 2017	Sheet 52 of 72	

UIF Controller



Power LED*3
Battery*3
Metal -Power BTN*2
Plastic -Power BTN*3
GPU_FAN*3

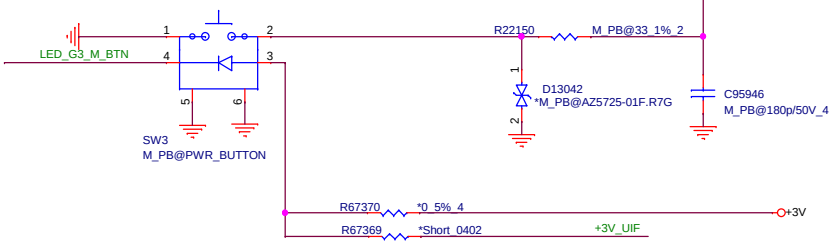
Plastic -Power BUTTON

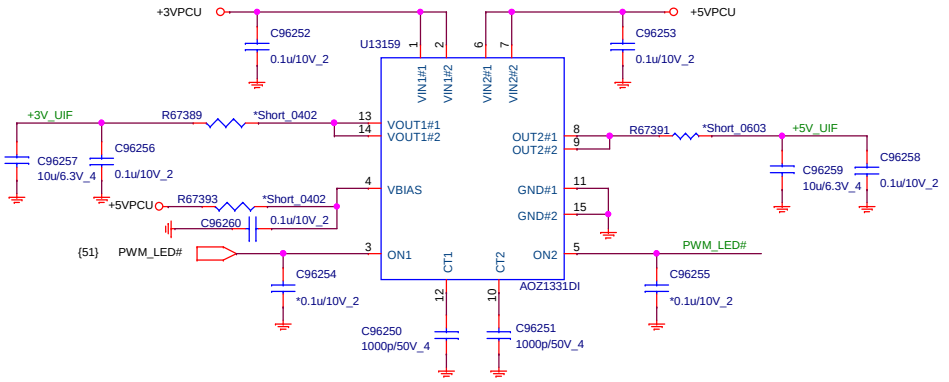


Battery

Power LED

Metal -Power BUTTON

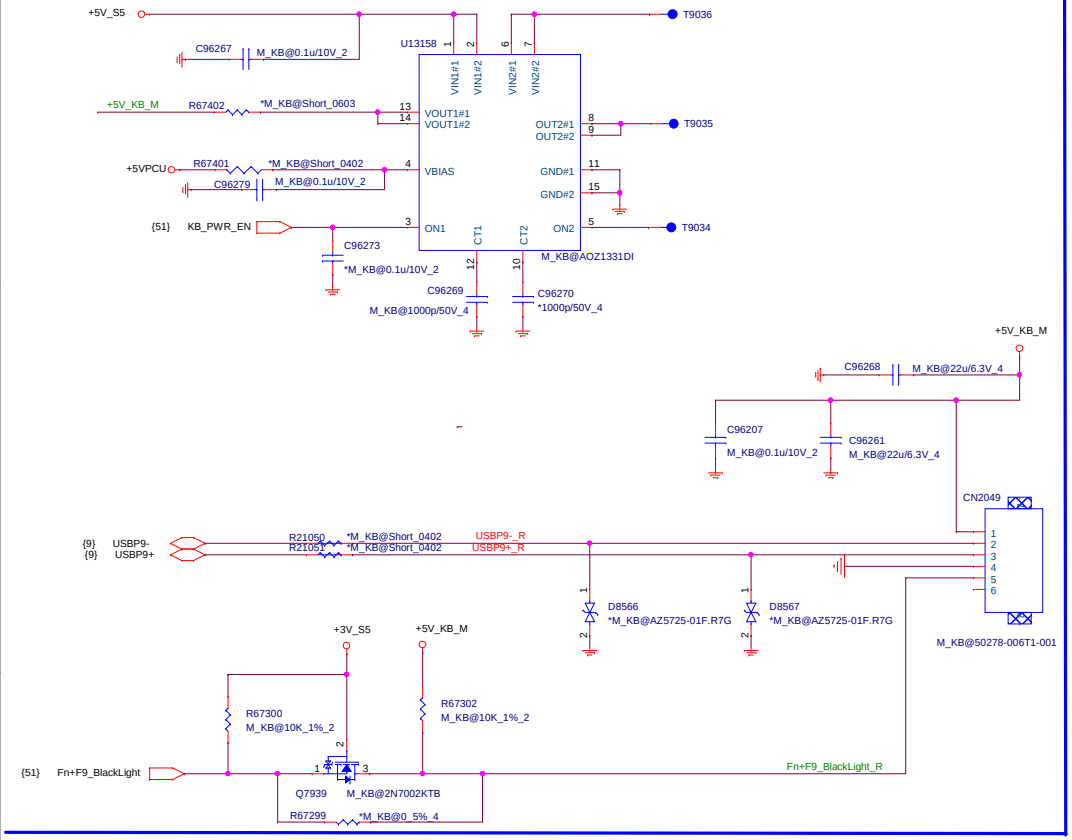




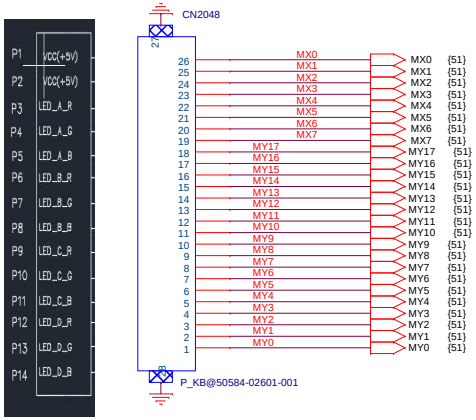
Quanta Computer Inc.
PROJECT : ZGL

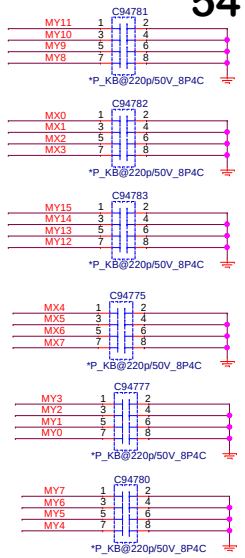
Size	Document Number	Rev
	Power Board , UIF LED	1A
Date: Thursday, July 06, 2017	Sheet 53 of 72	

Metal KB(Z=6.8mm)

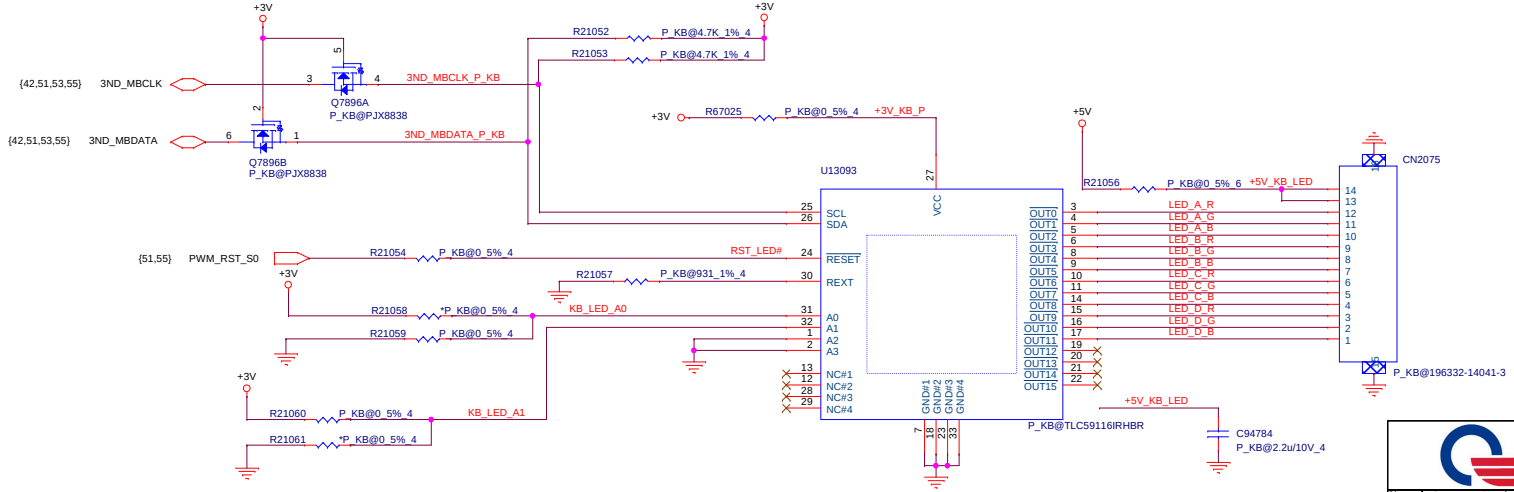


Plastic KB(Z=5.8mm)





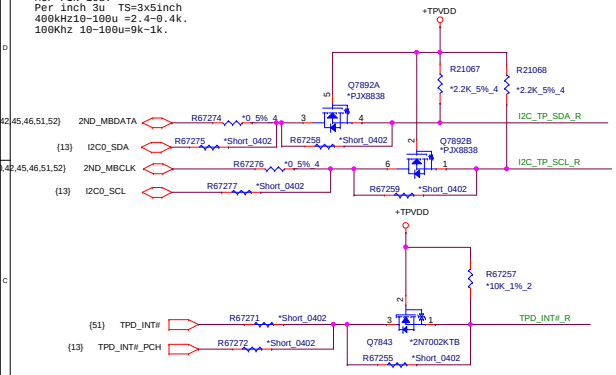
Plastic KB(Z=5.8mm)



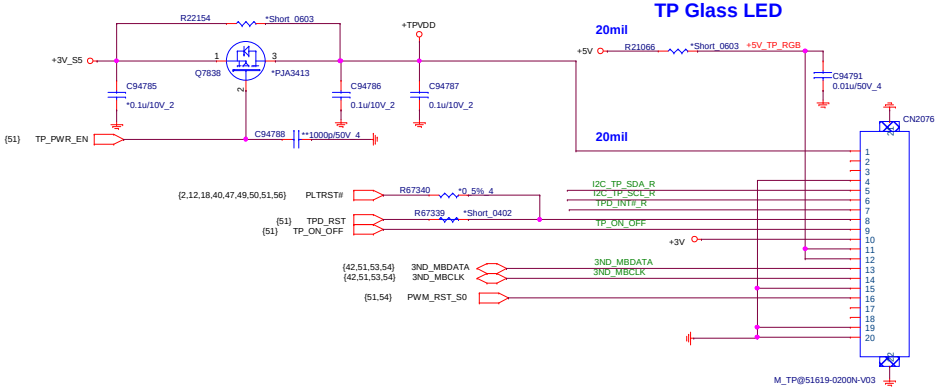
Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: KeyBoard	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 54 of 72	

Metal-Touch PAD

```
TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u  TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.
```



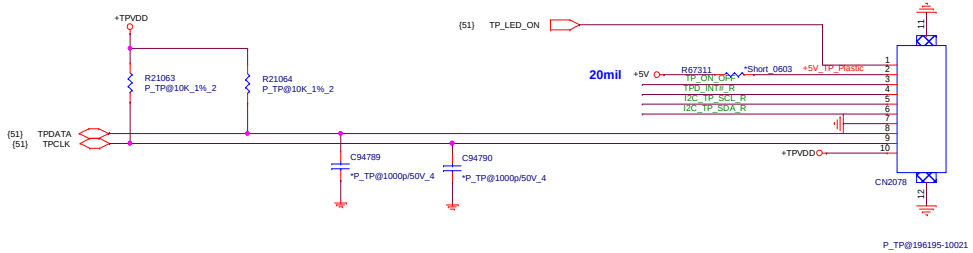
TP Glass LED



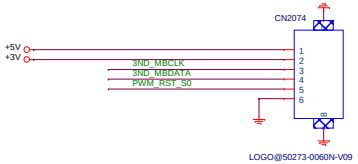
Macro Key LED

55

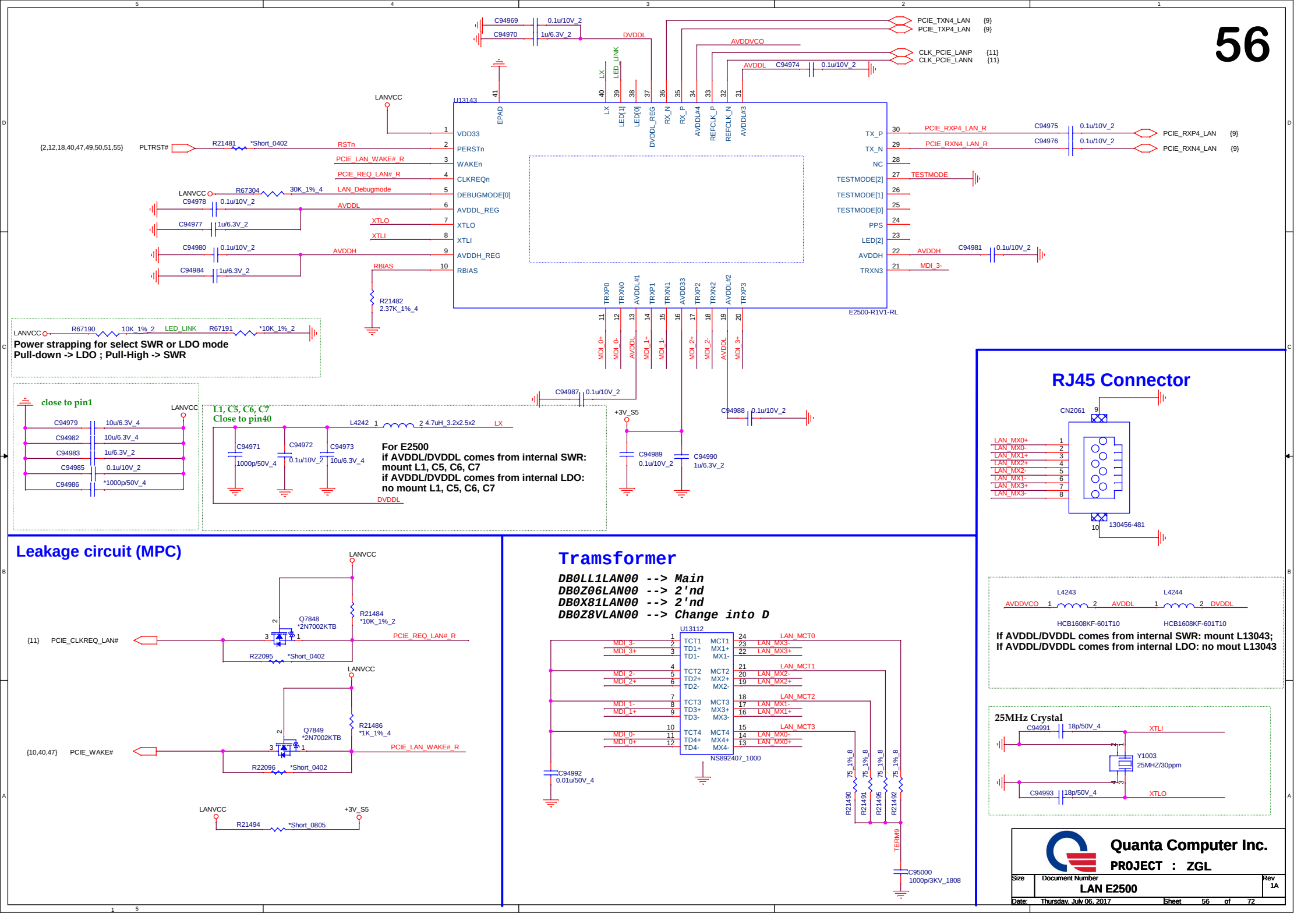
Plastic-Touch PAD



LCD Cover LED



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Macro key/LCD Cover/TP	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 55 of 72	



RJ45 Connector

Leakage circuit (MPC)

Tramsformer

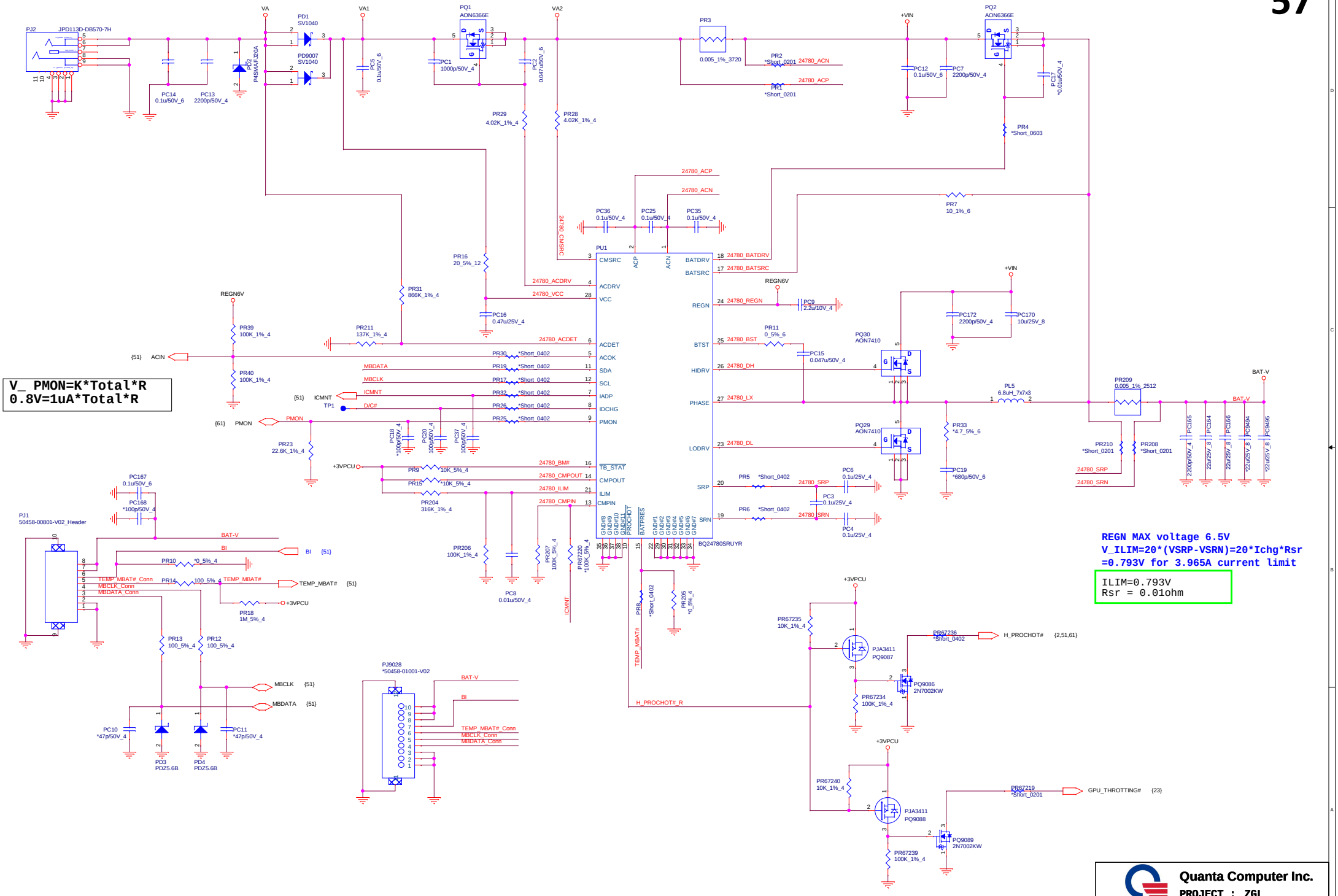
DB0LL1LAN00 --> Main
DB0Z06LAN00 --> 2'nd
DB0X81LAN00 --> 2'nd
DB0Z8VLAN00 --> Change into D

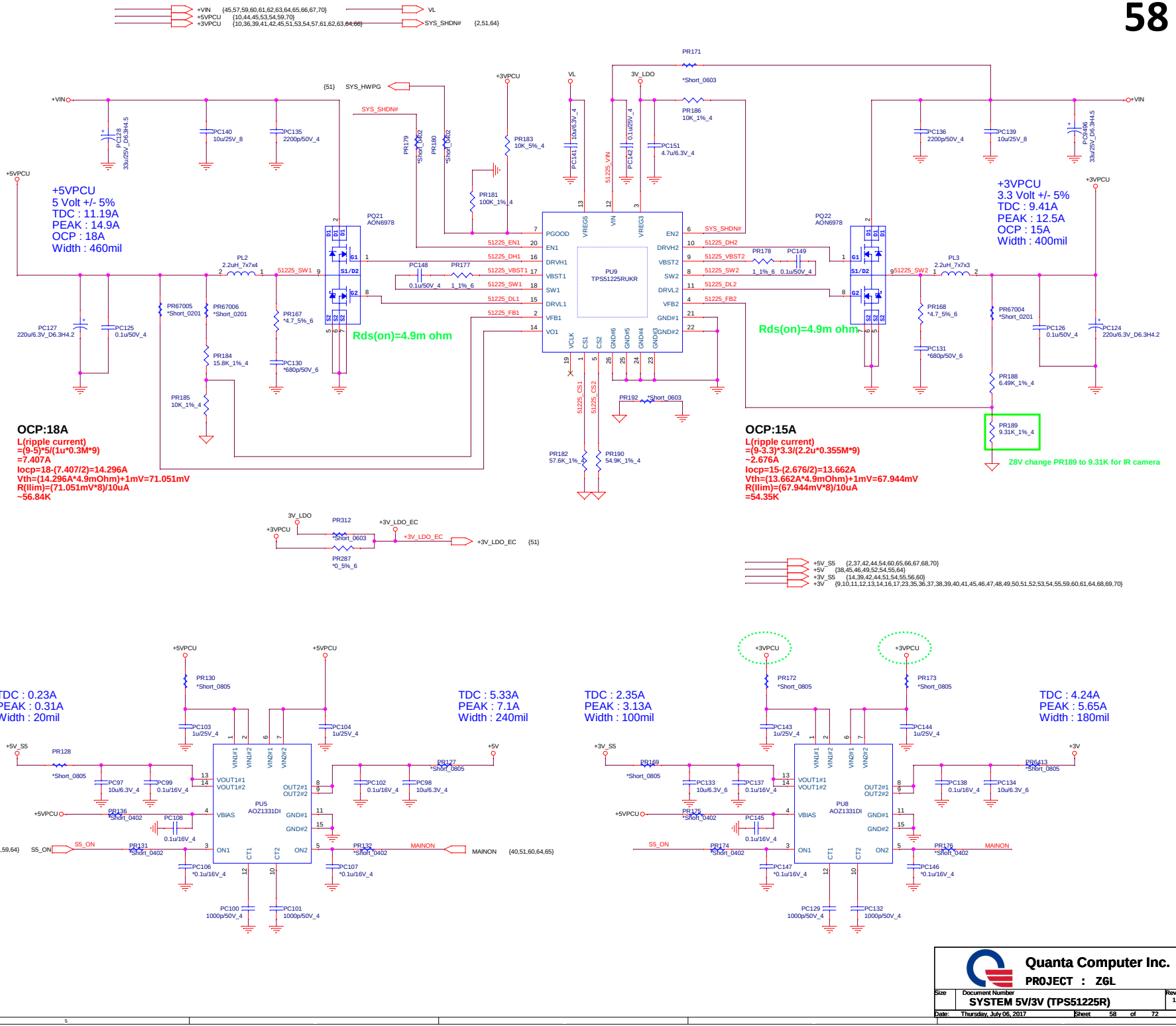
If AVDDL/DVDDL comes from internal SWR: mount L13043;
If AVDDL/DVDDL comes from internal LDO: no mout L13043

25MHz Crystal

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	LAN E2500	1A
Date: Thursday, July 06, 2017	Sheet 56 of 72	


V_ PMON=K*Total*R
0.8V=1uA*Total*R
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
BQ24780SRUYR
Quanta Computer Inc.
PROJECT : ZGL
Charger (BQ24780S)
Thursday, July 06, 2017



Quanta Computer Inc.			
PROJECT : ZGL			
Size	Document Number		Rev
	SYSTEM 5V/3V (TPS51225R)		1A
Date: Thursday, July 06, 2017		Sheet 58 of 72	

+VIN {45,57,58,60,61,62,63,64,65,66,67,70}
+1V_S5 {10,11,14}
+5VPCU {10,44,45,53,54,58,70}
+3V {9,10,11,12,13,14,16,17,23,35,36,37,38,39,40,41,45,46,47,48,49,50,51,52,53,54,55,58,60,61,64,68,69,70}
+1V_SUS {2,6,10,61}
+VCCIO {2,3,6,10,23,61,64}

+1V_S5_VIN
PJ3004 *short3720
+VIN
+5VPCU
PC220 2200p/50V_6
PC221 10u/25V_8
PC223 1u/10V_4
+3V
PR263 100K_1%_4
PU9015 RT8237CZQW_2
PQ9053 AON6978
{51} HWPG_1VS5
{51,58,64} S5_ON
{51} +1V_S5_ON
PR266 *Short_0402
PR115 *0_5%_4
PR114 *100K_1%_4
PR265 42.2K_1%_4
PR268 470K_1%_4
51211V_EN
51211V_TRIP
51211V_TST
PGOOD EN CS RF VCC FB
UGATE BOOT PHASE LGATE GND#1
51211V_DRVH
51211V_VBST
51211V_SW
51211V_DRVL
PR264 *Short_0603
PC222 0.1u/50V_6
G1 S1/D2 G2 D1 D1 D1 S2 S2 S2
PL12 0.68uH_7x7x3
51211V_SW
PR112 *4.7_5%_6
PC81 *680p/50V_6
PR67007 *Short_0201
PC217 0.1u/50V_6
PC219 330u/2V_7343H1.9
+1V_S5_SRC
PJ3005 *short3720
+1V_S5

+1V_S5
1.0 Volt +/- 5%
TDC : 8.19A
PEAK : 10.92A
OCP : 13A
Width : 340mil

OCP=13A
L ripple current
=(19-1)*1/(0.68u*290k*19)
=4.804A
Vtrip=13-(4.804/2)*4.9mohm
=51.9302mV
Rlimit=51.9302mV/10uA*8=41.54Kohm

RDSon=4.9mohm

51211V_FB
PR67003 4.3K_1%_4
PR267 10K_1%_4
VFB=0.7V

+VIN
+1V_SUS
+VIN
+1V_S5
PR84 1M_5%_6
PR86 22_5%_8
PR66972 1M_5%_6
PR83 1M_5%_6
{42,51,60,65} SUSON
PQ8 LTC044EUBFS8TL
PQ9059 2N7002K
PQ9054 2N7002K
PC62 *2200p/50V_4
SUSD
PQ9055 PJA3404
PR255 *0_5%_6
+1V_SUS

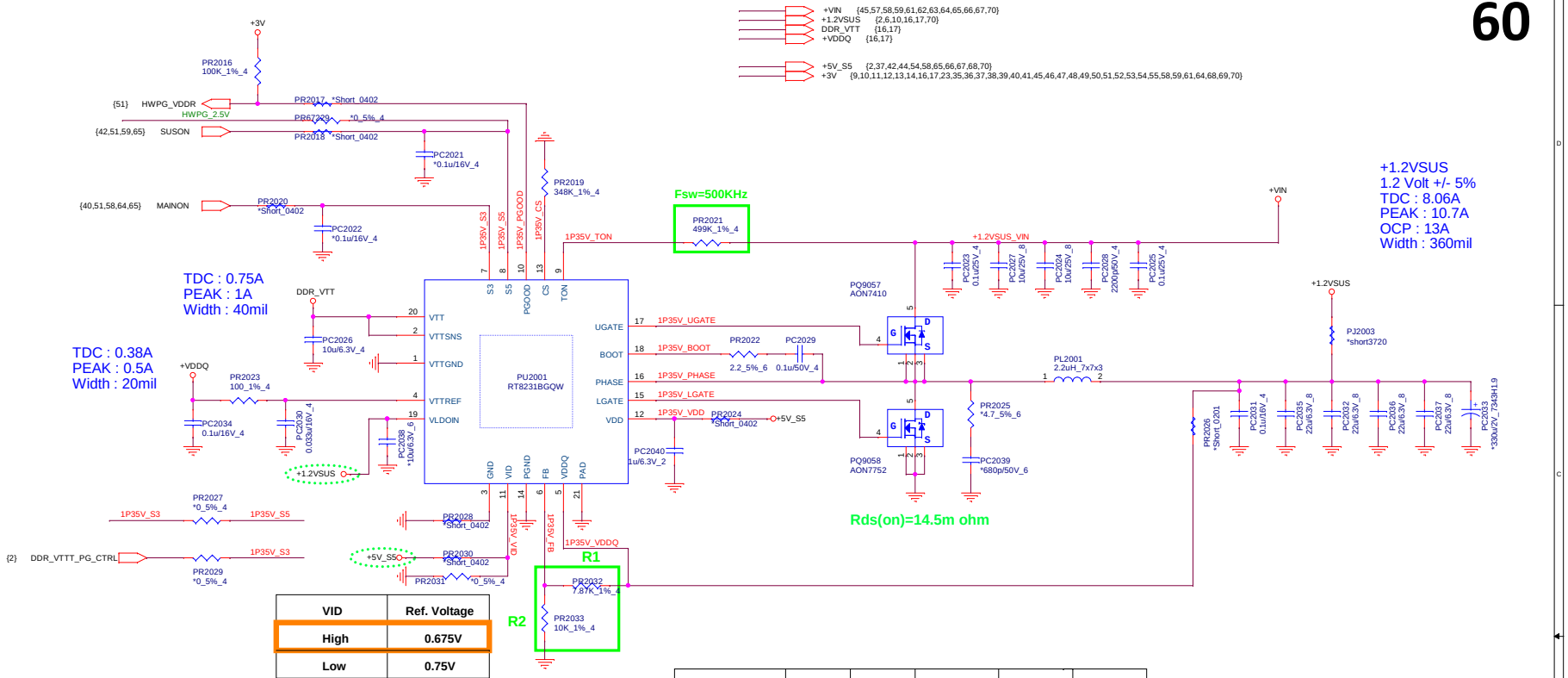
TDC : 0.23A
PEAK : 0.31A
Width : 20mil

+1V_S5
{60,64} MAIND
MAIND
PQ9056 TPCA8064-H
+VCCIO

TDC : 4.13A
PEAK : 5.5A
Width : 180mil

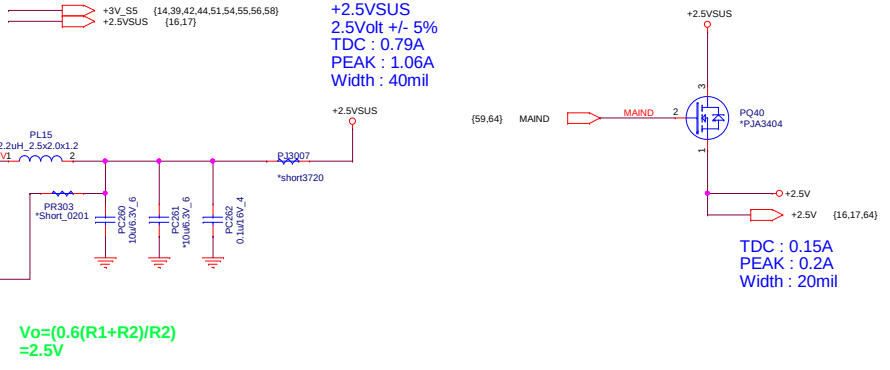
Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	+1V_S5 (RT8237CZQW)	1A
Date: Thursday, July 06, 2017	Sheet 59 of 72	

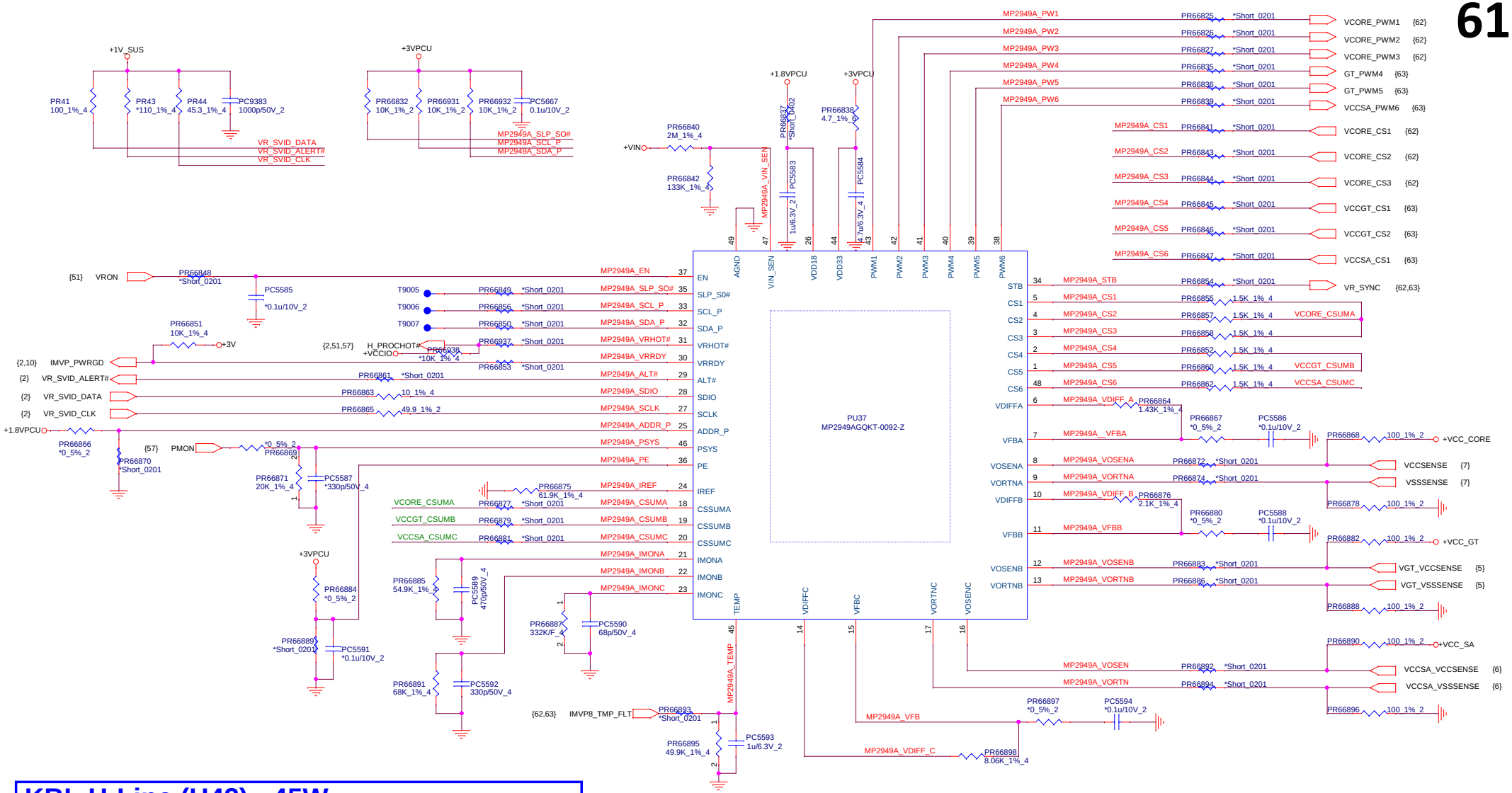


VID	Ref. Voltage
High	0.675V
Low	0.75V

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



Quanta Computer Inc.	
PROJECT : ZGL	
Size	Document Number: DDR4_+1.2VSUS (RT8231BGQW) — Rev: 1A
Date: Thursday, July 06, 2017	Sheet 60 of 72



KBL H-Line (H42) - 45W (3+2+1 Phase)

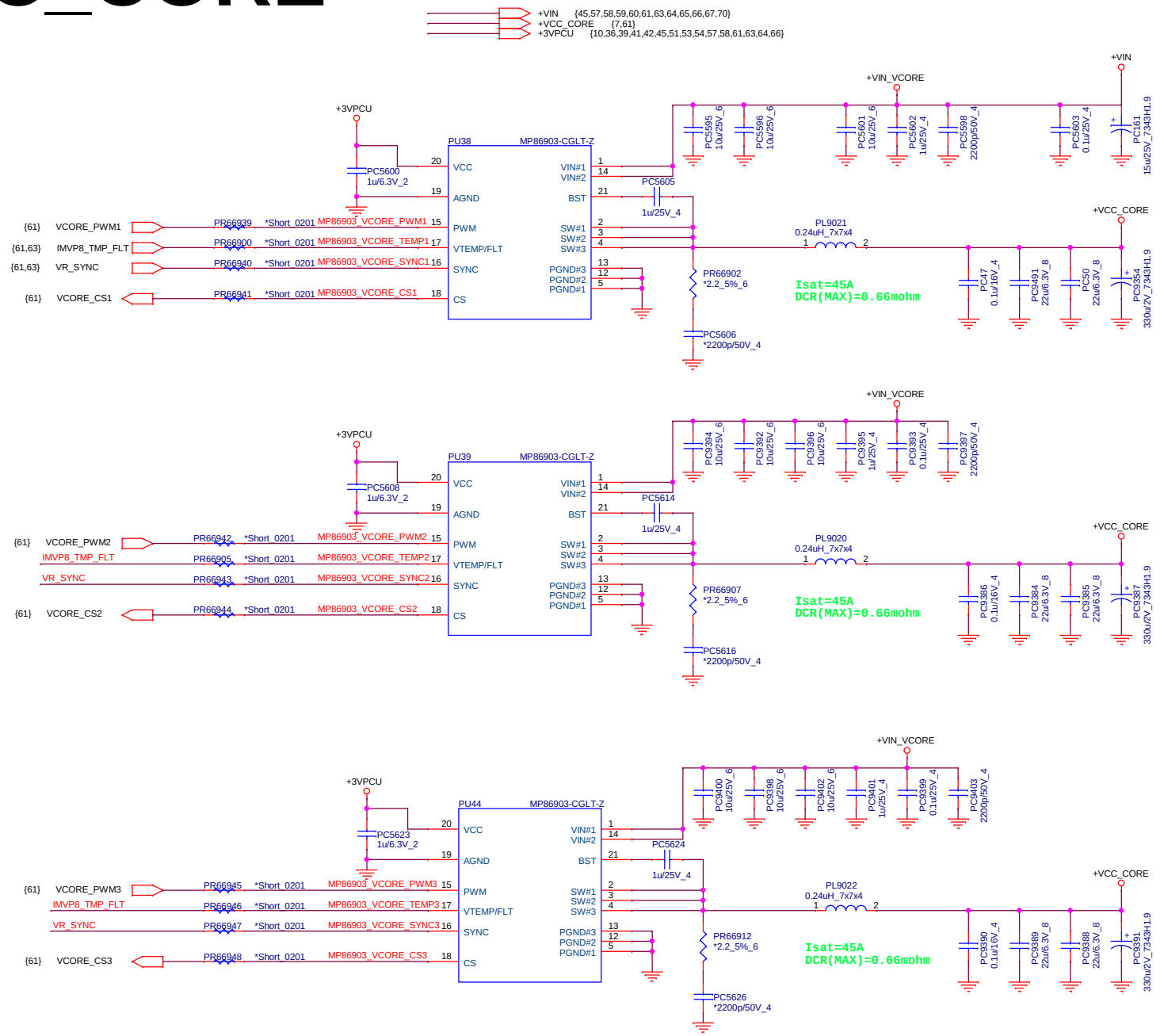
Vcore	VCCGT	VCCSA
Icc TDC：50A	Icc TDC：25A	Icc TDC：10A
Icc Max：68A	Icc Max：55A	Icc Max：11.1A
OCP：92A	OCP：75A	OCP：16A
VCORE L/L：	**VCORE L/L：**	**VCORE L/L：**
R_DC_LL：1.8mV/A	R_DC_LL：2.65mV/A	R_DC_LL：10mV/A
R_AC_LL：1.8mV/A	R_AC_LL：2.65mV/A	R_AC_LL：10mV/A

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	CPU VR IC (MP2949A)	1A
Date: Thursday, July 06, 2017	Sheet 61 of 72	

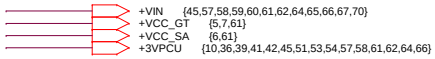
+VCC_CORE

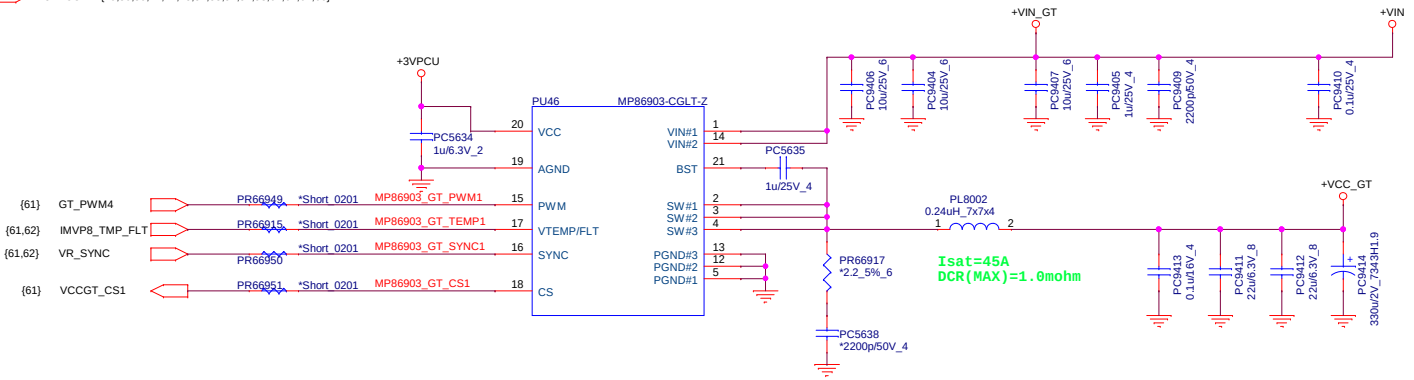
62

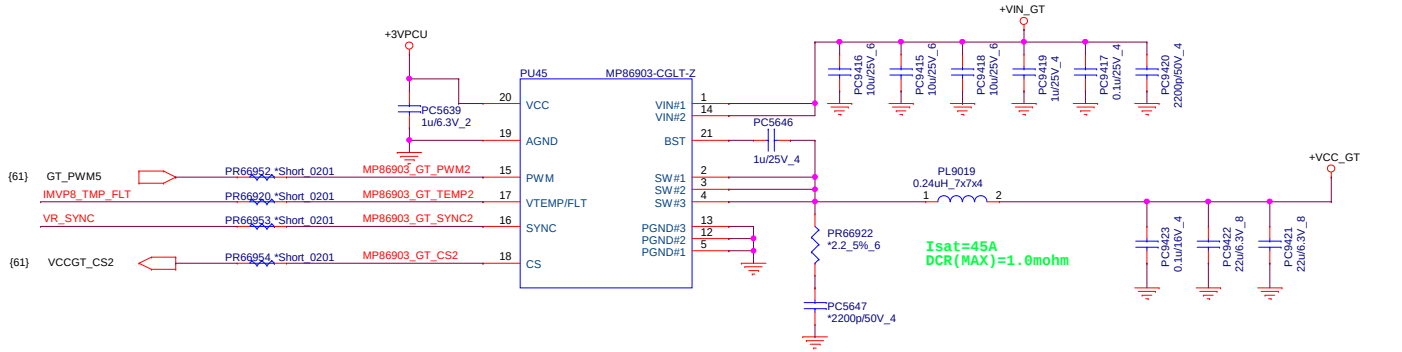


Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: +VCC_CORE (MP86903)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 62 of 72	

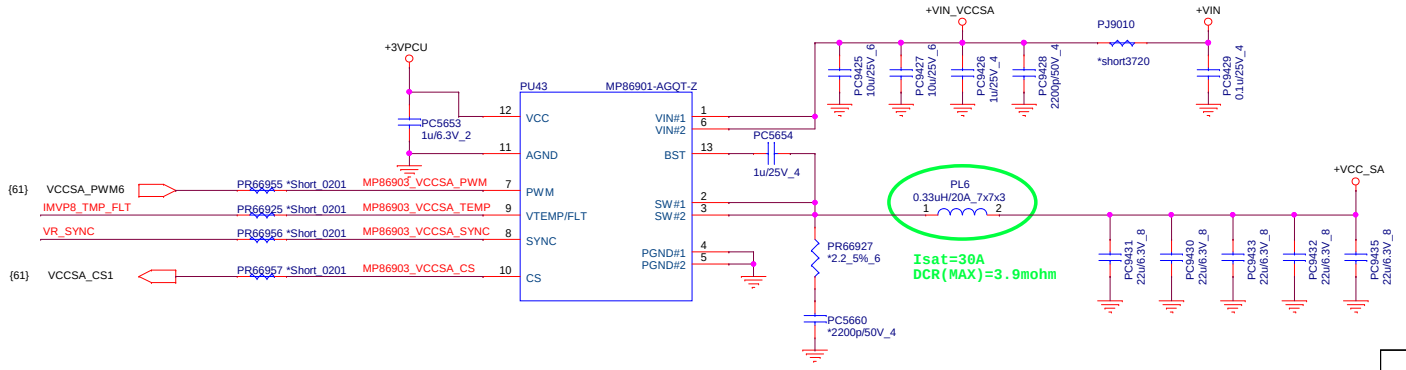
GT







VCCSA



Quanta Computer Inc.

PROJECT : ZGL

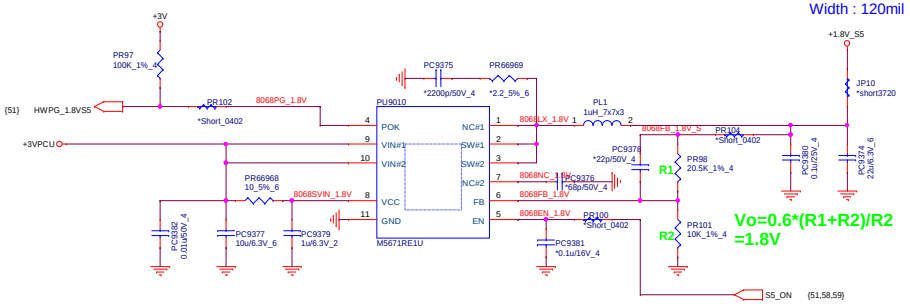
Size	Document Number	Rev
	+VCCGT/SA (MP86901)	1A

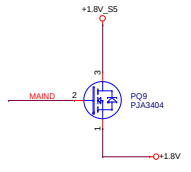
Date: Thursday, July 06, 2017 Sheet 63 of 72

+3VPCU {10,36,39,41,42,45,51,53,54,57,58,61,62,63,66}
+1.8V_S5 {70}
+1.8V {24,36,45,46}
+3V_S5 {14,39,42,44,51,54,55,56,58,60}
+3V {8,10,11,12,13,14,16,17,23,35,36,37,38,39,40,41,45,46,47,48,49,50,51,52,53,54,55,58,59,60,61,68,69,70}
VL {58}

+VIN {45,57,58,59,60,61,62,63,65,66,67,70}
+5V {38,45,46,49,52,54,55,58}
+VCCIO {2,3,6,10,23,59,61}
+2.5V {16,17,60}

+1.8V_S5
1.8Volt +/- 5%
TDC : 2.61A
PEAK : 3.48A
Width : 120mil

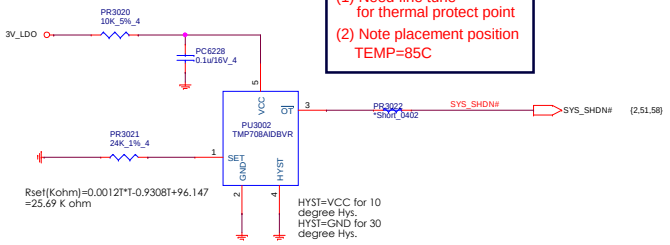


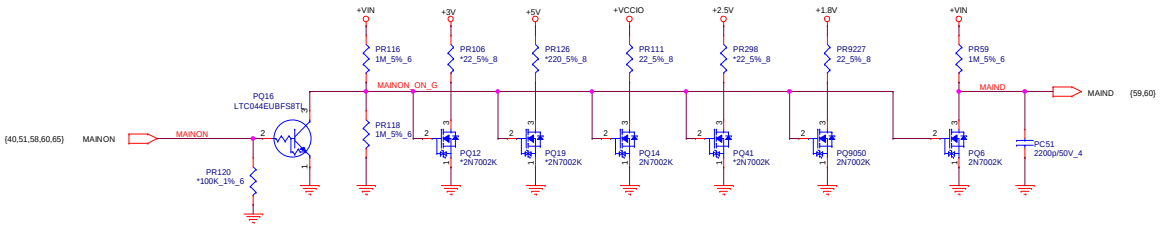


TDC : 0.08A
PEAK : 0.1A
Width : 20mil

Thermal protection

(1) Need fine tune
for thermal protect point
(2) Note placement position
TEMP=85C





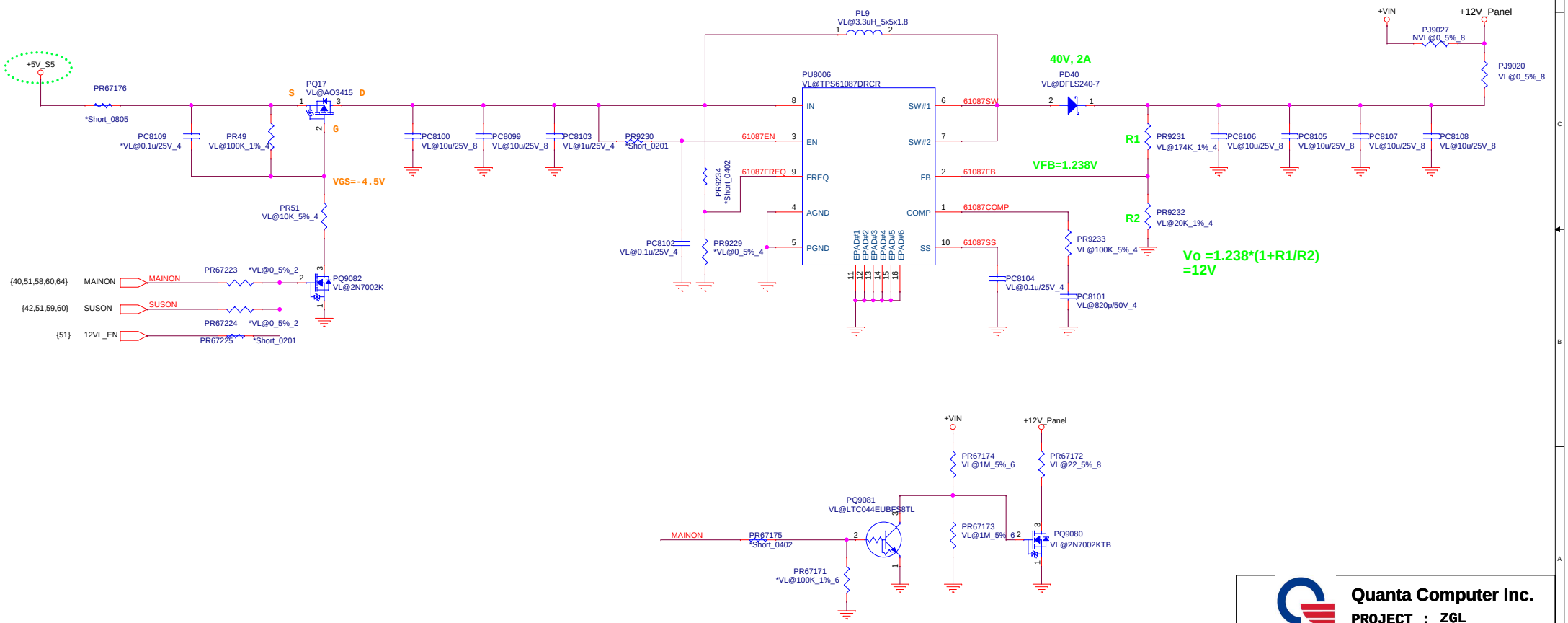
Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	+1.8V_S5/+1.5V/Thermal Protect	1A
Date: Thursday, July 06, 2017	Sheet 64 of 72	

LED Panel (TPS61087)

{2,37,42,44,54,58,60,66,67,68,70} +5V_S5
{36} +12V_Panel

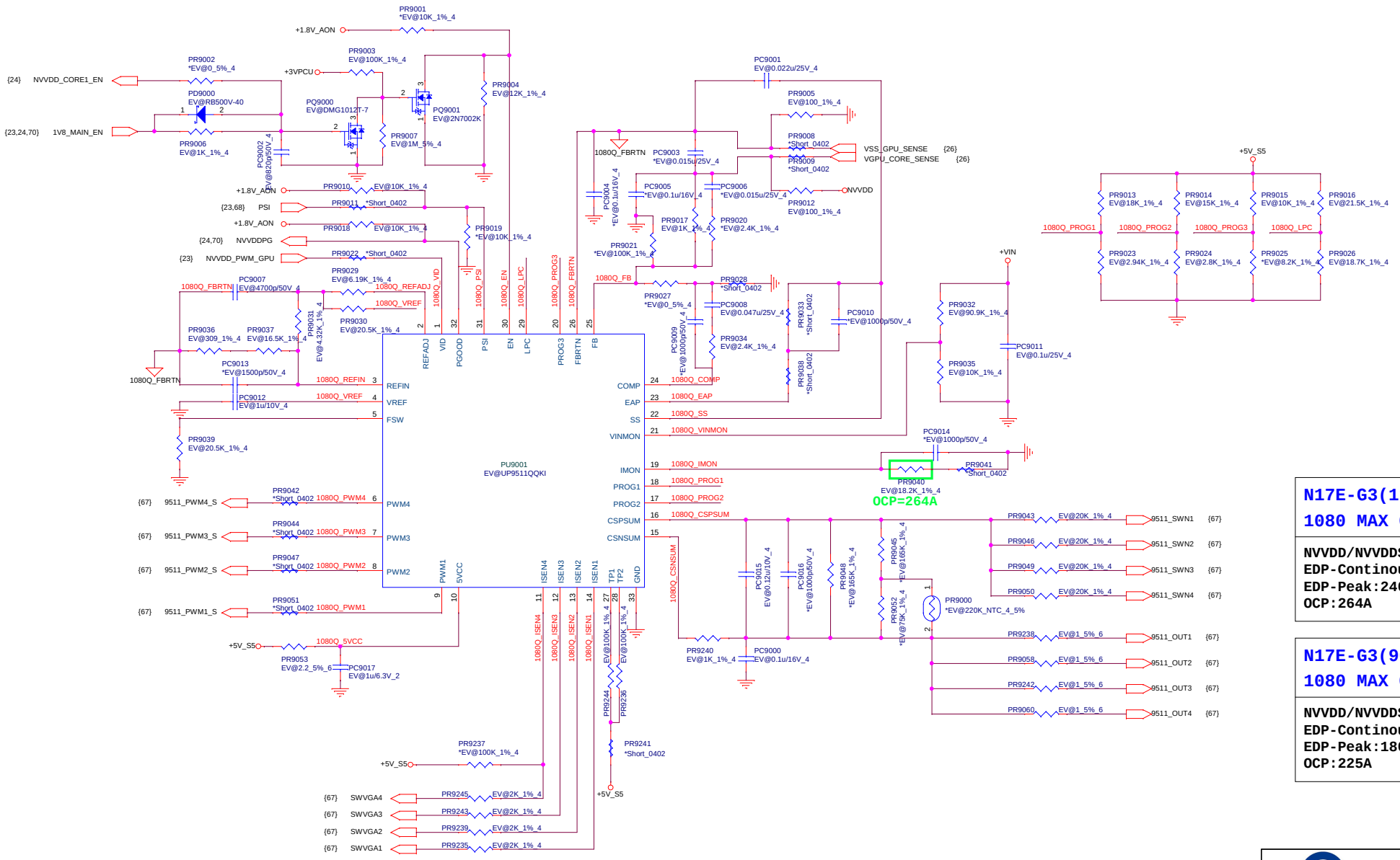
+12V_Panel
12 Volt +/- 5%
PEAK : 0.442A
Width : 20mil



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: LED Panel (TPS61087)	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 65 of 72	

VGA Core - NVVDD/NVDDS

+VIN {45,57,58,59,60,61,62,63,64,65,67,70}
NVVDD {26,67}
+5V_S5 {2,37,42,44,54,58,60,65,67,68,70}
+1.8V_AON {18,21,22,23,24,25,34,68,70}



N17E-G3(110W/GDDR5)
1080 MAX Q

NVVDD/NVDDS
EDP-Continous:104.6A
EDP-Peak:240A
OCP:264A

N17E-G3(90W/GDDR5)
1080 MAX Q

NVVDD/NVDDS
EDP-Continous:89A
EDP-Peak:180A
OCP:225A

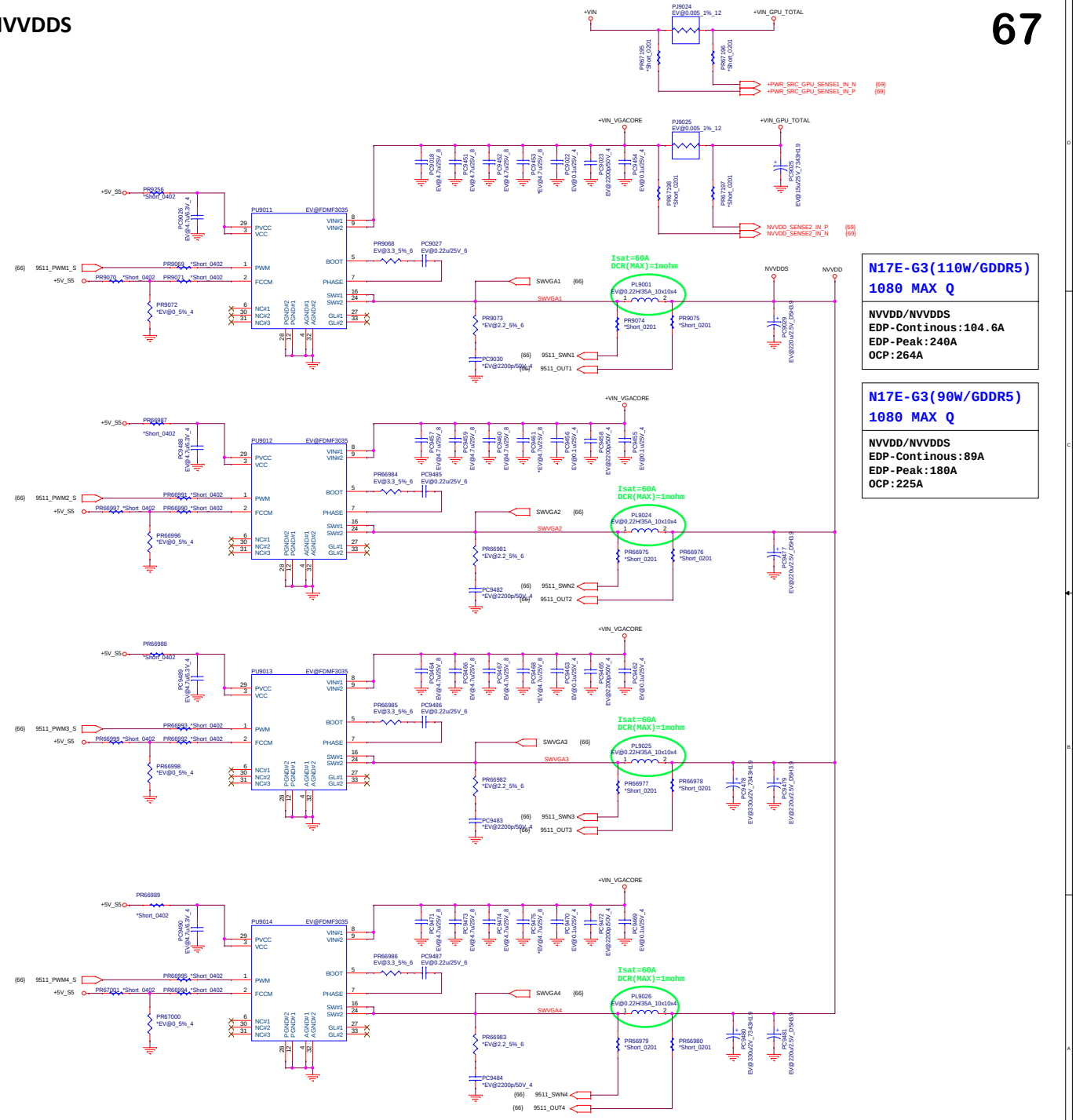
Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	+VGACORE (uP9511QQKI)	1A

Date: Thursday, July 06, 2017 Sheet 66 of 72

MAX Q : NVVDD&NVVDDS

+VIN (45,57,58,59,60,61,62,63,64,65,66,70)
+VIN_GPU_TOTAL (68)
NVVDD (26,66)
NVVDDS (26,66)
+5V_S5 (2,37,42,44,54,58,60,65,66,68,70)



N17E-G3(110W/GDDR5)
1080 MAX Q

NVVDD/NVVDDS
EDP-Continous:104.6A
EDP-Peak:240A
OCP:264A

N17E-G3(90W/GDDR5)
1080 MAX Q

NVVDD/NVVDDS
EDP-Continous:89A
EDP-Peak:180A
OCP:225A

Quanta Computer Inc.
PROJECT : ZGL
Size | Document Number | Rev
+VGPU (uP9511QQKI) | 1A
Date: Thursday, July 06, 2017 | Sheet 67 of 72

VGA Core - FBVDDQ_MEM

+VIN_GPU_TOTAL {67}
FBVDDQ_MEM {18,19,20,25,27,28,29,30,31,32,33,34}
+5V_S5 {2,37,42,44,54,58,60,65,66,67,70}
+1.8V_AON {18,21,22,23,24,25,34,66,70}
+3V {9,10,11,12,13,14,16,17,23,35,36,37,38,39,40,41,45,46,47,48,49,50,51,52,53,54,55,58,59,60,61,64,69,70}

PU9009 EV@RT8816AGQW

PR9215 EV@1_5%_6 — +5V_S5 — 1080Q_8816APVCC — 18 PVCC
PC9101 EV@2.2u/10V_4
PR9121 EV@10K_1%_4 — +3V
{24,37} PS_FBVDD_PGOOD — PR9217 *Short_0402 — 1080Q_8816APG — 13 PGOOD
PR9123 EV@15K_1%_4 — {24} FBVDD_EN — 1080Q_8816AEN — 3 EN
PC9112 *EV@0.047u/16V_4
PR9124 EV@12K_1%_4 — +1.8V_AON
{23,66} PSI — PR9224 *EV@0_5%_4 — 1080Q_8816APSI — 4 PSI
{23} NVVDDS_PSI — PR67009 *EV@0_5%_4
PR9126 *EV@10K_1%_4
5 VID
1080Q_8816AVREF — 1080Q_8816AVREF — 8 VREF
PR9129 EV@10K_1%_4 — PC9121 EV@0.1u/16V_4
6 REFADJ
R2 PR9131 EV@69.8K_1%_4 — R1 PR9128 EV@30.9K_1%_4
+5V_S5 — PR9132 EV@100K_1%_4
1080Q_8816AREFIN — PC9126 EV@100p/50V_4 — REFIN
PR9141 EV@75K_1%_4 — {23} MEM_VDD_CTRL
PR9140 EV@1M_5%_4 — PQ9021 EV@2N7002K
PR9139 *EV@100K_1%_4 — PQ9020 EV@METR3904-G
+VIN_FBVDDQ — PR9142 EV@1_5%_6 — PC9196 EV@1u/25V_6 — PR9145 EV@402K_1%_4 — PC9131 *EV@0.1u/25V_4 — 1080Q_8816ATON — 9 TON
21 GND

1080Q_8816AUGATE1 — 2 UGATE1 — PR9119 EV@1_5%_6 — 1080Q_8816AUGATE1_1
1080Q_8816ABOOT1 — 1 BOOT1 — PC9109 EV@0.22u/25V_6
1080Q_8816APHASE1 — 20 PHASE1
1080Q_8816ALGATE1 — 19 LGATE1
1080Q_8816AUGATE2 — 14 UGATE2 — PR66971 EV@1_5%_6 — 1080Q_8816AUGATE2_1
1080Q_8816ABOOT2 — 15 BOOT2 — PC9447 EV@0.22u/25V_6
1080Q_8816APHASE2 — 16 PHASE2
1080Q_8816ALGATE2 — 17 LGATE2
1080Q_8816ARGDN — 10 RGND — PC9128 *EV@56p/50V_4 — PR9135 *Short_0402
1080Q_8816AVSNS — 11 VSNS — PC9129 *EV@56p/50V_4 — PC9127 *EV@100p/50V_4 — PR9138 *Short_0402 — FBVDDQ_SENSE {25}
PR9136 EV@100_1%_4 — FBVDDQ_MEM
1080Q_8816ASS — 12 OCSET — PR9147 EV@86.6K_1%_4 — PC9124 *EV@56p/50V_4

OCP=65A

+VIN_FBVDDQ — PC9102 EV@10u/25V_8 — PC9103 EV@10u/25V_8 — PC9106 EV@0.1u/25V_4 — PC9107 EV@2200p/50V_4 — PC9194 EV@0.1u/25V_4
+VIN_GPU_TOTAL — PJ9002 *short3720

PQ9013 EV@AON6414AL
1080Q_8816AUGATE1_1 — PQ9049 EV@AON6752
1080Q_8816APHASE1 — PL9017 EV@0.22uH_7x7x4 — FBVDDQ_MEM
1080Q_8816ALGATE1 — PR9122 *EV@2.2_5%_6 — PC9113 *EV@2200p/50V_4
Isat=40A
DCR(MAX)=2.8mohm
PC9326 EV@22u/6.3V_8 — PC9324 *EV@22u/6.3V_8 — PC9325 *EV@22u/6.3V_8 — PC9110 EV@330u/2V_7343H1.9 — PC9305 EV@330u/2V_7343H1.9

Rds(on)=2.5mohm(MAX)

+VIN_FBVDDQ — PC9436 EV@10u/25V_8 — PC9438 EV@10u/25V_8 — PC9440 EV@0.1u/25V_4 — PC9441 EV@2200p/50V_4 — PC9442 EV@0.1u/25V_4

PQ9051 EV@AON6414AL
1080Q_8816AUGATE2_1 — PQ9052 EV@AON6752
1080Q_8816APHASE2 — PL9023 EV@0.22uH_7x7x4 — FBVDDQ_MEM
1080Q_8816ALGATE2 — PR66970 *EV@2.2_5%_6 — PC9439 *EV@2200p/50V_4
Isat=40A
DCR(MAX)=2.8mohm
PC9443 EV@47u/6.3V_6 — PC9462 *EV@47u/6.3V_6 — PC9463 *EV@47u/6.3V_6 — PC9444 EV@330u/2V_7343H1.9 — PC9446 EV@330u/2V_7343H1.9

Rds(on)=2.5mohm(MAX)

FBVDDQ_MEM — PR9208 EV@22_5%_8 — PQ9031 EV@2N7002K
+5V_S5 — PR9209 EV@100K_1%_4 — PR9210 EV@1M_5%_4 — 1080Q_8816AEN — PQ9032 EV@DMG1012T-7

RT8816AGQW	
PSI	Mode
<0.4V	1 Phase DCM
0.8V-1V	1 Phase CCM
1.4V-5.5V	2/3 Phase CCM

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V/1.5V
0	1.35V

FBVDDQ_MEM	R1	R2
1.55V	35.7K	53.6K
1.5V	30.9K	69.8K

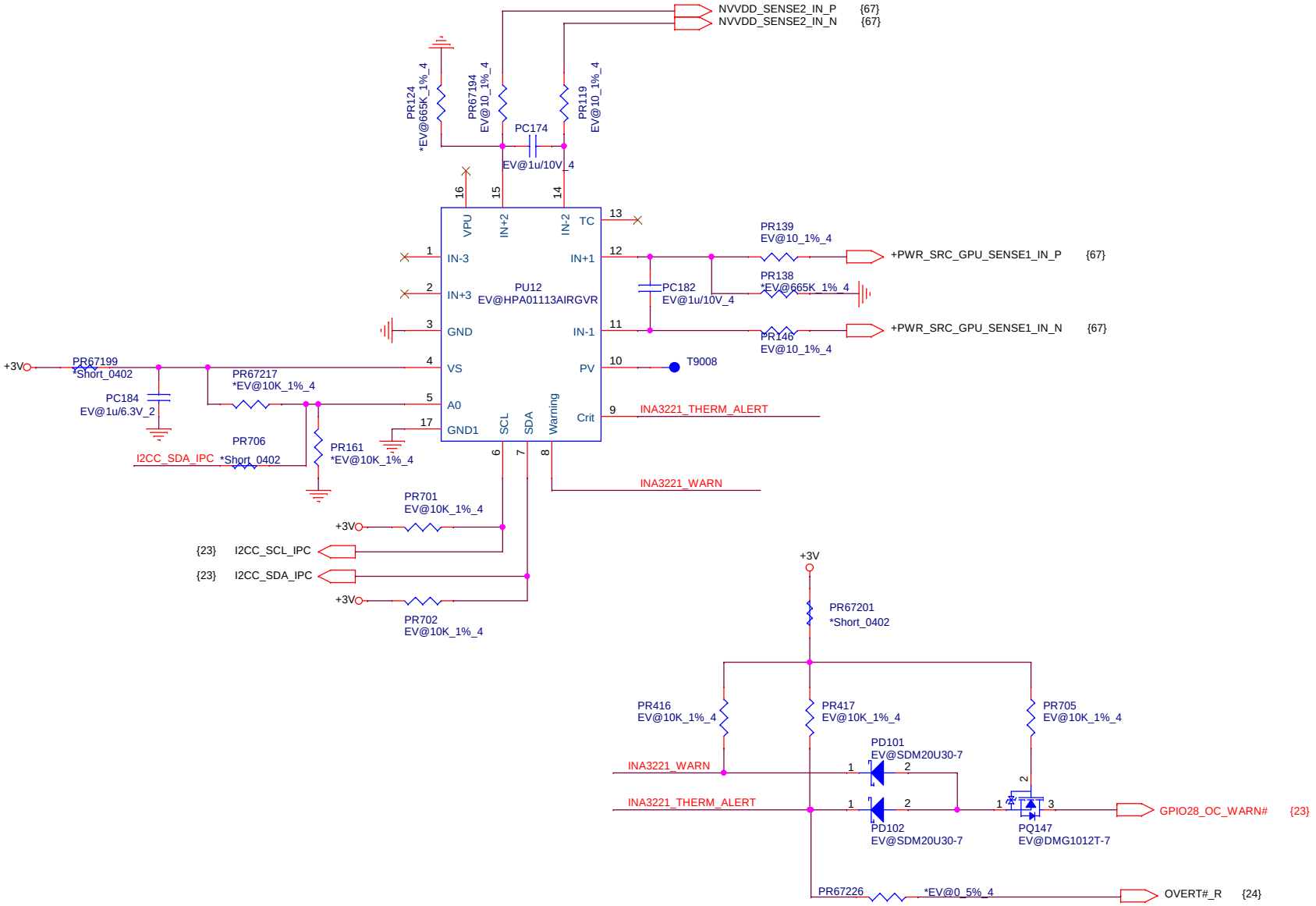
N17E-G3(90W/GDDR5)
1080Q

FBVDDQ_MEM
EDP-Continous:32.8A
EDP-Peak:47.3A
OCP:65A

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	+FBVDDQ_MEM (RT8816AGQW)	1A
Date: Thursday, July 06, 2017	Sheet 68 of 72	

+3V {9,10,11,12,13,14,16,17,23,35,36,37,38,39,40,41,45,46,47,48,49,50,51,52,53,54,55,58,59,60,61,64,68,70}



Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Current Sense	Rev: 1A
Date: Thursday, July 06, 2017	Sheet 69 of 72	

+1.8V_S5 {64}
+1.8V_MAIN {18,24,25,38}
+1.8V_AON {18,21,22,23,24,25,34,66,68}
+5VPCU {10,44,45,53,54,58,59}

TDC : 0.08A
PEAK : 0.1A
Width : 20mil

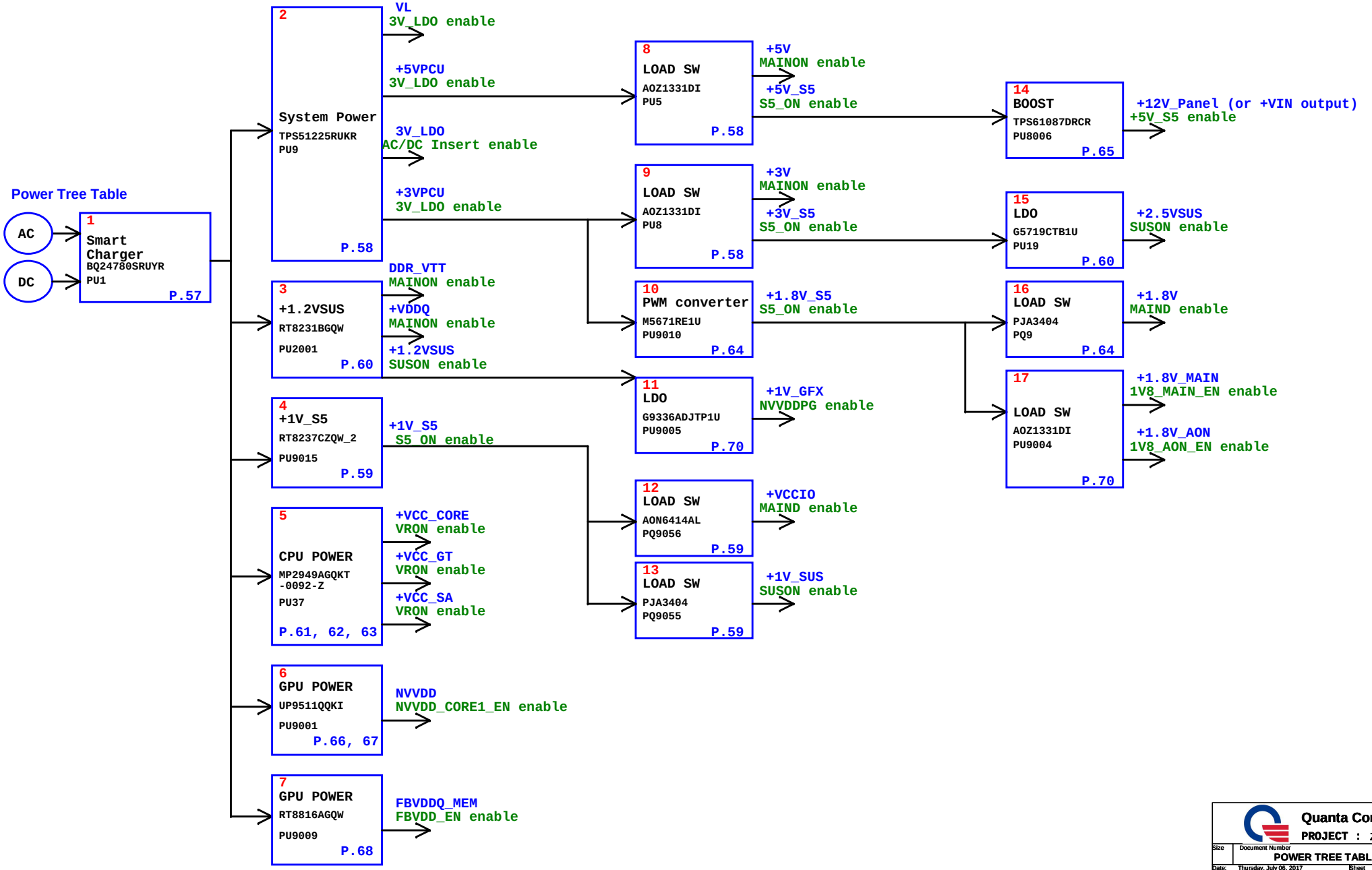
TDC : 2.21A
PEAK : 2.95A
Width : 100mil

+1.2VSUS {2,6,10,16,17,60}
+1V_GFX {18,21}
+5V_S5 {2,37,42,44,54,58,60,65,66,67,68}
+3V {9,10,11,12,13,14,16,17,23,35,36,37,38,39,40,41,45,46,47,48,49,50,51,52,53,54,55,58,59,60,61,64,68,69}

TDC : 1.52A
PEAK : 2.02A
Width : 80mil

Vout1=(1+R1/R2)*0.5
=1V

Quanta Computer Inc.			
PROJECT : ZGL			
Size	Document Number		Rev
	+1.8V_AON (AOZ1331DI)		1A
Date: Thursday, July 06, 2017	Sheet 70 of 72		



Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	POWER TREE TABLE	1A

Date: Thursday, July 06, 2017 Sheet 71 of 72

Model	Date	CHANGE LIST
ZGL REV:A	**2/16**	1. FIRST RELEASED
ZGL REV:B	**3/16**	1. Del R21309 and stuff R67240 for power sequence 2. Add D13095 for GPU_THROTTING# issue 3. Stuff Q7945 for G-sync 4. Add TVS on HDMI/DP port for MB L&L 5. Stuff R20825/R20828 for EA fail 6. Change Subwoofer ALC105 to ALC1006 for Design change 7. Reverse HDD Function 8. Change R21738/R21801 for Auto detect and change PCIE/SATA re-driver IC EQ0/EQ1 setting for EA fail
ZGL REV:C	**5/22**	1. Add C96247/C96248/C96281/C96280 for MB L&L ESD 2. Add R20915/R20917/R67381 for EDP Re-driver EA 3. Change R22118/R22119/R22120/R22121/R22122/R22123/R22124/R22125 to 6.2 ohm for HDMI EA 4. Change C94925/C94929 to 2.2UF for Codec EA 5. Change R67206/R67207 to 33 ohm for Smart AMP EA 6. Del L4271 and add U13161 for HP background noise 7. Change R382/R20887 to 100K and add U13158/U13159 circuit for S5 current leakage 8. Add Q7949 to 2nd SMBUS for USB UCSI function
ZGL REV:D	**7/6**	1. Change 0ohm resister to shortpad 2. Keep Q34 in main source: PJX138K for HDMI HDCP issue 3. Change R67206 / R67207 to 47 ohm , stuff R67263 & un-stuff R67262 , un-stuff C94947 & change R21454 to shortpad for Audio BOBO nosie 4. Change R67023 to 931 0hm for LED brightness design 5. Change MR1 (Hall sensor IC) to AL008132005 for S3 can't sleep issue 6. Keep PL8002/PL9019/PL9020/PL9021/PL9022 PN (CV+24Z0MZ00 (CYN)) for Noise