Drax MLK/Rocket MLK 11.6" Schematic

Stoney Ridge FT4

2018-01-02
REV : A00

DY : None Installed
0SP/1SP : different config for storage

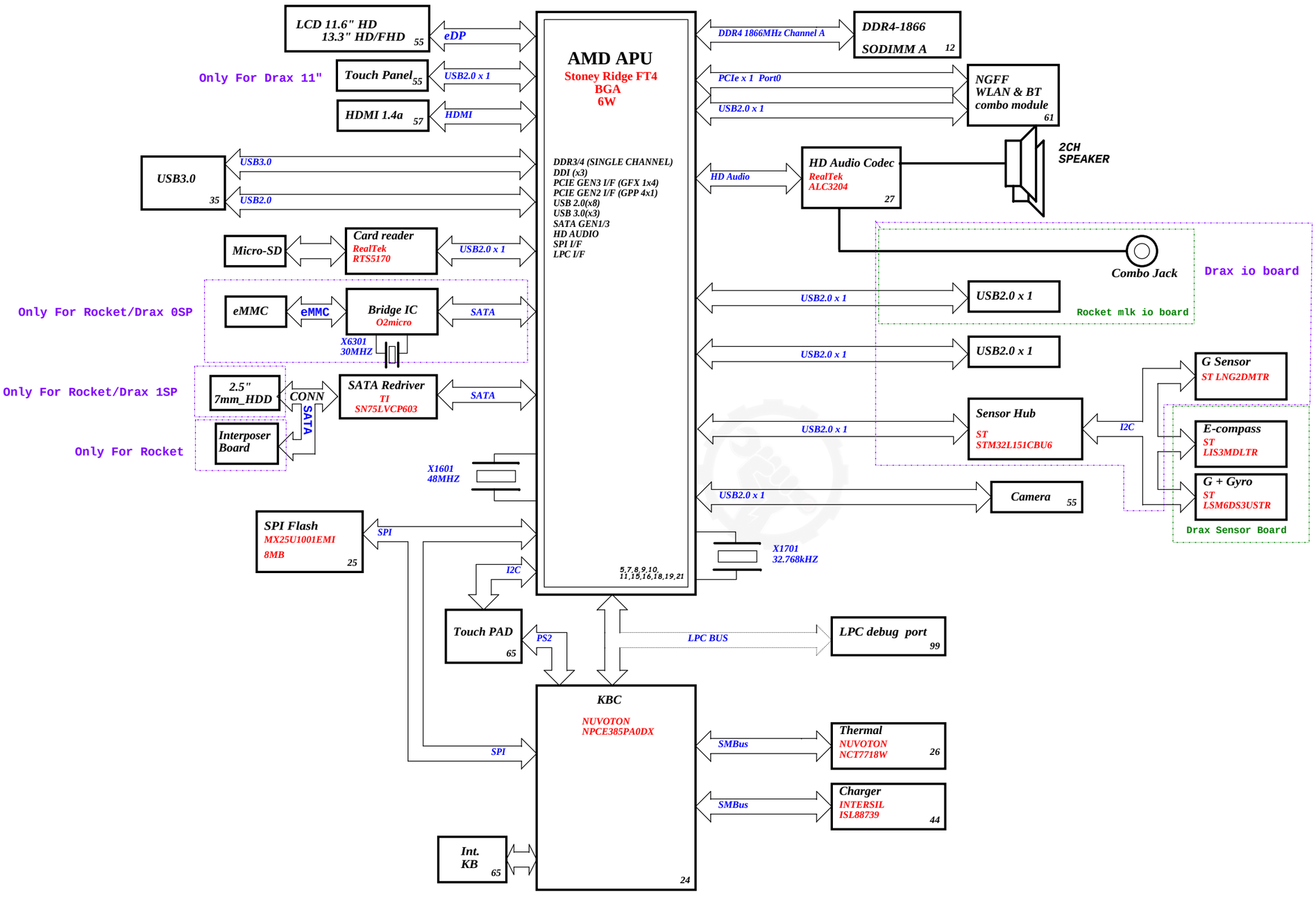
Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***		
Size: A3	Document Number: ***Drax MLK/Rocket MLK AMD***	Rev: ***A00***
Date: Tuesday, January 02, 2018	Sheet 1 of 109	

Project code : 4PD0DW010001-->Drax MLK_17877
4PD0E2010001-->Rocket MLK_17876
PCB P/N : 17837
Revision : -1

Drax MLK/Rocket MLK_AMD Stoney Ridge Block Diagram



CHARGER ISL88739HRZ-T 44	
INPUTS	OUTPUTS
AD+ 12V_BT+	DCBATOUT

SYSTEM DC/DC RT6575DGQW 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5 5V_AUX_S5

CPU Core Power ISL62771HRTZ 46-47	
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE 1D2V_CPU_VDDNB

DDR4 SUS G5388K11U 53	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3

CPU VDDP G5388K11U 52	
INPUTS	OUTPUTS
DCBATOUT	0D95V_S5

CPU VDD18 RT5797ALGQW RT9078-18GJ5 54	
INPUTS	OUTPUTS
3D3V_S5 3D3V_AUX_S5	1D8V_S5 1D8V_AUX_S5

CPU VDDCRGFX APL5337KAI 49	
INPUTS	OUTPUTS
1D8V_S5	0D775V_S5

Switches 40	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0
0D95V_S5	0D95V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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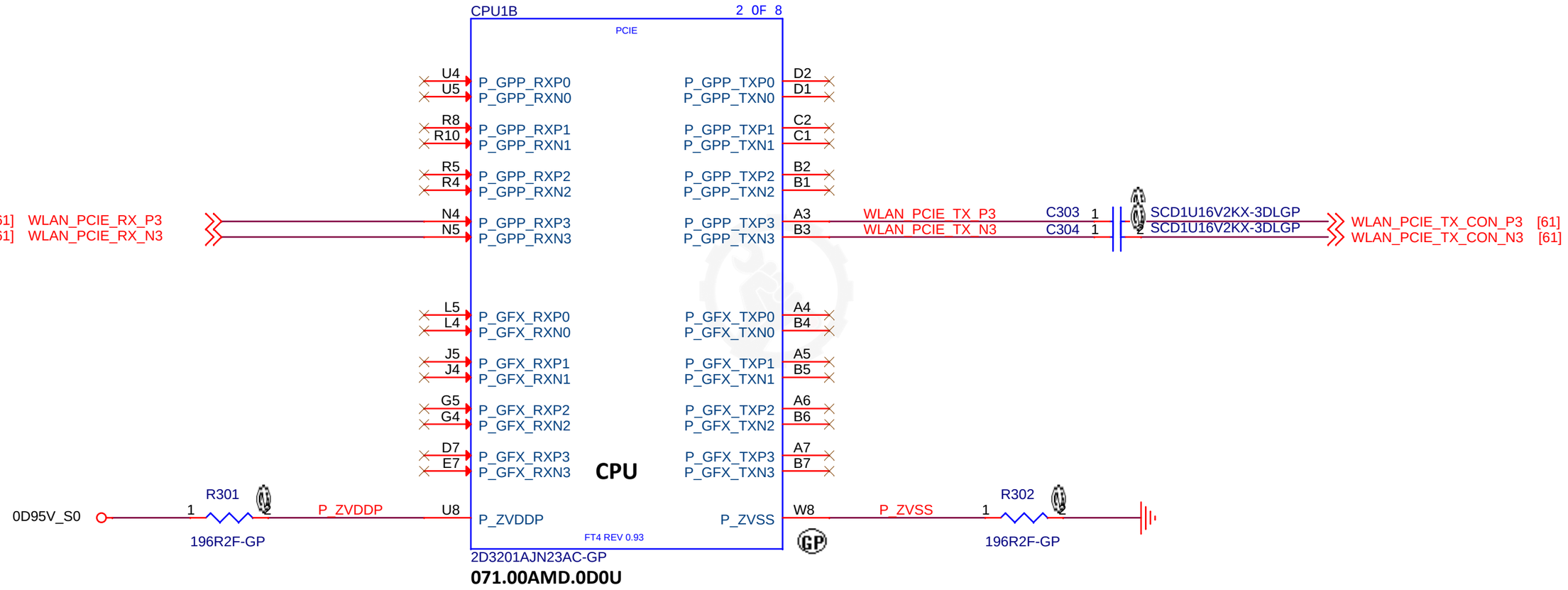
Title: Block Diagram

Size	Document Number	Rev
A2	Drax MLK/Rocket MLK AMD	A00

Date: Tuesday, January 02, 2018 Sheet 2 of 109

SSID = CPU

GPP CLK port	Device	CLKREQ#
3	WLAN	3



Drax Rocket MLK

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Title: ***CPU (PCIE)***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 3 of 106

SSID = CPU

(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 4 of 106

SSID = CPU

1D2V_S3

1 R504 1KR2J-1-GP M_A_EVENT#_APU

AMD Confirm: PU Needed even if not used

DDR4_A_DRAMRST#

1

20170818
ED501
Do Not Stuff

DY

2

CPU1A 1 0F 8

MEMORY

[12] M_A_A0	AG38	M_ADD0	M_DATA0	A34	M_A_DQ0 [12]
[12] M_A_A1	W35	M_ADD1	M_DATA1	B34	M_A_DQ1 [12]
[12] M_A_A2	W38	M_ADD2	M_DATA2	A38	M_A_DQ2 [12]
[12] M_A_A3	W34	M_ADD3	M_DATA3	B38	M_A_DQ3 [12]
[12] M_A_A4	U38	M_ADD4	M_DATA4	A33	M_A_DQ4 [12]
[12] M_A_A5	U37	M_ADD5	M_DATA5	B33	M_A_DQ5 [12]
[12] M_A_A6	U34	M_ADD6	M_DATA6	A37	M_A_DQ6 [12]
[12] M_A_A7	R35	M_ADD7	M_DATA7	B37	M_A_DQ7 [12]
[12] M_A_A8	R38	M_ADD8		B41	
[12] M_A_A9	N38	M_ADD9	M_DATA8	C40	M_A_DQ8 [12]
[12] M_A_A10	AG34	M_ADD10	M_DATA9	F41	M_A_DQ9 [12]
[12] M_A_A11	R34	M_ADD11	M_DATA10	G40	M_A_DQ10 [12]
[12] M_A_A12	N37	M_ADD12	M_DATA11	A40	M_A_DQ11 [12]
[12] M_A_A13	AN35	M_ADD13	M_DATA12	B40	M_A_DQ12 [12]
[12] M_A_BG1	L38	M_ADD14/M_BG1	M_DATA13	E41	M_A_DQ13 [12]
[12] M_A_ACT#	L35	M_ADD15/M_ACT_L	M_DATA14	F40	M_A_DQ14 [12]
			M_DATA15		M_A_DQ15 [12]
[12] M_A_BA0	AJ38	M_BANK0		J40	
[12] M_A_BA1	AG35	M_BANK1	M_DATA16	J41	M_A_DQ16 [12]
[12] M_A_BG0	N34	M_BANK2/M_BG0	M_DATA17	N40	M_A_DQ17 [12]
			M_DATA18	N41	M_A_DQ18 [12]
[12] M_A_DM0	B35	M_DM0	M_DATA19	H40	M_A_DQ19 [12]
[12] M_A_DM1	D40	M_DM1	M_DATA20	H41	M_A_DQ20 [12]
[12] M_A_DM2	K40	M_DM2	M_DATA21	M40	M_A_DQ21 [12]
[12] M_A_DM3	T41	M_DM3	M_DATA22	M41	M_A_DQ22 [12]
[12] M_A_DM4	AE41	M_DM4	M_DATA23		M_A_DQ23 [12]
[12] M_A_DM5	AL40	M_DM5		R40	
[12] M_A_DM6	AU40	M_DM6	M_DATA24	T40	M_A_DQ24 [12]
[12] M_A_DM7	BA37	M_DM7	M_DATA25	W40	M_A_DQ25 [12]
			M_DATA26	Y40	M_A_DQ26 [12]
[12] M_A_DQS_DP0	B36	M_DQS_H0	M_DATA27	P40	M_A_DQ27 [12]
[12] M_A_DQS_DN0	A36	M_DQS_L0	M_DATA28	P41	M_A_DQ28 [12]
[12] M_A_DQS_DP1	E40	M_DQS_H1	M_DATA29	V40	M_A_DQ29 [12]
[12] M_A_DQS_DN1	D41	M_DQS_L1	M_DATA30	V41	M_A_DQ30 [12]
[12] M_A_DQS_DP2	L40	M_DQS_H2	M_DATA31		M_A_DQ31 [12]
[12] M_A_DQS_DN2	K41	M_DQS_L2		AD41	
[12] M_A_DQS_DP3	U41	M_DQS_H3	M_DATA32	AD40	M_A_DQ32 [12]
[12] M_A_DQS_DN3	U40	M_DQS_L3	M_DATA33	AH41	M_A_DQ33 [12]
[12] M_A_DQS_DP4	AF41	M_DQS_H4	M_DATA34	AH40	M_A_DQ34 [12]
[12] M_A_DQS_DN4	AE40	M_DQS_L4	M_DATA35	AB40	M_A_DQ35 [12]
[12] M_A_DQS_DP5	AM40	M_DQS_H5	M_DATA36	AC40	M_A_DQ36 [12]
[12] M_A_DQS_DN5	AM41	M_DQS_L5	M_DATA37	AF40	M_A_DQ37 [12]
[12] M_A_DQS_DP6	AV40	M_DQS_H6	M_DATA38	AG40	M_A_DQ38 [12]
[12] M_A_DQS_DN6	AV41	M_DQS_L6	M_DATA39		M_A_DQ39 [12]
[12] M_A_DQS_DP7	BA36	M_DQS_H7		AK41	
[12] M_A_DQS_DN7	AY36	M_DQS_L7	M_DATA40	AK40	M_A_DQ40 [12]
			M_DATA41	AP41	M_A_DQ41 [12]
[12] M_A_CLK0	AC35	M_CLK_H0	M_DATA42	AP40	M_A_DQ42 [12]
[12] M_A_CLK#0	AC34	M_CLK_L0	M_DATA43	AJ41	M_A_DQ43 [12]
[12] M_A_CLK1	AA34	M_CLK_H1	M_DATA44	AJ40	M_A_DQ44 [12]
[12] M_A_CLK#1	AA32	M_CLK_L1	M_DATA45	AN41	M_A_DQ45 [12]
	AE38	M_CLK_H2	M_DATA46	AN40	M_A_DQ46 [12]
	AE37	M_CLK_L2	M_DATA47		M_A_DQ47 [12]
	AA37	M_CLK_H3		AT40	
	AA38	M_CLK_L3	M_DATA48	AU41	M_A_DQ48 [12]
	G38	M_RESET_L	M_DATA49	AY40	M_A_DQ49 [12]
[12] DDR4_A_DRAMRST#	1 2M_A_EVENT#_APU AA41	M_EVENT_L	M_DATA50	BA40	M_A_DQ50 [12]
[12] M_A_EVENT#	R501 Do Not Stuff 20171003		M_DATA51	AR40	M_A_DQ51 [12]
	J38	M0_CKE0	M_DATA52	AT41	M_A_DQ52 [12]
[12] M_A_CKE0	J34	M0_CKE1	M_DATA53	AW40	M_A_DQ53 [12]
[12] M_A_CKE1	L34	M1_CKE0	M_DATA54	AY41	M_A_DQ54 [12]
	J37	M1_CKE1	M_DATA55		M_A_DQ55 [12]
	AN37	M0_ODT0		BA38	
[12] M_A_ODT0	AU38	M0_ODT1	M_DATA56	AY37	M_A_DQ56 [12]
[12] M_A_ODT1	AL34	M1_ODT0	M_DATA57	BA34	M_A_DQ57 [12]
	AN34	M1_ODT1	M_DATA58	BA33	M_A_DQ58 [12]
	AL35	M0_CS_L0	M_DATA59	AY39	M_A_DQ59 [12]
[12] M_A_CS#0	AR37	M0_CS_L1	M_DATA60	AY38	M_A_DQ60 [12]
[12] M_A_CS#1	AJ34	M1_CS_L0	M_DATA61	AY35	M_A_DQ61 [12]
	AR38	M1_CS_L1	M_DATA62	AY34	M_A_DQ62 [12]
	AJ37	M_RAS_L/M_RAS_L_ADD16	M_DATA63		M_A_DQ63 [12]
[12] M_A_RAS#	AN38	M_CAS_L/M_CAS_L_ADD15			
[12] M_A_CAS#	AL38	M_WE_L/M_WE_L_ADD14			
[12] M_A_WE#					
TP502 1 DDR_VREF_S3	AA40	M_VREF			
TP501 1 M_VREFDQ	Y41	M_VREFDQ	M_ZVDDIO_MEM_S3	AB41	M_ZVDDIO

FT4 REV 0.93

2D3201AJN23AC-GP

071.00AMD.0D0U

CPU

R503 1 1D2V_S3

39D2R2F-L-GP

Drax Rocket MLK

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Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 5 of 106

SSID = CPU

(Blanking)

Drax Rocket MLK

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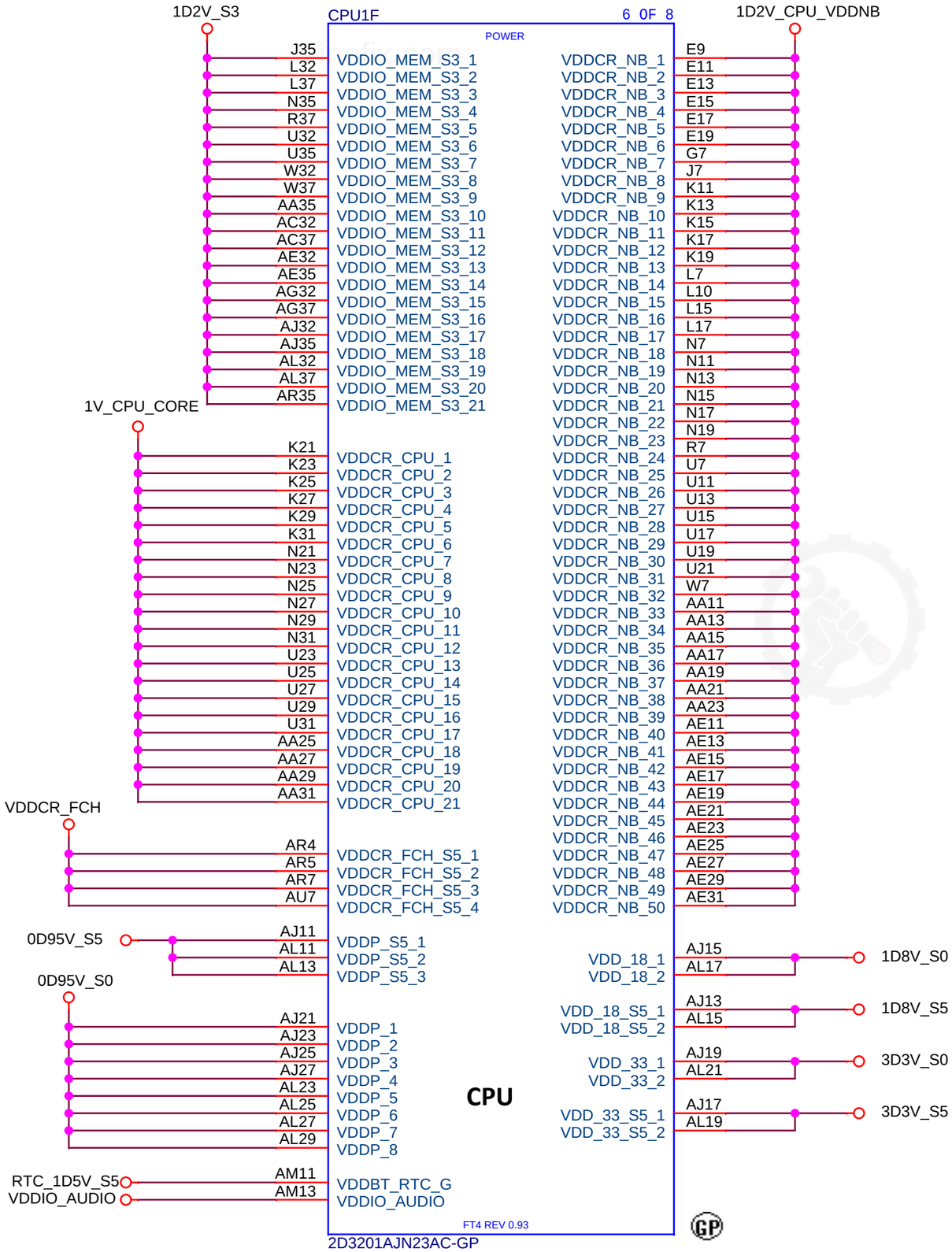
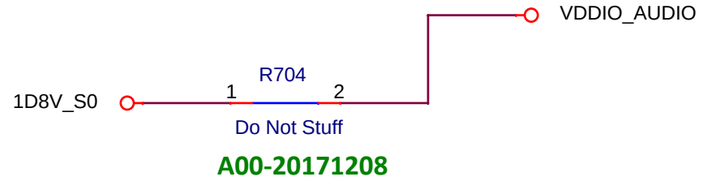
Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 6 of 106

SSID = CPU





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Title: ***CPU(VCC_CORE)***

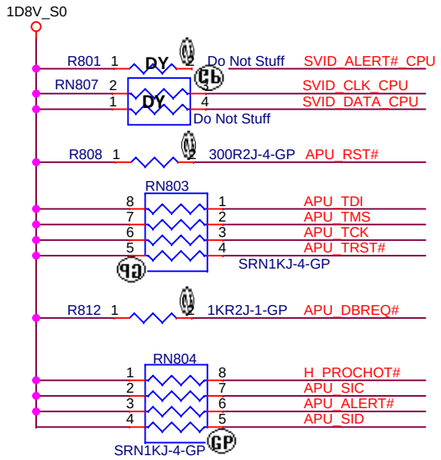
Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

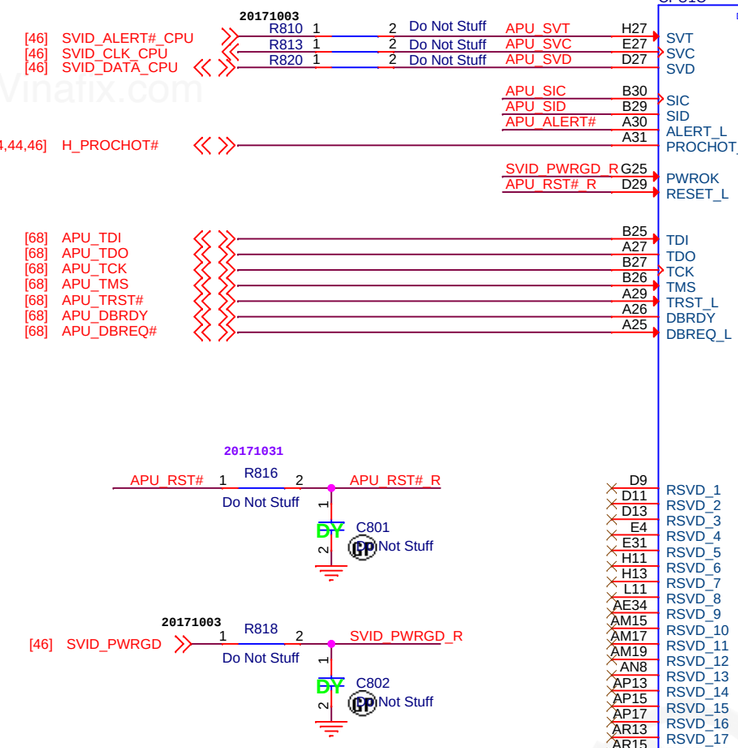
Date: Tuesday, January 02, 2018 Sheet 7 of 106

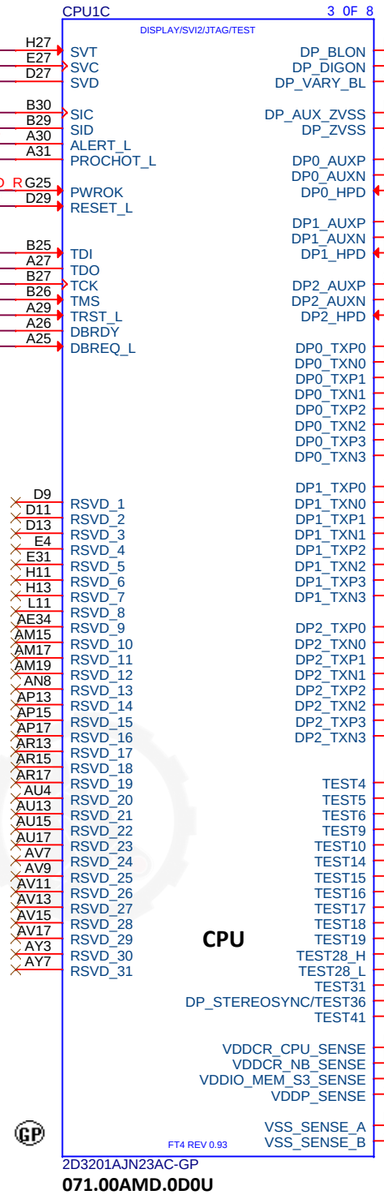
SSID = CPU

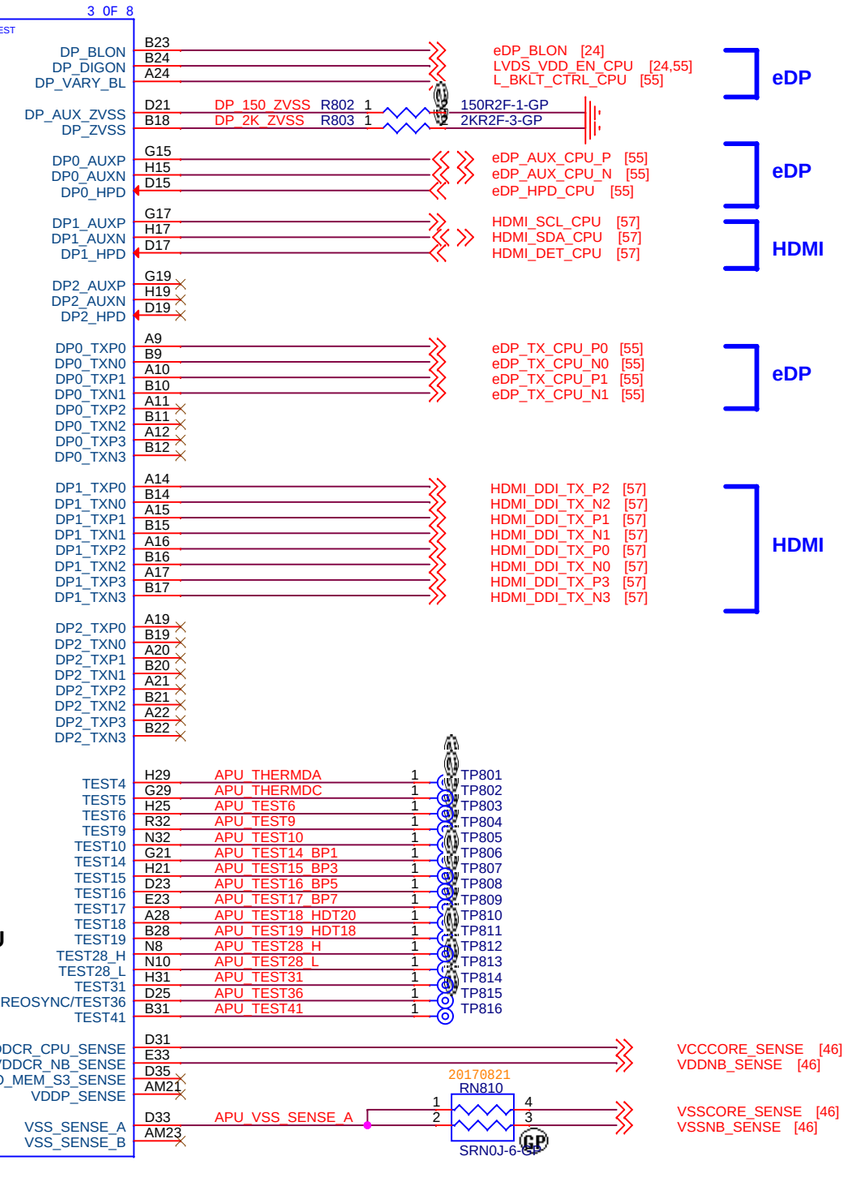
Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8

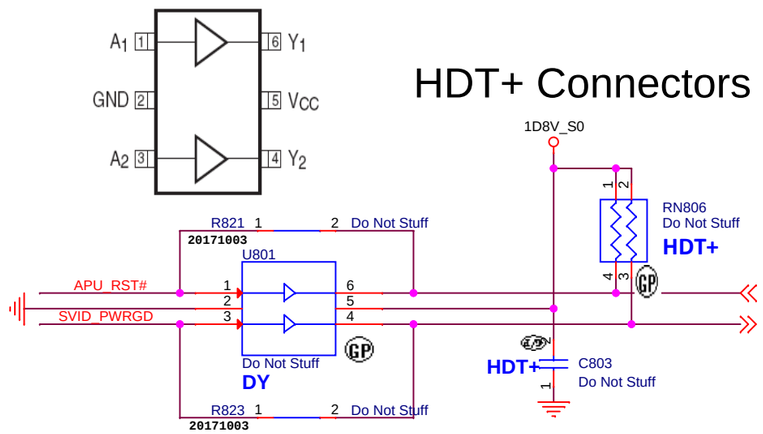








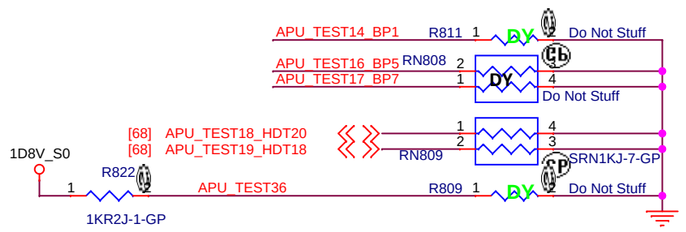
HDT+ Connectors



APU core Control

APU_RST_L_BUF [68]

APU_PWROK_HDT [68]



Drax Rocket MLK

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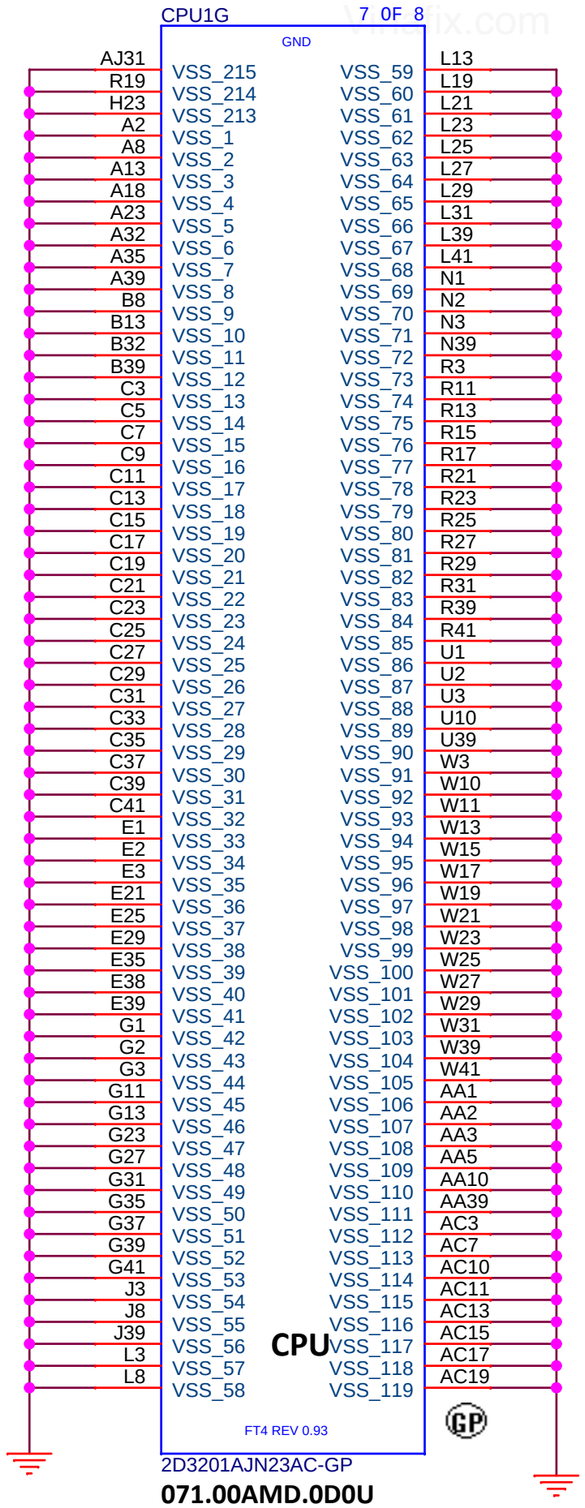
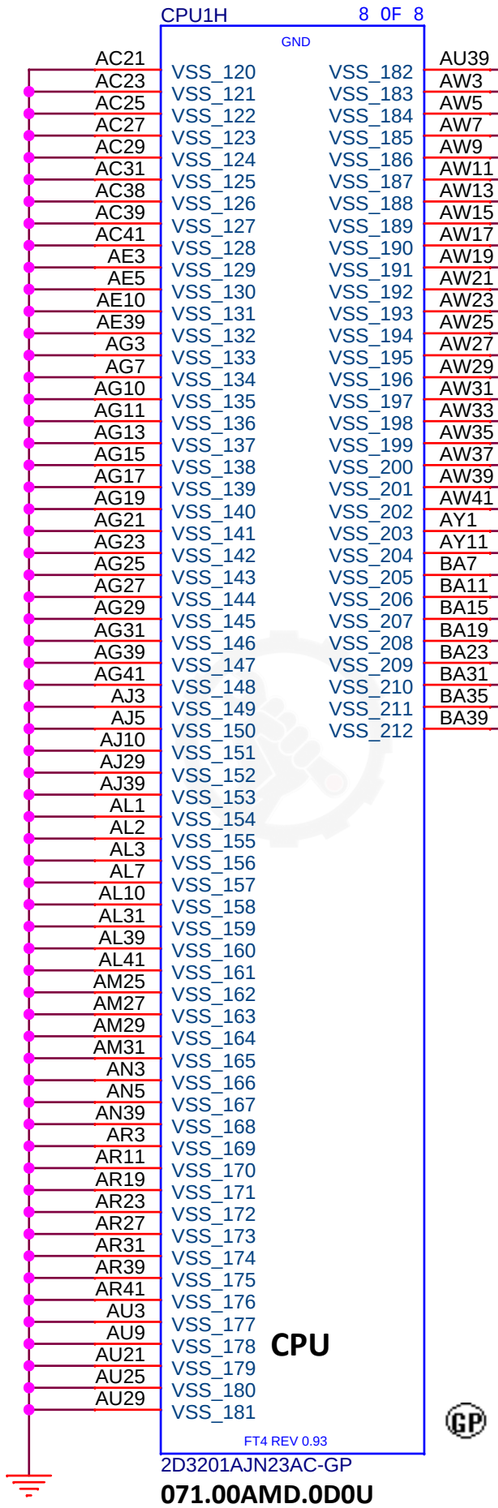
Title	CPU (DISPLAY/SVI2/JTAG/TES)	
Size A3	Document Number: Drax MLK/Rocket MLK AMD	Rev A00
Date: Tuesday, January 02, 2018	Sheet 8 of 106	

SSID = CPU





Drax Rocket MLK

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Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 9 of 106

SSID = CPU

1V_CPU_CORE

20171002

C1001 SC22U6D3V3MX-1-DL-GP
C1002 SC22U6D3V3MX-1-DL-GP
C1003 SC22U6D3V3MX-1-DL-GP
C1004 SC22U6D3V3MX-1-DL-GP
C1005 SC22U6D3V3MX-1-DL-GP
C1006 SC22U6D3V3MX-1-DL-GP
C1007 SC22U6D3V3MX-1-DL-GP
C1008 DY Do Not Stuff
C1009 SC180P50V2JN-1DLGP
C1075 SC1U10V2KX-1DLGP

1D2V_CPU_VDDNB

C1010 SC22U6D3V3MX-1-DL-GP
C1011 SC22U6D3V3MX-1-DL-GP
C1012 DY Do Not Stuff
C1013 SC22U6D3V3MX-1-DL-GP
C1014 DY Do Not Stuff
C1015 SC22U6D3V3MX-1-DL-GP
C1016 DY Do Not Stuff
C1017 SC22U6D3V3MX-1-DL-GP
C1018 SC22U6D3V3MX-1-DL-GP
C1019 DY Do Not Stuff
C1020 DY Do Not Stuff
C1021 SC180P50V2JN-1DLGP
C1076 SC1U10V2KX-1DLGP

1D2V_S3

C1022 SC22U6D3V3MX-1-DL-GP
C1023 DY Do Not Stuff
C1024 SC22U6D3V3MX-1-DL-GP
C1025 SC22U6D3V3MX-1-DL-GP
C1026 SC22U6D3V3MX-1-DL-GP
C1027 SC22U6D3V3MX-1-DL-GP
C1028 DY Do Not Stuff
C1029 DY Do Not Stuff
C1030 DY Do Not Stuff
C1031 SC1U10V2KX-1DLGP
C1032 DY Do Not Stuff
C1077 DY Do Not Stuff
C1033 SC180P50V2JN-1DLGP

1D8V_S5

C1052 SC10U6D3V3MX-DL-GP
C1053 SC1U10V2KX-1DLGP
C1054 SC1KP50V2KX-1DLGP

1D8V_S0

C1055 SC10U6D3V3MX-DL-GP
C1056 SC1U10V2KX-1DLGP
C1057 SC1KP50V2KX-1DLGP

VDDCR_FCH

C1043 DY Do Not Stuff
C1044 DY Do Not Stuff
C1045 SC1U10V2KX-1DLGP
C1078 SC10U6D3V3MX-DL-GP
C1079 DY Do Not Stuff
C1080 SC1KP50V2KX-1DLGP

0D95V_S5

C1048 DY Do Not Stuff
C1049 SC1U10V2KX-1DLGP
C1050 SC1KP50V2KX-1DLGP

0D95V_S0

C1034 DY Do Not Stuff
C1035 SC22U6D3V3MX-1-DL-GP
C1040 SC22U6D3V3MX-1-DL-GP
C1041 DY Do Not Stuff
C1051 SC22U6D3V3MX-1-DL-GP
C1037 SC10U6D3V3MX-DL-GP
C1047 DY Do Not Stuff
C1036 DY Do Not Stuff
C1046 SC1KP50V2KX-1DLGP
C1038 DY Do Not Stuff
C1039 SC1KP50V2KX-1DLGP
C1042 SC180P50V2JN-1DLGP

3D3V_S5

C1002 FC SC18P50V2JN-1DLGP
C1001 FC SC18P50V2JN-1DLGP
C1058 DY Do Not Stuff
C1059 SC1U10V2KX-1DLGP
C1060 SC1KP50V2KX-1DLGP

RF request
20171103

3D3V_S0

C1003 FC SC18P50V2JN-1DLGP
C1061 SC10U6D3V3MX-DL-GP
C1062 SC1U10V2KX-1DLGP
C1063 SC1KP50V2KX-1DLGP

RF request
20171103

VDDIO_AUDIO

C1064 DY Do Not Stuff
C1065 SC1U10V2KX-1DLGP
C1081 SC1KP50V2KX-1DLGP

RTC_1D5V_S5

C1066 SCD22U10V2KX-2-GP

1V_CPU_CORE

C1067 SC22U6D3V3MX-1-DL-GP
C1068 SC22U6D3V3MX-1-DL-GP
C1069 DY Do Not Stuff
C1070 SC22U6D3V3MX-1-DL-GP

1D2V_CPU_VDDNB

C1071 SC22U6D3V3MX-1-DL-GP
C1072 DY Do Not Stuff
C1073 SC22U6D3V3MX-1-DL-GP
C1074 DY Do Not Stuff

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP1)

Size: Custom | Document Number: Drax MLK/Rocket MLK AMD | Rev: A00

Date: Tuesday, January 02, 2018 | Sheet 10 of 106

SSID = CPU

(Blanking)

Drax Rocket MLK

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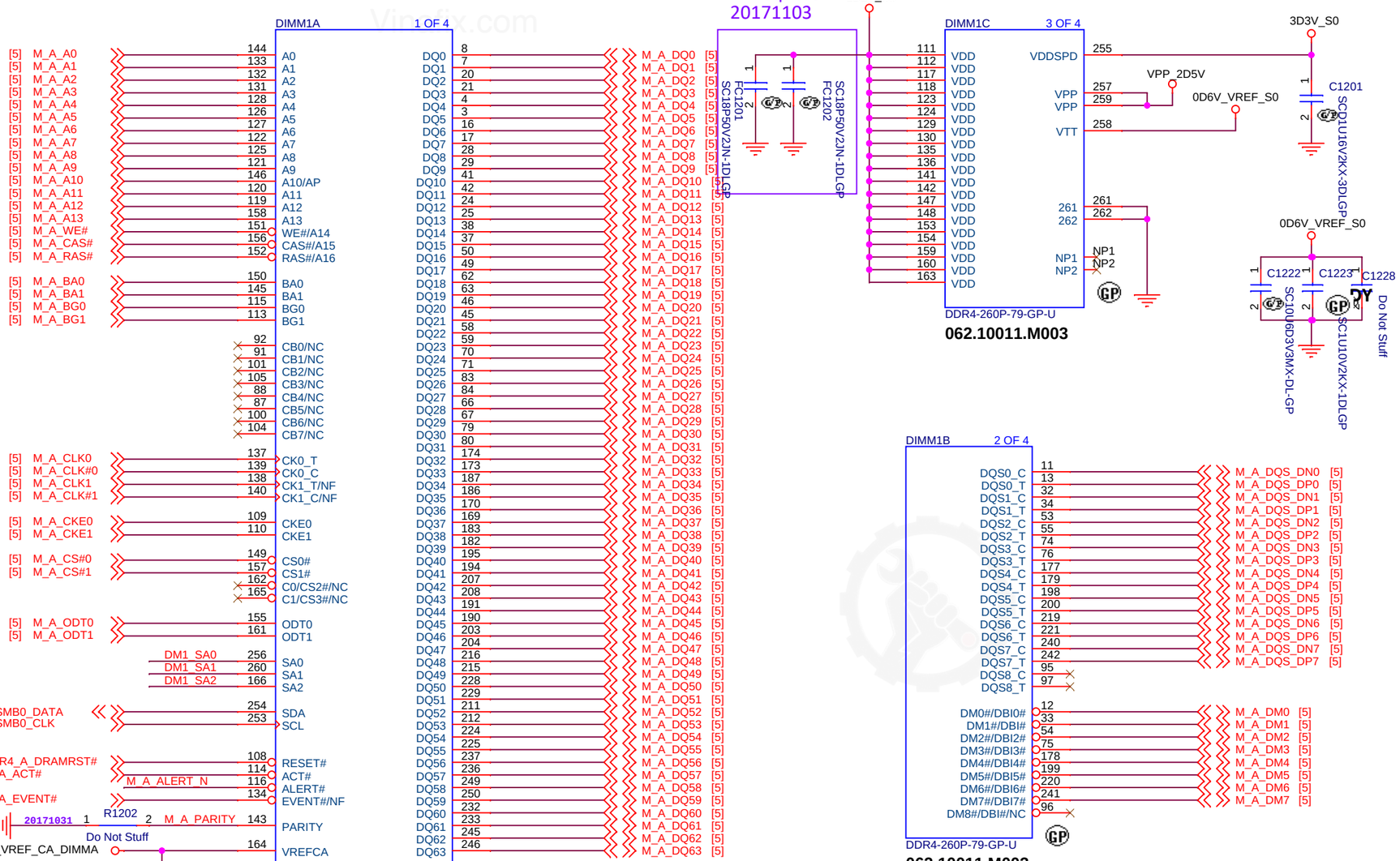
Taipei Hsien 221, Taiwan, R.O.C.

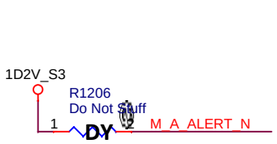
Title: *(Reserved)*

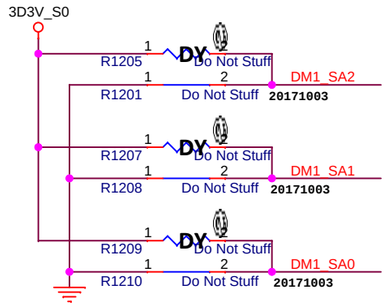
Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 11 of 106

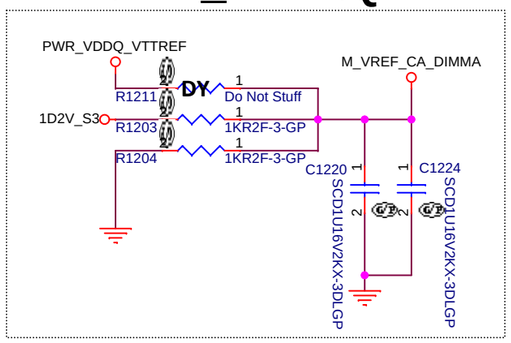
SSID = DDR4-SODIMM1

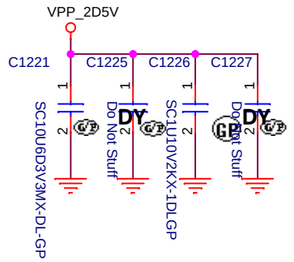






DIMM_VREFDQ

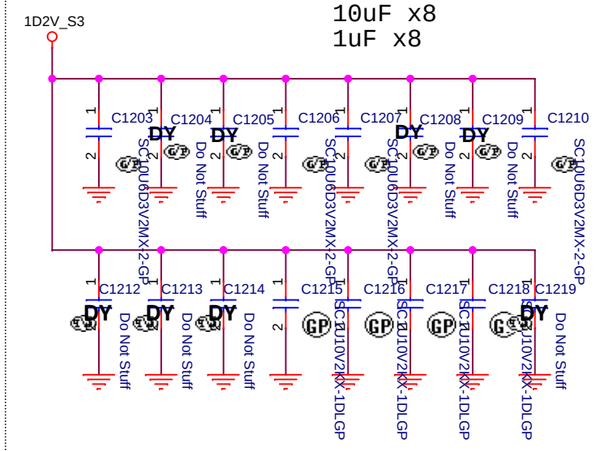




SPD Address of DIMMA

SPD SA2	0
SPD SA1	0
SPD SA0	0

Layout Note :
Place these Caps near DIM1



Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR4-SODIMM1*

Size	Document Number	Rev
A3	Drax MLK/Rocket MLK AMD	A00

Date: Tuesday, January 02, 2018 Sheet 12 of 106

SSID = DDR4-SODIMM2

Drax Rocket MLK

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***DDR4-SODIMM2***		
Size: A3	Document Number: **Drax MLK/Rocket MLK AMD**	Rev: **A00**
Date: Tuesday, January 02, 2018	Sheet 13 of 106	

SSID = CPU

(Blanking)

Drax Rocket MLK

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 14 of 106

SSID = CPU

(Blanking)

Drax Rocket MLK

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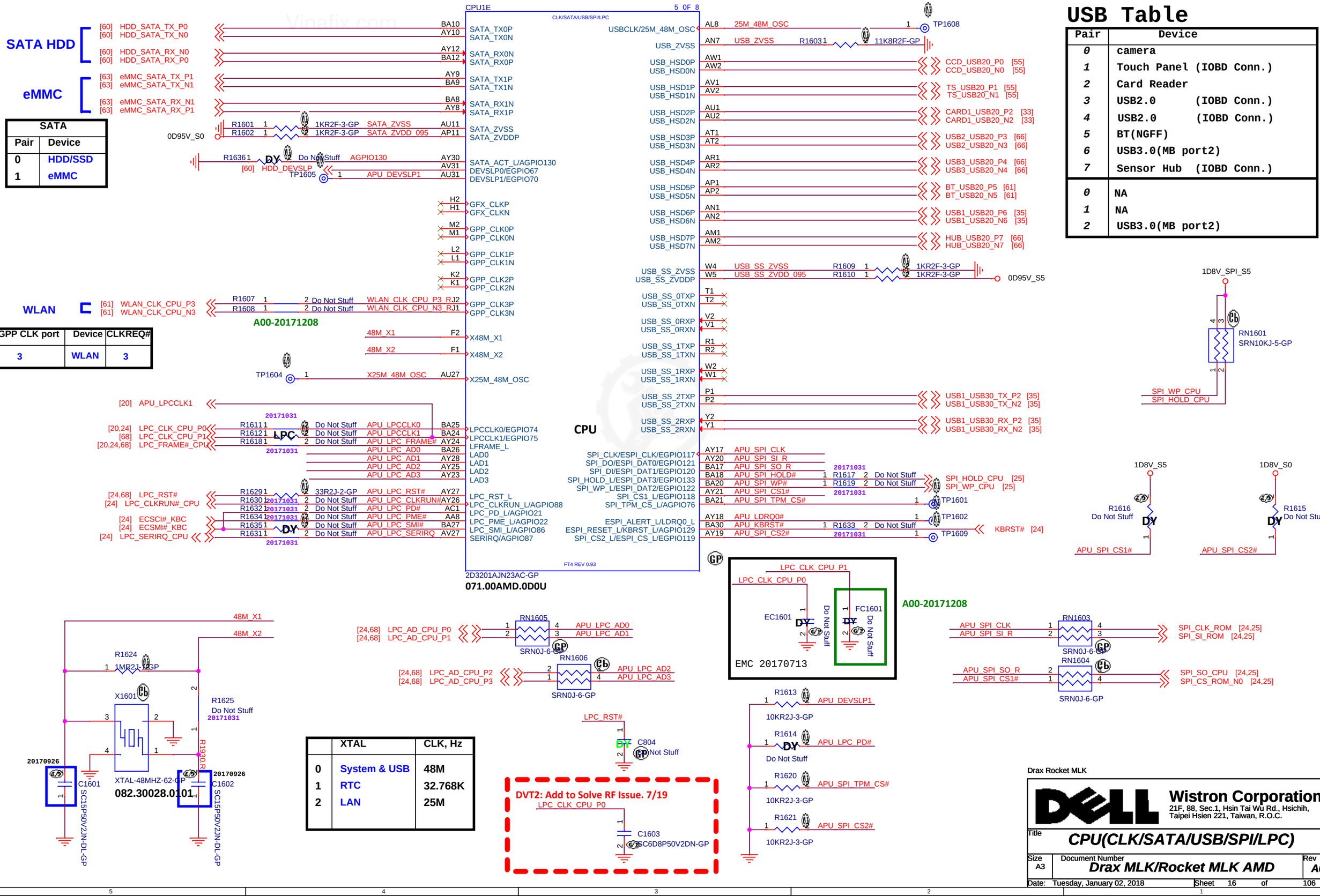
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 15 of 106

SSID = CPU



Drax Rocket MLK

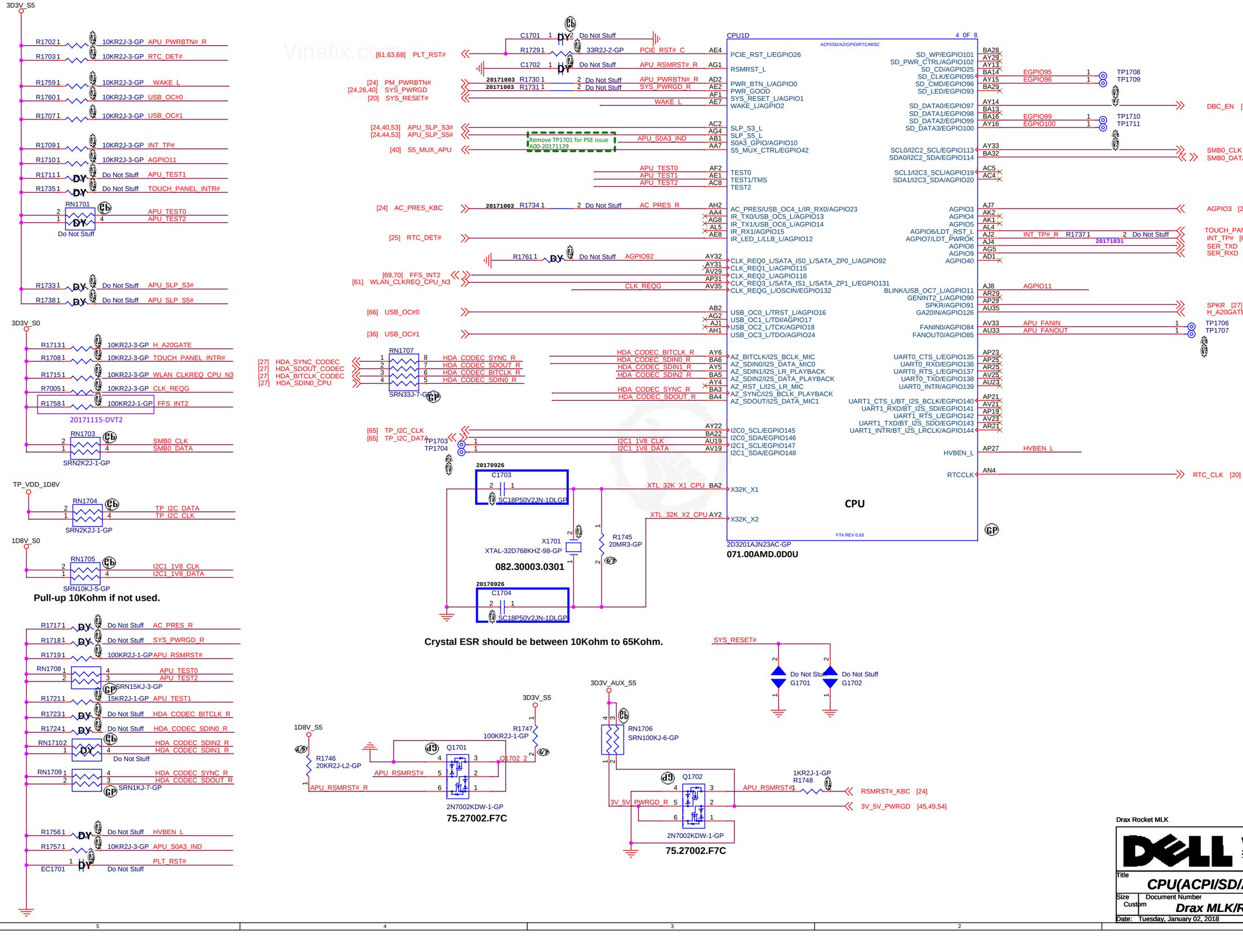
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(CLK/SATA/USB/SPI/LPC)

Size: A3 | Document Number: Drax MLK/Rocket MLK AMD | Rev: A00

Date: Tuesday, January 02, 2018 | Sheet 16 of 106

SSID = CPU



Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU(ACPI/SD/AZ/GPIO/RTC)	
Size: Custom	Document Number: Drax MLK/Rocket MLK AMD	Rev: A00
Date: Tuesday, January 02, 2018	Sheet 17 of 106	

SSID = CPU

(Blanking)

Drax Rocket MLK

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 18 of 106

SSID = CPU

(Blanking)

Drax Rocket MLK

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Taipei Hsien 221, Taiwan, R.O.C.

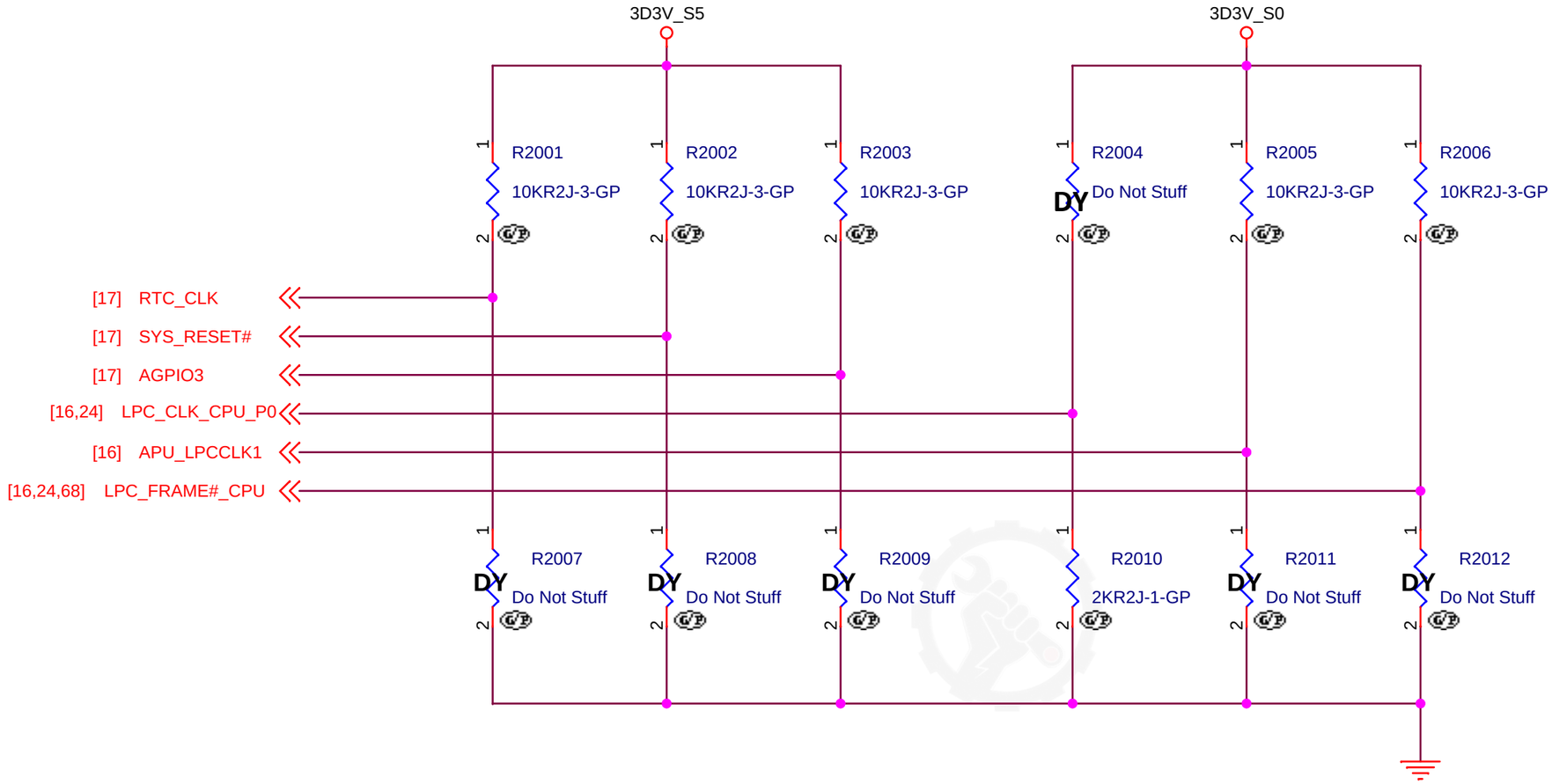
Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 19 of 106

SSID = STRAPING

SYSTEM STRAPPINGS



REQUIRED SYSTEM STRAPS

	RTC_CLK	SYS_RESET#	AGPIO3	LPC_CLK0	LPC_CLK1	LPC_FRAME#
Type	I	I	I	II	II	II
PULL HIGH	RTC Coin Battery is implemented DEFAULT	NORMAL POWR UP /RESET TIMING DEFAULT	Enhanced Reset logic DEFAULT	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT
PULL LOW	RTC Coin Battery is not implemented	Reserved	Traditional Reset logic	Boot Fail Timer Disabled DEFAULT	Reserved	LPC ROM

Drax Rocket MLK

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU Strappings*

Size: A4 | Document Number: *Drax MLK/Rocket MLK AMD* | Rev: *A00*

Date: Tuesday, January 02, 2018 | Sheet 20 of 106

SSID = CPU

(Blanking)

Drax Rocket MLK

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 21 of 106

SSID = CPU

(Blanking)

Drax Rocket MLK

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 22 of 106

SSID = CPU

(Blanking)

Drax Rocket MLK

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 23 of 106

SSID = KBC

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.524 V	< 1.126 V

Do Not Stuff

LPC strap pin

Battery/ Charger
APU
Thermal

KBC_RESET

High Active

Start up

Modle ID

	Rocket	Drax
ID	0	1

Drax Rocket MLK

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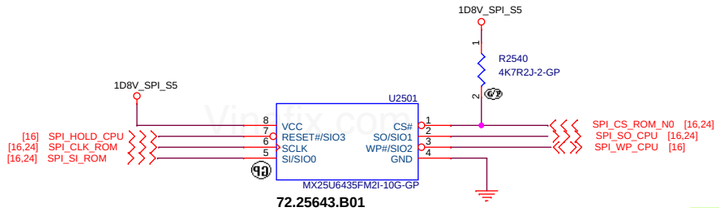
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_Nuvoton_NPCE385
Size: A1 | Document Number: Drax MLK/Rocket MLK AMD | Rev: A00
Date: Tuesday, January 02, 2018 | Sheet 24 of 109

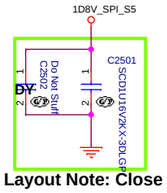
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for CPU

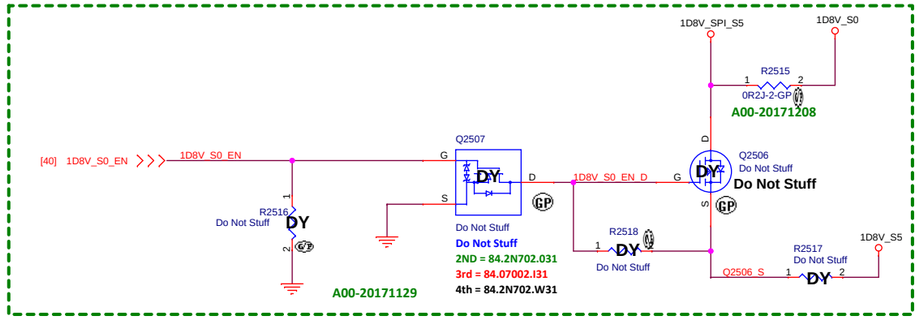


SPI ROM socket
Co-Layout with U2501

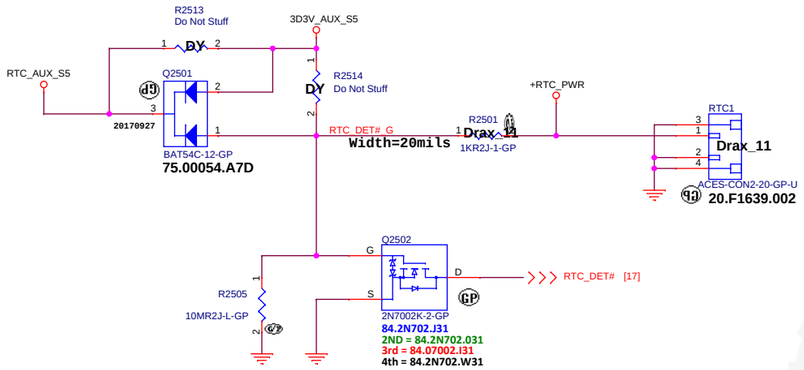
Remove SSKT1 co-lay
A00-20171129



Layout Note: Close to U2501 Pin 8

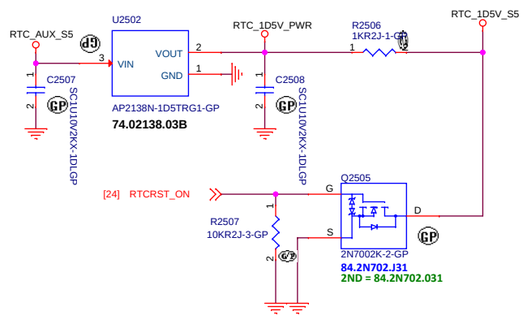


SSID = RTC



20170925

Delete RTC2 Conn



Drax Rocket MLK

Wistron Corporation
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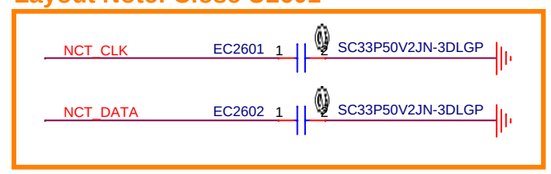
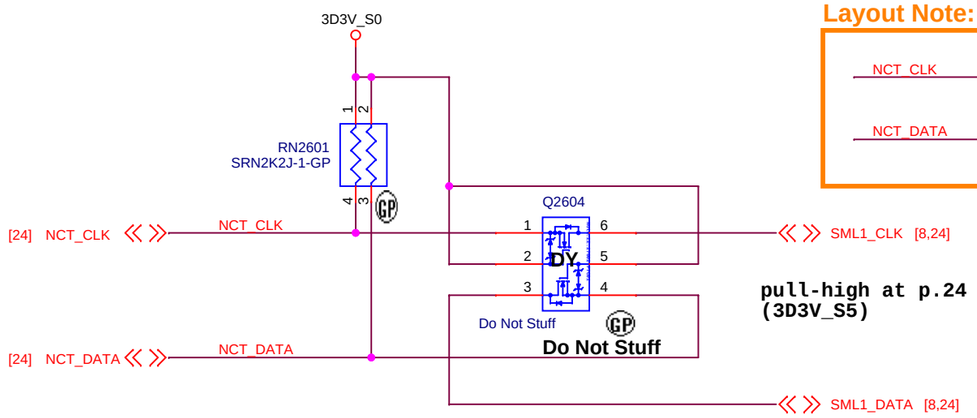
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC		
Size: A2	Document Number: Drax MLK/Rocket MLK AMD	Rev: A00
Date: Tuesday, January 02, 2018	Sheet 25 of 109	

SSID = Thermal

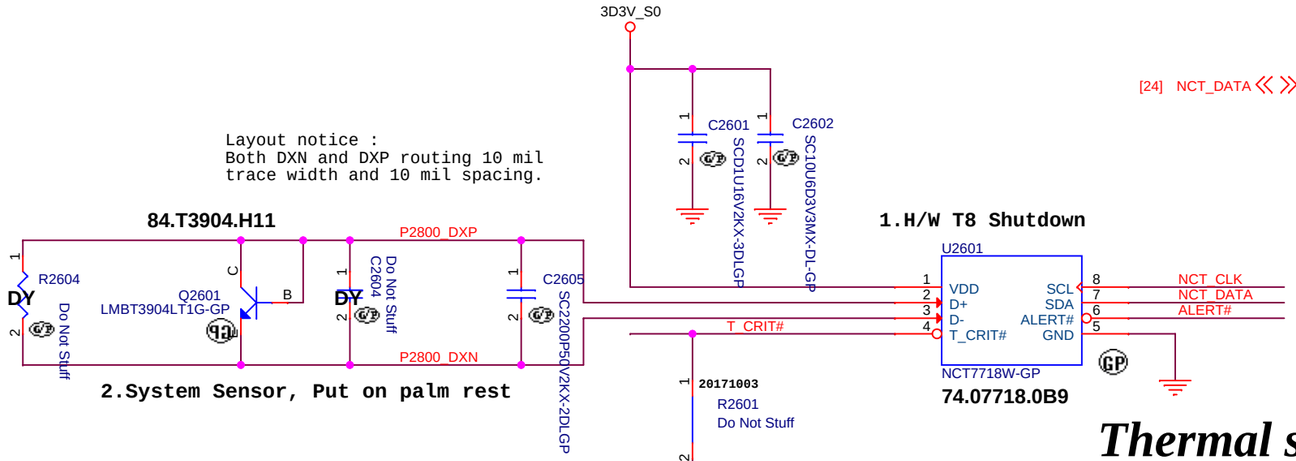
EE Note:
1. T8: PURE_HW_SHUTDOWN# through Q2603.
2. THM_SENSOR: Thermal sensor NCT7718W solution.



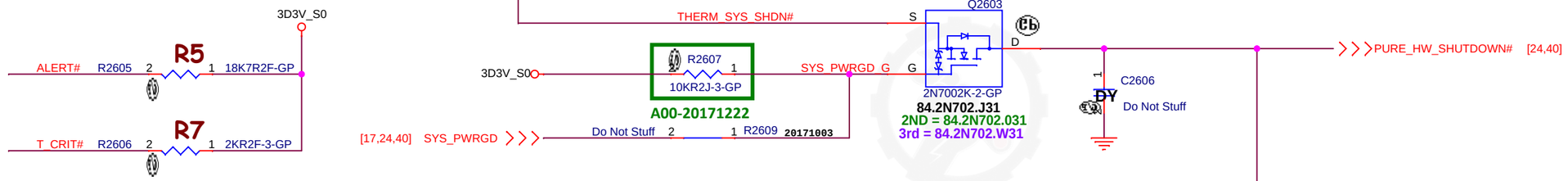


pull-high at p.24
(3D3V_S5)

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



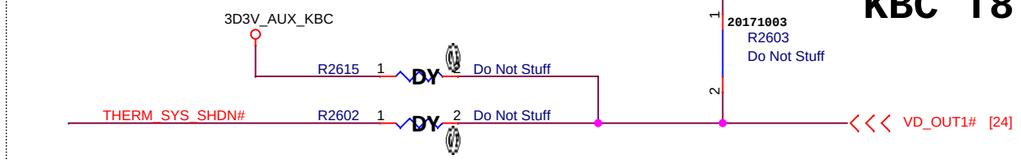
Thermal sensor NCT 7718W



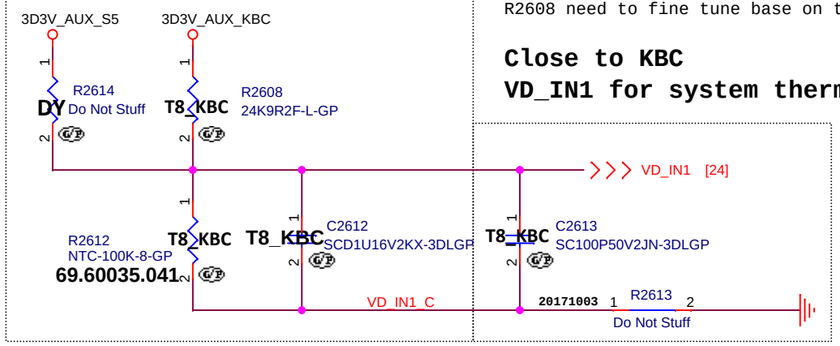
The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8



Close to Thermal sensor



EE Note:
R2608 need to fine tune base on thermal test.

Close to KBC
VD_IN1 for system thermal sensor

20170925

Delete FAN1 Conn

Drax Rocket MLK

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal*

Size: A3 | Document Number: *Drax MLK/Rocket MLK AMD* | Rev: *A00*

Date: Tuesday, January 02, 2018 | Sheet 26 of 109

Main Func = Audio

Audio Codec Chip ALC3204

Analog
Digital

1.8V power rail should be supplied by linear regulator, not awitching regulator.if switch regulator is unavilable, please make sure that switch frequency operates at out-band(over 20KHz)

>2A

Add this filter to avoid other components/chips to be influenced

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

ALC3204
QFN40 (5X5)

HDA27
ALC3204-CG-GR-U

Analog
Digital
moat

place close to pin8

place close to pin1

Close pin3

Layout Note:
Place close to Pin 20

Layout Note:
Tied at point only under Codec or near the Codec

DVDD must >= DVDD_IO

Azalia I/F EMI

Open drain output. pull up to DVDD or max. 5V

Drax Rocket MLK

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Title: Audio Codec ALC3204
Size: A2 | Document Number: Drax MLK/Rocket MLK AMD | Rev: A00
Date: Tuesday, January 02, 2018 | Sheet 27 of 105

Blanking

Drax Rocket MLK

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 28 of 109

SSID = AUDIO

Speaker

[27] AUD_SPK_11_R+
[27] AUD_SPK_11_R-
[27] AUD_SPK_11_L+
[27] AUD_SPK_11_L-

R29041 Drax_11 HCB1608KF121T30-GP AUD_SPK_R+_C11 1
R29031 Drax_11 HCB1608KF121T30-GP AUD_SPK_R-_C11 2
R29021 Drax_11 HCB1608KF121T30-GP AUD_SPK_L+_C11 3
R29011 Drax_11 HCB1608KF121T30-GP AUD_SPK_L-_C11 4
Bead 120ohm

SPK1
5
Drax_11
6
ACES-CON4-29-GP
20.F1639.004
2nd = 20.F1804.004

EC2901 SC1KP50V2KX-1DLGP
EC2902 SC1KP50V2KX-1DLGP
EC2903 SC1KP50V2KX-1DLGP
EC2904 SC1KP50V2KX-1DLGP
Drax_11 Drax_11 Drax_11 Drax_11

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

AUD_SPK_L-_C11 1 AFTP2901
AUD_SPK_L+_C11 1 AFTP2902
AUD_SPK_R-_C11 1 AFTP2903
AUD_SPK_R+_C11 1 AFTP2904

20170925

Delete SPK2 Conn

Combo Jack

[27] MIC2_VREFO
RN2901
SRN2K2J-1-GP

[27] RING2
[27] AUD_HP1_JACK_L
R29081 10R2F-L-GP
AUD_HP1_JACK_L

[27] LINE1_L
[27] AUD_HP1_JACK_R
C2907 SC10U6D3V3MX-DL-GP
LINE1-L
R29221 1KR2J-1-GP
R29101 10R2F-L-GP
AUD_HP1_JACK_R

[27] LINE1_R
C2908 SC10U6D3V3MX-DL-GP
LINE1-R
R29211 1KR2J-1-GP

[27] SLEEVE

[27] LINE1_VREFO
D2901
BAT54AW-4-GP
075.00054.0G7D
LINE1_VREFO_D1
R2912 4K7R2J-2-GP
LINE1_VREFO_D2
R2928 4K7R2J-2-GP

EC2908 SC100P50V2JN-3DLGP
EC2907 SC100P50V2JN-3DLGP
EC2906 SC100P50V2JN-3DLGP
EC2905 SC100P50V2JN-3DLGP
AUD_AGND AUD_AGND

need Change

R29061 20171031 2 Do Not Stuff RING2_R
R29071 20171031 2 Do Not Stuff AUD_PORTA_L_R_B
RING2_R [66]
AUD_PORTA_L_R_B [66]

JACK_PLUG
JACK_PLUG [66]

R29091 20171031 2 Do Not Stuff AUD_PORTA_R_R_B
R29111 20171031 2 Do Not Stuff SLEEVE_R
AUD_PORTA_R_R_B [66]
SLEEVE_R [66]

AUD_AGND
AUD_PORTA_L_R_B 1 AFTP2906
AUD_PORTA_R_R_B 1 AFTP2907
1 AFTP2908
AUD_SENSE 1 AFTP2909

Delay circuit

JACK_PLUG
R2905 Do Not Stuff DY
C2902 DY Do Not Stuff
Q2901 Do Not Stuff DY
Do Not Stuff
2nd = 84.2N702.W31
3rd = 84.07002.I31
AUD_AGND
R2914 0R3J-L1-GP
AUD_SENSE [27]
A00-20171129

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Speaker/HPMIC CONN***

Size	Document Number	Rev
A3	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 29 of 109

SSID = LOM

Blanking

Drax Rocket MLK

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)LOM*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 30 of 109

SSID = LAN

Blanking

Drax Rocket MLK

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*(Reserved)LAN*	
Size A4	Document Number Drax MLK/Rocket MLK AMD	Rev A00
Date: Tuesday, January 02, 2018	Sheet 31 of 109	

SSID = LAN CONN

Blanking

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)RJ45+Transformer***

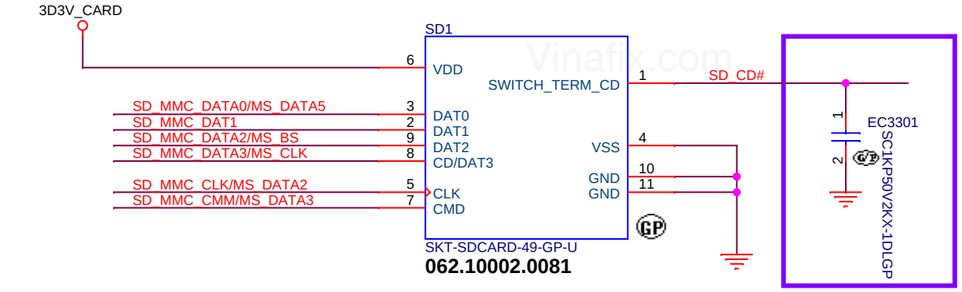
Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 32 of 109

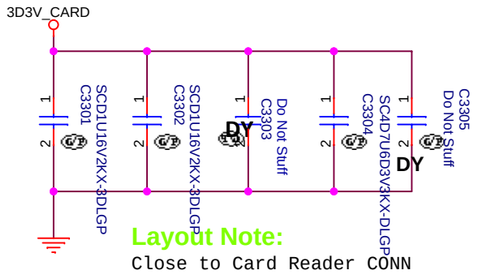
SSID = Card Reader

SD Card Connector

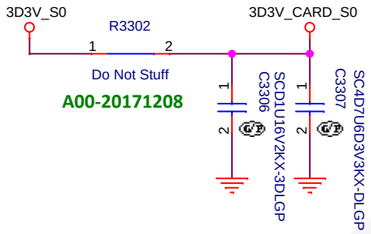
Pin Define	
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND



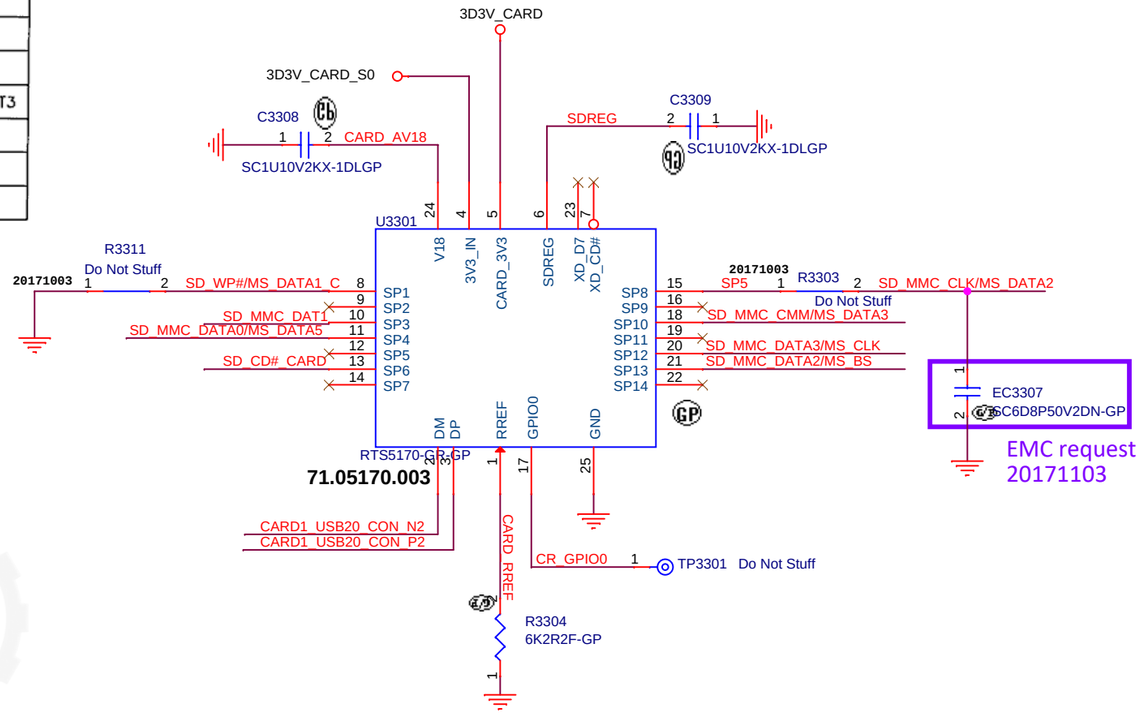
EMC request
need close to SD connector
20171103



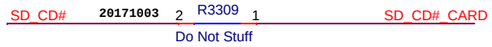
Layout Note:
Close to Card Reader CONN



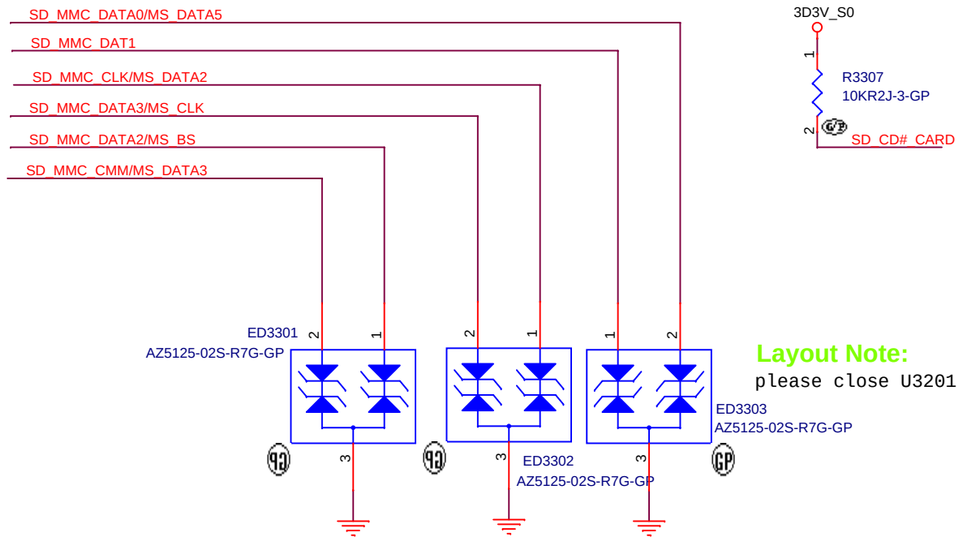
A00-20171208



EMC request
20171103

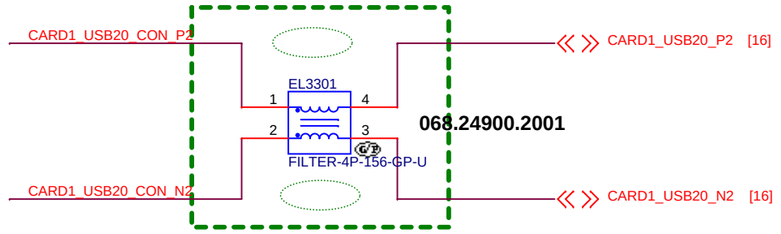


For EMI Reserved



Layout Note:
please close U3201

Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



Remove 0 ohm co-lay
A00-20171129

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Title: Card Reader + CONN

Size	Document Number	Rev
A3	Drax MLK/Rocket MLK AMD	A00

Date: Tuesday, January 02, 2018 Sheet 33 of 109

SSID = USB

Blanking

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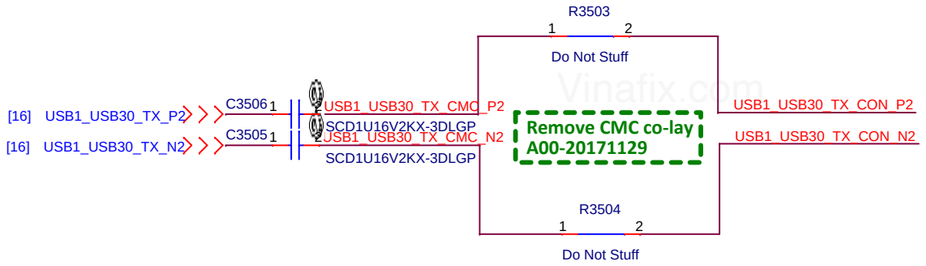
Taipei Hsien 221, Taiwan, R.O.C.

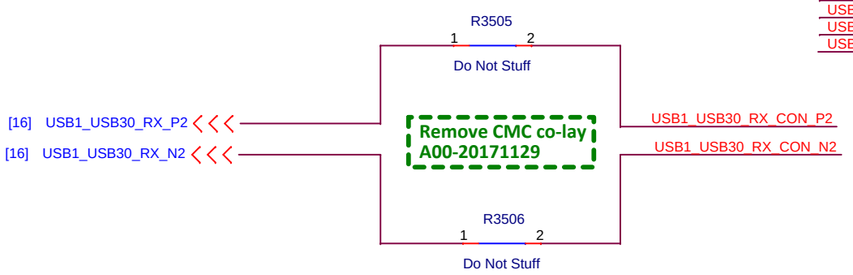
Title: *(Reserved)USB 2.0 Port*

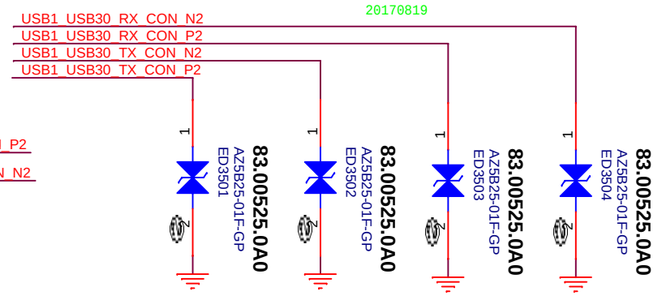
Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

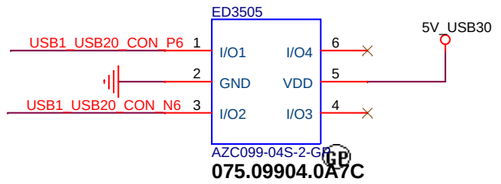
Date: Tuesday, January 02, 2018 Sheet 34 of 109

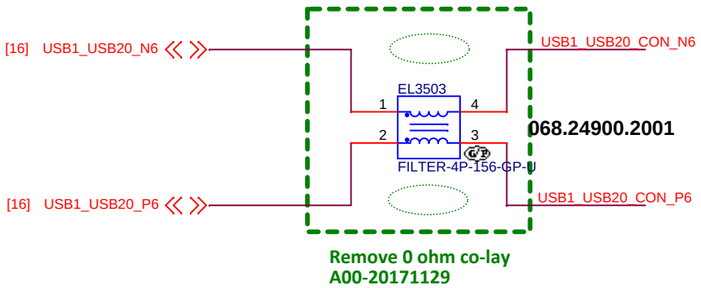
SSID = USB

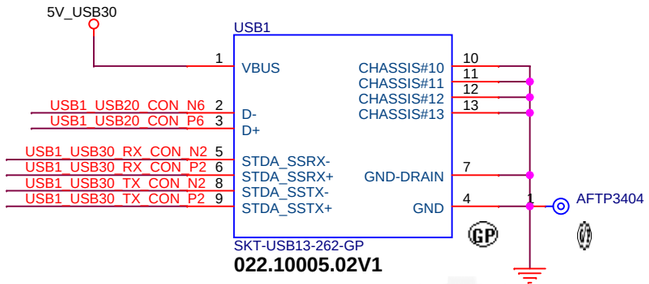


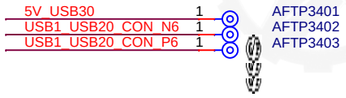








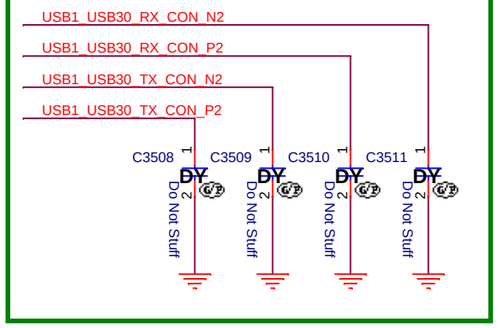




USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

Reserved for RF



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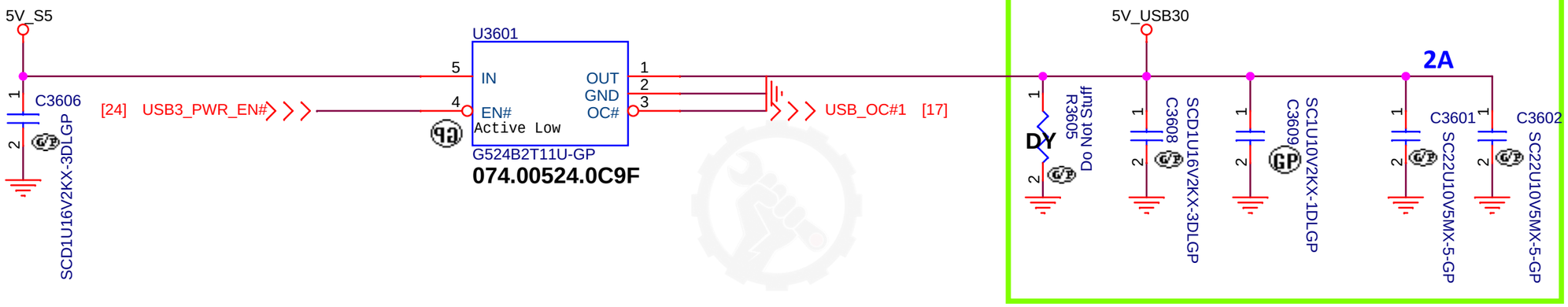
Title	USB3.0 CONN	
Size	Document Number: Drax MLK/Rocket MLK AMD	Rev: A00
Date: Tuesday, January 02, 2018	Sheet 35 of 109	

USB3.0 Port1



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Title	***USB Power SW***	
Size A4	Document Number ***Drax MLK/Rocket MLK AMD***	Rev ***A00***
Date: Tuesday, January 02, 2018	Sheet 36 of 109	

SSID = USB

Blanking

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Title: *USB2.0 HUB*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 37 of 109

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Title: **(Reserved)**

Size	Document Number	Rev
A4	**Drax MLK/Rocket MLK AMD**	**A00**

Date: Tuesday, January 02, 2018 Sheet 38 of 109

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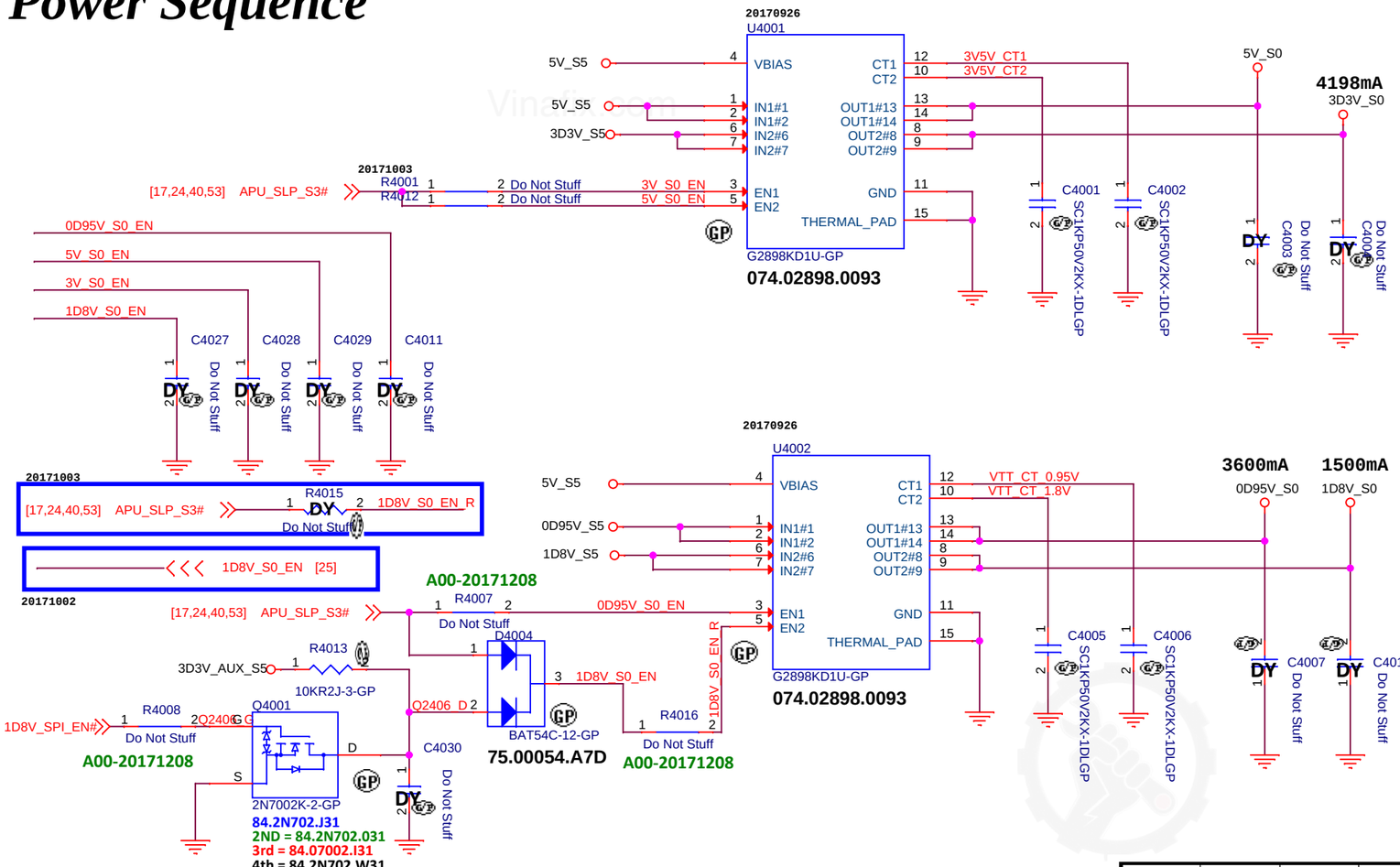
Title

(Reserved)

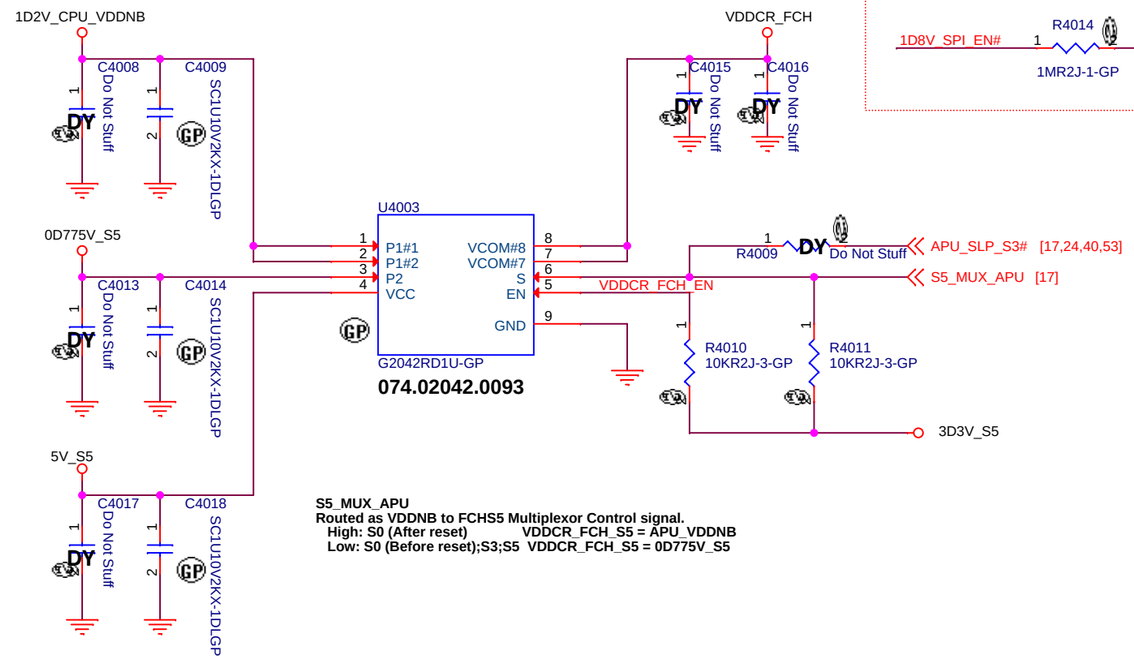
Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 39 of 109

Power Sequence



VDDNB to FCHS5 Multiplexor Control signal



S5_MUX_APU
Routed as VDDNB to FCHS5 Multiplexor Control signal.
High: S0 (After reset) VDDCR_FCH_S5 = APU_VDDNB
Low: S0 (Before reset);S3;S5 VDDCR_FCH_S5 = 0D775V_S5

DVT2: Add 1M ohm Pull-down on 1D8V_SPI_EN#. 7/18

VCC	EN	S	P1 Voltage	Function
5	0	X	X	Both P1 and P2 do not pass to VCOM VCOM is with pull low R of 200 Ω
5	1	0	< P2	P2 passed to VCOM
5	1	0	> P2	P1 passed to VCOM
5	1	1	< 2.0V	P1 passed to VCOM

"X" means don't care

Table 148. S5_MUX_CTRL State Table

Platform Power State	S5_MUX_CTRL Signal Level	SLP_S3_L	SLP_S5_L	VDDCR_FCH_S5 Voltage
G3	X	0	0	OFF
S5	0	0	0	ON (= VDDCR_FCH_ALW)
S3	0	0	1	ON (= VDDCR_FCH_ALW)
S0, but still in Reset	0	1	1	ON (= VDDCR_FCH_ALW) or if VDDCR_NB ≥ VDDCR_FCH_ALW, tracks VDDCR_NB
S0	1	1	1	Tracks VDDCR_NB

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Title: ***Power Plane Enable&Sequence***

Size: A3 | Document Number: **Drax MLK/Rocket MLK AMD** | Rev: **A00**

Date: Tuesday, January 02, 2018 | Sheet 40 of 106

(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 41 of 106

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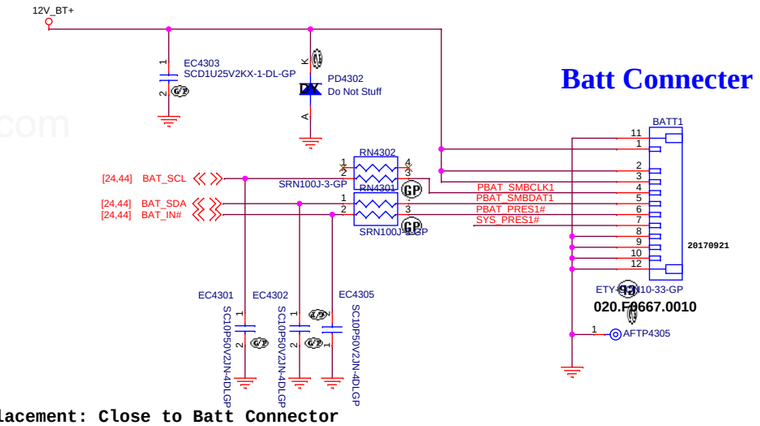
Title: *(Reserved)*

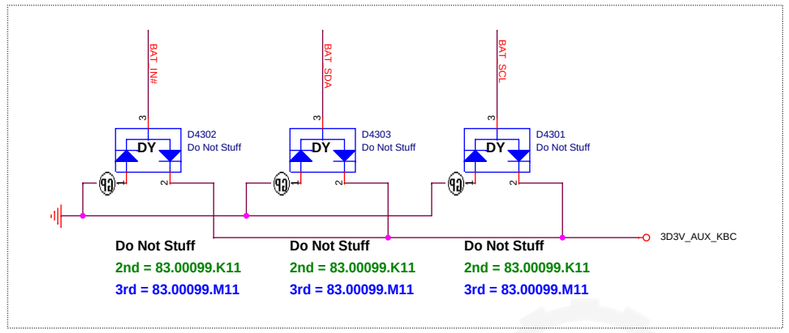
Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

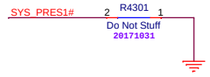
Date: Tuesday, January 02, 2018 Sheet 42 of 109

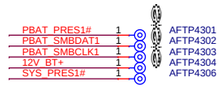
SSID = PWR.Support



Placement: Close to Batt Connector



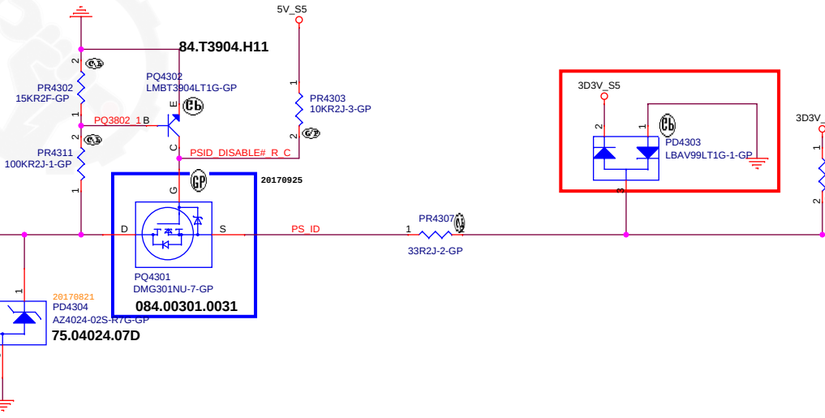


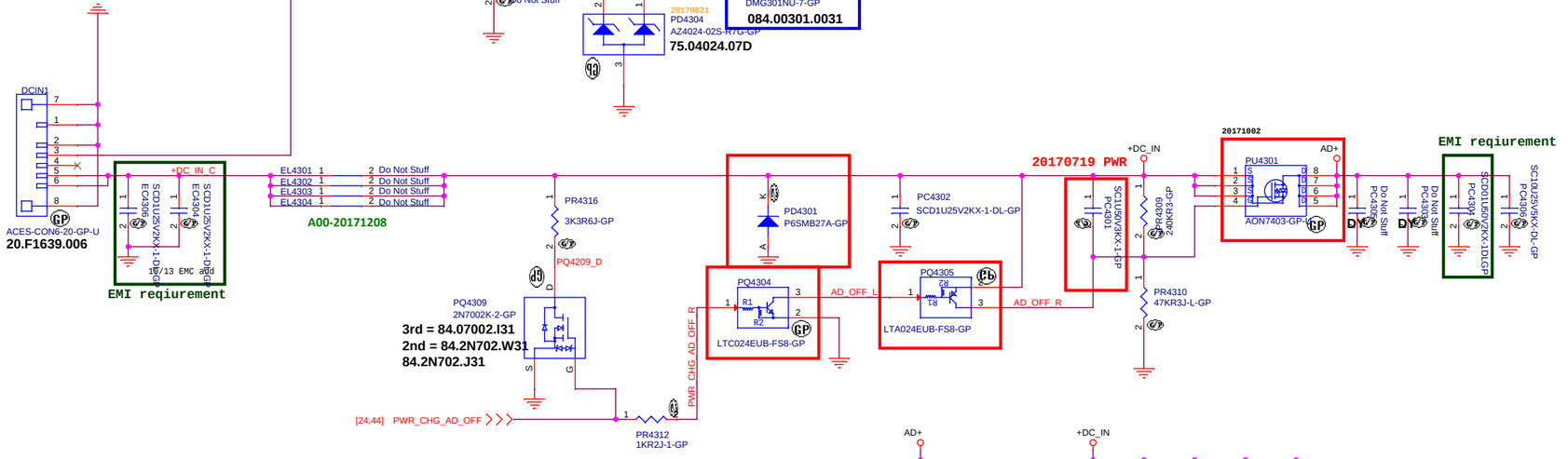


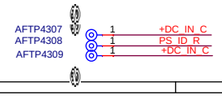
SSID = PWR.Support

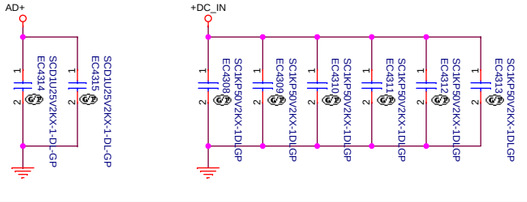
0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil









Drax Rocket MLK

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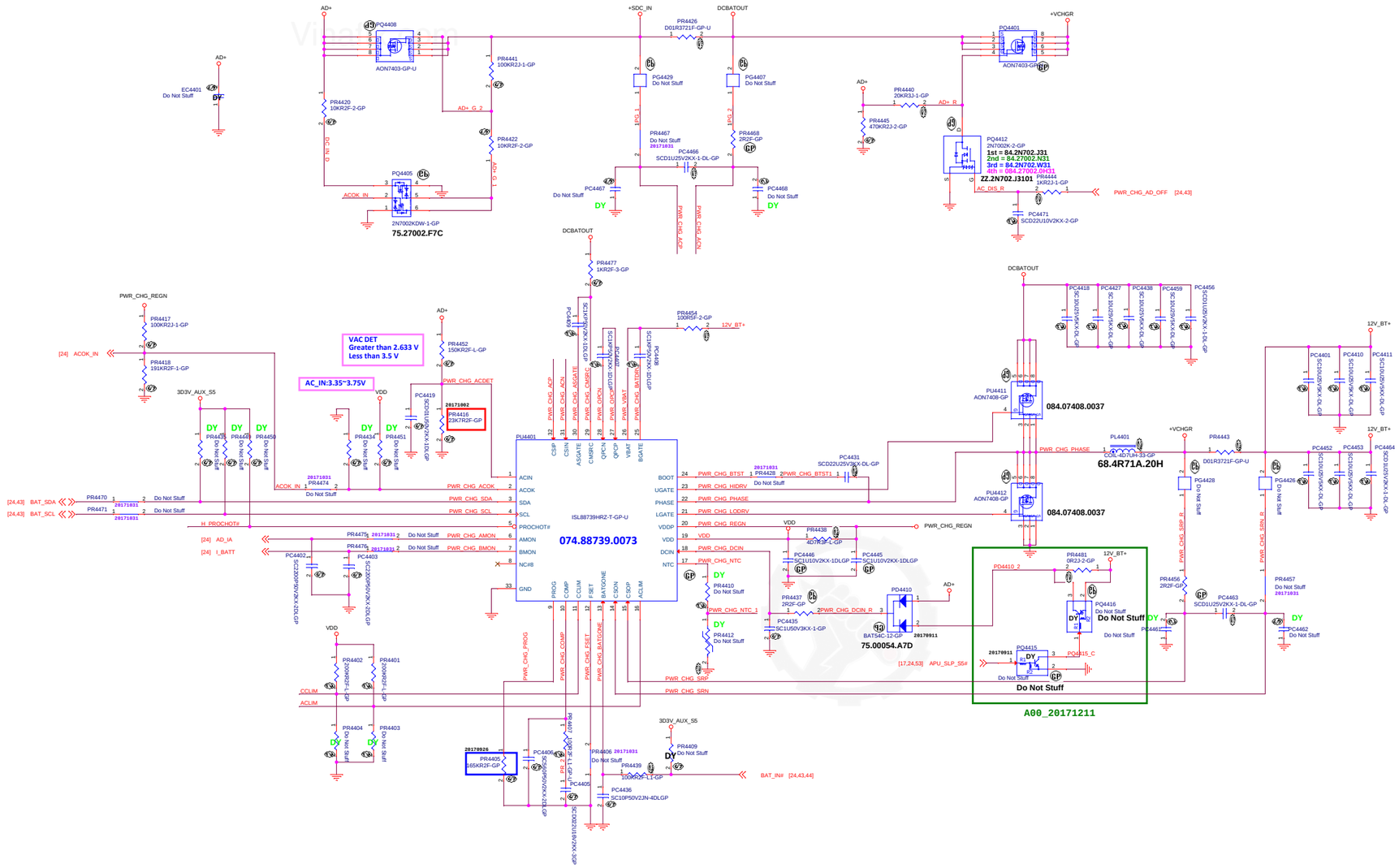
Taipei Hsien 221, Taiwan, R.O.C.

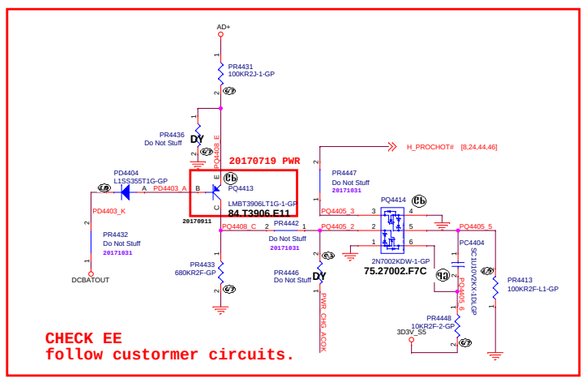
Title: BATTERY CONN

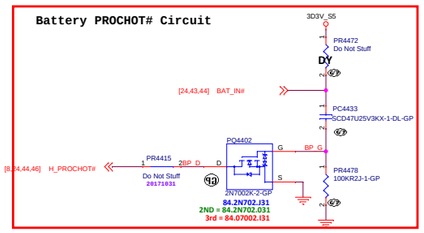
Size	Document Number	Rev
A2	Drax MLK/Rocket MLK AMD	A00

Date: Tuesday, January 02, 2018 Sheet 43 of 109

Main Func = Charger







A00_20171211

Drax Rocket MLK

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Title: CHARGER(ISL88739)

Size	Document Number	Rev
A1	Drax MLK/Rocket MLK AMD	A00

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SSID = PWR.Plane.Regulator_5v3p3v

Design Current = 3A
4.5A < OCP <6A

Cyntec, 7x7x3
DCR: 18~20mOhm
Idc : 8A , Isat : 14A

20171117-DVT2
Change IC to 6575 for
accustic noise issue

Design Current = 7.2A
10.8A < OCP < 14.4A

Cyntec, 7x7x3
DCR: 18~20mOhm
Idc : 8A , Isat : 14A

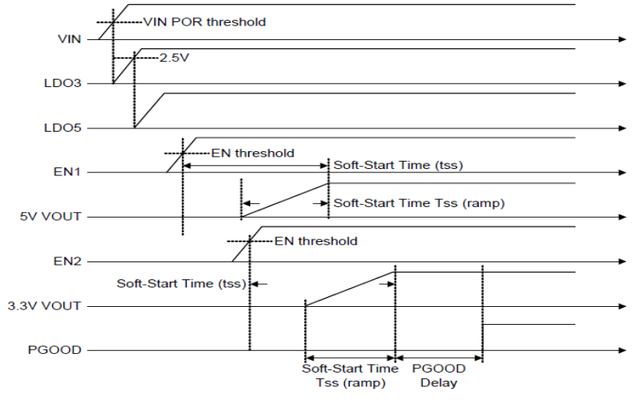

Figure 6. RT6575B Timing

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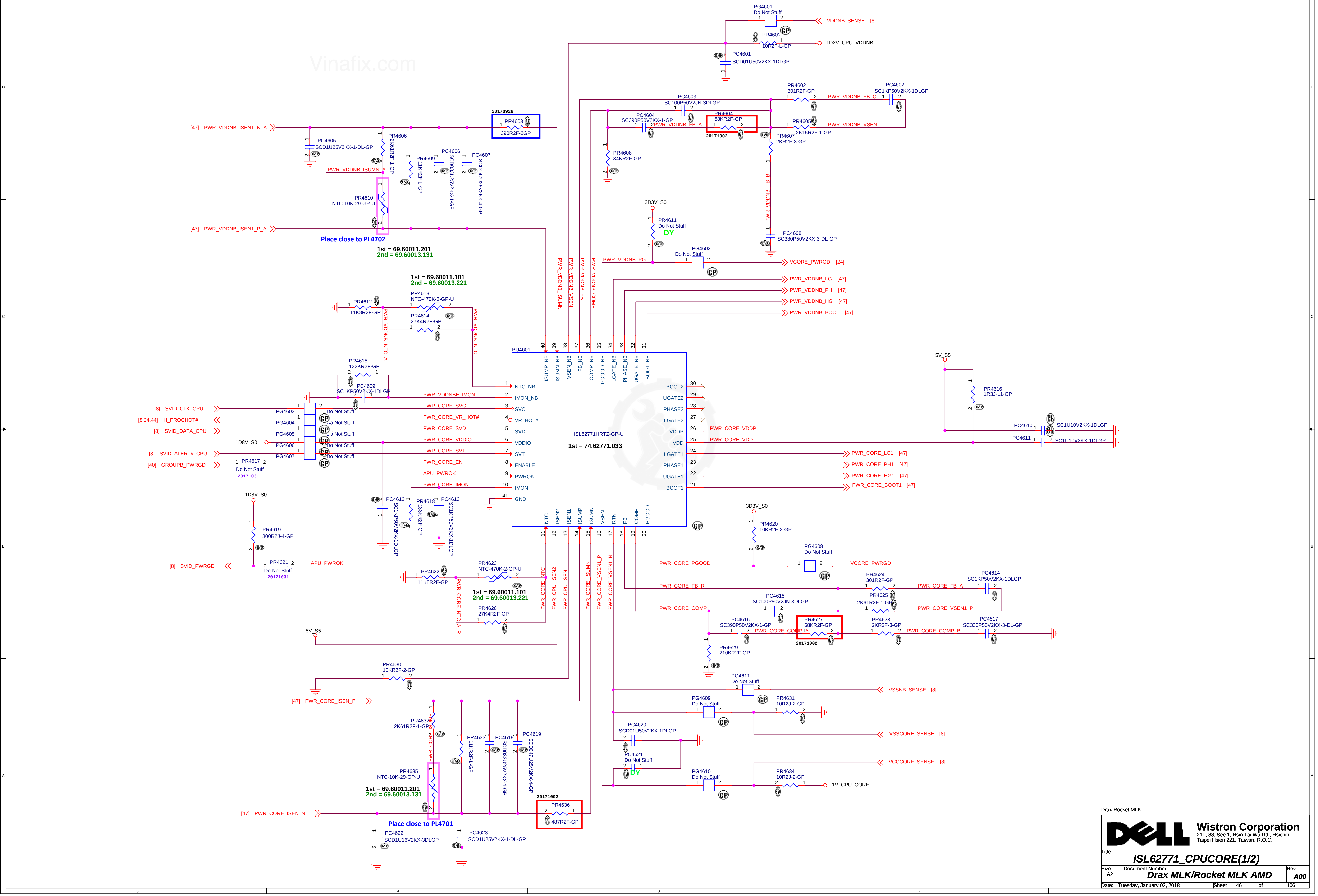
Title: RT6575_5V/3D3V

Size	Document Number	Rev
A2	Drax MLK/Rocket MLK AMD	A00

Date: Tuesday, January 02, 2018 Sheet 45 of 106

SSID = CPU.Regulator



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Taipei Hsien 221, Taiwan, R.O.C.

Title		
ISL62771_CPUCORE(1/2)		
Size A2	Document Number: Drax MLK/Rocket MLK AMD	Rev A00
Date: Tuesday, January 02, 2018	Sheet 46 of 106	

SSID = CPU.Regulator

DCBATOUT
PWR_DCBATOUT_VCCCORE
PG4701 Do Not Stuff
PG4702 Do Not Stuff
PG4703 Do Not Stuff
PG4704 Do Not Stuff
PG4705 Do Not Stuff

PU4701
[46,47] PWR_CORE_HG
[46,47] PWR_CORE_LG
FDMS3600-02-RJK0215-COLAY-GP
1st = 075.07321.0073

15W
PU4702
[46,47] PWR_CORE_HG
[46,47] PWR_CORE_LG
Do Not Stuff
1st = 075.07321.0073

PC4701 Do Not Stuff DY
PC4704 SC10U25V5KX-DL-GP
PC4705 SC10U25V5KX-DL-GP
PC4706 SC10U25V5KX-DL-GP
PC4707 SC10U25V5KX-DL-GP
PC4702 SCD1U25V2KX-1-DL-GP
PC4703 SCD1U25V2KX-1-DL-GP

Layout Note:
Close to CPU Power
DCBATOUT
PT4708 SE33U25VM-11-GP
For acoustic noice

[46] PWR_CORE_PH1
[46] PWR_CORE_BOOT1
PR4701 2D2R3-1-U-GP
PWR_CORE_BOOT
PC4708 SCD22U25V2KX-4-GP
20171002

Cyntec, 6.8x7.6x3
DCR: 0.902mOhm+/-7%
Idc : 37A , Isat : 41A
PL4701 COIL-D15UH-7-GP

6W:TDC=11A, EDP=15A, OCP>36A
1V_CPU_CORE

PG4706 Do Not Stuff
PG4707 Do Not Stuff
PT4701 SE330U2VDM-4-GP
PT4702 SE330U2VDM-4-GP
PC4709 DY Do Not Stuff
PC4710 SC22U6D3V3MX-1-DL-GP

330uF/2V, L:7.5, W: 4.5, H: 2.0
ESR=9mohm
Ripple Current=6300 mA

[46] PWR_CORE_ISEN_P
[46] PWR_CORE_ISEN_N
PR4702 3K65R2F-1-GP
PR4703 1R2F-GP
PWR_CORE_ISEN1_P
PWR_CORE_ISEN1_N

DCBATOUT
PWR_DCBATOUT_VDDNB
PG4708 Do Not Stuff
PG4709 Do Not Stuff
PG4710 Do Not Stuff
PG4711 Do Not Stuff

PU4705
[46,47] PWR_VDDNB_HG
[46,47] PWR_VDDNB_LG
FDMS3600-02-RJK0215-COLAY-GP
1st = 075.07321.0073

15W
PU4706
[46,47] PWR_VDDNB_HG
[46,47] PWR_VDDNB_LG
Do Not Stuff
1st = 075.07321.0073

PWR_DCBATOUT_VDDNB
PC4711 SCD1U25V2KX-1-DL-GP
PC4712 SC10U25V5KXDL-GP
PC4713 SC10U25V5KX-DL-GP
PC4714 SC10U25V5KX-DL-GP
PC4715 SC10U25V5KX-DL-GP
PC4716 SCD1U25V2KX-1-DL-GP
PC4720 DY Do Not Stuff

Layout Note:
Close to CPU Power
DCBATOUT
PT4707 SE33U25VM-11-GP
For acoustic noice

[46] PWR_VDDNB_PH
[46] PWR_VDDNB_BOOT
PR4704 2D2R3-1-U-GP
PWR_VDDNB_BOOT_A
PC4717 SCD22U25V2KX-4-GP
20171002

Cyntec, 6.8x7.6x3
DCR: 0.902mOhm+/-7%
Idc : 37A , Isat : 41A
PL4702 COIL-D15UH-7-GP

6W:TDC=11A, EDP=15A, OCP>36A
1D2V_CPU_VDDNB

PG4712 Do Not Stuff
PG4713 Do Not Stuff
PT4705 SE330U2VDM-4-GP
PT4706 SE330U2VDM-4-GP
PC4718 DY Do Not Stuff
PC4719 SC22U6D3V3MX-1-DL-GP

330uF/2V, L:7.5, W: 4.5, H: 2.0
ESR=9mohm
Ripple Current=6300 mA

[46] PWR_VDDNB_ISEN1_P_A
[46] PWR_VDDNB_ISEN1_N_A
PR4705 3K65R2F-1-GP
PR4706 1R2F-GP
PWR_VDDNB_ISEN1_P
PWR_VDDNB_ISEN1_N

Drax Rocket MLK

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62771_CPUCORE(2/2)
Size: A2
Document Number: Drax MLK/Rocket MLK AMD
Rev: A00
Date: Tuesday, January 02, 2018
Sheet 47 of 106

(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 48 of 106

VDDCR_FCH_S5=0.775V , IOUT=100mA

5V_S5

PC4901 1 — 2 DY Do Not Stuff

PC4902 1 — 2 SC1U10V2KX-1DLGP

PU4901
APL5337KAI-TRG-2-GP

5	NC#5	VOUT	4
6	VCNTL	VREF	3
7	NC#7	GND	2
8	NC#8	VIN	1
9	GND		

PWR_0D775V_VREF

PWR_0D775V_VIN

PG4902 Do Not Stuff 1 — 2 GP

1D8V_S5

PC4905 1 — 2 SC10U6D3V3MX-DL-GP

1st = 074.05337.0031

PWR_0D775V

PC4903 1 — 2 SC1U10V2KX-1DLGP

PC4904 1 — 2 SC10U6D3V3MX-DL-GP

PG4901 Do Not Stuff 1 — 2 GP

0D775V_S5

3D3V_S5

PR4901 1 — 2 DY Do Not Stuff

PQ4901

1	G1	D1	6
2	S1/D2	G2	5
3	S2	S2	4

DY

PWR_0D775V_EN_R

PWR_0D775V_EN

Do Not Stuff GP

PG4903 2 — 1 Do Not Stuff

3V_5V_PWRGD [17,45,54]

PC4907 1 — 2 DY Do Not Stuff

Do Not Stuff
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

1D8V_S5

PR4902 1 — 2 3K9R2F-GP

PR4903 1 — 2 3K01F-GP

PC4906 1 — 2 SC1U10V2KX-1DLGP

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VDDCRGFX_APL5337***	
Size: A4	Document Number: ***Drax MLK/Rocket MLK AMD***	Rev: ***A00***
Date: Tuesday, January 02, 2018	Sheet 49 of 106	

(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 50 of 106

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Drax Rocket MLK

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 51 of 106

DCBATOUT
PWR_DCBATOUT_0D95V
PG5201 Do Not Stuff
PG5202 Do Not Stuff
PG5203 Do Not Stuff

5V_S5
PR5201 10R2F-L-GP
PC5201 SC4D7U25V5KX-DL-GP
PC5202 SC1U10V2KX-1DLGP
PR5202 8K2R2F-1-GP
PWR_0D95V_VCC
PWR_0D95V_CS

PWR_DCBATOUT_0D95V
PC5203 SCD1U25V2KX-1-DL-GP
PC5204 SC10U25V5KX-DL-GP
PC5205 SC10U25V5KX-DL-GP
PD5201 Do Not Stuff
Add TVS PD5201 083.04024.0AA1

PWR_DCBATOUT_0D95V
PG5204 Do Not Stuff
PG5205 Do Not Stuff
PG5206 Do Not Stuff
PG5207 Do Not Stuff
PG5208 Do Not Stuff
PG5209 Do Not Stuff
PG5210 Do Not Stuff
PG5211 Do Not Stuff

PR5205 = 510K
Fs = 400~550KHz

3D3V_S5
PR5203 100KR2J-1-GP

20171031
[24] 0D95V_S5_PWRGD
PR5204 Do Not Stuff
PWR_0D95V_PG

PWR_DCBATOUT_0D95V
PR5205 510KR2F-GP
PWR_0D95V_TON

[24] 0D95V_S5_EN
PR5206 DY Do Not Stuff
PWR_0D95V_EN

[54] 1D8V_S5_PWRGD
PR5209 Do Not Stuff
20171031

TP5201
PWR_0D95V_VLDOIN

PU5201
CS, VCC, V+ V+ V+ V+ V+
PGOOD
TON
S5
S3
VLDOIN
VTTGND VTTGND VTTGND
VTT
VTTSNS
NC#26, GND, VTTREF
G5388K11U-GP

BST
LX#25
LX#17 LX#18 LX#19 LX#20 LX#35
PWR_0D95V_PH
PGND PGND PGND PGND PGND PGND
VDDQSNS
PWR_0D95V_VDDQ
VDDQSET
PWR_0D95V_FB
PWR_0D95V_VTTREF

PR5210 2R3F-GP
PWR_0D95V_BOOT
PC5206 SCD1U25V2KX-1-DL-GP
Add Boot R 2ohm 0603 and Net name

TDC : 7.69A
15.38A >OCP>11.535A
Cyntec. 7 x 7 x 3.0 mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A
PL5201 COIL-1UH-34-GP-U1

PR5211 Do Not Stuff
PWR_0D95V_SNUB
PC5214 Do Not Stuff
Add DY RC snubber and Net name
2.2 ohm 0805
1000 pF 0402 50V

PG5212 Do Not Stuff

R1 PR5207 2K67R2F-2-GP
R2 PR5208 10KR2F-2-GP
Manual:64.40215.6DL for 25W
Vout=0.75*(1+R1/R2) = 0.95V

PWR_0D95V
PC5207 PC5208 PC5209 PC5210 PC5211 PC5212
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
Do Not Stuff
Do Not Stuff

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G5338K11U_0D95V
Size: A3
Document Number: Drax MLK/Rocket MLK AMD
Rev: A00
Date: Tuesday, January 02, 2018
Sheet 52 of 106

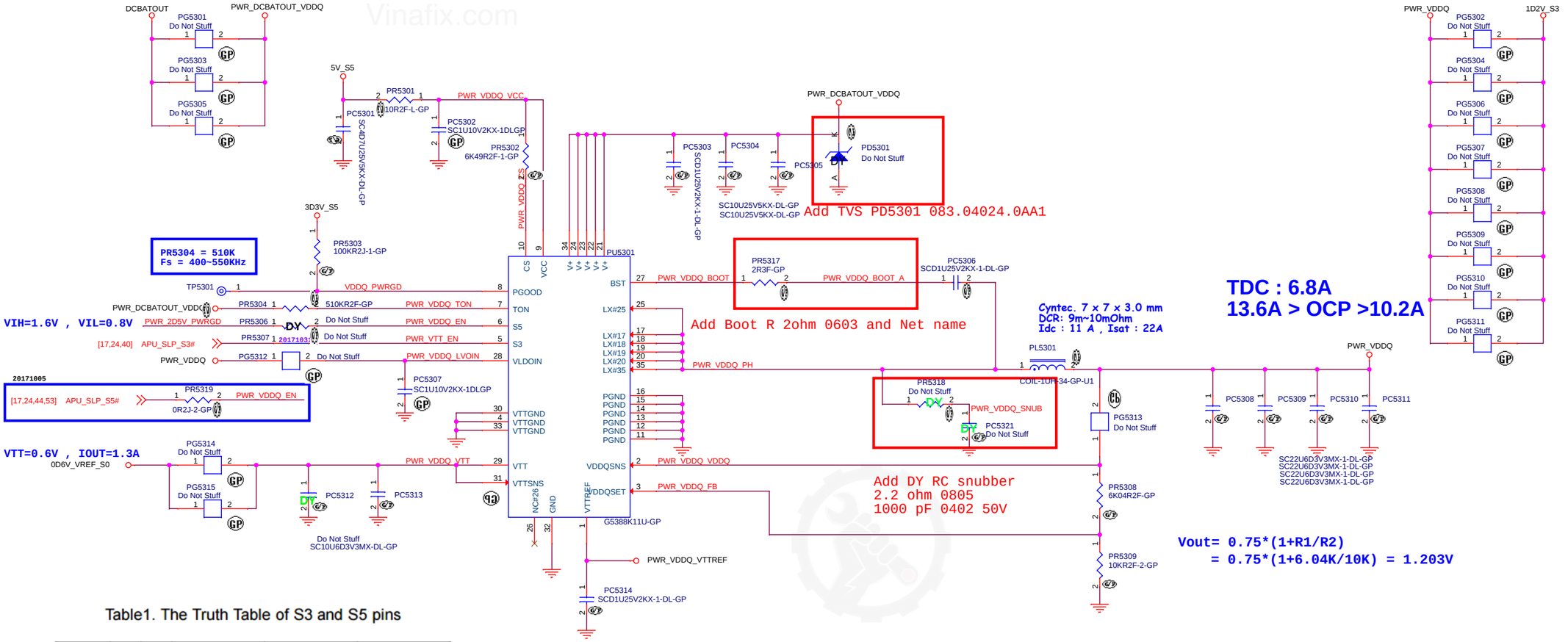
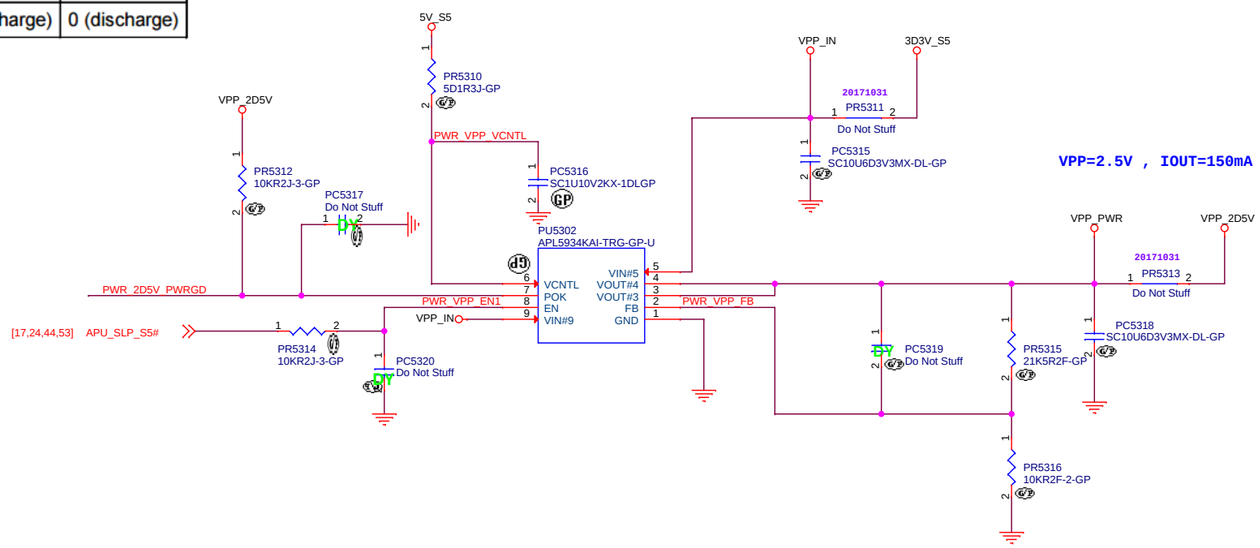


Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)



Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VDDQ&VTT&VPP_G5388K11U

Size: C | Document Number: Drax MLK/Rocket MLK AMD | Rev: A00

Date: Tuesday, January 02, 2018 | Sheet 53 of 106

SSID = PWR.Plane.Regulator_1p5v_1p8v

Design Current =1.88A

3D3V_S5
PG5402 Do Not Stuff
PG5403 Do Not Stuff
PC5405 SC10U6D3V3MX-DL-GP
PC5406 SC10U6D3V3MX-DL-GP

PU5401 RT5797ALGQW-GP
PGND 9
PGND 4
VIN 3
PG 2
FB 1
NC#5 5
LX 6
EN 7
SGND 8
PWR_1D8V_PVIN
PWR_1D8V_PH
PWR_1D8V_EN

Chilisin.
2.5mm¡Ñ2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A
PL5401 IND-1UH-300-GP

1D8V_PWR
PG5401 Do Not Stuff
PC5407 SC22U6D3V3MX-1-DL-GP
PC5408 SC22U6D3V3MX-1-DL-GP
PC5410 Do Not Stuff DY
PG5404 Do Not Stuff
PG5405 Do Not Stuff
PG5406 Do Not Stuff
1D8V_S5

PWR_1D8V_PG
3D3V_S5
PR5407 100KR2J-1-GP
[52] 1D8V_S5_PWRGD
PR5412 Do Not Stuff 20171031
1D8V_PWR_GOOD

[17,45,49] 3V_5V_PWRGD
PR5409 Do Not Stuff 20171031
PC5411 Do Not Stuff DY

PWR_1D8V_FB
PWR_1D8V_FB_R1
PR5403 102KR2F-GP
R1
PC5401 SC22P50V2JN-4DLGP
PR5406 Do Not Stuff DY
PR5405 51KR2F-L-GP
R2
PWR_1D8V_FB_R2
PC5412 Do Not Stuff DY

Vo=0.6x(1+R1/R2)
=0.6x(1+102/51)
=1.8

RT9078-18GJ5 for 1D8V_AUX_S5

Design Current =30mA

3D3V_AUX_S5
PR5413 Do Not Stuff 20171031
5V_AUX_S5
PR5410 Do Not Stuff DY
PC5420 SC1U10V2KX-1DLGP

20170818
PU5402
1D8V_PWR_VIN
1D8V_AUX_EN
VIN
GND
EN
VOUT
SNS/NC#4
RT9078-18GJ5-GP
074.09078.003F
PC5418 Do Not Stuff DY

1D8V_AUX_PWR
PG5411 Do Not Stuff
1D8V_AUX_S5
PC5419 SC1U10V2KX-1DLGP

[24] PSL_OUT#
PSL_OUT#
PR5411 Do Not Stuff 20171031
Q5102_G
Q5401
G
D
S
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31
1D8V_AUX_EN
3D3V_AUX_KBC
PR5414 10KR2J-3-GP

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC2DC_1D8V/1D5V(RT5797)
Size: A3 | Document Number: Drax MLK/Rocket MLK AMD | Rev: A00
Date: Tuesday, January 02, 2018 | Sheet 54 of 106

SSID = VIDEO

Panel Conn.

LCD1
ACES-CON40-184-GP
20.K0678.040

19V_DCBATOUT_LCD

eDP_TX_CON_N1 — C5513 — SCD1U16V2KX-3DLGP — eDP_TX_CPU_N1 [8]
eDP_TX_CON_P1 — C5510 — SCD1U16V2KX-3DLGP — eDP_TX_CPU_P1 [8]
eDP_TX_CON_N0 — C5507 — SCD1U16V2KX-3DLGP — eDP_TX_CPU_N0 [8]
eDP_TX_CON_P0 — C5506 — SCD1U16V2KX-3DLGP — eDP_TX_CPU_P0 [8]
eDP_AUX_CON_P — C5501 — SCD1U16V2KX-3DLGP — eDP_AUX_CPU_P [8]
eDP_AUX_CON_N — C5505 — SCD1U16V2KX-3DLGP — eDP_AUX_CPU_N [8]

FHD
FHT

Camera

CCD_USB20_CON_P0
CCD_USB20_CON_N0
DMIC_CLK_C
DMIC_DATA_C
MIC_GND
DBC_EN_R — R5501 (20171003) — Do Not Stuff — DBC_EN [17]
LCD_TST_C
DP_HPD0_C
BLON_OUT_C
LCD_BRIGHTNESS
TPNL_INT

Touch Panel

TS_USB20_CON_N1
TS_USB20_CON_P1
PROJECT_ID1 — TP5501 (20170925) — Do Not Stuff
3D3V_LCDVDD_S0
TPAN_VDD
3D3V_CAMERA_S0

Power Pin Count : 7
GND Pin Count : 9

3D3V_LCDVDD_S0
C5508 — SCD1U16V2KX-3DLGP
C5509 — SCD1U10V2KX-1DLGP

LCD_BRIGHTNESS
EC5507 — SC6P50V2CN-1-NL-GP

TPNL_INT — R5504 33R2J-2-GP — TOUCH_PANEL_INTR# [17,24]
C5518 — DY — Do Not Stuff

R55051 100KR2J2-GP BKLT_CTRL
R55061 100KR2J2-GP BLON_OUT_C
R55071 100KR2J2-GP eDP_HPD_CPU
R55081 100KR2J2-GP LVDS_VDD_EN_R

Layout: Close CONN LCD1

20171003 — R5502 — Do Not Stuff — MIC_GND

DMIC_CLK_C
DMIC_DATA_C
RN5502 — SRN33J-5-GP-U
DMIC_CLK [27]
DMIC_DATA [27]
EC5505 — SC22P50V2JN-4DLGP
EC5506 — SC22P50V2JN-4DLGP

Remove 0 ohm co-lay
A00-20171129

CCD_USB20_CON_P0 — CCD_USB20_P0 [16]
CCD_USB20_CON_N0 — CCD_USB20_N0 [16]
TS_USB20_CON_N1 — TS_USB20_N1 [16]
TS_USB20_CON_P1 — TS_USB20_P1 [16]

Camera
EL5501 — FILTER-4P-156-GP-U — 068.24900.2001

Touch Panel
EL5502 — FILTER-4P-156-GP-U — 068.24900.2001

ED5501 — DY — Do Not Stuff
TS_USB20_CON_P1 — I/O1
TS_USB20_CON_N1 — I/O4
GND
TPAN_VDD — VDD
I/O2
I/O3

EMC 20170713

Hi:2.0V
Lo:0.8V

3D3V_S0
3D3V_LCDVDD_S0
Layout 40 mil
U5501 — G517F1T12U-GP — 074.51712.009F
OUT / GND / OC# / IN / EN
C5512 — SC4D7U6D3V3KX-DLGP
20170928 — DY — C5521 Do Not Stuff — C5511 SC4D7U6D3V3KX-DLGP

LVDS_VDD_EN — D5501 — DY — Do Not Stuff — LVDS_VDD_EN_R
[24] LCD_TST_EN
20171003 — R5503 — Do Not Stuff

D5502 — BAT54C-12-GP — 75.00054.A7D
BKLT_CTRL
EC_BRIGHTNESS [24]
L_BKLT_CTRL
R5524 Do Not Stuff — DY

DP_HPD0_C
LCD_BRIGHTNESS
RN5503 — SRN100J-4-GP
BKLT_CTRL — eDP_HPD_CPU [8]
BLON_OUT_C
LCD_TST_C
RN5504 — SRN100J-4-GP
BLON_OUT [24]
LCD_TST [24]

Level shift

3D3V_S0 — R5516 Do Not Stuff — DY
1D8V_S0 — R5521 Do Not Stuff — DY
1D8V_S5 — R5522 Do Not Stuff — DY
LVDS_VDD_EN_B
LVDS_VDD_EN — Q5501 Do Not Stuff — LVDS_VDD_EN_CPU [8,24]

Do Not Stuff
2nd = 84.T3904.K11
3rd = 84.T3904.C11

3D3V_S0 — R5527 10KR2J-3-GP
1D8V_S0 — R5526 2K2R2J-2-GP
L_BKLT_CTRL_B
L_BKLT_CTRL — Q5503 LMBT3904LT1G-GP — L_BKLT_CTRL_CPU [8]

84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.T3904.C11

CAMERA POWER

Co-lay with F5502
3D3V_S0 — R5533 0R5J-5-GP — F5502 Do Not Stuff (20171003) — DY — 3D3V_CAMERA_S0
EC5510 — SC33P50V2JN-3DLGP
C5514 — SC4D7U6D3V3KX-DLGP

Do Not Stuff
2nd = 69.50011.081

INVERTER POWER

19V_DCBATOUT_LCD — F5501 PCTSW-1D1A24V-GP-U — 69.50007.A31 — DCBATOUT
C5502 — SC4D7U25V5KX-DL-GP
C5503 — SC1U50V2KX-1DLGP
C5504 — SCD1U25V2KX-1-DL-GP
EC5501 — SCD1U25V2KX-1-DL-GP
EC5502 — SCD1U25V2KX-1-DL-GP
EC5503 — SCD1U25V2KX-1-DL-GP

Co-lay with F5503
5V_S0 — R5534 0R5J-5-GP — F5503 (20171003) — DY — TPAN_VDD
Do Not Stuff
2nd = 69.50011.081
C5520 — SCD1U50V3KX-DL-GP
C5519 — SC4D7U25V5KX-DL-GP

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector
Size: A2
Document Number: Drax MLK/Rocket MLK AMD
Rev: A00
Date: Tuesday, January 02, 2018
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Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

Date: Tuesday, January 02, 2018 Sheet 56 of 109

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Follow Standard Net Naming rule

[8] HDMI_DDI_TX_N3
[8] HDMI_DDI_TX_P3
[8] HDMI_DDI_TX_N0
[8] HDMI_DDI_TX_P0
[8] HDMI_DDI_TX_N1
[8] HDMI_DDI_TX_P1
[8] HDMI_DDI_TX_N2
[8] HDMI_DDI_TX_P2

C5701 1 2 SCD1U16V2KX-3DLGP
C5702 1 2 SCD1U16V2KX-3DLGP
C5703 1 2 SCD1U16V2KX-3DLGP
C5704 1 2 SCD1U16V2KX-3DLGP
C5705 1 2 SCD1U16V2KX-3DLGP
C5706 1 2 SCD1U16V2KX-3DLGP
C5707 1 2 SCD1U16V2KX-3DLGP
C5708 1 2 SCD1U16V2KX-3DLGP

HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CON_P2

Close to HDMI Connector

RN5702 SRN499F-GP
RN5703 SRN499F-GP

3D3V_S0
Q5701
R5719 0Y Do Not Stuff
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

HDMI_PLL_GND

Close to Level Shift

HDMI_DDI_TX_CON_N3 ER5717 1 2 150R2F-1-GP HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N0 ER5714 1 2 150R2F-1-GP HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1 ER5715 1 2 150R2F-1-GP HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2 ER5716 1 2 150R2F-1-GP HDMI_DDI_TX_CON_P2

Reseve 150 ohm bridge resistance
on the HDMI trace as circle for EMI

5V_HDMI
EC5701 1 2 SCD1U25V2KX-1-DL-GP

Reseve 0.1uF for ESD

HDMI CONN

5V_S5
AFTP5402 1
F5701 POLYSW-1D1A6V-9-GP-U 2 1
69.48001.081
5V_HDMI

HDMI1
5V_HDMI 18 +5V_POWER
HDMI_DDI_TX_CON_P0 7 TMDS_DATA0+
HDMI_DDI_TX_CON_N0 9 TMDS_DATA0-
HDMI_DDI_TX_CON_P1 4 TMDS_DATA1+
HDMI_DDI_TX_CON_N1 6 TMDS_DATA1-
HDMI_DDI_TX_CON_P2 1 TMDS_DATA2+
HDMI_DDI_TX_CON_N2 3 TMDS_DATA2-
8 TMDS_DATA0_SHIELD
5 TMDS_DATA1_SHIELD
2 TMDS_DATA2_SHIELD
11 TMDS_CLOCK_SHIELD
HDMI_DDI_TX_CON_P3 10 TMDS_CLOCK+
HDMI_DDI_TX_CON_N3 12 TMDS_CLOCK-
SCL 15 HDMI_CLK_CON
SDA 16 HDMI_DATA_CON
CEC 13
DDC/CEC_GROUNG 17
HOT_PLUG_DETECT 19 HPD_HDMI_CON
RESERVED#14 14
GND 20
GND 21
GND 22
GND 23
HDMI (A_Type)
SKT-HDMI23-147-GP-U
022.10025.00F1

3D3V_S0
84.T3904.H11
Q5708 LMBT3904LT1G-GP
B HDMI_HPD_B 2 1 R5710 150KR2F-L-GP
R5711 200KR2F-L-GP
[8] HDMI_DET_CPU
R5712 1 2 HDMI_HPD_E 20171003 Do Not Stuff
R5709 100KR2J-1-GP

TP5701 Do Not Stuff
HPD_HDMI_CON
R5702 1 2 20171003 Do Not Stuff
HDMI_HPD_G

3D3V_S5
20170819 R5701 10KR2J-3-GP
Low active
HDMI_IN# [24]
Q5707
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

5V_S0
D5701 LBAW56LT1G-GP
83.00056.Y11
5V_DDC_HDMI1
5V_DDC_HDMI2
RN5701 SRN2K2J-1-GP

Level shift

HDMI_DATA_CON
Q5705 DMG301NU-7-GP
084.00301.0031
20170925
HDMI_SDA_CPU [8]
3D3V_S0

HDMI_CLK_CON
Q5703 DMG301NU-7-GP
084.00301.0031
20170925
HDMI_SCL_CPU [8]
3D3V_S0

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: Custom | Document Number: Drax MLK/Rocket MLK AMD | Rev: A00
Date: Tuesday, January 02, 2018 | Sheet 57 of 109

SSID = Display Port

Blanking

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved) Display Port*

Size | Document Number: *Drax MLK/Rocket MLK AMD* | Rev: *A00*

Date: Tuesday, January 02, 2018 | Sheet 58 of 109

SSID = DVI

Blanking

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

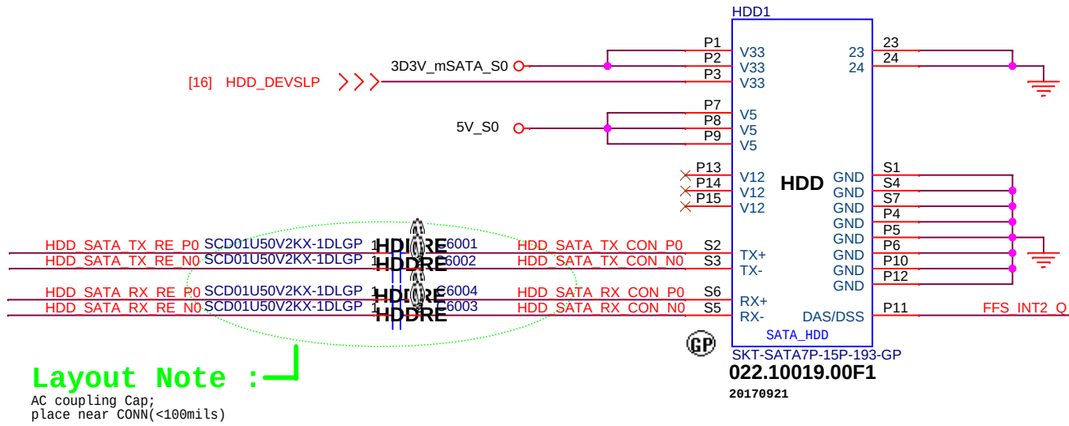
Title: *(Reserved) DVI*

Size	Document Number	Rev
	Drax MLK/Rocket MLK AMD	*A00*

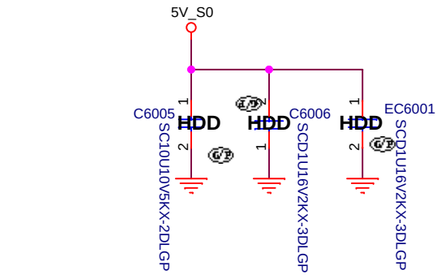
Date: Tuesday, January 02, 2018 Sheet 59 of 109

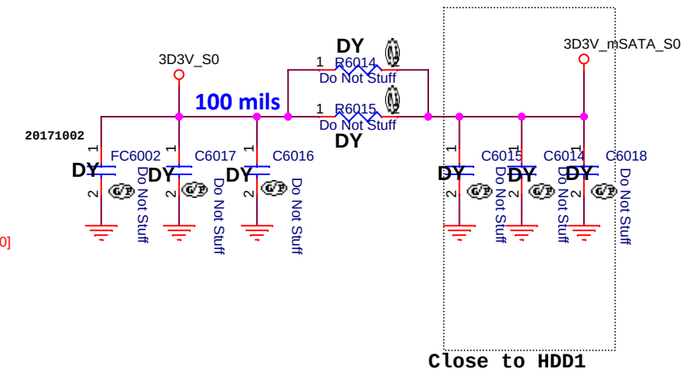
SSID = SATA

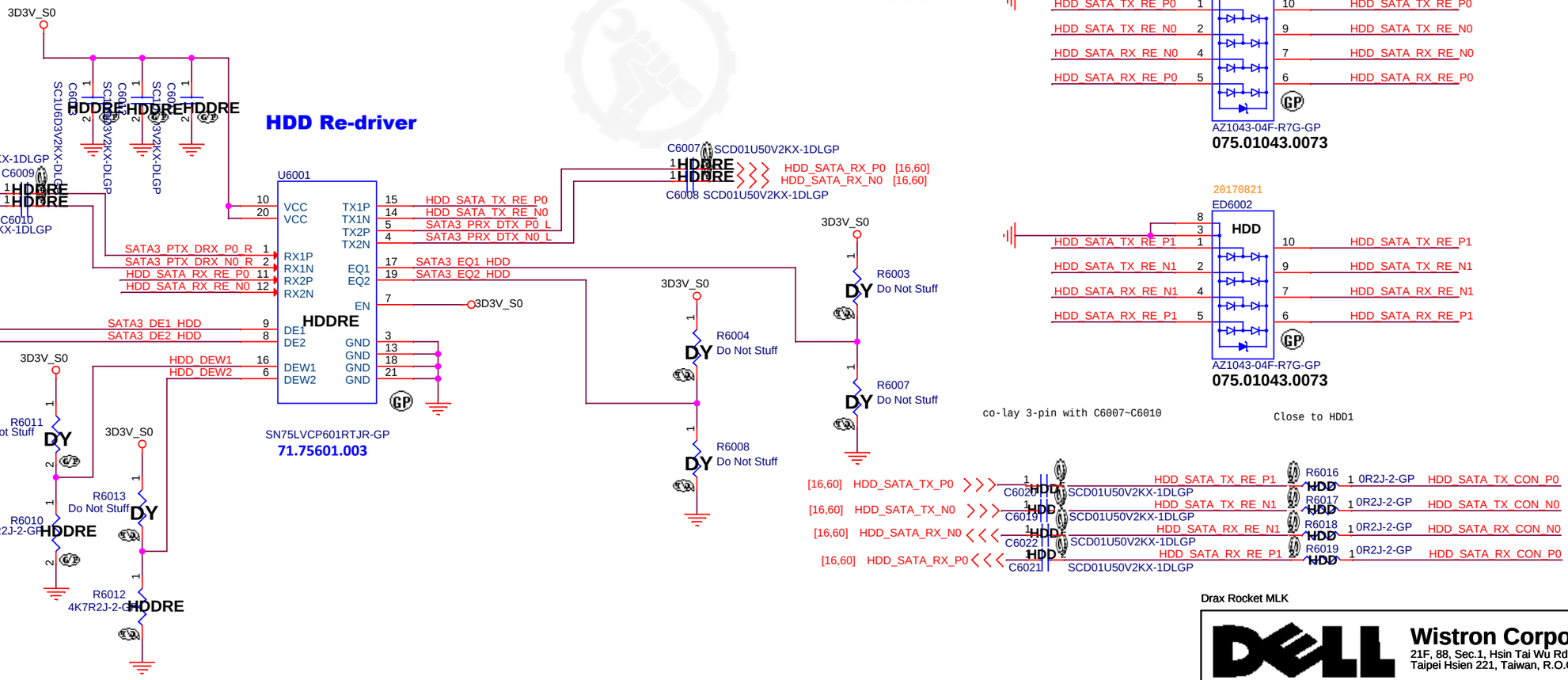
SATA HDD Connector



Layout Note :
AC coupling Cap;
place near CONN(<100mils)







Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD**

Size	Document Number	Rev
	Drax MLK/Rocket MLK AMD	A00

Date: Tuesday, January 02, 2018 Sheet 60 of 109

SSID = WLAN

Mini Card Connector(802.11a/b/g)

3D3V_S0 — R6105 (1–2) — 3D3V_WLAN_S0

Do Not Stuff

A00-20171208

3D3V_WLAN_S0 — R6111 10KR2J-3-GP

3D3V_WLAN_S0 — R6112 10KR2J-3-GP

[24] BLUETOOTH_EN — R6110 1 DY 2 — Do Not Stuff BLUETOOTH_EN_R

[24] WIFI_RF_EN — R6113 1 DY 2 — Do Not Stuff WIFI_RF_EN_R

A00-20171208

1.1A

3D3V_WLAN_S0 — C6102 SCD1U16V2KX-3DLGP — C6103 SC10U6D3V3MX-DL-GP — C6104 SCD1U16V2KX-3DLGP

BT_USB20_CON_P5 — EL6101 FILTER-4P-156-GP-U — BT_USB20_P5 [16]

068.24900.2001

BT_USB20_CON_N5 — BT_USB20_N5 [16]

Remove 0 ohm co-lay

A00-20171129

Do Not Stuff — TP6101 — E51_RX2

[17,63,73] PLT_RST# — WIFI_RF_EN_R — BLUETOOTH_EN_R

Do Not Stuff — TP6102 — E51_RX1 — E51_TX1

3D3V_WLAN_S0

WLAN1

NP2		NP1	
76	76	77	77
74	3_3V	75	GND
72	3_3V	73	REFCLKN1
70	PEWAKE1#_0/3_3V	71	REFCLKP1
68	CLKREQ1#_0/3_3V	69	GND
66	PERST1#_0/3_3V	67	PETN1
64	RESERVED#64	65	PETP1
62	ALERT_0/3_3	63	GND
60	I2C_CLK_0/3_3	61	PERN1
58	I2C_DATA_0/3_3	59	PERP1
56	W_DISABLE#1_0/3_3V	57	GND
54	RESERVED/W_DISABLE#2_0/3_3V	55	PEWAKE0#_0/3_3V
52	PERST0#_0/3_3V	53	CLKREQ0#_0/3_3V
50	SUSCLK/32KHZ_0/3_3V	51	GND
48	COEX1_0/1_8V	49	REFCLKN0
46	COEX2_0/1_8V	47	REFCLKP0
44	COEX3_0/1_8V	45	GND
42	CLINK_CLK	43	PETN0
40	CLINK_DATA	41	PETP0
38	CLINK_RESET	39	GND
36	GND	37	PERN0
34	DP_ML0P	35	PERP0
32	DP_ML0N	33	GND
30	GND	31	DP_HPD_0/3_3V
28	DP_ML1P	29	GND
26	DP_ML1N	27	DP_ML2P
24	GND	25	DP_ML2N
22	DP_AUXP	23	GND
20	DP_AUXN	21	DP_ML3P
18	GND	19	DP_ML3N
16	LED#2	17	DF_MLDIR
6	LED#1	7	GND
4	3_3V	5	USB_D-
2	3_3V	3	USB_D+
		1	GND

NC — DP_ML0P

NC — DP_ML3P / DP_ML3N / DF_MLDIR

Module Key

NGFF_KEY_A 75P

SKT-NGFF75P-47-GP

062.10003.0141

WLAN_CLKREQ_CPU_N3 [17]

WLAN_CLK_CPU_N3 [16]

WLAN_CLK_CPU_P3 [16]

WLANTX_N3 R6104 1 — 2 Do Not Stuff — WLAN_PCIE_RX_N3 [3]

WLANTX_P3 R6101 1 — 2 Do Not Stuff — WLAN_PCIE_RX_P3 [3]

A00-20171208

WLAN_PCIE_TX_CON_N3 [3]

WLAN_PCIE_TX_CON_P3 [3]

BT_USB20_CON_N5

BT_USB20_CON_P5

Reserved for NGFF Debug Card

3D3V_S5 — R6106 1 DY 2 — 3D3V_WLAN_S0

Do Not Stuff

[24] E51_TXD — R6107 1 DY 2 — Do Not Stuff — E51_TX1

[17] SER_TXD — R6108 1 DY 2 — Do Not Stuff

[17] SER_RXD — R6109 1 DY 2 — Do Not Stuff — E51_RX1

EE Note:
For NFGG Debug Card:
Stuff R6106,R6107,R6108(optional).
DY R6105

3D3V_WLAN_S0	1	AFTP6101
WLAN_CLKREQ_CPU_N3	1	AFTP6102
WIFI_RF_EN	1	AFTP6104
PLT_RST#	1	AFTP6105
BLUETOOTH_EN	1	AFTP6110
BT_USB20_CON_N5	1	AFTP6111
BT_USB20_CON_P5	1	AFTP6113

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WLAN***

Size | Document Number: ***Drax MLK/Rocket MLK AMD*** | Rev: ***A00***

Date: Tuesday, January 02, 2018 | Sheet 61 of 109

SSID = WWAN

Blanking

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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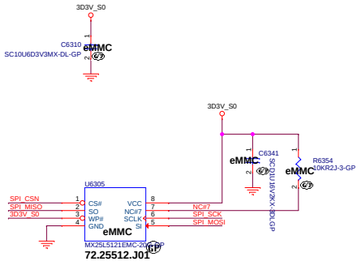
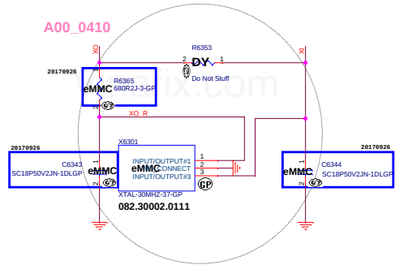
Title: *(Reserved) WWAN*

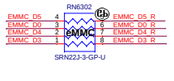
Size | Document Number: *Drax MLK/Rocket MLK AMD* | Rev: *A00*

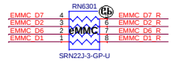
Date: Tuesday, January 02, 2018 | Sheet 62 of 109

SSID = SSD-NGFF



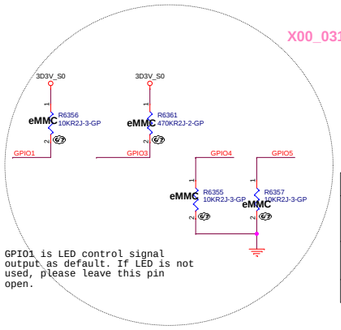






GPIO Setting

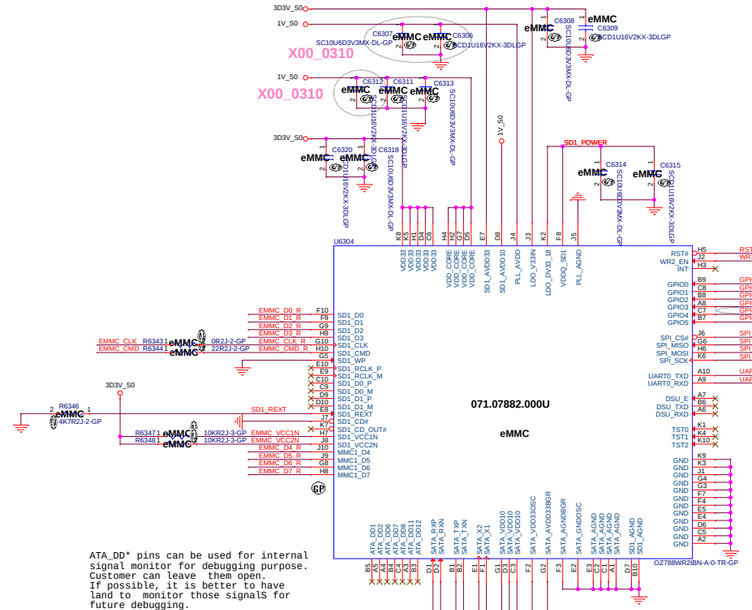
GPIO0 can be used as GPIO. And default is input mode, please clump this pin to GND or P3V3 to avoid input floating condition if customer doesn't use this pin.

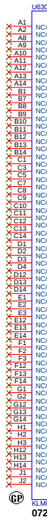


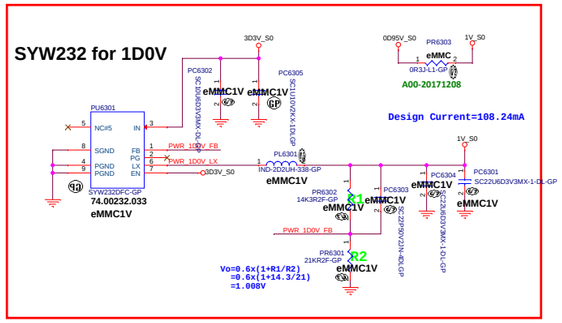
GPIO1 is LED control signal output as default. If LED is not used, please leave this pin open.

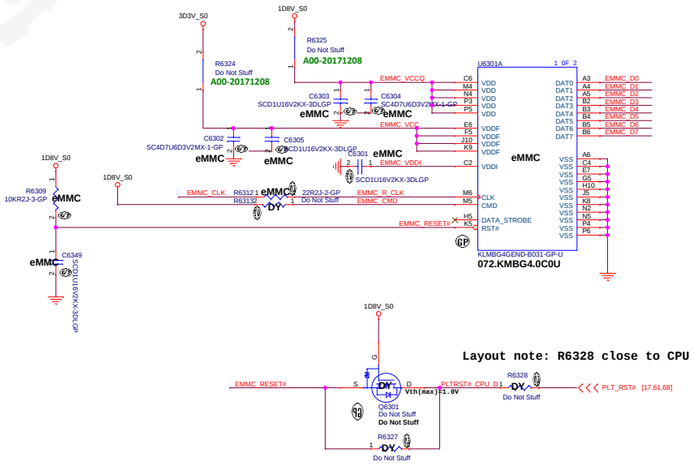
GPIO : 2013.08.19
0 : Lo (for input mode)
2 : Lo (for input mode)
3 : Hi = FW skip 10s time out
4 : Hi = 50MHz CPU clock
5 : Lo = 24bit (Which Flash?)

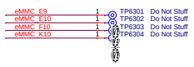
	Pull-down	Pull-up
GPIO3	FW will wait init done bit set or 10s time out	FW skip 10s time out
GPIO4	100MHz CPU clock frequency	50MHz CPU clock frequency
GPIO5	SPI 24bit Mode	SPI 16bit Mode











	SKU1		SKU1.1		SKU2		SKU3	
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 4c FCBGA 1.6GHz 6W , GT 12EU, CELERON QS QJ4T	071.00BSW.0C0U	BRASWELL 4c FCBGA 1.6GHz 6W, GT 16EU, PENTIUM QS QJ4S	071.00BSW.0B0U
eMMC	Hynix/32G	J6PD1	Hynix/32G	J6PD1	SanDisk/32G	4P0WC	Samsung/32G	N8DV6

	SKU7		SKU8		SKU9	
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 4c FCBGA 1.6GHz 6W , GT 12EU, CELERON QS QJ4T	071.00BSW.0C0U
eMMC	Hynix/64G	WF56J	SanDisk/64G	7F7DJ	Samsung/64G	67D71

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: eMMC

Size	Document Number	Rev
A1	Drax MLK/Rocket MLK AMD	A00

Date: Tuesday, January 02, 2018 Sheet 63 of 109

SSID = LED / PWRBTN

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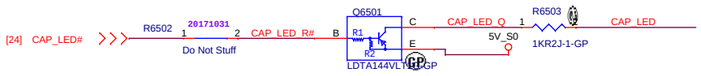
Taipei Hsien 221, Taiwan, R.O.C.

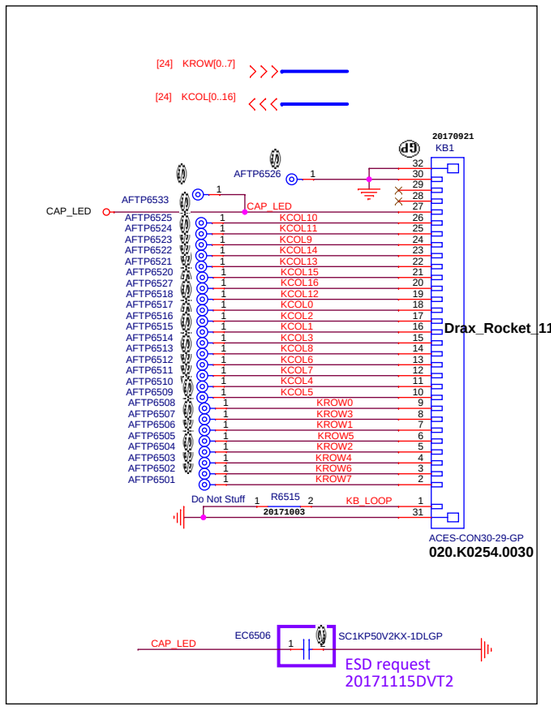
Title	***LED / PWRBTN***	
Size: A4	Document Number: ***Drax MLK/Rocket MLK AMD***	Rev: ***A00***
Date: Tuesday, January 02, 2018	Sheet 64 of 109	

SSID = KB / TOUCH PAD

CAP LED Control

LOW actived from KBC GPIO

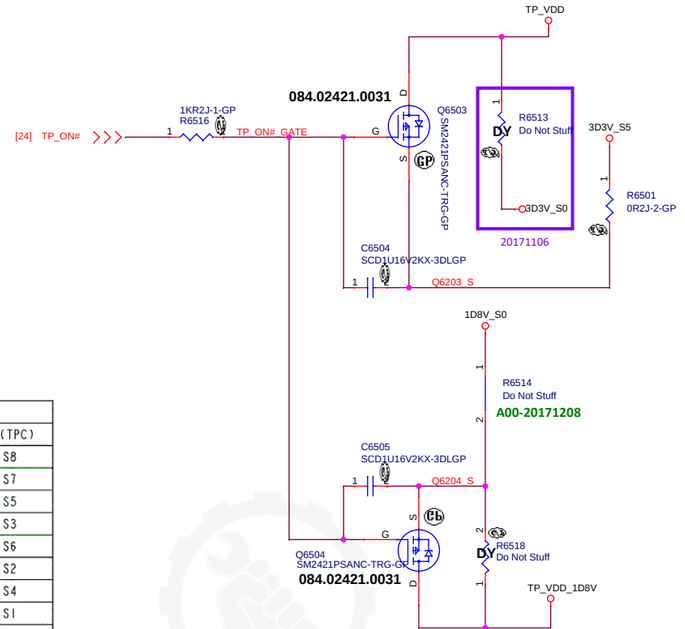


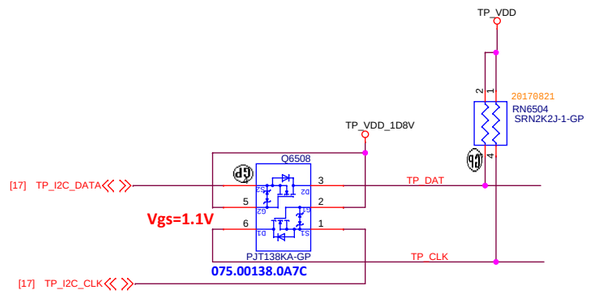


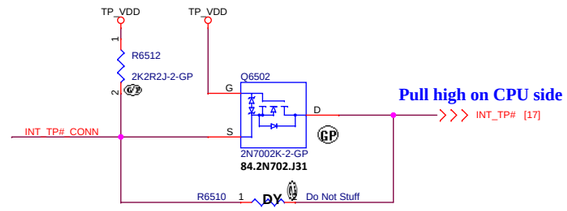
PIN#	SIGNAL
1	Diag_Loop=GPIO_1(TPC)
2	KSI [7] = KBD S8
3	KSI [6] = KBD S7
4	KSI [4] = KBD S5
5	KSI [2] = KBD S3
6	KSI [5] = KBD S6
7	KSI [1] = KBD S2
8	KSI [3] = KBD S4
9	KSI [0] = KBD S1
10	KSO [5] = KBD D6
11	KSO [4] = KBD D5
12	KSO [7] = KBD D8
13	KSO [6] = KBD D7
14	KSO [8] = KBD D9
15	KSO [3] = KBD D4
16	KSO [1] = KBD D2
17	KSO [2] = KBD D3
18	KSO [0] = KBD D1
19	KSO [12] = KBD D13
20	KSO [16] = KBD D17
21	KSO [15] = KBD D16
22	KSO [13] = KBD D14
23	KSO [14] = KBD D15
24	KSO [9] = KBD D10
25	KSO [11] = KBD D12
26	KSO [10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND

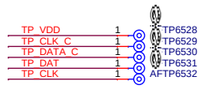
20170925

Delete KB2 Conn

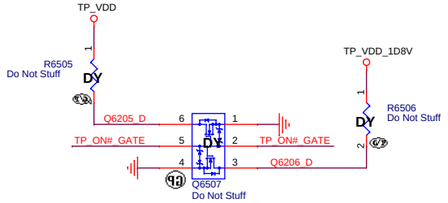


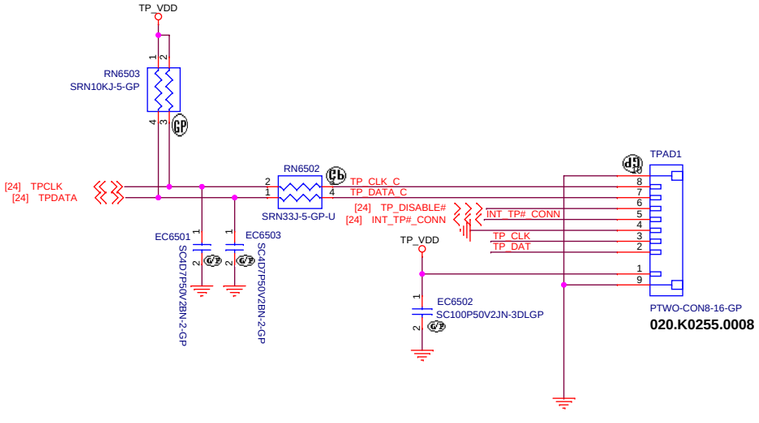


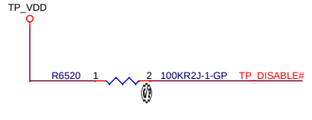




TOUCH PAD







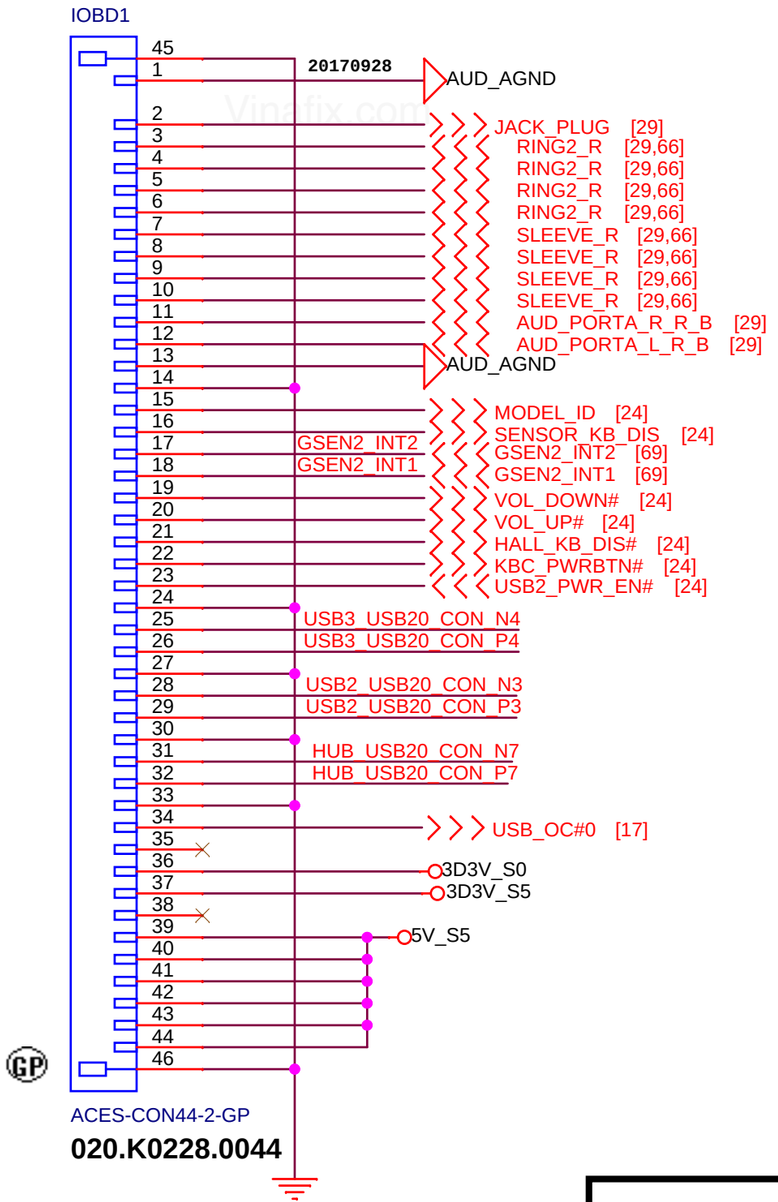
Drax Rocket MLK

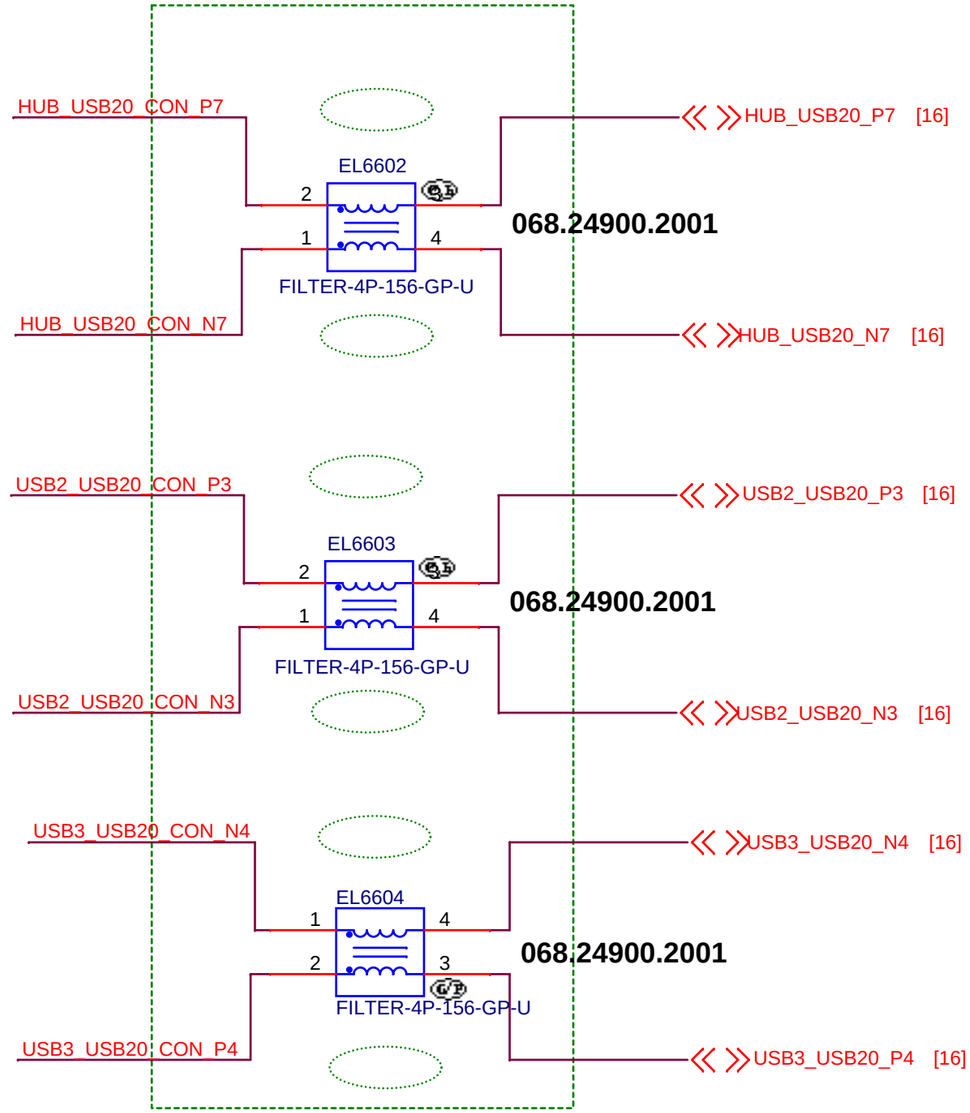
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Keyboard/Touchpad connector**

Size | Document Number: **Drax MLK/Rocket MLK AMD** | Rev: **A00**

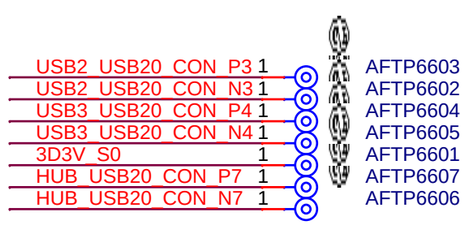
Date: Tuesday, January 02, 2018 | Sheet 65 of 109

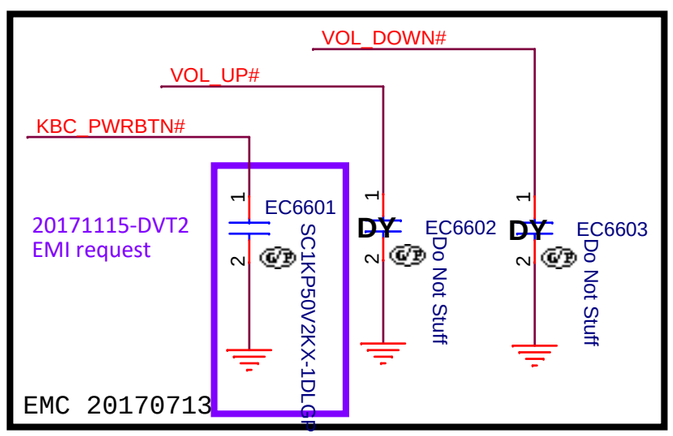




Remove 0 ohm co-lay
A00-20171129

Power Pin Count : 8
GND Pin Count : 8





Drax Rocket MLK

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board CONN***

Size	Document Number	Rev
A4	**Drax MLK/Rocket MLK AMD**	**A00**

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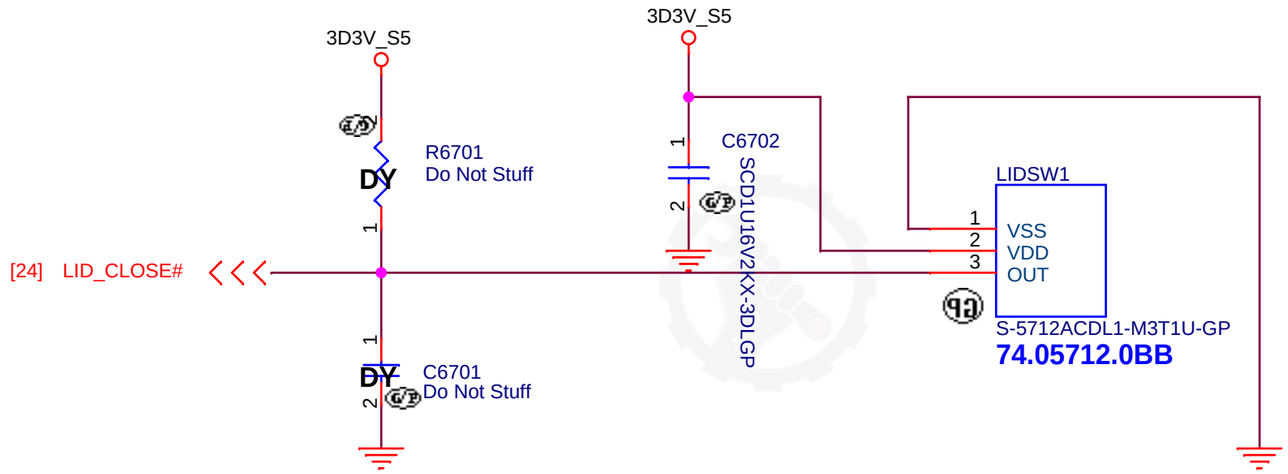

Drax Rocket MLK

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

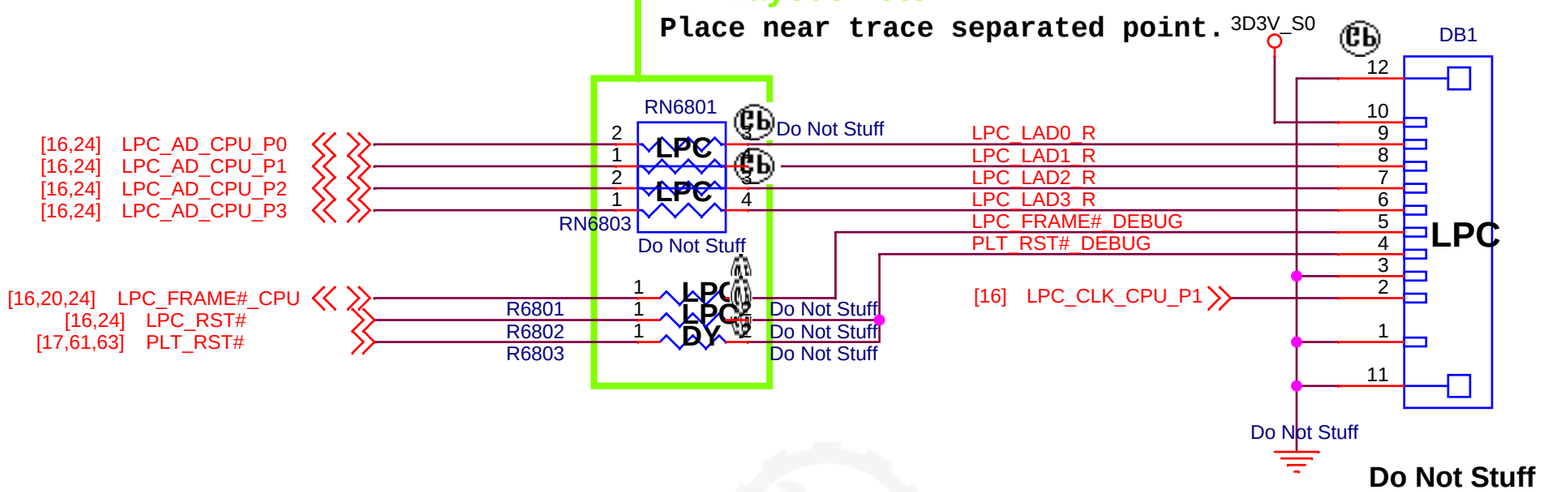
Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

Date: Tuesday, January 02, 2018 Sheet 67 of 109

SSID = DEBUG PORT

Debug Connector

Layout Note:
Place near trace separated point.

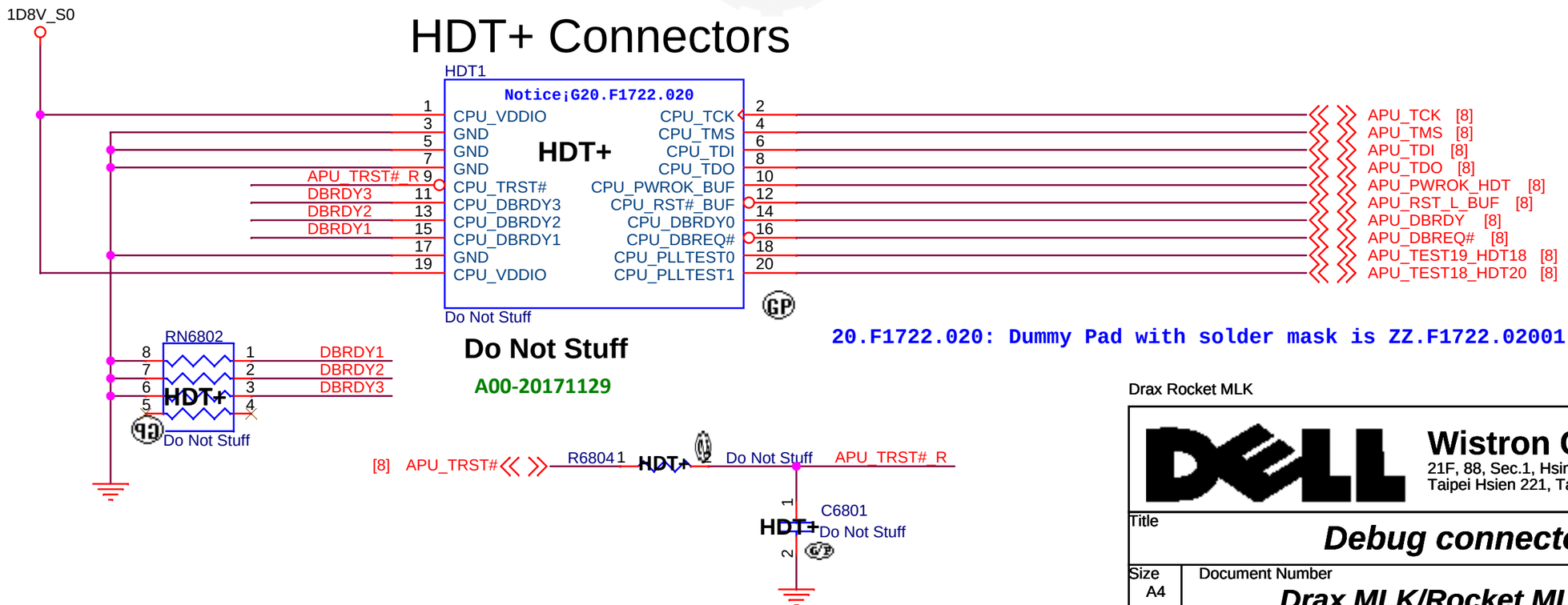


Do Not Stuff

A00-20171129

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.
20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

HDT+ Connectors



Do Not Stuff

A00-20171129

20.F1722.020: Dummy Pad with solder mask is ZZ.F1722.02001

Drax Rocket MLK

Wistron Corporation
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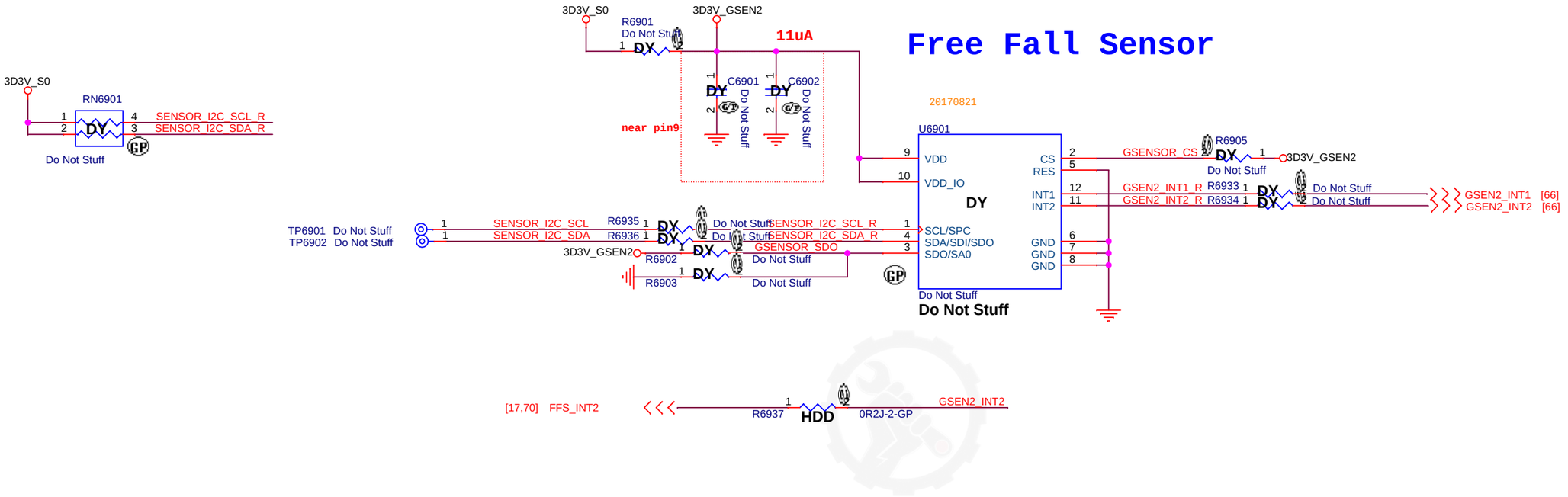
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Debug connector*		
Size: A4	Document Number: *Drax MLK/Rocket MLK AMD*	Rev: *A00*
Date: Tuesday, January 02, 2018	Sheet 68 of 106	

SSID = Sensor

Free Fall Sensor

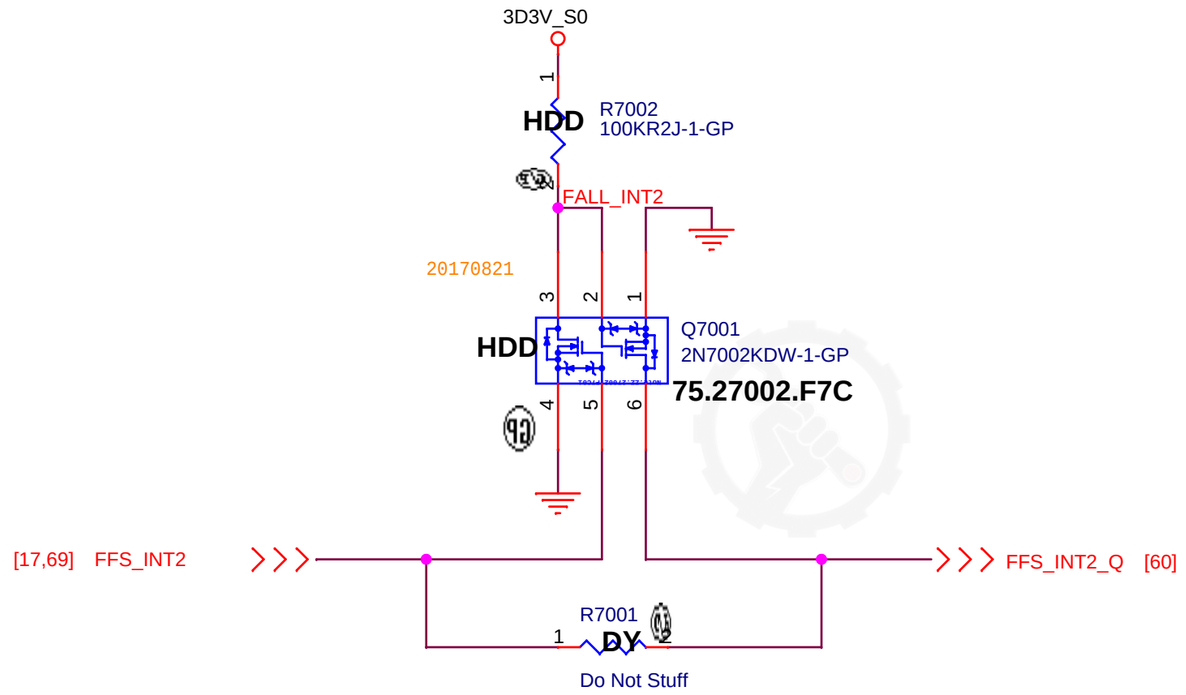


Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***FFS Sensor***	
Size: A3	Document Number: ***Drax MLK/Rocket MLK AMD***	Rev: ***A00***
Date: Tuesday, January 02, 2018	Sheet 69 of 109	

SSID = Free Fall Sensor



Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*		
Size: A4	Document Number: *Drax MLK/Rocket MLK AMD*	Rev: *A00*
Date: Tuesday, January 02, 2018	Sheet 70 of 109	

Blanking

Drax Rocket MLK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (1/5)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Blanking

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Title: *(Reserved)Thunderbolt (2/5)*		
Size: A4	Document Number: *Drax MLK/Rocket MLK AMD*	Rev: *A00*
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Title: *(Reserved)Thunderbolt (3/5)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Title: *(Reserved)Thunderbolt (4/5)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Title: *(Reserved)Thunderbolt (5/5)*		
Size: A4	Document Number: *Drax MLK/Rocket MLK AMD*	Rev: *A00*
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Title: *(Reserved)GPU (1/5) PEG*		
Size: A4	Document Number: *Drax MLK/Rocket MLK AMD*	Rev: *A00*
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Title	***(Reserved)GPU (2/5) DIGITAL***	
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Title	***(Reserved)GPU (3/5) VRAM***	
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Title: *(Reserved)GPU (4/5) GPIO*

Size	Document Number	Rev
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Title: *(Reserved)GPU (5/5) PWR/GND*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Title	***(Reserved)VRAM1,2 (1/4)***	
Size: A4	Document Number: ***Drax MLK/Rocket MLK AMD***	Rev: ***A00***
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Title: *(Reserved)VRAM3,4 (2/4)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Title: *(Reserved)VRAM5,6 (3/4)*

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Title: *(Reserved)VRAM7,8 (4/4)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Title: ***(Reserved)VGA_CORE***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

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Title	***(Reserved)DISCRETE VGAPOWER***	
Size	Document Number ***Drax MLK/Rocket MLK AMD***	Rev ***A00***
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Title

(Reserved)

Size	Document Number	Rev
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Title: *(Reserved)*

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Main Func = UnusedParts

Do Not Stuff
H9
Do Not Stuff

Do Not Stuff
H4
Do Not Stuff

34.43E24.001
SPRING-13-GP-U
SPR1

20170925
Delete SPR8

34.4Y806.001
SPR2
SPRING-63-GP

34.34S02.002
SPRING-98-GP
SPR3

34.34S02.002
SPRING-98-GP
SPR4

34.34S02.002
SPRING-98-GP
SPR5

34.34S02.002
SPRING-98-GP
SPR6

Do Not Stuff
H14
Do Not Stuff

Do Not Stuff
H1
Do Not Stuff

Do Not Stuff
H10
Do Not Stuff

Do Not Stuff
H11
Do Not Stuff

Do Not Stuff
H12
Do Not Stuff

Do Not Stuff
H13
Do Not Stuff

Main Func = EMI & RF Capacitors

DCBATOUT
20170928
FC8901 SC18P50V2JN-1DLGP
FC8902 SC18P50V2JN-1DLGP
FC8903 SC18P50V2JN-1DLGP
FC8904 SC18P50V2JN-1DLGP
FC8905 SC18P50V2JN-1DLGP
FC8906 SC18P50V2JN-1DLGP
FC8907 SC18P50V2JN-1DLGP
FC8908 SC18P50V2JN-1DLGP
FC8909 SC18P50V2JN-1DLGP
FC8910 SC18P50V2JN-1DLGP
FC8911 SC18P50V2JN-1DLGP
FC8912 SC18P50V2JN-1DLGP
FC8913 SC18P50V2JN-1DLGP
FC8914 SC18P50V2JN-1DLGP
FC8915 SC18P50V2JN-1DLGP

3D3V_S0
20170928
FC8916 SC18P50V2JN-1DLGP
FC8917 SC18P50V2JN-1DLGP
FC8918 SC18P50V2JN-1DLGP
FC8919 SC18P50V2JN-1DLGP
FC8920 SC18P50V2JN-1DLGP

5V_S0
20170928
FC8921 SC18P50V2JN-1DLGP
FC8922 SC18P50V2JN-1DLGP
FC8923 SC18P50V2JN-1DLGP
FC8924 SC18P50V2JN-1DLGP
FC8925 SC18P50V2JN-1DLGP

0D95V_S0
20170928
FC8926 SC18P50V2JN-1DLGP
FC8927 SC18P50V2JN-1DLGP

5V_S5
DY
Do Not Stuff
EC8901

3D3V_S0
DY
Do Not Stuff
EC8902
DY
Do Not Stuff
EC8903
DY
Do Not Stuff
EC8904
DY
Do Not Stuff
EC8905

EMC 20170816

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Title	UNUSED PARTS/EMI Capacitors	
Size A4	Document Number: Drax MLK/Rocket MLK AMD	Rev A00
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Title: *(Reserved)NFC Connector*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Title: ***(Reserved) TPM***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

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Title: ***(Reserved)Finger Print***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

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Drax Rocket MLK

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Title: ***(Reserved)Express Card***

Size	Document Number	Rev
A3	***Drax MLK/Rocket MLK AMD***	***A00***

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Drax Rocket MLK

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Title: *(Reserved)Smart Card Socket*		
Size: A4	Document Number: *Drax MLK/Rocket MLK AMD*	Rev: *A00*
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Title: *(Reserved)SW GFX eDP*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Drax Rocket MLK

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Title: ***(Reserved)Bottom Docking***

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Drax MLK/Rocket MLK AMD*	*A00*

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Title: *(Reserved)*

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SSID = DEBUG PORT

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Title

CPU XDP

Size	Document Number	Rev
A4	***Drax MLK/Rocket MLK AMD***	***A00***

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Title: Table of Content

Size	Document Number	Rev
A3	Drax MLK/Rocket MLK AMD	A00

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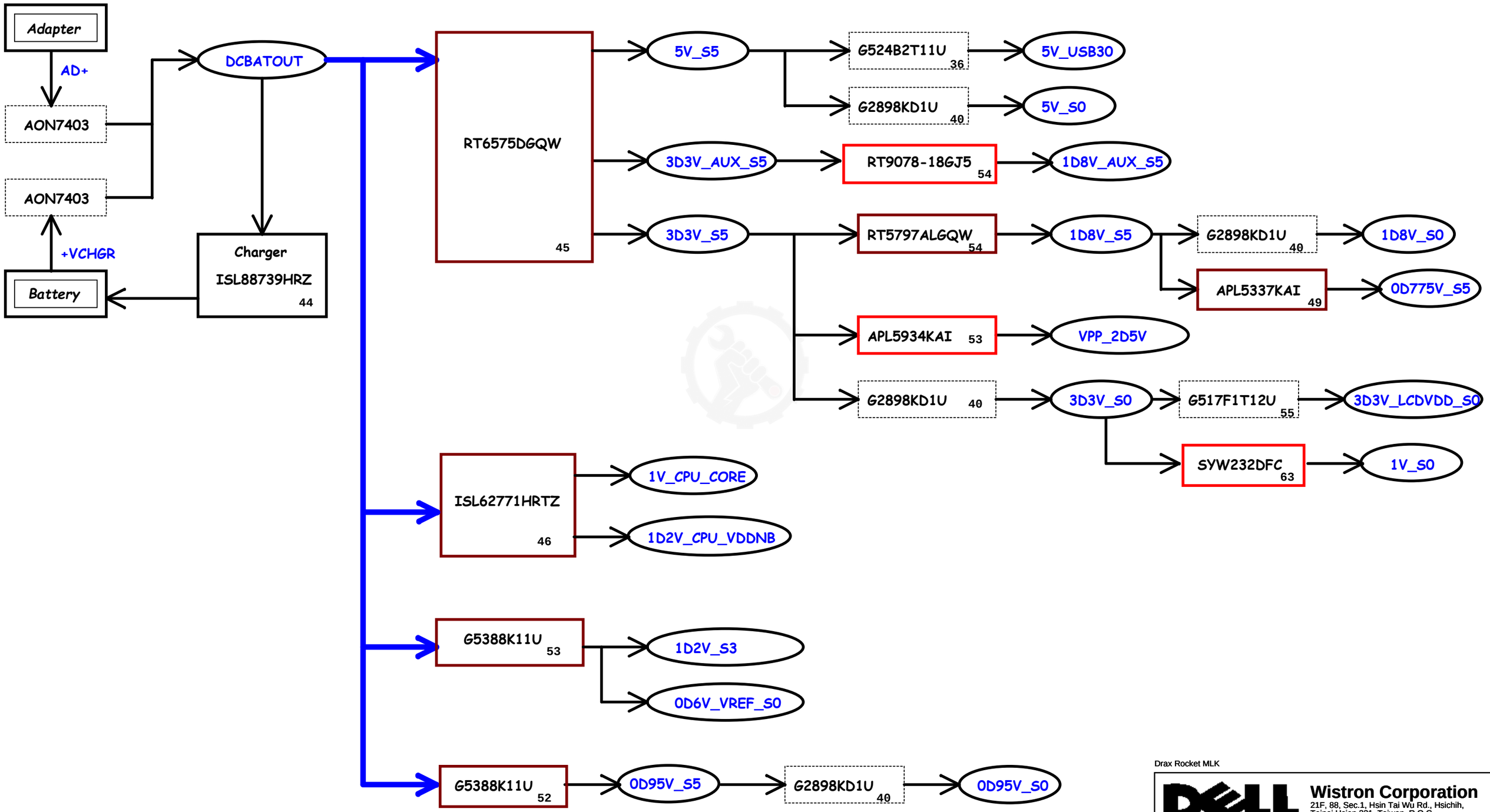
Power IC Type

Regulator | LDO | Load Switch



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Title	***Power Block Diagram***	
Size	Document Number: ***Drax MLK/Rocket MLK AMD***	Rev: ***A00***
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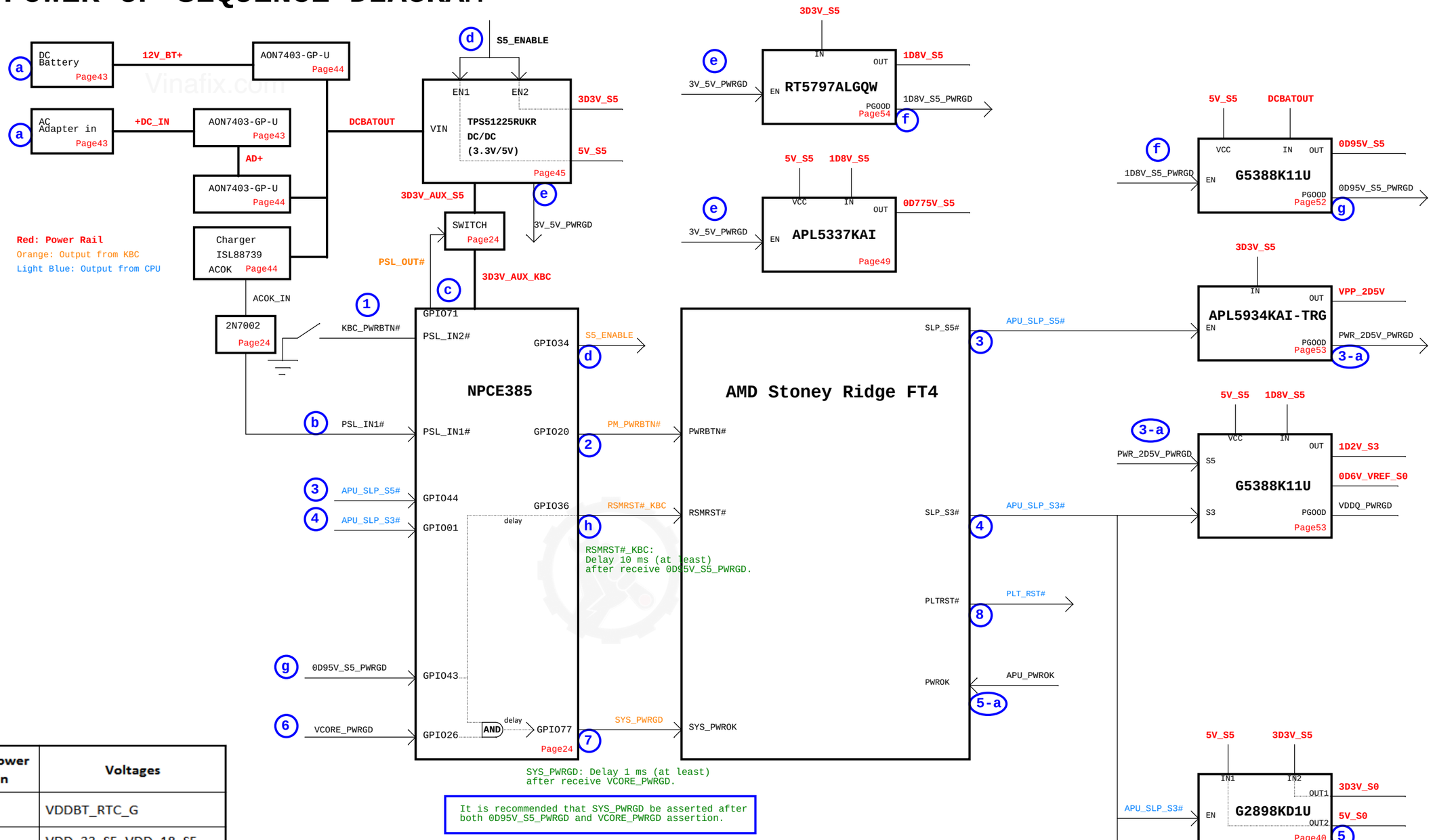
Drax STR-FT4 POWER UP SEQUENCE DIAGRAM



Red: Power Rail
Orange: Output from KBC
Light Blue: Output from CPU

Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5, VDDCR_FCH_S5
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP
Group D	S0	VDDCR_NB, VDDCR_CPU

a → b → c → d → e → f → g → h

1 → 2 → 3 → 3a → 4 → 5 → 5a → 5b → 6 → 7 → 8

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Title: Power Up Sequence

Size	Document Number	Rev
	Drax MLK/Rocket MLK AMD	A00

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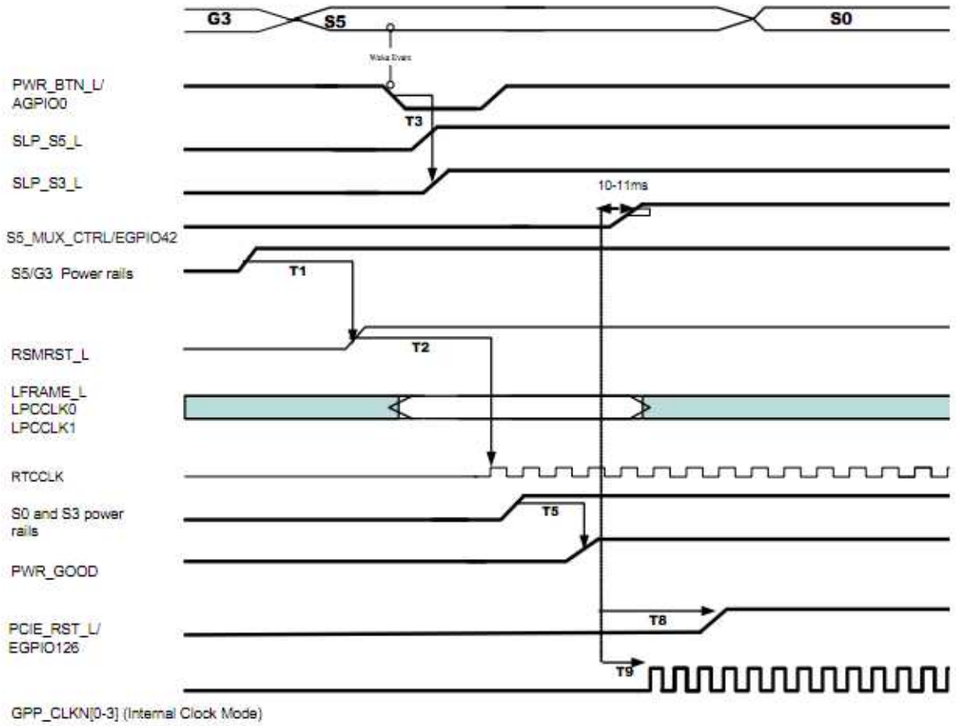

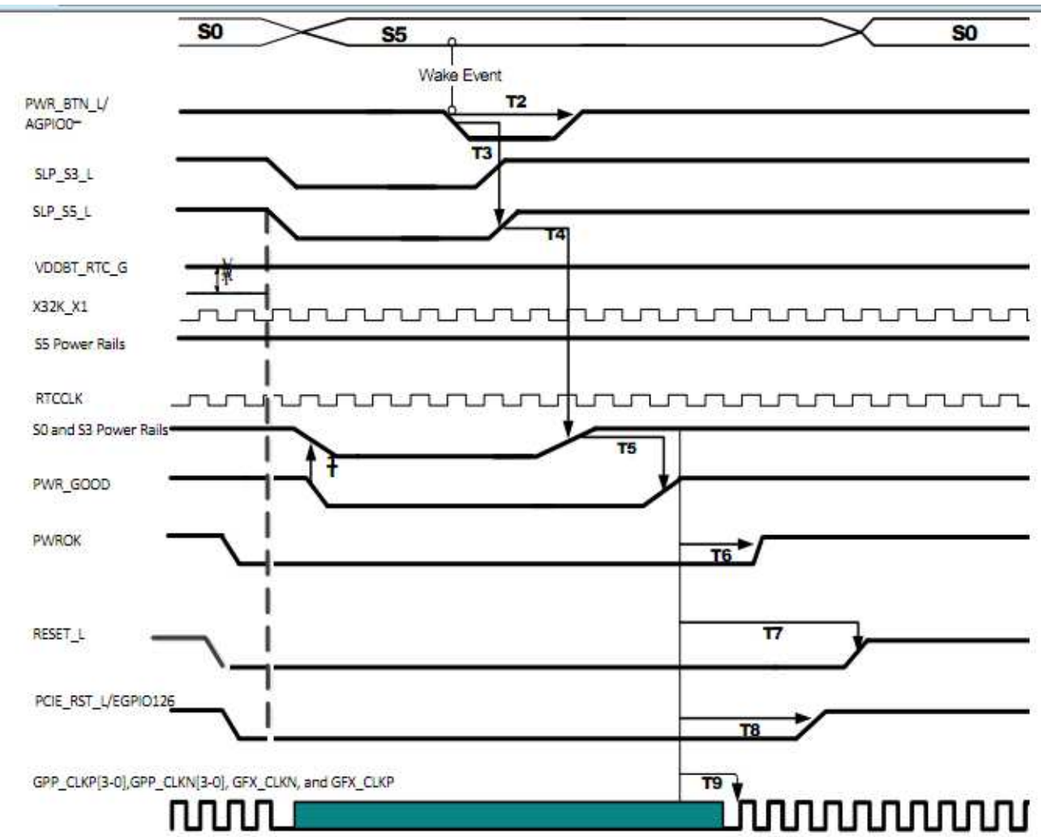

Figure 8. S0->S5->S0 Power Sequence Timing Diagram

Table 58. G3->S5->S0 Reset Sequencing Timing Parameters without coin cell battery

Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L. *This could take up to 5 seconds if power has been removed from VDDBT_RTC_G.
T2	16.5ms		15.5ms	From RSMRST_L to RTCCLK. *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L/EGPIO126 (rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3])stable.

Table 59. G3->S5->S0 Reset Sequencing Timing Parameter with coin cell battery

Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L.
T2	16.5ms			From RSMRST_L to RTCCLK. *This timing is only valid if a Schmitt trigger is used or RC time constant of 10ms is used.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising).
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L /EGPIO126(rising).
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3])stable.

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Title: ***Power Down Sequence***

Size | Document Number: ***Drax MLK/Rocket MLK AMD*** | Rev: ***A00***

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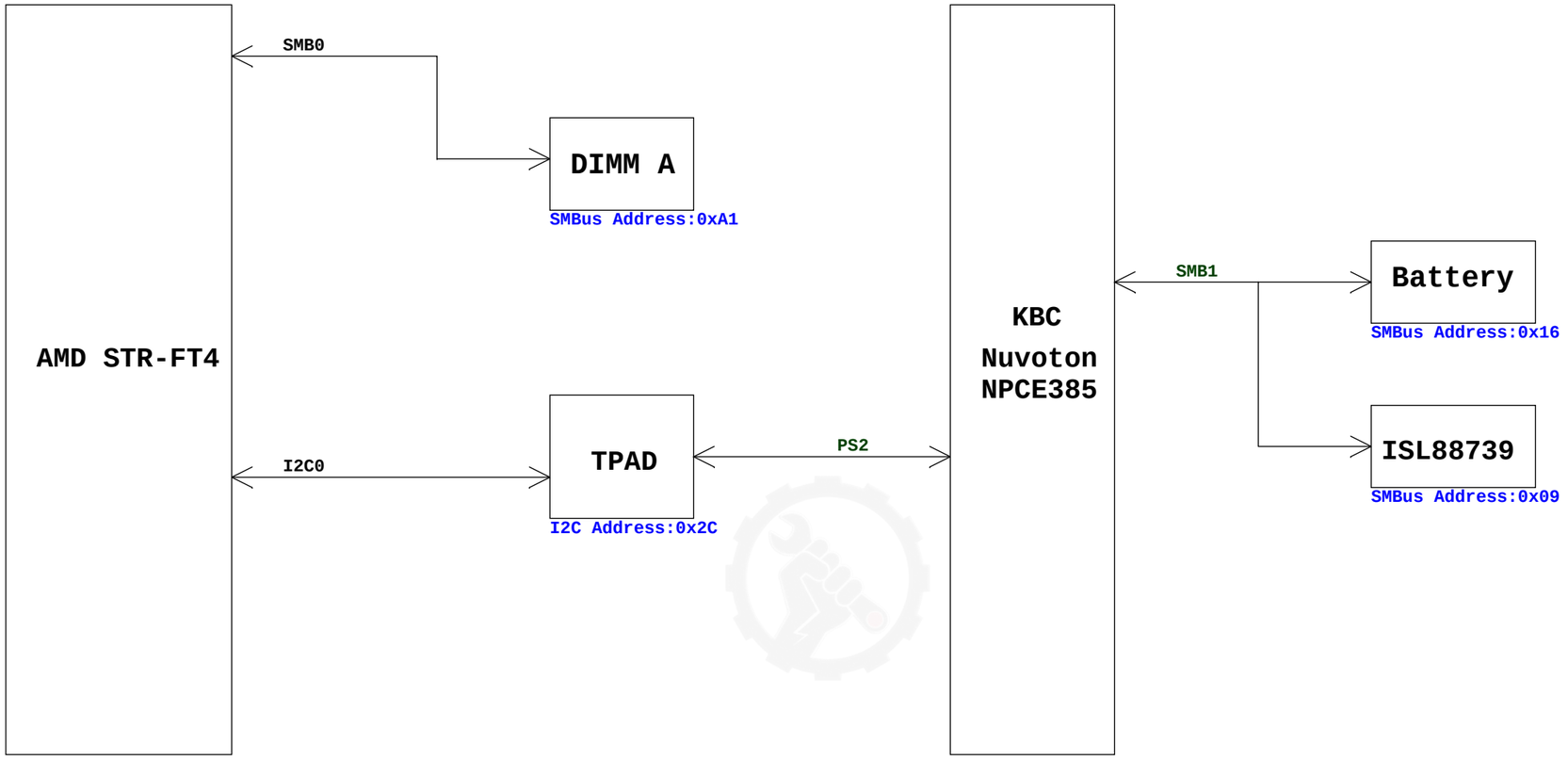

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Title: *SMBUS Block Diagram*

Size	Document Number	Rev
	Drax MLK/Rocket MLK AMD	*A00*

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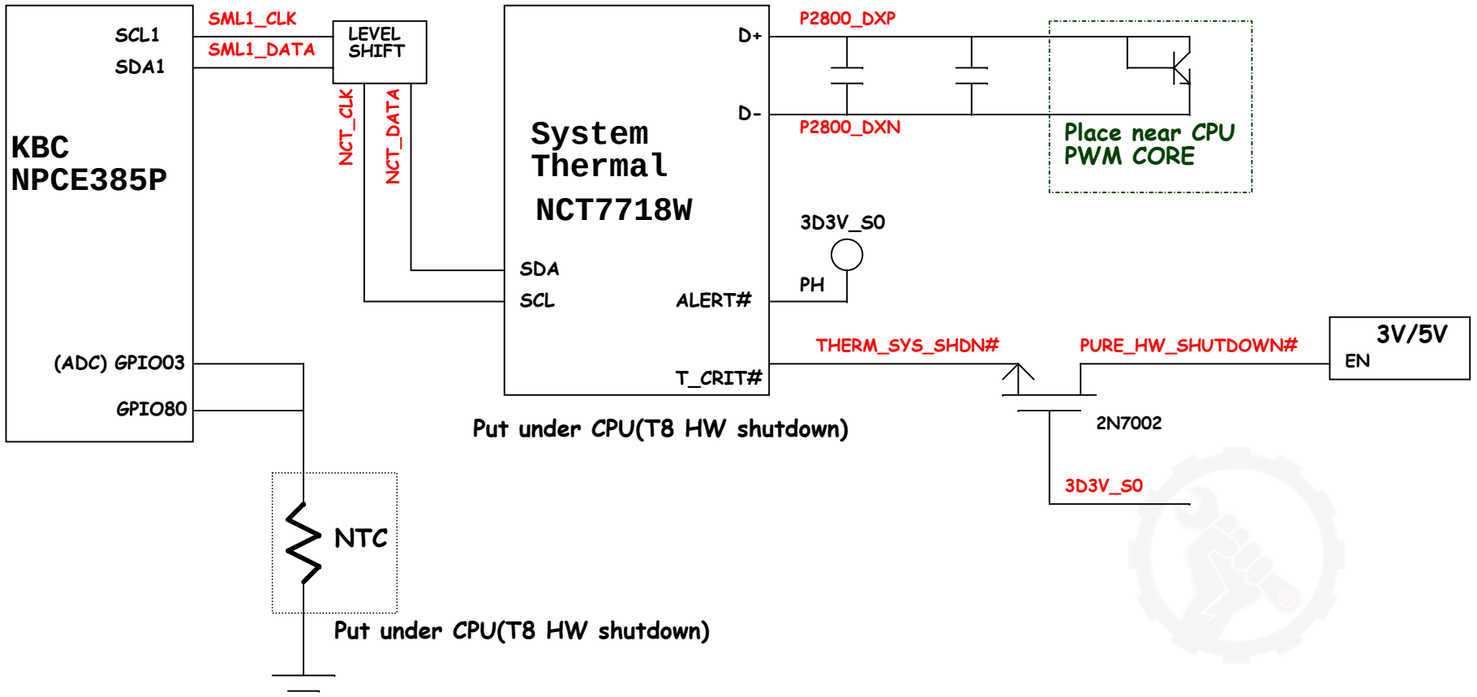
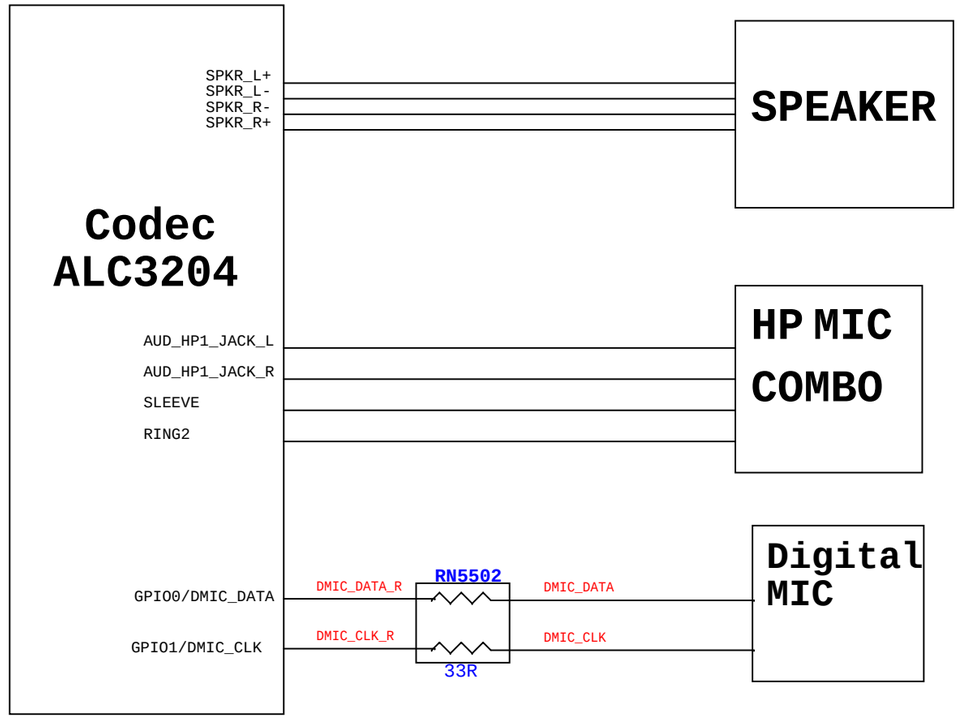
Thermal Block Diagram



Audio Block Diagram



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Title	***Thermal/Audio Block Diagram***	
Size	Document Number: ***Drax MLK/Rocket MLK AMD***	Rev: ***A00***
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Title

CLK / USB Block

Size	Document Number	Rev
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Date	Item	Change list and Desprition	Change Reasons
X01			
9/11/2017	**1**	PD4410 change to 75.00054.A7D	For common part
9/11/2017	**2**	PQ4415 change to 84.00024.A1K	For common part
9/11/2017	**3**	PQ4413 change to 84.T3906.E11	Power team request
9/11/2017	**4**	0402 0ohm change to 63.R0034.L0L (0 ohm,change to 13" tape-on-reel)	For factory need
9/20/2017	**5**	Add R2472(10Kohm) on PURE_HW_SHUTDOWN# signal	For PURE_HW_SHUTDOWN# signal
9/20/2017	**6**	R2492 change 20k to 47K	Solve 3D3V_AUX_S5 voltage drop
9/20/2017	**7**	Reserve C2448 (DY) on S5_ENABLE	Solve 3D3V_AUX_S5 voltage drop
9/20/2017	**8**	EC GPIO10 connect to LCD_TST	For panel BIST test
9/20/2017	**9**	EC GPIO50 connect to TOUCH_PANEL_EN	For panel BIST test
9/25/2017	**10**	PQ4301, Q5703 and Q5705 change to 084.00301.0031	For common part
9/25/2017	**11**	Delete SPR8, KB2, FAN1, SPK2, RTC2 connector and schematic	remove 13" colay components
9/25/2017	**12**	Q2604 (DY) and add R2476 & R2477 (0 ohm) for Thermal Sensor U2601's SMBUS	Solve CPU & thermal sensor SMBUS address conflicting problem
9/25/2017	**13**	Add TP2408, TP2409 for FAN_PWM1_C, FAN_TACH1_C	remove 13" colay components
9/25/2017	**14**	Add TP5501 for PROJECT_ID1 (For EC to check panel is 11'' or 13'')	remove 13" colay components
9/26/2017	**15**	PR4405 change to 64.16535.6DL	Power team fine tune Charger setting
9/26/2017	**16**	PR4603 change to 64.39005.6DL	Power team fine tune CPU PWR setting
9/26/2017	**17**	C1601, C1602 change to 78.15034.1FLDL (15pF) for CPU's 48MHz Crystal fine tune.	Crystal vendor fine tune result
9/26/2017	**18**	C1703, C1704, C6343, C6344 change to 78.18034.1FLDL(18pF) for CPU's 32.768KHz & SATA bridge IC's 30MHz Crystal fine tune.	Crystal vendor fine tune result
9/26/2017	**19**	R6365 change to 63.68134.1DL (680ohm) for SATA bridge IC's 30MHz Crystal fine tune.	Crystal vendor fine tune result
9/27/2017	**20**	Q2501 change to 75.00054.A7D	For common part
9/27/2017	**21**	Add R6110 for BLUETOOTH_EN signal, reserve R2478 and R6111 PU high 3.3V	Reserve Bluetooth control method.
9/28/2017	**22**	FC8901~FC8927 change BOM to 78.18034.1FLDL (18pF) for RF solution	RF solution
9/28/2017	**23**	R2499 (DY) , D2403 (DY) unused for fanless system (design for 13'')	Mark components are deisgned for 13".
9/28/2017	**24**	Re-arrage IO board pin definition, add one pin RING2_R and one pin SLEEVE_R to improve audio performance test.	For Audio performance test result, vendor debug solution
10/2/2017	**25**	Reserve Q2506(084.02421.0031), Q2507(84.2N702.J31), R2516(63.10434.1DL), R2517(63.R0034.1DL), R2515 (0 ohm) for BIOS SPI ROM power supply optional solution.	Reserve BIOS SPI ROM's power opional solution for backup only.
10/2/2017	**26**	EC GPIO14 connect to INT_TP#_CONN	Solve TP wake up problem

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Title: ***Change History-01***

Size | Document Number: ***Drax MLK/Rocket MLK AMD*** | Rev: ***A00***

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Date	Item	Change list and Desprition	Change Reasons
X02			
10/30/2017	1	R2437 Change to 33k	PCB version up to DVT2
10/31/2017	2	0 ohm change to short pad (94 pcs) for factory SMT request.	Factory SMT request
11/3/2017	3	EC6506 Change to 100pf	EMC request, enhance ESD performance
	4	SD_CD# add 1000pf (EC3301)	EMC request, enhance ESD performance
11/3/2017	5	page12. 1D2V_S3 add 2pcs 18pf cap: FC1201, FC1202	RF request , enhance RF performance
	6	page10. 3D3V_S5 add 2pcs 18pf cap: FC1001, FC1002	RF request , enhance RF performance
	7	page10. 3D3V_S0 add 1pcs 18pf cap: FC1003	RF request , enhance RF performance
	8	page24. 1D8V_AUX_S5 add 1pcs 18pf cap: FC2401	RF request , enhance RF performance

Drax Rocket MLK

Wistron Corporation
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Title ***Change History-02***

Size	Document Number	Rev
	Drax MLK/Rocket MLK AMD	***A00***

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Date	Item	Change list and Desprition	Change Reasons	Project	Category	Sub-Category	critical issues
A00							
11/29/2017	1	Page17. Remove TP1701	PSE had concern for test point location (too closed CPU). PSE agree to remove it.	Drax MLK_AMD		SMT concern	
	2	Page29. DY Q2901 C2902 R2905 Stuff R2914	improve audio jack detect time. (align schematic as Truis)	Drax MLK_AMD		Audio Jack detect	
	3	Page68. Change DB1 & HDT1 to solder mask dummy pad, and debug port circuit.	A00 do not need solder debug port.	Drax MLK_AMD		Debug port	
	4	Page24. Change R2437 to 100k	for A00 PCB VER AD	Drax MLK_AMD		PCB version	
	5	USB2.0 remove 0 ohm co-aly (remove R3501,R3502's PAD), USB3.0 remove CMC co-lay (remove EL3501's PAD . R3503,R3504 R change to shortPAD.)	A00 do not need co-lay	Drax MLK_AMD		USB EMI	
12/8/2017	6	Page16. DY FC1601	LPC CLK is for debug mode only. A00 will turn off debug mode(turn off CLK). RF test is OK.	Drax MLK_AMD		Debug port	
	7	Page60. add EC6002 22PF CAP	Reserve for EMI team	Drax MLK_AMD		EMI	
	8	Page61. R6112 R6113	WIFI/BT controlled by Driver, align with Starlord serise.	Drax MLK_AMD		WIFI/BT control	
	9	Page68. DY debug port & AMD HDT debug port circuit.	A00 DY debug solution	Drax MLK_AMD		Debug port	

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