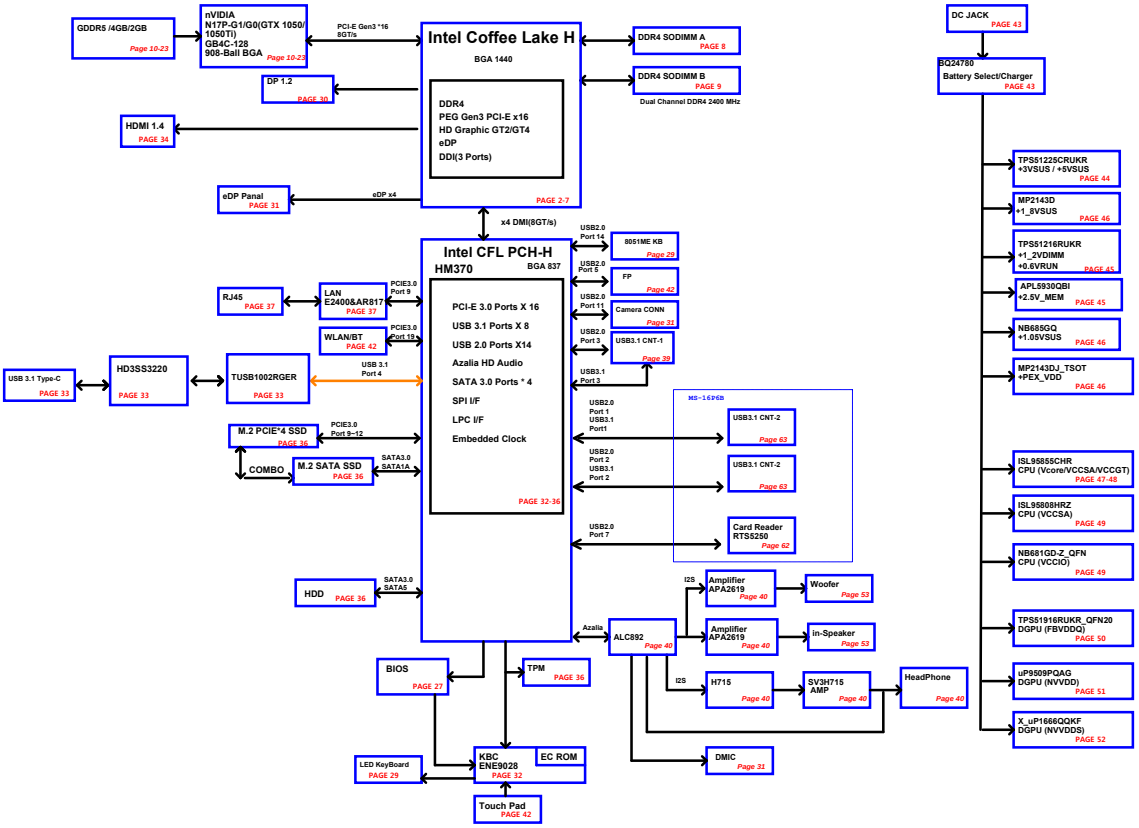
MS-16P6/MS-17C6 Ver: 10

Intel Coffee Lake platform

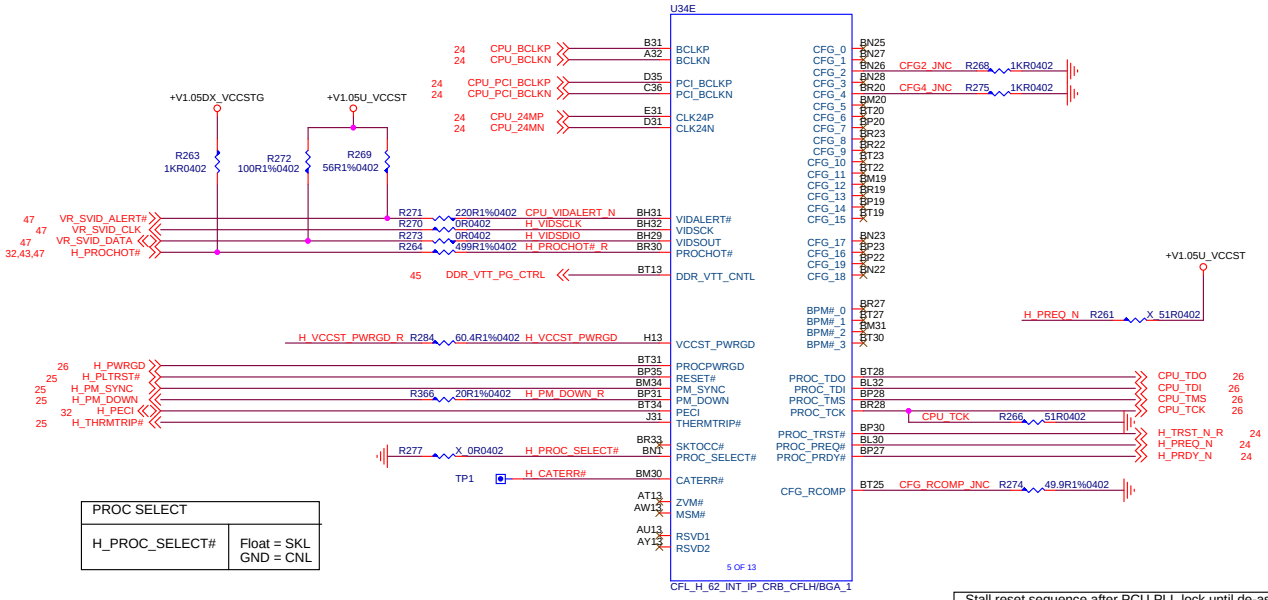


MICRO-STAR INT'L CO.,LTD.

Block Diagram

MS-16P61

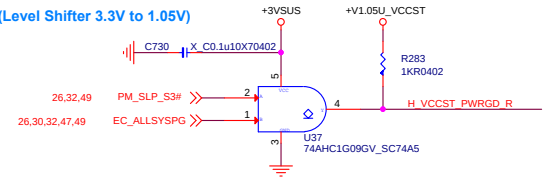
1.0



PROC SELECT	
H_PROC_SELECT#	Float = SKL GND = CNL

VCCST_PWRGD

(Level Shifter 3.3V to 1.05V)



E-2176M
OAH-16P5002-I06

i7-8750HQS
OAD-16K5004-I06

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	1 = (Default) Normal Operation; No stall 0 = Stall

PCIE Express * Static X16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*

PEG DEFER TRAINING	
CFG7	1: (default) PEG Train immediately following RESET# de assertion. 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title: **Coffeelake(HOST)**

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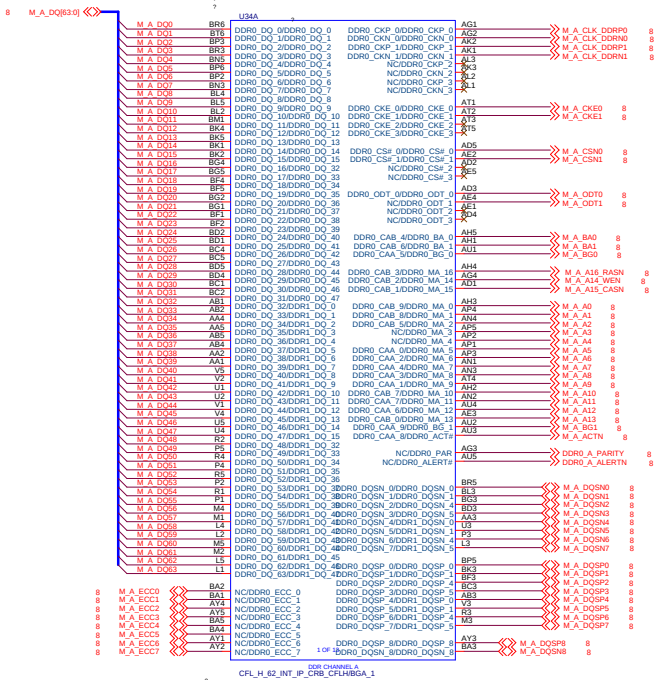
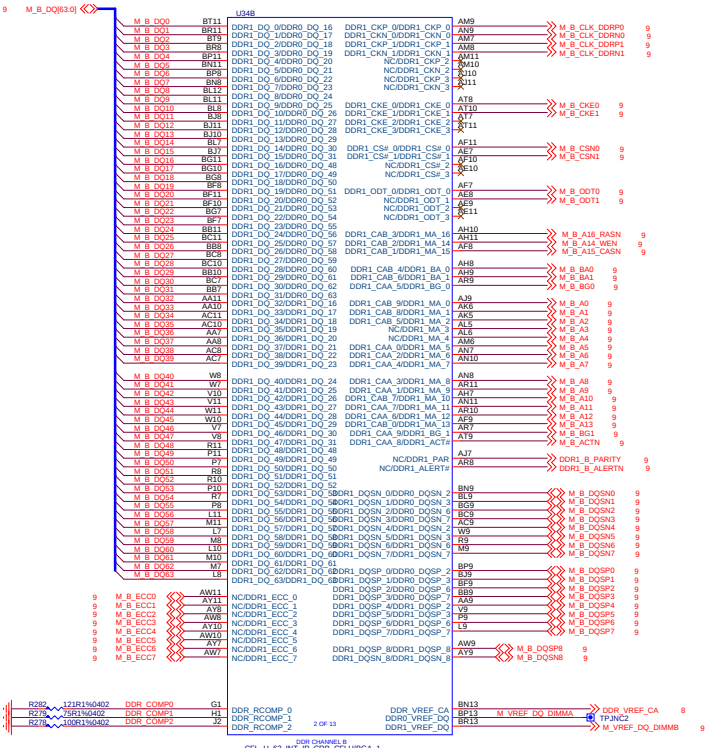
DDR Channel A



DDR Channel B



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	Coffeelake(DDR4)	
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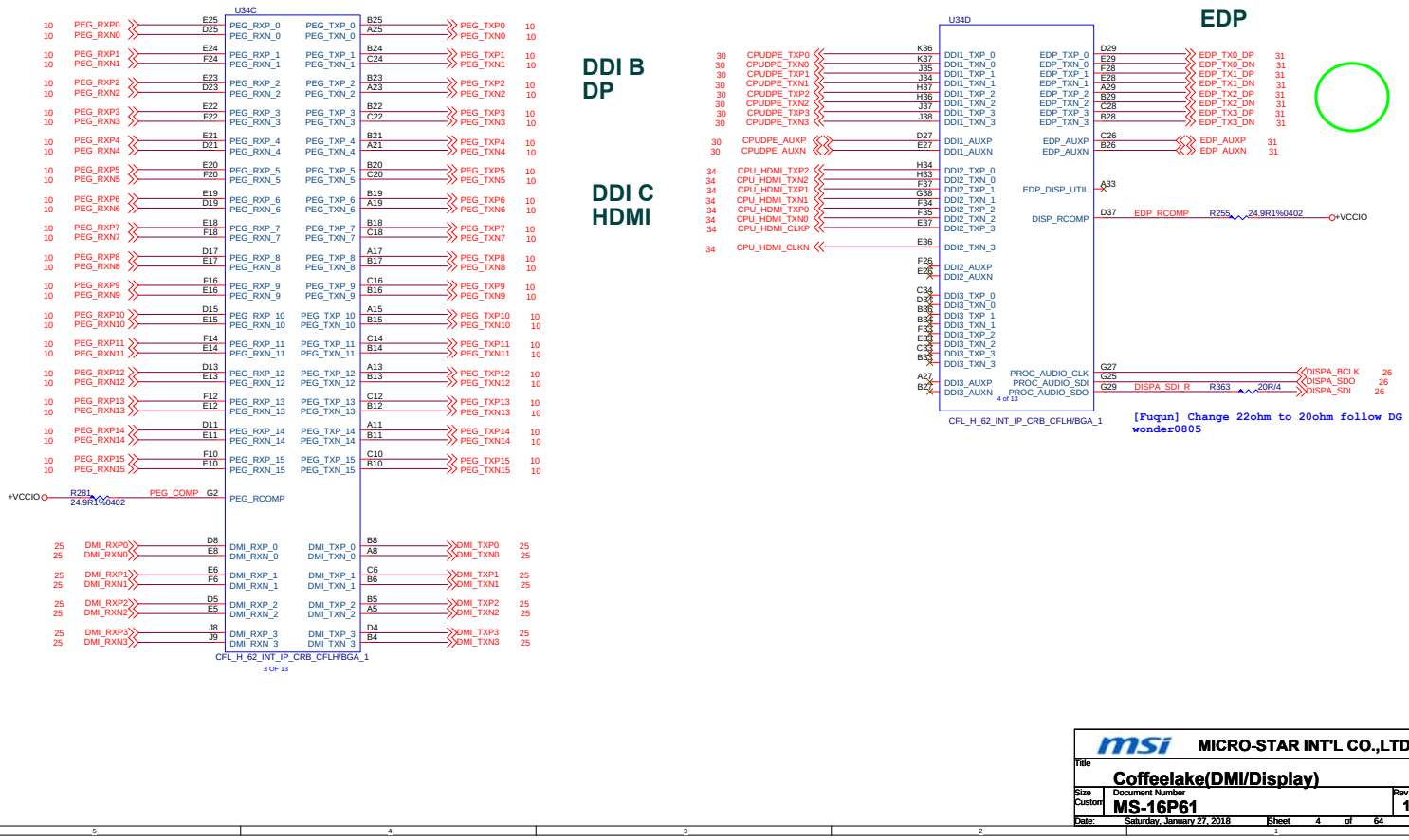

MICRO-STAR INT'L CO.,LTD.			
Title: Coffeelake(DMI/Display)			
Size: Custom	Document Number: MS-16P61		Rev: 10
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Title	Coffeelake(Power1)		
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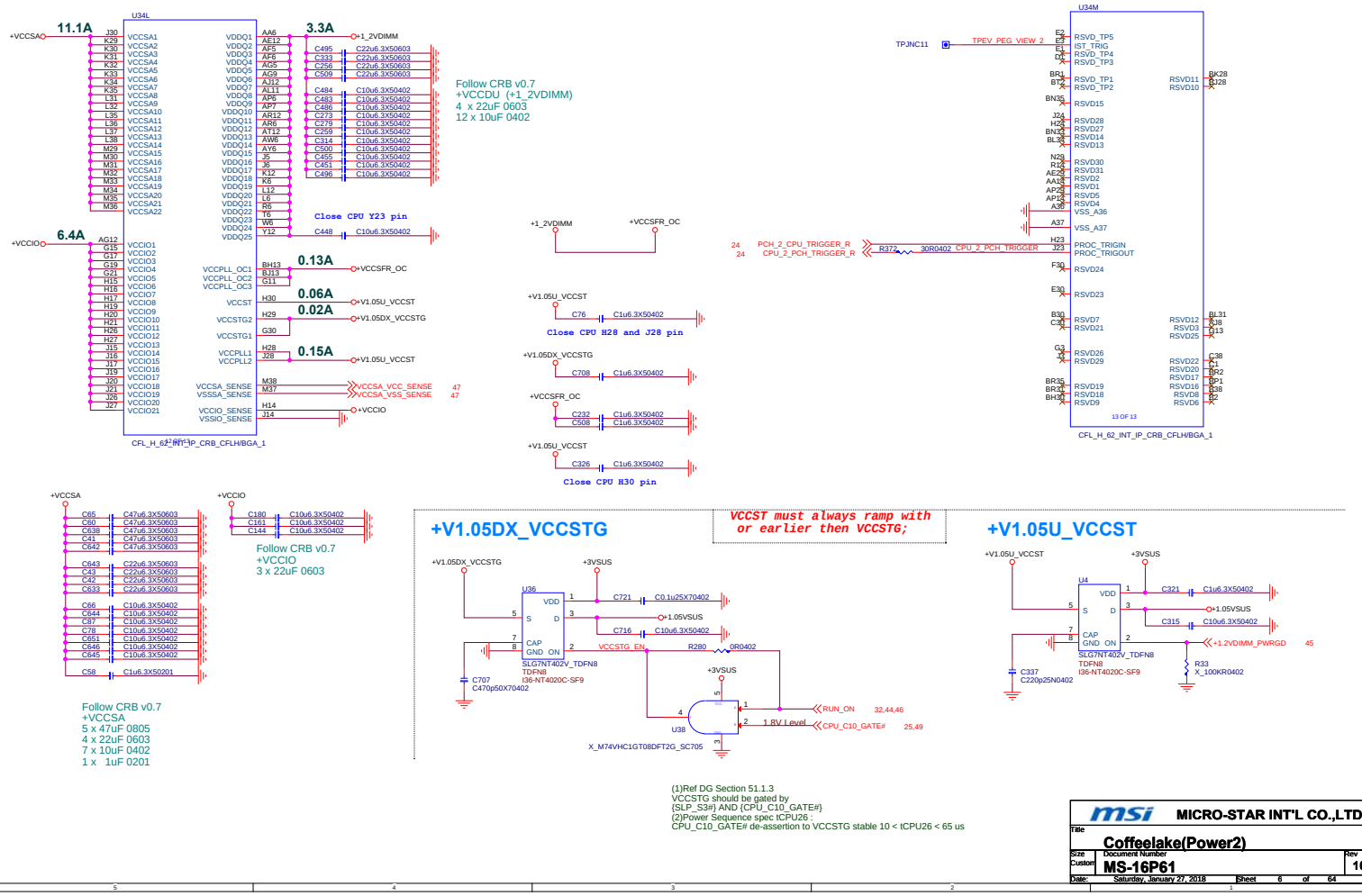
U34L
11.1A
+VCCSA
VCCSA1
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8
VCCSA9
VCCSA10
VCCSA11
VCCSA12
VCCSA13
VCCSA14
VCCSA15
VCCSA16
VCCSA17
VCCSA18
VCCSA19
VCCSA20
VCCSA21
VCCSA22
6.4A
+VCCIO
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
VCCIO9
VCCIO10
VCCIO11
VCCIO12
VCCIO13
VCCIO14
VCCIO15
VCCIO16
VCCIO17
VCCIO18
VCCIO19
VCCIO20
VCCIO21
CFL_H_62_INT_IP_CRB_CFLH/BGA_1
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDQ11
VDDQ12
VDDQ13
VDDQ14
VDDQ15
VDDQ16
VDDQ17
VDDQ18
VDDQ19
VDDQ20
VDDQ21
VDDQ22
VDDQ23
VDDQ24
VDDQ25
3.3A
+1_2VDIMM
C495 C22u6.3X50603
C333 C22u6.3X50603
C256 C22u6.3X50603
C509 C22u6.3X50603
C484 C10u6.3X50402
C483 C10u6.3X50402
C486 C10u6.3X50402
C273 C10u6.3X50402
C279 C10u6.3X50402
C259 C10u6.3X50402
C314 C10u6.3X50402
C500 C10u6.3X50402
C455 C10u6.3X50402
C451 C10u6.3X50402
C496 C10u6.3X50402
Close CPU Y23 pin
C448 C10u6.3X50402
0.13A
+VCCSFR_OC
0.06A
+V1.05U_VCCST
0.02A
+V1.05DX_VCCSTG
0.15A
+V1.05U_VCCST
VCCSA_SENSE
VSSSA_SENSE
VCCSA_VCC_SENSE 47
VCCSA_VSS_SENSE 47
VCCIO_SENSE
VSSIO_SENSE
+VCCIO
Follow CRB v0.7
+VCCDU (+1_2VDIMM)
4 x 22uF 0603
12 x 10uF 0402
+1_2VDIMM
+VCCSFR_OC
+V1.05U_VCCST
C76 C1u6.3X50402
Close CPU H28 and J28 pin
+V1.05DX_VCCSTG
C708 C1u6.3X50402
+VCCSFR_OC
C232 C1u6.3X50402
C508 C1u6.3X50402
+V1.05U_VCCST
C326 C1u6.3X50402
Close CPU H30 pin
U34M
TPJNC11
TPEV_PEG_VIEW_2
RSVD_TP5
IST_TRIG
RSVD_TP4
RSVD_TP3
RSVD_TP1
RSVD_TP2
RSVD15
RSVD28
RSVD27
RSVD14
RSVD13
RSVD30
RSVD31
RSVD2
RSVD1
RSVD5
RSVD4
VSS_A36
VSS_A37
24 PCH_2_CPU_TRIGGER_R
24 CPU_2_PCH_TRIGGER_R
R372 30R0402 CPU_2_PCH_TRIGGER
PROC_TRIGIN
PROC_TRIGOUT
RSVD24
RSVD23
RSVD7
RSVD21
RSVD26
RSVD29
RSVD22
RSVD20
RSVD17
RSVD19
RSVD18
RSVD9
RSVD11
RSVD10
RSVD12
RSVD3
RSVD25
RSVD16
RSVD8
RSVD6
13 OF 13
CFL_H_62_INT_IP_CRB_CFLH/BGA_1
+VCCSA
C65 C47u6.3X50603
C60 C47u6.3X50603
C638 C47u6.3X50603
C41 C47u6.3X50603
C642 C47u6.3X50603
C643 C22u6.3X50603
C43 C22u6.3X50603
C42 C22u6.3X50603
C633 C22u6.3X50603
C66 C10u6.3X50402
C644 C10u6.3X50402
C87 C10u6.3X50402
C78 C10u6.3X50402
C651 C10u6.3X50402
C646 C10u6.3X50402
C645 C10u6.3X50402
C58 C1u6.3X50201
Follow CRB v0.7
+VCCSA
5 x 47uF 0805
4 x 22uF 0603
7 x 10uF 0402
1 x 1uF 0201
+VCCIO
C180 C10u6.3X50402
C161 C10u6.3X50402
C144 C10u6.3X50402
Follow CRB v0.7
+VCCIO
3 x 22uF 0603
+V1.05DX_VCCSTG
VCCST must always ramp with or earlier then VCCSTG;
+V1.05U_VCCST
+V1.05DX_VCCSTG
+3VSUS
U36
VDD
S
D
CAP
GND
ON
SLG7NT402V_TDFN8
TDFN8
I36-NT4020C-SF9
C721 C0.1u25X70402
+1.05VSUS
C716 C10u6.3X50402
VCCSTG_EN
R280 0R0402
C707 C470p50X70402
U38
X_M74VHC1GT08DFT2G_SC705
RUN_ON 32,44,46
1.8V Level
CPU_C10_GATE# 25,49
+V1.05U_VCCST
+3VSUS
U4
C321 C1u6.3X50402
+1.05VSUS
C315 C10u6.3X50402
+1.2VDIMM_PWRGD 45
C337 C220p25N0402
R33 X_100KR0402
(1)Ref DG Section 51.1.3
VCCSTG should be gated by
{SLP_S3#} AND {CPU_C10_GATE#}
(2)Power Sequence spec tCPU26 :
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 65 us
MICRO-STAR INT'L CO.,LTD.
Title
Coffeelake(Power2)
Size
Custom
Document Number
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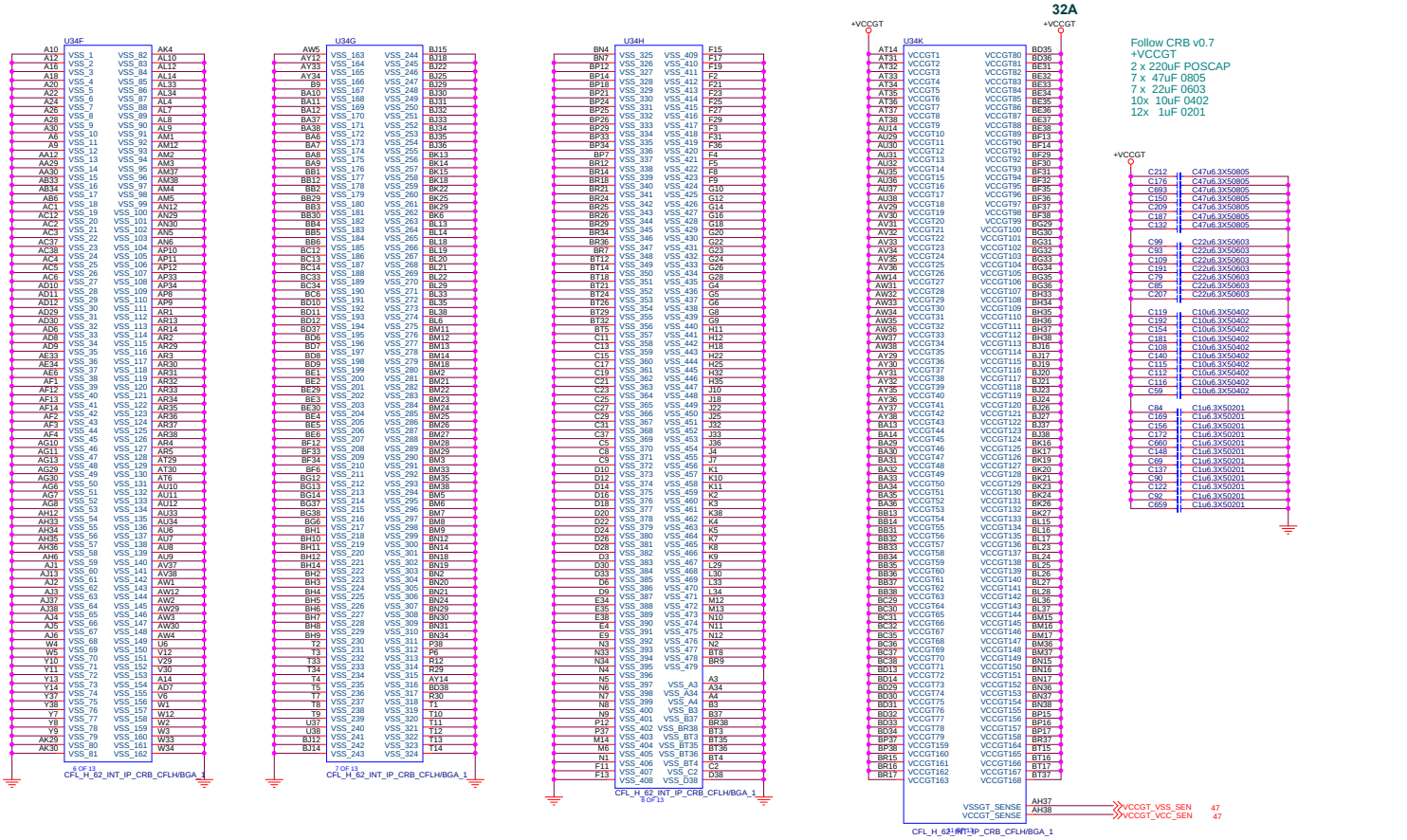

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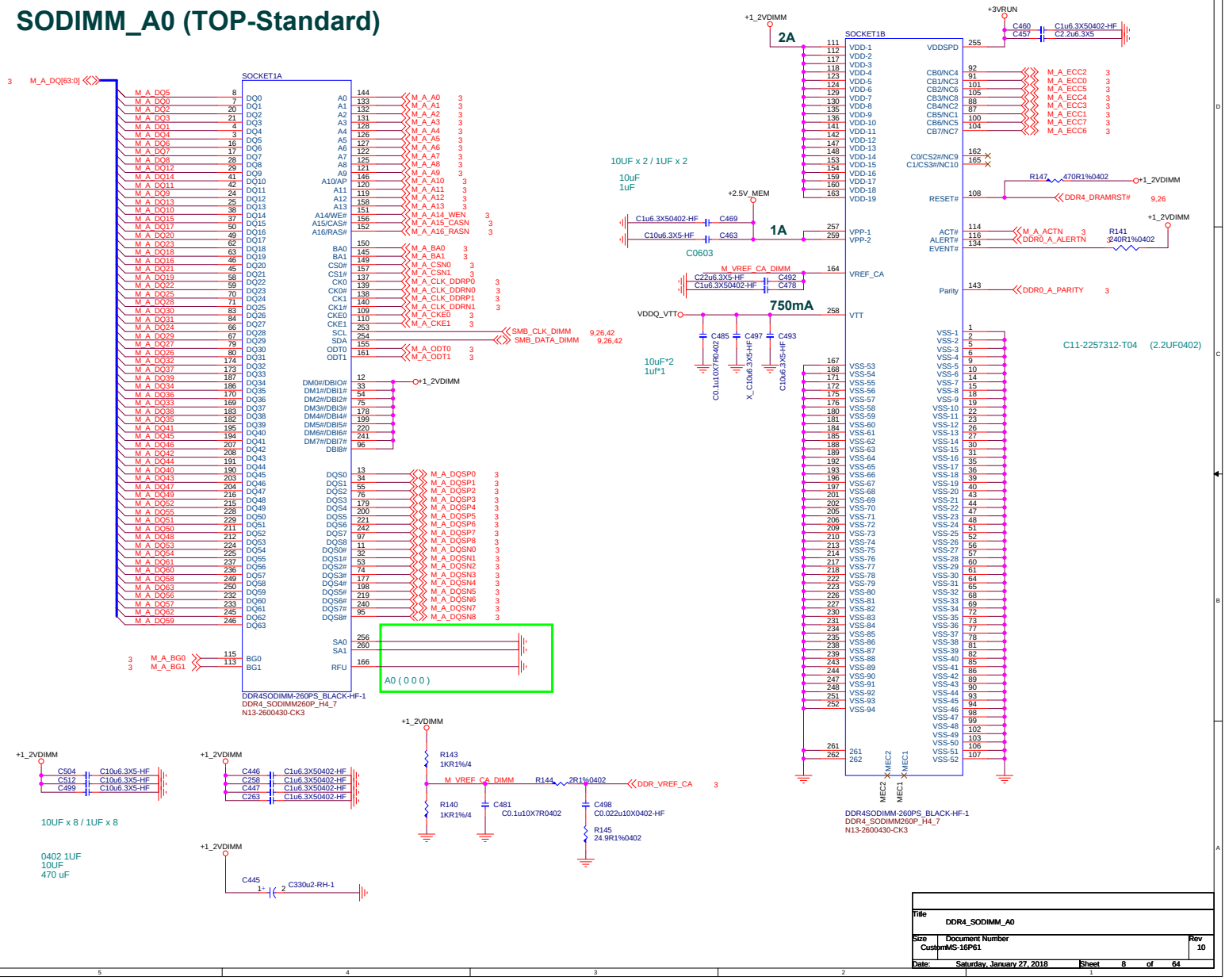
SODIMM_A0 (TOP-Standard)



Title	DDR4_SODIMM_A0		
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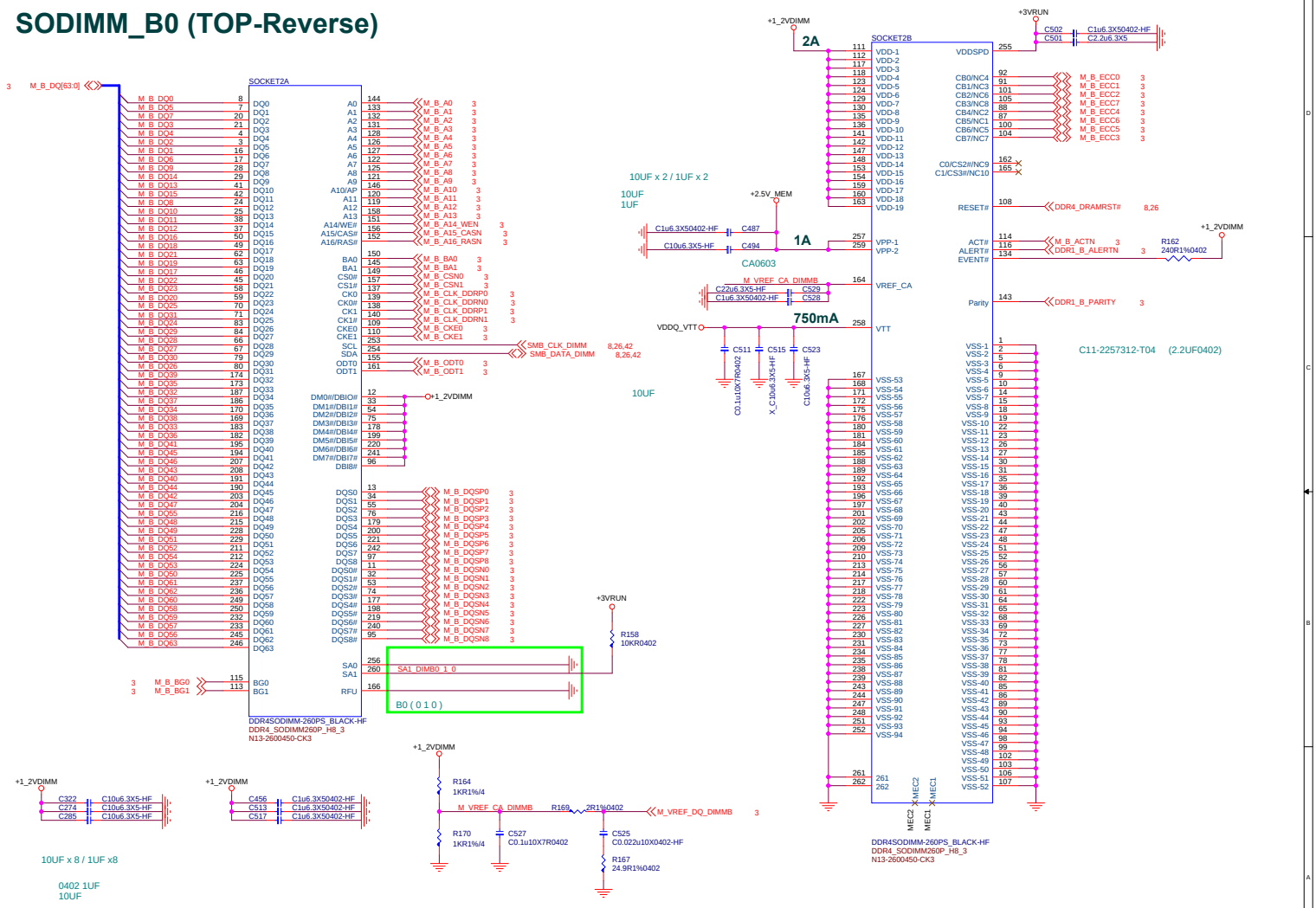
SODIMM_B0 (TOP-Reverse)



Title	DDR4_SODIMM_B0		
Size	Document Number		Rev
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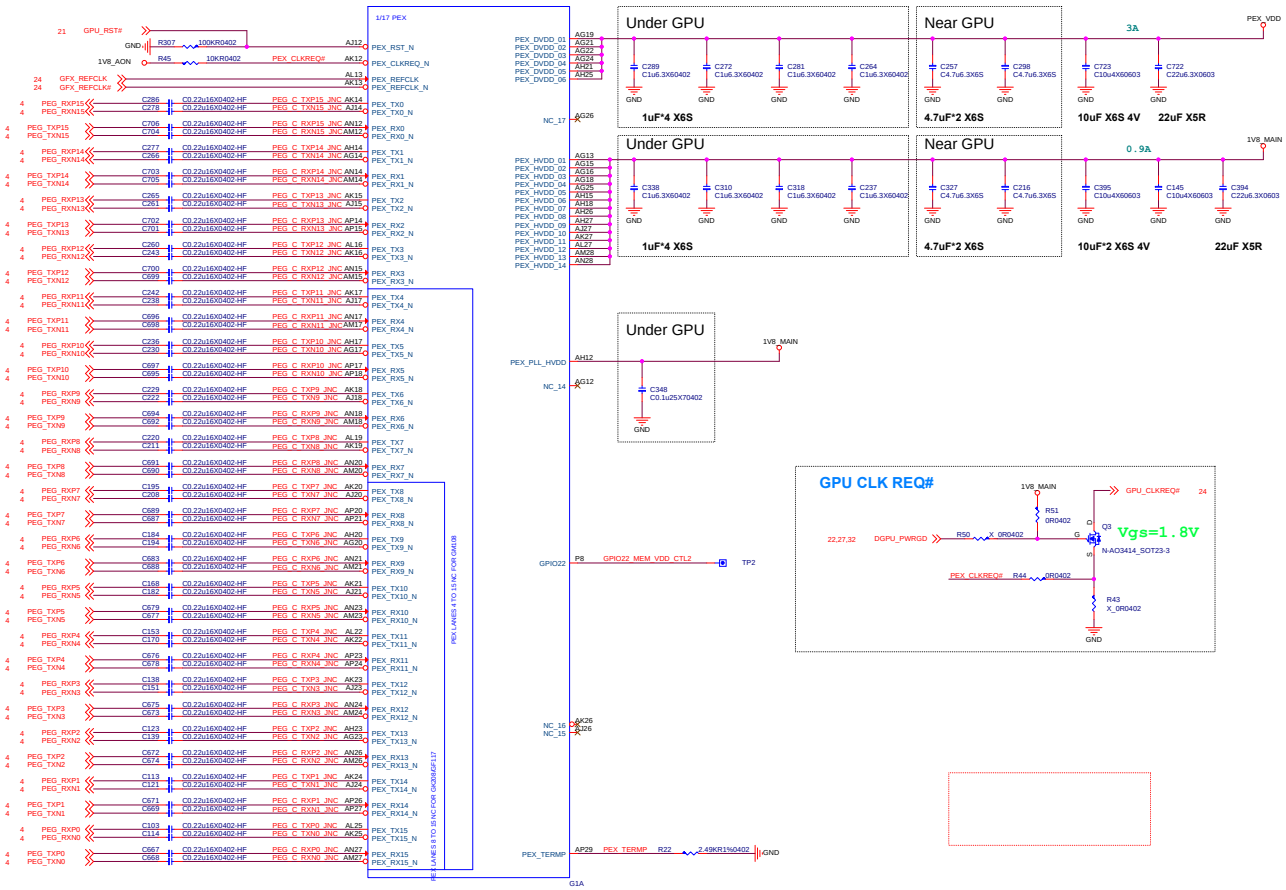
GPU PCI EXPRESS



Title	DGPU_GPU DECOUPLING
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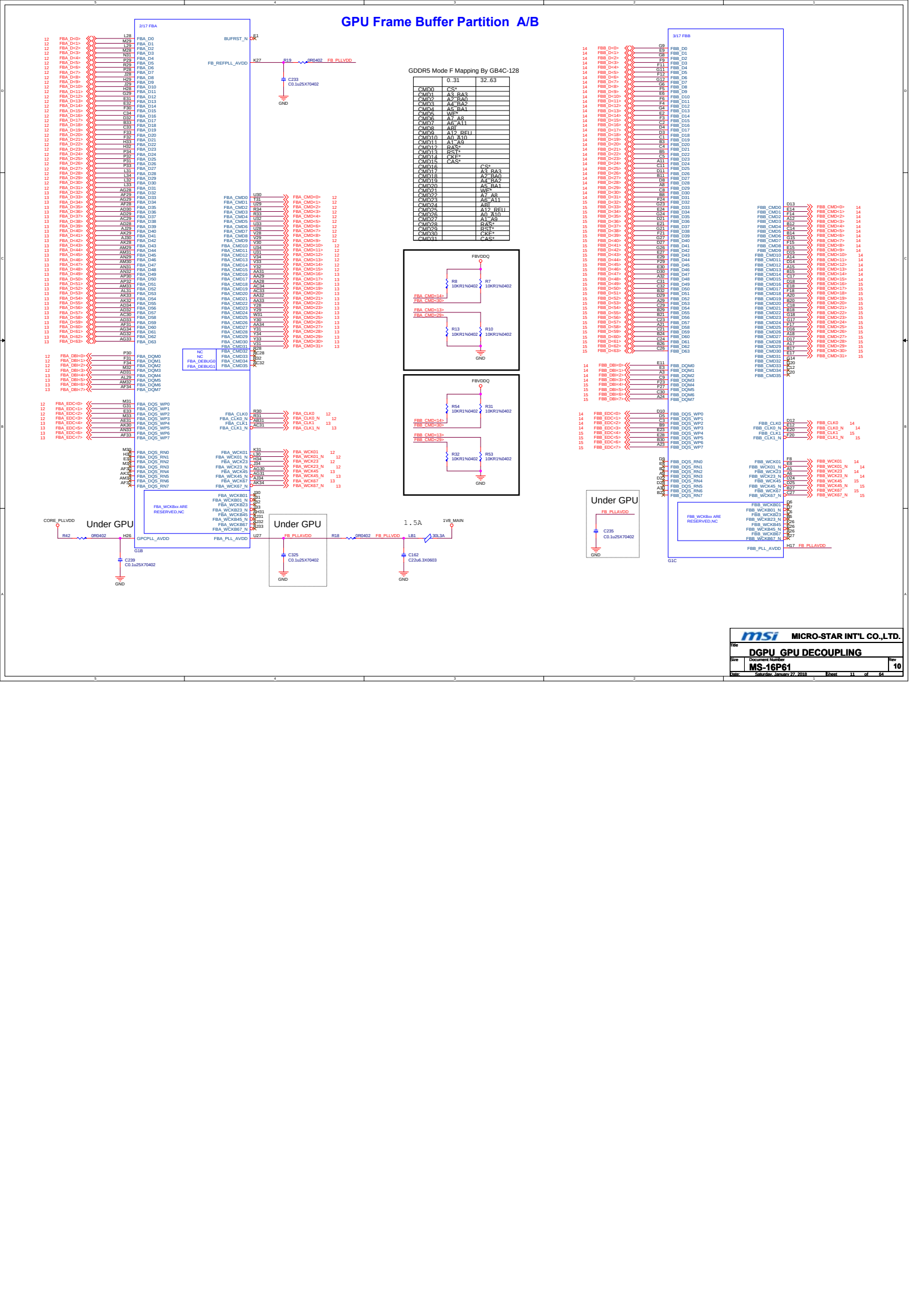
MICRO-STAR INT'L CO.,LTD.

GPU Frame Buffer Partition A/B



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING

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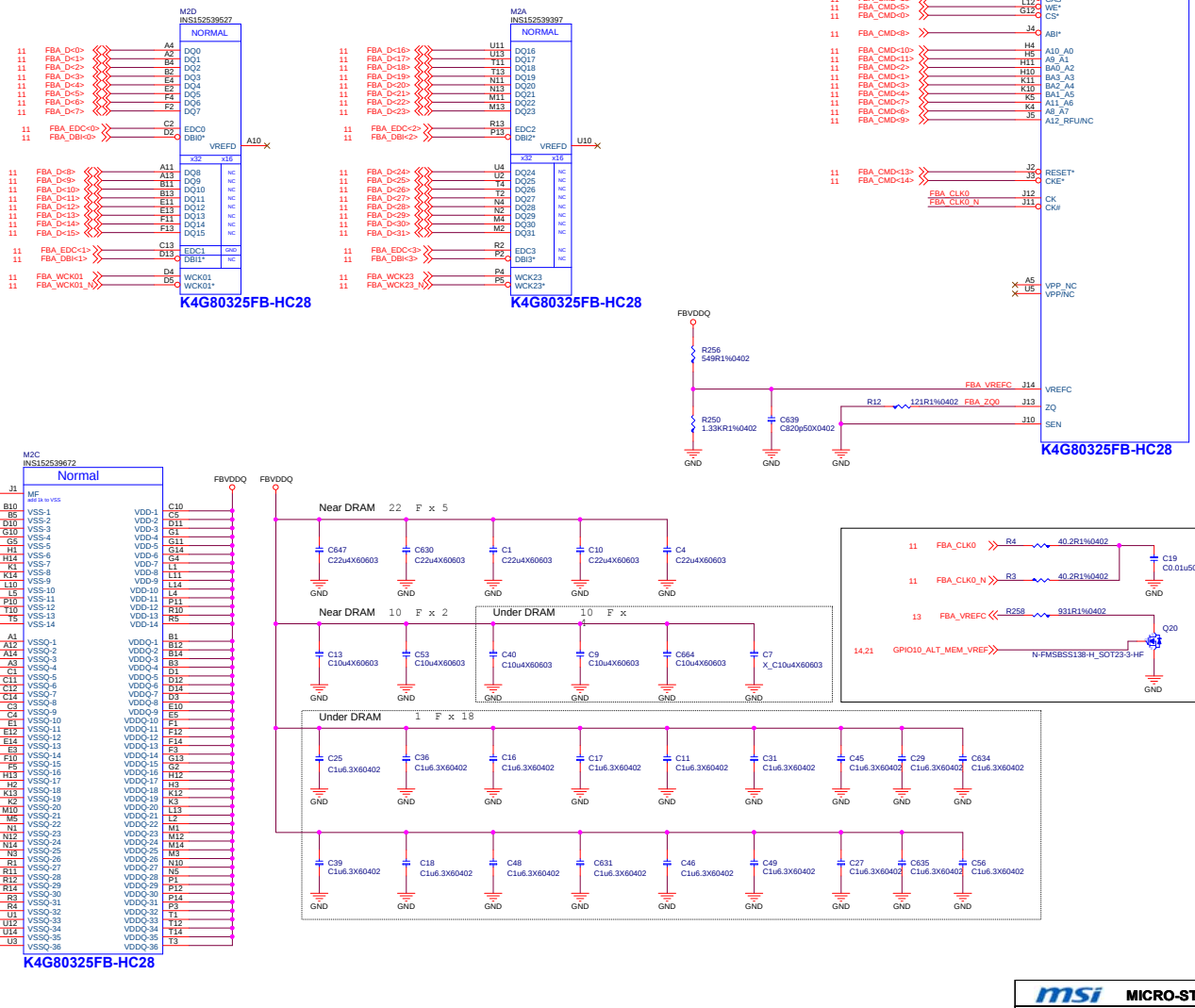
DGPU_GDDR5 FrameBuffer A0



msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_GPU DECOUPLING		
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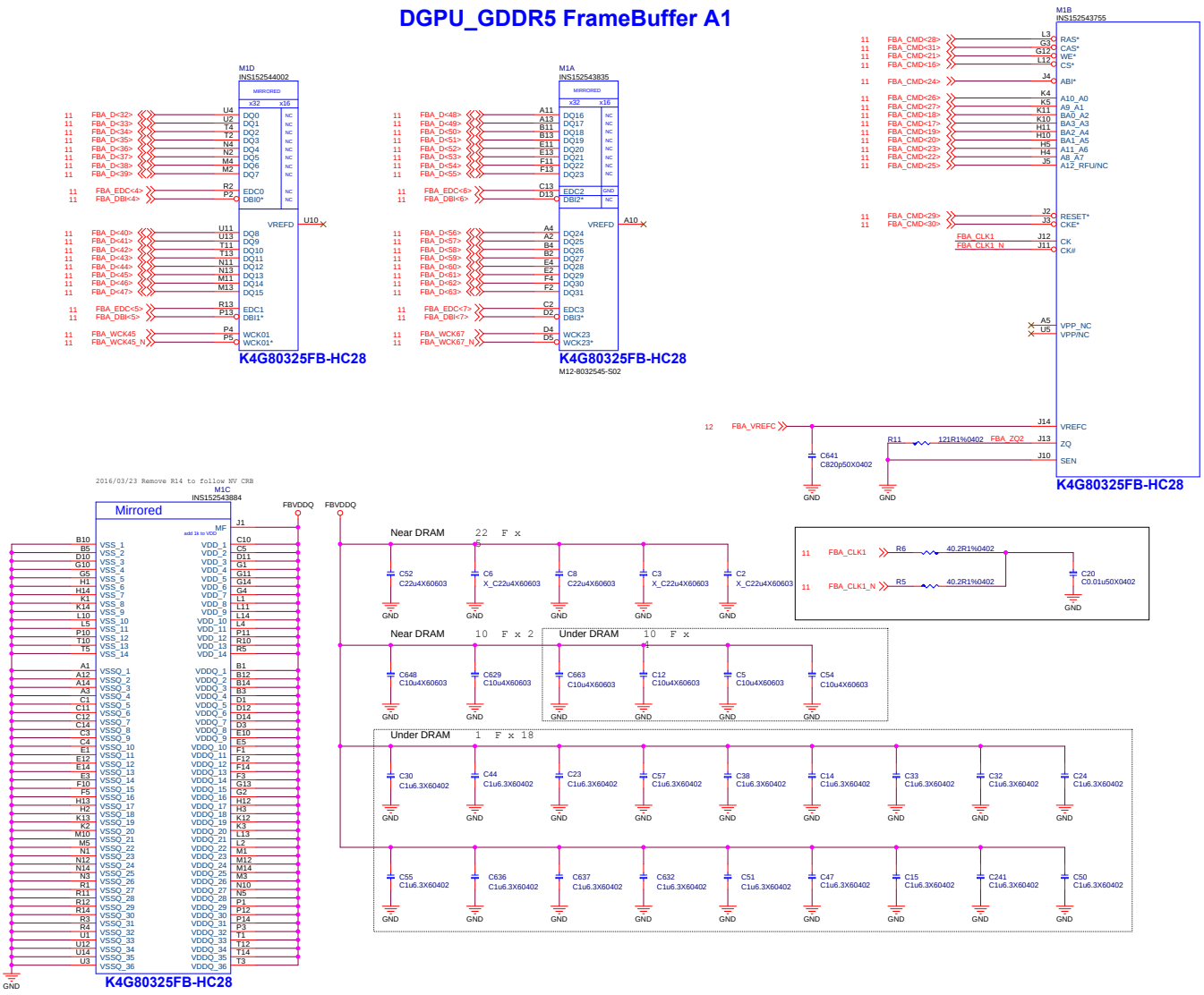
DGPU_GDDR5 FrameBuffer A1



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_GPU DECOUPLING	
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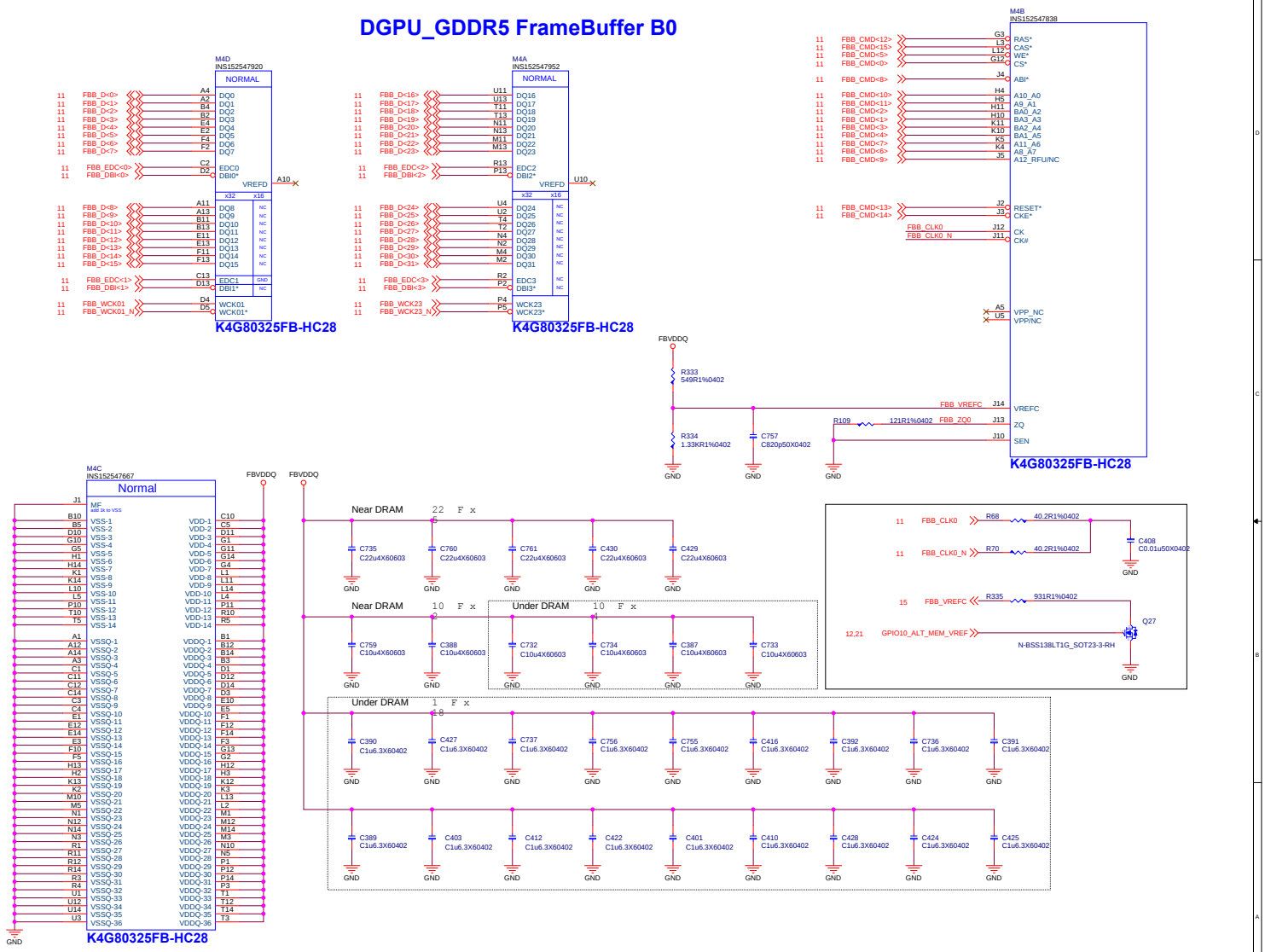
DGPU_GDDR5 FrameBuffer B0



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_GPU DECOUPLING	
Size	Document Number MS-16P61	Rev 10
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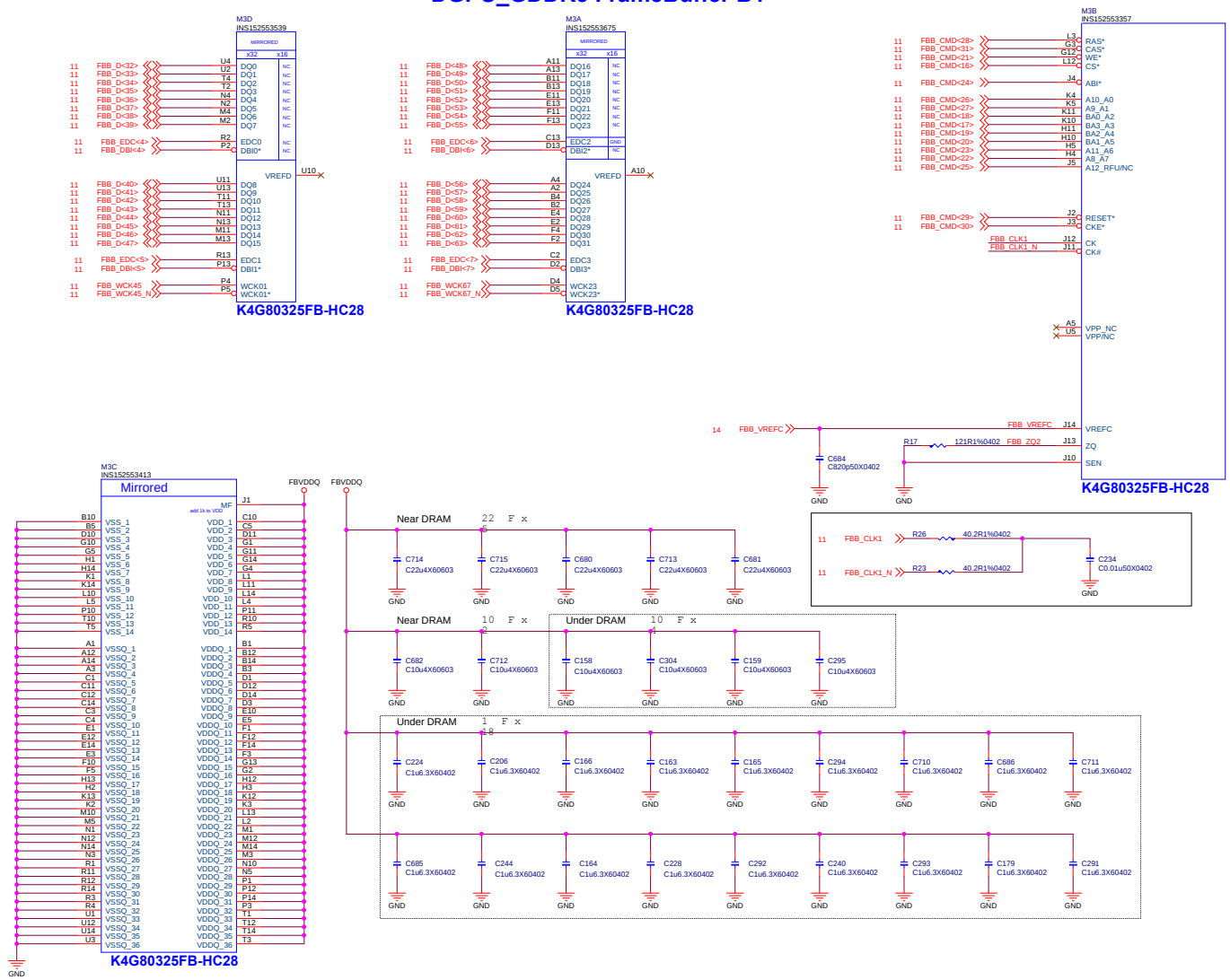
DGPU_GDDR5 FrameBuffer B1



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GPU DECOUPLING			
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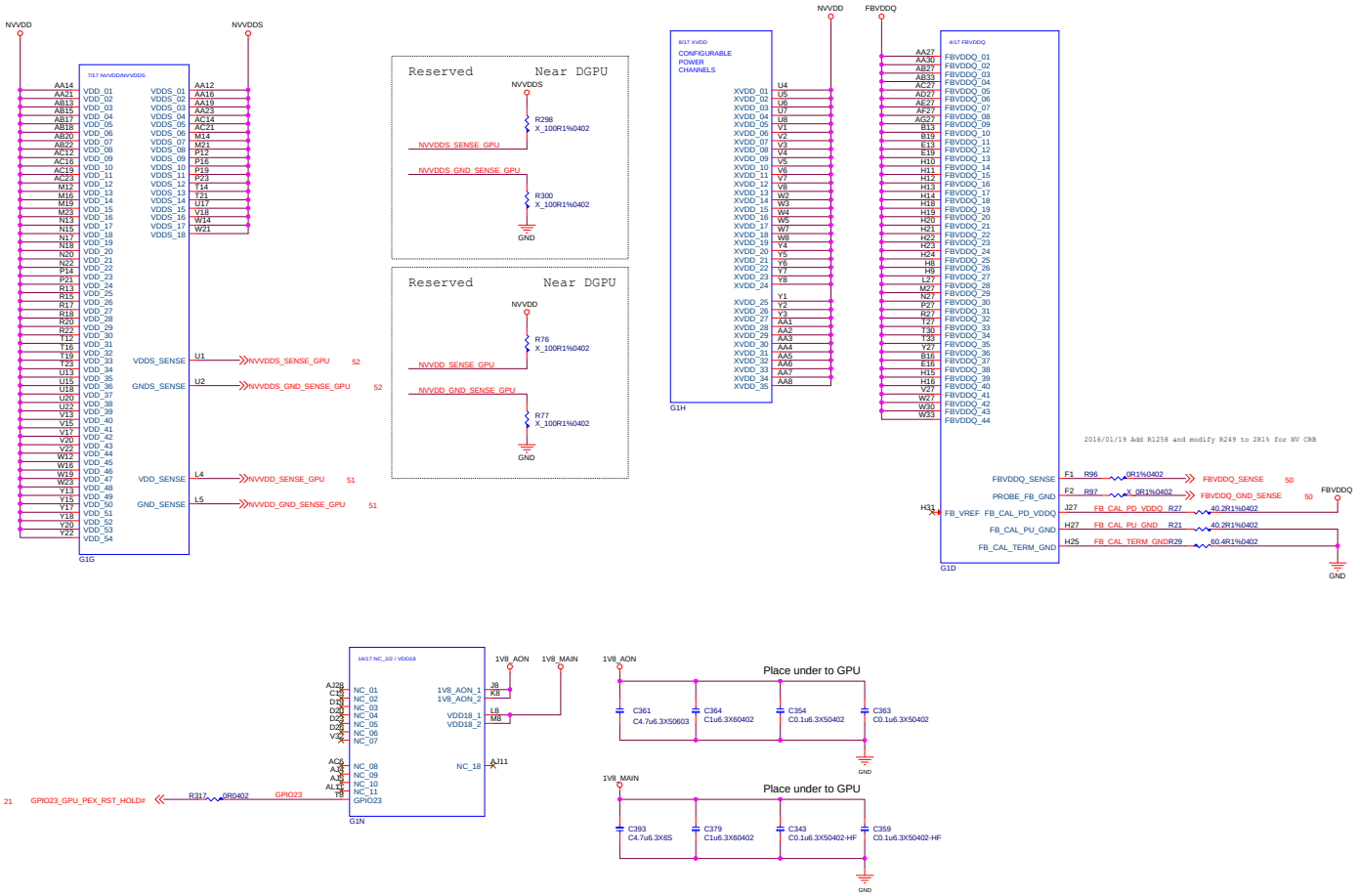
GPU NVVDD, FBVDDQ



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_GPU DECOUPLING		
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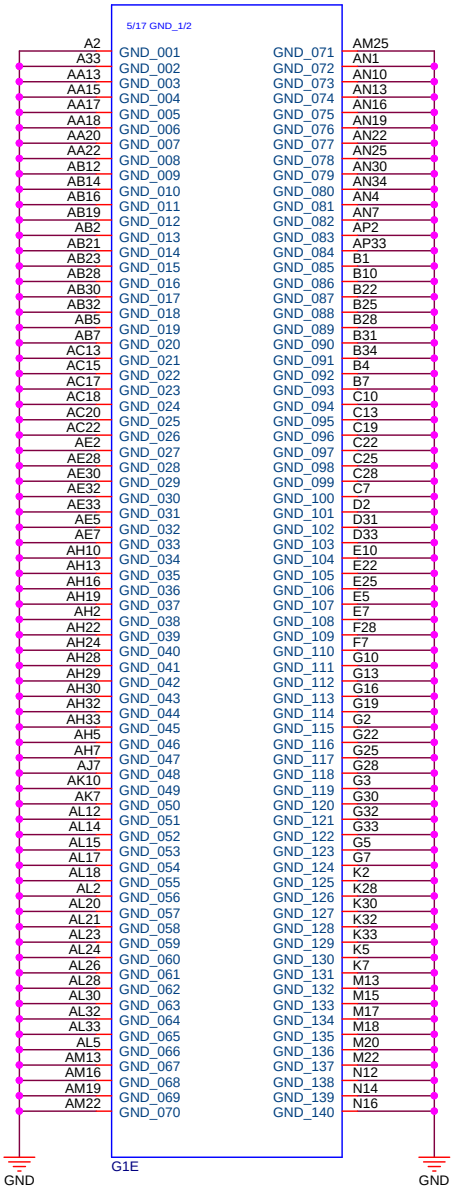
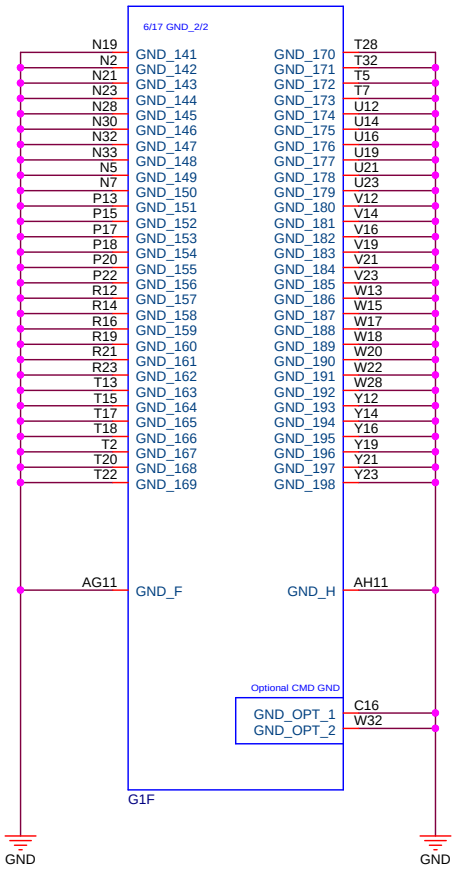
DGPU GND





MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_GPU DECOUPLING		
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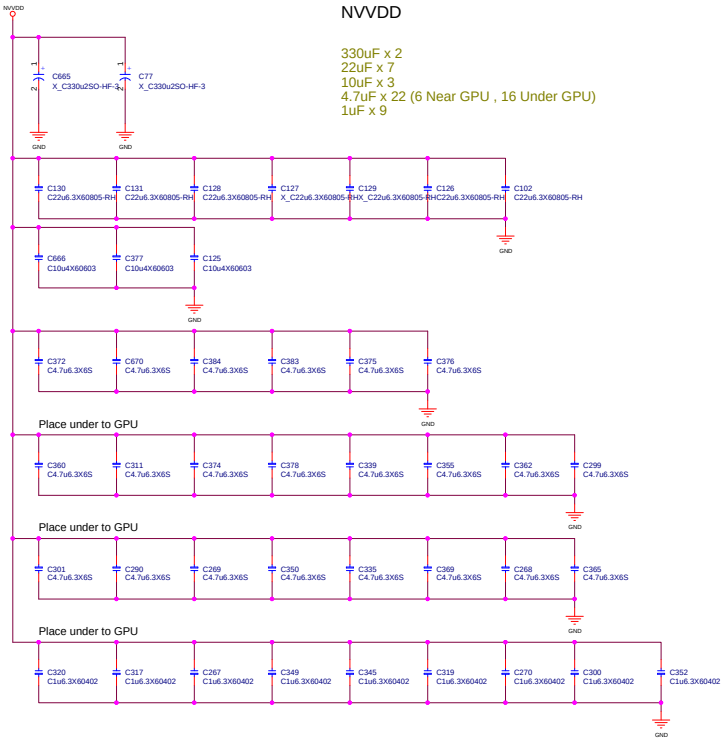
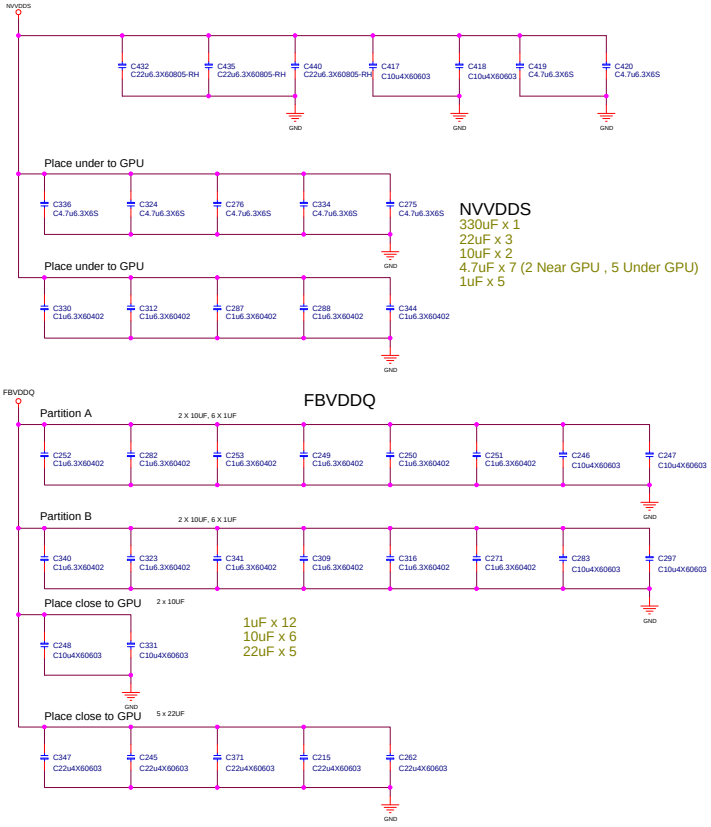
GPU DECOUPLING



NVVDD

330uF x 2
22uF x 7
10uF x 3
4.7uF x 22 (6 Near GPU , 16 Under GPU)
1uF x 9



NVVDDS

330uF x 1
22uF x 3
10uF x 2
4.7uF x 7 (2 Near GPU , 5 Under GPU)
1uF x 5

FBVDDQ

1uF x 12
10uF x 6
22uF x 5

MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_GPU DECOUPLING		
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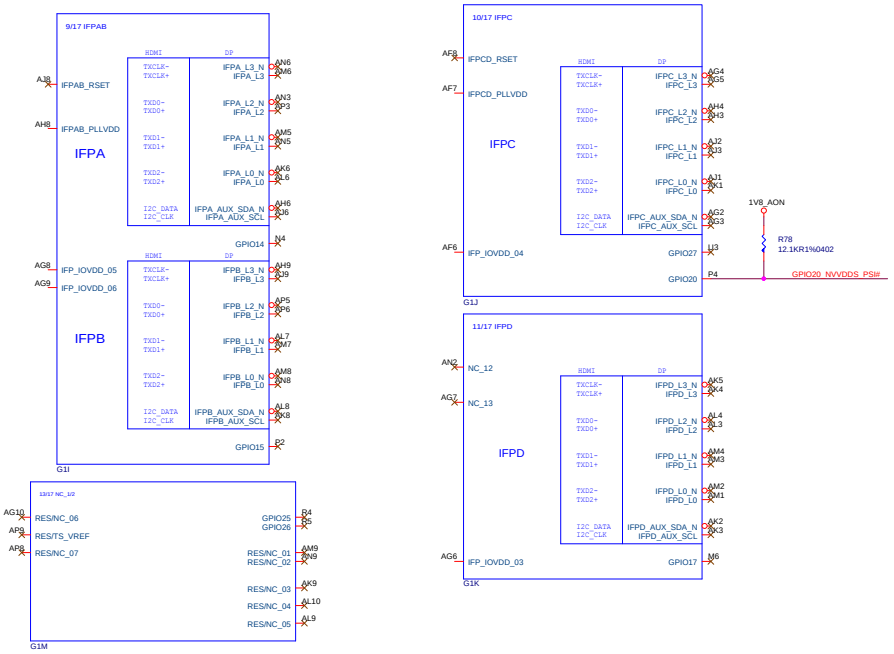
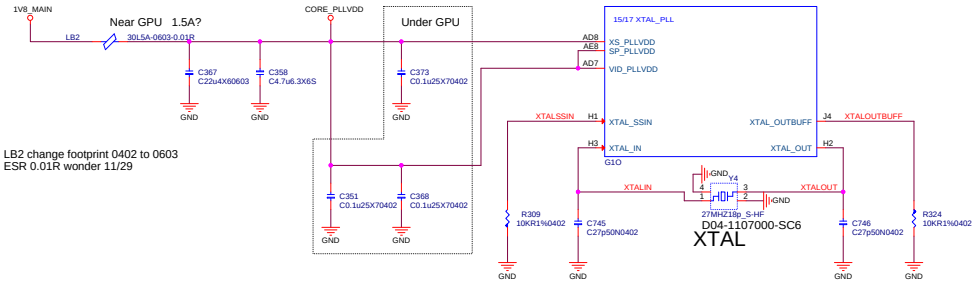
DACA,Display IF



DGPU XTAL



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_GPU DECOUPLING		
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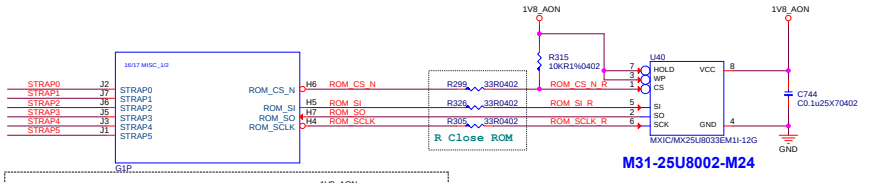
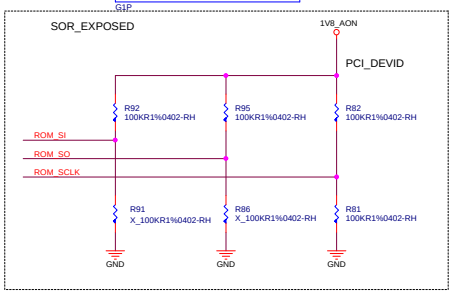
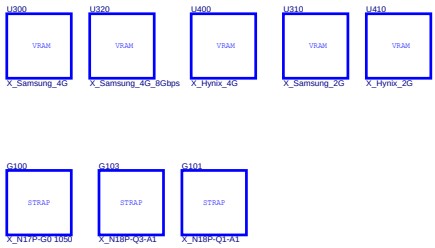
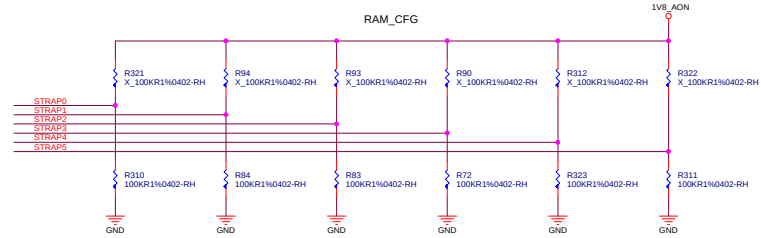
ROM, MULTI-LEVEL STRAPS



M31-25U8002-M24







ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		STRAP Set
L	L	L	**0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28**	**4GB**	R310 R84 R83
L	L	H	0x1 Micron: MT51J256M32HF-70:A		R310 R84 R93
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C		R310 R94 R83
L	H	H			
H	L	L			
H	L	H			
H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C		R321 R94 R83
H	H	H	**0x7 Samsung: M12-41325A5-S02/K4G41325FE-HC28**	**2GB**	R321 R94 R93
L	L	M	0x8 Micron: EDW032BABG-70-F:A		R310 R84 R93R83
L	M	L			

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING

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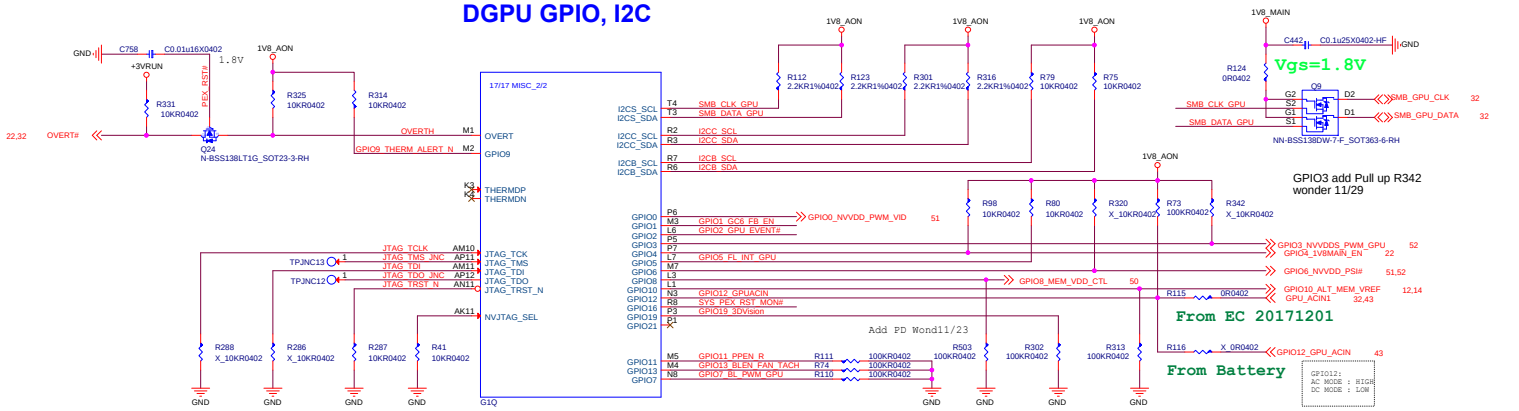
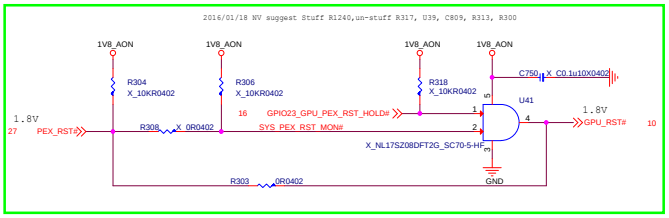
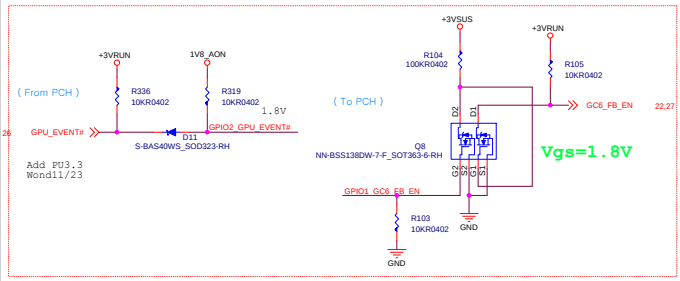
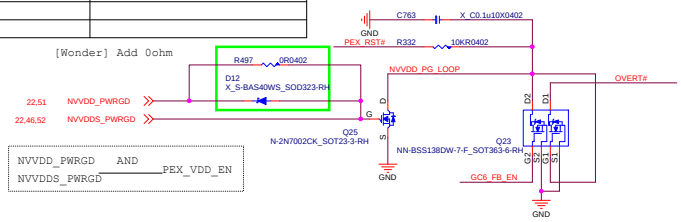
DGPU GPIO, I2C



Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, 1V8 pull-up to 1V8 _AON
GPIO6	NVVDD_PSI	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brighteness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to 1V8 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	







msi MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GPU DECOUPLING			
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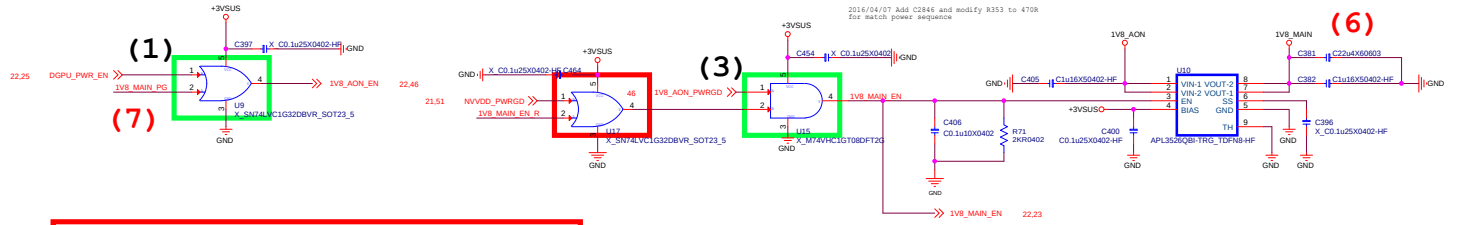
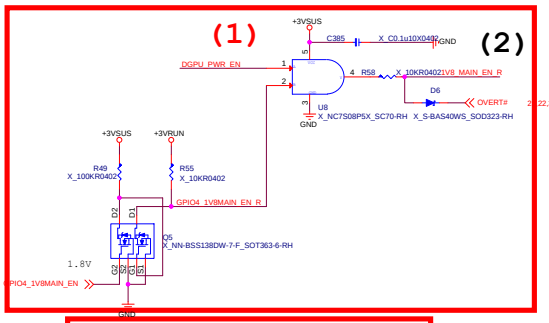
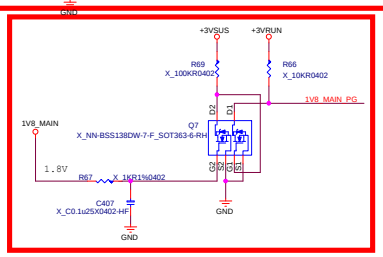
NVIDIA Power Sequence Control

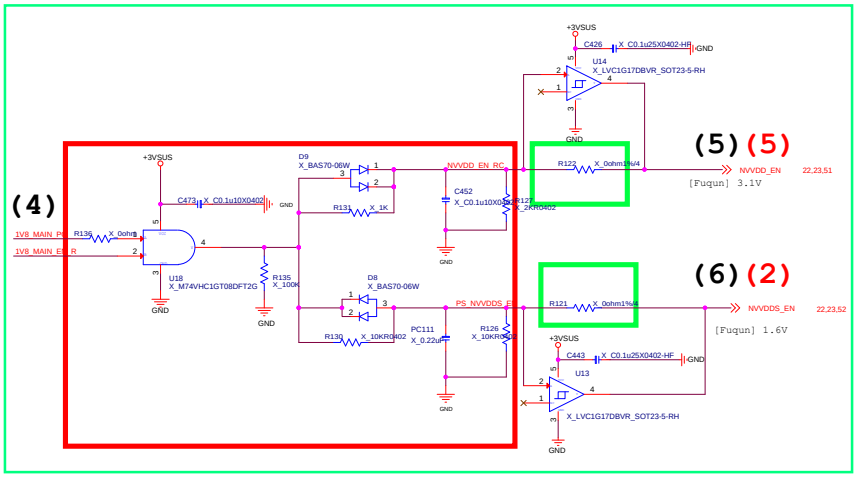
Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV/NVVDD -> NVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power down = NVDDS -> PEX_VDD -> NVVDD/FBVDDQ -> 3V3_NV -> 1V8_MAIN -> 1V8_AON

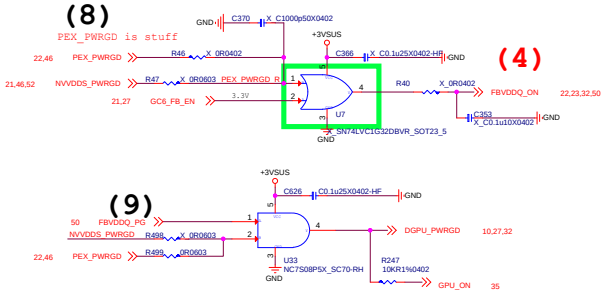


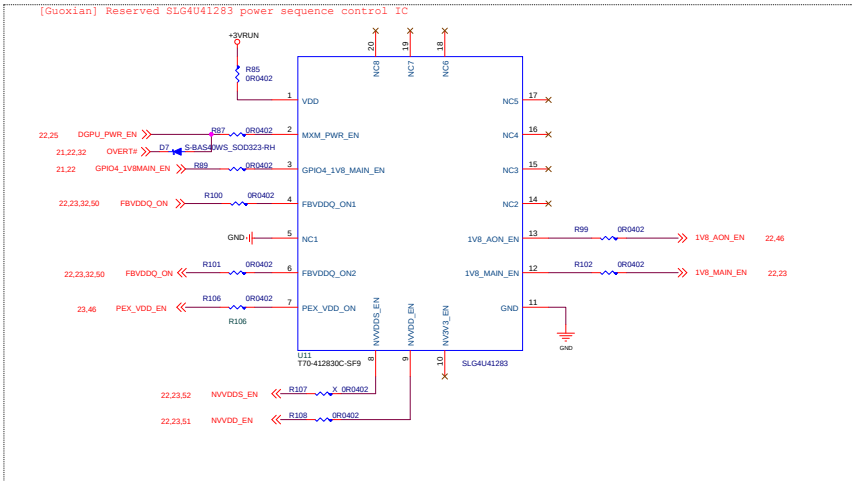






(7) NVVDDS_PWRGD → (3) PEX_VDD





msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_GPU DECOUPLING		
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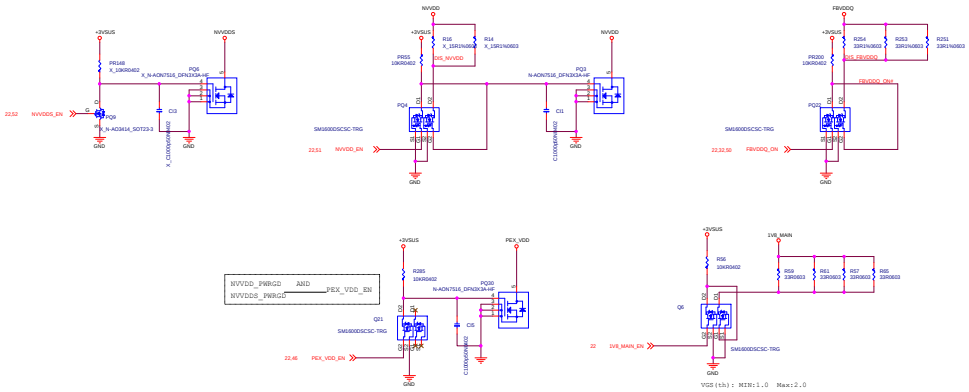
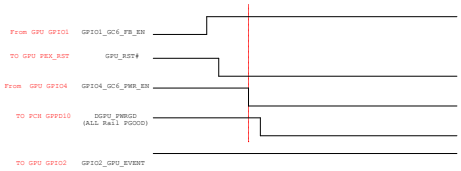
Discharge

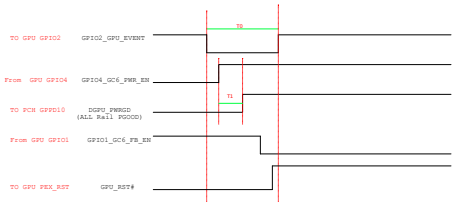
Remove NVVDS Power NC
PR148 PQ9 PQ9,CI3



GC6 2.1 ENTRY SEQUENCE



GC6 2.1 EXIT SEQUENCE

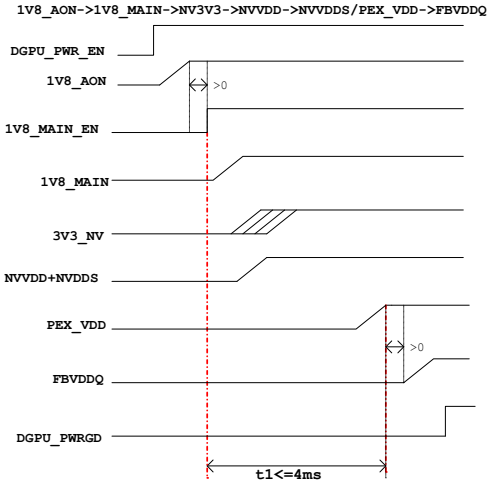


GC6 2.1 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU_EVENT# assertion
T1	0.04	4	mS	3V3_MAIN_EN assertion to all power rails up and stable

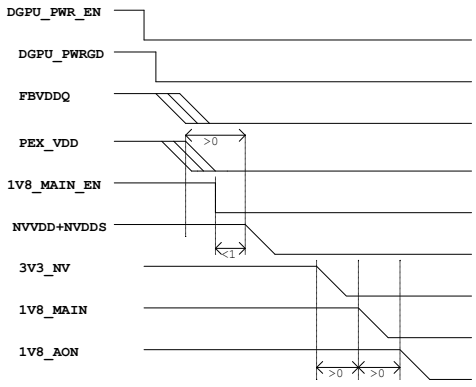
POWER UP Sequence

1V8_AON->1V8_MAIN->NV3V3->NVVDD->NVVDDS/PEX_VDD->FBVDDQ



POWER Down Sequence

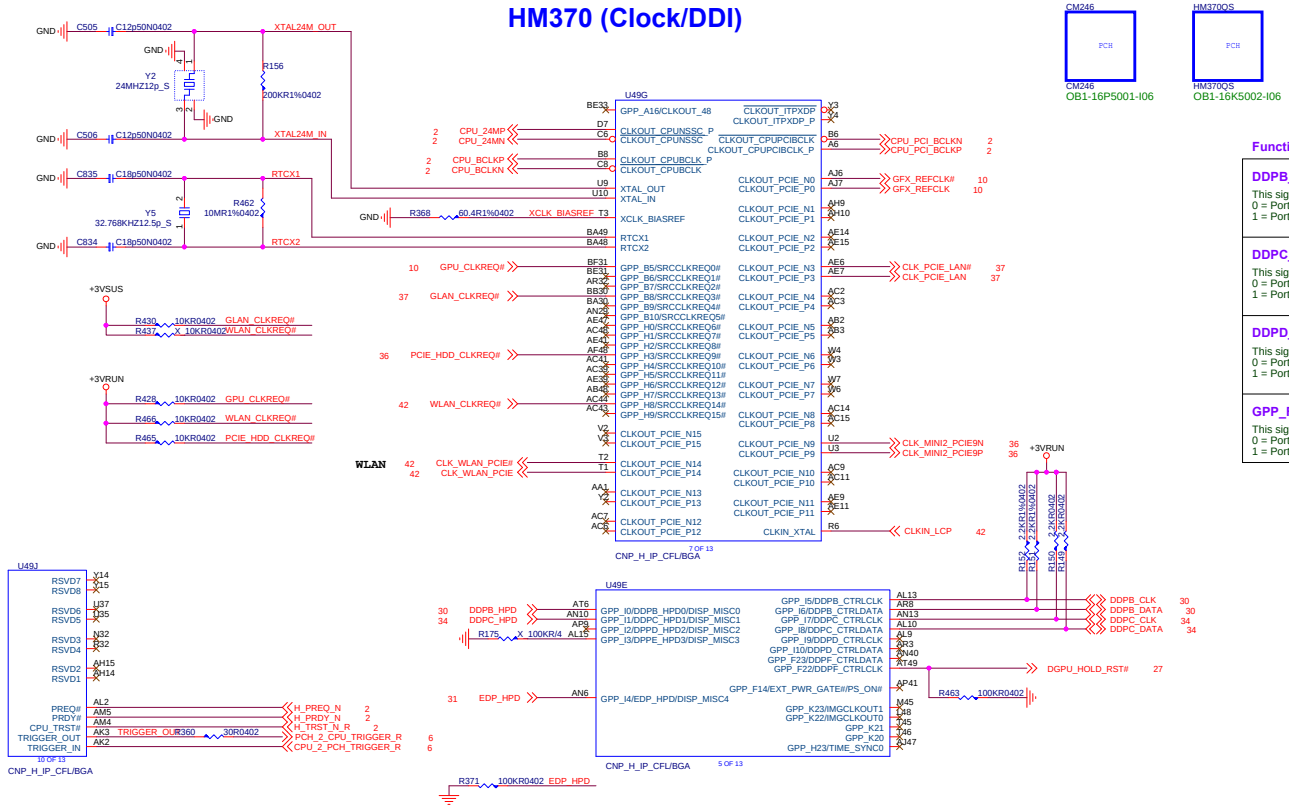
PEX_VDD/FBVDDQ->NVVDD+NVVDS->NV3V3->1V8_MAIN->1V8_AON



NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation.
   If any GPU power rail cannot ge guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

HM370 (Clock/DDI)



Functional Strap Definitions

DDPB_CTRLDATA / GPP_I6

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPC_CTRLDATA / GPP_I8

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPD_CTRLDATA / GPP_I10

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

GPP_F23

This signal has a weak internal pull-down.
0 = Port F is not detected. (Default)
1 = Port F is detected.

MICRO-STAR INT'L CO.,LTD.

Title: PCH_1(CLK/DDI)

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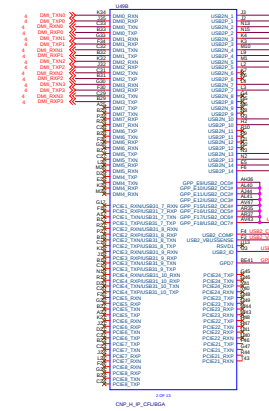
HM370 (DMI/PCIE/USB/CNVi)

EPF LED



USB1(DB)
USB2(DB)
USB3.1(MB)
USB3.1 TYPE_A-2
FP
Card Reader
8051 MCU
Webcam
M.2(WLAN)

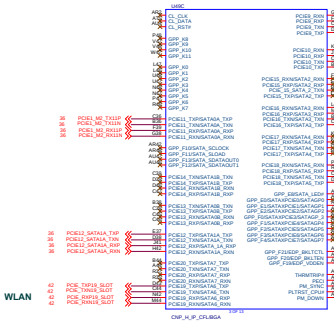
USB			
USB 2.0	USB 3.1	Device	Note
1	1	USB TYPE_C-1	
2	2	USB TYPE_C-2	
3	3	USB TYPE_A-1	
4	4	USB TYPE_A-2	
5			
6			
7		EPF021	
8		USB 2.0	16JB2
9			
10			
11		WebCam	
12		CARDREADER	16JB2
13			
14		WLAN	

GPD7

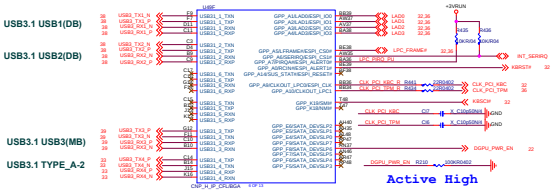
External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

High Speed I/O Ports			
HM370			Device
1	USB3.1 Gen 1		USB TYPE_A-1
2	USB3.1 Gen 1		USB TYPE_A-2
3	N/A		NC
4	N/A		NC
5	INTEL LAN Only		NC
6	N/A		NC
7	N/A		NC
8	N/A		NC
9	PCIE/LAN		
10	PCIE	PICE Configurable M.2	M.2 SSD-1
11	PCIE/SATA0		
12	PCIE/LAN/SATA1		
13	PCIE/LAN/SATA0		NC
14	PCIE/SATA1		NC
15	PCIE		WLAN
16	PCIE		LAN
17	PCIE/SATA4		ODD TO HDD
18	PCIE/SATA5		M.2 SSD-2
19	PCIE		NC
20	PCIE		NC
21	PCIE		
22	PCIE	PICE Configurable M.2	M.2 SSD-2
23	PCIE		
24	PCIE		

SATA Lane 0 has the flexibility to be mapped to PCIE 11 or 13
SATA Lane 1 has the flexibility to be mapped to PCIE 12 or 14



PCIE 9-12 (M2-1)
LAN
SATA 5 HDD
WLAN



USB3.1 USB1(DB)
USB3.1 USB2(DB)
USB3.1 USB3(MB)
USB3.1 TYPE_A-2

Active High

GPP_A6

PCI Interrupt Request Ax
Note: An external Pull-up is required

GPP_A7

PCI Interrupt Request Ax
Note: An external Pull-up is required

GPP_A14

LPC Mode - Suspend Status:
This signal is asserted by the PCH to indicate that the system will be entering a low power state soon.

GPP_J4 / CNV_BRI_DT

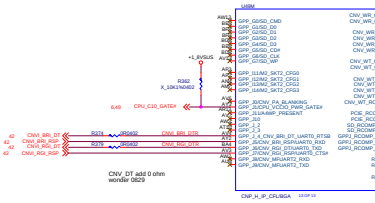
This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

GPP_J6 / CNV_RGI_DT

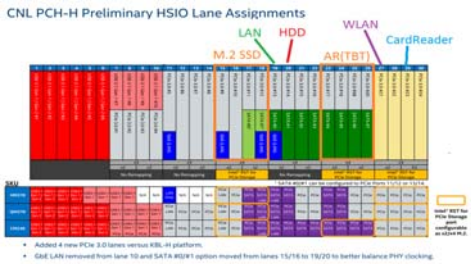
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J9

This signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail



CNV_DT add 0 ohm
wondair 0829



MSI	MICRO-STAR INT'L CO.,LTD.
Title	PCH 2(DMI/PCIE/USB/CNVi)
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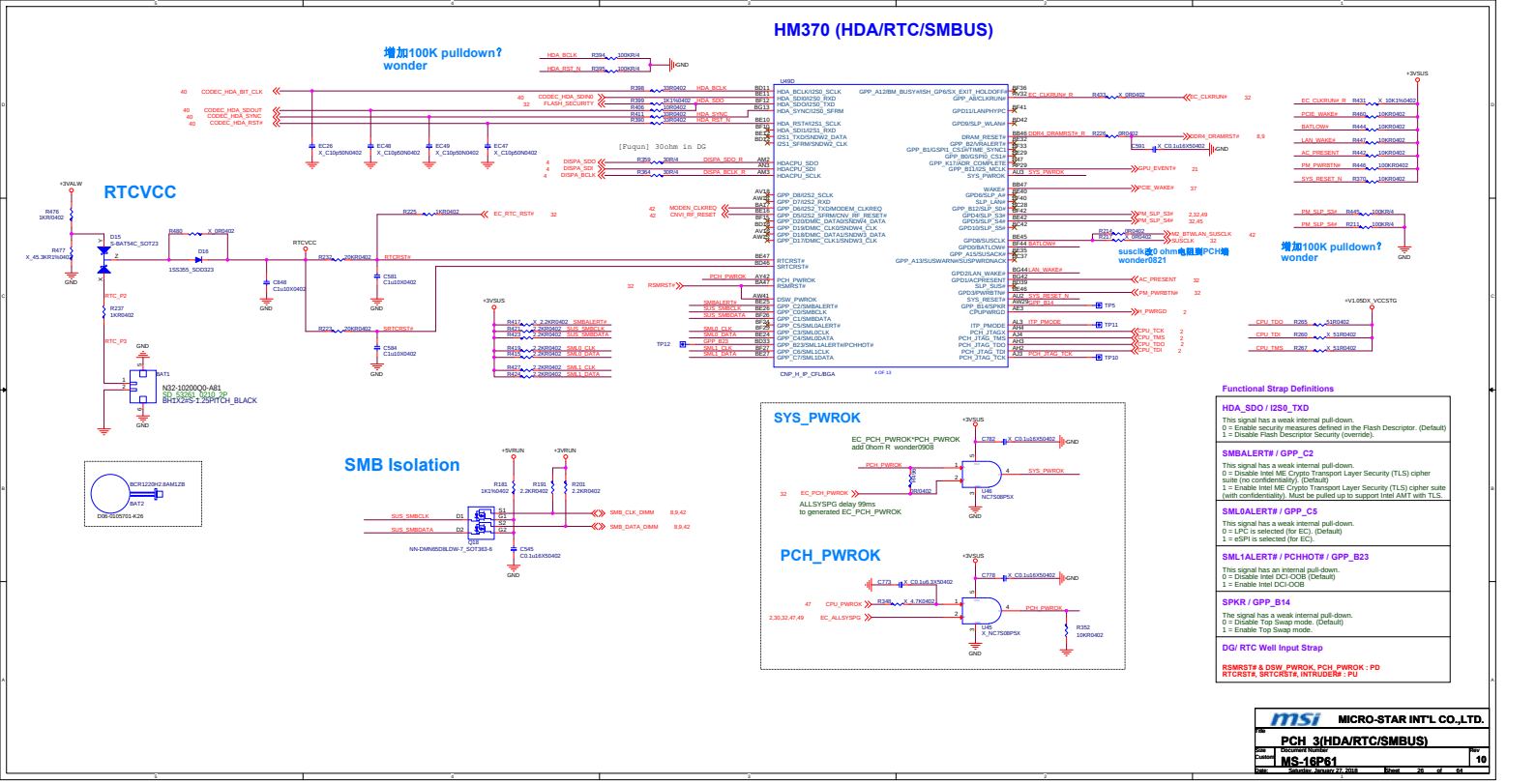
HM370 (HDA/RTC/SMBUS)



Functional Strap Definitions

HDA_SDO / I2S0_TXD

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

SMBALERT# / GPP_C2

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

SML0ALERT# / GPP_C5

This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

SML1ALERT# / PCHHOT# / GPP_B23

This signal has an internal pull-down.
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB

SPKR / GPP_B14

The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode.

DG/ RTC Well Input Strap

RSMRST# & DSW_PWROK_PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

MICRO-STAR INT'L CO.,LTD.			
Title: PCH_3(HDA/RTC/SMBUS)			
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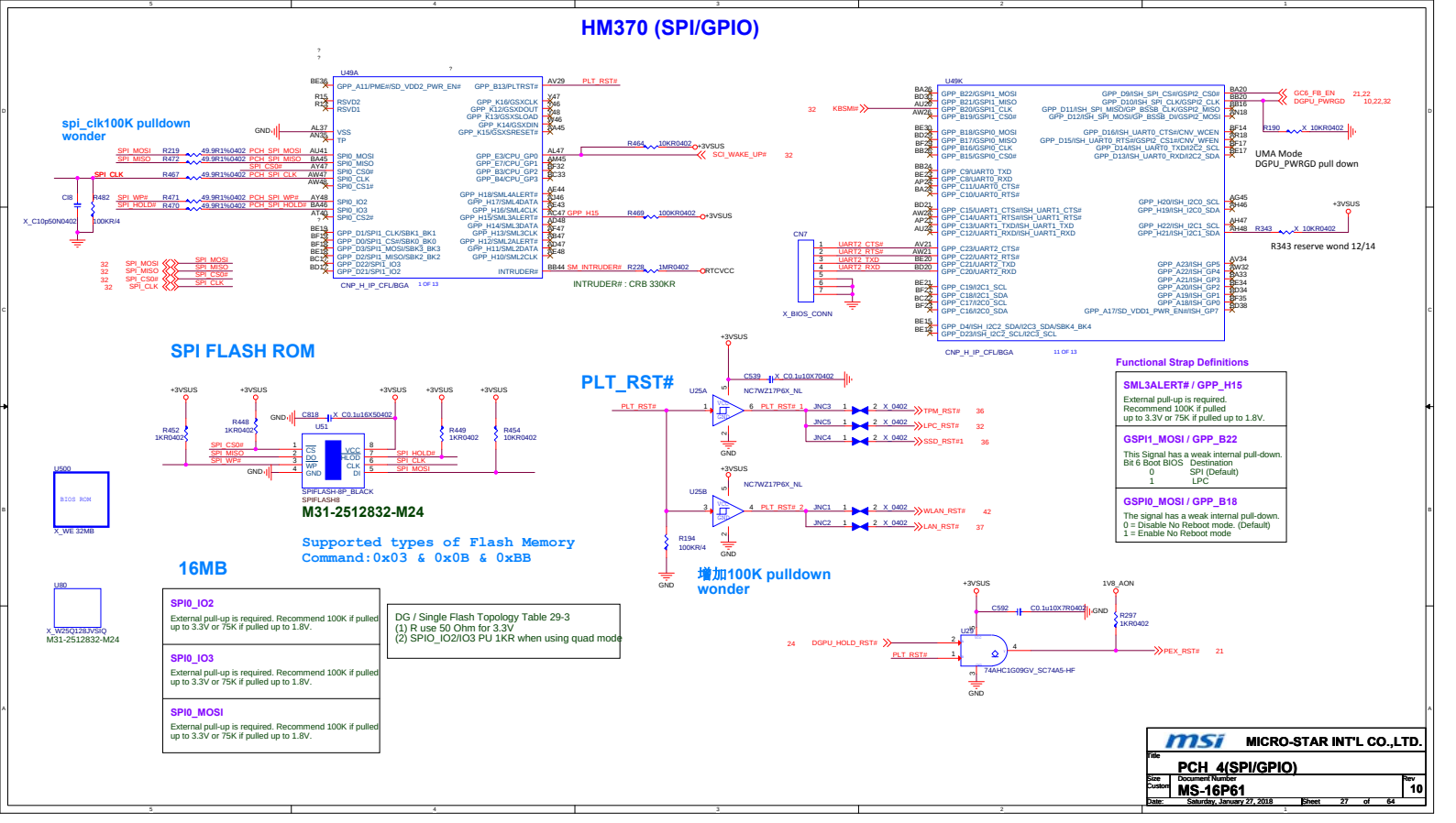
HM370 (SPI/GPIO)



SPI FLASH ROM

Supported types of Flash Memory
Command:0x03 & 0x0B & 0xBB

16MB

SPI0_IO2
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_IO3
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_MOSI
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

DG / Single Flash Topology Table 29-3
(1) R use 50 Ohm for 3.3V
(2) SPIO_IO2/IO3 PU 1KR when using quad mode

PLT_RST#

msi	MICRO-STAR INT'L CO.,LTD.				
Title	PCH_4(SPI/GPIO)				
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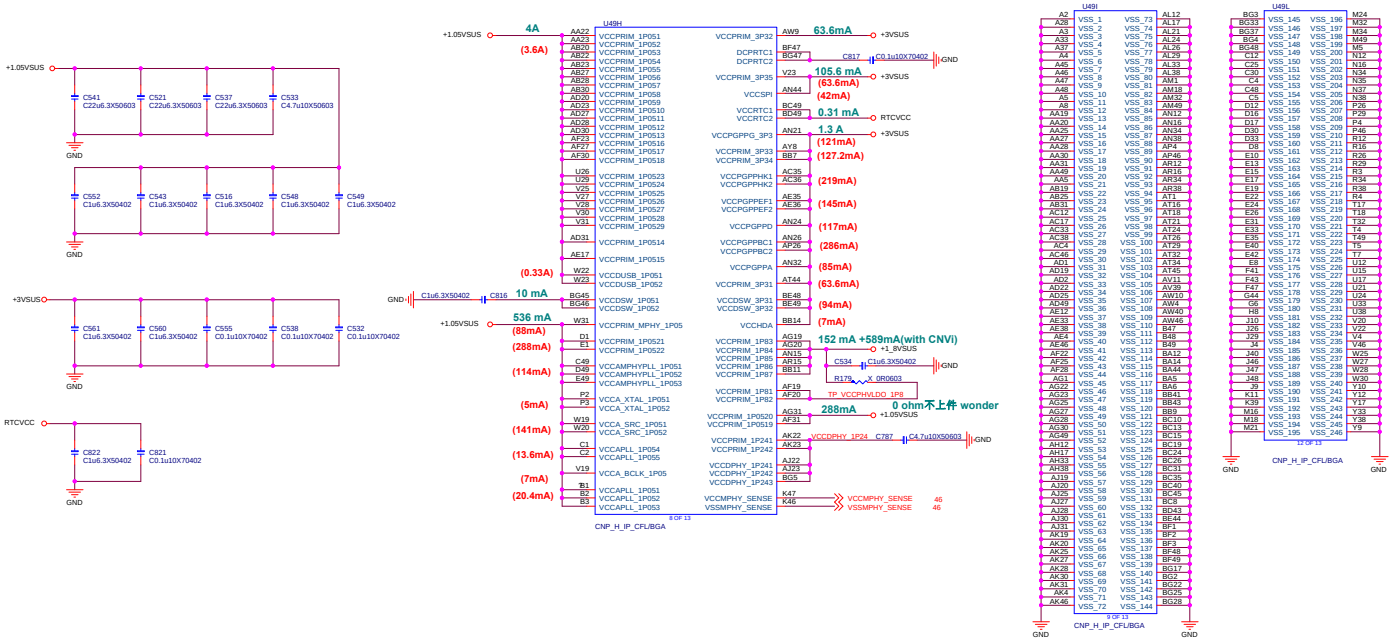
HM370 (Power & GND)



MSI	MICRO-STAR INT'L CO.,LTD.
Title	PCH 5(Power)
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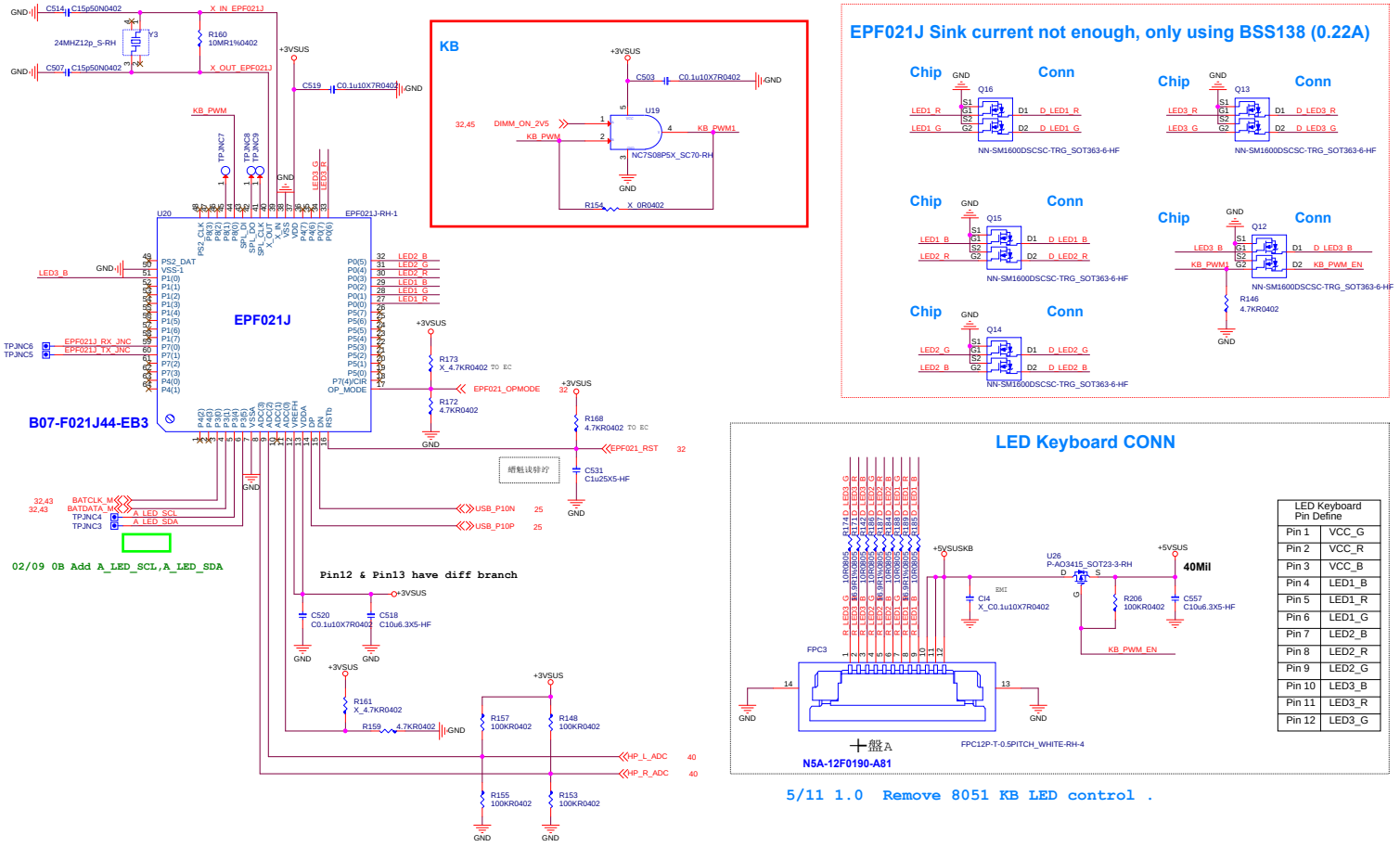
LED 8051 Controller



Title	LED 8051/KB CON
Size	Document Number: CustomMS-16P61
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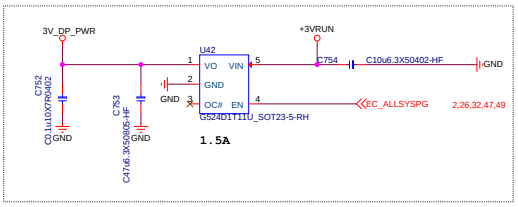
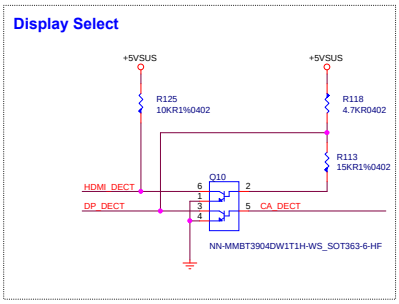
Display Port

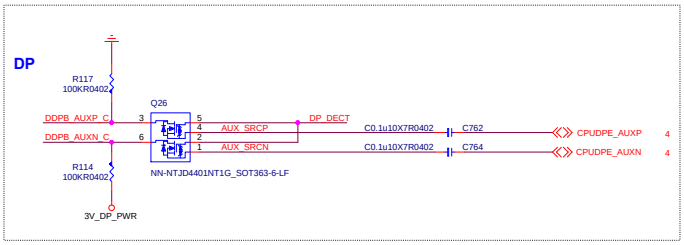
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



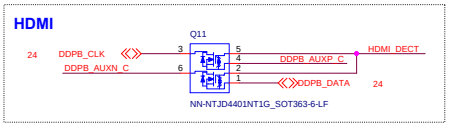
Display Select



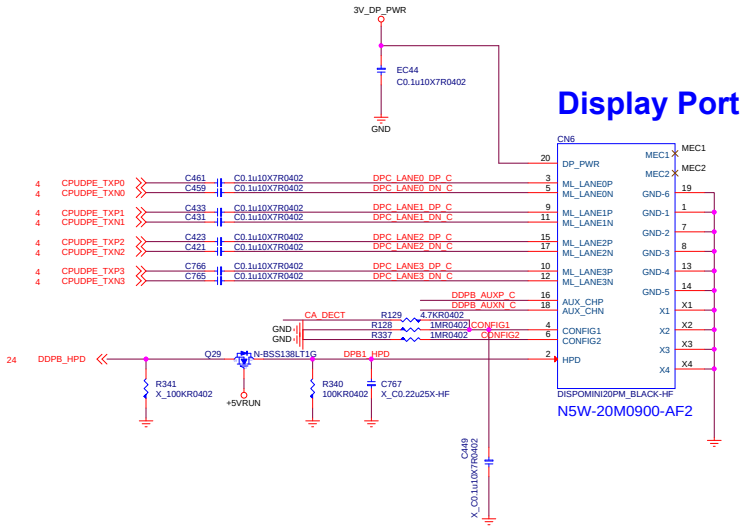
Dual Mode Switch



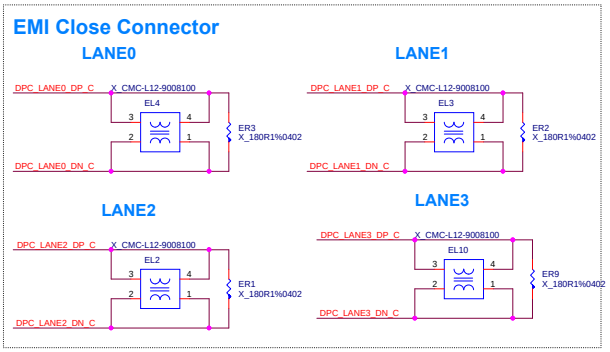
HDMI



Display Port



EMI Close Connector



MICRO-STAR INT'L CO.,LTD.

Title: DP

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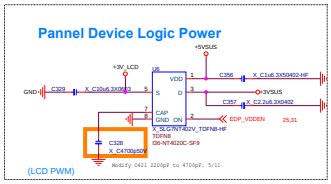
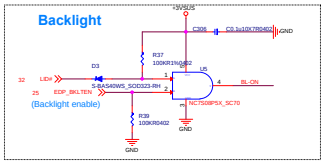
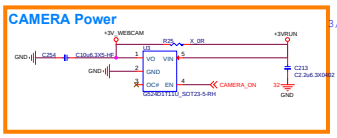
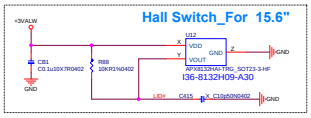
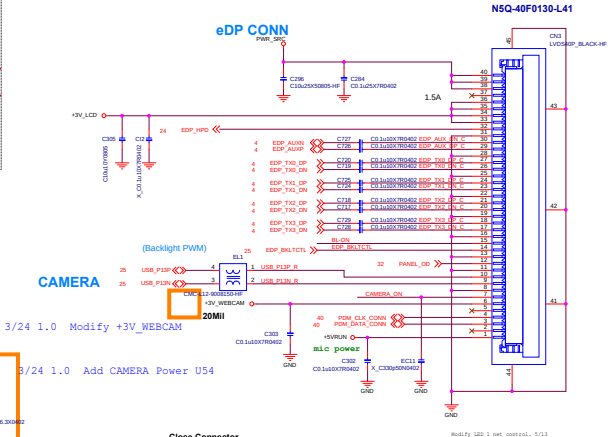
eDP/Camera

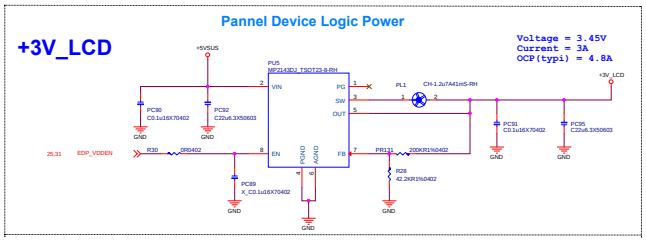












LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channe
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	**OE_EN**	**OD_Enable Signal of TCON**

LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channe
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	**OE_EN**	**OD_Enable Signal of TCON**

MICRO-STAR INT'L CO.,LTD.

Title: eDP Connector

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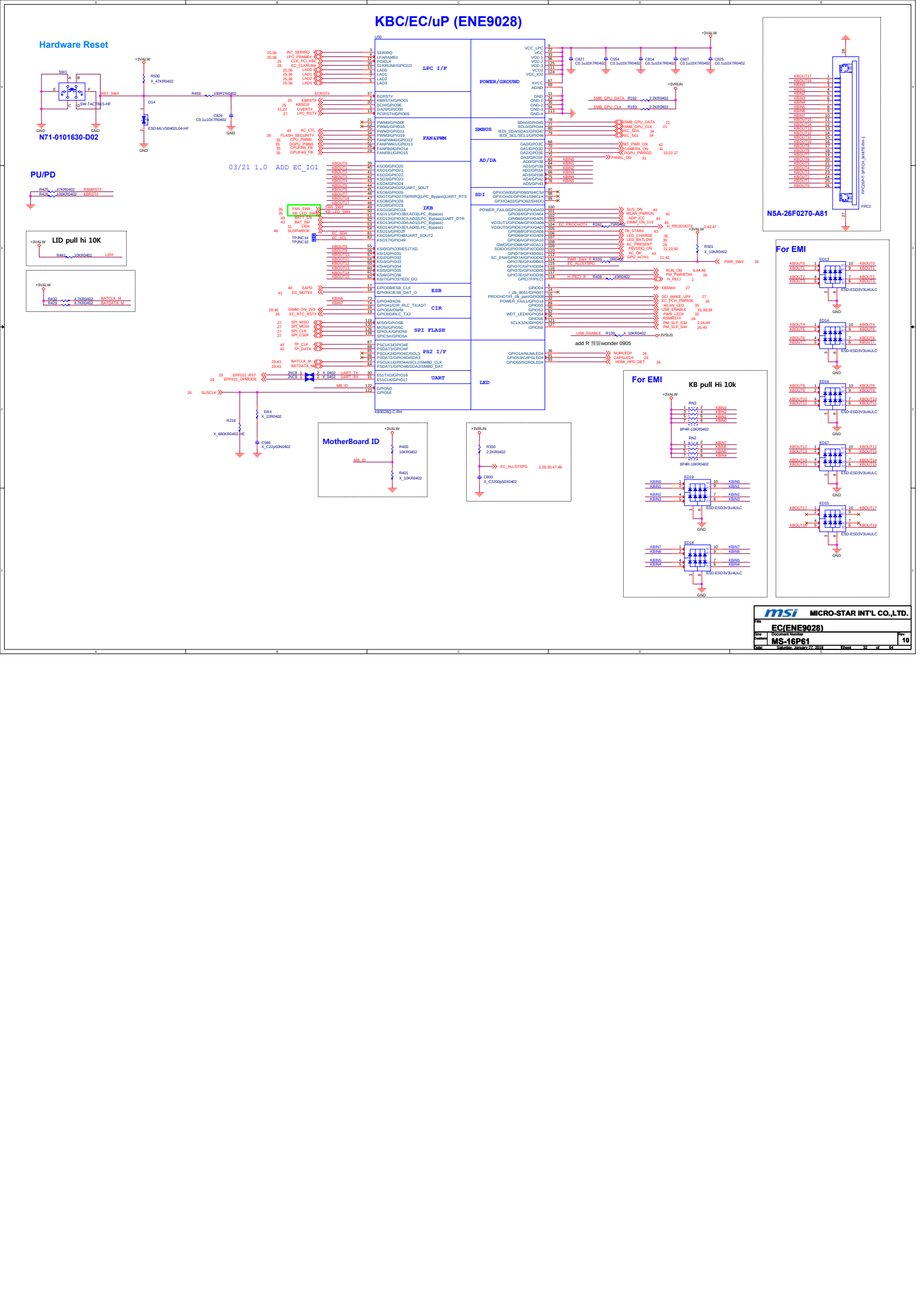
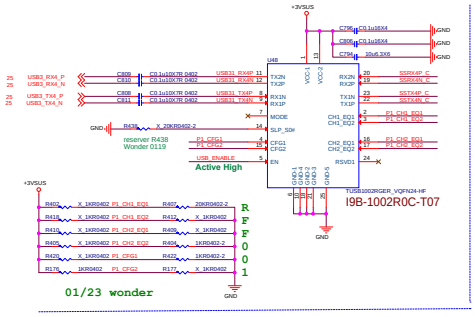
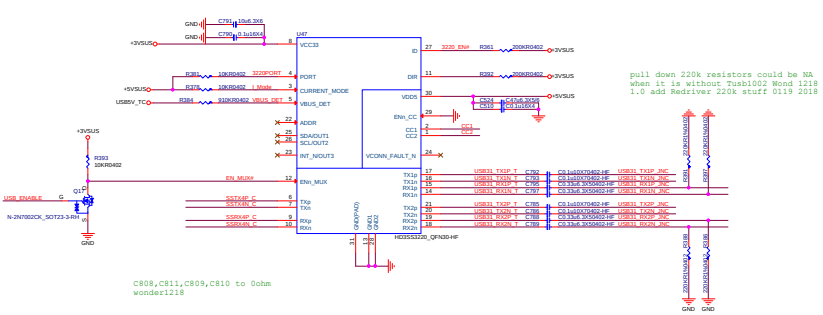
KBC/EC/uP (ENE9028)

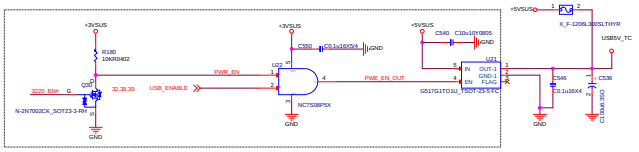


USB3.1 TYPE C

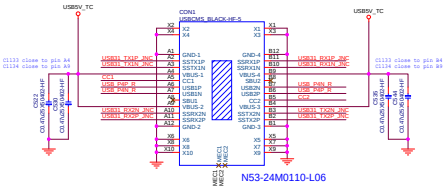




PWR Switch

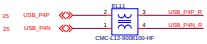


Type-C Connector

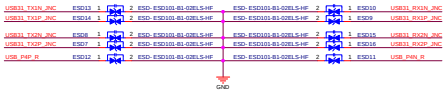


Port =1(DFP mode)
Current_Mode =1(3A)
ADDR= NC(GPIO mode)
ENn_MUX=0(Enable)
ENn_CC=0(Enable CC Controller)
ID: OD output =0 when CC pin detected device attachment

USB20 CMC



ESD



File	Skylake(HOST)
Size	Custom
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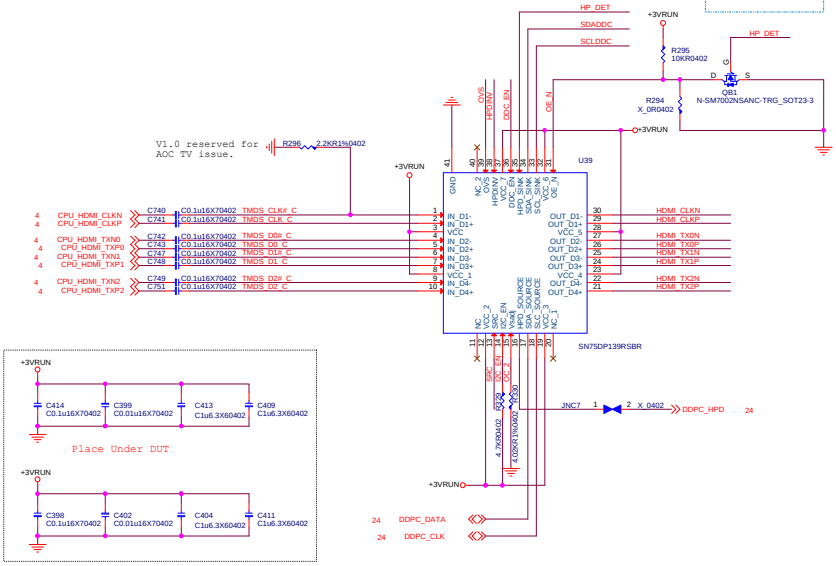
HDMI Level Shifter

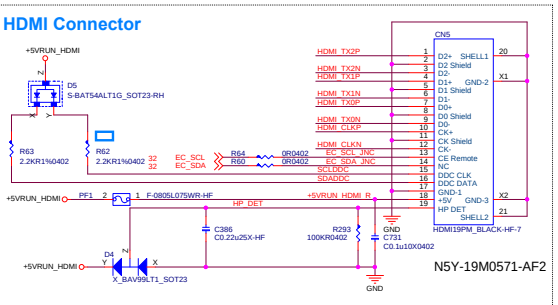
HPD_SNK Internal PD 130kohm

ESD 10KV

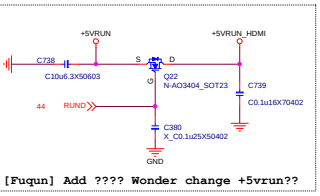
HP_DET	
PLUGGED	5V
UNPLUGGED	0V



HDMI Connector

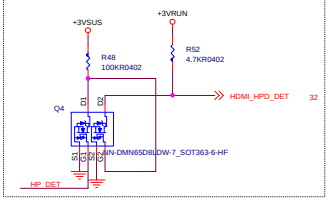


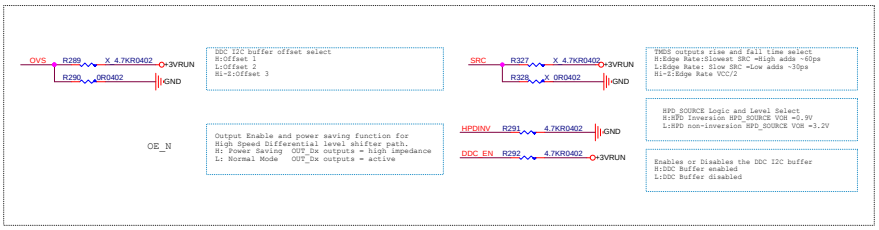
N5Y-19M0571-AF2



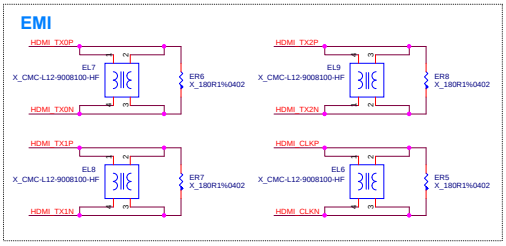
[Fuqun] Add ???? Wonder change +5vrun??

HPD Level Shift 5V to 3V





EMI



msi	MICRO-STAR INT'L CO.,LTD.		
Title	HDMI DP139		
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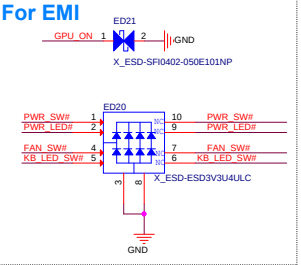
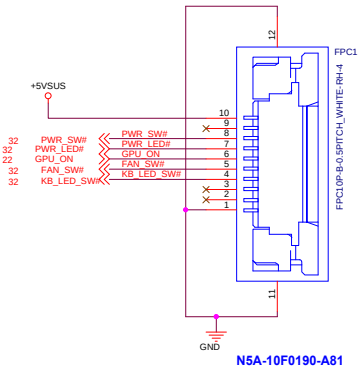
CPU FAN/GPU FAN/POWER Switch

Power Switch Connector

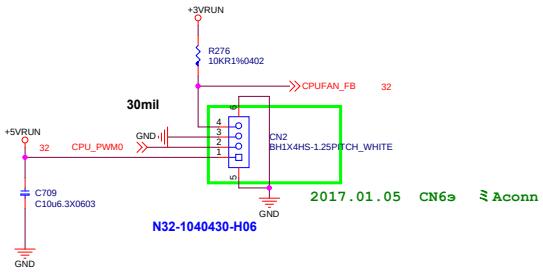
For EMI



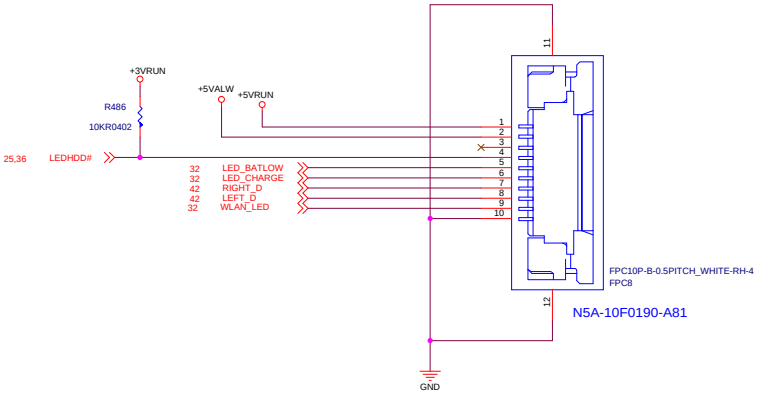


N5A-10F0190-A81

CPU FAN

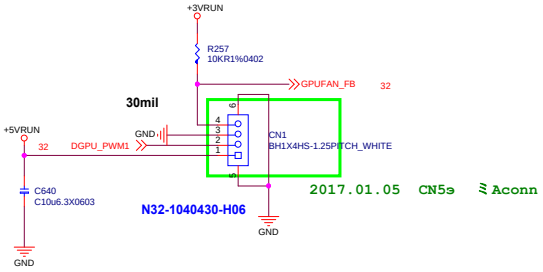


Switch connector



N5A-10F0190-A81

DGPU FAN



msi MICRO-STAR INT'L CO.,LTD.		
Title: CPU FAN/BTB CONN/LED		
Size: Custom	Document Number: MS-16P61	Rev: 10
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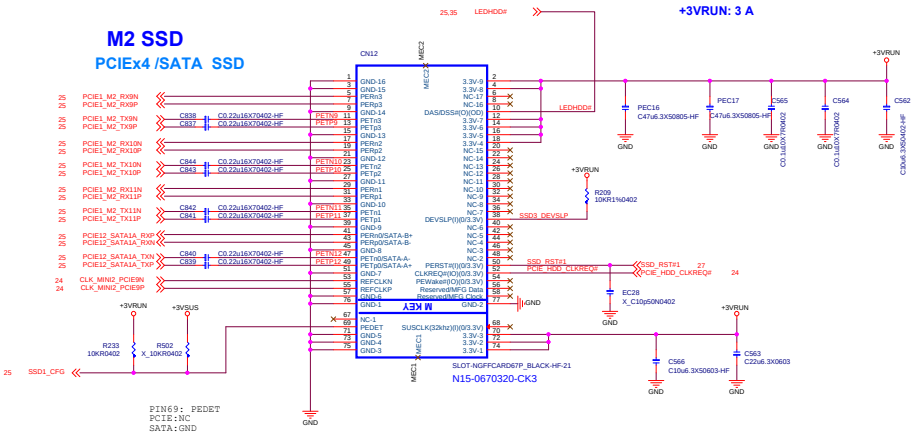
M2 SSD

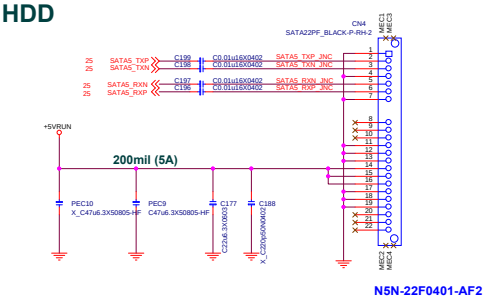
PCIEx4 /SATA SSD



40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

E2B-16J1010-A89

HDD



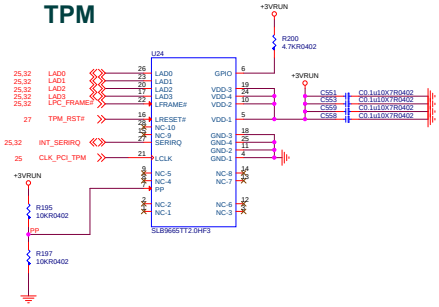
(Must used the gold fresh type)

RU20 E43-1205022-H29 RUBBER

RU21 E43-1205022-H29 RUBBER

03/21 1.0 Add E43-1205022-H29 脸捣

TPM



Title	M2 SSD/HDD/TPM
Size	Custom
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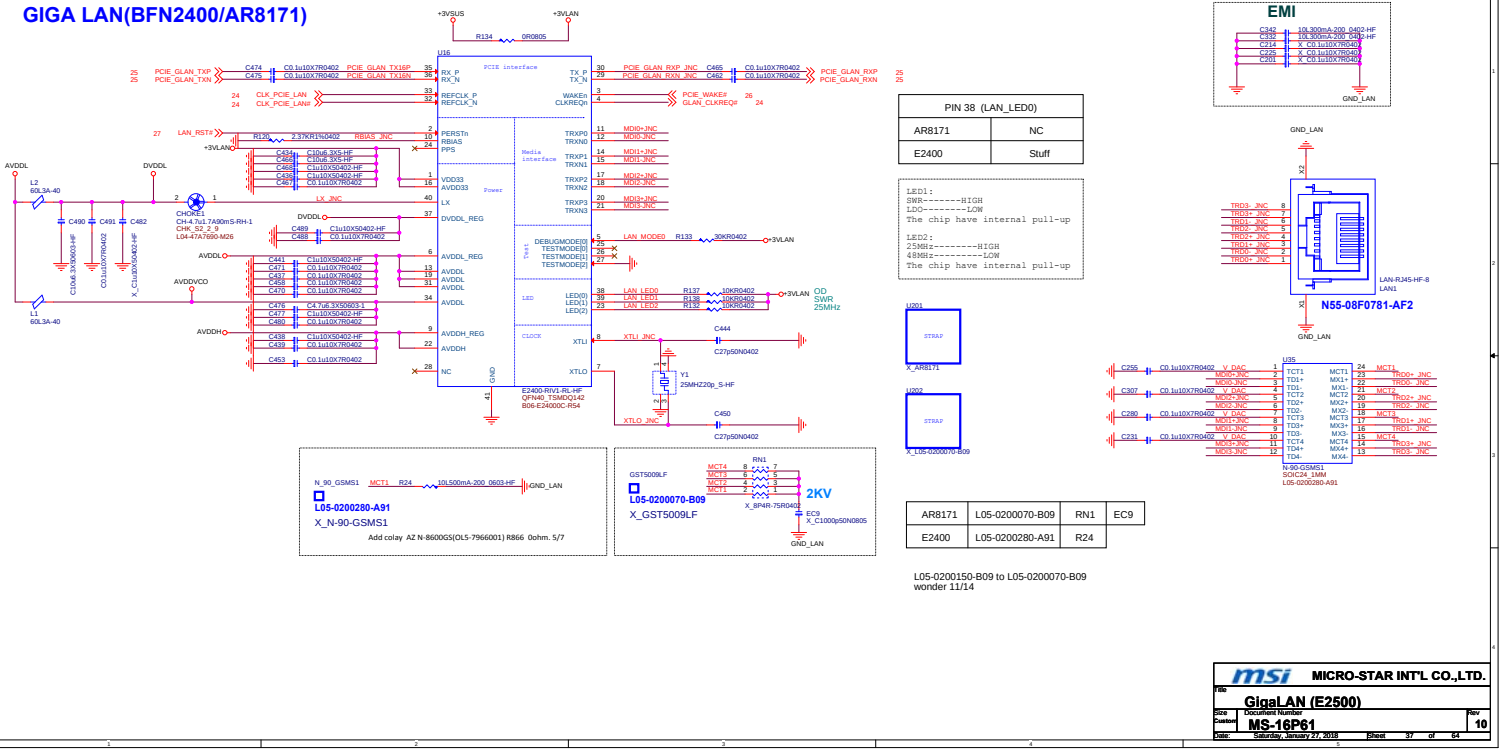
MICRO-STAR INT'L CO.,LTD.

GIGA LAN(BFN2400/AR8171)



PIN 38 (LAN_LED0)	
AR8171	NC
E2400	Stuff

```
LED1:
SWR-------HIGH
LDO--------LOW
The chip have internal pull-up

LED2:
25MHz--------HIGH
48MHz--------LOW
The chip have internal pull-up
```


AR8171	L05-0200070-B09	RN1	EC9
E2400	L05-0200280-A91	R24	

L05-0200150-B09 to L05-0200070-B09
wonder 11/14

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	GigaLAN (E2500)		
Size: Custom	Document Number: MS-16P61		Rev: 10
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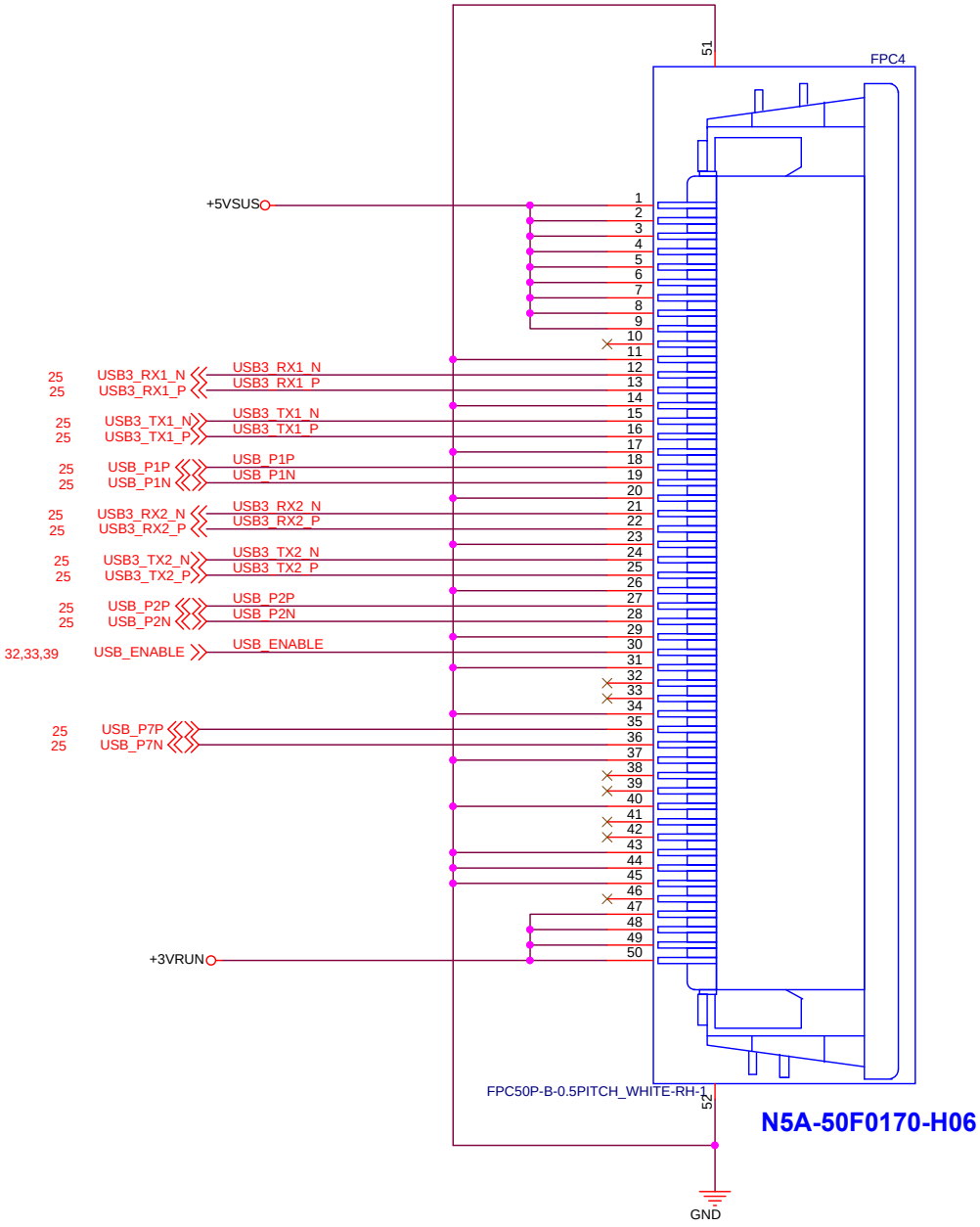

MICRO-STAR INT'L CO.,LTD.

Title: USB 3.0 connector

Size	Document Number	Rev
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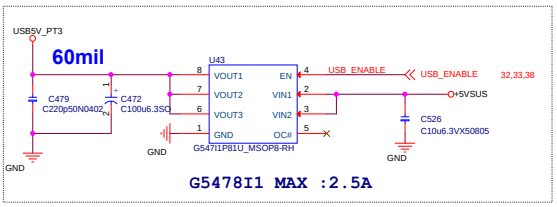
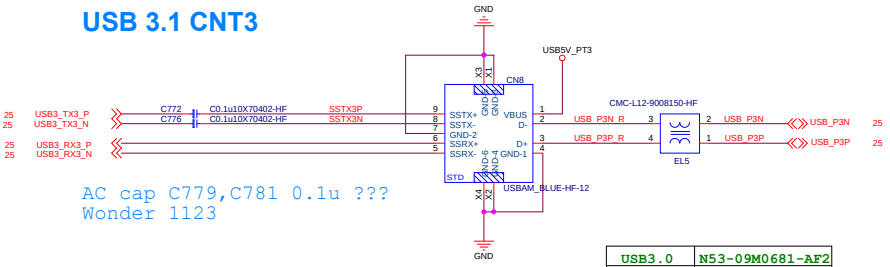
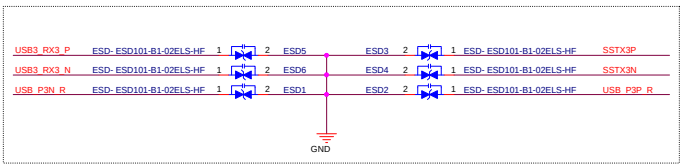
USB 3.1 CNT3





AC cap C779,C781 0.1u ???
Wonder 1123

USB3.0	N53-09M0681-AF2
USB3.0_LED	N53-13M0031-L06



MICRO-STAR INT'L CO.,LTD.

Title: USB 3.1 connector

Size: Custom | Document Number: MS-16P61 | Rev: 10

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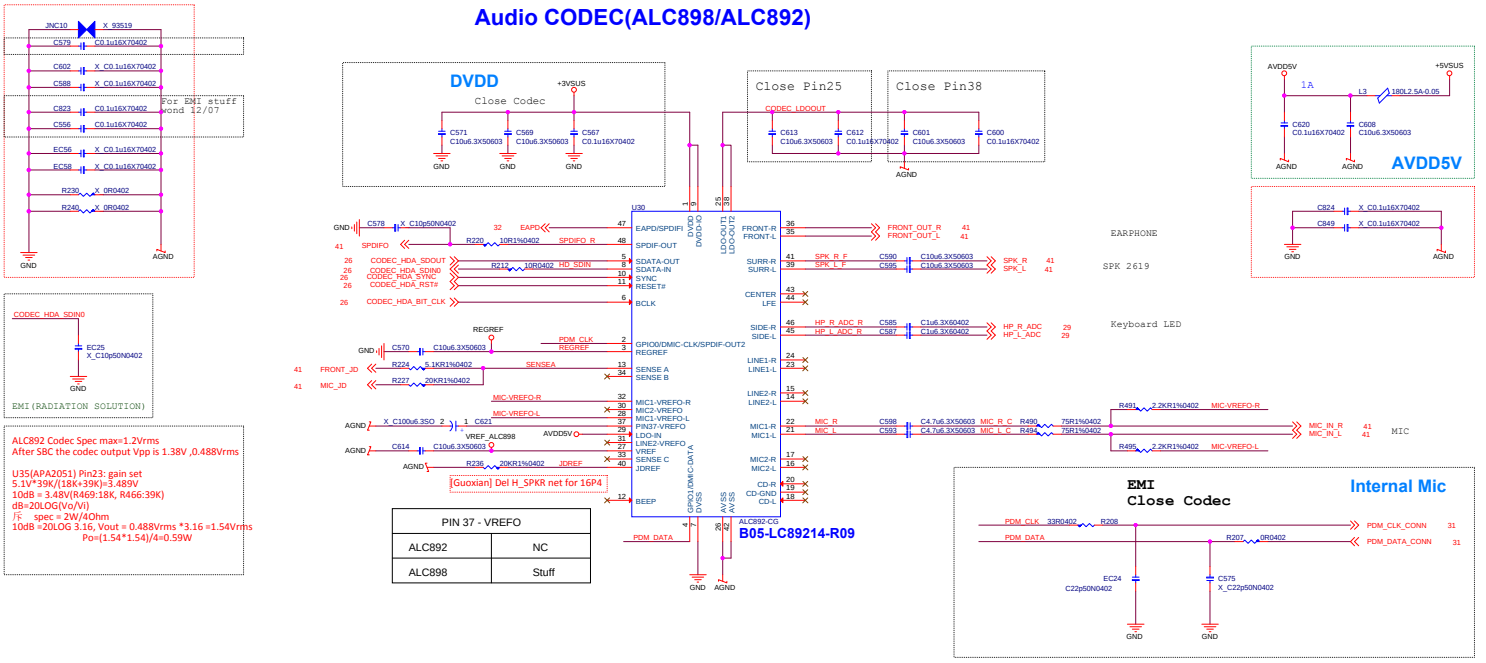
Audio CODEC(ALC898/ALC892)



Title	DGPU_GPU DECOUPLING
Size	Document Number: MS-16P61/17C61
Rev	10
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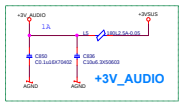
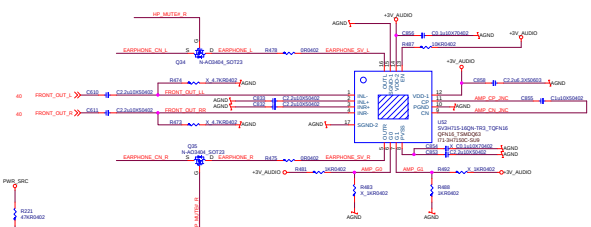
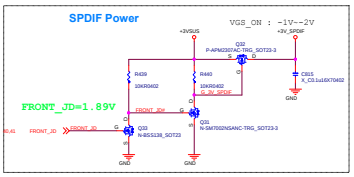
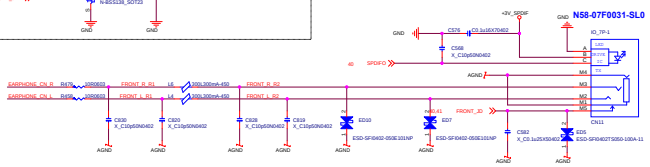
MICRO-STAR INT'L CO.,LTD.

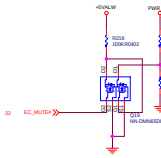




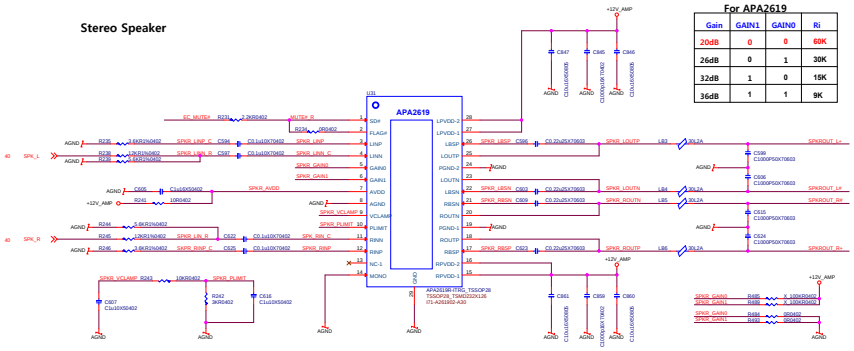
AMP_G1	AMP_G0	GAIN(dB)
L	L	-6
L	H	0
H	L	3
H	H	6





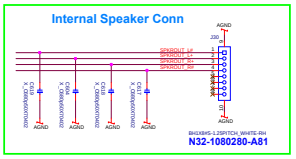


Stereo Speaker

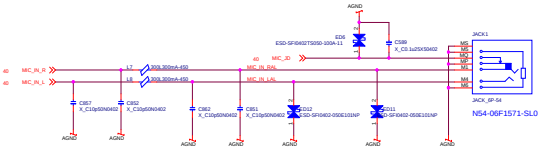


For APA2619			
Gain	GAIN1	GAIN0	Ri
20dB	0	0	60K
26dB	0	1	30K
32dB	1	0	15K
36dB	1	1	9K

Internal Speaker Conn

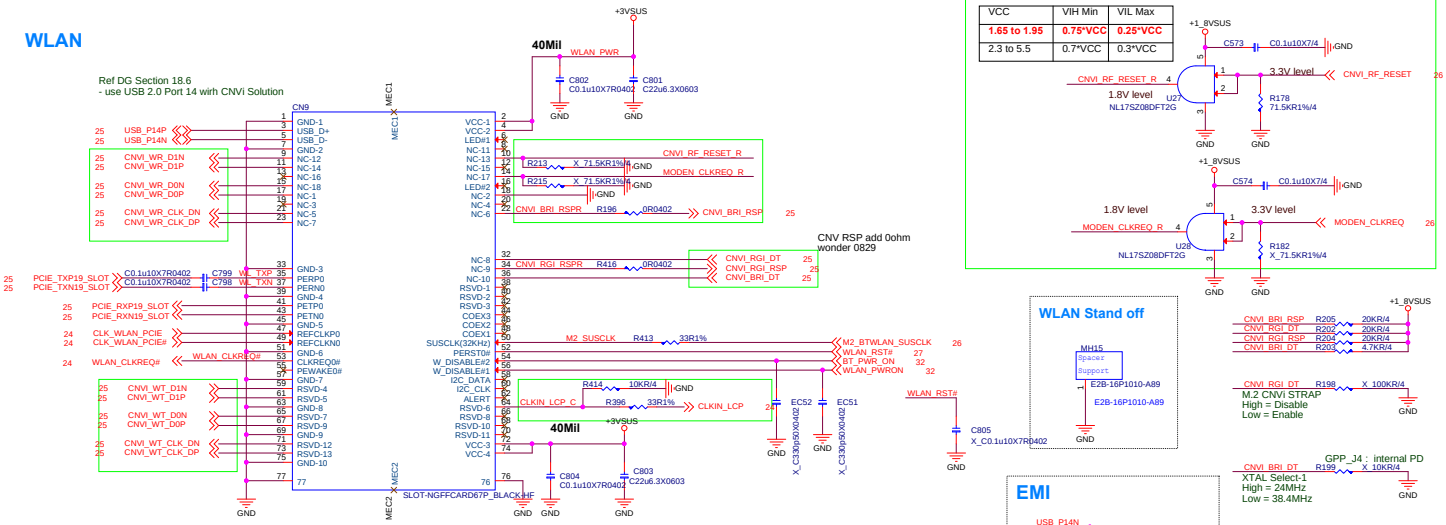


CODEC	
L	–
L	+
R	+
R	–
L+	–
L+	+
L#	+
L#	–
R+	–
R+	+
R#	–
R#	+



WLAN /Touch Pad

WLAN



N15-0670260-L06

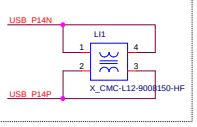
SLOT_NGFFCARD67_15

PN : T70-7SZ0870-O05
AND Gate/ NL17SZ08DFT2G

VCC	VIH Min	VIL Max
1.65 to 1.95	0.75*VCC	0.25*VCC
2.3 to 5.5	0.7*VCC	0.3*VCC

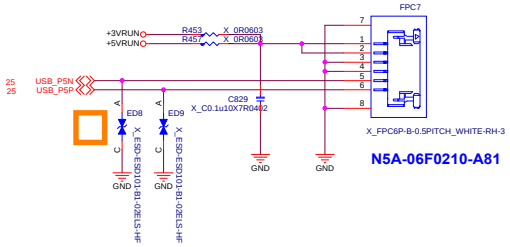
WLAN Stand off

EMI



Workstation:FingerPrint :S78-3701000-SD2

VDD: 3.3V Stuff R453

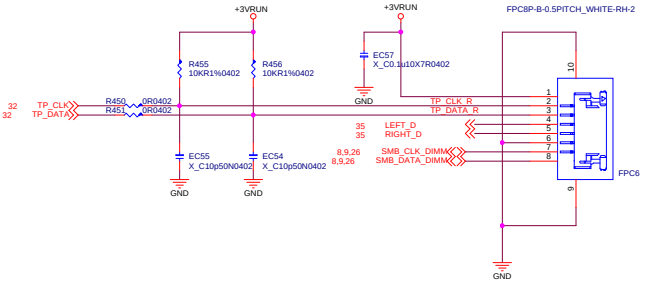


N5A-06F0210-A81

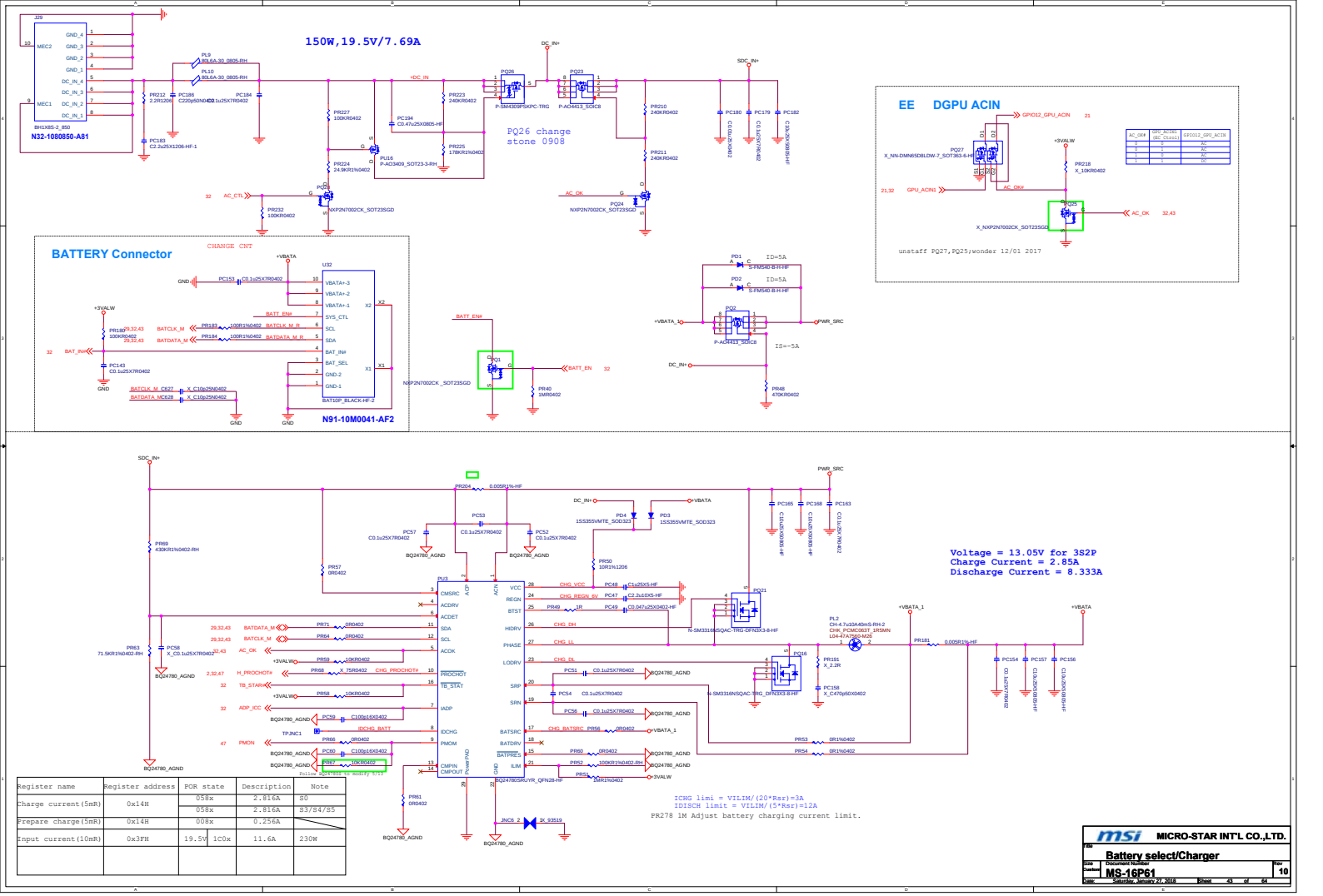
Touch Pad

03/20 FPC12 change to N5A-08F0130-H06

N5A-08F0130-H06



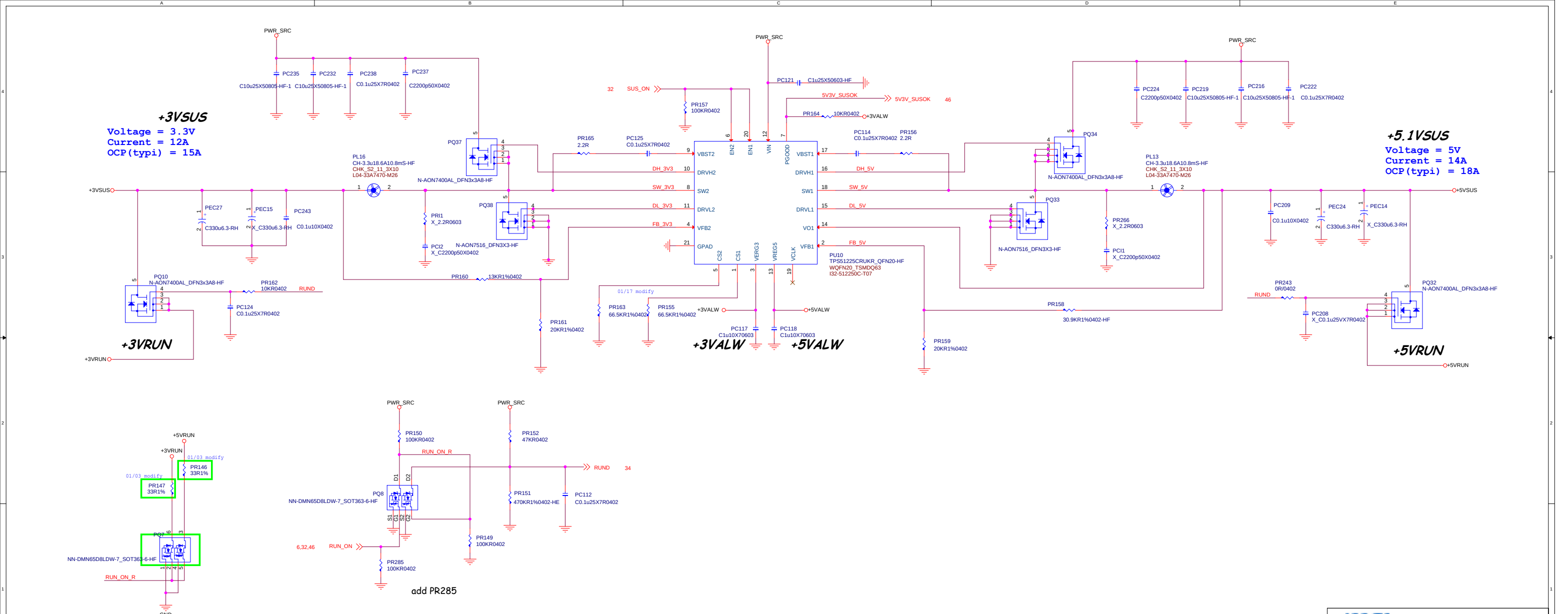
msi	MICRO-STAR INT'L CO.,LTD.		
Title	WLAN/Touch Pad/FP		
Size: Custom	Document Number: MS-16P61		Rev: 10
Date: Saturday, January 27, 2018	Sheet 42 of 64		



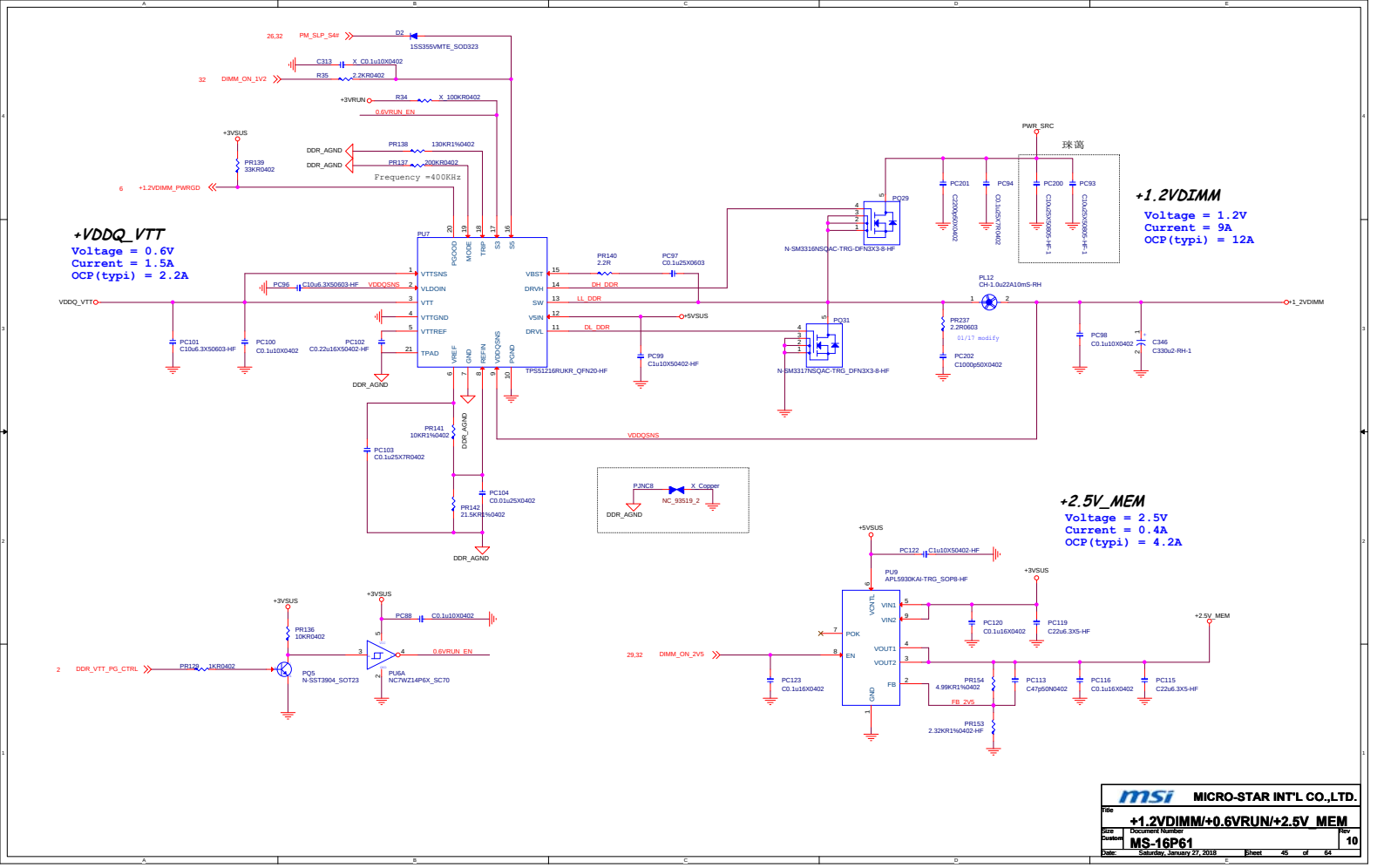
Register name	Register address	POR state	Description	Note
Charge current(5mR)	0x14H	058x	2.816A	S0
		058x	2.816A	S3/S4/S5
Prepare charge(5mR)	0x14H	008x	0.256A	
Input current(10mR)	0x3FH	19.5V 1C0x	11.6A	230W

Title	Battery select/Charger
Size	Document Number
Custom	MS-16P61
Date	Saturday, January 27, 2018
Sheet	43 of 64

MICRO-STAR INT'L CO.,LTD.



MICRO-STAR INT'L CO.,LTD.	
Title	System Power
Size Custom	Document Number: MS-16P61/17C61
Rev	10
Date	Saturday, January 27, 2018
Sheet	44 of 64



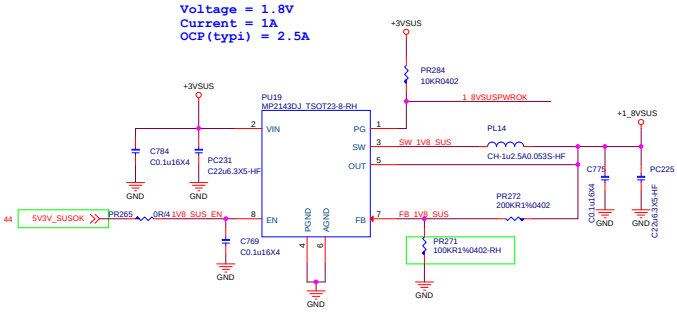
Title	+1.2VDIMM/+0.6VRUN/+2.5V_MEM
Size / Custom	Document Number: MS-16P61
Rev	10
Date:	Saturday, January 27, 2018
Sheet	45 of 64

MICRO-STAR INT'L CO.,LTD.

待預留+1_8VSUS

+1_8VSUS

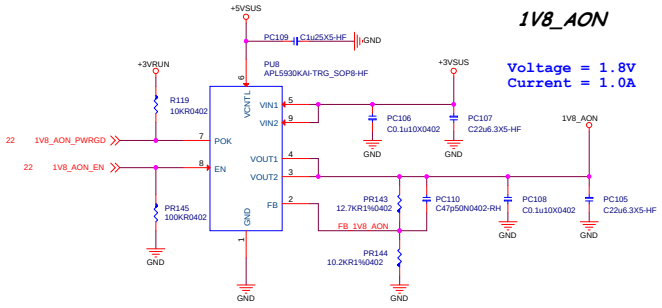
Voltage = 1.8V
Current = 1A
OCP(typi) = 2.5A



Reserve for1.8V_AON

1V8_AON

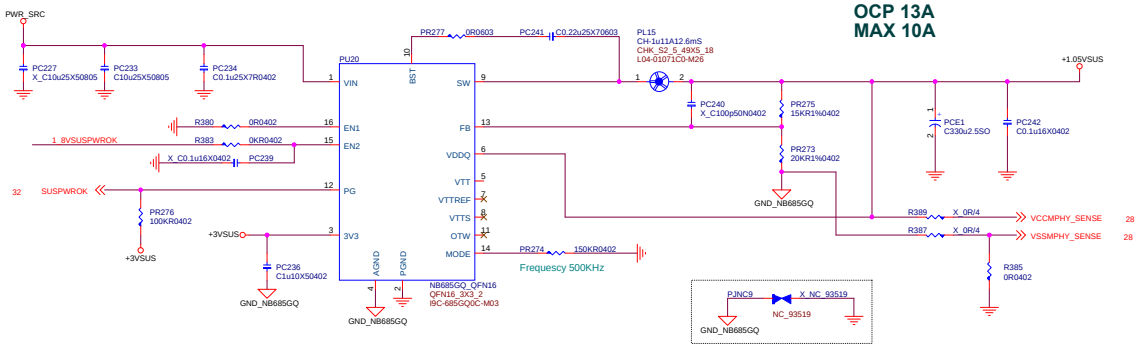
Voltage = 1.8V
Current = 1.0A



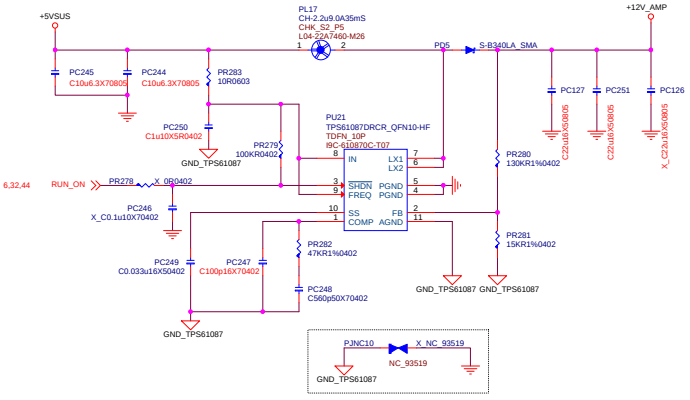
+1.05VSUS enable
1_8VSUSPWROK

+1.05VSUS

OCP 13A
MAX 10A

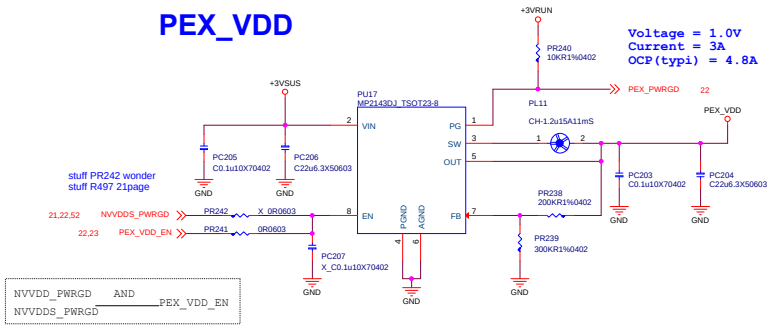


+12V_AMP



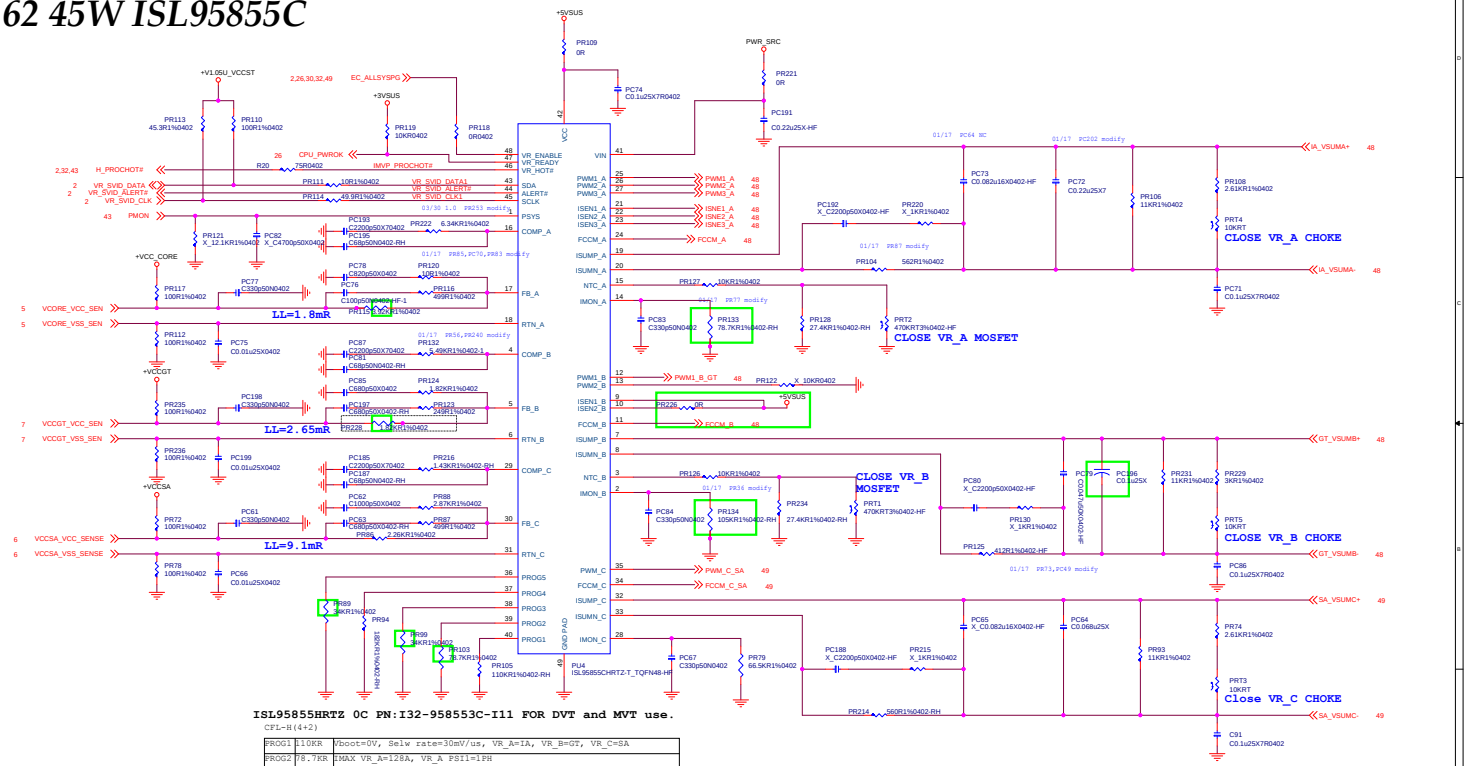
PEX_VDD

Voltage = 1.0V
Current = 3A
OCP(typi) = 4.8A



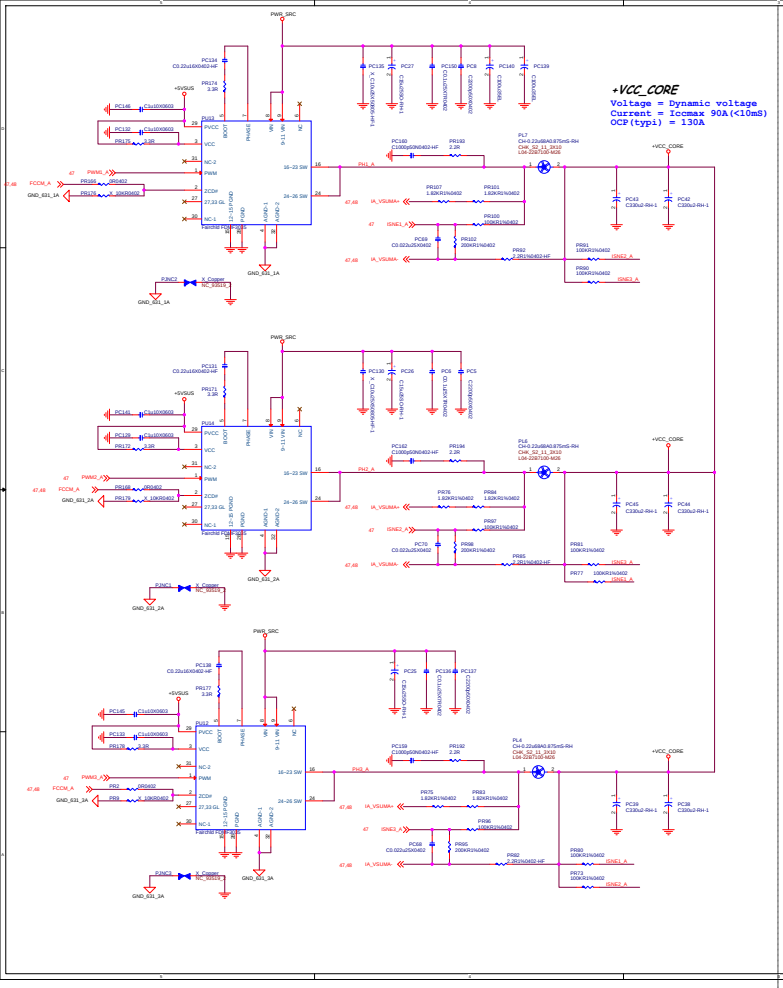
msi	MICRO-STAR INT'L CO.,LTD.	
Title	+1.05VSUS/+PEX_VDD/+1_8VSUS	
Size: Custom	Document Number: MS-16P61	Rev: 10
Date: Saturday, January 27, 2018	Sheet 46 of 64	

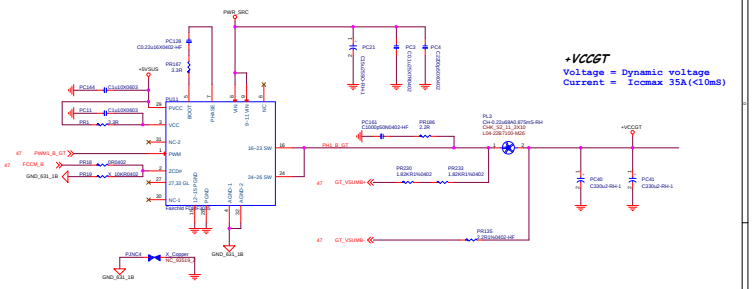
Coffee Lake H-line
62 45W ISL95855C



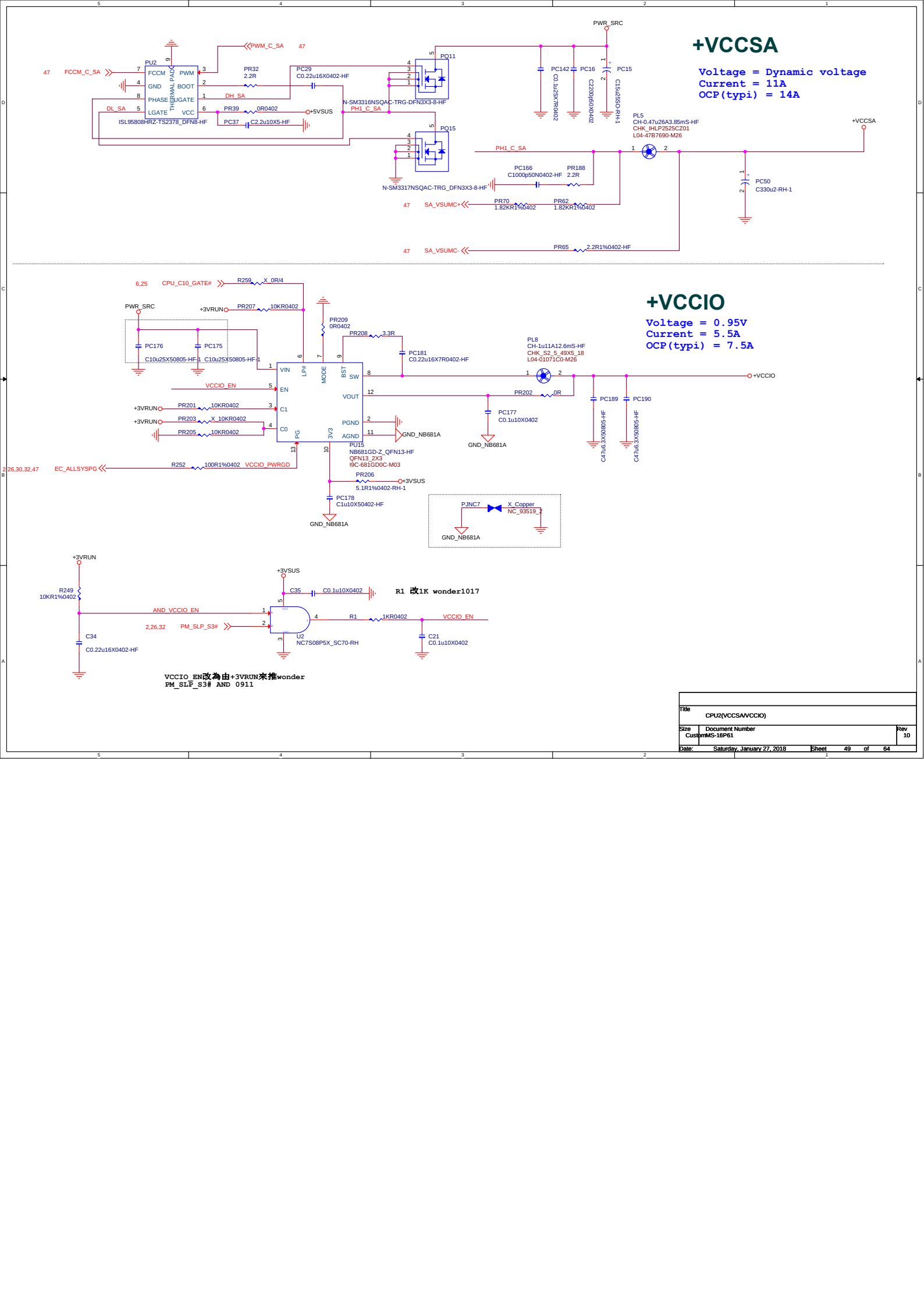
PROG1	110KR	Vboot=0V, Selw rate=30mV/us, VR_A=IA, VR_B=GT, VR_C=SA
PROG2	78.7KR	IMAX VR_A=128A, VR_A FSI1=1PH
PROG3	34KR	IMAX VR_B=70A, DROOP VR_B Active
PROG4	182KR	DROOP VR_A Active, DROOP VR_C Active, VR_A VR_B Frequency=750kHz
PROG5	64KR	IMAX VR_C=17A, Frequency=450kHz

Title	CPU Power (ISL95855)		
Size	Document Number		Rev
Custom	MS-16P61		10
Date:	Saturday, January 27, 2018	Sheet 47 of 64	





Title	GPU(VCore/VCCGT)	
Size	Document Number	Rev
	Custom_16P01	1.0
Date	Saturday, January 27, 2018	Sheet 48 of 64


+VCCSA
Voltage = Dynamic voltage
Current = 11A
OCP(typi) = 14A
PWR_SRC
PU2
ISL95808HRZ-TS2378_DFN8-HF
PWM_C_SA
FCCM_C_SA
DH_SA
DL_SA
PR32 2.2R
PC29 C0.22u16X0402-HF
PR39 0R0402
+5VSUS
PC37 C2.2u10X5-HF
PQ11
PQ15
N-SM3316NSQAC-TRG-DFN3X3-8-HF
PH1_C_SA
N-SM3317NSQAC-TRG_DFN3X3-8-HF
PC142 C0.1u25X7R0402
PC16 C2200p50X0402
PC15 C15u25SO-RH-1
PL5
CH-0.47u26A3.85mS-HF
CHK_IHLP2525CZ01
L04-47B7690-M26
+VCCSA
PC166 C1000p50N0402-HF
PR188 2.2R
PR70 1.82KR1%0402
PR62 1.82KR1%0402
SA_VSUMC+
SA_VSUMC-
PR65 2.2R1%0402-HF
PC50 C330u2-RH-1
+VCCIO
Voltage = 0.95V
Current = 5.5A
OCP(typi) = 7.5A
CPU_C10_GATE#
R259 X_0R/4
PR207 10KR0402
PR209 0R0402
PR208 3.3R
PC181 C0.22u16X7R0402-HF
PC176 C10u25X50805-HF-1
PC175 C10u25X50805-HF-1
VCCIO_EN
PR201 10KR0402
PR203 X_10KR0402
PR205 10KR0402
PU15
NB681GD-Z_QFN13-HF
QFN13_2X3
I9C-681GD0C-M03
PR202 0R
PC177 C0.1u10X0402
PL8
CH-1u11A12.6mS-HF
CHK_S2_5_49X5_18
L04-01071C0-M26
PC189 C47u6.3X5080S-HF
PC190 C47u6.3X5080S-HF
EC_ALLSYSPG
R252 100R1%0402
VCCIO_PWRGD
PR206 5.1R1%0402-RH-1
PC178 C1u10X50402-HF
GND_NB681A
PJNC7
X_Copper
NC_93519_2
+3VRUN
R249 10KR1%0402
C34 C0.22u16X0402-HF
+3VSUS
C35 C0.1u10X0402
R1 改1K wonder1017
AND_VCCIO_EN
PM_SLP_S3#
R1 1KR0402
C21 C0.1u10X0402
U2
NC7S08P5X_SC70-RH
VCCIO_EN改為由+3VRUN來推wonder
PM_SLP_S3# AND 0911
Title
CPU2(VCCSA/VCCIO)
Size
Custom
Document Number
MS-16P61
Rev
10
Date:
Saturday, January 27, 2018
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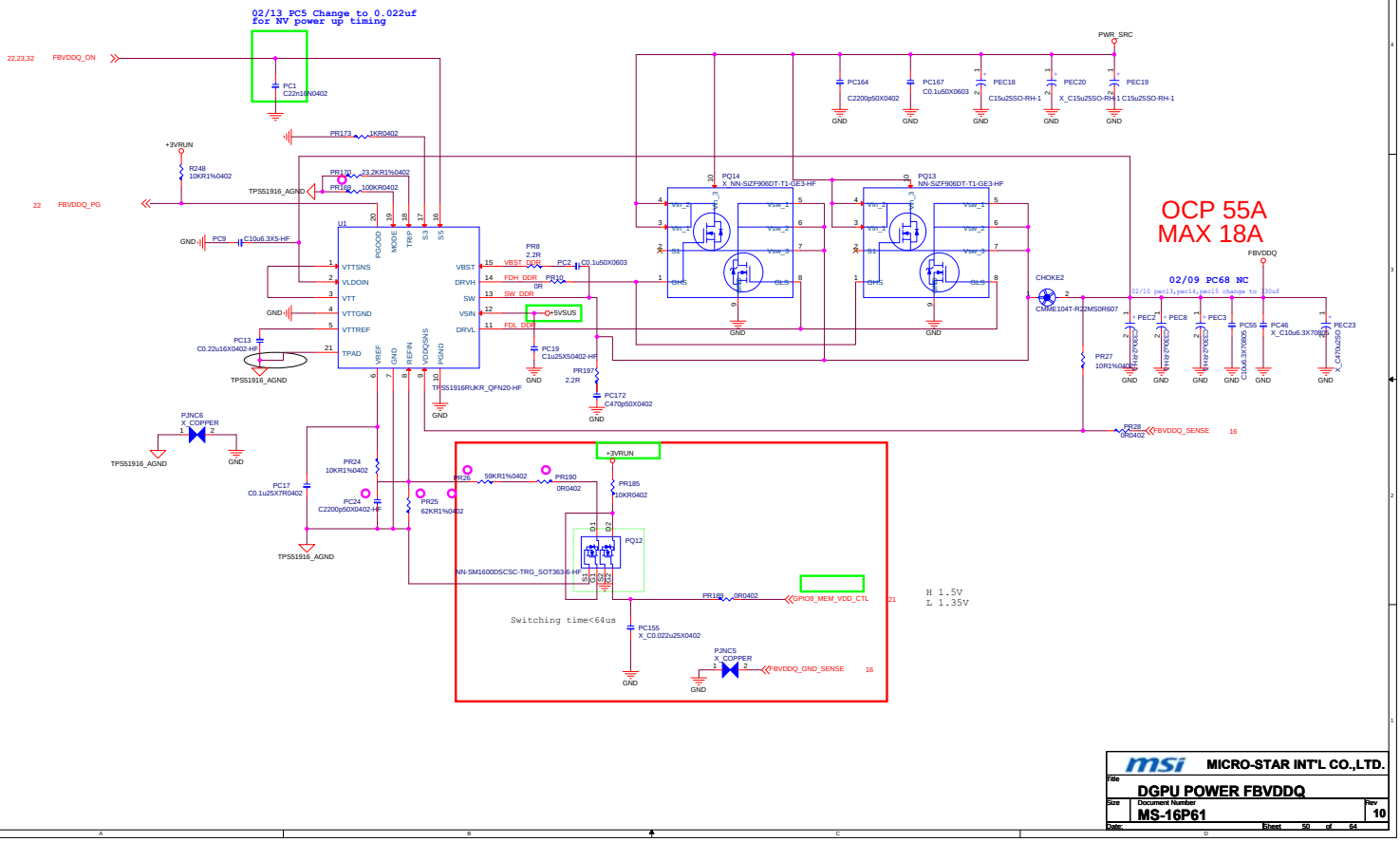
of
64

FBVDDQ



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU POWER FBVDDQ			
Size	Document Number: MS-16P61		Rev: 10
Date:		Sheet 50 of 64	

DGPU POWER / UP9509P

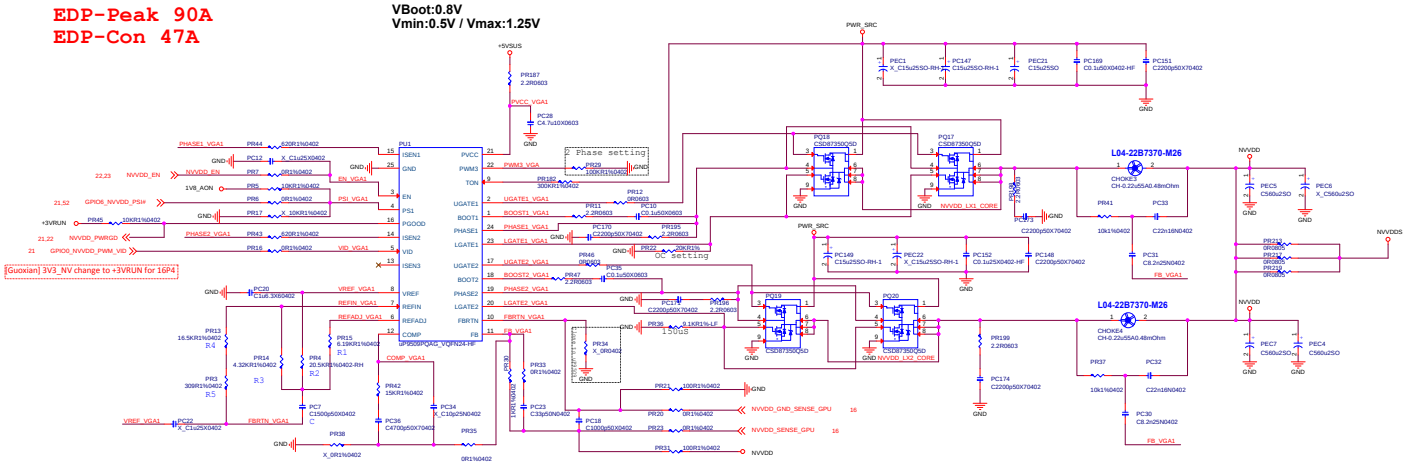
EDP-Peak 90A

EDP-Con 47A

DGPU POWER NVVDD

VBoot:0.8V

Vmin:0.5V / Vmax:1.25V



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_GPU DECOUPLING		
Size:	Document Number: MS-16P61/17C61	Rev: 1.0
Date: Saturday, January 27, 2018	Sheet 51 of 64	

DGPU POWER / UP1666P

EDP-Peak 74A

EDP-Con 28A

DGPU POWER NVVDDS

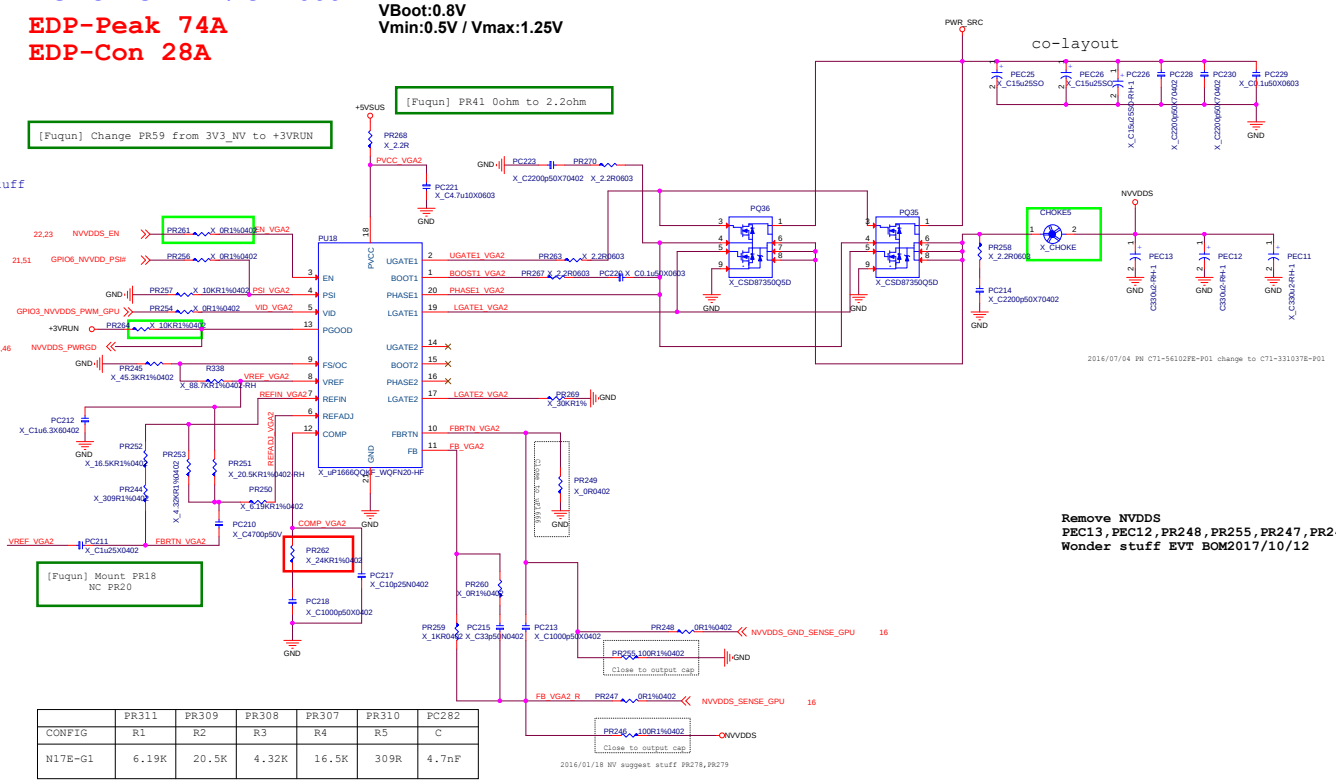
VBoot:0.8V

Vmin:0.5V / Vmax:1.25V

[Fuqun] Change PR59 from 3V3_NV to +3VRUN

[Fuqun] PR41 0ohm to 2.2ohm

Remove NVDDS
PR261 PR264 unstuff
wonder 0918



	PR311	PR309	PR308	PR307	PR310	PC282
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	4.7nF

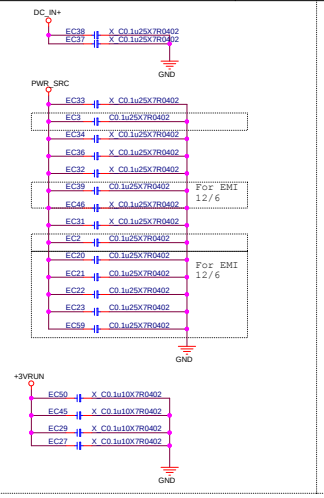
Remove NVDDS
PEC13,PEC12,PR248,PR255,PR247,PR246
Wonder stuff EVT BOM2017/10/12

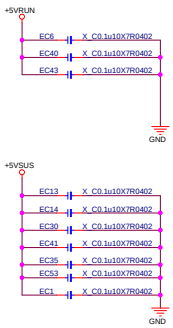
MICRO-STAR INT'L CO.,LTD.

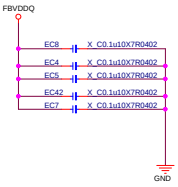
Title: DGPU_GPU DECOUPLING

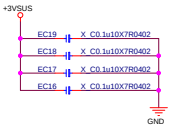
Size: | Document Number: MS-16P61/17C61 | Rev: 10

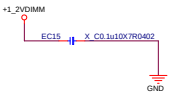
Date: Saturday, January 27, 2018 | Sheet 52 of 64

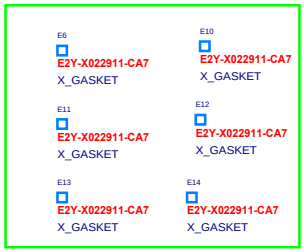






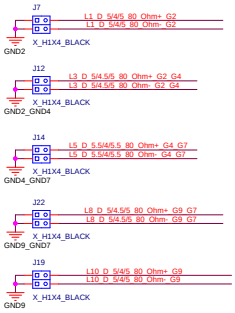




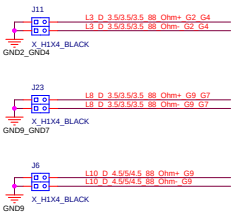


Add E4,E5,E6,E7,E8,E9for EMI.5/22

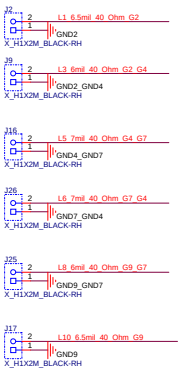
80 OHM / CLK/WCK/USB3.1



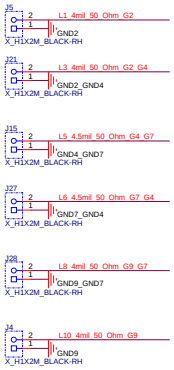
88 OHM /DDR4 CLK/DQS



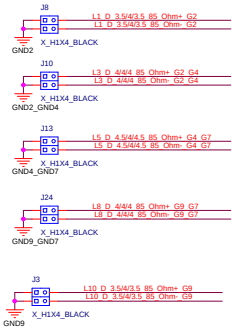
40 OHM DDR4 :CTL/ADD GPU:FBA/FBB DQ DB,



50OHM DDR4:RST/DQ/ECC/HPD/STRAP/SPI

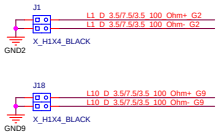


85 OHM /SATA /PCIE/ EDP/CNVI USB /HDMI/DP/DMI/CLK/PEG



90 OHM USB 3.1 MUX/XTLIN/OUT

100 OHM LAN



msi	MICRO-STAR INT'L CO.,LTD.	
Title: EMI		
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CPU Holes

MCPU1 H_R142D126BR197_MB_N
MCPU2 H_R142D126BR197_MB_N
MCPU5 H_R142D126BR197_MB_N
GND

H_R197D91_N MH7 X_HOLES_R236D98_1034
H_R197D91_N MH13 X_HOLES_R236D98_1034
H_R197D91_N MH6 X_HOLES_R236D98_1034
H_R197D91_N MH9 X_HOLES_R236D98_1034
H_R197D91_N MH1 X_HOLES_R236D98_1034
H_R197D91_N MH12 X_HOLES_R236D98_1034
MH2 H_R197D91_N
H_R197D91_N MH3 X_HOLES_R236D98_1034
GND

MH10 .VER.0A-.MECH,NB,CU,STANDOFF,M2.5/*D4.5*L3.5+1.1mm,FOR MS-16P1,.RoHS COMPLIANCE
GND
E2B-16P1020-A89

FM25 FM28 FM27 FM14
FM17 FM1 FM5 FM10
FM29 FM9 FM2 FM8
FM11 FM22 FM21 FM24
FM3 FM18 FM31 FM15
FM12 FM6 FM30 FM20
FM13 FM4 FM32 FM16
FM26 FM23 FM7 FM19

npth_80 MH4 X_npth_80
npth_80 MH5 X_npth_80
H_R197D118_V3_N MH11 X_H_R197D118_V3_N
H_R236D157_V3_N MH8 X_H_R236D157_V3_N
H_R197D91_N MH14 X_HOLES_R236D98_1034
npth_80 XX7 X_npth_80
npth_80 XX8 X_npth_80

160529

RU1 E2Y-4A10711-Y40 X_RUBBER	RU6 E2Y-4A10711-Y40 X_RUBBER	RU10 E2Y-4A10711-Y40 X_RUBBER	RU14 E2Y-4A10711-Y40 X_RUBBER
RU2 E2Y-4A10711-Y40 X_RUBBER	RU5 E2Y-4A10711-Y40 X_RUBBER	RU9 E2Y-4A10711-Y40 X_RUBBER	RU13 E2Y-4A10711-Y40 X_RUBBER
RU3 E2Y-4A10711-Y40 X_RUBBER	RU8 E2Y-4A10711-Y40 X_RUBBER	RU12 E2Y-4A10711-Y40 X_RUBBER	RU16 E2Y-4A10711-Y40 X_RUBBER
RU4 E2Y-4A10711-Y40 X_RUBBER	RU7 E2Y-4A10711-Y40 X_RUBBER	RU11 E2Y-4A10711-Y40 X_RUBBER	RU15 E2Y-4A10711-Y40 X_RUBBER
RU17 E2Y-4A10811-Y40 X_RUBBER	RU18 E2Y-4A10811-Y40 X_RUBBER	RU19 E2Y-4A10911-Y40 X_RUBBER	

NPTH_80 XX10 X_NPTH_80
NPTH_80 XX12 X_NPTH_80
NPTH_80 XX9 X_NPTH_80
NPTH_80 XX11 X_NPTH_80

Lay new add 4 loction
wonder 0913

NPTH118 XX1 X_NPTH118
NPTH118 XX3 X_NPTH118
NPTH118 XX4 X_NPTH118
npth_80 XX5 X_npth_80

UME5 CPU BKT — CPU BKT 307-6P10111-HG0
UME6 GPU BKT — GPU BKT 307-6P10211-HG0
UME18 MB MYLAR — MB_mylar E2P-6P11311-Y42
UME15 MB MYLAR — MB_mylar E2P-6P11311-Y42
UME16 MB MYLAR — MB_mylar E2P-6P11311-Y42
UME17 MB MYLAR — MB_mylar E2P-6P11311-Y42

RU27 E2Y-7C11711-Y42 17C6_RUBBER
RU26 E2Y-6P12611-Y42 16P61_RUBBER
RU28 E2Y-0113411-Y40 16P61_RUBBER

UME3 COMPLIANCE MYLAR — X_COMPLIANCE_mylar E2P-4A11411-Y42
UME11 COMPLIANCE MYLAR — X_COMPLIANCE_mylar E2Y-4A11011-Y42

UME1 HDMI Lable — HDMI ROYALTY Y01-RHDMI03-000
UME2 BIOS Lable — BIOS_LABEL G51-N1CO041-A09
For MP

PCB1 PD0-16P6110-H73
PD0-16P6110-H73
Hannstar:PD0-16P6110-H73
TRIPOD: PD0-16P6110-H73

DGPU Holes

MCPU3 MCPU7 MCPU4 MCPU6
H_R142D126BR197_MB_N
GND

E2 X_HS-MS1011-RH
GND

RU23 E2Y-3612111-Y40 X_RUBBER
RU24 E2Y-3612111-Y40 X_RUBBER
RU22 E2Y-7750211-Y40 X_RUBBER
RU25 E2Y-3612111-Y40 X_RUBBER

MICRO-STAR INT'L CO.,LTD.

Title	Screw/ME	
Size: Custom	Document Number: MS-16P61	Rev: 10
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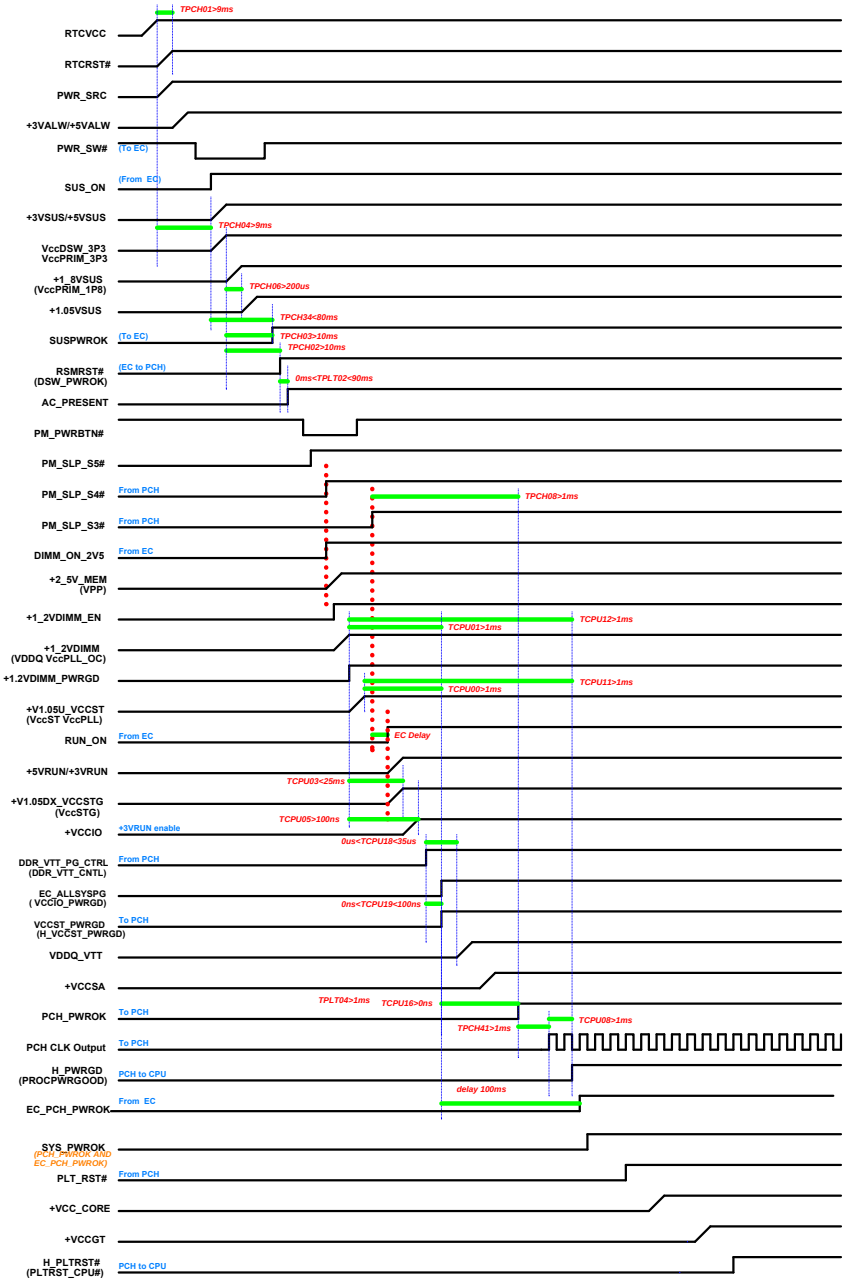
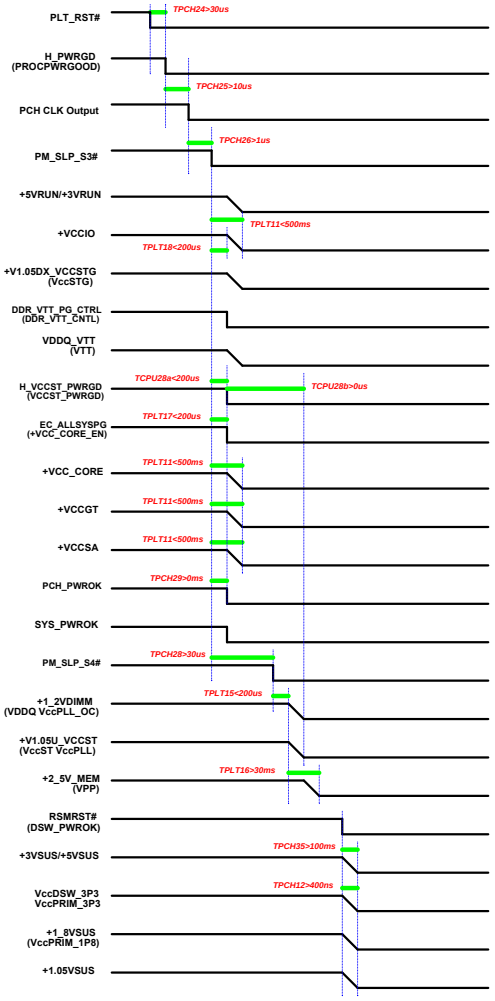
Power on Sequence

G3 -> S0



S0 -> G3



MICRO-STAR INT'L CO.,LTD.		
File: Power on Sequence		
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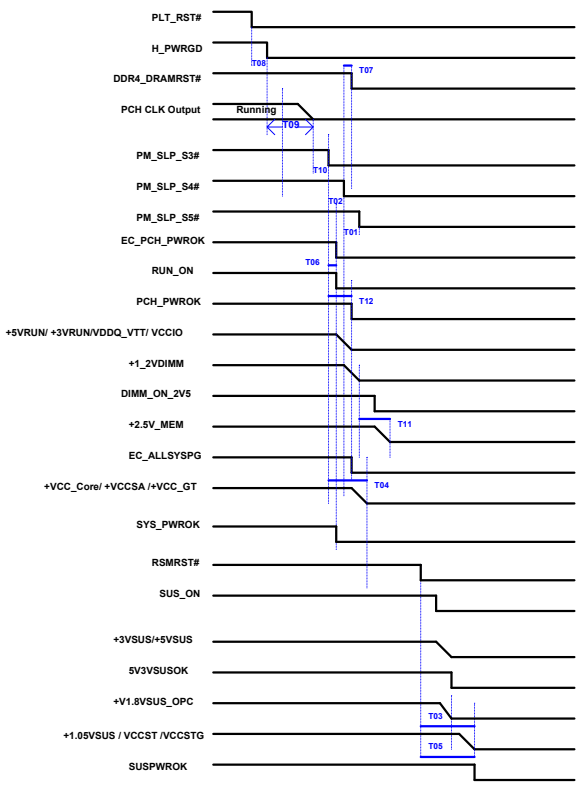
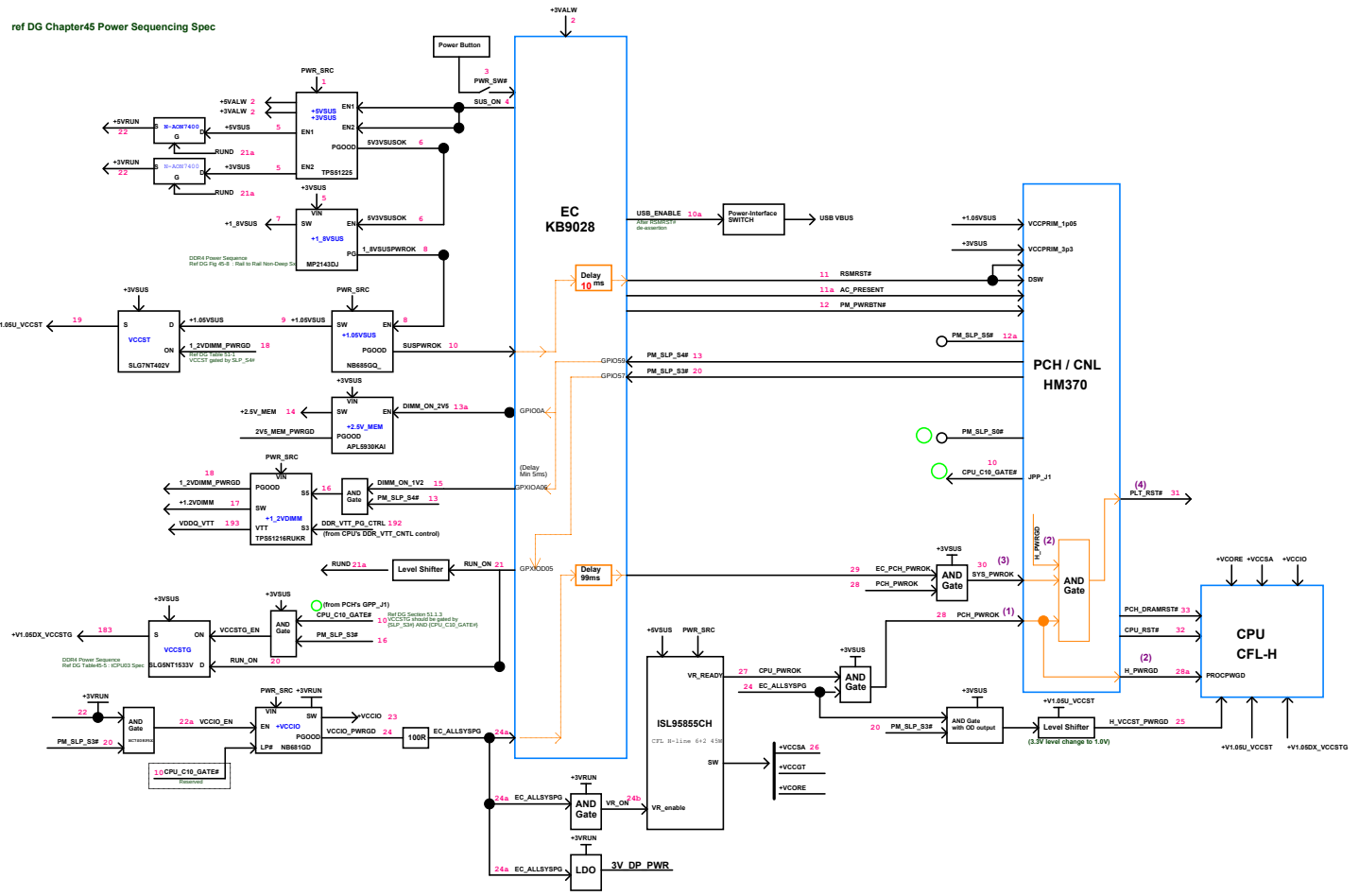
Power down Sequence

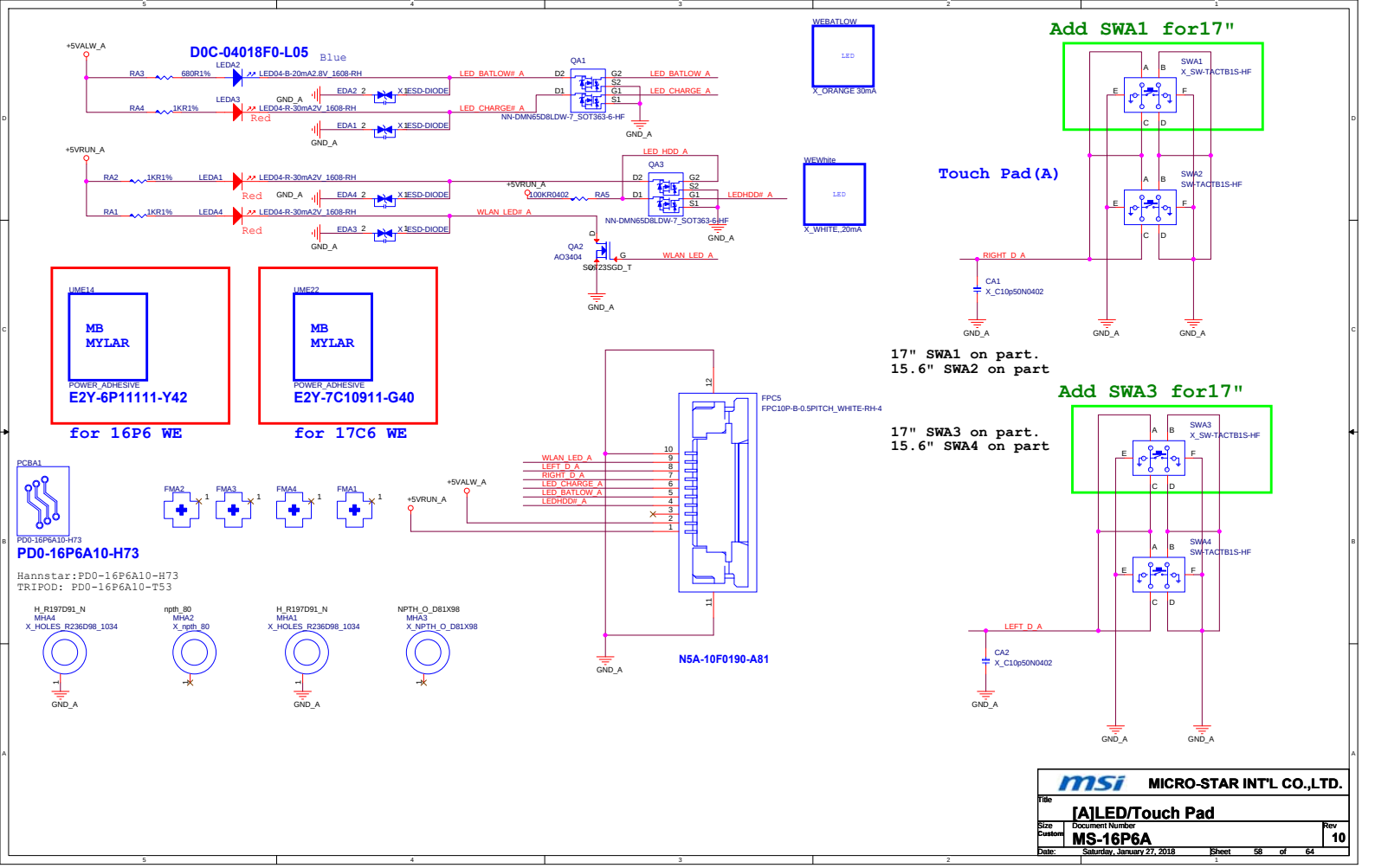
S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

MS-16P6 CFL-H Power on Block Diagram





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Title: [A]LED/Touch Pad

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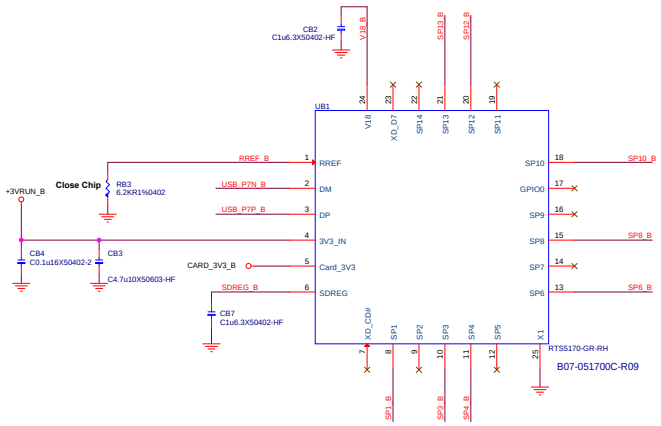
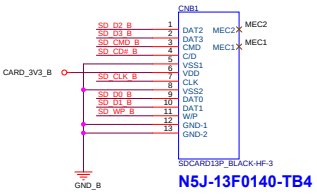
CardReader (RTS5170)

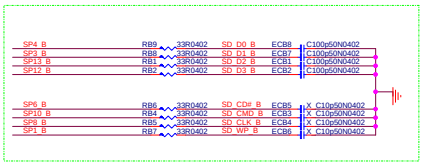


CARD_3V3: 950mA

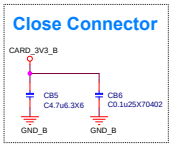


N5J-13F0140-TB4

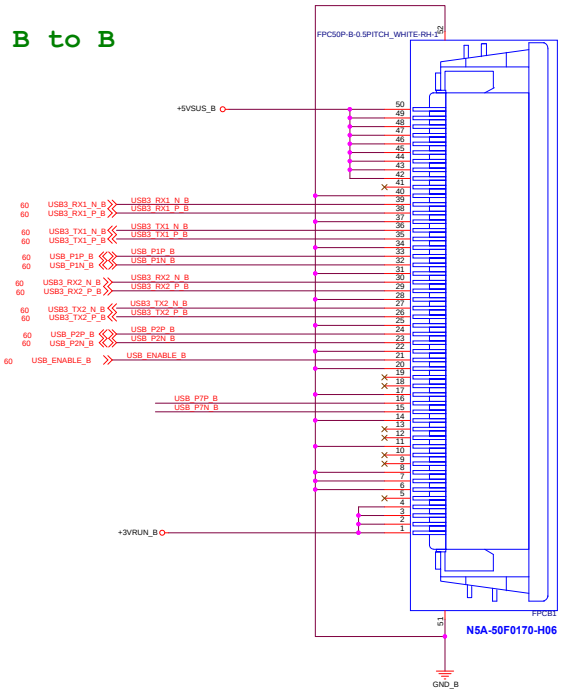
For EMI and Close to RTS5170;Wond 11/24
stuff RB1,2,4,5,6,7,8,9; ECB1,2,7,8



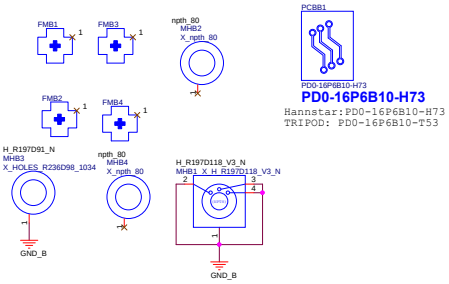
Close Connector



B to B



N5A-50F0170-H06



PD0-16P6B10-H73

Hannstar:PD0-16P6B10-H73
TRIPOD: PD0-16P6B10-T53

E2Y-X060211-G40

Title	[B]Card reader/BTB CONN	
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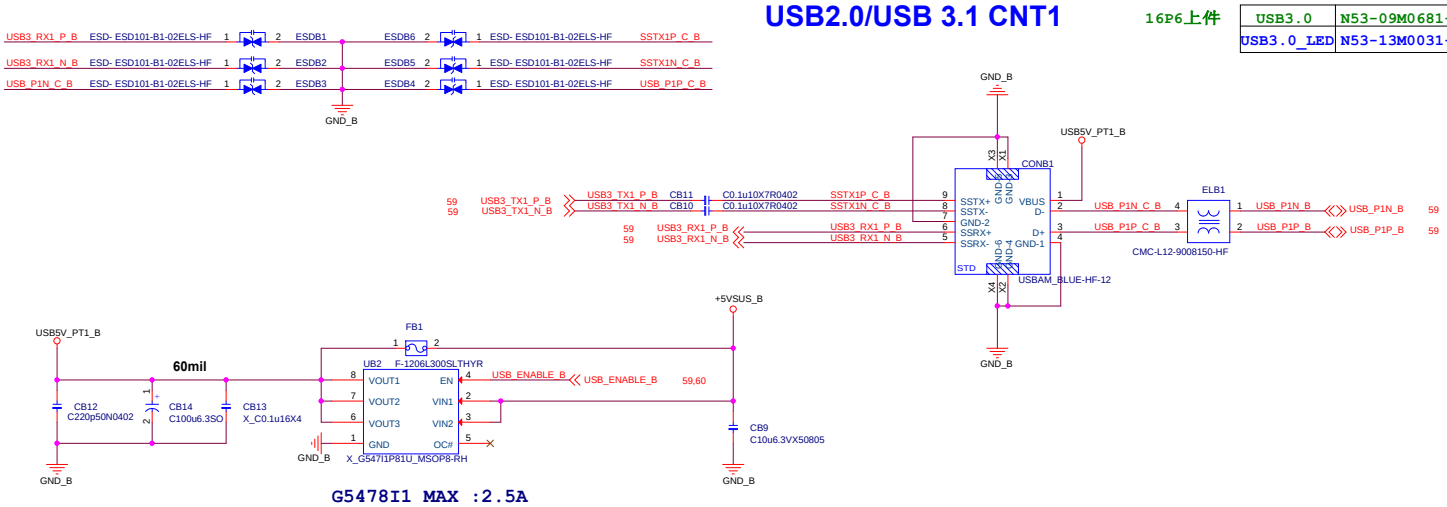
USB2.0/USB 3.1 CNT1

16P6上件

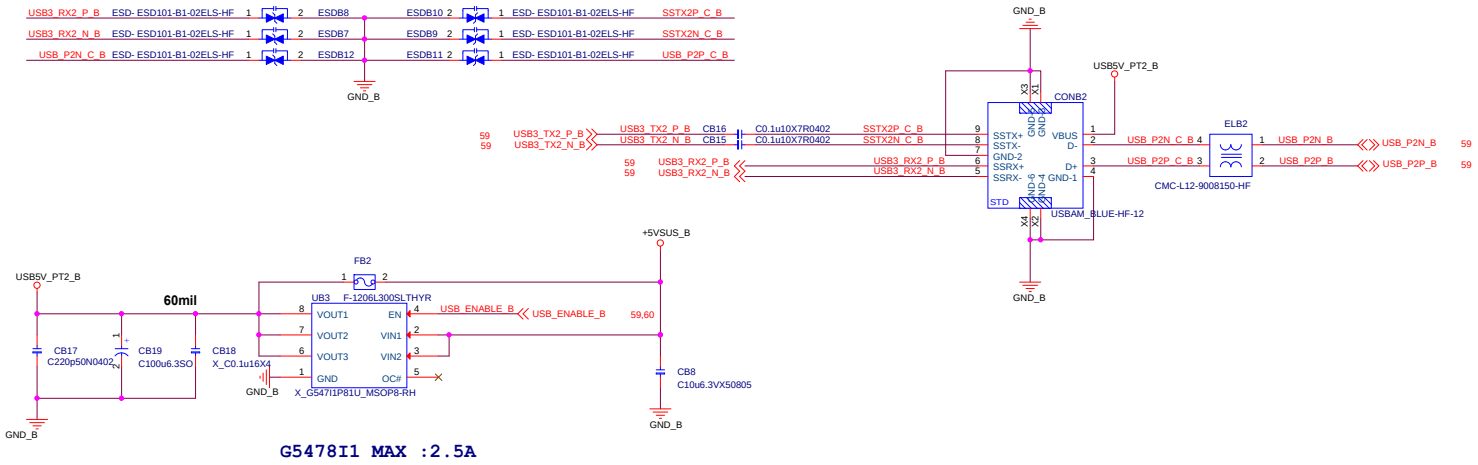
USB3.0	N53-09M0681-AF2
USB3.0_LED	N53-13M0031-L06



USB2.0/USB 3.1 CNT2

16P6上件

USB3.0	N53-09M0681-AF2
USB3.0_LED	N53-13M0031-L06



Title	[B]USB3.0		
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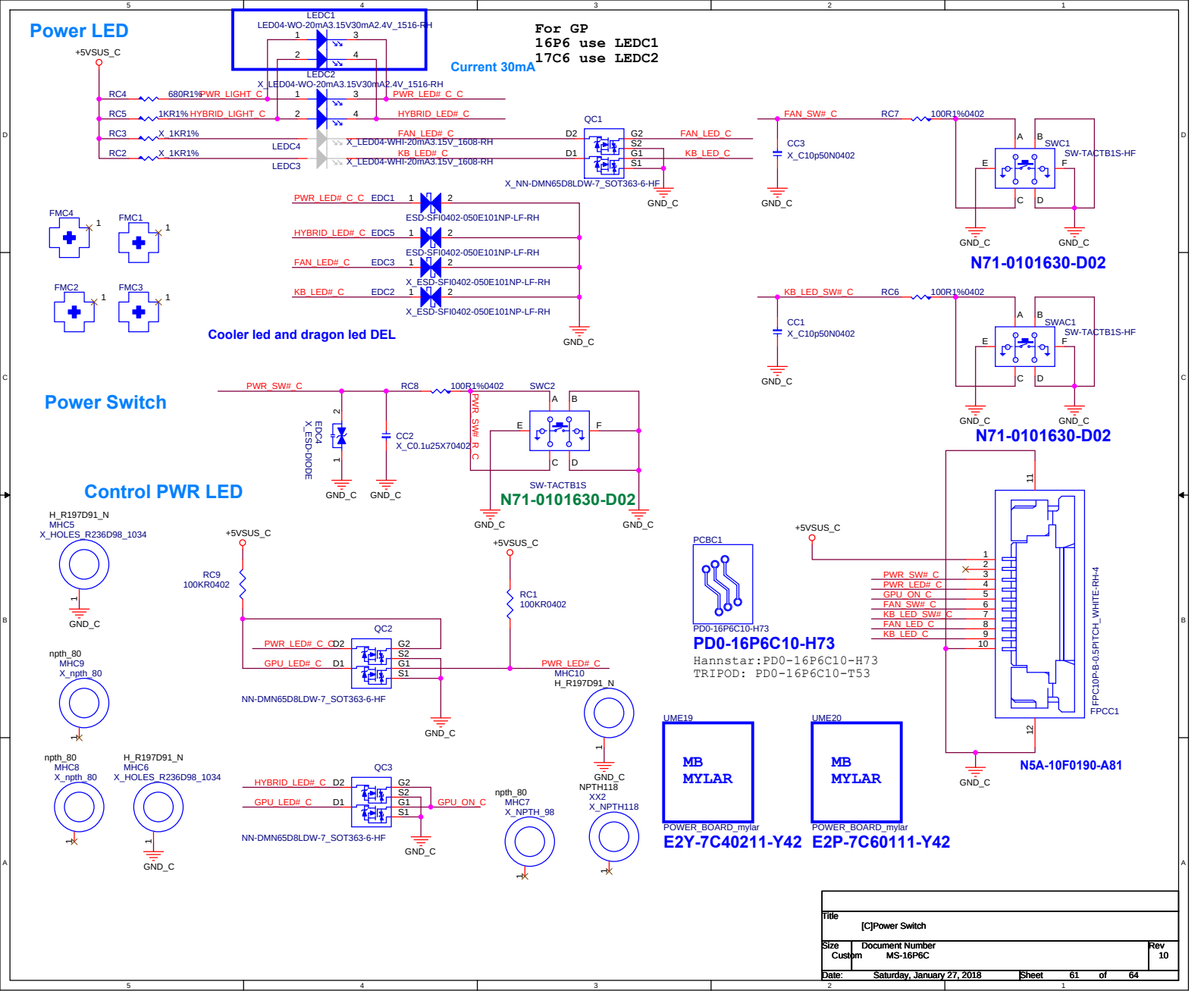

Title	[C]Power Switch	
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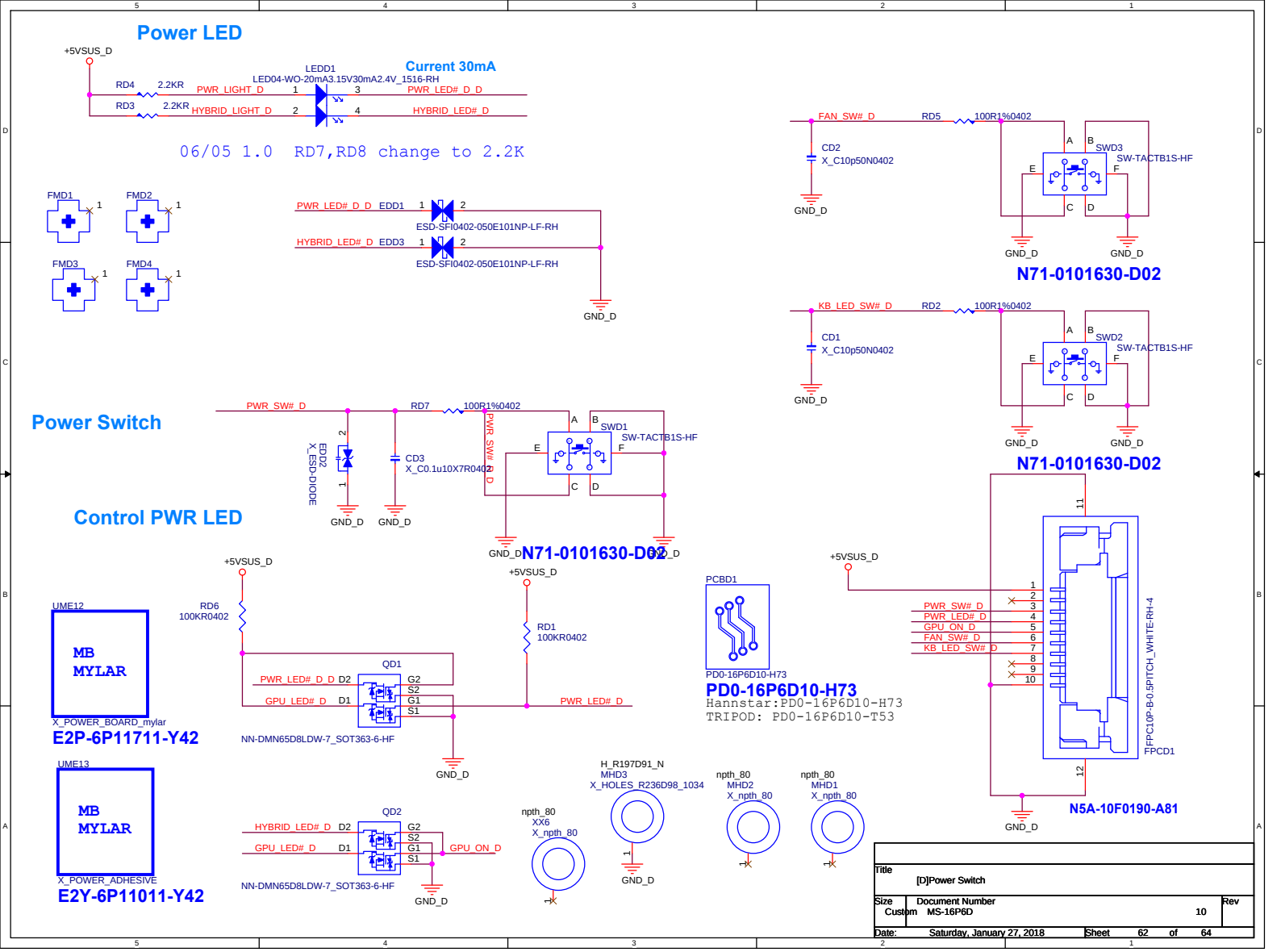

Title	[D]Power Switch		
Size	Document Number		Rev
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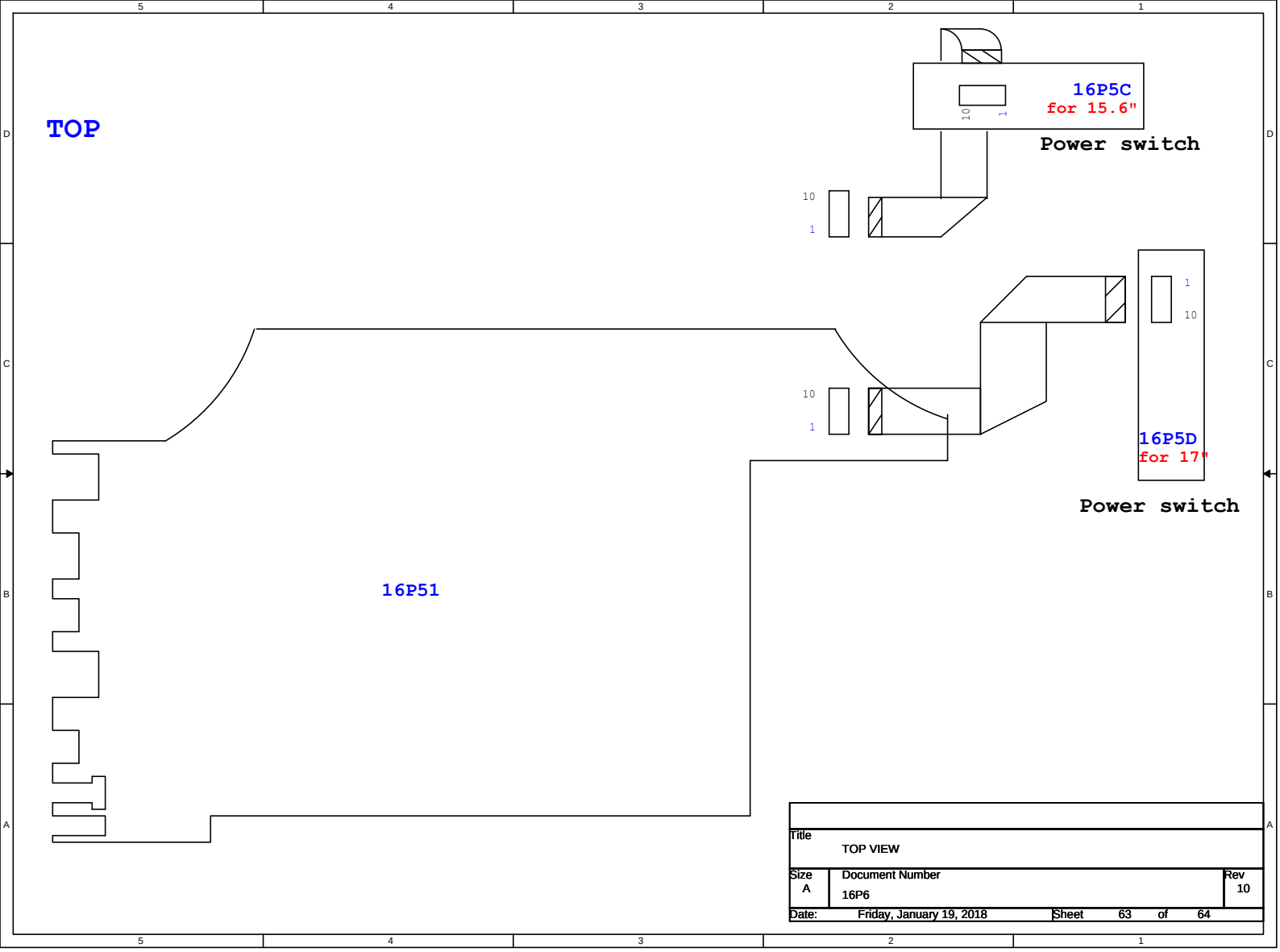

Title: TOP VIEW		
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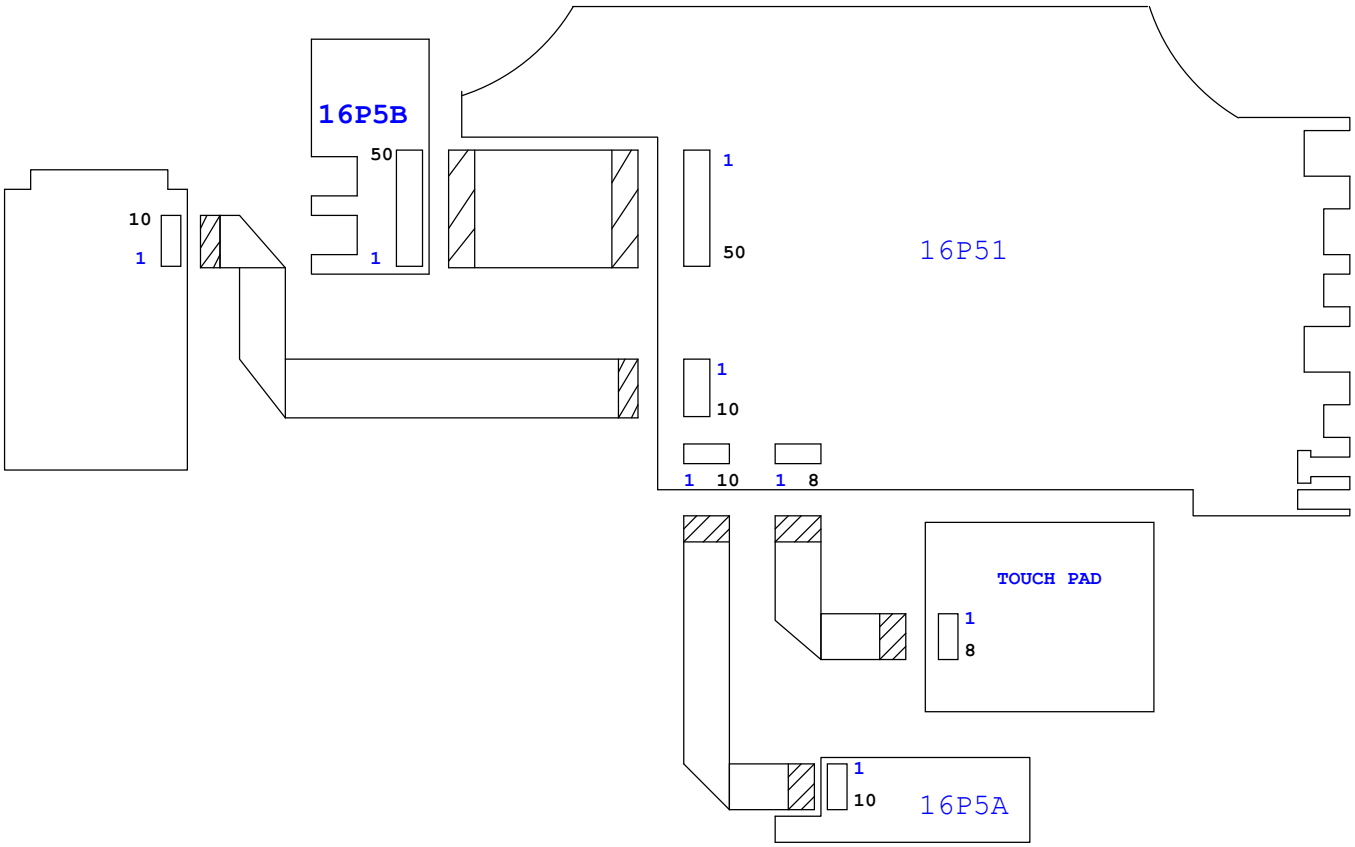
Bottom VIEW



Title: Bottom VIEW			
Size: Custom	Document Number: 16P6		Rev: 10
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