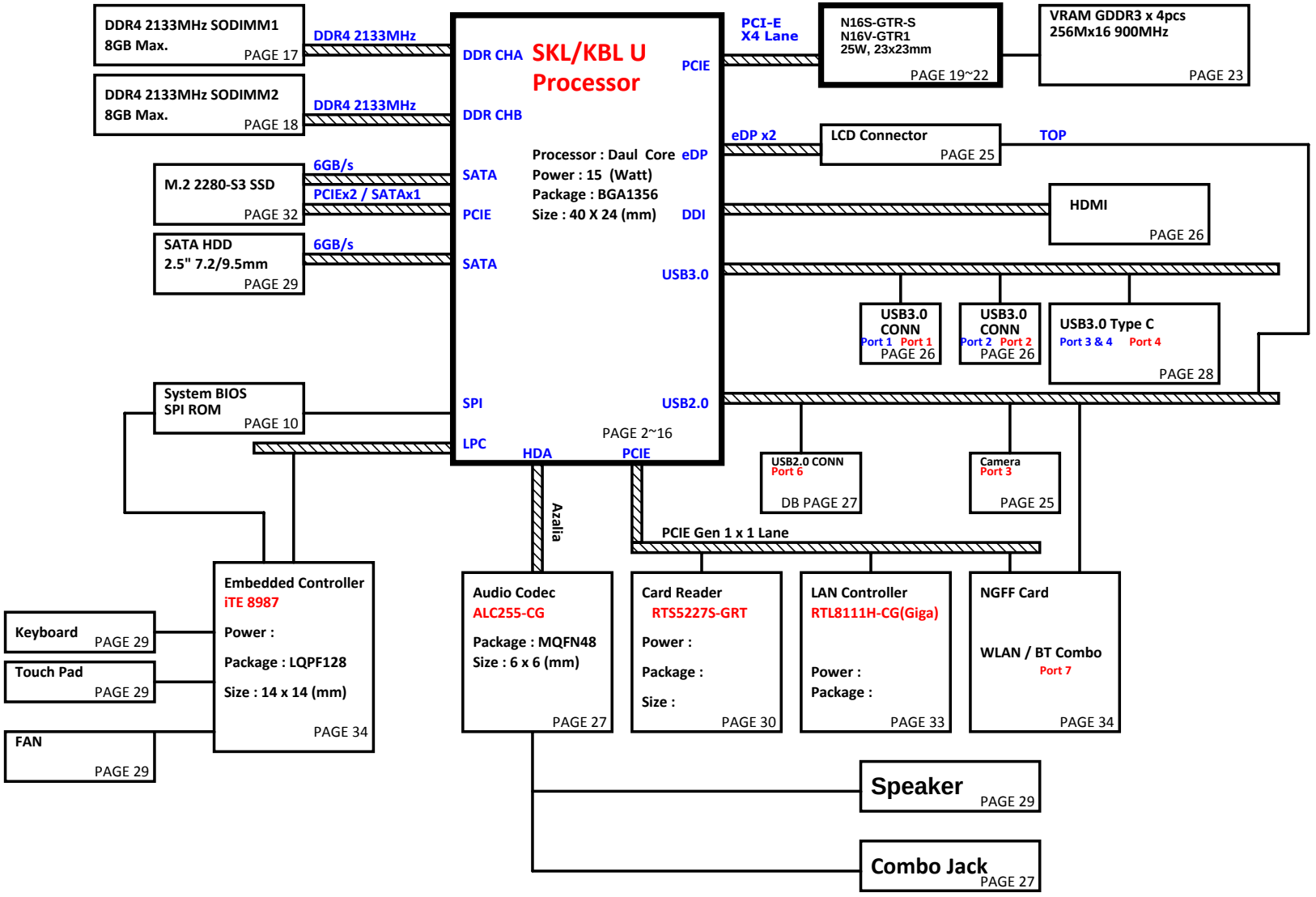
DIS (15") LG9

Intel SKL/KBL ULT Platform Block Diagram

01

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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+3V [4,10..13,15..21,25..27,29,30,32,33,35,41,45,46]
+1.0V [4,6,16,34,35,40]
+VCCSTPLL [4..6,9,13,40,41]

HDMI 1.4

DDPB_CTRLCLK	If using **HDMI***, 2.2 KΩ ±5% pull-up to 3.3 V before **HDMI*** level shifter. and 2.2 KΩ ±5% pull-up to 5V after the level shifter.
DDPB_CTRLDATA	This signal needs to be pulled up through a 2.2KΩ ±5% pull-up to 3.3V to enable Port B. For HDMI*, 2.2 KΩ ±5% pull-up to 3.3V before **HDMI*** level shifter and 2.2 KΩ ±5% pull-up to 5V after the level shifter is required.

0317 CQ
Del R868 & R869 2.2K PU +3V (重複)

U1A — SKL_ULT ? — Need apply PN

[26] IN_D2# → IN_D2# E55
[26] IN_D2 → IN_D2 F55
[26] IN_D1# → IN_D1# E58
[26] IN_D1 → IN_D1 F58
[26] IN_D0# → IN_D0# F53
[26] IN_D0 → IN_D0 G53
[26] IN_CLK# → IN_CLK# F56
[26] IN_CLK → IN_CLK G56

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3] — DDI — EDP
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3] — DISPLAY SIDEBANDS

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 [25]
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 [25]
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 [25]
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 [25]
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

need surport to FHD 2 Lane

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN [25]
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP [25]

EDP_DISP_UTIL B52 → TP1

DDI1_AUXN G50
DDI1_AUXP E50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

0224 CQ
Del INT_HDMI_AUXN & INT_HDMI_AUXN
HDMI 1.4 不需使用

GPP_E13/DDPB_HPD0 L9 → HDMI_HPD_CON → HDMI_HPD_CON [26]
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L5
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 → ULT_EDP_HPD

0309 CQ
HDMI_HPD_CON 預留PU 10K +3V (R1) & PD 100K (R2)接錯
應接ULT_EDP_HPD (整理線路接錯)

+3V → R1 *10K_4 → ULT_EDP_HPD [25]
R2 100K_4

Reserve EDP_HPD opposites circuit!

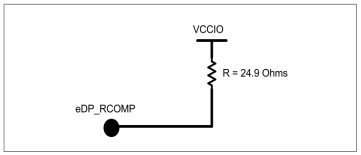
GPP_E18/DDPB_CTRLCLK L13 ← [26] SDVO_CLK
GPP_E19/DDPB_CTRLDATA L12 ← [26] SDVO_DATA
GPP_E20/DDPC_CTRLCLK N7
GPP_E21/DDPC_CTRLDATA N6
GPP_E22/DDPD_CTRLCLK N11
GPP_E23/DDPD_CTRLDATA N12

EDP_BKLTEN R12 → PCH_EDP_BLON → PCH_EDP_BLON [25]
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM [25]
EDP_VDDEN U13 → PCH_DISP_ON → PCH_DISP_ON [25]

+1.0V → R3 24.9/F_4 → EDP_RCOMP E52
EDP_RCOMP

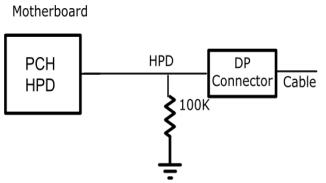
*SKL_ULT
REV = 1
1 OF 20
?

Embedded DisplayPort* Compensation Signal Routing Topology



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 ohms

Embedded DisplayPort* HPD Signal



Close to EC
+VCCSTPLL → 1K_4 R5 PM_THRMTRIP#

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

+VCCSTPLL

R6 *49.9/F_4 → CATERR# D63
[35] EC_PECI → EC_PECI A54
R4 499/F_4 → PROCHOT# C65
[35,41] H_PROCHOT# → PROCHOT# C63
[35] PM_THRMTRIP# → THERMTRIP# A65
SKTOCC# C65

TP8504 → C55
[16] XDP_BPM0 → BPM#[0] D55
[16] XDP_BPM1 → BPM#[1] B54
TP8505 → BPM#[2] C56
BPM#[3]

TP200 → 3D_FW_GPIO_R A6
TP4 → CPU_GP1 A7
TP5 → CPU_GP2 BA5
TP6 → CPU_GP3 AY5

GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

R8 49.9/F_4 → PROC_POPIRCOMP AT16
R11 49.9/F_4 → PCH_OPI_RCOMP AU16
R12 49.9/F_4 → EDRAM_OPIO_RCOMP H66
R14 49.9/F_4 → EOPIO_RCOMP H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

Rcomp < 600mil

U1D — SKL_ULT ? — Need apply PN

CPU MISC

JTAG

PROC_TCK B61 → XDP_TCK0 → XDP_TCK0 [16]
PROC_TDI D60 → XDP_TDI_CPU → XDP_TDI_CPU [16]
PROC_TDO A61 → XDP_TDO_CPU → XDP_TDO_CPU [16]
PROC_TMS C60 → XDP_TMS_CPU → XDP_TMS_CPU [16]
PROC_TRST# B59 → XDP_TRST#_CPU → XDP_TRST#_CPU [2,16]

PCH_JTAG_TCK B56 → JTAG_TCK_PCH → JTAG_TCK_PCH [16]
PCH_JTAG_TDI D59 → JTAG_TDI_PCH → JTAG_TDI_PCH [16]
PCH_JTAG_TDO A56 → JTAG_TDO_PCH → JTAG_TDO_PCH [16]
PCH_JTAG_TMS C59 → JTAG_TMS_PCH → JTAG_TMS_PCH [16]
PCH_TRST# C61 → XDP_TRST#_CPU → XDP_TRST#_CPU [2,16]
JTAGX A59 → JTAGX_PCH → JTAGX_PCH [16]

*SKL_ULT
REV = 1
4 OF 20

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

+1.0V
JTAGX_PCH *51_4 R10
JTAG_TMS_PCH 51_4 R13
JTAG_TDI_PCH 51_4 R15
JTAG_TDO_PCH 51_4 R16
JTAG_TCK_PCH 51_4 R18

Close to Chipset

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKL-01 [eDP/DDI/MISC]	1A

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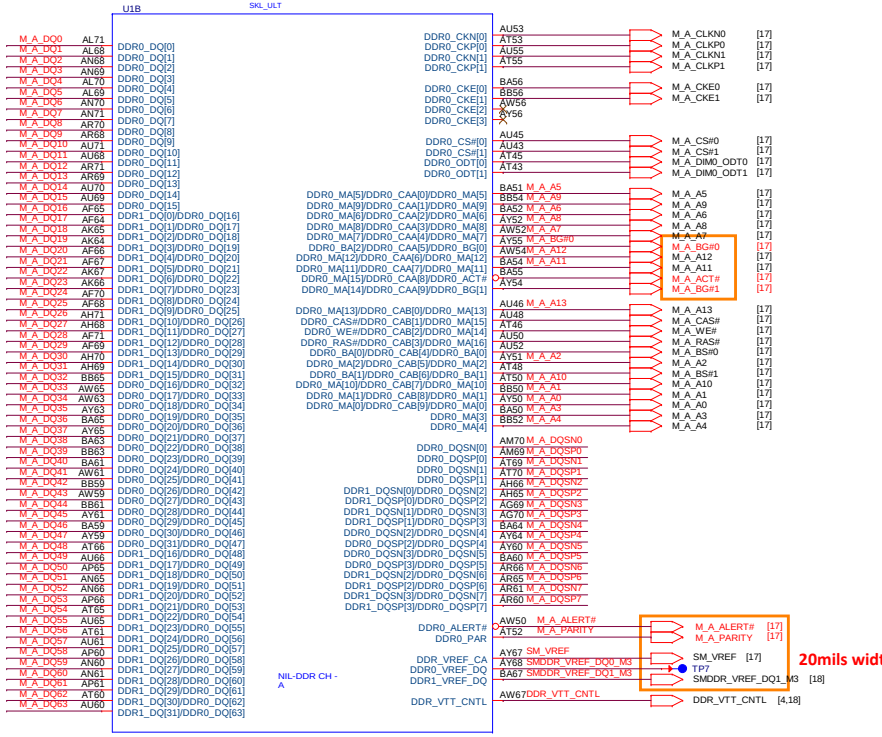
[17] M_A_DQSN[7:0]
[17] M_A_DQSP[7:0]
[18] M_B_DQSN[7:0]
[18] M_B_DQSP[7:0]
[17] M_A_DQ[63:0]
[18] M_B_DQ[63:0]

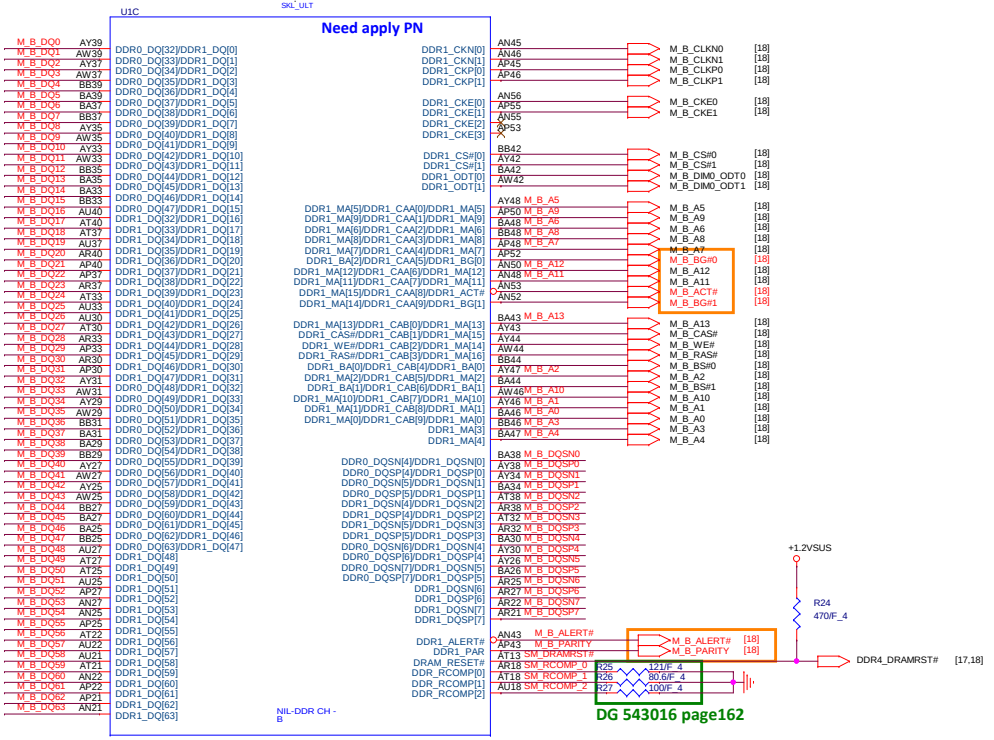
[6,17,18,38,40,48] +1.2VSUS

SkyLake ULT Processor (DDR4)

Non-Interleave / side by side

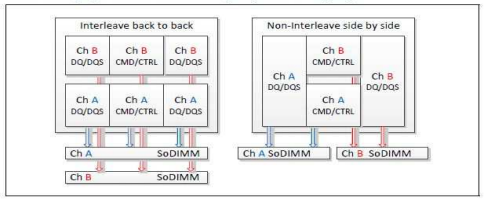
Need apply PN



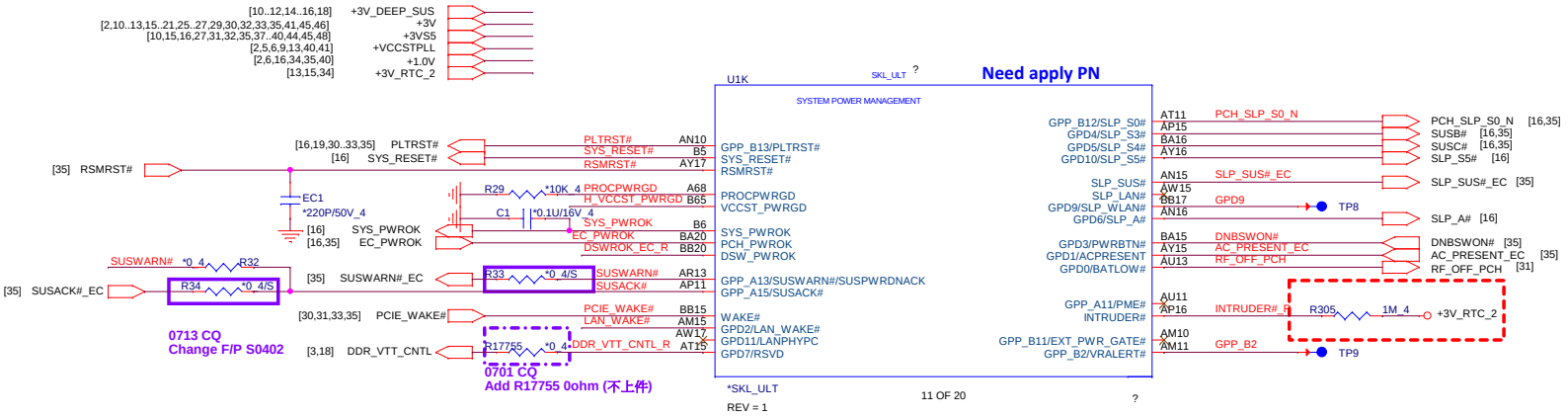


DG 543016 page162

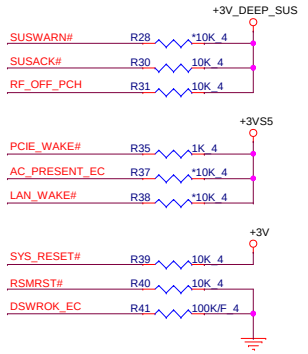
Interleave (IL) and Non-Interleave (NIL) Modes Mapping

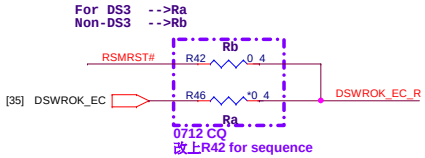


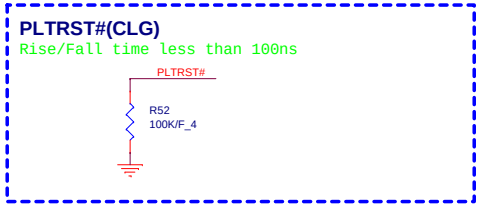
PROJECT : LG9 Quanta Computer Inc.			
Size: Custom	Document Number: SKL-02 [DDR4]		Rev: 1A
Date: Wednesday, July 20, 2016	Sheet 3 of 49		

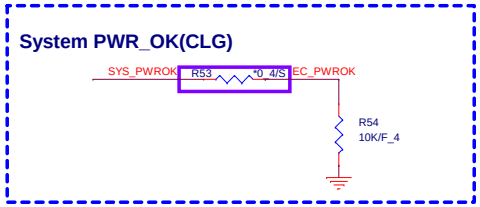


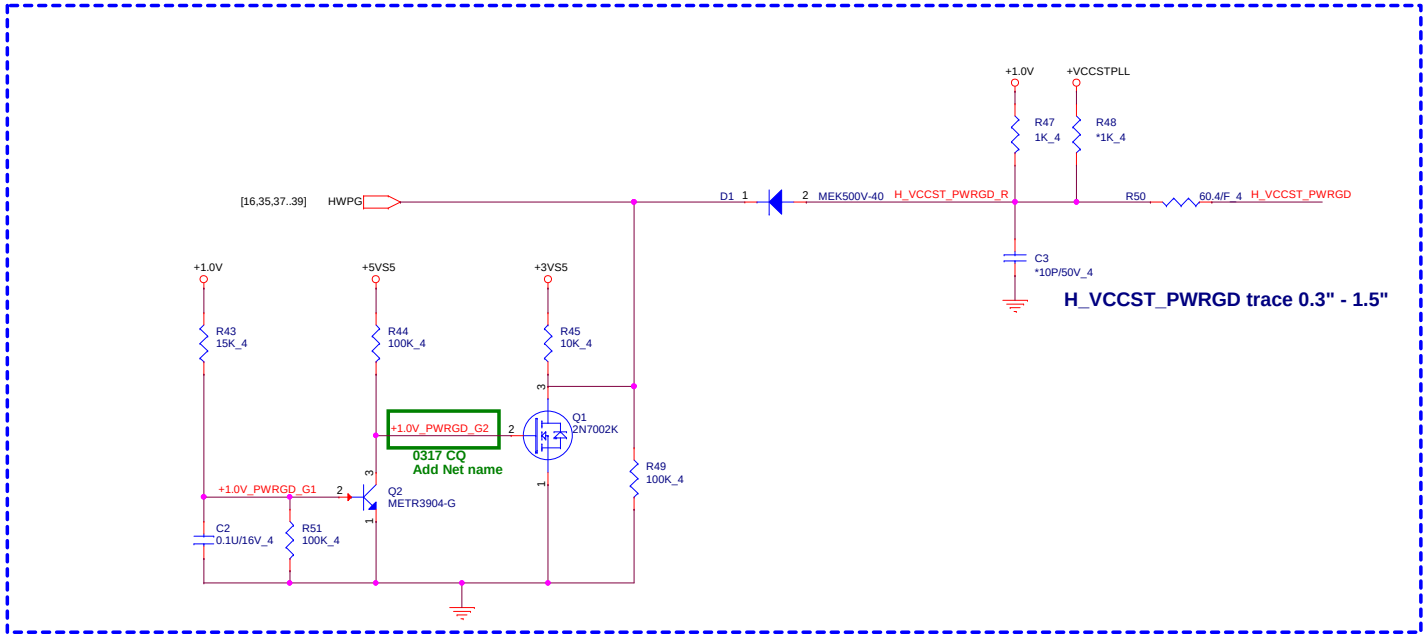
PCH Pull-high/low(CLG)



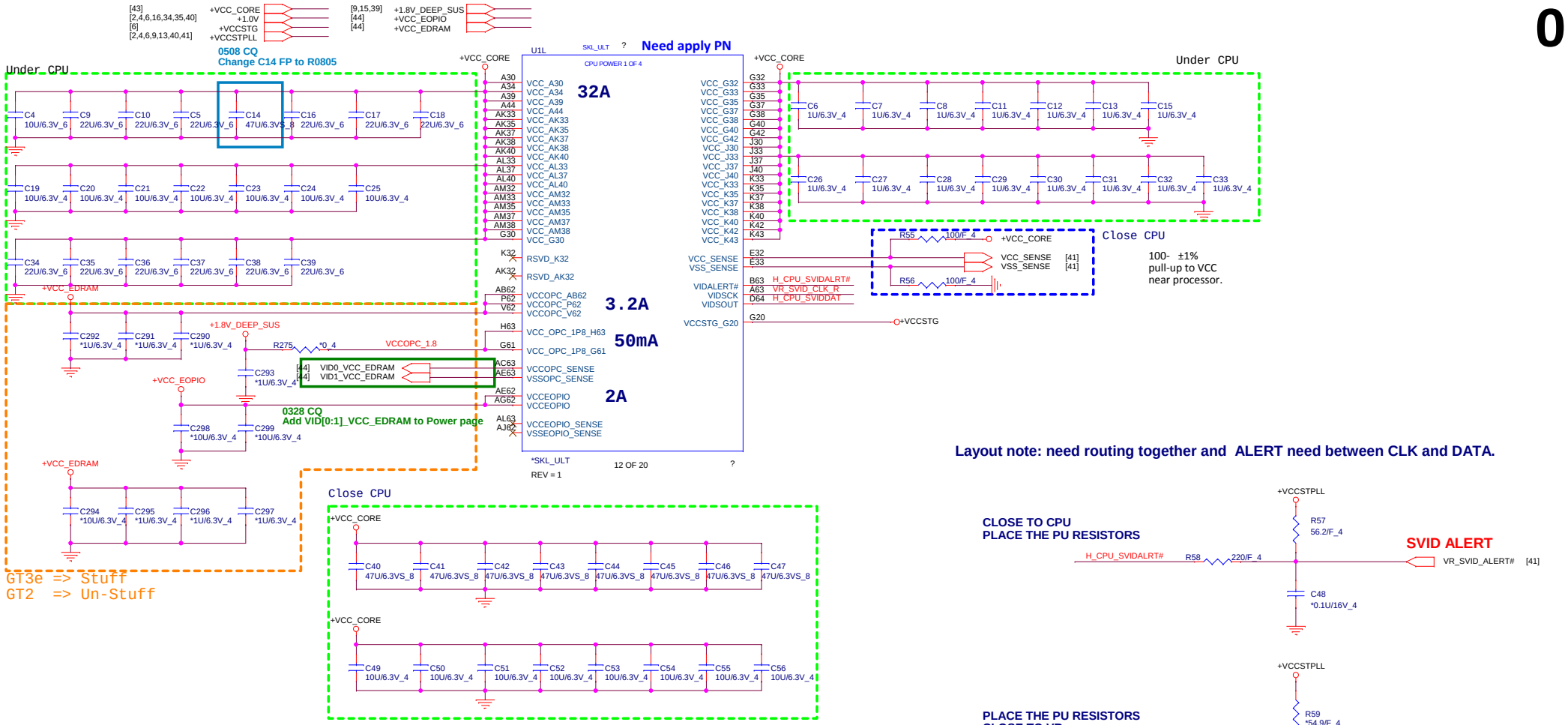








PROJECT : LG9 Quanta Computer Inc.		
Size: Custom	Document Number: SKL-03 [PowerManger]	Rev: 1A
Date: Wednesday, July 20, 2016	Sheet 4 of 49	



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Layout note: need routing together and ALERT need between CLK and DATA.

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKL-04 [POWER-1]	1A

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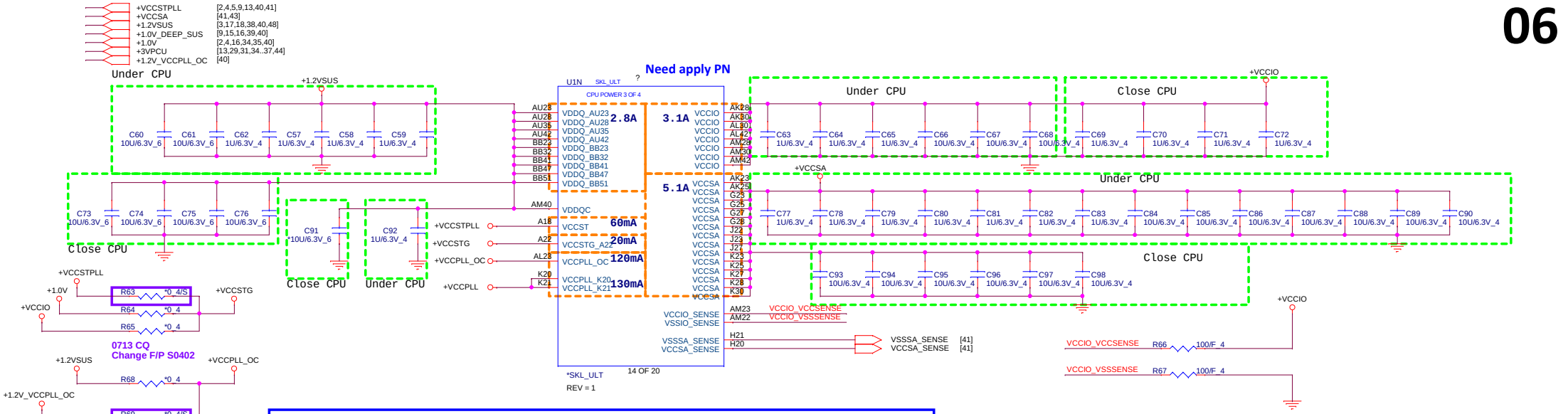

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKL-05 [POWER-2]	1A

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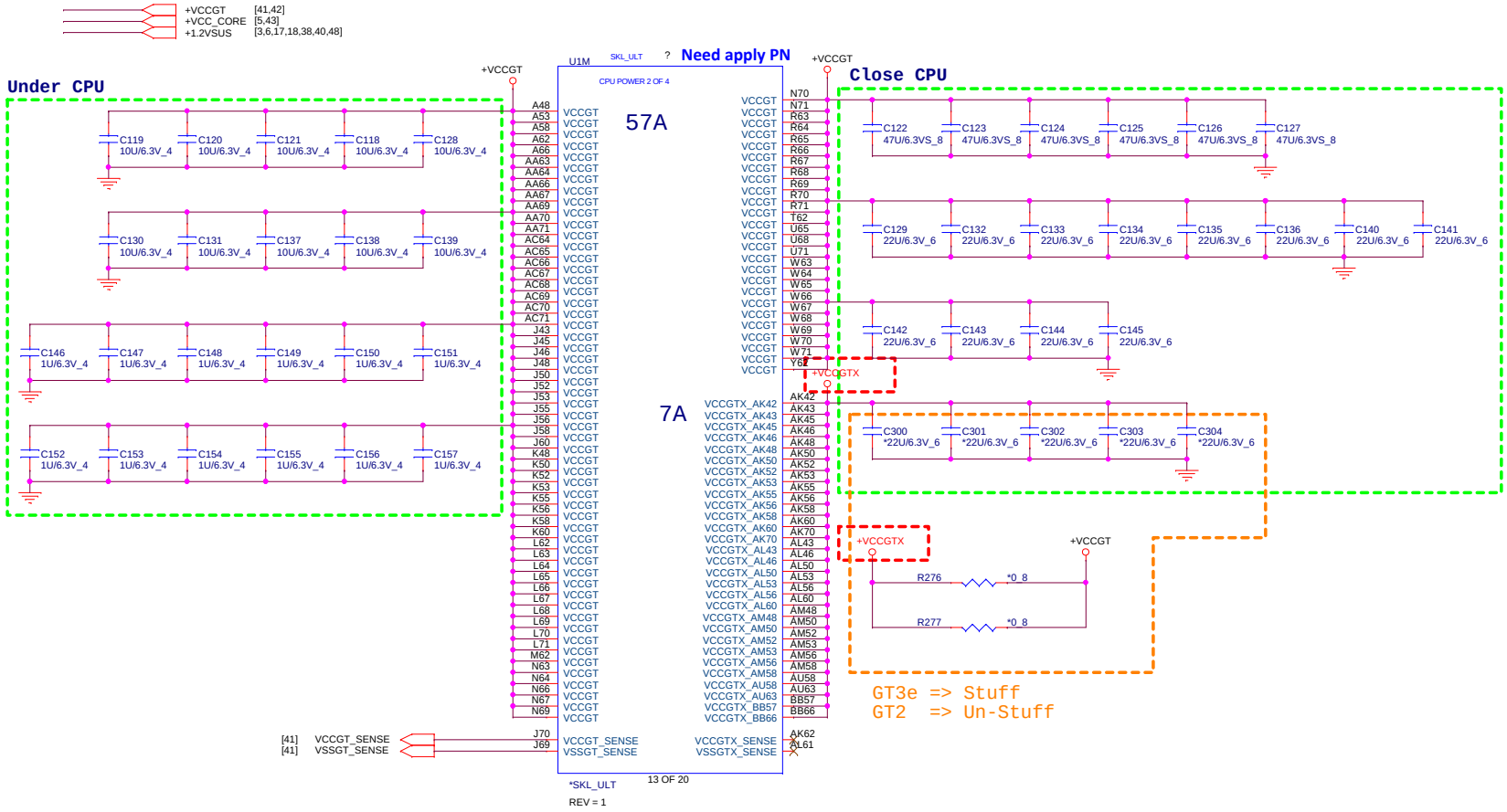

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKL-06 [POWER-3]	1A

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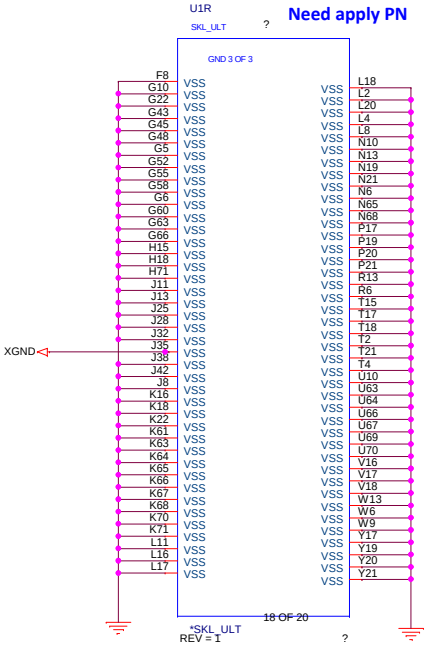

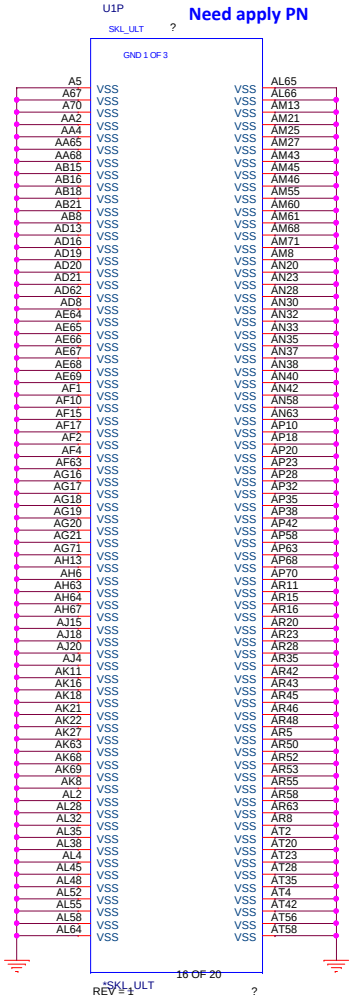

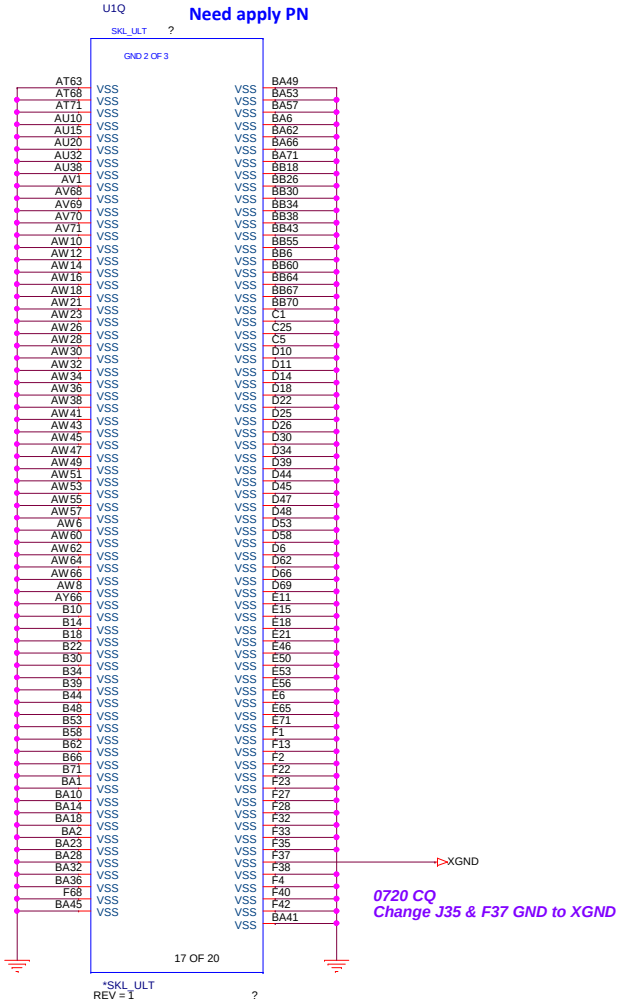

0720 CQ
Change J35 & F37 GND to XGND

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKL-07 [GND]	1A

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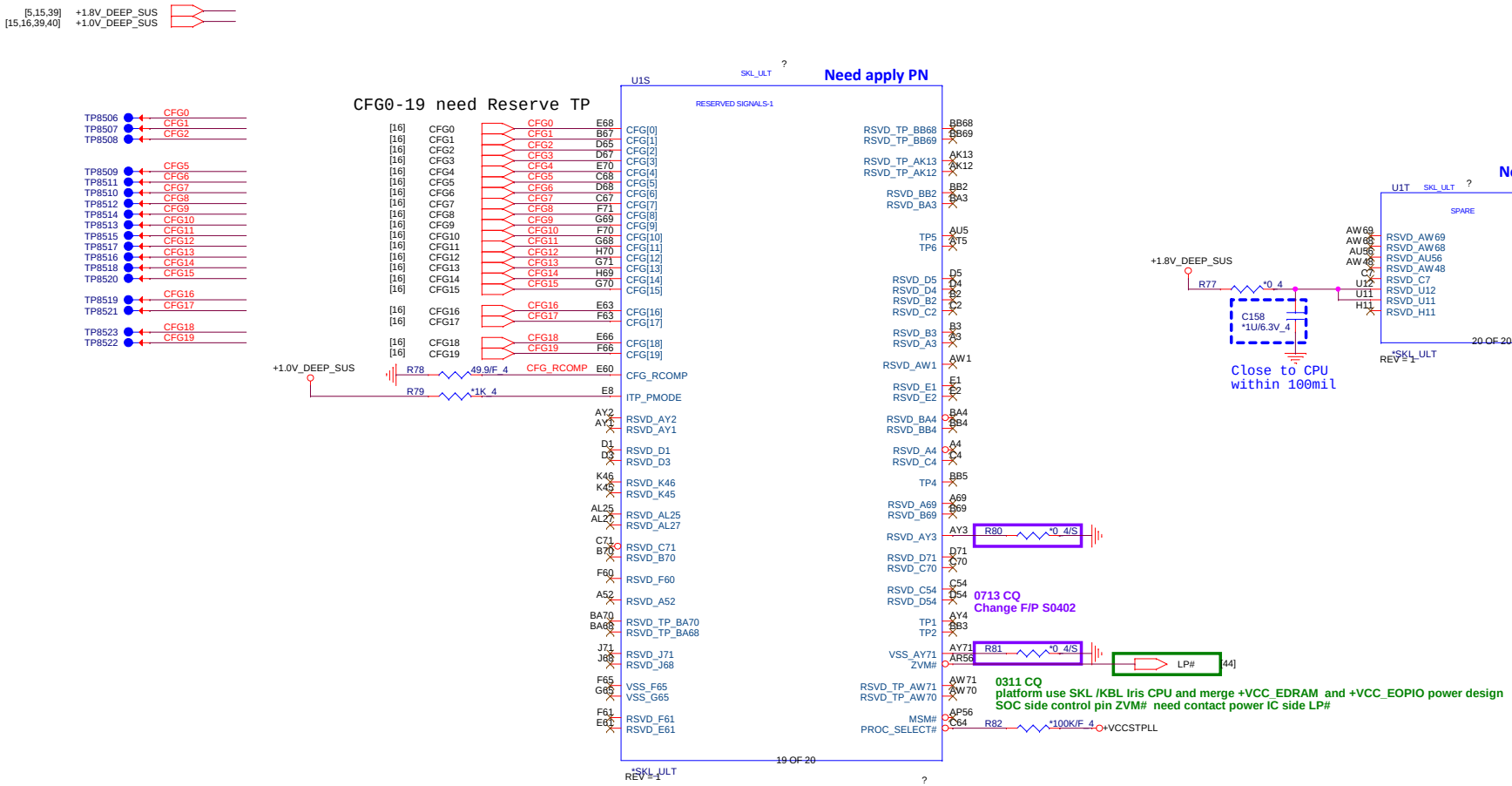

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

PROJECT : LG9
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Size	Document Number	Rev
Custom	SKL-08 [RSV]	1A

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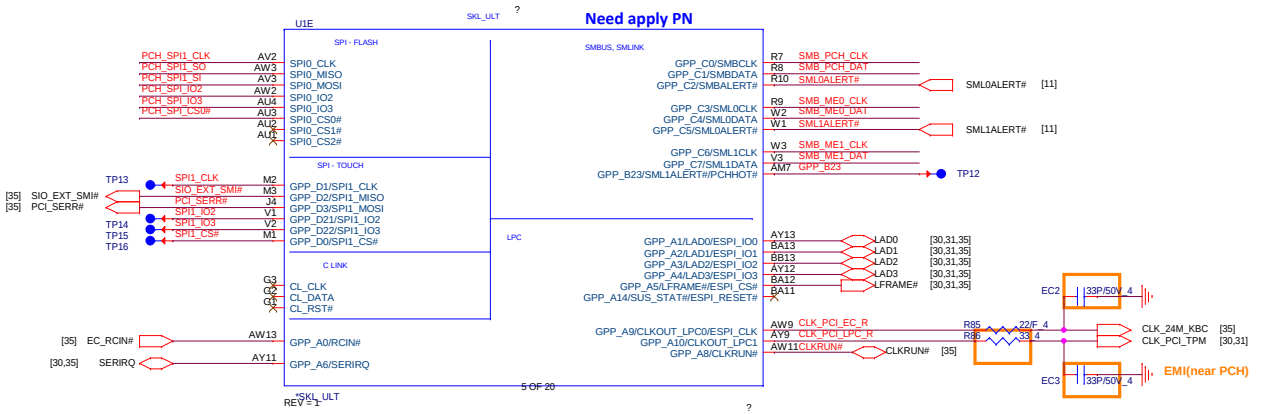
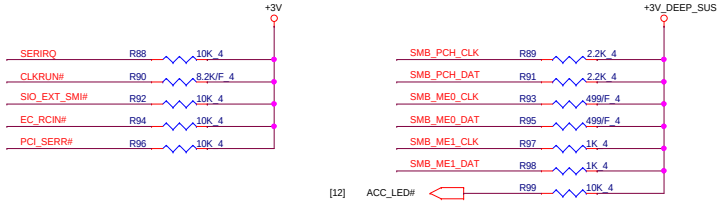
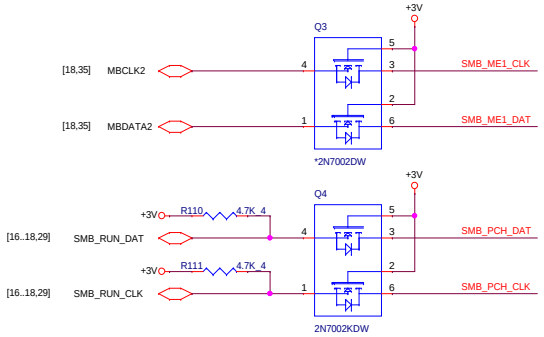
+3V_DEEP_SUS [4,11,12,14..16,18]
+3V [2,4,11..13,15..21,25..27,29,30,32,33,35,41,45,46]
+5V [26,27,29,45]
+1.0V [2,4,6,16,34,35,40]
+3VS5 [4,15,16,27,31,32,35,37..40,44,45,48]



GPIO Pull UP



SMBus/Pull-up(CLG)



CPU heat pipe local thermal sensor
DDR thermal sensor
RTD2136
EC

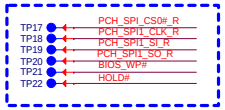
Touch Pad
XDP
DDR4

PCH SPI ROM(CLG)

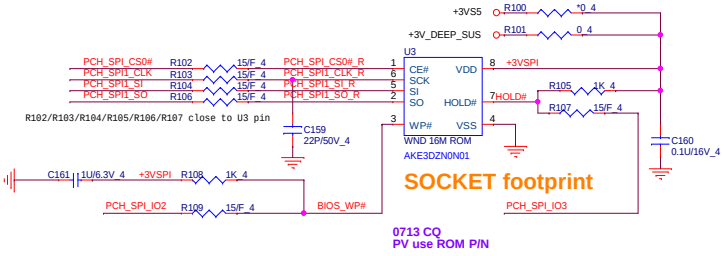
3/31 CQ
Fix ROM PN

Vender	Size	P/N
Winbond	16MB	AKE3DZN0N01 - IC FLASH(8P) W25Q128FVSIQ(SOIC)
GGD	16MB	AKE3DF00Q00 - IC FLASH(8P)GD25B128CSIGR(SOP)
Socket		DFHS08FS023

need place to TOP



PCH SPI ROM(CLG)



0713 CQ
PV use ROM P/N

PROJECT : LG9
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Size	Document Number	Rev
Custom	SKL-09 [SPI/LPC/SM]	1A
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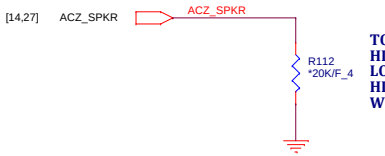
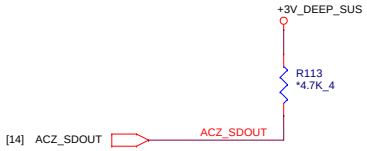
Functional Strap Definitions

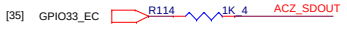
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

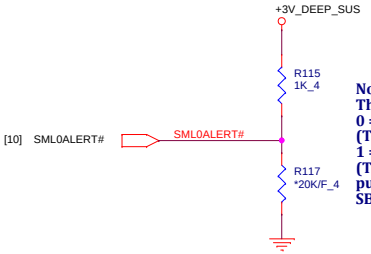


TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

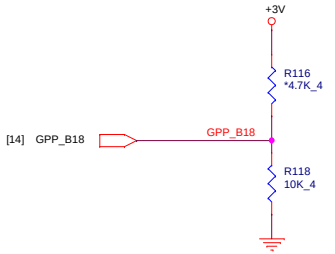


No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.





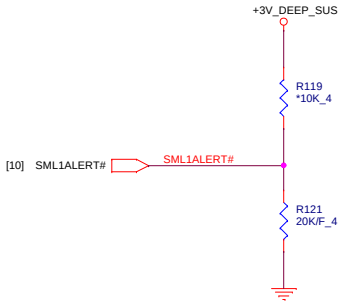
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

+3V	[2,4,10,12,13,15..21,25..27,29,30,32,33,35,41,45,46]
+3VS5	[4,10,15,16,27,31,32,35,37..40,44,45,48]
+3V_DEEP_SUS	[4,10,12,14..16,18]

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKL-10 [HDA]	1A

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+3V [2,4,10,11,13,15..21,25..27,29,30,32,33,35,41,45,46]
+3VS5 [4,10,15,16,27,31,32,35,37..40,44,45,48]
+3V_DEEP_SUS [4,10,11,14..16,18]

DIS only

dGPU

0306 CQ
~~刪除Cardreader PCIE net~~
~~LG9 use USB funciton~~
0311 CQ
改回PCIE Cardreafer

Cardreader

LAN

HDD

0525 CQ
WLAN port9 move to port8

WLAN

0525 CQ
Add PICe SSD to 4ch

SSD PCIE x2

~~0225 CQ~~
~~Del PCIE SSD port 11~~
0311 CQ
Add PCIE SSD port 11 for LG request

SSD SATA*1

0315 CQ
Add Net name

U1H SKL_ULT ?

Need apply PN

PCIE/USB3/SATA

SSIC / USB3

USB2

*SKL_ULT REV = 1 ? 8 OF 20

USB3.0 (M/B-1)

USB3.0 (M/B-2)

USB3.0 TYPE C

0128 Add USB3.0 TYPE C

Combo USB3.0 MB-1

Combo USB3.0 MB-2

Camera

Cobime USB3.0 TYPE C

0225 CQ
Del IR Camera function (USB5- & USB5+)

USB2.0 MB

WLAN

0225 CQ
Del Touch screen function (USB8- & USB8+)

0311 CQ
Del CR USB net (USBP10- & USBP10+)

CardReader

Ra

Modify 0922

PLACE 'Ra' WITHIN 500 MILS
FROM USB2_COMP PIN WITH
TRACE IMPEDANCE LESS THAN 0.5 OHMS

If OTG is not implemented on the platform,
then USB2_ID and USB2_VBUSSENSE should both
be connected to ground.

DB modify swap

DB modify

0713 CQ
Change F/P S0402

0309 CQ
Del ODD_PRSNT#_R & R128 (PU 10K +3V)

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

DIS ONLY

1002 Pull high

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	NA
Port3	dGPU	Port2	WLAN
Port4	dGPU	Port3	LAN
Port5	CardReader	Port4	CardReader
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8			
Port9	WLAN		
Port10			
Port11			
Port12	SATA2		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 TYPE C
PORT-4	USB3.0 TYPE C

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 MB-2
PORT-3	Camera
PORT-4	Cobime USB3.0 TYPE C
PORT-5	NC
PORT-6	USB2.0 MB
PORT-7	WLAN
PORT-8	NC
PORT-9	NC
PORT-10	NC

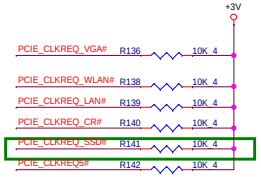
Table 12-7. PCI Express* Compensation Routing Guidelines

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length	Length Matching
PCIE_RCOMPN	M1: 4 mils min (breakout) 12-15 mils (max) Note: Must maintain low DC resistance routing (<0.1 ohm).	At least 12 mils to any adjacent high speed I/O.	100 ohm +/-1% external resistor. Differential impedance RCOMPN RCOMPN	NA	Both RCOMP & RCOMPN must be matched to less than 1% trace and board
PCIE_RCOMPP	M1: 4 mils min (breakout) 12-15 mils (max) Note: Must maintain low DC resistance routing (<0.1 ohm).			NA	

+1.0V_DEEP_SUS [9,15,16,39,40]
+BAT_RTC [31]
+1.8V_DEEP_SUS [5,9,15,39]
+3V [2,4,10..12,15..21,25..27,29,30,32,33,35,41,45,46]
+3VPCU [6,29,31,34..37,44]

~~0226 CQ~~
~~Del CLK_PCIE_SSDN & CLK_PCIE_SSDP~~
~~Change net name PCIE_CLKREQ_SSD# to PCIE_CLKREQ1#~~
0311 CQ
Add CLK_PCIE_SSDN & CLK_PCIE_SSDP for LG request
Change net name PCIE_CLKREQ1# to PCIE_CLKREQ_SSD#

CLK_REQ/Strap Pin(CLG)



VGA
SSD
WLAN
LAN
Cardreader

[19] CLK_VGA_N
[19] CLK_VGA_P
[19] PCIE_CLKREQ_VGA#
[32] CLK_PCIE_SSDN
[32] CLK_PCIE_SSDP
[32] PCIE_CLKREQ_SSD#
[31] CLK_PCIE_WLANN
[31] CLK_PCIE_WLANP
[31] PCIE_CLKREQ_WLAN#
[33] CLK_PCIE_LANN
[33] CLK_PCIE_LANP
[33] PCIE_CLKREQ_LAN#
[30] CLK_PCIE_CRN
[30] CLK_PCIE_CRP
[30] PCIE_CLKREQ_CR#

~~0307 CQ~~
~~Change net name PCIE_CLKREQ_CR# to PCIE_CLKREQ4#~~
0311 CQ
Add CLK_PCIE_CRN & CLK_PCIE_CRP
Change net name PCIE_CLKREQ4# to PCIE_CLKREQ_CR#

U1J SKL_ULT ? CLOCK SIGNALS

Need apply PN

CLK_VGA_N D42 CLKOUT_PCIE_N0
CLK_VGA_P C42 CLKOUT_PCIE_P0
PCIE_CLKREQ_VGA# AR10 GPP_B5/SRCCLKREQ0#
CLK_PCIE_SSDN B42 CLKOUT_PCIE_N1
CLK_PCIE_SSDP A42 CLKOUT_PCIE_P1
PCIE_CLKREQ_SSD# AT7 GPP_B6/SRCCLKREQ1#
CLK_PCIE_WLANN D41 CLKOUT_PCIE_N2
CLK_PCIE_WLANP C41 CLKOUT_PCIE_P2
PCIE_CLKREQ_WLAN# AT8 GPP_B7/SRCCLKREQ2#
CLK_PCIE_LANN D40 CLKOUT_PCIE_N3
CLK_PCIE_LANP C40 CLKOUT_PCIE_P3
PCIE_CLKREQ_LAN# AT10 GPP_B8/SRCCLKREQ3#
CLK_PCIE_CRN B40 CLKOUT_PCIE_N4
CLK_PCIE_CRP A40 CLKOUT_PCIE_P4
PCIE_CLKREQ_CR# AU8 GPP_B9/SRCCLKREQ4#
PCIE_CLKREQ5# E39 CLKOUT_PCIE_N5
AU7 CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N F43 CK_XDP_N R17731 *0_4/S XDP_N [16]
CLKOUT_ITPXDP_P E43 CK_XDP_P R17732 *0_4/S XDP_P [16]
GPD8/SUSCLK BA17 TP203
XTAL24_IN E37 XTAL24_IN
XTAL24_OUT E35 XTAL24_OUT
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2 TP38
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST# RTC_RST# [16]

*SKL_ULT REV = 1
10 OF 20
TBT

0305 CQ
Change net name
CK_XDP_N_R to CK_XDP_N
CK_XDP_P_R to CK_XDP_P
0307 CQ
Add 0 ohm contact to page16 xDP
XDP_N & XDP_P
Del TP

0713 CQ
Change F/P S0402

1027 modify for eazy layout

+VCCSTPLL
R135 2.7K/F_4
XCLK_BIASREF
R137 *60.4/F_4

U1I SKL_ULT ? CSI-2

Need apply PN

CSI2_DN0 A36
CSI2_DP0 B36
CSI2_DN1 C36
CSI2_DP1 D36
CSI2_DN2 C35
CSI2_DP2 D35
CSI2_DN3 A35
CSI2_DP3 B35
CSI2_DN4 C31
CSI2_DP4 D31
CSI2_DN5 C33
CSI2_DP5 D33
CSI2_DN6 A33
CSI2_DP6 B33
CSI2_DN7 A32
CSI2_DP7 B32
CSI2_DN8 A29
CSI2_DP8 B29
CSI2_DN9 C29
CSI2_DP9 D29
CSI2_DN10 A27
CSI2_DP10 B27
CSI2_DN11 C27
CSI2_DP11 D27

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 D32
CSI2_CLKP1 C32
CSI2_CLKN2 D29
CSI2_CLKP2 C29
CSI2_CLKN3 D26
CSI2_CLKP3 C26
CSI2_COMP E13
GPP_D4/FLASHTRIG B7 GPP_D4 R143 100/F_4 TP39

EMMC
GPP_F13/EMMC_DATA0 AP2
GPP_F14/EMMC_DATA1 AP1
GPP_F15/EMMC_DATA2 AP3
GPP_F16/EMMC_DATA3 AN3
GPP_F17/EMMC_DATA4 AN1
GPP_F18/EMMC_DATA5 AN2
GPP_F19/EMMC_DATA6 AM4
GPP_F20/EMMC_DATA7 AM1
GPP_F21/EMMC_RCLK AM2
GPP_F22/EMMC_CLK AM3
GPP_F12/EMMC_CMD AP4
EMMC_RCOMP AT1 EMMC_RCOMP R144 200/F_4

1001 Del TP

*SKL_ULT REV = 1
9 OF 20

RTC Clock 32.768KHz

0301 CQ
Add GCLK XTALIN (CLKGEN_RTC_X1) & 0ohm

[34] CLKGEN_RTC_X1 *0_4 R17724
C177 12P/50V_4 RTC_X1
Y1 32.768KHZ *0_4
R147 10M_4
C179 12P/50V_4 RTC_X2

RTC Circuitry(RTC)

30mils
Coin BAT -->Rb
Rb
Ra
+3V_RTC_2
+BAT_RTC
R307 *0_4
Modify 0922
RTC Power trace width 20mils.
R145 *0_6
R146 20K/F_4
R149 20K/F_4
RTC_RST#
SRTC_RST#
C178 1U/6.3V_4
C182 1U/6.3V_4
C181 1U/6.3V_4
+3V_RTC_0
R150 1K_4
+3VPCU
+3V_RTC_1
D2 BAT54CW-7-F
CN11 BAT_CONN DFHS02FS080 bat-ap-aaa-bat-054-k01-2p-smt

[4,15,34] +3V_RTC_2
R151 10K_4
EC_RTC_RST [35]
RTC_RST#
Q7705 2N7002K
EC_SRTC_RST [35]
Q7706 *2N7002K
SRTC_RST#
R8506 *10K_4

0413 CQ
Change Q5 circuit (Follow G31 MV)
0523 CQ
Del Q5 , add Q7705 & Q7706 (Q7706預留)
0526 CQ
Change Q7705 & Q7706 pin define

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

TP51
C176 27P/50V_4
XGND
XTAL24_IN
XTAL24_OUT
R148 1M_4
24MHZ +-20PPM Y2
C180 27P/50V_4
TP52
R17757 *0_4

0524 CQ
Change 24M X'tal P/N & F/P "BG624000112" "xtl-2x1_6-1_35x1_05"

0720 CQ
Del R17722 & R17723
Change 24M X'tal GND to XGND
Add R17757 contact XGND & GND

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Quanta Computer Inc.
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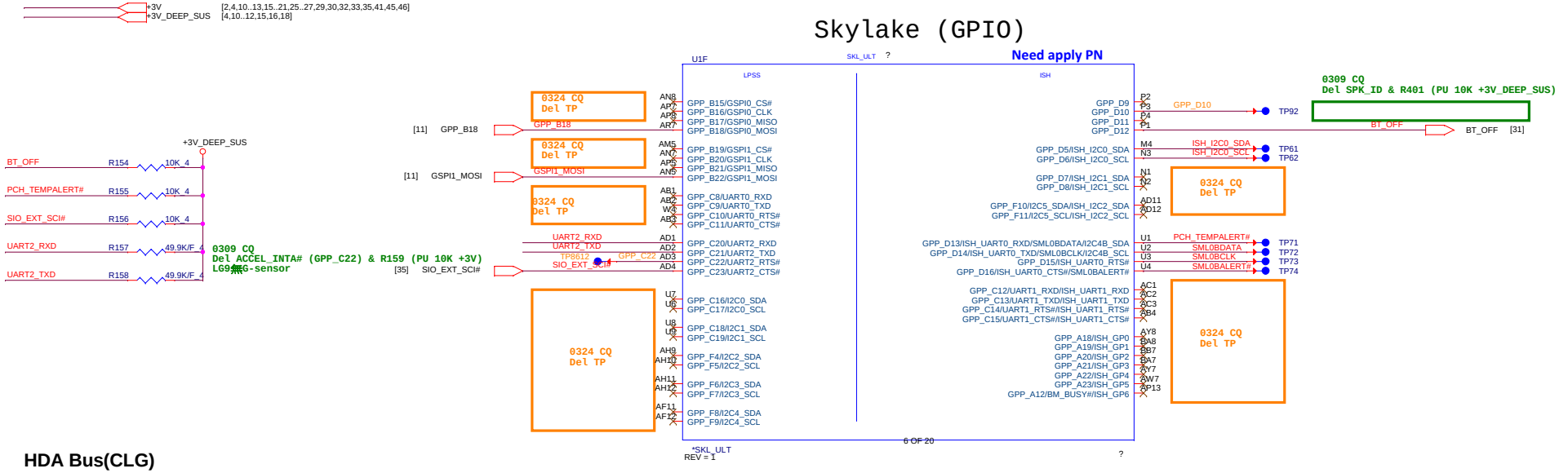
Skylake (GPIO)



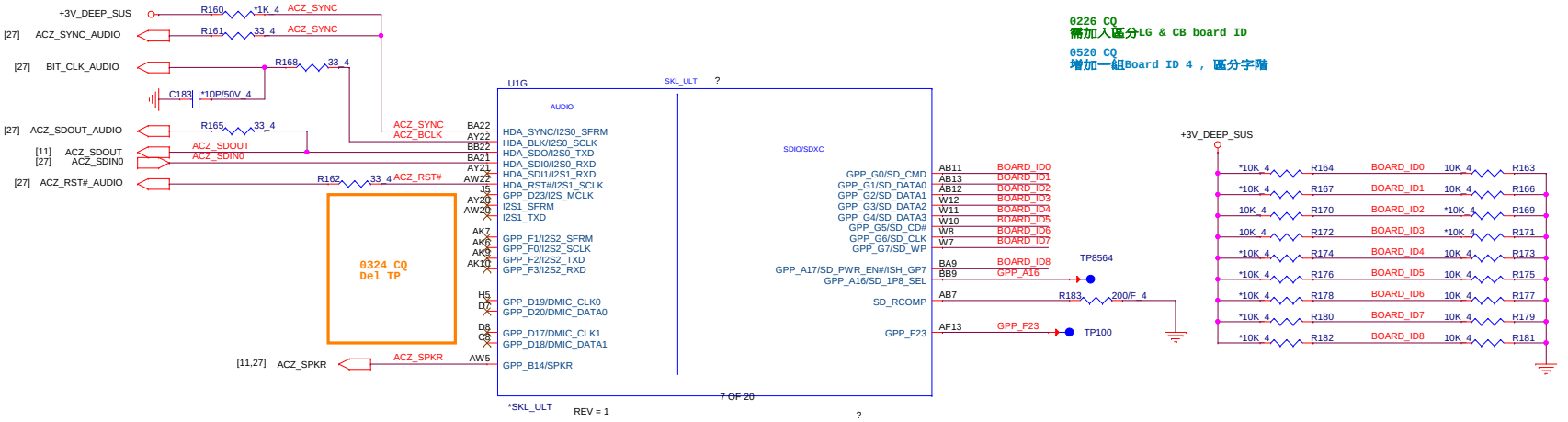
HDA Bus(CLG)

HDA Bus(CLG)

Model	BOARD_ID0 GPP_G0 LG9 : 0 LG9A : 1	BOARD_ID1 GPP_G1 LG : 0 CB : 1	BOARD_ID2 GPP_G2 N16V : 0 N16S : 1	BOARD_ID3 GPP_G3 UMA : 0 dGPU : 1	BOARD_ID4 GPP_G4 LG9 : 0 LG9A : 1	BOARD_ID5 GPP_G5 No Define	BOARD_ID6 GPP_G6 No Define	BOARD_ID7 GPP_G7 No Define	BOARD_ID8 GPP_G8 No Define
LG9 + UMA	0	0	0	0	0	0	0	0	0
LG9 + dGPU + N16S-GTR	0	0	1	1	0	0	0	0	0
LG9 + dGPU + N16V-GMR1	0	0	0	1	0	0	0	0	0
LG9A + UMA	1	1	0	0	1	0	0	0	0
LG9A + dGPU + N16S-GTR	1	1	1	1	1	0	0	0	0
LG9A + dGPU + N16V-GMR1	1	1	0	1	1	0	0	0	0

0226 CQ
需加入區分LG & CB board ID

0520 CQ
增加一組Board ID 4 , 區分字階



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[4,10..12,14,16,18]
[9,16,39,40]
[5,9,39]
[4,10,16,27,31,32,35,37..40,44,45,48]
[4,13,34]

+3V_DEEP_SUS
+1.0V_DEEP_SUS
+1.8V_DEEP_SUS
+3VS5
+3V_RTC_2

U1O SKL_ULT CPU POWER 4 OF 4

Need apply PN

PCH Internal VRM

Ca and Cb close to CPU less then 100 mils

+VCCPRIM
C184 1U/6.3V_4
AB19 AB20 P18 VCCPRIM_1P0 2.899A

+1.0V_DEEP_SUS
C185 1U/6.3V_4
AF18 AF19 V20 V21 VCCPRIM_CORE 2.57A

+VCCDSW_1.0V
Ca
C187 1U/6.3V_4
AL1 DCPDSW_1P0

+1.0V_DEEP_SUS
R188 *0_4/S 22mA +VCCMPHYAON_1P0
C188 1U/6.3V_4
K17 L1 VCCMPHYAON_1P0

+1.0V_DEEP_SUS
C189 1U/6.3V_4
C190 47U/6.3VS_8
N15 N16 N17 P15 P16 VCCMPHYGT_1P0 1.714A

+1.0V_DEEP_SUS
R194 *0_6/S +VCCAMPHYPLL_1P0
C192 1U/6.3V_4
K15 L15 VCCAMPHYPLL_1P0

+1.0V_DEEP_SUS
R196 *0_4/S 26mA +VCCAPLL_1.0V
V15 VCCAPLL_1P0 0.03A

+1.0V_DEEP_SUS
R199 *0_6/S +VCCPRIM
AB17 Y18 VCCPRIM_1P0_AB17 VCCPRIM_1P0_Y18

0713 CQ
Change F/P S0402

+3VS5
R201 *0_4/S +3VS5_AD17
C193 1U/6.3V_4
AD17 AD18 AJ17 VCCDSW_3P3 0.09A

+V3.3DX_1.5DX_ADO
C194 1U/6.3V_4
AJ19 VCCHDA

+3V_DEEP_SUS
R205 *0_4/S 11mA +VCCSPI
AJ16 VCCSPI

+1.0V_DEEP_SUS
R206 *0_6/S 700mA +VCCSRAM_1.0V
C196 1U/6.3V_4
AF20 AF21 T19 T20 VCCSRAM_1P0

+3V_DEEP_SUS
R207 *0_4/S 75mA +VCCPRIM_3.3V
AJ21 VCCPRIM_3P3_AJ21

+1.0V_DEEP_SUS
R208 *0_6/S 700mA +VCCPRIM_1.0V
AK20 VCCPRIM_1P0_AK20

+1.0V_DEEP_SUS
R209 *0_4/S 33mA +VCCAPLLEBB
C197 1U/6.3V_4
N18 VCCAPLLEBB

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*SKL_ULT
REV = 1

VCCPGPPA AK15 +VCCPGPPA
VCCPGPPB AG15 +VCCPGPPB
VCCPGPPC Y16 +VCCPGPPC
VCCPGPPD Y15 +VCCPGPPD
VCCPGPPE T16 +VCCPGPPE
VCCPGPPF AF16 +VCCPGPPF
VCCPGPPG AD15 +VCCPGPPG

VCCPRIM_3P3_V19 V19
C186 1U/6.3V_4 +3V_DEEP_SUS

VCCPRIM_1P0_T1 T1 +VCCPRIM_1.0V_T1
R187 *0_6/S +1.0V_DEEP_SUS

VCCATS_1P8 AA1 +VCCATS_1.8V 6mA
R190 *0_4/S +1.8V_DEEP_SUS

VCCRTCPRIM_3P3 AK17 +VCCRTCPRIM_3.3V 1mA
R192 *0_4/S +3V_DEEP_SUS

VCCRTC_AK19 AK19
VCCRTC_BB14 BB14
+3V_RTC_2

20mils

Cb
DCPRTC BB10 DCPRTC
C191 0.1U/16V_4 +1.0V_DEEP_SUS

VCCCLK1 A14 +VCCCLK1
R195 *0_4/S 35mA

VCCCLK2 K19 +VCCCLK2
R198 *0_4/S 29mA

VCCCLK3 L21 +VCCCLK3
R200 *0_4/S 24mA

VCCCLK4 N20 +VCCCLK4
R202 *0_4/S 33mA

VCCCLK5 L19 +VCCCLK5
R203 *0_4/S 4mA

VCCCLK6 A10 +VCCCLK6
R204 *0_4/S 10mA

C195 1U/6.3V_4

GPP_B0/CORE_VID0 AN11 CORE_VID0 TP102
GPP_B1/CORE_VID1 AN13 CORE_VID1 TP103

+3V_DEEP_SUS
20mA +VCCPGPPA R184 *0_4/S
4mA +VCCPGPPB R185 *0_4/S
6mA +VCCPGPPC R186 *0_4/S
8mA +VCCPGPPD R189 *0_4/S
6mA +VCCPGPPE R191 *0_4/S
41mA +VCCPGPPG R193 *0_4/S

+1.8V_DEEP_SUS
160mA +VCCPGPPF R197 *0_4/S

+V3.3DX_1.5DX_ADO
R210 *0_4/S +3V

+1.0V_DEEP_SUS
C203 *1U/6.3V_4
C204 *22U/6.3V_6

0711 CQ
R211 100K change to 10K for 1.8V_DEEP_SUS issue

+3VS5
R211 10K_4
C205 1U/6.3V_4

U4
5 IN
4 IN
3 ON/OFF
OUT 1
GND 2
IC OTHER(5P) G5245AT11U

[35,39,40] SLP_SUS_ON

C210 *10P/50V_4

+3V_DEEP_SUS
C209 0.1U/16V_4

0409 CQ
Chagne P/N AL005245000 (RDC suggest)

+VCCATS_1.8V
C198 1U/6.3V_4

+3V_RTC_2
C199 0.1U/16V_4
C200 1U/6.3V_4

+VCCRTCPRIM_3.3V
C201 1U/6.3V_4
C202 0.1U/16V_4

+VCCPGPPB
C206 1U/6.3V_4

+VCCPGPPC
C207 1U/6.3V_4

+VCCPGPPE
C208 1U/6.3V_4

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Quanta Computer Inc.

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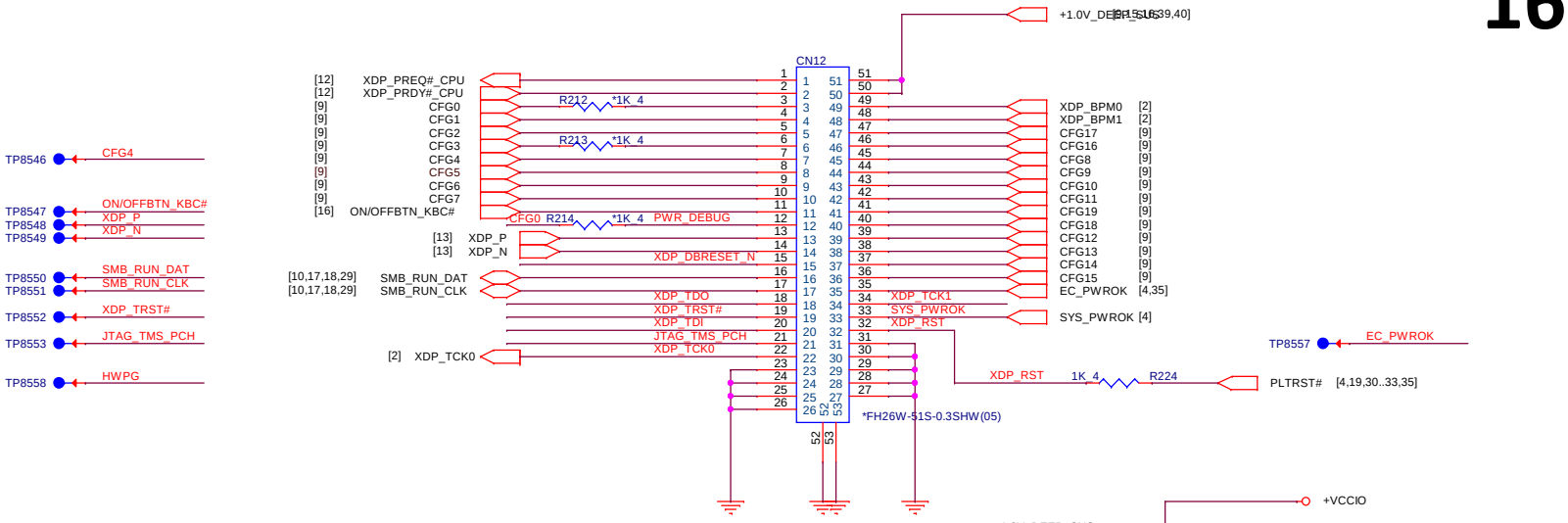
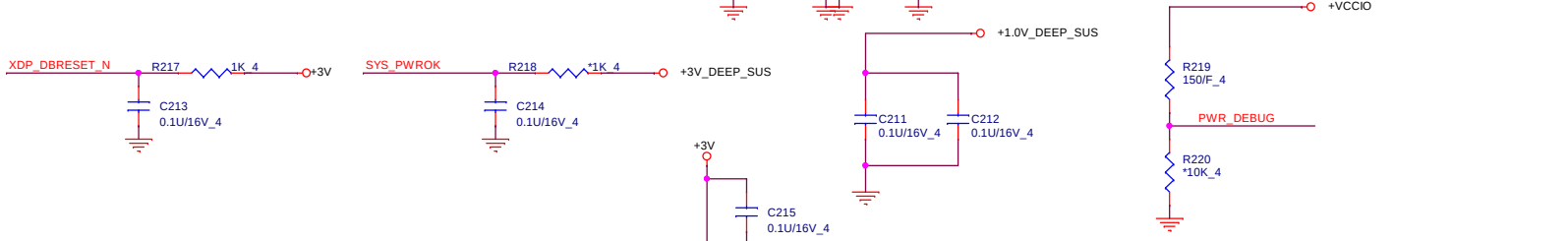
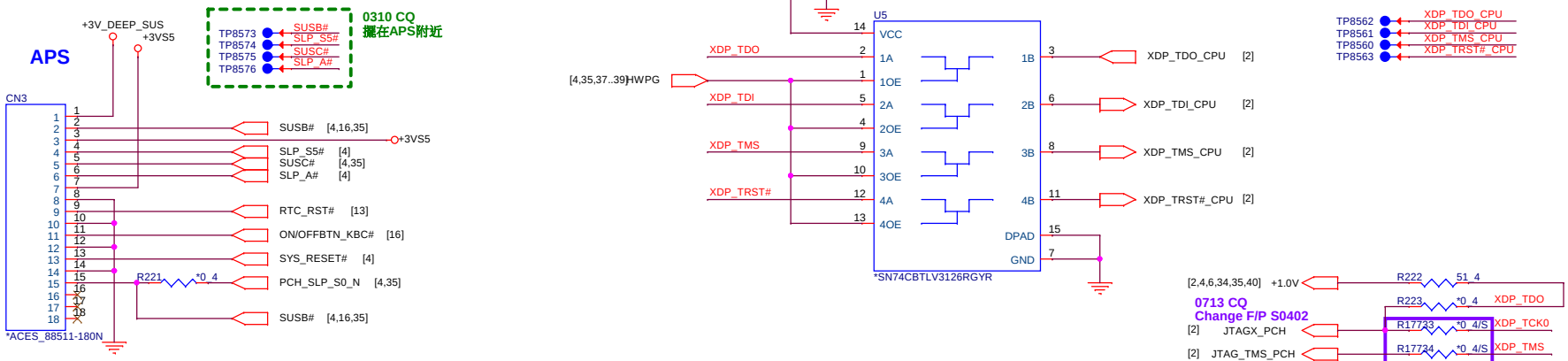
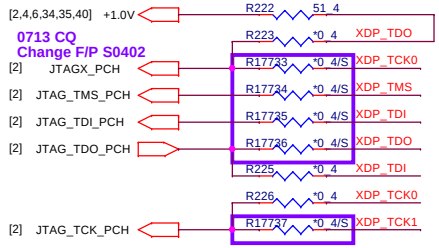
0322 CQ
Del repeat TP









[6,40]
[9,15,16,39,40]
[4,10..12,14,15,18]
[4,10,15,27,31,32,35,37..40,44,45,48]
[2,4,10..13,15,17..21,25..27,29,30,32,33,35,41,45,46]
+VCCIO
+1.0V_DEEP_SUS
+3V_DEEP_SUS
+3VS5
+3V

Quanta Computer Inc.	**PROJECT : LG9**	
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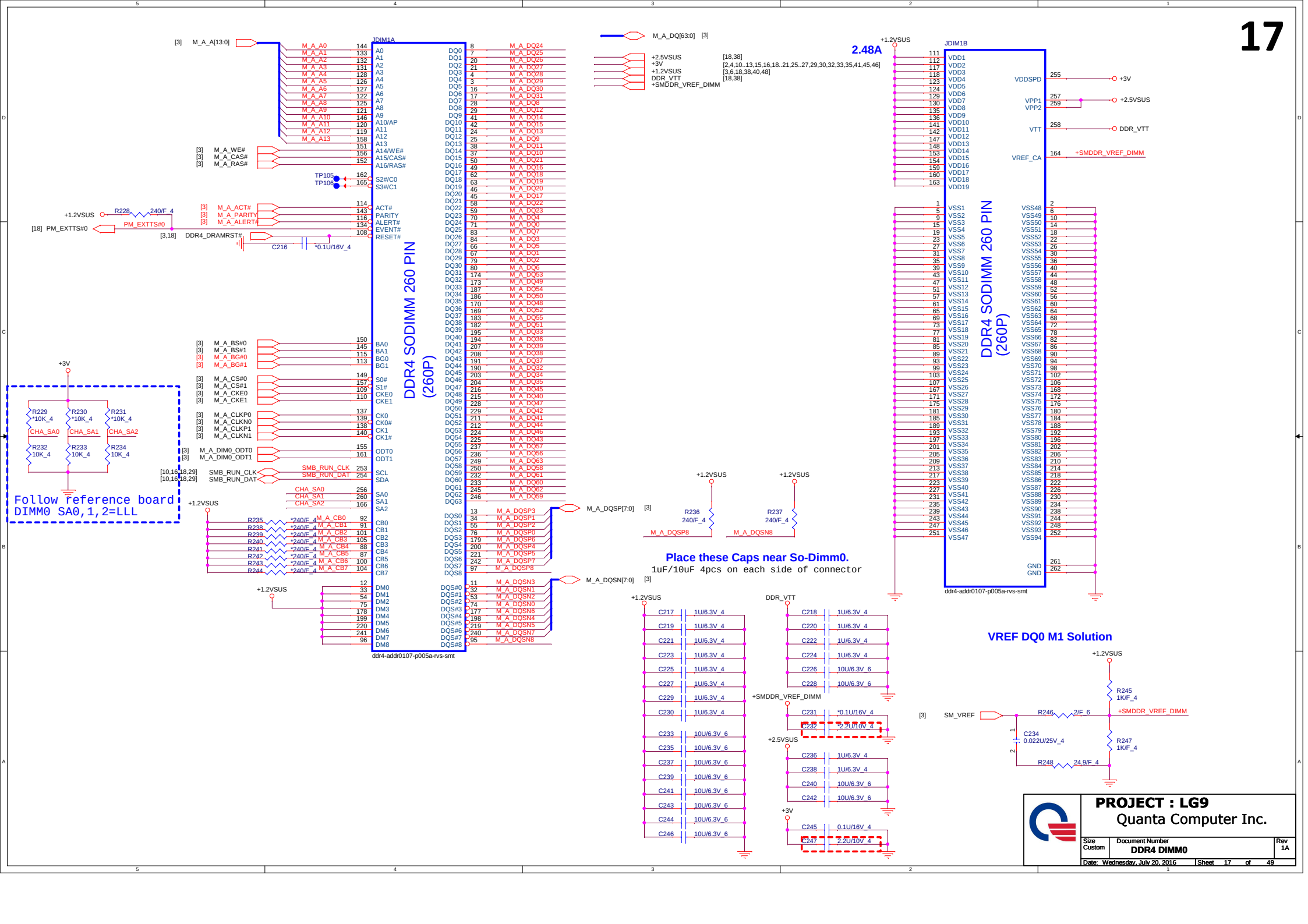
JDIM1A
DDR4 SODIMM 260 PIN (260P)
ddr4-addr0107-p005a-rvs-smt
JDIM1B
DDR4 SODIMM 260 PIN (260P)
ddr4-addr0107-p005a-rvs-smt
2.48A
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : LG9
Quanta Computer Inc.
DDR4 DIMM0
Size Custom
Document Number
Rev 1A
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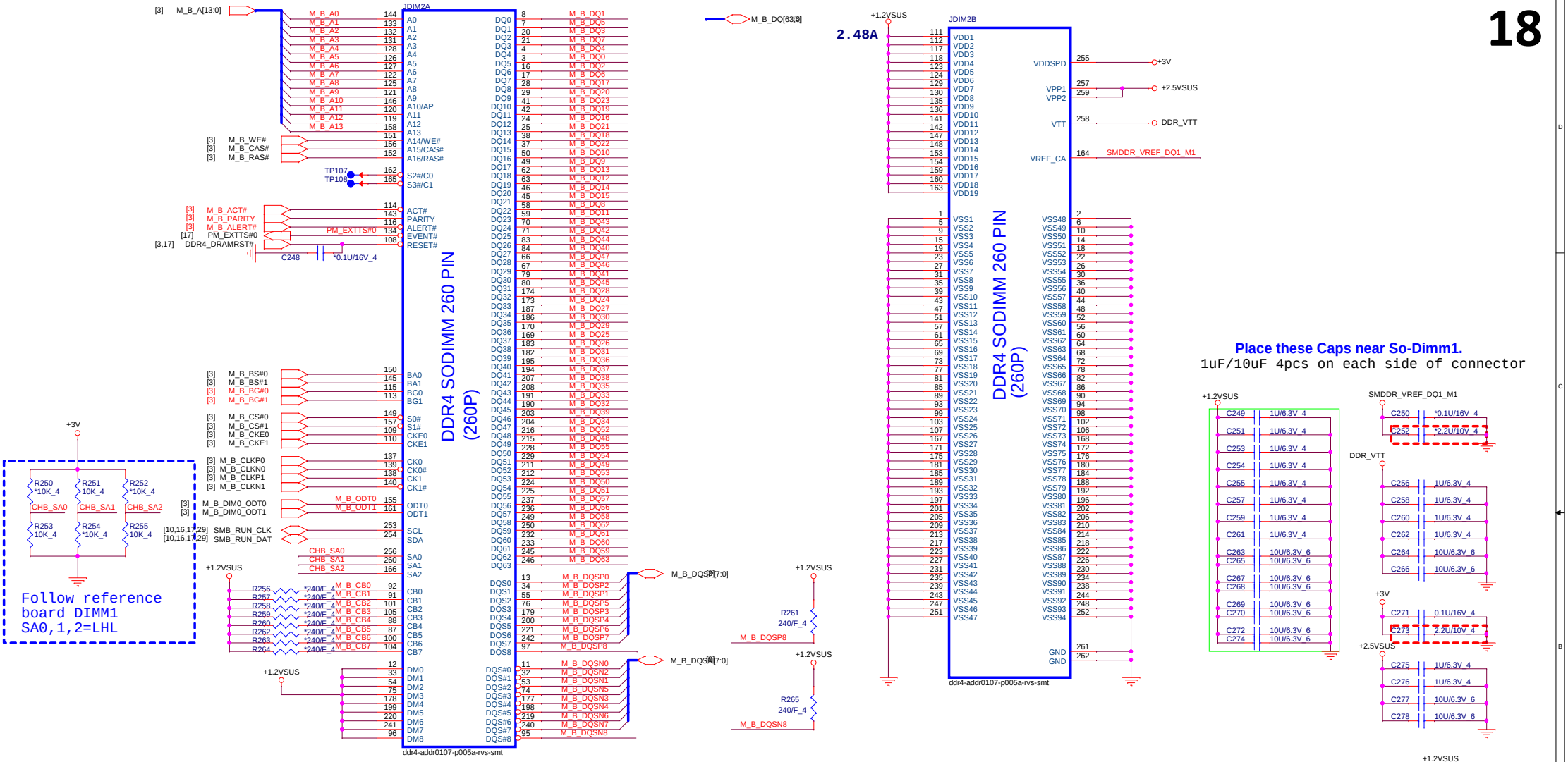

PROJECT : LG9			
Quanta Computer Inc.			
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PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

NVDD = 32.22 ~ 26.66 A

VDD33 = 56mA

0713 CQ
Change F/P S0402

0713 CQ
Change F/P S0603

0305 CQ
依NV建議，更改為AND Gate
Same as U1002

if stuff Da,Db,Ra,Rb
do not stuff Ua,Ub,Ca,Cb,Rc,Rd

Power up sequence

ALL 3.3V
+3VGFX & +3V3_AON

NVVDD
+VGACORE

PEX_VDD
+1.05V_GFX

FBVDDQ
+1.5V_GFX

- PEX_TSTCLK_OUT should be terminated with PEX_TSTCLK_OUT# using a 200 Ω resistor and made easily accessible for probing; default can be unstuffed.

17.2 TEST MODE

By default, pull-down the TESTMODE pin to GND with a 10 kΩ resistor. For ICT/boundary scan requirements, contact your NVIDIA AE.

- PEX_TERMP is used for internal calibration; pull-down this signal with a 2.49 kΩ, 1% resistor.

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R1012 10K/F_4 PS_FB_CLAMP F3

U1001B

NC	GF119
FB_CLAMP	GF117

2/14 FBA

0305 CQ
NV check , GDDR5 不需加下拉定
FBA_CMD2 , FBA_CMD18 , FBA_CMD3 ,
FBA_CMD5 , FBA_CMD19 pull down 10K
0324 CQ
改回DDR3 , 加回10K PD

FBA_ODT_L	FBA_CMD2	R1014	10K/F_4
FBA_ODT_H	FBA_CMD18	R1016	10K/F_4
FBA_RST#	FBA_CMD5	R1013	10K/F_4
FBA_CKE_L	FBA_CMD3	R1017	10K/F_4
FBA_CKE_H	FBA_CMD19	R1015	10K/F_4

[23]	FBA_CMD0	C27	FBA_CMD0
[23]	FBA_CMD1	C26	FBA_CMD1
[23]	FBA_CMD2	E24	FBA_CMD2
[23]	FBA_CMD3	F24	FBA_CMD3
[23,24]	FBA_CMD4	D27	FBA_CMD4
[23,24]	FBA_CMD5	D26	FBA_CMD5
[23,24]	FBA_CMD6	F25	FBA_CMD6
[23,24]	FBA_CMD7	F26	FBA_CMD7
[23,24]	FBA_CMD8	F23	FBA_CMD8
[23,24]	FBA_CMD9	G22	FBA_CMD9
[23,24]	FBA_CMD10	G23	FBA_CMD10
[23,24]	FBA_CMD11	G24	FBA_CMD11
[23,24]	FBA_CMD12	F27	FBA_CMD12
[23,24]	FBA_CMD13	G25	FBA_CMD13
[23,24]	FBA_CMD14	G27	FBA_CMD14
[23,24]	FBA_CMD15	G26	FBA_CMD15
[24]	FBA_CMD16	M24	FBA_CMD16
[24]	FBA_CMD17	M23	FBA_CMD17
[24]	FBA_CMD18	K24	FBA_CMD18
[24]	FBA_CMD19	K23	FBA_CMD19
[23,24]	FBA_CMD20	M27	FBA_CMD20
[23,24]	FBA_CMD21	M26	FBA_CMD21
[23,24]	FBA_CMD22	M25	FBA_CMD22
[23,24]	FBA_CMD23	K26	FBA_CMD23
[23,24]	FBA_CMD24	K22	FBA_CMD24
[23,24]	FBA_CMD25	J23	FBA_CMD25
[23,24]	FBA_CMD26	J25	FBA_CMD26
[23,24]	FBA_CMD27	J24	FBA_CMD27
[23,24]	FBA_CMD28	K27	FBA_CMD28
[23,24]	FBA_CMD29	K25	FBA_CMD29
[23,24]	FBA_CMD30	J27	FBA_CMD30
		J26	FBA_CMD31

0223 CQ
GDDR5 need add
0324 CQ
改回DDR3 Del FBA_CMD31

+1.5V_GFX

0305 CQ
NV check GDDR5 is 1.35V setting
0324 CQ
DDR3 use 1.5V setting

R1021 *60.4/F_4 F22 FBA_DEBUG0
R1022 *60.4/F_4 J22 FBA_DEBUG1

[23]	VMA_CLK0	D24	FBA_CLK0
[23]	VMA_CLK0#	D25	FBA_CLK0
[24]	VMA_CLK1	N22	FBA_CLK1
[24]	VMA_CLK1#	M22	FBA_CLK1

0223 CQ
Add for GDDR5 USE
0324 CQ
Del for DDR3

D18	FBA_WCK01
C18	FBA_WCK01
D17	FBA_WCK23
D16	FBA_WCK23
T24	FBA_WCK45
U24	FBA_WCK45
V24	FBA_WCK67
V25	FBA_WCK67

FB_PLLAVDD = 55mA

Add La (0402) for co-lay

L1001 *PBY160808T-300Y-N
L1002 HCB1005KF-330T30
+1.05V_GFX +FB_PLLAVDD
La
C1069 22U/6.3VS_6
C1070 0.1U/16V_4
C1071 0.1U/16V_4
C1072 0.1U/16V_4

F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22 FB_PLLAVDD

FB_PLLAVDD	GF119
FB_PLLAVDD	GF117

FB_DLLAVDD = 15mA

bga595-nvidia-n13p-gv2-s-a2 COMMON

FBA_D0	E18	VMA_DQ0	
FBA_D1	F18	VMA_DQ1	
FBA_D2	E16	VMA_DQ2	
FBA_D3	F17	VMA_DQ3	
FBA_D4	D20	VMA_DQ4	
FBA_D5	D21	VMA_DQ5	
FBA_D6	F20	VMA_DQ6	
FBA_D7	E21	VMA_DQ7	
FBA_D8	E15	VMA_DQ8	
FBA_D9	D15	VMA_DQ9	
FBA_D10	F15	VMA_DQ10	
FBA_D11	F13	VMA_DQ11	
FBA_D12	C13	VMA_DQ12	
FBA_D13	B13	VMA_DQ13	
FBA_D14	E13	VMA_DQ14	
FBA_D15	D13	VMA_DQ15	
FBA_D16	B15	VMA_DQ16	
FBA_D17	C16	VMA_DQ17	
FBA_D18	A13	VMA_DQ18	
FBA_D19	A15	VMA_DQ19	
FBA_D20	B18	VMA_DQ20	
FBA_D21	A18	VMA_DQ21	
FBA_D22	A19	VMA_DQ22	
FBA_D23	C19	VMA_DQ23	
FBA_D24	B24	VMA_DQ24	
FBA_D25	C23	VMA_DQ25	
FBA_D26	A25	VMA_DQ26	
FBA_D27	A24	VMA_DQ27	
FBA_D28	A21	VMA_DQ28	
FBA_D29	B21	VMA_DQ29	
FBA_D30	C20	VMA_DQ30	
FBA_D31	C21	VMA_DQ31	
FBA_D32	R22	VMA_DQ32	
FBA_D33	R24	VMA_DQ33	
FBA_D34	T22	VMA_DQ34	
FBA_D35	R23	VMA_DQ35	
FBA_D36	N25	VMA_DQ36	
FBA_D37	N26	VMA_DQ37	
FBA_D38	N23	VMA_DQ38	
FBA_D39	N24	VMA_DQ39	
FBA_D40	V23	VMA_DQ40	
FBA_D41	V22	VMA_DQ41	
FBA_D42	T23	VMA_DQ42	
FBA_D43	U22	VMA_DQ43	
FBA_D44	Y24	VMA_DQ44	
FBA_D45	AA24	VMA_DQ45	
FBA_D46	Y22	VMA_DQ46	
FBA_D47	AA23	VMA_DQ47	
FBA_D48	AD27	VMA_DQ48	
FBA_D49	AB25	VMA_DQ49	
FBA_D50	AD26	VMA_DQ50	
FBA_D51	AC25	VMA_DQ51	
FBA_D52	AA27	VMA_DQ52	
FBA_D53	AA26	VMA_DQ53	
FBA_D54	W26	VMA_DQ54	
FBA_D55	Y25	VMA_DQ55	
FBA_D56	R26	VMA_DQ56	
FBA_D57	T25	VMA_DQ57	
FBA_D58	N27	VMA_DQ58	
FBA_D59	R27	VMA_DQ59	
FBA_D60	V26	VMA_DQ60	
FBA_D61	V27	VMA_DQ61	
FBA_D62	W27	VMA_DQ62	
FBA_D63	W25	VMA_DQ63	

FBA_DQM0	D19	VMA_DM0
FBA_DQM1	D14	VMA_DM1
FBA_DQM2	C17	VMA_DM2
FBA_DQM3	C22	VMA_DM3
FBA_DQM4	P24	VMA_DM4
FBA_DQM5	W24	VMA_DM5
FBA_DQM6	AA25	VMA_DM6
FBA_DQM7	U25	VMA_DM7

FBA_DQS_WP0	E19	VMA_WDQS0
FBA_DQS_WP1	C15	VMA_WDQS1
FBA_DQS_WP2	B16	VMA_WDQS2
FBA_DQS_WP3	B22	VMA_WDQS3
FBA_DQS_WP4	R25	VMA_WDQS4
FBA_DQS_WP5	W23	VMA_WDQS5
FBA_DQS_WP6	AB26	VMA_WDQS6
FBA_DQS_WP7	T26	VMA_WDQS7

FBA_DQS_RN0	F19	VMA_RDQS0
FBA_DQS_RN1	C14	VMA_RDQS1
FBA_DQS_RN2	A16	VMA_RDQS2
FBA_DQS_RN3	A22	VMA_RDQS3
FBA_DQS_RN4	P25	VMA_RDQS4
FBA_DQS_RN5	W22	VMA_RDQS5
FBA_DQS_RN6	AB27	VMA_RDQS6
FBA_DQS_RN7	T27	VMA_RDQS7

FB_VREF_PROBE D23

VMA_DQ[63:0] VMA_DQ[63:0] [23,24]

VMA_DM[7:0] [23,24]

VMA_WDQS[7:0] [23,24]

VMA_RDQS[7:0] [23,24]

0223 CQ
Del VMA_RDQS[7:0]
GDDR5 NO USE
0324 CQ
Add for DRR3 use VMA_RDQS[7:0]

FBVDDQ + FBVDD = 3.116A

0305 CQ
NV check GDDR5 is 1.35V setting
0324 CQ
DDR3 use 1.5V setting

+1.5V_GFX

U1001D 12/14 FBVDDQ

C1060 0.1U/16V_4
C1061 0.1U/16V_4
C1062 1U/6.3V_4
C1065 1U/6.3V_4
C1066 4.7U/6.3V_6
C1063 4.7U/6.3V_6
C1067 10U/6.3V_6
C1064 22U/6.3V_6

B26	FBVDDQ
C25	FBVDDQ
E23	FBVDDQ
E26	FBVDDQ
F14	FBVDDQ
F21	FBVDDQ
G13	FBVDDQ
G14	FBVDDQ
G15	FBVDDQ
G16	FBVDDQ
G18	FBVDDQ
G19	FBVDDQ
G20	FBVDDQ
G21	FBVDDQ
H24	FBVDDQ
H26	FBVDDQ
J21	FBVDDQ
K21	FBVDDQ
L22	FBVDDQ
L24	FBVDDQ
L26	FBVDDQ
M21	FBVDDQ
N21	FBVDDQ
R21	FBVDDQ
T21	FBVDDQ
V21	FBVDDQ
W21	FBVDDQ

bga595-nvidia-n13p-gv2-s-a2 COMMON

0322 CQ
GDDR5 need change to 40.2 ohm
0324 CQ
DDR3 use 42.2 ohm

FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1018 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1019 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R1020 51.1/F_4

0322 CQ
GDDR5 need change to 60.4 ohm
0324 CQ
DDR3 use 51.1 ohm

Table 6-5. Default GPU Drive Calibration for DDR3

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3/DDR3L	1.5 V/1.35V	42.2 Ω	40.2 Ω	51.1 Ω

if stuff Da,Ra, do
not stuff Ua,Ca,Rb,Rc

GC6_FB_EN
DGPU_VC_EN
D1004 *BAT54CW-7-F
Da
R1123 Ra *100K/F_4
DGPU_FB_EN

For support GC6 2.0

+3V
Ua
U1003 NL17SZ32DFT2G
Ca C1068 0.1U/16V_4
[12,48] DGPU_PWR_EN R1023 *0_4
[46,48] DGPU_VC_EN R1024 *0_4/S
[12,22] GC6_FB_EN
Rc
DGPU_FB_EN [47]
Rb R1025 100K/F_4

0713 CQ
Change F/P S0402

SI 1127 CHANGE TO OR GATE

U1001F 13/14 GND

A2	GND	GND	M13
AB17	GND	GND	M15
AB20	GND	GND	M17
AB24	GND	GND	N10
AC2	GND	GND	N12
AC22	GND	GND	N14
AC26	GND	GND	N16
AC5	GND	GND	N18
AC8	GND	GND	P11
AD12	GND	GND	P13
AD13	GND	GND	P15
AD26	GND	GND	P17
AD15	GND	GND	P2
AD16	GND	GND	P23
AD18	GND	GND	P26
AD19	GND	GND	P5
AD21	GND	GND	R10
AD22	GND	GND	R12
AE11	GND	GND	R14
AE14	GND	GND	R16
AE17	GND	GND	R18
AE20	GND	GND	T11
AB11	GND	GND	T13
AF1	GND	GND	T15
AF11	GND	GND	T17
AF14	GND	GND	U10
AF17	GND	GND	U12
AF20	GND	GND	U14
AF23	GND	GND	U16
AF5	GND	GND	U18
AF8	GND	GND	U2
AG2	GND	GND	U23
AG26	GND	GND	U26
AB14	GND	GND	U5
B1	GND	GND	V11
B11	GND	GND	V13
B14	GND	GND	V15
B17	GND	GND	V17
B20	GND	GND	Y2
B23	GND	GND	Y23
B27	GND	GND	Y26
B5	GND	GND	Y5
B8	GND		
E11	GND		
E14	GND		
E17	GND		
E2	GND		
E20	GND		
E22	GND		
E25	GND		
E5	GND		
E8	GND		
H2	GND		
H23	GND		
H25	GND		
H5	GND		
K11	GND		
K13	GND		
K15	GND		
K17	GND		
L10	GND		
L12	GND		
L14	GND		
L16	GND		
L18	GND		
L2	GND		
L23	GND		
L25	GND		
L5	GND	GND	AA7
M11	GND	GND	AB7

bga595-nvidia-n13p-gv2-s-a2 COMMON

[19,21,48]
[19,21,22,46..48]
[19,22,34,48]
[23,24,47]
[2,4,10..13,15..19,21,25..27,29,30,32,33,35,41,45,46]

+1.05V_GFX
+3V_GFX
+3V_AON
+1.5V_GFX
+3V

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16x [Memory]	1A

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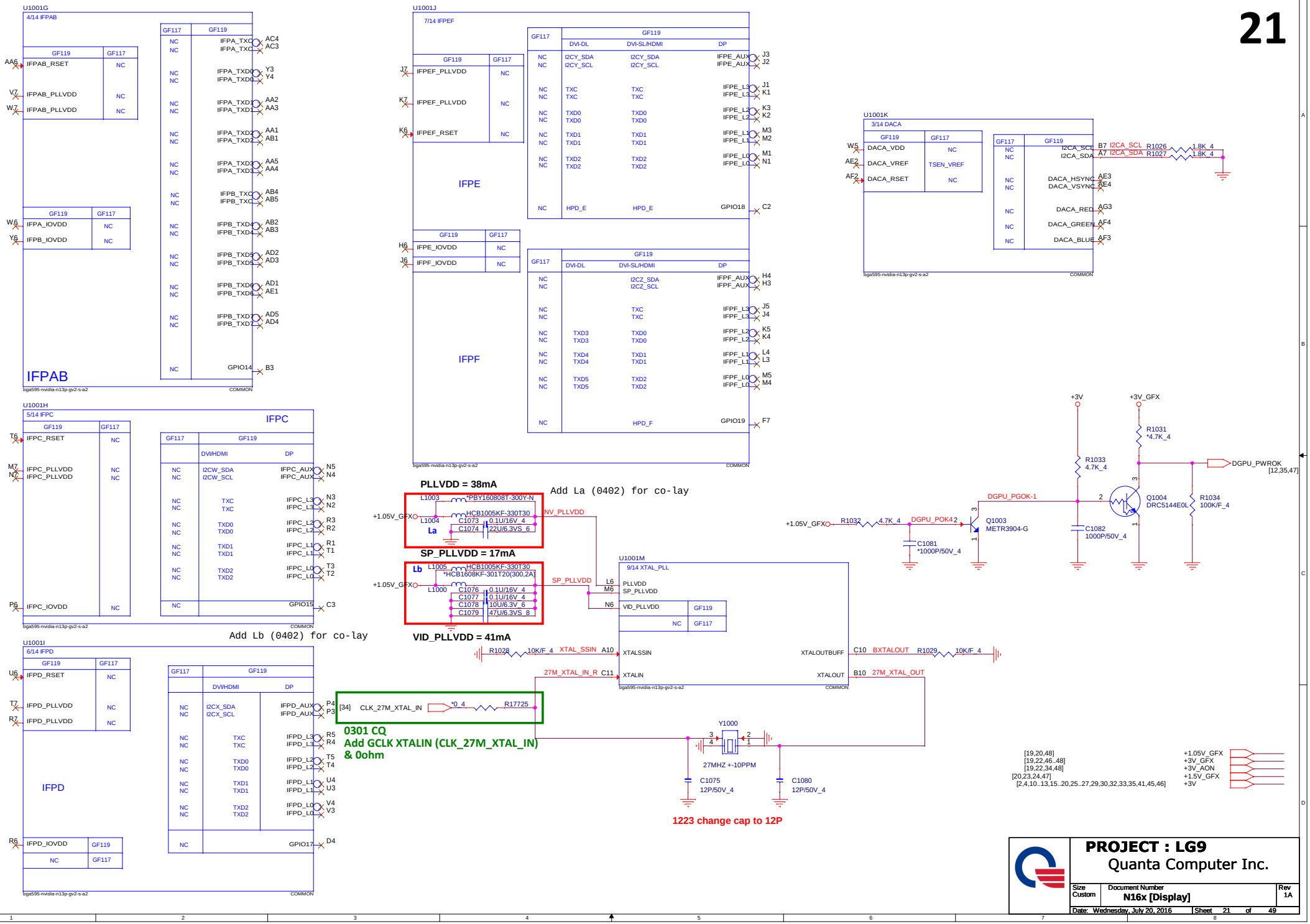
U1001G
4/14 IFPAB
IFPAB
U1001J
7/14 IFPEF
IFPE
IFPF
U1001K
3/14 DACA
U1001H
5/14 IFPC
IFPC
U1001I
6/14 IFPD
IFPD
U1001M
9/14 XTAL_PLL
PLLVDD = 38mA
Add La (0402) for co-lay
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
Add Lb (0402) for co-lay
0301 CQ
Add GCLK XTALIN (CLK_27M_XTAL_IN)
& 0ohm
1223 change cap to 12P
Y1000
27MHZ +-10PPM
PROJECT : LG9
Quanta Computer Inc.
Size Custom
Document Number N16x [Display]
Rev 1A
Date: Wednesday, July 20, 2016
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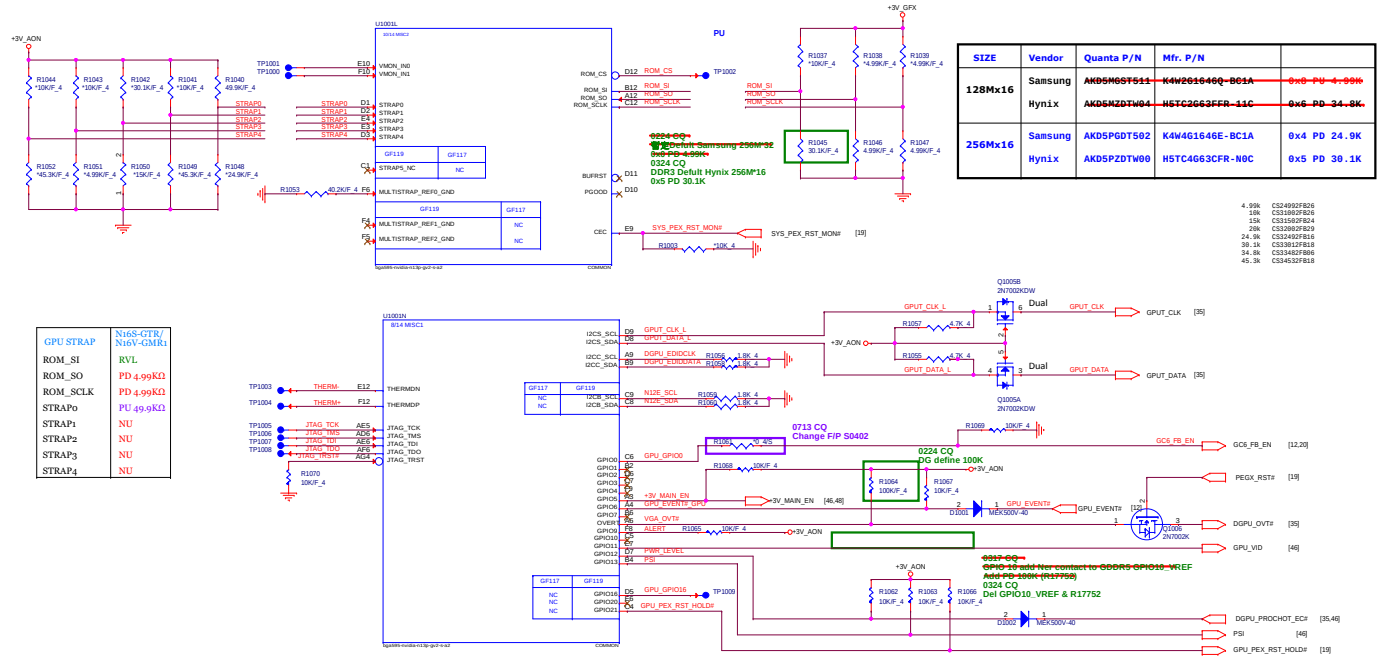

SIZE	Vendor	Quanta P/N	Mfr. P/N	
128Mx16	Samsung	~~AKD5MGST511~~	~~K4W2G1646Q-BC1A~~	~~0x8 PU 4.99K~~
	Hynix	~~AKD5MZDTW04~~	~~H5TC2G63FFR-11C~~	~~0x6 PD 34.8K~~
256Mx16	Samsung	AKD5PGDT502	K4W4G1646E-BC1A	0x4 PD 24.9K
	Hynix	AKD5PZDTW00	H5TC4G63CFR-N0C	0x5 PD 30.1K

GPU STRAP	N16S-GTR/ N16V-GMR1
ROM_SI	RVL
ROM_SO	PD 4.99KΩ
ROM_SCLK	PD 4.99KΩ
STRAPo	PU 49.9KΩ
STRAP1	NU
STRAP2	NU
STRAP3	NU
STRAP4	NU

Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	GC6_FB_EN	O	FB Enable for GC6 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing for GC6 2.0, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO6	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10 kΩ pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset monitor	10 kΩ pull-up to 3V3_AON unless actively driven
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AON; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AON
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

Table 13. N16V-GMR1 and N16S-GMR/-GTR DDR3 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(Mhz)	Memory Date Code Minimum	Status
DDR3	1.5V/ 1.5V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x6	1000	N/A	Production ready
				Micron	MT41J128M16JT-093G:K	K-die	0x7	1000	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0x8	1000	N/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x0	1000	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x4	1000	N/A	Production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0x5	1000	N/A	Production ready
				Micron	MT41J256M16LY-091G:N	N-die	0x3	1000	N/A	Post-production candidate
			Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x0	1000	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0xD	1000	N/A	Production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0xC	1000	N/A	Production ready
				Micron	MT41J256M16LY-091G:N	N-die	0x7	1000	N/A	Post-production candidate

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

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Rank0

U1004 — VRAM_DDR3_HYNIX_256MX16 (96-BALL SDRAM DDR3)

U1005 — VRAM_DDR3_HYNIX_256MX16 (96-BALL SDRAM DDR3)

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

stuff R1124 for
Hynix 8Gb DDP VRAM

stuff R1125 for
Hynix 8Gb DDP VRAM

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN_FBAO_ODT1	J1	NC/ODT1
SNN_FBAO_CKE1	J9	NC/CKE1
SNN_FBAO_CS1	L1	NC/CS1
SNN_FBAO_ZQ1	L9	NC/ZQ1

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Custom	VRAM1 DDR3 - RANK0	1A

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Rank0

1114SWAP

1114SWAP

1114SWAP

1114SWAP

U1006

U1007

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

stuff R1124 for
Hynix 8Gb DDP VRAM

stuff R1124 for
Hynix 8Gb DDP VRAM

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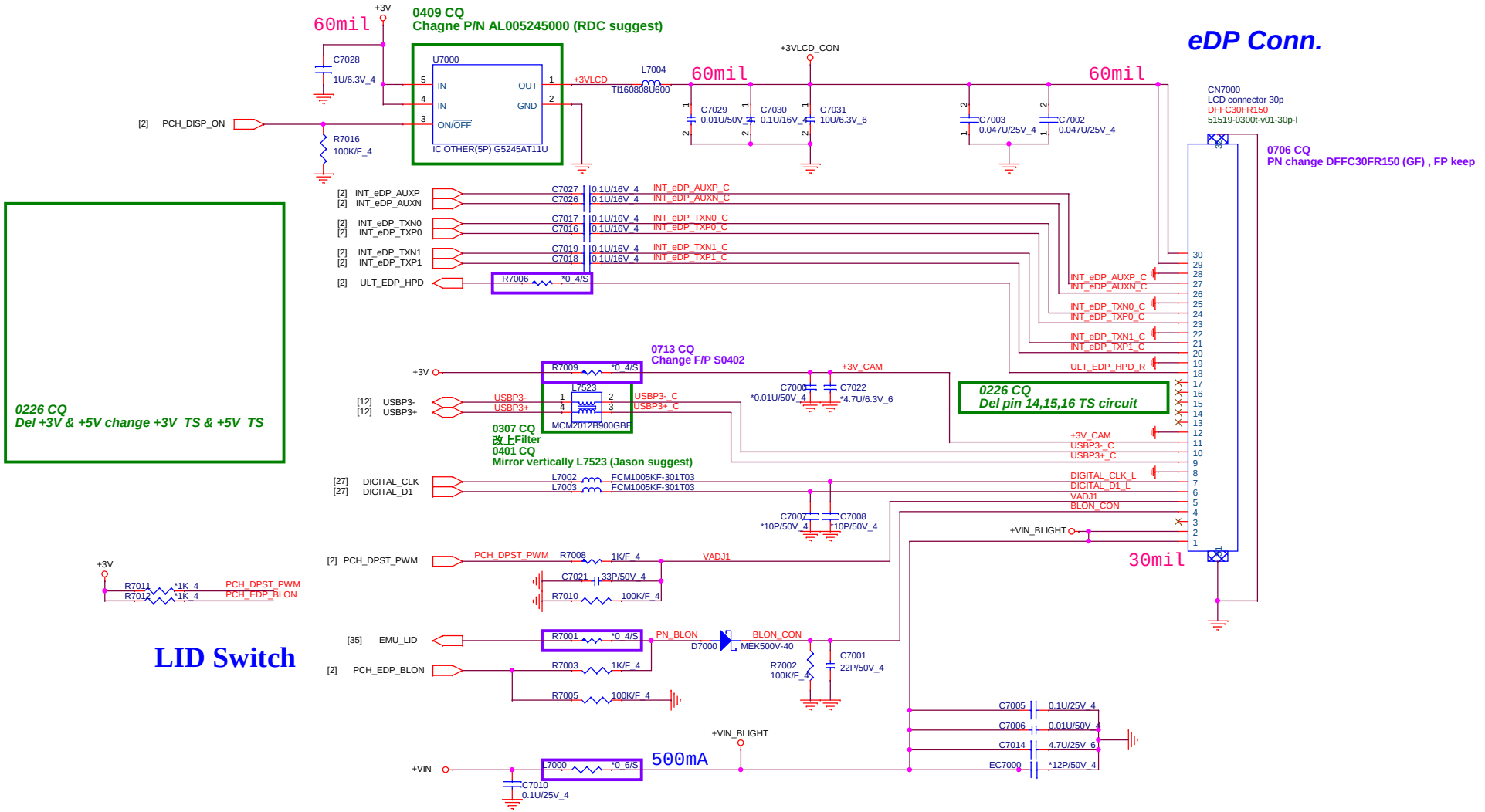
0219 CQ
Re-draw & Compare OK

eDP Conn.



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~~0301 CQ~~
~~Del HDMI 2.0 circuit , Change to HDMI 1.4~~
~~Use TWL circuit~~

0305 CQ
Del TWL HDMI circuit , change to G31 circuit

U8502
*AZ1043-04F.R7G

11/23 Reserve ESD chip

U8503
*AZ1043-04F.R7G

EMI Solution
0106 EMI Solution 120

0714 CQ
Change 0 ohm to 220 ohm

0714 CQ
C8631上件

0706 CQ
PN change DFHD19MR449 (GF) , FP keep

SSM14 spec is 40V 1A H=1.4mm(Max)
30 mils

0308 CQ
移除多餘net name , HDMI_DET_C

HDMI SMBus Isolation

Close to HDMI connector
Close to Q33

0305 CQ
Follow TWL USB Charger IC circuit

USB 2.0/3.0 Combo

0305 CQ
Need check EC pin

0713 CQ
Change F/P S0402

TPS2546
High Active

IC current limit is 2A
Ios = 48000/RILIMo

100 mils (Iout=2.5A)
BDB2047FVJ-GE2(MSOP)
Active Low

80 mils (Iout=2A)

USB 3.0

2A

0524 CQ
L7502 mirror Vertically(layout request)

USB 3.0

0706 CQ
USB3 PN change DFHS09FR707 (GF) , FP keep

0524 CQ
C8255 pin net swap (layout request)

11/23 Reserve ESD chip

0305 CQ
USB3 cricuit Change Page 28 to 26

0525 CQ
L24 mirror Vertically(layout request)

0307 CQ
解除Short pad

0312 CQ
換一USB net EDS part

0525 CQ
C8607 pin net swap (layout request)

0523 CQ
Change USB singel ESD part to SP3010-04UTG
Del C8608,C8609,C8524,C8525 , Add D7904,D7905

0524 CQ
Change D7904,D7905 net › layout request
D7905 swap pin net 5,6pin to R369 , 4,7pin to R366 (layout request)

0330 CQ
Fix USB2 FP usb-usb-04hjab-4p
PN DFHS04FR693

0509 CQ
Swap + & - , Pin define error

0412 CQ
SWAP

0409 CQ
與U7501使用同一顆 (OC : 3.2A)

0701 CQ
換BOT上件
DFHS04FR506 & usb-uarc6-4k1926-4p-r

0706 CQ
Change C8623 CH7151M8601 , FP cc3528-2h

0412 CQ
C8624,C8626 change PN CH4103K1B08 RDC suggest)

0318 CQ
Add USB2.0 circuit

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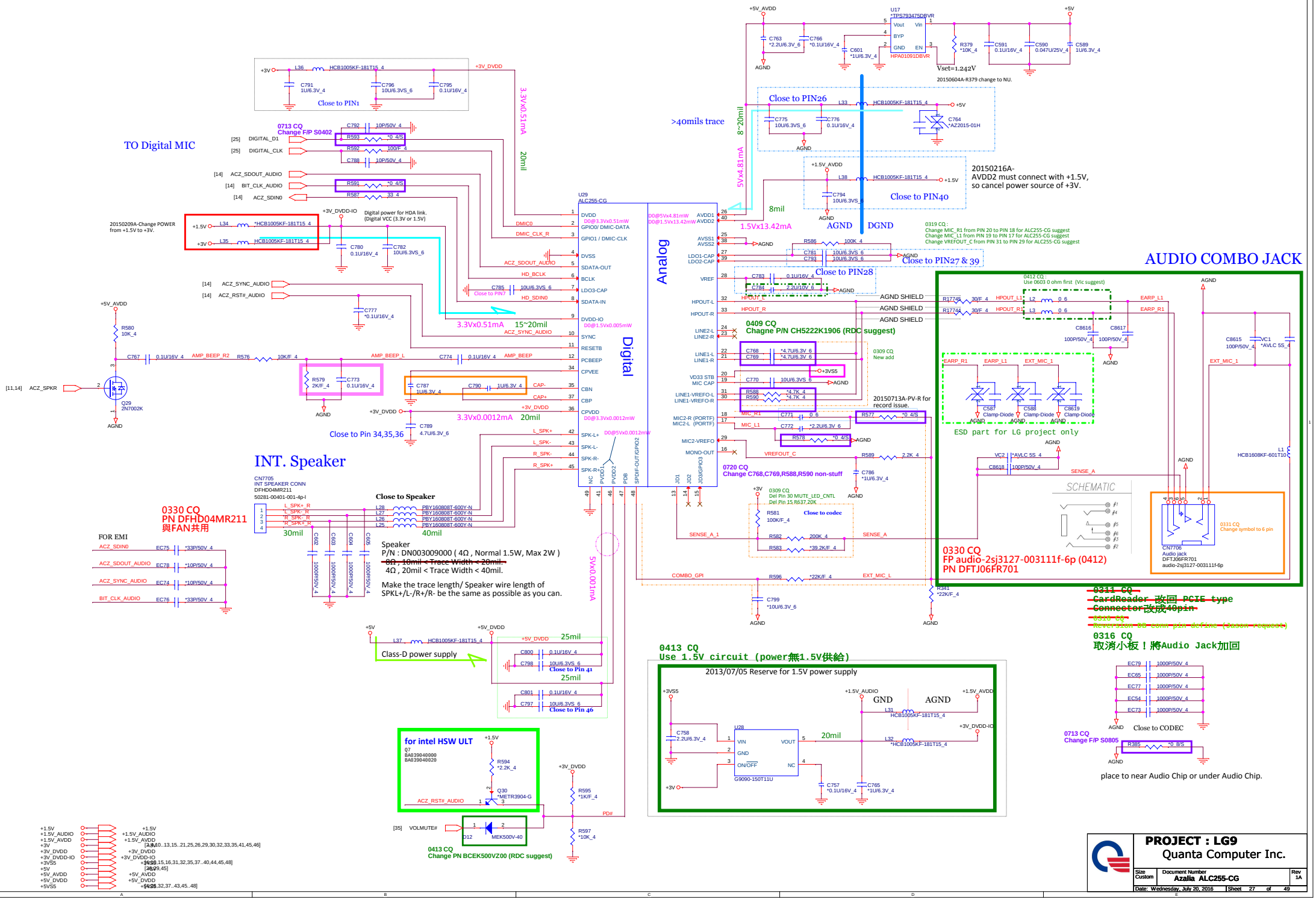

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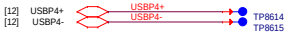

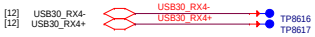

0412 CQ
刪除TypeC線路，保留USB & ID2 線段

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KEYBOARD Con.

need check pin define

[35] MY[0..17] MY[0..17]
[35] MX[0..7] MX[0..7]

196319-32021-3-32p-l
DFFC32FR025

KB Connector
CN6500

0307 CQ
Del CAPSLED# & MUTE_LED_CNTL cricuit
(Use TWL KB)
0411 Dennis
Swap KB Pin define for ME request

KEYBOARD PULL-UP

RP6500
RP6501
*10P8R-8.2K
R6506 *8.2K_4 MY16
R6507 *8.2K_4 MY17

0406 CQ
Swap pin for layout
0412 CQ
Swap pin for layout again

[35] MBATLED0#

HDD

0706 CQ
PN change DFFC10FR110 (GF) , FP keep

HD4600
SATA_TXP0_C C4600 0.01U/50V_4 SATA_TXP0 [12]
SATA_TXN0_C C4601 0.01U/50V_4 SATA_TXN0 [12]
SATA_RXN0_C C4602 0.01U/50V_4 SATA_RXN0 [12]
SATA_RXP0_C C4603 0.01U/50V_4 SATA_RXP0 [12]
+5V
C4604 *10U/6.3VS_6
C4605 10U/6.3VS_6
C4606 0.1U/16V_4

SATA HDD
51625-01001-001-10p-l
DFFC10FR110

60mil

[2,4,10..13,15..21,25..27,30,32,33,35,41,45,46]
[6,13,31,34..37,44]
[26,27,45]
[45]
[25]
[25,36..39,41..44,46,47,49]

+3V
+3VPCU
+5V
+3VSUS
+3V_CAM
+VIN

0307 CQ
刪除SATA LED雙色燈 circuit

0226 CQ
Del IR CAM circuit

0316 CQ
Add LED circuit
(小板移植)

+3VPCU
R17749 *10K_4
R17750 *10K_4
BATLOW# L
Q7704A *2N7002KDW
Q7704B *2N7002KDW
R17751 *0_4/S

0713 CQ
Change F/P S0402

0508 CQ
Change LED1 . LED2 , LED3 F/P ledltw-110uc5-3p

BAT LED
LED3 3P WHITE LED
R17748 330_6 +3VPCU
C8622 *AVLC 5S_4

SATA LED
[12] SATA_LED#
LED1 3P WHITE LED
R17746 330_6 +3V
C8620 *AVLC 5S_4

0517 CQ
Add PWR BTN LED
0518 CQ
Change LED3002 P/N & FP

PWR BTN LED
[29,31] DEEP_PWRLED#
LED3002 3P WHITE LED
R17754 330_6 +3VPCU
C8632 *AVLC 5S_4

PWR LED
[29,31] DEEP_PWRLED#
LED2 3P WHITE LED
R17747 330_6 +3VPCU
C8621 *AVLC 5S_4

FAN

1116 DB modify pindefine

[35] FAN1SIG
+3V R7201 4.7K_4
靠近EC
[35] FAN1_PWM
+5V
C7200 10U/6.3VS_6
C7201 0.1U/16V_4
FAN7201
FAN CONN
DFHD04MR211
50281-00401-001-4p-l

FAN1_PWM C7202 *220P/50V_4
FAN1SIG C7203 *220P/50V_4

0330 CQ
PN DFHD04MR211
FP 50281-00401-001-4p-l (0408)

KB LIGHT CONN

0307 CQ
Del KB LIGHT circuit

Touch Pad Connector

15 mils

+3VSUS
R6602 4.7K_4 TPCLK
R6603 4.7K_4 TPDATA
C6600 0.1U/16V_4
C6601 10P/50V_4
C6602 10P/50V_4
[35] TPDATA
[35] TPCLK
L6600 HCB1005KF-330T3
L6601 HCB1005KF-330T3
TPDATA-1
TPCLK-1
TP_SMB_CLK
TP_SMB_DATA
CN6600
TP Connector
DFFC06FR192
88513-0601-6p-l-smt

0412 CQ
Swap pin (TP定義相反)

Q6600A 2N7002KDW
Q6600B 2N7002KDW
Dual
[10,16..18] SMB_RUN_CLK
[10,16..18] SMB_RUN_DAT
TP_SMB_CLK
TP_SMB_DATA
R6600 4.7K_4
R6601 4.7K_4
+3V
+3VSUS

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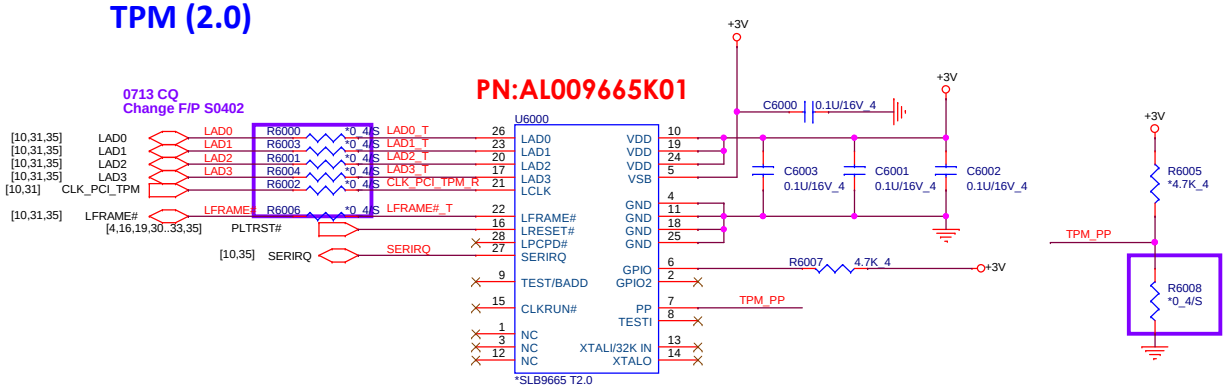
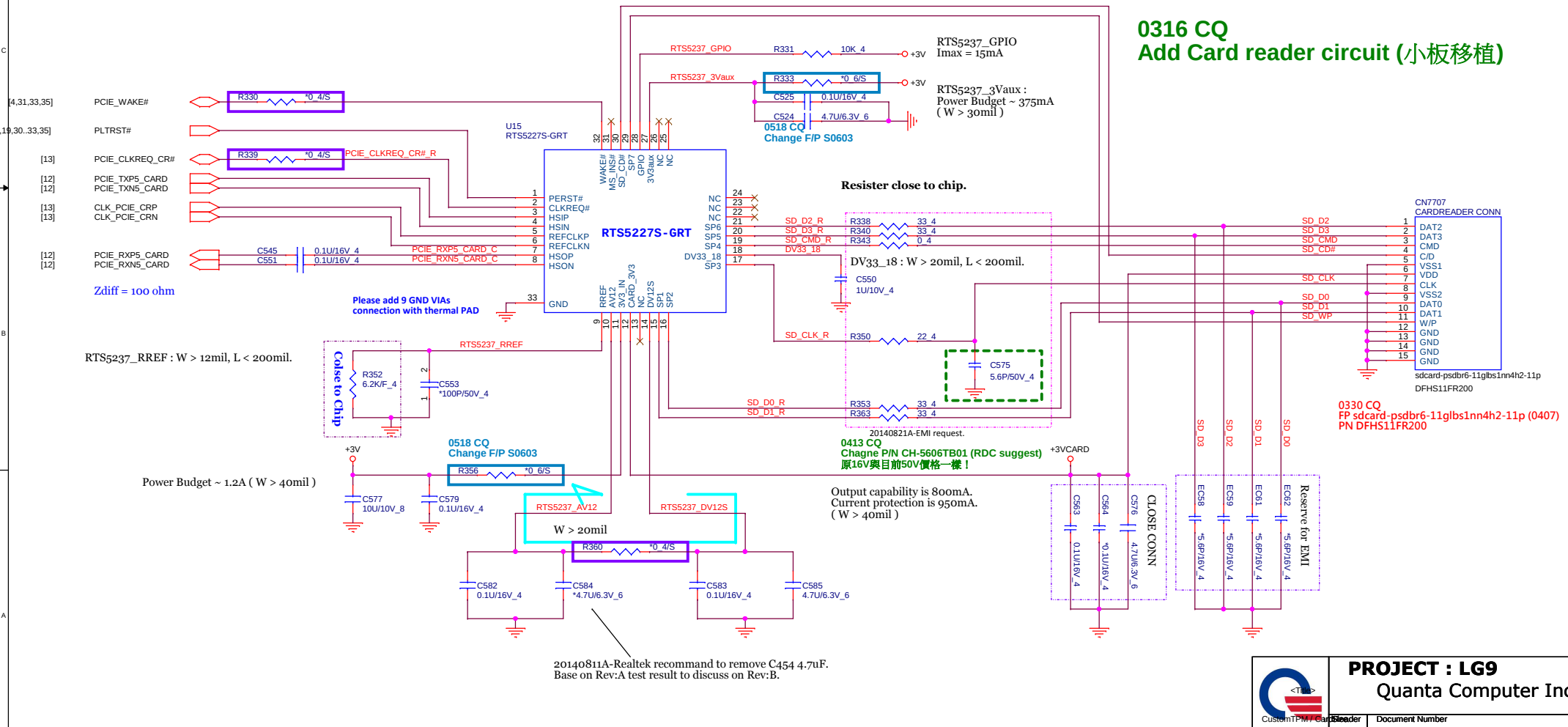
TPM (2.0)



0307 CQ
Del G-sensor circuit

0316 CQ
Add Card reader circuit (小板移植)



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Quanta Computer Inc.	
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Mini Card WLAN/BT(Option)

+3VPCU
R5001 10K_4
Q5002 2N7002K
[35] EC_AOCS
R5002 200K_4
C5005 0.022U/25V_4
+3VS5
Q5001 AO3409
+3V_AOCS
+3V_WLAN_P
C5000 *0.1U/16V_4
80mil

C5001 0.1U/16V_4
C5002 0.1U/16V_4
C5003 0.1U/16V_4
C5004 10U/6.3VS_6

0329 CQ
改FP ngff-apci0136-p001a-75p-ke (0418)
PN DFHS75FR326

[4,10,15,16,27,32,35,37..40,44,45,48] +3VS5

CN5000 NGFF

[12] USBP7+
[12] USBP7-

GND, USB_D+, USB_D-, GND, SDIO CLK(O), SDIO CMDI(O), SDIO DAT0(IO), SDIO DAT1(IO), SDIO DAT2(IO), SDIO DAT3(IO), SDIO Wake(I), SDIO Reset, KEY1, KEY2, KEY3, KEY4, GND, PETp0, PETn0, GND, PERp0, PERn0, GND, REFCLKP0, REFCLKN0, GND, CLKREQ0#, PEWake0#, GND, PETp1, PETn1, GND, PERp1, PERn1, GND, Reserved1, Reserved2, GND

3.3Vaux, 3.3Vaux, LED#1, PCM_CLK, PCM_SYNC, PCM_IN, PCM_OUT, LED#2, GND, UART Wake, UART Rx, Key 5, Key 6, Key 7, Key 8, UART Tx, UART CTS, UART RTS, Clink RESET, CLink DATA, CLink CLK, COEX3, COEX2, COEX1, SUSCLK(32KHz), PERST0#, W_DISABLE2#, W_DISABLE1#, NFC I2C SM DATA, NFC I2C SM CLK, ALERT#, RESERVED, UIM_SWP/PERST1#, UIM_POWER_SNK, UIM_POWER_SRC, 3.3Vaux, 3.3Vaux, GND, GND

WLAN_NGFF CONN (E-Key)
ngff-apci0136-p001a-75p-ke
DFHS75FR326

+3V_WLAN_P
80mil
WLAN_LED#
R5002 4.7K_4
R5004 *0_4/S
+3V_WLAN_P
RF_LINK#
0310 CQ
需與EC確認
0713 CQ
Change F/P S0402

Q5003 2N7002KDW
BT_OFF [14]
INT_BT_OFF#
RF_OFF_PCH [4]
INT_RF_OFF#

PLTRST# [4,16,19,30,32,33,35]
INT_BT_OFF#
INT_RF_OFF#
R5006 10K_4
R5007 10K_4
+3V_WLAN_P

LAD0 [10,30,35]
LAD1 [10,30,35]
LAD2 [10,30,35]
LAD3 [10,30,35]

0413 CQ
Add Q5004 , R5009 (G31 Add for MV change)

+3V_WLAN_P
R5009 *10K_4
Q5004 *2N7002K
R5005 0_4
[13] PCIE_CLKREQ_WLAN#

[12] PCIE_TXP6_WLAN
[12] PCIE_TXN6_WLAN
[12] PCIE_RXP6_WLAN
[12] PCIE_RXN6_WLAN
[13] CLK_PCIE_WLANP
[13] CLK_PCIE_WLANN
REQ_WLAN#
MINICAR_PME#

Support Wake Function(Reserve)

+3V_WLAN_P
R5008 *10K_4
Q5000 *DRC5144E0L
[4,30,33,35] PCIE_WAKE#
MINICAR_PME#

PCIE_WAKE# EC5002 *220P/50V_4

[10,30] CLK_PCI_TPM
[10,30,35] LFRAME#
LFRAME#

PAD/HOLE

0328 CQ
Add H1~H6 follow G31

H1 *H-TC315IC182BC197D150P2
H2 *H-TC315IC182BC197D150P2
H3 *H-TC315IC182BC197D150P2
H4 *H-TC315IC182BC197D150P2
H5 *H-TC276IBC197D150P2
H6 *H-TC276IBC197D150P2

0706 CQ
Change H8 FP H-LG9-H8

0526 CQ
Change H9 FP h-tic150bc197d110p2 (Layout request)

H7 *h-tc236ibc197d98p2
H8 *H-LG9-H8
H9 h-tic150bc197d110p2
H10 *h-tc315ibc138d87p2
H11 *H-C118D87P2
H12 H-TC217IC217D110PT
H13 *O-LG9-2
H14 *O-LG9-3

0707 CQ
Change H11 H-C118D87P2

H15 *O-LG9-4
H16 *h-tc315ibc236d98p2
H17 *O-LG9-1
H18 *SPAD-C197NP
H19 *SPAD-C197NP

0518 CQ
Change F/P H16 h-tc315ibc236d98p2

0602 CQ
Add H20 for EMI GND PAD

H20 *SPAD-RE213X114NP

0707 CQ
Change H20 FP SPAD-RE213X114NP

0508 CQ
Add H9 & H12 nut P/N (MBT01001010 , MBG34001010)

0518 CQ
Change F/P H7 h-tc236ibc197d98p2
Change F/P H8 h-tc158ibc118d98x87p2
Change F/P H9 h-tc197ibc150d110p2
Change F/P H10 h-tc315ibc138d87p2
Change F/P H11 h-c118d87x98p2
Change F/P H16 h-tc315ibc236d87p2
Add PAD1 spad-re232x169np
Add PAD2 spad-re236x59np

0518 CQ
Add PAD3 spad-re232x169np

PAD1 *spad-re232x169np
PAD2 *spad-re236x59np
PAD3 *spad-re232x169np

0408 CQ
Add H7~H19

0418 CQ
Final Hole
H1 / H2 / H3 / H4 => H-TC315IC182BC197D150P2
H5 / H6 => H-TC276IBC197D150P2
H11 => H-C118D87P2
H13 => O-LG9-2
H14 => O-LG9-3
H15 => O-LG9-4

H7 => H-TC236IBC197D87P2 (0418E再次更新)

PAD4 *SPAD-RE265X180NP
PAD5 *SPAD-RE630X55NP

0713 CQ
Add PAD3,PAD4 SPAD-RE265X180NP、SPAD-RE630X55NP

+3VPCU
R5140 10K_4
0307 CQ
Set net name DEEP_PWRLED#
DEEP_PWRLED#
DEEP_PWRLED# [29]

[35] PWR_LED#
PWR_LED#
Q5106 DRC5144E0L
C8508 0.1U/16V_4

0509 CQ
Q5106 2N7002K change to DRC5144E0L
Add 0.1u/16V (Follow G34)

SW7900 sw-tme-533b-q-tr-6p
R7900 1K_4
NBSWON1#
NBSWON1# [35]
C7902 0.1U/16V_4
C7901 *AVLC 5S

[13] +BAT_RTC
[6,13,29,34..37,44] +3VPCU

T1 T2 T3 T4 T5 T6

0307 CQ
Change net name to LID_EC#
0311 CQ
改回 LID# (原設power端)
LID_EC#
LID_EC# [35]
0509 CQ
Change net name to LID_EC#

+BAT_RTC
20mils
D7903 MEK500V-40
+3VPCU
HE7900 APX9132H AI-TRG
C7900 *2.2U/10V_6

+BAT_RTC
20mils
C7903 0.1U/16V_4
C7904 *2.2U/10V_6

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~~0226 CQ~~
~~Del PCIE_port11~~
0311 CQ
Add PCIE SSD function for LG request

0315 CQ
Remove 0 ohm & Net name
R17739 & R17740
PCIE_RXN11_SSD_C & PCIE_RXP11_SSD_C

0525 CQ
Add PICe SSD to 4ch

0525 CQ
Change Symbol & Add pin12,14,16,18 to +3V_SSD (Rico request)

32

CN4901
SSD_NGFF_CONN_75P_M-KEY

NGFF

80mil

[12] PCIE_RXN9_SSD
[12] PCIE_RXP9_SSD
[12] PCIE_TXN9_SSD
[12] PCIE_TXP9_SSD
[12] PCIE_RXN10_SSD
[12] PCIE_RXP10_SSD
[12] PCIE_TXN10_SSD
[12] PCIE_TXP10_SSD
[12] PCIE_RXN11_SSD
[12] PCIE_RXP11_SSD
[12] PCIE_TXN11_SSD
[12] PCIE_TXP11_SSD
[12] PCIE_RXP12_SSD
[12] PCIE_RXN12_SSD
[12] PCIE_TXN12_SSD
[12] PCIE_TXP12_SSD
[13] CLK_PCIE_SSDN
[13] CLK_PCIE_SSDP

C8634 0.22U/10V_4 PCIE_TXN9_SSD_DC_R
C8633 0.22U/10V_4 PCIE_TXP9_SSD_DC_R
C8636 0.22U/10V_4 PCIE_TXN10_SSD_DC_R
C8635 0.22U/10V_4 PCIE_TXP10_SSD_DC_R
C4919 0.22U/10V_4 SATA_TXN1_C
C4920 0.22U/10V_4 SATA_TXP1_C
R8557 *0_4/S PCIE_RXP12_SSD_DC_R
R8558 *0_4/S PCIE_RXN12_SSD_DC_R
C8519 0.22U/10V_4 PCIE_TXN12_SSD_DC_R
C8520 0.22U/10V_4 PCIE_TXP12_SSD_DC_R

1	CONFIG3/GND	3.3Vaux	2
3	GND	3.3Vaux	4
5	PERN3	N/A	6
7	PERP3	N/A	8
9	GND	DAS/DSS#(O)(OD)	10
11	PETN3	3.3Vaux	12
13	PETP3	3.3Vaux	14
15	GND	3.3Vaux	16
17	PERN2	3.3Vaux	18
19	PERP2	N/A	20
21	CONFIG0/GND	N/A	22
23	PETN2	N/A	24
25	PETP2	N/A	26
27	GND	N/A	28
29	PERN1	N/A	30
31	PERP1	N/A	32
33	GND	N/A	34
35	PETN1	N/A	36
37	PETP1	DEVSLP	38
39	GND	N/A	40
41	SATA RX+/PERN0	N/A	42
43	SATA RX-/PERP0	N/A	44
45	GND	N/A	46
47	SATA TX-/PETN0	N/A	48
49	SATA TX+/PETP0	PERST#	50
51	GND	CLKREQ#	52
53	REFCLKN	PEWAKE#/NC	54
55	REFCLKP	MFGDAT	56
57	GND	MFGCLK	58
59	KEY	KEY	60
61	KEY	KEY	62
63	KEY	KEY	64
65	KEY	KEY	66
67	N/A	SUSCLK	68
69	PEDET(NC-PCIE/GND-SATA)		70
71	GND	3.3Vaux	72
73	GND	3.3Vaux	74
75	GND	3.3Vaux	

ngff-apci0020-p002a-75p-km-smt

+3V_SSD
TP4901
C4915 0.01U/50V_4
C4916 0.1U/16V_4
C4913 4.7U/6.3V_6
R4911 *0_8/S +3V

0523 CQ
由25V改成16V

+3V
R8505 10K_4
R4914 *0_4 DEVSLP1 [12]

1005 Add DEVSLP0 PU R8505 10K to +3V

R17741 *0_4/S
R17742 *0_4/S
PCIE_CLKREQ_SSD#_C
PLTRST# [4,16,19,30,31,33,35]
PCIE_CLKREQ_SSD# [13]

R4926 *0_4

+3V_SSD
80mil
EC4903 470P/50V_4
EC4904 10U/6.3V_6
EC4905 10U/6.3V_6

+3V
R4927 100K/F_4 PEDET

0713 CQ
Change F/P S0402

[12] GPIO35
R4930 *0_4/S
R4931 *0_4

Q4901
2N7002K

0706 CQ
改FP ngff-apci0020-p002a-75p-km-smt

Table 36-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

EMI

+5VS5
EC7015 0.1U/16V_4
EC7017 0.1U/16V_4
EC7018 *0.1U/16V_4
EC7019 *0.1U/16V_4

1230 PV

+3VS5
EC7022 *0.1U/16V_4
EC7023 *0.1U/16V_4
EC7020 *0.1U/16V_4
EC7021 *0.1U/16V_4

+3V
EC7024 *0.1U/16V_4
EC7025 *0.1U/16V_4

[2,4,10..13,15..21,25..27,29,30,33,35,41,45,46] +3V

PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
B	NGFF (PCIE/SATA)	1A

Date: Wednesday, July 20, 2016 Sheet 32 of 49

9. Power Sequence

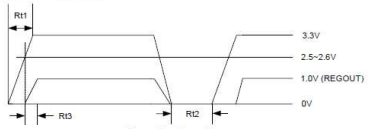


Figure 4. Power Sequence

Table 16. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3,8,22,30
Place Cg & Ch close to each VDD10 pin22

Power trace Layout W > 60mil
Trace<30 mil
Width > 60 mil

~~RTL8111GS (SWR Mode) Pin-24 REGOUT : Switching Regulator 1.0V Output.~~
RTL8111H (LDO Mode) Pin-24 REGOUT : LDO Regulator 1.0V Output.

0713 CQ
Change F/P S0805

~~RTL8111GS stuff Lx,Cy,Cz~~
~~(SWR mode need stuff Cx & Cz)~~

>60mil

Lx : SWR
Rx : LDO
LDO Mode:Stuff Rx
Switch Mode:Stuff Lx

0306 CQ
RTL8111H stuff C1017
(LDO mode)
Unstuff C132 , C133

0301 CQ
Add GCLK XTALIN (LAN_XTAL25_IN) & 0ohm
Change default use X'TAL

0104 change to 300 ohm

1015換料號(check fp)

0713 CQ
Change F/P S0402

0306 CQ
RTL8111H unstuff (or remove)
Cc , Cd for LDO mode

~~RTL8111GS stuff Cc, Cd~~
~~Remove For Not Using SWR mode~~
~~Stuff Ca and Cb only, close to each VDD33 pin--11, 32~~
~~Place Cc and Cd close to each VDD33 pin--23~~

20150316A-
Rich Power recommend to
change power for So state.

if ISOLATEB pin pull-low,the LAN
chip will not drive it's PCI-E outputs
(excluding PCIE_WAKE# pin)

Please add 9 GND VIAs
connection with thermal PAD

0523 CQ
Change U8504 P/N to DB0LL1LAN00 (Reco suggest)
Change Symbol , Change net

Differential Impedance : 100Ω

Differential Impedance : 100Ω

Pin-21 LANWAKEB : O/D, Low Active,
PU via 1KΩ to +3VSG on CPU side.

Pin-12 CLKREQB : O/D, PU via
10KΩ to +3V on CPU side.

LAN CONN
RJ45

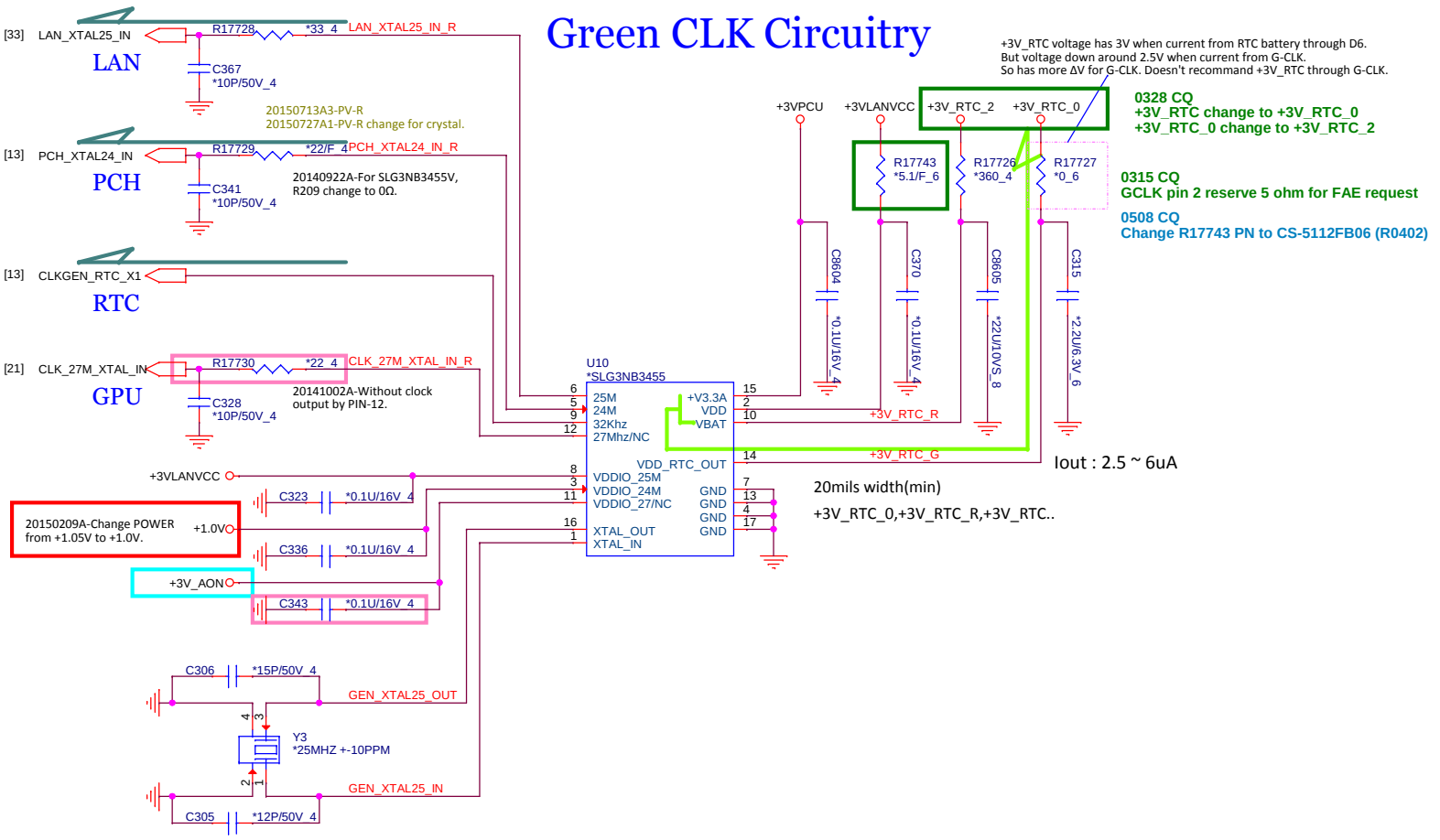
0706 CQ
FP rj45-2rj1754-000211f-8p (keep)
PN DFTJ08FR473 (GF)

RTL8111GS : Switching Regulater
RTL8111G : LDO Regulater

+1.0V_LAN
+1.0V_LAN_REGOUT
+3V [2,4,10..13,15..21,25..27,29,30,32,35,41,45,46]
+3VLANVCC [34,45]

PROJECT : LG9	Quanta Computer Inc.
Size C	Document Number LAN RTL8111H-CG
Rev 1A	
Date: Wednesday, July 20, 2016	Sheet 33 of 49

0226 CQ
Use TWL GCLK circuitry



PROJECT : LG9
Quanta Computer Inc.

Size	Document Number	Rev
B	GCLK-SLG3NB3455	1A

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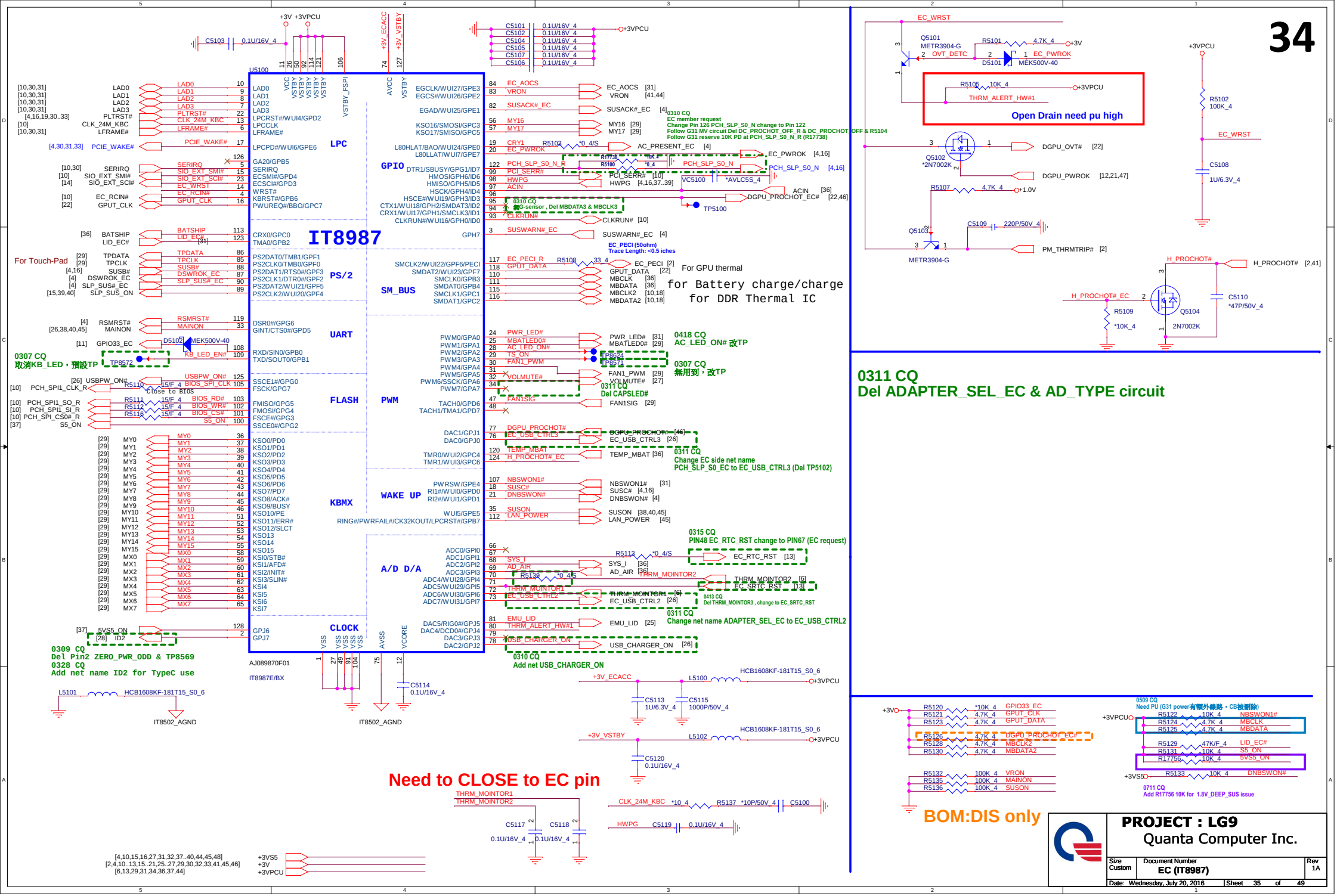


0311 CQ
Del ADAPTER_SEL_EC & AD_TYPE circuit

BOM:DIS only

PROJECT : LG9 Quanta Computer Inc.		
Size: Custom	Document Number: EC (IT8987)	Rev: 1A
Date: Wednesday, July 20, 2016	Sheet 35 of 49	

+3VPCU [6,13,29,31,34,35,37,44]
+5VPCU [37,45,48]
+BAT_RTC [13,31]
+VIN [25,37..39,41..44,46,47,49]

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN

SI stage

15"

PV stage

SI: For battery in detect

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

Vacdet=2.4V

Notes:
For 4S pack
Stuff Block A + Ra
Ra = 69.8K (P/N:CS36982FB11)

MIN. BATV=7.2V

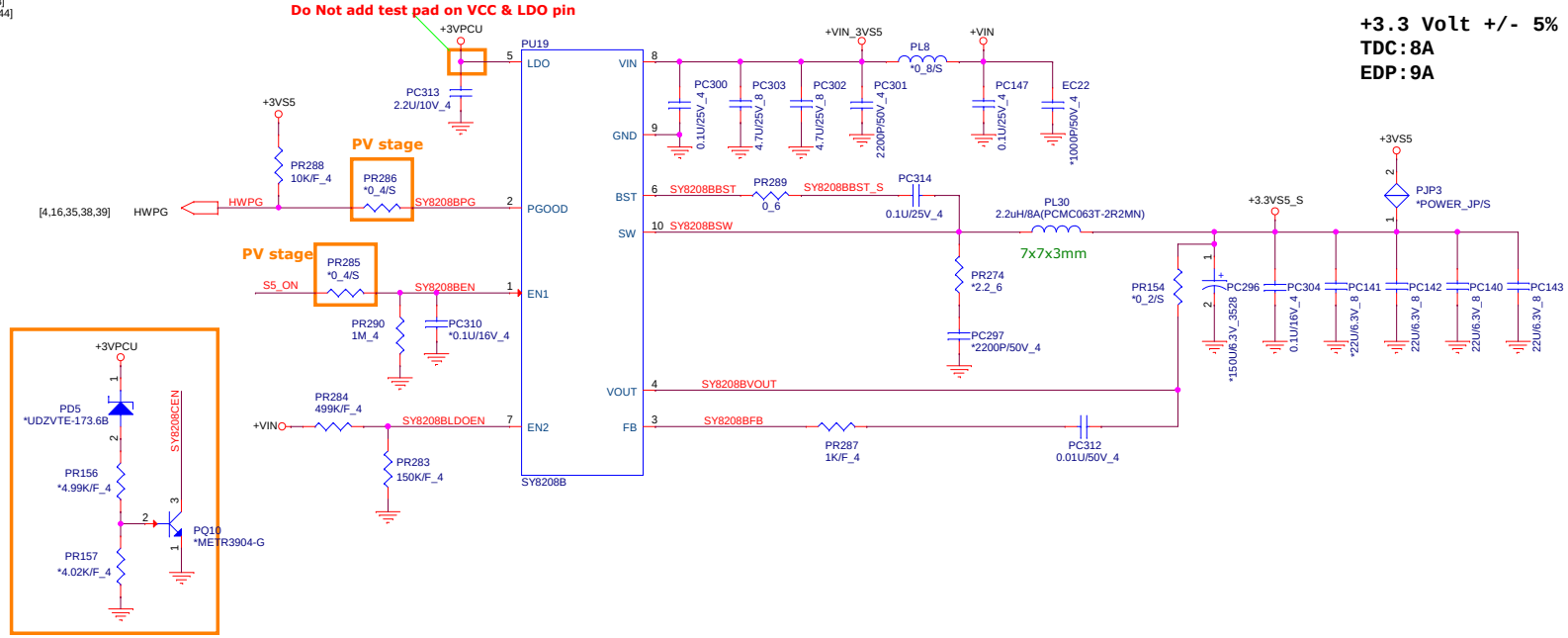
Place this R&C close to EC

Place this cap close to EC

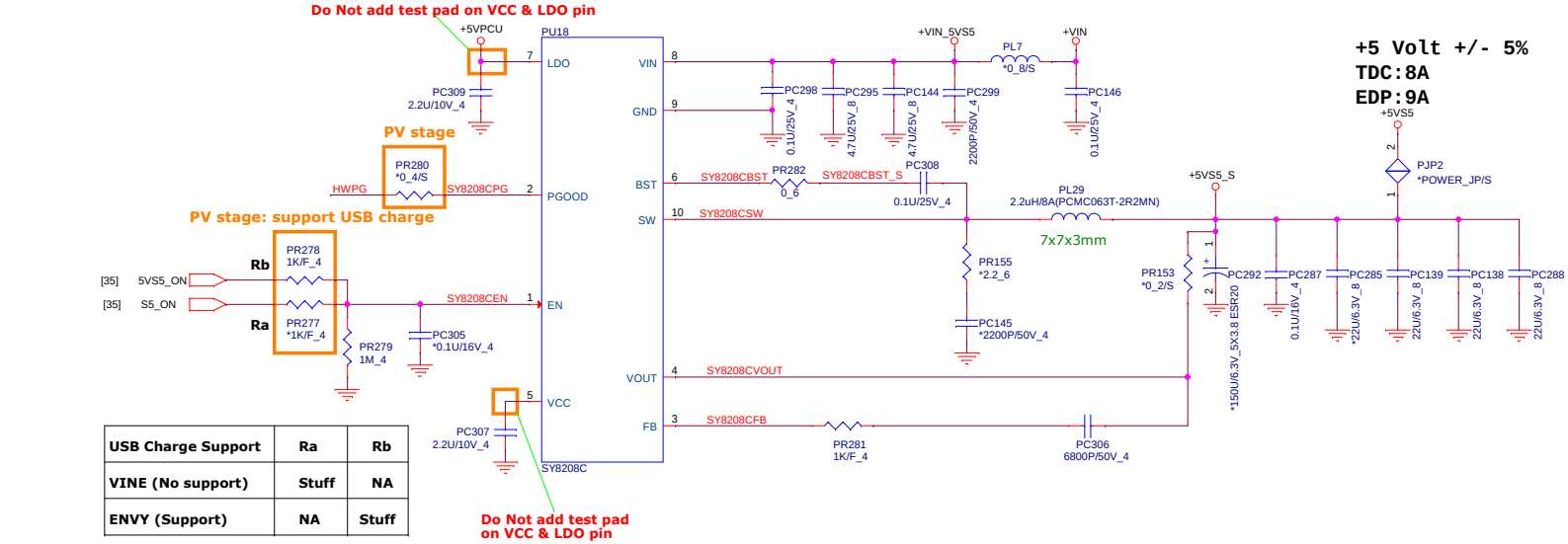
NB5	**PROJECT : X1Q** Quanta Computer Inc.	
	Size: Custom	Document Number: Charger(BQ24738H) Rev: 1A
	Date: Wednesday, July 20, 2016	Sheet 36 of 49

DC/DC +3VS5/+5VS5

+VIN [25,36,38,39,41..44,46,47,49]
+3VS5 [4,10,15,16,27,31,32,35,38..40,44,45,48]
+5VS5 [4,26,32,38..43,45..48]
+3VPCU [6,13,29,31,34..36,44]
+5VPCU [45,48]



+3.3 Volt +/- 5%
TDC:8A
EDP:9A



+5 Volt +/- 5%
TDC:8A
EDP:9A

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

PROJECT : X1Q
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A

Date: Wednesday, July 20, 2016 Sheet 37 of 49

+VIN [25,36,37,39,41..44,46,47,49]
+5VS5 [4,26,32,37,39..43,45..48]
+1.2VSUS [3,6,17,18,40,48]
DDR_VTT [17,18]

PV stage
PV:For 2.5VSUS sequence
PR303 *0_4/S
PR308 75K/F_4
PD27 MEK500V-40
PC333 0.1U/16V_4
PR309 *0_4
PR305 *0_4/S
PC334 *0.1U/16V_4
PR299 243K/F_4
PR304 499K/F_4
PR298 2.2_6
PC327 0.1U/25V_4
PR301 100/F_4
(3mA)
PC329 10U/6.3V_6
PC332 0.1U/16V_4
PC330 0.033U/25V_4
PC328 *10U/6.3V_6
PR300 *0_2/S
PR302 *0_2/S
PR306 10K/F_4
PR307 7.87K/F_4
PU21 G5619RZ1U
PQ49 EMB20N03V
PQ48 AON7752
PR166 *2.2_6
PC171 *2200P/50V_4
PC326 0.1U/25V_4
PC324 4.7U/25V_8
PC176 4.7U/25V_8
PC325 2200P/50V_4
PC173 0.1U/25V_4
PL9 *0_8/S
PL32 1uH/11A(PCMC063T-1R0MN)
7x7x3mm
PR297 *0_2/S
PC323 0.1U/16V_4
PC319 22U/6.3V_8
PC321 22U/6.3V_8
PC320 *22U/6.3V_8
PC322 *22U/6.3V_8
PJP4 *POWER_JP/S
Rds(on) 14m ohm

+1.2VSUS +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

+2.5VSUS +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

PU23 YB1282PSP
PR3163 *0_4/S
PC5370 10U/6.3V_6
PC5369 0.1U/16V_4
PC5371 *0.1U/16V_4
PC5368 1U/6.3V_4
PC5367 *10U/6.3V_6
PC5372 0.1U/16V_4
R1 PR3161 215K/F_4
R2 PR3162 100K/F_4
PR3164 *0_4/S
VO=(0.8(R1+R2)/R2)
R2<120Kohm

NB5	PROJECT : X1Q Quanta Computer Inc.	
Size	Document Number: DDR3 (RT8231B)/1.8VS5	Rev: 1A
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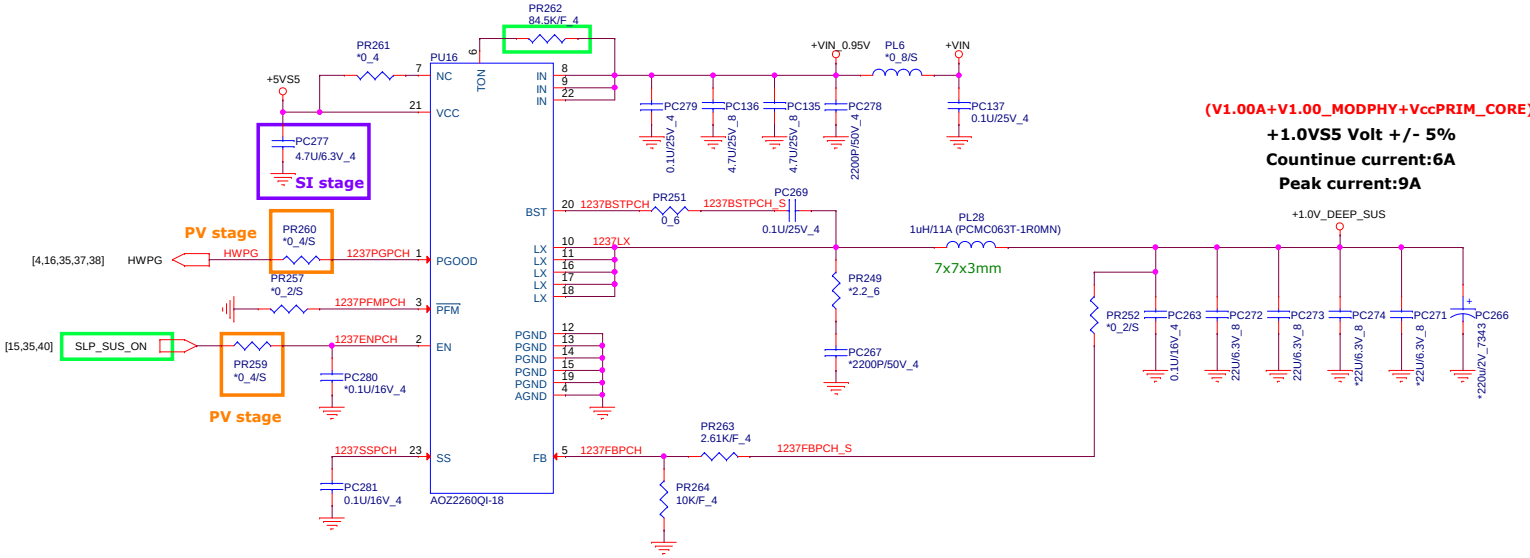
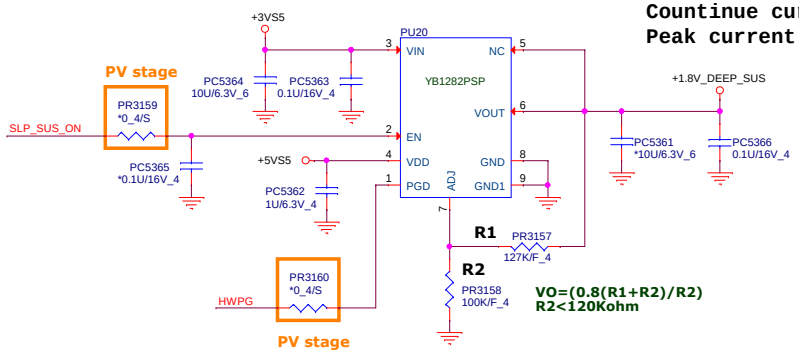
+VIN [25,36..38,41..44,46,47,49]
+3VS5 [4,10,15,16,27,31,32,35,37,38,40,44,45,48]
+5VS5 [4,26,32,37,38,40..43,45..48]
+1.0V_DEEP_SUS [9,15,16,40]
+1.8V_DEEP_SUS [5,9,15]



(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Countinue current:6A
Peak current:9A



+1.8V_DEEP_SUS +/- 5%
Countinue current:1.0A
Peak current:3A

VO=(0.8(R1+R2)/R2)
R2<120Kohm

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A

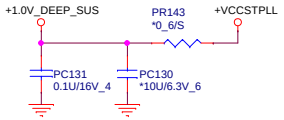
Date: Wednesday, July 20, 2016 Sheet 39 of 49

+1.0V [2,4,6,16,34,35]
+3VS5 [4,10,15,16,27,31,32,35,37..39,44,45,48]
+5VS5 [4,26,32,37..39,41..43,45..48]
+VCCIO [6,16]
+1.2VSUS [3,6,17,18,38,48]
+VCCSTPLL [2,4..6,9,13,41]
+1.0V_DEEP_SUS [9,15,16,39]
+1.2V_VCCPLL_OC [6]
MAINON [26,35,38,40,45]

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

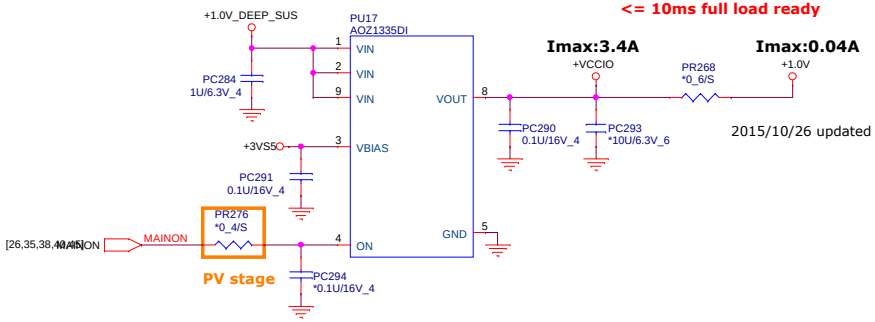
Imax:0.24A



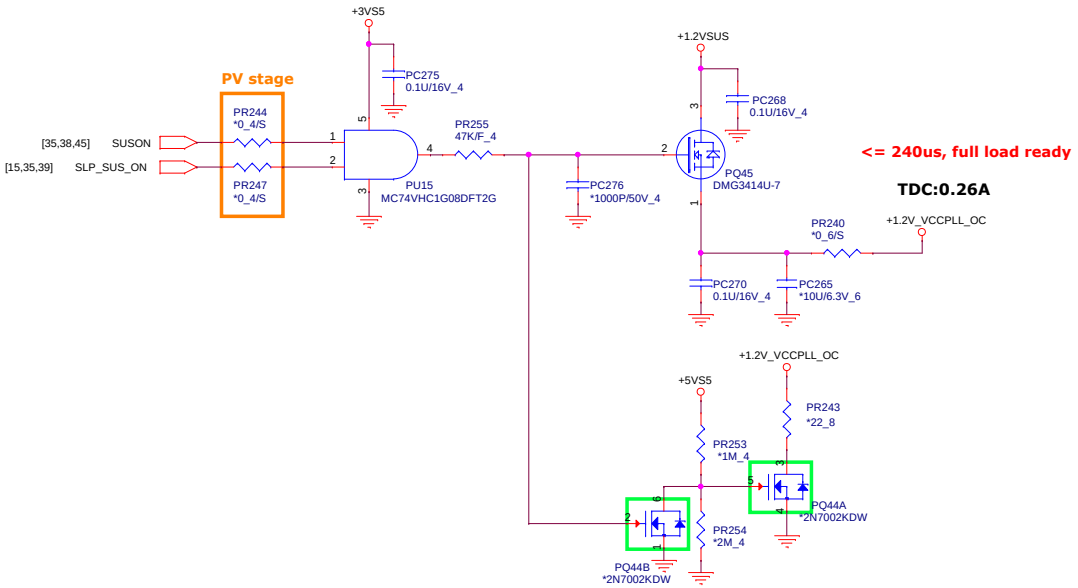
Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**



2015/10/26 updated



<= 240us, full load ready

TDC:0.26A

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
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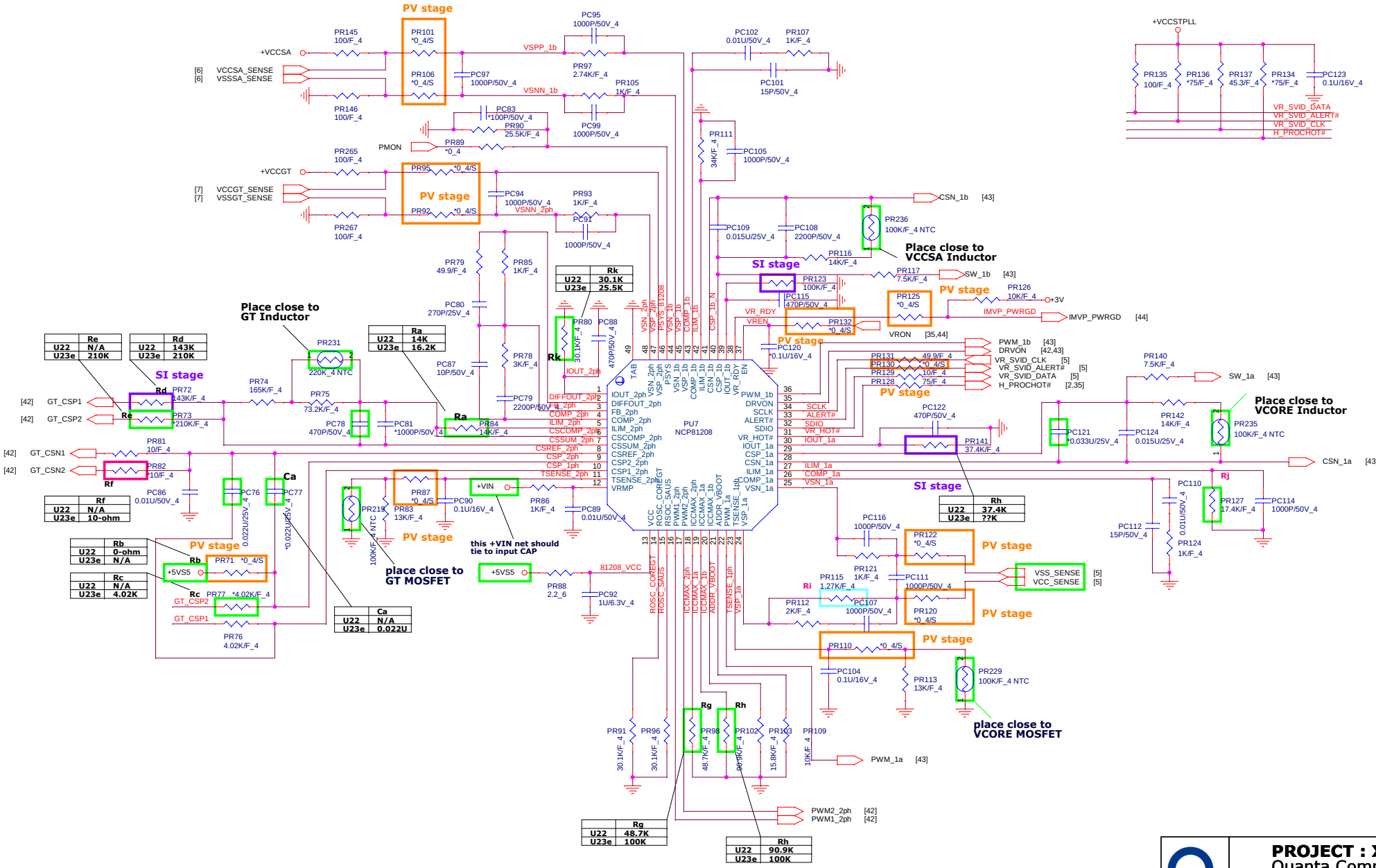
+3V [2,4,10..13,15..21,25..27,29,30,32,33,35,45,46]
+5V [26,27,29,45]
+VIN [25,36..39,42..44,46,47,49]
+5VPCU [37,45,48]
+VCCSA [6,43]
+VCCGT [7,42]
+VCCSTPLL [2,4..6,9,13,40]



Re	
U22	N/A
U23e	210K

Rd	
U22	143K
U23e	210K

Ra	
U22	14K
U23e	16.2K

Rk	
U22	30.1K
U23e	25.5K

Rf	
U22	N/A
U23e	10-ohm

Rb	
U22	0-ohm
U23e	N/A

Rc	
U22	N/A
U23e	4.02K

Ca	
U22	N/A
U23e	0.022U

Rh	
U22	37.4K
U23e	??K

Rg	
U22	48.7K
U23e	100K

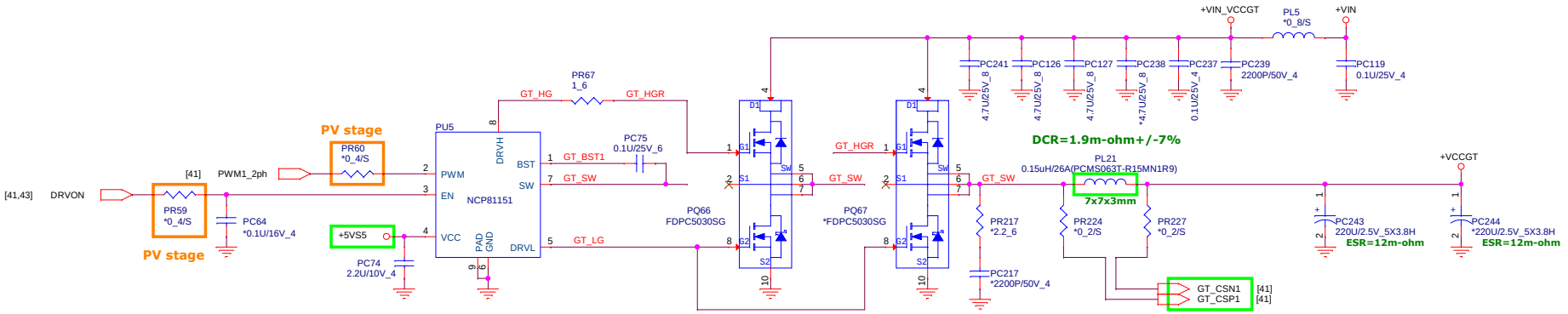
Rh	
U22	90.9K
U23e	100K

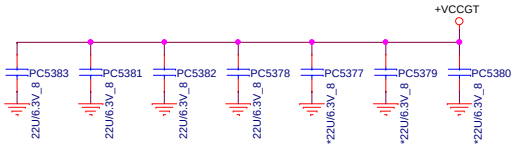
PROJECT : X1Q
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	CPU VR IC (NCP81206)	2A
Date: Wednesday, July 20, 2016	Sheet 41 of 49	

+5V [26,27,29,45]
+VIN [25,36..39,41,43,44,46,47,49]
+5VPCU [37,45,48]
+VCCGT [7,41]





H/W side output CAP list

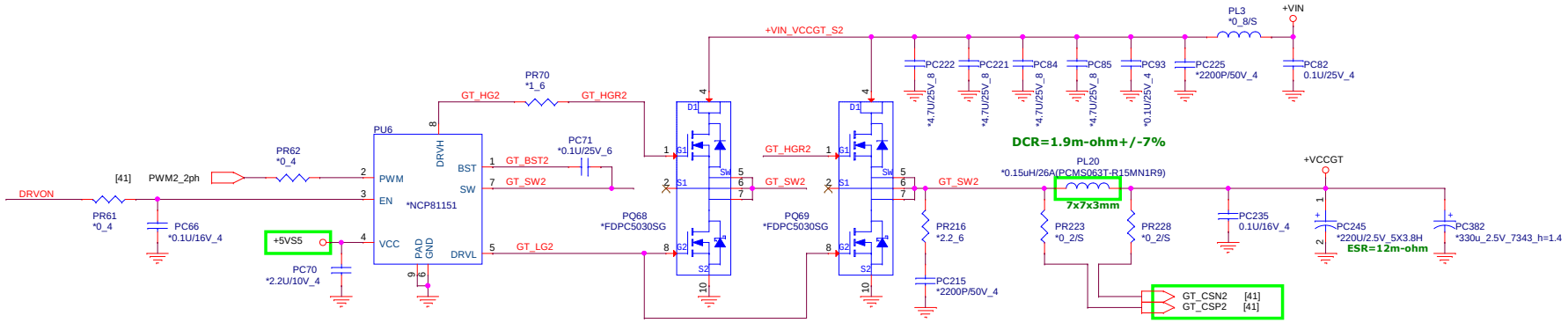
47U/6.3V_0805 X 6
22U/6.3V_0603 X 12 (GTX+5)
10U/6.3V_0402 X 10
1U/6.3V_0402 X 12

+VCC_GT

U-line 22 (15W)
TDC:18A(22)
Icc max:31A(22)
L/L=3.1mV/A

U-line 23e(28W)
TDC:35A(23e)
Icc max =64A(GT+GTx)
L/L=2mV/A

For U23e --> Add These Components



NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A
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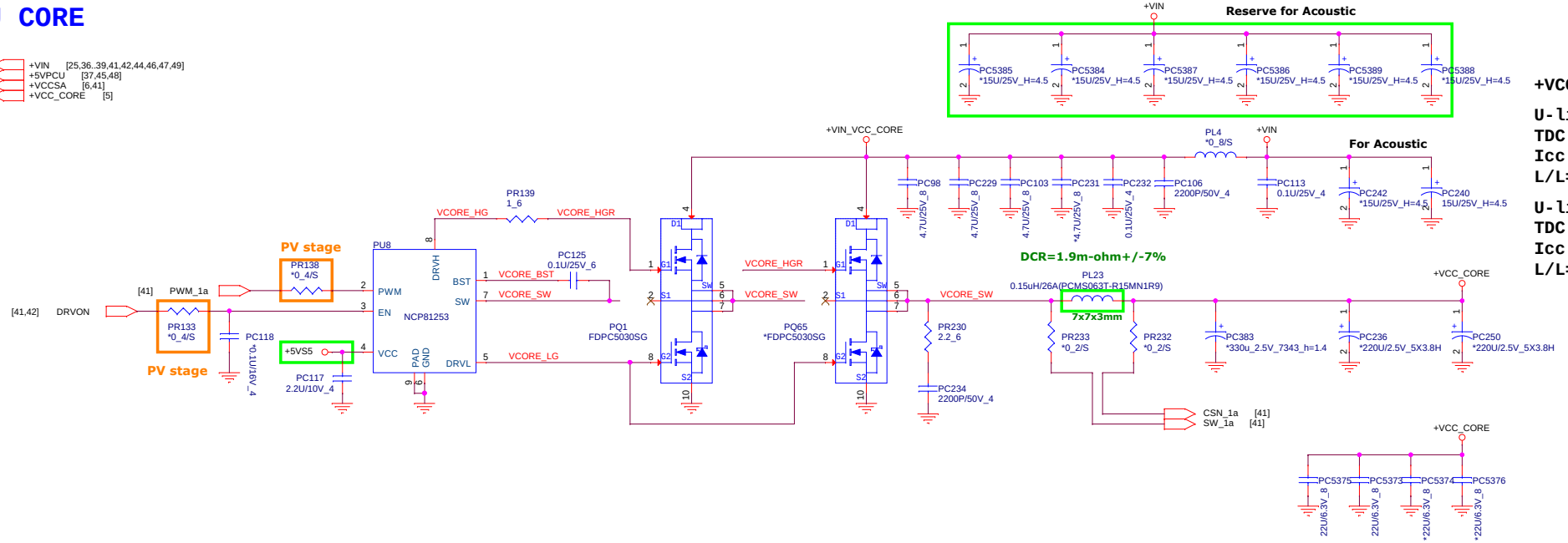
CPU CORE

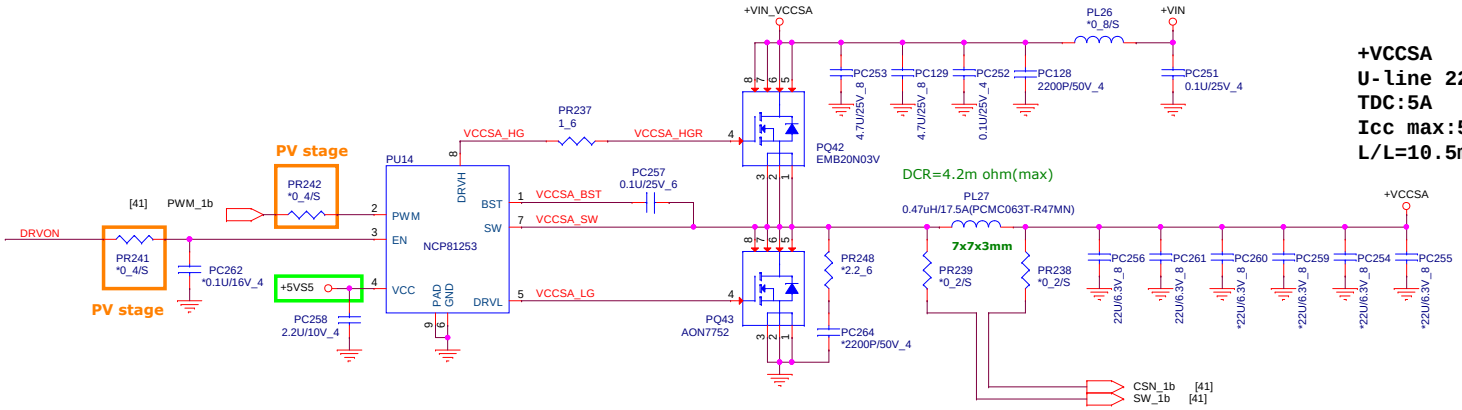
+VIN [25,36..39,41,42,44,46,47,49]
+5VPCU [37,45,48]
+VCCSA [6,41]
+VCC_CORE [5]



+VCC_CORE
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

U-line 23e(28W)
TDC:23A
Icc max:32A
L/L=2.4mV/A

VCCSA



+VCCSA
U-line 22&23e
TDC:5A
Icc max:5A
L/L=10.5mV/A

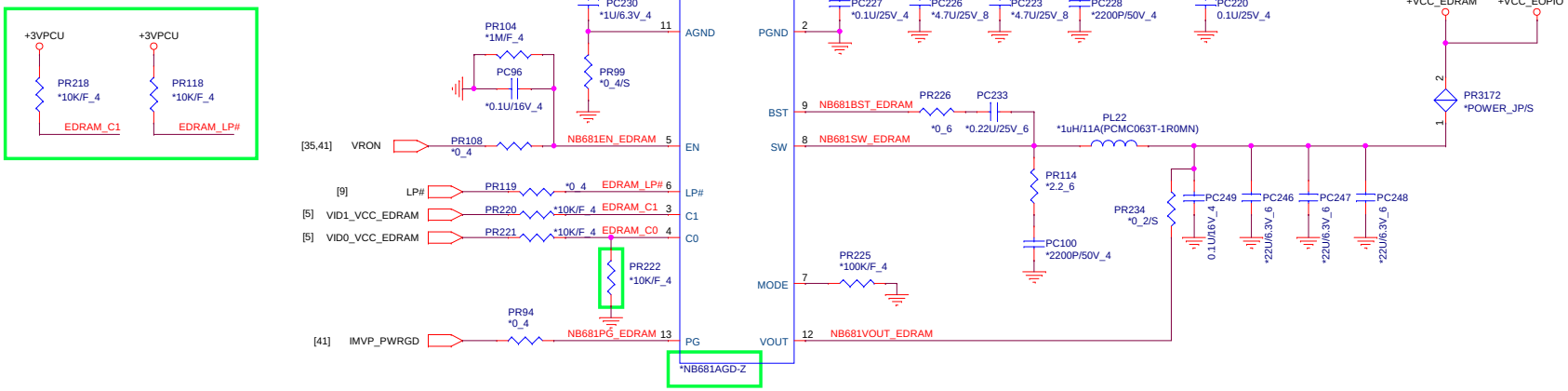
NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCORE/VCCSA (NCP81253)	
Date: Wednesday, July 20, 2016	Sheet 43 of 49	

+VIN [25,36..39,41..43,46,47,49]
+3VPCU [6,13,29,31,34..37]
+VCC_EOPIO [5]
+VCC_EDRAM [5]
+3VS5 [4,10,15,16,27,31,32,35,37..40,45,48]

+VCC_EDRAM +/- 5%
Countinue current:4.5A
Peak current:6A



VCC_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

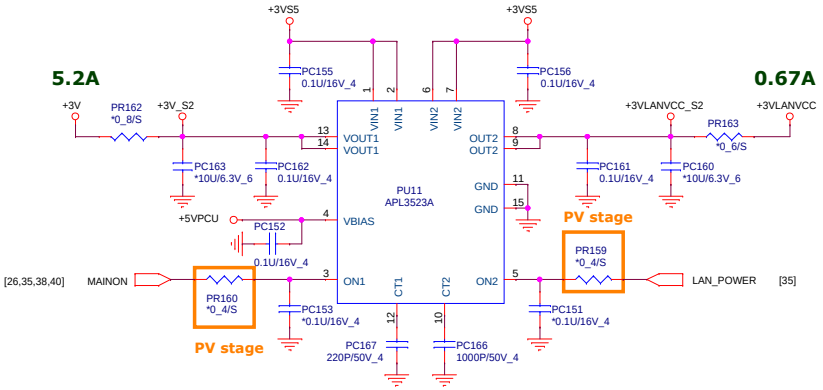
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

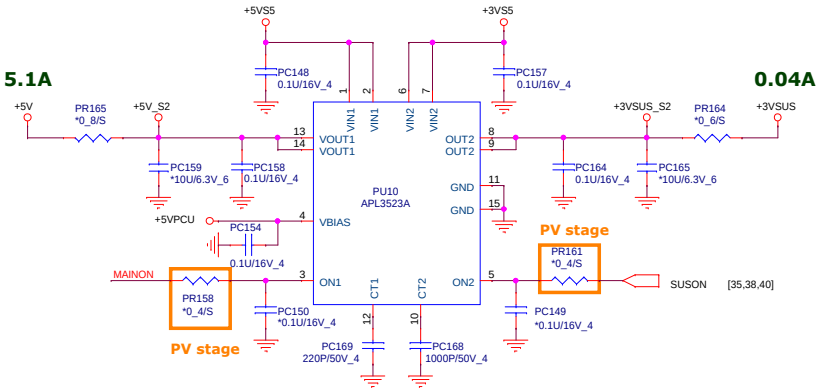
NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCC_EDRAM (NB681)_23E	
Date: Wednesday, July 20, 2016	Sheet 44 of 49	

+3V [2,4,10..13,15..21,25..27,29,30,32,33,35,41,46]
+5V [26,27,29]
+VIN [25,36..39,41..44,46,47,49]
+3VS5 [4,10,15,16,27,31,32,35,37..40,44,48]
+5VS5 [4,26,32,37..43,46..48]
+3VSUS [29]
+5VPCU [37,48]
+3VLANVCC [33,34]





NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A
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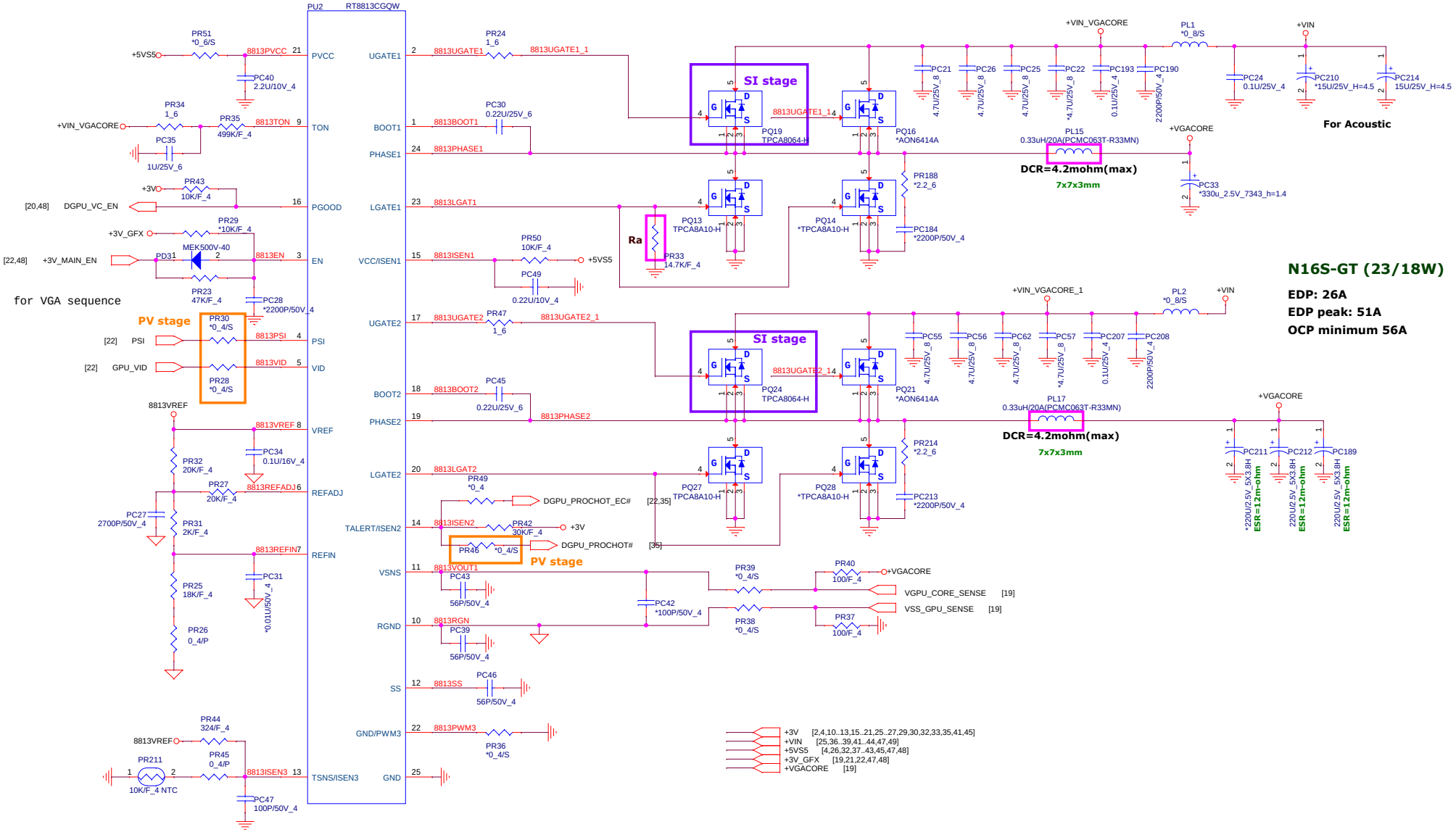
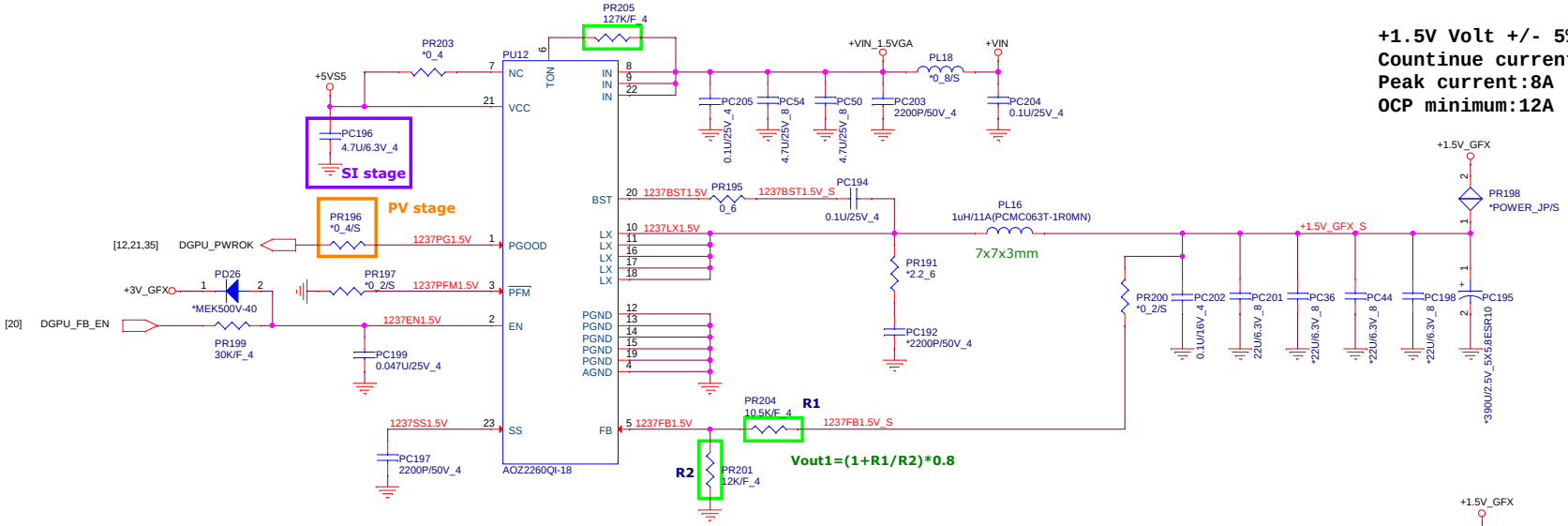
VGA Core

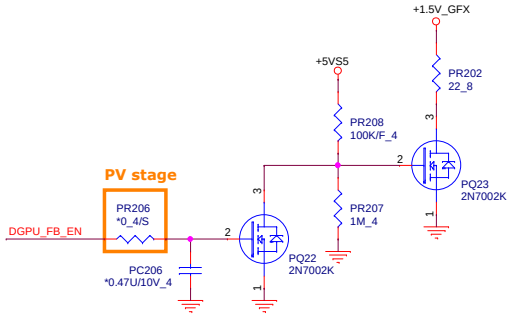


NB5	PROJECT : X1Q Quanta Computer Inc.		
	Size: Custom	Document Number: +VGACORE (RT8813A)	Rev: 2A
	Date: Wednesday, July 20, 2016	Sheet 46 of 49	

+VIN [25,36..39,41..44,46,49]
+5VS5 [4,26,32,37..43,45,46,48]
+1.5V_GFX [20,23,24]

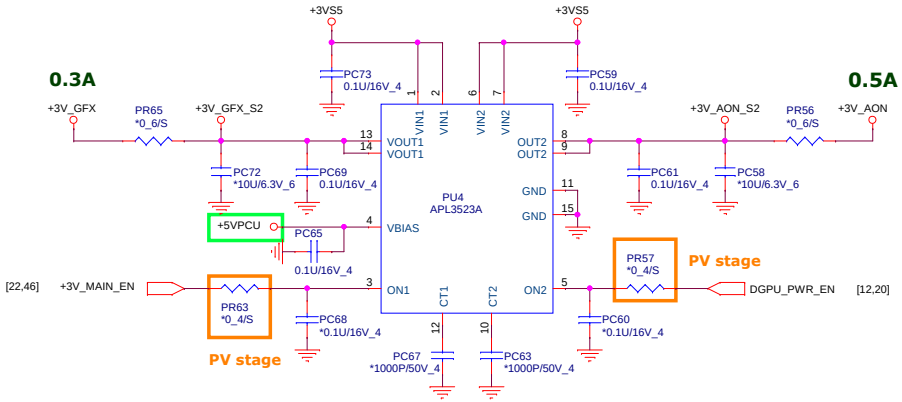
+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

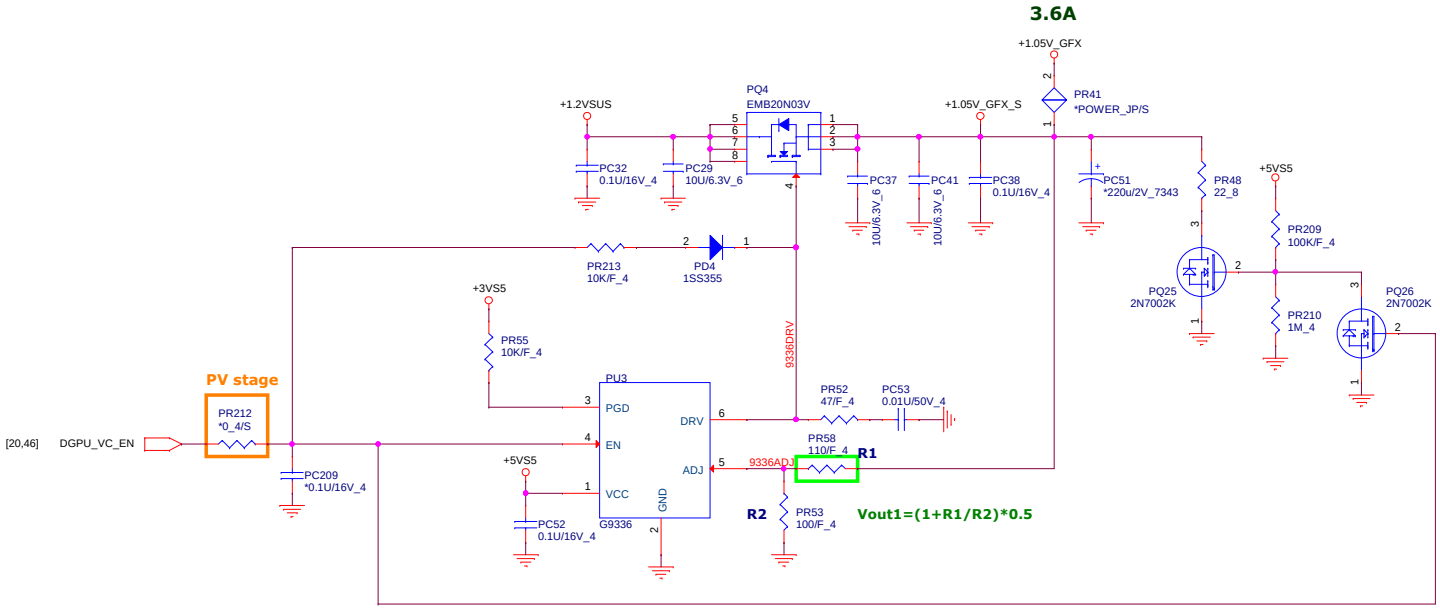




NB5	**PROJECT : X1Q** Quanta Computer Inc.	
Size: Custom	Document Number: +1.35V_VGA(AOZ1237)	Rev: 1A
Date: Wednesday, July 20, 2016	Sheet 47 of 49	

+VIN [25,36..39,41..44,46,47,49]
+3VS5 [4,10,15,16,27,31,32,35,37..40,44,45]
+5VS5 [4,26,32,37..43,45..47]
+3V_GFX [19,21,22,46,47]
+3V_AON [19,22,34]
+1.2VSUS [3,6,17,18,38,40]
+1.05V_GFX [19..21]





NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V_VGA/3V_VGA	1A
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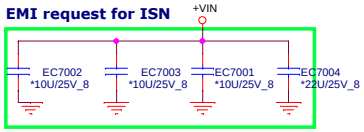
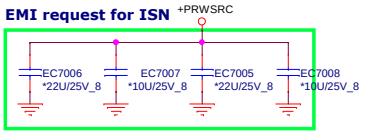
EMI request for ISN



EMI request for ISN



NB5

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Size	Document Number	Rev
Custom	EMI solution	1A
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