MS-7C35 Ver:21

CPU:
AMD AM4

System Chipset:
Prenium X570
(Performance gaming)

Main Memory:
DDR IV * 4S   MAX:64 GB

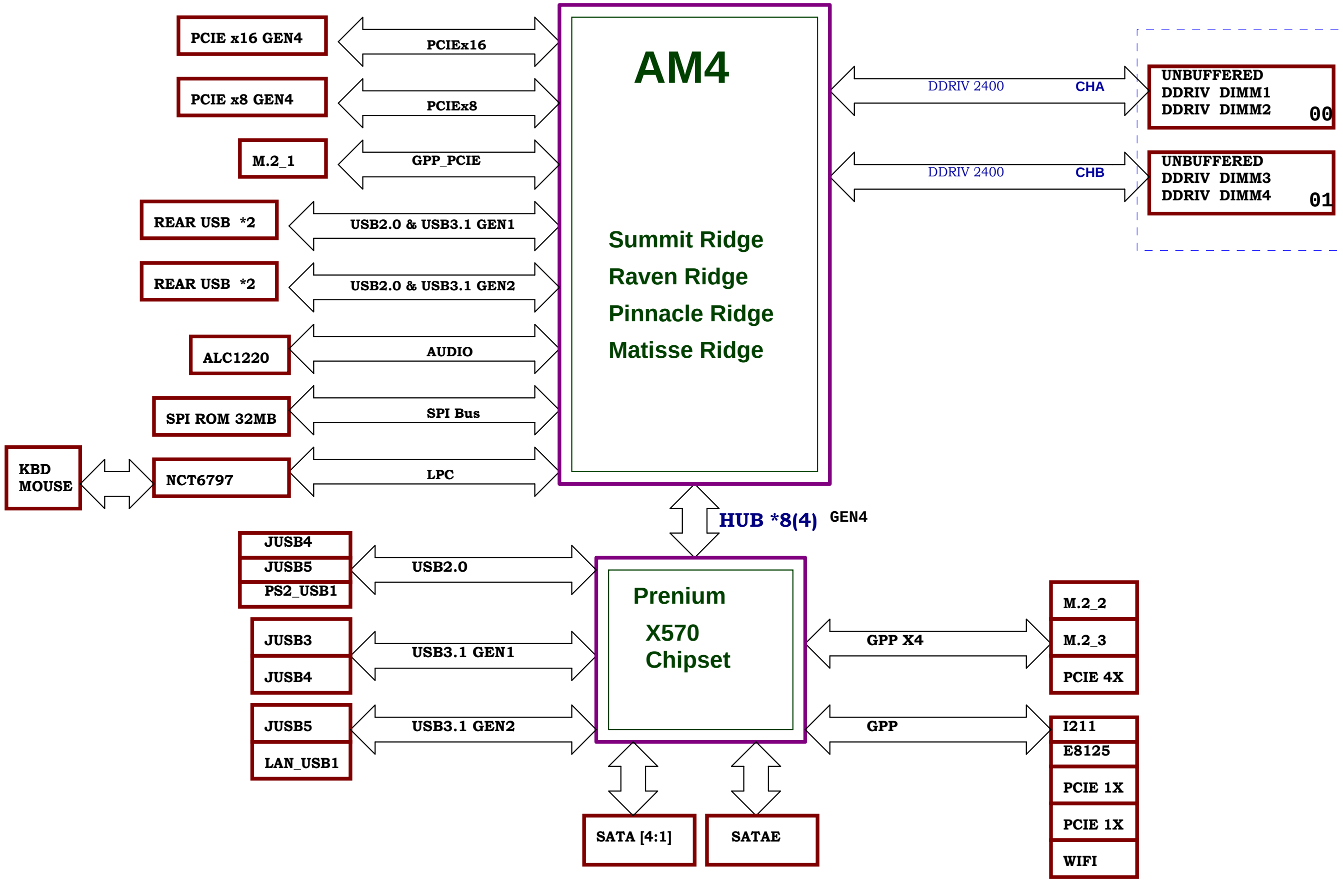
VRM
IR35201 12+2 O

On Board Chipset:
LPC Super I/O --NCT6797D
LAN I211
LAN 8125
Azalia CODEC - Realtek ALC1220

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X8 Slot * 1
From FCH
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X4 Slot * 1

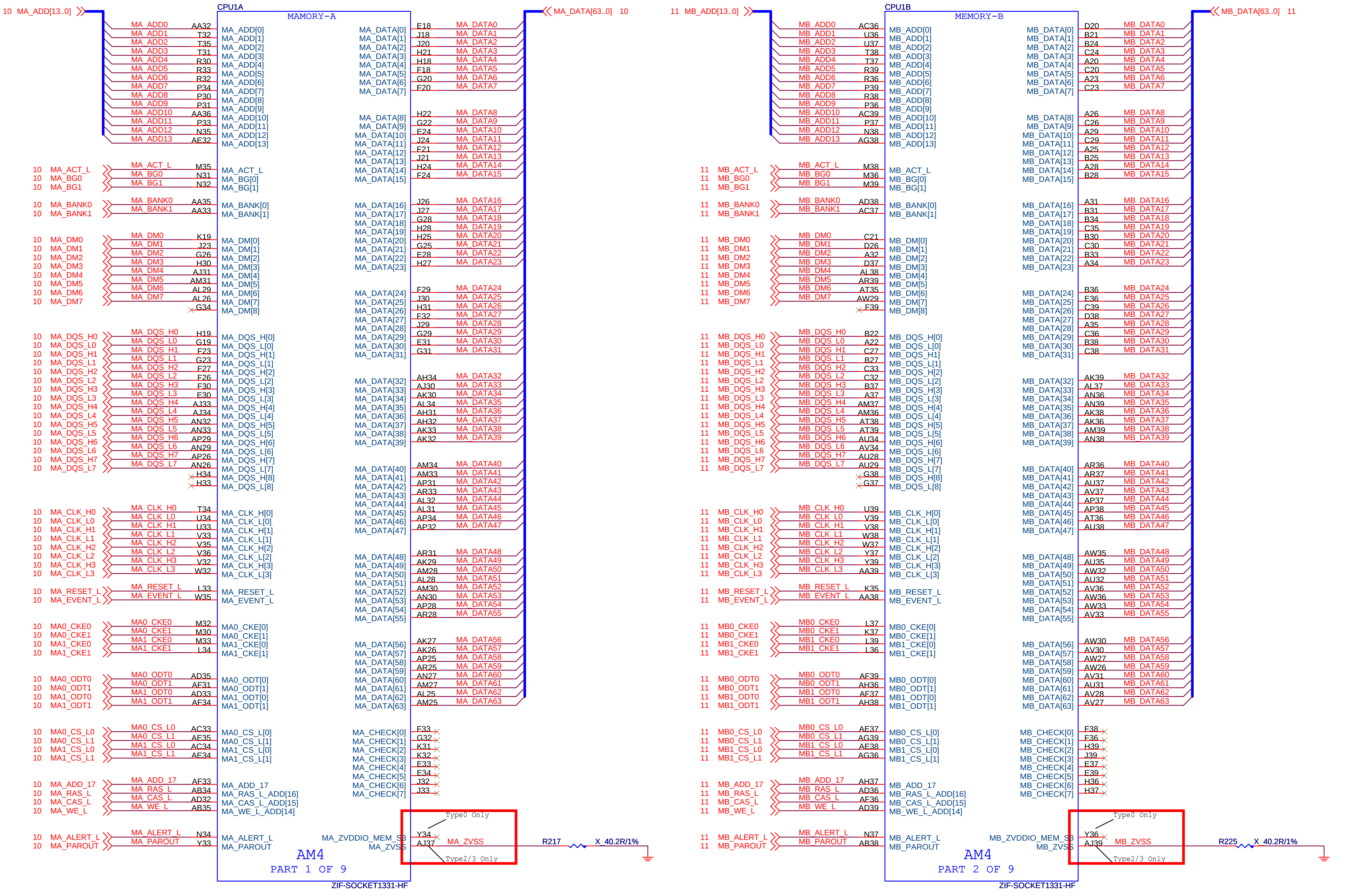
OCP IC:
RT9553

BLOCK DIAGRAM

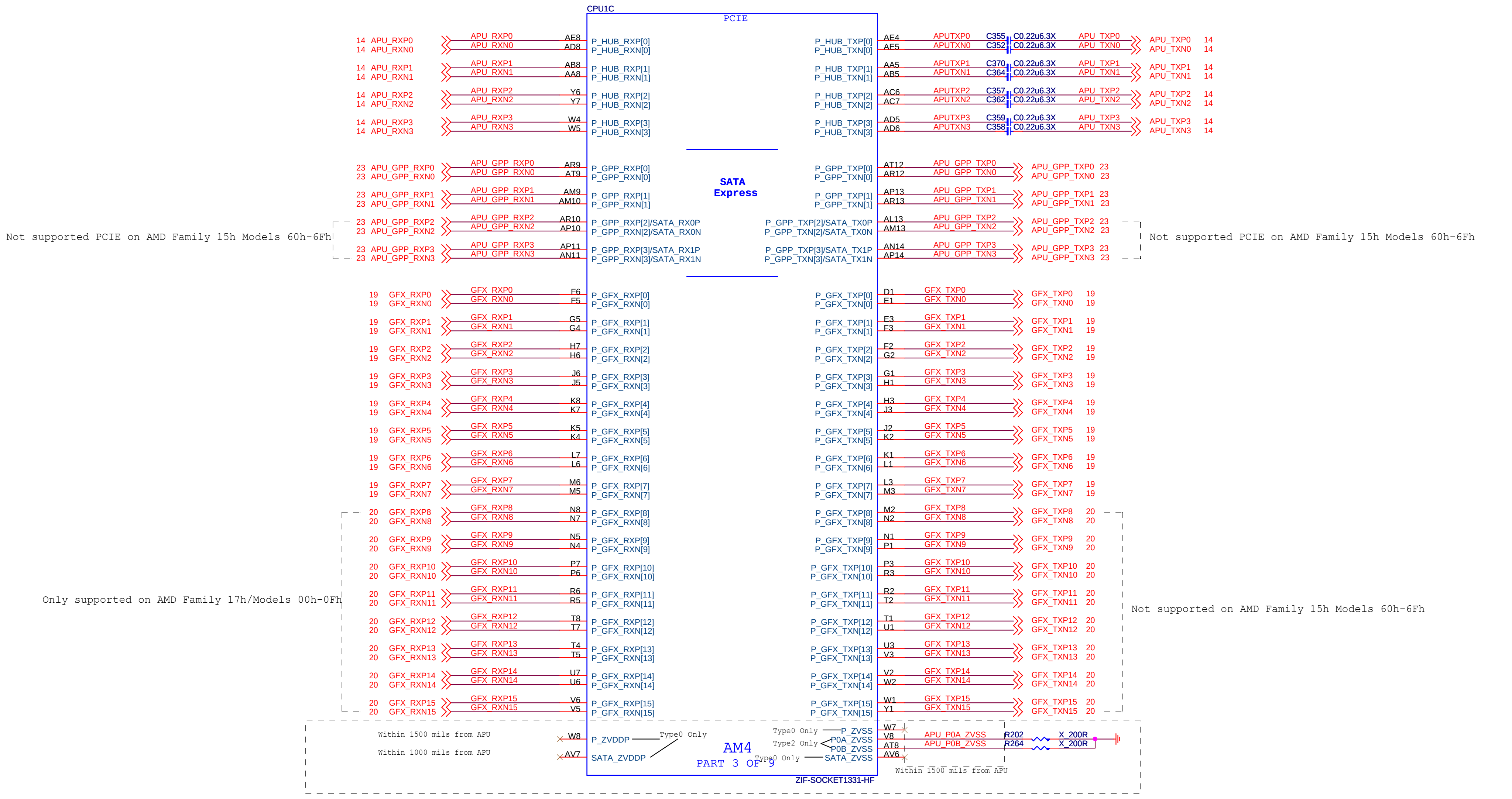


MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: Block Diagram	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 1 of 75	

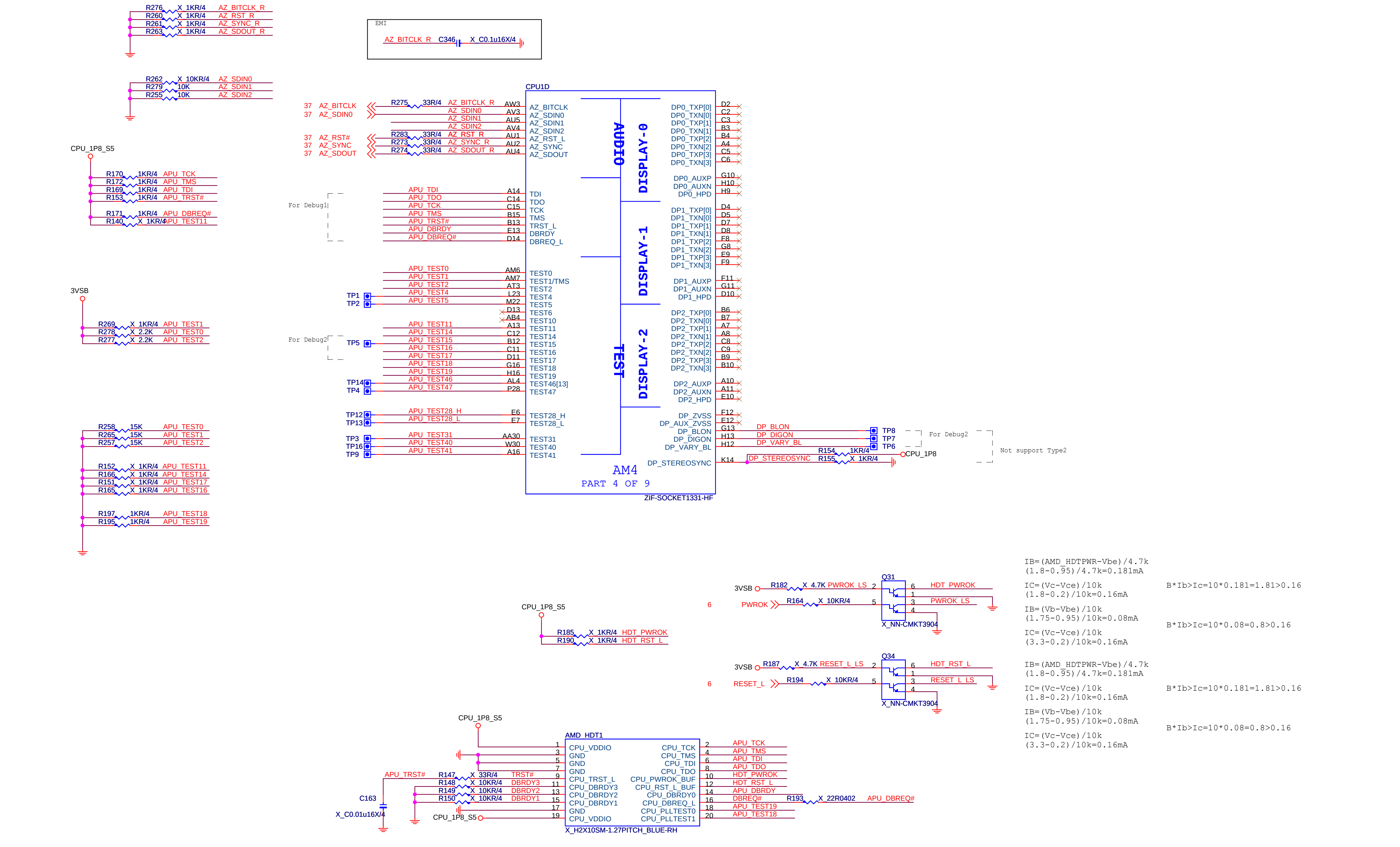
AMD AM4



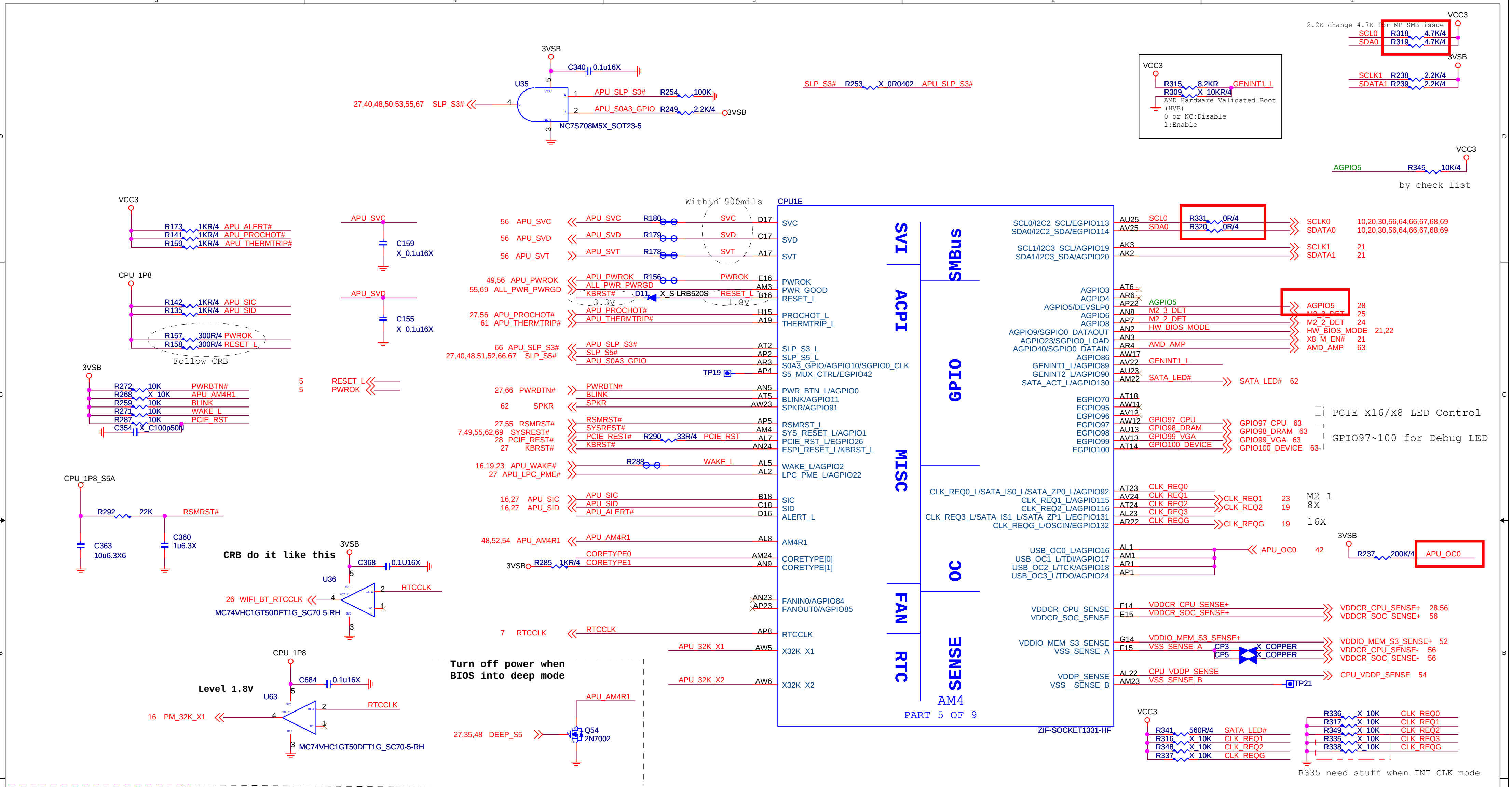
MICRO-STAR INT'L CO.,LTD	
MS-7C35	
Size: Custom	Document Description: AM4 DDR4 I/F — Rev 21
Date: Tuesday, August 13, 2019	Sheet 3 of 75



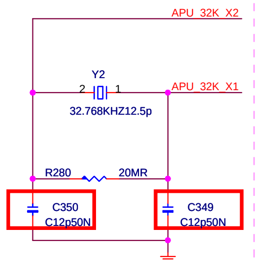
MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: AM4 PCIE/SATAE	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 4 of 75	



MICRO-STAR INT'L CO.,LTD			
MS-7C35			
Size: Custom	Document Description: AM4 Display/Audio		Rev: 21
Date: Tuesday, August 13, 2019	Sheet 5 of 75		



Layout:Place x'tal within 1.5 inch of APU

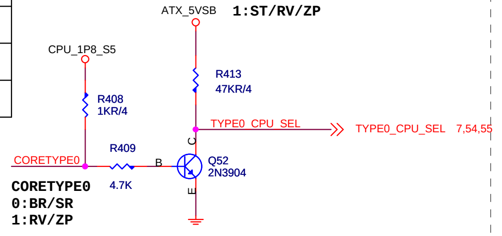


PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

AM4 CPU TYPE Circuit

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP



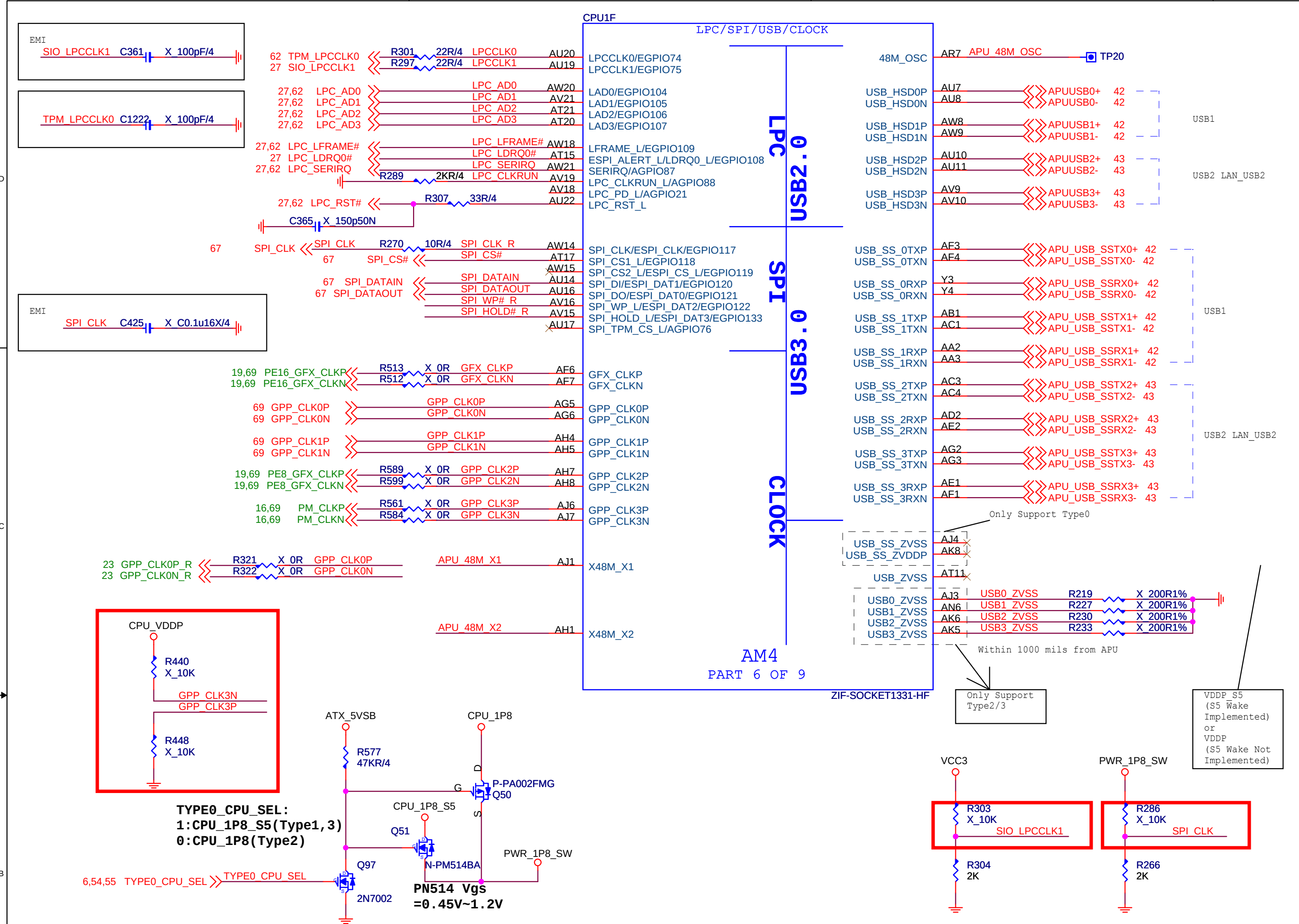
CORETYPE0
0:BR/SR
1:RV/ZP

MICRO-STAR INT'L CO.,LTD

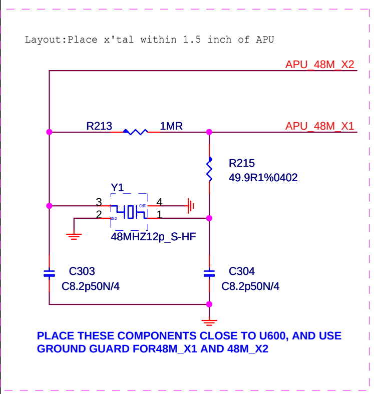
MS-7C35

Size	Document Description	Rev
Custom	AM4 SVI/ACPI/GPIO	21

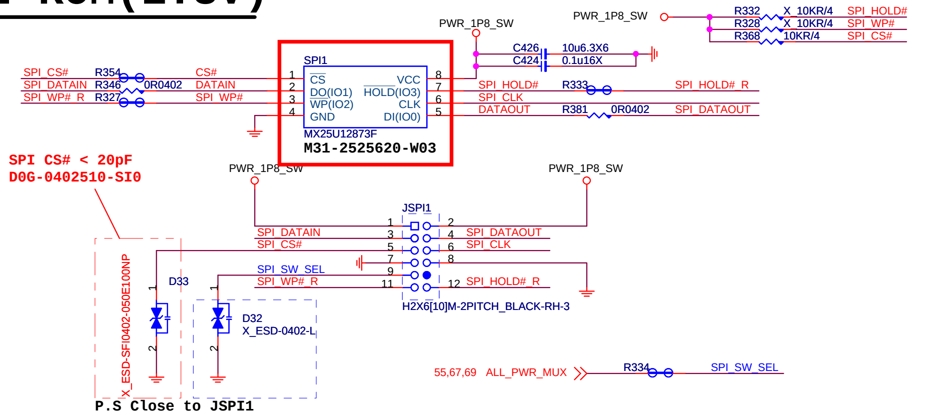
Date: Tuesday, August 13, 2019 Sheet 6 of 75



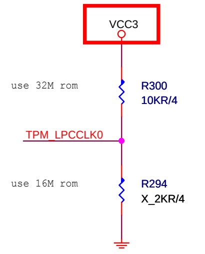
Strap pin for INT EXT select



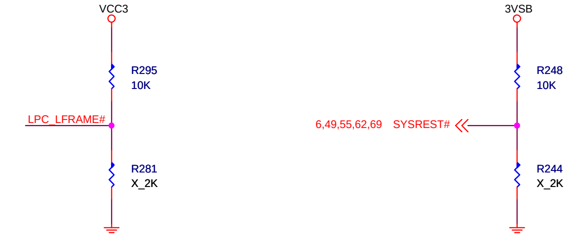
SPI ROM(1.8V)



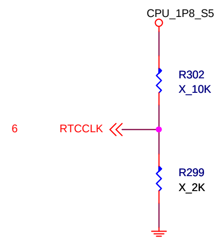
Strapping Options



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



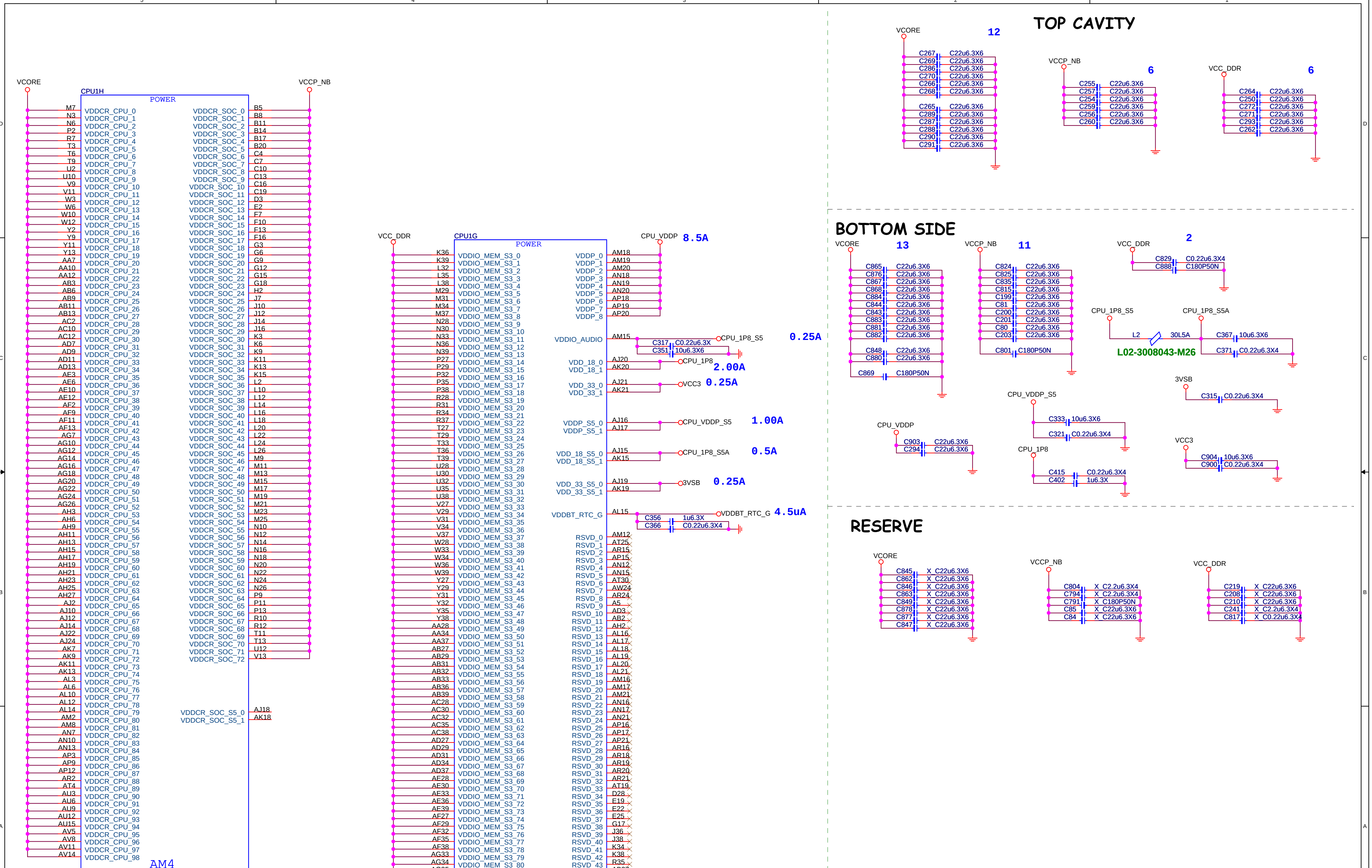
	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size: Custom | Document Description: AM4 LPC/SPI/USB/CLK/STRAP | Rev: 21

Date: Tuesday, August 13, 2019 | Sheet 7 of 75

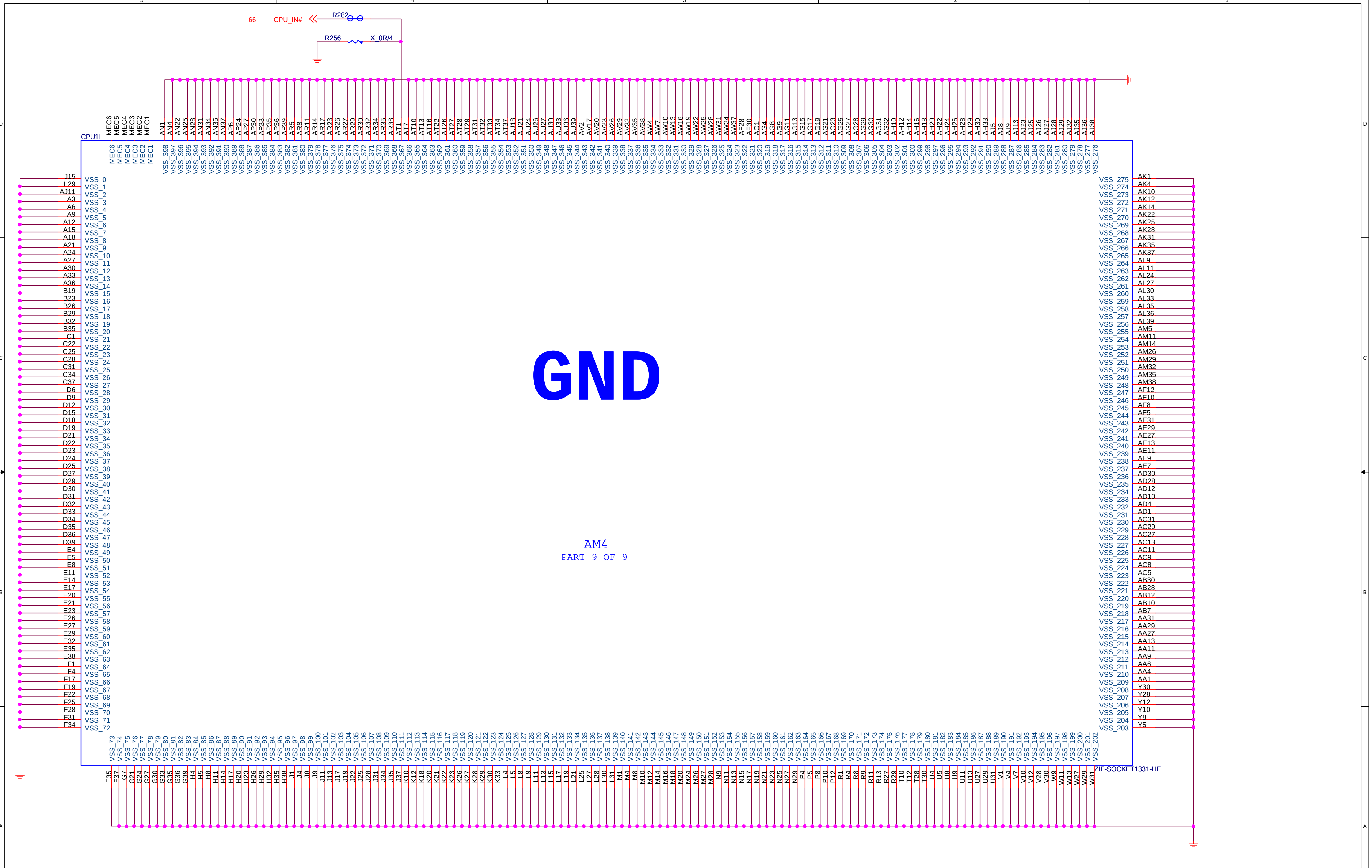


MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	AM4 Power/RTC Power	21

Date: Tuesday, August 13, 2019 Sheet 8 of 75

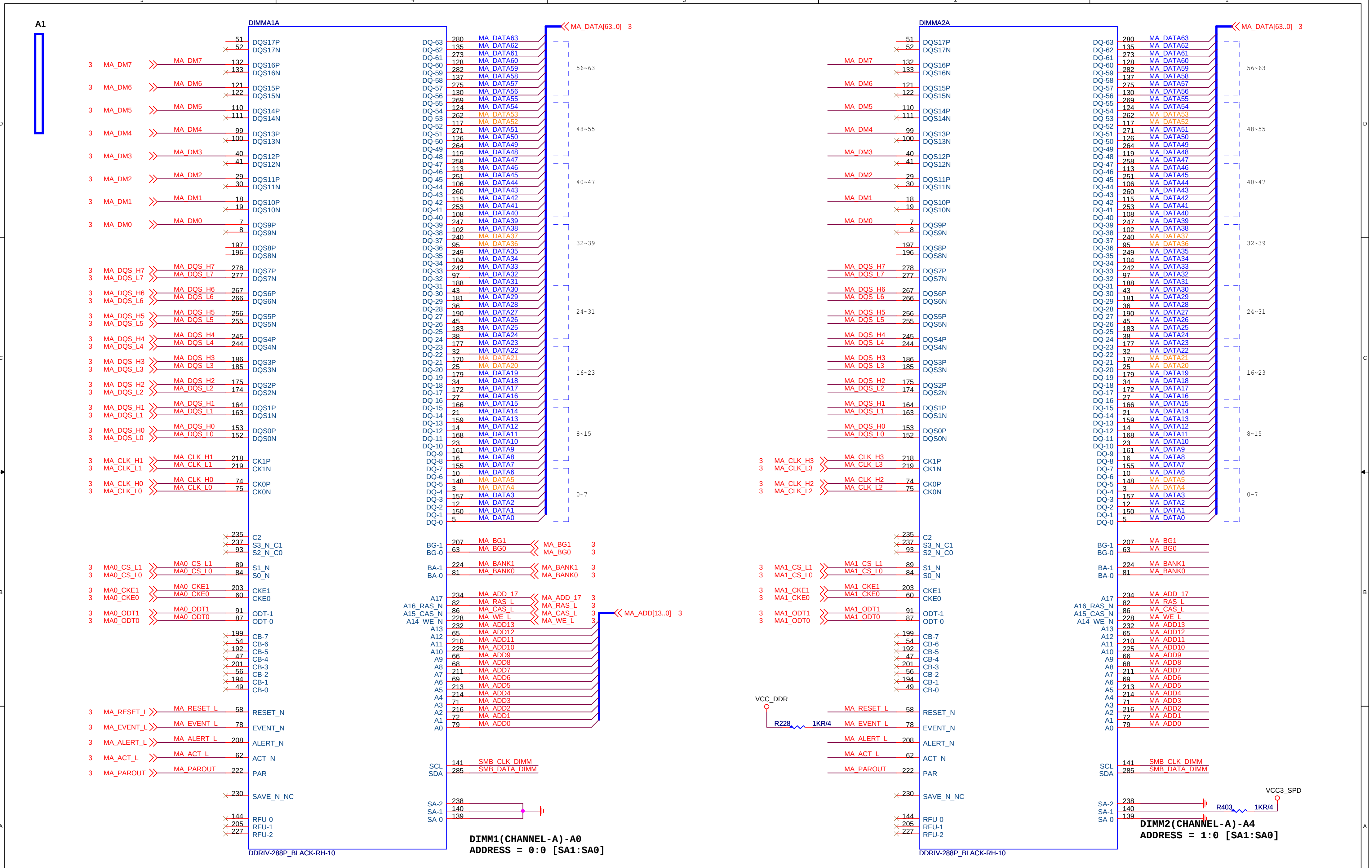


MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	AM4 GND	21

Date: Tuesday, August 13, 2019 Sheet 9 of 75

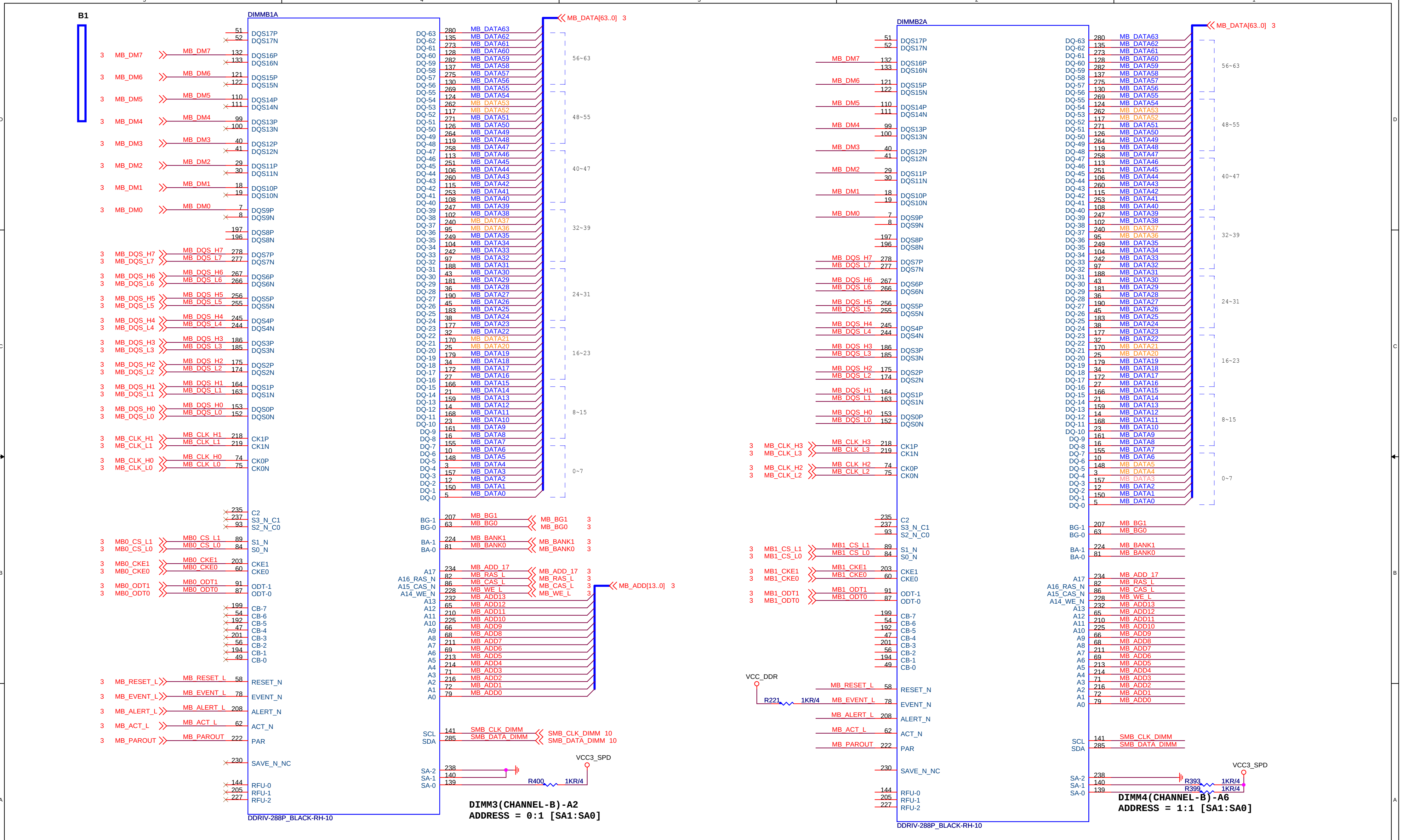


MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	DDR4-DIMM CH-A	21

Date: Tuesday, August 13, 2019 Sheet 10 of 75



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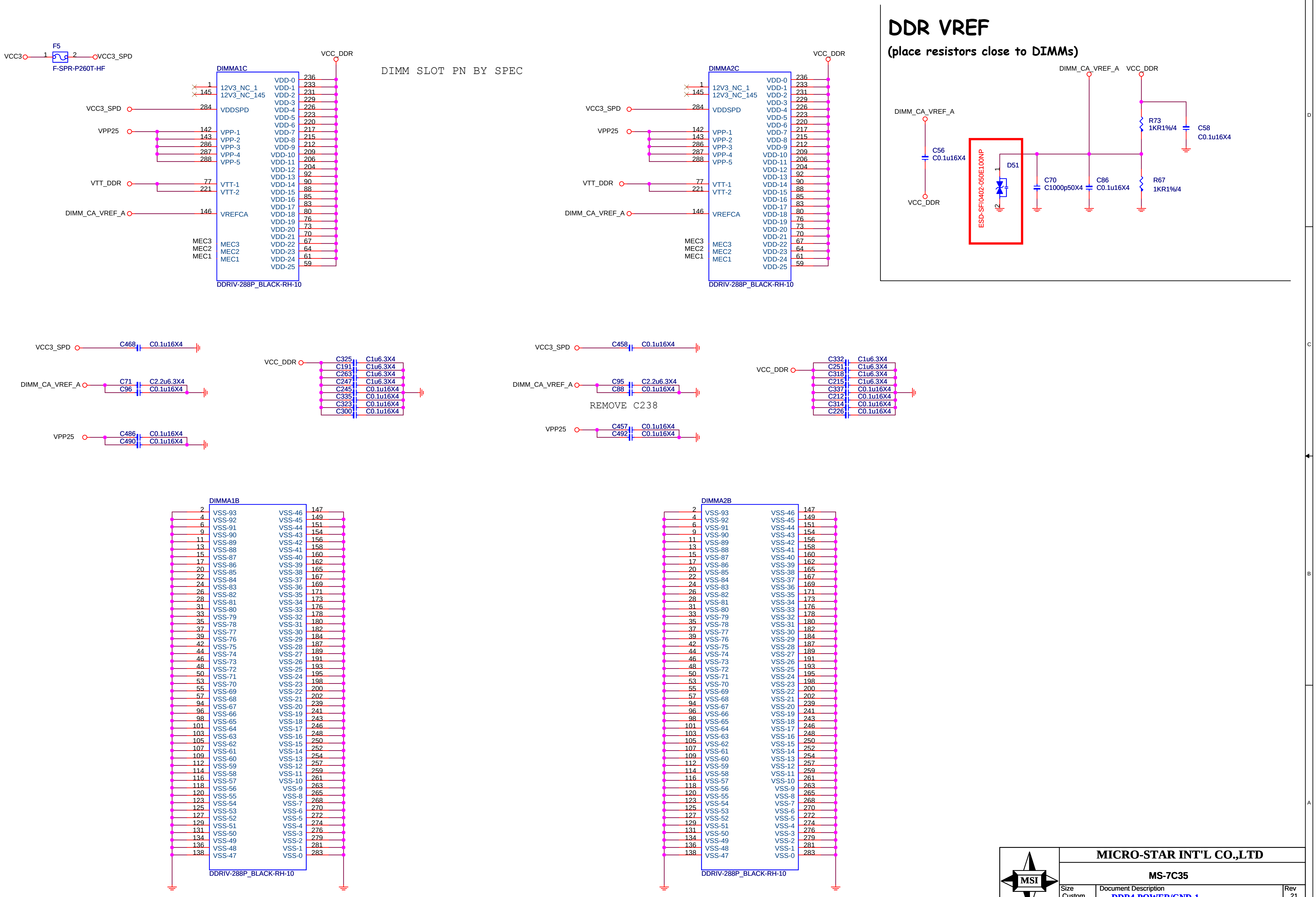
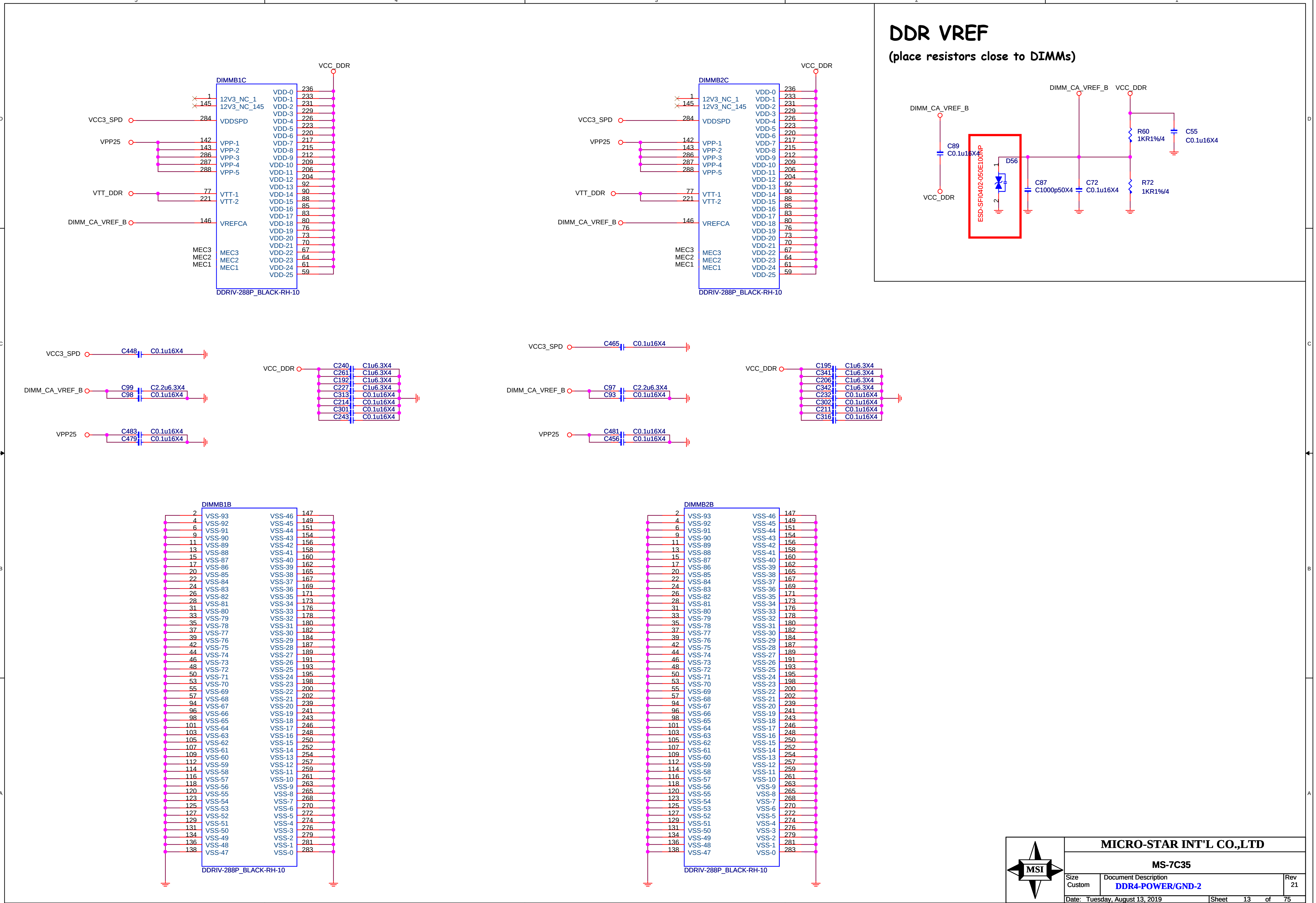
MS-7C35

Size	Document Description	Rev
Custom	DDR4-DIMM CH-B	21

Date: Tuesday, August 13, 2019 | Sheet 11 of 75



MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: DDR4-POWER/GND-1	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 12 of 75	

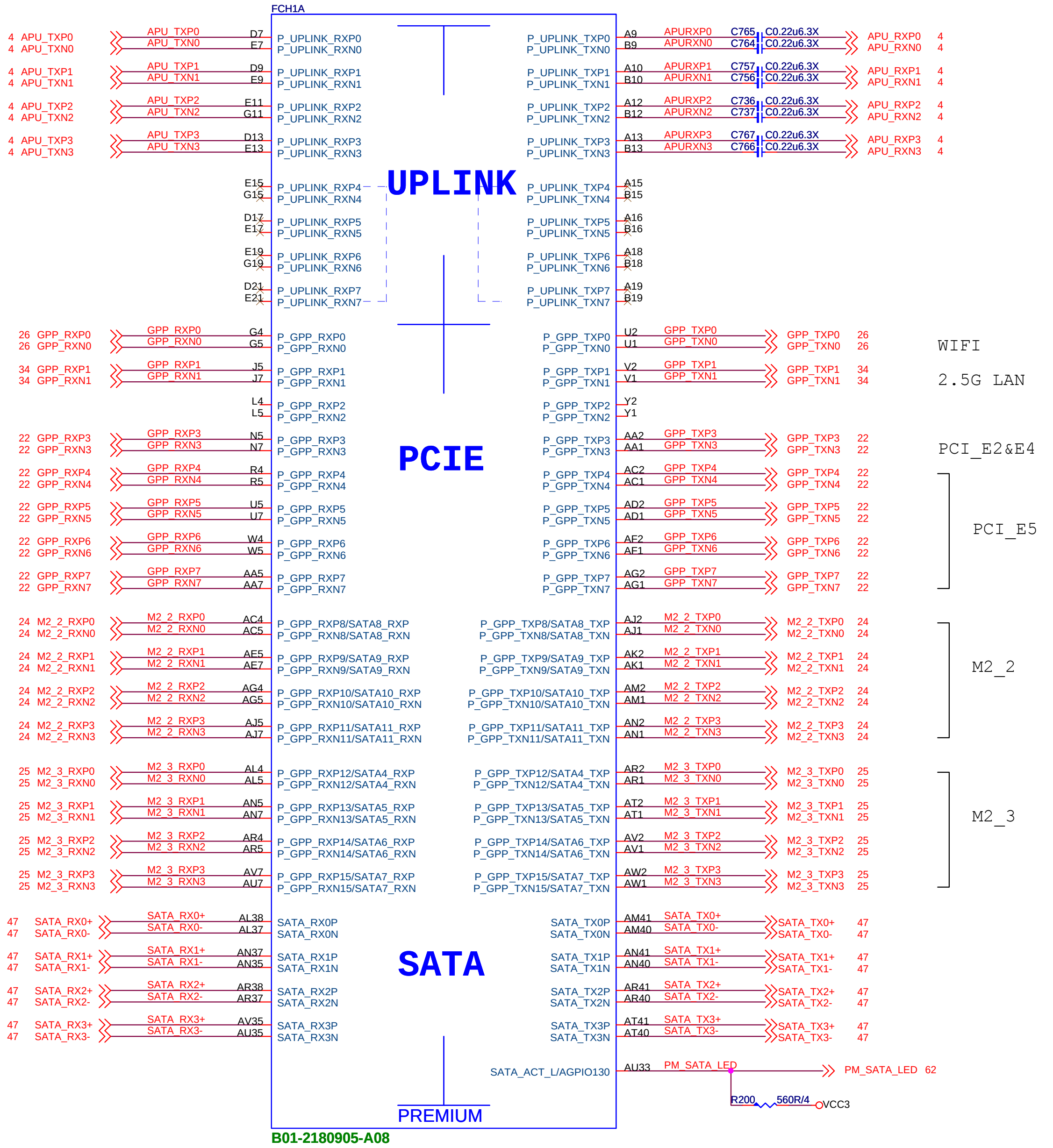


MICRO-STAR INT'L CO.,LTD

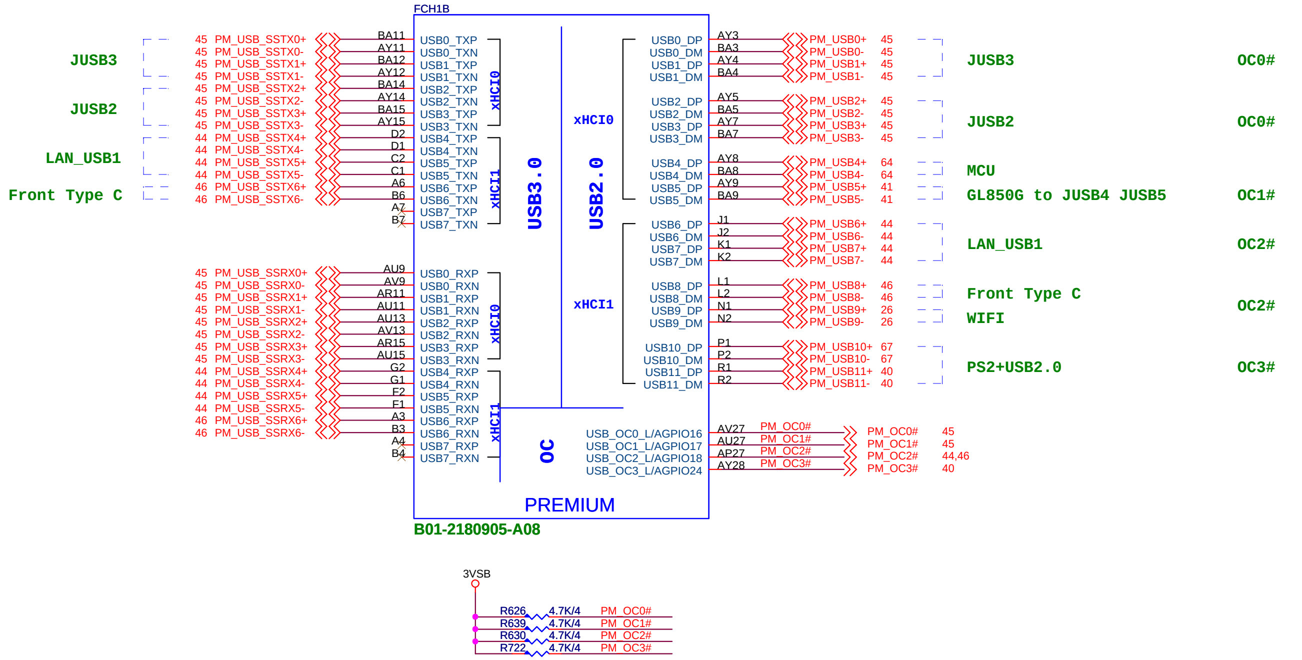
MS-7C35

Size	Document Description	Rev
Custom	DDR4-POWER/GND-2	21

Date: Tuesday, August 13, 2019 Sheet 13 of 75



MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: Promontory-PCIE/SATA/SATAE	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 14 of 75	



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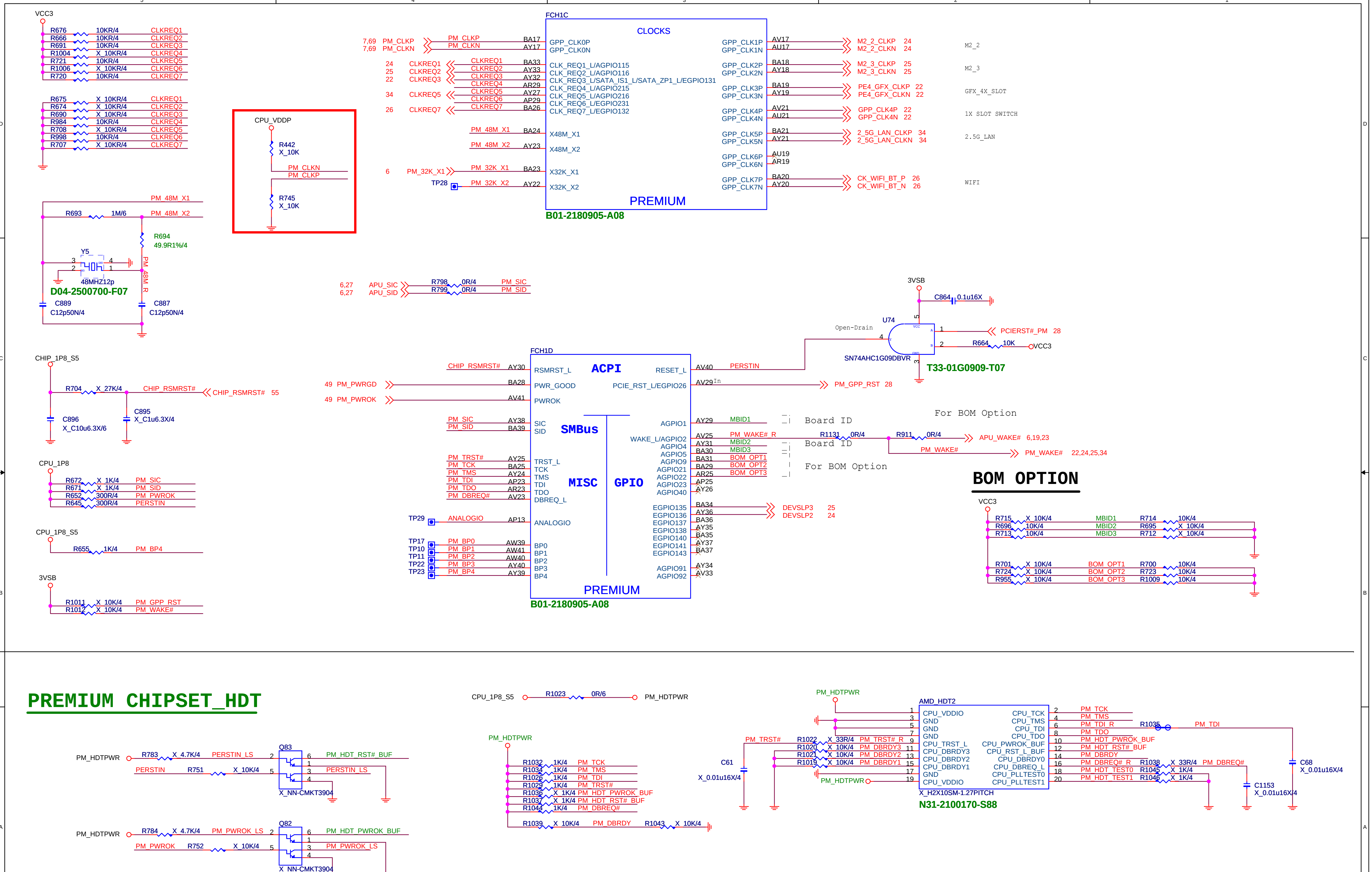
Size	Document Description	Rev
Custom	Promontory-USB/OC	21

Date: Tuesday, August 13, 2019 Sheet 15 of 75



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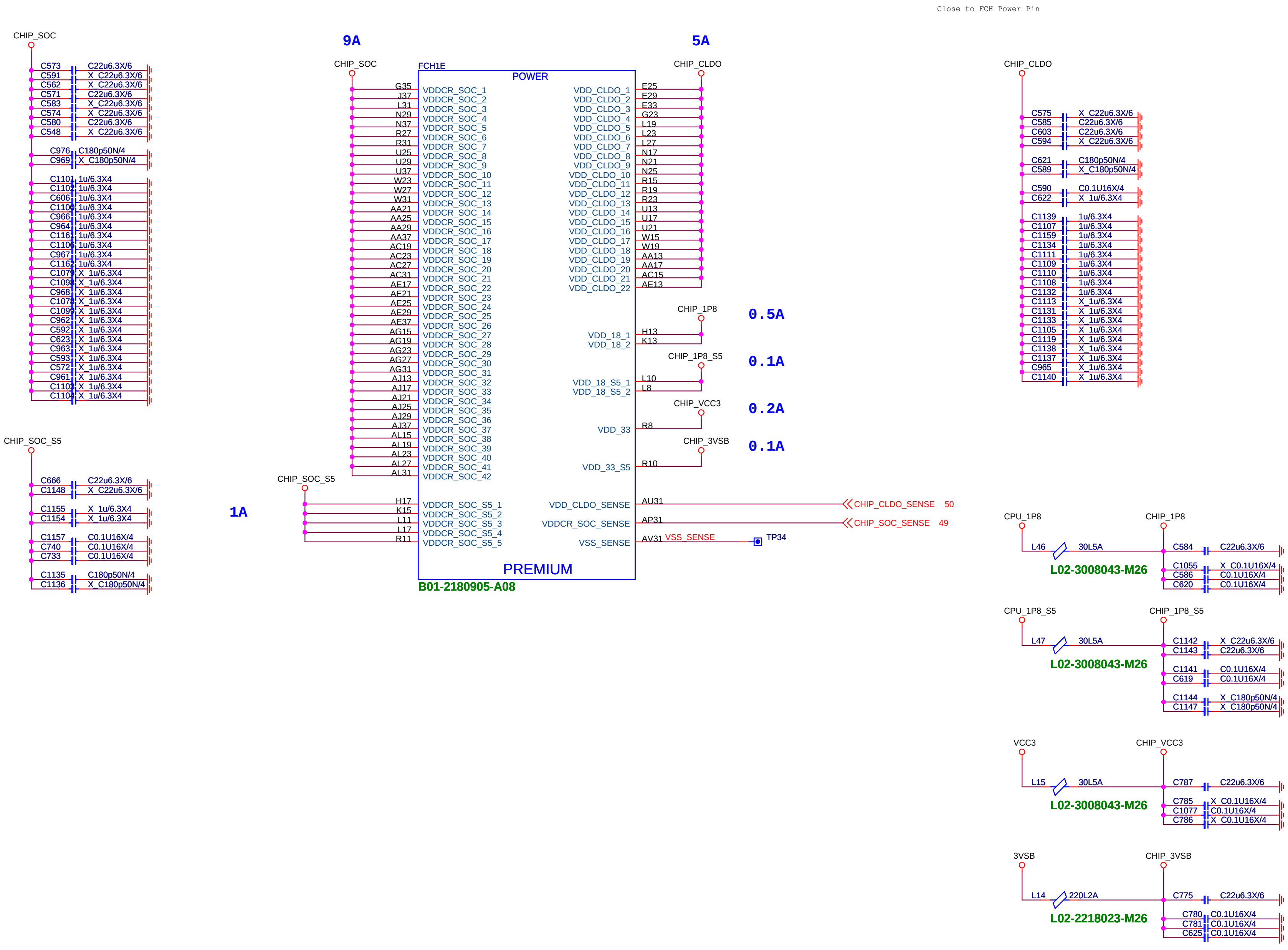
MS-7C35

Size	Document Description	Rev
Custom	Promontory-CLK/ACPI/GPIO	21

Date: Tuesday, August 13, 2019 | Sheet 16 of 75

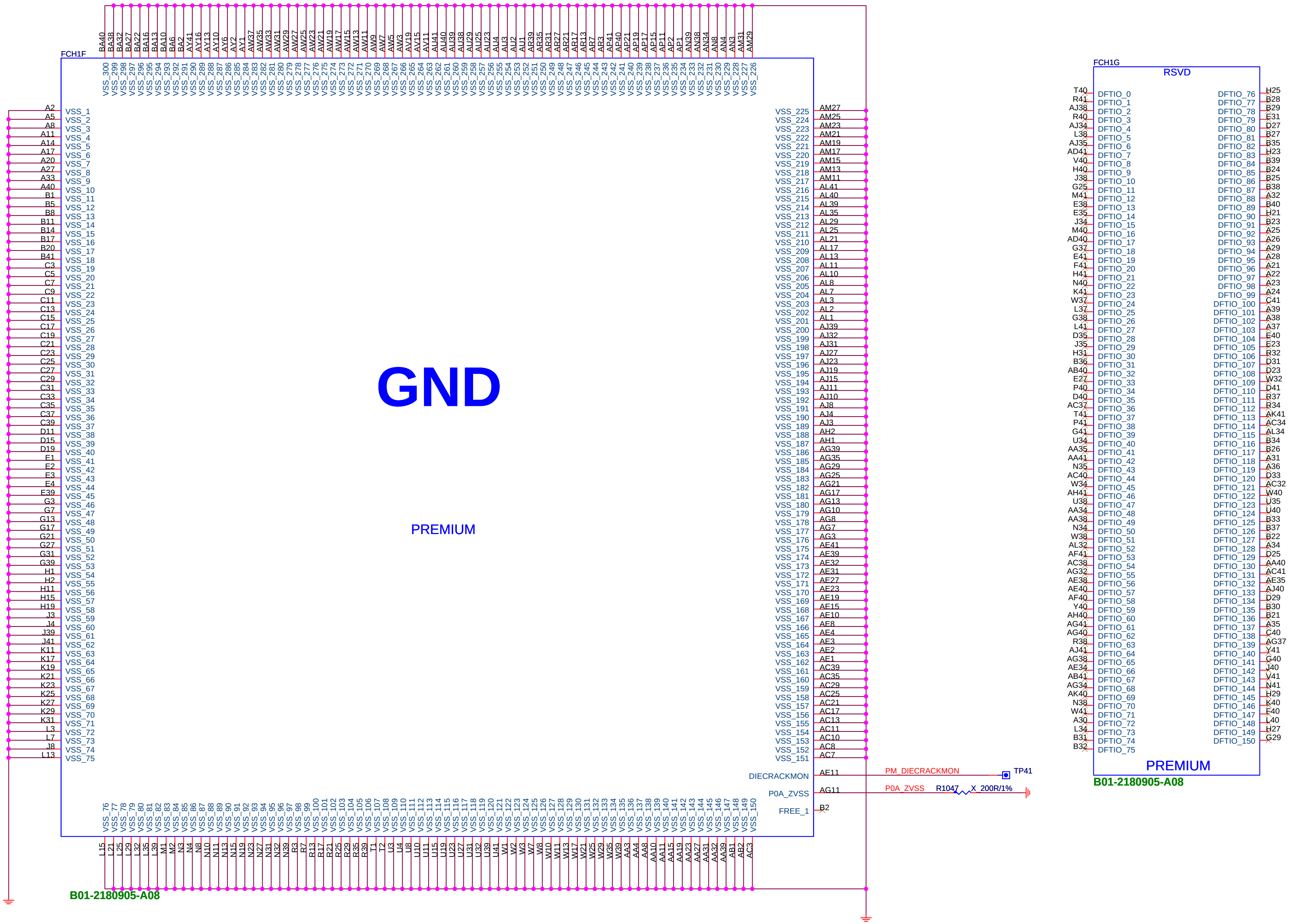


MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	Promontory-Power	21

Date: Tuesday, August 13, 2019 Sheet 17 of 75



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MS-7C35

Size	Document Description	Rev
Custom	Promontory-GND	21

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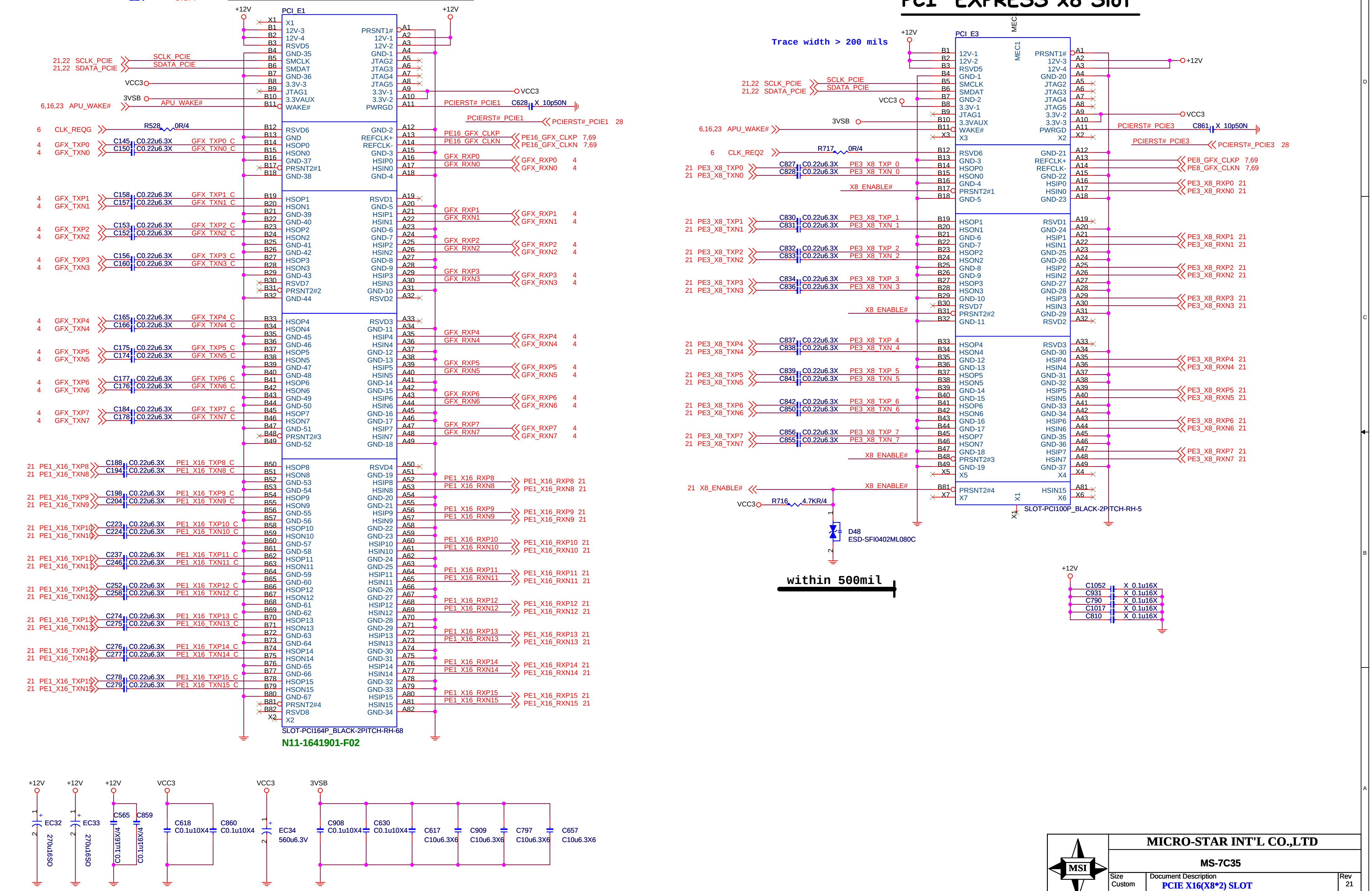
PCI EXPRESS x16 Slot

PCI EXPRESS x8 Slot



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Size	Document Description	Rev
Custom	PCIE X16(X8*2) SLOT	21

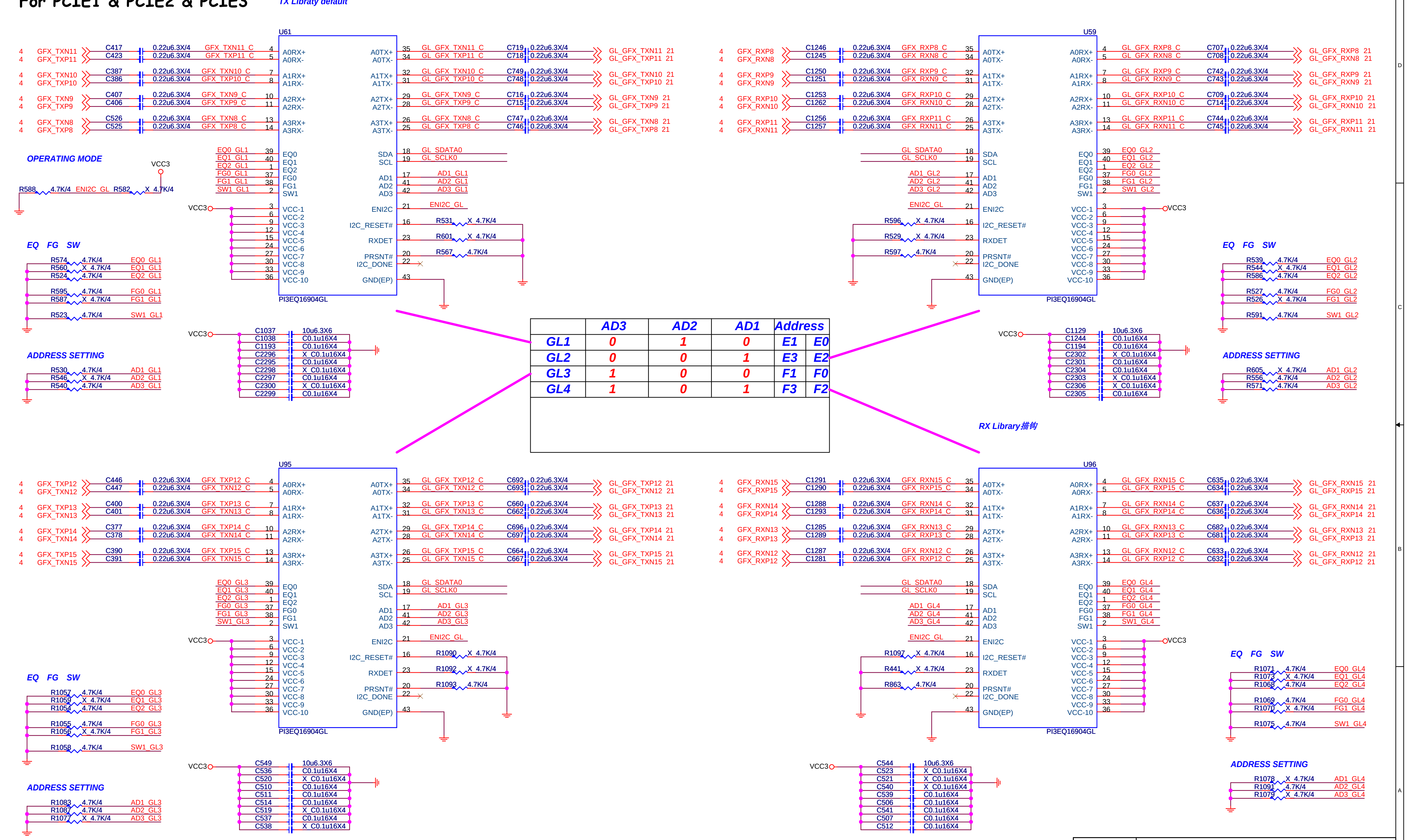
Date: Tuesday, August 13, 2019 Sheet 19 of 75

I²C Programming

Address assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	AD3	AD2	AD1	0	1=R, 0=W

For PCIE1 & PCIE2 & PCIE3



	AD3	AD2	AD1	Address	
GL1	0	1	0	E1	E0
GL2	0	0	1	E3	E2
GL3	1	0	0	F1	F0
GL4	1	0	1	F3	F2

MSI

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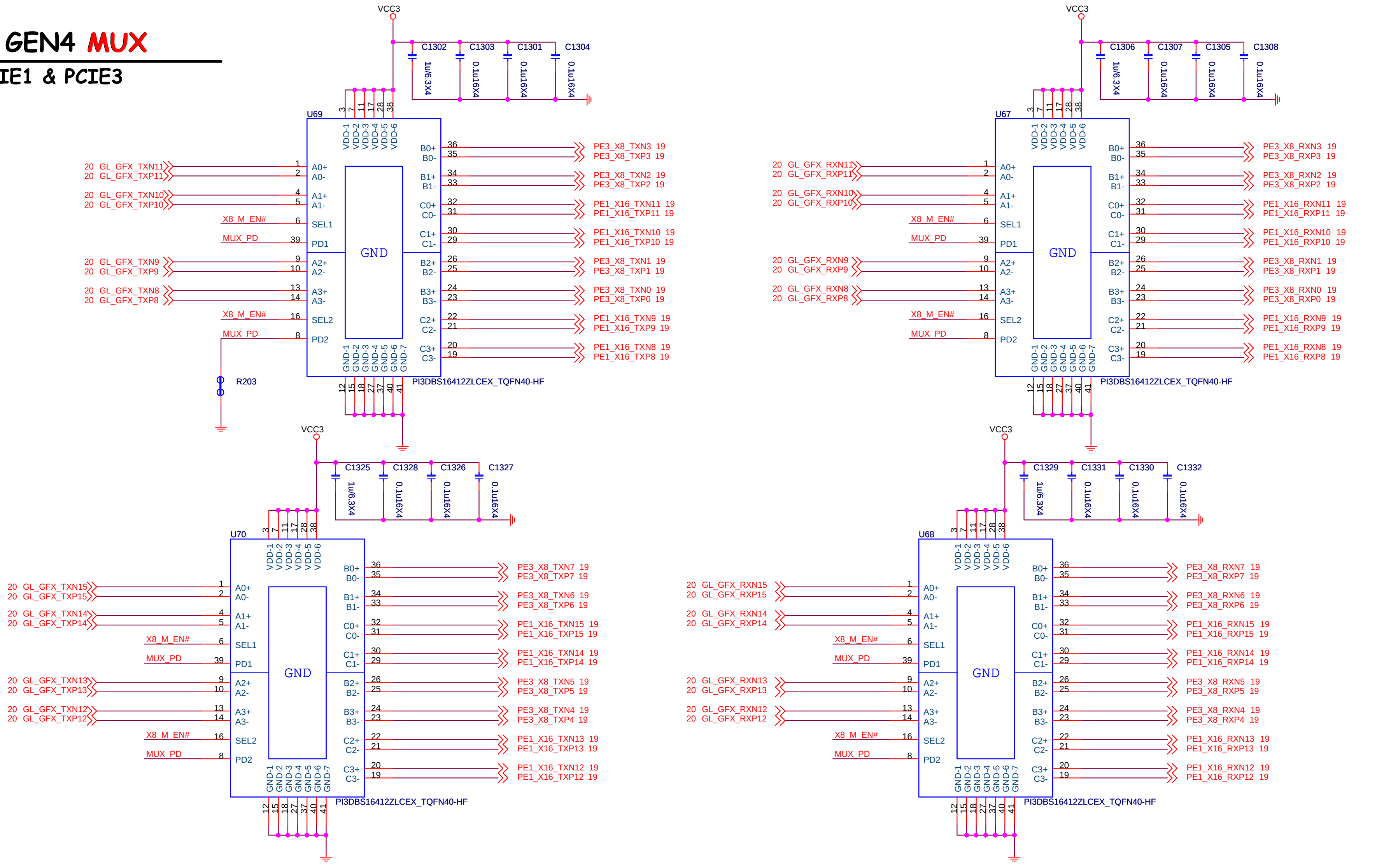
MS-7C35

Size	Document Description	Rev
Custom	PCIE Switch	21

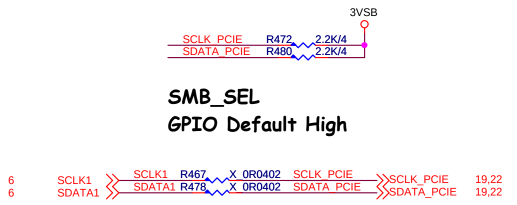
Date: Tuesday, August 13, 2019 Sheet 20 of 75

PCIE GEN4 MUX

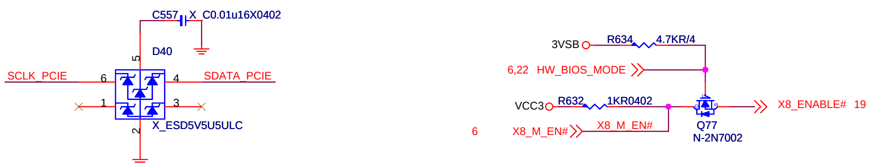
For PCIE1 & PCIE3



SMBus separate circuit



PCIE Lanes control circuit



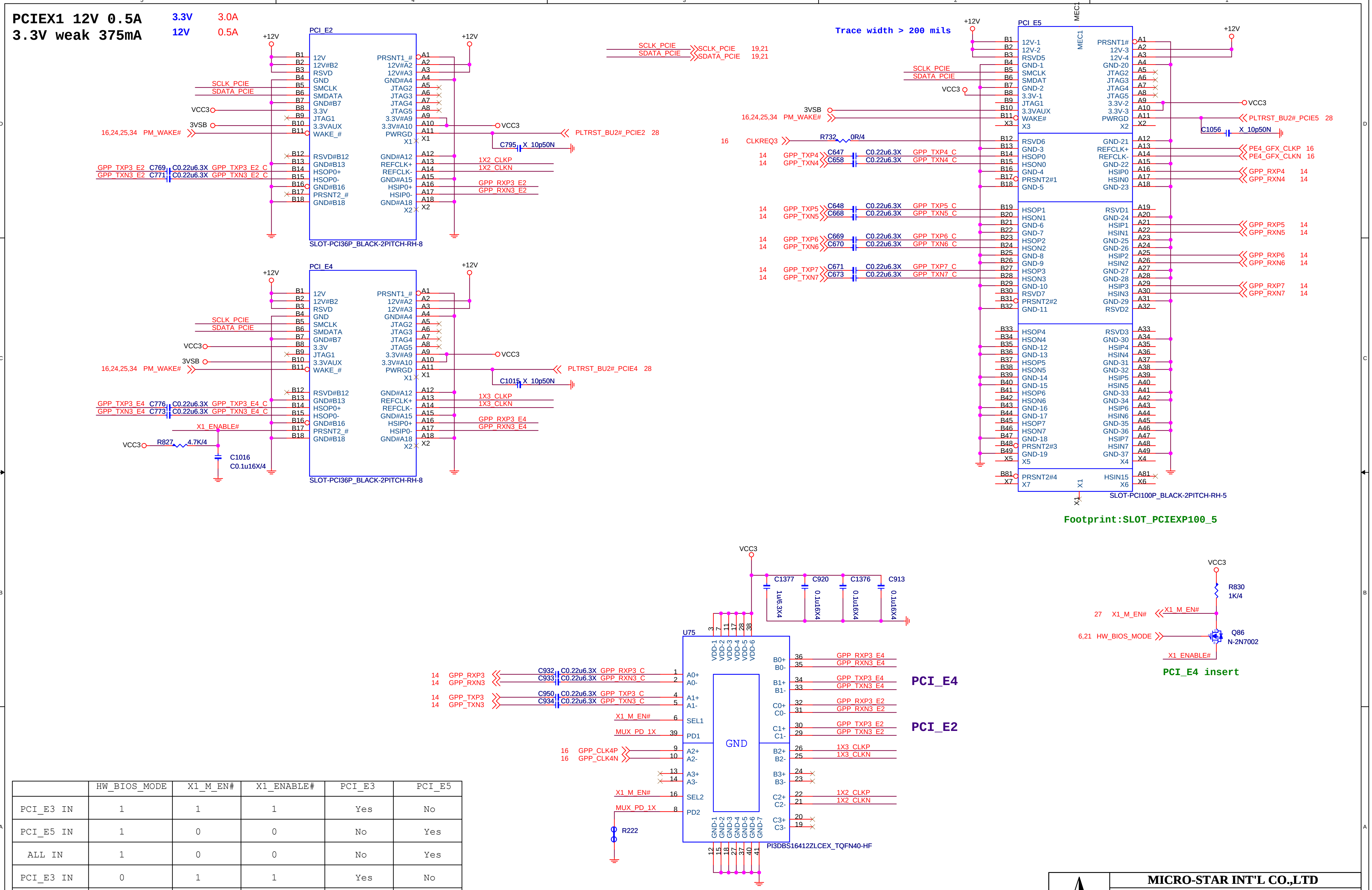
	PCIE_CNTL	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	PCIE Switch	21

Date: Tuesday, August 13, 2019 | Sheet 21 of 75



	HW_BIOS_MODE	X1_M_EN#	X1_ENABLE#	PCI_E3	PCI_E5
PCI_E3 IN	1	1	1	Yes	No
PCI_E5 IN	1	0	0	No	Yes
ALL IN	1	0	0	No	Yes
PCI_E3 IN	0	1	1	Yes	No
PCI_E5 IN	0	1	0	Yes	No
ALL IN	0	1	0	Yes	No

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size: Custom | Document Description: PCIE 1X 4X | Rev 21

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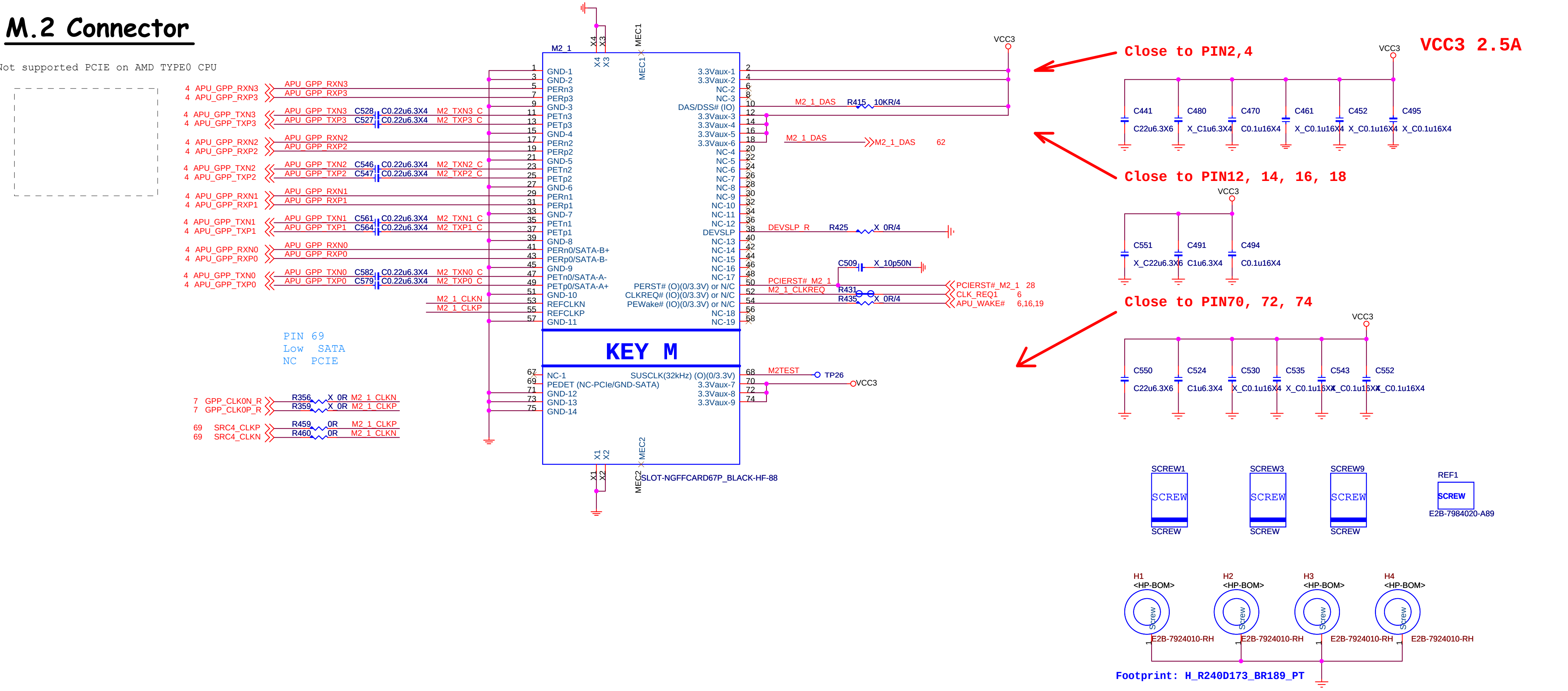
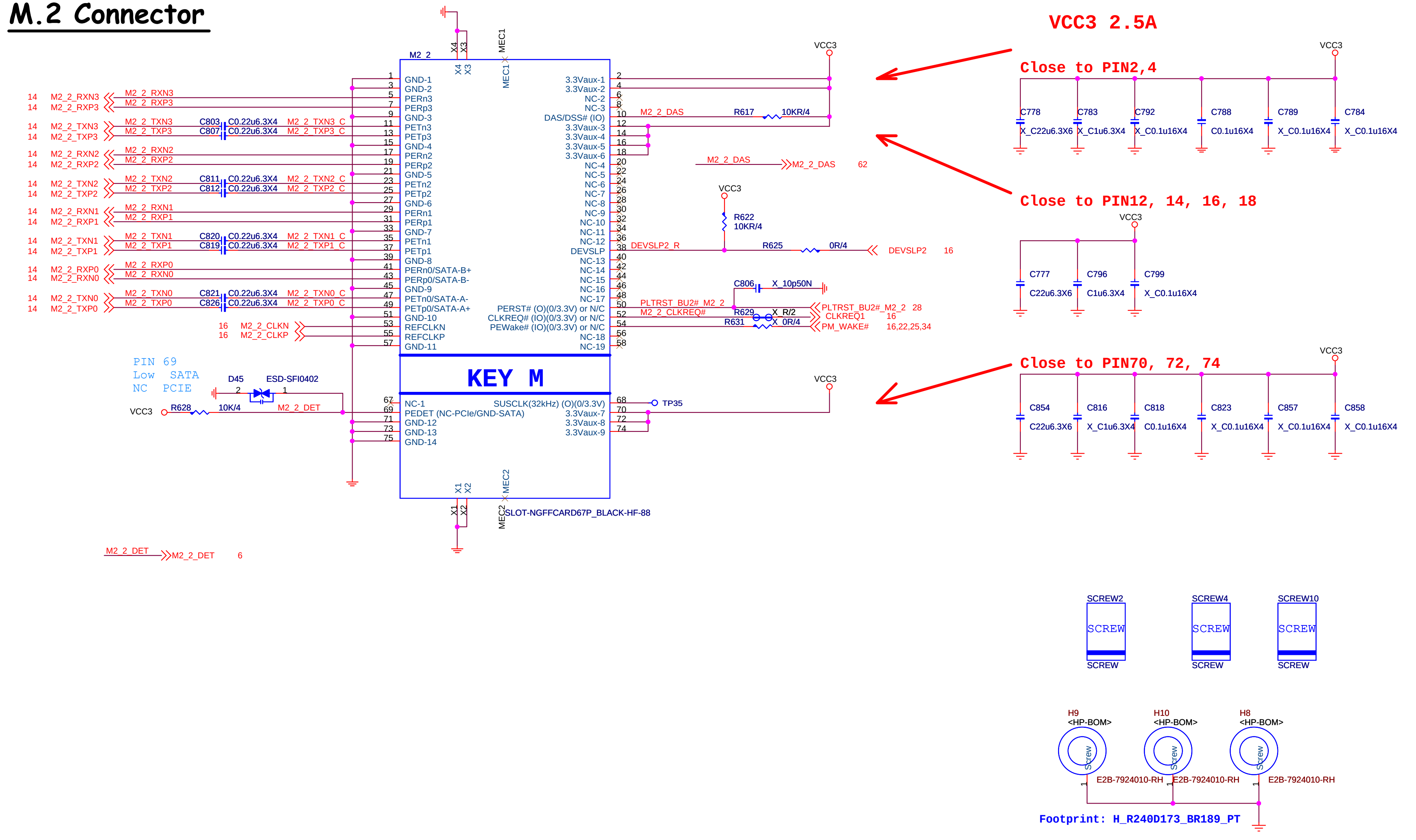
M.2 Connector

Not supported PCIE on AMD TYPE0 CPU



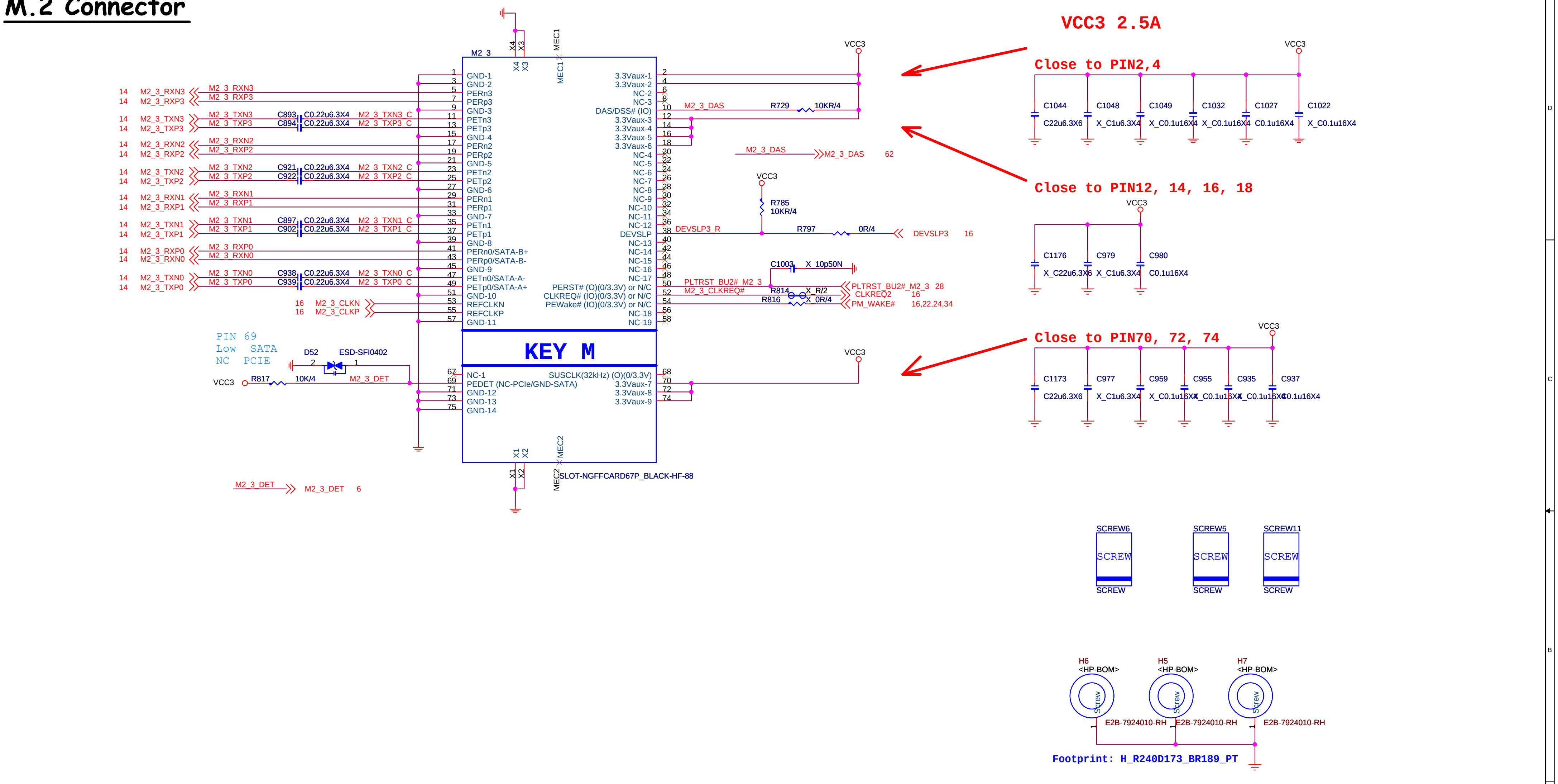
MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: M.2_1 Connector	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 23 of 75	

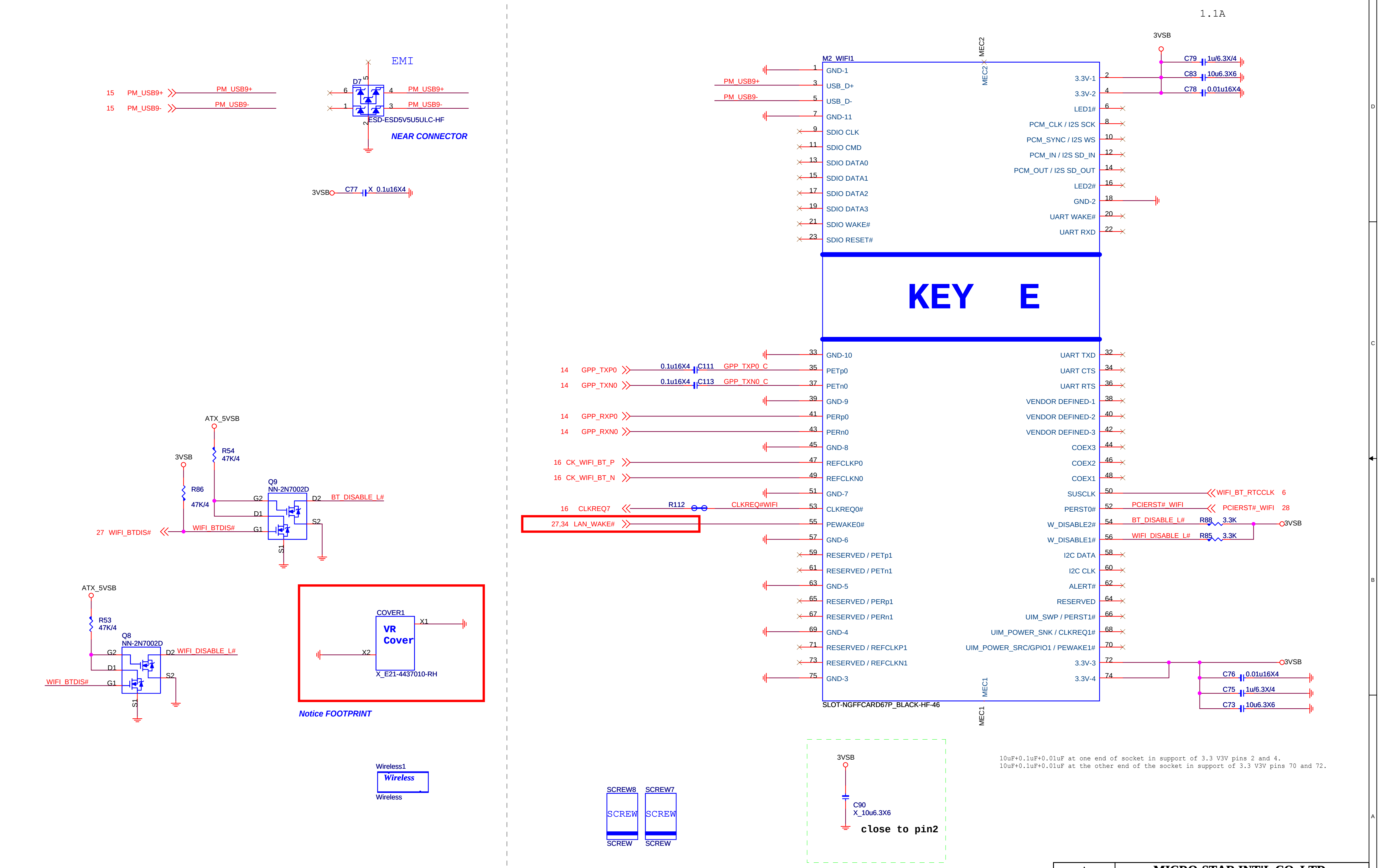
M.2 Connector



MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: M2_2 Connector	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 24 of 75	

M.2 Connector





MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	WIFI & BT	21

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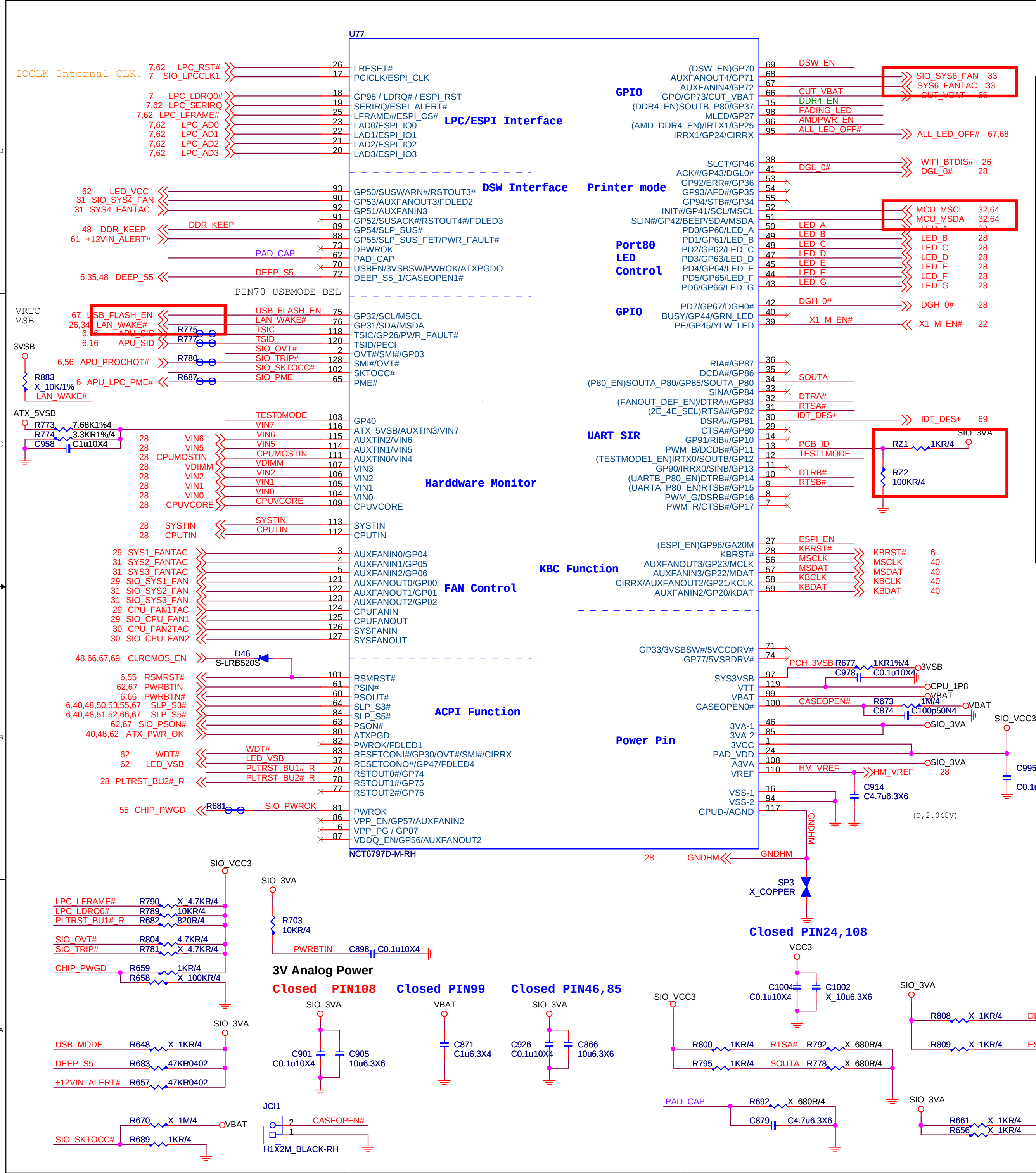
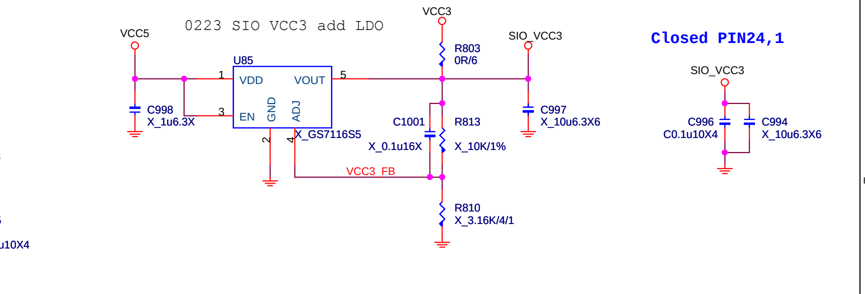


POWER ON STRAPPING PIN FOR NCT6797/6795

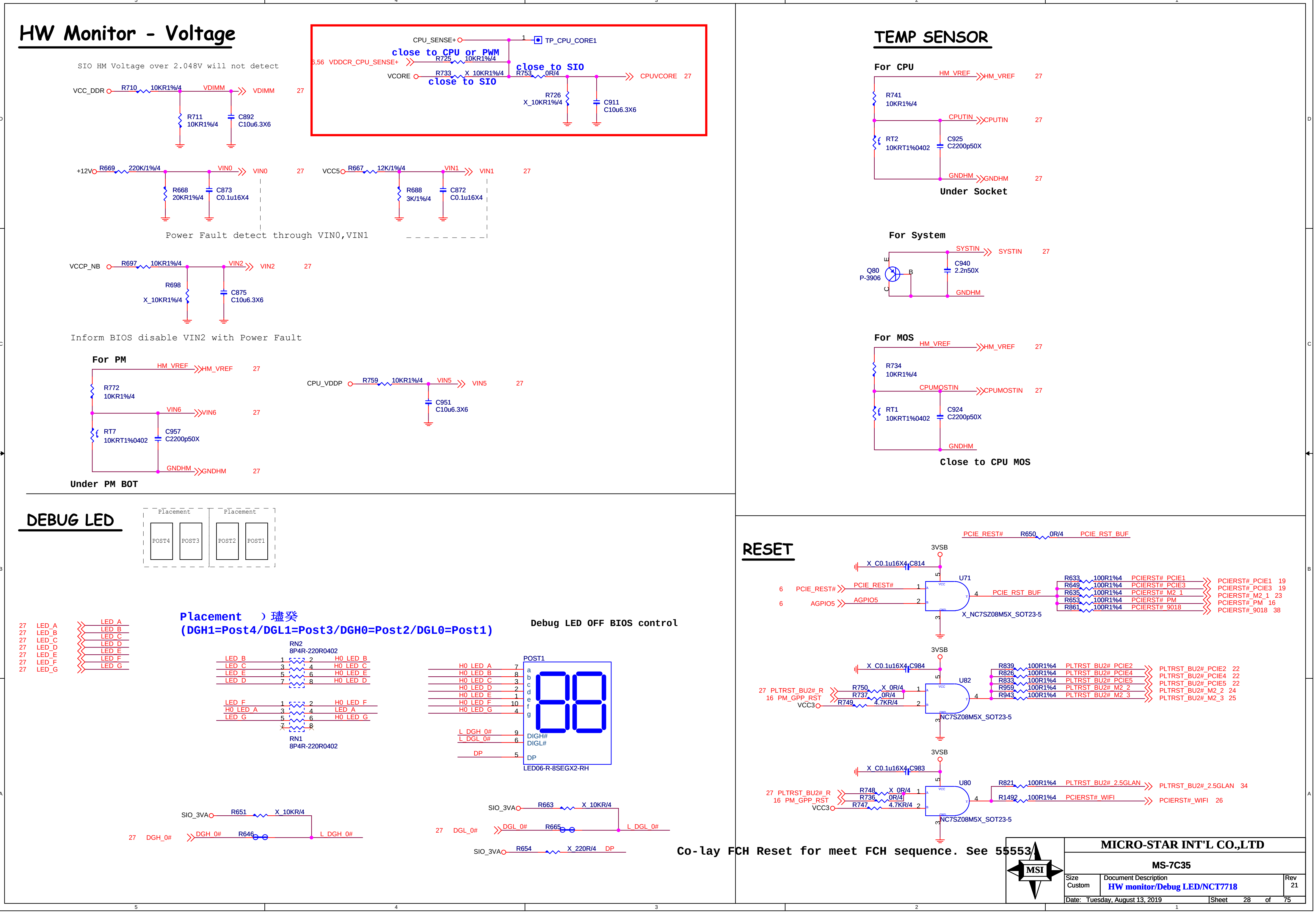
PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TESTMODE1_EN	ENABLE TESTMODE1_EN	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMD_DDR4_EN	AMD_DDR4_EN	DISABLE AMD DDR4 PWR	ENABLE AMD DDR4 PWR	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

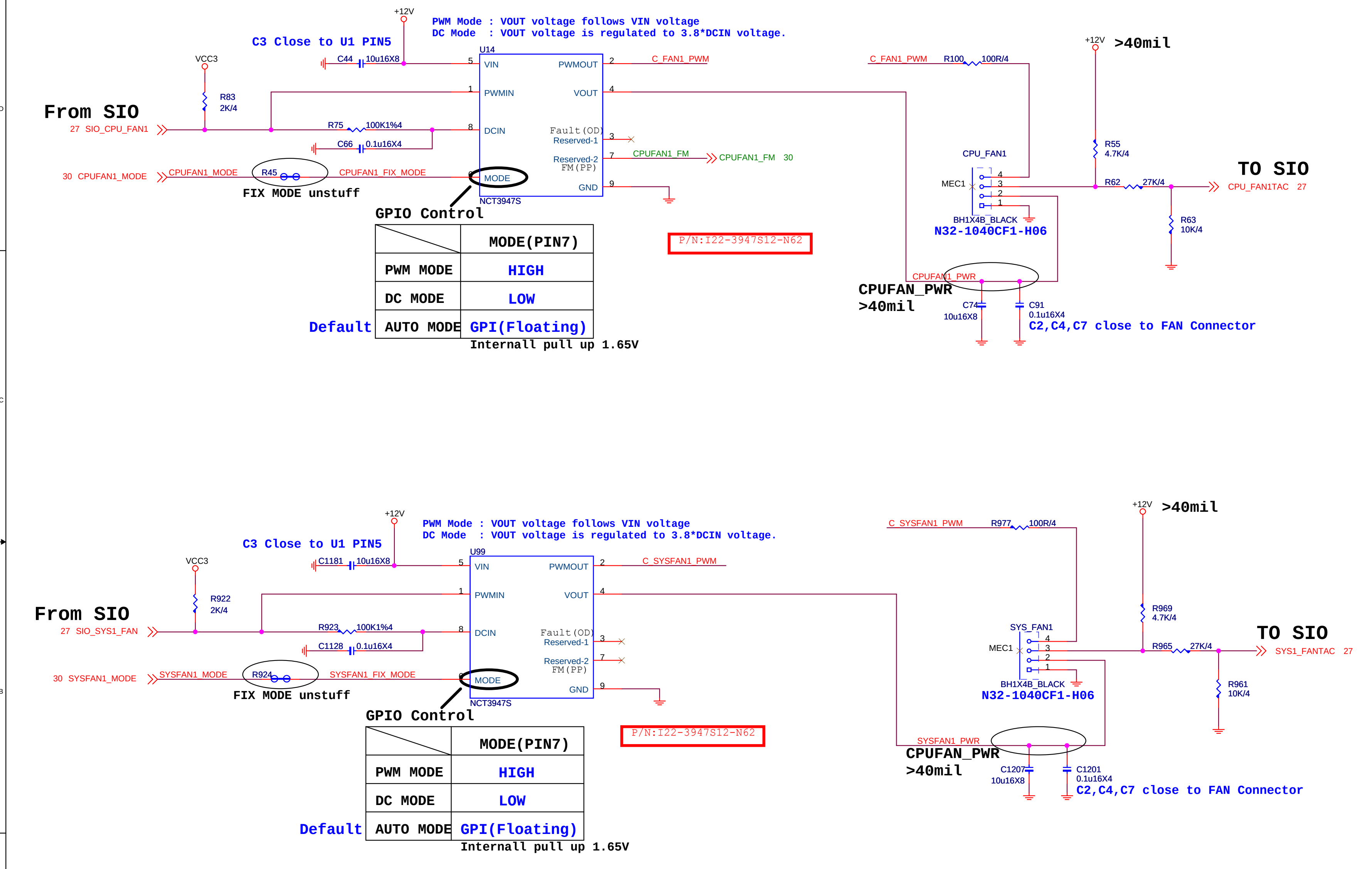


Co-Lay NCT6795

(PIN9)(RTSB#)80_ENA	0=Disable	1=Enable
(PIN10)(DTRB#)80_ENB	0=Disable	1=Enable
(PIN32)(DTRA#)FANOUT	0=50%	1=100%
(PIN12)TEST_MODE_EN1	0=Disable	1=Enable
(PIN103)TEST_MODE_EN0	0=Disable	1=Enable
(PIN27)ESPI_EN0	0=LPC	1=ESPI
(PIN15)DDR4_EN	0=Disable	1=Enable



HW Monitor - Voltage
SIO HM Voltage over 2.048V will not detect
VCC_DDR R710 10KR1%/4 VDIMM VDIMM 27
R711 10KR1%/4
C892 C10u6.3X6
CPU_SENSE+ TP_CPU_CORE1
close to CPU or PWM
5,56 VDDCR_CPU_SENSE+ R725 10KR1%/4
VCORE R733 X_10KR1%/4 R753 0R/4 CPUVCORE 27
close to SIO
close to SIO
R726 X_10KR1%/4
C911 C10u6.3X6
+12V R669 220K/1%/4 VIN0 VIN0 27
R668 20KR1%/4
C873 C0.1u16X4
VCC5 R667 12K/1%/4 VIN1 VIN1 27
R688 3K/1%/4
C872 C0.1u16X4
Power Fault detect through VIN0,VIN1
VCCP_NB R697 10KR1%/4 VIN2 VIN2 27
R698 X_10KR1%/4
C875 C10u6.3X6
Inform BIOS disable VIN2 with Power Fault
For PM
HM_VREF HM_VREF 27
R772 10KR1%/4
VIN6 VIN6 27
RT7 10KRT1%0402
C957 C2200p50X
GNDHM GNDHM 27
Under PM BOT
CPU_VDDP R759 10KR1%/4 VIN5 VIN5 27
C951 C10u6.3X6
TEMP SENSOR
For CPU
HM_VREF HM_VREF 27
R741 10KR1%/4
CPUTIN CPUTIN 27
RT2 10KRT1%0402
C925 C2200p50X
GNDHM GNDHM 27
Under Socket
For System
SYSTIN SYSTIN 27
Q80 P-3906
C940 2.2n50X
GNDHM
For MOS
HM_VREF HM_VREF 27
R734 10KR1%/4
CPUMOSTIN CPUMOSTIN 27
RT1 10KRT1%0402
C924 C2200p50X
GNDHM
Close to CPU MOS
DEBUG LED
Placement POST4 POST3
Placement POST2 POST1
27 LED_A
27 LED_B
27 LED_C
27 LED_D
27 LED_E
27 LED_F
27 LED_G
Placement ）璛癸
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)
RN2 8P4R-220R0402
LED_B H0_LED_B
LED_C H0_LED_C
LED_E H0_LED_E
LED_D H0_LED_D
LED_F H0_LED_F
H0_LED_A LED_A
LED_G H0_LED_G
RN1 8P4R-220R0402
Debug LED OFF BIOS control
POST1
H0_LED_A
H0_LED_B
H0_LED_C
H0_LED_D
H0_LED_E
H0_LED_F
H0_LED_G
L_DGH_0#
L_DGL_0#
DP
DIGH#
DIGL#
LED06-R-8SEGX2-RH
SIO_3VA R651 X_10KR/4
27 DGH_0# DGH_0# R646 L_DGH_0#
SIO_3VA R663 X_10KR/4
27 DGL_0# DGL_0# R665 L_DGL_0#
SIO_3VA R654 X_220R/4 DP
RESET
PCIE_REST# R650 0R/4 PCIE_RST_BUF
3VSB
X_C0.1u16X4 C814
U71
6 PCIE_REST# PCIE_REST#
6 AGPIO5 AGPIO5
PCIE_RST_BUF
X_NC7SZ08M5X_SOT23-5
R633 100R1%4 PCIERST#_PCIE1 PCIERST#_PCIE1 19
R649 100R1%4 PCIERST#_PCIE3 PCIERST#_PCIE3 19
R635 100R1%4 PCIERST#_M2_1 PCIERST#_M2_1 23
R653 100R1%4 PCIERST#_PM PCIERST#_PM 16
R861 100R1%4 PCIERST#_9018 PCIERST#_9018 38
3VSB
X_C0.1u16X4 C984
U82
27 PLTRST_BU2#_R
16 PM_GPP_RST
VCC3
R750 X_0R/4
R737 0R/4
R749 4.7KR/4
NC7SZ08M5X_SOT23-5
R839 100R1%4 PLTRST_BU2#_PCIE2 PLTRST_BU2#_PCIE2 22
R826 100R1%4 PLTRST_BU2#_PCIE4 PLTRST_BU2#_PCIE4 22
R833 100R1%4 PLTRST_BU2#_PCIE5 PLTRST_BU2#_PCIE5 22
R959 100R1%4 PLTRST_BU2#_M2_2 PLTRST_BU2#_M2_2 24
R943 100R1%4 PLTRST_BU2#_M2_3 PLTRST_BU2#_M2_3 25
3VSB
X_C0.1u16X4 C983
U80
27 PLTRST_BU2#_R
16 PM_GPP_RST
VCC3
R748 X_0R/4
R736 0R/4
R747 4.7KR/4
NC7SZ08M5X_SOT23-5
R821 100R1%4 PLTRST_BU2#_2.5GLAN PLTRST_BU2#_2.5GLAN 34
R1492 100R1%4 PCIERST#_WIFI PCIERST#_WIFI 26
Co-lay FCH Reset for meet FCH sequence. See 55553
MSI
MICRO-STAR INT'L CO.,LTD
MS-7C35
Size Custom
Document Description
HW monitor/Debug LED/NCT7718
Rev 21
Date: Tuesday, August 13, 2019
Sheet 28 of 75



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MSI

MICRO-STAR INT'L CO.,LTD

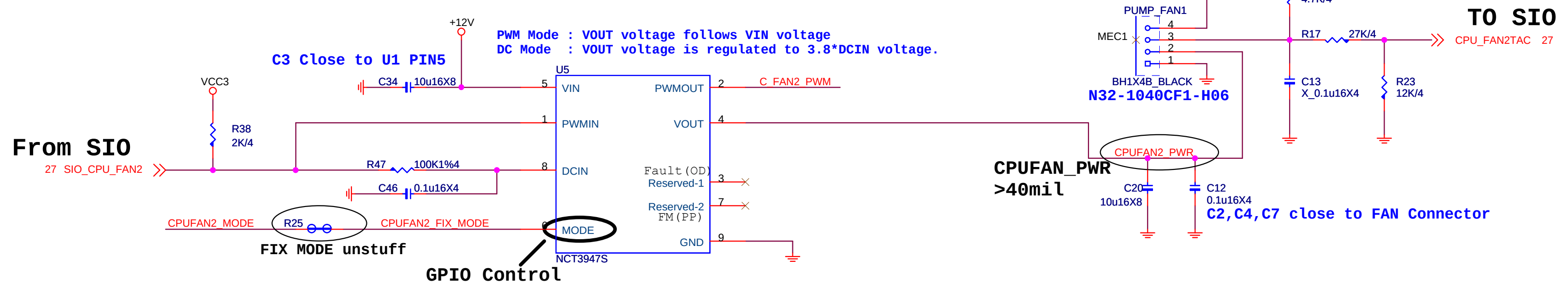
MS-7C35

Size	Document Description	Rev
Custom	CPU/SYS FAN X2 TYPE J	21

Date: Tuesday, August 13, 2019 Sheet 29 of 75

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パBIOSち俵 PWM/DC MODE



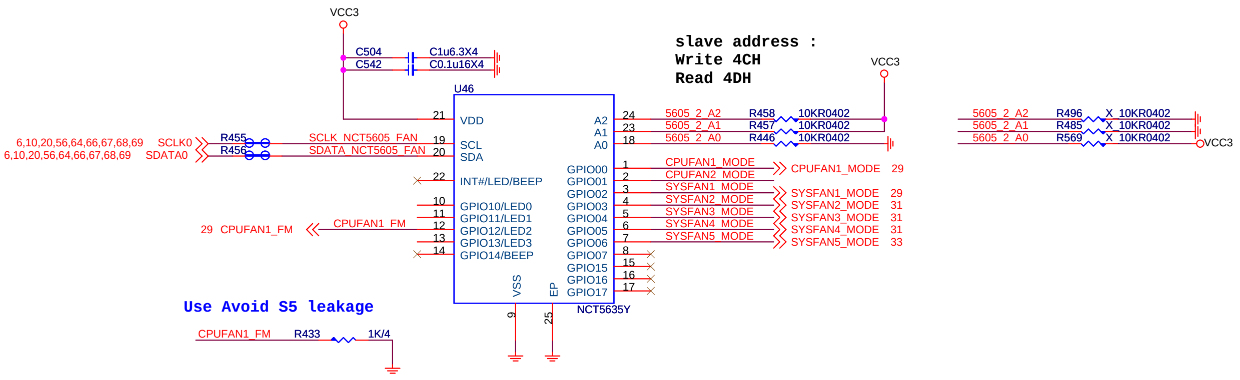
GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V

P/N:I22-3947S12-N62



1. GENERAL DESCRIPTION

20150722

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

Read 38H

NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W

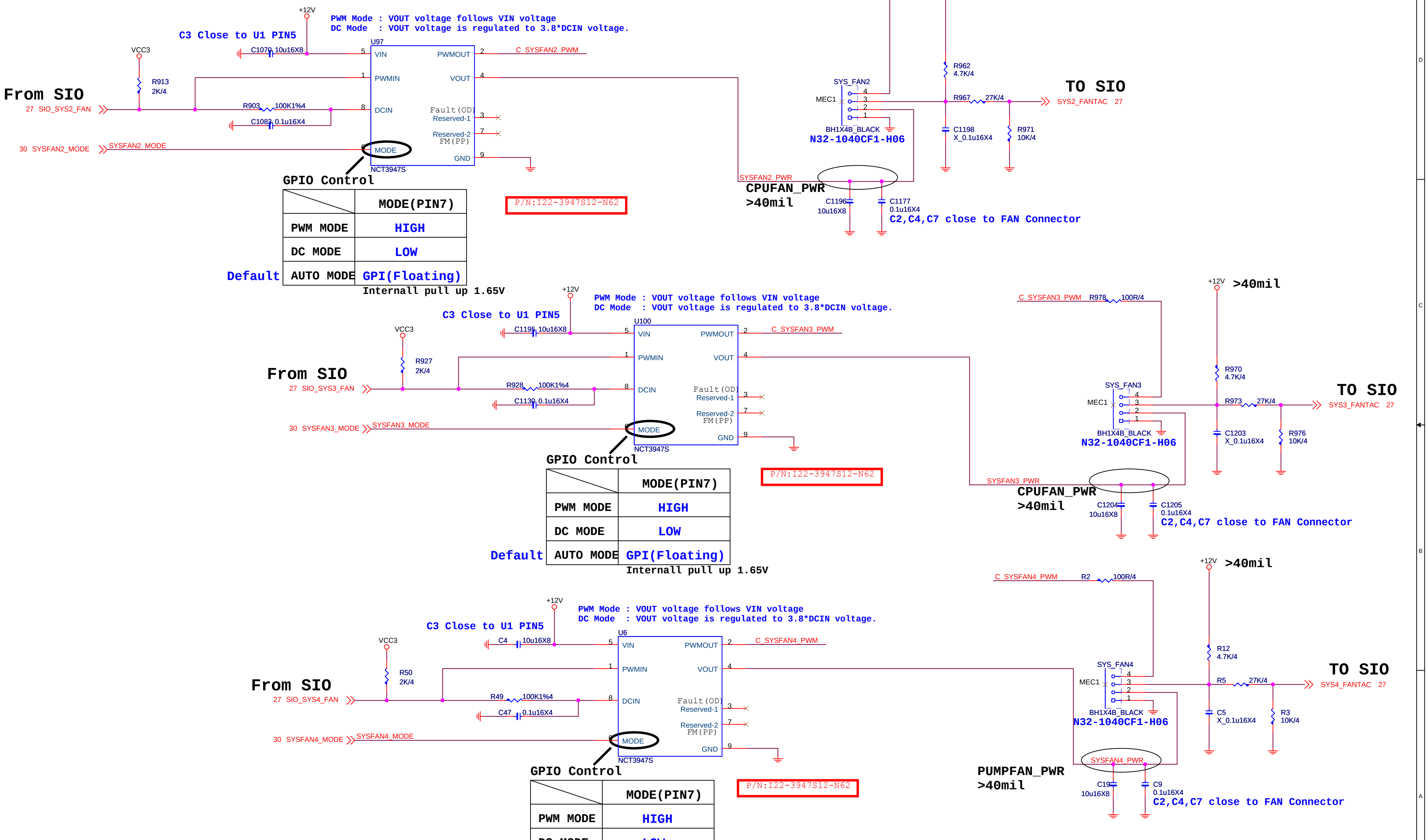
R/W: 0 (Read 38H), 1 (Write 39H)

Write 39H

MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: PUMP FAN TYPE J 2A	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 30 of 75	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パBIOSち传 PWM/DC MODE



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD
MS-7C35
Size: Custom | Document Description: SYS FAN X3 TYPE K | Rev 21
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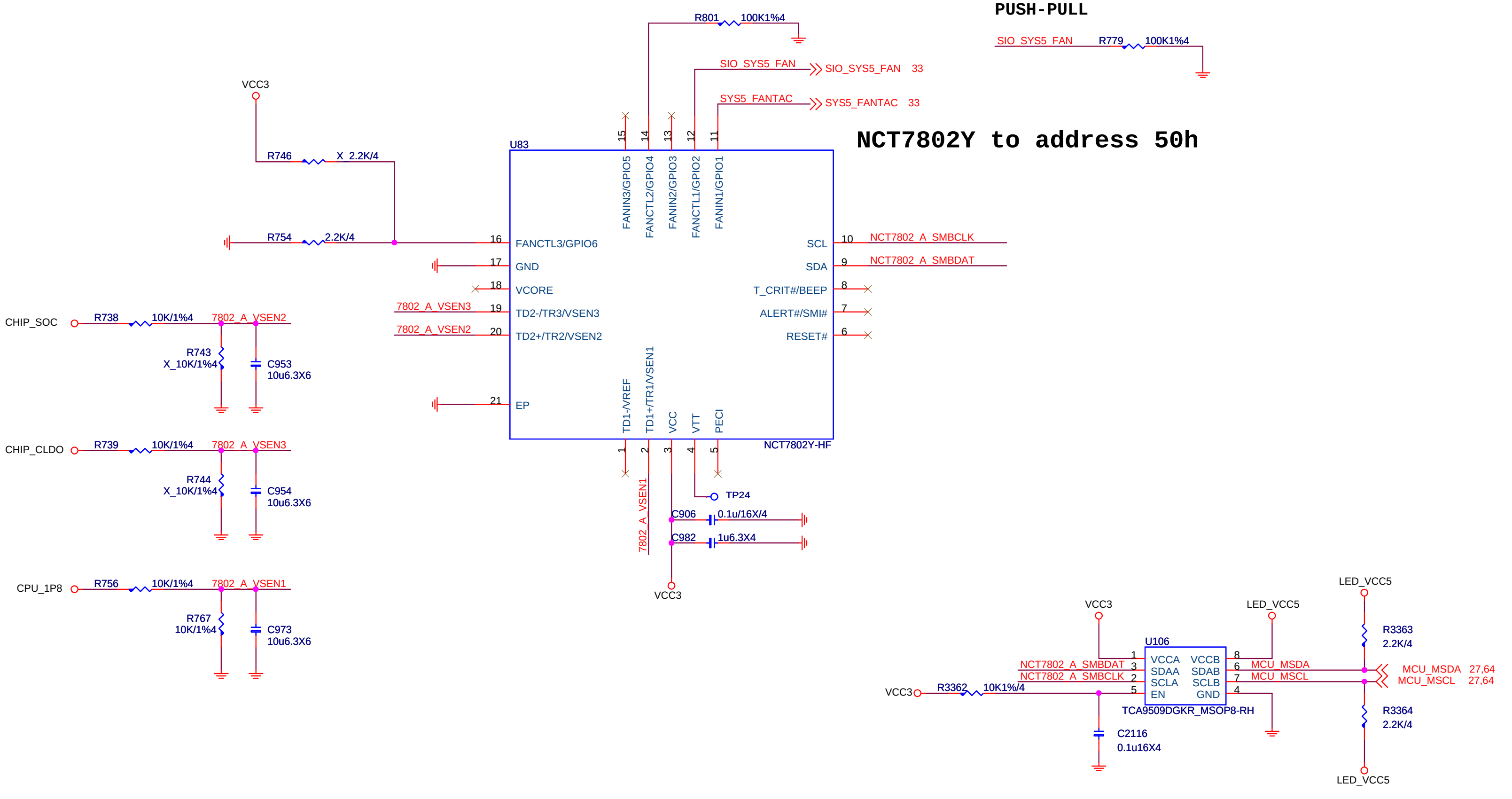
PUSH-PULL

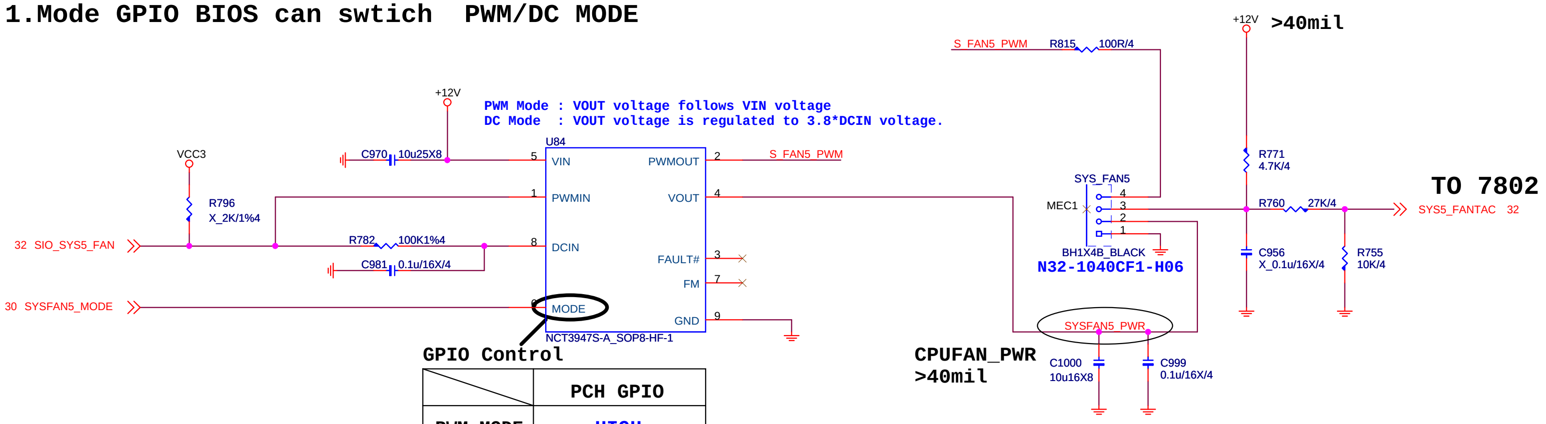
NCT7802Y to address 50h



MICRO-STAR INT'L CO.,LTD			
MS-7C35			
Size: Custom	Document Description: SYS FAN X3 TYPE K		Rev: 21
Date: Tuesday, August 13, 2019	Sheet 32 of 75		

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

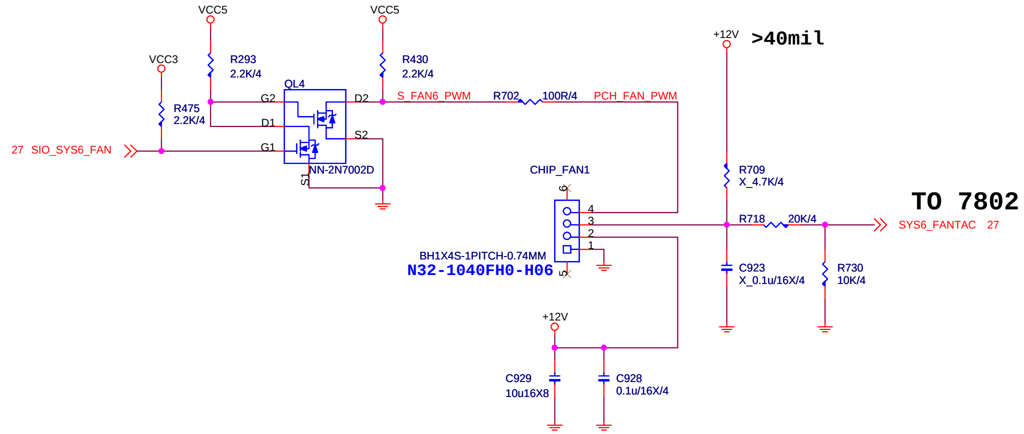


GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default (AUTO MODE)

Internall pull up 1.65V



MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: SYS FAN X3 TYPE K	Rev: 21
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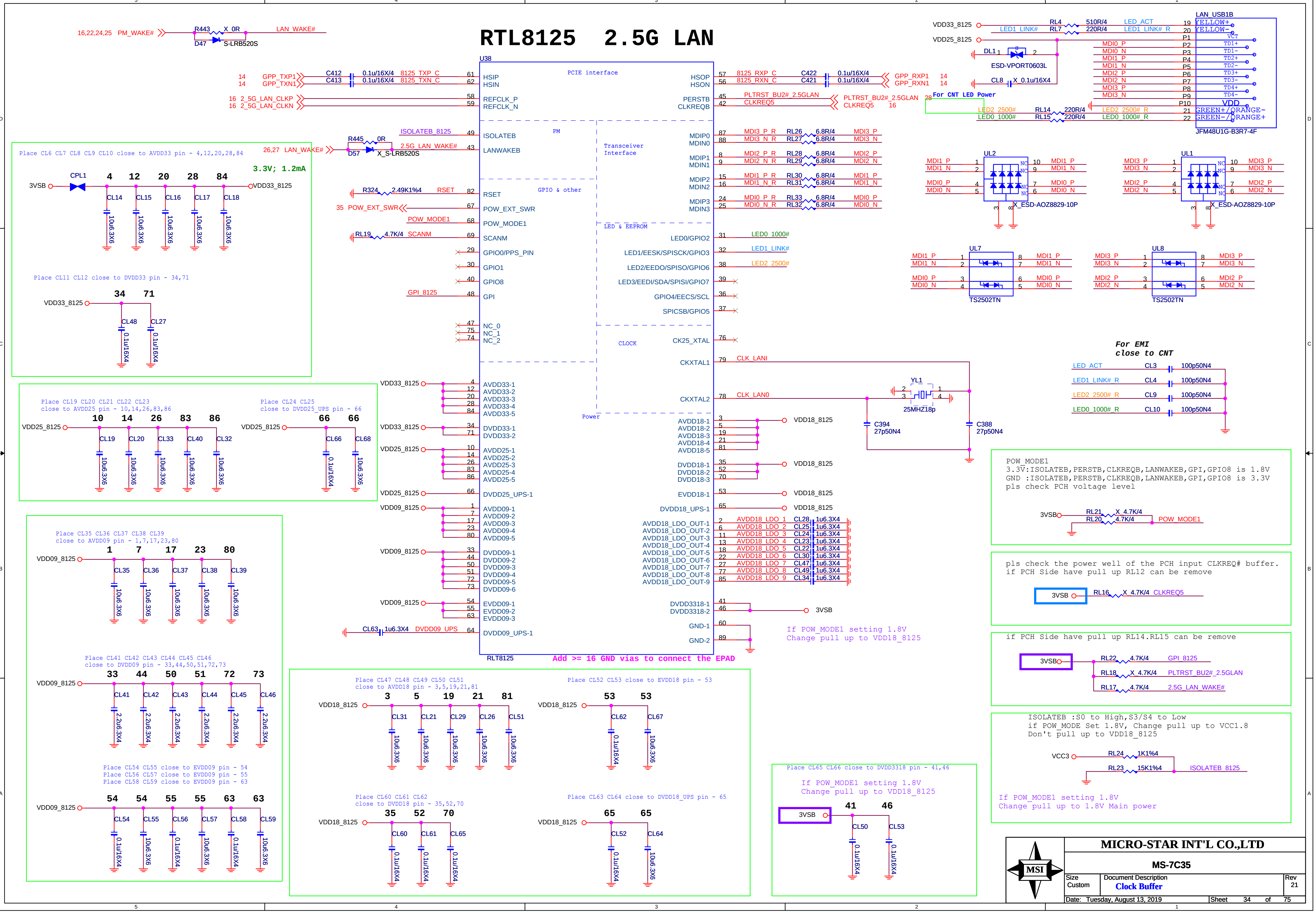

RTL8125 2.5G LAN
U38
PCIE interface
PM
Transceiver Interface
GPIO & other
LED & EEPROM
CLOCK
Power
RLT8125
Add >= 16 GND vias to connect the EPAD
HSIP
HSIN
REFCLK_P
REFCLK_N
ISOLATEB
LANWAKEB
RSET
POW_EXT_SWR
POW_MODE1
SCANM
GPIO0/PPS_PIN
GPIO1
GPIO8
GPI
NC_0
NC_1
NC_2
HSOP
HSON
PERSTB
CLKREQB
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
LED0/GPIO2
LED1/EESK/SPISCK/GPIO3
LED2/EEDO/SPISO/GPIO6
LED3/EEDI/SDA/SPISI/GPIO7
GPIO4/EECS/SCL
SPICSB/GPIO5
CK25_XTAL
CKXTAL1
CKXTAL2
16,22,24,25 PM_WAKE#
R443 X_0R
LAN_WAKE#
D47 S-LRB520S
26,27 LAN_WAKE#
R445 0R
2.5G_LAN_WAKE#
D57 X_S-LRB520S
14 GPP_TXP1
14 GPP_TXN1
C412 0.1u/16X/4 8125_TXP_C
C413 0.1u/16X/4 8125_TXN_C
16 2_5G_LAN_CLKP
16 2_5G_LAN_CLKN
ISOLATEB_8125
R324 2.49K1%4 RSET
35 POW_EXT_SWR
POW_MODE1
RL19 4.7K/4 SCANM
GPI_8125
8125_RXP_C C422 0.1u/16X/4 GPP_RXP1 14
8125_RXN_C C421 0.1u/16X/4 GPP_RXN1 14
PLTRST_BU2#_2.5GLAN
CLKREQ5
PLTRST_BU2#_2.5GLAN 28
CLKREQ5 16
MDI3_P_R RL26 6.8R/4 MDI3_P
MDI3_N_R RL27 6.8R/4 MDI3_N
MDI2_P_R RL28 6.8R/4 MDI2_P
MDI2_N_R RL29 6.8R/4 MDI2_N
MDI1_P_R RL30 6.8R/4 MDI1_P
MDI1_N_R RL31 6.8R/4 MDI1_N
MDI0_P_R RL33 6.8R/4 MDI0_P
MDI0_N_R RL32 6.8R/4 MDI0_N
LED0_1000#
LED1_LINK#
LED2_2500#
CLK_LANI
CLK_LANO
YL1 25MHZ18p
C394 27p50N4
C388 27p50N4
VDD33_8125
VDD25_8125
VDD09_8125
VDD18_8125
3VSB
AVDD33-1
AVDD33-2
AVDD33-3
AVDD33-4
AVDD33-5
DVDD33-1
DVDD33-2
AVDD25-1
AVDD25-2
AVDD25-3
AVDD25-4
AVDD25-5
DVDD25_UPS-1
AVDD09-1
AVDD09-2
AVDD09-3
AVDD09-4
AVDD09-5
DVDD09-1
DVDD09-2
DVDD09-3
DVDD09-4
DVDD09-5
DVDD09-6
EVDD09-1
EVDD09-2
EVDD09-3
DVDD09_UPS-1
CL63 1u6.3X4 DVDD09_UPS
AVDD18-1
AVDD18-2
AVDD18-3
AVDD18-4
AVDD18-5
DVDD18-1
DVDD18-2
DVDD18-3
EVDD18-1
DVDD18_UPS-1
AVDD18_LDO_OUT-1
AVDD18_LDO_OUT-2
AVDD18_LDO_OUT-3
AVDD18_LDO_OUT-4
AVDD18_LDO_OUT-5
AVDD18_LDO_OUT-6
AVDD18_LDO_OUT-7
AVDD18_LDO_OUT-8
AVDD18_LDO_OUT-9
AVDD18_LDO_1 CL28 1u6.3X4
AVDD18_LDO_2 CL25 1u6.3X4
AVDD18_LDO_3 CL24 1u6.3X4
AVDD18_LDO_4 CL23 1u6.3X4
AVDD18_LDO_5 CL22 1u6.3X4
AVDD18_LDO_6 CL30 1u6.3X4
AVDD18_LDO_7 CL47 1u6.3X4
AVDD18_LDO_8 CL49 1u6.3X4
AVDD18_LDO_9 CL34 1u6.3X4
DVDD3318-1
DVDD3318-2
GND-1
GND-2
If POW_MODE1 setting 1.8V
Change pull up to VDD18_8125
Place CL6 CL7 CL8 CL9 CL10 close to AVDD33 pin - 4,12,20,28,84
3.3V; 1.2mA
CPL1
CL14 CL15 CL16 CL17 CL18 10u6.3X6
Place CL11 CL12 close to DVDD33 pin - 34,71
CL48 CL27 0.1u/16X4
Place CL19 CL20 CL21 CL22 CL23 close to AVDD25 pin - 10,14,26,83,86
CL19 CL20 CL33 CL40 CL32 10u6.3X6
Place CL24 CL25 close to DVDD25_UPS pin - 66
CL66 0.1u/16X4
CL68 10u6.3X6
Place CL35 CL36 CL37 CL38 CL39 close to AVDD09 pin - 1,7,17,23,80
CL35 CL36 CL37 CL38 CL39 10u6.3X6
Place CL41 CL42 CL43 CL44 CL45 CL46 close to DVDD09 pin - 33,44,50,51,72,73
CL41 CL42 CL43 CL44 CL45 CL46 2.2u6.3X4
Place CL54 CL55 close to EVDD09 pin - 54
Place CL56 CL57 close to EVDD09 pin - 55
Place CL58 CL59 close to EVDD09 pin - 63
CL54 CL55 CL56 CL57 CL58 CL59
Place CL47 CL48 CL49 CL50 CL51 close to AVDD18 pin - 3,5,19,21,81
CL31 CL21 CL29 CL26 CL51 10u6.3X6
Place CL52 CL53 close to EVDD18 pin - 53
CL62 0.1u/16X4
CL67 10u6.3X6
Place CL60 CL61 CL62 close to DVDD18 pin - 35,52,70
CL60 CL61 CL65 0.1u/16X4
Place CL63 CL64 close to DVDD18_UPS pin - 65
CL52 0.1u/16X4
CL64 10u6.3X6
Place CL65 CL66 close to DVDD3318 pin - 41,46
If POW_MODE1 setting 1.8V
Change pull up to VDD18_8125
CL50 CL53 0.1u/16X4
LAN_USB1B
JFM48U1G-B3R7-4F
RL4 510R/4 LED_ACT
RL7 220R/4 LED1_LINK#_R
LED1_LINK#
YELLOW+
YELLOW-
VCT
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
VDD
GREEN+/ORANGE-
GREEN-/ORANGE+
MDI0_P MDI0_N MDI1_P MDI1_N MDI2_P MDI2_N MDI3_P MDI3_N
DL1 ESD-VPORT0603L
CL8 X_0.1u/16X4
For CNT LED Power
LED2_2500# RL14 220R/4 LED2_2500#_R
LED0_1000# RL15 220R/4 LED0_1000#_R
UL2 X_ESD-AOZ8829-10P
UL1 X_ESD-AOZ8829-10P
UL7 TS2502TN
UL8 TS2502TN
For EMI
close to CNT
LED_ACT CL3 100p50N4
LED1_LINK#_R CL4 100p50N4
LED2_2500#_R CL9 100p50N4
LED0_1000#_R CL10 100p50N4
POW_MODE1
3.3V:ISOLATEB,PERSTB,CLKREQB,LANWAKEB,GPI,GPIO8 is 1.8V
GND :ISOLATEB,PERSTB,CLKREQB,LANWAKEB,GPI,GPIO8 is 3.3V
pls check PCH voltage level
RL21 X_4.7K/4
RL20 4.7K/4 POW_MODE1
pls check the power well of the PCH input CLKREQ# buffer.
if PCH Side have pull up RL12 can be remove
RL16 X_4.7K/4 CLKREQ5
if PCH Side have pull up RL14.RL15 can be remove
RL22 4.7K/4 GPI_8125
RL18 X_4.7K/4 PLTRST_BU2#_2.5GLAN
RL17 4.7K/4 2.5G_LAN_WAKE#
ISOLATEB :S0 to High,S3/S4 to Low
if POW_MODE Set 1.8V, Change pull up to VCC1.8
Don't pull up to VDD18_8125
VCC3 RL24 1K1%4
RL23 15K1%4 ISOLATEB_8125
If POW_MODE1 setting 1.8V
Change pull up to 1.8V Main power
MICRO-STAR INT'L CO.,LTD
MSI
MS-7C35
Size Custom
Document Description
Clock Buffer
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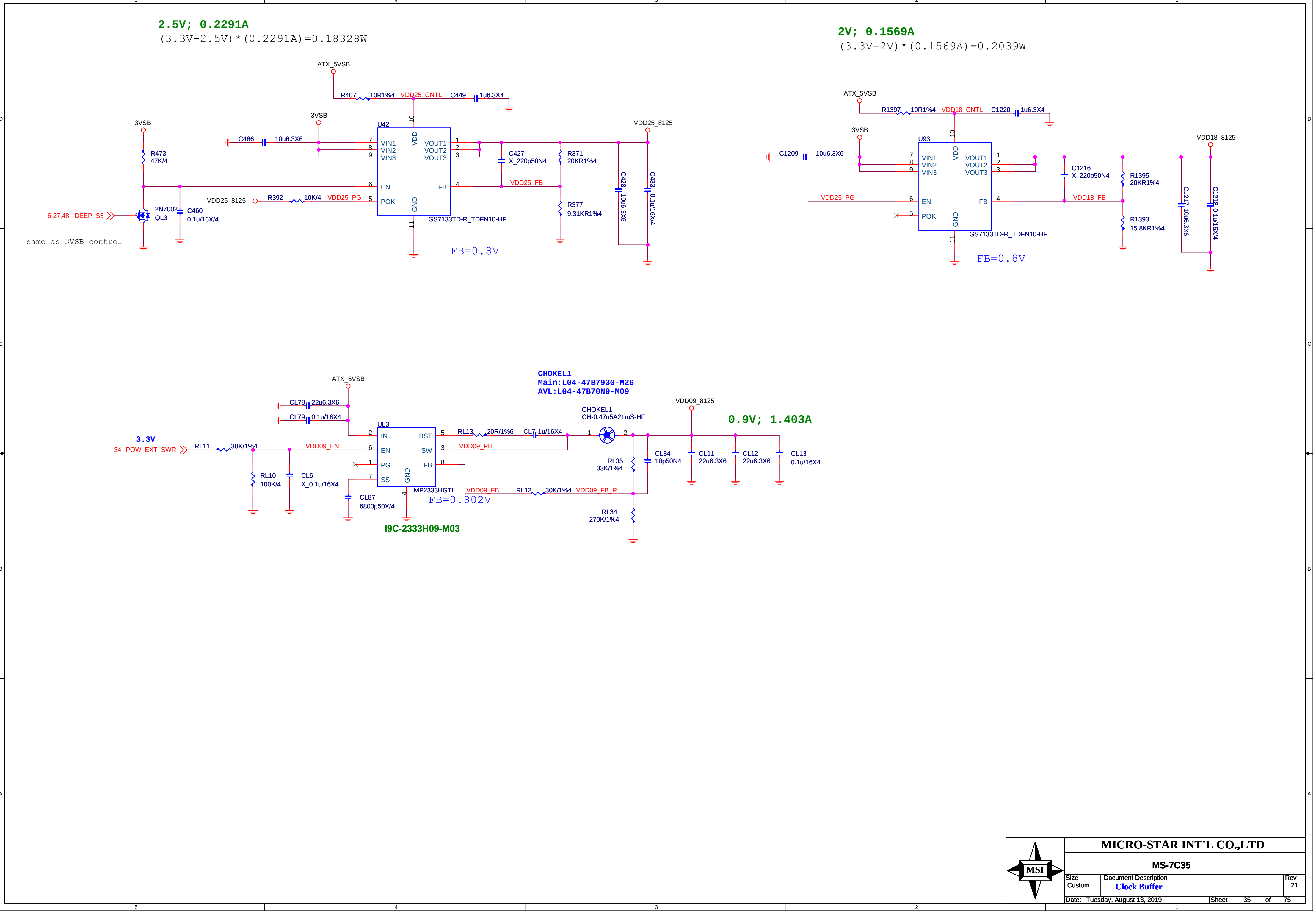
2.5V; 0.2291A
(3.3V-2.5V)*(0.2291A)=0.18328W
ATX_5VSB
R407 10R1%4 VDD25_CNTL C449 1u6.3X4
3VSB
C466 10u6.3X6
U42
VIN1 VIN2 VIN3 VDD VOUT1 VOUT2 VOUT3
EN FB POK GND
GS7133TD-R_TDFN10-HF
VDD25_8125
C427 X_220p50N4
R371 20KR1%4
R377 9.31KR1%4
C428 10u6.3X6
C433 0.1u/16X4
VDD25_FB
R473 47K/4
2N7002 QL3
C460 0.1u/16X/4
VDD25_8125 R392 10K/4 VDD25_PG
6,27,48 DEEP_S5
same as 3VSB control
FB=0.8V
2V; 0.1569A
(3.3V-2V)*(0.1569A)=0.2039W
ATX_5VSB
R1397 10R1%4 VDD18_CNTL C1220 1u6.3X4
3VSB
C1209 10u6.3X6
U93
VIN1 VIN2 VIN3 VDD VOUT1 VOUT2 VOUT3
EN FB POK GND
GS7133TD-R_TDFN10-HF
VDD18_8125
C1216 X_220p50N4
R1395 20KR1%4
R1393 15.8KR1%4
C1217 10u6.3X6
C1218 0.1u/16X4
VDD25_PG
VDD18_FB
FB=0.8V
CHOKEL1
Main:L04-47B7930-M26
AVL:L04-47B70N0-M09
ATX_5VSB
CL78 22u6.3X6
CL79 0.1u/16X4
UL3
IN BST EN SW PG FB SS GND
MP2333HGTL
3.3V
34 POW_EXT_SWR
RL11 30K/1%4
VDD09_EN
RL10 100K/4
CL6 X_0.1u/16X4
CL87 6800p50X/4
RL13 20R/1%6 CL7 1u/16X4
VDD09_PH
CHOKEL1 CH-0.47u5A21mS-HF
VDD09_8125
0.9V; 1.403A
RL35 33K/1%4
CL84 10p50N4
CL11 22u6.3X6
CL12 22u6.3X6
CL13 0.1u/16X4
VDD09_FB RL12 30K/1%4 VDD09_FB_R
FB=0.802V
RL34 270K/1%4
I9C-2333H09-M03
MICRO-STAR INT'L CO.,LTD
MSI
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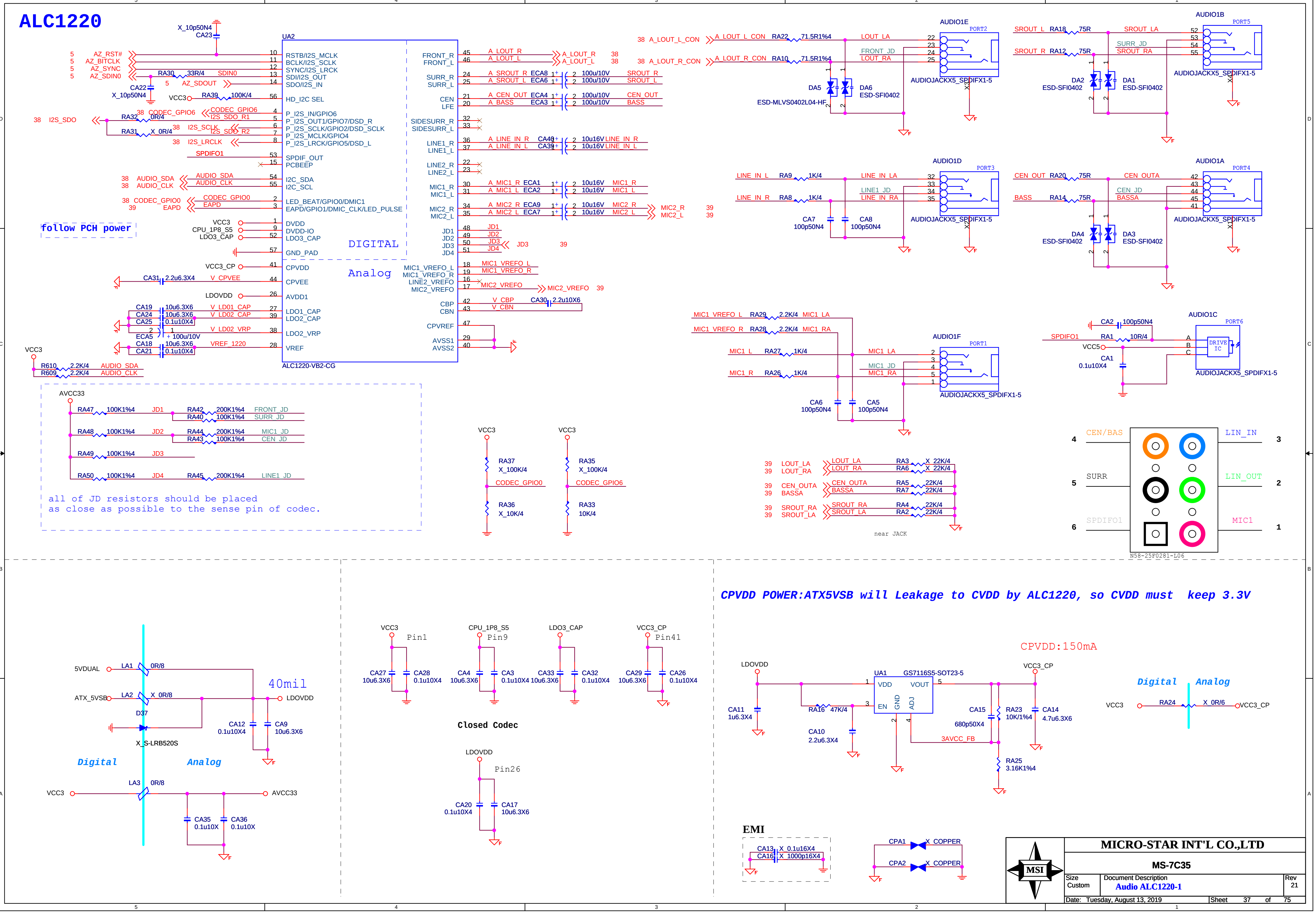
LAN2-- I211AT


ALC1220
UA2
ALC1220-VB2-CG
DIGITAL
Analog
follow PCH power
AUDIO1E
AUDIO1B
AUDIO1D
AUDIO1A
AUDIO1F
AUDIO1C
AUDIOJACKX5_SPDIFX1-5
ESD-MLVS0402L04-HF
ESD-SFI0402
all of JD resistors should be placed
as close as possible to the sense pin of codec.
near JACK
CEN/BAS
LIN_IN
SURR
LIN_OUT
SPDIFO1
MIC1
N58-25F0281-L06
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V
CPVDD:150mA
UA1
GS7116S5-SOT23-5
40mil
Digital
Analog
Closed Codec
Pin1
Pin9
Pin41
Pin26
EMI
MICRO-STAR INT'L CO.,LTD
MS-7C35
Size
Custom
Document Description
Audio ALC1220-1
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21
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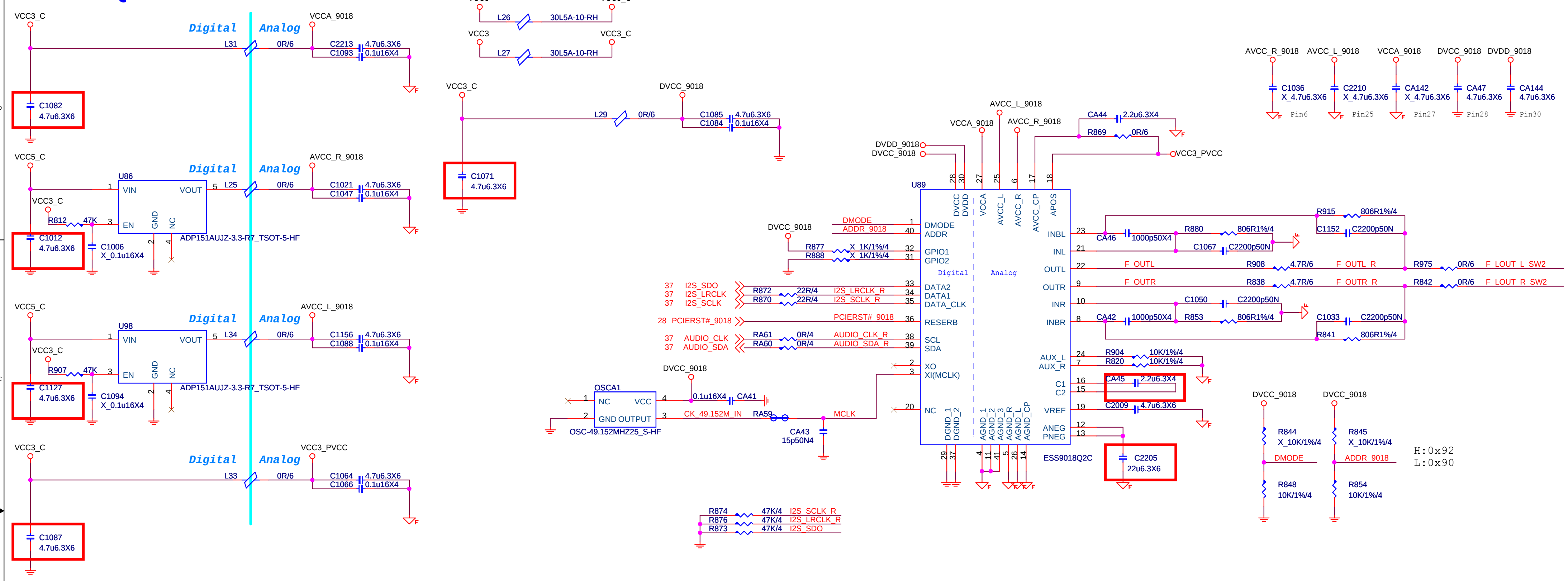
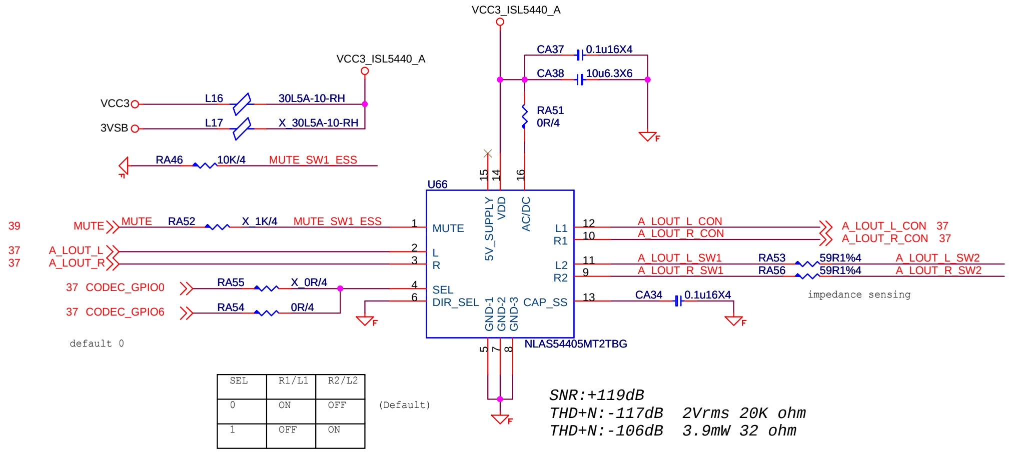
Ess9018Q2C



Analong SW1

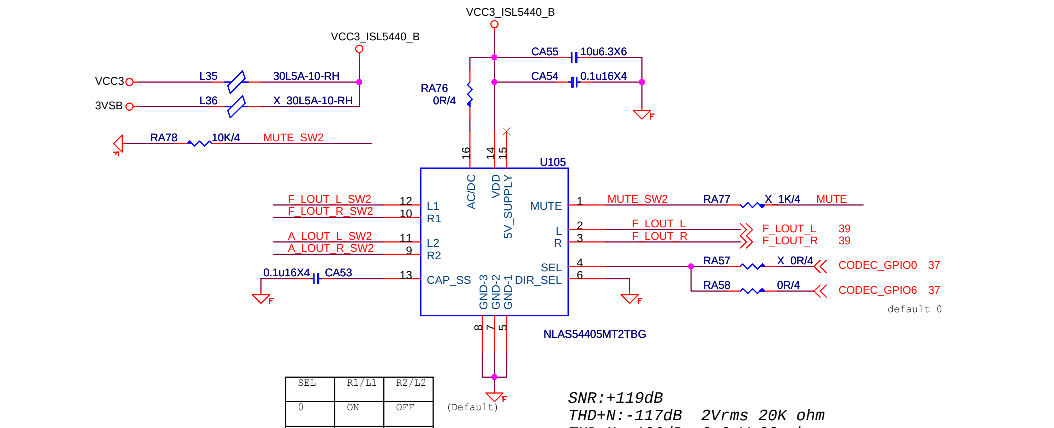


SEL	R1/L1	R2/L2
0	ON	OFF
1	OFF	ON

(Default)

SNR:+119dB
THD+N:-117dB 2Vrms 20K ohm
THD+N:-106dB 3.9mW 32 ohm

Analong SW2



SEL	R1/L1	R2/L2
0	ON	OFF
1	OFF	ON

(Default)

SNR:+119dB
THD+N:-117dB 2Vrms 20K ohm
THD+N:-106dB 3.9mW 32 ohm

MSI

MICRO-STAR INT'L CO.,LTD

MS-7C35

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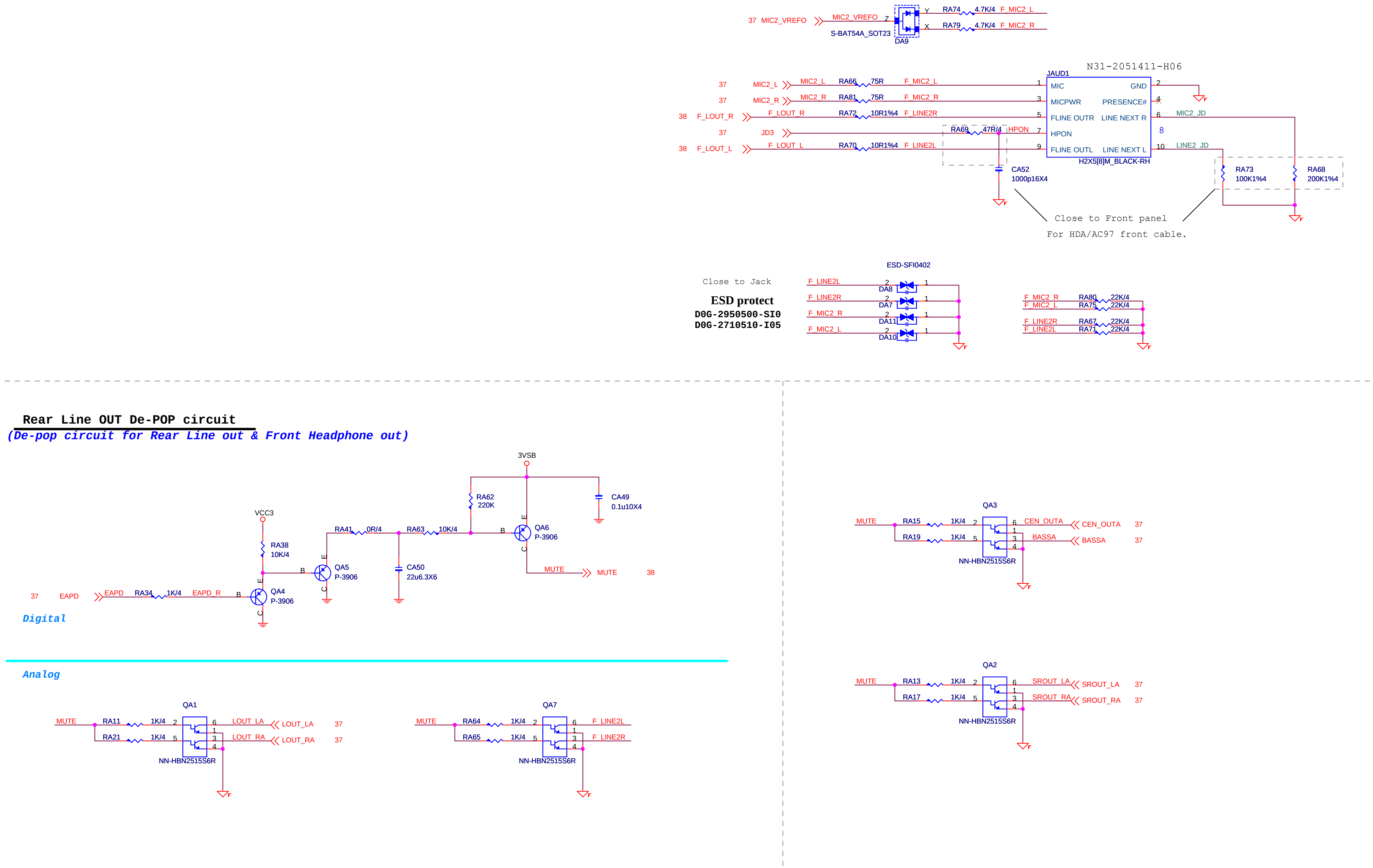

MSI	**MICRO-STAR INT'L CO.,LTD**	
	MS-7C35	
Size: Custom	Document Description: Audio ALC1220-2	Rev: 21
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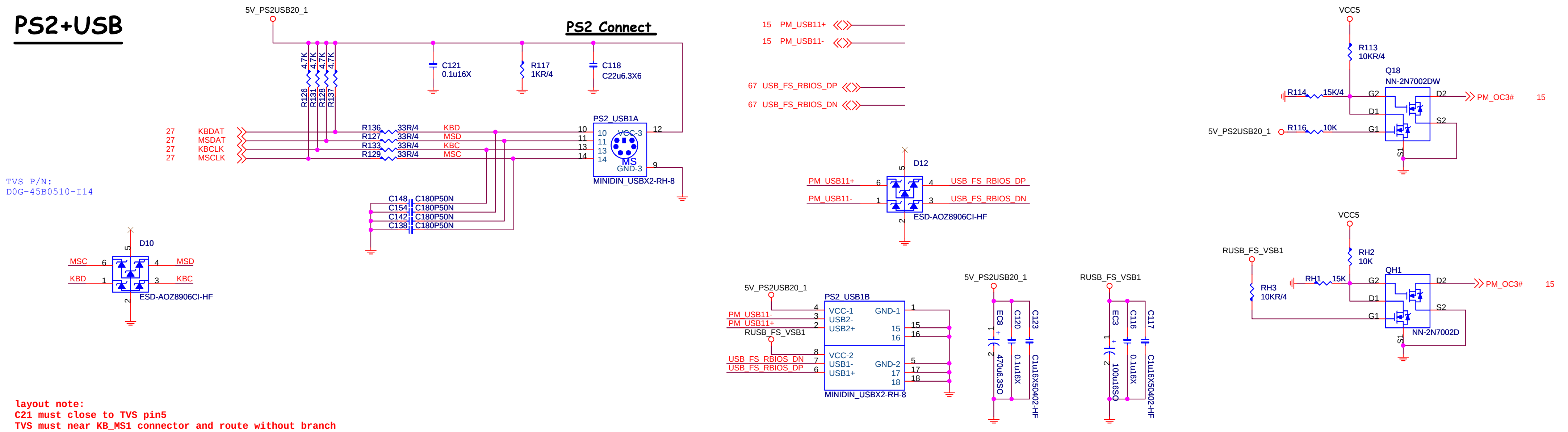
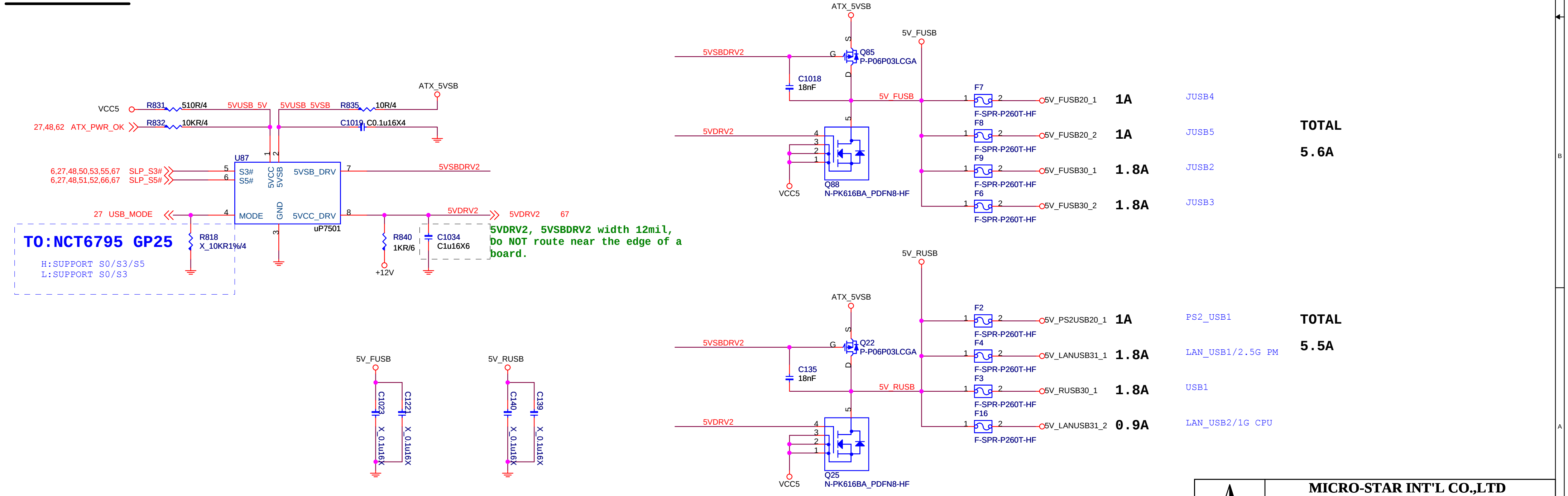
PS2+USB



layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

USB Power



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

MICRO-STAR INT'L CO.,LTD	
MS-7C35	
Size: Custom	Document Description: USB Rear PS2+USB2.0 — Rev 21
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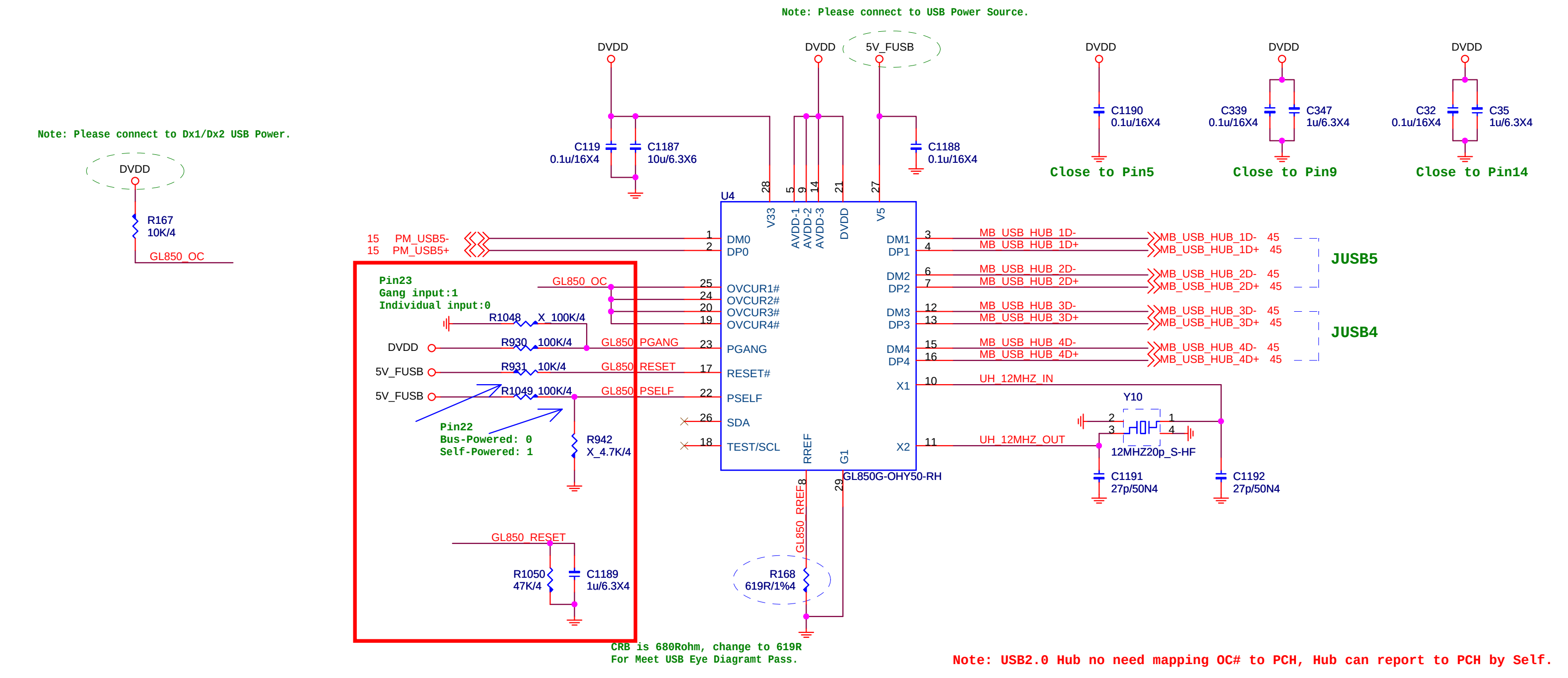
GL850G USB2.0 HUB

5V_FUSB



MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: USB Rear PS2+USB2.0	Rev: 21
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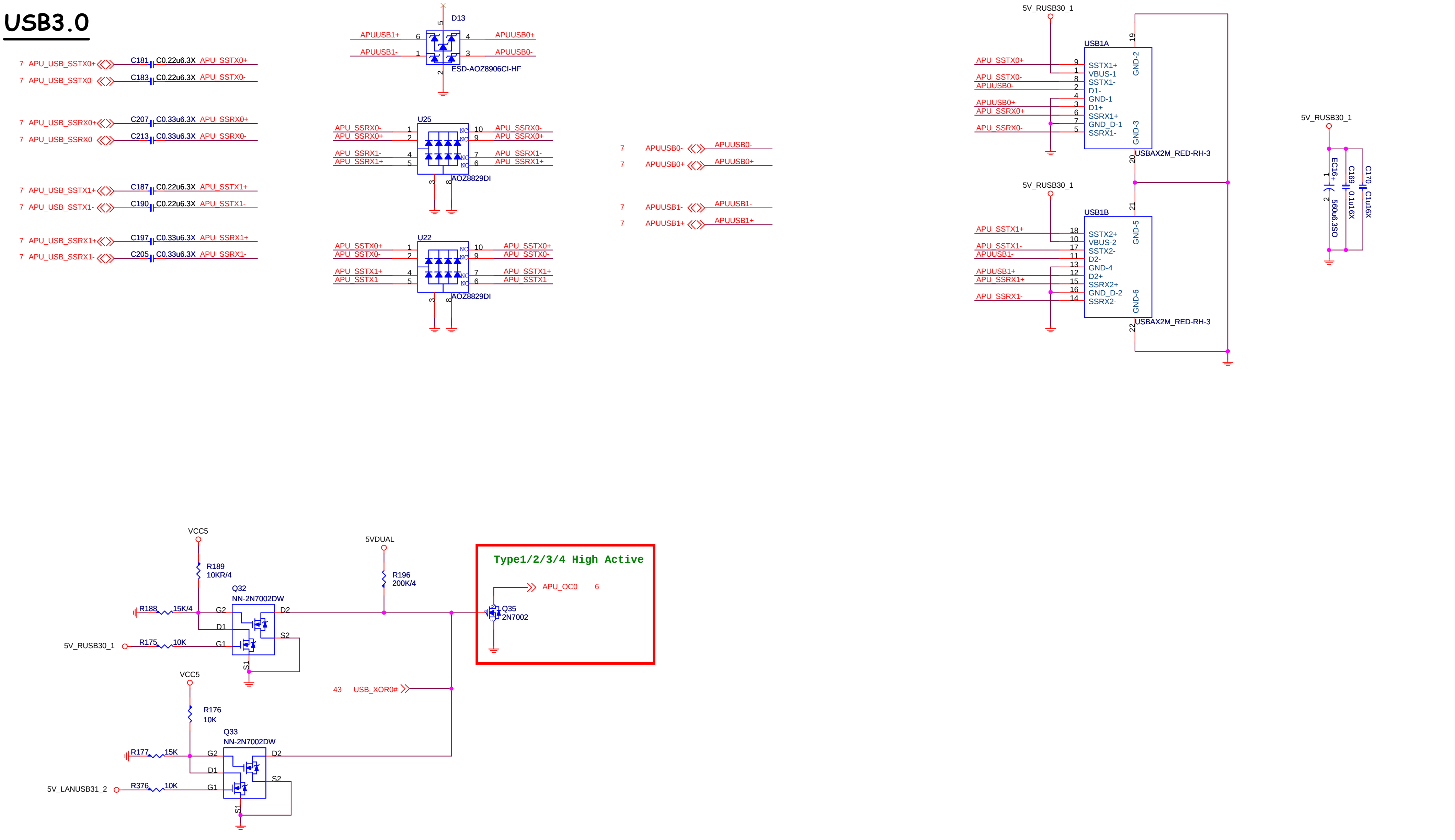
USB3.0



MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7C35		
	Size: Custom	Document Description: USB Rear USB3.0	Rev: 21
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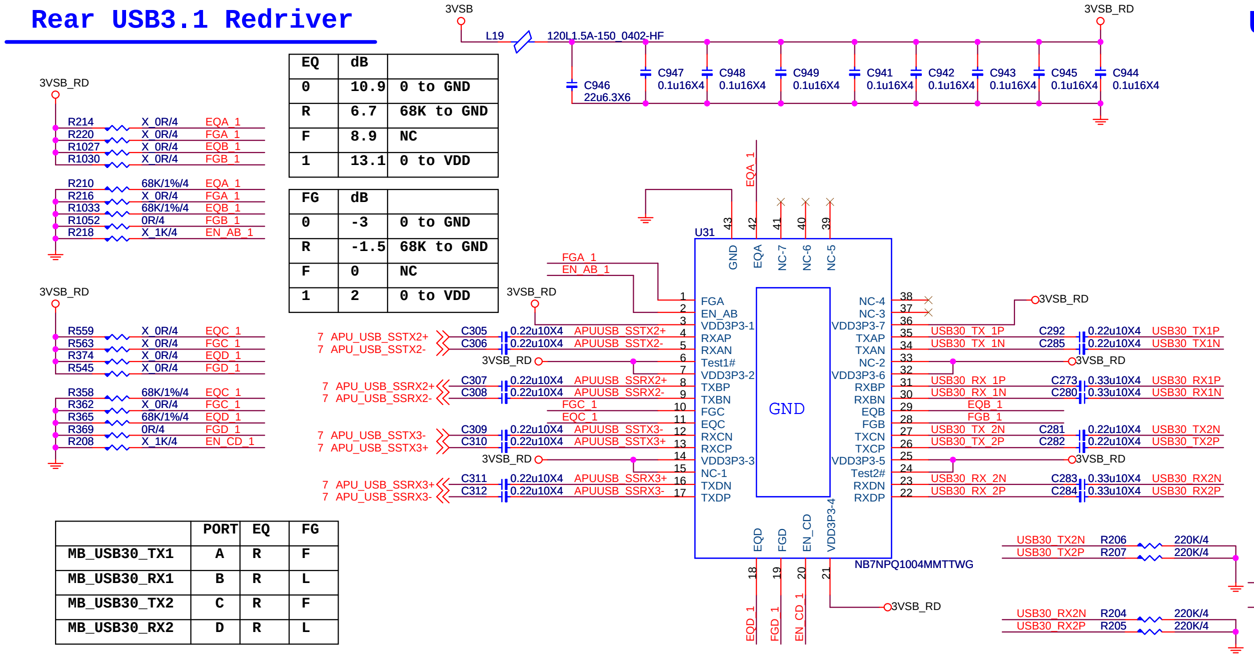
Rear USB3.1 Redriver

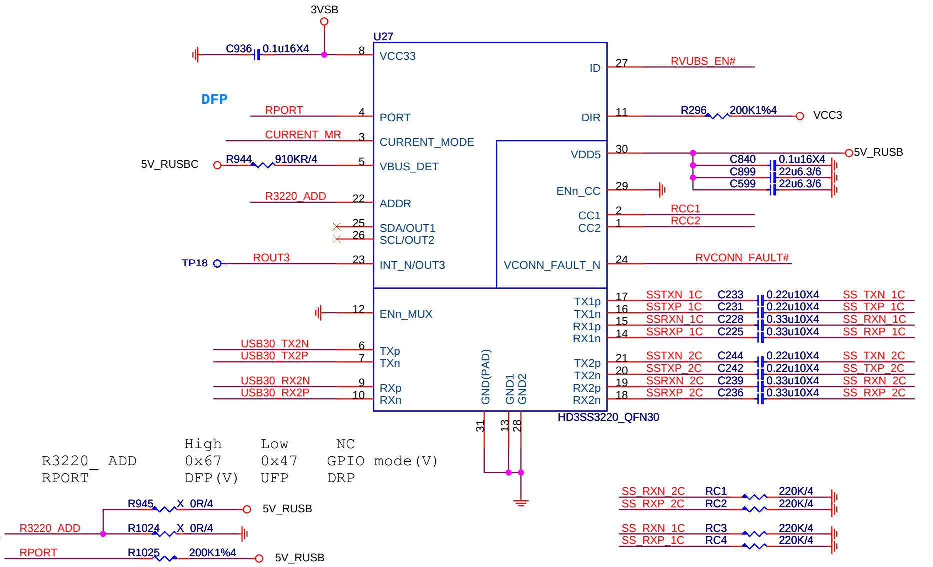
EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD



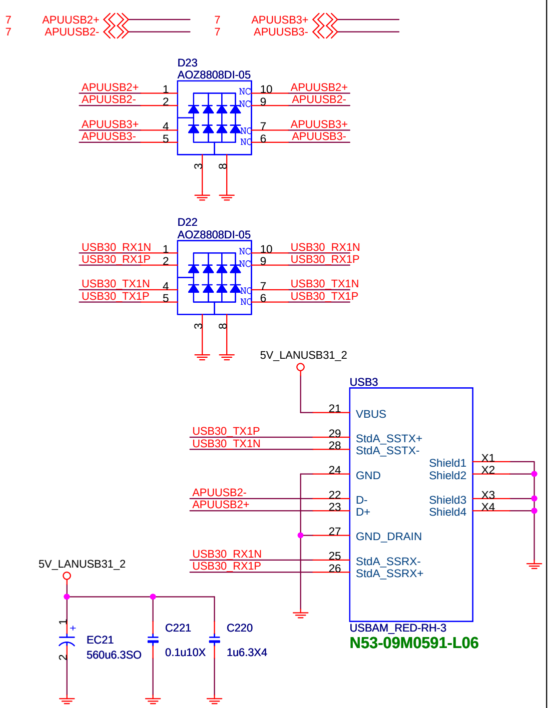
	PORT	EQ	FG
MB_USB30_TX1	A	R	F
MB_USB30_RX1	B	R	L
MB_USB30_TX2	C	R	F
MB_USB30_RX2	D	R	L

USB Type-C MUX with Configuration Channel (CC)



	High	Low	NC
R3220_ ADD	0x67	0x47	GPIO mode(V)
RPORT	DFP(V)	UFP	DRP

TYPE-A

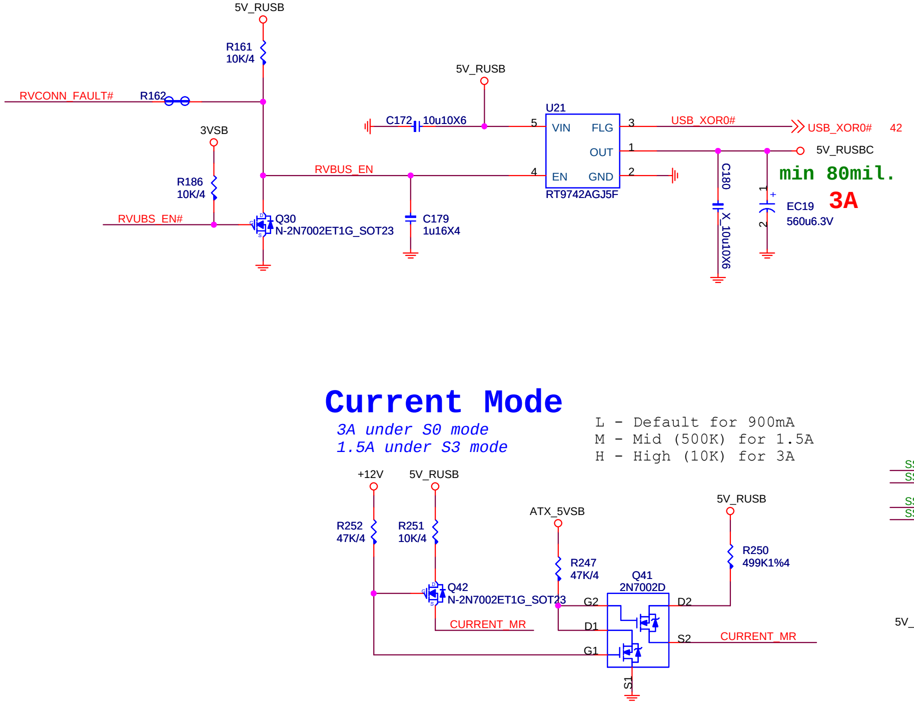


close to Type C Connector

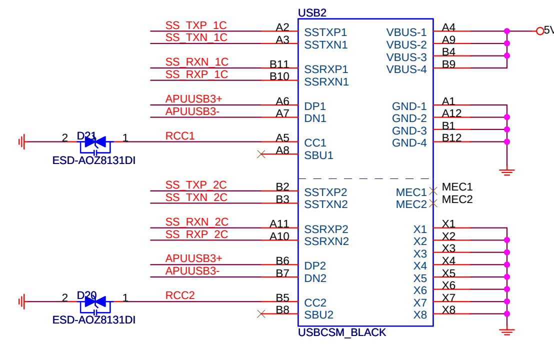
Current Mode

3A under S0 mode
1.5A under S3 mode

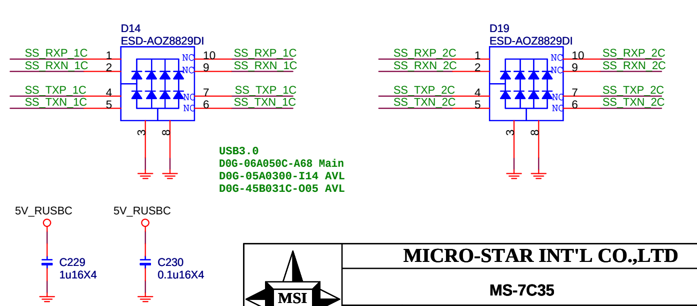
L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A



TYPE-C



ESD Protection



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL

Close to Type C Connector

MICRO-STAR INT'L CO.,LTD		
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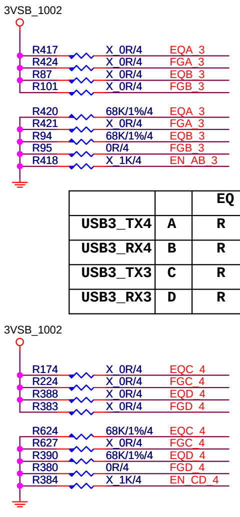
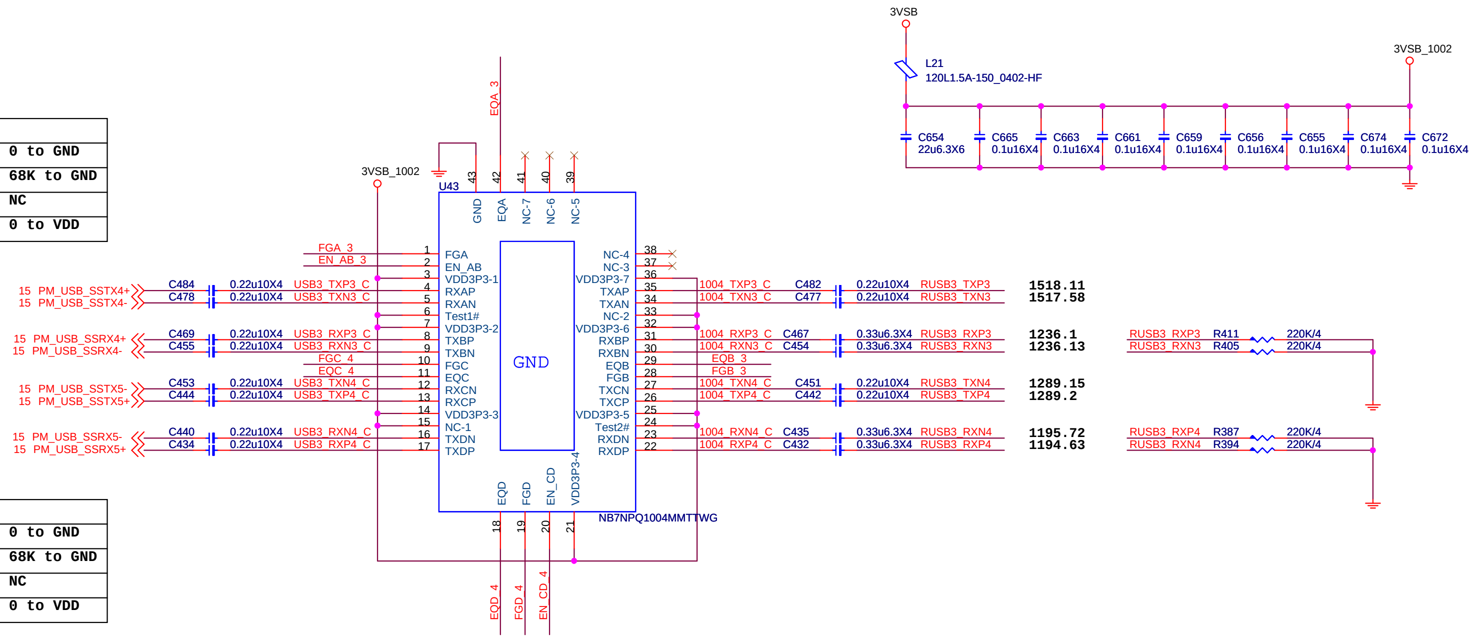
Rear USB3.1 Redriver



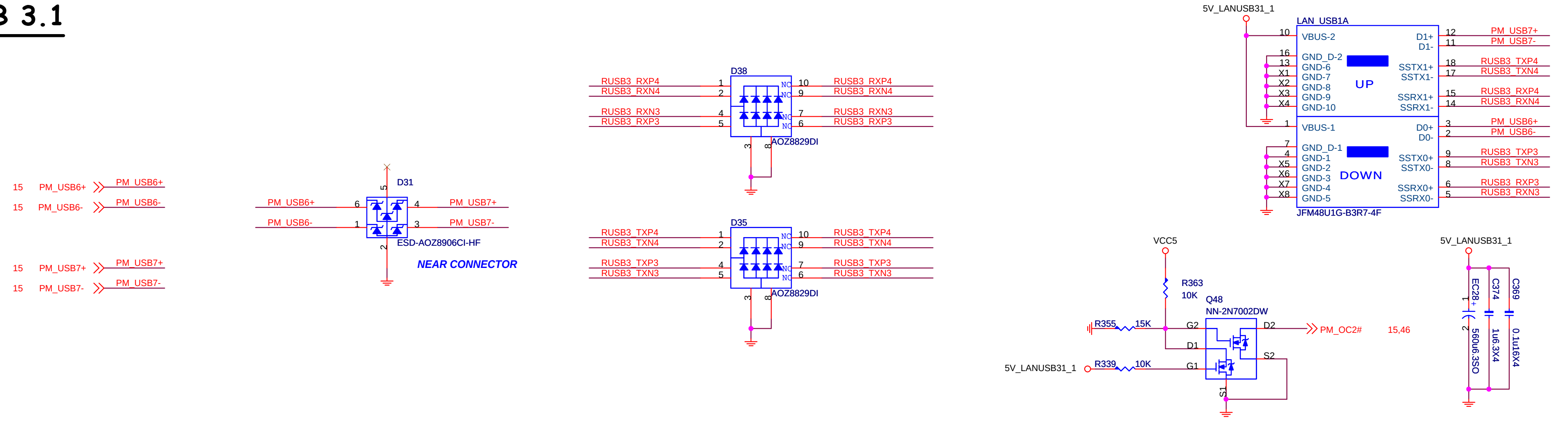
EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD



USB 3.1



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Size: Custom | Document Description: Type A+C | Rev: 21

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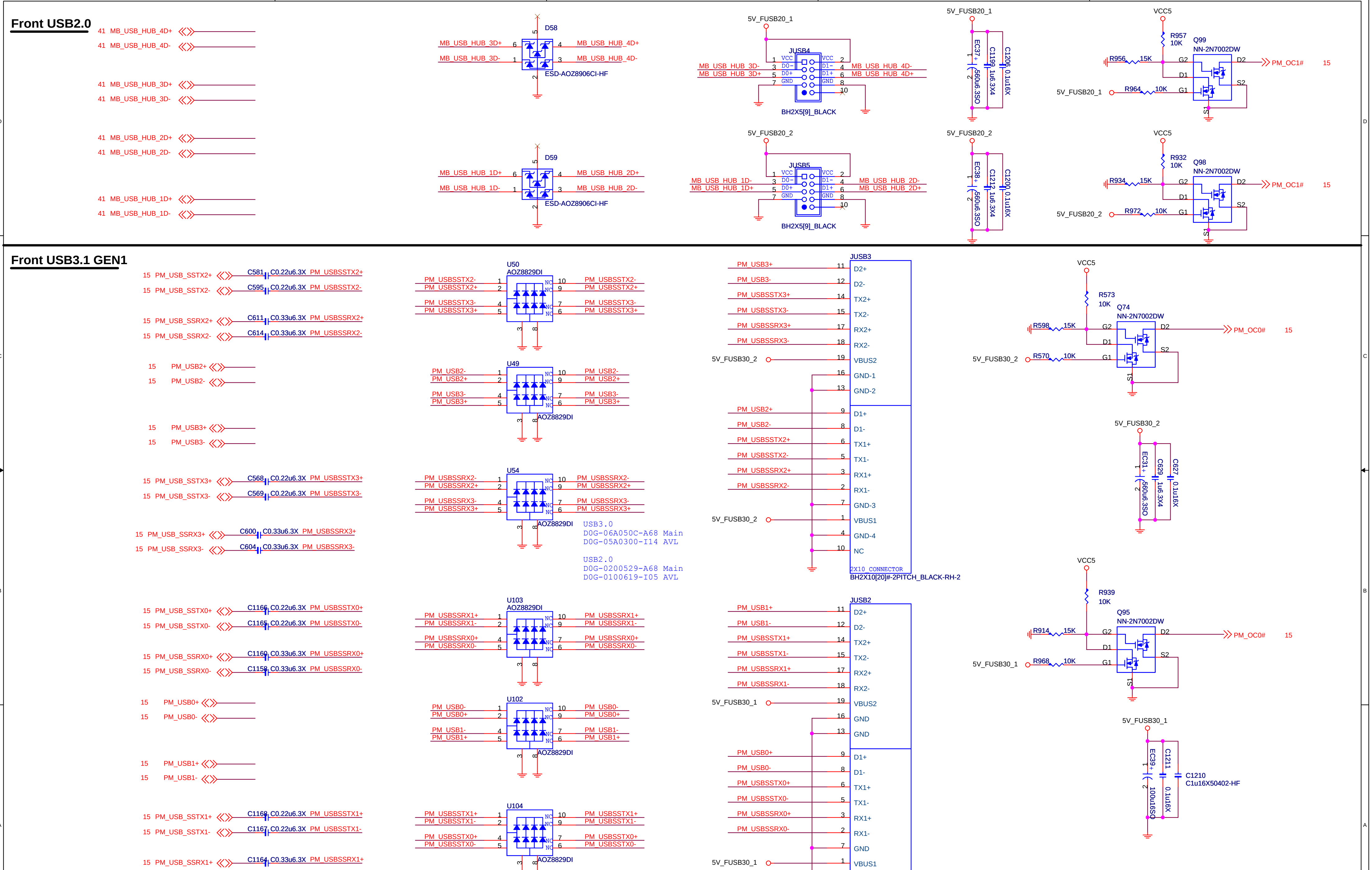

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MS-7C35

Size	Document Description	Rev
Custom	USB Front Side	21

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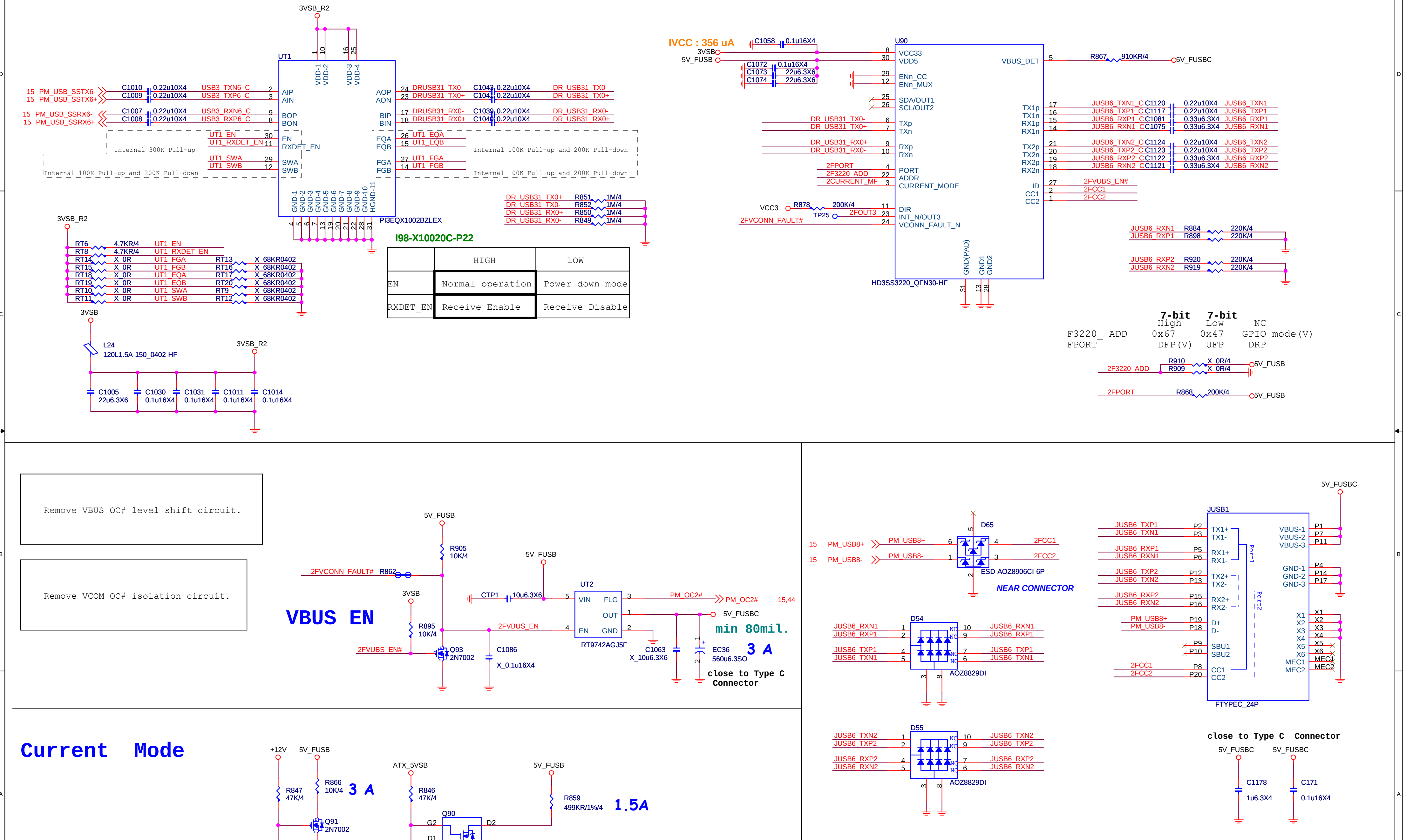
USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable

MICRO-STAR INT'L CO.,LTD

Size	Document Description	Rev
Custom	ASM1562 REAR USB3.1	21

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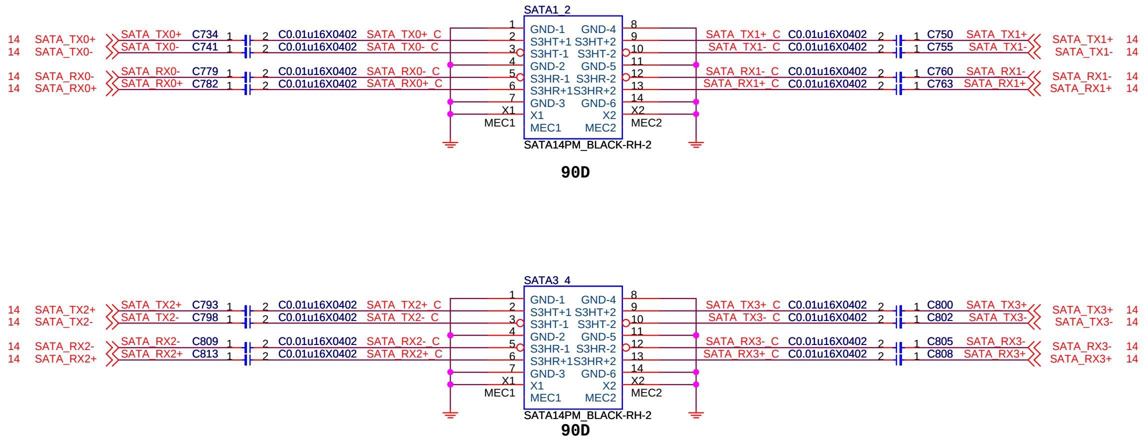
SATA Connector



MICRO-STAR INT'L CO.,LTD			
MS-7C35			
Size: Custom	Document Description: SATA Connector		Rev: 21
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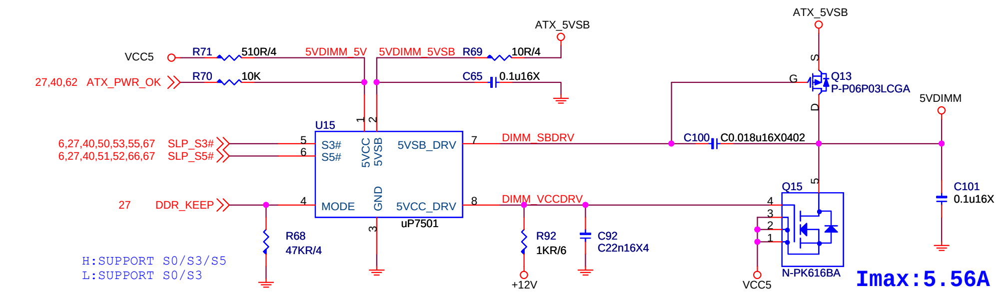
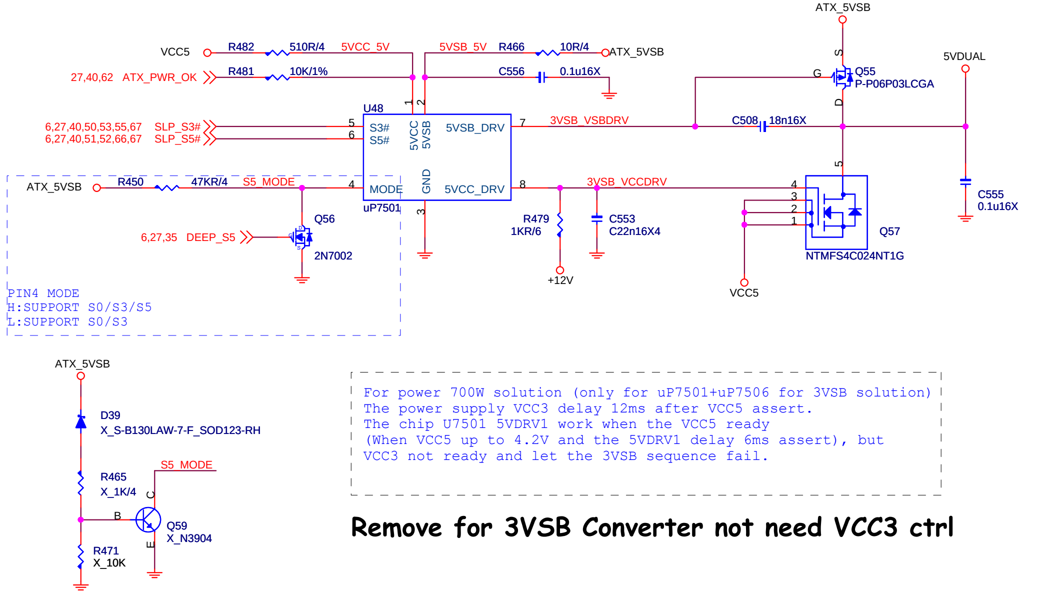
5VDIMM FOR DDR



Imax:5.56A

5VDUAL For 3VSB CPU 1.8V VDDP

Imax:4.5A

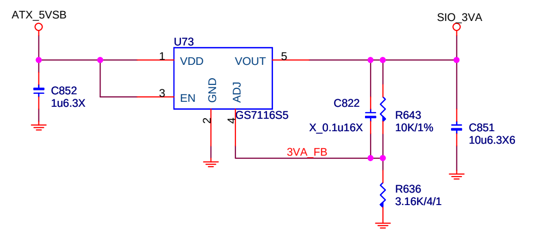


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

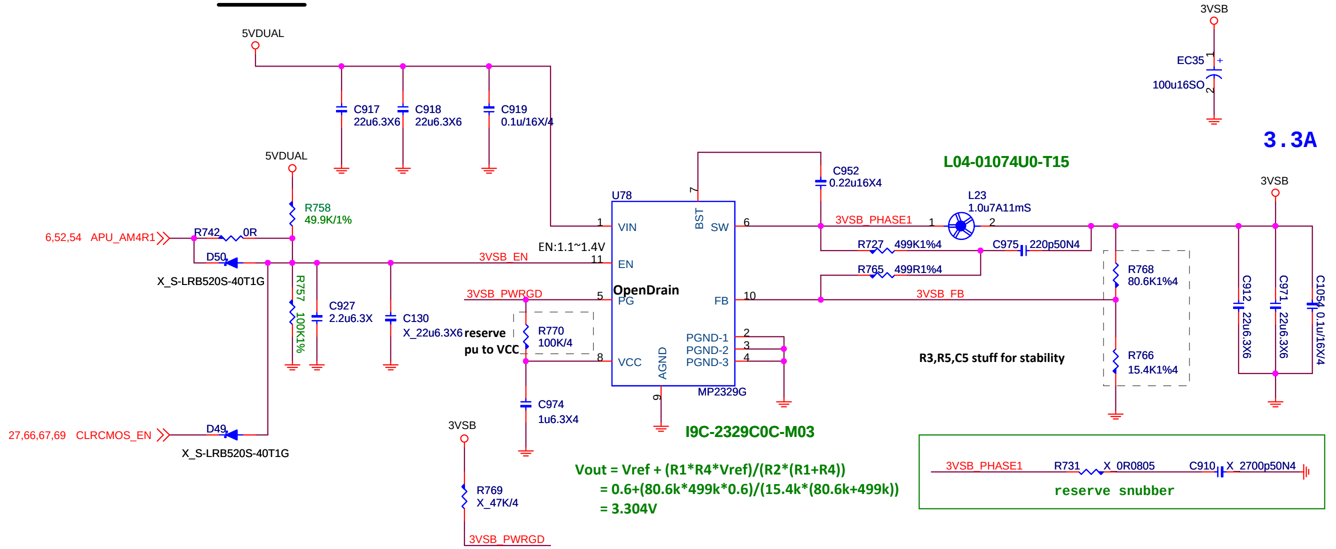
Remove for 3VSB Converter not need VCC3 ctrl

SIO_3VA

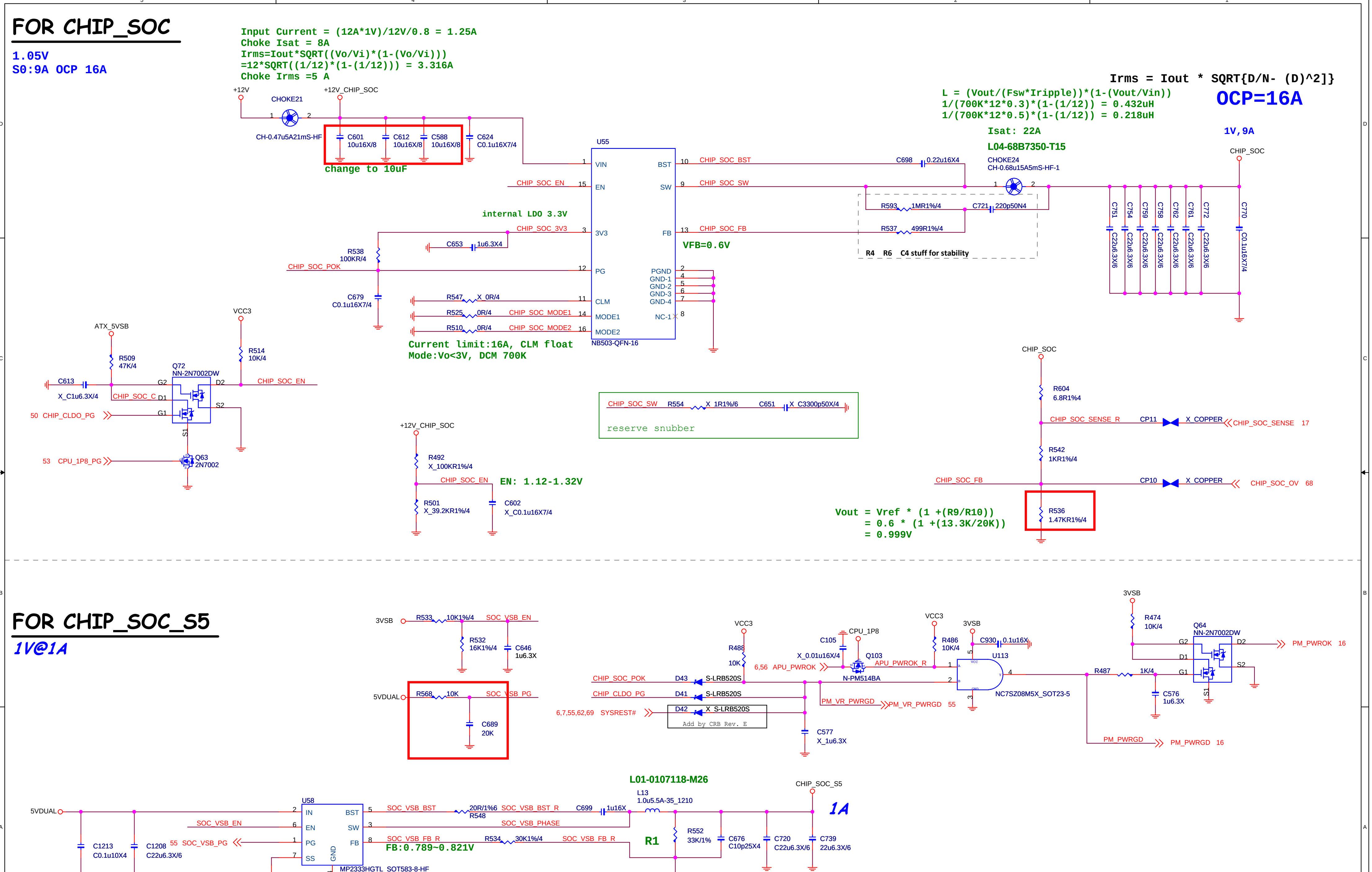
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V



3VSB



Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
= 0.6+(80.6k*499k*0.6)/(15.4k*(80.6k+499k))
= 3.304V



MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: PM-NB681GD-1.05V/GS7133-2.5V	Rev: 21
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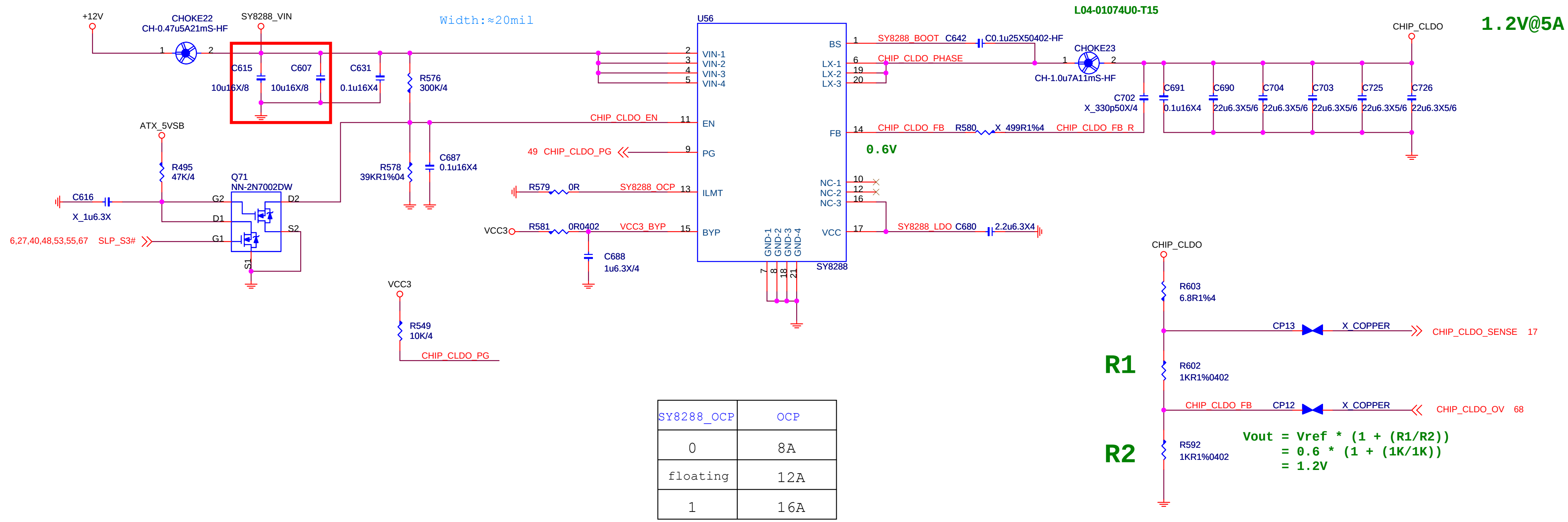
Promontory-2.5V

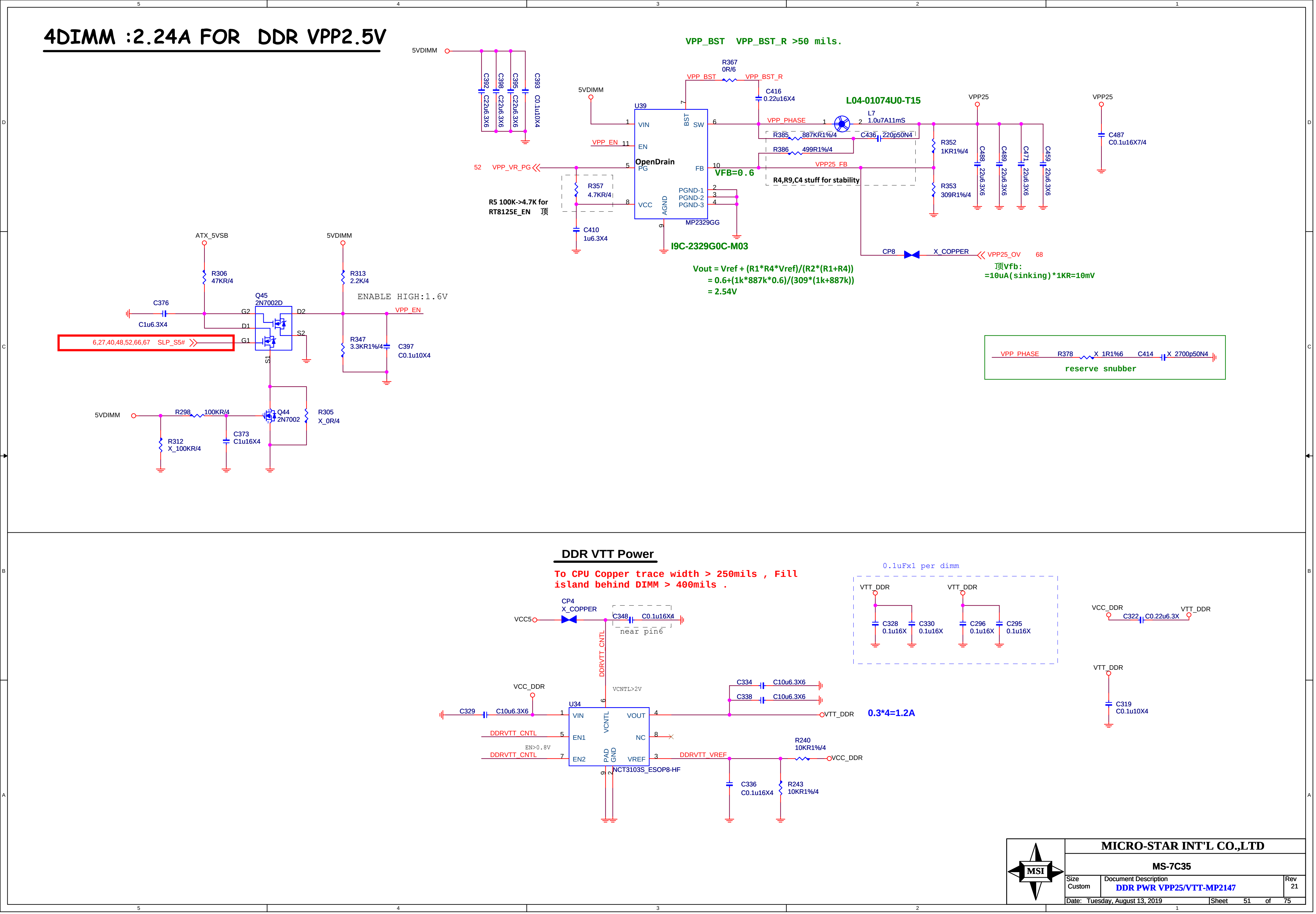
2.5V; 5A OCP 8A

Input Current= (5.5A*1.05V)/12V/0.8=0.625A

Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=5*SQRT((1.2/12*(1-(1.2/12))) = 1.5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A


4DIMM :2.24A FOR DDR VPP2.5V
VPP_BST VPP_BST_R >50 mils.
5VDIMM
C392 C22u6.3X6
C398 C22u6.3X6
C395 C22u6.3X6
C393 C0.1u10X4
R367 0R/6
VPP_BST VPP_BST_R
C416 0.22u16X4
L04-01074U0-T15
L7 1.0u7A11mS
VPP_PHASE
VPP25
C487 C0.1u16X7/4
U39
VIN BST SW
EN
OpenDrain
PG
FB
VCC AGND
PGND-1 PGND-2 PGND-3
MP2329GG
VPP_EN
52 VPP_VR_PG
R357 4.7KR/4
R5 100K->4.7K for RT8125E_EN 顶
C410 1u6.3X4
VFB=0.6
R385 887KR1%/4
C436 220p50N4
R386 499R1%/4
VPP25_FB
R4,R9,C4 stuff for stability
R352 1KR1%/4
R353 309R1%/4
C488 22u6.3X6
C489 22u6.3X6
C471 22u6.3X6
C459 22u6.3X6
I9C-2329G0C-M03
CP8 X_COPPER
VPP25_OV 68
Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
= 0.6+(1k*887k*0.6)/(309*(1k+887k))
= 2.54V
顶Vfb:
=10uA(sinking)*1KR=10mV
ATX_5VSB
R306 47KR/4
C376 C1u6.3X4
Q45 2N7002D
G2 D2 D1 G1 S2 S1
6,27,40,48,52,66,67 SLP_S5#
R313 2.2K/4
ENABLE HIGH:1.6V
VPP_EN
R347 3.3KR1%/4
C397 C0.1u10X4
R298 100KR/4
Q44 2N7002
R305 X_0R/4
R312 X_100KR/4
C373 C1u16X4
VPP_PHASE R378 X_1R1%6 C414 X_2700p50N4
reserve snubber
DDR VTT Power
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .
CP4 X_COPPER
VCC5
C348 C0.1u16X4
near pin6
DDRVTT_CNTL
VCNTL>2V
0.1uFx1 per dimm
VTT_DDR
C328 0.1u16X
C330 0.1u16X
C296 0.1u16X
C295 0.1u16X
VCC_DDR
C322 C0.22u6.3X
C319 C0.1u10X4
C334 C10u6.3X6
C338 C10u6.3X6
C329 C10u6.3X6
U34
VIN VCNTL VOUT
EN1 NC
EN2 PAD GND VREF
NCT3103S_ESOP8-HF
EN>0.8V
DDRVTT_VREF
0.3*4=1.2A
R240 10KR1%/4
C336 C0.1u16X4
R243 10KR1%/4
MICRO-STAR INT'L CO.,LTD
MS-7C35
Size Custom
Document Description
DDR PWR VPP25/VTT-MP2147
Rev 21
Date: Tuesday, August 13, 2019
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DDR4_1.2V 15.5A+9.5A+1.2A=26.2A

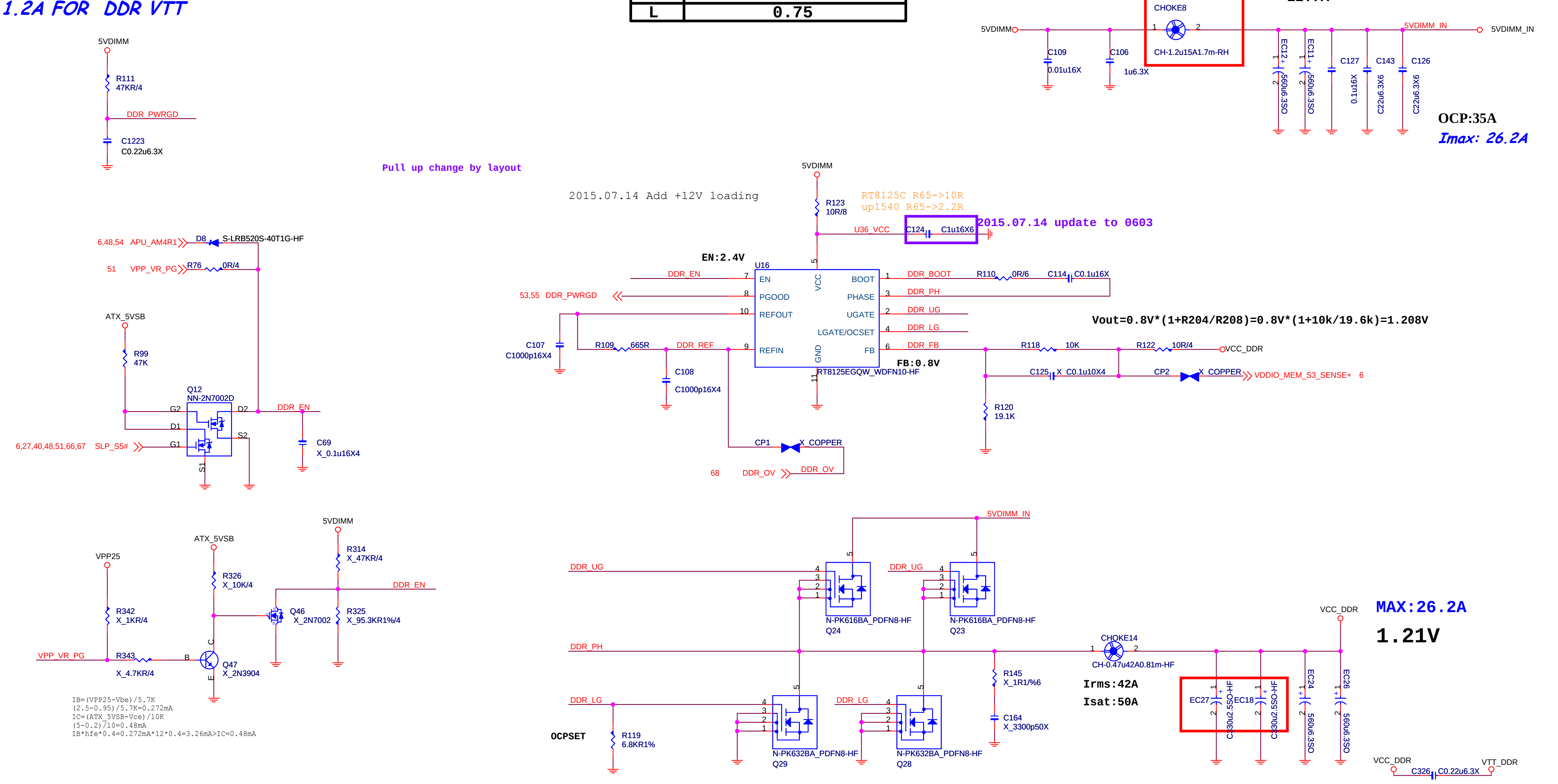
15.5A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

VID	Reference Voltage (V)
H	0.675
L	0.75

Irms = Iout * SQRT{D/N- (D)^2]}
D=Vout/Vin=1.9/5=0.38
N=Phase number=1
=26.2A*SQRT(0.38-0.1444)
=12.7A



OCP target=35A

OCPSET:min 5Kohm

R232=6.8K

OCP	OCP
=(R232*10uA)/Rdson	=(R232*10uA)/Rdson
=R232*10uA)/4m/2	=R232*10uA)/3.3m/2
=34A	=41A

D03-4C02403-005 : 4 mohm

D03-4C02403-005 : 3.3mohm

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
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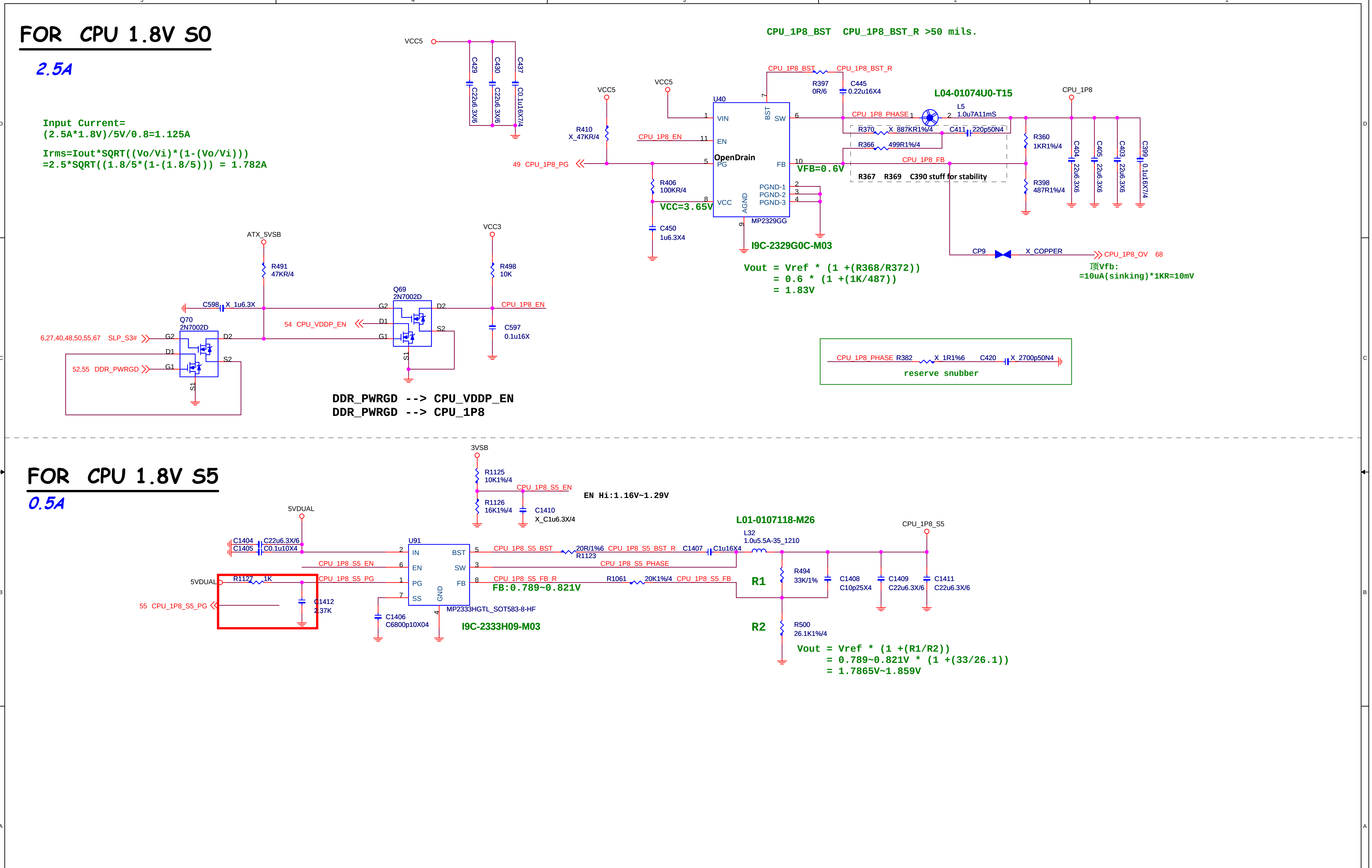

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
Size Custom	Document Description CPU Power 1P8/1P8_S5	Rev 21
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CPU_VDDP_S0

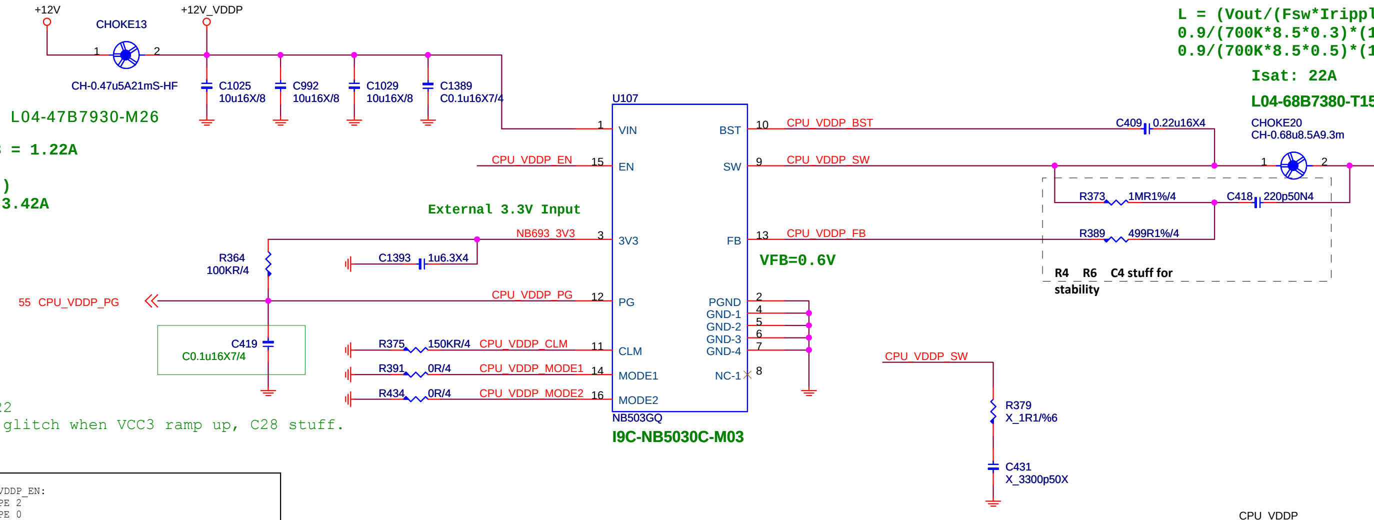
0.9V
S0:8.5A

Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A

L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
Isat: 22A
L04-68B7380-T15

OCP=13A

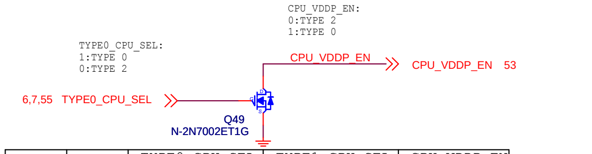
0.9V,8.5A



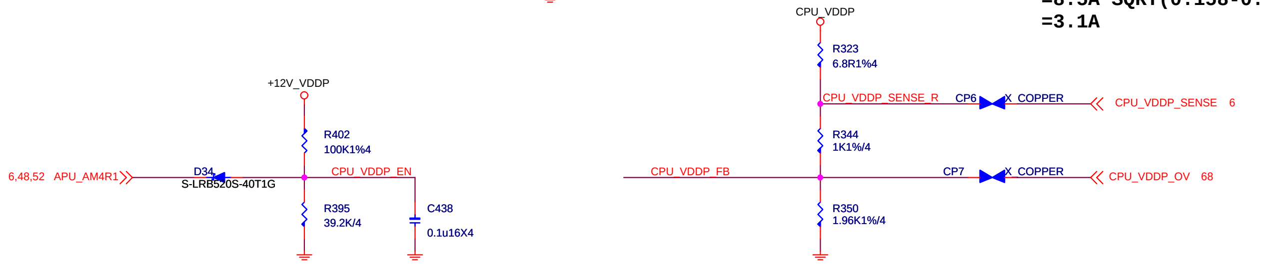
20180822
fix PG glitch when VCC3 ramp up, C28 stuff.

Irms = Iout * SQRT{D/N- (D)^2]}

D=Vout/Vin=1.9/12=0.158
N=Phase number=1
=8.5A*SQRT(0.158-0.025)
=3.1A



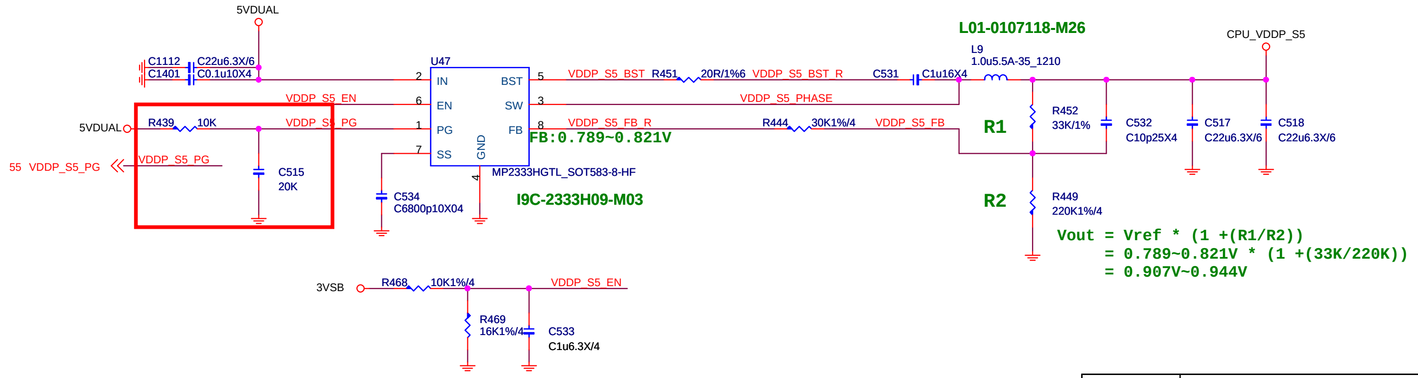
CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0 SPEC no Support	1
NA	X	0	0	0
SR	2	1	0 CPU VDDP NOT SUPPORT TYPE2	1
RV/ZP	3	0	1	1
MTS	4	1	0 CPU VDDP NOT SUPPORT TYPE2	1



CPU_VDDP_S5

0.9V
S0:1A

L01-0107118-M26



Vout = Vref * (1 +(R1/R2))
= 0.789~0.821V * (1 +(33K/220K))
= 0.907V~0.944V

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
Size: Custom	Document Description: CPU Power VDDP MP8712	Rev 21
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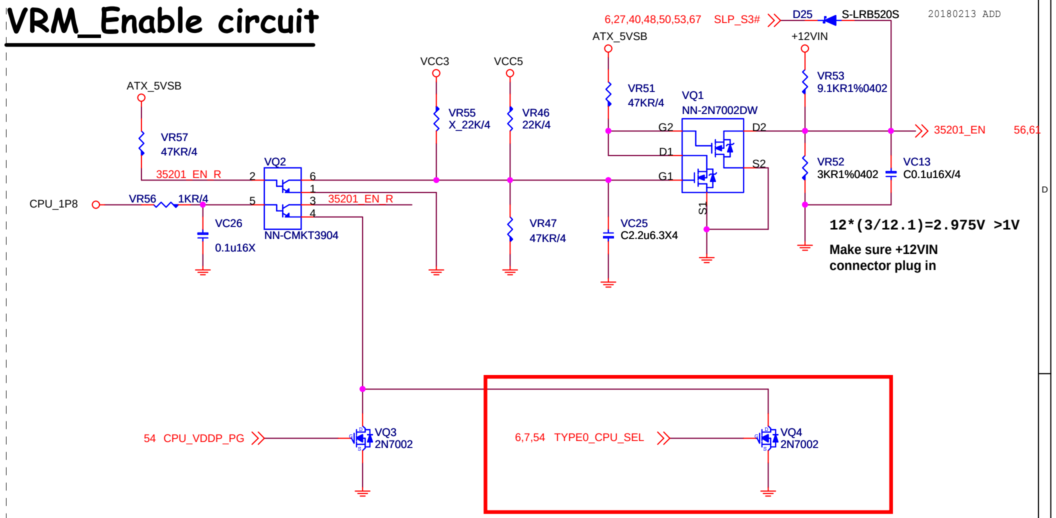
VRM_Enable circuit



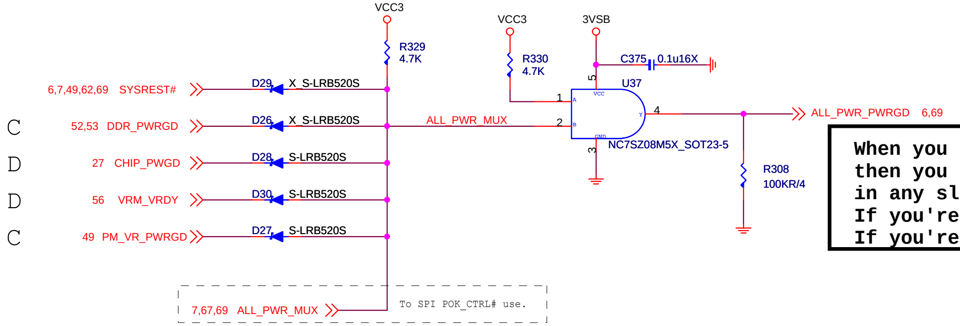
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
~~BR~~	~~0~~	~~0~~	~~1~~
NA		0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1

SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

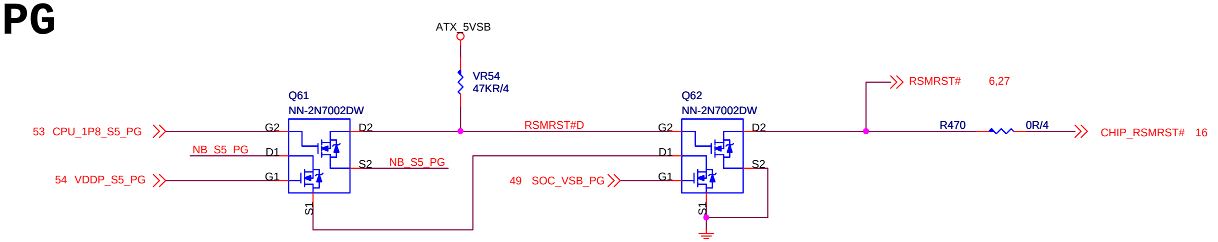
CPU VDDP NOT SUPPORT TYPE4

ALL POWER GOOD MUX



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG
S5 PG



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MS-7C35		
Size: Custom	Document Description: CPU Power Connector/PWRGD	Rev: 21
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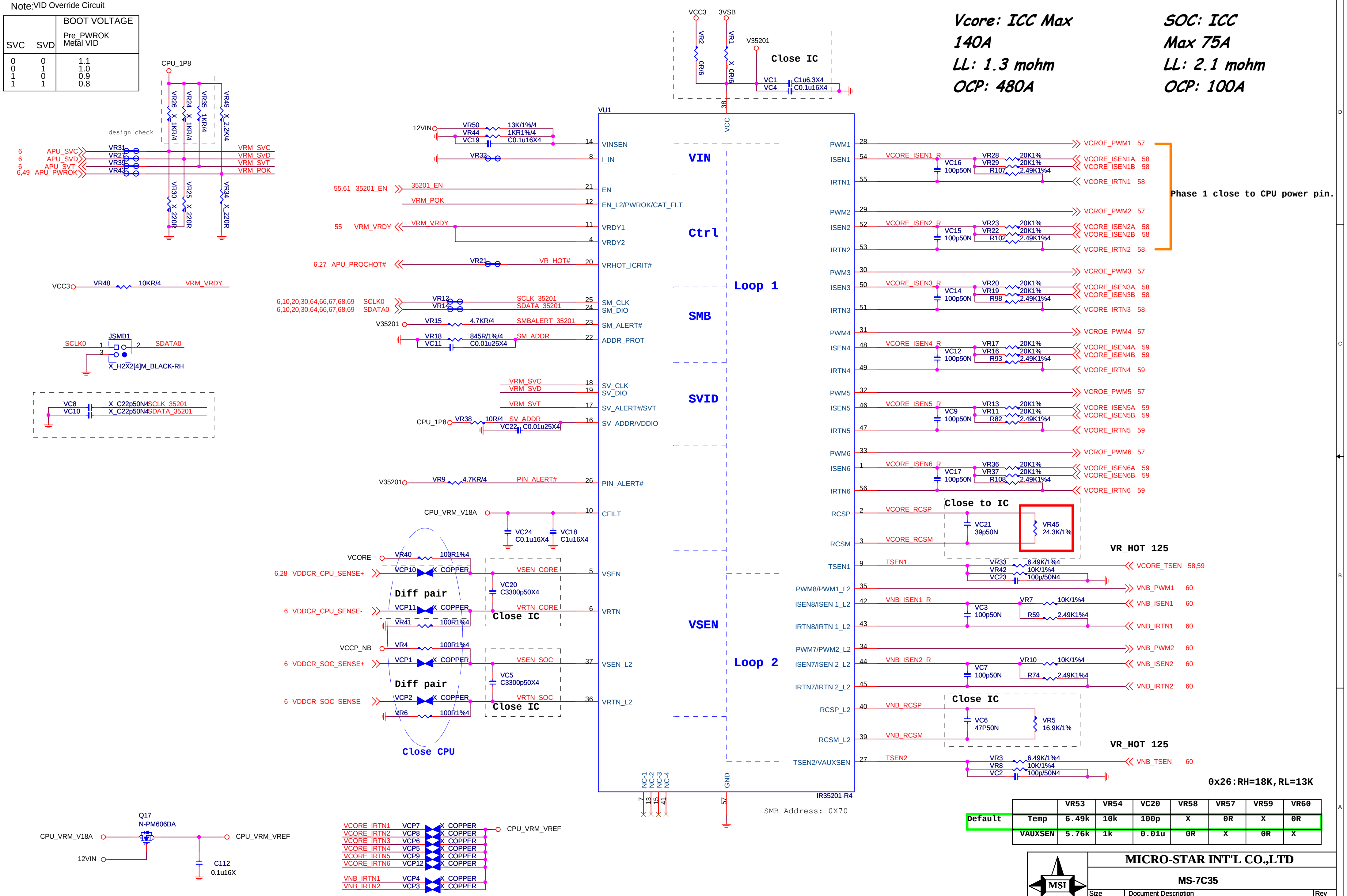
Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vcore: ICC Max
140A
LL: 1.3 mohm
OCP: 480A

SOC: ICC
Max 75A
LL: 2.1 mohm
OCP: 100A



0x26:RH=18K,RL=13K

SMB Address: 0X70

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size: Custom
Document Description: CPU Power IR35201 12 Phase
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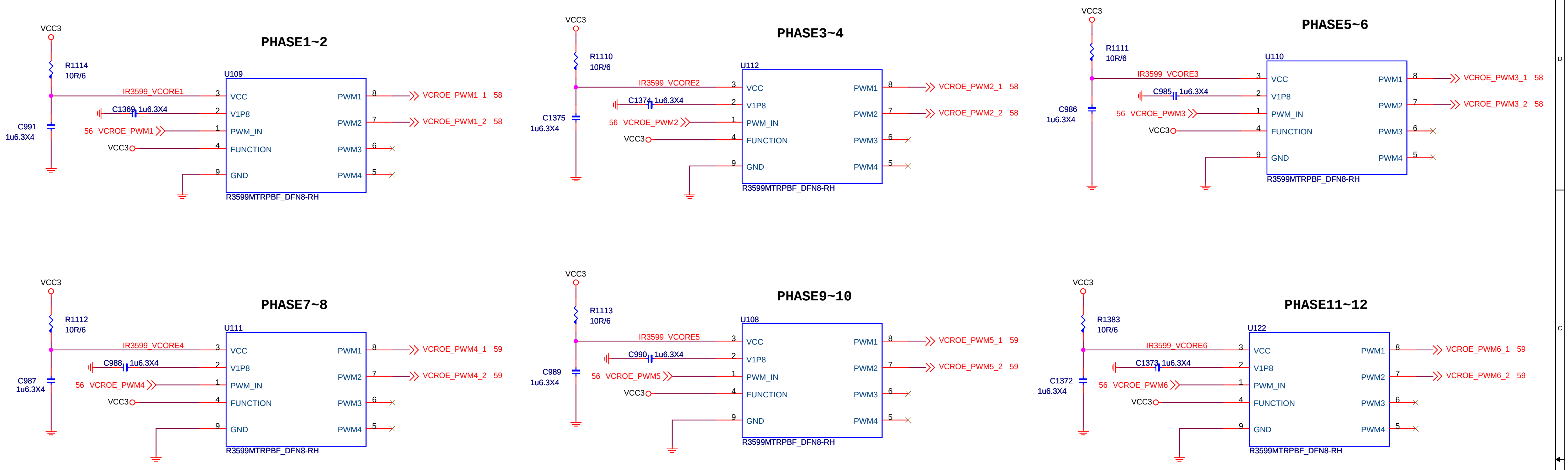
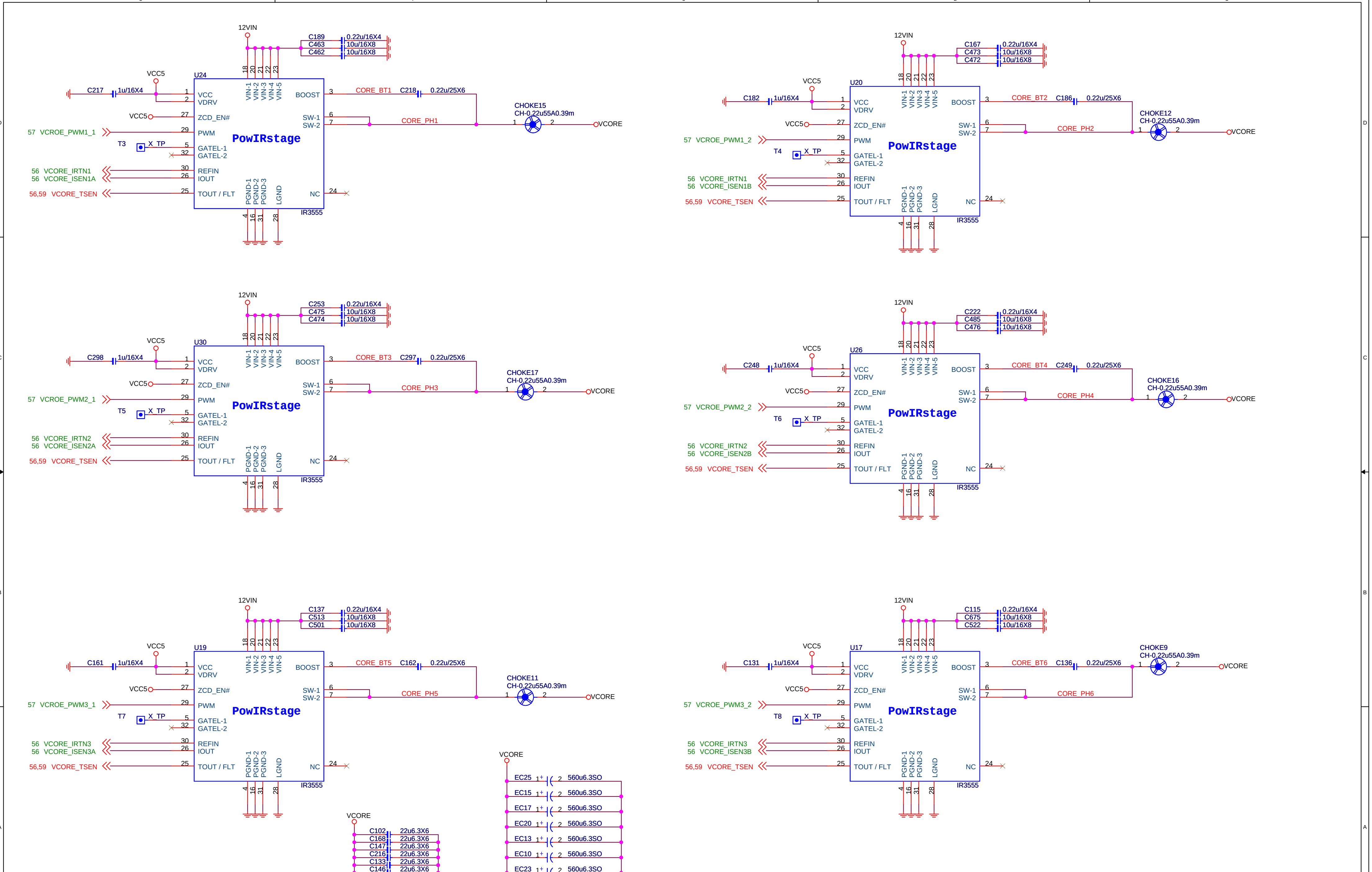
VCORE Double



MICRO-STAR INT'L CO.,LTD	
MS-7C35	
Size: Custom	Document Description: CPU Power IR3598	Rev: 21
Date: Tuesday, August 13, 2019	Sheet 57 of 75



MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	CPU Phase 1-4	21

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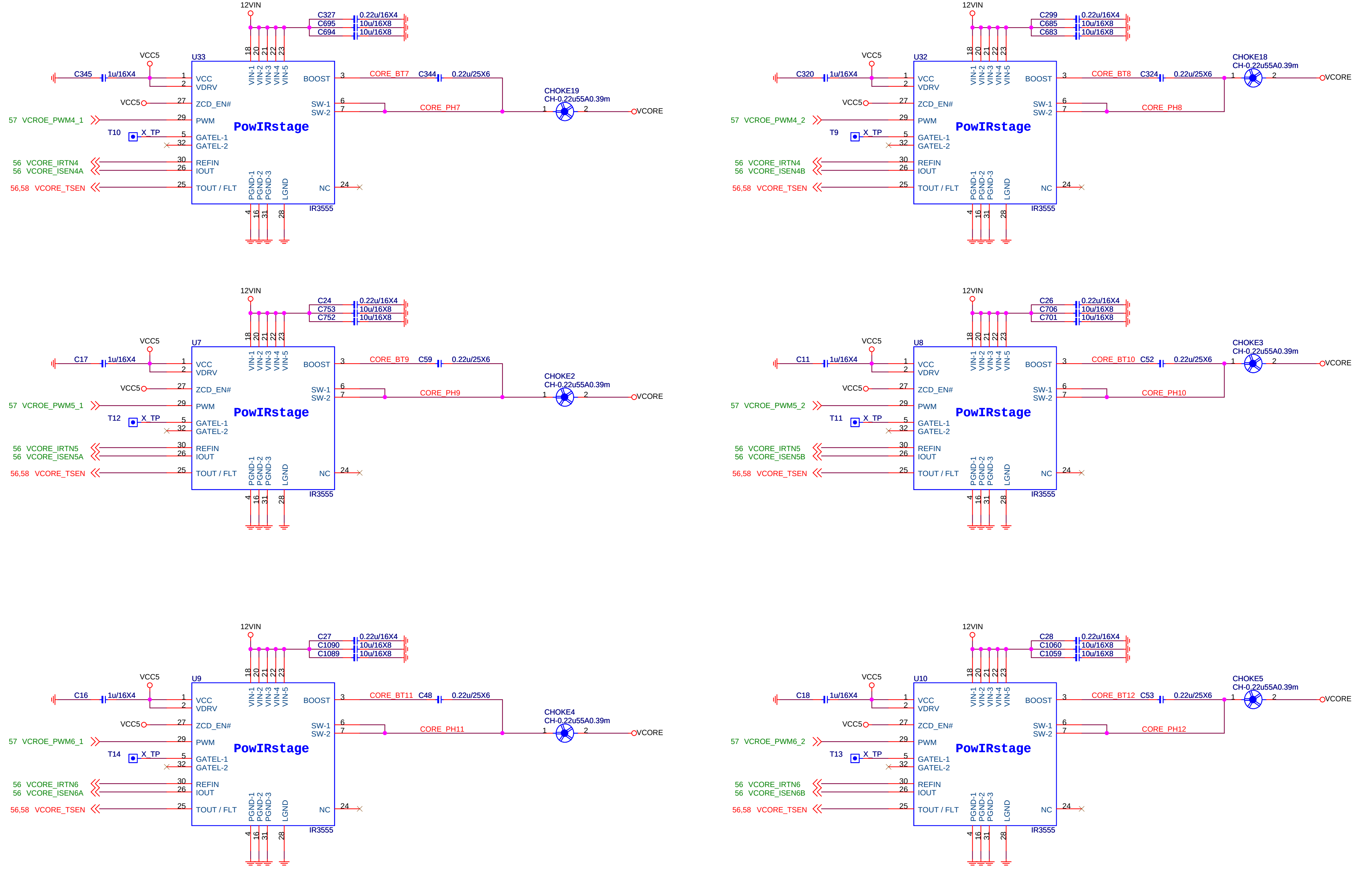

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
Size: Custom	Document Description: CPU Phase 5-8	Rev: 21
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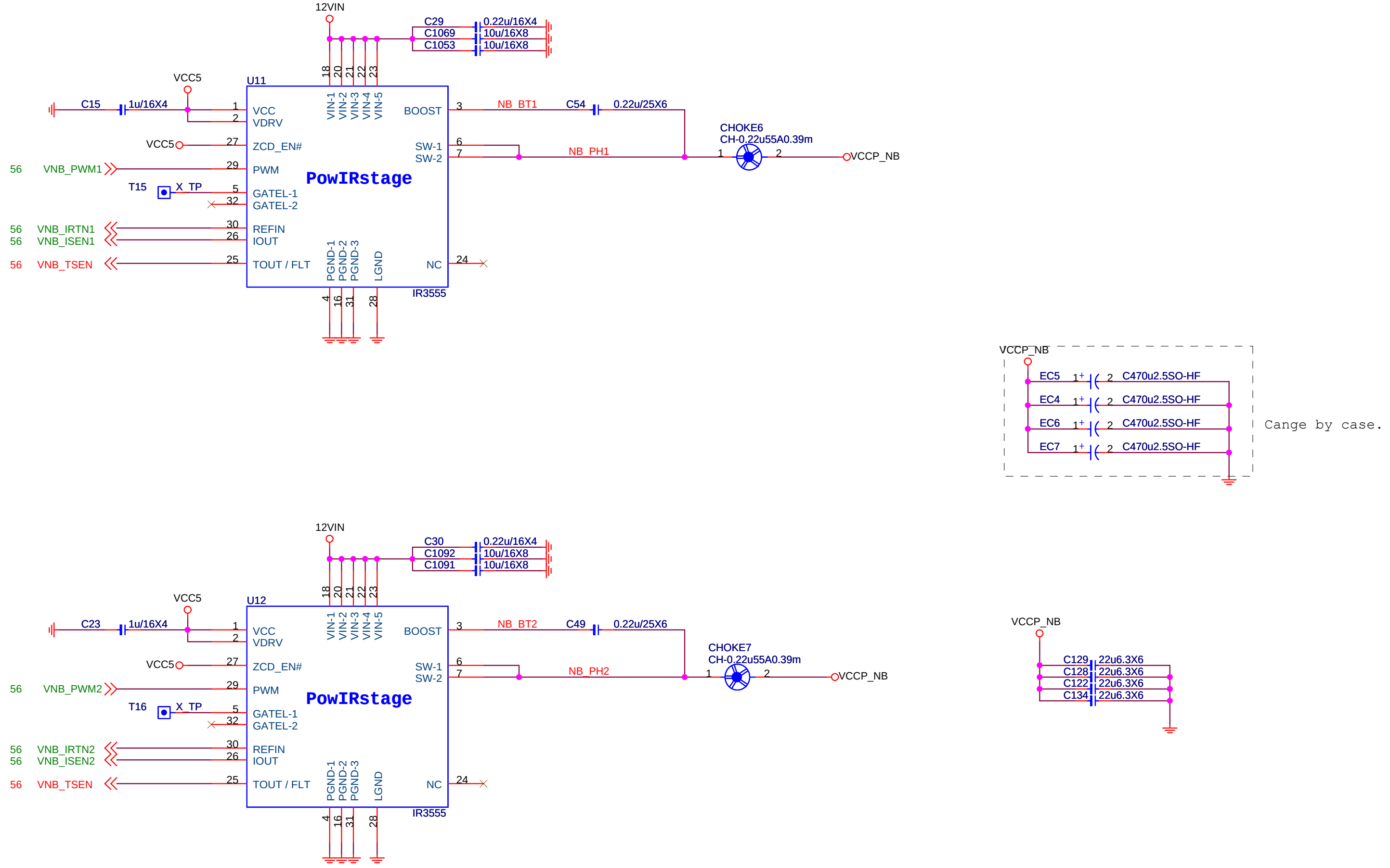

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	CPU Phase 9-12 NB Phase 1-2	21

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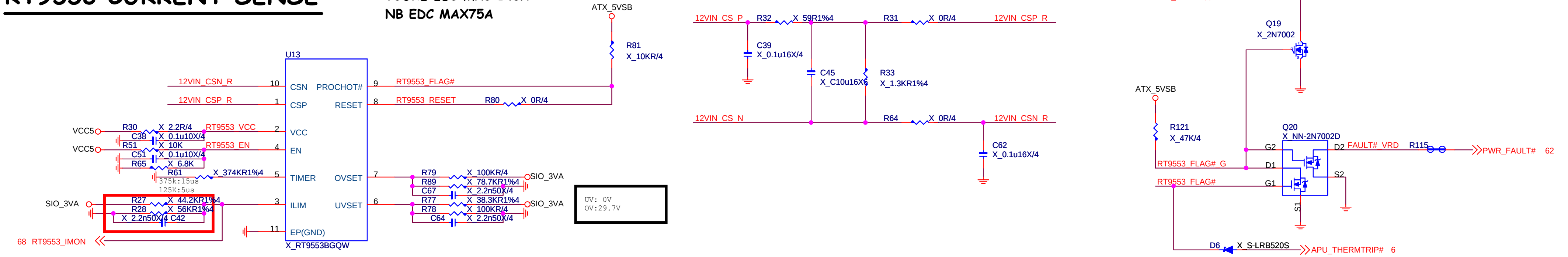
RT9553 CURRENT SENSE

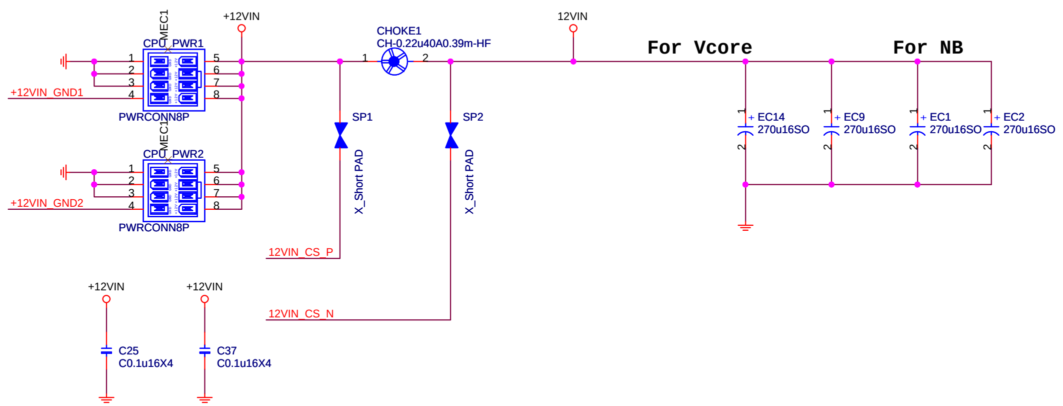
VCORE EDC MAC 140A
NB EDC MAX75A

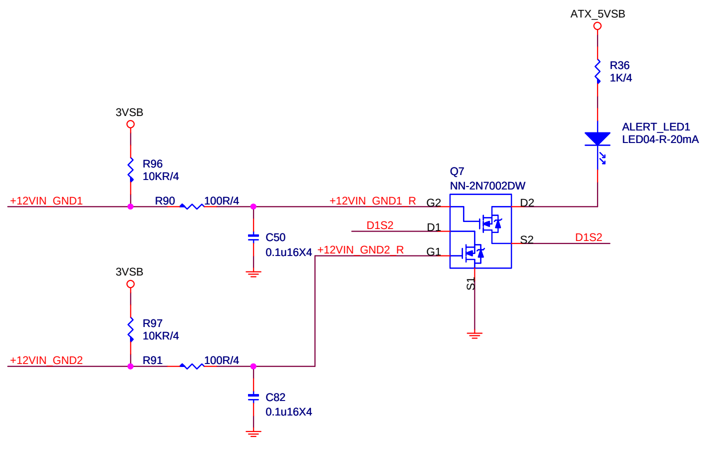


Default:Hi ;Acitve:UP

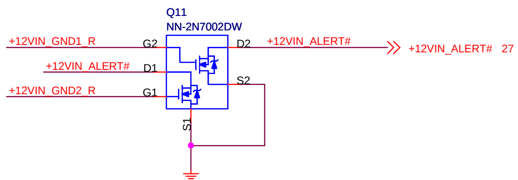
Vcore:480A ,SOC:100A
OCP:56A

CPU POWER CONNECTOR





+12VIN_GND1	+12VIN_GND2	LED	+12VIN_ALERT#(for BIOS show warning message)
0	0	OFF	OFF
0	1	OFF	ON
1	0	OFF	ON
1	1	ON	ON



Close Power Connector

Irms = Iout * SQRT{D/N- (D)^2]}
CORE:
D=Vout/Vin=1.6/12=0.133
N=Phase number=12
=140A*SQRT(0.133/12-0.133*0.133)
=12A

Iout = 80A,Irms=7.68A

NB:
D=Vout/Vin=1.2/12=0.1
N=Phase number=2
=75A*SQRT(0.05-0.01)
=15A

Iout = 50A,Irms=10A

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
Size: Custom	Document Description: RT9553 CURRENT SENSE	Rev: 21
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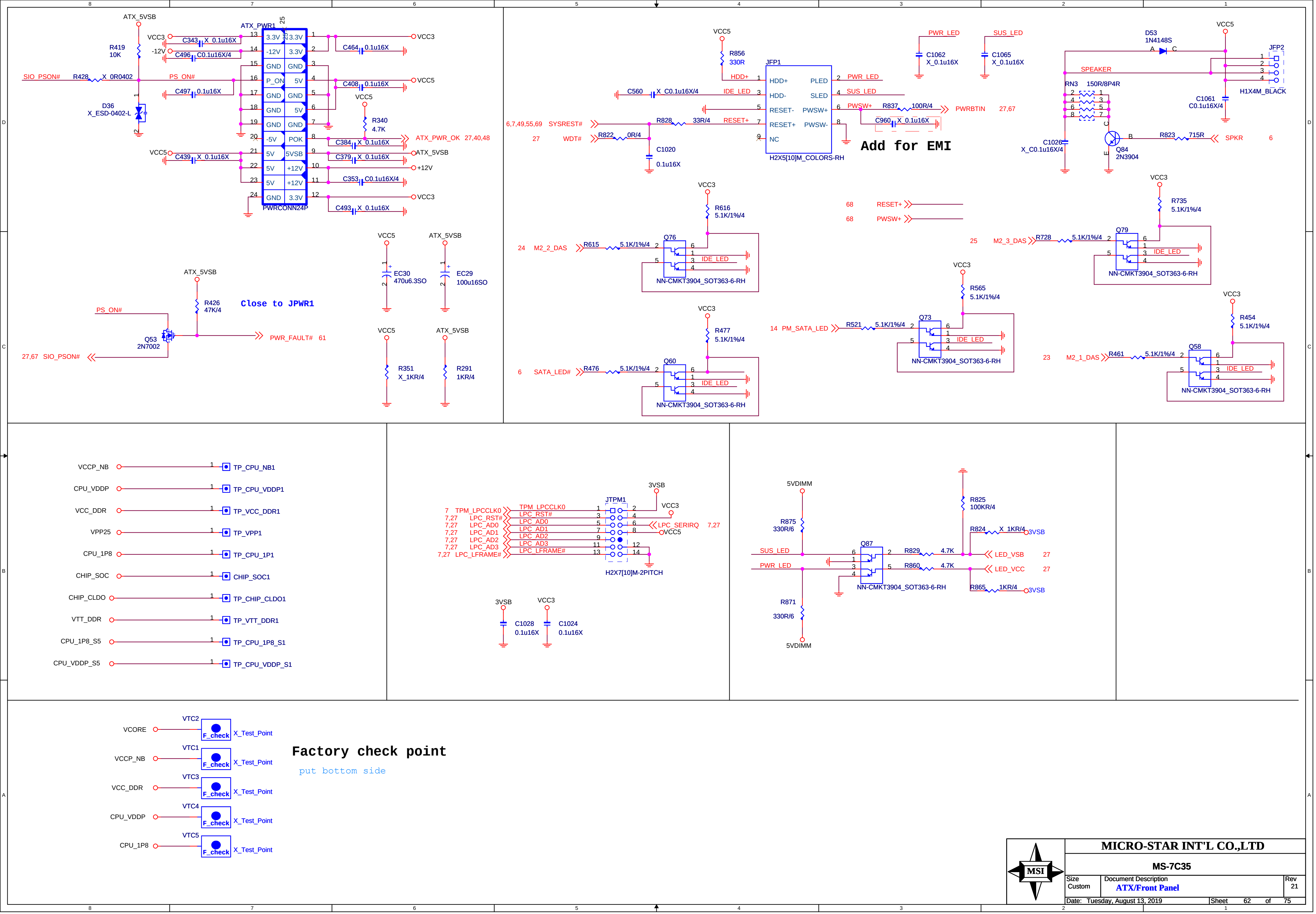

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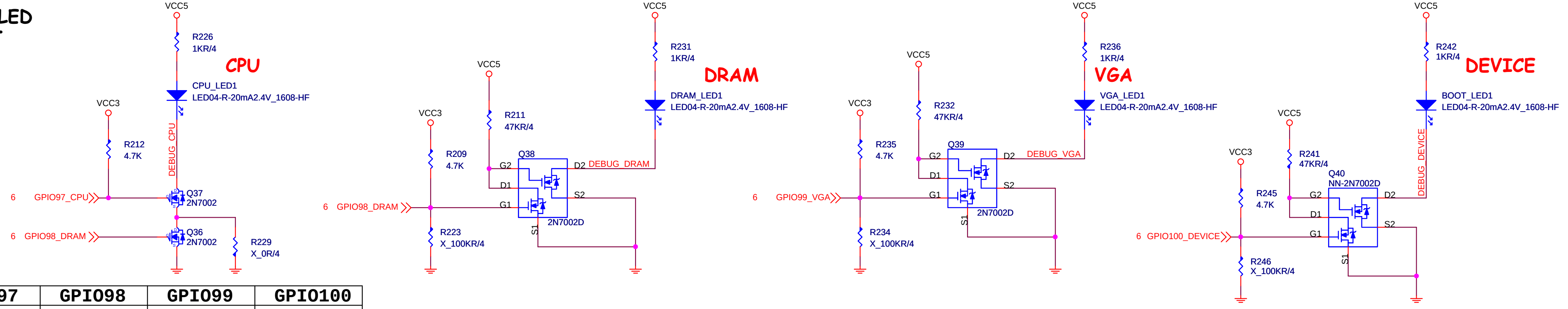
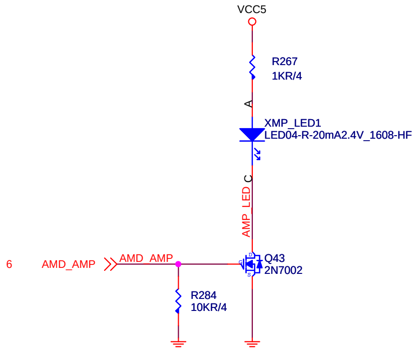
EZ Debug LED



LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獯	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED



LED	x16	x8	x4
PCIE2	Red	White	White

LED \ GPIO	EGPIO95	EGPIO96
獯	GPO PO HIGH	GPO PO HIGH
防	GPI (default LOW)	GPI (default LOW)

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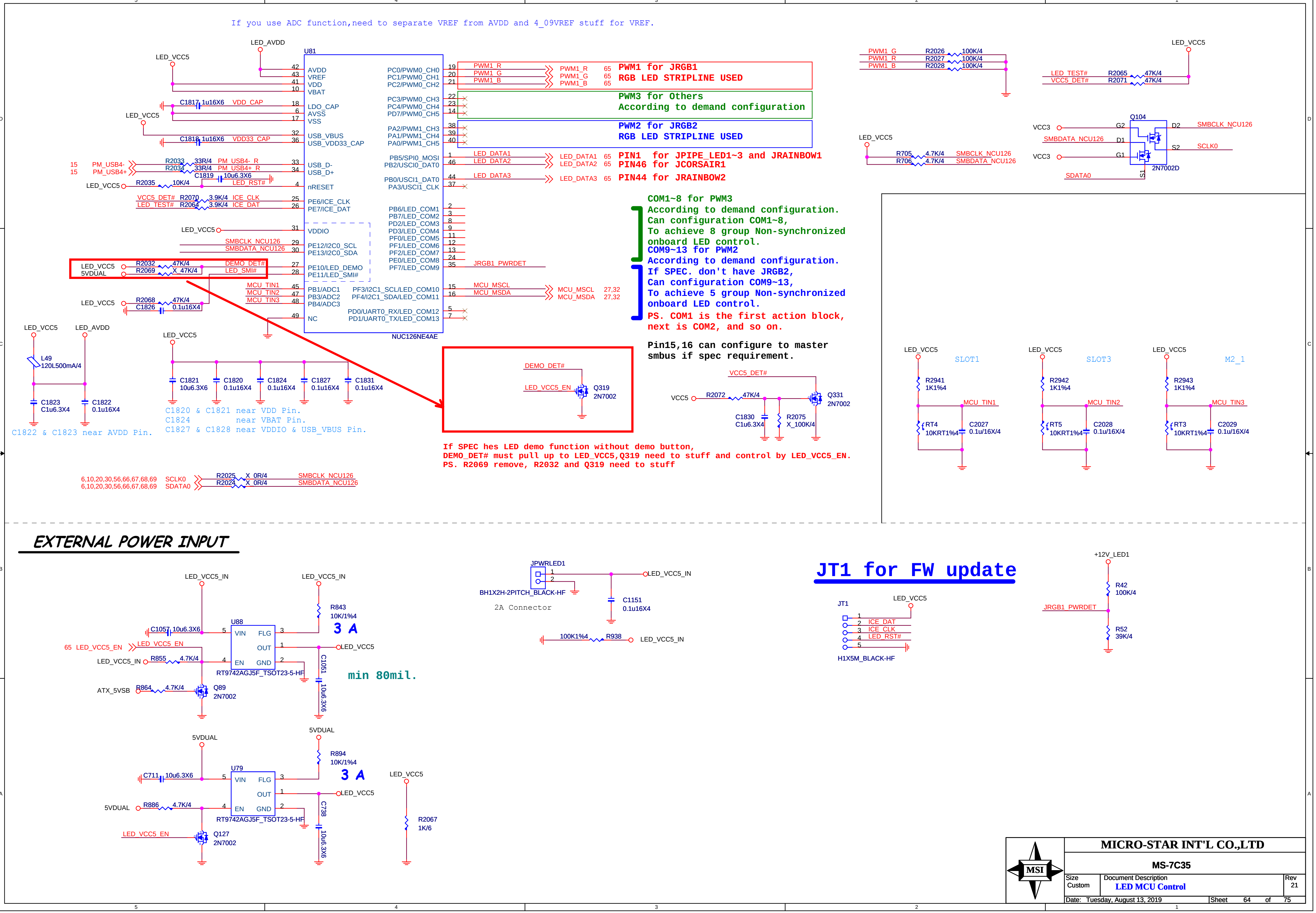
If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.
PWM1 for JRGB1
RGB LED STRIPLINE USED
PWM3 for Others
According to demand configuration
PWM2 for JRGB2
RGB LED STRIPLINE USED
PIN1 for JPIPE_LED1~3 and JRAINBOW1
PIN46 for JCORSAIR1
PIN44 for JRAINBOW2
COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.
COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized
onboard LED control.
PS. COM1 is the first action block,
next is COM2, and so on.
Pin15,16 can configure to master
smbus if spec requirement.
C1820 & C1821 near VDD Pin.
C1824 near VBAT Pin.
C1827 & C1828 near VDDIO & USB_VBUS Pin.
C1822 & C1823 near AVDD Pin.
If SPEC hes LED demo function without demo button,
DEMO_DET# must pull up to LED_VCC5,Q319 need to stuff and control by LED_VCC5_EN.
PS. R2069 remove, R2032 and Q319 need to stuff
U81
NUC126NE4AE
SLOT1
SLOT3
M2_1
EXTERNAL POWER INPUT
JT1 for FW update
JPWRLED1
BH1X2H-2PITCH_BLACK-HF
2A Connector
JT1
H1X5M_BLACK-HF
U88
RT9742AGJ5F_TSOT23-5-HF
3 A
min 80mil.
U79
RT9742AGJ5F_TSOT23-5-HF
3 A
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LED MCU Control
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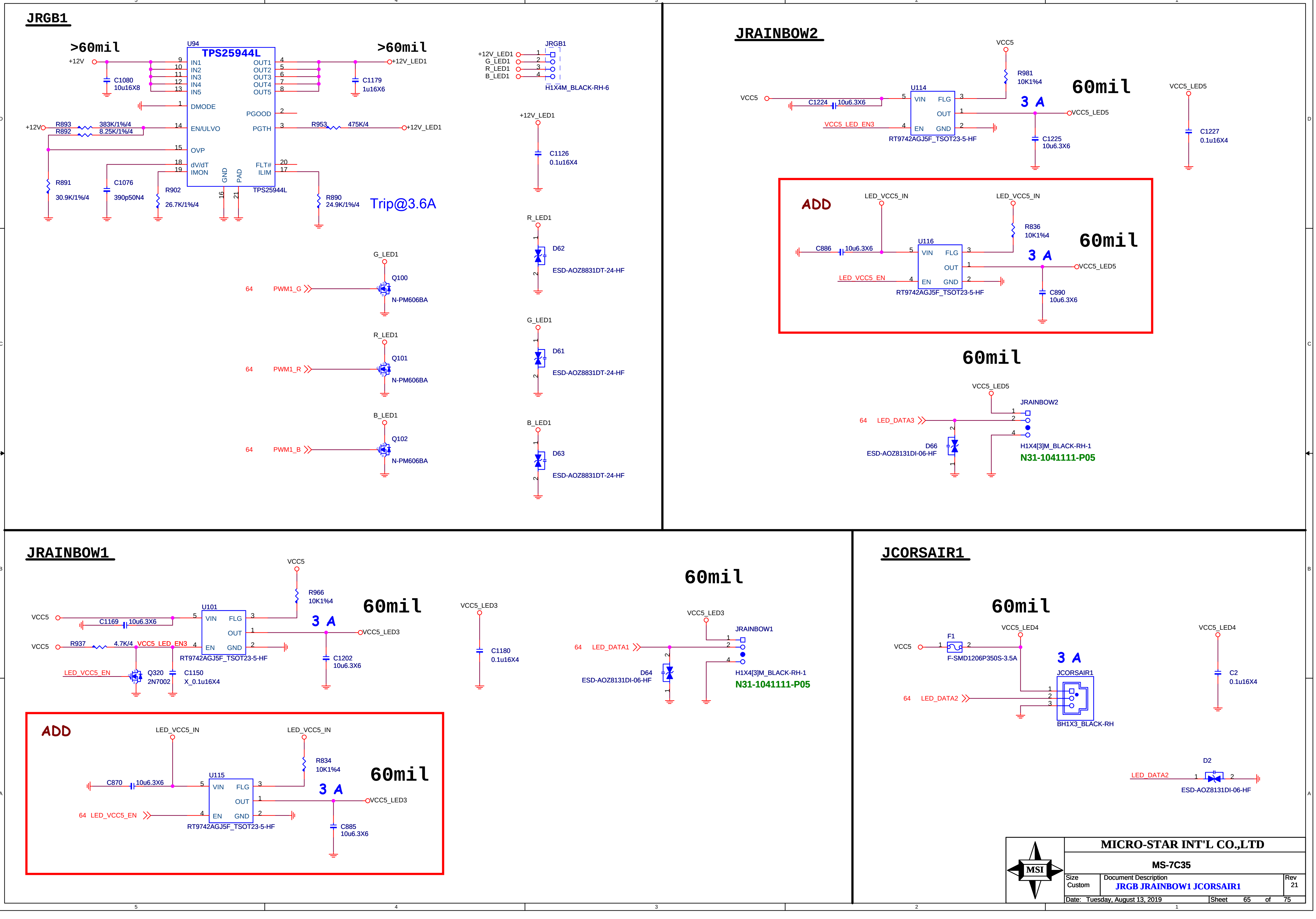
JRGB1
>60mil
U94
TPS25944L
+12V
C1080
10u16X8
IN1
IN2
IN3
IN4
IN5
OUT1
OUT2
OUT3
OUT4
OUT5
C1179
1u16X6
+12V_LED1
DMODE
PGOOD
EN/ULVO
PGTH
R893
R892
383K/1%/4
8.25K/1%/4
R953
475K/4
OVP
dV/dT
IMON
GND
PAD
FLT#
ILIM
R891
30.9K/1%/4
C1076
390p50N4
R902
26.7K/1%/4
R890
24.9K/1%/4
Trip@3.6A
JRGB1
+12V_LED1
G_LED1
R_LED1
B_LED1
H1X4M_BLACK-RH-6
C1126
0.1u16X4
D62
ESD-AOZ8831DT-24-HF
D61
D63
Q100
Q101
Q102
N-PM606BA
PWM1_G
PWM1_R
PWM1_B
JRAINBOW2
VCC5
R981
10K1%4
60mil
VCC5_LED5
C1224
10u6.3X6
U114
VIN
FLG
OUT
EN
GND
3 A
VCC5_LED_EN3
RT9742AGJ5F_TSOT23-5-HF
C1225
10u6.3X6
C1227
0.1u16X4
ADD
LED_VCC5_IN
R836
10K1%4
C886
10u6.3X6
U116
LED_VCC5_EN
C890
10u6.3X6
VCC5_LED5
JRAINBOW2
LED_DATA3
D66
ESD-AOZ8131DI-06-HF
H1X4[3]M_BLACK-RH-1
N31-1041111-P05
JRAINBOW1
VCC5
R966
10K1%4
U101
C1169
10u6.3X6
R937
4.7K/4
VCC5_LED_EN3
VCC5_LED3
C1202
10u6.3X6
Q320
2N7002
C1150
X_0.1u16X4
LED_VCC5_EN
C1180
0.1u16X4
JRAINBOW1
LED_DATA1
D64
ESD-AOZ8131DI-06-HF
H1X4[3]M_BLACK-RH-1
N31-1041111-P05
ADD
LED_VCC5_IN
R834
10K1%4
C870
10u6.3X6
U115
C885
10u6.3X6
JCORSAIR1
60mil
VCC5_LED4
F1
F-SMD1206P350S-3.5A
3 A
JCORSAIR1
LED_DATA2
BH1X3_BLACK-RH
C2
0.1u16X4
D2
ESD-AOZ8131DI-06-HF
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MSI
MS-7C35
Size
Custom
Document Description
JRGB JRAINBOW1 JCORSAIR1
Rev
21
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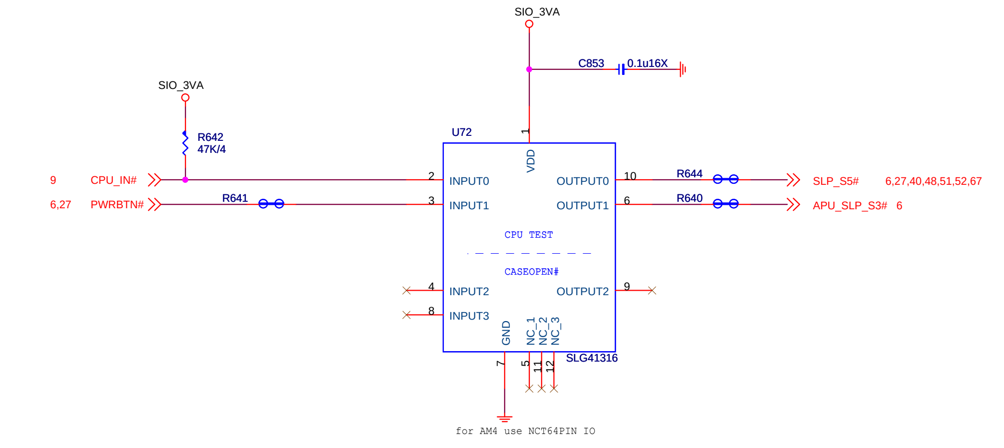
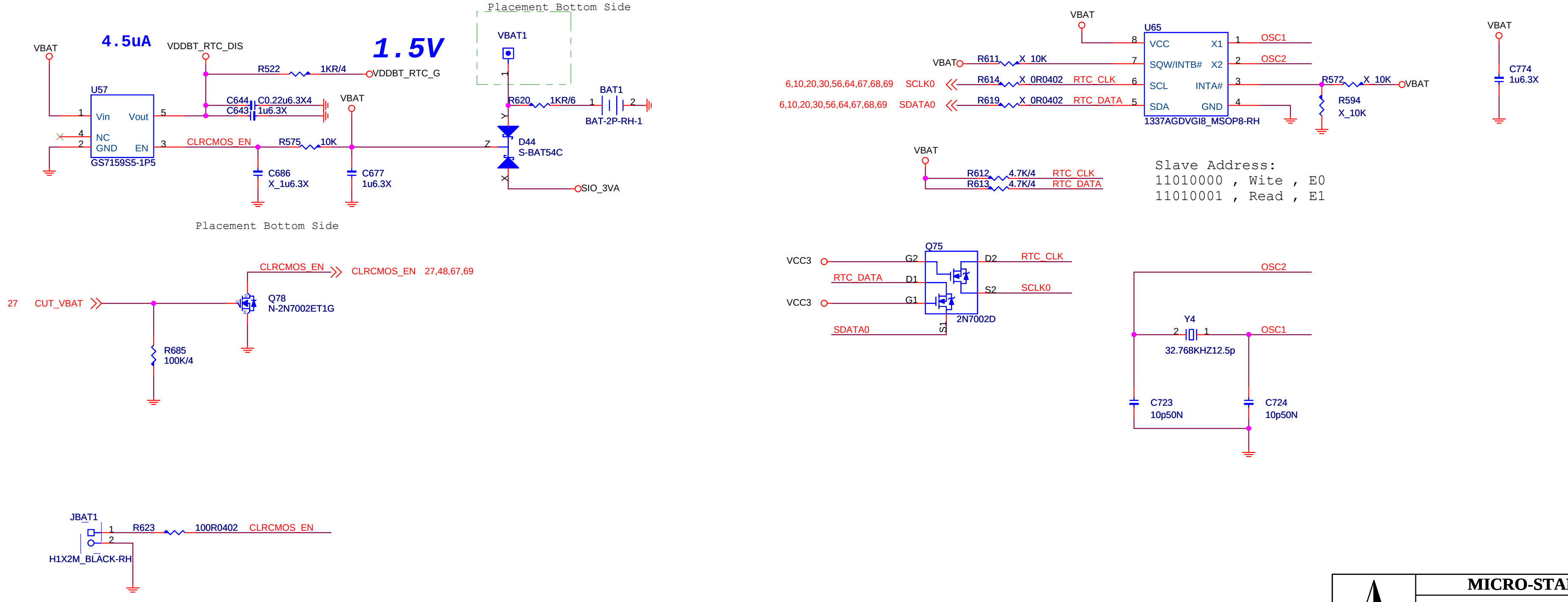


RTC & Clear CMOS Circuit



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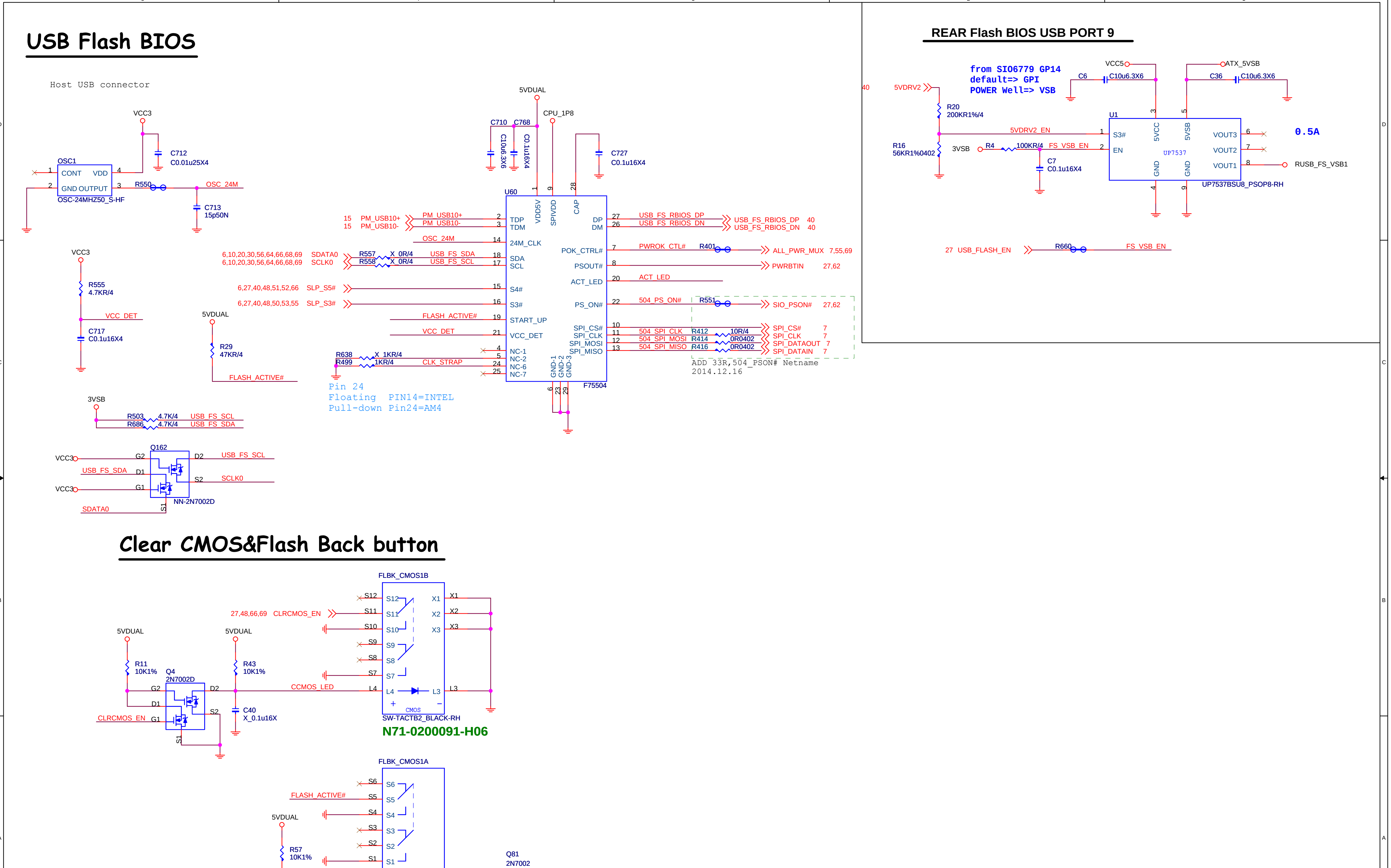
USB Flash BIOS



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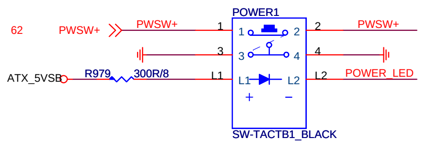
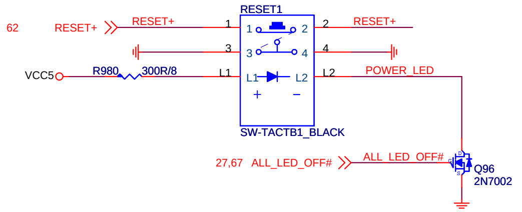
Power ON Button

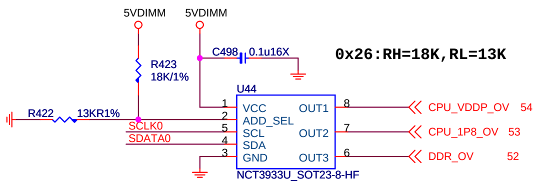


Reset Button

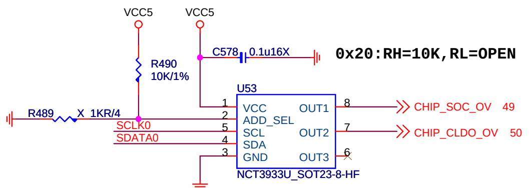


Over Voltage Control IC

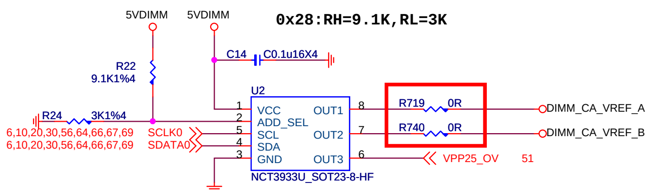
0x26:RH=18K,RL=13K



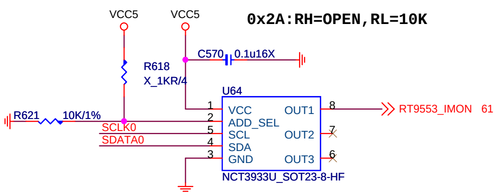
0x20:RH=10K,RL=OPEN



0x28:RH=9.1K,RL=3K



0x2A:RH=OPEN,RL=10K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
	0%	25%	40%	60%	75%	100%

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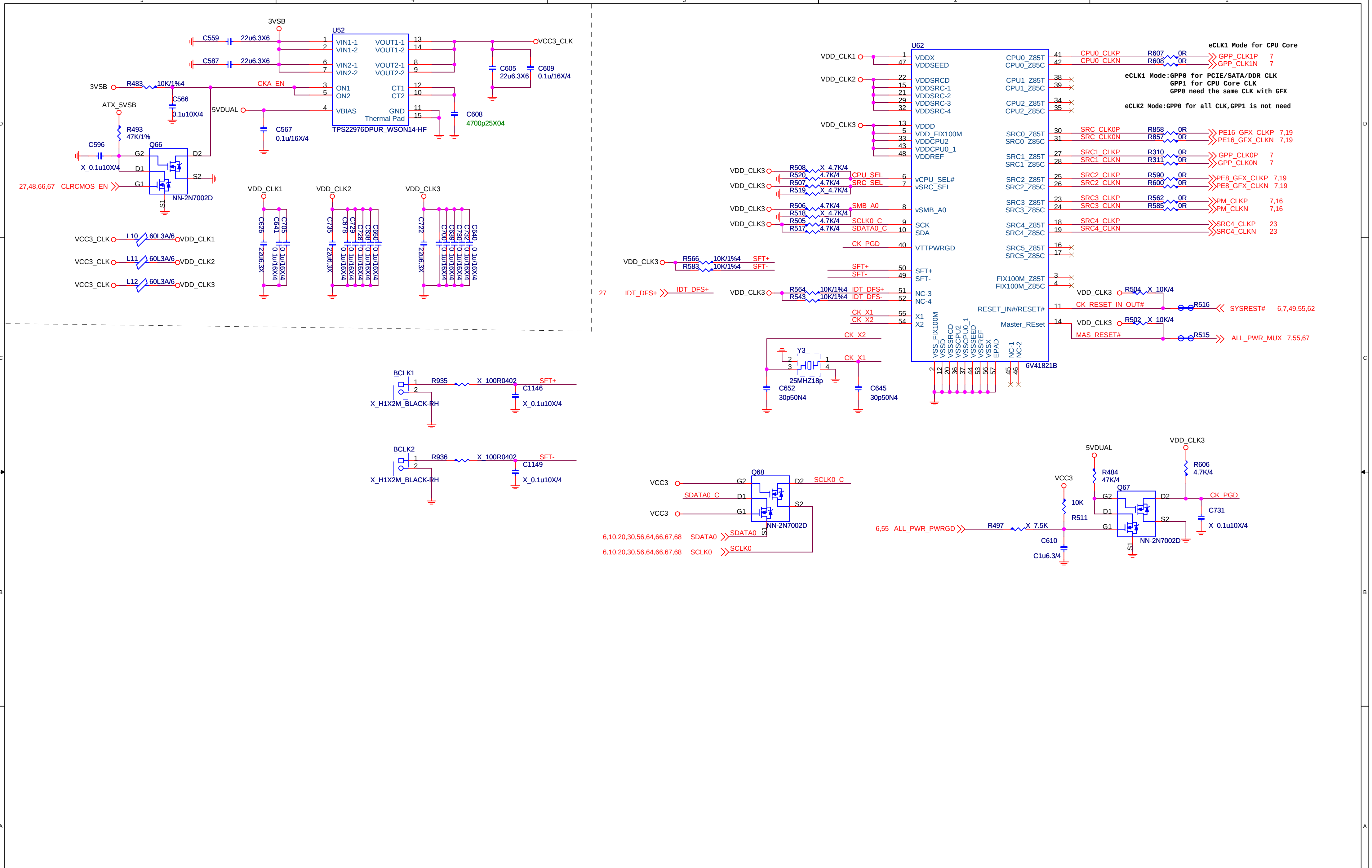

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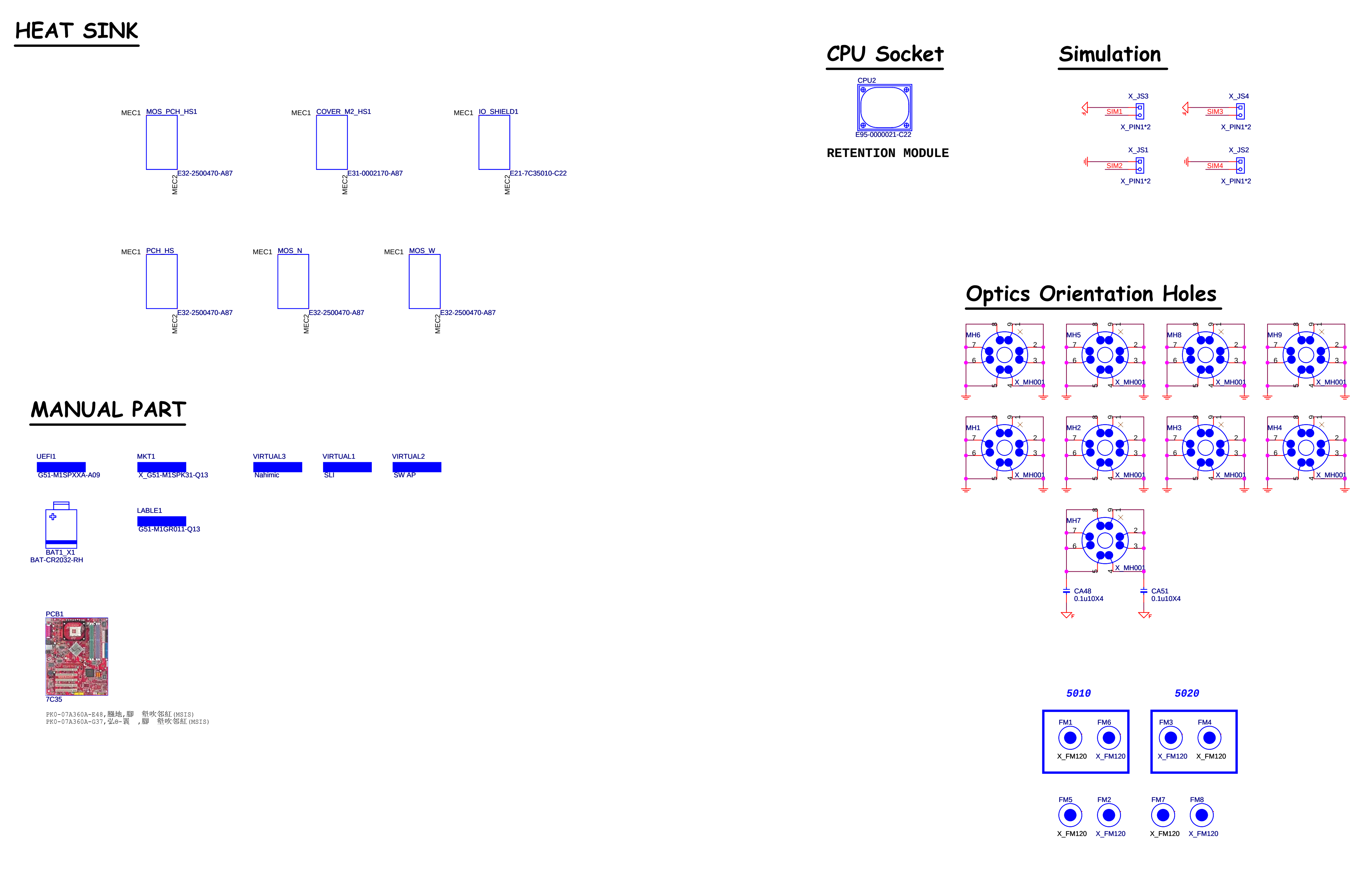

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