MS-7C35 Ver:11

CPU:
AMD AM4

System Chipset:
Prenium X570
(Performance gaming)

Main Memory:
DDR IV * 4S MAX:64 GB

VRM
IR35201 12+2 O

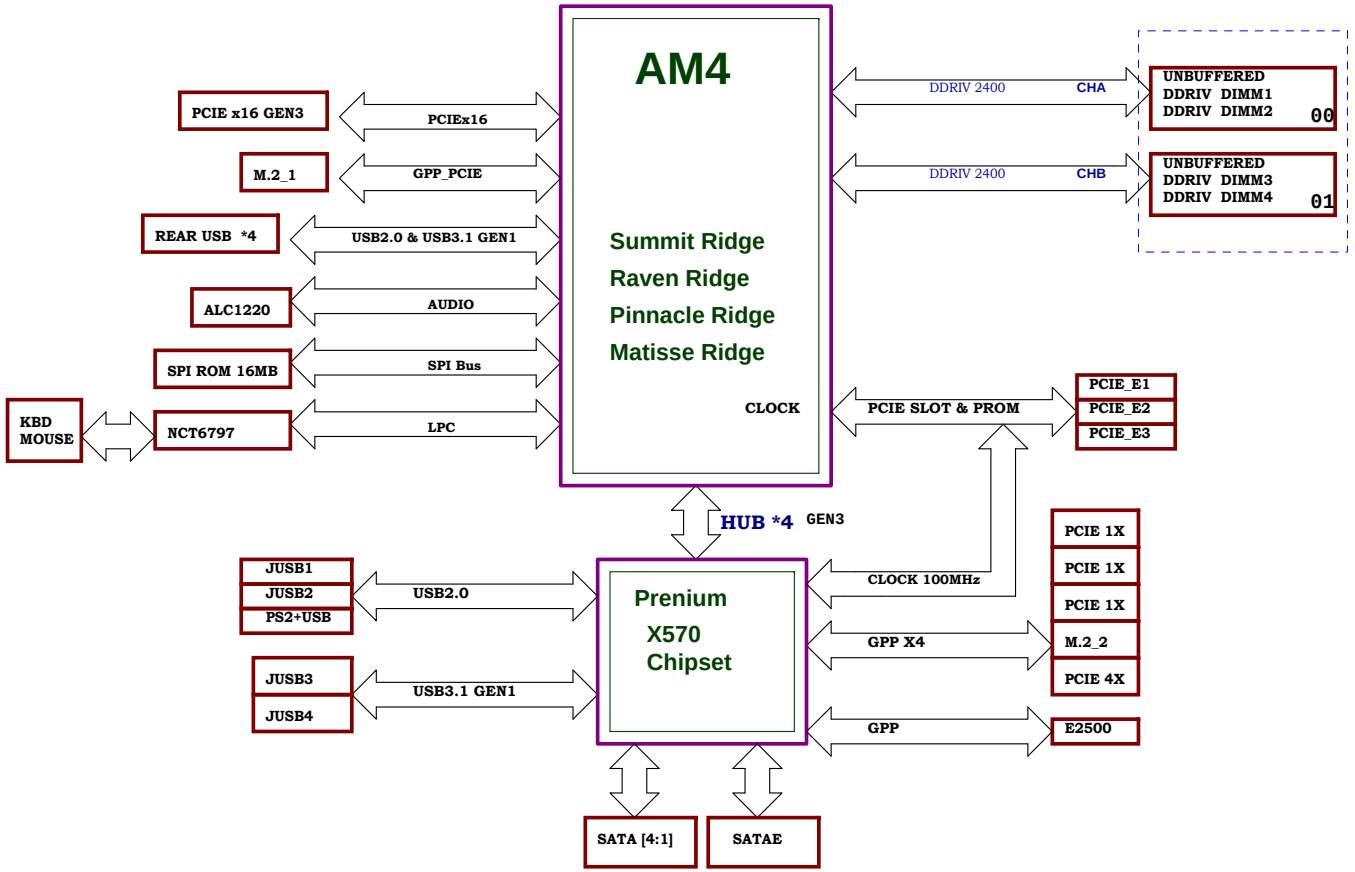
On Board Chipset:
LPC Super I/O --NCT6797D
LAN E2500
Azalia CODEC - Realtek ALC1220
ASM1143 USB3.1 Gen2

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X8 Slot * 1

From FCH
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X4 Slot * 1

OCP IC:
RT9553

BLOCK DIAGRAM



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AMD AM4

01 Block Diagram	36 USB Front Side	66 Clock Gen
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03 AM4 DDR4 I/F	38 Type A+C	68 Button/OV Ctrl
04 AM4 PCIE/SATAE	39 Type C Front	
05 AM4 Display/Audio	40 USB Charger	
06 AM4 SVI/ACPI/GPIO	41 ASM1562 REAR USB3.1	
07 AM4 LPC/SPI/USB/CLK/STRAP	42 SATA Connector	
08 AM4 Power/RTC Power/ 09 AM4 GND	43 ACPI 5VDIMM 5VDUAL & 3VSB	
10,11 DDR4-DIMM CH-A/B	44 PM-NB681GD-1.05V/GS7133-2.5V	
12,13 DDR4-POWER/GND	45 DDR PWR VPP25/VTT-MP2147	
14 Promontory-PCIE/SATA/SATAE	46 DDR Power-RT8125E	
15 Promontory-USB/OC	47CPU Power 1P8/1P8_S5	
16 Promontory-CLK/ACPI/GPIO	48CPU Power VDDP MP8712	
17 Promontory-Power / 18 Promontory-GND	49 CPU Power Connector/PWRGD	
19 PCIE X16(X8*2) SLOT	50 CPU Power IR35201 12 Phase	
20 PCIE Switch	51 CPU Power IR3598	
21 M.2_1 Connector	52 CPU Phase 1-4	
22 WIFI & BT	53 CPU Phase 5-8	
23 / 24 M2_2 Connector/M2_2 Swtch	54 CPU Phase 9-12 NB Phase 1-2	
25 PCIE 1X 4X	55 CPU Power NB S5	
26 SIO NCT6795D	56 RT9553 CURRENT SENSE	
27 HW monitor/Debug LED/NCT7718	57 ATX/Front Panel	
28 CPU/SYS FAN X2 TYPE J	58 EZ-Debug LED	
29 PUMP FAN TYPE J 2A	59 LED MCU Control	
30 SYS FAN X3 TYPE K	60 LED Board Side Stripline	
31 LAN E2500	61 JRGB JRAINBOW1 JCORSAIR1	
32 Audio ALC1220-1	62 LED DIMM/PCIE	
33 Audio ALC1220-2	63 RTC Circuit/Moat Cap	
34 USB Rear PS2+USB2.0	64 USB Flash BIOS	
35 USB Rear USB3.0	65 BOM Option	

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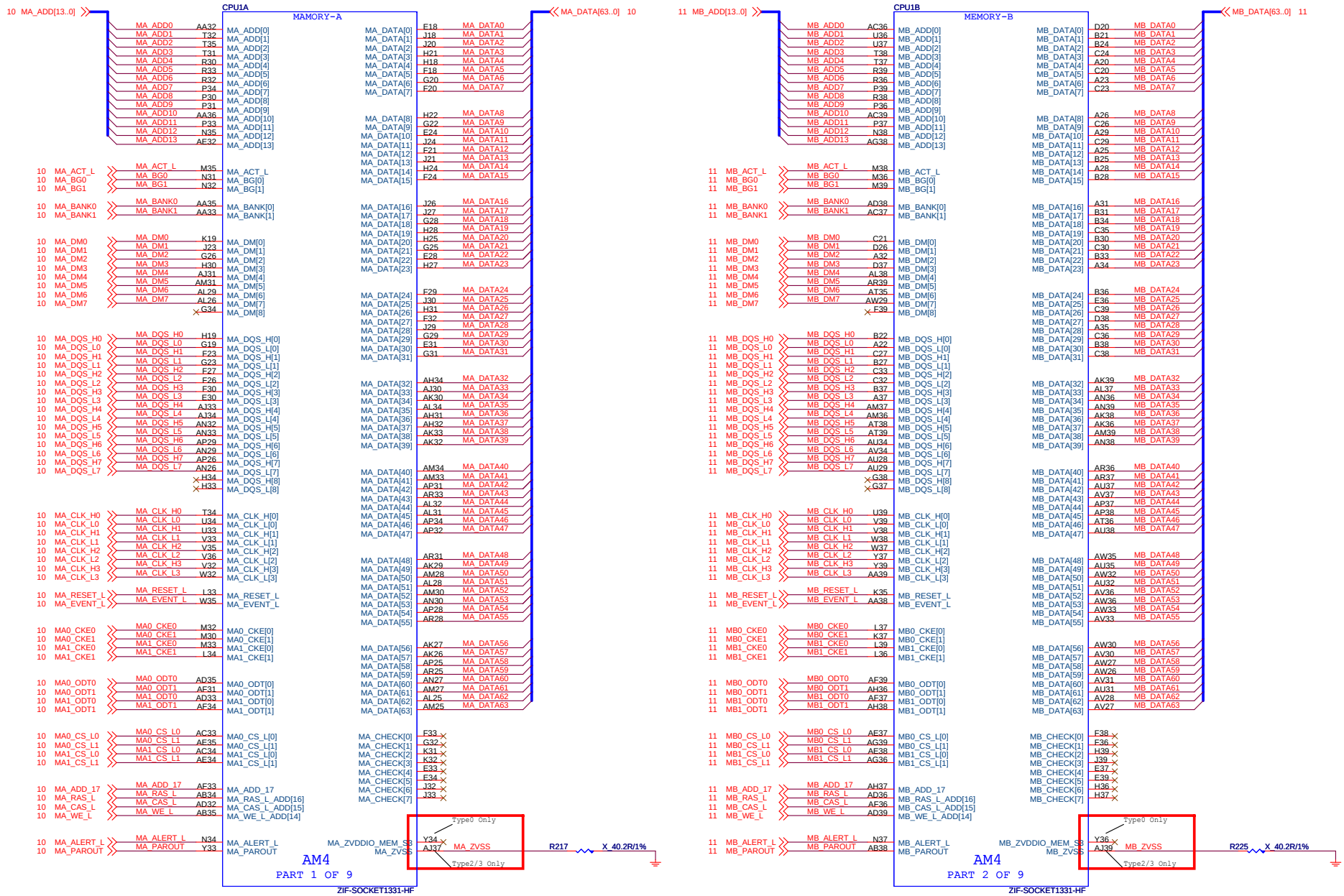

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Size: Custom	Document Description: AM4 DDR4 I/F	Rev: 11
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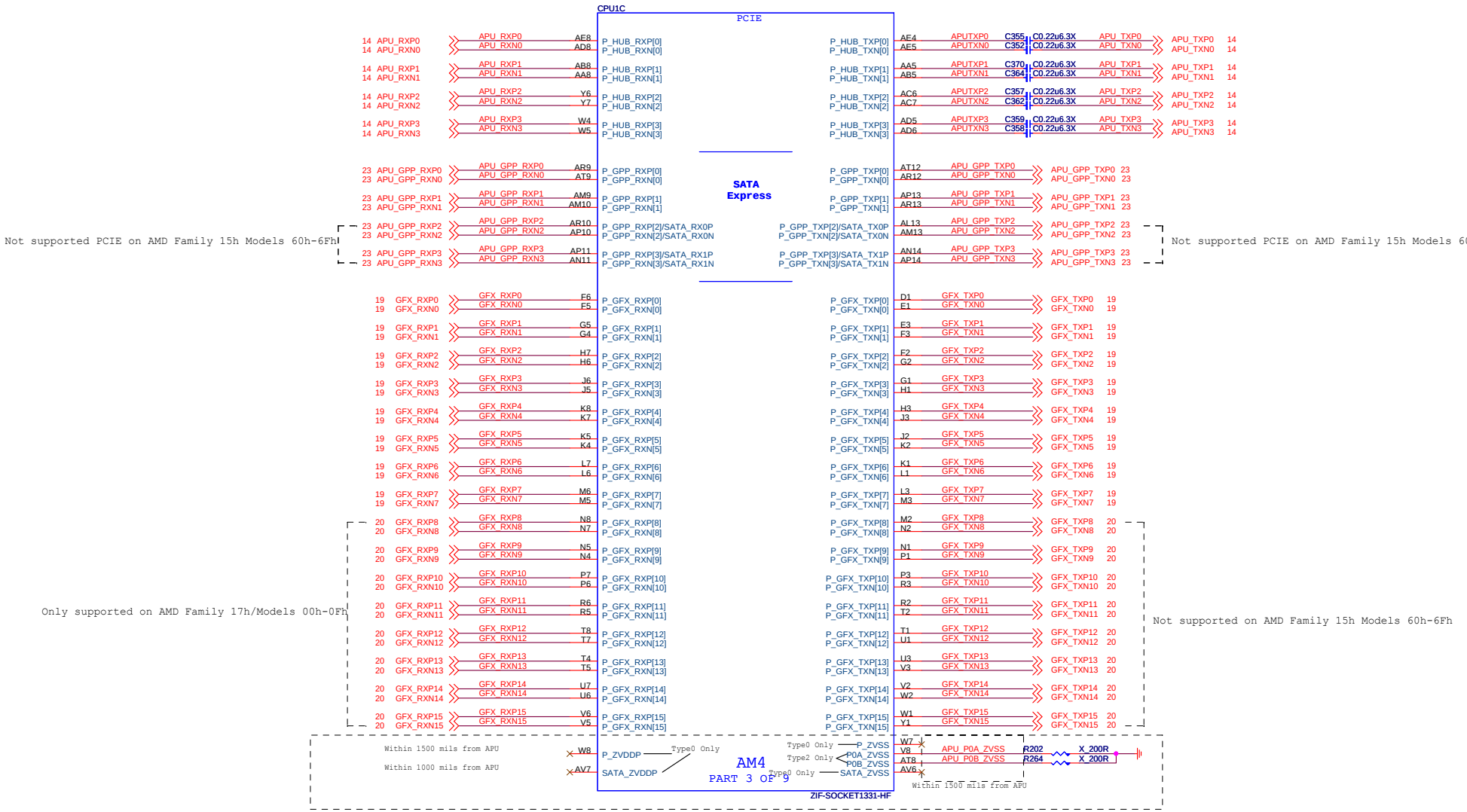

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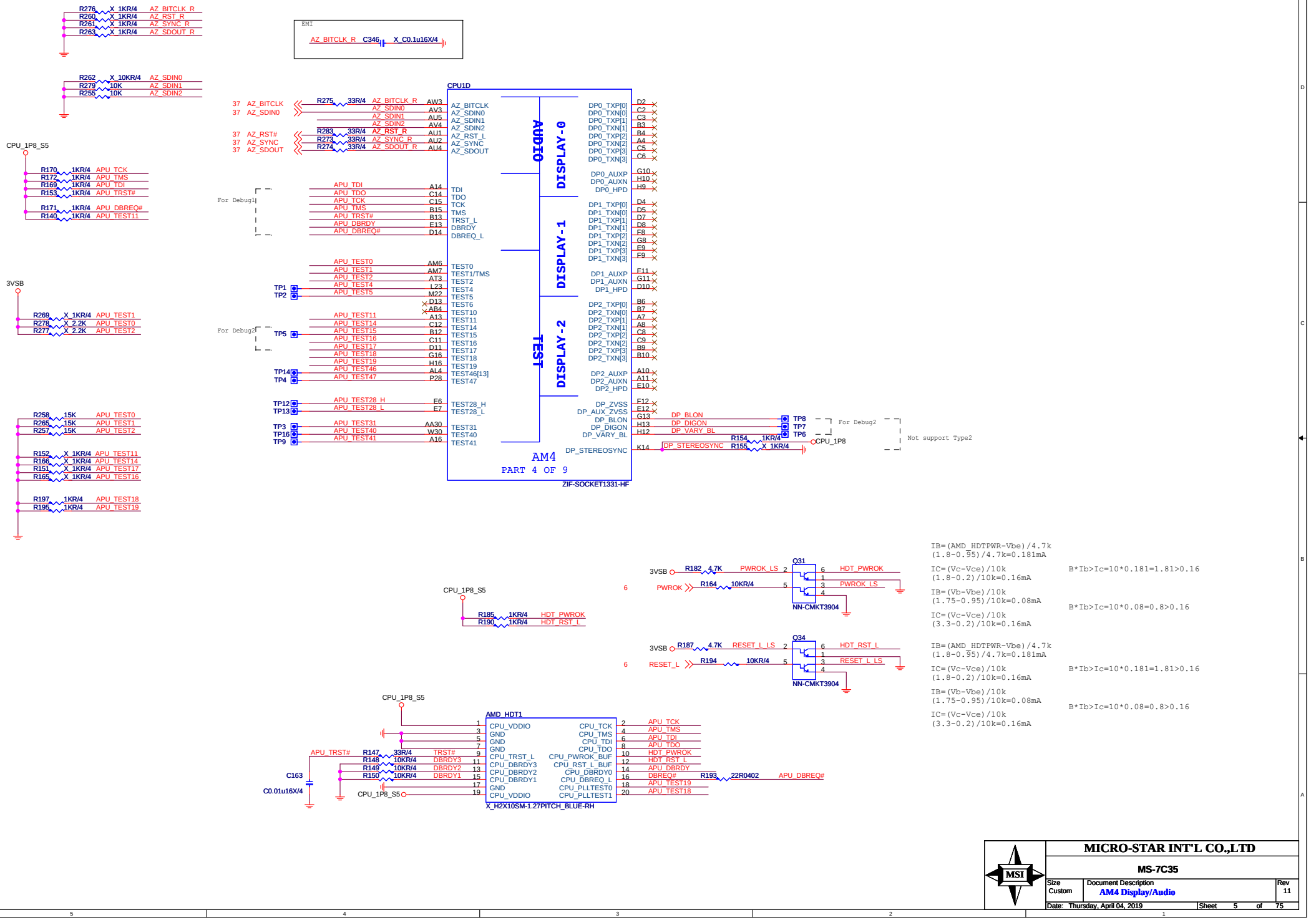
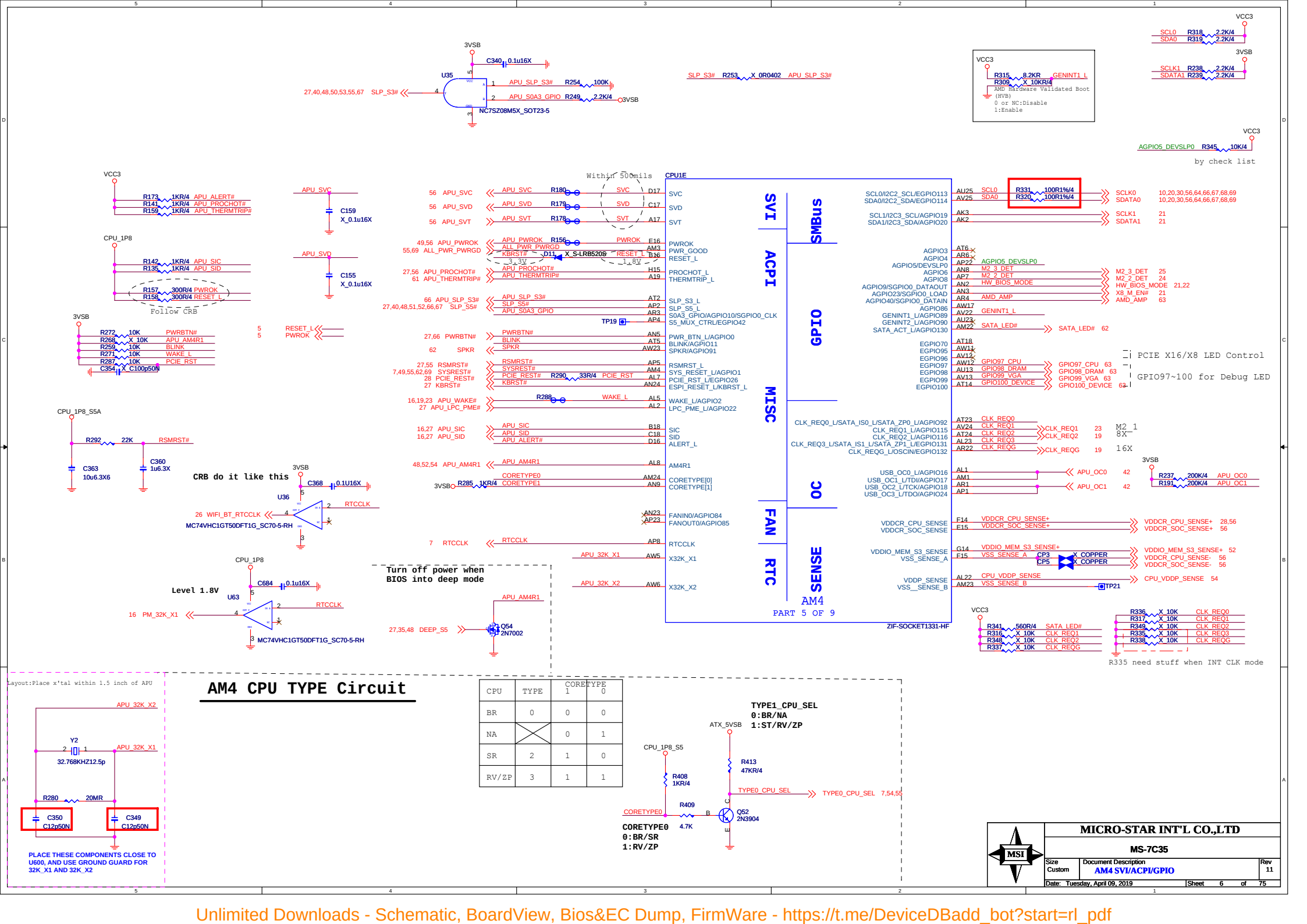
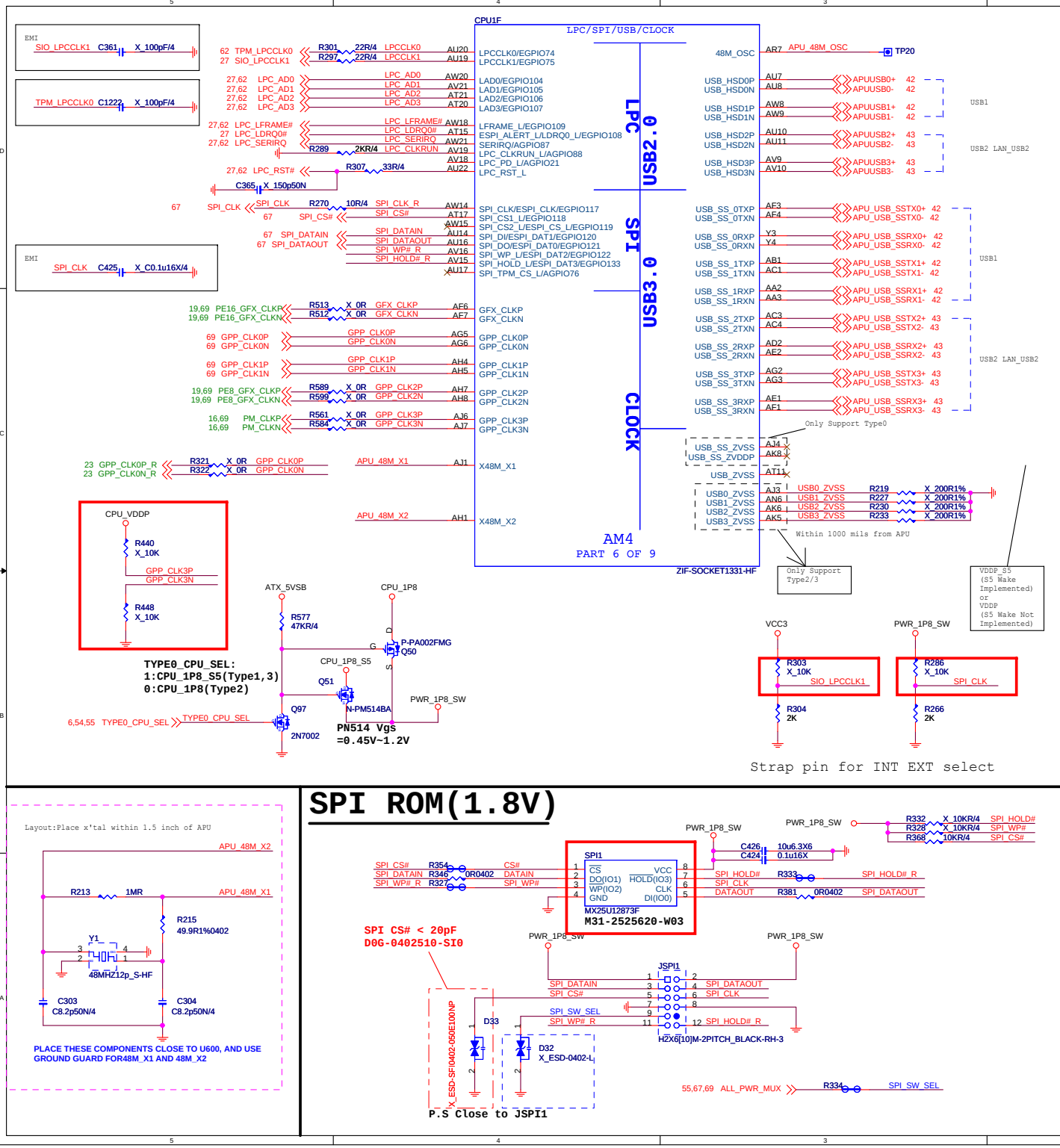
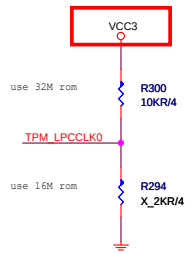


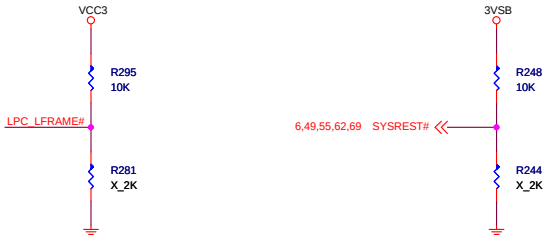




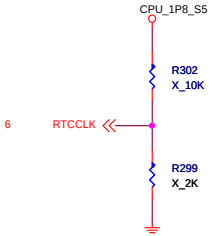
Strapping Options



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board

SPI ROM(1.8V)

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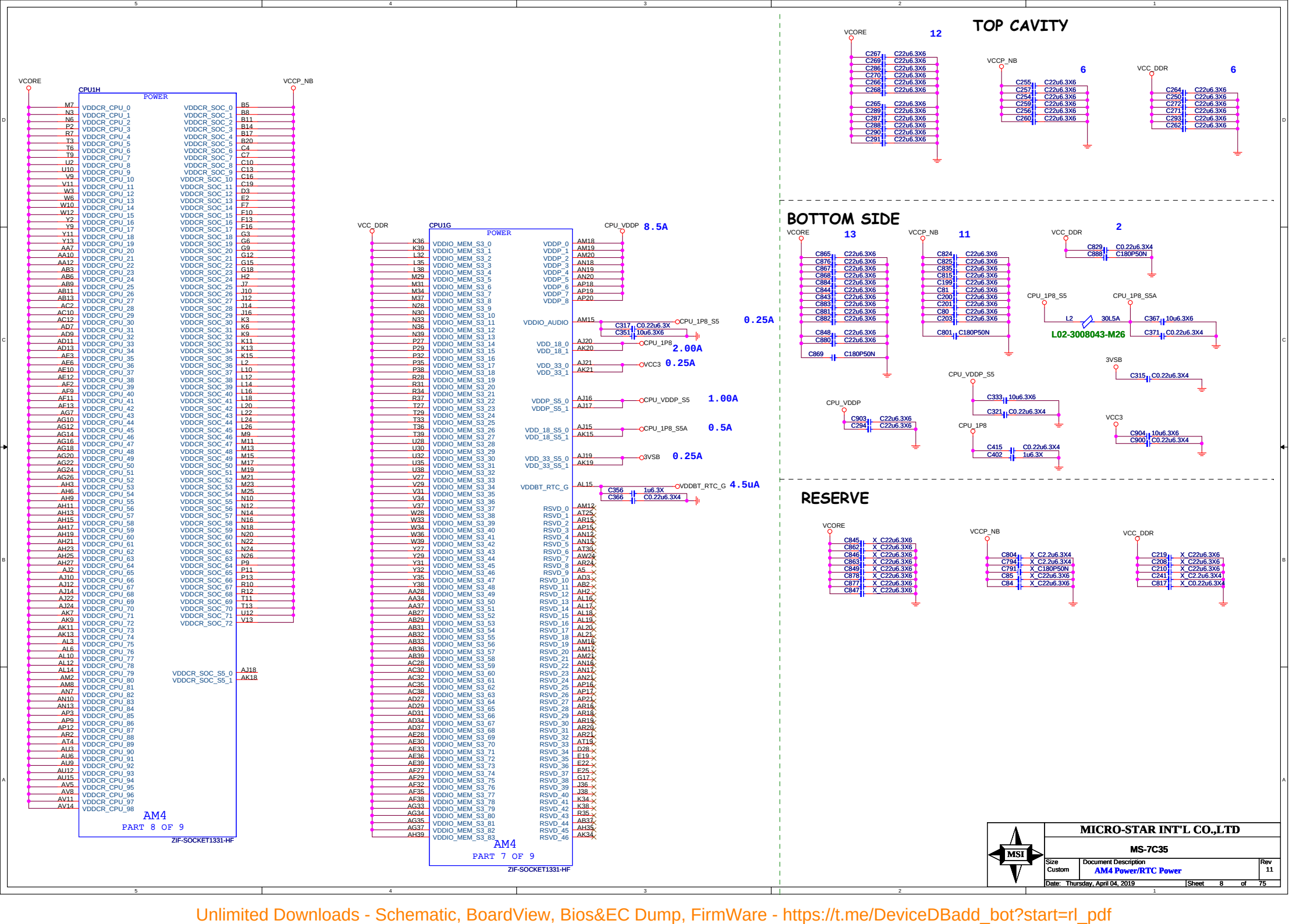

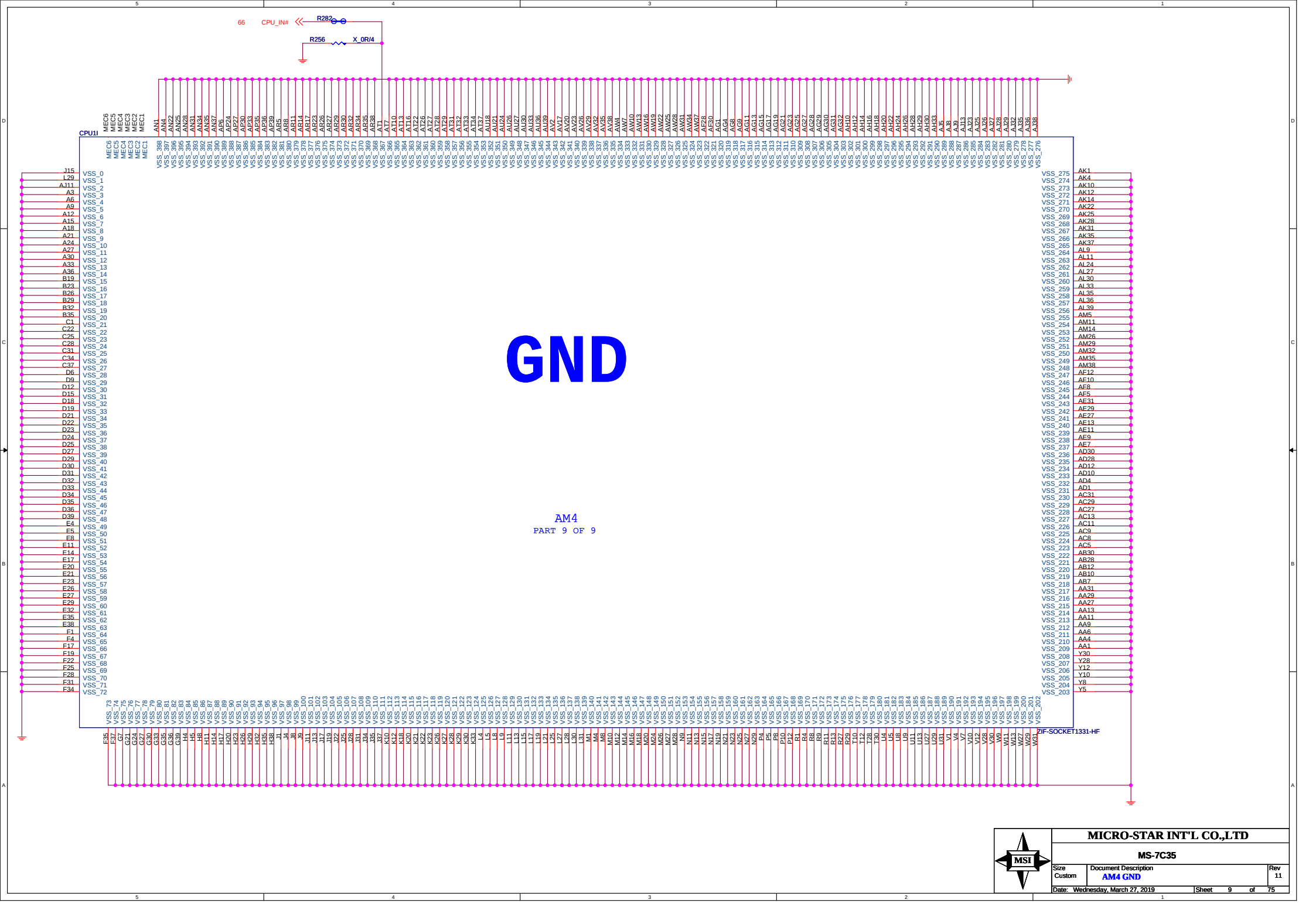

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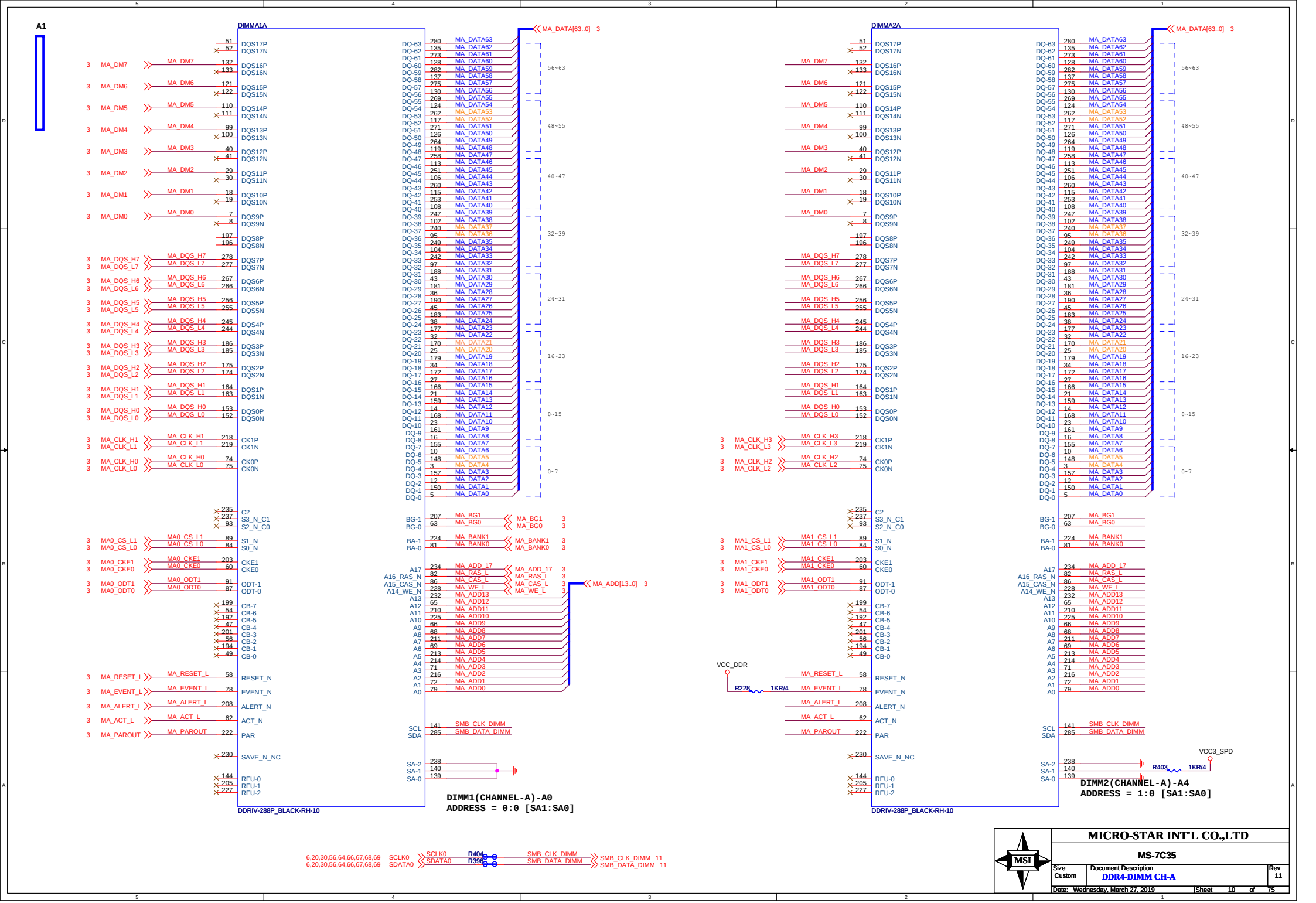
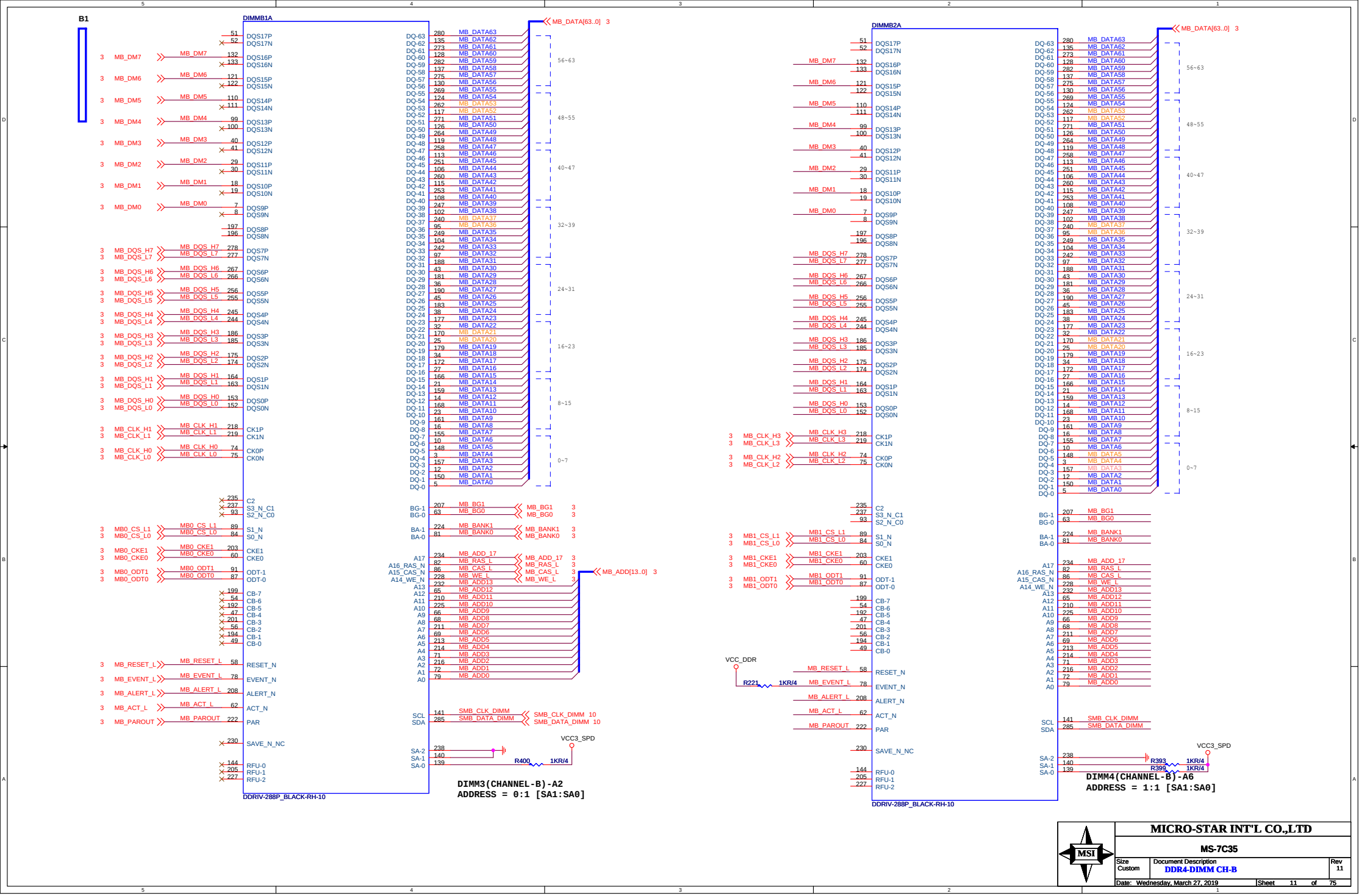
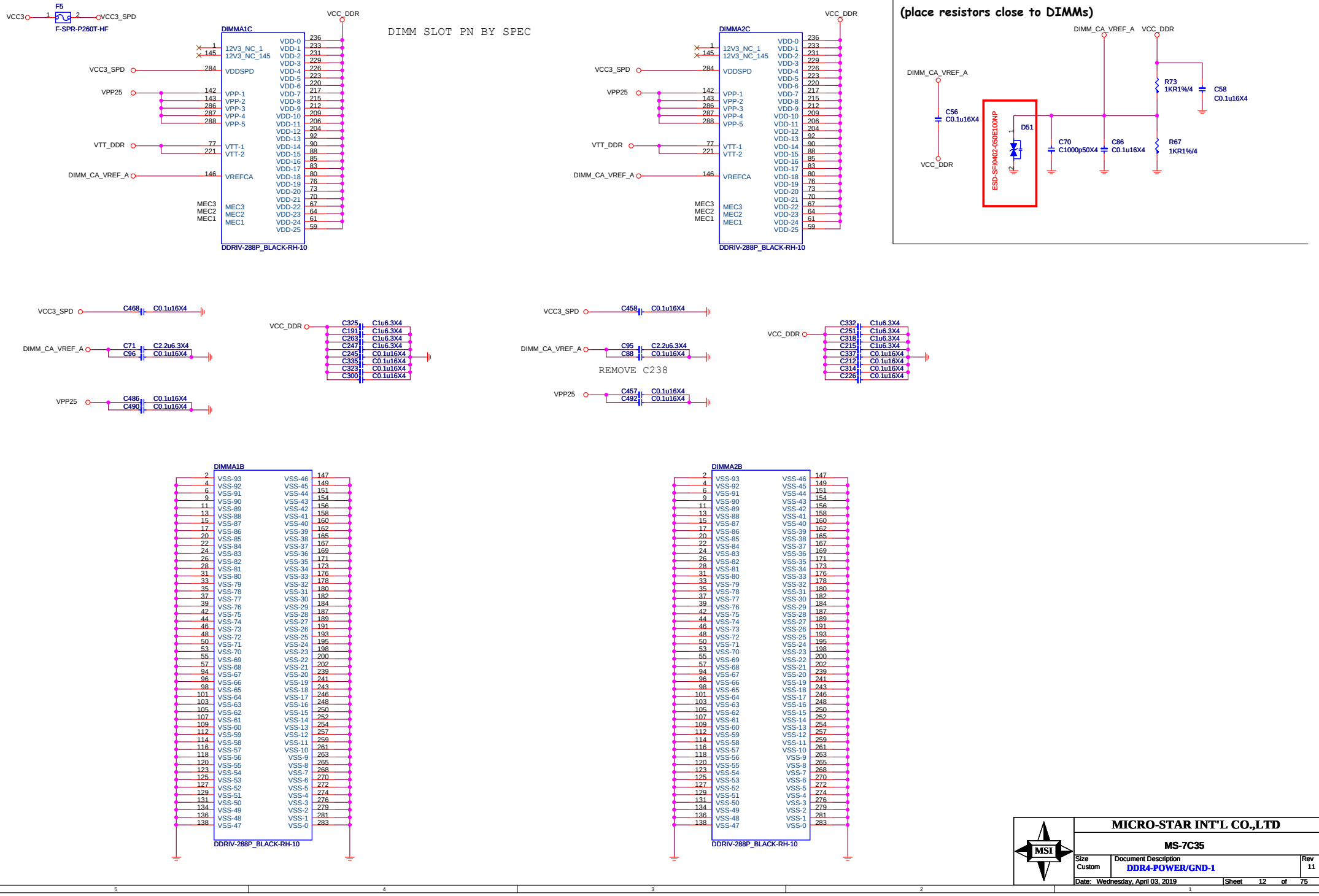
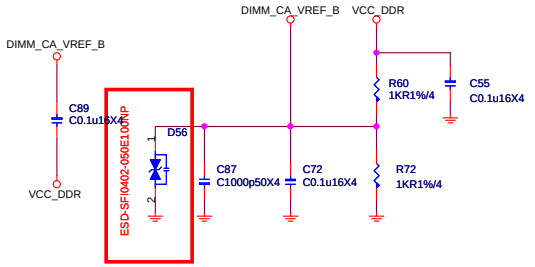


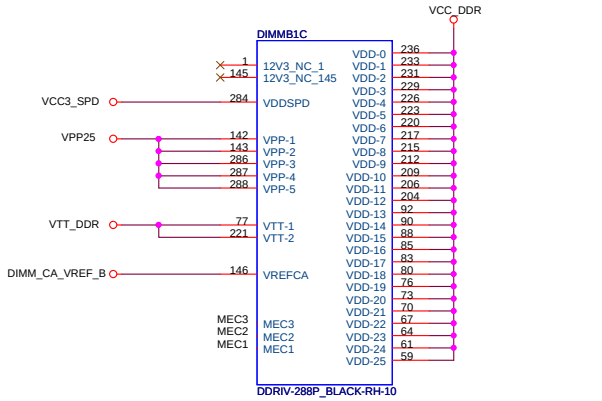


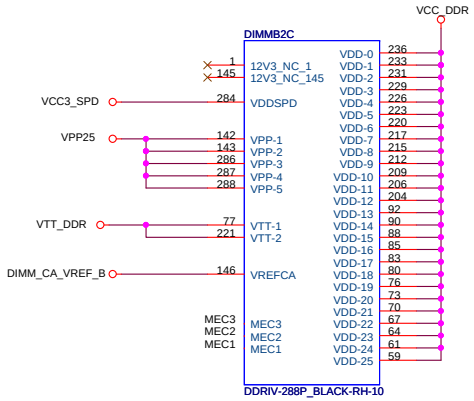


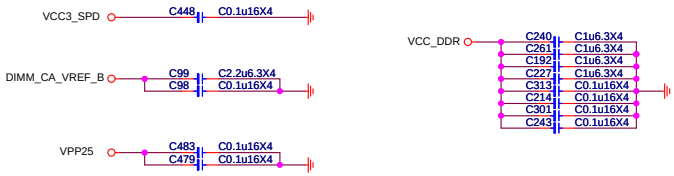
DDR VREF

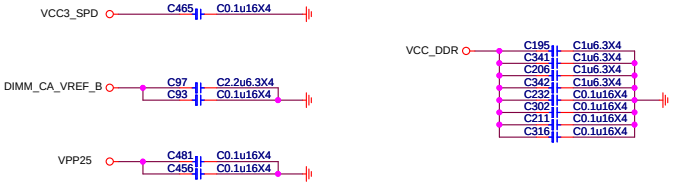
(place resistors close to DIMMs)

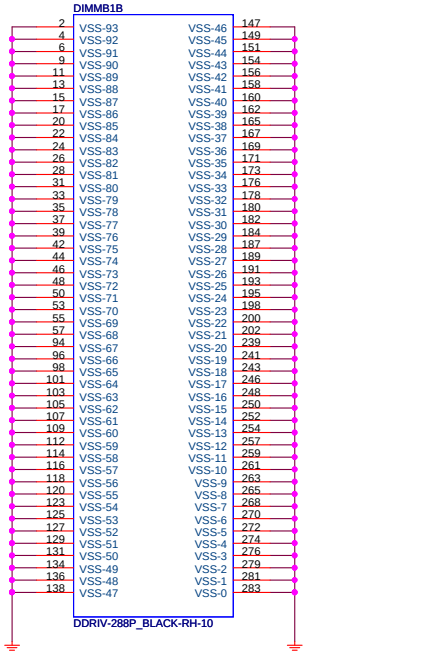


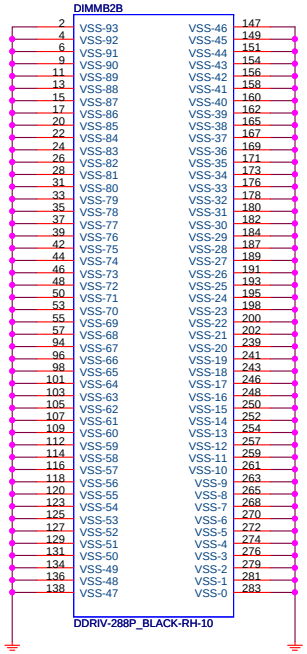












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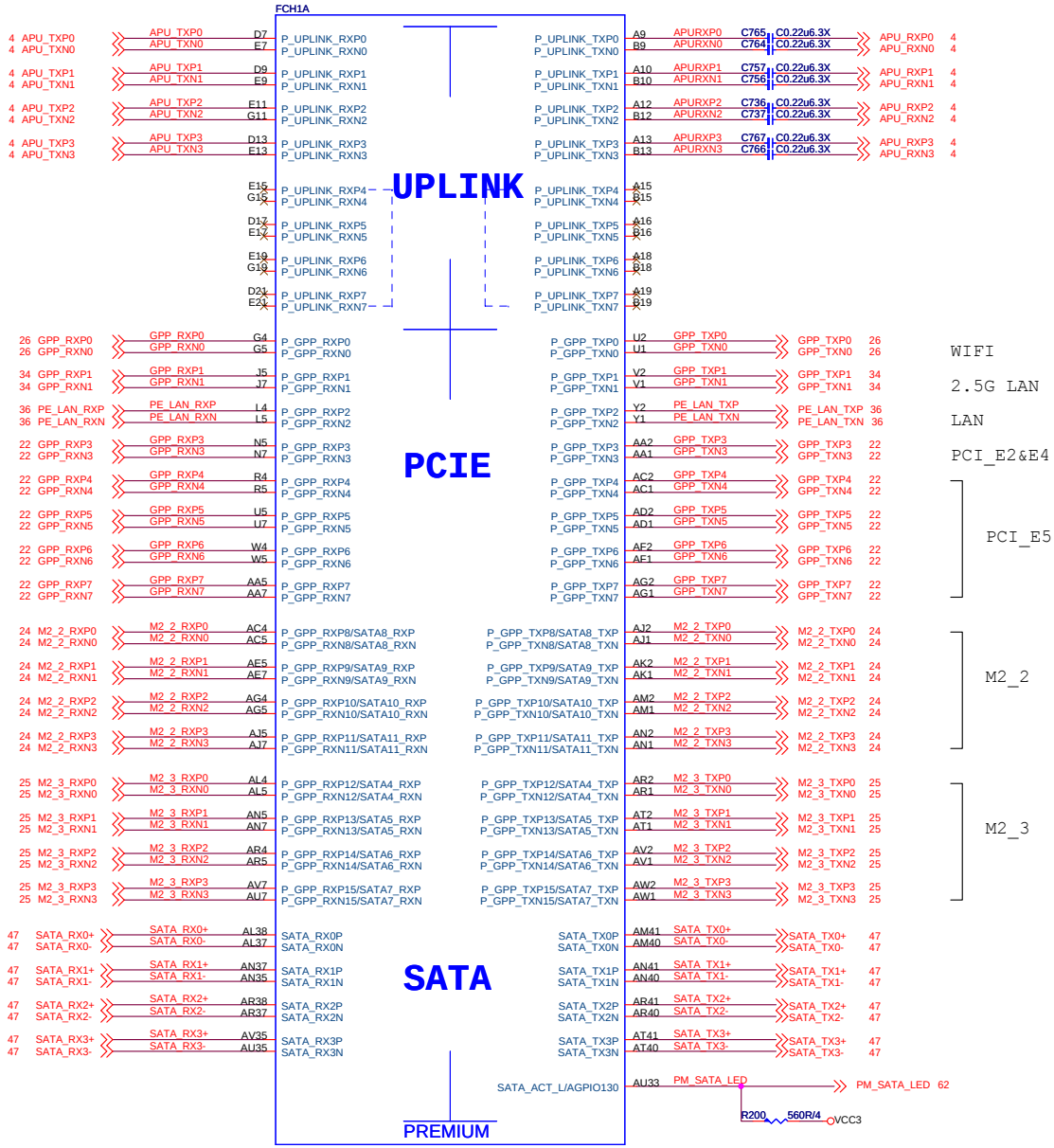

MICRO-STAR INT'L CO.,LTD	
MS-7C35	
Size: Custom	Document Description: Promontory-PCIE/SATA/SATAE
Rev: 11	
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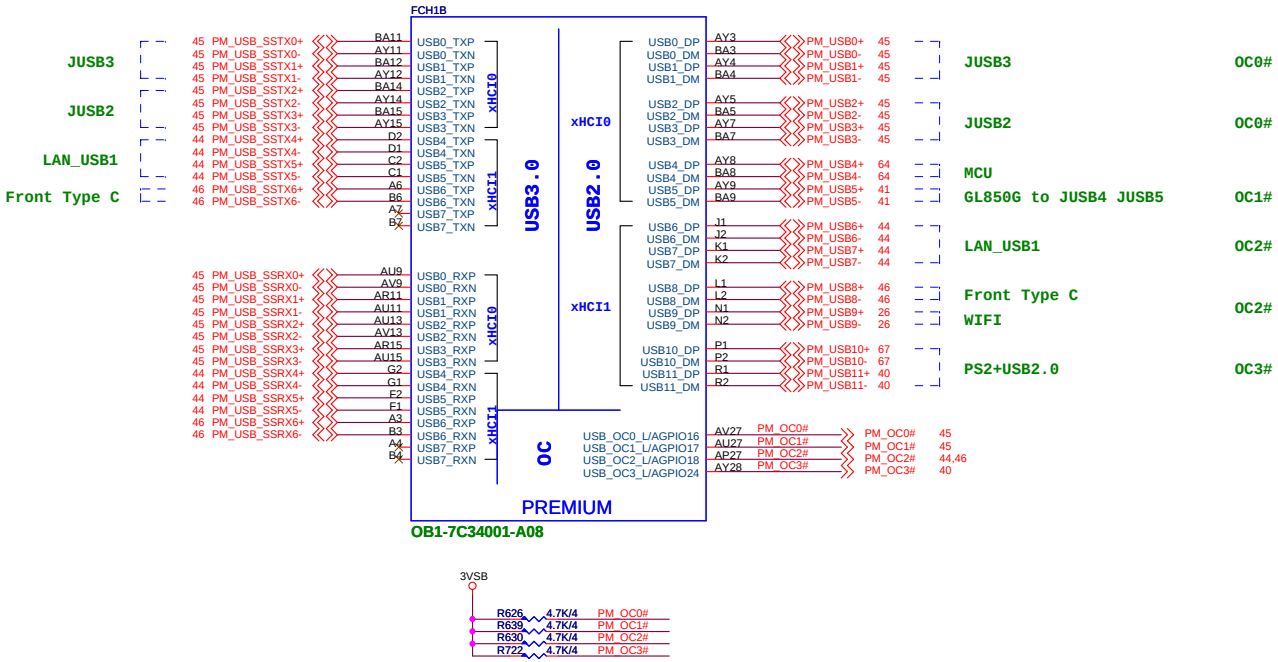

MICRO-STAR INT'L CO.,LTD		
Size: Custom	Document Description: Promontory-USB/OC	Rev: 11
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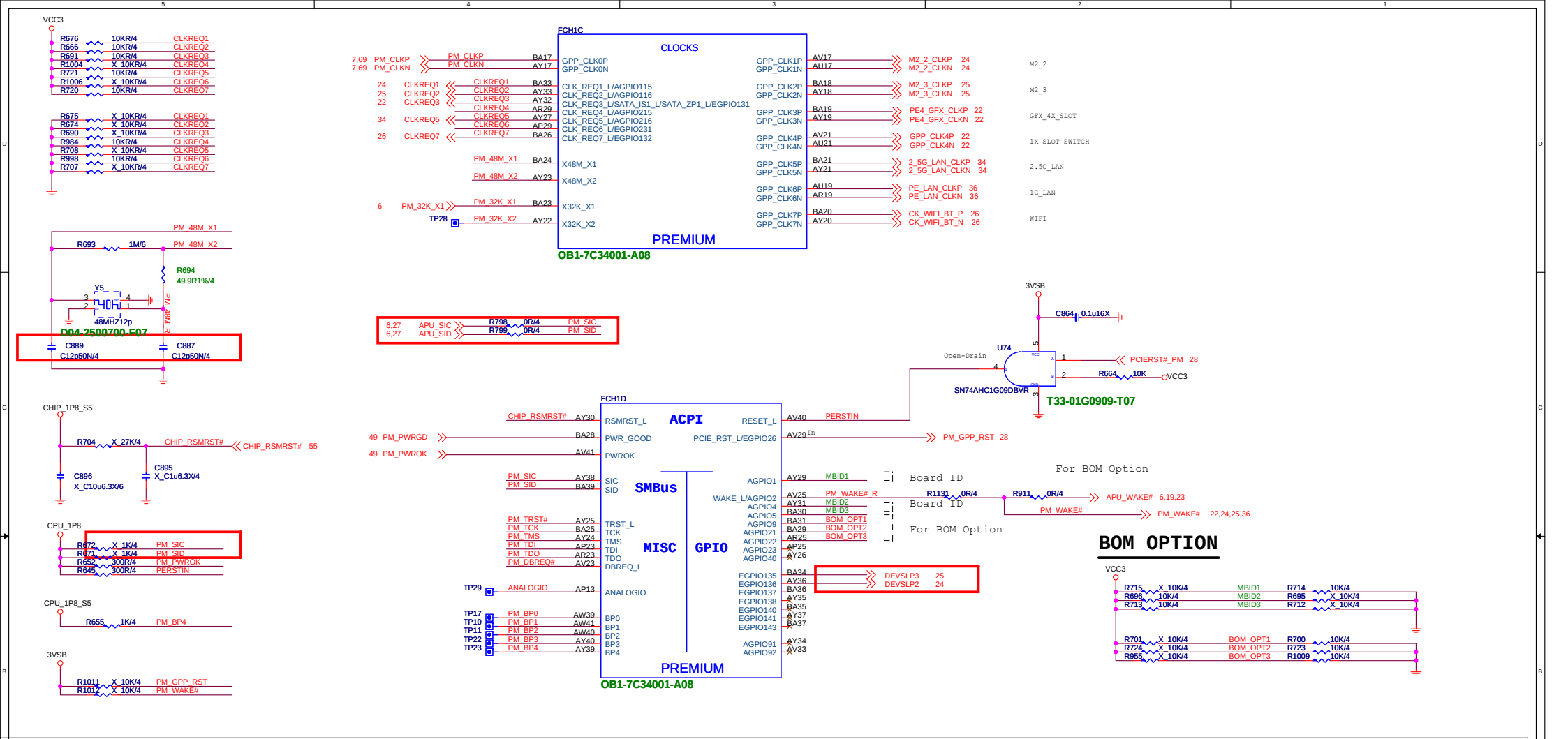
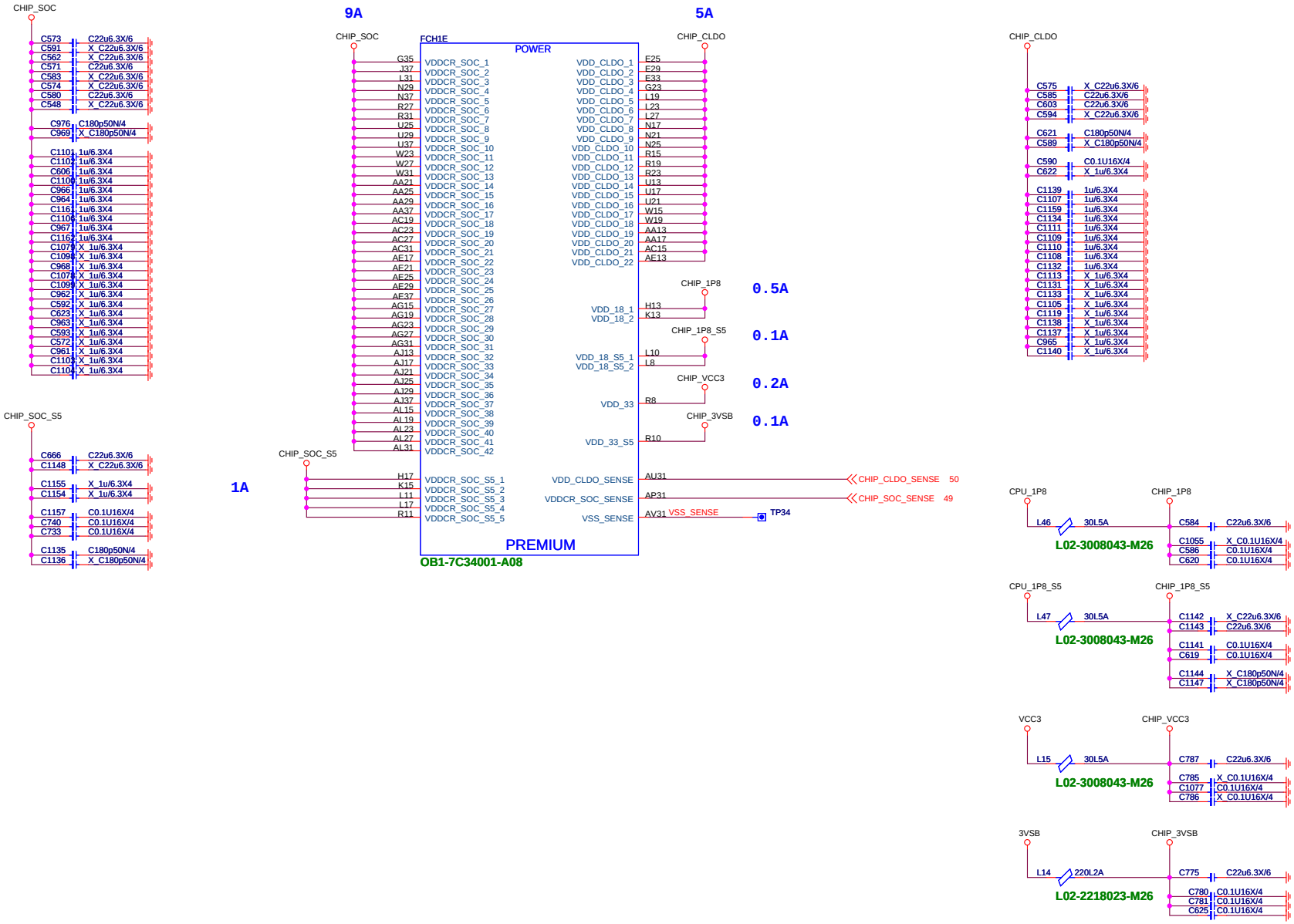


Close to FCH Power Pin



MICRO-STAR INT'L CO.,LTD

MS-7C35

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Custom	Promontory-Power	11

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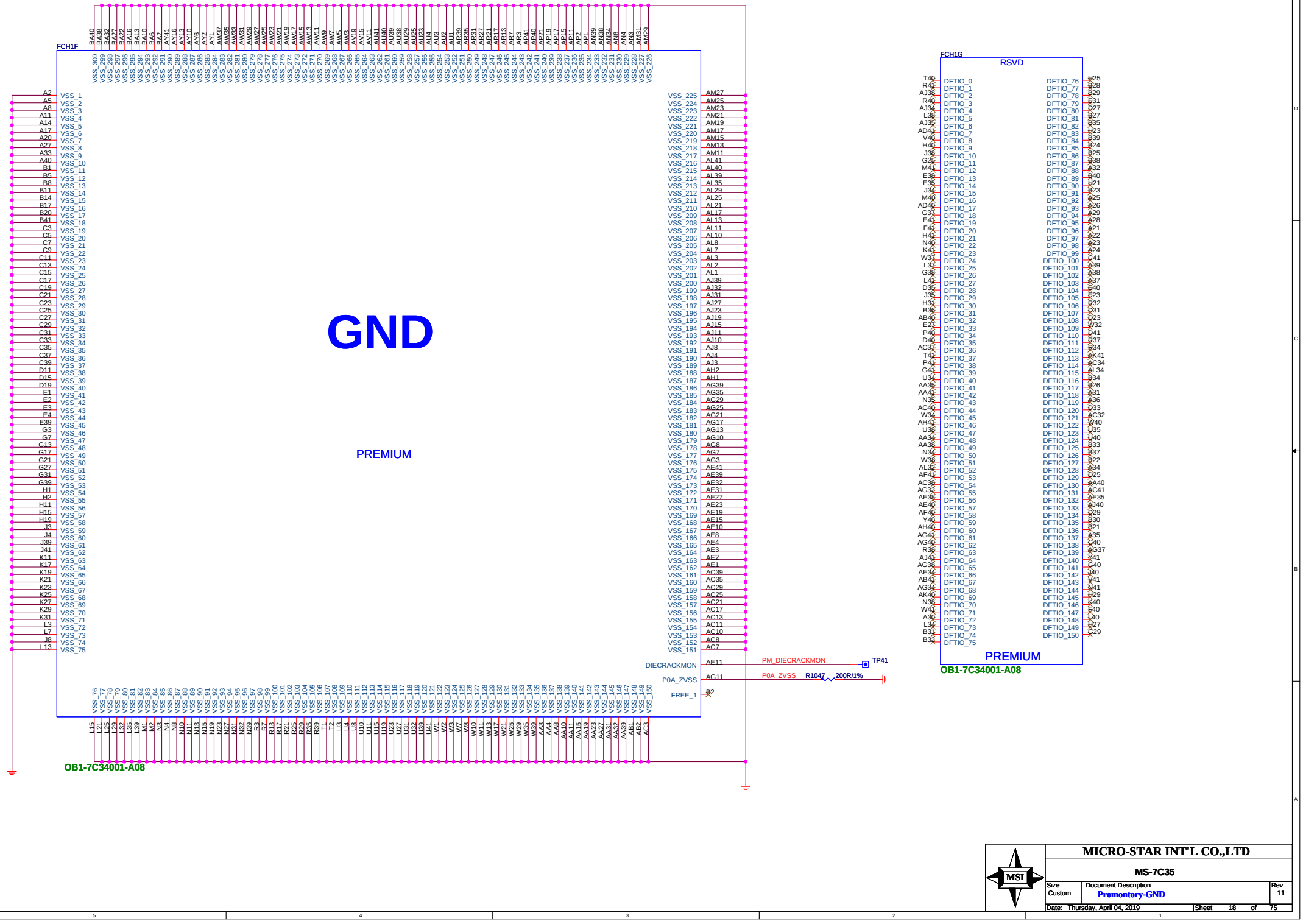

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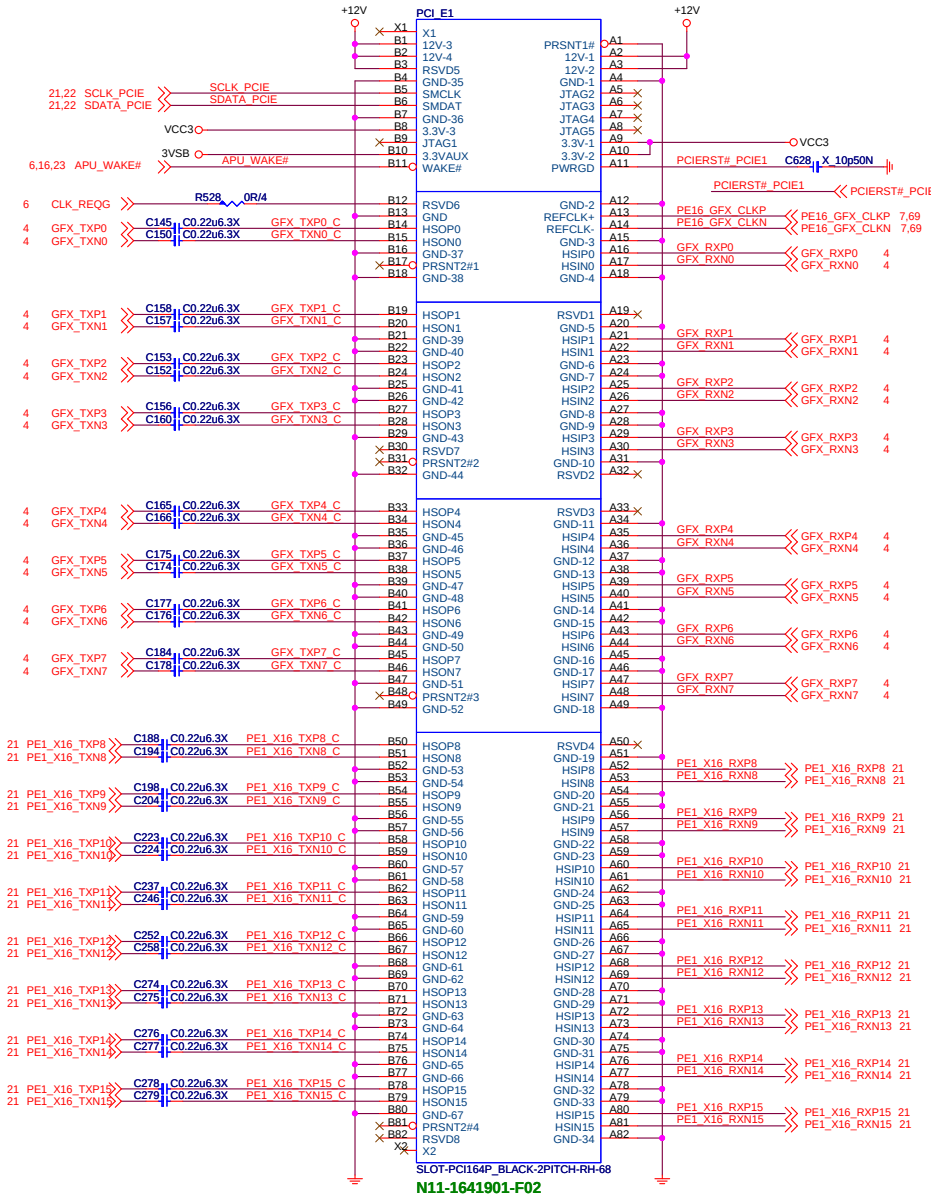
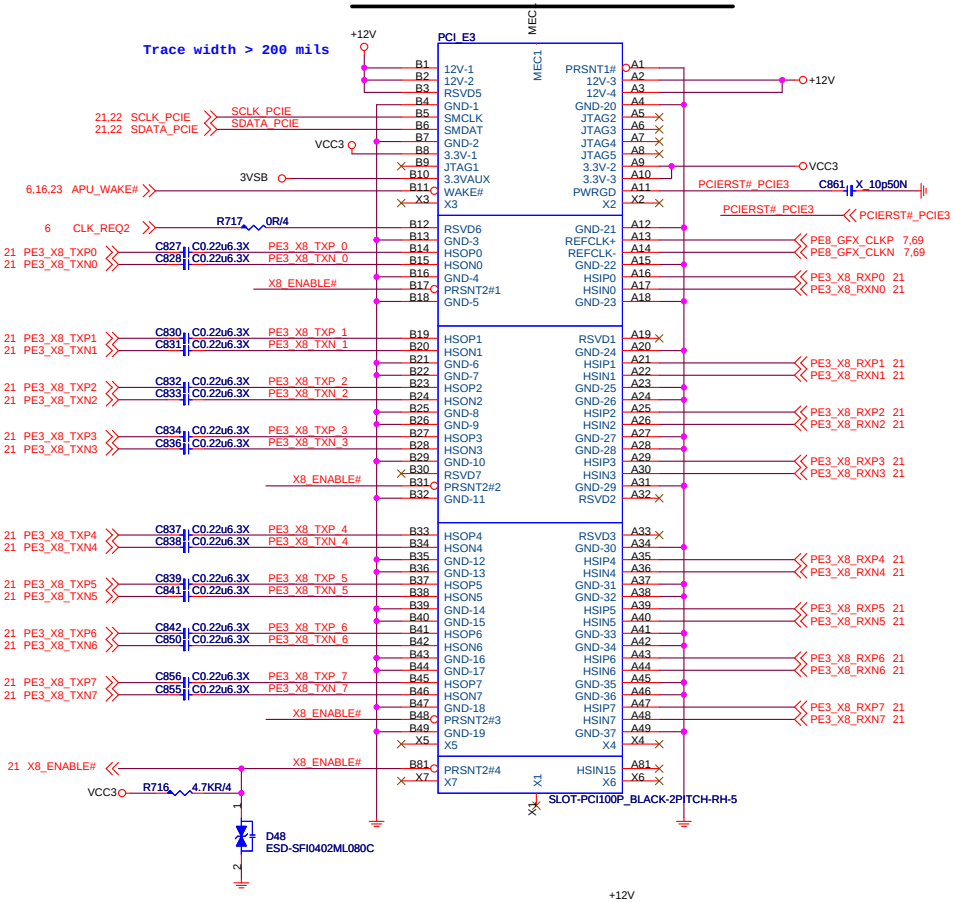
PCI EXPRESS x16 Slot

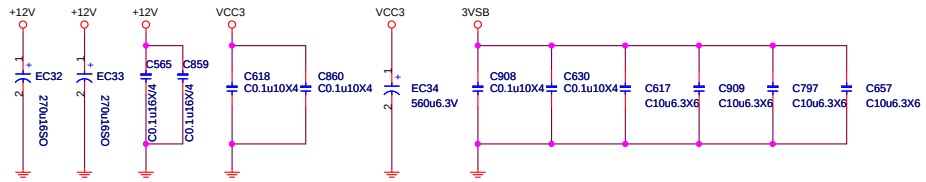
3.3V 3.0A
12V 5.5A

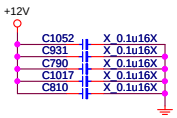


PCI EXPRESS x8 Slot

Trace width > 200 mils







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I²C Programming

Address assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	AD3	AD2	AD1	0	1=R, 0=W

For PCIE1 & PCIE2 & PCIE3

GL_SDATA0 R541 X_0R SDATA0 6,10,30,56,64,66,67,68,69

GL_SCLK0 R553 X_0R SCLK0 6,10,30,56,64,66,67,68,69

TX Libraty default

RX Library描构

RX Library描构

U61

PI3EQ16904GL

GFX_TXN11 C417 0.22u6.3X/4 GFX_TXN11_C → GL_GFX_TXN11_C C719 0.22u6.3X/4 → GL_GFX_TXN11 21

GFX_TXP11 C423 0.22u6.3X/4 GFX_TXP11_C → GL_GFX_TXP11_C C718 0.22u6.3X/4 → GL_GFX_TXP11 21

GFX_TXN10 C387 0.22u6.3X/4 GFX_TXN10_C → GL_GFX_TXN10_C C749 0.22u6.3X/4 → GL_GFX_TXN10 21

GFX_TXP10 C386 0.22u6.3X/4 GFX_TXP10_C → GL_GFX_TXP10_C C748 0.22u6.3X/4 → GL_GFX_TXP10 21

GFX_TXN9 C407 0.22u6.3X/4 GFX_TXN9_C → GL_GFX_TXN9_C C716 0.22u6.3X/4 → GL_GFX_TXN9 21

GFX_TXP9 C406 0.22u6.3X/4 GFX_TXP9_C → GL_GFX_TXP9_C C715 0.22u6.3X/4 → GL_GFX_TXP9 21

GFX_TXN8 C526 0.22u6.3X/4 GFX_TXN8_C → GL_GFX_TXN8_C C747 0.22u6.3X/4 → GL_GFX_TXN8 21

GFX_TXP8 C525 0.22u6.3X/4 GFX_TXP8_C → GL_GFX_TXP8_C C746 0.22u6.3X/4 → GL_GFX_TXP8 21

A0RX+ A0RX- A1RX+ A1RX- A2RX+ A2RX- A3RX+ A3RX-

A0TX+ A0TX- A1TX+ A1TX- A2TX+ A2TX- A3TX+ A3TX-

EQ0_GL1 EQ1_GL1 EQ2_GL1 FG0_GL1 FG1_GL1 SW1_GL1 → EQ0 EQ1 EQ2 FG0 FG1 SW1

SDA ← GL_SDATA0; SCL ← GL_SCLK0

AD1_GL1 AD2_GL1 AD3_GL1 → AD1 AD2 AD3

ENI2C ← ENI2C_GL

I2C_RESET# ← R531 X_4.7K/4

RXDET ← R601 X_4.7K/4

PRSNT# ← R567 4.7K/4

I2C_DONE

GND(EP)

VCC-1 VCC-2 VCC-3 VCC-4 VCC-5 VCC-6 VCC-7 VCC-8 VCC-9 VCC-10 ← VCC3

U59

PI3EQ16904GL

GFX_RXP8 C1246 0.22u6.3X/4 GFX_RXP8_C → GL_GFX_RXP8_C C707 0.22u6.3X/4 → GL_GFX_RXP8 21

GFX_RXN8 C1245 0.22u6.3X/4 GFX_RXN8_C → GL_GFX_RXN8_C C708 0.22u6.3X/4 → GL_GFX_RXN8 21

GFX_RXP9 C1250 0.22u6.3X/4 GFX_RXP9_C → GL_GFX_RXP9_C C742 0.22u6.3X/4 → GL_GFX_RXP9 21

GFX_RXN9 C1251 0.22u6.3X/4 GFX_RXN9_C → GL_GFX_RXN9_C C743 0.22u6.3X/4 → GL_GFX_RXN9 21

GFX_RXP10 C1253 0.22u6.3X/4 GFX_RXP10_C → GL_GFX_RXP10_C C709 0.22u6.3X/4 → GL_GFX_RXP10 21

GFX_RXN10 C1262 0.22u6.3X/4 GFX_RXN10_C → GL_GFX_RXN10_C C714 0.22u6.3X/4 → GL_GFX_RXN10 21

GFX_RXP11 C1256 0.22u6.3X/4 GFX_RXP11_C → GL_GFX_RXP11_C C744 0.22u6.3X/4 → GL_GFX_RXP11 21

GFX_RXN11 C1257 0.22u6.3X/4 GFX_RXN11_C → GL_GFX_RXN11_C C745 0.22u6.3X/4 → GL_GFX_RXN11 21

A0TX+ A0TX- A1TX+ A1TX- A2TX+ A2TX- A3TX+ A3TX-

A0RX+ A0RX- A1RX+ A1RX- A2RX+ A2RX- A3RX+ A3RX-

SDA ← GL_SDATA0; SCL ← GL_SCLK0

AD1_GL2 AD2_GL2 AD3_GL2 → AD1 AD2 AD3

ENI2C ← ENI2C_GL

I2C_RESET# ← R596 X_4.7K/4

RXDET ← R529 X_4.7K/4

PRSNT# ← R597 4.7K/4

I2C_DONE

GND(EP)

EQ0 EQ1 EQ2 FG0 FG1 SW1 → EQ0_GL2 EQ1_GL2 EQ2_GL2 FG0_GL2 FG1_GL2 SW1_GL2

VCC-1 VCC-2 VCC-3 VCC-4 VCC-5 VCC-6 VCC-7 VCC-8 VCC-9 VCC-10 ← VCC3

U95

PI3EQ16904GL

GFX_TXP12 C446 0.22u6.3X/4 GFX_TXP12_C → GL_GFX_TXP12_C C692 0.22u6.3X/4 → GL_GFX_TXP12 21

GFX_TXN12 C447 0.22u6.3X/4 GFX_TXN12_C → GL_GFX_TXN12_C C693 0.22u6.3X/4 → GL_GFX_TXN12 21

GFX_TXP13 C400 0.22u6.3X/4 GFX_TXP13_C → GL_GFX_TXP13_C C660 0.22u6.3X/4 → GL_GFX_TXP13 21

GFX_TXN13 C401 0.22u6.3X/4 GFX_TXN13_C → GL_GFX_TXN13_C C662 0.22u6.3X/4 → GL_GFX_TXN13 21

GFX_TXP14 C377 0.22u6.3X/4 GFX_TXP14_C → GL_GFX_TXP14_C C696 0.22u6.3X/4 → GL_GFX_TXP14 21

GFX_TXN14 C378 0.22u6.3X/4 GFX_TXN14_C → GL_GFX_TXN14_C C697 0.22u6.3X/4 → GL_GFX_TXN14 21

GFX_TXP15 C390 0.22u6.3X/4 GFX_TXP15_C → GL_GFX_TXP15_C C664 0.22u6.3X/4 → GL_GFX_TXP15 21

GFX_TXN15 C391 0.22u6.3X/4 GFX_TXN15_C → GL_GFX_TXN15_C C667 0.22u6.3X/4 → GL_GFX_TXN15 21

A0RX+ A0RX- A1RX+ A1RX- A2RX+ A2RX- A3RX+ A3RX-

A0TX+ A0TX- A1TX+ A1TX- A2TX+ A2TX- A3TX+ A3TX-

EQ0_GL3 EQ1_GL3 EQ2_GL3 FG0_GL3 FG1_GL3 SW1_GL3 → EQ0 EQ1 EQ2 FG0 FG1 SW1

SDA ← GL_SDATA0; SCL ← GL_SCLK0

AD1_GL3 AD2_GL3 AD3_GL3 → AD1 AD2 AD3

ENI2C ← ENI2C_GL

I2C_RESET# ← R1090 X_4.7K/4

RXDET ← R1092 X_4.7K/4

PRSNT# ← R1093 4.7K/4

I2C_DONE

GND(EP)

VCC-1 VCC-2 VCC-3 VCC-4 VCC-5 VCC-6 VCC-7 VCC-8 VCC-9 VCC-10 ← VCC3

U96

PI3EQ16904GL

GFX_RXP15 C1291 0.22u6.3X/4 GFX_RXN15_C → GL_GFX_RXN15_C C635 0.22u6.3X/4 → GL_GFX_RXN15 21

GFX_RXN15 C1290 0.22u6.3X/4 GFX_RXP15_C → GL_GFX_RXP15_C C634 0.22u6.3X/4 → GL_GFX_RXP15 21

GFX_RXP14 C1288 0.22u6.3X/4 GFX_RXN14_C → GL_GFX_RXN14_C C637 0.22u6.3X/4 → GL_GFX_RXN14 21

GFX_RXN14 C1293 0.22u6.3X/4 GFX_RXP14_C → GL_GFX_RXP14_C C636 0.22u6.3X/4 → GL_GFX_RXP14 21

GFX_RXP13 C1285 0.22u6.3X/4 GFX_RXN13_C → GL_GFX_RXN13_C C682 0.22u6.3X/4 → GL_GFX_RXN13 21

GFX_RXN13 C1289 0.22u6.3X/4 GFX_RXP13_C → GL_GFX_RXP13_C C681 0.22u6.3X/4 → GL_GFX_RXP13 21

GFX_RXP12 C1287 0.22u6.3X/4 GFX_RXN12_C → GL_GFX_RXN12_C C633 0.22u6.3X/4 → GL_GFX_RXN12 21

GFX_RXN12 C1281 0.22u6.3X/4 GFX_RXP12_C → GL_GFX_RXP12_C C632 0.22u6.3X/4 → GL_GFX_RXP12 21

A0TX+ A0TX- A1TX+ A1TX- A2TX+ A2TX- A3TX+ A3TX-

A0RX+ A0RX- A1RX+ A1RX- A2RX+ A2RX- A3RX+ A3RX-

SDA ← GL_SDATA0; SCL ← GL_SCLK0

AD1_GL4 AD2_GL4 AD3_GL4 → AD1 AD2 AD3

ENI2C ← ENI2C_GL

I2C_RESET# ← R1097 X_4.7K/4

RXDET ← R441 X_4.7K/4

PRSNT# ← R863 4.7K/4

I2C_DONE

GND(EP)

EQ0 EQ1 EQ2 FG0 FG1 SW1 → EQ0_GL4 EQ1_GL4 EQ2_GL4 FG0_GL4 FG1_GL4 SW1_GL4

VCC-1 VCC-2 VCC-3 VCC-4 VCC-5 VCC-6 VCC-7 VCC-8 VCC-9 VCC-10 ← VCC3

OPERATING MODE

VCC3 R588 4.7K/4 ENI2C_GL R582 X_4.7K/4

EQ FG SW

R574 4.7K/4 EQ0_GL1

R560 X_4.7K/4 EQ1_GL1

R524 4.7K/4 EQ2_GL1

R595 4.7K/4 FG0_GL1

R587 X_4.7K/4 FG1_GL1

R523 4.7K/4 SW1_GL1

ADDRESS SETTING

R530 4.7K/4 AD1_GL1

R546 X_4.7K/4 AD2_GL1

R540 4.7K/4 AD3_GL1

VCC3 C1037 10u6.3X6

C1038 C0.1u16X4

C1193 C0.1u16X4

C2296 X_C0.1u16X4

C2295 C0.1u16X4

C2298 X_C0.1u16X4

C2297 C0.1u16X4

C2300 X_C0.1u16X4

C2299 C0.1u16X4

EQ FG SW

R539 4.7K/4 EQ0_GL2

R544 X_4.7K/4 EQ1_GL2

R586 4.7K/4 EQ2_GL2

R527 4.7K/4 FG0_GL2

R526 X_4.7K/4 FG1_GL2

R591 4.7K/4 SW1_GL2

ADDRESS SETTING

R605 X_4.7K/4 AD1_GL2

R556 4.7K/4 AD2_GL2

R571 4.7K/4 AD3_GL2

VCC3 C1129 10u6.3X6

C1244 C0.1u16X4

C1194 C0.1u16X4

C2302 X_C0.1u16X4

C2301 C0.1u16X4

C2304 C0.1u16X4

C2303 X_C0.1u16X4

C2306 X_C0.1u16X4

C2305 C0.1u16X4

EQ FG SW

R1057 4.7K/4 EQ0_GL3

R1059 X_4.7K/4 EQ1_GL3

R1054 4.7K/4 EQ2_GL3

R1055 4.7K/4 FG0_GL3

R1056 X_4.7K/4 FG1_GL3

R1058 4.7K/4 SW1_GL3

ADDRESS SETTING

R1083 4.7K/4 AD1_GL3

R1087 4.7K/4 AD2_GL3

R1077 X_4.7K/4 AD3_GL3

VCC3 C549 10u6.3X6

C536 C0.1u16X4

C520 X_C0.1u16X4

C510 C0.1u16X4

C511 C0.1u16X4

C514 C0.1u16X4

C519 X_C0.1u16X4

C537 C0.1u16X4

C538 X_C0.1u16X4

EQ FG SW

R1071 4.7K/4 EQ0_GL4

R1073 X_4.7K/4 EQ1_GL4

R1068 4.7K/4 EQ2_GL4

R1069 4.7K/4 FG0_GL4

R1070 X_4.7K/4 FG1_GL4

R1075 4.7K/4 SW1_GL4

ADDRESS SETTING

R1078 X_4.7K/4 AD1_GL4

R1091 4.7K/4 AD2_GL4

R1079 X_4.7K/4 AD3_GL4

VCC3 C544 10u6.3X6

C523 X_C0.1u16X4

C521 X_C0.1u16X4

C540 X_C0.1u16X4

C539 C0.1u16X4

C506 C0.1u16X4

C541 C0.1u16X4

C507 C0.1u16X4

C512 C0.1u16X4

	AD3	AD2	AD1	Address	
GL1	0	1	0	E1	E0
GL2	0	0	1	E3	E2
GL3	1	0	0	F1	F0
GL4	1	0	1	F3	F2

MICRO-STAR INT'L CO.,LTD

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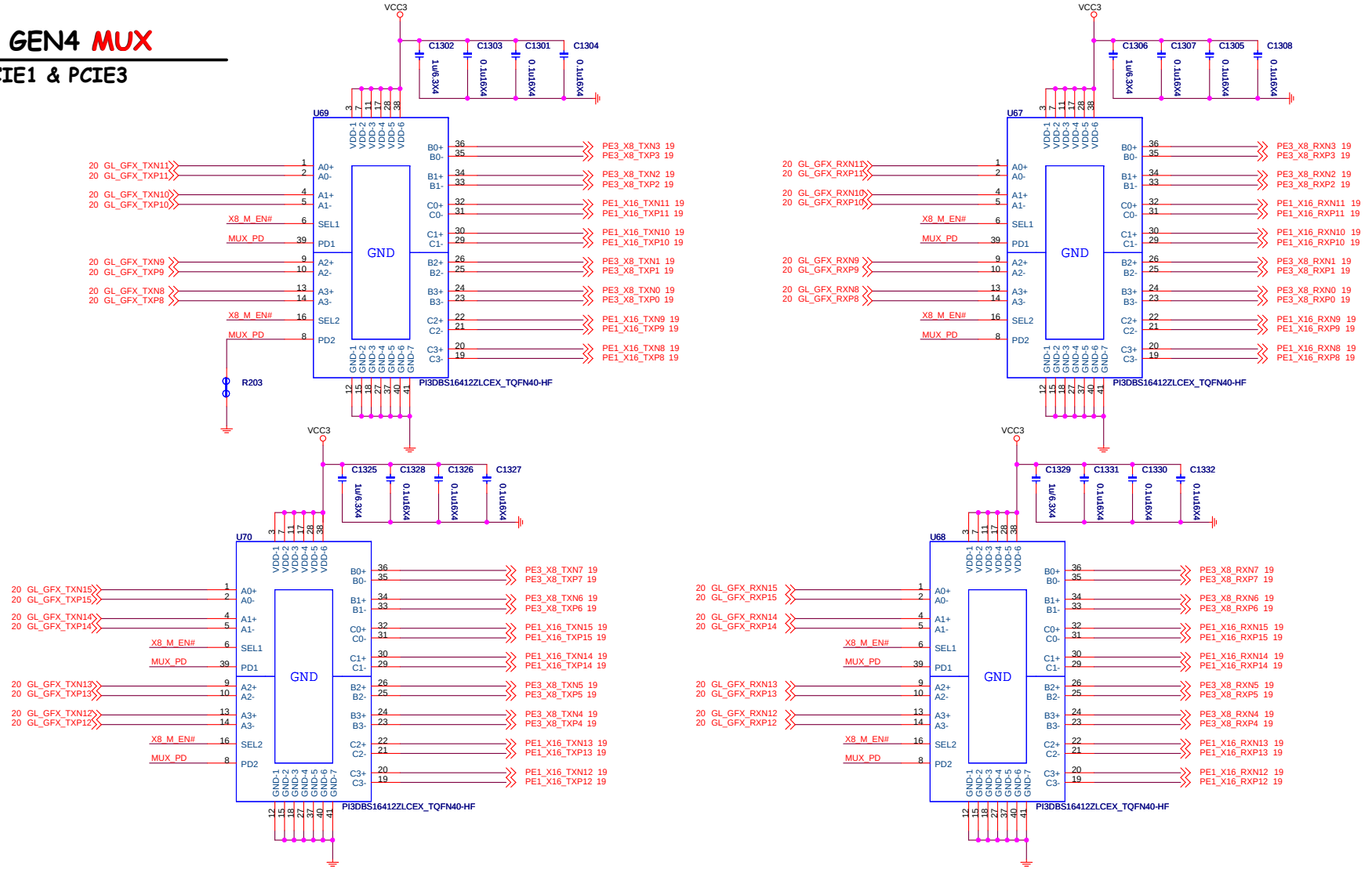
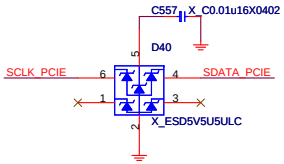
PCIE GEN4 MUX

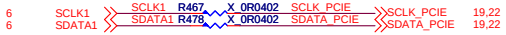
For PCIE1 & PCIE3



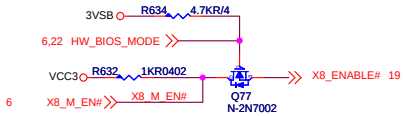
SMBus separate circuit

SMB_SEL
GPIO Default High





PCIE Lanes control circuit



	PCIE_CNTL	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0

MICRO-STAR INT'L CO.,LTD

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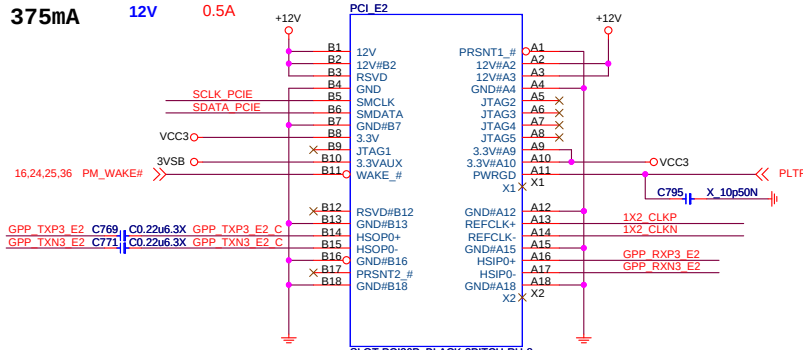
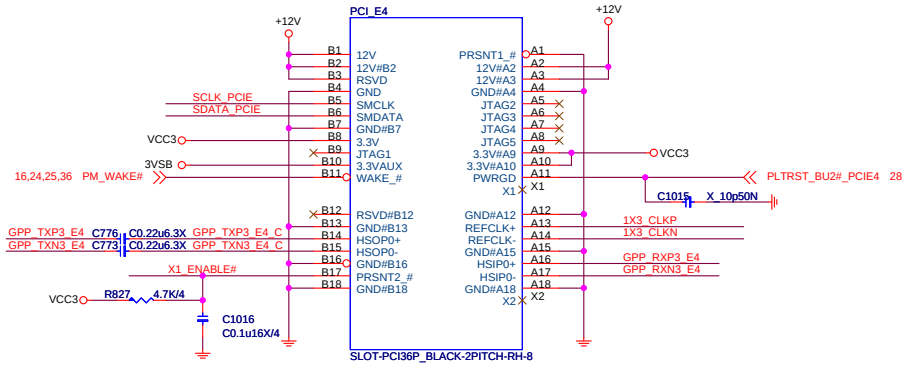
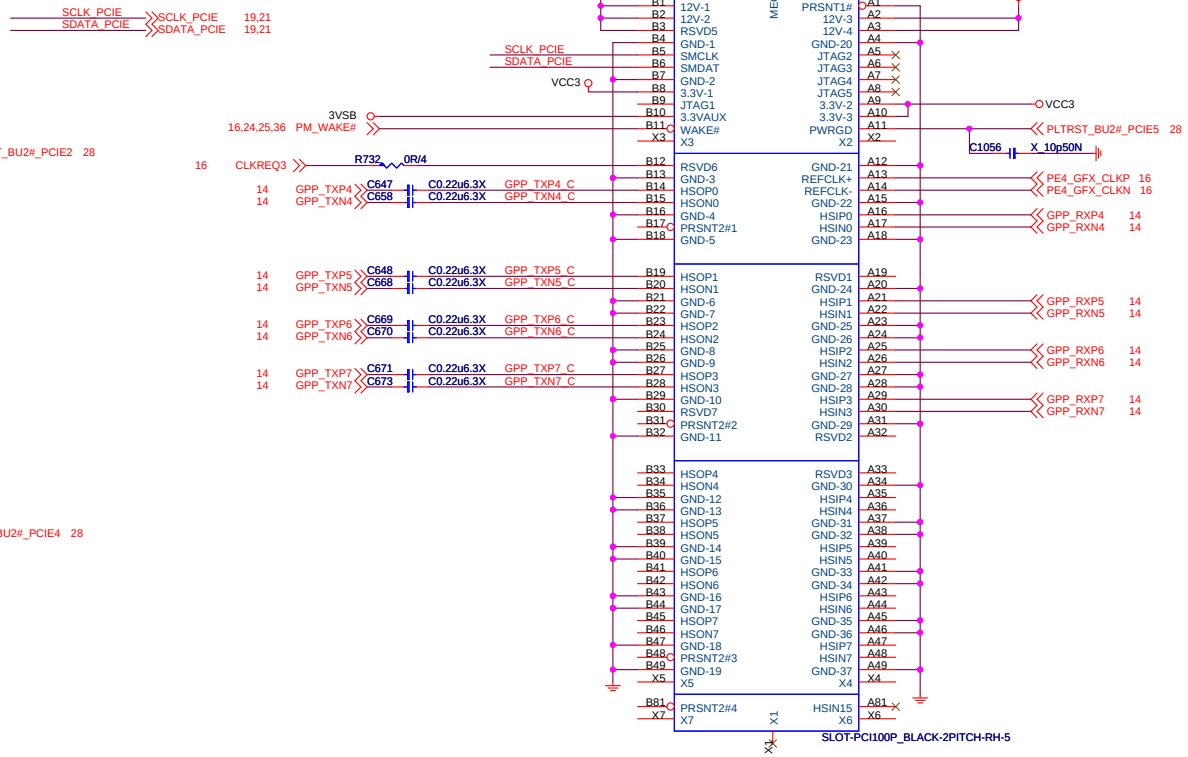
PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V 3.0A
12V 0.5A

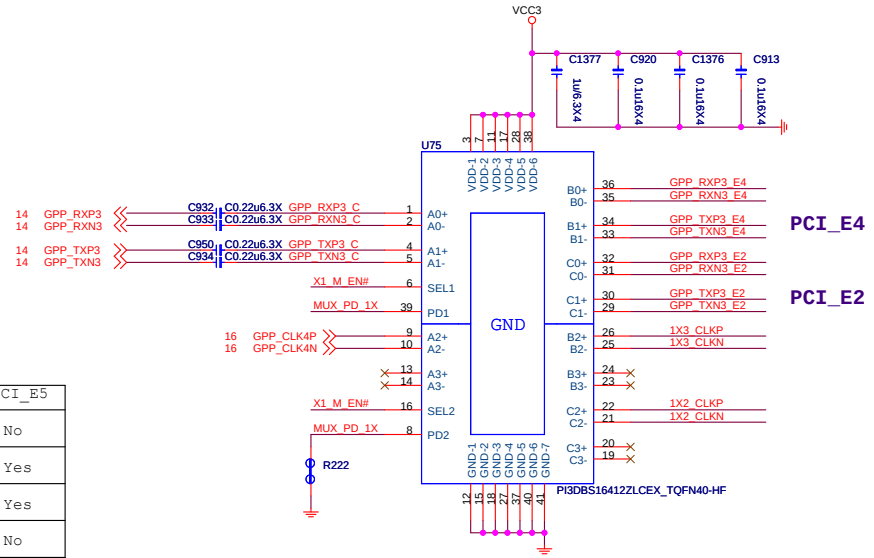
Trace width > 200 mils

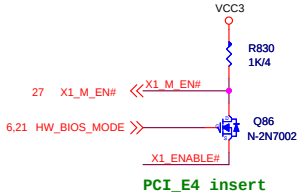






Footprint:SLOT_PCIEXP100_5





	HW_BIOS_MODE	X1_M_EN#	X1_ENABLE#	PCI_E3	PCI_E5
PCI_E3 IN	1	1	1	Yes	No
PCI_E5 IN	1	0	0	No	Yes
ALL IN	1	0	0	No	Yes
PCI_E3 IN	0	1	1	Yes	No
PCI_E5 IN	0	1	0	Yes	No
ALL IN	0	1	0	Yes	No

MICRO-STAR INT'L CO.,LTD

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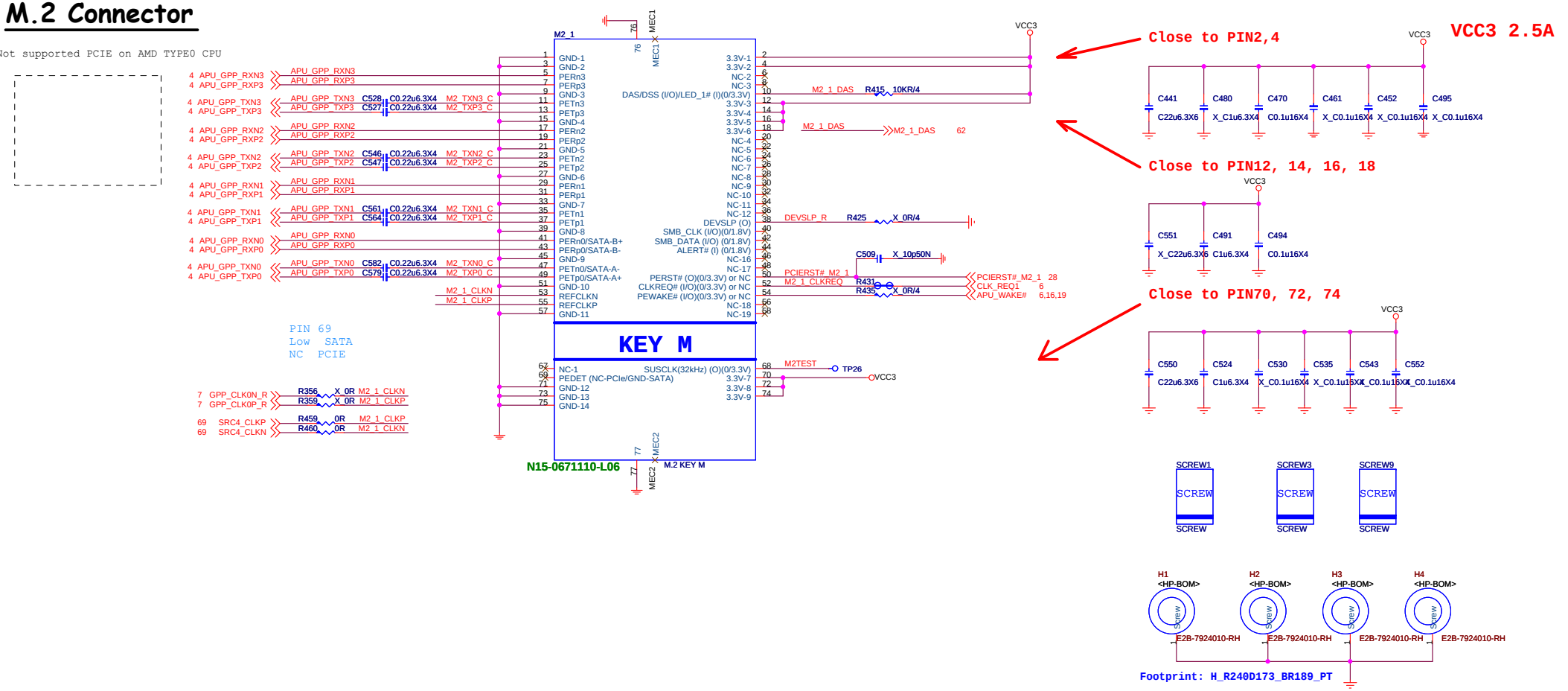
M.2 Connector

Not supported PCIE on AMD TYPE0 CPU



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Size: Custom	Document Description: M.2_1 Connector
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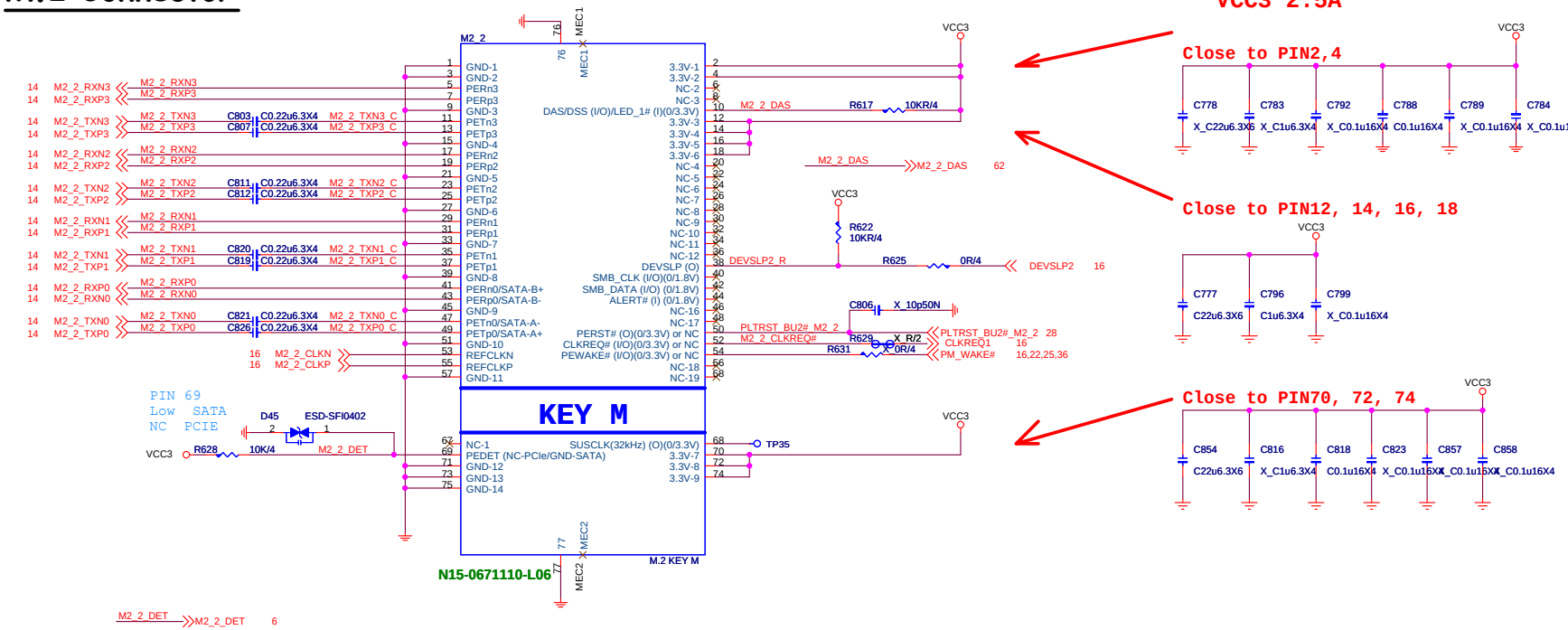
M.2 Connector

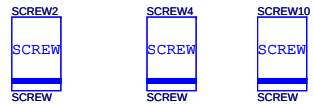


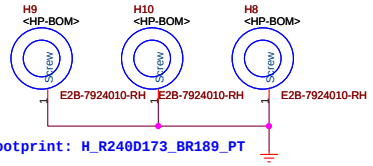
VCC3 2.5A

Close to PIN2,4

Close to PIN12, 14, 16, 18

Close to PIN70, 72, 74





Footprint: H_R240D173_BR189_PT

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Size: Custom	Document Description: M2_2 Connector	Rev: 11
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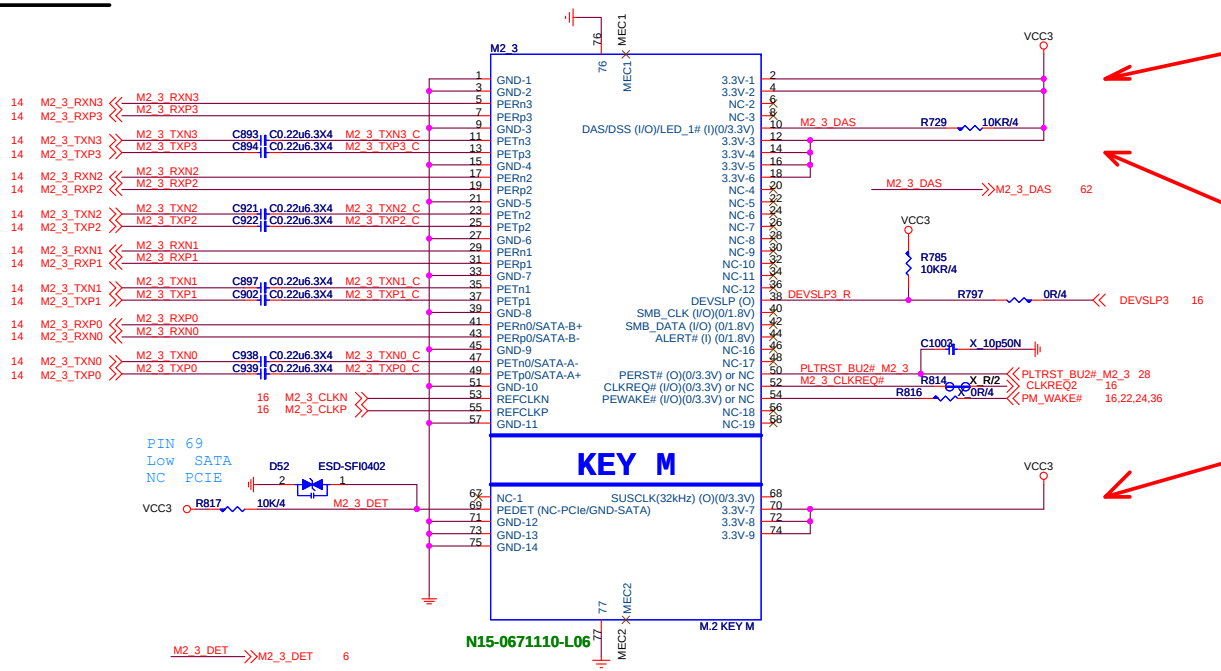
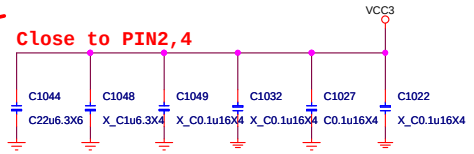
M.2 Connector

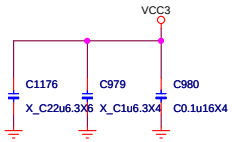


VCC3 2.5A

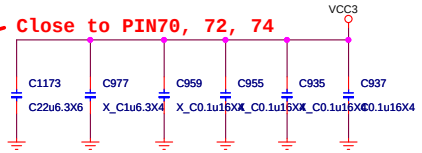
Close to PIN2,4

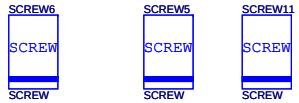


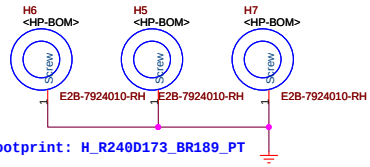
Close to PIN12, 14, 16, 18



Close to PIN70, 72, 74







Footprint: H_R240D173_BR189_PT

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1.1A

EMI

15 PM_USB9+ — PM_USB9+
15 PM_USB9- — PM_USB9-

D7 ESD-ESD5V5U5ULC-HF
6 → 4 PM_USB9+
1 → 3 PM_USB9-

NEAR CONNECTOR

3VSB — C77 X_0.1u16X4

ATX_5VSB
R54 47K/4
3VSB
R86 47K/4
Q9 NN-2N7002D
G2 D2 BT_DISABLE_L#
D1
27 WIFI_BTDIS# — WIFI_BTDIS# G1
S2
S1

ATX_5VSB
R53 47K/4
Q8 NN-2N7002D
G2 D2 WIFI_DISABLE_L#
D1
WIFI_BTDIS# G1
S2
S1

COVER1
VR Cover
X1
X2
X_E21-4437010-RH

Notice FOOTPRINT

Wireless1
Wireless
Wireless

M2_WIFI1 MEC2

	1 GND-1	2	3.3V-1
PM_USB9+	3 USB_D+	4	3.3V-2
PM_USB9-	5 USB_D-	6	LED1#
	7 GND-11	8	PCM_CLK / I2S SCK
	9 SDIO CLK	10	PCM_SYNC / I2S WS
	11 SDIO CMD	12	PCM_IN / I2S SD_IN
	13 SDIO DATA0	14	PCM_OUT / I2S SD_OUT
	15 SDIO DATA1	16	LED2#
	17 SDIO DATA2	18	GND-2
	19 SDIO DATA3	20	UART WAKE#
	21 SDIO WAKE#	22	UART RXD
	23 SDIO RESET#		

3VSB
C79 1u/6.3X/4
C83 10u6.3X6
C78 0.01u16X4

KEY E

	33 GND-10	32	UART TXD
14 GPP_TXP0 — 0.1u16X4 C111 GPP_TXP0_C	35 PETp0	34	UART CTS
14 GPP_TXN0 — 0.1u16X4 C113 GPP_TXN0_C	37 PETn0	36	UART RTS
	39 GND-9	38	VENDOR DEFINED-1
14 GPP_RXP0	41 PERp0	40	VENDOR DEFINED-2
14 GPP_RXN0	43 PERn0	42	VENDOR DEFINED-3
	45 GND-8	44	COEX3
16 CK_WIFI_BT_P	47 REFCLKP0	46	COEX2
16 CK_WIFI_BT_N	49 REFCLKN0	48	COEX1
	51 GND-7	50	SUSCLK — WIFI_BT_RTCCLK 6
16 CLKREQ7 — R112 — CLKREQ#WIFI	53 CLKREQ0#	52	PERST0# — PCIERST#_WIFI — PCIERST#_WIFI 28
27,34,36 LAN_WAKE#	55 PEWAKE0#	54	W_DISABLE2# — BT_DISABLE_L# R88 3.3K 3VSB
	57 GND-6	56	W_DISABLE1# — WIFI_DISABLE_L# R85 3.3K
	59 RESERVED / PETp1	58	I2C DATA
	61 RESERVED / PETn1	60	I2C CLK
	63 GND-5	62	ALERT#
	65 RESERVED / PERp1	64	RESERVED
	67 RESERVED / PERn1	66	UIM_SWP / PERST1#
	69 GND-4	68	UIM_POWER_SNK / CLKREQ1#
	71 RESERVED / REFCLKP1	70	UIM_POWER_SRC/GPIO1 / PEWAKE1#
	73 RESERVED / REFCLKN1	72	3.3V-3 — 3VSB
	75 GND-3	74	3.3V-4 — C76 0.01u16X4, C75 1u/6.3X/4, C73 10u6.3X6

SLOT-NGFFCARD67P_BLACK-HF-46
MEC1

SCREW8 SCREW
SCREW7 SCREW

3VSB
C90 X_10u6.3X6
close to pin2

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

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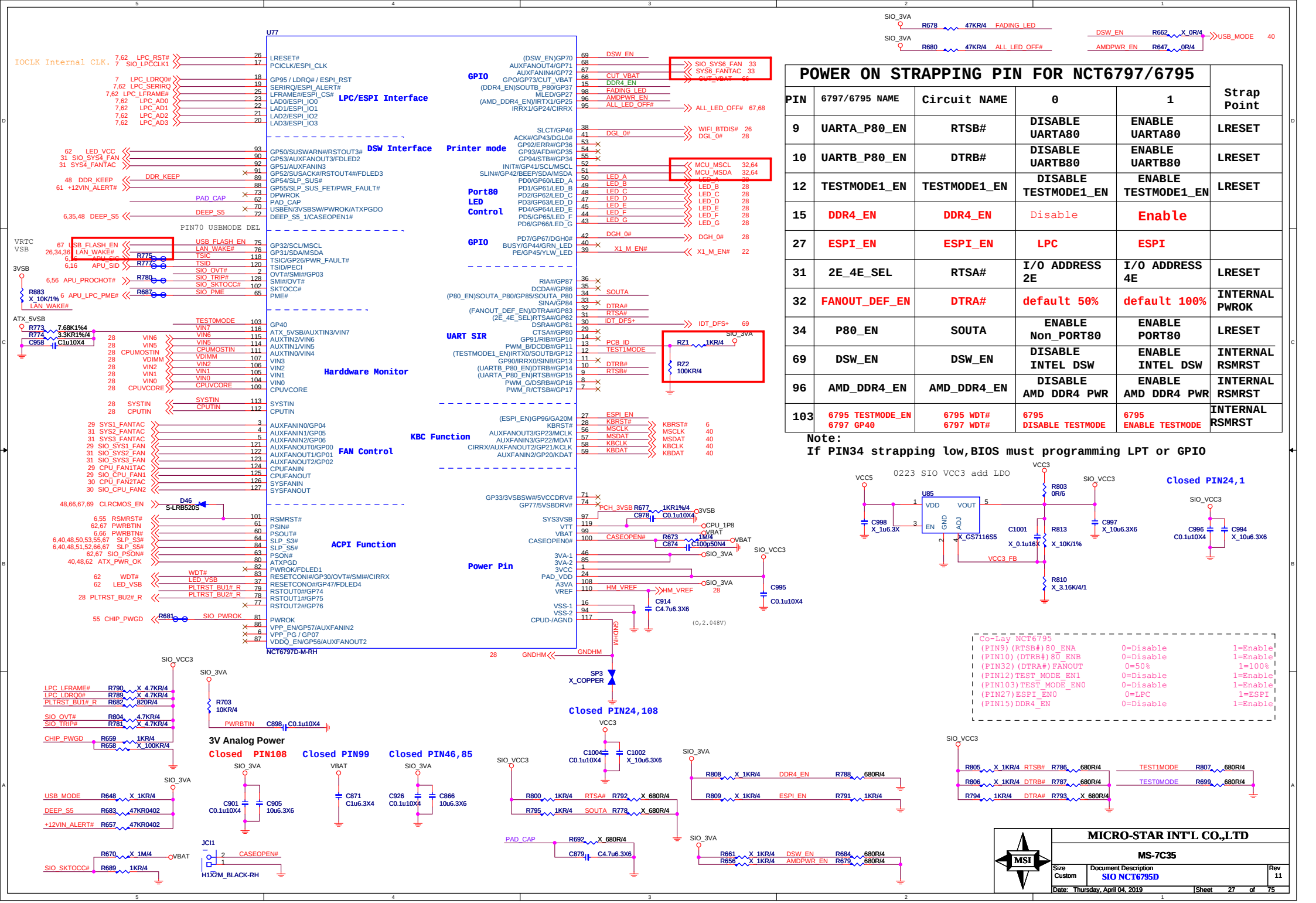

POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TESTMODE1_EN	ENABLE TESTMODE1_EN	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMD_DDR4_EN	AMD_DDR4_EN	DISABLE AMD DDR4 PWR	ENABLE AMD DDR4 PWR	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

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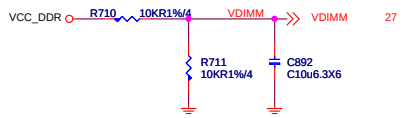
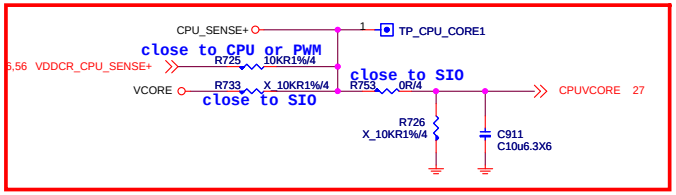
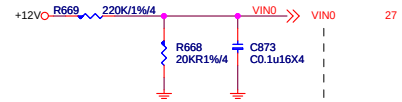
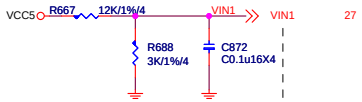
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

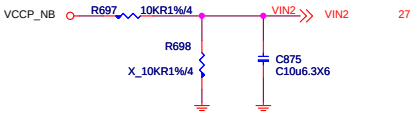




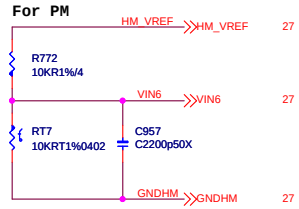


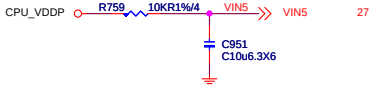


Power Fault detect through VIN0,VIN1

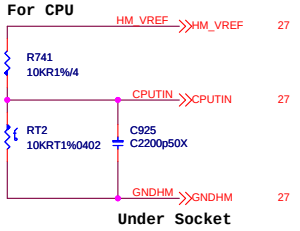


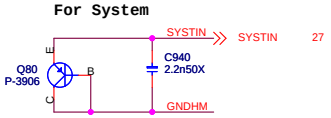
Inform BIOS disable VIN2 with Power Fault

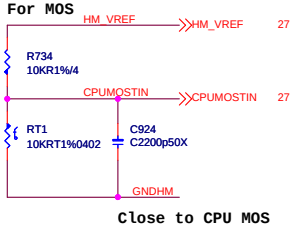




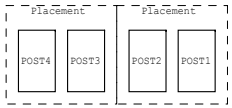
TEMP SENSOR







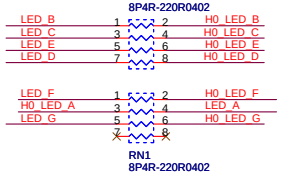
DEBUG LED

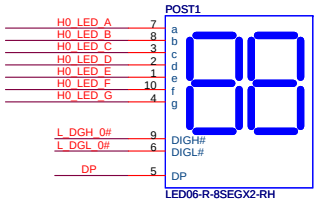


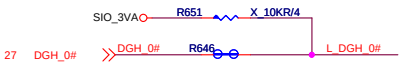
27 LED_A
27 LED_B
27 LED_C
27 LED_D
27 LED_E
27 LED_F
27 LED_G

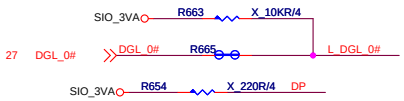
Placement ）璀癸
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)

Debug LED OFF BIOS control

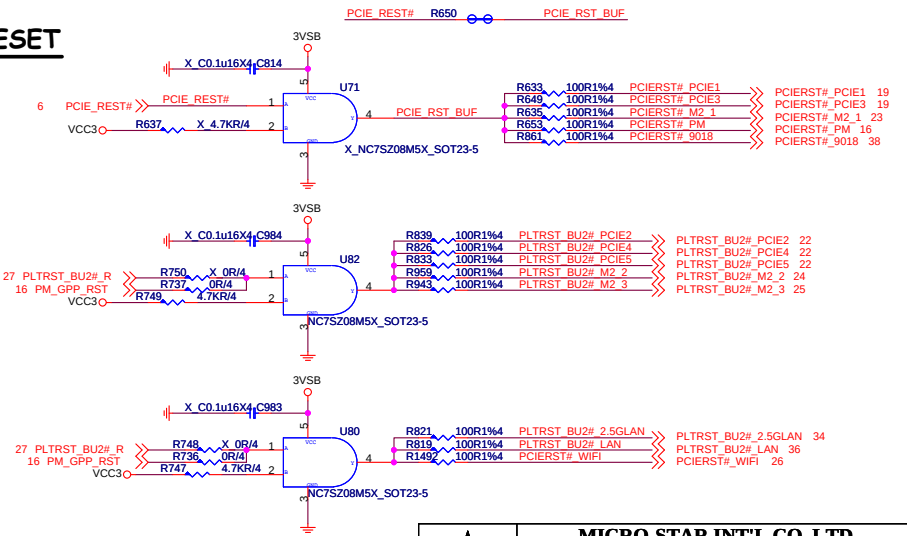








RESET



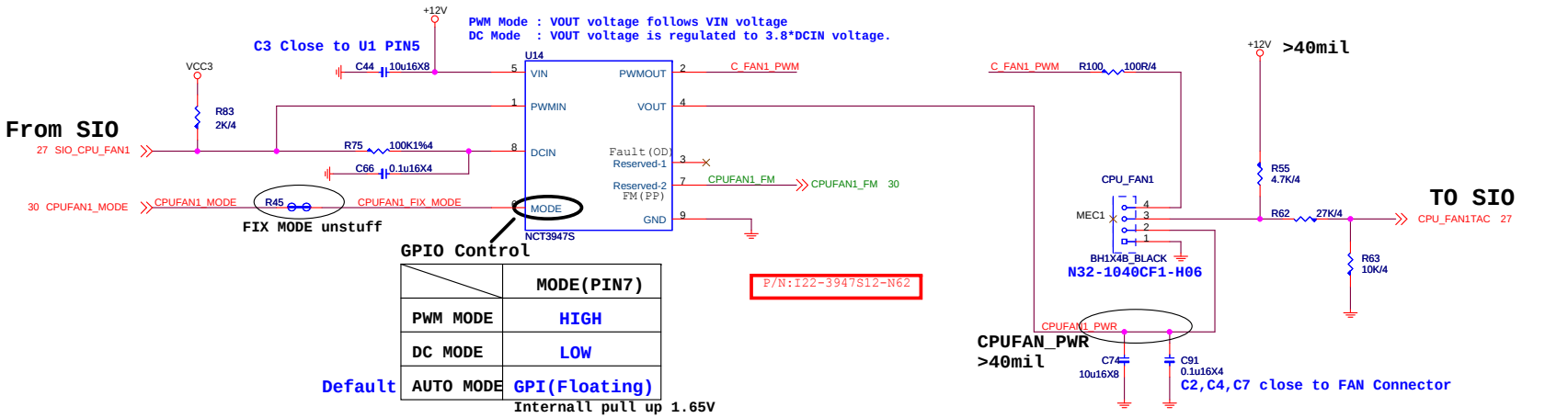
Co-lay FCH Reset for meet FCH sequence. See 55553

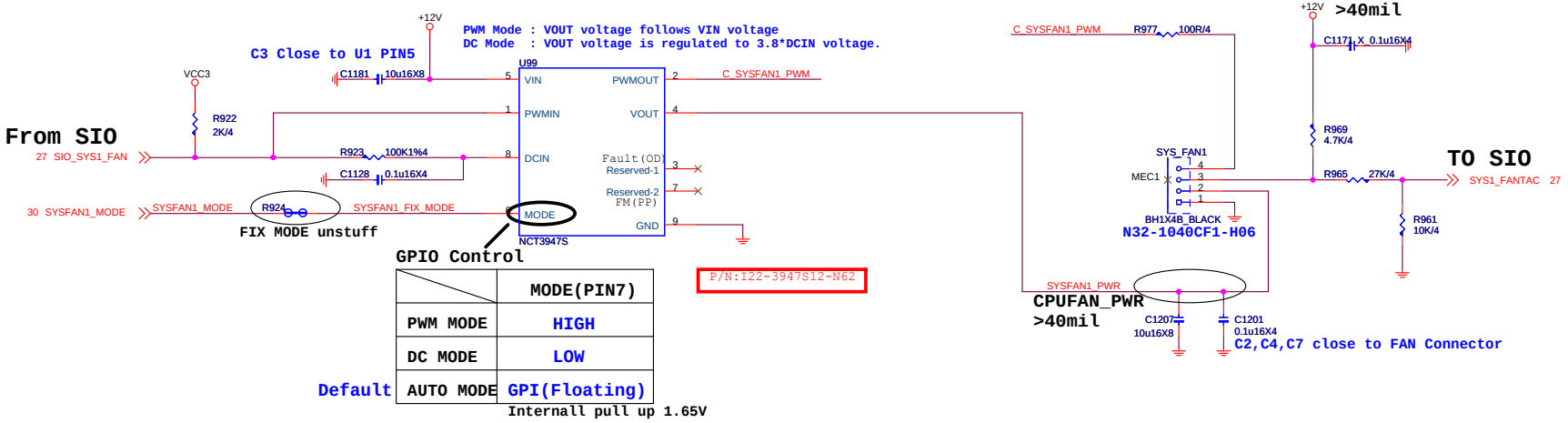
MICRO-STAR INT'L CO.,LTD

MS-7C35

Size: Custom | Document Description: HW monitor/Debug LED/NCT7718 | Rev: 11

Date: Tuesday, April 09, 2019 | Sheet 28 of 75

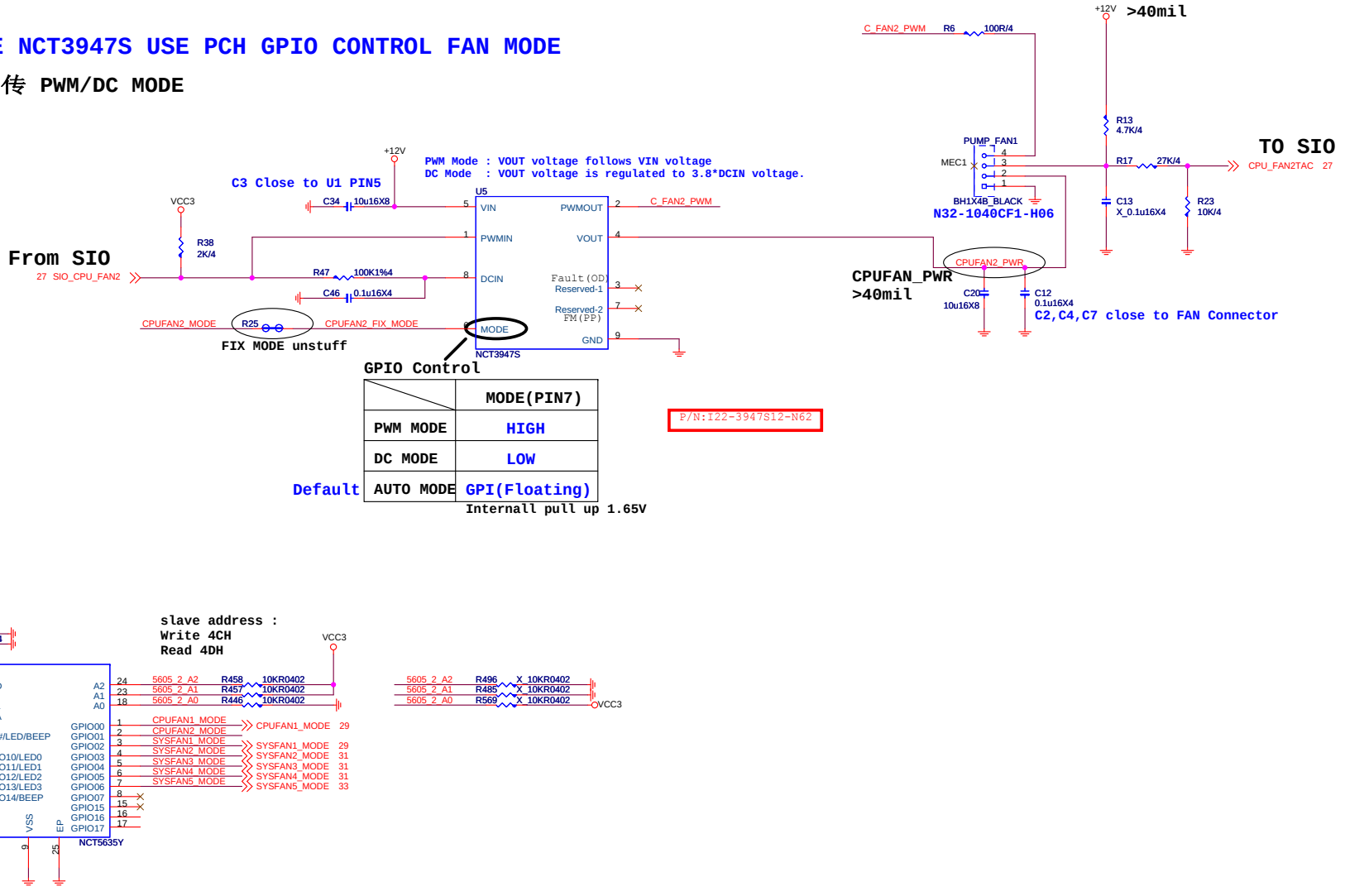




MICRO-STAR INT'L CO.,LTD	
MS-7C35	
Size: Custom	Document Description: CPU/SYS FAN X2 TYPE J
Rev: 11	
Date: Wednesday, March 27, 2019	Sheet 29 of 75

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち侍 PWM/DC MODE



1. GENERAL DESCRIPTION

20150722

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W

R/W: 0 = Write 39H, 1 = Read 38H

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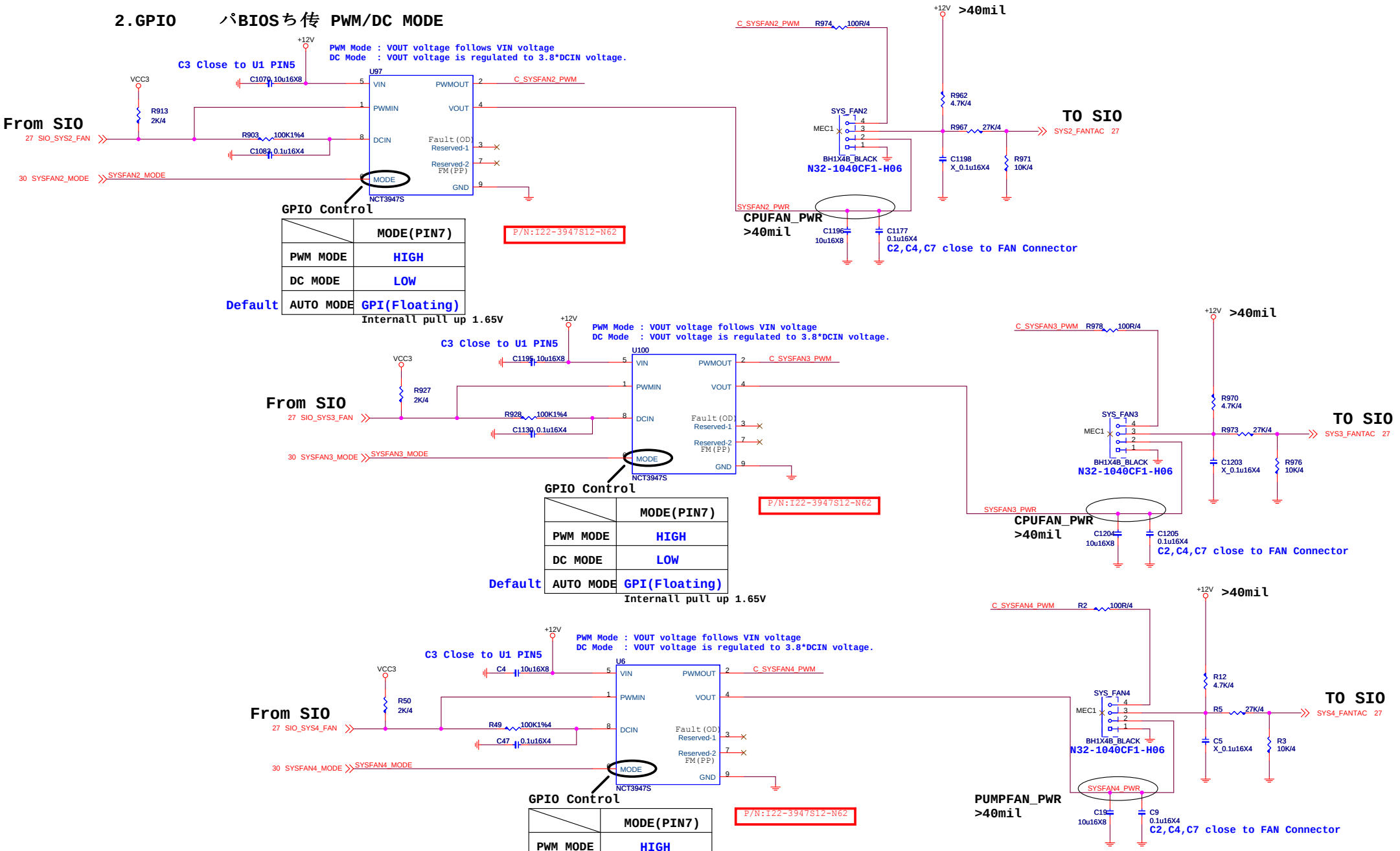
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち伝 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Size	Custom
Document Description	SYS FAN X3 TYPE K
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MICRO-STAR INT'L CO.,LTD

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PUSH-PULL

SIO_SYS5_FAN R779 100K1%4

SIO_SYS5_FAN >> SIO_SYS5_FAN 33

SYS5_FANTAC >> SYS5_FANTAC 33

NCT7802Y to address 50h

VCC3

R746 X_2.2K/4

R754 2.2K/4

U83

15 FANIN3/GPIO5
14 FANCTL2/GPIO4
13 FANIN2/GPIO3
12 FANCTL1/GPIO2
11 FANIN1/GPIO1

16 FANCTL3/GPIO6
17 GND
18 VCORE
7802_A_VSEN3 19 TD2-/TR3/VSEN3
7802_A_VSEN2 20 TD2+/TR2/VSEN2
21 EP

SCL 10 NCT7802_A_SMBCLK
SDA 9 NCT7802_A_SMBDAT
T_CRIT#/BEEP 8
ALERT#/SMI# 7
RESET# 6

1 TD1-/VREF
2 TD1+/TR1/VSEN1
3 VCC
4 VTT
5 PECI

NCT7802Y-HF

CHIP_SOC R738 10K/1%4 7802_A_VSEN2
R743 X_10K/1%4
C953 10u6.3X6

CHIP_CLDO R739 10K/1%4 7802_A_VSEN3
R744 X_10K/1%4
C954 10u6.3X6

CPU_1P8 R756 10K/1%4 7802_A_VSEN1
R767 10K/1%4
C973 10u6.3X6

7802_A_VSEN1
TP24
C906 0.1u/16X/4
C982 1u6.3X4

VCC3

VCC3 LED_VCC5

U106

NCT7802_A_SMBDAT 3 SDAA VCCA 8 VCC3
NCT7802_A_SMBCLK 2 SCLA VCCB 6 MCU_MSDA
SDAB 7 MCU_MSCL
EN GND 4
5

TCA9509DGKR_MSOP8-RH

VCC3 R3362 10K1%/4

C2116 0.1u16X4

LED_VCC5

R3363 2.2K/4

MCU_MSDA 27,64
MCU_MSCL 27,64

R3364 2.2K/4

LED_VCC5

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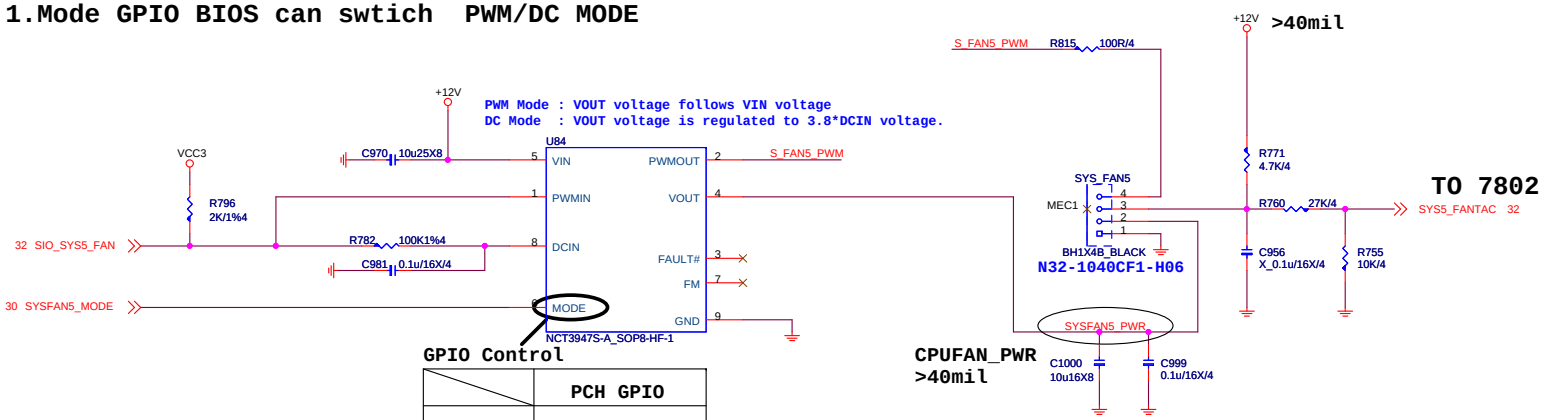
MS-7C35		
Size: Custom	Document Description: SYS FAN X3 TYPE K	Rev: 11
Date: Thursday, April 04, 2019	Sheet 32 of 75	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

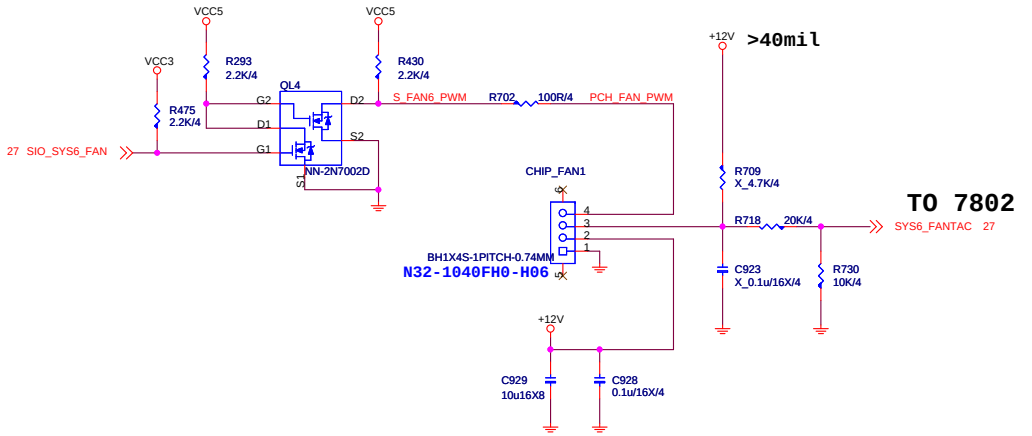


GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

CPUFAN_PWR >40mil



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MS-7C35

Size	Document Description	Rev
Custom	SYS FAN X3 TYPE K	11

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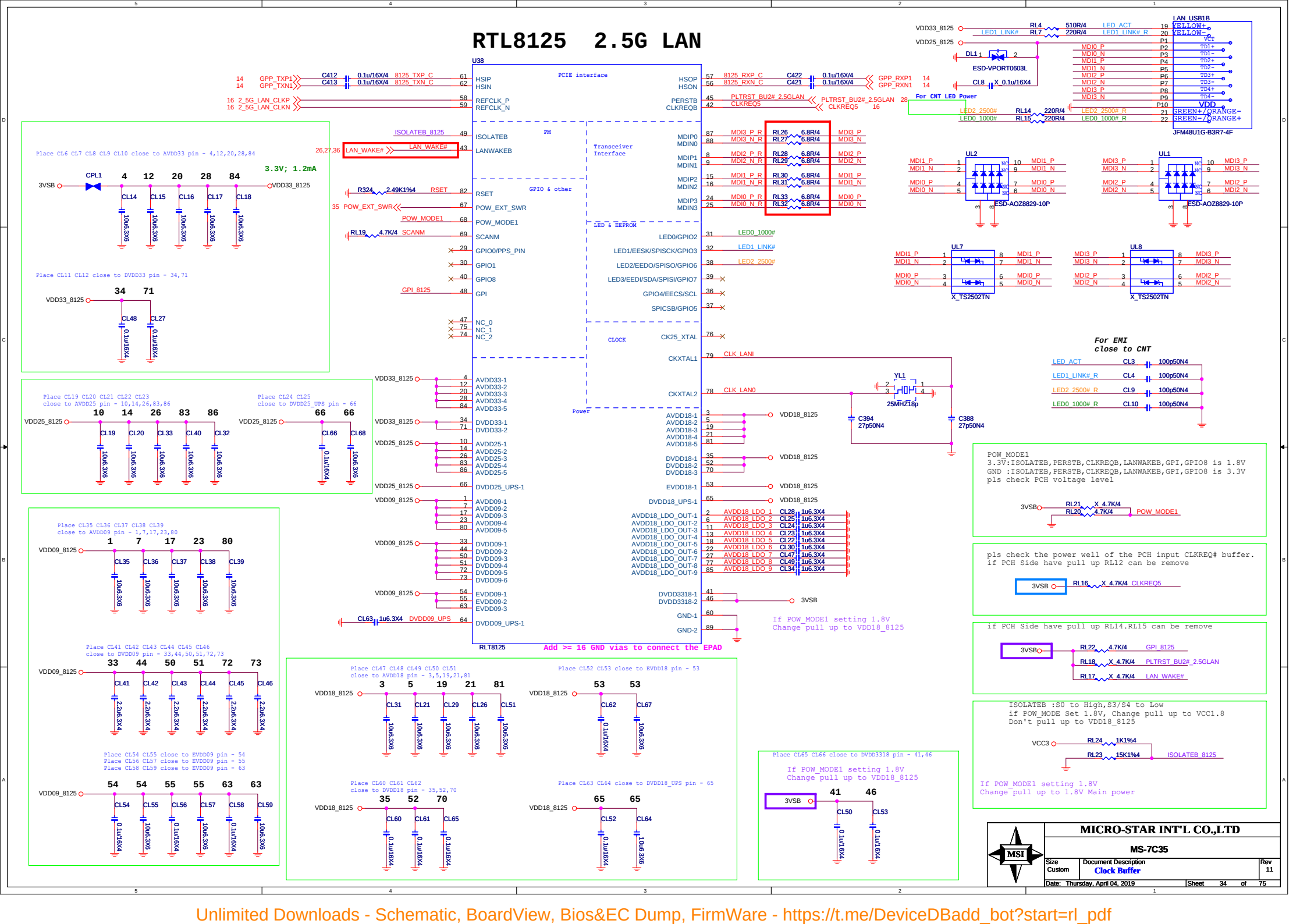
RTL8125 2.5G LAN



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MS-7C35	
Size: Custom	Document Description: Clock Buffer
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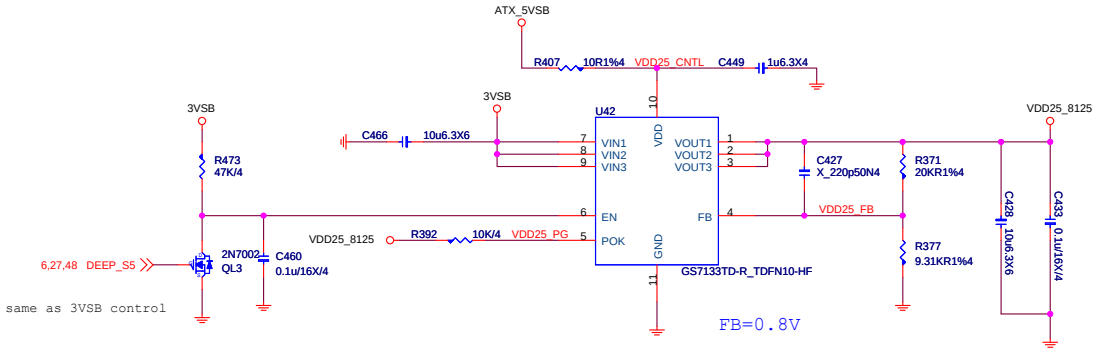
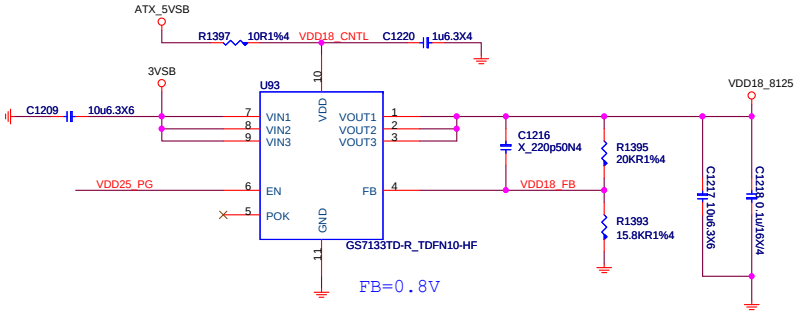
2.5V; 0.2291A

(3.3V-2.5V)*(0.2291A)=0.18328W

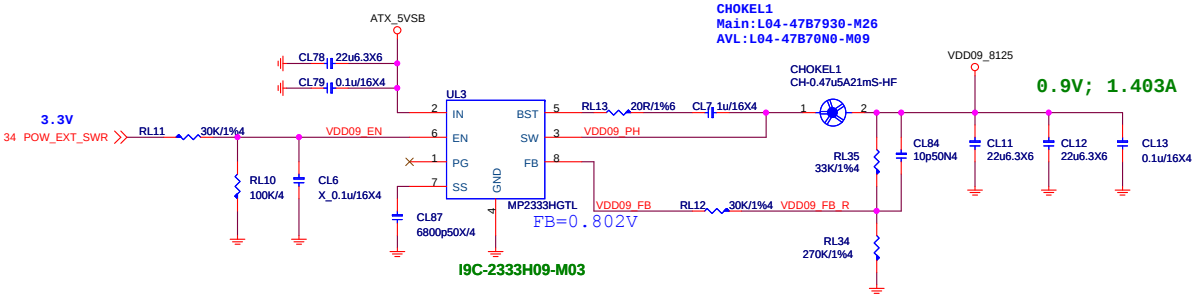


2V; 0.1569A

(3.3V-2V)*(0.1569A)=0.2039W



0.9V; 1.403A



MSI	MICRO-STAR INT'L CO.,LTD	
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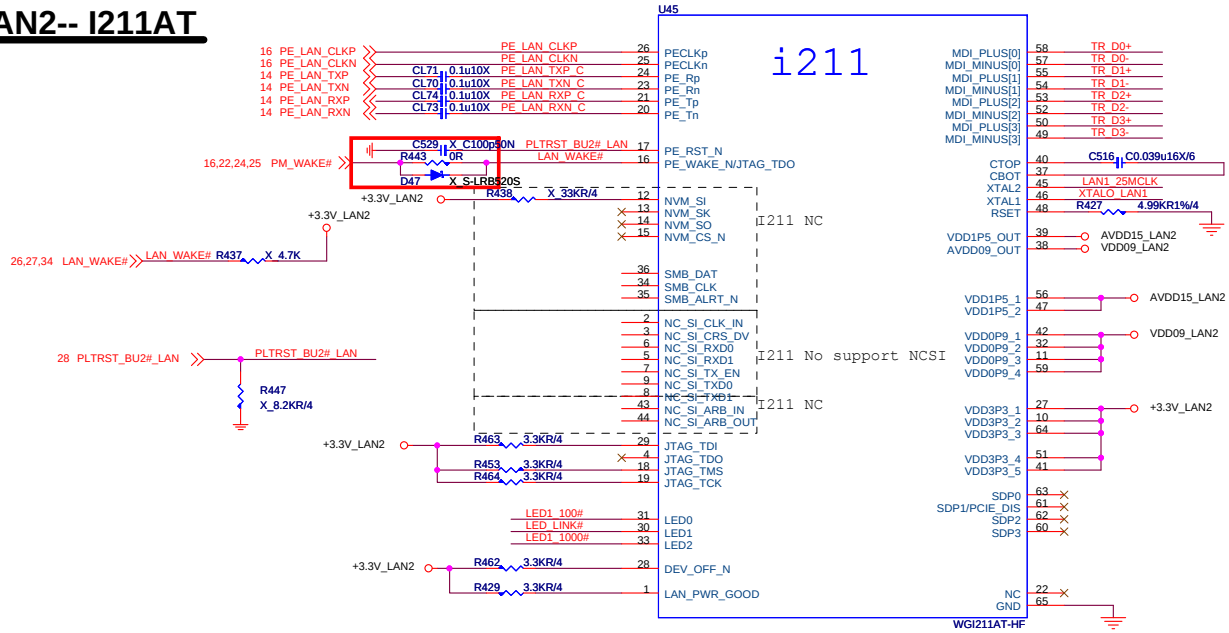
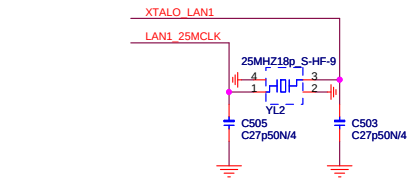
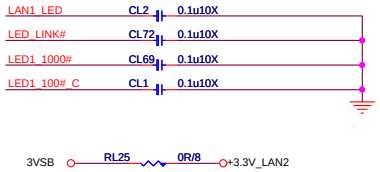
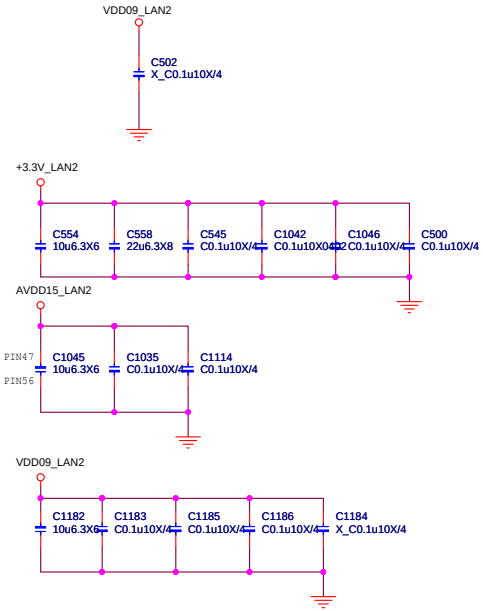
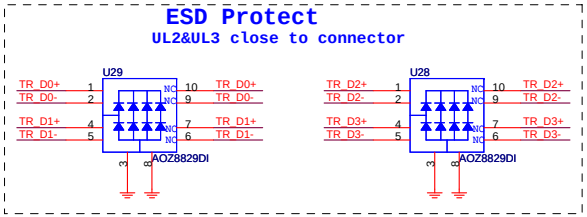
LAN2-- I211AT

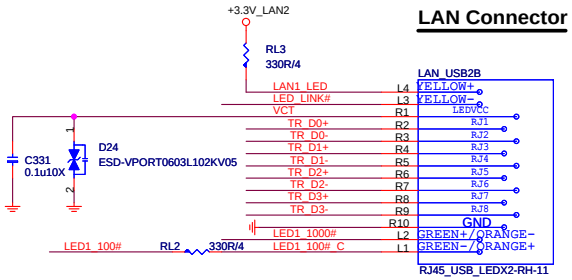












LED1 low is Orange 1000
LED2 low is Green 100

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ALC1220

follow PCH power

all of JD resistors should be placed
as close as possible to the sense pin of codec.

Closed Codec

CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

CPVDD:150mA

EMI

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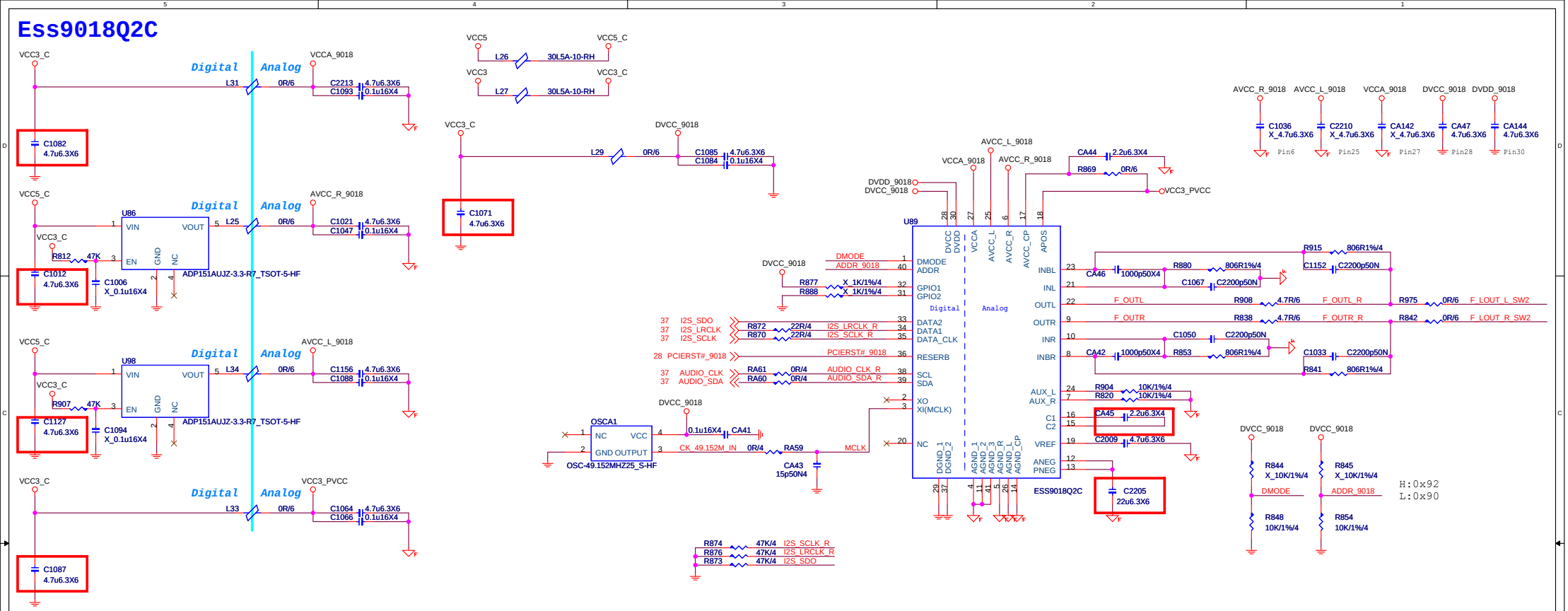
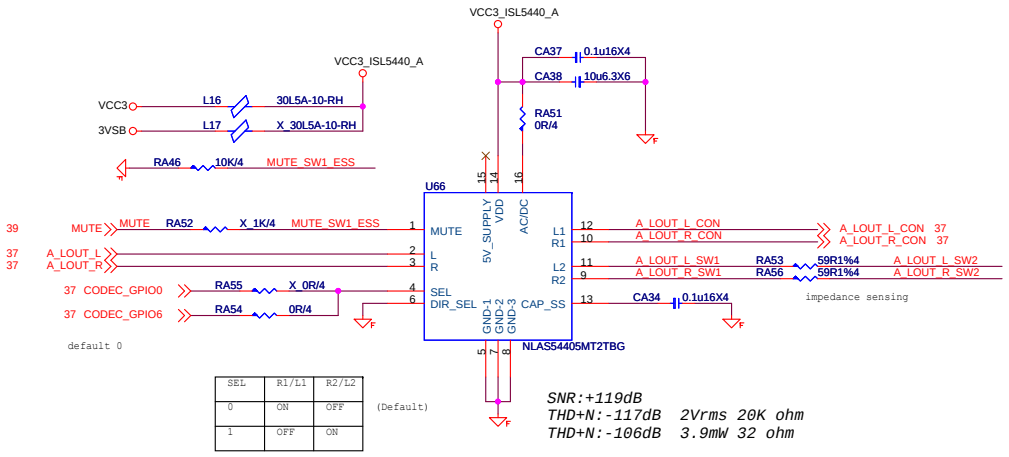
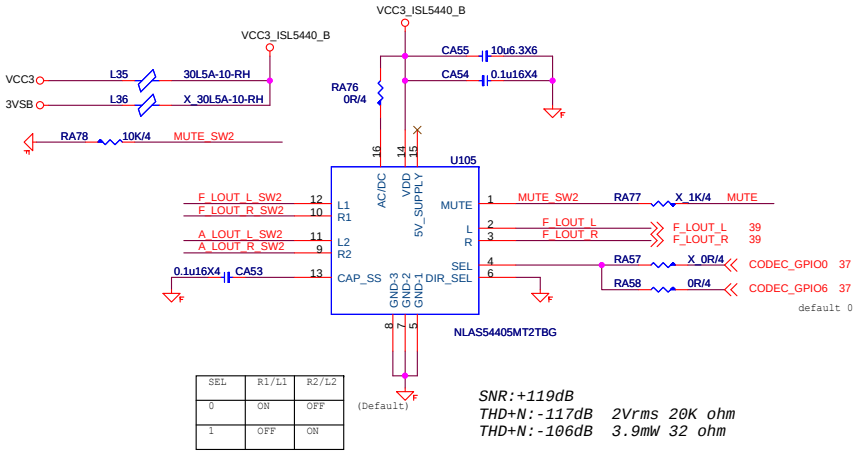
Ess9018Q2C



Analong SW1



Analong SW2



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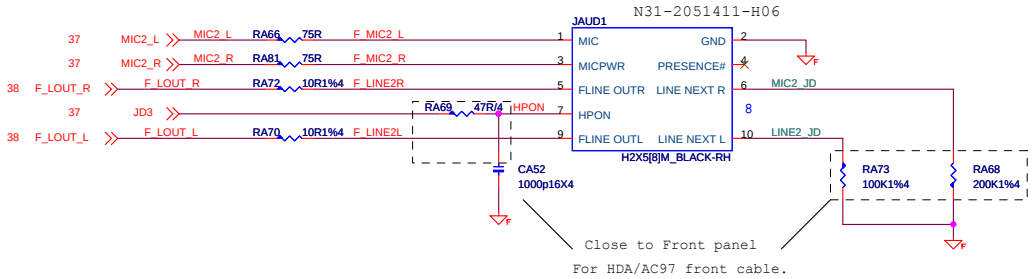
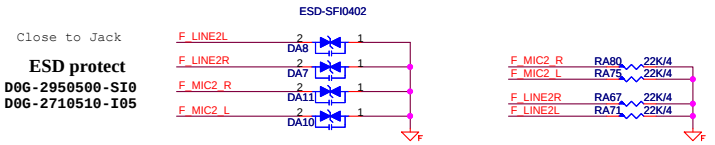
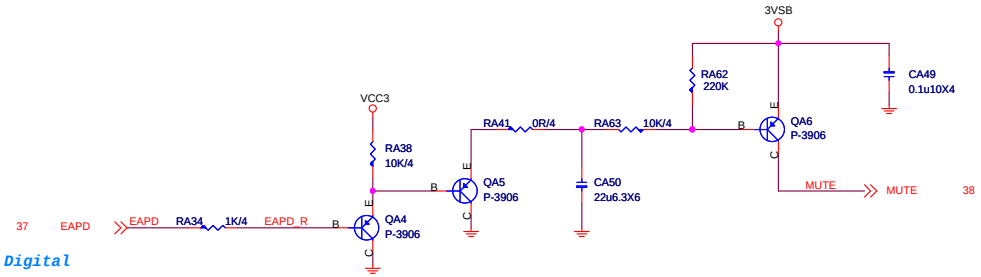




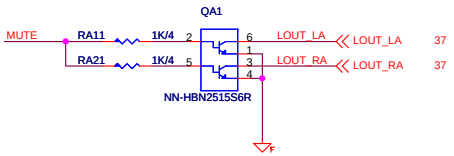
Rear Line OUT De-POP circuit

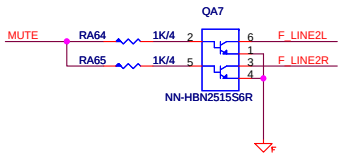
(De-pop circuit for Rear Line out & Front Headphone out)

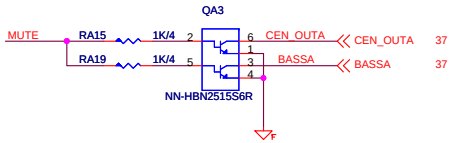


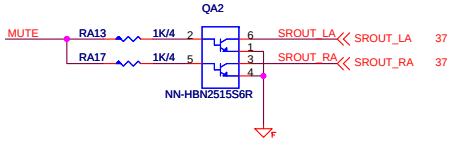
Digital

Analog









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Size: Custom	Document Description: Audio ALC1220-2	Rev: 11
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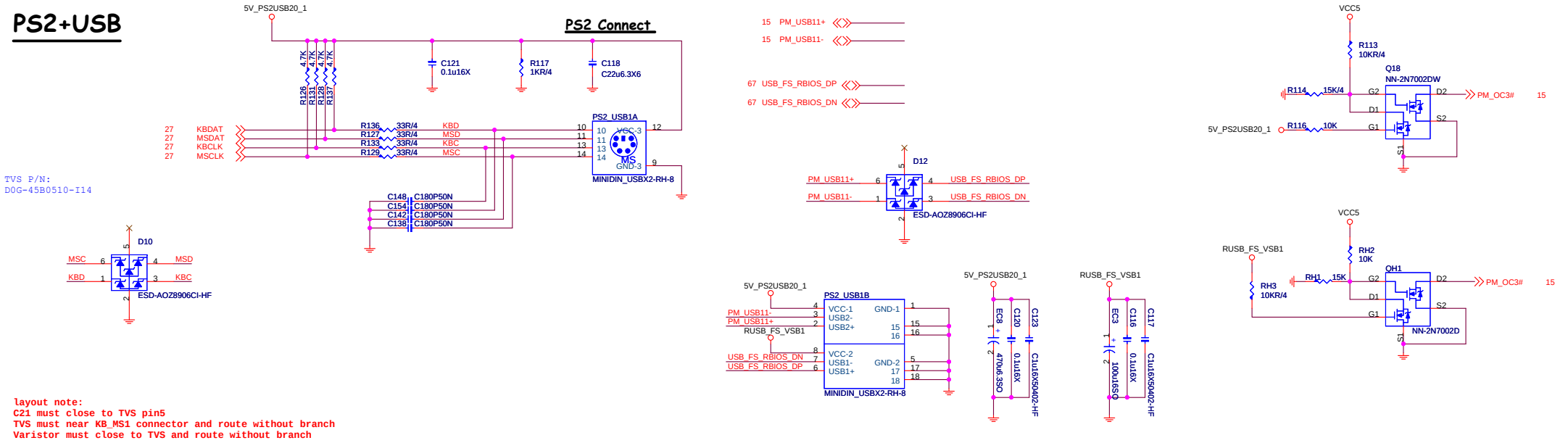
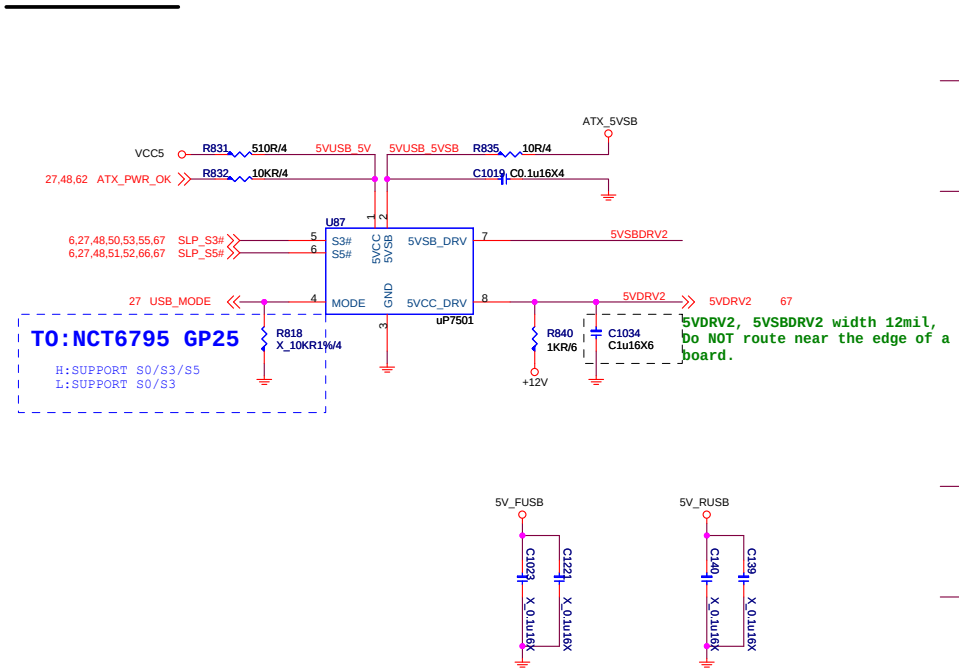
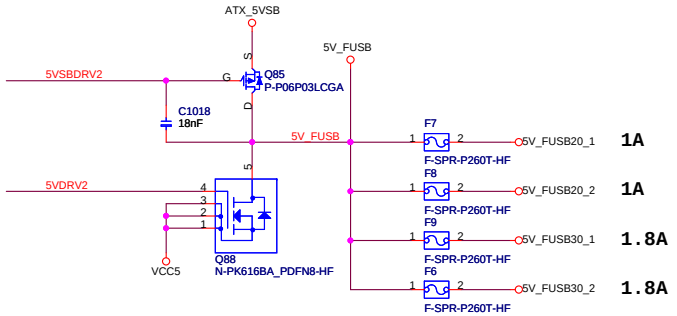
PS2+USB

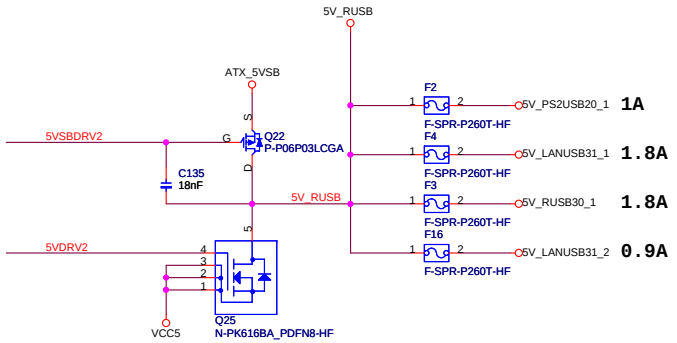


layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

USB Power







MICRO-STAR INT'L CO.,LTD

MS-7C35

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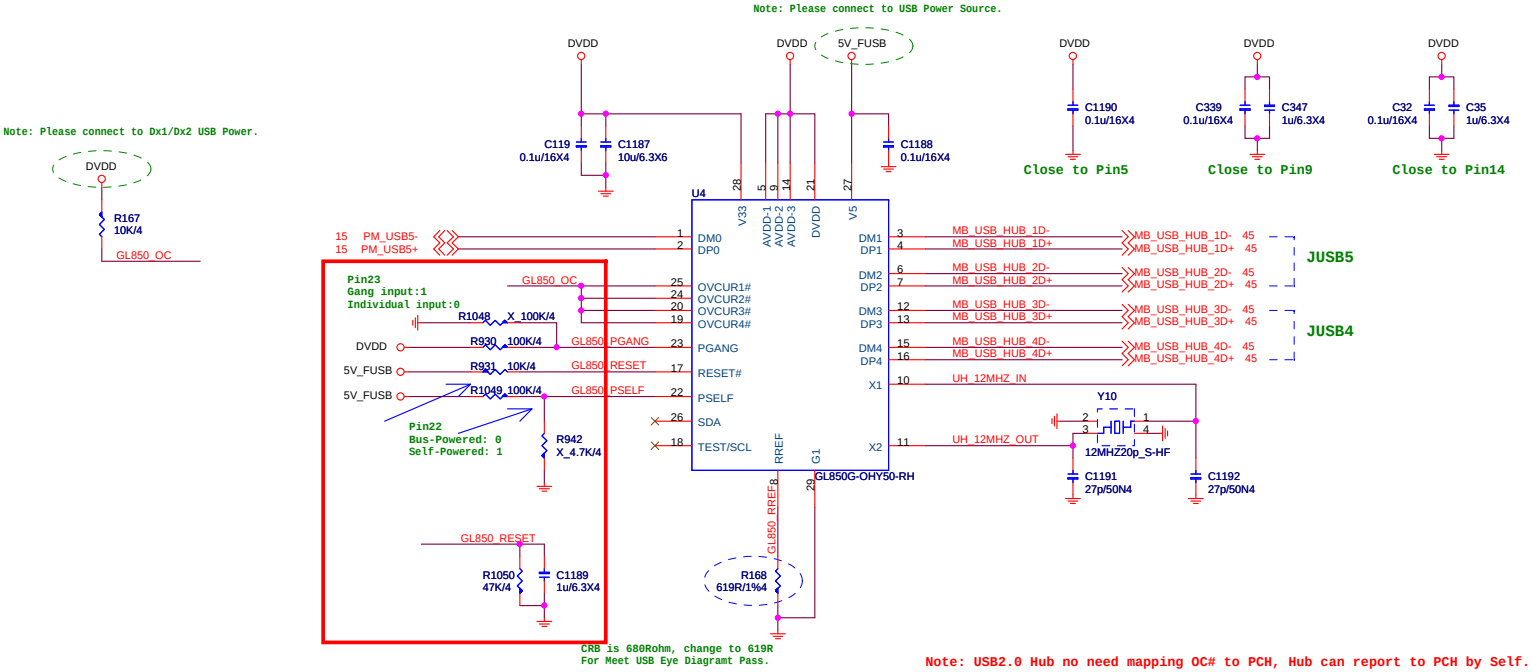
GL850G USB2.0 HUB

5V_FUSB



Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

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Size: Custom	Document Description: USB Rear PS2+USB2.0	Rev: 11
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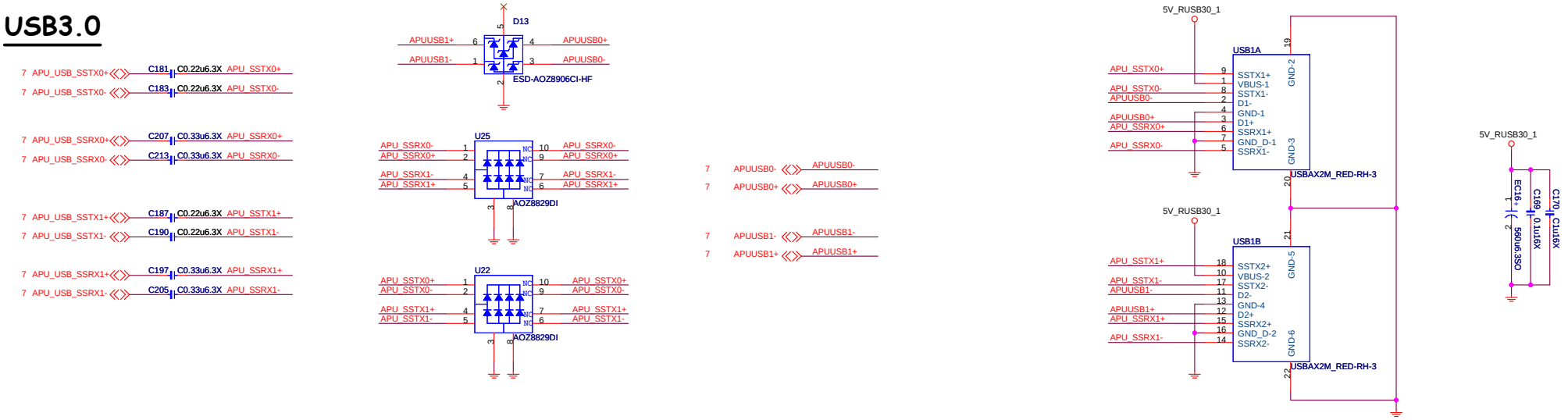
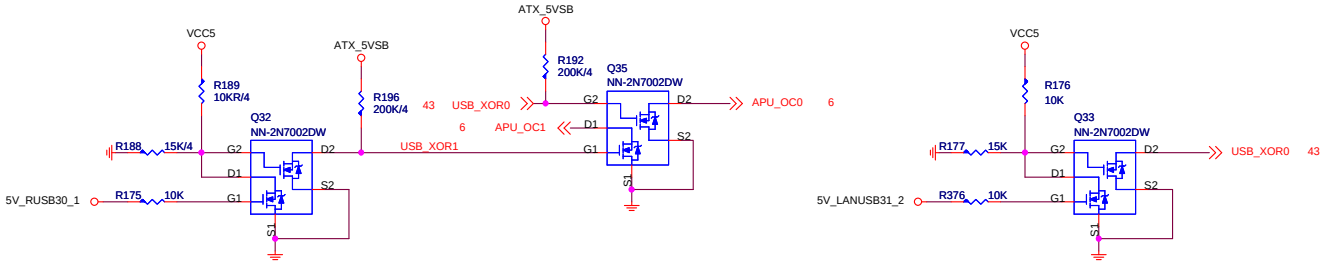
USB3.0



Type1/2/3/4 High Active



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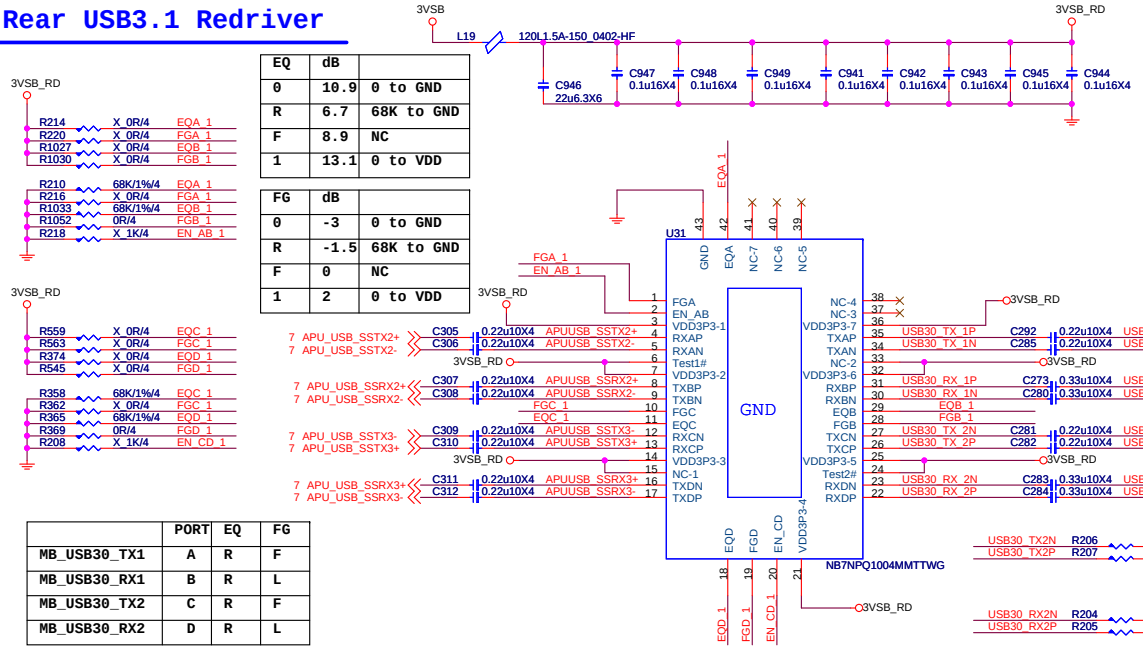
Rear USB3.1 Redriver

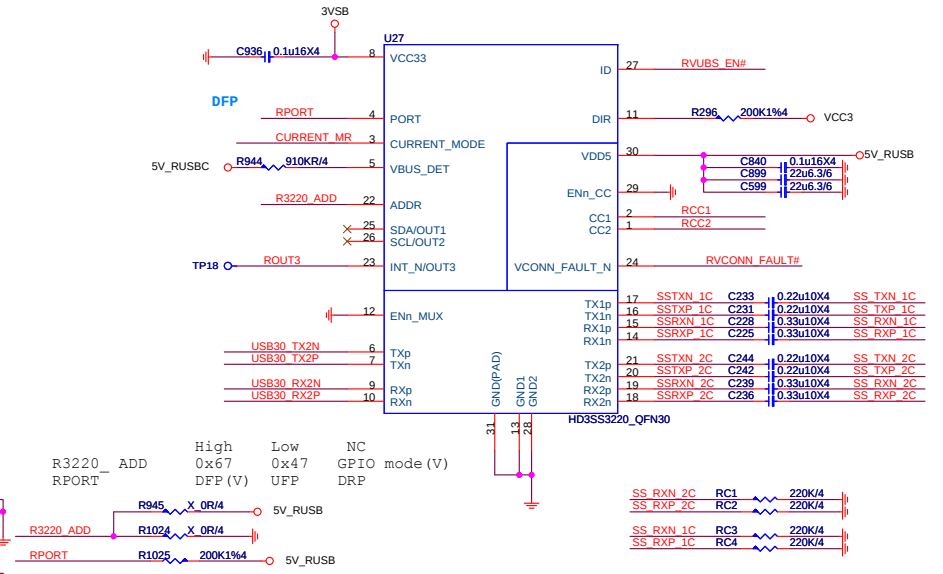
EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

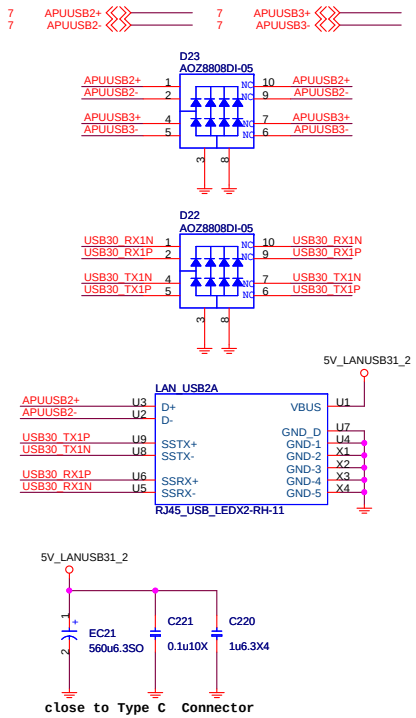
	PORT	EQ	FG
MB_USB30_TX1	A	R	F
MB_USB30_RX1	B	R	L
MB_USB30_TX2	C	R	F
MB_USB30_RX2	D	R	L



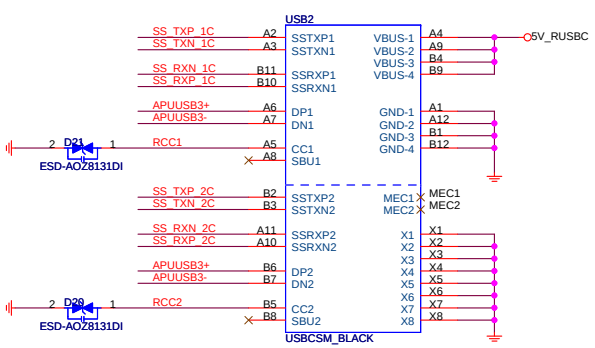
USB Type-C MUX with Configuration Channel (CC)



TYPE-A



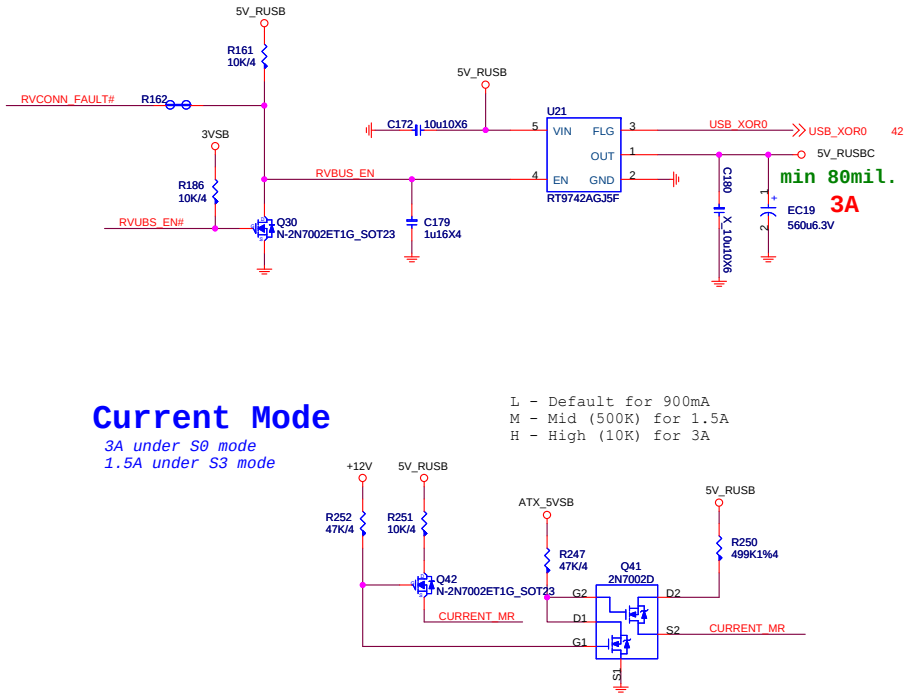
TYPE-C



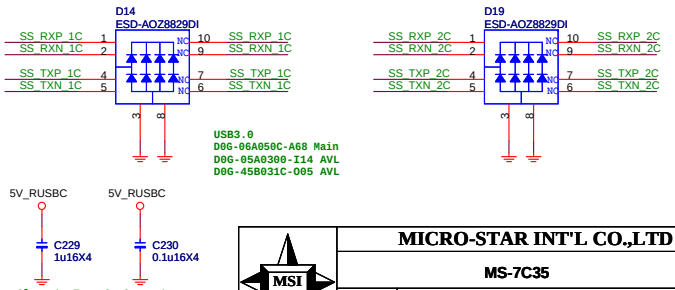
Current Mode

3A under S0 mode
1.5A under S3 mode

L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A



ESD Protection



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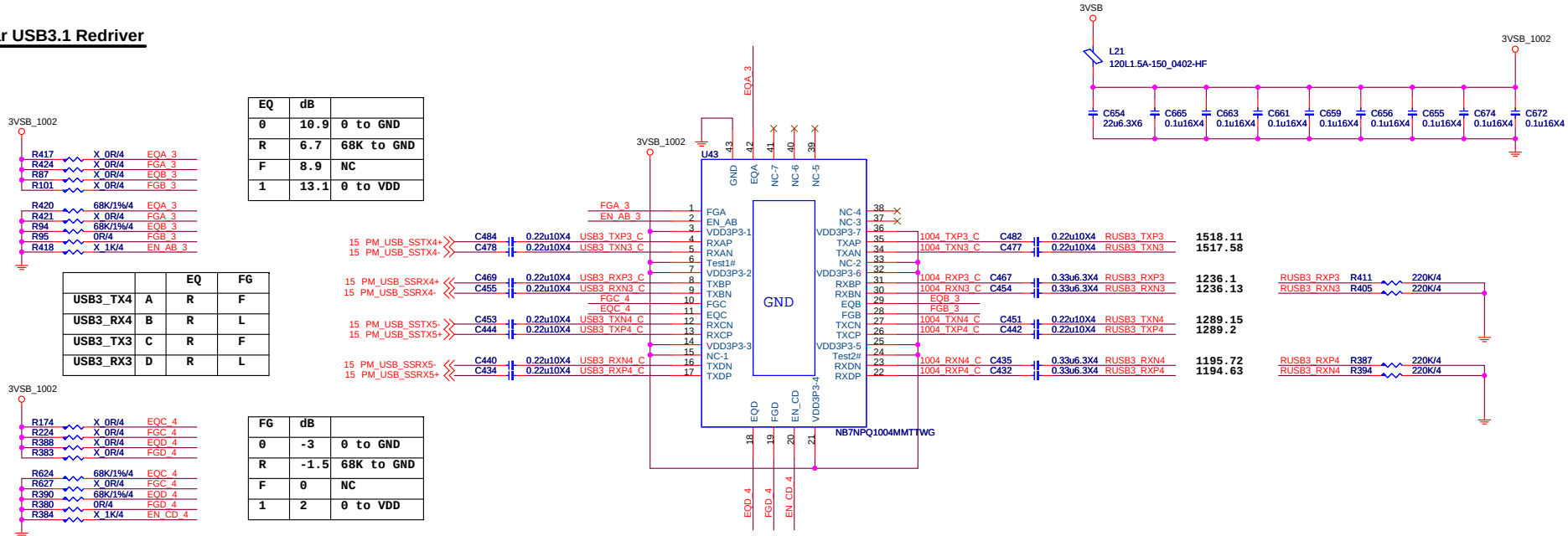
Rear USB3.1 Redriver

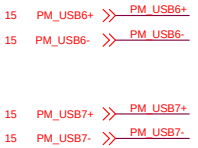
EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

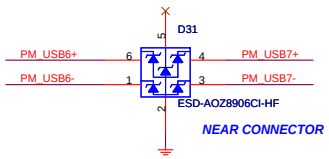
		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

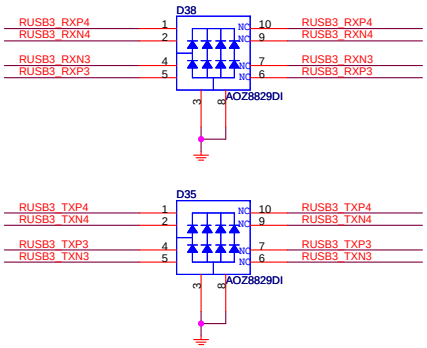
FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

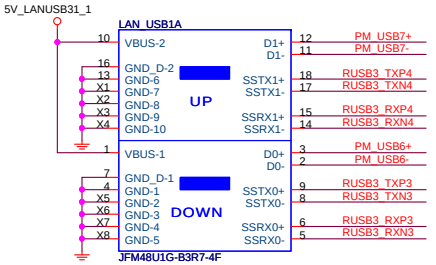


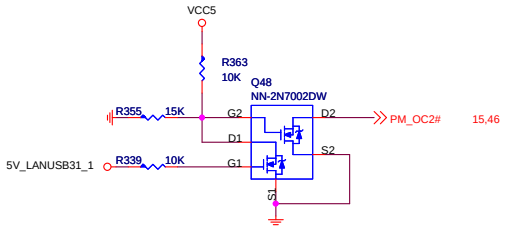
USB 3.1











MICRO-STAR INT'L CO.,LTD		
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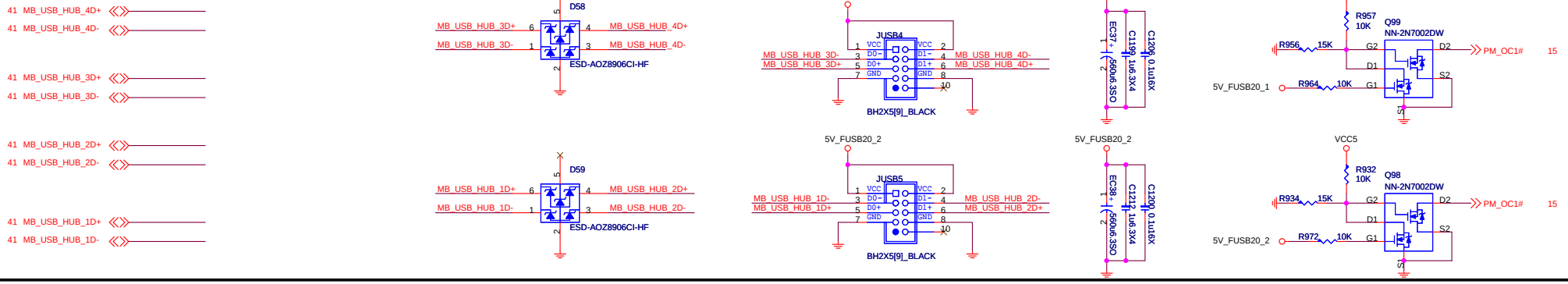
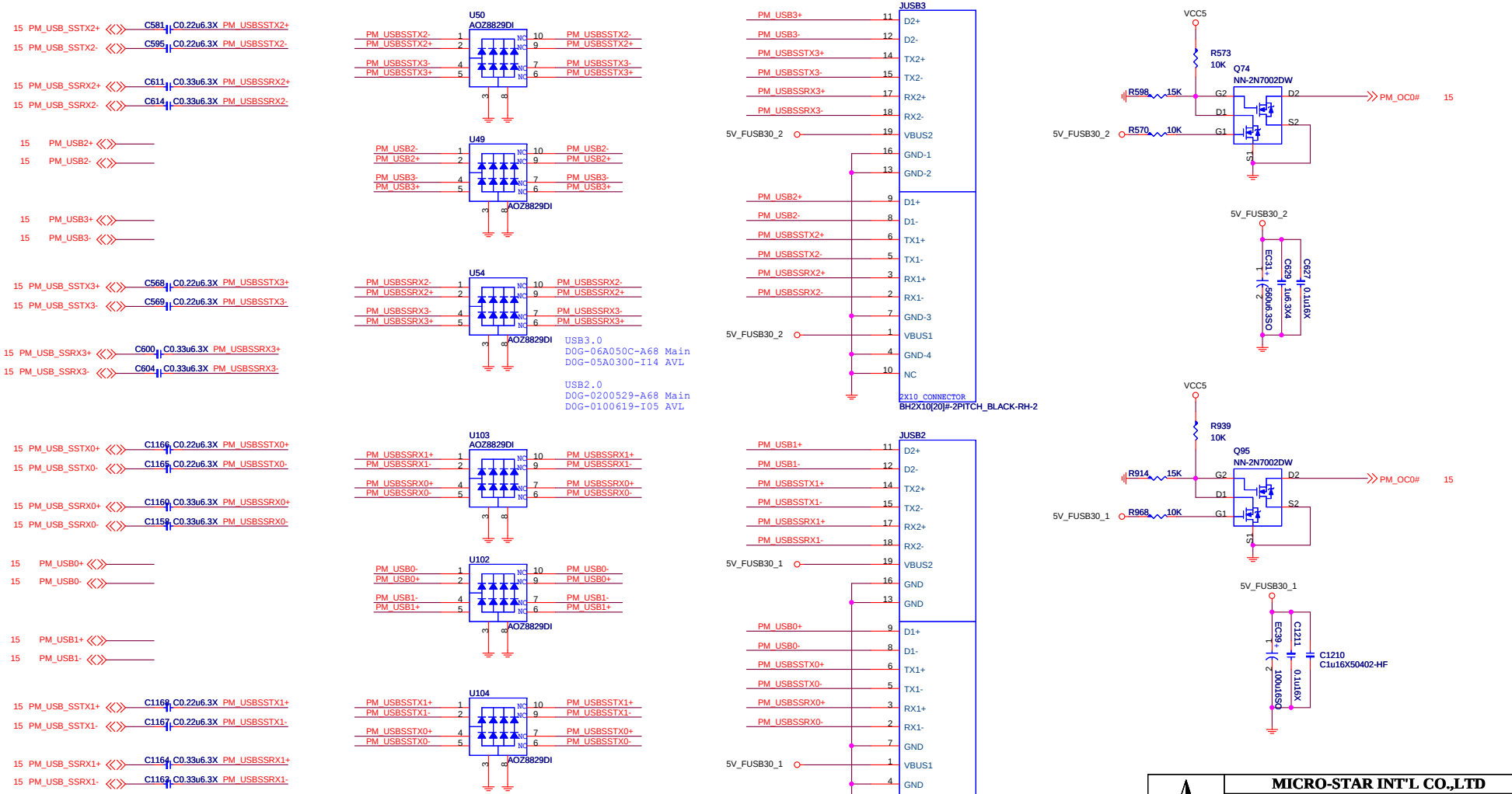
Front USB2.0



Front USB3.1 GEN1



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
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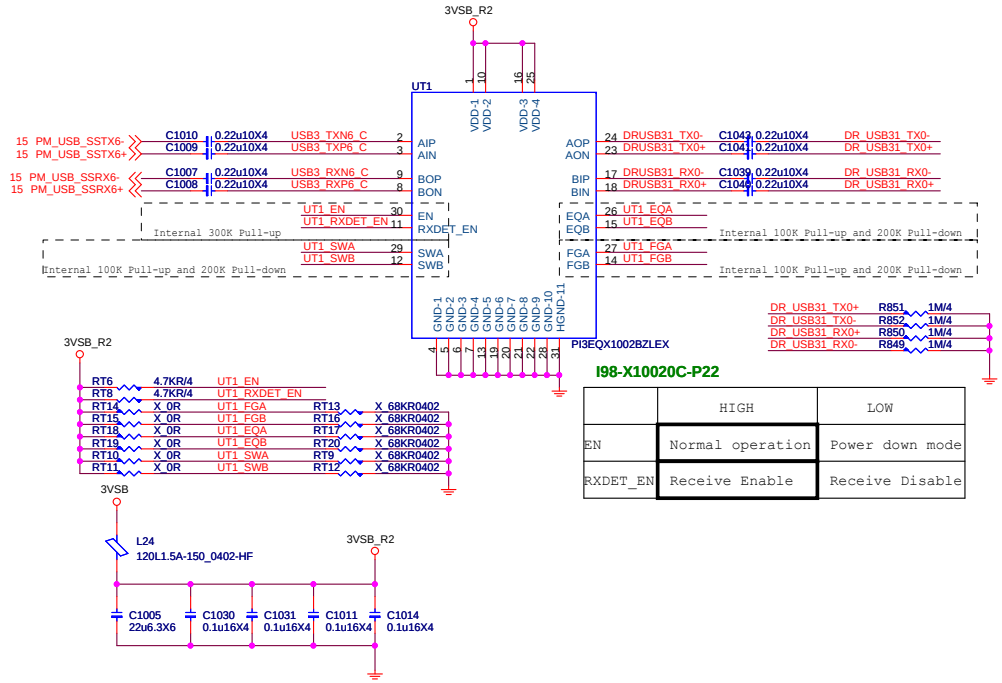
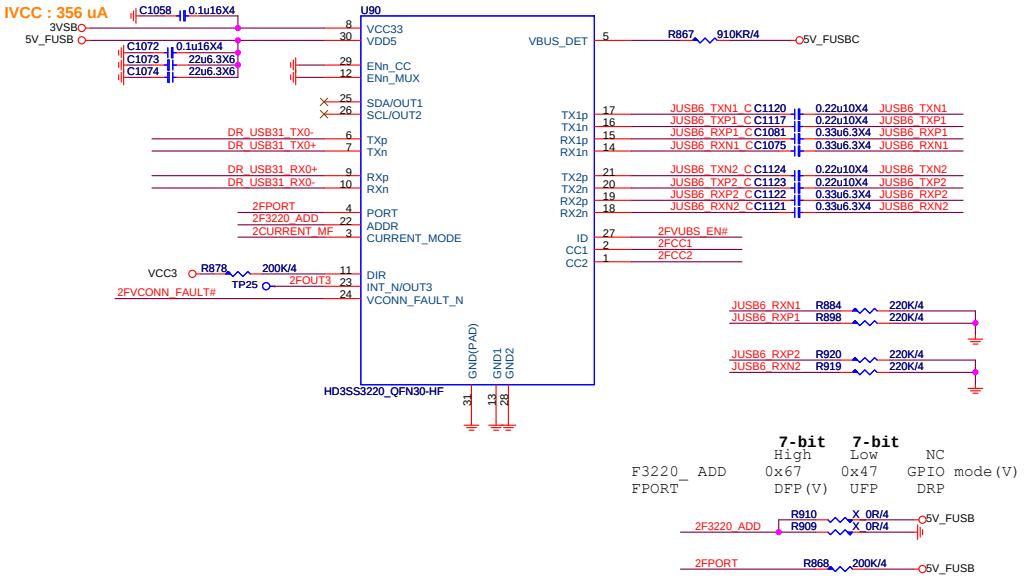
USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



I98-X10020C-P22

	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable

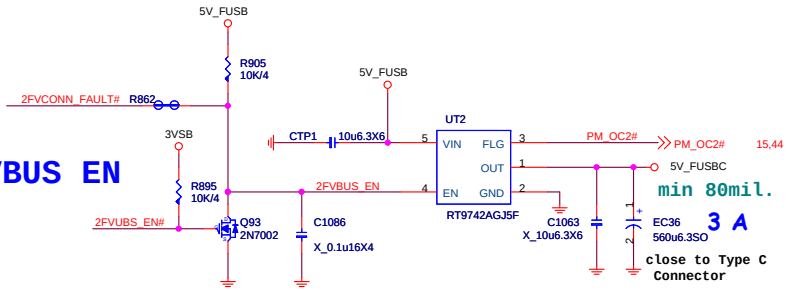


	7-bit High	7-bit Low	NC
F3220_ADD	0x67	0x47	GPIO mode(V)
FPORT	DFP(V)	UFP	DRP

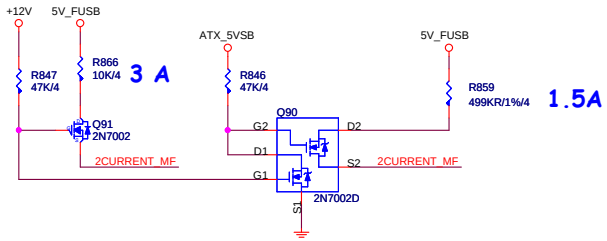
Remove VBUS OC# level shift circuit.

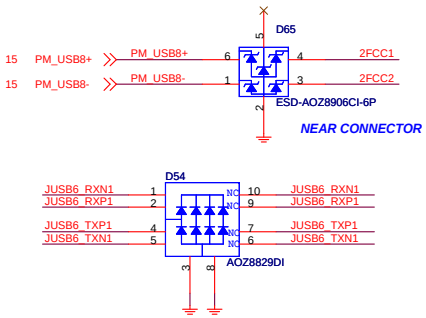
Remove VCOM OC# isolation circuit.

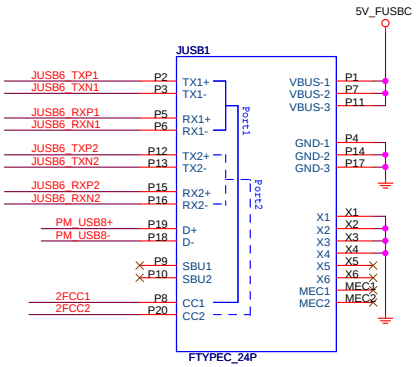
VBUS EN



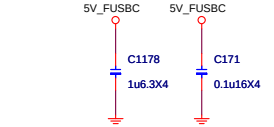
Current Mode







close to Type C Connector



ESD Protection
NEAR CONNECTOR

MICRO-STAR INT'L CO.,LTD

Size	Document Description	Rev
Custom	ASM1562 REAR USB3.1	11

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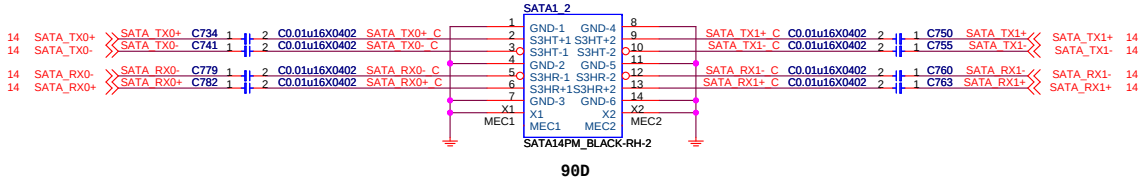
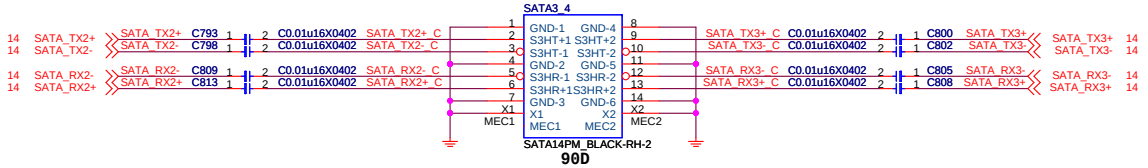
SATA Connector





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	MS-7C35	
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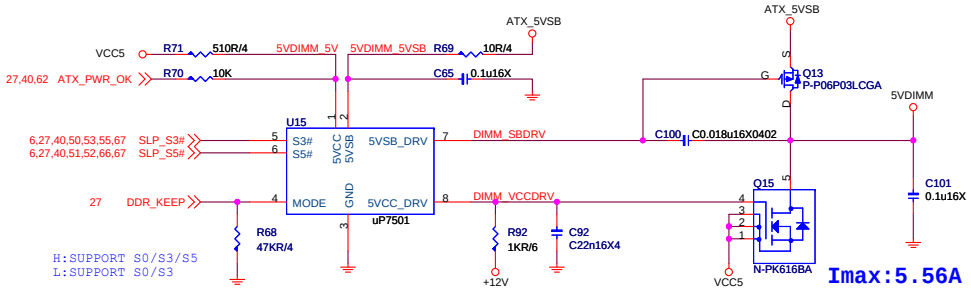
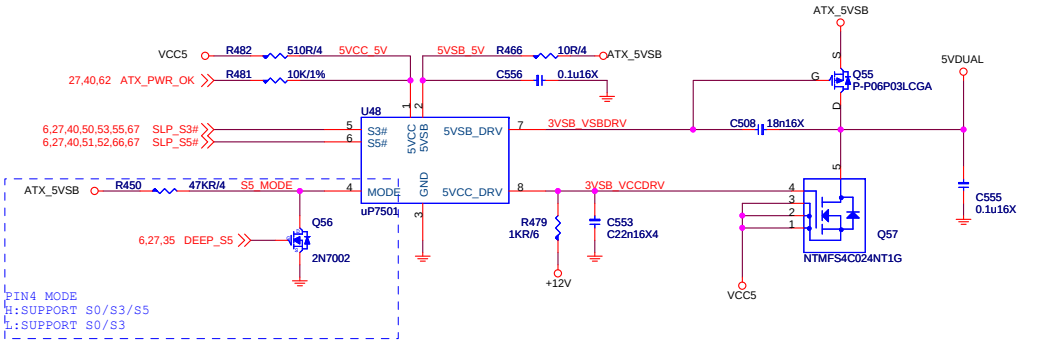
5VDIMM FOR DDR

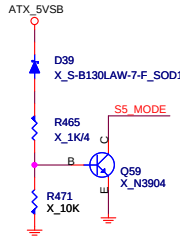


Imax:5.56A

5VDUAL For 3VSB CPU 1.8V VDDP

Imax:4.5A



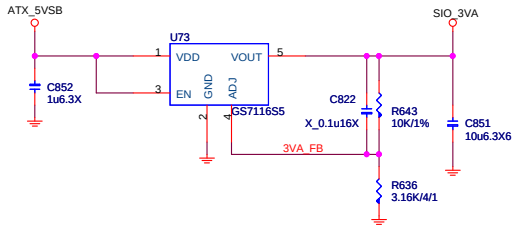


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

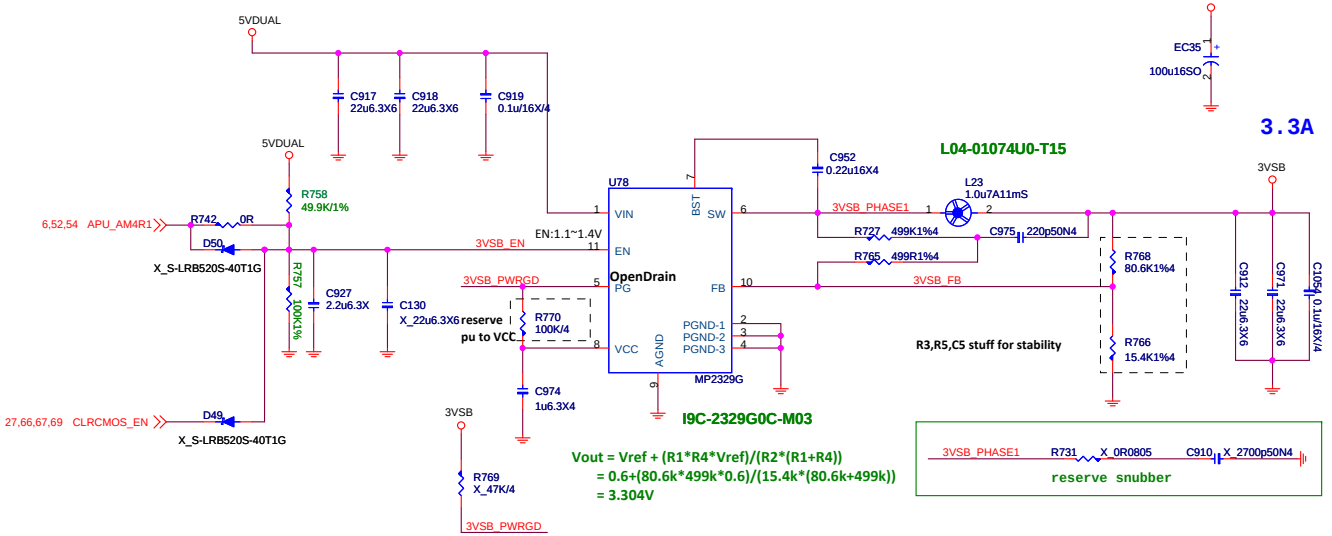
Remove for 3VSB Converter not need VCC3 ctrl

SIO_3VA

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V



3VSB



Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
= 0.6+(80.6k*499k*0.6)/(15.4k*(80.6k+499k))
= 3.304V

MSI	MICRO-STAR INT'L CO.,LTD	
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FOR CHIP_SOC

1.05V
S0:9A OCP 16A

Input Current = (12A*1V)/12V/0.8 = 1.25A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=12*SQRT((1/12)*(1-(1/12))) = 3.316A
Choke Irms =5 A

Irms = Iout * SQRT{D/N- (D)^2]}

L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
1/(700K*12*0.3)*(1-(1/12)) = 0.432uH
1/(700K*12*0.5)*(1-(1/12)) = 0.218uH

OCP=16A

Isat: 22A

L04-68B7350-T15

1V,9A

+12V
CHOKE21
+12V_CHIP_SOC
CH-0.47u5A21mS-HF
C601 10u16X/8
C612 10u16X/8
C588 10u16X/8
C624 C0.1u16X7/4
change to 10uF

U55
VIN
EN
3V3
PG
CLM
MODE1
MODE2
BST
SW
FB
PGND
GND-1
GND-2
GND-3
GND-4
NC-1
NB503-QFN-16

CHIP_SOC_EN
CHIP_SOC_BST
CHIP_SOC_SW
CHIP_SOC_FB
CHIP_SOC_3V3
CHIP_SOC_POK
CHIP_SOC_MODE1
CHIP_SOC_MODE2

internal LDO 3.3V
C653 1u6.3X4
VFB=0.6V
R538 100KR/4
C679 C0.1u16X7/4
R547 X_0R/4
R525 0R/4
R510 0R/4
Current limit:16A, CLM float
Mode:Vo<3V, DCM 700K

C698 0.22u16X4
CHOKE24
CH-0.68u15A5mS-HF-1
R593 1MR1%/4
C721 220p50N4
R537 499R1%/4
R4 R6 C4 stuff for stability

CHIP_SOC
C751 C22u6.3X/6
C754 C22u6.3X/6
C759 C22u6.3X/6
C758 C22u6.3X/6
C762 C22u6.3X/6
C761 C22u6.3X/6
C772 C22u6.3X/6
C770 C0.1u16X7/4

ATX_5VSB
VCC3
R509 47K/4
R514 10K/4
C613 X_C1u6.3X/4
Q72 NN-2N7002DW
CHIP_SOC_C
CHIP_SOC_EN
50 CHIP_CLDO_PG
53 CPU_1P8_PG
Q63 2N7002

+12V_CHIP_SOC
R492 X_100KR1%/4
CHIP_SOC_EN
EN: 1.12-1.32V
R501 X_39.2KR1%/4
C602 X_C0.1u16X7/4

CHIP_SOC_SW R554 X_1R1%/6 C651 X_C3300p50X/4
reserve snubber

CHIP_SOC
R604 6.8R1%4
CHIP_SOC_SENSE_R
CP11 X_COPPER
CHIP_SOC_SENSE 17
R542 1KR1%/4
CHIP_SOC_FB
CP10 X_COPPER
CHIP_SOC_OV 68
R536 1.47KR1%/4

Vout = Vref * (1 +(R9/R10))
= 0.6 * (1 +(13.3K/20K))
= 0.999V

FOR CHIP_SOC_S5

1V@1A

3VSB
R533 10K1%/4
SOC_VSB_EN
R532 16K1%/4
C646 1u6.3X
5VDUAL
R568 100K
SOC_VSB_PG
C689 C1000p10X4

VCC3
R488 10K
CHIP_SOC_POK
CHIP_CLDO_PG
6,7,55,62,69 SYSREST#
D43 S-LRB520S
D41 S-LRB520S
D42 X_S-LRB520S
Add by CRB Rev. E
C105 X_0.01u16X4
CPU_1P8
Q103 N-PM514BA
6,56 APU_PWROK
APU_PWROK_R
R486 10K/4
C930 0.1u16X
U113 NC7SZ08M5X_SOT23-5
PM_VR_PWRGD
PM_VR_PWRGD 55
C577 X_1u6.3X

3VSB
R474 10K/4
Q64 NN-2N7002DW
PM_PWROK 16
R487 1K/4
C576 1u6.3X
PM_PWRGD
PM_PWRGD 16

5VDUAL
U58
IN
EN
PG
SS
GND
BST
SW
FB
MP2333HGTL_SOT583-8-HF
C1213 C0.1u10X4
C1208 C22u6.3X/6
55 SOC_VSB_PG
C649 C6800p10X04
I9C-2333H09-M03
SOC_VSB_EN
SOC_VSB_BST
SOC_VSB_BST_R
20R/1%6 R548
C699 1u16X
SOC_VSB_PHASE
SOC_VSB_FB_R
R534 30K1%/4
FB:0.789~0.821V

L01-0107118-M26
L13 1.0u5.5A-35_1210
CHIP_SOC_S5
1A
R1 R552 33K/1%
C676 C10p25X4
C720 C22u6.3X/6
C739 22u6.3X/6
R2 R535 130K1%/4

Vout = Vref * (1 +(R1/R2))
= 0.789~0.821V * (1 +(33K/130K))
= 0.989V~1.029V

MICRO-STAR INT'L CO.,LTD
MS-7C35
Size: Custom
Document Description: PM-NB681GD-1.05V/GS7133-2.5V
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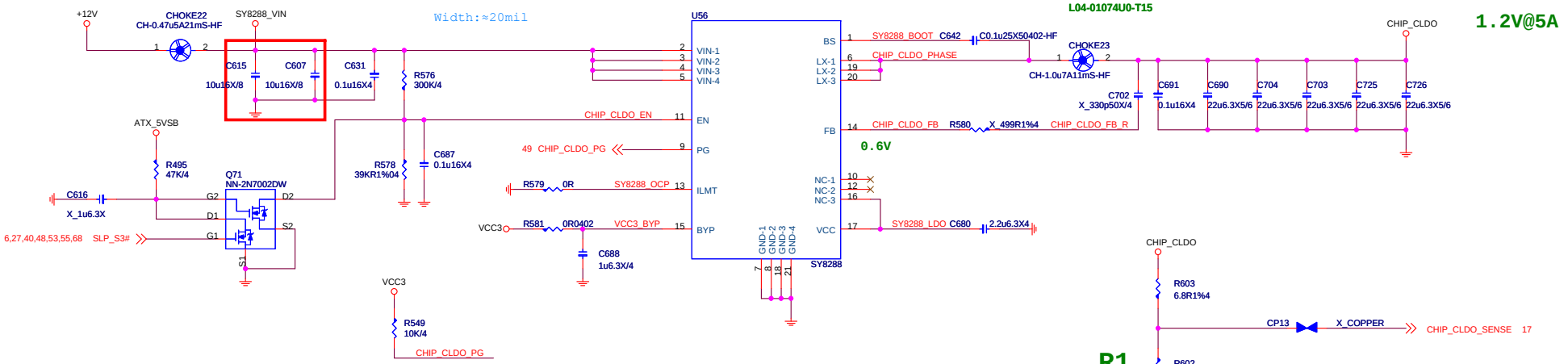
Promontory-2.5V

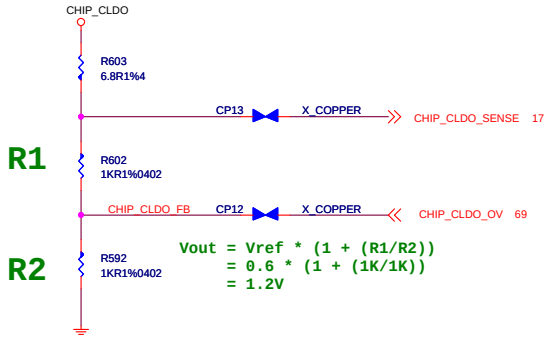
2.5V; 5A OCP 8A

Input Current= (5.5A*1.05V)/12V/0.8=0.625A

Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=5*SQRT((1.2/12*(1-(1.2/12))) = 1.5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A



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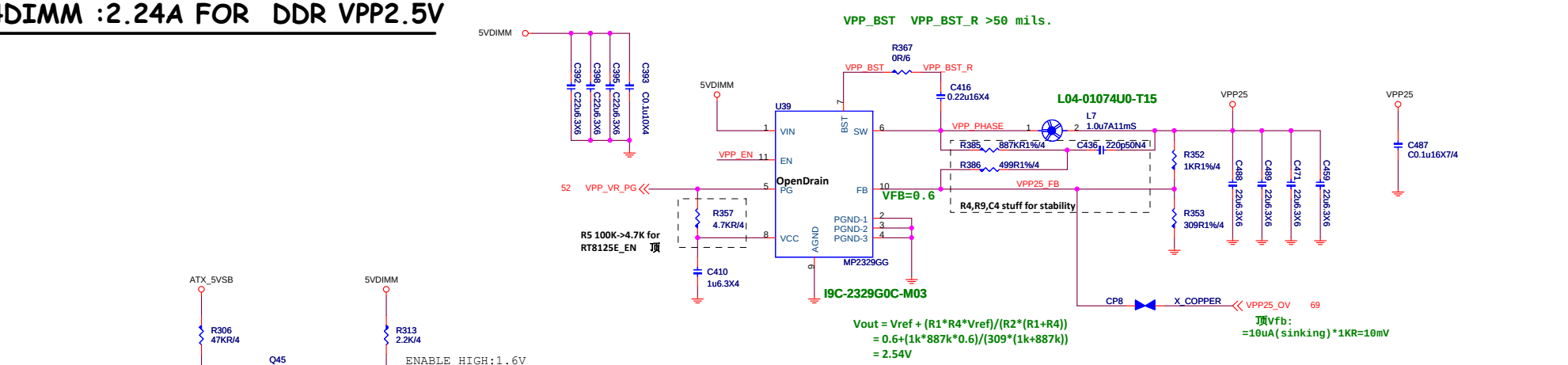
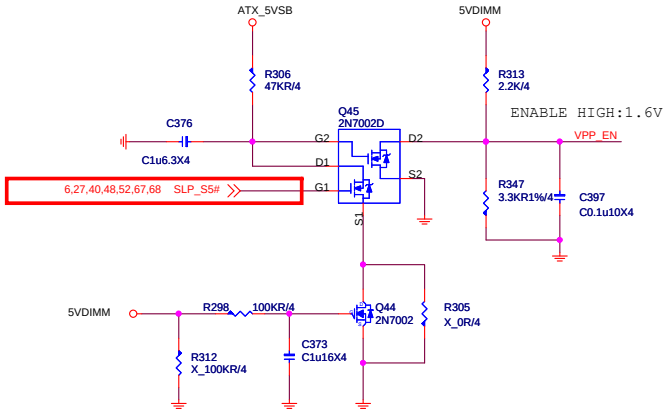
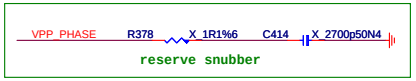
MS-7C35		
Size: Custom	Document Description: CPU Power NB S5	Rev: 11
Date: Monday, March 25, 2019	Sheet 50 of 75	

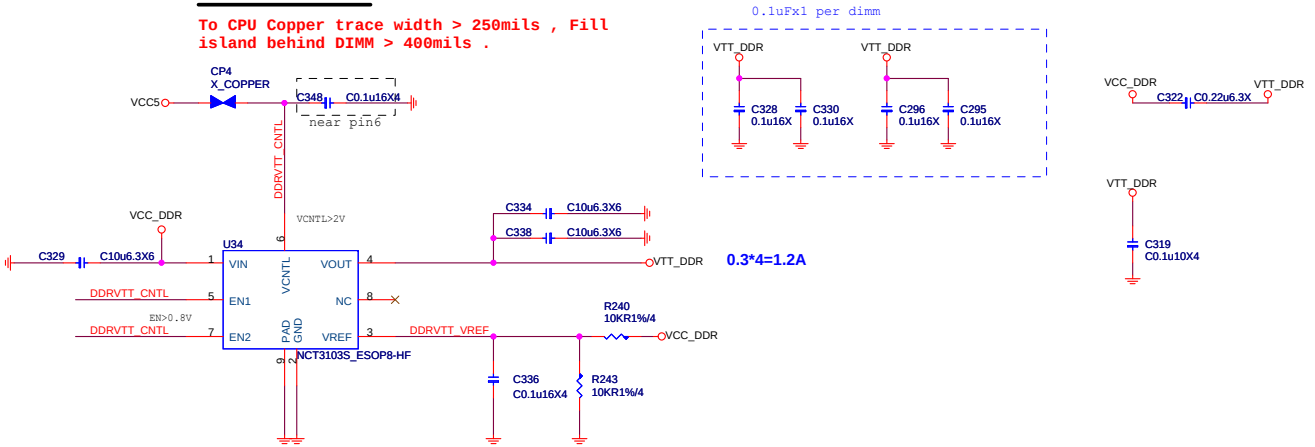
4DIMM :2.24A FOR DDR VPP2.5V







DDR VTT Power



MICRO-STAR INT'L CO.,LTD		
MS-7C35		
Size: Custom	Document Description: DDR PWR VPP25/VTT-MP2147	Rev: 11
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DDR4_1.2V 15.5A+9.5A+1.2A=26.2A

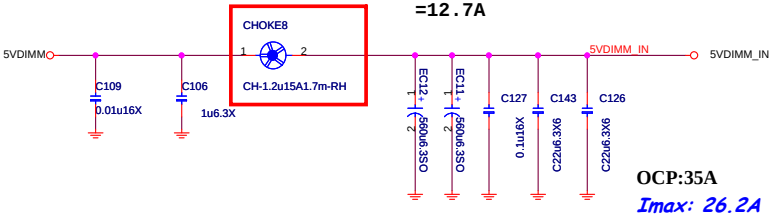
15.5A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

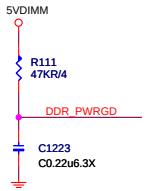
VID	Reference Voltage (V)
H	0.675
L	0.75

Irms = Iout * SQRT{D/N- (D)^2]}
D=Vout/Vin=1.9/5=0.38
N=Phase number=1
=26.2A*SQRT(0.38-0.1444)
=12.7A



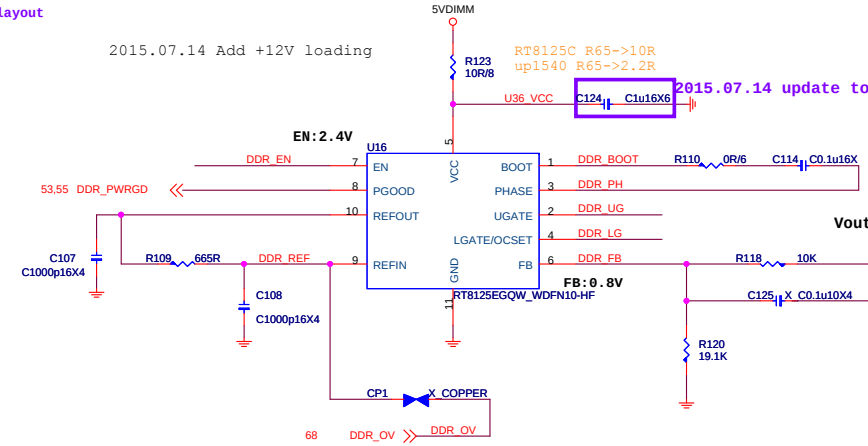
OCP:35A

Imax: 26.2A

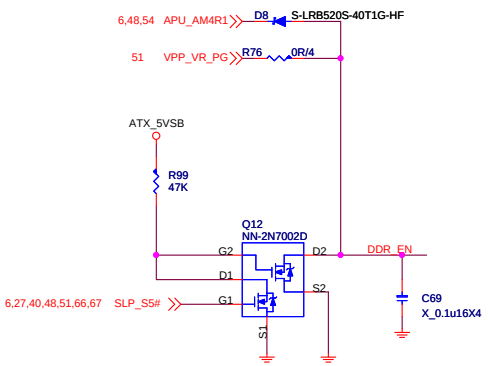


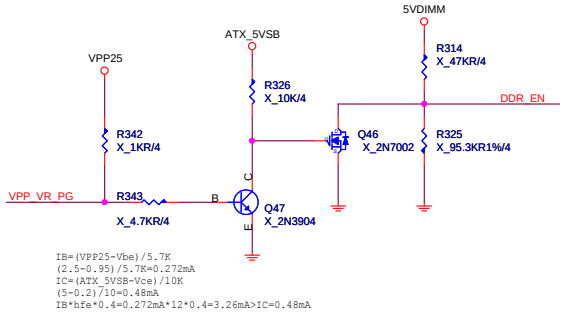
Pull up change by layout

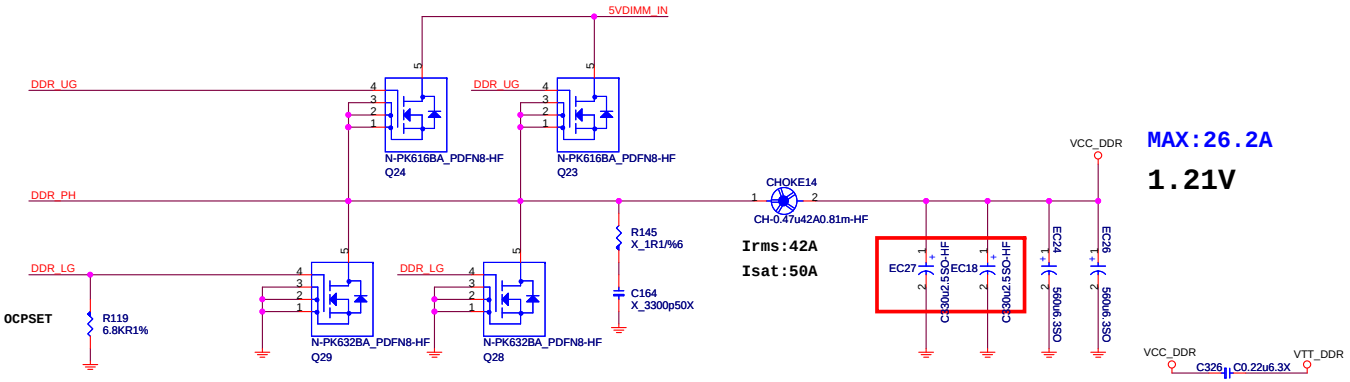
2015.07.14 Add +12V loading



Vout=0.8V*(1+R204/R208)=0.8V*(1+10k/19.6k)=1.208V







MAX:26.2A

1.21V

OCP target=35A

OCPSET:min 5Kohm

R232=6.8K

OCP =(R232*10uA)/Rdson =R232*10uA)/4m/2 =34A

OCP =(R232*10uA)/Rdson =R232*10uA)/3.3m/2 =41A

D03-4C02403-005 : 4 mohm

D03-4C02403-005 : 3.3mohm

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MS-7C35

Size: Custom | Document Description: DDR Power-RT8125E | Rev: 11

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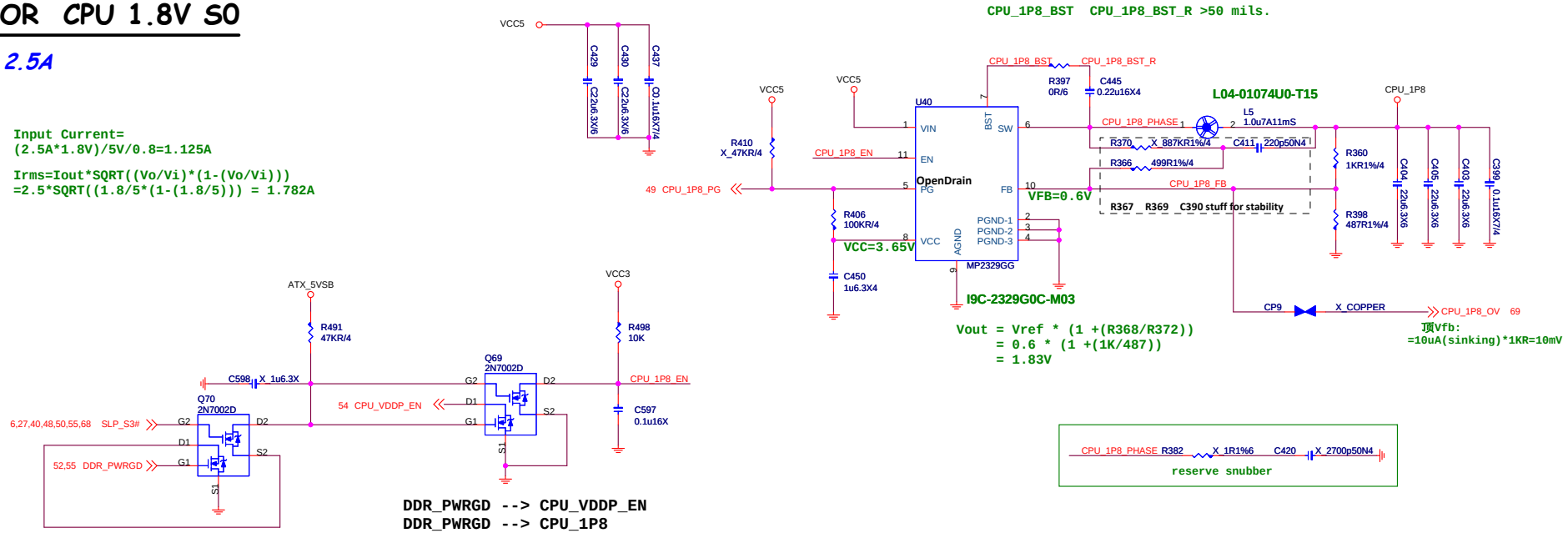
FOR CPU 1.8V S0

2.5A

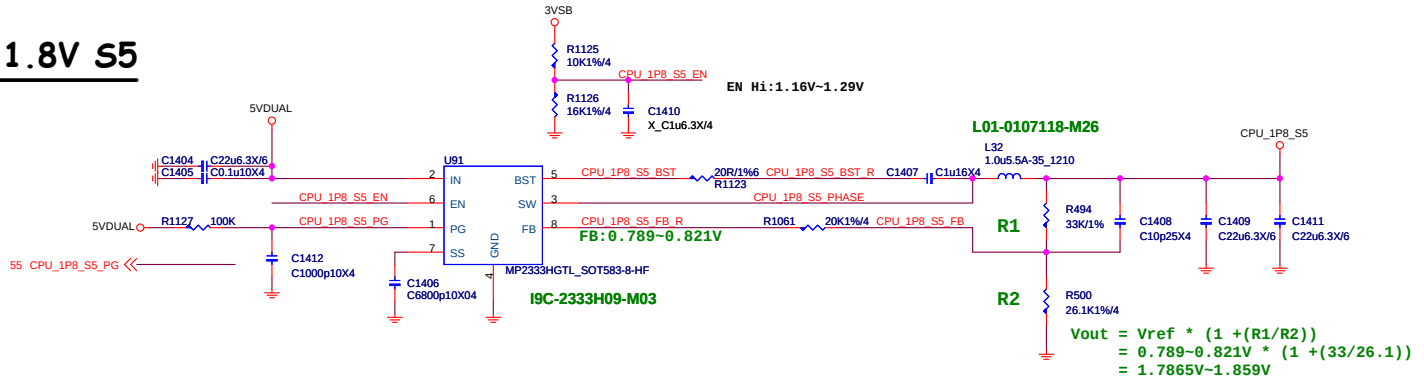
Input Current=
(2.5A*1.8V)/5V/0.8=1.125A

Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=2.5*SQRT((1.8/5*(1-(1.8/5))) = 1.782A



FOR CPU 1.8V S5

0.5A



MICRO-STAR INT'L CO.,LTD	
MS-7C35	
Size: Custom	Document Description: CPU Power 1P8/1P8_S5 — Rev: 11
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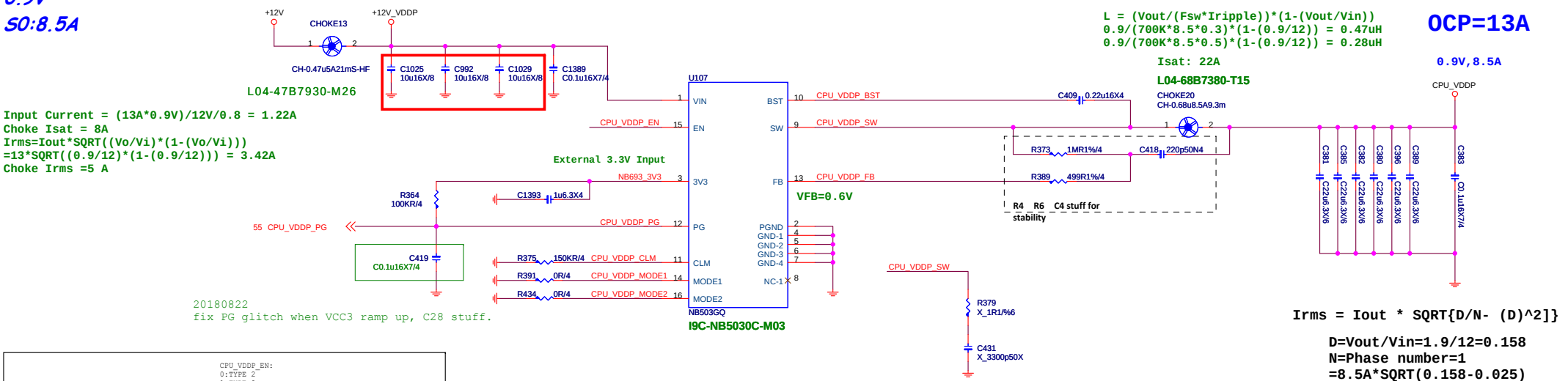
CPU_VDDP_S0

0.9V
S0:8.5A




```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```

```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
```

OCP=13A

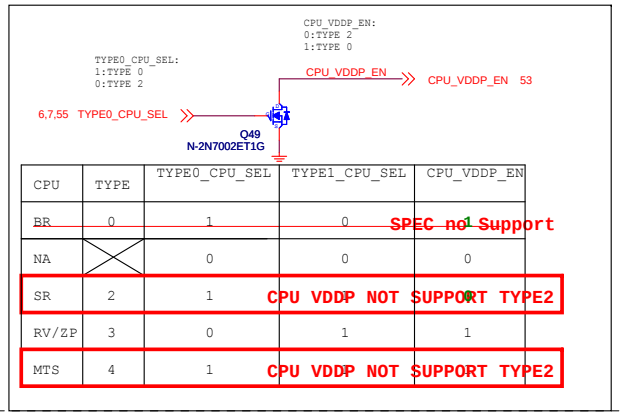
0.9V,8.5A

Isat: 22A

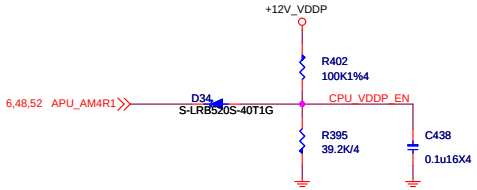
L04-68B7380-T15

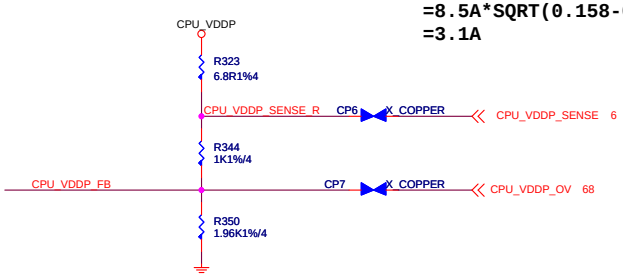
```
Irms = Iout * SQRT{D/N- (D)^2]}

D=Vout/Vin=1.9/12=0.158
N=Phase number=1
=8.5A*SQRT(0.158-0.025)
=3.1A
```

20180822
fix PG glitch when VCC3 ramp up, C28 stuff.



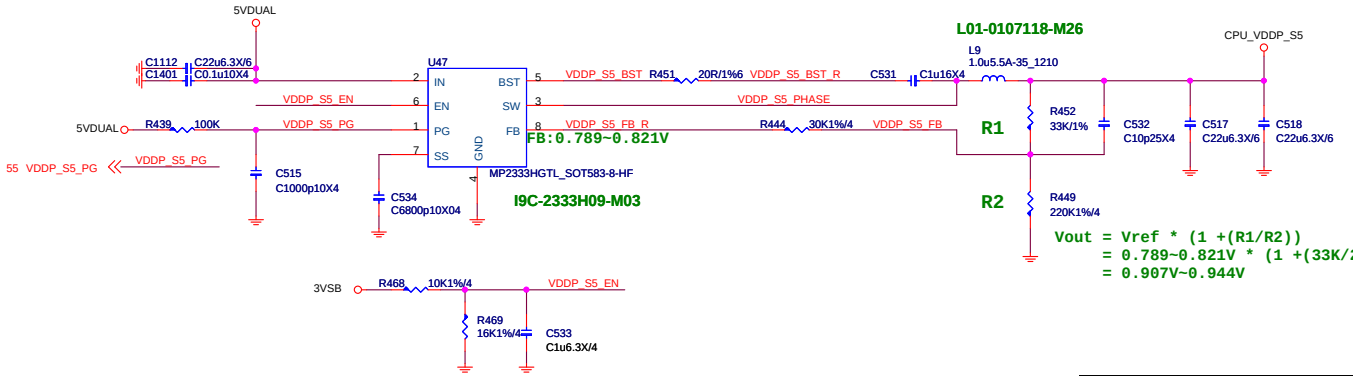
CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	SPEC no Support
NA	X	0	0	0
SR	2	1	1	CPU VDDP NOT SUPPORT TYPE2
RV/ZP	3	0	1	1
MTS	4	1	1	CPU VDDP NOT SUPPORT TYPE2





CPU_VDDP_S5

0.9V
S0:1A




```
Vout = Vref * (1 +(R1/R2))
     = 0.789~0.821V * (1 +(33K/220K))
     = 0.907V~0.944V
```

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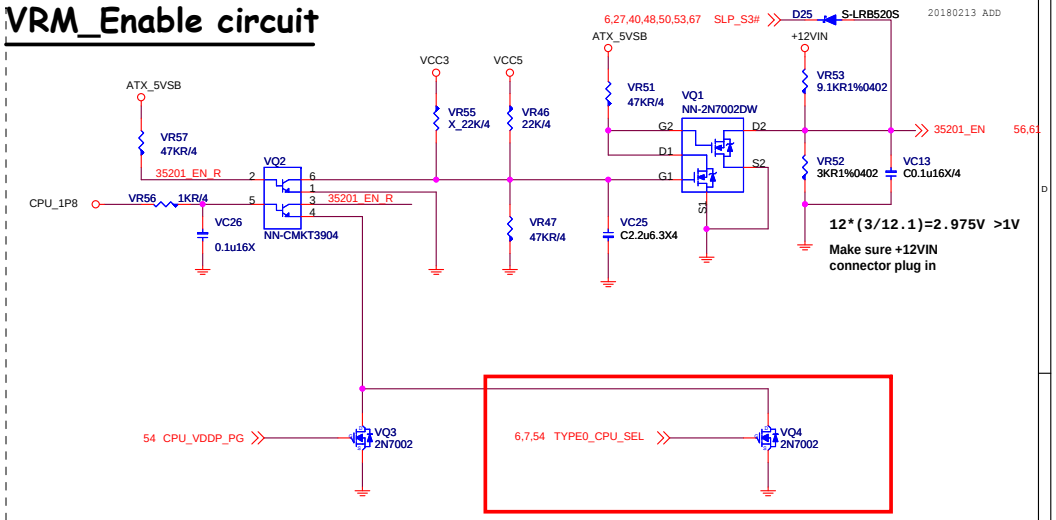
VRM_Enable circuit



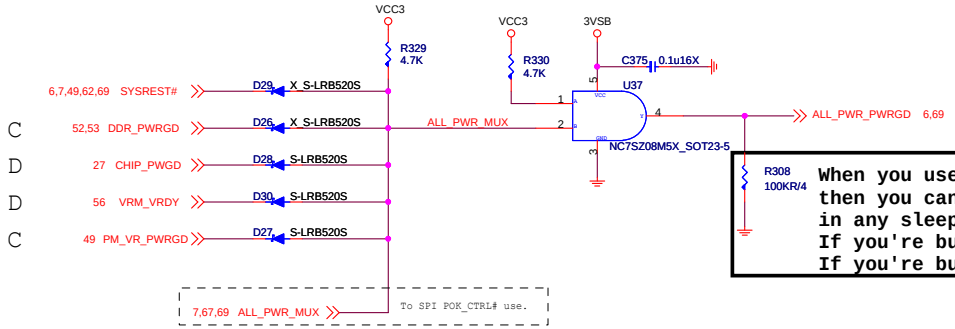
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
~~BR~~	~~0~~	~~0~~	~~1~~
NA		0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1

SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

CPU VDDP NOT SUPPORT TYPE4

ALL POWER GOOD MUX

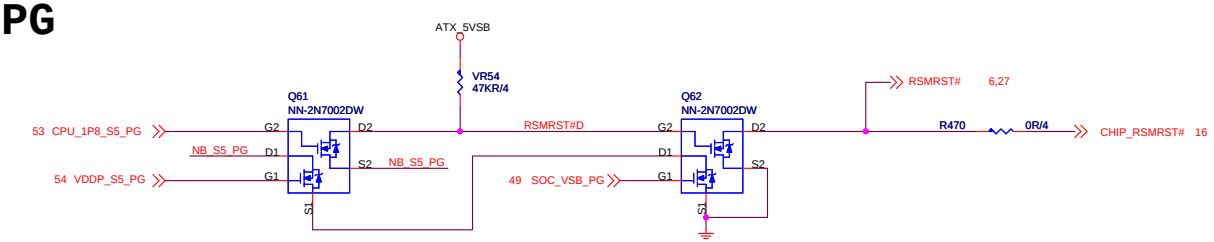


R308 100KR/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



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MS-7C35	
Size: Custom	Document Description: CPU Power Connector/PWRGD
Rev: 11	
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Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vcore: ICC Max 140A
LL: 1.3 mohm
OCP: 480A

SOC: ICC Max 75A
LL: 2.1 mohm
OCP: 100A

Phase 1 close to CPU power pin.

VR_HOT 125

VR_HOT 115

0x26:RH=18K,RL=13K

SMB Address: 0X70

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size: Custom | Document Description: CPU Power IR35201 12 Phase | Rev: 11

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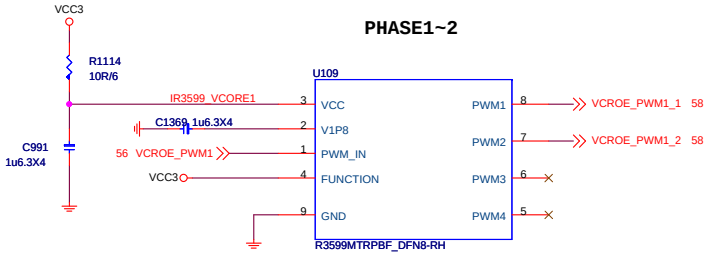
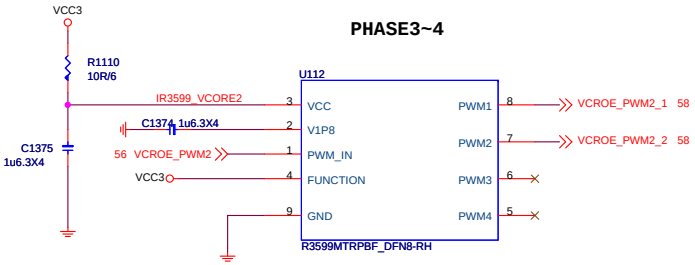
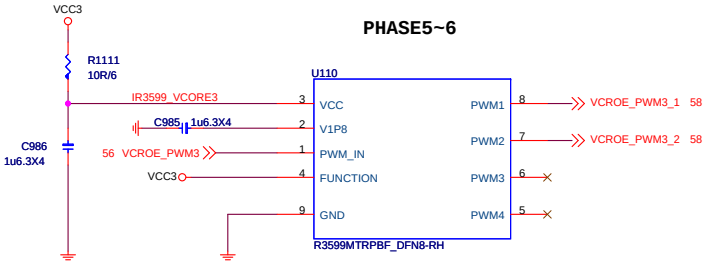
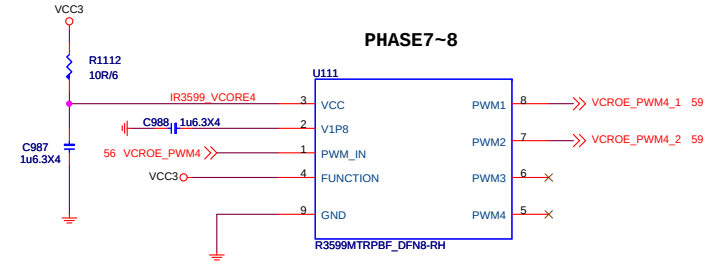
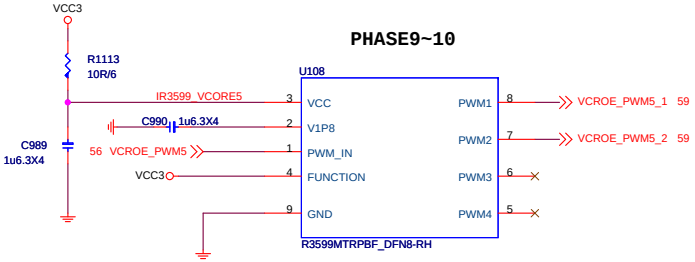
VCORE Double

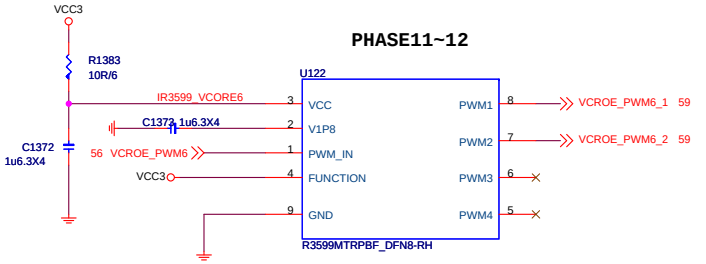




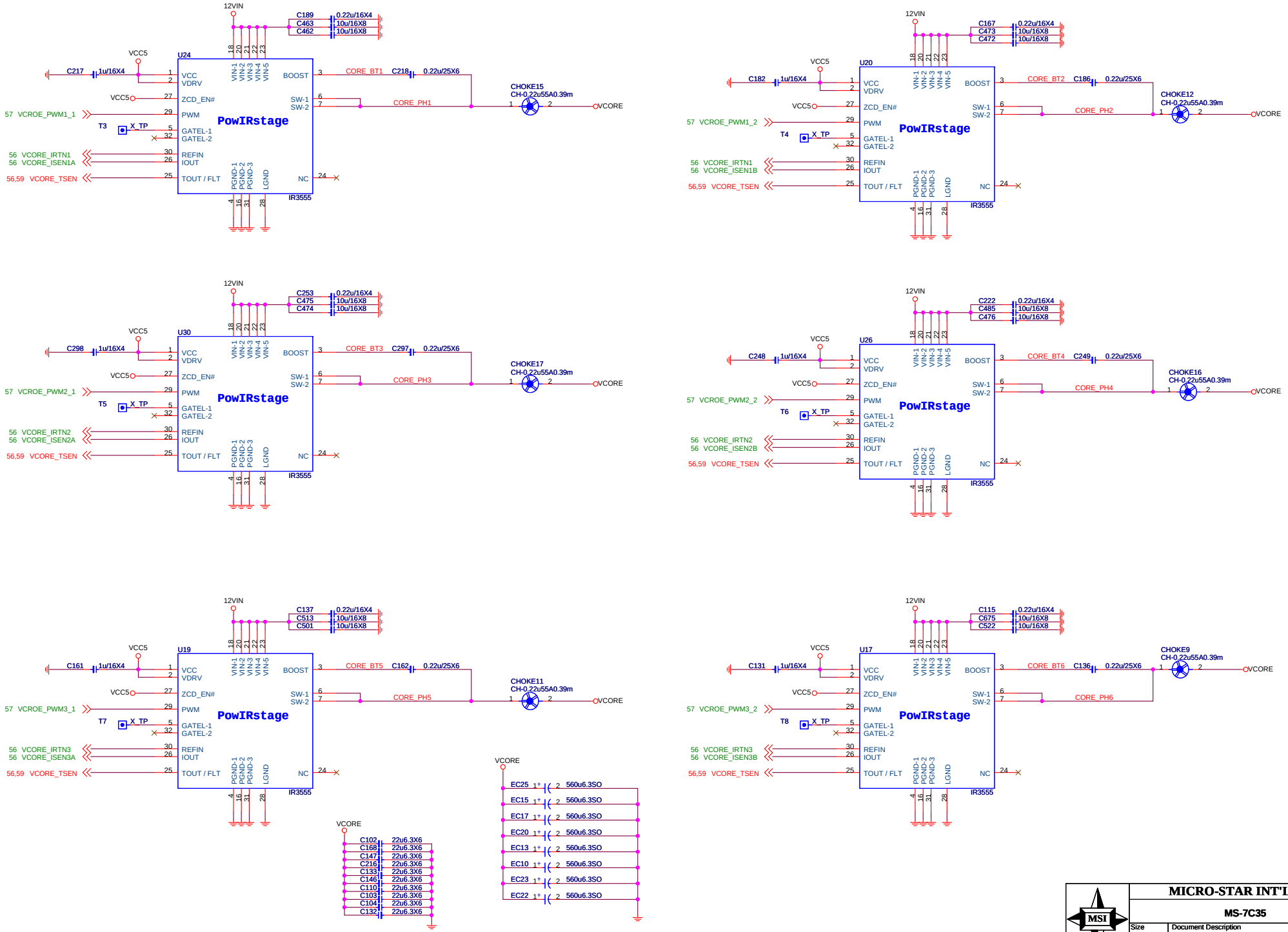




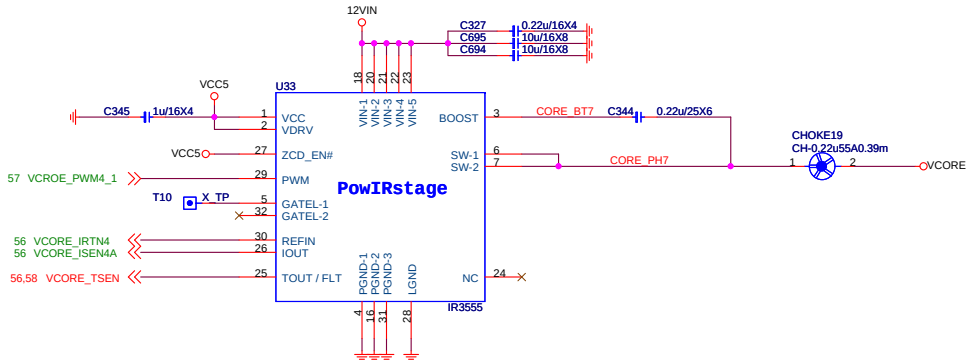


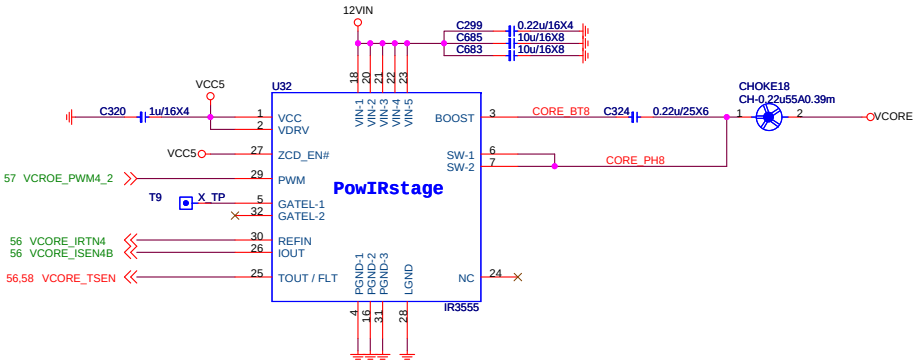


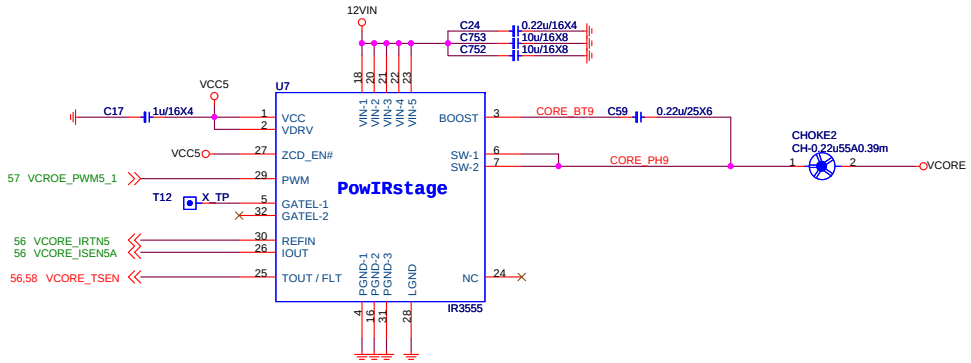
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
Size: Custom	Document Description: CPU Power IR3598	Rev: 11
Date: Thursday, April 04, 2019	Sheet 57 of 75	

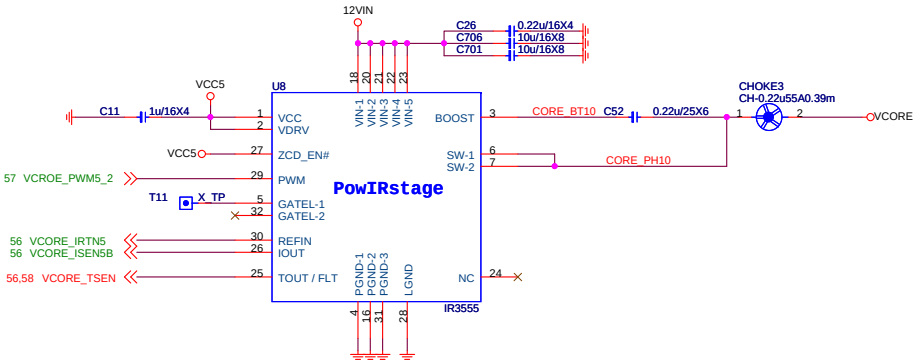


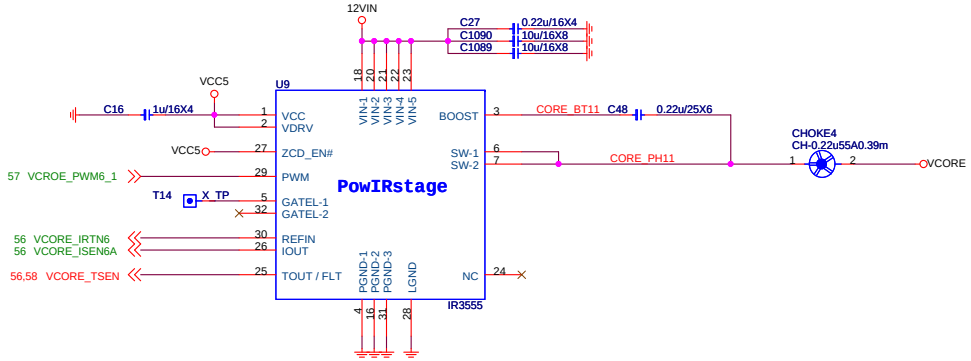
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
Size: Custom	Document Description: CPU Phase 1-4	Rev: 11
Date: Thursday, April 04, 2019	Sheet 58 of 75	

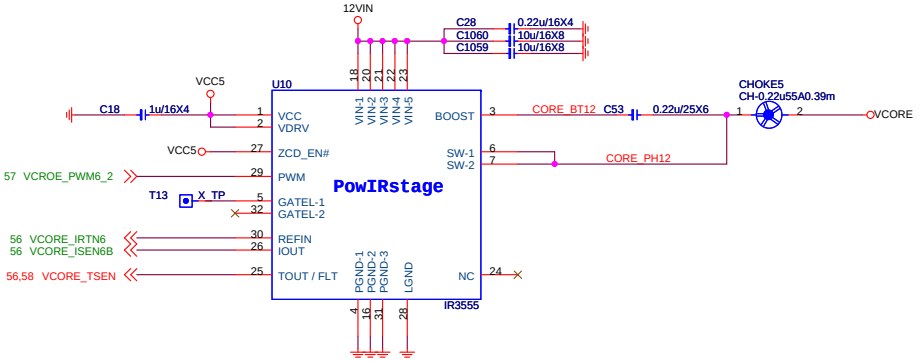












MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C35	
Size: Custom	Document Description: CPU Phase 5-8	Rev: 11
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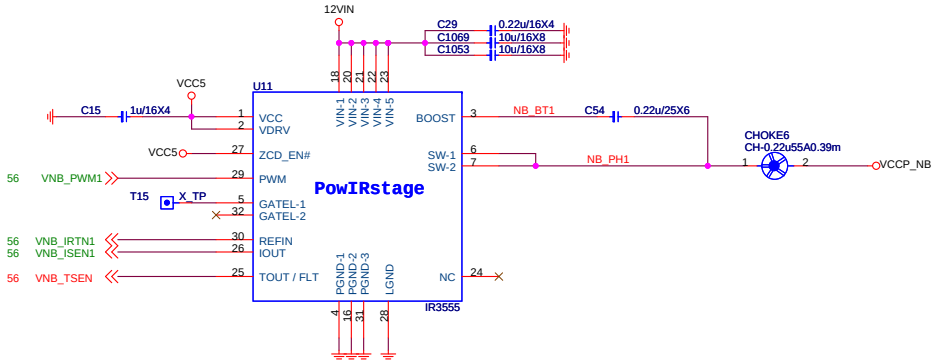
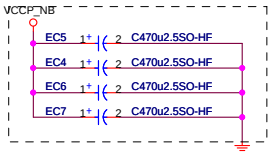
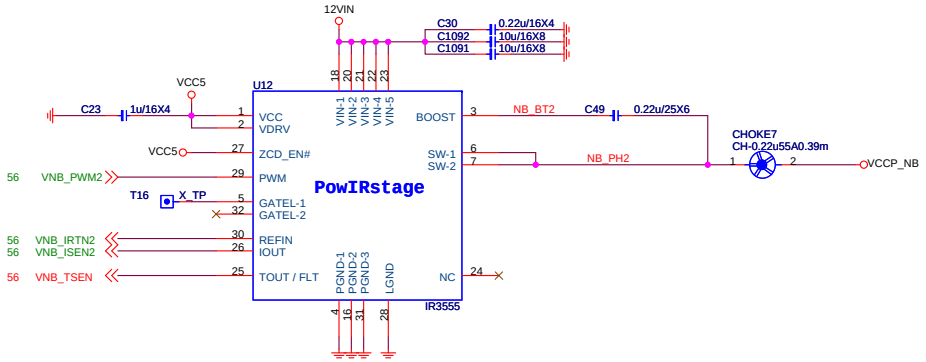
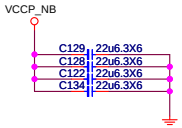




Cange by case.





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MS-7C35		
Size: Custom	Document Description: CPU Phase 9-12 NB Phase 1-2	Rev: 11
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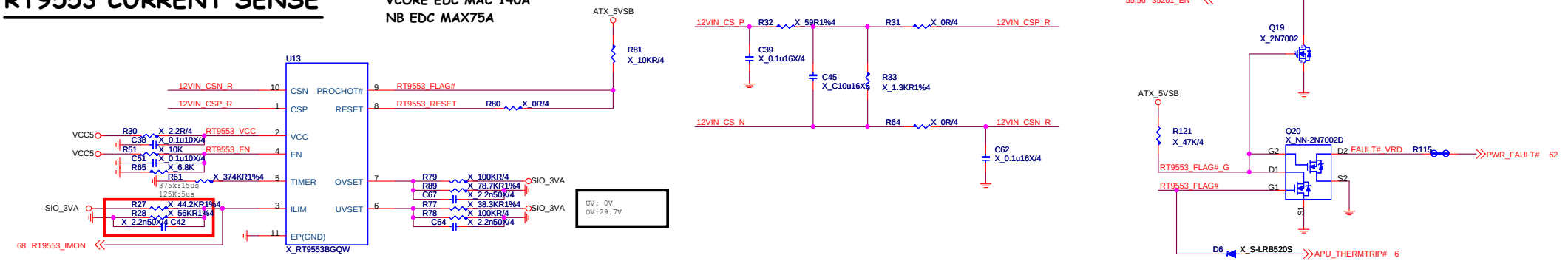
RT9553 CURRENT SENSE

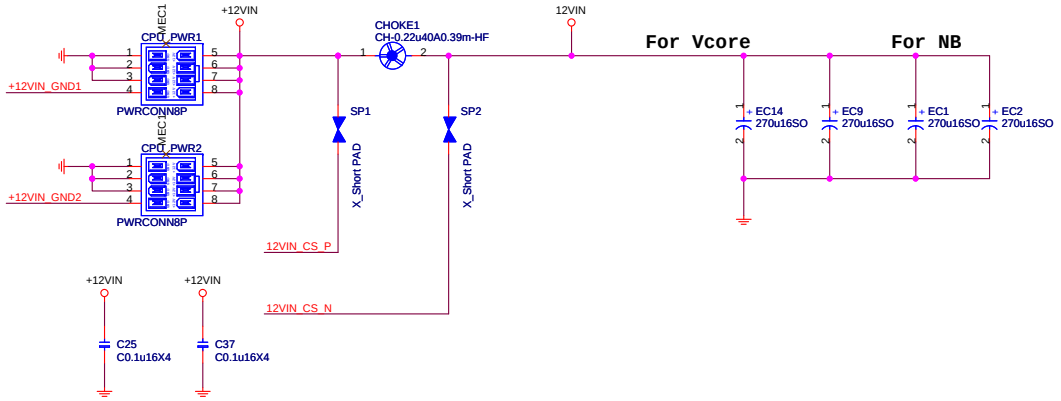
VCORE EDC MAC 140A
NB EDC MAX75A



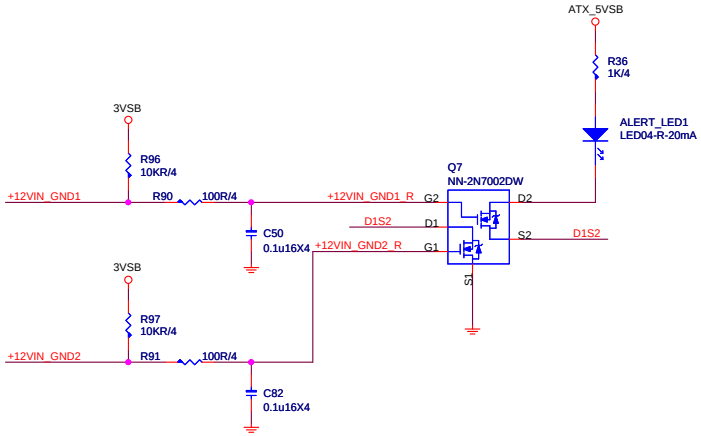
Default:Hi ;Acitve:UP

Vcore:480A ,SOC:100A
OCP:56A

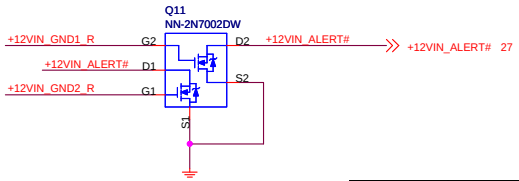
CPU POWER CONNECTOR



Close Power Connector



+12VIN_GND1	+12VIN_GND2	LED	+12VIN_ALERT#(for BIOS show warning message)
0	0	OFF	OFF
0	1	OFF	ON
1	0	OFF	ON
1	1	ON	ON



Irms = Iout * SQRT{D/N- (D)^2]}
CORE:
D=Vout/Vin=1.6/12=0.133
N=Phase number=12
=140A*SQRT(0.133/12-0.133*0.133)
=12A

Iout = 80A,Irms=7.68A

NB:
D=Vout/Vin=1.2/12=0.1
N=Phase number=2
=75A*SQRT(0.05-0.01)
=15A

Iout = 50A,Irms=10A

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size	Document Description	Rev
Custom	RT9553 CURRENT SENSE	11

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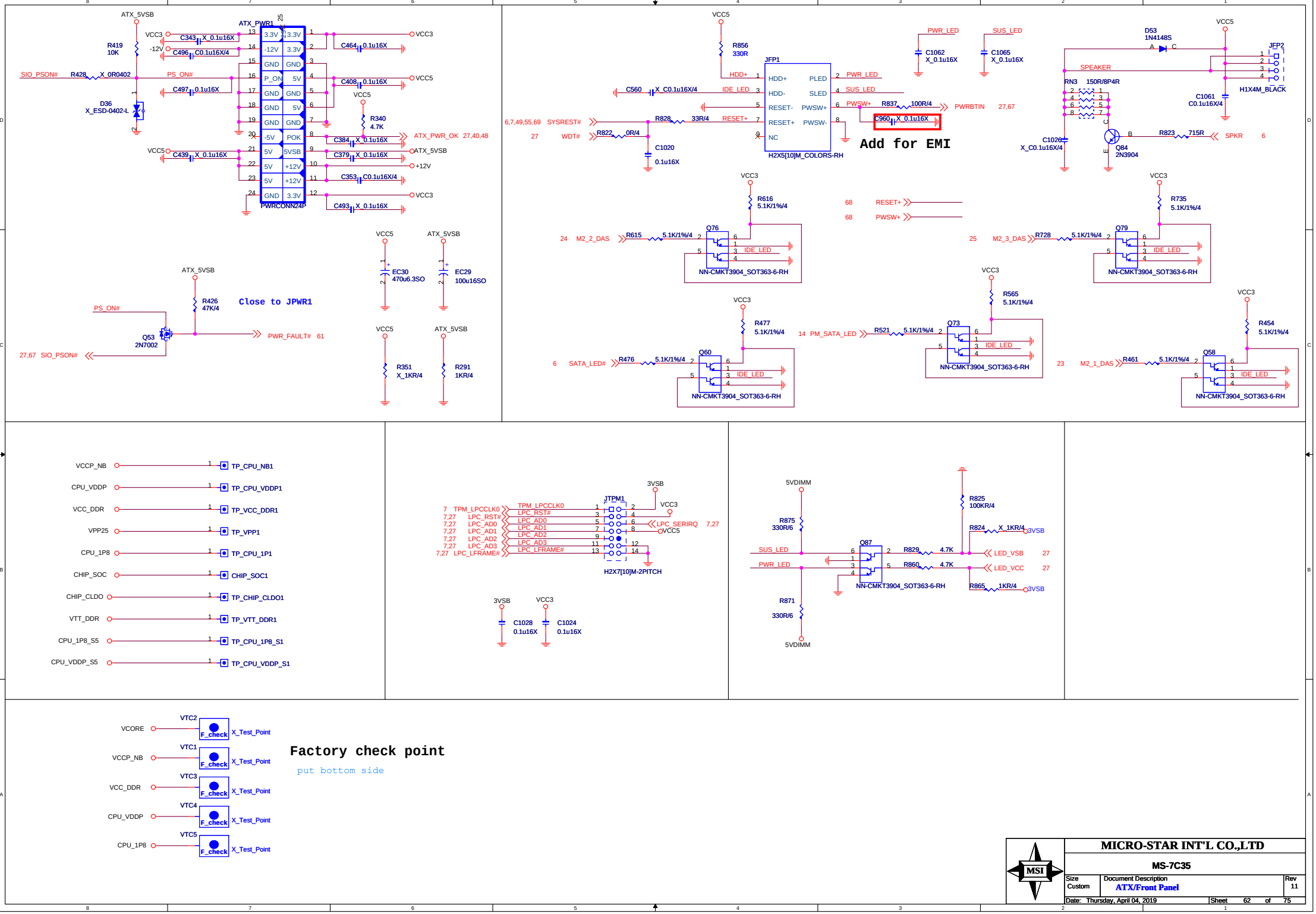
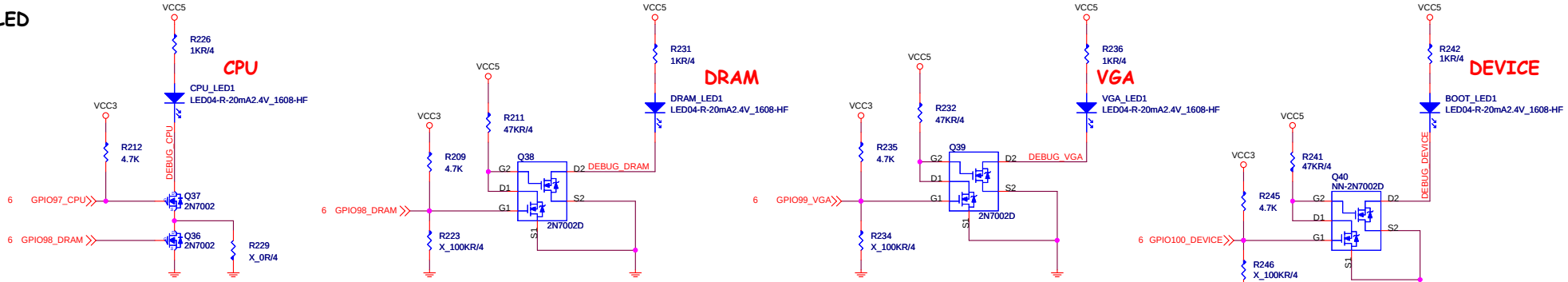
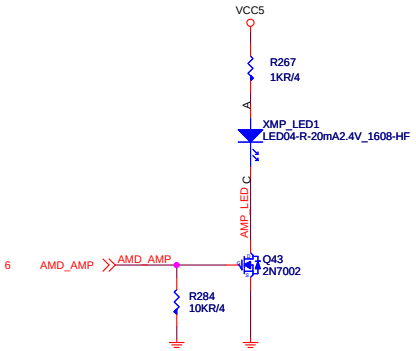


EZ Debug LED



LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獵	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED



LED	x16	x8	x4
PCIE2	Red	White	White

LED \ GPIO	EGPIO95	EGPIO96
獵	GPO PO HIGH	GPO PO HIGH
防	GPI (default LOW)	GPI (default LOW)

MICRO-STAR INT'L CO.,LTD

MS-7C35

Size: Custom | Document Description: EZ-Debug LED Control | Rev: 11

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If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

U81 NUC126NE4AE

PWM1 for JRGB1
RGB LED STRIPLINE USED

PWM3 for Others
According to demand configuration

PWM2 for JRGB2
RGB LED STRIPLINE USED

PIN1 for JPIPE_LED1~3 and JRAINBOW1
PIN46 for JCORSAIR1

PIN44 for JRAINBOW2

COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized onboard LED control.

COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized onboard LED control.
PS. COM1 is the first action block, next is COM2, and so on.

Pin15,16 can configure to master smbus if spec requirement.

C1822 & C1823 near AVDD Pin.
C1820 & C1821 near VDD Pin.
C1824 near VBAT Pin.
C1827 & C1828 near VDDIO & USB_VBUS Pin.

If SPEC hes LED demo function without demo button, DEMO_DET# must pull up to LED_VCC5,Q319 need to stuff and control by LED_VCC5_EN.
PS. R2069 remove, R2032 and Q319 need to stuff

JF1 H1X2M_BLACK-RH

SLOT1 SLOT3 M2_1

EXTERNAL POWER INPUT

U88 RT9742AGJ5F_TSOT23-5-HF
U79 RT9742AGJ5F_TSOT23-5-HF
3 A
min 80mil.

JPWRLED1 BH1X2H-2PITCH_BLACK-HF
2A Connector

JT1 for FW update

JT1 H1X5M_BLACK-HF

IO COVER LED

JPIPE_LED1 BH1X4S-1PITCH-0.74MM_BLACK-HF
N32-1040FH0-H06

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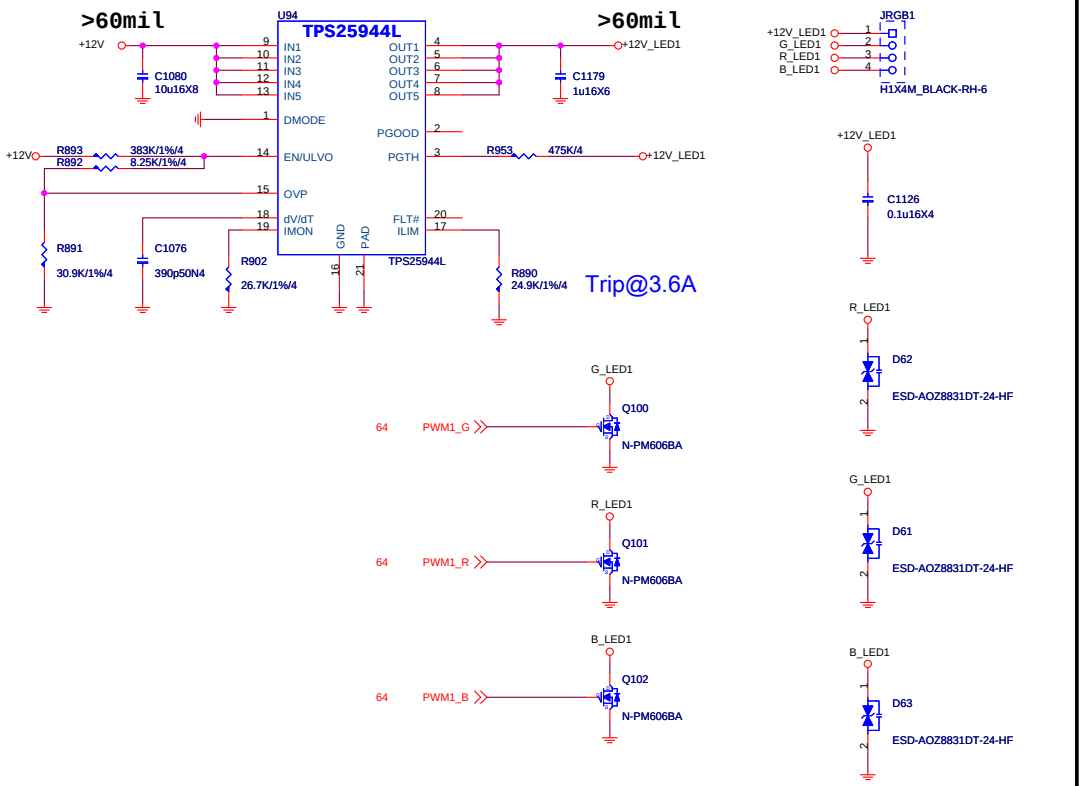
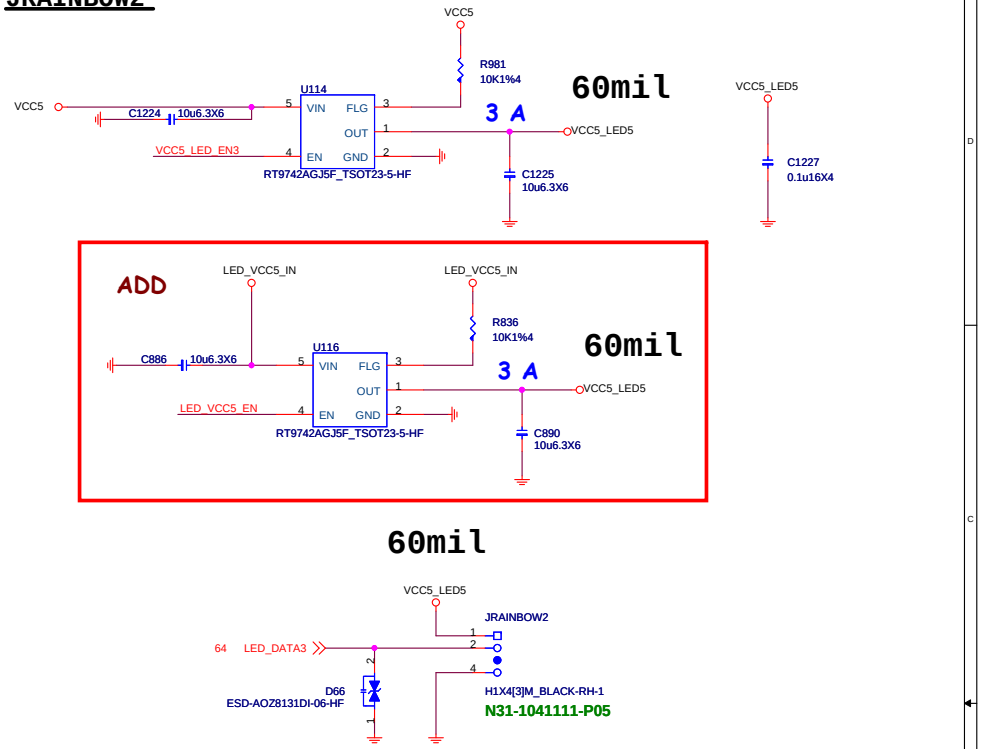
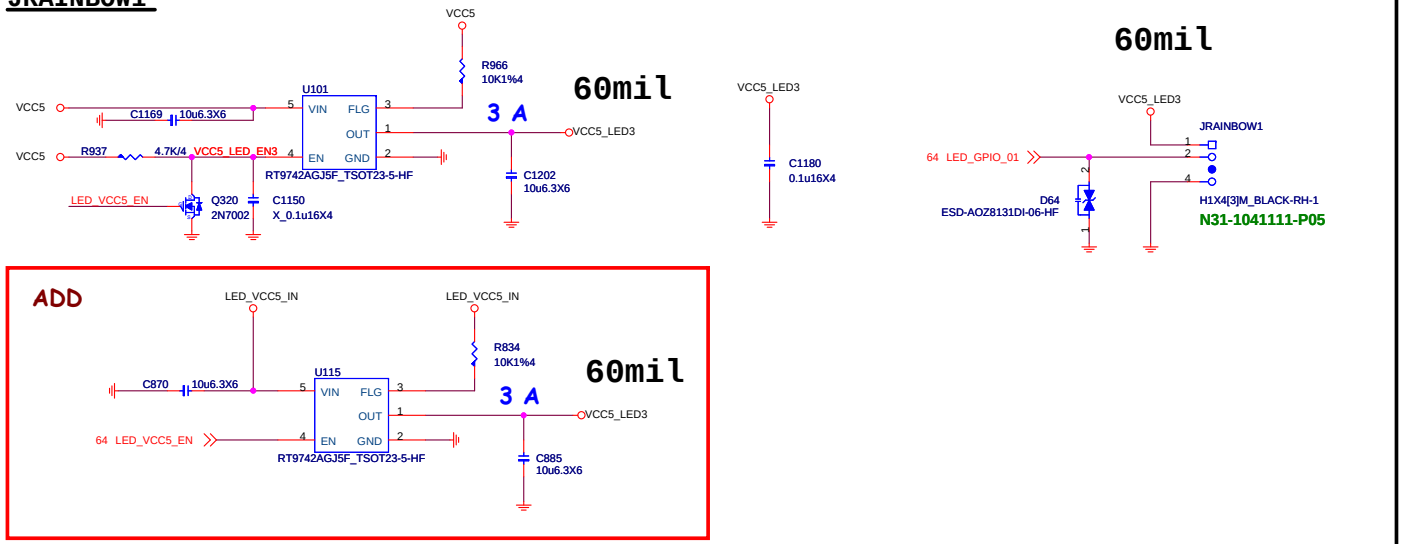
JRGB1



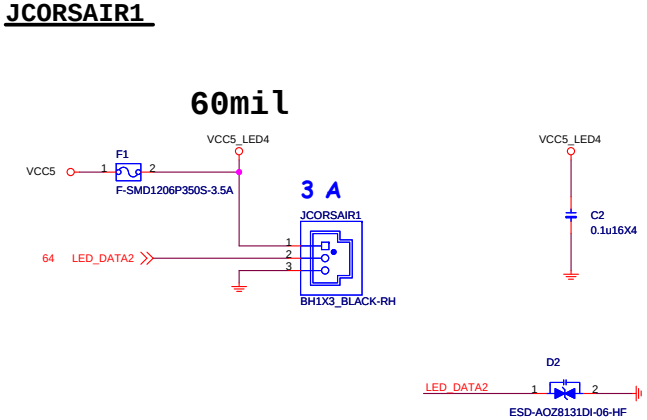
JRAINBOW2



JRAINBOW1



JCORSAIR1



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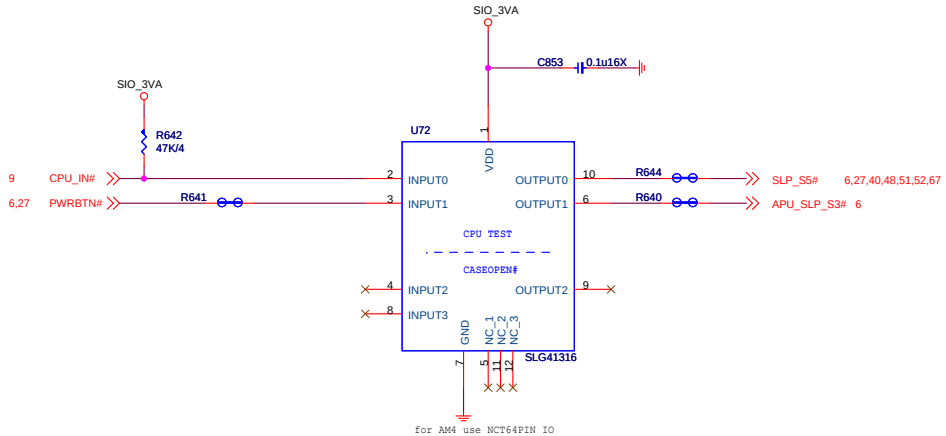
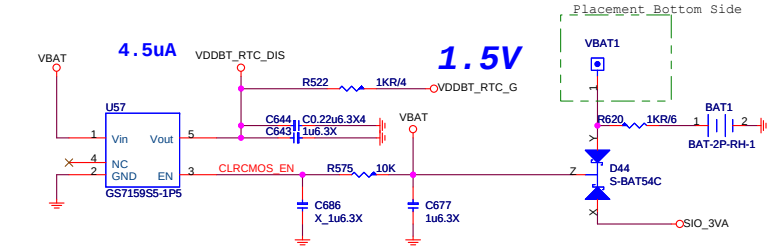
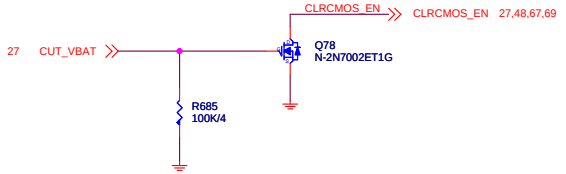
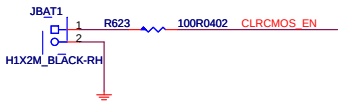
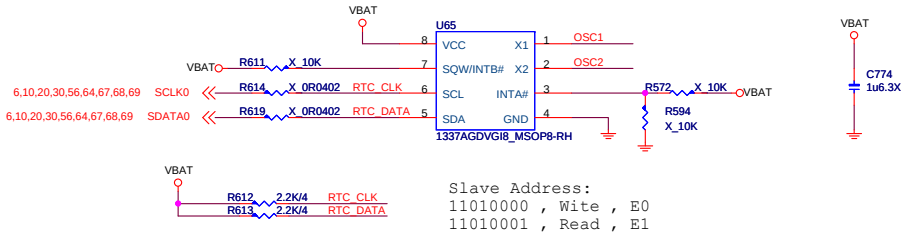


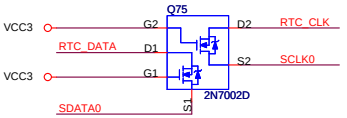
RTC & Clear CMOS Circuit

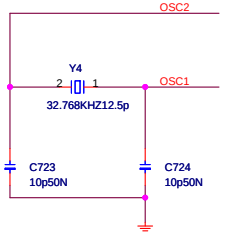












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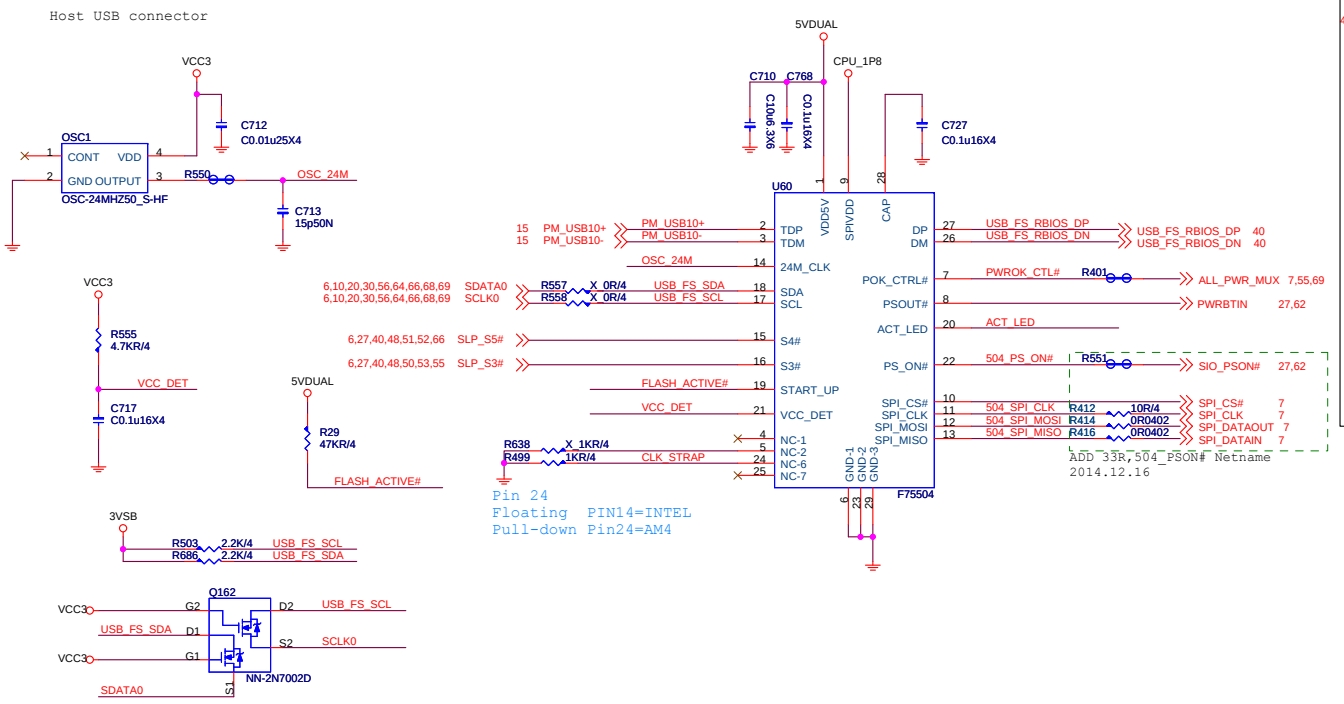
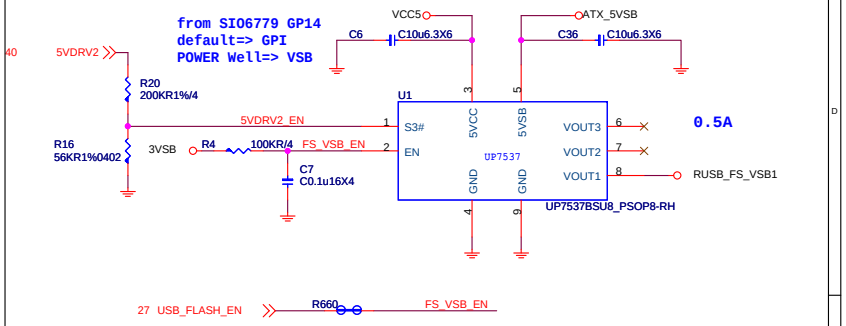
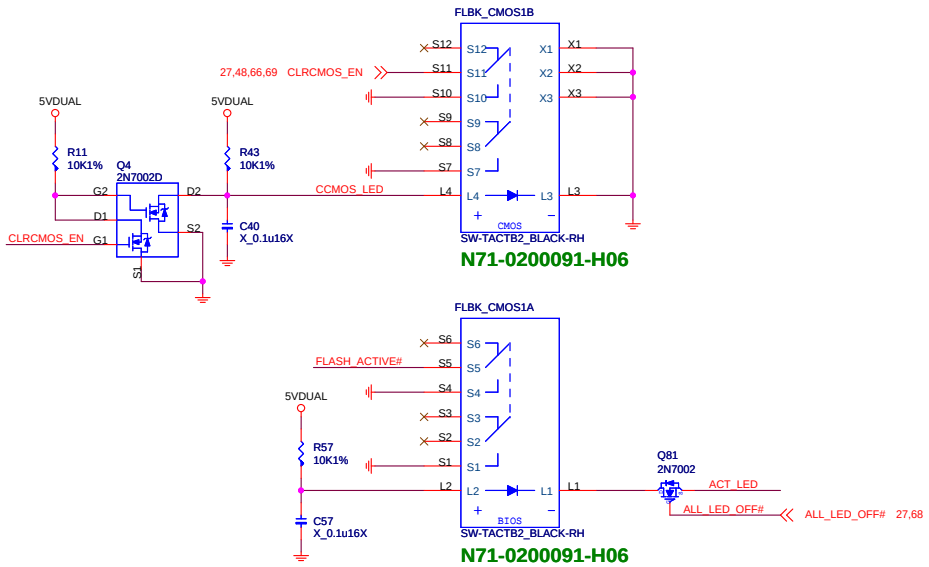
USB Flash BIOS



REAR Flash BIOS USB PORT 9



Clear CMOS&Flash Back button



MICRO-START INT'L CO.,LTD.

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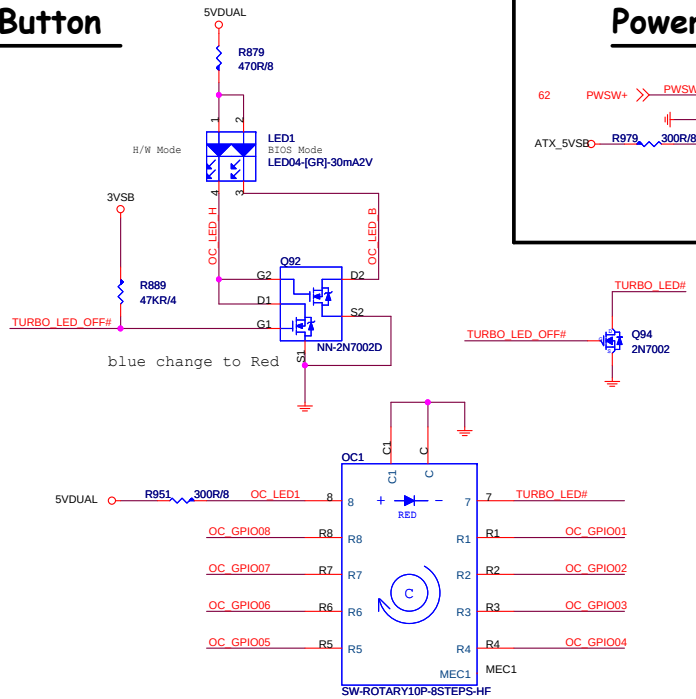
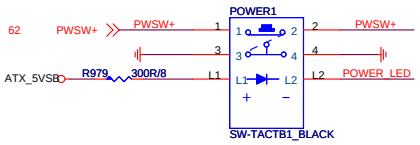
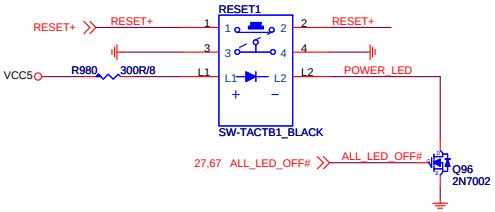
OC Button

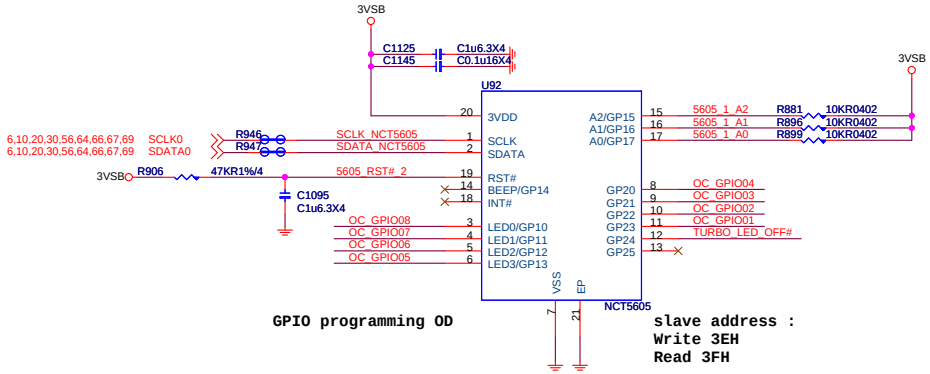


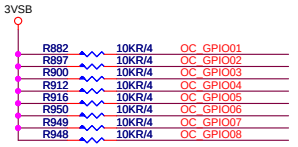
Power ON Button



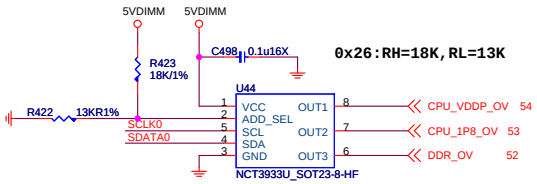
Reset Button

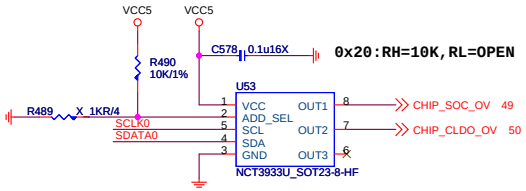


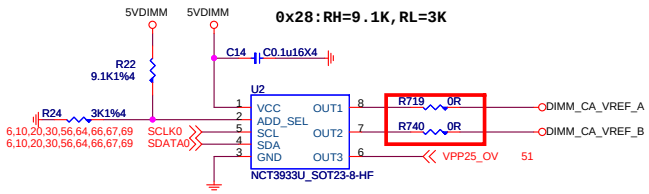


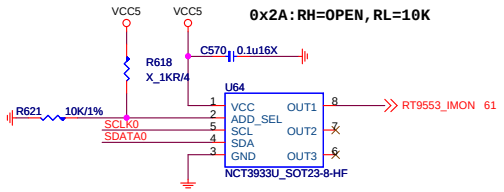


Over Voltage Control IC









UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
	0%	25%	40%	60%	75%	100%

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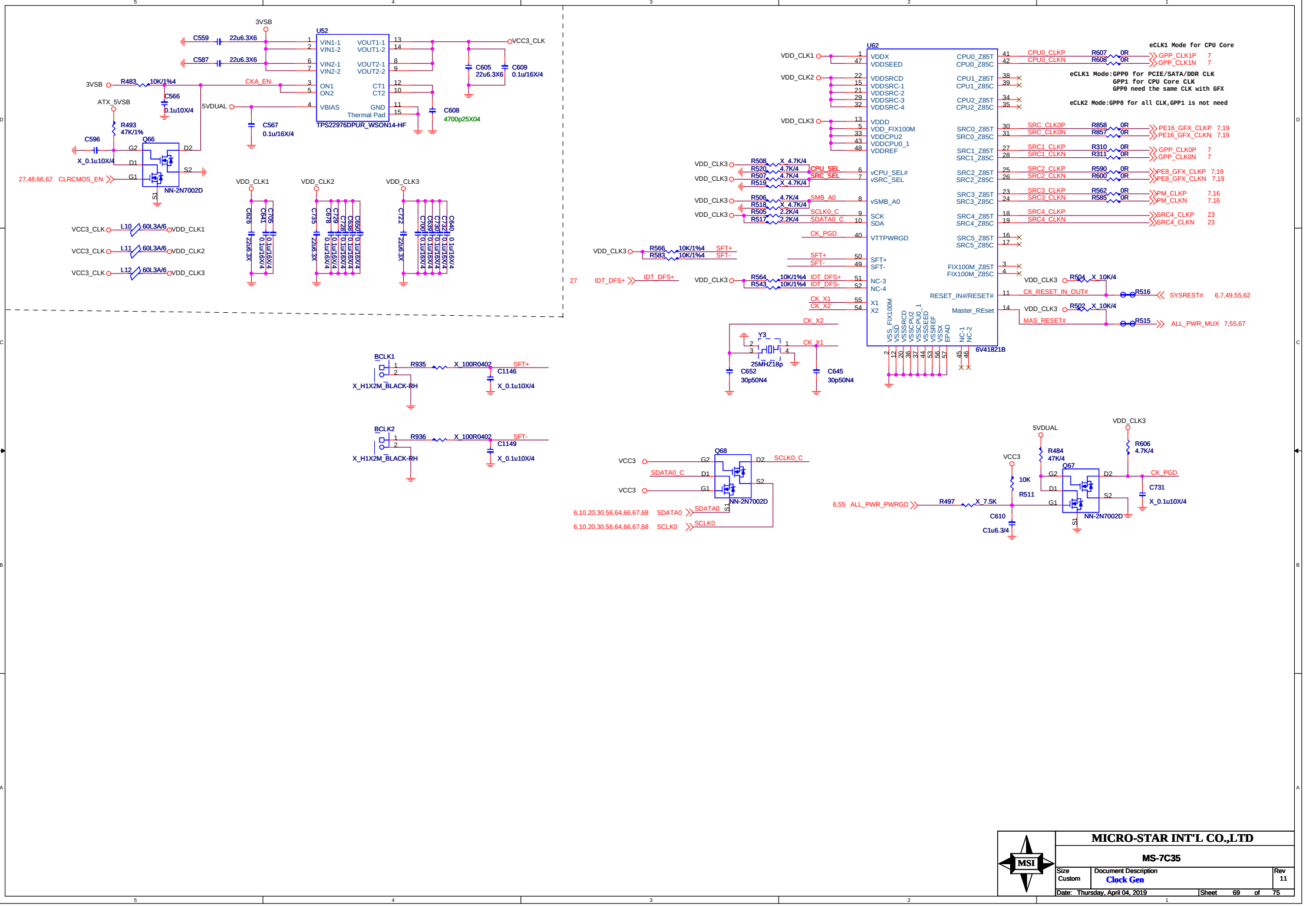

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HEAT SINK

MEC1 MOS_PCH_HS1
MEC2 HS-0408780-RH

MEC1 COVER_M2_HS1
MEC2 HS-0408780-RH

CPU Socket

CPU2
E95-0000021-C22

RETENTION MODULE

Simulation

X_JS3 SIM1 X_PIN1*2
X_JS4 SIM3 X_PIN1*2
X_JS1 SIM2 X_PIN1*2
X_JS2 SIM4 X_PIN1*2

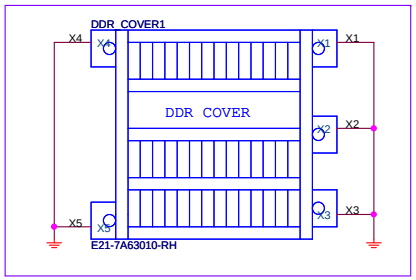
MANUAL PART

UEFI1 G51-M1SPXXA-A09
MKT1 X_G51-M1SPK31-Q13
VIRTUAL3 Nahimic
VIRTUAL1 SLI
VIRTUAL2 SW AP

BAT1_X1
BAT-CR2032-RH

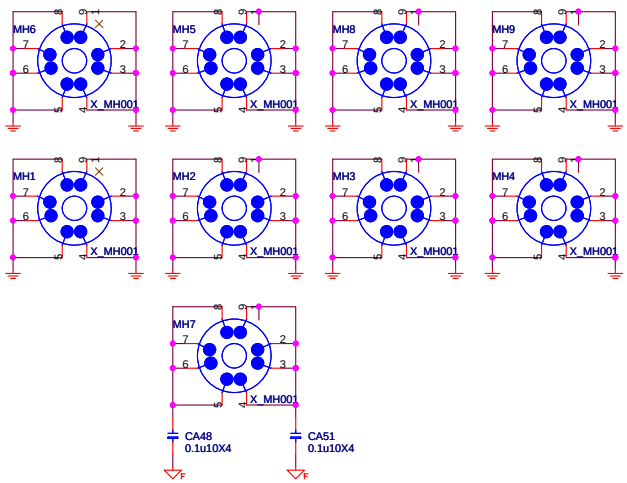
PCB1
7C35
PK0-07A360A-E48,腦地,腳 蛀吹邻紅(MSIS)
PK0-07A360A-G37,弘e-裏 ,腳 蛀吹邻紅(MSIS)

REF1
PCB
PD1-07C350A-G37



0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

Optics Orientation Holes



5010
FM1 FM6 X_FM120 X_FM120
FM5 FM2 X_FM120 X_FM120

5020
FM3 FM4 X_FM120 X_FM120
FM7 FM8 X_FM120 X_FM120

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