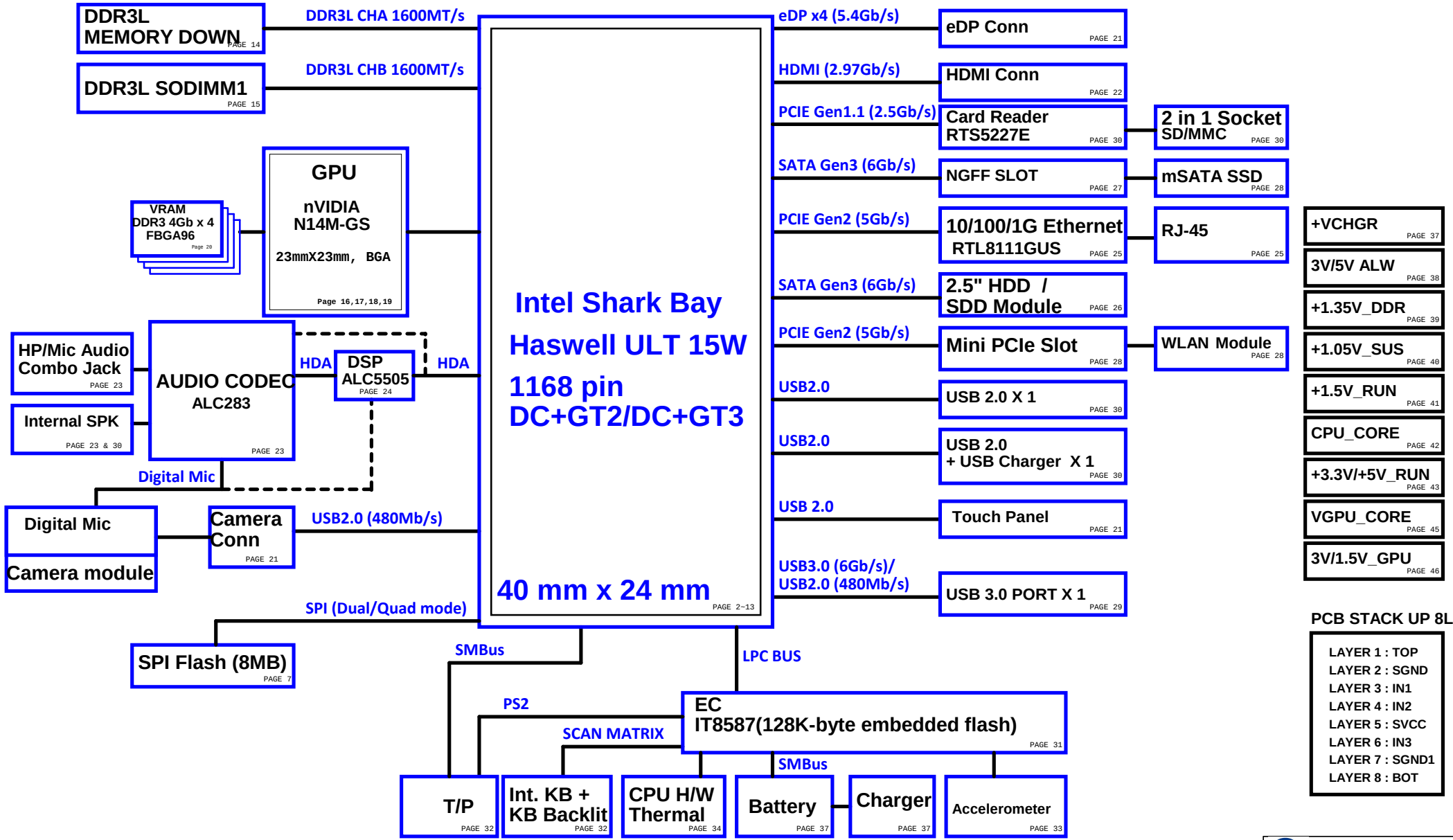
LZ9A 14" OPTIMUS
INTEL SHARK BAY ULT ONE CHIP PLATFORM



PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

PROJECT : LZ9A
Quanta Computer Inc.
System Block Diagram
Rev 1A
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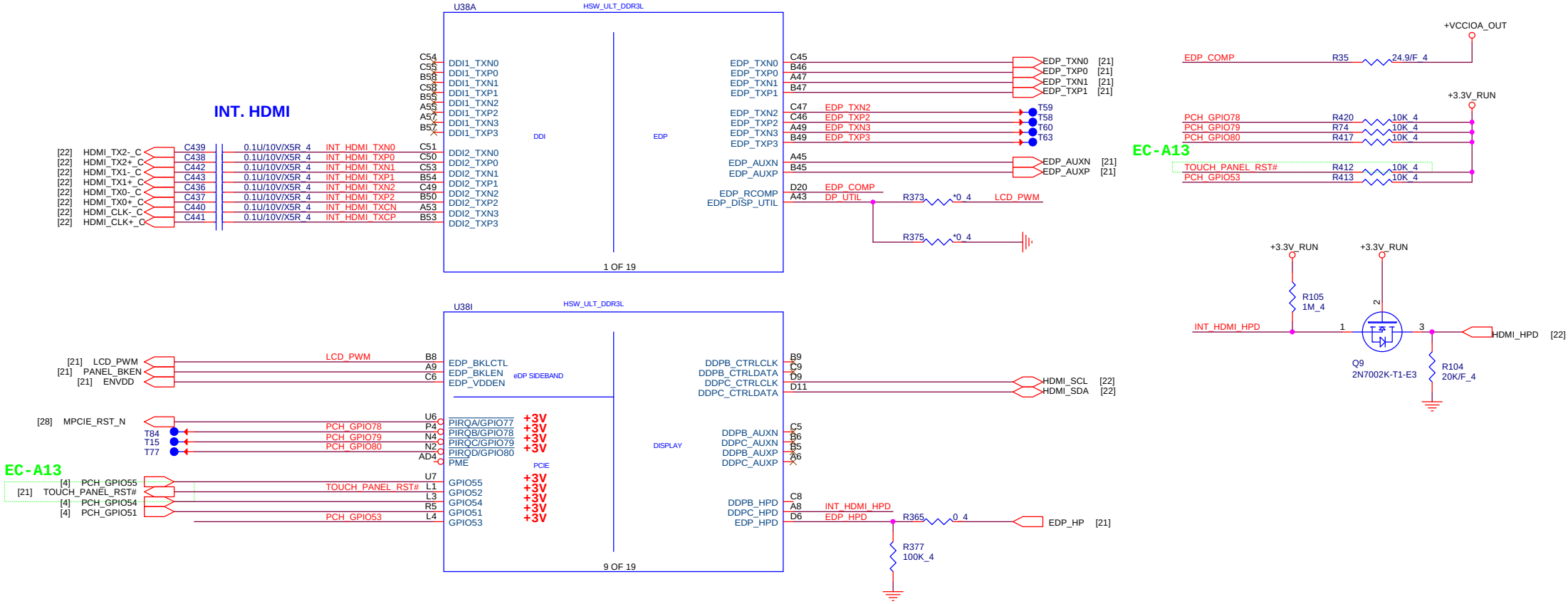
[9] +VCCIOA_OUT
[4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN

Haswell ULT (DISPLAY)



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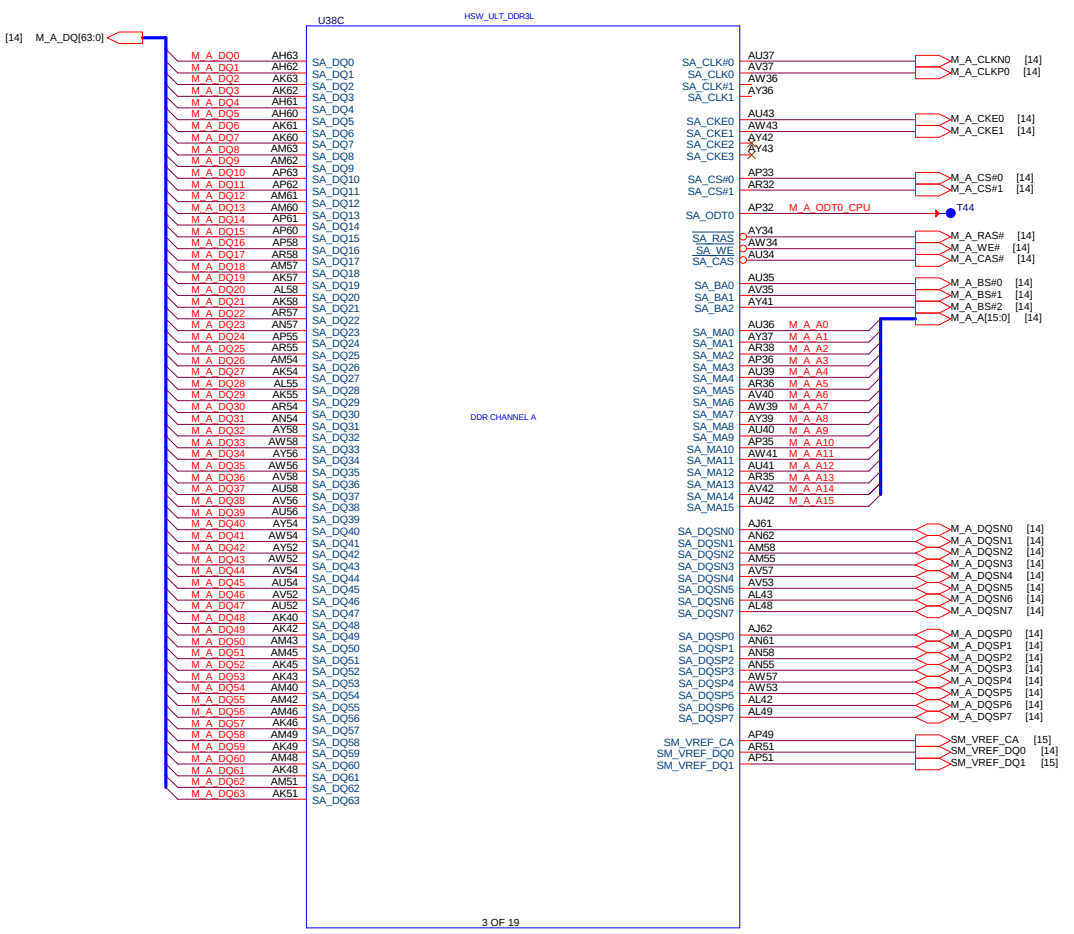
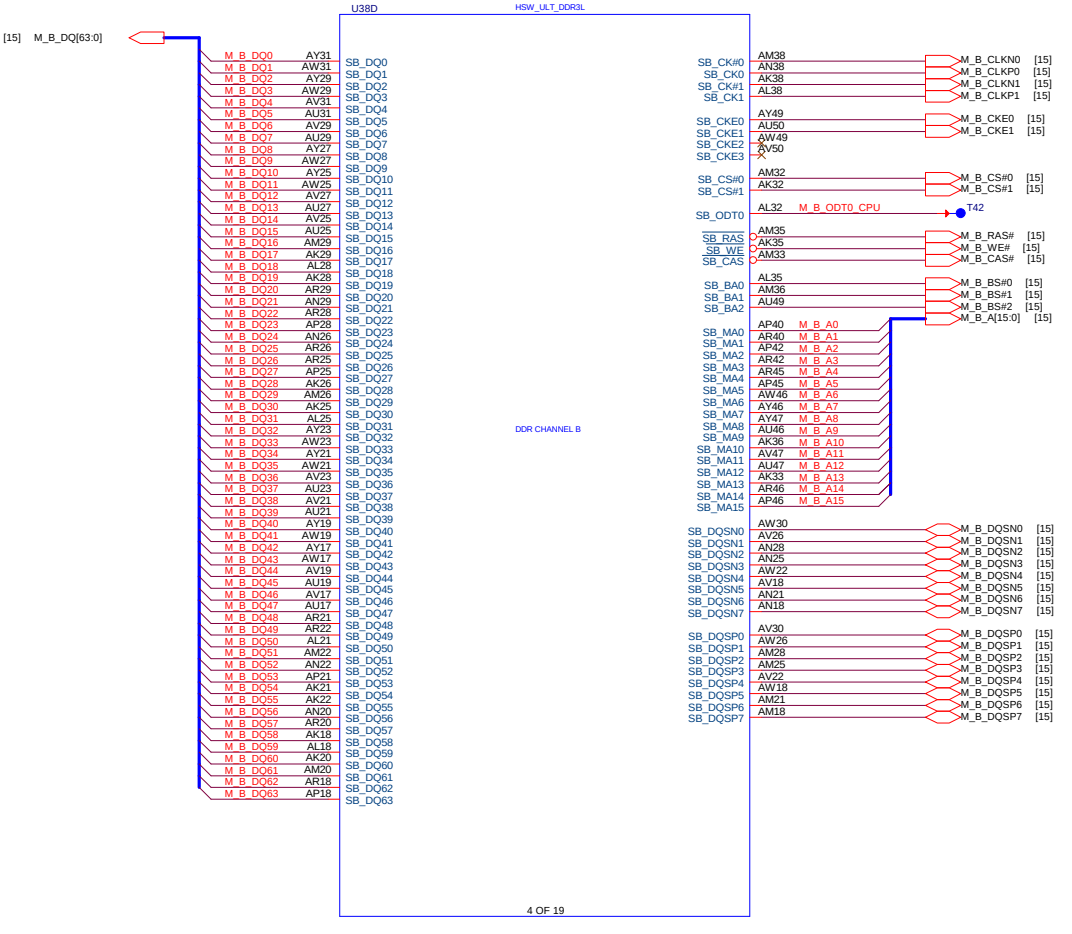
Haswell ULT (DDR3L)





PROJECT : LZ9A

Quanta Computer Inc.

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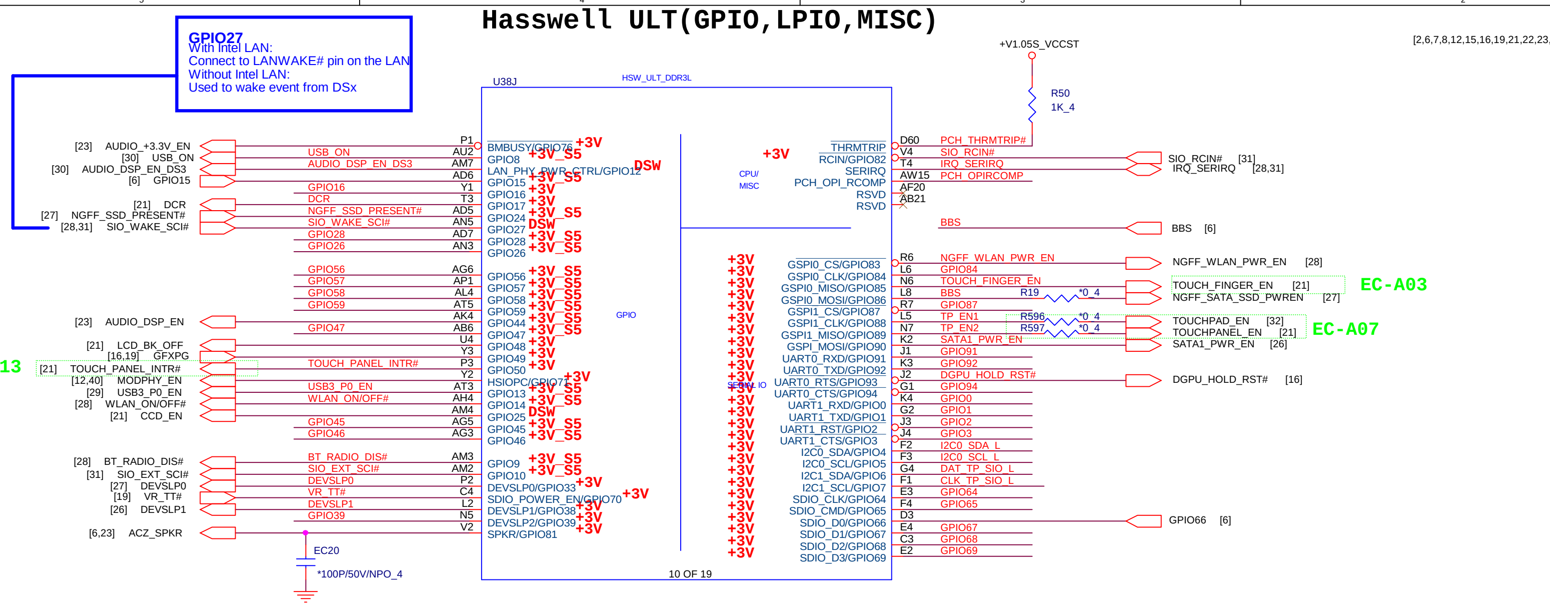
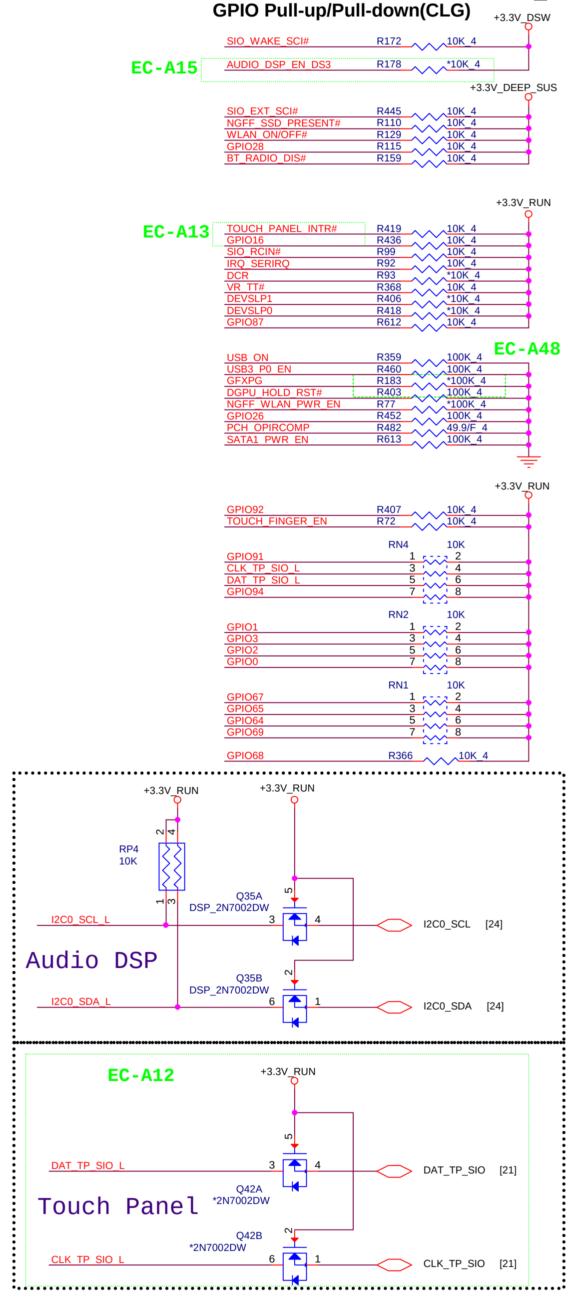
Hasswell ULT(GPIO,LPIO,MISC)

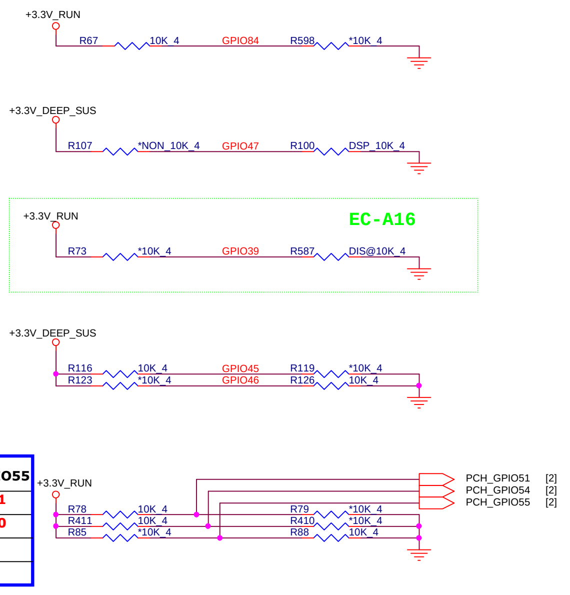




Thunderbolt ID	GPIO84
Supported	0
Not Supported	1

Audio DSP ID	GPIO47
Supported	0
Not Supported	1

DGPU SELECT	GPIO39
Supported	0
Not Supported	1

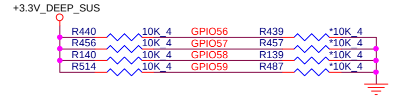


Model ID	GPIO45	GPIO46
LZ5-UMA	0	0
LZ9-UMA	0	1
LZ9A-DIS	1	0
LZA	1	1

Board ID	GPIO51	GPIO54	GPIO55
SDV	1	1	1
SIV	1	1	0
SIT			
SVT			

DDR3L Memory Down ID Table

Vendor	Description	Size	Quanta P/N	GPIO[56,57,58,59]
Default				1111
Samsung	K4B8G1646B-MYK0 (B/4Gb/35nm/DDP)	8Gb x 16	AKD5FGET500	1110
Micron	MT41K512M16TNA-125:E(V80A/4Gb/30nm/DDP)	8Gb x 16	AKD5FGSTL00	1101
ELPIDA	EDJ8416E6MB-GN-F(F/4Gb/30nm/DDP)	8Gb x 16	AKD5FGST402	1100
SK hynix		8Gb x 16		XXXX
Samsung	K4B4G1646B-HYK0(B/4Gb/35nm)	4Gb x 16	AKD5PGET500	1011
Micron	MT41K256M16HA-125:E(V80A/4Gb/30nm)	4Gb x 16	AKD5JGSTL02	1010
ELPIDA	EDJ4216EFBG-GN-F(F/4Gb/30nm)	4Gb x 16	AKD5JGST403	1001
SK hynix	H5TC4G63AFR-PBA(D/4Gb/29nm)	4Gb x 16	AKD5JGETW00	1000



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[4,6,7,8,12,15] +3.3V_DEEP_SUS
[12] +V1.05S_AUSB3PLL

5

Haswell ULT (PCIE,USB)

U38K HSW_ULT_DDR3L

VGA
WiFi/BT
Card Reader
LAN (Select PCIE)

PCIE

[16] PEG_RXN0					F10	PERN5_L0	
[16] PEG_RXP0					E10	PERP5_L0	
[16] PEG_TXN0	C447	0.1U/10V/X5R_4	PEG_TXN0_C	C23	PETN5_L0		
[16] PEG_TXP0	C444	0.1U/10V/X5R_4	PEG_TXP0_C	C22	PETP5_L0		
[16] PEG_RXN1					F8	PERN5_L1	
[16] PEG_RXP1					E8	PERP5_L1	
[16] PEG_TXN1	C425	0.1U/10V/X5R_4	PEG_TXN1_C	B23	PETN5_L1		
[16] PEG_TXP1	C424	0.1U/10V/X5R_4	PEG_TXP1_C	A23	PETP5_L1		
[16] PEG_RXN2					H10	PERN5_L2	
[16] PEG_RXP2					G10	PERP5_L2	
[16] PEG_TXN2	C422	0.1U/10V/X5R_4	PEG_TXN2_C	B21	PETN5_L2		
[16] PEG_TXP2	C423	0.1U/10V/X5R_4	PEG_TXP2_C	C21	PETP5_L2		
[16] PEG_RXN3					E6	PERN5_L3	
[16] PEG_RXP3					F6	PERP5_L3	
[16] PEG_TXN3	C446	0.1U/10V/X5R_4	PEG_TXN3_C	B22	PETN5_L3		
[16] PEG_TXP3	C445	0.1U/10V/X5R_4	PEG_TXP3_C	A21	PETP5_L3		
[28] PCIE_RXN3					G11	PERN3	
[28] PCIE_RXP3					F11	PERP3	
[28] PCIE_TXN3	C451	0.1U/10V/X5R_4	PCIE_TXN3_C	C29	PETN3		
[28] PCIE_TXP3	C452	0.1U/10V/X5R_4	PCIE_TXP3_C	B30	PETP3		
[30] PCIE_RXN4					F13	PERN4	
[30] PCIE_RXP4					G13	PERP4	
[30] PCIE_TXN4	C450	0.1U/10V/X5R_4	PCIE_TXN4_C	B29	PETN4		
[30] PCIE_TXP4	C449	0.1U/10V/X5R_4	PCIE_TXP4_C	A29	PETP4		
[25] PCIE_RXN5					G17	PERN1/USB3RN3	
[25] PCIE_RXP5					F17	PERP1/USB3RP3	
[25] PCIE_TXN5	C427	0.1U/10V/X5R_4	PCIE_TXN5_C	C30	PETN1/USB3TN3		
[25] PCIE_TXP5	C428	0.1U/10V/X5R_4	PCIE_TXP5_C	C31	PETP1/USB3TP3		
					F15	PERN2/USB3RN4	
					G15	PERP2/USB3RP4	
					B31	PETN2/USB3TN4	
					A31	PETP2/USB3TP4	
+V1.05S_AUSB3PLL							
	R25	3K/F_4	PCIE_RCOMP	A27	RSVD		
	R32	0_4	PCIE_IREF	B27	RSVD		
					E15	PCIE_RCOMP	
					E13	PCIE_IREF	

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USB

AN8	USB2N0		USB-_TPanel	[21]
AM8	USB2P0		USB+_TPanel	[21]
AR7	USB2N1		USBP1-	[29]
AT7	USB2P1		USBP1+	[29]
AR8	USB2N2		USBP2-	[30]
AP8	USB2P2		USBP2+	[30]
AR10	USB2N3		USBP3-	[30]
AT10	USB2P3		USBP3+	[30]
AM15	USB2N4		USBP4-	[21]
AL15	USB2P4		USBP4+	[21]
AM13	USB2N5		USBP5-	[28]
AN13	USB2P5		USBP5+	[28]
AP11	USB2N6			
AN11	USB2P6			
AR13	USB2N7			
AP13	USB2P7			
G20	USB3RN1		USB30_RX1-	[29]
H20	USB3RP1		USB30_RX1+	[29]
C33	USB3TN1		USB30_TX1-	[29]
B34	USB3TP1		USB30_TX1+	[29]
E18	USB3RN2			
F18	USB3RP2			
B33	USB3TN2			
A33	USB3TP2			

AJ10	USBRBIAS	USB_BIAS	R125	22.6/F_4	
AJ11	USBRBIAS				
AN10	RSVD	USBPLLMON_N	R165	49.9/F_4	
AM10	RSVD	USBPLLMON_P	R164	49.9/F_4	

+3V_S5	AL3	OC0/GPIO40	USB_OC0#	USB_OC0# [29]
+3V_S5	AT1	OC1/GPIO41	USB_OC1#	USB_OC1# [30]
+3V_S5	AH2	OC2/GPIO42	USB_OC2#	
+3V_S5	AV3	OC3/GPIO43	USB_OC3#	

+3.3V_DEEP_SUS

RP9 10K
USB_OC3# 4 3
USB_OC1# 2 1

RP5 10K
USB_OC2# 4 3
USB_OC0# 2 1

Touch Panel
USB3.0 Port 1 (CN7)
USB2.0 Port 1
USB2.0 Port 2
CAMERA
WLAN / BT NGFF
USB3.0 Port 1 (CN7)

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Quanta Computer Inc.

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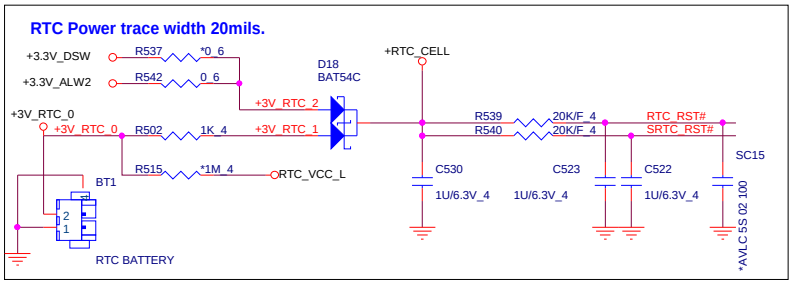
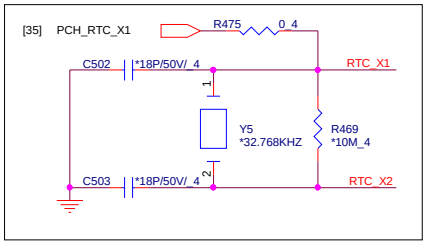
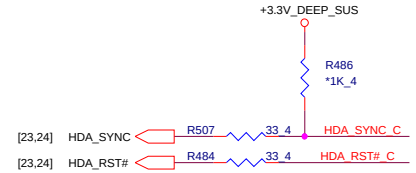
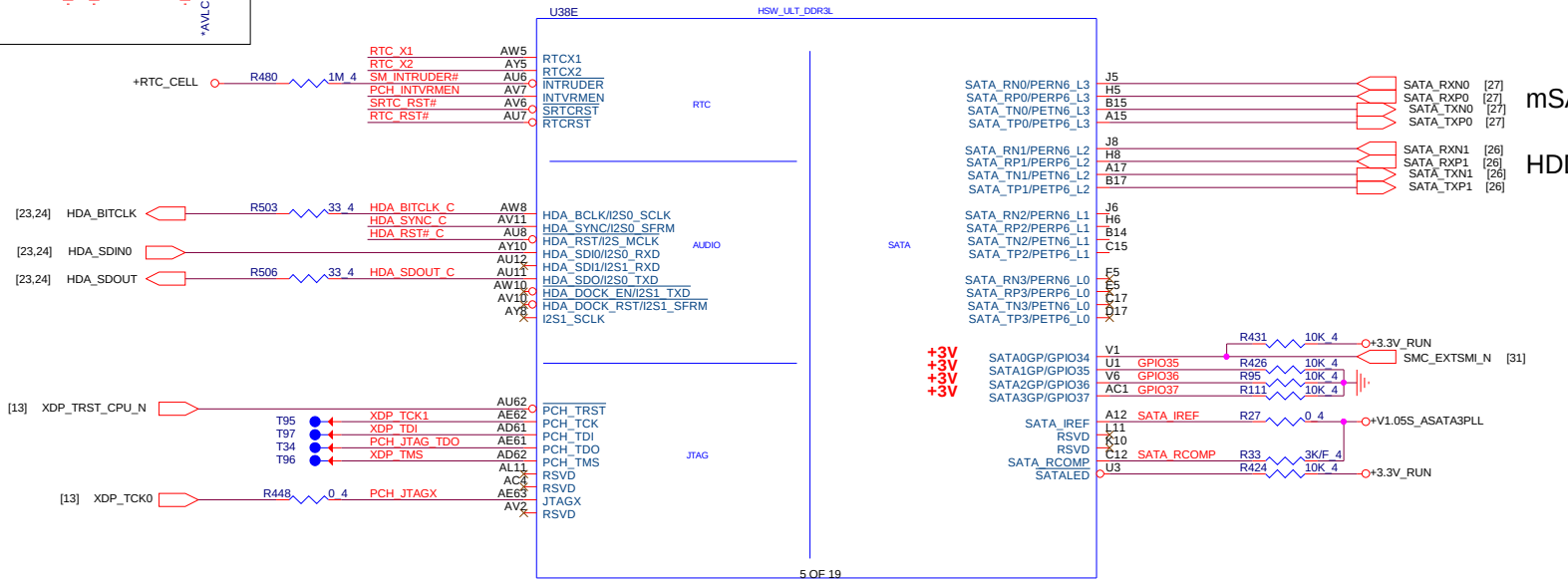
Haswell ULT (RTC, HDA, JTAG, SATA)









mSATA

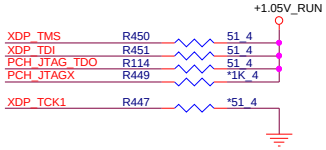
HDD

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R427 *1K_4 ACZ_SPKR [4,23]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	[31] ME_WR# R485 1K_4 HDA_SDOUT_C EC-A22
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R508 330K_4 PCH_INTVRMEN R479 *330K_4
GPIO66	Top-Block Swap override		**0 = Default disable (iPD 20K)** 1 = Enable TBS function	+V3.3S_1.8S_LPSS_SDIO R378 *1K_4 GPIO66 [4] R396 *1K_4
GPIO86	BBS(Boot BIOS Strap Bit)		**0 = Default SPI (iPD 20K)** 1 =LPC	+3.3V_RUN R34 *1K_4 BBS [4] R31 *1K_4
GPIO15	TLS(Transport layer security)		**0 = Default enable w/o confidentiality(iPD 20K)** 1 =Default enable with confidentiality	+3.3V_DEEP_SUS R112 *10K_4 GPIO15 [4]
DSWVREN	Deep Sx well on die DSW VR enable		**1=Should be always pull-up**	+RTC_CELL R481 330K_4 DSWVREN [8]

PCH JTAG Debug (CLG)

MP remove(Intel)



[2,4,6,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[4,5,6,8,12,15] +3.3V_DEEP_SUS
[6,9,12,35,40,44,46] +1.05V_RUN
[12] +V1.05S_AXCK_LCPLL

Haswell ULT (CLK)

U38F HSW_ULT_DDR3L

Card Reader
LAN
WiFi/BT(NGFF)
VGA

[30] CLK_PCIE_CRDN
[30] CLK_PCIE_CRDP
[30] PCIE_CLK_REQ2#
[25] CLK_PCIE_LANN
[25] CLK_PCIE_LANP
[25] PCIE_CLK_REQ3#
[28] CLK_PCIE_WIFIN
[28] CLK_PCIE_WIFIP
[28] PCIE_CLK_REQ4#
[16] CLK_PCIE_VGAN
[16] CLK_PCIE_VGAP
[16] CLK_PEGA_REQ#

PCIE_CLK_REQ0# → U2 CLKOUT_PCIE_N0 / C43, CLKOUT_PCIE_P0 / C42 → PCIECLKRQ0/GPIO18 +3V
PCIE_CLK_REQ1# → Y5 CLKOUT_PCIE_N1 / B41, CLKOUT_PCIE_P1 / A41 → PCIECLKRQ1/GPIO19 +3V
PCIE_CLK_REQ2# → AD1 CLKOUT_PCIE_N2 / C41, CLKOUT_PCIE_P2 / B42 → PCIECLKRQ2/GPIO20 +3V
PCIE_CLK_REQ3# → N1 CLKOUT_PCIE_N3 / B38, CLKOUT_PCIE_P3 / C37 → PCIECLKRQ3/GPIO21 +3V
PCIE_CLK_REQ4# → U5 CLKOUT_PCIE_N4 / A39, CLKOUT_PCIE_P4 / B39 → PCIECLKRQ4/GPIO22 +3V
CLK_PEGA_REQ# → T2 CLKOUT_PCIE_N5 / B37, CLKOUT_PCIE_P5 / A37 → PCIECLKRQ5/GPIO23 +3V

CLOCK SIGNALS

XTAL24_IN A25, XTAL24_OUT B25
RSVD K21, RSVD M21, DIFFCLK_BIASREF C26
TESTLOW_C35 C35, TESTLOW_C34 C34, TESTLOW_AK8 AK8, TESTLOW_AL8 AL8
CLKOUT_LPC_0 AN15, CLKOUT_LPC_1 AP15
CLKOUT_ITPXDP B35, CLKOUT_ITPXDP_P A35

R363 0_4 PCH_XTAL24_IN [35]
C432 *12P/50V_4
Y4 *24MHz
R374 *1M_4
C433 *12P/50V_4
R379 3K/F_4 +V1.05S_AXCK_LCPLL
R177 22_4, R176 22_4 CLKOUT_LPC_0 [31] / PCLK_DEBUG [28]
C196 *10P/50V_4

TESTLOW_0 TESTLOW_1 TESTLOW_2 TESTLOW_3 RP3 10K RP2 10K
Do not short the testlow pins together.

+3.3V_RUN
RN3 10K: CLK_PEGA_REQ# 1-2, PCIE_CLK_REQ0# 3-4, PCIE_CLK_REQ1# 5-6, PCIE_CLK_REQ2# 7-8
RP1 10K: PCIE_CLK_REQ4# 1-2, PCIE_CLK_REQ3# 3-4

+3.3V_DEEP_SUS
PCH_SMB_ALERT# R135 10K_4
RP6 2.2KX2: SMBCLK 1-2, SMBDATA 3-4
GPIO73 R462 10K_4
SML0CLK R453 2.2K_4, SML0DATA R442 2.2K_4
RP8 2.2KX2: SMB_DATA_ME1 1-2, SMB_CLK_ME1 3-4
CARDREADER_EN R443 100K_4

Haswell ULT (LPC/SPI/SMB/CLINK)

U38G HSW_ULT_DDR3L

[28,31] LPC_LAD0 AU14
[28,31] LPC_LAD1 AW12
[28,31] LPC_LAD2 AY12
[28,31] LPC_LAD3 AW11
[28,31] LPC_LFRAME# AV12
LAD0 LAD1 LAD2 LAD3 LFRAME — LPC

PCH_SPI_CLK AA3
PCH_SPI_CS0# Y7
Y4
AC2
PCH_SPI_SI AA2
PCH_SPI_SO AA4
PCH_SPI_IO2 Y6
PCH_SPI_IO3 AF1
SPI_CLK SPI_CS0 SPI_CS1 SPI_CS2 SPI_MOSI SPI_MISO SPI_IO2 SPI_IO3 — SPI

SMBUS +3V_S5
SMBALERT/GPIO11 AN2 PCH_SMB_ALERT# → T45
SMBCLK AP2
SMBDATA AH1
SML0ALERT/GPIO60 AL2 CARDREADER_EN → CARDREADER_EN [30]
SML0CLK AN1
SML0DATA AK1
+3V_S5 SML1ALERT/PCHHOT/GPIO73 AU4 GPIO73
SML1CLK/GPIO75 AU3 SMB_CLK_ME1
SML1DATA/GPIO74 AH3 SMB_DATA_ME1

C-LINK
AF2 CL_CLK
AD2 CL_DATA
AF4 CL_RST

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SMBus/Pull-up(CLG)

+3.3V_RUN
RP7 2.2KX2
Q36A 2N7002DW: SMBCLK 3 → 4 PCH_SCLK [15,32]
Q36B 2N7002DW: SMBDATA 6 → 1 PCH_SDATA [15,32]

+3.3V_DEEP_SUS
Q37A 2N7002DW: SMB_CLK_ME1 4 → 3 MBCLK_THRM [19,31]
Q37B 2N7002DW: SMB_DATA_ME1 1 → 6 MBDATA_THRM [19,31]

For EC(IT8587 e-flash) load code from BIOS flash ROM

EC-A17
R69 *10K_4
R65 *10K_4

[31] 8512_SI
[31] 8512_SO
[31] 8512_SCK
[31] 8512_SCE#
8512_SI R62 0_4 PCH_SPI_SI_R
8512_SO R57 0_4 PCH_SPI_SO_R
8512_SCK R59 0_4 PCH_SPI_CLK_R
8512_SCE# R61 0_4 PCH_SPI_CS0#_R

+3.3V_DEEP_SUS +3.3V_RUN
FC1 *68P/50V/NPO_4 PCH_SPI_VCC
R17 0_4, R26 *0_4
R30 10K_4
FC2 *22P/50V/NPO_4
FC3 *22P/50V/NPO_4
EC-A17
PCH_SPI_CS0# R60 15_4 PCH_SPI_CS0#_R
PCH_SPI_CLK R58 15_4 PCH_SPI_CLK_R
PCH_SPI_SI R51 15_4 PCH_SPI_SI_R
PCH_SPI_SO R56 15_4 PCH_SPI_SO_R
PCH_SPI_IO2 R29 15_4
U3 W25Q64FVSSIQ: 1 CE#, 2 SO, 3 WP#, 4 VSS, 5 SI, 6 SCK, 7 HOLD#, 8 VDD
R41 10K_4
R40 15_4 PCH_SPI_IO3
C37 0.1U/10V/X5R_4

SPI FLASH

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Quanta Computer Inc.

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Haswell ULT (SYSTEM POWER MANAGEMENT)

8

[4,6,12,17,23,25,28,30,32,38,43,46] +3.3V_DSW
[2,4,6,7,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[4,5,6,7,12,15] +3.3V_DEEP_SUS

U38H HSW_ULT_DDR3L
SYSTEM POWER MANAGEMENT
8 OF 19

[31] SUSACK# R120 0_4 SUSACK# AK2 SUSACK
SYS_RESET# AC3 SYS_RESET
SYS_PWROK AG2 SYS_PWROK
PCH_PWROK AY7 PCH_PWROK
PCH_APWROK AB5 APWROK
PLTRST# AG7 PLTRST
EC-A18
[23,31] EC_PWROK R509 0_4 R530 *0_4
[31] EC_APWROK R532 0_4

[31] RSMRST# RSMRST# AW6 RSMRST
[31] SUSWARN# SUSWARN# AV4 SUSWARN/SUSPWRDNACK/GPIO30
[31] SIO_PWRBTN# SIO_PWRBTN# AL7 PWRBTN
[19,31] AC_PRESENT AC_PRESENT AJ8 ACPRESENT/GPIO31
PM_BATLOW# AN4 BATLOW/GPIO72
AF3 SLP_S0
[31] SLP_S0# AM5 SLP_WLAN/GPIO29
T47

+3V
+3V_S5
+3V_S5
DSW
+3V_S5
DSW
DSW
DSW

DSWVRMEN [6]
AW7 DSWVRMEN
AV5 DPWROK DPWROK_R R512 0_4 R510 *0_4 RSMRST#
AJ5 WAKE PCIE_WAKE#_R R134 0_4
EC-A05
DPWROK [31]
PCIE_WAKE# [25,28]

V5 CLKRUN/GPIO32 CLKRUN#
AG4 SUS_STAT/GPIO61
AE6 SUSCLK
AP5 SUSCLK/GPIO62
SLP_S5/GPIO63
CLKRUN# [31]
SUS_STAT# [31]
SUSCLK
SIO_SLP_S5# [31]

AJ6 SLP_S4
AT4 SLP_S3
AL5 SLP_A SIO_SLP_A#
AP4 SLP_SUS
AJ7 SLP_LAN
SLP_S4# [31]
SIO_SLP_S3# [31]
T50
SLP_SUS# [31]
SIO_SLP_LAN# [25,44]

PCH Pull-high/low(CLG)

+3.3V_DEEP_SUS
SIO_PWRBTN# R130 *10K_4
SUSWARN# R152 10K_4
SUSCLK R118 10K_4

+3.3V_DSW
AC_PRESENT R154 10K_4
PM_BATLOW# R173 10K_4
PCIE_WAKE#_R R137 1K_4
EC-A31

+3.3V_RUN
CLKRUN# R94 10K_4
SYS_RESET# R101 10K_4
RSMRST# R511 10K_4
SYS_PWROK R529 10K_4
DPWROK_R R513 100K_4

SYS_PWROK
RSMRST#
PLTRST#
EC_PWROK
AVLC 5S 02 100 SC13
AVLC 5S 02 100 SC1
AVLC 5S 02 100 SC12
AVLC 5S 02 100 SC14
ESD

+3.3V_DEEP_SUS
R210 *10K_4
Q19 2N7002
PM_BATLOW#
PM_BATLOW_N [31]

+3.3V_DEEP_SUS
C479 *0.1U/10V/X7R_4
U33 *TC7SH08FU
[27,28] BUF_PLT_RST#
PLTRST#
PLTRST# [16,25,30]
RV2 *AVLC 5S 02 (5.5V,100p)_4
R397 100K_4
R395 0_4

For DS3

+3.3V_DSW
+3.3V_DEEP_SUS
R151 *0_6
R148 *100K_4
C175 1U/6.3V_4
U11
IN IN ON/OFF OUT GND
IC(5P) G5243AT11U
[31] SLP_SUS_ON_GPG2
C182 *10P/50V_4
R160 *100K_4
C184 0.1U/10V_4

System PWR_OK(CLG)

EC-A19

+3.3V_DEEP_SUS
+3.3V_RUN
R599 *10K_4
R600 *10K_4
Q50 *2N7002
[9,42] IMVP_PWRGD
R602 *4.7K_4
Q43 *MMBT3904-7-F

+3.3V_DEEP_SUS
C566 *0.1U/10V/X7R_4
U46 *TC7SH08FU
IMVP_PWRGD_3V
[31] SYS_PWROK_EC
SYS_PWROK
*AVLC 5S 02
SC33
R601 0_4

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Haswell ULT MCP(POWER)

CPU VDDQ

Haswell ULT 15W : 4.2A

6X10UF MLCC
4X2.2UF MLCC

+V_VDDQ_VR

C123 10U/6.3V/X5R_6
C122 10U/6.3V/X5R_6
C121 10U/6.3V/X5R_6
C120 10U/6.3V/X5R_6
C514 10U/6.3V/X5R_6
C516 10U/6.3V/X5R_6
C515 10U/6.3V/X5R_6

C512 2.2U/6.3V/X5R_4
C513 2.2U/6.3V/X5R_4
C510 2.2U/6.3V/X5R_4
C511 2.2U/6.3V/X5R_4

+V1.05S_VCCST

R371 10K_4

VCCST_PWRGD_L

[31] VCCST_PWRGD#

Q34 2N7002

EC-A20

C453 *0.1U/10V/X5R_4

[42] H_VR_ENABLE_MCP

R43 10K_4

[8,42] IMVP_PWRGD

+V1.05S_VCCST

R39 150_6

T5

+V_VDDQ_VR

+VCCIN

+VCCIOA_OUT

+VCCIO_OUT

U38L

HSW_ULT_DDR3L

T17	MCP_RSVD_61	L59	RSVD
T8	MCP_RSVD_62	J58	RSVD
		AH26	VDDQ
		AJ31	VDDQ
		AJ33	VDDQ
		AJ37	VDDQ
		AN33	VDDQ
		AP43	VDDQ
		AR48	VDDQ
		AY35	VDDQ
		AY40	VDDQ
		AY44	VDDQ
		AY50	VDDQ
		F59	VCC
T19	MCP_RSVD_63	N58	RSVD
T33	MCP_RSVD_64	AC58	RSVD
	VCCSENSE	E63	VCC_SENSE
T40	MCP_RSVD_65	AB23	RSVD
		A59	VCCIO_OUT
		E20	VCCIOA_OUT
T37	MCP_RSVD_66	AD23	RSVD
T36	MCP_RSVD_67	AA23	RSVD
T39	MCP_RSVD_68	AE59	RSVD
	H_CPU_SVIDALRT_N	L62	VIDALERT
	VR_SVID_CLK	N63	VIDSCLK
	VR_SVID_DATA	L63	VIDSOUT
		B59	VCCST_PWRGD
		F60	VR_EN
		C59	VR_READY
		D63	VSS
	FIVR_EN_BUF	H59	PWR_DEBUG
		P62	VSS
T79	MCP_RSVD_69	P60	RSVD_TP
T23	MCP_RSVD_70	P61	RSVD_TP
T20	MCP_RSVD_71	N59	RSVD_TP
T22	MCP_RSVD_72	N61	RSVD_TP
T24	MCP_RSVD_73	T59	RSVD
T35	MCP_RSVD_74	AD60	RSVD
T38	MCP_RSVD_75	AD59	RSVD
T31	MCP_RSVD_76	AA59	RSVD
T98	MCP_RSVD_77	AE60	RSVD
T32	MCP_RSVD_78	AC59	RSVD
T41	MCP_RSVD_79	AG58	RSVD
T26	MCP_RSVD_80	U59	RSVD
T29	MCP_RSVD_81	V59	RSVD
		AC22	VCCST
		AE22	VCCST
		AE23	VCCST
		AB57	VCC
		AD57	VCC
		AG57	VCC
		C24	VCC
		C28	VCC
		C32	VCC

HSW ULT POWER

12 OF 19

+V1.05S_VCCST

+1.05V_RUN

R16 0_12

+V1.05S_VCCST

+VCCIN

+VCCIN

R390 100/F_4

[42] VCCSENSE

VCCSENSE

CPU VCC

Haswell ULT 15W : 32A

23 X 22UF

+VCCIN

		C36	VCC
C118	22U/6.3V/X5R_6	C40	VCC
C133	22U/6.3V/X5R_6	C44	VCC
C111	22U/6.3V/X5R_6	C48	VCC
C108	22U/6.3V/X5R_6	C52	VCC
C96	22U/6.3V/X5R_6	C56	VCC
C88	22U/6.3V/X5R_6	E23	VCC
C63	22U/6.3V/X5R_6	E25	VCC
C79	22U/6.3V/X5R_6	E27	VCC
C64	22U/6.3V/X5R_6	E29	VCC
C70	22U/6.3V/X5R_6	E31	VCC
C68	22U/6.3V/X5R_6	E33	VCC
C67	22U/6.3V/X5R_6	E35	VCC
C66	22U/6.3V/X5R_6	E37	VCC
C65	22U/6.3V/X5R_6	E39	VCC
C73	22U/6.3V/X5R_6	E41	VCC
C74	22U/6.3V/X5R_6	E43	VCC
C75	22U/6.3V/X5R_6	E45	VCC
C69	22U/6.3V/X5R_6	E47	VCC
C128	22U/6.3V/X5R_6	E49	VCC
C126	22U/6.3V/X5R_6	E51	VCC
C61	22U/6.3V/X5R_6	E53	VCC
C78	22U/6.3V/X5R_6	E55	VCC
C77	22U/6.3V/X5R_6	E57	VCC
C60	22U/6.3V/X5R_6	F24	VCC
C140	22U/6.3V/X5R_6	F28	VCC
C76	22U/6.3V/X5R_6	F32	VCC
C72	22U/6.3V/X5R_6	F36	VCC
C71	22U/6.3V/X5R_6	F40	VCC
C129	22U/6.3V/X5R_6	F44	VCC
C95	22U/6.3V/X5R_6	F48	VCC
		F52	VCC
		F56	VCC
		G23	VCC
		G25	VCC
		G27	VCC
C97	100P/50VNPO_4	G29	VCC
C107	100P/50VNPO_4	G31	VCC
C90	100P/50VNPO_4	G33	VCC
C109	100P/50VNPO_4	G35	VCC
		G37	VCC
		G39	VCC
		G41	VCC
		G43	VCC
		G45	VCC
		G47	VCC
		G49	VCC
		G51	VCC
		G53	VCC
		G55	VCC
		G57	VCC
		H23	VCC
		J23	VCC
		K23	VCC
		K57	VCC
		L22	VCC
		M23	VCC
		M57	VCC
		P57	VCC
		U57	VCC
		W57	VCC

SVID ALERT

close to CPU

+V1.05S_VCCST +VCCIO_OUT

R409 75_4

R405 *75_4

H_CPU_SVIDALRT_N

R414 43_4

VR_SVID_ALERT# [42]

SVID DATA

close to CPU

+V1.05S_VCCST +VCCIO_OUT

R408 130_4

R402 *130_4

VR_SVID_DATA

close to VR

+V1.05S_VCCST +VCCIO_OUT

R422 130_4

R430 *130_4

EC-A04

VR_SVID_DATA [42]

SVID CLK

EC-A04

close to VR

+V1.05S_VCCST +VCCIO_OUT

R435 54.9_4

R434 *54.9_4

VR_SVID_CLK

VR_SVID_CLK [42]

C567 0.1U/10V_4

+V1.05S_VCCST

[42] +VCCIN
[4,13] +V1.05S_VCCST
[14,15,39,44] +V_VDDQ_VR
[13] +VCCIO_OUT
[6,12,35,40,44,46] +1.05V_RUN
[2] +VCCIOA_OUT

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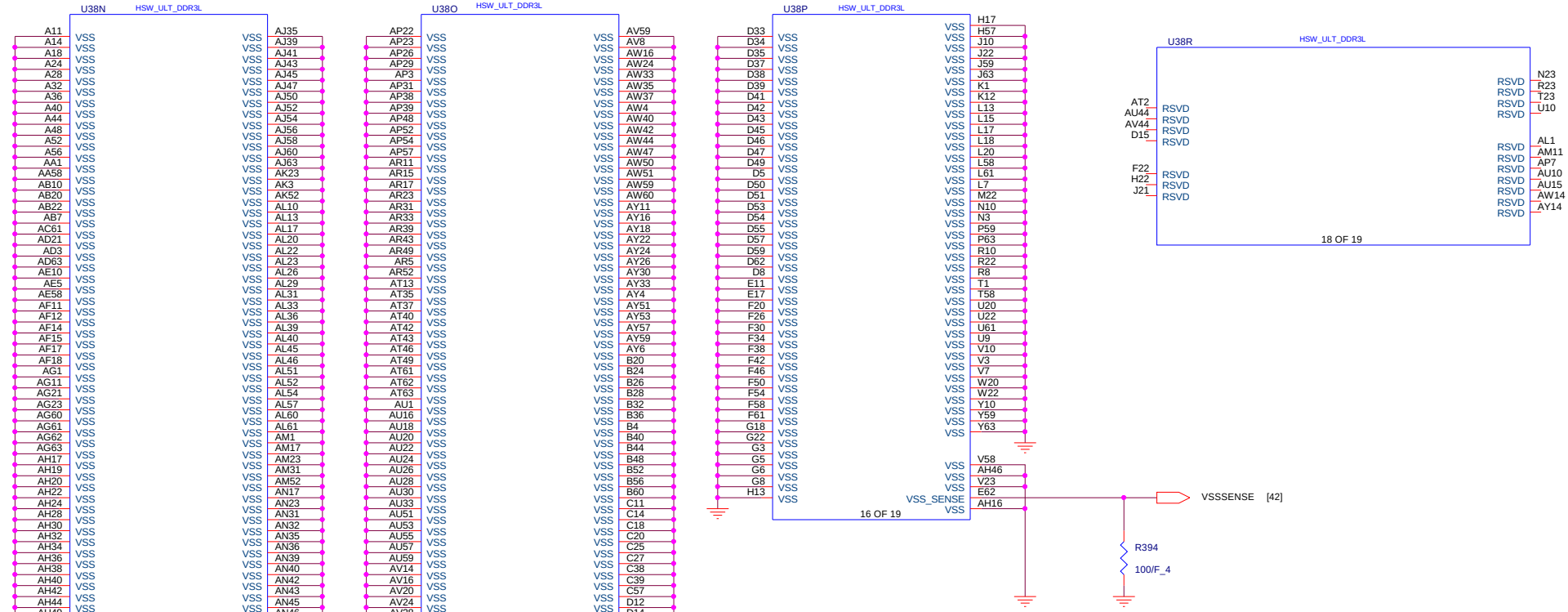
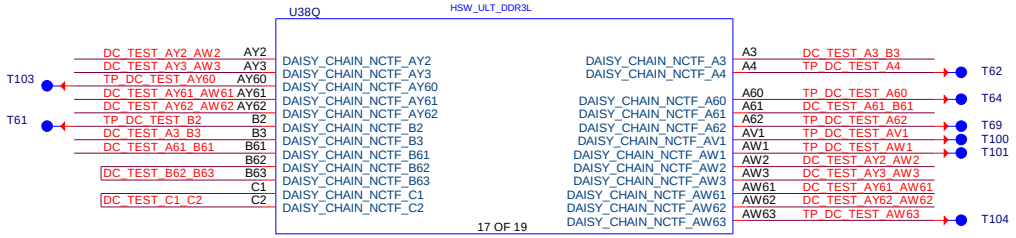
Haswell ULT (GND)





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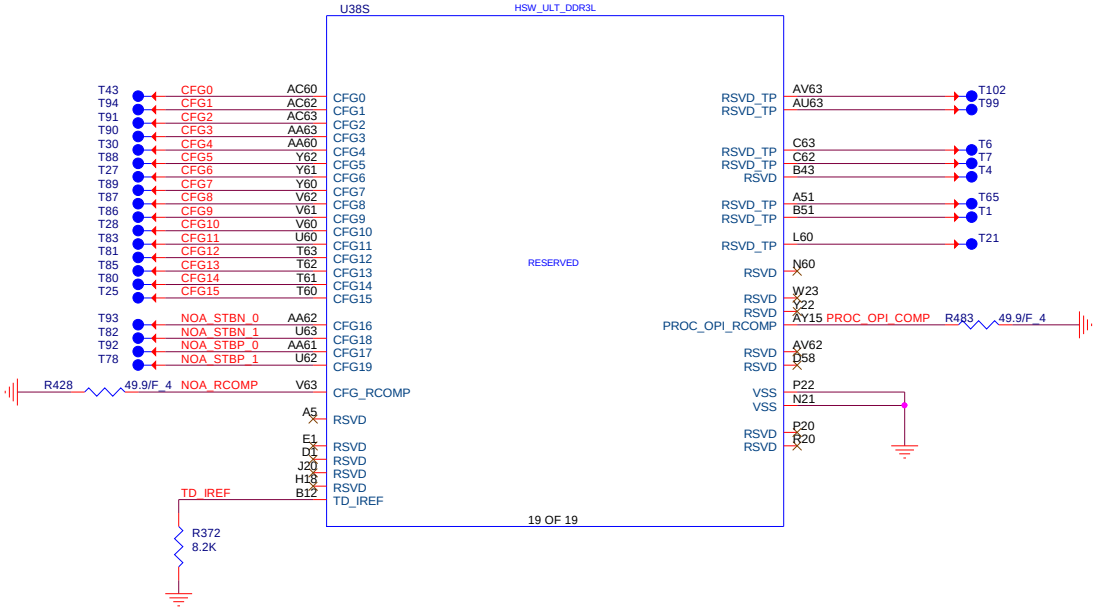
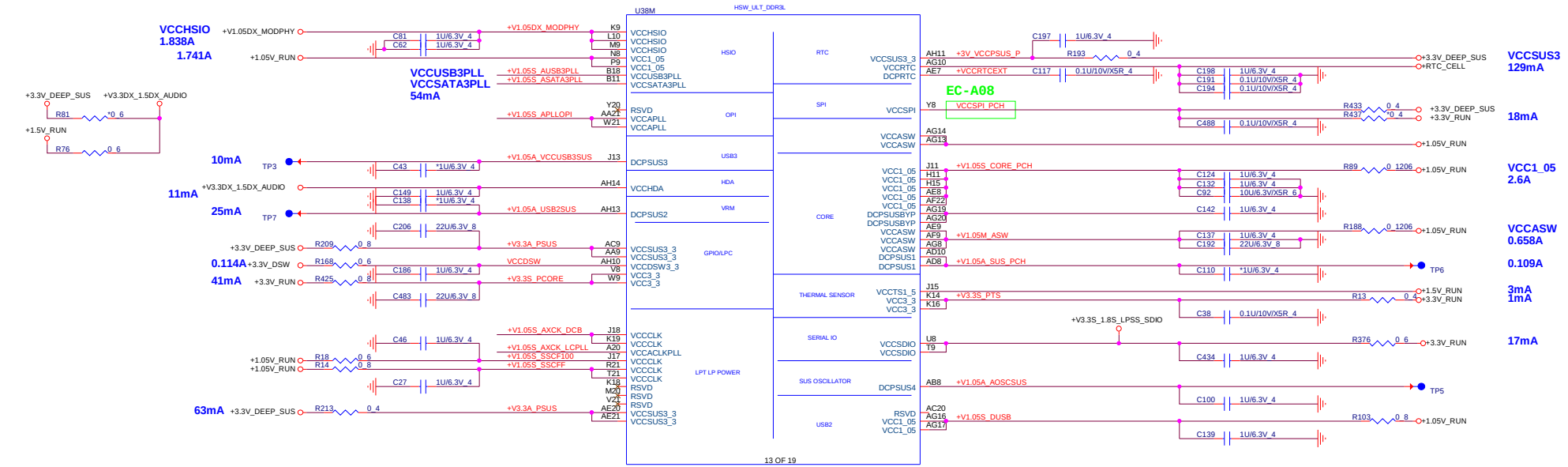


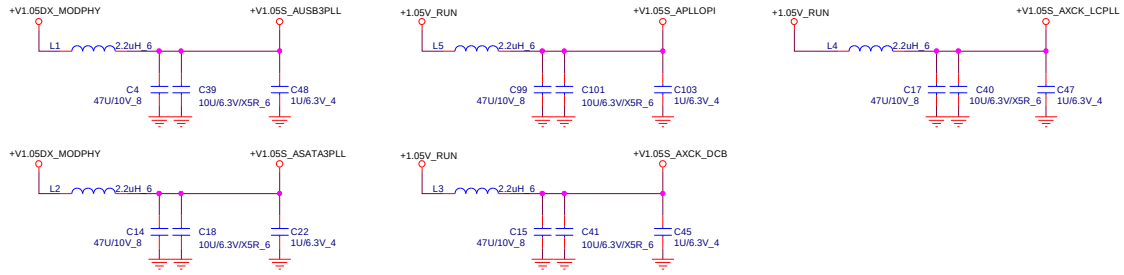
Processor Strapping

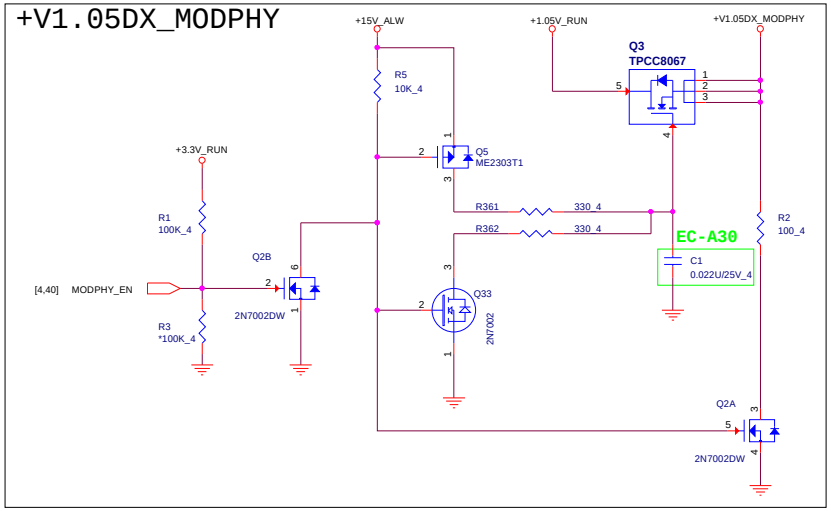
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R121 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R441 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R438 *1K_4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R102 1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R432 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R429 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R98 *1K_4

[4,5,6,7,8,15] +3.3V_DEEP_SUS
[6,9,35,40,44,46] +1.05V_RUN
[23,28,41,44,46] +1.5V_RUN
[2,4,6,7,8,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[4,6,8,17,23,25,28,30,32,38,43,46] +3.3V_DSW
[15,17,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW
[38,43,46] +15V_ALW
[7] +V1.05S_AXCK_LCPLL
[5] +V1.05S_AUSB3PLL
[6] +V1.05S_ASATA3PLL

Haswell ULT PCH(POWER)







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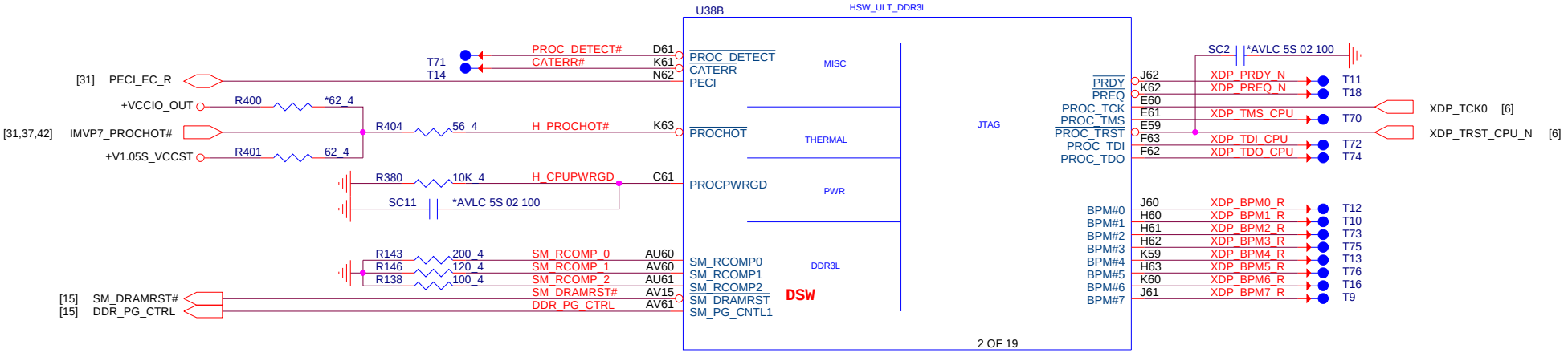
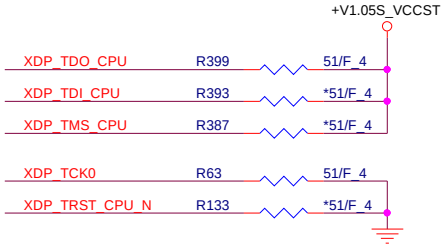
[4,9] +V1.05S_VCCST
[9] +VCCIO_OUT

13





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CHANNEL A: 4GB DDR3L

[3] M_A_DQSP[7:0]
[3] M_A_DQSN[7:0]
[3] M_A_DQ[63:0]

[15,39,44] +0.675V_DDR_VTT
[9,15,39,44] +V_VDDQ_VR
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[15,17,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW
[15] +SMDDR_VREF_CA

BYTE7_56-63 BYTE4_32-39

U14 — RAM_DDR3 — 100-BALL SDRAM DDR3

+SMDDR_VREF_CA
+SMDDR_VREF_DQ0
[3] M_A_A[15..0]

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

[3] M_A_BS#0
[3] M_A_BS#1
[3] M_A_BS#2
[3] M_A_CLKP0
[3] M_A_CLKN0
[3] M_A_CKE0
[3] M_A_CS#0
[3] M_A_RAS#
[3] M_A_CAS#
[3] M_A_WE#
[3] M_A_CS#1
[3] M_A_CKE1
[15] DDR3_DRAMRST#

+V_VDDQ_VR

Should be 240 Ohms +-1%

R170 240/F_4
R169 240/F_4

BYTE3_24-31 BYTE1_8-15

U44 — RAM_DDR3 — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R554 240/F_4
R558 240/F_4

BYTE2_16-23 BYTE0_0-7

U21 — RAM_DDR3 — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R235 240/F_4
R234 240/F_4

BYTE6_48-55 BYTE5_40-47

U41 — RAM_DDR3 — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R543 240/F_4
R544 240/F_4

+0.675V_DDR_VTT

R548 34.8/F_4 M_A_BS#0
R254 34.8/F_4 M_A_BS#1
R535 34.8/F_4 M_A_BS#2
R551 34.8/F_4 M_A_CS#0
R534 34.8/F_4 M_A_CKE0
R550 34.8/F_4 M_A_CAS#
R552 34.8/F_4 M_A_RAS#
R249 34.8/F_4 M_A_WE#
R240 34.8/F_4 M_A_A0
R242 34.8/F_4 M_A_A1
R538 34.8/F_4 M_A_A2
R546 34.8/F_4 M_A_A3
R541 34.8/F_4 M_A_A4
R236 34.8/F_4 M_A_A5
R232 34.8/F_4 M_A_A6
R222 34.8/F_4 M_A_A7
R226 34.8/F_4 M_A_A8
R220 34.8/F_4 M_A_A9
R549 34.8/F_4 M_A_A10
R216 34.8/F_4 M_A_A11
R536 34.8/F_4 M_A_A12
R262 34.8/F_4 M_A_A13
R218 34.8/F_4 M_A_A14
R547 34.8/F_4 M_A_A15
R260 34.8/F_4 M_A_CS#1
R533 34.8/F_4 M_A_CKE1

+0.675V_DDR_VTT
R174 26.1/F_4 M_A_CLKP0
R166 26.1/F_4 M_A_CLKN0

+V_VDDQ_VR
[3] SM_VREF_DQ0
R167 0_6
R150 1.8K/F_4
R295 30/F_4 M_A_ODT0
R175 5.11/F_4 +SMDDR_VREF_DQ0
C183 0.022U/16V_4
R545 1.8K/F_4
R158 24.9/F_4

Place near MD device

+SMDDR_VREF_CA
C202 0.047U/10V_4
C239 0.047U/10V_4
C527 0.047U/10V_4
C291 0.047U/10V_4

+SMDDR_VREF_DQ0
C301 0.047U/10V_4
C309 0.047U/10V_4
C180 0.047U/10V_4
C242 0.047U/10V_4

B.1119

+0.675V_DDR_VTT
C251 1U/6.3V_4
C246 1U/6.3V_4
C257 1U/6.3V_4
C243 1U/6.3V_4
C236 10U/6.3V_6

Place these Caps near Memory Down

ONLY 3 NEED TO BE STUFFED FOR ONE DEVICE

+V_VDDQ_VR
C231 1u/6.3V_4
C188 1u/6.3V_4
C531 1u/6.3V_4
C507 1u/6.3V_4
C187 1u/6.3V_4
C504 1u/6.3V_4

+V_VDDQ_VR
C241 1u/6.3V_4
C277 1u/6.3V_4
C529 1u/6.3V_4
C240 1u/6.3V_4
C244 1u/6.3V_4
C207 1u/6.3V_4

+V_VDDQ_VR
C214 10u/6.3V_6
C201 10u/6.3V_6
C272 10u/6.3V_6
C225 10u/6.3V_6
C250 *10u/6.3V_6
C538 *10u/6.3V_6
C553 *150u/6.3V_3528

+V_VDDQ_VR
C259 *1u/6.3V_4
C535 *1u/6.3V_4
C508 *1u/6.3V_4
C528 *1u/6.3V_4
C541 *1u/6.3V_4
C233 *1u/6.3V_4

+V_VDDQ_VR
C534 *1u/6.3V_4
C542 *1u/6.3V_4
C509 *1u/6.3V_4
C505 *1u/6.3V_4
C506 *1u/6.3V_4
C537 *1u/6.3V_4

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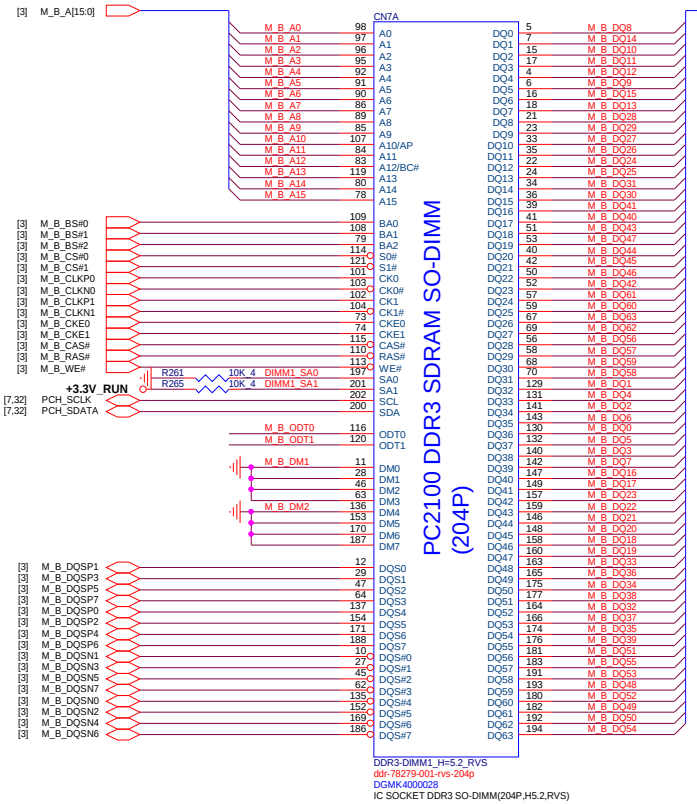
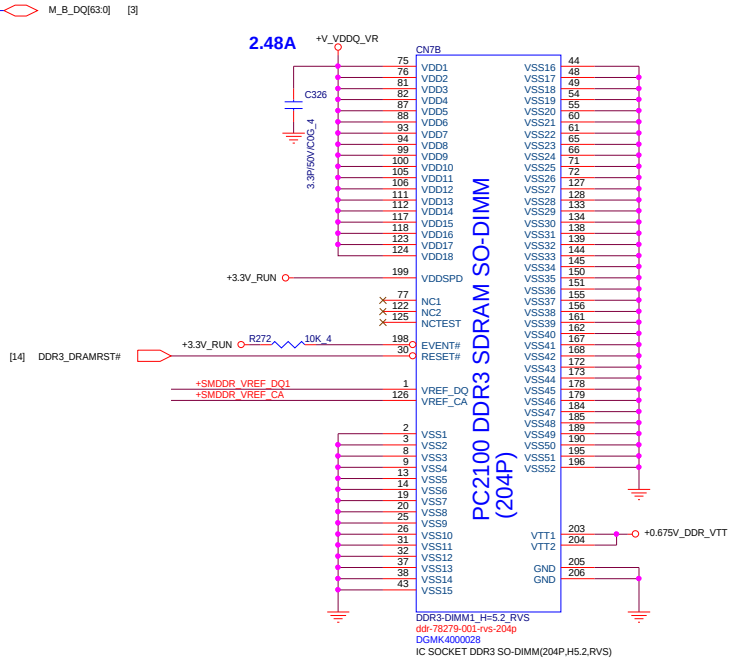
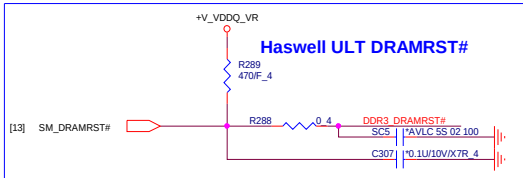
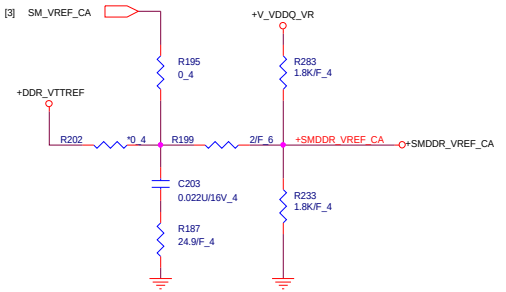
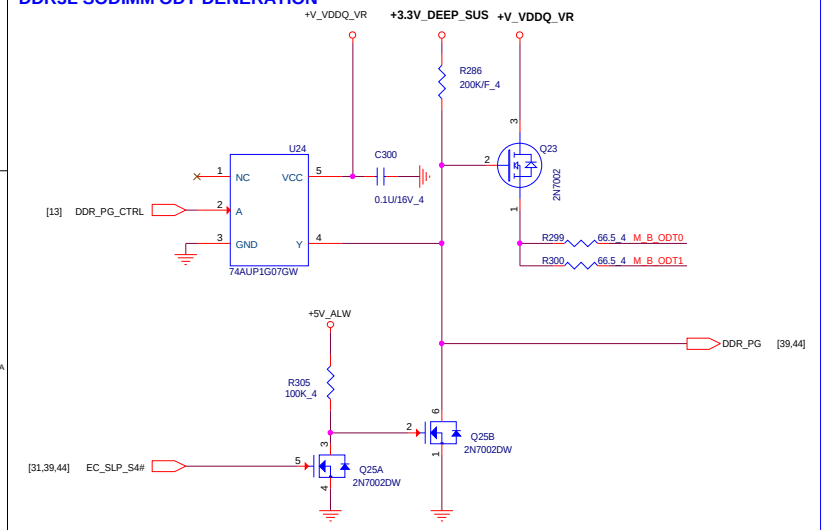
[14,39,44] +0.675V_DDR_VTT
[9,14,39,44] +V_VDDQ_VR
[2,4,6,7,8,12,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[17,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW
[14] +SMDDR_VREF_CA
[4,5,6,7,8,12] +3.3V_DEEP_SUS

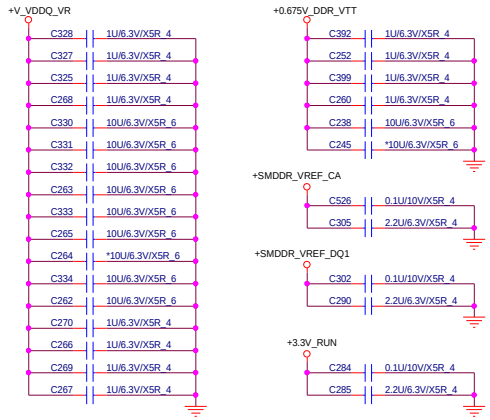


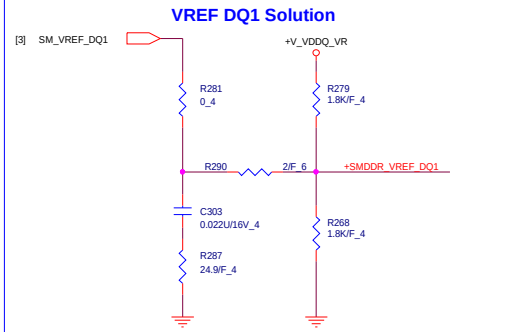












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Quanta Computer Inc.

Size	Document Number	Rev
	Custom DDR3 DIMM0-STD (5.2H)	3A
Date: Thursday, January 03, 2013	Sheet 15 of 47	

[17,19,35,45,46,47] 3V_GPU
[17,18,46,47] 1.05V_GFX_PCIE
[45,47] VGPU_CORE
[2,4,6,7,8,12,15,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.V_RUN

<VGA>

3300mA

1.05V_GFX_PCIE
Under GPU: C87 DIS@1U/6.3V/X5R_4, C85 DIS@1U/6.3V/X5R_4
Near GPU: C84 DIS@4.7U/6.3V/X5R_6
Midway between GPU and power supply: C456 DIS@4.7U/6.3V/X5R_6, C435 DIS@4.7U/6.3V/X5R_6, C419 DIS@22U/6.3V/X5R_8, C430 DIS@22U/6.3V/X5R_8
AA22 AB23 AC24 AD25 AE26 AE27 PEX_IOVDD

1.05V_GFX_PCIE
Under GPU: C91 DIS@1U/6.3V/X5R_4, C86 DIS@1U/6.3V/X5R_4
Near GPU: C470 DIS@4.7U/6.3V/X5R_6
Midway between GPU and power supply: C457 DIS@4.7U/6.3V/X5R_6, C458 DIS@4.7U/6.3V/X5R_6, C454 DIS@22U/6.3V/X5R_8, C420 DIS@22U/6.3V/X5R_8
AA10 AA12 AA13 AA16 AA18 AA19 AA20 AA21 AB22 AC23 AD24 AE25 AF26 AF27 PEX_IOVDDQ

210mA

3V_GPU
Near GPU: C151 DIS@4.7U/6.3V/X5R_6, C152 DIS@4.7U/6.3V/X5R_6, C83 DIS@0.1U/10V/X7R_4
AA8 AA9 PEX_PLL_HVDD
AB8 PEX_SVDD_3V3

[45] GPUCORE_VCCSENSE F2 VDD_SENSE
[45] GPUCORE_VSSSENSE F1 GND_SENSE

12~16 mils

R389 *DIS@200/F_4
AF22 AE22 PEX_TSTCLK_OUT

Under GPU: C89 DIS@0.1U/10V/X7R_4
Near GPU: C471 DIS@0.1U/10V/X7R_6, C421 DIS@4.7U/6.3V/X5R_6
AA14 AA15 PEX_PLLVDD

1.05V_GFX_PCIE
EC-A01
150mA

AD9 TESTMODE
R386 DIS@10K/F_4
AF25 PEX_TERMP
R385 DIS@2.49K/F_4

U39A
bga595-nvidia-n13m-gs-s-a2
COMMON
1/14 PCI_EXPRESS
GK208/GF117/GF119
NC

AB6	PEX_WAKE#	R24	*DIS@10K_4	3V_GPU	
AC7	VGA_RST#	C59	*DIS@0.1U/10V/X7R_4		
		R52	0_4	VGA_PLTRST#	
AC6	PEX_CLKREQ#			R21	DIS@10K_4
AE8				CLK_PCIE_VGAP	[7]
AD8				CLK_PCIE_VGAN	[7]

AC9	PEG_RXP0_C	C29	0.1U/10V/X5R_4	PEG_RXP0	[5]
AB9	PEG_RXN0_C	C30	0.1U/10V/X5R_4	PEG_RXN0	[5]
AG6	PEG_TXP0			PEG_TXP0	[5]
AG7	PEG_TXN0			PEG_TXN0	[5]
AB10	PEG_RXP1_C	C32	0.1U/10V/X5R_4	PEG_RXP1	[5]
AC10	PEG_RXN1_C	C31	0.1U/10V/X5R_4	PEG_RXN1	[5]
AF7	PEG_TXP1			PEG_TXP1	[5]
AE7	PEG_TXN1			PEG_TXN1	[5]
AD11	PEG_RXP2_C	C33	0.1U/10V/X5R_4	PEG_RXP2	[5]
AC11	PEG_RXN2_C	C34	0.1U/10V/X5R_4	PEG_RXN2	[5]
AE9	PEG_TXP2			PEG_TXP2	[5]
AF9	PEG_TXN2			PEG_TXN2	[5]
AC12	PEG_RXP3_C	C36	0.1U/10V/X5R_4	PEG_RXP3	[5]
AB12	PEG_RXN3_C	C35	0.1U/10V/X5R_4	PEG_RXN3	[5]
AG9	PEG_TXP3			PEG_TXP3	[5]
AG10	PEG_TXN3			PEG_TXN3	[5]

AB13 AC13 AF10 AE10 AD14 AC14 AE12 AF12 AC15 AB15 AG12 AG13 AB16 AC16 AF13 AE13 AD17 AC17 AE15 AF15 AC18 AB18 AG15 AG16 AB19 AC19 AF16 AE16 AD20 AC20 AE18 AF18 AC21 AB21 AG18 AG19 AD23 AE23 AF19 AE19 AF24 AE24 AE21 AF21 AG24 AG25 AG21 AG22

NC GF117 GK208 GF119
U_GPU_GB2_64

PEG CLK detect

GFXON [17,31,45,46]
CLK_PEGA_REQ# [7]
Q6 DIS@2N7002

GPU RST#(CLG)

3V_GPU
C57 DIS@0.1U/10V/X7R_4
U5 DIS@TC7SH08FU(F)
VGA_PLTRST# 4
DGPU_HOLD_RST# [4]
PLTRST# [8,25,30]
R49 DIS@100K/F_4

+3.3V_RUN
3V_GPU
R208 DIS@10K/F_4
R182 DIS@10K/F_4
GFXPG [4,19]
1.05V_GFX_PCIE
C213 2200P/50V/X7R_4
Q16 DIS@SST3904T116
R196 DIS@10K/F_4
Q14 DIS@MMBT3904-7-F
DIS@0.1U/10V/X7R_4 C210
1.5V_GPU
EC-A48
R206 DIS@10K/F_4
Q15 DIS@MMBT3904-7-F
*DIS@1000P/50V/X7R_4@NC C204

U39C
bga595-nvidia-n13m-gs-s-a2
COMMON
14/14 XVDD/VDD33
AD10 AD7 B19 NC
F11 3V3AUX_NC
V5 V6 FERMI_RSVD1_NC FERMI_RSVD2_NC
CONFIGURABLE POWER CHANNELS
* nc on substrate
G1 G2 G3 G4 G5 G6 G7 XPWR_G1..G7
V1 V2 XPWR_V1 V2
W1 W2 W3 W4 XPWR_W1..W4
VDD33 G10 G12 G8 G9
3V_GPU
Near GPU: C94 DIS@4.7U/6.3V/X5R_6, C166 DIS@1U/10V/X7R_6
Under GPU: C80 DIS@0.1U/10V/X7R_4, C159 DIS@0.1U/10V/X7R_4, C157 DIS@0.1U/10V/X7R_4, C158 DIS@0.1U/10V/X7R_4
U_GPU_GB2_64

Peak current:45A
Boosted:28A

U39E
bga595-nvidia-n13m-gs-s-a2
COMMON
11/14 NVDD
VGPU_CORE
PLACE UNDER BALLS
Under GPU: C104 DIS@4.7U/6.3V/X5R_6, C144 DIS@4.7U/6.3V/X5R_6, C130 DIS@4.7U/6.3V/X5R_6, C131 DIS@4.7U/6.3V/X5R_6, C115 DIS@4.7U/6.3V/X5R_6, C106 DIS@4.7U/6.3V/X5R_6, C146 DIS@4.7U/6.3V/X5R_6, C150 DIS@4.7U/6.3V/X5R_6, C114 DIS@4.7U/6.3V/X5R_6, C127 DIS@4.7U/6.3V/X5R_6, C125 DIS@0.1U/10V/X7R_4, C141 DIS@0.1U/10V/X7R_4, C102 DIS@0.1U/10V/X7R_4, C112 DIS@0.1U/10V/X7R_4
Near GPU: C493 DIS@47U/6.3V/X5R_8, C492 DIS@22U/6.3V/X5R_8, C486 DIS@4.7U/6.3V/X5R_6, C490 DIS@4.7U/6.3V/X5R_6, C148 DIS@4.7U/6.3V/X5R_6, C491 DIS@4.7U/6.3V/X5R_6, C147 DIS@4.7U/6.3V/X5R_6, C485 *220U/2.5V_3216
VDD K10 K12 K14 K16 K18 L11 L13 L15 L17 M10 M12 M14 M16 M18 N11 N13 N15 N17 P10 P12 P14 P16 P18 R11 R13 R15 R17 T10 T12 T14 T16 T18 U11 U13 U15 U17 V10 V12 V14 V16 V18
U_GPU_GB2_64

Table 2. GPU Power Rails

GPU Power Rail	Nominal Value	Comments
NVVDD	GPU SKU Specific	GPU Core power rail
FBVDD[2]	1.35 V or 1.5 V	VRAM Core power for Frame Buffer components
FBVDDQ[2]	1.35 V or 1.5 V	VRAM I/O and GPUs Frame Buffer I/O power rail
IFPx_IOVDD[3]	1.05 V or 3.3V	Powers IFP blocks
IFPx_PLLVDD[3]	1.05 V or 3.3 V	Integrated Digital Display PLL Power Rails
PEX_IOVDD/Q	1.05 V	GPUs PCIE interface power rail
PEX_SVDD_3V3, PEX_PLL_HVDD	3.3 V	GPU PCIE PLL Power Rails
PEX_PLLVDD	1.05 V	GPU PCIE PLL Power Rails
FBx_PLL_AVDD	1.05 V or 3.3 V	Frame Buffer PLL Power Rail
FBx_DLL_AVDD (GB2-192 and GB4-128)	1.05 V	Frame Buffer PLL and DLL Power Rail
FBx_PLL_DLL_AVDD (GB2-192 and GB3-256)	1.05 V	Frame Buffer PLL and DLL Power Rail
PLLVDD, GPCPLL_AVDD LXS_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
VID_PLLVDD	1.05 V	Video Pixel Clock PLL Analog Power Rail
SP_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
DACx_VDD[1]	3.3 V	Powers the DAC interfaces
VDD33(NV3V3)[4]	3.3 V	Powers slower logic such as GPIOs, I2C, AUX channels and SLI

Notes:
1. The same power plane can be used for VDD33 and DACx_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays)
4. On GB3-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

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Quanta Computer Inc.

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	N14M-GS (PCIE I/F) 1/5	1A
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<VGA>

[20] VMA_DQ[63..0] → VMA_DQ[63..0]
[20] VMA_DM[7..0] → VMA_DM[7..0]
[20] VMA_WDQS[7..0] → VMA_WDQS[7..0]
[20] VMA_RDQS[7..0] → VMA_RDQS[7..0]

[16,18,46,47] 1.05V_GFX_PCIE
[16,20,46,47] 1.5V_GPU
[16,19,35,45,46,47] 3V_GPU
[15,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW

U39B
bga595-nvidia-n13m-gs-s-a2
COMMON
2/14 FBA

R144 0_4 FB_CLAMP → F3
R147 DIS@10K/F_4

FB_CLAMP	NC
GF117/GK208	GF119

FBA_D0	E18	VMA_DQ0
FBA_D1	F18	VMA_DQ1
FBA_D2	E16	VMA_DQ2
FBA_D3	F17	VMA_DQ3
FBA_D4	D20	VMA_DQ4
FBA_D5	D21	VMA_DQ5
FBA_D6	F20	VMA_DQ6
FBA_D7	E21	VMA_DQ7
FBA_D8	E15	VMA_DQ8
FBA_D9	D15	VMA_DQ9
FBA_D10	F15	VMA_DQ10
FBA_D11	F13	VMA_DQ11
FBA_D12	C13	VMA_DQ12
FBA_D13	B13	VMA_DQ13
FBA_D14	E13	VMA_DQ14
FBA_D15	D13	VMA_DQ15
FBA_D16	B15	VMA_DQ16
FBA_D17	C16	VMA_DQ17
FBA_D18	A13	VMA_DQ18
FBA_D19	A15	VMA_DQ19
FBA_D20	B18	VMA_DQ20
FBA_D21	A18	VMA_DQ21
FBA_D22	A19	VMA_DQ22
FBA_D23	C19	VMA_DQ23
FBA_D24	B24	VMA_DQ24
FBA_D25	C23	VMA_DQ25
FBA_D26	A25	VMA_DQ26
FBA_D27	A24	VMA_DQ27
FBA_D28	A21	VMA_DQ28
FBA_D29	B21	VMA_DQ29
FBA_D30	C20	VMA_DQ30
FBA_D31	C21	VMA_DQ31
FBA_D32	R22	VMA_DQ32
FBA_D33	R24	VMA_DQ33
FBA_D34	T22	VMA_DQ34
FBA_D35	R23	VMA_DQ35
FBA_D36	N25	VMA_DQ36
FBA_D37	N26	VMA_DQ37
FBA_D38	N23	VMA_DQ38
FBA_D39	N24	VMA_DQ39
FBA_D40	V23	VMA_DQ40
FBA_D41	V22	VMA_DQ41
FBA_D42	T23	VMA_DQ42
FBA_D43	U22	VMA_DQ43
FBA_D44	Y24	VMA_DQ44
FBA_D45	AA24	VMA_DQ45
FBA_D46	Y22	VMA_DQ46
FBA_D47	AA23	VMA_DQ47
FBA_D48	AD27	VMA_DQ48
FBA_D49	AB25	VMA_DQ49
FBA_D50	AD26	VMA_DQ50
FBA_D51	AC25	VMA_DQ51
FBA_D52	AA27	VMA_DQ52
FBA_D53	AA26	VMA_DQ53
FBA_D54	W26	VMA_DQ54
FBA_D55	Y25	VMA_DQ55
FBA_D56	R26	VMA_DQ56
FBA_D57	T25	VMA_DQ57
FBA_D58	N27	VMA_DQ58
FBA_D59	R27	VMA_DQ59
FBA_D60	V26	VMA_DQ60
FBA_D61	V27	VMA_DQ61
FBA_D62	W27	VMA_DQ62
FBA_D63	W25	VMA_DQ63

FBA_DQM0	D19	VMA_DM0
FBA_DQM1	D14	VMA_DM1
FBA_DQM2	C17	VMA_DM2
FBA_DQM3	C22	VMA_DM3
FBA_DQM4	P24	VMA_DM4
FBA_DQM5	W24	VMA_DM5
FBA_DQM6	AA25	VMA_DM6
FBA_DQM7	U25	VMA_DM7

FBA_DQS_WP0	E19	VMA_WDQS0
FBA_DQS_WP1	C15	VMA_WDQS1
FBA_DQS_WP2	B16	VMA_WDQS2
FBA_DQS_WP3	B22	VMA_WDQS3
FBA_DQS_WP4	R25	VMA_WDQS4
FBA_DQS_WP5	W23	VMA_WDQS5
FBA_DQS_WP6	AB26	VMA_WDQS6
FBA_DQS_WP7	T26	VMA_WDQS7

FBA_DQS_RN0	F19	VMA_RDQS0
FBA_DQS_RN1	C14	VMA_RDQS1
FBA_DQS_RN2	A16	VMA_RDQS2
FBA_DQS_RN3	A22	VMA_RDQS3
FBA_DQS_RN4	P25	VMA_RDQS4
FBA_DQS_RN5	W22	VMA_RDQS5
FBA_DQS_RN6	AB27	VMA_RDQS6
FBA_DQS_RN7	T27	VMA_RDQS7

[20] FBA_CMD0 → C27 FBA_CMD0
C26 FBA_CMD1
[20] FBA_CMD2 → FBA_CMD2 E24 FBA_CMD2
[20] FBA_CMD3 → FBA_CMD3 F24 FBA_CMD3
D27 FBA_CMD4
[20] FBA_CMD5 → FBA_CMD5 D26 FBA_CMD5
[20] FBA_CMD6 → F25 FBA_CMD6
[20] FBA_CMD7 → F26 FBA_CMD7
[20] FBA_CMD8 → F23 FBA_CMD8
[20] FBA_CMD9 → G22 FBA_CMD9
[20] FBA_CMD10 → G23 FBA_CMD10
[20] FBA_CMD11 → G24 FBA_CMD11
[20] FBA_CMD12 → F27 FBA_CMD12
[20] FBA_CMD13 → G25 FBA_CMD13
[20] FBA_CMD14 → G27 FBA_CMD14
[20] FBA_CMD15 → G26 FBA_CMD15
[20] FBA_CMD16 → M24 FBA_CMD16
M23 FBA_CMD17
[20] FBA_CMD18 → FBA_CMD18 K24 FBA_CMD18
[20] FBA_CMD19 → FBA_CMD19 K23 FBA_CMD19
[20] FBA_CMD20 → M27 FBA_CMD20
[20] FBA_CMD21 → M26 FBA_CMD21
[20] FBA_CMD22 → M25 FBA_CMD22
[20] FBA_CMD23 → K26 FBA_CMD23
[20] FBA_CMD24 → K22 FBA_CMD24
[20] FBA_CMD25 → J23 FBA_CMD25
[20] FBA_CMD26 → J25 FBA_CMD26
[20] FBA_CMD27 → J24 FBA_CMD27
[20] FBA_CMD28 → K27 FBA_CMD28
[20] FBA_CMD29 → K25 FBA_CMD29
[20] FBA_CMD30 → J27 FBA_CMD30
[20] FBA_CMD31 → J26 FBA_CMD31

For debug only 10mA
1.5V_GPU → R131 *DIS@60.4/F_4 FBA_DEBUG0 → F22 FBA_DEBUG0
R128 *DIS@60.4/F_4 FBA_DEBUG1 → J22 FBA_DEBUG1

[20] VMA_CLK0 → D24 FBA_CLK0
[20] VMA_CLK0# → D25 FBA_CLK0
[20] VMA_CLK1 → N22 FBA_CLK1
[20] VMA_CLK1# → M22 FBA_CLK1

D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67

1.05V_GFX_PCIE
Near GPU 15mils width
L21 DIS@HCB1608KF-300T10_1A_6
200mA
+FB_PLLAVDD → F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22

FB_DLLAVDD	FB_PLLAVDD
GF119/GK208	GF117

30ohm/100MHz
ESR=0.01ohm

Under GPU
C167 DIS@0.1U/10V/X7R_4
C448 DIS@0.1U/10V/X7R_4
C169 DIS@0.1U/10V/X7R_4
Near GPU
C431 DIS@22U/6.3V/X5R_8

FB_VREF_PROBE → D23 +FB_VREF1 → TP8

U_GPU_GB2_64

GC6 feature for N14M-GS

DIS@2N7002_200MA
Q12
[31,46] FB_CLAMP → FB_CLAMP 3 1 → FB_CLAMP_MON [19]
2
C174 *DIS@10U/6.3V/X5R_6
R161 DIS@10K/F_4
+5V_ALW
R189 *DIS@10K/F_4
3V_GPU
R591 DIS@0_4
Q20A *DIS@2N7002KDW
C193 *DIS@10U/6.3V/X5R_6
+3.3V_DSW
R219 *DIS@10K/F_4
[16,31,45,46] GFXON → 2
Q20B *DIS@2N7002KDW

2.16A

1.5V_GPU

U39D
bga595-nvidia-n13m-gs-s-a2
COMMON
12/14 FBVDDQ

FBVDDQ	B26	
FBVDDQ	C25	
FBVDDQ	E23	
FBVDDQ	E26	
FBVDDQ	F14	
FBVDDQ	F21	
FBVDDQ	G13	
FBVDDQ	G14	
FBVDDQ	G15	
FBVDDQ	G16	
FBVDDQ	G18	
FBVDDQ	G19	
FBVDDQ	G20	
FBVDDQ	G21	
FBVDDQ	H24	
FBVDDQ	H26	
FBVDDQ	J21	
FBVDDQ	K21	
FBVDDQ	L22	
FBVDDQ	L24	
FBVDDQ	L26	
FBVDDQ	M21	
FBVDDQ	N21	
FBVDDQ	R21	
FBVDDQ	T21	
FBVDDQ	V21	
FBVDDQ	W21	

Under GPU
C116 DIS@0.1U/10V/X7R_4
C136 DIS@0.1U/10V/X7R_4
C168 DIS@4.7U/6.3V/X5R_6
C156 DIS@1U/10V/X7R_6
C105 DIS@1U/10V/X7R_6
C155 DIS@4.7U/6.3V/X5R_6
C484 DIS@10U/6.3V/X5R_6
C487 DIS@22U/6.3V/X5R_8
Near GPU

1.5V_GPU
R526 DIS@40.2/F_4 FB_CAL_PD_VDDQ → D22 FB_CAL_PD_VDDQ
R522 DIS@42.2/F_4 FB_CAL_PU_GND → C24 FB_CAL_PU_GND
R517 DIS@51.1/F_4 FB_CAL_TERM_GND → B25 FB_CALTERM_GND

U_GPU_GB2_64

U39F
bga595-nvidia-n13m-gs-s-a2
COMMON
13/14 GND

M13	GND	A2
M15	GND	AB17
M17	GND	AB20
N10	GND	AB24
N12	GND	AC2
N14	GND	AC22
N16	GND	AC26
N18	GND	AC5
P11	GND	AC8
P13	GND	AD12
P15	GND	AD13
P17	GND	A26
P2	GND	AD15
P23	GND	AD16
P26	GND	AD18
P5	GND	AD19
R10	GND	AD21
R12	GND	AD22
R14	GND	AE11
R16	GND	AE14
R18	GND	AE17
T11	GND	AE20
T13	GND	AB11
T15	GND	AF1
T17	GND	AF11
U10	GND	AF14
U12	GND	AF17
U14	GND	AF20
U16	GND	AF23
U18	GND	AF5
U2	GND	AF8
U23	GND	AG2
U26	GND	AG26
U5	GND	AB14
V11	GND	B1
V13	GND	B11
V15	GND	B14
V17	GND	B17
Y2	GND	B20
Y23	GND	B23
Y26	GND	B27
Y5	GND	B5
	GND	B8
	GND	E11
	GND	E14
	GND	E17
	GND	E2
	GND	E20
	GND	E22
	GND	E25
	GND	E5
	GND	E8
	GND	H2
	GND	H23
	GND	H25
	GND	H5
	GND	K11
	GND	K13
	GND	K15
	GND	K17
	GND	L10
	GND	L12
	GND	L14
	GND	L16
	GND	L18
	GND	L2
	GND	L23
	GND	L25
	GND	L5
AA7	GND	M11
AB7	GND	

U_GPU_GB2_64

FBA_CMD2 R474 DIS@10K/F_4
FBA_CMD3 R499 DIS@10K/F_4
FBA_CMD5 R122 DIS@10K/F_4
FBA_CMD18 R415 DIS@10K/F_4
FBA_CMD19 R423 DIS@10K/F_4

DDR3 Command Bit	Data[31..0]	Data[63..32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	N14M-GS (MEMORY/GND) 2/5	1A
Date: Thursday, January 03, 2013	Sheet 17 of 47	

<VGA> <HDM> <CRT>

[16,17,46,47] 1.05V_GFX_PCIE

Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm

U39G
bga595-nvidia-n13m-gs-s-a2
COMMON
4/14 IFPAB

IFPAB
U_GPU_GB2_64

U39K
bga595-nvidia-n13m-gs-s-a2
COMMON
3/14 DACA
U_GPU_GB2_64

U39I
bga595-nvidia-n13m-gs-s-a2
COMMON
6/14 IFPD
IFPD
U_GPU_GB2_64

U39H
bga595-nvidia-n13m-gs-s-a2
COMMON
5/14 IFPC
IFPC
U_GPU_GB2_64

U39J
bga595-nvidia-n13m-gs-s-a2
COMMON
7/14 IFPEF
IFPE
IFPF
U_GPU_GB2_64

1.05V_GFX_PCIE

Near GPU
L23 DIS@HCB1608KF-300T10_1A_6
12~16mils
12~16mils
1.05V_GFX_PCIE
Near GPU
L24 DIS@BLM18PG181SN1 180/1500mA
+NV_PLLVDD
+SP_PLLVDD
C498 DIS@0.1U/10V/X7R_4 Under GPU
C499 DIS@22U/6.3V/X5R_8 Near GPU
C497 DIS@22U/6.3V/X5R_8 Near GPU
C500 DIS@4.7U/6.3V/X5R_6
C134 DIS@0.1U/10V/X7R_4 Under GPU
C135 DIS@0.1U/10V/X7R_4
R113 0_4
R488 DIS@10K/F_4
R531 DIS@0_4
XTAL_SSIN
XTALIN
U39M
bga595-nvidia-n13m-gs-s-a2
COMMON
9/14 XTAL_PLL
U_GPU_GB2_64
XTALOUTBUFF
XTALOUT
R518 DIS@10K/F_4
Y6 *DIS@27MHz
C517 *DIS@8.2P/50V/C0G_4
C518 *DIS@8.2P/50V/C0G_4
[35] GPU_XTAL27_IN

PROJECT :	LZ9A
Quanta Computer Inc.	
Size	Document Number: N14M-GS (DISPLAY) 3/5 — Rev: 1A
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U39L
bga595-nvidia-n13m-gs-s-a2
COMMON

10/14 MISC2

	GF117/GF119/GK208
VMON_IN0	NC
VMON_IN1	NC

T46 E10 VMON_IN0
T52 F10 VMON_IN1

ROM_CS D12 ROM_CS
ROM_SI B12 ROM_SI
ROM_SO A12 ROM_SO
ROM_SCLK C12 ROM_SCLK

STRAP0 D1 STRAP0
STRAP1 D2 STRAP1
STRAP2 E4 STRAP2
STRAP3 E3 STRAP3
STRAP4 D3 STRAP4

GF119	GF117 GK208
STRAP5_NC	NC

C1

BUFRST D11 R185 *DIS@10K/F_4 R180 *DIS@10K/F_4 3V_GPU

NC	PGOOD
GF117 GK208	GF119

D10 T105

E9 R184 *DIS@10K/F_4 R179 *DIS@10K/F_4 3V_GPU

NC	CEC
GF117 GK208 GF119	

R171 DIS@40.2K/F_4 F6 MULTISTRAP_REF0_GND

GF119	GF117 GK208
MULTISTRAP_REF1_GND	NC
MULTISTRAP_REF2_GND	NC

R157 *DIS@40.2K/F_4 F4 MULTISTRAP_REF1_GND
R163 *DIS@40.2K/F_4 F5 MULTISTRAP_REF2_GND

U_GPU_GB2_64

U39N
bga595-nvidia-n13m-gs-s-a2
COMMON

8/14 MISC1

I2CS_SCL D9 DGPU_I2CS_SCL
I2CS_SDA D8 DGPU_I2CS_SDA

I2CC_SCL A9 I2CC_SCL_G R493 DIS@2.2K_4 3V_GPU
I2CC_SDA B9 I2CC_SDA_G R516 DIS@2.2K_4

GF117	GF119 GK208
NC	NC
NC	NC

I2CB_SCL C9 I2CB_SCL_G R494 DIS@2.2K_4 3V_GPU
I2CB_SDA C8 I2CB_SDA_G R495 DIS@2.2K_4

T48 E12 THERMDN
T49 F12 THERMDP

T67 AE5 JTAG_TCK
T3 AD6 JTAG_TMS
T2 AE6 JTAG_TDI
T66 AF6 JTAG_TDO
T68 AG4 JTAG_TRST#

GPIO0 C6 FB_CLAMP_MON [17]
GPIO1 B2
GPIO2 D6
GPIO3 C7
GPIO4 F9
GPIO5 A3
GPIO6 A4 FB_CLAMP_TGL_REQ#
GPIO7 B6 3D_STEREO
GPIO8 A6 DGPU_GPIO8
GPIO9 F8 EXT_ALERT#
GPIO10 C5 MEM_VREF_CTL
GPIO11 E7
GPIO12 D7 AC_BATT_DEC_R D17 DIS@RB500V-40 PWM-VID [45]
GPIO13 B4 PSI_GPU# AC_PRESENT [8,31] PSI_GPU# [45]

GK208 OVERT	GF117	GF119
GPIO16	NC	GPIO16
GPIO20	NC	GPIO20
GPIO8	NC	GPIO21

D5 E6 C4

U_GPU_GB2_64

Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVIDE[5]	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0011

DDR3 RAM_CFG

GPU SKU	GPU	VRAM Vendor	Type	BVDD/ FBVDDQ	Config	VRAM P/N	Max Speed CLK	D/C Mini	RAM_CFG	ROM_SI
GK208/GK107	N14M-GS/N14M-LP/N14P-GV2 N14P-GS/N14P-LP/N14P-GE	Samsung	DDR3	1.5 V/ 1.5 V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x7	PD 45K
						K4W2G1646E-BC11	900Mhz			
		Micro	DDR3	1.5 V/ 1.5 V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1234	0x5	PD 30K
						MT41J128M16JT-107G:K	900Mhz	1150		
		Hynix	DDR3	1.5 V/ 1.5 V	128Mx16	H5TQ2G63DFR-N0C	1000Mhz	NA	0x6	PD 35K
						H5TQ2G63DFR-11C	900Mhz			
		Samsung	DDR3	1.5 V/ 1.5 V	256Mx16	K4W4G1646B-HC11	900Mhz	NA	0x3	PD 20K
		Micro	DDR3	1.5 V/ 1.5 V	256Mx16	MT41K256M16HA-107G:E	900Mhz	NA	0x1	PD 10K
		Samsung	DDR3L	1.35V/ 1.35V	128Mx16	K4W2G1646E-BY11	900Mhz	1204	0xA	PU 15K
		Micro	DDR3L	1.35V/ 1.35V		MT41K128M16JT-107G:K	900Mhz	NA	0x8	PU 5K

3V_GPU
R489 *DIS@10K/F_4
R520 DIS@4.99K/F_4
R492 DIS@4.99K/F_4
ROM_SI
ROM_SO
ROM_SCLK
R490 DIS@20K/F_4
R523 *DIS@10K/F_4
R491 *DIS@10K/F_4

3V_GPU
STRAP0 R472 DIS@45.3K/F_4
STRAP1 R477 *DIS@10K/F_4
STRAP2 R501 *DIS@10K/F_4
STRAP3 R466 *DIS@10K/F_4
STRAP4 R505 *DIS@10K/F_4
R471 *DIS@10K/F_4
R476 DIS@45.3K/F_4
R500 DIS@4.99K/F_4
R465 DIS@4.99K/F_4
R504 DIS@45.3K/F_4

3V_GPU R527 *0_4 R528 DIS@0_4 GFXPG [4,16]
Q39 DIS@2N7002
DGPU_GPIO8 VGA_OVT# [31]

3V_GPU R190 DIS@10K/F_4
3V_GPU Q17 DIS@2N7002
EXT_ALERT# VR_TT# [4]

R200 *0_4
DGPU_I2CS_SCL MBCLK_THRM [7,31]
Q13A DIS@2N7002KDW
R186 DIS@2.2K_4
3V_GPU
R197 DIS@2.2K_4
DGPU_I2CS_SDA MBDATA_THRM [7,31]
Q13B DIS@2N7002KDW
R198 *0_4

3V_GPU
AC_BATT_DEC_R R521 DIS@100K/F_4
ROM_CS R181 *DIS@10K/F_4
JTAG_TMS R22 *DIS@10K/F_4
JTAG_TDI R23 *DIS@10K/F_4
DGPU_GPIO8 R497 DIS@10K/F_4
PSI_GPU# R519 DIS@10K/F_4
JTAG_TRST# R370 DIS@10K/F_4
JTAG_TCK R369 *DIS@10K/F_4
3D_STEREO R496 DIS@100K/F_4
MEM_VREF_CTL R498 DIS@100K/F_4

GC6 feature for N14M-GS

3V_GPU R214 DIS@10K/F_4
3V_GPU
+3.3V_RUN R217 10K/F_4
FB_CLAMP_TGL_REQ#
Q18 DIS@2N7002
FB_CLAMP_TGL_REQ_EC# [31]

GK208 SKU	
Item	N14M-GS-B/S-A2
Device ID	0X1290
Package	GB4-128
Internal P/N	GK208,28nm
ROM_SI	Refer to N14x_RAM_Straps table
ROM_SO	0x8, 5kohm pull high
ROM_SCLK	0x1000,0x8, 4.99Kohm pull up
Strap0	User Strap, 0xF, 45kohm pull up
Strap1	3GIO_PAD_Config, 0x7, 45kohm pull down(After QS)
Strap2	Device_ID, 0x0000_5Kohm pull down
Strap3	0x0 for Optimus, 5kohm pull low
Strap4	0x0111, 45kohm pull down(PCIE_SPEED_CHANGE=1)
Open_VRG SKU	Config B
NVVDD Boot Voltage	0.9V

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	N14M-GS (GPIO/STRAPS) 4/5	1A
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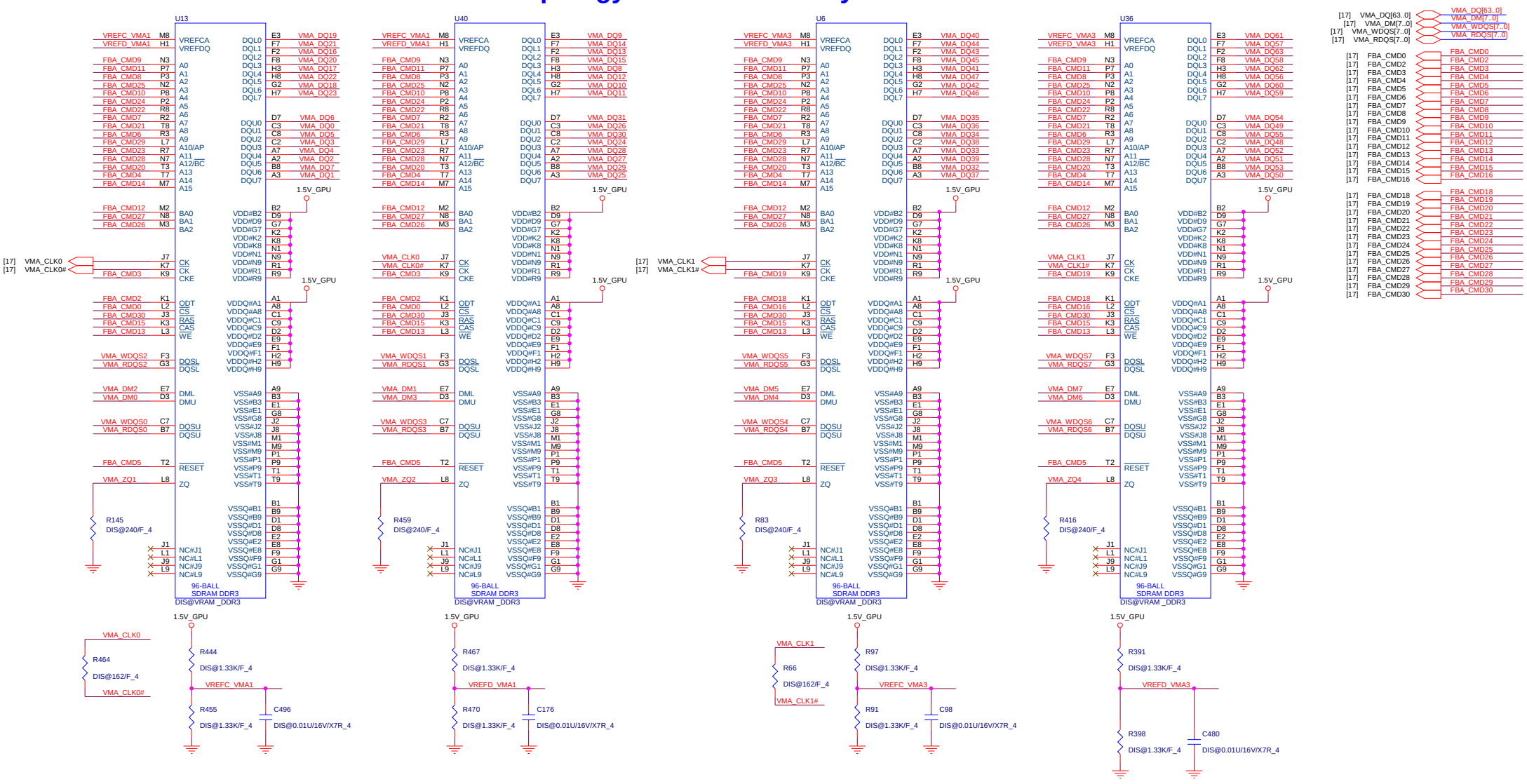
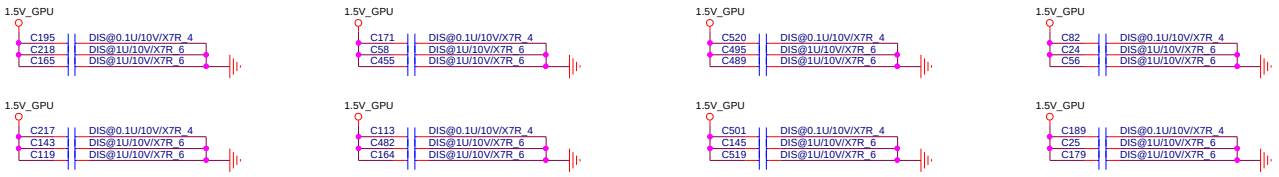
CHANNEL A: DDR3 4Gb x4
Double T Topology for DDR3 Memory



REV-00 change R3086 and R3091 from 240/F_4 to160 Ohms



Close to DRAM

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 VRAM (BGA96) 5/5	1A
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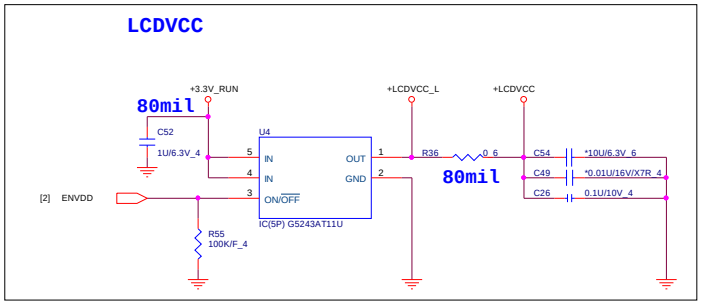
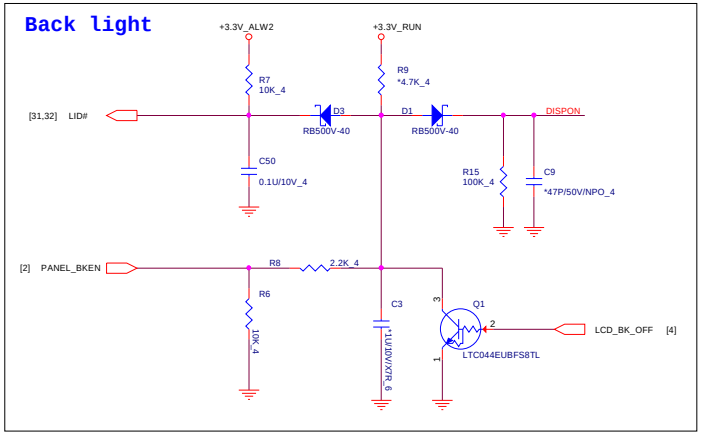
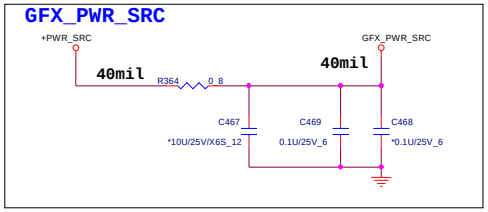
LCDVCC

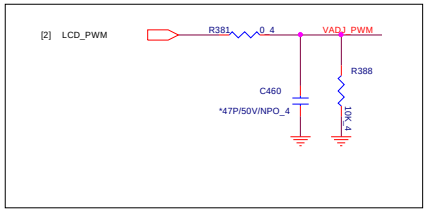


Back light



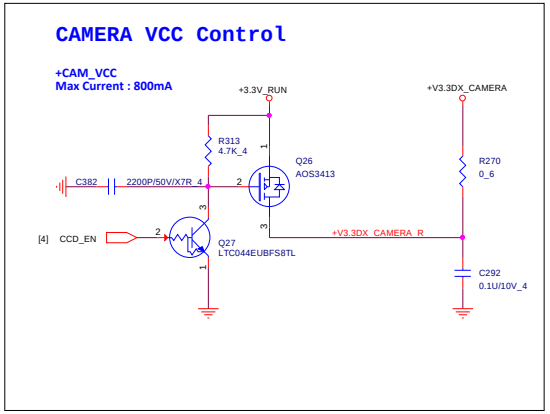
GFX_PWR_SRC



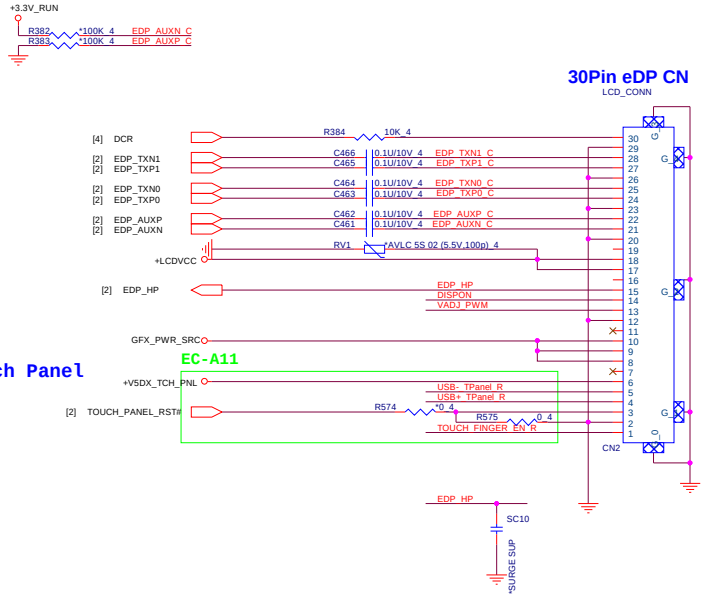


CAMERA VCC Control

+CAM_VCC
Max Current : 800mA

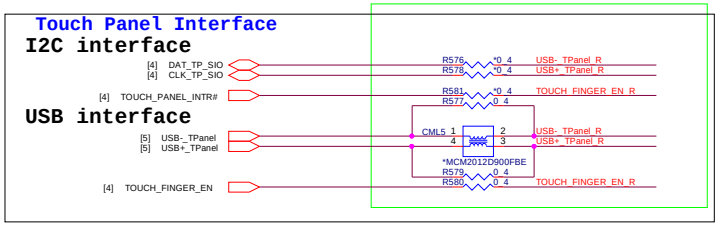


Touch Panel



Touch Panel Interface

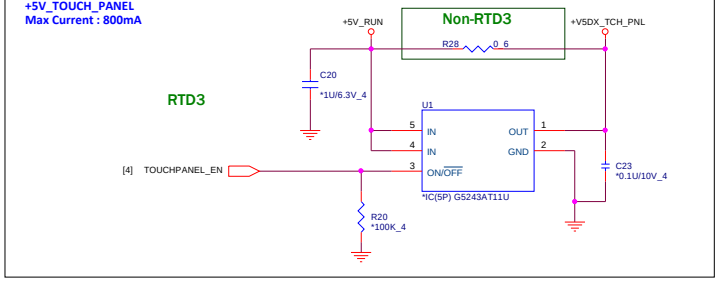
I2C interface



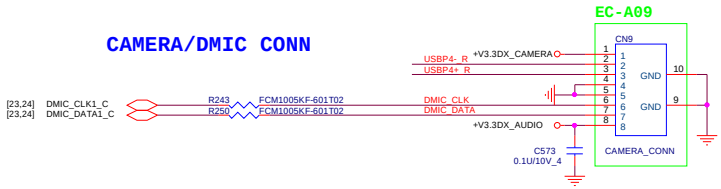
USB interface

Touch Panel VCC Control

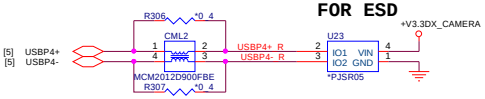
+5V_TOUCH_PANEL
Max Current : 800mA

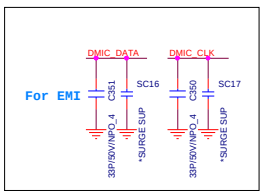


CAMERA/DMIC CONN



FOR ESD





PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	LCD/CAMERA/Touch Panel	1A
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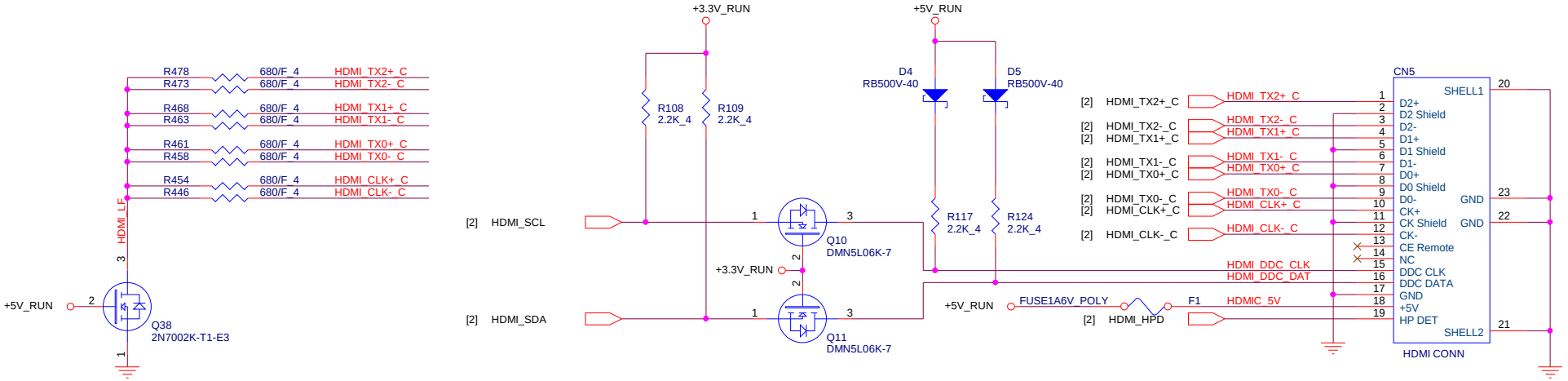
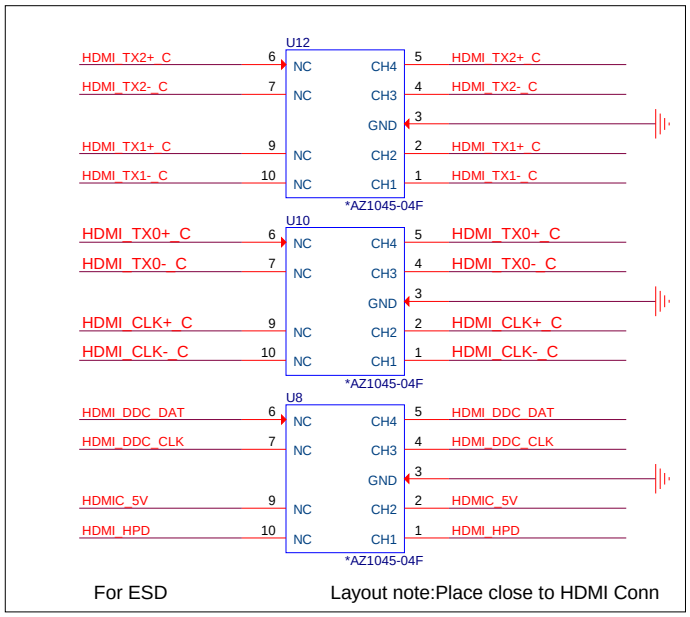
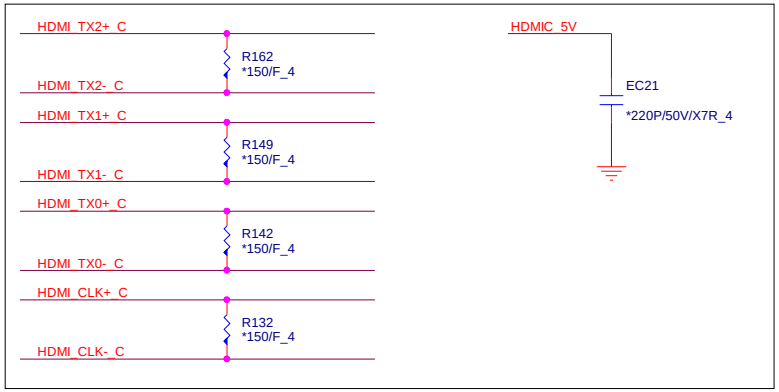




EMI reserve for HDMI



PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: HDMI CONN	Rev: 1A
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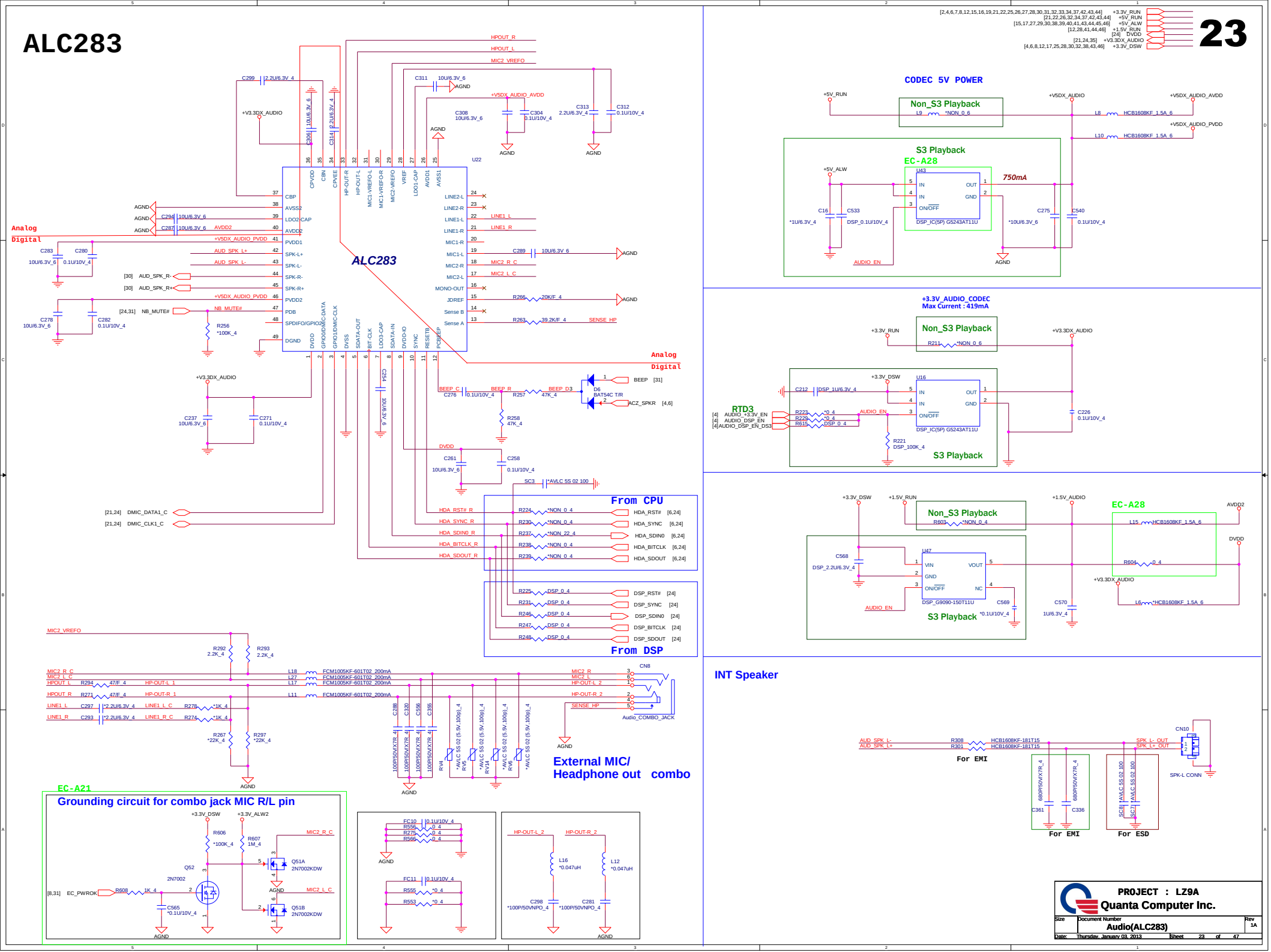
ALC283



PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: Audio(ALC283)	Rev: 1A
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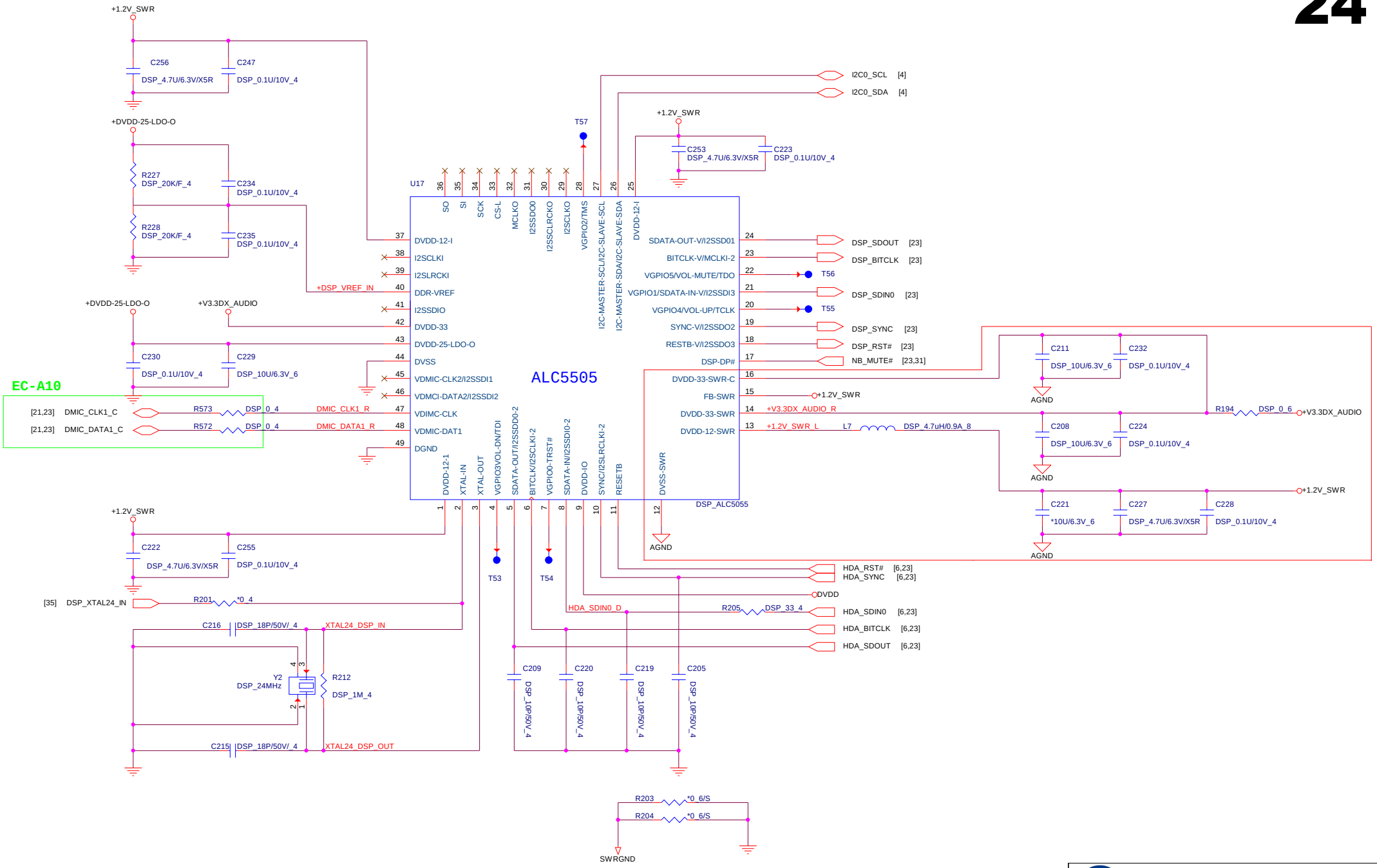

PROJECT : LZ9A		
Quanta Computer Inc.		
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	DSP(ALC5055)	1A
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[35,44] LANVCC
[4,6,8,12,17,23,28,30,32,38,43,46] +3.3V_DSW
[2,4,6,7,8,12,15,16,19,21,22,23,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN

LANVCC

+3.3V_DSW
Q4
AO3413
LANVCC
40 mils (Iout=1A)
40 mils (Iout=1A)
R4 4.7K_4
R37 *100K/F_4
C55 0.1U/10V_4
C51 10U/6.3V_6
C2 0.01U/16V/X7R_4

AOAC

[31,44] LAN_POWER
[8,44] SIO_SLP_LAN#
R46 0_4
R47 *0_4
Q7 LTC044EUBFS8TL

LANVCC
Trace width>60mil,
Trace length<200mil

U2 RTL8111GUS-CG

VDD10
R44 2.49K/F_4 RSET 10 mils
C28 *10P/50V/COG_4
C19 *10P/50V/COG_4
TP4 TP1 TP2
LANVCC
R38 0_4 LAN_XTAL25_IN [35]
C53 *6.8P/50V_4
XTAL2
Y1 *25MHZ +-30PPM
XTAL1
C44 *6.8P/50V_4
GND
MDI_0+ MDI_0-
VDD10
MDI_1+ MDI_1-
MDI_2+ MDI_2-
VDD10
REGOUT
VDDREG/VDD33
VDD10
ISOLATEB
PERSTB
GPP_TX5N_LAN C12 0.1U/10V_4
GPP_TX5P_LAN C13 0.1U/10V_4
PCIE_WAKE# [8,28]
PLTRST# [8,16,30]
PCIE_RXN5 [5]
PCIE_RXP5 [5]
+3.3V_RUN
R11 1K_4
ISOLATEB
D2 RB500V-40
R12 15K_4
LAN_ISOLATE [31]
MDI_3+ MDI_3-
LANVCC
CLK_PCIE_LANN [7]
CLK_PCIE_LANP [7]
PCIE_TXN5 [5]
PCIE_TXP5 [5]
PCIE_CLK_REQ3# [7]

For RTL8106E
* Place 1uF CAP close to each VDD10 pin-- 30 (reserve)

LANVCC
40 mils (Iout=1A)
C459 0.1U/10V_4
C477 0.1U/10V_4
For RTL8111GIS/RTL8106EUS
* Place 0.1uF CAP close to each VDD33 pin-- 11, 32

C5 *0.1U/10V_4
C10 *0.1U/10V_4
For RTL8106E
* Place 0.1uF CAP close to each VDD33 pin-- 23, 32

R10 0_8
40 mils (Iout=1A)
VDDREG/VDD33
C11 0.1U/10V_4
C6 4.7U/6.3V_6
Remove For Not Using SWR mode

REGOUT
R367 *0_8
40 mils (Iout=1A)
C21 *0.1U/10V_4
RTL8111G (LDO mode) support
RTL8106E (LDO mode) doesn't need

L22 4.7uH
C7 4.7U/6.3V_6
C476 0.1U/10V_4
RTL8111GUS/RTL8106EUS-CG
(SWR mode) support

For RTL8111G(S)
* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30 For RTL8106E
* Place 0.1uF CAP close to each VDD10 pin-- 8, 30
40 mils (Iout=1A)
C473 0.1U/10V_4
C475 0.1U/10V_4
C472 0.1U/10V_4
C474 0.1U/10V_4
C8 *1U/6.3V_4
C429 *0.1U/10V_4
C42 *1U/6.3V_4
C426 *0.1U/10V_4
VDD10

For RTL8111G(S)
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

Tramsformer

U34
MDI_0+_C MDI_0-_C
MDI_1-_C MDI_1+_C
*CM1293A-04SO
LANVCC

U37
MDI_2+_C MDI_2-_C
MDI_3-_C MDI_3+_C
*CM1293A-04SO
LANVCC

Reserve for Surge
Line to GND TVS

U35
MDI_3- R82 1/F_4 MDI_3-_C
MDI_3+ R87 1/F_4 MDI_3+_C
MDI_2- R75 1/F_4 MDI_2-_C
MDI_2+ R71 1/F_4 MDI_2+_C
MDI_1- R64 1/F_4 MDI_1-_C
MDI_1+ R53 1/F_4 MDI_1+_C
MDI_0- R48 1/F_4 MDI_0-_C
MDI_0+ R42 1/F_4 MDI_0+_C
TD4- TD4+ TCT4 TD3- TD3+ TCT3 TD2- TD2+ TCT2 TD1- TD1+ TCT1
MX4- MX4+ MCT4 MX3- MX3+ MCT3 MX2- MX2+ MCT2 MX1- MX1+ MCT1
LAN_Transformer_NS892407
LAN_MX3- LAN_MX3+ LAN_MCT0 LAN_MX2- LAN_MX2+ LAN_MCT1 LAN_MX1- LAN_MX1+ LAN_MCT2 LAN_MX0- LAN_MX0+ LAN_MCT3
R80 75/F_12 LANCT3
R70 75/F_12
R54 75/F_12
R45 75/F_12
R90 0_12
C494 10P/3KV/NPO_1808
R106 1M_8
D16 *BS4200N-C_1812
C478 0.01U/50V/X7R_4

Layout:All termination signal should have 30 mil trace

RJ45 Connector

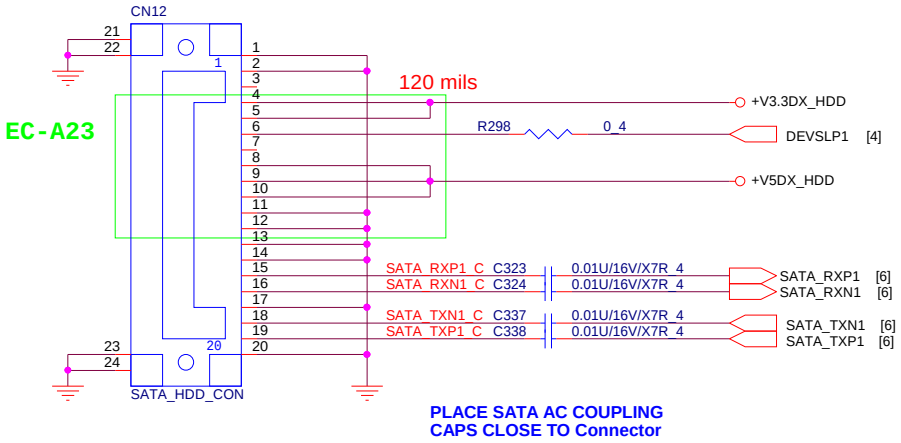
CN1
LAN_MX0+ LAN_MX0- LAN_MX1+ LAN_MX2+ LAN_MX2- LAN_MX1- LAN_MX3+ LAN_MX3-
LAN_RJ45

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	LAN(RTL8111GUS)	1A
Date: Thursday, January 03, 2013	Sheet 25 of 47	

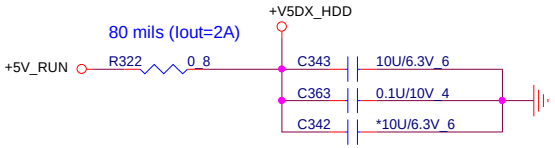
HDD

[2,4,6,7,8,12,15,16,19,21,22,23,25,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[21,22,23,32,34,37,42,43,44] +5V_RUN

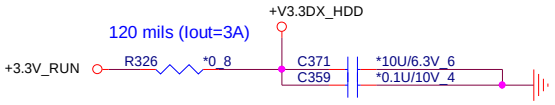


PLACE SATA AC COUPLING
CAPS CLOSE TO Connector

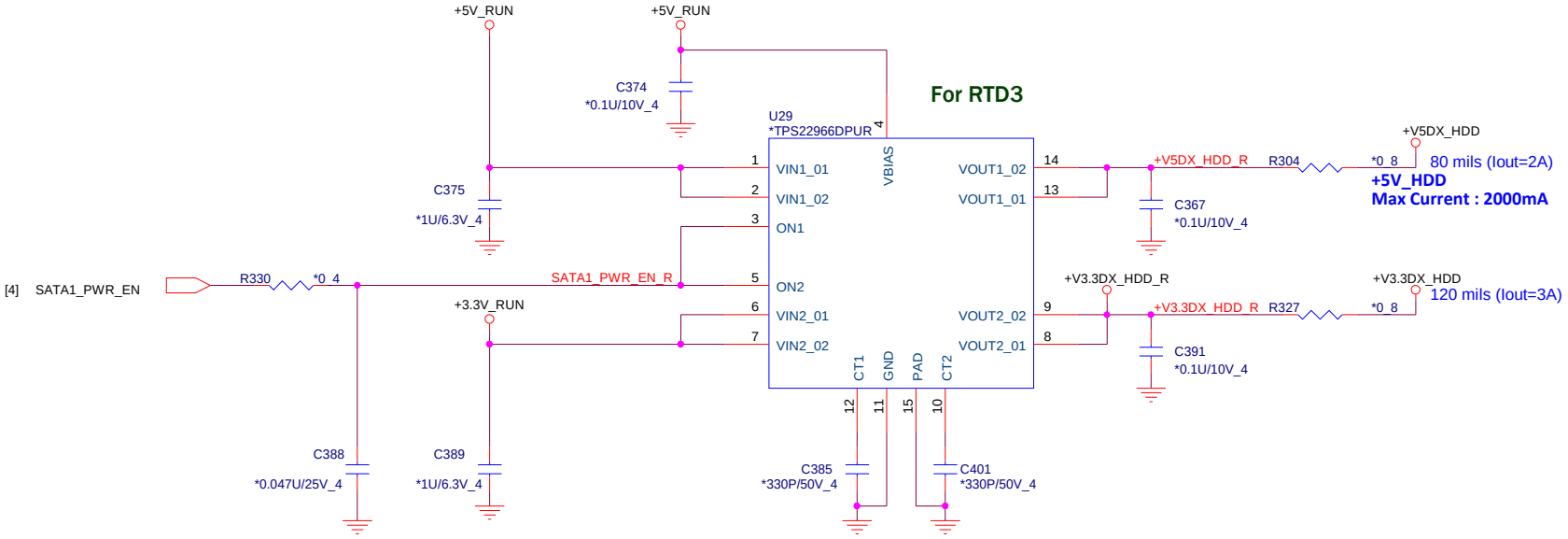
DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



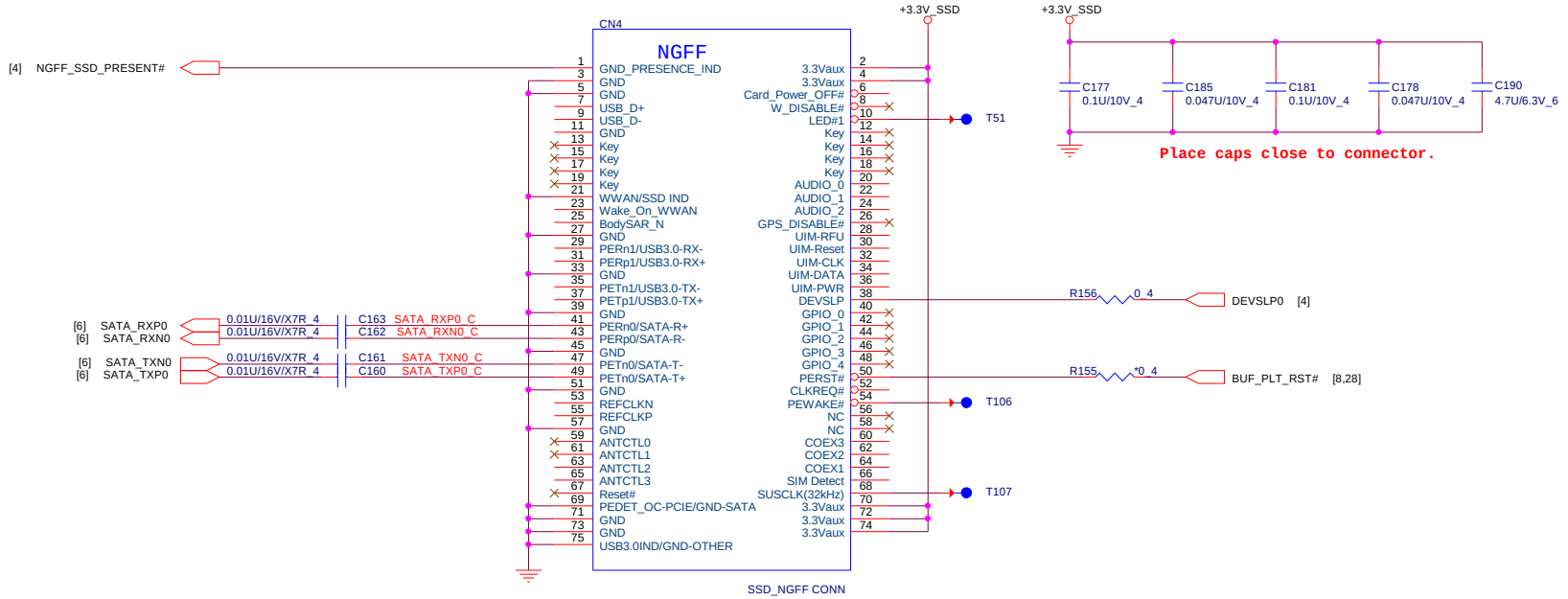
For RTD3

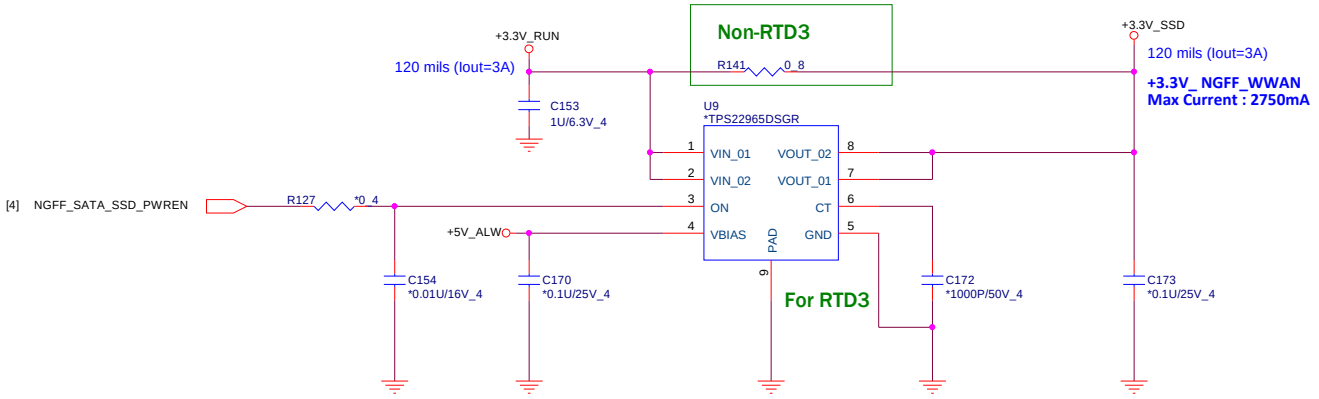


PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: SATA	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 26 of 47	

NGFF SSD connector

[2,4,6,7,8,12,15,16,19,21,22,23,25,26,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN





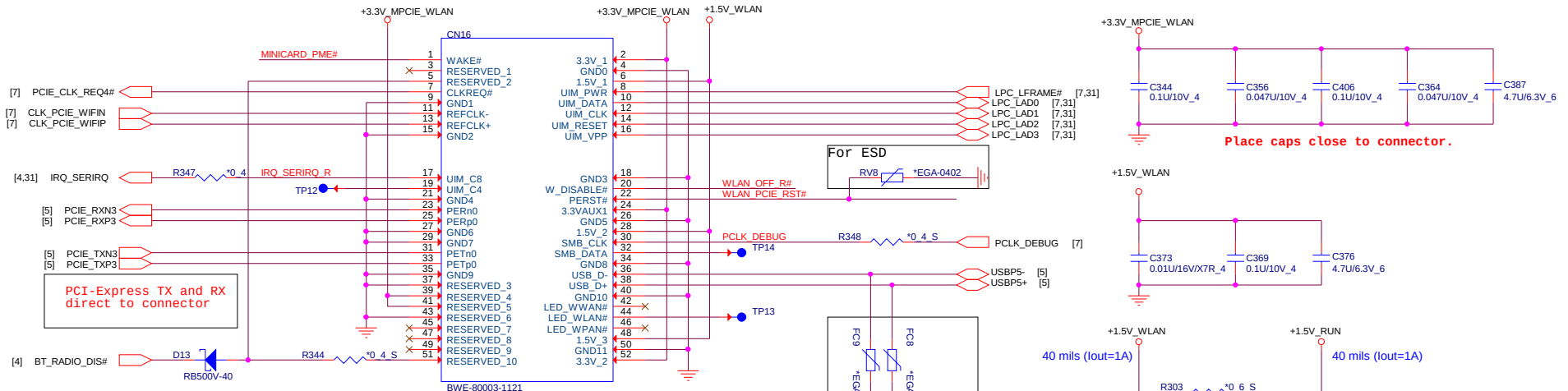
PROJECT : LZ9A

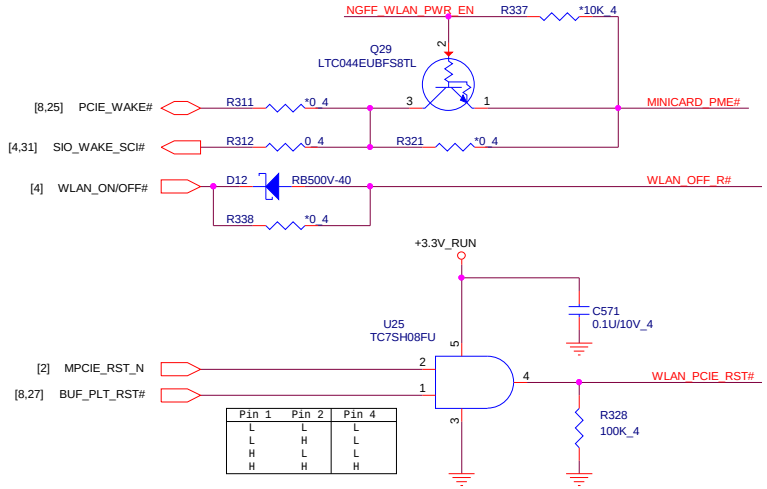
Quanta Computer Inc.

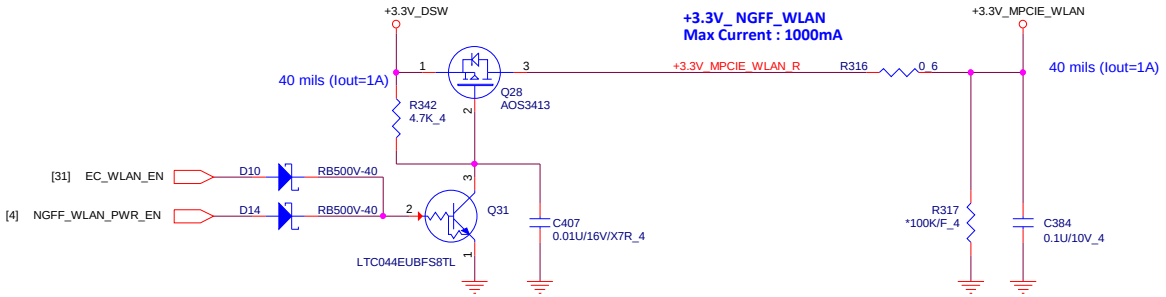
Size	Document Number	Rev
	SSD NGFF	1A
Date: Thursday, January 03, 2013	Sheet 27 of 47	

Mini PCIE Wifi/BT connector

[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[4,6,8,12,17,23,25,30,32,38,43,46] +3.3V_DSW
[12,23,41,44,46] +1.5V_RUN

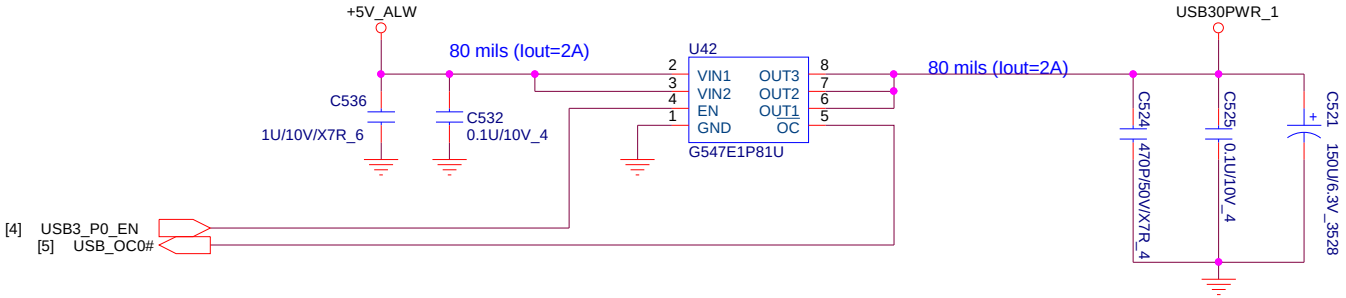


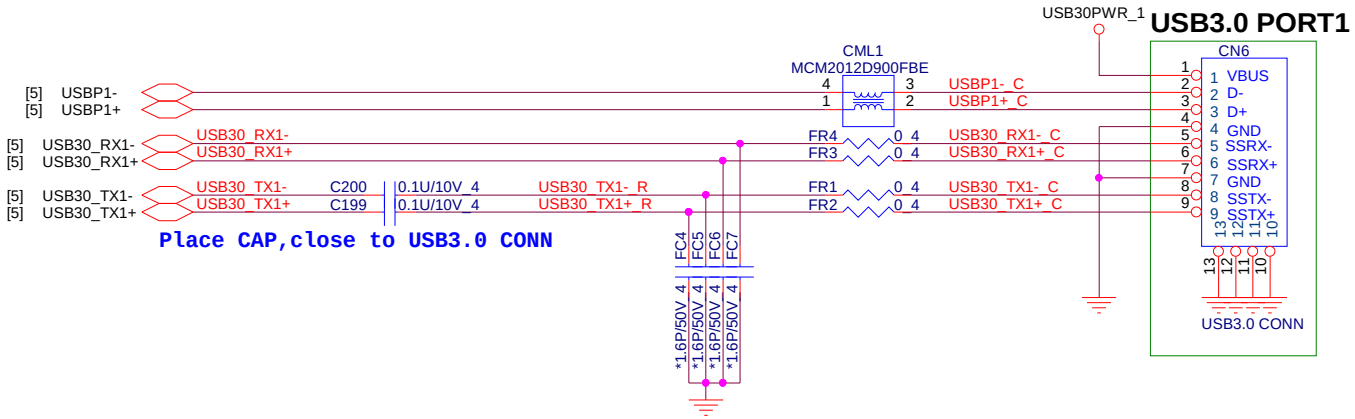


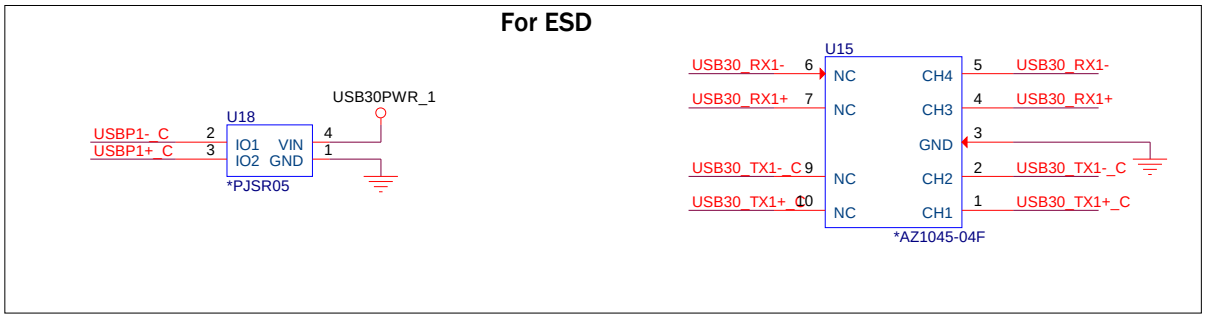


PROJECT : LZ9A			
Quanta Computer Inc.			
Size	Document Number		Rev
	Wifi/BT MiniPCIE		1A
Date: Thursday, January 03, 2013	Sheet 28 of 47		

[15,17,23,27,30,38,39,40,41,43,44,45,46] +5V_ALW





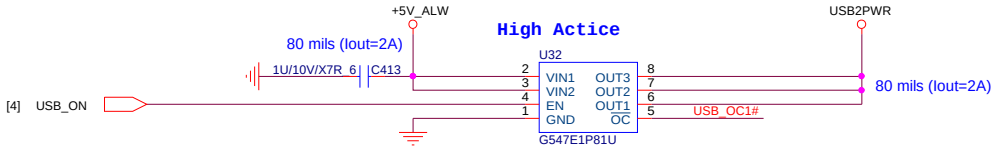


PROJECT : LZ9A

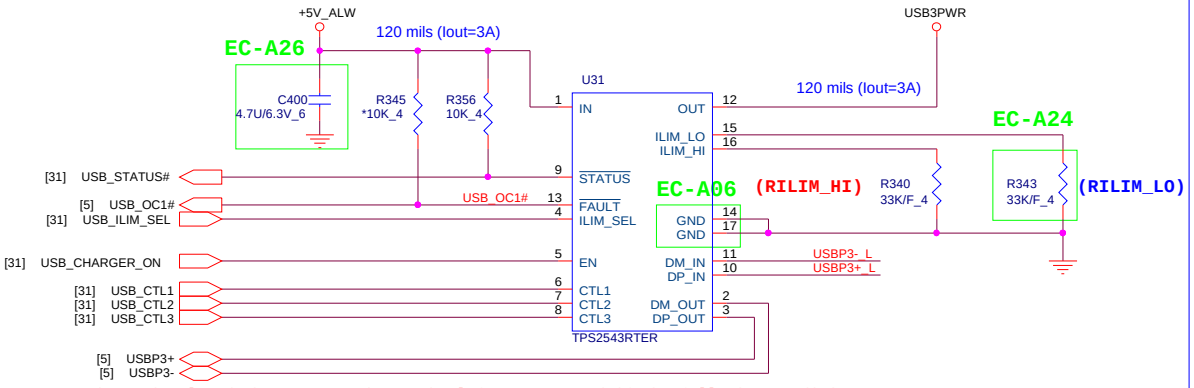
Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x1	1A
Date: Thursday, January 03, 2013	Sheet 29 of 47	

USB 2.0 Port



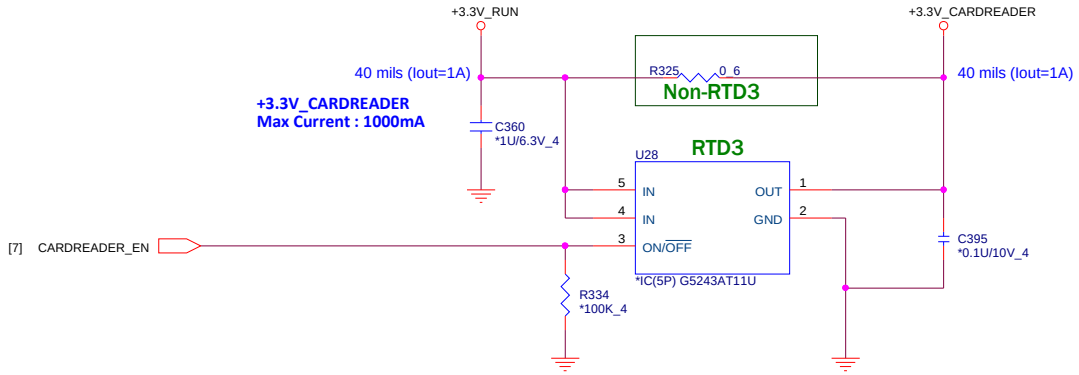
USB Charger 2.0 Port



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

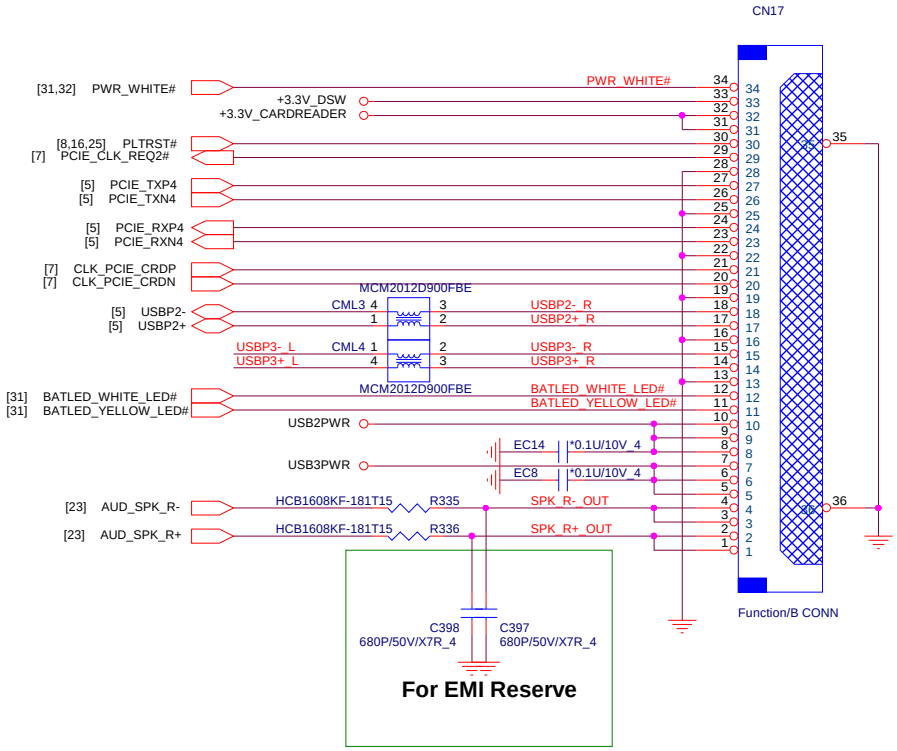
$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

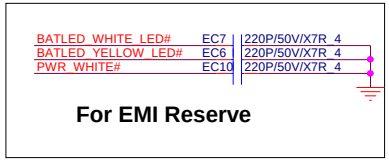
Card Reader VCC Control



[15,17,23,27,29,38,39,40,41,43,44,45,46] +5V_ALW
[4,6,8,12,17,23,25,28,32,38,43,46] +3.3V_DSW
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,31,32,33,34,37,42,43,44] +3.3V_RUN

30





PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	USB2.0--Audio Jack Conn	1A
Date: Thursday, January 03, 2013	Sheet 30 of 47	

IT8587

FOR EC auto load code

Layout Note:
net "+3.3V_ALW2" and "RTC_VCC"
minimum trace width 12mils.

Layout Note:
Place all capacitors close to IT8512.

EMI suggestion:
Add a 15p bypass
CAP on CLK_PCI_8512

For EMI, Close EC. pin74

EC-A29

EC-A25

EC-A46

EC-A22

(For PLL Power)

For ESD

LPC

GPIO

SM BUS

PS/2

CIR

PWM

UART port

WAKE UP

EXTERNAL SERIAL FLASH

SPI ENABLE

KBMX

A/D D/A

CLOCK

For EC E-flash(embedded flash) auto load code

Note:
IT8587 with 128K-byte e-flash
Auto load code condition:
1. Let PCH SPI interface in High-Z state.
2. RSMRST# pull low
(PCH SPI pins are tri-stated prior to RSMRST# de-assertion)
3. EC pin 100(GPG2) pull high(force EC load code)
4. Supply power to SPI flash ROM,PCH(VCCSPI,+1.05V_SUS) and EC

EC Board ID

Thermal reset function

EC reset function, press power button 8 sec

NOVO BUTTON

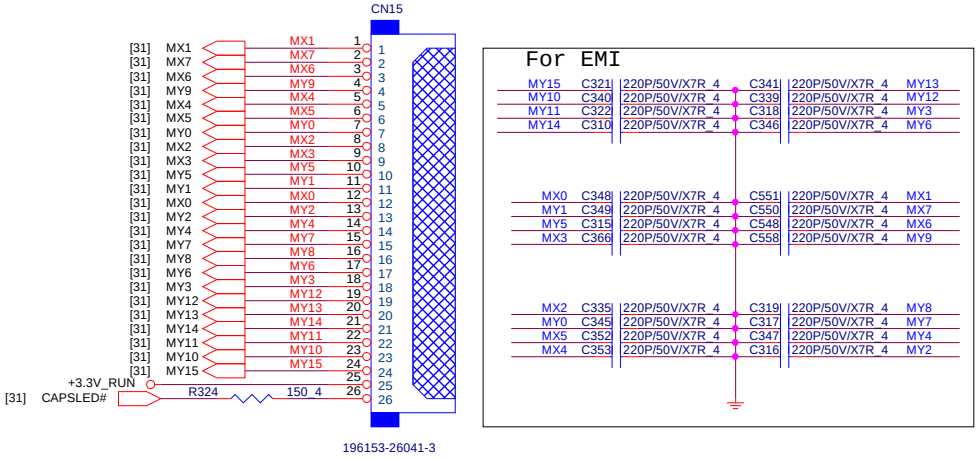
POWER SWITCH

PROJECT : LZ9A
Quanta Computer Inc.

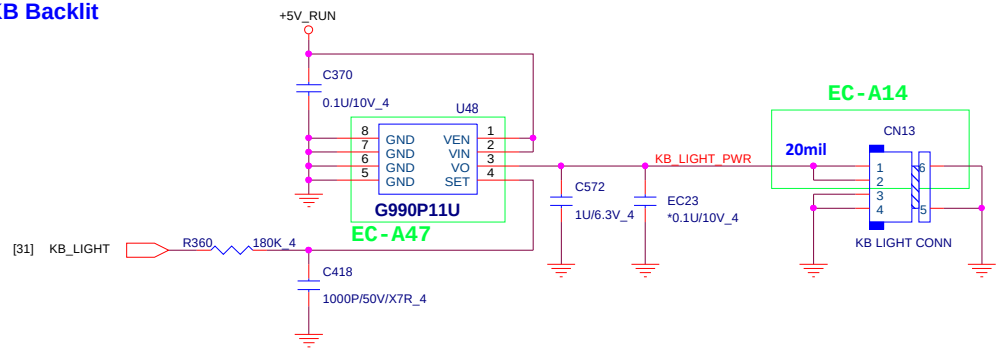
Size	Document Number	Rev
Custom	KBC IT8587	1A

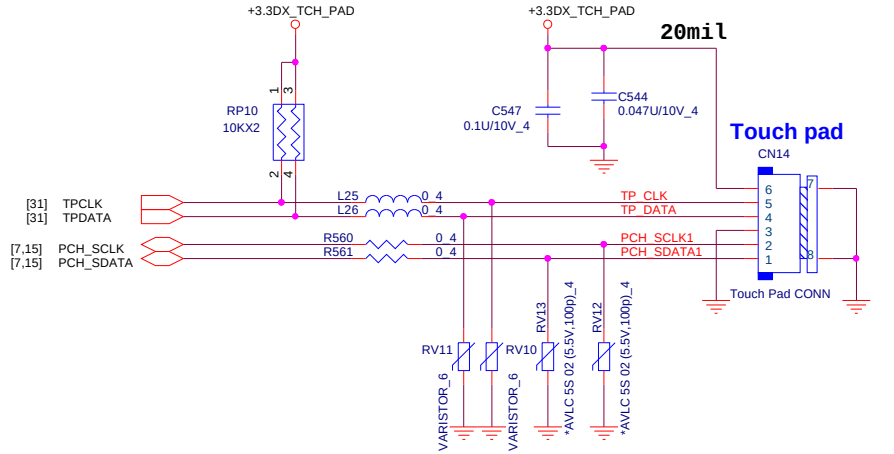
Date: Thursday, January 03, 2013 Sheet 31 of 47

KEYBOARD

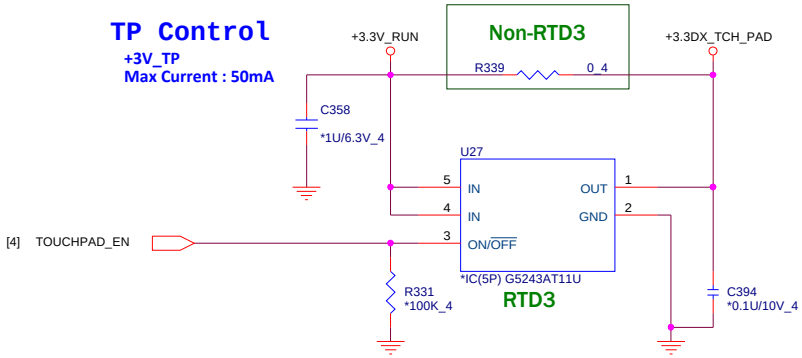


KB Backlit

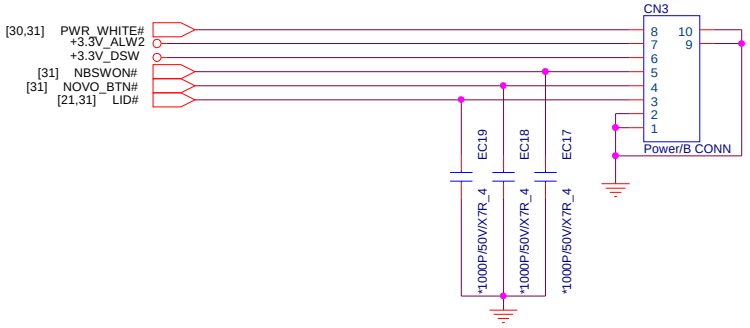




TP Control



Power Board CONN



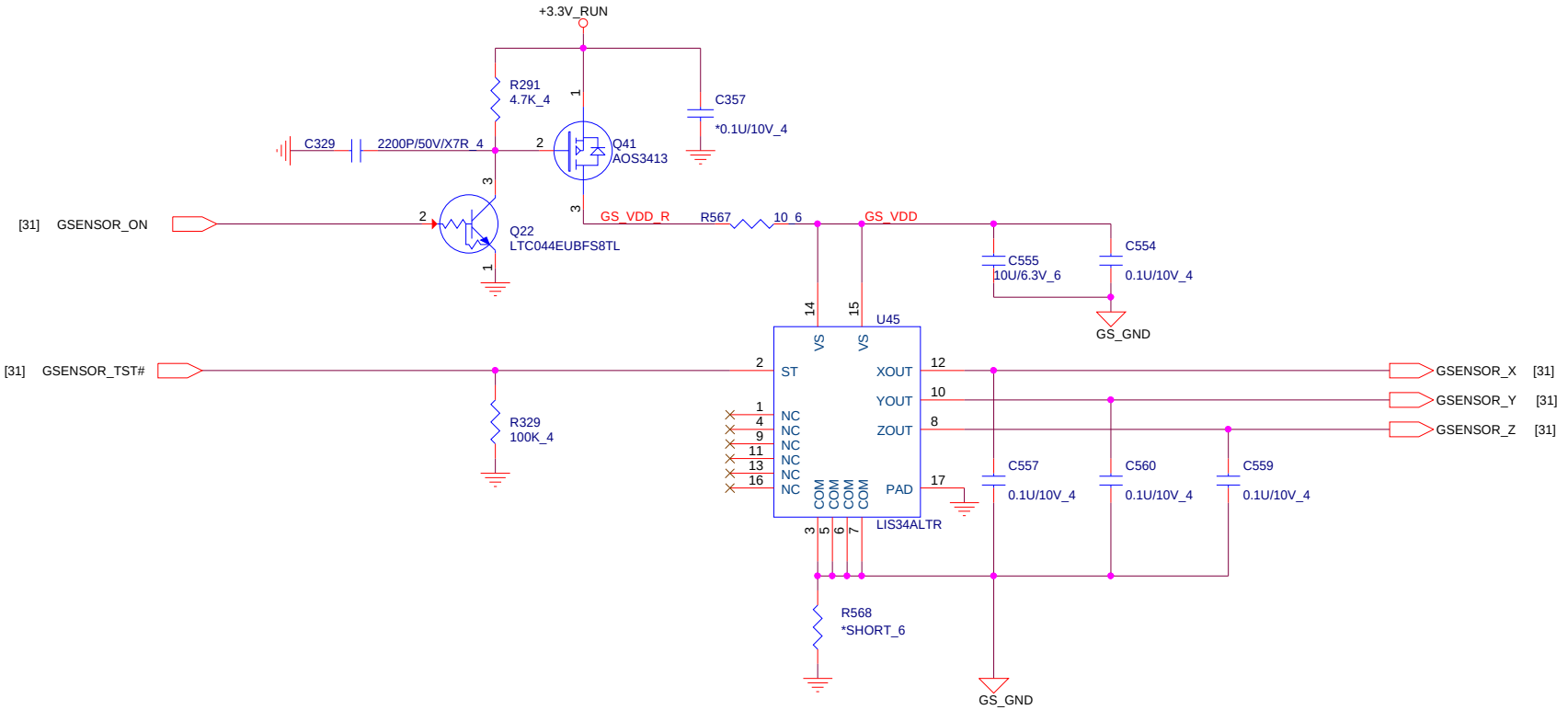
PROJECT : LZ9A

Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/LID	1A
Date: Thursday, January 03, 2013	Sheet 32 of 47	

G-SENSOR (3-Axial)

[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,34,37,42,43,44] +3.3V_RUN

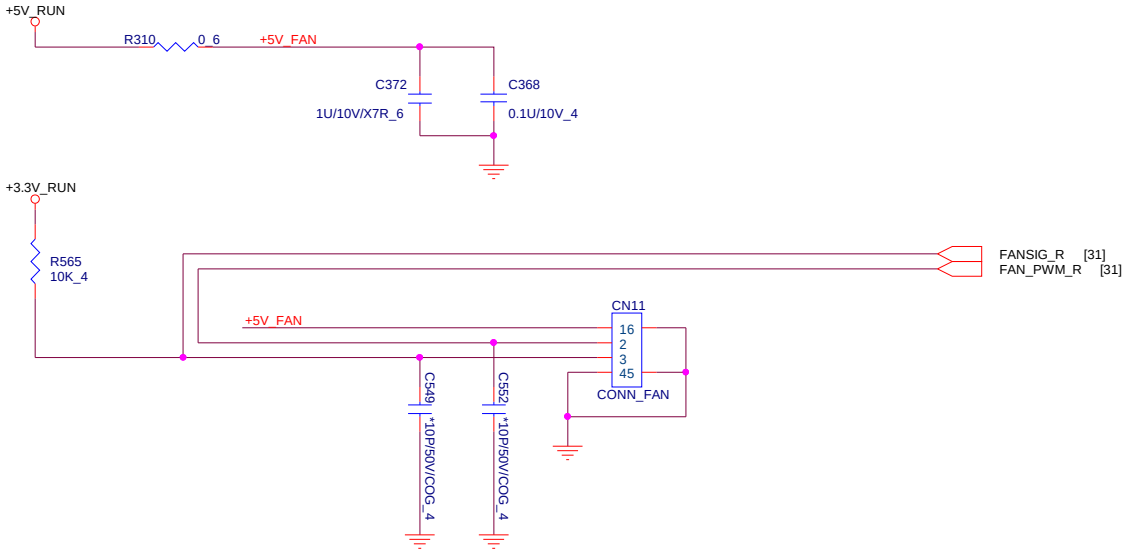


PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: G-sensor	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 33 of 47	

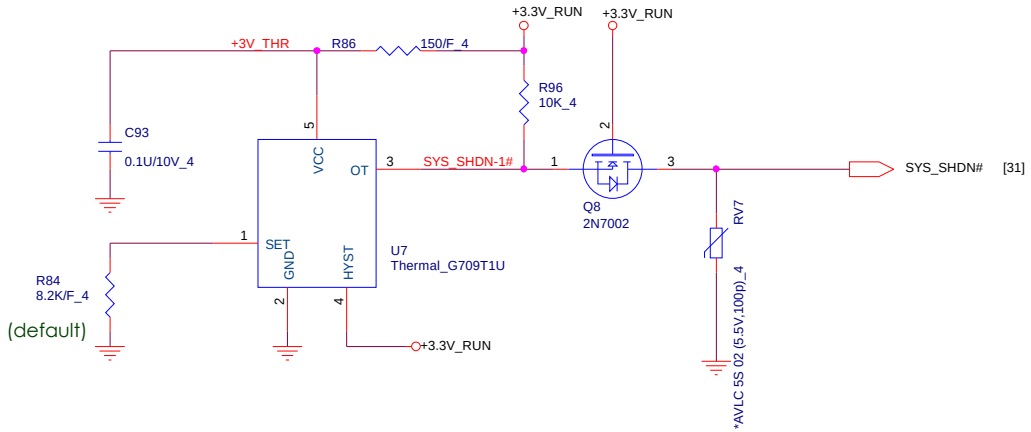
FAN CONTROL

[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,37,42,43,44] +3.3V_RUN
[21,22,23,26,32,37,42,43,44] +5V_RUN

34

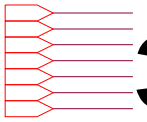


Thermal Sensor

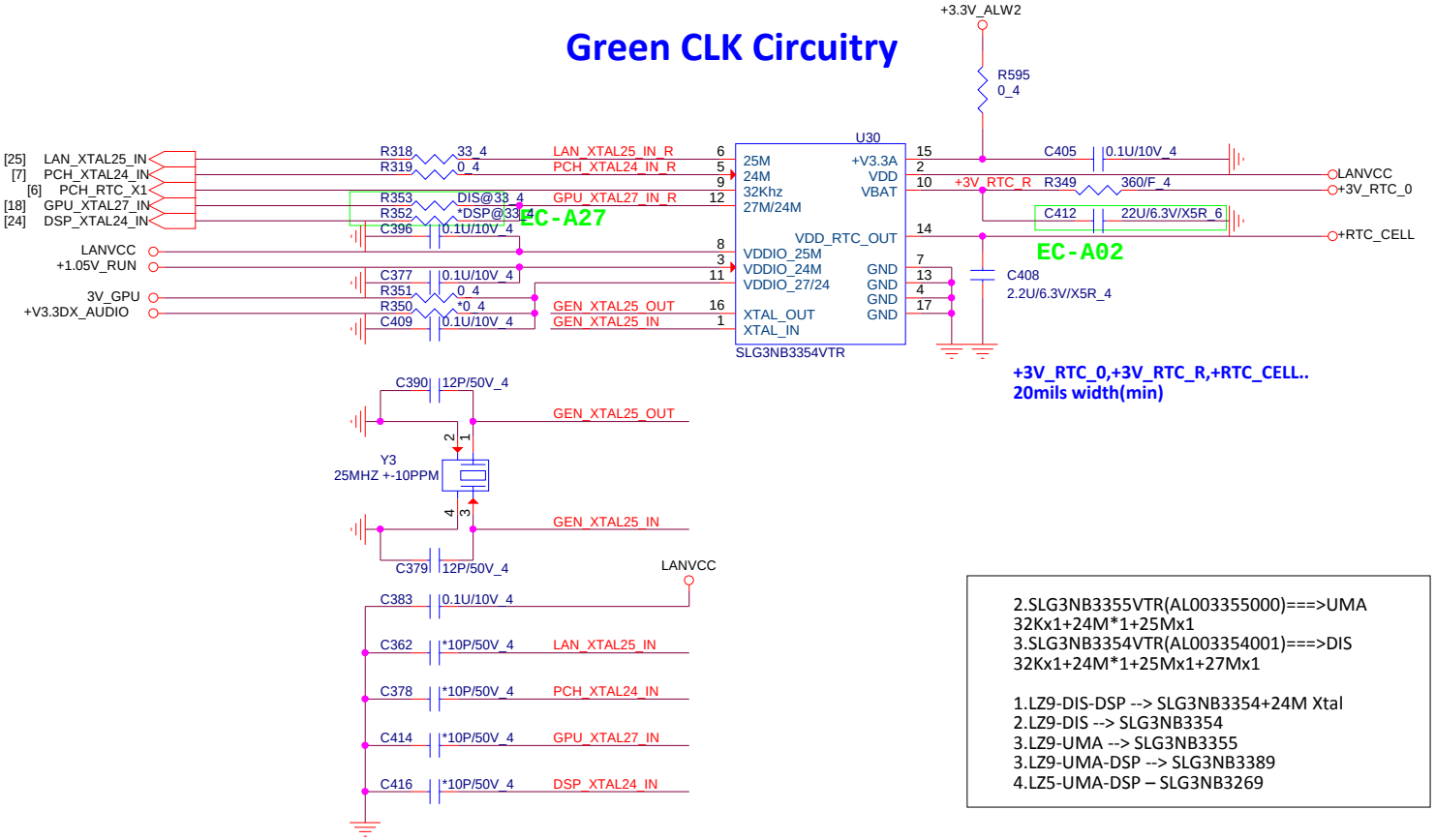


PROJECT : LZ9A Quanta Computer Inc.		
Size	Document Number FAN/Thermal	Rev 1A
Date: Thursday, January 03, 2013	Sheet 34 of 47	

[6,21,23,31,32,37,38] +3.3V_ALW2
[25,44] LANVCC
[6] +3V_RTC_0
[6,12,31] +RTC_CELL
[6,9,12,40,44,46] +1.05V_RUN
[16,17,19,45,46,47] 3V_GPU
[21,23,24] +V3.3DX_AUDIO



Green CLK Circuitry



+3V_RTC_0,+3V_RTC_R,+RTC_CELL..
20mils width(min)

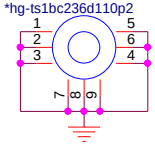
2.SLG3NB3355VTR(AL003355000)===>UMA
32Kx1+24M*1+25Mx1
3.SLG3NB3354VTR(AL003354001)===>DIS
32Kx1+24M*1+25Mx1+27Mx1

1.LZ9-DIS-DSP --> SLG3NB3354+24M Xtal
2.LZ9-DIS --> SLG3NB3354
3.LZ9-UMA --> SLG3NB3355
3.LZ9-UMA-DSP --> SLG3NB3389
4.LZ5-UMA-DSP – SLG3NB3269

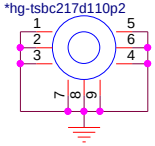
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Green Clock	1A
Date: Thursday, January 03, 2013	Sheet 35 of 47	

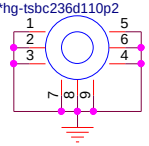
HOLE15
*hg-ts1bc236d110p2



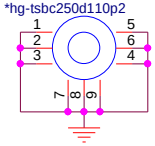
HOLE16
*hg-tsbc217d110p2



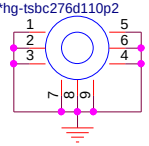
HOLE17
*hg-tsbc236d110p2



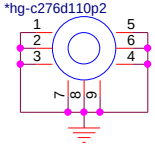
HOLE18
*hg-tsbc250d110p2



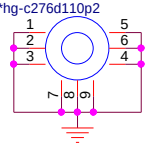
HOLE19
*hg-tsbc276d110p2



HOLE20
*hg-c276d110p2



HOLE21
*hg-c276d110p2



CPU HOLE

HOLE5
*H-C197D142P2

HOLE6
*H-C197D142P2

WLAN HOLE

HOLE13
*H-TC217BIC142D102P2

HOLE12
*H-TC217BIC142D102P2

VGA HOLE

HOLE1
*H-TC236BIC142D142N

HOLE8
*H-TC236BIC142D142N

SSD HOLE

HOLE14
*H-TC217BIC142D102P2

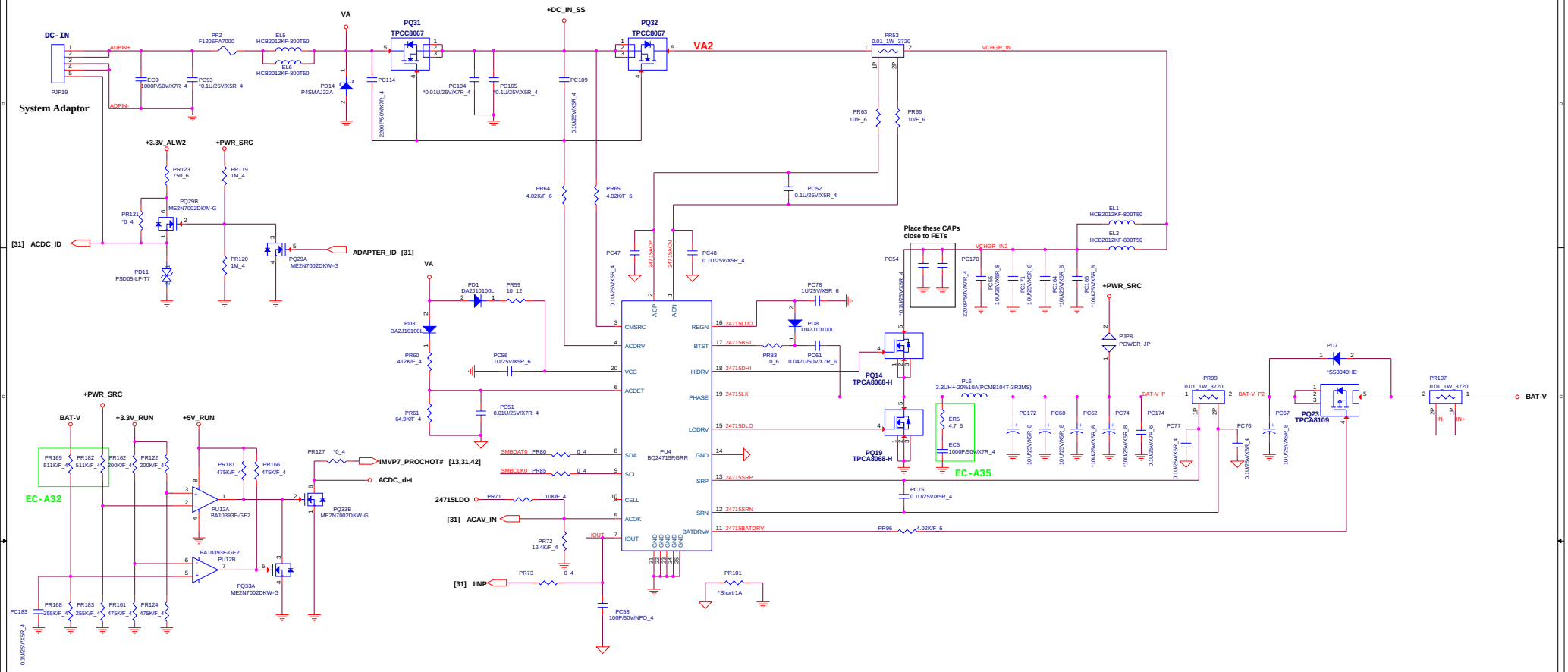
ESD

PROJECT : LZ9A

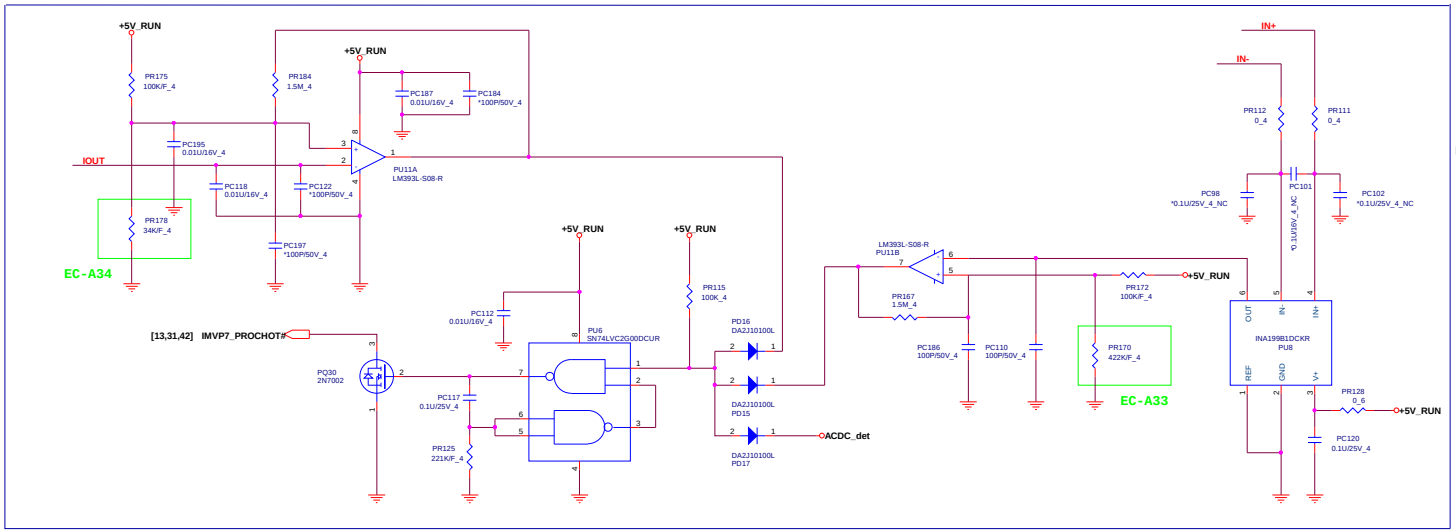
Quanta Computer Inc.

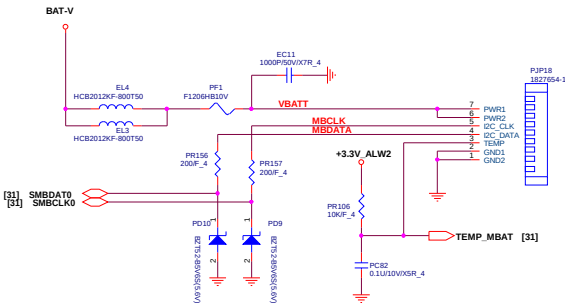
Size	Document Number	Rev
	Screw Hole/EMI	1A
Date: Thursday, January 03, 2013	Sheet 36 of 47	

[21,38,39,40,41,42,45] +PWR_SRC
[6,21,23,31,32,35,38] +3.3V_ALW2



10ms one-shot circuit





PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER (BQ24715)	1A
Date: Thursday, January 03, 2013	Sheet 37 of 47	

[21,37,39,40,41,42,45] +PWR_SRC
[4,6,8,12,17,23,25,28,30,32,43,46] +3.3V_DSW
[15,17,23,27,29,30,39,40,41,43,44,45,46] +5V_ALW
[6,21,23,31,32,35,37] +3.3V_ALW2
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[12,43,46] +15V_ALW

+5V_ALW
5 Volt +/-5%
Fsw : 400KHz
TDC : 7A
OCP : 10A

+3.3V_DSW
3.3 Volt +/-5%
Fsw : 475KHz
TDC : 8A
OCP: 11A

Place these CAPs close to FETs

Place these CAPs close to FETs

POWER_JP PJP7
POWER_JP PJP15
POWER_JP PJP16
POWER_JP PJP17

+PWR_SRC
+5V_PWR_SRC
+3.3V_PWR_SRC
+3.3V_ALW2
+5V_ALW2
+5V_ALW
+3.3V_DSW
+5V_ALW_P
+3.3V_DSW_R

PC100 *10U/25V/X5R_8
PC95 *10U/25V/X5R_8
PC189 10U/25V/X5R_8
PC94 10U/25V/X5R_8
PC96 *0.1U/25V/X5R_4
PC180 2200p/50V/X7R_4
PC101 *0.1U/25V/X5R_4
PC85 2200p/50V/X7R_4
PC182 10U/25V/X5R_8
PC98 10U/25V/X5R_8

PR116 10_8
PR92 0_4
PC100
PC107 0.1U/25V/X7R_6
4.7U/6.3V/X5R_6
PC65 4.7U/6.3V/X5R_6

PR187 *0_4
S5_ON_R
PR163 0_4
[31] S5_ON_5V
PR102 0_4
S5_ON_C [31]

PQ22 TPCC8067
PQ21 TPCC8067
PQ28 TPCC8065
PQ25 TPCC8065

PU5 TPS51285BRUKR

EN1 EN2 VIN VREG5 VREG3
DRVH1 DRVH2 VBST1 VBST2 SW1 SW2 DRVL1 DRVL2 VO1 VFB2 VFB1 VCLK CS1 CS2 PDDG
GP_AD GP_AD GP_AD GP_AD GP_AD GP_AD

5V_DH 5V_BST 5V_LX 5V_DL TPS51275_VO1 TPS51275_VFB1
3.3V_DH 3.3V_BST 3.3V_LX 3.3V_DL TPS51275_VFB2

PC87 0.1U/25V/X7R_6
PR109 2.2_6
PR110 2.2_6
PC89 0.1U/25V/X7R_6

PL7 2.2UH/8A-PCMC063T-2R2MN
PL8 2.2UH/8A-PCMC063T-2R2MN

ER7 *4.7_6
EC12 *1000P/50V_4
ER6 4.7_6
EC13 1000P/50V_4

EC-A36
EC-A37

PC79 4.7U/6.3V/X5R_6
PC84 0.1U/10V/X5R_4
PC193 *100U/6.3V/ESR45_3528
PC177 220U/6.3V/ESR25_7343
PR93 30K/F_4
PR94 19.6K/F_4

PC192 220U/6.3V_6.3*4.2
PC175 *100U/6.3V/ESR45_3528
PC99 4.7U/6.3V/X5R_6
PC97 0.1U/10V/X5R_4
PR91 13K/F_4
PR90 20K/F_4

Power-02

HWPG [31,39,40,41]
PR104 0_4
RV3 *AVLC 5S 02 (5.5V,100)_4

PR95 16.2K/F_4
PR89 21.5K/F_4

VCLK

+5V_ALW_P
PC59 0.1U/25V/X5R_4
PR105 0_6
PD6 BAT54S-7-F
PC60 0.1U/25V/X5R_4
PC44 0.1U/25V/X5R_4
PD5 BAT54S-7-F
PR56 22_8
+15V_ALW
+15V_ALWP
PC42 0.1U/25V/X5R_4

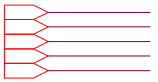
+3.3V_ALW2
PR160 *39K/F_4
S5_ON_R

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	3V/5V (TPS51285)	1A

Date: Thursday, January 03, 2013 Sheet 38 of 47

[21,37,38,40,41,42,45] +PWR_SRC
[9,14,15,44] +V_VDDQ_VR
[15,17,23,27,29,30,38,40,41,43,44,45,46] +5V_ALW
[14,15,44] +0.675V_DDR_VTT
[15] +DDR_VTTREF



39

+V_VDDQ_VR
1.35 Volt +/-5%
Fsw : 400KHz
TDC : 7A
OCP : 12A

+0.675V_DDR_VTT
TDC : 1A

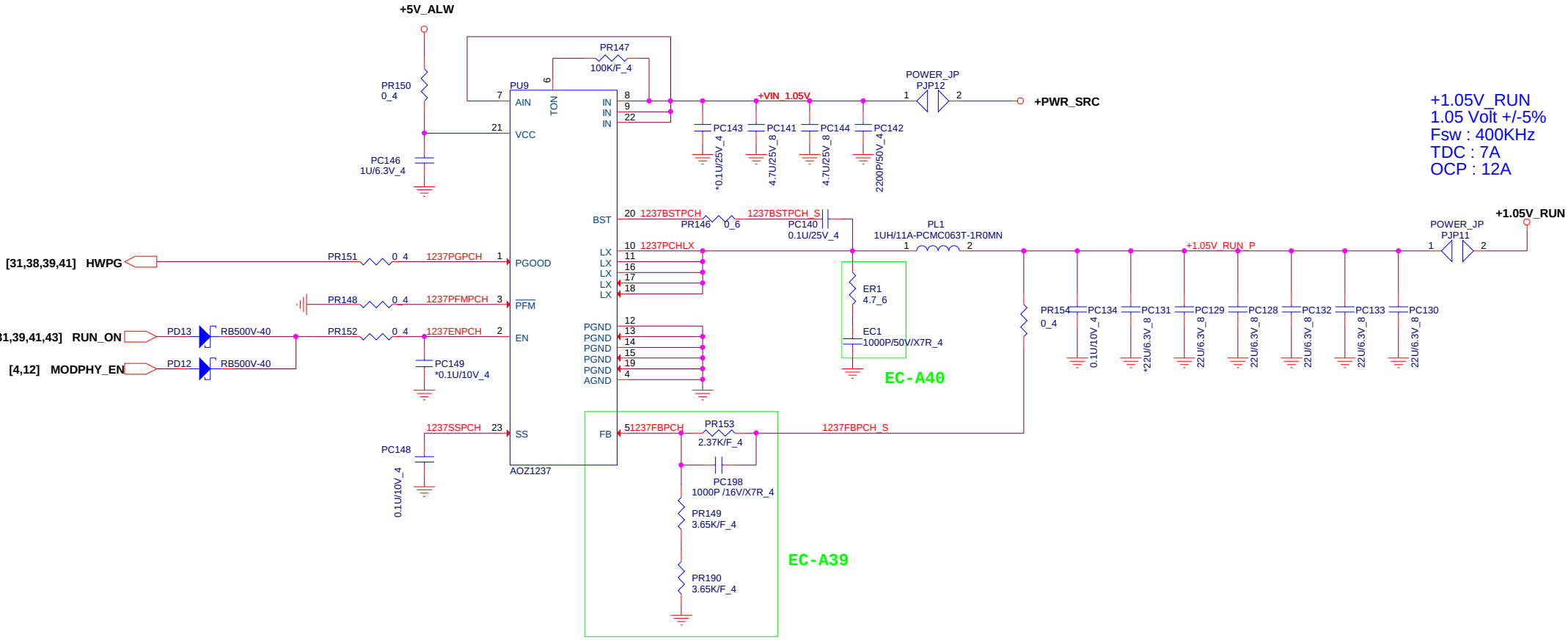
EC-A38

PU10 AOZ1237
PU7 TPS51206DSQR

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	1.35V_DDR/0.675 (AOZ1237)	1A
Date: Thursday, January 03, 2013	Sheet 39 of 47	

[21,37,38,39,41,42,45] +PWR_SRC
[6,9,12,35,44,46] +1.05V_RUN
[15,17,23,27,29,30,38,39,41,43,44,45,46] +5V_ALW

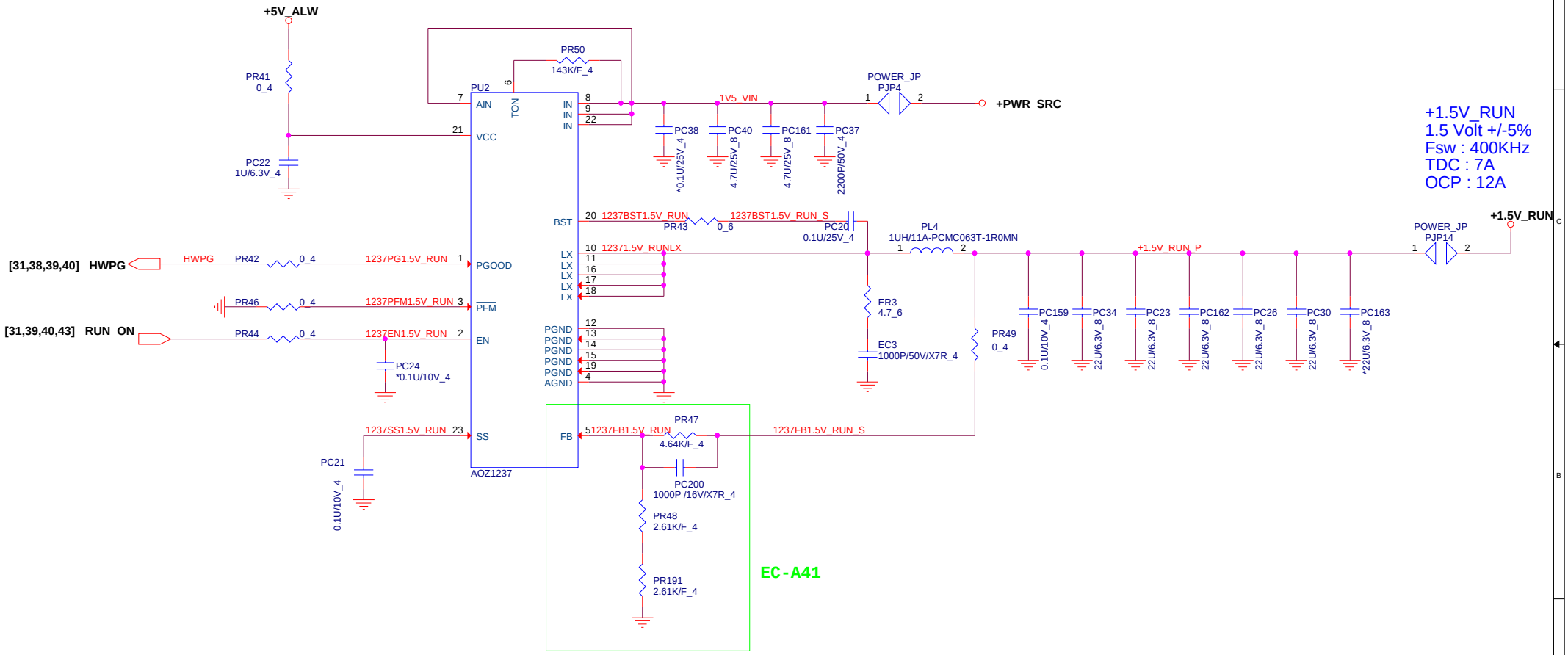


PROJECT : LZ9A

Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V_RUN (AOZ1237)	1A
Date: Thursday, January 03, 2013	Sheet 40 of 47	

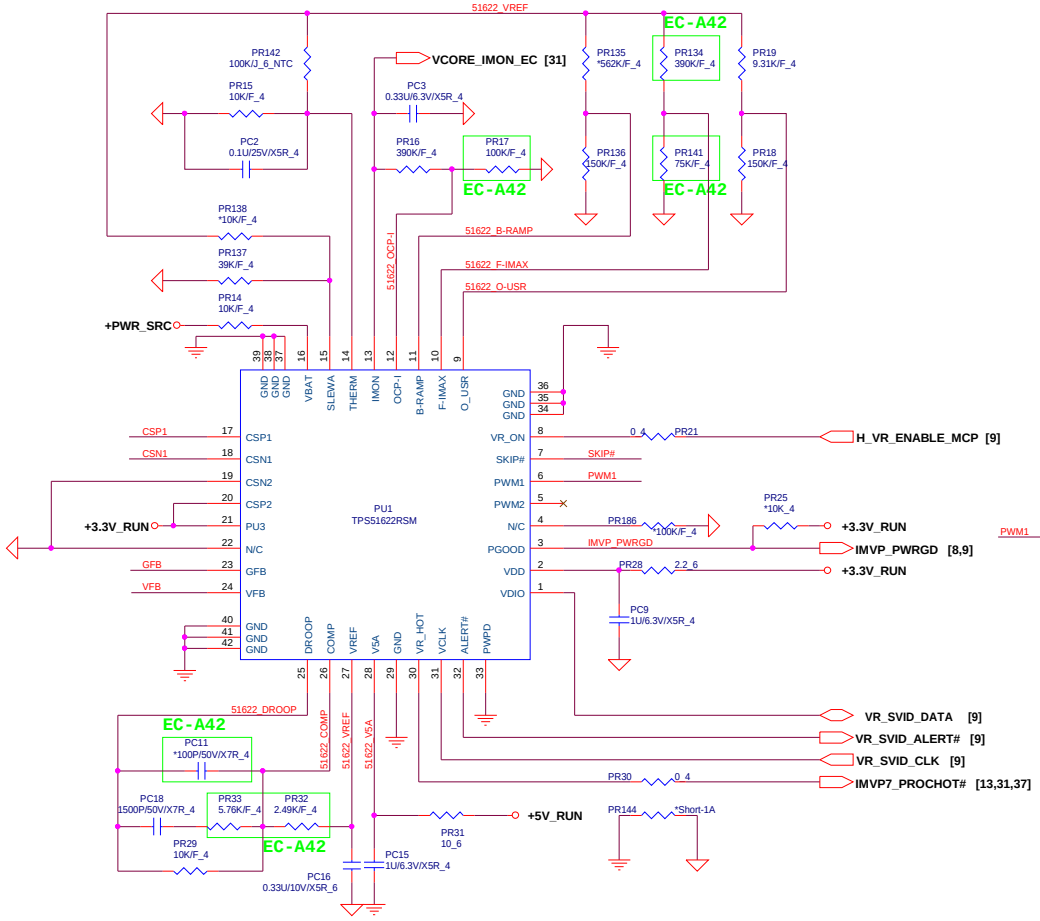
[21,37,38,39,40,42,45] +PWR_SRC
[12,23,28,44,46] +1.5V_RUN
[15,17,23,27,29,30,38,39,40,43,44,45,46] +5V_ALW

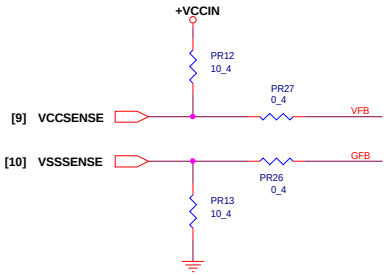


PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: +1.5V_RUN (AOZ1237)	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 41 of 47	

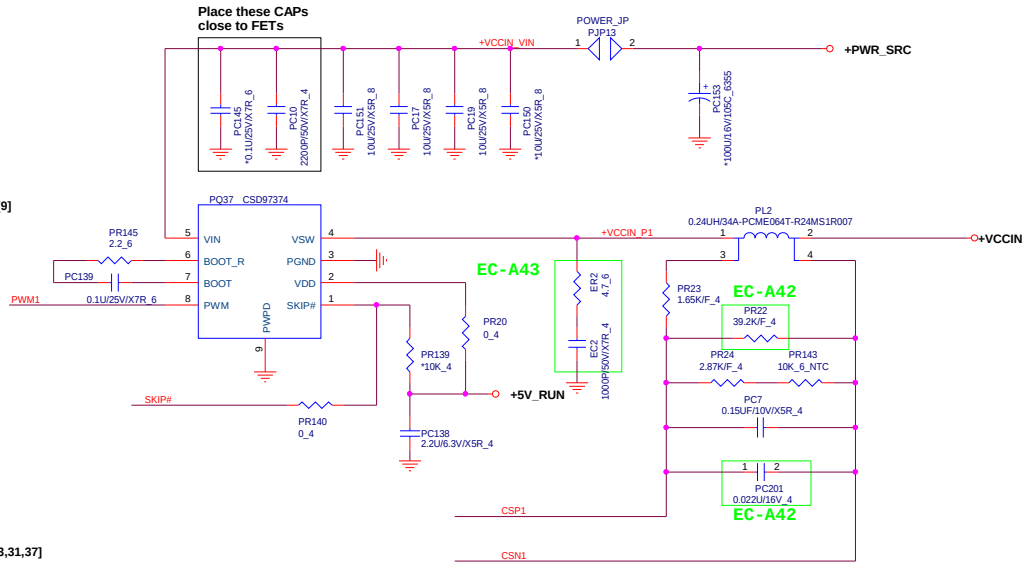
[21,37,38,39,40,41,45] [9] [15,17,23,27,29,30,38,39,40,41,43,44,45,46] [6,9,12,35,40,44,46] [2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,43,44] [21,22,23,26,32,34,37,43,44]

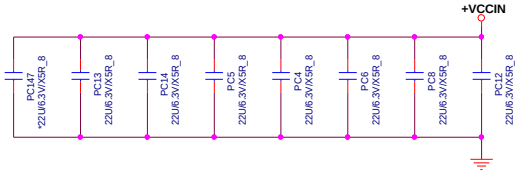
+PWR_SRC
+VCCIN
+5V_ALW
+1.05V_RUN
+3.3V_RUN
+5V_RUN





Place these CAPs close to FETs



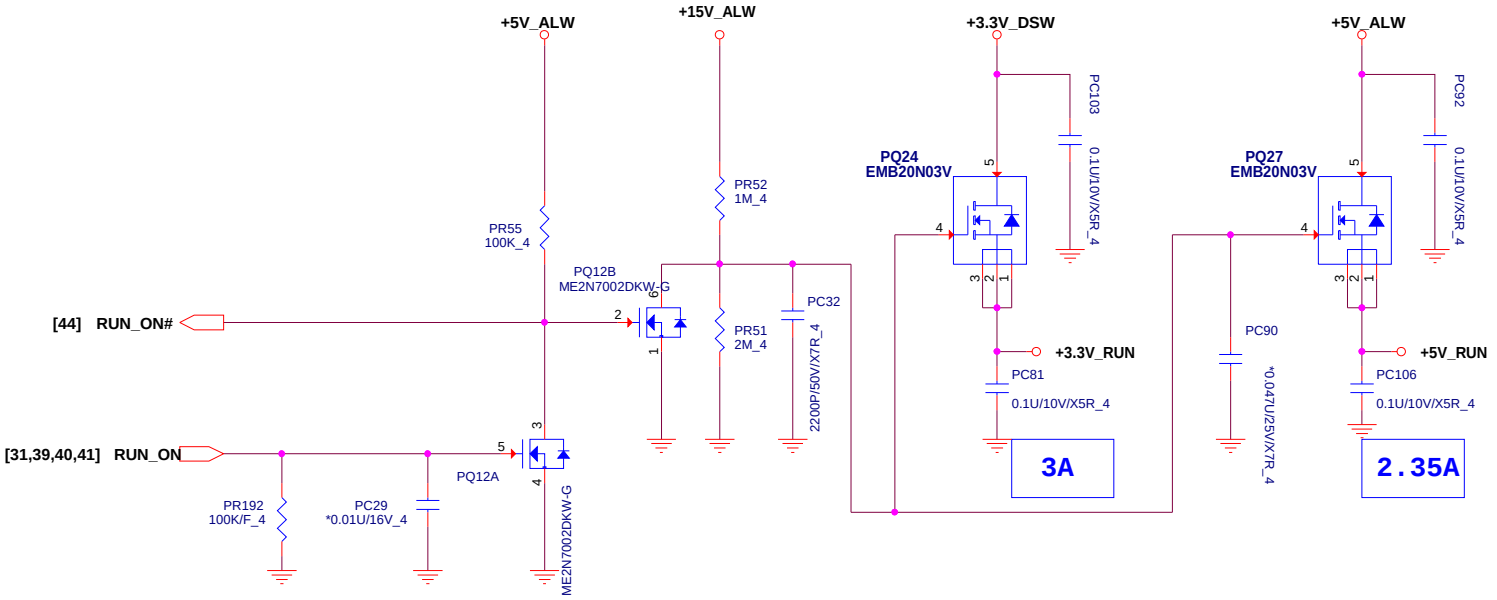



```
Icc_Max=32A
I_TDC=14A
I_Dynamic=27A
V_Operate=1.6V~1.8V
DC_LL=2m
AC_LL=9m
AC_LL_VOS=9.4m
VBOOT=1.7V
```

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE (TPS51622RSML)	1A
Date: Thursday, January 03, 2013	Sheet 42 of 47	

[15,17,23,27,29,30,38,39,40,41,44,45,46] +5V_ALW
[12,38,46] +15V_ALW
[21,22,23,26,32,34,37,42,44] +5V_RUN
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,44] +3.3V_RUN
[4,6,8,12,17,23,25,28,30,32,38,46] +3.3V_DSW
[6,9,12,35,40,44,46] +1.05V_RUN

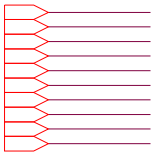


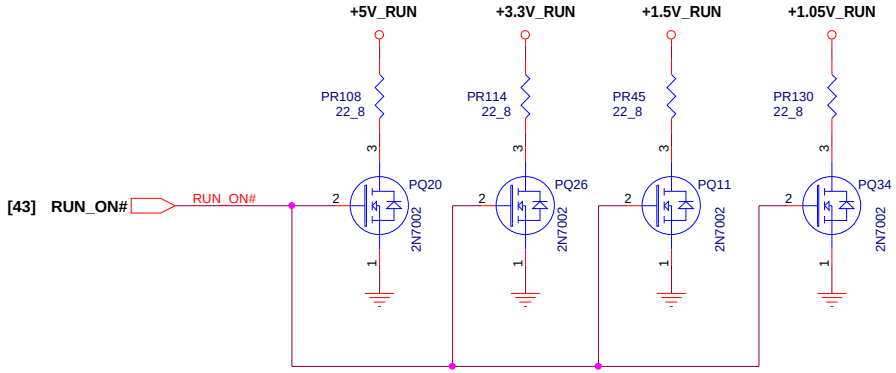
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Load Switch	1A
Date: Thursday, January 03, 2013	Sheet 43 of 47	

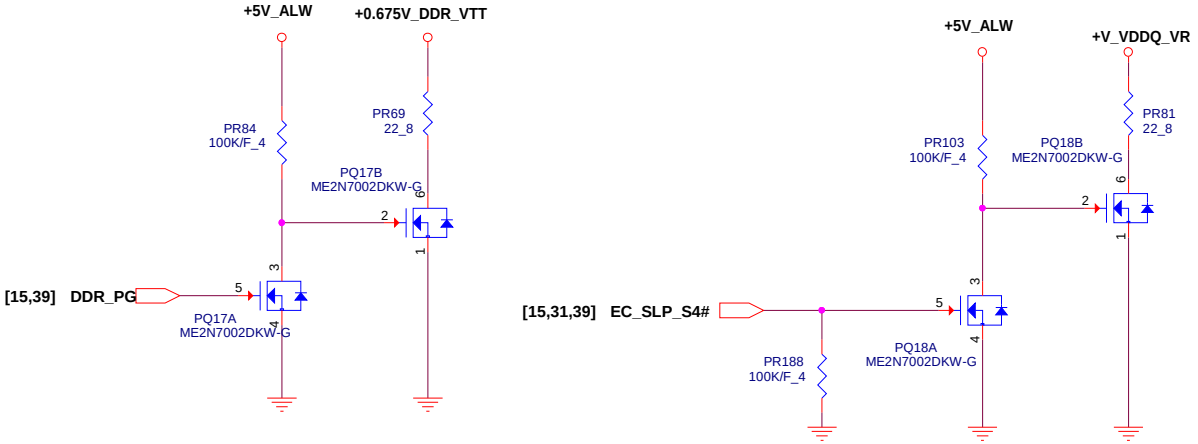
DISCHARGE

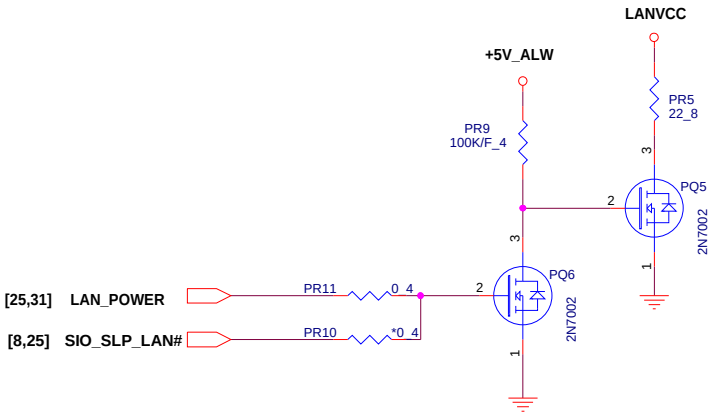
[15,17,23,27,29,30,38,39,40,41,43,45,46] +5V_ALW
[21,22,23,26,32,34,37,42,43] +5V_RUN
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43] +3.3V_RUN
[12,23,28,41,46] +1.5V_RUN
[6,9,12,35,40,46] +1.05V_RUN
[14,15,39] +0.675V_DDR_VTT
[4,5,6,7,8,12,15] +3.3V_DEEP_SUS
[9,14,15,39] +V_VDDQ_VR
[25,35] LANVCC
[12,38,43,46] +15V_ALW





LANVCC





PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	
Date: Thursday, January 03, 2013	Sheet 44 of 47	

[21,37,38,39,40,41,42] +PWR_SRC
[16,47] VGPU_CORE
[15,17,23,27,29,30,38,39,40,41,43,44,46] +5V_ALW
[16,17,19,35,46,47] 3V_GPU

[16,17,31,46] GFXON
PR74 0_4 8812EN
PC53 *0.022U/16V/X7R_4

+5V_ALW
PR57 1/F_6
PC43 1U/6.3V_4

RT8812A_1_VIN
PC73 0.01U/25V/X7R_4
PR100 1/F_6
PR88 499K/F_4

PU3 RT8812A
8812PVCC
8812TON TON
8812EN EN
8812PSI PSI
8812VID VID
8812VREF VREF
8812REFADJ REFADJ
8812REFIN REFIN
SS
GND
BOOT1 8812BOOST1
UGATE1 8812UGATE1
PHASE1 8812PHASE1
LGATE1 8812LGATE1
BOOT2 8812BOOST2
UGATE2 8812UGATE2
PHASE2 8812PHASE2
LGATE2 8812LGATE2
PG 8812PG
VSNS 8812VSNS
RGND 8812RGND

[19] PSI_GPU#
[19] PWM-VID
PR76 0_4
PR79 0_4
PC64 *2200P/50V_4
PC71 0.1U/10V/X5R_4
PR87 20K/F_4
PR82 20K/F_4
PC72 2700P/50V/X7R_4
PR98 2.15K/F_4
PC70 47P/50V/NPO_4
PC63 22P/50V/NPO_4
PR86 18K/F_4
PR97 0_4

8812BOOST1
PR67 2.2_6
PC45 0.22U/25V/X5R_6
8812UGATE1
PQ15 TPCA8068-H
8812PHASE1
PL5 0.36UH +-20% 30A(ETQP4LR36WFC)
8812LGATE1
PQ13 TPCA8059-H
PR58 11.5K/F_4
EC-A45
ER4 *4.7_6
EC4 *1000P/50V/X7R_4
RT8812A_1_VIN
PC168 *0.1U/25V_6
PC49 2200P/50V_4
PC167 4.7U/25V/X5R_8
PC169 4.7U/25V/X5R_8
PC50 *4.7U/25V/X5R_8
POWER_JP PJP5
+PWR_SRC
VGPU_CORE_P
PC158 330U/2.5V_6.3*4.2ESR17
PC166 330U/2.5V_6.3*4.2ESR17
PC27 10U/6.3V_6
PC31 0.1U/10V_4
POWER_JP PJP2
POWER_JP PJP1
VGPU_CORE

VGPU_CORE
PEAK :30A
OCP :38A

8812BOOST2
PR68 2.2_6
PC46 0.22U/25V/X5R_6
8812UGATE2
PQ10 TPCA8068-H
8812PHASE2
PL3 0.36UH +-20% 30A(ETQP4LR36WFC)
8812LGATE2
PQ9 TPCA8059-H
ER9 *4.7_6
EC22 *1000P/50V/X7R_4
RT8812A_2_VIN
PC28 *0.1U/25V_6
PC36 2200P/50V_4
PC33 4.7U/25V/X5R_8
PC41 4.7U/25V/X5R_8
PC39 *4.7U/25V/X5R_8
POWER_JP PJP3
+PWR_SRC
PC160 330U/2.5V_6.3*4.2ESR17
PC25 10U/6.3V_6
PC35 0.1U/10V_4

3V_GPU
PR70 1.91K/F_4
PR75 0_4
8812PG
NVVDD_PG [46]

VGPU_CORE
VGPU_CORE_P
PC57 *47P/50V/NPO_4
PR39 *100/F_4
PR36 100/F_4
8812VSNS
PR40 0_4
PC66 *47P/50V/NPO_4
8812RGND
PR37 0_4
PC69 *47P/50V/NPO_4
PR38 100/F_4
GPUCORE_VCCSENSE [16]
GPUCORE_VSSSENSE [16]

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Quanta Computer Inc.
Size
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GFX_CORE (RT8812A)
Rev
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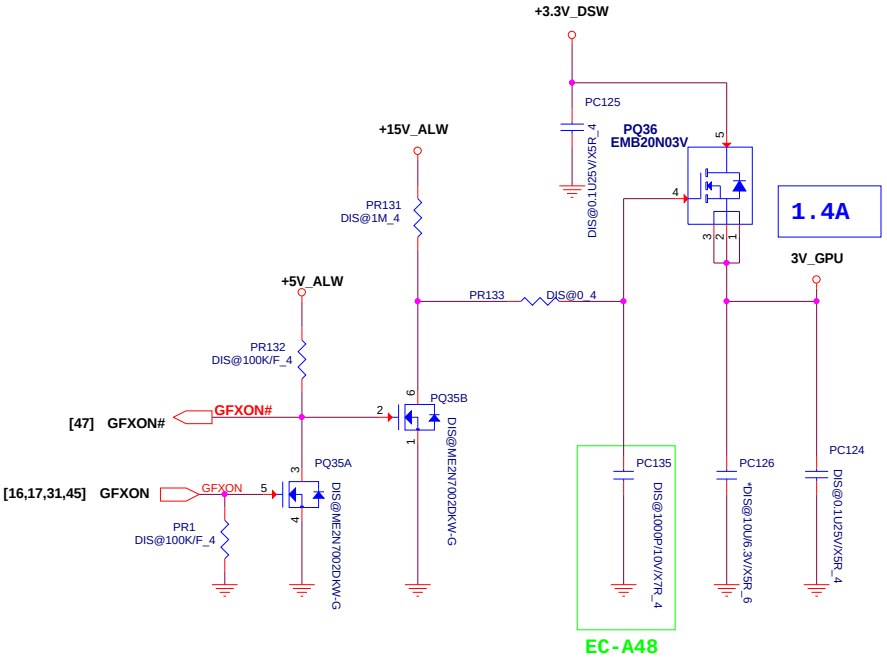
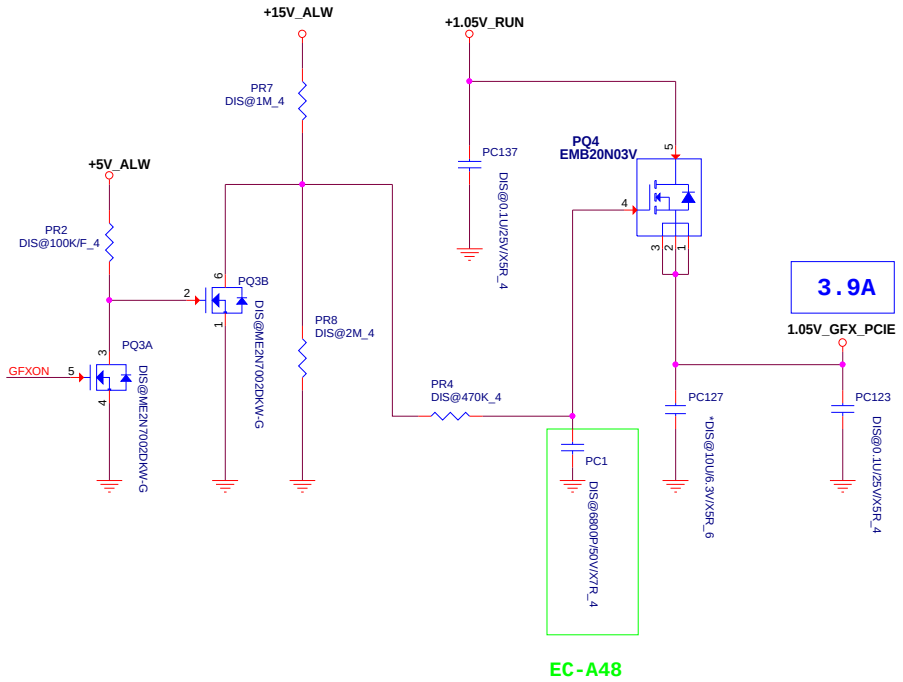
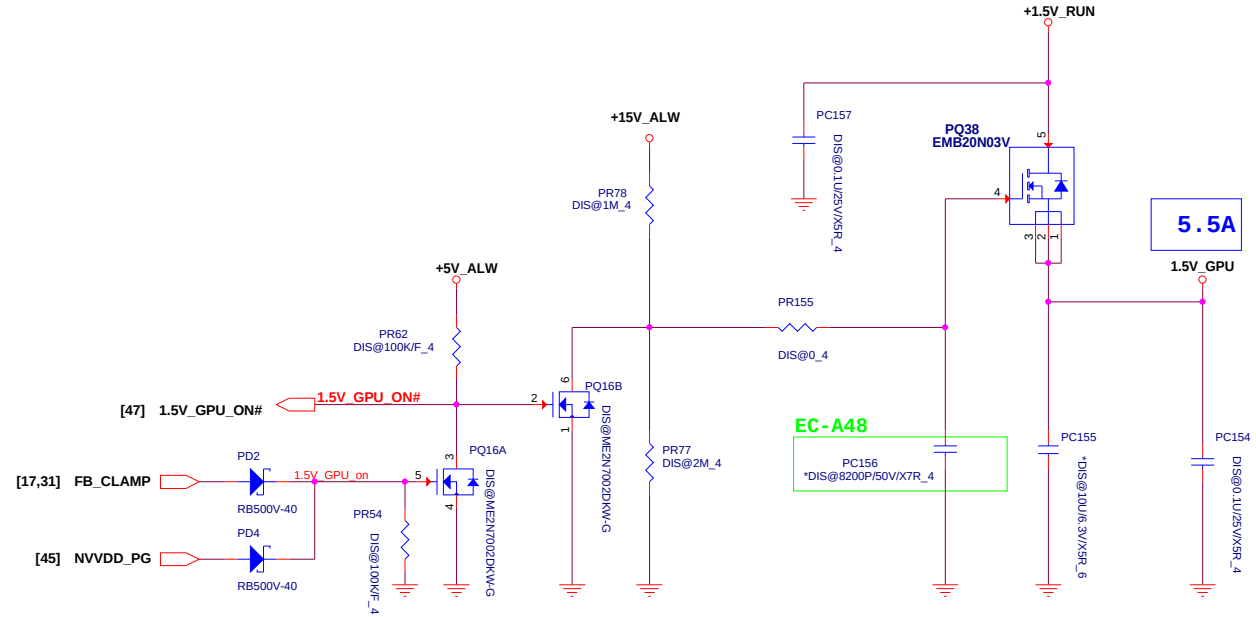




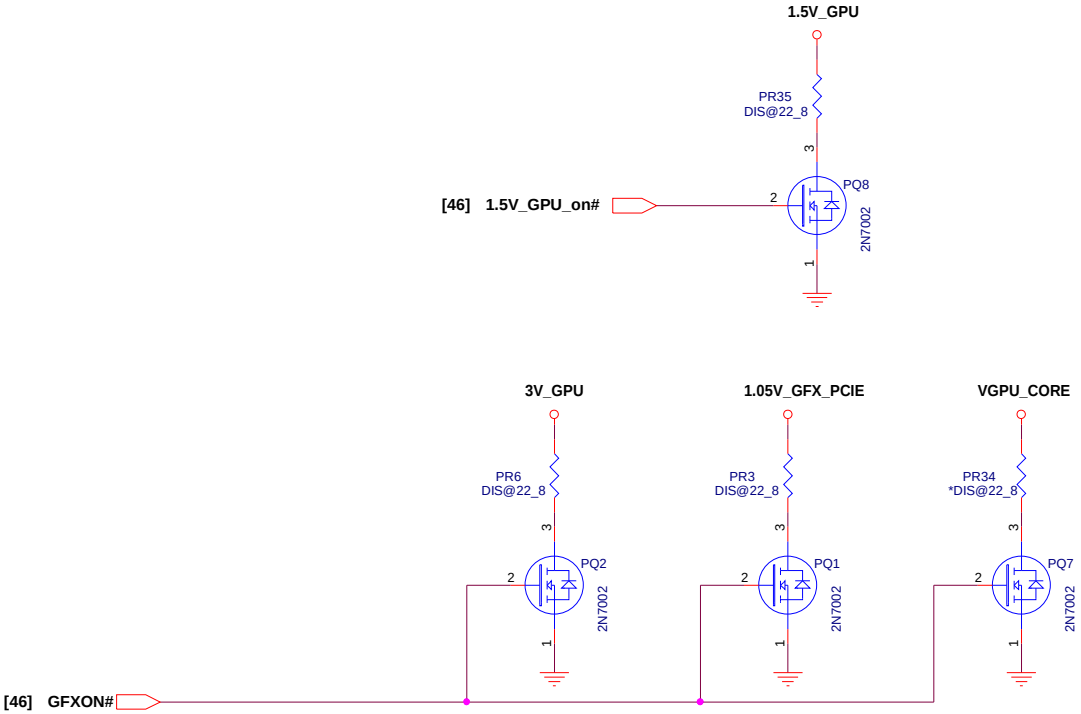


Quanta Computer Inc.	PROJECT : LZ9A	
Size	Document Number: DIS_Load Switch	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 46 of 47	

DISCHARGE

[15,17,23,27,29,30,38,39,40,41,43,44,45,46]	+5V_ALW
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44]	+3.3V_RUN
[12,23,28,41,44,46]	+1.5V_RUN
[6,9,12,35,40,44,46]	+1.05V_RUN
[14,15,39,44]	+0.675V_DDR_VTT
[9,14,15,39,44]	+V_VDDQ_VR
[25,35,44]	LANVCC
[12,38,43,46]	+15V_ALW

47



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Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	
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