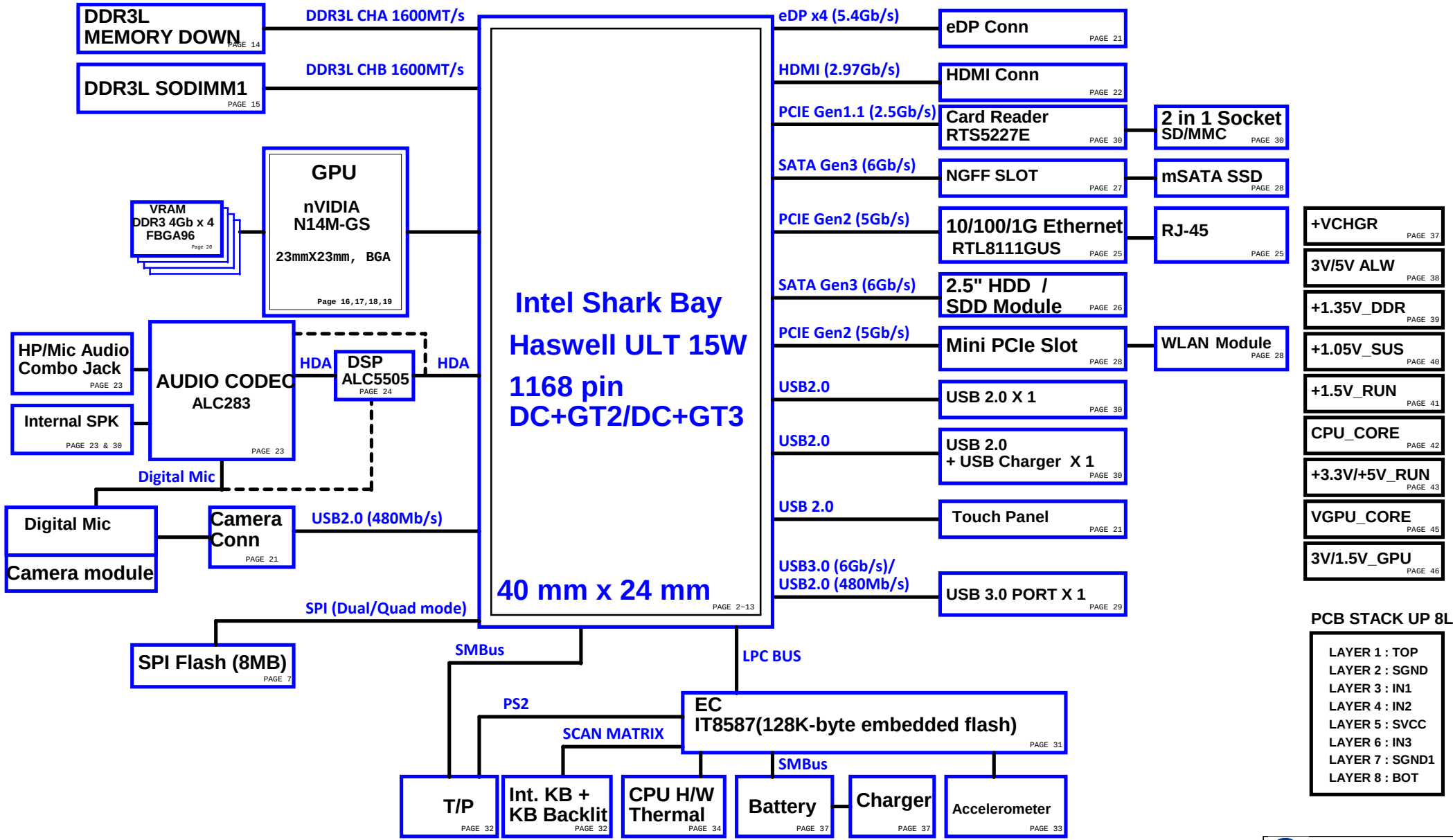
LZ9A 14" OPTIMUS
INTEL SHARK BAY ULT ONE CHIP PLATFORM



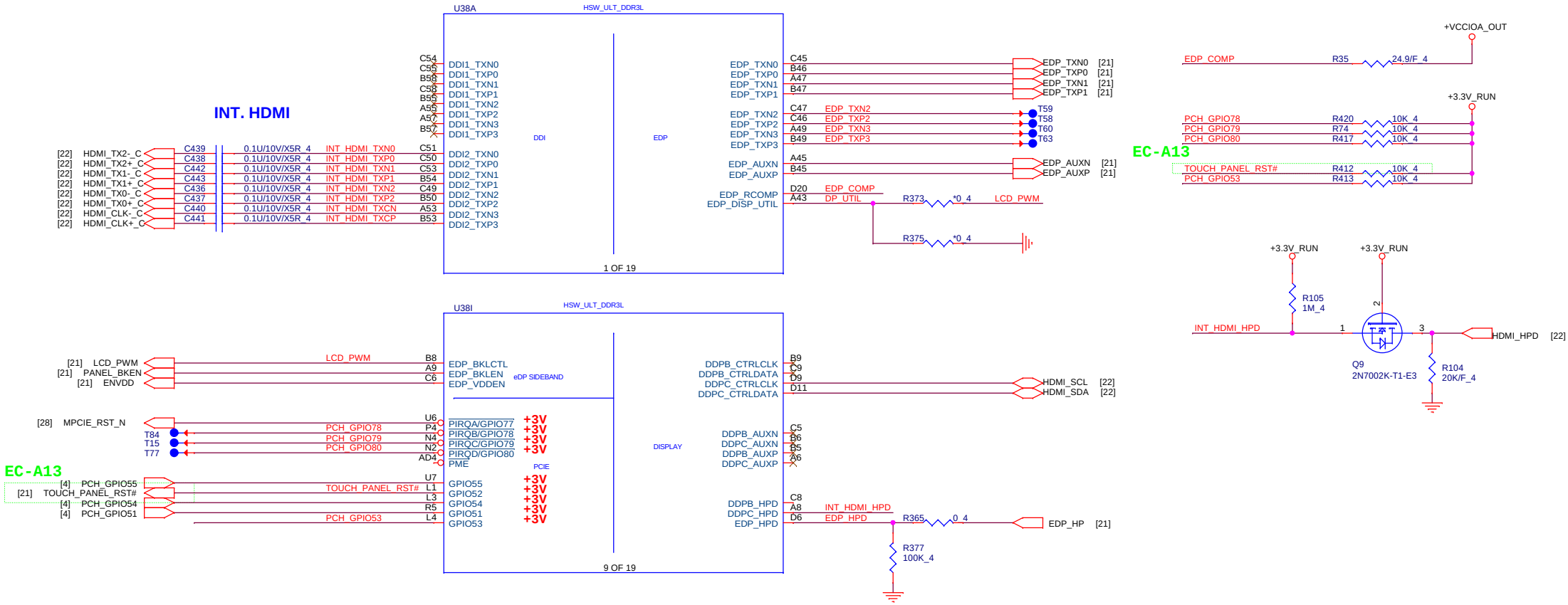
PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

PROJECT : LZ9A
Quanta Computer Inc.
System Block Diagram
Rev 1A
Thursday, January 03, 2013
Sheet 1 of 47

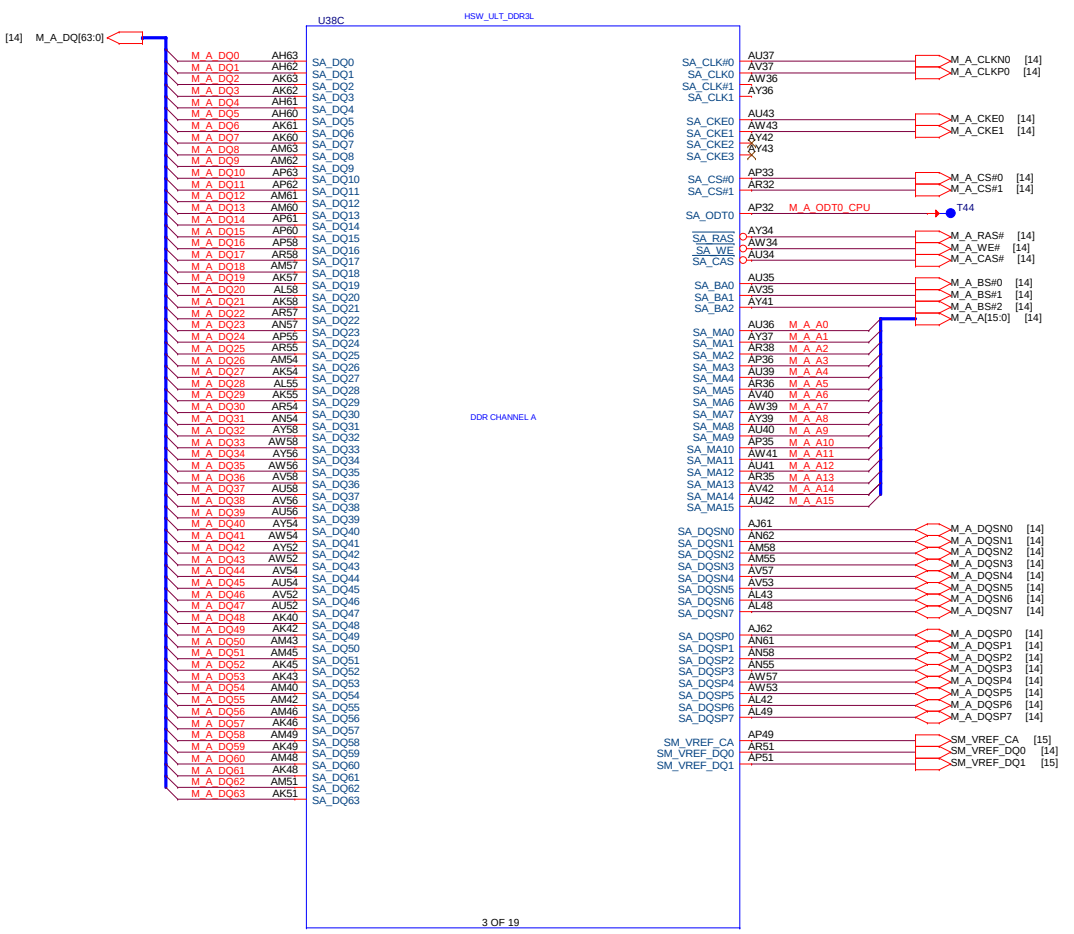
[9] +VCCIOA_OUT
[4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN

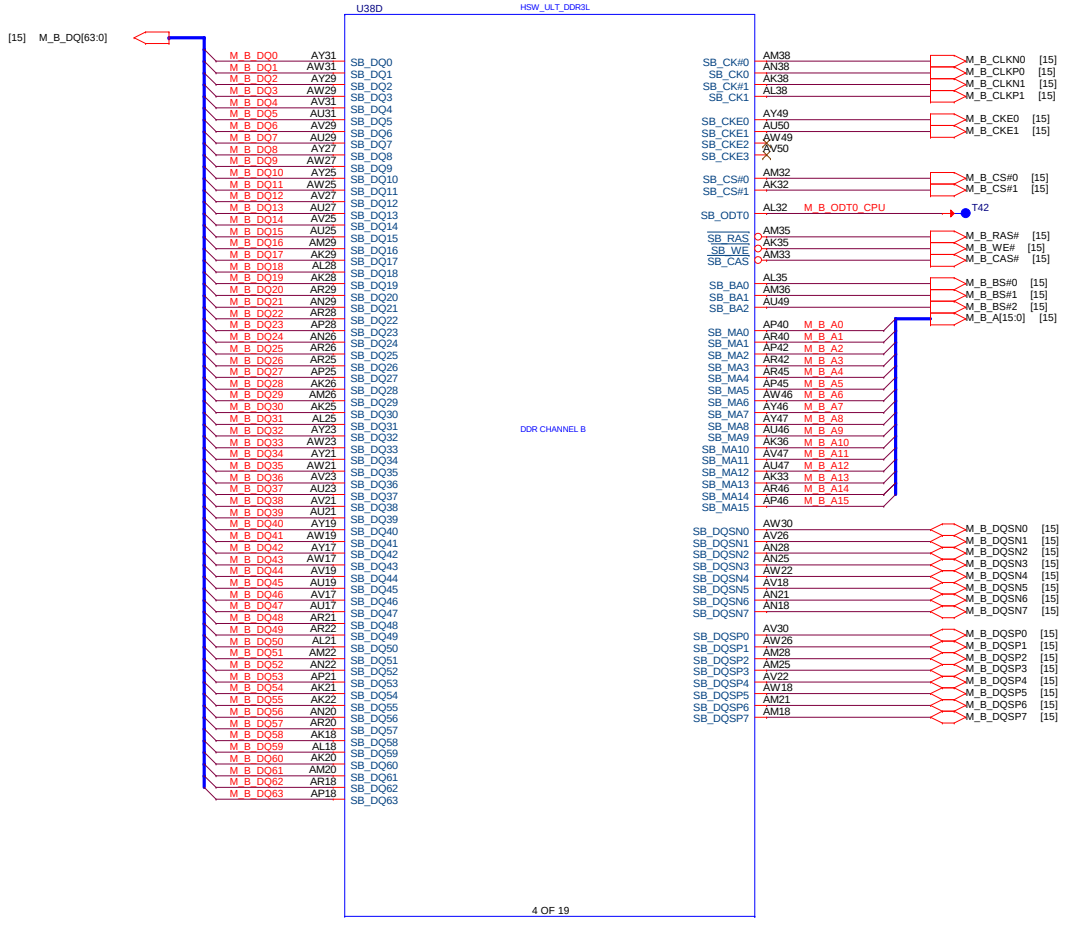
Haswell ULT (DISPLAY)



PROJECT :	LZ9A
Quanta Computer Inc.	
Size	Document Number: Haswell ULT 1/12 — Rev: 1A
Date: Thursday, January 03, 2013	Sheet 2 of 47

Haswell ULT (DDR3L)





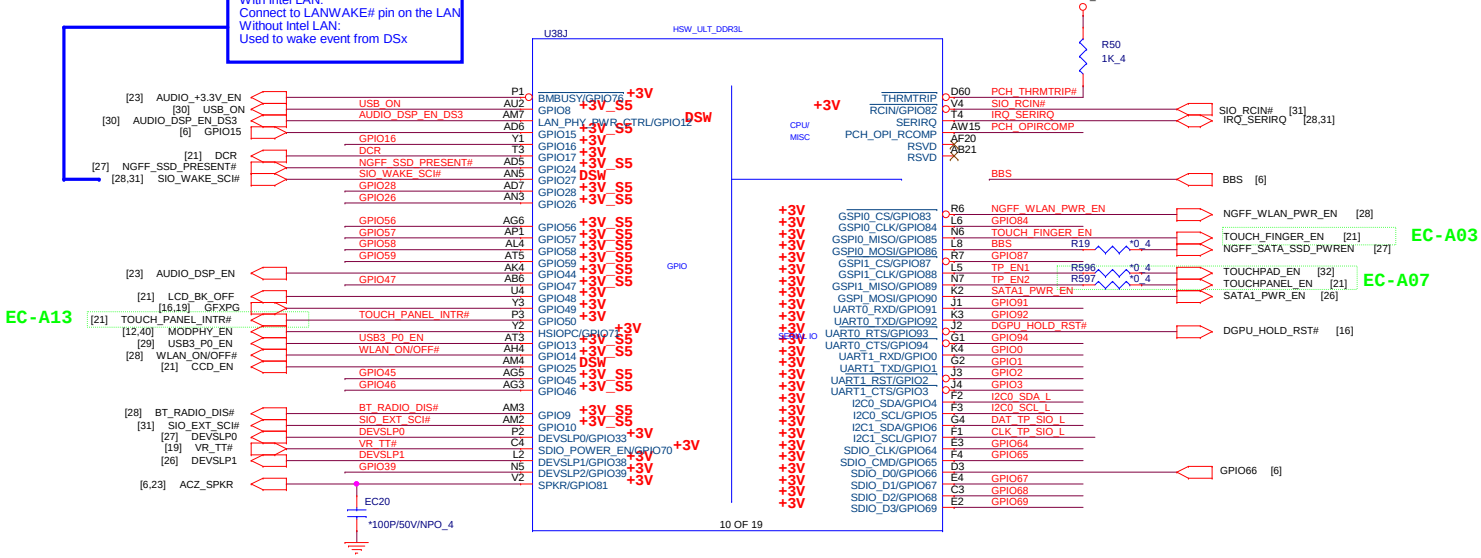
PROJECT : LZ9A

Quanta Computer Inc.

Size	Document Number	Rev
	Haswell ULT 2/12	1A
Date: Thursday, January 03, 2013	Sheet 3 of 47	

Hasswell ULT(GPIO,LPIO,MISC)

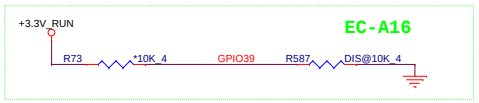
GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx



Thunderbolt ID	GPIO84
Supported	0
Not Supported	1

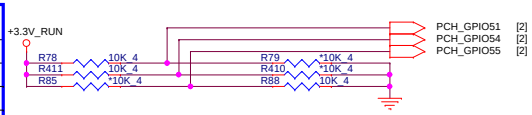
Audio DSP ID	GPIO47
Supported	0
Not Supported	1

DGPU SELECT	GPIO39
Supported	0
Not Supported	1



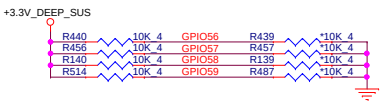
Model ID	GPIO45	GPIO46
LZ5-UMA	0	0
LZ9-UMA	0	1
LZ9A-DIS	1	0
LZA	1	1

Board ID	GPIO51	GPIO54	GPIO55
SDV	1	1	1
SIV	1	1	0
SIT			
SVT			



DDR3L Memory Down ID Table

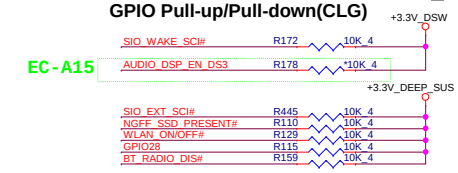
Vendor	Description	Size	Quanta P/N	GPIO[56,57,58,59]
Default				1111
Samsung	K4B8G1646B-MYK0 (B/4Gb/35nm/DDP)	8Gb x 16	AKD5FGET500	1110
Micron	MT41K512M16TNA-125:E(V80A/4Gb/30nm/DDP)	8Gb x 16	AKD5FGSTL00	1101
ELPIDA	EDJ8416E6MB-GN-F(F/4Gb/30nm/DDP)	8Gb x 16	AKD5FGST402	1100
SK hynix		8Gb x 16		XXXX
Samsung	K4B4G1646B-HYK0(B/4Gb/35nm)	4Gb x 16	AKD5PGET500	1011
Micron	MT41K256M16HA-125:E(V80A/4Gb/30nm)	4Gb x 16	AKD5JGSTL02	1010
ELPIDA	EDJ4216EFBG-GN-F(F/4Gb/30nm)	4Gb x 16	AKD5JGST403	1001
SK hynix	H5TC4G63AFR-PBA(D/4Gb/29nm)	4Gb x 16	AKD5JGETW00	1000

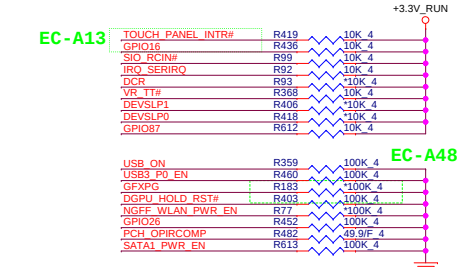


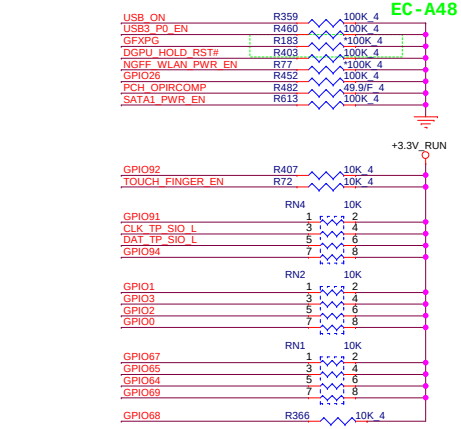
[9,13] +V1.05S_VCCST
[5,6,7,8,12,15] +3.3V_DEEP_SUS
[2,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[6,8,12,17,23,25,28,30,32,38,43,46] +3.3V_DSW

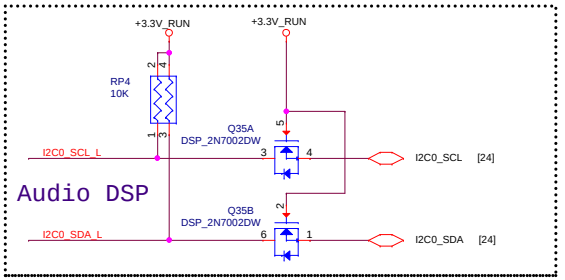
4

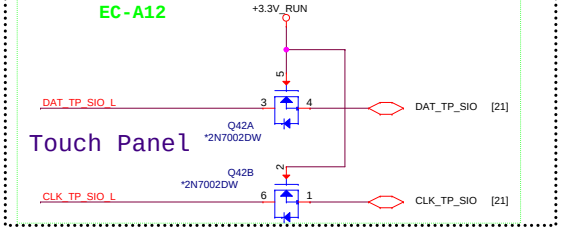
GPIO Pull-up/Pull-down(CLG)











PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Haswell ULT 3/12	1A
Date: Thursday, January 03, 2013	Sheet 4 of 47	

[4,6,7,8,12,15] +3.3V_DEEP_SUS
[12] +V1.05S_AUSB3PLL

5

Haswell ULT (PCIE,USB)

U38K — HSW_ULT_DDR3L

VGA

[16] PEG_RXN0				F10	PERN5_L0	
[16] PEG_RXP0				E10	PERP5_L0	
[16] PEG_TXN0	C447	0.1U/10V/X5R_4	PEG_TXN0_C	C23	PETN5_L0	
[16] PEG_TXP0	C444	0.1U/10V/X5R_4	PEG_TXP0_C	C22	PETP5_L0	
[16] PEG_RXN1				F8	PERN5_L1	
[16] PEG_RXP1				E8	PERP5_L1	
[16] PEG_TXN1	C425	0.1U/10V/X5R_4	PEG_TXN1_C	B23	PETN5_L1	
[16] PEG_TXP1	C424	0.1U/10V/X5R_4	PEG_TXP1_C	A23	PETP5_L1	
[16] PEG_RXN2				H10	PERN5_L2	
[16] PEG_RXP2				G10	PERP5_L2	
[16] PEG_TXN2	C422	0.1U/10V/X5R_4	PEG_TXN2_C	B21	PETN5_L2	
[16] PEG_TXP2	C423	0.1U/10V/X5R_4	PEG_TXP2_C	C21	PETP5_L2	
[16] PEG_RXN3				E6	PERN5_L3	
[16] PEG_RXP3				F6	PERP5_L3	
[16] PEG_TXN3	C446	0.1U/10V/X5R_4	PEG_TXN3_C	B22	PETN5_L3	
[16] PEG_TXP3	C445	0.1U/10V/X5R_4	PEG_TXP3_C	A21	PETP5_L3	

WiFi/BT

[28] PCIE_RXN3				G11	PERN3	
[28] PCIE_RXP3				F11	PERP3	
[28] PCIE_TXN3	C451	0.1U/10V/X5R_4	PCIE_TXN3_C	C29	PETN3	
[28] PCIE_TXP3	C452	0.1U/10V/X5R_4	PCIE_TXP3_C	B30	PETP3	

Card Reader

[30] PCIE_RXN4				F13	PERN4	
[30] PCIE_RXP4				G13	PERP4	
[30] PCIE_TXN4	C450	0.1U/10V/X5R_4	PCIE_TXN4_C	B29	PETN4	
[30] PCIE_TXP4	C449	0.1U/10V/X5R_4	PCIE_TXP4_C	A29	PETP4	

LAN (Select PCIE)

[25] PCIE_RXN5				G17	PERN1/USB3RN3	
[25] PCIE_RXP5				F17	PERP1/USB3RP3	
[25] PCIE_TXN5	C427	0.1U/10V/X5R_4	PCIE_TXN5_C	C30	PETN1/USB3TN3	
[25] PCIE_TXP5	C428	0.1U/10V/X5R_4	PCIE_TXP5_C	C31	PETP1/USB3TP3	
				F15	PERN2/USB3RN4	
				G15	PERP2/USB3RP4	
				B31	PETN2/USB3TN4	
				A31	PETP2/USB3TP4	

PCIE

+V1.05S_AUSB3PLL

R25	3K/F_4	PCIE_RCOMP	E15	RSVD	
R32	0_4	PCIE_IREF	E13	RSVD	
			A27	PCIE_RCOMP	
			B27	PCIE_IREF	

USB

USB2N0	AN8			USB-_TPanel [21]	Touch Panel
USB2P0	AM8			USB+_TPanel [21]	
USB2N1	AR7			USBP1- [29]	USB3.0 Port 1 (CN7)
USB2P1	AT7			USBP1+ [29]	
USB2N2	AR8			USBP2- [30]	USB2.0 Port 1
USB2P2	AP8			USBP2+ [30]	
USB2N3	AR10			USBP3- [30]	USB2.0 Port 2
USB2P3	AT10			USBP3+ [30]	
USB2N4	AM15			USBP4- [21]	CAMERA
USB2P4	AL15			USBP4+ [21]	
USB2N5	AM13			USBP5- [28]	WLAN / BT NGFF
USB2P5	AN13			USBP5+ [28]	
USB2N6	AP11				
USB2P6	AN11				
USB2N7	AR13				
USB2P7	AP13				

USB3RN1	G20			USB30_RX1- [29]	USB3.0 Port 1 (CN7)
USB3RP1	H20			USB30_RX1+ [29]	
USB3TN1	C33			USB30_TX1- [29]	
USB3TP1	B34			USB30_TX1+ [29]	
USB3RN2	E18				
USB3RP2	F18				
USB3TN2	B33				
USB3TP2	A33				

USBRBIAS	AJ10	USB_BIAS	R125	22.6/F_4	
USBRBIAS	AJ11				
RSVD	AN10	USBPLLMON_N	R165	49.9/F_4	
RSVD	AM10	USBPLLMON_P	R164	49.9/F_4	

+3V_S5	OC0/GPIO40	AL3	USB_OC0#	USB_OC0# [29]	
+3V_S5	OC1/GPIO41	AT1	USB_OC1#	USB_OC1# [30]	
+3V_S5	OC2/GPIO42	AH2	USB_OC2#		
+3V_S5	OC3/GPIO43	AV3	USB_OC3#		

+3.3V_DEEP_SUS

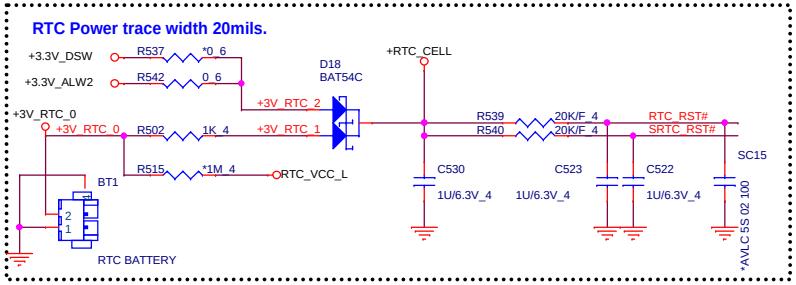
RP9	10K		
USB_OC3#	4	3	
USB_OC1#	2	1	
RP5	10K		
USB_OC2#	4	3	
USB_OC0#	2	1	

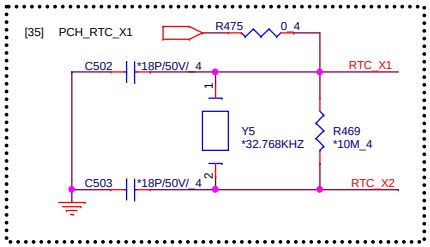
11 OF 19

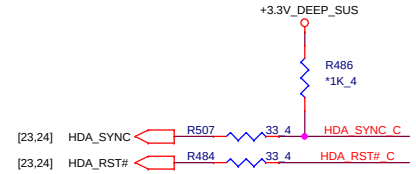
PROJECT : LZ9A
Quanta Computer Inc.

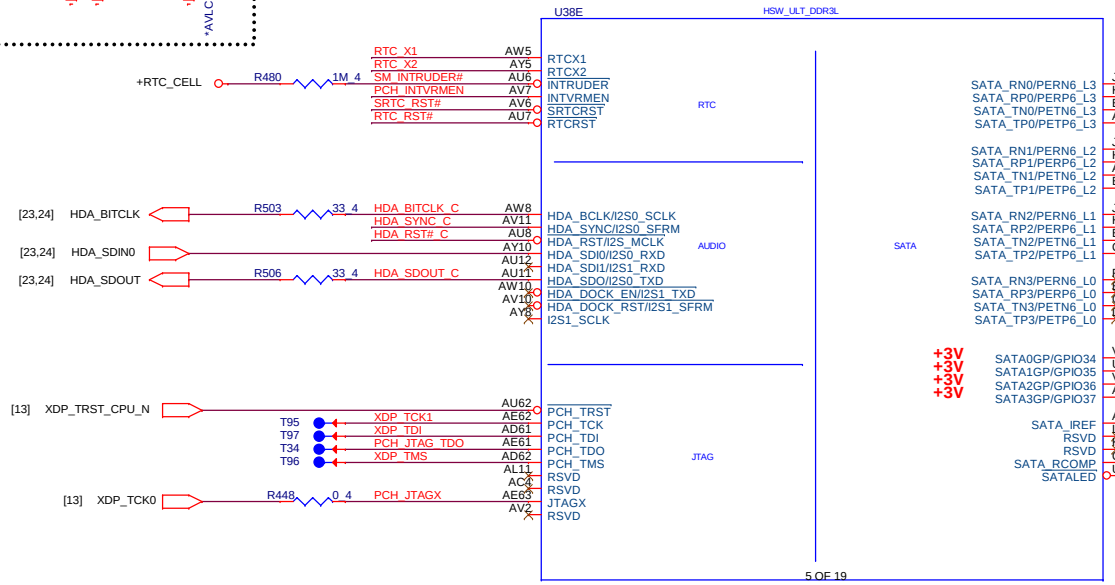
Size	Document Number	Rev
	Haswell ULT 4/12	1A
Date: Thursday, January 03, 2013	Sheet 5 of 47	

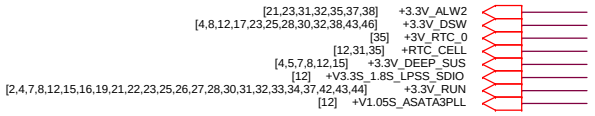
Haswell ULT (RTC, HDA, JTAG, SATA)









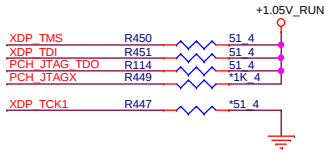


PCH Strap Table

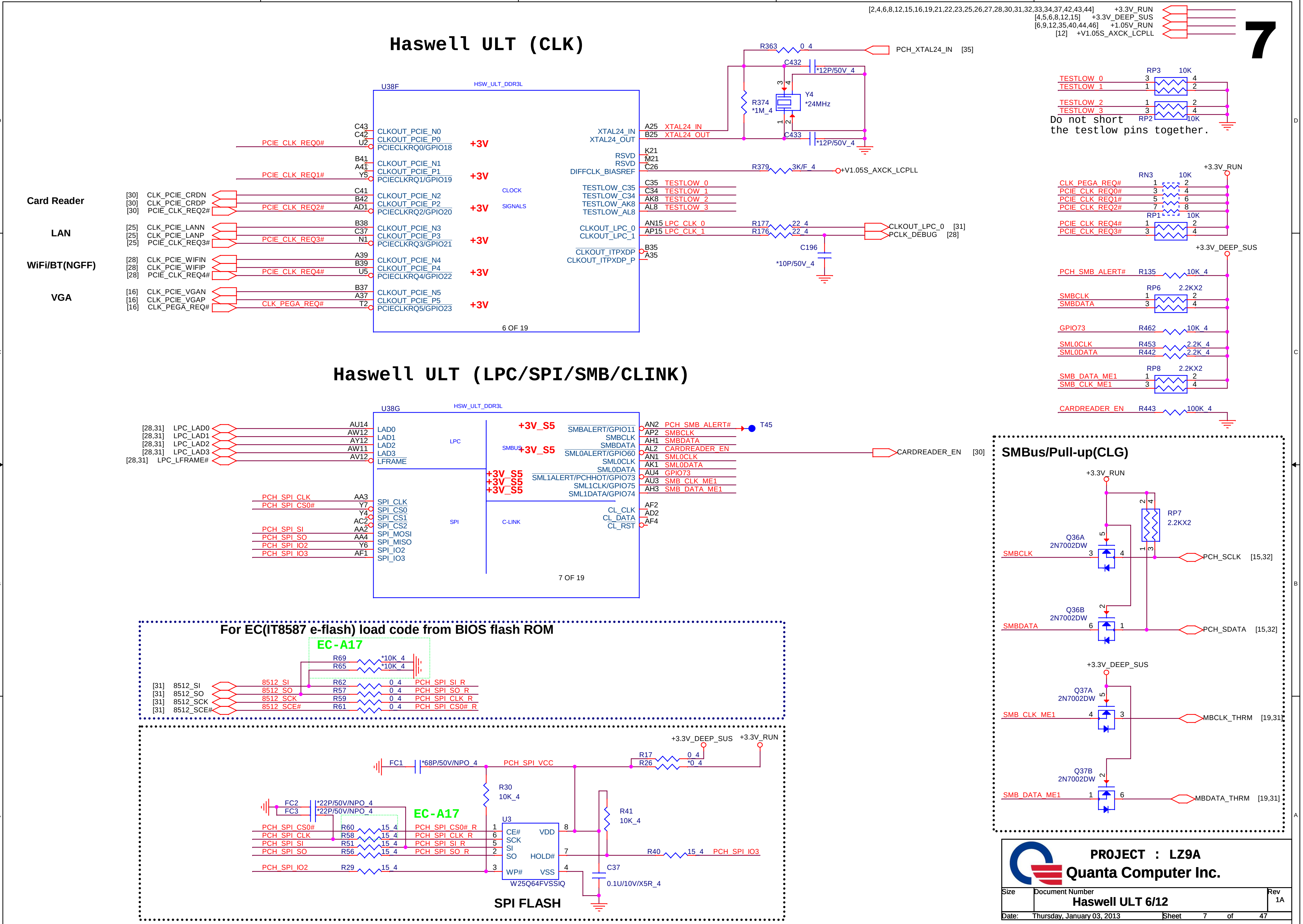
Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R427 *1K_4 ACZ_SPKR [4,23]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	[31] ME_WR# R485 1K_4 HDA_SDOUT_C EC-A22
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R508 330K_4 PCH_INTVRMEN R479 *330K_4
GPIO66	Top-Block Swap override		**0 = Default disable (iPD 20K)** 1 = Enable TBS function	+V3.3S_1.8S_LPSS_SDIO R378 *1K_4 GPIO66 [4] R396 *1K_4
GPIO86	BBS(Boot BIOS Strap Bit)		**0 = Default SPI (iPD 20K)** 1 =LPC	+3.3V_RUN R34 *1K_4 BBS [4] R31 *1K_4
GPIO15	TLS(Transport layer security)		**0 = Default enable w/o confidentiality(iPD 20K)** 1 =Default enable with confidentiality	+3.3V_DEEP_SUS R112 *10K_4 GPIO15 [4]
DSWVREN	Deep Sx well on die DSW VR enable		**1=Should be always pull-up**	+RTC_CELL R481 330K_4 DSWVRMEN [8]

PCH JTAG Debug (CLG)

MP remove(Intel)



PROJECT : LZ9A			
Quanta Computer Inc.			
Size	Document Number		Rev
	Haswell ULT 5/12		1A
Date: Thursday, January 03, 2013	Sheet 6 of 47		



PROJECT : LZ9A

Quanta Computer Inc.

Size | Document Number | Rev
Haswell ULT 6/12 | 1A

Date: Thursday, January 03, 2013 Sheet 7 of 47

Haswell ULT (SYSTEM POWER MANAGEMENT)

8

[4,6,12,17,23,25,28,30,32,38,43,46] +3.3V_DSW
[2,4,6,7,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[4,5,6,7,12,15] +3.3V_DEEP_SUS

U38H HSW_ULT_DDR3L
SYSTEM POWER MANAGEMENT
8 OF 19

[31] SUSACK# R120 0_4 SUSACK# AK2 SUSACK
SYS_RESET# AC3 SYS_RESET
SYS_PWROK AG2 SYS_PWROK
PCH_PWROK AY7 PCH_PWROK
[23,31] EC_PWROK R509 0_4
[31] EC_APWROK R530 *0_4 PCH_APWROK AB5 APWROK
R532 0_4 PLTRST# AG7 PLTRST

EC-A18

+3V
+3V_S5
+3V_S5
DSW

[31] RSMRST# RSMRST# AW6 RSMRST
[31] SUSWARN# SUSWARN# AV4 SUSWARN/SUSPWRDNACK/GPIO30
[31] SIO_PWRBTN# SIO_PWRBTN# AL7 PWRBTN
[19,31] AC_PRESENT AC_PRESENT AJ8 ACPRESENT/GPIO31
PM_BATLOW# AN4 BATLOW/GPIO72
[31] SLP_S0# AF3 SLP_S0
T47 AM5 SLP_WLAN/GPIO29

+3V_S5
DSW
DSW
DSW

DSWVRMEN [6]
AW7 DSWVRMEN
AV5 DPWROK_R DPWROK
AJ5 PCIE_WAKE#_R WAKE
R512 0_4
R510 *0_4 RSMRST#
R134 0_4

EC-A05

DPWROK [31]
PCIE_WAKE# [25,28]

V5 CLKRUN# CLKRUN/GPIO32
AG4 SUS_STAT#/GPIO61
AE6 SUSCLK SUSCLK/GPIO62
AP5 SLP_S5#/GPIO63

CLKRUN# [31]
SUS_STAT# [31]
SIO_SLP_S5# [31]

AJ6 SLP_S4#
AT4 SLP_S3#
AL5 SIO_SLP_A# SLP_A#
AP4 SLP_SUS#
AJ7 SLP_LAN#

SLP_S4# [31]
SIO_SLP_S3# [31]
T50
SLP_SUS# [31]
SIO_SLP_LAN# [25,44]

PCH Pull-high/low(CLG)

+3.3V_DEEP_SUS
SIO_PWRBTN# R130 *10K_4
SUSWARN# R152 10K_4
SUSCLK R118 10K_4

+3.3V_DSW
AC_PRESENT R154 10K_4
PM_BATLOW# R173 10K_4
PCIE_WAKE#_R R137 1K_4

EC-A31

+3.3V_RUN
CLKRUN# R94 10K_4
SYS_RESET# R101 10K_4
RSMRST# R511 10K_4
SYS_PWROK R529 10K_4
DPWROK_R R513 100K_4

SYS_PWROK
RSMRST#
PLTRST#
EC_PWROK

ESD
AVLC 5S 02 100 SC13
AVLC 5S 02 100 SC1
AVLC 5S 02 100 SC12
AVLC 5S 02 100 SC14

+3.3V_DEEP_SUS
R210 *10K_4
Q19 2N7002
PM_BATLOW# PM_BATLOW_N [31]

+3.3V_DEEP_SUS
C479 *0.1U/10V/X7R_4
U33 *TC7SH08FU
[27,28] BUF_PLT_RST#
PLTRST# PLTRST# [16,25,30]
RV2 *AVLC 5S 02 (5.5V,100p)_4
R397 100K_4
R395 0_4

For DS3

+3.3V_DSW +3.3V_DEEP_SUS
R151 *0_6
R148 *100K_4
C175 1U/6.3V_4
U11
[31] SLP_SUS_ON_GPG2
IN IN ON/OFF OUT GND
IC(5P) G5243AT11U
C182 *10P/50V_4
R160 *100K_4
C184 0.1U/10V_4

System PWR_OK(CLG)

EC-A19

+3.3V_DEEP_SUS +3.3V_RUN
R599 *10K_4
R600 *10K_4
Q50 *2N7002
[9,42] IMVP_PWRGD R602 *4.7K_4
Q43 *MMBT3904-7-F

+3.3V_DEEP_SUS
C566 *0.1U/10V/X7R_4
U46 *TC7SH08FU
IMVP_PWRGD_3V
[31] SYS_PWROK_EC
SYS_PWROK
*AVLC 5S 02 SC33
R601 0_4

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Haswell ULT 7/12	1A
Date: Thursday, January 03, 2013	Sheet 8 of 47	

Haswell ULT MCP(POWER)

CPU VDDQ

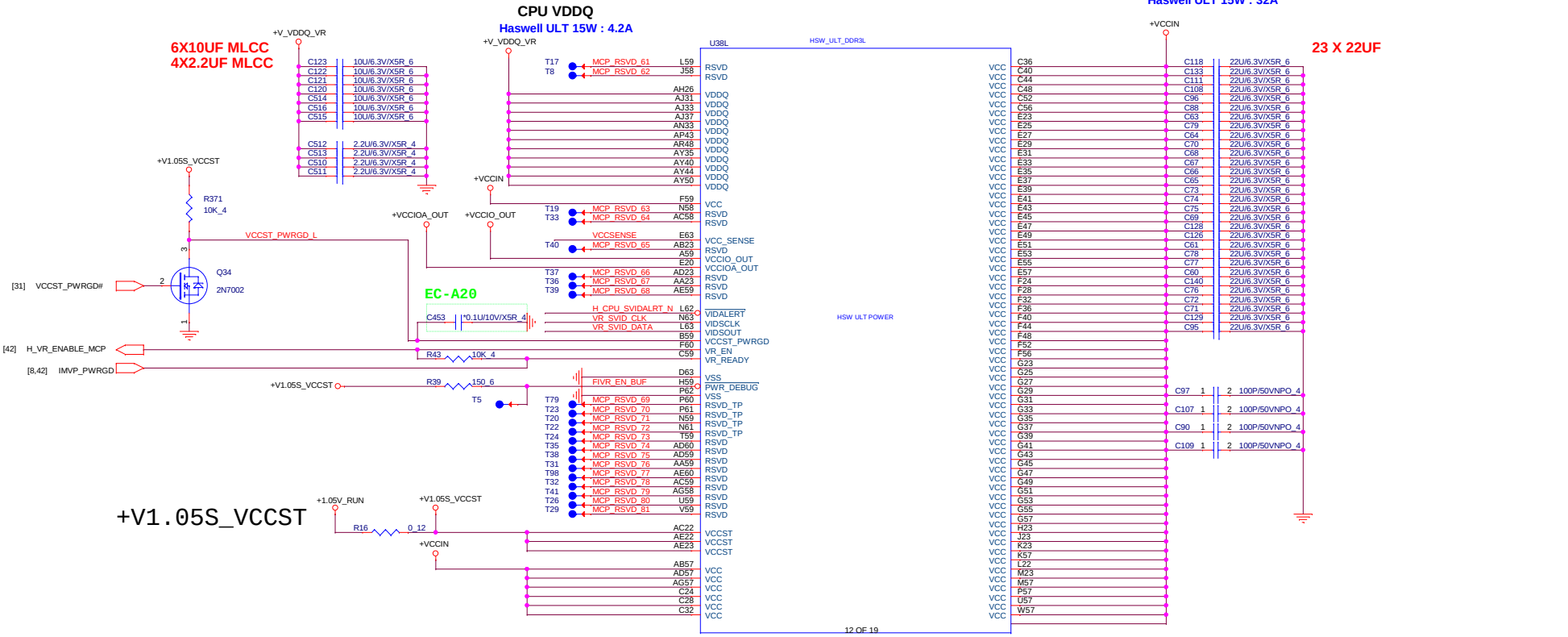
Haswell ULT 15W : 4.2A

6X10UF MLCC
4X2.2UF MLCC

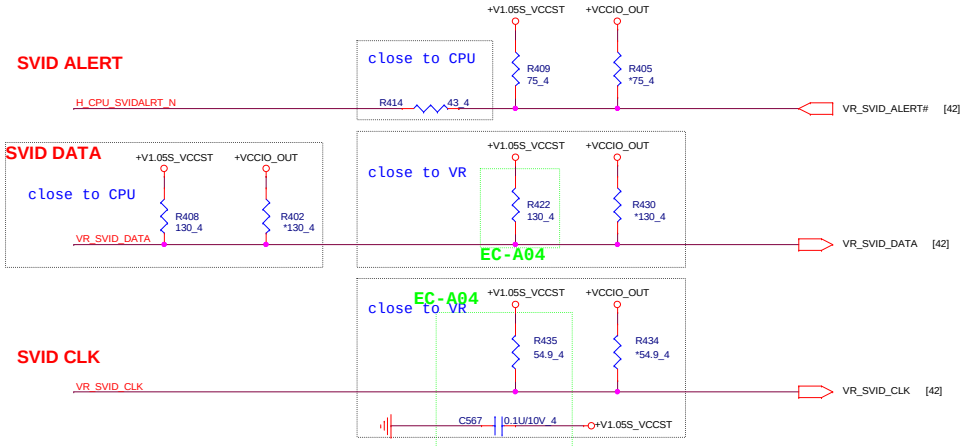
CPU VCC

Haswell ULT 15W : 32A

23 X 22UF

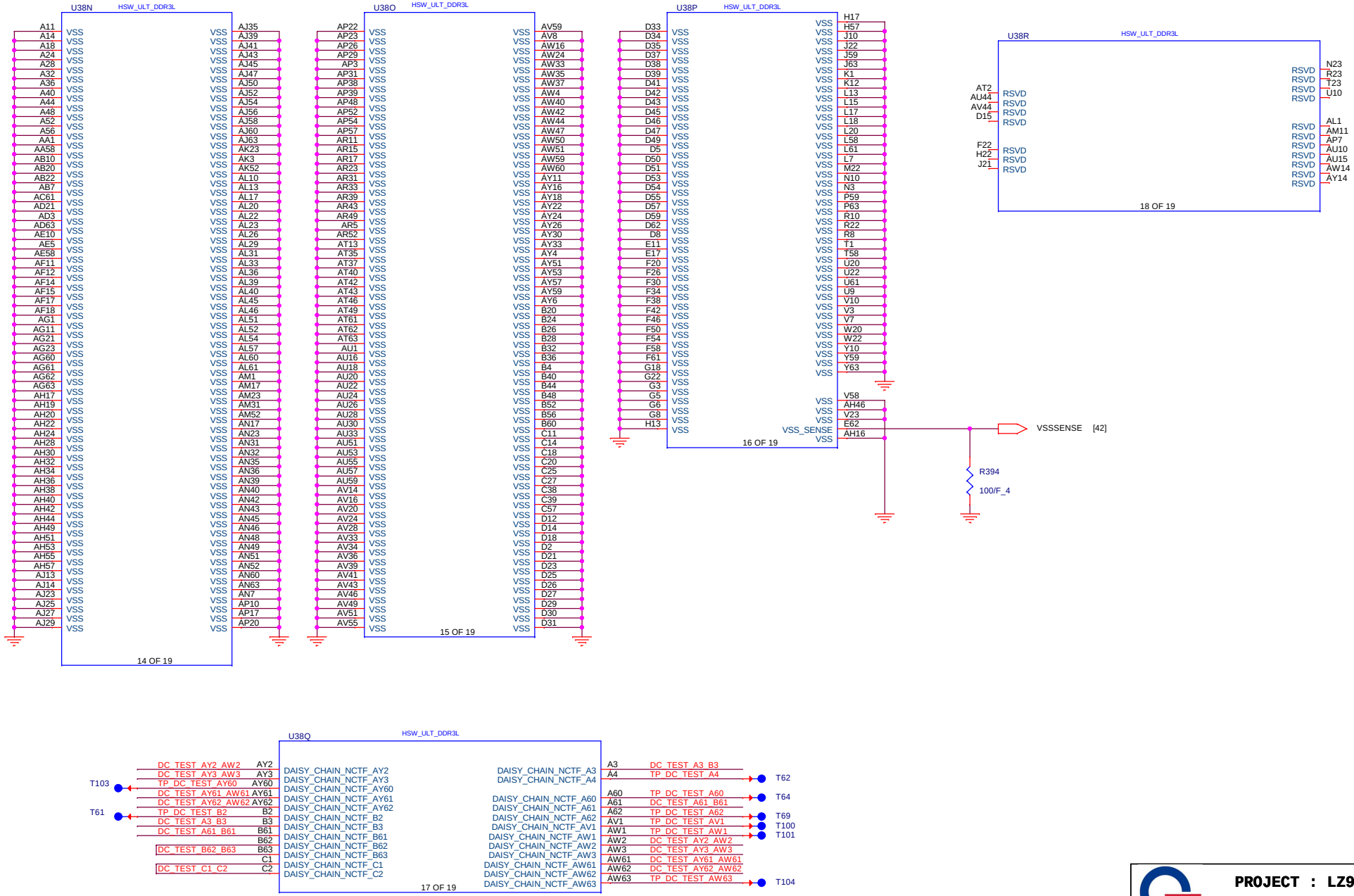


+V1.05S_VCCST

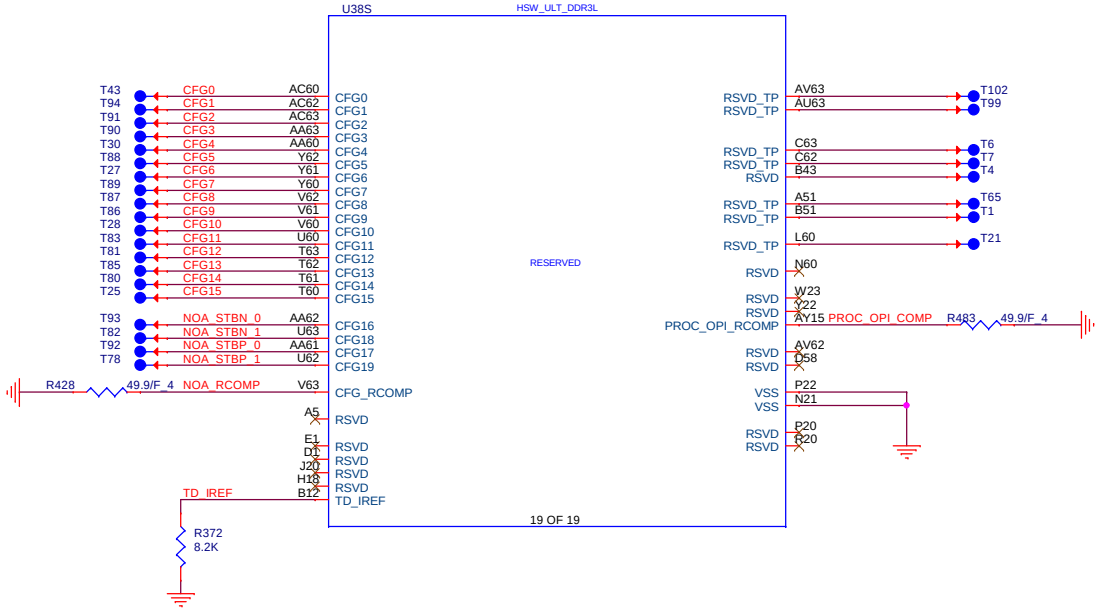


PROJECT :	LZ9A
Quanta Computer Inc.	
Size	Document Number: Haswell ULT 8/12 — Rev: 1A
Date: Thursday, January 03, 2013	Sheet 9 of 47

Haswell ULT (GND)



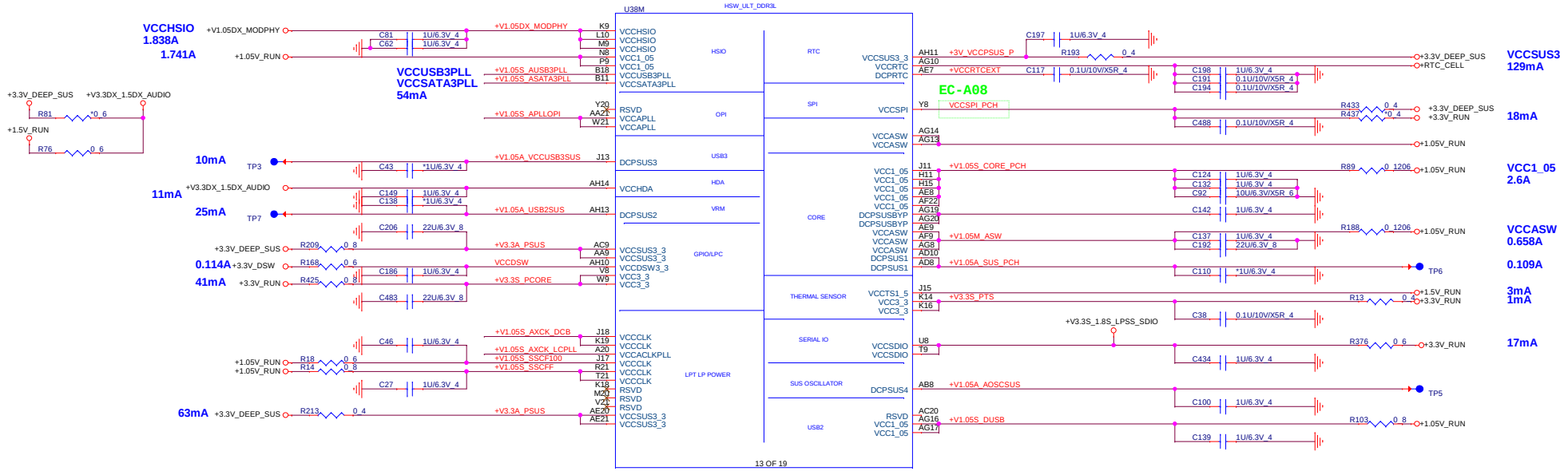
PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: Haswell ULT 9/12	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 10 of 47	

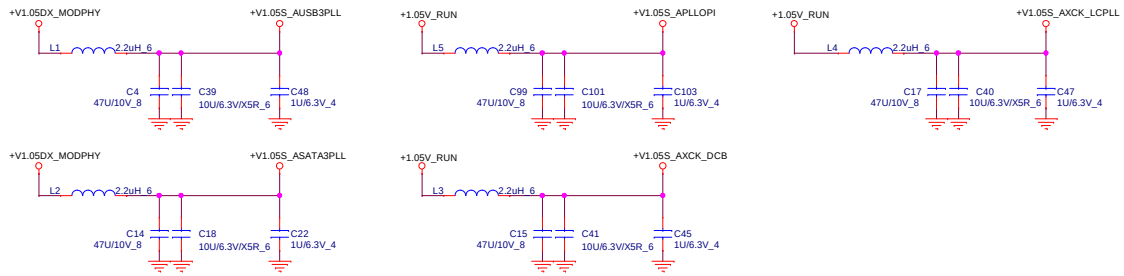


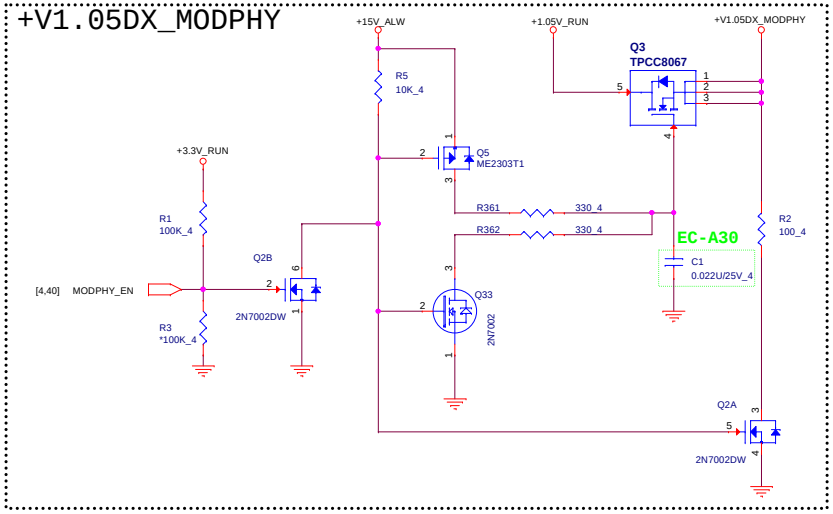
Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R121 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R441 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R438 *1K_4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R102 1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R432 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R429 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R98 *1K_4

Haswell ULT PCH(POWER)



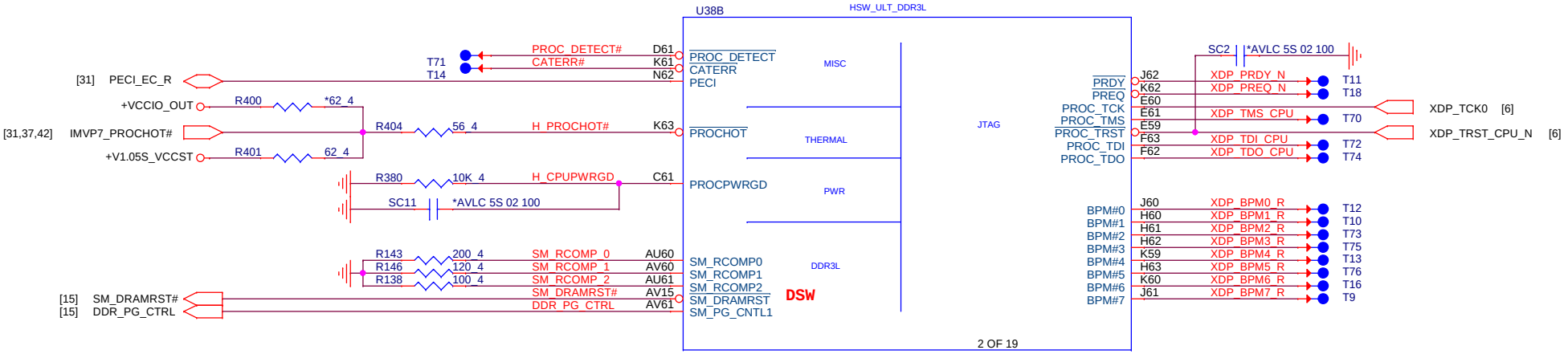


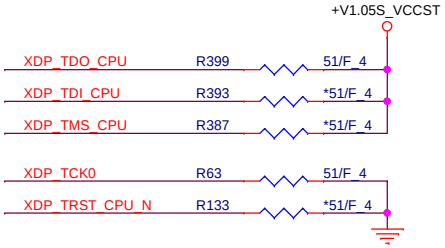


PROJECT : LZ9A
Quanta Computer Inc.
Size
Document Number
Haswell ULT 11/12
Rev
1A
Date: Thursday, January 03, 2013
Sheet 12 of 47

[4,9] +V1.05S_VCCST
[9] +VCCIO_OUT

13





PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Haswell ULT 12/12	1A
Date: Thursday, January 03, 2013	Sheet 13 of 47	

CHANNEL A: 4GB DDR3L

[3] M_A_DQSP[7:0]
[3] M_A_DQSN[7:0]
[3] M_A_DQ[63:0]

[15,39,44] +0.675V_DDR_VTT
[9,15,39,44] +V_VDDQ_VR
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[15,17,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW
[15] +SMDDR_VREF_CA

BYTE7_56-63 BYTE4_32-39

U14

+SMDDR_VREF_CA
+SMDDR_VREF_DQ0
[3] M_A_A[15..0]

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

+V_VDDQ_VR

Should be 240 Ohms +-1%
R170 240/F_4
R169 240/F_4

[15] DDR3_DRAMRST#

RAM_DDR3

BYTE3_24-31 BYTE1_8-15

U44

Should be 240 Ohms +-1%
R554 240/F_4
R558 240/F_4

BYTE2_16-23 BYTE0_0-7

U21

Should be 240 Ohms +-1%
R235 240/F_4
R234 240/F_4

BYTE6_48-55 BYTE5_40-47

U41

Should be 240 Ohms +-1%
R543 240/F_4
R544 240/F_4

+0.675V_DDR_VTT

R548 34.8/F_4 M_A_BS#0
R254 34.8/F_4 M_A_BS#1
R535 34.8/F_4 M_A_BS#2
R551 34.8/F_4 M_A_CS#0
R534 34.8/F_4 M_A_CKE0
R550 34.8/F_4 M_A_CAS#
R552 34.8/F_4 M_A_RAS#
R249 34.8/F_4 M_A_WE#
R240 34.8/F_4 M_A_A0
R242 34.8/F_4 M_A_A1
R538 34.8/F_4 M_A_A2
R546 34.8/F_4 M_A_A3
R541 34.8/F_4 M_A_A4
R236 34.8/F_4 M_A_A5
R232 34.8/F_4 M_A_A6
R222 34.8/F_4 M_A_A7
R226 34.8/F_4 M_A_A8
R220 34.8/F_4 M_A_A9
R549 34.8/F_4 M_A_A10
R216 34.8/F_4 M_A_A11
R536 34.8/F_4 M_A_A12
R262 34.8/F_4 M_A_A13
R218 34.8/F_4 M_A_A14
R547 34.8/F_4 M_A_A15
R260 34.8/F_4 M_A_CS#1
R533 34.8/F_4 M_A_CKE1

+0.675V_DDR_VTT
R174 26.1/F_4 M_A_CLKP0
R166 26.1/F_4 M_A_CLKN0

+V_VDDQ_VR
[3] SM_VREF_DQ0
R295 30/F_4 M_A_ODT0
R167 0_6
R150 1.8K/F_4
R175 5.11/F_4 +SMDDR_VREF_DQ0
C183 0.022U/16V_4
R158 24.9/F_4
R545 1.8K/F_4

Place near MD device

+SMDDR_VREF_CA
C202 0.047U/10V_4
C239 0.047U/10V_4
C527 0.047U/10V_4
C291 0.047U/10V_4
+SMDDR_VREF_DQ0
C301 0.047U/10V_4
C309 0.047U/10V_4
C180 0.047U/10V_4
C242 0.047U/10V_4
B.1119

+0.675V_DDR_VTT
C251 1U/6.3V_4
C246 1U/6.3V_4
C257 1U/6.3V_4
C243 1U/6.3V_4
C236 10U/6.3V_6

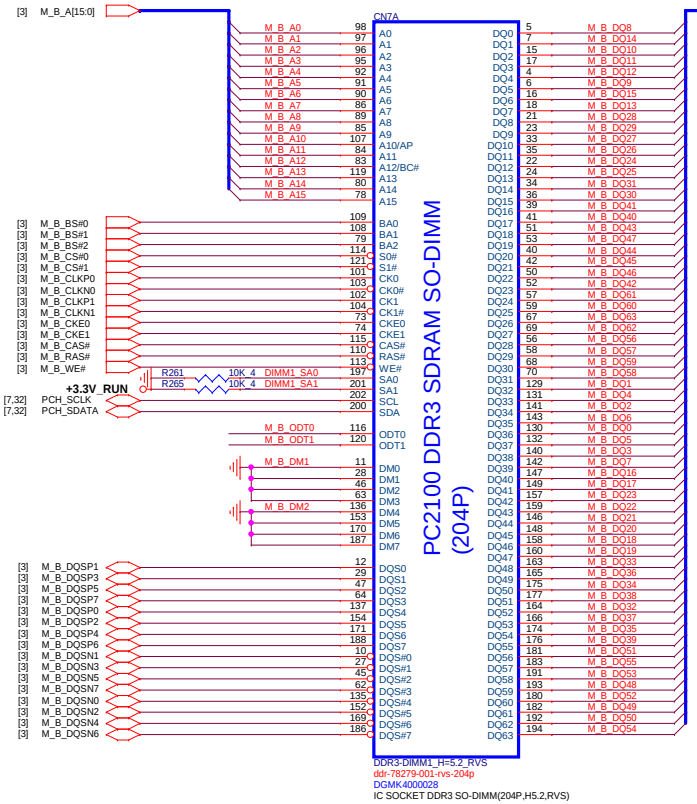
Place these Caps near Memory Down

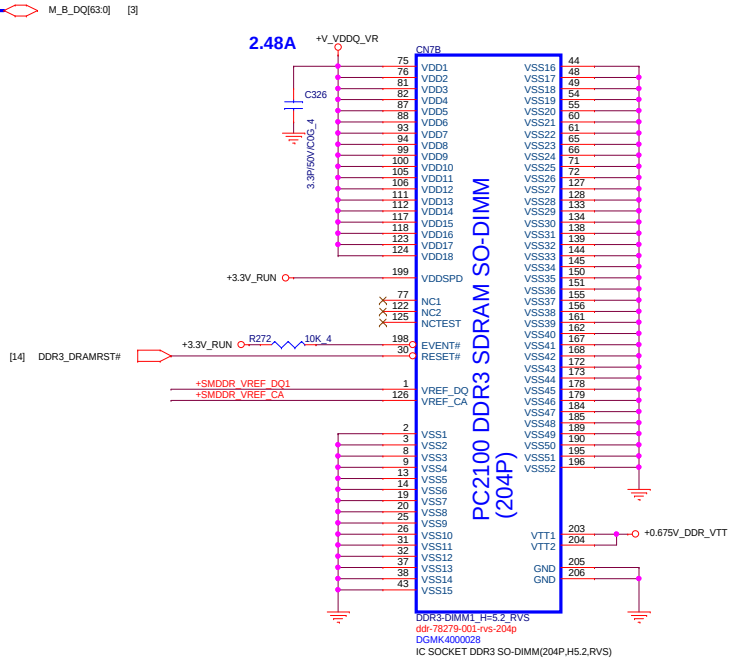
ONLY 3 NEED TO BE STUFFED FOR ONE DEVICE

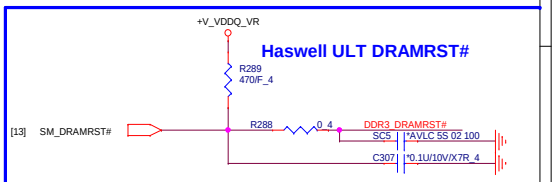
+V_VDDQ_VR
C231 1u/6.3V_4
C188 1u/6.3V_4
C531 1u/6.3V_4
C507 1u/6.3V_4
C187 1u/6.3V_4
C504 1u/6.3V_4
C259 *1u/6.3V_4
C535 *1u/6.3V_4
C508 *1u/6.3V_4
C528 *1u/6.3V_4
C541 *1u/6.3V_4
C233 *1u/6.3V_4
C241 1u/6.3V_4
C277 1u/6.3V_4
C529 1u/6.3V_4
C240 1u/6.3V_4
C244 1u/6.3V_4
C207 1u/6.3V_4
C534 *1u/6.3V_4
C542 *1u/6.3V_4
C509 *1u/6.3V_4
C505 *1u/6.3V_4
C506 *1u/6.3V_4
C537 *1u/6.3V_4
C214 10u/6.3V_6
C201 10u/6.3V_6
C272 10u/6.3V_6
C225 10u/6.3V_6
C250 *10u/6.3V_6
C538 *10u/6.3V_6
C553 *150u/6.3V_3528

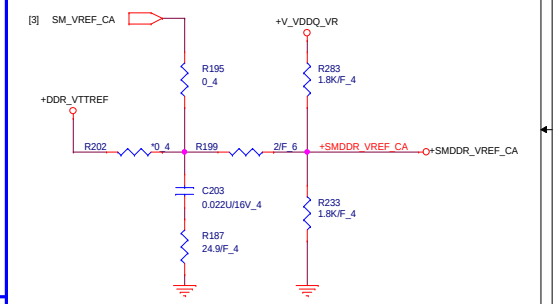
PROJECT : LZ9A
Quanta Computer Inc.
Size: Document Number: DDR3L MEMORY DOWN Rev: 1A
Date: Thursday, January 03, 2013 Sheet 14 of 47

[14,39,44] +0.675V_DDR_VTT
[9,14,39,44] +V_VDDQ_VR
[2,4,6,7,8,12,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[17,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW
[14] +SMDDR_VREF_CA
[4,5,6,7,8,12] +3.3V_DEEP_SUS

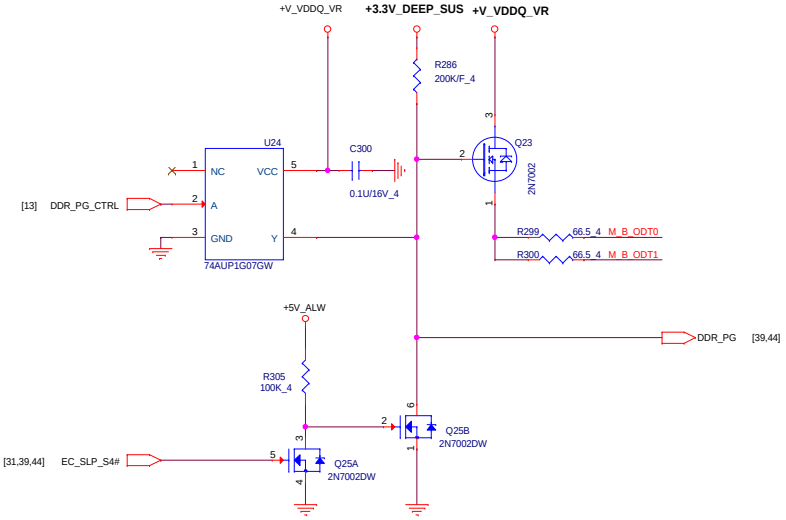




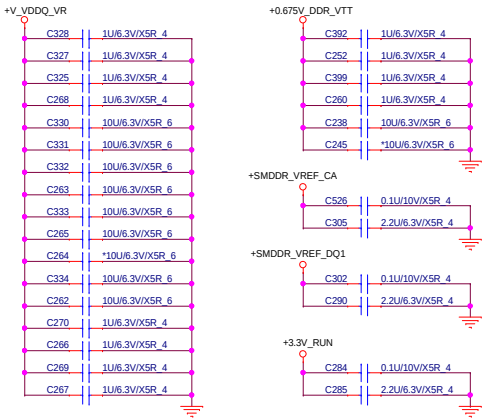




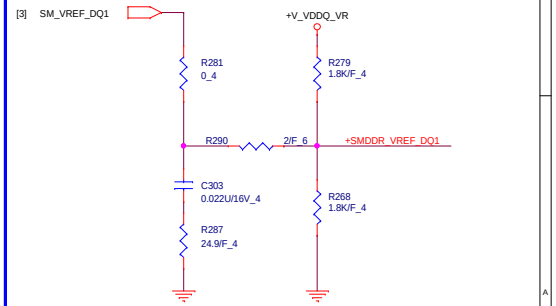
DDR3L SODIMM ODT DENERATION



Place these Caps near So-Dimm1



VREF DQ1 Solution



PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Custom DDR3 DIMM0-STD (5.2H)	3A
Date: Thursday, January 03, 2013	Sheet 15 of 47	

[17,19,35,45,46,47] 3V_GPU
[17,18,46,47] 1.05V_GFX_PCIE
[45,47] VGPU_CORE
[2,4,6,7,8,12,15,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN

<VGA>

3300mA

Peak current:45A
Boosted:28A

210mA

150mA

12~16 mils

EC-A01

EC-A48

PEG CLK detect

GPU RST#(CLG)

Table 2. GPU Power Rails

GPU Power Rail	Nominal Value	Comments
NVVDD	GPU SKU Specific	GPU Core power rail
FBVDD[2]	1.35 V or 1.5 V	VRAM Core power for Frame Buffer components
FBVDDQ[2]	1.35 V or 1.5 V	VRAM I/O and GPUs Frame Buffer I/O power rail
IFPx_IOVDD[3]	1.05 V or 3.3V	Powers IFP blocks
IFPx_PLLVDD[3]	1.05 V or 3.3 V	Integrated Digital Display PLL Power Rails
PEX_IOVDD/Q	1.05 V	GPUs PCIE interface power rail
PEX_SVDD_3V3, PEX_PLL_HVDD	3.3 V	GPU PCIE PLL Power Rails
PEX_PLLVDD	1.05 V	GPU PCIE PLL Power Rails
FBx_PLL_AVDD	1.05 V or 3.3 V	Frame Buffer PLL Power Rail
FBx_DLL_AVDD (GB2-192 and GB3-256)	1.05 V	Frame Buffer PLL and DLL Power Rail
FBx_PLL_DLL_AVDD (GB2-192 and GB3-256)	1.05 V	Frame Buffer PLL and DLL Power Rail
PLLVDD, GPCPLL_AVDD LXS_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
VID_PLLVDD	1.05 V	Video Pixel Clock PLL Analog Power Rail
SP_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
DACx_VDD[1]	3.3 V	Powers the DAC interfaces
VDD33(NV3V3)[4]	3.3 V	Powers slower logic such as GPIOs, I2C, AUX channels and SLI

Notes:
1. The same power plane can be used for VDD33 and DACx_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays)
4. On GB3-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	N14M-GS (PCIE I/F) 1/5	1A

Date: Tuesday, January 08, 2013 Sheet 16 of 47

<VGA>

[20] VMA_DQ[63..0] — VMA_DQ[63..0]
[20] VMA_DM[7..0] — VMA_DM[7..0]
[20] VMA_WDQS[7..0] — VMA_WDQS[7..0]
[20] VMA_RDQS[7..0] — VMA_RDQS[7..0]

U39B
bga595-nvidia-n13m-gs-s-a2
COMMON
2/14 FBA

R144 FB_CLAMP — F3 — 0_4
R147 — DIS@10K/F_4

FB_CLAMP	NC
GF117/GK208	GF119

FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63

[20] FBA_CMD0 — C27 — FBA_CMD0
FBA_CMD1 — C26
[20] FBA_CMD2 — FBA_CMD2 — E24
[20] FBA_CMD3 — FBA_CMD3 — F24
[20] FBA_CMD4 — D27
[20] FBA_CMD5 — FBA_CMD5 — D26
[20] FBA_CMD6 — F25
[20] FBA_CMD7 — F26
[20] FBA_CMD8 — F23
[20] FBA_CMD9 — G22
[20] FBA_CMD10 — G23
[20] FBA_CMD11 — G24
[20] FBA_CMD12 — F27
[20] FBA_CMD13 — G25
[20] FBA_CMD14 — G27
[20] FBA_CMD15 — G26
[20] FBA_CMD16 — M24
FBA_CMD17 — M23
[20] FBA_CMD18 — FBA_CMD18 — K24
[20] FBA_CMD19 — FBA_CMD19 — K23
[20] FBA_CMD20 — M27
[20] FBA_CMD21 — M26
[20] FBA_CMD22 — M25
[20] FBA_CMD23 — K26
[20] FBA_CMD24 — K22
[20] FBA_CMD25 — J23
[20] FBA_CMD26 — J25
[20] FBA_CMD27 — J24
[20] FBA_CMD28 — K27
[20] FBA_CMD29 — K25
[20] FBA_CMD30 — J27
[20] FBA_CMD31 — J26

For debug only 10mA
1.5V_GPU — R131 *DIS@60.4/F_4 — FBA_DEBUG0 — F22 — FBA_DEBUG0
R128 *DIS@60.4/F_4 — FBA_DEBUG1 — J22 — FBA_DEBUG1

[20] VMA_CLK0 — D24 — FBA_CLK0
[20] VMA_CLK0# — D25 — FBA_CLK0
[20] VMA_CLK1 — N22 — FBA_CLK1
[20] VMA_CLK1# — M22 — FBA_CLK1

D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67

FBA_DQM0 D19 VMA_DM0
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7

FBA_DQS_WP0 E19 VMA_WDQS0
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 R25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7

FBA_DQS_RN0 F19 VMA_RDQS0
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7

1.05V_GFX_PCIE
Near GPU 15mils width
L21 DIS@HCB1608KF-300T10_1A_6 — +FB_PLLAVDD — F16 — FB_PLLAVDD
P22 — FB_PLLAVDD
H22
200mA
30ohm/100MHz
ESR=0.01ohm

FB_DLLAVDD	FB_PLLAVDD
GF119/GK208	GF117

Under GPU
C167 DIS@0.1U/10V/X7R_4
C448 DIS@0.1U/10V/X7R_4
C169 DIS@0.1U/10V/X7R_4
Near GPU
C431 DIS@22U/6.3V/X5R_8

FB_VREF_PROBE — D23 — +FB_VREF1 — TP8

U_GPU_GB2_64

GC6 feature for N14M-GS

DIS@2N7002_200MA
Q12
[31,46] FB_CLAMP — FB_CLAMP — 3 — 1 — FB_CLAMP_MON [19]
2
C174 *DIS@10U/6.3V/X5R_6
R161 DIS@10K/F_4
+5V_ALW
R189 *DIS@10K/F_4
3V_GPU
R591 DIS@0_4
3
5 — Q20A *DIS@2N7002KDW — 4
C193 *DIS@10U/6.3V/X5R_6
+3.3V_DSW
R219 *DIS@10K/F_4
[16,31,45,46] GFXON — 2 — 6 — 1 — Q20B *DIS@2N7002KDW

2.16A

1.5V_GPU

U39D
bga595-nvidia-n13m-gs-s-a2
COMMON
12/14 FBVDDQ

FBVDDQ B26
FBVDDQ C25
FBVDDQ E23
FBVDDQ E26
FBVDDQ F14
FBVDDQ F21
FBVDDQ G13
FBVDDQ G14
FBVDDQ G15
FBVDDQ G16
FBVDDQ G18
FBVDDQ G19
FBVDDQ G20
FBVDDQ G21
FBVDDQ H24
FBVDDQ H26
FBVDDQ J21
FBVDDQ K21
FBVDDQ L22
FBVDDQ L24
FBVDDQ L26
FBVDDQ M21
FBVDDQ N21
FBVDDQ R21
FBVDDQ T21
FBVDDQ V21
FBVDDQ W21

Under GPU
C116 DIS@0.1U/10V/X7R_4
C136 DIS@0.1U/10V/X7R_4
C168 DIS@4.7U/6.3V/X5R_6
C156 DIS@1U/10V/X7R_6
C105 DIS@1U/10V/X7R_6
C155 DIS@4.7U/6.3V/X5R_6
C484 DIS@10U/6.3V/X5R_6
C487 DIS@22U/6.3V/X5R_8
Near GPU

U_GPU_GB2_64

1.5V_GPU — R526 DIS@40.2/F_4 — FB_CAL_PD_VDDQ — D22 — FB_CAL_PD_VDDQ
R522 DIS@42.2/F_4 — FB_CAL_PU_GND — C24 — FB_CAL_PU_GND
R517 DIS@51.1/F_4 — FB_CAL_TERM_GND — B25 — FB_CALTERM_GND

U_GPU_GB2_64

U39F
bga595-nvidia-n13m-gs-s-a2
COMMON
13/14 GND

M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5 — GND
AA7 AB7 — GND
A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 A26 AE15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11 — GND

U_GPU_GB2_64

FBA_CMD2 R474 DIS@10K/F_4
FBA_CMD3 R499 DIS@10K/F_4
FBA_CMD5 R122 DIS@10K/F_4
FBA_CMD18 R415 DIS@10K/F_4
FBA_CMD19 R423 DIS@10K/F_4

DDR3 Command Bit	Data[31..0]	Data[63..32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

[16,18,46,47] 1.05V_GFX_PCIE
[16,20,46,47] 1.5V_GPU
[16,19,35,45,46,47] 3V_GPU
[15,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW

PROJECT : LZ9A
Quanta Computer Inc.

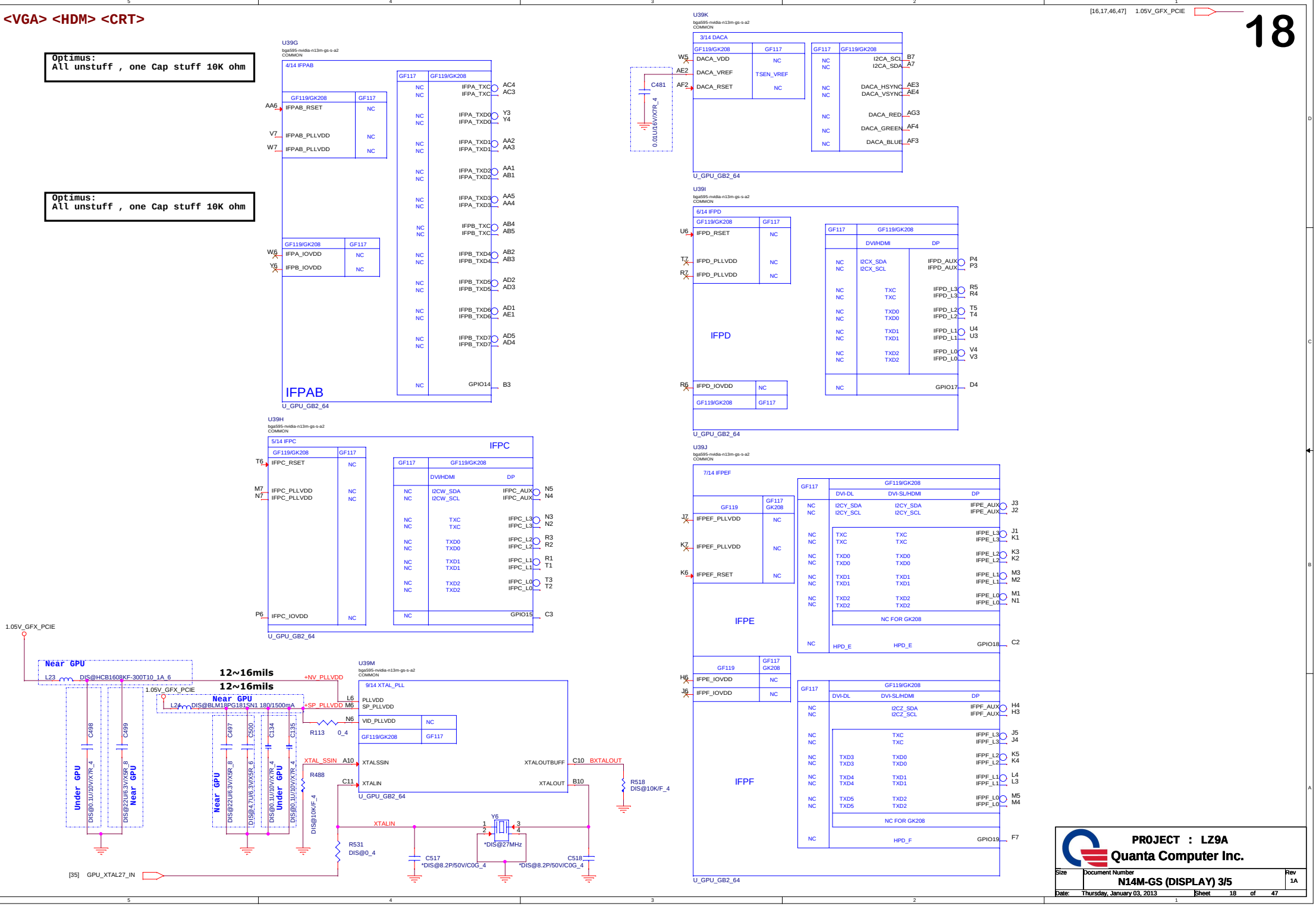
Size	Document Number	Rev
	N14M-GS (MEMORY/GND) 2/5	1A

Date: Thursday, January 03, 2013 Sheet 17 of 47

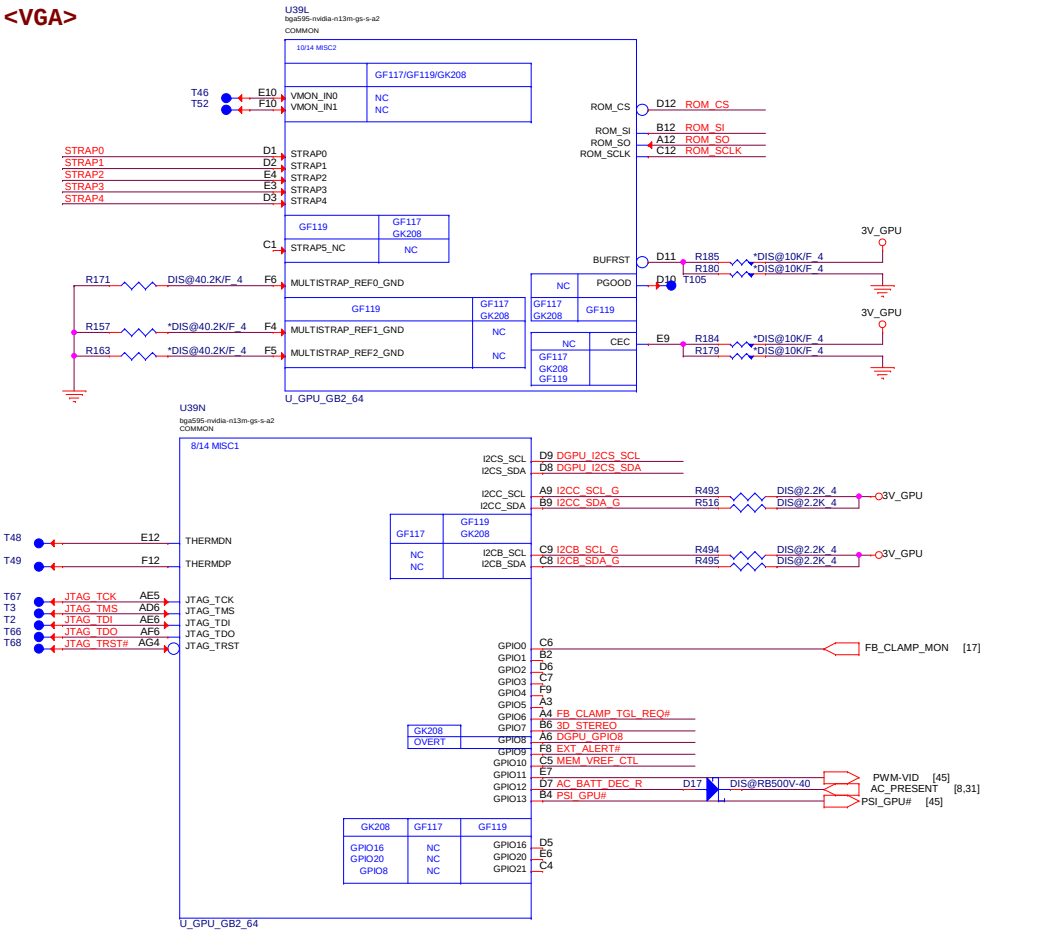
<VGA> <HDM> <CRT>

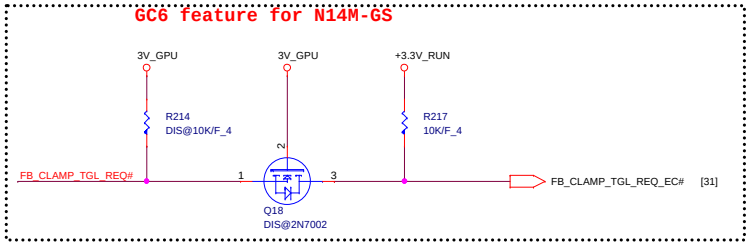
Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm



PROJECT : LZ9A			
Quanta Computer Inc.			
Size	Document Number		Rev
	N14M-GS (DISPLAY) 3/5		1A
Date: Thursday, January 03, 2013		Sheet 18 of 47	



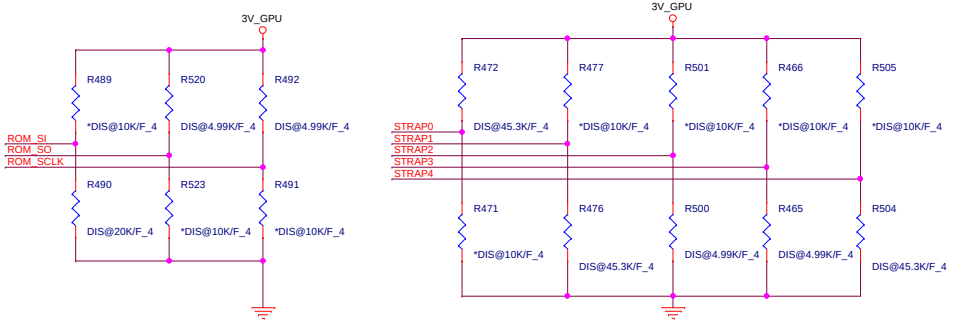


Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVIDE[5]	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0011

DDR3 RAM_CFG

GPU SKU	GPU	VRAM Vendor	Type	BVDD/ FBVDDQ	Config	VRAM P/N	Max Speed CLK	D/C Mini	RAM_CFG	ROM_SI
GK208/GK107	N14M-GS/N14M-LP/N14P-GV2 N14P-GS/N14P-LP/N14P-GE	Samsung	DDR3	1.5 V/ 1.5 V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x7	PD 45K
						K4W2G1646E-BC11	900Mhz			
		Micro	DDR3	1.5 V/ 1.5 V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1234	0x5	PD 30K
						MT41J128M16JT-107G:K	900Mhz	1150		
		Hynix	DDR3	1.5 V/ 1.5 V	128Mx16	H5TQ2G63DFR-N0C	1000Mhz	NA	0x6	PD 35K
						H5TQ2G63DFR-11C	900Mhz			
		Samsung	DDR3	1.5 V/ 1.5 V	256Mx16	K4W4G1646B-HC11	900Mhz	NA	0x3	PD 20K
		Micro	DDR3	1.5 V/ 1.5 V	256Mx16	MT41K256M16HA-107G:E	900Mhz	NA	0x1	PD 10K
		Samsung	DDR3L	1.35V/ 1.35V	128Mx16	K4W2G1646E-BY11	900Mhz	1204	0xA	PU 15K
		Micro	DDR3L	1.35V/ 1.35V		MT41K128M16JT-107G:K	900Mhz	NA	0x8	PU 5K

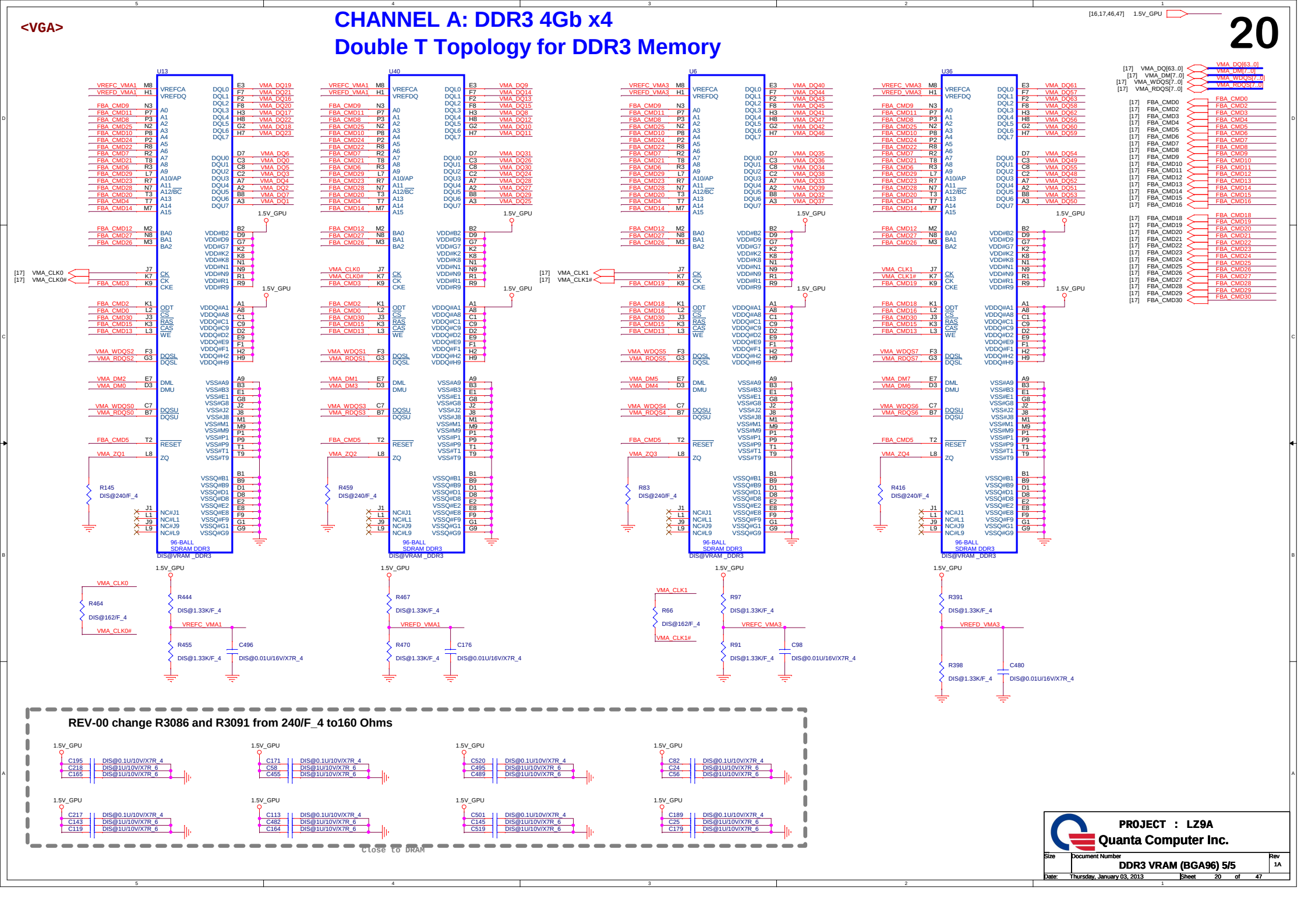


GK208 SKU	
Item	N14M-GS-B/S-A2
Device ID	0X1290
Package	GB4-128
Internal P/N	GK208,28nm
ROM_SI	Refer to N14x_RAM_Straps table
ROM_SO	0x8, 5kohm pull high
ROM_SCLK	0x1000,0x8, 4.99Kohm pull up
Strap0	User Strap, 0xF, 45kohm pull up
Strap1	3GIO_PAD_Config, 0x7, 45kohm pull down(After QS)
Strap2	Device_ID, 0x0000_5Kohm pull down
Strap3	0x0 for Optimus, 5kohm pull low
Strap4	0x0111, 45kohm pull down(PCIE_SPEED_CHANGE=1)
Open_VRG SKU	Config B
NVVDD Boot Voltage	0.9V

PROJECT : LZ9A
Quanta Computer Inc.

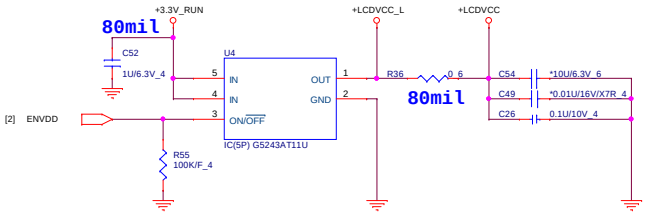
Size	Document Number	Rev
	N14M-GS (GPIO/STRAPS) 4/5	1A
Date: Thursday, January 03, 2013	Sheet 19 of 47	

CHANNEL A: DDR3 4Gb x4
Double T Topology for DDR3 Memory

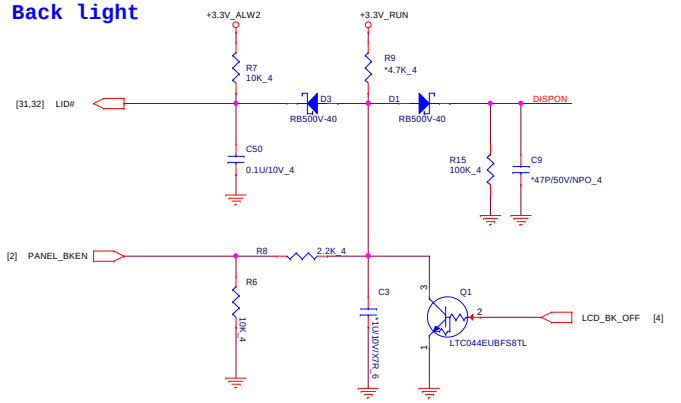


PROJECT : LZ9A			
Quanta Computer Inc.			
Size	Document Number		Rev
	DDR3 VRAM (BGA96) 5/5		1A
Date: Thursday, January 03, 2013	Sheet 20 of 47		

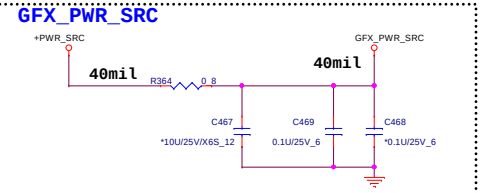
LCDVCC

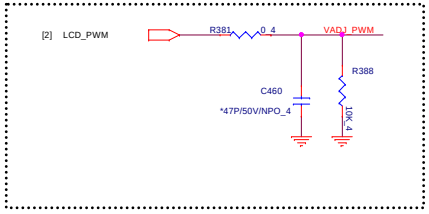


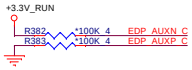
Back light



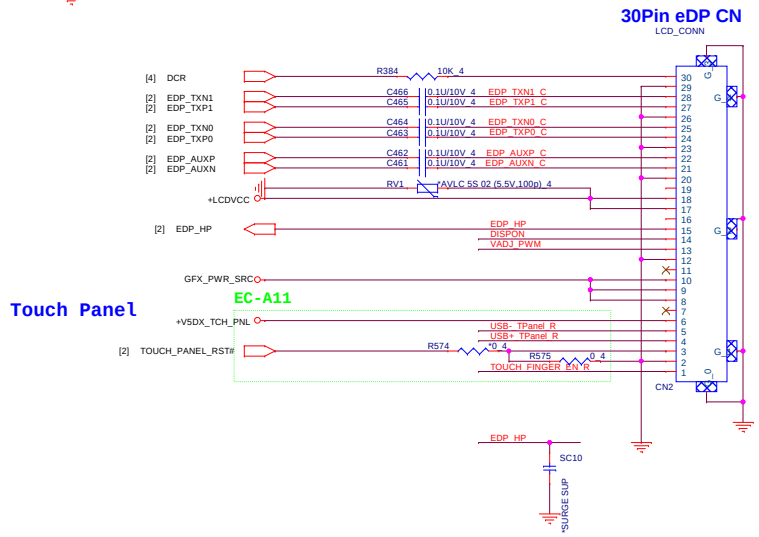
GFX_PWR_SRC







Touch Panel

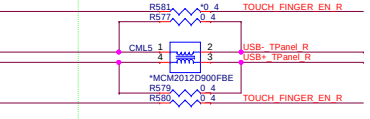


Touch Panel Interface

EC-A11

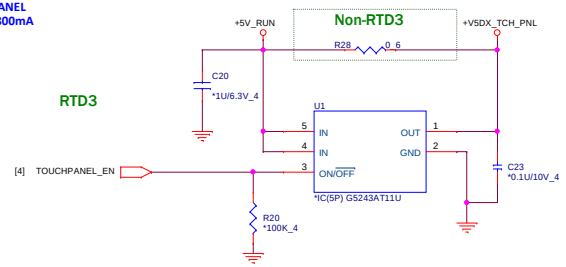
I2C interface

USB interface



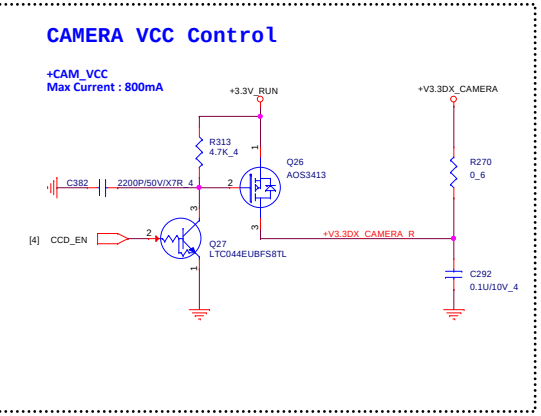
Touch Panel VCC Control

+5V_TOUCH_PANEL
Max Current : 800mA



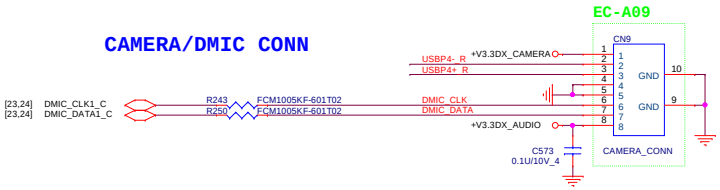
CAMERA VCC Control

+CAM_VCC
Max Current : 800mA

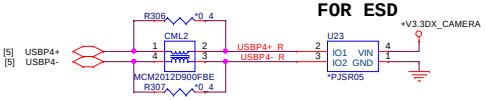


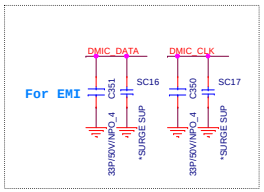
CAMERA/DMIC CONN

EC-A09



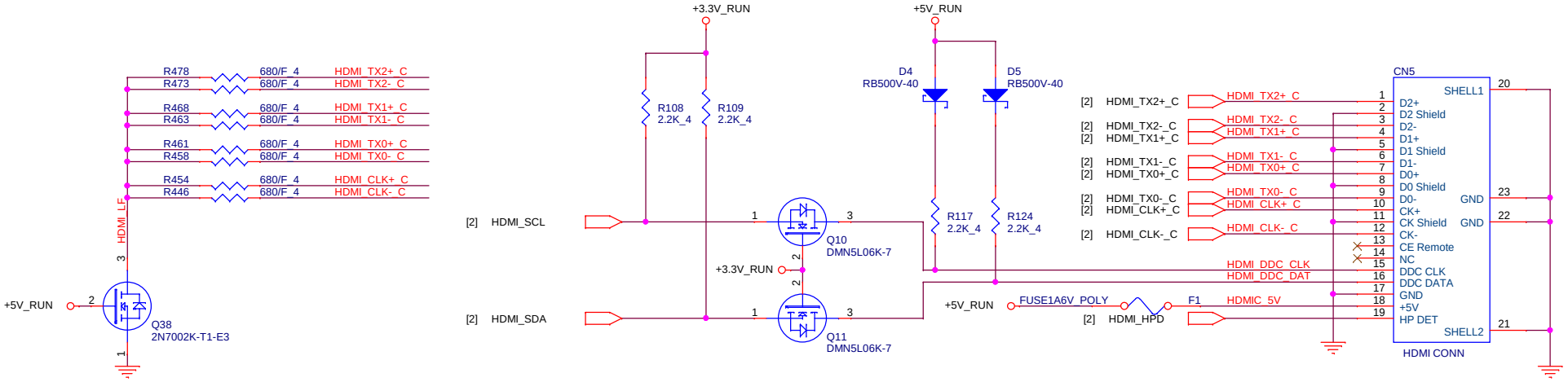
FOR ESD

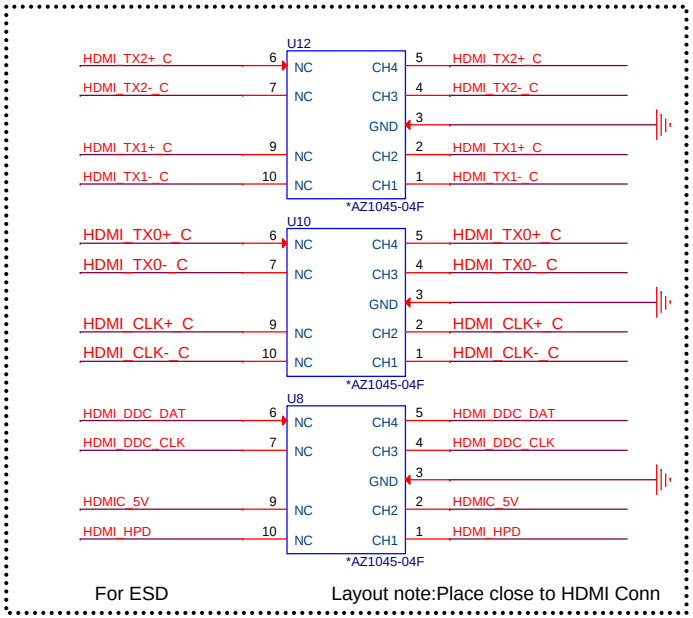




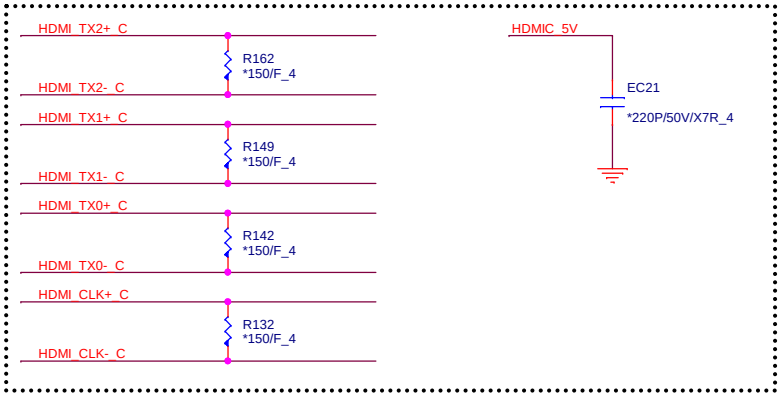
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	LCD/CAMERA/Touch Panel	1A
Date: Thursday, January 03, 2013	Sheet 21 of 47	





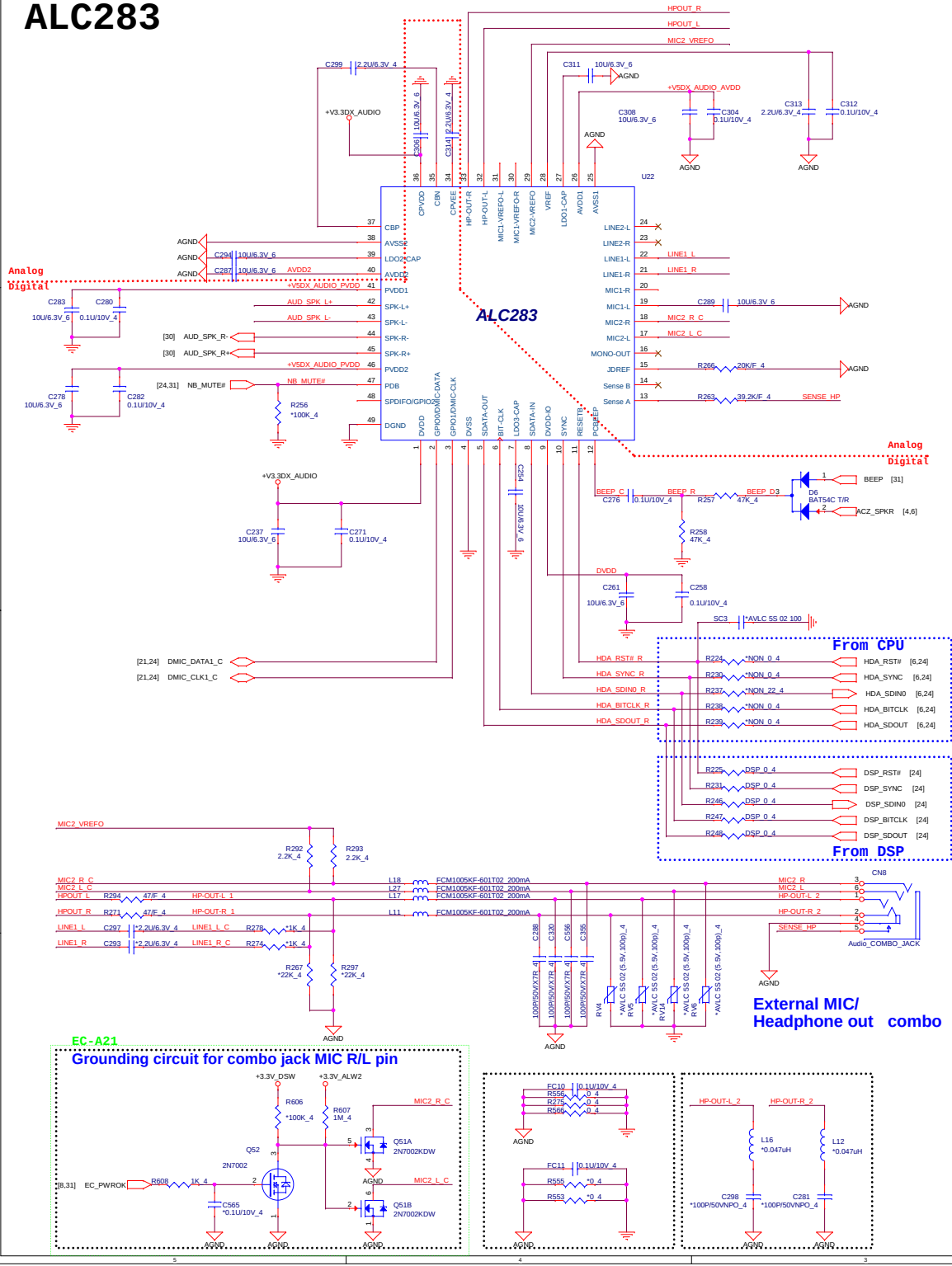
EMI reserve for HDMI



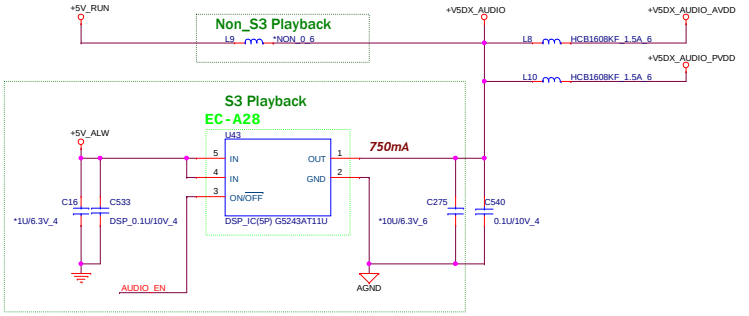
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI CONN	1A
Date: Thursday, January 03, 2013	Sheet 22 of 47	

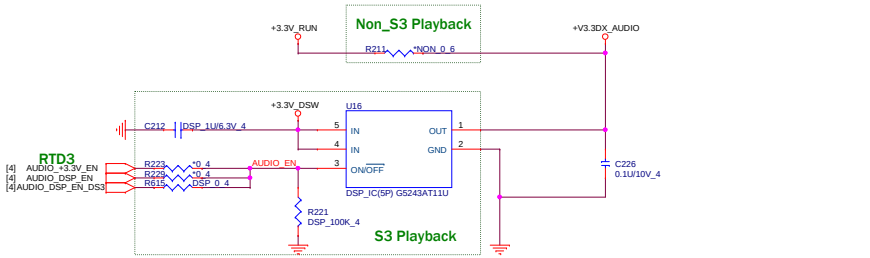
ALC283

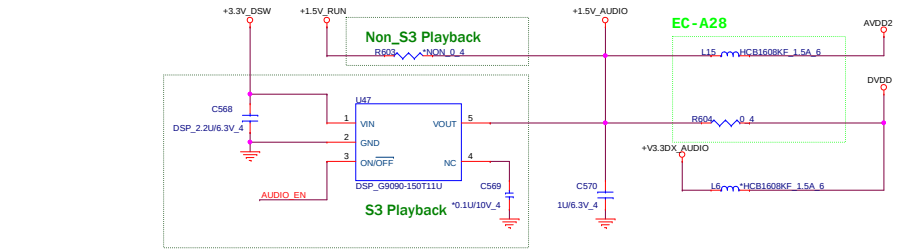


CODEC 5V POWER

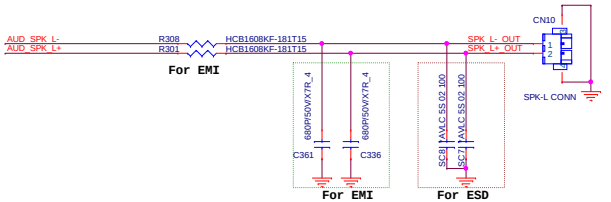


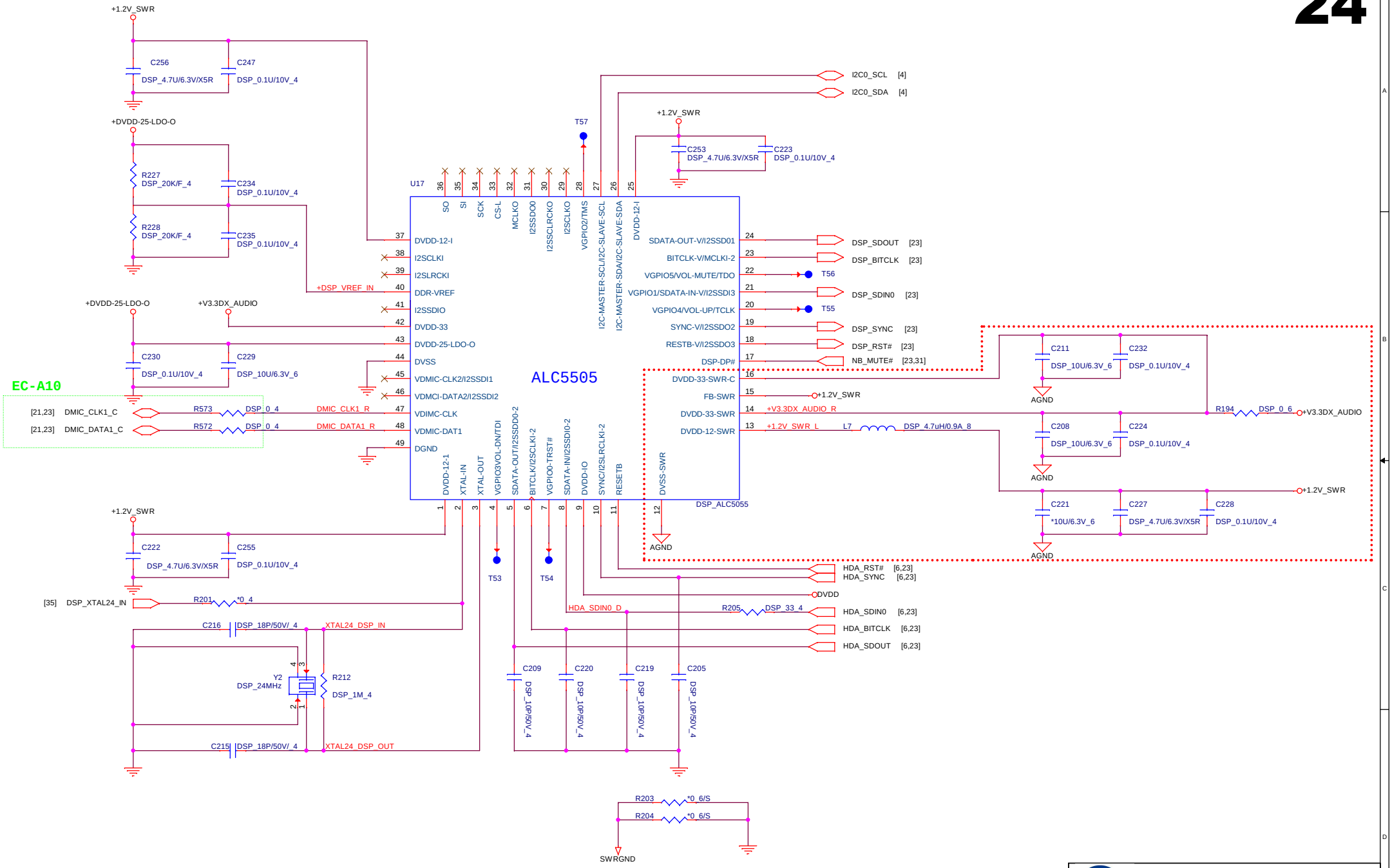
+3.3V_AUDIO_CODEC
Max Current : 419mA





INT Speaker





PROJECT : LZ9A			
Quanta Computer Inc.			
Size	Document Number		Rev
	DSP(ALC5055)		1A
Date: Thursday, January 03, 2013	Sheet 24 of 47		

[35,44] LANVCC
[4,6,8,12,17,23,28,30,32,38,43,46] +3.3V_DSW
[2,4,6,7,8,12,15,16,19,21,22,23,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN

LANVCC

+3.3V_DSW
Q4
AO3413
LANVCC
40 mils (Iout=1A)
40 mils (Iout=1A)
R4 4.7K_4
R37 *100K/F_4
C55 0.1U/10V_4
C51 10U/6.3V_6
C2 0.01U/16V/X7R_4

AOAC

[31,44] LAN_POWER
[8,44] SIO_SLP_LAN#
R46 0_4
R47 *0_4
Q7 LTC044EUBFS8TL

LANVCC
Trace width>60mil,
Trace length<200mil

U2 RTL8111GUS-CG

VDD10
R44 2.49K/F_4 RSET 10 mils
C28 *10P/50V/COG_4
C19 *10P/50V/COG_4
TP4 TP1 TP2
R38 0_4 LAN_XTAL25_IN [35]
C53 *6.8P/50V_4
XTAL2
Y1 *25MHZ +-30PPM
XTAL1
C44 *6.8P/50V_4
GND
MDI_0+ MDI_0- MDI_1+ MDI_1- MDI_2+ MDI_2-
MDIP0 MDIN0 AVDD10(NC) MDIN1 MDIP2(NC) MDIN2(NC) AVDD10
REGOUT VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP
REGOUT VDDREG/VDD33 VDD10
ISOLATEB
PCIE_WAKE# [8,28]
GPP_TX5N_LAN C12 0.1U/10V_4 PLTRST# [8,16,30]
GPP_TX5P_LAN C13 0.1U/10V_4 PCIE_RXN5 [5]
PCIE_RXP5 [5]
+3.3V_RUN
R11 1K_4
R12 15K_4
D2 RB500V-40
ISOLATEB LAN_ISOLATE [31]
MDI_3+ MDI_3-
CLK_PCIE_LANN [7]
CLK_PCIE_LANP [7]
PCIE_TXN5 [5]
PCIE_TXP5 [5]
PCIE_CLK_REQ3# [7]
LANVCC

For RTL8106E
* Place 1uF CAP close to each VDD10 pin-- 30 (reserve)

LANVCC
40 mils (Iout=1A)
C459 0.1U/10V_4
C477 0.1U/10V_4

For RTL8111GIS/RTL8106EUS
* Place 0.1uF CAP close to each VDD33 pin-- 11, 32

C5 *0.1U/10V_4
C10 *0.1U/10V_4

For RTL8106E
* Place 0.1uF CAP close to each VDD33 pin-- 23, 32

R10 0_8
40 mils (Iout=1A)
VDDREG/VDD33
C11 0.1U/10V_4
C6 4.7U/6.3V_6

Remove For Not Using SWR mode

REGOUT
40 mils (Iout=1A)
R367 *0_8
C21 *0.1U/10V_4

RTL8111G (LDO mode) support
RTL8106E (LDO mode) doesn't need

L22 4.7uH
C7 4.7U/6.3V_6
C476 0.1U/10V_4

RTL8111GUS/RTL8106EUS-CG
(SWR mode) support

For RTL8111G(S)
* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30 For RTL8106E
* Place 0.1uF CAP close to each VDD10 pin-- 8, 30
40 mils (Iout=1A)
C473 0.1U/10V_4
C475 0.1U/10V_4
C472 0.1U/10V_4
C474 0.1U/10V_4
VDD10
C8 *1U/6.3V_4
C429 *0.1U/10V_4
C42 *1U/6.3V_4
C426 *0.1U/10V_4

For RTL8111G(S)
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

Tramsformer

RJ45 Connector

U34 *CM1293A-04SO
U37 *CM1293A-04SO
MDI_0+_C MDI_0-_C MDI_1-_C MDI_1+_C
MDI_2+_C MDI_2-_C MDI_3-_C MDI_3+_C
LANVCC

Reserve for Surge
Line to GND TVS

U35 LAN_Transformer_NS892407
MDI_3- R82 1/F_4 MDI_3-_C
MDI_3+ R87 1/F_4 MDI_3+_C
MDI_2- R75 1/F_4 MDI_2-_C
MDI_2+ R71 1/F_4 MDI_2+_C
MDI_1- R64 1/F_4 MDI_1-_C
MDI_1+ R53 1/F_4 MDI_1+_C
MDI_0- R48 1/F_4 MDI_0-_C
MDI_0+ R42 1/F_4 MDI_0+_C
TD4- TD4+ TCT4 TD3- TD3+ TCT3 TD2- TD2+ TCT2 TD1- TD1+ TCT1
MX4- MX4+ MCT4 MX3- MX3+ MCT3 MX2- MX2+ MCT2 MX1- MX1+ MCT1
LAN_MX3- LAN_MX3+ LAN_MCT0 LAN_MX2- LAN_MX2+ LAN_MCT1 LAN_MX1- LAN_MX1+ LAN_MCT2 LAN_MX0- LAN_MX0+ LAN_MCT3

Layout:All termination signal should have 30 mil trace

R80 75/F_12 LANCT3
R70 75/F_12
R54 75/F_12
R45 75/F_12
R90 0_12
D16 *BS4200N-C_1812
C494 10P/3KV/NPO_1808
R106 1M_8
C478 0.01U/50V/X7R_4

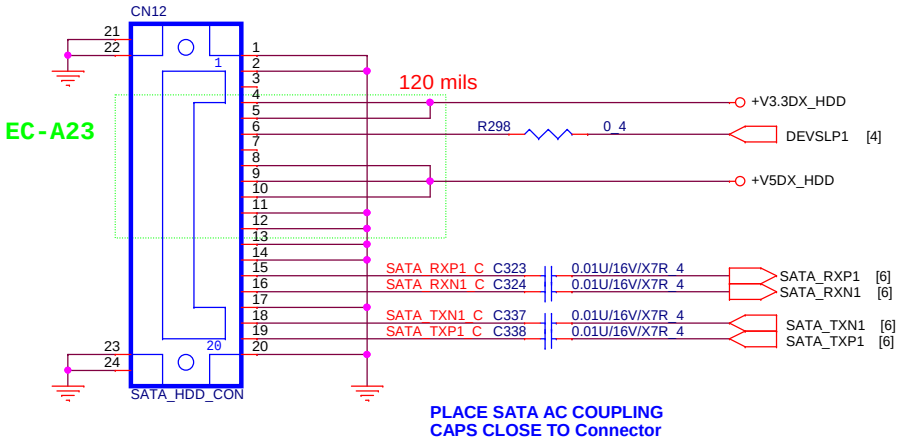
CN1
LAN_MX0+ LAN_MX0- LAN_MX1+ LAN_MX2+ LAN_MX2- LAN_MX1- LAN_MX3+ LAN_MX3-
LAN_RJ45

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	LAN(RTL8111GUS)	1A
Date: Thursday, January 03, 2013	Sheet 25 of 47	

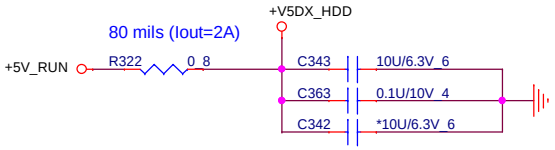
HDD

[2,4,6,7,8,12,15,16,19,21,22,23,25,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[21,22,23,32,34,37,42,43,44] +5V_RUN

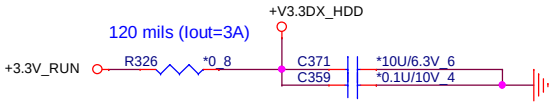


PLACE SATA AC COUPLING
CAPS CLOSE TO Connector

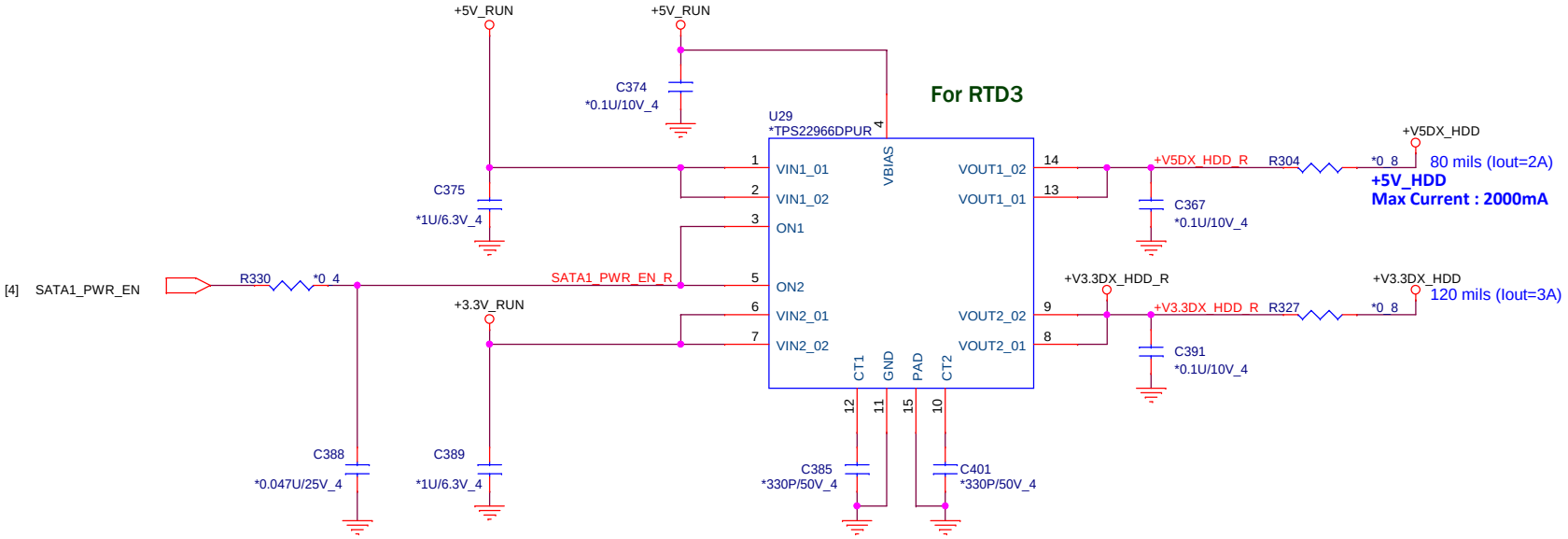
DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



For RTD3

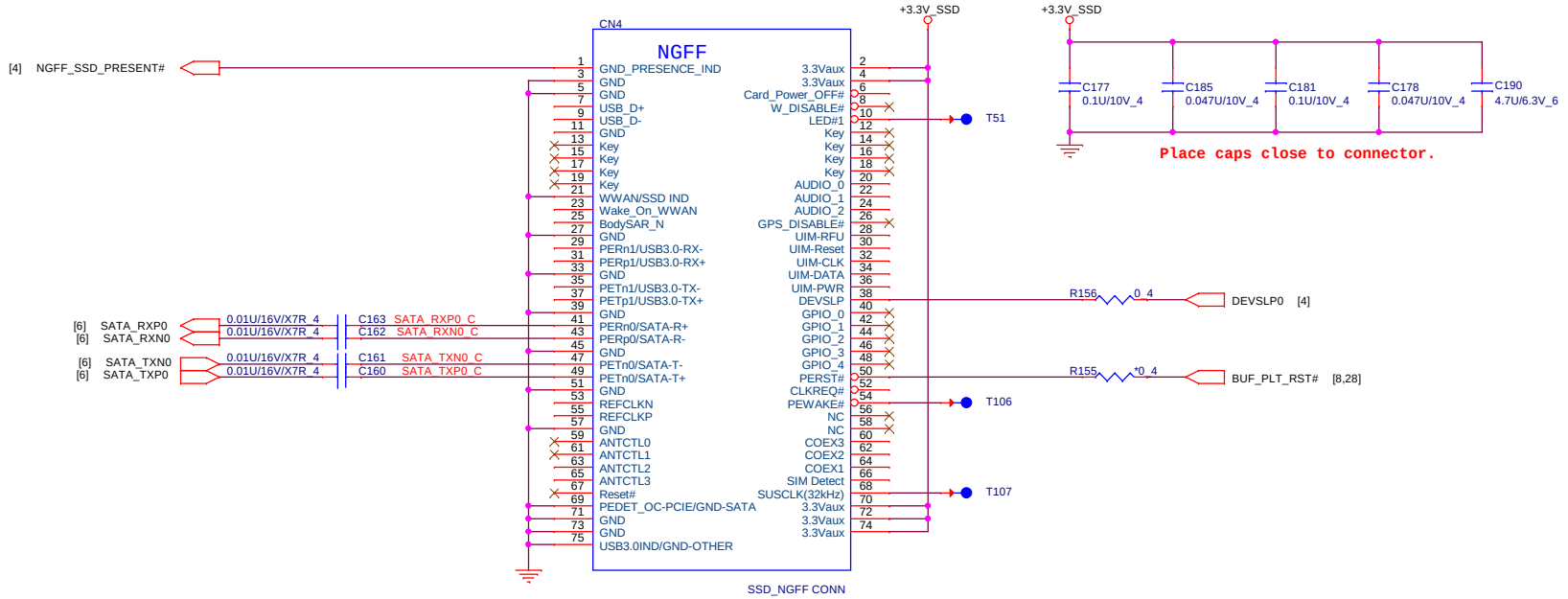


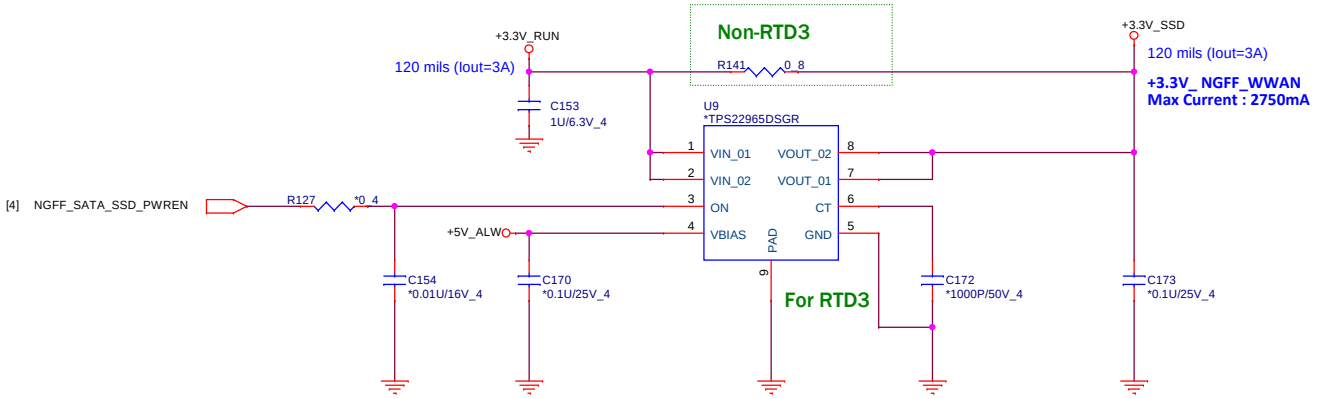
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	SATA	1A
Date: Thursday, January 03, 2013	Sheet 26 of 47	

[2,4,6,7,8,12,15,16,19,21,22,23,25,26,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN

NGFF SSD connector





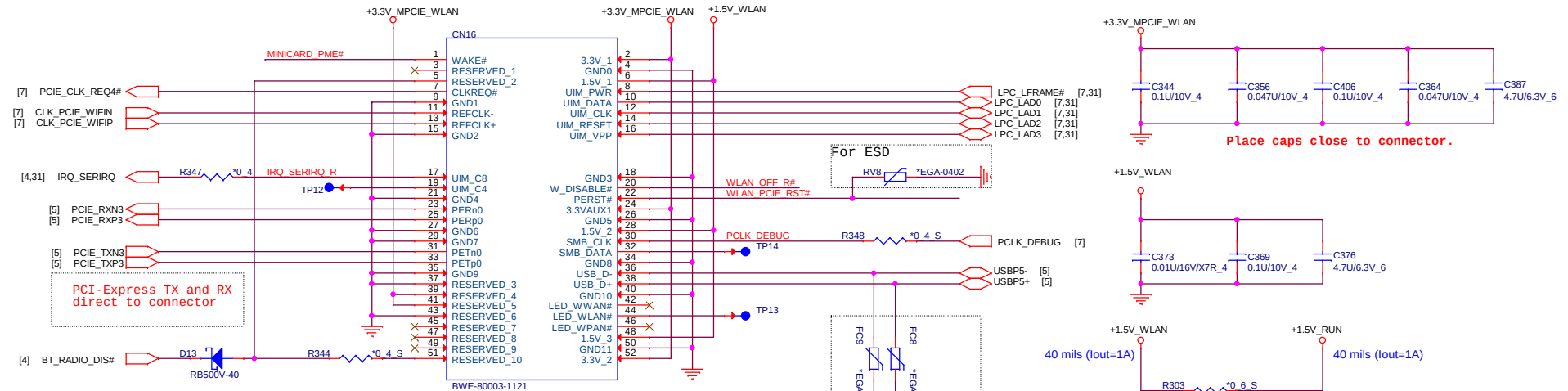
PROJECT : LZ9A

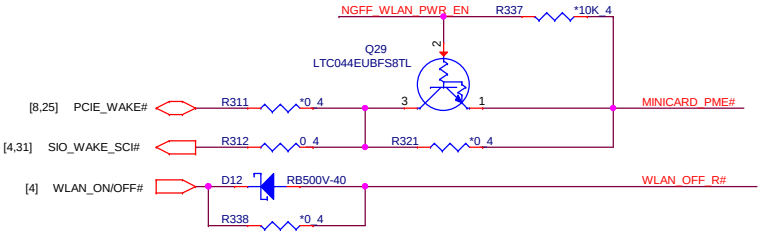
Quanta Computer Inc.

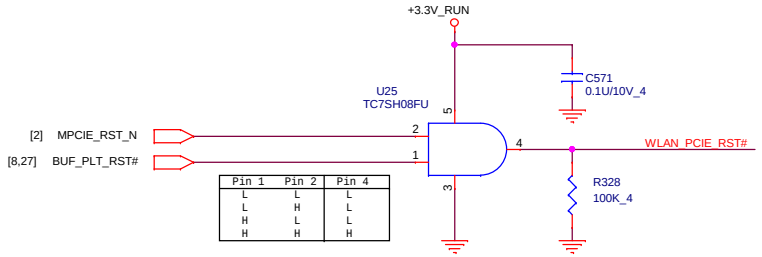
Size	Document Number	Rev
	SSD NGFF	1A
Date: Thursday, January 03, 2013	Sheet 27 of 47	

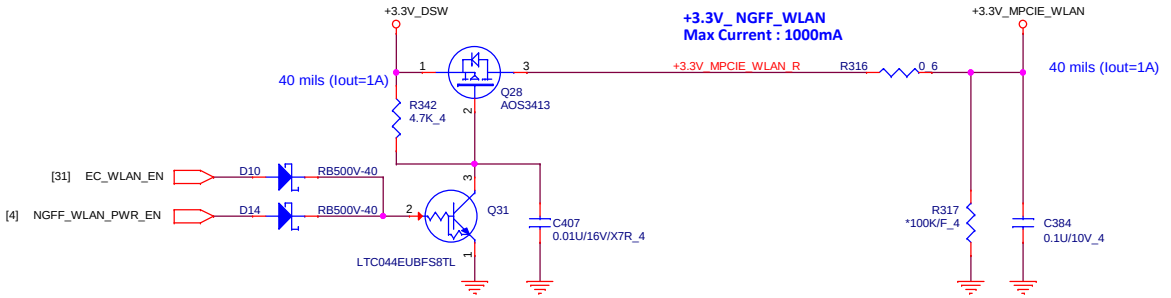
Mini PCIE Wifi/BT connector

[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[4,6,8,12,17,23,25,30,32,38,43,46] +3.3V_DSW
[12,23,41,44,46] +1.5V_RUN



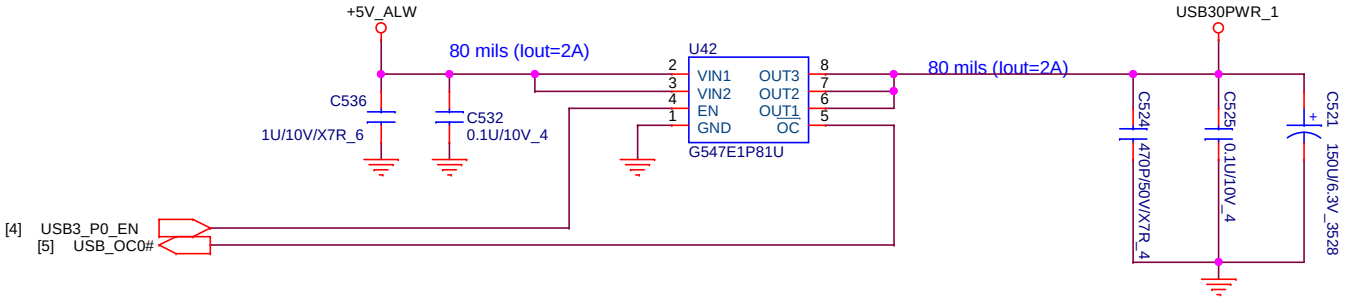


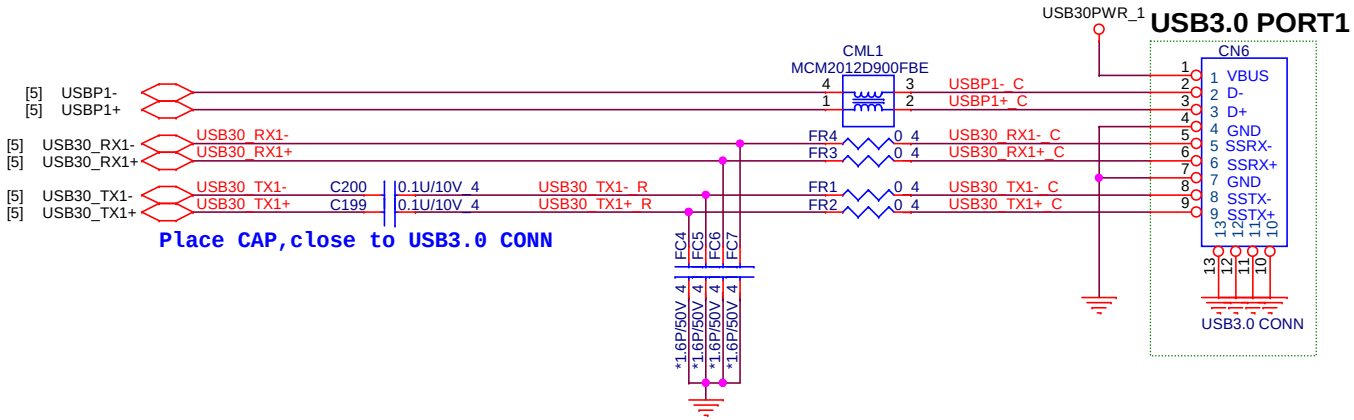


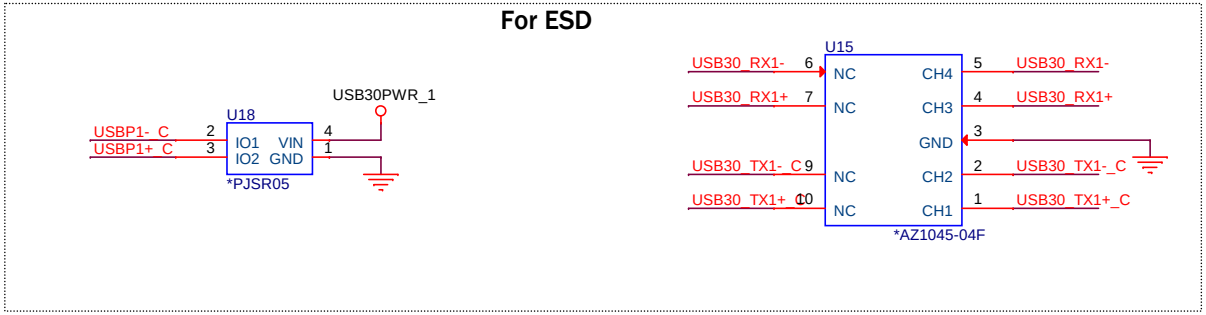


PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Wifi/BT MiniPCIE	1A
Date: Thursday, January 03, 2013	Sheet 28 of 47	





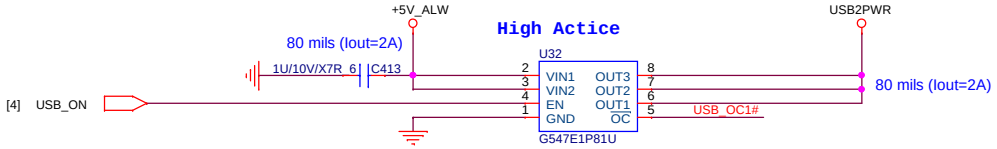


PROJECT : LZ9A

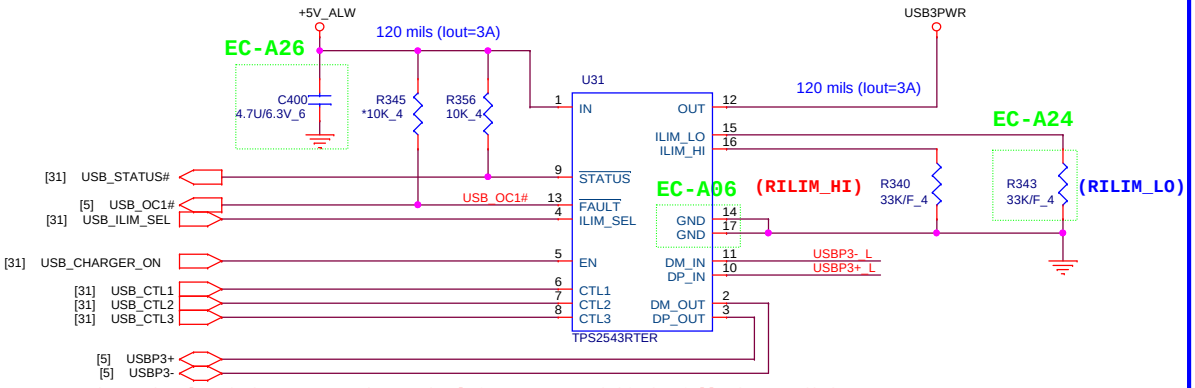
Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x1	1A
Date: Thursday, January 03, 2013	Sheet 29 of 47	

USB 2.0 Port



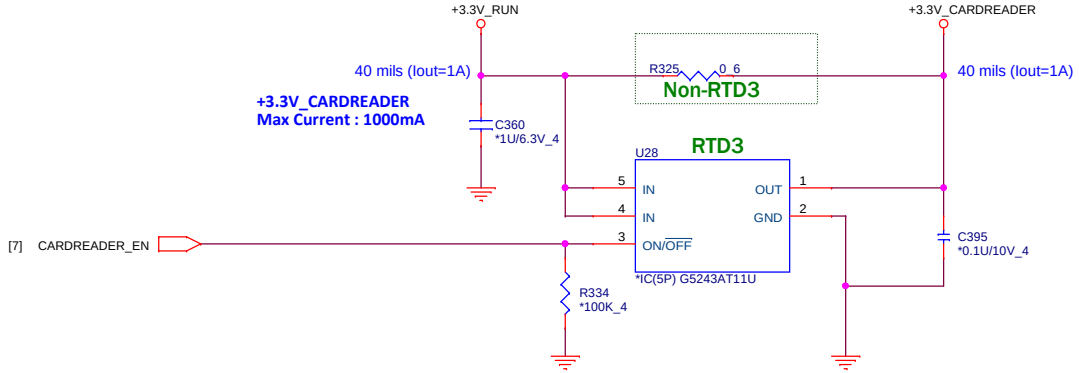
USB Charger 2.0 Port



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

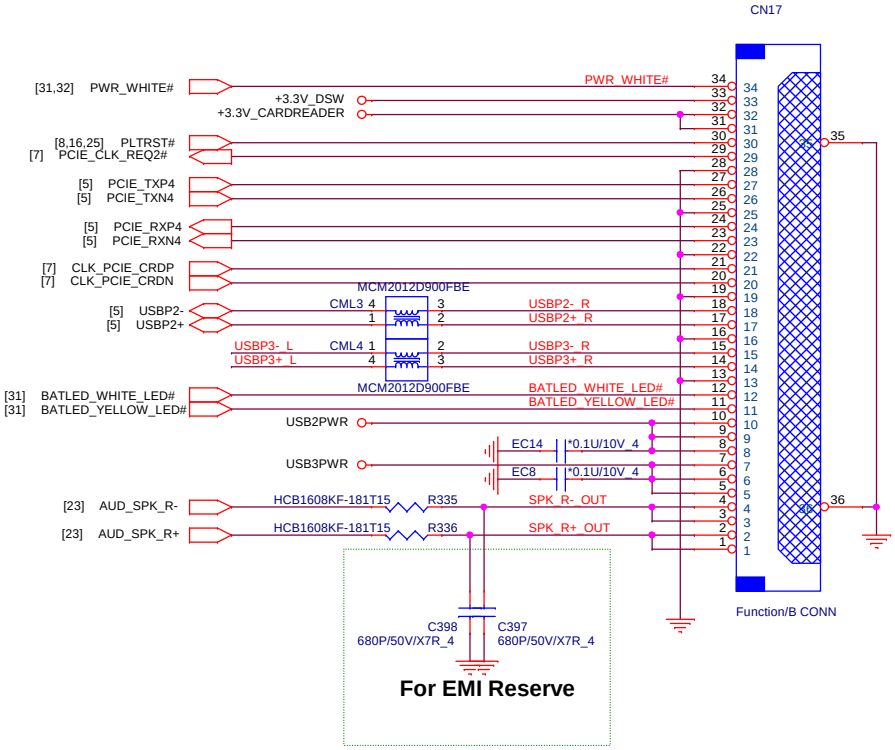
$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

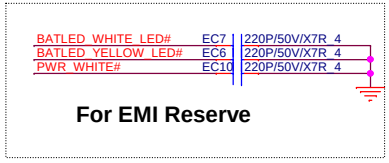
Card Reader VCC Control



[15,17,23,27,29,38,39,40,41,43,44,45,46] +5V_ALW
[4,6,8,12,17,23,25,28,32,38,43,46] +3.3V_DSW
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,31,32,33,34,37,42,43,44] +3.3V_RUN

30





PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	USB2.0--Audio Jack Conn	1A
Date: Thursday, January 03, 2013	Sheet 30 of 47	

IT8587

Power Rails

- +3.3V_ALW2
- +3.3V_RUN
- +3.3V_RUN_EC
- IT8512_VSTBY
- RTC_VCC
- RTC_VCC_L
- +RTC_CELL
- IT8512_AVCC
- VBAT
- AVCC
- VSTBY
- VSS
- AVSS
- VCORE

Clock

- CK32KE/GPJ7
- CK32K/GPJ6
- GPJ1(X)
- GPJ0(X)

LPC

- LAD0/GPM0(X)
- LAD1/GPM1(X)
- LAD2/GPM2(X)
- LAD3/GPM3(X)
- LPCRST#/WUI4/GPD2(Up)
- LPCCLK/GPM4(X)
- LFRAME#/GPM5(X)
- LPCPD#/WUI6/GPE6(Dn)
- GA20/GPB5(X)
- SERIRQ/GPM6(X)
- ECSMI#/GPD4(Up)
- ECSCI#/GPD3(Up)
- WRST#
- KBRST#/GPB6(X)
- PWUREQ#/BBO/SMCLK2ALT/GPC7(Up)/SMCLK2ALT
- CRX0/GPC0(Dn)
- CTX0/TMA0/GPB2(Dn)

GPIO

- EGCLK/WUI27/GPE3(Dn)
- EGDI/WUI26/GPE2(Dn)
- EGDO/WUI25/GPE1(Dn)
- L80HLAT/BAO/WUI24/GPE0(Dn)
- L80LLAT/WUI7/GPE7(Up)
- WUI42/GPH6/ID6(Dn)
- WUI41/GPH5/ID5(Dn)
- WUI40/GPH4/ID4(Dn)
- WUI39/GPH3/ID3(Dn)
- WUI16/GPH0/ID0(Dn)
- CLKRUN#/WUI16/GPH0/ID0(Dn)

SM BUS

- SMCLK0/GPB3(X)
- SMDAT0/GPB4(X)
- SMCLK1/GPC1(X)
- SMDAT1/GPC2(X)
- PECI/SMCLK2/WUI22/GPF6(Up)
- SMDAT2/WUI23/GPF7(Up)

PS/2

- PS2CLK0/TMB0/CEC/GPF0(Up)
- PS2DAT0/TMB1/GPF1(Up)
- PS2CLK2/WUI20/GPF4(Up)
- PS2DAT2/WUI21/GPF5(Up)

PWM

- PWM0/GPA0(Up)
- PWM1/GPA1(Up)
- PWM2/GPA2(Up)
- PWM3/GPA3(Up)
- PWM4/GPA4(Up)
- PWM5/GPA5(Up)

CIR

- DAC4/DCD0#/GPJ4(X)
- DSR0#/GPC6(X)
- GINT/CTS0#/GPD5(Up)
- PS2DAT1/RTS0#/GPF3(Up)
- DAC5/RIG0#/GPJ5(X)
- PS2CLK1/DTR0#/GPF2(Up)
- TXD/SOUT0/GPB1(Up)
- RXD/SIN0/GPB0(Up)

UART port

- ADC5/DCD1#/WUI29/GPI5(X)
- ADC6/DSR1#/WUI30/GPI6(X)
- ADC7/CTS1#/WUI31/GPI7(X)
- RTS1#/WUI5/GPE5(Dn)
- PWM7/RIG1#/GPA7(Up)
- DTR1#/SBUSY/GPG1/ID7(Dn)
- CTX1/WUI18/SQUT1/GPH2/SMDAT3/ID2(Dn)
- CRX1/WUI17/SIN1/SMCLK3/GPH1/ID1(Dn)

WAKE UP

- PWRSW/GPE4(Up)
- RI1#/WUI0/GPD0(Up)
- RI2#/WUI1/GPD1(Up)
- RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7(Dn)

EXTERNAL SERIAL FLASH

- FSCK/GPG7
- FSCE#/GPG3
- FMOSI/GPG4
- FMISO/GPG5

SPI ENABLE

- SSCE0#/GPG2(X)
- SSCE1#/GPG0(X)

KBMX

- KSO0/PD0
- KSO1/PD1
- KSO2/PD2
- KSO3/PD3
- KSO4/PD4
- KSO5/PD5
- KSO6/PD6
- KSO7/PD7
- KSO8/ACK#
- KSO9/BUSY
- KSO10/PE
- KSO11/ERR#
- KSO12/SLCT
- KSO13
- KSO14
- KSO15
- KSO16/SMOSI/GPC3(Dn)
- KSO17/SMISO/GPC5(Dn)
- PWM6/SSCK/GPA6(Up)

A/D D/A

- ADC0/GPI0(X)
- ADC1/GPI1(X)
- ADC2/GPI2(X)
- ADC3/GPI3(X)
- ADC4/WUI28/GPI4(X)
- TACH2/GPJ0(X)
- DAC2/TACH0B/GPJ2(X)
- DAC3/TACH1B/GPJ3(X)

Signals

- VGA_OVT#
- SIO_WAKE_SCI#
- S5_ON_5V
- EC_PWROK
- USB_CTL3
- USB_CTL2
- USB_CTL1
- USB_STATUS#
- CLKRUN#_R
- SMBCLK0
- SMBDAT0
- MBCLK_THRM
- MBDATA_THRM
- PECI_EC
- R276 43_4
- LAN_ISOLATE
- USB_ILIM_SEL
- TPCLK
- TPDATA
- R314 10K_4
- R315 10K_4
- PWR_WHITE
- FB_CLAMP
- FAN_PWM_R
- KB_LIGHT
- GSENSOR_ON
- BEEP
- FANSIG_R
- FB_CLAMP_TGL_REQ_EC#
- USB_CHARGER_ON
- HWPG
- C286 *0.1U/10V_4
- NBSWON#
- SIO_SLP_S3#
- ACAV_IN
- ADAPTER_ID
- TEMP_MBAT
- ACDC_ID
- IINP
- GSENSOR_Z
- GSENSOR_X
- R354 0_4
- H_PROCHOT_EC
- SLP_SUS#
- DPWROK
- SUS_STAT#
- TP10
- EC_SLP_S4#
- SUSACK#
- R273 *0_4
- C380 *1U/6.3V/X5R_4
- C381 0.1U/10V_4
- CLKRUN#
- R309 0_4
- SIO_WAKE_SCI#
- S5_ON_5V
- GFXON
- EC_PWROK
- SMBCLK0
- SMBDAT0
- MBCLK_THRM
- MBDATA_THRM
- PECI_EC_R
- NB_MUTE#
- LAN_ISOLATE
- USB_ILIM_SEL
- TPCLK
- TPDATA
- +3.3V_RUN
- FB_CLAMP
- FAN_PWM_R
- KB_LIGHT
- GSENSOR_ON
- BEEP
- FANSIG_R
- FB_CLAMP_TGL_REQ_EC#
- USB_CHARGER_ON
- HWPG
- NBSWON#
- SIO_SLP_S3#
- ACAV_IN
- ADAPTER_ID
- TEMP_MBAT
- ACDC_ID
- IINP
- GSENSOR_Z
- GSENSOR_X
- SLP_SUS#
- DPWROK
- SUS_STAT#
- EC_SLP_S4#
- SUSACK#
- CLKRUN#
- SMBCLK0
- SMBDAT0
- MBCLK_THRM
- MBDATA_THRM
- PECI_EC_R
- NB_MUTE#
- LAN_ISOLATE
- USB_ILIM_SEL
- TPCLK
- TPDATA
- +3.3V_RUN
- FB_CLAMP
- FAN_PWM_R
- KB_LIGHT
- GSENSOR_ON
- BEEP
- FANSIG_R
- FB_CLAMP_TGL_REQ_EC#
- USB_CHARGER_ON
- HWPG
- NBSWON#
- SIO_SLP_S3#
- ACAV_IN
- ADAPTER_ID
- TEMP_MBAT
- ACDC_ID
- IINP
- GSENSOR_Z
- GSENSOR_X
- SLP_SUS#
- DPWROK
- SUS_STAT#
- EC_SLP_S4#
- SUSACK#
- CLKRUN#
- LPC_LAD0
- LPC_LAD1
- LPC_LAD2
- LPC_LAD3
- LID#
- CLKOUT_LPC_0
- LPC_LFRAME#
- RUN_ON
- SUSWARN#
- IRQ_SERIRQ
- SMC_EXTSMI_N
- SIO_EXT_SCI#
- SIO_RCIN#
- CAPSLED#
- SC34 *0.1U/10V_4
- S5_ON
- LAN_POWER
- SIO_PWRBTN#
- EC_APWROK
- RSMRST#
- SLP_S0#
- PM_BATLOW_N
- SIO_SLP_S5#
- BATLED_YELLOW_LED#
- BATLED_WHITE_LED#
- GSENSOR_Y
- VCORE_IMON_EC
- NOVO_BTN#
- NOVO_BTN#
- AC_PRESENT
- GSENSOR_TST#
- SLP_S4#
- VCCST_PWRGD#
- 8512_SCK
- 8512_SCE#
- 8512_SI
- 8512_SO
- SYS_PWROK_EC
- EC_WLAN_EN
- BOARD_ID
- ME_WR#
- MY[0..15]
- MX[0..7]
- SYS_SHDN#
- VGA_OVT#
- SIO_WAKE_SCI#
- S5_ON_5V
- EC_PWROK
- USB_CTL3
- USB_CTL2
- USB_CTL1
- USB_STATUS#
- CLKRUN#
- SMBCLK0
- SMBDAT0
- MBCLK_THRM
- MBDATA_THRM
- PECI_EC_R
- NB_MUTE#
- LAN_ISOLATE
- USB_ILIM_SEL
- TPCLK
- TPDATA
- +3.3V_RUN
- FB_CLAMP
- FAN_PWM_R
- KB_LIGHT
- GSENSOR_ON
- BEEP
- FANSIG_R
- FB_CLAMP_TGL_REQ_EC#
- USB_CHARGER_ON
- HWPG
- NBSWON#
- SIO_SLP_S3#
- ACAV_IN
- ADAPTER_ID
- TEMP_MBAT
- ACDC_ID
- IINP
- GSENSOR_Z
- GSENSOR_X
- SLP_SUS#
- DPWROK
- SUS_STAT#
- EC_SLP_S4#
- SUSACK#
- CLKRUN#
- SMBCLK0
- SMBDAT0
- MBCLK_THRM
- MBDATA_THRM
- PECI_EC_R
- NB_MUTE#
- LAN_ISOLATE
- USB_ILIM_SEL
- TPCLK
- TPDATA
- +3.3V_RUN
- FB_CLAMP
- FAN_PWM_R
- KB_LIGHT
- GSENSOR_ON
- BEEP
- FANSIG_R
- FB_CLAMP_TGL_REQ_EC#
- USB_CHARGER_ON
- HWPG
- NBSWON#
- SIO_SLP_S3#
- ACAV_IN
- ADAPTER_ID
- TEMP_MBAT
- ACDC_ID
- IINP
- GSENSOR_Z
- GSENSOR_X
- SLP_SUS#
- DPWROK
- SUS_STAT#
- EC_SLP_S4#
- SUSACK#
- CLKRUN#

Notes

- Layout Note: net "+3.3V_ALW2" and "RTC_VCC" minimum trace width 12mils.
- Layout Note: Place all capacitors close to IT8512.
- EMI suggestion: Add a 15p bypass CAP on CLK_PCI_8512
- For EMI, Close EC. pin74
- EC-A29
- (For PLL Power)
- For ESD
- EC-A25
- EC-A46
- EC-A22
- FOR EC auto load code

For EC E-flash(embedded flash) auto load code

Note:
IT8587 with 128K-byte e-flash
Auto load code condition:
1. Let PCH SPI interface in High-Z state.
2. RSMRST# pull low
   (PCH SPI pins are tri-stated prior to RSMRST# de-assertion)
3. EC pin 100(GPG2) pull high(force EC load code)
4. Supply power to SPI flash ROM,PCH(VCCSPI,+1.05V_SUS) and EC

NOVO BUTTON

POWER SWITCH

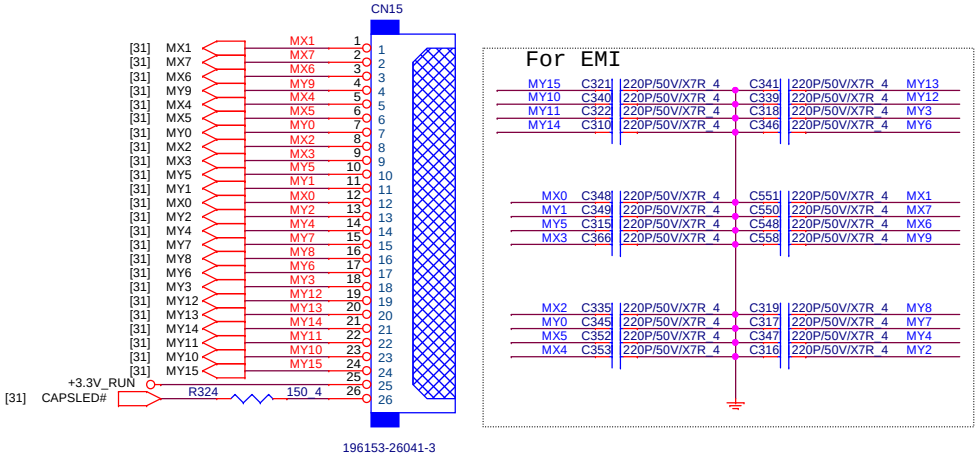
EC Board ID

Thermal reset function

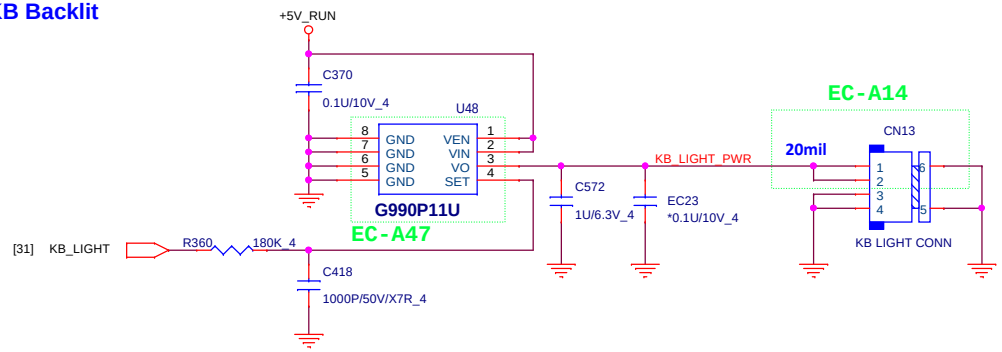
EC reset function, press power button 8 sec

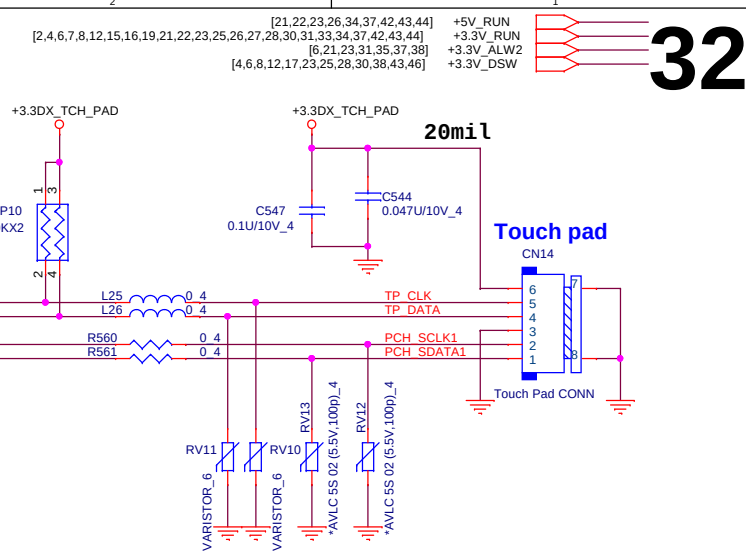
Project	LZ9A
Quanta Computer Inc.	
Size	Custom
Document Number	KBC IT8587
Rev	1A
Date	Thursday, January 03, 2013
Sheet	31 of 47

KEYBOARD

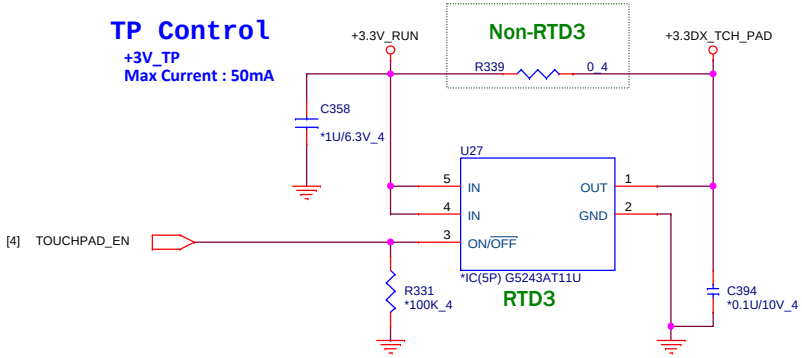


KB Backlit

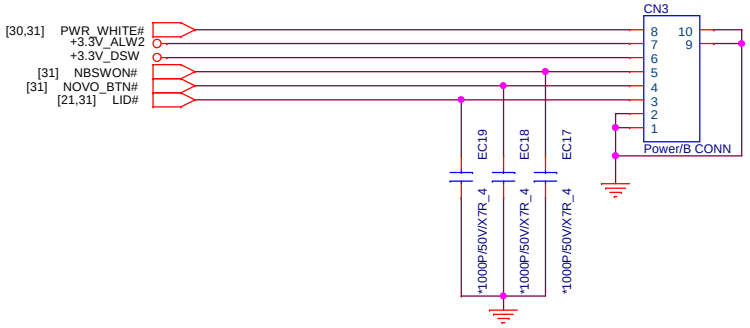




TP Control



Power Board CONN



PROJECT : LZ9A

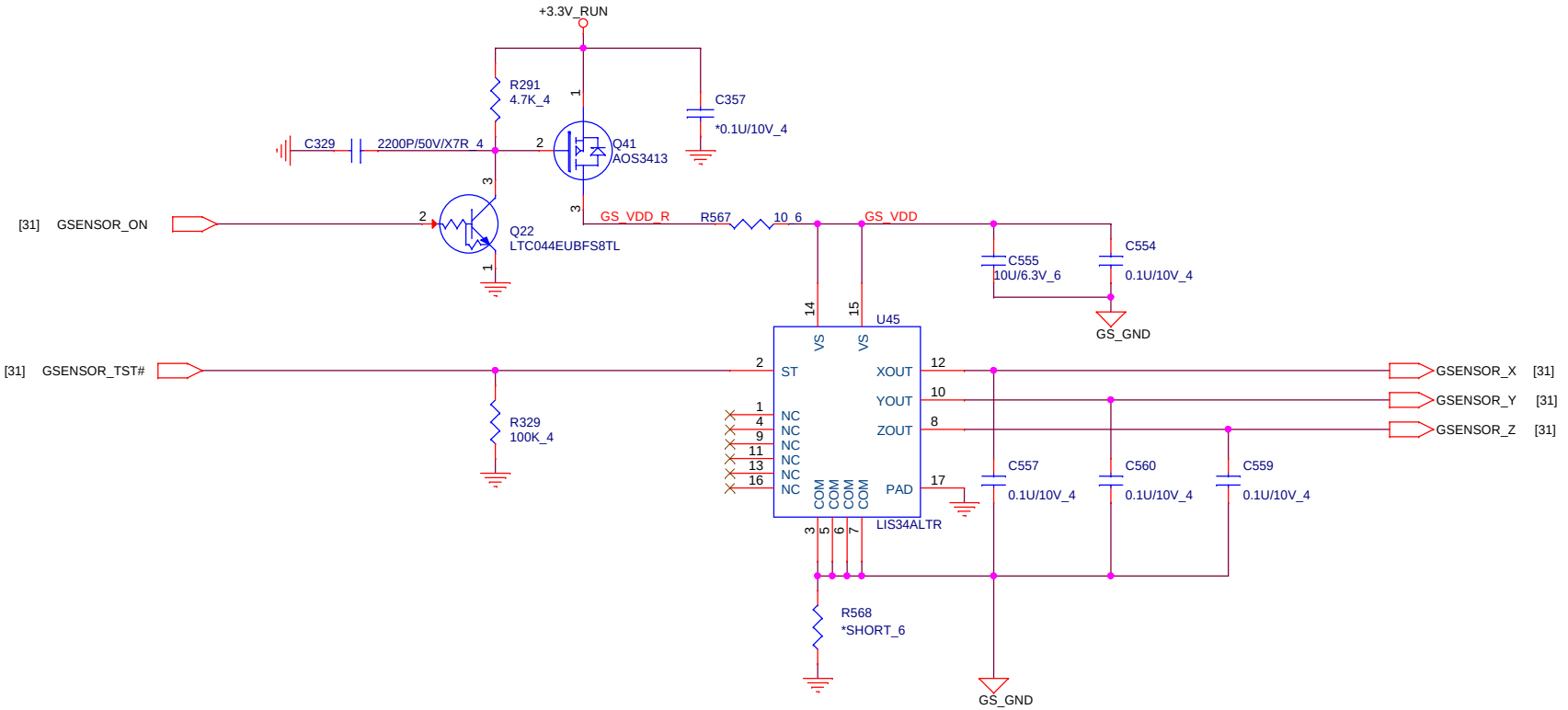
Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/LID	1A

Date: Thursday, January 03, 2013 Sheet 32 of 47

G-SENSOR (3-Axial)

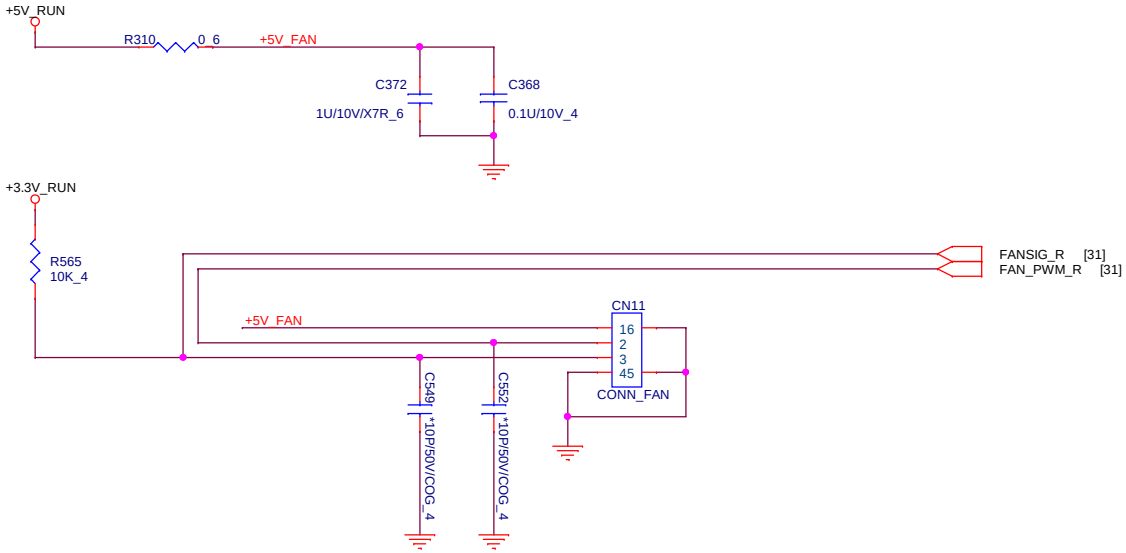
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,34,37,42,43,44] +3.3V_RUN



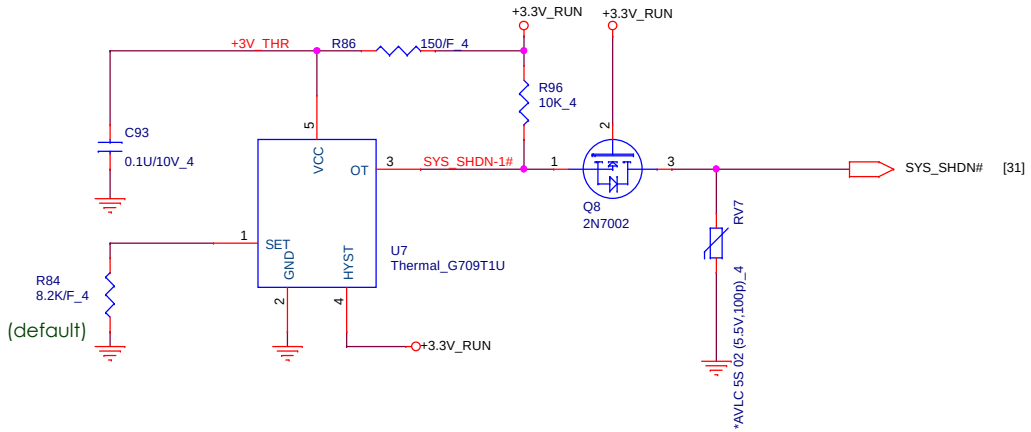
PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: G-sensor	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 33 of 47	

FAN CONTROL

[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,37,42,43,44] +3.3V_RUN
[21,22,23,26,32,37,42,43,44] +5V_RUN



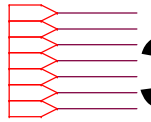
Thermal Sensor



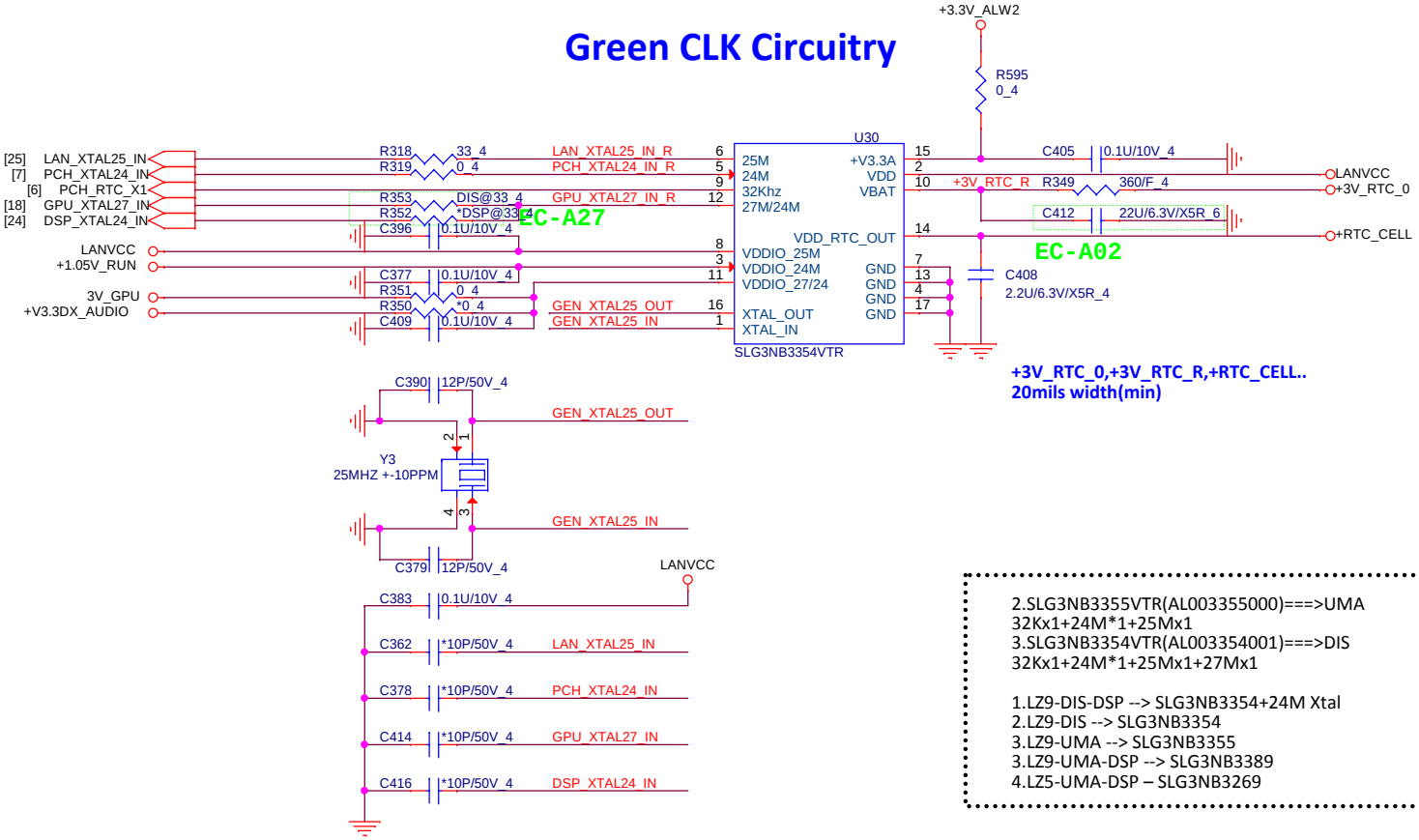
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal	1A
Date: Thursday, January 03, 2013	Sheet 34 of 47	

[6,21,23,31,32,37,38] +3.3V_ALW2
[25,44] LANVCC
[6] +3V_RTC_0
[6,12,31] +RTC_CELL
[6,9,12,40,44,46] +1.05V_RUN
[16,17,19,45,46,47] 3V_GPU
[21,23,24] +V3.3DX_AUDIO



Green CLK Circuitry



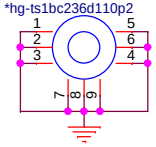
2.SLG3NB3355VTR(AL003355000)===>UMA
32Kx1+24M*1+25Mx1
3.SLG3NB3354VTR(AL003354001)===>DIS
32Kx1+24M*1+25Mx1+27Mx1

1.LZ9-DIS-DSP --> SLG3NB3354+24M Xtal
2.LZ9-DIS --> SLG3NB3354
3.LZ9-UMA --> SLG3NB3355
3.LZ9-UMA-DSP --> SLG3NB3389
4.LZ5-UMA-DSP – SLG3NB3269

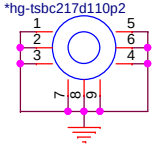
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Green Clock	1A
Date: Thursday, January 03, 2013	Sheet 35 of 47	

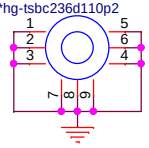
HOLE15
*hg-ts1bc236d110p2



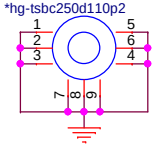
HOLE16
*hg-tsbc217d110p2



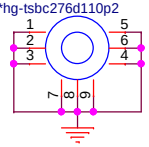
HOLE17
*hg-tsbc236d110p2



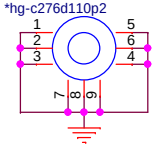
HOLE18
*hg-tsbc250d110p2



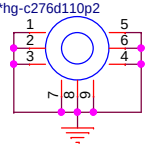
HOLE19
*hg-tsbc276d110p2



HOLE20
*hg-c276d110p2



HOLE21
*hg-c276d110p2



CPU HOLE

HOLE5
*H-C197D142P2

HOLE6
*H-C197D142P2

WLAN HOLE

HOLE13
*H-TC217BIC142D102P2

HOLE12
*H-TC217BIC142D102P2

VGA HOLE

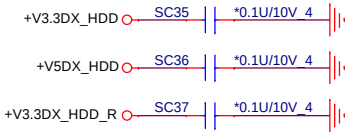
HOLE1
*H-TC236BIC142D142N

HOLE8
*H-TC236BIC142D142N

SSD HOLE

HOLE14
*H-TC217BIC142D102P2

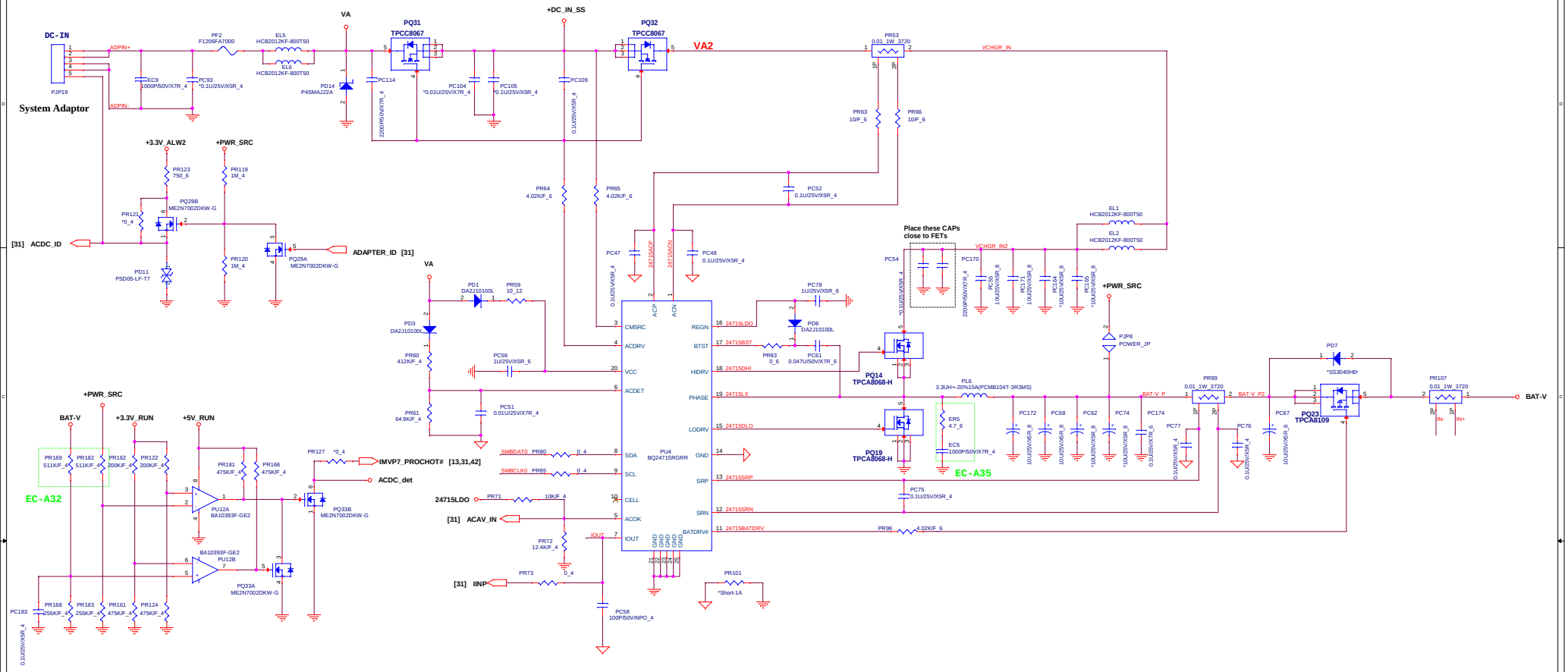
ESD



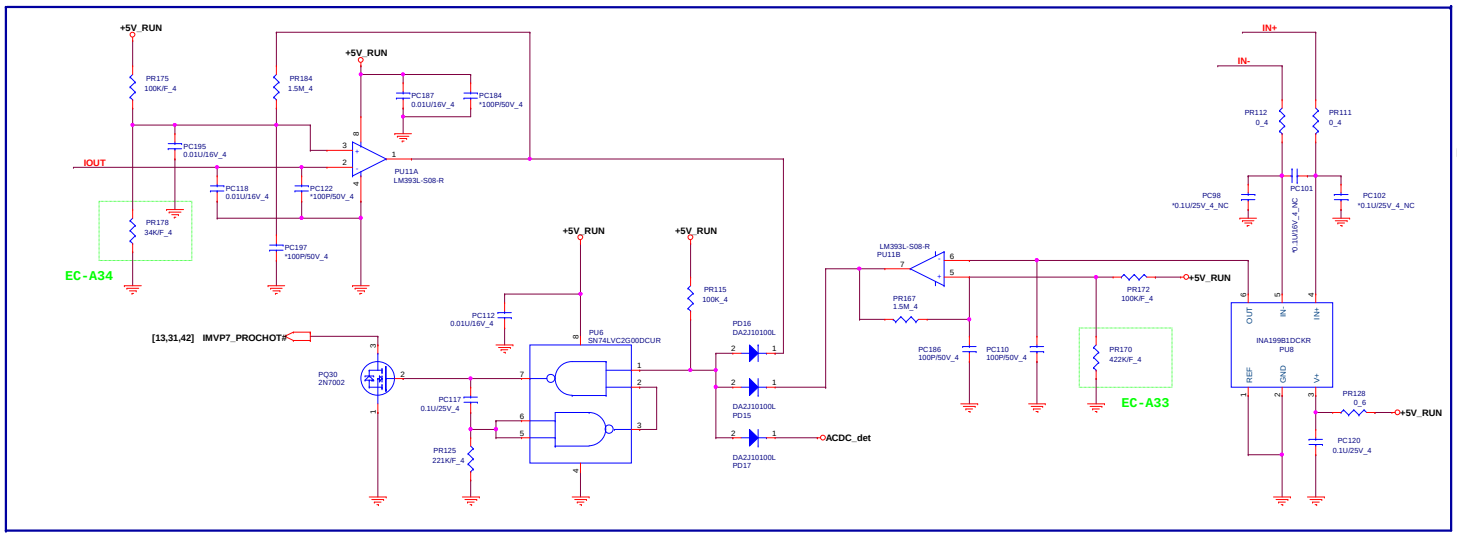
PROJECT : LZ9A
Quanta Computer Inc.

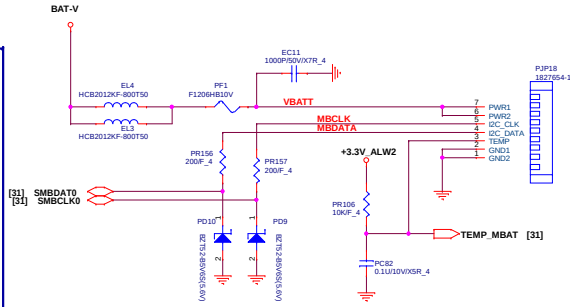
Size	Document Number	Rev
	Screw Hole/EMI	1A
Date: Thursday, January 03, 2013	Sheet 36 of 47	

[21,38,39,40,41,42,45] +PWR_SRC
[6,21,23,31,32,35,38] +3.3V_ALW2



10ms one-shot circuit





PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER (BQ24715)	1A
Date: Thursday, January 03, 2013	Sheet 37 of 47	

[21,37,39,40,41,42,45] +PWR_SRC
[4,6,8,12,17,23,25,28,30,32,43,46] +3.3V_DSW
[15,17,23,27,29,30,39,40,41,43,44,45,46] +5V_ALW
[6,21,23,31,32,35,37] +3.3V_ALW2
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44] +3.3V_RUN
[12,43,46] +15V_ALW

+5V_ALW
5 Volt +/-5%
Fsw : 400KHz
TDC : 7A
OCP : 10A

+3.3V_DSW
3.3 Volt +/-5%
Fsw : 475KHz
TDC : 8A
OCP: 11A

Place these CAPs close to FETs

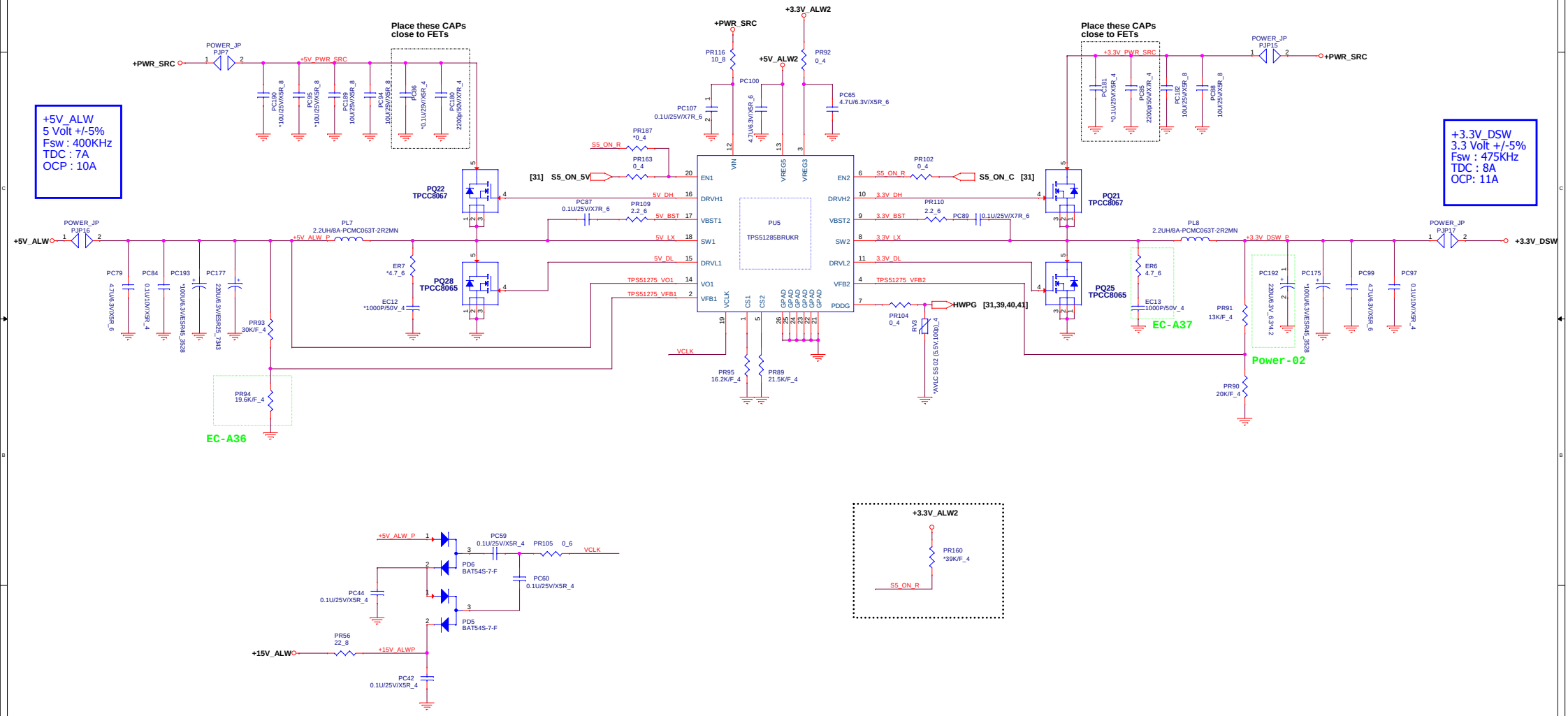
Place these CAPs close to FETs

PU5 TPS51285BRUKR

PQ22 TPCC8067
PQ28 TPCC8065
PQ21 TPCC8067
PQ25 TPCC8065

PL7 2.2UH/8A-PCMC063T-2R2MN
PL8 2.2UH/8A-PCMC063T-2R2MN

EC-A36
EC-A37
Power-02



PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	3V/5V (TPS51285)	1A

Date: Thursday, January 03, 2013 Sheet 38 of 47

[21,37,38,40,41,42,45] +PWR_SRC
[9,14,15,44] +V_VDDQ_VR
[15,17,23,27,29,30,38,40,41,43,44,45,46] +5V_ALW
[14,15,44] +0.675V_DDR_VTT
[15] +DDR_VTTREF

+V_VDDQ_VR
1.35 Volt +/-5%
Fsw : 400KHz
TDC : 7A
OCP : 12A

+0.675V_DDR_VTT
TDC : 1A

EC-A38

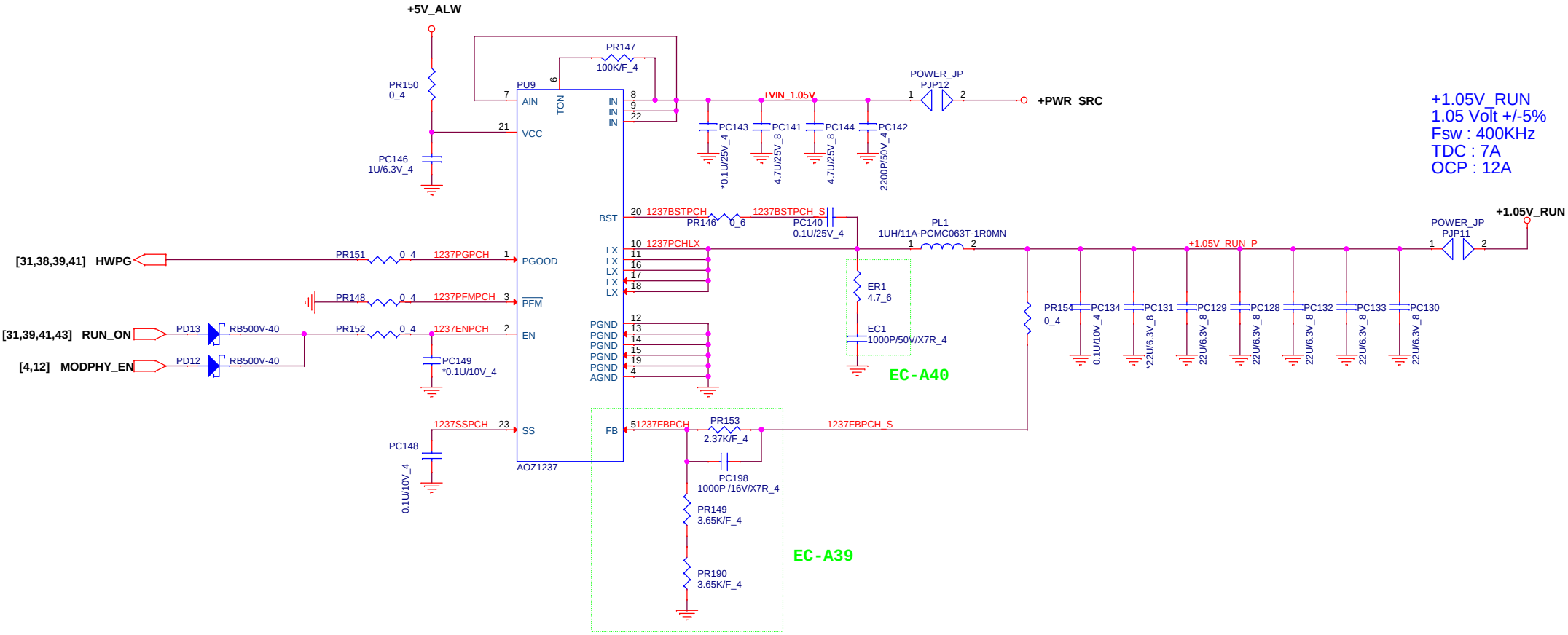
PU10 AOZ1237
PU7 TPS51206DSQR

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	1.35V_DDR/0.675 (AOZ1237)	1A

Date: Thursday, January 03, 2013 Sheet 39 of 47

[21,37,38,39,41,42,45] +PWR_SRC
[6,9,12,35,44,46] +1.05V_RUN
[15,17,23,27,29,30,38,39,41,43,44,45,46] +5V_ALW

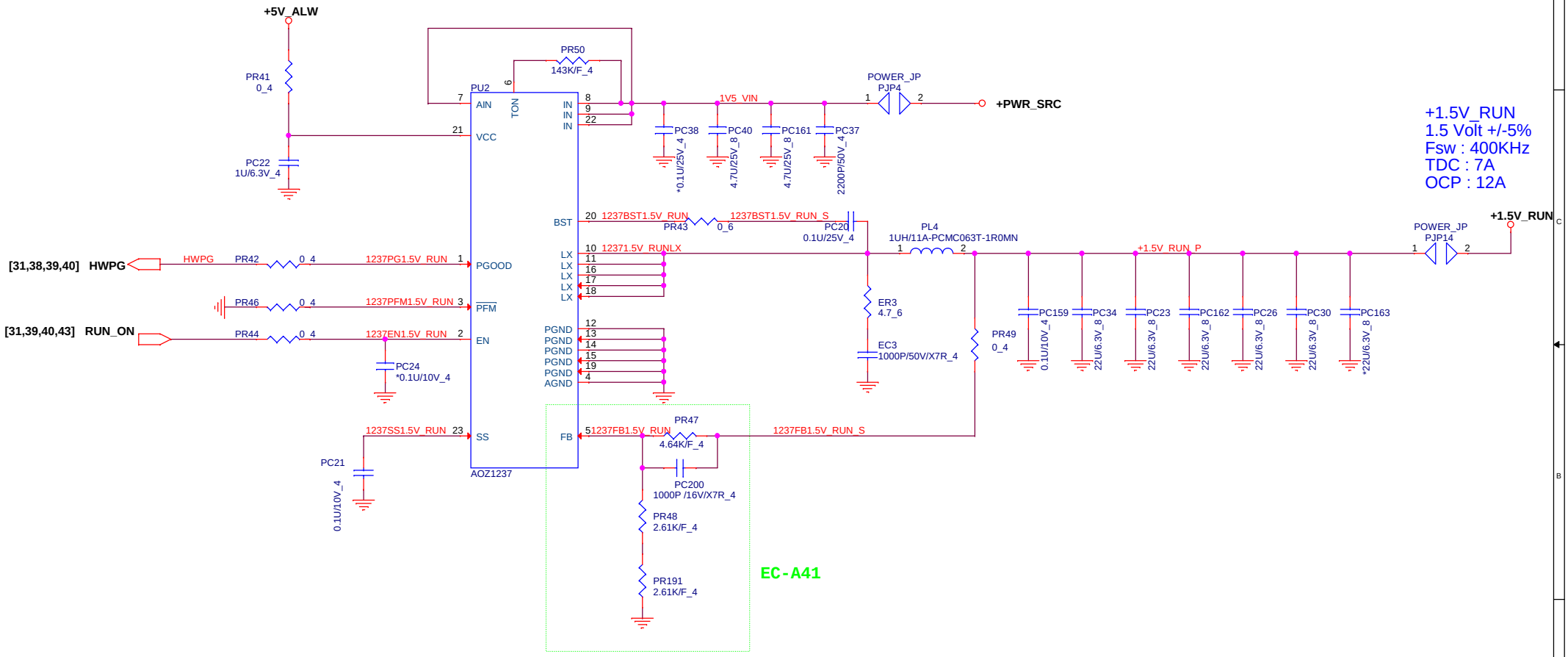


PROJECT : LZ9A

Quanta Computer Inc.

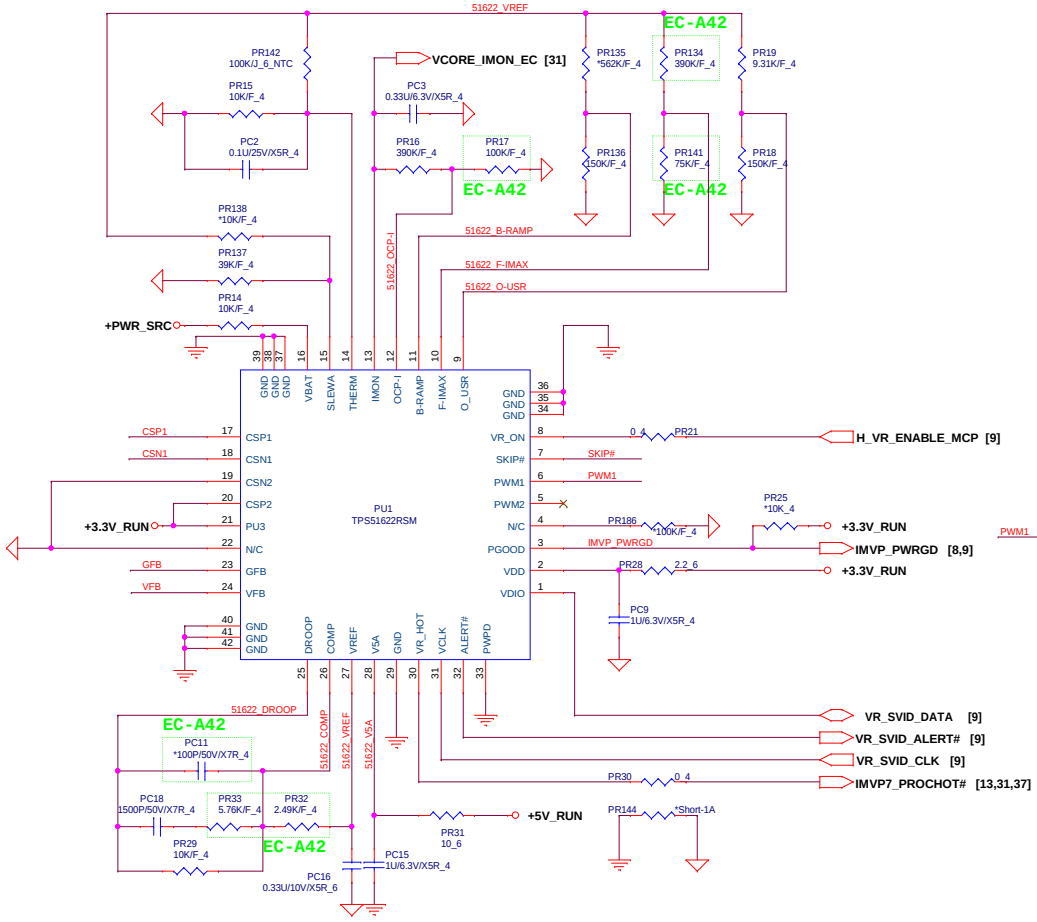
Size	Document Number	Rev
	+1.05V_RUN (AOZ1237)	1A
Date: Thursday, January 03, 2013	Sheet 40 of 47	

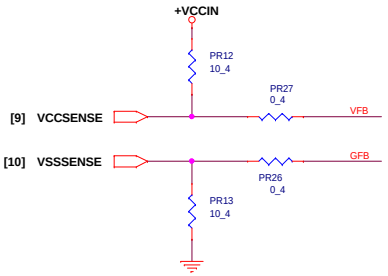
[21,37,38,39,40,42,45] +PWR_SRC
[12,23,28,44,46] +1.5V_RUN
[15,17,23,27,29,30,38,39,40,43,44,45,46] +5V_ALW

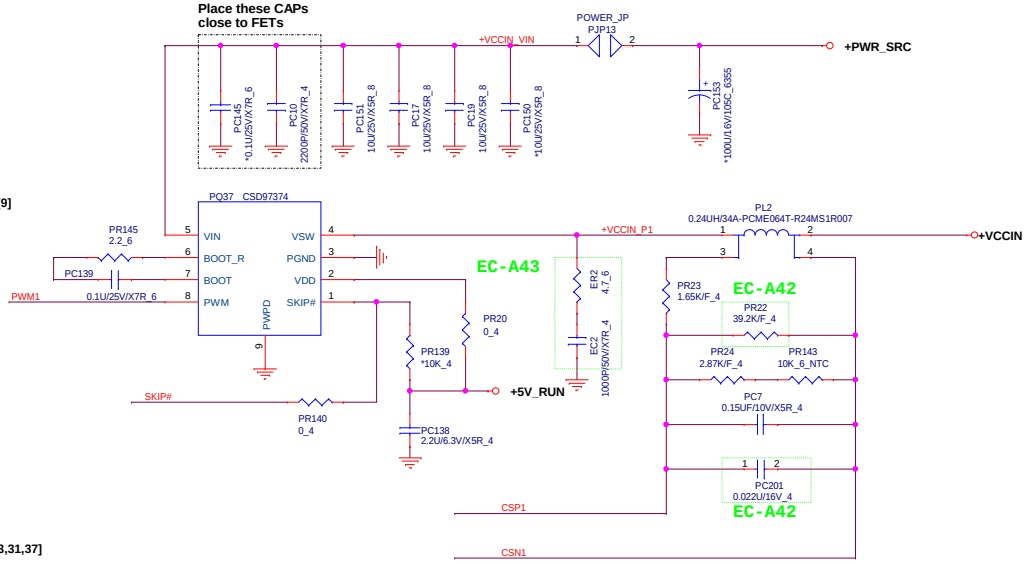


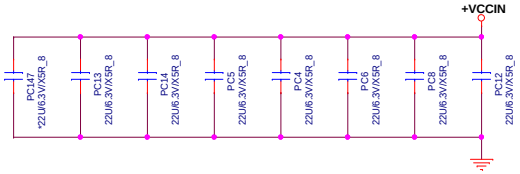
PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: +1.5V_RUN (AOZ1237)	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 41 of 47	

[21,37,38,39,40,41,45] [9] +PWR_SRC +VCCIN
[15,17,23,27,29,30,38,39,40,41,43,44,45,46] +5V_ALW
[6,9,12,35,40,44,46] +1.05V_RUN
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,43,44] +3.3V_RUN
[21,22,23,26,32,34,37,43,44] +5V_RUN







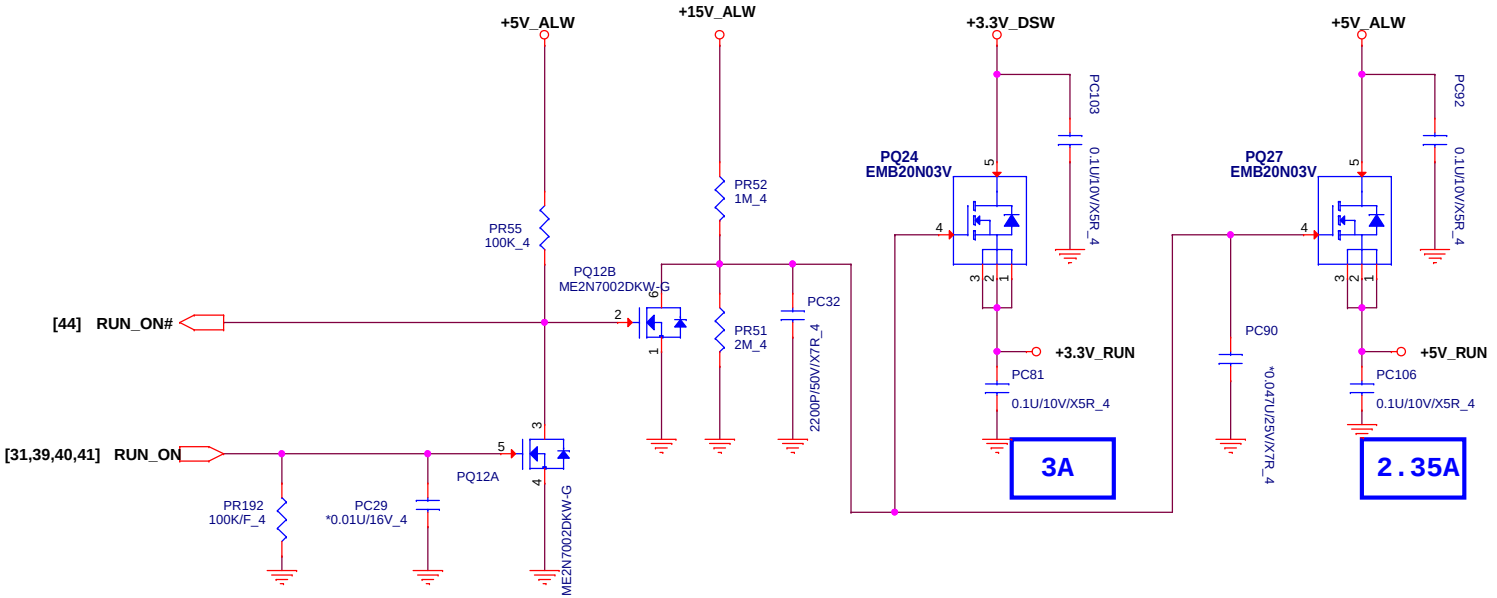


Icc_Max=32A
I_TDC=14A
I_Dynamic=27A
V_Operate=1.6V~1.8V
DC_LL=2m
AC_LL=9m
AC_LL_VOS=9.4m
VBOOT=1.7V

PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE (TPS51622RSML)	1A
Date: Thursday, January 03, 2013	Sheet 42 of 47	

[15,17,23,27,29,30,38,39,40,41,44,45,46] +5V_ALW
[12,38,46] +15V_ALW
[21,22,23,26,32,34,37,42,44] +5V_RUN
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,44] +3.3V_RUN
[4,6,8,12,17,23,25,28,30,32,38,46] +3.3V_DSW
[6,9,12,35,40,44,46] +1.05V_RUN



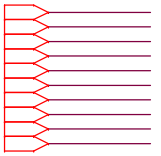
43

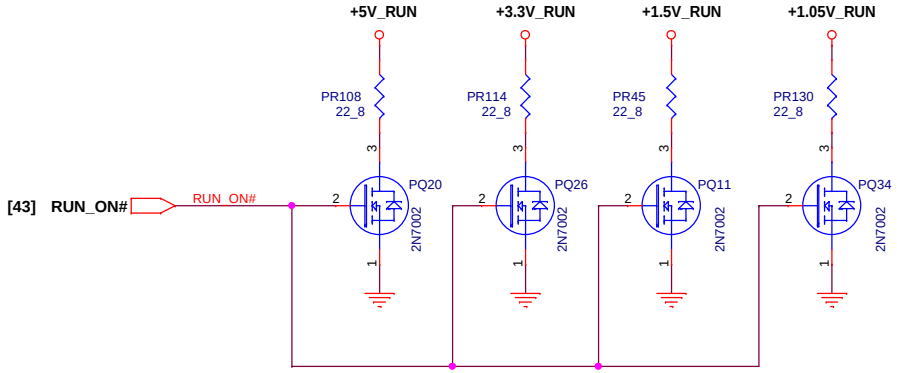
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Load Switch	1A
Date: Thursday, January 03, 2013	Sheet 43 of 47	

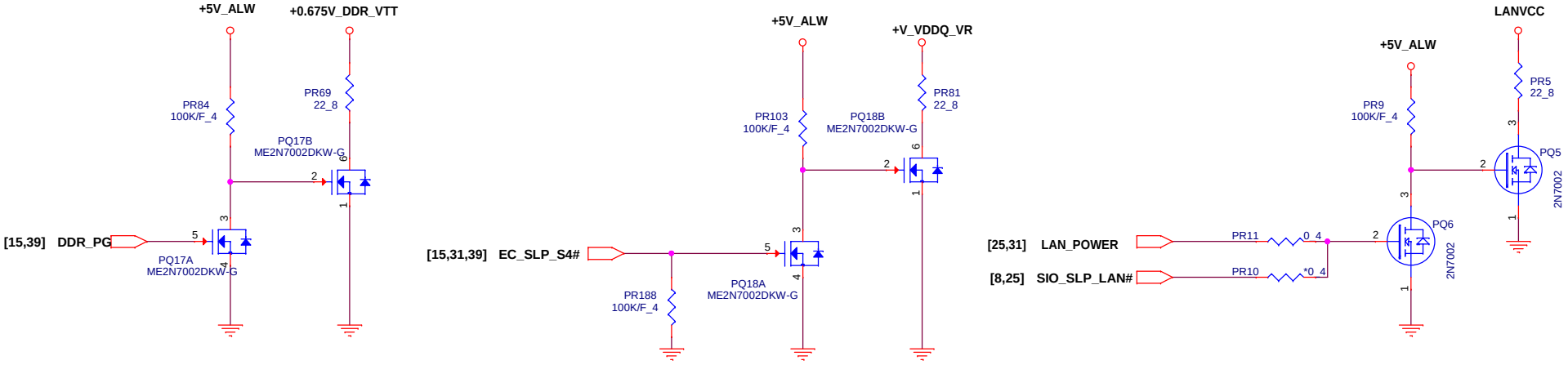
DISCHARGE

[15,17,23,27,29,30,38,39,40,41,43,45,46] +5V_ALW
[21,22,23,26,32,34,37,42,43] +5V_RUN
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43] +3.3V_RUN
[12,23,28,41,46] +1.5V_RUN
[6,9,12,35,40,46] +1.05V_RUN
[14,15,39] +0.675V_DDR_VTT
[4,5,6,7,8,12,15] +3.3V_DEEP_SUS
[9,14,15,39] +V_VDDQ_VR
[25,35] LANVCC
[12,38,43,46] +15V_ALW





LANVCC



PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	

Date: Thursday, January 03, 2013 Sheet 44 of 47

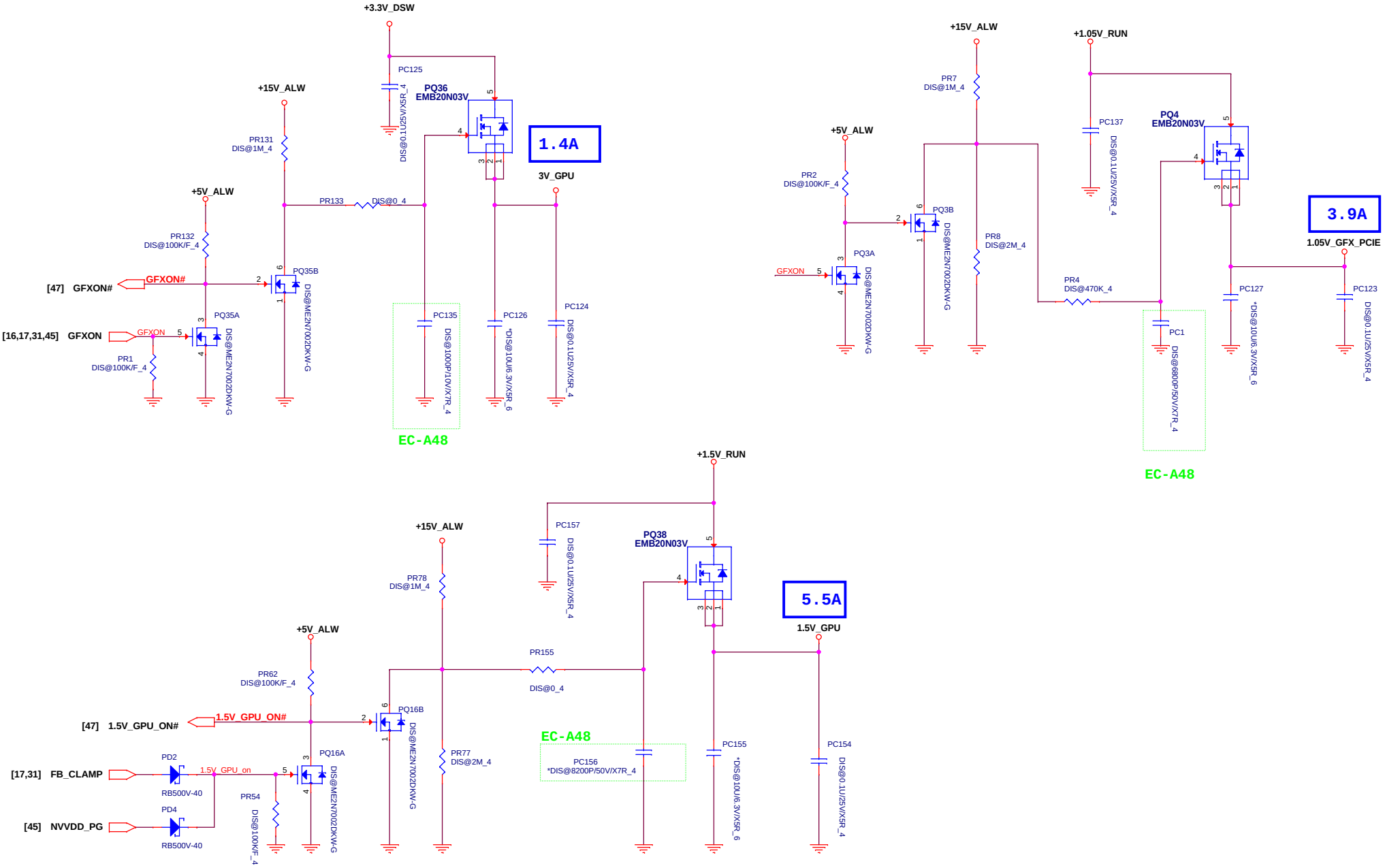
[21,37,38,39,40,41,42] +PWR_SRC
[16,47] VGPU_CORE
[15,17,23,27,29,30,38,39,40,41,43,44,46] +5V_ALW
[16,17,19,35,46,47] 3V_GPU

[16,17,31,46] GFXON

VGPU_CORE
PEAK :30A
OCP :38A

EC-A45

PROJECT :	LZ9A
Quanta Computer Inc.	
Size	Document Number: GFX_CORE (RT8812A) Rev
Date: Thursday, January 03, 2013	Sheet 45 of 47

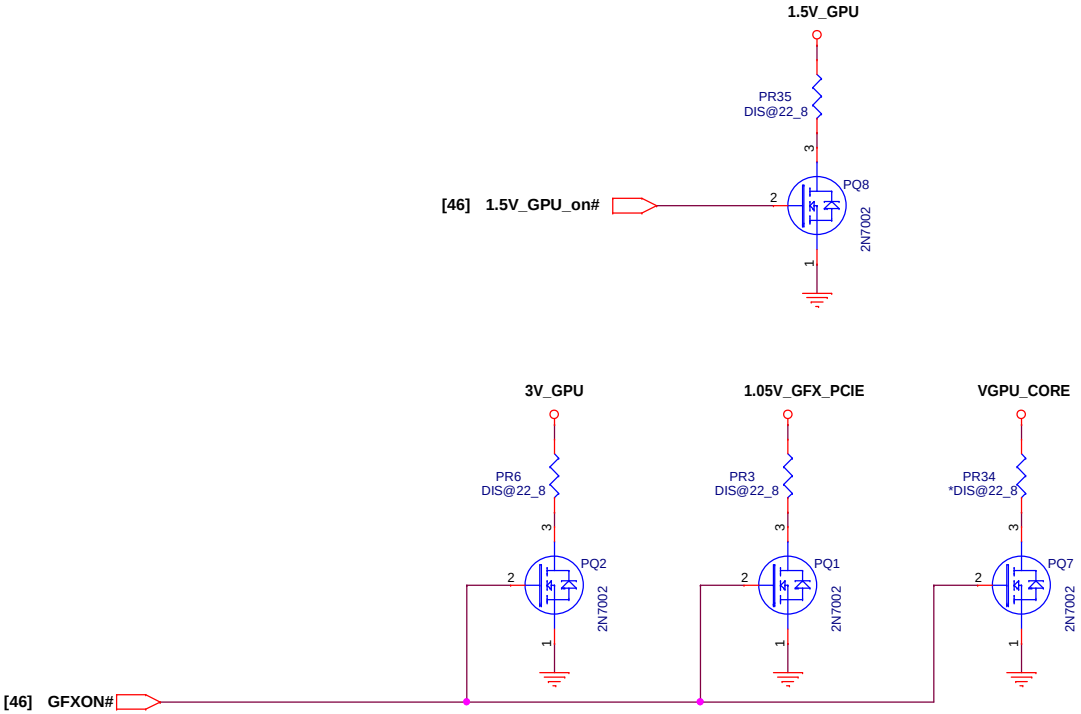


PROJECT : LZ9A		
Quanta Computer Inc.		
Size	Document Number: DIS_Load Switch	Rev: 1A
Date: Thursday, January 03, 2013	Sheet 46 of 47	

DISCHARGE

[15,17,23,27,29,30,38,39,40,41,43,44,45,46]	+5V_ALW
[2,4,6,7,8,12,15,16,19,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43,44]	+3.3V_RUN
[12,23,28,41,44,46]	+1.5V_RUN
[6,9,12,35,40,44,46]	+1.05V_RUN
[14,15,39,44]	+0.675V_DDR_VTT
[9,14,15,39,44]	+V_VDDQ_VR
[25,35,44]	LANVCC
[12,38,43,46]	+15V_ALW

47



PROJECT : LZ9A

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	
Date: Thursday, January 03, 2013	Sheet 47 of 47	