MS-1453(Switchable) & MS-1454(UMA) Ver : 10

2009/07/07

Calpella Platform

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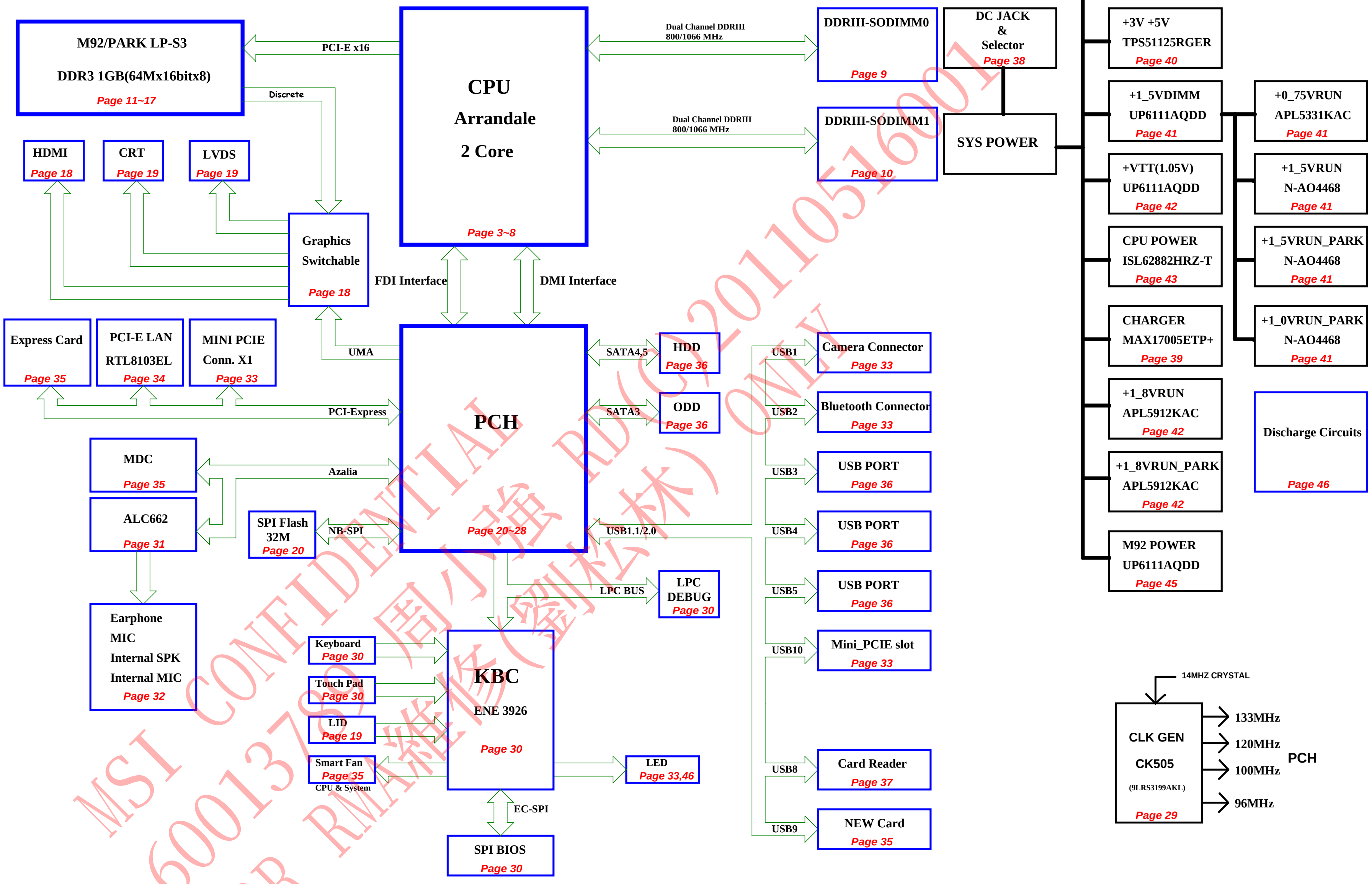

MICRO-STAR INT'L CO.,LTD.

Title	BLOCK DIAGRAM		
Size: Custom	Document Number: MS-145X		Rev: 10
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0,S3	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
		S0	
M92S_VDD_CORE	0.95V	S0	GPU core power
+1_8VRUN_PARK	1.8V	S0	GPU PCIE power
+1_5VRUN_PARK	1.5V	S0	GPU DDR3 power
+1_0VRUN_PARK	1.0V	S0	GPU PCIE power
VDDR3	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

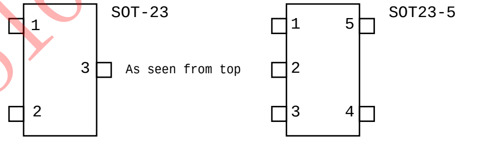
Suffix

\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



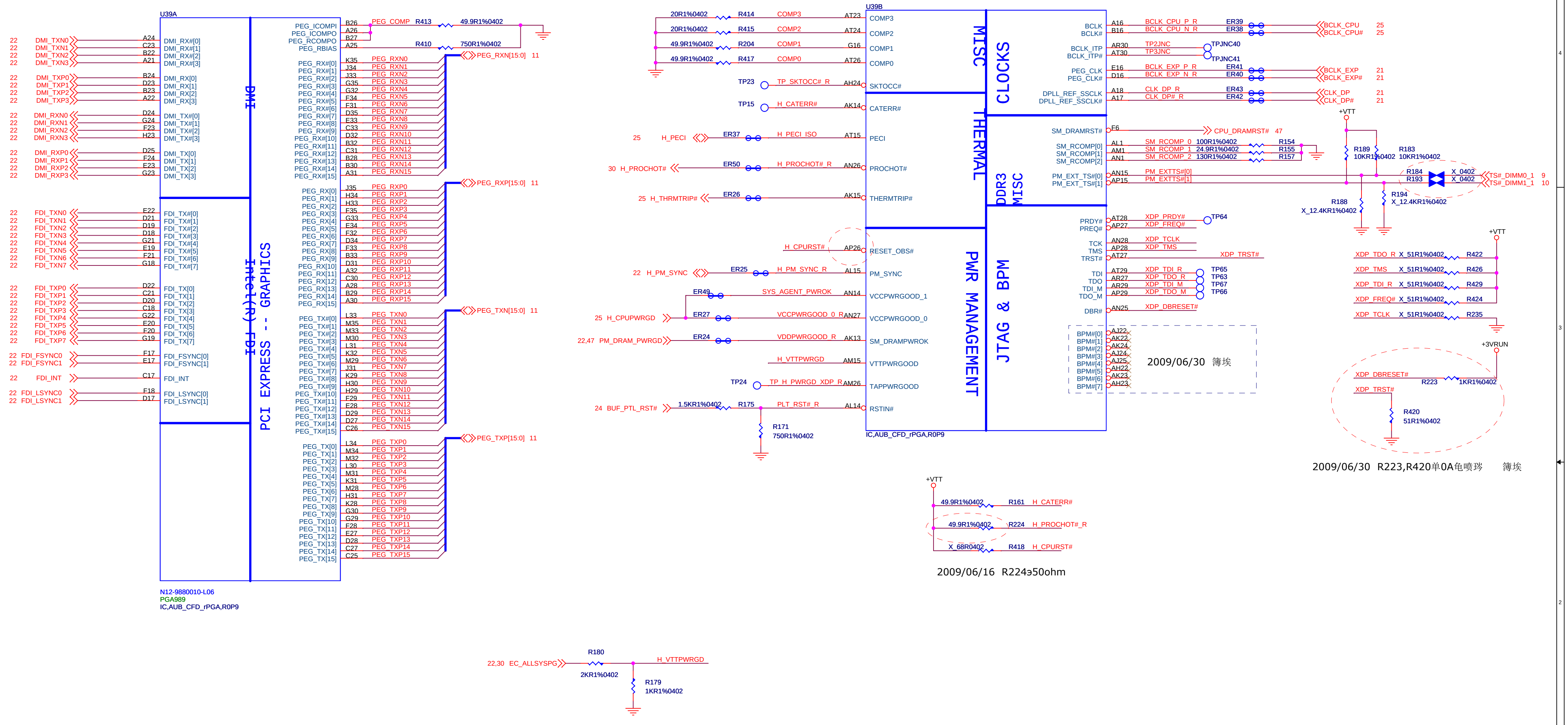
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



MSI MICRO-STAR INT'L CO.,LTD.

Title	PROCESSOR	
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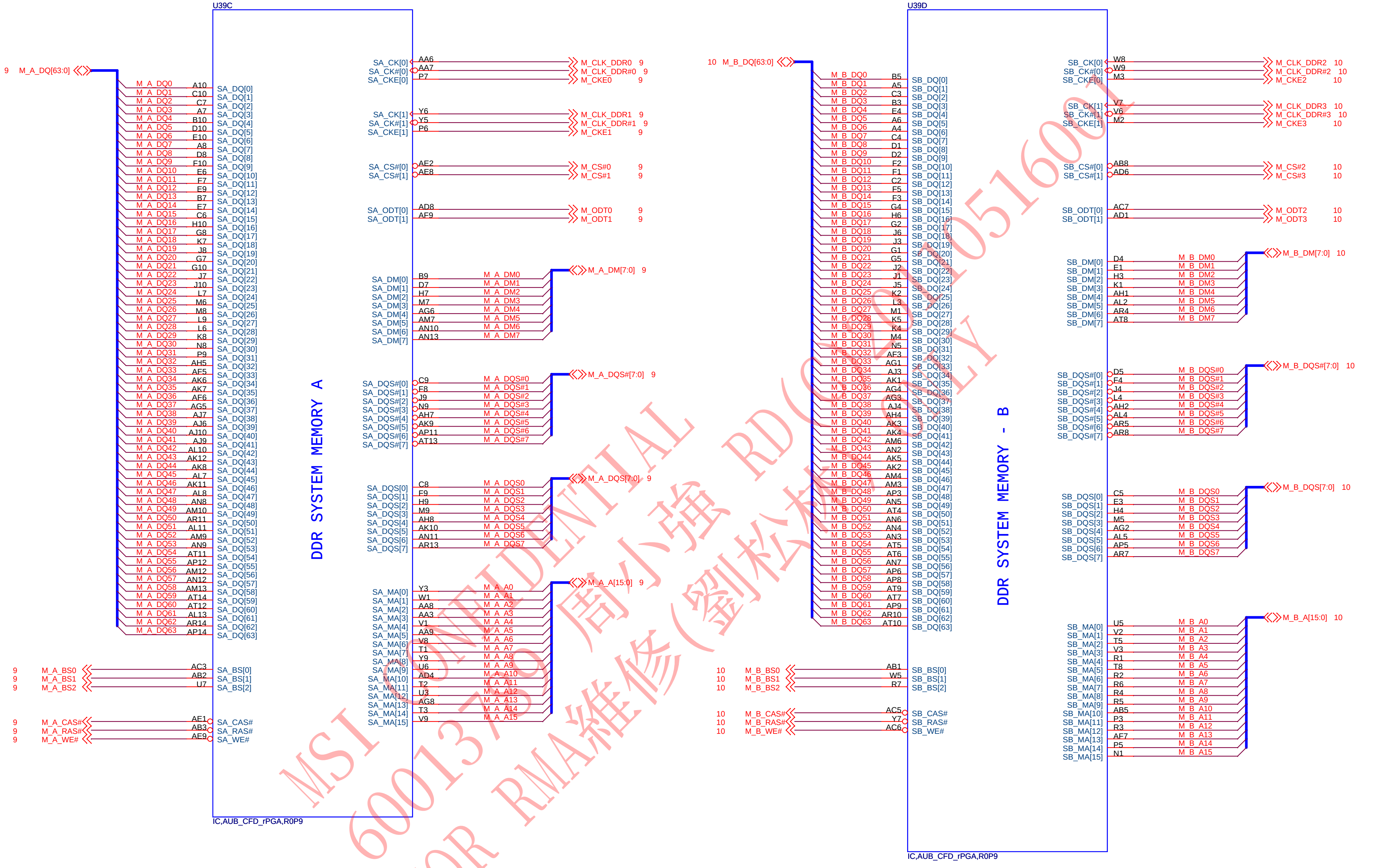
ARRANDALE PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.

Title	DDR3	
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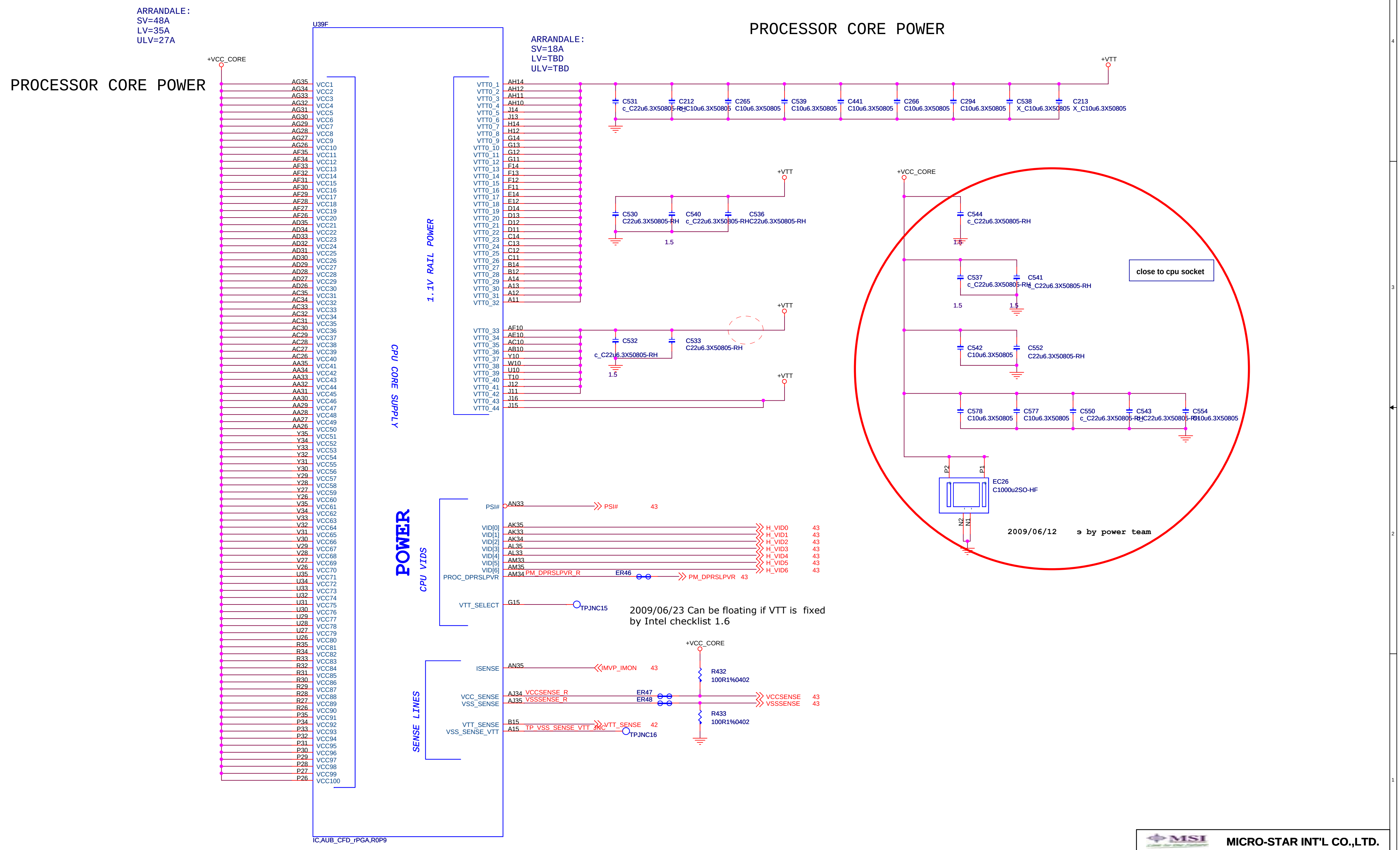
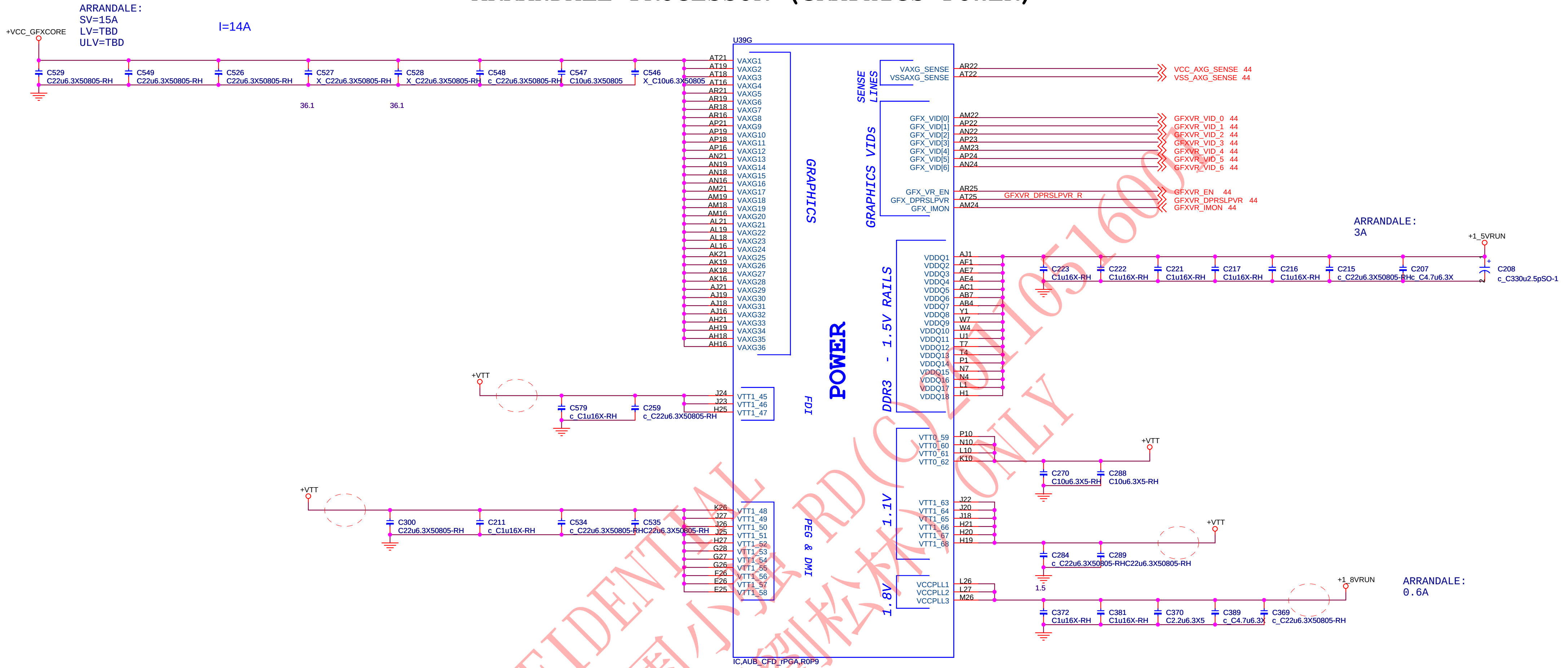
ARRANDALE PROCESSOR (POWER)



ARRANDALE PROCESSOR (GRAPHICS POWER)



MICRO-STAR INT'L CO.,LTD.

Title: GRAPHICS POWER

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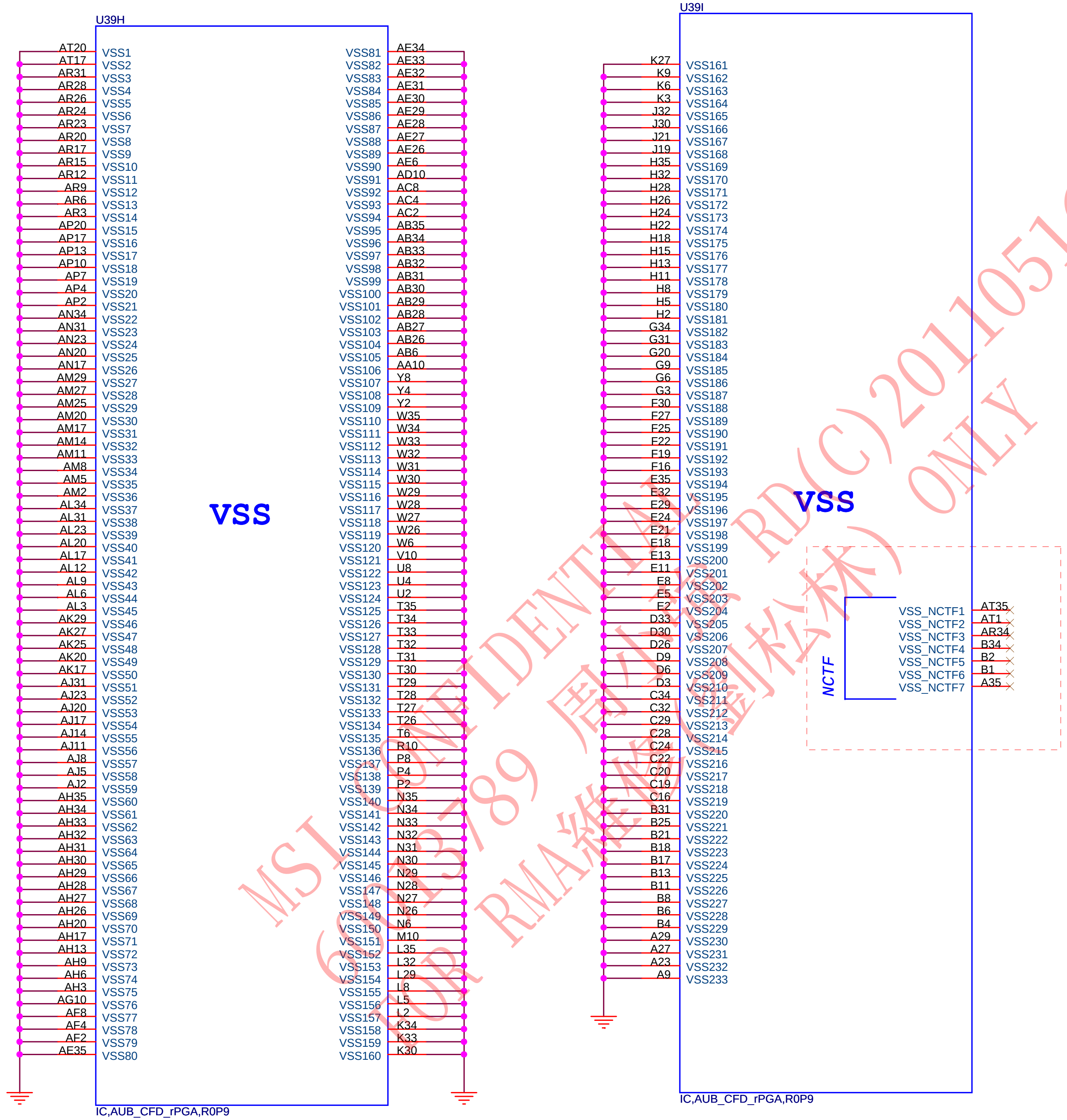
ARRANDALE PROCESSOR (GND)



MICRO-STAR INT'L CO.,LTD.

Title	PROCESSOR GND
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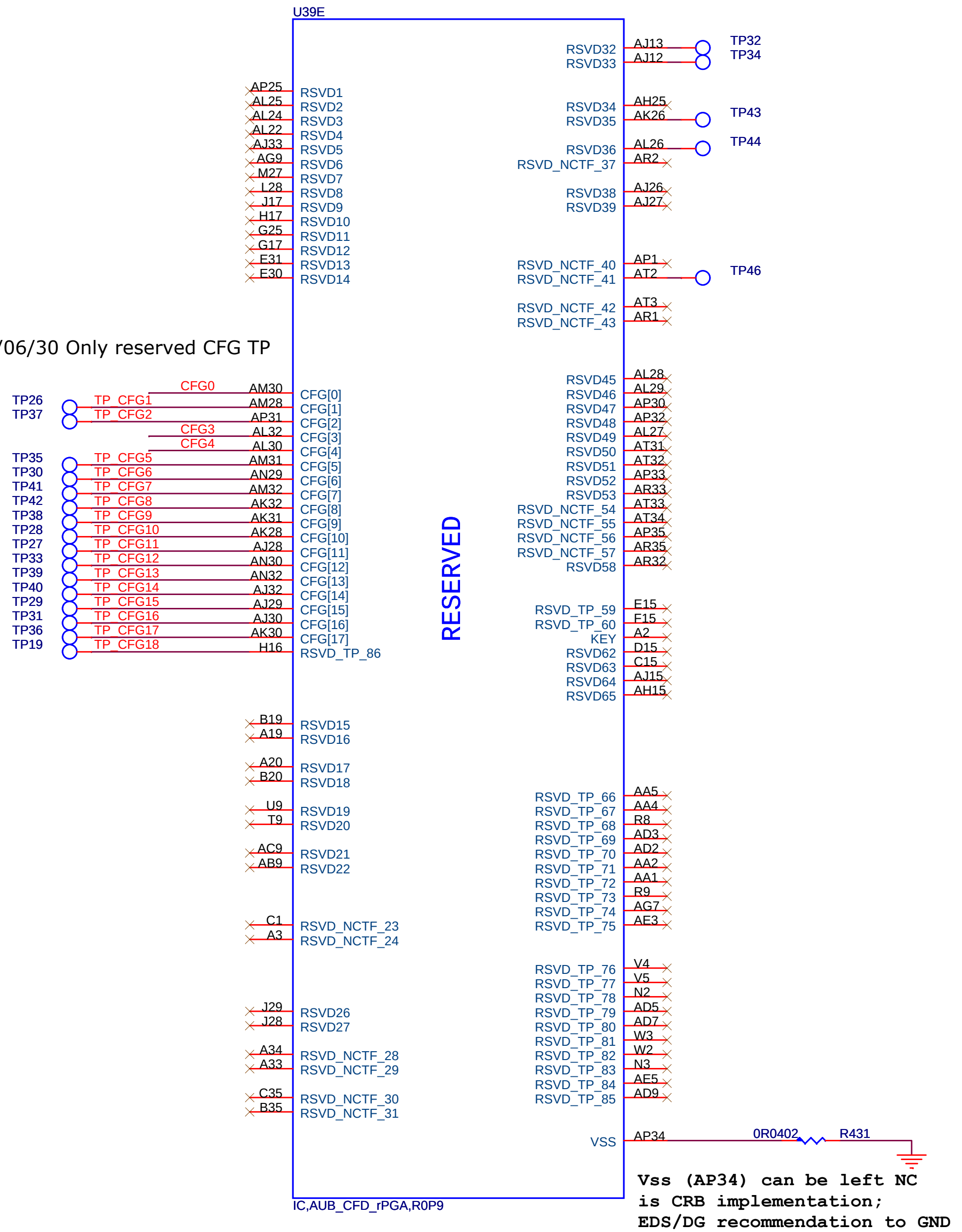
ARRANDALE PROCESSOR (RESERVED)

2009/06/30 Only reserved CFG TP

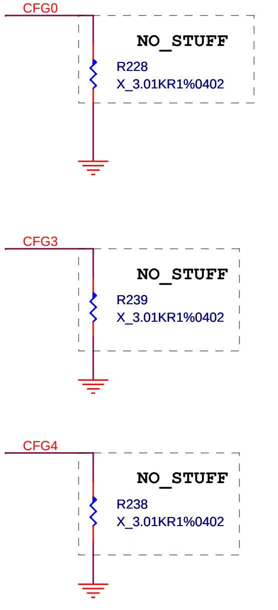


Vss (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

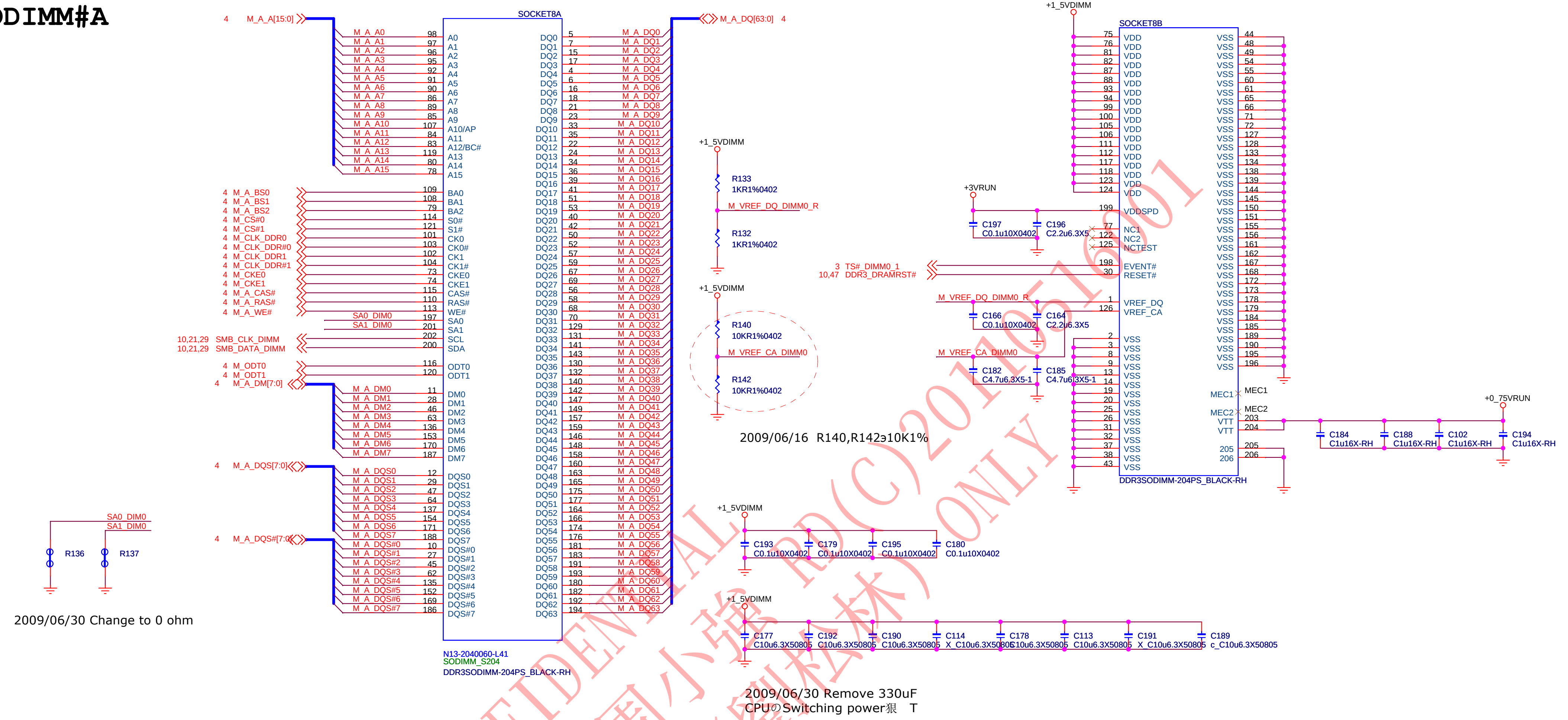
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



Layout Note:
Location of all CFG strap resistors needs to be close to trace to minimize stub

SODIMM#A



MICRO-STAR INT'L CO.,LTD.

Title: DDR3 SODIMM0

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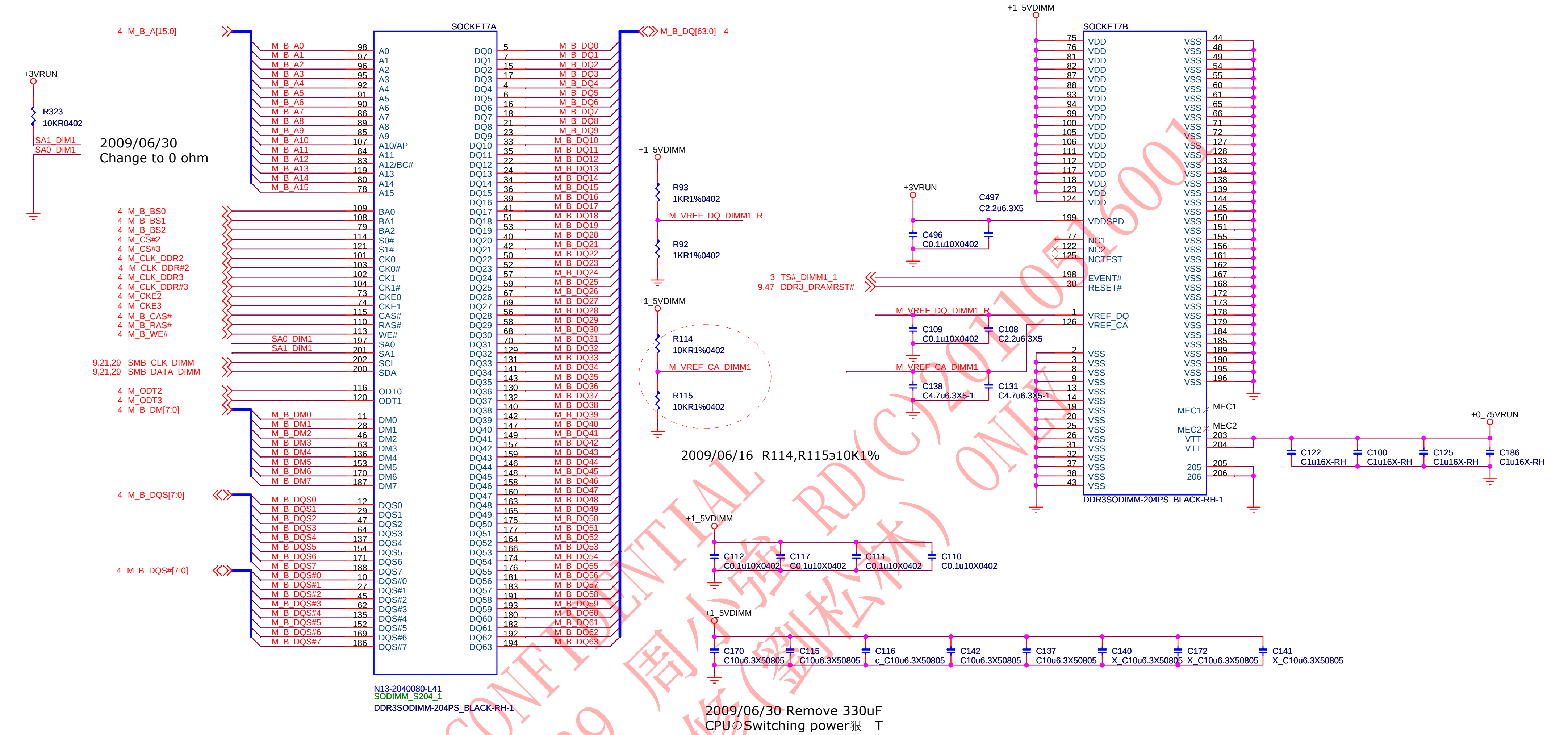
SODIMM#B



MICRO-STAR INT'L CO.,LTD.

Title	DDR3 SODIMM1	
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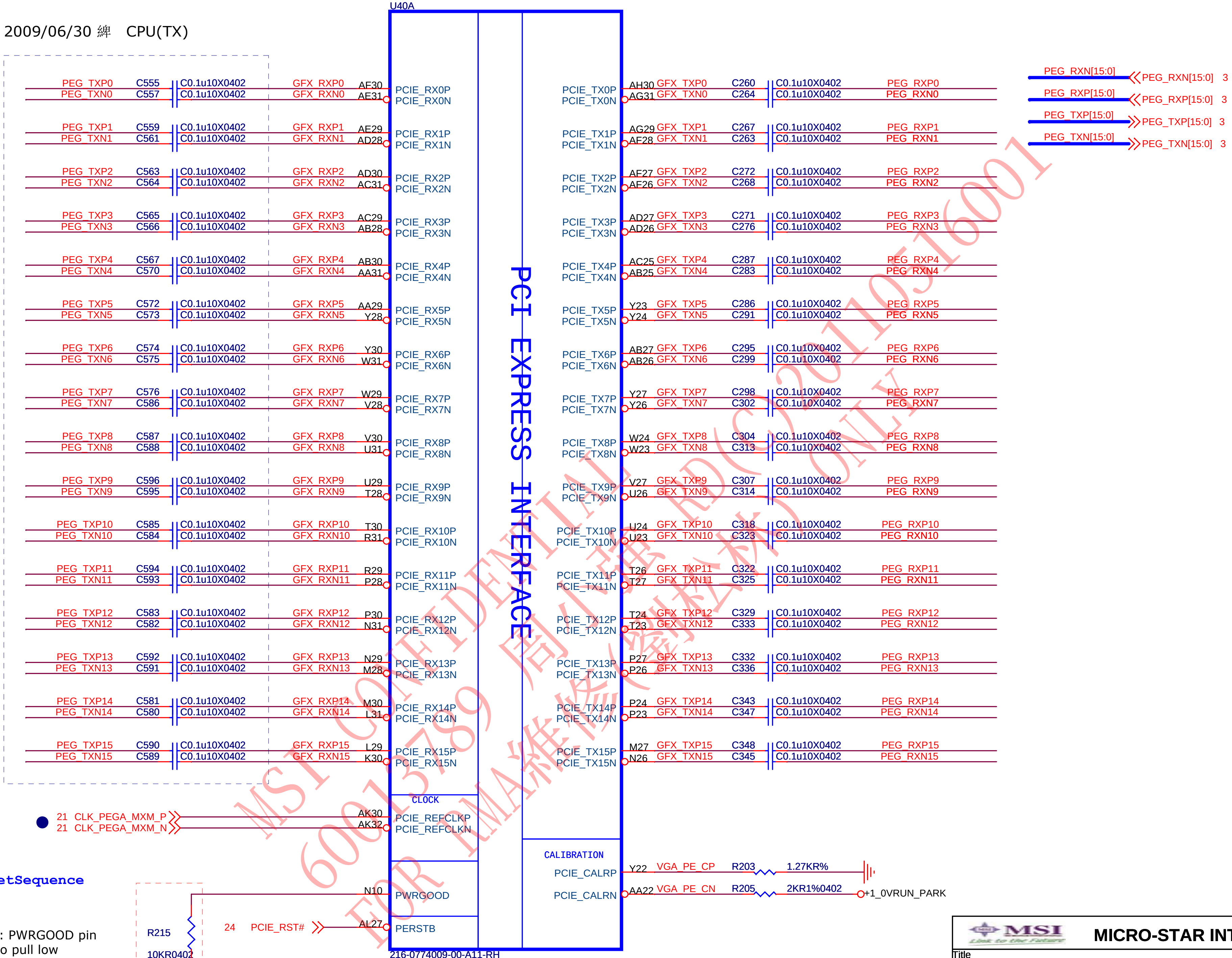
2009/06/30 緋 CPU(TX)



CheckResetSequence

For Park-S3: PWRGOOD pin must need to pull low

For M92-S2/S3: PWRGOOD pin should be NC

	M92-S2	PARK-S3
R215	X	-

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (PCIE_Interface)

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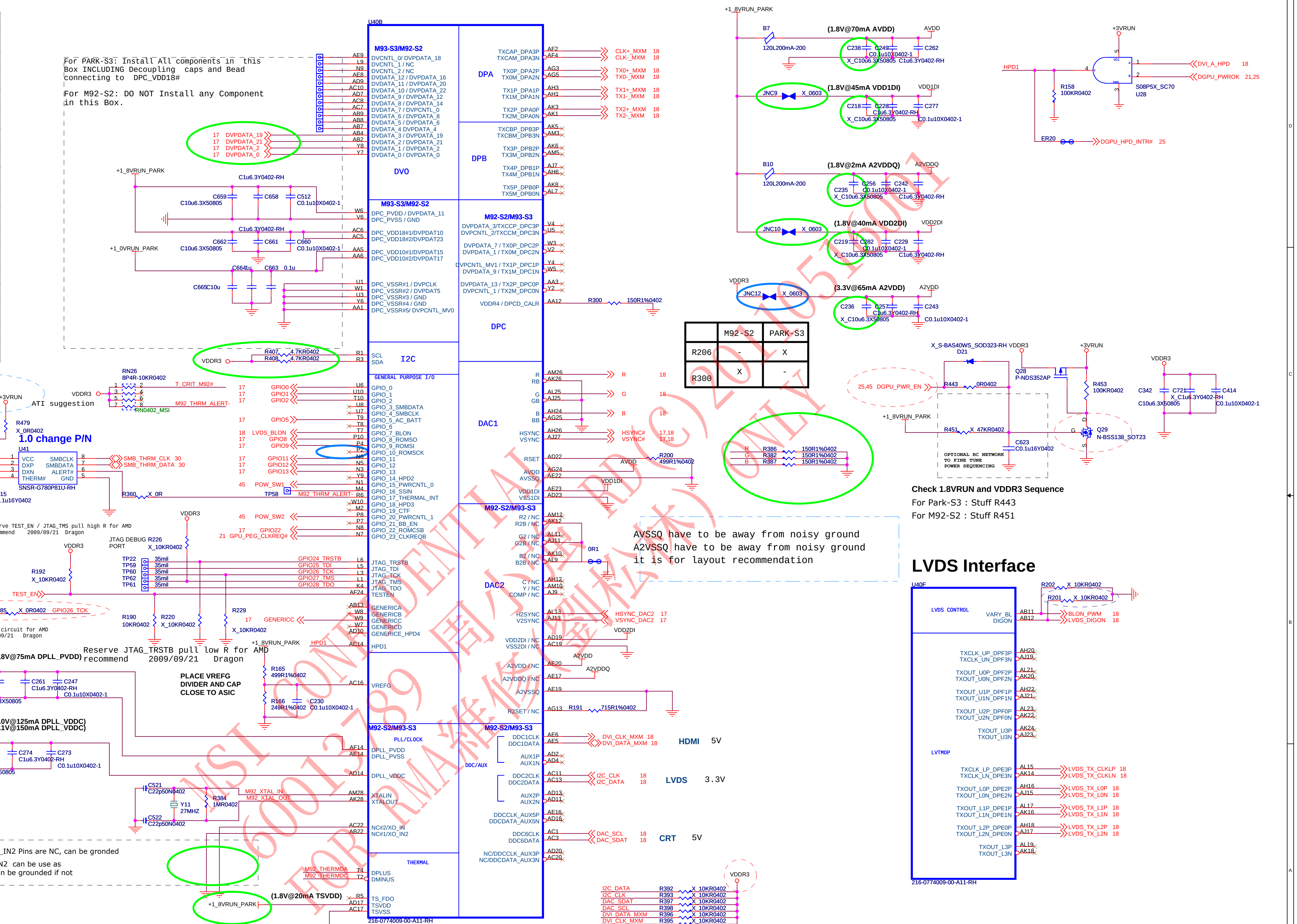
	M92-S2	PARK-S3
R210	X	-
R195	X	-
R208	X	-
C659	X	-
C658	X	-
C512	X	-
C662	X	-
C661	X	-
C660	X	-
R197	X	-
R356	X	-
C665	X	-
C664	X	-
C663	X	-
R406	X	-
R404	X	-
R402	X	-



	M92-S2	PARK-S3
R206	-	X
R300	X	-

Note:1
For M9x-S2/S3 XO_IN and XO_IN2 Pins are NC, can be gronded
For Park-S3: XO_IN and XO_IN2 can be use as 3.3V CLK Input. These poins can be grounded if not in use.

MICRO-STAR INT'L CO.,LTD.

Title	M92/Pak-Sx (Main_IO)		
Size: Custom	Document Number: MS-145X		Rev: 10
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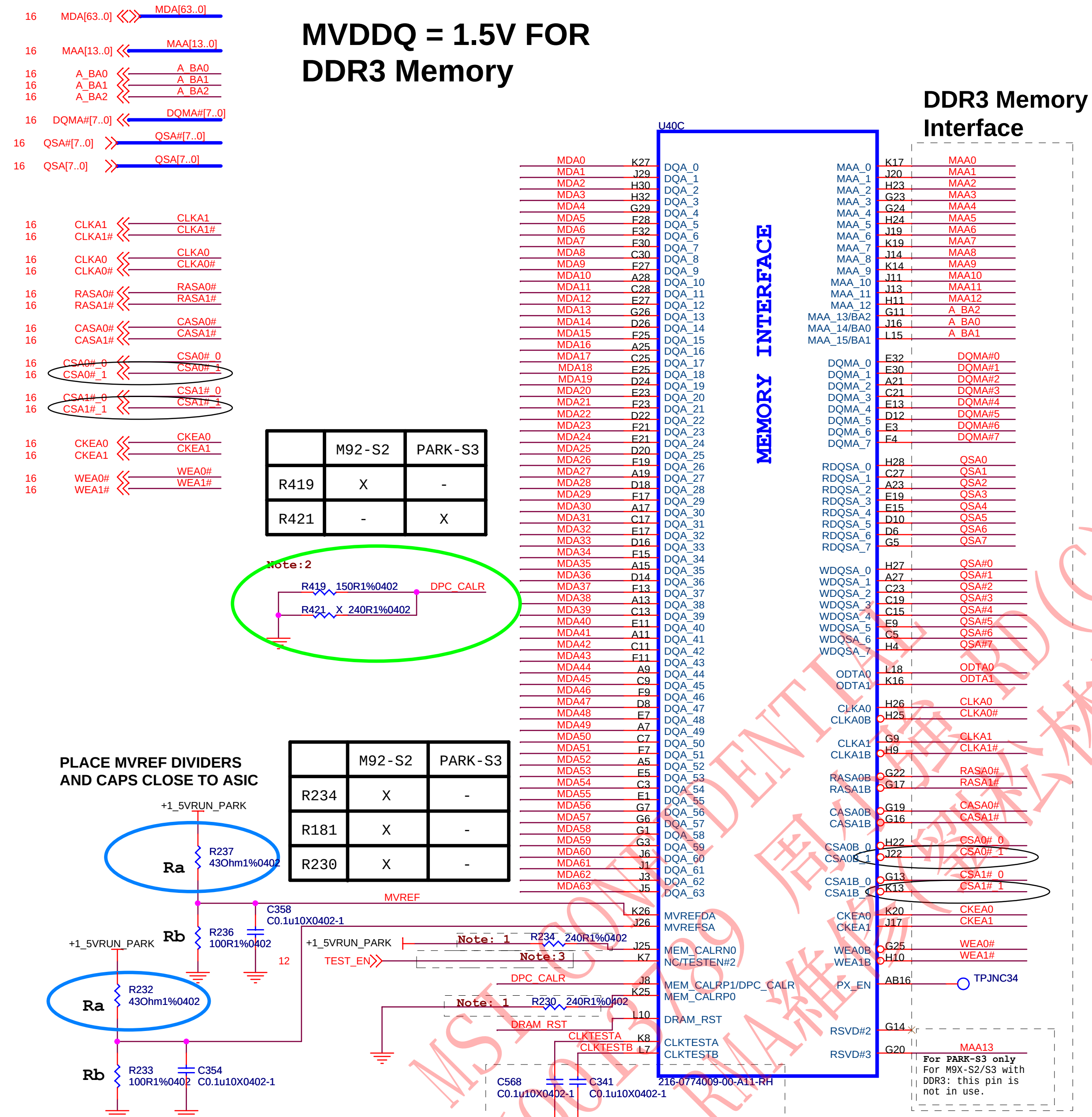
MVDDQ = 1.5V FOR DDR3 Memory

DDR3 Memory Interface

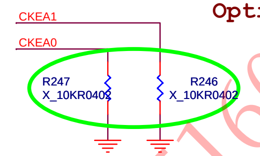


route 50ohms single-ended/100ohms diff and keep short

Use this option ONLY for Park-S3

	M92-S2	PARK-S3
R247	X	-
R246	X	-

Option for DDR3/GDDR3/DDR2 with Park



Do not Install for M9X-S2/S3

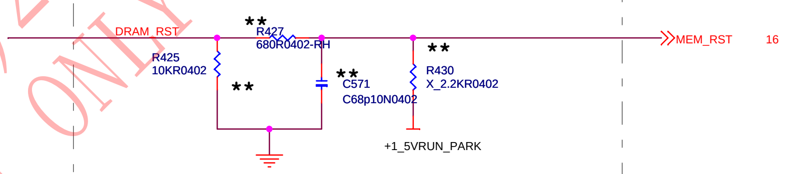
INSTALL for Park-S3 to save power in auto refresh mode

These can be placed close to ASIC side or Memory side.

Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.

Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR

Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24



** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor vvalues are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

	M92-S2	PARK-S3
R419	X	-
R421	-	X

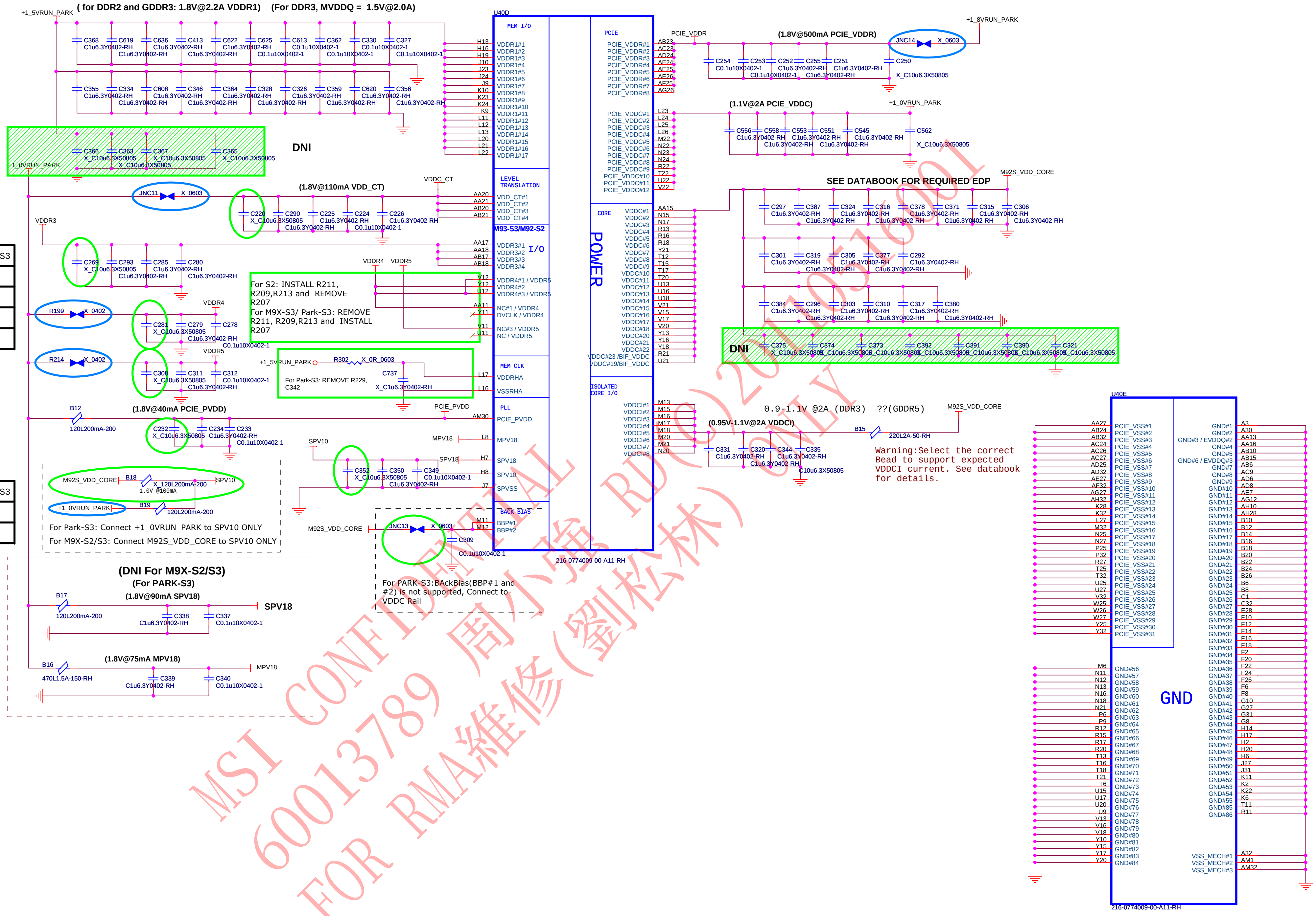
	M92-S2	PARK-S3
R234	X	-
R181	X	-
R230	X	-

Designator	For M9X-S2 and M93-S3	For Park-S3
R425	DNI	10K
R427	0R/Short	680R
R430	2.2K	DNI
C571	2.2nF	68pF

	M92-S2	PARK-S3
R428	-	X
R226	-	X

DIVIDER RESISTORS	DDR3
MVREF TO 1.5V (Ra)	43R
MVREF TO GND (Rb)	100R

	M92-S2	PARK-S3
C568	X	-
C341	X	-
R423	X	-
R227	X	-



	M92-S2	PARK-S3
R211	-	X
R207	X	-
R209	-	X
R213	-	X

	M92-S2	PARK-S3
B18	-	X
B19	X	-

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (Power & GND)

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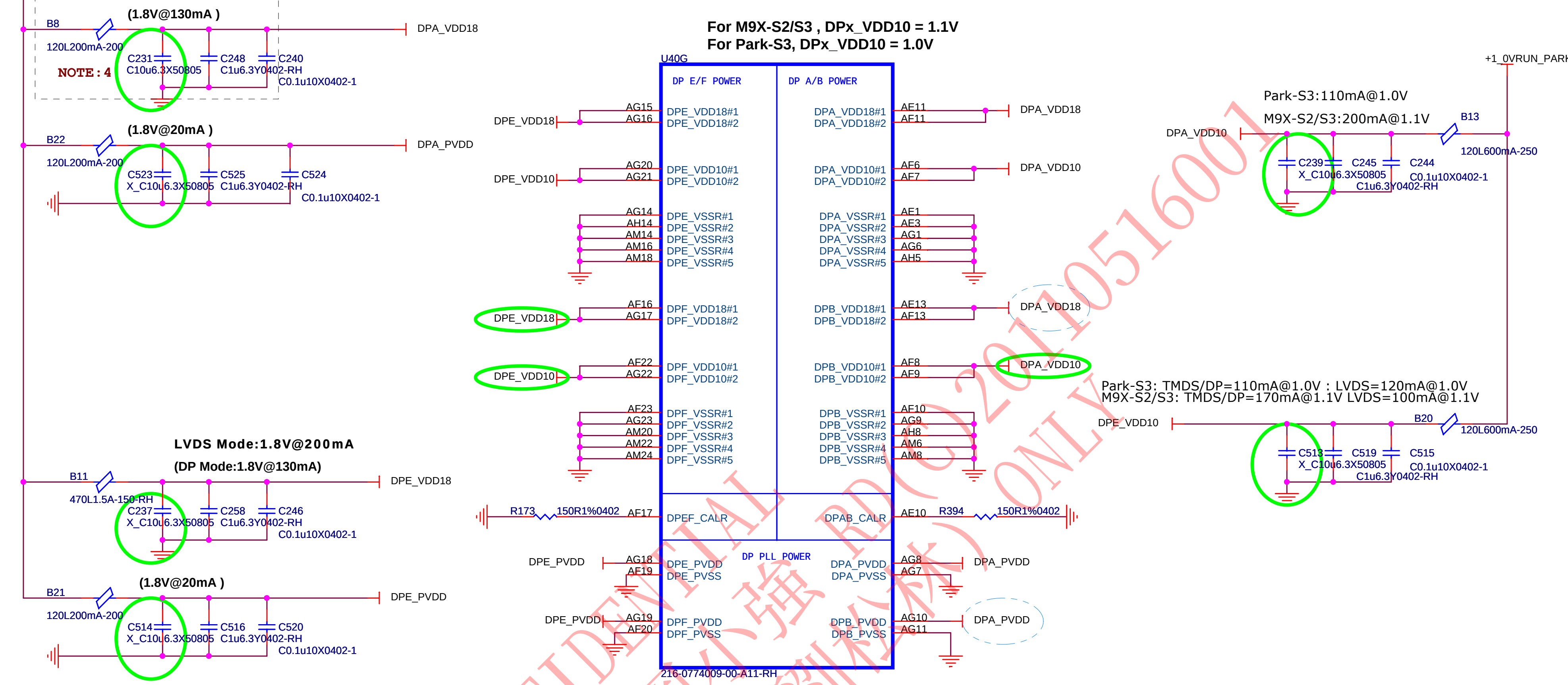
See Databook and Application note table for Voltage and Current requirements for each individual rail.



NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

MICRO-STAR INT'L CO.,LTD.

Title	M92/Pak-Sx (DP_Power)	
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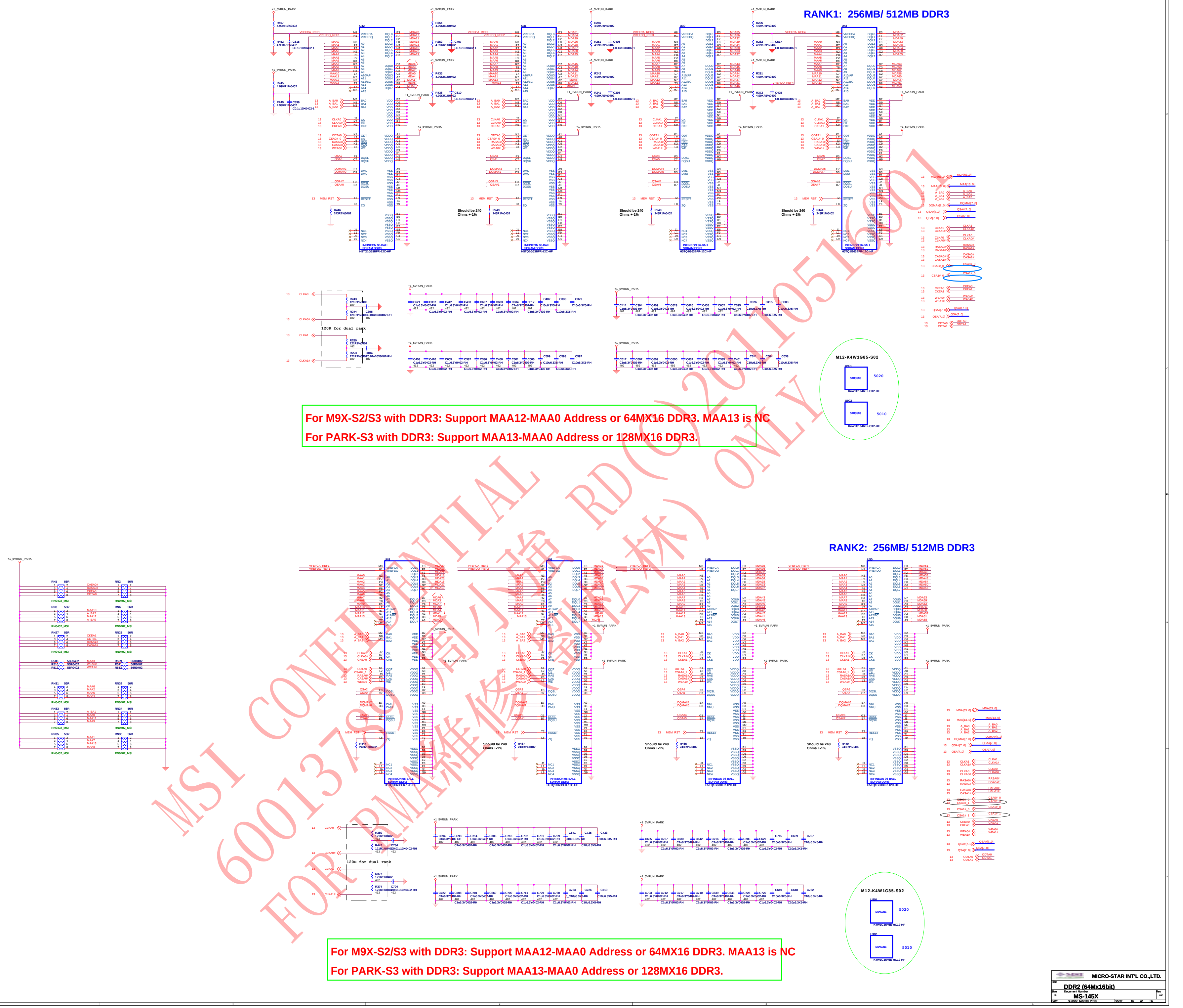

MICRO-STAR INT'L CO.,LTD.

DDR2 (64Mx16bit)

MS-145X

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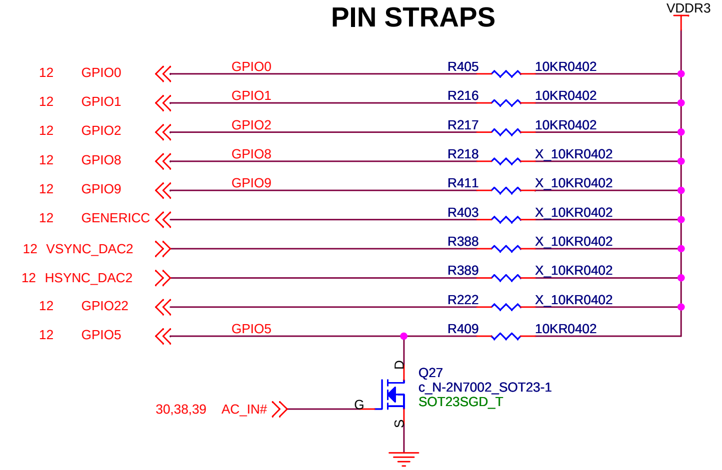
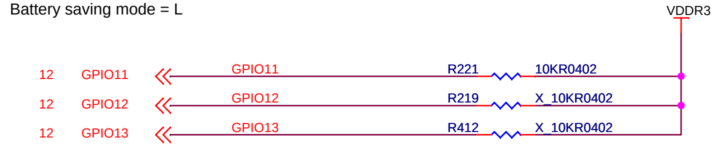
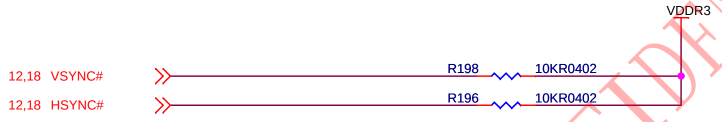
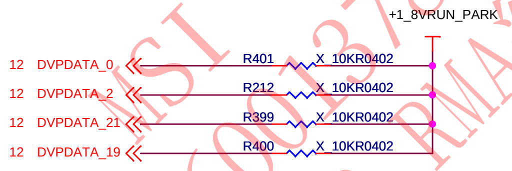
PIN STRAPS



GPIO_5_AC_BATT is an optional input which allows the system to request (AC) performance mode or battery mode operation.
AC (Performance mode) = H
Battery saving mode = L







CONFIGURATION STRAPS

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO0	1		GPIO=0 50% TX output swing GPIO=1 Full TX output swing
GPIO1	1		GPIO=0 TX de-emphasis disabled GPIO=1 TX de-emphasis enabled
GPIO2	1		GPIO=0 Advertises the PCIE device as 2.5 GT/S capable at power -on GPIO=1 Advertises the PCIE device as 5 GT/S capable at power -on
GPIO9	0		GPIO=0 VGA controller capacity enabled. GPIO=1 The device will not be recognized as the system's VGA controler.
VSYNC_DAC2	0		GPIO=0 Driver would ignore the value sampled on DVPDATA_20 during reset.
GPIO22	0		GPIO=0 not used external BIOS ROM GPIO=1 if used

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO 13 GPIO 12 GPIO 11	0 0 1		0 0 0=128 MB 0 0 1=256 MB 0 1 0=64 MB

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
VGA_HSYNC# VGA_VSYNC#	1 1		0 0=No audio function 0 1=Audio for display port only 1 0=Audio for display port and HDMI if dongle is detected 1 1=Audio for both displayport and HDMI

DVPDATA19	DVPDATA21	DVPDATA2	DVPDATA0	MEM_TYPE
0	0	0	0	Hynix 64Mx16 DDR3 (M12-5TQ1G25-H23)
0	0	0	1	Samsung 64Mx16 DDR3 (M12-K4W1G85-S02)
0	0	1	0	
0	0	1	1	

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (Straps & Thermal)

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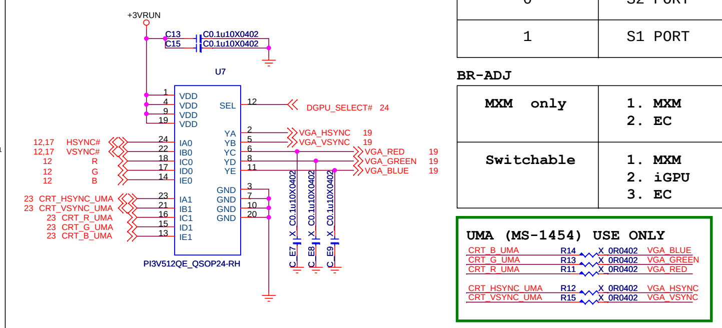
CRT Switch

2009/07/14 Change RGB SW

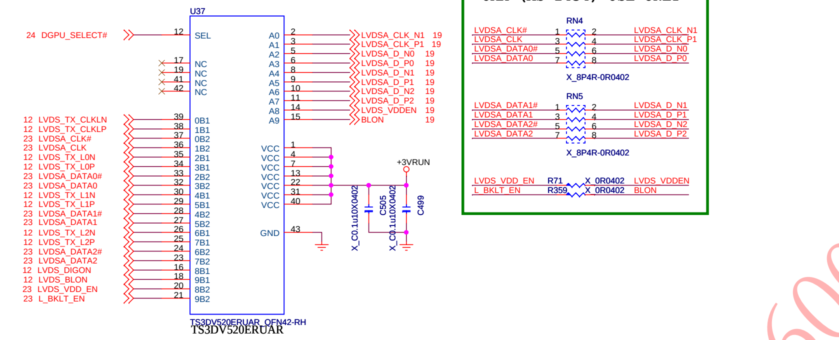


Logic Input	Function
0	S2 PORT
1	S1 PORT

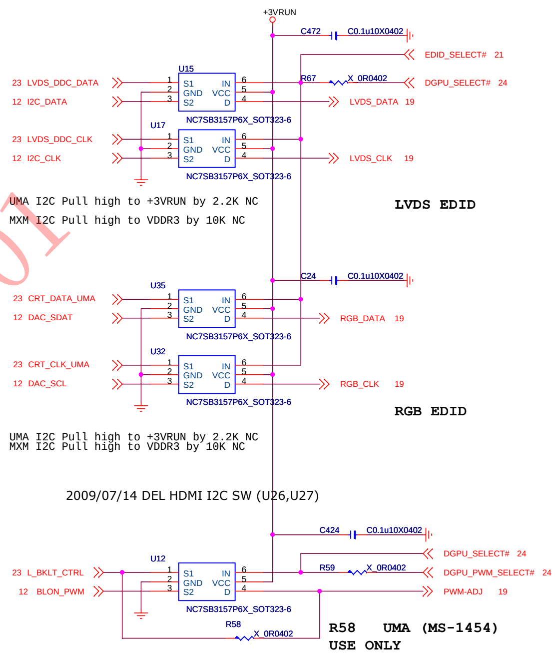
BR-ADJ

MXM only	1. MXM 2. EC
Switchable	1. MXM 2. iGPU 3. EC

LVDS Switch



EDID Switch (CRT,LVDS)

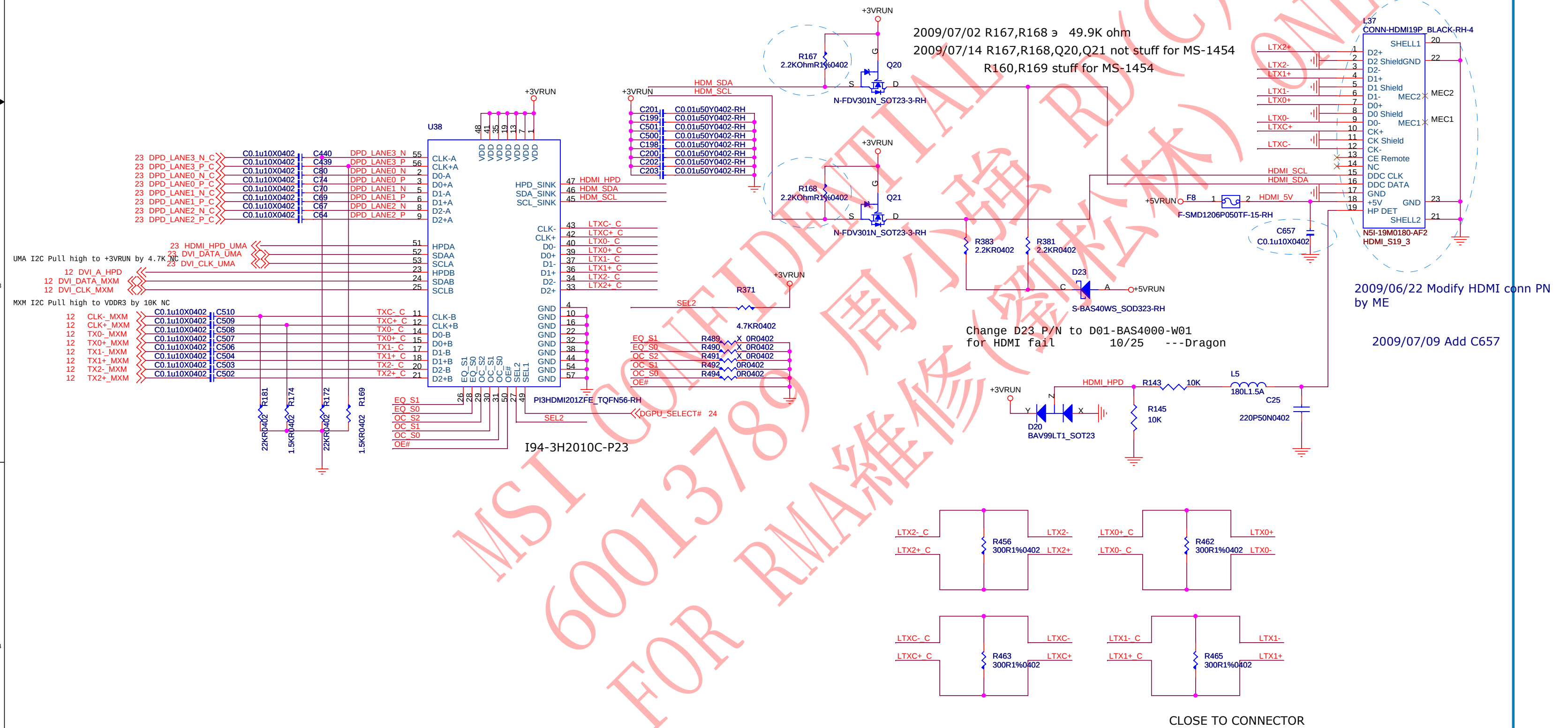


Logic Input	Function
0	PORT 1
1	PORT 2

HDMI Switch

2009/07/14 Change HDMI SW

Logic Input	Function
0	B PORT
1	A PORT



UMA (MS-1454) USE ONLY

LVDS_DDC_CLK	R84	X_0R0402	LVDS_CLK
LVDS_DDC_DATA	R82	X_0R0402	LVDS_DATA
CRT_DATA_UMA	R265	X_0R0402	RGB_DATA
CRT_CLK_UMA	R266	X_0R0402	RGB_CLK

2009/07/14 DEL HDMI I2C RES (R372,R374)

MICRO-STAR INT'L CO.,LTD.

Title	SWITCH&HDMI	
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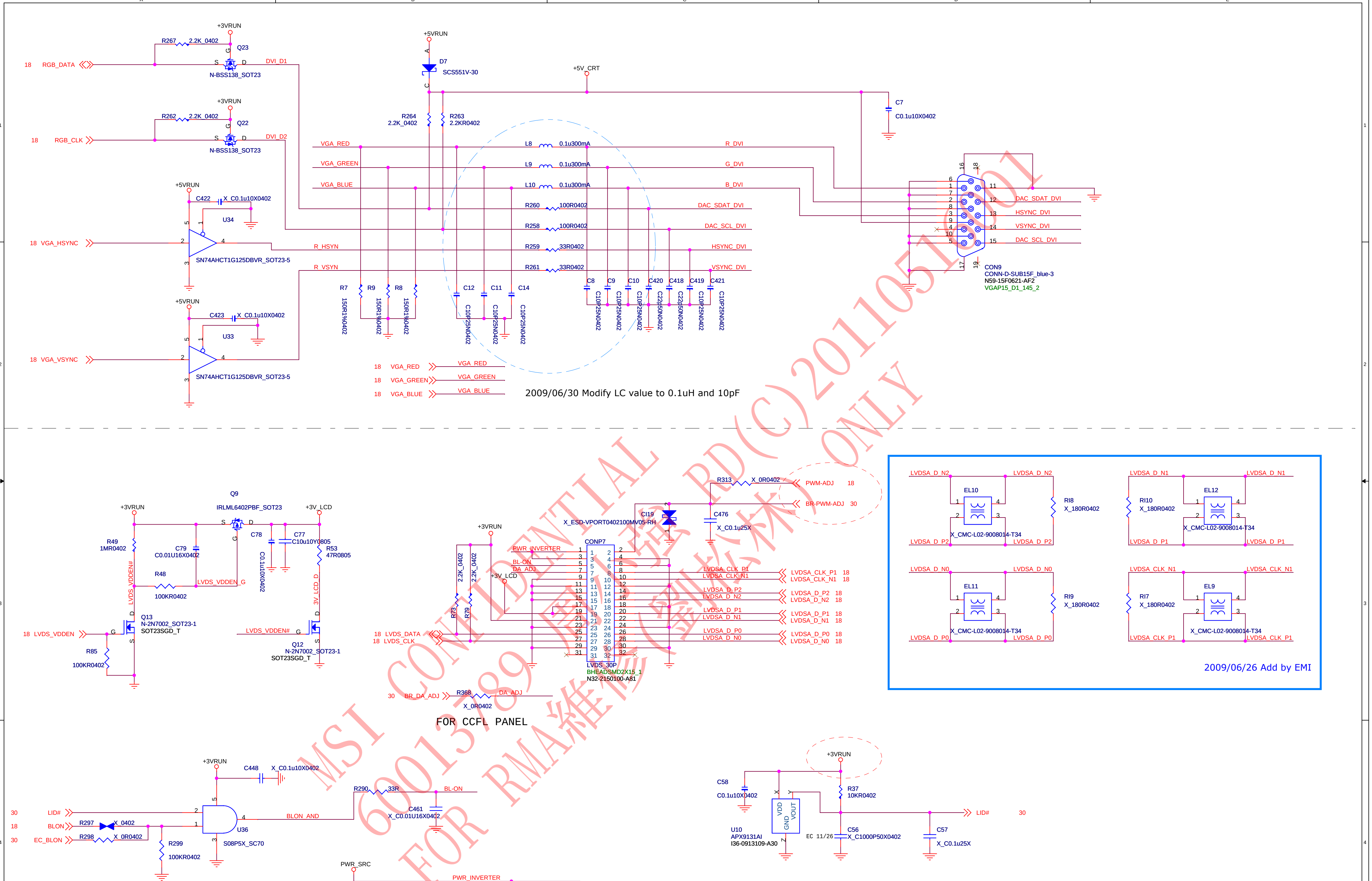

MICRO-STAR INT'L CO.,LTD.

Title: CRT & LVDS

Size	Document Number	Rev
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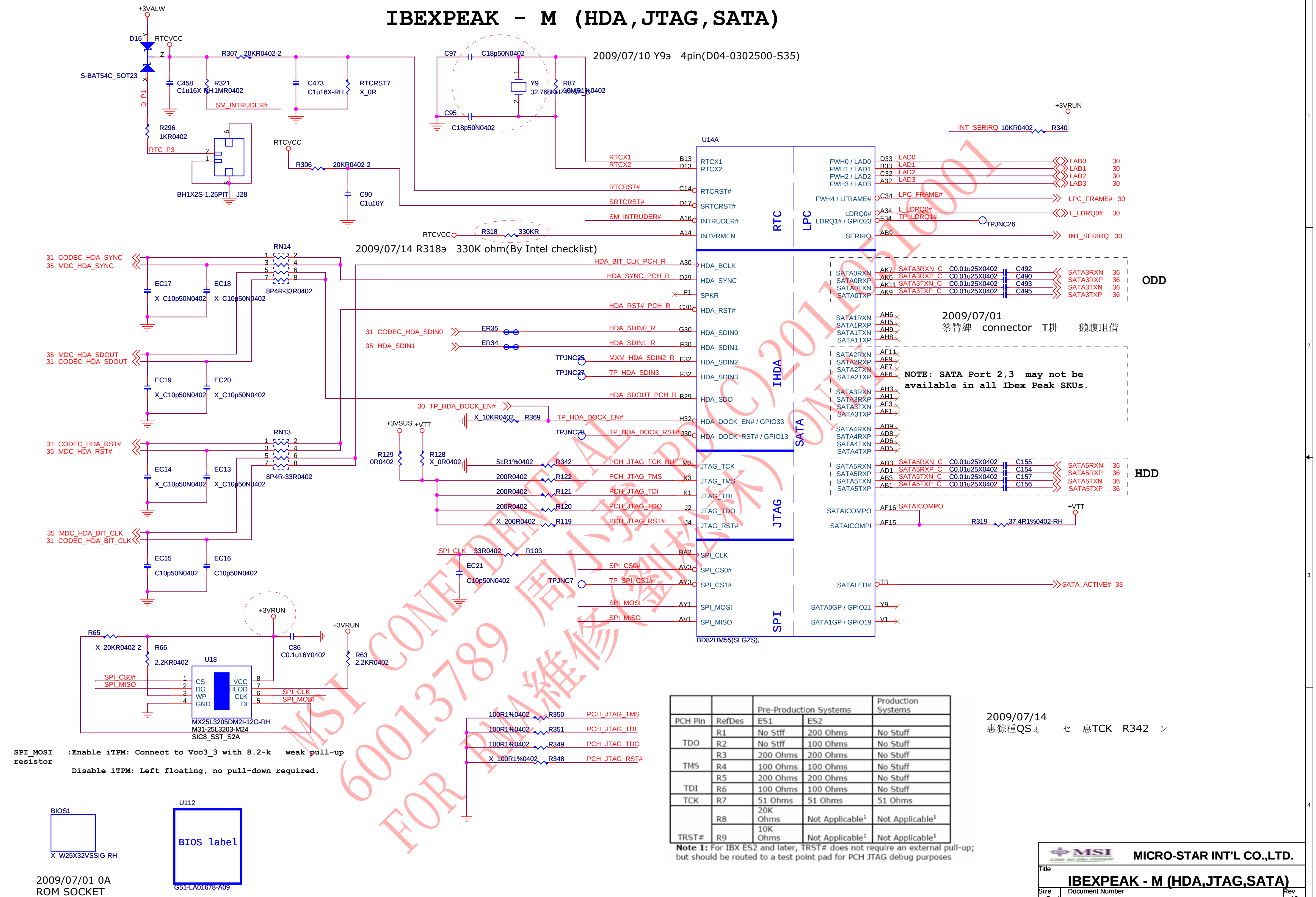
IBEXPEAK - M (HDA,JTAG,SATA)



2009/07/10 Y9϶ 4pin(D04-0302500-S35)

2009/07/14 R318϶ 330K ohm(By Intel checklist)

2009/07/01 箓箐緈 connector T耕 獭腹珇借

NOTE: SATA Port 2,3 may not be available in all Ibex Peak SKUs.

PCH Pin	RefDes	Pre-Production Systems ES1	Pre-Production Systems ES2	Production Systems
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	200 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

2009/07/14 惠䑮種QSぇ セ 惠TCK R342 ン

SPI_MOSI :Enable iTPM: Connect to Vcc3_3 with 8.2-k weak pull-up resistor

Disable iTPM: Left floating, no pull-down required.

2009/07/01 0A
ROM SOCKET

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (HDA,JTAG,SATA)

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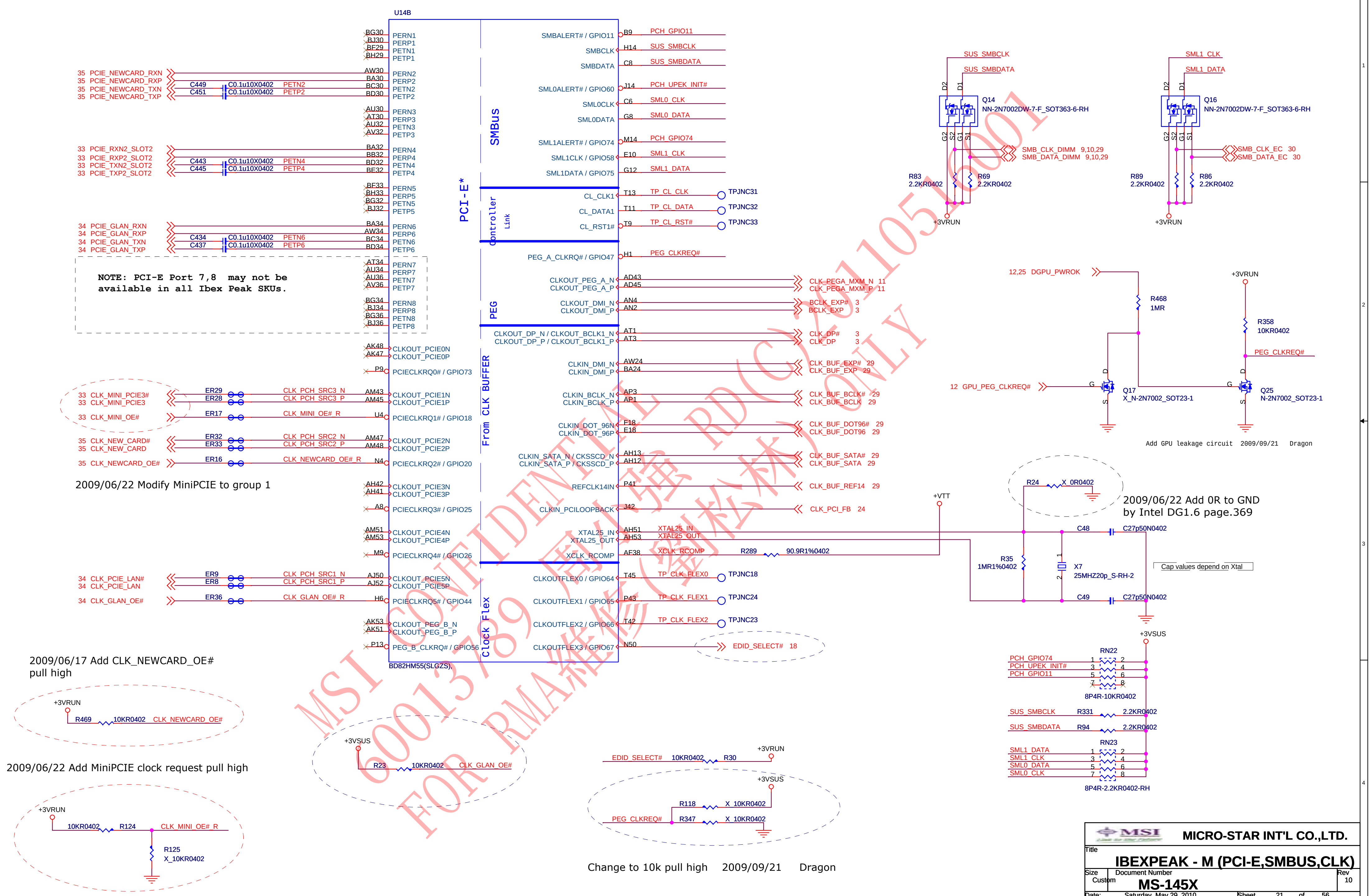
IBEXPEAK - M (PCI-E,SMBUS,CLK)



MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (PCI-E,SMBUS,CLK)	
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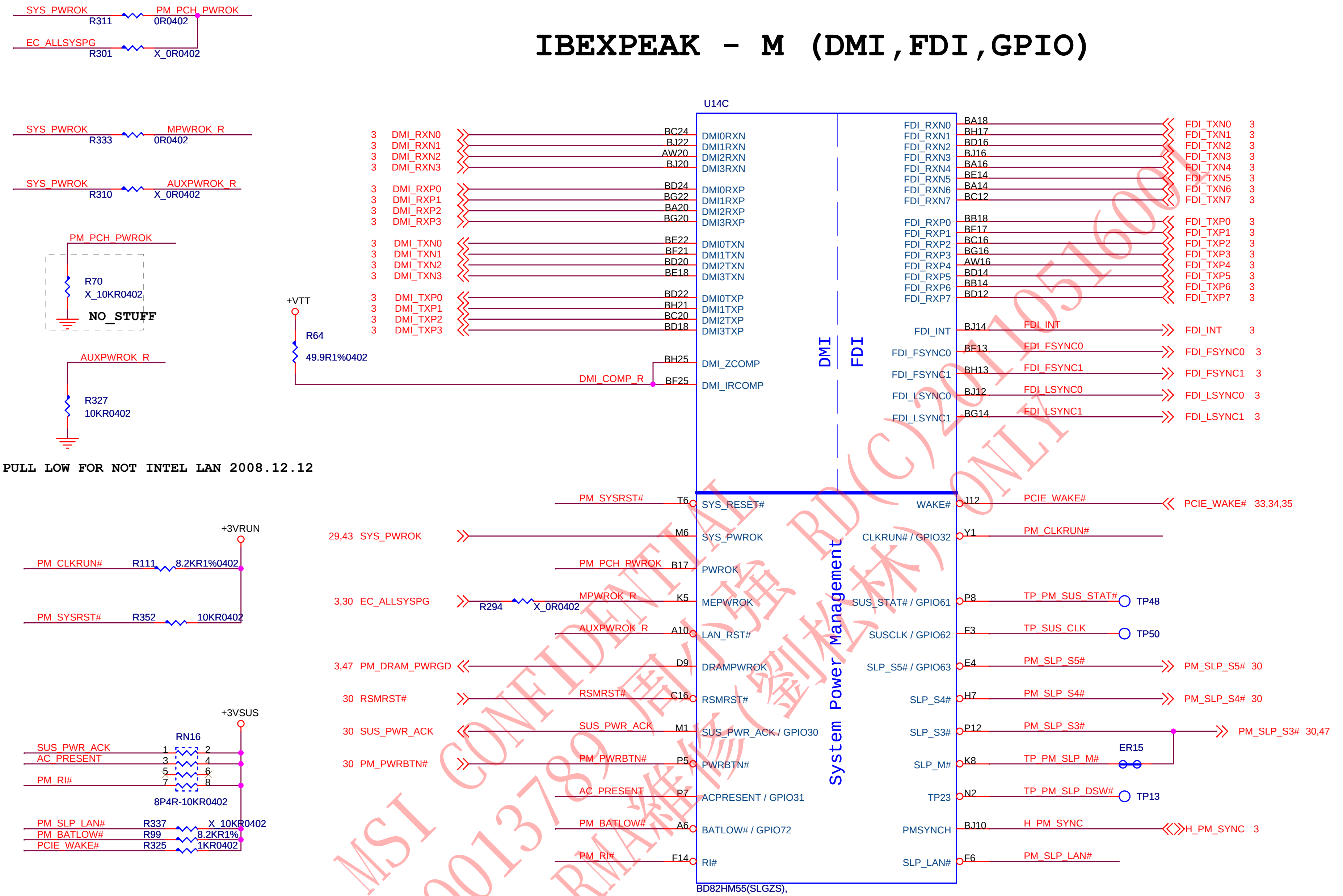
IBEXPEAK - M (DMI,FDI,GPIO)



MSI
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Title
IBEXPEAK - M (DMI,FDI,GPIO)

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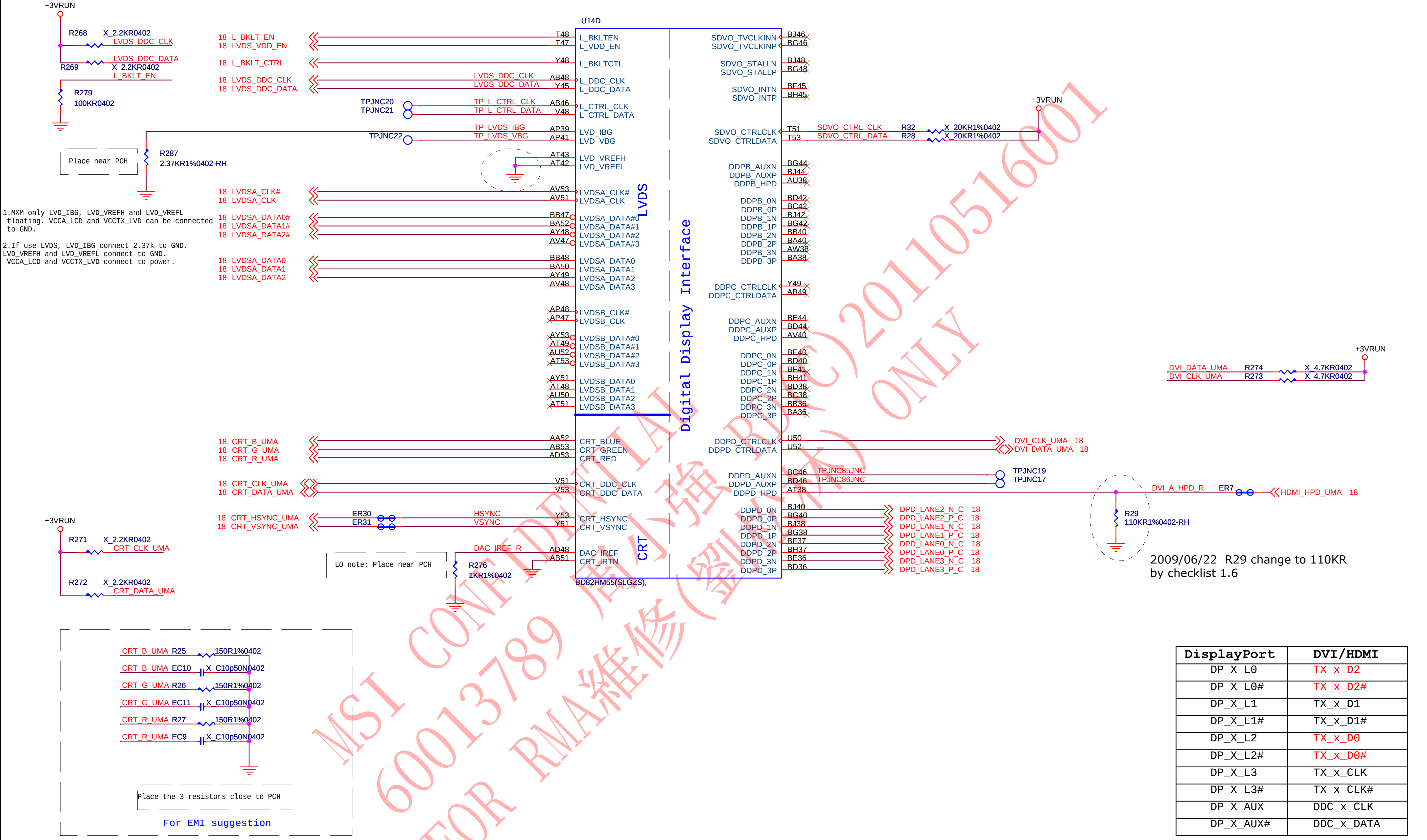
IBEXPEAK - M (LVDS,DDI)



1.MXM only LVD_IBG, LVD_VREFH and LVD_VREFL floating. VCCA_LCD and VCCTX_LVD can be connected to GND.

2.If use LVDS, LVD_IBG connect 2.37k to GND. LVD_VREFH and LVD_VREFL connect to GND. VCCA_LCD and VCCTX_LVD connect to power.

DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (LVDS,DDI)

Size: Custom | Document Number: MS-145X | Rev: 10

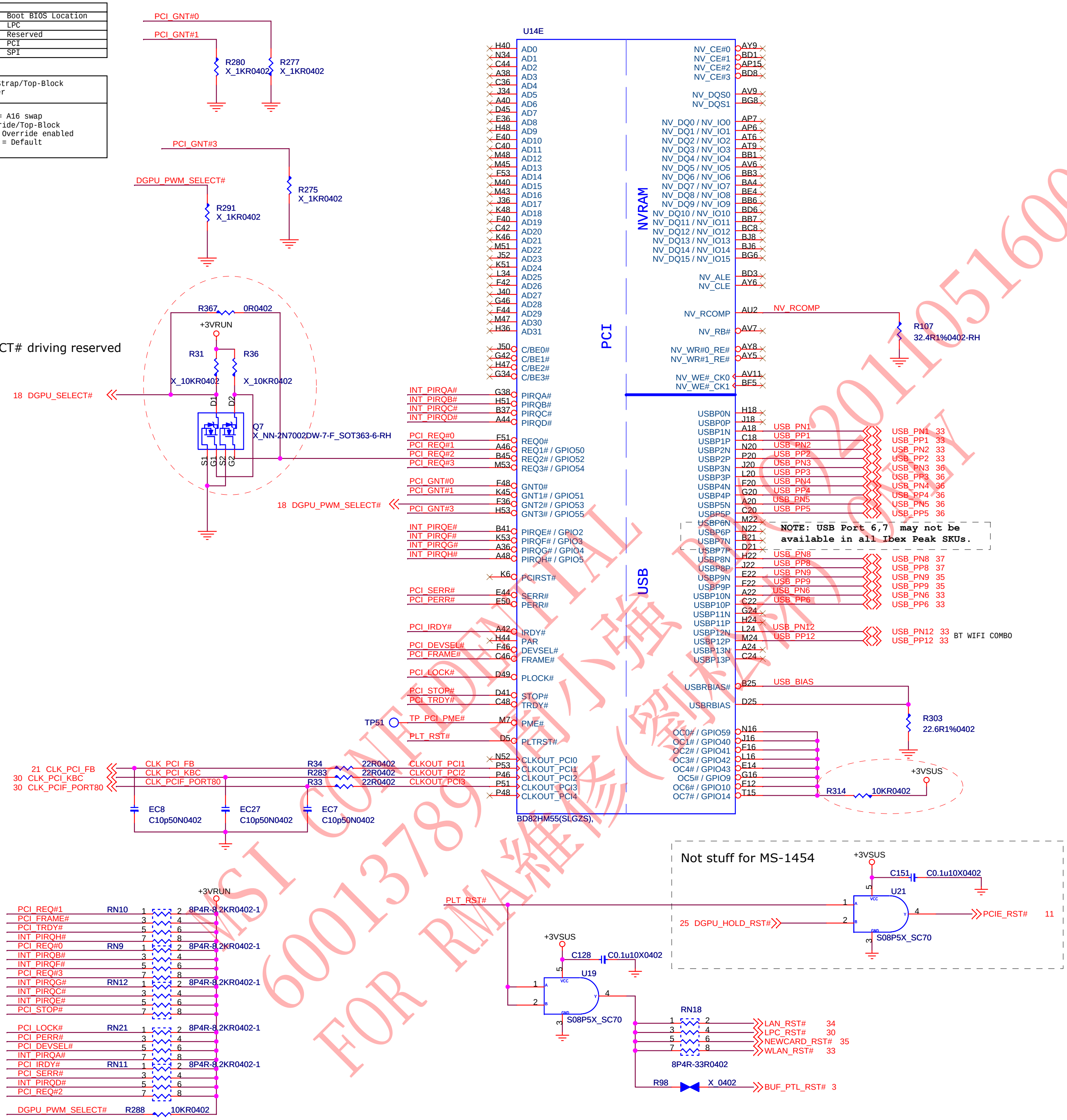
Date: Saturday, May 29, 2010 | Sheet 23 of 56

IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

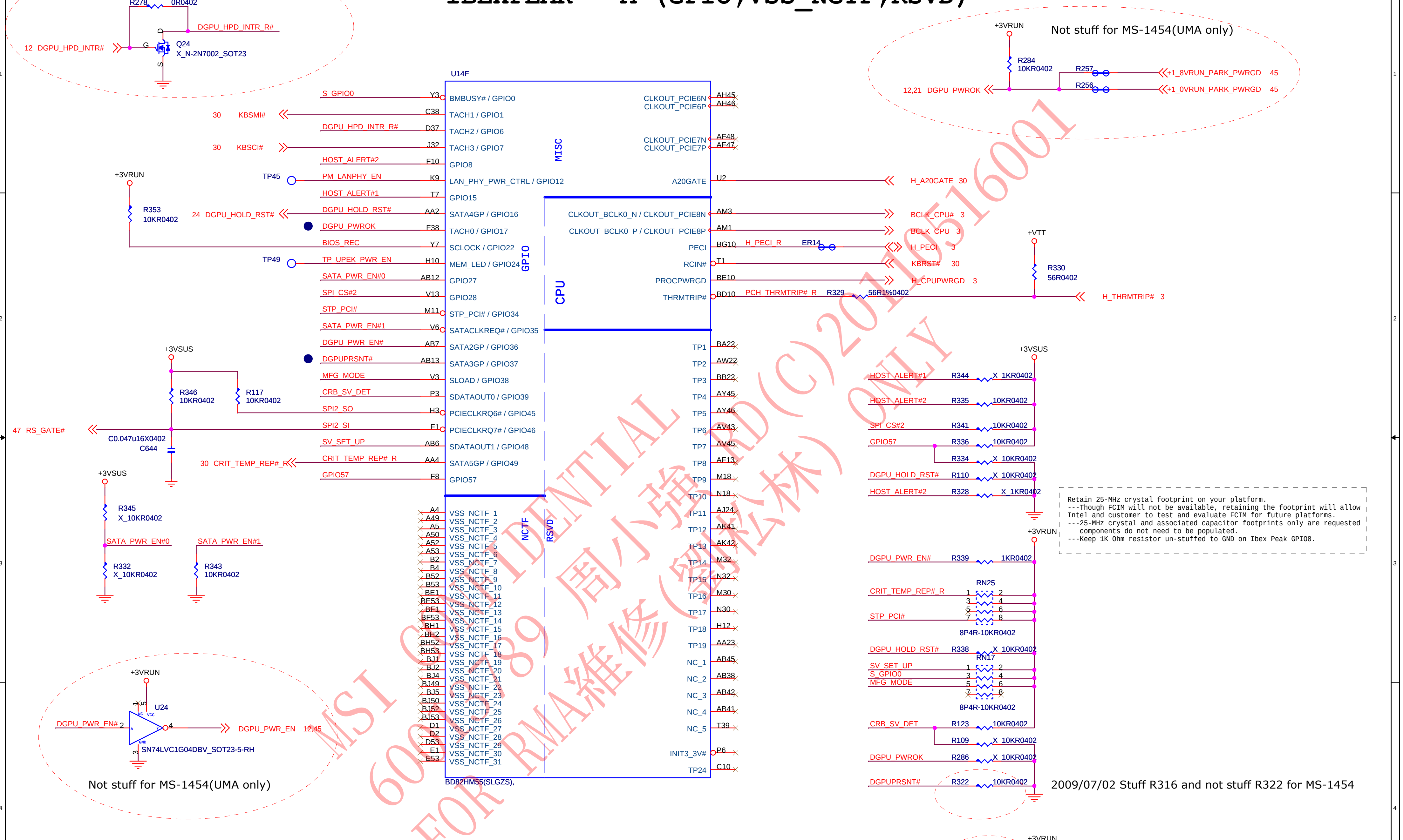
2009/06/26 For DGPU_SELECT# driving reserved
(No need for MS-1454)
R367 not stuff for MS-1454



MICRO-STAR INT'L CO.,LTD.		
Title: IBEXPEAK - M (PCI,USB,NVRAM)		
Size: Custom	Document Number: MS-145X	Rev: 10
Date: Saturday, May 29, 2010	Sheet 24 of 56	

IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

2009/07/01 Combine Park 1.8V and 1.0V to DGPU_PWROK

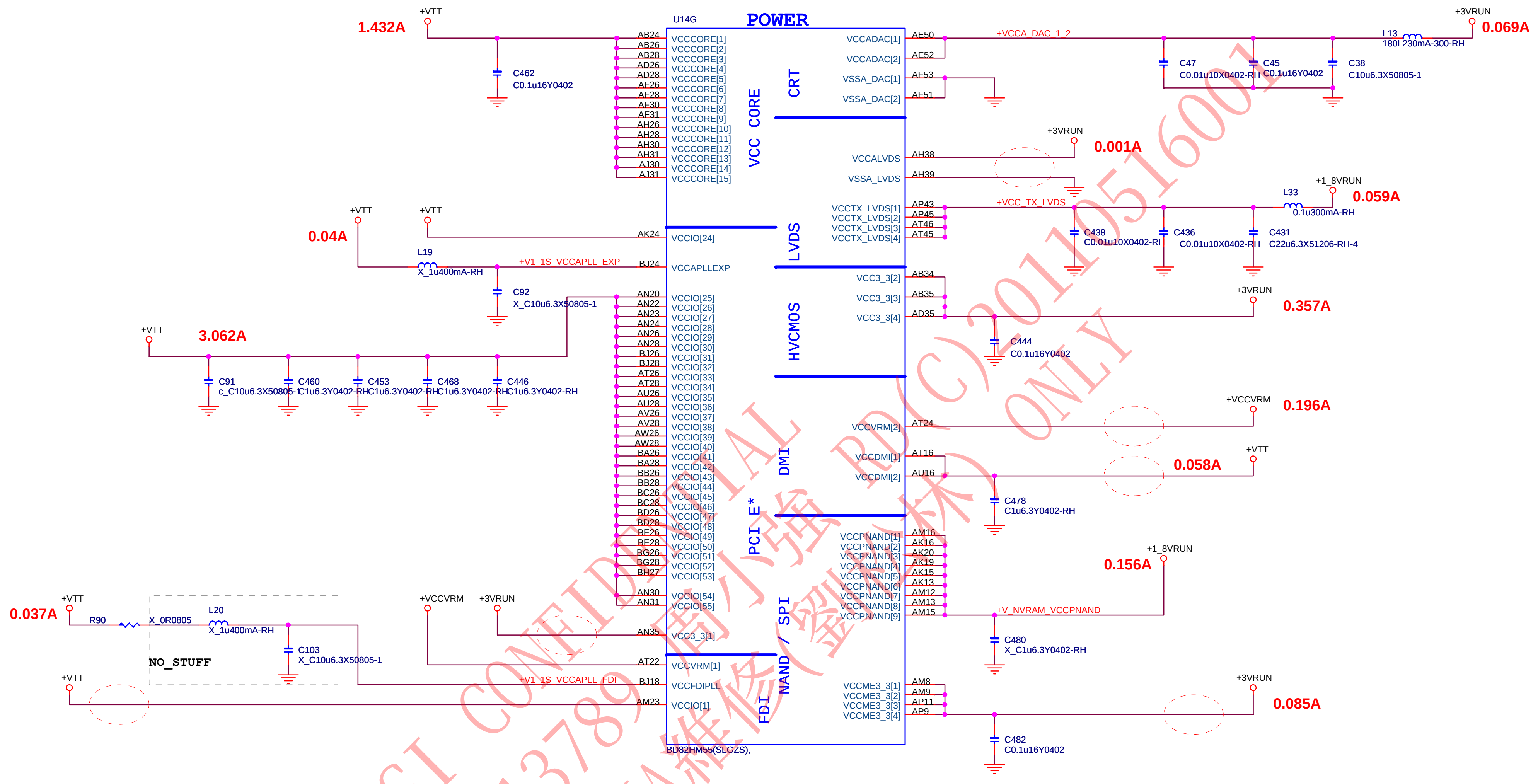


Retain 25-MHz crystal footprint on your platform.
---Though FCIM will not be available, retaining the footprint will allow Intel and customer to test and evaluate FCIM for future platforms.
---25-MHz crystal and associated capacitor footprints only are requested components do not need to be populated.
---Keep 1K Ohm resistor un-stuffed to GND on Ibex Peak GPIO8.

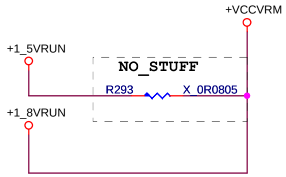
2009/07/02 Stuff R316 and not stuff R322 for MS-1454

MICRO-STAR INT'L CO.,LTD.		
Title: IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)		
Size: Custom	Document Number: MS-145X	Rev: 10
Date: Saturday, May 29, 2010	Sheet 25 of 56	

IBEXPEAK - M (POWER)



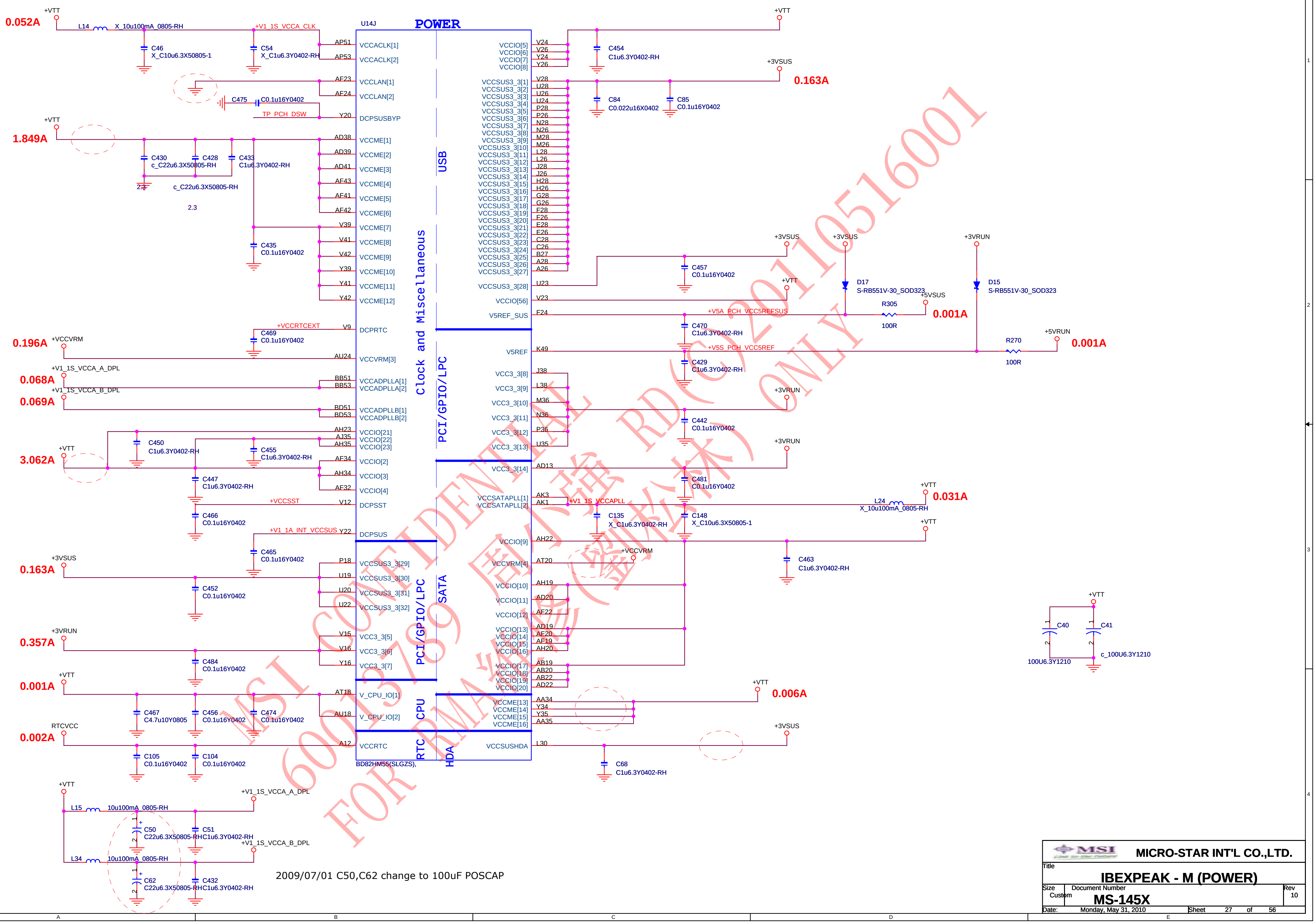
The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCACLk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (POWER)	
Size: Custom	Document Number: MS-145X	Rev: 10
Date: Saturday, May 29, 2010	Sheet 26 of 56	

IBEXPEAK - M (POWER)



2009/07/01 C50,C62 change to 100uF POSCAP

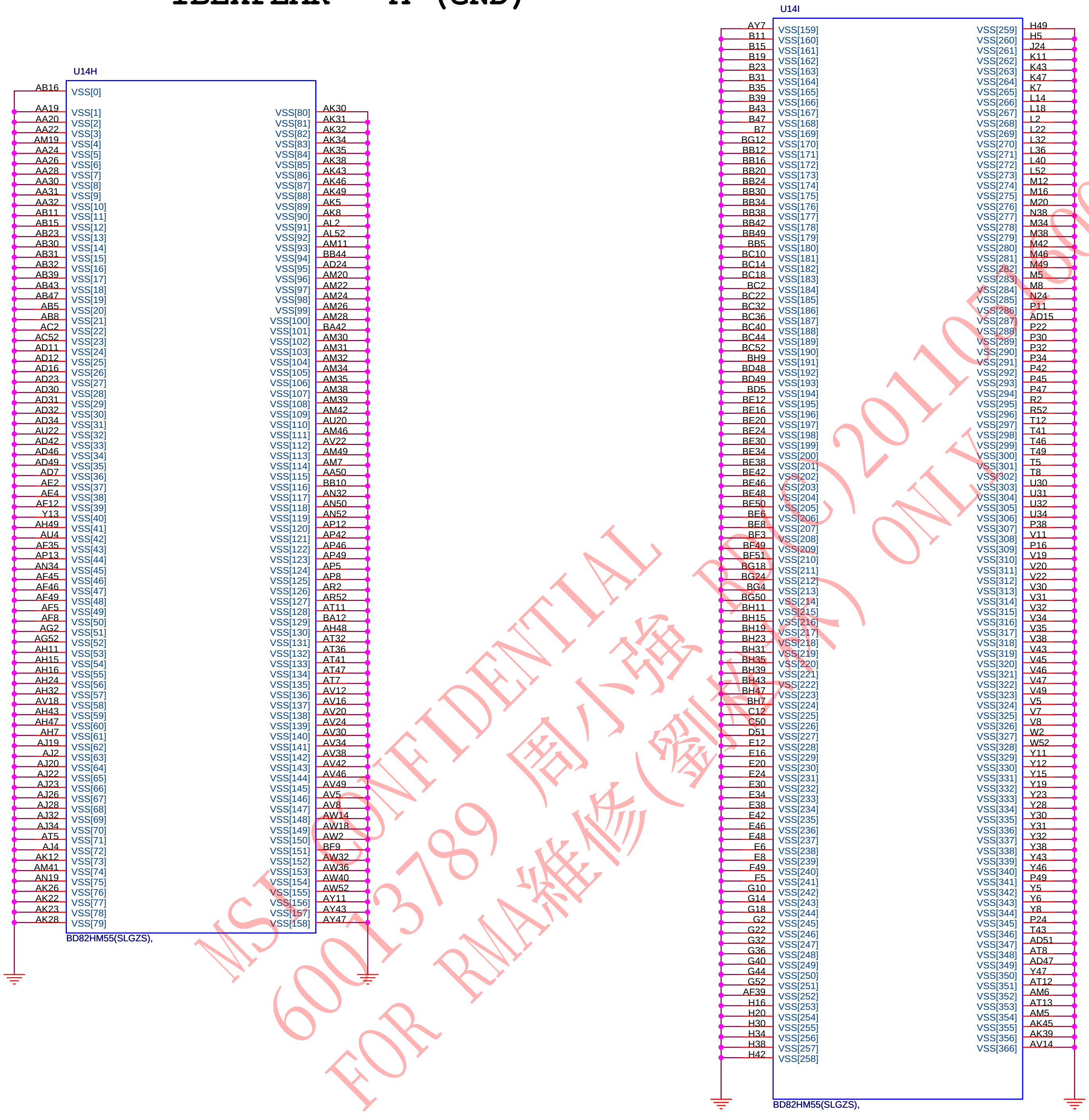
MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (POWER)

Size: Custom | Document Number: MS-145X | Rev: 10

Date: Monday, May 31, 2010 | Sheet 27 of 56

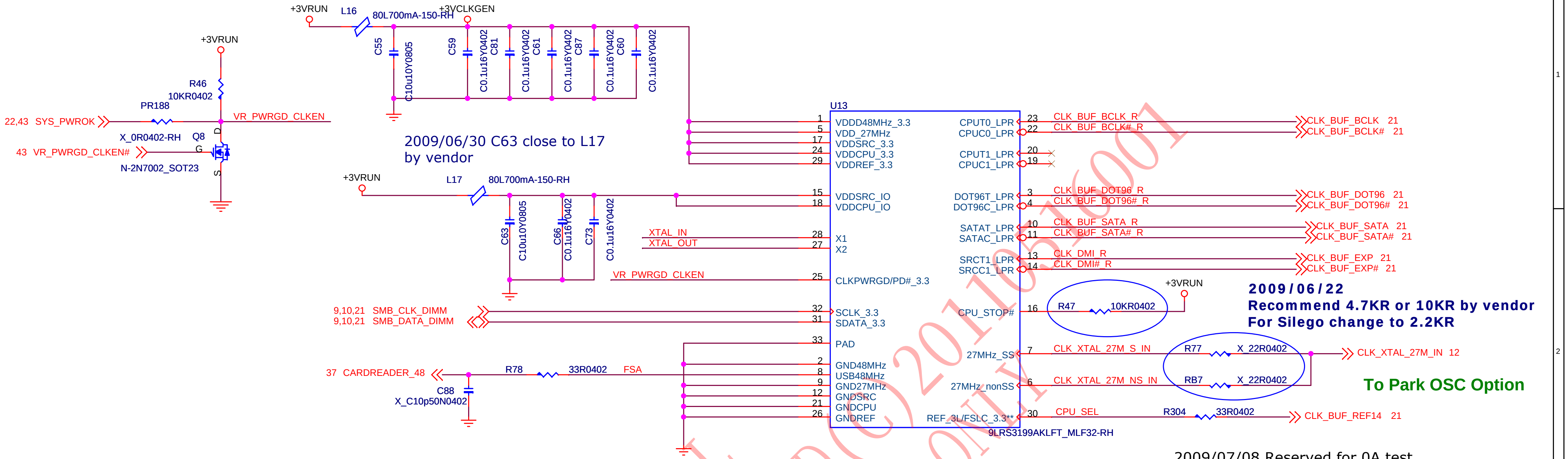
IBEXPEAK - M (GND)



MICRO-STAR INT'L CO.,LTD.

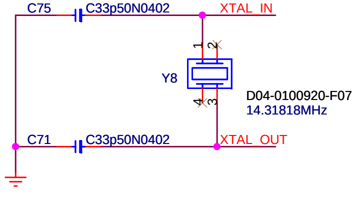
Title	IBEXPEAK - M (GND)	
Size: Custom	Document Number: MS-145X	Rev: 10
Date: Saturday, May 29, 2010	Sheet 28 of 56	

C59 Close to L16 ; C60,C61,C81,C87 Close to power pin



2009/07/08 Reserved for 0A test
R3211 is for Spread clock(Default use)
RB8 is for non-Spread clock

2009/07/08
Y4传Θ49S type(cost down as MS-1122)

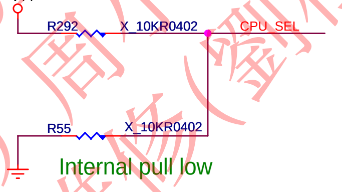


Capacity select

If Cload=20pf C71/C75=33pf

If Cload=32pf C71/C75=56pf

2009/06/30 R292 not stuff



Internal pull low

For CPU frequency select (133MHz)

CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

Clock GEN. Vendor Table

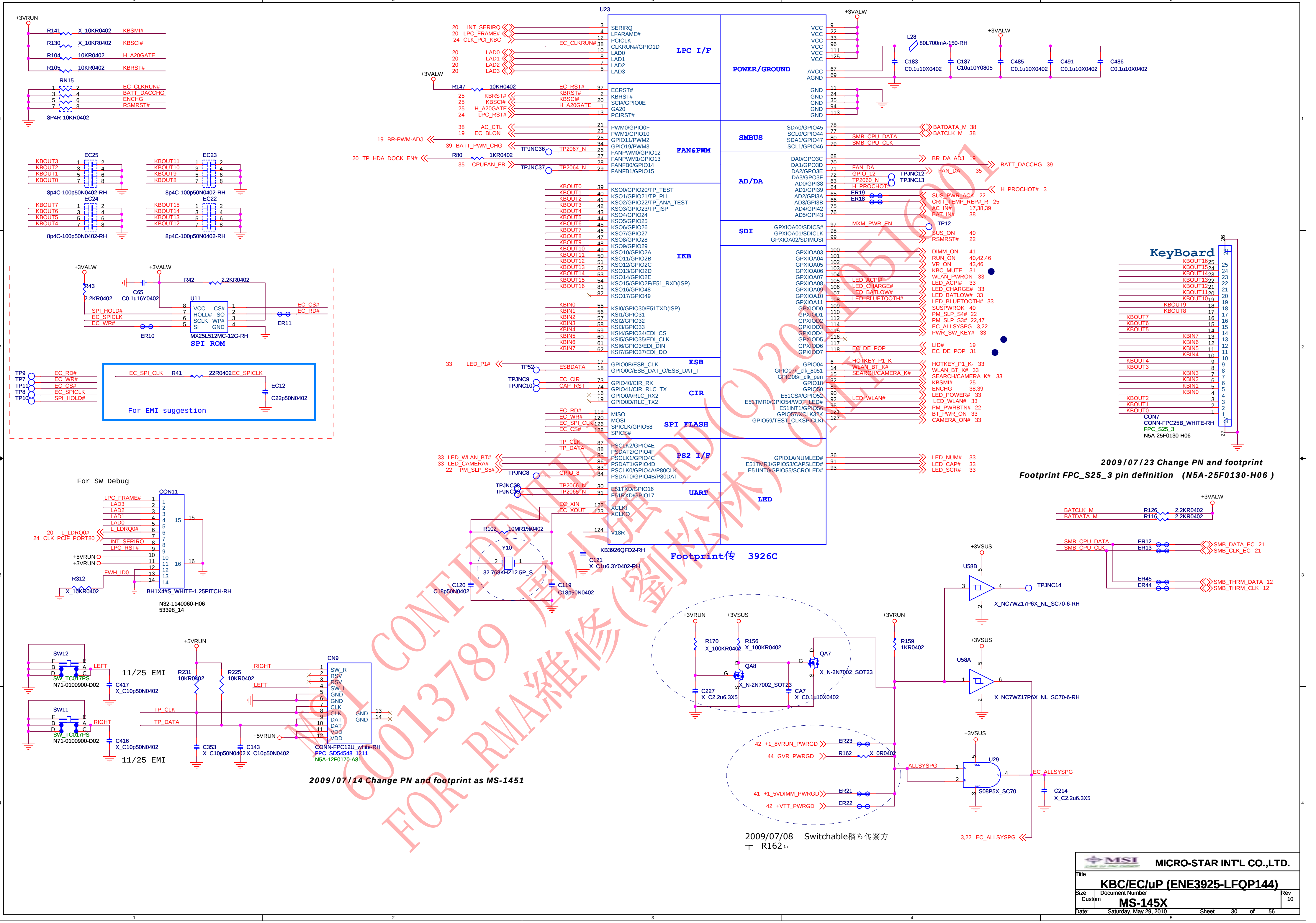
	9LRS3199	SLG8SP587V
VDDIO spec	0.9975~3.465	1.05~3.466
BOM	R39 stuff	R40 stuff

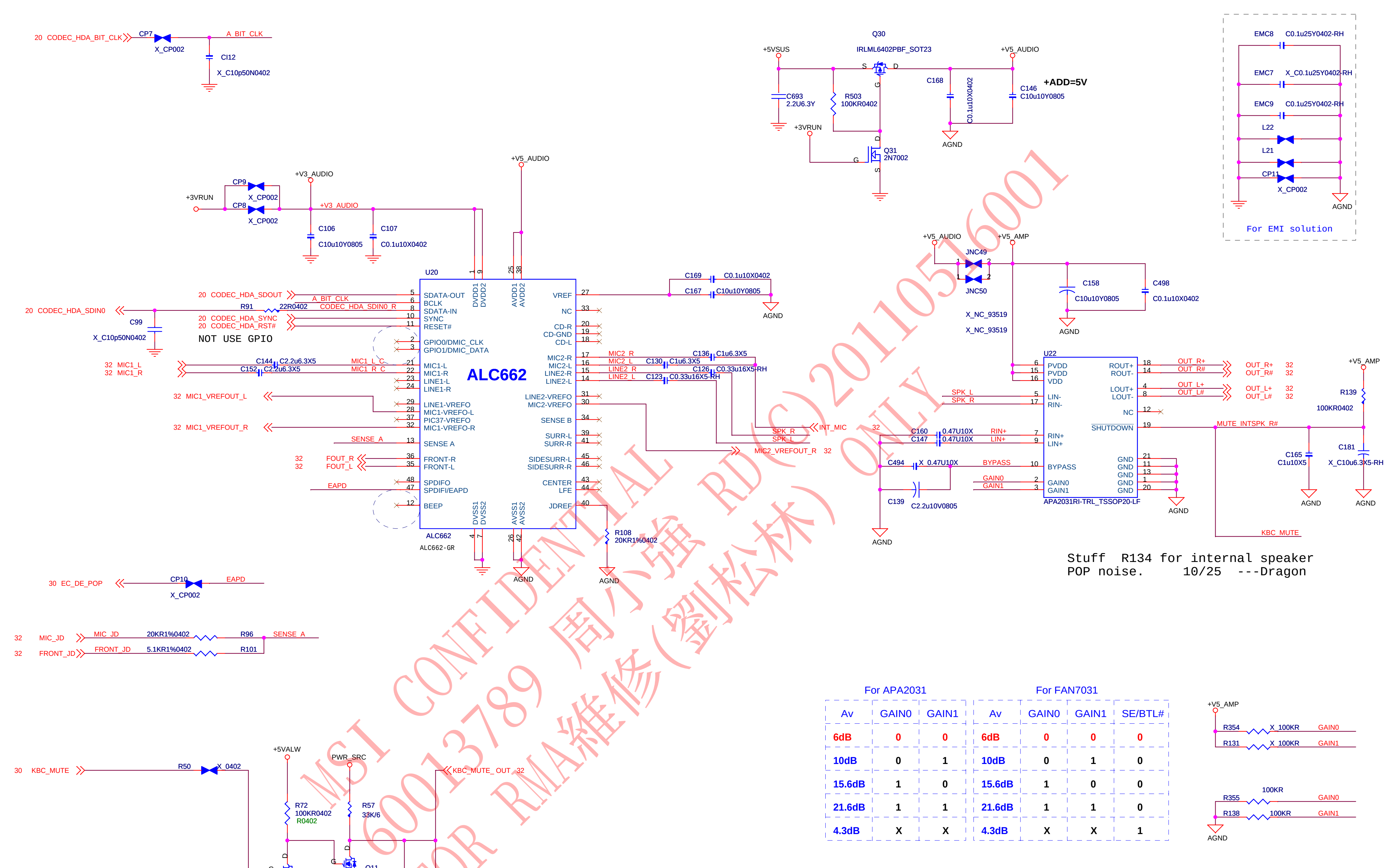
MICRO-STAR INT'L CO.,LTD.

Title: Clock Generator (9LRS3199AKLFT)

Size: Custom | Document Number: MS-145X | Rev: 10

Date: Saturday, May 29, 2010 | Sheet 29 of 56


U23
KB3926QFD2-RH
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
Footprint传 3926C
KeyBoard
CON7
CONN-FPC25B_WHITE-RH
FPC_S25_3
N5A-25F0130-H06
2009/07/23 Change PN and footprint
Footprint FPC_S25_3 pin definition (N5A-25F0130-H06)
U11
MX25L512MC-12G-RH
SPI ROM
For EMI suggestion
For SW Debug
CON11
BH1X4#S_WHITE-1.25PITCH-RH
N32-1140060-H06
53398_14
SW12
SW11
N71-0100900-D02
11/25 EMI
CN9
CONN-FPC12U_white-RH
FPC_SD54548_1211
N5A-12F0170-A81
2009/07/14 Change PN and footprint as MS-1451
Y10
32.768KHZ12.5P_S
U58B
U58A
X_NC7WZ17P6X_NL_SC70-6-RH
U29
S08P5X_SC70
QA7
QA8
X_N-2N7002_SOT23
2009/07/08 Switchable
R162
MICRO-STAR INT'L CO.,LTD.
Title
KBC/EC/uP (ENE3925-LFQP144)
Size
Custom
Document Number
MS-145X
Rev
10
Date: Saturday, May 29, 2010
Sheet 30 of 56



Stuff R134 for internal speaker
POP noise. 10/25 ---Dragon

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

For FAN7031

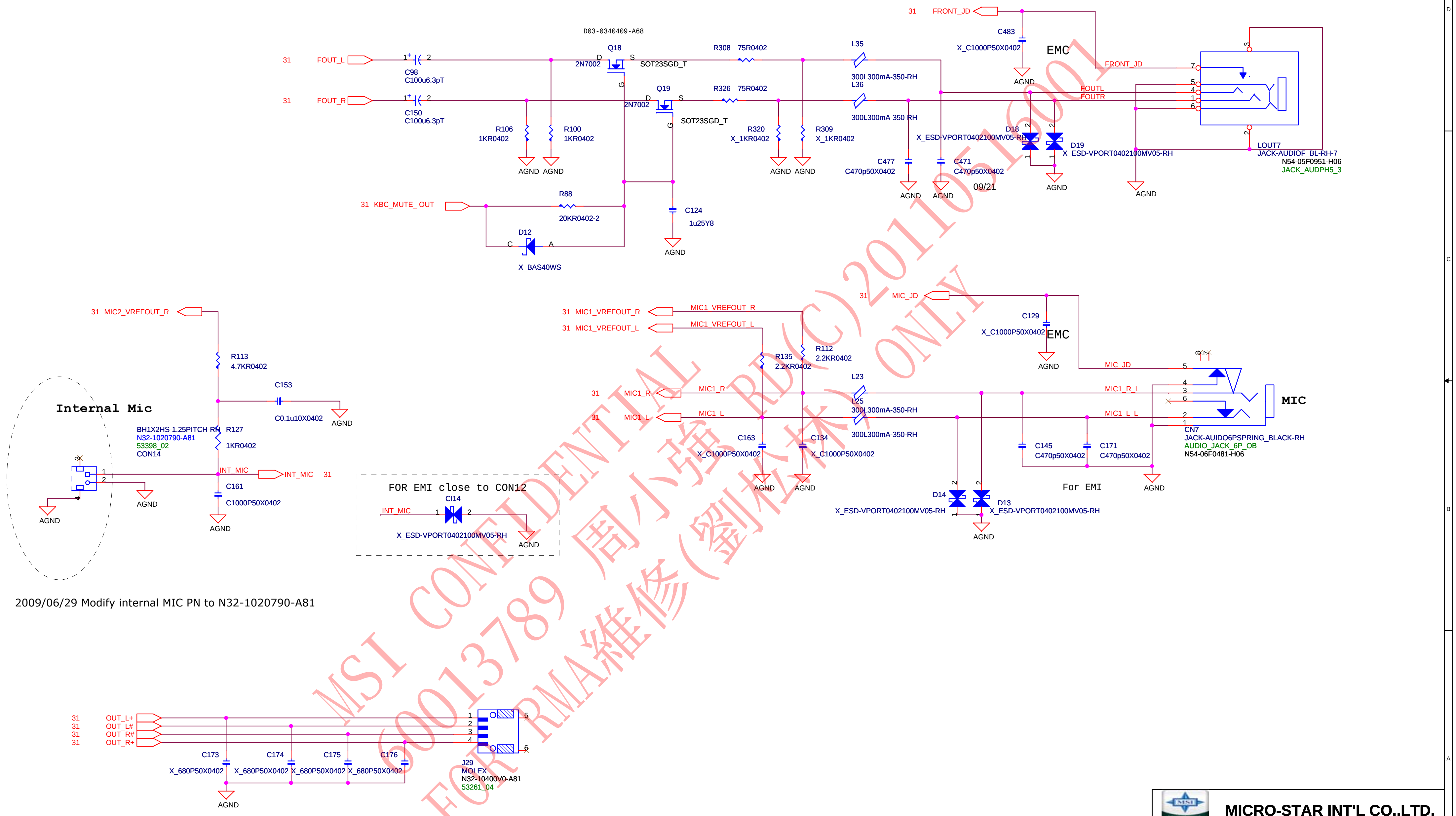
Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

MICRO-STAR INT'L CO.,LTD.

Title: AUDIO(ALC662 + AMP(APA2031)

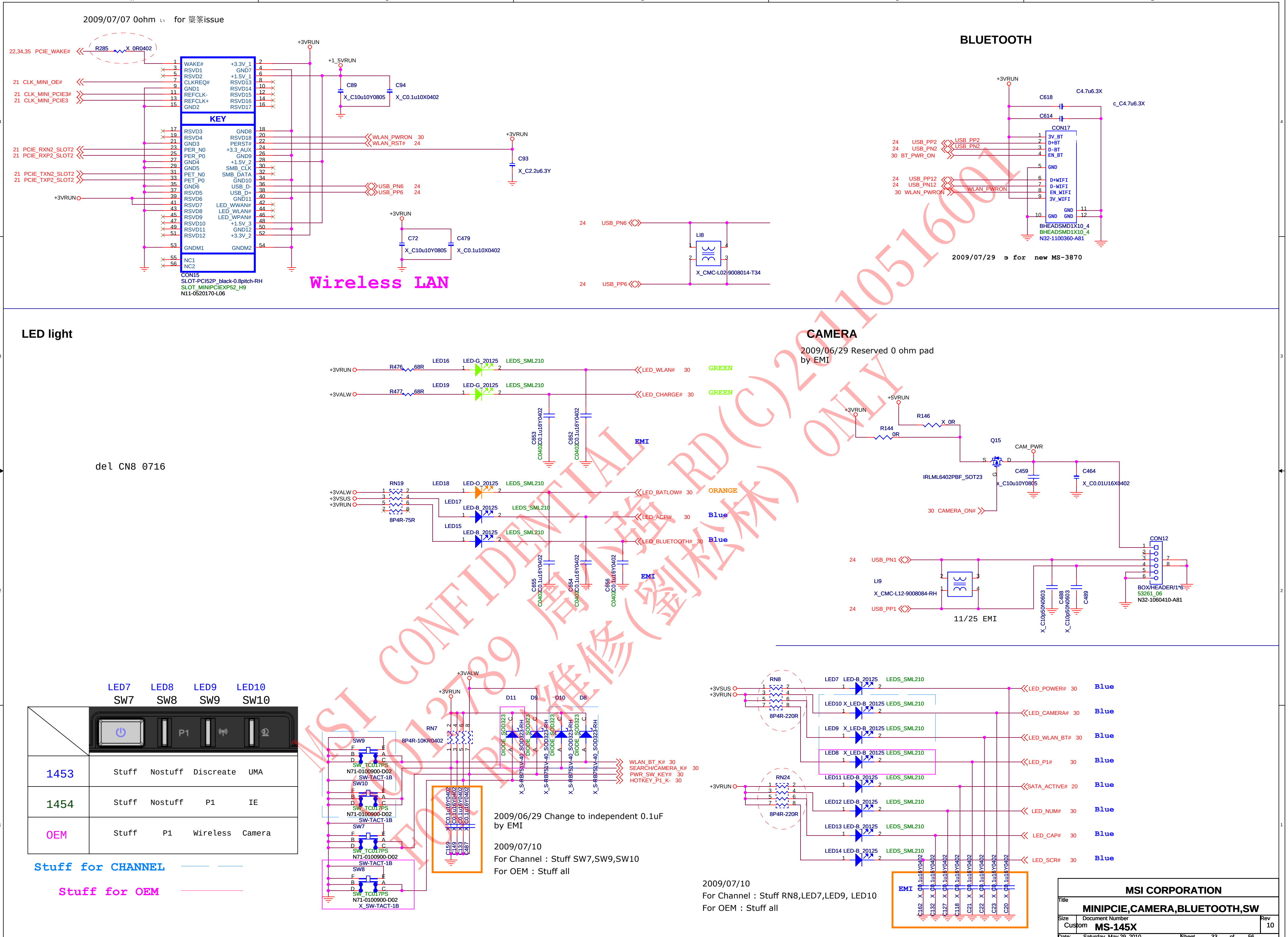
Size: Custom | Document Number: MS-145X | Rev: 10

Date: Saturday, May 29, 2010 | Sheet 31 of 56



MICRO-STAR INT'L CO.,LTD.

Title	SPK / HP / MIC		
Size: Custom	Document Number: MS-145X		Rev: 10
Date: Saturday, May 29, 2010	Sheet 32 of 56		



	LED7 SW7	LED8 SW8	LED9 SW9	LED10 SW10
1453	Stuff	Nostuff	Discreate	UMA
1454	Stuff	Nostuff	P1	IE
OEM	Stuff	P1	Wireless	Camera

Stuff for CHANNEL

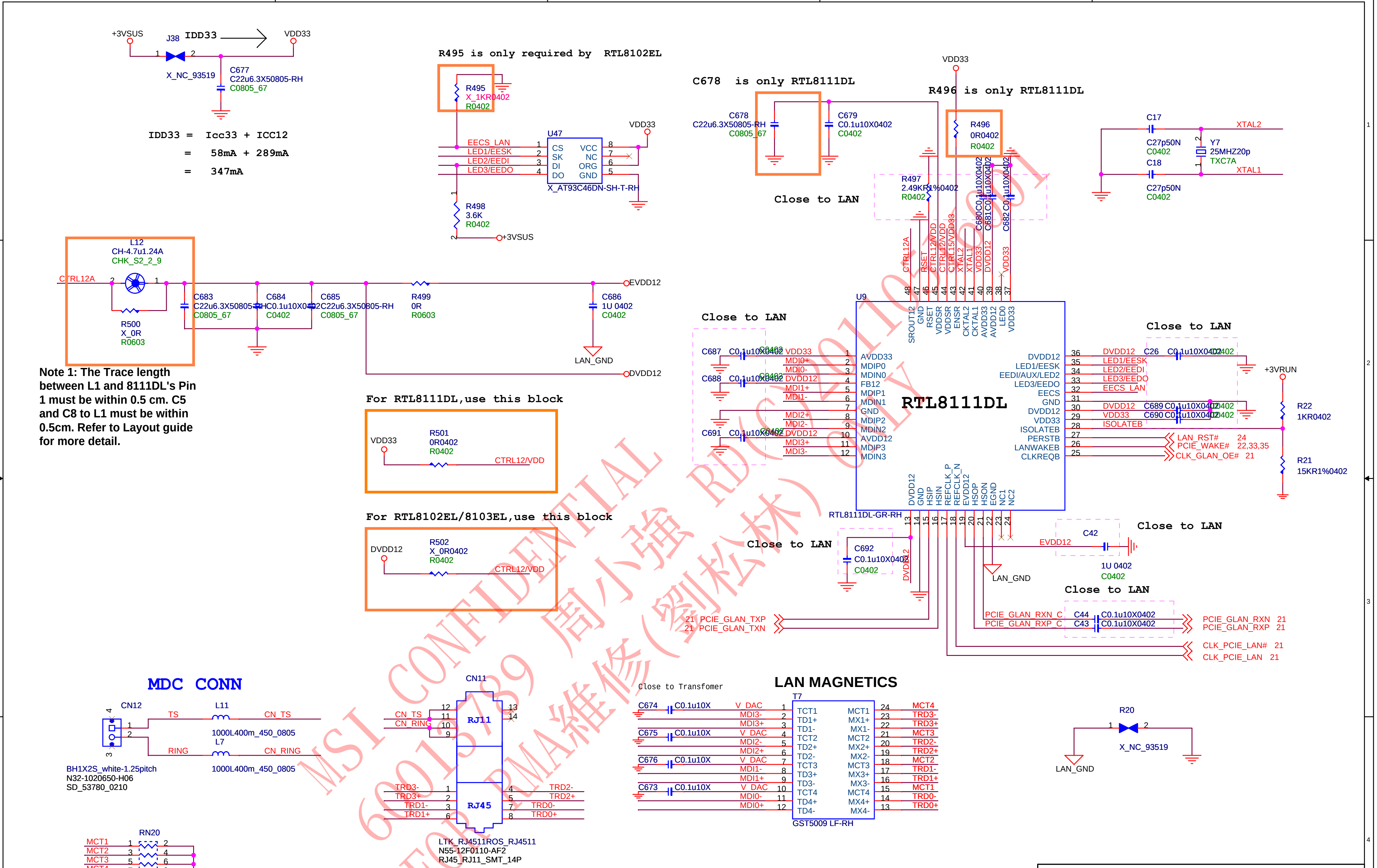
Stuff for OEM

MSI CORPORATION

Title: MINIPCIE,CAMERA,BLUETOOTH,SW

Size	Document Number	Rev
Custom	MS-145X	10

Date: Saturday, May 29, 2010 Sheet 33 of 56



MICRO-STAR INT'L CO.,LTD.

Title: **PCIE 1G LAN (RTL8111DL)**

Size	Document Number	Rev
Custom	MS-145X	10

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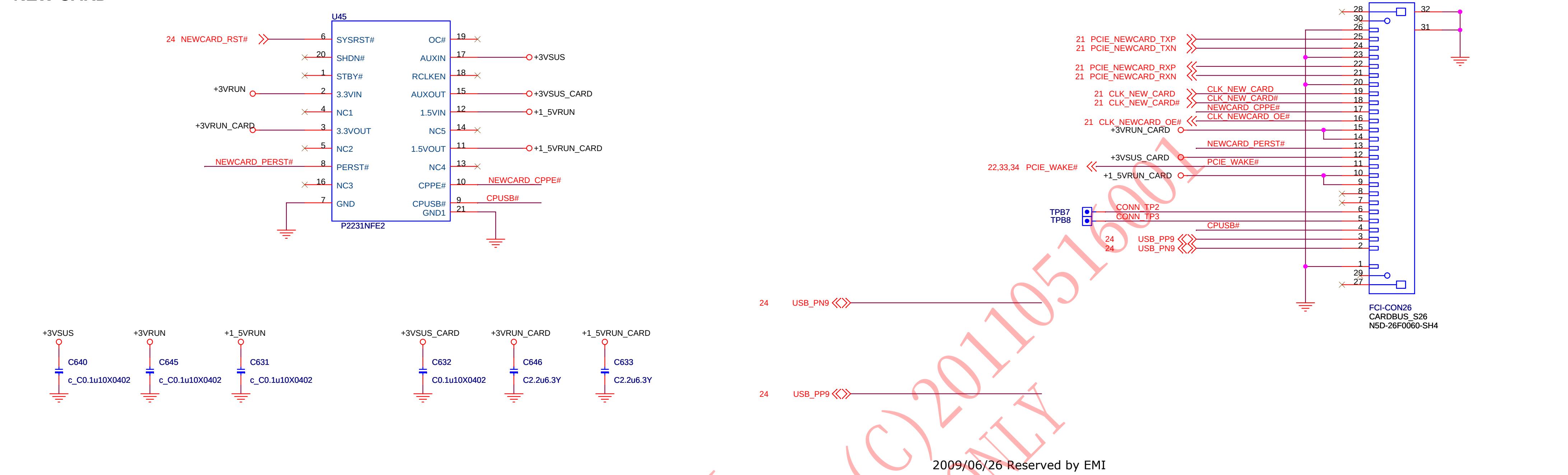
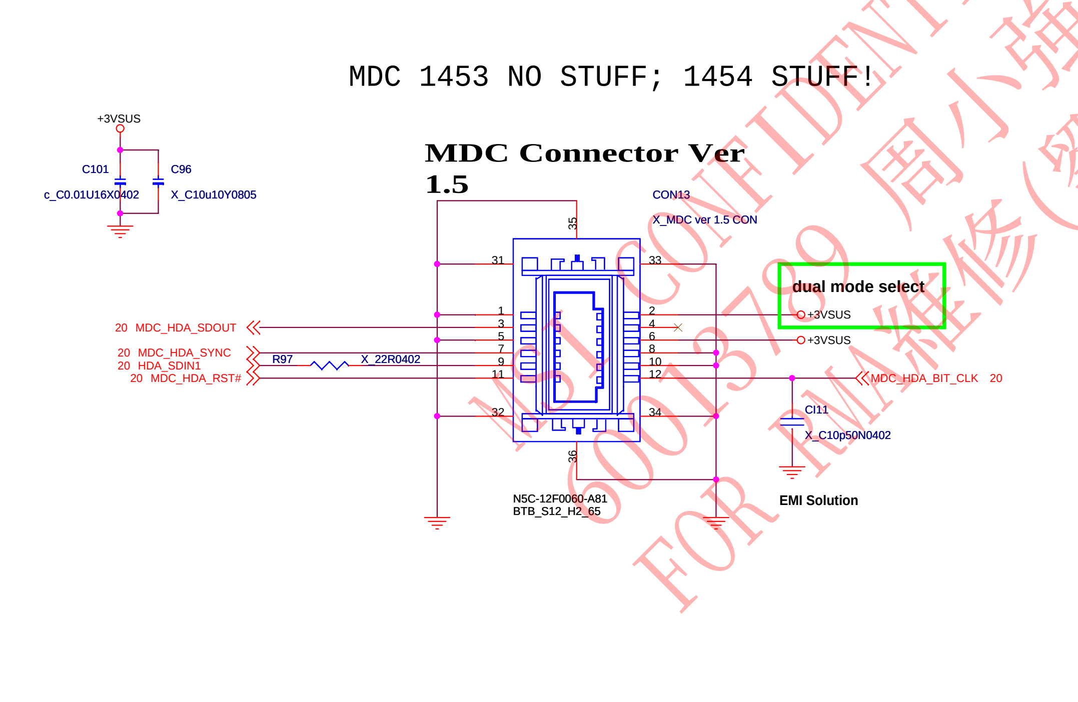
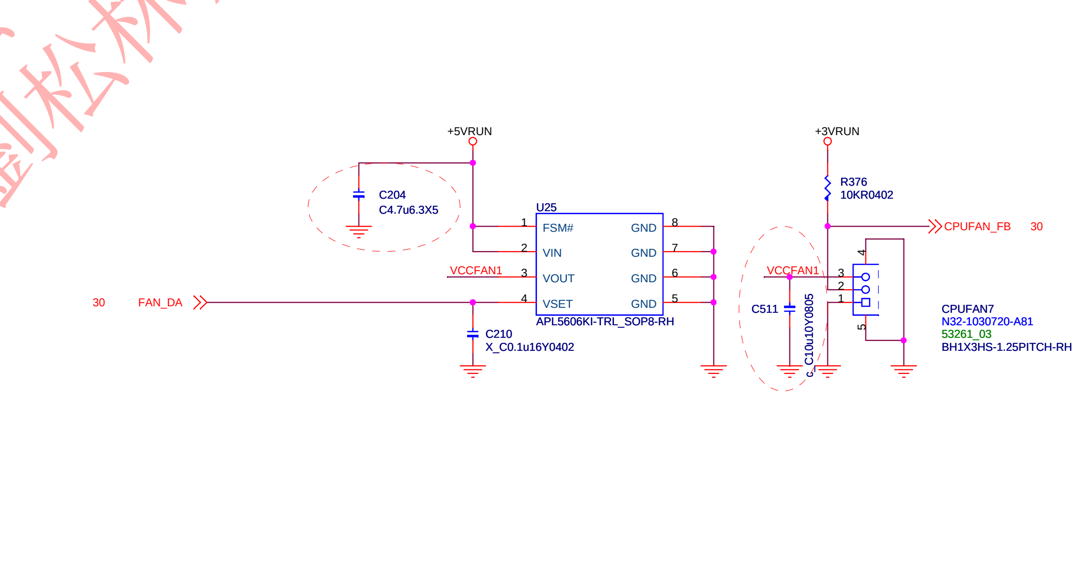
NEW CARD



MDC Connector



CPU FAN

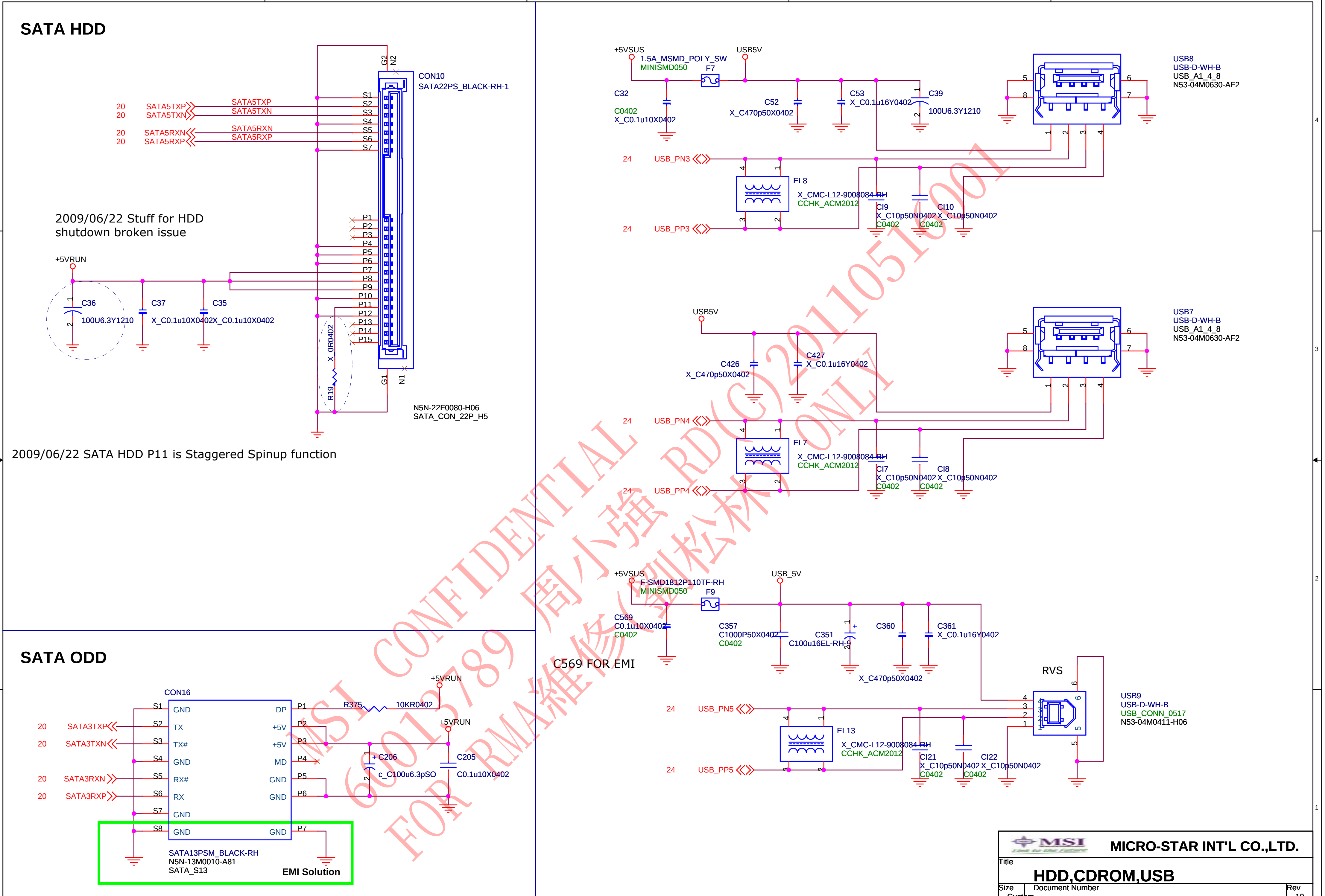


MICRO-STAR INT'L CO.,LTD.

Title: NEWCARD,FAN

Size: Custom | Document Number: MS-145X | Rev: 10

Date: | Sheet 35 of 56



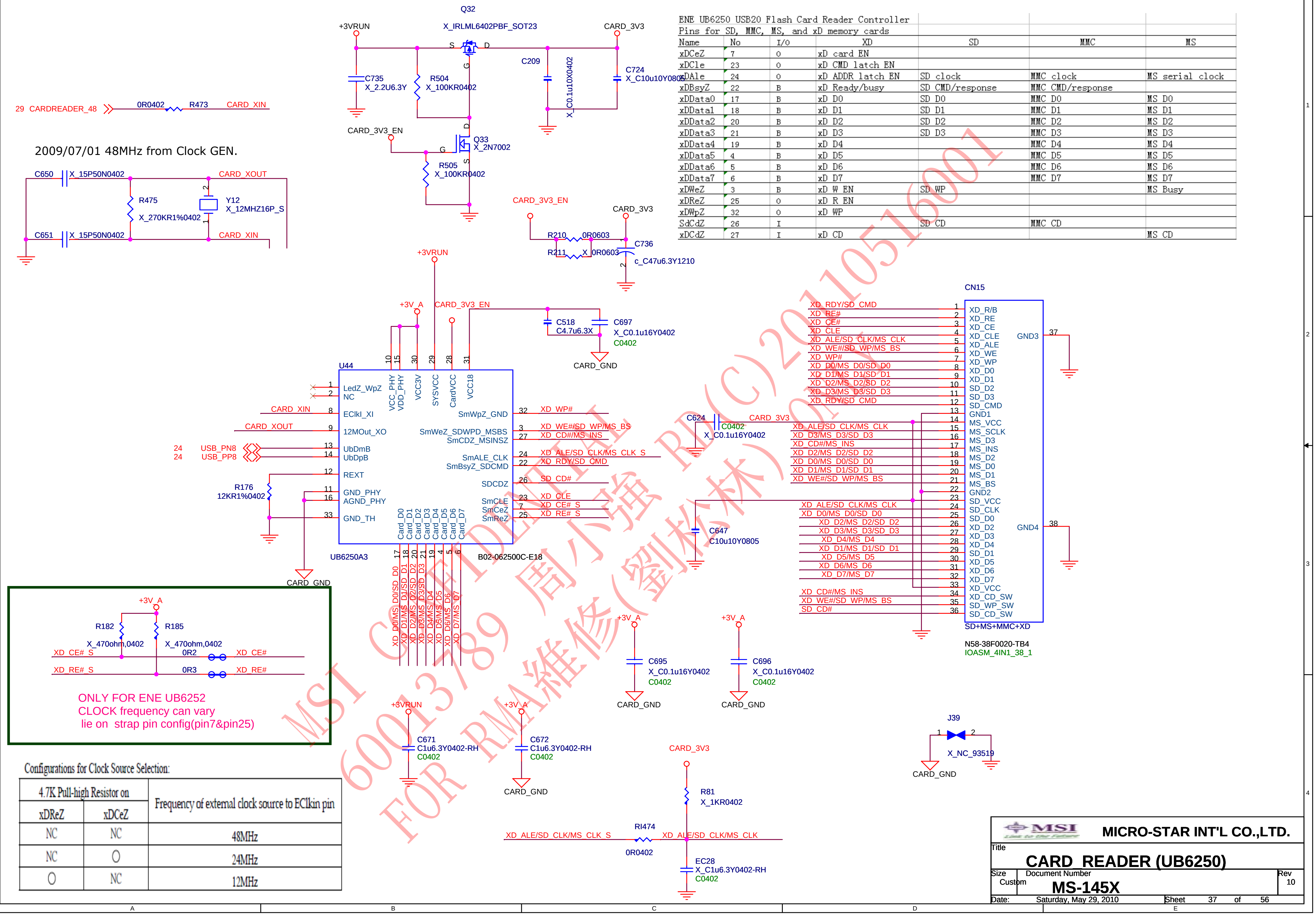
2009/06/22 Stuff for HDD
shutdown broken issue

2009/06/22 SATA HDD P11 is Staggered Spinup function

C569 FOR EMI

MSI
MICRO-STAR INT'L CO.,LTD.

Title	HDD,CDROM,USB
Size	Custom
Document Number	MS-145X
Rev	10
Date:	Saturday, May 29, 2010
Sheet	36 of 56



ENE UB6250 USB20 Flash Card Reader Controller						
Pins for SD, MMC, MS, and xD memory cards						
Name	No	I/O	XD	SD	MMC	MS
xDCeZ	7	O	xD card EN			
xDCle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDBsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SdCdZ	26	I		SD CD	MMC CD	
xDCdZ	27	I	xD CD			MS CD

Configurations for Clock Source Selection:

4.7K Pull-high Resistor on		Frequency of external clock source to EClkin pin
xDReZ	xDCeZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

MSI Link to the Future
MICRO-STAR INT'L CO.,LTD.

Title: CARD_READER (UB6250)

Size	Document Number	Rev
Custom	MS-145X	10

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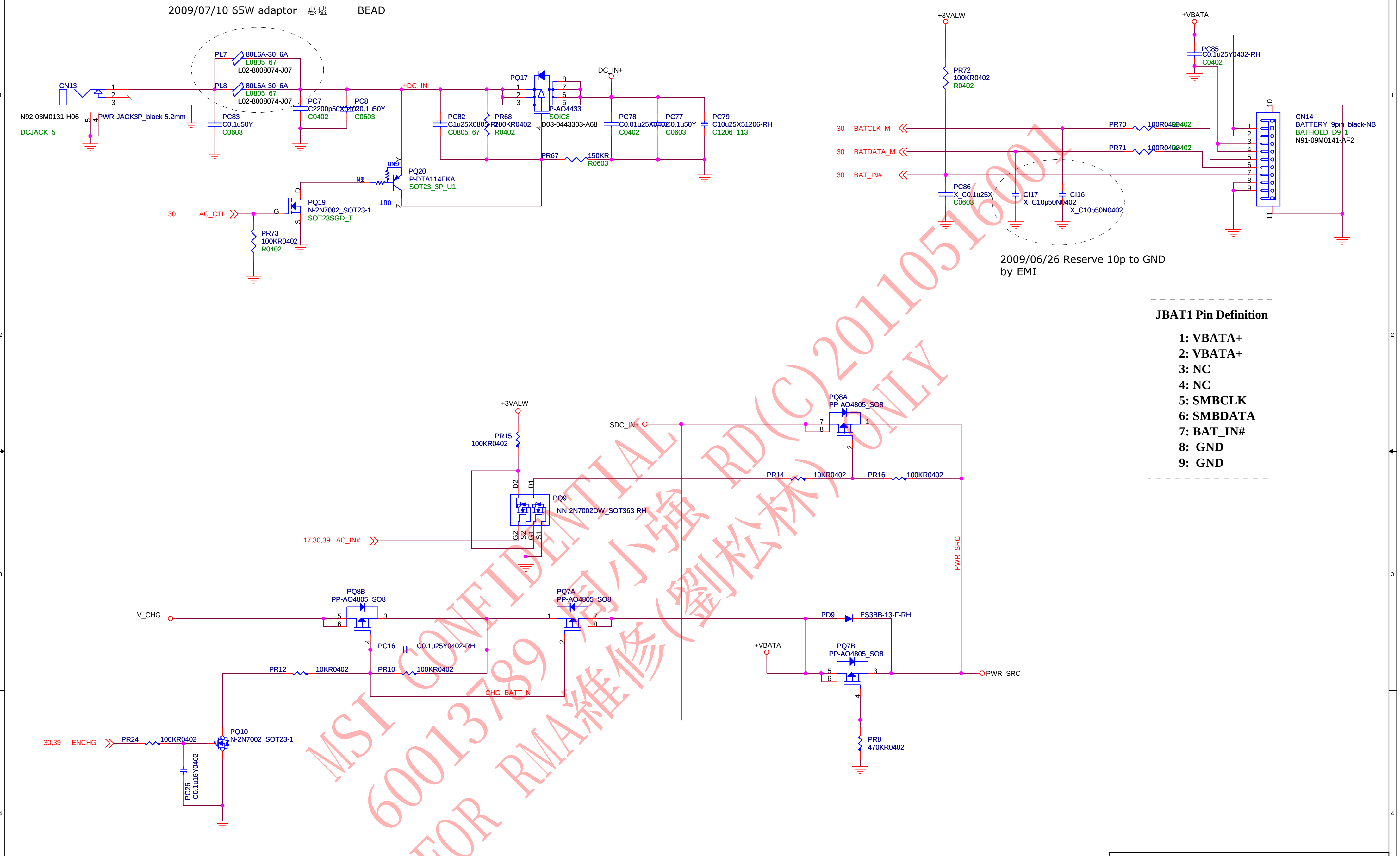


JBAT1 Pin Definition

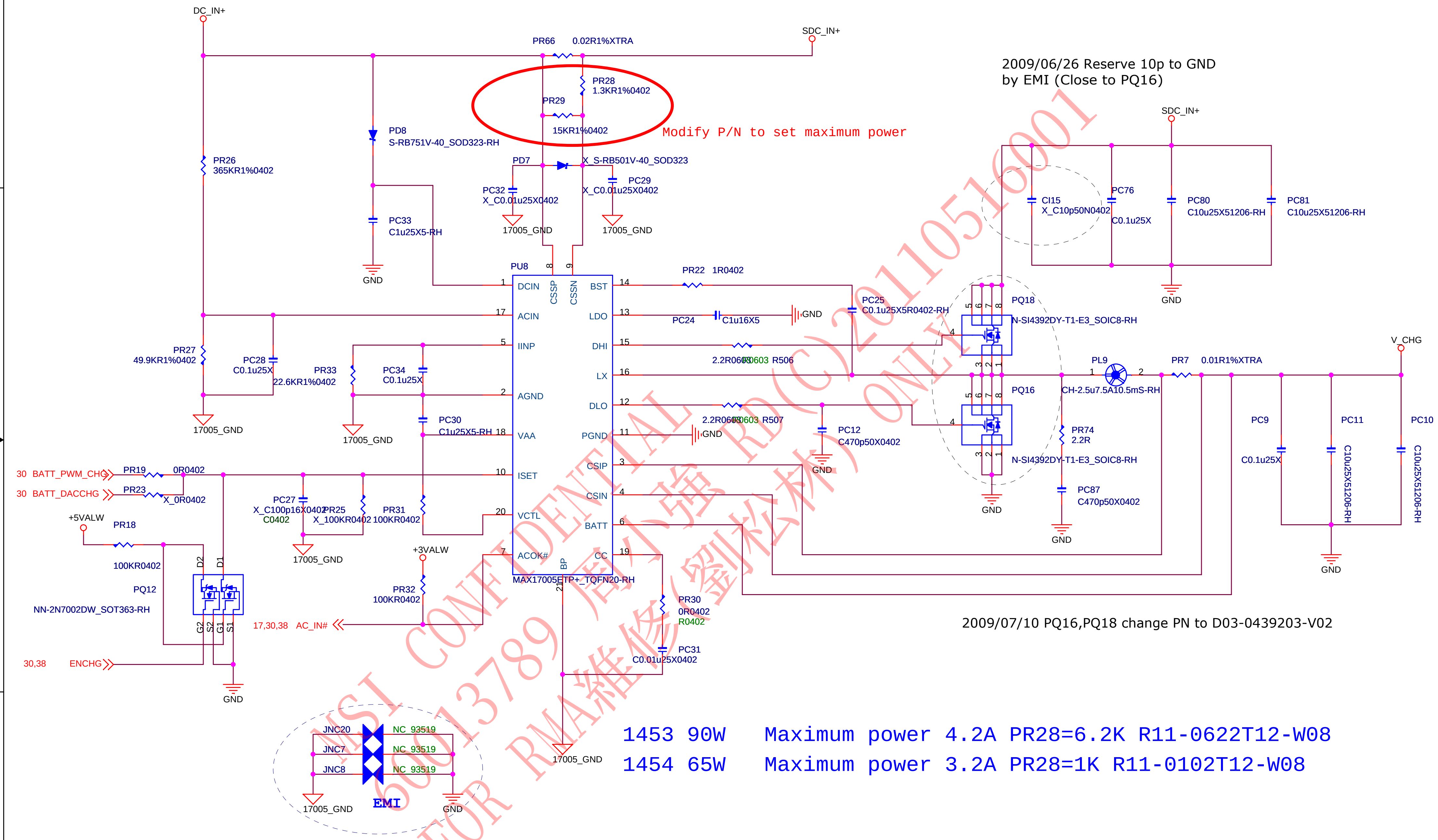
1: VBATA+
2: VBATA+
3: NC
4: NC
5: SMBCLK
6: SMBDATA
7: BAT_IN#
8: GND
9: GND

MICRO-STAR INT'L CO.,LTD.

Title: Battery Select

Size: Custom | Document Number: MS-145X | Rev: 10

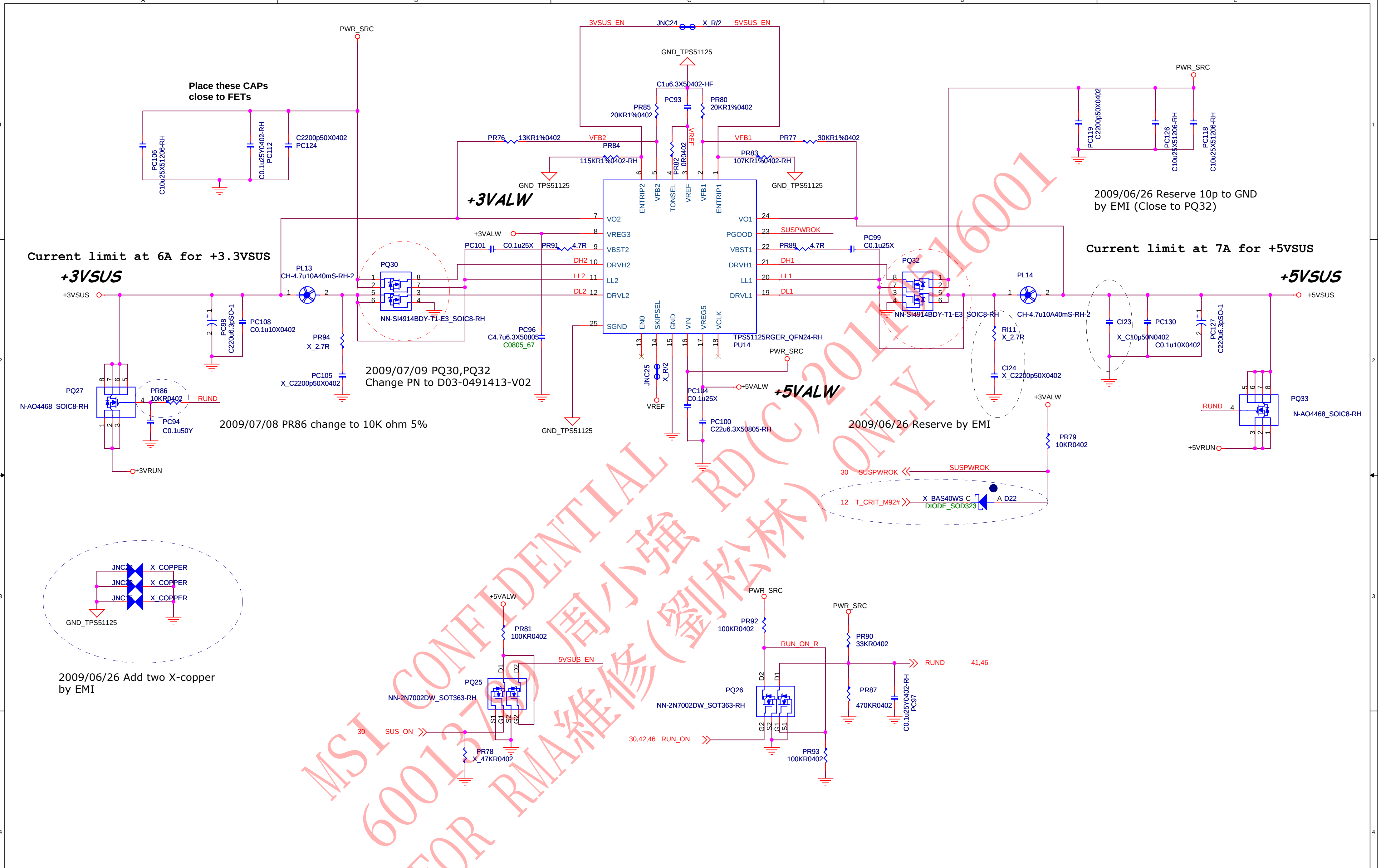
Date: Saturday, May 29, 2010 | Sheet 38 of 56



2009/06/26 Add two X-copper
by EMI

MICRO-STAR INT'L CO.,LTD.

Title	Battery Charger	
Size: Custom	Document Number: MS-145X	Rev: 10
Date: Saturday, May 29, 2010	Sheet 39 of 56	

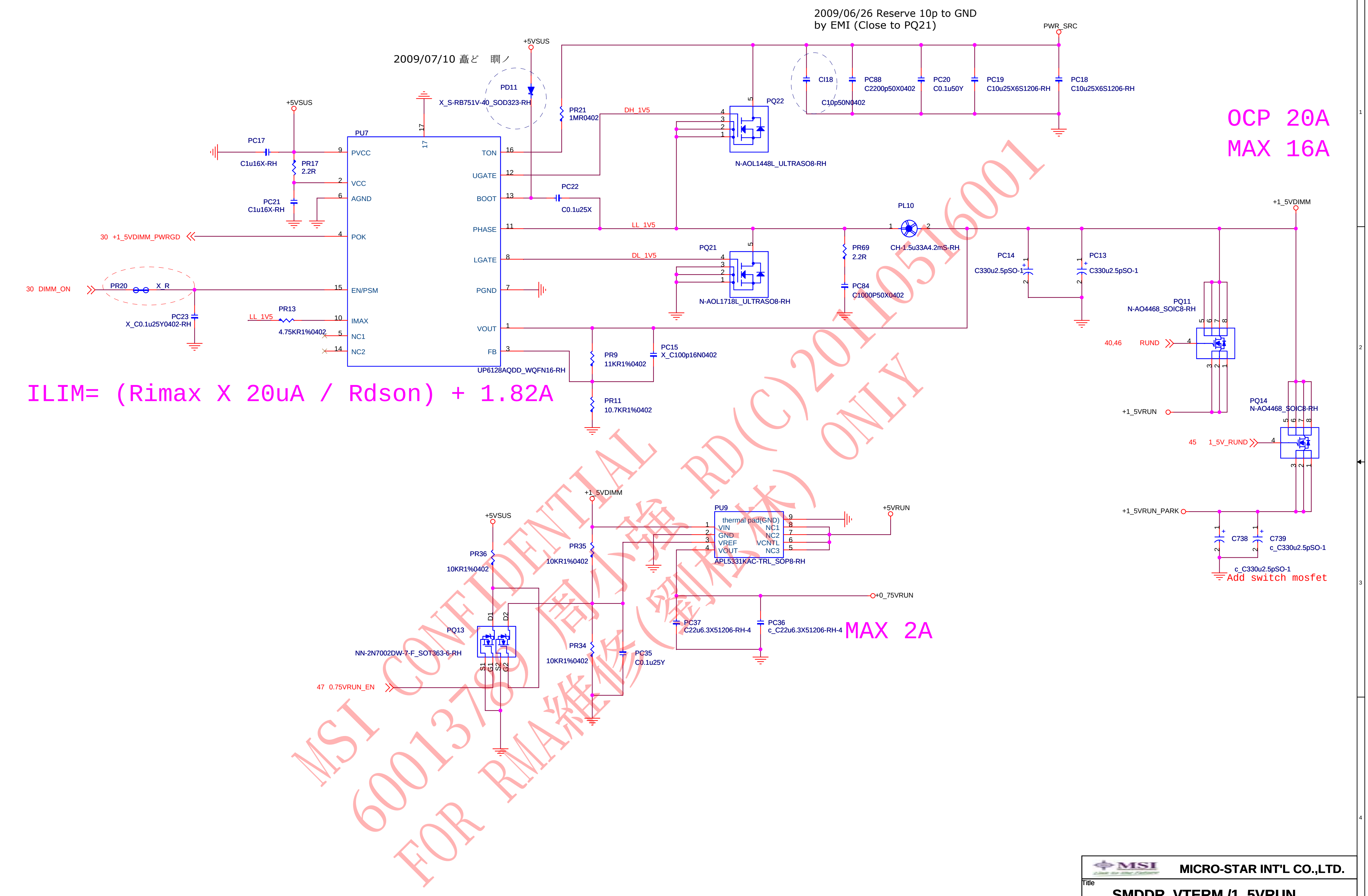


MICRO-STAR INT'L CO.,LTD.

Title: System power

Size	Document Number	Rev
Custom	MS-145X	10

Date: Saturday, May 29, 2010 — Sheet 40 of 56

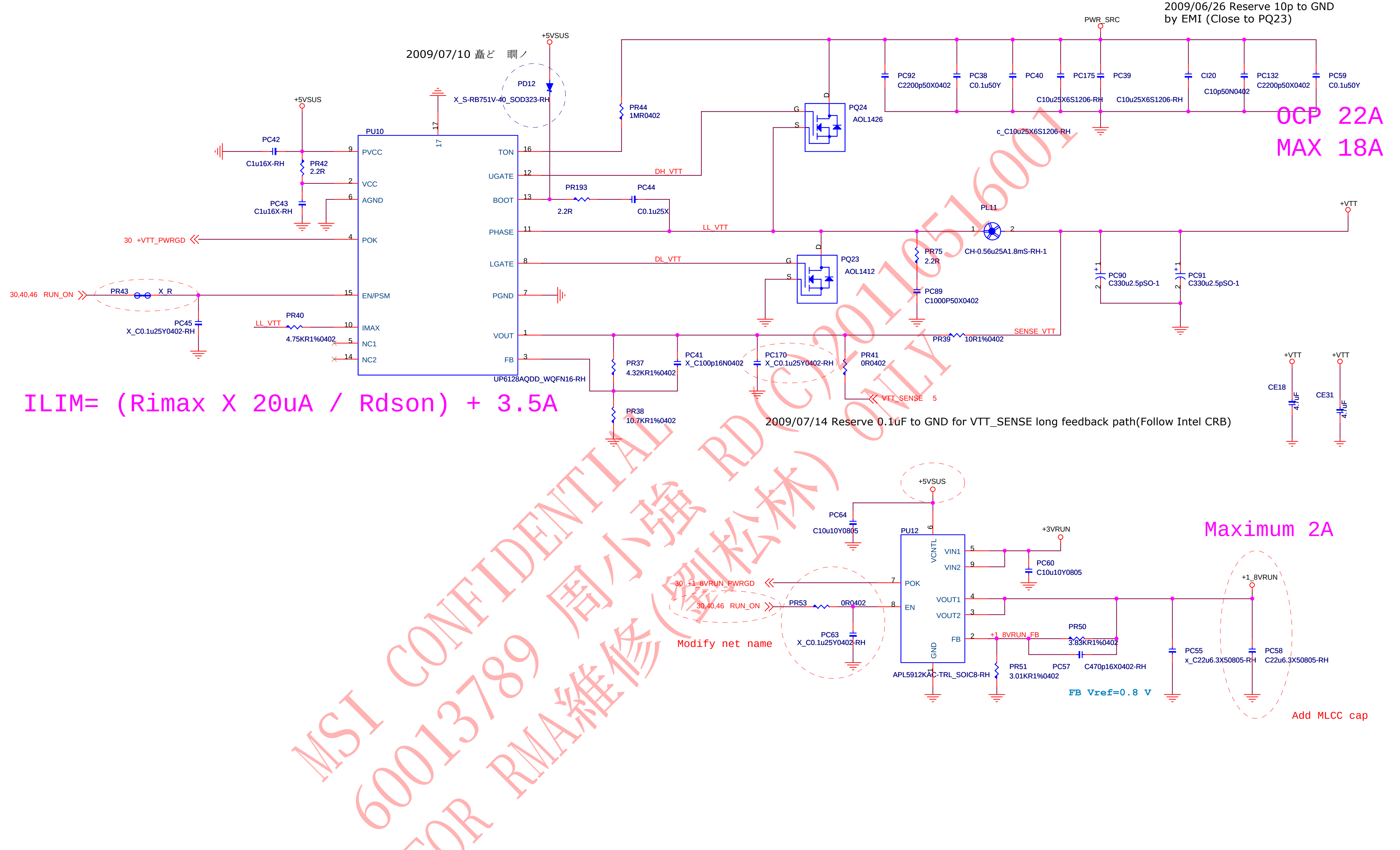


MICRO-STAR INT'L CO.,LTD.

Title: SMDDR_VTERM /1_5VRUN

Size	Document Number	Rev
Custom	MS-145X	10

Date: Saturday, May 29, 2010 Sheet 41 of 56

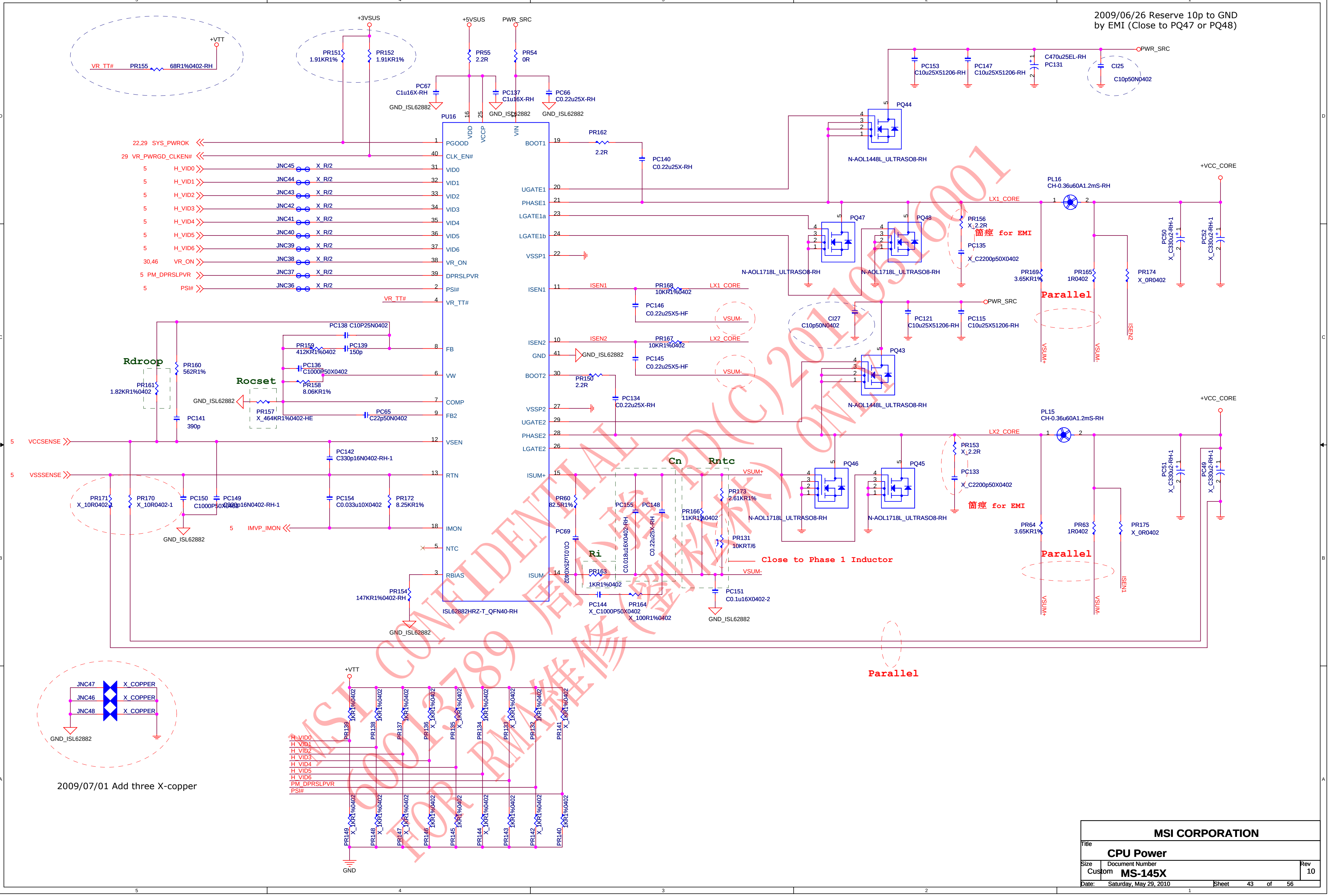


MICRO-STAR INT'L CO.,LTD.

Title: VTT Power,+1.8VRUN

Size	Document Number	Rev
Custom	MS-145X	10

Date: Saturday, May 29, 2010 Sheet 42 of 56


2009/06/26 Reserve 10p to GND
by EMI (Close to PQ47 or PQ48)
+VTT
VR_TT#
PR155
68R1%0402-RH
+3VSUS
PR151
1.91KR1%
PR152
1.91KR1%
+5VSUS
PR55
2.2R
PWR_SRC
PR54
0R
PC67
C1u16X-RH
PC137
C1u16X-RH
PC66
C0.22u25X-RH
GND_ISL62882
PU16
VDD
VCCP
VIN
22,29 SYS_PWROK
29 VR_PWRGD_CLKEN#
PGOOD
CLK_EN#
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
30,46 VR_ON
5 PM_DPRSLPVR
PSI#
JNC45
JNC44
JNC43
JNC42
JNC41
JNC40
JNC39
JNC38
JNC37
JNC36
X_R/2
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
PSI#
VR_TT#
BOOT1
UGATE1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
ISEN2
GND
BOOT2
VSSP2
UGATE2
PHASE2
LGATE2
ISUM+
ISUM-
FB
VW
COMP
FB2
VSEN
RTN
IMON
NTC
RBIAS
ISL62882HRZ-T_QFN40-RH
PR162
2.2R
PC140
C0.22u25X-RH
PC153
C10u25X51206-RH
PC147
C10u25X51206-RH
C470u25EL-RH
PC131
CI25
C10p50N0402
PQ44
N-AOL1448L_ULTRASO8-RH
+VCC_CORE
PL16
CH-0.36u60A1.2mS-RH
LX1_CORE
PQ47
PQ48
N-AOL1718L_ULTRASO8-RH
PR156
X_2.2R
PC135
X_C2200p50X0402
箇瘞 for EMI
PR169
3.65KR1%
PR165
1R0402
PR174
X_0R0402
PC50
X_C330u2-RH-1
PC52
X_C330u2-RH-1
Parallel
PR168
10KR1%0402
PC146
C0.22u25X5-HF
VSUM-
VSUM+
CI27
C10p50N0402
PC121
C10u25X51206-RH
PC115
C10u25X51206-RH
PQ43
N-AOL1448L_ULTRASO8-RH
PR167
10KR1%0402
LX2_CORE
PC145
C0.22u25X5-HF
PR150
2.2R
PC134
C0.22u25X-RH
PL15
CH-0.36u60A1.2mS-RH
PC138 C10P25N0402
PR159
412KR1%0402
PC139
150p
PC136
C1000P50X0402
PR158
8.06KR1%
Rdroop
PR160
562R1%
PR161
1.82KR1%0402
Rocset
PR157
X_464KR1%0402-HE
PC65
C22p50N0402
PC141
390p
5 VCCSENSE
5 VSSSENSE
PC142
C330p16N0402-RH-1
PR171
X_10R0402-1
PR170
X_10R0402-1
PC150
C1000P50X0402
PC149
C330p16N0402-RH-1
PC154
C0.033u10X0402
PR172
8.25KR1%
5 IMVP_IMON
PR154
147KR1%0402-RH
PR60
82.5R1%
PC69
C0.01u25X0402
PC155
C0.018u16X0402-RH
PC148
C0.22u25X-RH
Cn
Rntc
PR166
11KR1%0402
PR173
2.61KR1%
PR131
10KRT/6
Ri
PR163
1KR1%0402
PC144
X_C1000P50X0402
PR164
X_100R1%0402
PC151
C0.1u16X0402-2
Close to Phase 1 Inductor
PQ46
PQ45
PR153
X_2.2R
PC133
X_C2200p50X0402
PR64
3.65KR1%
PR63
1R0402
PR175
X_0R0402
PC51
X_C330u2-RH-1
PC49
X_C330u2-RH-1
ISEN1
ISEN2
JNC47
JNC46
JNC48
X_COPPER
2009/07/01 Add three X-copper
PR139
PR138
PR137
PR136
PR135
PR134
PR133
PR132
PR141
1KR1%0402
X_1KR1%0402
PR149
PR148
PR147
PR146
PR145
PR144
PR143
PR142
PR140
PM_DPRSLPVR
GND
MSI CORPORATION
Title
CPU Power
Size
Custom
Document Number
MS-145X
Rev
10
Date: Saturday, May 29, 2010
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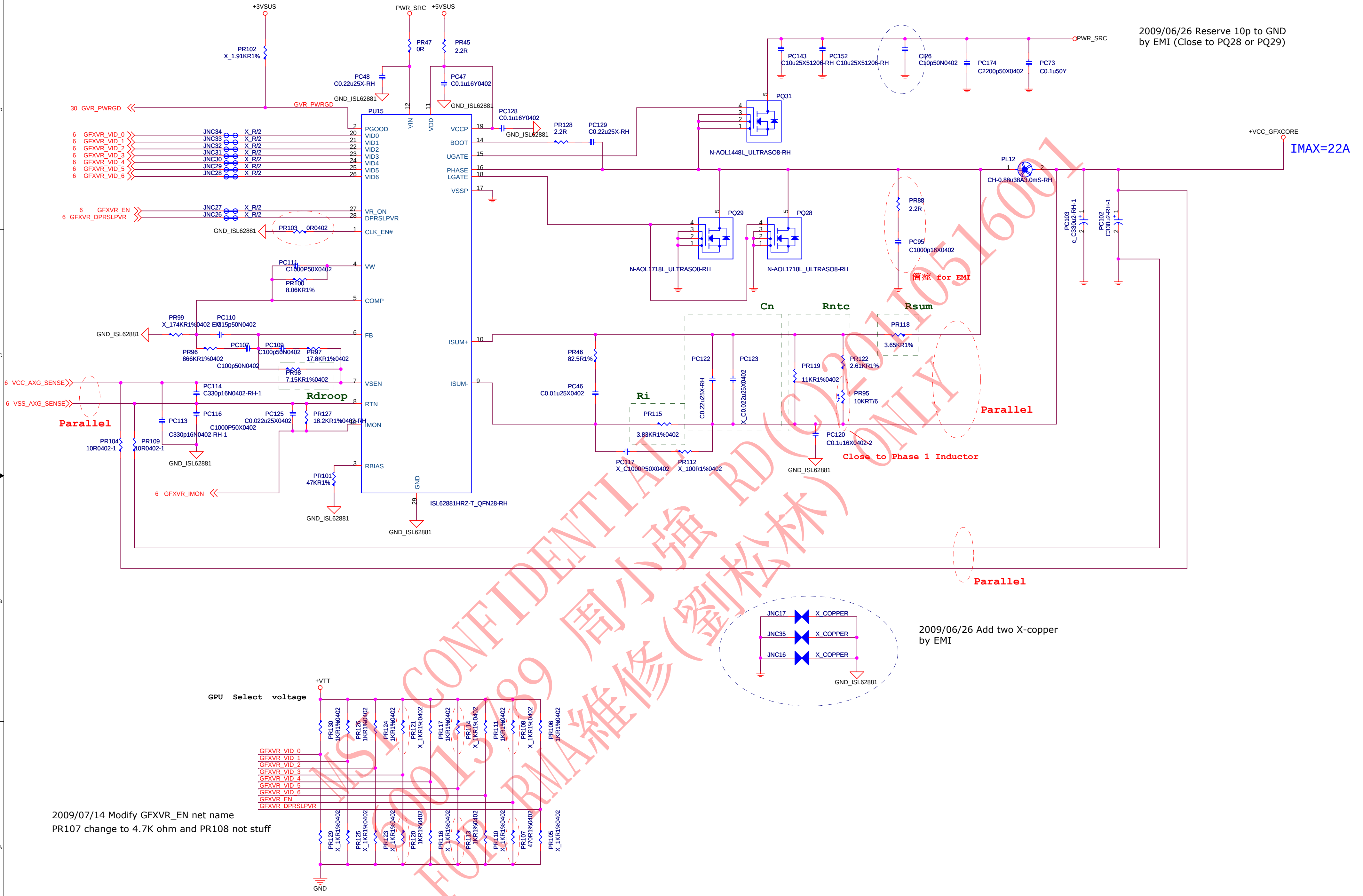
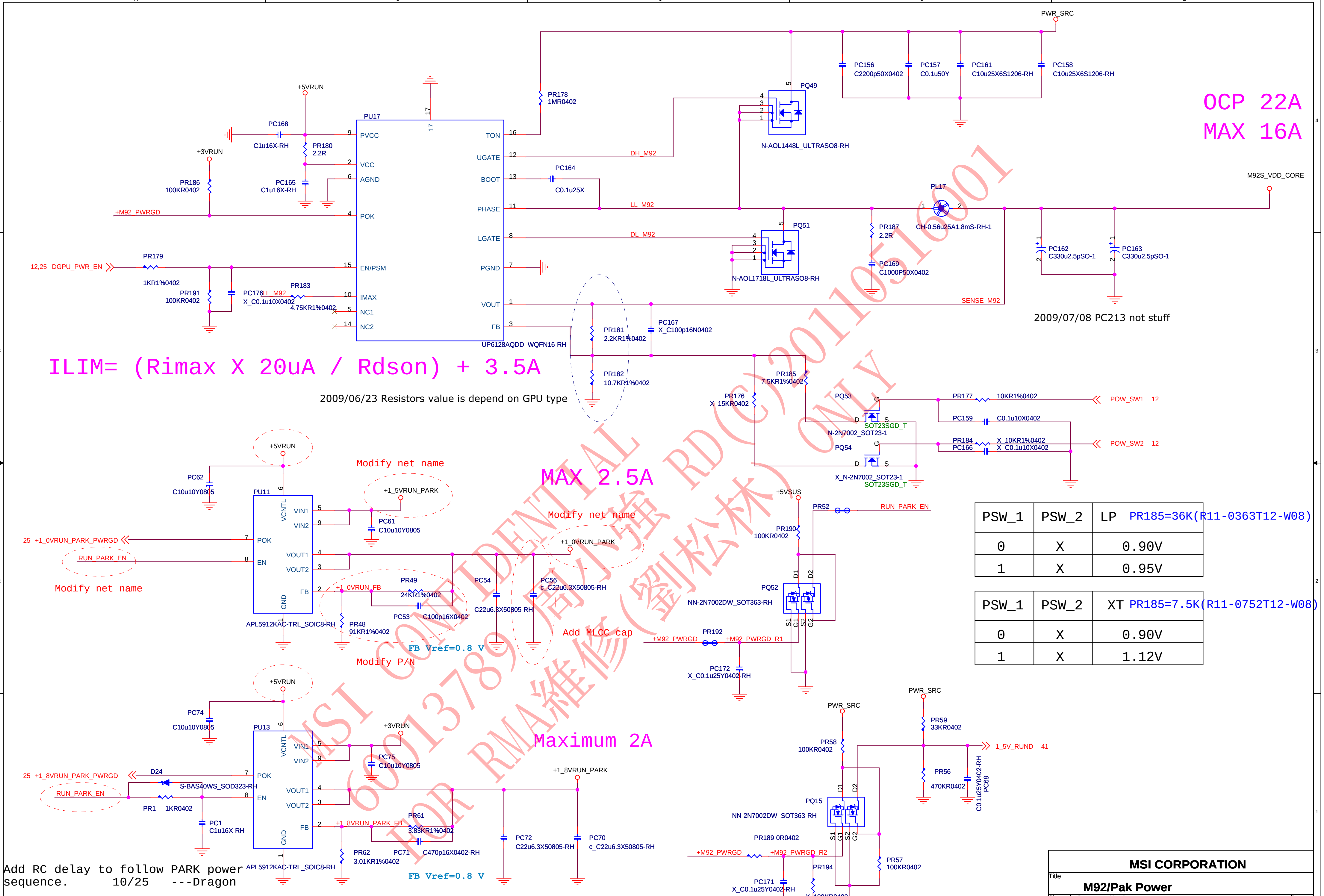


MSI CORPORATION

Title	Graphic Core	
Size: Custom	Document Number: MS-145X	Rev: 10
Date: Saturday, May 29, 2010	Sheet 44 of 56	



Add RC delay to follow PARK power sequence. 10/25 ---Dragon

PSW_1	PSW_2	LP PR185=36K(R11-0363T12-W08)
0	X	0.90V
1	X	0.95V

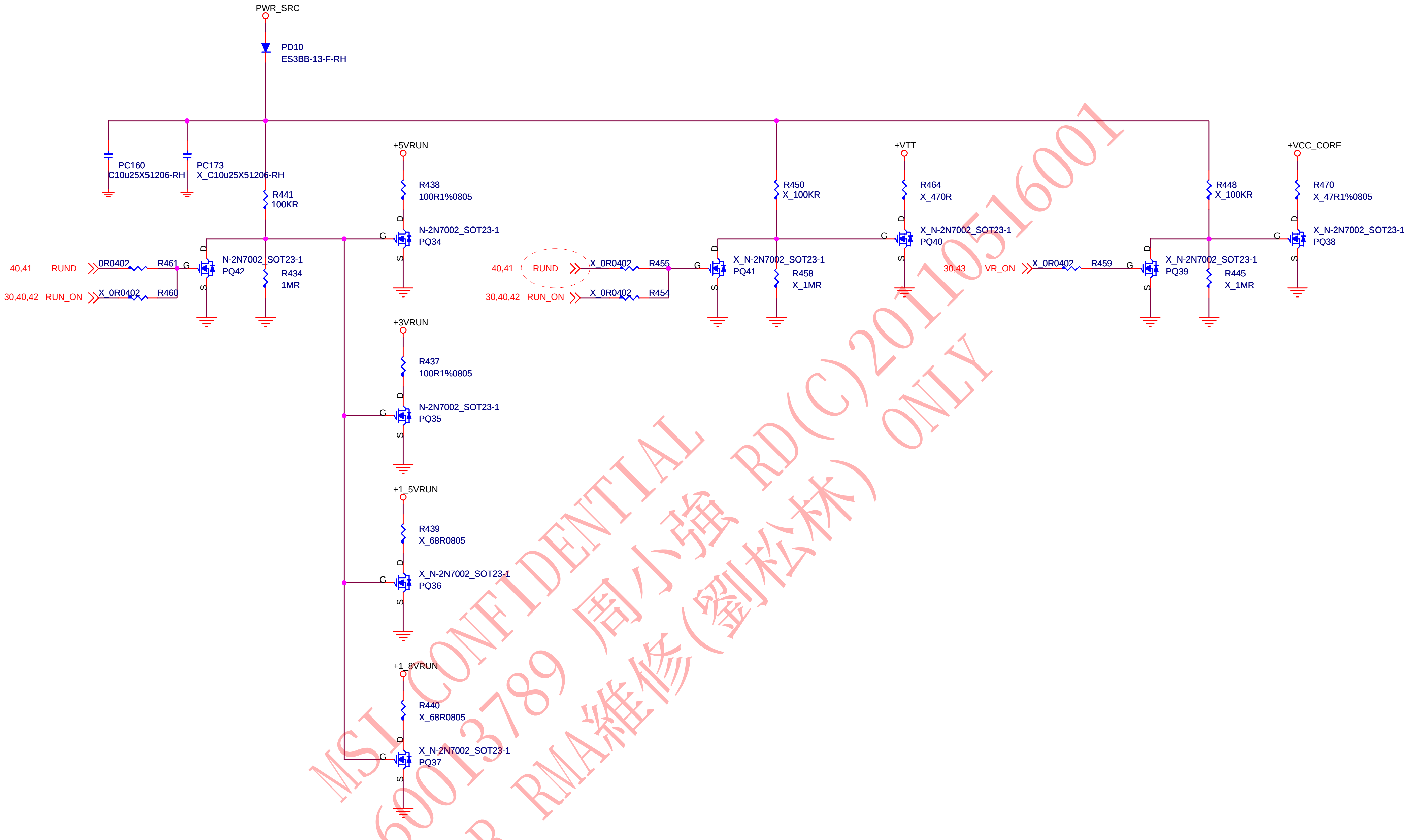
PSW_1	PSW_2	XT PR185=7.5K(R11-0752T12-W08)
0	X	0.90V
1	X	1.12V

MSI CORPORATION

Title: M92/Pak Power

Size: Custom | Document Number: MS-145X | Rev: 10

Date: Saturday, May 29, 2010 |



MICRO-STAR INT'L CO.,LTD.

Title

Discharge Circuits

Size	Document Number	Rev
Custom	MS-145X	10

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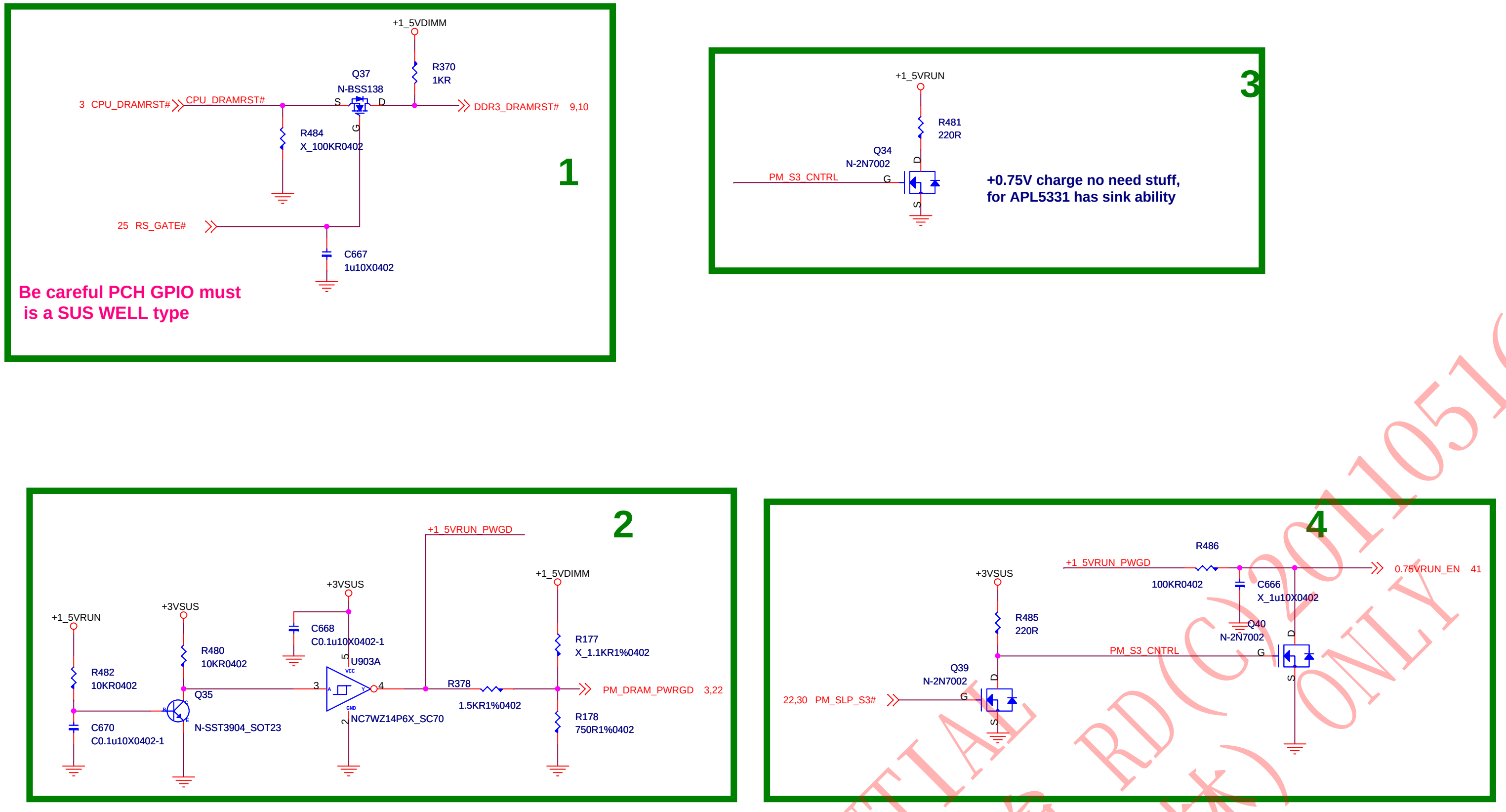

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	INTEL S3 POWER	
Size Custom	Document Number MS-145X	Rev 10
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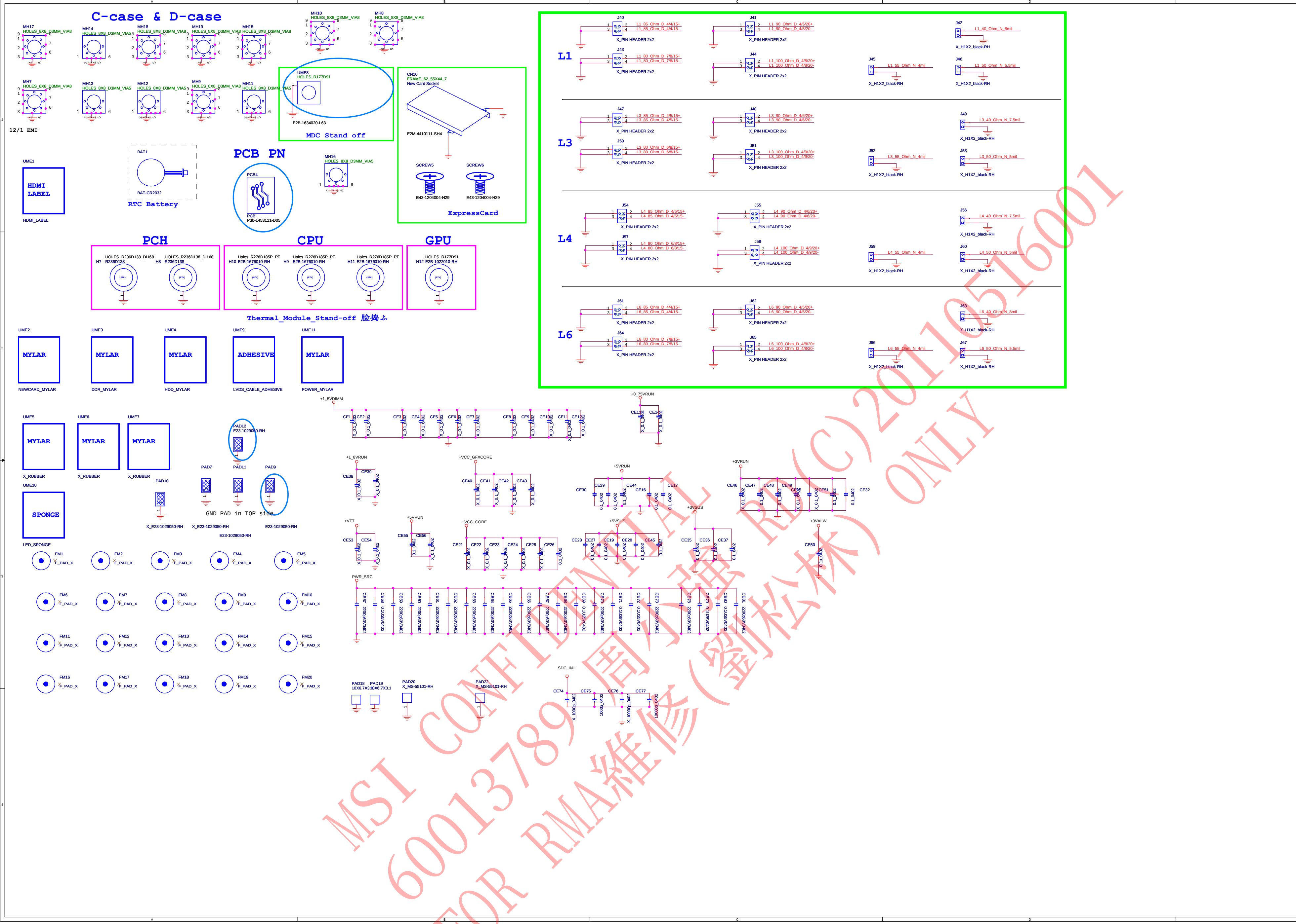

MICRO-STAR INT'L CO.,LTD.

Title: Screw/EMI

Size: D | Document Number: MS-145X | Rev: 10

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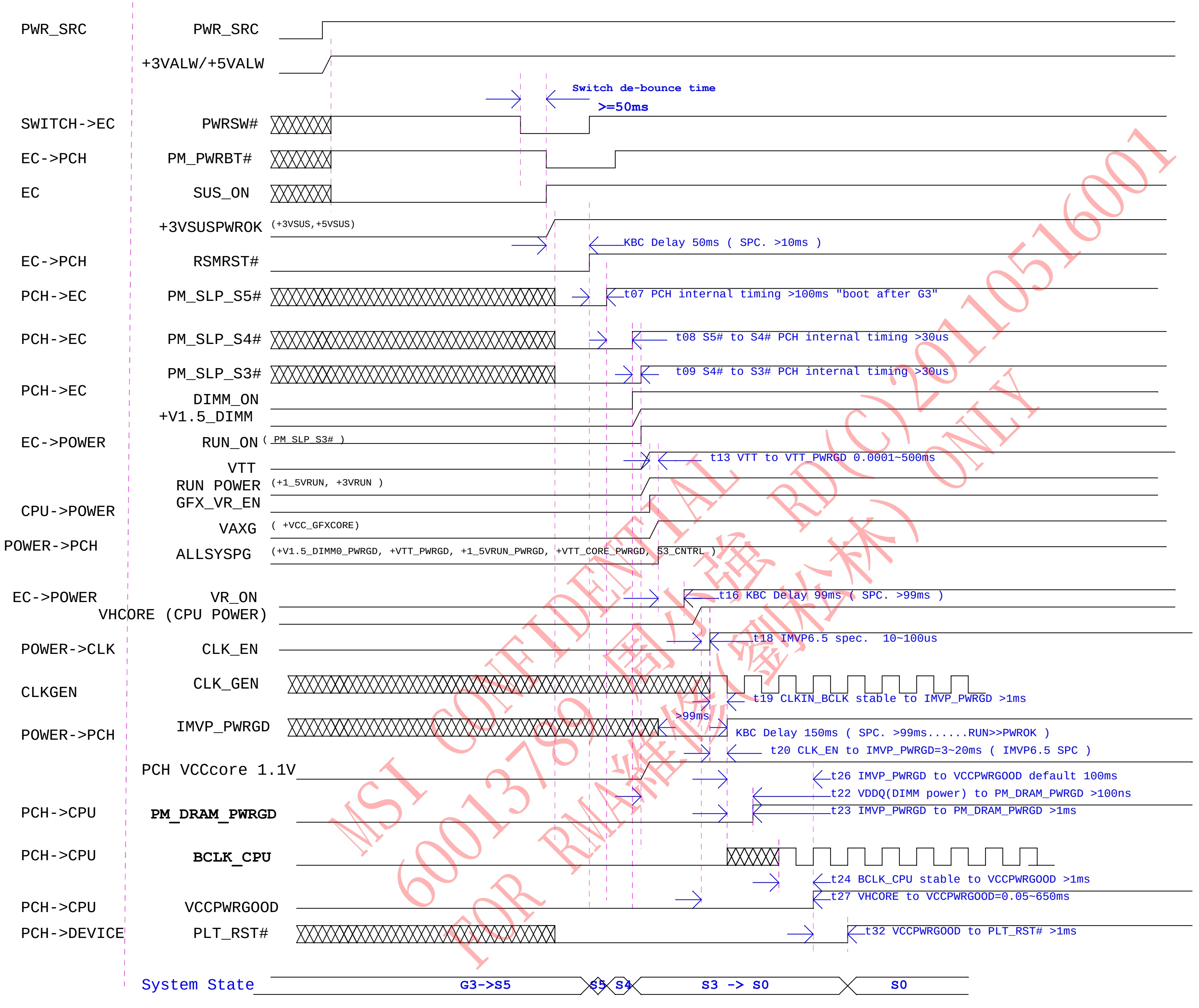
Calpella System Power on Sequence DC mode



MSI

MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequency

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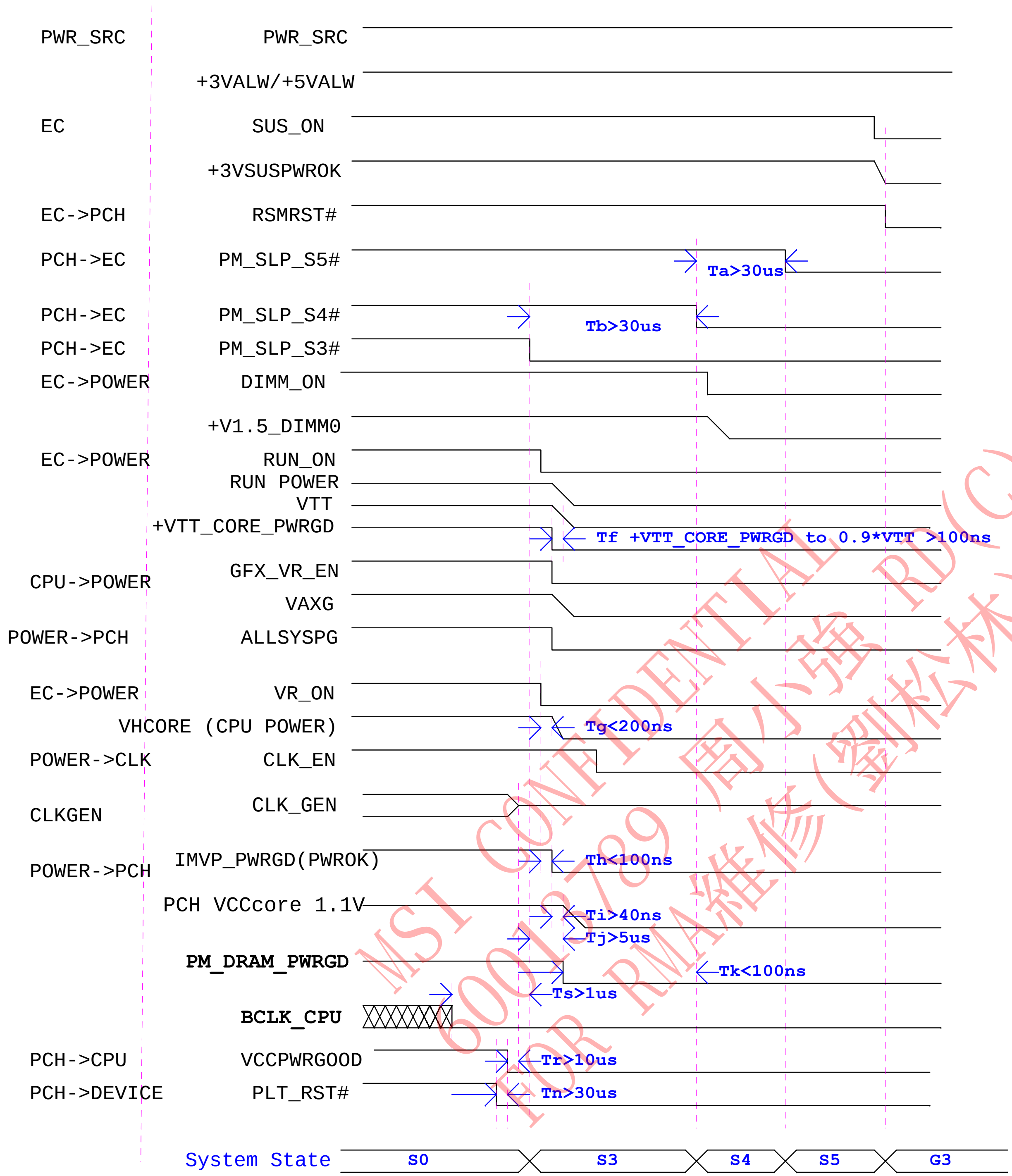
Power down Sequence DC mode S0 to G3



MSI	MICRO-STAR INT'L CO.,LTD.
Title	Power on Sequency
Size: A3	Document Number: MS-145X	Rev: 10
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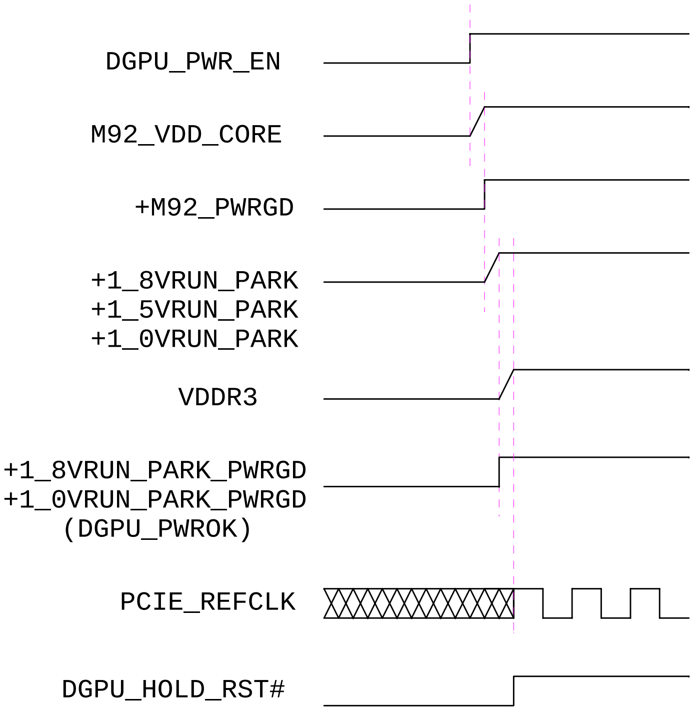
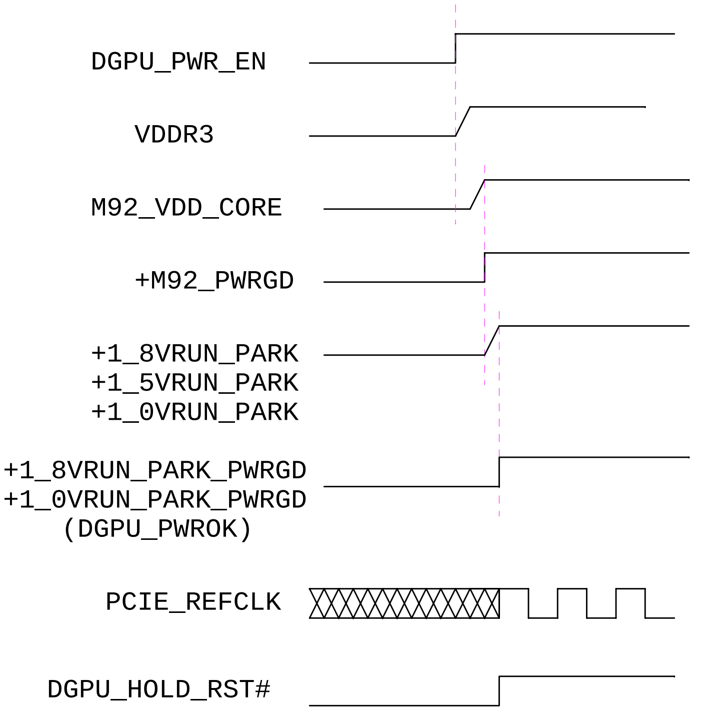
M92 Power on Sequence



PARK Power on Sequence



MICRO-STAR INT'L CO.,LTD.

Title: M92/PARK Power on Sequence

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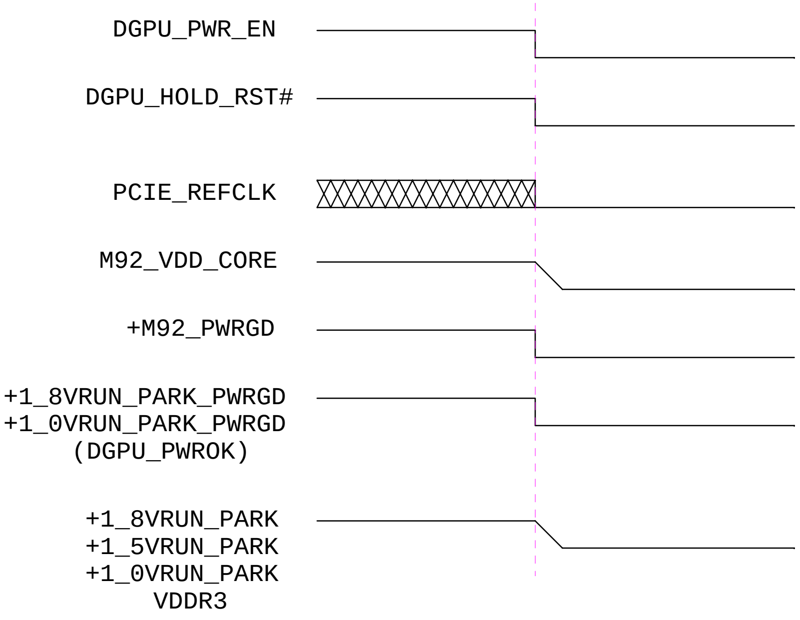
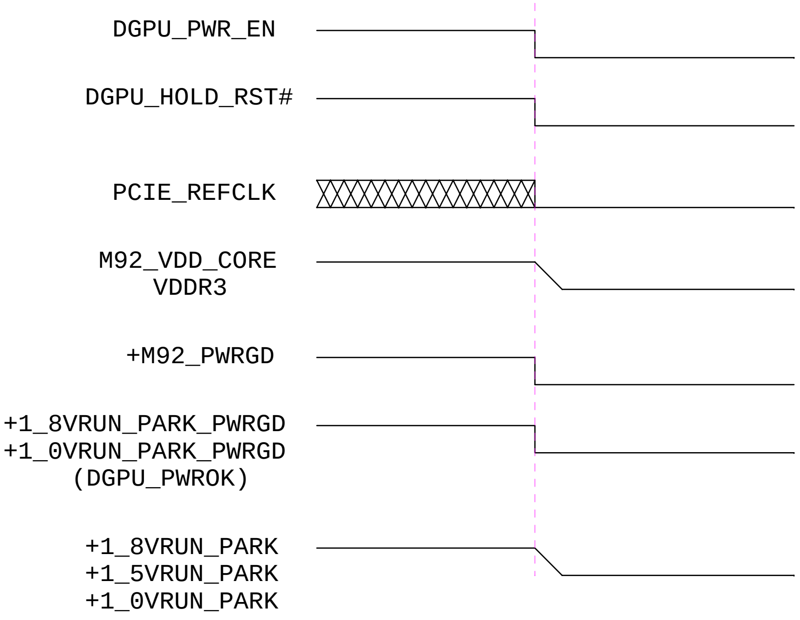
M92 Power down Sequence



PARK Power down Sequence



MICRO-STAR INT'L CO.,LTD.

Title	M92/PARK Power down Sequence
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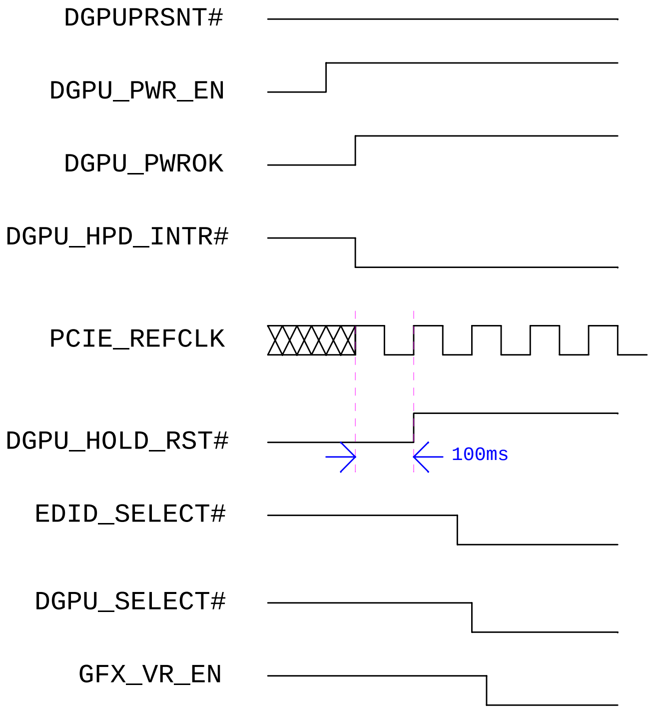
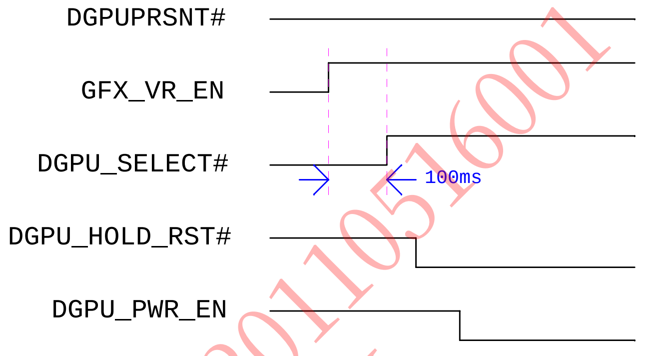
Switchable DGPU Power on Sequence
Discrete Mode



Switchable DGPU Power off Sequence
UMA Mode



MICRO-STAR INT'L CO.,LTD.		
Title: Switchable Power Sequence		
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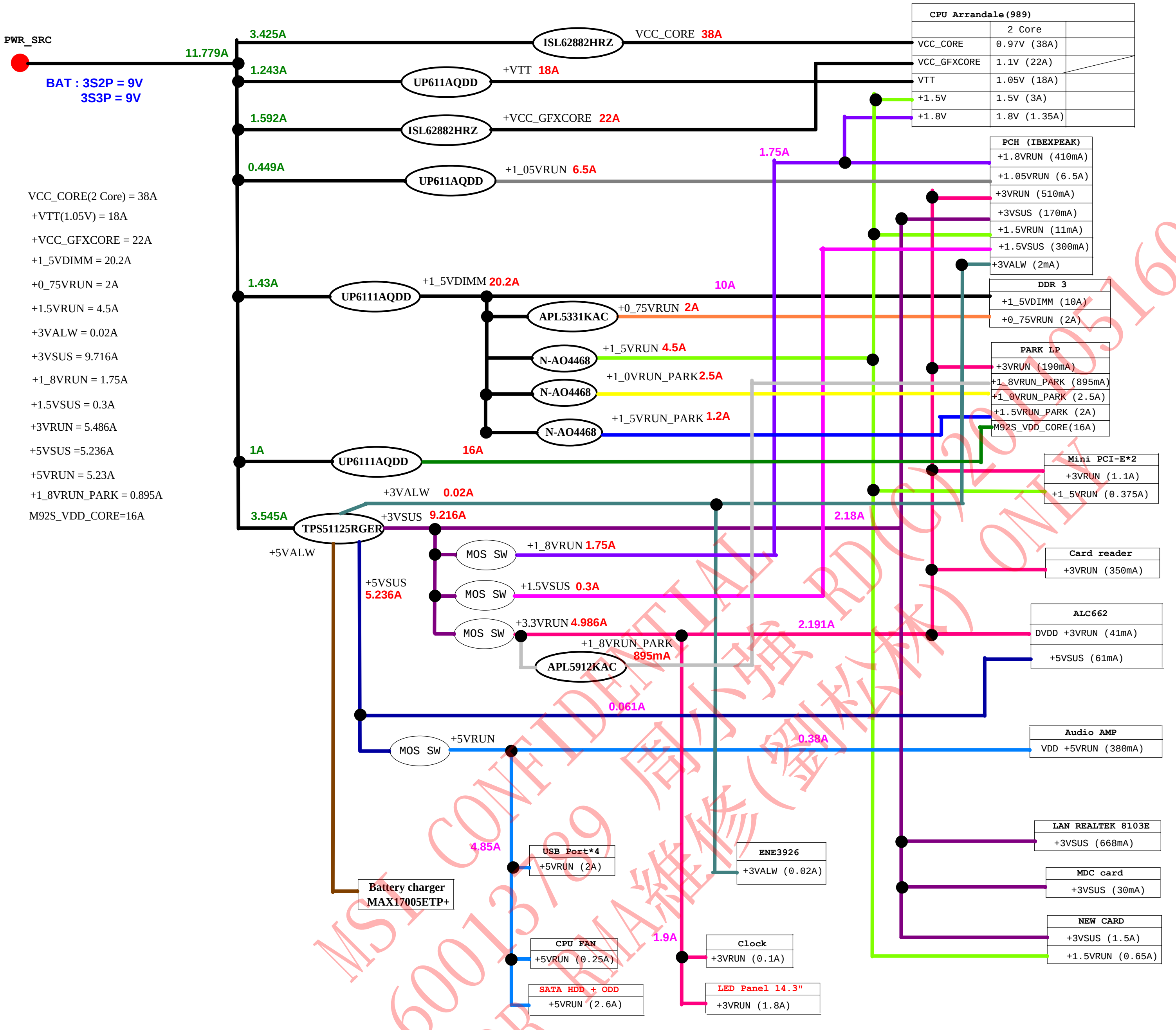

MSI	MICRO-STAR INT'L CO.,LTD.
Title	Power MAP
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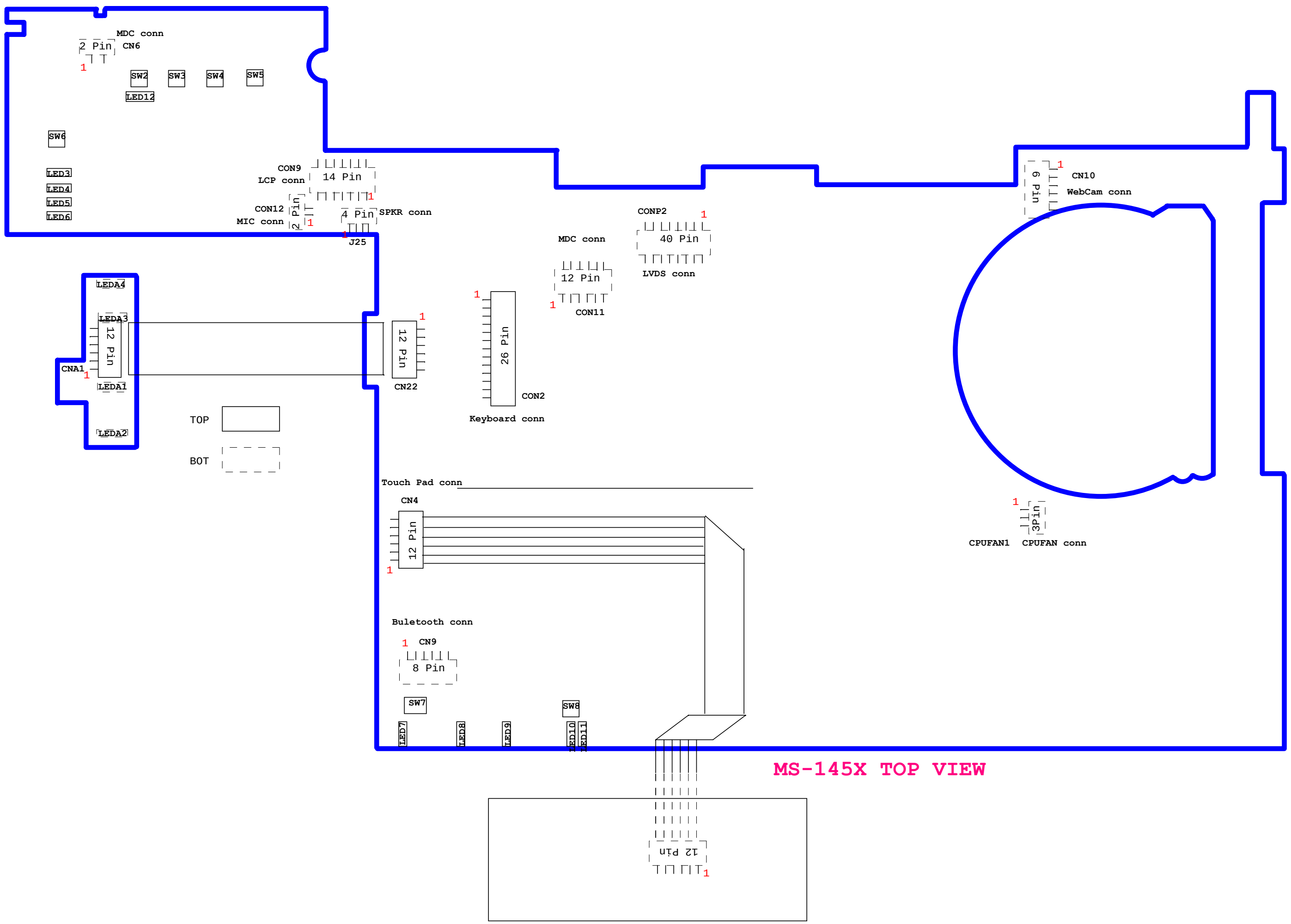
MS-145X	
SW2	Power_button(FOR OEM)
SW3	HotKeyP1_button(FOR OEM)
SW4	WLAN/BT_button(FOR OEM)
SW5	Search/Webcam_button (FOR OEM)
SW6	Power_button(FOR Channel)
SW7	Right_button
SW8	Left_button

MS-145X	
LED3	HDD LED(FOR OEM)
LED4	NUM_LED(FOR OEM)
LED5	CAP_LED(FOR OEM)
LED6	SCR_LED (FOR OEM)
LED7	BT_LED
LED8	WLAN_LED
LED9	ACPI_LED
LED10	CHARGE_LED
LED11	BATTERY_LOW_LED
LED12	POWER_LED

MS-145XA	
LEDA1	NUM_LED(FOR OEM)
LEDA2	HDD_LED(FOR OEM)
LEDA3	CAP_LED(FOR OEM)
LEDA4	SCR_LED (FOR OEM)



MS-145X TOP VIEW

MS-145X : Main Board
MS-145XA : LED board

MICRO-STAR INT'L CO.,LTD.		
Title: Topology		
Size: Custom	Document Number: MS-145X	Rev: 10
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2009/06/25 [Page33] Add LED and switch function for OEM reserved
[Page30] Delete KBOUT16,KBOUT17 for MS-1451 keyboard matrix
[Page41/42] Modify APL5912 VCNTL to +5VSUS
[Page43/44] Modify some RC footprint and value

2009/06/26 Modify circuit to Switchable
[Page19] Add LVDS common choke by EMI
[Page12] Reserve RGB 10p to GND
[Page38] Reserve BAT CLK and DATA 10p to GND
[Page39] Reserve 10p SDC_IN+ to GND and close to PQ57
Add two X-Copper
[Page40] Reserve 10p +5VSUS to GND and close to PQ60
Reserve 2.2R+2200p
[Page41] Reserve 10p PWR_SRC to GND and close to PQ68
[Page42] Reserve 10p PWR_SRC to GND and close to PQ72
[Page43] Reserve 10p PWR_SRC to GND and close to PQ75 or PQ76
Reserve 10p PWR_SRC to GND and close to PQ78 or PQ79
[Page43] Reserve 10p PWR_SRC to GND and close to PQ81 or PQ82
Add two X-Copper

2009/06/29 [Page35] Modify CPU FAN.Add C121 and C304 by datasheet.Add one more RC for FAN speed calculation(as MS-1122)
Modify PARK circuit
Modify PCH PN to OB1-1675001 for Mobile IntelR 5 Series Chipset Full Feature
Modify Audio jack PN to N54-05F0951-H06
Modify internal MIC PN to N32-1020790-A81
Modify power sequence map

2009/07/01 [Page3] R234,R412单0A龟喷挡猢 /﹚珱 簿埃
BPM#[0~7] remove
BCLK 獬瘗from PCH,簿埃from CLOCK GEN.

[Page5] Short bead

[Page6] Short bead

[Page7] VSS_NCTF1~7 remove

[Page8] 獬瘗CFG 代獯,尢緇簿埃

[Page9] SA0_DIM0のSA1_DIM0ɜ 0 ohm癸

簿埃330uF, CPU のswitching power狠 T

[Page10] SA0_DIM1ɜ 0 ohm癸

簿埃330uF, CPU のswitching power狠 T

[Page12] 干 HPD絬隔

[Page16] MDA0~MDA7 swap

[Page18] CRTのLVDS 箇瘗篆 (for MS-1454)Aɜ 虫聋 0 ohm

EDID switch 篆方pin 0.1uF

R3238,R3239ɜ 10K ohm

簿埃BR-AD-ADJ,BR-PWM-ADJ 嘿ɜ PWM-ADJ,HDMI DDC 嘿ɜ HDM_SDAのHDM_SCL

[Page19] 聄猧LC ɜ 0.1uH+10pF

稷糤LVDS DDC pull high,backlight adj箇瘗net PWM-ADJ

[Page25] DGPUPRSNT#ɜ铡pull down

[Page30] ɜ+1_8VRUN_PARK_PWRGDの+1_0VRUN_PARK_PWRGD挡 DGPU_PWROK

[Page34] C47,C49ɜ 0.1uF

[Page43] Add three X-copper

10 VER

[Page21] Add GPU leakage circuit

[Page12] Reserve TEST_EN / JTAG_TMS pull high R for AMD recommend
Reserve GPIO26_TCK circuit for AMD recommend
Reserve JTAG_TRSTB pull low R for AMD recommend

[Page18] Change D23 P/N to D01-BAS4000-W01
for HDMI fail

[Page36] Change F9 P/N to D08-0100110-P16
for USB HDD shut down issue

[Page36] Change C351 P/N to C98-1011650-P01
for USB HDD shut down issue

[Page31] Stuff R134 for internal speaker POP noise.

[Page45] Add RC delay to follow PARK power sequence.

[Page12] GPIO26_TCK pull down through 10k R229.