MS-1453(Switchable) & MS-1454(UMA) Ver : 0A

2009/07/07

Calpella Platform

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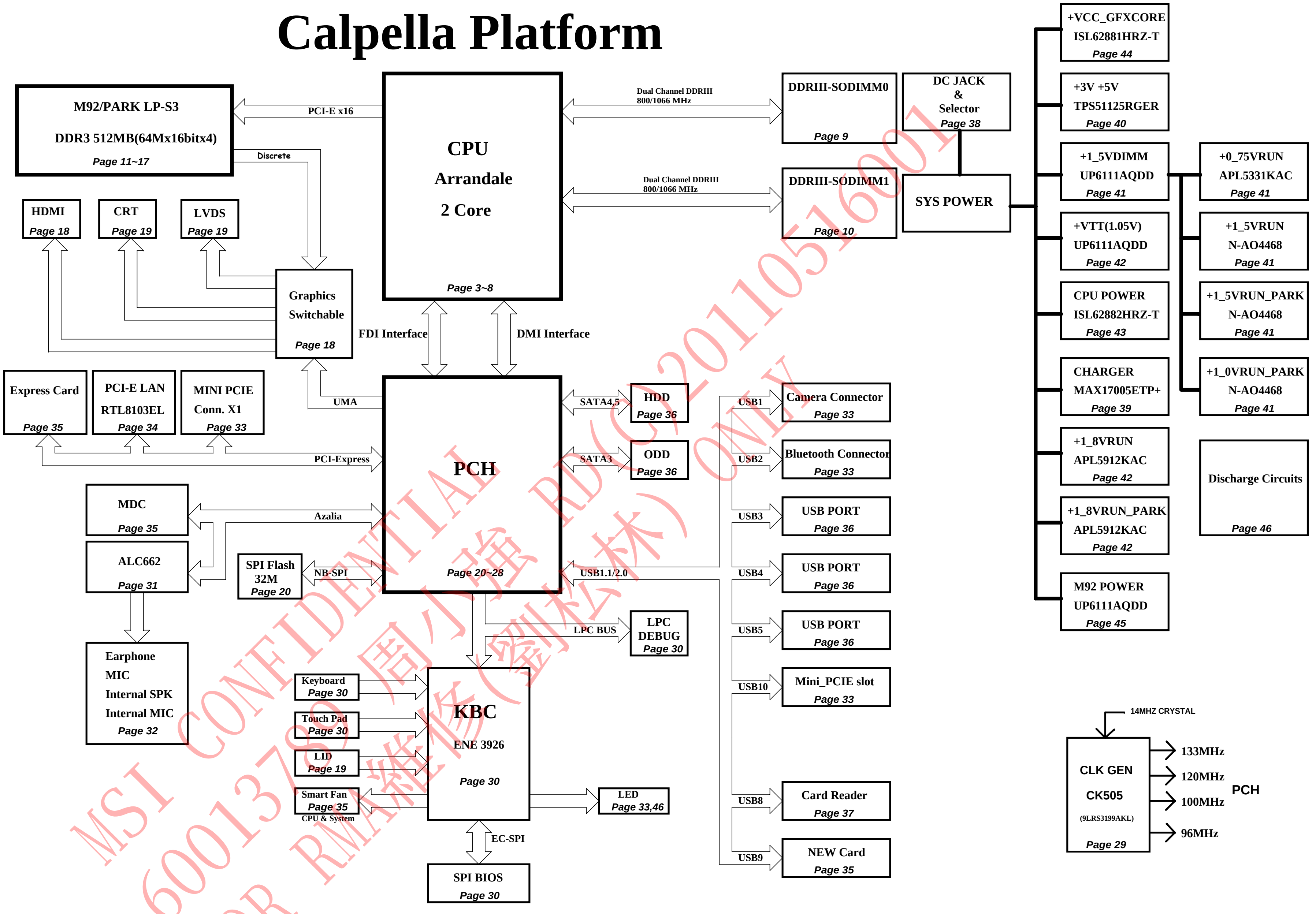
Page Description



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0,S3	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
		S0	
M92S_VDD_CORE	0.95V	S0	GPU core power
+1_8VRUN_PARK	1.8V	S0	GPU PCIE power
+1_5VRUN_PARK	1.5V	S0	GPU DDR3 power
+1_0VRUN_PARK	1.0V	S0	GPU PCIE power
VDDR3	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

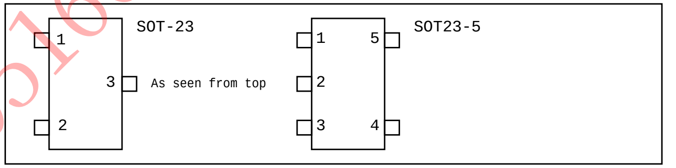
Suffix

= Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



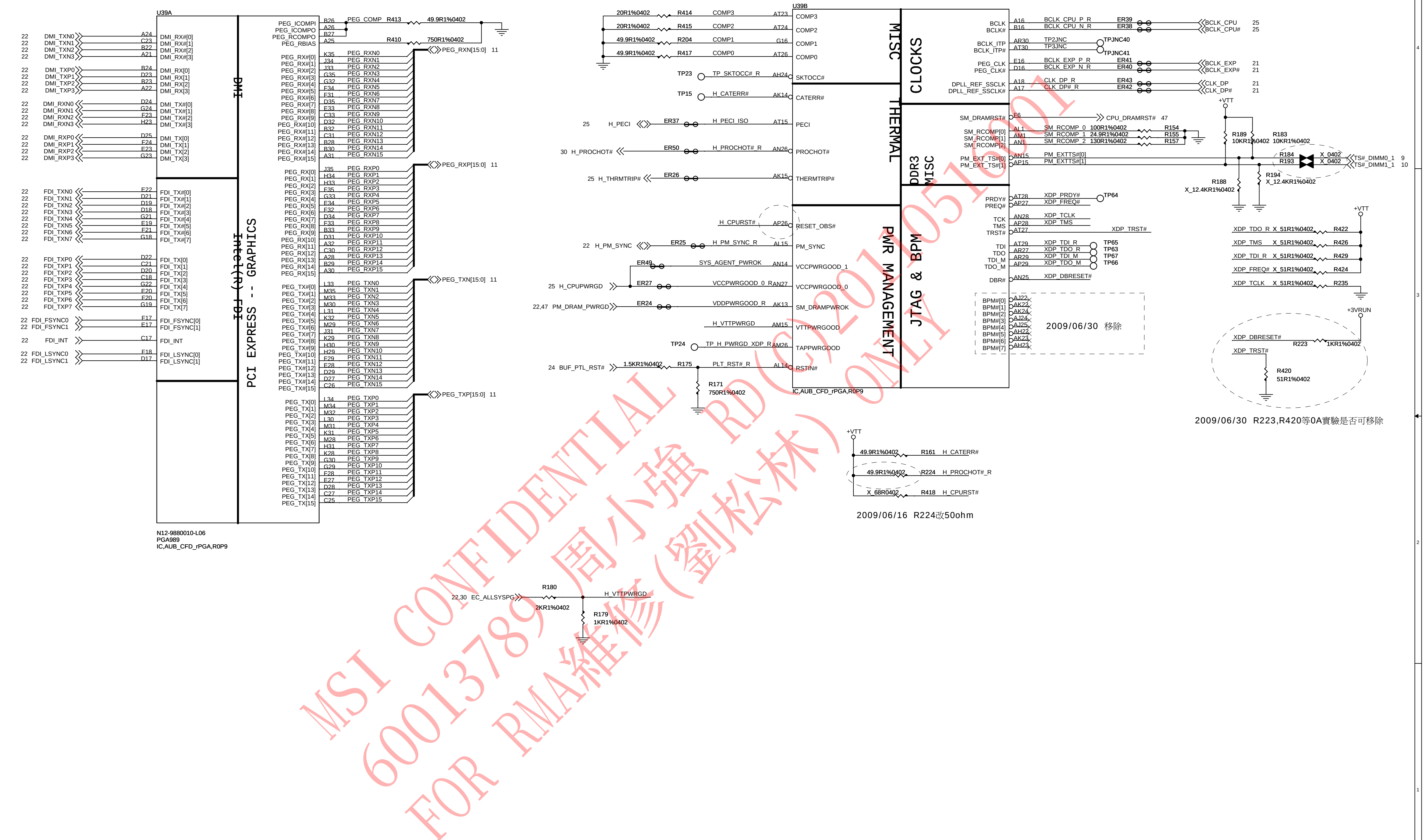
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR

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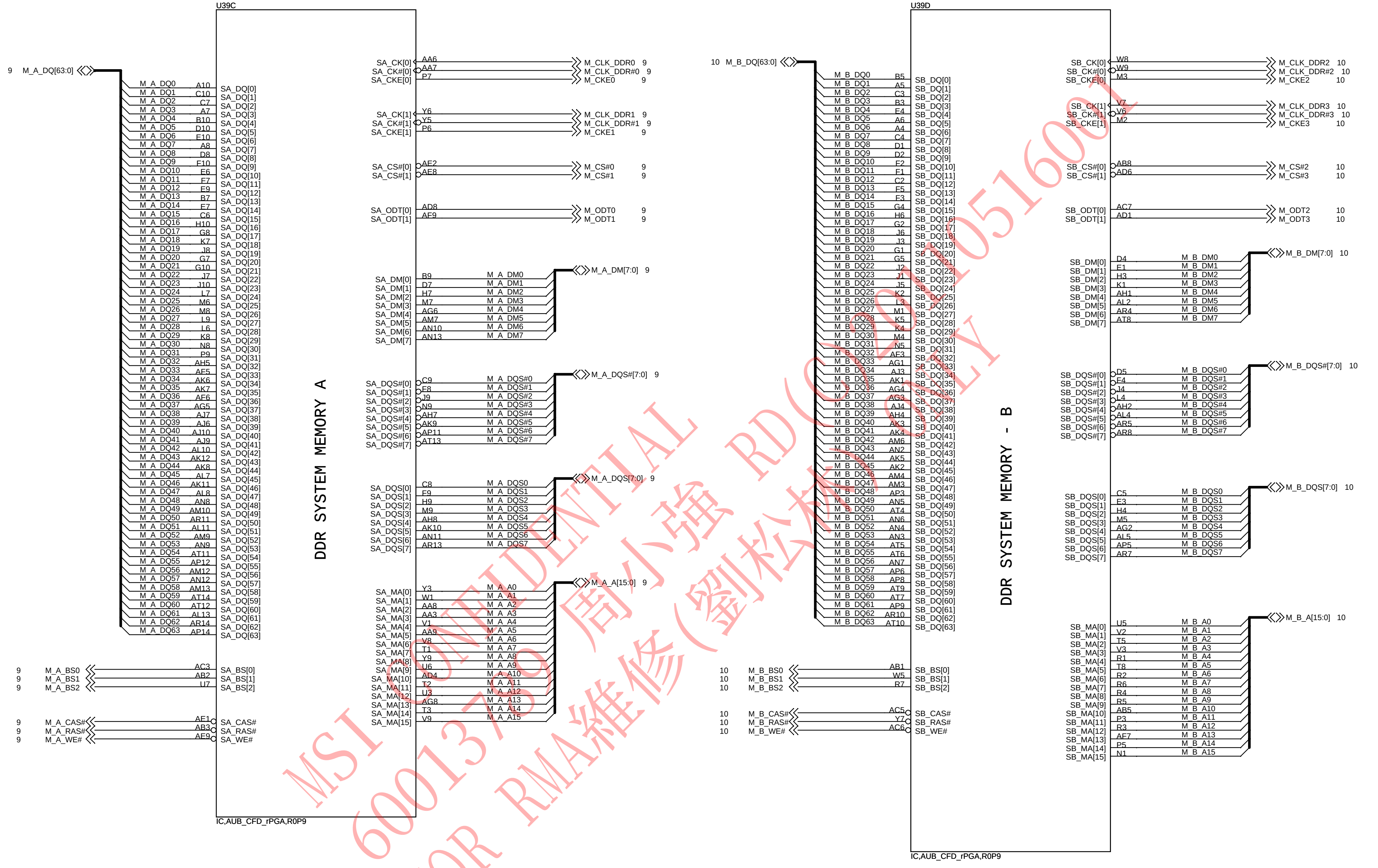
ARRANDALE PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.

Title	DDR3	
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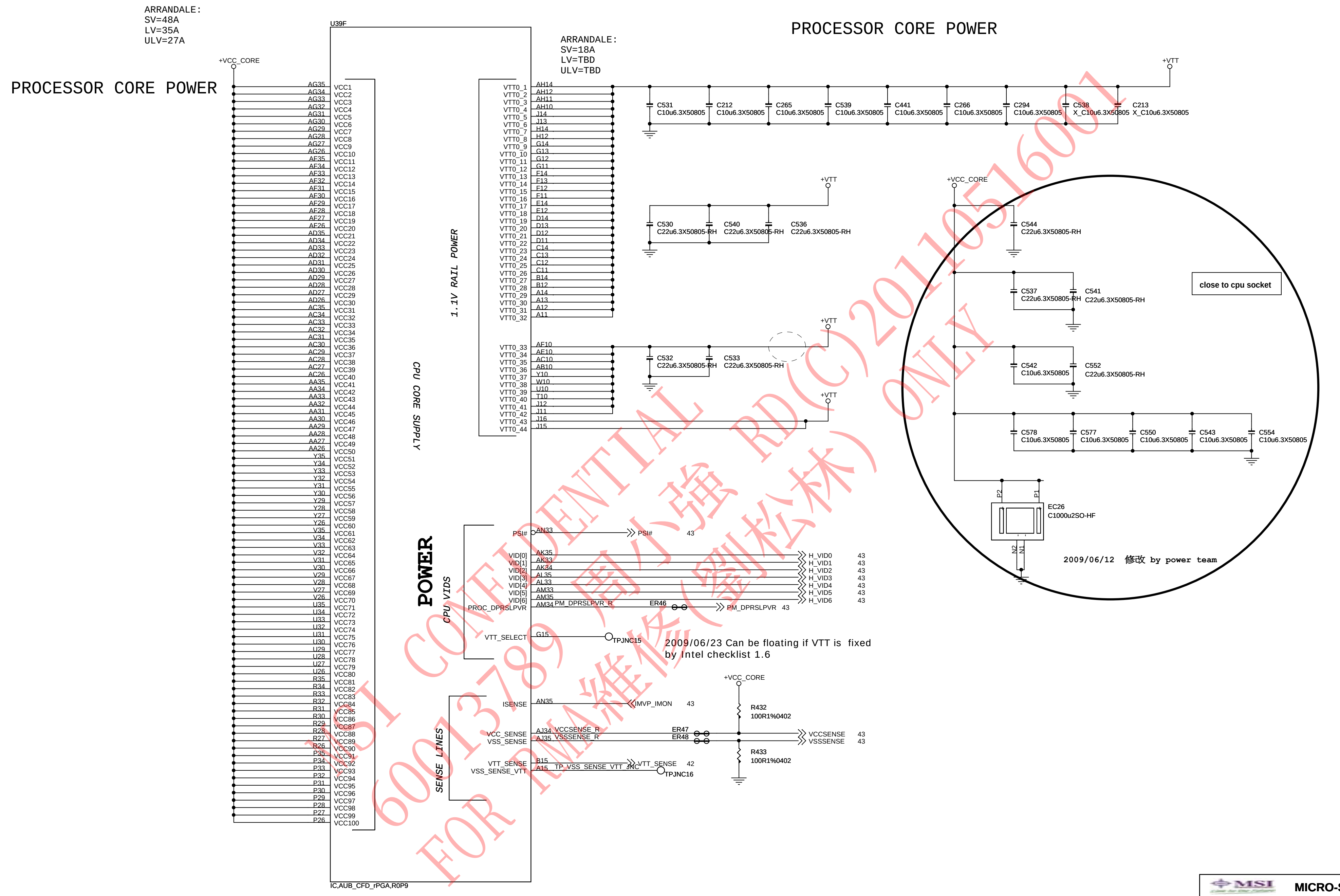
ARRANDALE PROCESSOR (POWER)



MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR POWER

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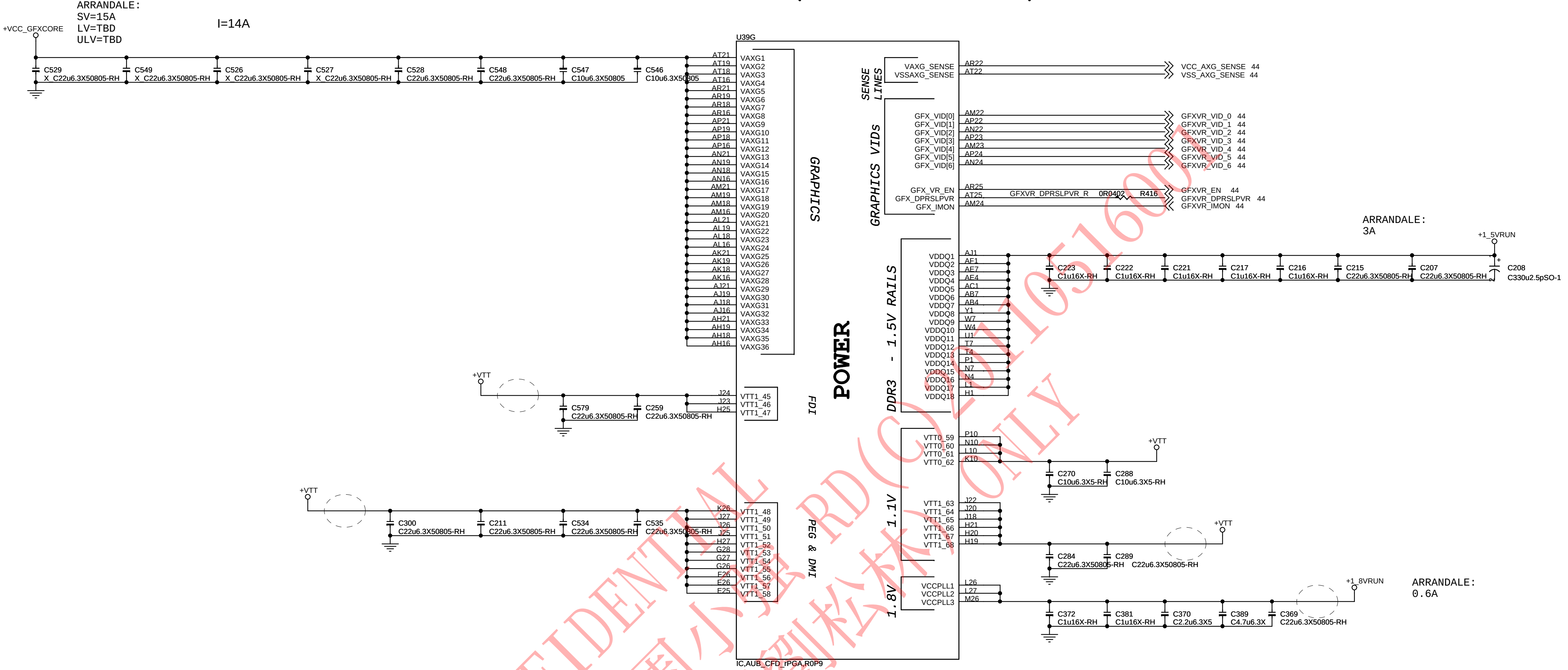
ARRANDALE PROCESSOR (GRAPHICS POWER)



MICRO-STAR INT'L CO.,LTD.

Title: GRAPHICS POWER

Size	Document Number	Rev
Custom	MS-145X	0A

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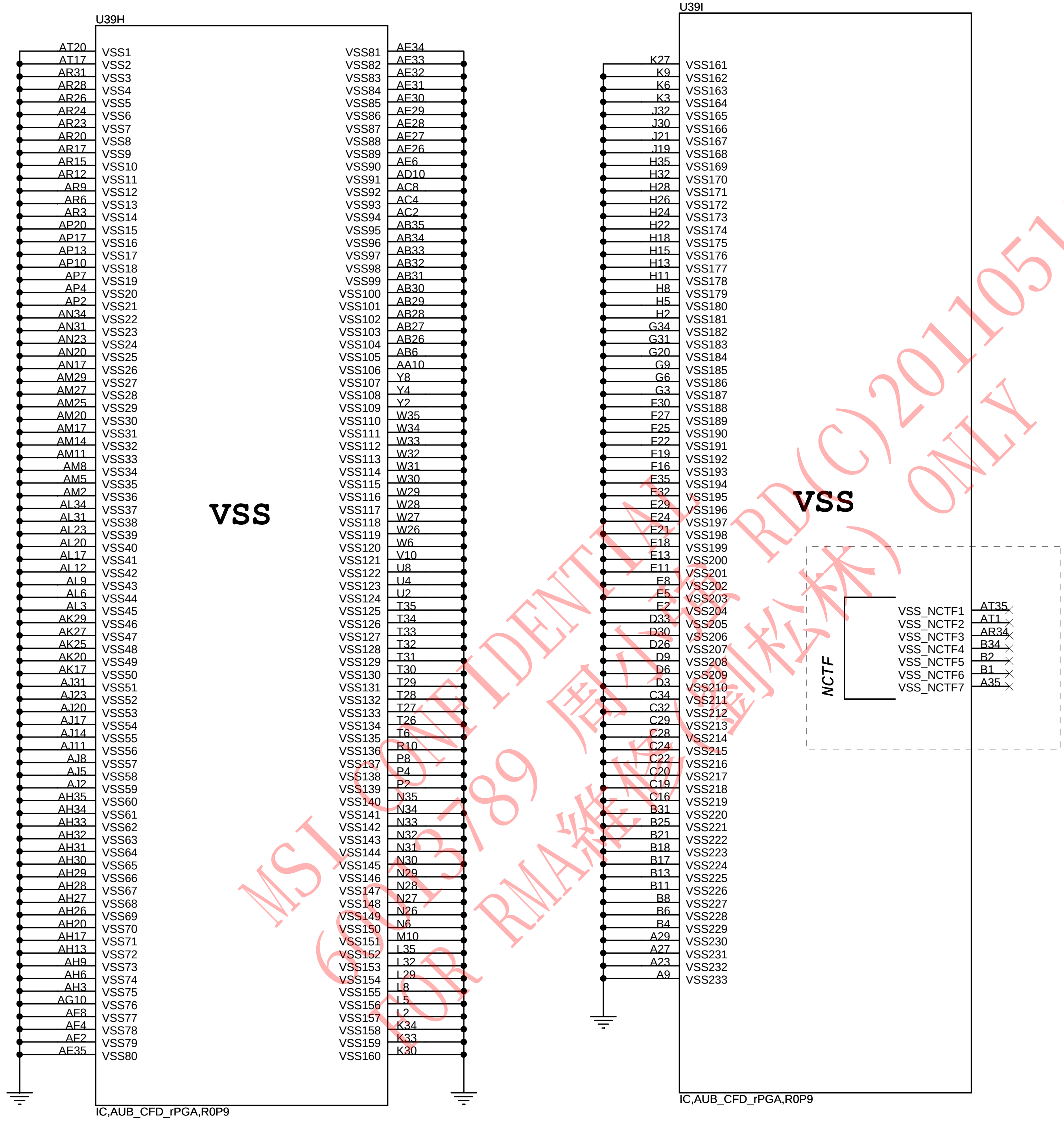
ARRANDALE PROCESSOR (GND)



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Title	PROCESSOR GND	
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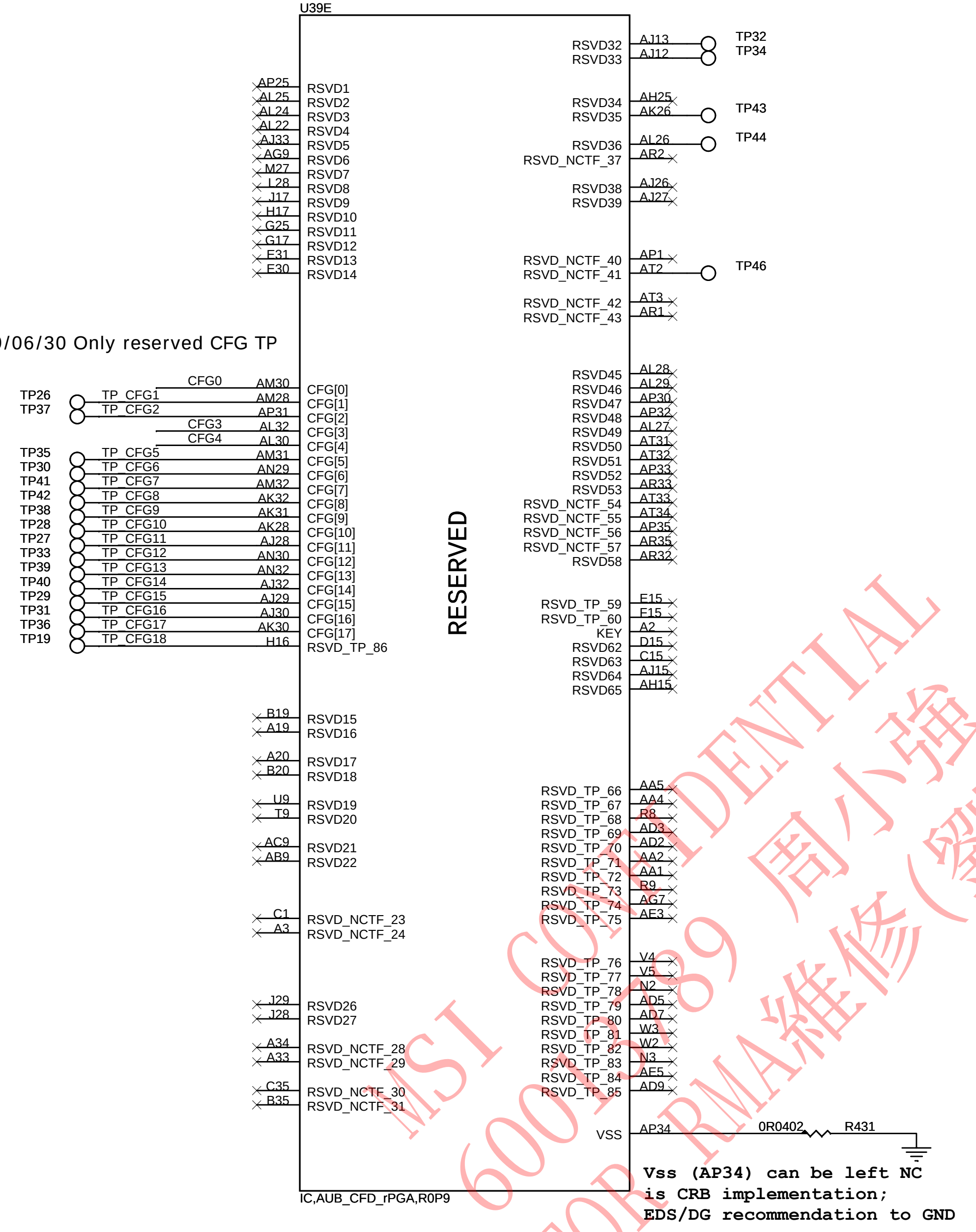
ARRANDALE PROCESSOR (RESERVED)

2009/06/30 Only reserved CFG TP

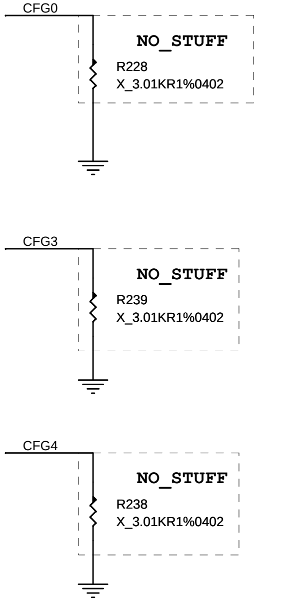


Vss (AP34) can be left NC
is CRB implementation;
EDS/DG recommendation to GND

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

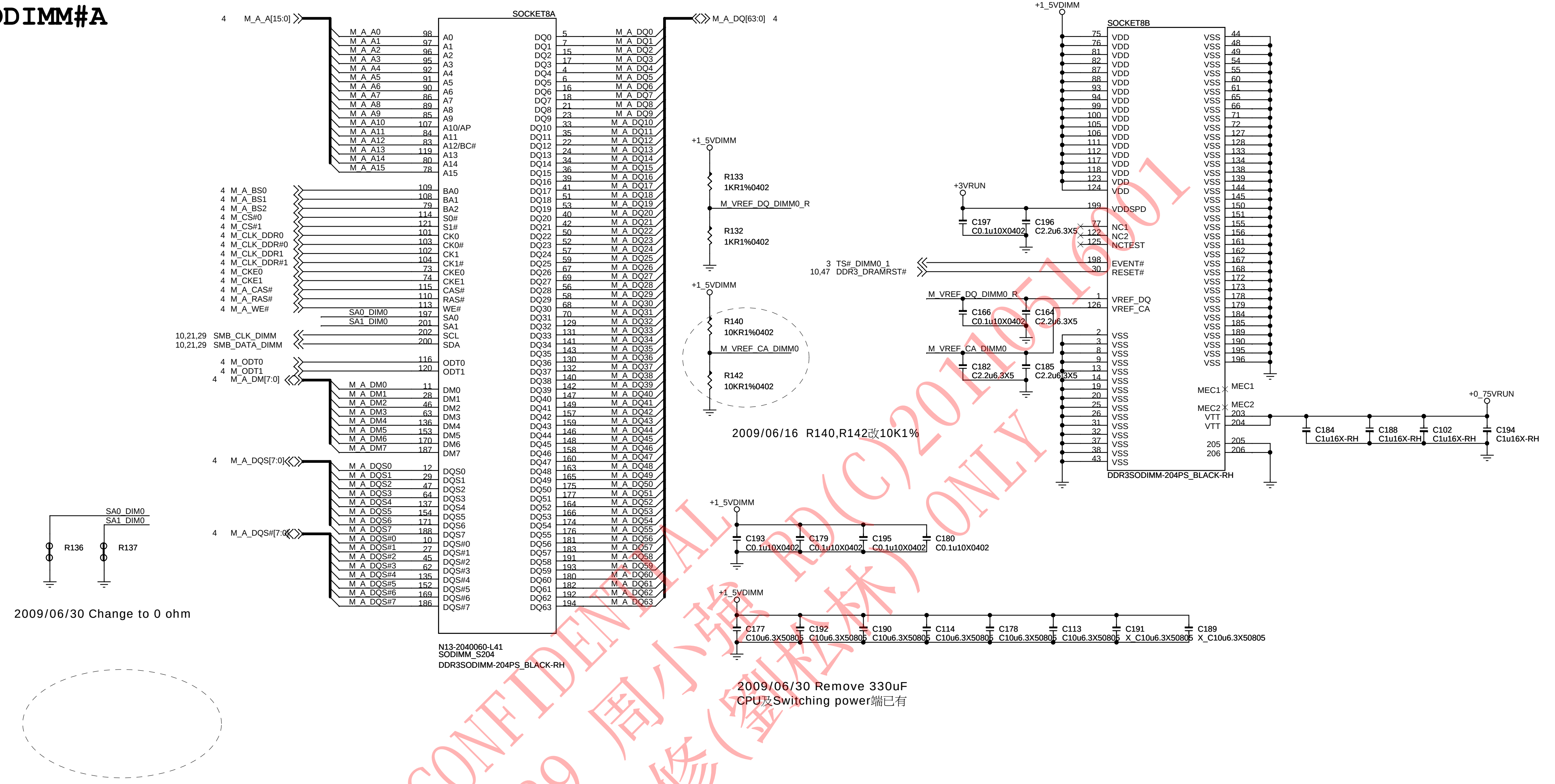
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



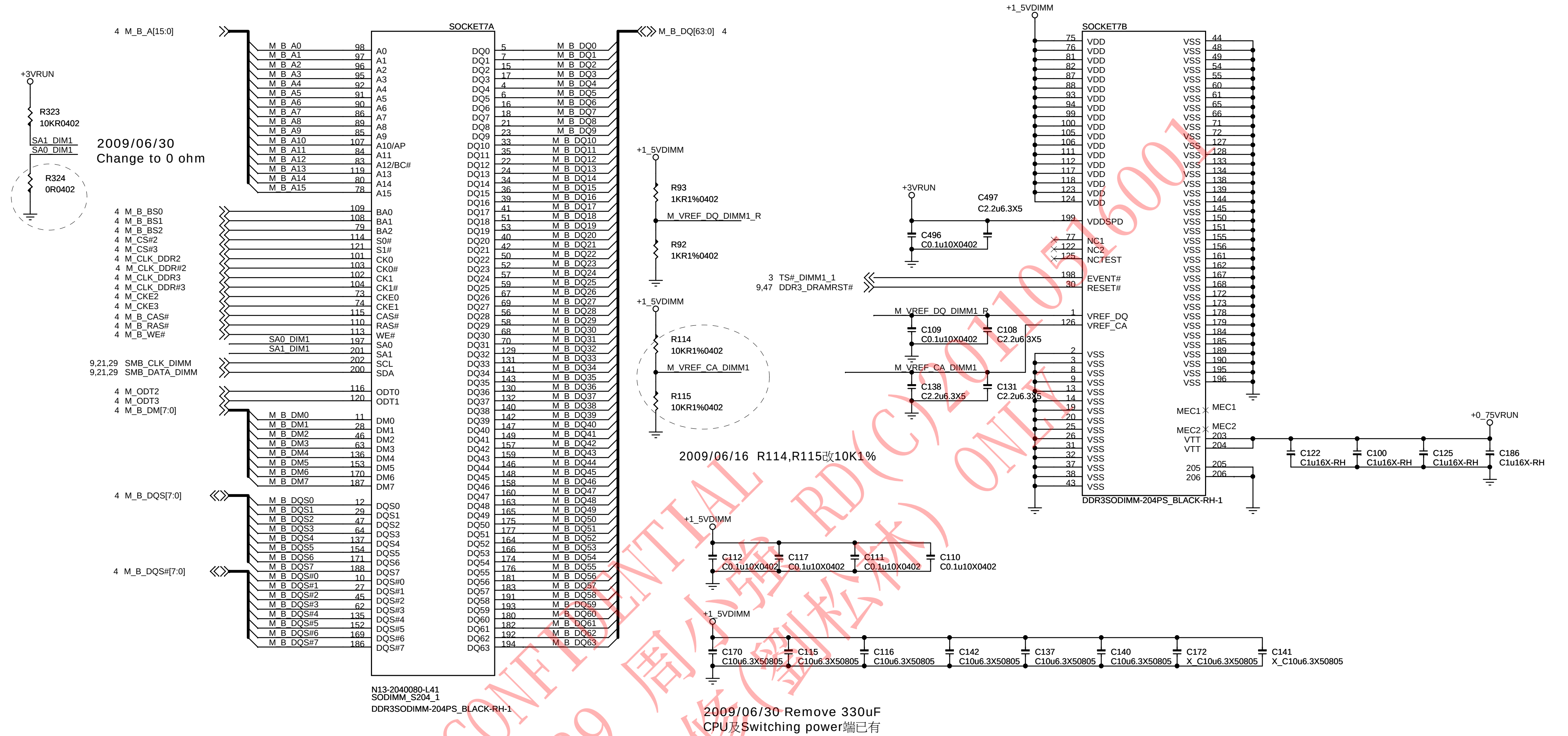
Layout Note:
Location of all CFG strap resistors needs
to be close to trace to minimize stub

SODIMM#A



SOCKET8A
M_A_A[15:0]
M_A_DQ[63:0]
M_A_BS0
M_A_BS1
M_A_BS2
M_CS#0
M_CS#1
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
M_CKE0
M_CKE1
M_A_CAS#
M_A_RAS#
M_A_WE#
SA0_DIM0
SA1_DIM0
SMB_CLK_DIMM
SMB_DATA_DIMM
M_ODT0
M_ODT1
M_A_DM[7:0]
M_A_DQS[7:0]
M_A_DQS#[7:0]
N13-2040060-L41
SODIMM_S204
DDR3SODIMM-204PS_BLACK-RH
SOCKET8B
+1_5VDIMM
+3VRUN
+0_75VRUN
R133 1KR1%0402
R132 1KR1%0402
M_VREF_DQ_DIMM0_R
R140 10KR1%0402
R142 10KR1%0402
M_VREF_CA_DIMM0
TS#_DIMM0_1
DDR3_DRAMRST#
C197 C0.1u10X0402
C196 C2.2u6.3X5
C166 C0.1u10X0402
C164 C2.2u6.3X5
C182 C2.2u6.3X5
C185 C2.2u6.3X5
C184 C1u16X-RH
C188 C1u16X-RH
C102 C1u16X-RH
C194 C1u16X-RH
C193 C0.1u10X0402
C179 C0.1u10X0402
C195 C0.1u10X0402
C180 C0.1u10X0402
C177 C10u6.3X50805
C192 C10u6.3X50805
C190 C10u6.3X50805
C114 C10u6.3X50805
C178 C10u6.3X50805
C113 C10u6.3X50805
C191 X_C10u6.3X50805
C189 X_C10u6.3X50805
R136
R137
2009/06/16 R140,R142改10K1%
2009/06/30 Change to 0 ohm
2009/06/30 Remove 330uF
CPU及Switching power端已有

SODIMM#B



MSI	MICRO-STAR INT'L CO.,LTD.
Title	DDR3 SODIMM1
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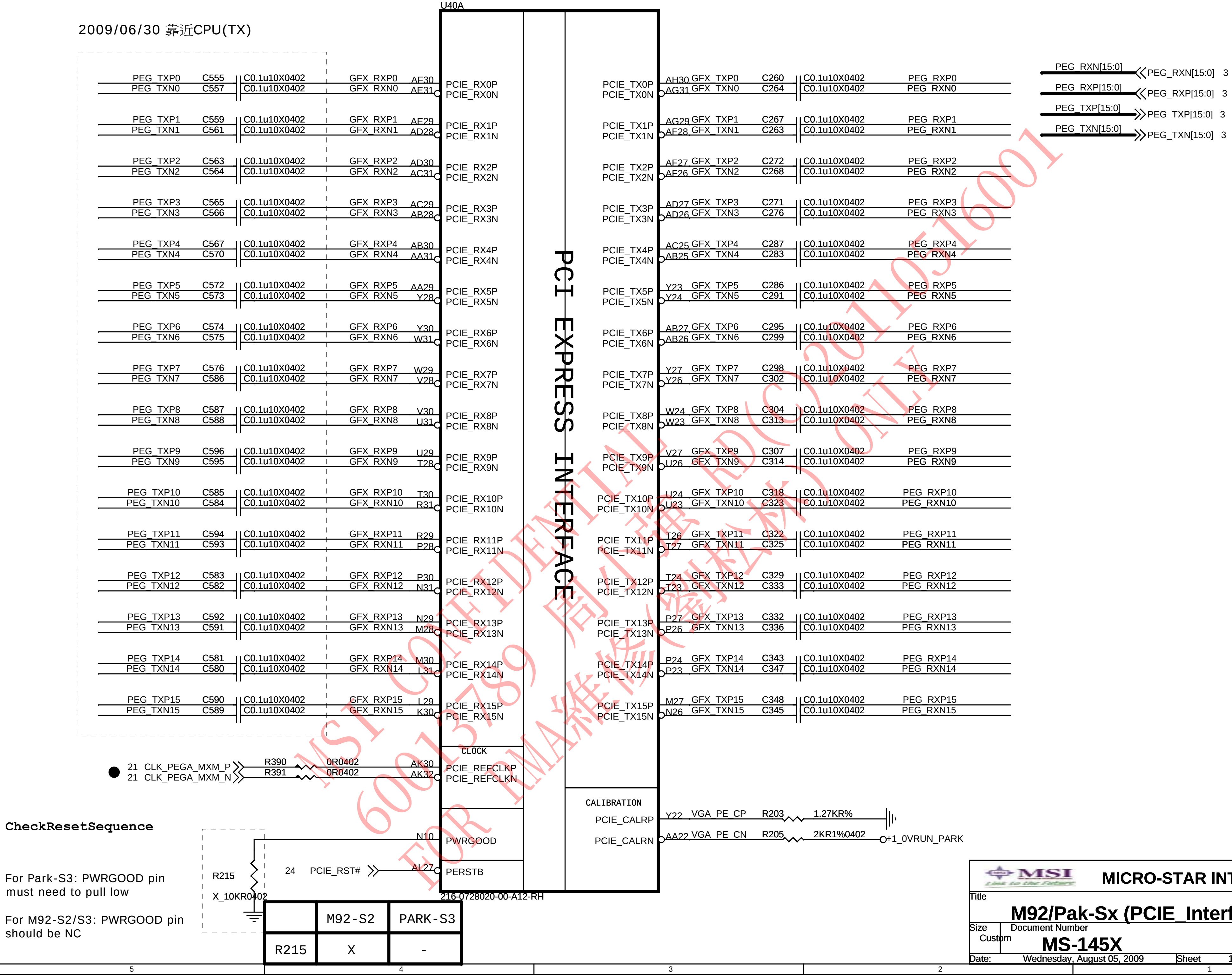
2009/06/30 靠近CPU(TX)



	M92-S2	PARK-S3
R215	X	-

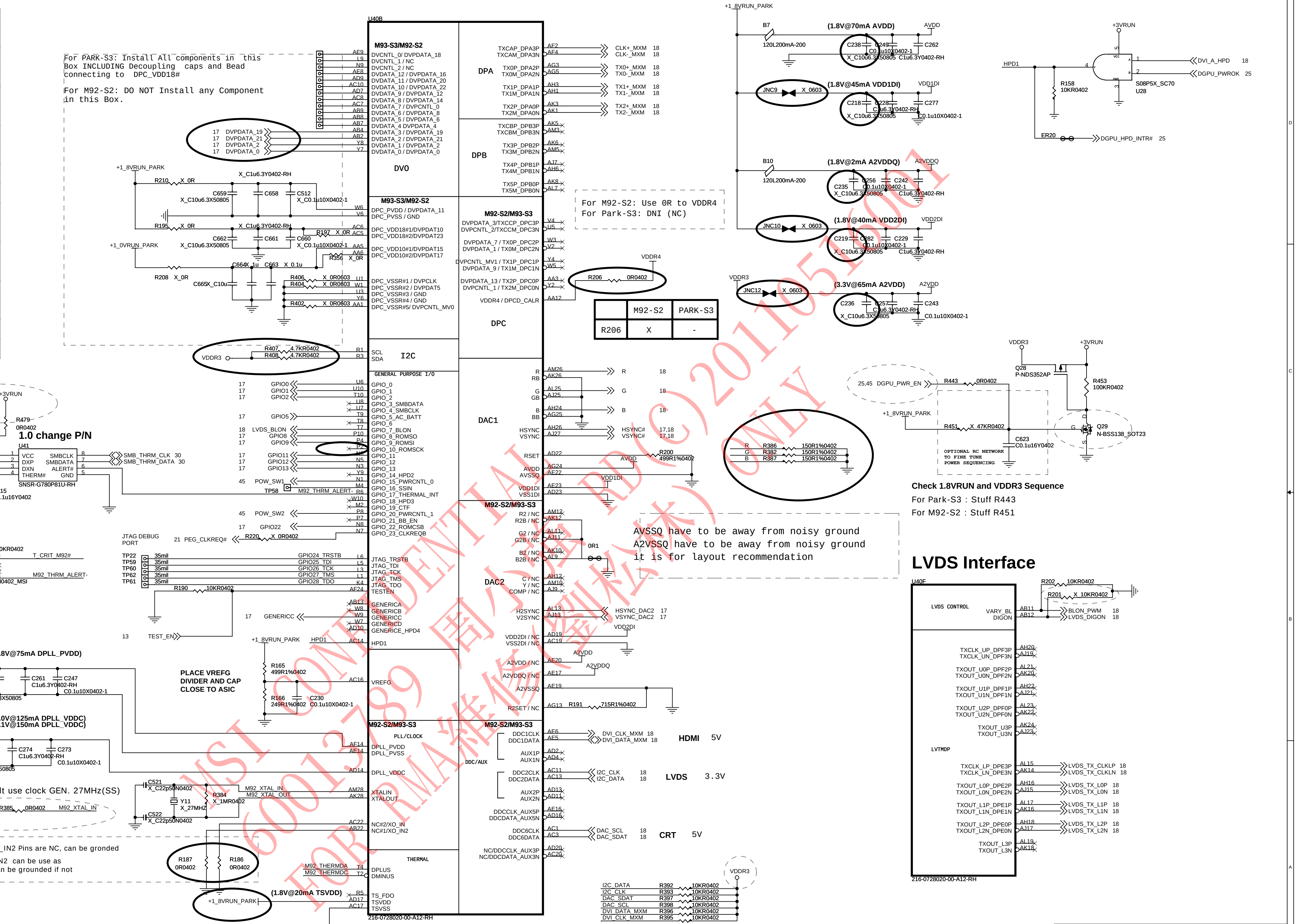
MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (PCIE_Interface)

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 11 of 56

	M92-S2	PARK-S3
R210	X	-
R195	X	-
R208	X	-
C659	X	-
C658	X	-
C512	X	-
C662	X	-
C661	X	-
C660	X	-
R197	X	-
R356	X	-
C665	X	-
C664	X	-
C663	X	-
R406	X	-
R404	X	-
R402	X	-



	M92-S2	PARK-S3
R206	X	-

Note:1
For M9x-S2/S3 XO_IN and XO_IN2 Pins are NC, can be gronded
For Park-S3: XO_IN and XO_IN2 can be use as 3.3V CLK Input. These poins can be grounded if not in use.

MICRO-STAR INT'L CO.,LTD.
Title: M92/Pak-Sx (Main IO)
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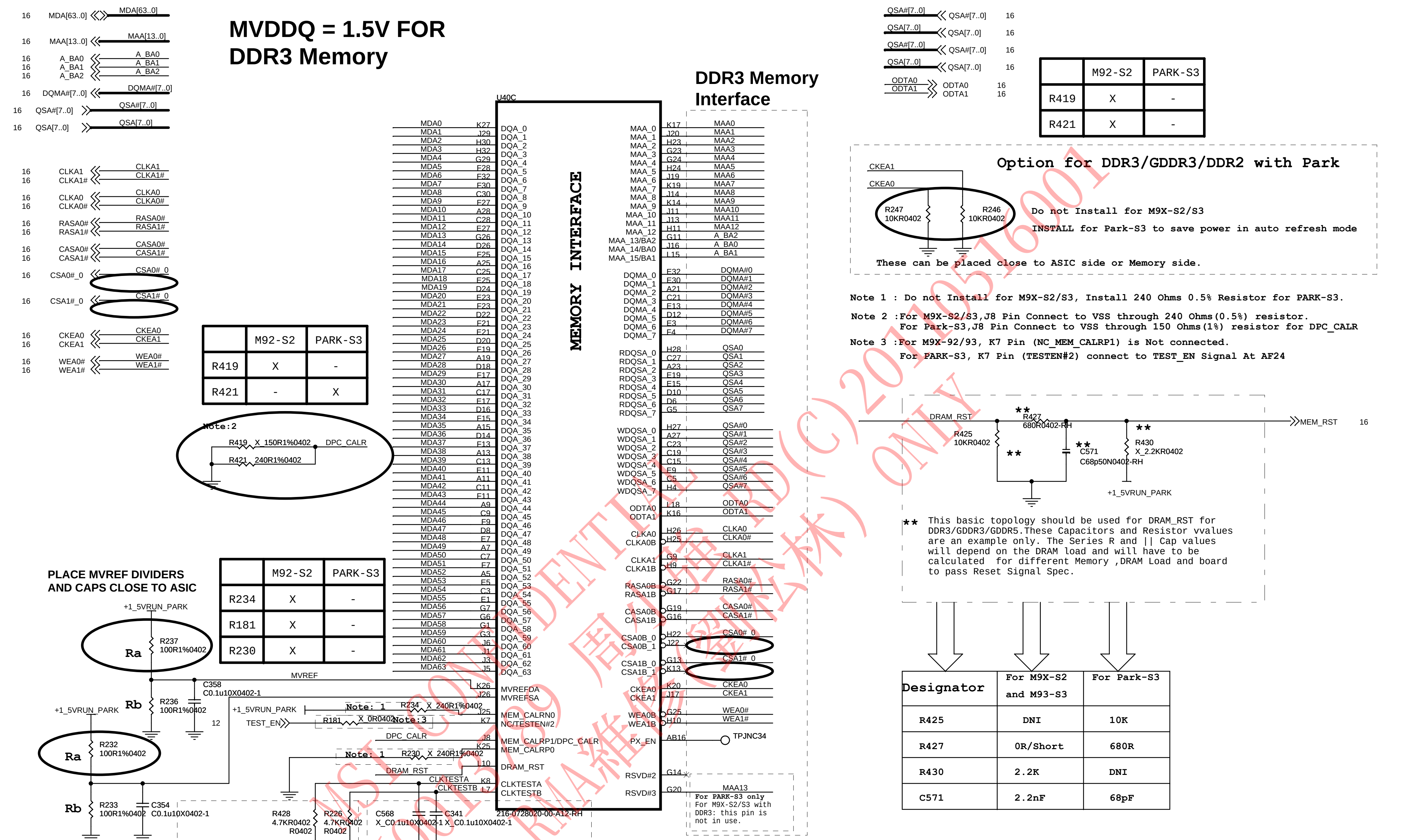
MVDDQ = 1.5V FOR DDR3 Memory

DDR3 Memory Interface



Use this option ONLY for M9x-S2/S3vFamily

route 50ohms single-ended/100ohms diff and keep short

Use this option ONLY for Park-S3

	M92-S2	PARK-S3
R419	X	-
R421	X	-

	M92-S2	PARK-S3
R419	X	-
R421	-	X

	M92-S2	PARK-S3
R234	X	-
R181	X	-
R230	X	-

	M92-S2	PARK-S3
R428	-	X
R226	-	X

	M92-S2	PARK-S3
C568	X	-
C341	X	-
R423	X	-
R227	X	-

DIVIDER RESISTORS	DDR3	GDDR3
MVREF TO 1.5V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

Option for DDR3/GDDR3/DDR2 with Park

Do not Install for M9X-S2/S3

INSTALL for Park-S3 to save power in auto refresh mode

These can be placed close to ASIC side or Memory side.

Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.

Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR

Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor vvalues are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For M9X-S2 and M93-S3	For Park-S3
R425	DNI	10K
R427	0R/Short	680R
R430	2.2K	DNI
C571	2.2nF	68pF

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (MEM_Interface)

Size: Custom | Document Number: MS-145X | Rev: 0A

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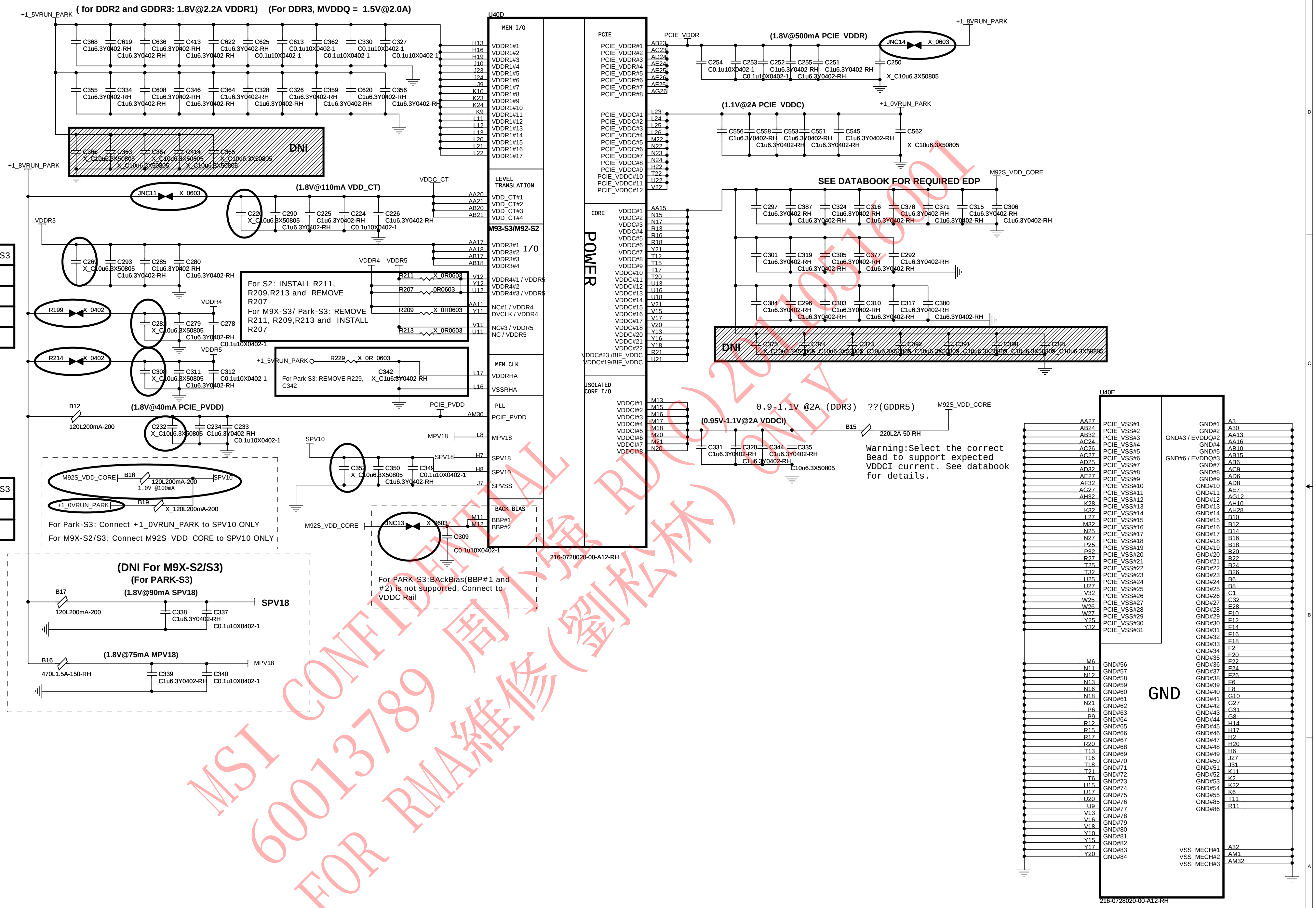
	M92-S2	PARK-S3
R211	-	X
R207	X	-
R209	-	X
R213	-	X

	M92-S2	PARK-S3
B18	-	X
B19	X	-



MICRO-STAR INT'L CO.,LTD.

Title: **M92/Pak-Sx (Power & GND)**

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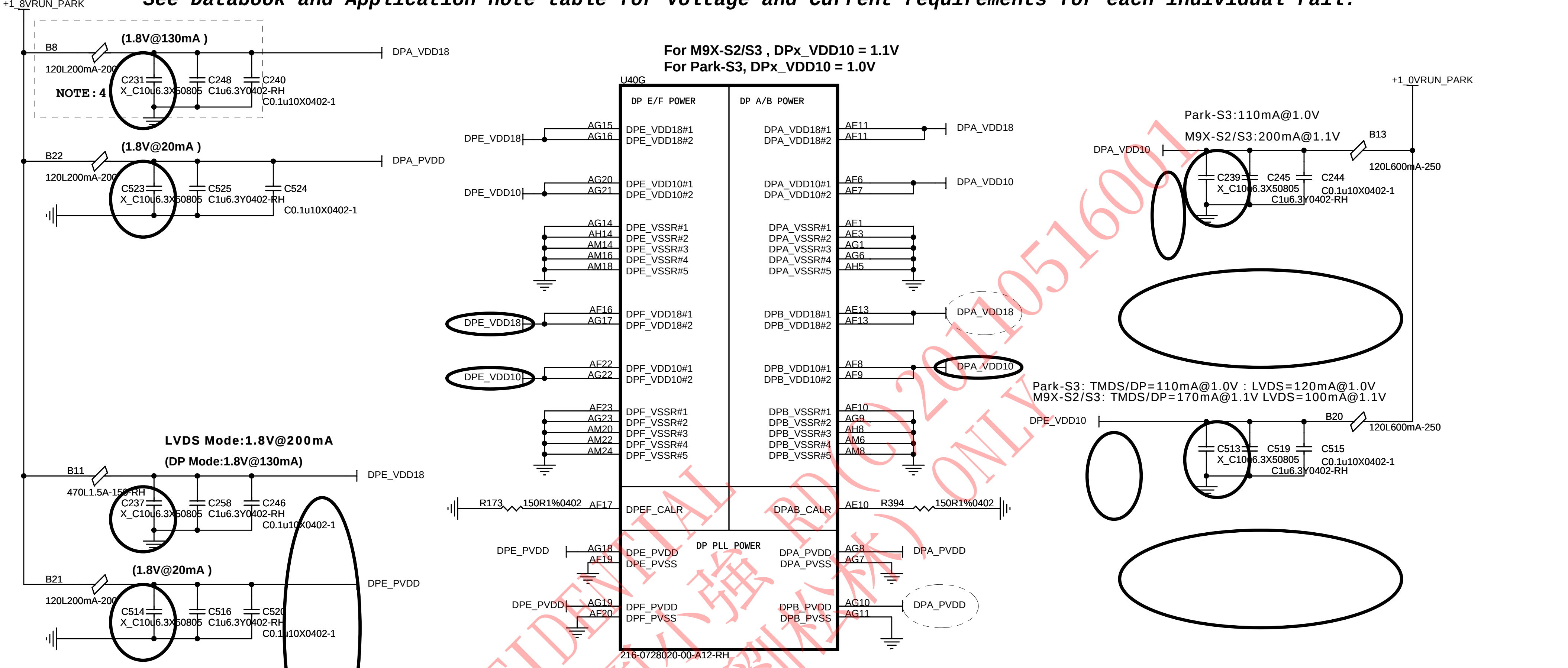
See Databook and Application note table for Voltage and Current requirements for each individual rail.



NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

MSI	MICRO-STAR INT'L CO.,LTD.
Title	M92/Pak-Sx (DP_Power)
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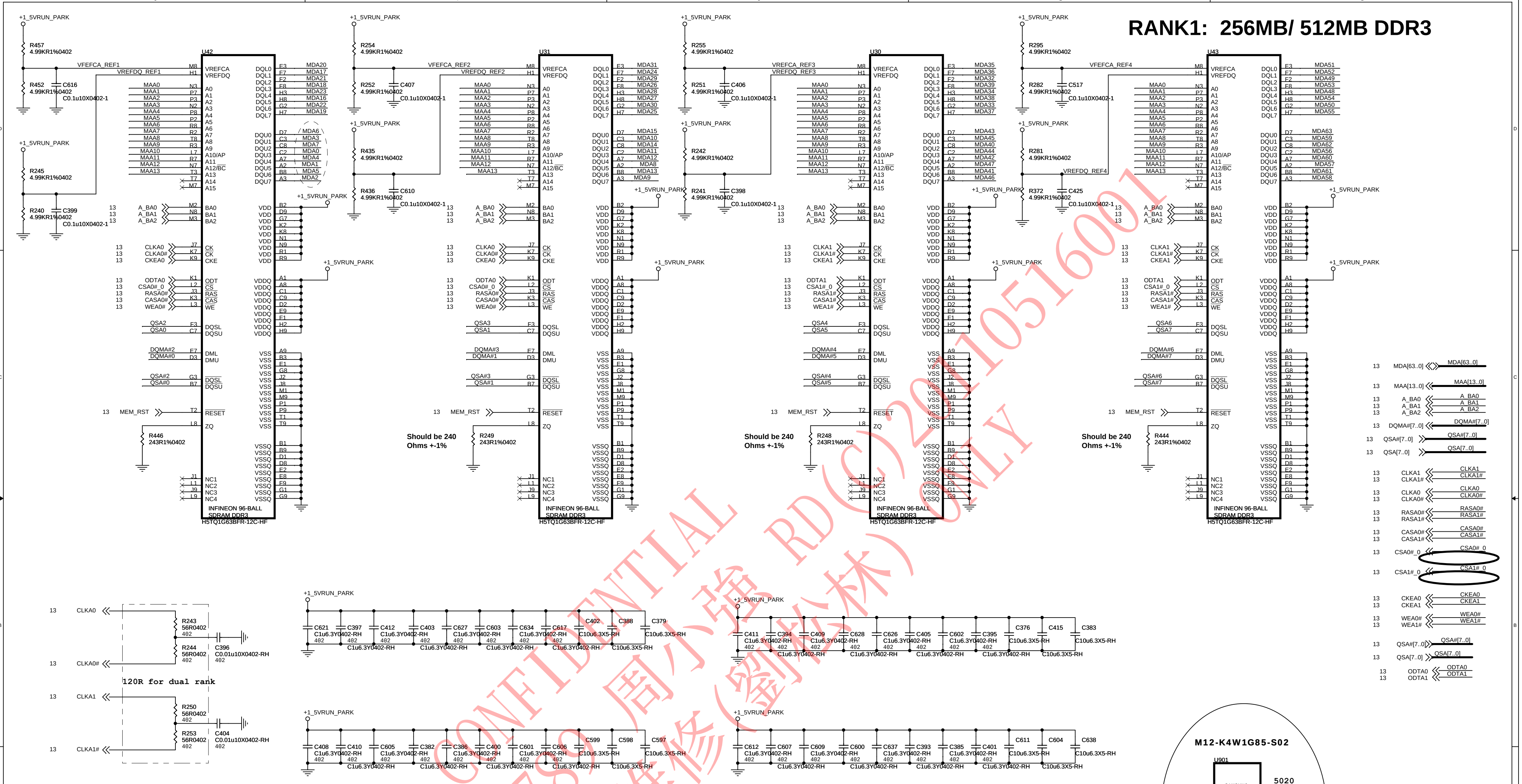

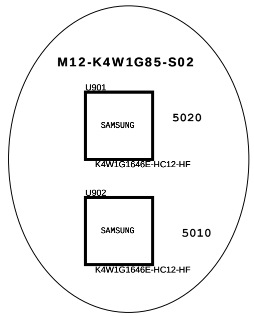

For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64MX16 DDR3. MAA13 is NC

For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128MX16 DDR3.

MICRO-STAR INT'L CO.,LTD.		
Title: DDR2 (64Mx16bit)		
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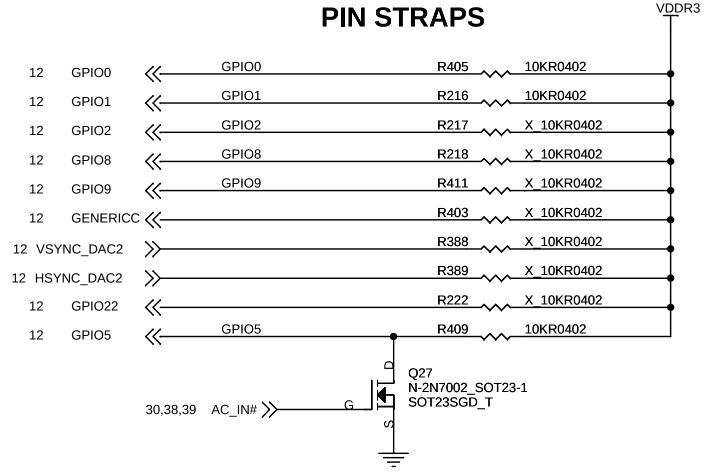
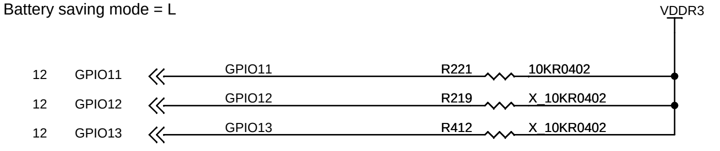
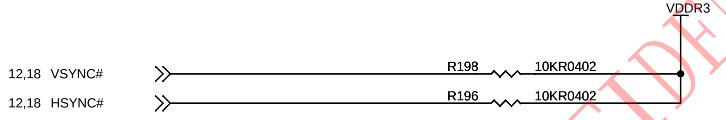
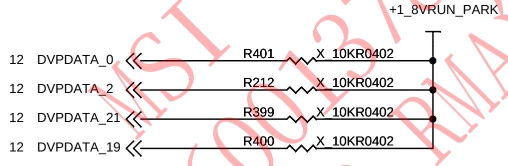
PIN STRAPS



GPIO_5_AC_BATT is an optional input which allows the system to request (AC) performance mode or battery mode operation.
AC (Performance mode) = H
Battery saving mode = L







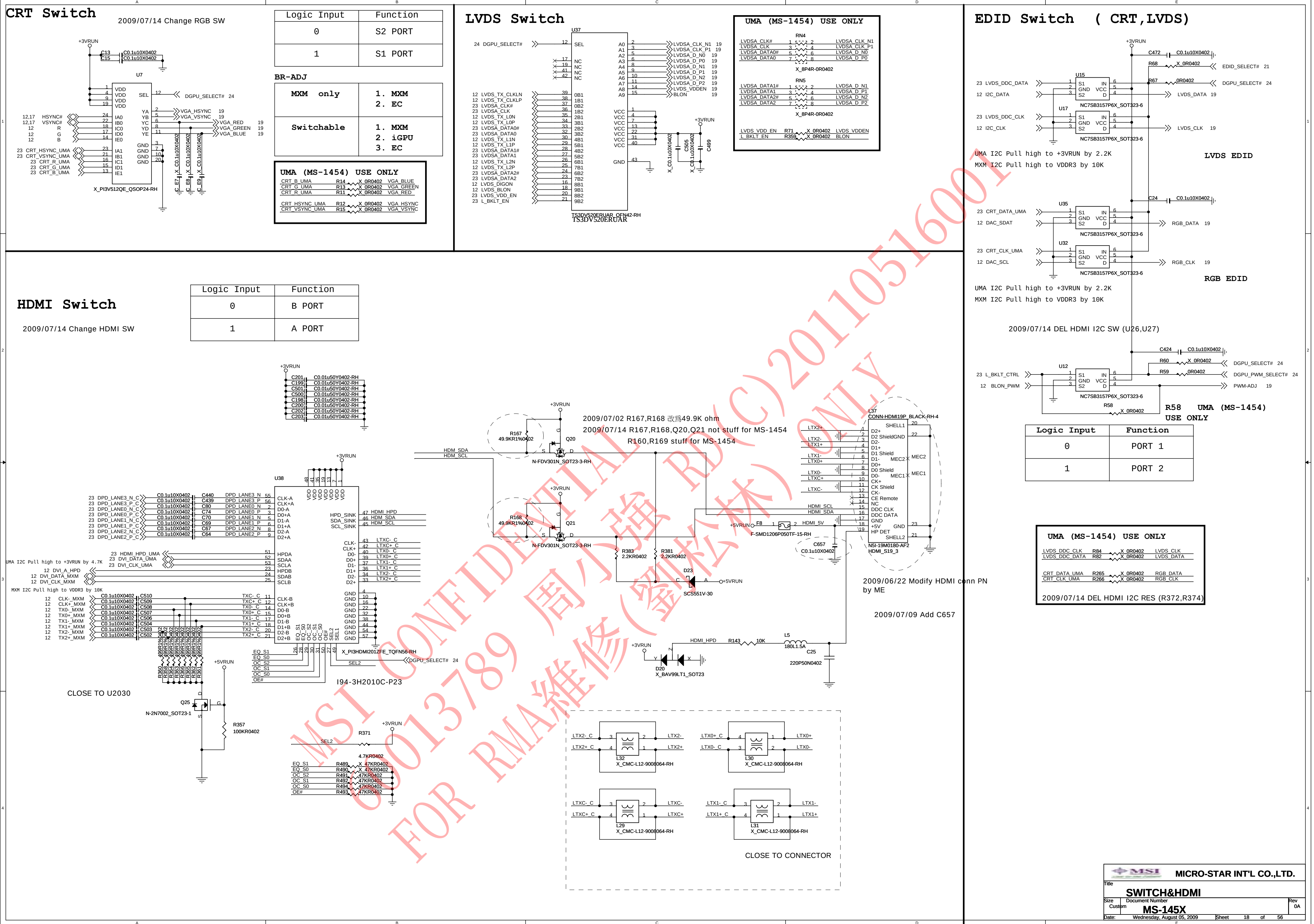
CONFIGURATION STRAPS

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO0	1		GPIO=0 50% TX output swing GPIO=1 Full TX output swing
GPIO1	1		GPIO=0 TX de-emphasis disabled GPIO=1 TX de-emphasis enabled
GPIO2	1		GPIO=0 Advertises the PCIE device as 2.5 GT/S capable at power -on GPIO=1 Advertises the PCIE device as 5 GT/S capable at power -on
GPIO9	0		GPIO=0 VGA controller capacity enabled. GPIO=1 The device will not be recognized as the system's VGA controler.
VSYNC_DAC2	0		GPIO=0 Driver would ignore the value sampled on DVPDATA_20 during reset.
GPIO22	0		GPIO=0 not used external BIOS ROM GPIO=1 if used

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO 13 GPIO 12 GPIO 11	0 0 1		0 0 0=128 MB 0 0 1=256 MB 0 1 0=64 MB

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
VGA_HSYNC# VGA_VSYNC#	1 1		0 0=No audio function 0 1=Audio for display port only 1 0=Audio for display port and HDMI if dongle is detected 1 1=Audio for both displayport and HDMI

DVPDATA19	DVPDATA21	DVPDATA2	DVPDATA0	MEM_TYPE
0	0	0	0	Hynix 64Mx16 DDR3 (M12-5TQ1G25-H23)
0	0	0	1	Samsung 64Mx16 DDR3 (M12-K4W1G85-S02)
0	0	1	0	
0	0	1	1	



CRT Switch

Logic Input	Function
0	S2 PORT
1	S1 PORT

BR-ADJ

MXM only	1. MXM 2. EC
Switchable	1. MXM 2. iGPU 3. EC

HDMI Switch

Logic Input	Function
0	B PORT
1	A PORT

EDID Switch (CRT,LVDS)

Logic Input	Function
0	PORT 1
1	PORT 2

UMA (MS-1454) USE ONLY

MICRO-STAR INT'L CO.,LTD.

Title: SWITCH&HDMI

Size: Custom | Document Number: MS-145X | Rev: 0A

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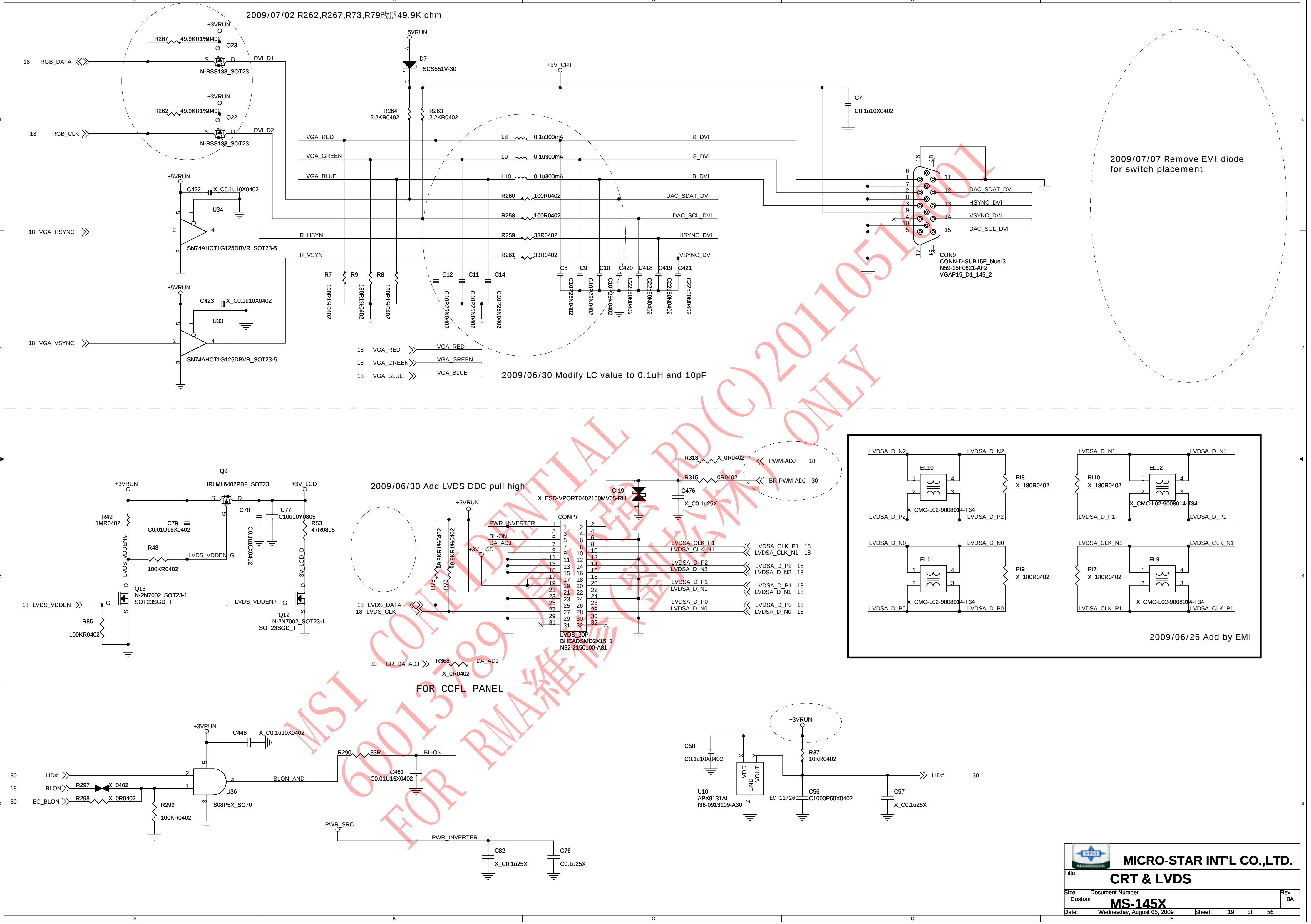

2009/07/02 R262,R267,R73,R79改爲49.9K ohm
RGB_DATA
RGB_CLK
N-BSS138_SOT23
+5VRUN
D7
SCS551V-30
+5V_CRT
C7
C0.1u10X0402
VGA_RED
VGA_GREEN
VGA_BLUE
R_DVI
G_DVI
B_DVI
DAC_SDAT_DVI
DAC_SCL_DVI
HSYNC_DVI
VSYNC_DVI
VGA_HSYNC
VGA_VSYNC
SN74AHCT1G125DBVR_SOT23-5
CON9
CONN-D-SUB15F_blue-3
N59-15F0621-AF2
VGAP15_D1_145_2
2009/07/07 Remove EMI diode for switch placement
2009/06/30 Modify LC value to 0.1uH and 10pF
2009/06/30 Add LVDS DDC pull high
IRLML6402PBF_SOT23
+3V_LCD
LVDS_VDDEN
N-2N7002_SOT23-1
CONP7
LVDS_30P
BHEADSMD2X15_1
N32-2150100-A81
PWM-ADJ
BR-PWM-ADJ
X_ESD-VPORT0402100MV05-RH
LVDSA_CLK_P1
LVDSA_CLK_N1
LVDSA_D_P2
LVDSA_D_N2
LVDSA_D_P1
LVDSA_D_N1
LVDSA_D_P0
LVDSA_D_N0
X_CMC-L02-9008014-T34
2009/06/26 Add by EMI
BR_DA_ADJ
FOR CCFL PANEL
LID#
BLON
EC_BLON
S08P5X_SC70
BLON_AND
BL-ON
PWR_SRC
PWR_INVERTER
U10
APX9131AI
I36-0913109-A30
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CRT & LVDS
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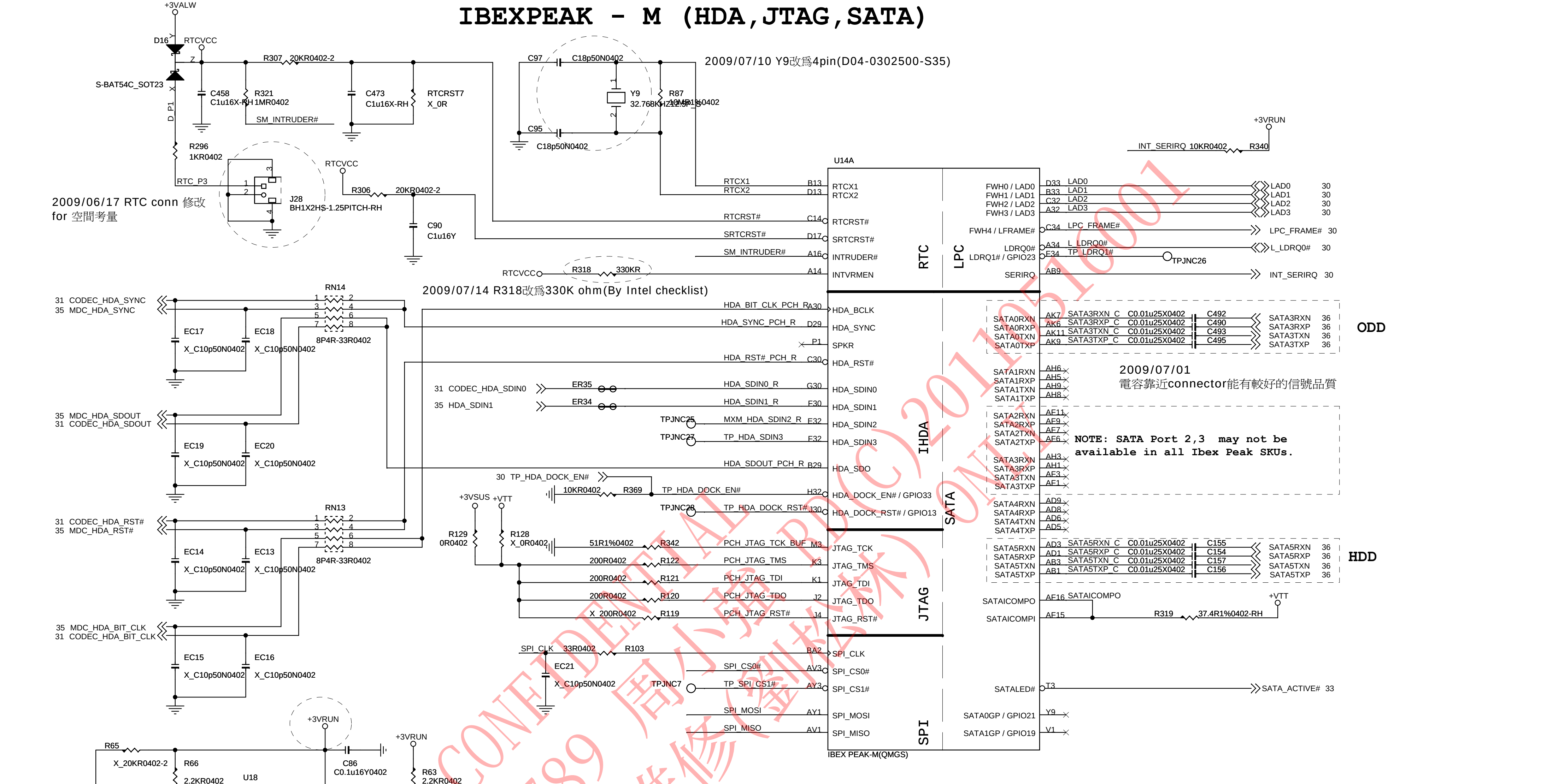
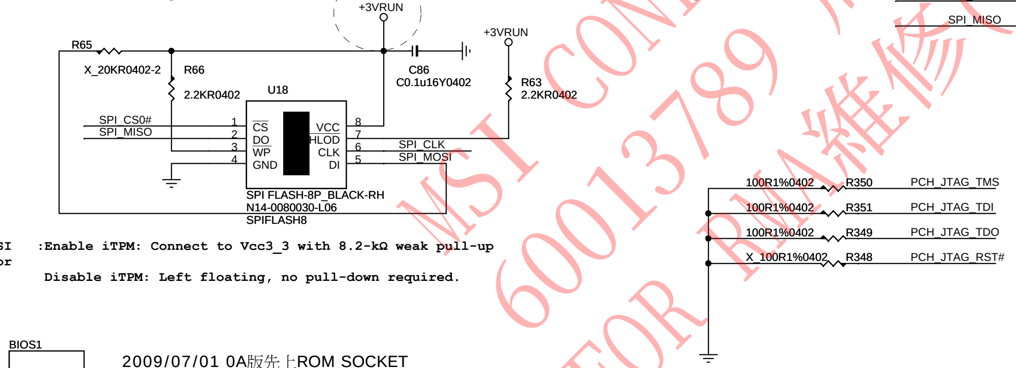
IBEXPEAK - M (HDA,JTAG,SATA)





SPI_MOSI :Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor

Disable iTPM: Left floating, no pull-down required.

BIOS1

W25X32VSSIG-RH

2009/07/01 0A版先上ROM SOCKET

PCH Pin	RefDes	Pre-Production Systems ES1	ES2	Production Systems
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

2009/07/14
需注意QS之後版本只需TCK的R342上件

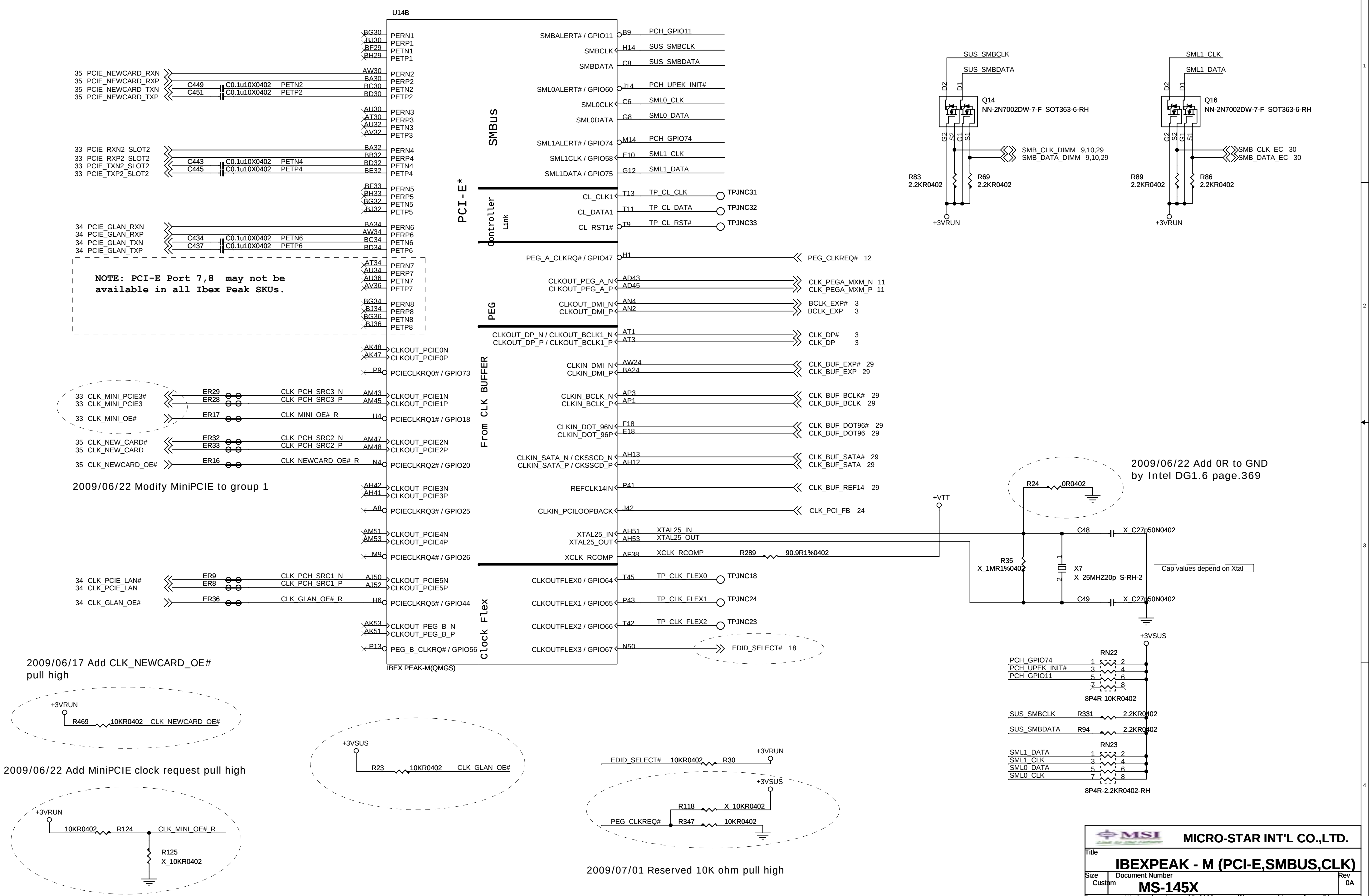
MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (HDA,JTAG,SATA)

Size: Custom | Document Number: MS-145X | Rev: 0A

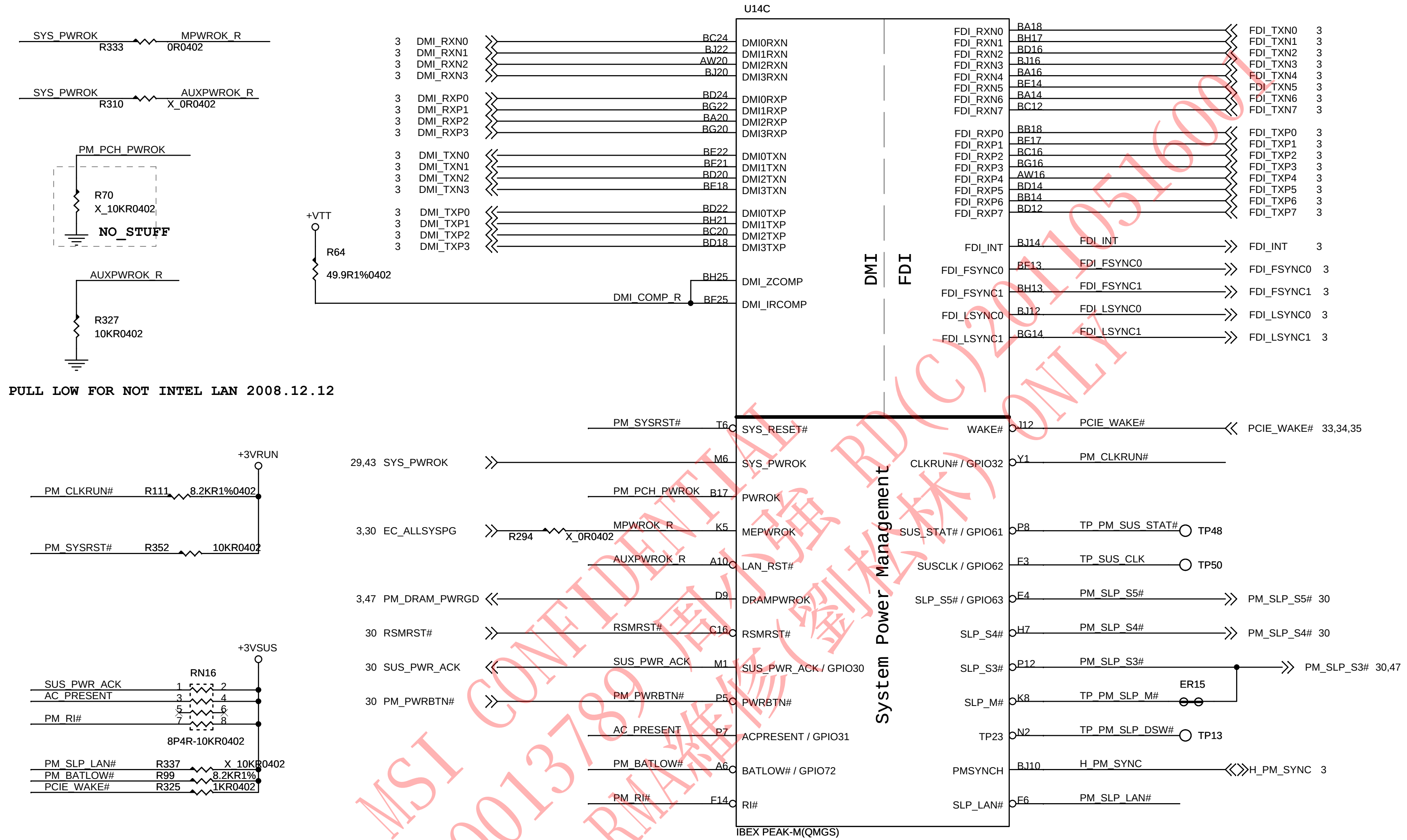
Date: Wednesday, August 05, 2009 | Sheet 20 of 56

IBEXPEAK - M (PCI-E,SMBUS,CLK)



MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK - M (PCI-E,SMBUS,CLK)	
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 21 of 56	

IBEXPEAK - M (DMI,FDI,GPIO)



MSI MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (DMI,FDI,GPIO)
Size	Custom
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Date:	Wednesday, August 05, 2009
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IBEXPEAK - M (LVDS,DDI)

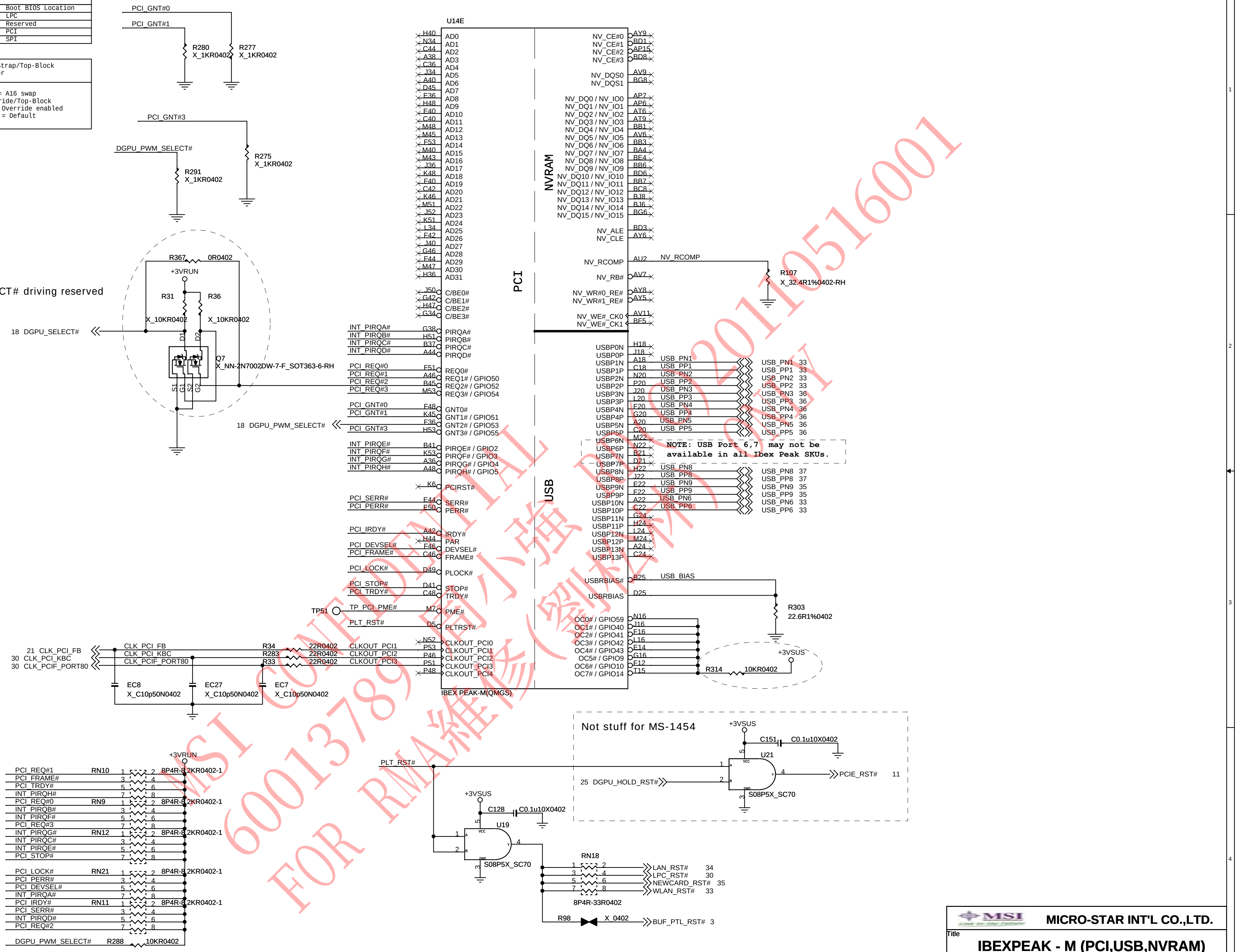
DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

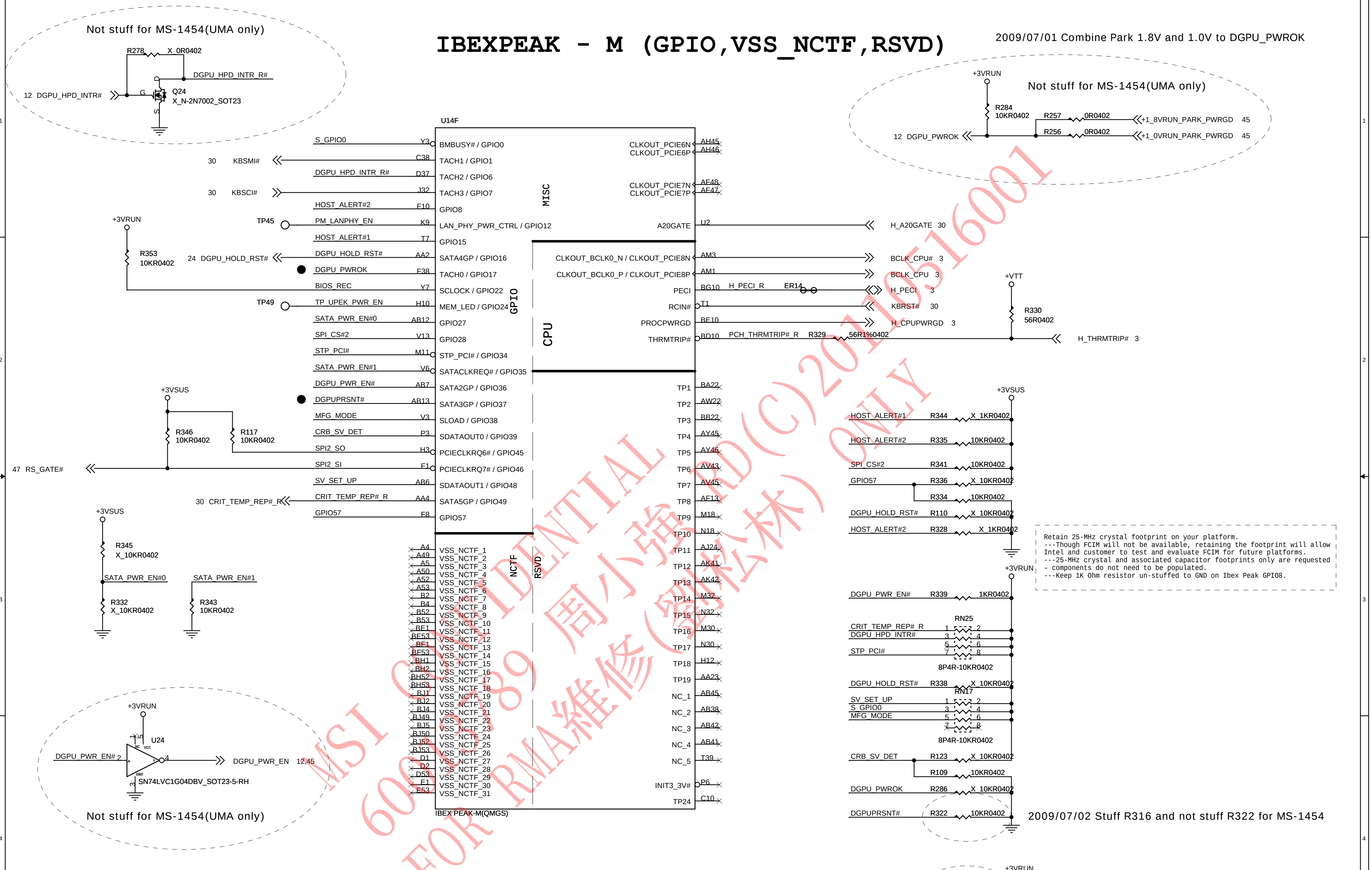
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

2009/06/26 For DGPU_SELECT# driving reserved
(No need for MS-1454)
R367 not stuff for MS-1454



IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

2009/07/01 Combine Park 1.8V and 1.0V to DGPU_PWROK



MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)

Size: Custom | Document Number: MS-145X | Rev: 0A

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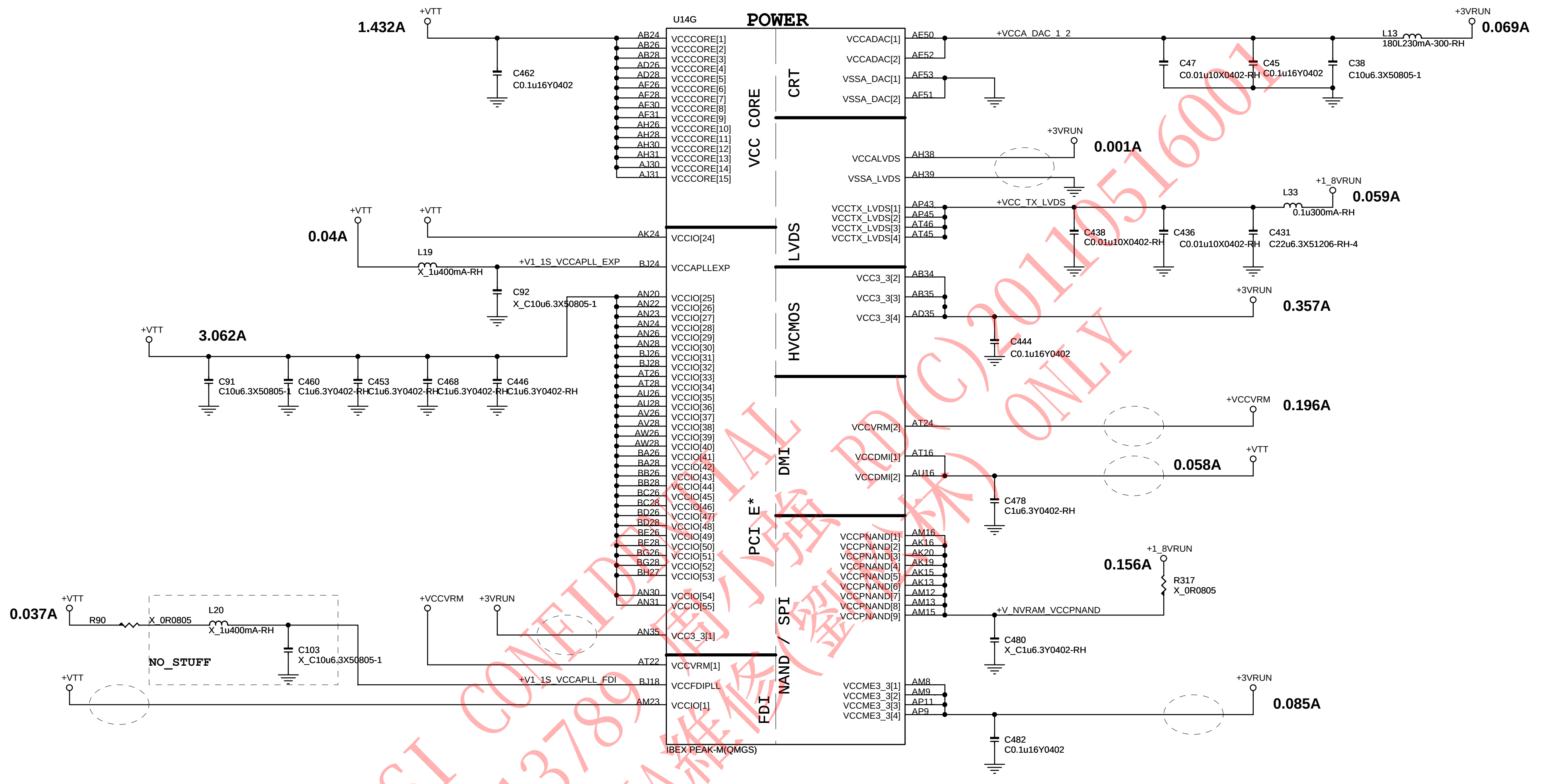
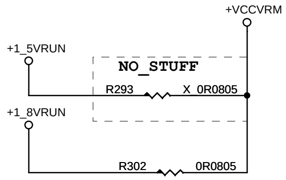
IBEXPEAK - M (POWER)



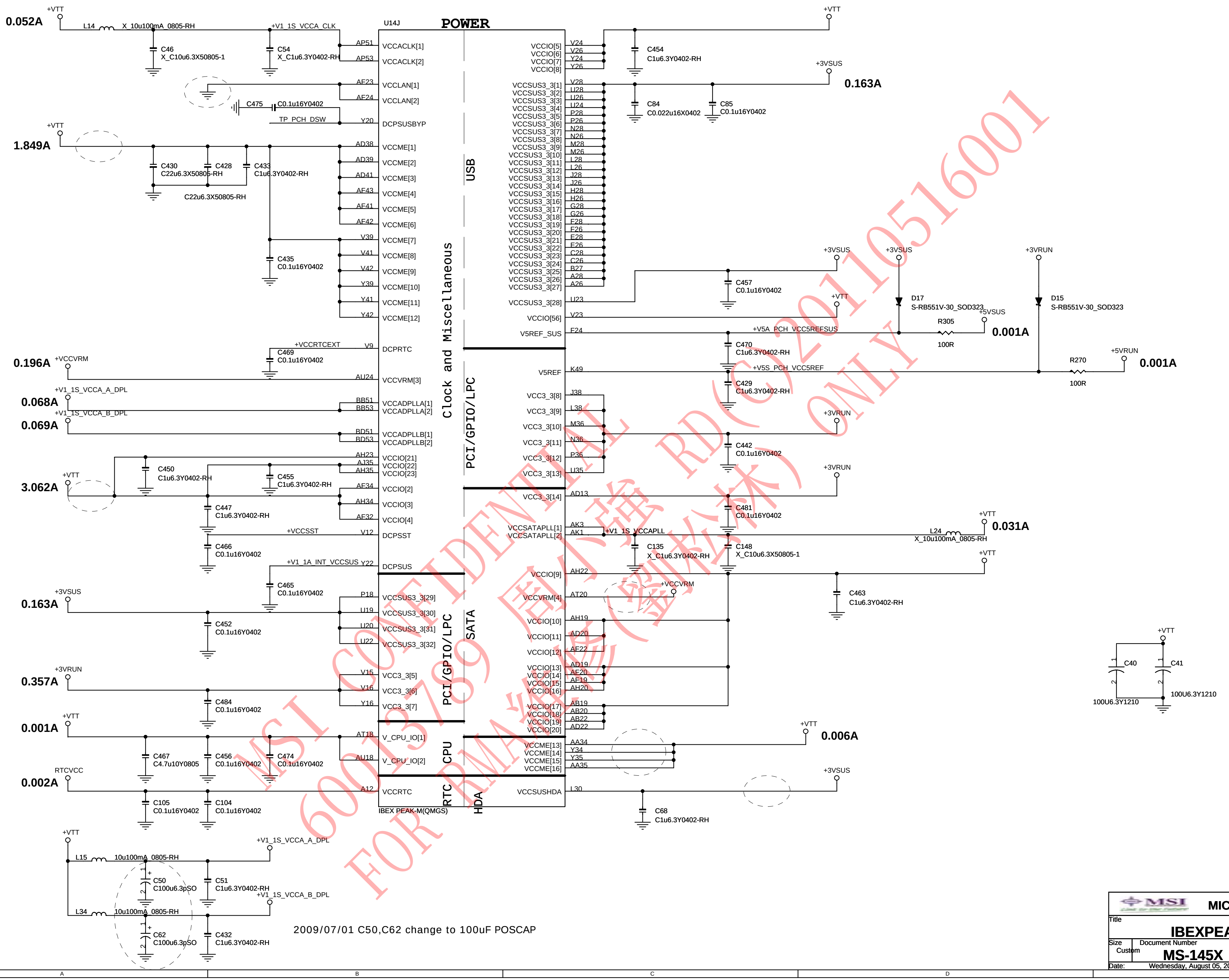
The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



MICRO-STAR INT'L CO.,LTD.

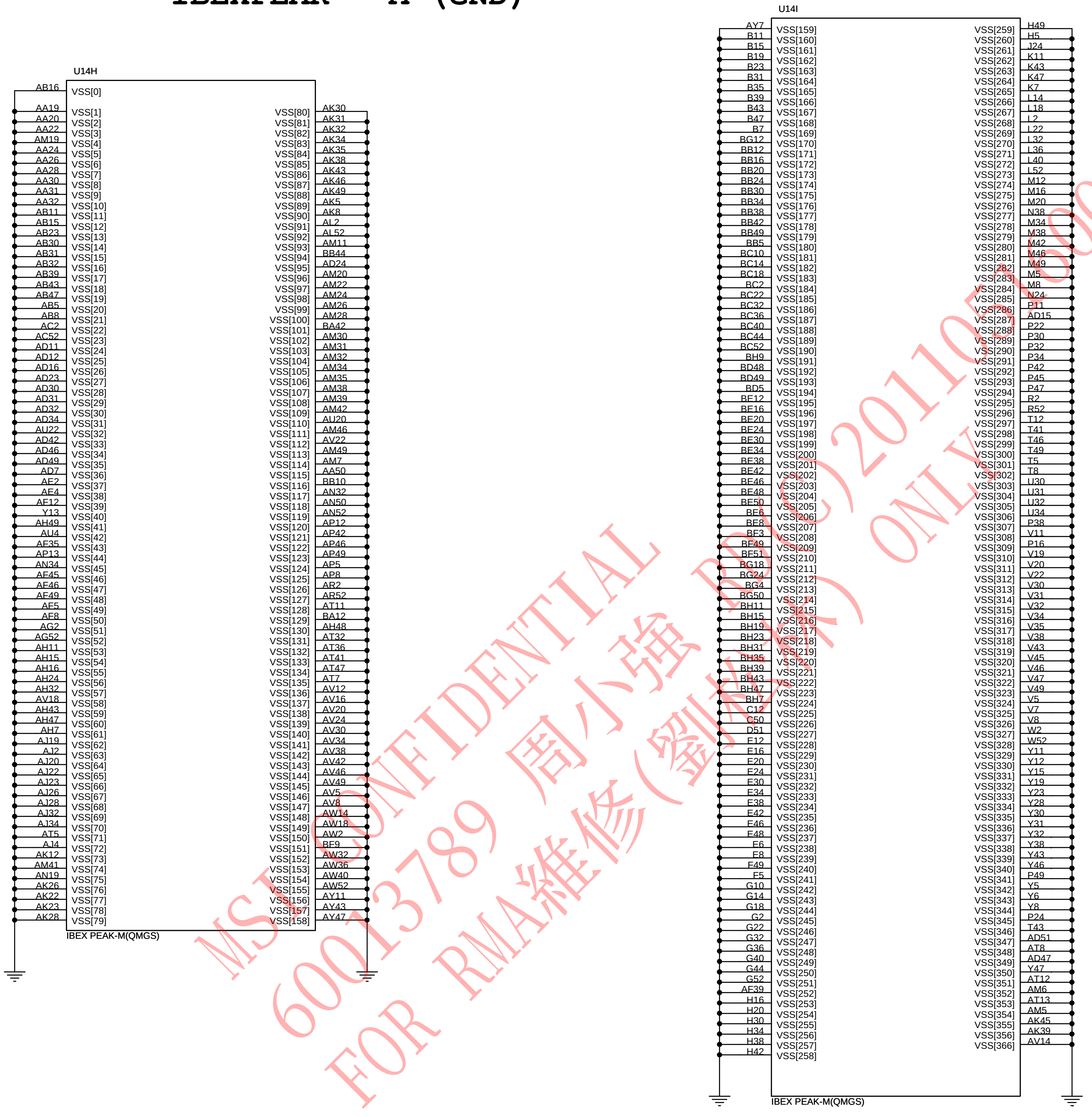
Title	IBEXPEAK - M (POWER)	
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 26 of 56	

IBEXPEAK - M (POWER)



2009/07/01 C50,C62 change to 100uF POSCAP

IBEXPEAK - M (GND)



MICRO-STAR INT'L CO.,LTD.			
Title	IBEXPEAK - M (GND)		
Size: Custom	Document Number: MS-145X		Rev: 0A
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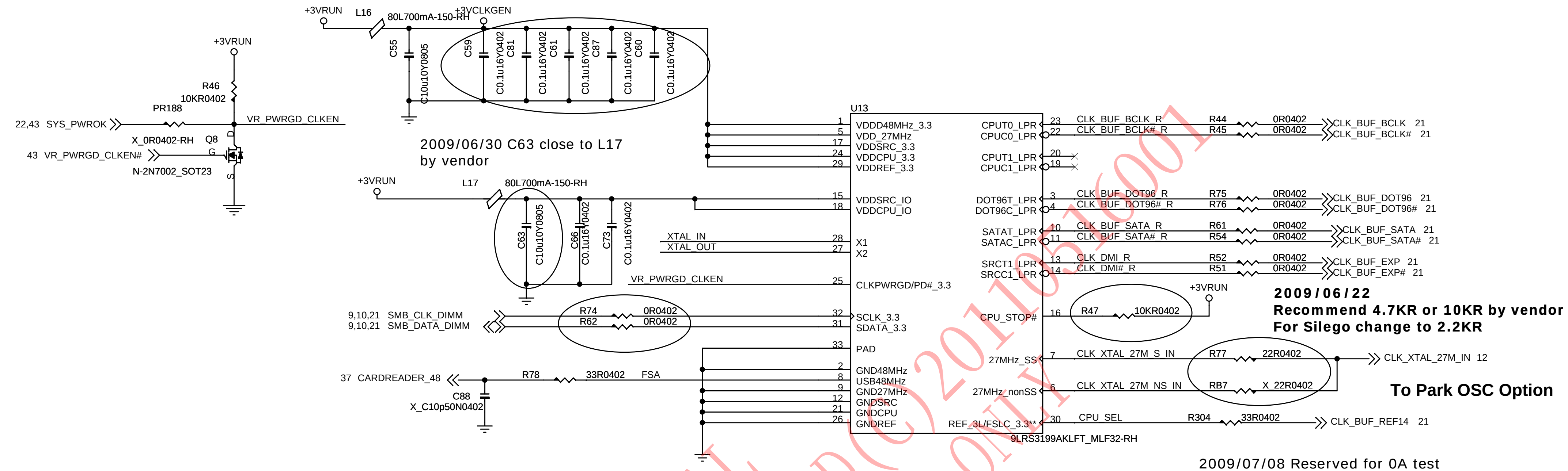
C59 Close to L16 ; C60,C61,C81,C87 Close to power pin



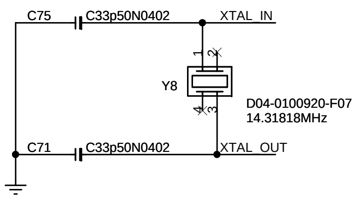
2009/06/30 C63 close to L17
by vendor

2009/06/22
Recommend 4.7KR or 10KR by vendor
For Silego change to 2.2KR

To Park OSC Option

2009/07/08 Reserved for 0A test
R3211 is for Spread clock(Default use)
RB8 is for non-Spread clock

2009/07/08
Y4換成49S type(cost down as MS-1122)

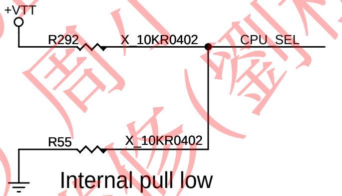


Capacity select

If Cload=20pf C71/C75=33pf

If Cload=32pf C71/C75=56pf

2009/06/30 R292 not stuff



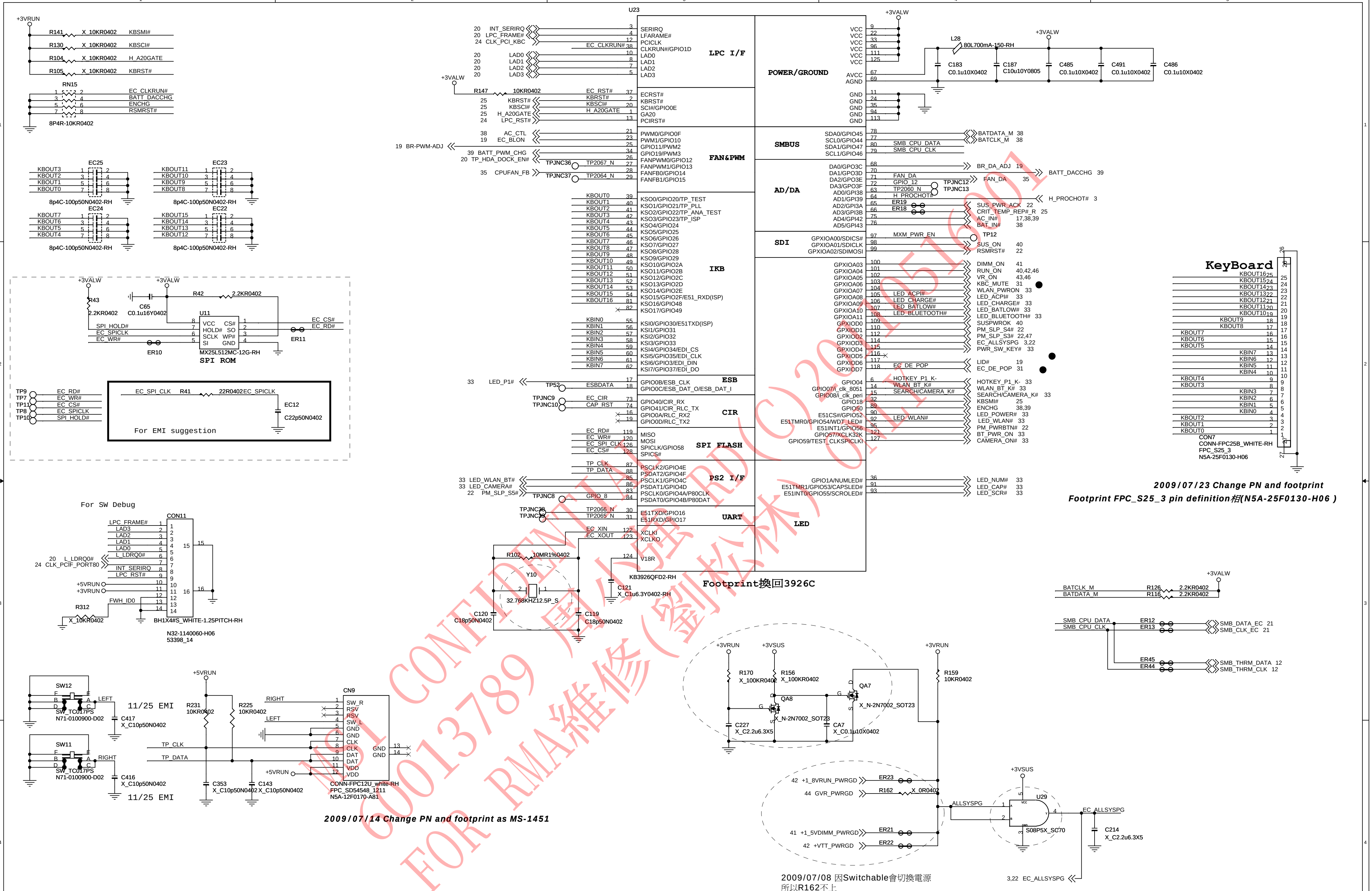
Internal pull low

For CPU frequency select (133MHz)

CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

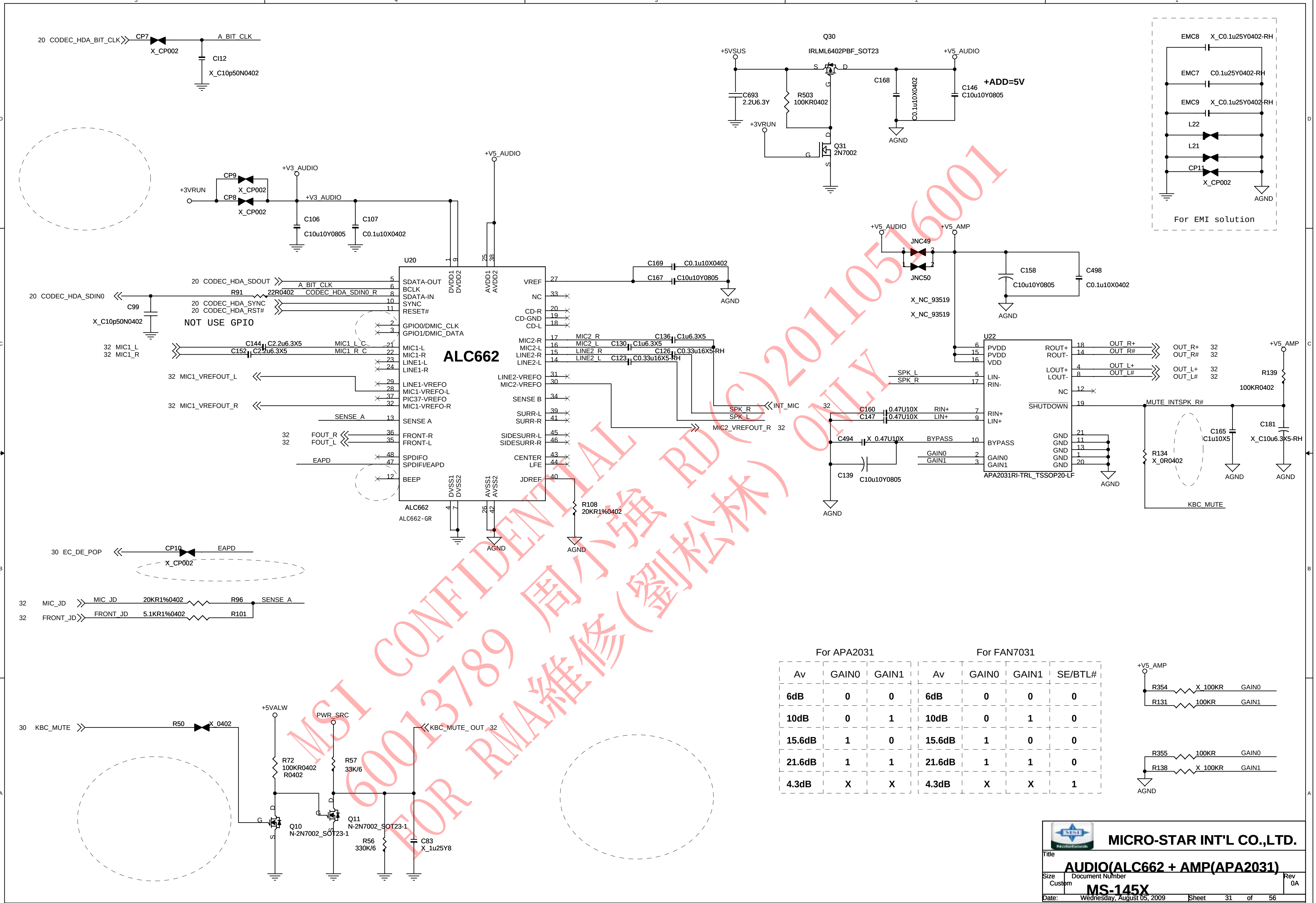
Clock GEN. Vendor Table

	9LRS3199	SLG8SP587V
VDDIO spec	0.9975~3.465	1.05~3.466
BOM	R39 stuff	R40 stuff



MICRO-STAR INT'L CO.,LTD.

Title	KBC/EC/uP (ENE3925-LFQP144)	
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 30 of 56	



For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

For FAN7031

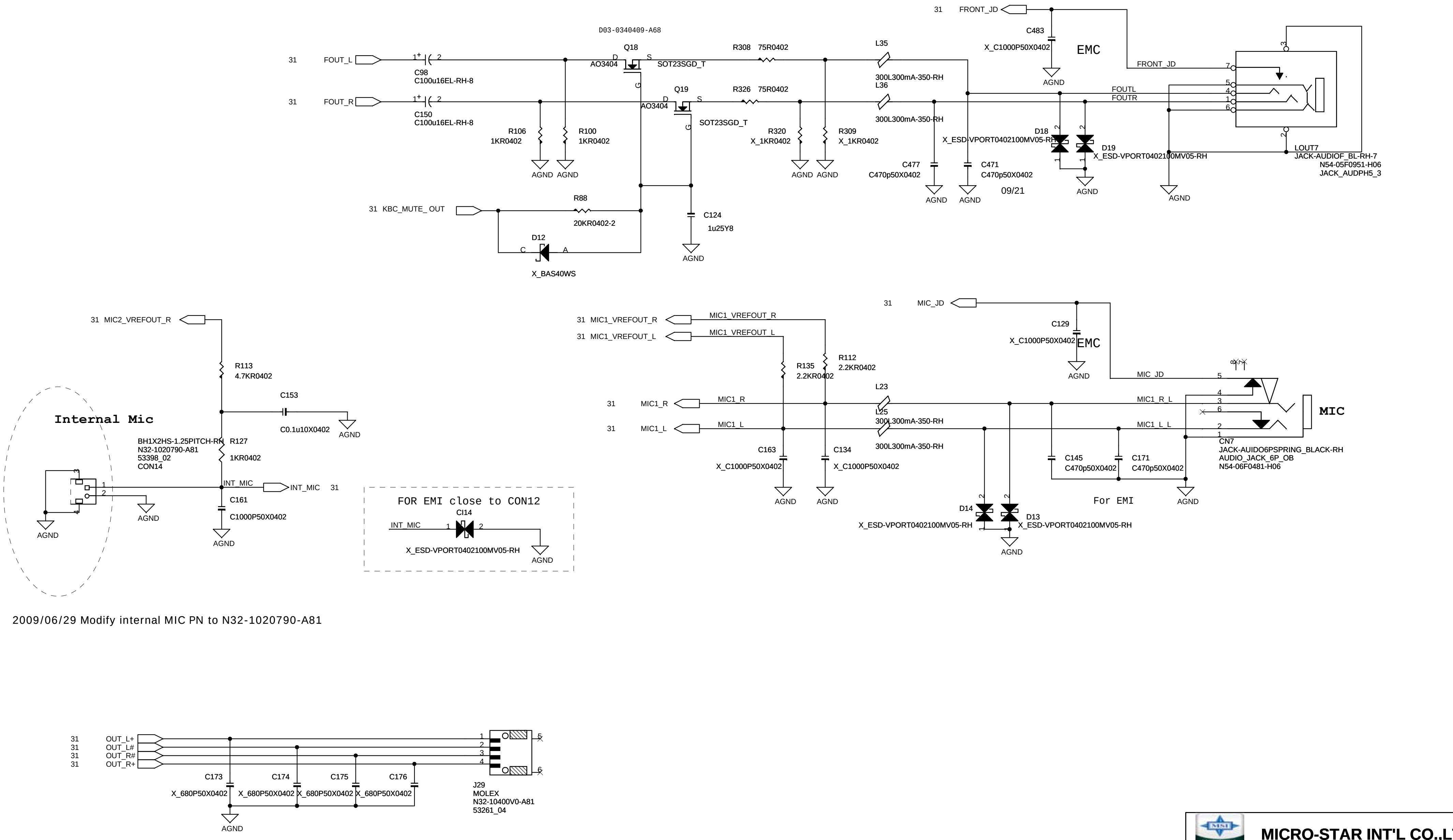
Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

MICRO-STAR INT'L CO.,LTD.

Title: AUDIO(ALC662 + AMP(APA2031))

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 31 of 56



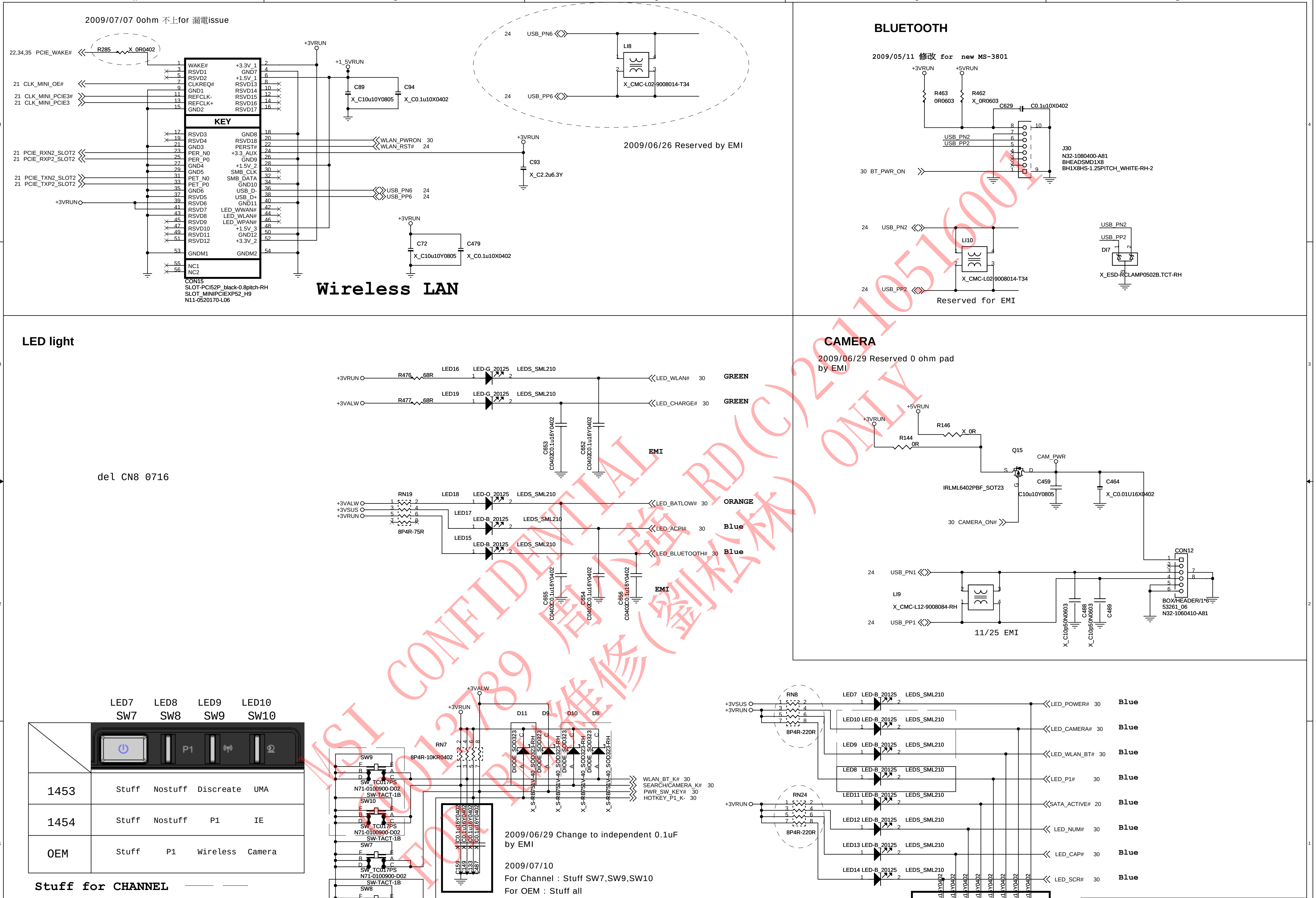
2009/06/29 Modify internal MIC PN to N32-1020790-A81

MICRO-STAR INT'L CO.,LTD.

Title: **SPK / HP / MIC**

Size	Document Number	Rev
Custom	MS-145X	0A

Date: Wednesday, August 05, 2009 | Sheet 32 of 56



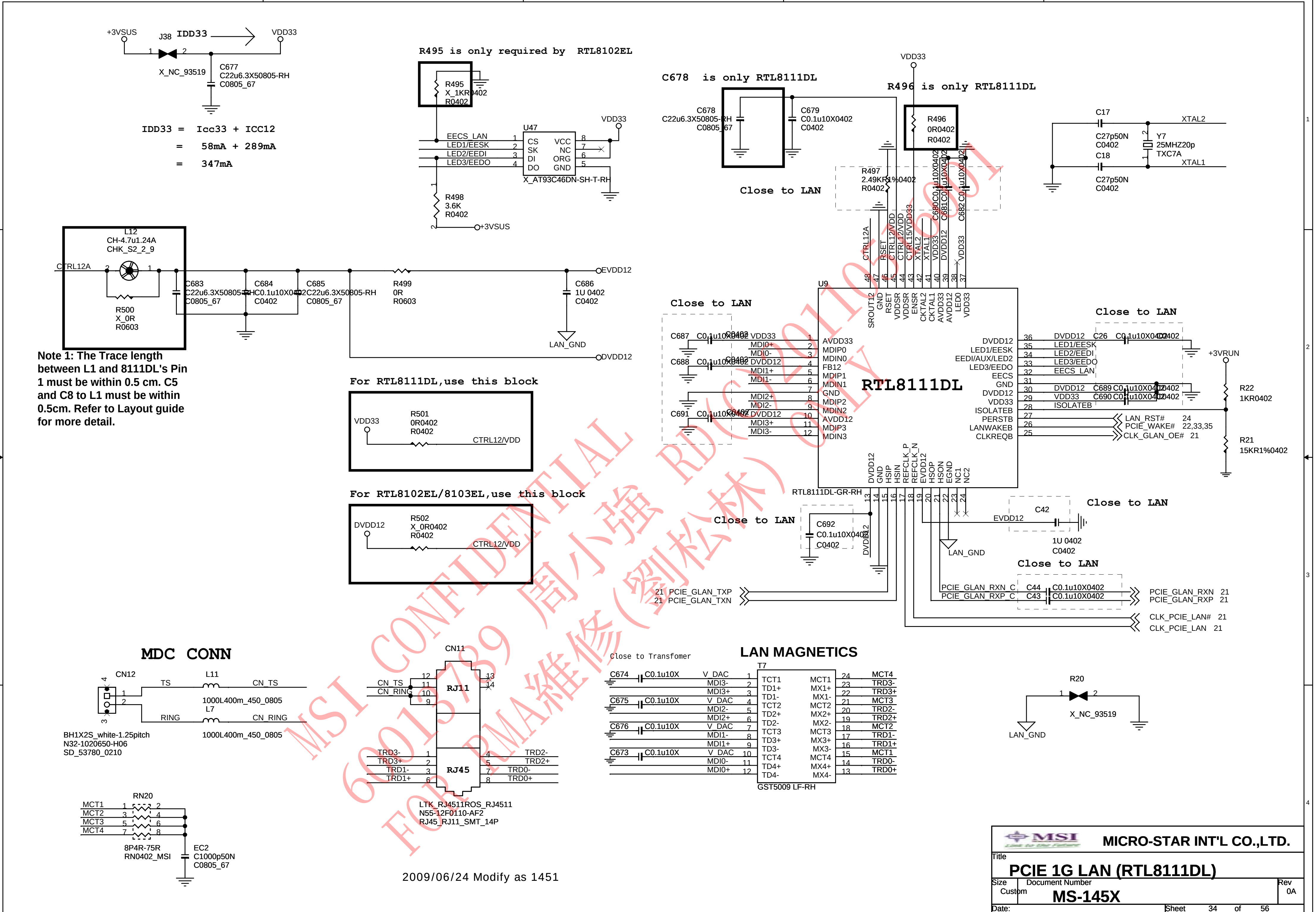
	LED7 SW7	LED8 SW8	LED9 SW9	LED10 SW10
1453	Stuff	Nostuff	Discreate	UMA
1454	Stuff	Nostuff	P1	IE
OEM	Stuff	P1	Wireless	Camera

MSI CORPORATION

Title: MINIPCIE,CAMERA,BLUETOOTH,SW

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 33 of 56



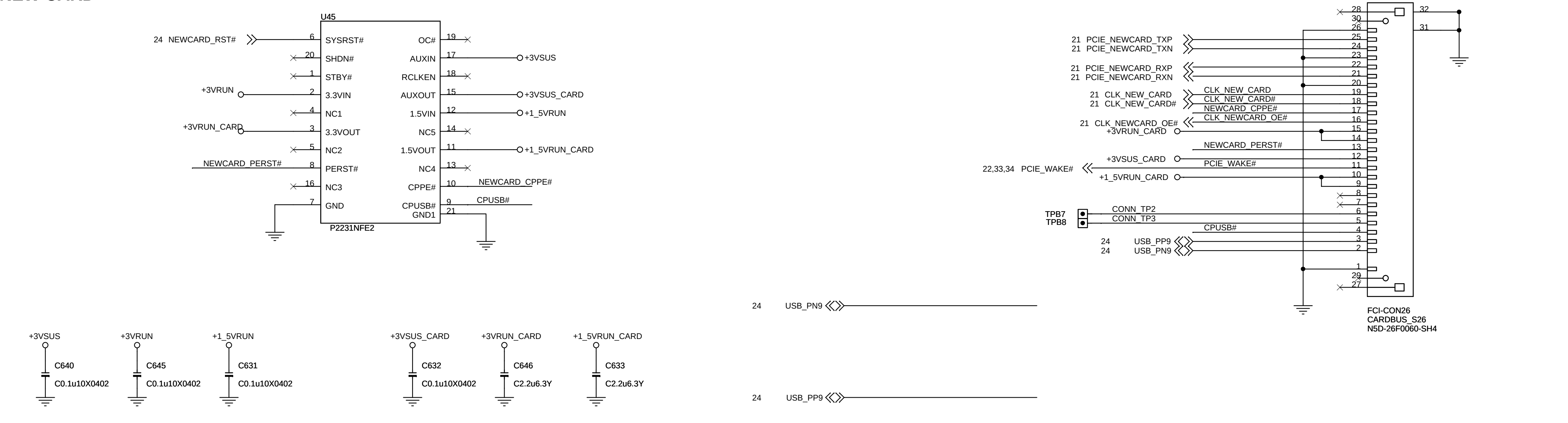
MICRO-STAR INT'L CO.,LTD.

Title: PCIE 1G LAN (RTL8111DL)

Size: Custom | Document Number: MS-145X | Rev: 0A

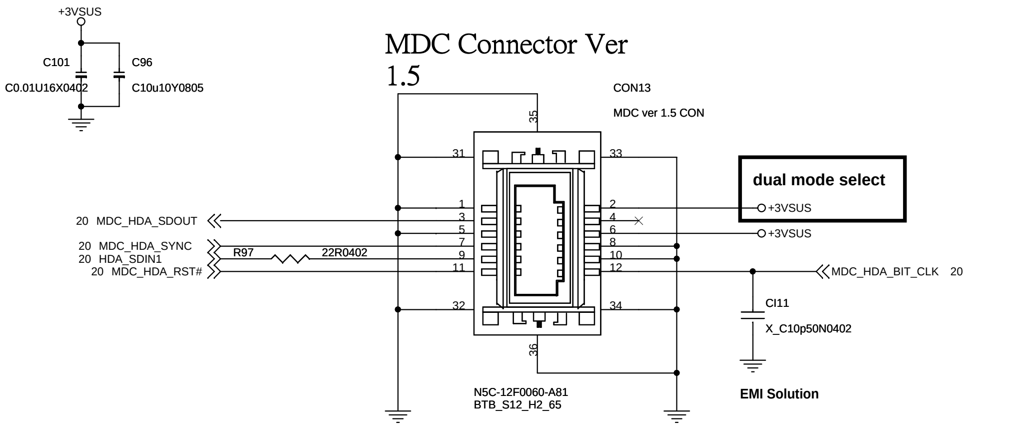
Date: | Sheet 34 of 56

NEW CARD



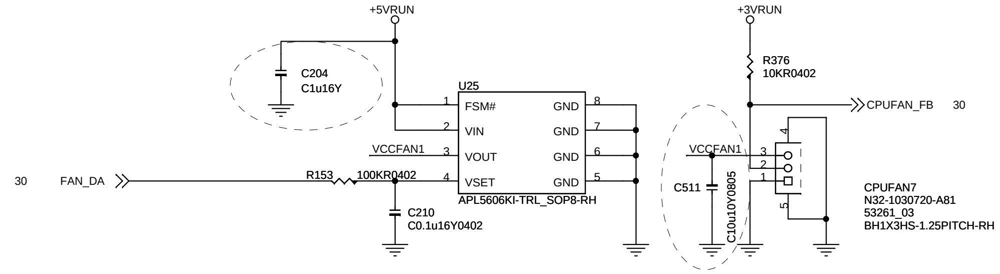
2009/06/26 Reserved by EMI

MDC Connector



2009/07/14 因限高問題,改回1451用料N5C-12F0060-A81

CPU FAN



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	NEWCARD,FAN	
Size: Custom	Document Number: MS-145X	Rev: 0A
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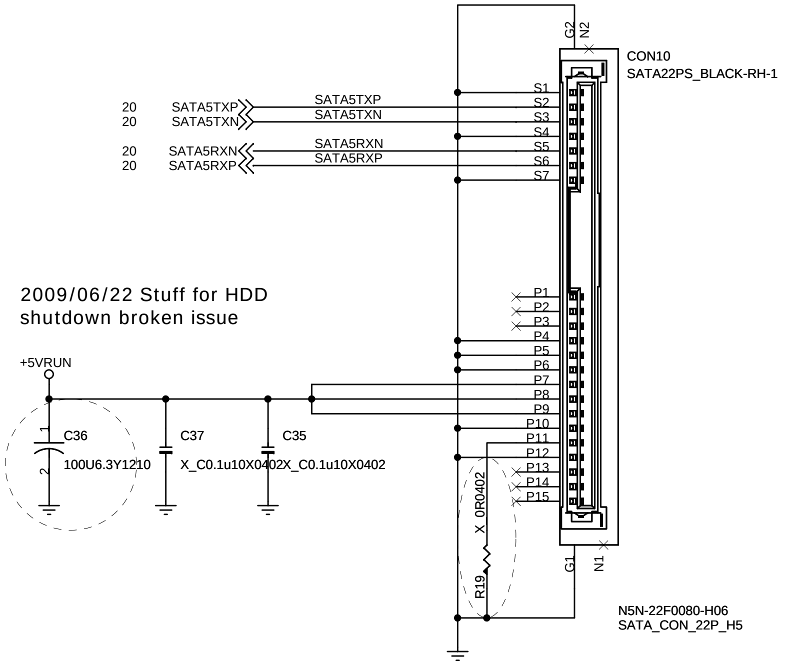
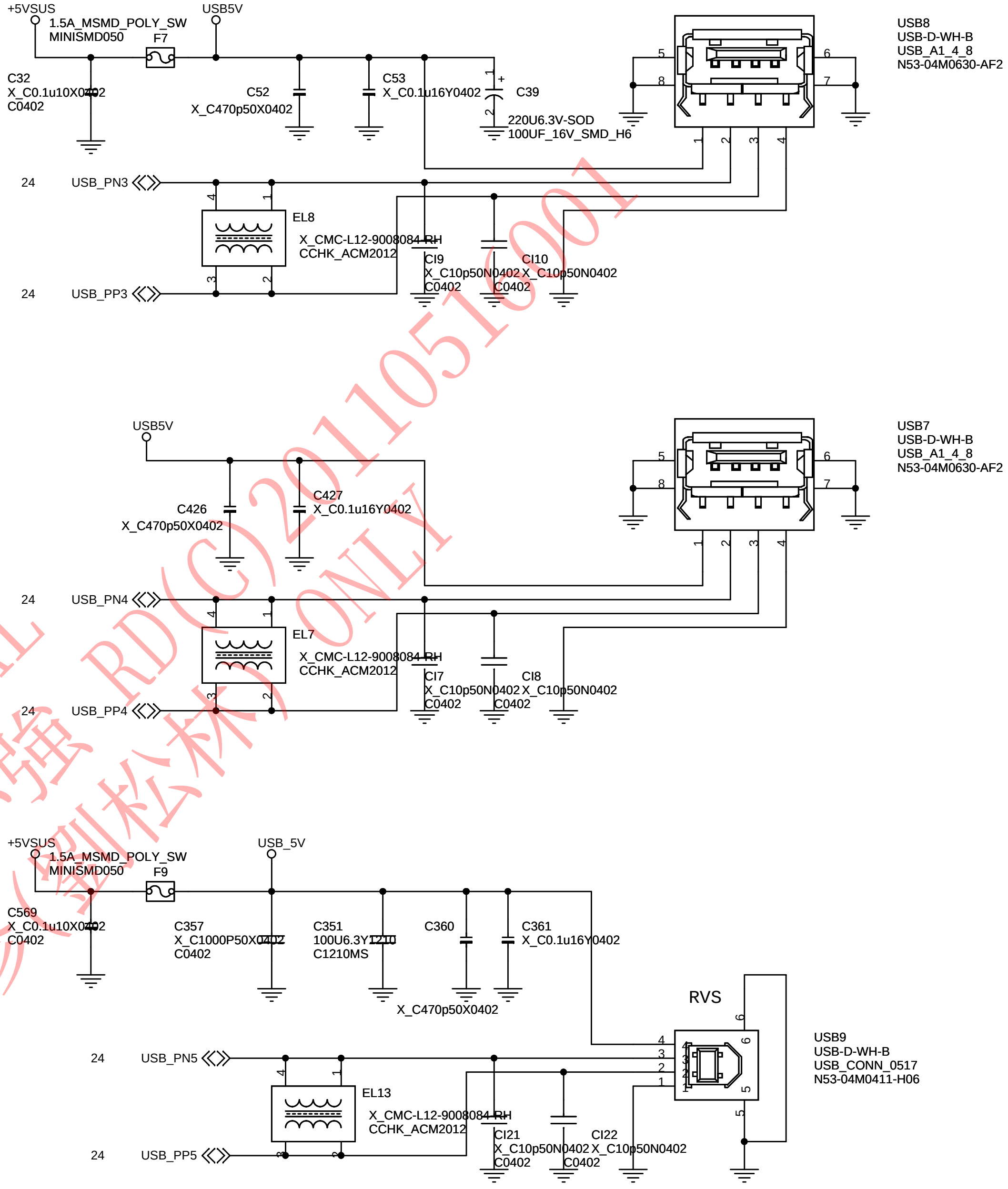
SATA HDD



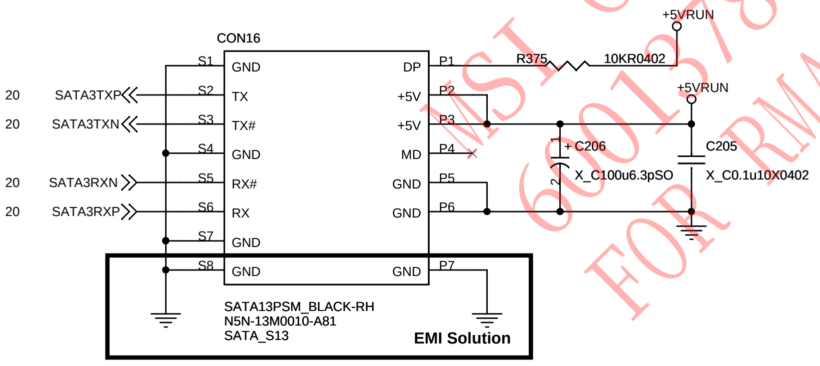
2009/06/22 SATA HDD P11 is Staggered Spinup function

Staggered Spinup :

如果**system** 支援這個功能,開機時 **HDD** 的馬達是不轉的,
BIOS 必須下**command** 把 **HDD wake up**,才能做偵測**HDD**的動作
如果不支援**Staggered Spinup** 這個**function** 這隻腳必須接地



SATA ODD



2009/07/07 USB common choke先不上

MSI	MICRO-STAR INT'L CO.,LTD.
Title	HDD,CDROM,USB
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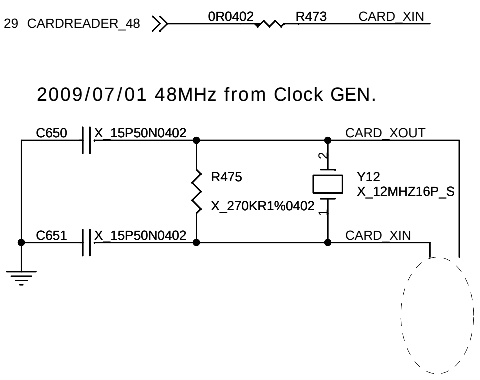
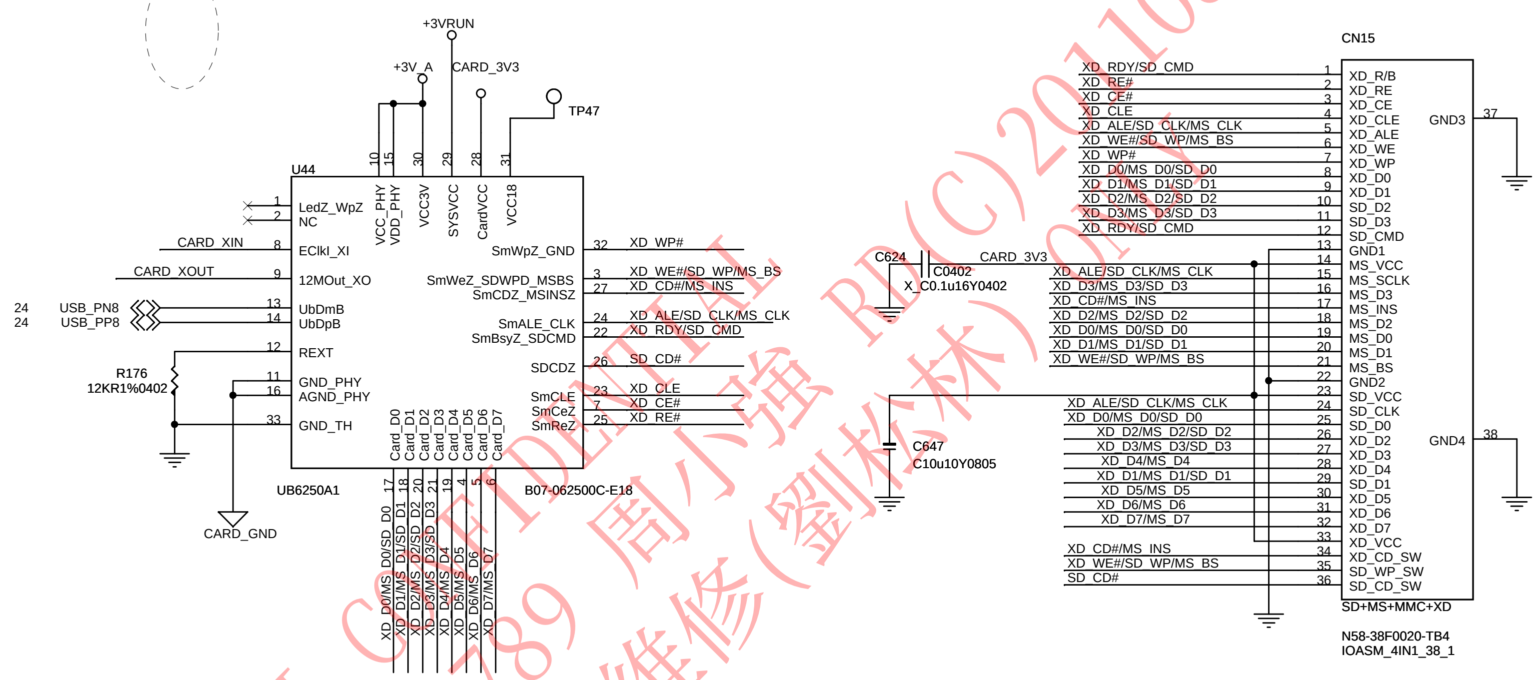
ENE UB6250 USB20 Flash Card Reader Controller
Pins for SD, MMC, MS, and xD memory cards

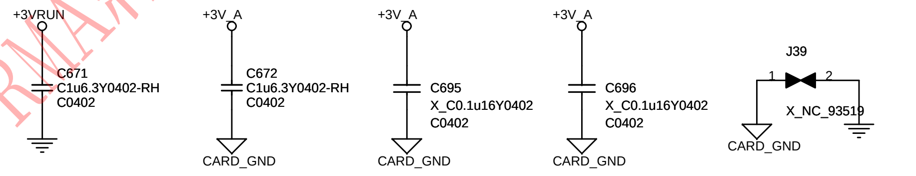
Name	No	I/O	XD	SD	MMC	MS
xDCeZ	7	O	xD card EN			
xDCle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDBsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SdCdZ	26	I		SD CD	MMC CD	
xDCdZ	27	I	xD CD			MS CD

2009/07/01 48MHz from Clock GEN.





CLOCK frequency can vary
lie on strap pin config(pin7&pin25)



Configurations for Clock Source Selection:

4.7K Pull-high Resistor on		Frequency of external clock source to EClkin pin
xDReZ	xDCeZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

MICRO-STAR INT'L CO.,LTD.

Title: CARD_READER (RTS5159)

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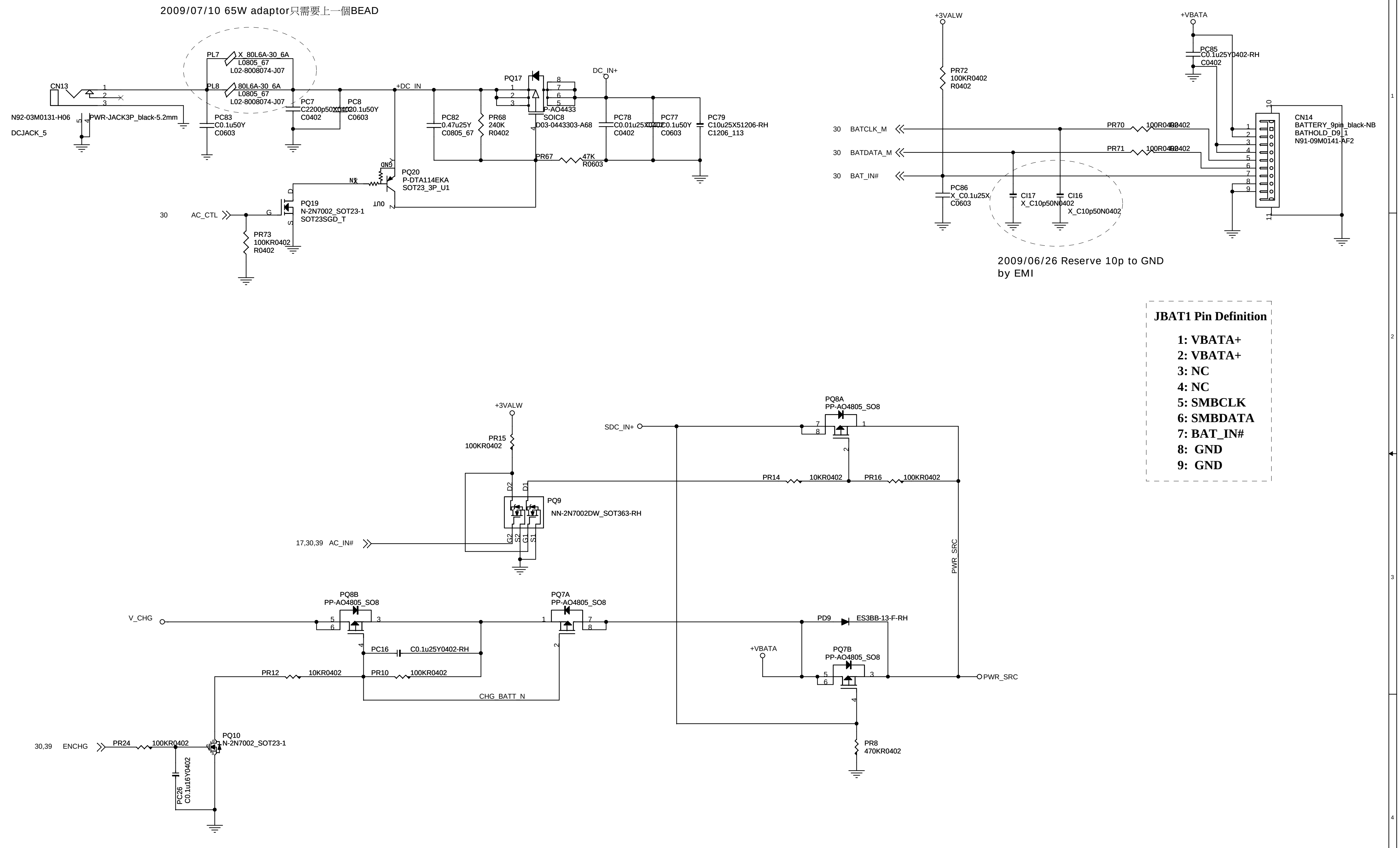


JBAT1 Pin Definition

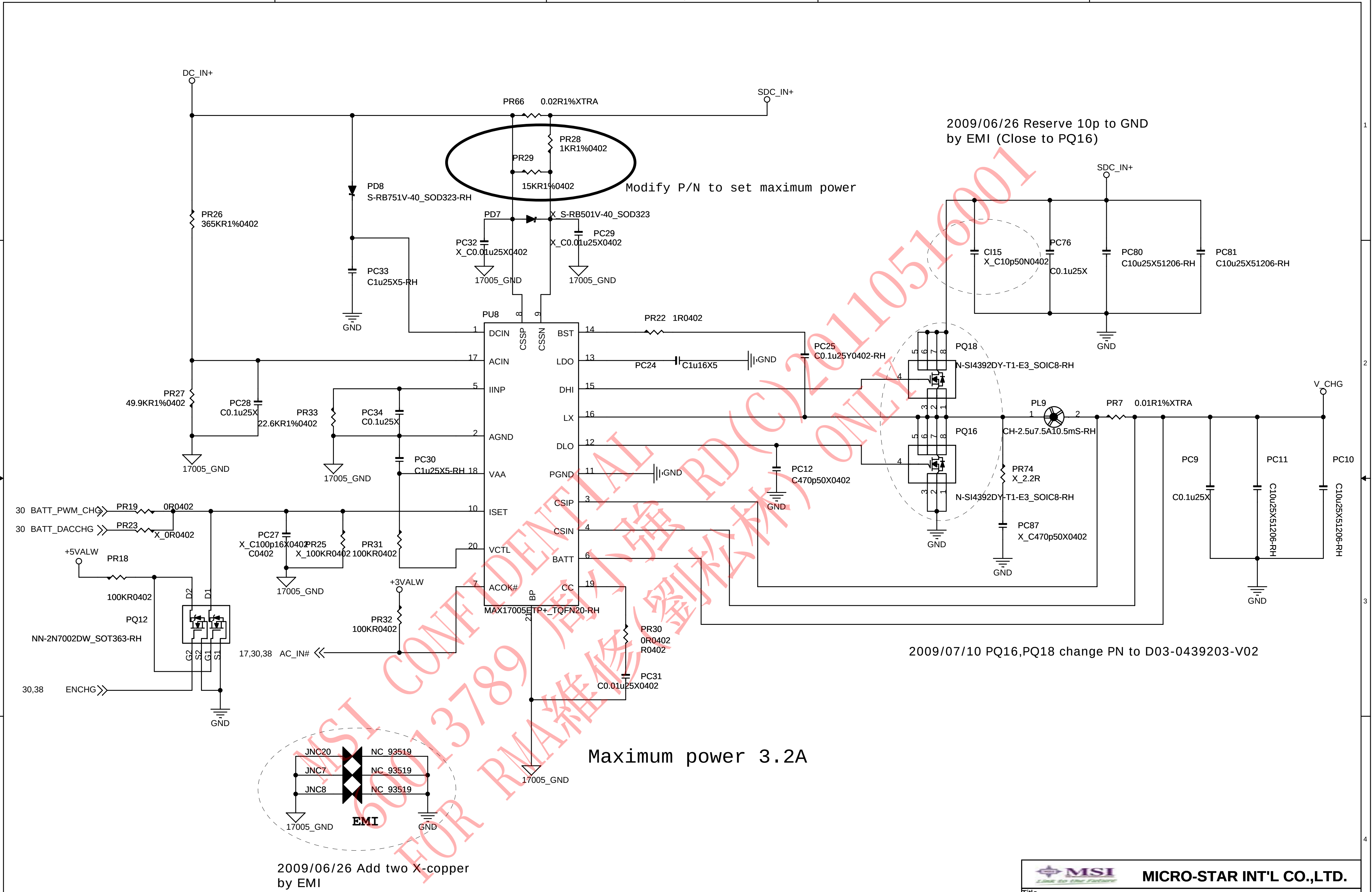
1: VBATA+
2: VBATA+
3: NC
4: NC
5: SMBCLK
6: SMBDATA
7: BAT_IN#
8: GND
9: GND

MICRO-STAR INT'L CO.,LTD.

Title: **Battery Select**

Size: Custom | Document Number: **MS-145X** | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 38 of 56

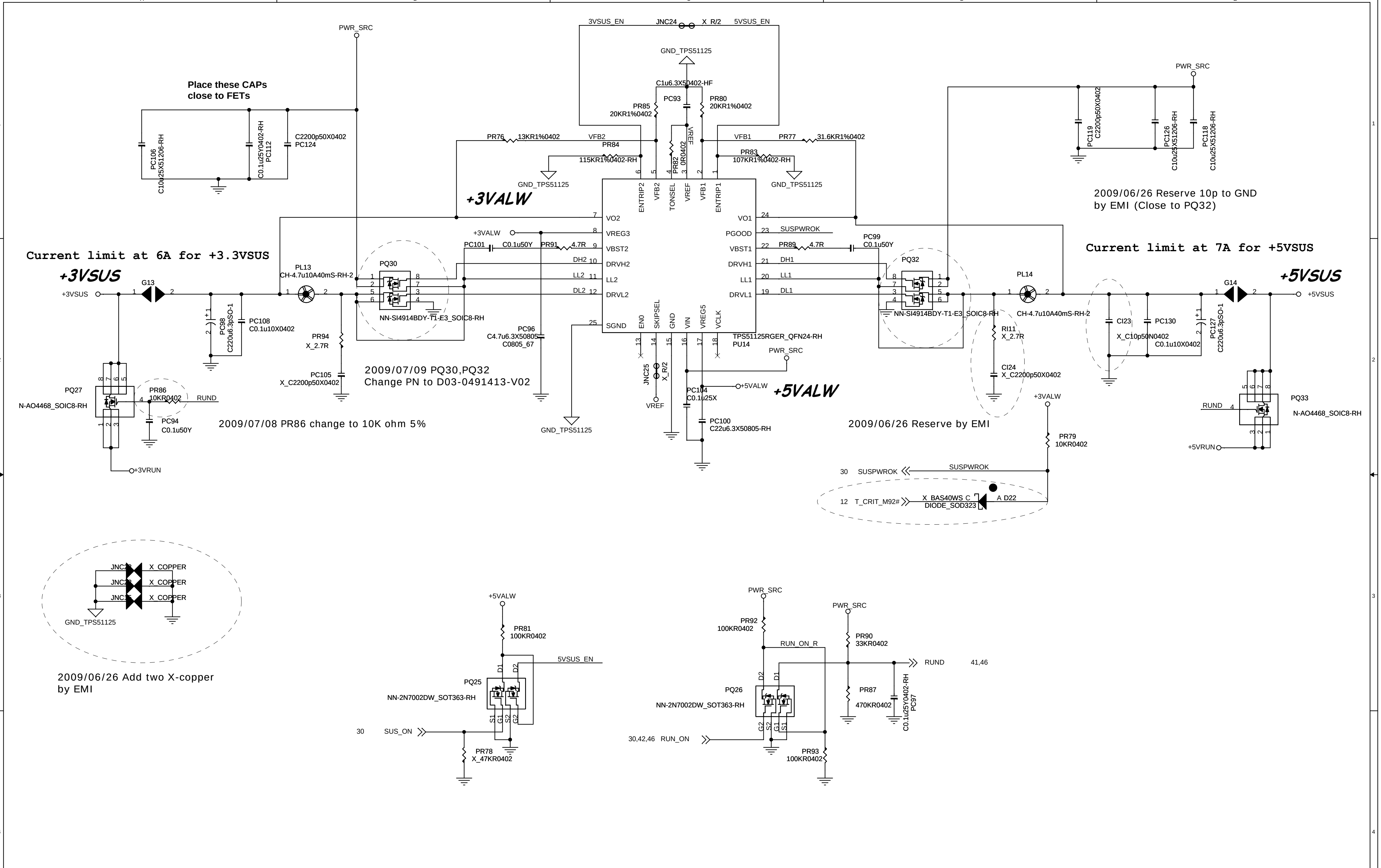


MICRO-STAR INT'L CO.,LTD.

Title: **Battery Charger**

Size	Document Number	Rev
Custom	MS-145X	0A

Date: Wednesday, August 05, 2009 — Sheet 39 of 56



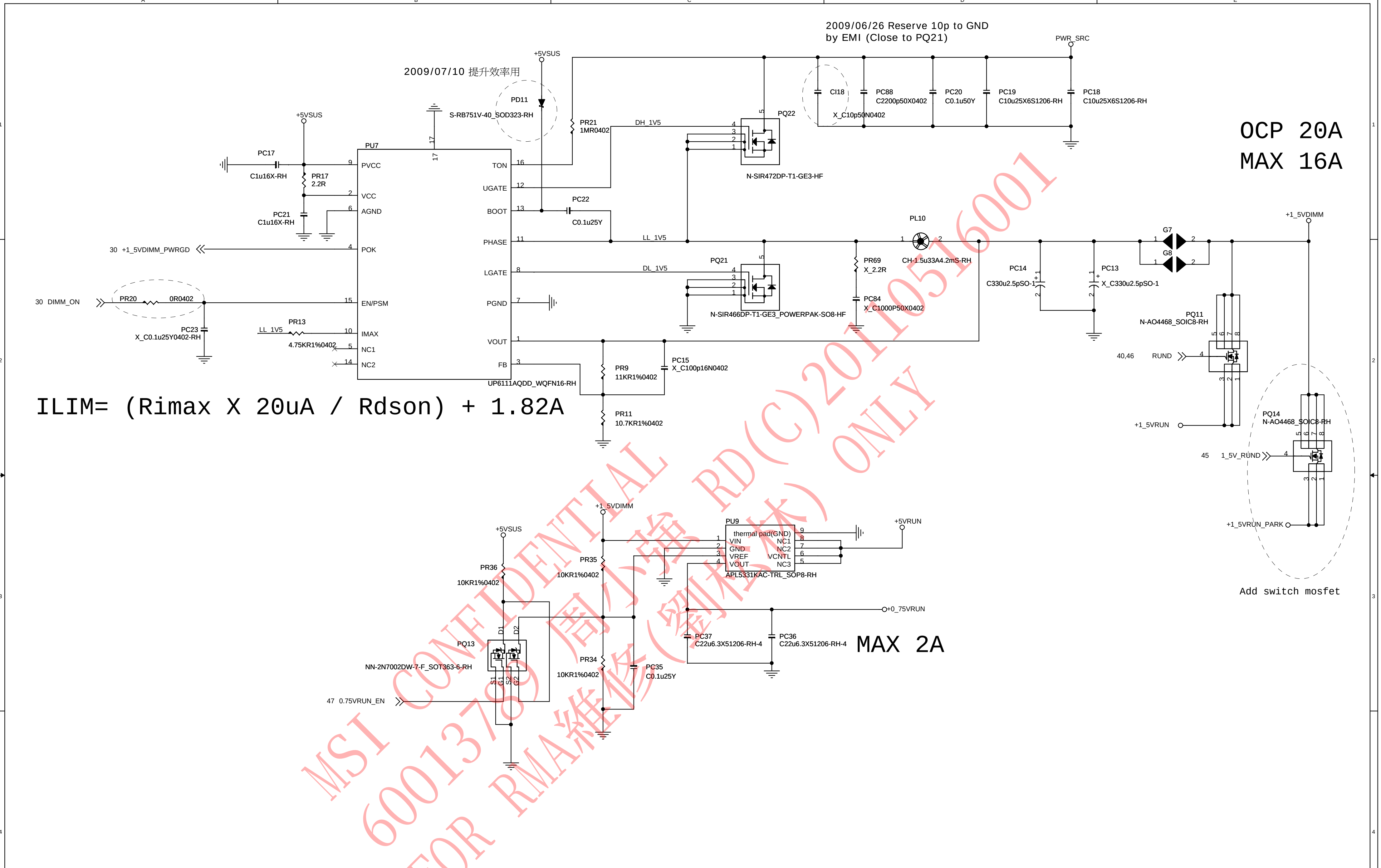
MICRO-STAR INT'L CO.,LTD.

Title

System power

Size	Document Number	Rev
Custom	**MS-145X**	0A

Date: Wednesday, August 05, 2009 Sheet 40 of 56



MICRO-STAR INT'L CO.,LTD.

Title: SMDDR_VTERM /1_5VRUN

Size	Document Number	Rev
Custom	MS-145X	0A

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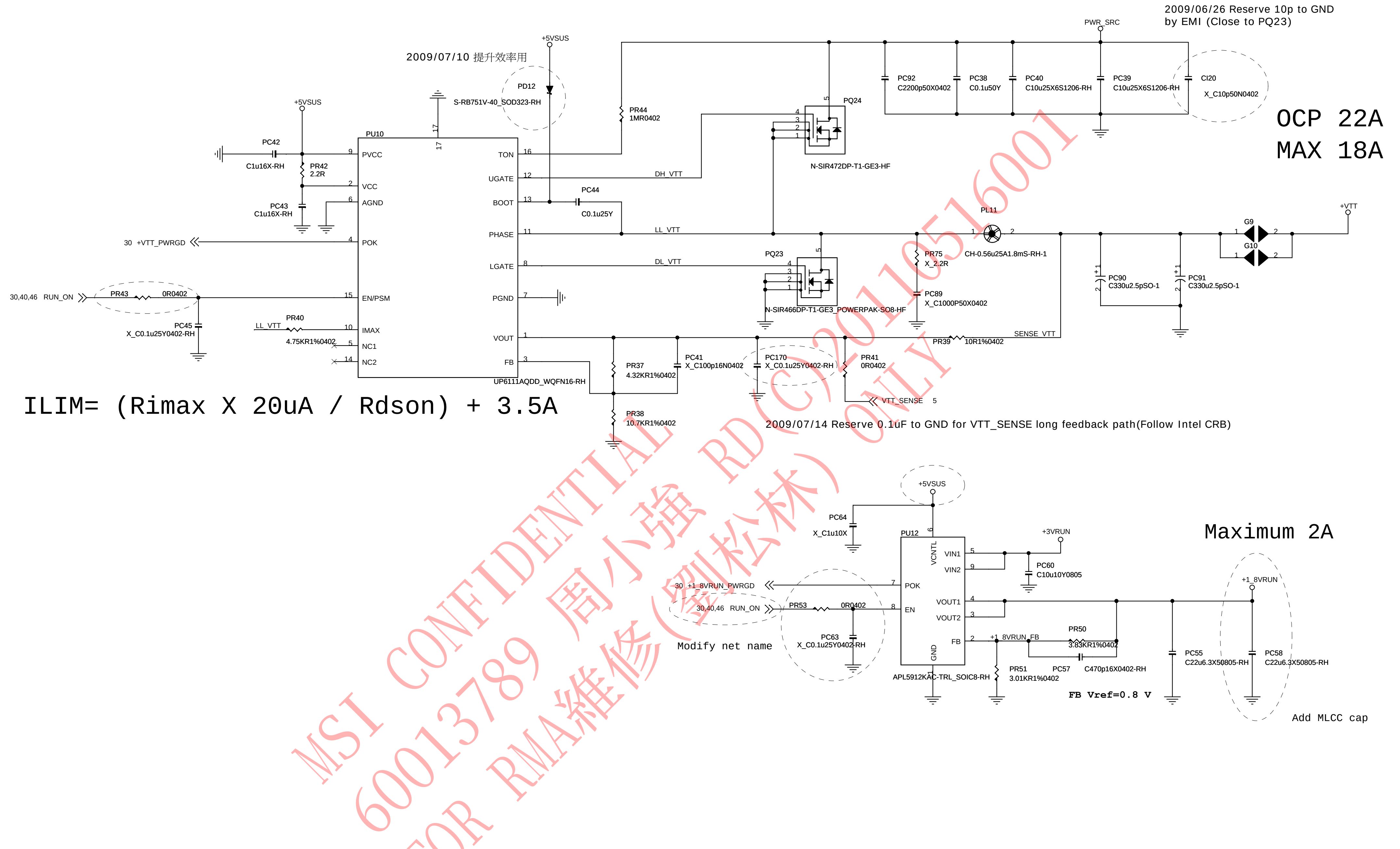
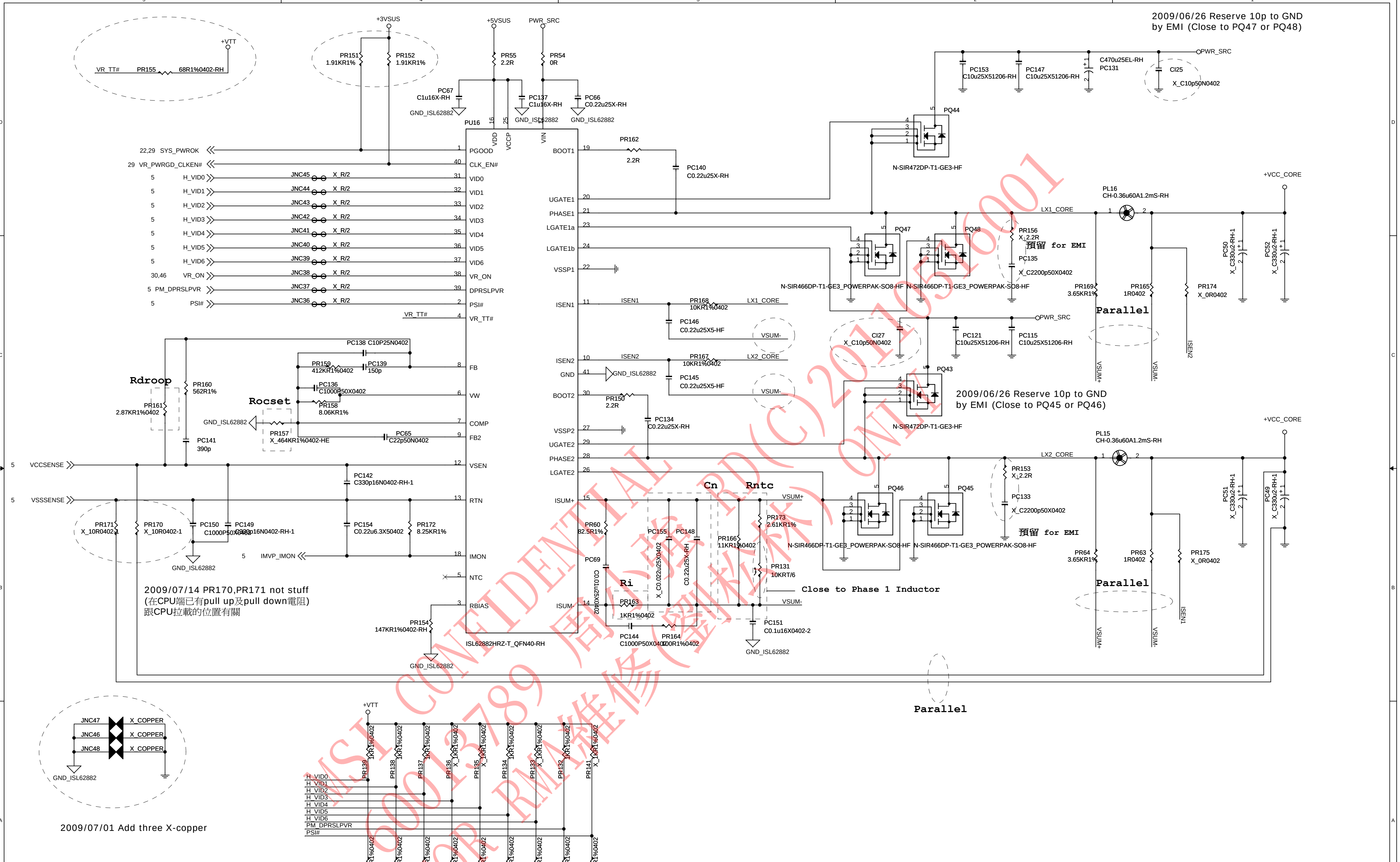


MICRO-STAR INT'L CO.,LTD.

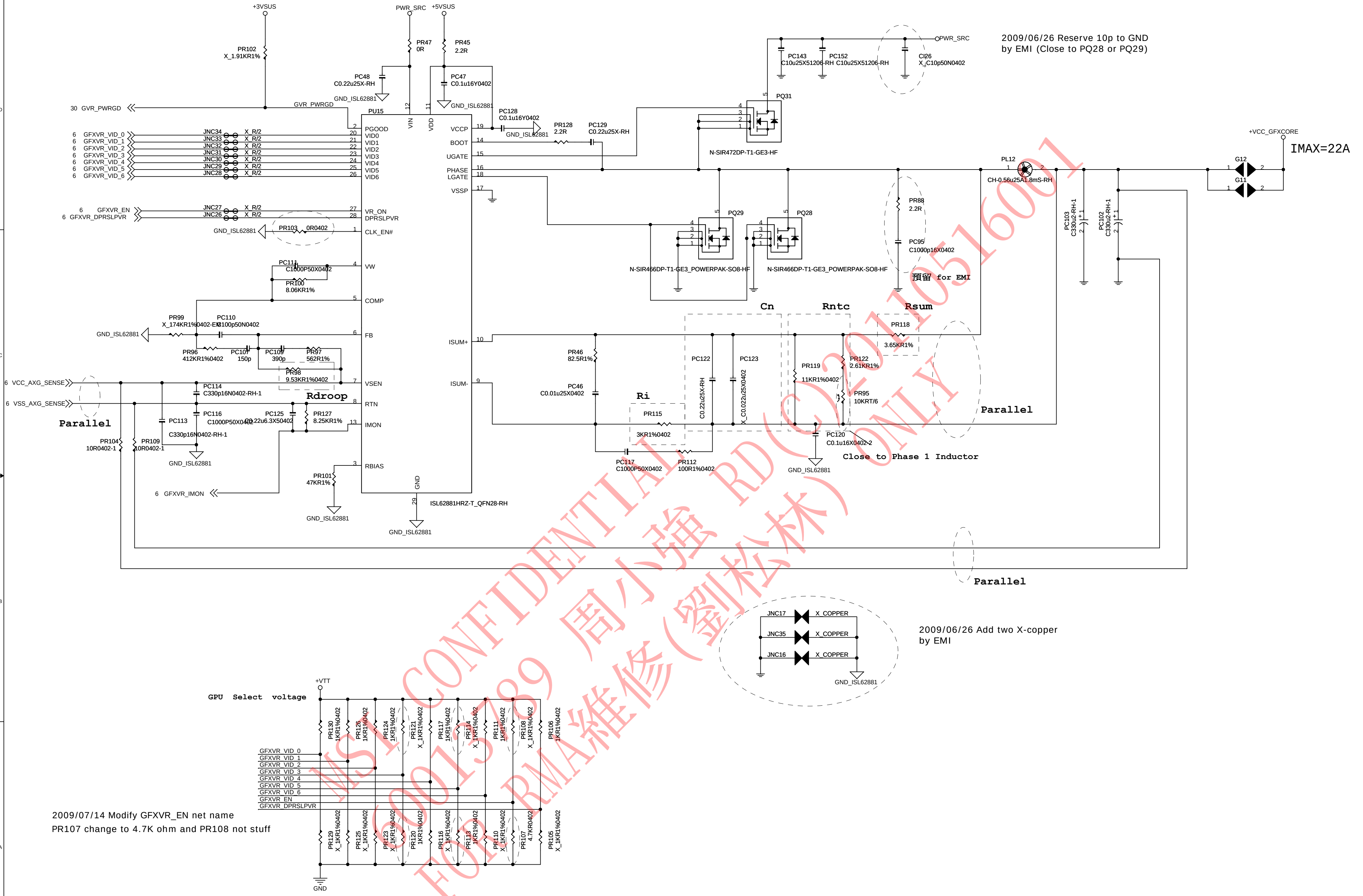
Title: VTT Power,+1.8VRUN

Size	Document Number	Rev
Custom	MS-145X	0A

Date: Wednesday, August 05, 2009 — Sheet 42 of 56



MSI CORPORATION			
Title	CPU Power		
Size: Custom	Document Number: MS-145X		Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 43 of 56		

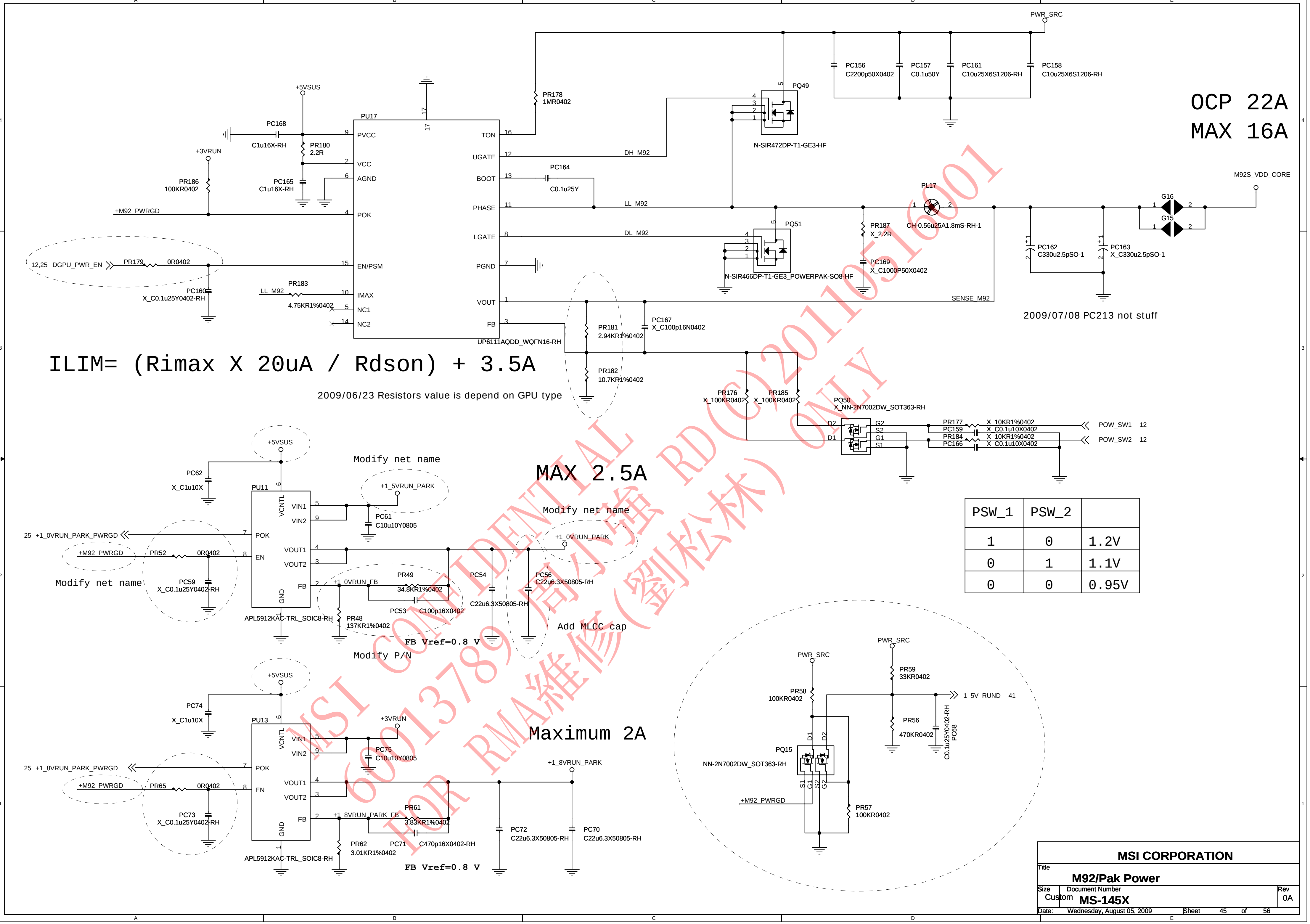


2009/06/26 Reserve 10p to GND
by EMI (Close to PQ28 or PQ29)

2009/06/26 Add two X-copper
by EMI

2009/07/14 Modify GFXVR_EN net name
PR107 change to 4.7K ohm and PR108 not stuff

MSI CORPORATION	
Title	Graphic Core
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 44 of 56



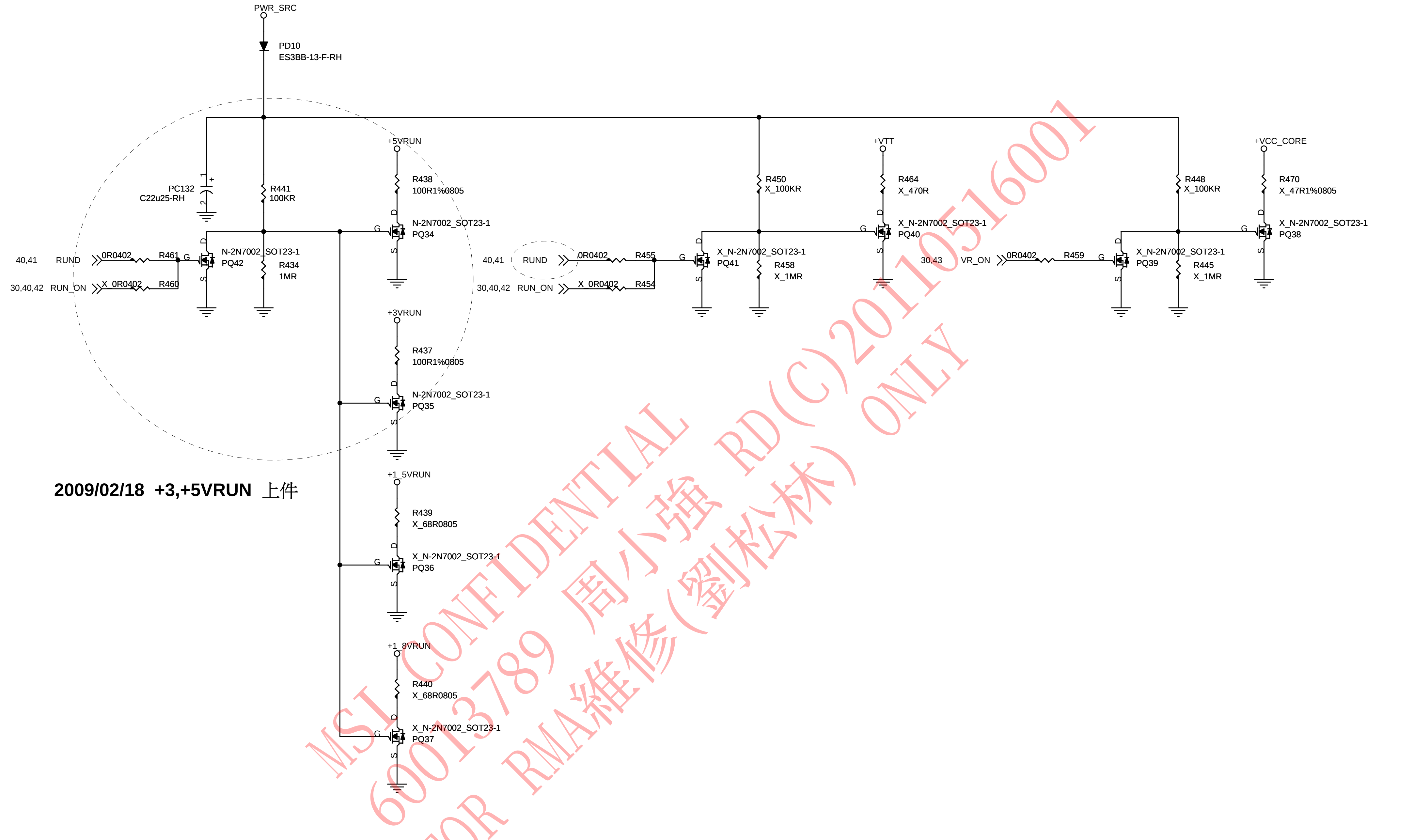
PSW_1	PSW_2	
1	0	1.2V
0	1	1.1V
0	0	0.95V

MSI CORPORATION

Title: **M92/Pak Power**

Size: Custom | Document Number: **MS-145X** | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 45 of 56

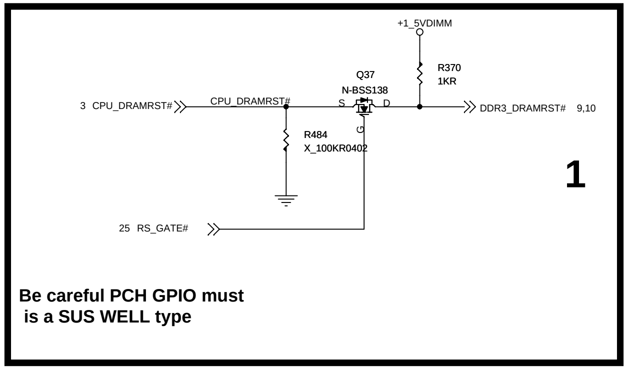


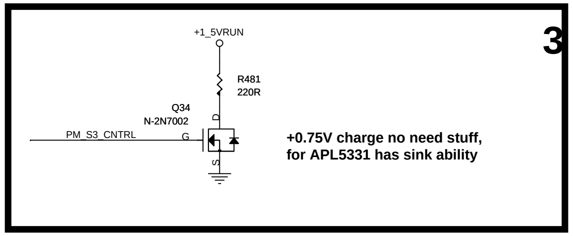
MICRO-STAR INT'L CO.,LTD.

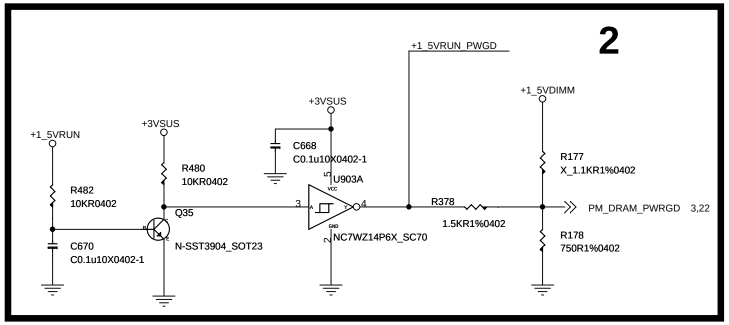
Title: **Discharge Circuits**

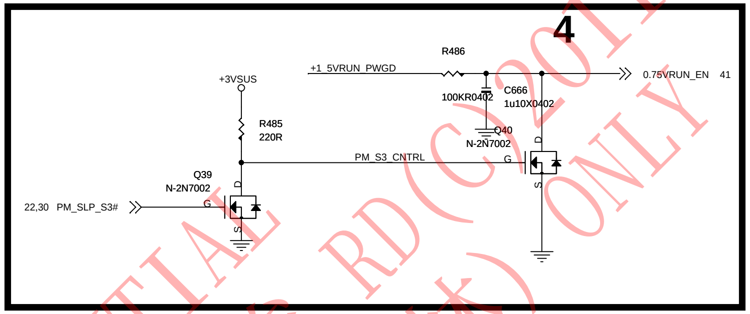
Size	Document Number	Rev
Custom	MS-145X	0A

Date: Wednesday, August 05, 2009 — Sheet 46 of 56







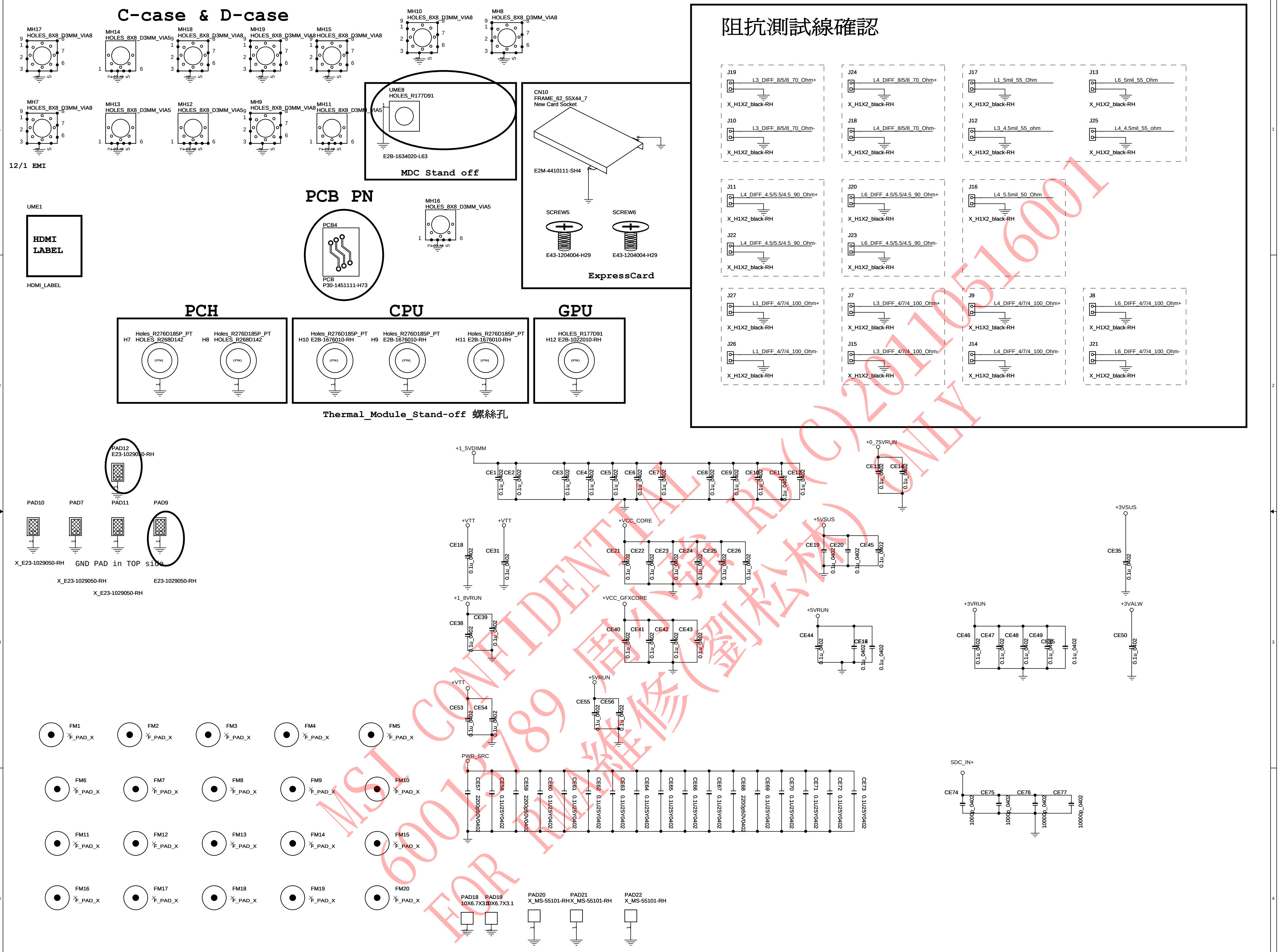


MICRO-STAR INT'L CO.,LTD.

Title: **INTEL S3 POWER**

Size	Document Number	Rev
Custom	MS-145X	0A

Date: Wednesday, August 05, 2009 Sheet 47 of 56



MICRO-STAR INT'L CO.,LTD.

Title	Screw/EMI	
Size Custom	Document Number MS-145X	Rev 0A
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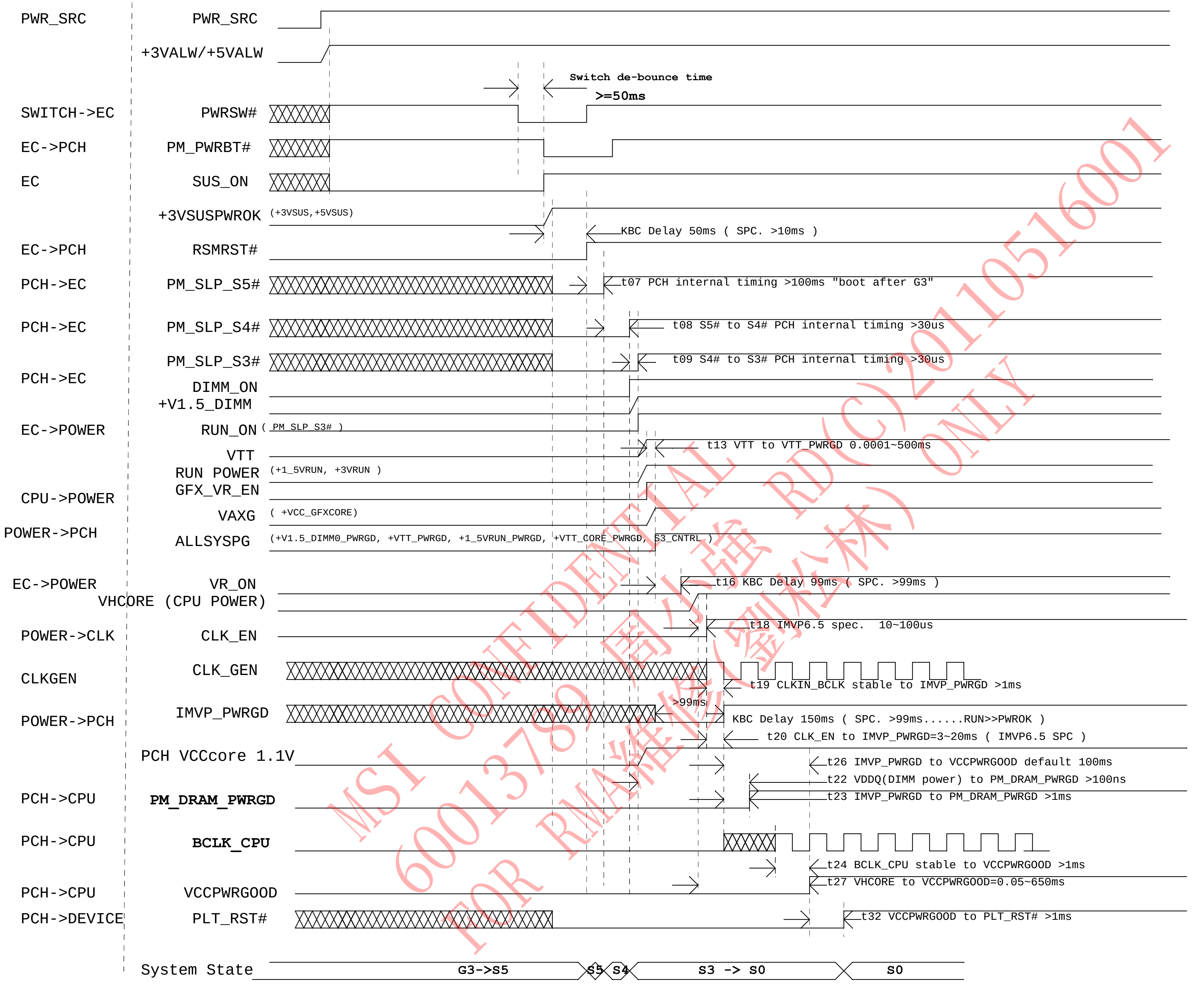
Calpella System Power on Sequence DC mode



MICRO-STAR INT'L CO.,LTD.

Title
Power on Sequency

Size	Document Number	Rev
Custom	MS-145X	0A

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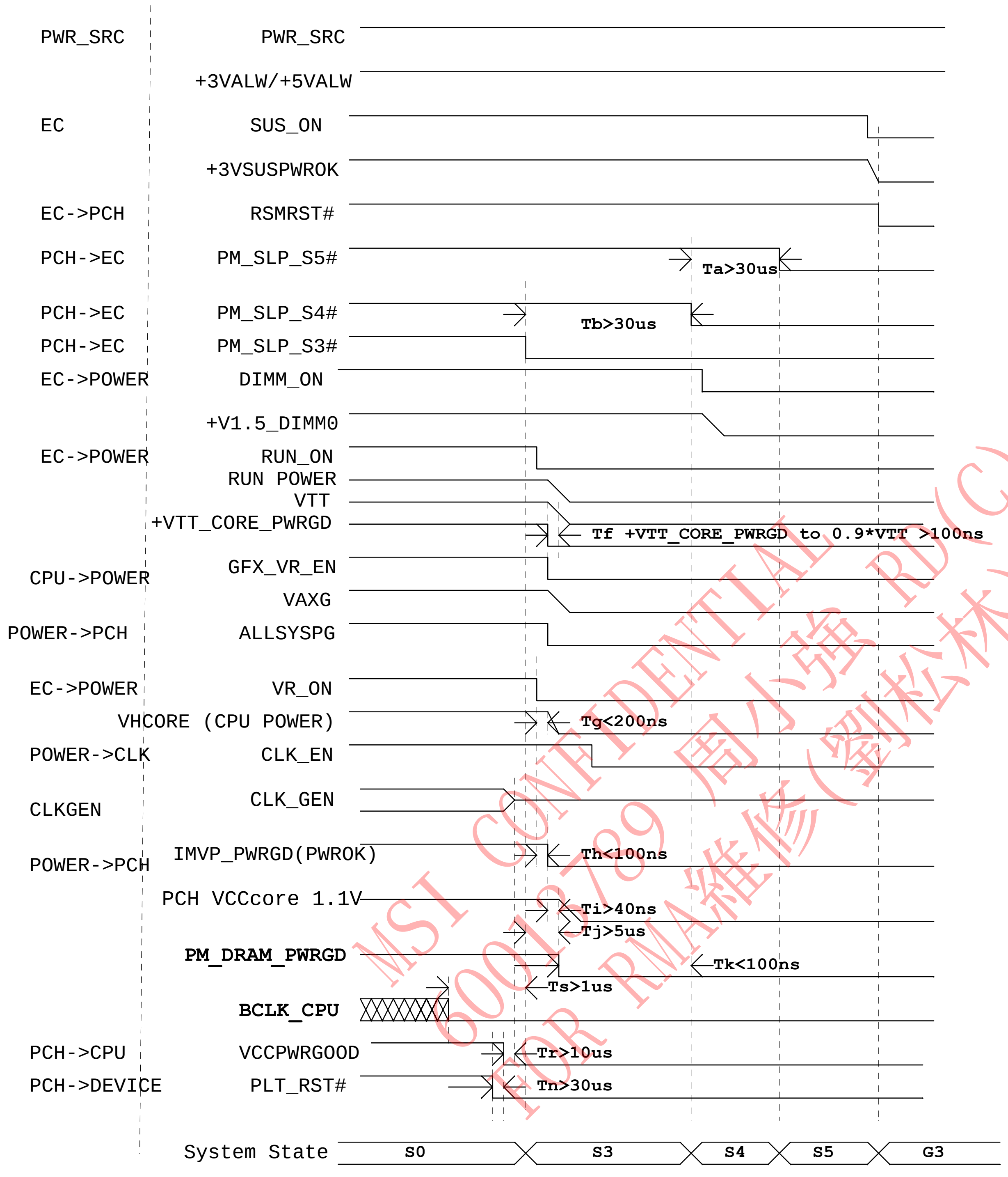
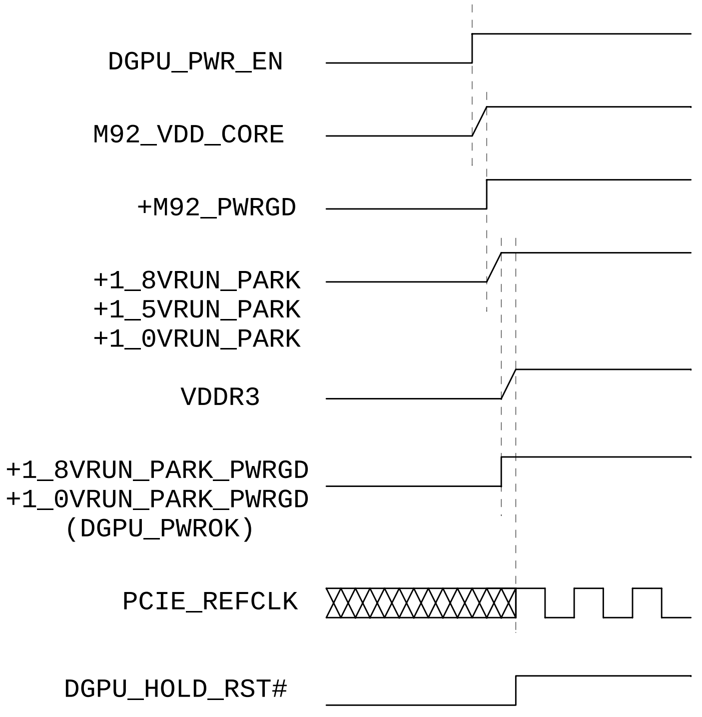
Power down Sequence DC mode S0 to G3



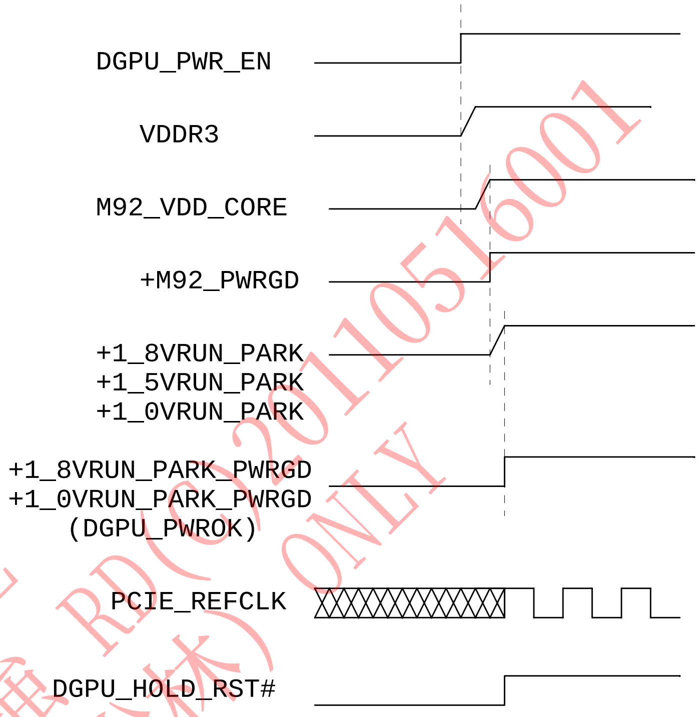
MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequency		
Size: A3	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 50 of 56	

M92 Power on Sequence



PARK Power on Sequence



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	M92/PARK Power on Sequence		
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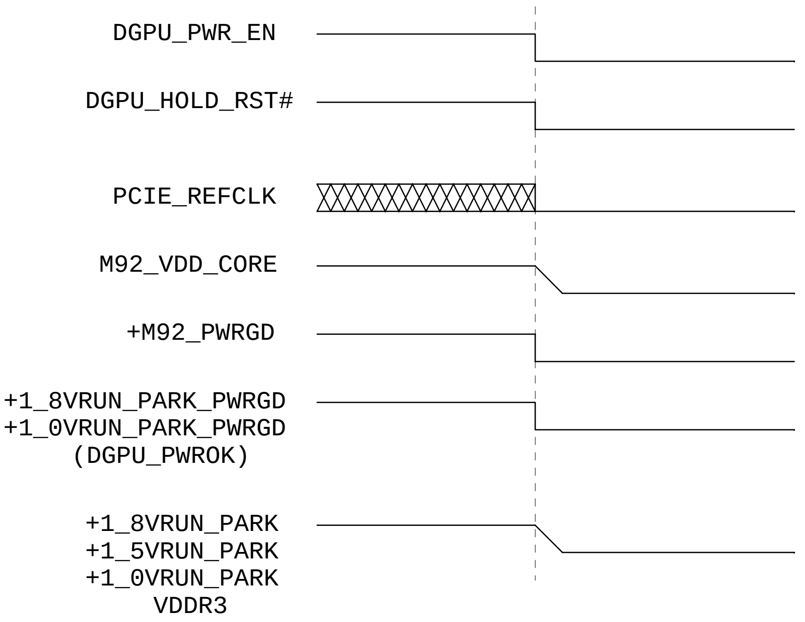
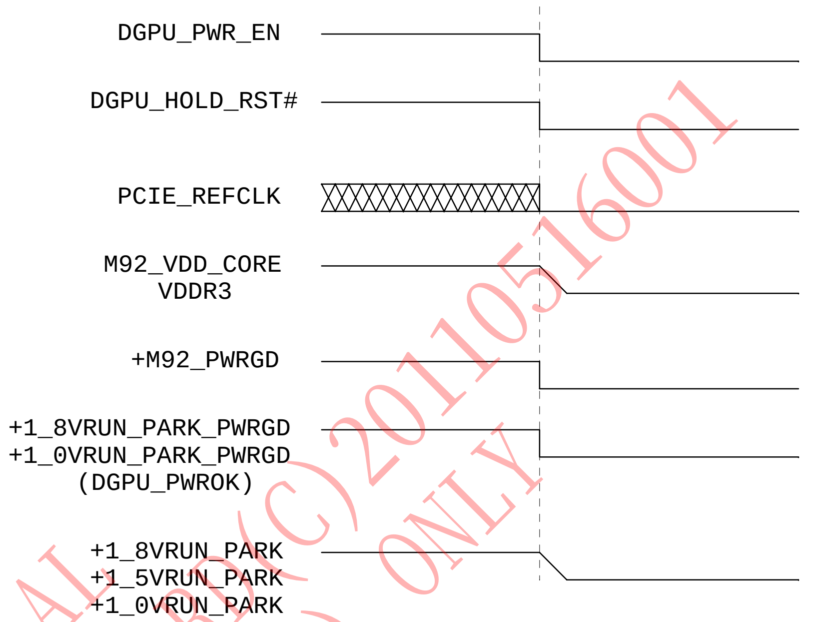
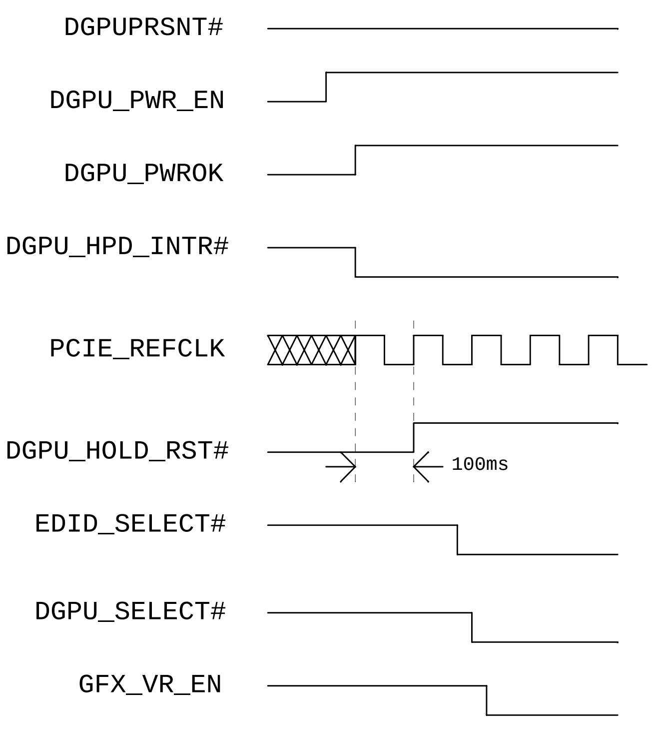
M92 Power down Sequence



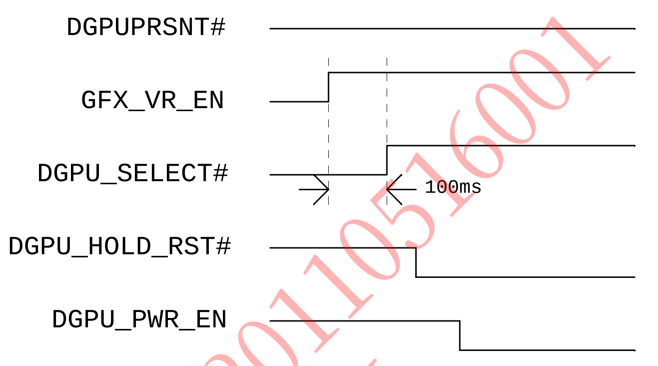
PARK Power down Sequence



Switchable DGPU Power on Sequence
Discrete Mode



Switchable DGPU Power off Sequence
UMA Mode



MICRO-STAR INT'L CO.,LTD.		
Title: Switchable Power Sequence		
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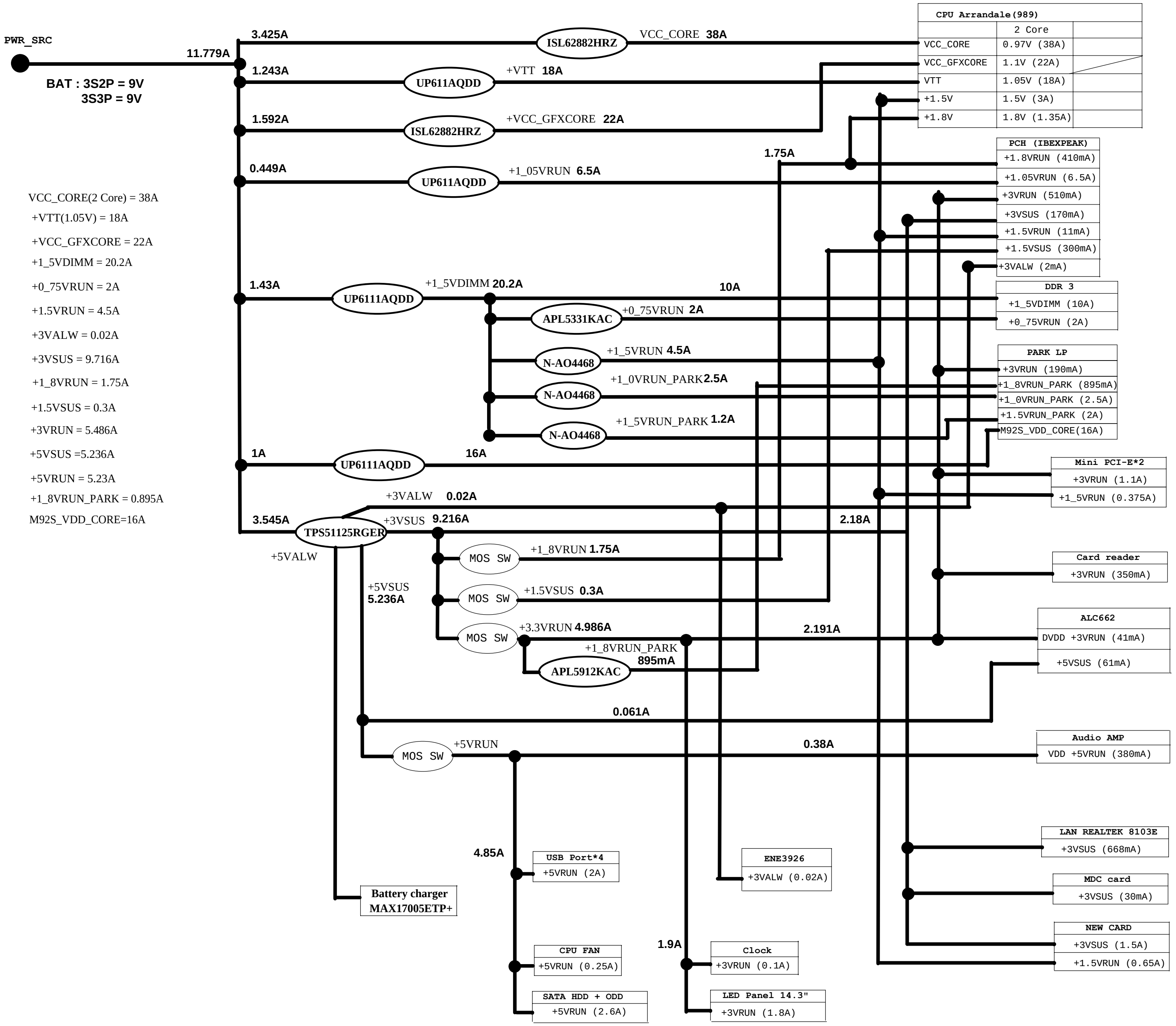

MICRO-STAR INT'L CO.,LTD.		
Title: Power MAP		
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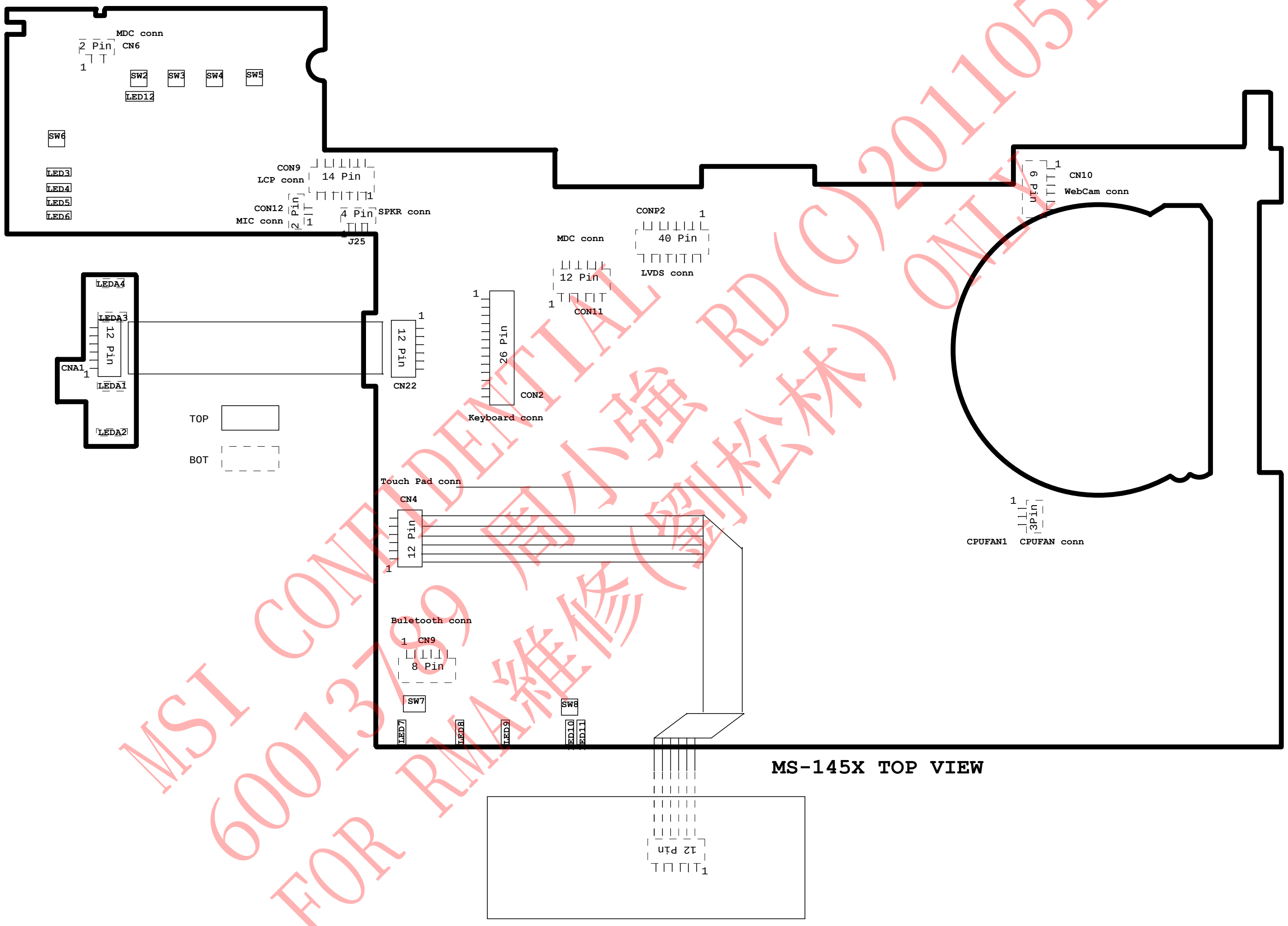
MS-145X	
SW2	Power_button(FOR OEM)
SW3	HotKeyP1_button(FOR OEM)
SW4	WLAN/BT_button(FOR OEM)
SW5	Search/Webcam_button (FOR OEM)
SW6	Power_button(FOR Channel)
SW7	Right_button
SW8	Left_button

MS-145X	
LED3	HDD LED(FOR OEM)
LED4	NUM_LED(FOR OEM)
LED5	CAP_LED(FOR OEM)
LED6	SCR_LED (FOR OEM)
LED7	BT_LED
LED8	WLAN_LED
LED9	ACPI_LED
LED10	CHARGE_LED
LED11	BATTERY_LOW_LED
LED12	POWER_LED

MS-145XA	
LEDA1	NUM_LED(FOR OEM)
LEDA2	HDD_LED(FOR OEM)
LEDA3	CAP_LED(FOR OEM)
LEDA4	SCR_LED (FOR OEM)



MS-145X : Main Board
MS-145XA : LED board

MICRO-STAR INT'L CO.,LTD.

Title	Topology		
Size: Custom	Document Number: MS-145X		Rev: 0A
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2009/06/25 [Page33] Add LED and switch function for OEM reserved
[Page30] Delete KBOUT16,KBOUT17 for MS-1451 keyboard matrix
[Page41/42] Modify APL5912 VCNTL to +5VSUS
[Page43/44] Modify some RC footprint and value

2009/06/26 Modify circuit to Switchable
[Page19] Add LVDS common choke by EMI
[Page12] Reserve RGB 10p to GND
[Page38] Reserve BAT CLK and DATA 10p to GND
[Page39] Reserve 10p SDC_IN+ to GND and close to PQ57
Add two X-Copper
[Page40] Reserve 10p +5VSUS to GND and close to PQ60
Reserve 2.2R+2200p
[Page41] Reserve 10p PWR_SRC to GND and close to PQ68
[Page42] Reserve 10p PWR_SRC to GND and close to PQ72
[Page43] Reserve 10p PWR_SRC to GND and close to PQ75 or PQ76
Reserve 10p PWR_SRC to GND and close to PQ78 or PQ79
[Page43] Reserve 10p PWR_SRC to GND and close to PQ81 or PQ82
Add two X-Copper

2009/06/29 [Page35] Modify CPU FAN.Add C121 and C304 by datasheet.Add one more RC for FAN speed calculation(as MS-1122)
Modify PARK circuit
Modify PCH PN to OB1-1675001 for Mobile IntelR 5 Series Chipset Full Feature
Modify Audio jack PN to N54-05F0951-H06
Modify internal MIC PN to N32-1020790-A81
Modify power sequence map

2009/07/01 [Page3] R234,R412等0A實驗結果再決定是否移除
BPM#[0~7] remove
BCLK只保留from PCH,移除from CLOCK GEN.

[Page5] Short bead

[Page6] Short bead

[Page7] VSS_NCTF1~7 remove

[Page8] 只保留CFG的測點,其餘移除

[Page9] SA0_DIM0及SA1_DIM0改爲0 ohm對地

移除330uF,因在CPU以及switching power端已有

[Page10] SA0_DIM1改爲0 ohm對地

移除330uF,因在CPU以及switching power端已有

[Page12] 補上HPD線路

[Page16] MDA0~MDA7 swap

[Page18] CRT及LVDS的預留電阻(for MS-1454)均改爲單顆的0 ohm

EDID switch的電源pin加上0.1uF

R3238,R3239改爲10K ohm

移除BR-AD-ADJ,BR-PWM-ADJ名稱改爲PWM-ADJ,HDMI DDC名稱改爲HDM_SDA及HDM_SCL

[Page19] 兀型濾波LC値改爲0.1uH+10pF

新增LVDS DDC pull high,backlight adj預留net PWM-ADJ

[Page25] DGPUPRSNT#改接pull down

[Page30] 修改+1_8VRUN_PARK_PWRGD及+1_0VRUN_PARK_PWRGD結合爲DGPU_PWROK

[Page34] C47,C49改爲0.1uF

[Page43] Add three X-copper