South Peak 15" Schematics

Tiger Lake-UP3

2020-04-24

REV:SB

Multi

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Title	Cover Page	
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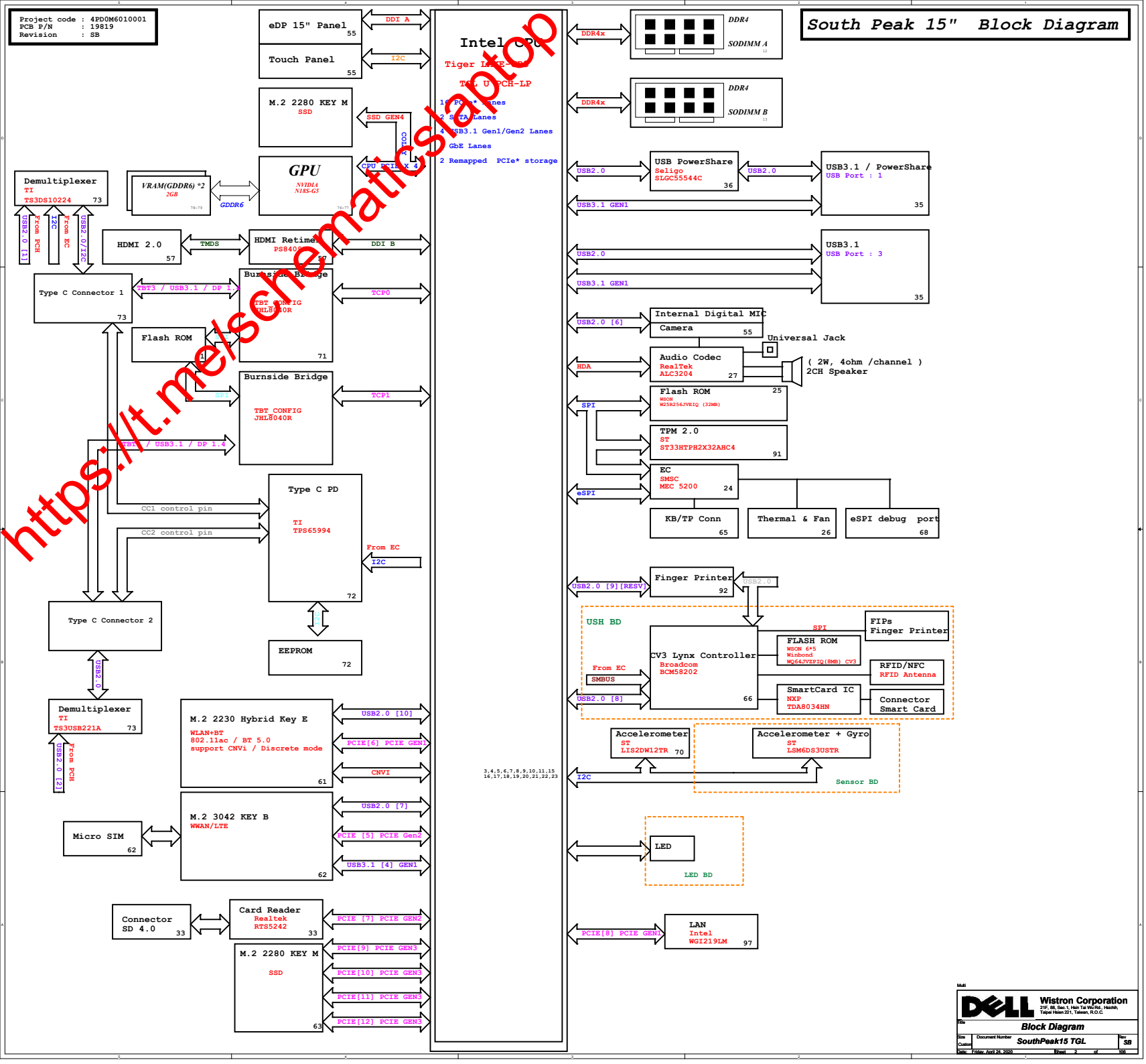

Main Func = CPU

24 PECI_CPU
22,24 PROCHOT#_CPU
22,44 PROCHOT#_PD_R
24 THERMTRIP#_CPU
99 EAR_N_TEST_NCTF
99 CPU_JTAG_TCK
99 CPU_JTAG_TDI
99 CPU_JTAG_TDO
99 CPU_JTAG_TMS
99 CPU_JTAG_TRST#
99 CPU_JTAG_PRDY#
99 CPU_JTAG_PREQ#
99 PCH_JTAG_TCK

TOUCH_SCREEN_PD#_R
TOUCHPAD_INTR# 24,65
GPU_EVENT# 79
DBG_PMODE 15,99
TOUCH_SCREEN_DET# 55

CPU1U — TGL-U-1-GP-U1 — 21 OF 21 — ZZ.00CPU.481

CATERR# M7
PECI_CPU K8
PROCHOT#_CPU_R E2
THERMTRIP#_CPU M5
CPU_POPIRCOMP F39
PCH_POPIRCOMP CB9
TP#CW12 CW12
TP#CM39 CM39
DBG_PMODE DF4
TOUCH_SCREEN_DET# DB42
TOUCH_SCREEN_PD# DB41
TOUCHPAD_INTR# DF8
MEM_INTERLEAVED DU5
GPP_H2 DF31
GPP_H1 DV32
GPP_H0 DW32
DJ27

CATERR#
PECI
PROCHOT#
THRMTRIP#
PROC_POPIRCOMP
PCH_OPIRCOMP
TP#CW12
TP#CM39
DBG_PMODE
GPP_B4/CPU_GP3
GPP_B3/CPU_GP2
GPP_E7/CPU_GP1
GPP_E3/CPU_GP0
GPP_H2
GPP_H1
GPP_H0
GPP_H19/TIME_SYNC0

PROC_TRST# K4 — CPU_JTAG_TRST#
PROC_TMS B9 — CPU_JTAG_TMS
PROC_TDO D12 — CPU_JTAG_TDO
PROC_TDI A12 — CPU_JTAG_TDI
PROC_TCK B6 — CPU_JTAG_TCK
PCH_JTAGX D8
PCH_TMS A9
PCH_TDO E12
PCH_TDI B12
PCH_TCK A7 — PCH_JTAG_TCK
PCH_TRST# H4
PROC_PREQ# C11 — CPU_JTAG_PREQ#
PROC_PRDY# D11 — CPU_JTAG_PRDY#
EAR_N/EAR_N_TEST_NCTF G1 — EAR_N_TEST_NCTF
GPP_F7 DT15
GPU_EVENT# DR15
GPP_F10 DT14

49D9R2F-GP R305 — CPU_POPIRCOMP
49D9R2F-GP R304 — PCH_POPIRCOMP
Do Not Stuff R324 — TP#CW12
Do Not Stuff R325 — TP#CM39
TP301 GPP_H2
TP302 GPP_H1
TP303 GPP_H0

R302 100R2F-L1-GP-U: TOUCH_SCREEN_PD#_R — TOUCH_SCREEN_PD#

1D05V_VCCSTG_TERM
R323 100R2F-L1-GP-U — CPU_JTAG_TDO
R320 DY Do Not Stuff — CPU_JTAG_PREQ#
R326 DEBUG 51R2J-2-GP — CPU_JTAG_TDI
R327 DEBUG 51R2J-2-GP — CPU_JTAG_TMS

R319 51R2J-2-GP — CPU_JTAG_TCK
R311 DY Do Not Stuff — CPU_JTAG_TRST#
R313 DY Do Not Stuff — PCH_JTAG_TCK

#544669 CRB Rev0.52
1D05V_VCCST
R310 1KR2J-1-GP — THERMTRIP#_CPU

1D05V_VCCSTG
R312 1KR2J-1-GP — EAR_N_TEST_NCTF

1D05V_VCCST
R316 1KR2J-1-GP — CATERR#

3D3V_S0
R308 100KR2F-L1-GP — TOUCHPAD_INTR#
R309 DY Do Not Stuff — TOUCH_SCREEN_PD#
On_LCD_SIDE

1D05V_VCCSTG_TERM
R306 Rb 1KR2J-1-GP
R307 Ra 499R2F-2-GP
R303 DY Do Not Stuff
PROCHOT#_PD_R — PROCHOT#_CPU — PROCHOT#_CPU_R

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

3D3V_S5_PCH
R314 DY Do Not Stuff
MEM_INTERLEAVED
R315 10KR2J-3-GP

Figure 10-1. Routing Illustration for PROCHOT# Topology

M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

3D3V_S0
R317 DY Do Not Stuff
GPP_F7
R318 DY Do Not Stuff

3D3V_S0
R321 DY Do Not Stuff
GPP_F10
R322 DY Do Not Stuff

DIMM_TYPE	
LOW	HIGH
NON_INTERLEAVED	INTERLEAVED

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Title: CPU (THML/JTAG)
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Main Func = CPU

eDP

eDP_TX_CPU_N0 55
eDP_TX_CPU_P0 55
eDP_TX_CPU_N1 55
eDP_TX_CPU_P1 55
eDP_TX_CPU_N2 55
eDP_TX_CPU_P2 55
eDP_TX_CPU_N3 55
eDP_TX_CPU_P3 55

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

EDP_HPD 55

eDP_BLEN_CPU 55
eDP_BLCTRL_CPU 55
eDP_VDDEN_CPU 55

USB_OC1#

DP to MUX

DP2_DDI_TX_N1 57
DP2_DDI_TX_P0 57
DP2_DDI_TX_P1 57
DP2_DDI_TX_N2 57
DP2_DDI_TX_P2 57
DP2_DDI_TX_N3 57
DP2_DDI_TX_P3 57

DP_HPD_CPU 57

57 CPU_DP2_CTRL_CLK
57 CPU_DP2_CTRL_DATA

KB_DET# 65

TBT2_LSX0_RXD 4,15,71

71 USB1_TCSS_RX_P1
71 USB1_TCSS_RX_N1
71 USB1_TCSS_RX_P0
71 USB1_TCSS_RX_N0
71 USB1_TCSS_TX_P1
71 USB1_TCSS_TX_N1
71 USB1_TCSS_TX_P0
71 USB1_TCSS_TX_N0
71 USB1_TCSS_AUX_P
71 USB1_TCSS_AUX_N

71 USB2_TCSS_RX_P1
71 USB2_TCSS_RX_N1
71 USB2_TCSS_RX_P0
71 USB2_TCSS_RX_N0
71 USB2_TCSS_TX_P1
71 USB2_TCSS_TX_N1
71 USB2_TCSS_TX_P0
71 USB2_TCSS_TX_N0
71 USB2_TCSS_AUX_P
71 USB2_TCSS_AUX_N

71 TBT_LSX0_TXD
15,71 TBT_LSX0_RXD

71 TBT2_LSX0_TXD
4,15,71 TBT2_LSX0_RXD

3.3V_CAM_EN# 40

HDMI 2.0

TBT

CY20 CPU_DISP_HPD4

CPU1A 1 OF 21

eDP_TX_CPU_P3 AC2 DDIA_TXP3
eDP_TX_CPU_N3 AC1 DDIA_TXN3
eDP_TX_CPU_P2 AD2 DDIA_TXP2
eDP_TX_CPU_N2 AD1 DDIA_TXN2
eDP_TX_CPU_P1 AF1 DDIA_TXP1
eDP_TX_CPU_N1 AF2 DDIA_TXN1
eDP_TX_CPU_P0 AG2 DDIA_TXP0
eDP_TX_CPU_N0 AG1 DDIA_TXN0

eDP_AUX_CPU_P AJ2 DDIA_AUX_P
eDP_AUX_CPU_N AJ1 DDIA_AUX_N

DN4
DT6
GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA

EDP_HPD DR5 GPP_E14/DDSP_HPDA/DISP_MISCA

DP2_DDI_TX_P3 T12 DDIB_TXP3
DP2_DDI_TX_N3 T11 DDIB_TXN3
DP2_DDI_TX_P0 Y11 DDIB_TXP2
DP2_DDI_TX_N0 Y9 DDIB_TXN2
DP2_DDI_TX_P1 T9 DDIB_TXP1
DP2_DDI_TX_N1 P9 DDIB_TXN1
DP2_DDI_TX_P2 V11 DDIB_TXP0
DP2_DDI_TX_N2 V9 DDIB_TXN0

AB9
AD9
DDIB_AUX_P
DDIB_AUX_N

CPU_DP2_CTRL_CLK DM29 GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
CPU_DP2_CTRL_DATA DK27 GPP_H17/DDPB_CTRLDATA

DP_HPD_CPU DG43 GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

3.3V_CAM_EN# DG47 GPP_A21/DDPC_CTRLCLK/I2S5_TXD
KB_DET# DJ47 GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT_LSX0_TXD DU8 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
TBT_LSX0_RXD DV8 GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

TBT2_LSX0_TXD DF6 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
TBT2_LSX0_RXD DD6 GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

DN23
DM23
GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK

DK23
DN21
GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI

3MM_CAM_DET# DF43 GPP_A17/DISP_MISCC/I2S4_TXD
CPU_DISP_HPD1 DF45 GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
DF47 GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

USB_OC1# DH52
USB_OC2# DK45
GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

eDP_VDDEN_CPU DM8 EDP_VDDEN
eDP_BLEN_CPU DN8 EDP_BKLTEN
eDP_BLCTRL_CPU DG10 EDP_BKLTCTL

TGL-U-1-GP-U1

ZZ.00CPU.481

TCP0_TXRX_P1 AY2 USB1_TCSS_RX_P1
TCP0_TXRX_N1 AY1 USB1_TCSS_RX_N1
TCP0_TXRX_P0 BB1 USB1_TCSS_RX_P0
TCP0_TXRX_N0 BB2 USB1_TCSS_RX_N0
TCP0_TX_P1 AM5 USB1_TCSS_TX_P1
TCP0_TX_N1 AM7 USB1_TCSS_TX_N1
TCP0_TX_P0 AT7 USB1_TCSS_TX_P0
TCP0_TX_N0 AT5 USB1_TCSS_TX_N0
TCP0_AUX_P AP7 USB1_TCSS_AUX_P
TCP0_AUX_N AP5 USB1_TCSS_AUX_N

TBT

TCP1_TXRX_P1 AT2 USB2_TCSS_RX_P1
TCP1_TXRX_N1 AT1 USB2_TCSS_RX_N1
TCP1_TXRX_P0 AU1 USB2_TCSS_RX_P0
TCP1_TXRX_N0 AU2 USB2_TCSS_RX_N0
TCP1_TX_P1 AD5 USB2_TCSS_TX_P1
TCP1_TX_N1 AD7 USB2_TCSS_TX_N1
TCP1_TX_P0 AH7 USB2_TCSS_TX_P0
TCP1_TX_N0 AH5 USB2_TCSS_TX_N0
TCP1_AUX_P AF7 USB2_TCSS_AUX_P
TCP1_AUX_N AF5 USB2_TCSS_AUX_N

TBT2

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE2
TCP2_TXRX_N0 BE1
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX_N BB7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7

TC_RCOMP_P AN2 TCSS_RCOMP_P
TC_RCOMP_N AN1 TCSS_RCOMP_N R402 1 2 150R2F-1-GP

DSI_DE_TE_2 M8 DSI_DE_TE_2 R403 1 2 100KR2J-1-GP

DDI_RCOMP AB1 eDP_RCOMP_CPU R401 1 2 150R2F-1-GP

DISP_UTILS/DSI_DE_TE_1 CE4

CPU_DISP_HPD1
R404 DY Do Not Stuff

3D3V_S5_PCH
R415 1 2 10KR2J-3-GP USB_OC1#
R416 1 2 10KR2J-3-GP USB_OC2#
R408 1 2 100KR2F-L1-GP 3.3V_CAM_EN#
R405 1 2 100KR2F-L1-GP KB_DET#

3D3V_S0
R407 1 DY 2 3MM_CAM_DET#
Do Not Stuff

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Title: CPU (DDI/EDP)
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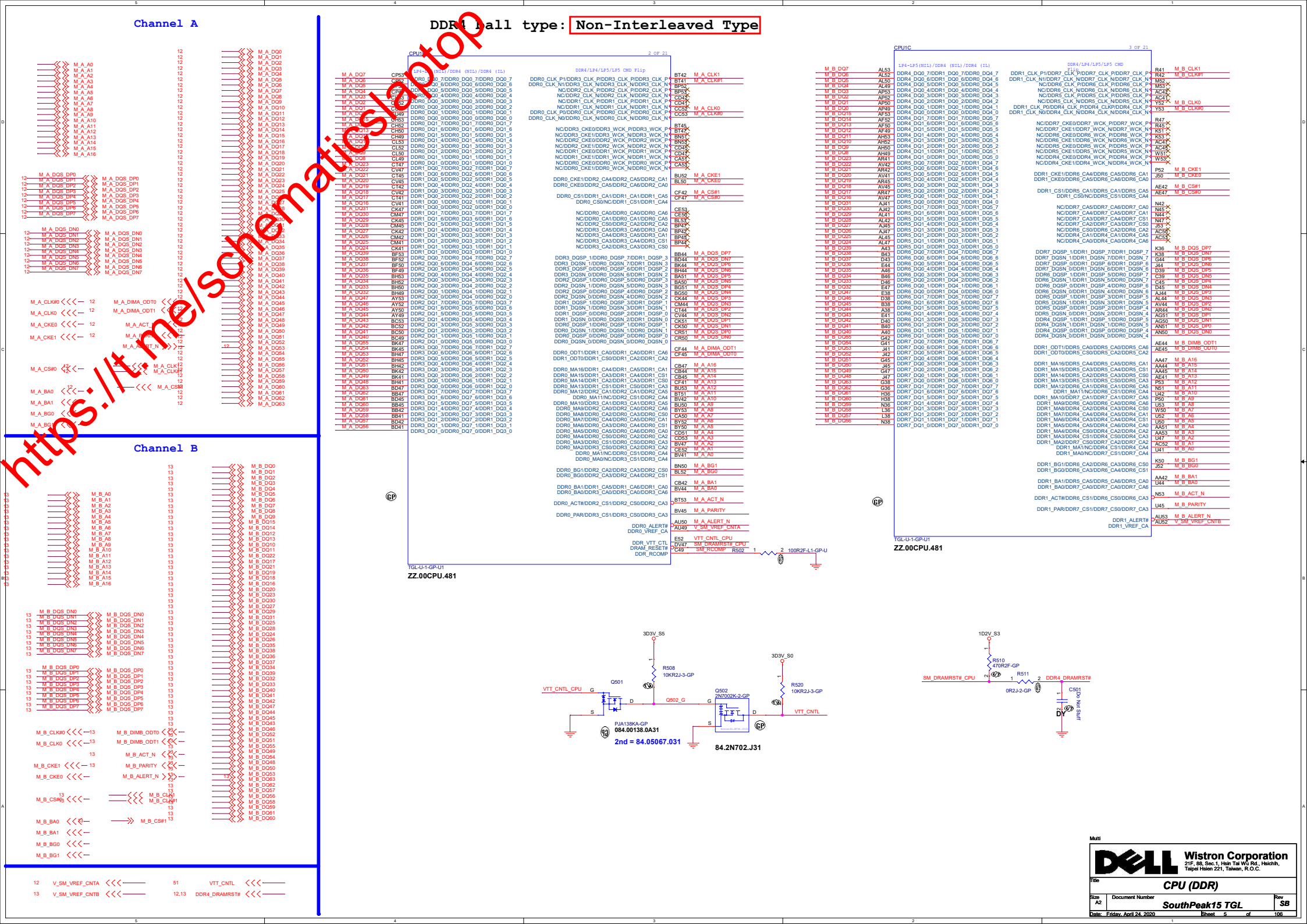

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Title: CPU (DDR)

Size	Document Number	Rev
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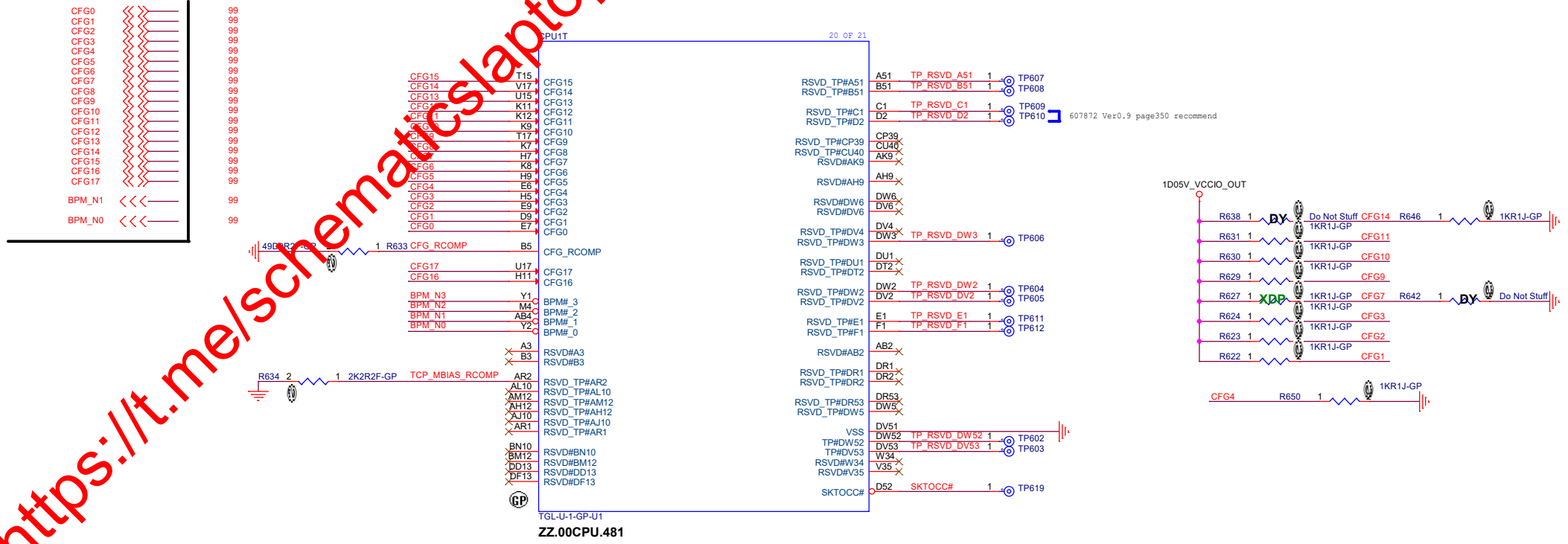
Main Func = CPU



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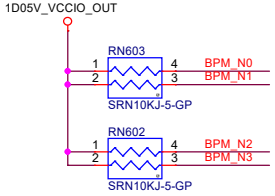

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

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Title: CPU (CFG/IST)

Size: A3 | Document Number: SouthPeak15 TGL | Rev: SB

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Main Func = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU

CPU_1M 13 OF 21

1V_CPU_CORE

VCCIN: AK26, A29, A30, A33, A35, AY39, B24, B26, B29, B30, B33, B35, BA10, BA40, BB39, BB9, BC10, BC40, BD39, BD9, BE10, BE40, BF9, BG10, BG40, BH12, BH39, BH9, BJ10, BJ40, BK39, BL10, BL40, BM39, BN40, BP12, BP39, BR10, BR40, BT12, BT39, BU10, BU40, BV12, BY12, CA10, CB12, D24, D26, D29, D30, D33, D35, E24, E26, E27, E29, E30, E32, E33, G2, G24, G26, G30

1V_CPU_CORE

VCCIN: G32, H24, H26, H30, H32, J1, J2, K1, K2, K24, K26, K30, K32, L24, L26, L30, L32, N24, N26, N30, N32, P24, P26, P28, P30, P32, T21, T23, T25, T27, T31, U23, U27, U29, U31, U33, V23, V25, V27, V29, V31, V33, W22, W24, W28, W32

VCCIN_SENSE — R38 — VCCCORE_SENSE
VSSIN_SENSE — R37 — VSSCORE_SENSE

VIDSOUT — M12 — SVID_DATA_CPU
VIDSCK — M11 — SVID_CLK_CPU
VIDALERT# — P12 — SVID_ALERT#_CPU_R

R706 1 — 2 0R2J-2-GP — SVID_ALERT#_CPU

TGL-U-1-GP-U1

ZZ.00CPU.481

1D05V_VCCST

R703 1 — 2 100R2F-L1-GP-U — SVID_DATA_CPU
R701 1 — 2 56R2J-4-GP — SVID_ALERT#_CPU

Layout note:
Length matchin 25mil, and close SOC in 2inch "

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

1V_CPU_CORE

R704 1 — 2 100R2F-L1-GP-U — VCCCORE_SENSE
R705 2 — 100R2F-L1-GP-U — VSSCORE_SENSE

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Title: **CPU (VCORE/VID)**

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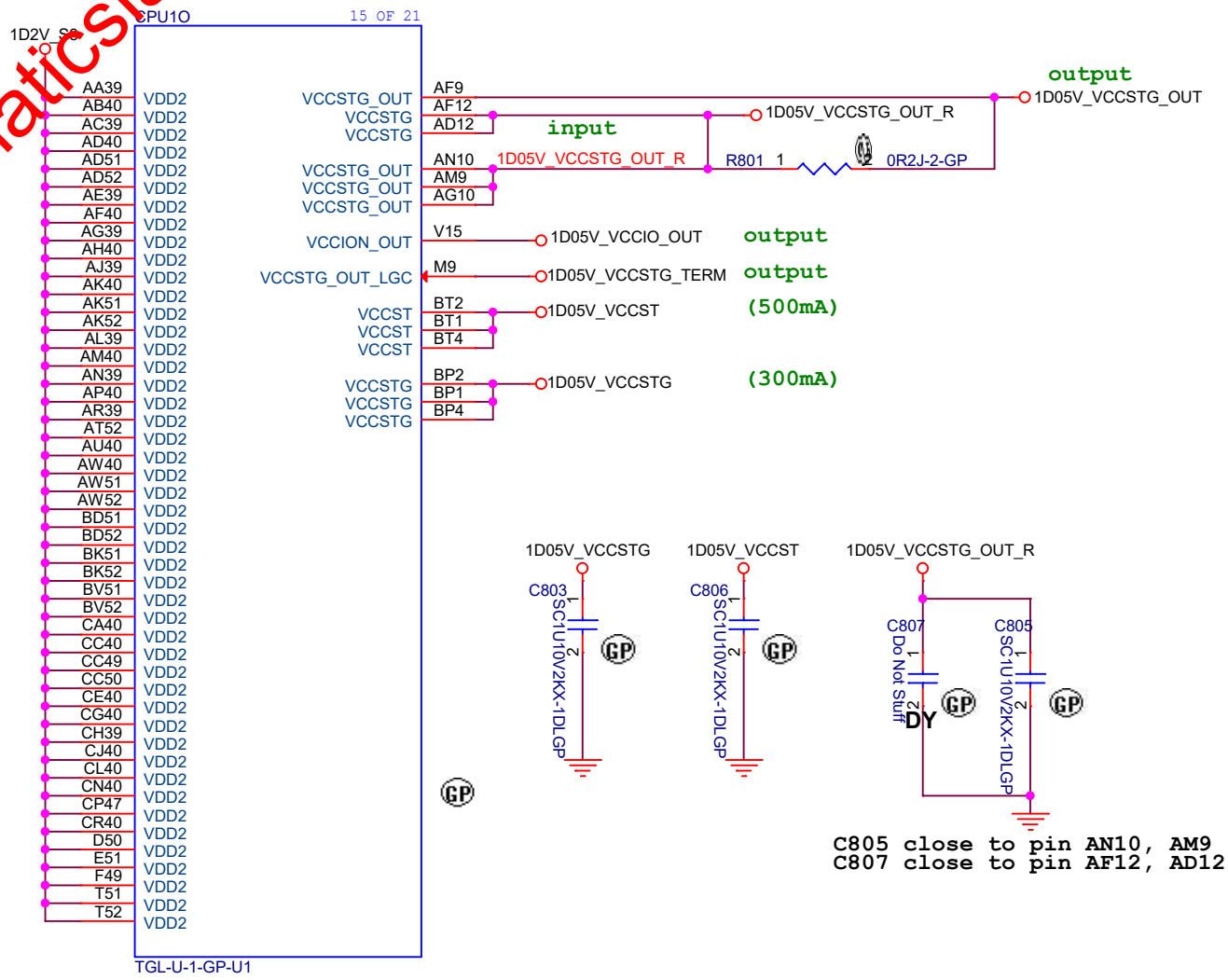
Main Func = CPU



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Title: CPU (VCCGT/VCCIO/VDDQ/VCCSA)

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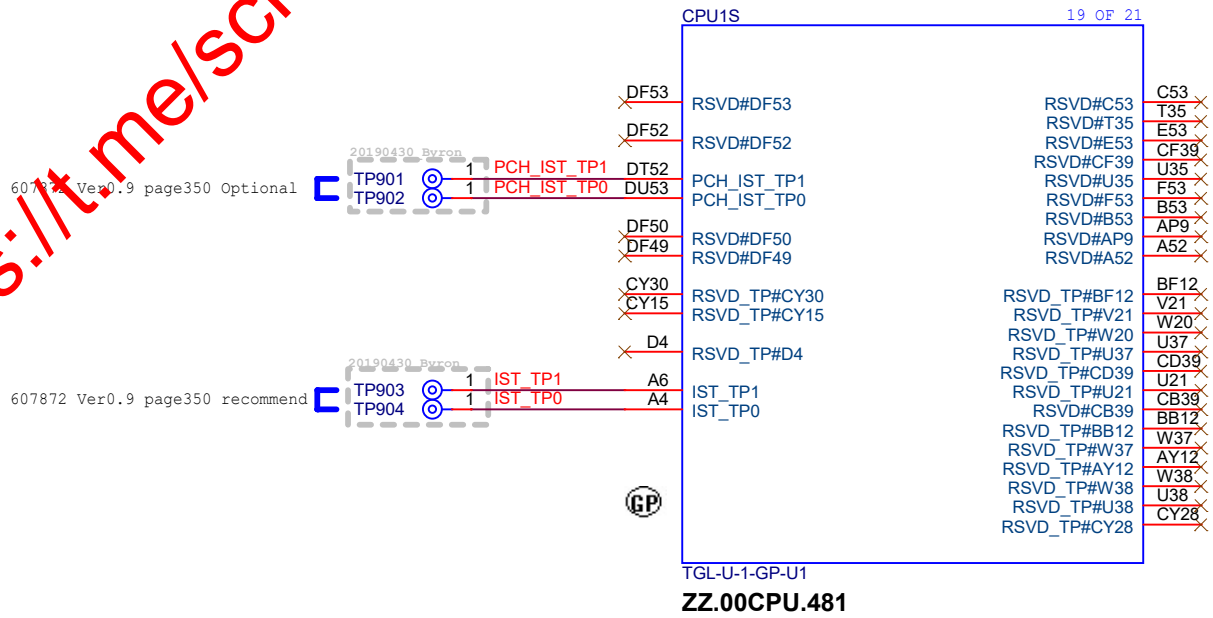

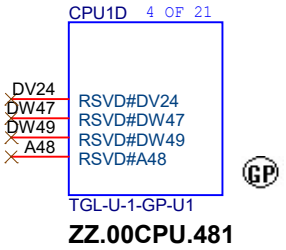

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Title: CPU (RSVD)

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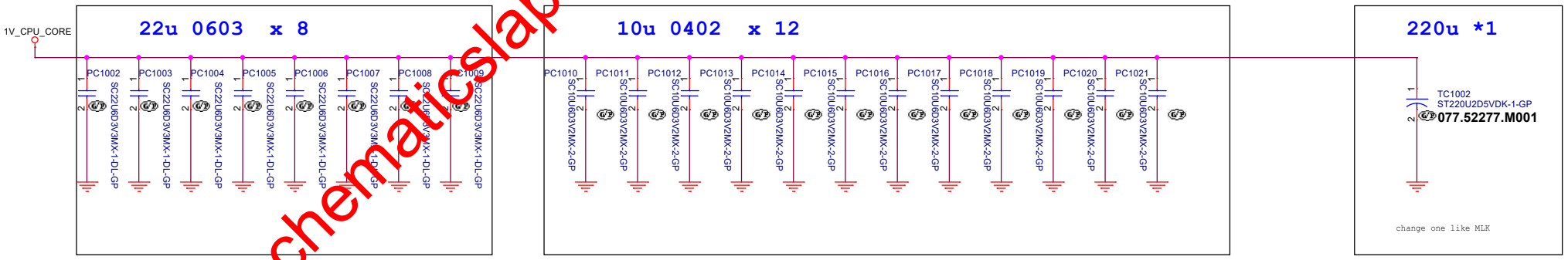
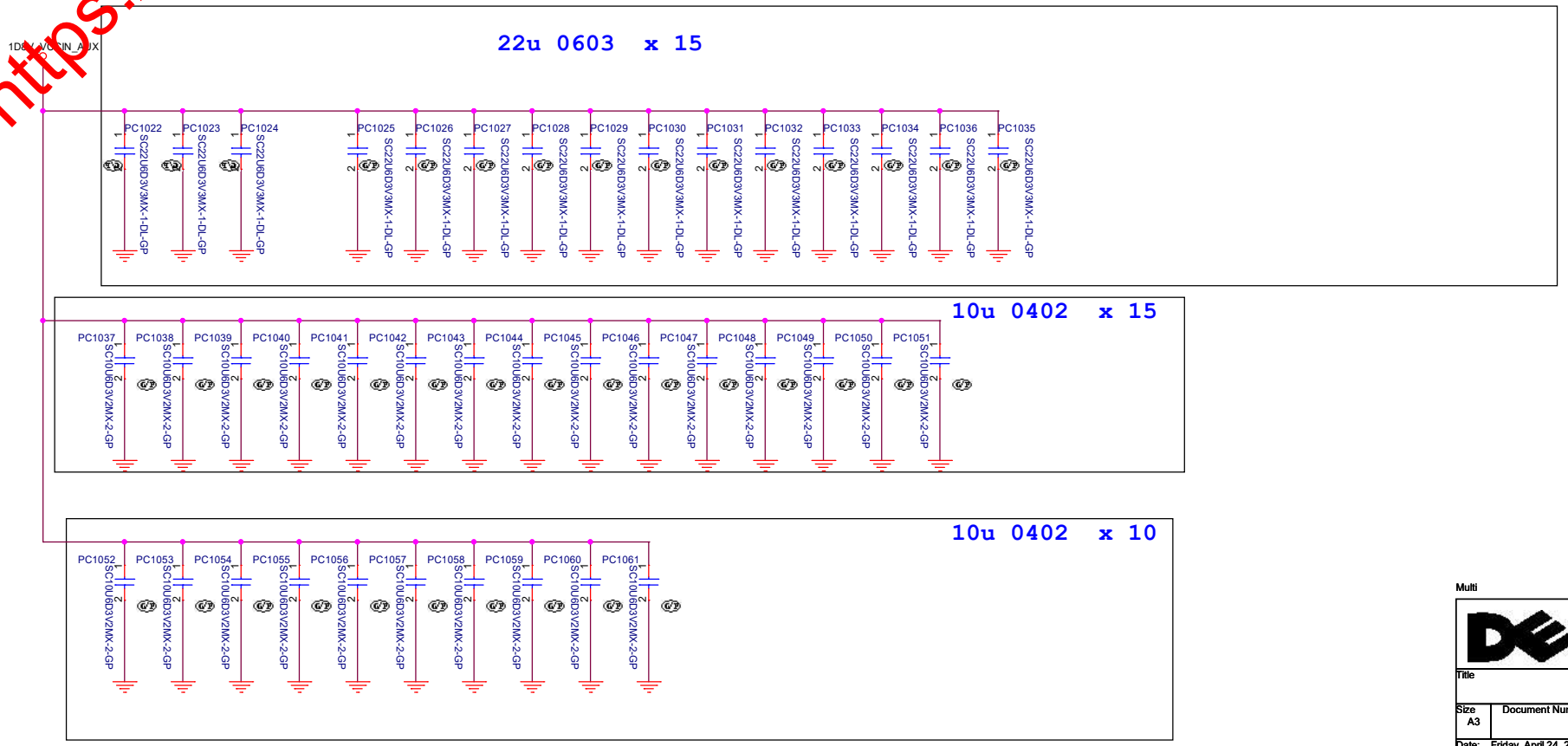
Main Func = CPU

1V_CPU_CORE (VCCIN)



VCCIN_AUX



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Title	CPU (CORE Power Cap1)	
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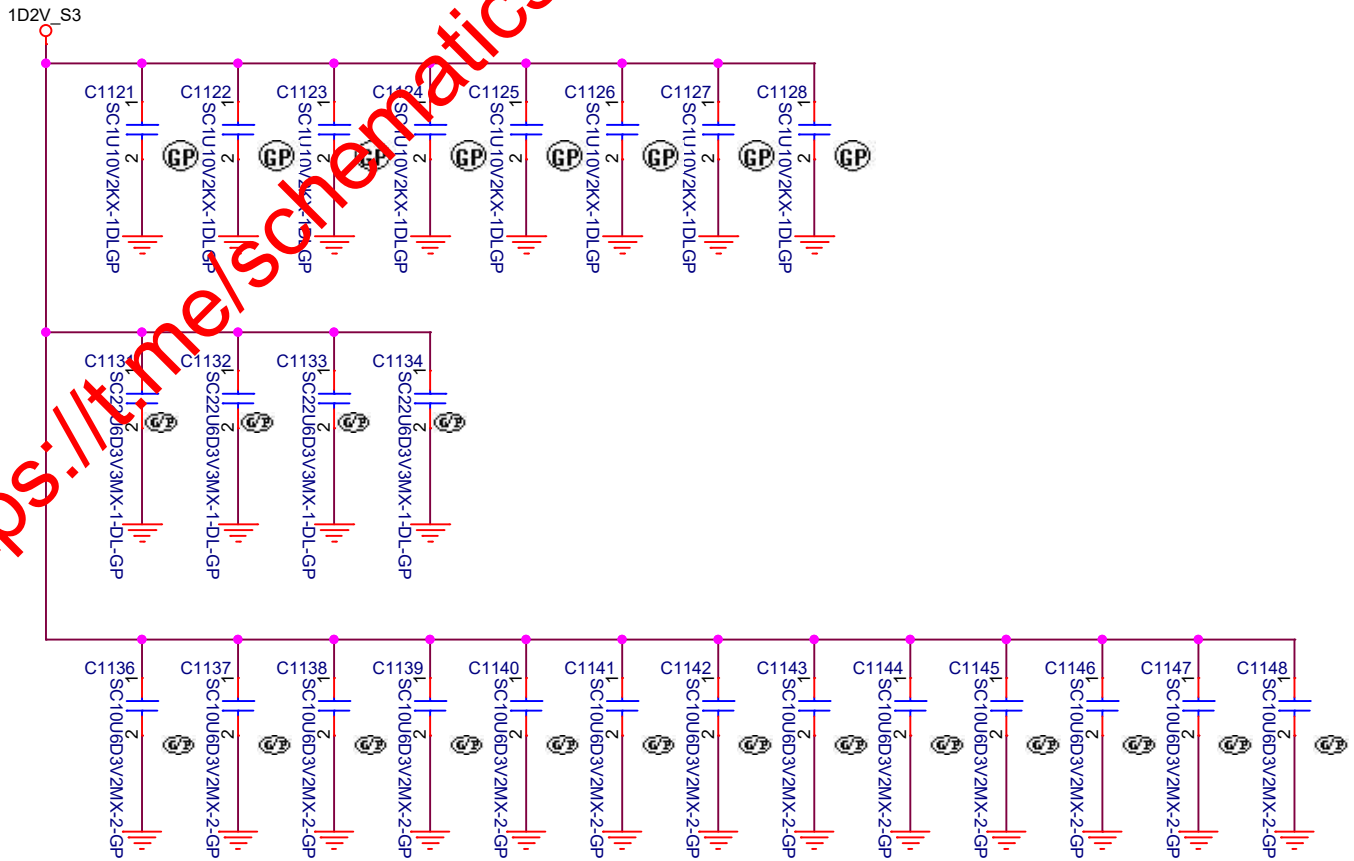
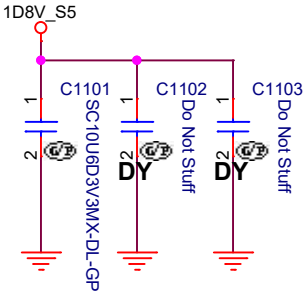
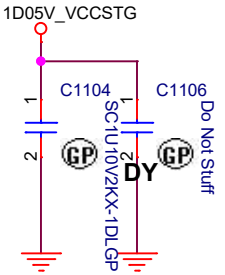
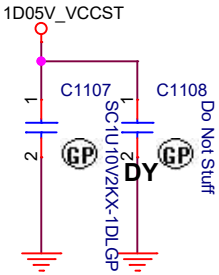
Main Func = CPU

VDDQ









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Title	CPU (Power Cap2)	
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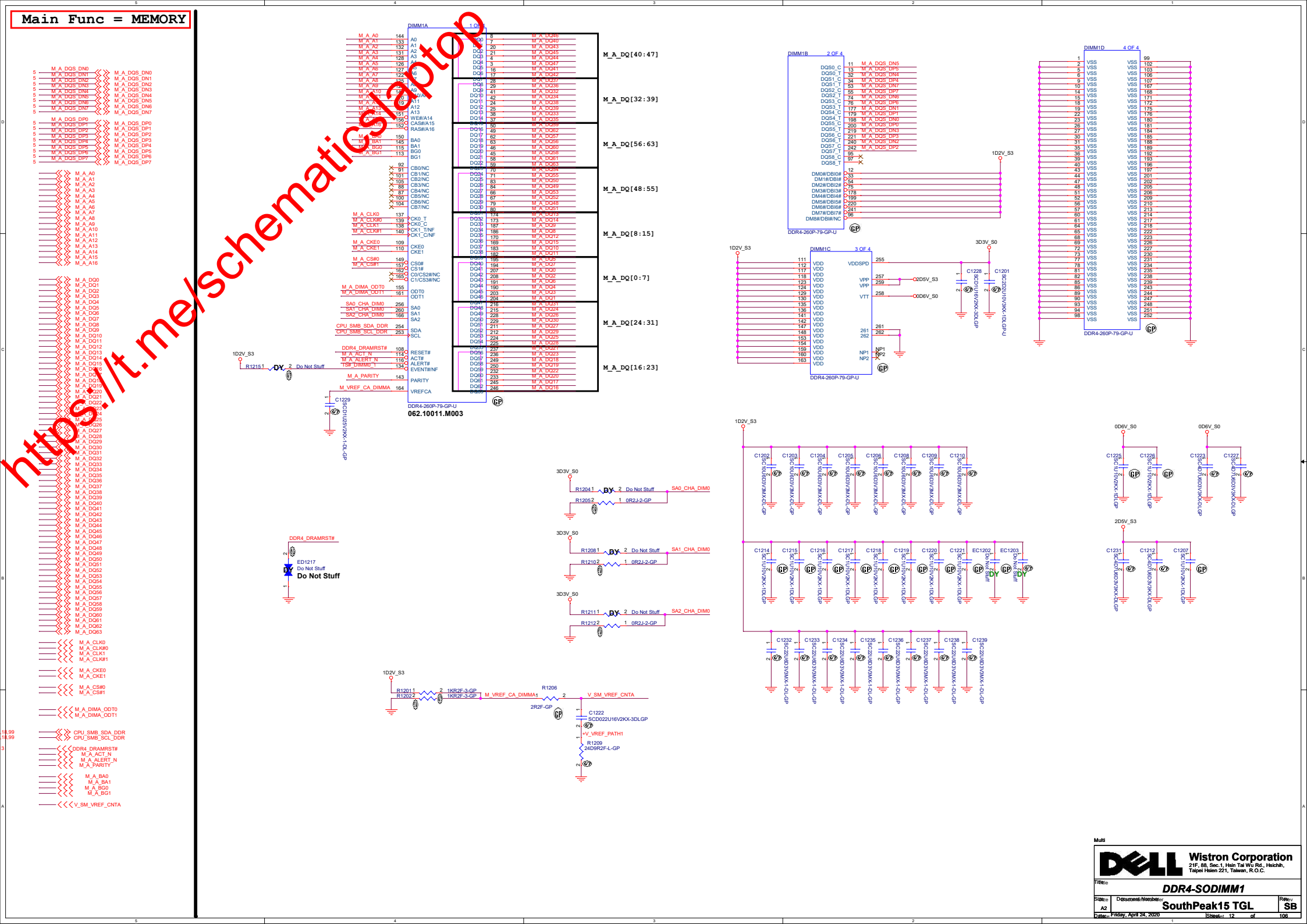
Main Func = MEMORY



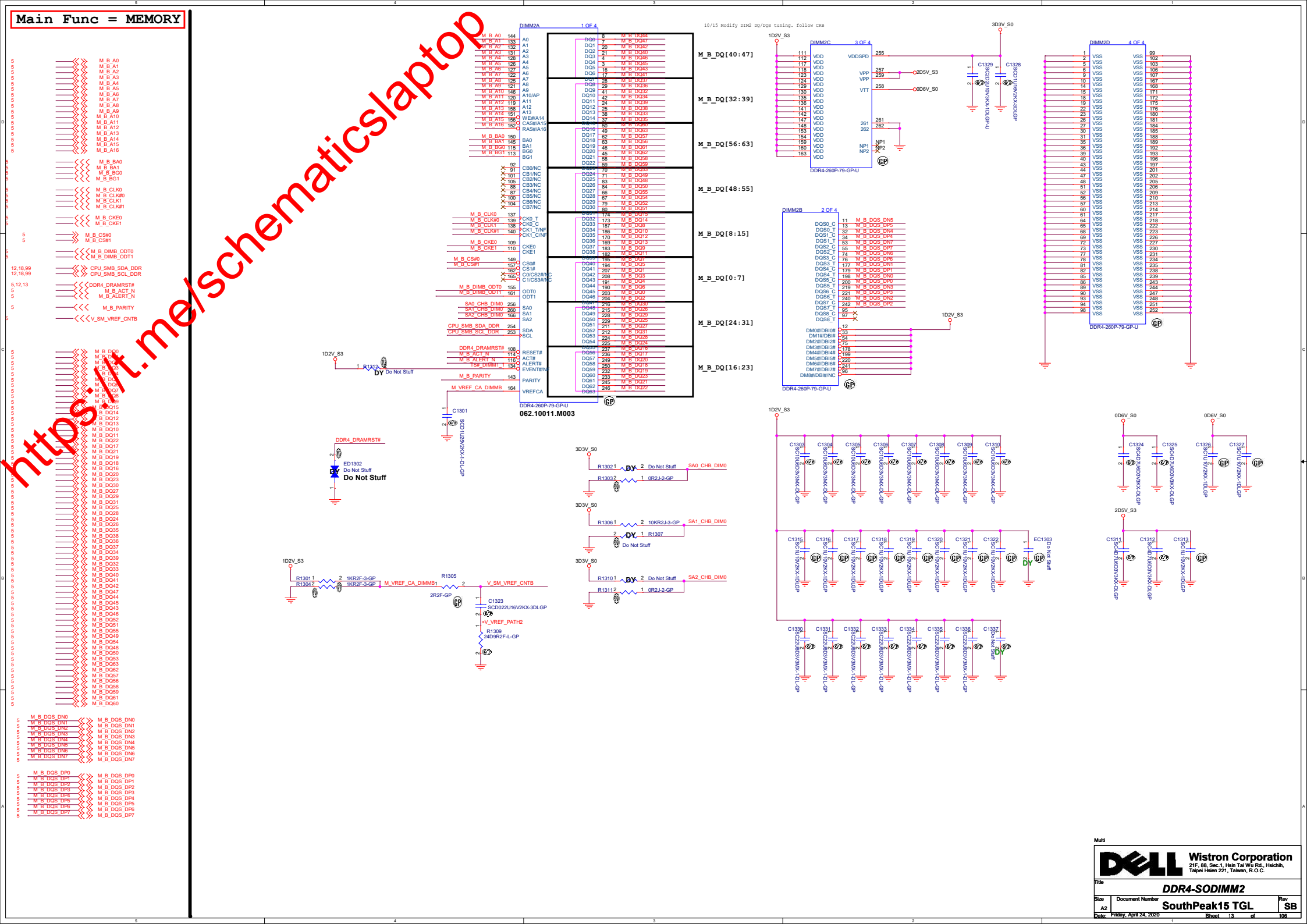
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4-SODIMM1

Size: A2 | Document Number: SouthPeak15 TGL | Rev: SB

Date: Friday, April 24, 2020 | Sheet 12 of 106

Main Func = MEMORY



Multi
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR4-SODIMM2**

Size	Document Number	Rev
A2	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 13 of 106

(Blanking)

Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (RSVD) (DDR4-CHA1)

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

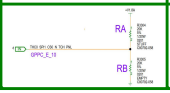
Date: Friday, April 24, 2020 Sheet 14 of 106

18,68,99 SPI_SI_CPU
18,68,99 SPI_WP_CPU
18,68,99 SPI_HOLD_CPU
CNV_RGI_DT
18 GPP_C5
18 GPP_E6
19 HDA_SDO
TBT_LSX0_RXD
3,99 DBG_PMODE
4,71 TBT2_LSX0_RXD
18 GPP_E10

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic	21,61 4,71 3D3V_S5_PCH =20K PD= R1501 DY Do Not Stuff GPP_C5 R1502 DY Do Not Stuff	3D3V_SPI =NO INTERNAL= R1503 4K7R2J-2-GP SPI_SI_CPU BOOT_HALT Close to U2501 R1511 DY Do Not Stuff	3D3V_S5_PCH =NO INTERNAL= R1504 check if PH 3D3V_SUS ??? 100KR2J-1-GP GPP_E6 R1512 DY Do Not Stuff	=20K PD=	3D3V_SPI =NO INTERNAL= R1506 100KR2J-1-GP SPI_WP_CPU Close to U2501 R1514 DY Do Not Stuff CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	* PH as VCCPGPPR =20K PD= 1D8V_GPPR_S5 R1509 DY Do Not Stuff ME_UNLOCK R1515 0R2J-2-GP HDA_SDO	1D8V_S5 =NO INTERNAL= R1507 100KR2J-1-GP CNV_RGI_DT R1516 DY Do Not Stuff
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic	E11 3D3V_S5_PCH =NO INTERNAL= R1518 DY Do Not Stuff TBT_LSX0_RXD R1521 20KR2J-L2-GP	E21 3D3V_S5_PCH =NO INTERNAL= R1519 DY Do Not Stuff TBT2_LSX0_RXD R1522 20KR2J-L2-GP	D10 =NO INTERNAL=	D12 =NO INTERNAL=	3D3V_SPI =NO INTERNAL= R1526 100KR2J-1-GP SPI_HOLD_CPU Close to U2501 R1527 DY Do Not Stuff	1D05V_S5_OUT =20K PU= R1528 XDP 1KR2F-3-GP DBG_PMODE R1529 DY Do Not Stuff	1D8V_S5 R1531 20KR2J-L2-GP GPP_E10	
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD				

Multi

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (STRAP)		
Size: A2	Document Number: SouthPeak15 TGL	Rev: SB
Date: Friday, April 24, 2020	Sheet 15 of 106	

Main Func = PCH

USB3.1 PORT1
35USB1_USB31_RX_N
35USB1_USB31_RX_P
35USB1_USB31_TX_N
35USB1_USB31_TX_P

USB3.1 PORT2
35USB2_USB31_RX_N
35USB2_USB31_RX_P
35USB2_USB31_TX_N
35USB2_USB31_TX_P

WWAN
62WWAN_USB31_RX_N
62WWAN_USB31_RX_P
62WWAN_USB31_TX_N
62WWAN_USB31_TX_P

LAN
97 LAN_PCIE_RX_N
97 LAN_PCIE_RX_P
97 LAN_PCIE_TX_N
97 LAN_PCIE_TX_P

CARD
33 CARD_PCIE_RX_N
33 CARD_PCIE_RX_P
33 CARD_PCIE_TX_N
33 CARD_PCIE_TX_P

WLAN
61 WLAN_PCIE_RX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_TX_P

WWAN
62 WWAN_PCIE_RX_N
62 WWAN_PCIE_RX_P
62 WWAN_PCIE_TX_N
62 WWAN_PCIE_TX_P

SSD
63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P1
63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P2
63 SSD_SATA_RX_N
63 SSD_SATA_RX_P
63 SSD_SATA_TX_N
63 SSD_SATA_TX_P

Type C USB 1
73 USB1_USB20_N
73 USB1_USB20_P

Type C USB 2
73 USB2_USB20_P
73 USB2_USB20_N

FP
92 FP_USB20_P
92 FP_USB20_N

USB charger
36 Charger_USB20_N
36 Charger_USB20_P

USB2.0 port4
35 USB4_USB20_N
35 USB4_USB20_P

CAMERA
56 CCD_USB20_N
56 CCD_USB20_P

WWAN
62 WWAN_USB20_N
62 WWAN_USB20_P

USH
66 USH_USB20_N
66 USH_USB20_P

BT
61 BT_USB20_N
61 BT_USB20_P

36 USB_OC0#
CONTACTLESS_DET# 66
GPU_GC6_FB_EN 75,86
m2280_PCIE_SATA# 63
M2280_DEVSLP 63

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

SSD
LAN
CARDREADER
WLAN
WINDOS WWAN
UBUNTU WWAN
USB4 Type A port2
USB3 Type A port1

CPU1I — 9 OF 21
TGL-U-1-GP-U1
ZZ.00CPU.481

BT
FP
USH
WWAN
CAMERA
USB4 Type A port 4
USB3 Type A port 3
USB2 Type C port 2
USB1 Type C port 1
Reserved for BC feature, PAID for 2.5" HDD

GPU is NV, not AMD

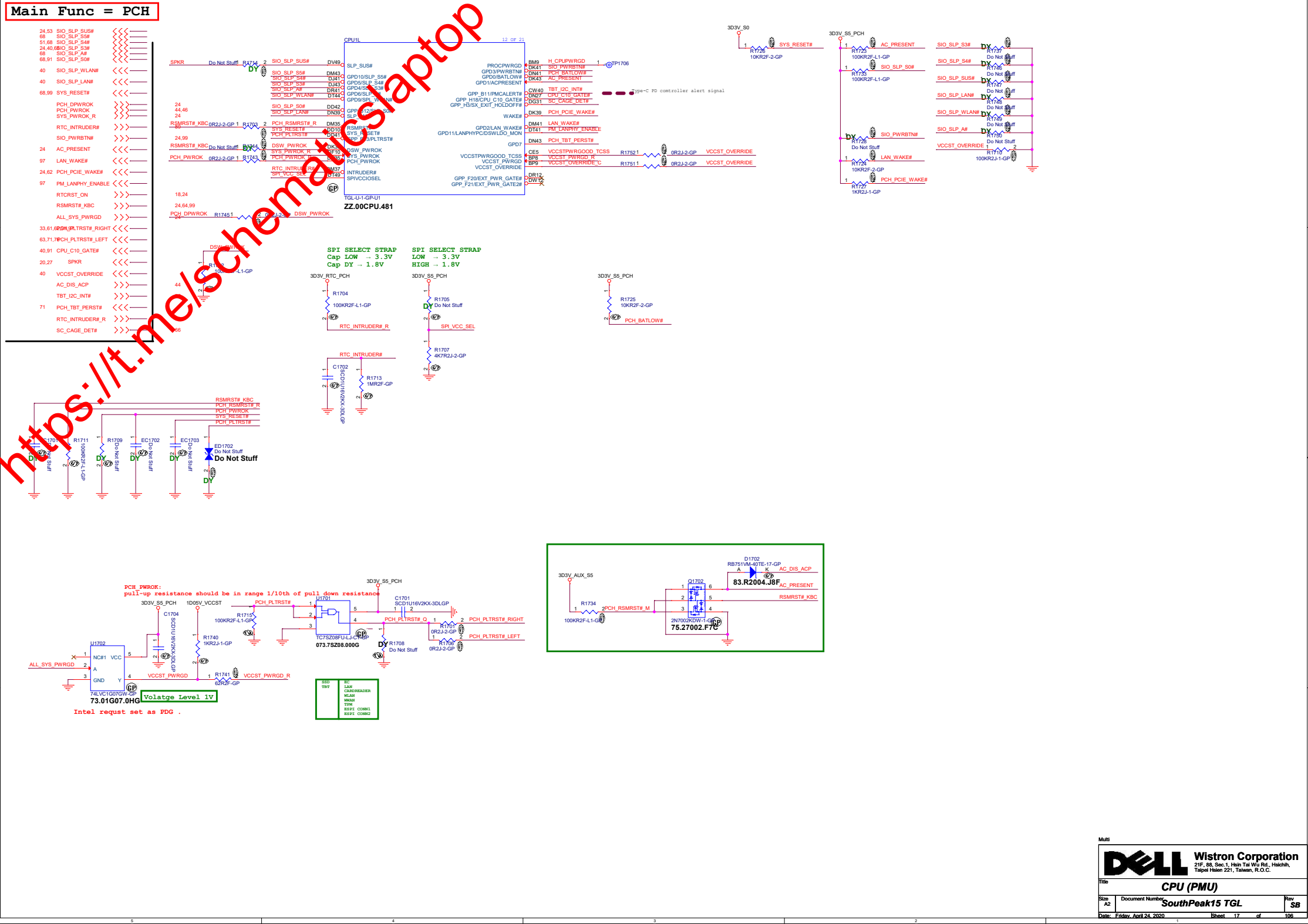
teknisi indonesia

CPU1H — 8 OF 21
TGL-U-1-GP-U1
ZZ.00CPU.481

Layout Note:
1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

Multi
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (PCIE/SATA/USB)
Size: A2
Document Number: SouthPeak15 TGL
Rev: SB
Date: Friday, April 24, 2020
Sheet 16 of 106

Main Func = PCH



Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)

Size	Document Number	Rev
A2	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 17 of 106

Main Func = PCH

SPI ROM
68,96 SPI_CLK_CPU
15,68,99 SPI_SI_CPU
SPI_SO_CPU
15,68,99 SPI_WP_CPU
15,68 SPI_HOLD_CPU
68 SPI_CS_CPU_N0
68 SPI_CS_CPU_N1
91 SPI_CS_CPU_N2

WLAN
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
WLAN_CLKREQ_CPU_N

WWAN
WWAN_CLK_CPU_P
WWAN_CLK_CPU_N
WWAN_CLKREQ_CPU_N
62 WWAN_GPIO_PERST#
62 WWAN_GPIO_WAKE#

LAN
LAN_CLK_CPU_N
LAN_CLK_CPU_P
LAN_CLKREQ_CPU_N

CARD
CARD_CLK_CPU_N
CARD_CLK_CPU_P
CARD_CLKREQ_CPU_N

SSD
SSD_CLK_CPU_N
SSD_CLK_CPU_P
SSD_CLKREQ_CPU_N

SSD2
SSD2_CLK_CPU_N
SSD2_CLK_CPU_P
SSD2_CLKREQ_CPU_N

ESPI
24,68,96 ESPI_IO0
24,68,96 ESPI_IO1
24,68,96 ESPI_IO2
24,68,96 ESPI_IO3
24,68 ESPI_CS#
24,68 ESPI_RESET#
24,68,96 ESPI_CLK

OTHER
12,68,99 SMB_SCL_DDR
12,68,99 SMB_SDA_DDR
SML0_SMBCLK
SML0_SMBDATA
72 SML1_SMBCLK
72 SML1_SMBDATA
15 GPE_E6
61 SUSCLK
71 LID_CL#
71 PWRBTN#
61 HDMI_PD#
61 TS_INT#
61 WWAN_BB_RST#
61 CL_CLK
61 CL_RST#
61 CL_DATA
68 RTC_RST#
RTCRST_ON
33 MEDIACARD_IRQ#
RTC_DET#
56 SECURE_BIO
96 ESPI_CPU_CLK_R
96 ESPI_CPU_IO0_R
96 ESPI_CPU_IO1_R
96 ESPI_CPU_IO2_R
96 ESPI_CPU_IO3_R

CPU1E 5 OF 21
SPI_CLK_CPU DJ37
SPI_HOLD_CPU DG35
SPI_WP_CPU DJ39
SPI_SO_CPU DJ33
SPI_SI_CPU DJ35
SPI_CS_CPU_N1 DF35
SPI_CS_CPU_N0 DG37
SPI_CS_CPU_N2 DF37
VPRO_DET# DJ41
MEDIACARD_IRQ# DN9
TS_INT# DJ9
RTC_DET# DM6
TBT_DET# DK6
GPP_E6 DK8
SECURE_BIO DV11
WWAN_BB_RST# DW9
CL_CLK DT8
CL_DATA DN15
CL_RST# DK13
DM13
DN13
DJ15
DK15
DN19
DV14
DH3
DH4
DF2
GPP_E10 GPP_E11/SPI1_CLK/THC0_SPI1_CLK
GPP_E2/SPI1_IO3/THC0_SPI1_IO3
GPP_E1/SPI1_IO2/THC0_SPI1_IO2
GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
GPP_E10/SPI1_CS#/THC0_SPI1_CS#
GPP_E8/SPI1_CS1#/SATA_LED#
GPP_E17/THC0_SPI1_INT#
GPP_E6/THC0_SPI1_RST#
GPP_F11/THC1_SPI2_CLK
GPP_F15/GSXSRESET#/THC1_SPI2_IO3
GPP_F14/GSXDIN/THC1_SPI2_IO2
GPP_F13/GSXSLOAD/THC1_SPI2_IO1
GPP_F12/GSXDOUT/THC1_SPI2_IO0
GPP_F16/GSXCLK/THC1_SPI2_CS#
GPP_F18/THC1_SPI2_INT#
GPP_F17/THC1_SPI2_RST#
TGL-U-1-GP-U1
ZZ.00CPU.481

GPP_C0/SMBCLK DK21 MEM_SMBCLK
GPP_C1/SMBDATA DM19 MEM_SMBDATA
GPP_C2/SMBALERT# DN19 GPP_C2
GPP_C3/SML0CLK DK19 SML0_SMBCLK
GPP_C4/SML0DATA DM17 SML0_SMBDATA
GPP_C5/SML0ALERT# DN17 GPP_C5
GPP_C6/SML1CLK DK17 SML1_SMBCLK
GPP_C7/SML1DATA DJ17 SML1_SMBDATA
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# CY50 GPP_B23
GPP_A5/ESPI_CLK DN53 ESPI_CPU_CLK_R
GPP_A3/ESPI_IO3/SUSACK# DJ53 ESPI_CPU_IO3_R
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK DH50 ESPI_CPU_IO2_R
GPP_A1/ESPI_IO1 DP50 ESPI_CPU_IO1_R
GPP_A0/ESPI_IO0 DR52 ESPI_CPU_IO0_R
GPP_A4/ESPI_CS# DK52 ESPI_CS#
GPP_A6/ESPI_RESET# DL50 ESPI_RESET#
Not Used, need 150Kohm PU

HDMI_PD# R18011 Do Not Stuff DY
3D3V_S5_PCH
NON_TBT R1810 10KR2F-GP
TBT_DET R1811 10KR2F-GP
TBT_DET# Dectect

TBT_DET#	Dectect
HIGH	NON TBT
LOW	TBT

CPU1K 11 OF 21
CAM_MIC_CBL_DET# need be confirm with Dell
LAN_CLK_CPU_P BW1
LAN_CLK_CPU_N BW2
CARD_CLK_CPU_P CB2
CARD_CLK_CPU_N CB1
WLAN_CLK_CPU_P BW4
WLAN_CLK_CPU_N BW5
SSD2_CLK_CPU_P CL7
SSD2_CLK_CPU_N CL8
SSD_CLK_CPU_P CB4
SSD_CLK_CPU_N CB5
WWAN_CLK_CPU_P BY4
WWAN_CLK_CPU_N BY3
GFX_CLK_CPU_P CN7
GFX_CLK_CPU_N CN8
XCLK_BIASREF DJ5
CLKOUT_PCIE_P6 / CLKOUT_PCIE_N6
CLKOUT_PCIE_P5 / CLKOUT_PCIE_N5
CLKOUT_PCIE_P4 / CLKOUT_PCIE_N4
CLKOUT_PCIE_P3 / CLKOUT_PCIE_N3
CLKOUT_PCIE_P2 / CLKOUT_PCIE_N2
CLKOUT_PCIE_P1 / CLKOUT_PCIE_N1
CLKOUT_PCIE_P0 / CLKOUT_PCIE_N0
GPP_F10/SRCCLKREQ6# DU14 LAN_CLKREQ_CPU_N
GPP_F11/SRCCLKREQ5# DG25 WLAN_CLKREQ_CPU_N
GPP_H10/SRCCLKREQ4# DG25 SSD2_CLKREQ_CPU_N
GPP_D8/SRCCLKREQ3# DT24 SSD_CLKREQ_CPU_N
GPP_D7/SRCCLKREQ2# DT30 WWAN_CLKREQ_CPU_N
GPP_D6/SRCCLKREQ1# DV30 GFX_CLKREQ_CPU_N
GPP_D5/SRCCLKREQ0# DW30
XTAL_OUT DM1 XTL_38D4M_X2_CPU
XTAL_IN DL1 XTL_38D4M_X1_CPU
GPD8/SUSCLK DW41 SUSCLK
RTCX2 DT47 XTL_32K_X2_CPU
RTCX1 DR47 XTL_32K_X1_CPU
RTCRST# DN37 RTC_RST#
SRTCRST# DK37 SRTC_RST#
TGL-U-1-GP-U1
ZZ.00CPU.481

R1826 2 1 60D4R2F-GP XCLK_BIASREF

3D3V_S0
RN1805 SRN20KJ-4-GP
CARD_CLKREQ_CPU_N
WWAN_CLKREQ_CPU_N
WLAN_CLKREQ_CPU_N
SSD_CLKREQ_CPU_N
R18221 20KR2J-2-GP LAN_CLKREQ_CPU_N
R18241 20KR2J-2-GP SSD2_CLKREQ_CPU_N
R18281 20KR2J-2-GP GFX_CLKREQ_CPU_N
R18291 10KR2F-2-GP SECURE_BIO
SUSCLK R18171 Do Not Stuff DY

3D3V_S5
R1812 100KR2F-L1-GP
TPM_ID
R1816 100KR2F-L1-GP
NUVOTON

XTL_38D4M_X1_CPU
XTL_38D4M_X2_CPU
R1827 200KR2F-L-GP
R1806 0R2J-2-GP
R1805 0R2J-2-GP
XTL_38D4M_X2_CPU_R
XTL_38D4M_X1_CPU_R
C1806 C1805 SC15P50V2JN-DL-GP
X1803 XTAL-38D4MHZ-37-GP
INPUT/OUTPUT#3 NC#2 INPUT/OUTPUT#1
082.30040.0251

3D3V_S5_PCH
R18021 Do Not Stuff DY GPP_C2
1D8V_S5
R18031 4K7R2J-2-GP GPP_C2
R18041 Do Not Stuff DY GPP_B23

3D3V_S5_PCH
SML0_SMBCLK R18071 499R2F-2-GP
SML0_SMBDATA R18081 499R2F-2-GP
RN1804 SRN2K2J-1-GP
SML1_SMBCLK
SML1_SMBDATA
MEM_SMBCLK
MEM_SMBDATA
RN1806 SRN1KJ-7-GP

SPI_CLK_CPU R18091 100KR2F-L1-GP
ESPI_RESET# R18131 75KR2J-GP
ESPI_CS# R1814 Do Not Stuff DY

3D3V_S5_PCH
R1820 100KR2F-L1-GP
NON_VPRO
VPRO_DET#
R1821 100KR2F-L1-GP
VPRO

3D3V_RTC_PCH
RN1802 SRN20KJ-1-GP
C1801 SC1U10V2KX-1DLGP
SRTC_RST#
RTC_RST#
G1802 Do Not Stuff
C1802 SC1U10V2KX-1DLGP

ESPI_CPU_CLK_R R1834 49D9R2F-GP ESPI_CLK
ESPI_CPU_IO0_R R1835 15R2F-2-GP ESPI_IO0
ESPI_CPU_IO1_R R1836 15R2F-2-GP ESPI_IO1
ESPI_CPU_IO2_R R1838 15R2F-2-GP ESPI_IO2
ESPI_CPU_IO3_R R1850 15R2F-2-GP ESPI_IO3
Intel requst set as PDG .

RF Reserve
ESPI_CLK
FC1802 Do Not Stuff DY

XTL_32K_X2_CPU
XTL_32K_X1_CPU
R1815 10MR2J-L-GP
C1804 C1803 SC15P50V2JN-DL-GP
X1802 XTAL-32D768KHZ-98-GP
082.30003.0301

RTCRST_ON R1844 0R2J-2-GP
RTCRST_ON_Q
Q1802 2N7002K-2-GP
RTC_RST#_R R1852 75R2F-2-GP RTC_RST#
R1846 100KR2F-L1-GP
84.2N702.J31
ARD 0.85

3D3V_S0
RN1803 SRN2K2J-1-GP
MEM_SMBDATA
Q1803 2N7002KDW-1-GP
75.27002.F7C
CPU_SMB_SDA_DDR
CPU_SMB_SCL_DDR
MEM_SMBCLK

Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (SPI/ESPI/SMBS/XTAL/CLK)**
Size: A2 | Document Number: **SouthPeak15 TGL** | Rev: **SB**
Date: Friday, April 24, 2020 | Sheet 18 of 106

Main Func = PCH

ME_FWP_PCH 1 — R1904 1KR2J-1-GP — 2 HDA_SDO

27,96 HDA_SDI0
27 HDA_SDOUT_CODEC
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
15 HDA_SDO
HDA_RST#
PCH_BT_RADIO_DIS#
CLKREQ_CNV
DGPU_PWROK
55 TOUCH_SCREEN_RST#_R
61 CNV_EN#
68 ME_FWP_PCH
CNV_RF_RESET#
55 BLON_OUT_R
96 HDA_BCLK
DGPU_HOLD_RST#

HDA_BITCLK_CODEC 1 R1914 33R2F-3-GP 2 — 27
HDA_SYNC_CODEC 1 R1915 33R2F-3-GP 2 — 61
HDA_SDOUT_CODEC 1 R1916 33R2F-3-GP 2 — 61
HDA_RST# 1 R1917 33R2F-3-GP 2 — 24
DY EC1902 Do Not Stuff

R1919 200R2F-L-GP 2 1 — 61

7 OF 21 — CPU1G

HDA_BCLK	DR38	GPP_R0/HDA_BCLK/I2S0_SCLK
HDA_SYNC	DU37	GPP_R1/HDA_SYNC/I2S0_SFRM
HDA_SDO	DT37	GPP_R2/HDA_SDO/I2S0_TXD
HDA_SDI0	DV37	GPP_R3/HDA_SDI0/I2S0_RXD
HDA_RST#	DV41	GPP_R4/HDA_RST#
CNV_EN#	DL53	GPP_A7/I2S2_SCLK/DMIC_CLK_A0
CNV_RF_RESET#	DG51	GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
TOUCH_SCREEN_RST#	DG50	GPP_A10/I2S2_RXD/DMIC_DATA1
CLKREQ_CNV_R	DL49	GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
AUD_PWR_EN	DL52	GPP_A11/PMC_I2C_SDA/I2S3_SCLK
PCH_BT_RADIO_DIS#	DH49	GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0
SNDW_RCOMP	DF33	SNDW_RCOMP

GPP_F8_I2S_MCLK2_INOUT	DW15	DGPU_PWROK
GPP_D19/I2S_MCLK1	DW24	BLON_OUT_R
GPP_A23/I2S1_SCLK	DG41	
GPP_R7/I2S1_SFRM	DT38	
GPP_R6/I2S1_TXD	DV38	
GPP_R5/HDA_SDI1/I2S1_RXD	DW38	PROJECT_ID1
GPP_S6/SNDW3_CLK/DMIC_CLK_A0	DN31	GPP_S6 1 — TP1901
GPP_S7/SNDW3_DATA/DMIC_DATA0	DM31	GPP_S7 1 — TP1902
GPP_S4/SNDW2_CLK/DMIC_CLK_A1	DK33	PROJECT_ID2
GPP_S5/SNDW2_DATA/DMIC_DATA1	DK31	DGPU_HOLD_RST#
GPP_S2/SNDW1_CLK/DMIC_CLK_B0	DW35	
GPP_S3/SNDW1_DATA/DMIC_CLK_B1	DV35	
GPP_S0/SNDW0_CLK	DT32	
GPP_S1/SNDW0_DATA	DR35	

TGL-U-1-GP-U1

ZZ.00CPU.481

CLKREQ_CNV_R 1 R1912 33R2F-3-GP 2 CLKREQ_CNV

TOUCH_SCREEN_RST#_R 1 R1901 100R2F-L1-GP-U 2 TOUCH_SCREEN_RST#

3D3V_S0
R1908 1 — 2 100KR2F-L-GP AUD_PWR_EN

HDA_BCLK
DY EC1901 Do Not Stuff

1D8V_S5_VCCPRIM
R1934 10KR1J-GP — 15P OPS — PROJECT_ID2
R1935 10KR2J-3-GP — 15/15P UMA

3D3V_S0
R1936 10KR1J-GP — UMA — PROJECT_ID1
R1937 10KR1J-GP — OPS

	15 (i3, i5, i7)		15P (i5, i7)	
	UMA	DSC (N15S-G5)	UMA	DSC (QN20-M1)
Accelerometer sensor on MB	LNG2DMTR (8-bit)	LNG2DMTR	LNG2DMTR	LIS2DW12TR (16-bit)
GPP_R5 (PROJECT_ID1)	1	0	1	0
GPP_S4 (PROJECT_ID2)	0	0	0	1

Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HDA/I2S/SD/DMIC)

Size: A3 | Document Number: SouthPeak15 TGL | Rev: SB

Date: Friday, April 24, 2020 | Sheet 19 of 106

Main Func = PCH

CPU_UART2_TXD
CPU_UART2_RXD
CPU_I2C_SDA_TS
CPU_I2C_SCL_TS
CPU_I2C_SDA_TP
CPU_I2C_SCL_TP
SPKR
SMBUS_I2C_SDA_SENSOR
SMBUS_I2C_SCL_SENSOR
P_SENSOR_PWR_SAVE#_1P8
CPU_I2C_SDA_GNSS
CPU_I2C_SCL_GNSS
GSEN_INT1
LNG2DMTR_INT1
NB_MODE#
LID_CL#_NB_R
P_CLK
P_DATA
TPM_PIRQ#
PCH_TOUCH_SCREEN_EN
ISH_P_SENSOR_INT#_1P8
ISH_ALS_INT#
LCD_CBL_DET#
SBIOS_TX
ISH_TABLE_MODE#
CAM_MIC_CBL_DET#
IR_CAM_DET#
SML0B_SMBDATA
SML0B_SMBCLK
HOST_SD_WP#
WWAN_FULL_PWR_EN_R
DGPU_PWR_EN
CNV_MFUART2_TXD
CNV_MFUART2_RXD

CPU1I 6 OF 21

ONE_DIMM#
NRB_BIT
HOST_SD_WP#
SPKR
SPK_DET#
LCD_CBL_DET#
PCH_TOUCH_SCREEN_EN
SBIOS_TX
WWAN_FULL_PWR_EN
P_SENSOR_PWR_SAVE#_1P8
TP2001
TP2002
TP2003
PCH_SSD_PWR_EN
2.7MM_CAM_DET#
IR_CAM_DET#
TPM_PIRQ#
CPU_UART2_TXD
CPU_UART2_RXD
TS_I2C_SCL
TS_I2C_SDA
I2C1_SCK_TP
I2C1_SDA_TP
DDR_CHB_EN_1P8
DDR_CHA_EN_1P8
CAM_MIC_CBL_DET#
SPK_DET1#
CNV_MFUART2_TXD
CNV_MFUART2_RXD

GPP_B16/GSPI0_CLK
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
GPP_B15/GSPI0_CS0#
GPP_B20/GSPI1_CLK
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B19/GSPI1_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_H5/I2C2_SCL
GPP_H4/I2C2_SDA
GPP_H7/I2C3_SCL
GPP_H6/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

TGL-U-1-GP-U1
ZZ.00CPU.481

Circuit not ready
Need confirm with Dell

GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5
GPP_B6/ISH_I2C0_SCL
GPP_B5/ISH_I2C0_SDA
GPP_B8/ISH_I2C1_SCL
GPP_B7/ISH_I2C1_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_E16/ISH_GP7
GPP_E15/ISH_GP6
GPP_D18/ISH_GP5
GPP_D17/ISH_GP4
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCOMP
GPP_T3/I2C7_SCL
GPP_T2/I2C7_SDA
GPP_U5/GSPI3_CLK
GPP_U4/GSPI3_CS0#

SML0B_SMBCLK
SML0B_SMBDATA
SML0BALERT#
DGPU_PWR_EN
ISH_I2C0_SCL
ISH_I2C0_SDA
ISH_I2C1_SCL
ISH_I2C1_SDA
ISH_I2C2_SCL
ISH_I2C2_SDA
ISH_P_SENSOR_INT#_1P8
ISH_LID_CL#_TAB
ISH_LID_CL#_NB
ISH_NB_MODE
ISH_ALS_INT#
ISH_TABLE_MODE#
ISH_ACC2_INT#
ISH_ACC1_INT#
GPP_RCOMP
SENSOR
ALS
WWAN

Circuit not ready
Do Not Stuff
LID_CL#_TAB_R
LID_CL#_NB_R
LNG2DMTR_INT1
GSEN_INT1
200R2F-L-GP

1D8V_S0
R2030 10KR2F-2-GP ISH_ALS_INT#

3D3V_S5_PCH
R2003 49K9R2F-L-GP CPU_UART2_RXD
R2005 49K9R2F-L-GP CPU_UART2_TXD
DEBUG

3D3V_S0
R2041 100KR2F-L1-GP CAM_MIC_CBL_DET#

RN2002 SRN2K2J-1-GP
R2014 0R2J-2-GP TS_I2C_SDA CPU_I2C_SDA_TS
R2015 0R2J-2-GP TS_I2C_SCL CPU_I2C_SCL_TS
R2025 0R2J-2-GP I2C1_SDA_TP CPU_I2C_SDA_TP
R2024 0R2J-2-GP I2C1_SCK_TP CPU_I2C_SCL_TP
R2008 0R2J-2-GP WWAN_FULL_PWR_EN_R WWAN_FULL_PWR_EN

RN2006 Do Not Stuff
R2022 Do Not Stuff ISH_I2C2_SDA CPU_I2C_SDA_GNSS
R2023 Do Not Stuff ISH_I2C2_SCL CPU_I2C_SCL_GNSS
R2032 0R2J-2-GP CPU_I2C_SDA_SENSOR ISH_I2C0_SDA
R2031 0R2J-2-GP CPU_I2C_SCL_SENSOR ISH_I2C0_SCL

R2038 0R2J-2-GP ISH_NB_MODE NB_MODE#
R2009 100KR2F-L1-GP
R2013 Do Not Stuff ONE_DIMM#
R2011 100KR2J-1-GP
R2036 4K7R2J-2-GP NRB_BIT

DIMM Dectect	
HIGH	1 DIMM
LOW	2 DIMM

For N18S-G5
R2027 2 0PS 1 10KR1J-GP DGPU_PWR_EN

1D8V_S0
RN2003 SRN2K2J-1-GP
P_CLK R2033 0R2J-2-GP ISH_I2C1_SCL
P_DATA R2034 0R2J-2-GP ISH_I2C1_SDA

3D3V_S0
R2021 10KR2F-2-GP LID_CL#_NB_R
R2020 Do Not Stuff LID_CL#_TAB_R
R2007 100KR2F-L1-GP LCD_CBL_DET#
R2028 10KR2F-2-GP GSEN_INT1
R2029 10KR2F-2-GP LNG2DMTR_INT1
R2016 100KR2F-L1-GP IR_CAM_DET#
R2001 10KR2F-2-GP HOST_SD_WP#
RN2001 ISH_I2C1_SDA ISH_I2C1_SCL
Do Not Stuff

3D3V_S5_PCH
R2010 1KR2J-1-GP SML0B_SMBCLK
R2012 1KR2J-1-GP SML0B_SMBDATA
R2017 Do Not Stuff SML0BALERT#

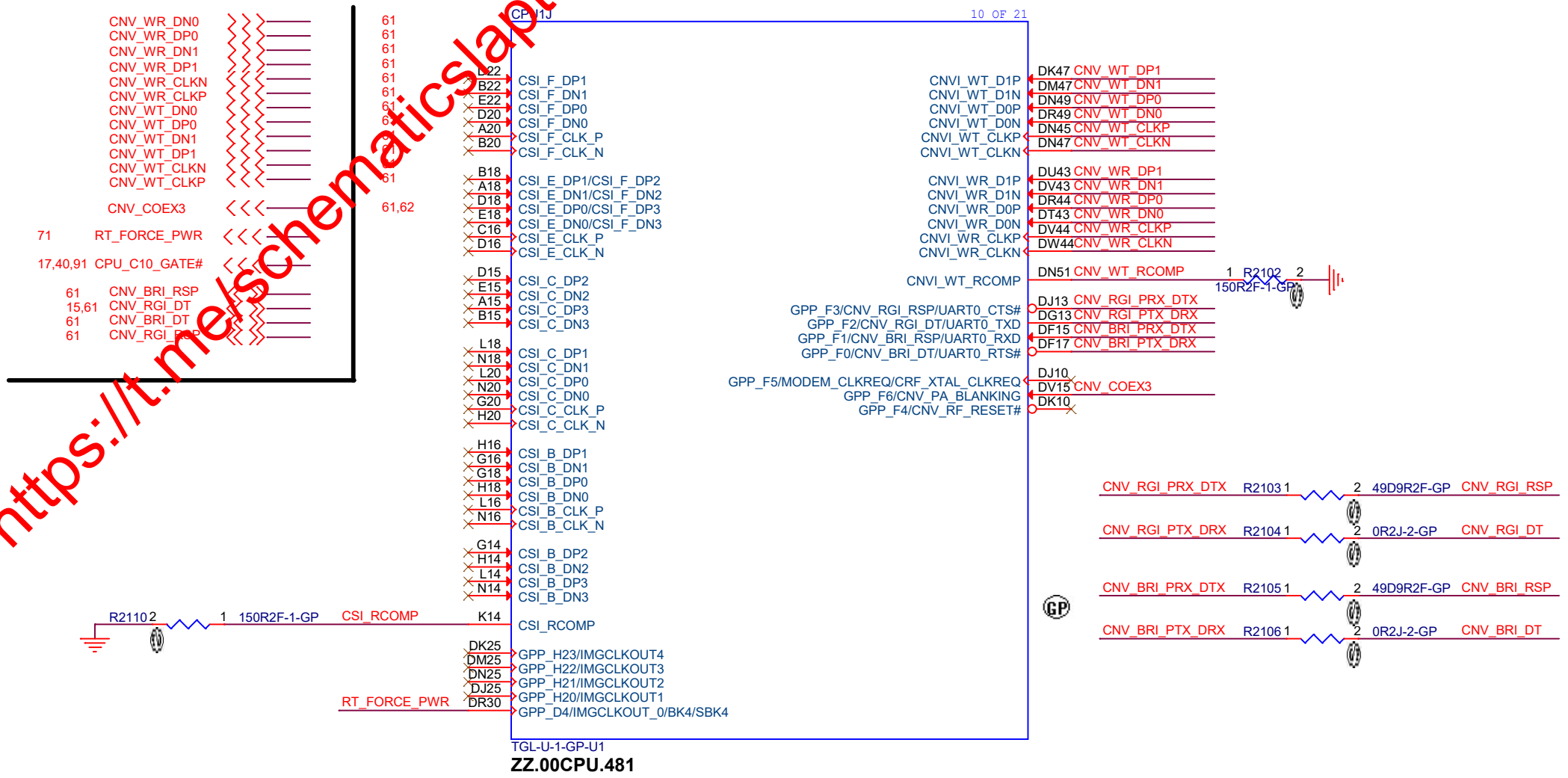
1D8V_S5_VCCPRIM
R2039 10KR2F-2-GP ISH_P_SENSOR_INT#_1P8
R2040 10KR2F-2-GP P_SENSOR_PWR_SAVE#_1P8

Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A2
Document Number: SouthPeak15 TGL
Rev: SB
Date: Friday, April 24, 2020
Sheet 20 of 106

Main Func = PCH



Multi

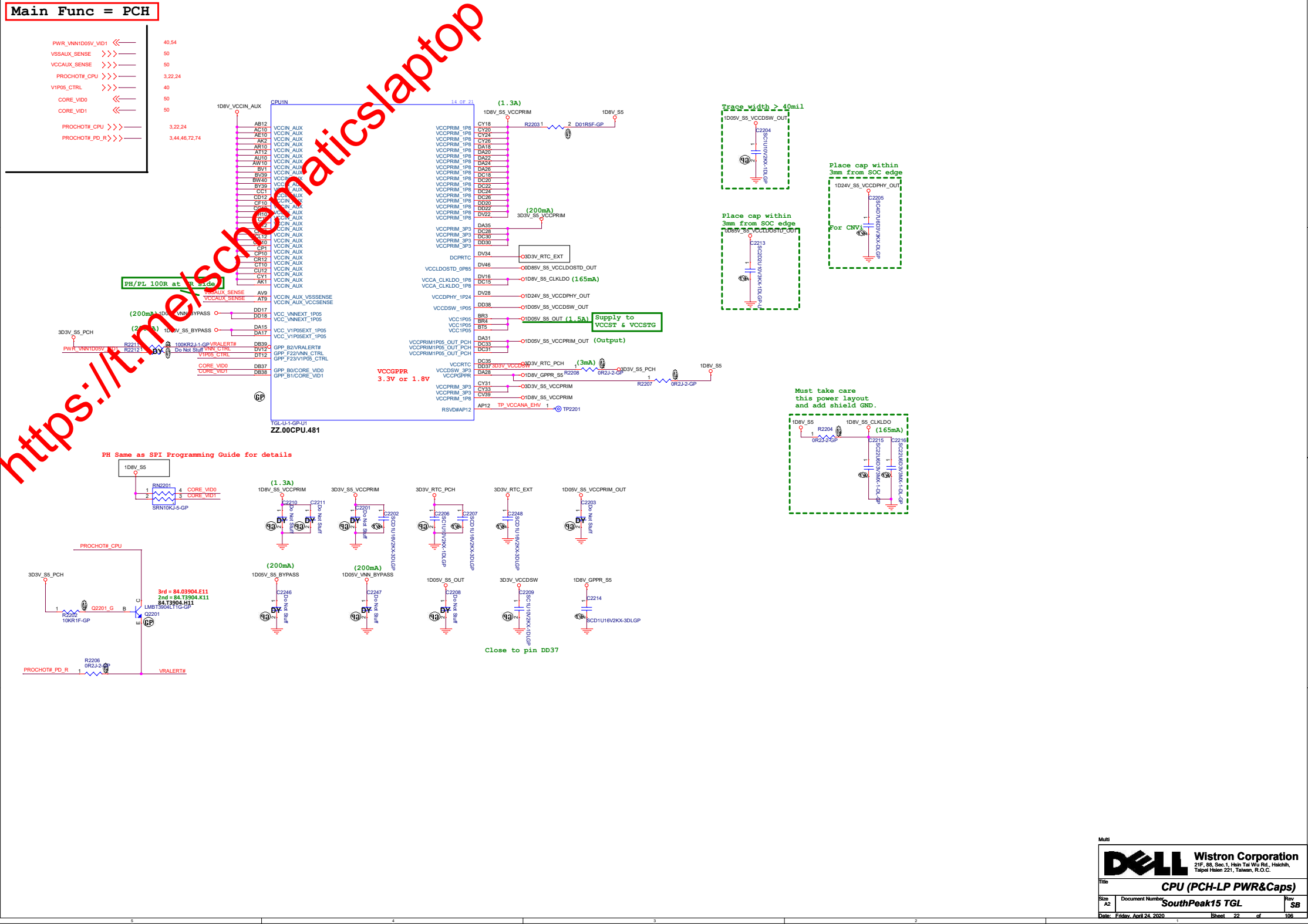
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (EMMC/CNVi)

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 21 of 106

Main Func = PCH



Main Func = PCH

CPU1P 16 OF 21

A27	VSS	VSS	B19
A32	VSS	VSS	B2
A45	VSS	VSS	B23
A49	VSS	VSS	B27
AA41	VSS	VSS	B32
AA48	VSS	VSS	B36
AB5	VSS	VSS	B39
AB7	VSS	VSS	B42
AB8	VSS	VSS	B48
AC44	VSS	VSS	B52
AC49	VSS	VSS	B8
AD4	VSS	VSS	BA48
AD48	VSS	VSS	BA53
AD8	VSS	VSS	BB4
AF4	VSS	VSS	BB8
AF8	VSS	VSS	BC1
AG41	VSS	VSS	BC2
AG42	VSS	VSS	BD12
AG44	VSS	VSS	BD4
AG45	VSS	VSS	BD48
AG47	VSS	VSS	BD8
AG48	VSS	VSS	BF39
AG53	VSS	VSS	BF4
AH4	VSS	VSS	BF41
AH8	VSS	VSS	BF42
AK12	VSS	VSS	BF44
AK4	VSS	VSS	BF45
AK48	VSS	VSS	BF47
AK5	VSS	VSS	BF5
AK7	VSS	VSS	BF7
AK8	VSS	VSS	BF8
AM1	VSS	VSS	BG48
AM2	VSS	VSS	BG53
AM4	VSS	VSS	BH1
AM8	VSS	VSS	BH2
AN41	VSS	VSS	BH4
AN42	VSS	VSS	BH8
AN44	VSS	VSS	BK12
AN45	VSS	VSS	BK4
AN47	VSS	VSS	BK48
AN48	VSS	VSS	BK8
AN53	VSS	VSS	BL49
AP4	VSS	VSS	BM1
AP8	VSS	VSS	BM4
AT4	VSS	VSS	BM41
AT48	VSS	VSS	BM42
AT51	VSS	VSS	BM44
AT8	VSS	VSS	BM45
AV12	VSS	VSS	BM47
AV39	VSS	VSS	BM8
AV4	VSS	VSS	BN48
AV5	VSS	VSS	BP41
AV7	VSS	VSS	BP49
AV8	VSS	VSS	BP5
AW1	VSS	VSS	BP50
AW2	VSS	VSS	BP7
AW48	VSS	VSS	BT44
AY4	VSS	VSS	BT48
AY41	VSS	VSS	BU49
AY42	VSS	VSS	BV3
AY44	VSS	VSS	BV48
AY45	VSS	VSS	BV5
AY47	VSS	VSS	BW10
AY8	VSS	VSS	BY41
AY9	VSS	VSS	BY42
B13	VSS	VSS	

GP

TGL-U-1-GP-U1

ZZ.00CPU.481

CPU1R 18 OF 21

K34	VSS	DP53
K48	VSS	DR11
K5	VSS	DR16
L22	VSS	DR22
L28	VSS	DR28
L34	VSS	DR34
L39	VSS	DR40
L41	VSS	DR46
L42	VSS	DT4
L44	VSS	DT50
L45	VSS	DU11
L47	VSS	DU16
L49	VSS	DU22
M1	VSS	DU28
M2	VSS	DU34
M50	VSS	DU40
N22	VSS	DU46
N28	VSS	DV1
N34	VSS	DV40
N39	VSS	DV52
N41	VSS	DW51
N48	VSS	E13
P11	VSS	E19
P14	VSS	E35
P16	VSS	E48
P18	VSS	G22
P20	VSS	G28
P22	VSS	G34
P33	VSS	G39
P35	VSS	G48
P4	VSS	G51
P49	VSS	G52
P8	VSS	H12
R39	VSS	H22
R44	VSS	H28
T19	VSS	H34
T29	VSS	H8
T33	VSS	J39
T4	VSS	J49
T48	VSS	K16
T8	VSS	K18
U19	VSS	K20
U25	VSS	K22
U39	VSS	K28
U49	VSS	
V19	VSS	
V4	VSS	
V8	VSS	
W1	VSS	
W16	VSS	
W26	VSS	
W30	VSS	
W39	VSS	
W41	VSS	
W42	VSS	
W44	VSS	
W45	VSS	
W47	VSS	
W48	VSS	
Y4	VSS	
Y49	VSS	
Y50	VSS	
Y8	VSS	

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TGL-U-1-GP-U1

ZZ.00CPU.481

CPU1Q 17 OF 21

BY44	VSS	CY44
BY45	VSS	CY45
BY47	VSS	CY47
BY49	VSS	CY5
BY9	VSS	D27
C13	VSS	D32
C19	VSS	D36
C23	VSS	D42
CA48	VSS	D49
CB41	VSS	D5
CC10	VSS	DA30
CC3	VSS	DA33
CC5	VSS	DA53
CD44	VSS	DC17
CD48	VSS	DD15
CD7	VSS	DD24
CE49	VSS	DD26
CG48	VSS	DD28
CG51	VSS	DD31
CG52	VSS	DD33
CG9	VSS	DD35
CH41	VSS	DD39
CH42	VSS	DD45
CH44	VSS	DD51
CH45	VSS	DD52
CH47	VSS	DE3
CJ3	VSS	DE5
CJ5	VSS	DF19
CJ9	VSS	DF37
CK39	VSS	DG15
CK48	VSS	DG21
CK53	VSS	DG27
CL9	VSS	DG33
CN12	VSS	DG39
CN48	VSS	DG45
CN51	VSS	DG5
CN52	VSS	DG53
CN9	VSS	DG6
CP3	VSS	DJ1
CP41	VSS	DJ2
CP42	VSS	DJ4
CP44	VSS	DK51
CP45	VSS	DL3
CP5	VSS	DL5
CR48	VSS	DM10
CR53	VSS	DM15
CR9	VSS	DM21
CT5	VSS	DM27
CU4	VSS	DM33
CU9	VSS	DM39
CV10	VSS	DM4
CV48	VSS	DM45
CV5	VSS	DN1
CV51	VSS	DN2
CV52	VSS	
CY17	VSS	
CY22	VSS	
CY35	VSS	
CY41	VSS	
CY42	VSS	

GP

TGL-U-1-GP-U1

ZZ.00CPU.481

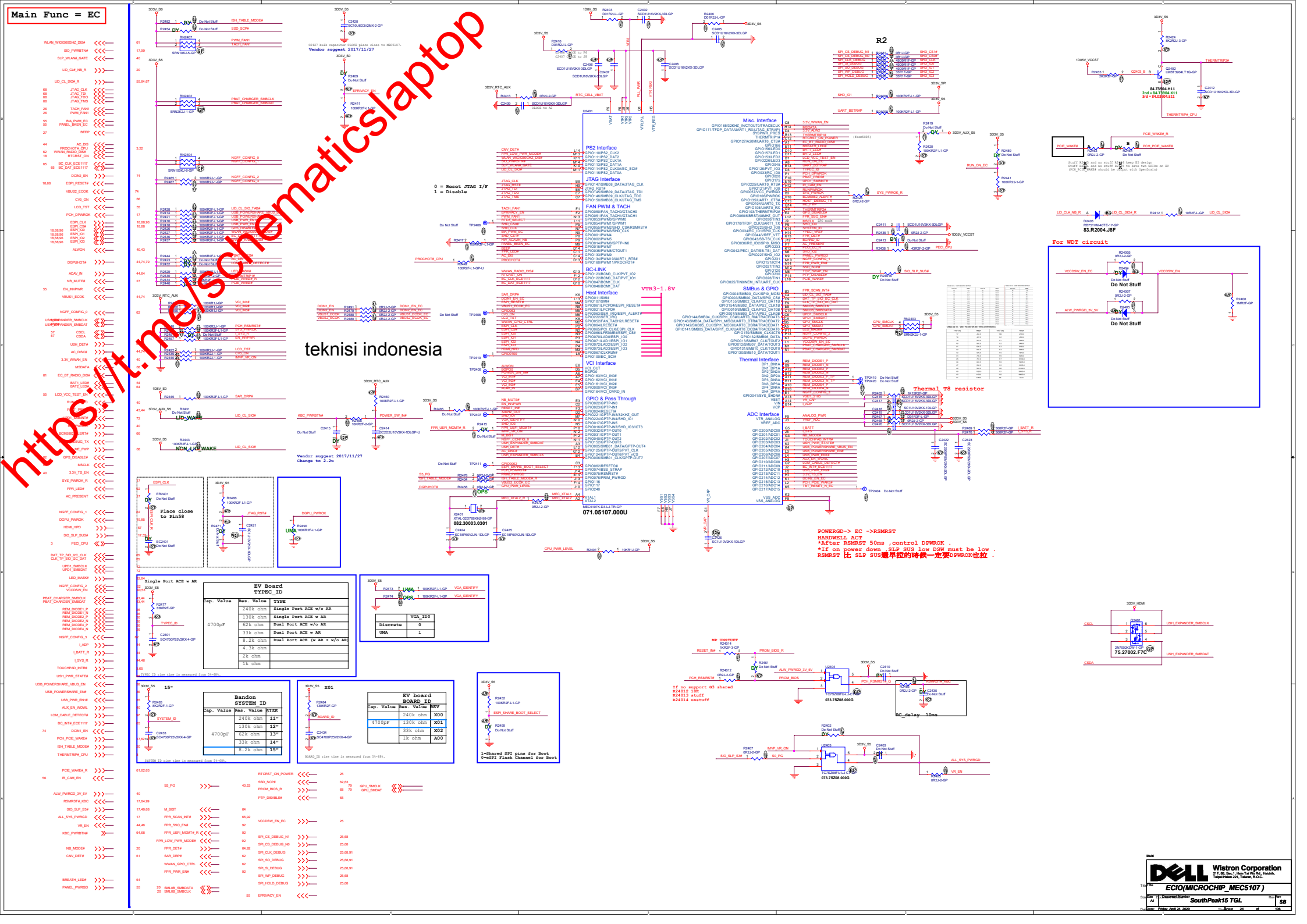
Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VSS)**

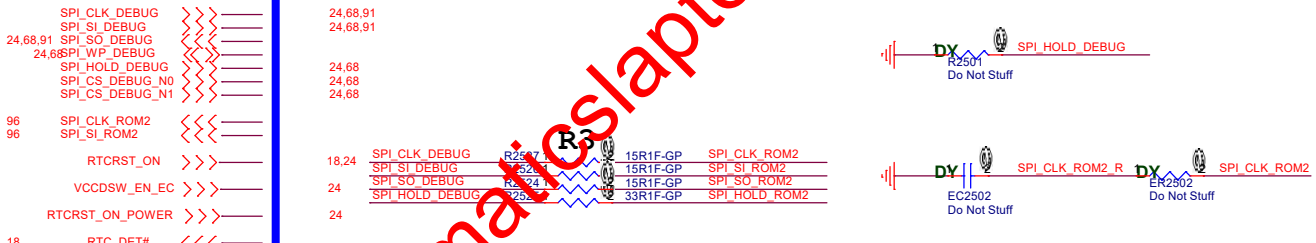
Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 23 of 106

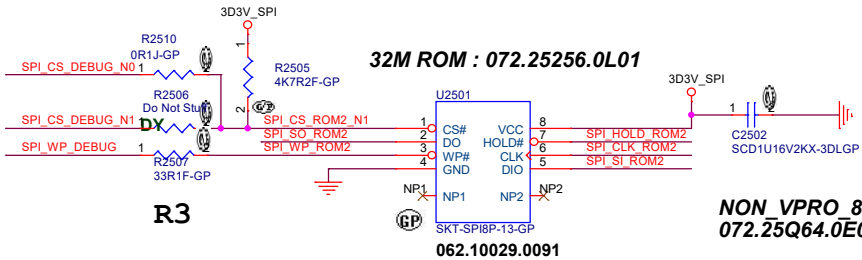

Main Func = EC
https://t.me/schematicslaptop
teknisi indonesia
0 = Reset JTAG I/F
1 = Disable
VTR3-1.8V
Misc. Interface
PS2 Interface
JTAG Interface
FAN PWM & TACH
BC-LINK
Host Interface
VCI Interface
GPIO & Pass Through
ADC Interface
SMBus & GPIO
Thermal Interface
Thermal T8 resistor
For WDT circuit
Do Not Stuff
Place close to Pin58
LID_WAKE
NON_LID_WAKE
Vendor suggest 2017/11/27
Change to 2.2u
Vendor suggest 2017/11/27
EV Board TYPEC_ID
Cap. Value
Res. Value
TYPE
4700pF
240k ohm
Single Port ACE w/o AR
130k ohm
Single Port ACE w AR
62k ohm
Dual Port ACE w/o AR
33k ohm
Dual Port ACE w AR
8.2k ohm
Dual Port ACE (w AR + w/o AR)
4.3k ohm
2k ohm
1k ohm
Single Port ACE w AR
Bandon SYSTEM_ID
SIZE
11"
12"
13"
14"
15"
EV board BOARD_ID
REV
X00
X01
X02
A00
VGA_ID0
Discrete
0
UMA
1
1=Shared SPI pins for Boot
0=eSPI Flash Channel for Boot
If no support G3 shared
R24012 10K
R24013 stuff
R24014 unstuff
POWERGD-> EC ->RSMRST
HARDWELL ACE
*After RSMRST 50ms ,control DPWROK .
*If on power down ,SLP SUS low DSW must be low .
RSMRST 比 SLP SUS還早拉的時候一定要DPWROK也拉 .
R2
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.23004.211
83.R2004.J8F
MP UNSTUFF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ECIO(MICROCHIP_MEC5107)
SouthPeak15 TGL
Friday, April 24, 2020

Main Func = BIOS ROM/RTC

SYSTEM SPI ROM



Vpor-WSON-32MB
Non_Vpor-WSON-8MB



32M ROM : 072.25256.0L01

NON_VPRO_8MB 手動換料
072.25Q64.0E03

Non-vPRO configs - 16MB (UI)
Winbond W25Q128JVSIQ; MXIC: MX25L12873FM; GigaDevice: GD25B127D
If more than 3 sources are required then these parts can be considered:
Spansion: S25FL128L; Micron: MT25QL128ABA1ESE-0SIT

vPRO Configs: 32MB
Winbond W25Q256JV, Gigadevice GD25Q256C, Cypress S25FL256L

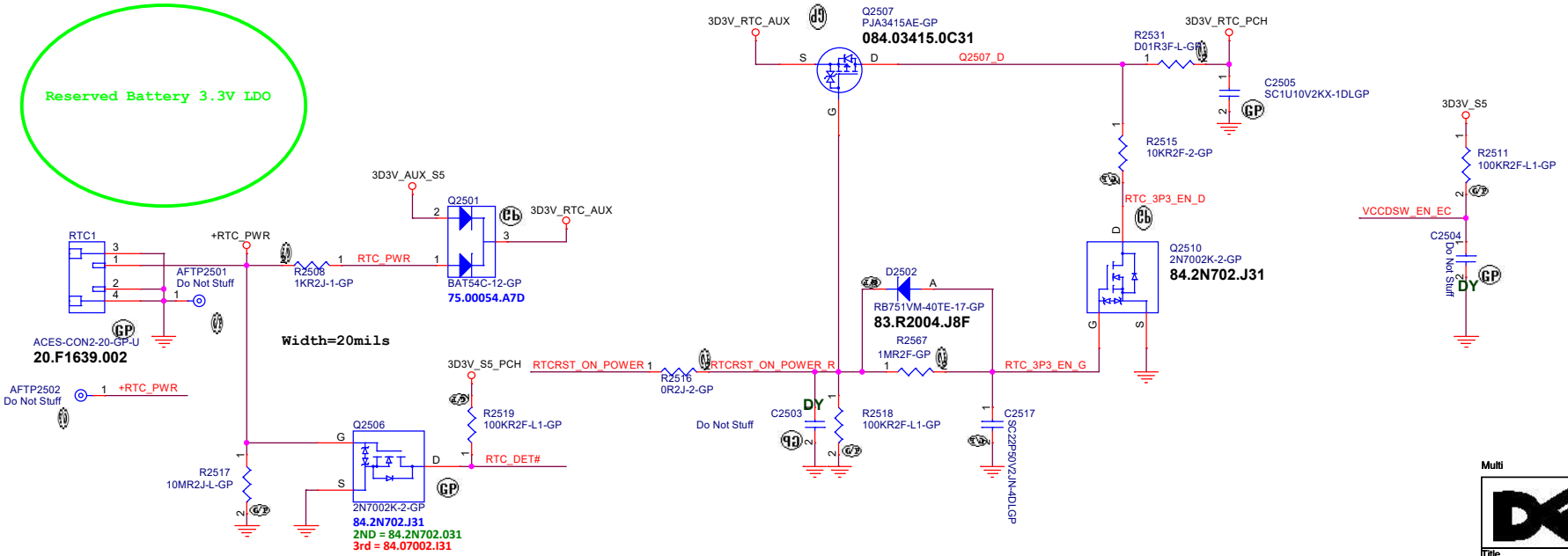
WinBond		WSON (8x6)		8-Pin SOIC 208-mil	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.25Q64.0E03	W25Q64JVZEIQ	072.25Q64.0H01	W25Q64JVSSIQ
16 M Byte	128 M bit	072.25128.0A11	W25Q128JVEIQ	072.25128.0B51	W25Q128JVSIQ
32 M Byte	256 M bit	072.25256.0N01	W25Q256JVEIQ		N/A

MXIC		WSON (8x6)		8-pin SOP (200mil)	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.25643.0B01	MX25L6433FZ2I	072.25647.000D	MX25L6473FM2I-08G
16 M Byte	128 M bit	XX	XX	72.12873.001	MX25L12873FM2I-10G
32 M Byte	256 M bit	072.25673.0003	MX25L25673GZ4I-08G	072.25673.0001	MX25L25673GM2I-08G

GIGADEVICE		WSON (8x6)		SOP8 208MIL	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.02564.0F01	GD25B64CYIGR	072.25B64.0C01	GD25B64CSIGR
16 M Byte	128 M bit			072.25127.0001	GD25B127DSIGR
32 M Byte	256 M bit	072.25656.0B03	GD25B256DYIGR		

X09 design DS3_Non-DS3 with RTC power gating

Reserved Battery 3.3V LDO



Multi

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Title: Flash/RTC		
Size: A3	Document Number: SouthPeak15 TGL	Rev: SB
Date: Friday, April 24, 2020	Sheet 25 of 106	

Main Func = Thermal / FAN

5105 Channel	Location
DP1/DN1	CPU (Q2601)
DP2/DN2	WWAN (Q2602)
DN2a/DP2a	DDR (Q2603)
DP4/DN4	V.R (Q2605)

REM_DIODE1_P
REM_DIODE1_N
REM_DIODE2_P
REM_DIODE2_N
REM_DIODE4_P
REM_DIODE4_N
PWM_FAN1
TACH_FAN1

24

24 24 24 24 Q2601 LMBT3904LT1G-GP 84.T3904.H11 2nd = 84.T3904.K11 3rd = 84.03904.E11

C2601 Do Not Stuff

C2602 SC2200P50V2KX-2DLGP

REM_DIODE1_P / REM_DIODE1_N

Layout Note: Place to CPU
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

Layout Note: Close to WWAN/2nd SSD

C2604 Do Not Stuff

Q2603 LMBT3904LT1G-GP 84.T3904.H11 3rd = 84.03904.E11 2nd = 84.T3904.K11

C2603 Do Not Stuff

Q2602 LMBT3904LT1G-GP 84.T3904.H11 2nd = 84.T3904.K11 3rd = 84.03904.E11

C2605 SC2200P50V2KX-2DLGP

REM_DIODE2_P / REM_DIODE2_N

Layout Note:Place to DIMM
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

Q2605 LMBT3904LT1G-GP 84.T3904.H11 2nd = 84.T3904.K11 3rd = 84.03904.E11

C2610 Do Not Stuff

C2609 SC2200P50V2KX-2DLGP

REM_DIODE4_P / REM_DIODE4_N

Layout Note:Place to V.R
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

3D3V_S0

U2601

PWM_FAN1 → PWM_FAN1_Q

TACH_FAN1_Q → TACH_FAN1

2N7002KDW-1-GP
75.27002.F7C

5V_S0

RN2601 SRN10KJ-5-GP **FAN**

AFTP2601 Do Not Stuff

C2608 SC4D7U6D3V3KX-DLGP

TACH_FAN1_Q
PWM_FAN1_Q

FAN1 ACES-CON4-29-GP
20.F1639.004
2nd:020.F0097.0004

Layout Note:
Signal Routing Guideline:
Trace width = 15mil

TACH_FAN1_Q
PWM_FAN1_Q
AFTP2602 Do Not Stuff
AFTP2603 Do Not Stuff

Multi

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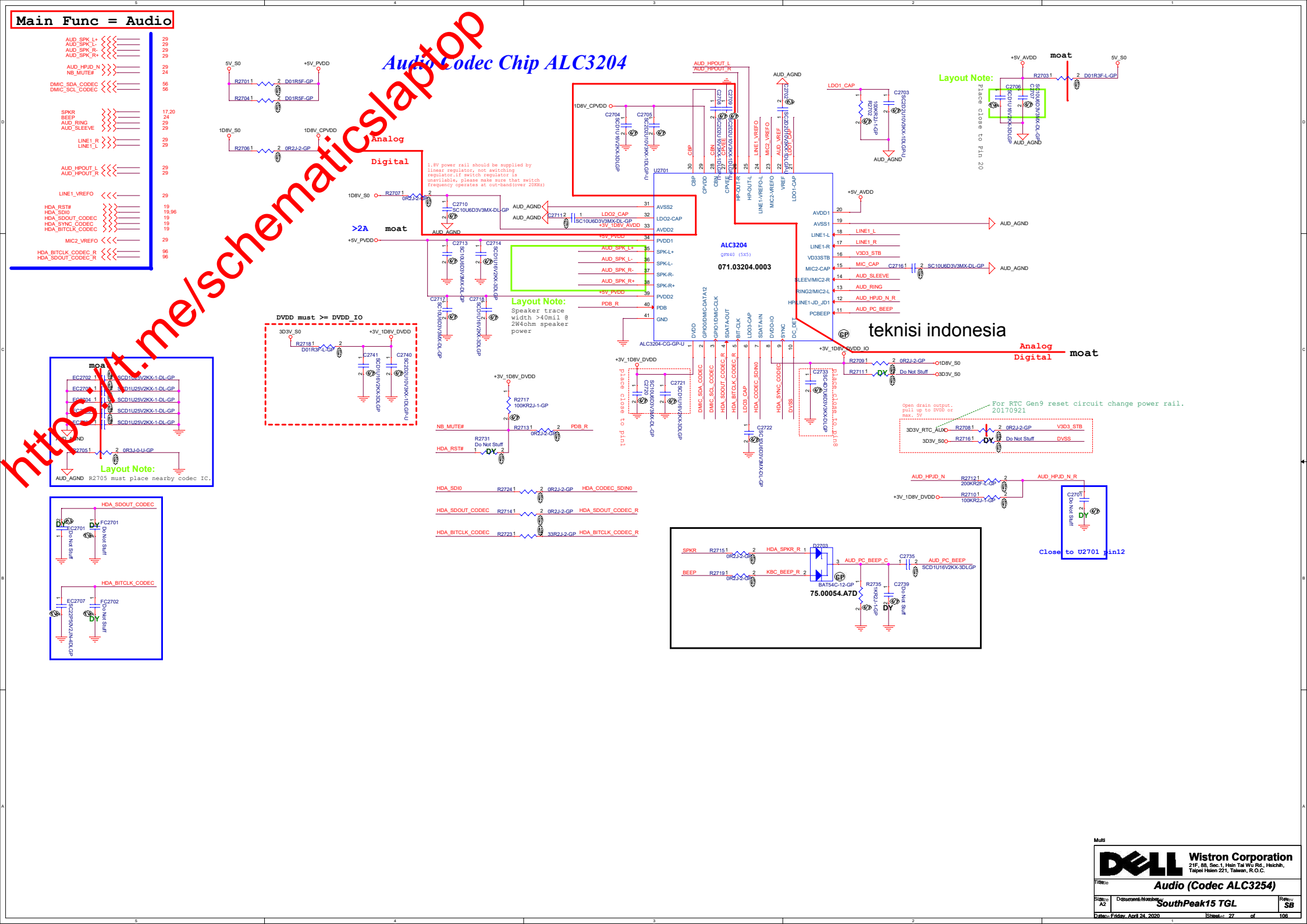
Title: INT IO (Thermal/Fan)

Size: A4 | Document Number: SouthPeak15 TGL | Rev: SB

Date: Friday, April 24, 2020 | Sheet 26 of 106

Main Func = Audio

Audio Codec Chip ALC3204



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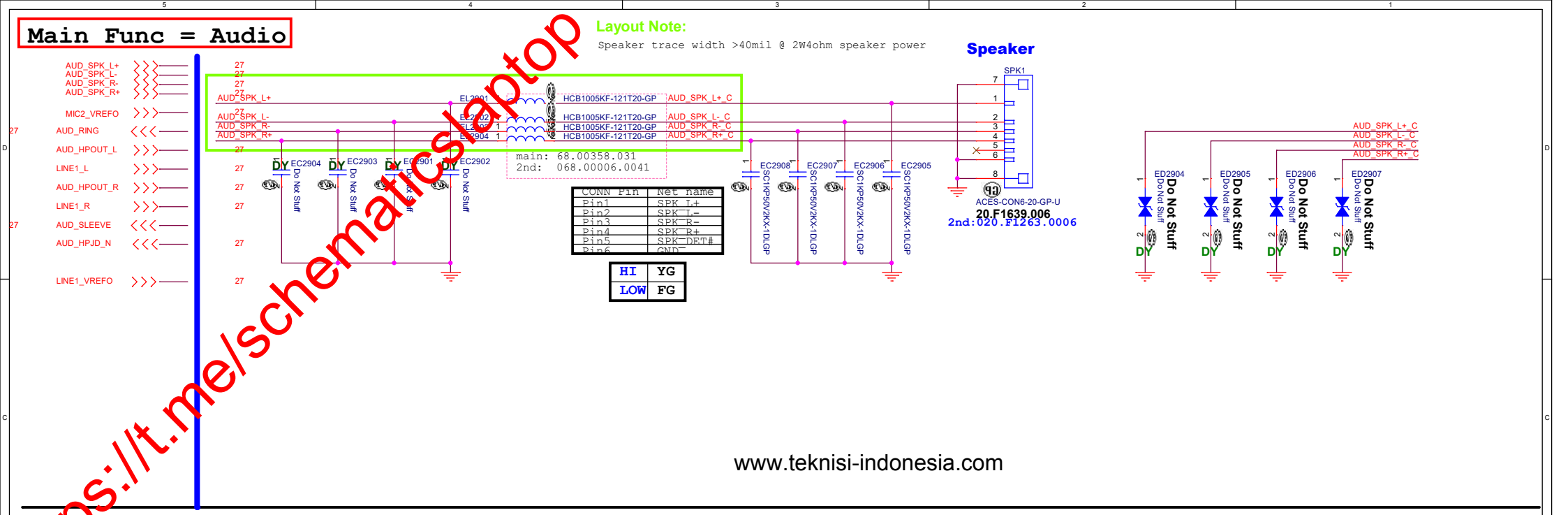
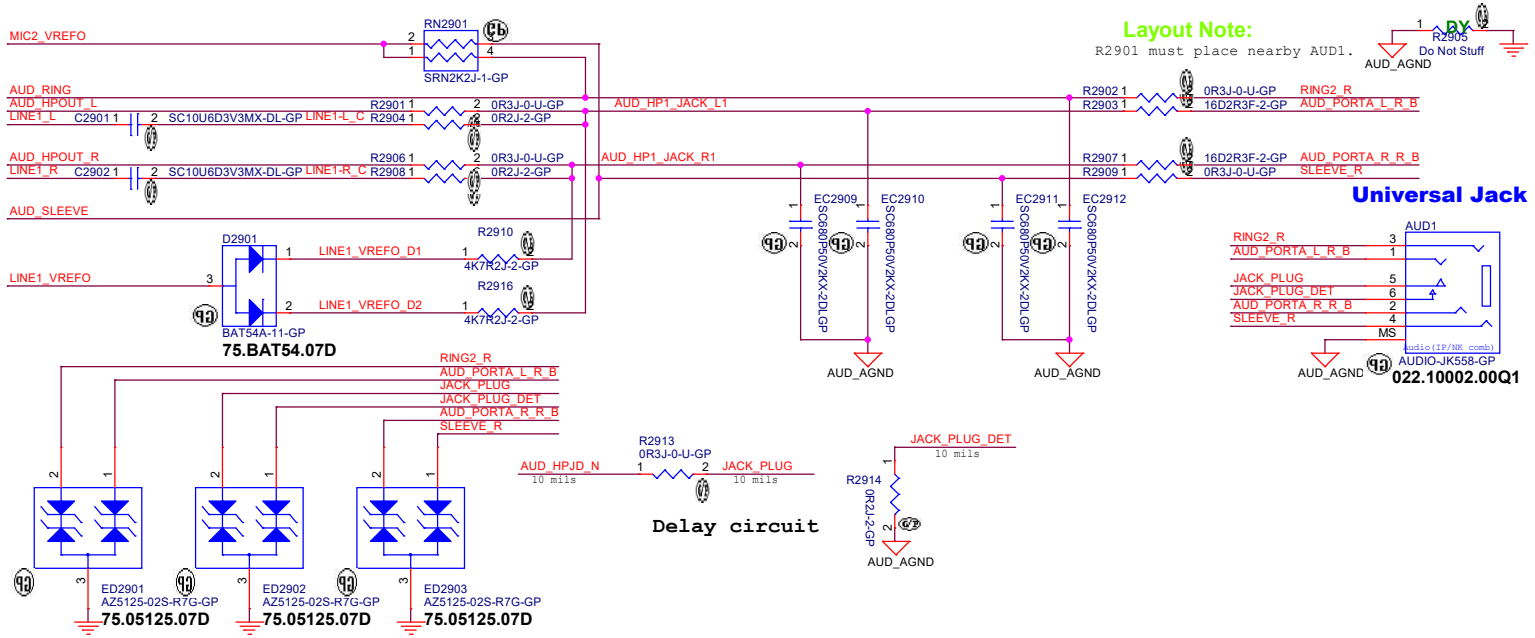
Title: **Audio (RSVD) (Audio AMP)**

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 28 of 106

Main Func = Audio





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Title: **Audio (HP/SPK/MIC Jack)**

Size	Document Number	Rev
A3	SouthPeak15 TGL	SB

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Title: **Audio (HP/SPK/MIC Jack)**

Size	Document Number	Rev
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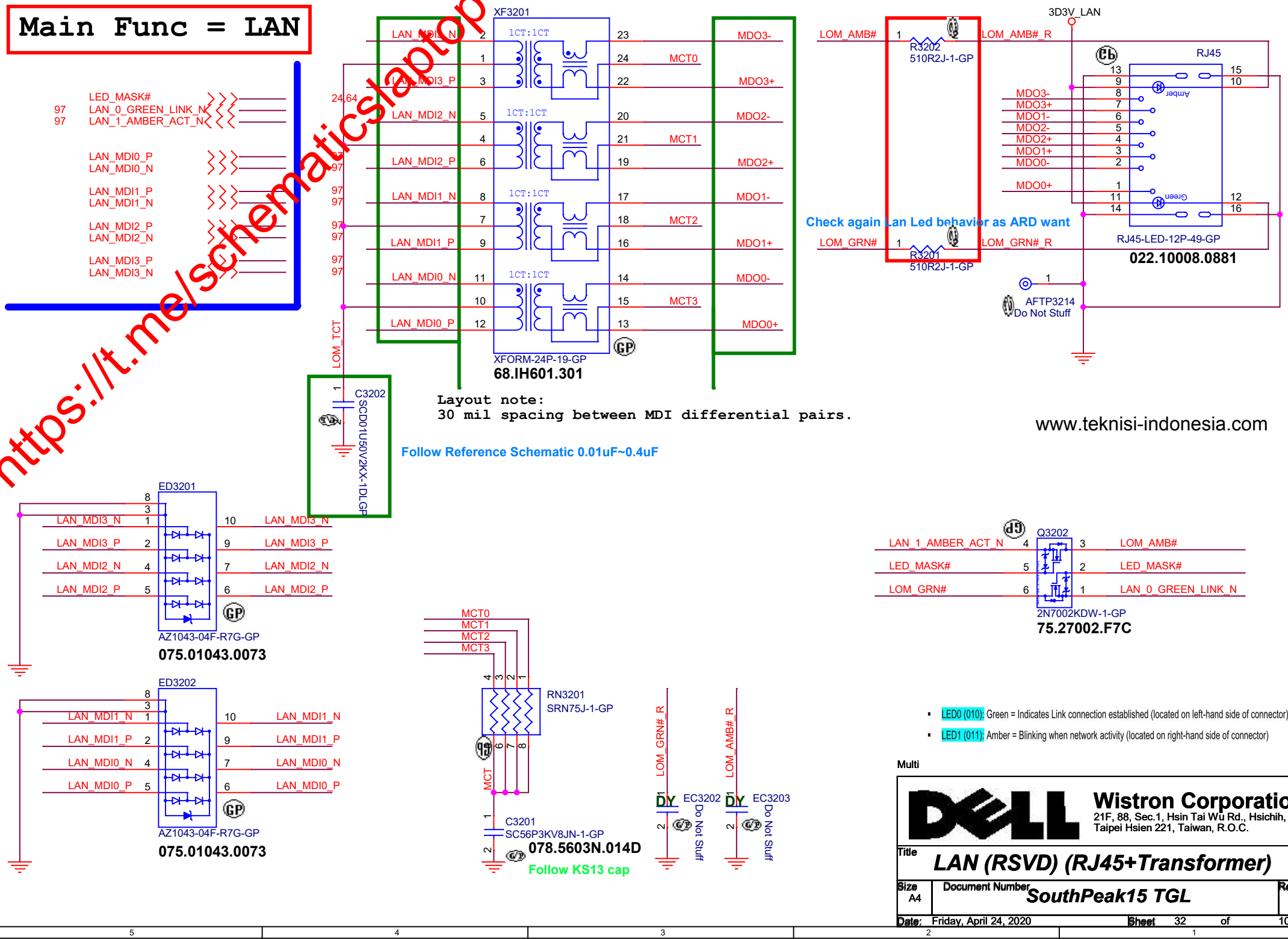
Title: *LAN (RSVD)*

Size	Document Number	Rev
A4	*SouthPeak15 TGL*	*SB*

Date: Friday, April 24, 2020 Sheet 31 of 106

Main Func = LAN



- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

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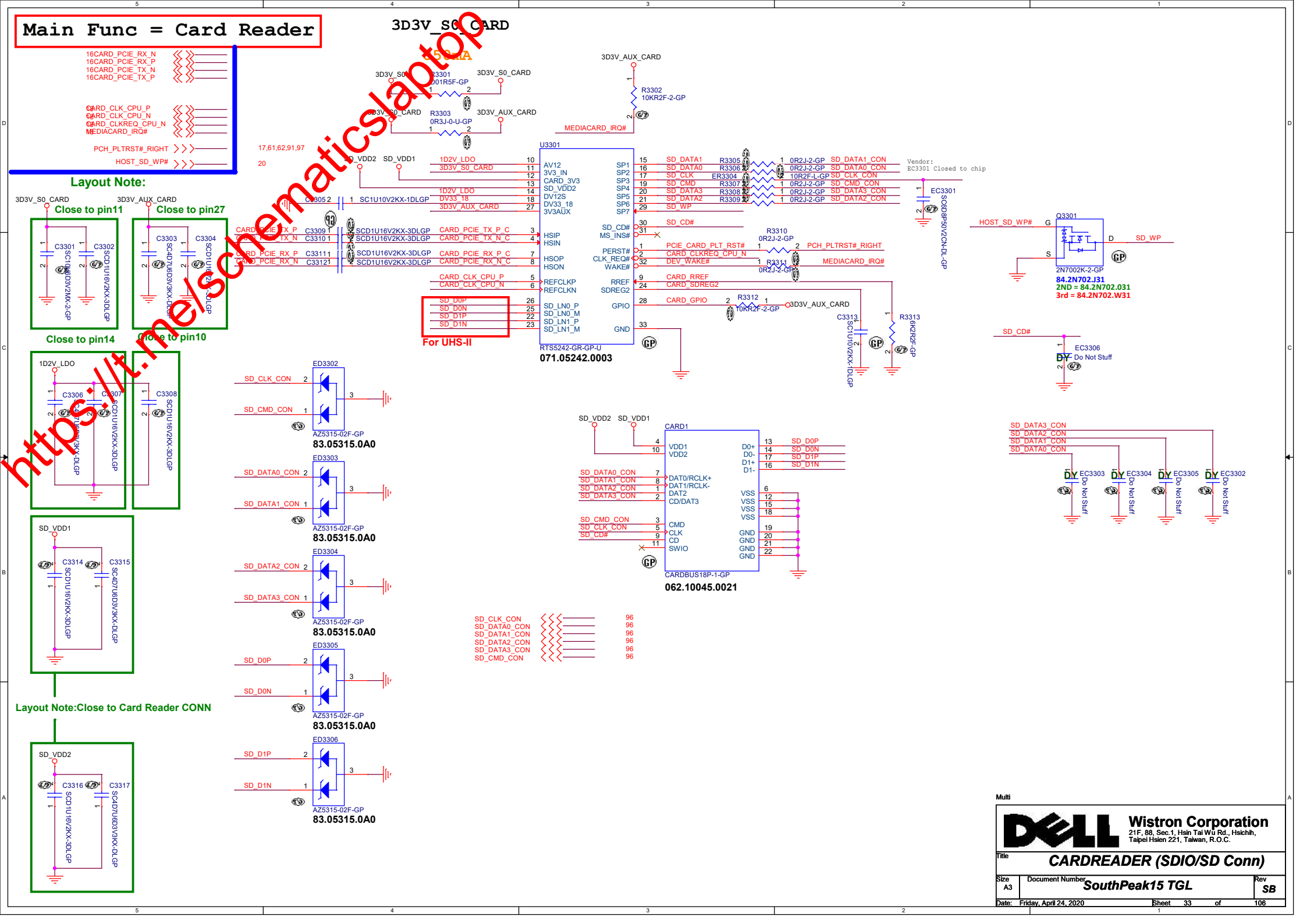
Title: **LAN (RSVD) (RJ45+Transformer)**

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 32 of 106

Main Func = Card Reader



Multi

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Title: CARDREADER (SDIO/SD Conn)

Size	Document Number	Rev
A3	SouthPeak15 TGL	SB

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Multi

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Title: USB (RSVD) (USB2.0 CONN)

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

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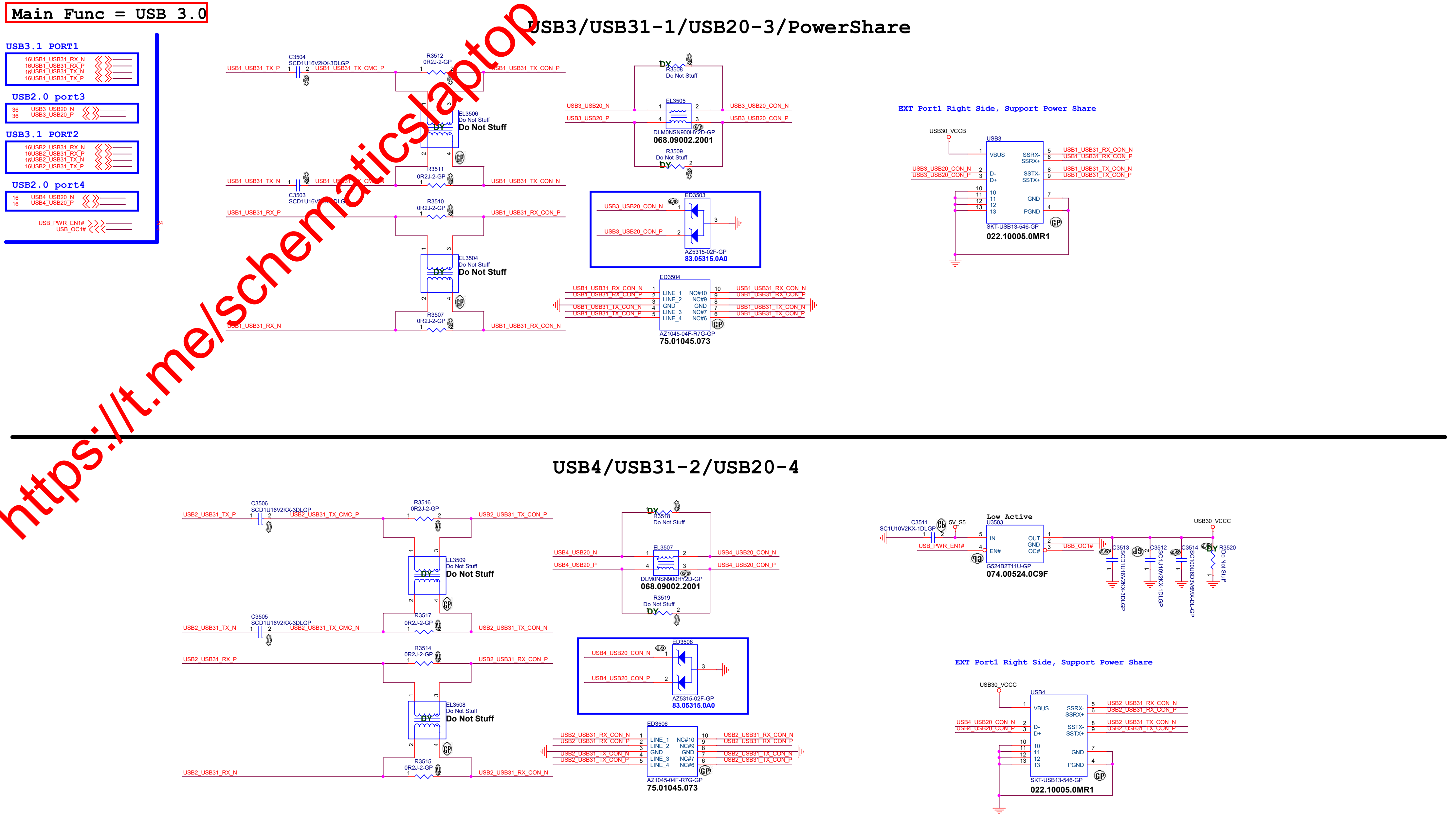

Main Func = USB 3.0
USB3/USB31-1/USB20-3/PowerShare
USB3.1 PORT1
16USB1_USB31_RX_N
16USB1_USB31_RX_P
16USB1_USB31_TX_N
16USB1_USB31_TX_P
USB2.0 port3
36 USB3_USB20_N
36 USB3_USB20_P
USB3.1 PORT2
16USB2_USB31_RX_N
16USB2_USB31_RX_P
16USB2_USB31_TX_N
16USB2_USB31_TX_P
USB2.0 port4
16 USB4_USB20_N
16 USB4_USB20_P
USB_PWR_EN1#
USB_OC1#
C3504
SCD1U16V2KX-3DLGP
R3512
0R2J-2-GP
USB1_USB31_TX_P
USB1_USB31_TX_CMC_P
USB1_USB31_TX_CON_P
EL3506
Do Not Stuff
Do Not Stuff
R3511
0R2J-2-GP
USB1_USB31_TX_N
USB1_USB31_TX_CON_N
C3503
SCD1U16V2KX-3DLGP
R3510
0R2J-2-GP
USB1_USB31_RX_P
USB1_USB31_RX_CON_P
EL3504
Do Not Stuff
Do Not Stuff
R3507
0R2J-2-GP
USB1_USB31_RX_N
USB1_USB31_RX_CON_N
R3508
Do Not Stuff
EL3505
USB3_USB20_N
USB3_USB20_P
USB3_USB20_CON_N
USB3_USB20_CON_P
DLM0NSN900HY2D-GP
068.09002.2001
R3509
Do Not Stuff
ED3503
USB3_USB20_CON_N
USB3_USB20_CON_P
AZ5315-02F-GP
83.05315.0A0
ED3504
LINE_1
LINE_2
GND
LINE_3
LINE_4
NC#10
NC#9
GND
NC#7
NC#6
AZ1045-04F-R7G-GP
75.01045.073
EXT Port1 Right Side, Support Power Share
USB30_VCCB
USB3
VBUS
D-
D+
SSRX-
SSRX+
SSTX-
SSTX+
GND
PGND
USB1_USB31_RX_CON_N
USB1_USB31_RX_CON_P
USB1_USB31_TX_CON_N
USB1_USB31_TX_CON_P
SKT-USB13-546-GP
022.10005.0MR1
USB4/USB31-2/USB20-4
C3506
SCD1U16V2KX-3DLGP
R3516
0R2J-2-GP
USB2_USB31_TX_P
USB2_USB31_TX_CMC_P
USB2_USB31_TX_CON_P
EL3509
Do Not Stuff
Do Not Stuff
C3505
SCD1U16V2KX-3DLGP
R3517
0R2J-2-GP
USB2_USB31_TX_N
USB2_USB31_TX_CMC_N
USB2_USB31_TX_CON_N
R3514
0R2J-2-GP
USB2_USB31_RX_P
USB2_USB31_RX_CON_P
EL3508
Do Not Stuff
Do Not Stuff
R3515
0R2J-2-GP
USB2_USB31_RX_N
USB2_USB31_RX_CON_N
R3518
Do Not Stuff
EL3507
USB4_USB20_N
USB4_USB20_P
USB4_USB20_CON_N
USB4_USB20_CON_P
DLM0NSN900HY2D-GP
068.09002.2001
R3519
Do Not Stuff
ED3508
USB4_USB20_CON_N
USB4_USB20_CON_P
AZ5315-02F-GP
83.05315.0A0
ED3506
AZ1045-04F-R7G-GP
75.01045.073
Low Active
U3503
C3511
SC1U10V2KX-1DLGP
5V_S5
IN
EN#
OUT
GND
OC#
USB_PWR_EN1#
USB_OC1#
G524B2T11U-GP
074.00524.0C9F
USB30_VCCC
C3513
SCD1U16V2KX-3DLGP
C3512
SC1U10V2KX-1DLGP
C3514
SC100U6D3V6MX-DL-GP
R3520
Do Not Stuff
EXT Port1 Right Side, Support Power Share
USB4
VBUS
USB2_USB31_RX_CON_N
USB2_USB31_RX_CON_P
USB2_USB31_TX_CON_N
USB2_USB31_TX_CON_P
USB4_USB20_CON_N
USB4_USB20_CON_P
SKT-USB13-546-GP
022.10005.0MR1

Multi

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Title: USB (USB3.0 CONN)

Size	Document Number	Rev
A2	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 35 of 106

Main Func = USB Charger

support power share on the USB3.0 port on the right side of platform

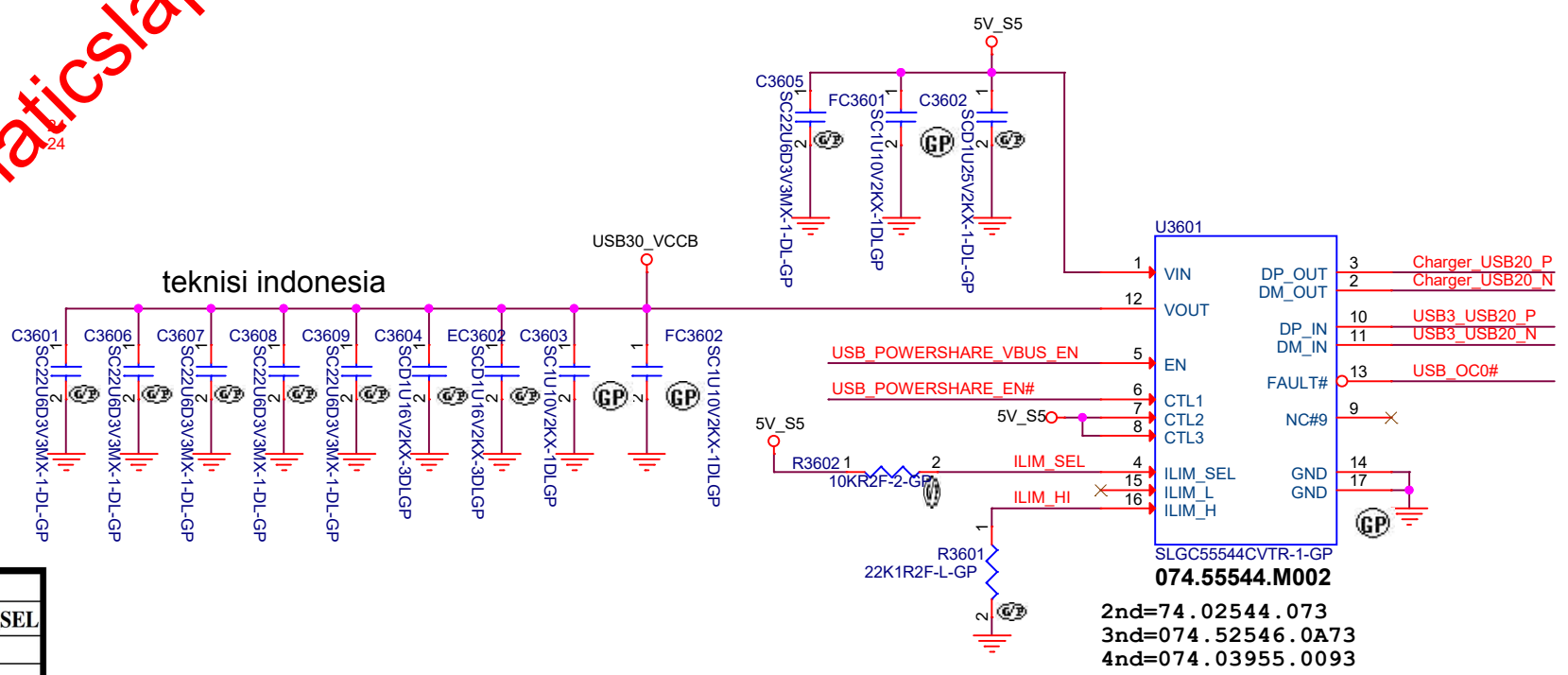
USB2.0 port3

35 USB3_USB20_N
35 USB3_USB20_P
USB_OC0# 16
USB_POWERSHARE_VBUS_EN
USB_POWERSHARE_EN# 24

USB charger

16 Charger_USB20_N
16 Charger_USB20_P

USB3.0 Port2



teknisi indonesia

Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570

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Title: USB (USB Charger)

Size: A4 | Document Number: SouthPeak15 TGL | Rev: SB

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Title

USB (RSVD) (PCIE to USB3.0)

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

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Title: USB (RSVD) (USB Redriver/Hub)

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

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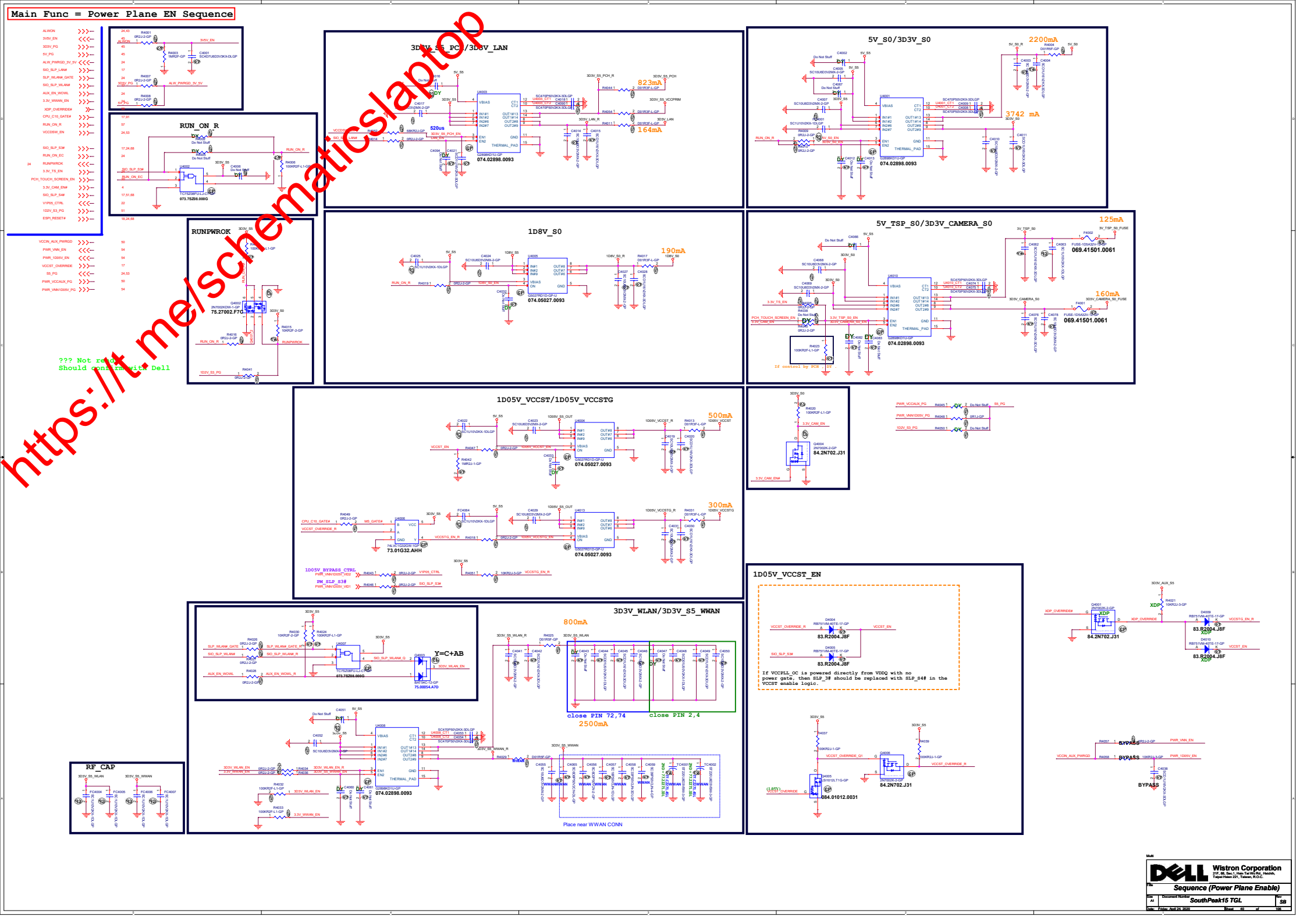
Title

Sequence (RSVD)

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 39 of 106

Main Func = Power Plane EN Sequence



??? Not ready
Should confirm with Dell

Multi	
File:	Sequence (Power Plane Enable)
Size: A1	Document Number: SouthPeak15 TGL
Date: Friday, April 24, 2020	Sheet 40 of 106

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Multi

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sequence (RSVD) (DS3/S0ix)*

Size	Document Number	Rev
A4	*SouthPeak15 TGL*	*SB*

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Title

INT IO (RSVD)

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

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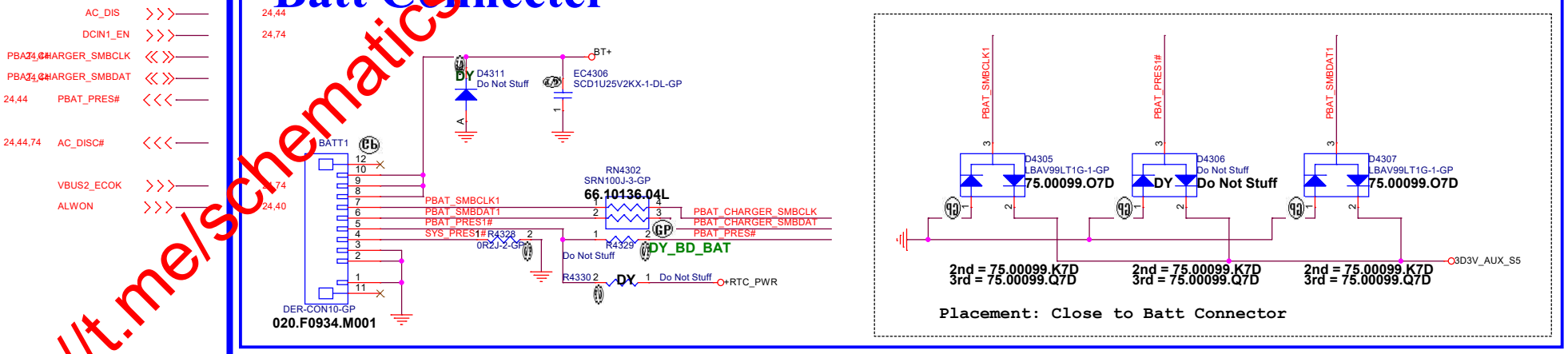
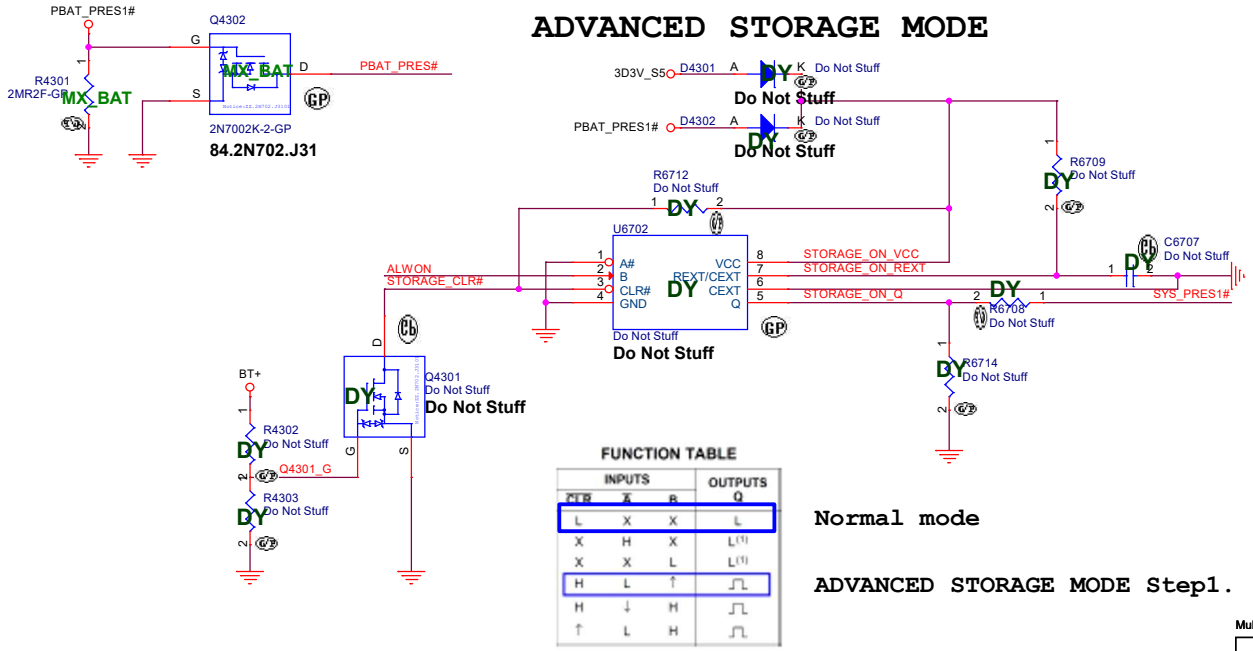
Main Func = BATT Com

Batt Connecter





Multi

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Title: DC IN/BATT Conn

Size: A3 | Document Number | Rev: SB

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Main Func = Power_Charger

OFFPAGE

PBAT_CHARGER_SMBDAT — PC4411 0R22-2-GP — PWR_CHG_DATA
PBAT_CHARGER_SMBCLK — PC4412 0R22-2-GP — PWR_CHG_CLK
I_ADP — PR4440 0R1J-GP — PWR_CHG_AMON
I_BATT_R — PR4419 0R1J-GP
I_SYS_R — PR4418 0R1J-GP — PWR_CHG_PMON
PROCHOT#_PD_R — PR4446 0R1J-GP — PWR_CHG_PROCHOT#_RR
PBAT_PRES# — PR4447 Do Not Stuff — PWR_PBAT_PRES#
ACAV_IN — PR4448 0R1J-GP — PWR_ACAV_IN
AC_DIS_ACP
VBUS1_ECOK — 24,74
VR_EN — 24,46
PCH_PWROK — 17,46
AC_DISC# — 24,74

DY_BD_BAT

Vcore_OVP

Location	Gen11	Gen12
PC4451	Stuff	DY
PC4454	Stuff	DY
PC4456	Stuff	DY
PQ4425	Stuff	DY
PR4436	Stuff	DY
PR4437	Stuff	DY
PR4438	Stuff	DY
PR4439	Stuff	DY
PR4441	Stuff	DY
PR4445	Stuff	DY
PR4452	Stuff	DY
PR4453	Stuff	DY
PR4460	Stuff	DY
PR4491	Stuff	DY
PU4415	Stuff	DY
PD4403	DY	Stuff
PD4404	DY	Stuff
PR4455	DY	Stuff
PR4457	DY	Stuff
PD4409	Stuff	DY
PR4493	DY	Stuff

	PR4461	PC4430	PR4447	EC token "SUPPORT_3VLDO_AS_BATTPRES"
Coin cell battery	DY	Stuff	Stuff	Disable
Battery internal LDO	Stuff	DY	DY	Enable

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP ±%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

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Title: Charger

OFFPAGE

3V5V_EN — PR4518 0R1J-GP — PWR_3V5V_EN
5V_PG — PR4517 0R1J-GP — PWR_5V_PG
3D3V_PG — PR4516 0R1J-GP — PWR_3V_PG

Main Func = Power_System 5V/3D3V

19V_DCBATOUT — PR4527 Do Not Stuff — PWR_DCBATOUT_3D3V
PR4528 Do Not Stuff
PR4529 Do Not Stuff
PR4530 Do Not Stuff

3D3V_AUX
PR4501 Do Not Stuff
PR4502 Do Not Stuff
PR4503 0R1J-GP — PWR_5V_EN1_R — PWR_5V_EN1
PR4504 0R1J-GP
PR4505 0R1J-GP — PWR_3V5V_EN — PWR_3D3V_EN1

3D3V_AUX_S5
PR4561 Do Not Stuff

PR4506 0R3J-0-U-GP — PWR_3D3V_BOOT — PWR_3D3V_VCC — PWR_3D3V_BOOT_A
PC4502 SCD1U25V2KX-1-DL-GP
Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PC4551 SC2D2U10V3KX-1DLGP-U

PU4501 TPS51393PRJER-GP
074.51393.0A43
VIN ×4 — VCC — SW#6 — SW#19 — SW#20 — PWR_3D3V_PH
EN — PWR_3D3V_EN1 — PWR_3D3V_EN2
ENLDO — NC#10 — NC#16 — LDO — PWR_3D3V_LDO
BOOT — PWR_3D3V_BOOT
PGOOD — PWR_3V_PG
FB — PWR_3D3V_FB
VOUT — PWR_3D3V_VOUT
GND ×4

PL4501 IND-1D5UH-23-GP-U 68.1R510.10K

PWR_3D3V — Design Current=5A — OCP>9.75A

PC4502 FC4501 FC4508 SC1U10V2KX-1DLGP
PC4503 PC4504 PC4505 PC4506 SC22U6D3V3MX-1DLGP
PC4508 DY Do Not Stuff

PR4519–PR4526 Do Not Stuff

	TPS51393	JW5068B
PR4560	上件	DY
PR4561	DY	上件

PWR_3D3V_PH — DY PR4559 Do Not Stuff — PWR_3D3V_SNB — DY PC4524 Do Not Stuff

PC4509 DY Do Not Stuff
PR4507 1MR1F-GP
PR4508 300KR1F-GP
PR4562 100KR1F-GP
PC4511 SC470P50V2KX-3DLGP
PR4509 240KR1F-GP
PR4560 0R2J-2-GP
PC4510 SC10U6D3V3MX-DL-GP
PG4513 Do Not Stuff
PR4510 Do Not Stuff

Trace used 10 mil
EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 12A
OPEN DRAIN

SY8288C For 5V

19V_DCBATOUT — PR4531 Do Not Stuff — PWR_DCBATOUT_5V
PR4532 Do Not Stuff
PR4533 Do Not Stuff
PR4534 Do Not Stuff

19V_DCBATOUT — FC4507 SC1U25V2KX-4-GP — PWR_5V_FB
PR4551 560KR2F-GP
20171228 EE request

PWR_5V — PR4535 Do Not Stuff — 5V_S5
PR4536 Do Not Stuff
PR4537 Do Not Stuff
PR4538 Do Not Stuff
PR4539 Do Not Stuff
PR4540 Do Not Stuff
PR4541 Do Not Stuff
PR4542 Do Not Stuff

5V_AUX_S5 — PG4565 Do Not Stuff — PWR_5V_LDO

5V_AUX_S5 — DY PR4552 Do Not Stuff
Place another side , make GND plan bigger

PWR_DCBATOUT_5V — PC4554 SC10U25V3MX-5-GP — DY PC4552 Do Not Stuff — DY PC4555 Do Not Stuff
For 2cell use

PU4551 SY8288CRAC-GP
074.08288.0B43
INI#2 — INI#3 — INI#4 — INI#5 — PWR_5V_PG
NC#10 — NC#16
VCC — PWR_5V_VCC
EN1 — PWR_5V_EN1
EN2 — PWR_5V_EN2
GND ×4
PG — PWR_5V_PG
BS — PWR_5V_BOOT — PR4554 Do Not Stuff — PWR_5V_BOOT_A — PC4553 SCD1U25V2KX-1-DL-GP
LXI#6 — LXI#19 — LXI#20 — PWR_5V_PH
OUT — PWR_5V_VOUT
FF — PWR_5V_FB — PWR_5V_FB_A — PR4555 1KR2F-3-GP — PC4563 SC1KP50V2KX-1DLGP
LDO — PWR_5V_LDO — PC4567 SC4D7U6D3V3KX-DLGP

PC4562 SC2D2U10V3KX-1DLGP-U

PR4556 1MR2J-1-GP
PR4557 499KR2F-1-GP
PR4558 499KR2F-1-GP
19V_DCBATOUT — DY PC4566 Do Not Stuff
Place another side , make GND plan bigger

EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PL4502 IND-1D5UH-23-GP-U 68.1R510.10K

Design Current : 8A

PWR_5V — PG4562 Do Not Stuff
PC4565 PC4556 PC4557 PC4558 PC4559 SC22U6D3V3MX-1DLGP
DY PC4560 DY PC4561 Do Not Stuff
For 2cell use

Trace used 10 mil

Multi

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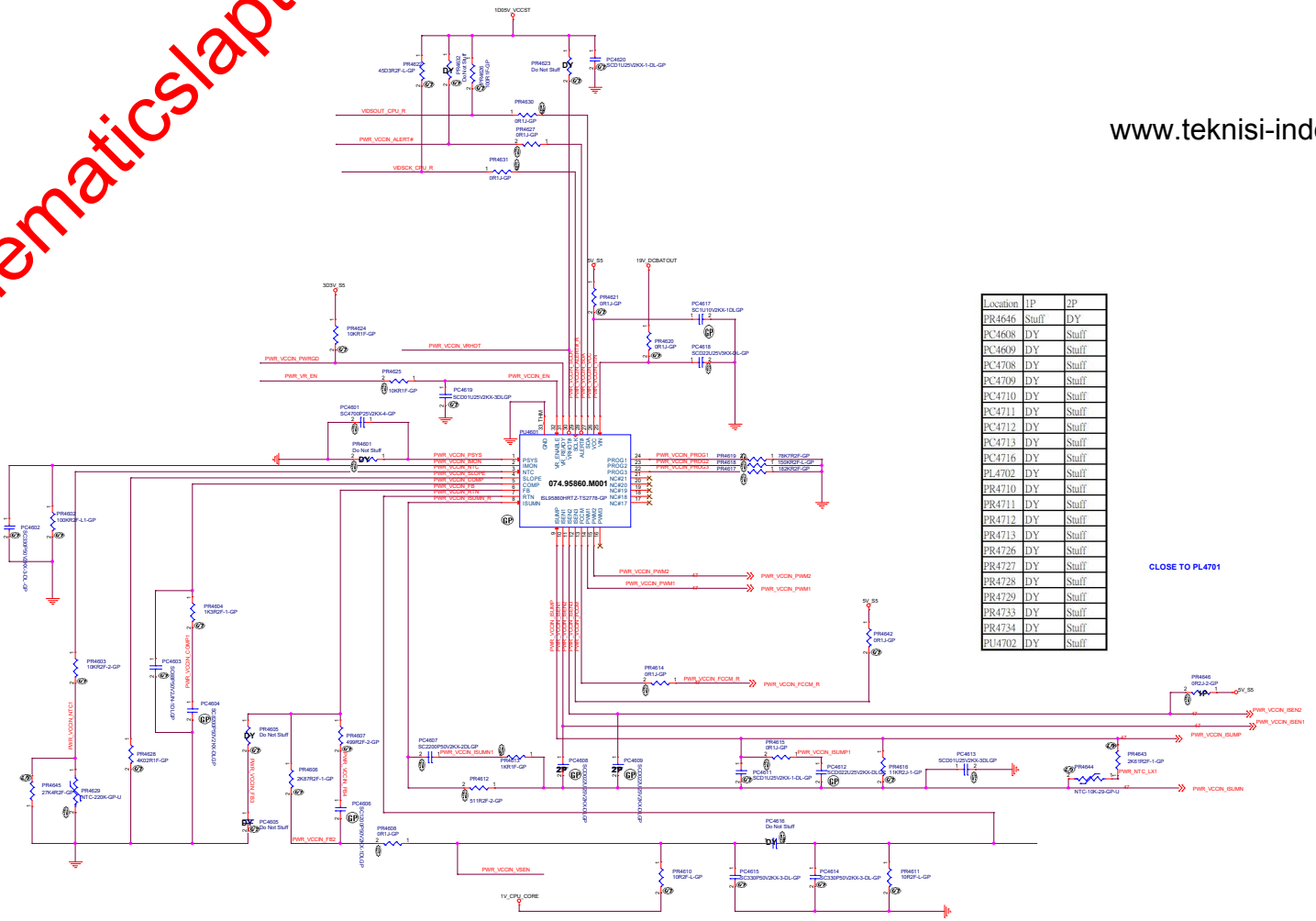
Title: 5V/3D3V
Size: A2 — Document Number — Rev: SB
Date: Friday, April 24, 2020 — Sheet 45 of 106

OFFPAGE

PROCHOT#_PD_R
SVID_CLK_CPU
SVID_DATA_CPU
SVID_ALERT#_CPU
VR_EN
PCH_PWROK
VSSCORE_SENSE
VCCCORE_SENSE
I_SYS_R

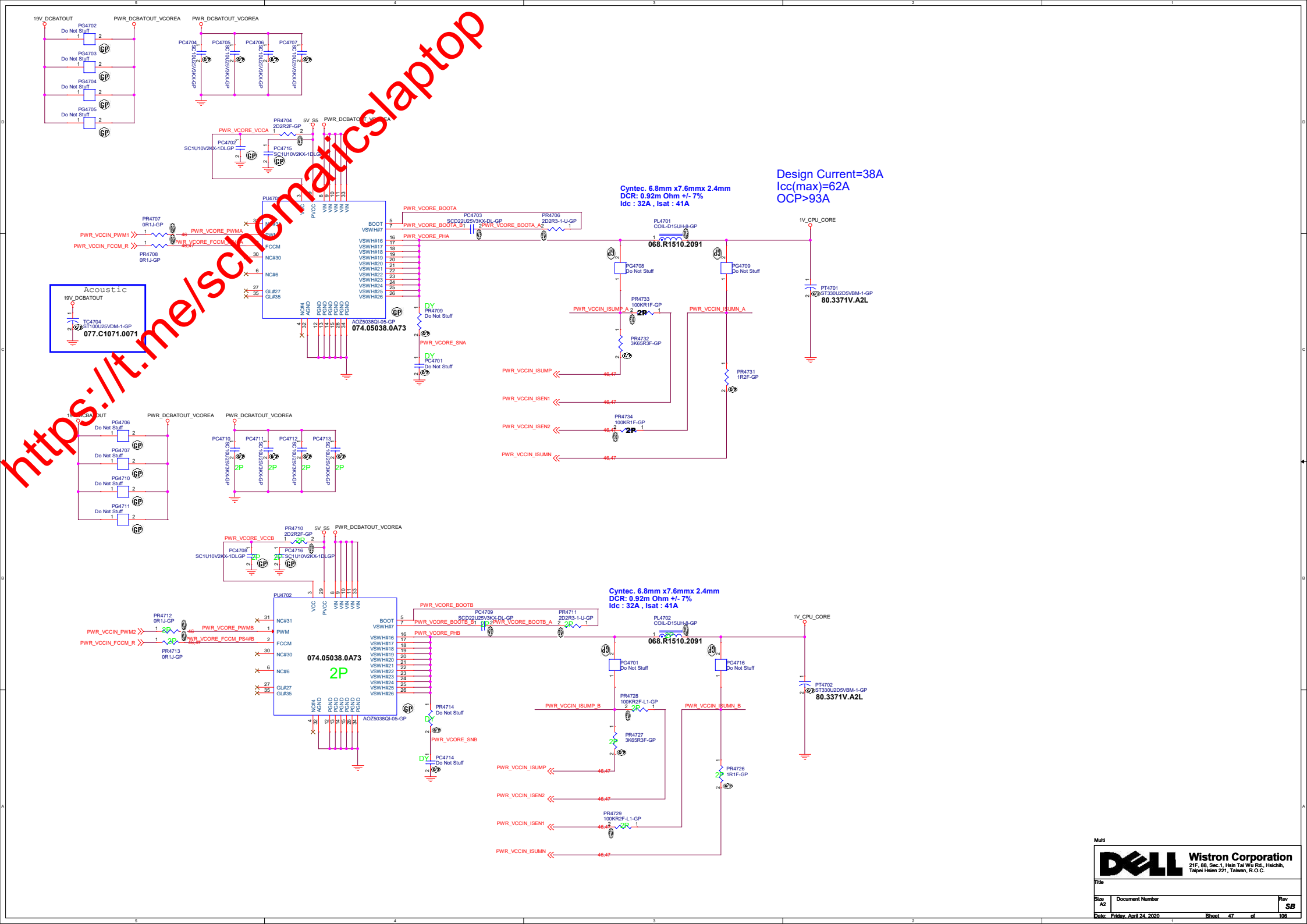


Location	1P	2P
PR4646	Stuff	DY
PC4608	DY	Stuff
PC4609	DY	Stuff
PC4708	DY	Stuff
PC4709	DY	Stuff
PC4710	DY	Stuff
PC4711	DY	Stuff
PC4712	DY	Stuff
PC4713	DY	Stuff
PC4716	DY	Stuff
PL4702	DY	Stuff
PR4710	DY	Stuff
PR4711	DY	Stuff
PR4712	DY	Stuff
PR4713	DY	Stuff
PR4726	DY	Stuff
PR4727	DY	Stuff
PR4728	DY	Stuff
PR4729	DY	Stuff
PR4733	DY	Stuff
PR4734	DY	Stuff
PU4702	DY	Stuff

CLOSE TO PL4701

Multi

Title	CPUCORE(1/3)		
Size	Document Number		Rev
A3	South Point-15 TQL		3S
Date:	Friday, April 24, 2020	Sheet 45 of 106	



Multi

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A2		SB

Date: Friday, April 24, 2020 Sheet 47 of 106

Multi

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Taipei Hsien 221, Taiwan, R.O.C.

Title
POWER

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 48 of 106

Multi

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

NCP81210MN_CPU_VCCGTUS

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 49 of 106

OFFPAGE

PH on EE Side

PH on CPU side

CORE_VID1

CORE_VID0

PH on CPU side

VCCAUX_SENSE

VSSAUX_SENSE

PR5012 0R2F-1-GP

PWR_1D8V_PG

PWR_VCCAUX_AUX_EN

PR5016 0R2F-1-GP

VCCIN_AUX_PWRGD

PWR_VCCAUX_PG

OFFPAGE_GAP

19V_DCBATOUT

PWR_DCBATOUT_VCCAUX

PG5001 Do Not Stuff

PG5002 Do Not Stuff

PG5003 Do Not Stuff

PG5004 Do Not Stuff

TABLE: MP2941 VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

LOGIC

PWR_DCBATOUT_VCCAUX

PC5002 PC5003 PC5004 PC5005 SC 10U25V3KX-GP

19V_DCBATOUT

Acoustic

TC5004 ST100U25VDM-1-GP

077.C1071.0071

3D3V_S5

PR5003 5D1R2J-1-GP

PC5001 SC1U10V2KX-1DLGP

PWR_VCCAUX_AGND

PR5004 100KR1F-GP

PWR_VCCAUX_PG

PR5006 Do Not Stuff DY

CORE_VID1 PR5008 Do Not Stuff

CORE_VID0 PR5009 Do Not Stuff

PR5001 Do Not Stuff DY

PR5013 150KR1F-GP DY

PR5014 Do Not Stuff DY

PR5015 Do Not Stuff DY

PU5001

VIN 3V3 EN VID1 VID0 FS PG CLM MODE

BST1 SW1 SW2 BST2 VOUT RGND

PGND PGND PGND AGND

MP2941BGL-Z-2-GP

074.02941.M006

PWR_VCCAUX_3D3V

PWR_VCCIN_AUX_EN_R

PWR_VCCAUX_VID1

PWR_VCCAUX_VID0

PWR_VCCAUX_FS

PWR_VCCAUX_PG

PWR_VCCAUX_CLM

PWR_VCCAUX_MODE

PWR_VCCAUX_BOOT

PWR_VCCAUX_PH

PWR_VCCAUX_BOOTB

PWR_VCCAUX_SENSE

PWR_VCCAUX_RGND

PR5036 0R2J-2-GP

PWR_VCCAUX_AGND

PC5012 SC1U25V3KX-1-DLGP

PC5013 SC1U25V3KX-1-DLGP

PL5001 COIL-D15UH-8-GP

068.R1510.2091

1D8V_VCCIN_AUX

PT5001 ST220U2DSV0K-1-GP

077.52277.M001

PANASONIC

ESR: 9 mohm

9 Pcs 22uF for 1.0MHz + 5 Pcs 22uF DY

Cyntec. 6.8mm x7.6mmx 2.4mm

DCR: 0.92m Ohm +/- 7%

Idc : 32A , Isat : 41A

OCP = 40A

Iccmax= 32A

TDC=14A

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PR5010 100R2F-L1-GP-U

PR5035 Do Not Stuff 22.5Ω VCCAUX_SENSE

PR5034 Do Not Stuff 22.5Ω VSSAUX_SENSE

PR5011 100R2F-L1-GP-U

TABLE: MP2941 FS Selection

RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

LOGIC

TABLE: MP2941 CLM/Phase Selection

RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

LOGIC

TABLE: MP2941 Mode Selection

RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay

LOGIC

TABLE : MP2941

Item	R0 sample	R1 sample
VOUT	1.65V fixed	Defined by VCCPCHCORE_VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary

Multi

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Title: Power_VCCIN_AUX

Size: Custom | Document Number | Rev: SB

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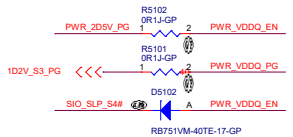
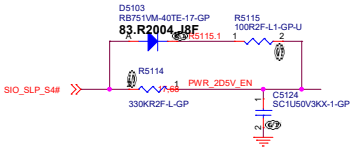
OFFPAGE

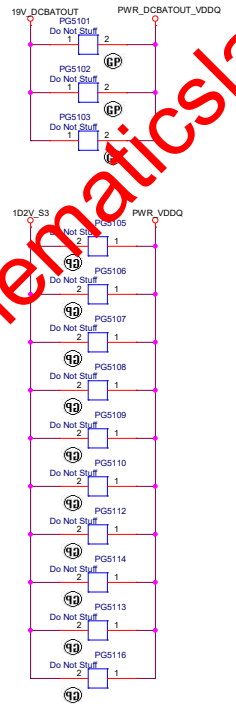
S5

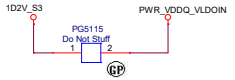


S3

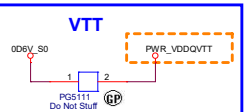


OFFPAGE_GAP

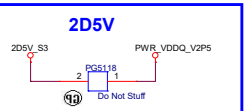


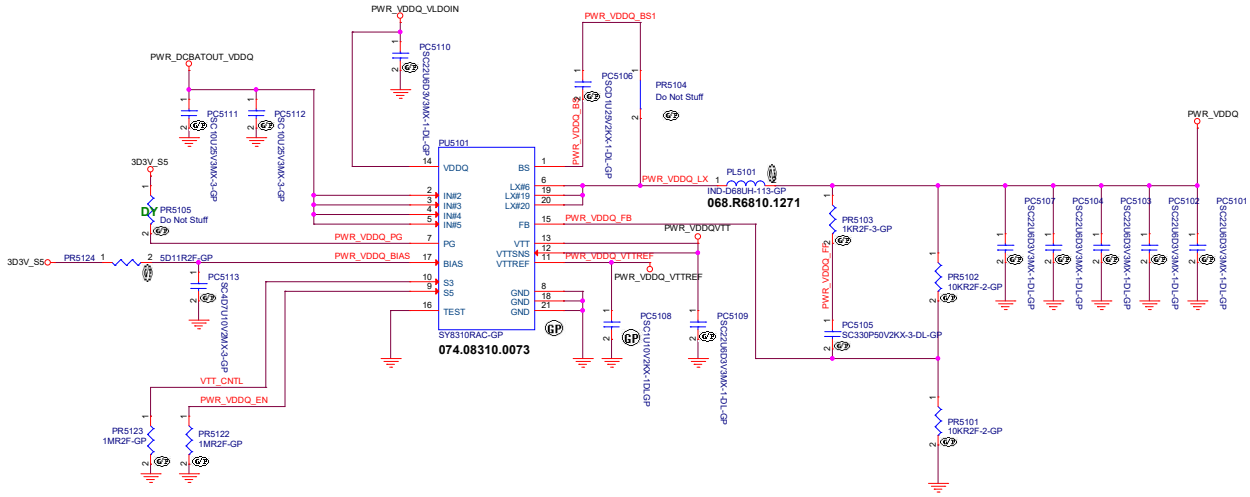


VTT



2D5V

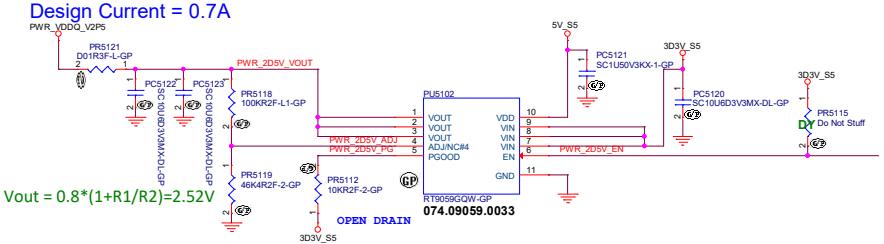




MAX:300
TPE:210

Design Current = 0.7A

RT9059GQW for 2D5V



Vout = 0.8*(1+R1/R2)=2.52V

Multi

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Title: *SY8310_VDDQ/VTT*		
Size: A2	Document Number: SouthPeak15 TGL	Rev: SB
Date: Friday, April 24, 2020	Sheet 51 of 106	

Multi

Wistron Corporation
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Title

(Reserved)

Size	Document Number	Rev
Custom		*SB*

Date: Friday, April 24, 2020 Sheet 52 of 106

OFFPAGE-Signal

SIO_SLP_SUS# — 17,24
VCCDSW_EN — 24,48
S5_PG — 24,48
PWR_1D8V_PG — 50

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_1D8V
PG5302 Do Not Stuff
PG5303 Do Not Stuff

1D8V_S5 — PWR_1D8V
PG5311 Do Not Stuff
PG5310 Do Not Stuff
PG5307 Do Not Stuff
PG5308 Do Not Stuff
PG5309 Do Not Stuff

PWR_DCBATOUT_1D8V

PU5301 TPS51396RJER-GP
074.51396.0043

PC5301 SC10U25V3MX-3-GP
PC5302 SC10U25V3MX-3-GP
PC5313 SCD1U25V2KX-1-DL-GP
PC5309 SC2D2U10V3KX-1DLGP-U
PC5311 SCD022U16V2KX-3DLGP

PWR_1D8V_VCC
PWR_1D8V_EN
PWR_1D8V_SS
PWR_1D8V_PG
PWR_1D8V_BOOT
PWR_1D8V_BOOT_A
PWR_1D8V_PH
PWR_1D8V_FB
PWR_1D8V_MODE

PR5303 Do Not Stuff
PC5303 SCD1U25V2KX-1-DL-GP

Cyntec, 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

IDC:5A

PL5301 COIL-1UH-34-GP-U1
68.1R01A.20B

Trace used 10 mil

PR5304 332KR1F-GP
PR5305 1MR1F-GP
PR5301 5K11R1F-GP

Vout = 0.6V x (1+ R1/R2)
= 0.6 x (1 + 20K/10K)
= 0.6 x 3 = 1.8 V

R1 PR5306 20KR1F-GP
R2 PR5307 10KR1F-GP

PWR_1D8V
PG5306 Do Not Stuff
PC5304 PC5305 PC5306 PC5307 PC5308
PR5313 Do Not Stuff
SC22U6D3V3MX-1-DL-GP
PC5310 Do Not Stuff
PWR_1D8V_FB_B

3D3V_S5
PR5302 100KR1F-GP
Place another side , make GND plan bigger

SIO_SLP_SUS#
VCCDSW_EN
PR5309 0R2J-2-GP
PR5308 Do Not Stuff
PC5312 Do Not Stuff

S5_PG
PR5311 Do Not Stuff

PWR_1D8V_PH
PR5312 Do Not Stuff
PWR_1D8V_SNB
PC5314 Do Not Stuff

Multi

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Title: TPS51396_1D8V		
Size: Custom	Document Number: SouthPeak15 TGL	Rev: SB
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OFFPAGE

PH on EE Side

VCCIN_AUX_PWRGD
PWR_VNN_EN

PWR_VNN_EN 40

PWR_1D05V_EN

PWR_1D05V_EN 40

PH on EE Side

1D05V_BYPASS_CTRL
PWR_VNN1D05V_VID2

PWR_VNN1D05V_VID2 40

PM_SLP_S3#
PWR_VNN1D05V_VID1

PWR_VNN1D05V_VID1 40

PWR_VNN1D05V_PG

40

OFFPAGE-CAP

1D05V_VNN_BYPASS

R5498 1 2 D01R2J-L-GP

PWR_VNN

1D05V_S5_BYPASS

R5498 1 2 D01R2J-L-GP

PWR_1D05V

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

3D3V_S5

100KR1J-GP
PR5420

PWR_VNN1D05V_PG

Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A

PL5401
IND-1UH-382-GP
068.1R010.1131

PWR_VNN

PC5411 SC22U6D3V3MX-1-DL-GP
PC5412 SC22U6D3V3MX-1-DL-GP

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A

PL5402
IND-10UH-330-GP
68.1001S.10K

PWR_1D05V

PC5414 DY Do Not Stuff
PR5408 0R1J-GP
PR5407 DY Do Not Stuff
PC5410 SC22U6D3V3MX-1-DL-GP
PC5415 SC22U6D3V3MX-1-DL-GP

PR5419 Do Not Stuff
PR5430 DY Do Not Stuff

PC5401 SC1U10V2KX-1DLGP
PR5413 2D2R2F-GP
5V_S5

PC5402 SC10U25V3MX-5-GP
PR5422 Do Not Stuff
PR5410 Do Not Stuff
19V_DCBATOUT
PC5403 SC10U25V3MX-5-GP

PC5404 SCD1U25V2KX-1-DL-GP
PC5405 SCD1U25V2KX-1-DL-GP
PWR_VNN1D05V_BOOTA_A
PWR_VNN1D05V_BOOTB_A

PC5406 DY Do Not Stuff

PR5423 0R1J-GP PWR_VNN1D05V_PHB
PR5401 0R1J-GP PWR_VNN1D05V_PHA

PU5401
APW8743CQBI-TRG-GP
074.08743.0A73

VCC	8	EN1	15
VIN1	11	EN2	6
VIN2	10	LX1	1
VID1	13	LX2	4
VID2	14	VOUT2	5
POK	7	VOUT1	16
BOOT1	2	AGND	17
BOOT2	3	PGND	9
		PGND	12

PWR_VNN1D05V_VCC
PWR_VNN1D05V_VINA
PWR_VNN1D05V_VINB
PWR_VNN1D05V_VID1
PWR_VNN1D05V_BOOTA
PWR_VNN1D05V_BOOTB
PWR_VNN1D05V_VID2
PWR_VNN1D05V_PG
PWR_VNN_EN
PWR_1D05V_EN
PWR_VNN1D05V_PHA
PWR_VNN1D05V_PHB
PWR_VNN1D05V_FB2
PWR_VNN1D05V_VOUT1

3D3V_S5 3D3V_S5

PR5426 Do Not Stuff DY PWR_VNN1D05V_VID1
PR5427 Do Not Stuff DY PWR_VNN1D05V_VID2

PR5433 10KR1F-GP
PR5428 10KR1F-GP

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Multi

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Title: APW8738_ByPASS

Size: Custom | Document Number: SouthPeak15 TGL | Rev: SB

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Main Func = LCD/Touch

LCD1
ACES-CON50-7-GP
020.F0285.0050

INVERTER POWER

1086mA

LCDVDD

850mA

PANEL_PWRGD CIRCUIT

Do Not Stuff

Multi

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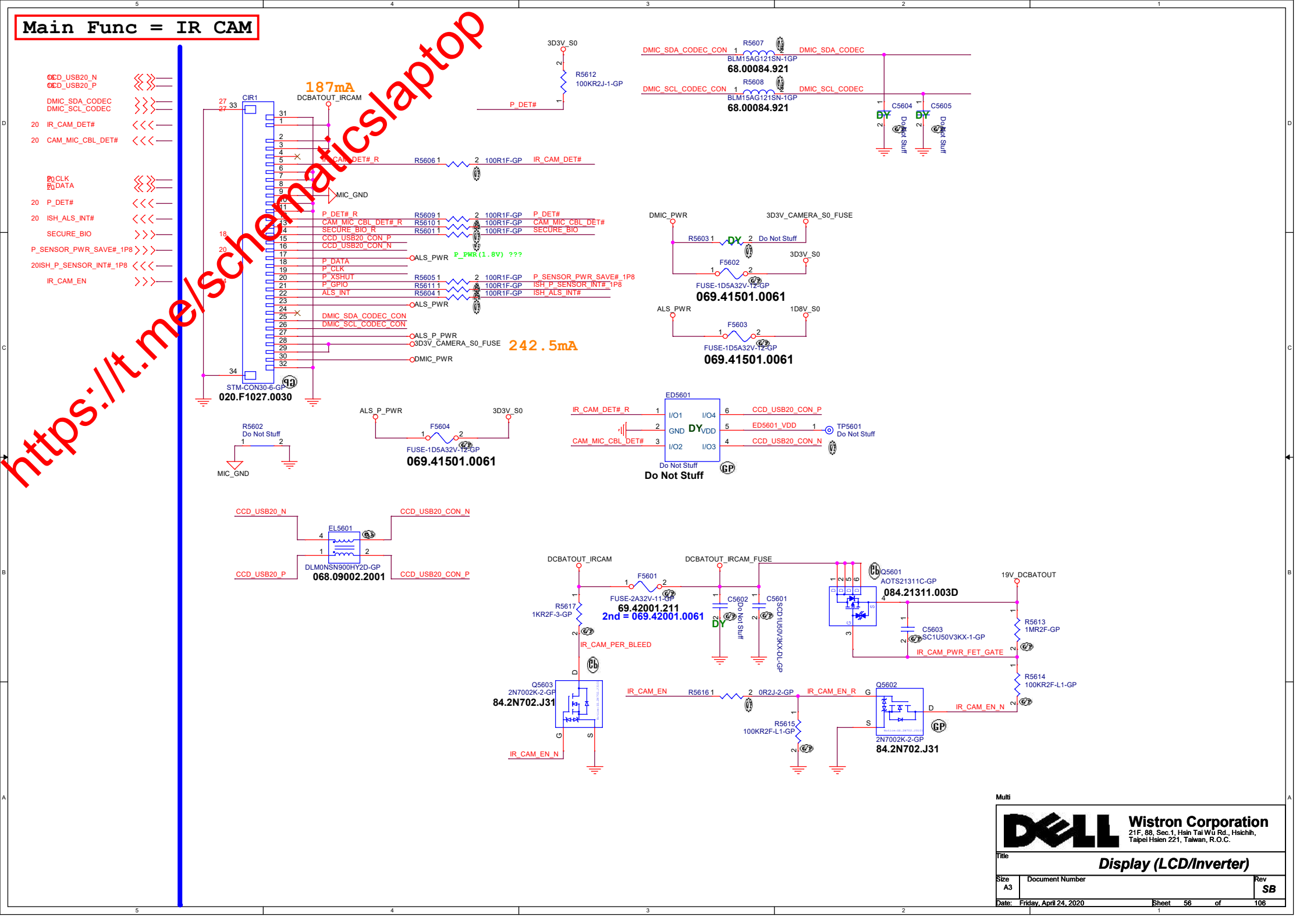
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Inverter)

Size: A2 | Document Number | Rev: SB

Date: Friday, April 24, 2020 | Sheet 55 of 106

Main Func = IR CAM



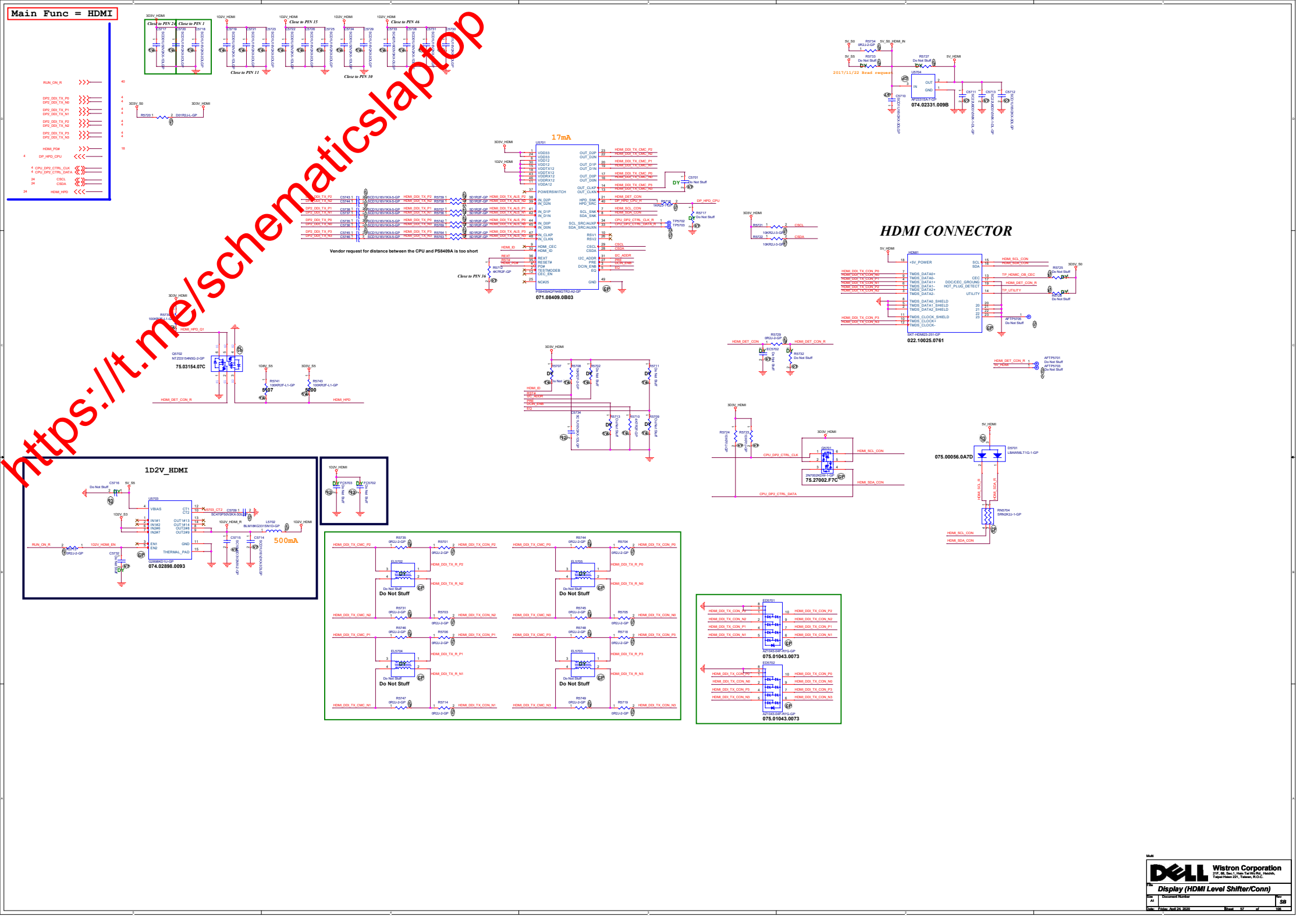
Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display (LCD/Inverter)**

Size	Document Number	Rev
A3		SB

Date: Friday, April 24, 2020 Sheet 56 of 106


Main Func = HDMI
1D2V_HDMI
HDMI CONNECTOR
17mA
500mA
Vendor request for distance between the CPU and PS8409A is too short
Do Not Stuff
075.00056.0A7D
075.01043.0073
074.02331.009B
074.02898.0093
71.03154.07C
71.08409.0B03
022.10025.0761
Display (HDMI Level Shifter/Conn)
Wistron Corporation
https://t.me/schematicslaptop

Multi

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (RSVD) DP*

Size	Document Number	Rev
A4		*SB*

Date: Friday, April 24, 2020 Sheet 58 of 106

Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Display (RSVD) DVI

Size	Document Number	Rev
A4		*SB*

Date: Friday, April 24, 2020 Sheet 59 of 106

Multi

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

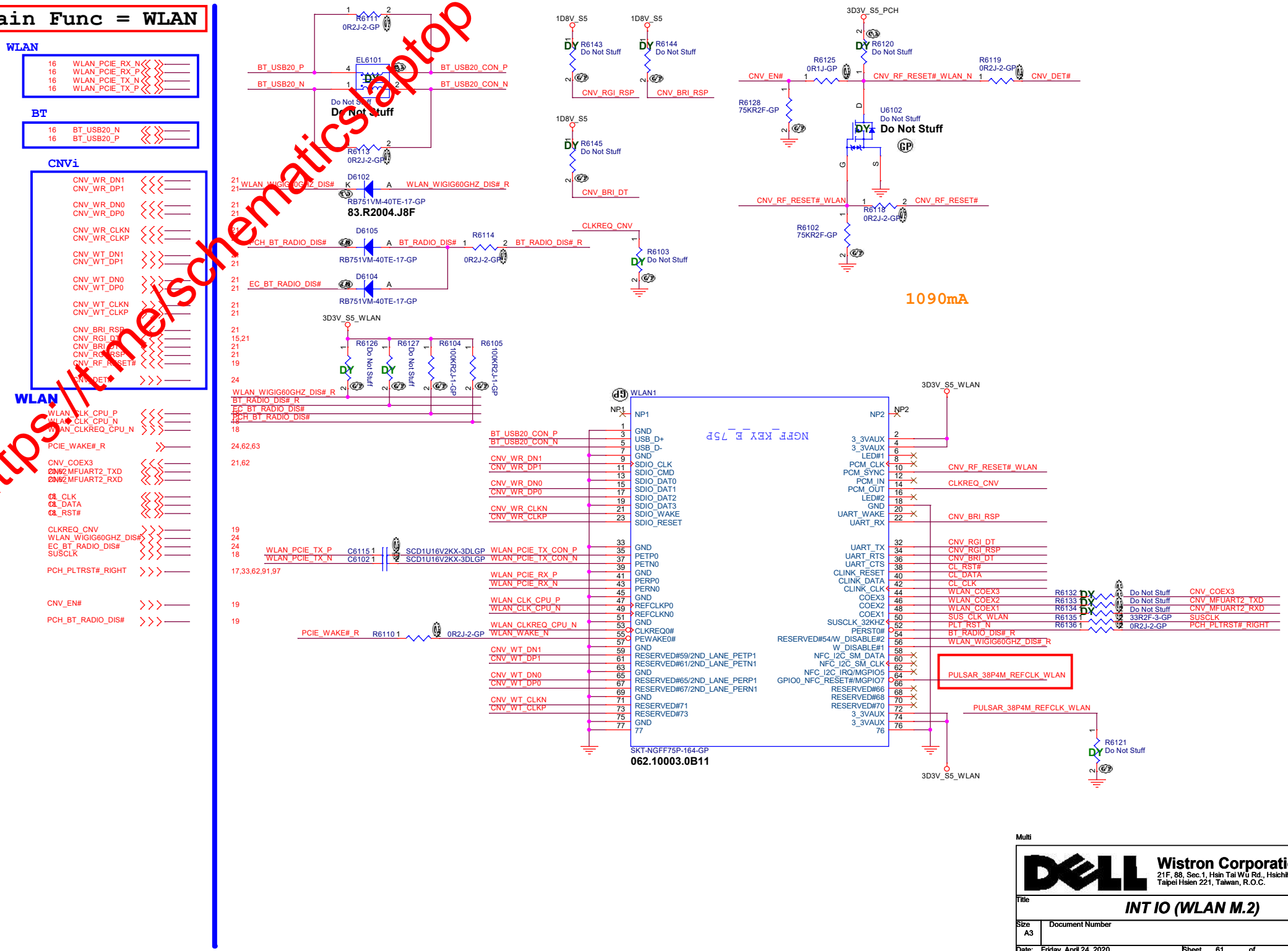
Title

INT IO (RSVD)(HDD)

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 60 of 106

Main Func = WLAN



Multi

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2)

Size	Document Number	Rev
A3		SB

Date: Friday, April 24, 2020 Sheet 61 of 106

Main Func = WWAN

NGFF(WWAN/SSD)

WWAN

16WWAN_USB31_RX_N
16WWAN_USB31_RX_P
16WWAN_USB31_TX_N
16WWAN_USB31_TX_P

WWAN

16 WWAN_USB20_N
16 WWAN_USB20_P

WWAN

16WWAN_PCIE_RX_N
16WWAN_PCIE_RX_P
16WWAN_PCIE_TX_N
16WWAN_PCIE_TX_P

NGFF_CONFIG_0
NGFF_CONFIG_1
NGFF_CONFIG_2
NGFF_CONFIG_3

WWAN_RADIO_DIS#
GPS_DISABLE#

20CPU_I2C_SDA_GNSS
20CPU_I2C_SCL_GNSS
PCH_PLTRST#_RIGHT
PCIE_WAKE#_R
CNV_COEX3
20CNV_MFUART2_TXD
20CNV_MFUART2_RXD
WWAN_CLK_CPU_P
WWAN_CLK_CPU_N
WWAN_CLKREQ_CPU_N
WWAN_GPIO_WAKE#
WWAN_GPIO_CTRL
WWAN_GPIO_PERST#
WWAN_BB_RST#
PCH_PCIE_WAKE#
SAR_DRP#
SSD_SCP#
WWAN_CFG_PWR_EN_R

WWAN_RADIO_DIS# 1 — WWAN 2 — WWAN_RADIO_DIS#_R
D6201 0R2J-2-GP

GPS_DISABLE# 1 — WWAN 2 — GPS_DISABLE#_R
D6202 0R2J-2-GP

1 — WWAN 2
R6244 0R2J-2-GP

WWAN_USB20_P 4 — EL6202 — WWAN_USB20_CON_P
WWAN_USB20_N 1 — DY — WWAN_USB20_CON_N
Do Not Stuff

1 — WWAN 2
R6245 0R2J-2-GP

2500mA

WWAN1

NGFF_CONFIG_2	R6223	0R2J-2-GP	NGFF_CONFIG_2_R
NGFF_CONFIG_1	R6224	0R2J-2-GP	NGFF_CONFIG_1_R
WWAN_CLK_CPU_P			WWAN_CLK_CPU_P
WWAN_CLK_CPU_N			WWAN_CLK_CPU_N
WWAN_PCIE_TX_P	C6206	SCD1U16V1KX-5-GP	WWAN_PCIE_TX_CON_P
WWAN_PCIE_TX_N	C6203	SCD1U16V1KX-5-GP	WWAN_PCIE_TX_CON_N
WWAN_PCIE_RX_P	R6250	0R1J-GP	WWAN_PCIE_RX_CON_P
WWAN_PCIE_RX_N	R6251	0R1J-GP	WWAN_PCIE_RX_CON_N
WWAN_USB31_TX_P	C6204	SCD1U16V1KX-5-GP	WWAN_USB31_TX_CON_P
WWAN_USB31_TX_N	C6205	SCD1U16V1KX-5-GP	WWAN_USB31_TX_CON_N
WWAN_USB31_RX_P	R6233	0R1J-GP	WWAN_USB31_RX_CON_P
WWAN_USB31_RX_N	R6249	0R1J-GP	WWAN_USB31_RX_CON_N
SAR_DRP#	R6231	0R2J-2-GP	SAR_DRP#_R
NGFF_CONFIG_0	R6226	0R2J-2-GP	NGFF_CONFIG_0_R
WWAN_USB20_CON_N			WWAN_USB20_CON_N
WWAN_USB20_CON_P			WWAN_USB20_CON_P
NGFF_CONFIG_3	R6227	0R2J-2-GP	NGFF_CONFIG_3_R

76	76	CONFIG2
75	CONFIG_2	
73	GND	
71	GND	
69	CONFIG_1	
67	RESET#_0/1_8V	
65	ANTCTL3_0/1_8V	
63	ANTCTL2_0/1_8V	
61	ANTCTL1_0/1_8V	
59	ANTCTL0_0/18V	
57	GND	
55	RESERVED#55	
53	RESERVED#53	
51	GND	
49	PETP0/SATA_A+	
47	PETN0/SATA_A-	
45	GND	
43	PERP0/SATA_B-	
41	PERN0/SATA_B+	
39	GND	
37	USB3_0_RX+	
35	USB3_0_RX-	
33	GND	
31	USB3_0_TX+	
29	USB3_0_TX-	
27	GND	
25	DPR	
23	WAKE_ON_WWAN#	
21	COFIG_0	
11	GND	
9	USB_D-	
7	USB_D+	
5	GND	
3	GND	
1	CONFIG_3	
77	77	

SKT-NGFF75P-54-GP

062.10003.0221

WWAN

NP1	NP1	
3_3V	74	3D3V_S5_WWAN
3_3V	72	
3_3V	70	
SUSCLK/32KHZ_0/3_3V	68	SUS_CLK_WWAN
SIM_DETECT	66	UIM_DET
COEX1_0/1_8V	64	WWAN_COEX1
COEX2_0/1_8V	62	WWAN_COEX2
COEX3_0/1_8V	60	WWAN_COEX3
RESERVED#58	58	NC#58
RESERVED#56	56	NC#56
RESERVED#54	54	WWAN_WAKE#
RESERVED#52	52	WWAN_CLKREQ_CPU_N
RESERVED#50	50	WWAN_RESET#
GPIO_4_0/1_8V	48	
GPIO_3_0/1_8V	46	
GPIO_2_0/1_8V	44	
GPIO_1_0/1_8V	42	CPU_I2C_SDA_GNSS
GPIO_0_0/1_8V	40	CPU_I2C_SCL_GNSS
DEVSLP_0/3_3V	38	M3042_DEVSLP_R
UIM_PWR	36	UIM_PWR
UIM_DATA	34	UIM_DATA_R
UIM_CLK	32	UIM_CLK_R
UIM_RESET	30	UIM_RESET
UIM_RFU	28	UIM_RFU
UIM_RFU	26	GPS_DISABLE#_R
W_DISABLE#2_0/3_3V	24	
NC	22	
NC	20	
NC		
LED#1/DAS/DSS#	10	WWAN_RADIO_DIS#_R
W_DISABLE#1_0/3_3V	8	WWAN_FULL_PWR_EN_R
FULL_CARD_POWER_OFF#_0/1_8V	6	
3_3V	4	
3_3V	2	3D3V_S5_WWAN
NP2	NP2	

Reserved

SUS_CLK_WWAN	R6208	DY	Do Not Stuff
UIM_DET	R6217	DY	Do Not Stuff CNV_MFUART2_RXD
WWAN_COEX1	R6219	DY	Do Not Stuff CNV_MFUART2_TXD
WWAN_COEX2	R6230	DY	Do Not Stuff CNV_COEX3
WWAN_COEX3			
WWAN_WAKE#	R6266	DY	Do Not Stuff PCIE_WAKE#_R
WWAN_CLKREQ_CPU_N			
WWAN_RESET#			
CPU_I2C_SDA_GNSS			
CPU_I2C_SCL_GNSS			
M3042_DEVSLP_R			
UIM_PWR			
UIM_DATA_R	R6216	0R1J-GP	UIM_DATA
UIM_CLK_R	R6218	0R1J-GP	UIM_CLK
UIM_RESET			
UIM_RFU			
GPS_DISABLE#_R			

TP6205

WWAN_RADIO_DIS#_R — R6221 Do Not Stuff — 3D3V_S5_WWAN
WWAN_FULL_PWR_EN_R — R6257 — WWAN 00KR2F-L1-GP

D6205 DY Do Not Stuff
WWAN_RADIO_DIS#_R — SSD_SCP#

3D3V_S5_WWAN — R6248 DY Do Not Stuff — UIM_DET
R6253 WWAN 100KR2J-1-GP — UIM_DET#

To use GPIO as PEWAKE without SPDT ,unstuff R6241 ,R6243 and stuff R6242 or simply un stuff the SPDT.

3D3V_S5 — R6211 10KR2F-2-GP — WWAN_GPIO_WAKE#_R
3D3V_S5_WWAN — R6213 Do Not Stuff
WWAN_GPIO_WAKE#_R — R6243 0R2J-2-GP — PCH_PCIE_WAKE#

U6202 WWAN
NO, GND, NC#3, IN, V+, COM
TS5A3159ADCKR-1-GP
73.53159.00J

3D3V_S5 — WWAN_GPIO_CTRL_Q
NGFF_WAKE#_R — R6241 0R2J-2-GP — NGFF_WAKE#
WWAN_GPIO_WAKE#_R — R6242 Do Not Stuff — NGFF_WAKE#

Status	S1	S4	S5	S3@20 cold	S3/L1.2	S3/L2
Ctrl_gpio	H	H	H	H	H	L

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

3D3V_S5 — R6209 DY Do Not Stuff — NGFF_WAKE#
3D3V_S5_WWAN — R6212 DY Do Not Stuff

1D8V_S5 — R6207 100KR2F-L1-GP — WWAN_GPIO_CTRL
R6202 1MR2F-GP — 5107
3D3V_S5 — R6210 100KR2F-L-1-GP — 5107 — WWAN_GPIO_CTRL_Q
Q6202 PJA138KA-GP
084.00138.0A31
R62011 — 5200 — 0R2J-2-GP

Y=A*C+B*C̄

3D3V_WWAN_S5_S0_1 — R6239 0R2J-2-GP — WWAN
R6240 Do Not Stuff
3D3V_S5 — 3D3V_S0 — 3D3V_WWAN_S5_S0_1 — R6205 WWAN 0KR2F-2-GP

PCH_PLTRST#_RIGHT — U6203 SN74AUP1G97DCKR-GP WWAN — WWAN_GPIO_PERST#_R
R6235 0R2J-2-GP — WWAN_GPIO_PERST#
WWAN_RESET#_R — R6238 0R2J-2-GP — WWAN_RESET#
WWAN — R6234 100KR2F-L1-GP
073.01G97.0A0J

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN--USB3.1, PCIe Gen1	0

SIM

SIM1 — SIM 6P — SKT-SIMM6-33-GP-U
062.10008.0281

UIM_PWR — R6220 DY Do Not Stuff — UIM_VPP
UIM_DATA
UIM_RESET — R6225 0R2J-2-GP — UIM_DET#
Reverse type
Q6201 2N7002K-2-GP — UIM_DET
AFTP6201 Do Not Stuff
84.2N702.J31

UIM_PWR — C6201 SCD1U16V2KX-3DLGP — EC6202 Do Not Stuff
UIM_DET

ED6203 AZ5315-02F-GP — UIM_DATA, UIM_CLK
ED6204 AZ5315-02F-GP — UIM_RESET, UIM_VPP
83.05315.0A0
FC6215 FC6218 FC6219 FC6217 SC3P50V2JN-3DLGP
ED6205 AZ5725-01FDR7G-GP — UIM_PWR — FC6216 Do Not Stuff

Layout Close to SIM1 Connector

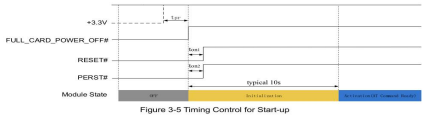


Figure 3-5 Timing Control for Start-up

Index	Minimum	Typical	Notes
t_{pr}	-	-	+3.3V power supply rises time. If power supply always ready, there is no t_{pr}
t_{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t_{on2}	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#

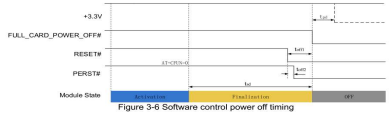


Figure 3-6 Software control power off timing

Index	Minimum	Typical	Maxim	Notes
t_{pd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t_{pd}
t_{off1}	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_OFF#
t_{off2}	0ms	30ms	t_{off1}	PERST# should asserted after RESET#

Multi

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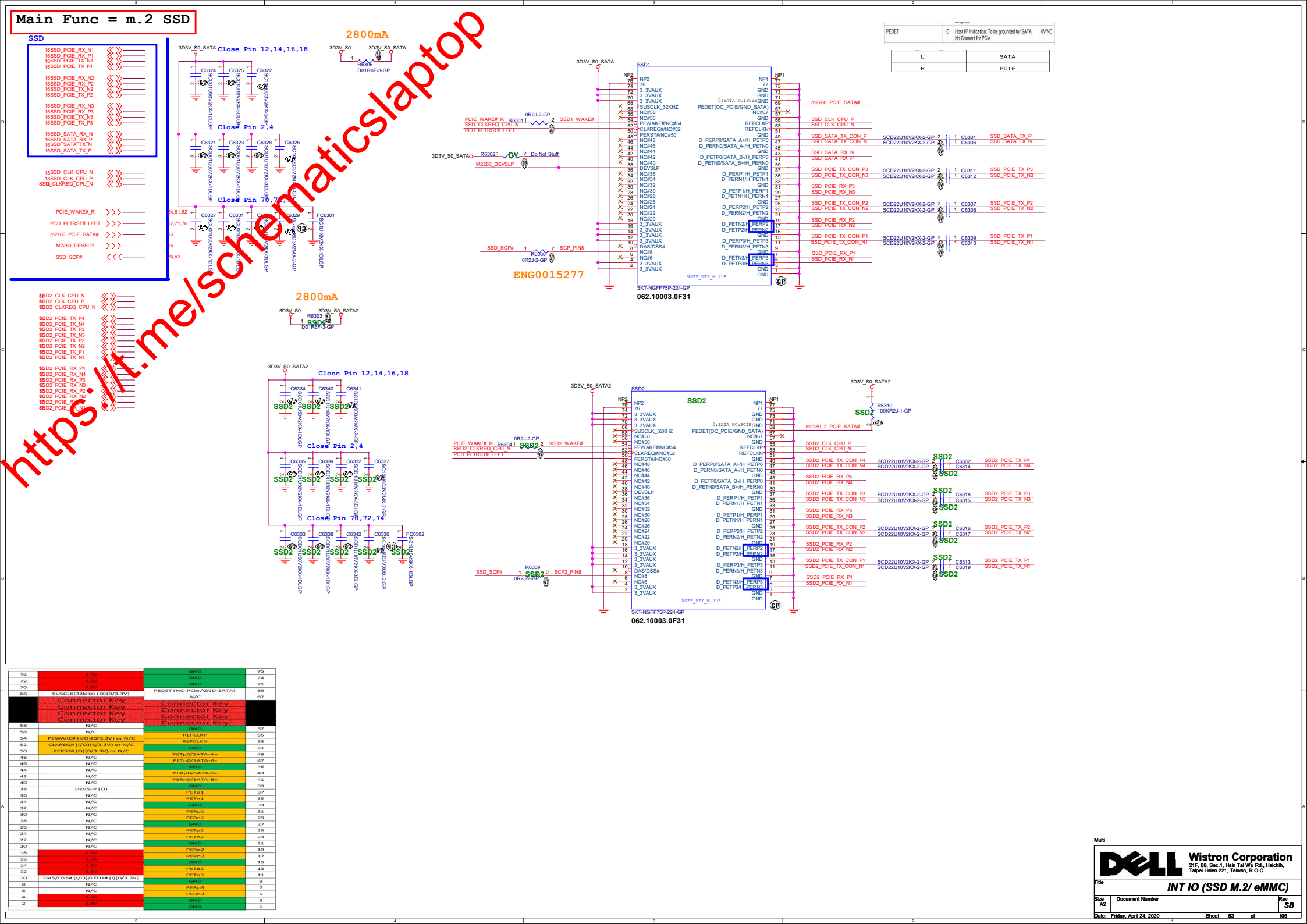
Title: INT IO WWAN

Size: A2 — Document Number — Rev: SB

Date: Friday, April 24, 2020 — Sheet 62 of 106

Main Func = m.2 SSD



74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

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Title: INT IO (SSD M.2/ eMMC)

Size: A2 | Document Number | Rev: SB

Date: Friday, April 24, 2020 | Sheet 63 of 106

Main Func = LED/HALL/Button

BAT2_LED#
BAT1_LED#
LED_MASK#
KBC_PWRBTN#
LID_CL_SIO#_R
MASK_BASE_LEDS#_Q
BREATH_LED#
FPR_DET#
M_BIST
ACAV_IN
RSMRST#_KBC
3D3V_LID
LID_CL_SIO#_R

R6412 0R2J-2-GP
Q6401
BAT2_LED#
LED_MASK#
LED_BATLOW
LED_BATCHG
LED_MASK#
BAT1_LED#
Do Not Stuff
Do Not Stuff
R6411 0R2J-2-GP
Stealth mode

Battery LED2(White_LED)
LOW actived from KBC GPIO

LED board
5V_S5
CLEDB1 HIG-CON6-6-GP
R6402 649R2F-GP
LED_BATCHG
BAT_WHITE_LED_A
3D3V_LID
LID_CL_SIO#_R
R6406 330R2J-3-GP
LED_BATLOW
BAT_AMBER_LED_A
020.K0270.0006

Battery LED1(Orange_LED)
LOW actived from KBC GPIO

Do Not Stuff AFTP6402
Do Not Stuff AFTP6403
BAT_WHITE_LED_A
BAT_AMBER_LED_A
EC6401 Do Not Stuff
EC6402 Do Not Stuff
LED_BATLOW
LED_BATCHG

3D3V_S5
C6402 SCD1U16V2KX-3DLGP
C6404 SCD1U16V2KX-3DLGP
LID_CL_SIO#_R
LED_MASK#
MASK_BASE_LEDS#_Q
FPR_DET#
MASK_BASE_LEDS#
U6402
TC7SZ08FU-LJ-CT-GP
073.7SZ08.000G
R6405 Do Not Stuff
R6409 Do Not Stuff
OTHER
POWERBT

POWER BUTTON

KBC_PWRBTN#
PWRBT1
SW-TACT-4P-218-GP
062.40004.0111
2nd:062.40001.0981
EC6410 Do Not Stuff

BREATH_LED#
MASK_BASE_LEDS#
Q6404
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
BREATH_LED#_D
Q6405 LDTA144VLT1G-GP
5V_S5
R6404 1KR2J-1-GP
BREATH_LED#_C
BREATH_SWLED1#_A
LED1
LED-W-45-GP
83.19213.H70
084.00144.0B11
R1=47K /R2=10K

Resistor already reserve on EC side

Power LED
LOW actived from KBC GPIO

BREATH_SWLED1#_A
EC6411 Do Not Stuff

M-BIST

3D3V_S5
RSMRST#_KBC
R6410 Do Not Stuff
R6403 330KR2F-L-GP
M_BIST
ACAV_IN
D6403 Do Not Stuff
C6405 SC2D2U10V3KX-1DLGP-U
R6408 Do Not Stuff
Q6407
DDTA144EUA-7-F-GP
84.00144.K11
Q6407_B
Q6407_C
BAT_AMBER_LED_A
R6413 150R2F-1-GP
Q6406 MMBT3904WT1G-1-GP
84.M3904.D11
KBC_PWRBTN#
Do Not Stuff

Multi

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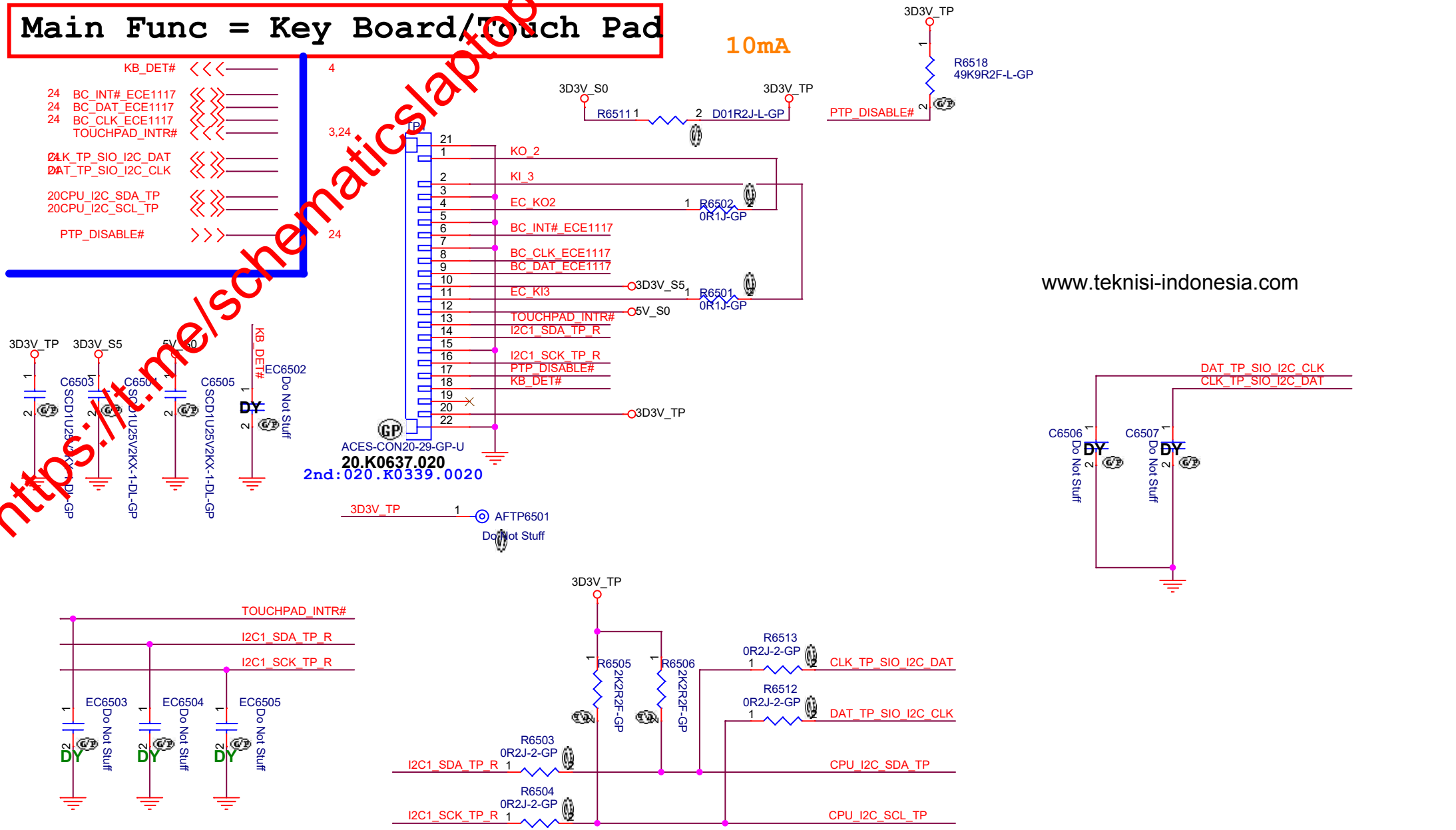
Title: LED / Button / Power Button

Size	Document Number	Rev
Custom		SB

Date: Friday, April 24, 2020 Sheet 64 of 106

Main Func = Key Board/Touch Pad

10mA



Multi

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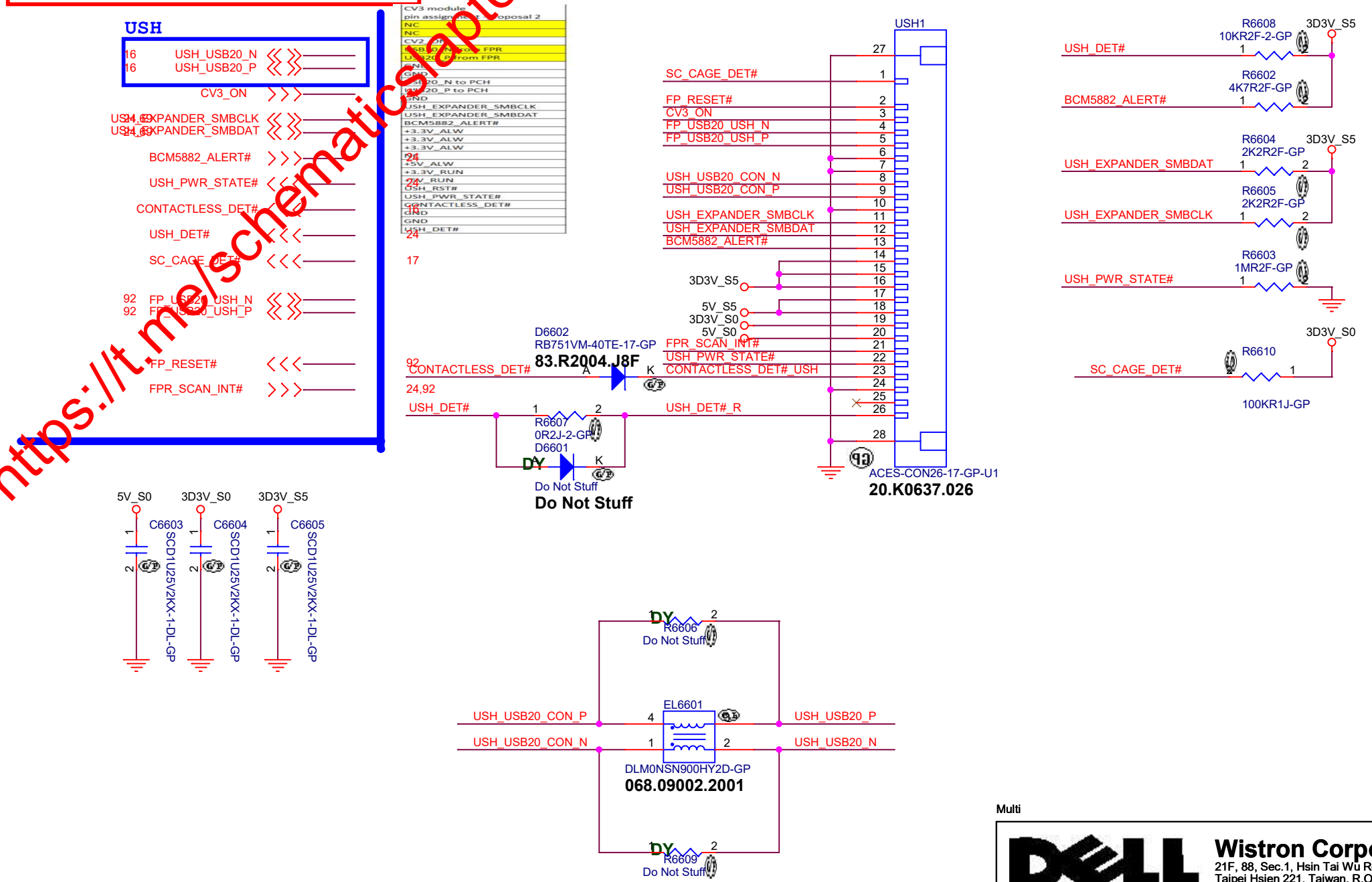
Title: **INT IO (KB/TP)**

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 65 of 106

Main Func = USH BD



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Title: **IO Board Conn (USH)**

Size	Document Number	Rev
A4		SB

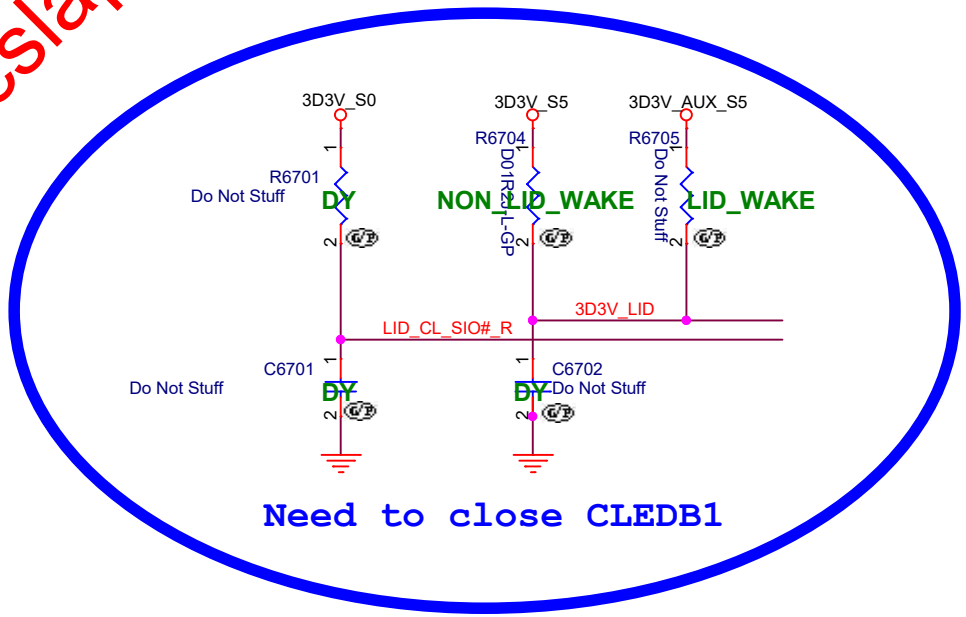
Date: Friday, April 24, 2020 Sheet 66 of 106

Main Func = Sensor (Hall-Sensor)

24,55,64 LID_CL_SIO#_R

3D3V_LID

64



Need to close CLEDB1

Multi

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Title: Sensor (Hall-Sensor)

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 67 of 106

Main Func = Debug

ME_FWP_PCH
ME_FWP
CPU_UART2_TXD
CPU_UART2_RXD
SIO_SLP_S3#
SIO_SLP_S5#
SIO_SLP_S4#
SIO_SLP_A#
RTC_RST#
KBC_PWRBTN#
SYS_RESET#
SIO_SLP_S0#
ESPI_IO0
ESPI_IO1
ESPI_IO2
ESPI_IO3
ESPI_CS#
ESPI_RESET#
ESPI_CLK
JTAG_TDI
JTAG_TMS
JTAG_CLK
JTAG_TDO
MSCLK
MSDATA
HOST_DEBUG_TX
SBIOS_TX
SPI_CLK_DEBUG
SPI_SI_DEBUG
SPI_SO_DEBUG
SPI_WP_DEBUG
SPI_HOLD_DEBUG
SPI_CS_DEBUG_N0
SPI_CS_DEBUG_N1
SPI_CLK_CPU
SPI_SI_CPU
SPI_WP_CPU
SPI_HOLD_CPU
SPI_CS_CPU_N0
SPI_CS_CPU_N1
PROM_BIOS_R

Firmware SW

R6819 Do Not Stuff
ME_FWP_PCH — DX — ME_FWP
Install after MP
R6820 1KR2F-1-GP
3D3V_S5_PCH
ME_FWP
ME_FWP_PCH
MESW1_B
MESW1 COM
DEBUG
SW-SLIDE3P-36-GP
062.40006.0151

ME_FWP_PCH	A	B
	Low	High
	Normal Operation (Default)	Override

ESPI DEBUG (Wistron)

ESPI2
ESPI_CLK
ESPI_RESET#
ESPI_CS#
ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0
ESPI_DEBUG_PWR
DEBUG_TX
CPU_UART2_TXD
CPU_UART2_RXD
R6818 0R2J-2-GP
R6817 0R2J-2-GP
3D3V_S0
HOST_DEBUG_TX
DEBUG
ACES-CON14-11-GP
20.F1637.014

ESPI DEBUG (DELL)

3D3V_S0
ESPI1
ESPI_IO0
ESPI_IO1
ESPI_IO2
ESPI_IO3
ESPI_CS#
ESPI_RESET#
ESPI_CLK
DEBUG
ACES-CON10-60-GP-U
020.K0156.0010

teknisi indonesia

APS DEBUG

APS1
3D3V_S5_PCH
SIO_SLP_S3#
SIO_SLP_S5#
SIO_SLP_S4#
SIO_SLP_A#
RTC_RST#
KBC_PWRBTN#
SYS_RESET#
SIO_SLP_S0#
DEBUG
SUYIN-ETY-CON18-2-GP
20.K0493.018

SPI DEBUG

R1
SPI1
R6808 0R1J-GP SPI_CS_DEBUG_N1
R6809 10R1F-GP SPI_SI_DEBUG
R6810 10R1F-GP SPI_SO_DEBUG
R6811 10R1F-GP SPI_CLK_DEBUG
R6812 0R1J-GP SPI_CS_DEBUG_N0
R6813 10R1F-GP SPI_WP_DEBUG
R6814 10R1F-GP SPI_HOLD_DEBUG
SPI_CS_CPU_N1
SPI_SI_CPU
SPI_SO_CPU
SPI_CLK_CPU
SPI_CS_CPU_N0
SPI_WP_CPU
SPI_HOLD_CPU
3D3V_SPI_R1
PROM_BIOS_R
3D3V_SPI
D6802 SBA0520Q-R1-00001-GP-U
R6815 0R2J-2-GP
DEBUG
083.00520.0F8F
52mA
ACES-CON20-29-GP-U
20.K0637.020

3D3V_S5_PCH — D6801 — 3D3V_SPI_R1
SBA0520Q-R1-00001-GP-U
083.00520.0F8F
58mA

MP change to short pad

JTAG

3D3V_S5
R6821 49D9R2F-GP
RN6801 SRN10KJ-6-GP
R6804 10KR2F-2-GP 5107
R6803 100KR2F-L1-GP 5200
R6807 10KR2F-2-GP 5107
R6805 10KR2F-2-GP
JTAG1
JTAG_PU
JTAG_TDI
JTAG_TMS
JTAG_CLK
JTAG_TDO
MSCLK
MSDATA
HOST_DEBUG_TX_C
UART0_TXD_R
R6802 0R2J-2-GP HOST_DEBUG_TX
R6816 0R2J-2-GP
DEBUG
DX — R6806 Do Not Stuff — SBIOS_TX
ACES-CON10-28-GP-U
20.K0460.010
R6801 pull DN, Enable JTAG debug mode
MSDATA R6801 1 2 10KR2F-2-GP 5107
MSCLK R6822 1 2 10KR2F-2-GP 5200

Multi

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Title: Debug (LPC debug)
Size: A3 | Document Number | Rev: SB
Date: Friday, April 24, 2020 | Sheet 68 of 106

Main Func = Sensor (E-compass/A+Gyro/SAR)

20 GSEN_INT1

CPU_I2C_SCL_SENSOR

CPU_I2C_SDA_SENSOR

USH_EXPANDER_SMBDAT

USH_EXPANDER_SMBCLK

3D3V_SEN_S0 — F6901 — 3D3V_S0

FUSE-D5A63V-1-GP

069.4R500.0091

3D3V_S5_WWAN

R6902 Do Not Stuff — CPU_I2C_SDA_SAR_CON — DY

R6903 Do Not Stuff — CPU_I2C_SCL_SAR_CON — DY

3D3V_SEN_S0

R6904 2K2R2F-GP — CPU_I2C_SDA_SENSOR

R6905 2K2R2F-GP — CPU_I2C_SCL_SENSOR

SENBD1

11 — 3D3V_SEN_S0

1 — 3D3V_S5_WWAN

2

3

4 — CPU_I2C_SDA_SAR_CON

5 — CPU_I2C_SCL_SAR_CON

6 — CPU_I2C_SDA_SENSOR

7 — CPU_I2C_SCL_SENSOR

8 — GSEN_INT1

9

10

12

ACES-CON10-GP-U

20.F2255.010

Q6902

CPU_I2C_SDA_SAR_CON 6 — 1 CPU_I2C_SDA_SENSOR

3D3V_S0 5 — DY — 2 3D3V_S0

CPU_I2C_SCL_SENSOR 4 — 3 CPU_I2C_SCL_SAR_CON

Do Not Stuff

Do Not Stuff

Q6901

CPU_I2C_SDA_SAR_CON 1 — 6 USH_EXPANDER_SMBDAT

3D3V_S5_WWAN 2 — DY — 5 3D3V_S5_WWAN

USH_EXPANDER_SMBCLK 3 — 4 CPU_I2C_SCL_SAR_CON

Do Not Stuff

Do Not Stuff

ED6901

CPU_I2C_SDA_SENSOR 2

DY 3

CPU_I2C_SCL_SENSOR 1

Do Not Stuff

Do Not Stuff

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Title: ***Sensor (GYROSCOPE/PRESSUE/ALS)***

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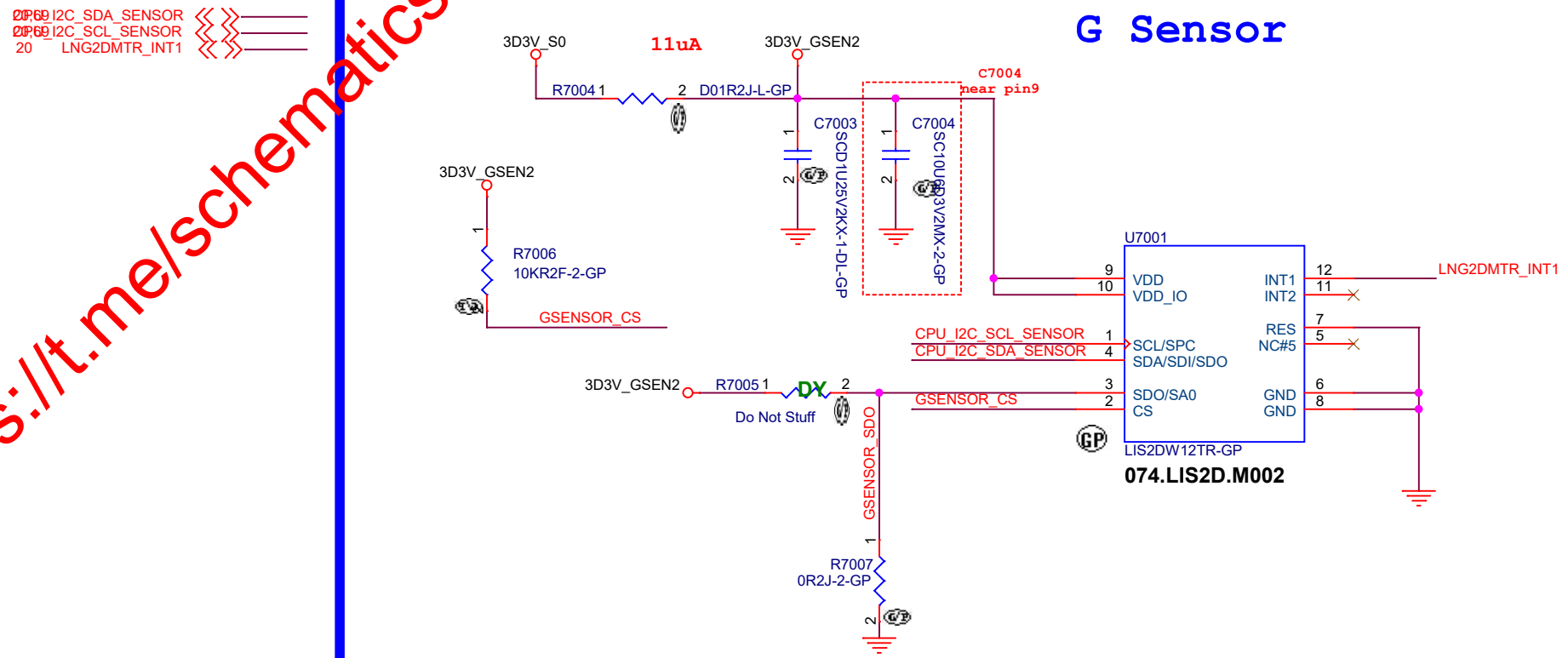
Main Func = G-sensor

G Sensor



Multi

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Title: ***Sensor (G-sensor)***

Size	Document Number	Rev
A4		SB

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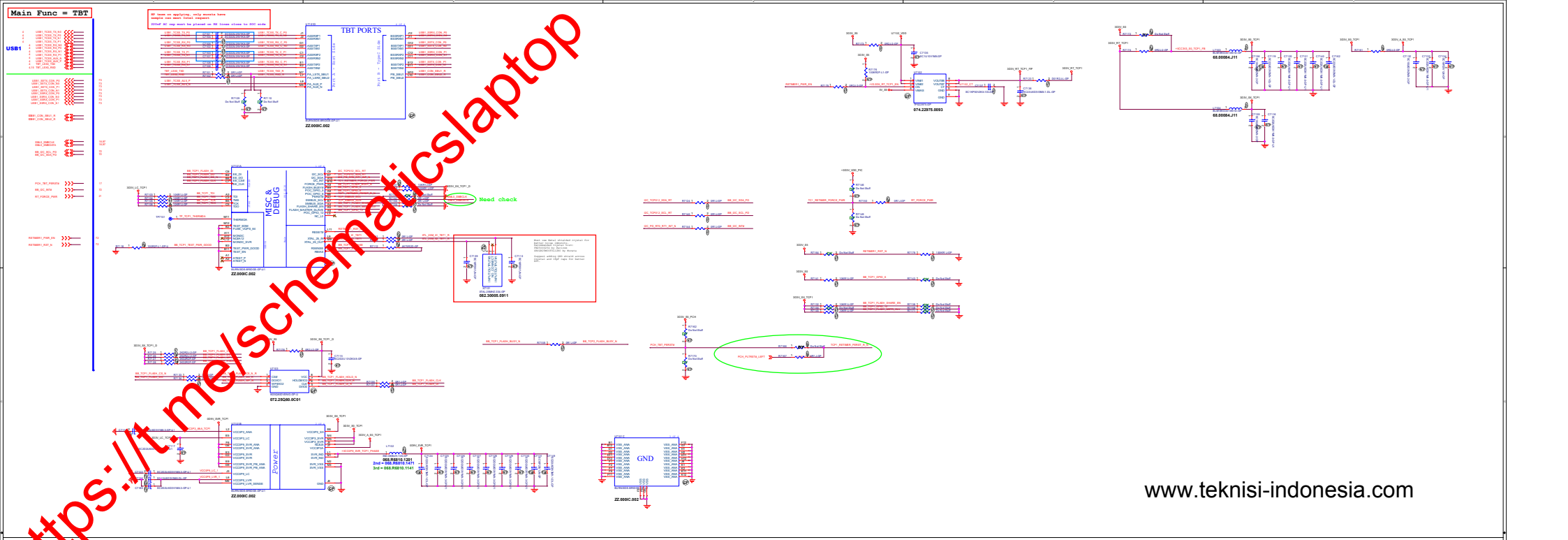
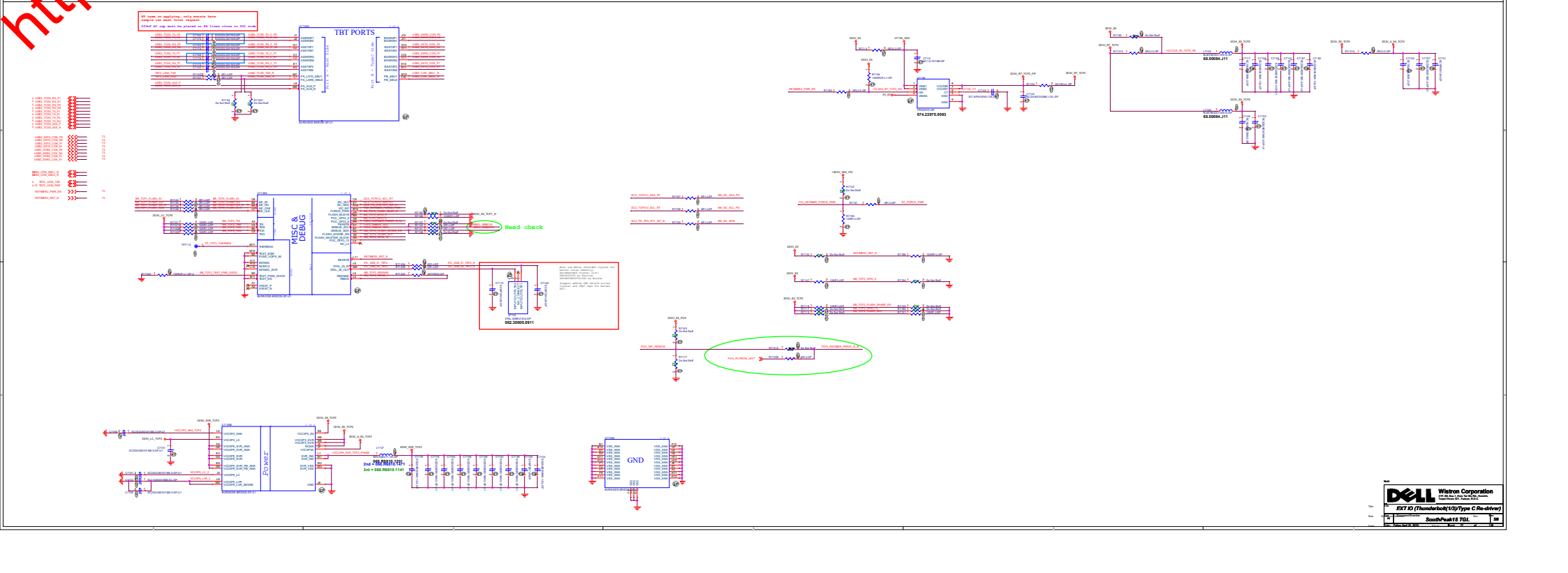
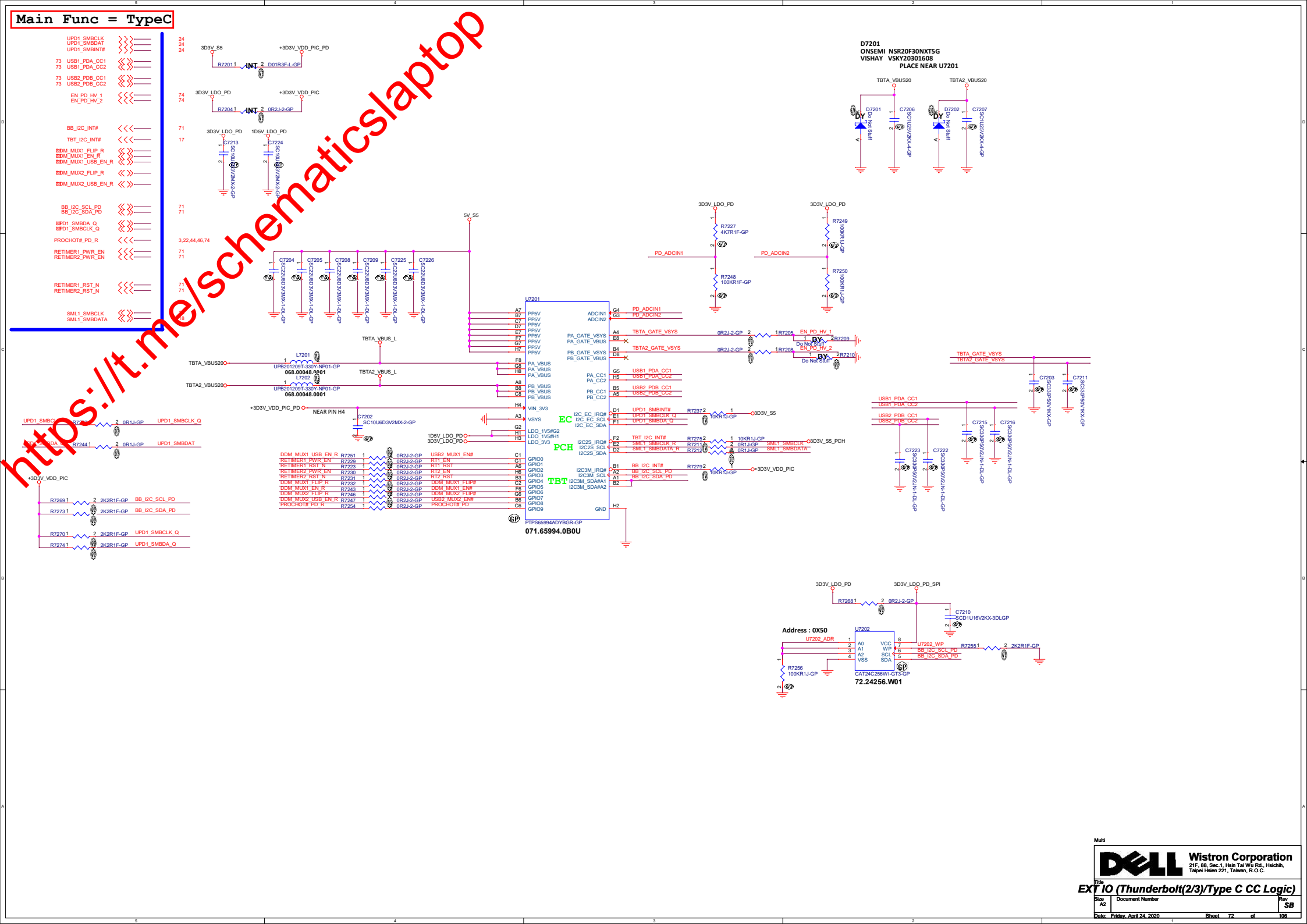
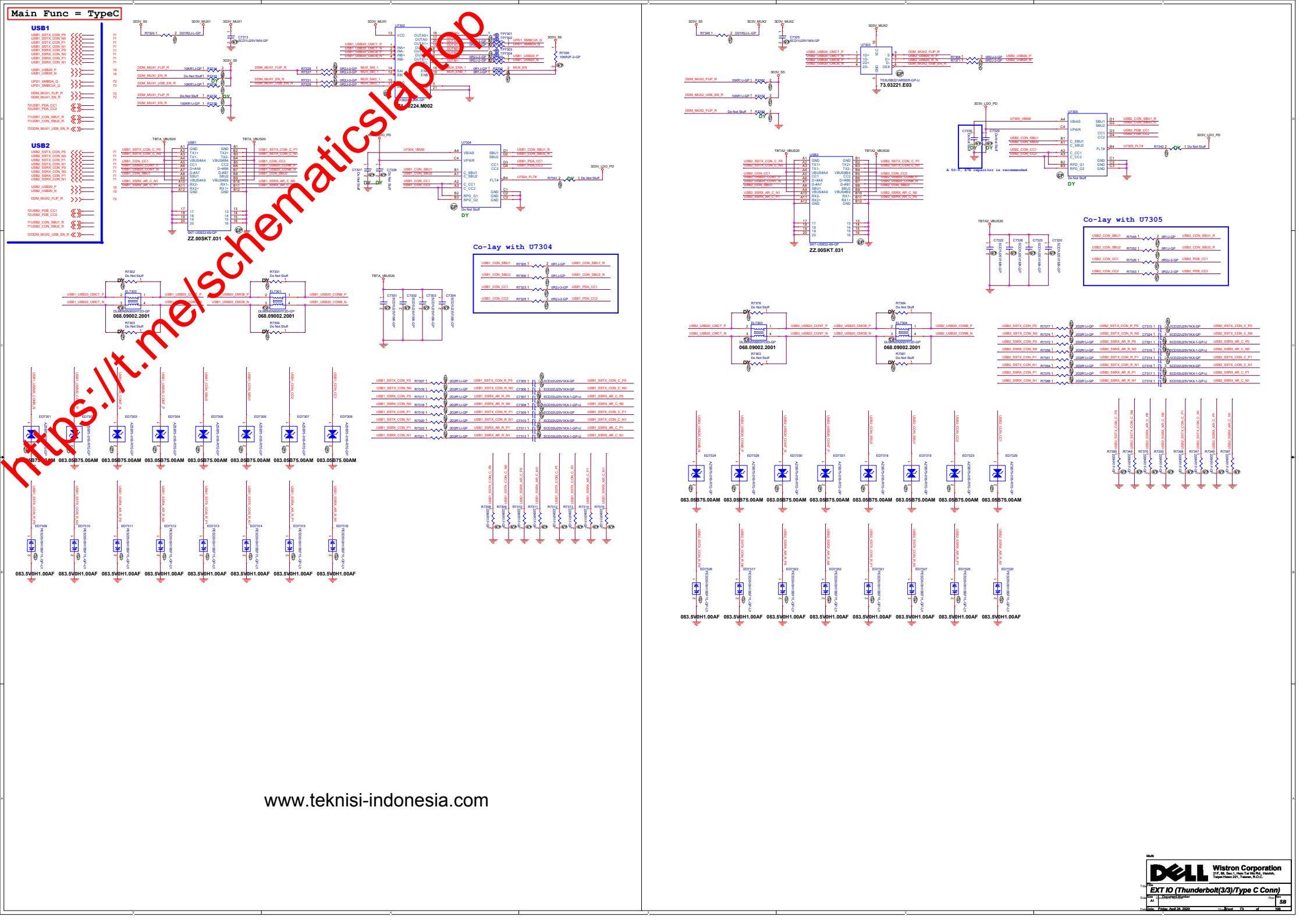


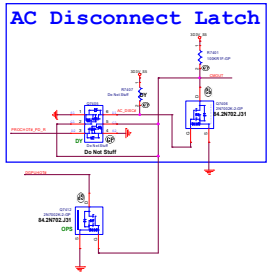



Main Func = TypeC
https://t.me/schematicslaptop
D7201
ONSEMI NSR20F30NXT5G
VISHAY VSKY20301608
PLACE NEAR U7201
U7201
PTPS65994ADYBGR-GP
071.65994.0B0U
EC
PCH
TBT
U7202
CAT24C256WI-GT3-GP
72.24256.W01
Address : 0X50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
EXT IO (Thunderbolt(2/3)/Type C CC Logic)
Size A2
Document Number
Rev SB
Date: Friday, April 24, 2020
Sheet 72 of 106

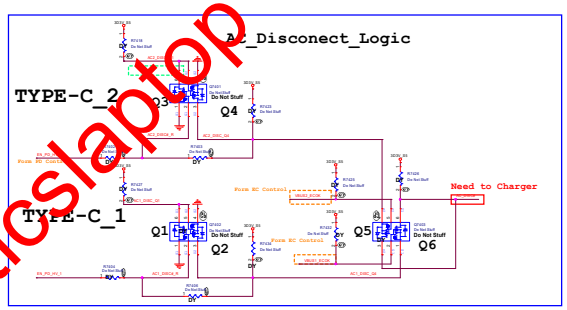

Main Func = TypeC
USB1
USB2
Co-lay with U7304
Co-lay with U7305
ZZ.00SKT.031
A4.00224.M002
73.03221.E03
www.teknisi-indonesia.com
https://t.me/schematicslaptop
Wistron Corporation
EXT IO (Thunderbolt(3/3)/Type C Conn)
Friday, April 24, 2020

Main Func = TypeC

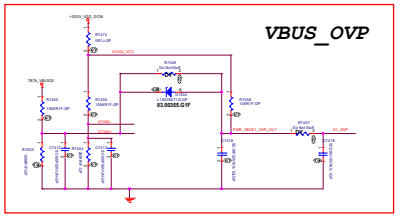
AC Disconnect Latch

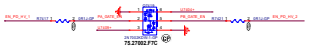


AC_Disconect_Logic

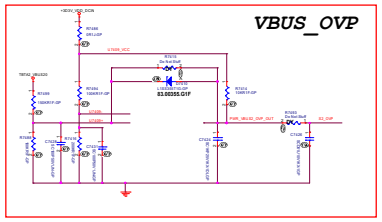


VBUS_OVP

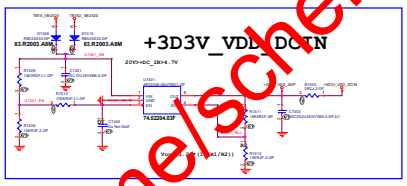




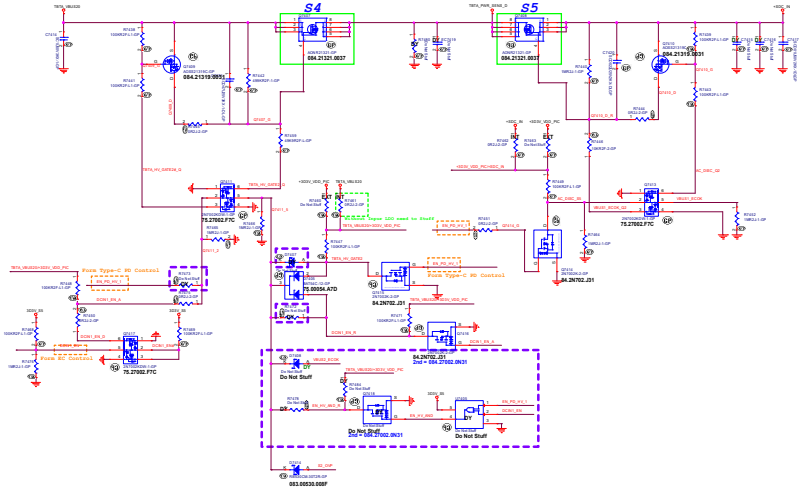
VBUS_OVP



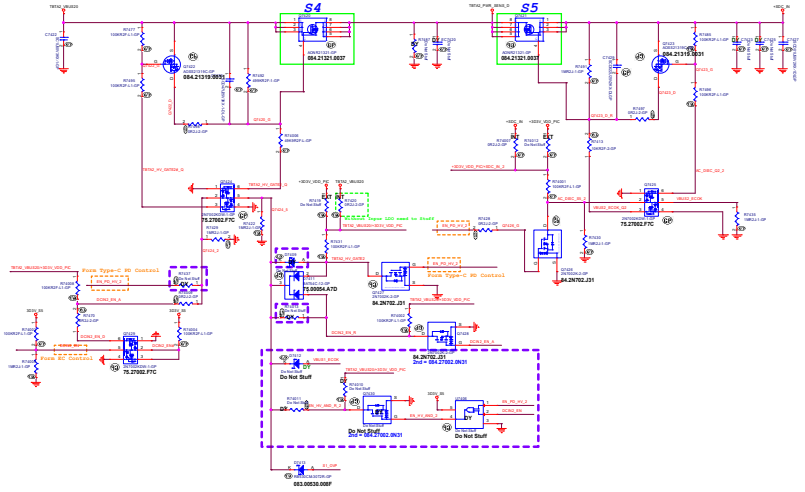
+3D3V_VDD_DCIN



TYPE-C 1



TYPE-C 2



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EXT IO (TYPEC PD)

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Title

EXT IO (RSVD)

Size	Document Number	Rev
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PEX_CLKREQ0# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.

DGPU_PWROK 19,24,85

GFX_CLK_CPU_P 18
GFX_CLK_CPU_N 18
GFX_CLKREQ_CPU_N 18

DGPU_HOLD_RST# 19

GFX_PCIE_RX_P0 16
GFX_PCIE_RX_N0 16
GFX_PCIE_TX_P0 16
GFX_PCIE_TX_N0 16

GFX_PCIE_RX_P1 16
GFX_PCIE_RX_N1 16
GFX_PCIE_TX_P1 16
GFX_PCIE_TX_N1 16

GFX_PCIE_RX_P2 16
GFX_PCIE_RX_N2 16
GFX_PCIE_TX_P2 16
GFX_PCIE_TX_N2 16

GFX_PCIE_RX_P3 16
GFX_PCIE_RX_N3 16
GFX_PCIE_TX_P3 16
GFX_PCIE_TX_N3 16

PCH_PLTRST#_LEFT 17,68,71

SYS_PEX_RST_MON# 79

EMI Reserved

GPU_PEX_RST#

EC7601 DY Do Not Stuff

R7602 10KR2J-GP OPS

dGPU Reset

U7601 OPS 74LVC1G08GW-T-GP
73.01G08.L04
2nd = 73.7SZ08.DAH

DGPU_HOLD_RST#
PCH_PLTRST#_LEFT
SYS_PEX_RST_MON#

1D8V_AON_S0

R7606 100KR1J-GP OPS

1D8V_VGA_S0

1D8V_AON_S0

R7603 10KR2J-3-GP OPS

GFX_CLKREQ_CPU_N

Q7601 PJA138KA-GP OPS
084.00138.0A31
2nd = 084.00138.0C31

SYS_PEX_RST_MON#

R7613 0R2J-2-GP OPS

GPU_PEX_RST#

GFX_CLKREQ_dGPU_N

GPU1A 1 OF 14
1/14 PCI_EXPRESS

PEX_WAKE# AA14
PEX_RST# AC7
PEX_CLKREQ# AC6
PEX_REFCLK AE8
PEX_REFCLK* AD8

GFX_CLK_CPU_P
GFX_CLK_CPU_N

PEX_TX0 AC9
PEX_TX0* AB9
PEX_RX0 AG6
PEX_RX0* AG7
PEX_TX1 AB10
PEX_TX1* AC10
PEX_RX1 AF7
PEX_RX1* AE7
PEX_TX2 AD11
PEX_TX2* AC11
PEX_RX2 AE9
PEX_RX2* AF9
PEX_TX3 AC12
PEX_TX3* AB12
PEX_RX3 AG9
PEX_RX3* AG10
PEX_TX4 AB13
PEX_TX4* AC13
PEX_RX4 AF10
PEX_RX4* AE10
PEX_TX5 AD14
PEX_TX5* AC14
PEX_RX5 AE12
PEX_RX5* AF12
PEX_TX6 AC15
PEX_TX6* AB15
PEX_RX6 AG12
PEX_RX6* AG13
PEX_TX7 AB16
PEX_TX7* AC16
PEX_RX7 AF13
PEX_RX7* AE13
PEX_TX8 AD17
PEX_TX8* AC17
PEX_RX8 AE15
PEX_RX8* AF15
PEX_TX9 AC18
PEX_TX9* AB18
PEX_RX9 AG15
PEX_RX9* AG16
PEX_TX10 AB19
PEX_TX10* AC19
PEX_RX10 AF16
PEX_RX10* AE16
PEX_TX11 AD20
PEX_TX11* AC20
PEX_RX11 AE18
PEX_RX11* AF18
PEX_TX12 AG21
PEX_TX12* AB21
PEX_RX12 AG18
PEX_RX12* AG19
PEX_TX13 AD23
PEX_TX13* AE23
PEX_RX13 AF19
PEX_RX13* AE19
PEX_TX14 AF24
PEX_TX14* AE24
PEX_RX14 AE21
PEX_RX14* AF21
PEX_TX15 AG24
PEX_TX15* AG25
PEX_RX15 AG21
PEX_RX15* AG22

PEX LANES 15 - 4 ARE DEFEATURED

OPS

N18S-G5-A1-GP

PEX_CVDD AA22

PCIE/PLL DIGITAL PWR
PEX_DVDD_1 AB23
PEX_DVDD_2 AC24
PEX_DVDD_3 AD25
PEX_DVDD_4 AE26
PEX_DVDD_5 AE27
PEX_DVDD_6

1V Interface

PCIE/PLL ANALOG PWR
PEX_HVDD_1 AA10
PEX_HVDD_2 AA12
PEX_HVDD_3 AA13
PEX_HVDD_4 AA16
PEX_HVDD_5 AA18
PEX_HVDD_6 AA19
PEX_HVDD_7 AA20
PEX_HVDD_8 AA21
PEX_HVDD_9 AB22
PEX_HVDD_10 AC23
PEX_HVDD_11 AD24
PEX_HVDD_12 AE25
PEX_HVDD_13 AF26
PEX_HVDD_14 AF27

1.8V Interface

PEX_PLL_HVDD_1 AA8
PEX_PLL_HVDD_2 AA9

PEX_TERMP AF25

R7601 2K49R2F-GP OPS

1V_VGA_S0

1U 0201*6 X6S
Place under GPU
C7627 C7628 C7629 C7630 C7631 C7632 SC1U4V9MX-1NF-GP OPS

4.7U 0603*3 X6S
Place under GPU
C7633 SC4D7U10V9KX-6-GP OPS
C7634 C7635 Do Not Stuff DY

10U 0805*3 X6S
Place near GPU
C7650 Do Not Stuff DY
C7624 SC10U6D3V9KX-5DN-GP OPS
C7623 SC10U6D3V9KX-5DN-GP OPS

22U 0603*2 X6S
Place near GPU
C7636 SC22U6D3V3MX-9-GP-U OPS
C7637 SC22U6D3V3MX-9-GP-U OPS

1U 0201*7 X6S
Place under GPU
1D8V_VGA_S0
C7638 C7639 C7640 C7641 C7642 C7643 C7652 SC1U4V1MX-1NF-GP OPS DY Do Not Stuff

4.7U 0603*3 X6S
Place under GPU
C7645 Do Not Stuff DY
C7646 SC4D7U10V3KX-6GP OPS
C7647 Do Not Stuff DY

10U 0603*3 X6S
Place near GPU
C7648 Do Not Stuff DY
C7649 SC10U6D3V3MX-7-GP-U OPS
C7651 SC10U6D3V3MX-7-GP-U OPS

22U 0603*2 X6S
Place near GPU
C7660 SC22U6D3V3MX-9-GP-U OPS
C7661 SC22U6D3V3MX-9-GP-U OPS

1U 0201*1 X6S
Place under GPU
1D8V_VGA_S0
C7644 SC1U4V9MX-1NF-GP OPS

Multi

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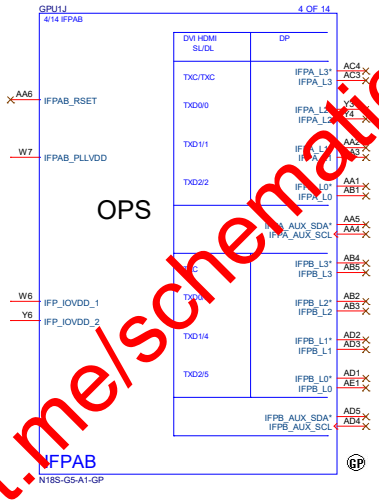
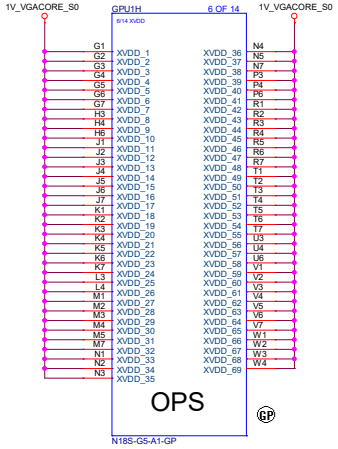
Title: GPU_960M_PEG (1/5)

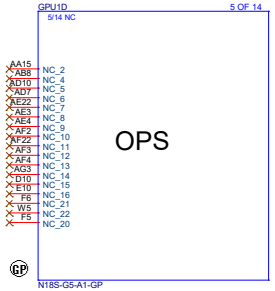
Size: A2 | Document Number: SouthPeak15 TGL | Rev: SB

Date: Friday, April 24, 2020 | Sheet 76 of 106

Main Func = dGPU







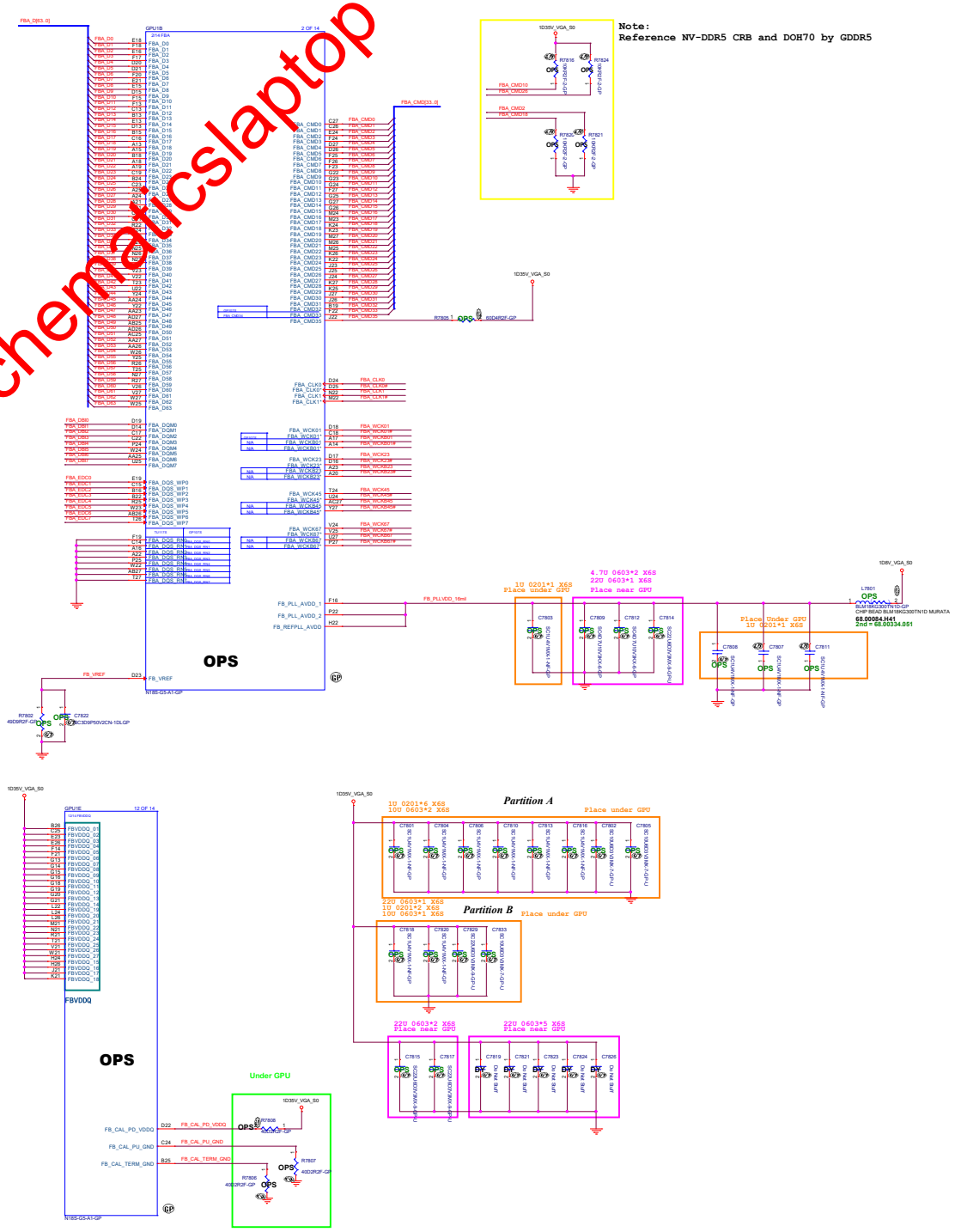
Multi

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU DIGITALOUT (2/5)	
Size A2	Document Number SouthPeak15 TGL	Rev SB
Date: Friday, April 24, 2020	Sheet 77 of 106	

Group A

Group B

Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5



Multi

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File: GPU_VRAM I/F (3/5)

Size: A1 | Document Number: SouthPeak15 TGL | Rev: SB

Date: Friday, April 24, 2020 | Sheet 29 of 106

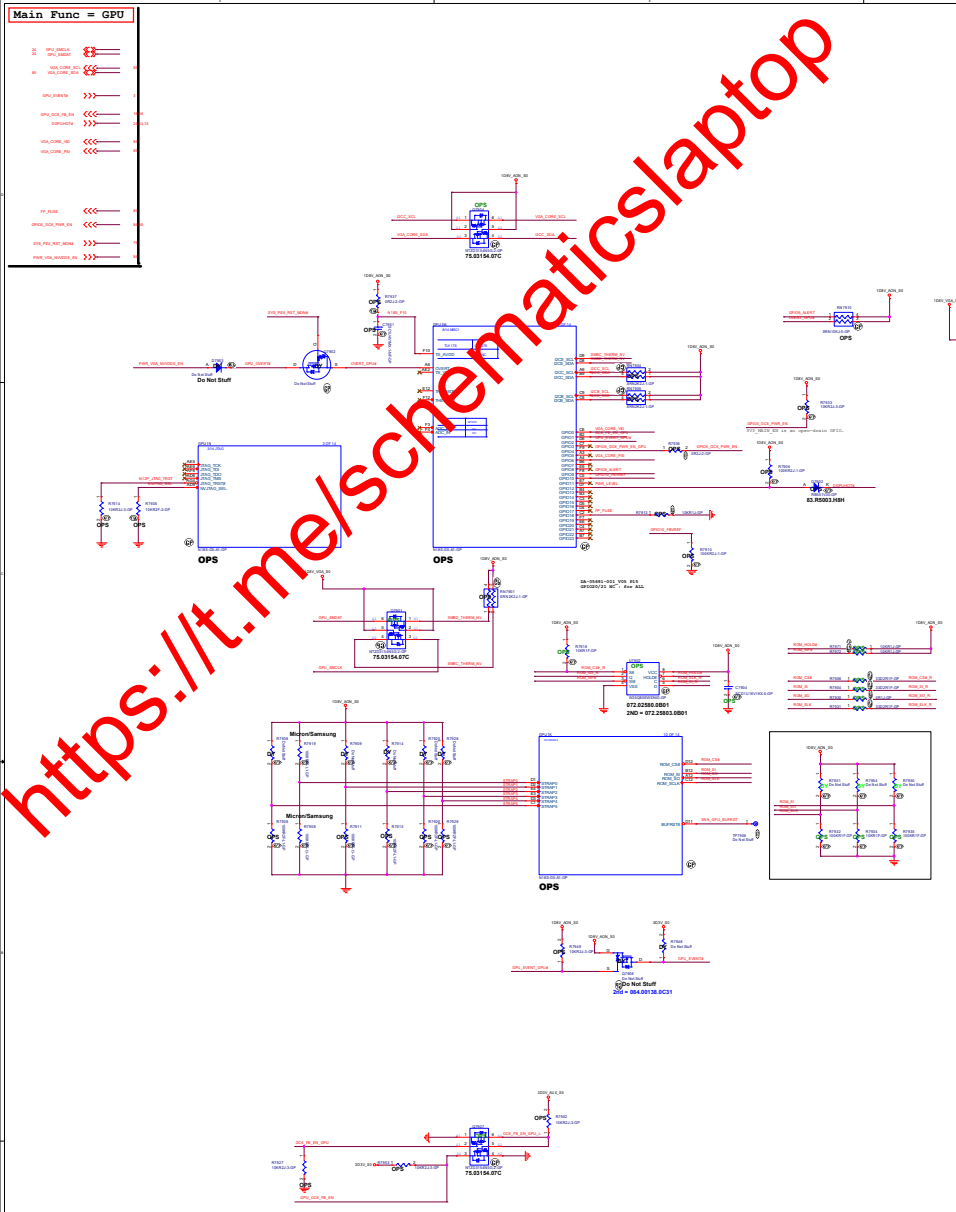


Table 11. N18S-G5-B, N18S-G5 and N18S-LP GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[3]	Full	Production candidate

Notes:
1. For N18S-G5-B, N18S-G5 and N18S-LP, the maximum allowable memory case temperature is 95 °C.
2. Before the date code is available, the specially screened Micron memory (for 11 Gbps @ 1.2V support) will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
3. Before the date code is available, the specially screened Samsung memory (for 11 Gbps @ 1.2V support) is identified by "SPL" letters inserted before the seven digits in its lot ID.

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED

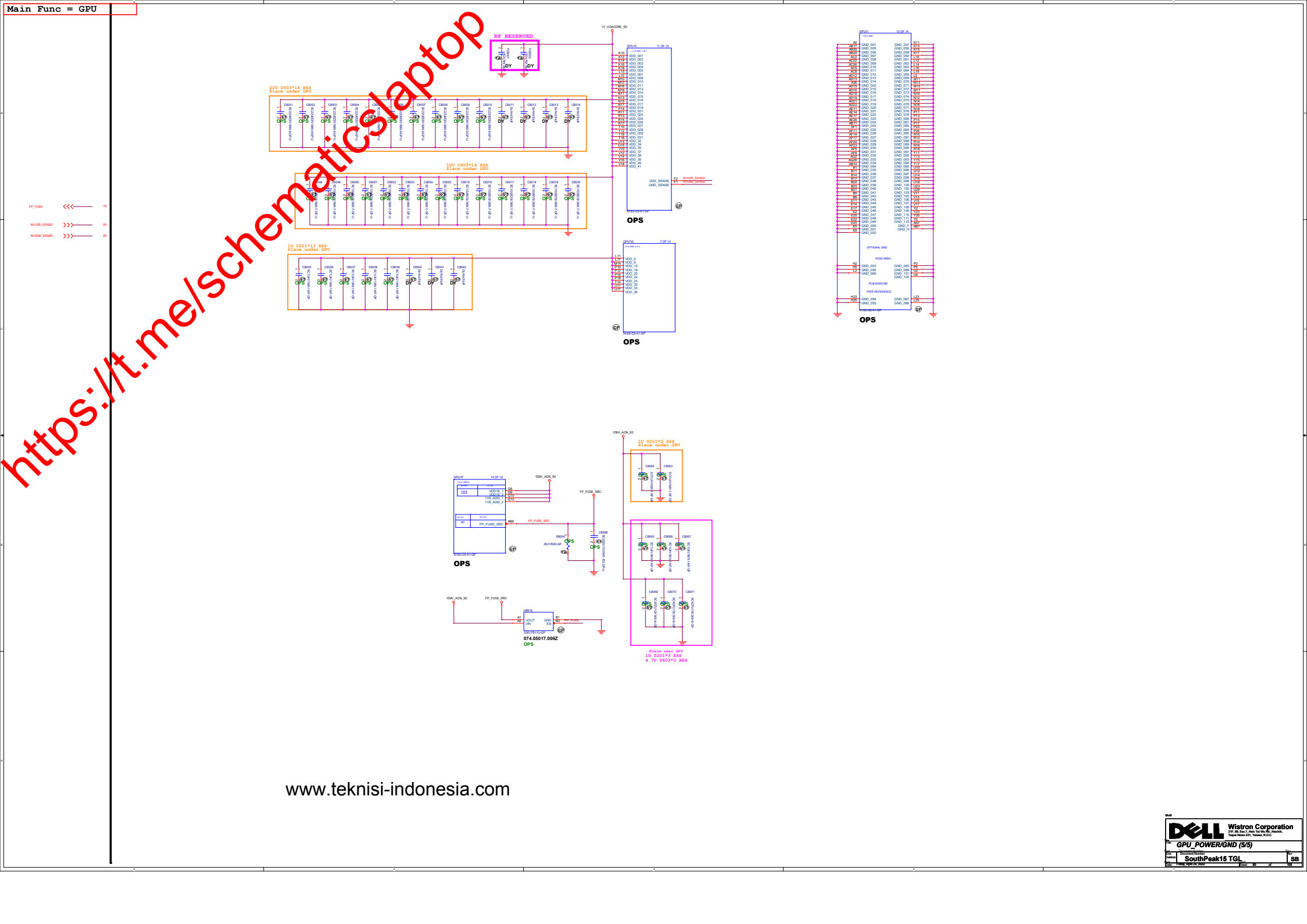
Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Strap Pin	N18/GB2E-64
ROM_SI	Pull low to enable FS_OVERT*
ROM_SO[1]	
ROM_CLK	
STRAP5	• SMB_ALT_ADDR • DEVID_SEL • PCIE_CFG • VGA_DEVICE
STRAP4	
STRAP3	
STRAP2	RAMCFG[4:0]
STRAP1	
STRAP0	

Note
1. The ROM_SO pin should be pulled low using a 10 kΩ resistor for N18/GB2E-64 GPUs and using a 100 kΩ resistor for N17/GB2D-64/GB2C-64 GPUs.

Main Func = GPU



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Title: GPU_POWER/GND (5/5)

Size: Custom | Document Number: SouthPeak15 TGL | Rev: SB

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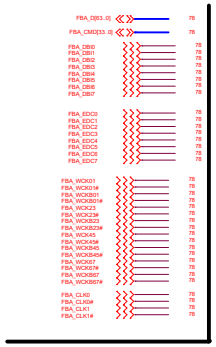
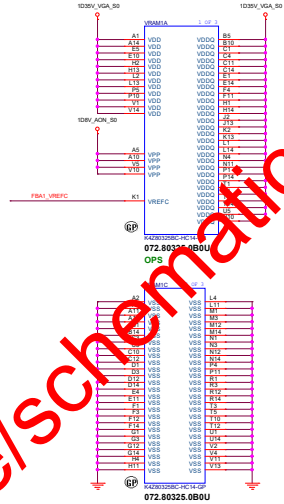
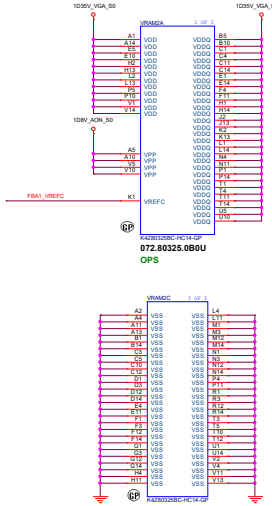






8.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for CMD and ADDR). Figure 8.8 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values.

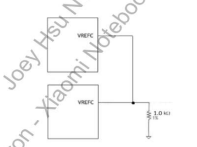
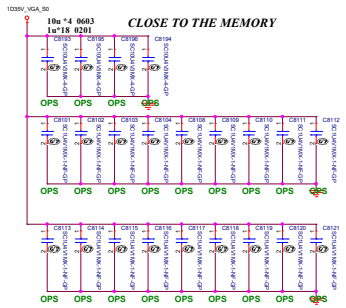
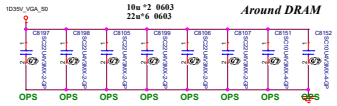


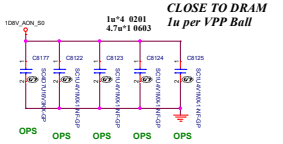
Figure 8.8 Use of Integrated VREFC for ×16 Mode

FOR VRAM1

PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE

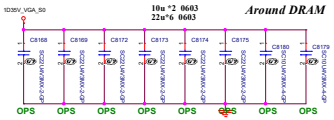


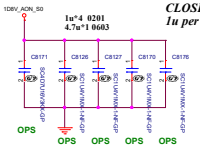


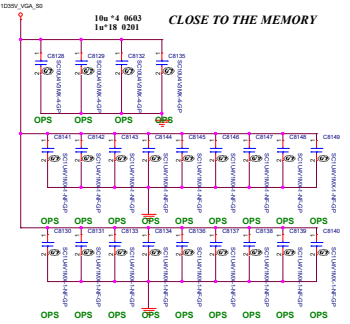


FOR VRAM2

PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE







Multi

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File: VRAM 1,2 (1/4)

Size	Document Number	Rev
A1	SouthPeak15 TGL	SB
Date: Friday, April 24, 2020	Sheet 81 of 186	

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Title: VRAM 3,4 (2/4)

Size	Document Number	Rev
A1	SouthPeak15 TGL	SB

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Title: *VGA Power A*

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 83 of 106

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Title: *VGA Power B*

Size	Document Number	Rev
A4	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 84 of 106

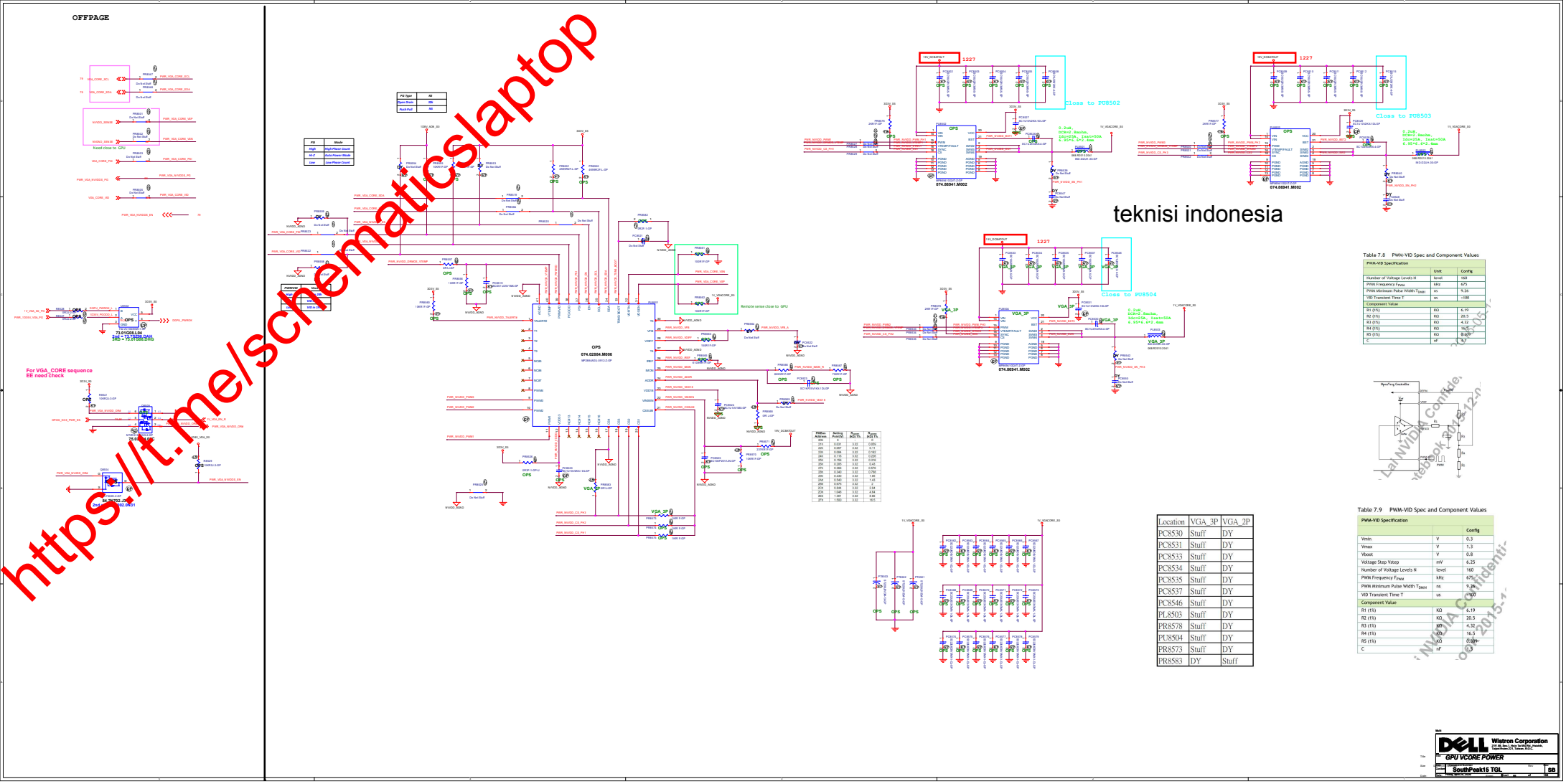

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	~100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Location	VGA_3P	VGA_2P
PC8530	Stuff	DY
PC8531	Stuff	DY
PC8533	Stuff	DY
PC8534	Stuff	DY
PC8535	Stuff	DY
PC8537	Stuff	DY
PC8546	Stuff	DY
PL8503	Stuff	DY
PR8578	Stuff	DY
PU8504	Stuff	DY
PR8573	Stuff	DY
PR8583	DY	Stuff

Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		
		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	~100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Wistron Corporation
GPU VCORE POWER
SouthPeak15 TGL

OFFPAGE

Main Func = dGPU

[09-07158-001 Rev03]Power up sequence:
3.3V ==> 3VVDD (VGA_CORE) ==> 1.05V ==> PEXVDD/Q (1.35V)

3D3V_S0 to 3D3V_AON_S0 and 3D3V_VGA_S0

dGPU Power Discharge Circuit

1V_VGA_S0

VGA_CORE

1D35V_VGA_S0

1D8V_AON_S0

1D8V_VGA_S0

1D8V_AON_S0 to 1D8V_VGA_S0

RT5797 for 1V_VGA_S0

For tuning VGA_CORE sequence.

1V_VGA_S0

Table 1	
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.86V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

GPU	FBVDD Voltage	FBMA0	FBMA1	FBMA2
N18P-G62	(P0/1.25V,P3/P5/P8/1.2V)	4.75K	8.06K	64.9K
N19P-Q3	(P0/P3/P5/P8/1.25V)	4.75K	8.06K	NC

OCP setting
96.3K -> OCP = 96.5A

SS setting

Iccmax : 38A
OCP : 60A

Power 1228

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GPU GDDR 1D35V
Stradale CML-H

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Title: *Discharge*

Size	Document Number	Rev
A2	SouthPeak15 TGL	SB

Date: Friday, April 24, 2020 Sheet 87 of 106

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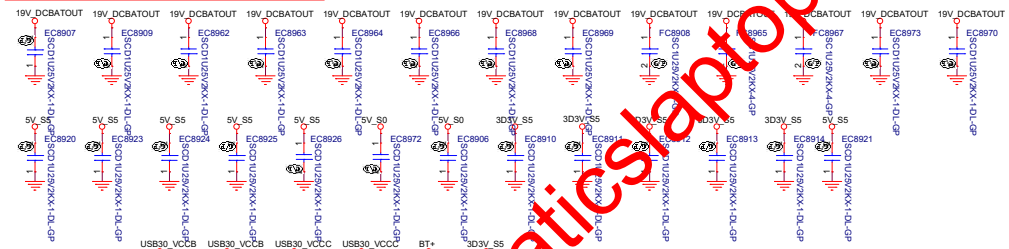
Title

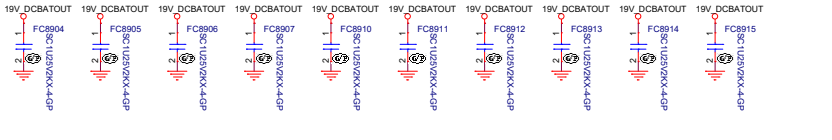
UNUSED PARTS (RSVD)

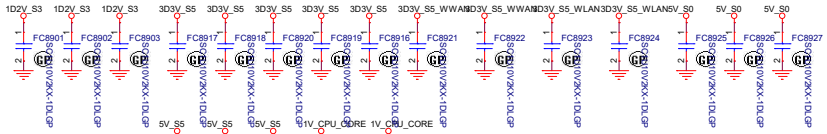
Size	Document Number	Rev
A4		SB

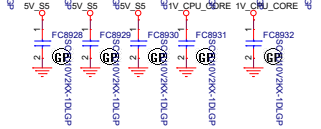
Date: Friday, April 24, 2020 Sheet 88 of 106

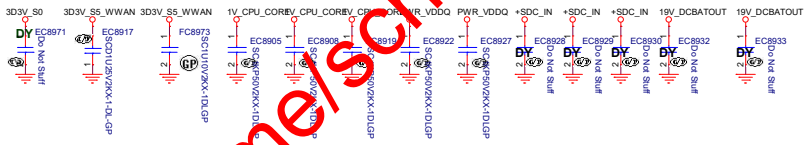
Main Func = EMC/ RF

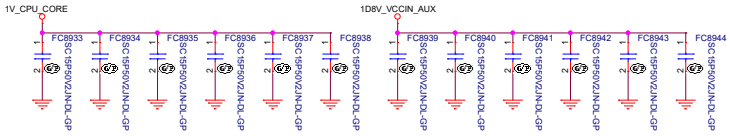


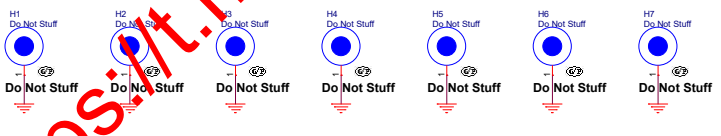


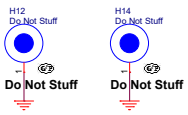


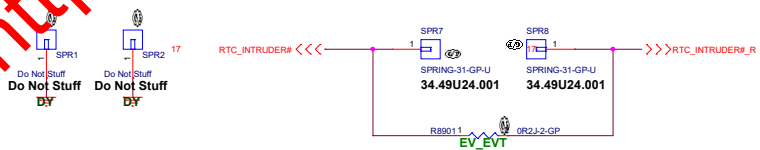


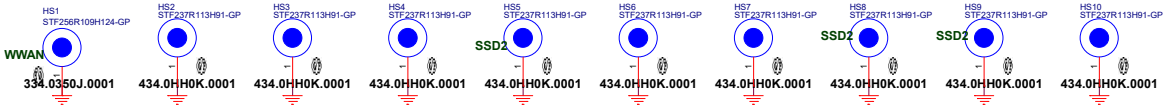


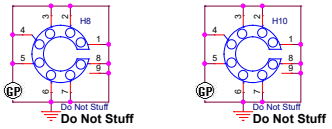


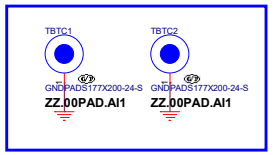






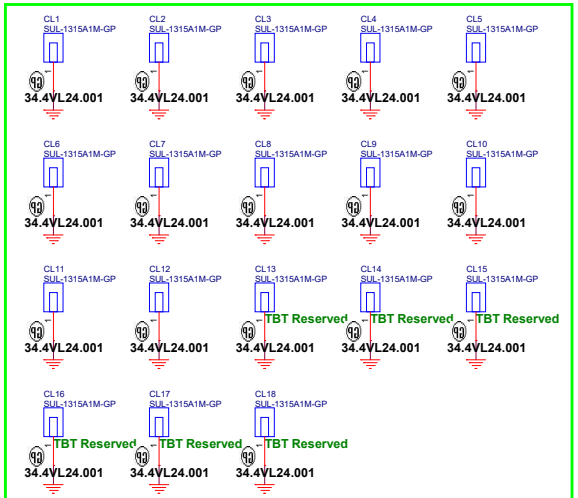


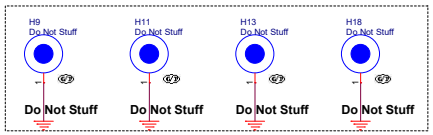




TBT XTAL shielding can

434.0M601.0001





Layout need

Multi

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Title: UNUSED PARTS (RF/EMI Capacitors)

Size: A2 | Document Number | Rev: SB

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Multi

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Title

INT IO (RSVD) (NFC)

Size	Document Number	Rev
A4		*SB*

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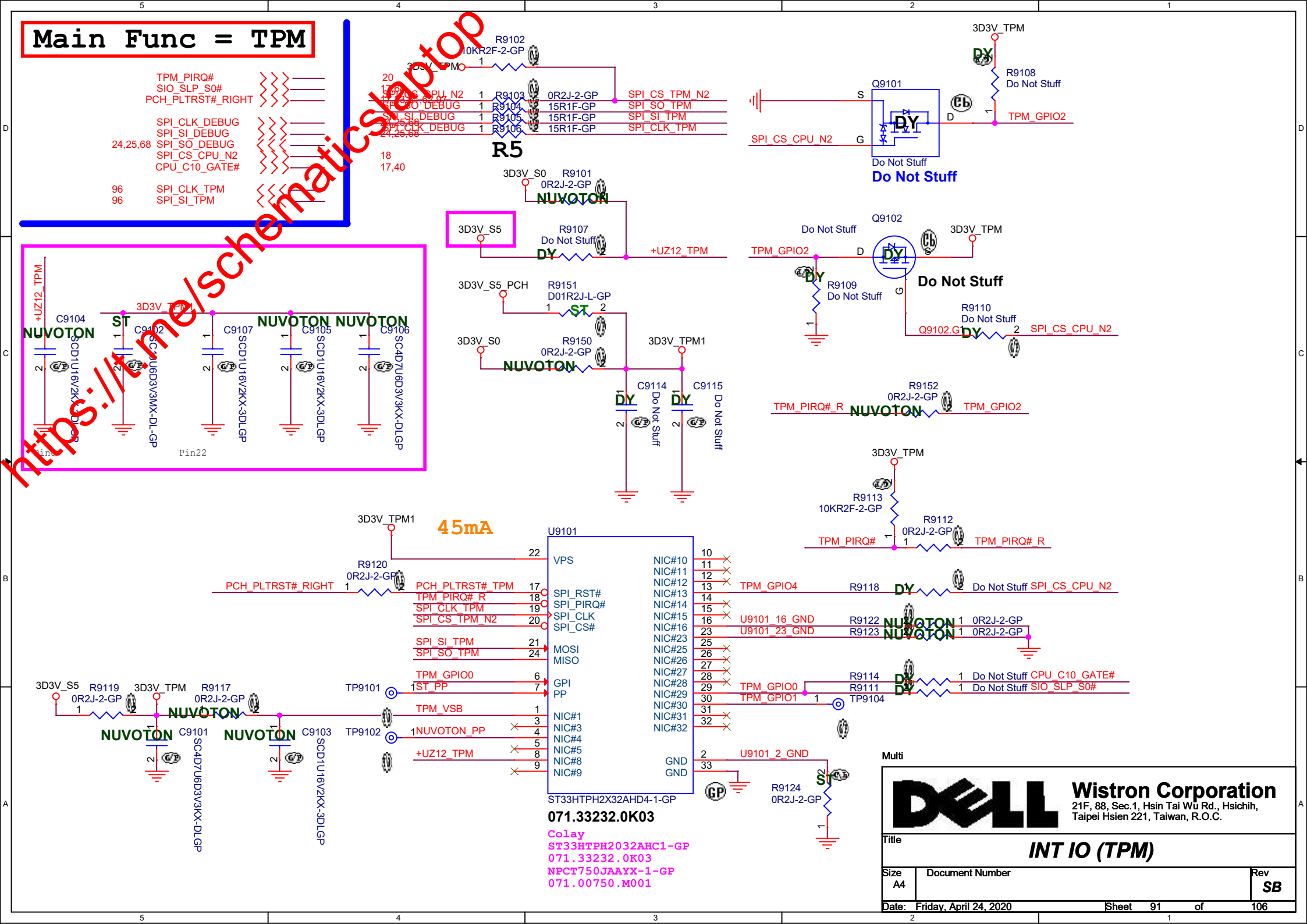
Main Func = TPM



Multi

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Title: **INT IO (TPM)**

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 91 of 106

Main Func = Finger Printer

FP_USB20_P		
FP_USB20_N		
FPR_DET#		24,64
USB20_USH_N		
USB20_USH_P		
FPR_PWR_EN#		24
FPR_SCAN_INT#		24,66
FPR_SSO_EN#		24
FPR_UEFI_MGMT#_R		24
FPR_LOW_PWR_MODE#		24
FP_RESET#		66
FPR_LED#		24
MASK_BASE_LEDS#_Q		64

Try to co-lay

PCH

R9208 Do Not Stuff FP_USB20_N — FP_USB20_R_N
R9209 Do Not Stuff FP_USB20_P — FP_USB20_R_P

USH

R9206 0R2J-2-GP FP_USB20_R_N — FP_USB20_USH_N
R9207 0R2J-2-GP FP_USB20_R_P — FP_USB20_USH_P

3D3V_S0_FP
R9216 0R2J-2-GP
FP_PH
R9212 Do Not Stuff FPR_UEFI_MGMT#_R
R9213 10KR2F-2-GP FPR_SSO_EN#
R9214 10KR2F-2-GP FPR_LOW_PWR_MODE#
3D3V_S5
R9220 Do Not Stuff FPR_PWR_EN#

3D3V_S0_FP
R9204 10KR2F-L1-GP
EC9202 Do Not Stuff
FPR_DET#
FPR_LED_4
FPR_LED_3
FPR_LED_2
FPR_LED_1
FPR_LOW_PWR_MODE#
FPR_UEFI_MGMT#_R
FPR_SCAN_INT#_R
FP2
FOX-CONN16D-1-GP
20.F2321.016
2nd:20.F2448.016
FP_USB20_CON_P
FP_USB20_CON_N
FP_RESET#_R
FPR_SSO_EN#
3D3V_S0_FP
R9215 100KR2J-1-GP
EC9203 Do Not Stuff

3D3V_S5
R9205 D01R2J-L-GP
Q9202 PJA3415AE-GP
3D3V_FP_PWR
C9202 Do Not Stuff
R9219 Do Not Stuff
C9204
084.03415.0C31
3D3V_S0_FP_R
R9217 D01R2J-L-GP
C9203 Do Not Stuff
FPR_PWR_EN#
R9224 20KR1J-GP
FPR_PWR_EN#_R
C9208 Do Not Stuff

100mA

EU9202
FP_USB20_CON_N
FP_USB20_CON_P
AZ5315-02F-GP
83.05315.0A0

5V_S5
Q9204 PJA3415AE-GP
C9205 Do Not Stuff
R9230 10KR1J-GP Do Not Stuff
C9206
084.03415.0C31
FP_LED_D
R9225 100R2J-2-GP FPR_LED_1
R9226 100R2J-2-GP FPR_LED_2
R9227 100R2J-2-GP FPR_LED_3
R9228 100R2J-2-GP FPR_LED_4
Q9207
FPR_LED#
MASK_BASE_LEDS#_Q
FP_LED_EN#
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
R9231 20KR1J-GP
FP_LED_EN#_R
C9207 Do Not Stuff

R9202 0R2J-2-GP
EL9201
FP_USB20_CON_P — FP_USB20_R_P
FP_USB20_CON_N — FP_USB20_R_N
Do Not Stuff
Do Not Stuff
R9201 0R2J-2-GP

3D3V_S0_FP 3D3V_S0_FP
R9211 100KR2F-L1-GP
FPR_SCAN_INT#_R
Q9203
2N7002K-2-GP
84.2N702.J31
3D3V_S5
R9222 100KR2F-L-GP
FPR_SCAN_INT#
R9223 Do Not Stuff
FP_RESET#_R
D9202A
RB751VM-40TE-17-GP
83.R2004.J8F
R9221 Do Not Stuff
FP_RESET#

Multi

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Title: INT IO (Finger Printer)
Size: A3 | Document Number | Rev: SB
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Multi

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Title
EXT IO (RSVD) (Express Card/PCIE slot)

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 93 of 106

Multi

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Title
EXT IO (RSVD) (Smart Card/COM/PS2)

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 94 of 106

Multi

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Title

EXT IO (RSVD) (Docking/LPT)

Size	Document Number	Rev
A4		SB

Date: Friday, April 24, 2020 Sheet 95 of 106

SPI

Close CPU1

SPI_CLK_CPU	STCPU1CC	18,68	Do Not Stuff
SPI_SO_CPU	STCPU1C1	18,68	Do Not Stuff

Close ROM(U2501)

SPI_CLK_ROM2	STU2501AC	25	Do Not Stuff
SPI_SI_ROM2	STU2501A1	25	Do Not Stuff

Close TPM(U9101)

SPI_CLK_TPM	STU9101AC	91	Do Not Stuff
SPI_SI_TPM	STU9101A1	91	Do Not Stuff

HDA

Close CPU1

HDA_BCLK	STCPU1AC	19	Do Not Stuff
HDA_SDI0	STCPU1A1	19,27	Do Not Stuff

Close Codec(U2701)

HDA_BITCLK_CODEC_R	STU2701AC	27	Do Not Stuff

Close Codec(U2701)

HDA_SDOUT_CODEC_R	STU2701A1	27	Do Not Stuff

SDIO

Close CARD1

SD_CLK_CON	STCARD1AC	33	Do Not Stuff
SD_DATA0_CON	STCARD1A1	33	Do Not Stuff
SD_DATA1_CON	STCARD1A2	33	Do Not Stuff

Close Codec(U2701)

SD_DATA2_CON	STCARD1A3	33	Do Not Stuff
SD_DATA3_CON	STCARD1A4	33	Do Not Stuff
SD_CMD_CON	STCARD1A5	33	Do Not Stuff

ESPI

Close CPU1

ESPI_CPU_CLK_R	STCPU1BC	18	Do Not Stuff
ESPI_CPU_IO0_R	STCPU1B1	18	Do Not Stuff
ESPI_CPU_IO1_R	STCPU1B2	18	Do Not Stuff
ESPI_CPU_IO2_R	STCPU1B3	18	Do Not Stuff
ESPI_CPU_IO3_R	STCPU1B4	18	Do Not Stuff

Close EC(U2401)

ESPI_CLK	STU2401AC	18,24,68	Do Not Stuff
ESPI_IO0	STU2401A1	18,24,68	Do Not Stuff
ESPI_IO1	STU2401A2	18,24,68	Do Not Stuff
ESPI_IO2	STU2401A3	18,24,68	Do Not Stuff
ESPI_IO3	STU2401A4	18,24,68	Do Not Stuff

Multi

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Title: Commercial (RSVD) (SW GFX eDP)

Size: A3 | Document Number | Rev: SB

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Main Func = LAN

LAN

16LAN_PCIE_RX_N
16LAN_PCIE_RX_P
16LAN_PCIE_TX_N
16LAN_PCIE_TX_P

PCH_PLTRST#_RIGHT
17 LAN_WAKE#
PM_LANPHY_ENABLE
SML0_SMBCLK
SML0_SMBDATA
32 LAN_0_GREEN_LINK_N
32 LAN_1_AMBER_ACT_N
LOM_CABLE_DETECT#
LAN_MDI0_P
LAN_MDI0_N
LAN_MDI1_P
LAN_MDI1_N
LAN_MDI2_P
LAN_MDI2_N
LAN_MDI3_P
LAN_MDI3_N
LAN_CLK_CPU_N
LAN_CLK_CPU_P
LAN_CLKREQ_CPU_N

DESIGN NOTE: LAN_DISABLE_N must be connected to PCH's GPIO/LANPHYPC output. This GPIO pin must be set as "LANPHYPC" function through FITC tool. The signal does not require pull-up. R15 resistor is no-stuff default (for testing purpose).

3D3V_LAN
R9701 DY Do Not Stuff
PM_LANPHY_ENABLE
R9702 DY Do Not Stuff
17,33,61,62,91
17

U9701 WGI219LM-GP
071.219LM.0003

LAN_CLKREQ_CPU_N 48 CLK_REQ#
PCH_PLTRST#_RIGHT 36 PE_RST#
LAN_CLK_CPU_P 44 PE_CLKP
LAN_CLK_CPU_N 45 PE_CLKN
PCIE

LAN_PCIE_RX_P C9701 SCD1U16V2KX-3DLGP LAN_PCIE_RX_C_P 38 PETP
LAN_PCIE_RX_N C9702 SCD1U16V2KX-3DLGP LAN_PCIE_RX_C_N 39 PETN
LAN_PCIE_TX_P C9703 SCD1U16V2KX-3DLGP LAN_PCIE_TX_C_P 41 PERP
LAN_PCIE_TX_N C9704 SCD1U16V2KX-3DLGP LAN_PCIE_TX_C_N 42 PERN

MDI
MDI_PLUS0 13 LAN_MDI0_P
MDI_MINUS0 14 LAN_MDI0_N
MDI_PLUS1 17 LAN_MDI1_P
MDI_MINUS1 18 LAN_MDI1_N
MDI_PLUS2 20 LAN_MDI2_P
MDI_MINUS2 21 LAN_MDI2_N
MDI_PLUS3 23 LAN_MDI3_P
MDI_MINUS3 24 LAN_MDI3_N

SML0_SMBCLK R9704 0R2J-2-GP CPU_SMB_SCL_LAN 28 SMB_CLK
SML0_SMBDATA R9706 0R2J-2-GP CPU_SMB_SDA_LAN 31 SMB_DATA
SMBUS

LAN_WAKE# R9708 0R2J-2-GP LAN_WAKE#_R 2 LANWAKE#
PM_LANPHY_ENABLE R9710 0R2J-2-GP LAN_DISABLE# 3 LAN_DISABLE#

NOTE: DESIGN NOTE: LANWAKE_N must be connected to PCH's LANWAKE input.

LAN_0_GREEN_LINK_N 26 LED0
LAN_1_AMBER_ACT_N 27 LED1
TP9703 Do Not Stuff LAN_LED2 25 LED2
LED

TP9701 Do Not Stuff LAN_JTAG_TDI 32 JTAG_TDI
TP9702 Do Not Stuff LAN_JTAG_TDO 34 JTAG_TDO
LAN_JTAG_TMS 33 JTAG_TMS
LAN_JTAG_TCK 35 JTAG_TCK
JTAG

XTL_25M_X2_LAN 9 XTAL_OUT
XTL_25M_X1_LAN 10 XTAL_IN

R9713 1KR2F-3-GP TEST_EN 30 TEST_EN
R9714 3K01R2F-3-GP RBIAS 12 RBIAS

SVR_EN# 6 SVR_EN_N
RSVD1_VSS3P3 1 RSVD1_VCC3P3
VDD3P3_IN 5
VDD3P3 4
VDD3P3 15
VDD3P3 19
VDD3P3 29
VDD0P9 8
VDD0P9_11 11
VDD0P9 16
VDD0P9 22
VDD0P9 37
VDD0P9 40
VDD0P9 43
VDD0P9 46
VDD0P9 47
CTRL0P9 7
GND 49

R9703 0R2J-2-GP 3D3V_LAN
R9705 DY Do Not Stuff
R9707 4K7R2F-GP

3D3V_LANOUT
C9705 SC22U6D3V3MX-1-DL-GP
C9714 SCD1U16V2KX-3DLGP
R9709 0R3J-0-U-GP 3D3V_LAN
R9707 DY Do Not Stuff

VDD0P9_LAN
L9701 IND-4D7UH-200-GP-U 68.4R71D.10E
CTRL_0P9
C9708 SC22U6D3V3MX-1-DL-GP
C9709 SCD1U16V2KX-3DLGP
C9710 DY Do Not Stuff

3D3V_LAN R9711 1MR2F-GP Refer RoundRock
LAN_0_GREEN_LINK_N

LAN_0_GREEN_LINK_N
LAN_1_AMBER_ACT_N
LAN_LED2
EC9702 DY Do Not Stuff
EC9703 DY Do Not Stuff
EC9704 DY Do Not Stuff

3D3V_LAN
R9715 DY Do Not Stuff LAN_JTAG_TMS
R9716 DY Do Not Stuff LAN_JTAG_TCK
R9718 DY Do Not Stuff LAN_CLKREQ_CPU_N
R9719 DY Do Not Stuff LAN_WAKE#_R

C9711 SC15P50V2JN-DL-GP XTL_25M_X2_LAN_R
X9701
INPUT/OUTPUT#1
NO_CONNECT
INPUT/OUTPUT#3
XTAL-25MHZ-334-GP
082.30005.0911
GP
R9717 0R2J-2-GP XTL_25M_X2_LAN
R9720 1MR2F-GP
C9713 SC15P50V2JN-DL-GP XTL_25M_X1_LAN

R9712 0R2J-2-GP
LAN_0_GREEN_LINK_N LOM_CABLE_DETECT#

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Title: Commercial (Intel LAN)

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Title

Commercial (LAN Switch)

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Main Func = Debug (MIPI)

CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17

BPM_N0
BPM_N1
DBG_PMODE

3 PCH_JTAG_TCK
3 CPU_JTAG_PRDY#
3 CPU_JTAG_PREQ#
3 CPU_JTAG_TRST#
3 CPU_JTAG_TCK
3 CPU_JTAG_TDI
3 CPU_JTAG_TDO
3 CPU_JTAG_TMS
SYS_RESET#
SIO_PWRBTN#
12,13,68 CPU_SMB_SCL_DDR
12,13,68 CPU_SMB_SDA_DDR
15,18,68 SPI_SI_CPU
15,18,68 SPI_WP_CPU
17,24,64 RSMRST#_KBC
40 XDP_OVERRIDE#
3 EAR_N_TEST_NCTF

SIO_PWRBTN# — C9903 SCD1U16V2KX-3DLGP — DEBUG

1D05V_S5_XDP — R9905 0R3J-0-U-GP — 1D05V_CPU_XDP_CD — DEBUG
C9904 SCD1U16V2KX-3DLGP — DEBUG

SPI_WP_CPU — R9923 1KR1J-GP — DEBUG
3D3V_AUX_S5 — R9901 100KR1J-GP — DEBUG

CPU_JTAG_TRST# — R9904 0R1J-GP — XDP_JTAG_TRST# — DEBUG
CPU_JTAG_TDI — R9906 0R1J-GP — XDP_JTAG_TDI — DEBUG
17,68 CPU_JTAG_TDO 17,24 — R9908 0R1J-GP — XDP_JTAG_TDO — DEBUG
CPU_JTAG_TMS — R9910 0R1J-GP — XDP_JTAG_TMS — DEBUG
CPU_JTAG_TCK — R9912 0R1J-GP — XDP_JTAG_TCK — DEBUG
PCH_JTAG_TCK — R9916 0R1J-GP — XDP_JTAG_TCK1 — DEBUG
XDP_DBRESET# — R9913 0R1J-GP — SYS_RESET# — DEBUG
C9901 SCD1U16V2KX-3DLGP — DEBUG

1D05V_VCCIO_OUT — R9909 0R3J-0-U-GP — 1D05V_VCCIO_XDP — DEBUG
1D05V_S5_OUT — R9907 0R3J-0-U-GP — 1D05V_S5_XDP — DEBUG

XDP1 — STC-CONN60A-GP-U1 — 20.F0971.060 — DEBUG

XDP_JTAG_TCK	3	4	XDP_JTAG_TDO
XDP_JTAG_TDI	5	6	XDP_DBRESET#
XDP_ITP_PMODE	7	8	XDP_TRST_PD
XDP_JTAG_TRST#	9	10	CPU_JTAG_PREQ#
CPU_JTAG_PRDY#	11	12	1D05V_VCCIO_XDP
CFG16	13	14	R9902 10KR1J-GP — DEBUG
XDP_PRSNT_PIN1	15	16	
XDP_OVERRIDE#	17	18	
CFG0	19	20	
CFG1	21	22	
CFG2	23	24	
CFG3	25	26	
CFG4	27	28	
CFG5	29	30	
CFG6	31	32	
CFG7	33	34	
CFG8	35	36	SPI_SI_XDP — R9919 0 DX — Do Not Stuff — SPI_SI_CPU
CFG9	37	38	XDP_CFG0_N_R — R9924 0 DX — Do Not Stuff — CFG0
CFG10	39	40	SIO_PWRBTN#_IDP — R9926 0 DX — Do Not Stuff — SIO_PWRBTN#
CFG11	41	42	XDP_RSMRST# — R9920 0 DEBUG — 1KR1J-GP — RSMRST#_KBC
CFG12	43	44	
CFG13	45	46	
CFG14	47	48	CPU_SMB_SCL_XDP — R9922 0 DEBUG — 0R1J-GP — CPU_SMB_SCL_DDR — 3D3V_S5
CFG15	49	50	CPU_SMB_SDA_XDP — R9921 0 DEBUG — 0R1J-GP — CPU_SMB_SDA_DDR
XDP_JTAG_TCK1	51	52	3D3V_S5_XDP — R9903 2 DEBUG — 0R3J-0-U-GP
BPM_N1	53	54	
BPM_N0	55	56	
	57	58	
CFG17	59	60	
		63	
		64	XDP_CFG0_N_R — R9927 0 DX — Do Not Stuff — EAR_N_TEST_NCTF

DBG_PMODE — R9917 0R1J-GP — XDP_ITP_PMODE — DEBUG

Pull high on Page15

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Title: **Debug (XDP debug)**

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Table of Content

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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Title: Table of Content

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Change notes -

DATE	VERSON	DATE	Page	Modify list	OWNER
	X00				
	X00				
	X00				
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Bandon /NorthBay Power Up Sequence Diagram (Non_Deep Sx Platform)

Battery BATT1 — BT+ — MOS AONR21321 — DCBATOUT

Barrel Adapter DCIN1 — +DC_IN — MOS AONR21321 (S1) — AD+ — MOS AONR21321 (S2) — +SDC_IN — Chargrer ISL9538C

TypeC USB1 — TBTA_VBUS20 — MOS AONR21321 (S4) — TBTA_PWR_SENS_D — MOS AONR21321 (S5) — +SDC_IN

KBC MEC5107

DCBATOUT → Vin TPS51393RJER Vout → 3D3V_S5; PGOOD → 3D3V_PG

DCBATOUT → Vin SY8288CRAC Vout → 5V_S5; PGOOD → 5V_PG

(a) (b) ACAV_IN

(c) ALWON

VCI_OVRD_IN

VCI_OUT

GPIO013

(d) VCCDSW_EN — 3D3V_S5 5V_S5 — Vin VCNTL EN G2898KD1U Vout → 3D3V_S5_PCH; 3D3V_S5_LAN

(e) PCH_DPWROK

SIO_SLP_SUS#

19V_DCBATOUT — Vin EN TPS51397RJER Vout → 1D8V_S5; PGOOD → PWR_1D8V_POK (i)

Switching Regulator

19V_DCBATOUT 3D3V_S5 — Vin 3V3 EN MP2941BGL Vout → 1D8V_VCCIN_AUX; PGOOD → PWR_VCCAUX_PG (j)

CORE_VID1

CORE_VID2

Switching Regulator

19V_DCBATOUT 5V_S5 — Vin VCC EN APW8743CQBI Vout → PWR_VNN, PWR_1D05V; PGOOD → PWR_1D05V_PG (k)

Switching Regulator

GPIO076/PRIM_PWRGD — PRIM_PWRGD

RSMRST# (l)

ALW_PWRGD_3V_5V

PCH_RSMRST#

AND GATE → PCH_RSMRST#_R (m) → RSMRST#

eSPI_RESET# (n) → eSPI_RESET#

ACPRESENT (o) → ACPRESENT

(f) PCH_DPWROK → DSW_PWROK

SIO_SLP_SUS# (g) → SLP_SUS#

TGL U

(1) KBC_PWRBTN#

(2) SIO_PWRBTN# → GPD3/PWRBTN#

SIO_SLP_S3#

Virtual Wire

SLP_S5#

SLP_S4#

SIO_SLP_S5# (3)

SIO_SLP_S4# (4)

3D3V_S5 5V_S5 — Vin VCNTL EN RT9059GQW Vout → 2D5V_S3; PGOOD → PWR_2D5V_PG

Switching Regulator

VTT_CNTL

DCBATOUT PWR_VDDQ_VCC — Vin VCNTL S5 S3 SY8310RAC Vout → 1D2V_S3, 0D6V_S0; PGOOD → 1D2V_S3_PG

Switching Regulator

GPIO045

(8) RUN_ON_EC — AND GATE (SIO_SLP_S3#) → RUN_ON_R

5V_S5 3D3V_S5 — Vin1 Vin2 EN1 EN2 G2898KD1U Vout1 → 5V_S0; Vout2 → 3D3V_S0

Load SW

(9) RUNPWROK — LS — 1D2V_S3_PG

GPIO057/VCC_PWRGD

1D8V_S5 — Vin EN G5027RD1D Vout → 1D8V_S0

Load SW

5ms GPIO031/GPTF-OUT1

(10) IMVP_VR_ON — AND GATE (SIO_SLP_S3#) → ALL_SYS_PWRGD — LS

VCCST_PWRGD_R → VCCST_PWRGOOD

(13) VTT_CNTL → DDR_VTT_CTL

(14) PCH_PWROK → PCH_PWROK

CPU_C10_GATE#

(15) PCH_CLK_OUTPUTS

(16) SYS_PWROK → SYS_PWROK

SLP_S3#

(17) H_CPUPWRGD → PROCPWRGD

SLP_S0#

(18) PLT_RST# → PCH_PLTRST#

CPU_C10_GATE# (5)

VCCST_OVERRIDE (6)

OR GATE → VCCSTG_EN_R

Switching Regulator

1D05V_S55V_S5 — Vin VCNTL EN G5027RD1D Vout → 1D05V_VCCSTG

Load SW

SIO_SLP_S3# (7)

SIO_SLP_S0#

1D05V_S55V_S5 — Vin VCNTL EN G5027RD1D Vout → 1D05V_VCCST

Load SW

10ms GPIO106/PWROK

(11) VR_EN — (12) VR_RDY

VR_ENABLE VR_READY

IMVP8 ISL95860HRTZ

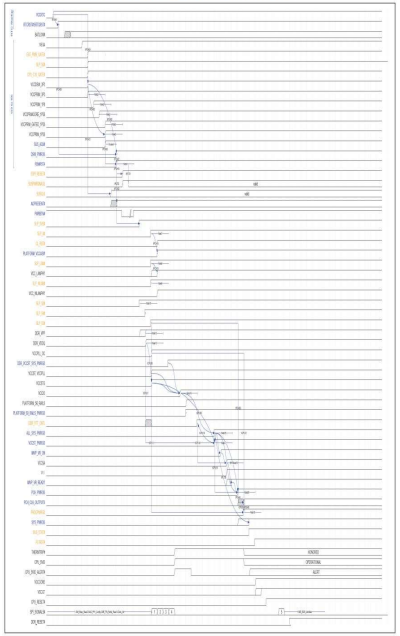
PWR_VCCIN_PWM1 — PWM AOZ5038QI Vout → 1V_CPU_CORE; FCCM ← PWR_VCCIN_FCCM_R

Switching Regulator

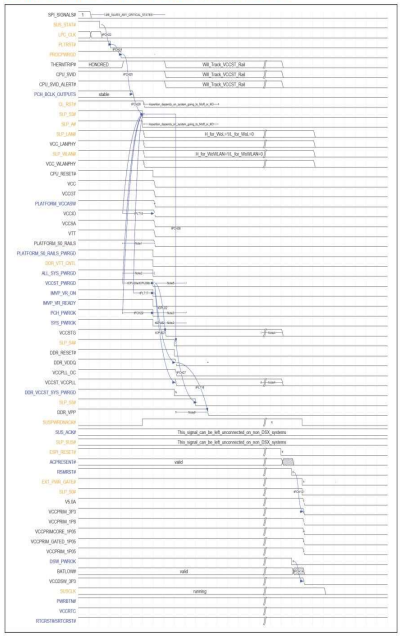
PWR_VCCIN_PWM2 — PWM AOZ5038QI Vout → 1V_CPU_CORE; FCCM ← PWR_VCCIN_FCCM_R

Switching Regulator

Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]



a b c d e f g h i

1 2 3 4 5 6 7 8 9 10

11 12 13 14 15 16 17 18 19

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File: Power Sequence

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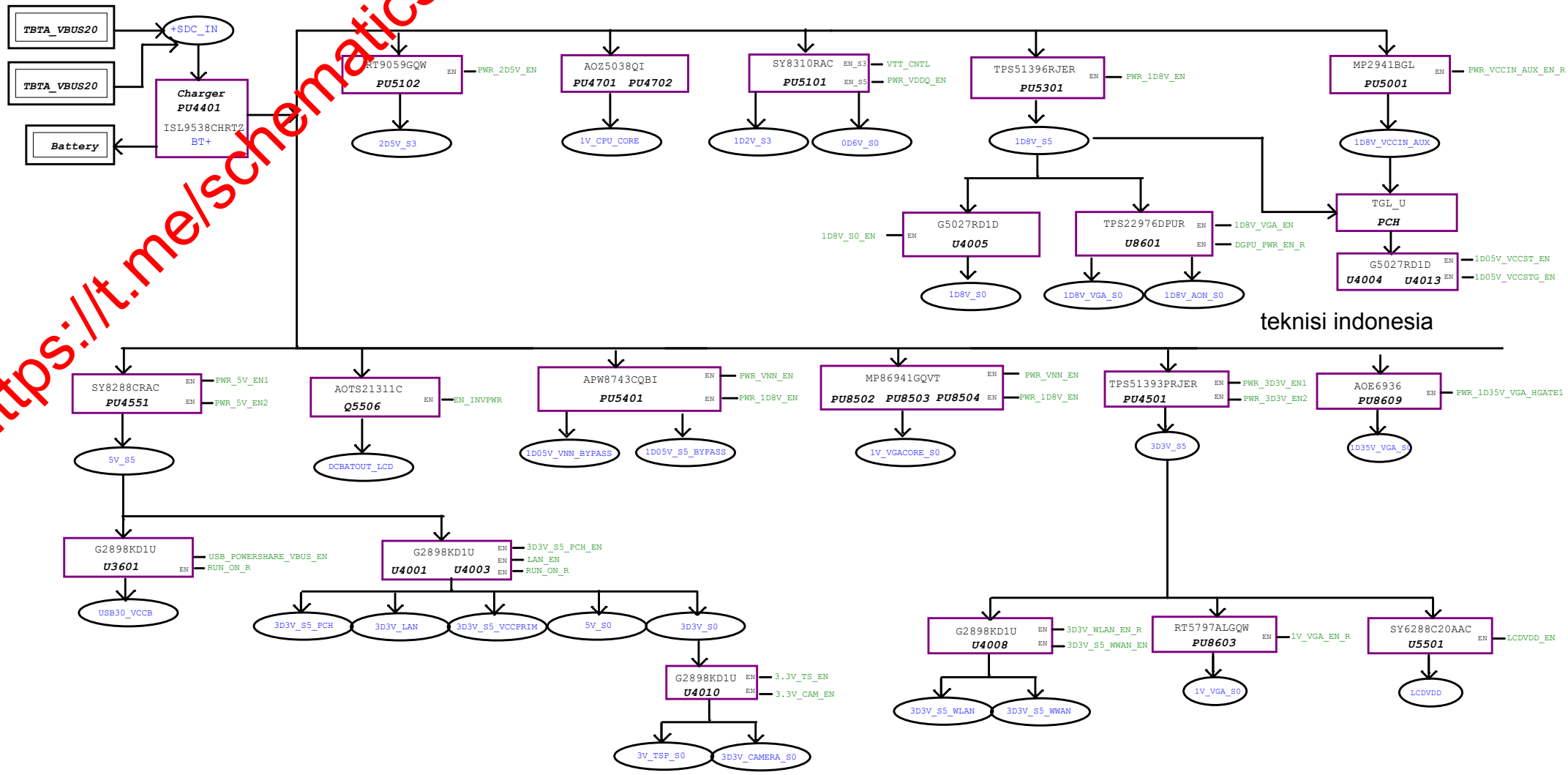

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Title: Power Block Diagram

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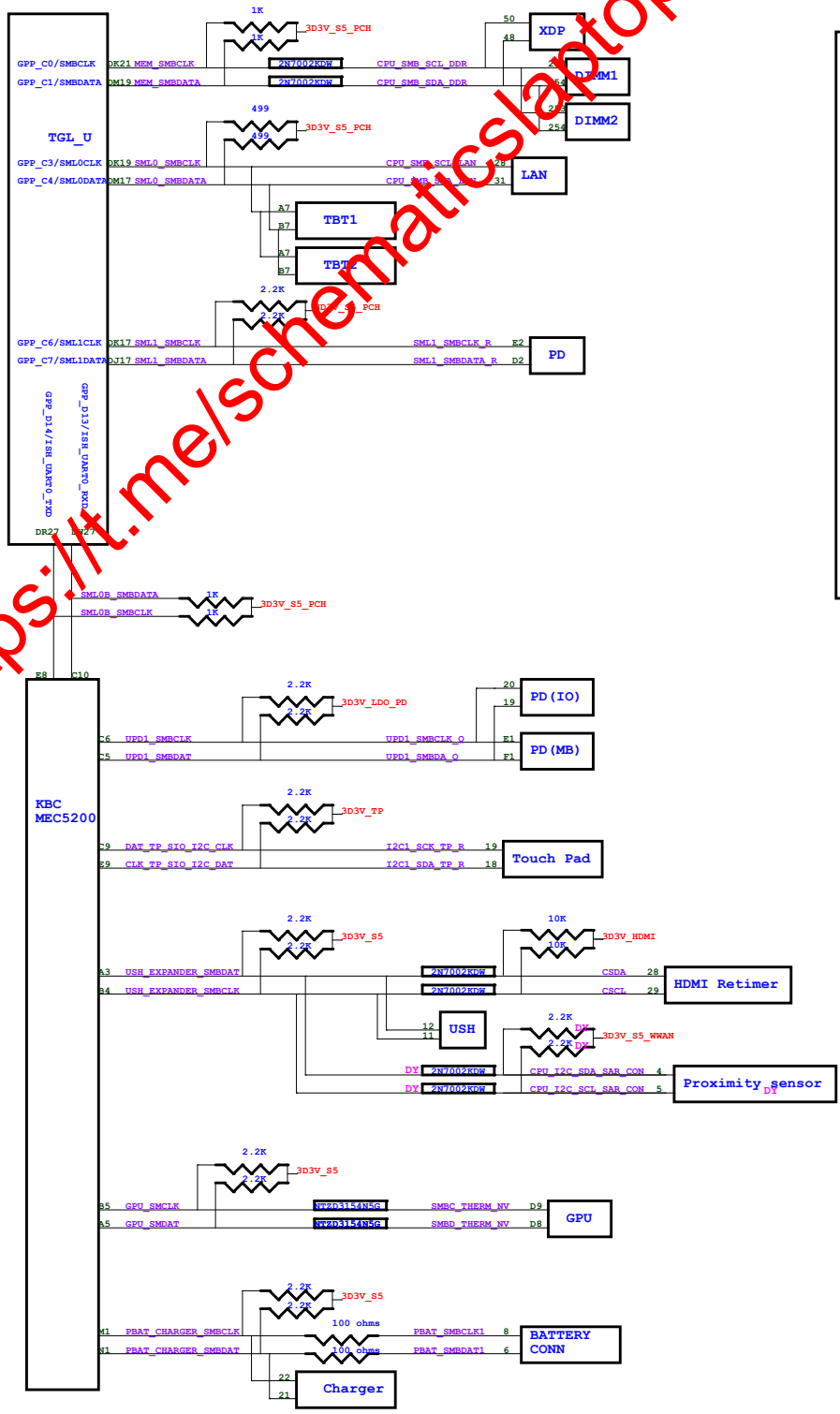
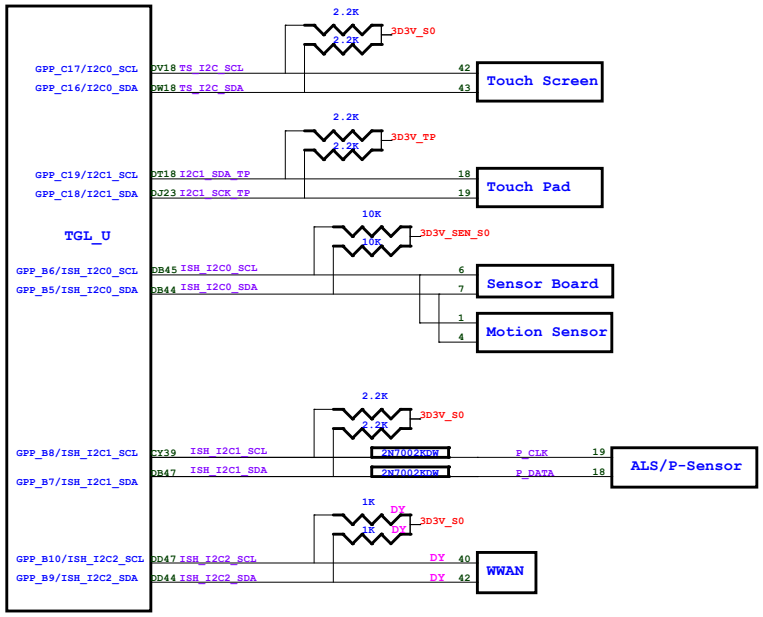
SMbus Block Diagram



I2C Block Diagram



LAN DATASHEET

Pin Name	Pin #	Type	Op Mode	Name and Function
SMB_CLK	29	O/d	Bi-dir	SMBus clock. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in S0 mode).
SMB_DATA	31	O/d	Bi-dir	SMBus data. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in S0 mode).

Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship

Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength (Refer EDS)
Upto 400 pF	2.2KΩ	100Ω
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength
Upto 100pF	2.7KΩ	100Ω
Upto 200pF	1.5KΩ	
Upto 300pF	1KΩ	
Upto 400 pF	680Ω	
Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength
Upto 50pF	2.2KΩ	100Ω
Upto 100pF	1.2KΩ	
Upto 200pF	560Ω	
Upto 300pF	390Ω	
Upto 400 pF	270Ω	67Ω

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Title: SMBUS/I2C BLOCK DIAGRAM

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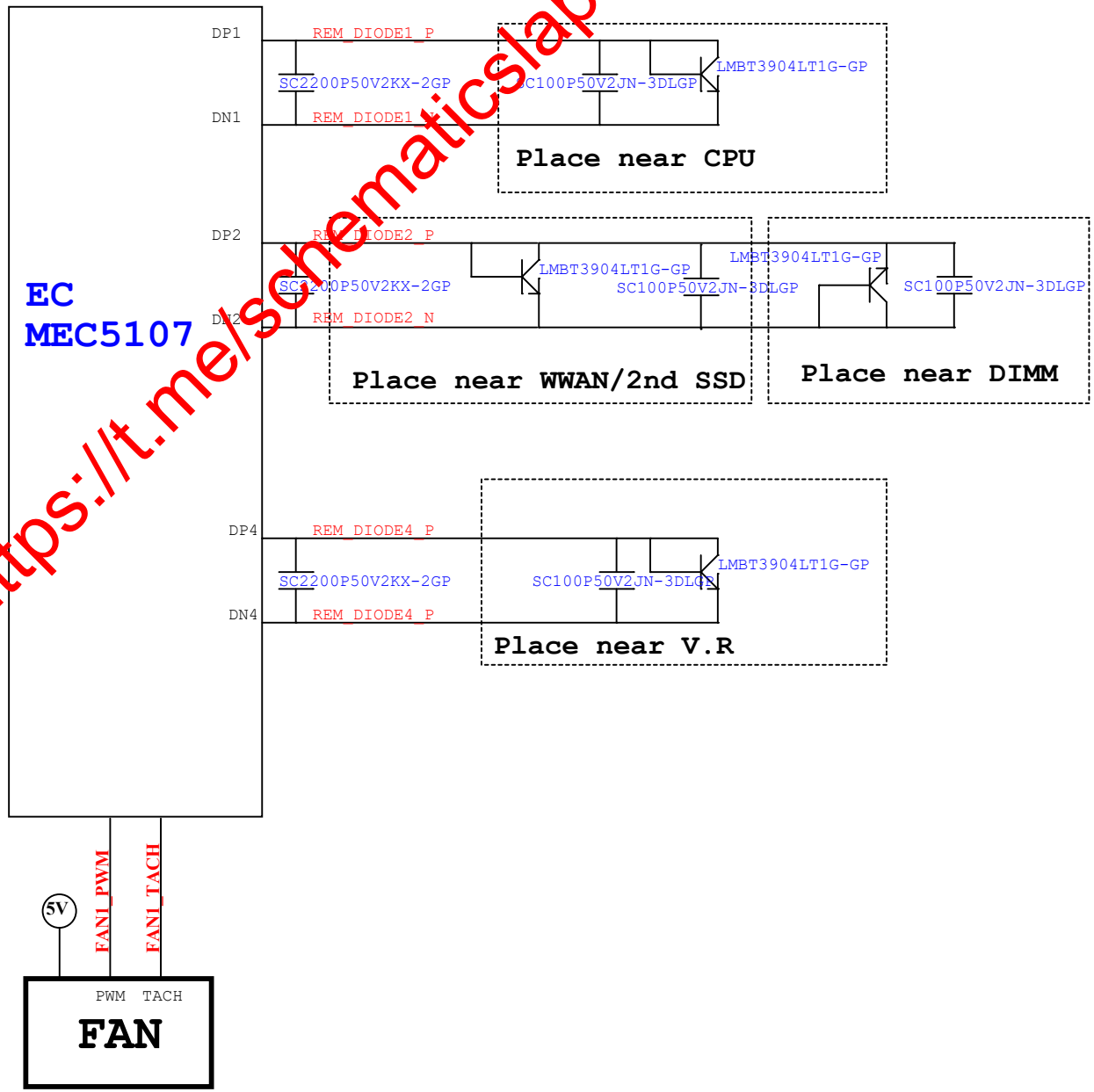
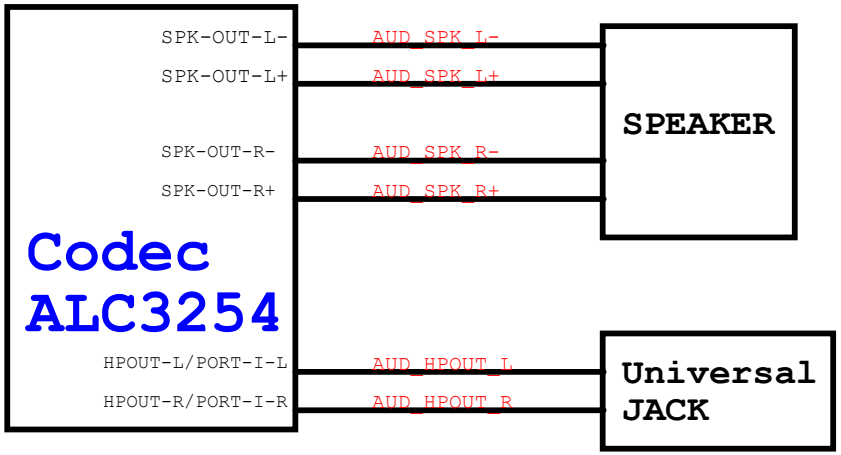
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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Title

CLK Block

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