MS-7B38 Ver:1.0

CPU:
AMD AM4

System Chipset:
Promontory A320
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

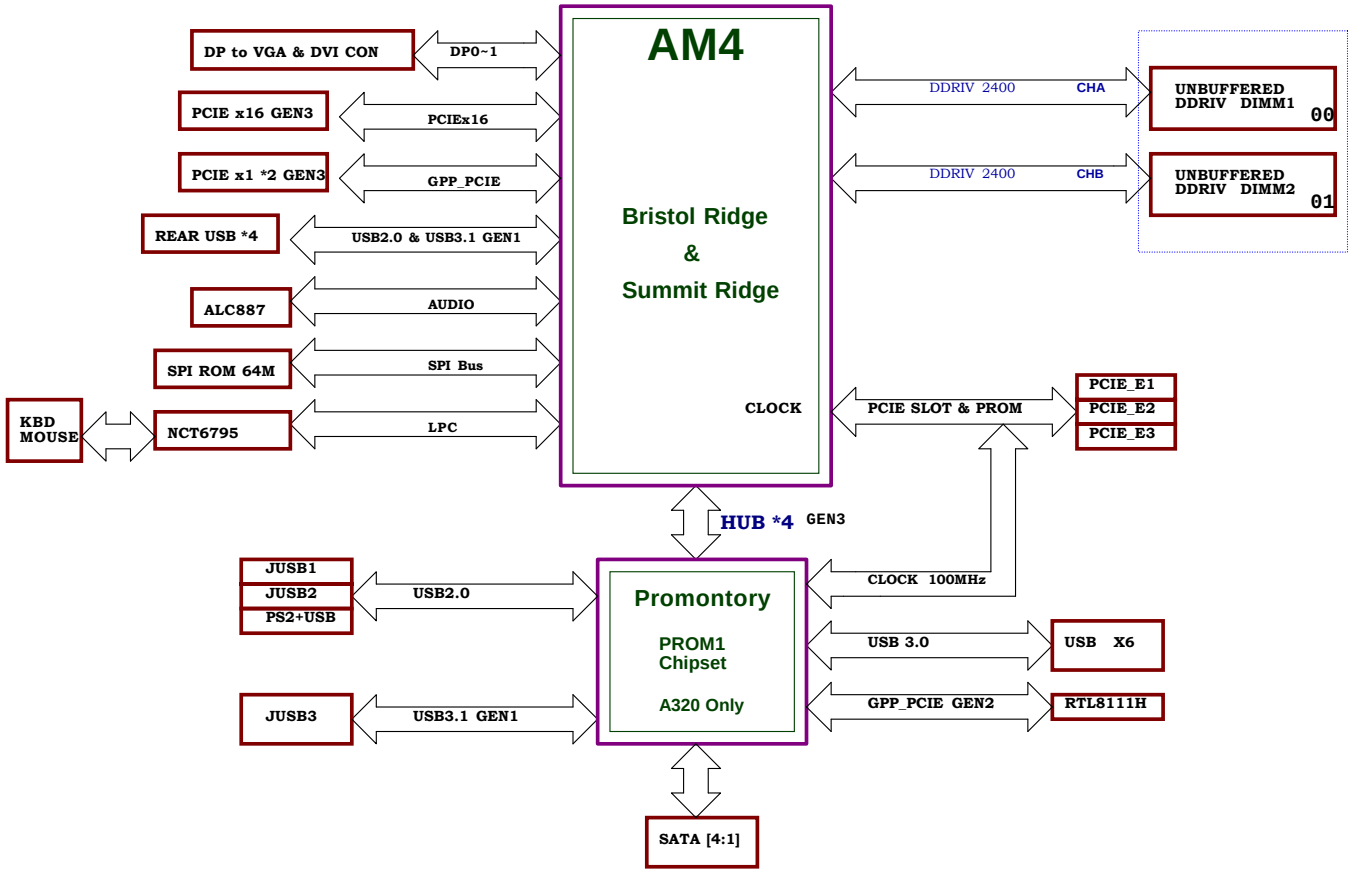
VRM
RT8894 3+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

OCP IC:
UP6273

FUSION BLOCK DIAGRAM



MSI MICRO-START INT'L CO.,LTD.

Title: Block Diagram		
Size: Custom	Document Number: MS-7B38	Rev: 1.0
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AMD AM4

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22 LAN-RTL8111H	
23 / 24 Audio ALC887	
25 USB Rear PS2+USB2.0	
26 USB Rear LAN+USB3.1 GEN1	
27 USB Front Side	
28 SATA Connector	
29 DVI Connector	
30 DP to VGA ITE6516	
31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTT-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: COVER SHEET

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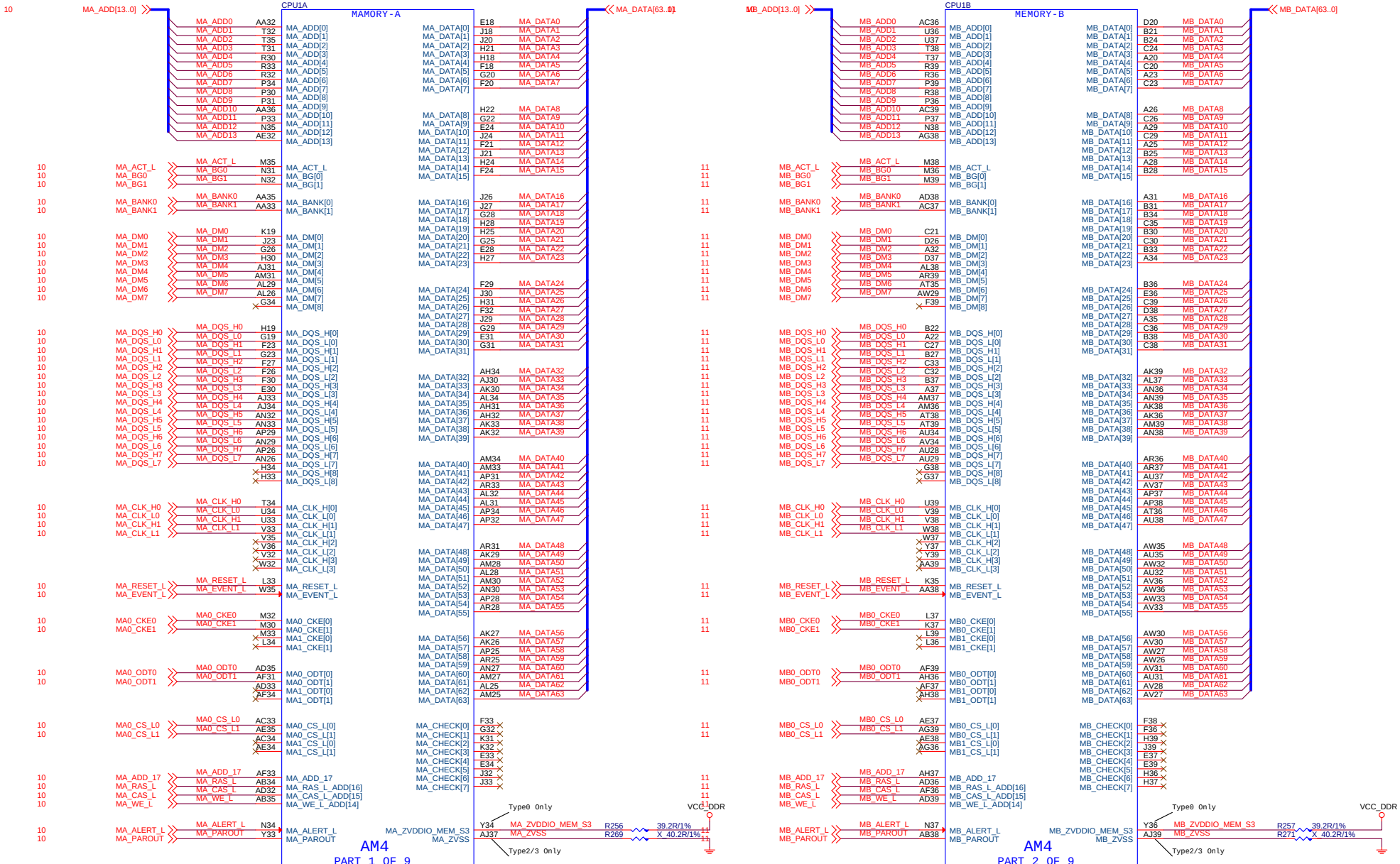

MSI Link to the Future MICRO-START INTL CO.,LTD.

Title	AM4 DDR4 I/F		
Size: Custom	Document Number: MS-7B38		Rev: 1.0
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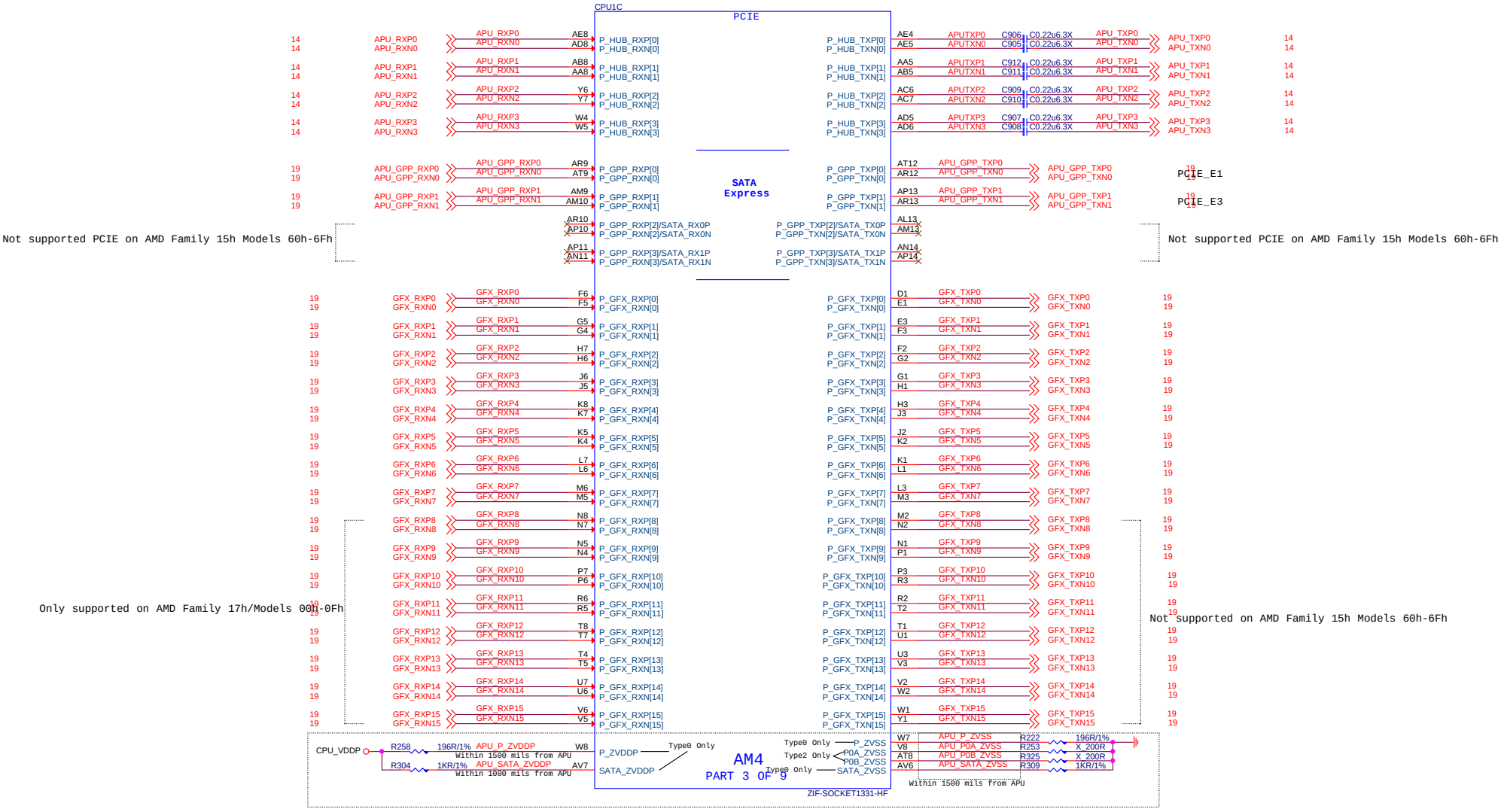
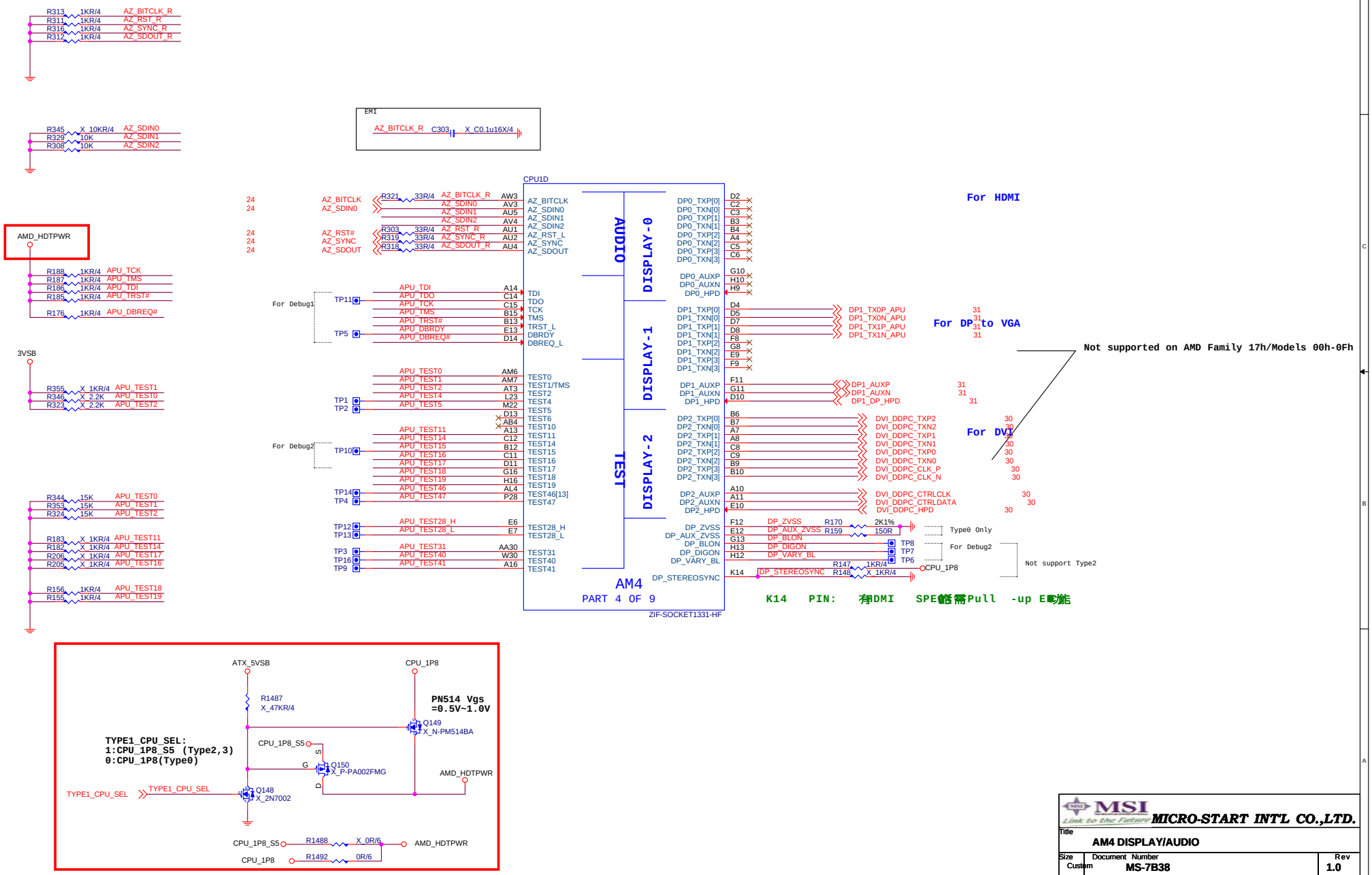
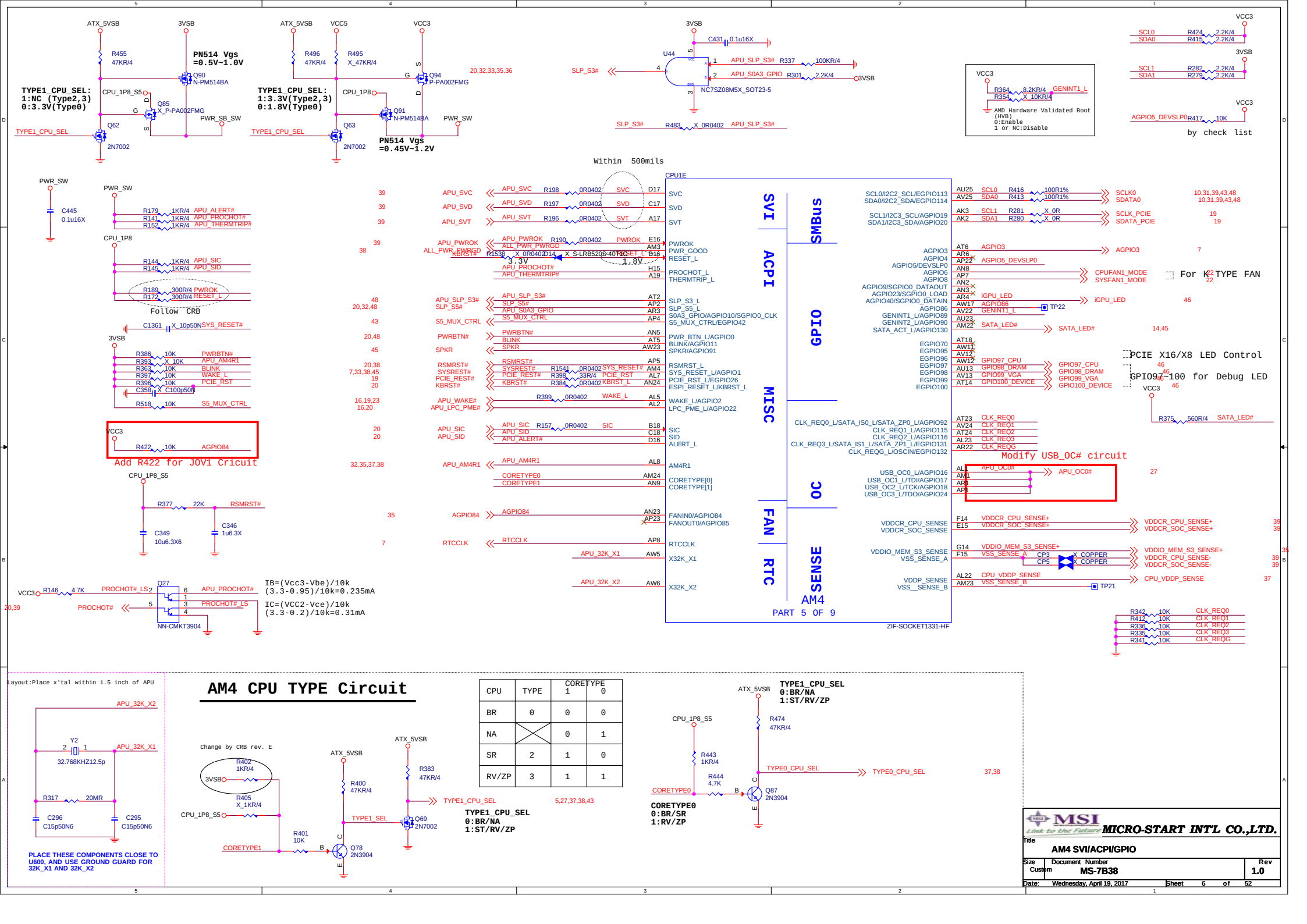


MSI MICRO-START INT'L CO.,LTD.		
Title: AM4 PCIE/SATAE		
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 4 of 52	



MICRO-START INTL CO.,LTD.

Title	AM4 DISPLAY/AUDIO		
Size: Custom	Document Number: MS-7B38		Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 5 of 52		



CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

MICRO-START INTL CO.,LTD.

Title: AM4 SVI/ACPI/GPIO

Size: Custom | Document Number: MS-7B38 | Rev: 1.0

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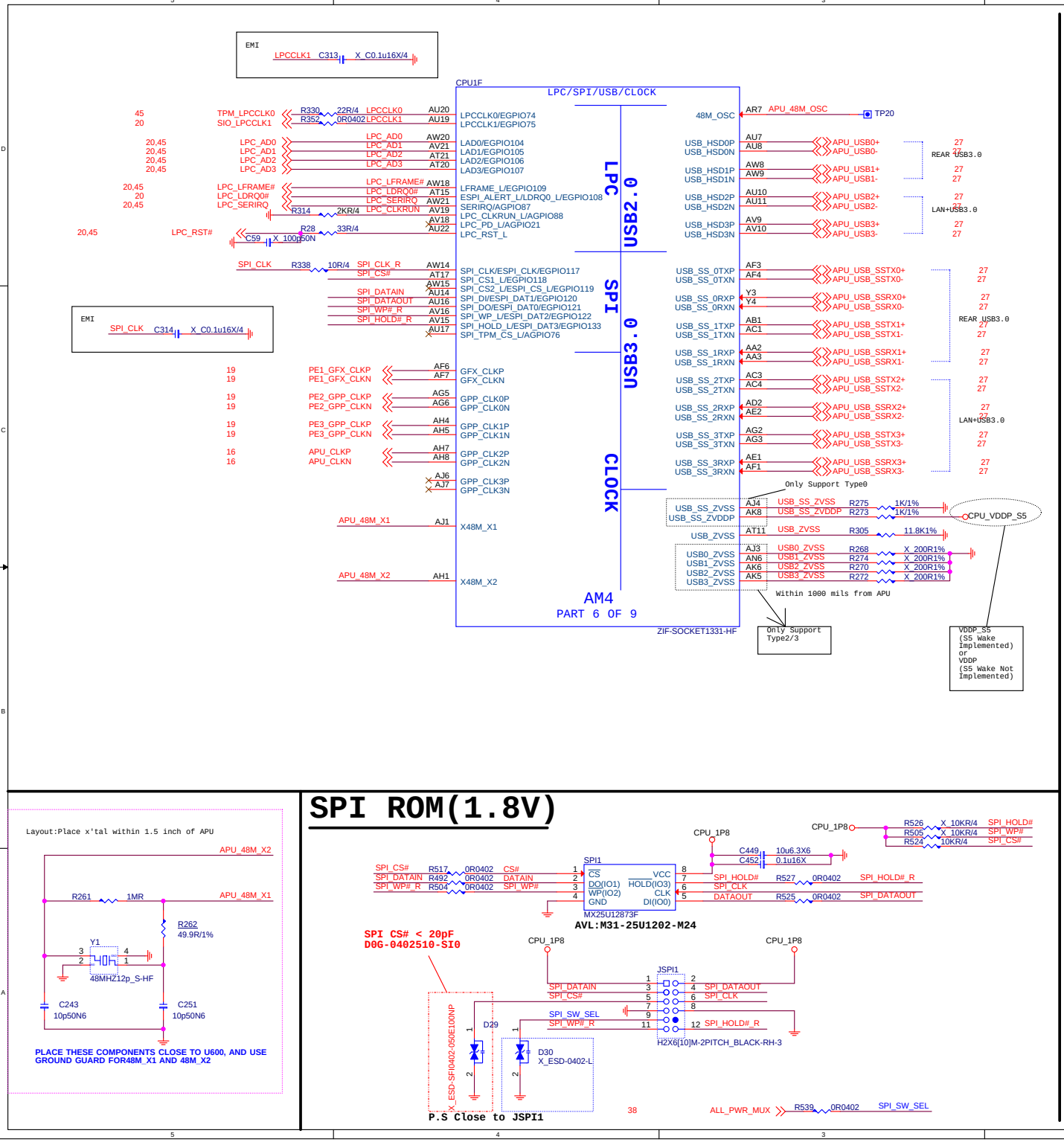
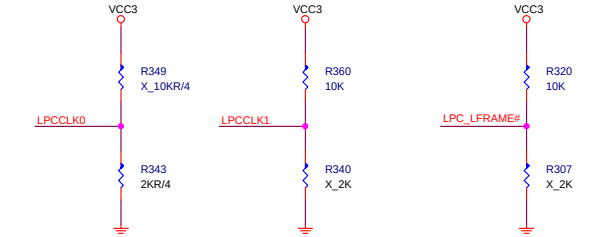
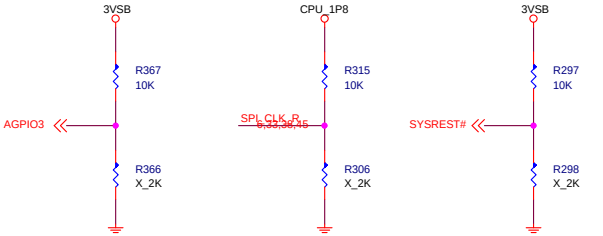


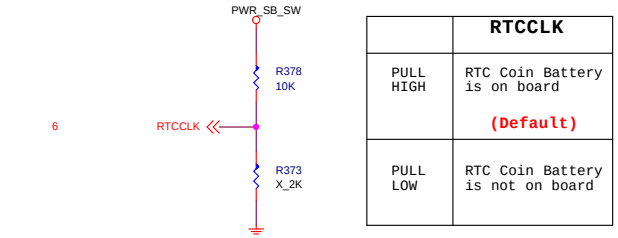
Strapping Options



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board

SPI ROM(1.8V)

Layout:Place x'tal within 1.5 inch of APU	
Title	AM4 LPC/SPI/USB/CLK/STRAP
Size: Custom	Document Number: MS-7B38
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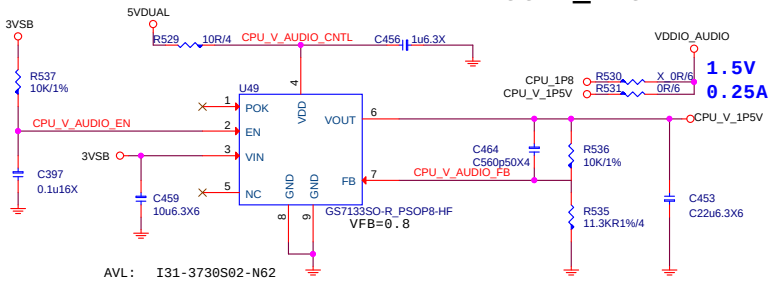
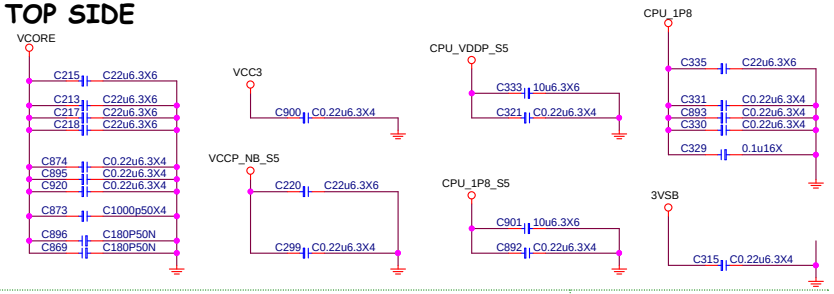
MSI Link to the Future MICRO-START INTL CO.,LTD.

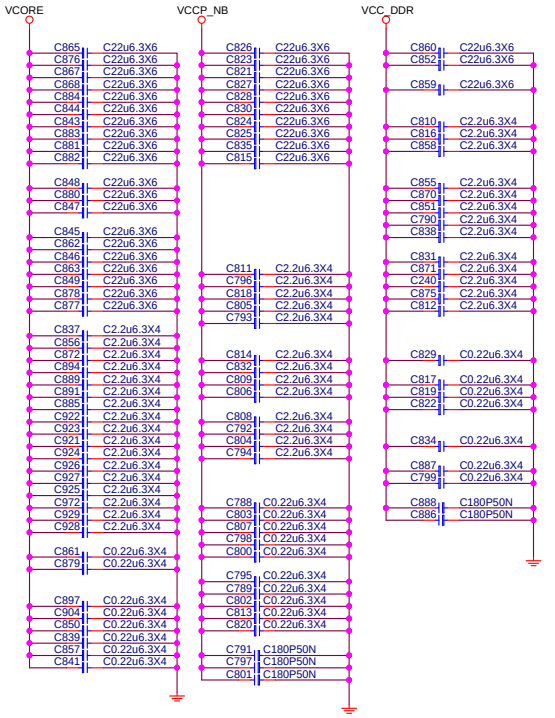
VDDIO_AUDIO Circuit



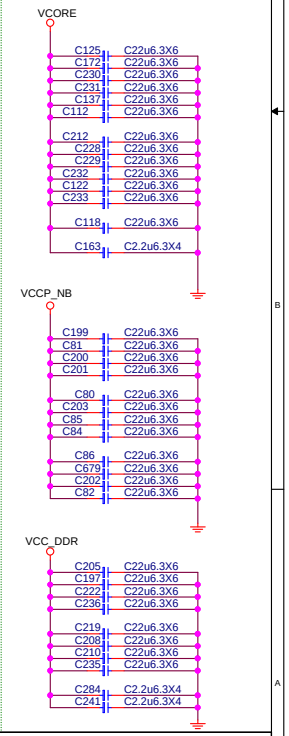
TOP SIDE

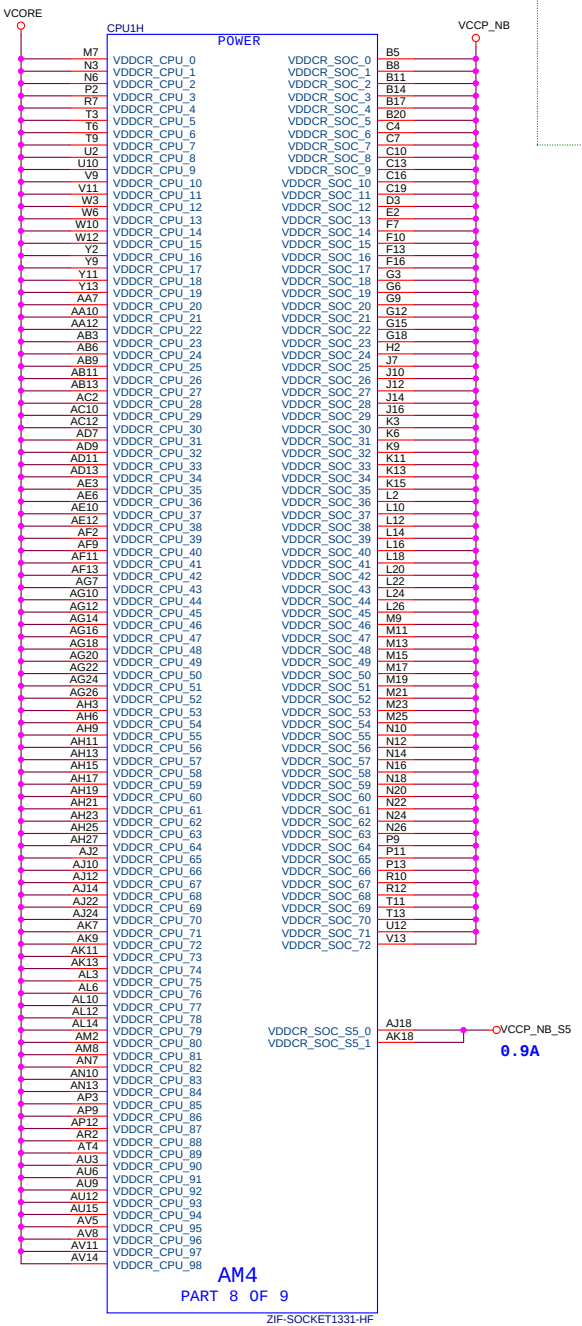


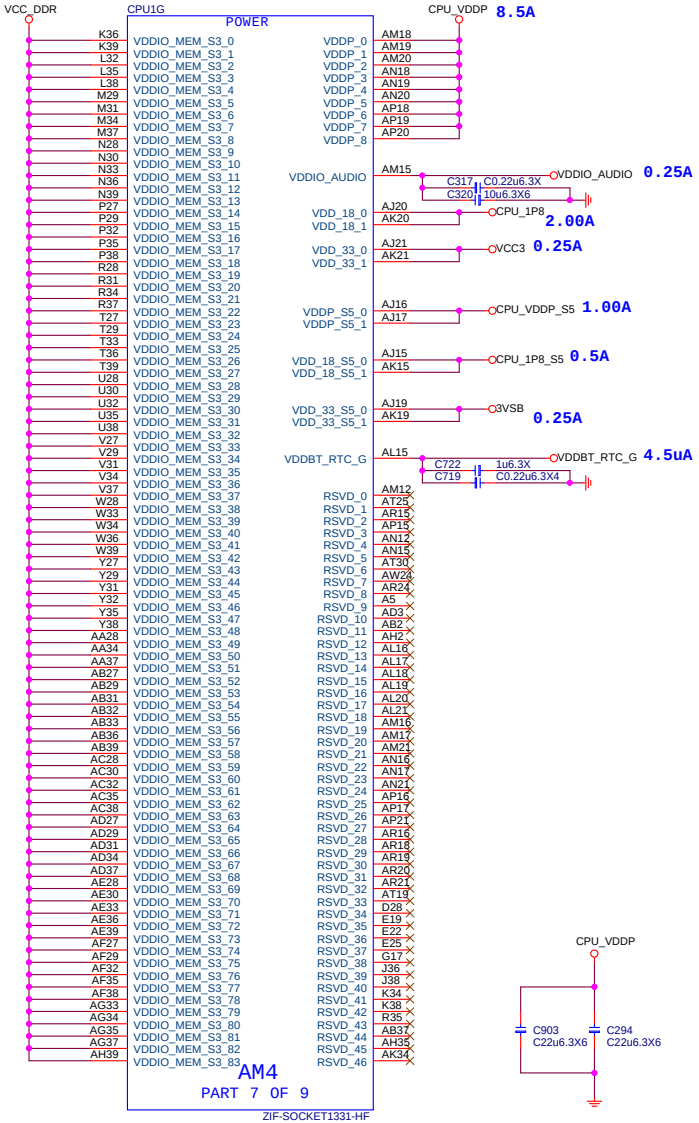
BOTTOM SIDE



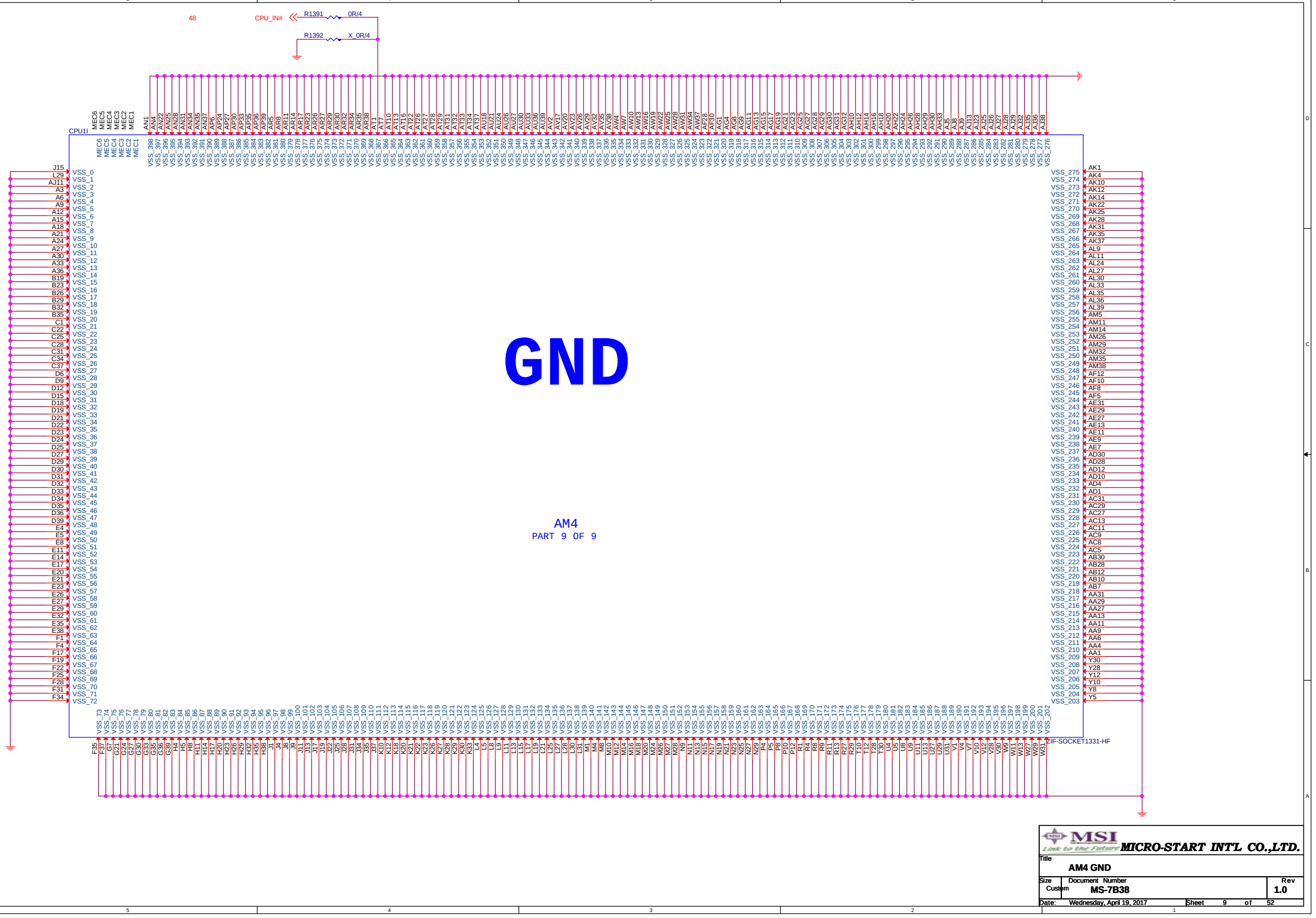
TOP CAVITY





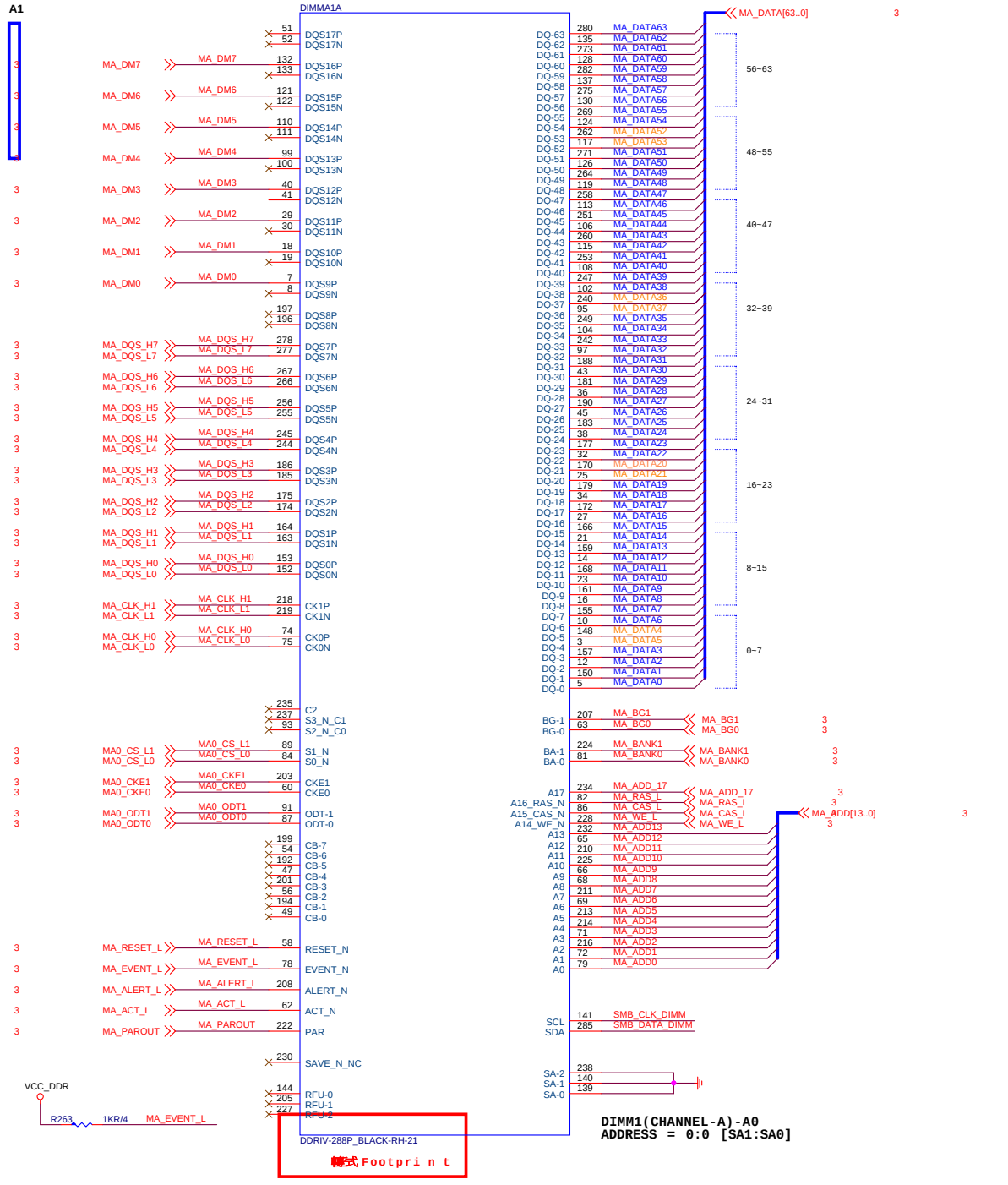


MSI Link to the Future	MICRO-START INTL CO.,LTD.		
Title: AM4 Power/RTC Power			
Size: Custom	Document Number: MS-7B38	Rev: 1.0	
Date: Wednesday, April 19, 2017	Sheet 8 of 52		



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	AM4 GND	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 9 of 52	



Title	DDR4 DIMM CH-A
Size	Custom
Document Number	MS-7B38
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Date:	Wednesday, April 19, 2017
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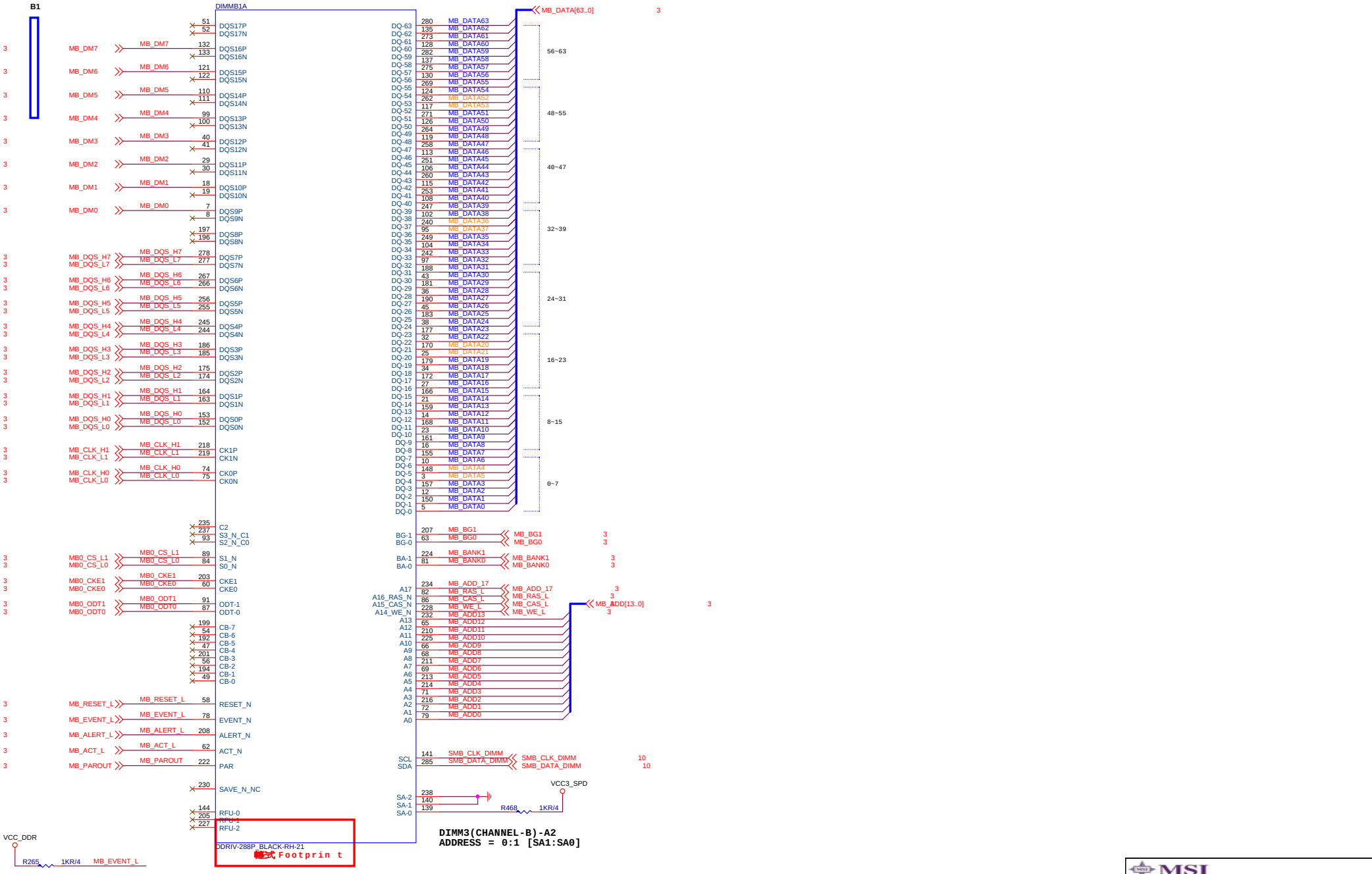
MICRO-START INTL CO.,LTD.



Title	DDR4 DIMM CH-B
Size	Custom
Document Number	MS-7B38
Rev	1.0
Date:	Wednesday, April 19, 2017
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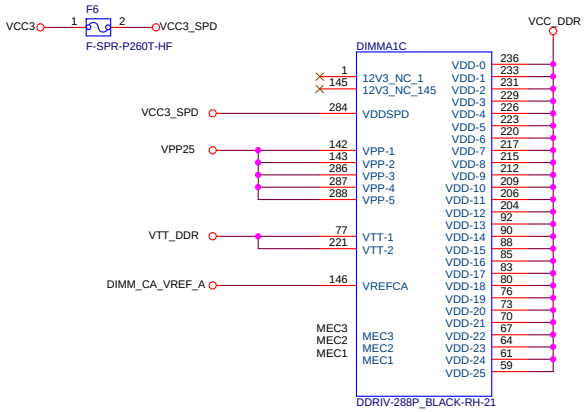
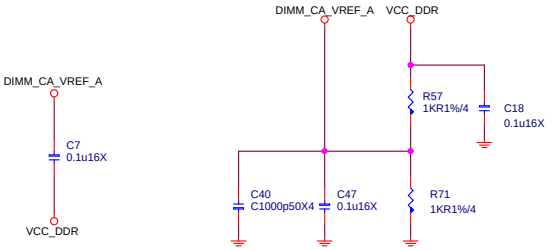
MICRO-START INT'L CO.,LTD.

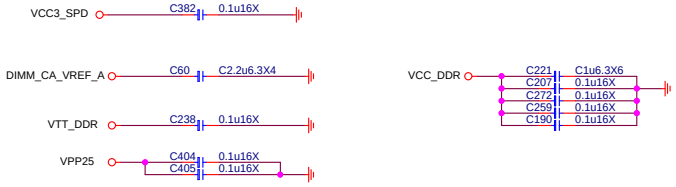


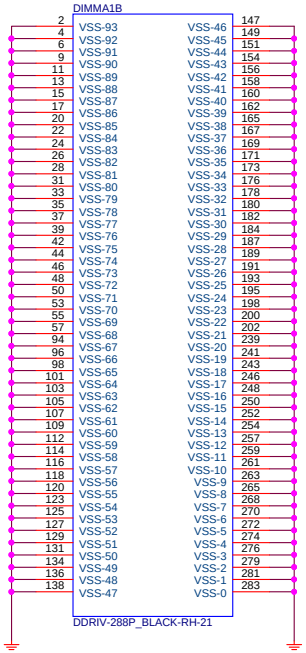
DIMM SLOT PN BY SPEC

DDR VREF

(place resistors close to DIMMs)





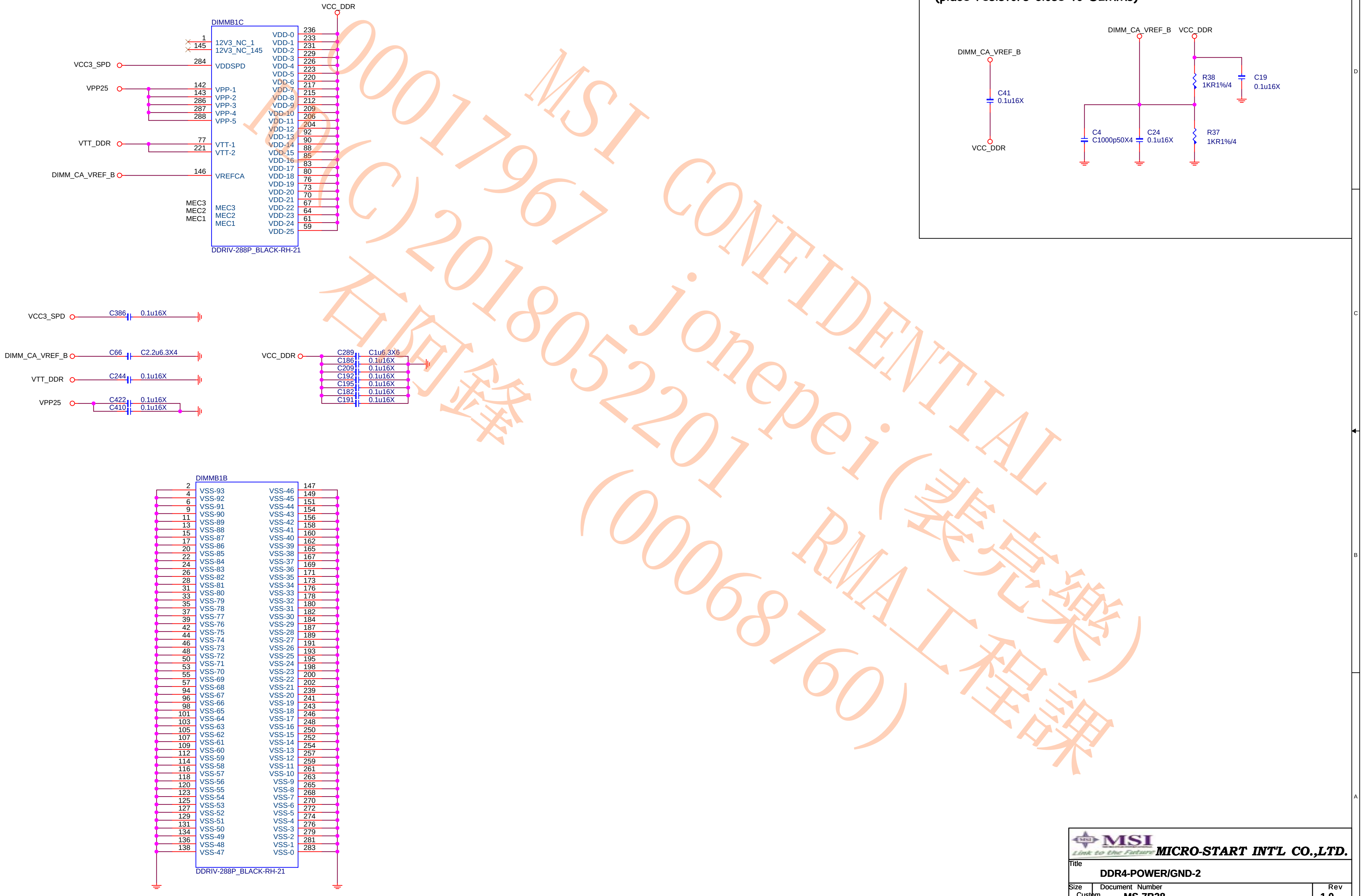


MSI Link to the Future **MICRO-START INTL CO.,LTD.**

Title	DDR4-POWER/GND-1	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 12 of 52	

DDR VREF

(place resistors close to DIMMs)

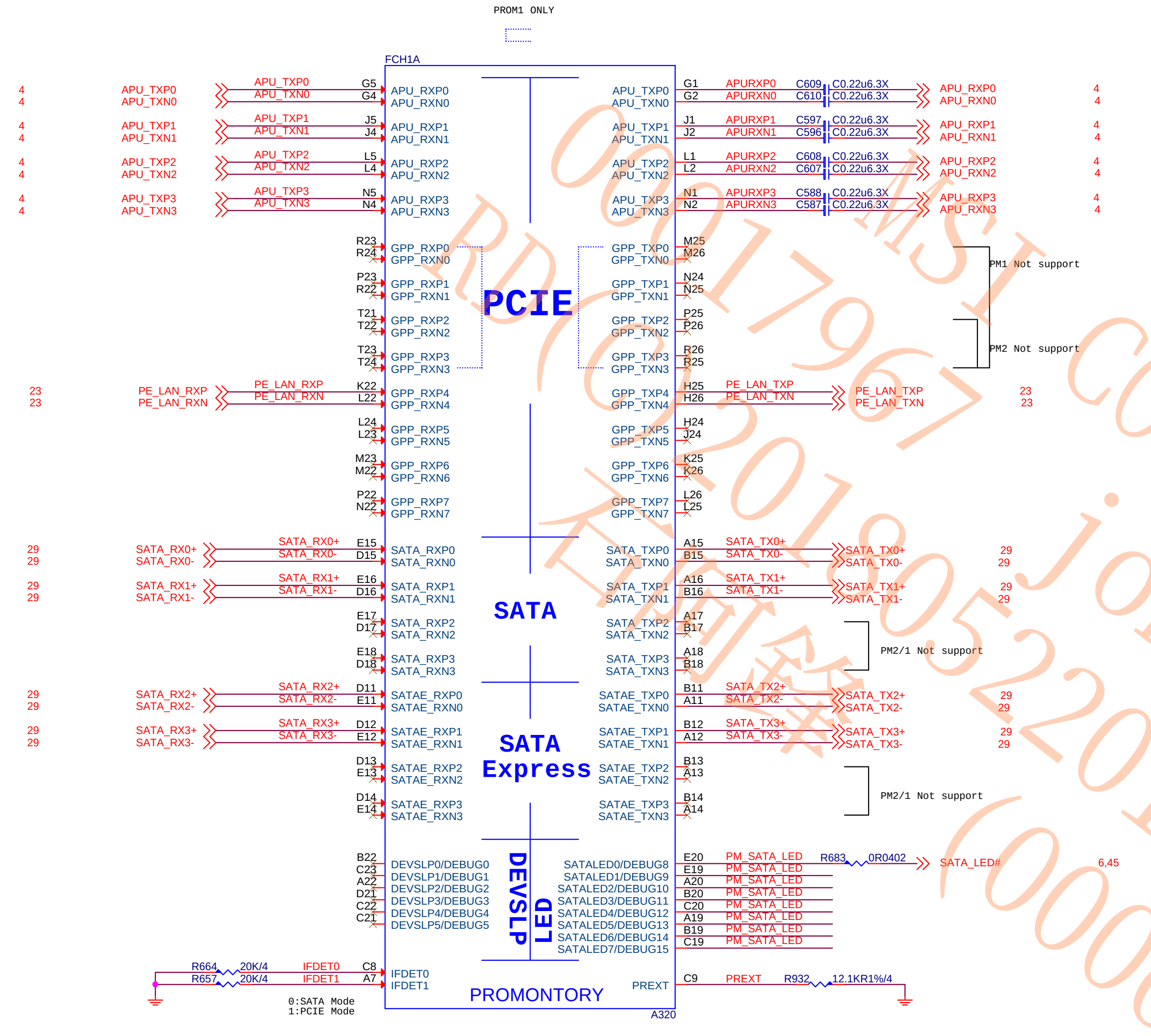


MSI MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-2

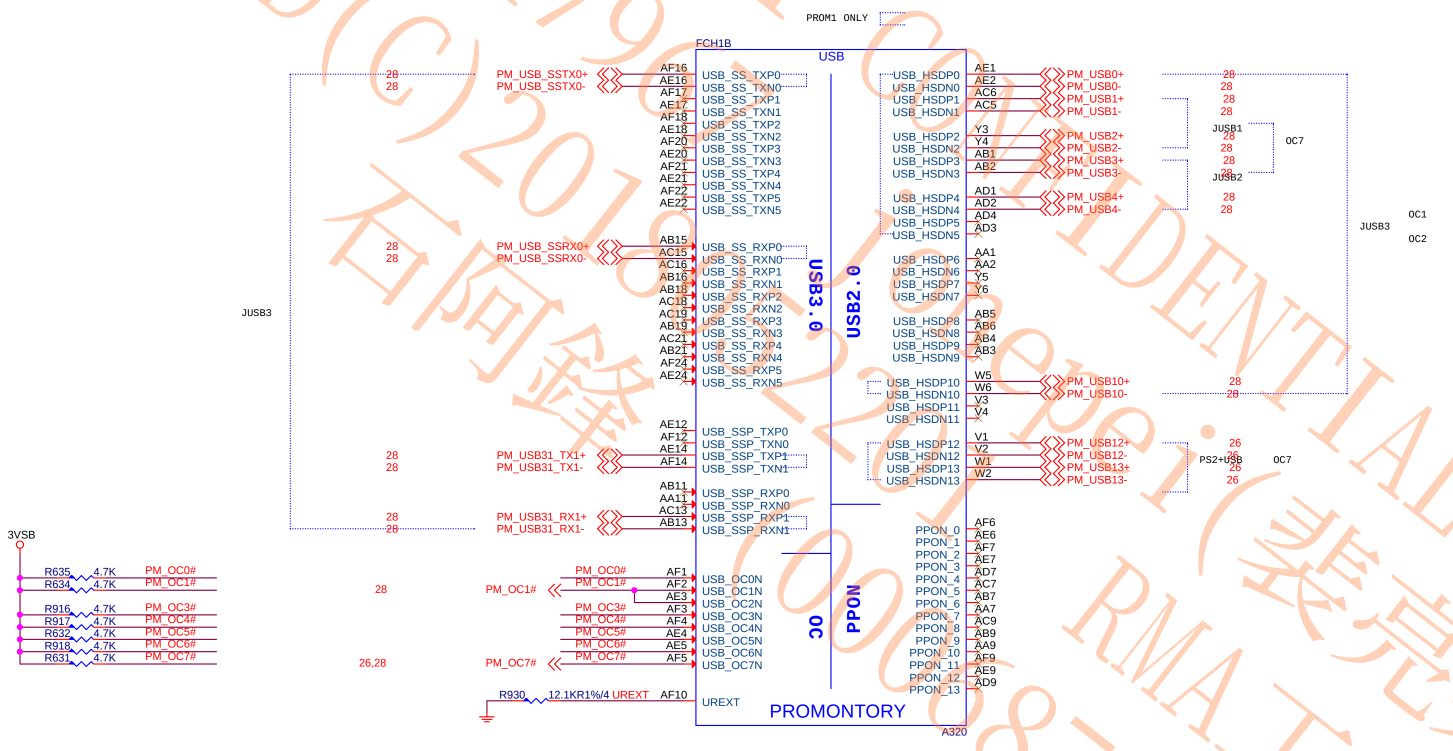
Size	Document Number	Rev
Custom	MS-7B38	1.0

Date: Wednesday, April 19, 2017 Sheet 13 of 52



MICRO-START INT'L CO.,LTD.

Title	Promontory-PCIE/SATA/SATAE	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 14 of 52	



MICRO-START INT'L CO.,LTD.

Title: **Promontory-USB/OC**

Size	Document Number	Rev
Custom	MS-7B38	1.0

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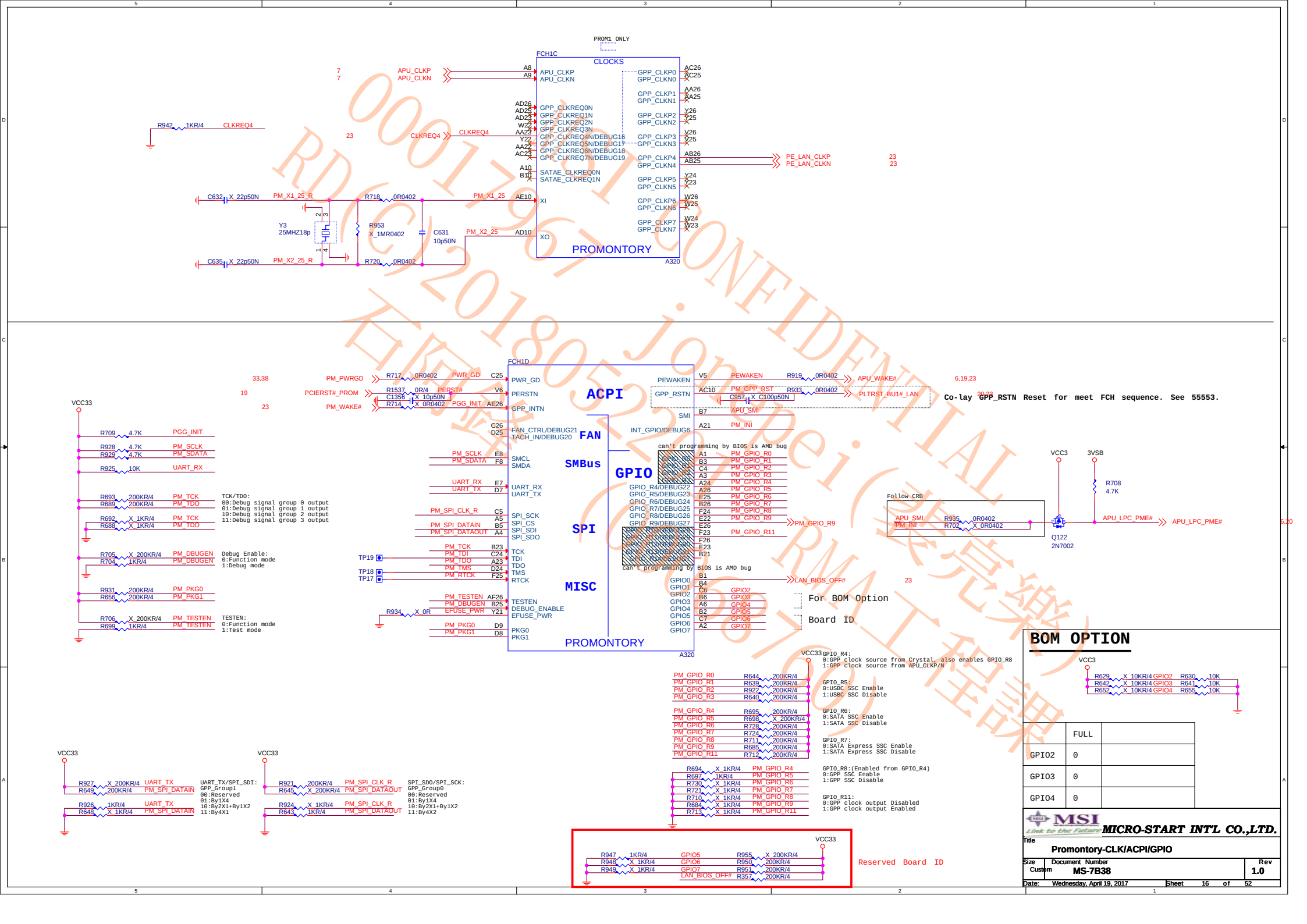
PROM1 ONLY
FCH1C
CLOCKS
APU_CLKP
APU_CLKN
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEBUG16
GPP_CLKREQ5N/DEBUG17
GPP_CLKREQ6N/DEBUG18
GPP_CLKREQ7N/DEBUG19
SATAE_CLKREQ0N
SATAE_CLKREQ1N
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
PE_LAN_CLKP
PE_LAN_CLKN
R942 1KR/4 CLKREQ4
C632 X_22p50N PM_X1_25_R
R718 0R0402 PM_X1_25
Y3 25MHZ18p
R953 X_1MR0402
C631 10p50N
PM_X2_25
C635 X_22p50N PM_X2_25_R
R720 0R0402
XI
XO
PROMONTORY
A320
FCH1D
ACPI
FAN
SMBus
GPIO
SPI
MISC
PROMONTORY
A320
PM_PWRGD
PCIERST#_PROM
PM_WAKE#
R717 0R0402 PWR_GD
R1537 0R/4 PERST#
C1356 X_10p50N
R714 X_0R0402 PGG_INIT
PWR_GD
PERSTN
GPP_INTN
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMCL
SMDA
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
TCK
TDI
TDO
TMS
RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PKG0
PKG1
PEWAKEN
GPP_RSTN
SMI
INT_GPIO/DEBUG6
PEWAKEN
R919 0R0402
APU_WAKE#
PM_GPP_RST
R933 0R0402
C957 X_C100p50N
PLTRST_BU1#_LAN
APU_SMI
PM_INI
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
can't programming by BIOS is AMD bug
GPIO_R0/DEBUG22
GPIO_R1/DEBUG23
GPIO_R2/DEBUG24
GPIO_R3/DEBUG25
GPIO_R4/DEBUG22
GPIO_R5/DEBUG23
GPIO_R6/DEBUG24
GPIO_R7/DEBUG25
GPIO_R8/DEBUG26
GPIO_R9/DEBUG27
GPIO_R10/DEBUG28
GPIO_R11/DEBUG29
PM_GPIO_R9
PM_GPIO_R11
LAN_BIOS_OFF#
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
For BOM Option
Board ID
Follow CRB
APU_SMI
PM_INI
R935 0R0402
R702 X_0R0402
Q122
2N7002
R708 4.7K
APU_LPC_PME#
VCC33
3VSB
R709 4.7K PGG_INIT
R928 4.7K PM_SCLK
R929 4.7K PM_SDATA
R925 10K UART_RX
R693 200KR/4 PM_TCK
R689 200KR/4 PM_TDO
R692 X_1KR/4 PM_TCK
R688 X_1KR/4 PM_TDO
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
R705 X_200KR/4 PM_DBGUEN
R704 1KR/4 PM_DBGUEN
Debug Enable:
0:Function mode
1:Debug mode
R931 200KR/4 PM_PKG0
R656 200KR/4 PM_PKG1
R706 X_200KR/4 PM_TESTEN
R699 1KR/4 PM_TESTEN
TESTEN:
0:Function mode
1:Test mode
TP19
TP18
TP17
R934 X_0R
PM_TESTEN
PM_DBGUEN
EFUSE_PWR
PM_PKG0
PM_PKG1
R927 X_200KR/4 UART_TX
R649 200KR/4 PM_SPI_DATAIN
R926 1KR/4 UART_TX
R648 X_1KR/4 PM_SPI_DATAIN
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X1
R921 200KR/4 PM_SPI_CLK_R
R645 X_200KR/4 PM_SPI_DATAOUT
R924 X_1KR/4 PM_SPI_CLK_R
R643 1KR/4 PM_SPI_DATAOUT
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
GPIO_R4:
0:GPP clock source from Crystal, also enables GPIO_R8
1:GPP Clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
R947 1KR/4 GPIO5
R948 X_1KR/4 GPIO6
R949 X_1KR/4 GPIO7
LAN_BIOS_OFF#
R955 X_200KR/4
R950 200KR/4
R951 200KR/4
R357 200KR/4
Reserved Board ID
BOM OPTION
R629 X_10KR/4 GPIO2
R642 X_10KR/4 GPIO3
R652 X_10KR/4 GPIO4
R630 10K
R641 10K
R655 10K
FULL
GPIO2 0
GPIO3 0
GPIO4 0
MICRO-START INTL CO.,LTD.
Title
Promontory-CLK/ACPI/GPIO
Size Custom
Document Number MS-7B38
Rev 1.0
Date: Wednesday, April 19, 2017
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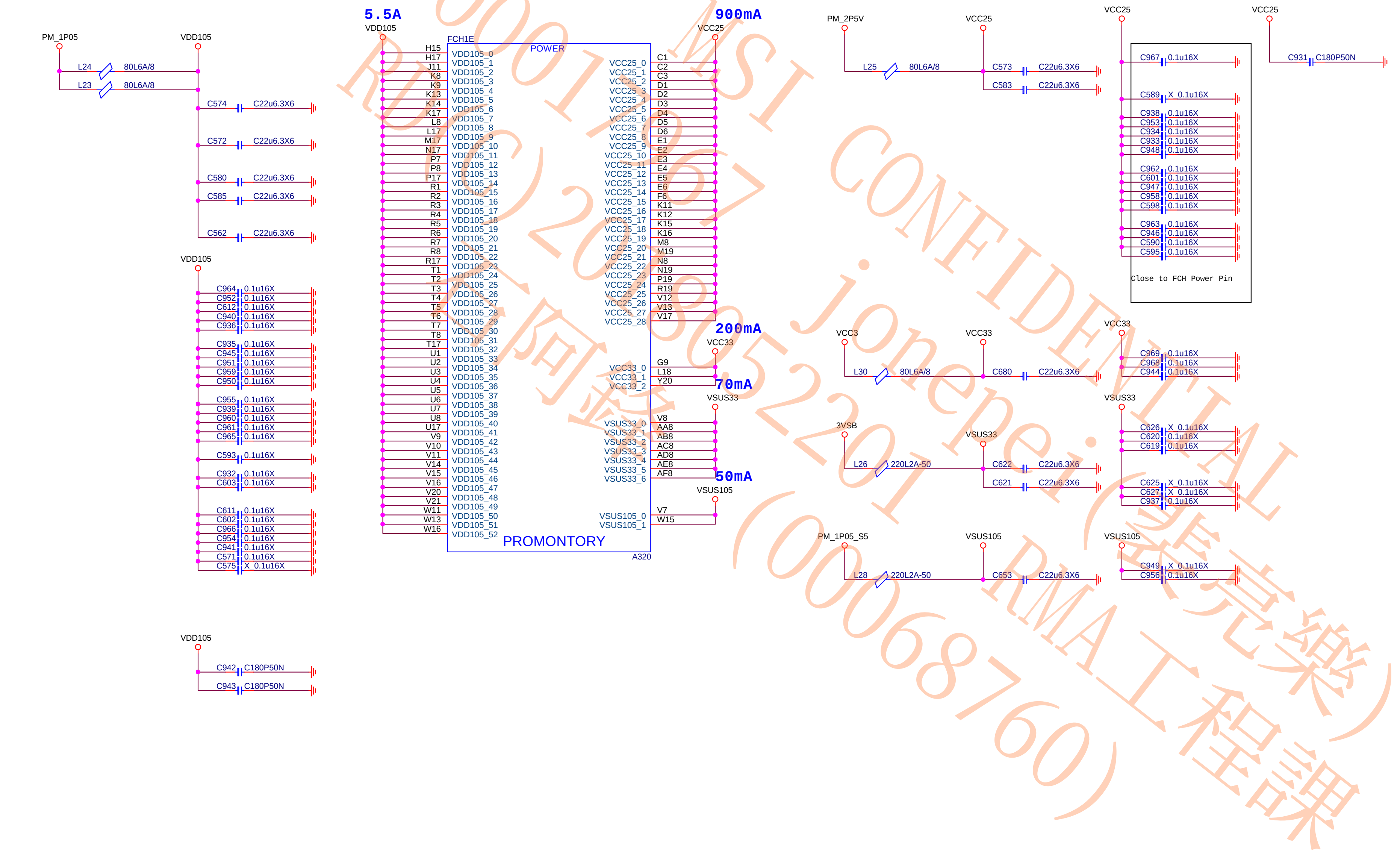
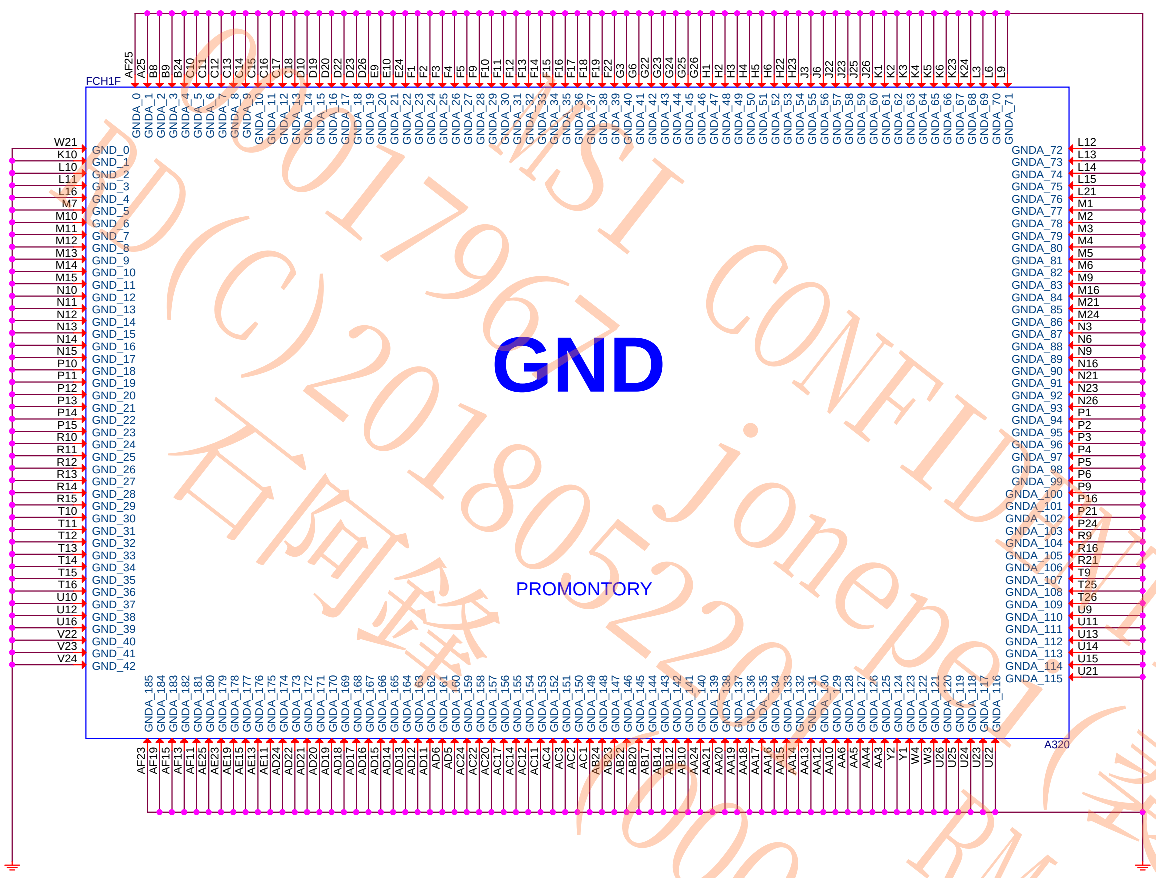


MSI MICRO-START INT'L CO.,LTD.

Title	Promontory-Power	
Size Custom	Document Number MS-7B38	Rev 1.0
Date: Wednesday, April 19, 2017	Sheet 17 of 52	



MSI MICRO-START INT'L CO.,LTD.

Title: **Promontory-GND**

Size	Document Number	Rev
Custom	MS-7B38	1.0

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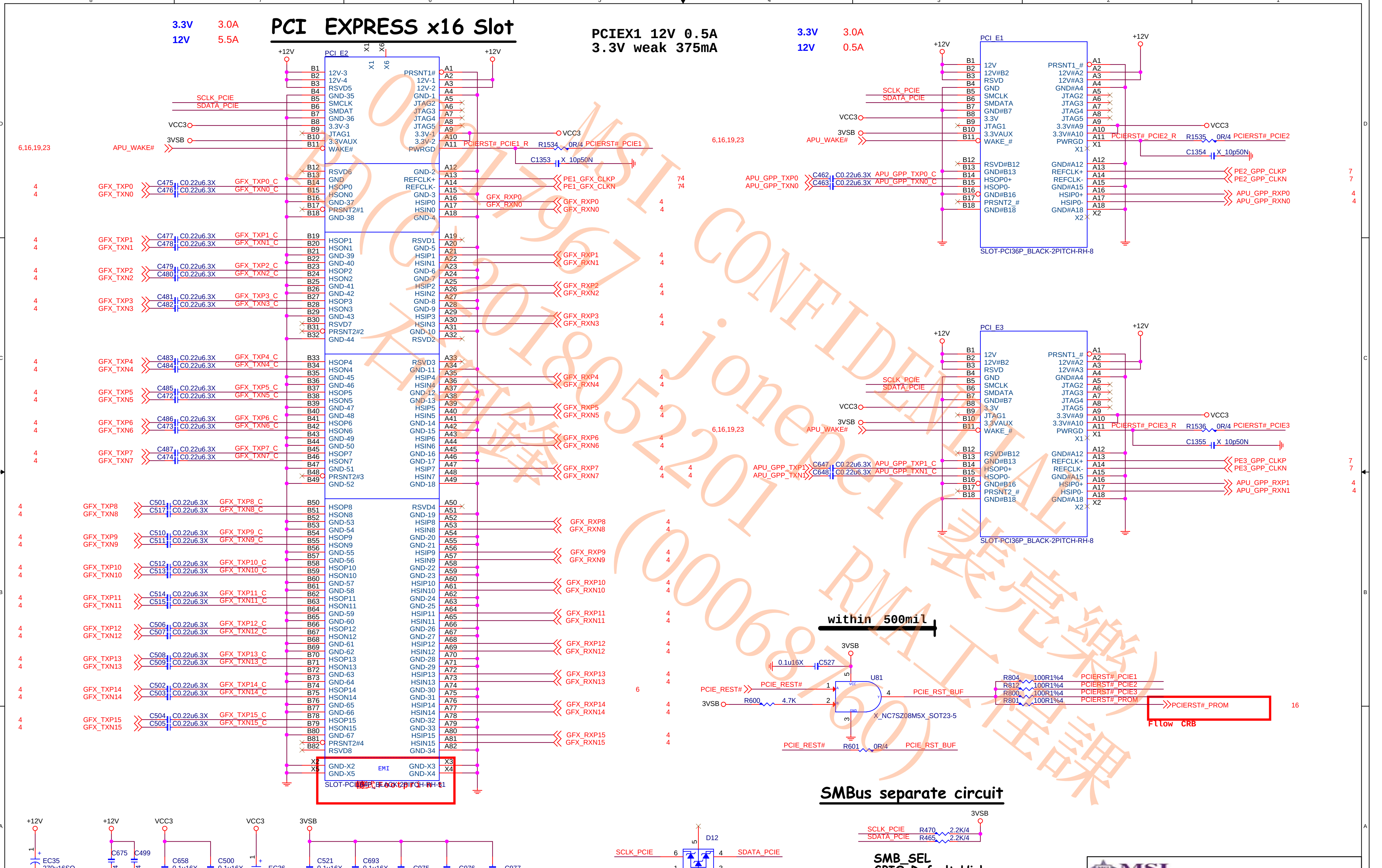

MSI	MICRO-START INT'L CO.,LTD.
Title	PCIE X16(X1*2) SLOT
Size: Custom	Document Number: MS-7B38
Rev	1.0
Date:	Wednesday, April 19, 2017
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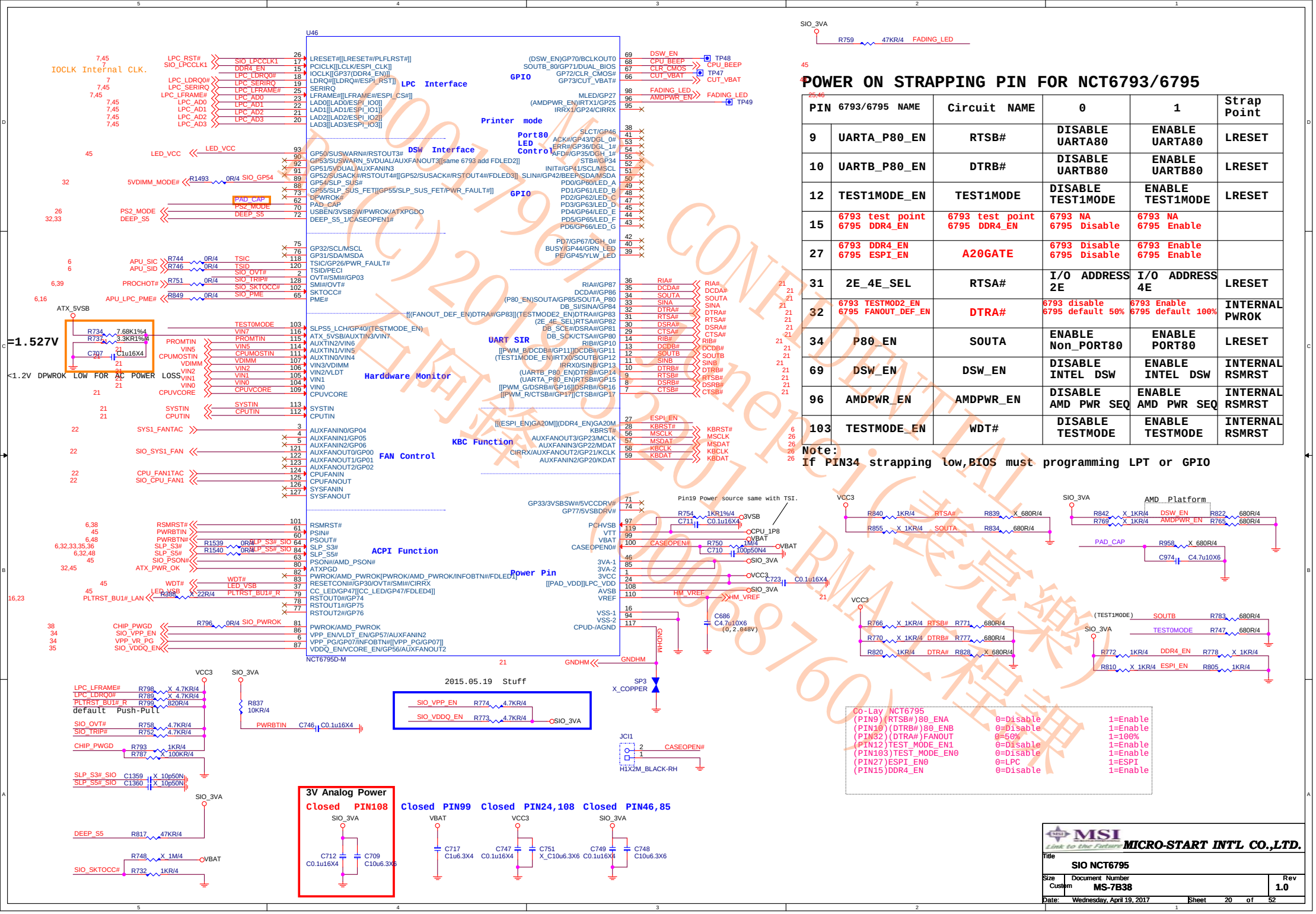


POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

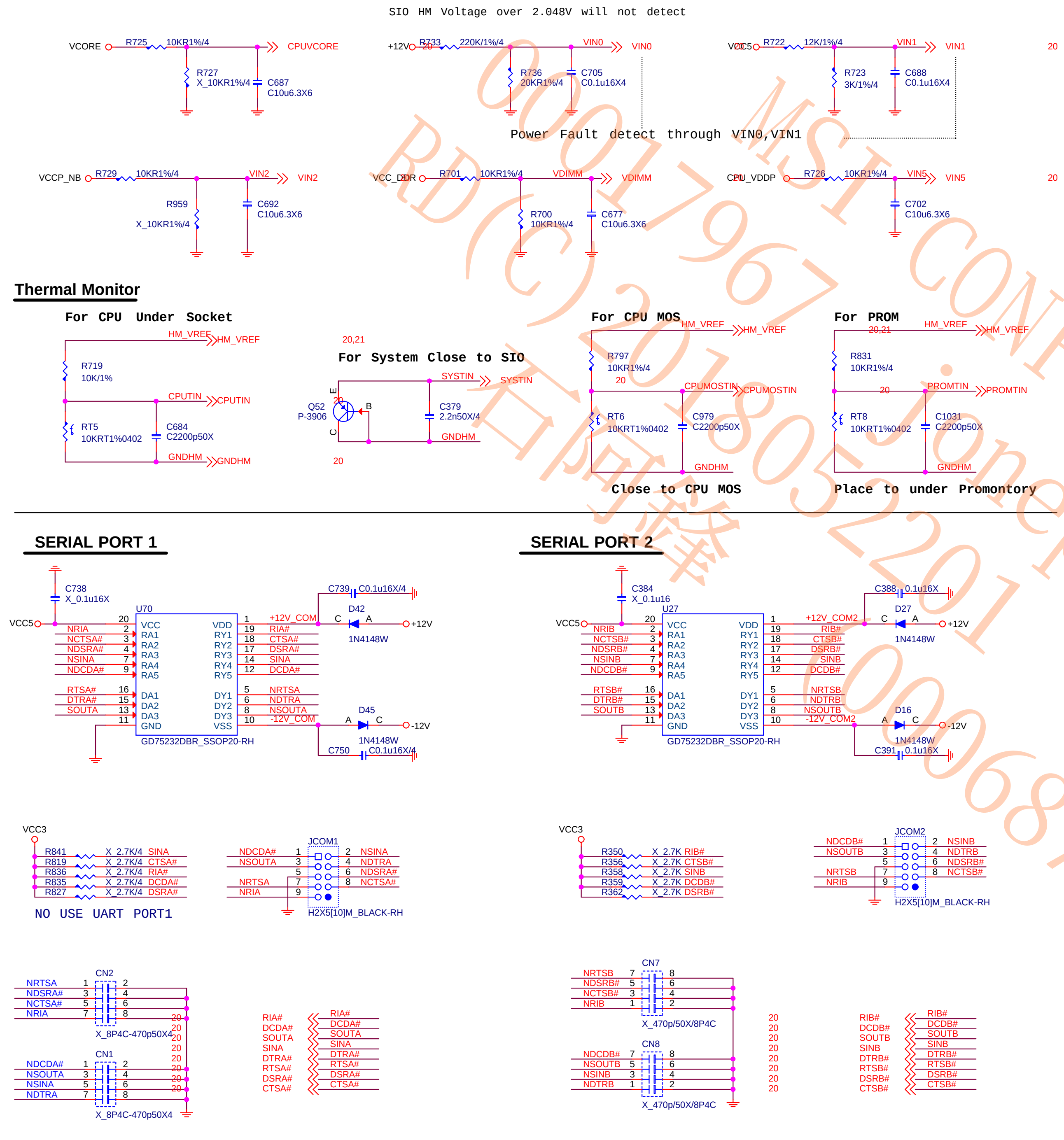
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Co-Lay NCT6795
(PIN9)(RTSB#)80_ENA 0=Disable 1=Enable
(PIN10)(DTRB#)80_ENB 0=Disable 1=Enable
(PIN32)(DTRA#)FANOUT 0=50% 1=100%
(PIN12)TEST_MODE_EN1 0=Disable 1=Enable
(PIN103)TEST_MODE_EN0 0=Disable 1=Enable
(PIN27)ESPI_EN0 0=LPC 1=ESPI
(PIN15)DDR4_EN 0=Disable 1=Enable

MICRO-START INTL CO.,LTD.

Title	SIO NCT6795	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 20 of 52	

HW Monitor - Voltage



MSI MICRO-START INT'L CO.,LTD.		
Title	SIO NCT6795	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
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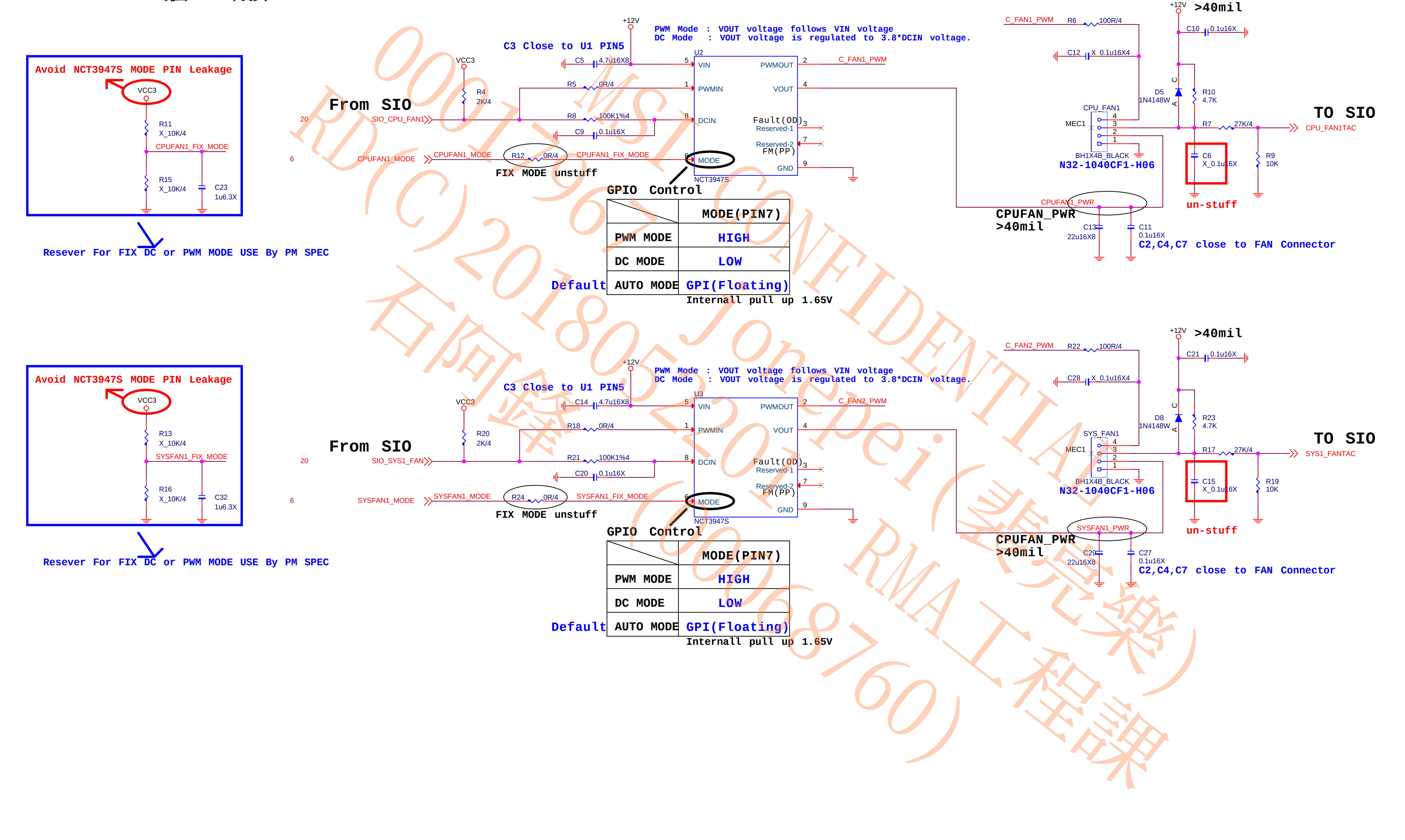
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO項由B0 切換 PW M/DC M O D E



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MSI Link to the Future MICRO-START INT'L CO.,LTD.
Title: CPU FAN Control
Size: Custom | Document Number: MS-7B38 | Rev: 1.0
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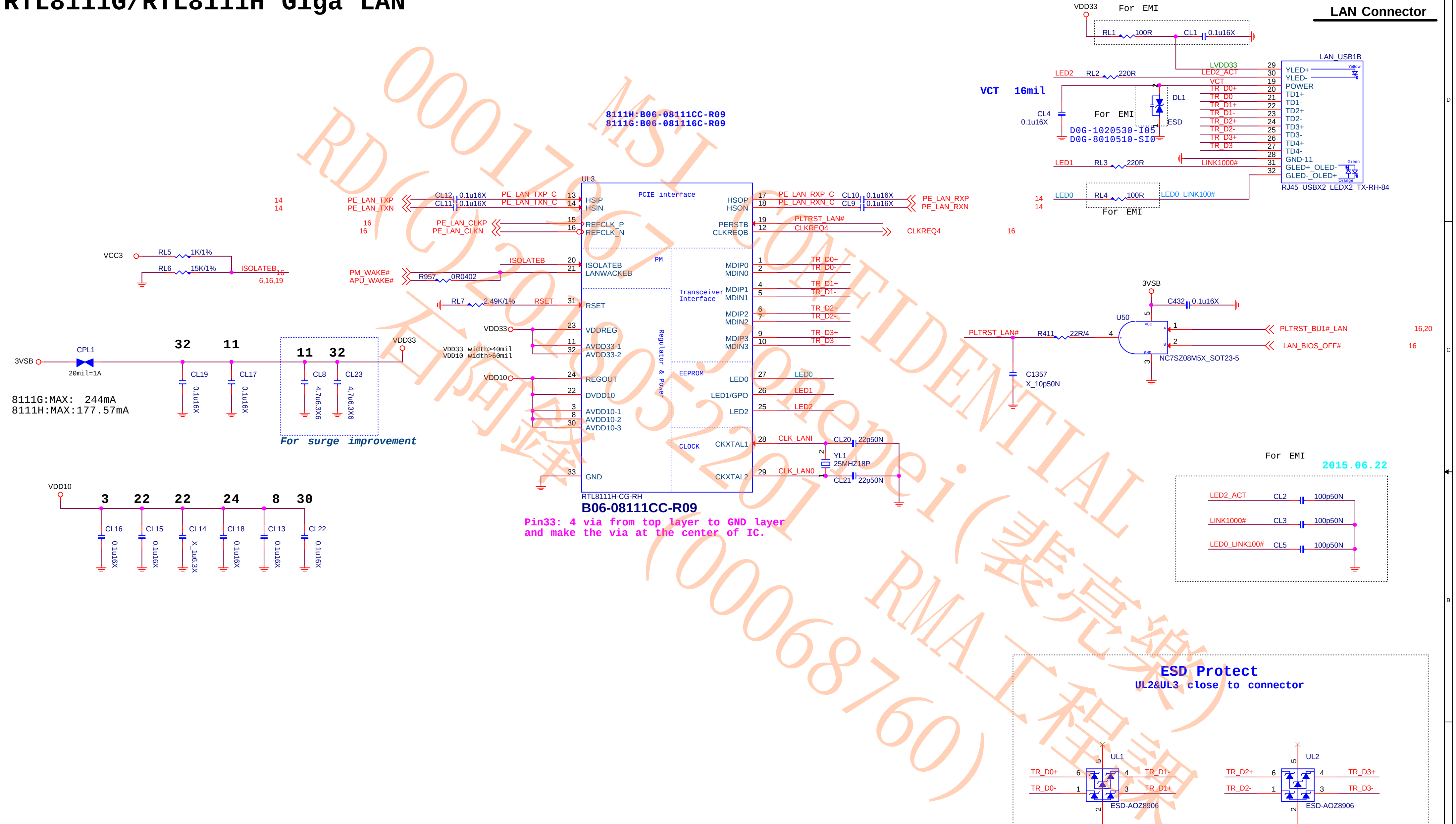
RTL8111G/RTL8111H Giga LAN



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: LAN-RTL8111H

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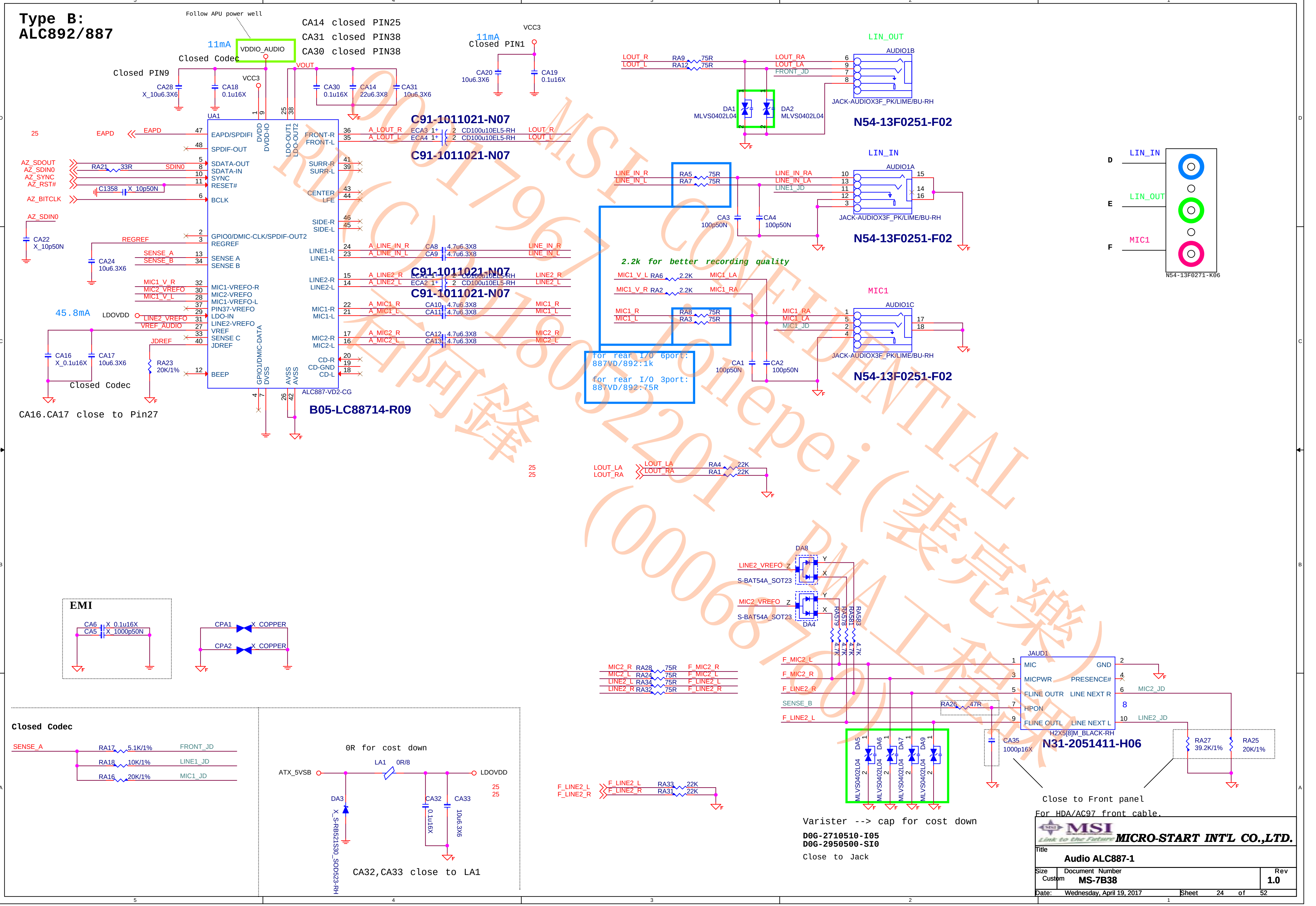

MICRO-START INT'L CO.,LTD.

Title: Audio ALC887-1

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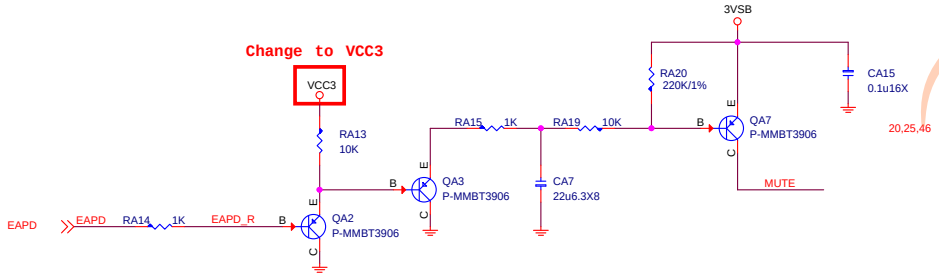
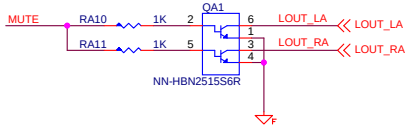
Rear Line OUT De-POP circuit

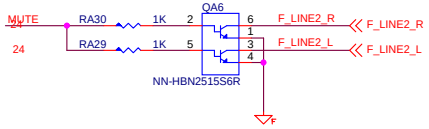
De-pop circuit for Rear Line out & Front Headphone out)

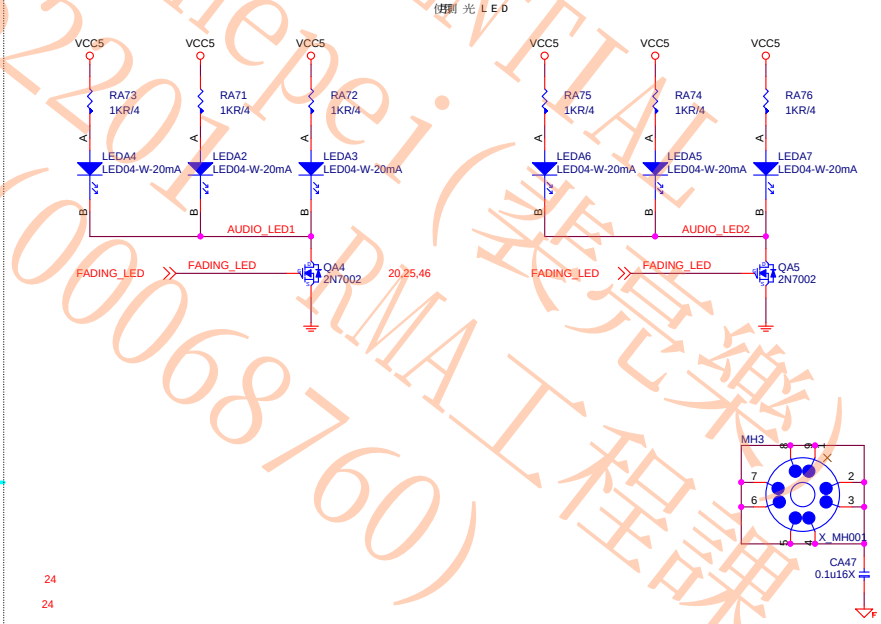


Digital

Analog







MSI Link to the Future **MICRO-START INTL CO.,LTD.**

Title	Audio ALC887-2	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
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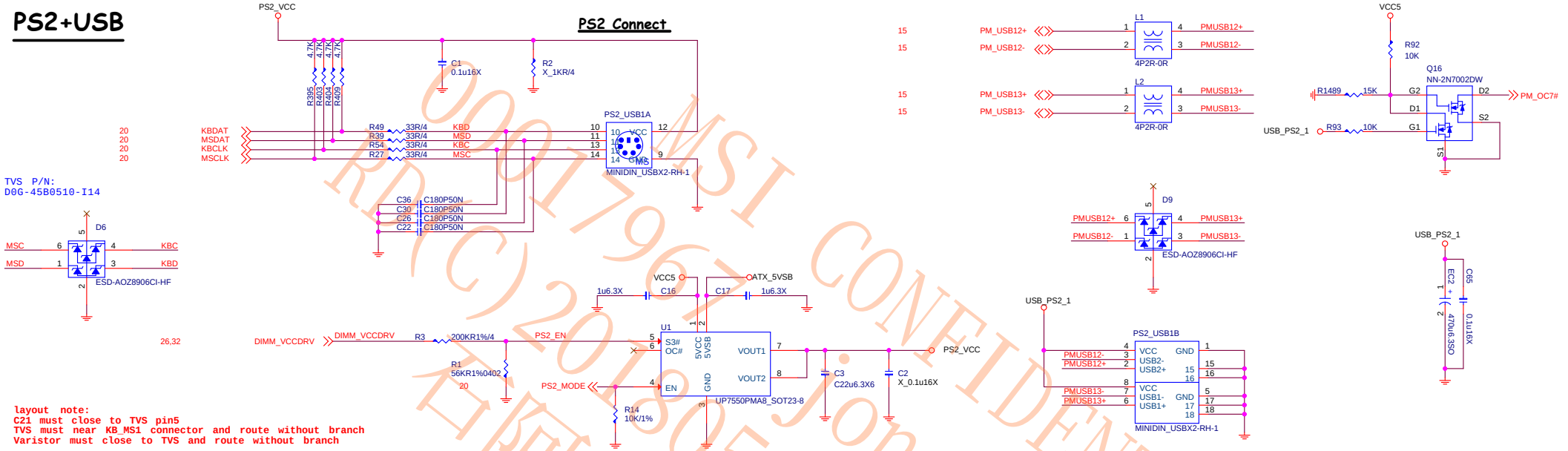
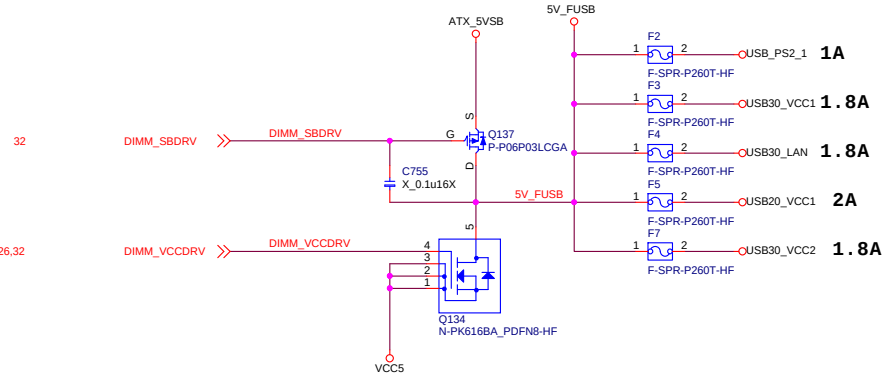
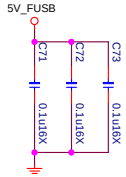
PS2+USB



layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

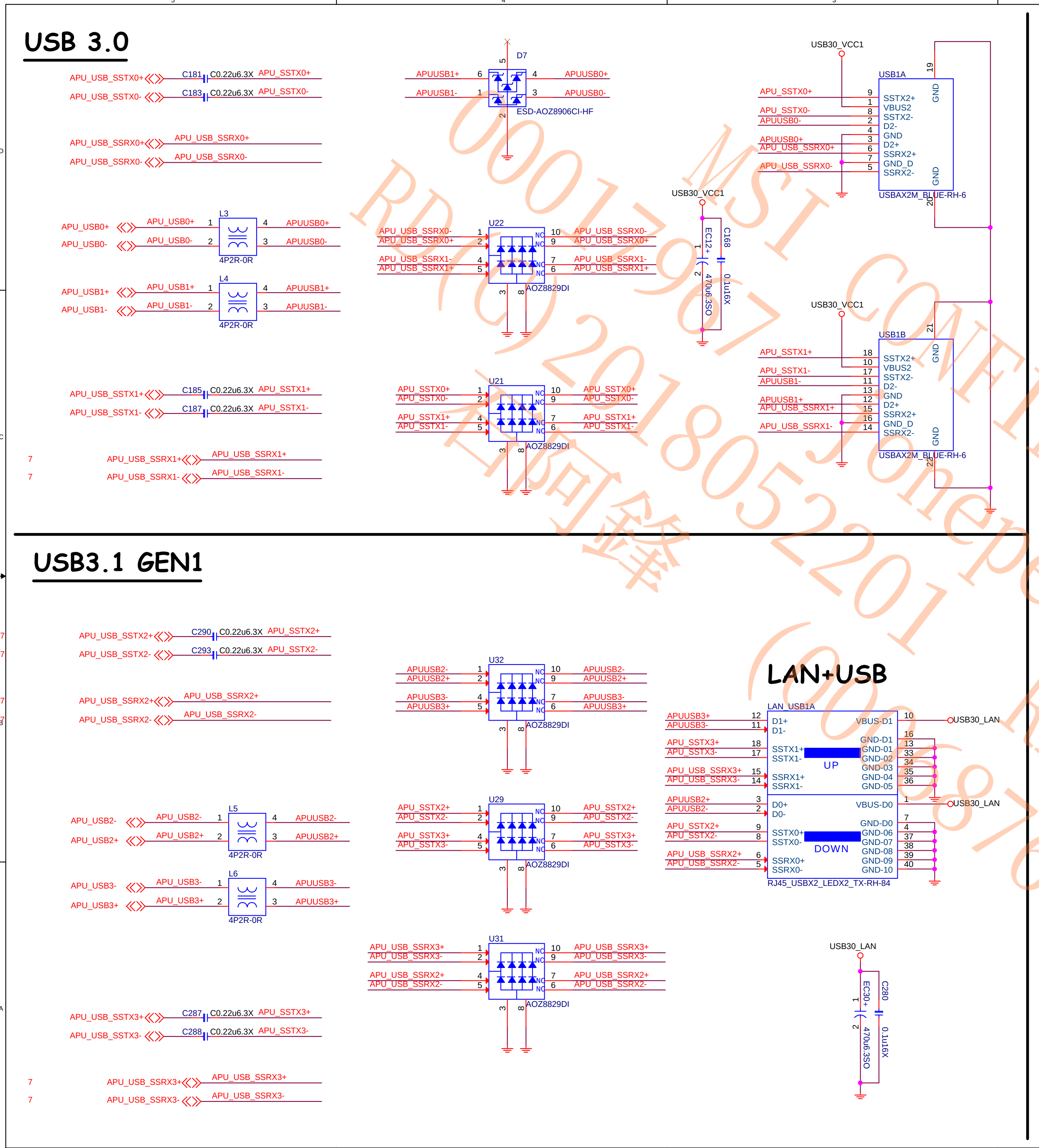
USB Power

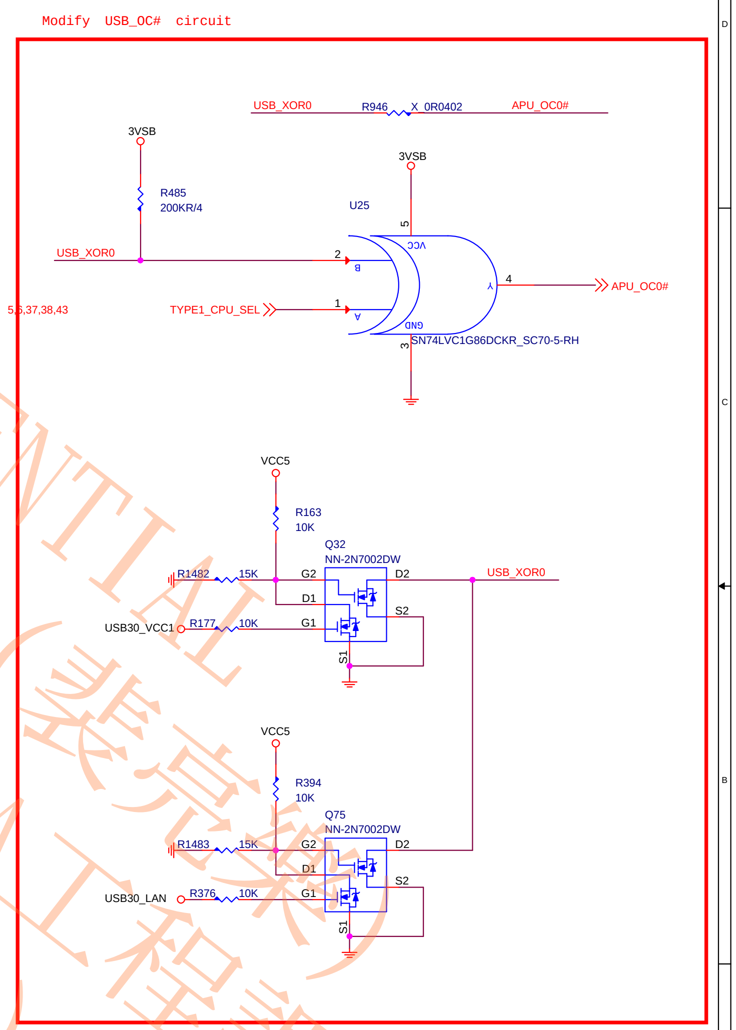




MSI MICRO-START INTL CO.,LTD.

Title: USB Rear PS2+USB2.0		
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 26 of 52	





	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MSI *Link to the Future* ***MICRO-START INT'L CO.,LTD.***

Title: **USB Rear LAN+USB3.1 GEN1**

Size	Document Number	Rev
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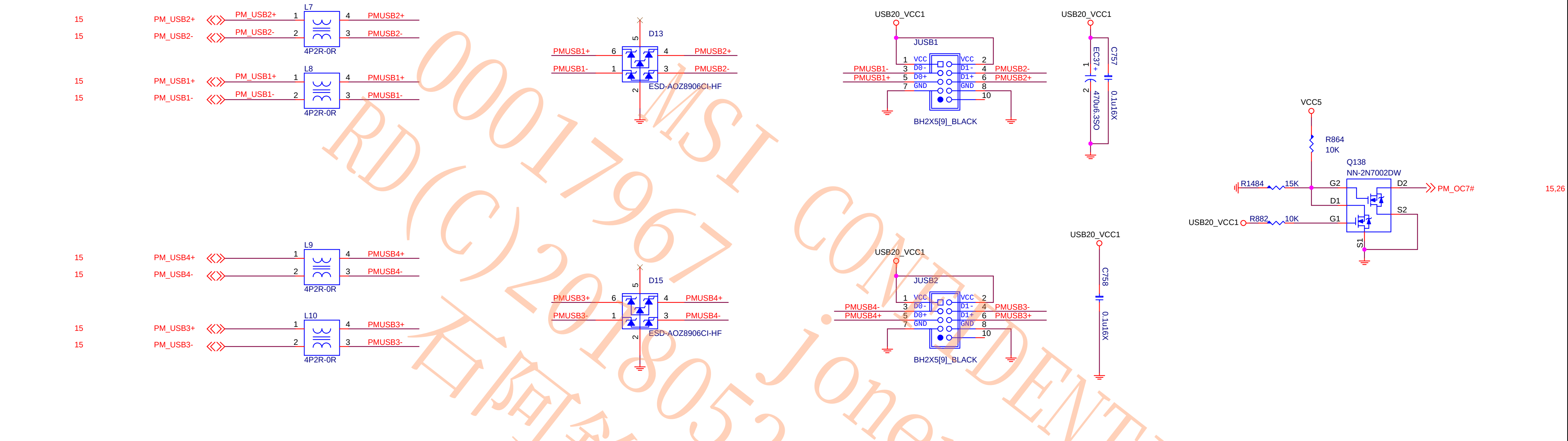
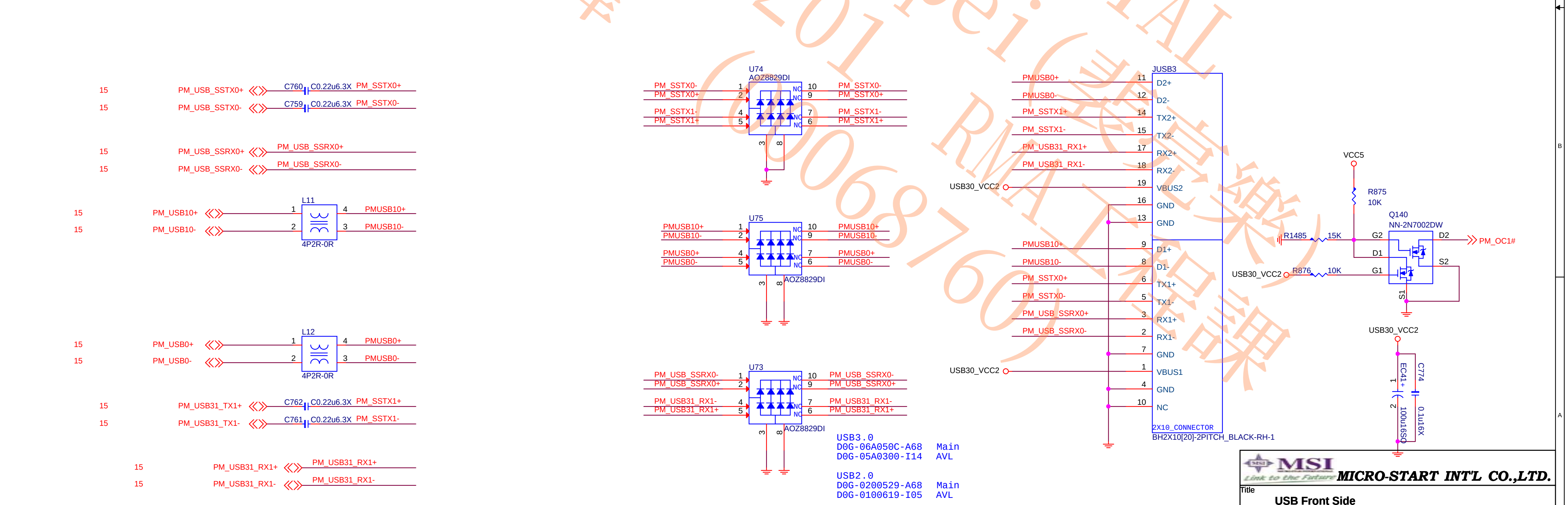
Front USB2.0



Front USB3.1 GEN1



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL

MSI MICRO-START INT'L CO.,LTD.

Title: USB Front Side

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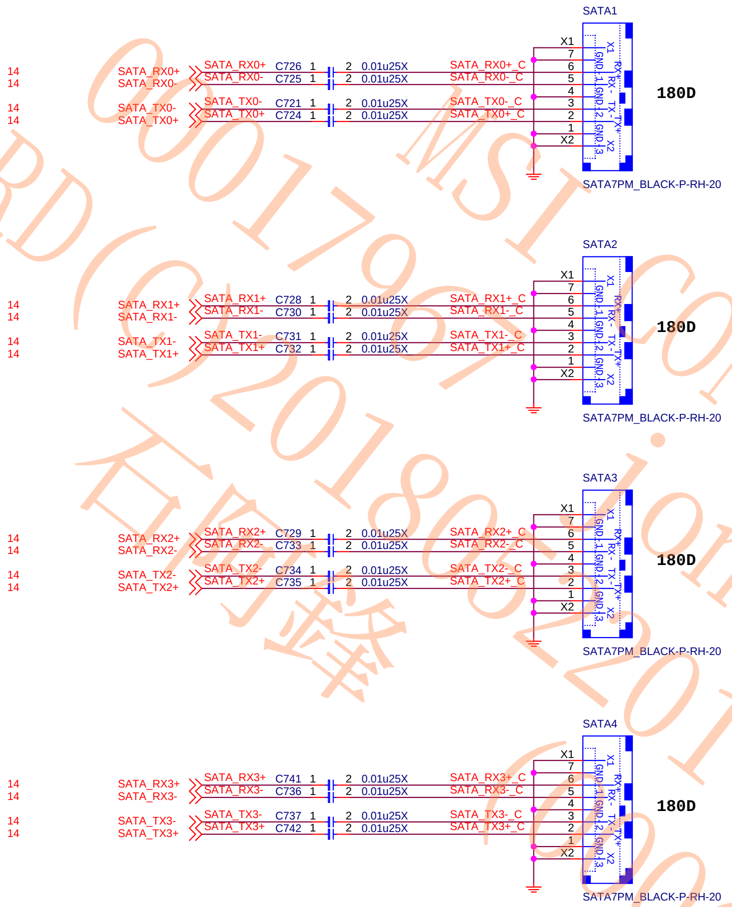
SATA Connector



MSI MICRO-START INT'L CO.,LTD.

Title: SATA Connector

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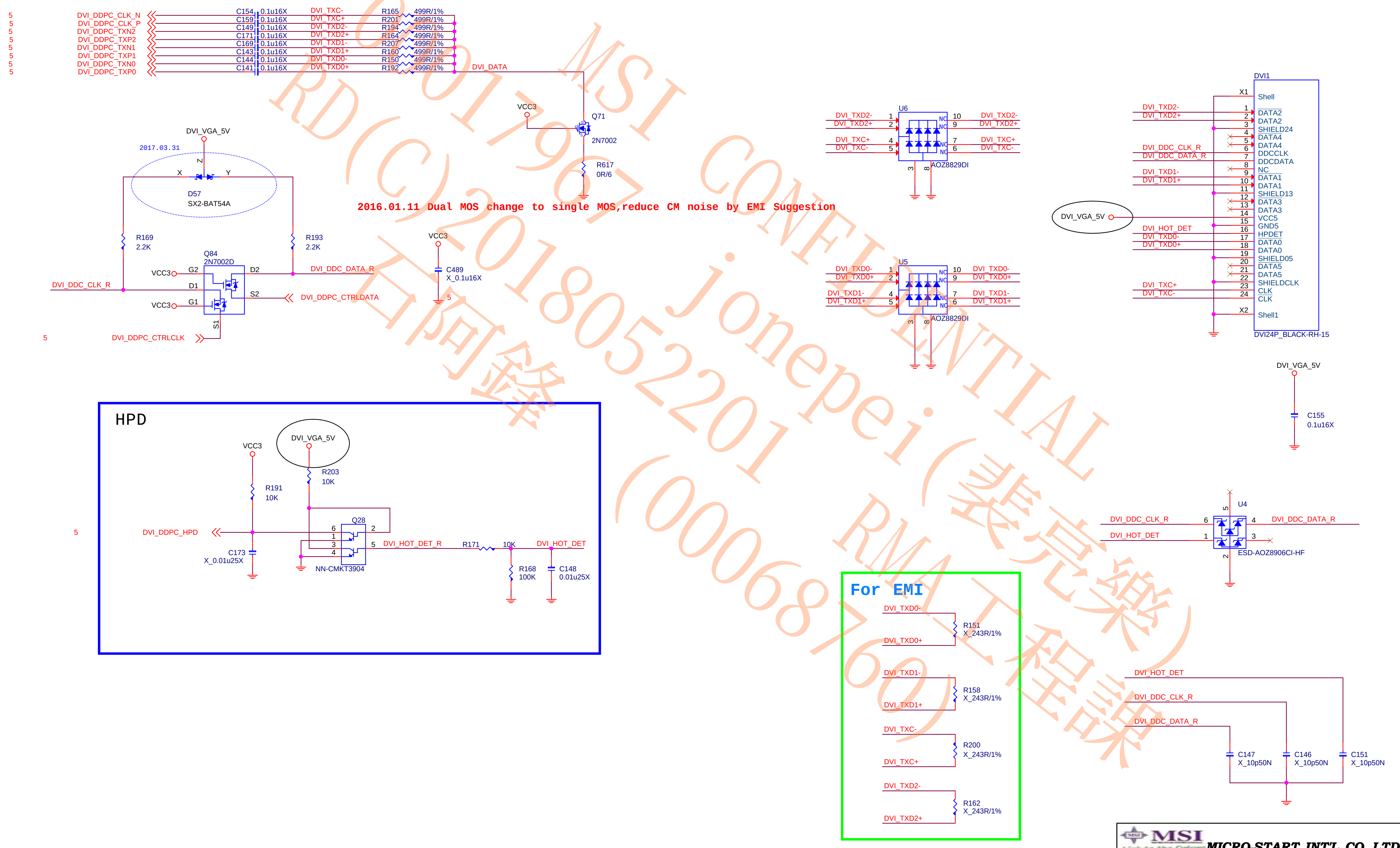
Date: Wednesday, April 19, 2017 | Sheet 29 of 52

DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion



MSI MICRO-START INT'L CO.,LTD.

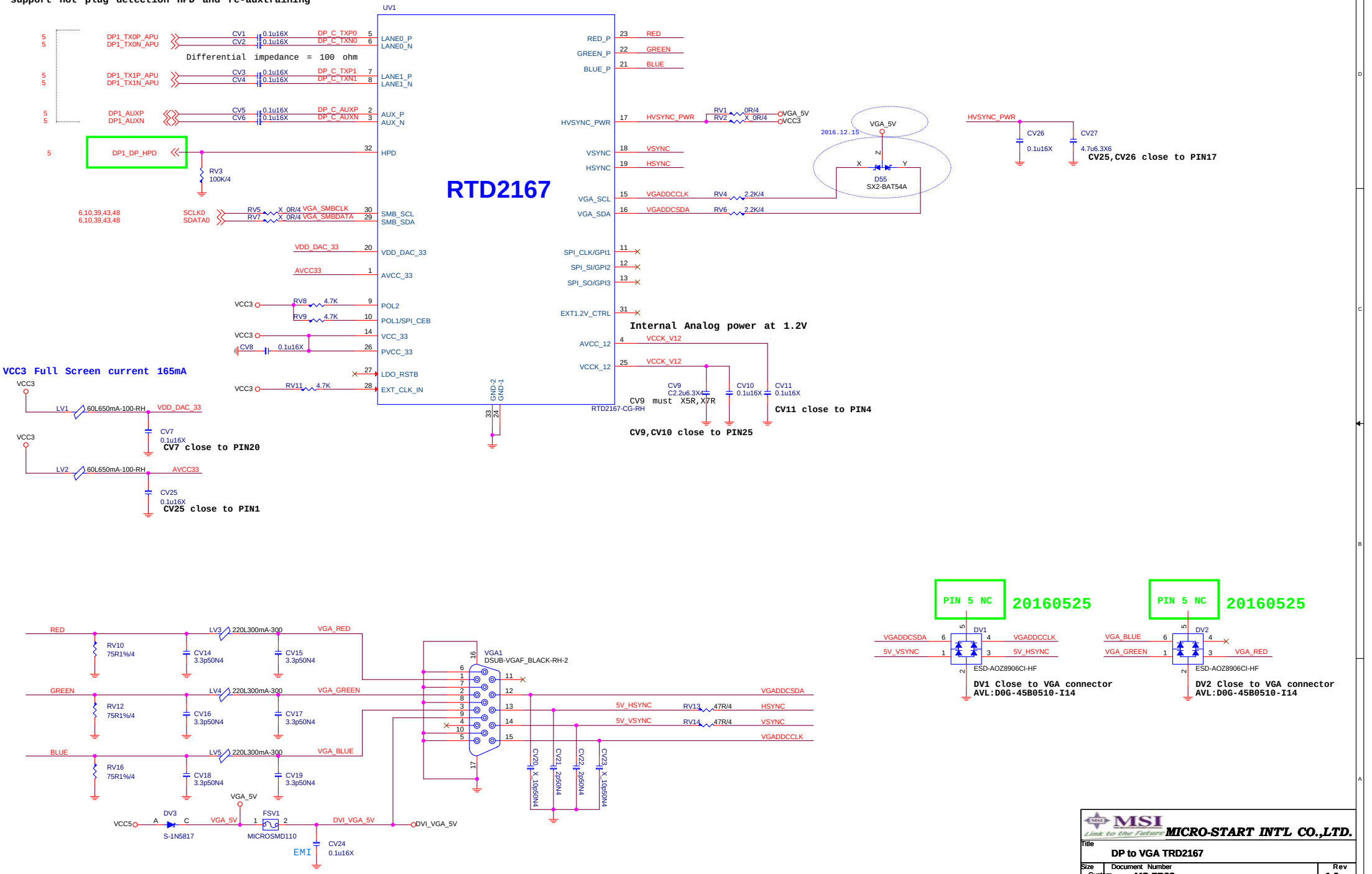
Title: HDMI Connector

Size	Document Number	Rev
Custom	MS-7B38	1.0

Date: Wednesday, April 19, 2017 Sheet 30 of 52

Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



MSI MICRO-START INTL CO.,LTD.

Title: DP to VGA TRD2167

Size: Custom | Document Number: MS-7B38 | Rev: 1.0

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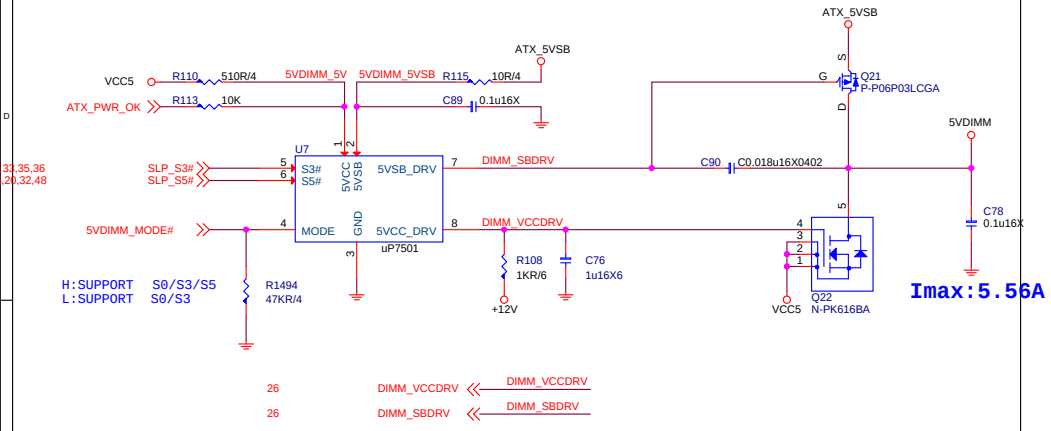
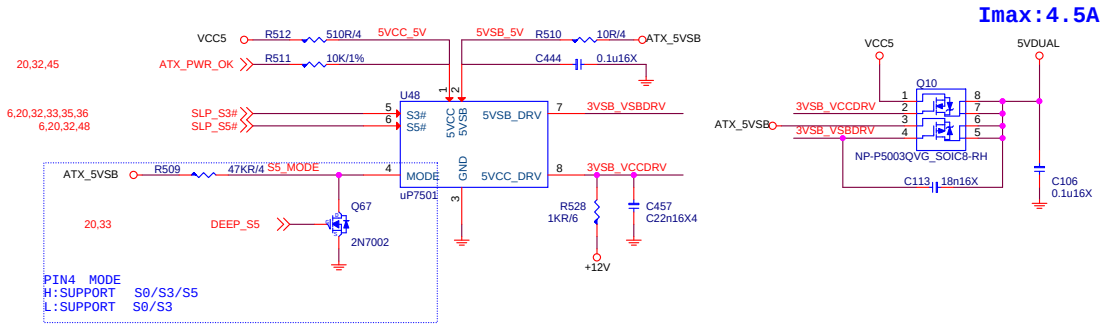
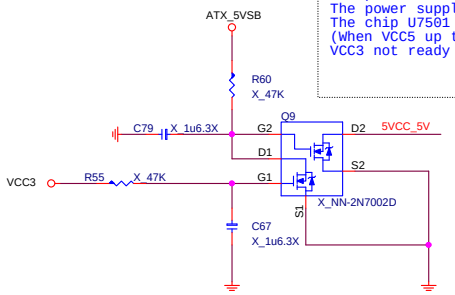
5VDIMM FOR DDR



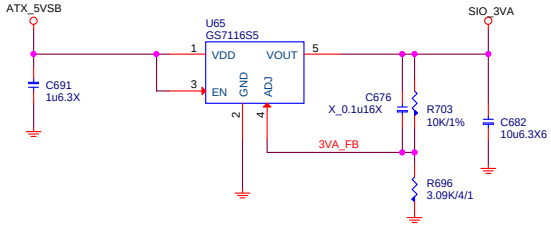
5VDUAL For 3VSB、CPU 1.8V、 VDDP



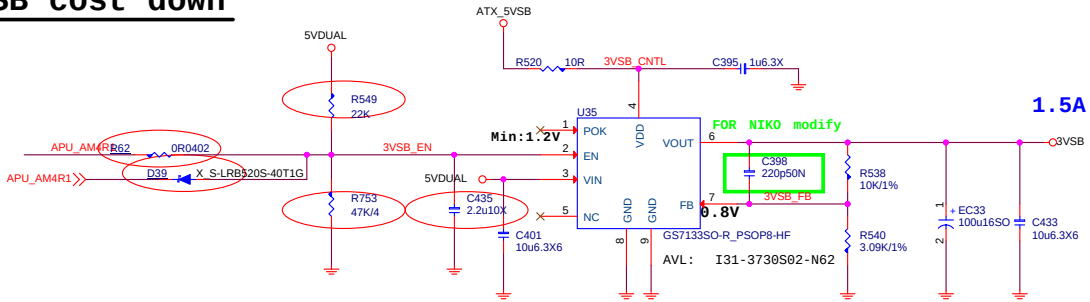
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



SIO_3VA



3VSB cost down



I31-7133S02-N03

MSI Link to the Future	MICRO-START INTL CO.,LTD.	
Title: ACPI uPI-5VDIMM&3VSB		
Size: Custom	Document Number: MS-7B38	Rev: 1.0
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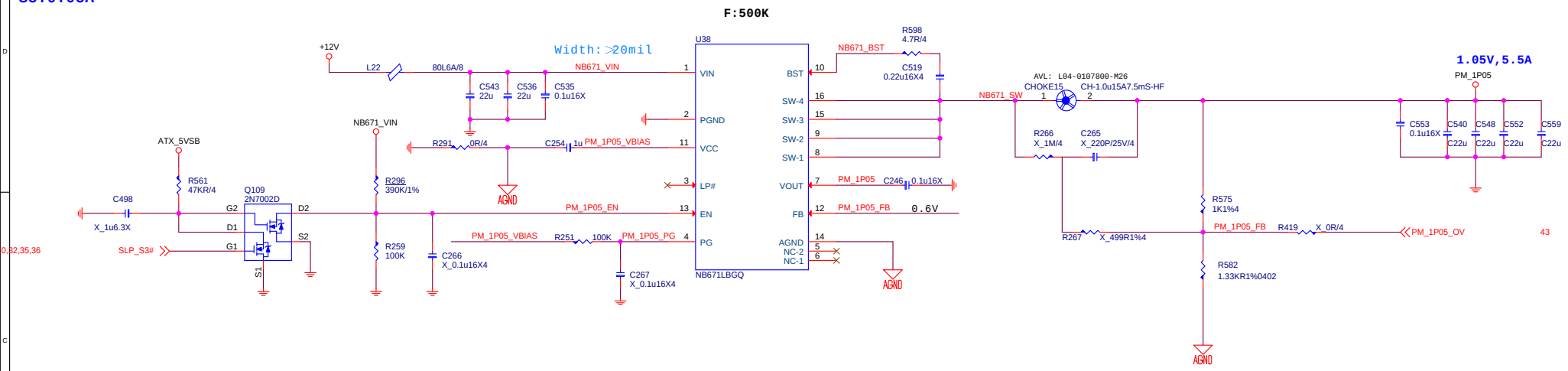
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

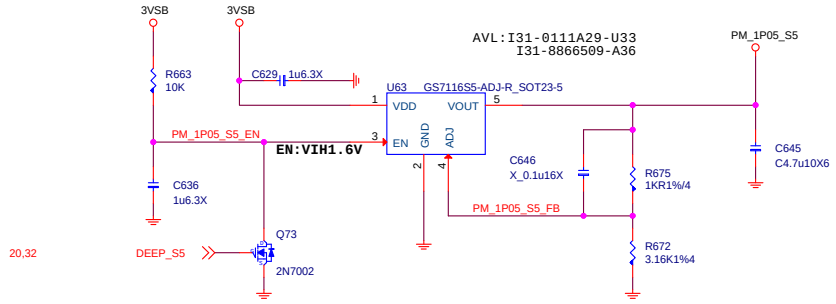
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH < 1.1664u H



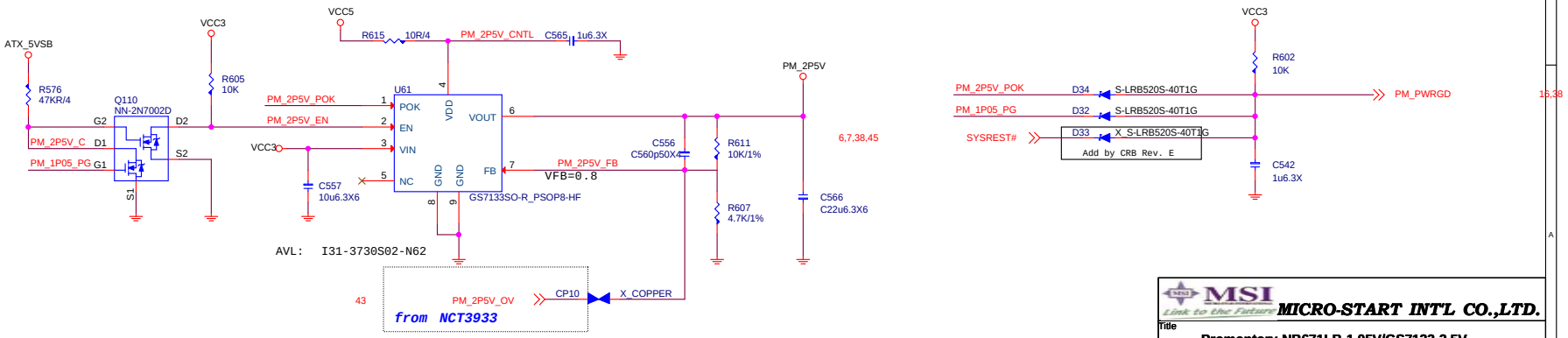
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

2.5V; 900mA



MSI MICRO-START INTL CO.,LTD.

Title	Promontory-NB671LB-1.05V/GS7133-2.5V	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
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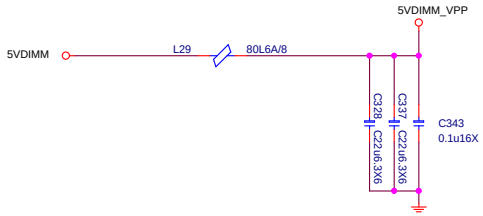
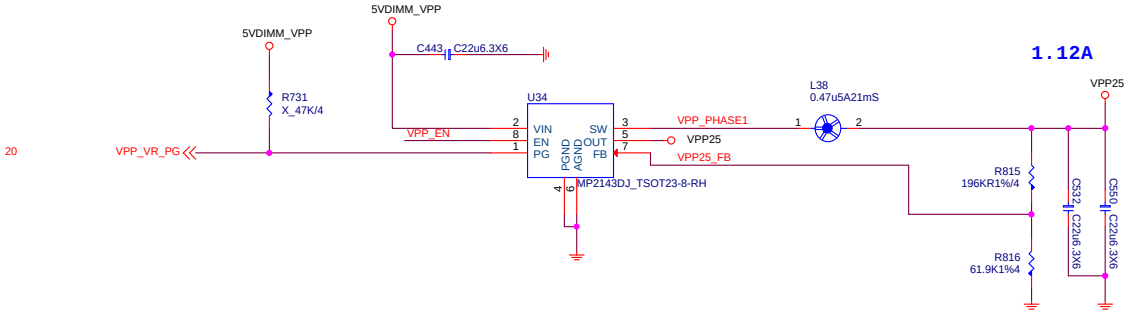
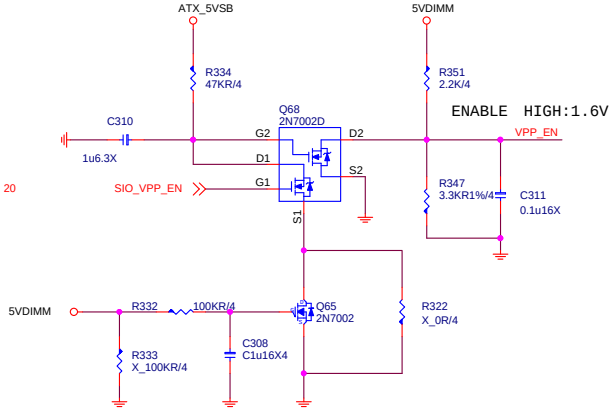
2DIMM :1.12A FOR DDR VPP2.5V







MSI Link to the Future	MICRO-START INTL CO.,LTD.		
Title: DDR PWR VPP25/VTT-MP2143			
Size: Custom	Document Number: MS-7B38		Rev: 1.0
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DDR4_1.2V 15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM

0.6A FOR DDR VTT

Irms = Iout * SQRT{D/N- (D)^2]}

VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675
L	0.75

2V

f:400KHz

By layout modify

OCP:27.5A

Imax: 20.85A

27.5A

FB:0.75V

Close to PIN19

default=1.36V

I32-8231A0C-R11

Add JOV1

MAX:20.85A

1.2V

1.1uH change to 0.47uH

0.1uFx1 per dimm

AGPIO84
Low , VCC_DDR Base 1.4V
High , VCC_DDR Base 1.36V

Title	DDR Power-RT8231AGQW
Size	Custom
Document Number	MS-7B38
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MICRO-START INTL CO.,LTD.

FOR CPU 1.8V S5

0.5A

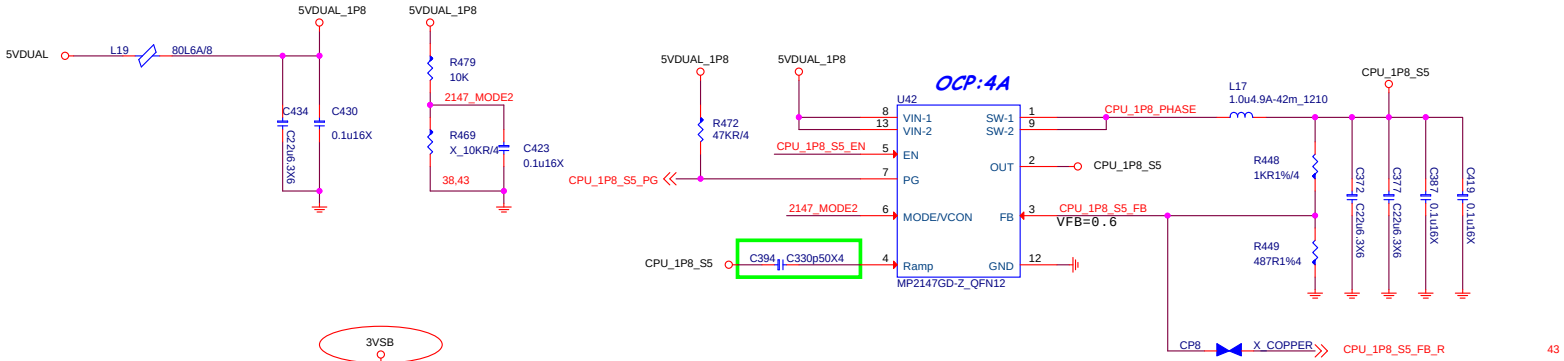
FOR VCCP_SOC_S5

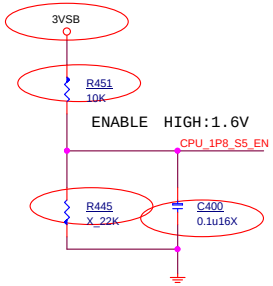
0.9A

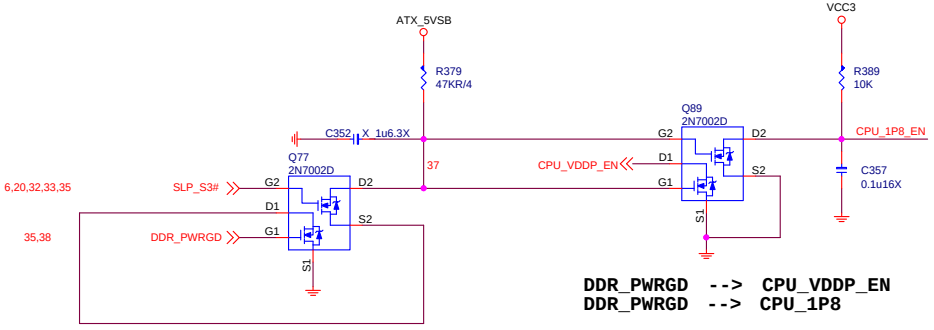
FOR CPU 1.8V S0

2.0A

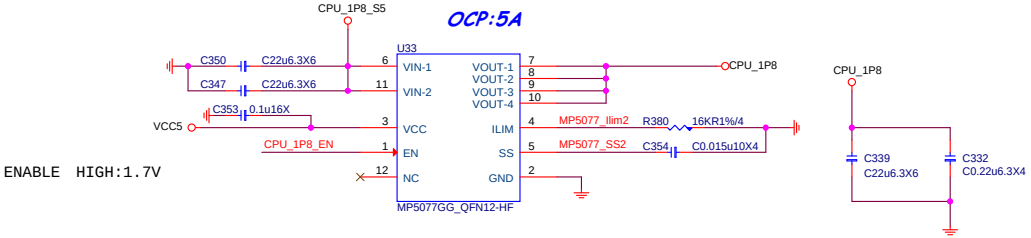
0.5A + 2.0A + 0.9A =3.4A







DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



ENABLE HIGH:1.7V

```
Ilimit=(1/Rlimit)*S,S=80000,when    VIN=1.8V
=(1/16)*80000=5.0375A

Tss=(1/3)*((Vout*Css)/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n)/9uA)=1mS
```

MSI Link to the Future **MICRO-START INTL CO.,LTD.**

Title: CPU Power 1P8V-MP2147		
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 36 of 52	

by layout

CPU_VDDP_S0

1.05V/0.9
S0:8.5A
OCP=12A

+12V
R406 100K1%4
EN:VIH1.6V
CPU_VDDP_EN
R418 33K/1%
C389 0.1u16X

VCC5
R437 10K
6,32,35,38
38
CPU_VDDP_PG

by layout
+12V
R494 10R/8
U6_VCC
C429 4.7u16X8

EN:VIH1.6V
EN pin Maximum:6.5V

APU_AM4R1
D20 S-LRB520S-40T1G-HF
CPU_VDDP_EN

U41
EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT
PHASE
UGATE
LGATE/OCSET
FB
RT8125EGQW_WDFN10-HF

CPU_VDDP_BOOT1
CPU_VDDP_PH1
CPU_VDDP_UG1
CPU_VDDP_LG1
CPU_VDDP_FB
R484 0R/6
C440 0.1u16X25

CPU_VDDP_REFOUT
C426 C1000p50X4
R453 768R1%4
CPU_VDDP_REFIN
C374 C1000p50X4
R463 4.53KR1%4
0.8V
0.684V

FB:0.8V

CPU_VDDP
R420 10R1%4
R438 1KR1%/4
CPU_VDDP_SENSE_R
R421 0R/4
CPU_VDDP_SENSE
C399 X_0.1u16X
R450 3.16K/1%

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/3.16K))
= 1.05V

Vout = Vref * (1 +(R1/R2))
= 0.684 * (1 +(1K/3.16K))
= 0.9V

AM4_CPU_SEL
0:Type 0/1 1.05V
1:Type 2/3 0.9V

Q86
NN-2N7002DW
TYPE1_CPU_SEL
16
PM_GPIO_R9
CPU_VDDP_OV
CP25
X_COPPER

PM_GPIO_R9
1:Type 0/1 1.05V
0:Type 2/3 0.9V

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.8 * 0.282566
= 3.46A

TYPE0_CPU_SEL:
1:TYPE 0
0:TYPE 2
TYPE1_CPU_SEL:
0:TYPE 0
1:TYPE 2
CPU_VDDP_EN:
0:TYPE 2
1:TYPE 0

Q92
NN-2N7002DW
TYPE0_CPU_SEL
VDDP_SEL
TYPE1_CPU_SEL
CPU_VDDP_EN
CPU_VDDP_EN
VDDP_SEL

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

36

12VCC_IN
CHOKE14
CH-0.47u5A21mS-HF
+12V
C461 C1u16X6
C460 22u16X8
EC11 270u16SO
C446 0.1u16X

CPU_VDDP_UG1
R508 0R/6
CPU_VDDP_UG1_R
R500 X_10KR/4
N-PK616BA_PDFN8-HF
Q97

CPU_VDDP_PH1

CPU_VDDP_LG1
R475 5.1K/1%/4
N-PK632BA_PDFN8-HF
Q96

OCPSET:min 5Kohm
OCP
=(R475*10uA)/DCR
=(5.1k*10uA)/3.3m
=15.45A

CHOKE13
1.0u15A7.5mS-HF
CPU_VDDP
R482 X_2.2R/8
snubber
C437 X_C3300p50X4
C334 1u6.3X
C425 C22u6.3X6
EC31 560u6.3SO
EC32 560u6.3SO

OCP=12A
1.05V,8.5A

CPU_VDDP_S5

VDDP_S5 1.05V/0.9
S5:1A

3VSB
R501 X_10KR/4
38
VDDP_VSB_PG
3VSB
R502 10K
VDDP_VSB_EN
C390 1u6.3X

5VDUAL
L20 80L6A/8
C439 C22u6.3X6
VDDP_VSB_VIN
VDDP_VSB_EN
VDDP_VSB_PG
Internal Pull-Up 500K

U45
VIN
EN
PG
SW
OUT
FB
PGND
AGND
MP2143DJ

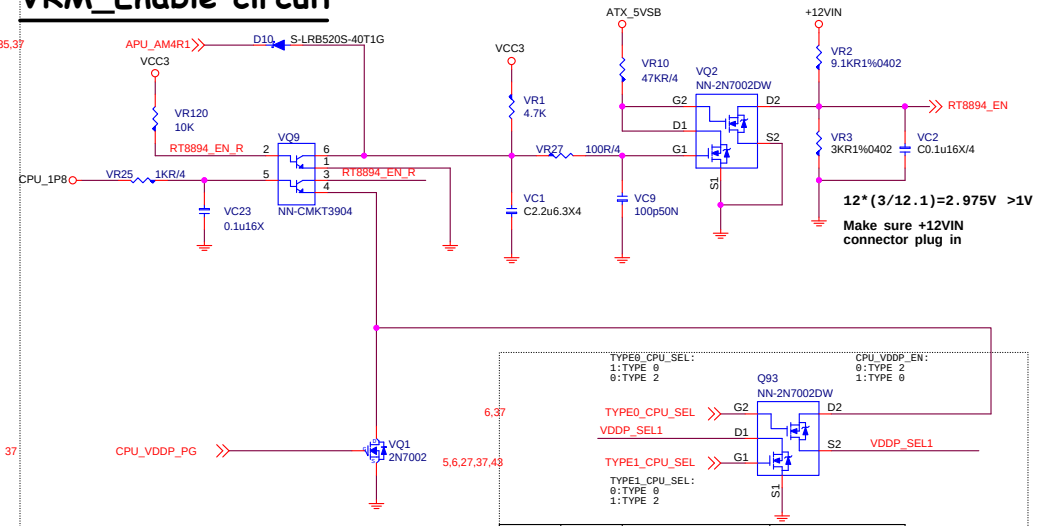
VDDP_VSB_PHASE
L18 1.0u6.3A_1210-HF
VDDP_VSB_FB
R489 1KR1%/4
R488 2KR1%/4
C412 C22u6.3X6
C421 C22u6.3X6
C427 C0.22u6.3X4
CPU_VDDP_S5
5,6,27,37,38,43

VDDP_VSB_FB
ATX_5VSB
R490 47KR/4
R464 3.83KR1%4
C436 0.1u16X
Q95
NN-2N7002DW
TYPE1_CPU_SEL
AM4_CPU_SEL
0:Type 0/1
1:Type 2/3

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

MSI
MICRO-START INTL CO.,LTD.
Title
CPU Power VDDP-RT8125E
Size Custom
Document Number MS-7B38
Rev 1.0
Date: Wednesday, April 19, 2017
Sheet 37 of 52

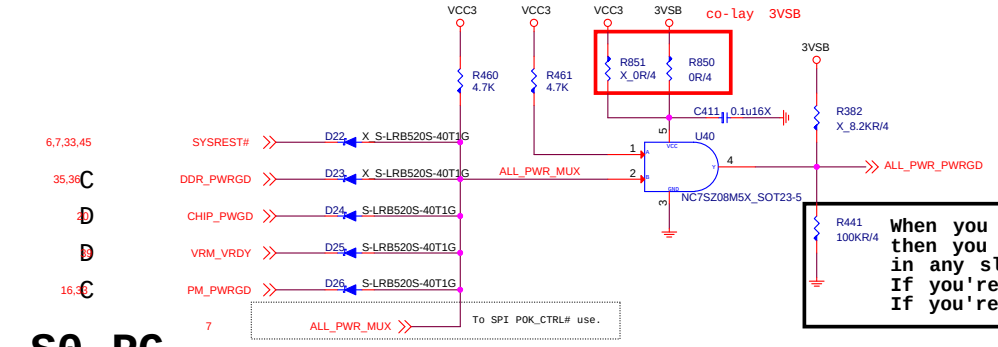
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

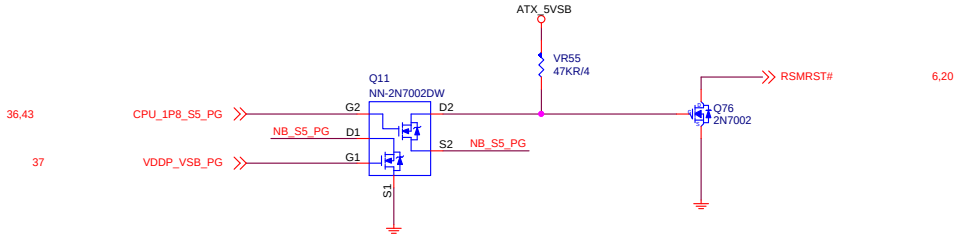


R441 100KR/4

When you use external buffer then you cannot let APU PWR_GOOD pin float in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MSI Link to the Future MICRO-START INTL CO.,LTD.

Title	CPU PWR-IR3599	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
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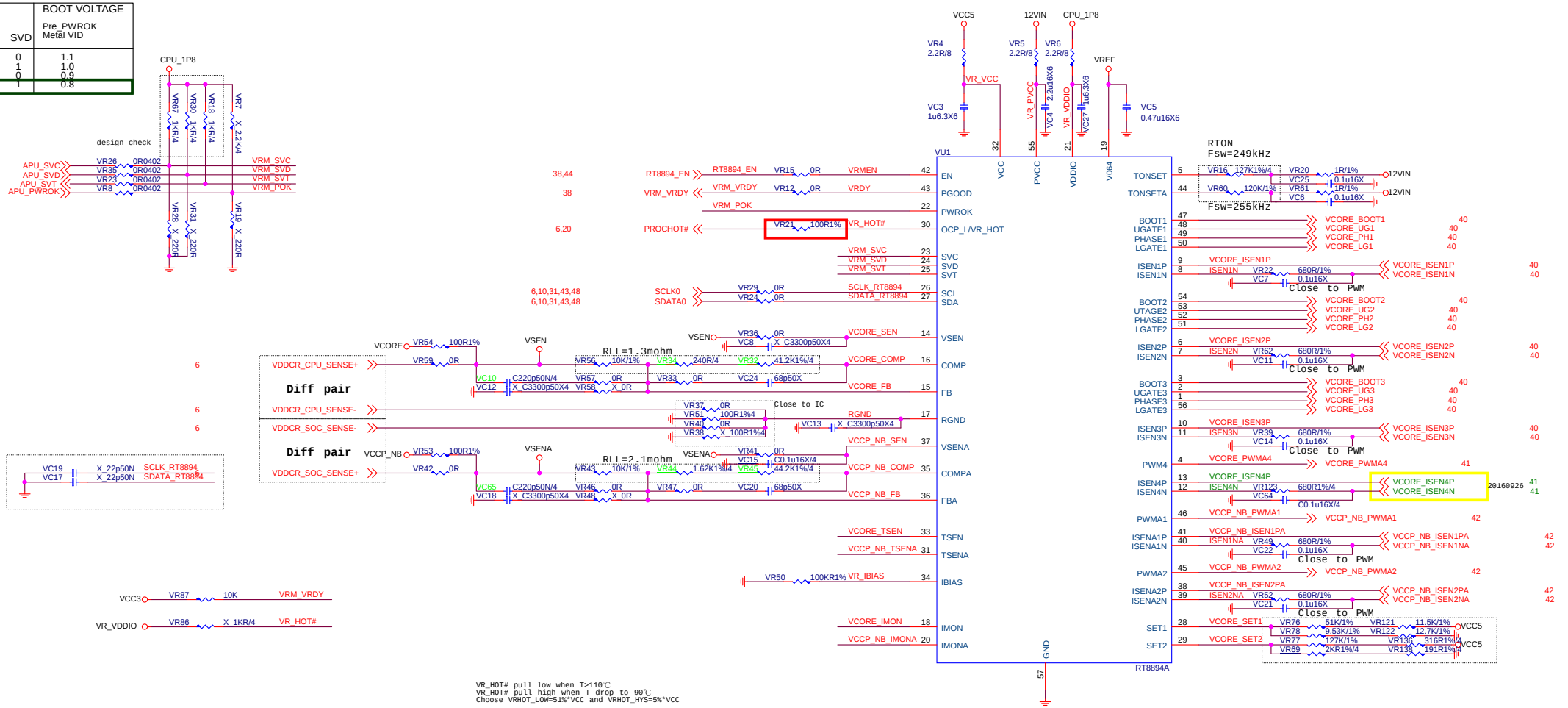
Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



Title	CPU Power RT8894 3+2 Phase
Size	Custom
Document Number	MS-7B38
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Date:	Wednesday, April 19, 2017
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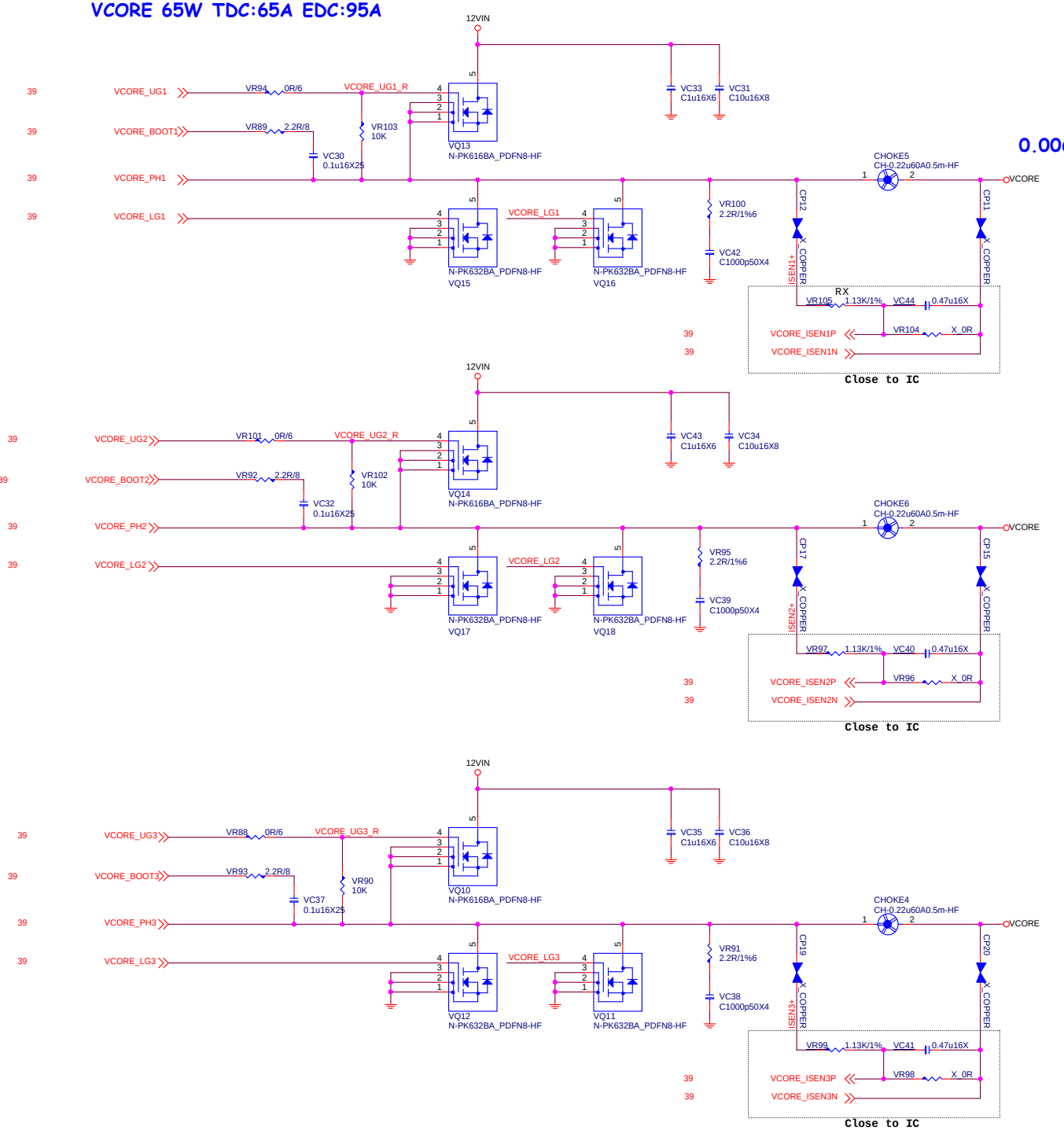
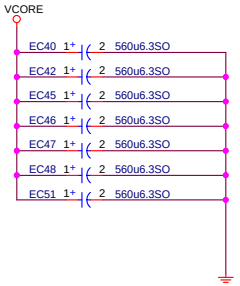
MSI MICRO-START INTL CO.,LTD.

VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

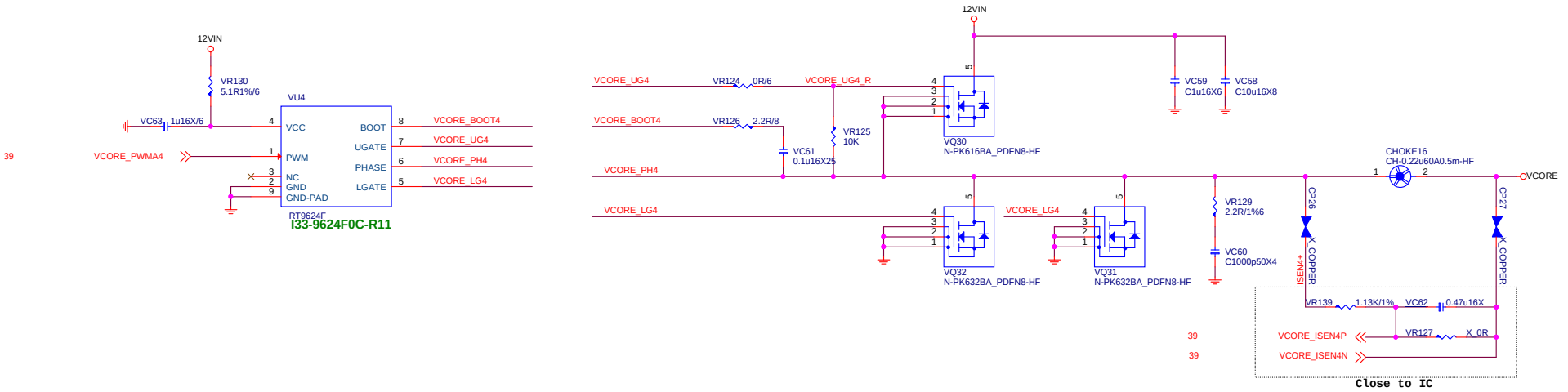


0.00625V~1.55V

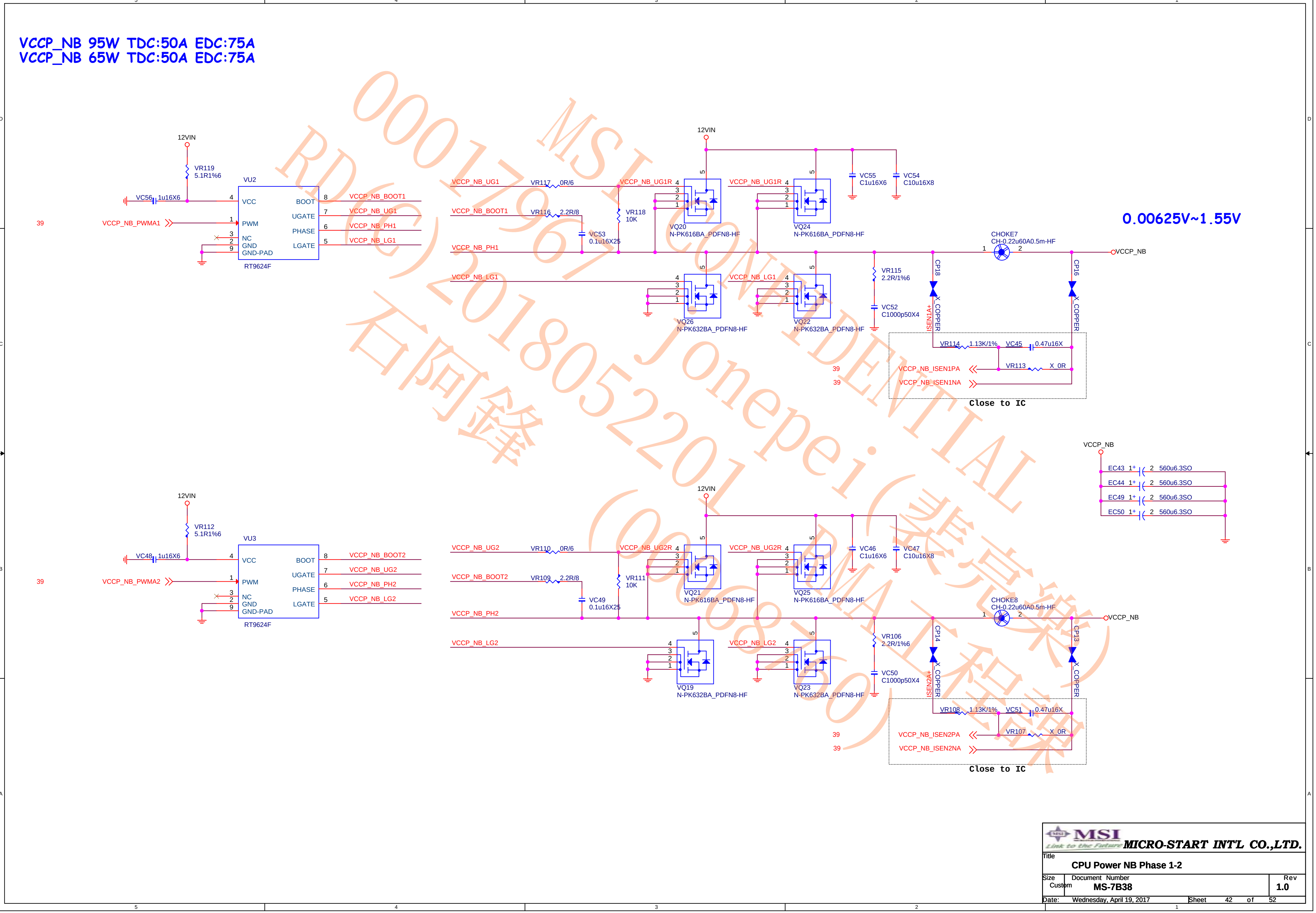


MICRO-START INTL CO.,LTD.

Title: CPU Power Phase 1-3		
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 40 of 52	



MSI Link to the Future	MICRO-START INTL CO.,LTD.		
Title: CPU Power Phase 1-3			
Size: Custom	Document Number: MS-7B38		Rev: 1.0
Date: Wednesday, April 19, 2017		Sheet 41 of 52	


VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A
0.00625V~1.55V
12VIN
VR119 5.1R1%6
VU2
VC56 1u16X6
VCC
BOOT
UGATE
PHASE
LGATE
PWM
NC
GND
GND-PAD
RT9624F
39
VCCP_NB_PWMA1
VCCP_NB_BOOT1
VCCP_NB_UG1
VCCP_NB_PH1
VCCP_NB_LG1
VR117 0R/6
VR116 2.2R/8
VC53 0.1u16X25
VR118 10K
VCCP_NB_UG1R
VQ20 N-PK616BA_PDFN8-HF
VQ24 N-PK616BA_PDFN8-HF
VC55 C1u16X6
VC54 C10u16X8
VQ26 N-PK632BA_PDFN8-HF
VQ22 N-PK632BA_PDFN8-HF
VR115 2.2R/1%6
VC52 C1000p50X4
CHOKE7 CH-0.22u60A0.5m-HF
VCCP_NB
CP18 X_COPPER
CP16 X_COPPER
ISEN1A+
VR114 1.13K/1%
VC45 0.47u16X
VR113 X_0R
VCCP_NB_ISEN1PA
VCCP_NB_ISEN1NA
Close to IC
EC43 560u6.3SO
EC44 560u6.3SO
EC49 560u6.3SO
EC50 560u6.3SO
VR112 5.1R1%6
VU3
VC48 1u16X6
VCCP_NB_PWMA2
VCCP_NB_BOOT2
VCCP_NB_UG2
VCCP_NB_PH2
VCCP_NB_LG2
VR110 0R/6
VR109 2.2R/8
VC49 0.1u16X25
VR111 10K
VCCP_NB_UG2R
VQ21 N-PK616BA_PDFN8-HF
VQ25 N-PK616BA_PDFN8-HF
VC46 C1u16X6
VC47 C10u16X8
VQ19 N-PK632BA_PDFN8-HF
VQ23 N-PK632BA_PDFN8-HF
VR106 2.2R/1%6
VC50 C1000p50X4
CHOKE8 CH-0.22u60A0.5m-HF
CP14 X_COPPER
CP13 X_COPPER
ISEN2A+
VR108 1.13K/1%
VC51 0.47u16X
VR107 X_0R
VCCP_NB_ISEN2PA
VCCP_NB_ISEN2NA
Close to IC
MSI
MICRO-START INT'L CO.,LTD.
Title
CPU Power NB Phase 1-2
Size Custom
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Rev 1.0
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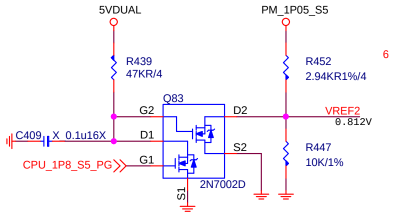
FOR VCCP_SOC_s5
0.9A

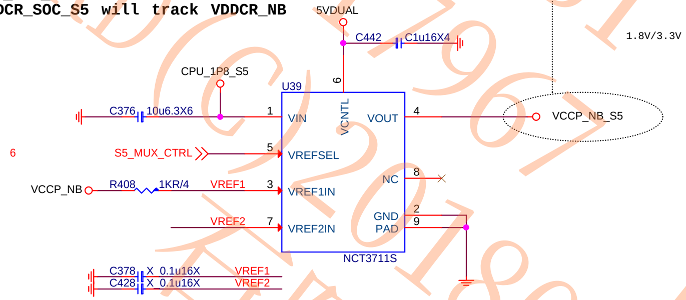
TYPE0 Only

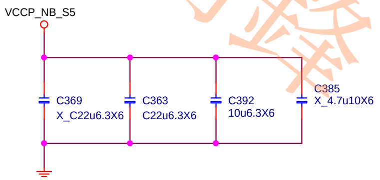
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

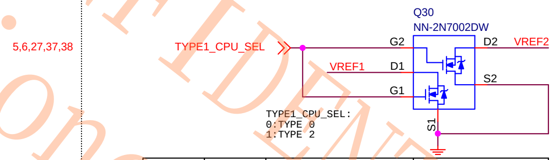
(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)Bristol Ridge TYPE0







5,6,27,37,38



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

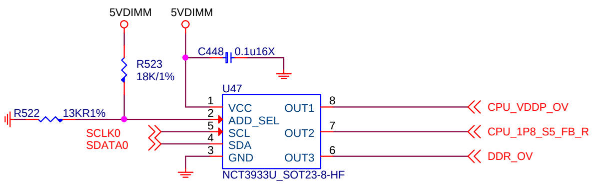
CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

UPI VOLTAGE CONSOLE

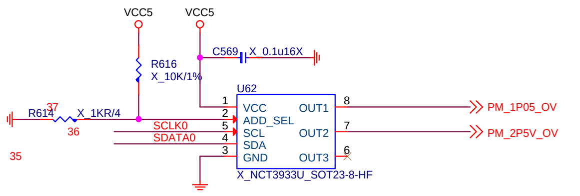
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x26:RH=18K,RL=13K

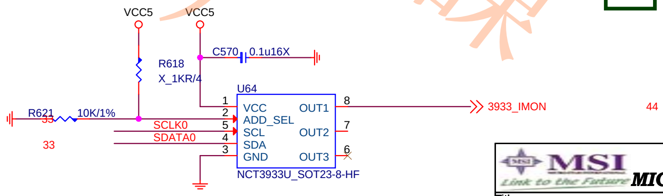


除非超過要求功能 有任 何 幫 助 ,否則不 上N CT3933 與關 超過選 項

0x20:RH=10K,RL=OPEN



0x2A:RH=OPEN,RL=10K



44

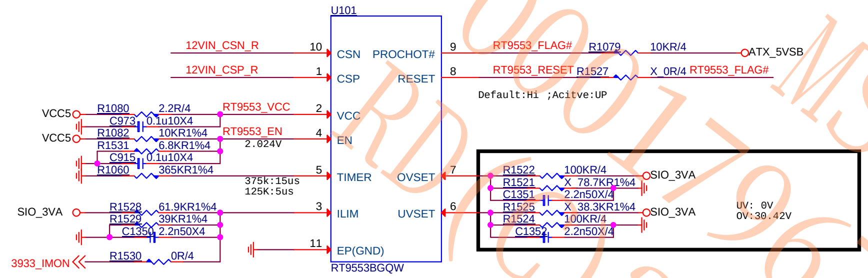
MICRO-START INT'L CO.,LTD.

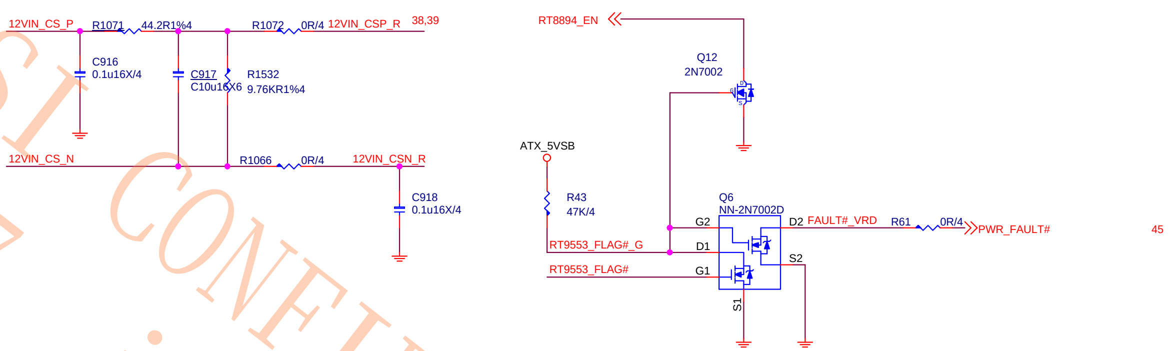
Title	CPU Power NB Switch / NCT3933 OV	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 43 of 52	

RT9553B CURRENT SENSE

VCORE EDC MAC 125A

NB EDC MAX75A





OCP:30A

Real OCP:30.05A

R17+R18>100k Vsio_3va= 3.38V Rdcr= 0.5 mohm

I3933_imon*[R17*R18/(R17+R18)]= Istep* Rdcr*100

I3933_imon= 10uA/step

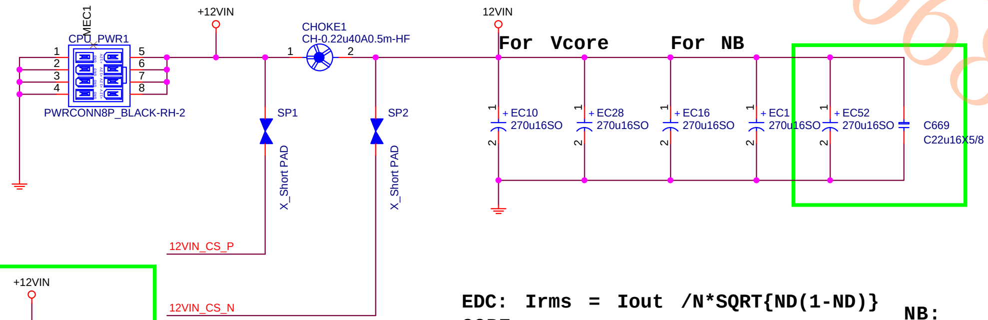
Istep=4.968A

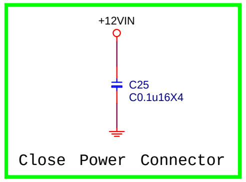
CPU POWER CONNECTOR

uP6273 CURRENT SENSE

VCORE EDC MAC 125A

NB EDC MAX75A





TDC: Irms = Iout /N*SQRT{ND(1-ND)}

CORE:

D=Vout/Vin=1.5/12=0.125

N=Phase number=4

=80/4*SQRT{4*0.125*[1-4*0.125]}

=10A

NB:

D=Vout/Vin=1.2/12=0.1

N=Phase number=2

=65A/2*SQRT(2*0.1*(1-2*0.1))

=13A

EDC: Irms = Iout /N*SQRT{ND(1-ND)}

CORE:

D=Vout/Vin=1.5/12=0.125

N=Phase number=4

=125/4*SQRT{4*0.125*[1-4*0.125]}

=15.625A

NB:

D=Vout/Vin=1.2/12=0.1

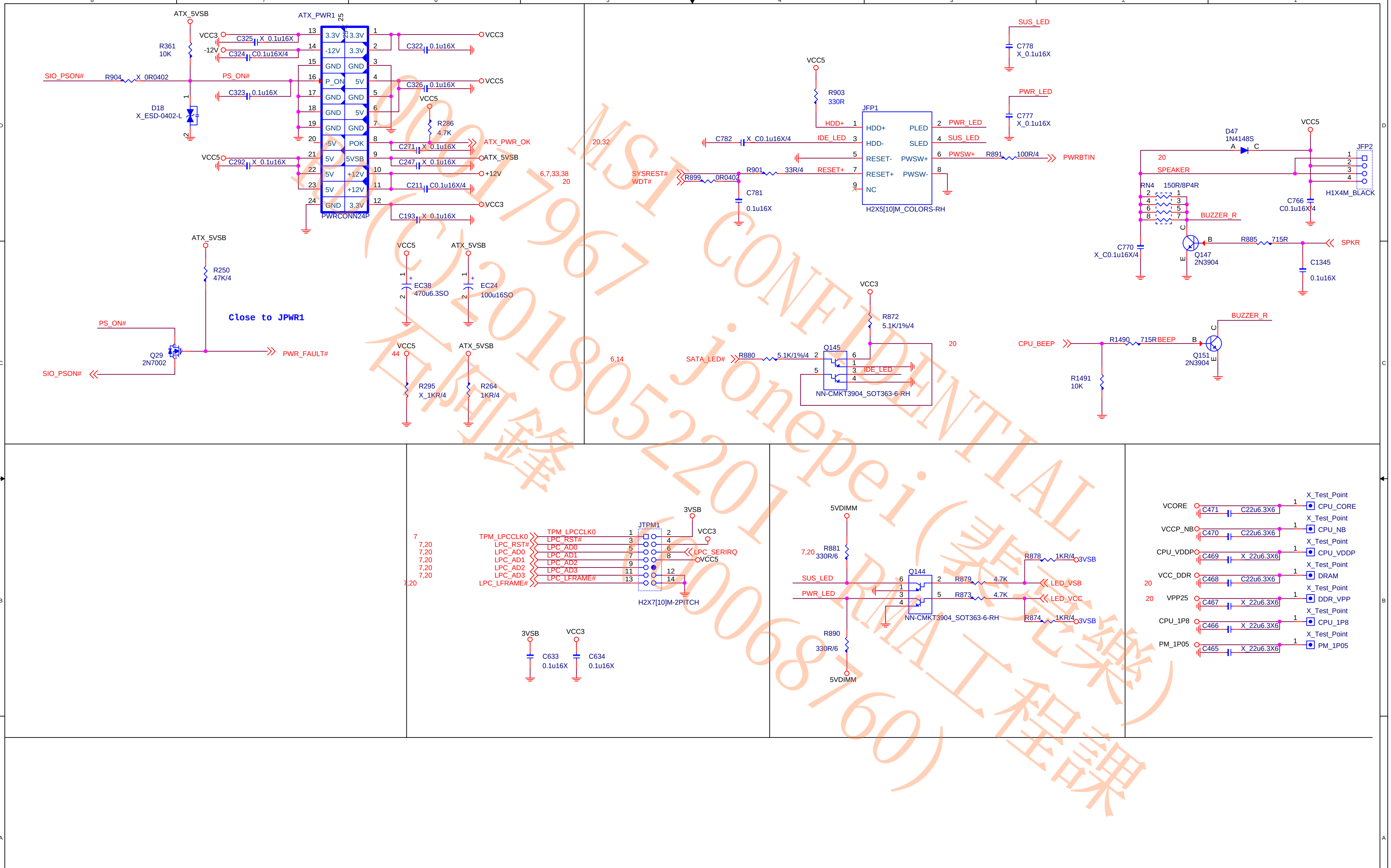
N=Phase number=2

=75A/2*SQRT(2*0.1*(1-2*0.1))

=15A

MICRO-START INT'L CO.,LTD.

Title	uP6273 CURRENT SENSE	
Size: Custom	Document Number: MS-7B38	Rev: 1.0
Date: Wednesday, April 19, 2017	Sheet 44 of 52	



MICRO-START INT'L CO.,LTD.

Title: ATX/Front Panel

Size	Document Number	Rev
Custom	MS-7B38	1.0

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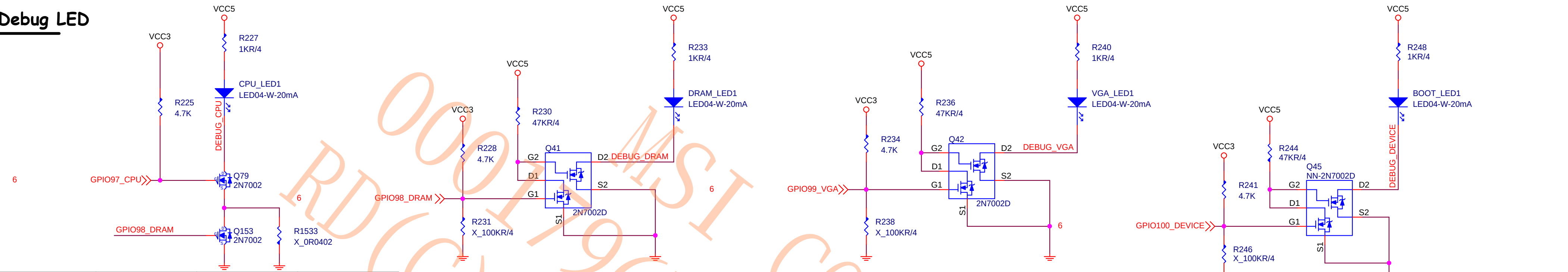
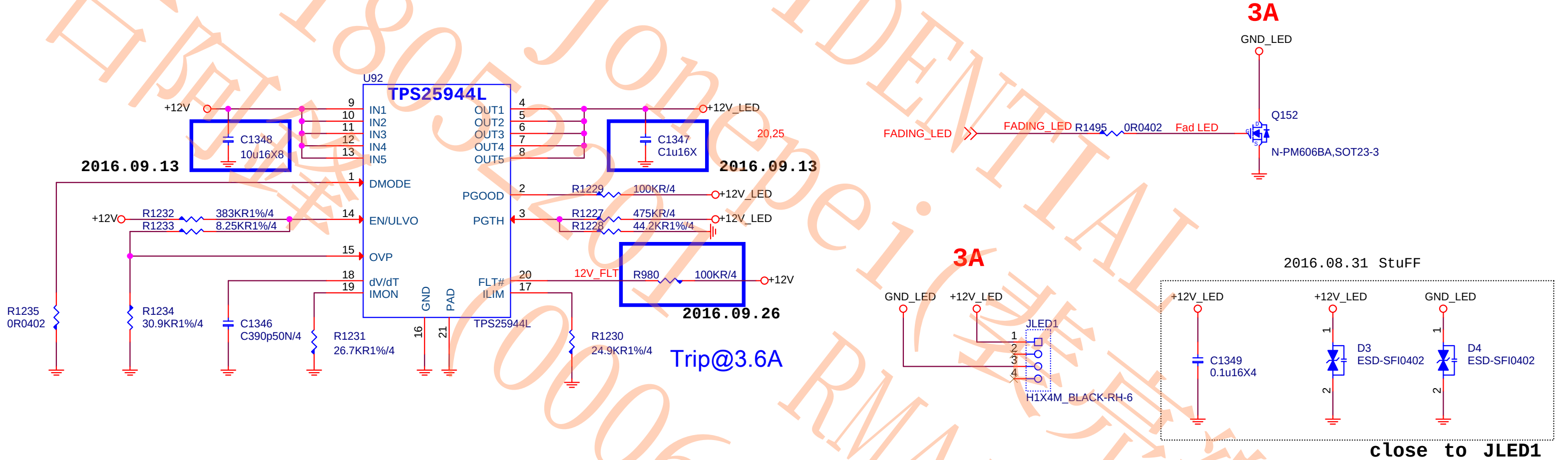
EZ Debug LED



GPIO / LED	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

JLED

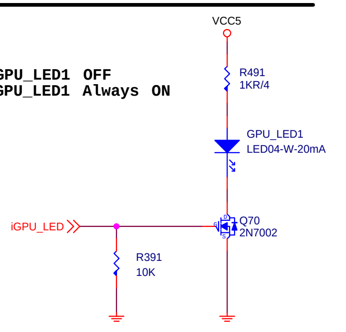


LED	x16	x8	x4
PCIE2	Red	White	White

GPIO / LED	EGPIO95	EGPIO96
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

AM4 APU Detect LED Circuit

iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON



Bottom LED

MICRO-START INT'L CO.,LTD.

Title	ALL LED Control
Size	Custom
Document Number	MS-7B38
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Date:	Wednesday, April 19, 2017
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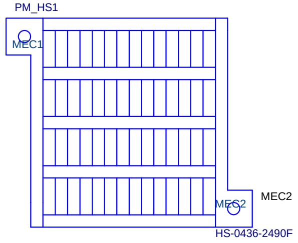
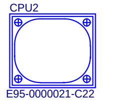
HEAT SINK

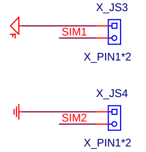


CPU Socket



RETENTION MODULE

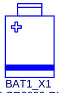
Simulation



MANUAL PART

UEFI1 G51-M1SPXXA-A09

MKT1 G51-M1SPL37-Q13



PCB1

7B07-0A

PK0-07A3610-G37, [illegible]

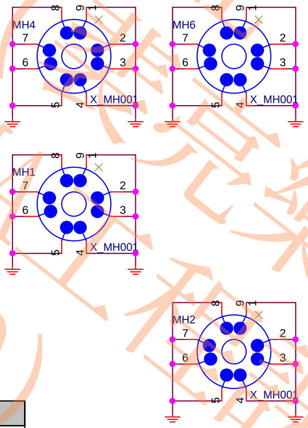
PK0-07A3610-E48, [illegible]

REF1 OPT X_FCH

REF2 OPT X_MKT

MOS HS(VCORE)

Optics Orientation Holes



5010

FM1 X_FM120 FM2 X_FM120 FM8 X_FM120

5020

FM3 X_FM120 FM4 X_FM120 FM7 X_FM120

FM5 X_FM120 FM6 X_FM120

OPT	Configure	BOM	Function
		601-7A36-A01	XXXX
		601-7A36-01S	MS-7A36 1.0 A320 A320M PRO-VD,A320,AM4,2DDR4,1PCI-Ex16,2PCI-Ex1,4SATA3,6USB3.1 Gen1,HD Audio,GB LAN,DVI-D,VGA
		601-7A36-010	MS-7A36 1.0 A320 A320M PRO-VD,A320,AM4,2DDR4,1PCI-Ex16,2PCI-Ex1,4SATA3,6USB3.1 Gen1,HD Audio,GB LAN,DVI-D,VGA

MSI MICRO-START INT'L CO.,LTD.

Title: BOM OPTION

Size: Custom | Document Number: MS-7B38 | Rev: 1.0

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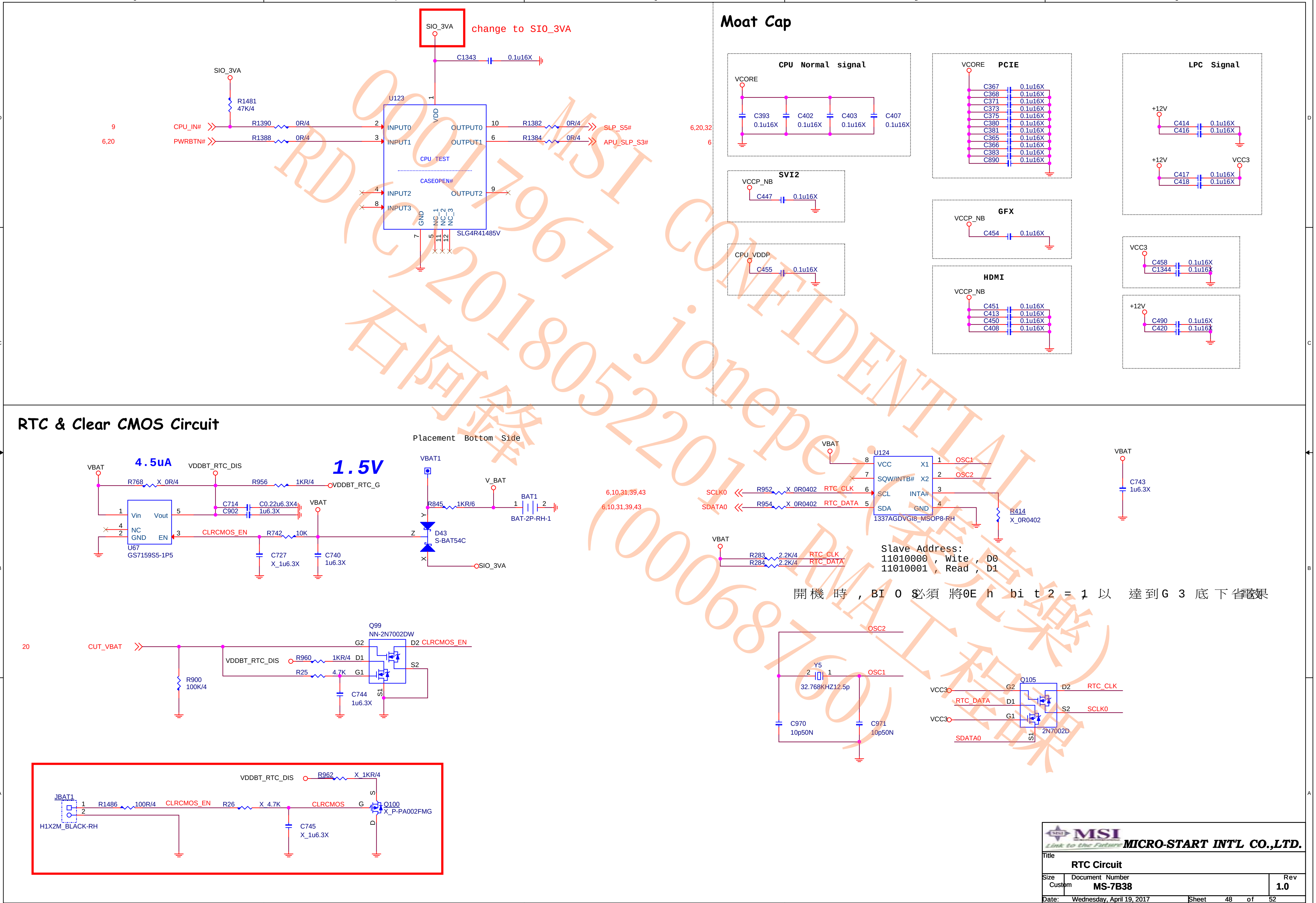
Moat Cap
CPU Normal signal
VCORE
C393 0.1u16X
C402 0.1u16X
C403 0.1u16X
C407 0.1u16X
SVI2
VCCP_NB
C447 0.1u16X
CPU_VDDP
C455 0.1u16X
PCIE
C367 C368 C371 C373 C375 C380 C381 C365 C366 C383 C890 0.1u16X
GFX
C454 0.1u16X
HDMI
C451 C413 C450 C408 0.1u16X
LPC Signal
+12V
C414 C416 0.1u16X
VCC3
C417 C418 0.1u16X
C458 C1344 0.1u16X
C490 C420 0.1u16X
SIO_3VA
change to SIO_3VA
C1343 0.1u16X
R1481 47K/4
U123
CPU_IN#
PWRBTN#
R1390 0R/4
R1388 0R/4
INPUT0 INPUT1 INPUT2 INPUT3
OUTPUT0 OUTPUT1 OUTPUT2
CPU TEST
CASEOPEN#
VDD GND NC_1 NC_2 NC_3
SLG4R41485V
R1382 0R/4
R1384 0R/4
SLP_S5#
APU_SLP_S3#
6,20,32
RTC & Clear CMOS Circuit
Placement Bottom Side
4.5uA
1.5V
VBAT
VDDBT_RTC_DIS
R768 X_0R/4
R956 1KR/4
VDDBT_RTC_G
Vin Vout NC GND EN
U67
GS7159S5-1P5
C714 C902
C0.22u6.3X4
1u6.3X
CLRCMOS_EN
R742 10K
C727 X_1u6.3X
C740 1u6.3X
VBAT1
V_BAT
R845 1KR/6
BAT1
BAT-2P-RH-1
D43 S-BAT54C
6,10,31,39,43
SCLK0
SDATA0
R952 X_0R0402
R954 X_0R0402
RTC_CLK
RTC_DATA
U124
VCC SQW/INTB# SCL SDA X1 X2 INTA# GND
OSC1 OSC2
1337AGDVGI8_MSOP8-RH
R414 X_0R0402
C743 1u6.3X
R283 2.2K/4
R284 2.2K/4
Slave Address:
11010000 , Wite , D0
11010001 , Read , D1
20
CUT_VBAT
Q99
NN-2N7002DW
R900 100K/4
R960 1KR/4
R25 4.7K
C744 1u6.3X
Y5
32.768KHZ12.5p
C970 10p50N
C971 10p50N
Q105
2N7002D
RTC_DATA
SDATA0
SCLK0
JBAT1
H1X2M_BLACK-RH
R1486 100R/4
R26 X_4.7K
CLRCMOS
R962 X_1KR/4
Q100
X_P-PA002FMG
C745 X_1u6.3X
MICRO-START INT'L CO.,LTD.
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