BSWD-LM V:1.0

ECS CONFIDENTIAL

SCHEMATICS TABLE:

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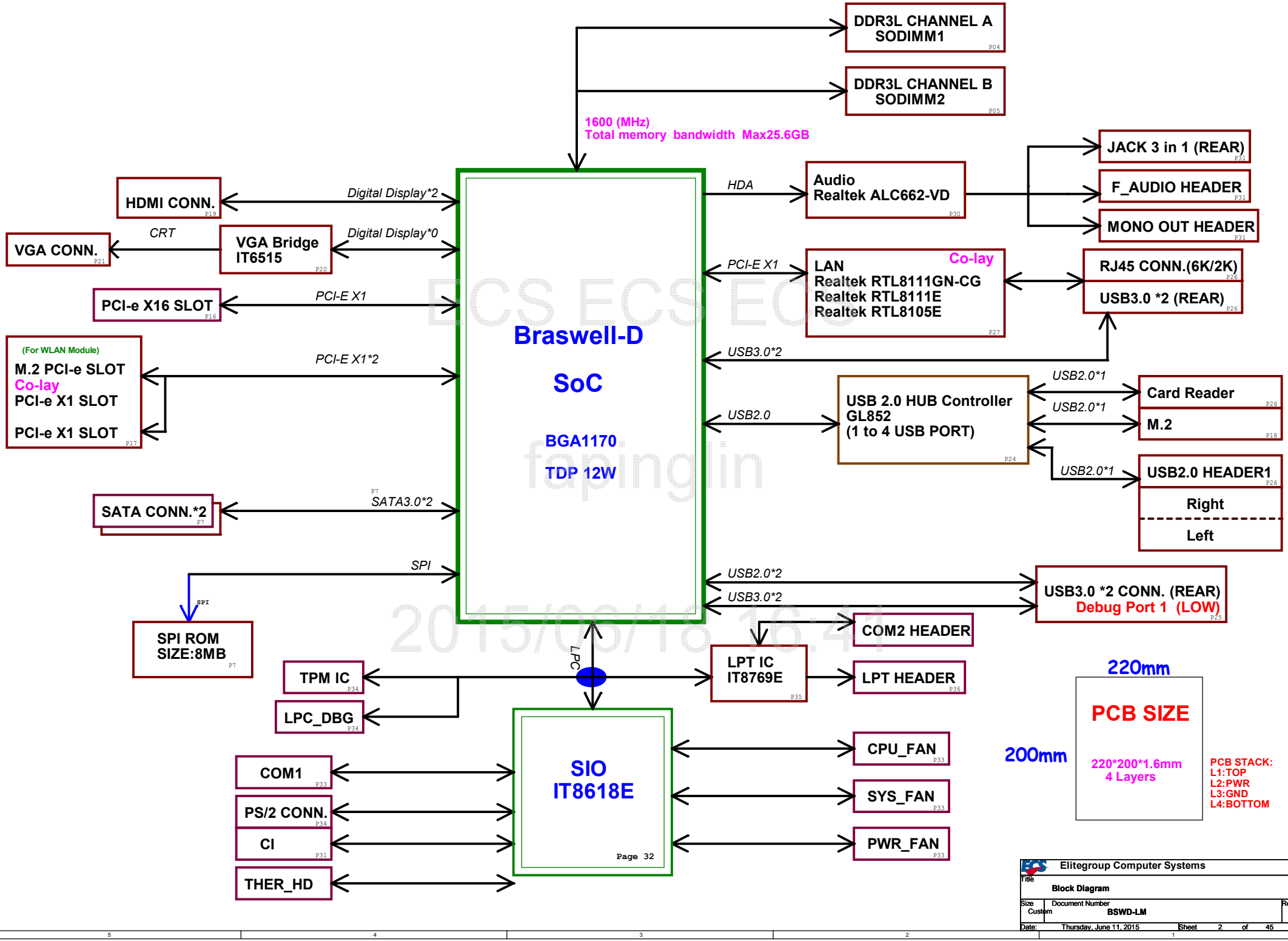
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220mm
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PCB SIZE
220*200*1.6mm
4 Layers
PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM
Elitegroup Computer Systems
Title
Block Diagram
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SoC-GPIO function

Data:2014/11/25

Pin Name	Power Well	Usage	Boot Set S0/S3/S4/S5 (BIOS Check)
DDI0_DDC_SDA	+1V8_S5	WLAN_DIS_L	OUTPUT(L/L/L/L)ACTIVE(H)
PANEL0_BKLTEN	+1V8_S5	SOC_USB_DET1	INPUT(H/H/H/H)ACTIVE(L)
PANEL0_BKLTCTL	+1V8_S5	SOC_USB_DET2	INPUT(H/H/H/H)ACTIVE(L)
PANEL0_VDDEN	+1V8_S5	HUB_RST N1	OUTPUT(L/L/L/L)ACTIVE(H)
PANEL1_BKLTEN	+1V8_S5	USB__EN N1,N2	OUTPUT(L/L/H/H,L=Enabled,H=Diabled)
PANEL1_BKLTCTL	+1V8_S5	GPIO_D17	OUTPUT(H/H/H/H)ACTIVE(L)-Reserve
PANEL1_VDDEN	+1V8_S5	GPIO_D18	INPUT(L=DEBUG CARD,H=COM)
PCIE_CLK0B	+1V8_S5	F_AUD_DET_L	INPUT(H/H/H/H)ACTIVE(L)
PCIE_CLK1B	+1V8_S5	TPM_DET	INPUT(L=No TPM,H=TPM)-Reserve
SATA_GP0	+1V8_S5	CLR_CMOS_SW	INPUT(H/H/H/H)ACTIVE(L)
SATA_GP1	+1V8_S5	TP_VGA	INPUT(H/H/H/H)ACTIVE(L)
SATA_GP2	+1V8_S5	GPIO_CASE0	INPUT(H/H/H/H)ACTIVE(L)
SATA_GP3	+1V8_S5	GPIO_CASE1	INPUT(H/H/H/H)ACTIVE(L)
GPIO_SUS2	+1V8_S5	SOC_PME_L	INPUT(H/H/H/H)ACTIVE(L)
GPIO_SUS3	+1V8_S5	SOC_RI_L	INPUT(H/H/H/H)ACTIVE(L)
GPIO_SUS5	+1V8_S5	ME_DIS_L	INPUT(H/H/H/H)ACTIVE(L)
GPIO_SUS11	+1V8_S5	F_FP_EN N1	OUTPUT(L/L/H/H,L=En,H=Dis)
GPIO_ALERT	+1V8_S5	SIO_BT_DIS_L N1	OUTPUT(L/L/L/L)ACTIVE(H)-Reserve
GPIO_SUS7	+1V8_S5	Reserve	INPUT
GPIO_SUS8	+1V8_S5	Reserve	INPUT
GPIO_SUS9	+1V8_S5	Reserve	INPUT
GPIO_SUS10	+1V8_S5	Reserve	INPUT

SIO-GPIO function---IT8618E

Data:2014/11/25

Pin Name	Power Well	Usage	Default SET	Boot Set S0/S3/S4/S5 (BIOS Check)
GP23	+F_USBPWR2	SIO_GPIO23_LED1	GPIO	OUTPUT(L/L 1HZ/H/H)
GP22(Reserve)	+F_USBPWR2	SIO_GPIO23_LED0	GPIO	OUTPUT(L/L 1HZ/H/H)
GP42(Reserve)	+V3P3A_PRIME	SIO_SMI_GPIO	GPIO	OUTPUT(L Active)
GP56	+3V3_S0	GPIO0_COM2_DET N1	GPIO	INPUT(H/L/L/L)ACTIVE(L)
GP57	+3V3_S0	GPIO1_LPTDET3	GPIO	INPUT(H/L/L/L)ACTIVE(L)

SIO-GPIO function---IT8769E

GP57	+3V3_S0	GPIO1_LPTDET3	GPIO	INPUT(S0 L Active)
GP56	+3V3_S0	GPIO0_COM2_DET	GPIO	INPUT(S0 L Active)

NOTE:

1、This GPIO control functions have the correspond items in BIOS setting interface!

2、This GPIO should be High in S4/S5 for power save!

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
PCIEX16	INTA#	Port 1	PCIEX16 slot
PCIEX1	INTD#	Port 2	1X SLOT
M2	INTC#	Port 3	WIFI
LAN	INTB#	Port 4	RTL8111GN-CG

USB OC Setting

Data:2014/11/25

Function	OC port	USB port	Device
USB2.0_OC	USB_OC0_B	USB4	F_USB1,F_USB2, USB HUB,
USB3.0_OC	USB_OC1_B	USB0,USB1,USB2,USB3	USB3_0,USB3_LAN

Elitegroup Computer Systems

Title: GPIO Function/INT# Mapping

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SoC-1 DDR3L

14 M_MA_A[0..15] M_MA_A[0..15]
14 M_DM_A[0..7] M_DM_A[0..7]
14 M_DATA_A[0..63] M_DATA_A[0..63]
14 M_DQS_A_P[0..7] M_DQS_A_P[0..7]
14 M_DQS_A_N[0..7] M_DQS_A_N[0..7]

CPU1A BSW_MCP_EDS

M_MA_A15	BD49	DDR3_M0_MA_15			BG33	M_DATA_A63
M_MA_A14	BD47	DDR3_M0_MA_14	DDR0	DDR3_M0_DQ_63	BH28	M_DATA_A62
M_MA_A13	BF44	DDR3_M0_MA_13		DDR3_M0_DQ_62	BJ29	M_DATA_A61
M_MA_A12	BF48	DDR3_M0_MA_12		DDR3_M0_DQ_61	BG28	M_DATA_A60
M_MA_A11	BB49	DDR3_M0_MA_11		DDR3_M0_DQ_60	BG32	M_DATA_A59
M_MA_A10	BJ45	DDR3_M0_MA_10		DDR3_M0_DQ_59	BH34	M_DATA_A58
M_MA_A9	BE52	DDR3_M0_MA_9		DDR3_M0_DQ_58	BG29	M_DATA_A57
M_MA_A8	BD44	DDR3_M0_MA_8		DDR3_M0_DQ_57	BJ33	M_DATA_A56
M_MA_A7	BE46	DDR3_M0_MA_7		DDR3_M0_DQ_56		
M_MA_A6	BB46	DDR3_M0_MA_6			BD28	M_DATA_A55
M_MA_A5	BH48	DDR3_M0_MA_5		DDR3_M0_DQ_55	BF30	M_DATA_A54
M_MA_A4	BD42	DDR3_M0_MA_4		DDR3_M0_DQ_54	BA34	M_DATA_A53
M_MA_A3	BH47	DDR3_M0_MA_3		DDR3_M0_DQ_53	BD34	M_DATA_A52
M_MA_A2	BJ48	DDR3_M0_MA_2		DDR3_M0_DQ_52	BD30	M_DATA_A51
M_MA_A1	BC42	DDR3_M0_MA_1		DDR3_M0_DQ_51	BA32	M_DATA_A50
M_MA_A0	BB47	DDR3_M0_MA_0		DDR3_M0_DQ_50	BC34	M_DATA_A49
				DDR3_M0_DQ_49	BF34	M_DATA_A48
M_BS_A2	BF52	DDR3_M0_BS_2		DDR3_M0_DQ_48		
M_BS_A1	AY40	DDR3_M0_BS_1			AV32	M_DATA_A47
M_BS_A0	BH46	DDR3_M0_BS_0		DDR3_M0_DQ_47	AV34	M_DATA_A46
M_CASB_A	BG45			DDR3_M0_DQ_46	BD36	M_DATA_A45
M_RASB_A	BA40	DDR3_M0_CASB		DDR3_M0_DQ_45	BF36	M_DATA_A44
M_WEB_A	BH44	DDR3_M0_RASB		DDR3_M0_DQ_44	AU32	M_DATA_A43
M_CSB_A1	AU38	DDR3_M0_WEB		DDR3_M0_DQ_43	AU34	M_DATA_A42
M_CSB_A0	AY38	DDR3_M0_CSB_1		DDR3_M0_DQ_42	BA36	M_DATA_A41
		DDR3_M0_CSB_0		DDR3_M0_DQ_41	BC36	M_DATA_A40
M_CK_A1	BD38			DDR3_M0_DQ_40		
M_CKB_A1	BF38	DDR3_M0_CK_1			BH38	M_DATA_A39
M_CKE_A1	AY42	DDR3_M0_CKB_1		DDR3_M0_DQ_39	BH36	M_DATA_A38
		DDR3_M0_CKE_1		DDR3_M0_DQ_38	BJ41	M_DATA_A37
M_CK_A0	BD40			DDR3_M0_DQ_37	BH42	M_DATA_A36
M_CKB_A0	BF40	DDR3_M0_CK_0		DDR3_M0_DQ_36	BJ37	M_DATA_A35
M_CKE_A0	BB44	DDR3_M0_CKB_0		DDR3_M0_DQ_35	BG37	M_DATA_A34
		DDR3_M0_CKE_0		DDR3_M0_DQ_34	BG43	M_DATA_A33
	AT30			DDR3_M0_DQ_33	BG42	M_DATA_A32
	AU30	RSVD1		DDR3_M0_DQ_32		
		RSVD2			BB51	M_DATA_A31
M_ODT_0	AV36			DDR3_M0_DQ_31	AW53	M_DATA_A30
M_ODT_1	BA38	DDR3_M0_ODT_0		DDR3_M0_DQ_30	BC52	M_DATA_A29
		DDR3_M0_ODT_1		DDR3_M0_DQ_29	AW51	M_DATA_A28
	AT28			DDR3_M0_DQ_28	AV51	M_DATA_A27
	AU28	DDR3_M0_OCAVREF		DDR3_M0_DQ_27	BC53	M_DATA_A26
		DDR3_M0_ODQVREF		DDR3_M0_DQ_26	AV52	M_DATA_A25
M0_DRAM_RSTL	BA42			DDR3_M0_DQ_25	BD52	M_DATA_A24
DRAM_S4_PWRGD	AV28	DDR3_M0_DRAMRSTB		DDR3_M0_DQ_24		
		DDR3_DRAM_PWROK			AV42	M_DATA_A23
M0_RCOMP	BA28			DDR3_M0_DQ_23	AP41	M_DATA_A22
		DDR3_M0_RCOMPPD		DDR3_M0_DQ_22	AV41	M_DATA_A21
M_DM_A7	BH30			DDR3_M0_DQ_21	AT44	M_DATA_A20
M_DM_A6	BD32	DDR3_M0_DM_7		DDR3_M0_DQ_20	AP40	M_DATA_A19
M_DM_A5	AY36	DDR3_M0_DM_6		DDR3_M0_DQ_19	AT38	M_DATA_A18
M_DM_A4	BG41	DDR3_M0_DM_5		DDR3_M0_DQ_18	AP42	M_DATA_A17
M_DM_A3	BA53	DDR3_M0_DM_4		DDR3_M0_DQ_17	AT40	M_DATA_A16
M_DM_A2	AP44	DDR3_M0_DM_3		DDR3_M0_DQ_16		
M_DM_A1	AT48	DDR3_M0_DM_2			AV45	M_DATA_A15
M_DM_A0	AP52	DDR3_M0_DM_1		DDR3_M0_DQ_15	AY50	M_DATA_A14
		DDR3_M0_DM_0		DDR3_M0_DQ_14	AT50	M_DATA_A13
M_DQS_A_P7	BH32			DDR3_M0_DQ_13	AP47	M_DATA_A12
M_DQS_A_N7	BG31	DDR3_M0_DQS_7		DDR3_M0_DQ_12	AV50	M_DATA_A11
M_DQS_A_P6	BC30	DDR3_M0_DQSB_7		DDR3_M0_DQ_11	AY48	M_DATA_A10
M_DQS_A_N6	BC32	DDR3_M0_DQS_6		DDR3_M0_DQ_10	AT47	M_DATA_A9
M_DQS_A_P5	AT32	DDR3_M0_DQSB_6		DDR3_M0_DQ_9	AP48	M_DATA_A8
M_DQS_A_N5	AT34	DDR3_M0_DQS_5		DDR3_M0_DQ_8		
M_DQS_A_P4	BH40	DDR3_M0_DQSB_5			AP51	M_DATA_A7
M_DQS_A_N4	BG39	DDR3_M0_DQS_4		DDR3_M0_DQ_7	AR53	M_DATA_A6
M_DQS_A_P3	AY52	DDR3_M0_DQSB_4		DDR3_M0_DQ_6	AK52	M_DATA_A5
M_DQS_A_N3	BA51	DDR3_M0_DQS_3		DDR3_M0_DQ_5	AL53	M_DATA_A4
M_DQS_A_P2	AT42	DDR3_M0_DQSB_3		DDR3_M0_DQ_4	AR51	M_DATA_A3
M_DQS_A_N2	AT41	DDR3_M0_DQS_2		DDR3_M0_DQ_3	AT52	M_DATA_A2
M_DQS_A_P1	AV47	DDR3_M0_DQSB_2		DDR3_M0_DQ_2	AL51	M_DATA_A1
M_DQS_A_N1	AV48	DDR3_M0_DQS_1		DDR3_M0_DQ_1	AK51	M_DATA_A0
M_DQS_A_P0	AM52	DDR3_M0_DQSB_1		DDR3_M0_DQ_0		
M_DQS_A_N0	AM51	DDR3_M0_DQS_0				
		DDR3_M0_DQSB_0				

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DRAM_S4_PWROK

36 VDDQ_PWRGD — R349 0-04 — DRAM_S4_PWRGD

+1V35_MEM — R348 10K-04

C387 .1U-16VX7-04-O

C388 .1U-16VX7-04-O

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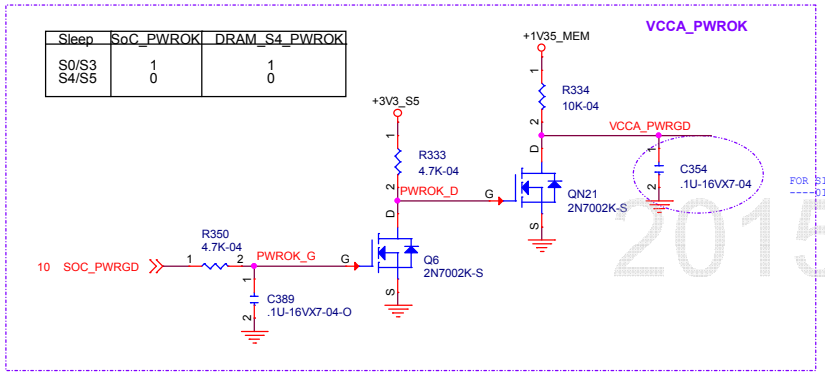
SoC-2 DDR3L

15 M_MA_B[0..15] — M_MA_B[0..15]
15 M_DM_B[0..7] — M_DM_B[0..7]
15 M_DATA_B[0..63] — M_DATA_B[0..63]
15 M_DQS_B_P[0..7] — M_DQS_B_P[0..7]
15 M_DQS_B_N[0..7] — M_DQS_B_N[0..7]



CPU1B — BSW_MCP_EDS — DDR1

M_MA_B15	BD5	DDR3_M1_MA_15	DDR3_M1_DQ_63	BG21	M_DATA_B63
M_MA_B14	BD7	DDR3_M1_MA_14	DDR3_M1_DQ_62	BH26	M_DATA_B62
M_MA_B13	BF10	DDR3_M1_MA_13	DDR3_M1_DQ_61	BJ25	M_DATA_B61
M_MA_B12	BF6	DDR3_M1_MA_12	DDR3_M1_DQ_60	BG26	M_DATA_B60
M_MA_B11	BB5	DDR3_M1_MA_11	DDR3_M1_DQ_59	BG22	M_DATA_B59
M_MA_B10	BJ9	DDR3_M1_MA_10	DDR3_M1_DQ_58	BH20	M_DATA_B58
M_MA_B9	BE2	DDR3_M1_MA_9	DDR3_M1_DQ_57	BG25	M_DATA_B57
M_MA_B8	BD10	DDR3_M1_MA_8	DDR3_M1_DQ_56	BJ21	M_DATA_B56
M_MA_B7	BE8	DDR3_M1_MA_7			
M_MA_B6	BB8	DDR3_M1_MA_6	DDR3_M1_DQ_55	BD26	M_DATA_B55
M_MA_B5	BH6	DDR3_M1_MA_5	DDR3_M1_DQ_54	BF24	M_DATA_B54
M_MA_B4	BD12	DDR3_M1_MA_4	DDR3_M1_DQ_53	BA20	M_DATA_B53
M_MA_B3	BH7	DDR3_M1_MA_3	DDR3_M1_DQ_52	BD20	M_DATA_B52
M_MA_B2	BJ6	DDR3_M1_MA_2	DDR3_M1_DQ_51	BD24	M_DATA_B51
M_MA_B1	BC12	DDR3_M1_MA_1	DDR3_M1_DQ_50	BA22	M_DATA_B50
M_MA_B0	BB7	DDR3_M1_MA_0	DDR3_M1_DQ_49	BC20	M_DATA_B49
			DDR3_M1_DQ_48	BF20	M_DATA_B48
M_BS_B2	BF2	DDR3_M1_BS_2			
M_BS_B1	AY14	DDR3_M1_BS_1	DDR3_M1_DQ_47	AV22	M_DATA_B47
M_BS_B0	BH8	DDR3_M1_BS_0	DDR3_M1_DQ_46	AV20	M_DATA_B46
			DDR3_M1_DQ_45	BD18	M_DATA_B45
M_CASB_B	BG9	DDR3_M1_CASB	DDR3_M1_DQ_44	BF18	M_DATA_B44
M_RASB_B	BA14	DDR3_M1_RASB	DDR3_M1_DQ_43	AU22	M_DATA_B43
M_WEB_B	BH10	DDR3_M1_WEB	DDR3_M1_DQ_42	AU20	M_DATA_B42
M_CSB_B1	AU16	DDR3_M1_CSB_1	DDR3_M1_DQ_41	BA18	M_DATA_B41
M_CSB_B0	AY16	DDR3_M1_CSB_0	DDR3_M1_DQ_40	BC18	M_DATA_B40
M_CK_B1	BD16	DDR3_M1_CK_1			
M_CKB_B1	BF16	DDR3_M1_CKB_1	DDR3_M1_DQ_39	BH16	M_DATA_B39
M_CKE_B1	AY12	DDR3_M1_CKE_1	DDR3_M1_DQ_38	BH18	M_DATA_B38
			DDR3_M1_DQ_37	BJ13	M_DATA_B37
M_CK_B0	BD14	DDR3_M1_CK_0	DDR3_M1_DQ_36	BH12	M_DATA_B36
M_CKB_B0	BF14	DDR3_M1_CKB_0	DDR3_M1_DQ_35	BJ17	M_DATA_B35
M_CKE_B0	BB10	DDR3_M1_CKE_0	DDR3_M1_DQ_34	BG17	M_DATA_B34
			DDR3_M1_DQ_33	BG11	M_DATA_B33
	AT24		DDR3_M1_DQ_32	BG12	M_DATA_B32
	AU24	RSVD1			
		RSVD2			
M1_ODT_0	AV18	DDR3_M1_ODT_0	DDR3_M1_DQ_31	BB3	M_DATA_B31
M1_ODT_1	BA16	DDR3_M1_ODT_1	DDR3_M1_DQ_30	AW1	M_DATA_B30
			DDR3_M1_DQ_29	BC2	M_DATA_B29
	AT26		DDR3_M1_DQ_28	AW3	M_DATA_B28
	AU26	DDR3_M1_OCAVREF	DDR3_M1_DQ_27	AV3	M_DATA_B27
		DDR3_M1_ODQVREF	DDR3_M1_DQ_26	BC1	M_DATA_B26
M1_DRAM_RSTL	BA12		DDR3_M1_DQ_25	AV2	M_DATA_B25
VCCA_PWRGD	AV26	DDR3_M1_DRAMRSTB	DDR3_M1_DQ_24	BD2	M_DATA_B24
		DDR3_VCCA_PWROK			
M1_RCOMP	BA26				
		DDR3_M1_RCOMPPD	DDR3_M1_DQ_23	AV12	M_DATA_B23
M_DM_B7	BH24	DDR3_M1_DM_7	DDR3_M1_DQ_22	AP13	M_DATA_B22
M_DM_B6	BD22	DDR3_M1_DM_6	DDR3_M1_DQ_21	AV13	M_DATA_B21
M_DM_B5	AY18	DDR3_M1_DM_5	DDR3_M1_DQ_20	AT10	M_DATA_B20
M_DM_B4	BG13	DDR3_M1_DM_4	DDR3_M1_DQ_19	AP14	M_DATA_B19
M_DM_B3	BA1	DDR3_M1_DM_3	DDR3_M1_DQ_18	AT16	M_DATA_B18
M_DM_B2	AP10	DDR3_M1_DM_2	DDR3_M1_DQ_17	AP12	M_DATA_B17
M_DM_B1	AT6	DDR3_M1_DM_1	DDR3_M1_DQ_16	AT14	M_DATA_B16
M_DM_B0	AP2	DDR3_M1_DM_0			
			DDR3_M1_DQ_15	AV9	M_DATA_B15
M_DQS_B_P7	BH22		DDR3_M1_DQ_14	AY4	M_DATA_B14
M_DQS_B_N7	BG23	DDR3_M1_DQS_7	DDR3_M1_DQ_13	AT4	M_DATA_B13
M_DQS_B_P6	BC24	DDR3_M1_DQSB_7	DDR3_M1_DQ_12	AP7	M_DATA_B12
M_DQS_B_N6	BC22	DDR3_M1_DQS_6	DDR3_M1_DQ_11	AV4	M_DATA_B11
M_DQS_B_P5	AT22	DDR3_M1_DQSB_6	DDR3_M1_DQ_10	AY6	M_DATA_B10
M_DQS_B_N5	AT20	DDR3_M1_DQS_5	DDR3_M1_DQ_9	AT7	M_DATA_B9
M_DQS_B_P4	BH14	DDR3_M1_DQSB_5	DDR3_M1_DQ_8	AP6	M_DATA_B8
M_DQS_B_N4	BG15	DDR3_M1_DQS_4			
M_DQS_B_P3	AY2	DDR3_M1_DQSB_4	DDR3_M1_DQ_7	AP3	M_DATA_B7
M_DQS_B_N3	BA3	DDR3_M1_DQS_3	DDR3_M1_DQ_6	AR1	M_DATA_B6
M_DQS_B_P2	AT12	DDR3_M1_DQSB_3	DDR3_M1_DQ_5	AK2	M_DATA_B5
M_DQS_B_N2	AT13	DDR3_M1_DQS_2	DDR3_M1_DQ_4	AL1	M_DATA_B4
M_DQS_B_P1	AV7	DDR3_M1_DQSB_2	DDR3_M1_DQ_3	AR3	M_DATA_B3
M_DQS_B_N1	AV6	DDR3_M1_DQS_1	DDR3_M1_DQ_2	AT2	M_DATA_B2
M_DQS_B_P0	AM2	DDR3_M1_DQSB_1	DDR3_M1_DQ_1	AL3	M_DATA_B1
M_DQS_B_N0	AM3	DDR3_M1_DQS_0	DDR3_M1_DQ_0	AK3	M_DATA_B0
		DDR3_M1_DQSB_0			

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Elitegroup Computer Systems			
Title: SOC-DDR3L_CHB			
Size: Custom	Document Number: BSWD-LM		Rev: V1.0
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SOC-3 DISPLAY

SoC Display Configuration

Feature	eDP*	DP	HDMI/DVI
Number of Ports	2 (DDI[0:1]) (2x4 @2.7 Gb/s)	3 (DDI[0:2]) (2x4 @2.7 Gb/s)	3 (DDI[0:2]) (2x4 @1.65 Gb/s)
Maximum Resolution	3840x2160 @ 30Hz 2560x1600 @ 60Hz 24bpp	3840x2160 @ 30Hz 2560x1600 @ 60Hz 24bpp	3840x2160 @ 30Hz 2560x1600 @ 60Hz 24bpp
Minimum Resolution	none	none	480i/576i
Data Rate	10.8Gb/s	10.8Gb/s	6.6 Gb/s
Standard	DP1.1a/eDP1.4	DP1.1a	HDMI1.4b
Power gated during display off	Yes	Yes	Yes
DRRS (Refresh reduction)	Yes (Panel command)	N/A	N/A
Self-Refresh with Frame buffer in Panel	No	No	No
Content-Based backlight control	DPST6/CABC	N/A	N/A
HDCP wired display	N/A(ASSR support)	1.4	1.4
PAVP	AES-encrypted buffer, plane control, panic attack		
SEC	All display registers can be accessed by CEC		
HD-Audio	N/A	Yes	Yes
LPE Audio	N/A	No	No
Compressed Audio	N/A	Yes	Yes

VGA Bridge

HDMI

CPU1C — BSW_MCP_EDS

3 OF 13

.VSDIO Voltage Setting

SDMMC3_PWR_EN_B	SDMMC3_1P8_EN	VSDIO(V)
1	0	0
1	1	0
0	0	3.3
0	1	1.8

IF use SDIO function,SoC Power net should be controled by Pin K2,L3 to choose different power supply

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port	How to Disable Port
DDI0	GPIO_SUS0	Pull-up to V1P8A with 4.7-KΩ ±5% resistor	N/A, Weak internal pull-down
DDI1	GPIO_SUS1	Pull-up to V1P8A with 4.7-KΩ ±5% resistor	N/A, Weak internal pull-down
Note: DDI2 is always enabled an no Hard Strap is needed.			

Digital Display Interface Supported

Port	Supported
DDI0	HDMI, DP, or eDP*
DDI1	HDMI, DP, or eDP*
DDI2	HDMI or DP
Notes: Up to two HDMI can be supported at the same time.	

Elitegroup Computer Systems

Title: SOC-3 DISPLAY

Size: C | Document Number: BSWD-LM | Rev: V1.0

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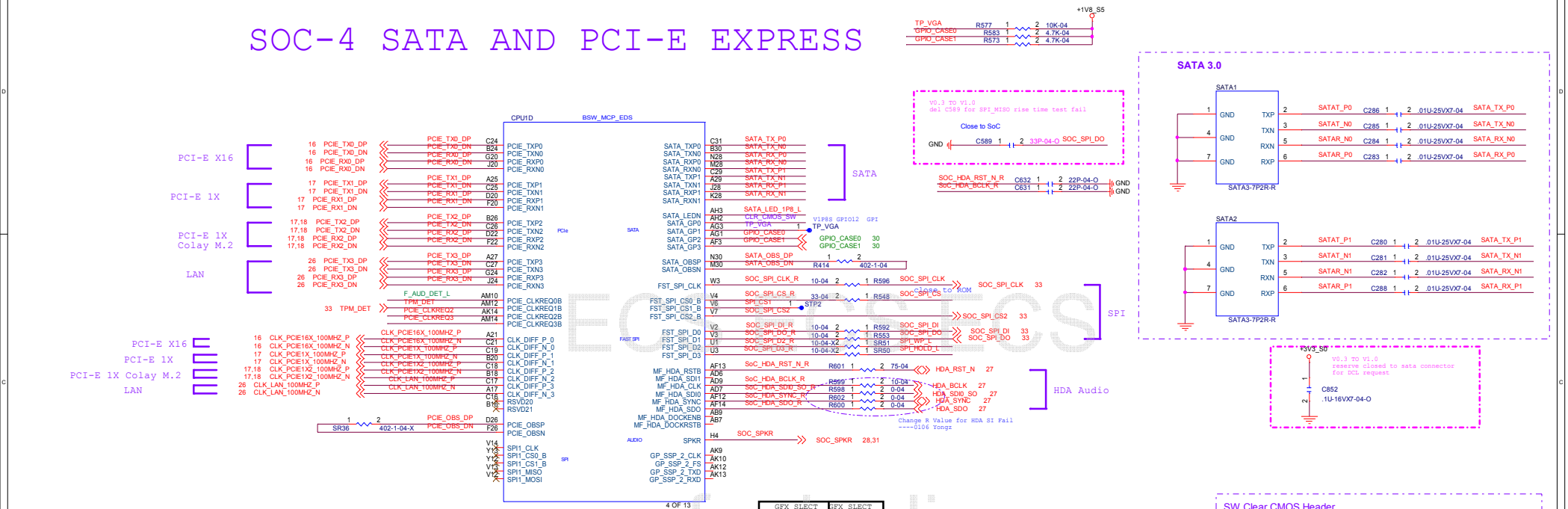
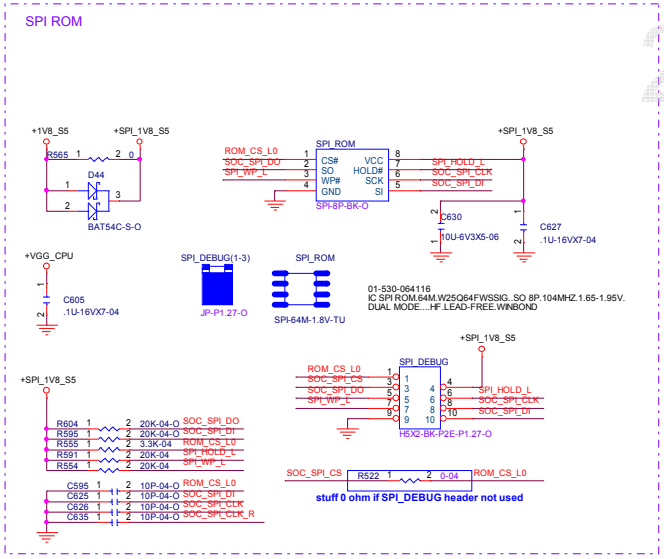
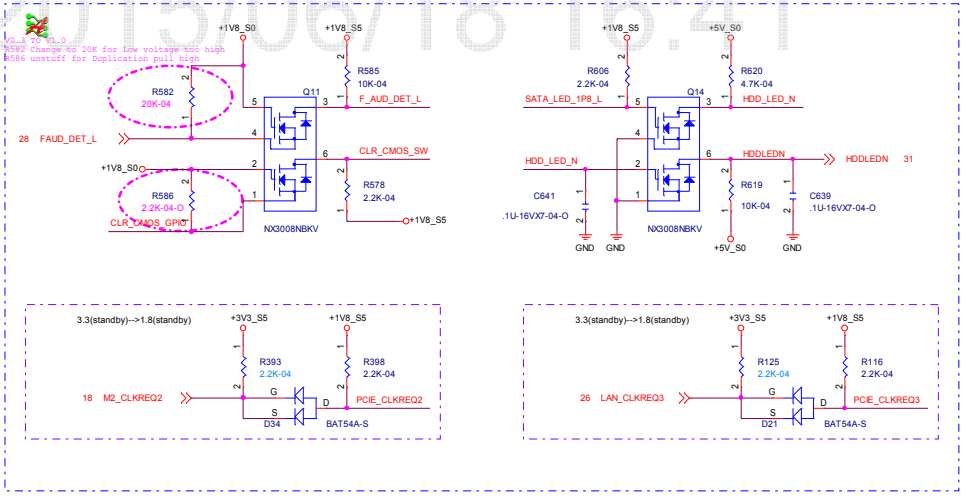
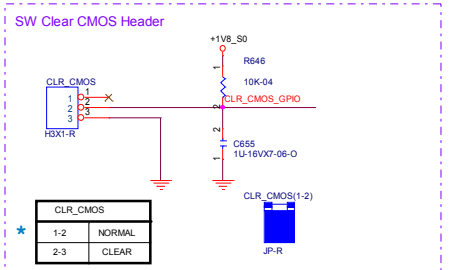
SOC-4 SATA AND PCI-E EXPRESS



- If no PCI Express* ports is implemented on the platform:
  - — PCIE_TXp/n [3:0] and PCIE_RXp/n [3:0] may be left unconnected.
  - — Pull-up PMC_WAKE_PCIE[3:0]# to V1P8 by means of a 10-KΩ resistor.
  - — PCI_CLKREQ[3:0]# can be let open.







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Title	SOC-4 SATA AND PCI-E/ SPI
Size C	Document Number BSWD-LM
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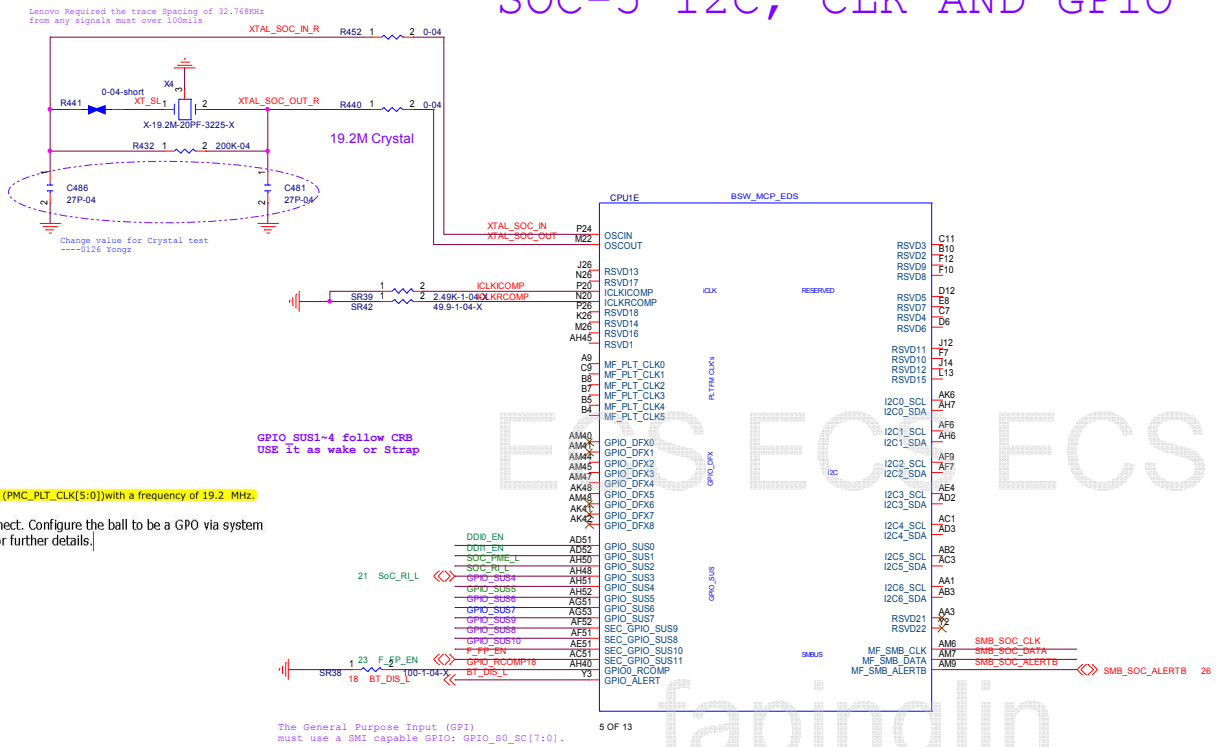
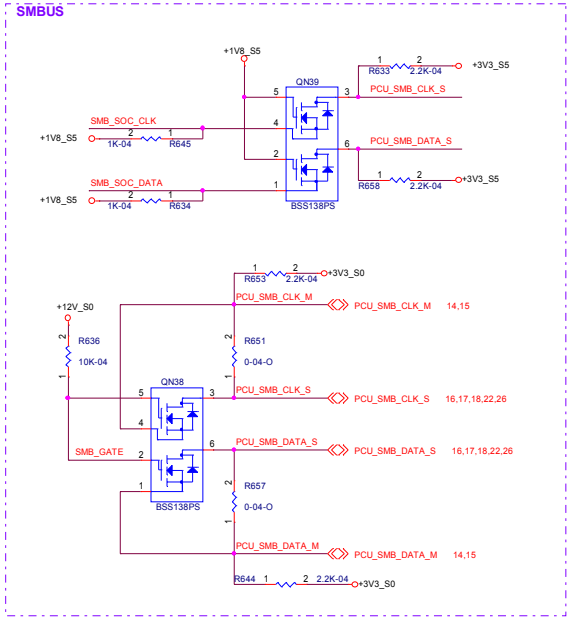
SOC-5 I2C, CLK AND GPIO

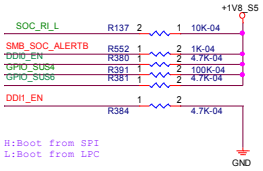


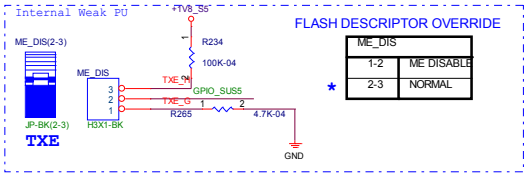


13.1.2 Platform Clocks

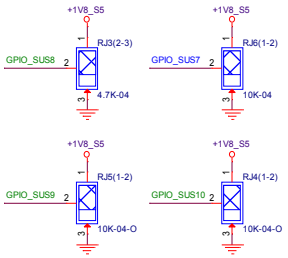
The SoC supports up to 6 clocks (PMC_PLT_CLK[5:0])with a frequency of 19.2 MHz.

Each signal may be left as a No Connect. Configure the ball to be a GPO via system BIOS. See the BIOS Writers Guide for further details.





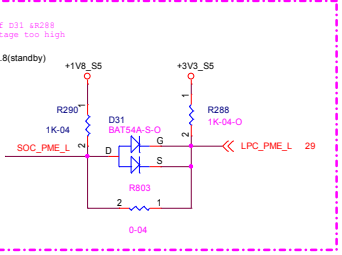
GPIO_SUS4/6/7/8/9/10 For BIOS Reerve



CHV Straps [CRB] -- strap detect @ RSMRST# assertion

Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1 - DDI0 Detect, 0 - Disable	High
DDI1 Detected	GPIO_SUS1	PD	1 - DDI1 Detect, 0 - Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1 - Boot from SPI, 0 - Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0 - Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0 - Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select-	SEC_GPIO_SUS8	PU	1 - 1.35V, 0 - 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1 - Bypass with 1.05V, 0 - No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1 - PMC, 0 - Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1 - Bypass, 0 - No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1 - Bypass, 0 - No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1 - Bypass, 0 - No bypass	Low

Note:SEC_GPIO_SUS8
This strap also contains PLL LDO
0: supply is 1.25V; 1: supply is 1.35V.
Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI



Elitegroup Computer Systems

Title	SOC-5 I2C, CLK AND GPIO,NFC	
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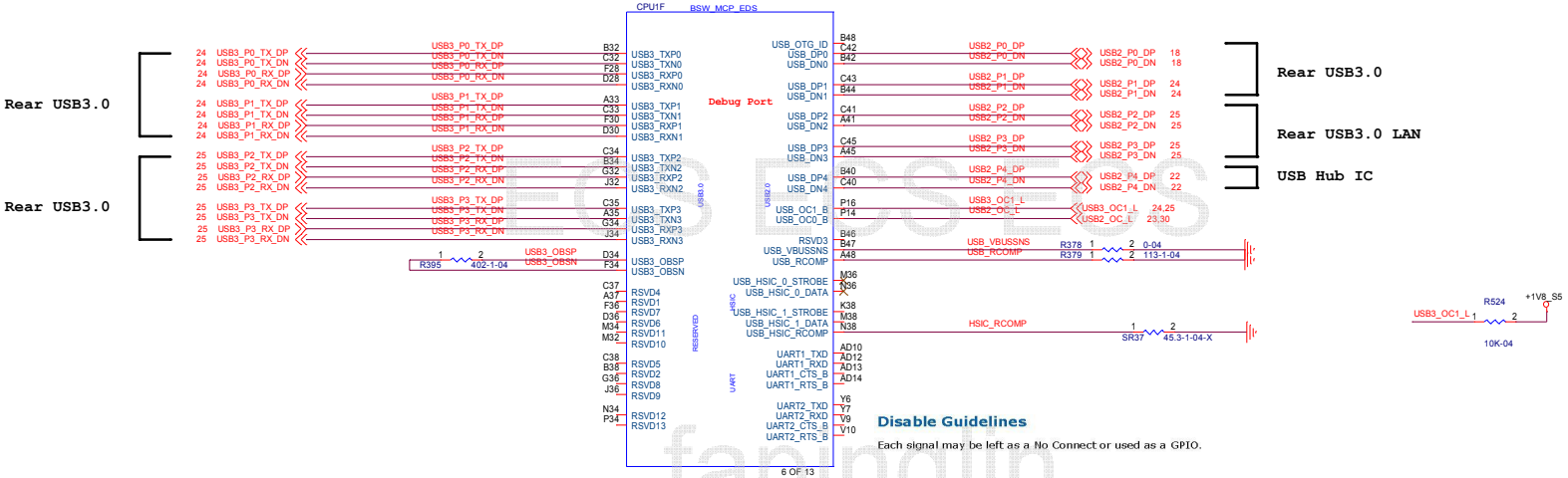
SOC-6 USB/UART



Elitegroup Computer Systems			
Title: SOC-6 USB/UART			
Size: C	Document Number: BSWD-LM		Rev: V1.0
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SOC-7 RTC, PWM, PMU AND SVID

Note: Customers can set this clock to 19 MHz or 25 MHz

CAD NOTE:
PAD SHARING PLACE THEM NEAR EC

Close to SoC

29 SIO_25MHZ
32 LPT_25MHZ
33 TPM_25MHZ
33 LPC_25MHZ

SR43 22-04-X
SR329 22-04
R665 0-04-O
R744 0-04

For The Best wave rise time
----0108 Yongz

PLACE HOLDER FOR DIE#2

Add PU for CX_PREQ_B to follow CRB
----0108 Yongz

+1V8_S5 R717 51-04 PREQ_B
SR44 10K-04-X-S PCM_SOC

CPU1G BSW_MCP_EDS

JTAG/ITP: TCK, TDI, TDO, TMS, TRST_B
CX_PRDY_B, CX_PREQ_B, RSVD5
LPC_CLK0_25MHZ, LPC_CLK1_25MHZ, LPC_CLKRUN, LPC_FRAMEB
MF_LPC_CLKOUT0, MF_LPC_CLKOUT1, LPC_CLKRUNB, LPC_FRAMEB
MF_LPC_AD0, MF_LPC_AD1, MF_LPC_AD2, MF_LPC_AD3
LPC_HVT_RCOMP, ILB_SERIRQ
RSVD23, RSVD24
RSVD8, RSVD7, RSVD4, RSVD3, RSVD1, RSVD2, PROCHOT_B
RTC: BRTCX1_PAD, BRTCX2_PAD, BVCCRTC_EXTPAD, SRTCRST_B, COREPWROK, RSMRST_B, RTEST_B, RSVD_VSS
PMU: SUSPWRDNACK, SUS_STAT_B, PMU_SUSCLK, PMU_SLP_S4_B, PMU_SLP_S3_B, PMU_RESETBUTTON_B, PMU_PLTRST_B, PMU_BATLOW_B, PMU_AC_PRESENT, PMU_SLP_S0IX_B, PMU_SLP_LAN_B, PMU_WAKE_B, PMU_PWRBTN_B, PMU_WAKE_LAN_B
SVID: SVID0_CLK, SVID0_DATA, SVID0_ALERT_B
Voltage sense: CORE_VCC0_SENSE, CORE_VSS0_SENSE, CORE_VCC1_SENSE, CORE_VSS1_SENSE, DDI_VGG_SENSE, UNCORE_VSS_SENSE2, UNCORE_VSS_SENSE1
Reserved

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BRTCX1, BRTCX2, BVCCRTC_EXTPAD
C502 0.1U-16VX7-04
SRTCRST_N
SOC_PWRGD 5
SOC_RSMRST_L
RTC_TEST_L
SOC_INTRUDER R435 10K-04 GND
SOC_SUSPWRDANCK 1 TP8
SUS_STAT_L
SOC_SUSCLK 1 TP3
SOC_SLP4_L
SOC_SLP3_L
FP_RST_L 31
SOC_PLTRST_L 33
SOC_BATLOW
SOC_ACPRESENT
PCIE_WAKE_N
SOC_PWRON_L
VCC_SVID_CLK 37
VCC_SVID_DATA 37
VCC_SVID_ALERT_N 37

RTC 32.768KHz

Lenovo Required the trace Spacing of 32.768KHz from any signals must over 100mils

BRTCX1
BRTCX2
R401 10M-04
GND
X3
JP-WI-P6.25
07-141-327624
R397 0-04-short
RTCT_L
X-32.768K-5m12.5D
C448 15P-04
C450 15P-04

11/06 V0.2 Eason change to 18P-04 for 32.768KHz crystal test Fail

Change value for RTC test
----0126 Yongz

LPC_CLK0_25MHZ
LPC_CLK1_25MHZ
C570 10P-04-O
C575 10P-04-O
GND GND

29,32,33 SOC_LFRAME_L
TP7
29,32,33 SOC_LAD0
29,32,33 SOC_LAD1
29,32,33 SOC_LAD2
29,32,33 SOC_LAD3
SERIRQ_1P8
SR48 100-1-04-X
LPC_RCOMP
R570 75-04
C603 30P-04-O
29 SERIRQ_1P8

CPU_PROCHOT_N
+1V05_S5 R309 20K-04-O
+1V8_S5 R310 20K-04-O
37 VCC0_VR_HOT_N
38 VGG_VR_HOT_N
30 THER_HOT_N
R313 0-04
R312 0-04
R306 0-04-O
CPU_PRO R311 0-04

AD42 VCC_SVID_CLK
AD41 VCC_SVID_DATA
AD40 VCC_SVID_ALERT_N
AG32 VCC0_SENSEP_R
AJ32 VCC0_SENSEN_R
AD29 VCC1_SENSEP_R
AF27 VCC1_SENSEN_R
AD24 VGG_SENSEP_R
AD22 VGG_SENSEN_R
AC27 VNN_REFIN_R
STP1

TP2D2
R346 100-1-04 VCC0_SENSEP
R331 100-1-04 VCC0_SENSEN
TP2D1
R343 100-1-04 VCC0_SENSEP
TP2C2
R340 100-1-04 VCC0_SENSEN
TP2C1
R529 0-04 VGG_SENSEP
TP4C1
R531 0-04 VGG_SENSEN
TP4C2

VCC0_SENSEP 37
VCC0_SENSEN 37
VCC0_SENSEN 37
VGG_SENSEP 38
VGG_SENSEN 38

CAD NOTE:
ROUTE THESE AS DIFFERENTIAL LINES

8/16 V0.3 to V0.3A for SERIRQ fail lead to hang 69 issue

U41 NTB0101GMS
VCCA GND A VCB OE B
C644 .1U-16VX7-04
C647 .1U-16VX7-04
+1V8_S5 +3V3_S0 +1V8_S0
SERIRQ_1P8 LPC_EN GND LPC_SERIRQ
R647 0-04
R632 1K-04-O
R617 2.2K-04-O
R631 2.2K-04-O
R622 0-04-O
LPC_SERIRQ 29,32,33

8/16 V0.3 to V0.3A for SERIRQ fail lead to hang 69 issue

Sleep	SoC_PLTRST_L	PLTRST_L
S0	1	1
S3/S4/S5	0	0

SOC_SLP4_L R485 2.2K-04-O SLP_S4
SLP_S3_R R505 8.2K-04-O +5V_S5
Q8 3904-DUAL-O
+5V_S5 R472 8.2K-04-O SLP_S4_R
SLP_S3 R478 2.2K-04-O SOC_SLP3_L

QN28 NX3008NBKV-O
R491 2.2K-04-O +3V3_S5
SLP_S4_R SLP_S4_L 10,24,29,36
R512 2.2K-04-O +3V3_S5
SLP_S3_R SLP_S3_L 10,29,34,38,40

SOC_SLP3_L R513 0-04 SLP_S3_L 10,29,34,38,40
SOC_SLP4_L R486 0-04 SLP_S4_L 10,24,29,36

+RTCVCC R492 20K-04 RTC_TEST_L
C527 1U-16VX7-06

8/16 V0.3 to V0.3A add R804 unstuff D40&R510 for PWRON low voltage too high

+3V3_S5 +1V8_S5
R510 2.2K-04-O
R496 2.2K-04
29 SIO_PWRON_L
SOC_PWRON_L
D40 BAT54A-S-O
R804 0-04

3.3(standby)-->1.8(standby)

+3V3_S5 +1V8_S5
R515 2.2K-04
R518 2.2K-04
16,17,18,21,26 PCIE_WAKE_N_R
PCIE_WAKE_N
D41 BAT54A-S

SOC_PLTRST_L R469 2.2K-04 PLT_RST_L
GND
SUS_STAT_R R438 8.2K-04-O +5V_S5
Q7 3904-DUAL
+5V_S5 8.2K-04 R453 PLT_RST_L_R
SUS_STAT R456 2.2K-04-O SUS_STAT_L

QN24 BSS138PS
PLT_RST_L_R
R431 2.2K-04 +3V3_S0 PLTRST_L PLTRST_L 29,32
R450 2.2K-04-O +3V3_S5 LPCPD_L LPCPD_L 33
SUS_STAT_R
GND

Change the diode location
----0106 Yongz

+RTCVCC
D27 BAT54C-S
+3V3_DSW
R164 1K-04
VBAT_R VBAT
BAT1 SK-CR2032-D
CR2032

+VBAT_IO
R536 0-04
C568 1U-16VX7-06-O
RTC_TEST_L
1N4148W-S-O D55
SRTCRST_N
R382 20K-04
C430 1U-16VX7-06

MRS:RTC-RST Jumper NA

MRS:RTC-RST Jumper NA
If need HW Clear CMOS must to connect +VBAT_IO

29 RSMRST_L
R543 0-04
SOC_RSMRST_L
R566 100K-04
C537 1U-16VX5-04-O

CORE_PWROK / RSMRST_N Platform Power is V3P3

V0.3 TO V1.0 add C498 for SOC-PWRGD Fall time fail

29 SIO_PWRGD3
R466 0-04
SOC_PWRGD
R457 100K-04
C498 1000P-16VX5-04

All RTC-well inputs (PMC_RSMRST#, ILB_RTC_RST#,PMC_CORE_PWROK,ILB_RTC_TEST#) must be either pulled up to RTC_VCC or pulled down to ground while in the G3 state.

Close to SoC

9/10 V0.3A to V1.0 Add C398 for SoC_PWRON ring up

SOC_PWRON_L C524 1000P-50VX7-04
FP_RST_L C612 .1U-16VX7-04

7/26 V0.2 to V0.3 SI for FP_RST_L has glitch.

+1V8_S5
SOC_ACPRESENT R468 10K-04
SOC_BATLOW R460 20K-04

Title	SOC-7 RTC, PWM, PMU AND SVID
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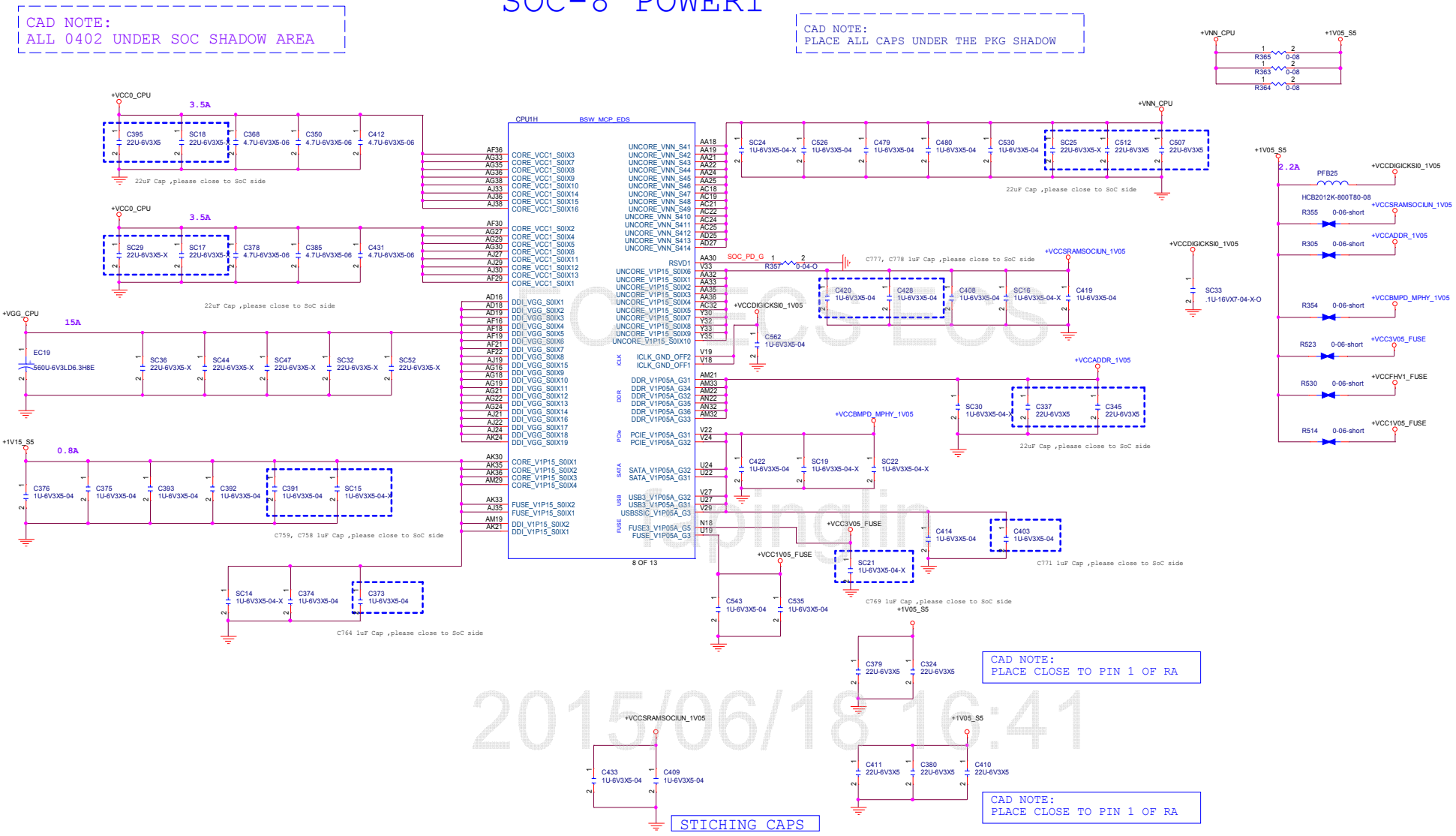
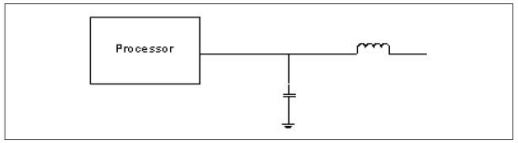


4.4.4 SoC High Frequency Decoupling Requirements

In addition to the low and mid frequency decoupling above, the SoC requires high frequency decoupling as shown.

Where inductors are included as part of the decoupling network, follow the example shown in figure below. From the SoC pin, the capacitor is seen first, followed by the series inductor. Inductor placeholders are stuffed with 0 Ω resistors.

Figure 47. Example LC Decoupling



Elitegroup Computer Systems			
Title: SOC-8 POWER1			
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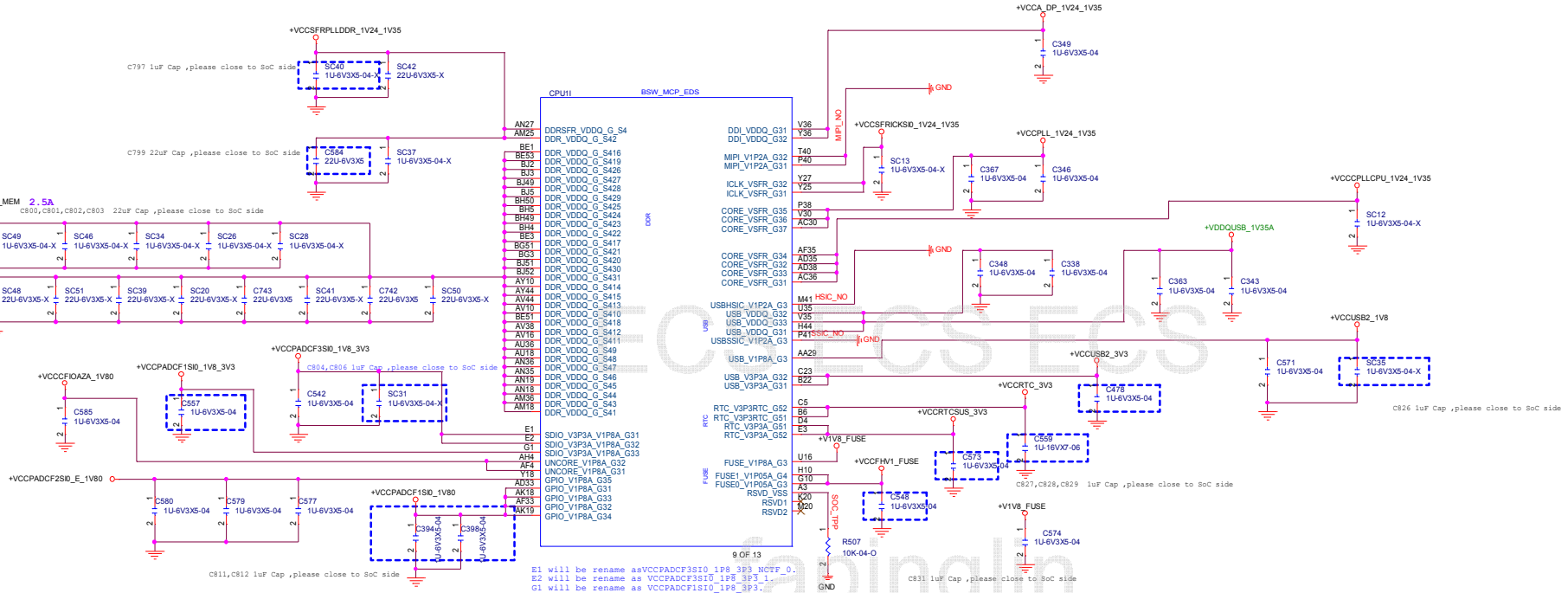
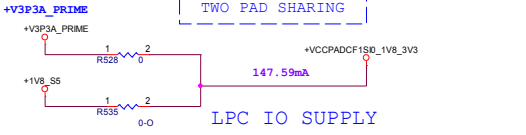
SOC-9 POWER2

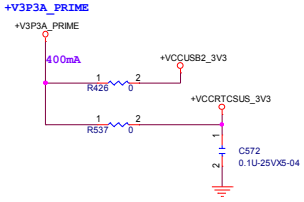
CAD NOTE:
PLACE THE CAPS UNDER THE PKG SHADOW



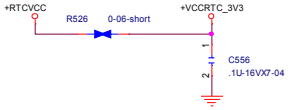
E1 will be rename asVCCPADCF3SI0_1P8_3P3_NCTF_0.
E2 will be rename as VCCPADCF3SI0_1P8_3P3_1.
G1 will be rename as VCCPADCF1SI0_1P8_3P3.
+VCCPADCF1SI0_1P8_3P3 is fixed at 3.3V.
+VCCPADCF3SI0_1P8_3P3 is switchable between 1.8V and 3.3, based on different speed mode.

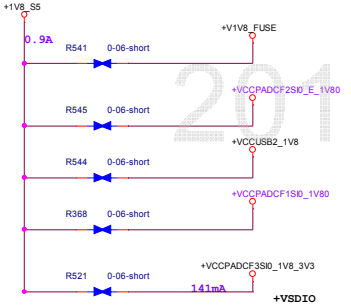
CAD NOTE:
TWO PAD SHARING

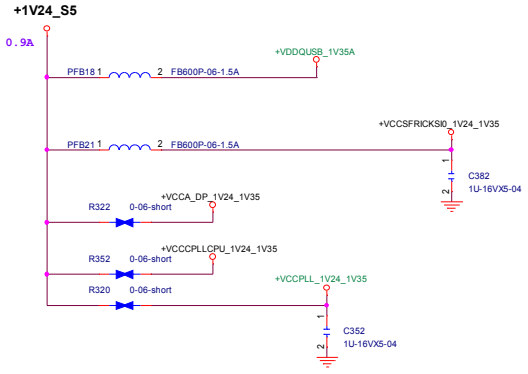


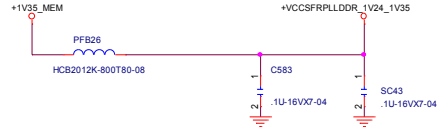


CAD NOTE:
CAPS PLACE NEAR SOC PIN









Elitegroup Computer Systems			
Title: SOC-9 POWER2			
Size: C	Document Number: BSWD-LM		Rev: V1.0
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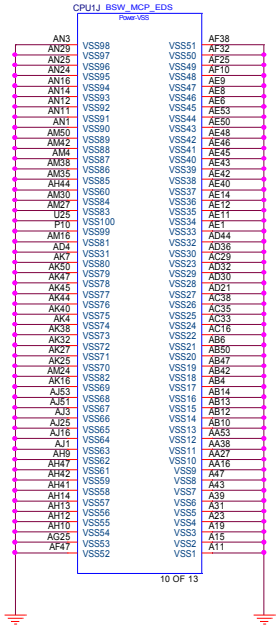
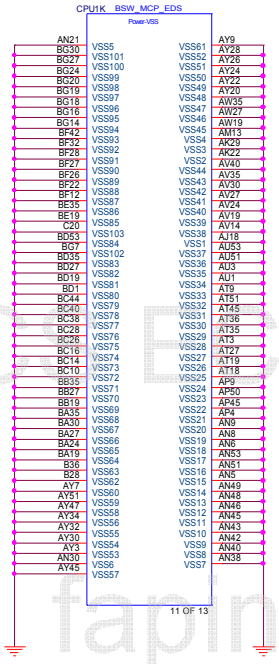
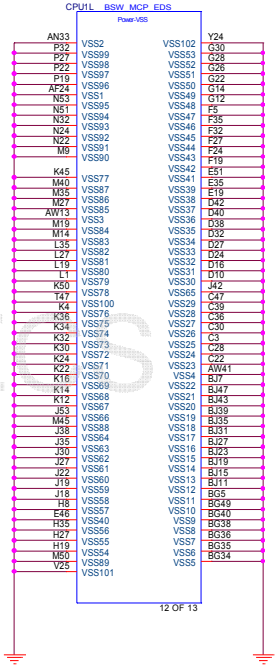
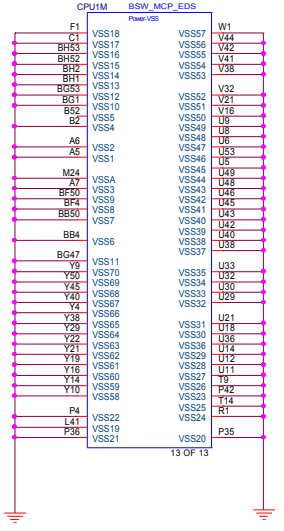
SOC-10 VSS

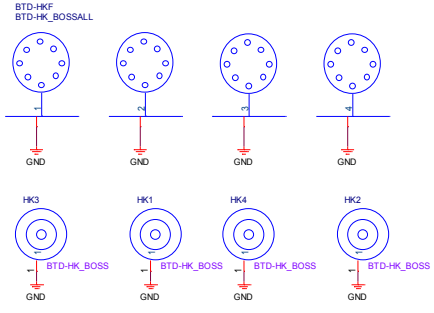




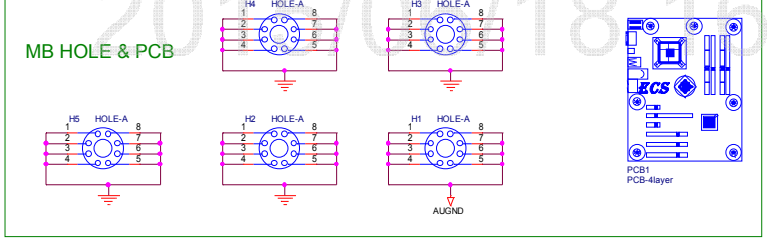




681 phase:
BOSS P/N:23-765-300145 *4PCS



MB HOLE & PCB



Elitegroup Computer Systems			
Title: SOC-10 VSS			
Size: C	Document Number: BSWD-LM		Rev: V1.0
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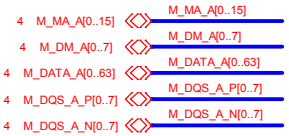
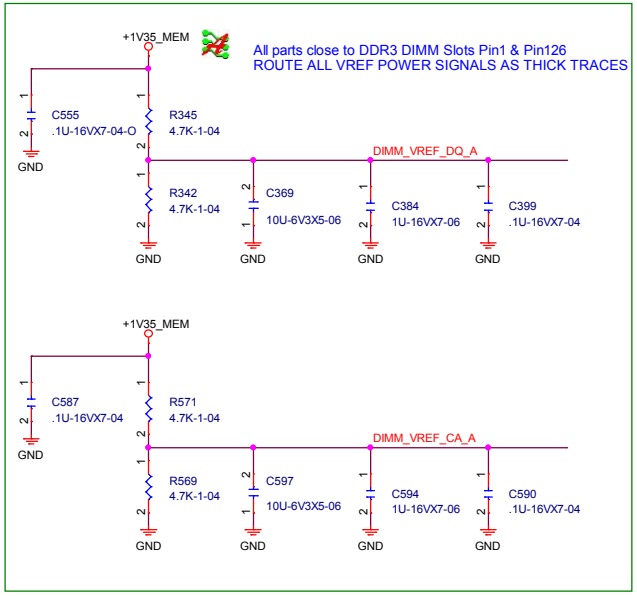
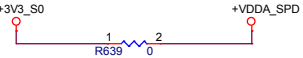
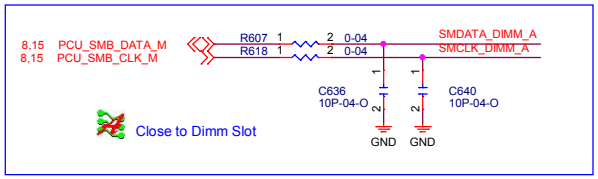
SODIMM DQ & DQS 换层方式及GND VIA务必参考PDG设计

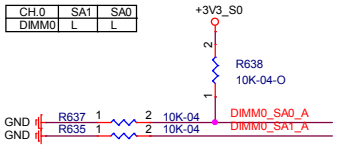


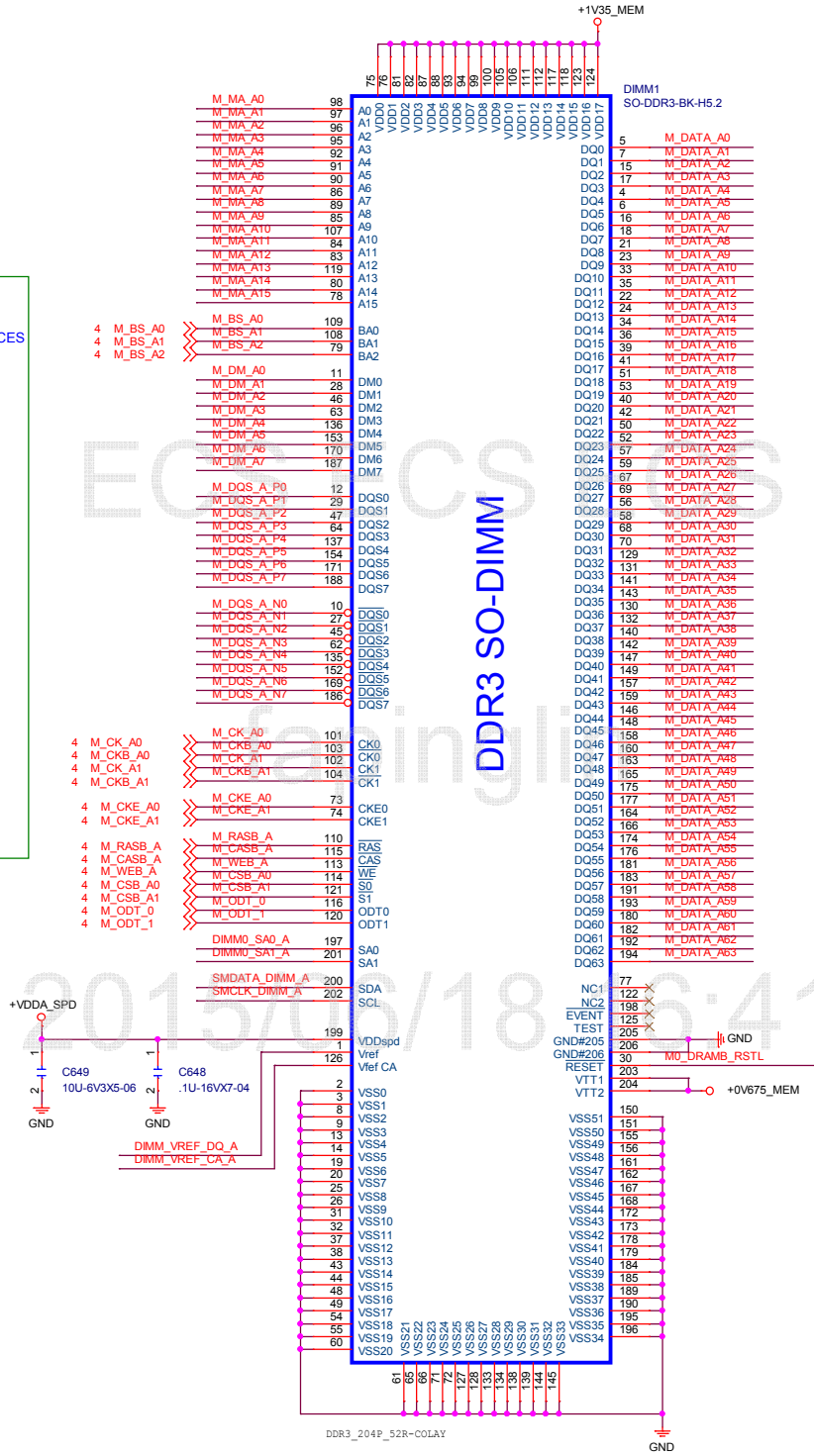


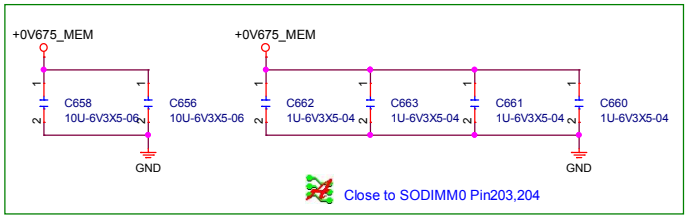


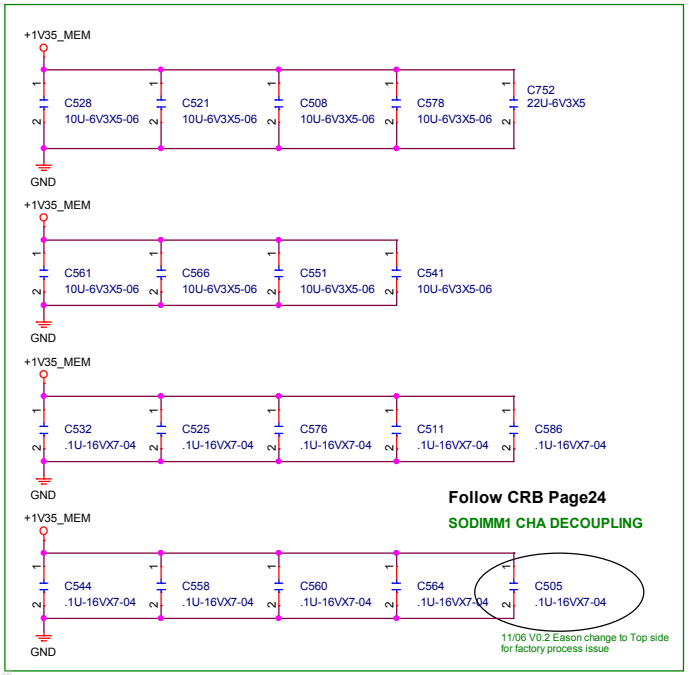


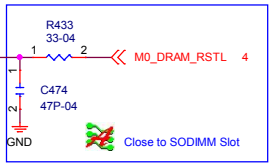
CH.0	SA1	SA0
DIMM0	L	L











Elitegroup Computer Systems	
Title	SODIMM1-CHA-H5.2MM
Size: Custom	Document Number: BSWD-LM
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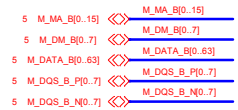
- Braswell SOC will support memory speed at 1600 MHz and 1066 MHz only.
- If 1333 MHz DIMM is installed, it will run at 1066 Mhz.

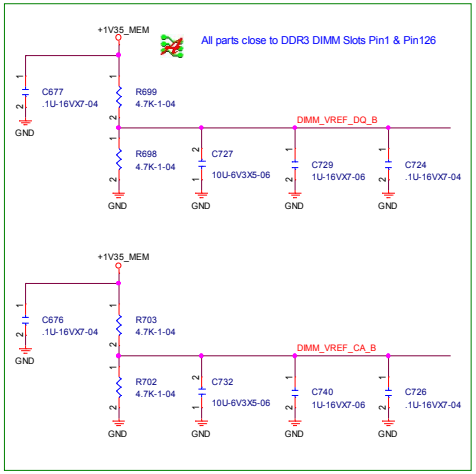
Channel 0	Channel 1	Supported Memory Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

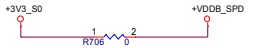
- This will be noted in the upcoming Braswell POR document update.

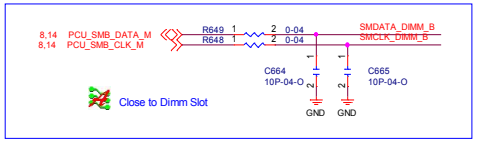
Braswell Memory Support POR Update
----20140909 Yongz

SODIMM DQ & DQS 换层方式及GND VIA务必参考PDG设计

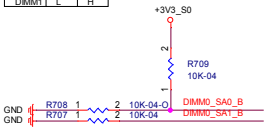


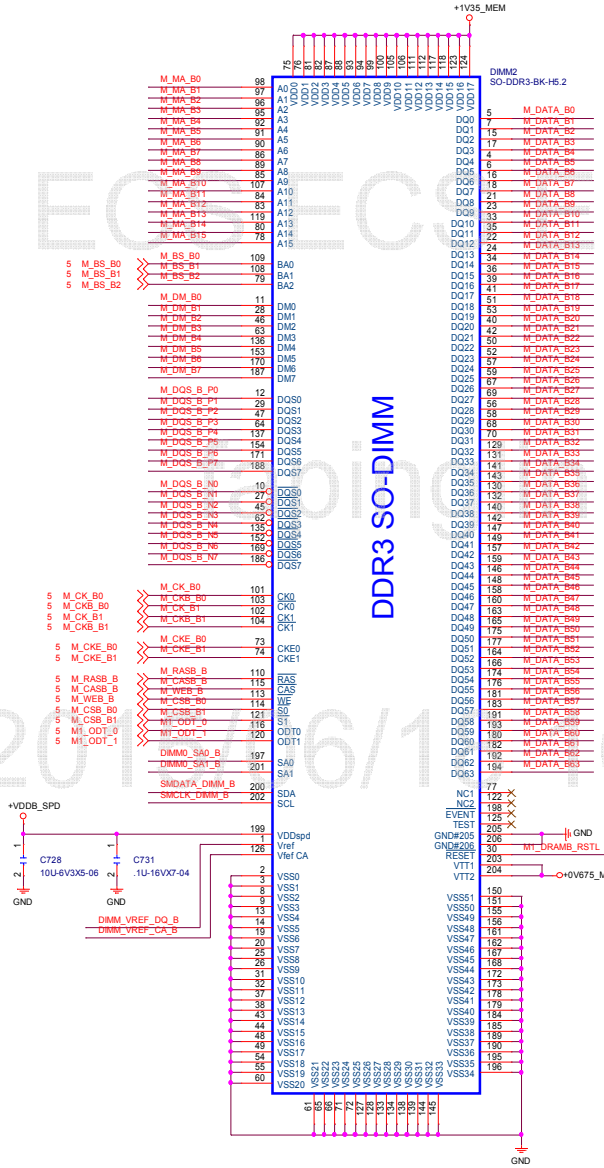


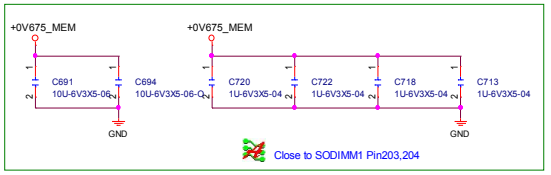


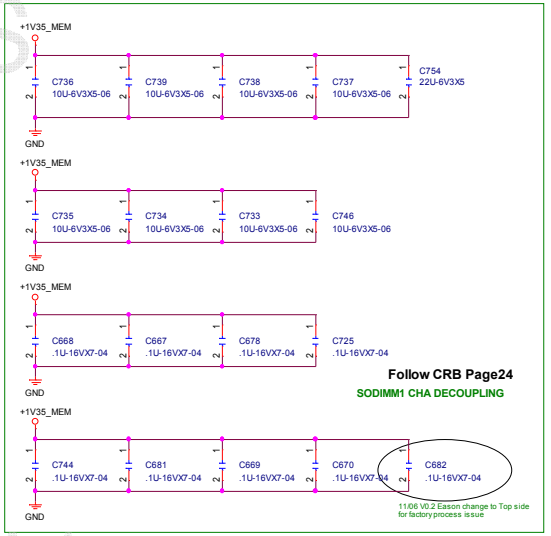


CH.1	SA1	SA0
DIMM1	L	H









Elitegroup Computer Systems	
Title	SODIMM1-CHA-H5.2MM
Size C	Document Number BSWD-LM
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Date:	Thursday, June 11, 2015
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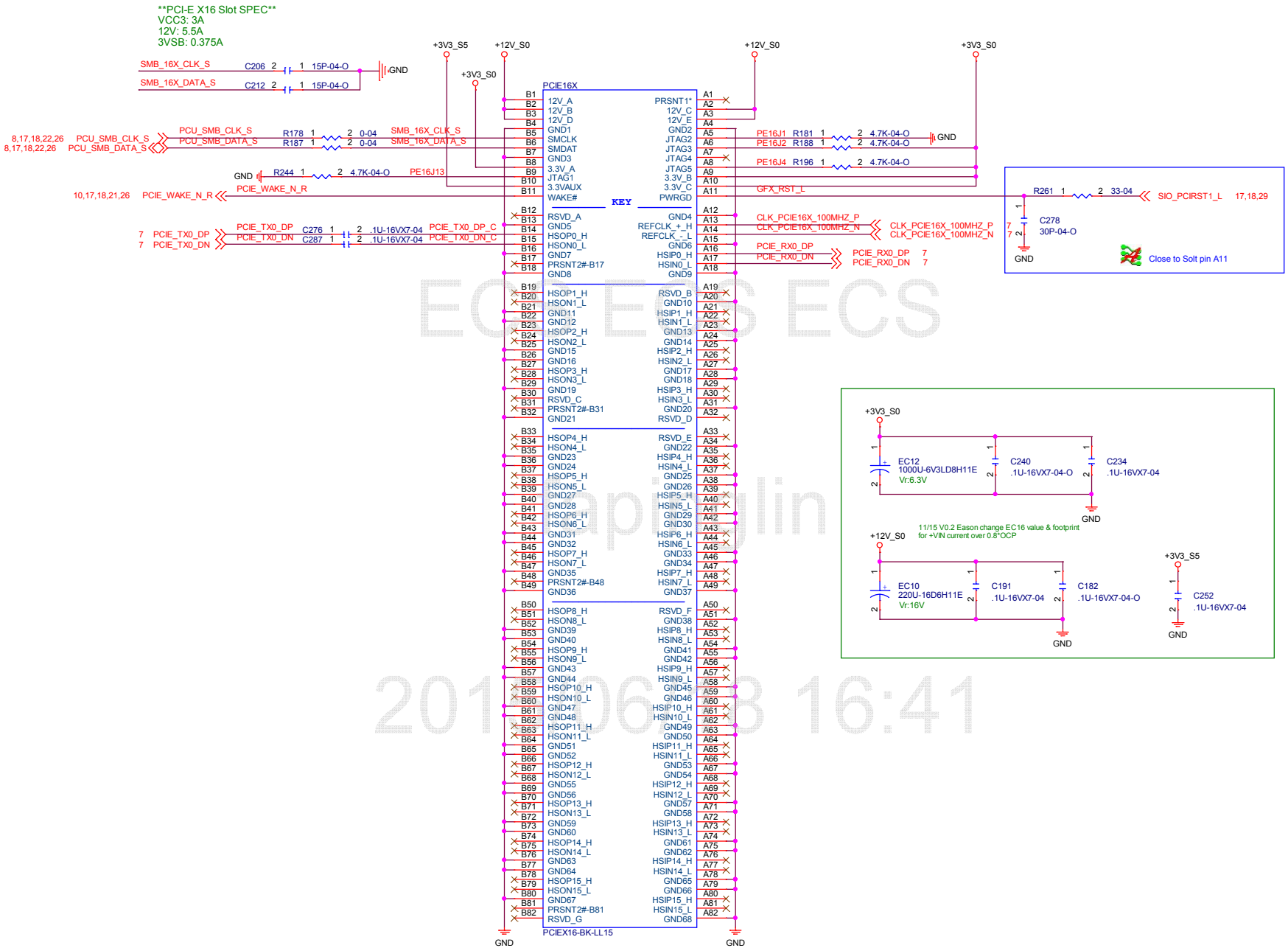
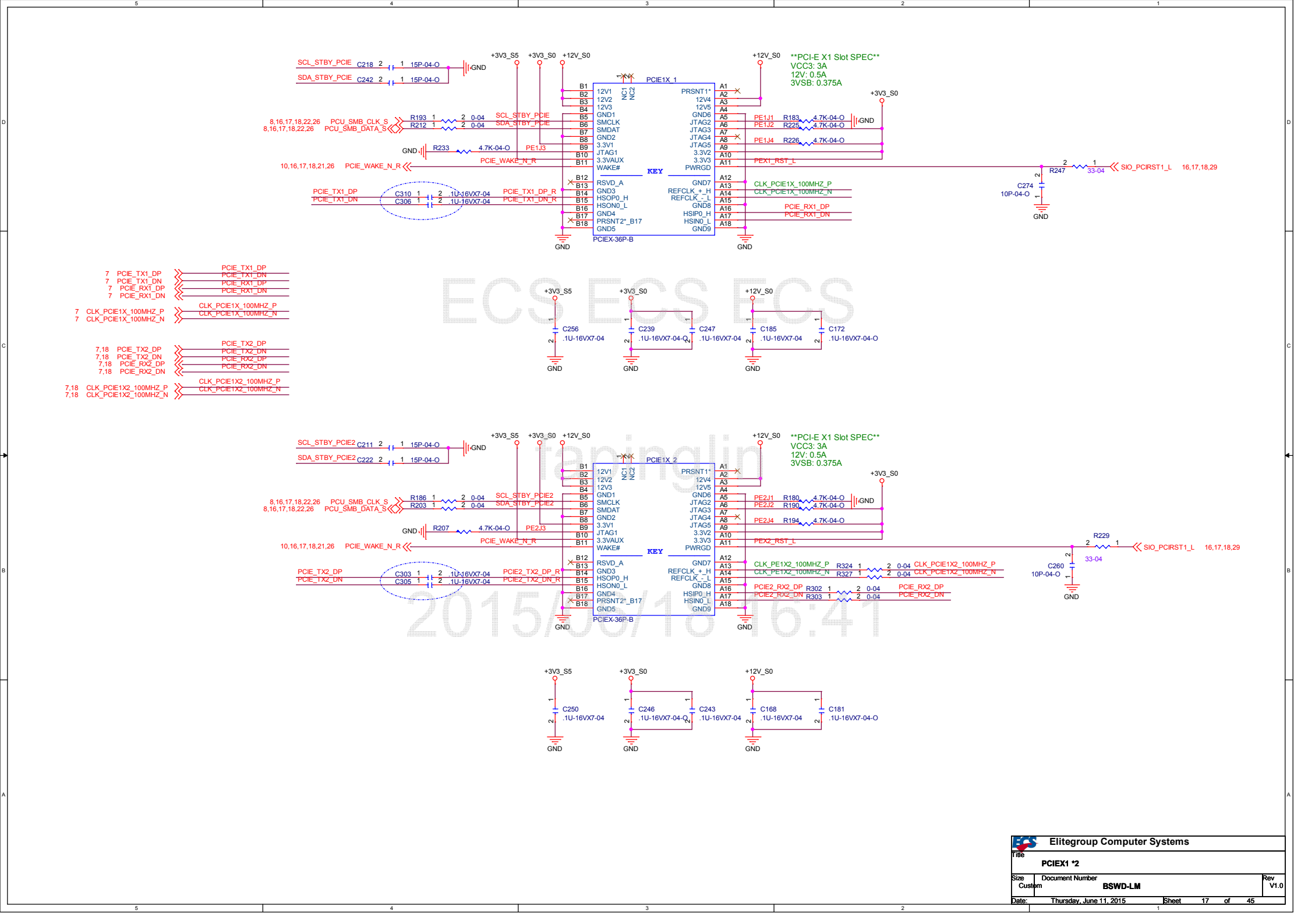
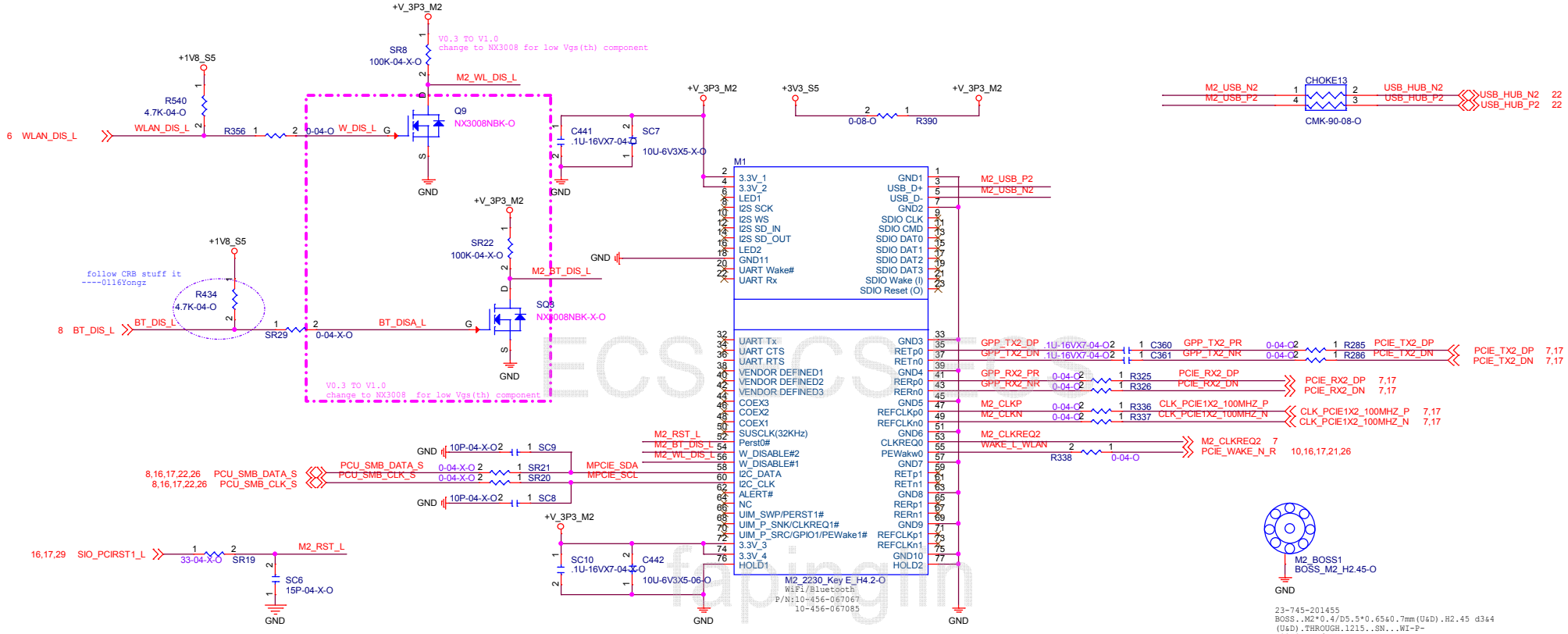


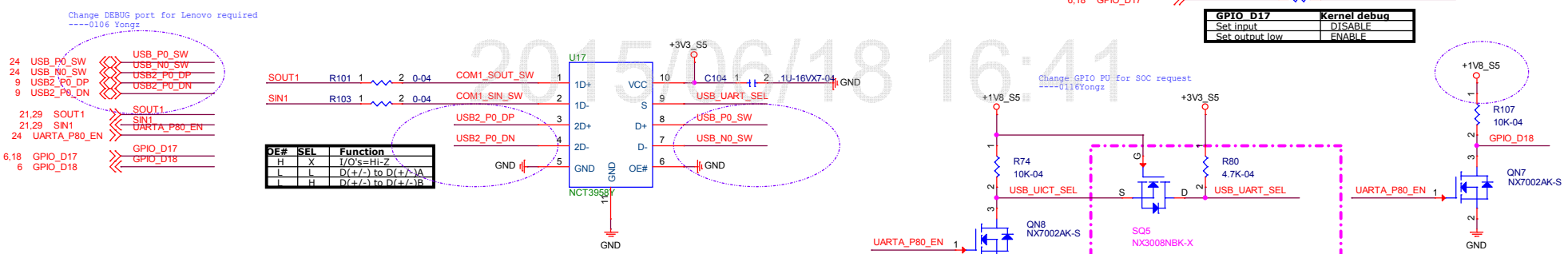
Elitegroup Computer Systems			
Title: PCI-E X2			
Size: Custom	Document Number: BSWD-LM		Rev: V1.0
Date: Thursday, June 11, 2015	Sheet 16 of 45		



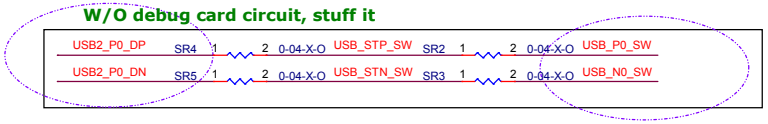
Elitegroup Computer Systems	
Title	PCIEX1 *2
Size: Custom	Document Number: BSWD-LM
Rev	V1.0
Date: Thursday, June 11, 2015	Sheet 17 of 45



W debug card circuit, stuff it



W/O debug card circuit, stuff it



UARTA_P80_EN	USB_UART_SEL	POST 80
H	L	ENABLE
L	H	DISABLE

Plug debug card,UARTA_P80_EN is High
Unplug debug card,UARTA_P80_EN is Low

Title	M.2
Size	Custom
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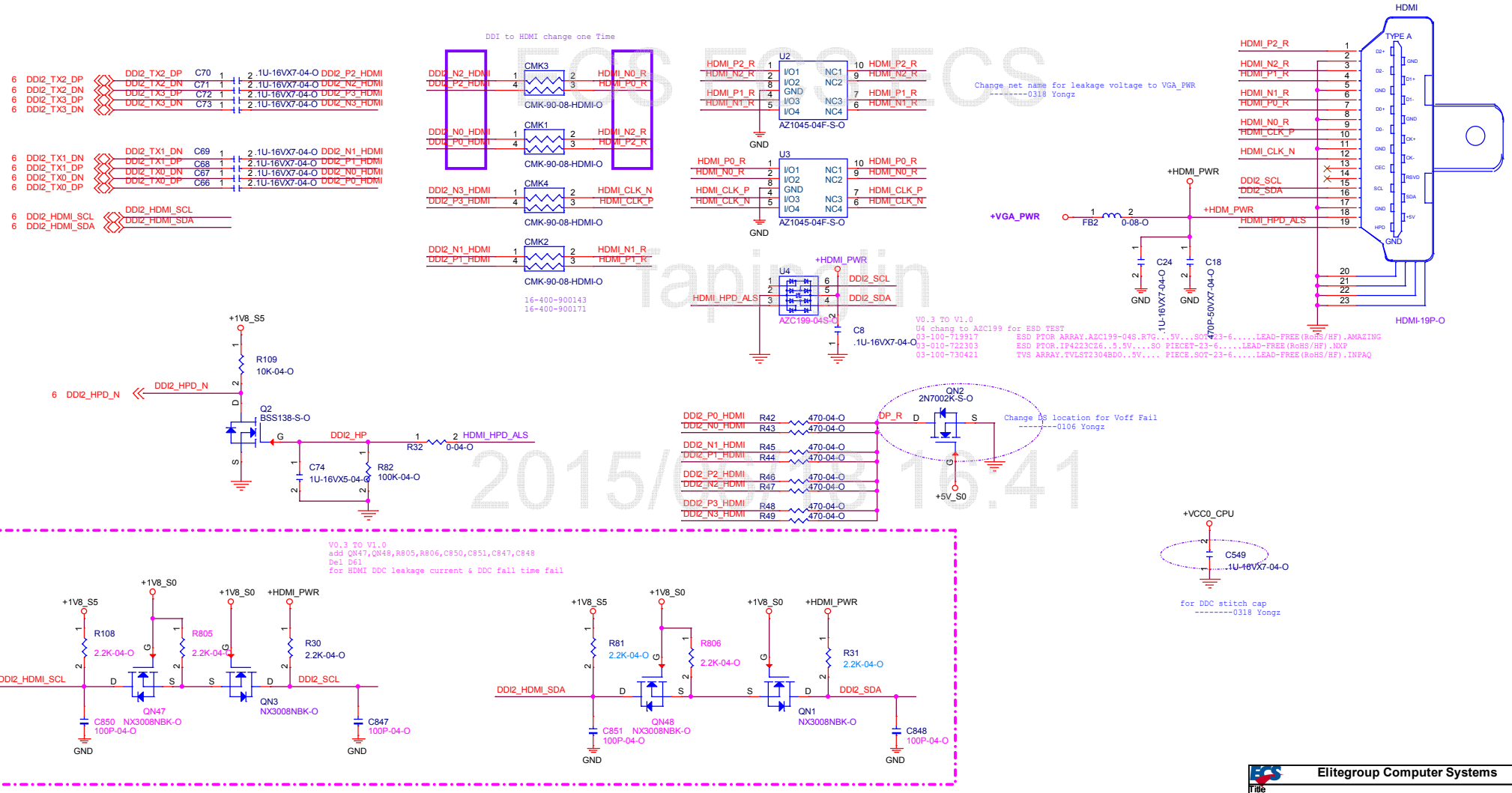
Elitegroup Computer Systems



Company	Elitegroup Computer Systems
Title	DisplayPort DP
Size	Custom
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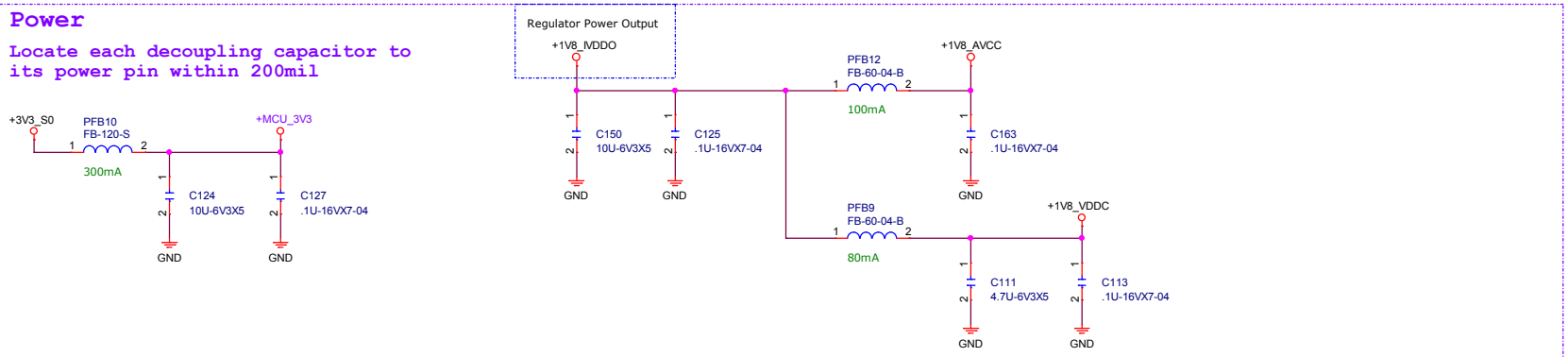
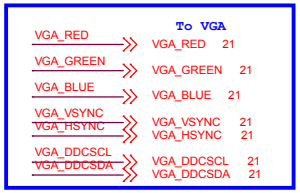
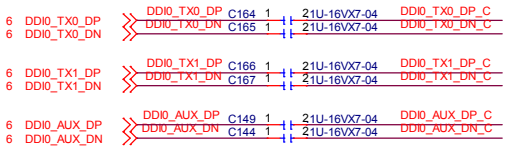
Power

Locate each decoupling capacitor to its power pin within 200mil



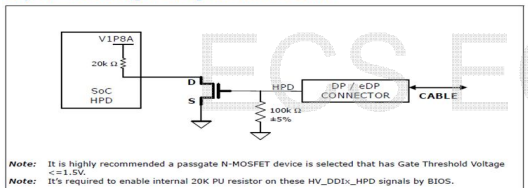


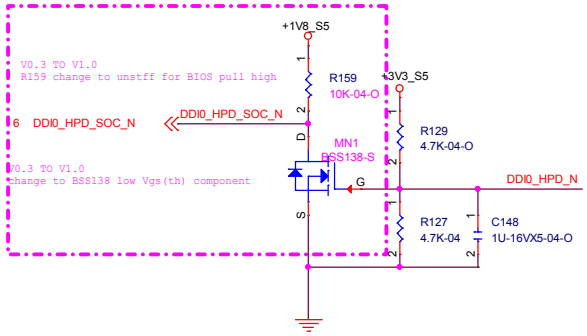
From SoC



Differential impedance = 100 ohm

DP/eDP* HPD Passgate Design Recommendation

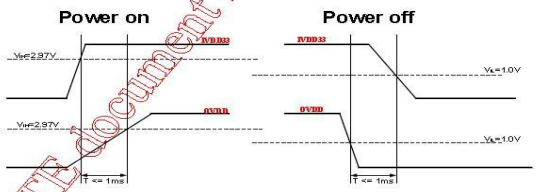




Power/Ground Pins

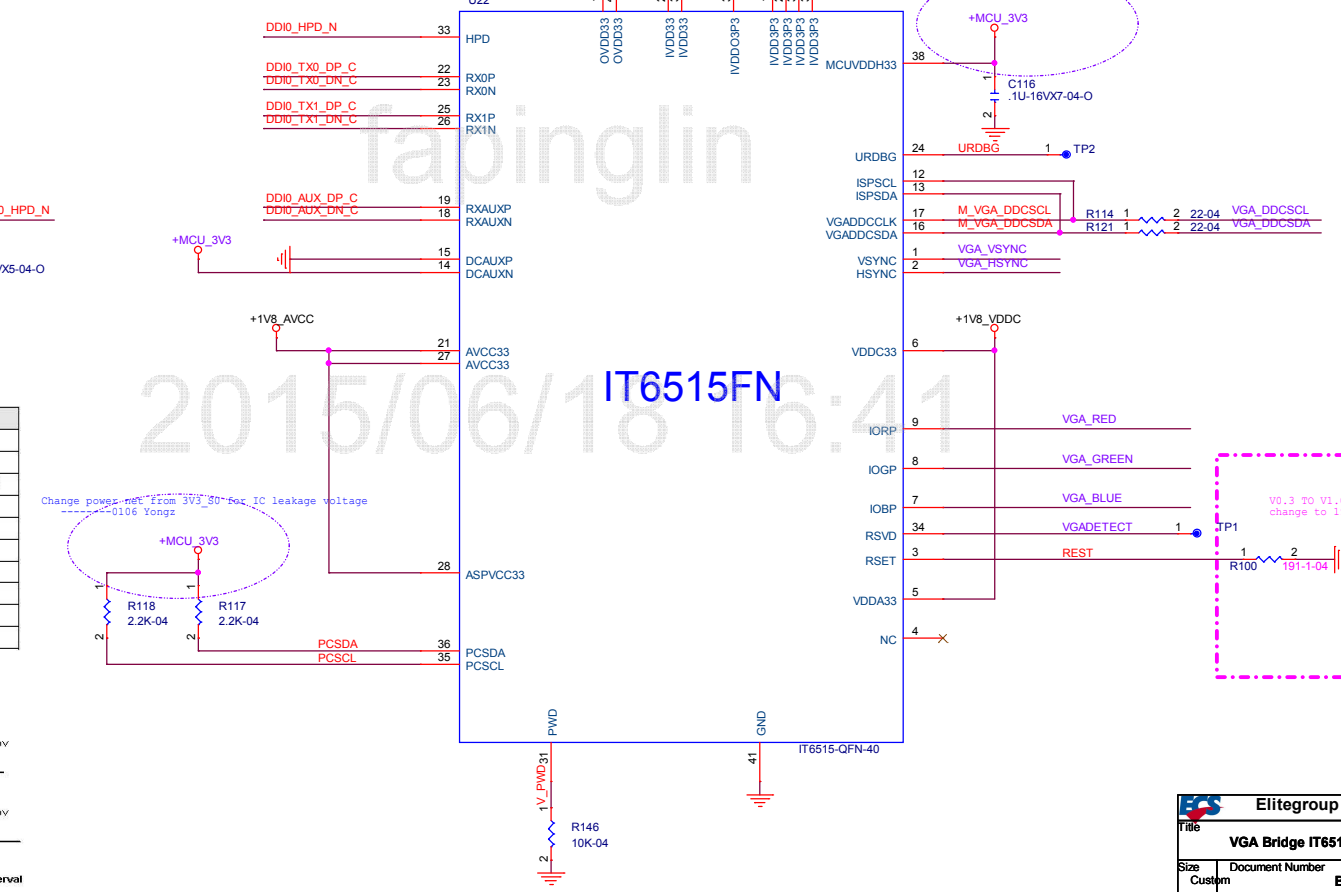
Pin Name	Description	Type	Pin No.
IVDD33	Regulator power input (3.3V)	Power	29, 30
IVDDO	Regulator power output (1.8V)	Power	32
IVDD	Digital logic power (1.8V)	Power	11, 20, 37, 39
OVDD	I/O Pin power (3.3V)	Power	10, 40
AVCC	DP analog front-end power (1.8V)	Power	21, 27
ASPVCC	Power for oscillator and PLL	Power	28
VDDC	DAC analog power (1.8V)	Power	6
VDDA	Voltage reference circuit analog power (1.8V)	Power	5
MCUVDDH	Supply power for Embedded MCU (3.3V~5V)	Power	38
GND	**Exposed GND pad**	**Ground**	**41**

Power Sequence for Power on and Power off.



When power on, please keep IVDD33 go VIH before OVDD go VIH. And please keep the time interval between IVDD33 and OVDD shorter than 1ms when power on or power off.

IT6515 Output 1.8V



VGA Bridge (DP to VGA)
ITE IT6515FN

Elitegroup Computer Systems			
Title: VGA Bridge IT6515FN			
Size: Custom	Document Number: BSWD-LM		Rev: V1.0
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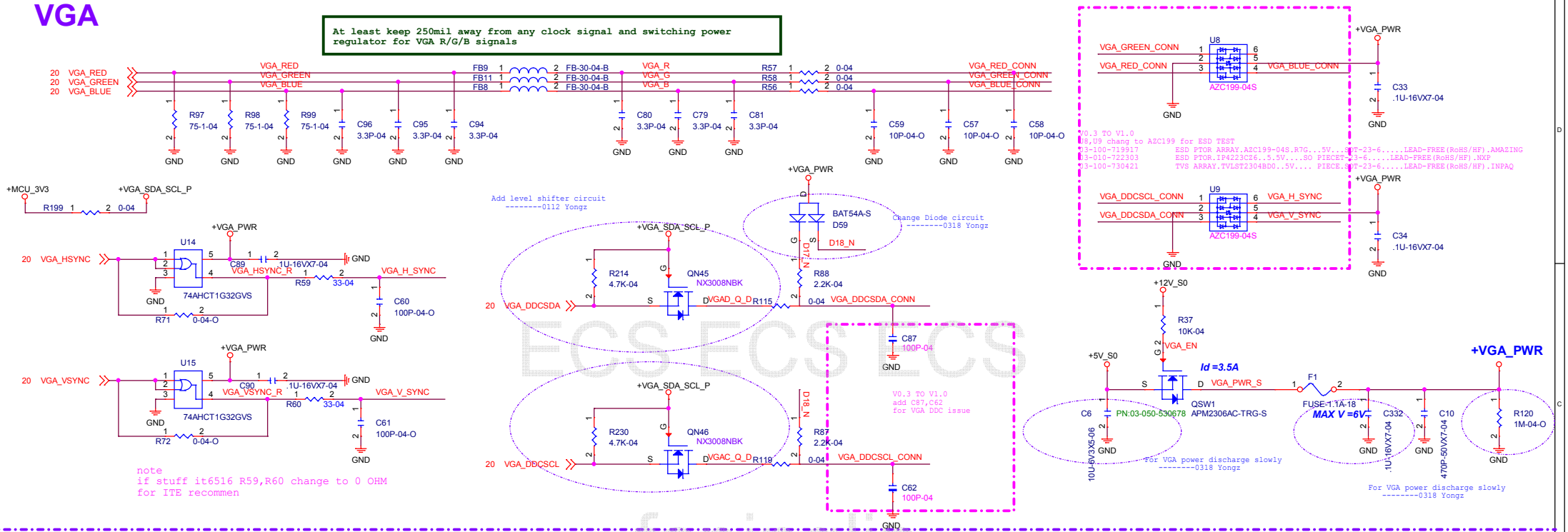
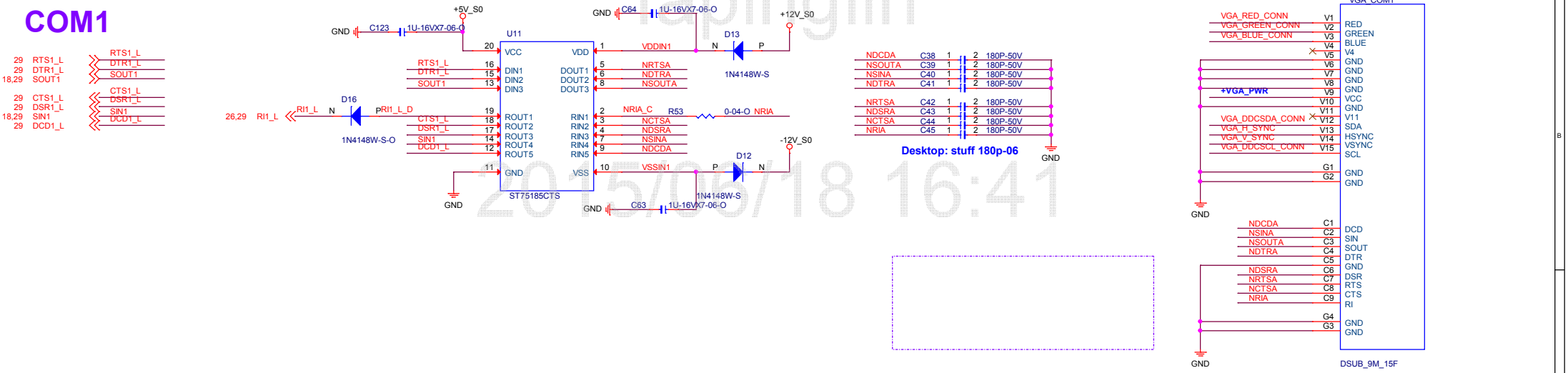
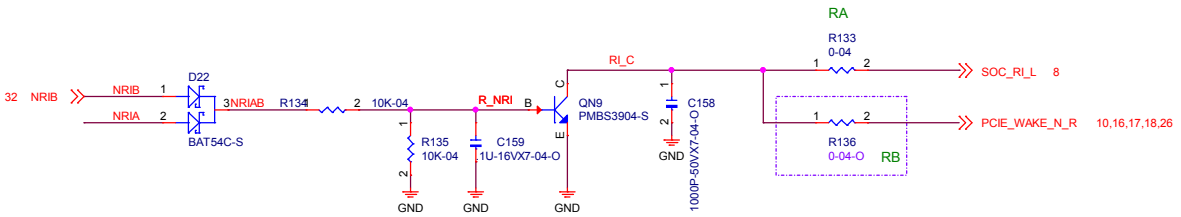
VGA

At least keep 250mil away from any clock signal and switching power regulator for VGA R/G/B signals



COM1





Elitegroup Computer Systems	
Title: VGA/COM1	
Size: Custom	Document Number: BSWD-LM
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USB2.0 HUB
GL850G-50
Colay GL852G-50

Table 5.3 - QFN 28 Non-removable Port Configurations

OVCURn#	Non-removable Configuration of Portn
Floating	Non-removable
Pull high	Removable

Card Reader

23 USB_HUB_P1 — USB_HUB_N1
23 USB_HUB_N1

M.2

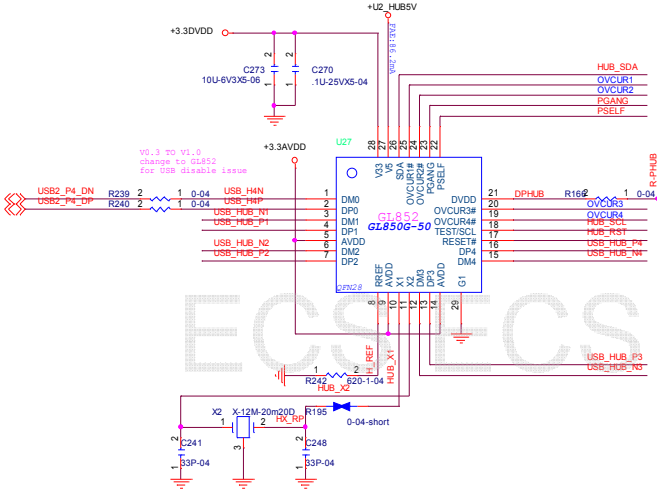
18 USB_HUB_P2 — USB_HUB_N2
18 USB_HUB_N2

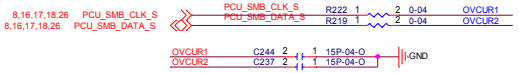
USB2.0 Header

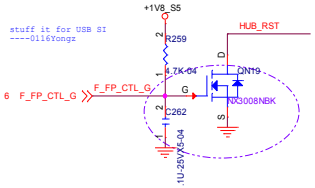
23 USB_HUB_P3 — USB_HUB_N3
23 USB_HUB_N3

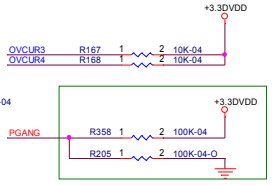
USB2.0 Charge Header

23 USB_HUB_P4 — USB_HUB_N4
23 USB_HUB_N4



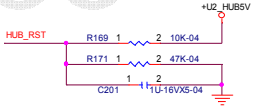




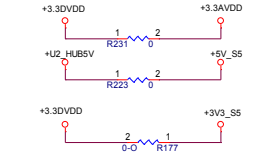


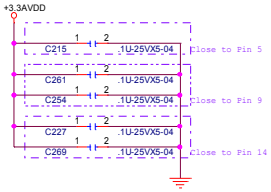
PGANG
0 Individual mode (OVCUR)x4Group via 4 Fuse output 1@normal ; 0@suspend
1 Gang mode (OVCUR) x1Group via 1 fuse output 0@normal ; 1@suspend

PSELF
0 GL850G is bus-powered*Upstrem port power Downstrem port 100mA/per
1 GL850G is self-powered *external Power Downstrem port 500mA/per



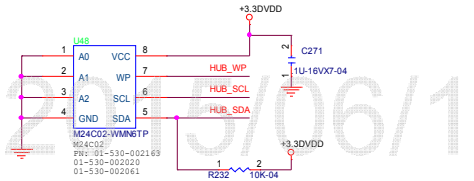
No sequence require





Option:
Customized VID, PID,
String, Configuration.

TEST/SCL	14	18	I /B	TEST: 0: Switch mode. 1: Chip will be put in test mode. NC: Normal hub operation. I2C:clock output pin



HUB_SCL Floating for internal ROM

If client do not have the special VID/PID of USB need to feedback,GL850G will use internal Rom(預設 VID/PID) reply the Host request USB Descriptor

If client have theirself VID/PID need to be feedback,that must use a external EEPROM to record VID/PID information

Elitegroup Computer Systems

Title: GL852G-12

Size: C | Document Number: BSWD-LM | Rev: V1.0

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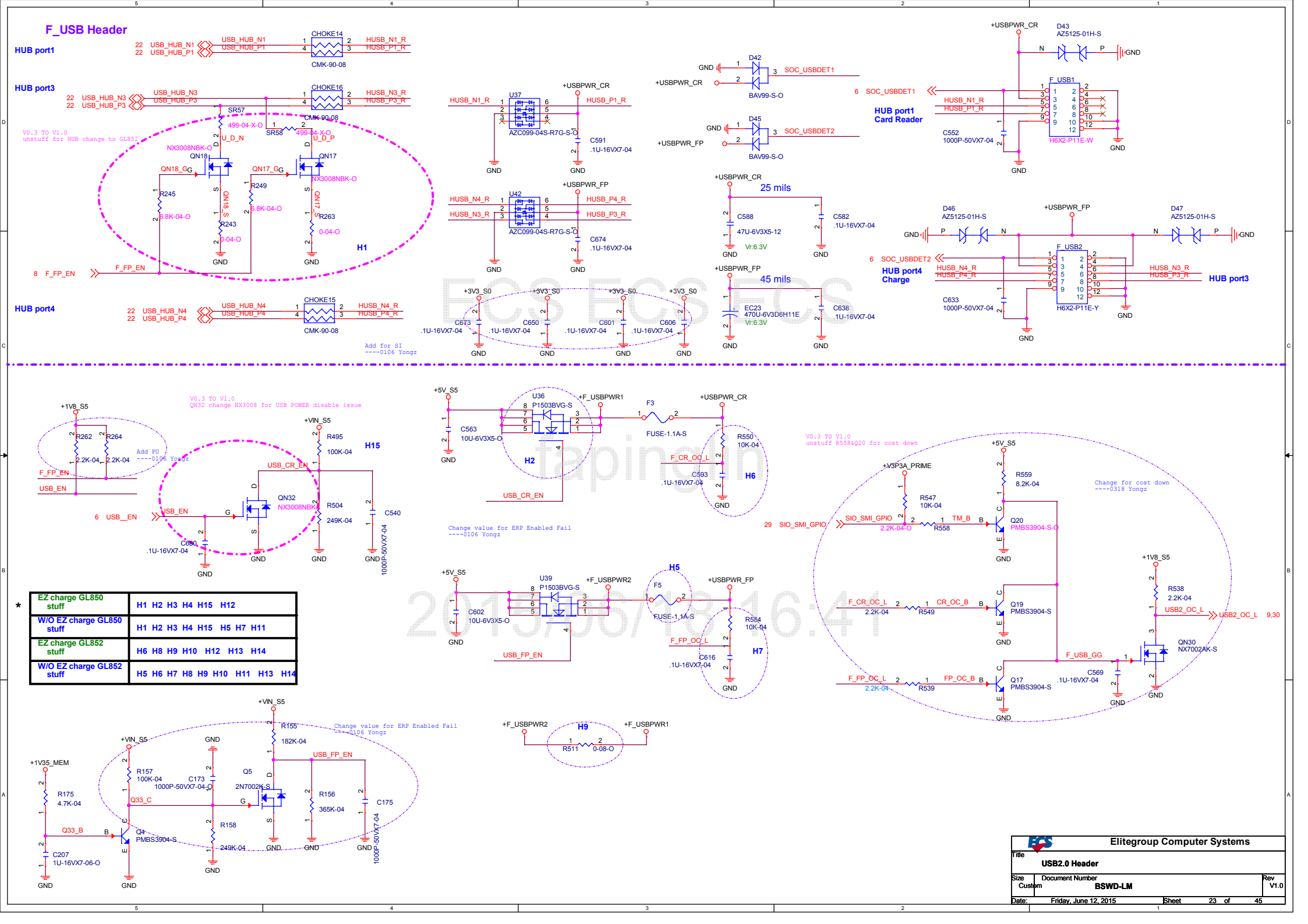
F_USB Header
HUB port1
HUB port3
HUB port4
HUB port1 Card Reader
HUB port4 Charge
HUB port3
H1
H2
H5
H6
H7
H9
H15
Add for SI ----0106 Yongz
Add PU ----0106 Yongz
Change value for ERP Enabled Fail ----0106 Yongz
Change for cost down ----0318 Yongz
25 mils
45 mils
EZ charge GL850 stuff | H1 H2 H3 H4 H15 H12
W/O EZ charge GL850 stuff | H1 H2 H3 H4 H15 H5 H7 H11
EZ charge GL852 stuff | H6 H8 H9 H10 H12 H13 H14
W/O EZ charge GL852 stuff | H5 H6 H7 H8 H9 H10 H11 H13 H14
Elitegroup Computer Systems
USB2.0 Header
BSWD-LM
V1.0
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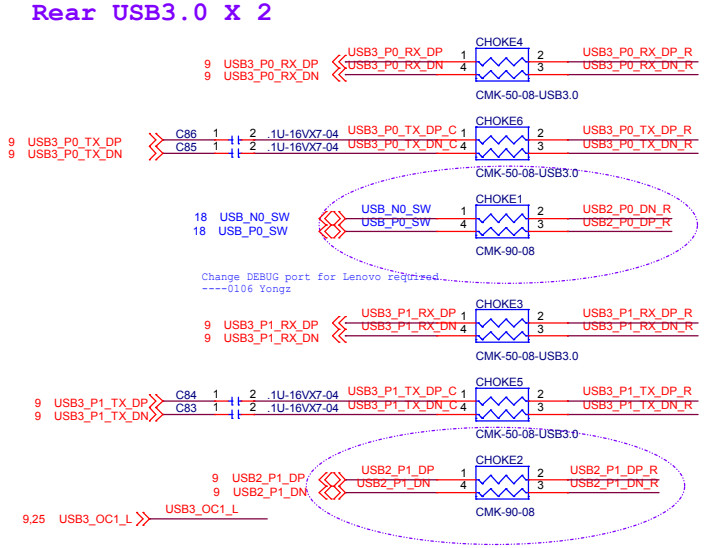
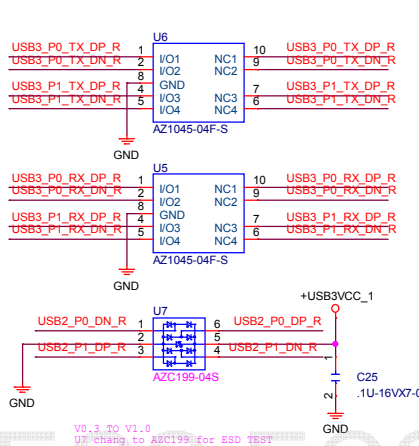
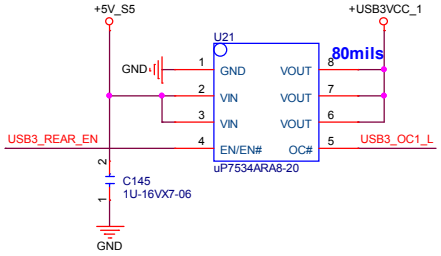
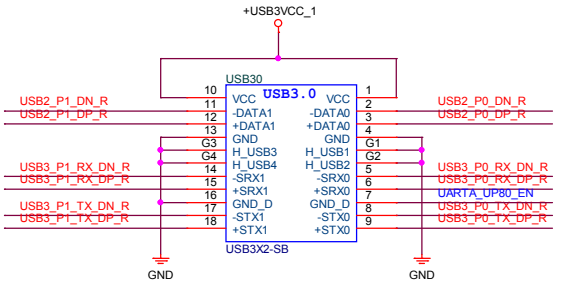
Rear USB3.0 X 2

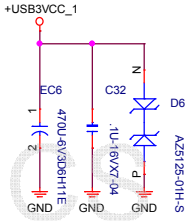


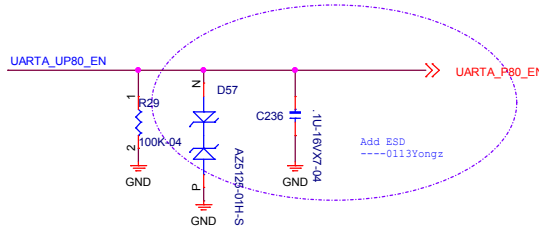


USB3.0 Power

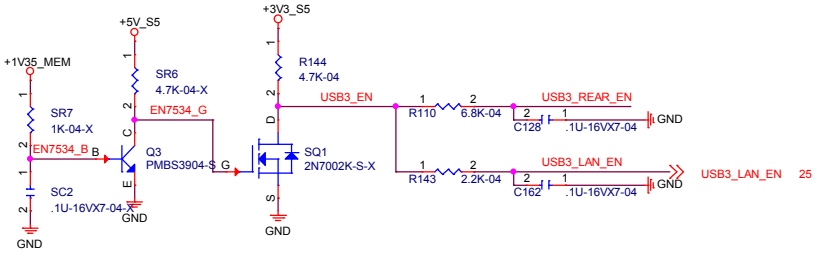




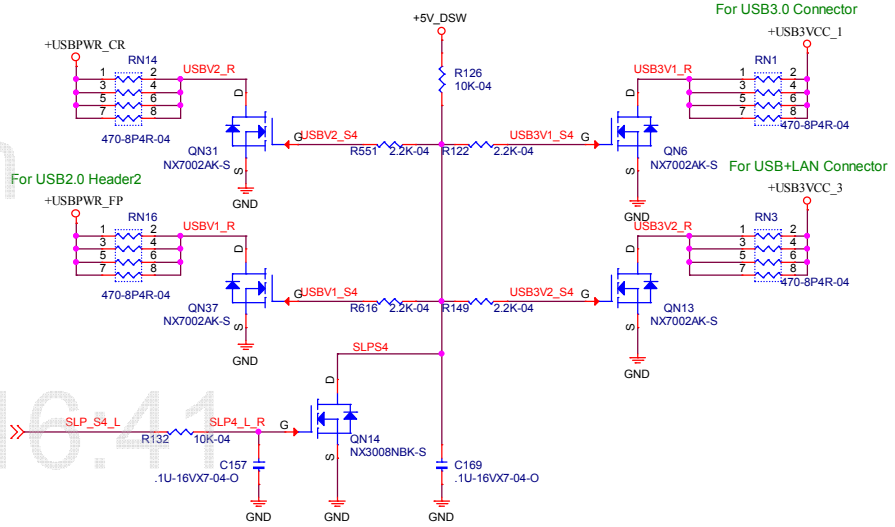




USB_EN



USB Discharge Circuit



Elitegroup Computer Systems		
Title: USB3.0 Conn./USB Discharge		
Size: Custom	Document Number: BSWD-LM	Rev: V1.0
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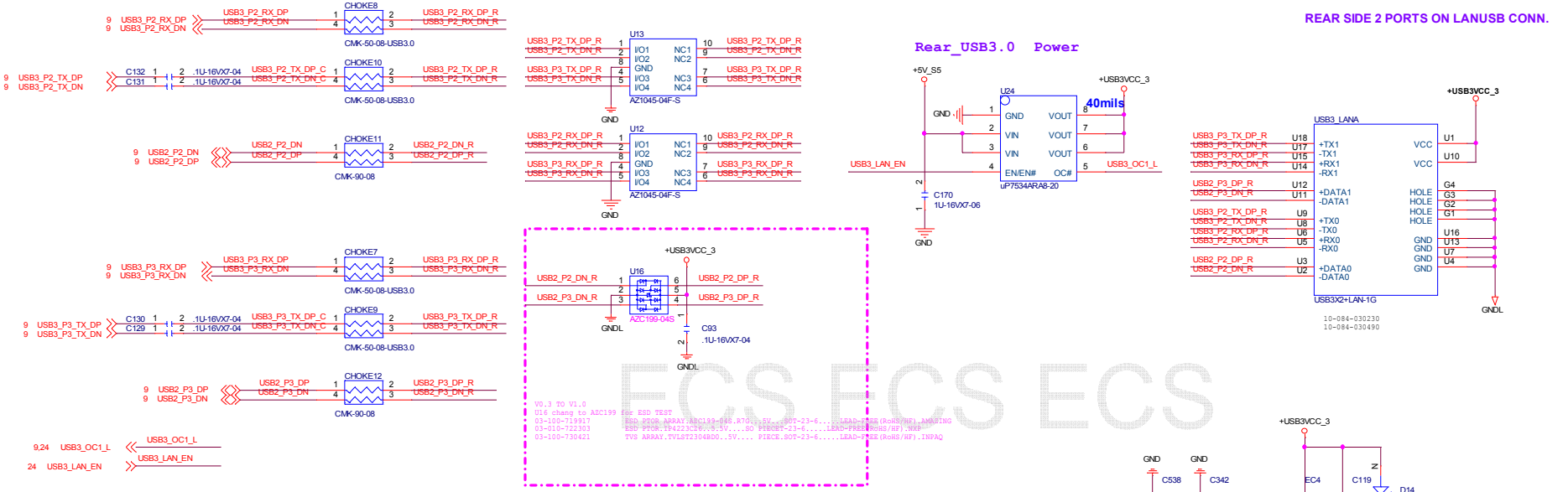
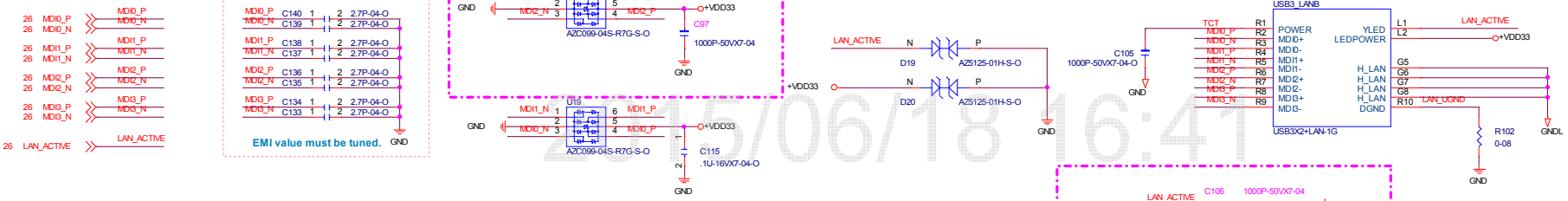
REAR SIDE 2 PORTS ON LANUSB CONN.

Rear_USB3.0 Power

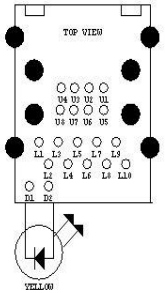


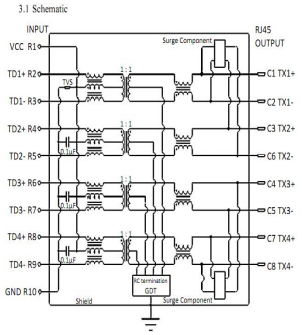


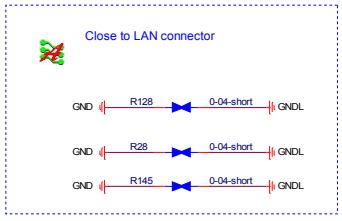
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on

blinking







Elitegroup Computer Systems		
Title: LAN Connector		
Size: Custom	Document Number: BSWD-LM	Rev: V1.0
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Reserve EEROM & ASF

Internal Switching Regulator

RTL8105E-VD 3.3V rise time > 1ms , < 100ms

Close to SoC SIDE

Close to LAN SIDE

RTL8111GN-CG C1

LC

LD

LA

LB

LE

EA

RK

LF

WD

WC

WB

Close to LAN chip

Remove For Not Using Switching Regulator

RC FOR ASF RTL8111E-VB

For WOL option

MODE	WB	WC	WD
WOL Normal(PCH_WAKE#)	X	V	X
WOL G3->S5(SIO_RI)	V	X	V
WOL_Normal and G3->S5	V	V	X

Chip/Version	MODE	LC	LD	LE	LF	Ra	C1
RTL8111E-VB	SWR	X	V	V	V(1-2)	V	RTL8111E-VB
RTL8111GN-CG	SWR	X	V	V	V(1-2)	V	RTL8111GN-CG
RTL8111GN-CG*	LDO	V	X	X	V(2-3)	V	RTL8111GN-CG
RTL8105E	LDO	X	X	X	V(2-3)	X	RTL8105E

Used	EA	RK
eFuse *	X	V
EEPROM	V	V

9. Power Sequence

Figure 3. Power Sequence

Table 19. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Unit
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

Title	LAN RTL8111GN-CG
Size	Custom
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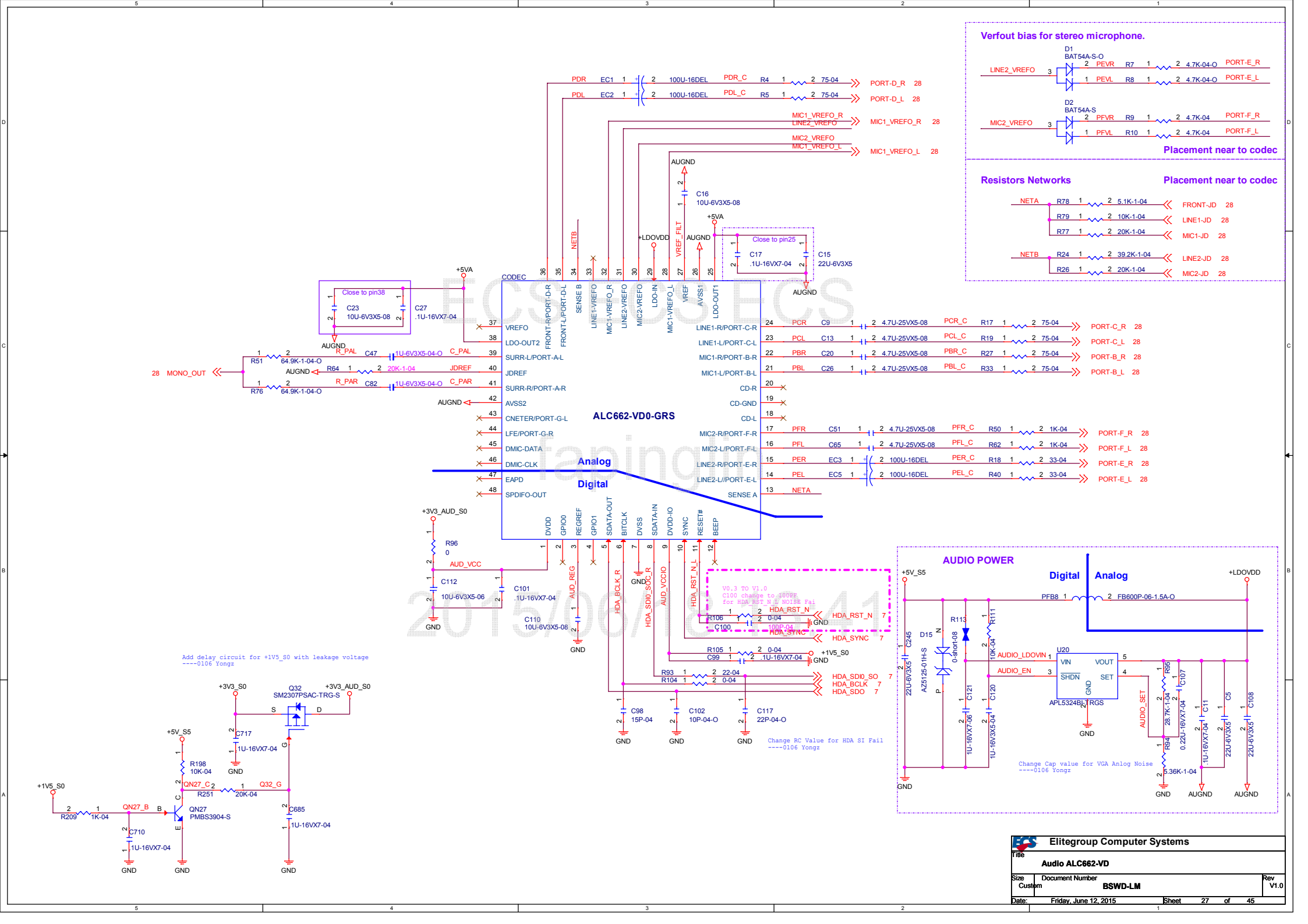
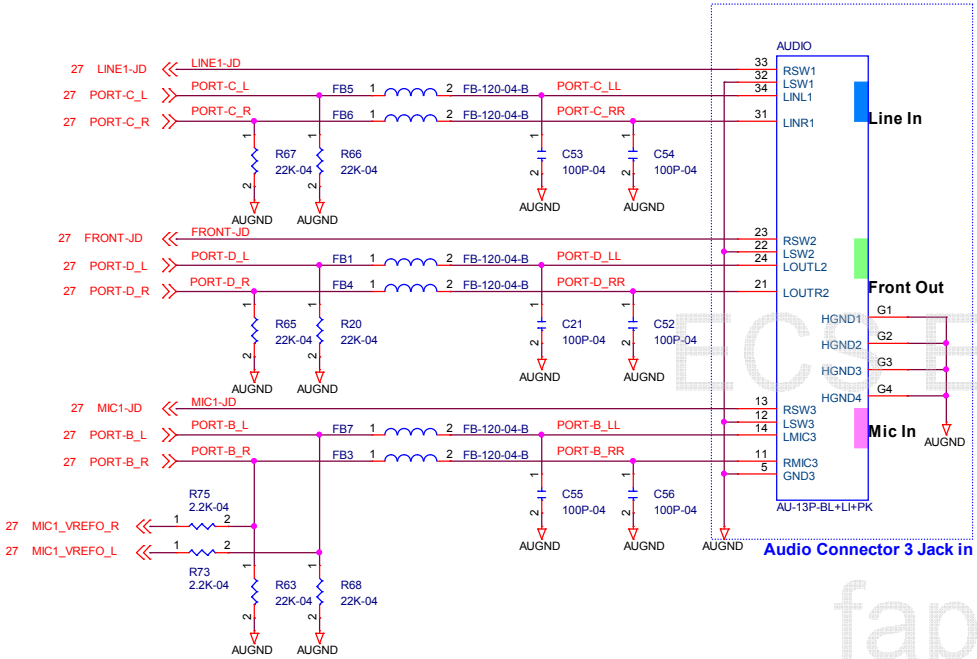
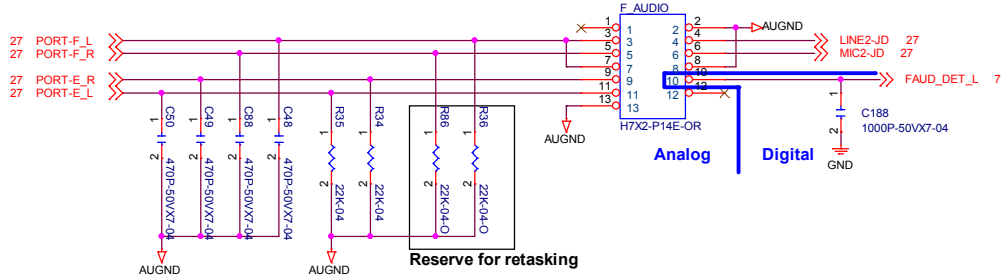
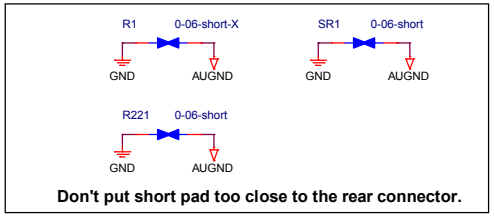
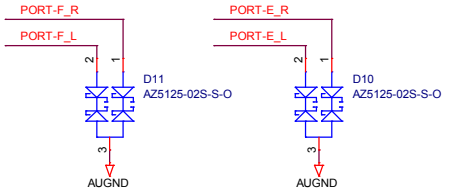
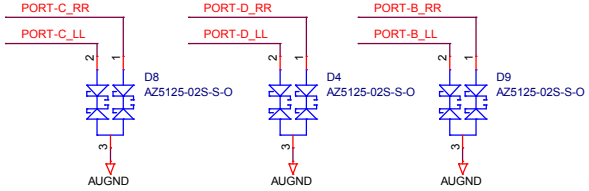

Verfout bias for stereo microphone.
Placement near to codec
Resistors Networks
Placement near to codec
CODEC
ALC662-VD0-GRS
Analog
Digital
AUDIO POWER
Add delay circuit for +1V5_S0 with leakage voltage
----0106 Yongz
Change RC Value for HDA SI Fail
----0106 Yongz
Change Cap value for VGA Anlog Noise
----0106 Yongz
Elitegroup Computer Systems
Audio ALC662-VD
BSWD-LM
Friday, June 12, 2015

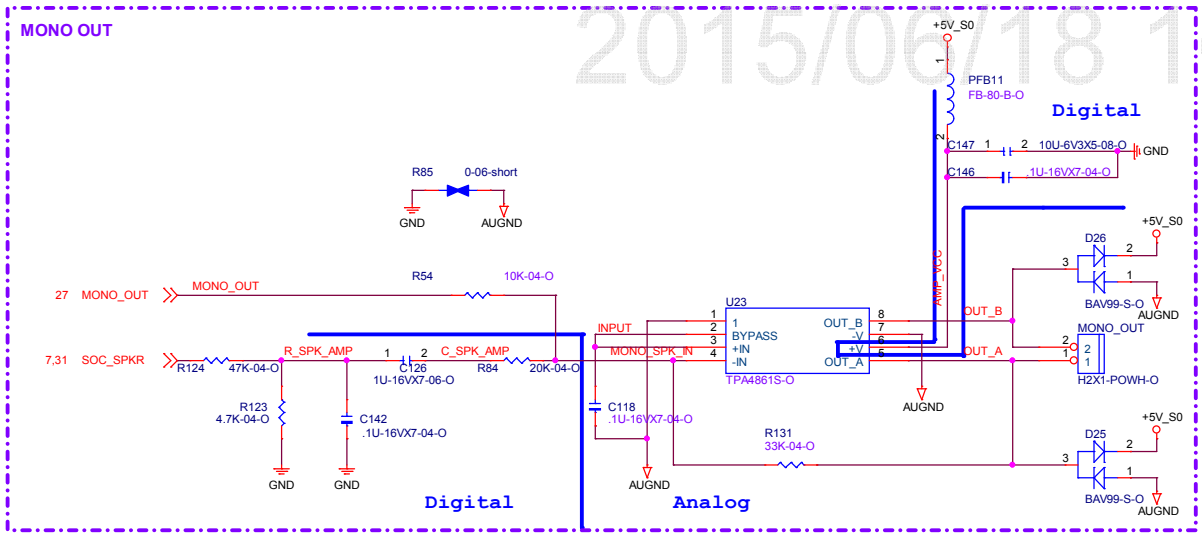












F_AUDIO:	Header color: ORANGE
pin1: NC	pin2: SENSE_A
pin3: MIC_L	pin4: HP_SNS
pin5: MIC_R	pin6: MIC_SNS
pin7: MIC_L	pin8: AGND
pin9: HP R	pin10: LC_Sense
pin11: HP L	pin12: N/A
pin13: AGND	pin14: KEY

Elitegroup Computer Systems		
Title: Audio Conn./Panel		
Size: Custom	Document Number: BSWD-LM	Rev: V1.0
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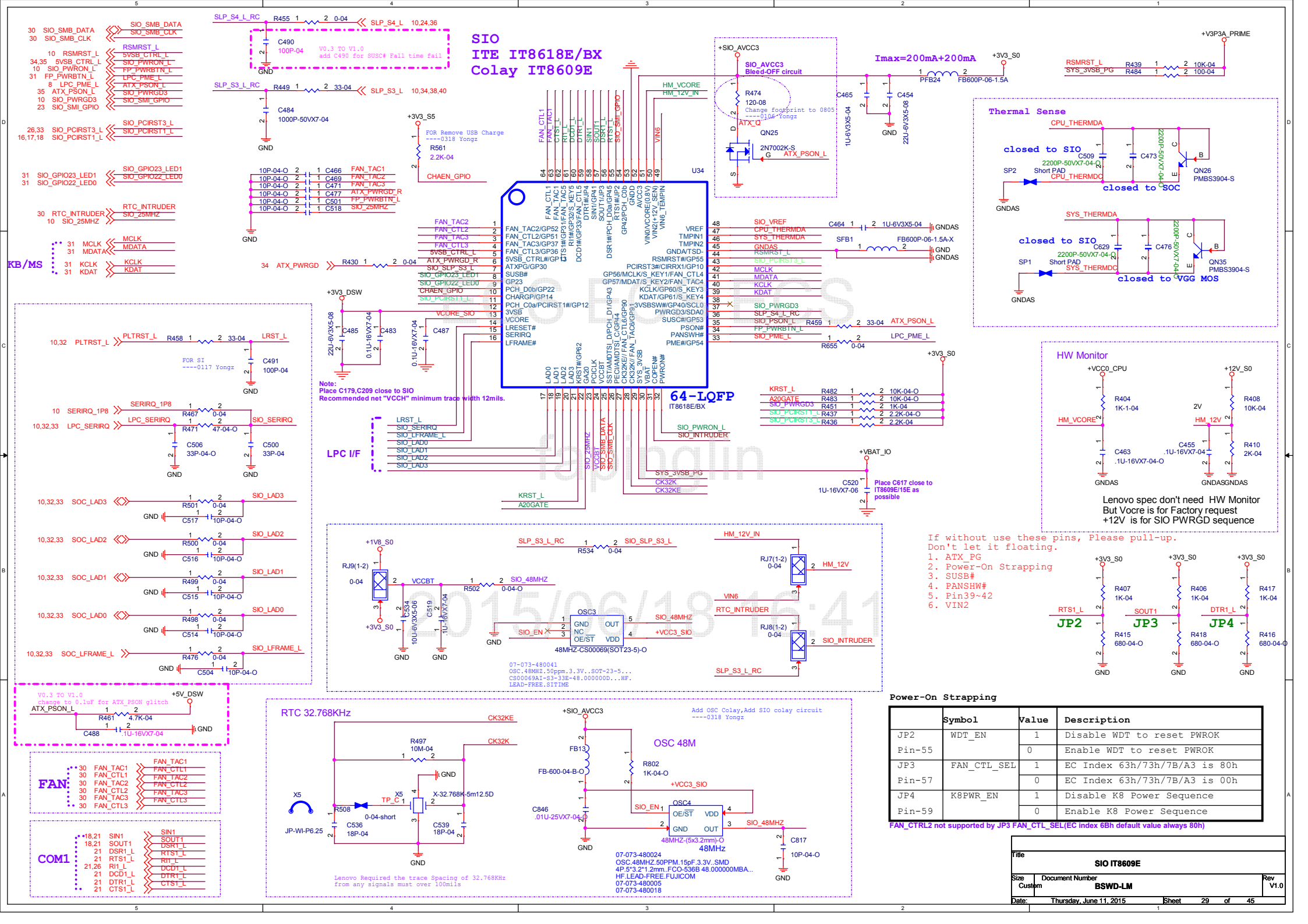
SIO
ITE IT8618E/BX
Colay IT8609E



Power-On Strapping

	Symbol	Value	Description
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-55		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
Pin-57		0	EC Index 63h/73h/7B/A3 is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-59		0	Enable K8 Power Sequence

FAN_CTRL2 not supported by JP3 FAN_CTL_SEL(EC index 6Bh default value always 80h)

Title	SIO IT8609E		
Size: Custom	Document Number: BSWD-LM		Rev: V1.0
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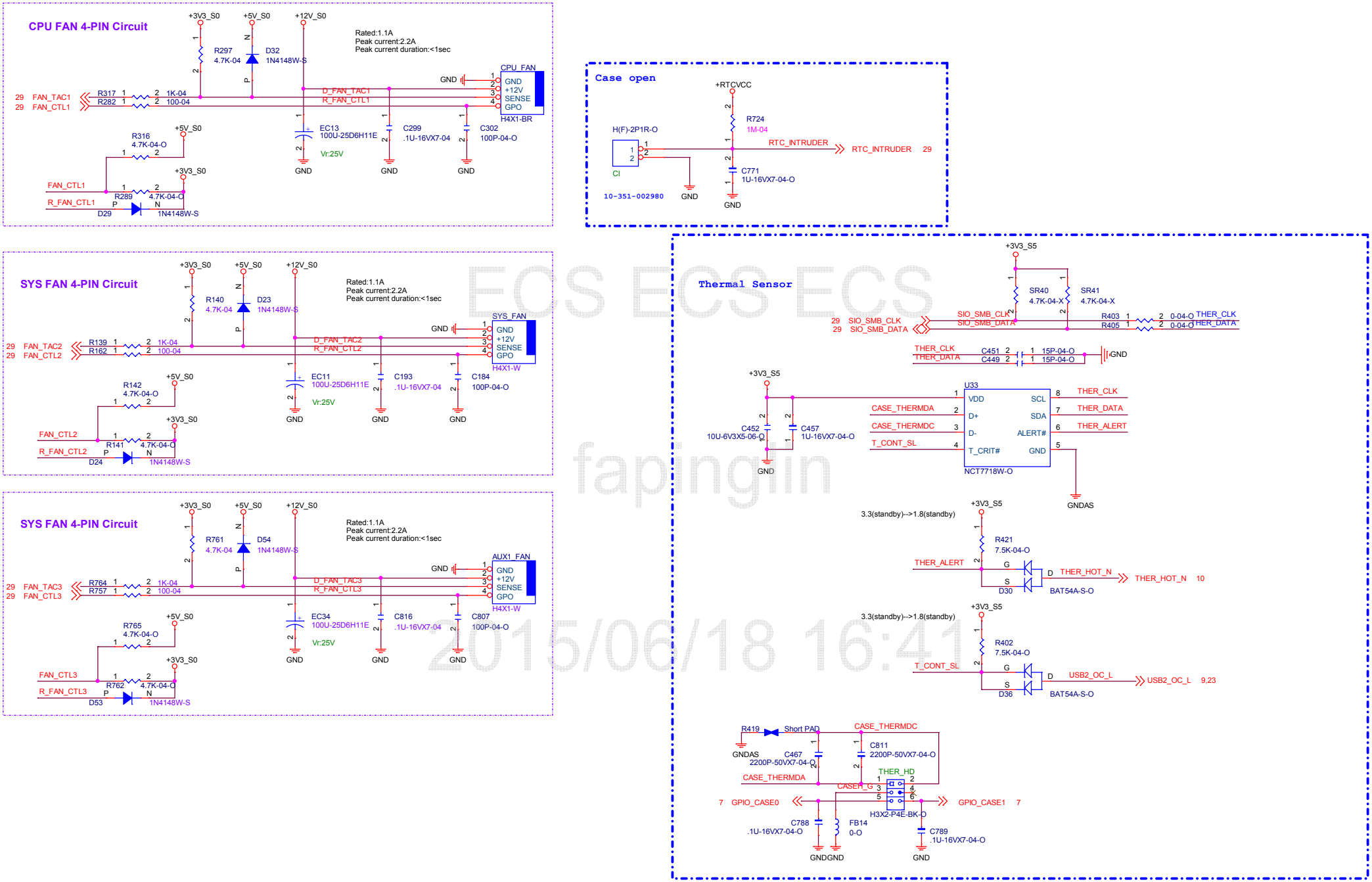

Elitegroup Computer Systems		
Title: FAN/CASE OPEN		
Size: Custom	Document Number: BSWD-LM	Rev: V1.0
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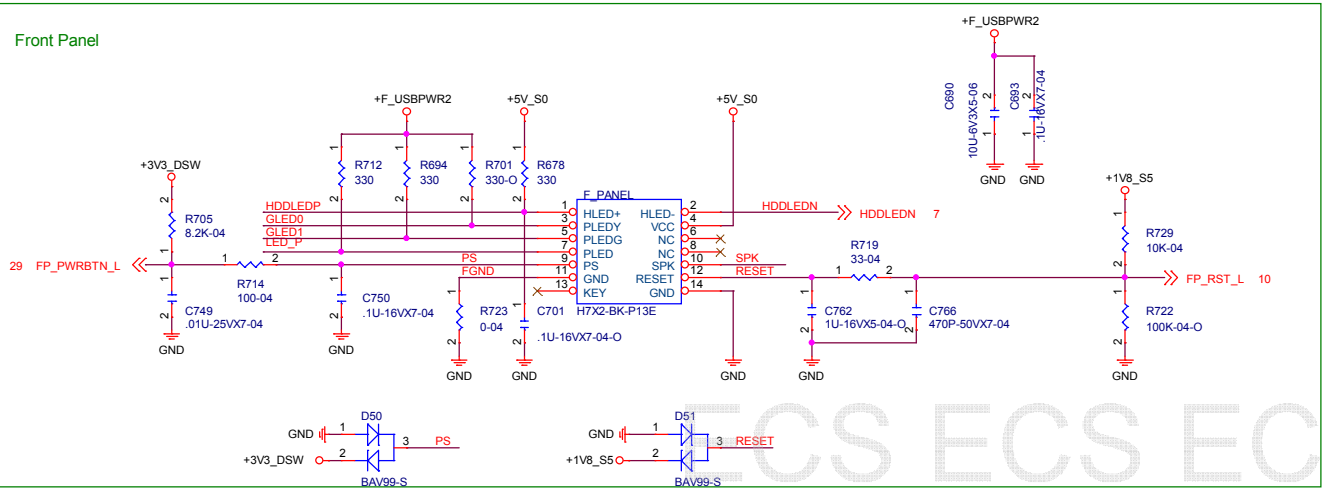
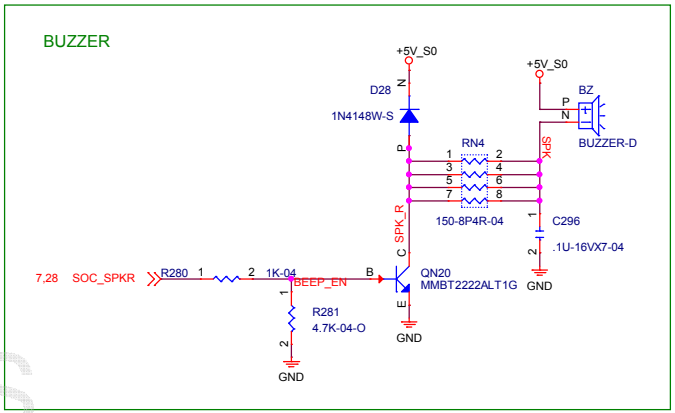
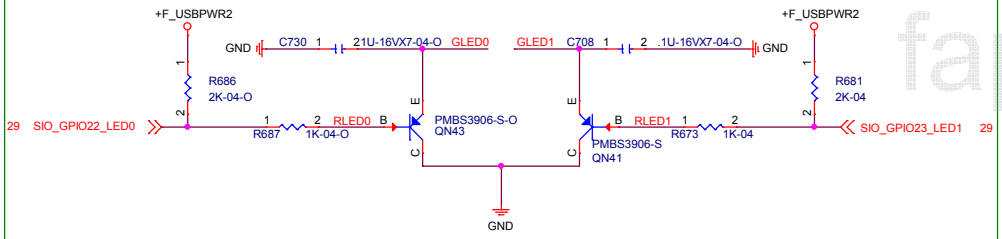
Front Panel



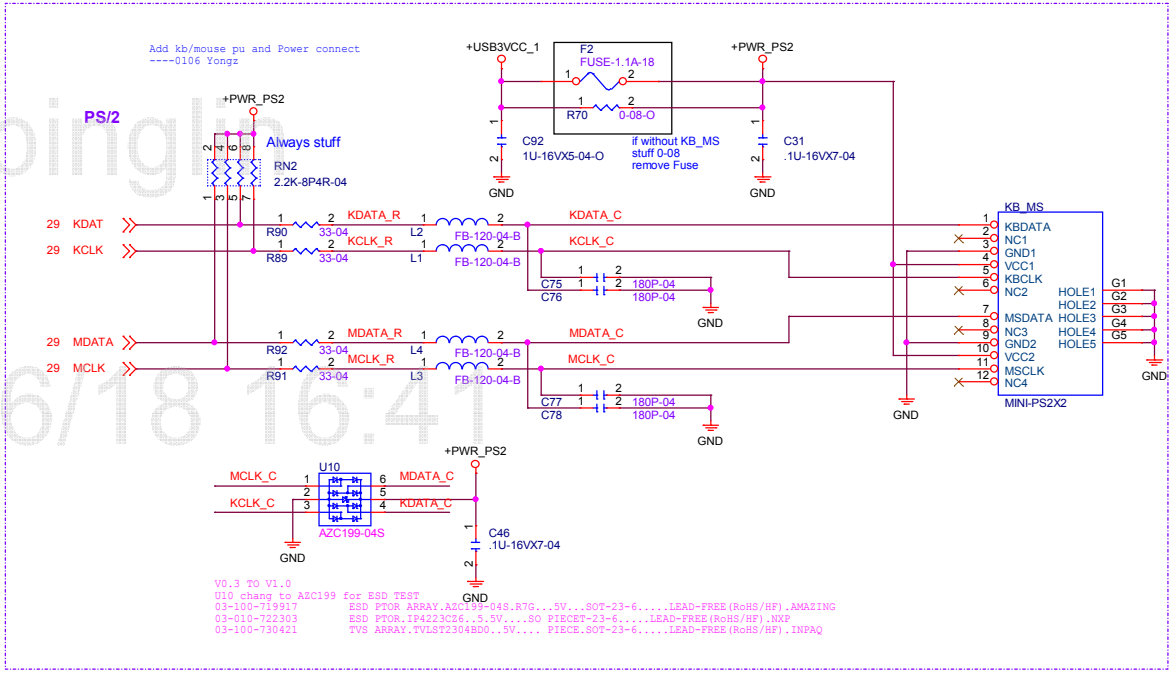
BUZZER

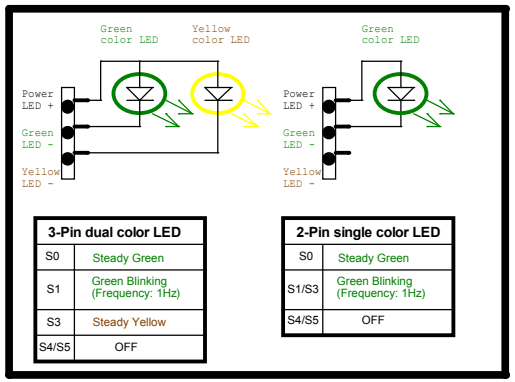


Power LED



PS/2





3-Pin dual color LED	
S0	Steady Green
S1	Green Blinking (Frequency: 1Hz)
S3	Steady Yellow
S4/S5	OFF

2-Pin single color LED	
S0	Steady Green
S1/S3	Green Blinking (Frequency: 1Hz)
S4/S5	OFF

Lenovo LED線路阻值330-06	
Source Voltage (V)	5
LED Forward Voltage (V)	1.8
BJT Vce(s) (V)	0
Pull Up Resistor (ohm)	330
LED Forward Current (A)	0.009697
Pull Up Resistor Power (R<1/10 W)	0.03103
LED Power (W)	0.017455

Elitegroup Computer Systems			
Title: F_PANEL/BUZZER			
Size: Custom	Document Number: BSWD-LM		Rev: V1.0
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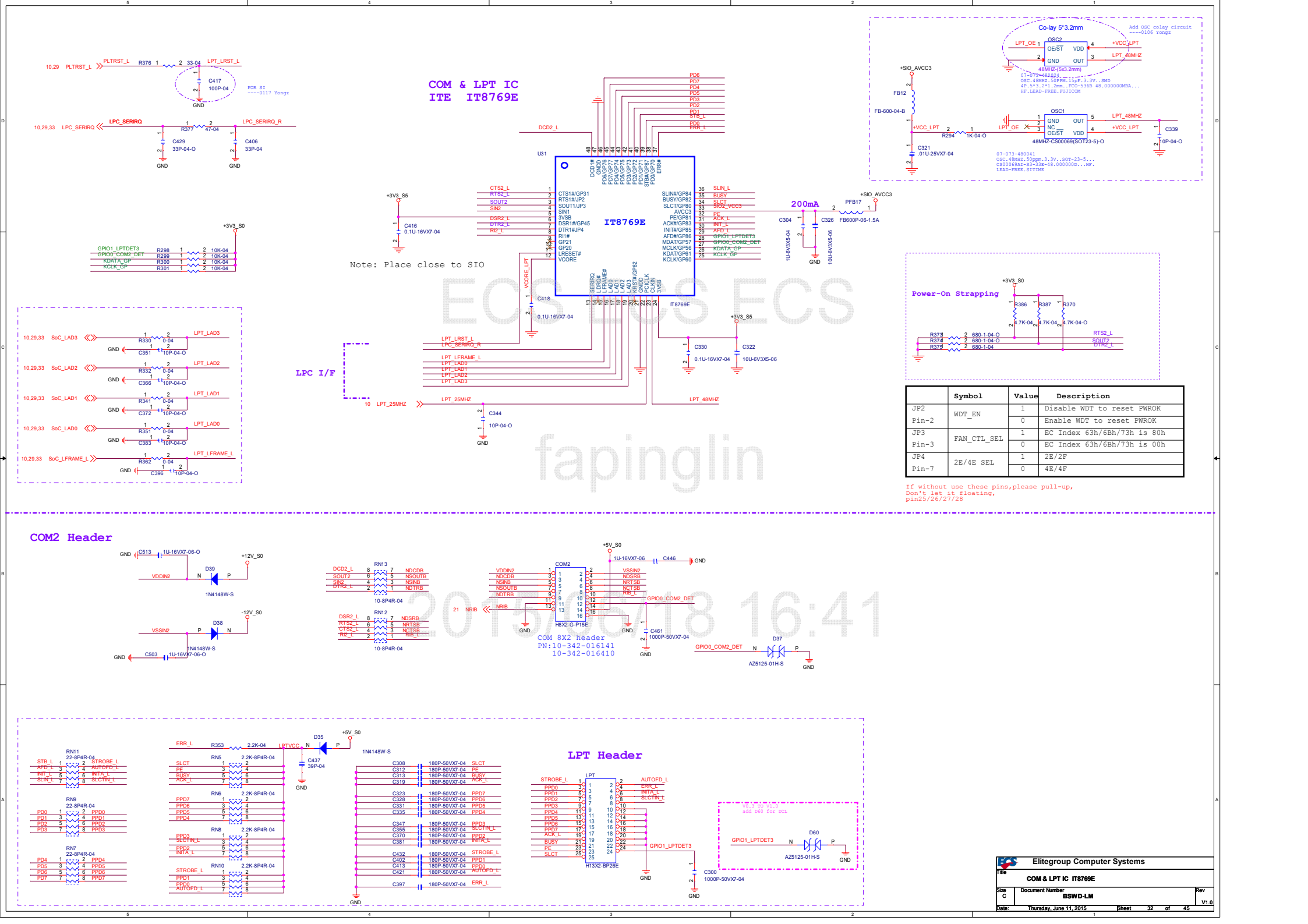

	Symbol	Value	Description
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-2		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
Pin-3		0	EC Index 63h/6Bh/73h is 00h
JP4	2E/4E SEL	1	2E/2F
Pin-7		0	4E/4F

Title	Elitegroup Computer Systems		
	COM & LPT IC IT8769E		
Size C	Document Number BSWD-LM		Rev V1.0
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TPM Circuit Reserve

TPM

	Ra	Rb	Rc	Rd	Re	Rf	Rg	Rh	Ri
ST	X	X	X	X	X	X	V	V	X
Nuvoton	V	X	V	V	X	X	V	V	X
Nationz	X	V	V	V	X	X	V	V	X
Infineon	X	X	V	V	X	X	V	V	V
ST TPM SPI	X	X	X	X	V	X	X	X	X
Nuvoton	V	X	X	V	V	V	X	V	X

ST332P24AR28PVSP 1.2
02-440-028264
NPCT650LA0WX 1.2
83-212-000352
Z32H320TC-LPC-T28-233 2.0
SLB9665TT 2.0
83-212-000203
ST33HTPM0028ASTL 1.2
83-212-000302
NPCT652LA0WX
SPITPM 1.2 83-212-000350

7 TPM_DET — TPM_DET — Rg — R676 0-04-O — TPCM_SERIRQ
10,29,32 LPC_SERIRQ — LPC_SERIRQ
10,29,32 SOC_LAD3 — R629 0-04-O — LPC_LAD3
10,29,32 SOC_LAD2 — R628 0-04-O — LPC_LAD2
10,29,32 SOC_LAD1 — R626 0-04-O — LPC_LAD1
10,29,32 SOC_LAD0 — R627 0-04-O — LPC_LAD0

+LPC_PWR — Ri — R718 0-04-O — TPM_VS1

U43 NPCT650LAAWX-O

1	GPIO1	LPCPD#	28
2	GPIO2	SERIRQ	27
3	NC3	LAD0	26
4	GND	GND	25
5	3VSB	3V	24
6	GPIO6	LAD1	23
7	PP	LFRAME#	22
8	TESTI	LCLK	21
9	TESTBI/GPIO	LAD2	20
10	3V	3V	19
11	GND	GND	18
12	NC12	LAD3	17
13	NC13	LRESET#	16
14	NC14	CLKRUN#/GPIO	15

TS_VDD_C
LPCPDL — R672 Rg 0-04-O — LPCPD_L 10
TPCM_SERIRQ
LPC_LAD0
TPMGND1 — R666 Rd 0-04-O — GND
LPC_LAD1
TPM_LFRAME_L — R659 Rg 0-04-O — SOC_LFRAME_L 10,29,32
CLK_TPM_25MHZ — R654 Rg 0-04-O — TPM_25MHZ 10
LPC_LAD2
TS_VDD_B — R642 Rd 0-04-O — +LPC_PWR
LPC_LAD3
LPC_RST — R625 Rg 33-04-O — SIO_PCIRST3_L 26,29
TPM_CLKRUN_L — R624 Rd 0-04-O
C666 10P-04-O GND
C645 33P-04-O GND
TPM_GND
R641 1 Rh 2 0-04-O GND

Infineon N/A

+3V3_S5 — R663 Rd 0-04-O — TPM_VS1
Reserve
GND — R652 10K-04-O — TPM_PP
+LPC_PWR — R661 10K-04-O
GND — R643 10K-04-O — TPM_BADD
+LPC_PWR — R675 0-04-O — TS_VDD_A
GND — R623 Rg 0-04-O — TPMGND
Rh

On-board TPM detect

+1V8_S5
TPM_DET 2 — RJ10(2-3) 1K-04
GND

Hi with on-board TPM
Low W/O on-board TPM

+3V3_S5 — C696 10U-6V3X5-06-O — C692 1U-16VX7-04-O — GND
Close to Chip. Close to Pin5.

+3V3_S0 — C709 10U-6V3X5-06-O — GND
Close to Chip.

TS_VDD_B — C654 .1U-16VX7-04-O — GND
Close to Pin19.

TS_VDD_C — C686 .1U-16VX7-04-O — GND
Close to Pin24.

TS_VDD_A — C695 .1U-16VX7-04-O — GND
Close to Pin10.

LPC COLAY SPI

Re

7 SOC_SPI_DO — SOC_SPI_DO — R605 0-04-O — LPC_LAD0
7 SOC_SPI_DI — SOC_SPI_DI — R597 0-04-O — LPC_LAD1
7 SOC_SPI_CS2 — SOC_SPI_CS2 — R611 33-04-O — TPM_LFRAME_L
7 SOC_SPI_CLK — SOC_SPI_CLK — R609 0-04-O — CLK_TPMR_25MHZ
R715 0-04-O — CLK_TPM_25MHZ

TPCM_SERIRQ — R674 10K-04-O — GND

+LPC_PWR+1V8_S5
R668 0-O
R669 0-O — TS_VDD_C

+1V8_S5
Rf
R685 0-O — TS_VDD_A
R650 0-O — TS_VDD_B
R662 3.3K-04-O — TPM_LFRAME_L
R753 3.3K-04-O — LPC_LAD2

LPC_RST — R751 0-04-O — SOC_PLTRST_L — SOC_PLTRST_L 10

LPC_DEBUG

+LPC_PWR
LPC_DEBUG
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
DBG_LFRAME_L
LPC_DB_RST
LPC_DB_25MHZ
R760 0-04 — SOC_LFRAME_L
SIO_PCIRST3_L
R750 0-04 — LPC_25MHZ — LPC_25MHZ 10
R749 0-04
H5X2-BK-P10E-P2.0
C812 1U-16VX7-04
C799 10P-04-O GND
C798 22P-04-O GND

+12V_S0
Change power net from 3V3_S0 for IC leakage voltage
--------0106 Yongz
R61 10K-04
TPM_EN
+3V3_S0
S D LPC_PWR_S
QSW4
PN:03-050-530678 APM2306AC-TRG-S
SR60 0-X-O
SR59 0-X-O
+3V3_S5

+LPC_PWR
C37 10U-6V3X5-06
C220 470P-50VX7-04
GND

Elitegroup Computer Systems		
Title: TPM/TCM		
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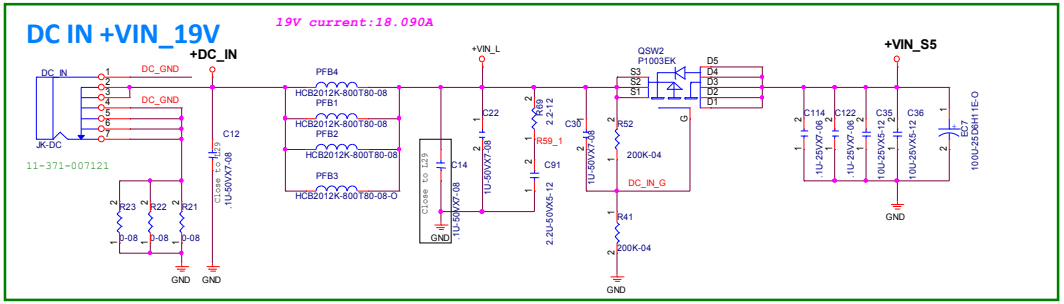
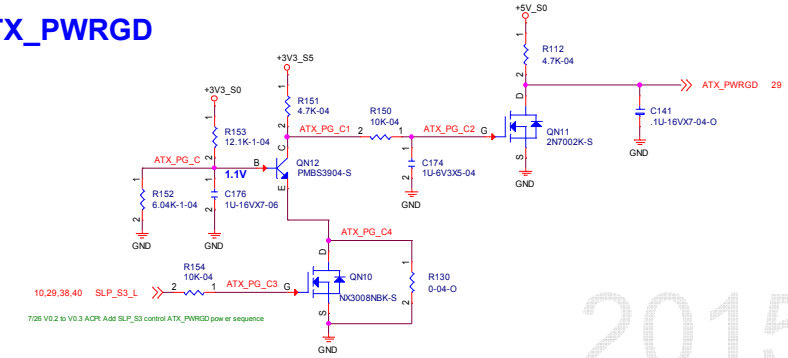
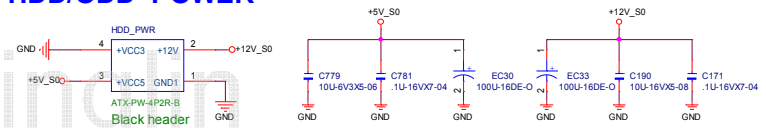
DC IN +VIN_19V



ATX_PWRGD

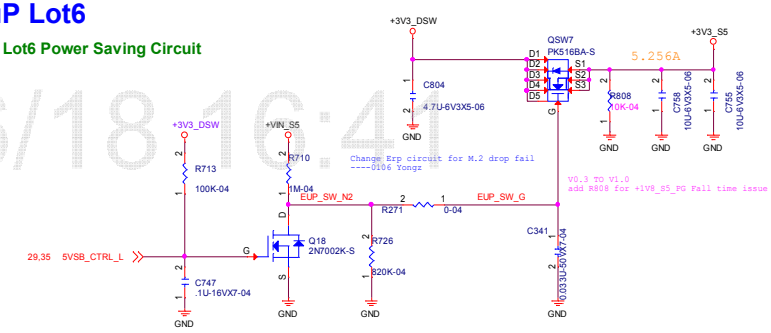


HDD/ODD POWER



EuP Lot6

EuP Lot6 Power Saving Circuit



EUP Lot 6.0 state

	G3	Deep S5	S5	S0	S3
5VSB_CTRL_L	L	H	L	L	L
+5V_S5	OFF	OFF	ON	ON	ON
+3V3_S5	OFF	OFF	ON	ON	ON

check sequence control

Elitegroup Computer Systems			
Title: DC-19V/HDD POWER			
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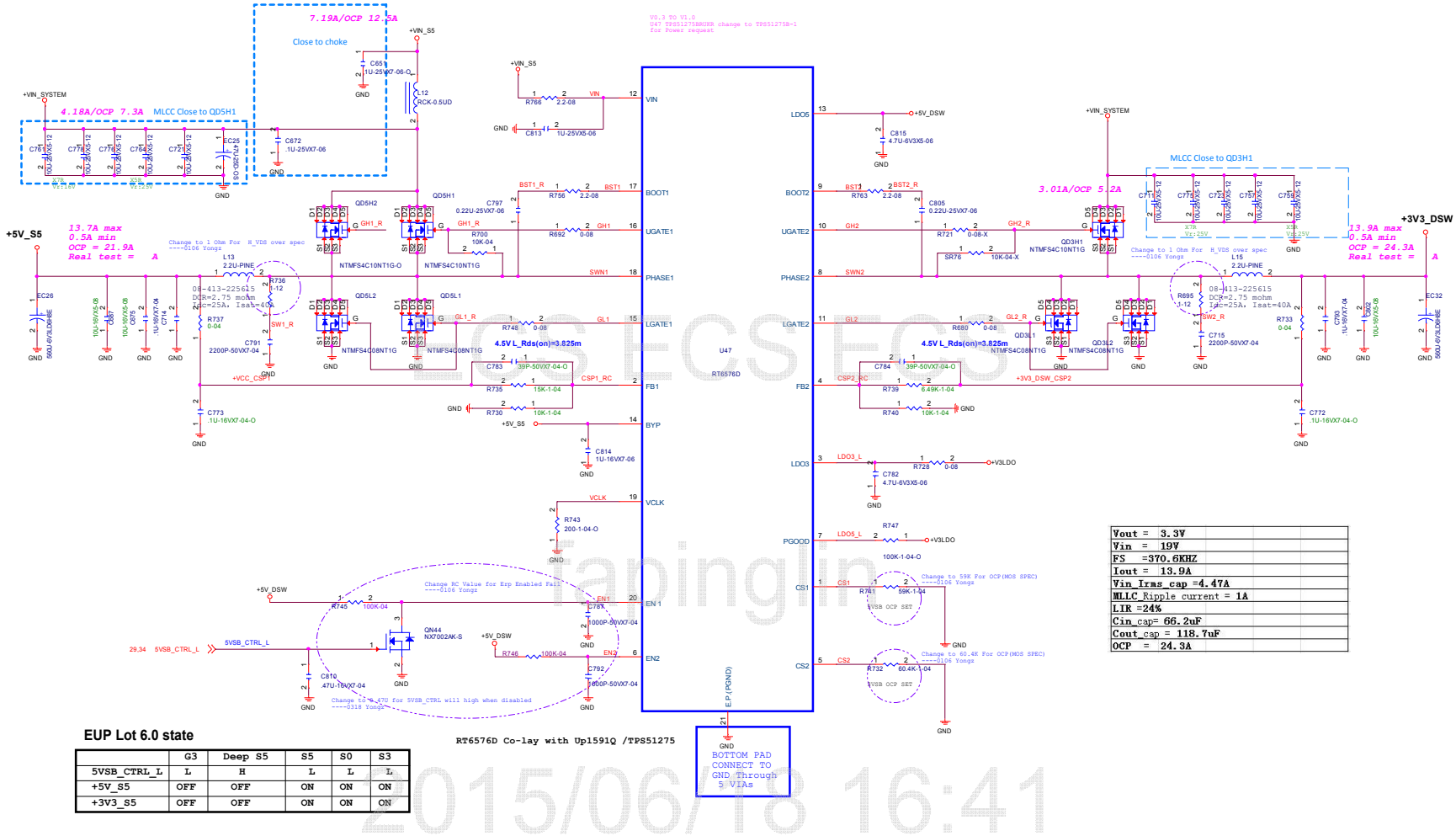
$V_{ILIM} = (R_{ILIM} \times 10uA) / 10 = I_{ILIM} \times R_{DS(ON)}$

$R_{ILIM} = (I_{ILIM} \times R_{DS(ON)}) \times 10 / 10uA$

+5VSB & +3VSB



P36 +5V_S5:	RT6576D
Vout =	5V
Vin =	19V
FS	=303.2KHZ
Iout =	13.7A
Vin_Irms_cap	=5.1A
MLLC_Ripple current =	1A
LIR	=38%
Cin_cap=	73.5uF
Cout_cap =	73.78uF
OCP =	21.9A

Vout =	3.3V
Vin =	19V
FS	=370.6KHZ
Iout =	13.9A
Vin_Irms_cap	=4.47A
MLLC_Ripple current =	1A
LIR	=24%
Cin_cap=	66.2uF
Cout_cap =	118.7uF
OCP =	24.3A

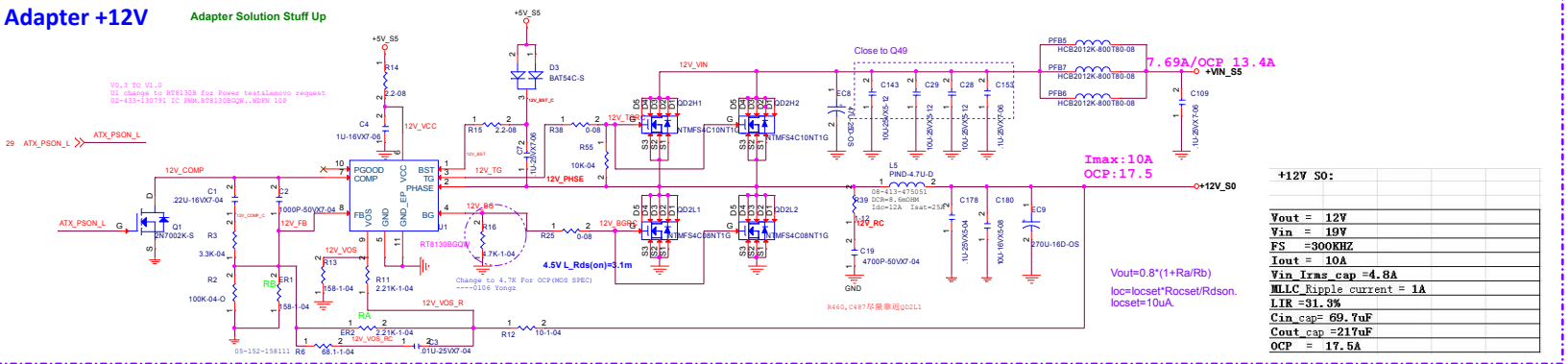
EUP Lot 6.0 state

	G3	Deep S5	S5	S0	S3
5VSB_CTRL_L	L	H	L	L	L
+5V_S5	OFF	OFF	ON	ON	ON
+3V3_S5	OFF	OFF	ON	ON	ON

RT6576D Co-lay with Up1591Q /TPS51275

Adapter +12V

Adapter Solution Stuff Up



+12V_S0:	
Vout =	12V
Vin =	19V
FS	=300KHZ
Iout =	10A
Vin_Irms_cap	=4.8A
MLLC_Ripple current =	1A
LIR	=31.3%
Cin_cap=	69.7uF
Cout_cap	=217uF
OCP =	17.5A

Elitegroup Computer Systems		
Title: DC-DC_VIN/5VSB/3VSB/12V		
Size: Custom	Document Number: BSWD-LM	Rev: V1.0
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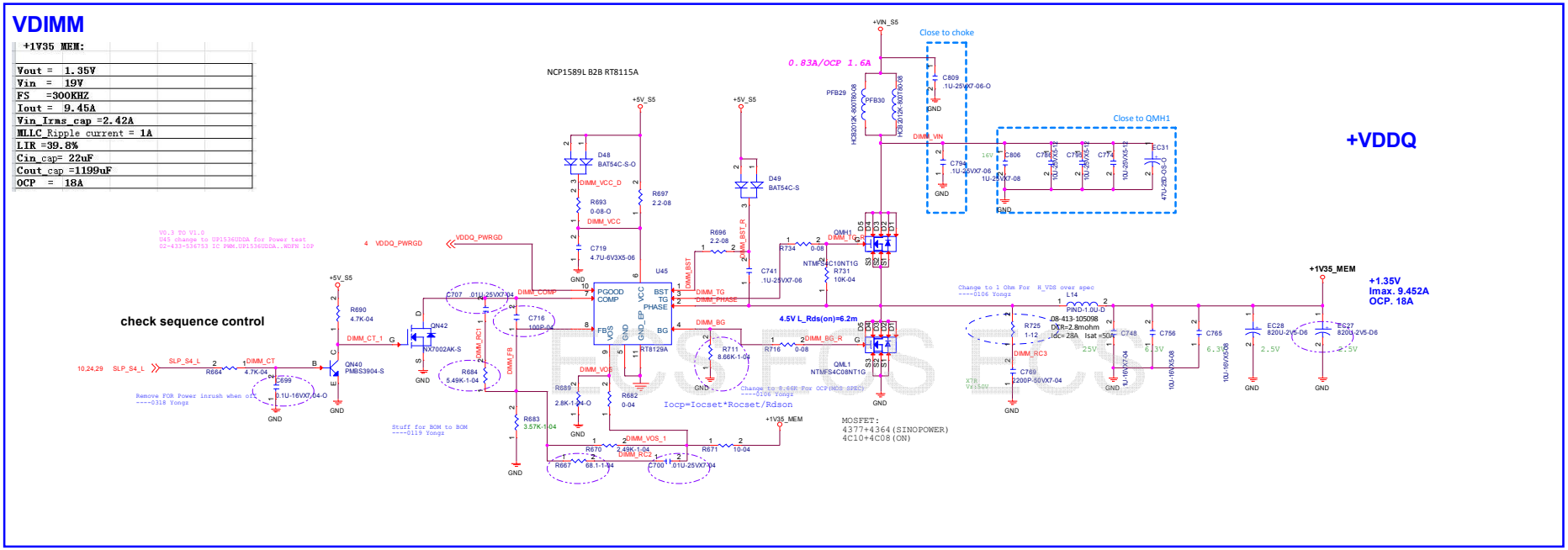
VDIMM&VTT_DDR

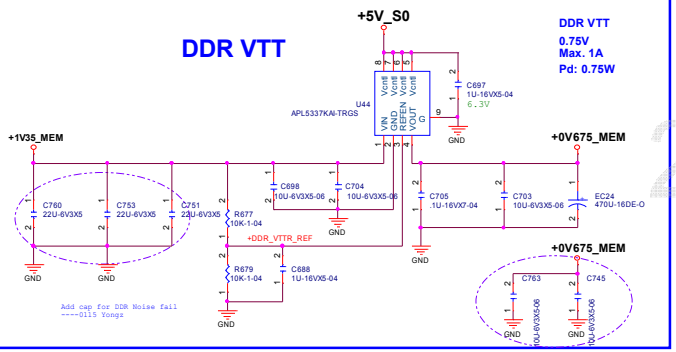
VDIMM

+1V35 MEM:

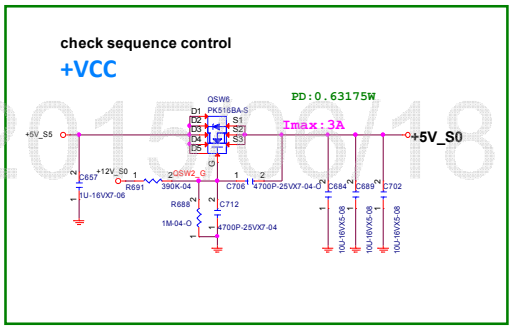
Vout =	1.35V
Vin =	19V
FS	=300KHZ
Iout =	9.45A
Vin_Irms_cap	=2.42A
MLLC_Ripple current	= 1A
LIR	=39.8%
Cin_cap	= 22uF
Cout_cap	=1199uF
OCP =	18A



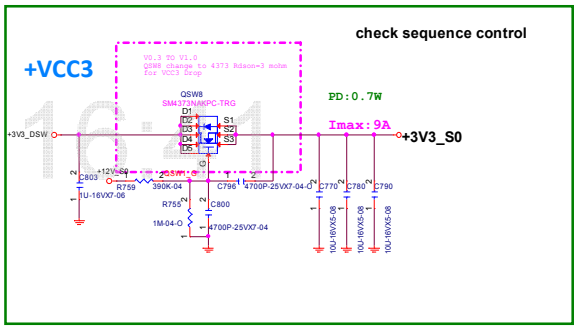
DDR VTT



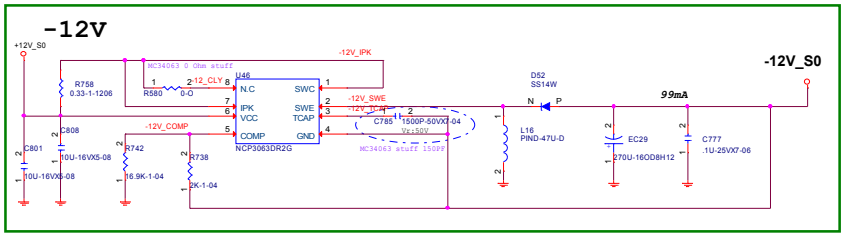
check sequence control +VCC



check sequence control +VCC3



-12V



Elitegroup Computer Systems			
Title	DC-DIMM/DDR_VTT		
Size: Custom	Document Number: BSWD-LM		Rev: V1.0
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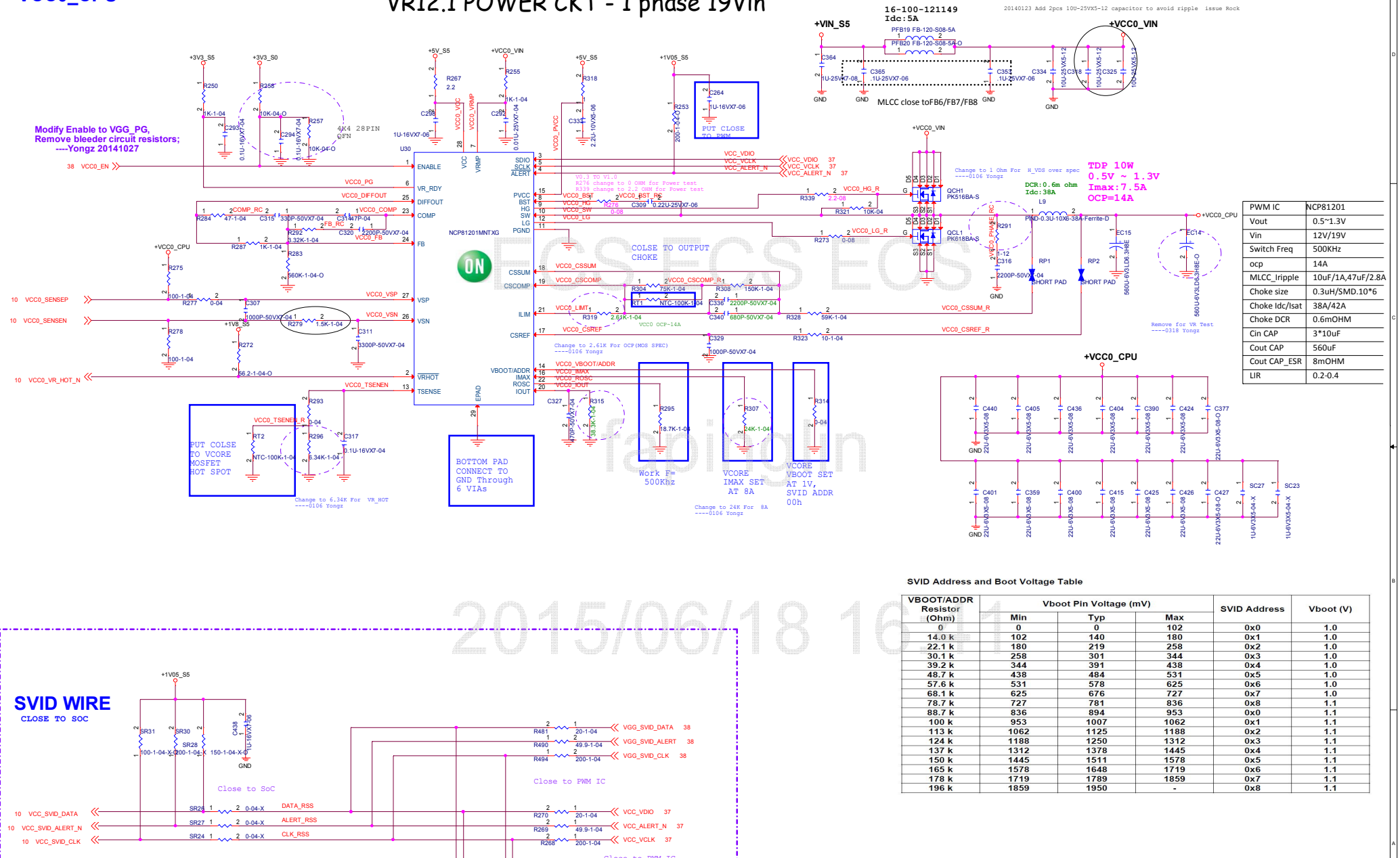
+VCC0_CPU

VR12.1 POWER CKT - 1 phase 19Vin



PWM IC	NCP81201
Vout	0.5~1.3V
Vin	12V/19V
Switch Freq	500KHz
ocp	14A
MLCC_Iripple	10uF/1A,47uF/2.8A
Choke size	0.3uH/SMD.10*6
Choke Idc/Isat	38A/42A
Choke DCR	0.6mOHM
Cin CAP	3*10uF
Cout CAP	560uF
Cout CAP_ESR	8mOHM
LIR	0.2-0.4

SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

SVID WIRE

CLOSE TO SOC

Elitegroup Computer Systems

Title	DC-CPU_VCC0		
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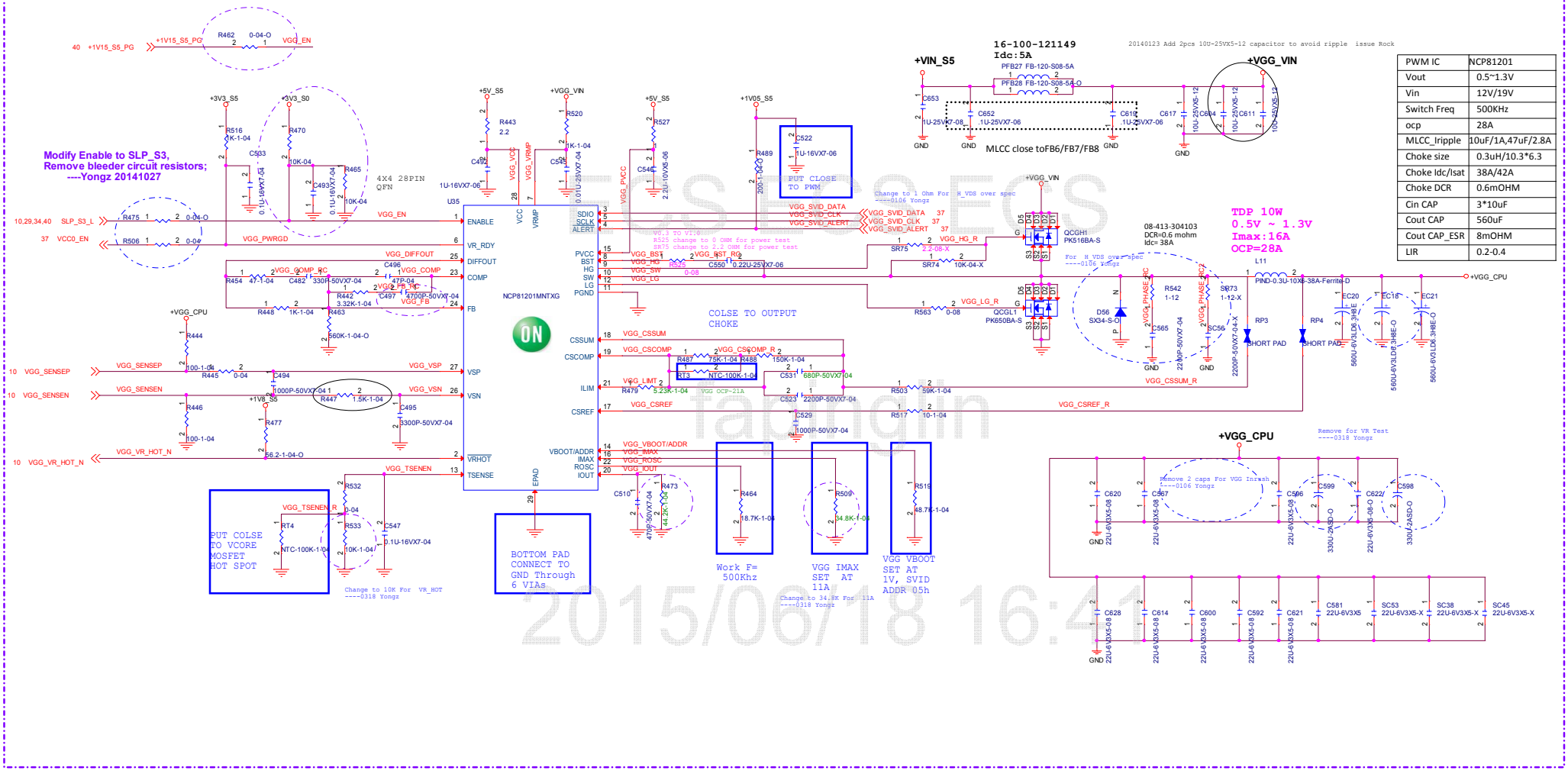
+VGG_CPU



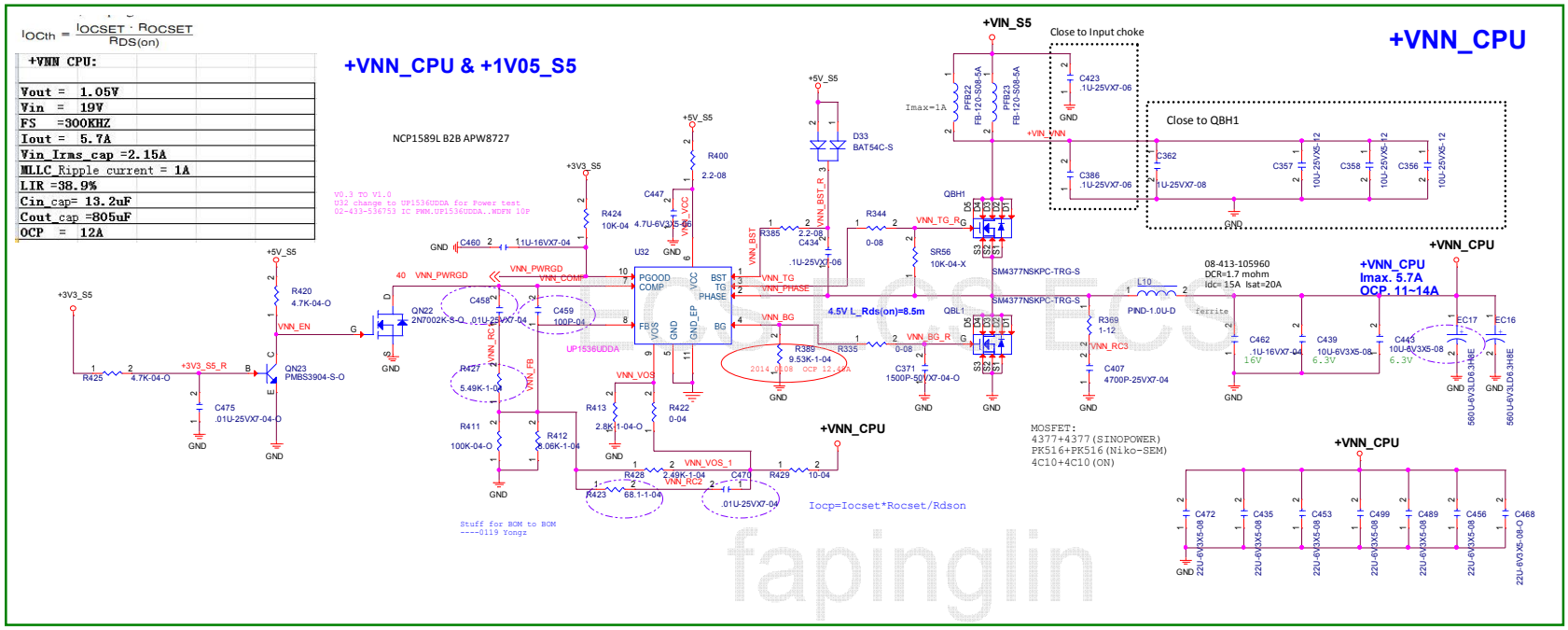
PWM IC	NCP81201
Vout	0.5~1.3V
Vin	12V/19V
Switch Freq	500KHz
ocp	28A
MLCC_ripple	10uF/1A,47uF/2.8A
Choke size	0.3uH/10.3*6.3
Choke Idc/Isat	38A/42A
Choke DCR	0.6mOHM
Cin CAP	3*10uF
Cout CAP	560uF
Cout CAP_ESR	8mOHM
LIR	0.2-0.4

Elitegroup Computer Systems

Title: DC-CPU_VGG

Size: C | Document Number: BSWD-LM | Rev: V1.0

Date: Thursday, June 11, 2015 | Sheet 38 of 45



$$I_{OCth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}}$$

+VNN CPU:

Vout =	1.05V
Vin =	19V
FS =	300KHZ
Iout =	5.7A
Vin_Irms_cap =	2.15A
MLLC_Ripple current =	1A
LIR =	38.9%
Cin_cap=	13.2uF
Cout_cap =	805uF
OCP =	12A

Elitegroup Computer Systems			
Title: DC-CPU_VNN			
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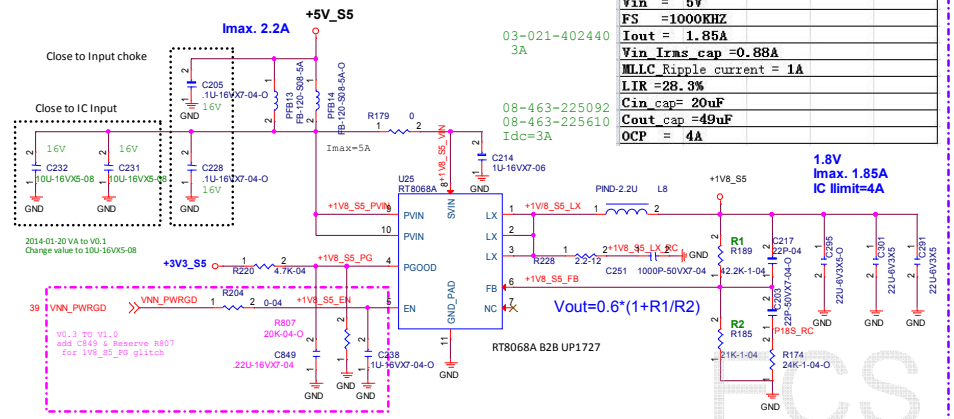
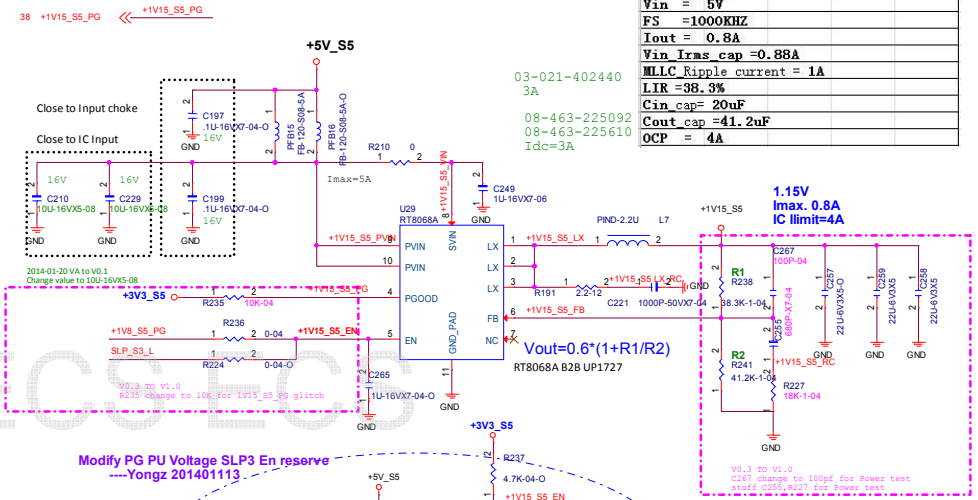
+1V8_S5



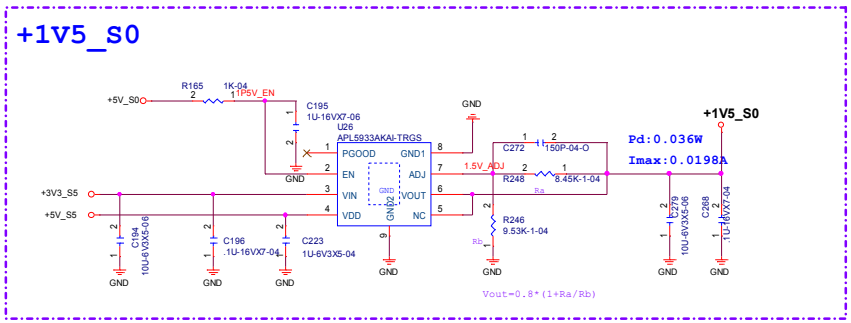
+1V8_S5:	
Vout =	1.8V
Vin =	5V
FS	=1000KHZ
Iout =	1.85A
Vin_Irms_cap	=0.88A
MLLC_Ripple current	= 1A
LIR	=28.3%
Cin_cap	= 20uF
Cout_cap	=49uF
OCP =	4A

+1V15_S5（+1V15_S0）

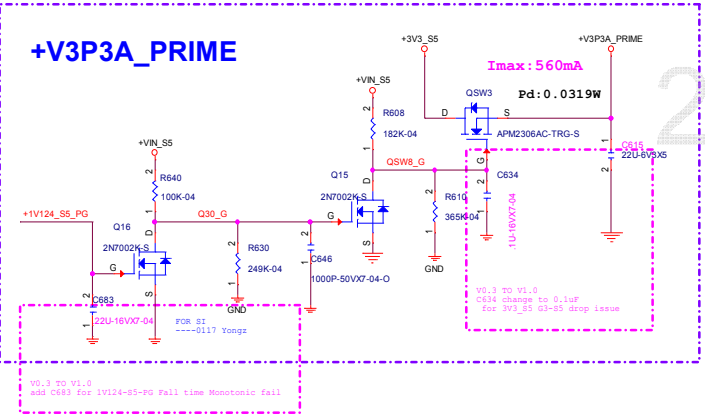


+1V15_S5:	
Vout =	1.15V
Vin =	5V
FS	=1000KHZ
Iout =	0.8A
Vin_Irms_cap	=0.88A
MLLC_Ripple current	= 1A
LIR	=38.3%
Cin_cap	= 20uF
Cout_cap	=41.2uF
OCP =	4A

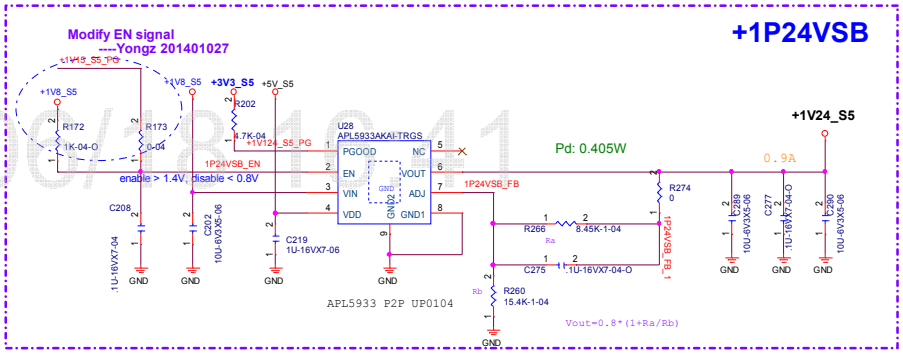
+1V5_S0



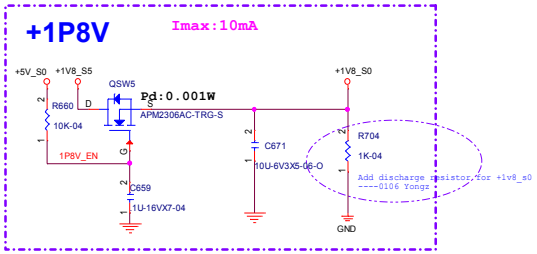
+V3P3A_PRIME



+1P24VSB



+1P8V



Elitegroup Computer Systems			
Title	DC-V1P05SB&V1P15SB		
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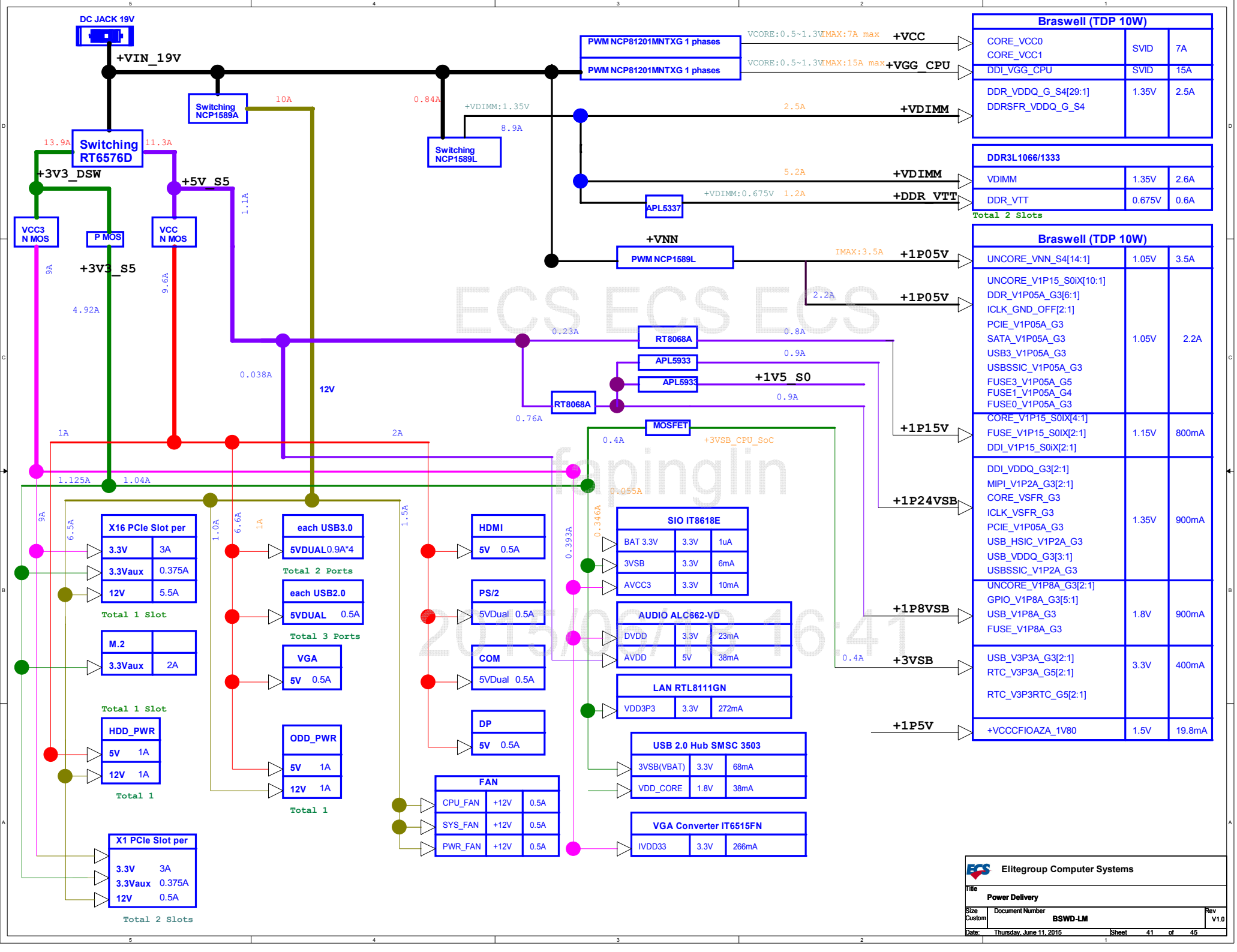
DC JACK 19V
+VIN_19V
Switching NCP1589A
10A
0.84A
+VDIMM:1.35V
8.9A
Switching NCP1589L
13.9A
Switching RT6576D
11.3A
+3V3_DSW
+5V_S5
1.1A
VCC3 N MOS
P MOS
VCC N MOS
9A
+3V3_S5
4.92A
9.6A
0.038A
12V
1A
2A
1.125A
1.04A
PWM NCP81201MNTXG 1 phases
PWM NCP81201MNTXG 1 phases
VCORE:0.5~1.3V IMAX:7A max
+VCC
VCORE:0.5~1.3V IMAX:15A max
+VGG_CPU
2.5A
+VDIMM
5.2A
+VDIMM
+VDIMM:0.675V 1.2A
+DDR_VTT
APL5337
+VNN
PWM NCP1589L
IMAX:3.5A
+1P05V
2.2A
+1P05V
0.23A
RT8068A
0.8A
0.9A
APL5933
APL5933
+1V5_S0
0.9A
RT8068A
0.76A
MOSFET
0.4A
+3VSB_CPU_SoC
+1P15V
0.055A
+1P24VSB
0.346A
0.393A
1.5A
1.0A
6.6A
1A
6.5A
9A
X16 PCIe Slot per
3.3V 3A
3.3Vaux 0.375A
12V 5.5A
Total 1 Slot
M.2
3.3Vaux 2A
Total 1 Slot
HDD_PWR
5V 1A
12V 1A
Total 1
X1 PCIe Slot per
3.3V 3A
3.3Vaux 0.375A
12V 0.5A
Total 2 Slots
each USB3.0
5VDUAL 0.9A*4
Total 2 Ports
each USB2.0
5VDUAL 0.5A
Total 3 Ports
VGA
5V 0.5A
ODD_PWR
5V 1A
12V 1A
Total 1
HDMI
5V 0.5A
PS/2
5VDual 0.5A
COM
5VDual 0.5A
DP
5V 0.5A
FAN
CPU_FAN +12V 0.5A
SYS_FAN +12V 0.5A
PWR_FAN +12V 0.5A
SIO IT8618E
BAT 3.3V 3.3V 1uA
3VSB 3.3V 6mA
AVCC3 3.3V 10mA
AUDIO ALC662-VD
DVDD 3.3V 23mA
AVDD 5V 38mA
LAN RTL8111GN
VDD3P3 3.3V 272mA
USB 2.0 Hub SMSC 3503
3VSB(VBAT) 3.3V 68mA
VDD_CORE 1.8V 38mA
VGA Converter IT6515FN
IVDD33 3.3V 266mA
0.4A
+3VSB
+1P8VSB
+1P5V
Braswell (TDP 10W)
CORE_VCC0
CORE_VCC1 SVID 7A
DDI_VGG_CPU SVID 15A
DDR_VDDQ_G_S4[29:1] 1.35V 2.5A
DDRSFR_VDDQ_G_S4
DDR3L1066/1333
VDIMM 1.35V 2.6A
DDR_VTT 0.675V 0.6A
Total 2 Slots
Braswell (TDP 10W)
UNCORE_VNN_S4[14:1] 1.05V 3.5A
UNCORE_V1P15_S0iX[10:1]
DDR_V1P05A_G3[6:1]
ICLK_GND_OFF[2:1]
PCIE_V1P05A_G3
SATA_V1P05A_G3
USB3_V1P05A_G3
USBSSIC_V1P05A_G3
FUSE3_V1P05A_G5
FUSE1_V1P05A_G4
FUSE0_V1P05A_G3
1.05V 2.2A
CORE_V1P15_S0IX[4:1]
FUSE_V1P15_S0IX[2:1]
DDI_V1P15_S0iX[2:1]
1.15V 800mA
DDI_VDDQ_G3[2:1]
MIPI_V1P2A_G3[2:1]
CORE_VSFR_G3
ICLK_VSFR_G3
PCIE_V1P05A_G3
USB_HSIC_V1P2A_G3
USB_VDDQ_G3[3:1]
USBSSIC_V1P2A_G3
1.35V 900mA
UNCORE_V1P8A_G3[2:1]
GPIO_V1P8A_G3[5:1]
USB_V1P8A_G3
FUSE_V1P8A_G3
1.8V 900mA
USB_V3P3A_G3[2:1]
RTC_V3P3A_G5[2:1]
RTC_V3P3RTC_G5[2:1]
3.3V 400mA
+VCCCFIOAZA_1V80 1.5V 19.8mA
ECS ECS ECS
fapinglin
2015/06/12 16:41
Elitegroup Computer Systems
Title
Power Delivery
Size Custom
Document Number
BSWD-LM
Rev V1.0
Date: Thursday, June 11, 2015
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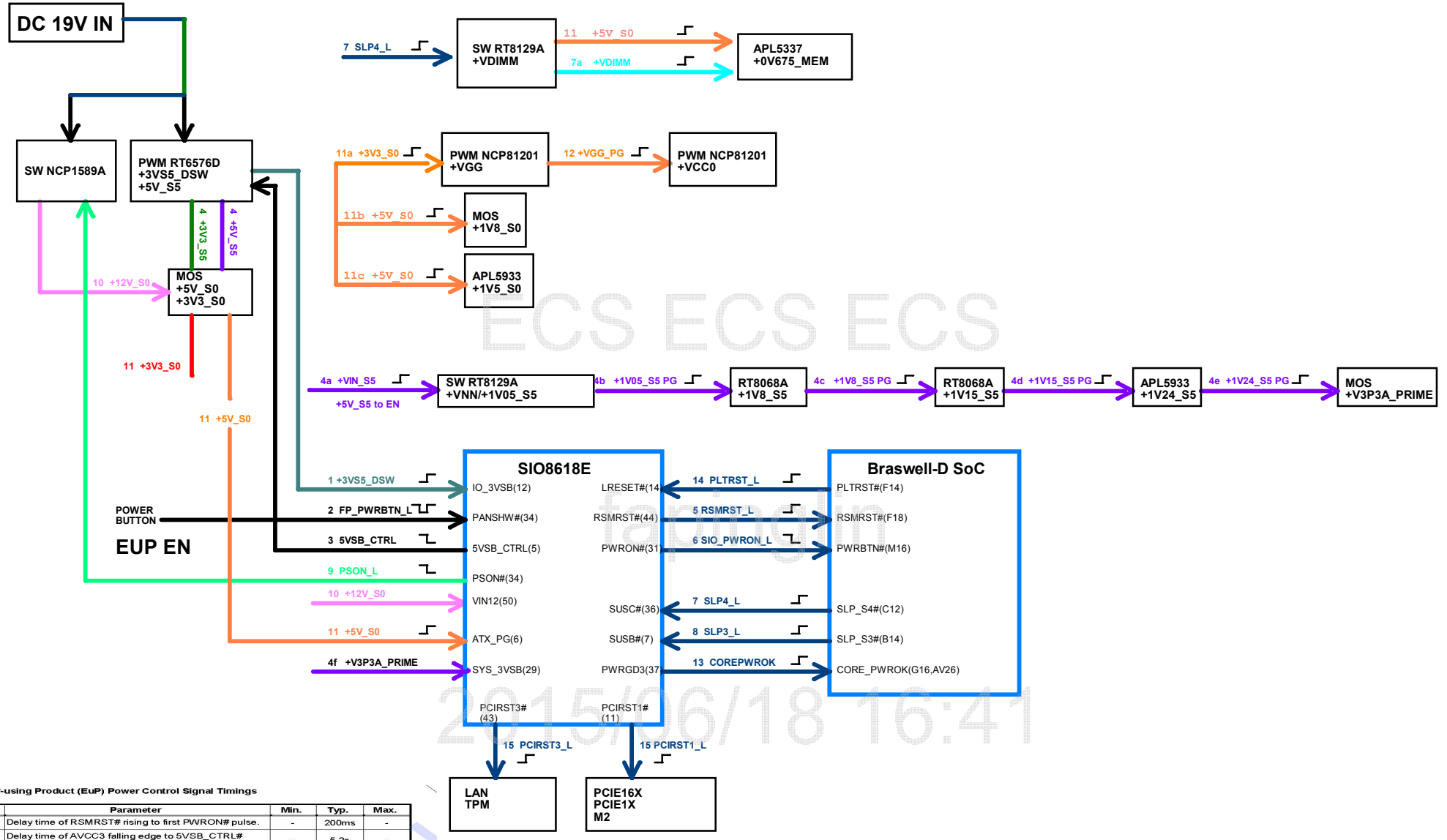
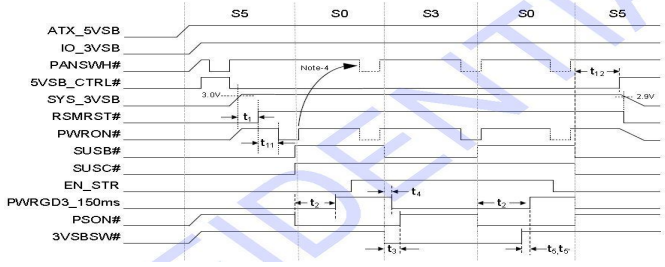


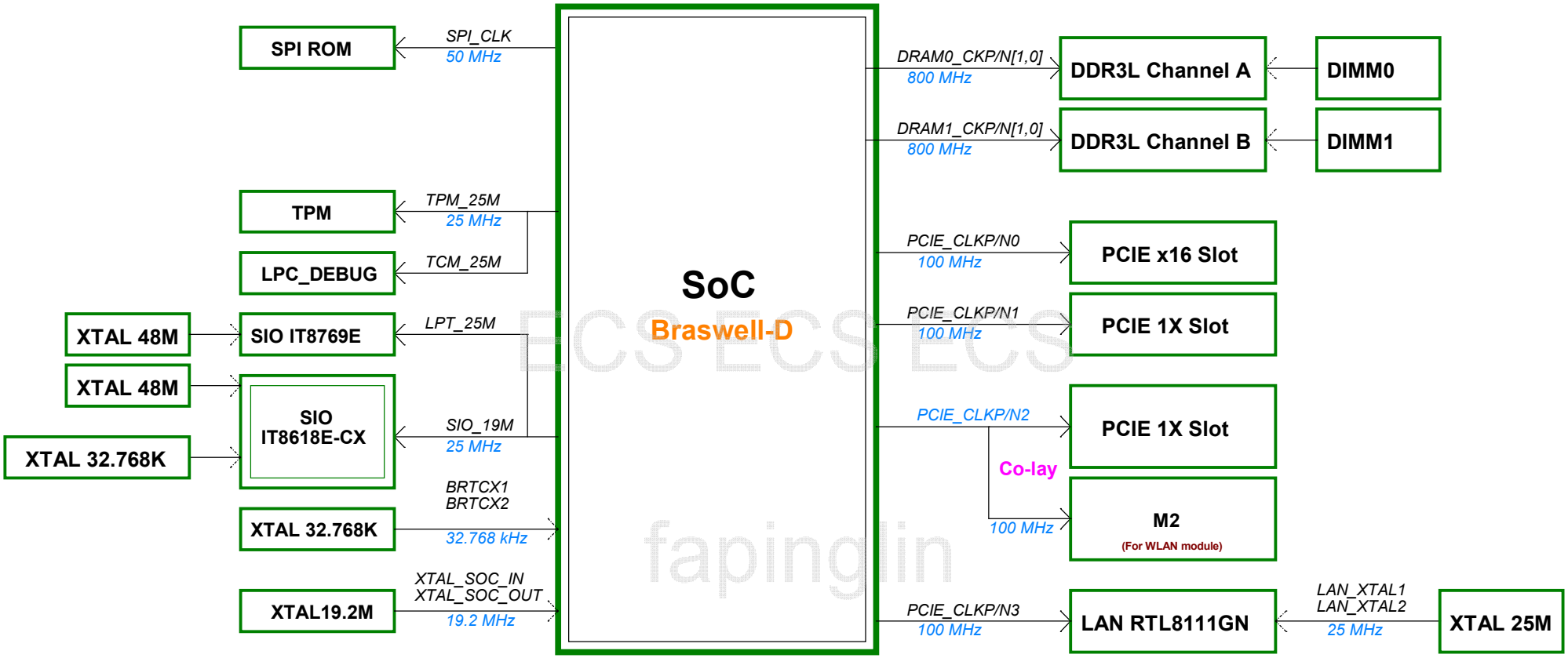
.10 Energy-using Product (EuP) Power Control Signal Timings

Symbol	Parameter	Min.	Typ.	Max.
t_{11}	Delay time of RSMRST# rising to first PWRON# pulse.	-	200ms	-
t_{12}	Delay time of AVCC3 falling edge to 5VSB_CTRL# rising edge.	-	5.2s	-

Figure 11-11. EuP Function Signal Timings



ECS Elitegroup Computer Systems			
Title: Power Sequence			
Size: C	Document Number: BSWD-LM		Rev: V1.0
Date: Thursday, June 11, 2015	Sheet 42 of 45		



SMBUS **Data:2014/11/25**

Function	SMBUS
DIMM0	SMBUS_MAIN
DIMM1	SMBUS_MAIN
LAN	SMBUS_STBY
PCIE1X *2	SMBUS_STBY
PCIE1X	SMBUS_STBY
PCIE16X	SMBUS_STBY
M.2	SMBUS_STBY
PCIE16X	SMBUS_STBY

Elitegroup Computer Systems

Title: Clock Distribution

Size: Custom | Document Number: BSWD-LM | Rev: V1.0

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REVISION HISTORY:

Rev	Date	Page	Notes
V0.1	2014/07/26	48	First Release
V0.1.	2014/11/25	46	Base on V0.1 Modify Spec and PCB size from 244*244 to 220*200
V0.2	2015/01/12	46	Base on V0.1. Modify ET Issue solution for SDV 1、Change USB2.0 HUB location near 16x to decrease routing length 2、Add delay circuit for Audio 3V3_S0 for 1V5_S5 voltage leakage 3、Modify Erp circuit for M2 Max loading Fail 4、Remove SIO colay circuit 5、Add ITE8769 OSC colay 6、Add 3V_S0,5V_S5 power channel for Max loading Fail 7、Change the location of DDR_VERF VIN connection; 8、Change the USB debug port to the low one 9、Change the LAN IC location for USBHUB 10、Add the level shifter for VGA CONV
V0.3	2015/03/19	45	Base on V0.2 Modify SDV Issue solution for SIT 1、Remove Charge IC and merge charge power with FP 2、Modify HDMI and VGA DDC diode and add Diode for HDMI ESD power for leakage voltage 3、Add SIO colay for IT8609E 4、Modify Erp circuit for 5VS5_CTRL and 5VS5_EN high un-nomal 5、Reserve MONO_OUT,THER_HD,TPM,DIMM2, 6、Add MOS control F_usb port3 for EN/DIS

Elitegroup Computer Systems			
Title: Revision History			
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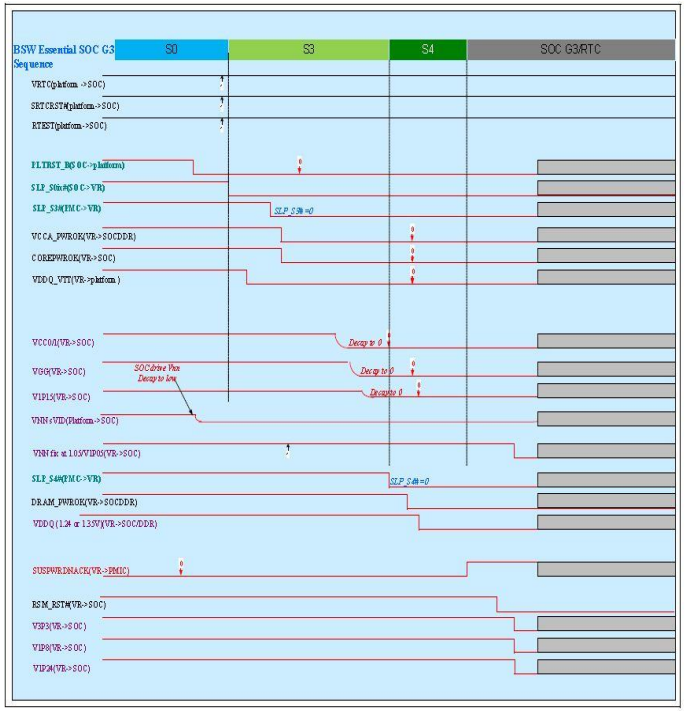
Table 35. Power and Ground Pins (Sheet 1 of 2)

Power Rails	Platform Power	Nominal Voltage	First Off State
CORE_V1P05_S3	V1P05S	1.05 V	S3
CORE_VCC_S0iX	VCC	Variable	S0ix
CORE_VCC_SENSE	-	-	-
CORE_VSS_SENSE	-	-	-
DDI_V1P0_S0iX	V1P0Sx	1.0 V	S0ix
DRAM_V1P0_S0iX	V1P0Sx	1.0 V	S0ix
DRAM_V1P35_S0iX_F1	VSFR	1.35 V	S0ix
DRAM_VDD_S4	V1P35U	1.35 V	S4
GPIO_V1P0_S3	V1P0S	1.0 V	S3
HDA_LPE_V1P5V1P8_S3	VAUD	1.5/1.8 V	S3
ICLK_V1P35_S3_F1		1.35 V	S3
ICLK_V1P35_S3_F2		1.35 V	S3
LPC_V1P8V3P3_S3	VLPC	1.8/3.3 V	S3
PCIE_SATA_V1P0_S3	VPCIESATA	1.0 V	S3
PCIE_V1P0_S3	VPCIESATA	1.0 V	S3
PCU_V1P8_G3	V1P8A	1.8 V	G3
PCU_V3P3_G3	V3P3A	3.3 V	G3
PMC_V1P8_G3	V1P8A	1.8 V	G3
RTC_VCC	VRTC	2.0-3.3	(normally battery backed)
SATA_V1P0_S3	VPCIESATA	1.0 V	S3
SD3_V1P8V3P3_S3	VSDIO	1.8/3.3 V	S3
SIO_V1P8_S3	V1P8S	1.8 V	S3
SVID_V1P0_S3	V1P0S	1.0 V	S3
UNCORE_V1P0_G3	V1P0A	1.0 V	G3
UNCORE_V1P0_S0iX	V1P0Sx	1.0 V	S0ix
UNCORE_V1P0_S3	V1P0S	1.0 V	S3
UNCORE_V1P35_S0iX_F1	VSFR	1.35 V	S0ix
UNCORE_V1P35_S0iX_F2	VSFR	1.35 V	S0ix
UNCORE_V1P35_S0iX_F3	VSFR	1.35 V	S0ix
UNCORE_V1P35_S0iX_F4	VSFR	1.35 V	S0ix
UNCORE_V1P35_S0iX_F5	VSFR	1.35 V	S0ix
UNCORE_V1P35_S0iX_F6	VSFR	1.35 V	S0ix
UNCORE_V1P8_G3	V1P8A	1.8 V	G3
UNCORE_V1P8_S3	V1P8S	1.8 V	S3

Table 35. Power and Ground Pins (Sheet 2 of 2)

Power Rails	Platform Power	Nominal Voltage	First Off State
UNCORE_VNN_S3	VNN	Variable	S3
UNCORE_VNN_SENSE	-	-	-
USB_HSIC_V1P24_G3*	V1P24A	1.24 V	G3
USB_V1P0_S3	V1P0S	1.0 V	S3
USB_V1P8_G3	V1P8A	1.8 V	G3
USB_V3P3_G3	VUSB2	3.3 V	G3
USB_VSSA	-	-	-
USB3_V1P0_G3	V1P0A	1.0 V	G3
VGA_V1P0_S3	V1P0S	1.0 V	S3
VGA_V1P35_S3_F1	VVGA	1.35 V	S3
VGA_V3P3_S3	VVGA_GPIO	3.3 V	S3
VSS	-	-	-
VSSA	-	-	-



Note: VIP15 (VR->SoC: V1P15 can also start to ramp down at a time similar to "VNN fix at 1.05/V1P05" ramping down.

Figure 7. RTC Power Well Timing Diagrams

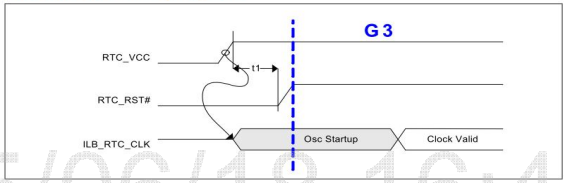


Table 47. RTC Power Well Timing Parameters

Parameter	Description	Minimum	Maximum	Units
t1	RTC_VCC to RTC_RST# de-assertion	9	-	ms

NOTES:
1. This delay is typically created from an RC circuit.
2. The oscillator startup times are component and design specific. A crystal oscillator can take several second to reach a large enough voltage swing. A silicon oscillator can have startups times <10 ms.
3. Pre-silicon estimates

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