B450 AORUS M

Revision : 1.05

2015.12.30--B.L

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Title: COVER SHEET		
Size: Custom	Document Number: B450 AORUS M	Rev: 1.05
Date: Tuesday, November 12, 2019	Sheet 1 of 38	

Model Name:B450 AORUS M

Component value change history

Version: 1.05

P-Code: U98126-0

Date	Change Item	Reason
2017.11.01	10C BOM Release. PCB: 1.01	1. update B33006 RoHS LOGO & 小版本修改 , other not change
2018.01.17	11A E-BOM Release. PCB:1.11	1. rename DR25 2. PCB cheange to Rev1.11 3. SIO OR15 NA , OR7 上件
2018.06.14	10A P-BOM Release. PCB:1.0	1. SEQUENCE CHANGE (PC34 NA, SQR2 8.2K-->39K , SQC1-->2.2u) 2. PCB cheange to Rev1.0 3. F_PANNEL (ADD MPD-) 4. M2 SOCKET SMBUS NA 5. DR38 20.5K-->18.7K
2018.08.20	10G P-BOM Release. PCB:1.01	1. Vcore SENSE 位置 2. C125 10u change to 22u 3. VINA0 change to APU_PWRGD(for summit / Pinnacle 不上DIMM時,值亮CPU DEBUD LED,應改為亮DDR DEBUG LED) 4.BRN1 change to 1K
2019.05.21	10H P-BOM Release. PCB:1.01	UPDATE NEW EC FW V684.BIN
2019.11.12	10L P-BOM PCB:1.05	1. Vcore choke Footprint 自動插件修改

VCORE	11LC5-F3500C-11R	CHOKE05U-40A-1PQ-3	11LC5-F3500C-18R	CHOKE-INCG109-R80M-JJ1W-AT
SOC	11LC5-F5300C-01R	CHOKE05U-40A-1PQ-3	11LC5-F5300C-08R	CHOKE-INCG109-R30M-JJ1W-AT
VDDIO_MEM	11LC5-M3100B-2*R	CHOKE05U-40A-1PQ-3	11LC5-M3100B-28R/2	CHOKE05U-40A-1PQ-AT

Circuit or PCB layout change for next version

Date	Change Item	Reason
		1. Add USB 3.1 2nd re-driver. 2. Fix VDDCR_SOC_S5 power issue. 3. PWM/DRIVER change to 12V. 4. LAN, R_USB30_1 signal swap. 5. CPU side 0603 10u change to 0805 22u. 6. Add POS CAP 470U DEC3. 7. Debug port turn to left. 8. KB/MS EMI CAP change to 0402. 9. Update PWM choke (P/N not done). 10. Update PWM OV (current dac)

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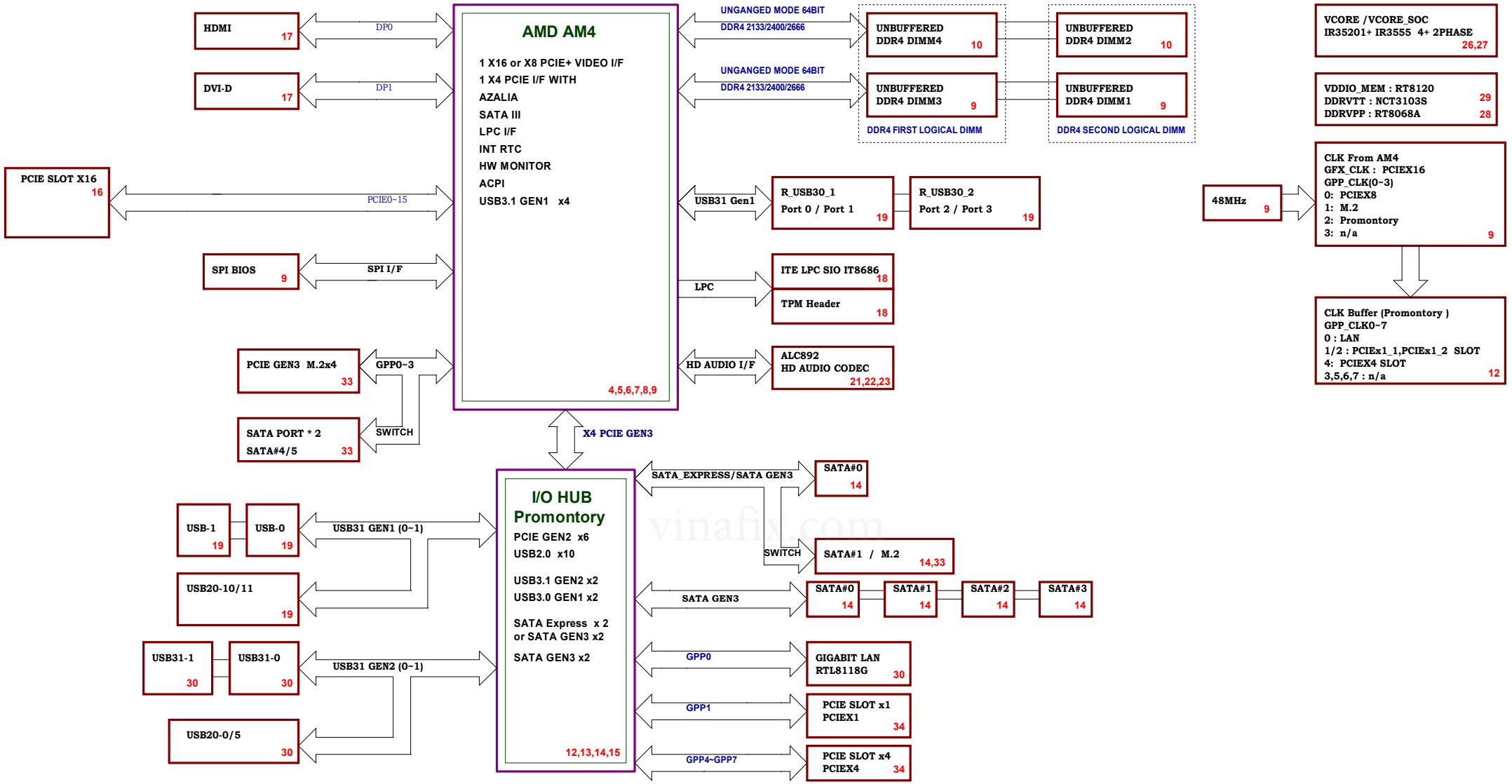
Title: BOM & PCB HISTORY		
Size: Custom	Document Number: B450 AORUS M	Rev: 1.05
Date: Wednesday, November 20, 2019	Sheet 2 of 38	



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Title: BLOCK DIAGRAM

Size: Custom | Document Number: B450 AORUS M | Rev: 1.05

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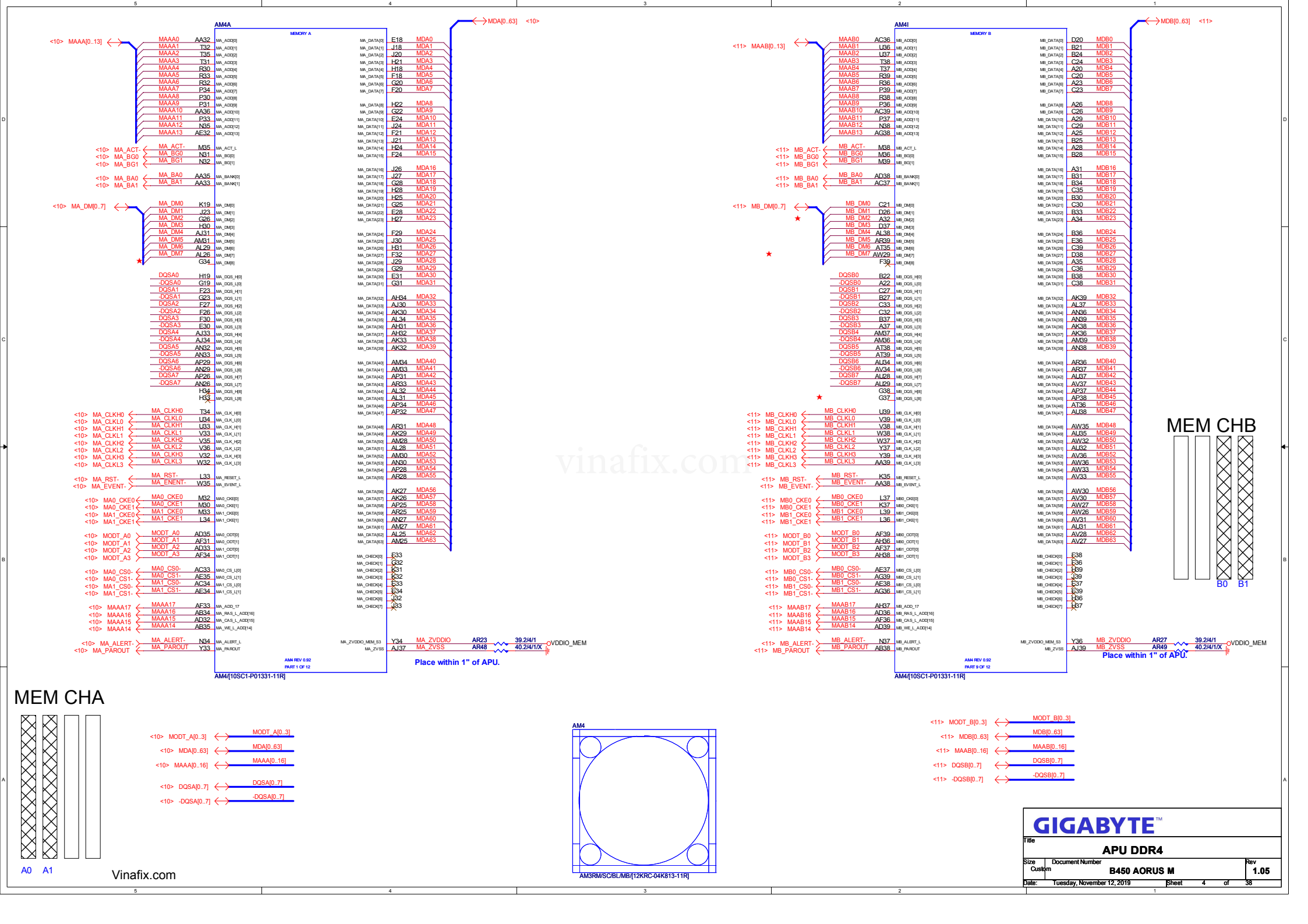
AM4A
MEMORY A
AM4I
MEMORY B
MEM CHA
MEM CHB
A0
A1
B0
B1
Place within 1" of APU.
Vinafix.com
AM4
AM3RM/SC/BL/MB/[12KRC-04K813-11R]
AM4/[10SC1-P01331-11R]
GIGABYTE
APU DDR4
B450 AORUS M
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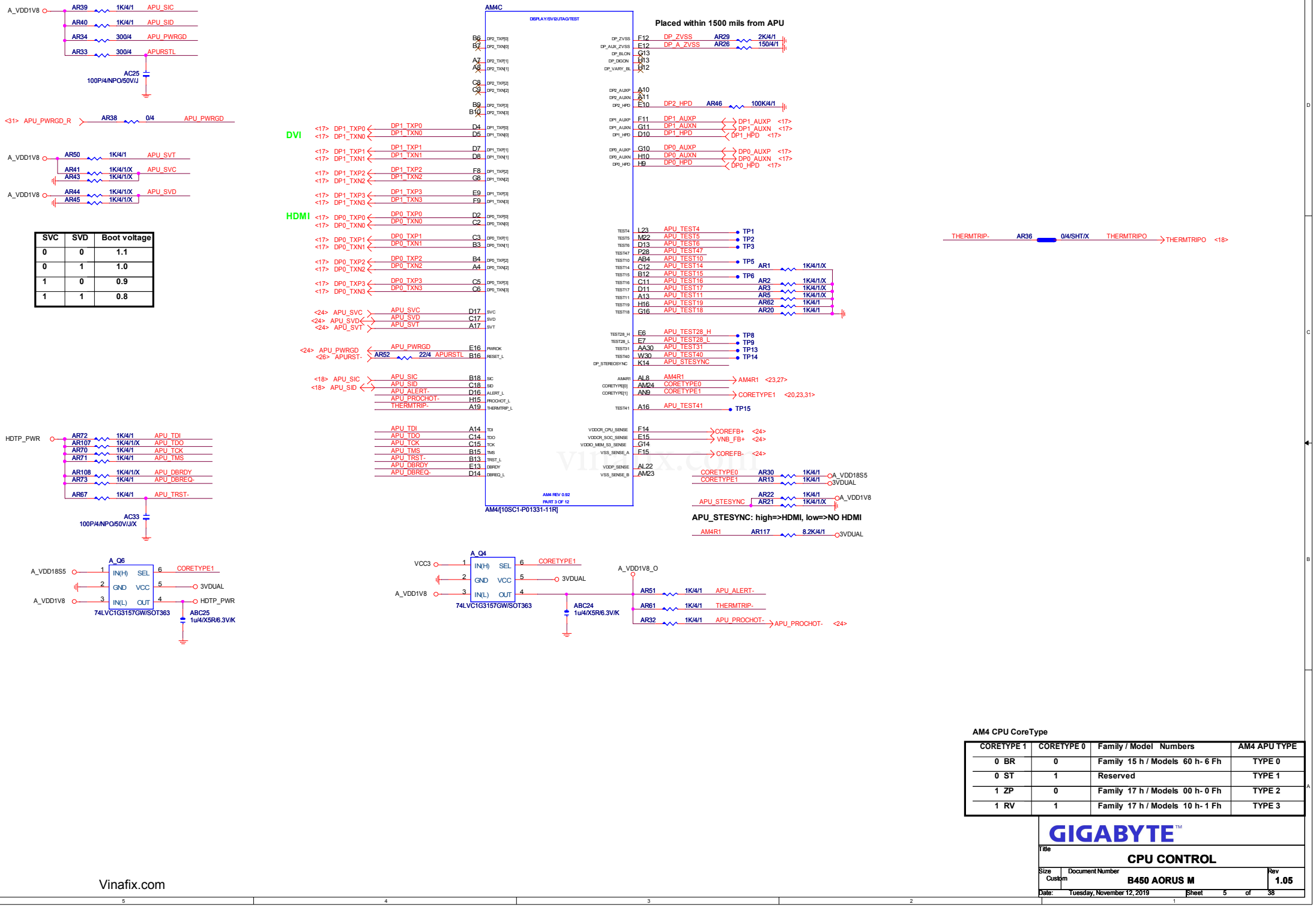
A_VDD1V8
AR39 1K/4/1 APU_SIC
AR40 1K/4/1 APU_SID
AR34 300/4 APU_PWRGD
AR33 300/4 APURSTL
AC25 100P/4/NPO/50V/J
<31> APU_PWRGD_R AR38 0/4 APU_PWRGD
AR50 1K/4/1 APU_SVT
AR41 1K/4/1/X APU_SVC
AR43 1K/4/1/X
AR44 1K/4/1/X APU_SVD
AR45 1K/4/1/X
SVC SVD Boot voltage
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
HDTP_PWR
AR72 1K/4/1 APU_TDI
AR107 1K/4/1/X APU_TDO
AR70 1K/4/1 APU_TCK
AR71 1K/4/1 APU_TMS
AR108 1K/4/1/X APU_DBRDY
AR73 1K/4/1 APU_DBREQ-
AR67 1K/4/1 APU_TRST-
AC33 100P/4/NPO/50V/J/X
A_Q6
IN(H) SEL GND VCC IN(L) OUT
74LVC1G3157GW/SOT363
A_VDD18S5 CORETYPE1 3VDUAL HDTP_PWR A_VDD1V8
ABC25 1u/4/X5R/6.3V/K
AM4C
DISPLAY/SVID/JTAG/TEST
AM4 REV 0.92
PART 3 OF 12
AM4[10SC1-P01331-11R]
Placed within 1500 mils from APU
DP_ZVSS F12 DP_ZVSS AR29 2K/4/1
DP_AUX_ZVSS E12 DP_A_ZVSS AR26 150/4/1
DP_BLON G13
DP_DIGON H13
DP_VARY_BL H12
DP2_AUXP A10
DP2_AUXN A11
DP2_HPD E10 DP2_HPD AR46 100K/4/1
DP1_AUXP F11 DP1_AUXP <17>
DP1_AUXN G11 DP1_AUXN <17>
DP1_HPD D10 DP1_HPD <17>
DP0_AUXP G10 DP0_AUXP <17>
DP0_AUXN H10 DP0_AUXN <17>
DP0_HPD H9 DP0_HPD <17>
DVI
<17> DP1_TXP0 DP1_TXP0 D4
<17> DP1_TXN0 DP1_TXN0 D5
<17> DP1_TXP1 DP1_TXP1 D7
<17> DP1_TXN1 DP1_TXN1 D8
<17> DP1_TXP2 DP1_TXP2 F8
<17> DP1_TXN2 DP1_TXN2 G8
<17> DP1_TXP3 DP1_TXP3 E9
<17> DP1_TXN3 DP1_TXN3 F9
HDMI
<17> DP0_TXP0 DP0_TXP0 D2
<17> DP0_TXN0 DP0_TXN0 C2
<17> DP0_TXP1 DP0_TXP1 C3
<17> DP0_TXN1 DP0_TXN1 B3
<17> DP0_TXP2 DP0_TXP2 B4
<17> DP0_TXN2 DP0_TXN2 A4
<17> DP0_TXP3 DP0_TXP3 C5
<17> DP0_TXN3 DP0_TXN3 C6
<24> APU_SVC APU_SVC D17
<24> APU_SVD APU_SVD C17
<24> APU_SVT APU_SVT A17
<24> APU_PWRGD APU_PWRGD E16
<26> APURST- AR52 22/4 APURSTL RESET_L B16
<18> APU_SIC APU_SIC B18
<18> APU_SID APU_SID C18
APU_ALERT- D16
APU_PROCHOT- H15
THERMTRIP- A19
APU_TDI A14
APU_TDO C14
APU_TCK C15
APU_TMS B15
APU_TRST- B13
APU_DBRDY E13
APU_DBREQ- D14
TEST4 L23 APU_TEST4 TP1
TEST5 M22 APU_TEST5 TP2
TEST6 D13 APU_TEST6 TP3
TEST47 P28 APU_TEST47
TEST10 AB4 APU_TEST10 TP5
TEST14 C12 APU_TEST14 AR1 1K/4/1/X
TEST15 B12 APU_TEST15 TP6
TEST16 C11 APU_TEST16 AR2 1K/4/1/X
TEST17 D11 APU_TEST17 AR3 1K/4/1/X
TEST11 A13 APU_TEST11 AR5 1K/4/1/X
TEST19 H16 APU_TEST19 AR62 1K/4/1
TEST18 G16 APU_TEST18 AR20 1K/4/1
TEST28_H E6 APU_TEST28_H TP8
TEST28_L E7 APU_TEST28_L TP9
TEST31 AA30 APU_TEST31 TP13
TEST40 W30 APU_TEST40 TP14
DP_STEREOSYNC K14 APU_STESYNC
AM4R1 AL8 AM4R1 AM4R1 <23,27>
CORETYPE[0] AM24 CORETYPE0
CORETYPE[1] AN9 CORETYPE1 CORETYPE1 <20,23,31>
TEST41 A16 APU_TEST41 TP15
VDDCR_CPU_SENSE F14 COREFB+ <24>
VDDCR_SOC_SENSE E15 VNB_FB+ <24>
VDDIO_MEM_S3_SENSE G14
VSS_SENSE_A F15 COREFB- <24>
VDDP_SENSE AL22
VSS_SENSE_B AM23
CORETYPE0 AR30 1K/4/1 A_VDD18S5
CORETYPE1 AR13 1K/4/1 3VDUAL
APU_STESYNC AR22 1K/4/1 AR21 1K/4/1/X A_VDD1V8
APU_STESYNC: high=>HDMI, low=>NO HDMI
AM4R1 AR117 8.2K/4/1 3VDUAL
THERMTRIP- AR36 0/4/SHT/X THERMTRIPO THERMTRIPO <18>
A_Q4
VCC3 A_VDD1V8 CORETYPE1 3VDUAL
74LVC1G3157GW/SOT363
ABC24 1u/4/X5R/6.3V/K
A_VDD1V8_O
AR51 1K/4/1 APU_ALERT-
AR61 1K/4/1 THERMTRIP-
AR32 1K/4/1 APU_PROCHOT- APU_PROCHOT- <24>
AM4 CPU CoreType
CORETYPE 1 CORETYPE 0 Family / Model Numbers AM4 APU TYPE
0 BR 0 Family 15 h / Models 60 h- 6 Fh TYPE 0
0 ST 1 Reserved TYPE 1
1 ZP 0 Family 17 h / Models 00 h- 0 Fh TYPE 2
1 RV 1 Family 17 h / Models 10 h- 1 Fh TYPE 3
GIGABYTE
Title
CPU CONTROL
Size Custom
Document Number B450 AORUS M
Rev 1.05
Date: Tuesday, November 12, 2019
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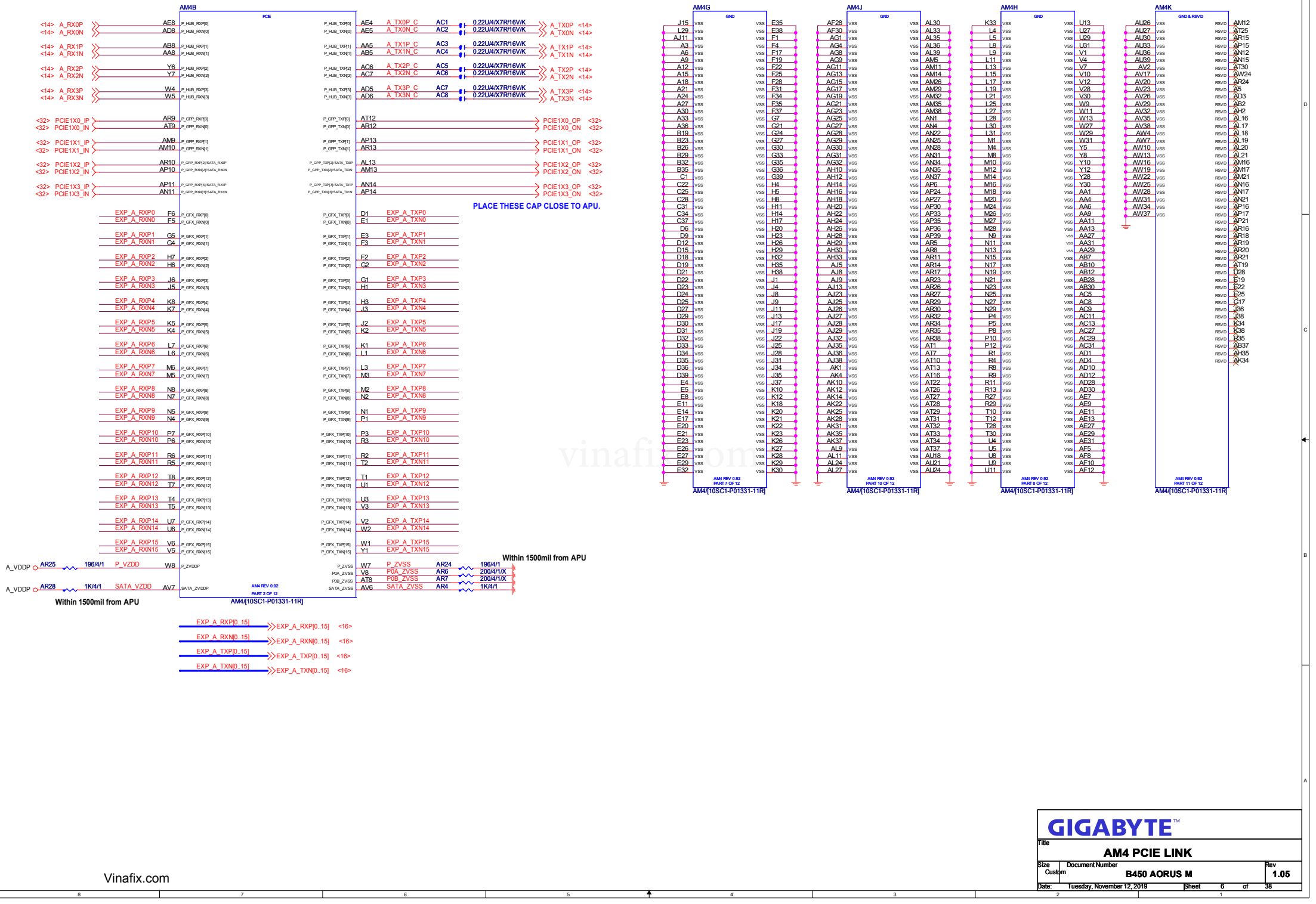

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Title	AM4 PCIE LINK	
Size: Custom	Document Number: B450 AORUS M	Rev: 1.05
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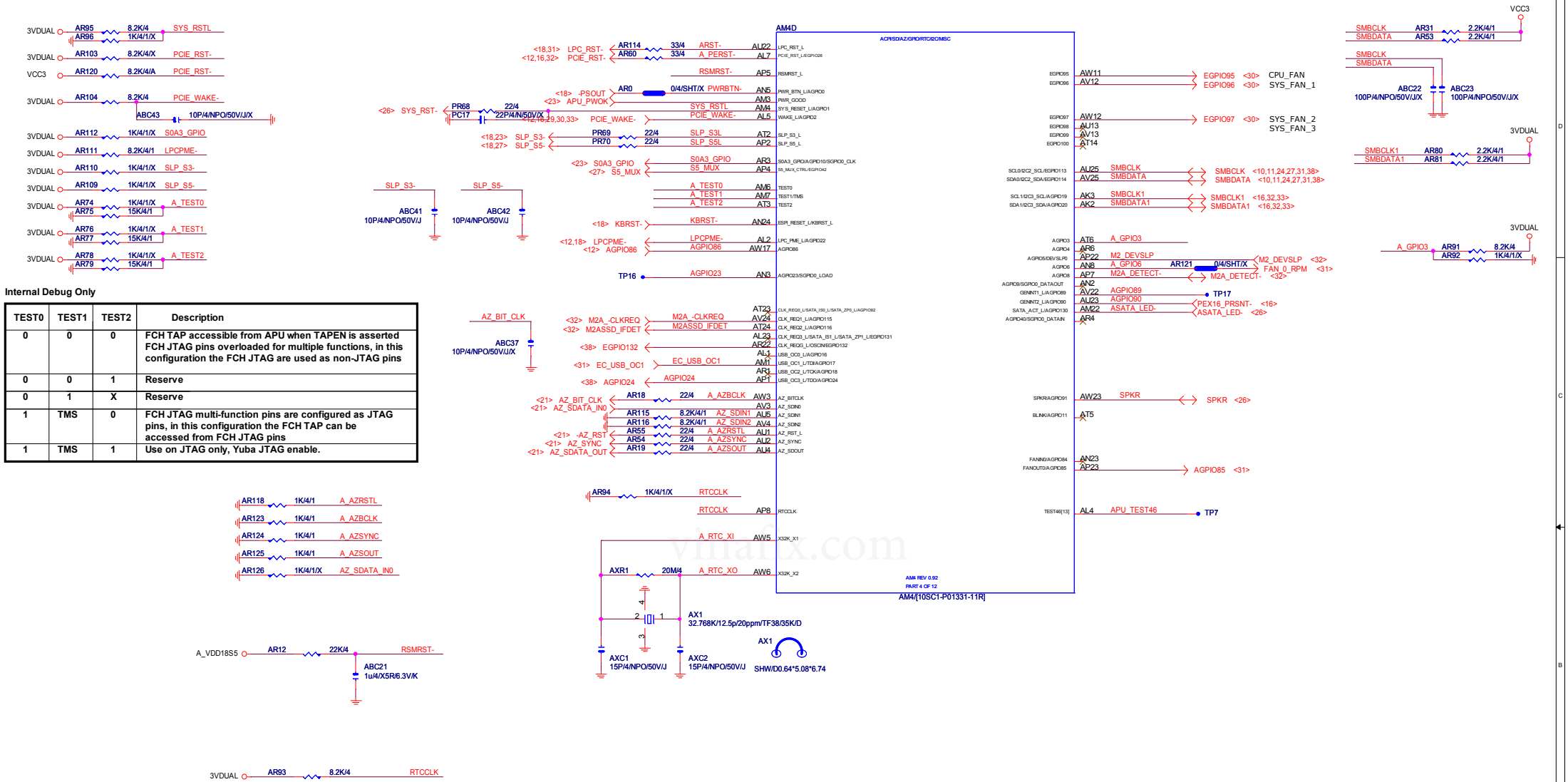
AM4D
AM4/[10SC1-P01331-11R]
3VDUAL
VCC3
SYS_RSTL
PCIE_RST-
PCIE_WAKE-
S0A3_GPIO
LPCPME-
SLP_S3-
SLP_S5-
A_TEST0
A_TEST1
A_TEST2
Internal Debug Only
TEST0 TEST1 TEST2 Description
0 0 0 FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0 0 1 Reserve
0 1 X Reserve
1 TMS 0 FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1 TMS 1 Use on JTAG only, Yuba JTAG enable.
LPC_CLK0 LPC_CLK1 AGPIO3 RTC_CLK LFRAME_L SYS_RST# SPI CLK (ZP)
PULL HIGH
BOOT FAIL TIMER ENABLED
Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)
Coin battery is on board. (DEFAULT)
SPI ROM (DEFAULT)
normal reset mode (DEFAULT)
Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW
BOOT FAIL TIMER DISABLED (DEFAULT)
Use 100Mhz PCIE clock as reference clock and generate internal clocks only
Default to traditional reset logic
Coin battery is not on board.
LPC ROM
short reset mode
Use 100Mhz PCIE clock as reference clock and generate internal clocks only
CE/ST DIE ONLY
ZP DIE ONLY
Vinafix.com
ORTCR1 20M/4 ORTCXO ORTCXI
ORTCX 32.768K/12.5p/20ppm/TF38/35K/D
ORTC2 12P/4/NPO/50V/J/X
ORTC1 12P/4/NPO/50V/J/X
SHW/D0.64*5.08*6.74
RTC
XI XO INT- VSS BGND VDD CLKOUT SCL SDA
PCF85063TP/HWSON8
RTCVDD3 TP12 SMBCLK1 SMBDATA1
GIGABYTE
Title AM4 MISC
Size Custom Document Number B450 AORUS M Rev 1.05
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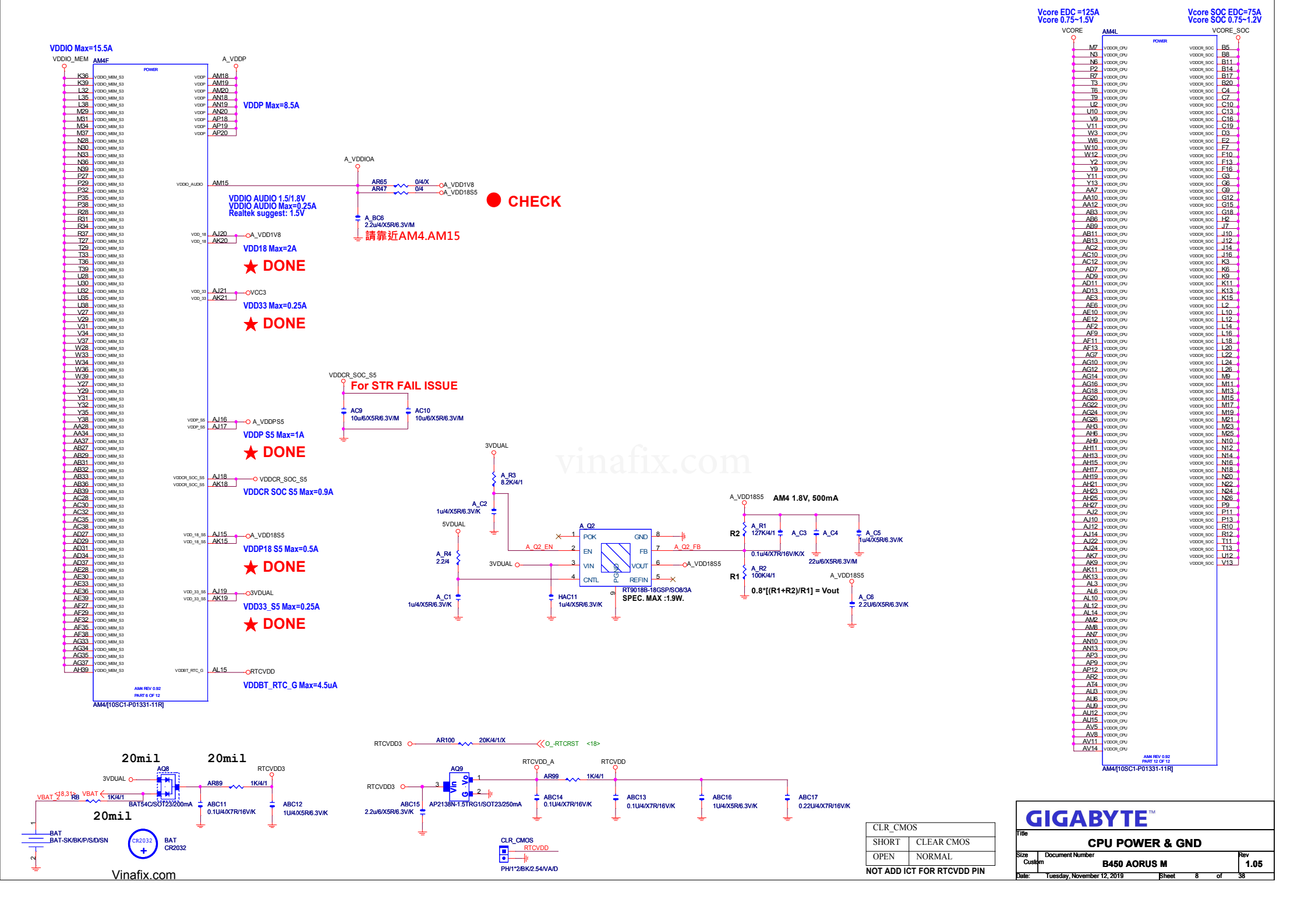
VDDIO Max=15.5A
VDDIO_MEM
AM4F
POWER
A_VDDP
VDDP Max=8.5A
A_VDDIOA
VDDIO_AUDIO
AM15
AR65 0/4/X
AR47 0/4
A_VDD1V8
A_VDD18S5
VDDIO AUDIO 1.5/1.8V
VDDIO AUDIO Max=0.25A
Realtek suggest: 1.5V
CHECK
A_BC6
2.2u/4/X5R/6.3V/M
請靠近AM4.AM15
A_VDD1V8
VDD18 Max=2A
DONE
VCC3
VDD33 Max=0.25A
DONE
VDDCR_SOC_S5
For STR FAIL ISSUE
AC9
10u/6/X5R/6.3V/M
AC10
10u/6/X5R/6.3V/M
A_VDDPS5
VDDP S5 Max=1A
DONE
VDDCR_SOC_S5
VDDCR SOC S5 Max=0.9A
A_VDD18S5
VDDP18 S5 Max=0.5A
DONE
3VDUAL
VDD33_S5 Max=0.25A
DONE
RTCVDD
VDDBT_RTC_G Max=4.5uA
AM4 REV 0.92
PART 6 OF 12
AM4/[10SC1-P01331-11R]
3VDUAL
A_R3
8.2K/4/1
A_C2
1u/4/X5R/6.3V/K
5VDUAL
A_R4
2.2/4
A_C1
1u/4/X5R/6.3V/K
A_Q2
POK
EN
VIN
CNTL
GND
FB
VOUT
REFIN
PGND
A_Q2_EN
A_Q2_FB
A_VDD18S5
HAC11
1u/4/X5R/6.3V/K
RT9018B-18GSP/SO8/3A
SPEC. MAX :1.9W.
A_VDD18S5
AM4 1.8V, 500mA
R2
A_R1
127K/4/1
A_C3
0.1u/4/X7R/16V/K/X
A_C4
22u/6/X5R/6.3V/M
A_C5
1u/4/X5R/6.3V/K
R1
A_R2
100K/4/1
0.8*[(R1+R2)/R1] = Vout
A_VDD18S5
A_C6
2.2U/6/X5R/6.3V/K
Vcore EDC =125A
Vcore 0.75~1.5V
Vcore SOC EDC=75A
Vcore SOC 0.75~1.2V
VCORE
AM4L
POWER
VCORE_SOC
AM4 REV 0.92
PART 12 OF 12
AM4/[10SC1-P01331-11R]
20mil
20mil
20mil
3VDUAL
AQ8
AR89
1K/4/1
RTCVDD3
VBAT
RB
1K/4/1
BAT54C/SOT23/200mA
ABC11
0.1U/4/X7R/16V/K
ABC12
1U/4/X5R/6.3V/K
BAT
BAT-SK/BK/P/S/D/SN
CR2032
BAT
CR2032
Vinafix.com
RTCVDD3
AR100
20K/4/1/X
O_-RTCRST
<18>
AQ9
RTCVDD_A
AR99
1K/4/1
RTCVDD
ABC15
2.2u/6/X5R/6.3V/K
AP2138N-1.5TRG1/SOT23/250mA
ABC14
0.1U/4/X7R/16V/K
ABC13
0.1U/4/X7R/16V/K
ABC16
1U/4/X5R/6.3V/K
ABC17
0.22U/4/X7R/16V/K
CLR_CMOS
RTCVDD
PH/1*2/BK/2.54/VA/D
CLR_CMOS
SHORT CLEAR CMOS
OPEN NORMAL
NOT ADD ICT FOR RTCVDD PIN
GIGABYTE
Title
CPU POWER & GND
Size Custom
Document Number
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Rev 1.05
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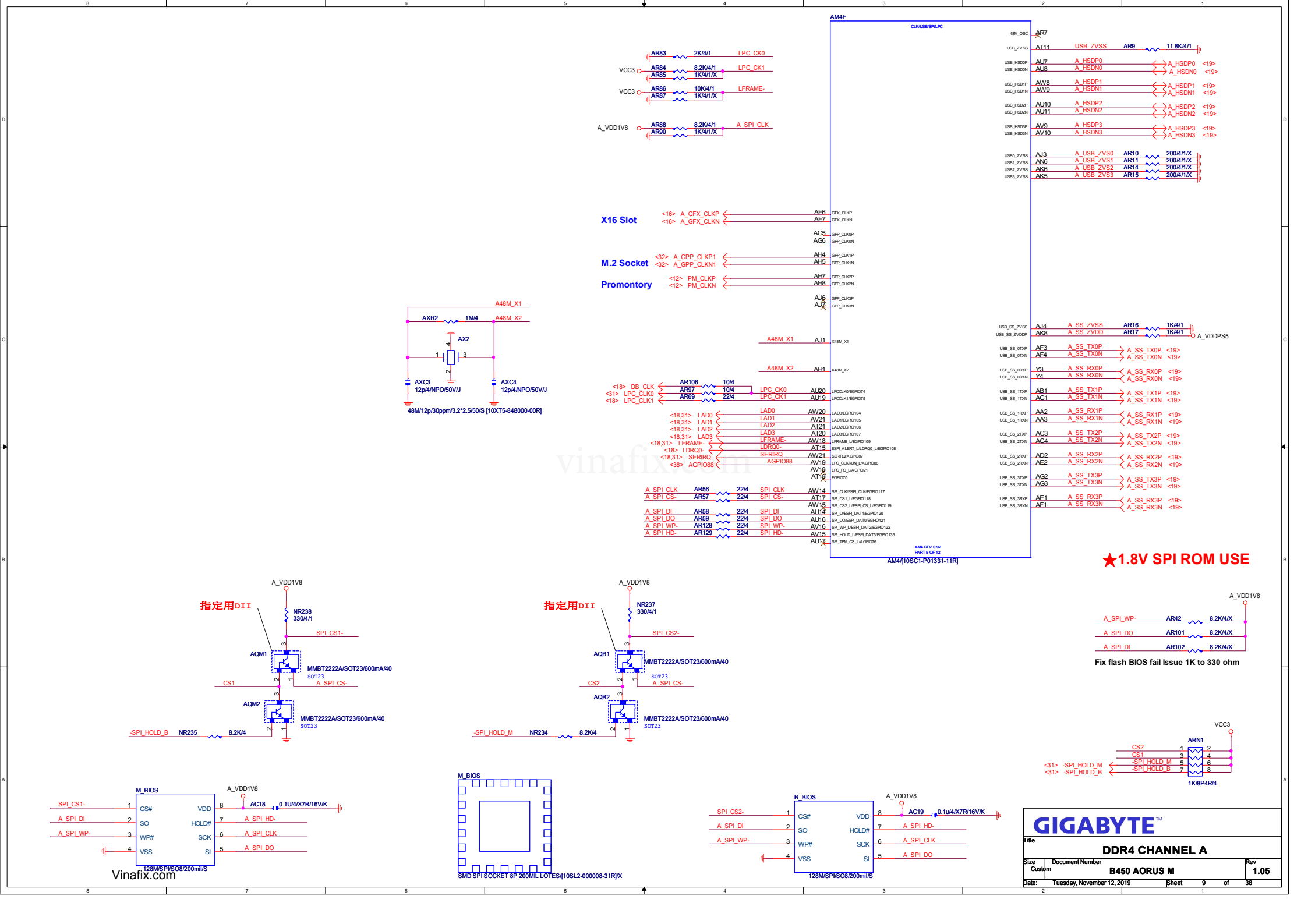
AM4E
CLK/USB/SPI/LPC
AR83 2K/4/1 LPC_CK0
AR84 8.2K/4/1 LPC_CK1
AR85 1K/4/1/X
AR86 10K/4/1 LFRAME-
AR87 1K/4/1/X
AR88 8.2K/4/1 A_SPI_CLK
AR90 1K/4/1/X
AR7
AT11 USB_ZVSS AR9 11.8K/4/1
AU7 A_HSDP0
AU8 A_HSDN0
AW8 A_HSDP1
AW9 A_HSDN1
AU10 A_HSDP2
AU11 A_HSDN2
AV9 A_HSDP3
AV10 A_HSDN3
AJ3 A_USB_ZVS0 AR10 200/4/1/X
AN6 A_USB_ZVS1 AR11 200/4/1/X
AK6 A_USB_ZVS2 AR14 200/4/1/X
AK5 A_USB_ZVS3 AR15 200/4/1/X
X16 Slot
M.2 Socket
Promontory
AF6 GFX_CLKP
AF7 GFX_CLKN
AG5 GPP_CLK0P
AG6 GPP_CLK0N
AH4 GPP_CLK1P
AH5 GPP_CLK1N
AH7 GPP_CLK2P
AH8 GPP_CLK2N
AJ6 GPP_CLK3P
AJ7 GPP_CLK3N
A48M_X1 AJ1 X48M_X1
A48M_X2 AH1 X48M_X2
AR106 10/4
AR97 10/4 LPC_CK0 AU20
AR69 22/4 LPC_CK1 AU19
LAD0 AW20
LAD1 AV21
LAD2 AT21
LAD3 AT20
LFRAME- AW18
LDRQ0- AT15
SERIRQ AV21
AGPIO88 AV19
AV18
AT18
A_SPI_CLK AR56 22/4 SPI_CLK AW14
A_SPI_CS- AR57 22/4 SPI_CS- AT17
A_SPI_DI AR58 22/4 SPI_DI AU14
A_SPI_DO AR59 22/4 SPI_DO AU16
A_SPI_WP- AR128 22/4 SPI_WP- AV16
A_SPI_HD- AR129 22/4 SPI_HD- AV15
AU17
AM4 REV 0.92
PART 5 OF 12
AM4[10SC1-P01331-11R]
USB_SS_ZVSS AJ4 A_SS_ZVSS AR16 1K/4/1
USB_SS_ZVDDP AK8 A_SS_ZVDD AR17 1K/4/1
A_VDDPS5
AF3 A_SS_TX0P
AF4 A_SS_TX0N
Y3 A_SS_RX0P
Y4 A_SS_RX0N
AB1 A_SS_TX1P
AC1 A_SS_TX1N
AA2 A_SS_RX1P
AA3 A_SS_RX1N
AC3 A_SS_TX2P
AC4 A_SS_TX2N
AD2 A_SS_RX2P
AE2 A_SS_RX2N
AG2 A_SS_TX3P
AG3 A_SS_TX3N
AE1 A_SS_RX3P
AF1 A_SS_RX3N
A48M_X1
AXR2 1M/4 A48M_X2
AX2
AXC3 12p/4/NPO/50V/J
AXC4 12p/4/NPO/50V/J
48M/12p/30ppm/3.2*2.5/50/S [10XT5-848000-00R]
DB_CLK
LPC_CLK0
LPC_CLK1
LAD0
LAD1
LAD2
LAD3
LFRAME-
LDRQ0-
SERIRQ
AGPIO88
A_SPI_CLK
A_SPI_CS-
A_SPI_DI
A_SPI_DO
A_SPI_WP-
A_SPI_HD-
★1.8V SPI ROM USE
指定用DII
A_VDD1V8
NR238 330/4/1
SPI_CS1-
AQM1
MMBT2222A/SOT23/600mA/40
SOT23
CS1
A_SPI_CS-
AQM2
MMBT2222A/SOT23/600mA/40
SOT23
-SPI_HOLD_B
NR235 8.2K/4
NR237 330/4/1
SPI_CS2-
AQB1
MMBT2222A/SOT23/600mA/40
SOT23
CS2
A_SPI_CS-
AQB2
MMBT2222A/SOT23/600mA/40
SOT23
-SPI_HOLD_M
NR234 8.2K/4
A_SPI_WP- AR42 8.2K/4/X
A_SPI_DO AR101 8.2K/4/X
A_SPI_DI AR102 8.2K/4/X
Fix flash BIOS fail Issue 1K to 330 ohm
VCC3
ARN1
CS2
CS1
-SPI_HOLD_M
-SPI_HOLD_B
1K/8P4R/4
M_BIOS
SPI_CS1-
A_SPI_DI
A_SPI_WP-
CS#
SO
WP#
VSS
VDD
HOLD#
SCK
SI
AC18 0.1U/4/X7R/16V/K
A_SPI_HD-
A_SPI_CLK
A_SPI_DO
128M/SPI/SO8/200mil/S
SMD SPI SOCKET 8P 200MIL LOTES/[10SL2-000008-31R]/X
B_BIOS
SPI_CS2-
AC19 0.1u/4/X7R/16V/K
Vinafix.com
GIGABYTE
Title
DDR4 CHANNEL A
Size Custom
Document Number B450 AORUS M
Rev 1.05
Date: Tuesday, November 12, 2019
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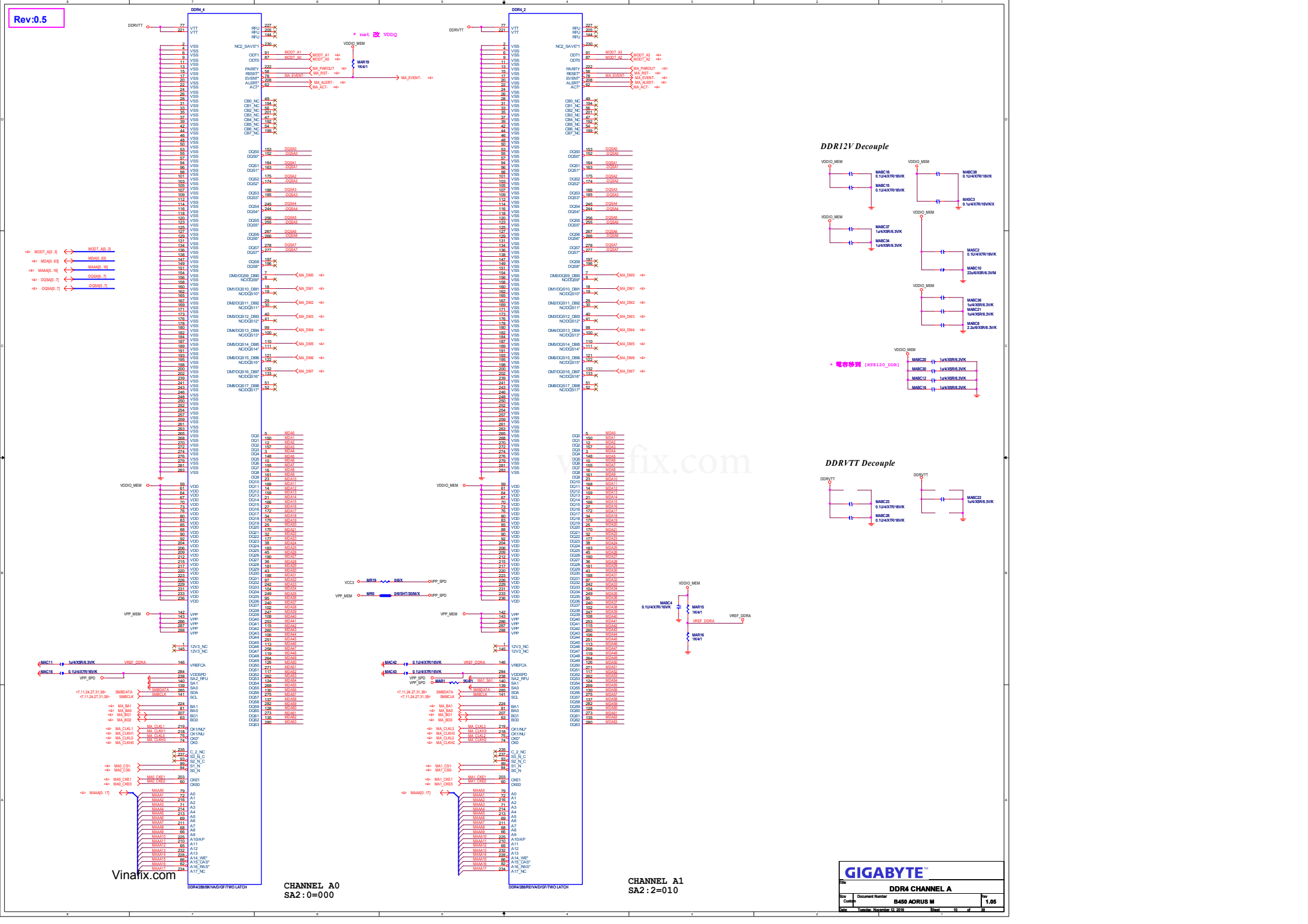
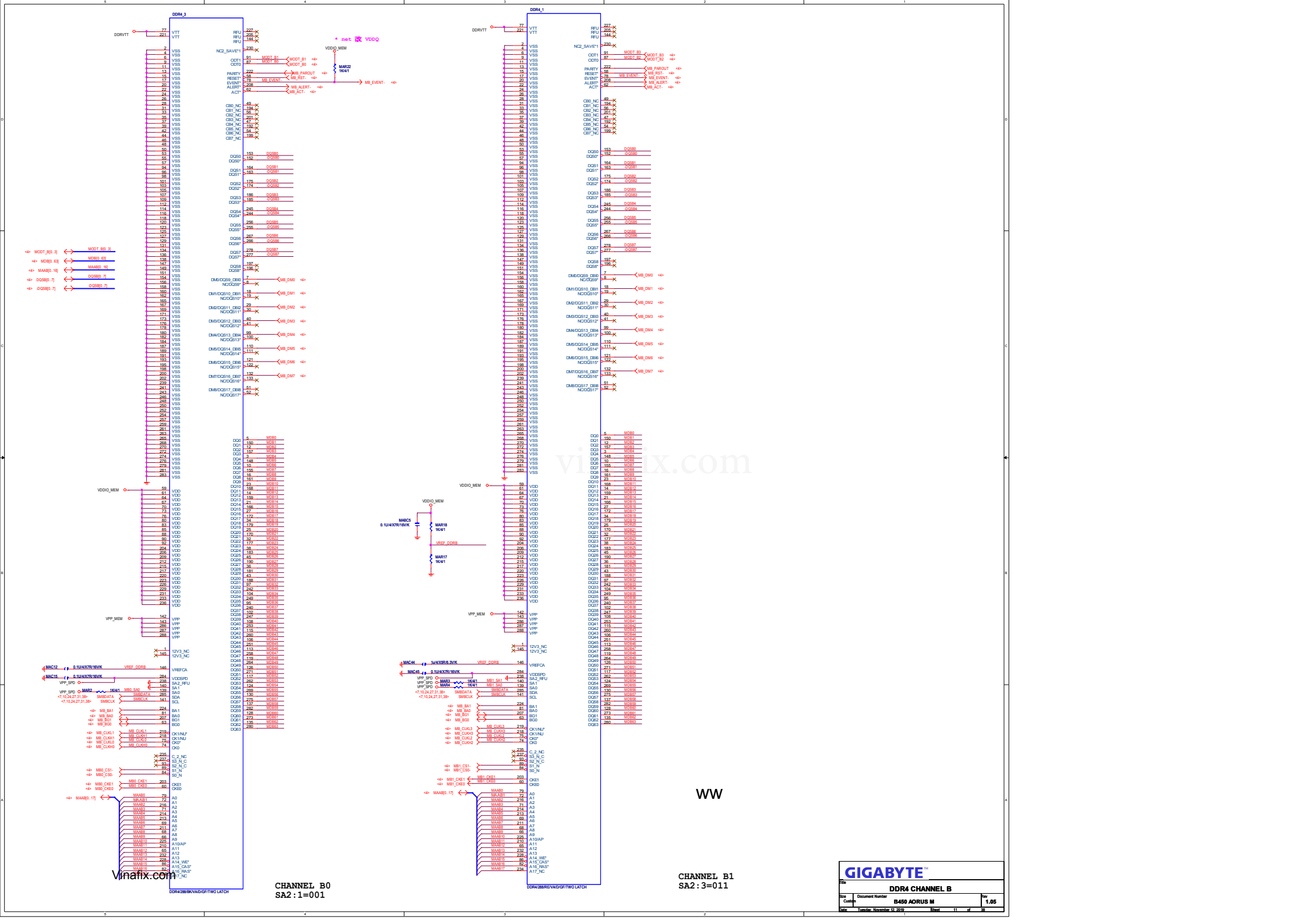
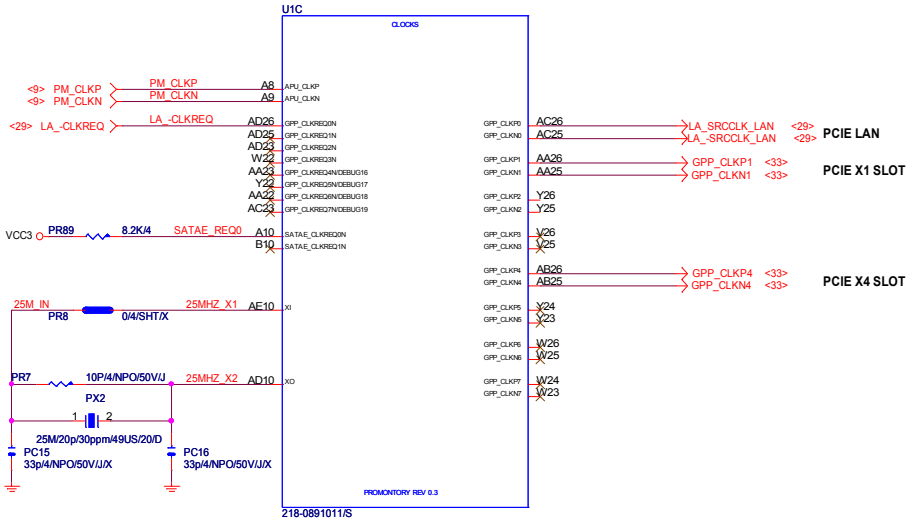
Rev:0.5

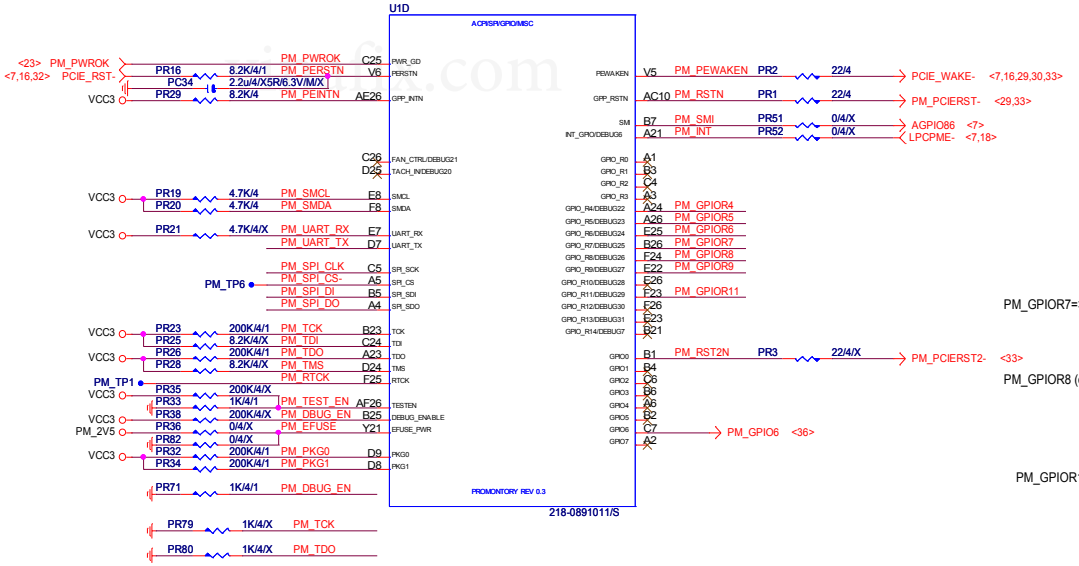


GIGABYTE

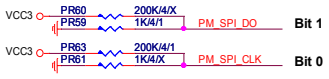
Title	DDR4 CHANNEL A	
Size: Custom	Document Number: B450 AORUS M	Rev: 1.05
Date: Tuesday, November 12, 2019	Sheet 10 of 38	


DDR4_3
DDR4_1
* not for VDDQ
VDDIO_MEM
VPP_MEM
DDRVTT
MAR22 1K/4/1
MAR2 1K/4/1
MAR3 1K/4/1
MAR4 1K/4/1
MAR18 1K/4/1
MAR17 1K/4/1
MABC5 0.1U/4/X7R/16V/K
MAC12 0.1U/4/X7R/16V/K
MAC15 0.1U/4/X7R/16V/K
MAC44 1U/4/X5R/6.3V/K
MAC45 0.1U/4/X7R/16V/K
VREF_DDRB
MB_EVENT-
MB_PAROUT
MB_ALERT-
MB_ACT-
MODT_B1
MODT_B0
MODT_B3
MODT_B2
SMBDATA
SMBCLK
DDR4/28B/RVA/D/GF/TWO LATCH
CHANNEL B0
SA2:1=001
CHANNEL B1
SA2:3=011
WW
GIGABYTE
DDR4 CHANNEL B
B450 AORUS M
1.05
Tuesday, November 12, 2019
Vinafix.com

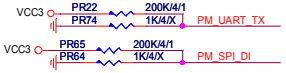




PM GPP Group 0 Strap: 11=> 1PCIe x4, 10=>1PCIe x2, 2PCIex1, 01=>4PCIe x1, 00=>Reserved.
PM GPP Group 0=>0~3



PM GPP Group 1 Strap: 11=> 1PCIe x4, 10=>1PCIe x2, 2PCIex1, 01=>4PCIe x1, 00=>Reserved.
PM GPP Group 1=>4~7



PM_GPIOR4 1: GPP clock source from APU_CLKP/N; 0: GPP clock source from Crystal, also enables GPIO_R8 .

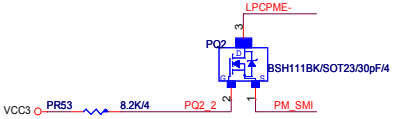
PM_GPIOR5=>1 : USBC SSC disable, 0: USBC SSC enable

PM_GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable

PM_GPIOR7=>1: SATA Express SSC disable, 0: SATA Express SSC enable

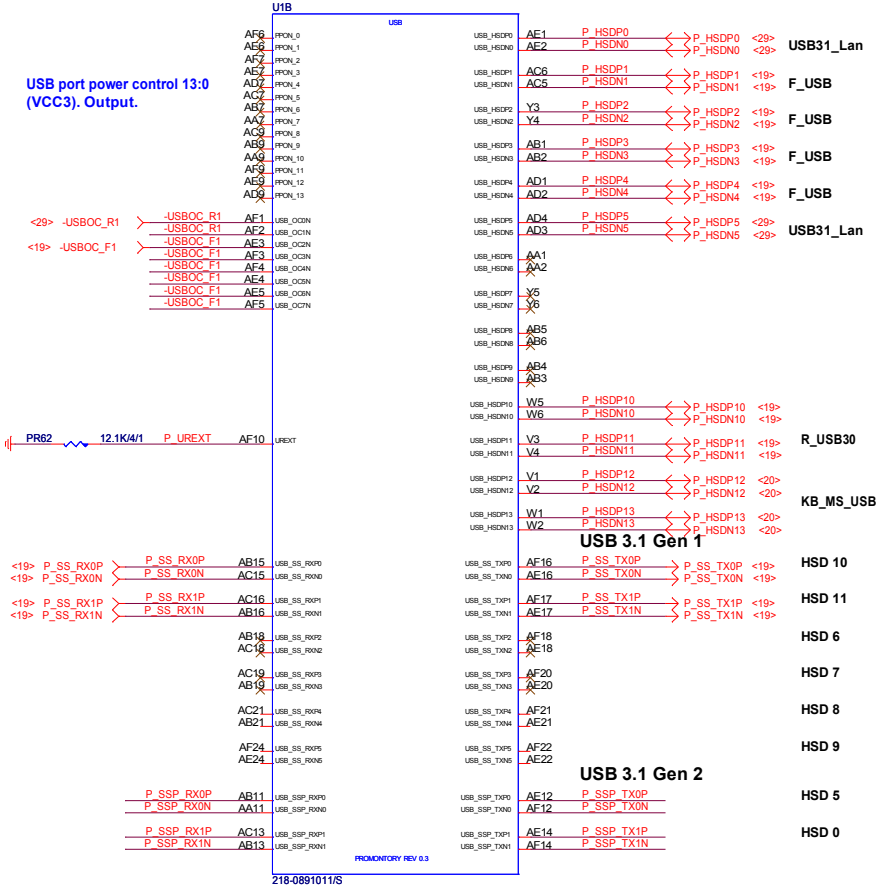
PM_GPIOR8 (enabled from GPIO_R4) =>1: GPP SSC disable, 0: GPP SSC enable

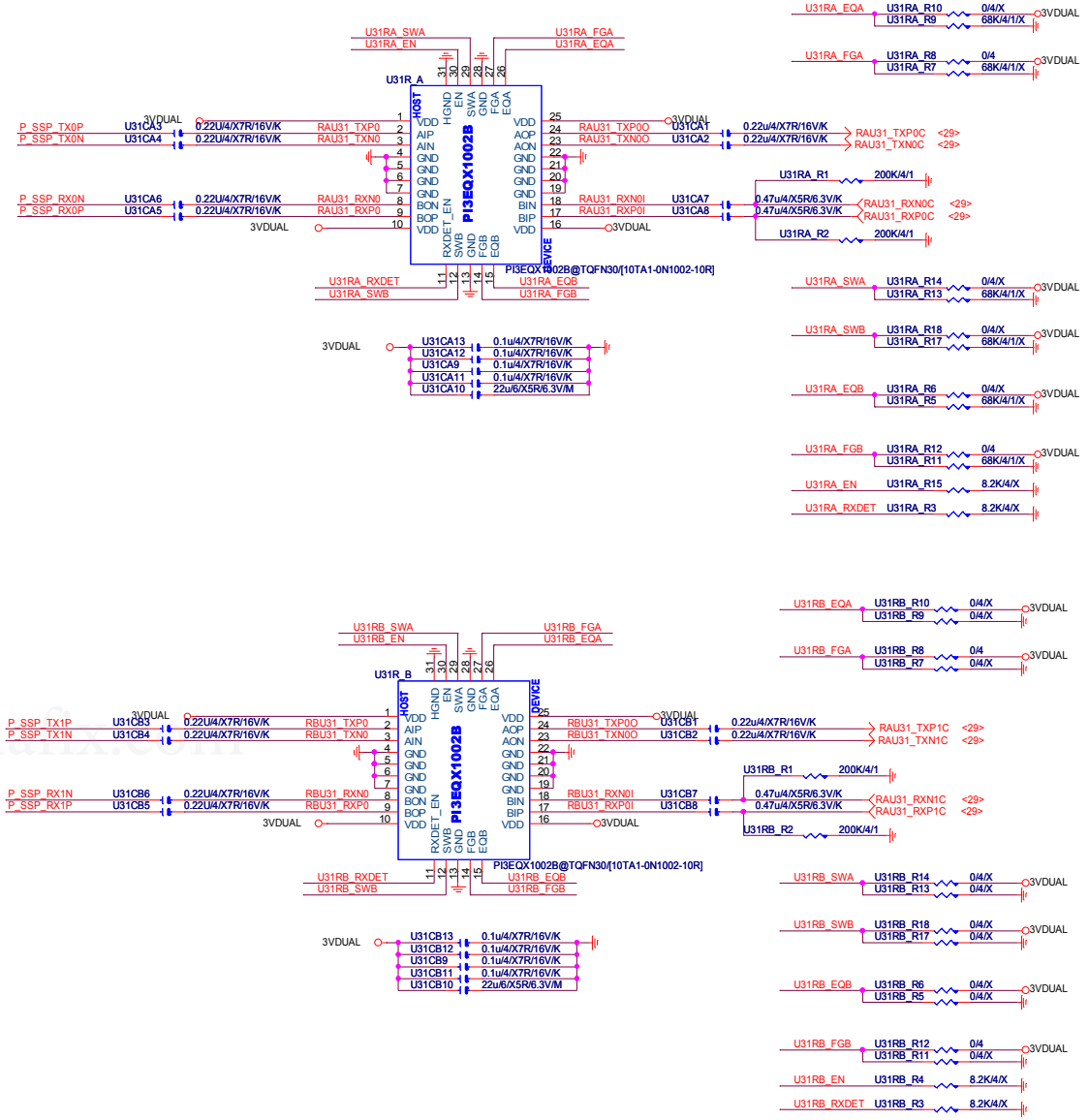
PM_GPIOR11=>1: GPP clock output enabled,0: GPP clock output disabled



GIGABYTE™ ANS 7633475

Title	B350 CLK GEN / GPIO	
Size: Custom	Document Number: B450 AORUS M	Rev: 1.05
Date: Friday, January 17, 2020	Sheet 12 of 38	





USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

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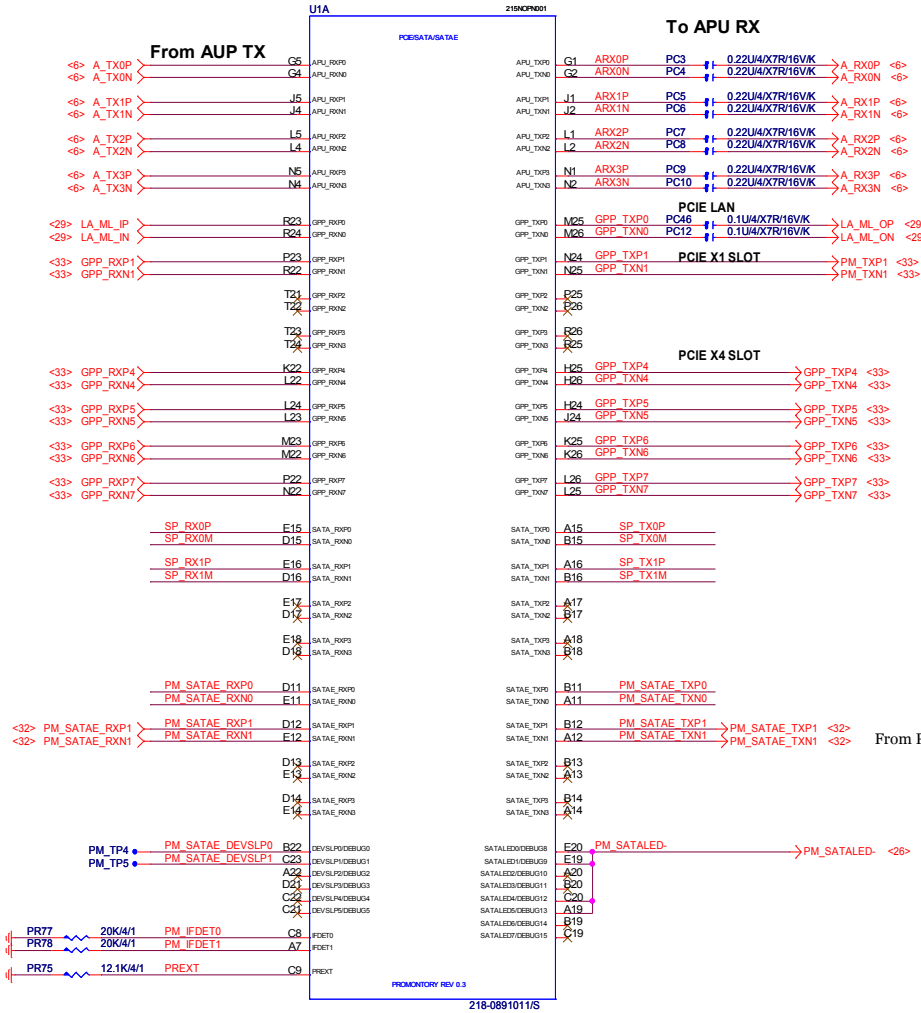
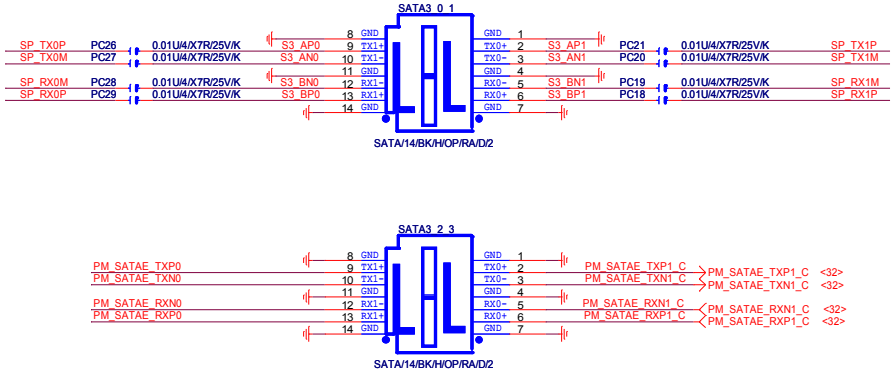
Title: B350 USB , PI3EQX1002B

Size: Custom | Document Number: B450 AORUS M | Rev: 1.05

Date: Friday, January 17, 2020 | Sheet 13 of 38





BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

GIGABYTE™ ANS 7633475

Title: B350 SATA/SPI

Size: Custom | Document Number: B450 AORUS M | Rev: 1.05

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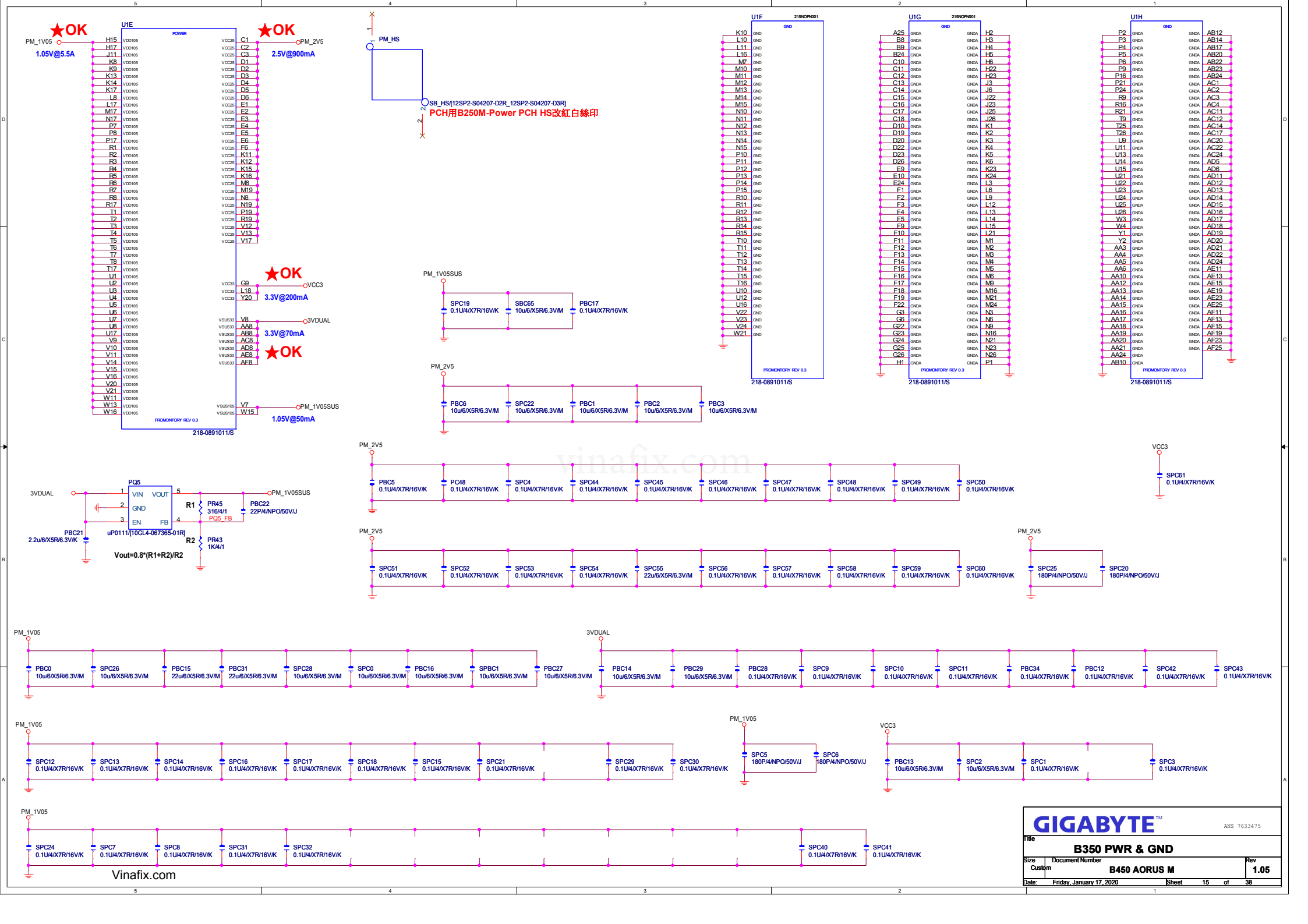
OK
PM_1V05
1.05V@5.5A
U1E
POWER
PROMONTORY REV 0.3
218-0891011/S
OK
PM_2V5
2.5V@900mA
PM_HS
SB_HS[12SP2-S04207-D2R_12SP2-S04207-D3R]
PCH用B250M-Power PCH HS改紅白絲印
OK
VCC3
3.3V@200mA
OK
3VDUAL
3.3V@70mA
OK
PM_1V05SUS
1.05V@50mA
U1F
215NDPN001
GND
PROMONTORY REV 0.3
218-0891011/S
U1G
215NDPN001
GND
PROMONTORY REV 0.3
218-0891011/S
U1H
GND
PROMONTORY REV 0.3
218-0891011/S
PM_1V05SUS
SPC19 0.1U/4/X7R/16V/K
SBC85 10u/6/X5R/6.3V/M
PBC17 0.1U/4/X7R/16V/K
PM_2V5
PBC6 10u/6/X5R/6.3V/M
SPC22 10u/6/X5R/6.3V/M
PBC1 10u/6/X5R/6.3V/M
PBC2 10u/6/X5R/6.3V/M
PBC3 10u/6/X5R/6.3V/M
PQ5
3VDUAL
VIN
VOUT
GND
EN
FB
uP0111/[10GL4-067365-01R]
R1
PR45 316/4/1
PQ5_FB
R2
PR43 1K/4/1
PBC21 2.2u/6/X5R/6.3V/K
PBC22 22P/4/NPO/50V/J
PM_1V05SUS
Vout=0.8*(R1+R2)/R2
PM_2V5
PBC5 0.1U/4/X7R/16V/K
PC48 0.1U/4/X7R/16V/K
SPC4 0.1U/4/X7R/16V/K
SPC44 0.1U/4/X7R/16V/K
SPC45 0.1U/4/X7R/16V/K
SPC46 0.1U/4/X7R/16V/K
SPC47 0.1U/4/X7R/16V/K
SPC48 0.1U/4/X7R/16V/K
SPC49 0.1U/4/X7R/16V/K
SPC50 0.1U/4/X7R/16V/K
VCC3
SPC61 0.1U/4/X7R/16V/K
PM_2V5
SPC51 0.1U/4/X7R/16V/K
SPC52 0.1U/4/X7R/16V/K
SPC53 0.1U/4/X7R/16V/K
SPC54 0.1U/4/X7R/16V/K
SPC55 22u/6/X5R/6.3V/M
SPC56 0.1U/4/X7R/16V/K
SPC57 0.1U/4/X7R/16V/K
SPC58 0.1U/4/X7R/16V/K
SPC59 0.1U/4/X7R/16V/K
SPC60 0.1U/4/X7R/16V/K
PM_2V5
SPC25 180P/4/NPO/50V/J
SPC20 180P/4/NPO/50V/J
PM_1V05
PBC0 10u/6/X5R/6.3V/M
SPC26 10u/6/X5R/6.3V/M
PBC15 22u/6/X5R/6.3V/M
PBC31 22u/6/X5R/6.3V/M
SPC28 10u/6/X5R/6.3V/M
SPC0 10u/6/X5R/6.3V/M
PBC16 10u/6/X5R/6.3V/M
SPBC1 10u/6/X5R/6.3V/M
PBC27 10u/6/X5R/6.3V/M
3VDUAL
PBC14 10u/6/X5R/6.3V/M
PBC29 10u/6/X5R/6.3V/M
PBC28 0.1U/4/X7R/16V/K
SPC9 0.1U/4/X7R/16V/K
SPC10 0.1U/4/X7R/16V/K
SPC11 0.1U/4/X7R/16V/K
PBC34 0.1U/4/X7R/16V/K
PBC12 0.1U/4/X7R/16V/K
SPC42 0.1U/4/X7R/16V/K
SPC43 0.1U/4/X7R/16V/K
PM_1V05
SPC12 0.1U/4/X7R/16V/K
SPC13 0.1U/4/X7R/16V/K
SPC14 0.1U/4/X7R/16V/K
SPC16 0.1U/4/X7R/16V/K
SPC17 0.1U/4/X7R/16V/K
SPC18 0.1U/4/X7R/16V/K
SPC15 0.1U/4/X7R/16V/K
SPC21 0.1U/4/X7R/16V/K
SPC29 0.1U/4/X7R/16V/K
SPC30 0.1U/4/X7R/16V/K
PM_1V05
SPC5 180P/4/NPO/50V/J
SPC6 180P/4/NPO/50V/J
VCC3
PBC13 10u/6/X5R/6.3V/M
SPC2 10u/6/X5R/6.3V/M
SPC1 0.1U/4/X7R/16V/K
SPC3 0.1U/4/X7R/16V/K
PM_1V05
SPC24 0.1U/4/X7R/16V/K
SPC7 0.1U/4/X7R/16V/K
SPC8 0.1U/4/X7R/16V/K
SPC31 0.1U/4/X7R/16V/K
SPC32 0.1U/4/X7R/16V/K
SPC40 0.1U/4/X7R/16V/K
SPC41 0.1U/4/X7R/16V/K
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GIGABYTE
ANS 7633475
Title
B350 PWR & GND
Size
Custom
Document Number
B450 AORUS M
Rev
1.05
Date:
Friday, January 17, 2020
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15
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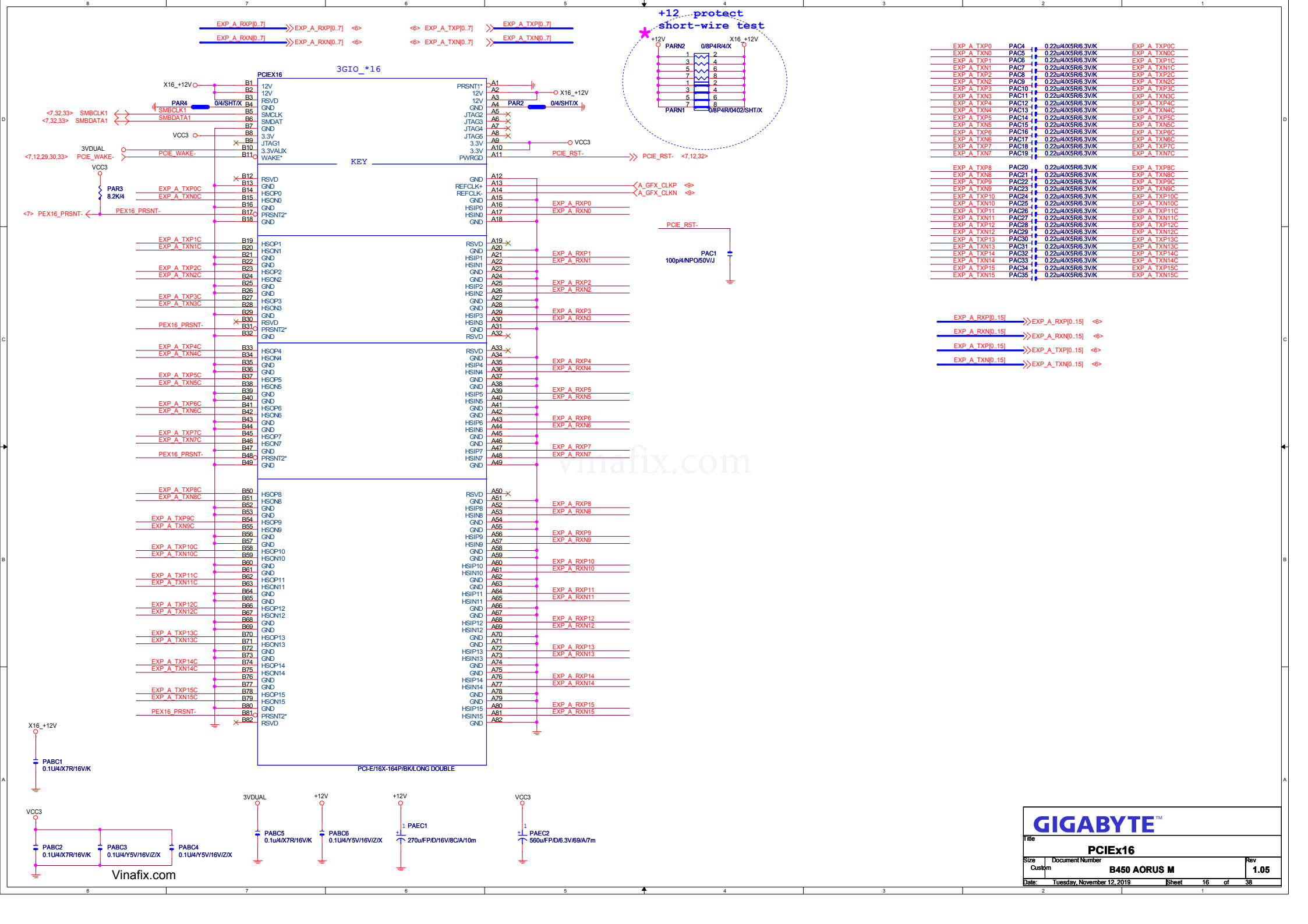
38


+12 protect
short-wire test
PCIEX16
3GIO_*16
KEY
PCI-E/16X-164P/BK/LONG DOUBLE
PAR4 0/4/SHT/X
PAR2 0/4/SHT/X
PAR3 8.2K/4
PAC1 100p/4/NPO/50V/J
PARN2 0/8P4R/4/X
PARN1 0/8P4R/0402/SHT/X
PABC1 0.1U/4/X7R/16V/K
PABC2 0.1U/4/X7R/16V/K
PABC3 0.1U/4/Y5V/16V/Z/X
PABC4 0.1U/4/Y5V/16V/Z/X
PABC5 0.1u/4/X7R/16V/K
PABC6 0.1U/4/Y5V/16V/Z/X
PAEC1 270u/FP/D/16V/8C/A/10m
PAEC2 560u/FP/D/6.3V/69/A/7m
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GIGABYTE
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Size: Custom
Document Number: B450 AORUS M
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Date: Tuesday, November 12, 2019
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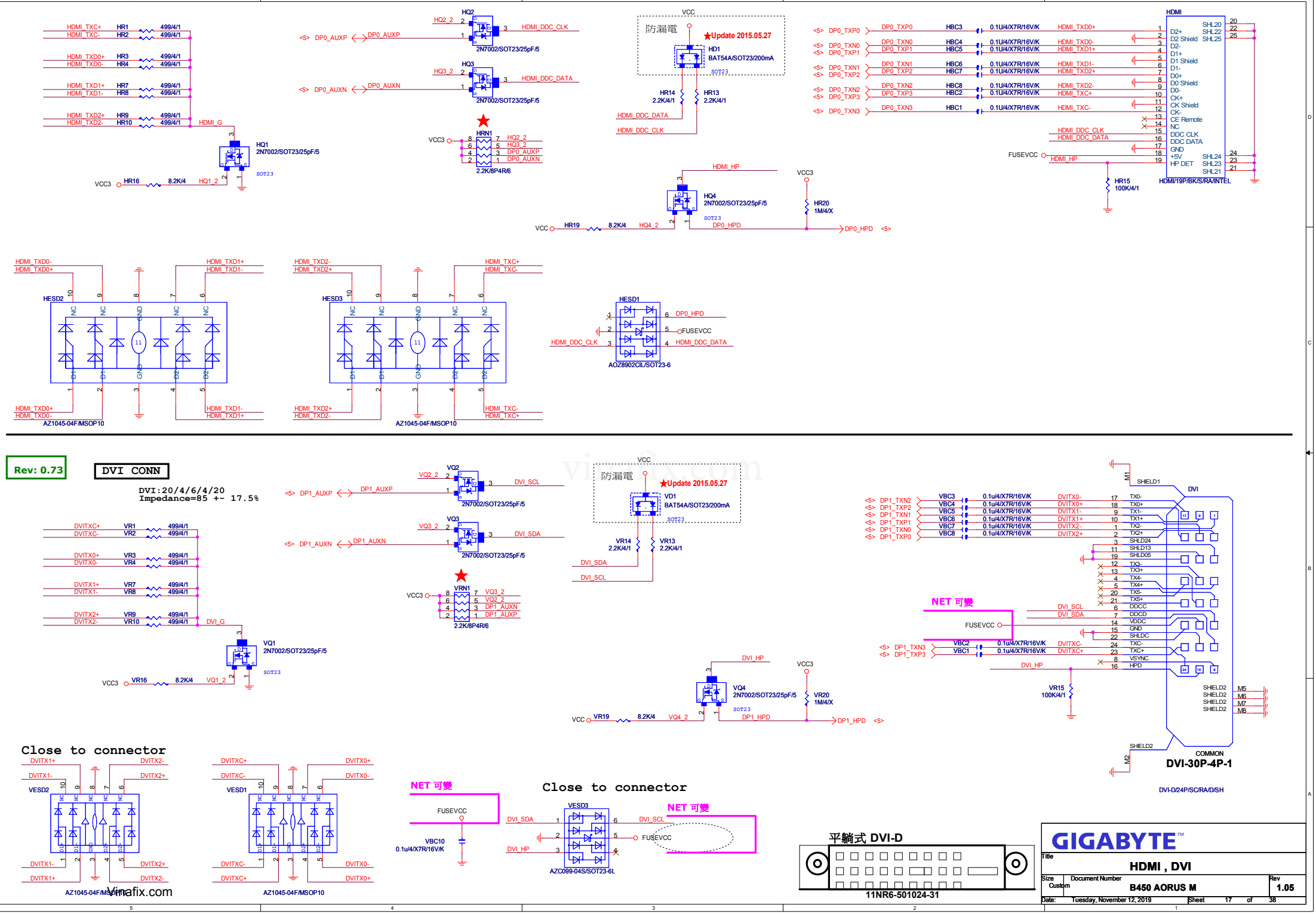
HDMI_TXC+ HR1 499/4/1
HDMI_TXC- HR2 499/4/1
HDMI_TXD0+ HR3 499/4/1
HDMI_TXD0- HR4 499/4/1
HDMI_TXD1+ HR7 499/4/1
HDMI_TXD1- HR8 499/4/1
HDMI_TXD2+ HR9 499/4/1
HDMI_TXD2- HR10 499/4/1
HDMI_G
HQ1 2N7002/SOT23/25pF/5
VCC3 HR16 8.2K/4 HQ1_2
HQ2 HQ2_2 HDMI_DDC_CLK
HQ3 HQ3_2 HDMI_DDC_DATA
<5> DP0_AUXP DP0_AUXP
<5> DP0_AUXN DP0_AUXN
2N7002/SOT23/25pF/5
HRN1 2.2K/8P4R/6
防漏電
★Update 2015.05.27
HD1 BAT54A/SOT23/200mA
HR14 2.2K/4/1
HR13 2.2K/4/1
HDMI_DDC_DATA
HDMI_DDC_CLK
HDMI
HDMI/19P/BK/S/RA/INTEL
HR15 100K/4/1
FUSEVCC
HDMI_HP
HQ4 2N7002/SOT23/25pF/5
HR20 1M/4/X
HR19 8.2K/4 HQ4_2
DP0_HPD
HESD2
HESD3
AZ1045-04F/MSOP10
HESD1
AOZ8902CIL/SOT23-6
Rev: 0.73
DVI CONN
DVI:20/4/6/4/20
Impedance=85 +- 17.5%
VQ1 2N7002/SOT23/25pF/5
VR16 8.2K/4 VQ1_2
VQ2 VQ2_2 DVI_SCL
VQ3 VQ3_2 DVI_SDA
VRN1 2.2K/8P4R/6
VD1 BAT54A/SOT23/200mA
VR14 2.2K/4/1
VR13 2.2K/4/1
VQ4 2N7002/SOT23/25pF/5
VR20 1M/4/X
VR19 8.2K/4 VQ4_2
DP1_HPD
NET 可變
DVI
DVI-30P-4P-1
DVI-D/24P/SC/RA/D/SH
Close to connector
VESD2
VESD1
VESD3
AZC099-04S/SOT23-6L
VBC10 0.1u/4/X7R/16V/K
平鋪式 DVI-D
11NR6-501024-31
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HDMI , DVI
Size Custom
Document Number B450 AORUS M
Rev 1.05
Date: Tuesday, November 12, 2019
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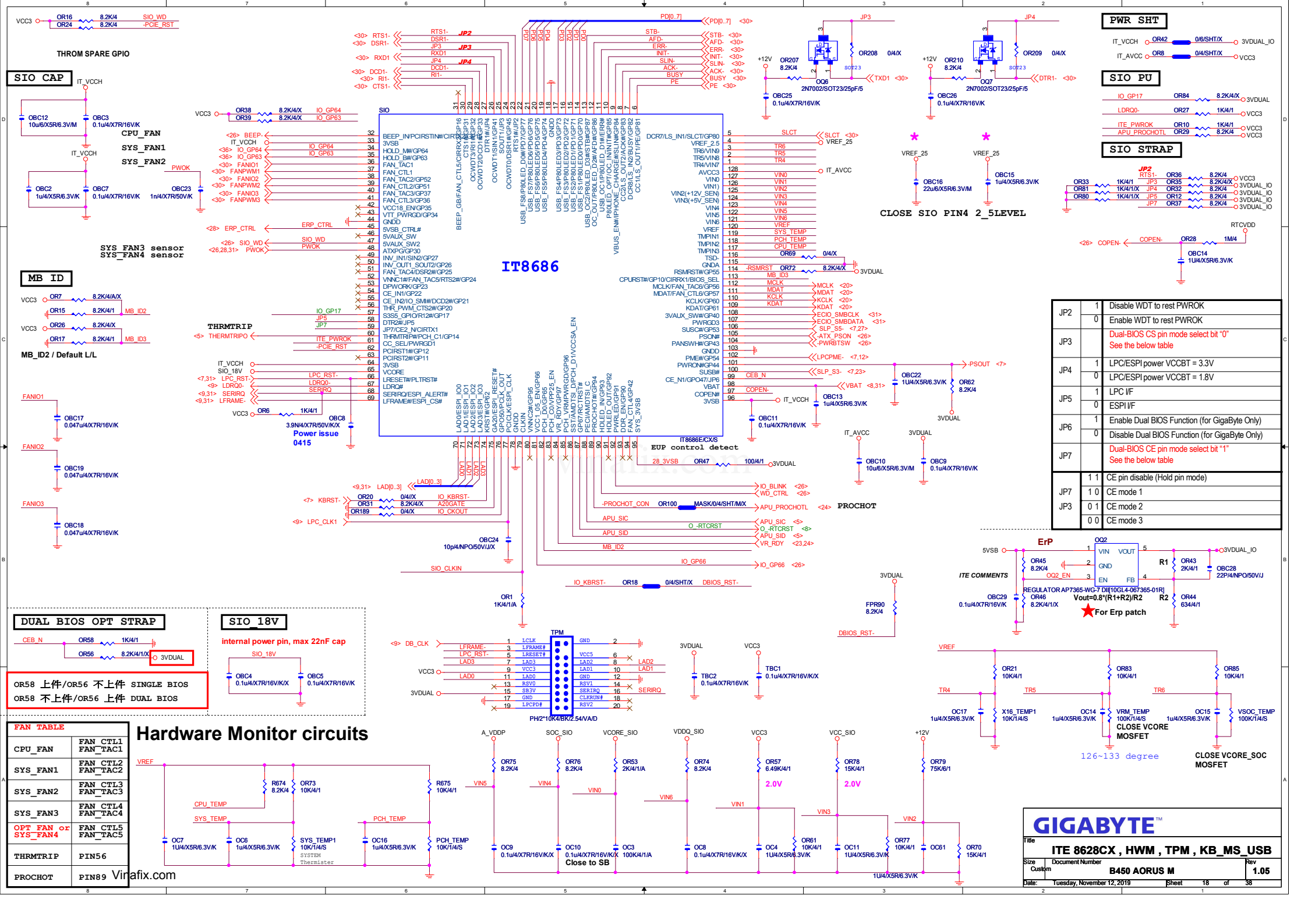

JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table

JP7	JP3	
1	1	CE pin disable (Hold pin mode)
1	0	CE mode 1
0	1	CE mode 2
0	0	CE mode 3

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

Title	ITE 8628CX , HWM , TPM , KB_MS_USB
Size	Custom
Document Number	B450 AORUS M
Rev	1.05
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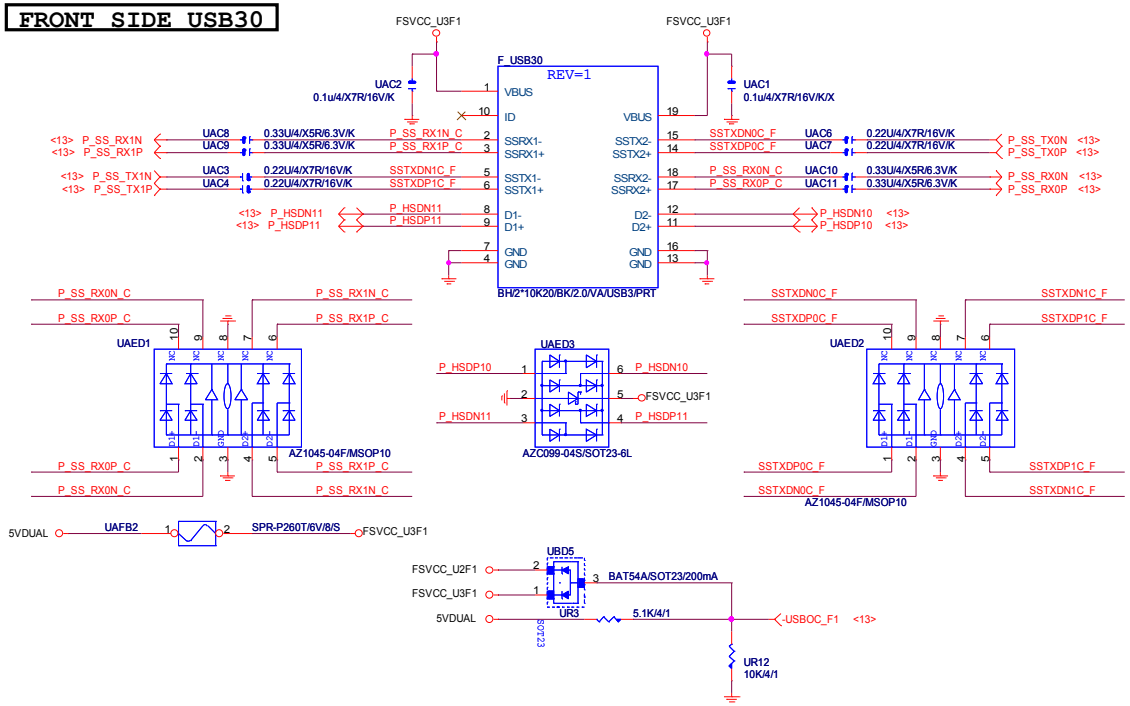
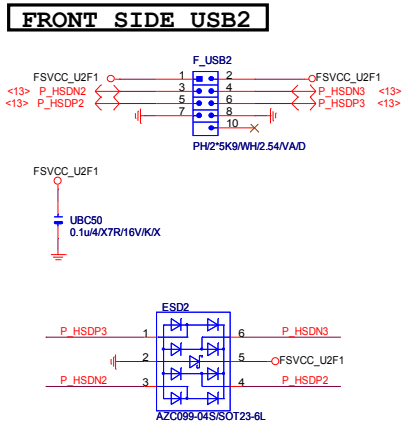
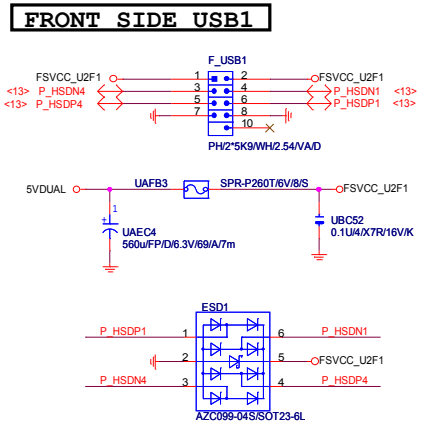
FRONT SIDE USB30



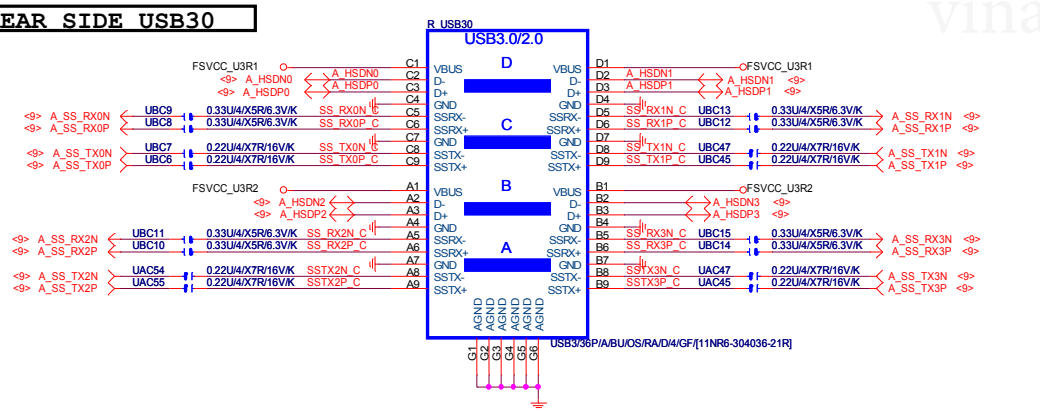
FRONT SIDE USB2

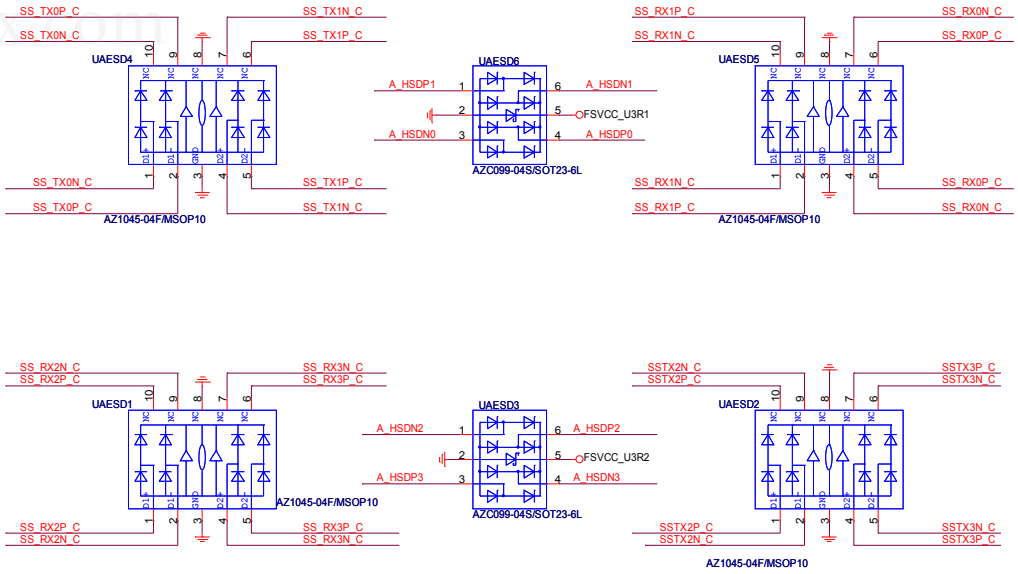


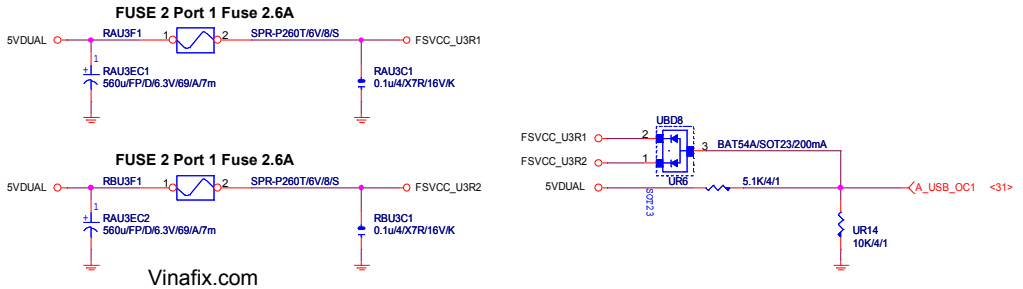
FRONT SIDE USB1



REAR SIDE USB30







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Title	F_USB30_20 , R_USB30		
Size: Custom	Document Number: B450 AORUS M		Rev: 1.05
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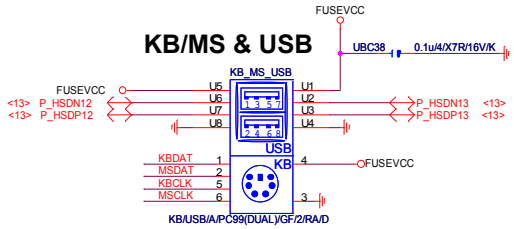
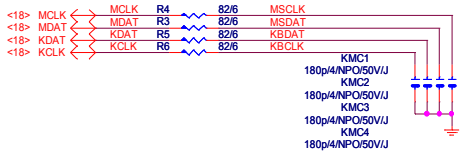
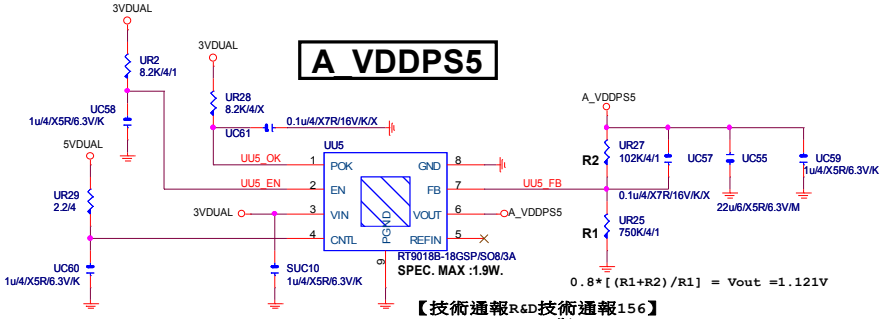
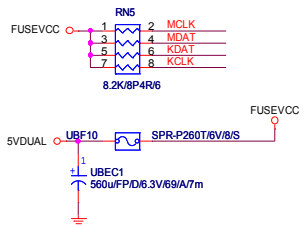


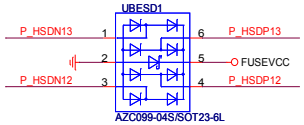


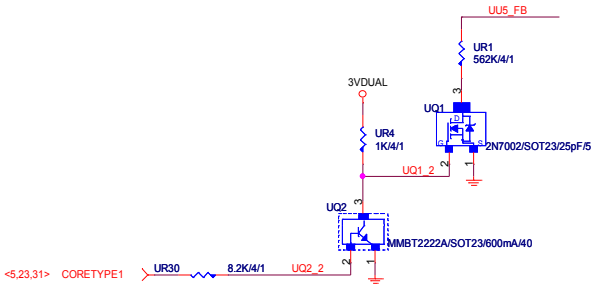


【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON)，
EM5103GE(EMC)做共用，針對PIN7(FB)分壓阻值部份
(R1/R2)須做修改為100K以上電阻值

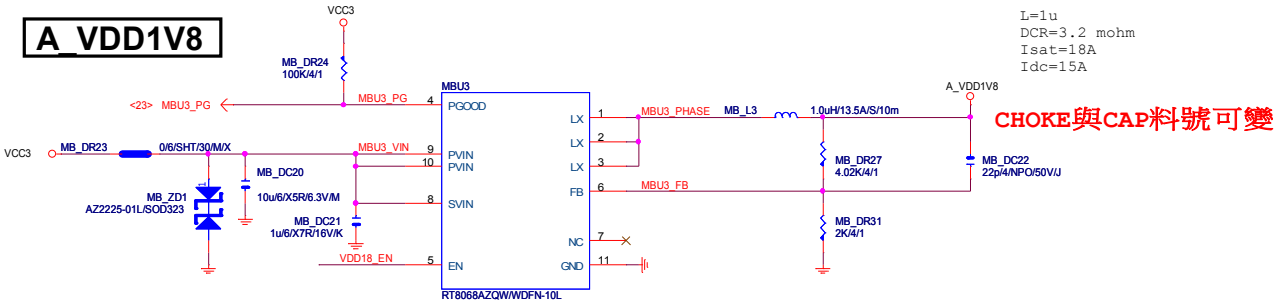
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V





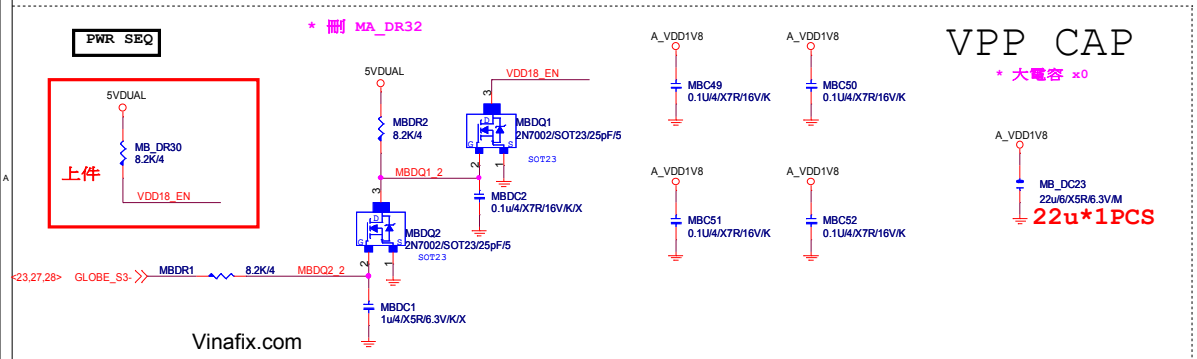


REV:0.4



L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A

CHOKE與CAP料號可變



VPP CAP
* 大電容 x0

22u*1PCS

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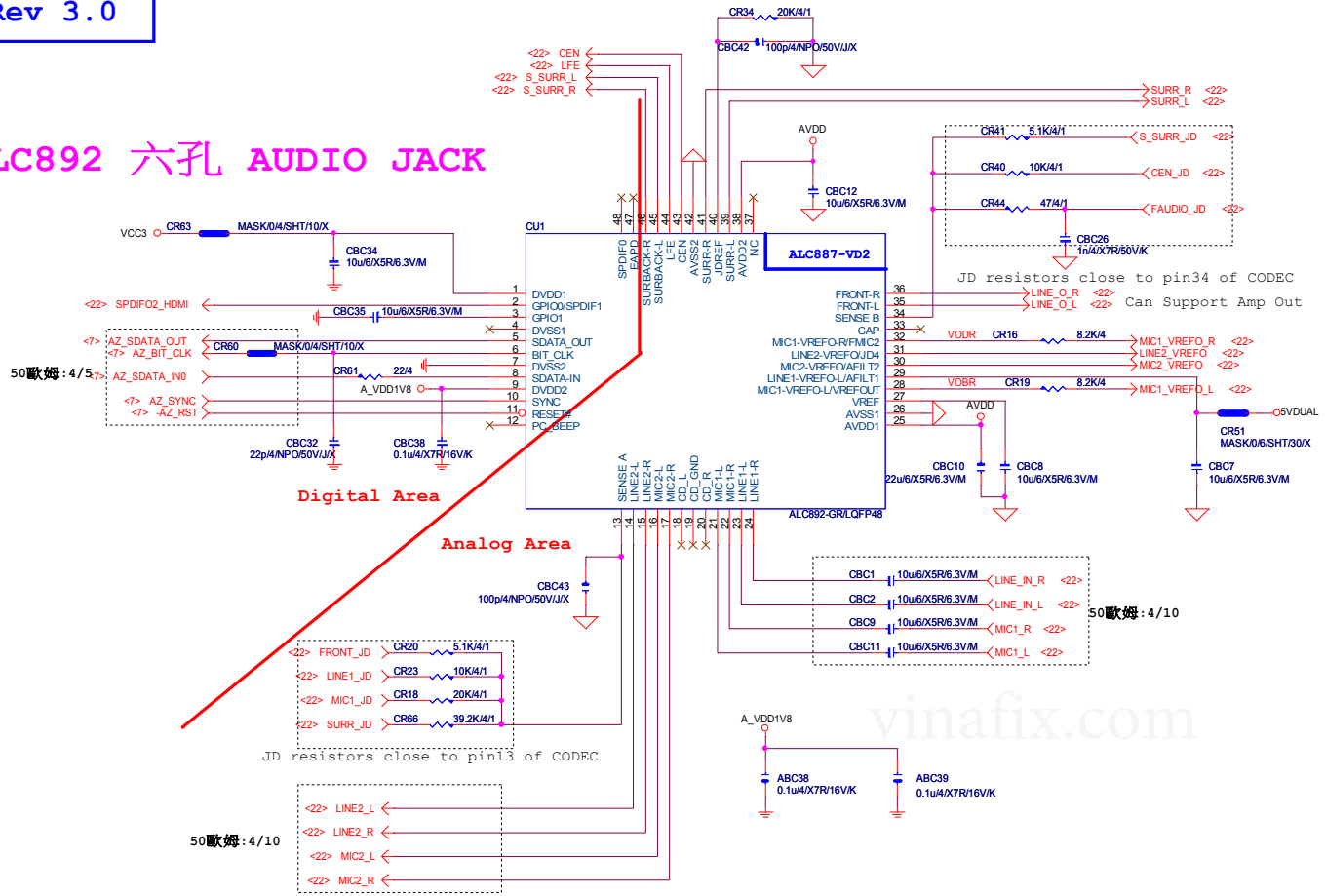
ALC892 六孔 AUDIO JACK



LAYOUT注意:螺絲孔下GND方式

1. MH1空間夠,下DGND
   空間不夠,才改為Isolate
2. MH2一律改為Isolate
3. Codec下方,第二層必須參考GND

MH1	MH2
DGND	Isolate

LAYOUT注意:要加

GND切割線

音效區域印刷

BOM OPTION :
1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

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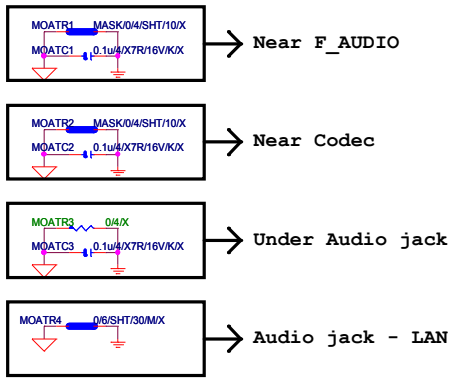
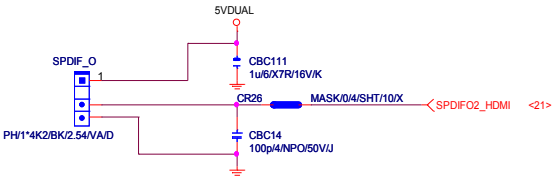
Rev 3.0

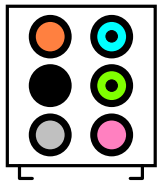


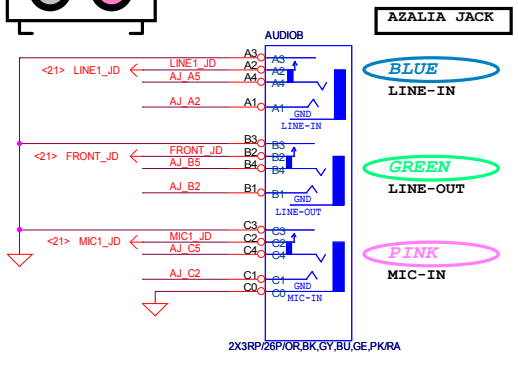
*量產前,0ohm改short pad

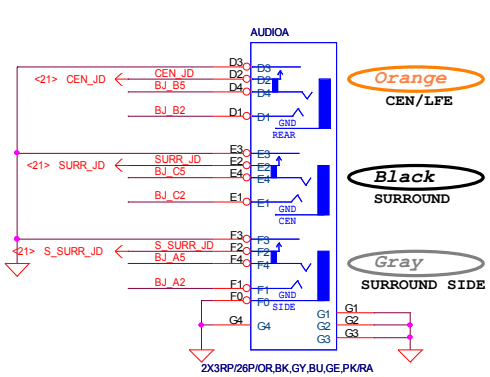


For HDMI SPDIF （依SPEC保留或移除）

AZALIA JACK







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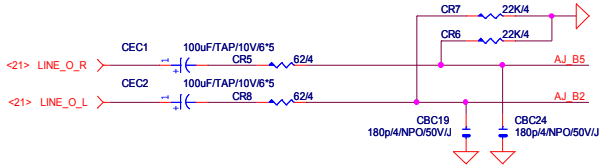
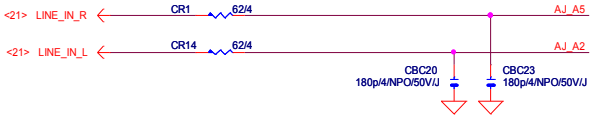
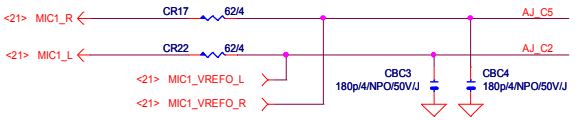
LINE-OUT



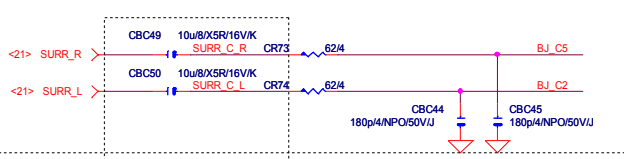
LINE-IN



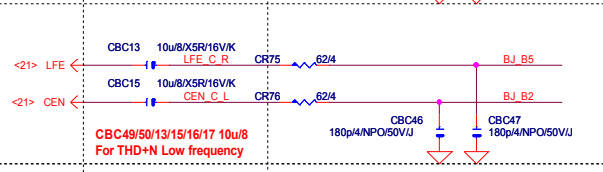
MIC-IN



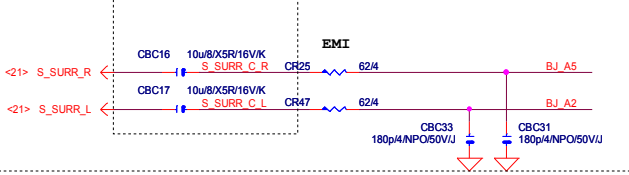
SURROUND



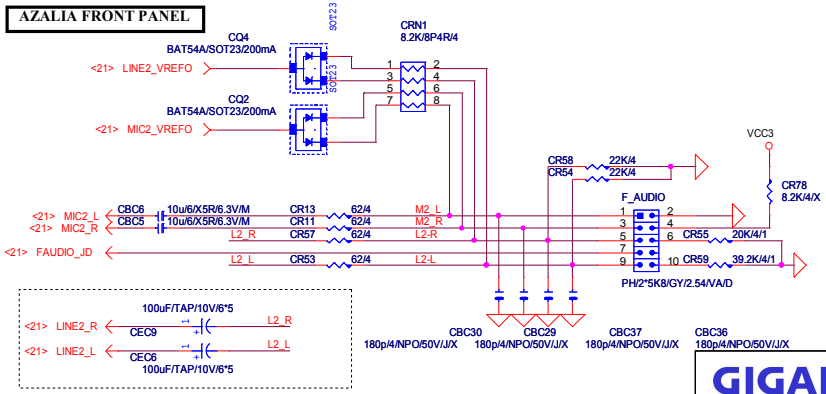
CEN/LFE



SURR BACK



AZALIA FRONT PANEL



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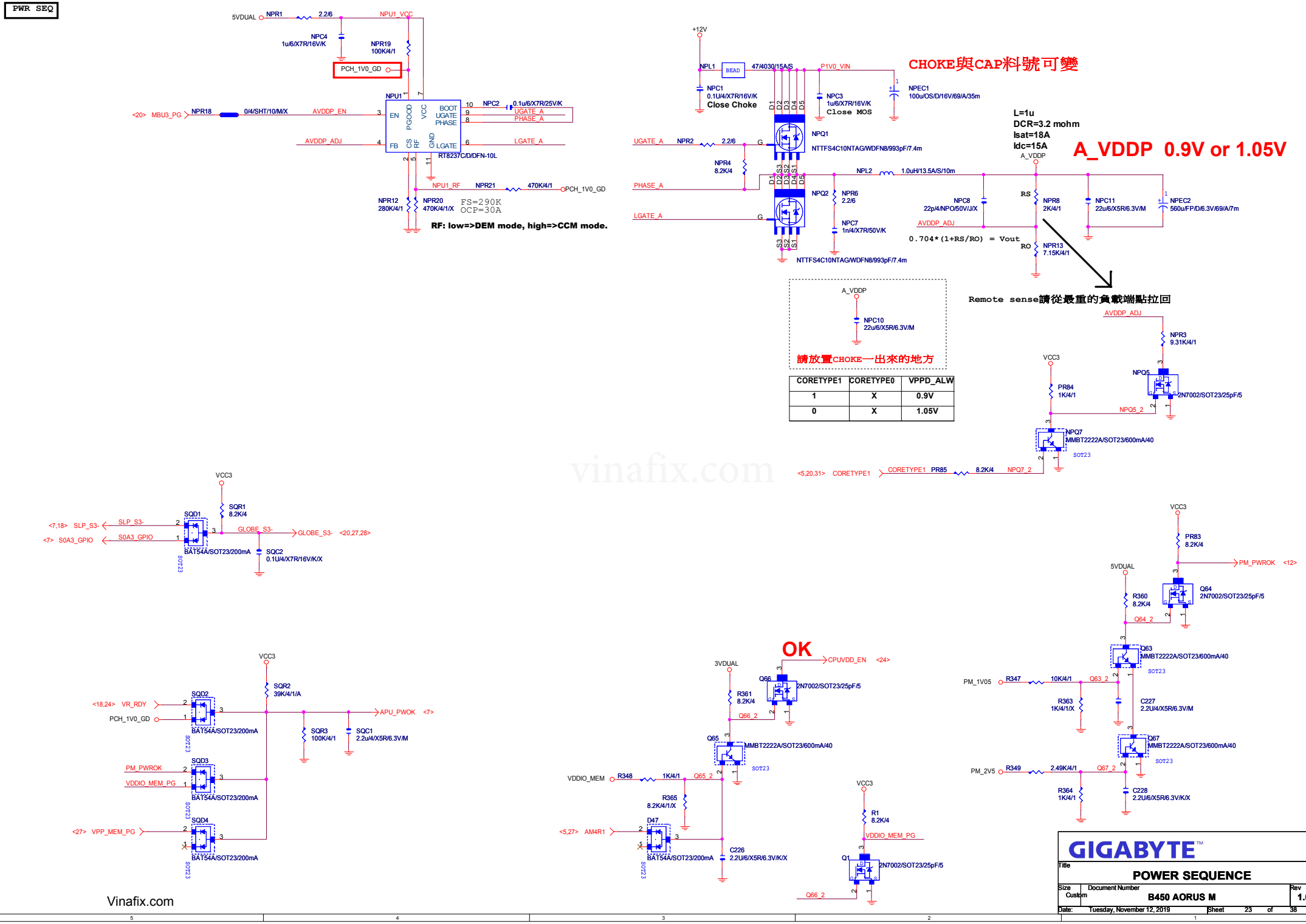
PWR SEQ



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Title	POWER SEQUENCE	
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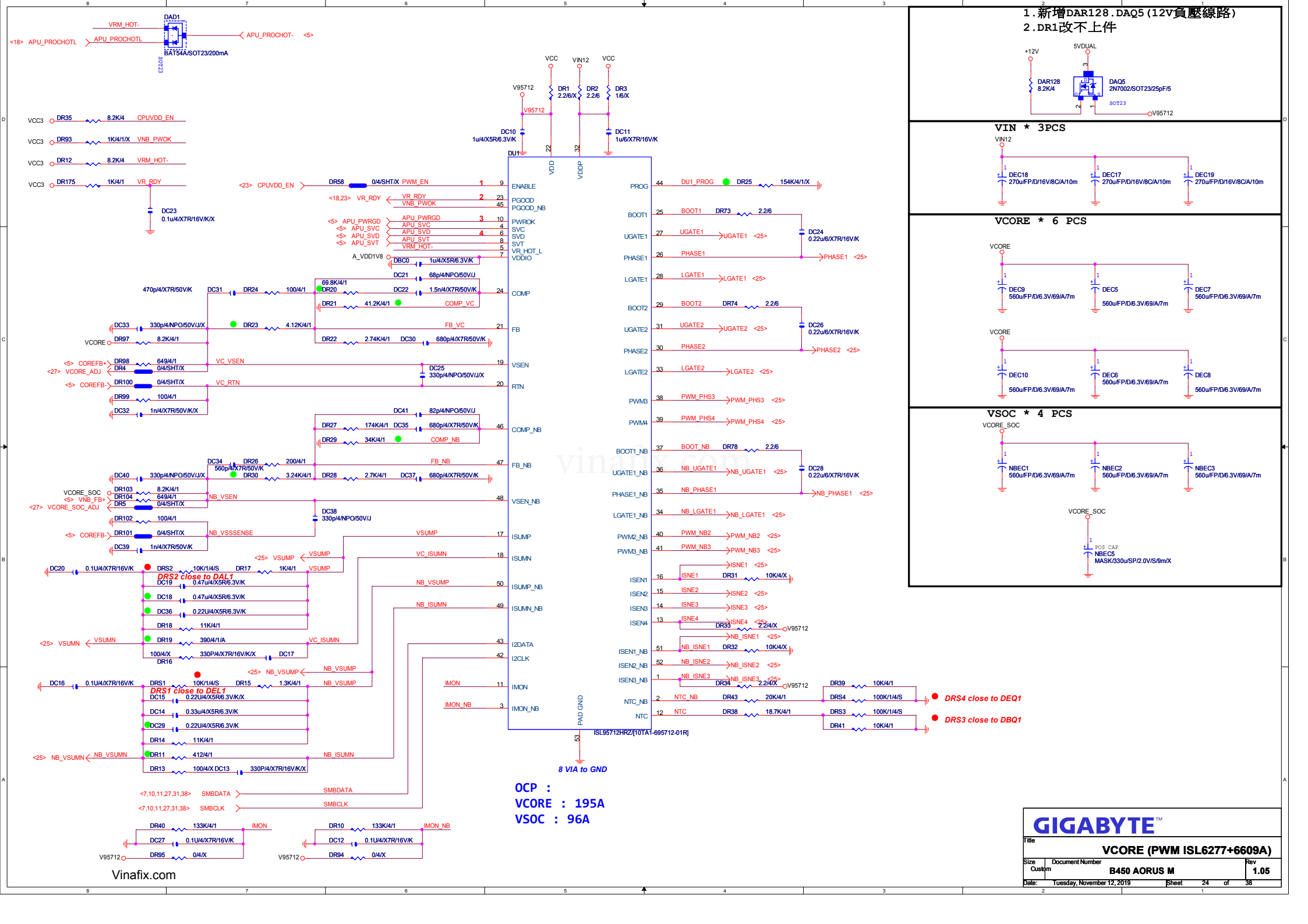
1.新增DAR128.DAQ5(12V負壓線路)
2.DR1改不上件
VIN * 3PCS
VCORE * 6 PCS
VSOC * 4 PCS
DU1
ISL95712HRZ/[10TA1-695712-01R]
DRS2 close to DAL1
DRS1 close to DEL1
DRS4 close to DEQ1
DRS3 close to DBQ1
8 VIA to GND
OCP :
VCORE : 195A
VSOC : 96A
Vinafix.com
GIGABYTE
VCORE (PWM ISL6277+6609A)
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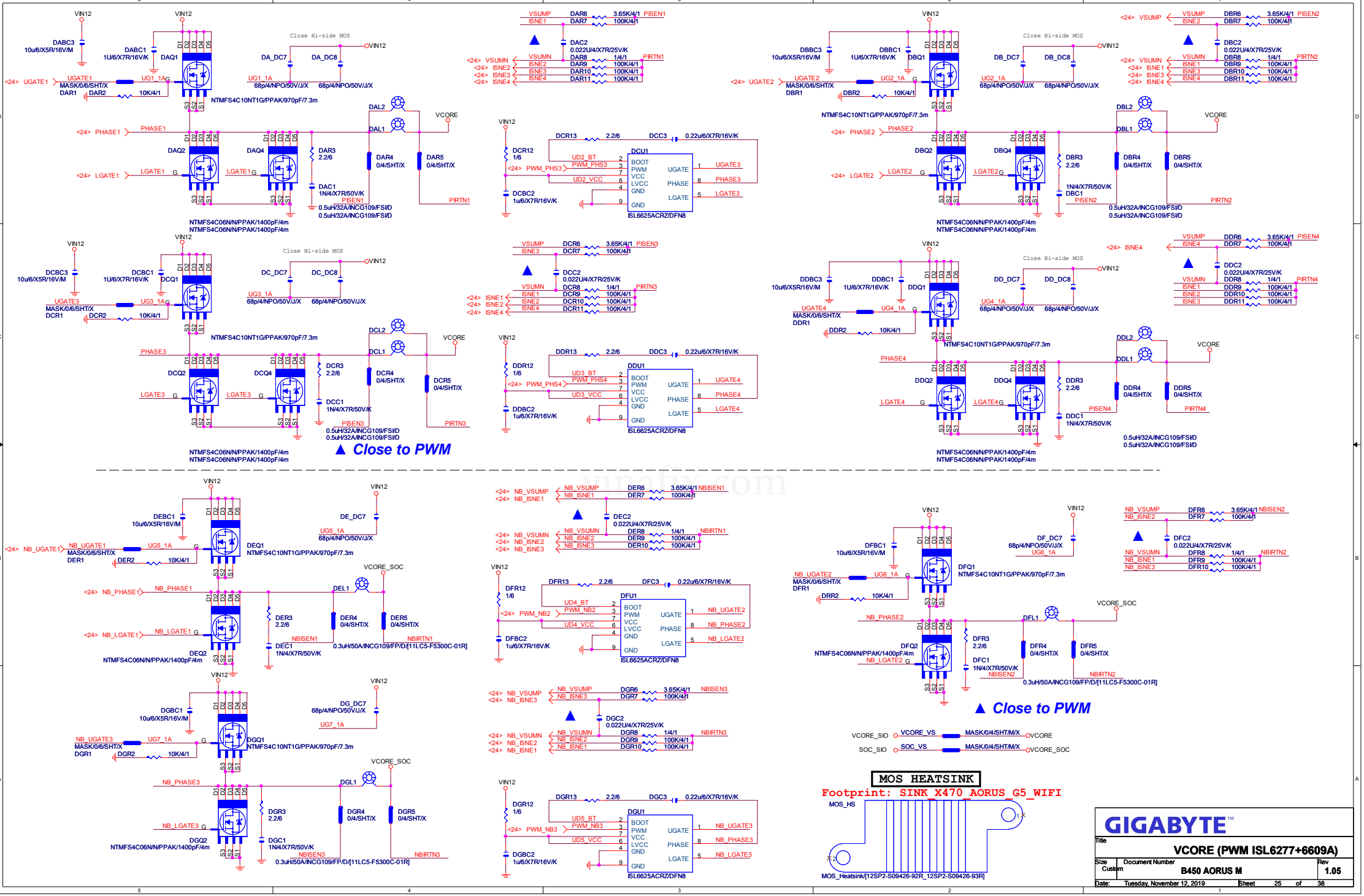
VIN12
VCORE
VCORE_SOC
Close Hi-side MOS
NTMFS4C10NT1G/PPAK/970pF/7.3m
NTMFS4C06N/N/PPAK/1400pF/4m
ISL6625ACRZ/DFN8
0.5uH/32A/INCG109/FSI/D
0.3uH/50A/INCG109/FP/D/[11LC5-F5300C-01R]
▲ Close to PWM
MOS HEATSINK
Footprint: SINK_X470_AORUS_G5_WIFI
MOS_Heatsink/[12SP2-S09426-92R_12SP2-S09426-93R]
GIGABYTE
VCORE (PWM ISL6277+6609A)
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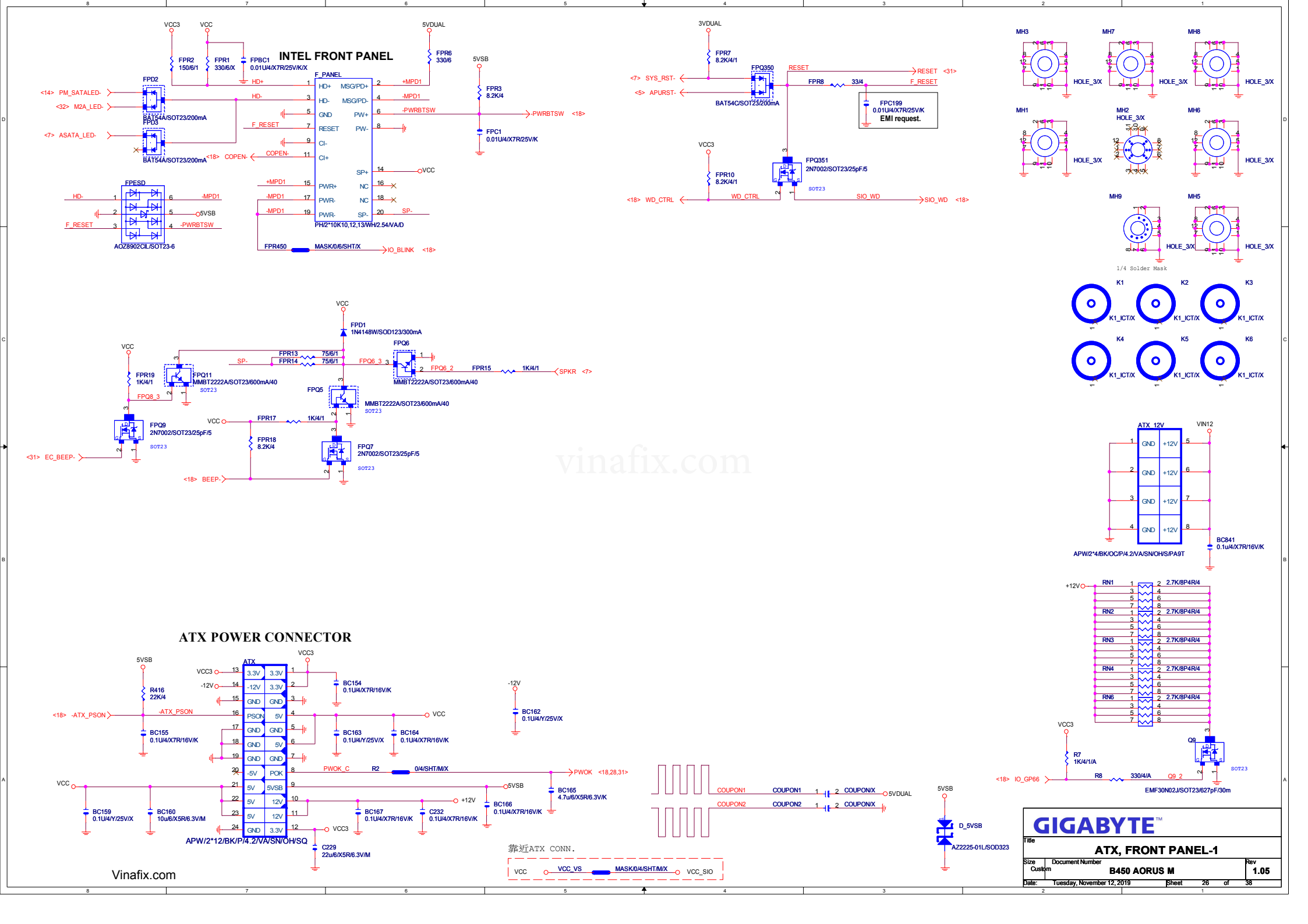
INTEL FRONT PANEL
F_PANEL
PH/2*10K10,12,13/WH/2.54/VA/D
FPESD
AOZ8902CIL/SOT23-6
ATX POWER CONNECTOR
ATX
APW/2*12/BK/P/4.2/VA/SN/OH/SQ
APW/2*4/BK/OC/P/4.2/VA/SN/OH/S/PA9T
EMF30N02J/SOT23/627pF/30m
靠近ATX CONN.
GIGABYTE
ATX, FRONT PANEL-1
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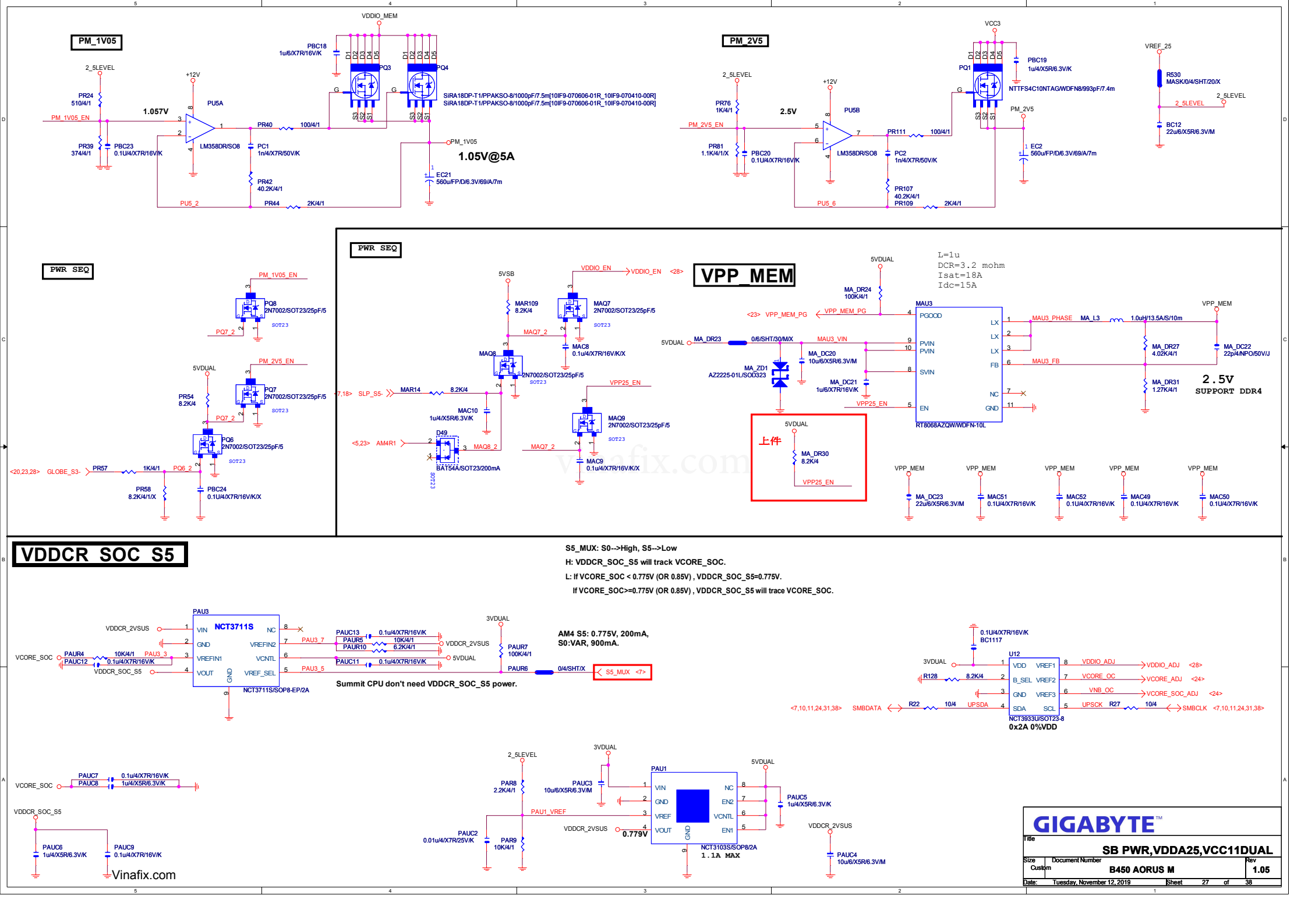
PM_1V05
PM_2V5
PWR SEQ
VPP_MEM
VDDCR SOC S5
L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A
1.057V
2.5V
1.05V@5A
2.5V
SUPPORT DDR4
S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.
AM4 S5: 0.775V, 200mA,
S0:VAR, 900mA.
Summit CPU don't need VDDCR_SOC_S5 power.
0x2A 0%VDD
1.1A MAX
GIGABYTE
SB PWR,VDDA25,VCC11DUAL
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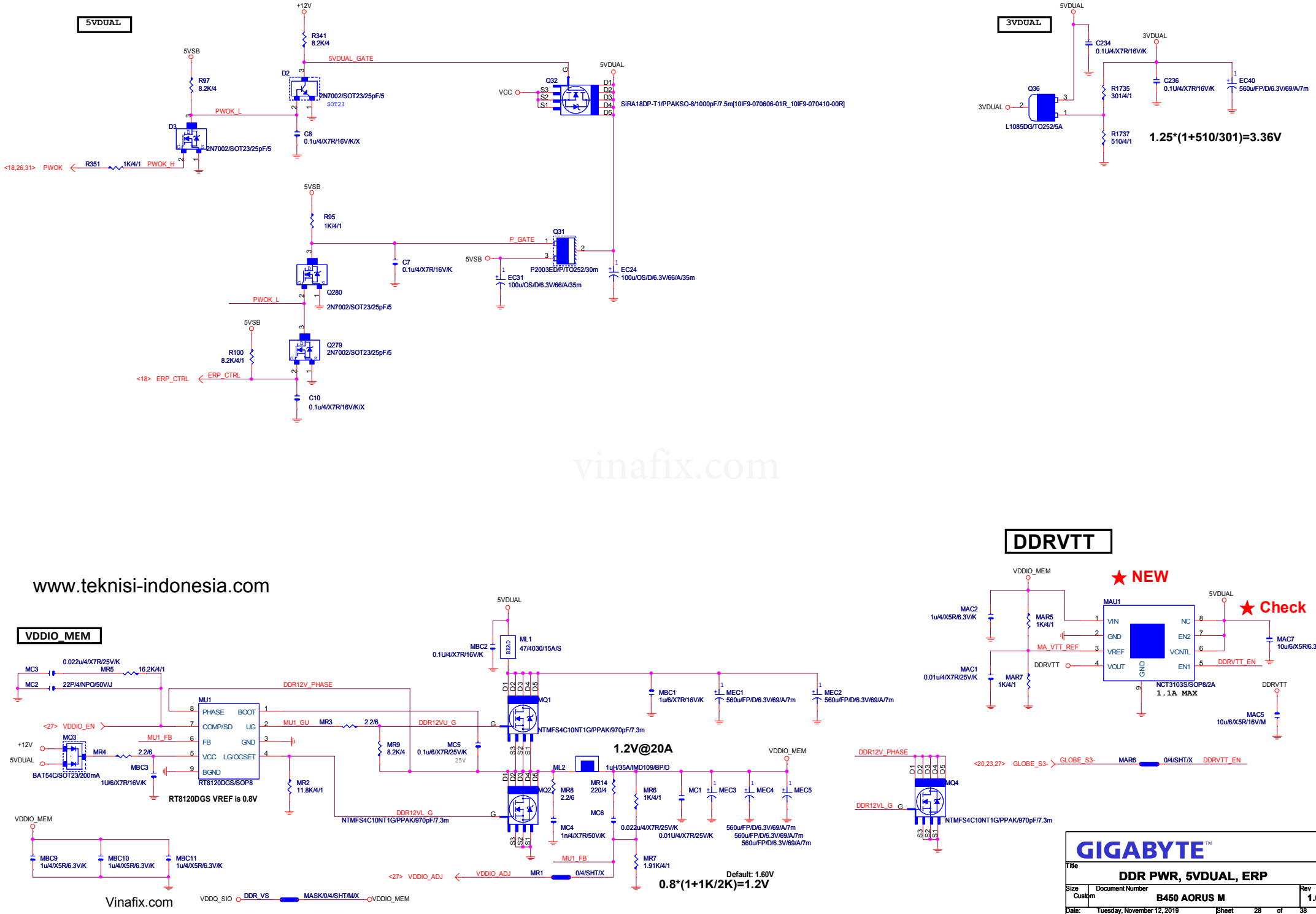
5VDUAL
+12V
R341
8.2K/4
5VDUAL_GATE
5VSB
R97
8.2K/4
D2
2N7002/SOT23/25pF/5
SOT23
PWOK_L
D3
2N7002/SOT23/25pF/5
C8
0.1u/4/X7R/16V/K/X
<18,26,31> PWOK
R351
1K/4/1
PWOK_H
VCC
Q32
SiRA18DP-T1/PPAKSO-8/1000pF/7.5m[10IF9-070606-01R_10IF9-070410-00R]
R95
1K/4/1
P_GATE
Q31
P2003EDP/TO252/30m
C7
0.1u/4/X7R/16V/K
EC31
100u/OS/D/6.3V/66/A/35m
EC24
100u/OS/D/6.3V/66/A/35m
Q280
2N7002/SOT23/25pF/5
R100
8.2K/4/1
Q279
2N7002/SOT23/25pF/5
<18> ERP_CTRL
C10
0.1u/4/X7R/16V/K/X
3VDUAL
C234
0.1U/4/X7R/16V/K
C236
0.1U/4/X7R/16V/K
EC40
560u/FP/D/6.3V/69/A/7m
Q36
L1085DG/TO252/5A
R1735
301/4/1
R1737
510/4/1
1.25*(1+510/301)=3.36V
www.teknisi-indonesia.com
VDDIO_MEM
MC3
0.022u/4/X7R/25V/K
MR5
16.2K/4/1
MC2
22P/4/NPO/50V/J
<27> VDDIO_EN
MU1
PHASE
BOOT
COMP/SD
UG
FB
GND
VCC
LG/OCSET
BGND
RT8120DGS/SOP8
DDR12V_PHASE
MU1_GU
MR3
2.2/6
DDR12VU_G
MU1_FB
MQ3
BAT54C/SOT23/200mA
MR4
2.2/6
MBC3
1U/6/X7R/16V/K
MR9
8.2K/4
MC5
0.1u/6/X7R/25V/K
MR2
11.8K/4/1
RT8120DGS VREF is 0.8V
DDR12VL_G
NTMFS4C10NT1G/PPAK/970pF/7.3m
MBC2
0.1U/4/X7R/16V/K
ML1
47/4030/15A/S
MQ1
NTMFS4C10NT1G/PPAK/970pF/7.3m
MBC1
1u/6/X7R/16V/K
MEC1
560u/FP/D/6.3V/69/A/7m
MEC2
560u/FP/D/6.3V/69/A/7m
1.2V@20A
ML2
1uH/35A/IMD109/BP/D
MQ2
MR8
2.2/6
MR14
220/4
MR6
1K/4/1
MC6
MC4
1n/4/X7R/50V/K
0.022u/4/X7R/25V/K
0.01U/4/X7R/25V/K
MC1
MEC3
MEC4
MEC5
560u/FP/D/6.3V/69/A/7m
560u/FP/D/6.3V/69/A/7m
560u/FP/D/6.3V/69/A/7m
MR7
1.91K/4/1
<27> VDDIO_ADJ
VDDIO_ADJ
MR1
0/4/SHT/X
Default: 1.60V
0.8*(1+1K/2K)=1.2V
MBC9
1u/4/X5R/6.3V/K
MBC10
1u/4/X5R/6.3V/K
MBC11
1u/4/X5R/6.3V/K
Vinafix.com
VDDQ_SIO
DDR_VS
MASK/0/4/SHT/M/X
VDDIO_MEM
DDRVTT
★ NEW
★ Check
MAU1
VIN
GND
VREF
VOUT
NC
EN2
VCNTL
EN1
NCT3103S/SOP8/2A
1.1A MAX
MAC2
1u/4/X5R/6.3V/K
MAR5
1K/4/1
MA_VTT_REF
MAC1
0.01u/4/X7R/25V/K
MAR7
1K/4/1
MAC7
10u/6/X5R/6.3V/M
DDRVTT_EN
MAC5
10u/6/X5R/16V/M
MQ4
NTMFS4C10NT1G/PPAK/970pF/7.3m
<20,23,27> GLOBE_S3-
MAR6
0/4/SHT/X
GIGABYTE
DDR PWR, 5VDUAL, ERP
Size
Custom
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LAN:RTL8118 | R2.03

EMI SHORT PAD

PS:視EMI需求

LAN POWER

(CLOSE LAU1 PIN22,30,3,8)

LABC2:1U CLOSE PIN22[REALTEK REQ]

LAN POWER

note: lan power連接及電流

(CLOSE LAU1 PIN23)

LAN POWER

(CLOSE LAU1 PIN:11,32)

PWR SURGE

PWR SURGE

LABC18,27:CLOSE PIN11[REALTEK SURGE]

LABC14,20:CLOSE PIN32[REALTEK SURGE]

LAN POWER

(CLOSE LAU1 PIN24)

LAN POWER

note: lan power連接及電流

可變

RTL8111G(S)/8106E

RTL8118-CG/S/[10HP2-408118-20R]

SRCCLK-->50歐姆:[18/4/10/4/18]

FOR ERP WAKEUP

MDI ESD

AZC399-04S.R7G/SOT23-6L/[10DEF-510399-10R]

AZC399-04S.R7G/SOT23-6L/[10DEF-510399-10R]

L1+CLK REQ# 節能:

需對應LA_SRCCLK_LAN之CLKREQ#

LA_ ML-->80歐姆:[15/5/5/5/15]

USB_LAN CONNECTOR

LAN 100 Ohm

USB 90 Ohm

USB31_LAN

USB3.0

USB3.0

USB3.1+LAN/1G/RE/GO,Y/OS/RA/D/1/15KV

AZ164S-04F.R7G/DFN10/[10DE2-510164-10R_10DE2-508809-10R]

AZC099-04S/SOT23-6L

AZ164S-04F.R7G/DFN10/[10DE2-510164-10R_10DE2-508809-10R]

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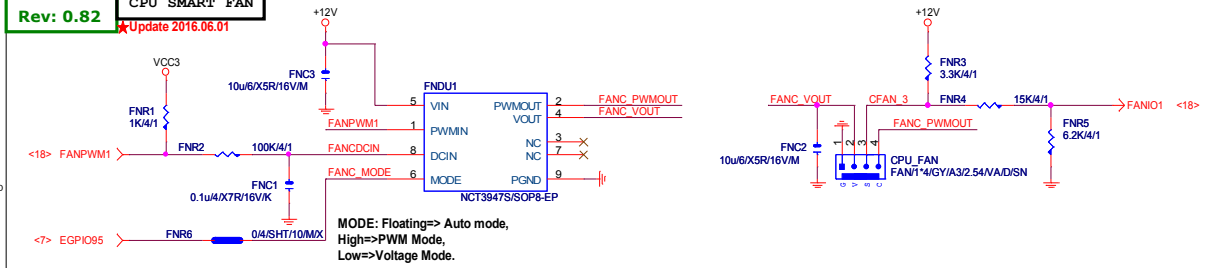
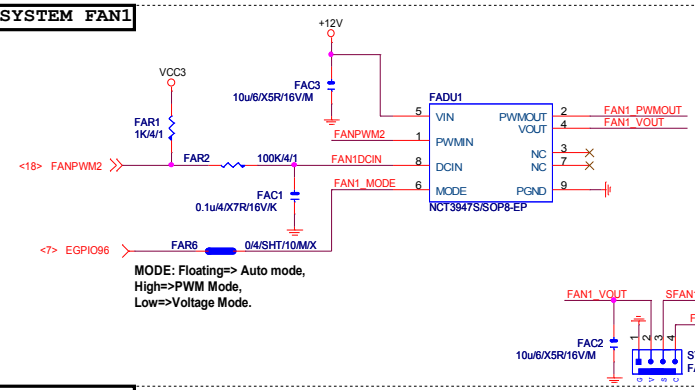
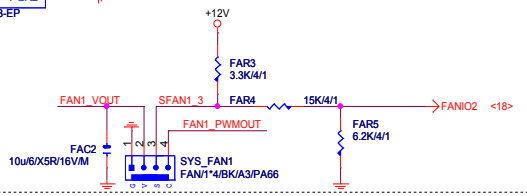
CPU SMART FAN

★Update 2016.06.01

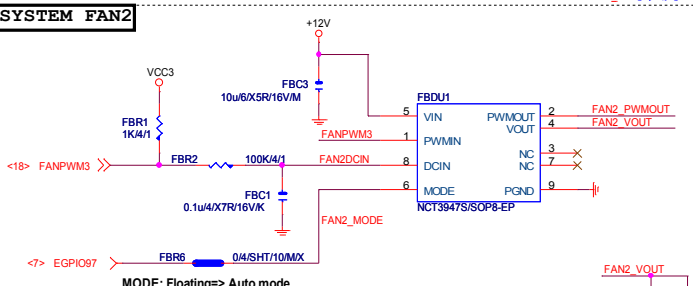


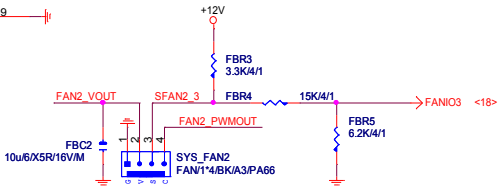
SYSTEM FAN1





SYSTEM FAN2





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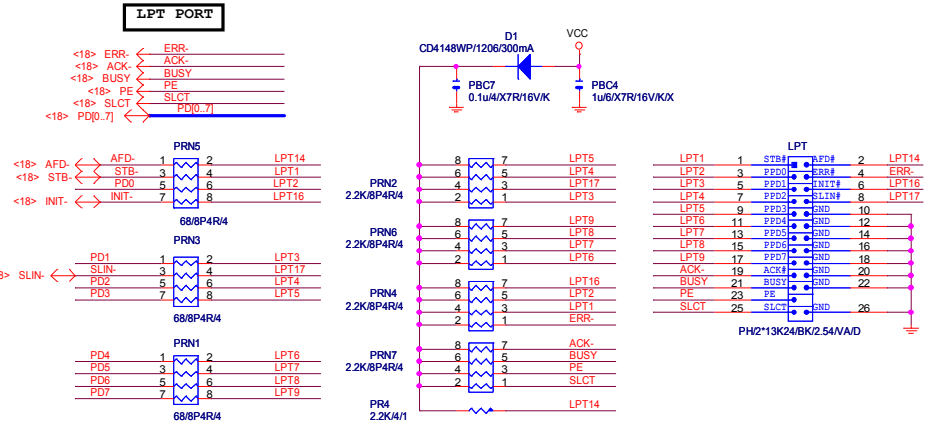
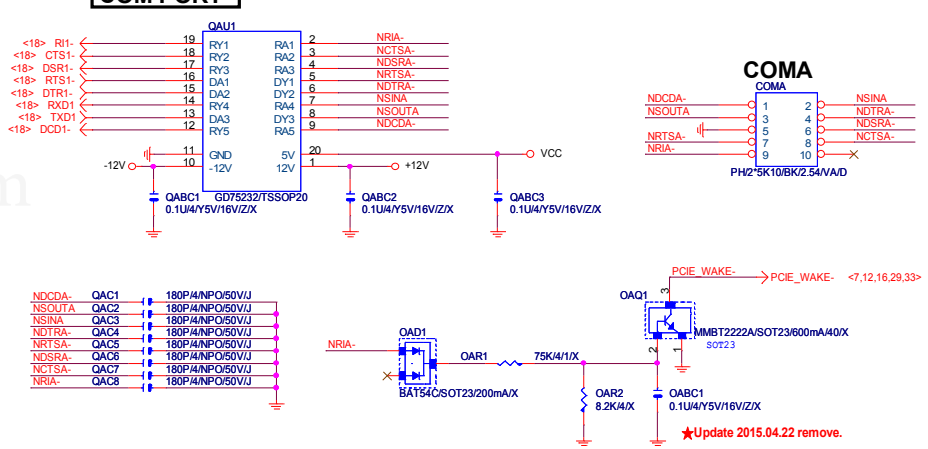
LPT PORT



COM PORT



GIGABYTE™

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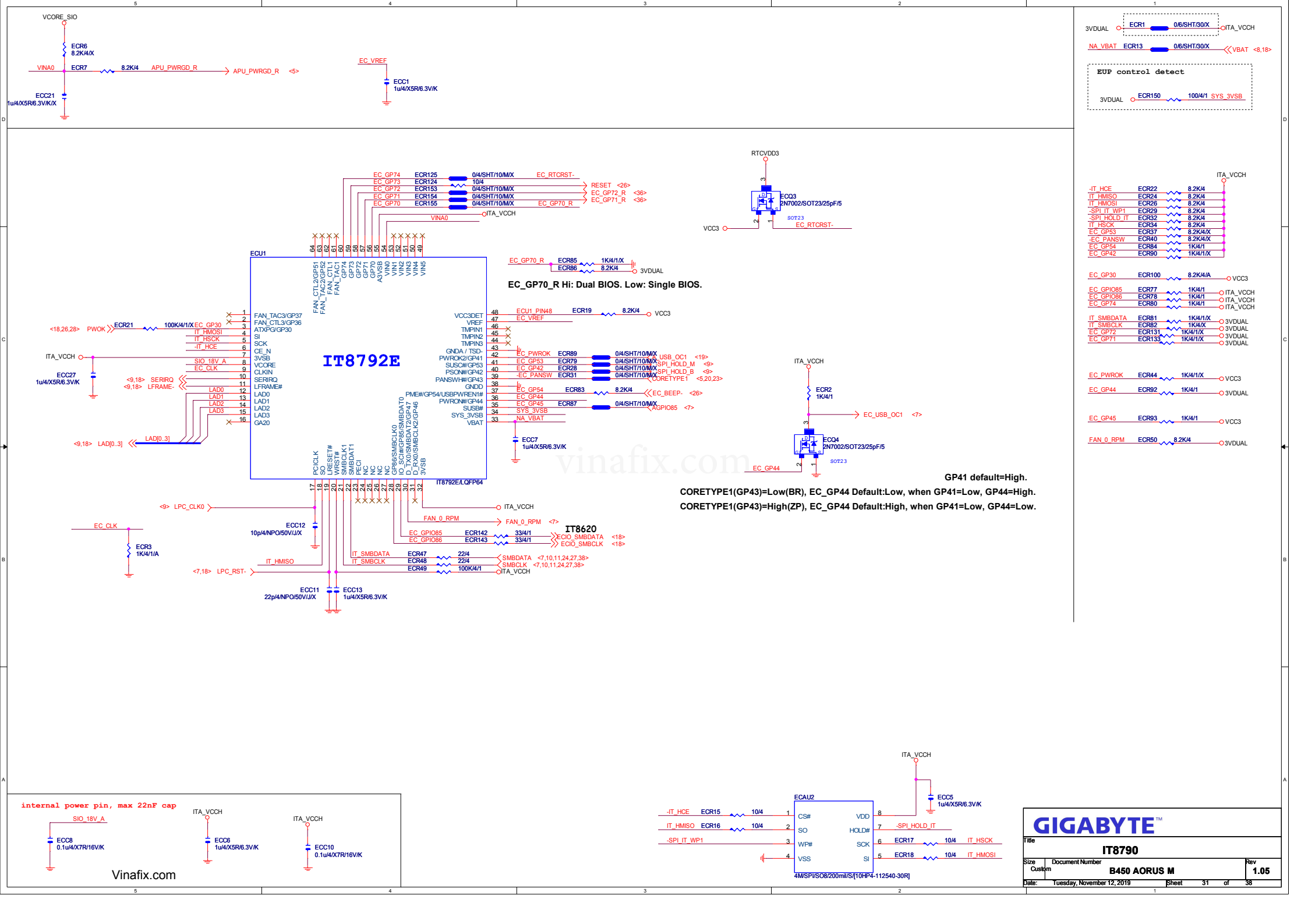
IT8792E
IT8620
ECU1
ECU2
EC_GP70_R Hi: Dual BIOS. Low: Single BIOS.
GP41 default=High.
CORETYPE1(GP43)=Low(BR), EC_GP44 Default:Low, when GP41=Low, GP44=High.
CORETYPE1(GP43)=High(ZP), EC_GP44 Default:High, when GP41=Low, GP44=Low.
EUP control detect
internal power pin, max 22nF cap
Vinafix.com
GIGABYTE
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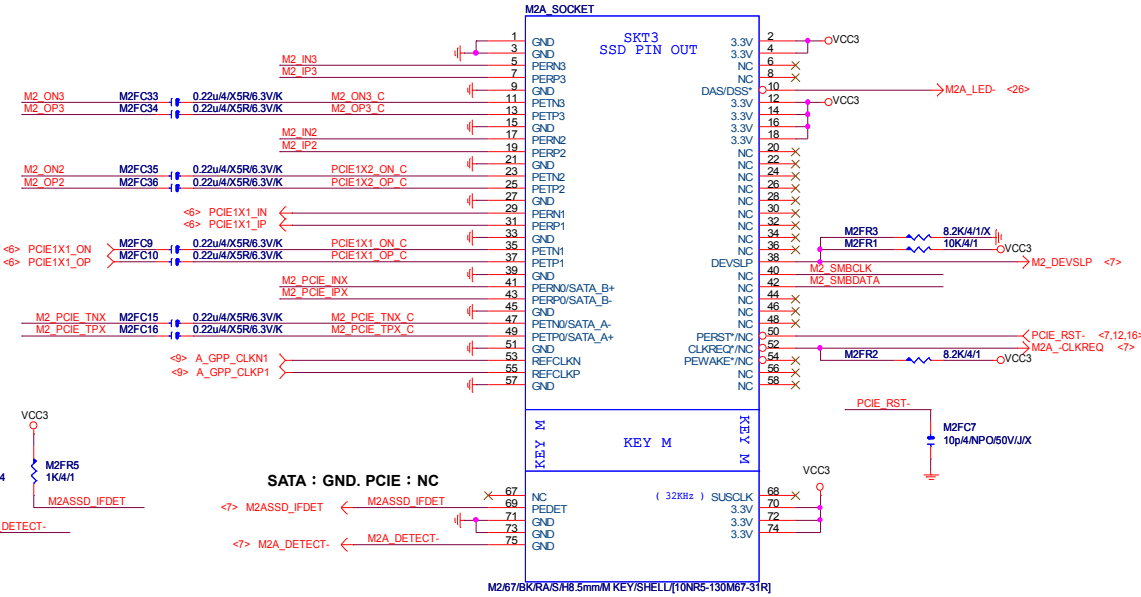
Rev 0.5

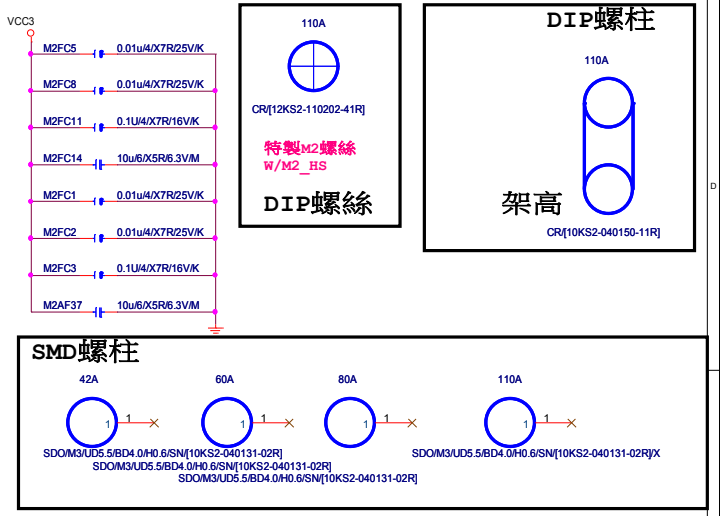
M.2 Lane4 from AM4 port3

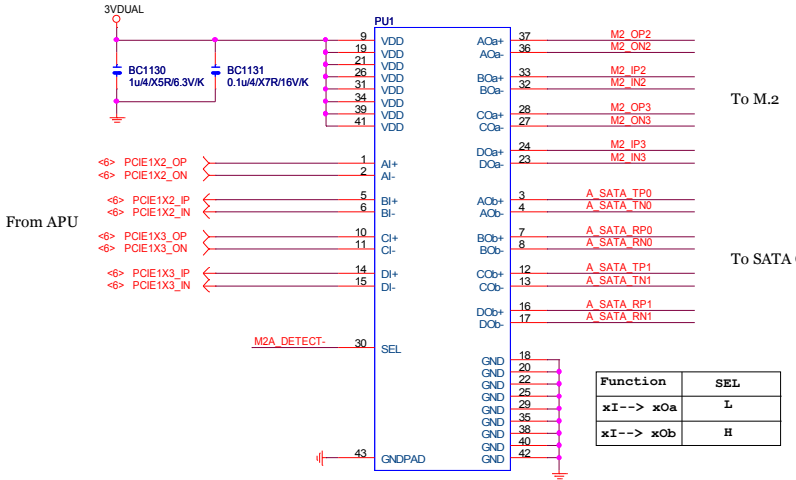
M.2 Lane4 from AM4 port2

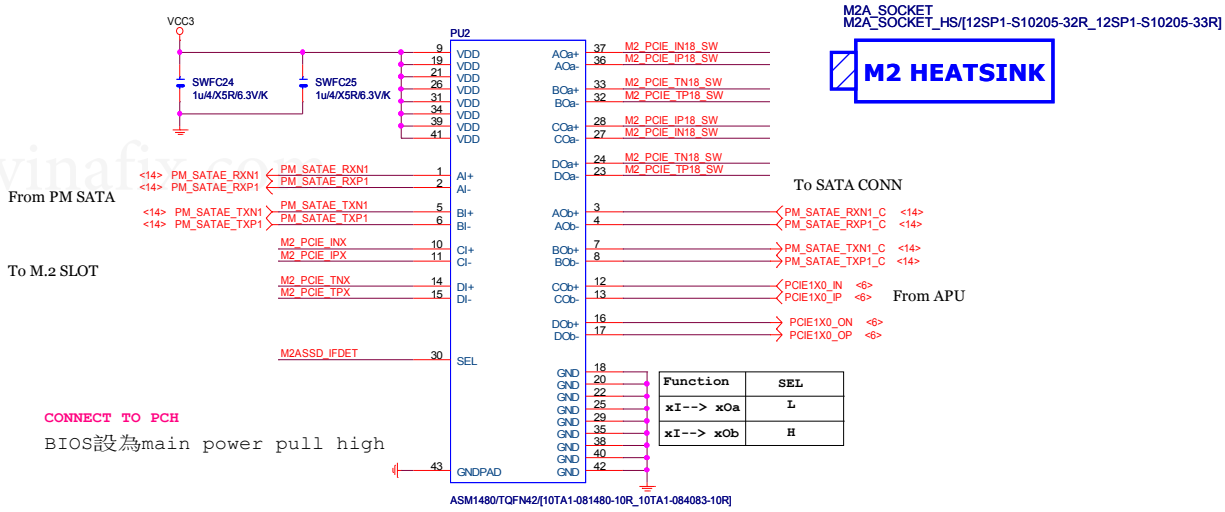
M.2 Lane4 from AM4 port1

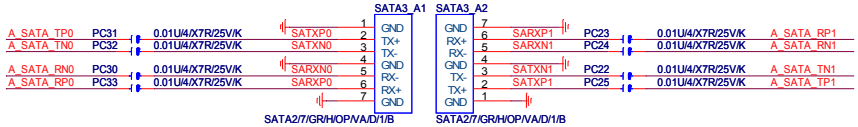
by SWITCH Select

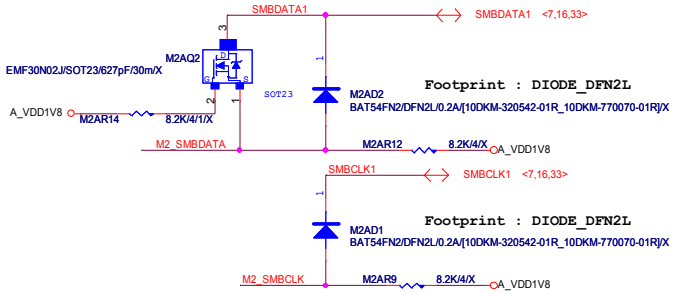












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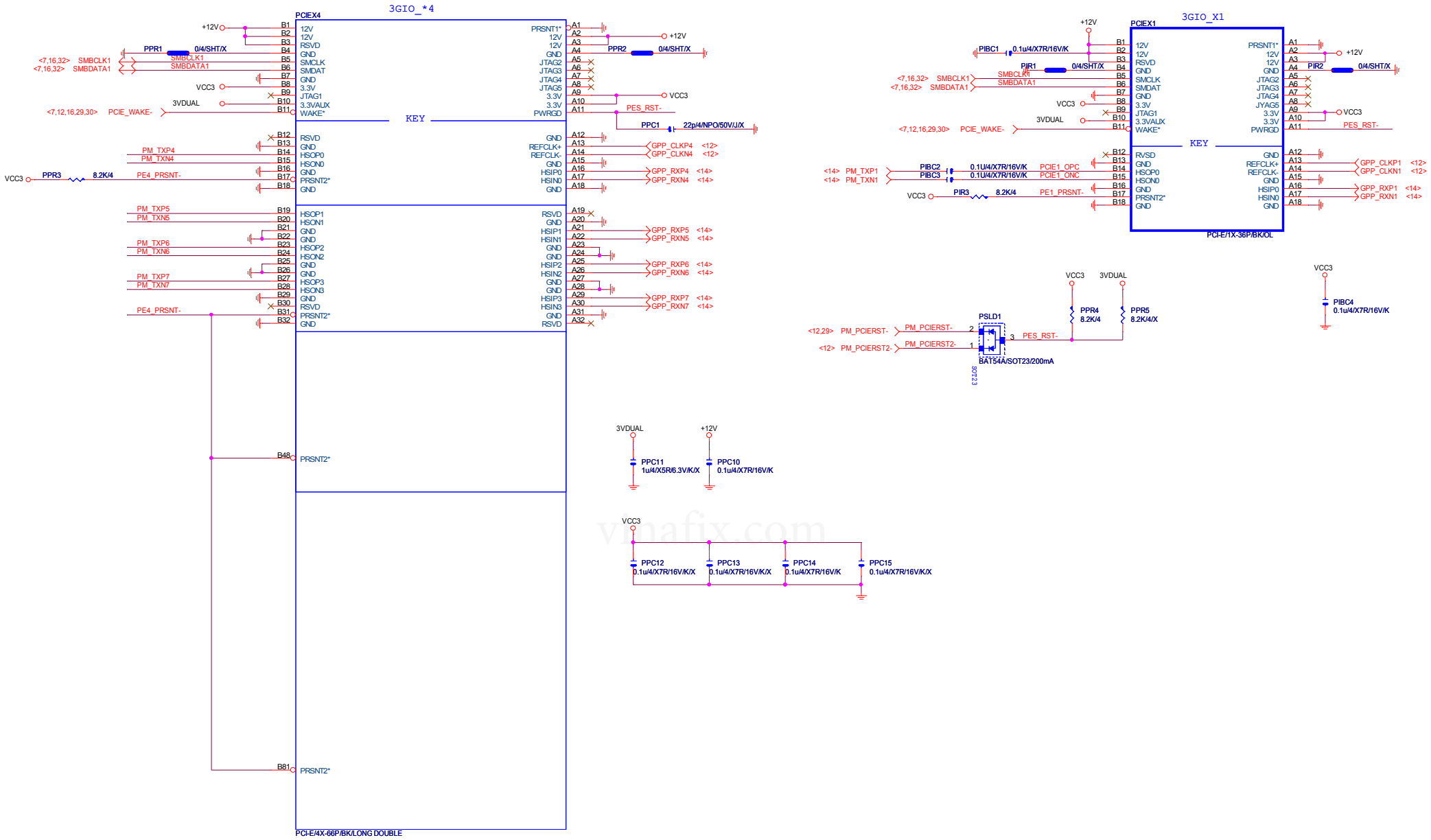

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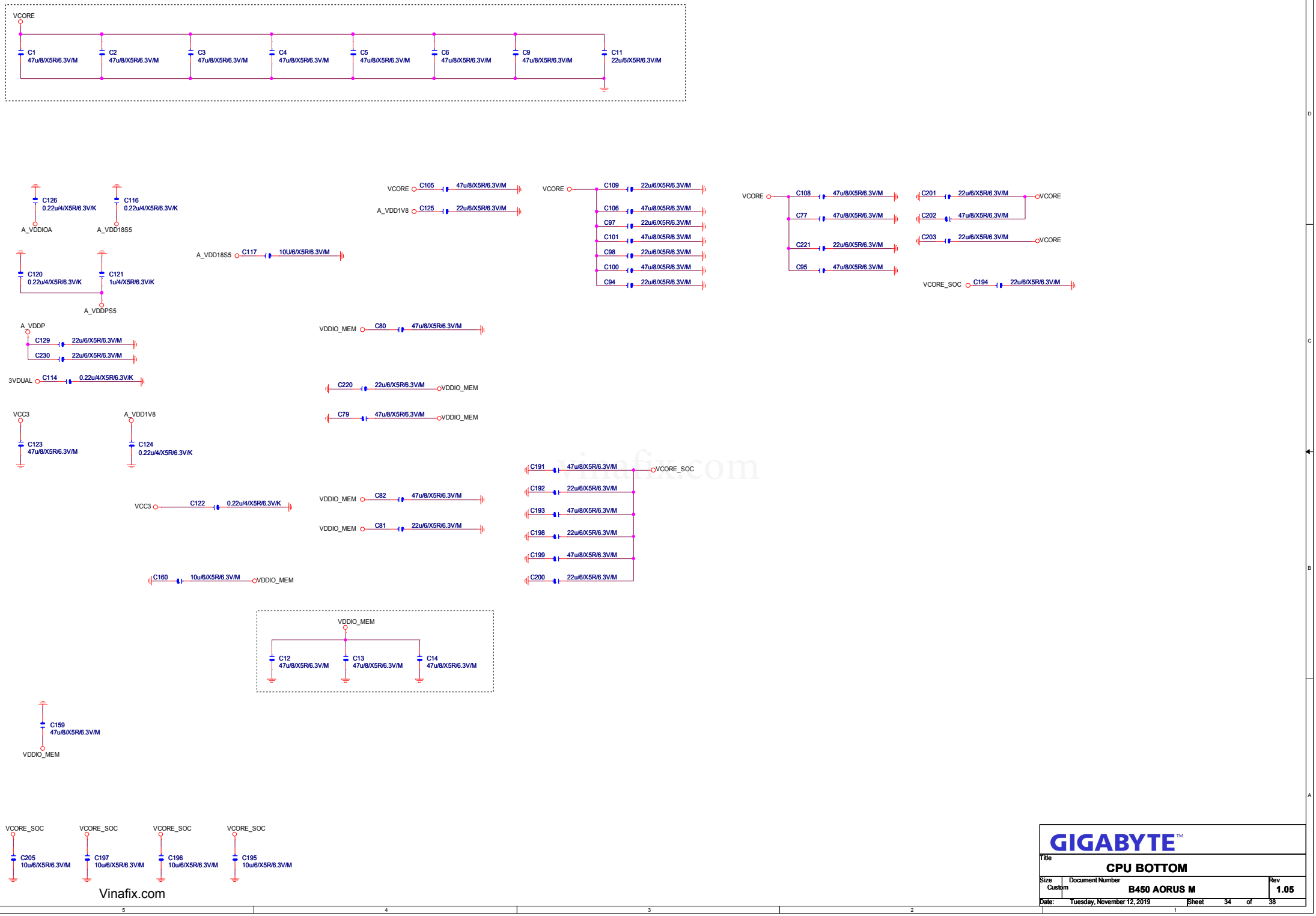
VCORE
C1 47u/8/X5R/6.3V/M
C2 47u/8/X5R/6.3V/M
C3 47u/8/X5R/6.3V/M
C4 47u/8/X5R/6.3V/M
C5 47u/8/X5R/6.3V/M
C6 47u/8/X5R/6.3V/M
C9 47u/8/X5R/6.3V/M
C11 22u/6/X5R/6.3V/M
C126 0.22u/4/X5R/6.3V/K
A_VDDIOA
C116 0.22u/4/X5R/6.3V/K
A_VDD18S5
C120 0.22u/4/X5R/6.3V/K
C121 1u/4/X5R/6.3V/K
A_VDDPS5
A_VDD18S5 C117 10U/6/X5R/6.3V/M
VCORE C105 47u/8/X5R/6.3V/M
A_VDD1V8 C125 22u/6/X5R/6.3V/M
VCORE C109 22u/6/X5R/6.3V/M
C106 47u/8/X5R/6.3V/M
C97 22u/6/X5R/6.3V/M
C101 47u/8/X5R/6.3V/M
C98 22u/6/X5R/6.3V/M
C100 47u/8/X5R/6.3V/M
C94 22u/6/X5R/6.3V/M
VCORE C108 47u/8/X5R/6.3V/M
C77 47u/8/X5R/6.3V/M
C221 22u/6/X5R/6.3V/M
C95 47u/8/X5R/6.3V/M
C201 22u/6/X5R/6.3V/M VCORE
C202 47u/8/X5R/6.3V/M
C203 22u/6/X5R/6.3V/M VCORE
VCORE_SOC C194 22u/6/X5R/6.3V/M
A_VDDP
C129 22u/6/X5R/6.3V/M
C230 22u/6/X5R/6.3V/M
3VDUAL C114 0.22u/4/X5R/6.3V/K
VDDIO_MEM C80 47u/8/X5R/6.3V/M
C220 22u/6/X5R/6.3V/M VDDIO_MEM
C79 47u/8/X5R/6.3V/M VDDIO_MEM
VCC3
C123 47u/8/X5R/6.3V/M
A_VDD1V8
C124 0.22u/4/X5R/6.3V/K
VCC3 C122 0.22u/4/X5R/6.3V/K
VDDIO_MEM C82 47u/8/X5R/6.3V/M
VDDIO_MEM C81 22u/6/X5R/6.3V/M
C160 10u/6/X5R/6.3V/M VDDIO_MEM
C191 47u/8/X5R/6.3V/M VCORE_SOC
C192 22u/6/X5R/6.3V/M
C193 47u/8/X5R/6.3V/M
C198 22u/6/X5R/6.3V/M
C199 47u/8/X5R/6.3V/M
C200 22u/6/X5R/6.3V/M
VDDIO_MEM
C12 47u/8/X5R/6.3V/M
C13 47u/8/X5R/6.3V/M
C14 47u/8/X5R/6.3V/M
C159 47u/8/X5R/6.3V/M
VDDIO_MEM
VCORE_SOC C205 10u/6/X5R/6.3V/M
VCORE_SOC C197 10u/6/X5R/6.3V/M
VCORE_SOC C196 10u/6/X5R/6.3V/M
VCORE_SOC C195 10u/6/X5R/6.3V/M
GIGABYTE
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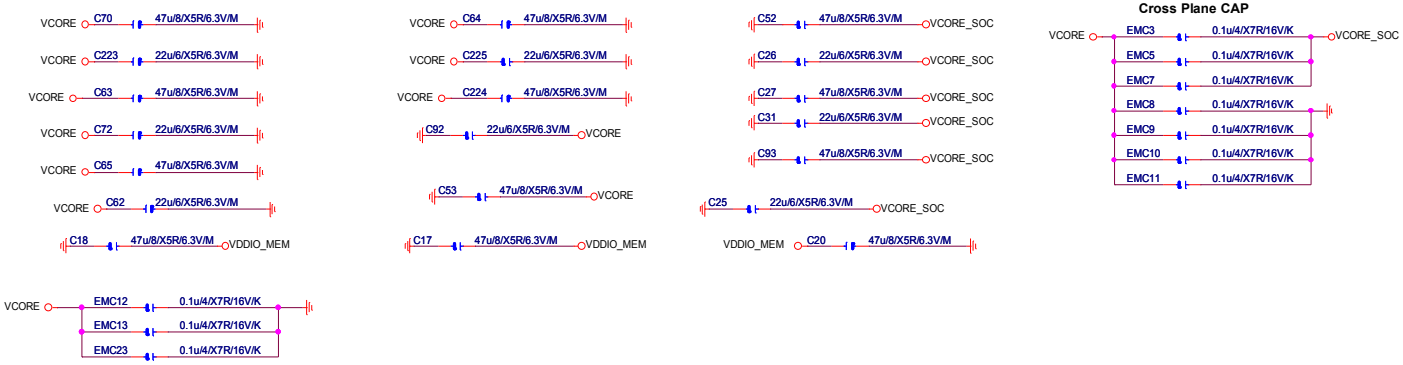
CPU TOP CAVITY



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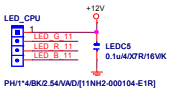
Rev 3.1

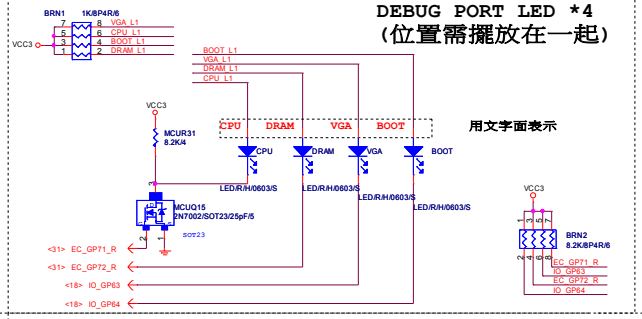
第一區 LED

FOR CPU 正發光 LED*4
(在CPU CHOKE之間,MOS_HS下方,不外露)

AMD CPU_FAN LED connector



DEBUG PORT LED *4
(位置需擺放在一起)



EC_GP71	CPU DEBUG
EC_GP72	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEVICE DEBUG
PM_GPIO6	software beat mode control
N_GPP_A22	
N_GPP_D12	

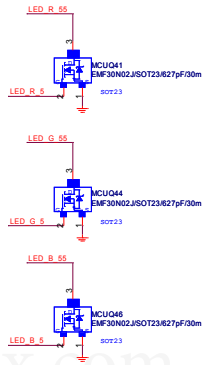
第二區 LED

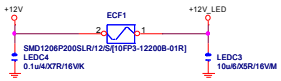
FOR DIMM 側發光 LED*12
(位置在DIMM兩側)

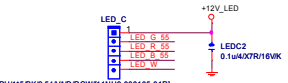
第五區 LED

燈條 LED (LED_C1放在PCB左邊板邊位置)

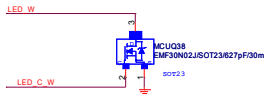
第五區 LED CONTROL



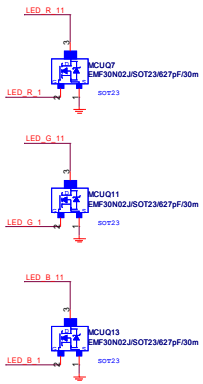


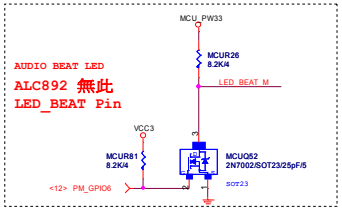


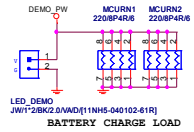
Footprint "PH1X5-ROW-L"

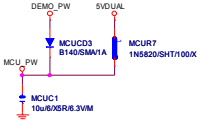


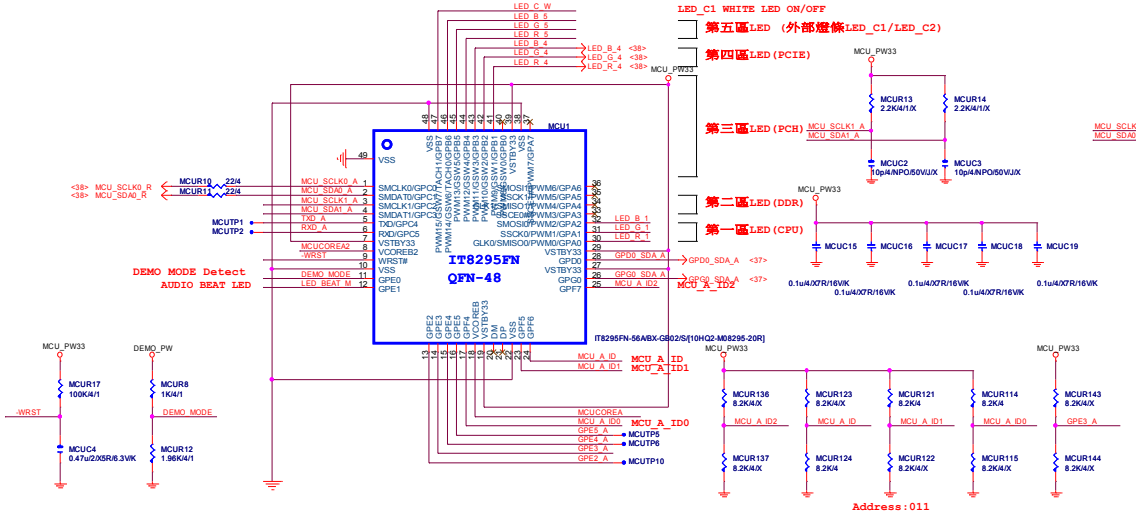
第一區 LED CONTROL











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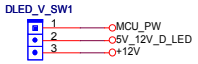
第六區 LED （靠近左上板邊位置）

DLED_V_SW1



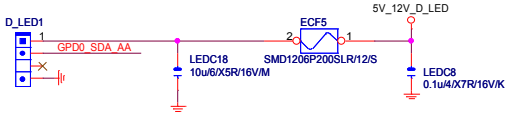
PH/1*3/BK/2.54/VA/D

DLED_V_SW1

DLED_V_SW1	
1-2	5V
2-3	12V

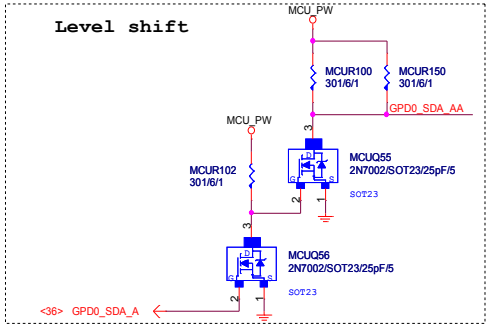
JP/1*2/BK/H/2.54/C/GF/[11NH1-000102-V1R]:[1-2]CLOSE

Digital LED Strip1



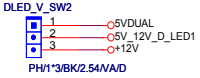
PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint "PH1X4-CUT3-LED-L"



第七區 LED （靠近右下DDR板邊位置）

DLED_V_SW2



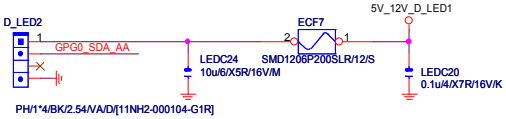
PH/1*3/BK/2.54/VA/D

DLED_V_SW2

DLED_V_SW2	
1-2	5V
2-3	12V

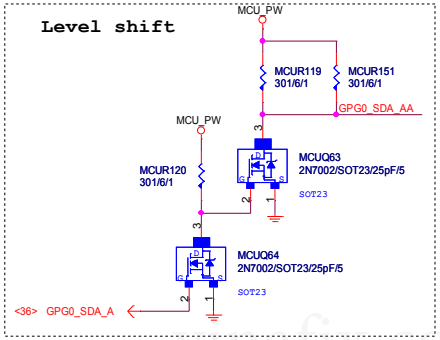
JP/1*2/BK/H/2.54/C/GF/[11NH1-000102-V1R]:[1-2]CLOSE

Digital LED Strip2



PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint "PH1X4-CUT3-LED-L"
(for pin-name 與 model-name 同方向)



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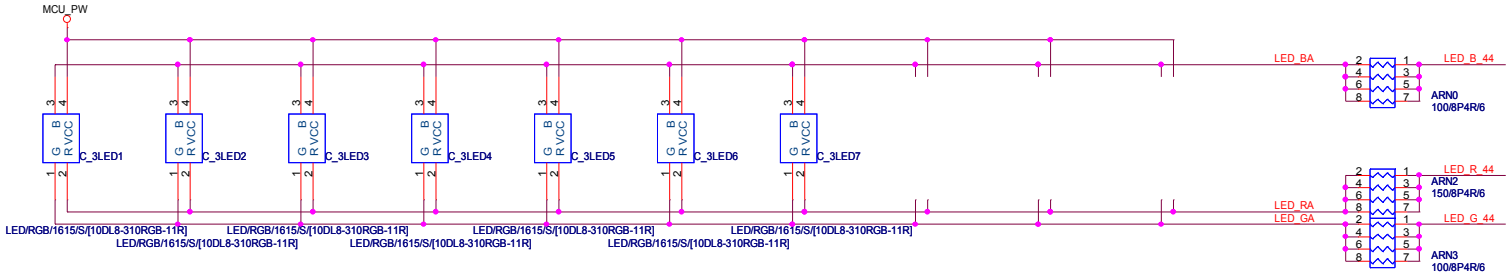
第三區 LED

第四區 LED

FOR AUDIO 正發光 LED*8 C_3LED1~8)

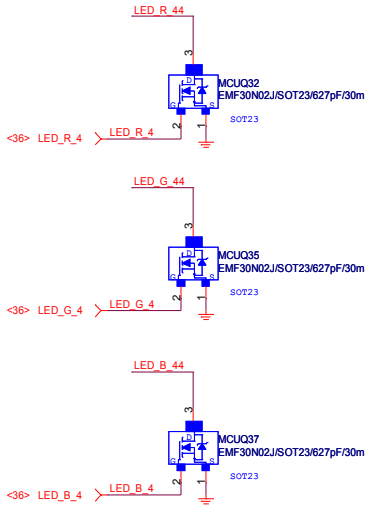


FOOTPRINT:LED-4P-RGB

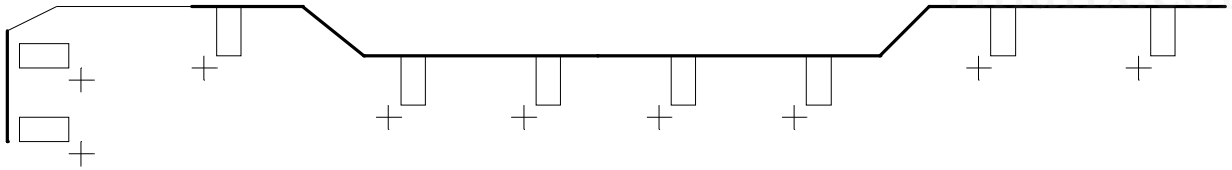
FOR PCIEX16_1 側發光 LED*4
(位置在PCIEX16_1 SLOT兩側各4顆)

FOR PCIEX8 側發光 LED*4
(位置在PCIEX8 SLOT兩側各4顆)

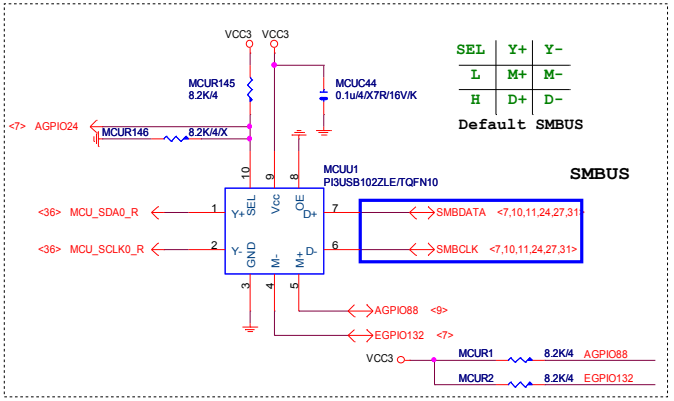
第四區 LED CONTROL



Audio Ground切割線+背面 RGB LED



For AMD MCU update



RGB LED LAYOUT 注意事項 :

1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下
   (整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU_PW & MCU_PW33電源一律走20mils
5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1 .....
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11,LED_W.....
   (包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils
   GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC

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