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MS-7A59

ATX

Ver: 2.1

Intel -Kabylake plamform Z270

CPU:

kabylake-S

System Chipset:

Z270

Onboard Chip:

HD Audio Codec:ALC1220
LAN:INTEL I219
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X8) Slot *1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*M2 * 3*

Other:

SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 *2*
*REAR USB2.0 *2*
REAR USB TYPE A+C

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MS-7A59

Size: Custom | Document Description: Cover Sheet | Rev: 2.1

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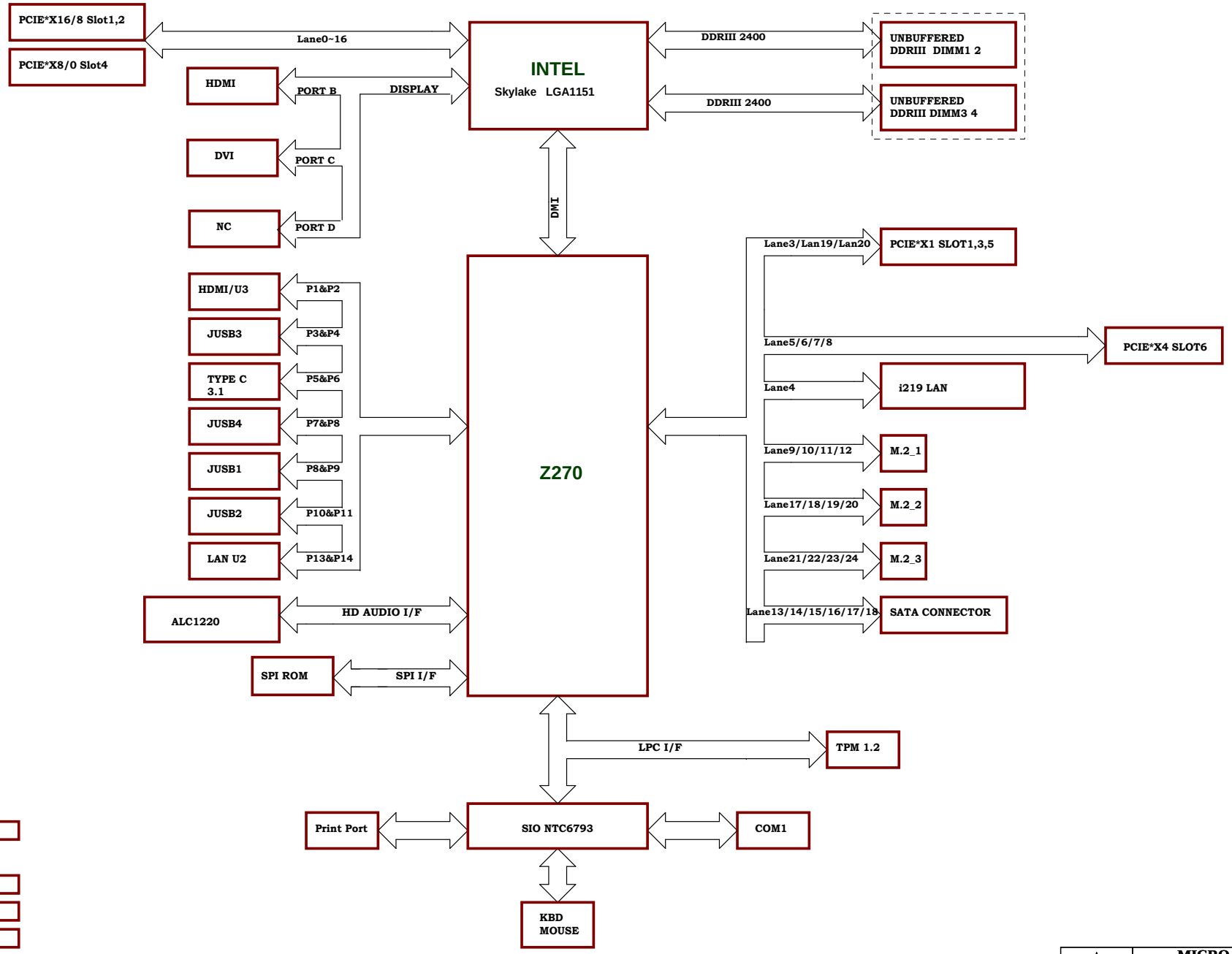
MS-7A59 Block Diagram



Slot Sequence:

- M.2
- PCIE X1
- PCIE X16
- PCIE X1 / M.2
- PCIE X8
- PCIE X1 / M.2
- PCIE X4

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Size	Document Description	Rev
Custom	Block Diagram	2.1

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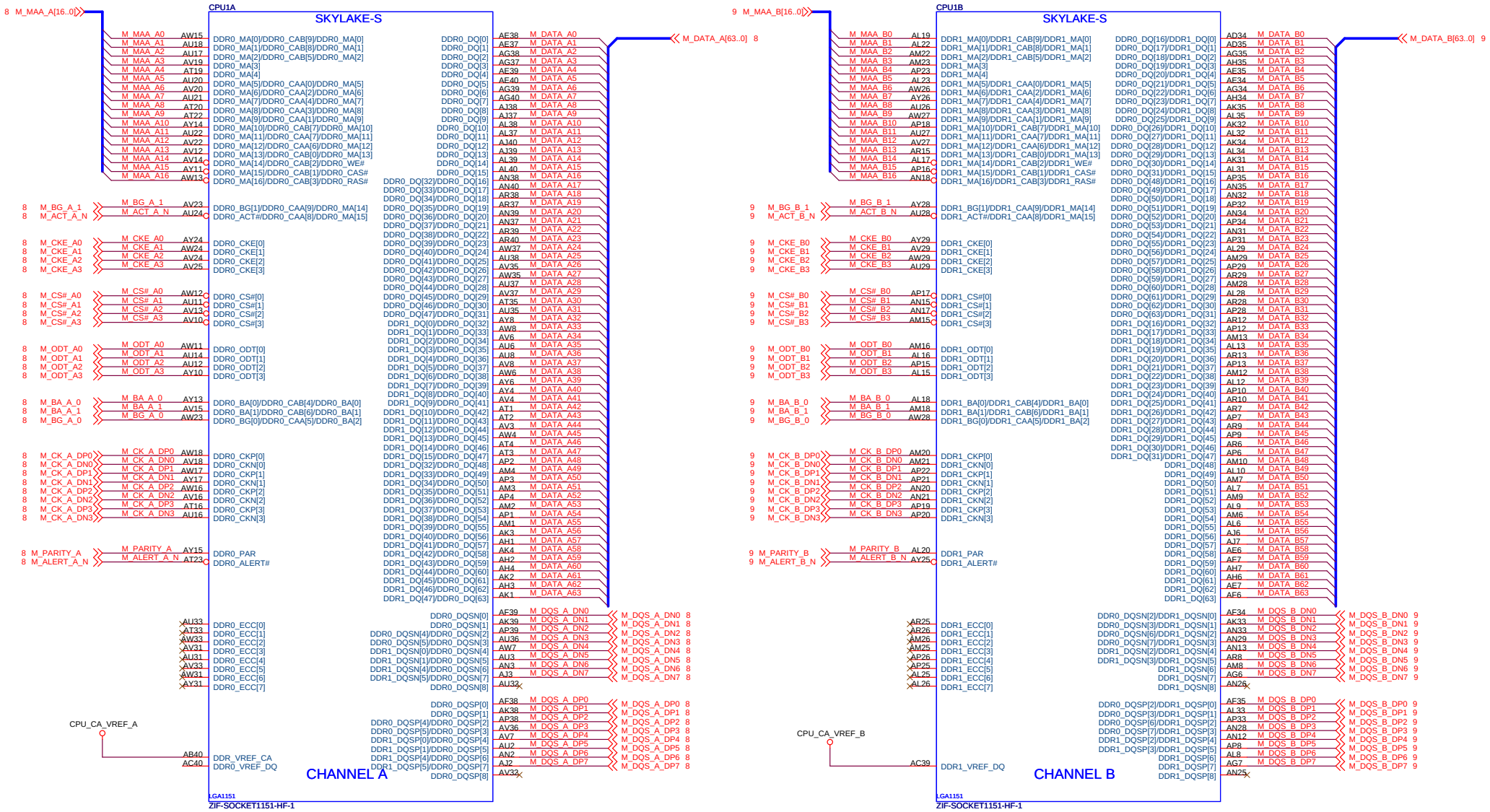
CPU1A
SKYLAKE-S
8 M_MAA_A[16..0]
M_MAA_A0 AW15
M_MAA_A1 AU18
M_MAA_A2 AU17
M_MAA_A3 AV19
M_MAA_A4 AT19
M_MAA_A5 AU20
M_MAA_A6 AV20
M_MAA_A7 AU21
M_MAA_A8 AT20
M_MAA_A9 AT22
M_MAA_A10 AY14
M_MAA_A11 AU22
M_MAA_A12 AV22
M_MAA_A13 AV12
M_MAA_A14 AV14
M_MAA_A15 AY11
M_MAA_A16 AW13
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]
DDR0_MA[3]
DDR0_MA[4]
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]
DDR0_MA[14]/DDR0_CAB[2]/DDR0_WE#
DDR0_MA[15]/DDR0_CAB[1]/DDR0_CAS#
DDR0_MA[16]/DDR0_CAB[3]/DDR0_RAS#
8 M_BG_A_1 AV23
8 M_ACT_A_N AU24
DDR0_BG[1]/DDR0_CAA[9]/DDR0_MA[14]
DDR0_ACT#/DDR0_CAA[8]/DDR0_MA[15]
8 M_CKE_A0 AY24
8 M_CKE_A1 AW24
8 M_CKE_A2 AV24
8 M_CKE_A3 AV25
DDR0_CKE[0]
DDR0_CKE[1]
DDR0_CKE[2]
DDR0_CKE[3]
8 M_CS#_A0 AW12
8 M_CS#_A1 AU11
8 M_CS#_A2 AV13
8 M_CS#_A3 AV10
DDR0_CS#[0]
DDR0_CS#[1]
DDR0_CS#[2]
DDR0_CS#[3]
8 M_ODT_A0 AW11
8 M_ODT_A1 AU14
8 M_ODT_A2 AU12
8 M_ODT_A3 AY10
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
8 M_BA_A_0 AY13
8 M_BA_A_1 AV15
8 M_BG_A_0 AW23
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]
DDR0_BG[0]/DDR0_CAA[5]/DDR0_BA[2]
8 M_CK_A_DP0 AW18
8 M_CK_A_DN0 AV18
8 M_CK_A_DP1 AW17
8 M_CK_A_DN1 AY17
8 M_CK_A_DP2 AW16
8 M_CK_A_DN2 AV16
8 M_CK_A_DP3 AT16
8 M_CK_A_DN3 AU16
DDR0_CKP[0]
DDR0_CKN[0]
DDR0_CKP[1]
DDR0_CKN[1]
DDR0_CKP[2]
DDR0_CKN[2]
DDR0_CKP[3]
DDR0_CKN[3]
8 M_PARITY_A AY15
8 M_ALERT_A_N AT23
DDR0_PAR
DDR0_ALERT#
AU33 DDR0_ECC[0]
AT33 DDR0_ECC[1]
AW33 DDR0_ECC[2]
AV31 DDR0_ECC[3]
AU31 DDR0_ECC[4]
AV33 DDR0_ECC[5]
AW31 DDR0_ECC[6]
AY31 DDR0_ECC[7]
CPU_CA_VREF_A
AB40 DDR_VREF_CA
AC40 DDR0_VREF_DQ
DDR0_DQ[0] AE38 M_DATA_A0
DDR0_DQ[1] AE37 M_DATA_A1
DDR0_DQ[2] AG38 M_DATA_A2
DDR0_DQ[3] AG37 M_DATA_A3
DDR0_DQ[4] AE39 M_DATA_A4
DDR0_DQ[5] AE40 M_DATA_A5
DDR0_DQ[6] AG39 M_DATA_A6
DDR0_DQ[7] AG40 M_DATA_A7
DDR0_DQ[8] AJ38 M_DATA_A8
DDR0_DQ[9] AJ37 M_DATA_A9
DDR0_DQ[10] AL38 M_DATA_A10
DDR0_DQ[11] AL37 M_DATA_A11
DDR0_DQ[12] AJ40 M_DATA_A12
DDR0_DQ[13] AJ39 M_DATA_A13
DDR0_DQ[14] AL39 M_DATA_A14
DDR0_DQ[15] AL40 M_DATA_A15
DDR0_DQ[32]/DDR0_DQ[16] AN38 M_DATA_A16
DDR0_DQ[33]/DDR0_DQ[17] AN40 M_DATA_A17
DDR0_DQ[34]/DDR0_DQ[18] AR38 M_DATA_A18
DDR0_DQ[35]/DDR0_DQ[19] AR37 M_DATA_A19
DDR0_DQ[36]/DDR0_DQ[20] AN39 M_DATA_A20
DDR0_DQ[37]/DDR0_DQ[21] AN37 M_DATA_A21
DDR0_DQ[38]/DDR0_DQ[22] AR39 M_DATA_A22
DDR0_DQ[39]/DDR0_DQ[23] AR40 M_DATA_A23
DDR0_DQ[40]/DDR0_DQ[24] AW37 M_DATA_A24
DDR0_DQ[41]/DDR0_DQ[25] AU38 M_DATA_A25
DDR0_DQ[42]/DDR0_DQ[26] AV35 M_DATA_A26
DDR0_DQ[43]/DDR0_DQ[27] AW35 M_DATA_A27
DDR0_DQ[44]/DDR0_DQ[28] AU37 M_DATA_A28
DDR0_DQ[45]/DDR0_DQ[29] AV37 M_DATA_A29
DDR0_DQ[46]/DDR0_DQ[30] AT35 M_DATA_A30
DDR0_DQ[47]/DDR0_DQ[31] AU35 M_DATA_A31
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DDR1_DQ[1]/DDR0_DQ[33] AW8 M_DATA_A33
DDR1_DQ[2]/DDR0_DQ[34] AV6 M_DATA_A34
DDR1_DQ[3]/DDR0_DQ[35] AU6 M_DATA_A35
DDR1_DQ[4]/DDR0_DQ[36] AU8 M_DATA_A36
DDR1_DQ[5]/DDR0_DQ[37] AV8 M_DATA_A37
DDR1_DQ[6]/DDR0_DQ[38] AW6 M_DATA_A38
DDR1_DQ[7]/DDR0_DQ[39] AY6 M_DATA_A39
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DDR1_DQ[9]/DDR0_DQ[41] AV4 M_DATA_A41
DDR1_DQ[10]/DDR0_DQ[42] AT1 M_DATA_A42
DDR1_DQ[11]/DDR0_DQ[43] AT2 M_DATA_A43
DDR1_DQ[12]/DDR0_DQ[44] AV3 M_DATA_A44
DDR1_DQ[13]/DDR0_DQ[45] AW4 M_DATA_A45
DDR1_DQ[14]/DDR0_DQ[46] AT4 M_DATA_A46
DDR1_DQ[15]/DDR0_DQ[47] AT3 M_DATA_A47
DDR1_DQ[32]/DDR0_DQ[48] AP2 M_DATA_A48
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DDR1_DQ[34]/DDR0_DQ[50] AP3 M_DATA_A50
DDR1_DQ[35]/DDR0_DQ[51] AM3 M_DATA_A51
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DDR1_DQ[37]/DDR0_DQ[53] AM2 M_DATA_A53
DDR1_DQ[38]/DDR0_DQ[54] AP1 M_DATA_A54
DDR1_DQ[39]/DDR0_DQ[55] AM1 M_DATA_A55
DDR1_DQ[40]/DDR0_DQ[56] AK3 M_DATA_A56
DDR1_DQ[41]/DDR0_DQ[57] AH1 M_DATA_A57
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DDR1_DQ[43]/DDR0_DQ[59] AH2 M_DATA_A59
DDR1_DQ[44]/DDR0_DQ[60] AH4 M_DATA_A60
DDR1_DQ[45]/DDR0_DQ[61] AK2 M_DATA_A61
DDR1_DQ[46]/DDR0_DQ[62] AH3 M_DATA_A62
DDR1_DQ[47]/DDR0_DQ[63] AK1 M_DATA_A63
M_DATA_A[63..0] 8
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DDR0_DQSN[4]/DDR0_DQSN[2] AP39 M_DQS_A_DN2
DDR0_DQSN[5]/DDR0_DQSN[3] AU36 M_DQS_A_DN3
DDR1_DQSN[0]/DDR0_DQSN[4] AW7 M_DQS_A_DN4
DDR1_DQSN[1]/DDR0_DQSN[5] AU3 M_DQS_A_DN5
DDR1_DQSN[4]/DDR0_DQSN[6] AN3 M_DQS_A_DN6
DDR1_DQSN[5]/DDR0_DQSN[7] AJ3 M_DQS_A_DN7
DDR0_DQSN[8] AU32
M_DQS_A_DN[0..7] 8
DDR0_DQSP[0] AF38 M_DQS_A_DP0
DDR0_DQSP[1] AK38 M_DQS_A_DP1
DDR0_DQSP[4]/DDR0_DQSP[2] AP38 M_DQS_A_DP2
DDR0_DQSP[5]/DDR0_DQSP[3] AV36 M_DQS_A_DP3
DDR1_DQSP[0]/DDR0_DQSP[4] AV7 M_DQS_A_DP4
DDR1_DQSP[1]/DDR0_DQSP[5] AU2 M_DQS_A_DP5
DDR1_DQSP[4]/DDR0_DQSP[6] AN2 M_DQS_A_DP6
DDR1_DQSP[5]/DDR0_DQSP[7] AJ2 M_DQS_A_DP7
DDR0_DQSP[8] AV32
M_DQS_A_DP[0..7] 8
CHANNEL A
LGA1151
ZIF-SOCKET1151-HF-1
CPU1B
SKYLAKE-S
9 M_MAA_B[16..0]
M_MAA_B0 AL19
M_MAA_B1 AL22
M_MAA_B2 AM22
M_MAA_B3 AM23
M_MAA_B4 AP23
M_MAA_B5 AL23
M_MAA_B6 AW26
M_MAA_B7 AY26
M_MAA_B8 AU26
M_MAA_B9 AW27
M_MAA_B10 AP18
M_MAA_B11 AU27
M_MAA_B12 AV27
M_MAA_B13 AR15
M_MAA_B14 AL17
M_MAA_B15 AP16
M_MAA_B16 AN18
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_MA[3]
DDR1_MA[4]
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAB[2]/DDR1_WE#
DDR1_MA[15]/DDR1_CAB[1]/DDR1_CAS#
DDR1_MA[16]/DDR1_CAB[3]/DDR1_RAS#
9 M_BG_B_1 AY28
9 M_ACT_B_N AU28
DDR1_BG[1]/DDR1_CAA[9]/DDR1_MA[14]
DDR1_ACT#/DDR1_CAA[8]/DDR1_MA[15]
9 M_CKE_B0 AY29
9 M_CKE_B1 AV29
9 M_CKE_B2 AW29
9 M_CKE_B3 AU29
DDR1_CKE[0]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]
9 M_CS#_B0 AP17
9 M_CS#_B1 AN15
9 M_CS#_B2 AN17
9 M_CS#_B3 AM15
DDR1_CS#[0]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]
9 M_ODT_B0 AM16
9 M_ODT_B1 AL16
9 M_ODT_B2 AP15
9 M_ODT_B3 AL15
DDR1_ODT[0]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]
9 M_BA_B_0 AL18
9 M_BA_B_1 AM18
9 M_BG_B_0 AW28
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_BG[0]/DDR1_CAA[5]/DDR1_BA[2]
9 M_CK_B_DP0 AM20
9 M_CK_B_DN0 AM21
9 M_CK_B_DP1 AP22
9 M_CK_B_DN1 AP21
9 M_CK_B_DP2 AN20
9 M_CK_B_DN2 AN21
9 M_CK_B_DP3 AP19
9 M_CK_B_DN3 AP20
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DDR1_CKN[0]
DDR1_CKP[1]
DDR1_CKN[1]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]
9 M_PARITY_B AL20
9 M_ALERT_B_N AY25
DDR1_PAR
DDR1_ALERT#
AR25 DDR1_ECC[0]
AR26 DDR1_ECC[1]
AM26 DDR1_ECC[2]
AM25 DDR1_ECC[3]
AP26 DDR1_ECC[4]
AP25 DDR1_ECC[5]
AL25 DDR1_ECC[6]
AL26 DDR1_ECC[7]
CPU_CA_VREF_B
AC39 DDR1_VREF_DQ
DDR0_DQ[16]/DDR1_DQ[0] AD34 M_DATA_B0
DDR0_DQ[17]/DDR1_DQ[1] AD35 M_DATA_B1
DDR0_DQ[18]/DDR1_DQ[2] AG35 M_DATA_B2
DDR0_DQ[19]/DDR1_DQ[3] AH35 M_DATA_B3
DDR0_DQ[20]/DDR1_DQ[4] AE35 M_DATA_B4
DDR0_DQ[21]/DDR1_DQ[5] AE34 M_DATA_B5
DDR0_DQ[22]/DDR1_DQ[6] AG34 M_DATA_B6
DDR0_DQ[23]/DDR1_DQ[7] AH34 M_DATA_B7
DDR0_DQ[24]/DDR1_DQ[8] AK35 M_DATA_B8
DDR0_DQ[25]/DDR1_DQ[9] AL35 M_DATA_B9
DDR0_DQ[26]/DDR1_DQ[10] AK32 M_DATA_B10
DDR0_DQ[27]/DDR1_DQ[11] AL32 M_DATA_B11
DDR0_DQ[28]/DDR1_DQ[12] AK34 M_DATA_B12
DDR0_DQ[29]/DDR1_DQ[13] AL34 M_DATA_B13
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DDR0_DQ[31]/DDR1_DQ[15] AL31 M_DATA_B15
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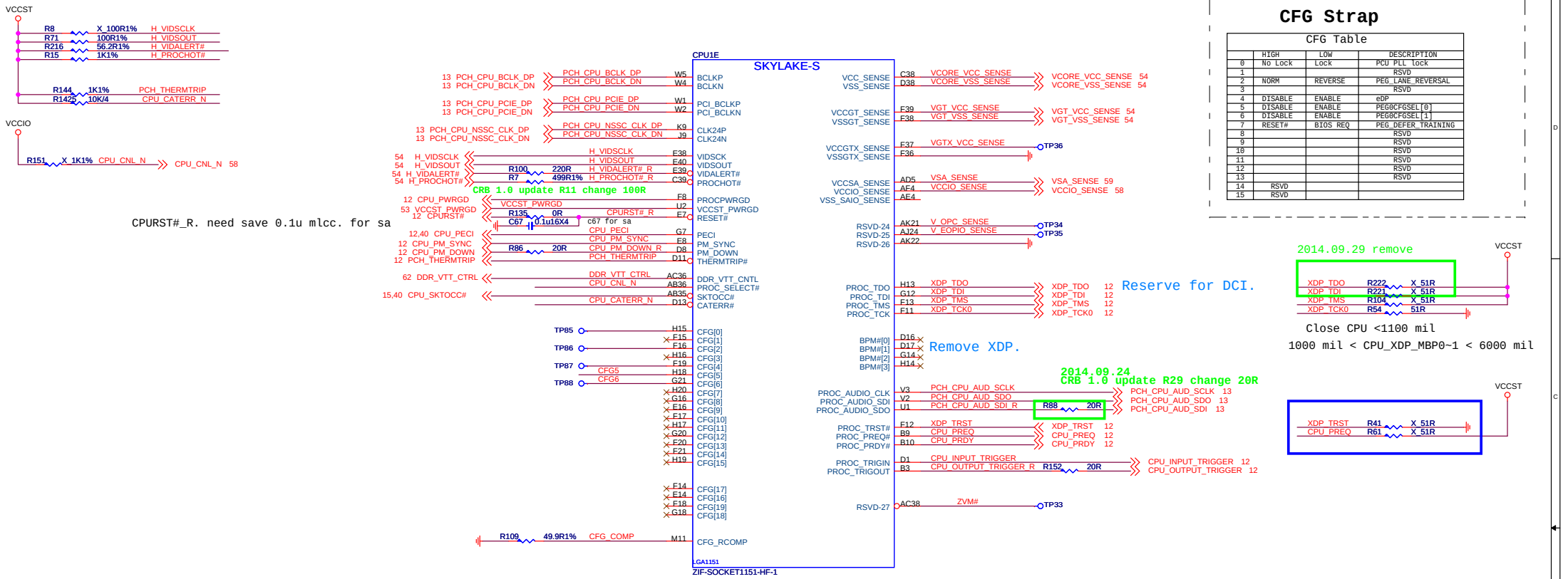
DDR0_DQ[49]/DDR1_DQ[17] AN35 M_DATA_B17
DDR0_DQ[50]/DDR1_DQ[18] AN32 M_DATA_B18
DDR0_DQ[51]/DDR1_DQ[19] AP32 M_DATA_B19
DDR0_DQ[52]/DDR1_DQ[20] AN34 M_DATA_B20
DDR0_DQ[53]/DDR1_DQ[21] AP34 M_DATA_B21
DDR0_DQ[54]/DDR1_DQ[22] AN31 M_DATA_B22
DDR0_DQ[55]/DDR1_DQ[23] AP31 M_DATA_B23
DDR0_DQ[56]/DDR1_DQ[24] AL29 M_DATA_B24
DDR0_DQ[57]/DDR1_DQ[25] AM29 M_DATA_B25
DDR0_DQ[58]/DDR1_DQ[26] AP29 M_DATA_B26
DDR0_DQ[59]/DDR1_DQ[27] AR29 M_DATA_B27
DDR0_DQ[60]/DDR1_DQ[28] AM28 M_DATA_B28
DDR0_DQ[61]/DDR1_DQ[29] AL28 M_DATA_B29
DDR0_DQ[62]/DDR1_DQ[30] AR28 M_DATA_B30
DDR0_DQ[63]/DDR1_DQ[31] AP28 M_DATA_B31
DDR1_DQ[16]/DDR1_DQ[32] AR12 M_DATA_B32
DDR1_DQ[17]/DDR1_DQ[33] AP12 M_DATA_B33
DDR1_DQ[18]/DDR1_DQ[34] AM13 M_DATA_B34
DDR1_DQ[19]/DDR1_DQ[35] AL13 M_DATA_B35
DDR1_DQ[20]/DDR1_DQ[36] AR13 M_DATA_B36
DDR1_DQ[21]/DDR1_DQ[37] AP13 M_DATA_B37
DDR1_DQ[22]/DDR1_DQ[38] AM12 M_DATA_B38
DDR1_DQ[23]/DDR1_DQ[39] AL12 M_DATA_B39
DDR1_DQ[24]/DDR1_DQ[40] AP10 M_DATA_B40
DDR1_DQ[25]/DDR1_DQ[41] AR10 M_DATA_B41
DDR1_DQ[26]/DDR1_DQ[42] AR7 M_DATA_B42
DDR1_DQ[27]/DDR1_DQ[43] AP7 M_DATA_B43
DDR1_DQ[28]/DDR1_DQ[44] AR9 M_DATA_B44
DDR1_DQ[29]/DDR1_DQ[45] AP9 M_DATA_B45
DDR1_DQ[30]/DDR1_DQ[46] AR6 M_DATA_B46
DDR1_DQ[31]/DDR1_DQ[47] AP6 M_DATA_B47
DDR1_DQ[48] AM10 M_DATA_B48
DDR1_DQ[49] AL10 M_DATA_B49
DDR1_DQ[50] AM7 M_DATA_B50
DDR1_DQ[51] AL7 M_DATA_B51
DDR1_DQ[52] AM9 M_DATA_B52
DDR1_DQ[53] AL9 M_DATA_B53
DDR1_DQ[54] AM6 M_DATA_B54
DDR1_DQ[55] AL6 M_DATA_B55
DDR1_DQ[56] AJ6 M_DATA_B56
DDR1_DQ[57] AJ7 M_DATA_B57
DDR1_DQ[58] AE6 M_DATA_B58
DDR1_DQ[59] AE7 M_DATA_B59
DDR1_DQ[60] AH7 M_DATA_B60
DDR1_DQ[61] AH6 M_DATA_B61
DDR1_DQ[62] AE7 M_DATA_B62
DDR1_DQ[63] AF6 M_DATA_B63
M_DATA_B[63..0] 9
DDR0_DQSN[2]/DDR1_DQSN[0] AF34 M_DQS_B_DN0
DDR0_DQSN[3]/DDR1_DQSN[1] AK33 M_DQS_B_DN1
DDR0_DQSN[6]/DDR1_DQSN[2] AN33 M_DQS_B_DN2
DDR0_DQSN[7]/DDR1_DQSN[3] AN29 M_DQS_B_DN3
DDR1_DQSN[2]/DDR1_DQSN[4] AN13 M_DQS_B_DN4
DDR1_DQSN[3]/DDR1_DQSN[5] AR8 M_DQS_B_DN5
DDR1_DQSN[6] AM8 M_DQS_B_DN6
DDR1_DQSN[7] AG6 M_DQS_B_DN7
DDR1_DQSN[8] AN26
M_DQS_B_DN[0..7] 9
DDR0_DQSP[2]/DDR1_DQSP[0] AF35 M_DQS_B_DP0
DDR0_DQSP[3]/DDR1_DQSP[1] AL33 M_DQS_B_DP1
DDR0_DQSP[6]/DDR1_DQSP[2] AP33 M_DQS_B_DP2
DDR0_DQSP[7]/DDR1_DQSP[3] AN28 M_DQS_B_DP3
DDR1_DQSP[2]/DDR1_DQSP[4] AN12 M_DQS_B_DP4
DDR1_DQSP[3]/DDR1_DQSP[5] AP8 M_DQS_B_DP5
DDR1_DQSP[6] AL8 M_DQS_B_DP6
DDR1_DQSP[7] AG7 M_DQS_B_DP7
DDR1_DQSP[8] AN25
M_DQS_B_DP[0..7] 9
CHANNEL B
LGA1151
ZIF-SOCKET1151-HF-1
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size Custom
Document Description CPU-Memory
Rev 2.1
Date: Wednesday, November 09, 2016
Sheet 3 of 70



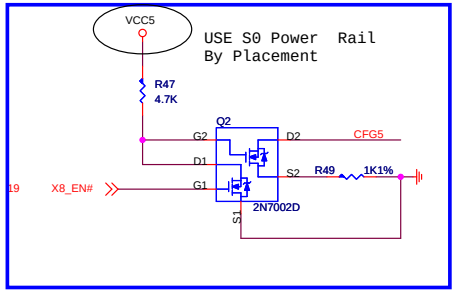
CFG Strap

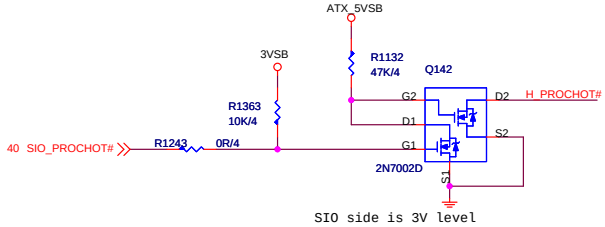
CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

X8 Ctrl

ENABLE# X8	SLOT1	SLOT4
0	X8	X8
1	X16	X0





CFG Strap

CFG Table

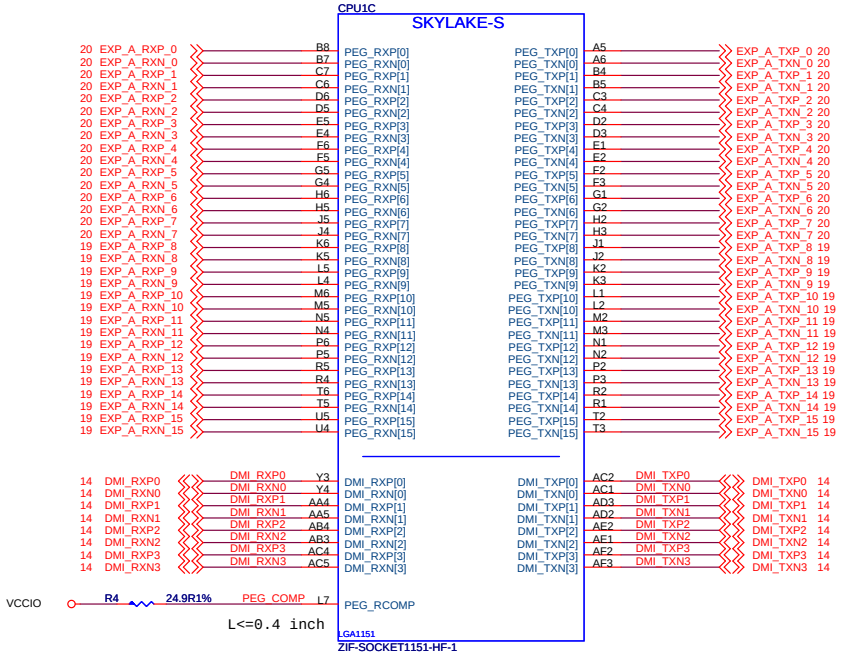
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

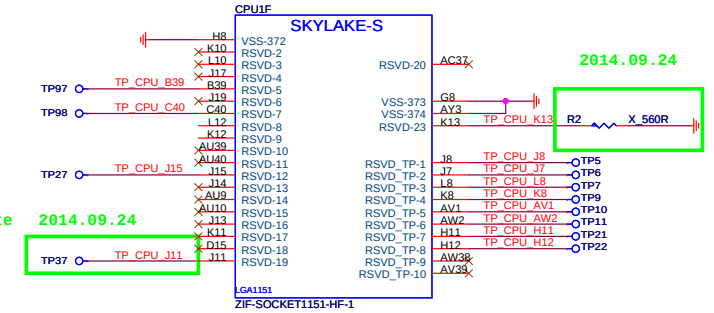
MICRO-STAR INT'L CO.,LTD

MS-7A59

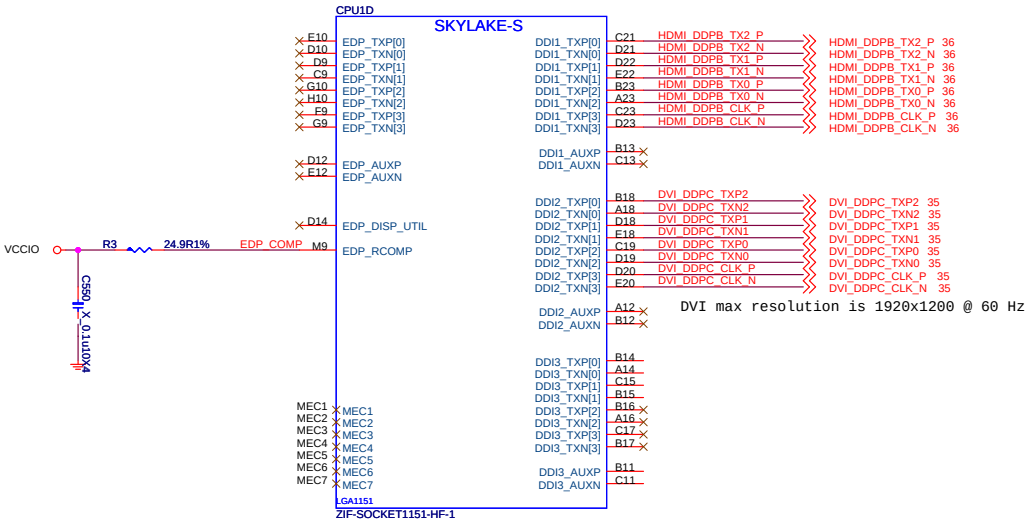
Size: Custom | Document Description: CPU-Control/MISC/CFG/Audio | Rev: 2.1

Date: Wednesday, November 09, 2016 | Sheet 4 of 70

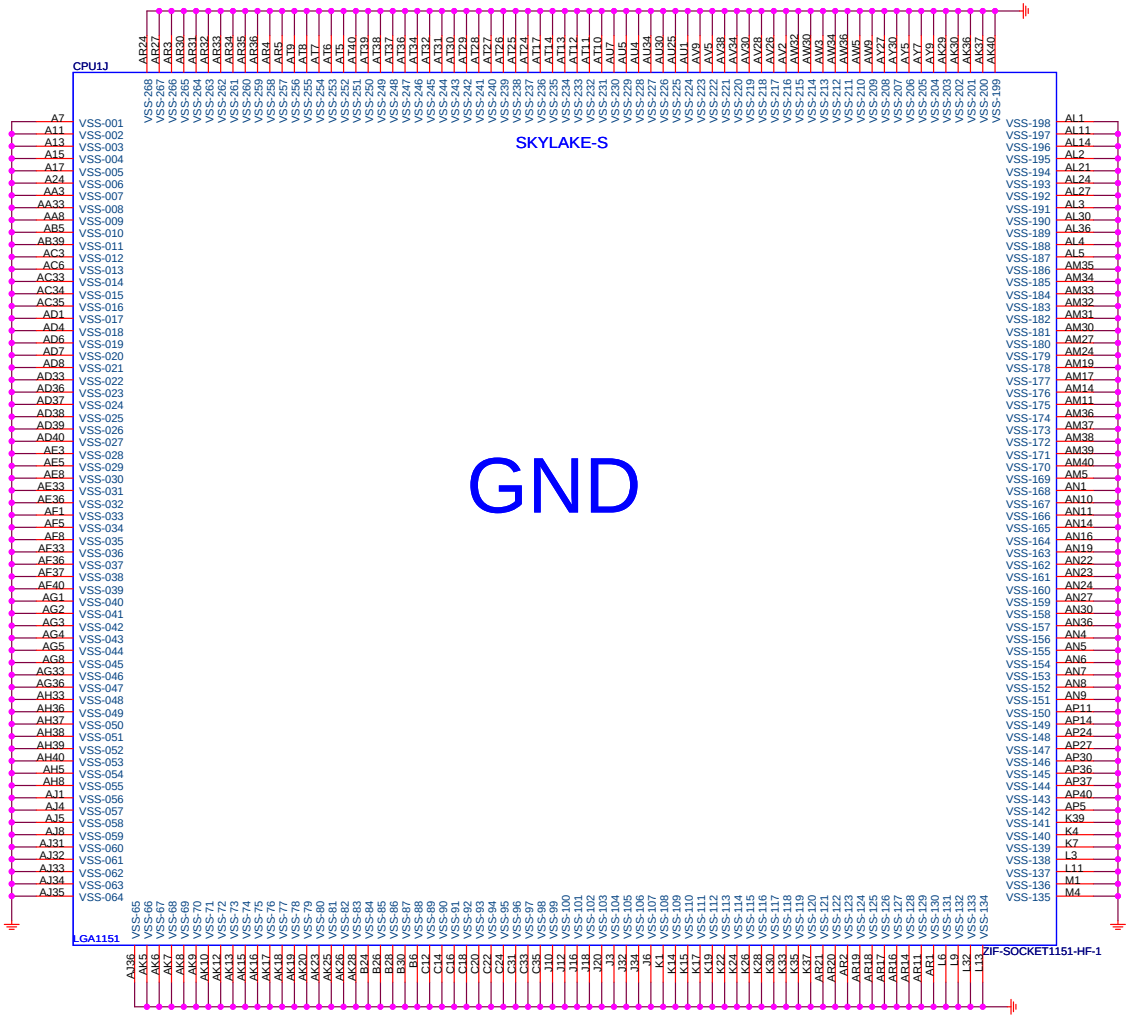


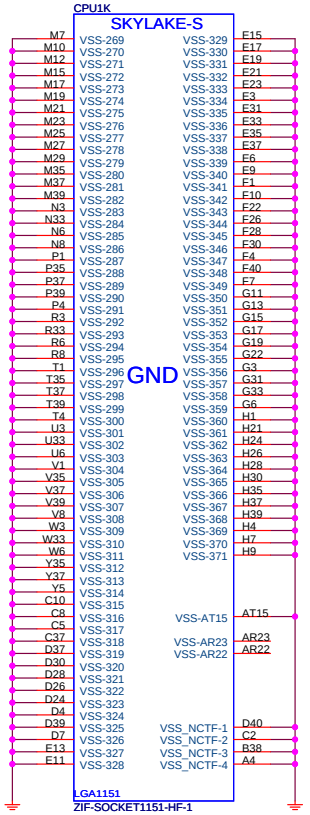


Vinafix.com

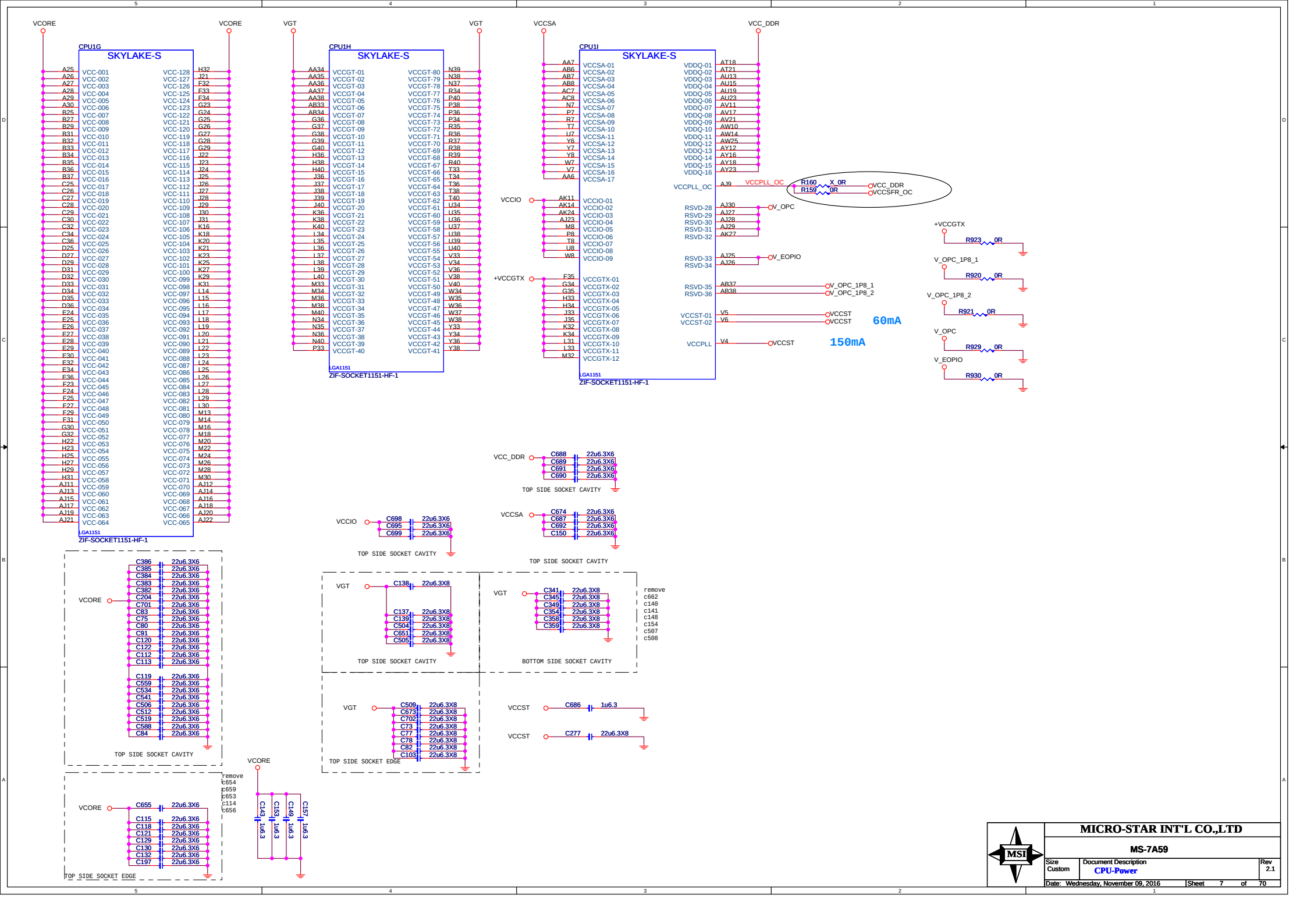


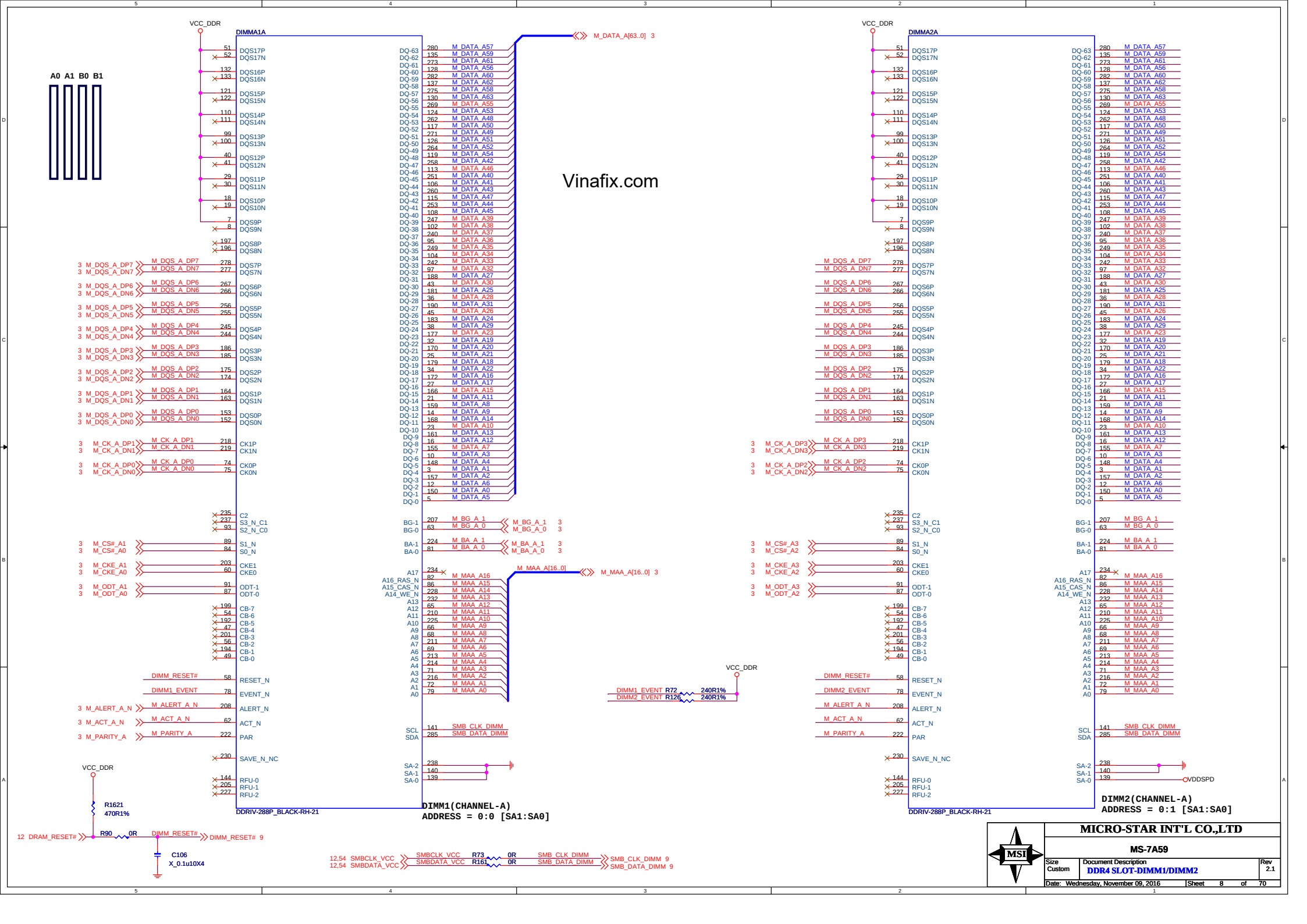
MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: CPU-PEG/Display
Rev: 2.1	
Date: Wednesday, November 09, 2016	Sheet 5 of 70





MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: CPU-GND
Rev: 2.1	
Date: Wednesday, November 09, 2016	Sheet 6 of 70


VCORE
CPU1G
SKYLAKE-S
VCC-001 VCC-002 VCC-003 VCC-004 VCC-005 VCC-006 VCC-007 VCC-008 VCC-009 VCC-010 VCC-011 VCC-012 VCC-013 VCC-014 VCC-015 VCC-016 VCC-017 VCC-018 VCC-019 VCC-020 VCC-021 VCC-022 VCC-023 VCC-024 VCC-025 VCC-026 VCC-027 VCC-028 VCC-029 VCC-030 VCC-031 VCC-032 VCC-033 VCC-034 VCC-035 VCC-036 VCC-037 VCC-038 VCC-039 VCC-040 VCC-041 VCC-042 VCC-043 VCC-044 VCC-045 VCC-046 VCC-047 VCC-048 VCC-049 VCC-050 VCC-051 VCC-052 VCC-053 VCC-054 VCC-055 VCC-056 VCC-057 VCC-058 VCC-059 VCC-060 VCC-061 VCC-062 VCC-063 VCC-064
VCC-065 VCC-066 VCC-067 VCC-068 VCC-069 VCC-070 VCC-071 VCC-072 VCC-073 VCC-074 VCC-075 VCC-076 VCC-077 VCC-078 VCC-079 VCC-080 VCC-081 VCC-082 VCC-083 VCC-084 VCC-085 VCC-086 VCC-087 VCC-088 VCC-089 VCC-090 VCC-091 VCC-092 VCC-093 VCC-094 VCC-095 VCC-096 VCC-097 VCC-098 VCC-099 VCC-100 VCC-101 VCC-102 VCC-103 VCC-104 VCC-105 VCC-106 VCC-107 VCC-108 VCC-109 VCC-110 VCC-111 VCC-112 VCC-113 VCC-114 VCC-115 VCC-116 VCC-117 VCC-118 VCC-119 VCC-120 VCC-121 VCC-122 VCC-123 VCC-124 VCC-125 VCC-126 VCC-127 VCC-128
LGA1151
ZIF-SOCKET1151-HF-1
VGT
CPU1H
SKYLAKE-S
VCCGT-01 VCCGT-02 VCCGT-03 VCCGT-04 VCCGT-05 VCCGT-06 VCCGT-07 VCCGT-08 VCCGT-09 VCCGT-10 VCCGT-11 VCCGT-12 VCCGT-13 VCCGT-14 VCCGT-15 VCCGT-16 VCCGT-17 VCCGT-18 VCCGT-19 VCCGT-20 VCCGT-21 VCCGT-22 VCCGT-23 VCCGT-24 VCCGT-25 VCCGT-26 VCCGT-27 VCCGT-28 VCCGT-29 VCCGT-30 VCCGT-31 VCCGT-32 VCCGT-33 VCCGT-34 VCCGT-35 VCCGT-36 VCCGT-37 VCCGT-38 VCCGT-39 VCCGT-40
VCCGT-41 VCCGT-42 VCCGT-43 VCCGT-44 VCCGT-45 VCCGT-46 VCCGT-47 VCCGT-48 VCCGT-49 VCCGT-50 VCCGT-51 VCCGT-52 VCCGT-53 VCCGT-54 VCCGT-55 VCCGT-56 VCCGT-57 VCCGT-58 VCCGT-59 VCCGT-60 VCCGT-61 VCCGT-62 VCCGT-63 VCCGT-64 VCCGT-65 VCCGT-66 VCCGT-67 VCCGT-68 VCCGT-69 VCCGT-70 VCCGT-71 VCCGT-72 VCCGT-73 VCCGT-74 VCCGT-75 VCCGT-76 VCCGT-77 VCCGT-78 VCCGT-79 VCCGT-80
LGA1151
ZIF-SOCKET1151-HF-1
VCCSA
VCC_DDR
CPU1I
SKYLAKE-S
VCCSA-01 VCCSA-02 VCCSA-03 VCCSA-04 VCCSA-05 VCCSA-06 VCCSA-07 VCCSA-08 VCCSA-09 VCCSA-10 VCCSA-11 VCCSA-12 VCCSA-13 VCCSA-14 VCCSA-15 VCCSA-16 VCCSA-17
VDDQ-01 VDDQ-02 VDDQ-03 VDDQ-04 VDDQ-05 VDDQ-06 VDDQ-07 VDDQ-08 VDDQ-09 VDDQ-10 VDDQ-11 VDDQ-12 VDDQ-13 VDDQ-14 VDDQ-15 VDDQ-16
VCCPLL_OC
VCCIO-01 VCCIO-02 VCCIO-03 VCCIO-04 VCCIO-05 VCCIO-06 VCCIO-07 VCCIO-08 VCCIO-09
VCCGTX-01 VCCGTX-02 VCCGTX-03 VCCGTX-04 VCCGTX-05 VCCGTX-06 VCCGTX-07 VCCGTX-08 VCCGTX-09 VCCGTX-10 VCCGTX-11 VCCGTX-12
RSVD-28 RSVD-29 RSVD-30 RSVD-31 RSVD-32
RSVD-33 RSVD-34
RSVD-35 RSVD-36
VCCST-01 VCCST-02
VCCPLL
LGA1151
ZIF-SOCKET1151-HF-1
VCCPLL_OC
R160 X_0R
R159 0R
VCC_DDR
VCCSFR_OC
VCCIO
V_OPC
V_EOPIO
+VCCGTX
V_OPC_1P8_1
V_OPC_1P8_2
VCCST
60mA
150mA
+VCCGTX
R923 0R
V_OPC_1P8_1
R920 0R
V_OPC_1P8_2
R921 0R
V_OPC
R929 0R
V_EOPIO
R930 0R
VCC_DDR
C688 C689 C691 C690 22u6.3X6
TOP SIDE SOCKET CAVITY
VCCIO
C698 C695 C699 22u6.3X6
TOP SIDE SOCKET CAVITY
VCCSA
C674 C687 C692 C150 22u6.3X6
TOP SIDE SOCKET CAVITY
VCORE
C386 C385 C384 C383 C382 C204 C701 C83 C75 C80 C91 C120 C122 C112 C113 22u6.3X6
C119 C559 C534 C541 C506 C512 C519 C588 C84 22u6.3X6
TOP SIDE SOCKET CAVITY
VGT
C138 22u6.3X8
C137 C139 C504 C651 C505 22u6.3X8
TOP SIDE SOCKET CAVITY
VGT
C341 C345 C349 C354 C356 C359 22u6.3X8
BOTTOM SIDE SOCKET CAVITY
remove
c662
c140
c141
c148
c154
c507
c508
VGT
C509 C673 C702 C73 C77 C78 C82 C103 22u6.3X8
TOP SIDE SOCKET EDGE
VCCST
C686 1u6.3
VCCST
C277 22u6.3X8
VCORE
C655 C115 C118 C121 C129 C130 C132 C197 22u6.3X6
TOP SIDE SOCKET EDGE
remove
c654
c659
c653
c114
c656
VCORE
C143 C153 C149 C157 1u6.3
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size
Custom
Document Description
CPU-Power
Rev
2.1
Date: Wednesday, November 09, 2016
Sheet 7 of 70



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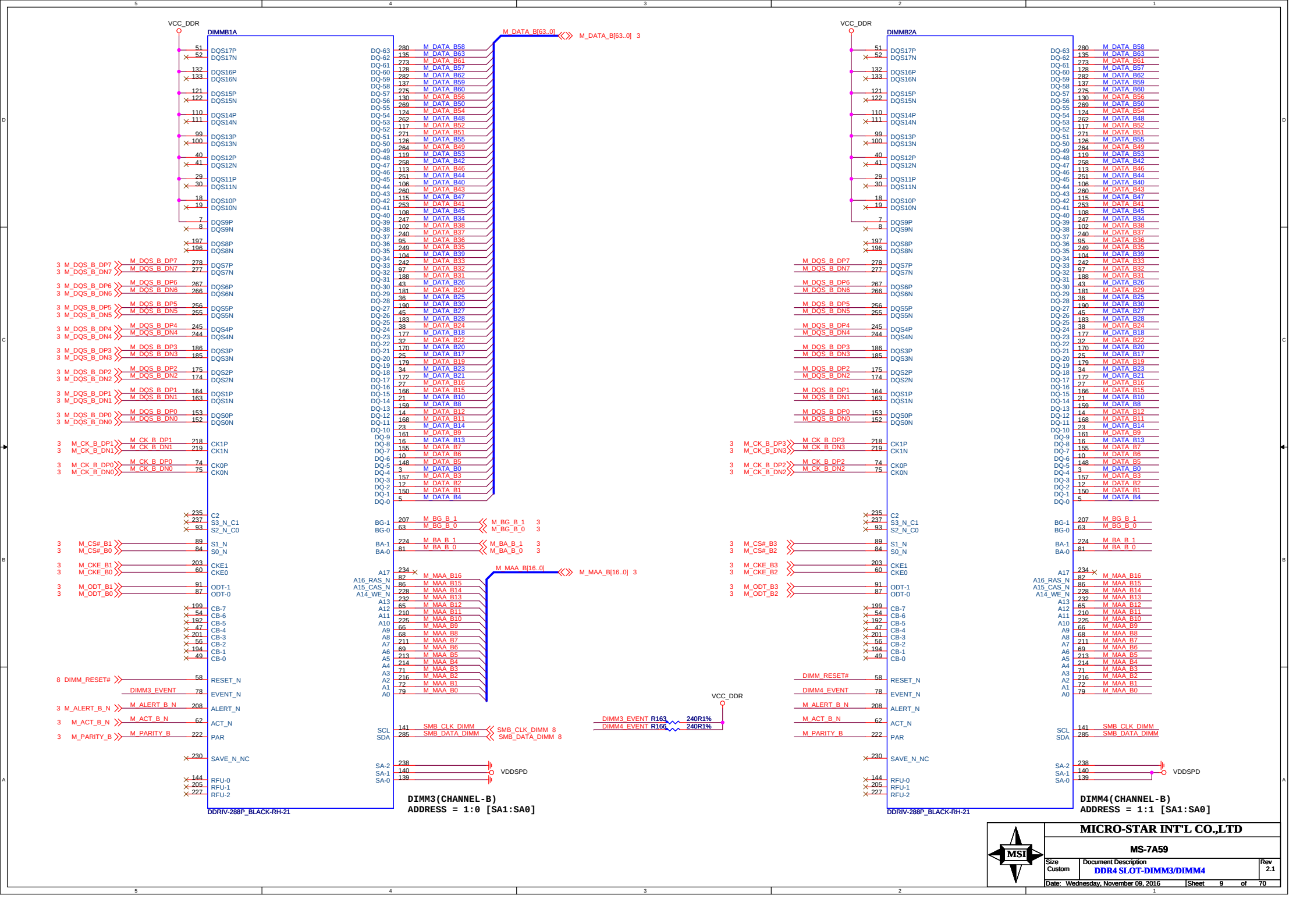
MS-7A59	
Size: Custom	Document Description: DDR4 SLOT-DIMM1/DIMM2
Rev: 2.1	
Date: Wednesday, November 09, 2016	Sheet 8 of 70



MICRO-STAR INT'L CO.,LTD	
MS-7A59	
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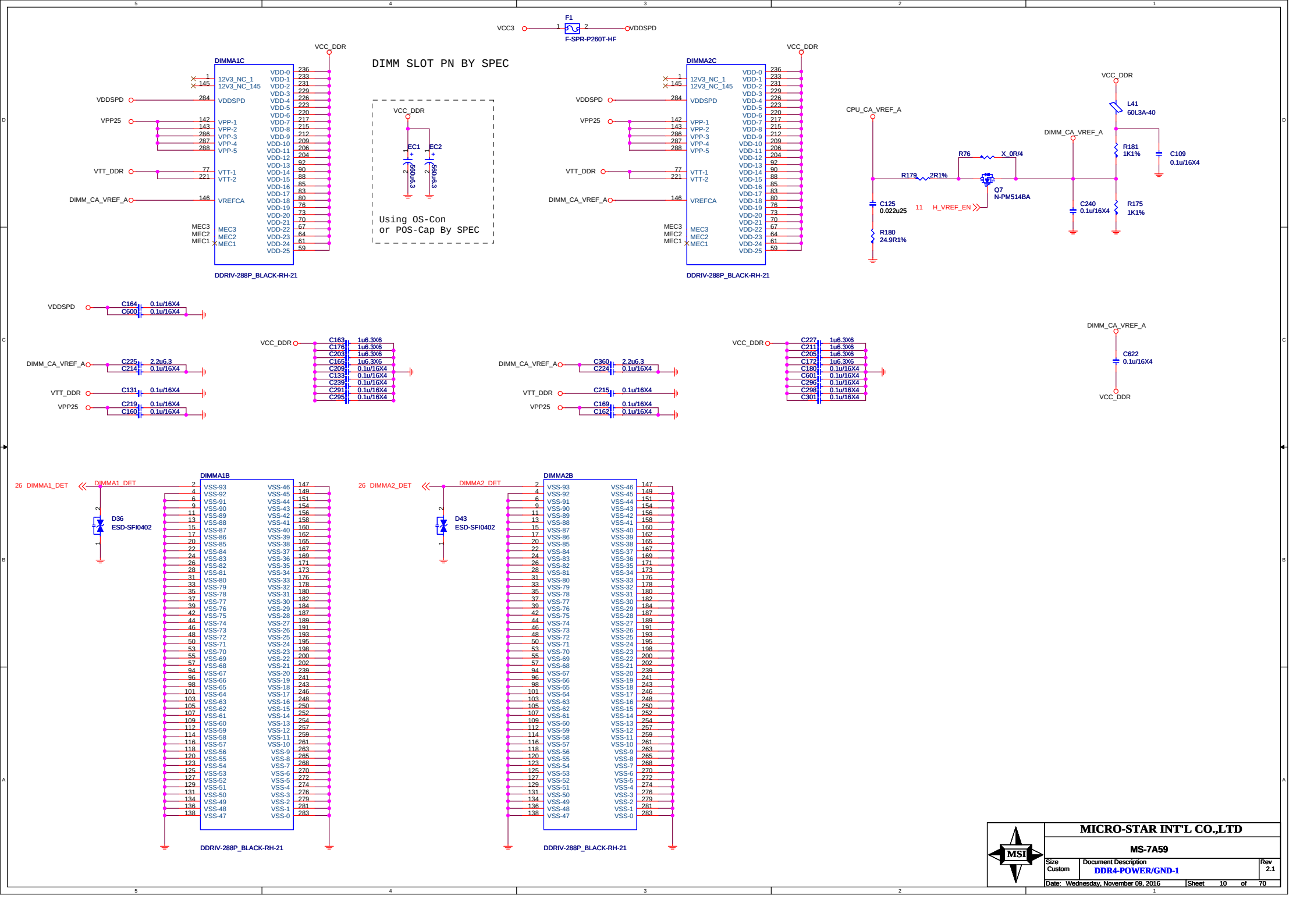
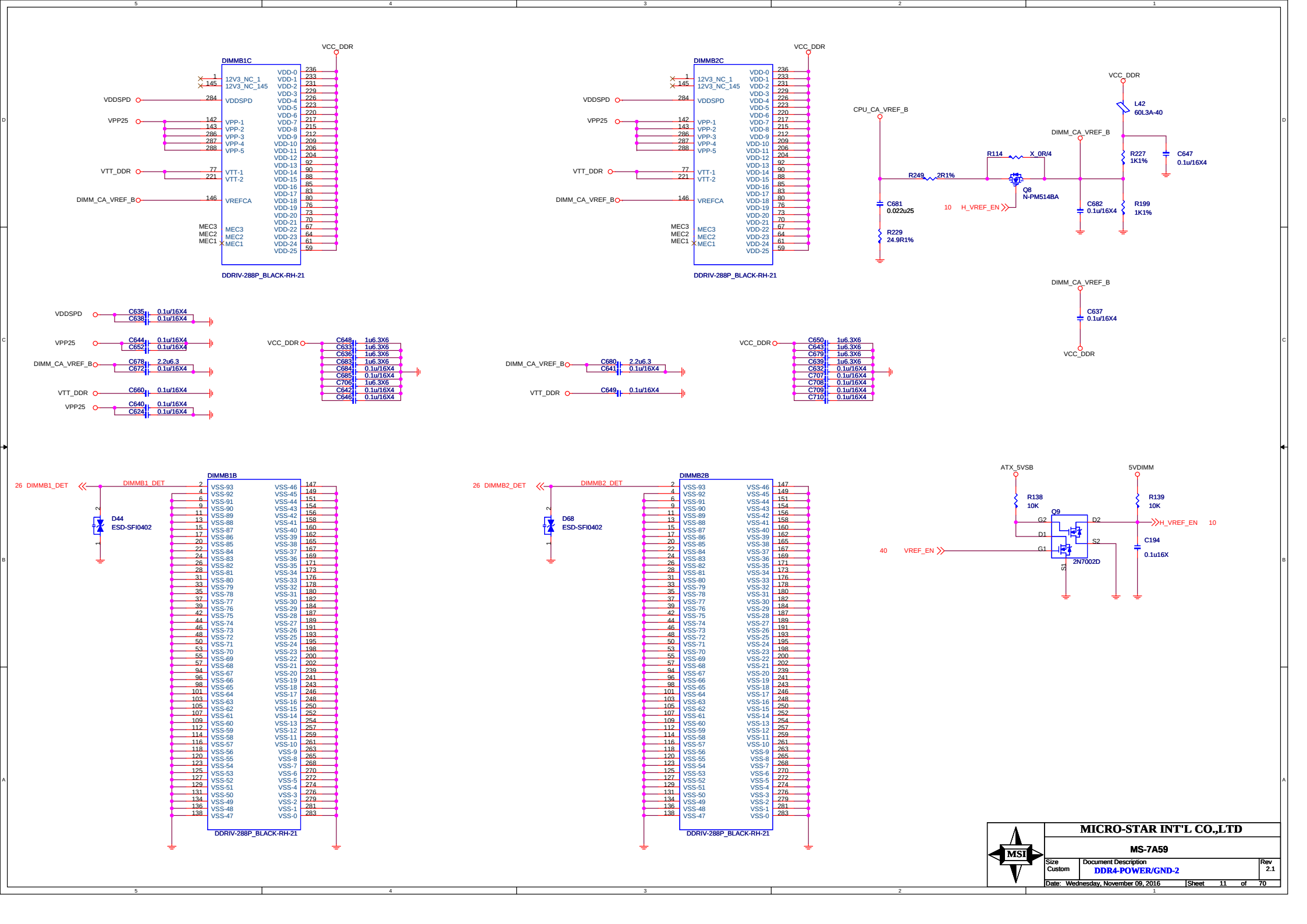
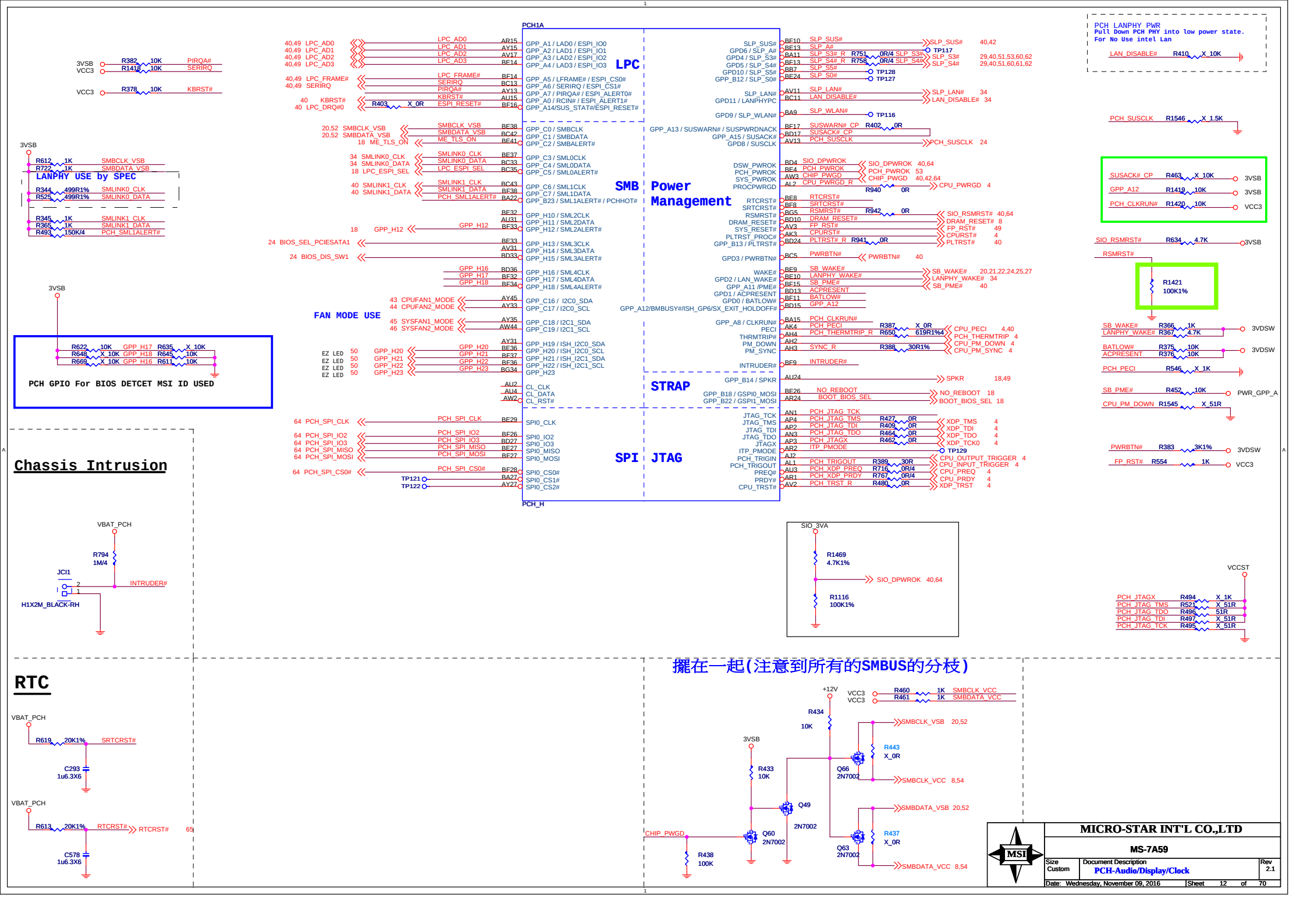
Rev: 2.1	
Date: Wednesday, November 09, 2016	Sheet 9 of 70



MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: DDR4-POWER/GND-1
Rev: 2.1	
Date: Wednesday, November 09, 2016	Sheet 10 of 70

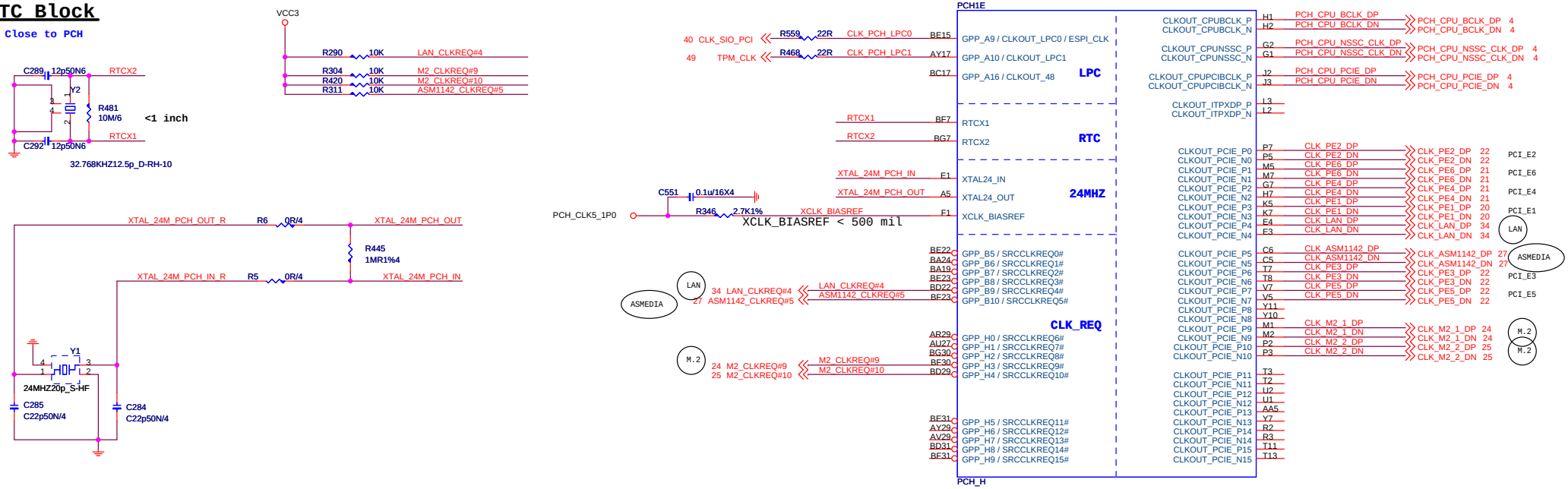

DIMMB1C
VCC_DDR
VDDSPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
DDRIV-288P_BLACK-RH-21
DIMMB2C
CPU_CA_VREF_B
L42
60L3A-40
R114
X_0R/4
R249
2R1%
Q8
N-PM514BA
R227
1K1%
C647
0.1u/16X4
C681
0.022u25
R229
24.9R1%
H_VREF_EN
C682
0.1u/16X4
R199
1K1%
C635
C638
C644
C652
C678
2.2u6.3
C672
C660
C640
C624
C648
C633
C636
C683
C684
C685
C706
C642
C646
1u6.3X6
C680
C641
C649
C637
C650
C643
C679
C639
C632
C707
C708
C709
C710
DIMMB1B
DIMMB2B
26 DIMMB1_DET
DIMMB1_DET
D44
ESD-SFI0402
26 DIMMB2_DET
DIMMB2_DET
D68
ESD-SFI0402
ATX_5VSB
5VDIMM
R138
10K
R139
10K
Q9
2N7002D
C194
0.1u16X
40
VREF_EN
10
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size
Custom
Document Description
DDR4-POWER/GND-2
Rev
2.1
Date: Wednesday, November 09, 2016
Sheet 11 of 70


PCH1A
LPC
SMB
Power Management
STRAP
SPI
JTAG
PCH_H
LANPHY USE by SPEC
FAN MODE USE
PCH GPIO For BIOS DETCET MSI ID USED
Chassis Intrusion
RTC
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
摆在一起(注意到所有的SMBUS的分枝)
MICRO-STAR INT'L CO.,LTD
MS-7A59
PCH-Audio/Display/Clock
Date: Wednesday, November 09, 2016
Sheet 12 of 70

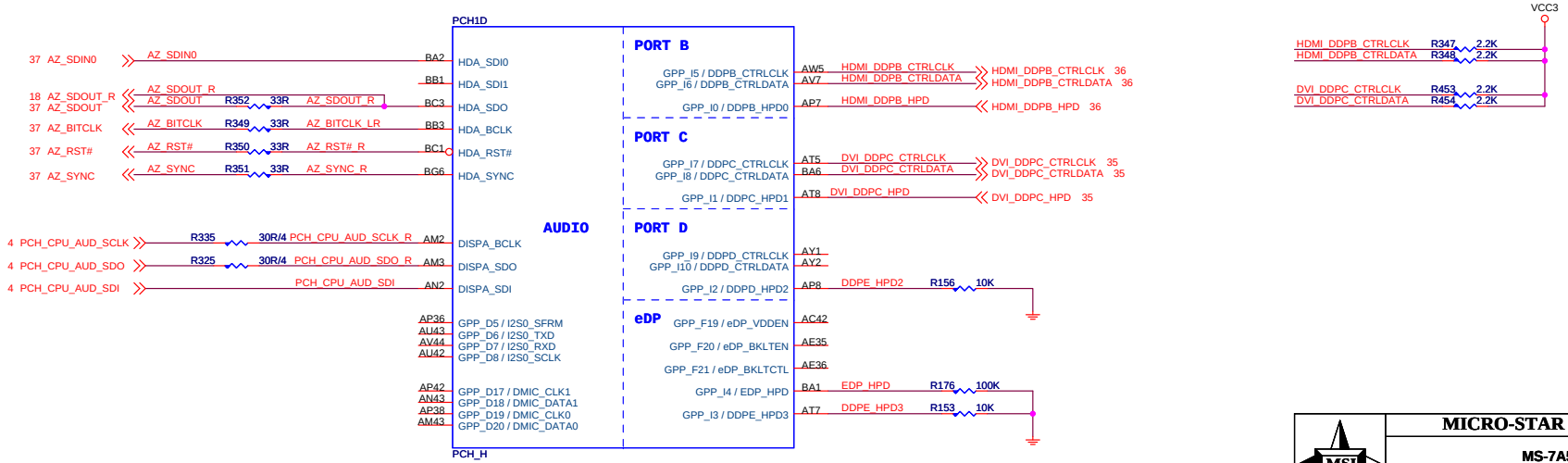
PCH_CLK

RTC Block

Close to PCH



Vinafix.com



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	MS-7A59	
Size: Custom	Document Description: PCH-USB/PCIE/DMI/SATA	Rev: 2.1
Date: Wednesday, November 09, 2016	Sheet 13 of 70	

PCH1B

DMI

PCIE

PCH_H

PCH1C

USB3

USB2

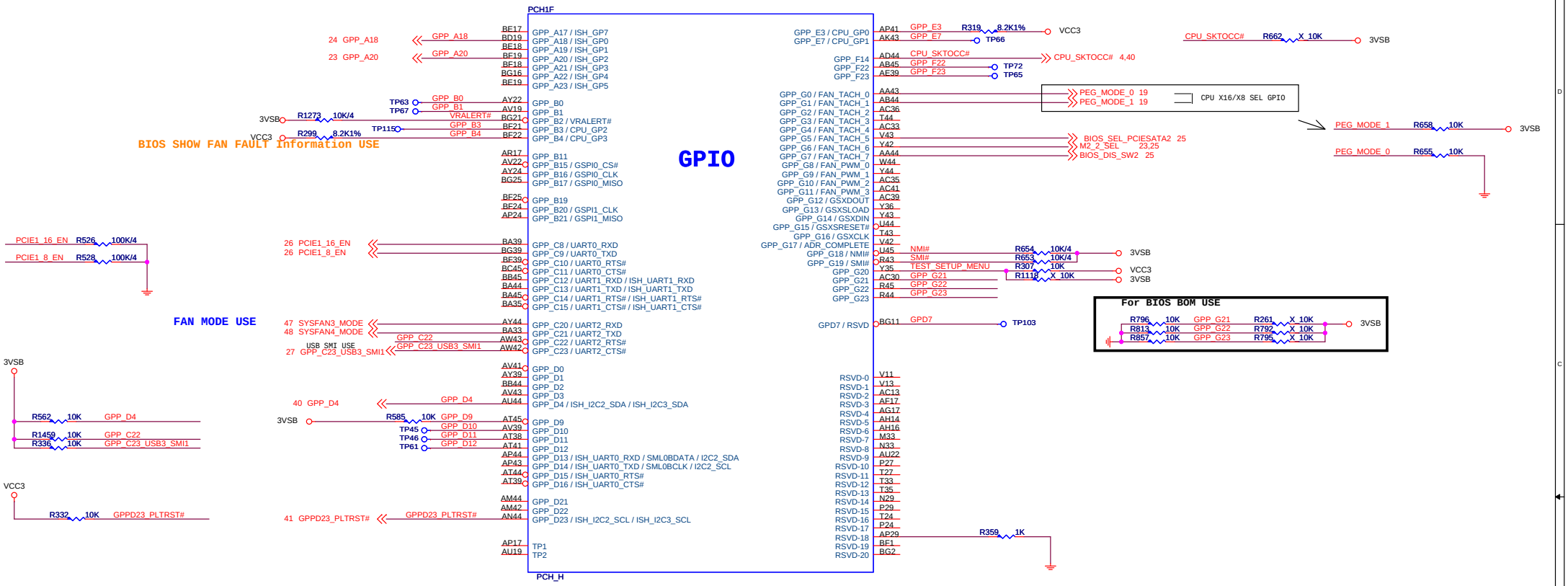
PCH_H

PCIECOMP_P
PCIECOMP_N
Length Match < 5mil

SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA

KB CRB

MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: PCH-GPIO/USBOC#/SATASTRAP
Rev: 2.1	
Date: Wednesday, November 09, 2016	Sheet 14 of 70



MICRO-STAR INT'L CO.,LTD		
MS-7A59		
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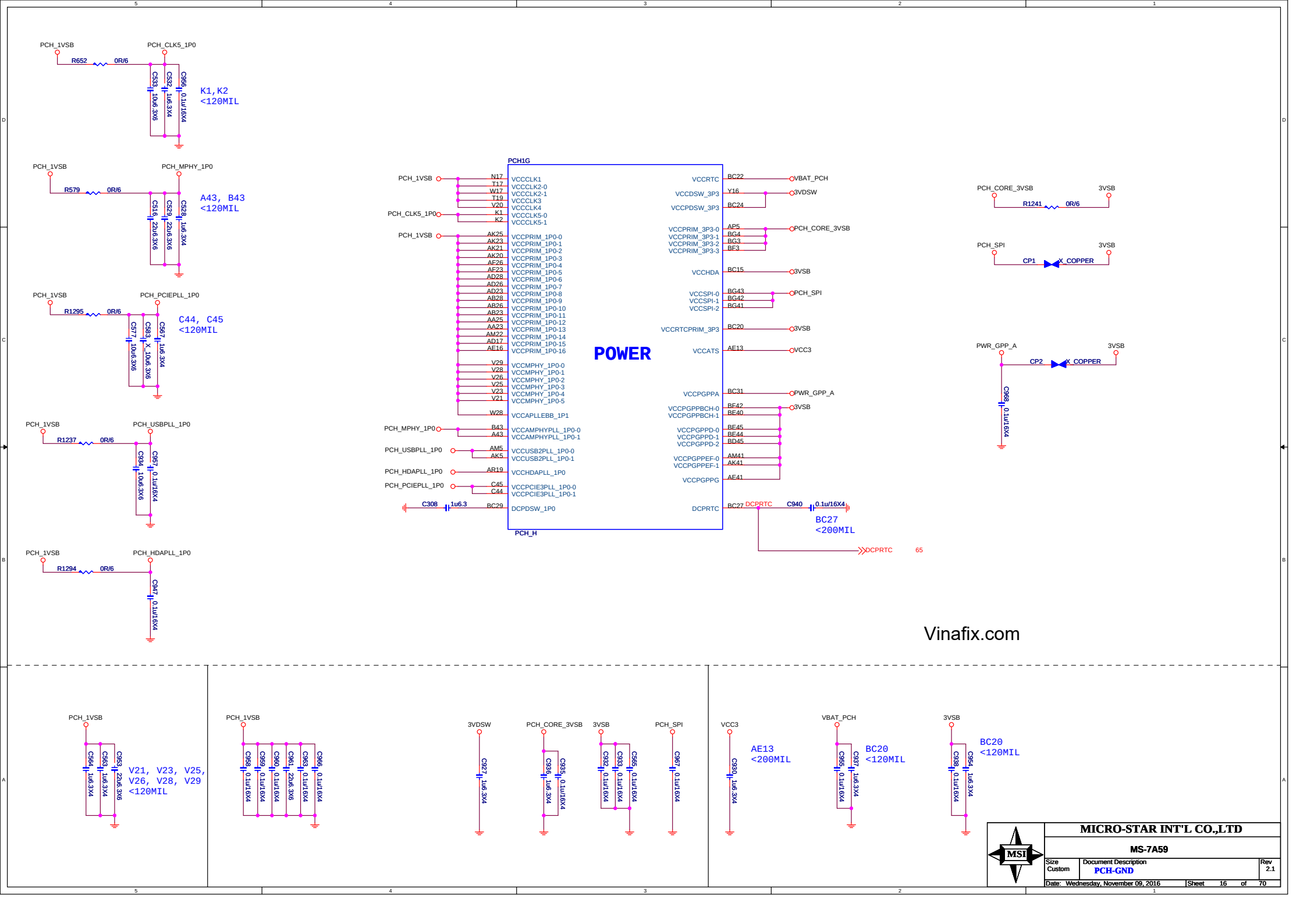
Date: Wednesday, November 09, 2016	Sheet 15 of 70	


PCH_1VSB
PCH_CLK5_1P0
R652
0R/6
C553
10u6.3X6
C552
1u6.3X4
C956
0.1u/16X4
K1,K2
<120MIL
PCH_1VSB
PCH_MPHY_1P0
R579
0R/6
C516
22u6.3X6
C529
22u6.3X6
C528
1u6.3X4
A43, B43
<120MIL
PCH_1VSB
PCH_PCIEPLL_1P0
R1295
0R/6
C577
10u6.3X6
C583
X_10u6.3X6
C567
1u6.3X4
C44, C45
<120MIL
PCH_1VSB
PCH_USBPLL_1P0
R1237
0R/6
C934
10u6.3X6
C957
0.1u/16X4
PCH_1VSB
PCH_HDAPLL_1P0
R1294
0R/6
C947
0.1u/16X4
PCH1G
POWER
PCH_H
PCH_1VSB
PCH_CLK5_1P0
PCH_1VSB
PCH_MPHY_1P0
PCH_USBPLL_1P0
PCH_HDAPLL_1P0
PCH_PCIEPLL_1P0
C308
1u6.3
VCCCLK1
VCCCLK2-0
VCCCLK2-1
VCCCLK3
VCCCLK4
VCCCLK5-0
VCCCLK5-1
VCCPRIM_1P0-0
VCCPRIM_1P0-1
VCCPRIM_1P0-2
VCCPRIM_1P0-3
VCCPRIM_1P0-4
VCCPRIM_1P0-5
VCCPRIM_1P0-6
VCCPRIM_1P0-7
VCCPRIM_1P0-8
VCCPRIM_1P0-9
VCCPRIM_1P0-10
VCCPRIM_1P0-11
VCCPRIM_1P0-12
VCCPRIM_1P0-13
VCCPRIM_1P0-14
VCCPRIM_1P0-15
VCCPRIM_1P0-16
VCCMPHY_1P0-0
VCCMPHY_1P0-1
VCCMPHY_1P0-2
VCCMPHY_1P0-3
VCCMPHY_1P0-4
VCCMPHY_1P0-5
VCCAPLLEBB_1P1
VCCAMPHYPLL_1P0-0
VCCAMPHYPLL_1P0-1
VCCUSB2PLL_1P0-0
VCCUSB2PLL_1P0-1
VCCHDAPLL_1P0
VCCPCIE3PLL_1P0-0
VCCPCIE3PLL_1P0-1
DCPDSW_1P0
VCCRTC
VCCDSW_3P3
VCCPDSW_3P3
VCCPRIM_3P3-0
VCCPRIM_3P3-1
VCCPRIM_3P3-2
VCCPRIM_3P3-3
VCCHDA
VCCSPI-0
VCCSPI-1
VCCSPI-2
VCCRTCPRIM_3P3
VCCATS
VCCPGPPA
VCCPGPPBCH-0
VCCPGPPBCH-1
VCCPGPPD-0
VCCPGPPD-1
VCCPGPPD-2
VCCPGPPEF-0
VCCPGPPEF-1
VCCPGPPG
DCPRTC
VBAT_PCH
3VDSW
PCH_CORE_3VSB
3VSB
PCH_SPI
VCC3
DCPRTC
C940
0.1u/16X4
BC27
<200MIL
DCPRTC
65
PCH_CORE_3VSB
3VSB
R1241
0R/6
PCH_SPI
3VSB
CP1
X_COPPER
PWR_GPP_A
3VSB
CP2
X_COPPER
C968
0.1u/16X4
Vinafix.com
PCH_1VSB
C564
1u6.3X4
C563
1u6.3X4
C953
22u6.3X6
V21, V23, V25,
V26, V28, V29
<120MIL
PCH_1VSB
C958
0.1u/16X4
C959
0.1u/16X4
C960
0.1u/16X4
C961
22u6.3X6
C963
0.1u/16X4
C966
0.1u/16X4
3VDSW
C927
1u6.3X4
PCH_CORE_3VSB
C936
1u6.3X4
C935
0.1u/16X4
3VSB
C932
0.1u/16X4
C933
0.1u/16X4
C965
0.1u/16X4
PCH_SPI
C967
0.1u/16X4
VCC3
C930
1u6.3X4
AE13
<200MIL
VBAT_PCH
C955
0.1u/16X4
C937
1u6.3X4
BC20
<120MIL
3VSB
C938
0.1u/16X4
C954
1u6.3X4
BC20
<120MIL
MSI
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size
Custom
Document Description
PCH-GND
Rev
2.1
Date: Wednesday, November 09, 2016
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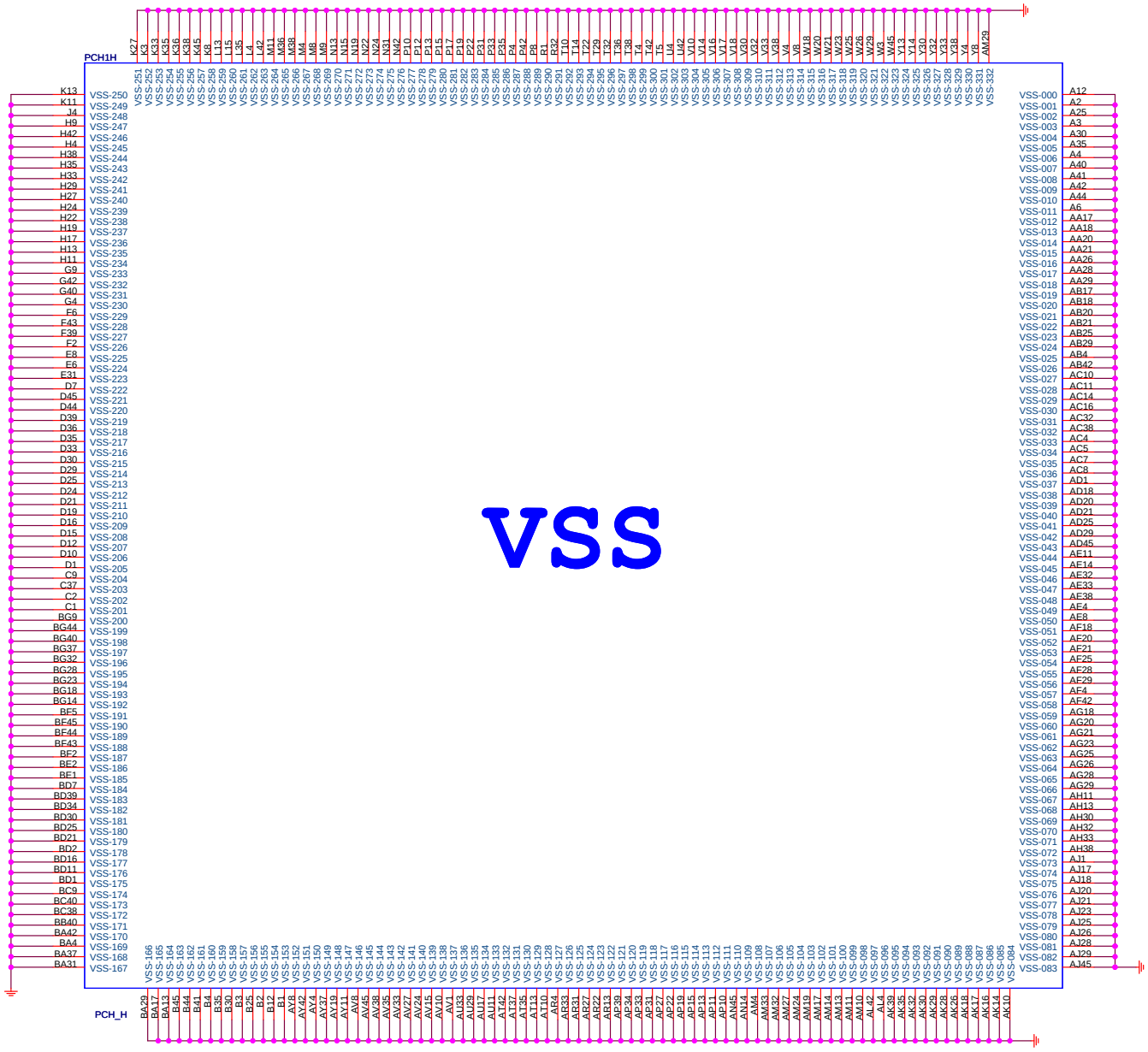

MICRO-STAR INT'L CO.,LTD		
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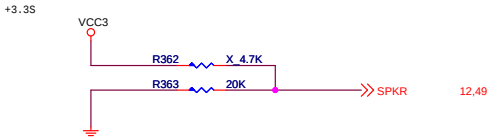
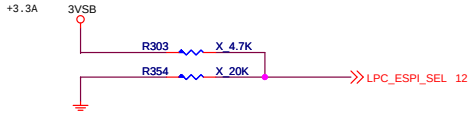
TOP Swap



Internal pull-down is disabled after PLTRST#

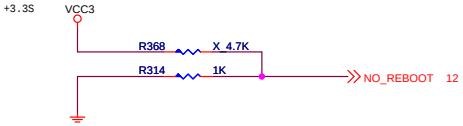
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

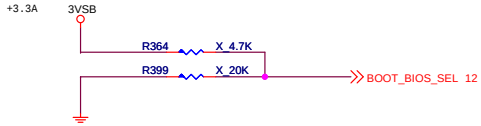
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

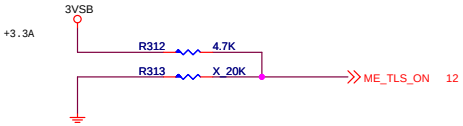
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

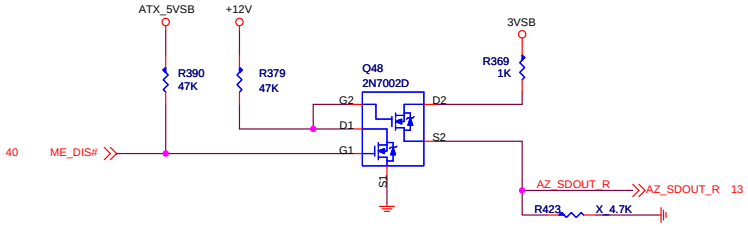
AMT and SBA with confidentiality



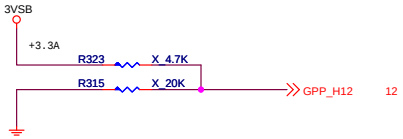
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

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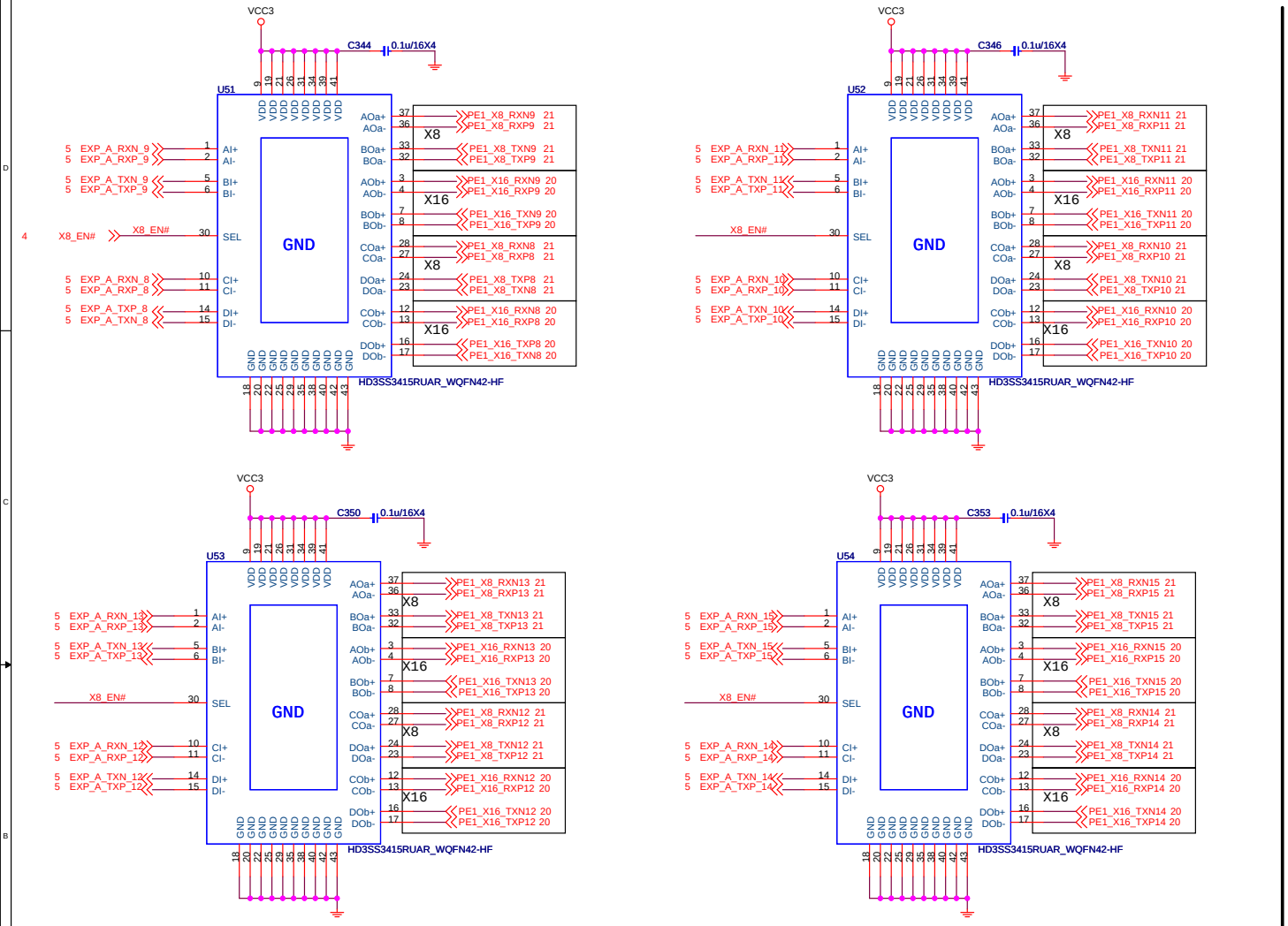

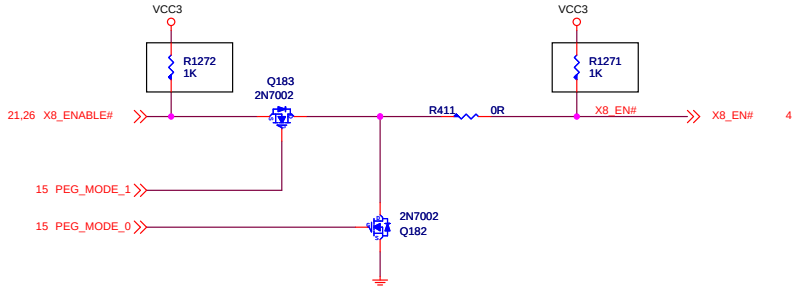

MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

MODE_1/3

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0/2	MODE_1
AUTO	0	1

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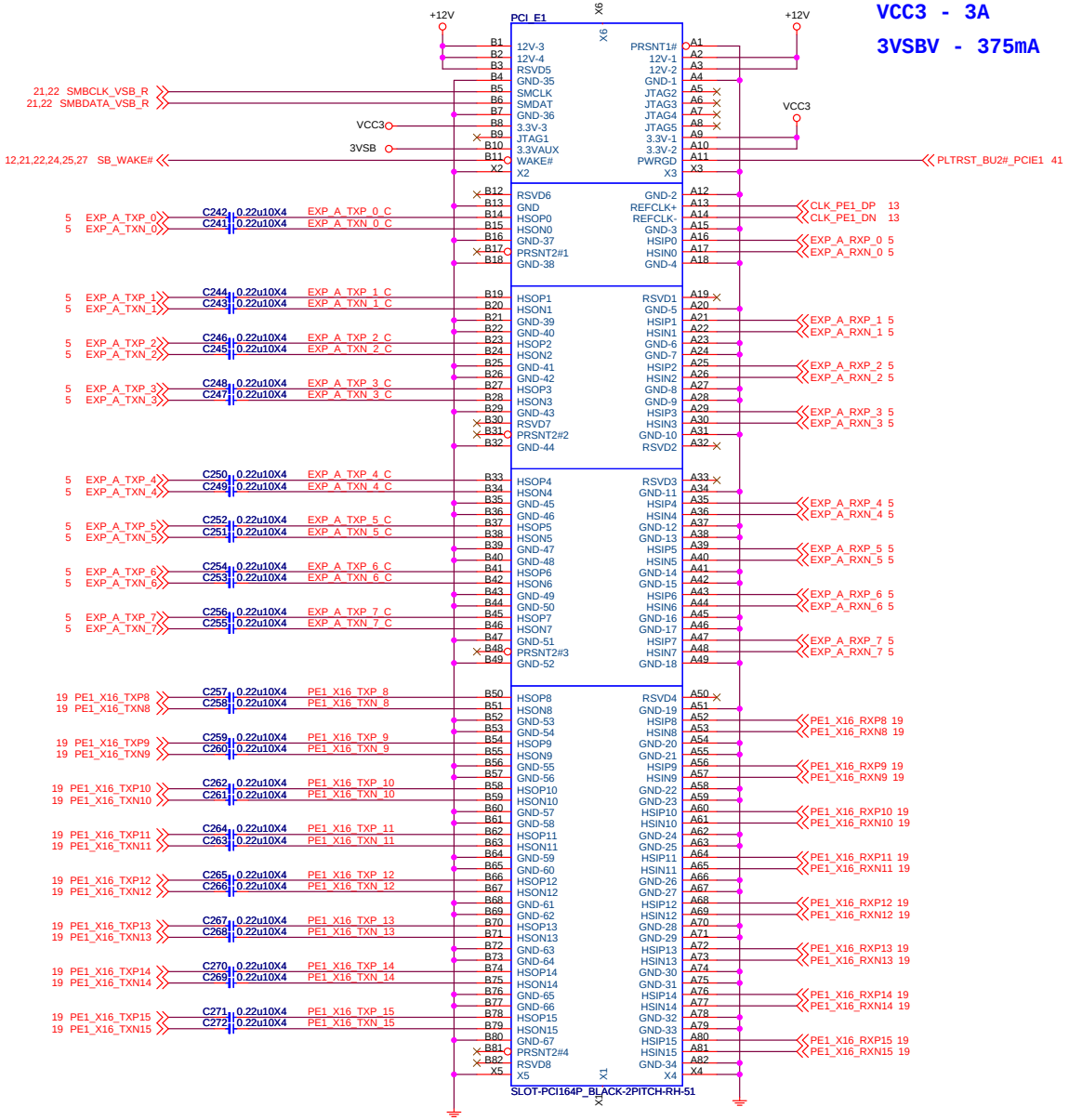
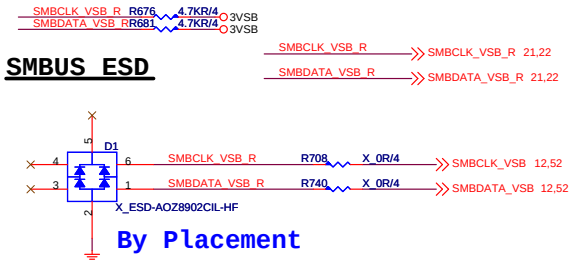
12V - 5.5A

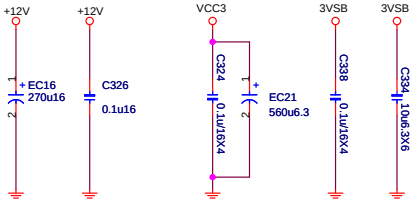
VCC3 - 3A

3VSBV - 375mA



SMBUS_ESD





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Custom	PCIE SLOT (X16)	2.1

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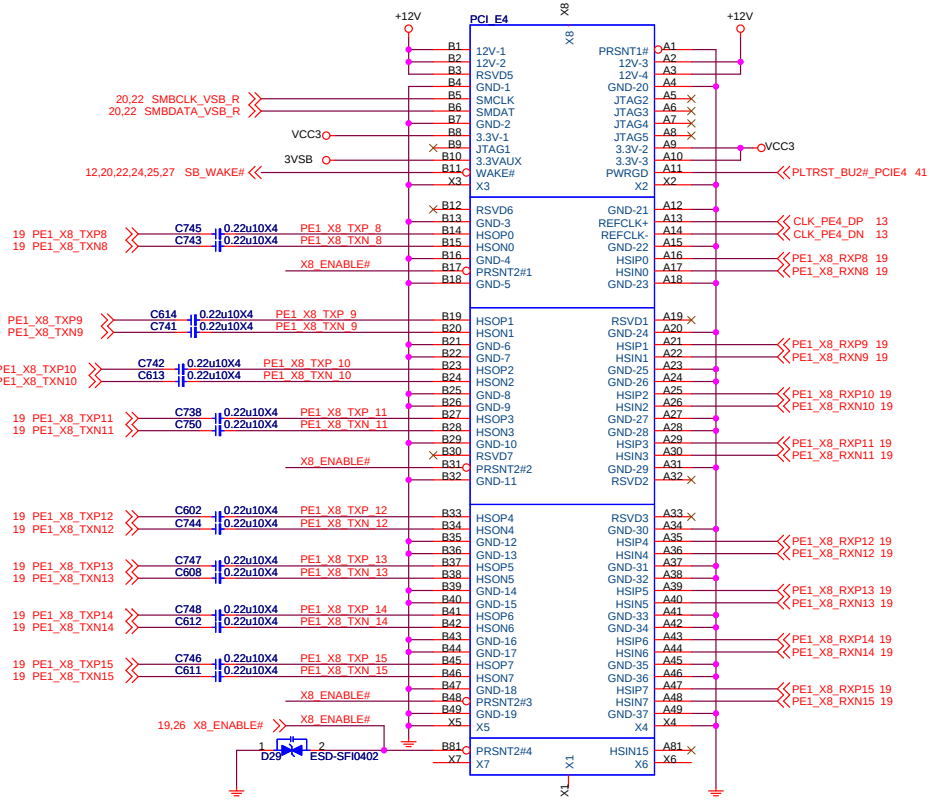
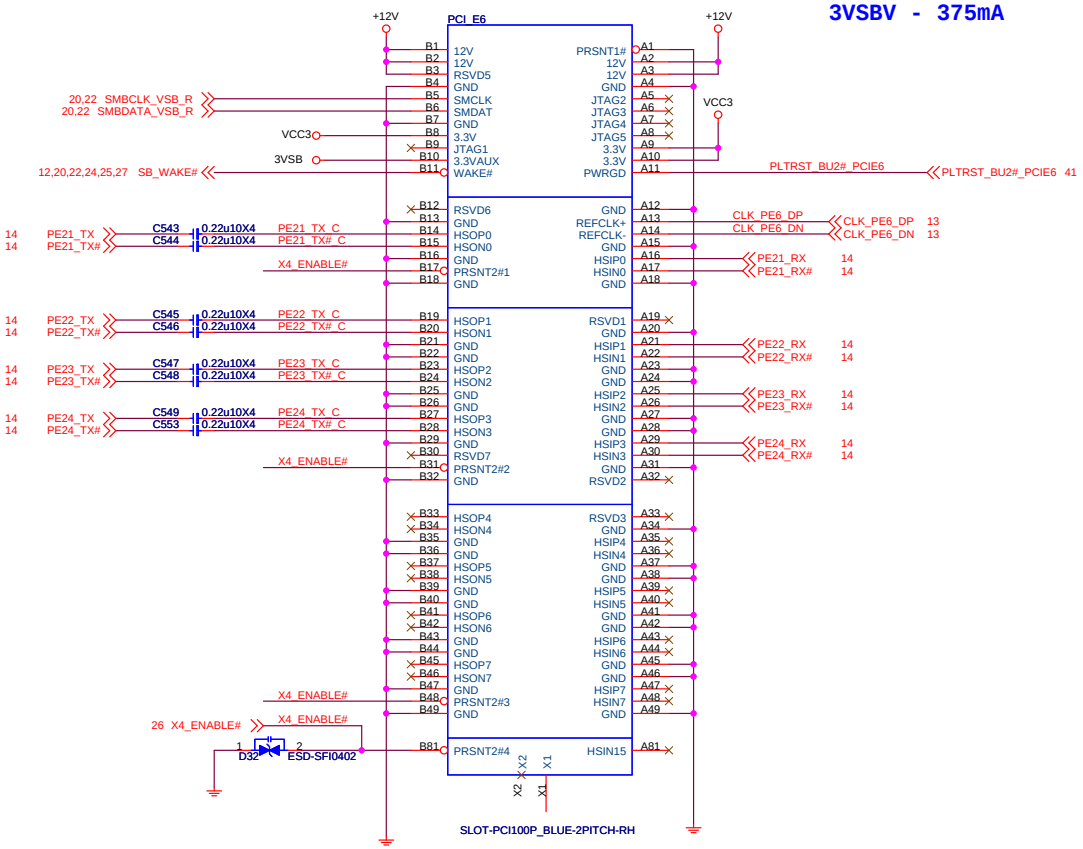
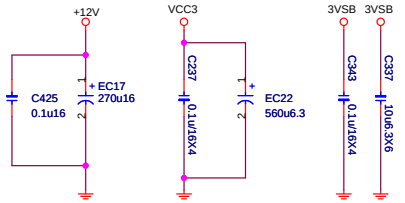
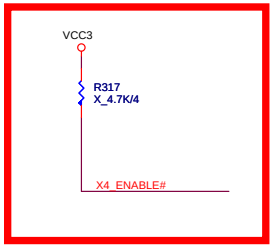
PCI_Express X4 Slot

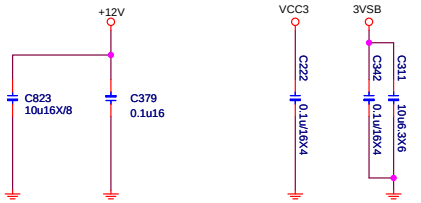
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA











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Size: Custom	Document Description: PCIE SLOT (X4)	Rev: 2.1
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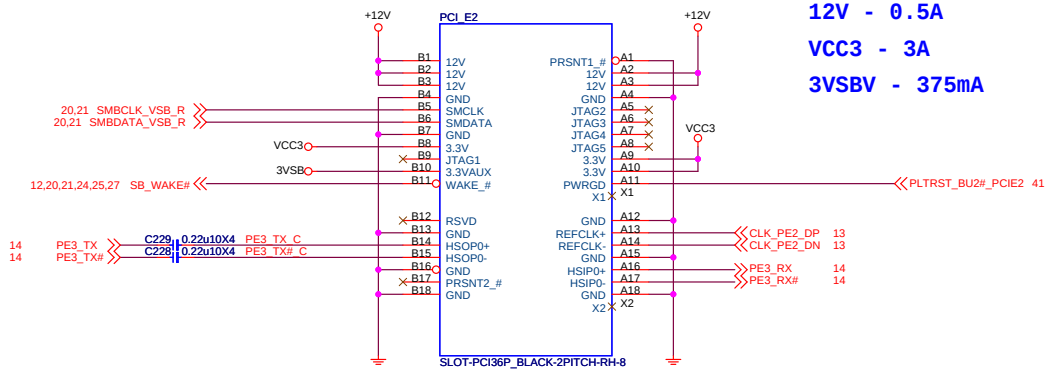

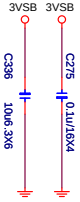

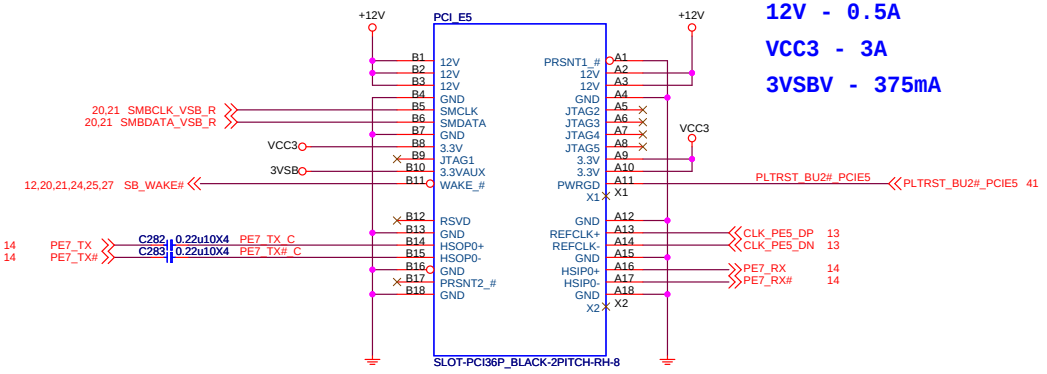

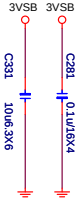

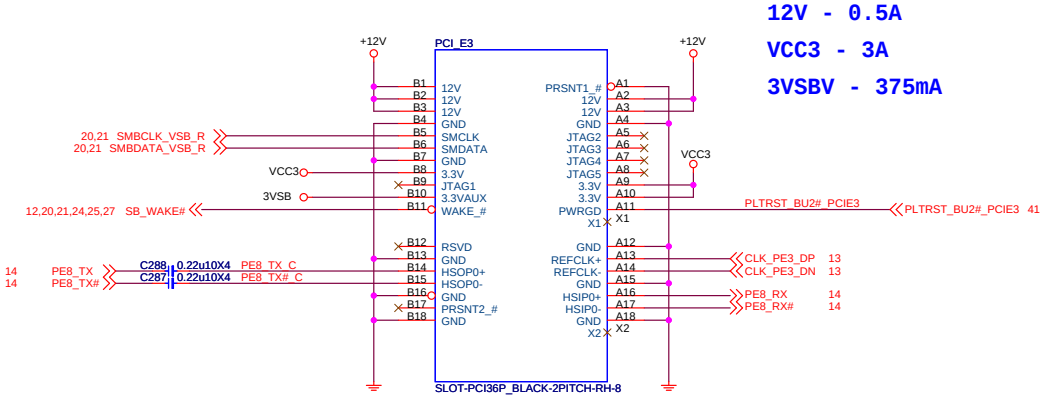

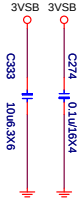

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Size	Document Description	Rev
Custom	PCIE SLOT (X1)	2.1

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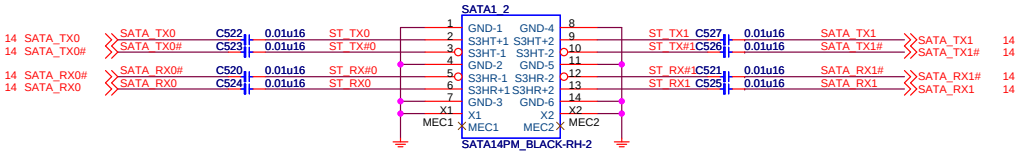

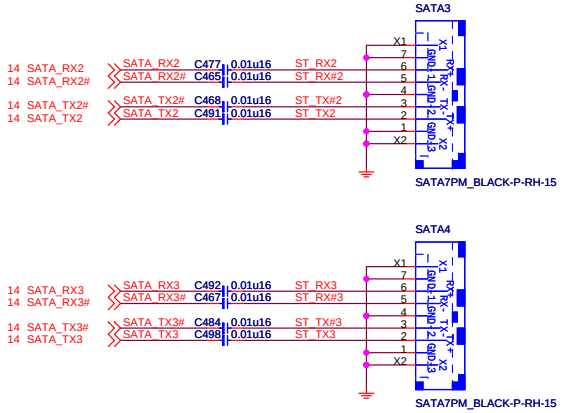

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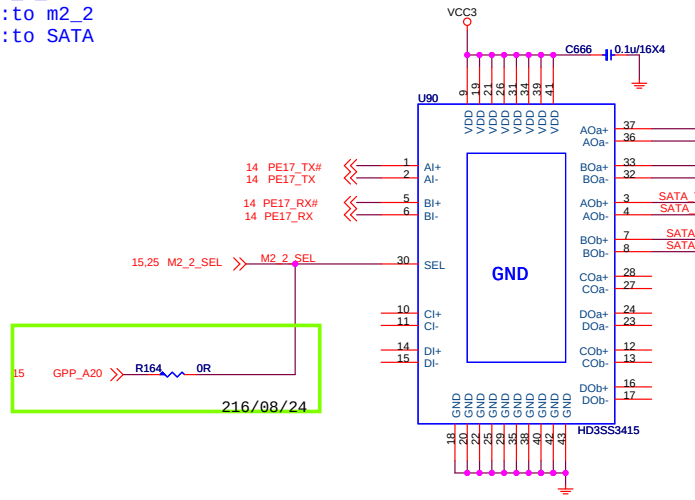
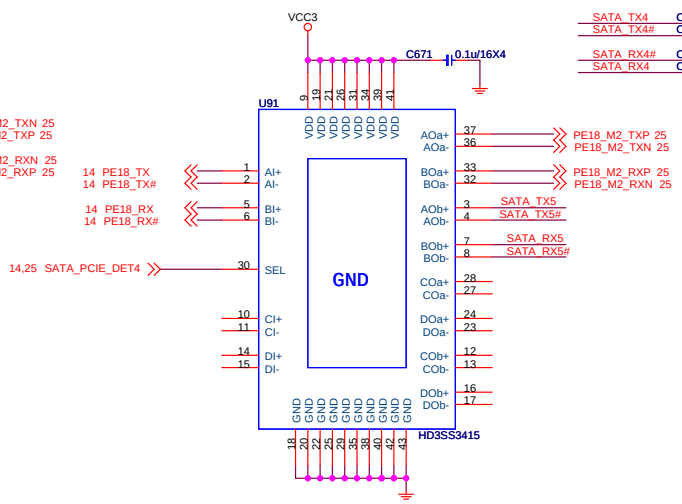
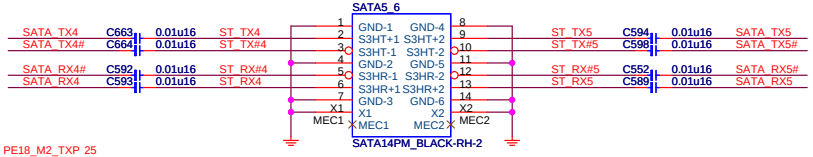
M2_2_SEL
0:to m2_2
1:to SATA







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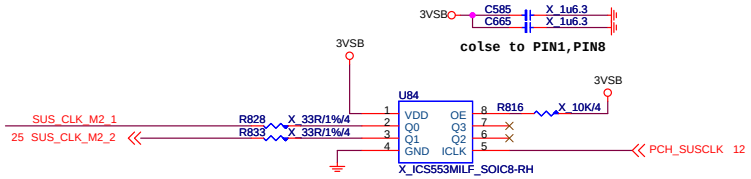
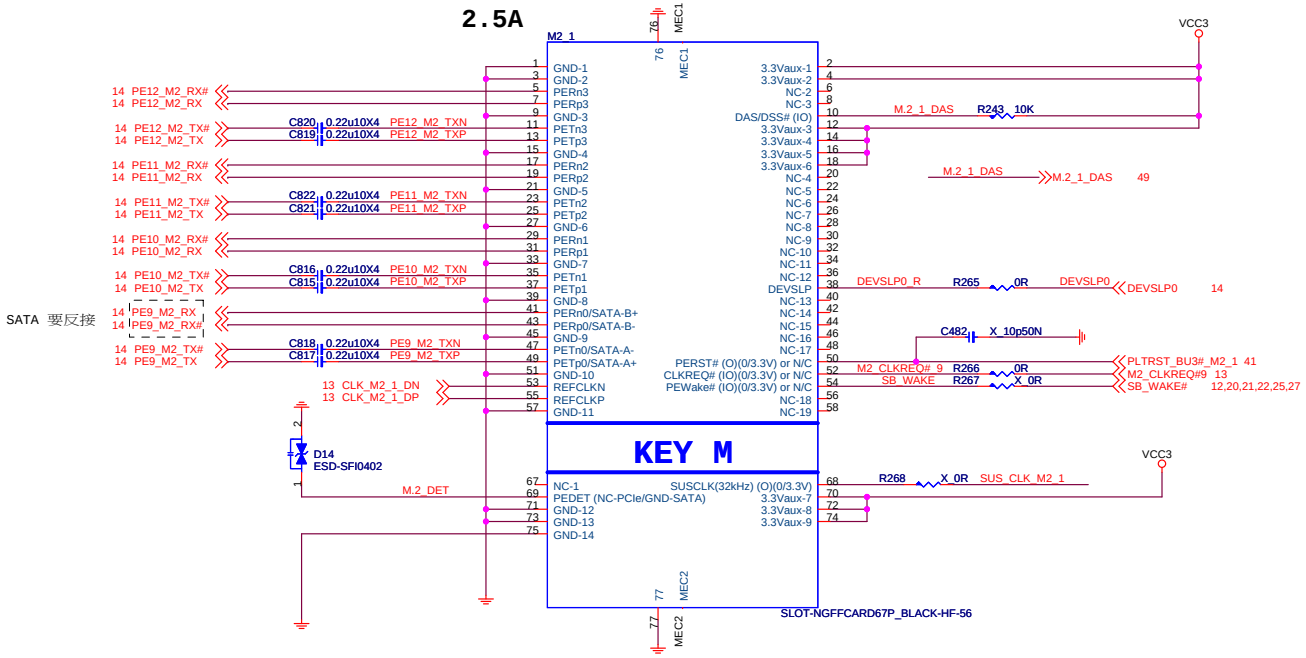
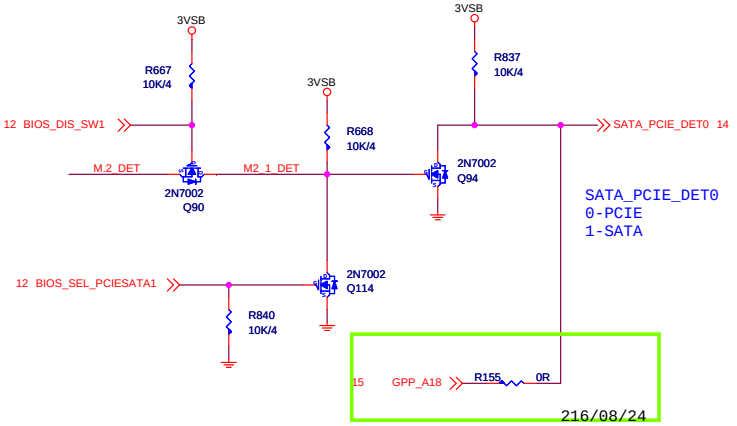
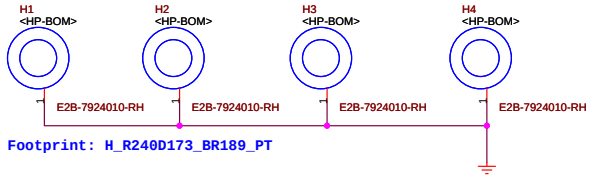


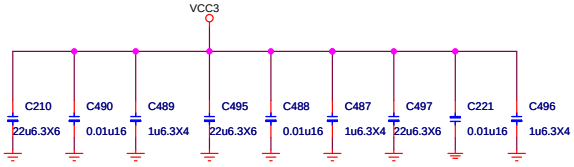




BIOS_MODE

BIOS_DIS_SW	*BIOS_SEL_PCIESATA1*	*Mode*
0	*1*	*M2-SATA*
0	*0*	*M2-PCIE*
GPI	*GPI*	*AUTO*





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Custom	M.2-SLOT1	2.1

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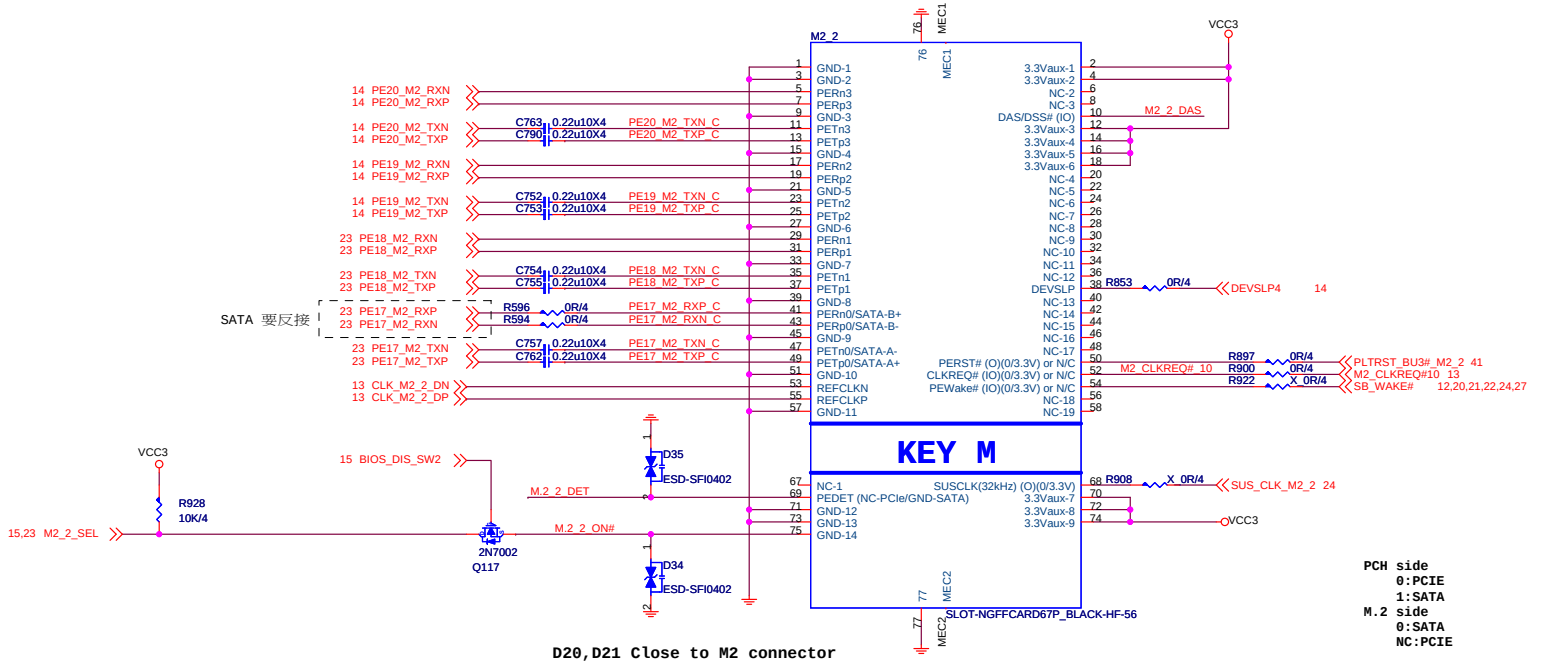
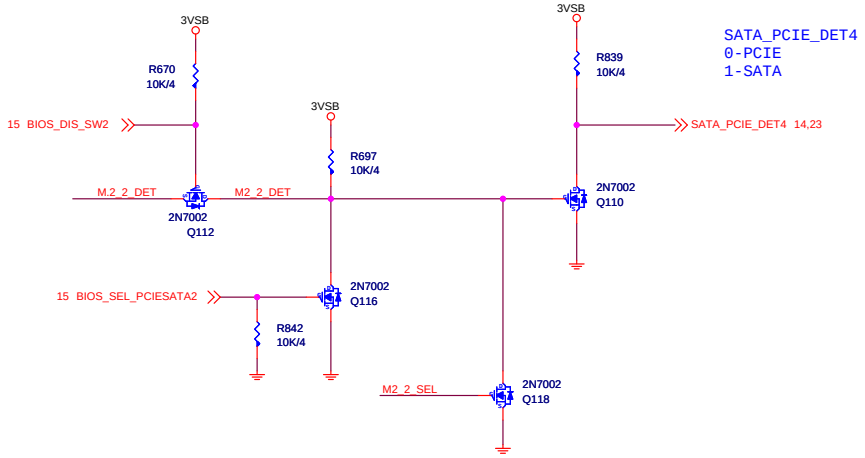
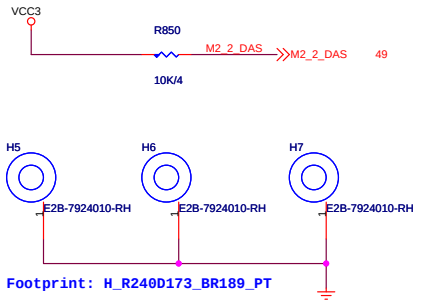


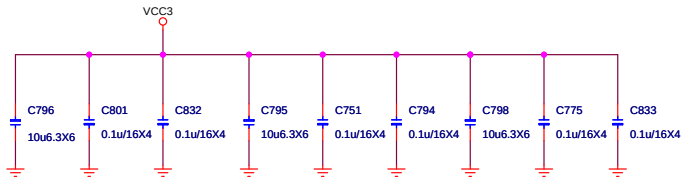
SCREW2
SCREW
M2_SCREW



BIOS_MODE

BIOS_DIS_SW	*M2_2_SEL*	*BIOS_SEL_PCIESATA2*	*Mode*
GPI(1)	*GPI(1)*	*GPI(0)*	*AUTO*
0	*1*	*0*	*SATA*
0	*0*	*1*	*M2-SATA*
0	*0*	*0*	*M2-PCIE*





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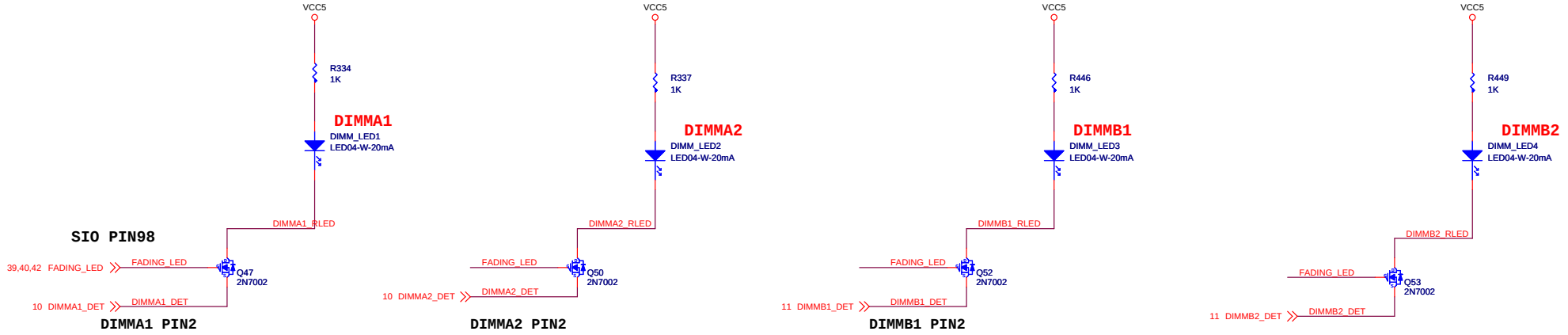
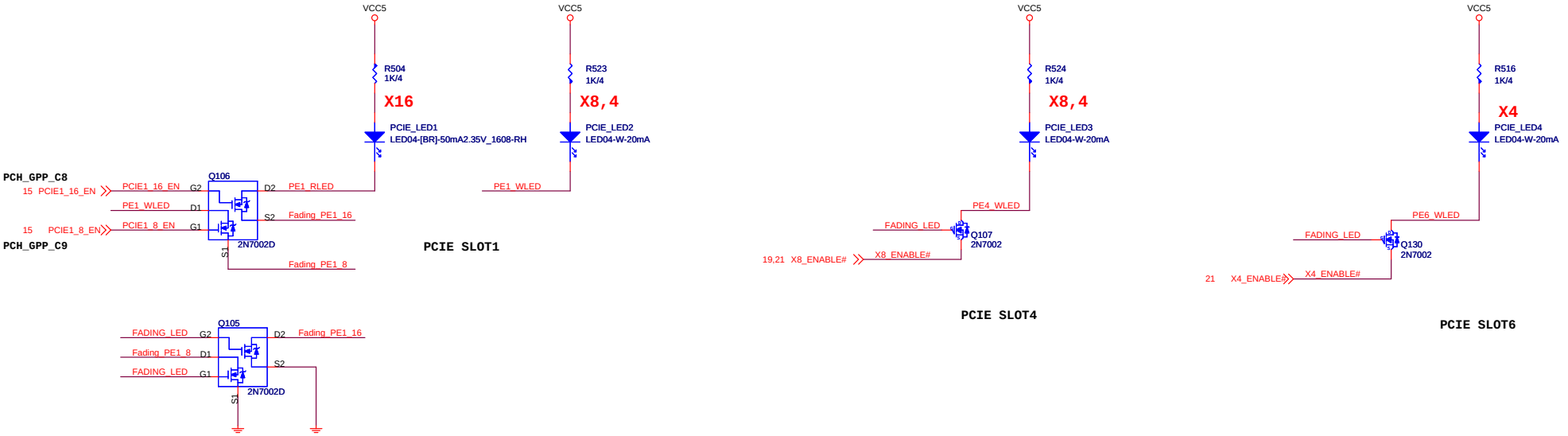
DIMM_SLOT

KRAIT GAMING LED >>WHITE:DOC-040S200-E07



LED 命名請以DIMM_LEDn n為數字

PCIE SLOT LED



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Minimun gap should be greater of
>15mil with other signal.

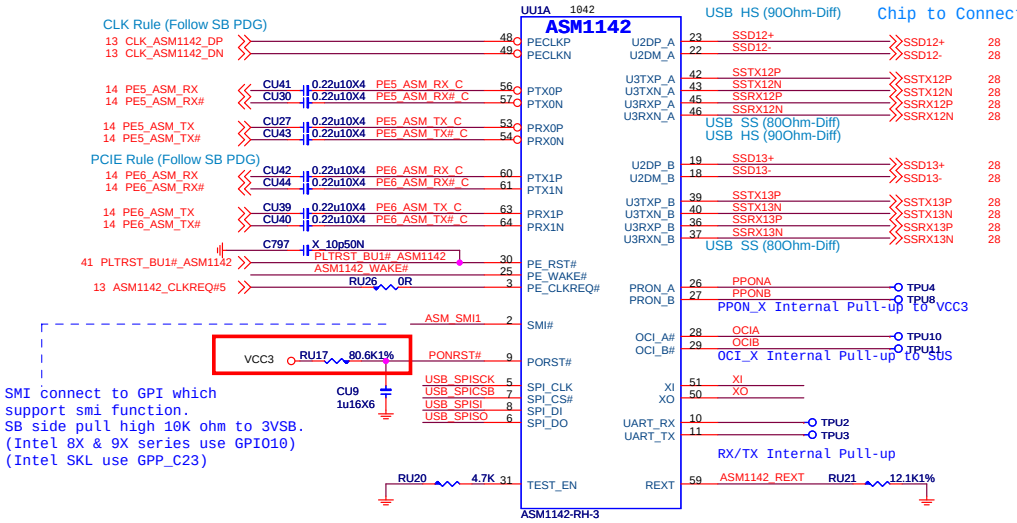
USB HS (90Ohm-Diff) Chip to Connector 1.5 inch.

Power Consumption

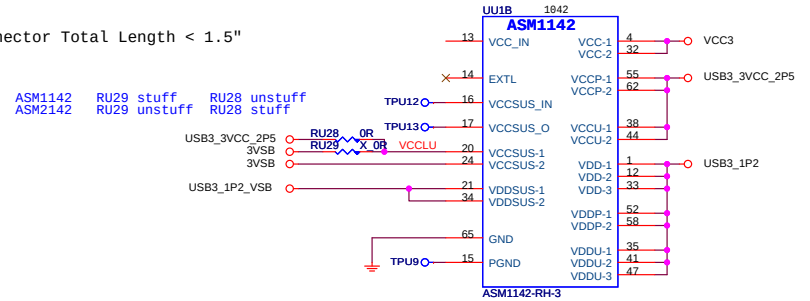
	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA		1573.8(mW)
ASM2142	TDP	TDP	TDP	TDP	300mA(TDP)	TDP

Layout Guide:

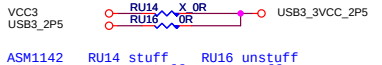
1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2



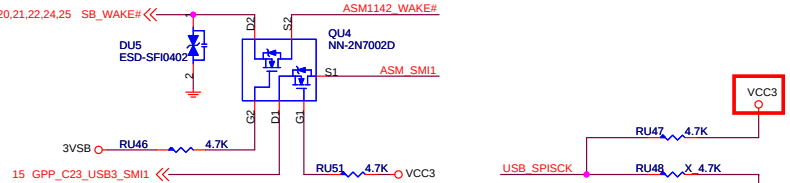
SMI connect to GPI which
support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

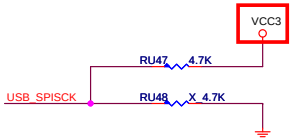


ASM1142 RU29 stuff RU28 unstuff
ASM2142 RU29 unstuff RU28 stuff

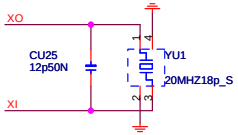


ASM1142 RU14 stuff RU16 unstuff
ASM2142 RU14 unstuff RU16 stuff

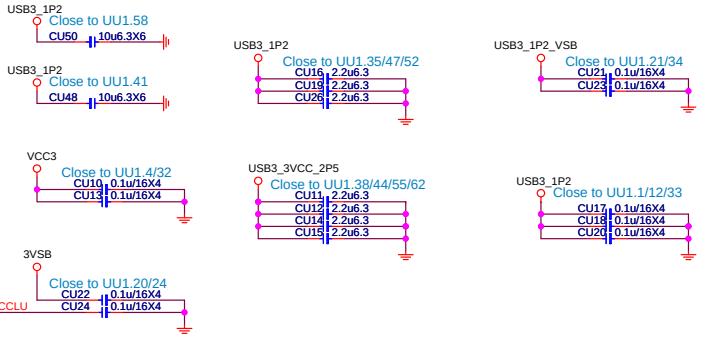




X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8



YU1
D04-0901200-F07
D04-0901100-T16

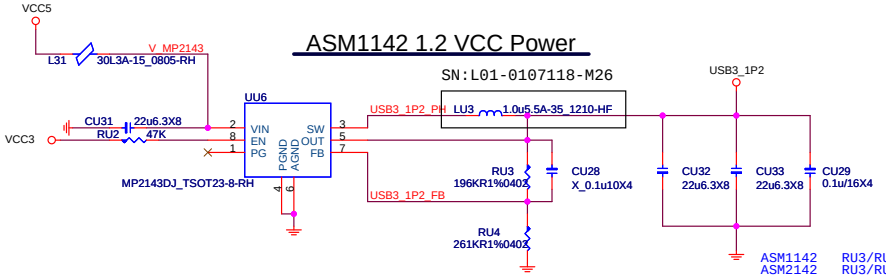


atx5vsb change to vcc5

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

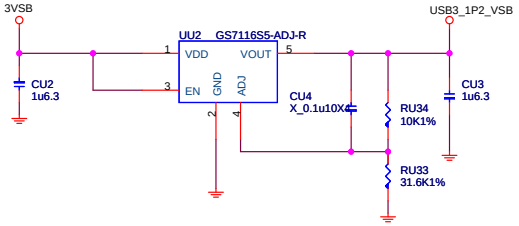
ASM1142 1.2 VCC Power

SN:L01-0107118-M26



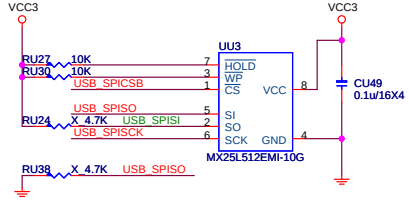
ASM1142 RU3/RU4 200K/187K__1.24V
ASM2142 RU3/RU4 196K/261K__1.05V

ASM1142 1.2 VSB Power

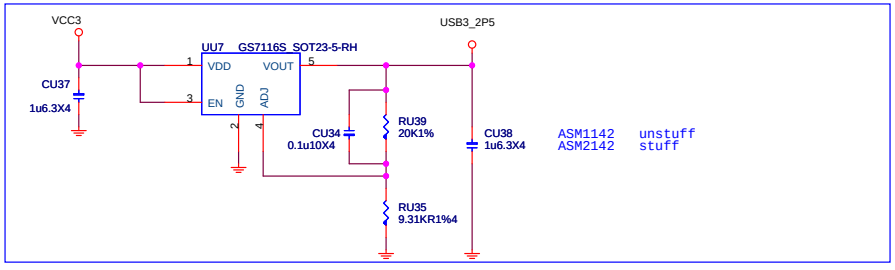


ASM1142 RU33 18K____1.24V
ASM2142 RU33 31.6K__1.05V

EEPROM



ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-25L1022-M24(1M bit)



ASM1142 unstuff
ASM2142 stuff

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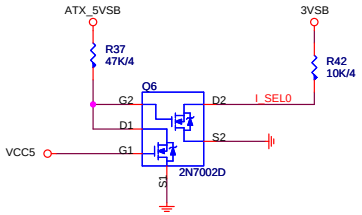
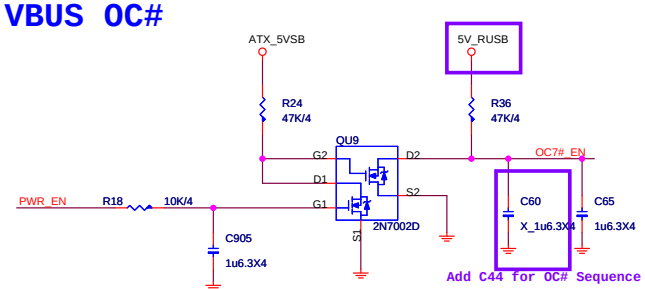
Current Mode

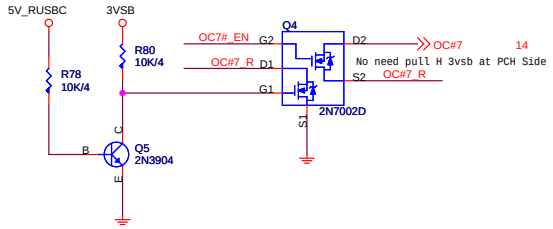


I_SEL0 : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

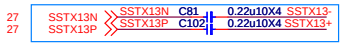
1.5A under S3 mode
3A under S0 mode

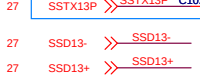
VBUS OC#

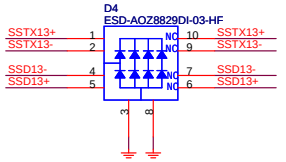


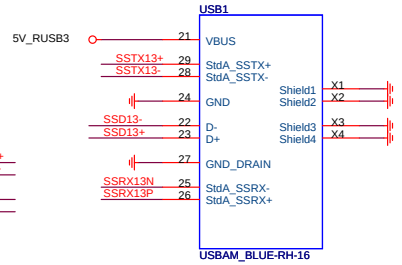


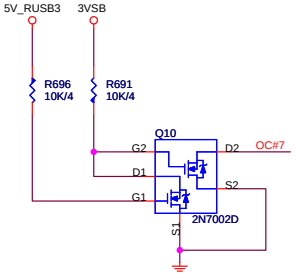
TYPE-A

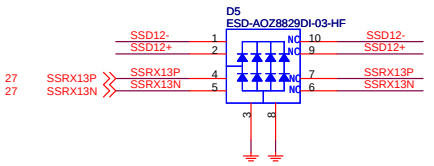


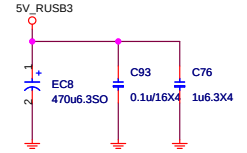




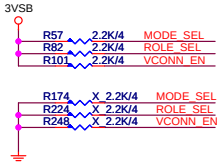








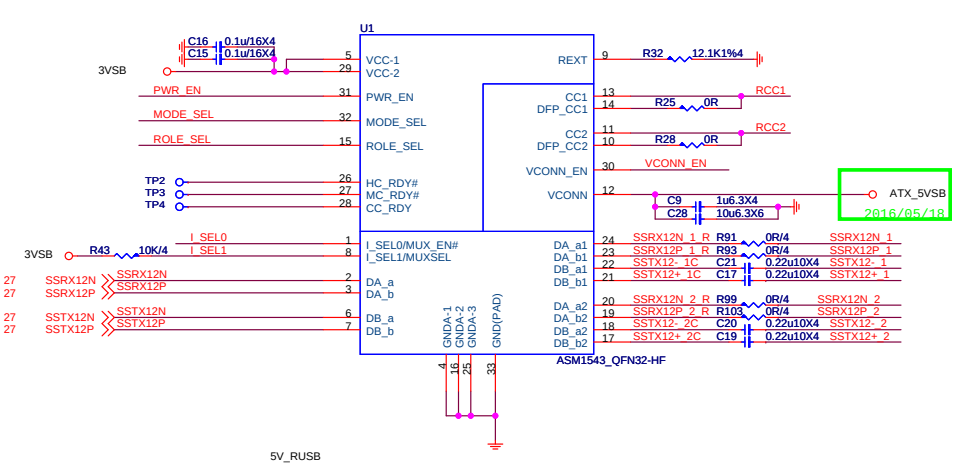
USB Type-C MUX with Configuration Channel (CC)

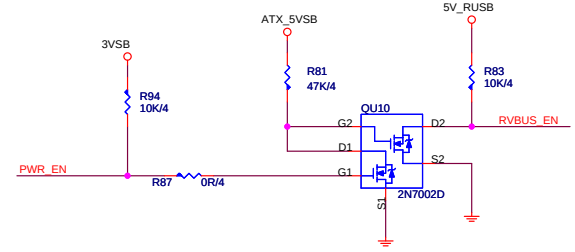


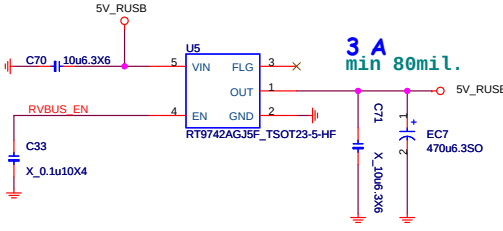
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

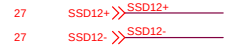
VCONN_EN	
1	enable
0	disable



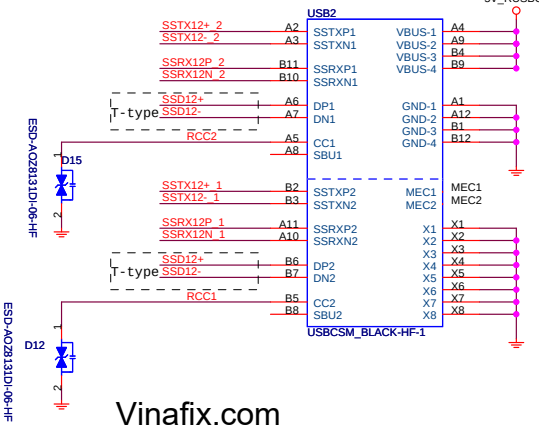




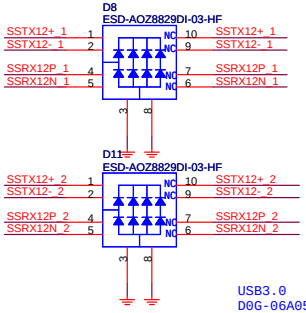
TYPE-C

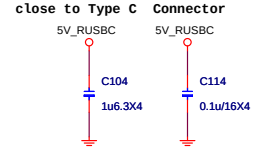


T-type 分支需小於140mils



ESD Protection
NEAR CONNECTOR





Vinafix.com

USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL

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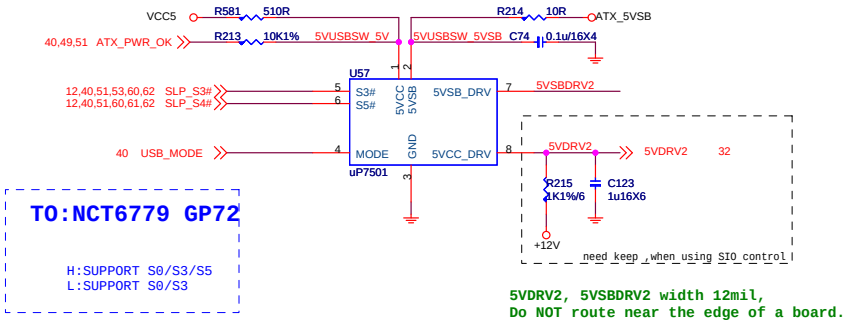
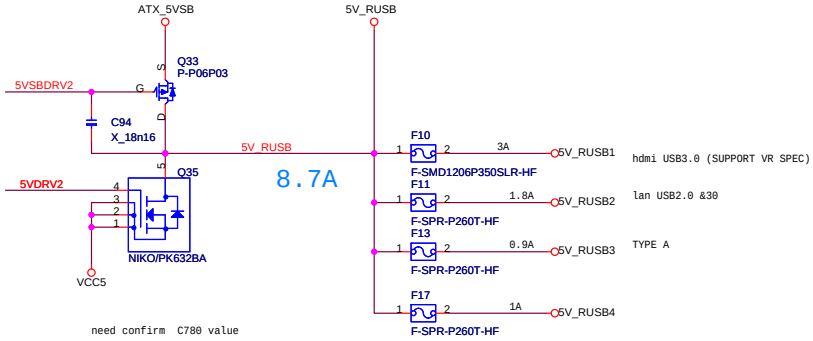
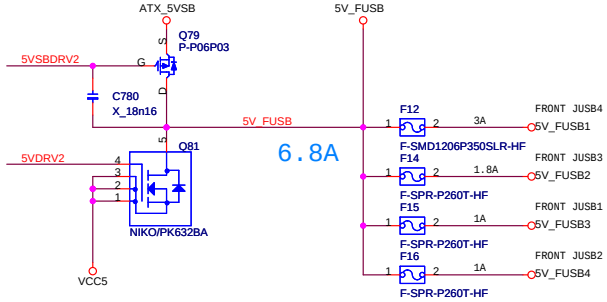
USB PORT POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.





P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)

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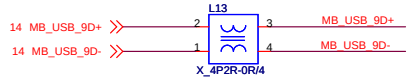
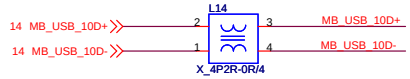
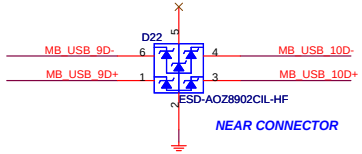
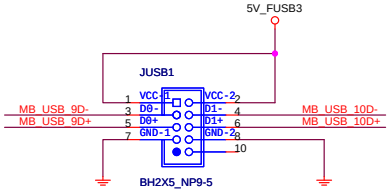


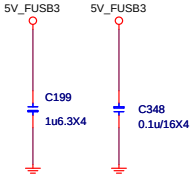


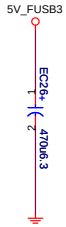


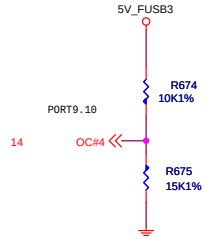
1.0A

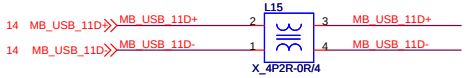


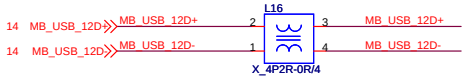
EMI Cap near Connector.

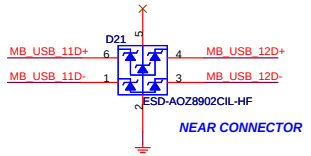




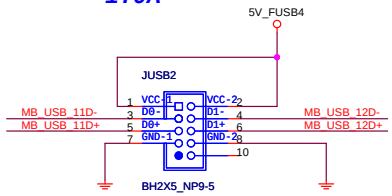




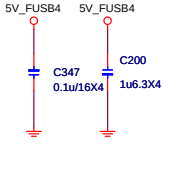


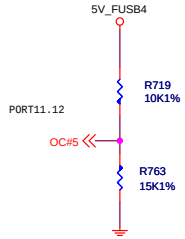


1.0A



EMI Cap near Connector.





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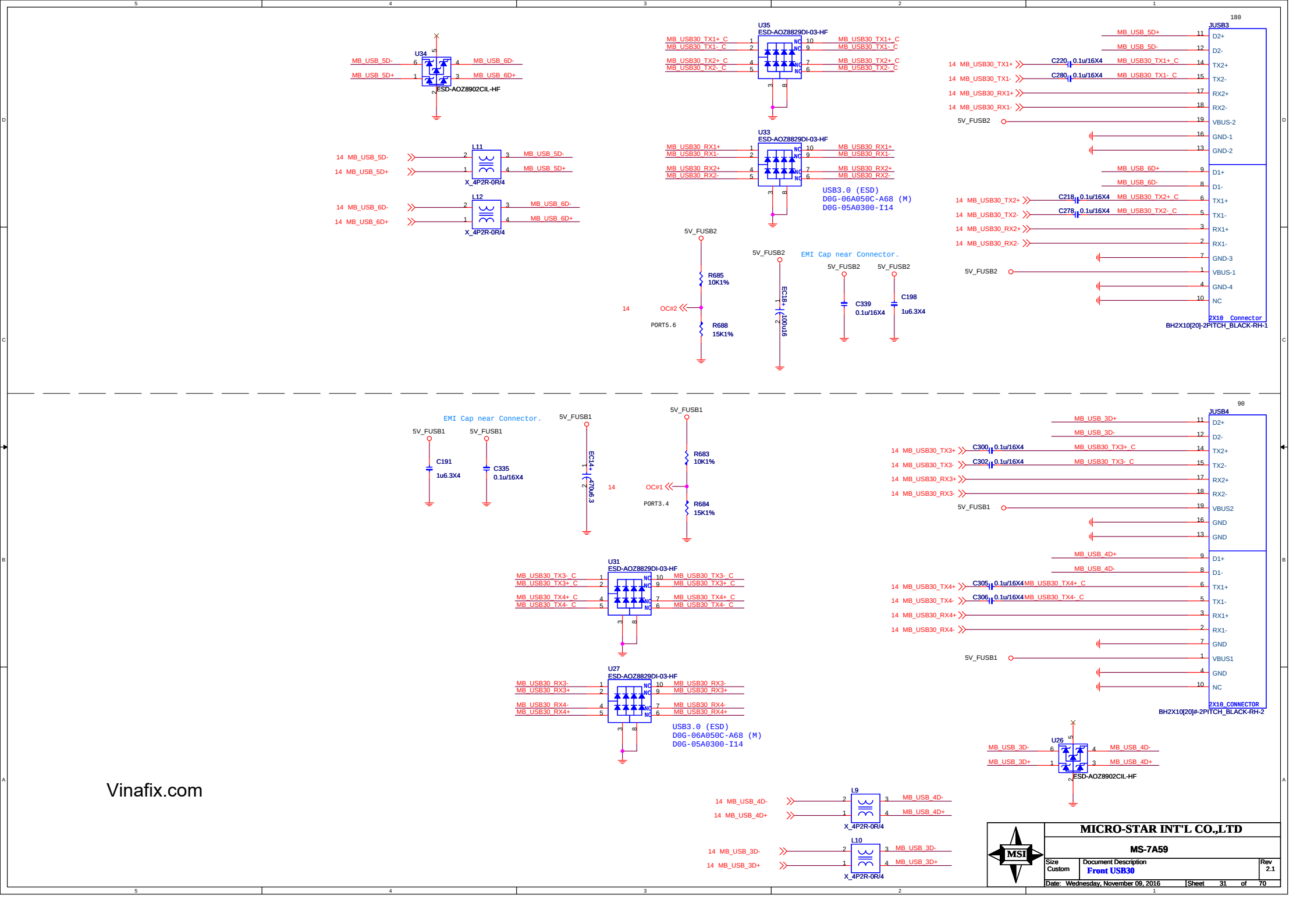
U34
MB_USB_5D-
MB_USB_5D+
MB_USB_6D-
MB_USB_6D+
ESD-AOZ8902CIL-HF
L11
14 MB_USB_5D-
14 MB_USB_5D+
X_4P2R-0R/4
L12
14 MB_USB_6D-
14 MB_USB_6D+
X_4P2R-0R/4
U35
ESD-AOZ8829DI-03-HF
MB_USB30_TX1+_C
MB_USB30_TX1-_C
MB_USB30_TX2+_C
MB_USB30_TX2-_C
U33
ESD-AOZ8829DI-03-HF
MB_USB30_RX1+
MB_USB30_RX1-
MB_USB30_RX2+
MB_USB30_RX2-
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
5V_FUSB2
R685
10K1%
14 OC#2
PORT5.6
R688
15K1%
EC18+
470u16
EMI Cap near Connector.
C339
0.1u/16X4
C198
1u6.3X4
JUSB3
180
MB_USB_5D+
MB_USB_5D-
C220 0.1u/16X4
C280 0.1u/16X4
MB_USB30_TX1+_C
MB_USB30_TX1-_C
MB_USB_6D+
MB_USB_6D-
C218 0.1u/16X4
C278 0.1u/16X4
MB_USB30_TX2+_C
MB_USB30_TX2-_C
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS-2
GND-1
GND-2
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND-3
VBUS-1
GND-4
NC
2X10 Connector
BH2X10[20]-2PITCH_BLACK-RH-1
EMI Cap near Connector.
5V_FUSB1
C191
1u6.3X4
C335
0.1u/16X4
EC14+
470u6.3
R683
10K1%
14 OC#1
PORT3.4
R684
15K1%
U31
ESD-AOZ8829DI-03-HF
MB_USB30_TX3-_C
MB_USB30_TX3+_C
MB_USB30_TX4+_C
MB_USB30_TX4-_C
U27
ESD-AOZ8829DI-03-HF
MB_USB30_RX3-
MB_USB30_RX3+
MB_USB30_RX4-
MB_USB30_RX4+
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
JUSB4
90
MB_USB_3D+
MB_USB_3D-
C300 0.1u/16X4
C302 0.1u/16X4
MB_USB30_TX3+_C
MB_USB30_TX3-_C
MB_USB_4D+
MB_USB_4D-
C305 0.1u/16X4
C306 0.1u/16X4
MB_USB30_TX4+_C
MB_USB30_TX4-_C
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND
GND
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND
VBUS1
GND
NC
2X10_CONNECTOR
BH2X10[20]#-2PITCH_BLACK-RH-2
U26
MB_USB_3D-
MB_USB_3D+
MB_USB_4D-
MB_USB_4D+
ESD-AOZ8902CIL-HF
L9
14 MB_USB_4D-
14 MB_USB_4D+
X_4P2R-0R/4
L10
14 MB_USB_3D-
14 MB_USB_3D+
X_4P2R-0R/4
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MS-7A59
Size Custom
Document Description
Front USB30
Rev 2.1
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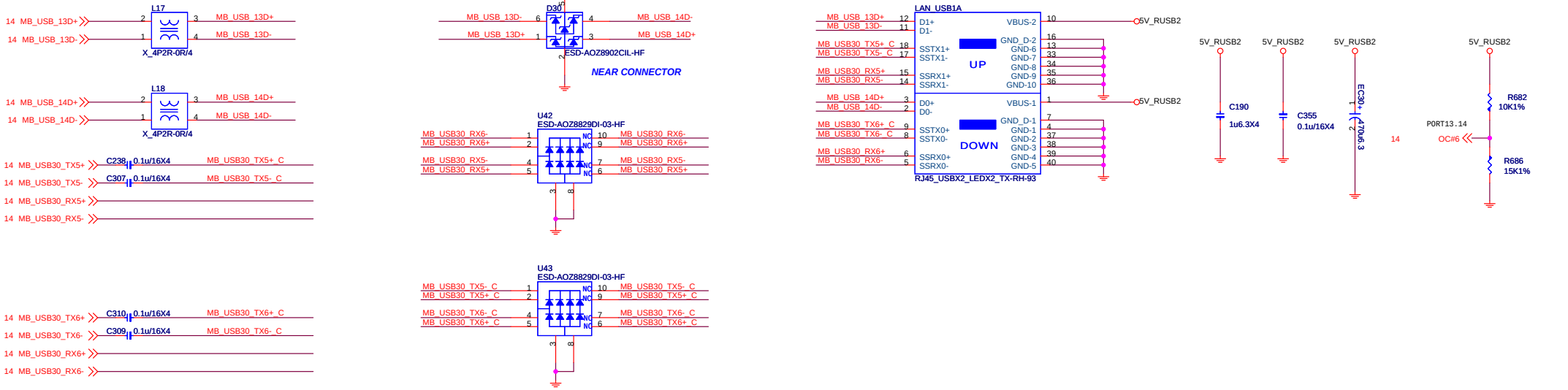
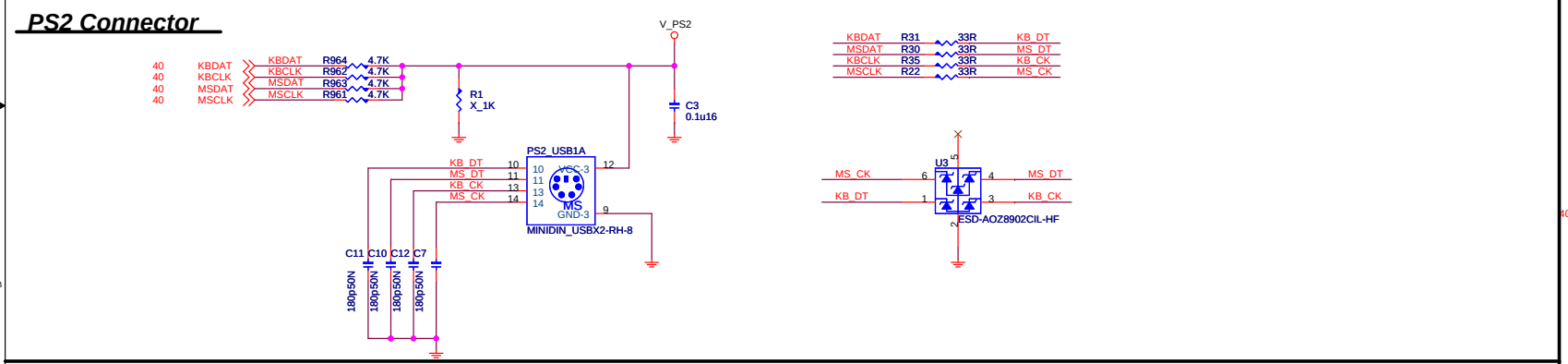
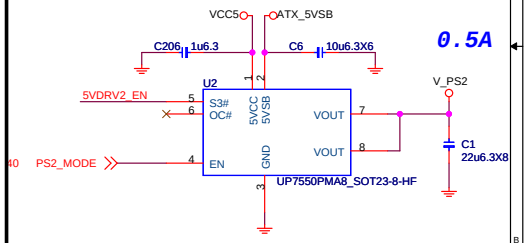
LAN USB2.0 &3.0

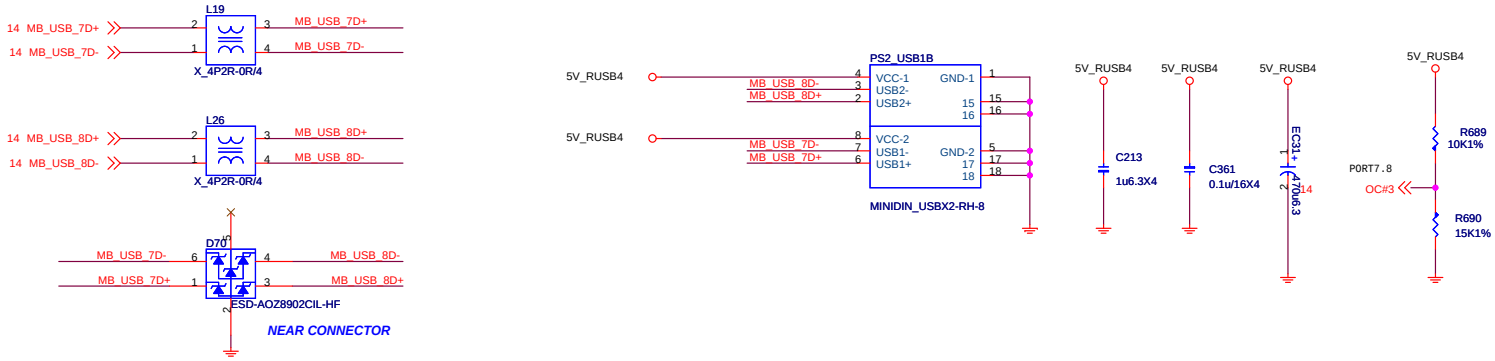


PS2 Connector

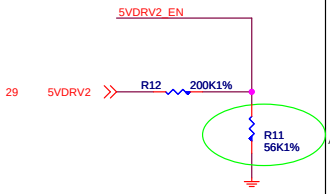


PS2 Power





USB MODE



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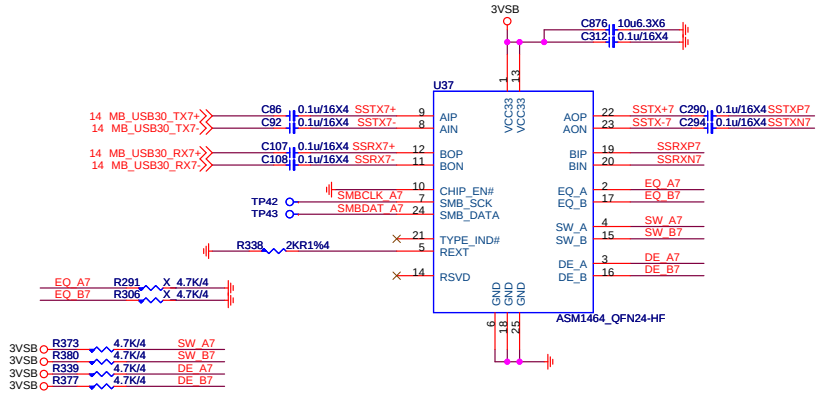
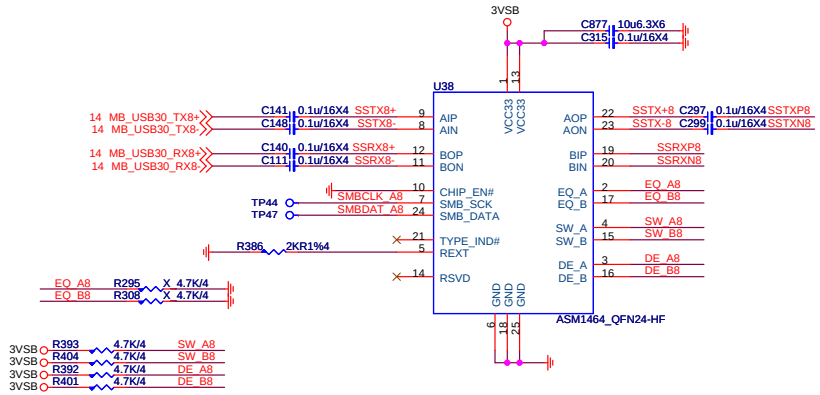
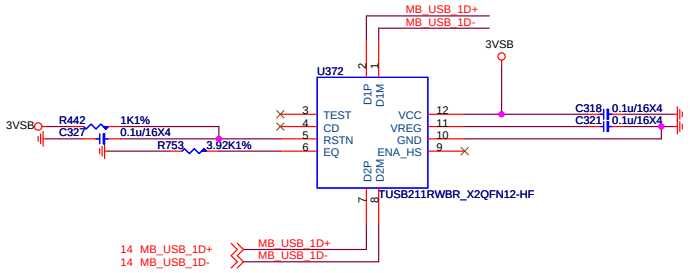
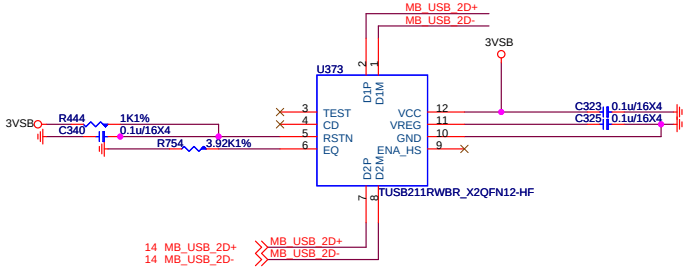
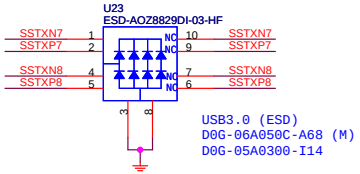
HDMI USB3.0

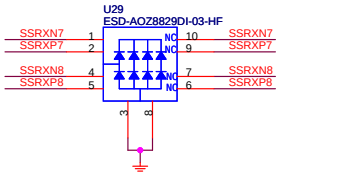


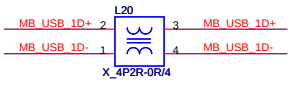


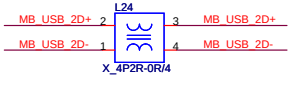


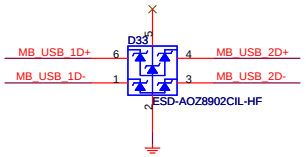


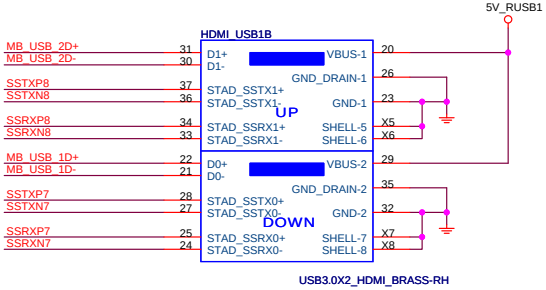


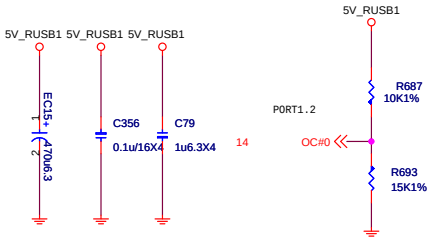












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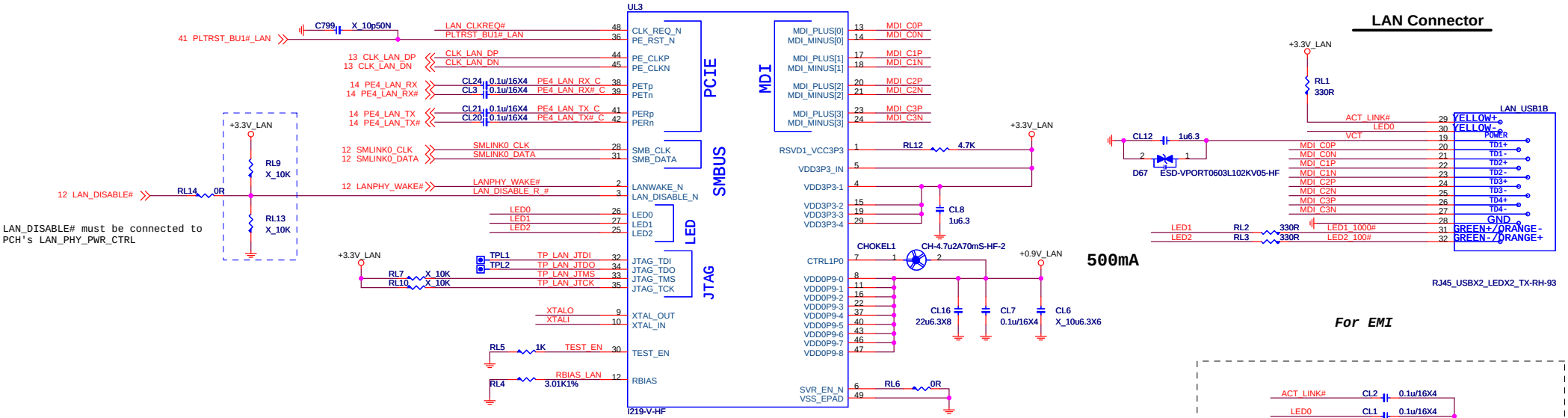
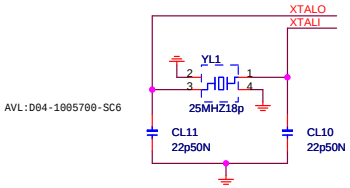
Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



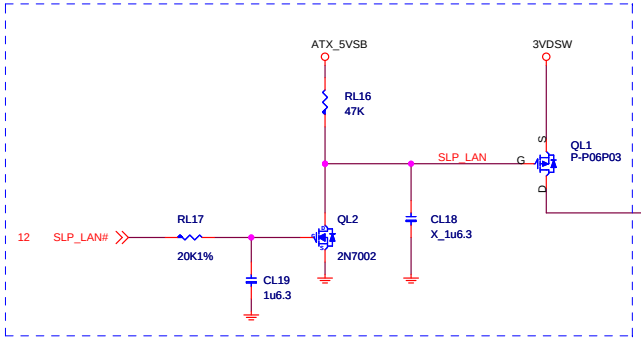
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N
is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well
of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



+3.3V_LAN
I218:132mA
I219:542mW

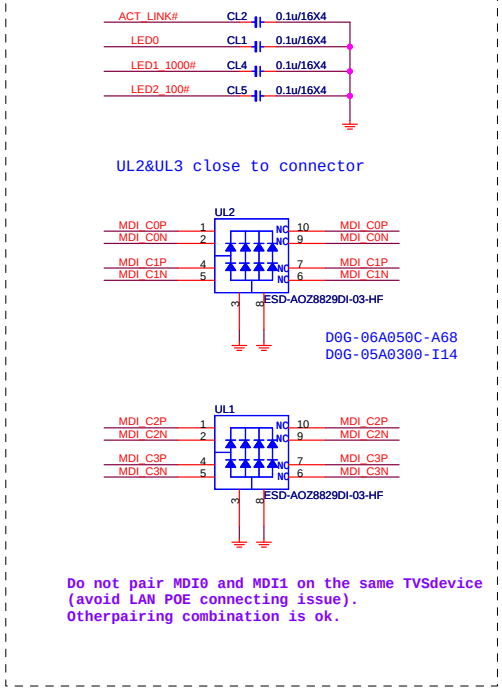
Note:These caps closed to PHY

LAN Connector

RJ45_USBX2_LEDX2_TX-RH-93

500mA

For EMI



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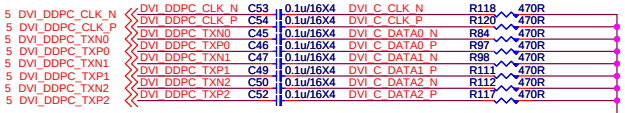
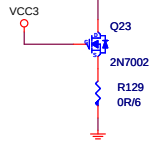
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)





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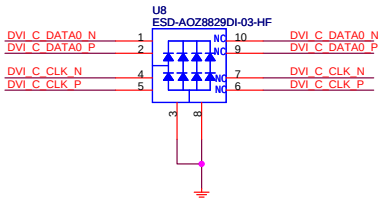
D0G-06A050C-A68



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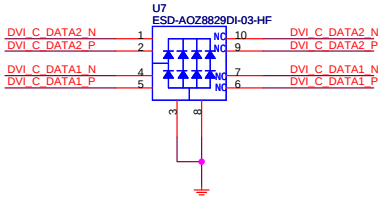

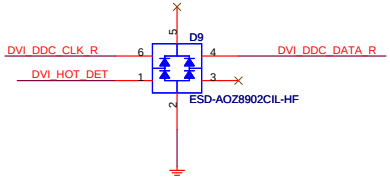

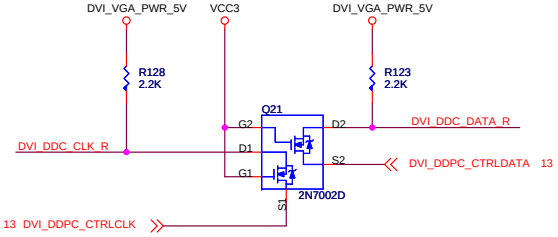

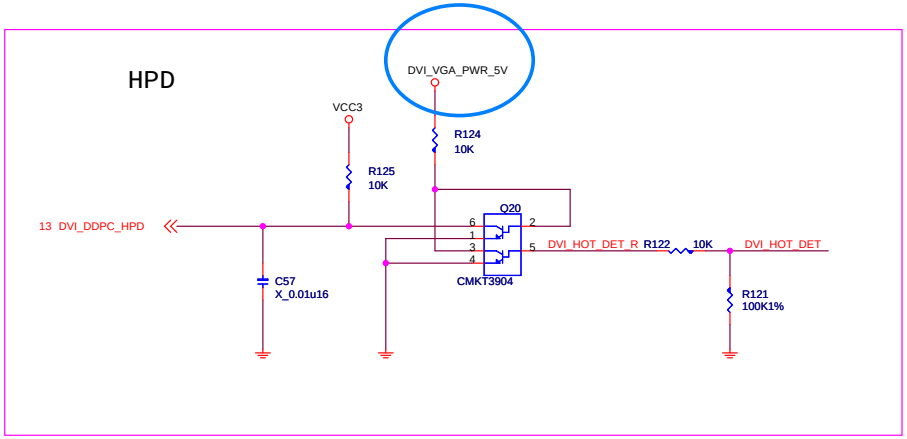

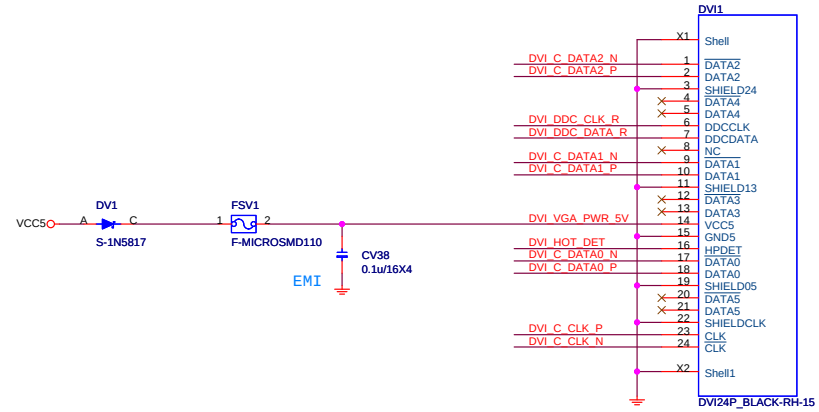

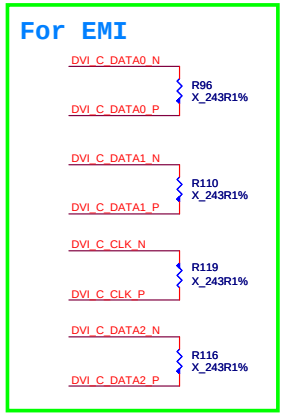

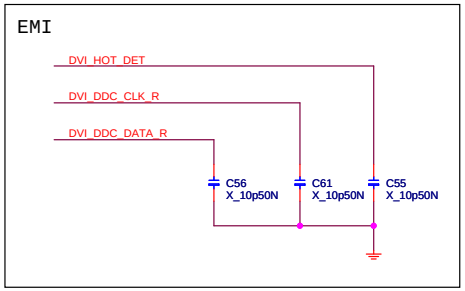

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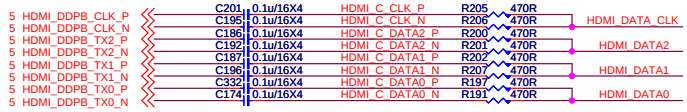
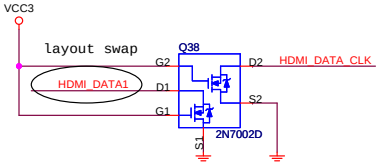
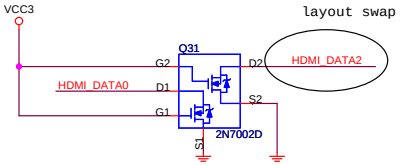
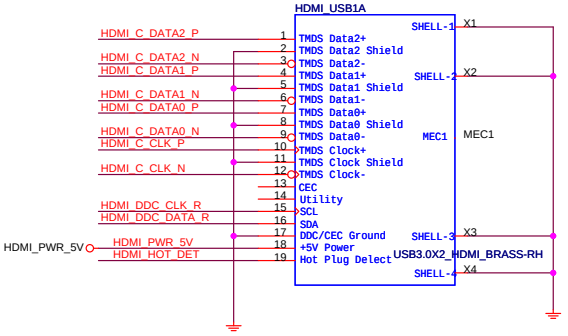
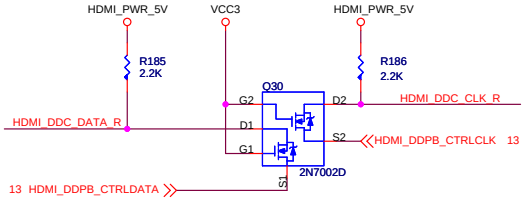
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

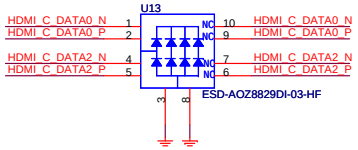


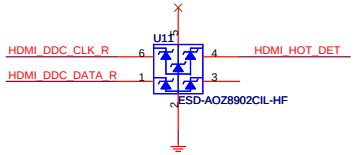


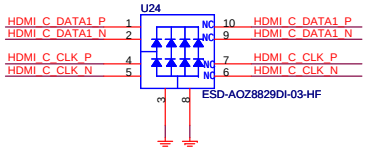


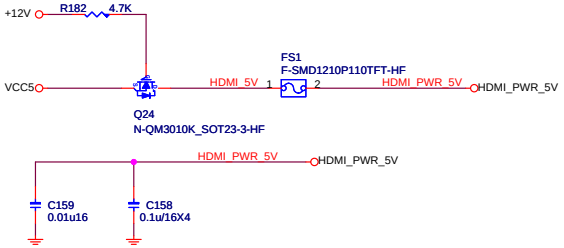






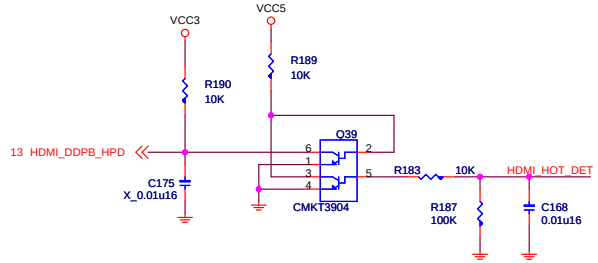




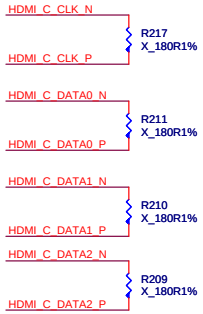


Vinafix.com

HPD



For EMI



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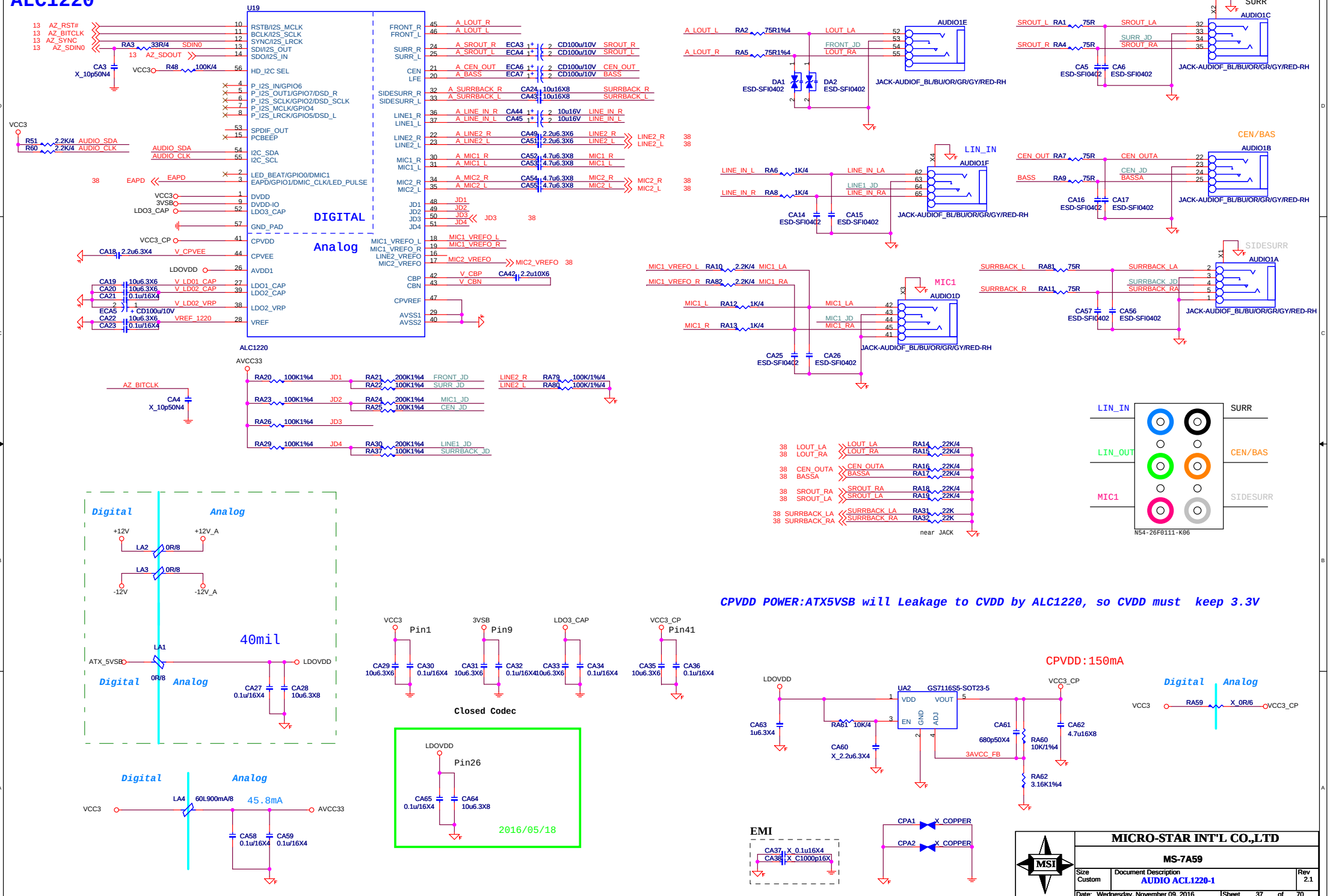
ALC1220


U19
DIGITAL
Analog
ALC1220
AUDIO1E
AUDIO1C
AUDIO1F
AUDIO1B
AUDIO1D
AUDIO1A
JACK-AUDIOF_BL/BU/OR/GR/GY/RED-RH
SURR
CEN/BAS
LIN_IN
SIDESURR
MIC1
LIN_IN
LIN_OUT
MIC1
SURR
CEN/BAS
SIDESURR
N54-26F0111-K06
near JACK
Digital
Analog
40mil
Pin1
Pin9
Pin41
Pin26
Closed Codec
2016/05/18
CPVDD:150mA
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V
EMI
MICRO-STAR INT'L CO.,LTD
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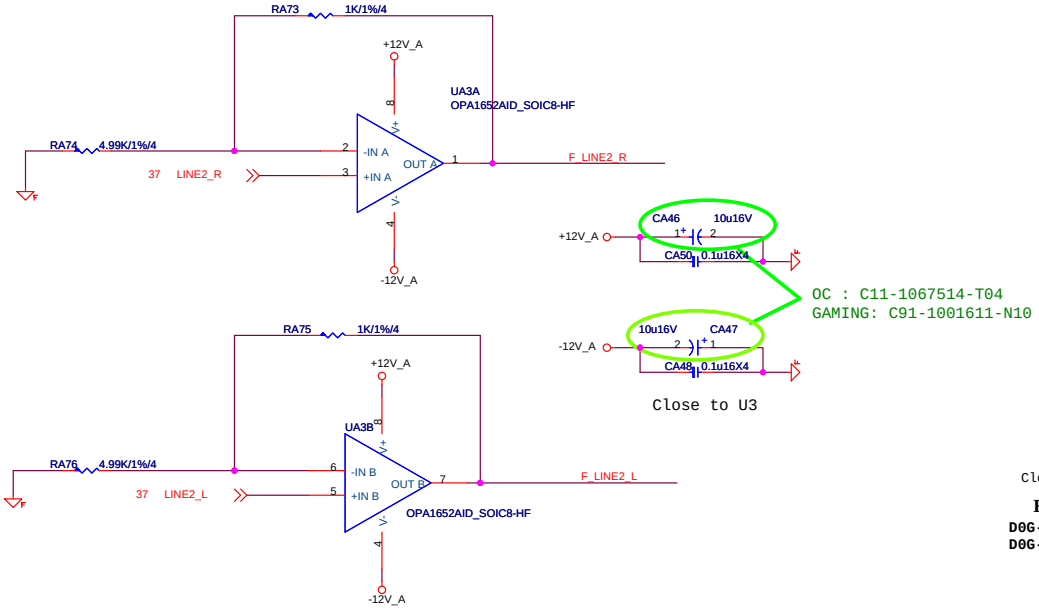
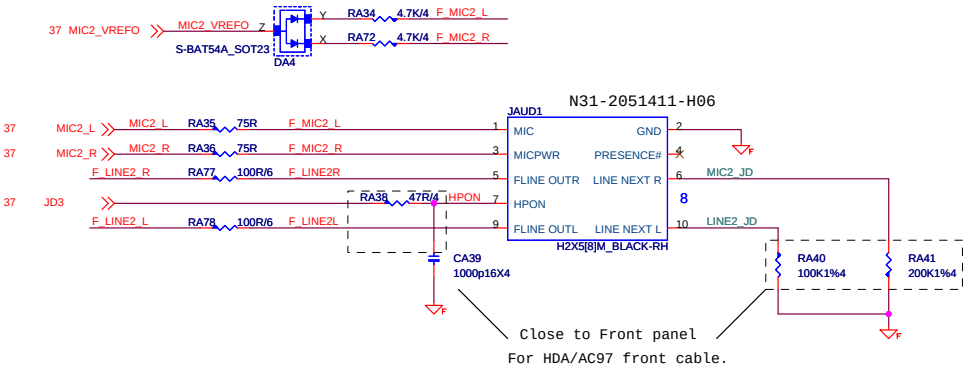
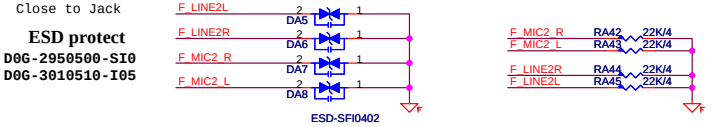
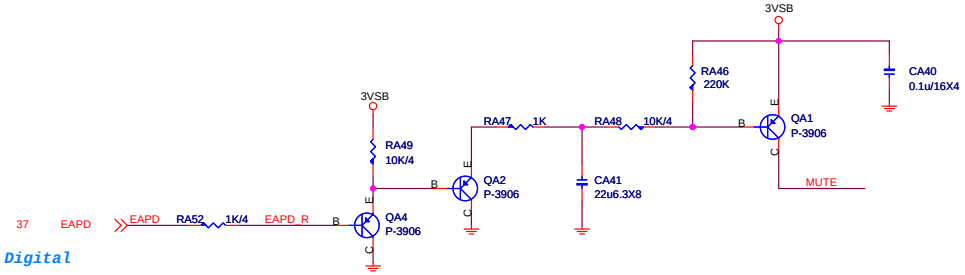




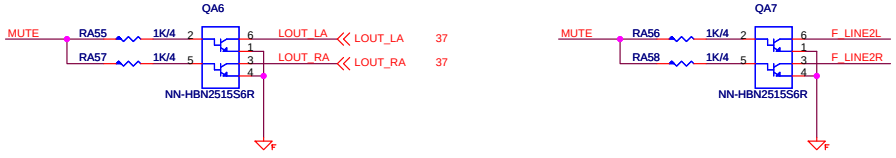


Rear Line OUT De-POP circuit

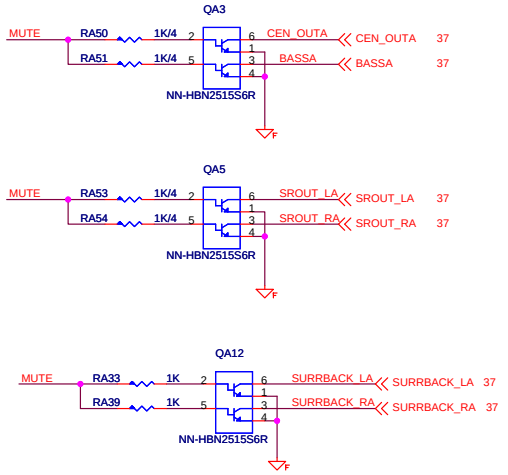
(De-pop circuit for Rear Line out & Front Headphone out)



Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



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Size: Custom	Document Description: AUDIO ACL1220-2	Rev: 2.1
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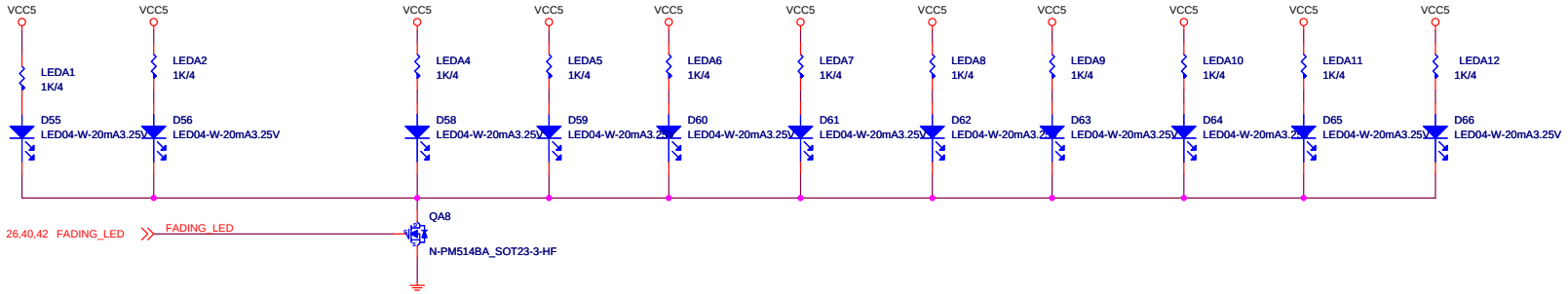
Audio moat is transparent and width 40mil



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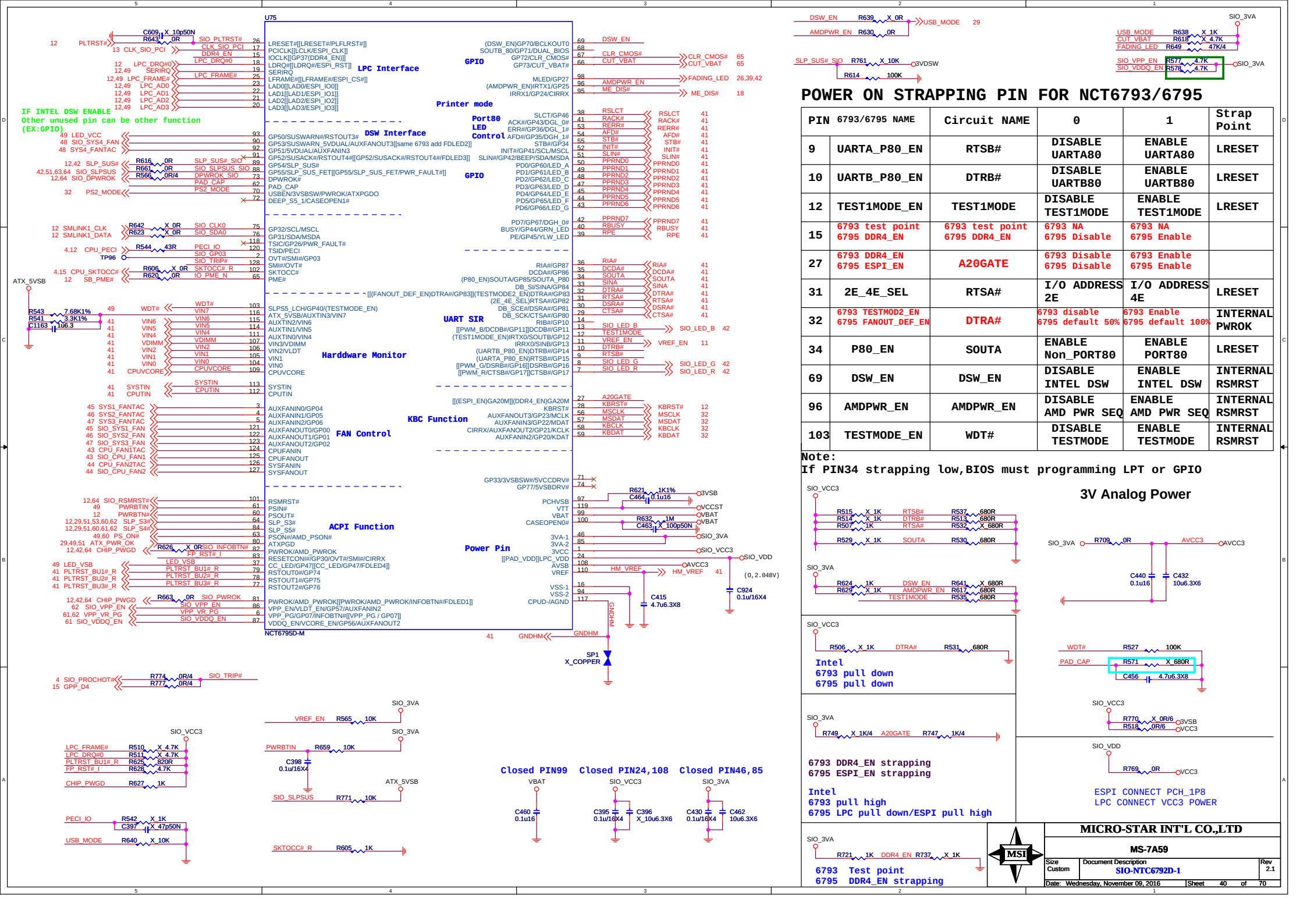
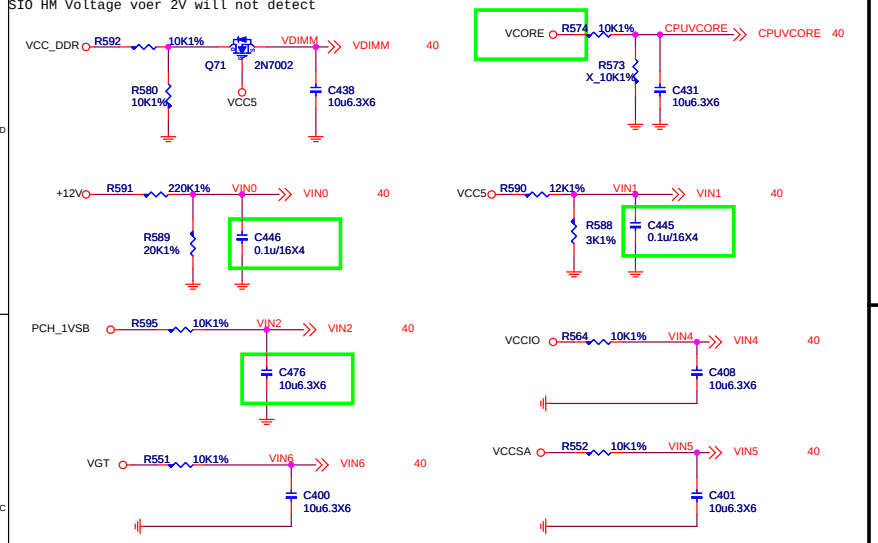


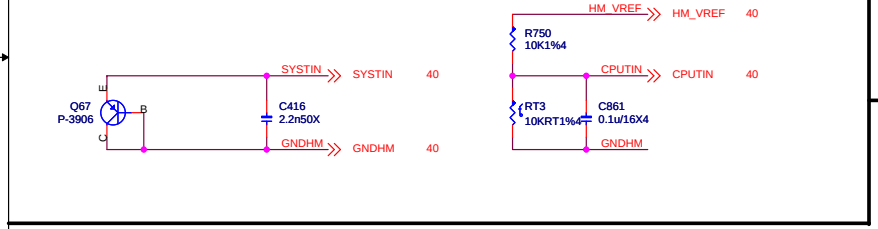
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

HW Monitor - Voltage

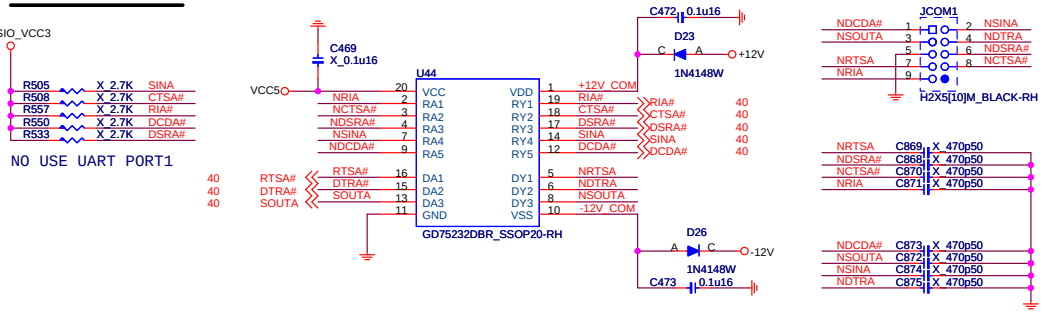
SIO HM Voltage voer 2V will not detect



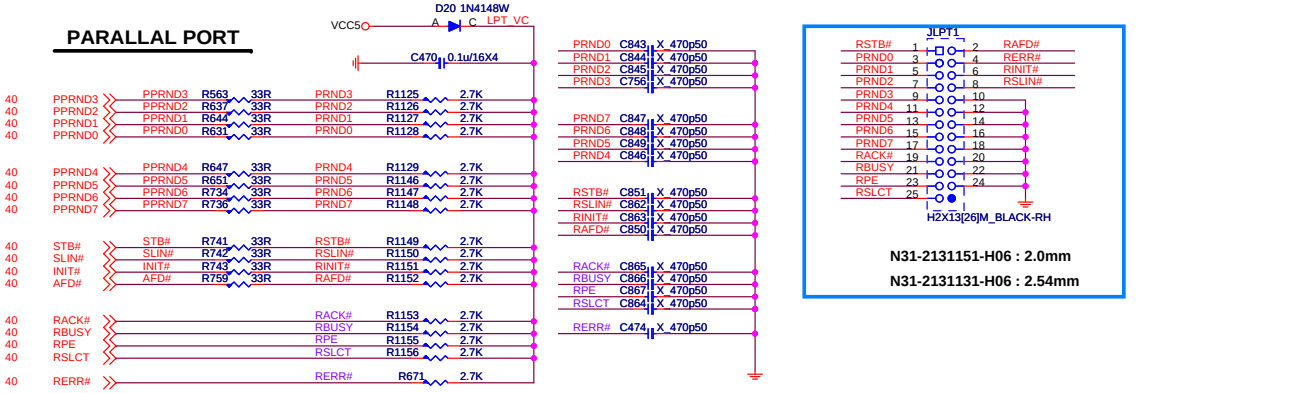
Thermal Monitor

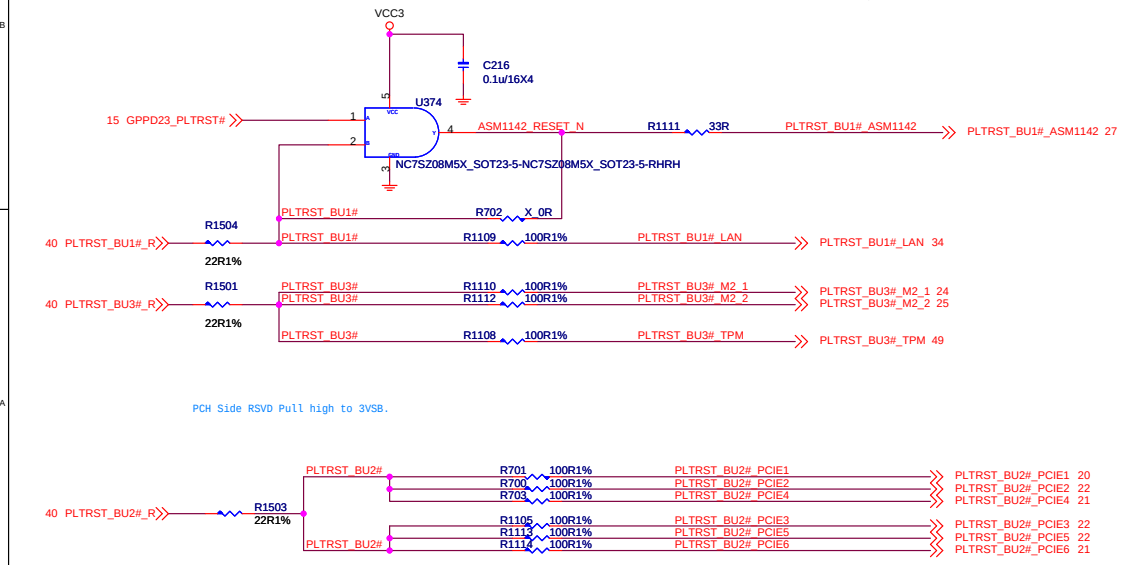


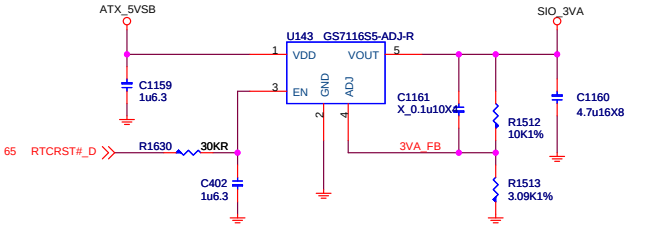
SERIAL PORT 1



PARALLAL PORT







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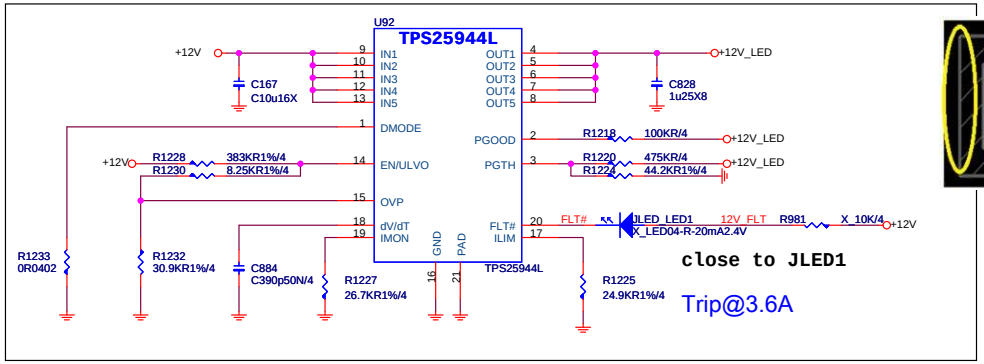
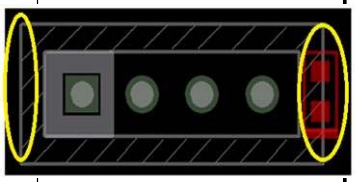
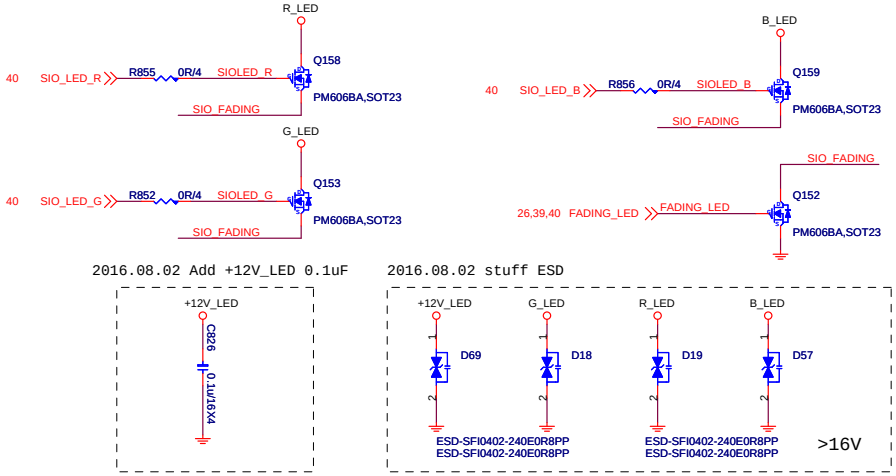
LED Control by SIO

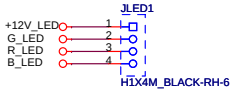
2016.07.06 Use TPS25944L



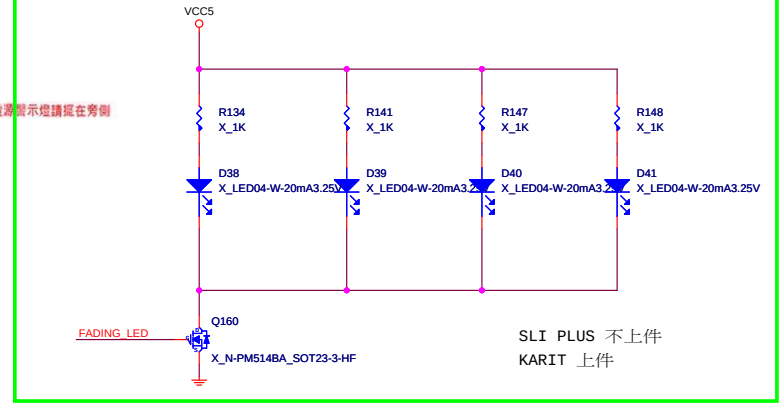


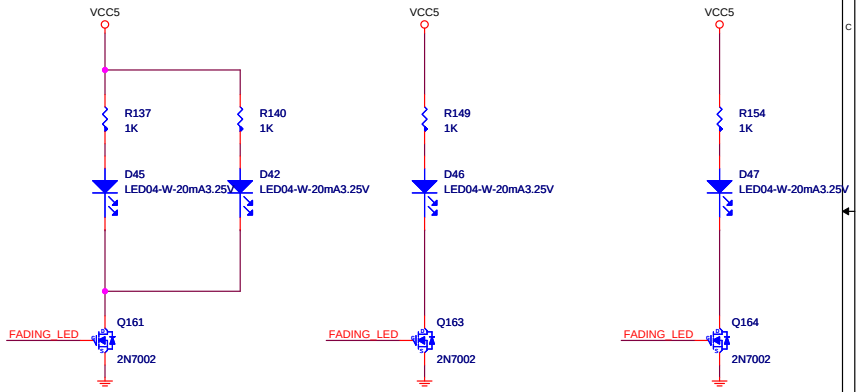
JLED1电源显示燈請擺在旁側



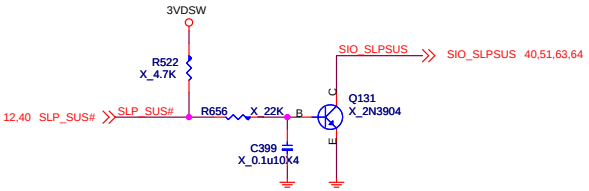


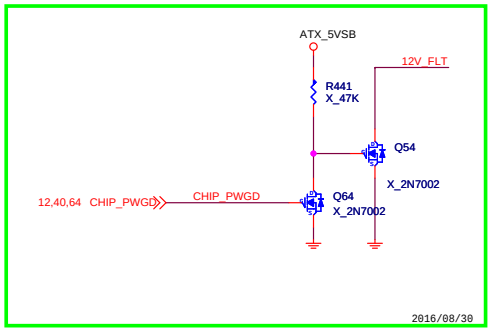
PCH LED

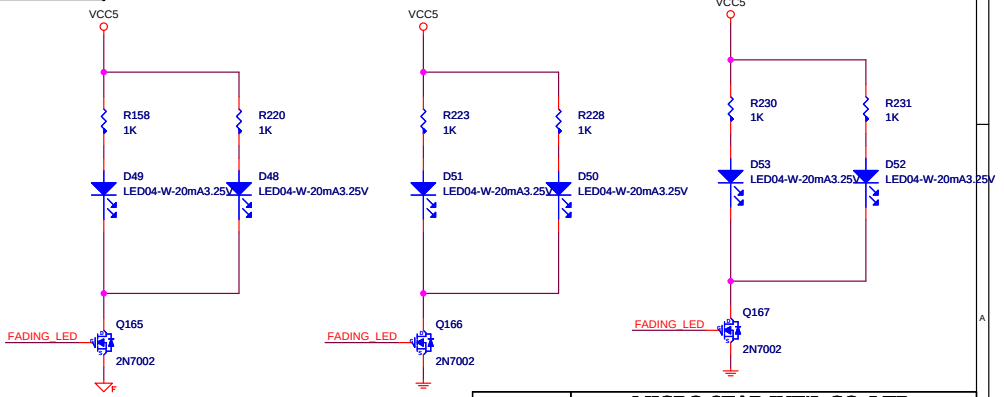




SLP_SUS Co-lay circuit







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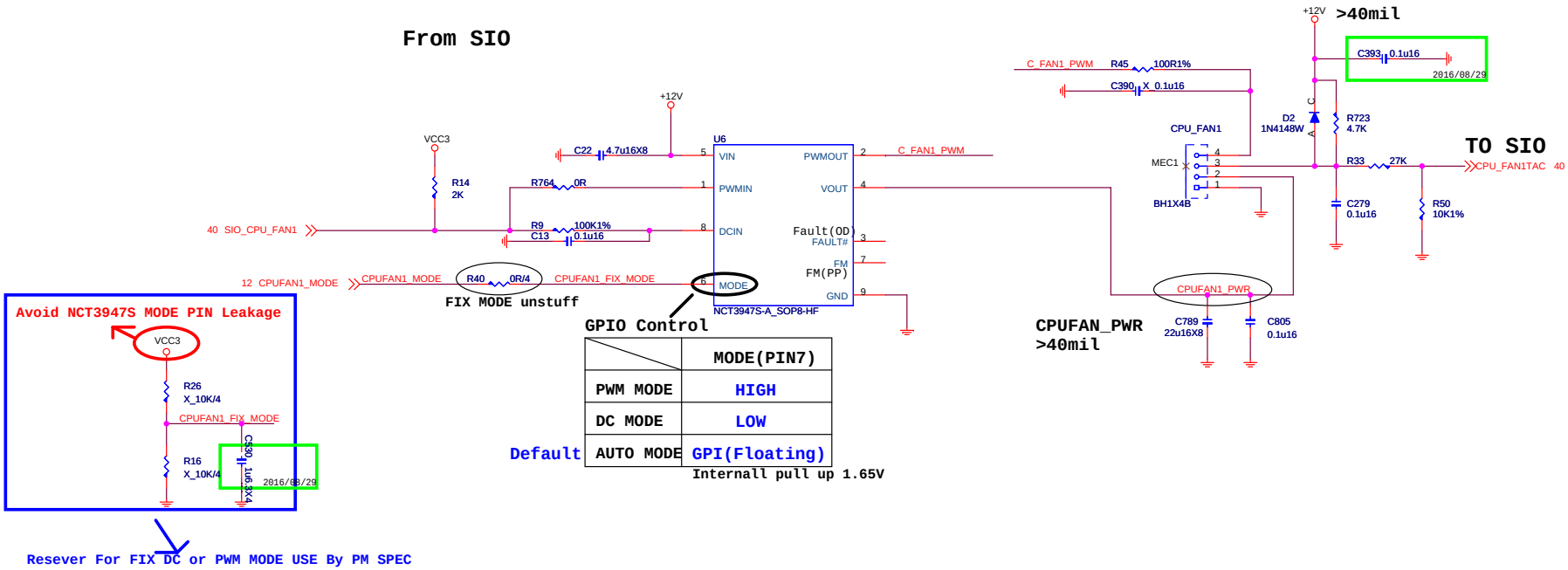

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

Vinafix.com

1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

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Size	Document Description	Rev
Custom	CPU FAN1	2.1

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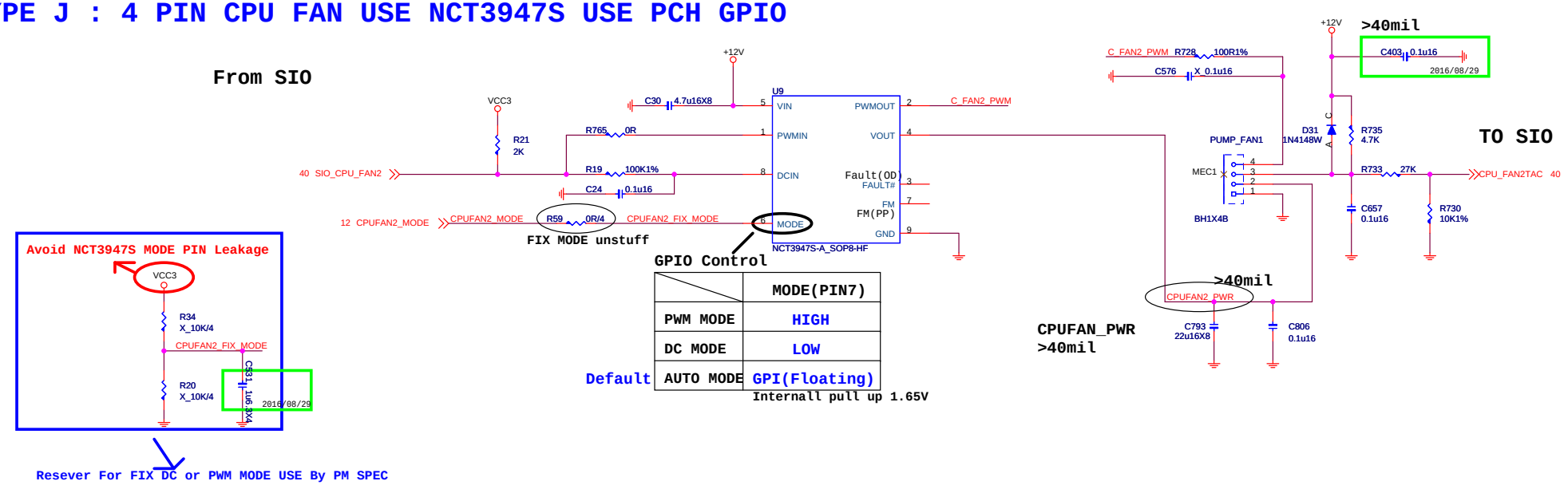
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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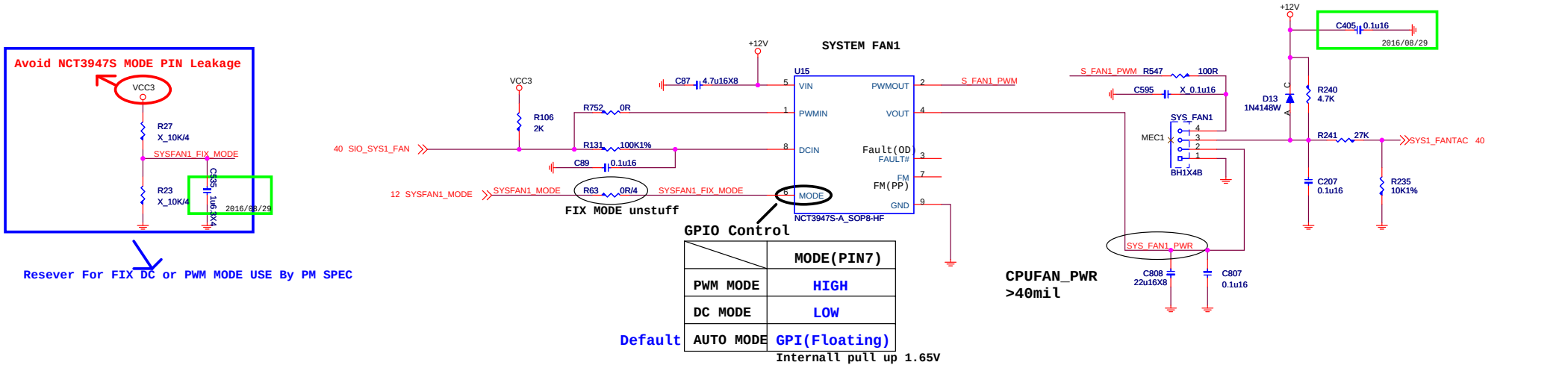

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SYSTEM FAN1	2.1

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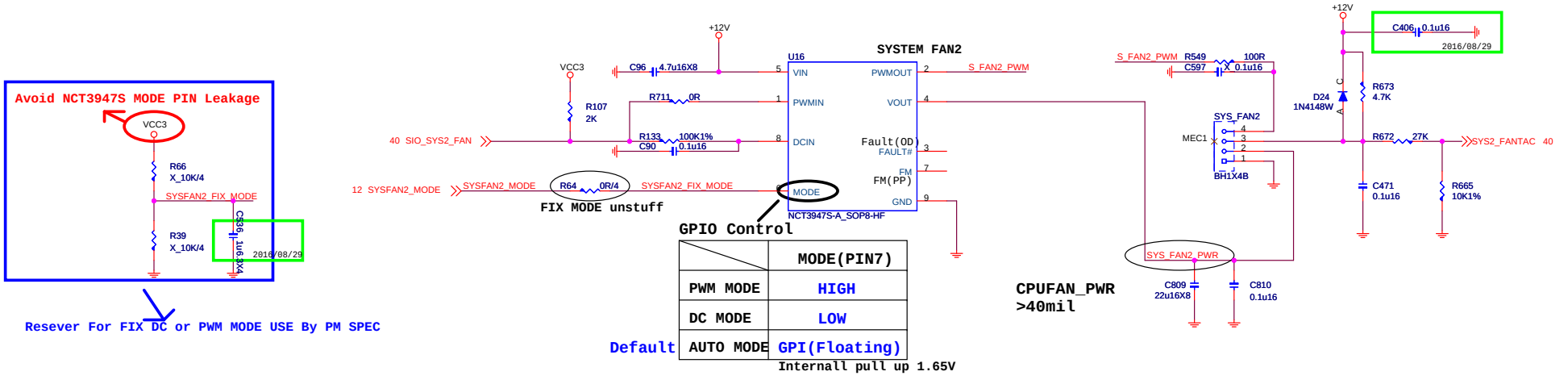

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Size: Custom	Document Description: SYSTEM FAN2	Rev: 2.1
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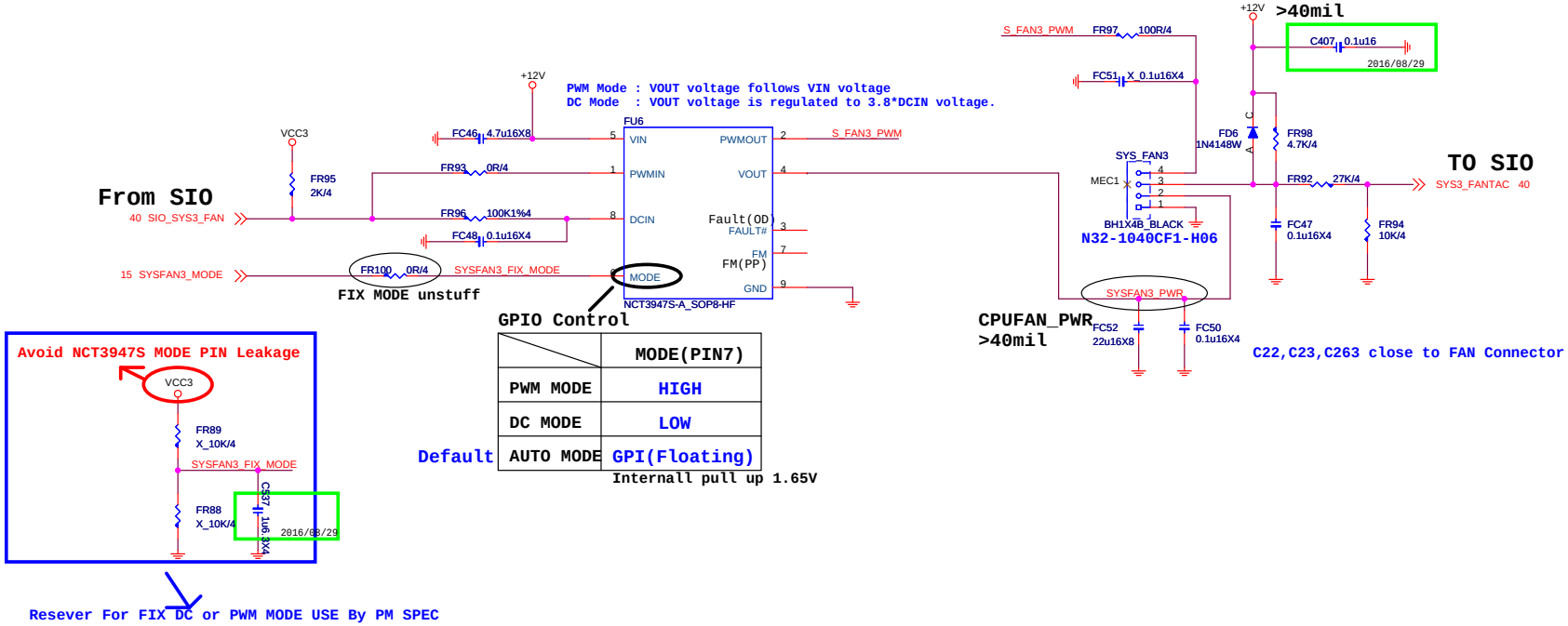
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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Size	Document Description	Rev
Custom	SYSTEM FAN3	2.1

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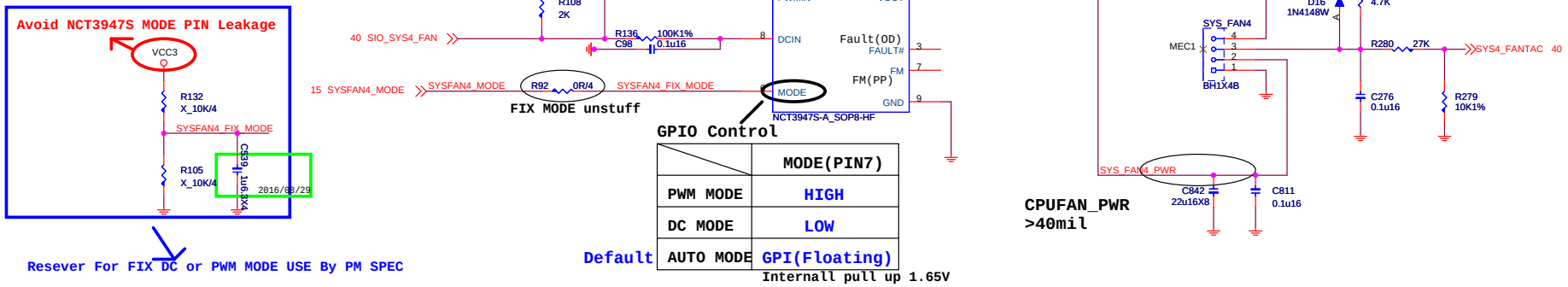
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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Custom	SYSTEM FAN4	2.1

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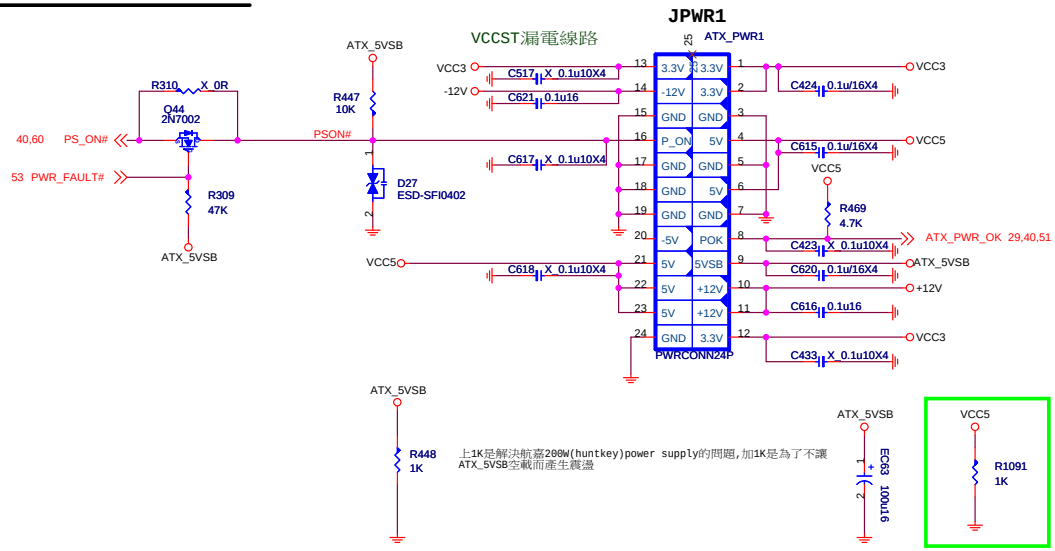
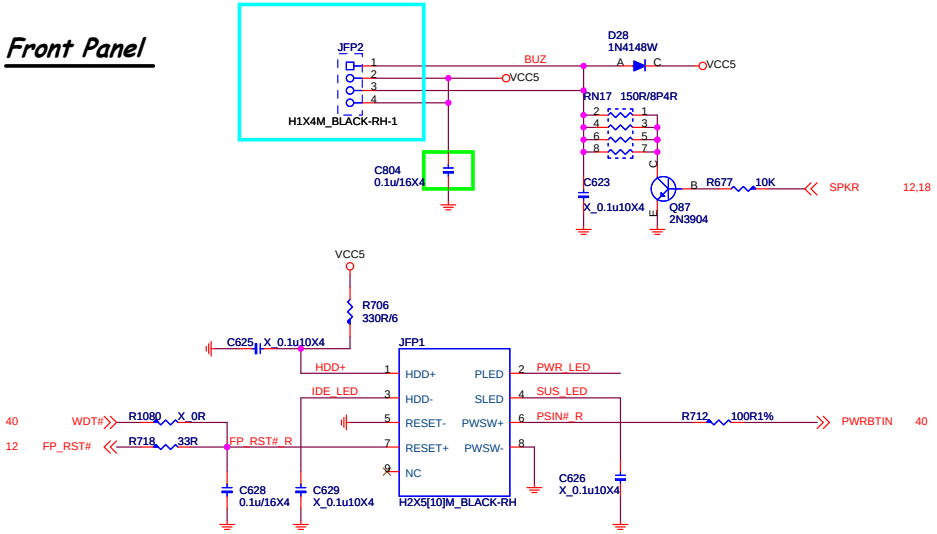
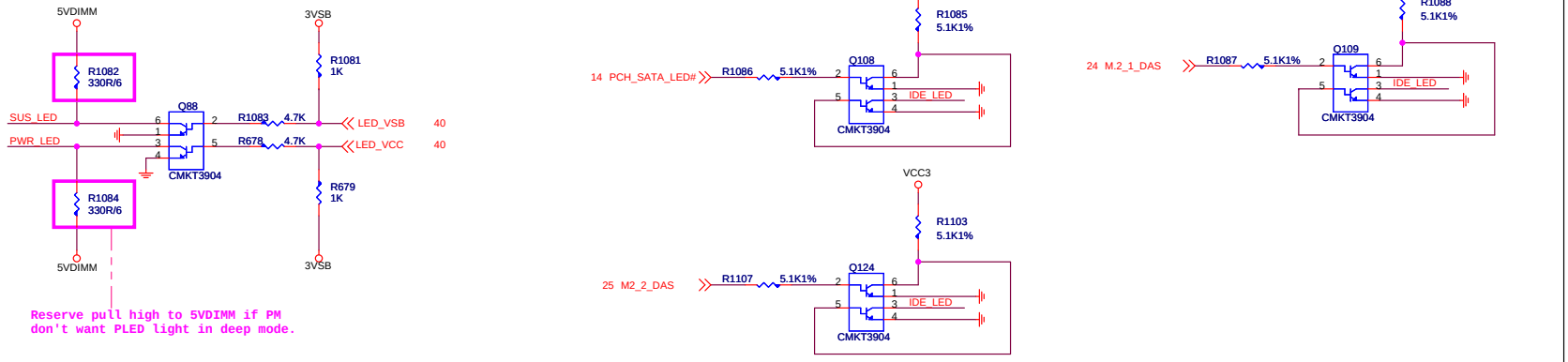
ATX POWER CONNECTOR

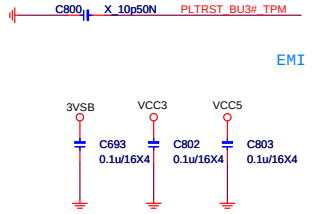


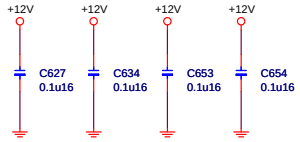
Front Panel



LED

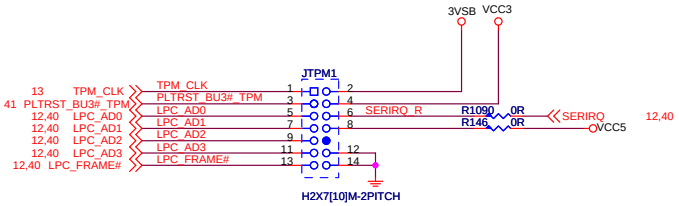






TPM

Confirm ESPI TPM card and TPM card pin difine
(Not ready)



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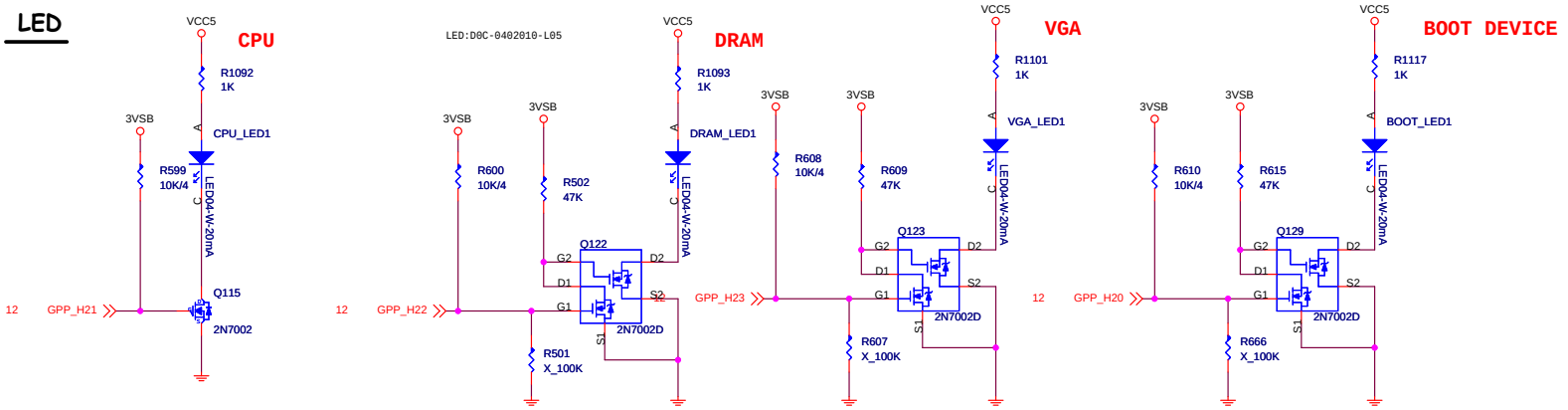
LED



KRAIT GAMING LED >>WHITE:D0C-040S200-E07

關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。
   （系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

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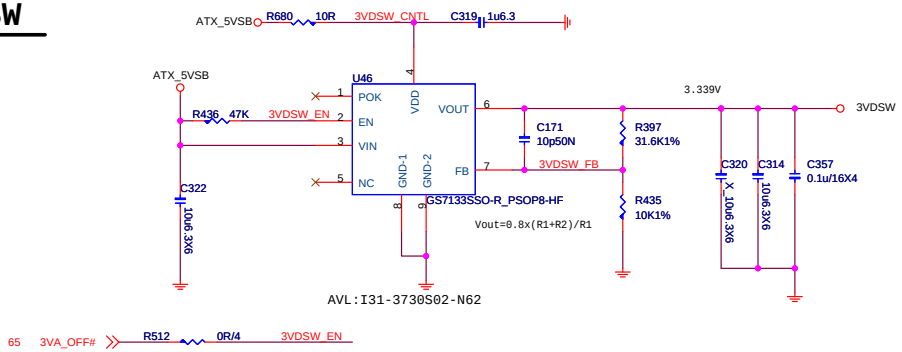
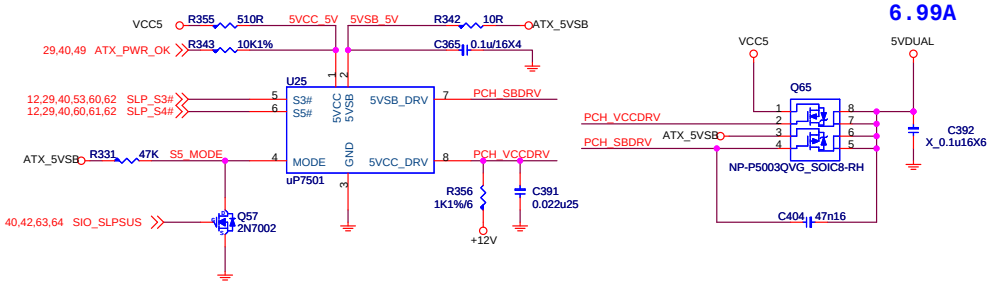
3VDSW

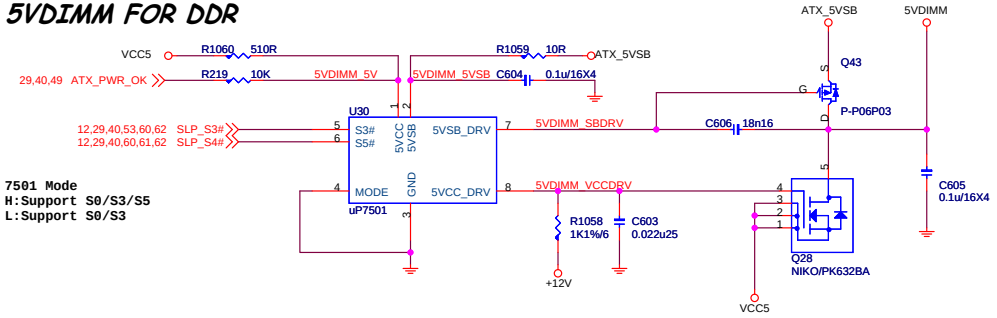


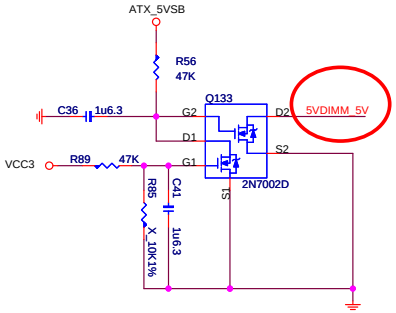
5VDUAL

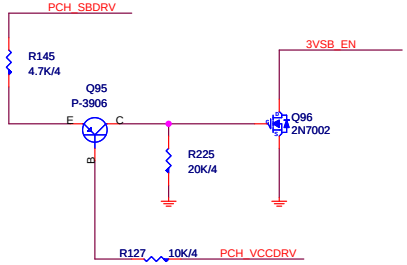
5VDUAL is power source of 1P0SB



5VDIMM FOR DDR

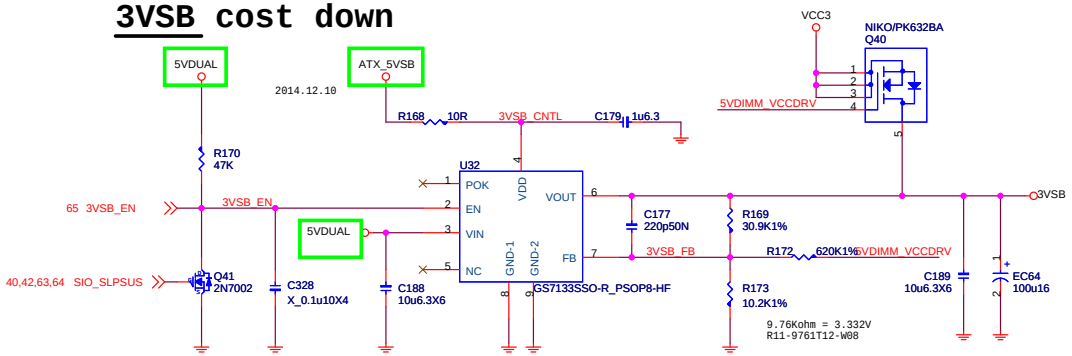






防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

3VSB cost down



AVL:I31-3730S02-N62 2014.10.15 update

VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

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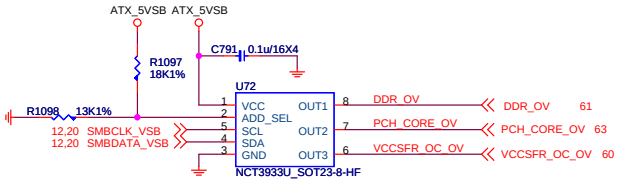
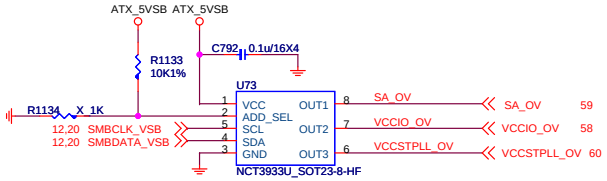
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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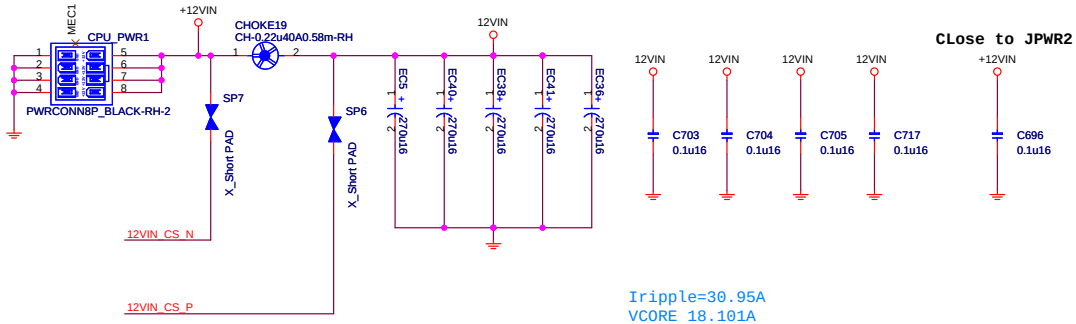
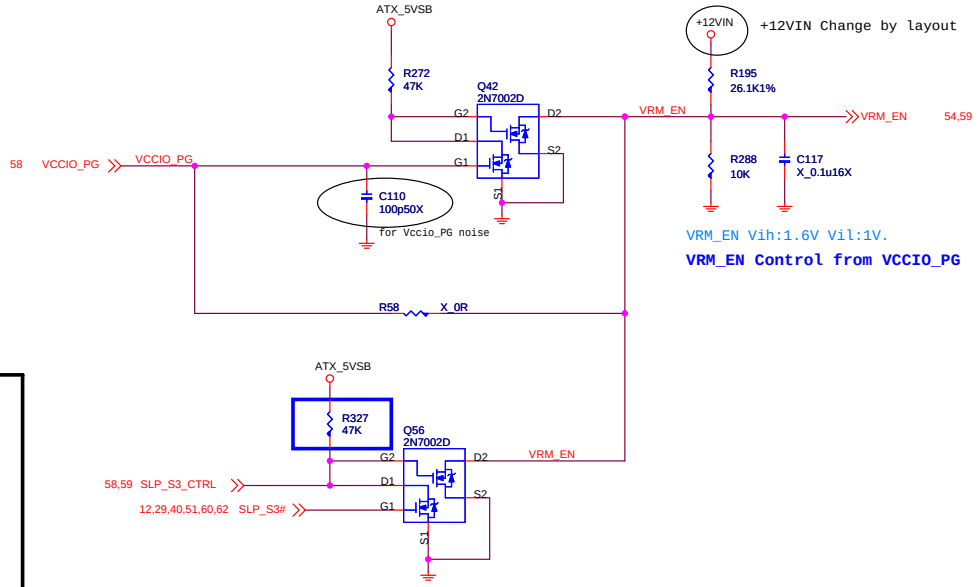


CLose to JPWR2

Iripple=30.95A
VCORE 18.101A
VGT 8.457A
VCCSA 4.392A

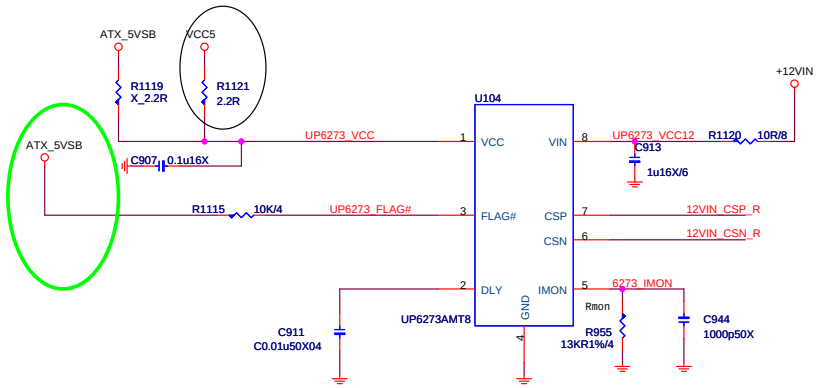
VRM_EN Control from VCCIO_PG



VRM_EN Vih:1.6V Vil:1V.

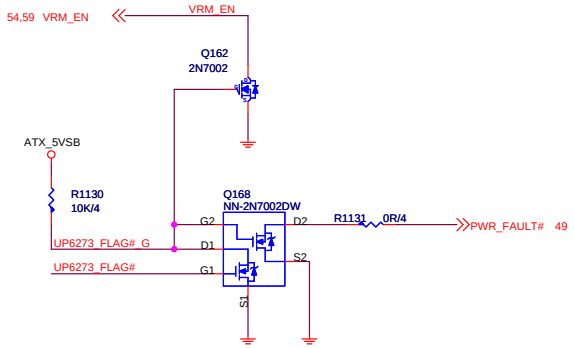
VRM_EN Control from VCCIO_PG

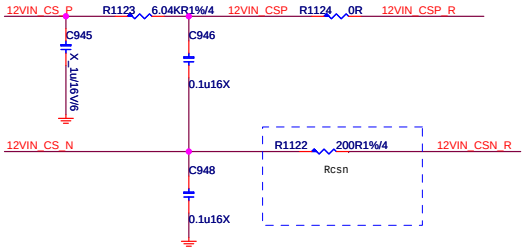
POWER METER
OCP: 32A



Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon

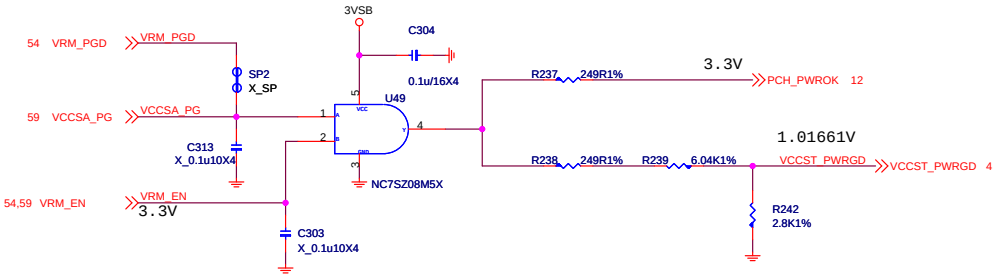
(1.2 * 0.2) / (10K* 0.3m) = 80A





PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PGD

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



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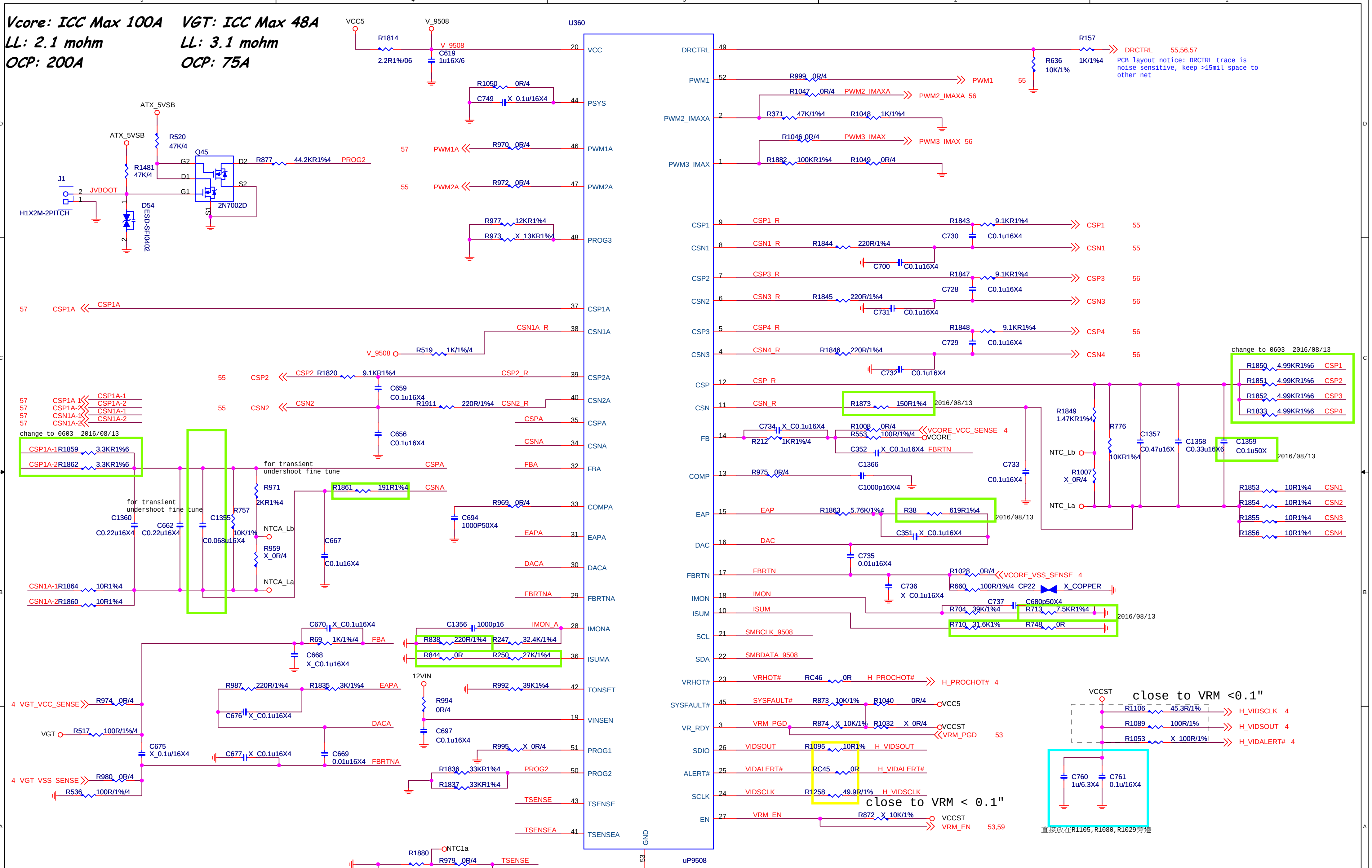

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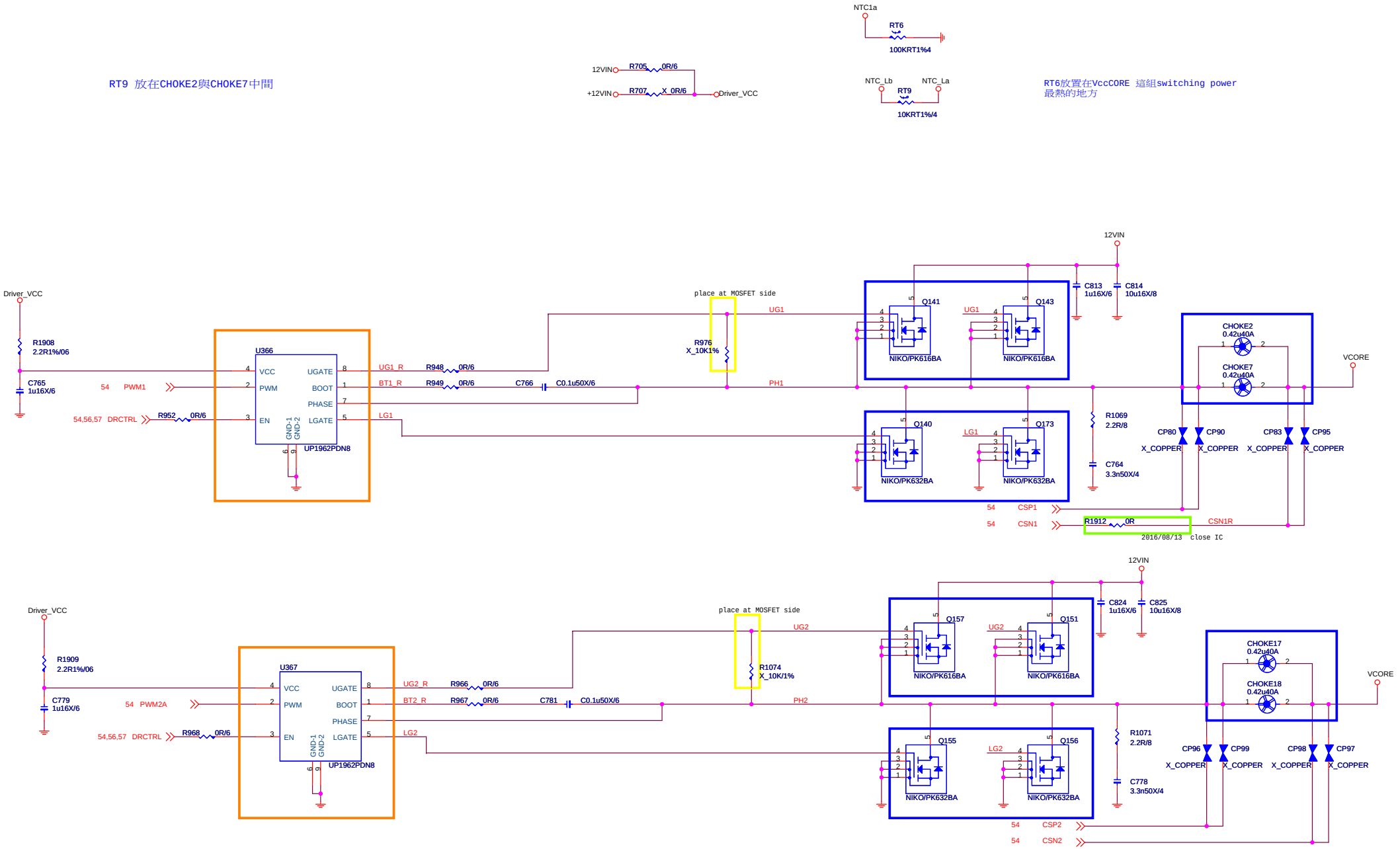
RT9 放在CHOKE2與CHOKE7中間

RT6放置在VccCORE 這組switching power 最熱的地方



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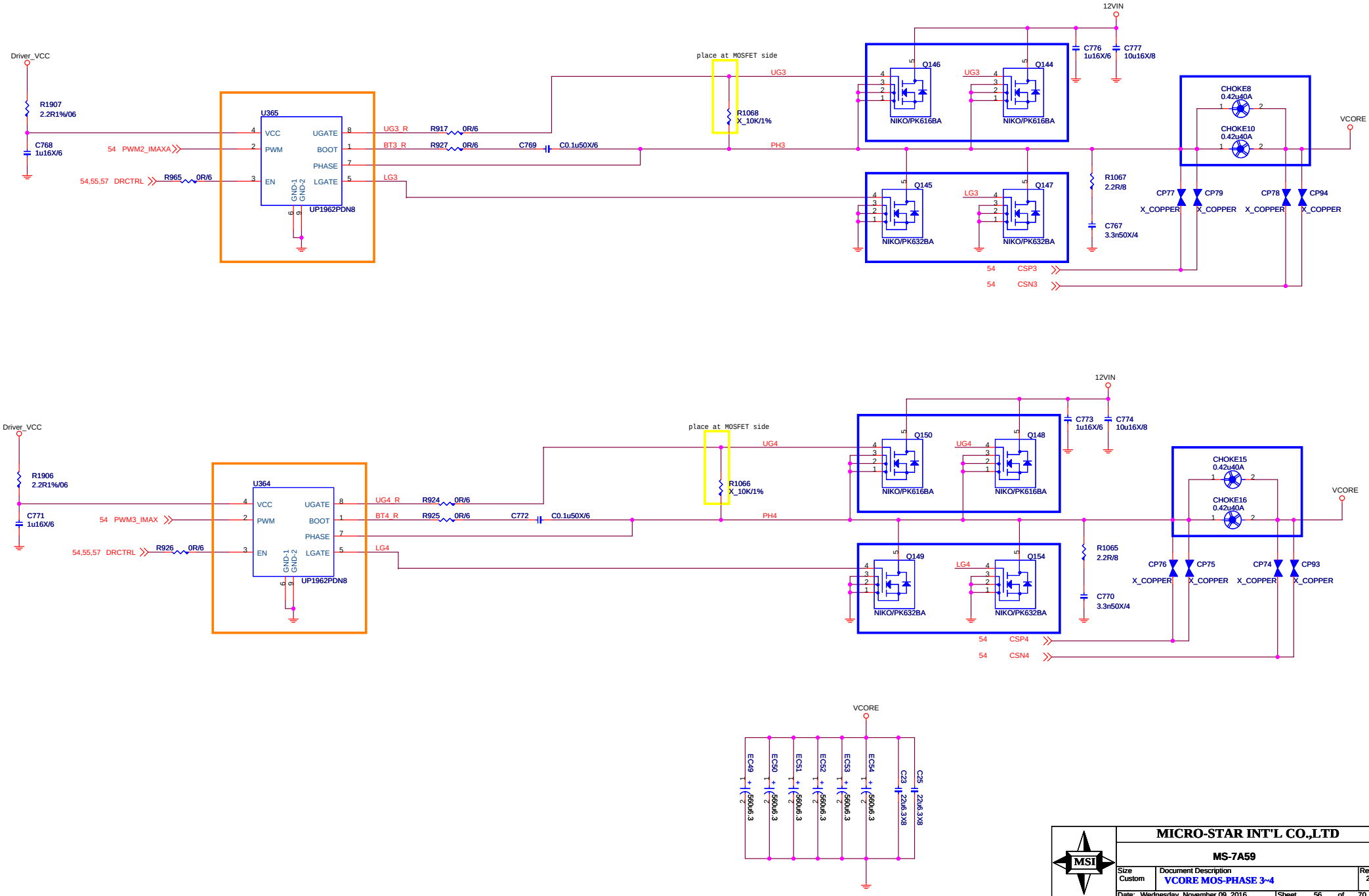
Driver_VCC
R1907
2.2R1%/06
C768
1u16X/6
54 PWM2_IMAXA
54,55,57 DRCTRL
R965 0R/6
U365
VCC
PWM
EN
UGATE
BOOT
PHASE
LGATE
GND-1
GND-2
UP1962PDN8
UG3_R
R917 0R/6
BT3_R
R927 0R/6
C769 C0.1u50X/6
LG3
place at MOSFET side
R1068
X_10K/1%
UG3
PH3
Q146
Q144
NIKO/PK616BA
12VIN
C776
1u16X/6
C777
10u16X/8
CHOKE8
0.42u40A
CHOKE10
0.42u40A
VCORE
Q145
Q147
NIKO/PK632BA
R1067
2.2R/8
C767
3.3n50X/4
CP77
CP79
CP78
CP94
X_COPPER
54 CSP3
54 CSN3
Driver_VCC
R1906
2.2R1%/06
C771
1u16X/6
54 PWM3_IMAX
54,55,57 DRCTRL
R926 0R/6
U364
UP1962PDN8
UG4_R
R924 0R/6
BT4_R
R925 0R/6
C772 C0.1u50X/6
LG4
place at MOSFET side
R1066
X_10K/1%
UG4
PH4
Q150
Q148
Q149
Q154
C773
1u16X/6
C774
10u16X/8
CHOKE15
0.42u40A
CHOKE16
0.42u40A
R1065
2.2R/8
C770
3.3n50X/4
CP76
CP75
CP74
CP93
54 CSP4
54 CSN4
VCORE
EC49
EC50
EC51
EC52
EC53
EC54
C23
C25
560u6.3
22u6.3X8
MSI
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size
Custom
Document Description
VCORE MOS-PHASE 3~4
Rev
2.1
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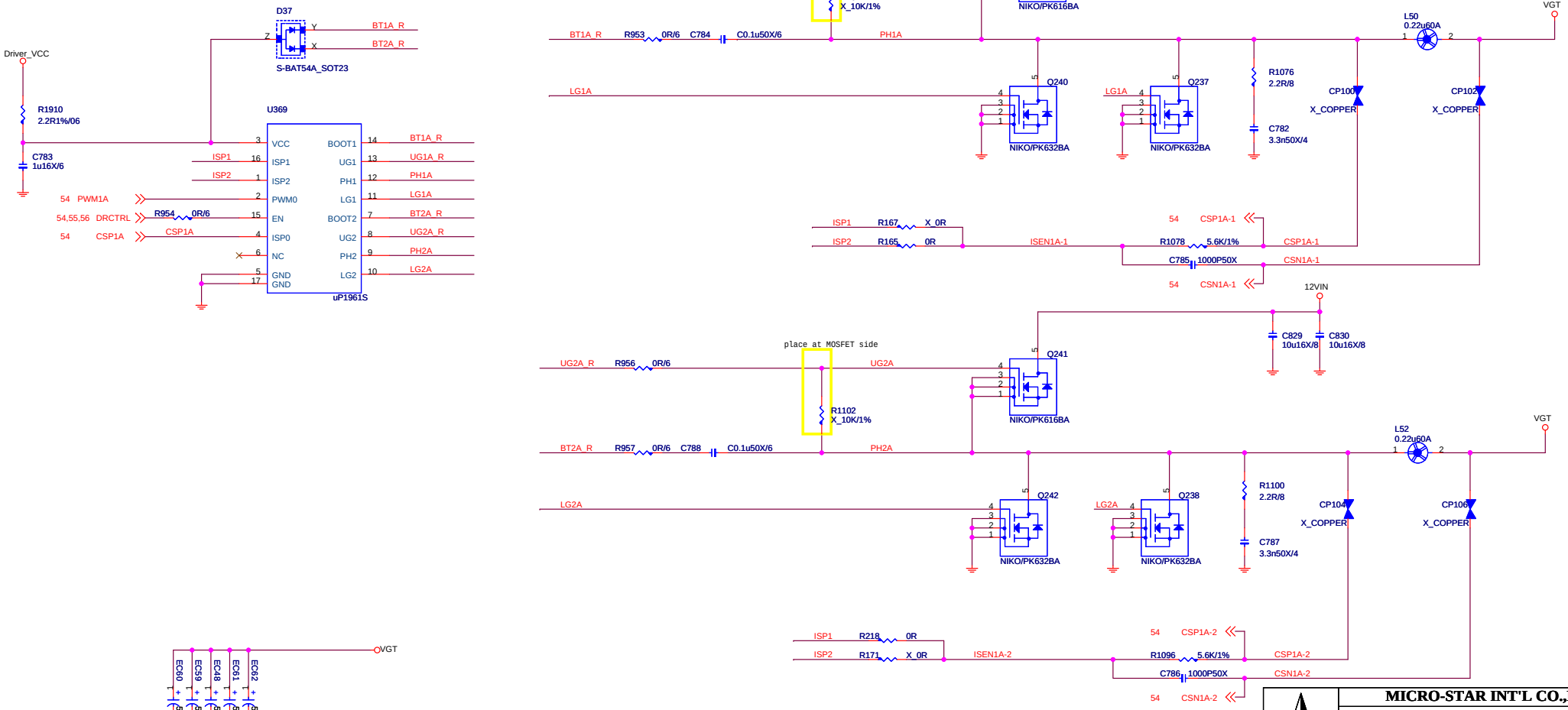
RT7 放在L50與L52中間

RT8放置在VccGT 這組switching power 最熱的地方



MICRO-STAR INT'L CO.,LTD

MS-7A59

Size	Document Description	Rev
Custom	VGT MOS-PHASE 1~2	2.1

Date: Wednesday, November 09, 2016 Sheet 57 of 70

VCCIO

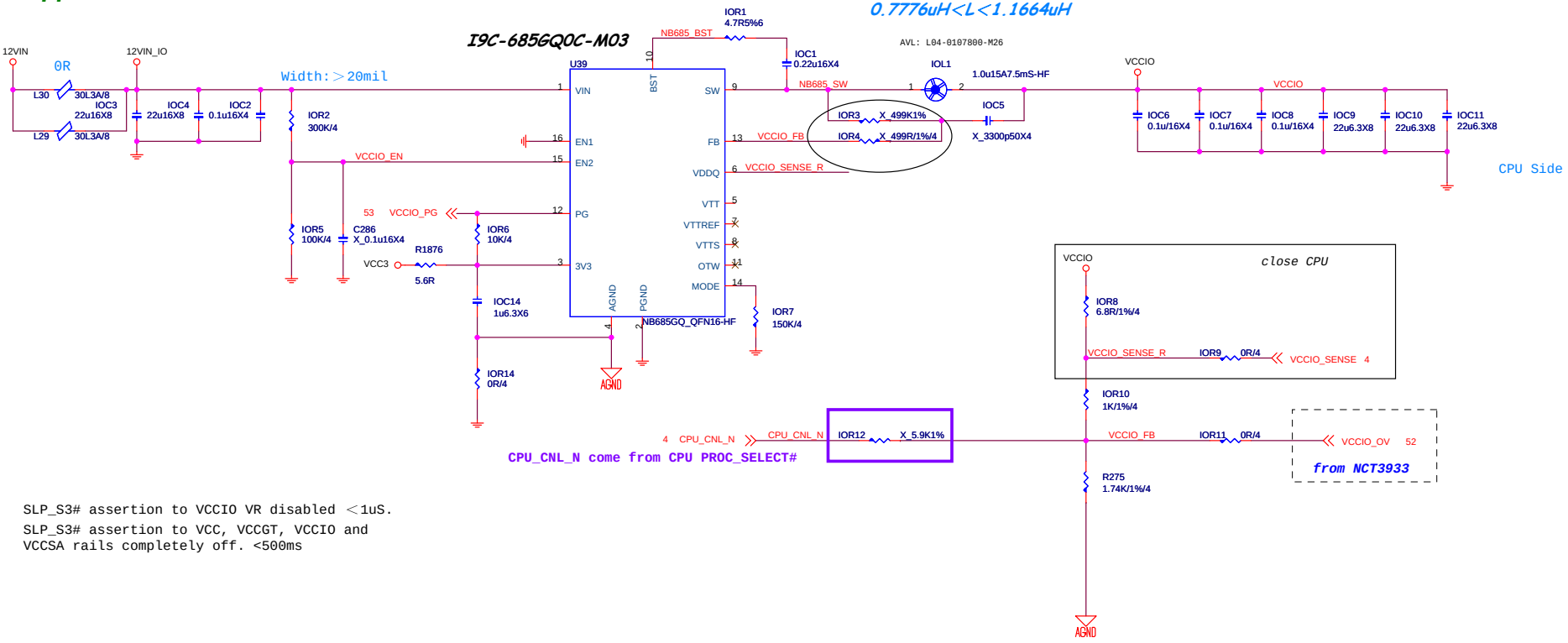
0.95V; 5.5A

IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*

support 0V=>NB685

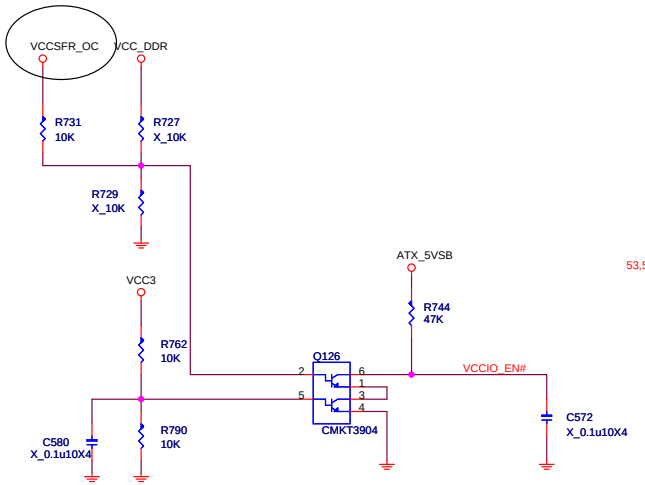
0.7776uH<L<1.1664uH

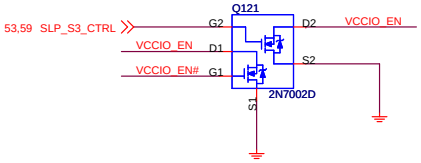
I9C-685GQ0C-M03



CPU_CNL_N come from CPU PROC_SELECT#

SLP_S3# assertion to VCCIO VR disabled ＜1uS.
SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms





SLP_S3# assertion to VR disabled
max:1us

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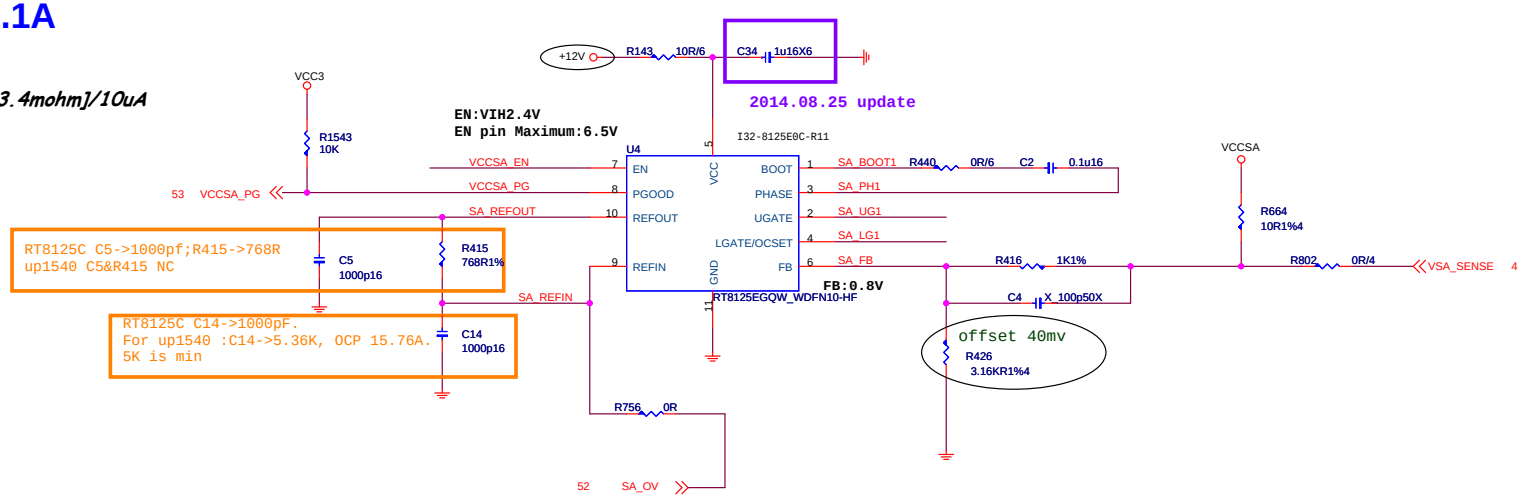
SA Power:1.05V,11.1A

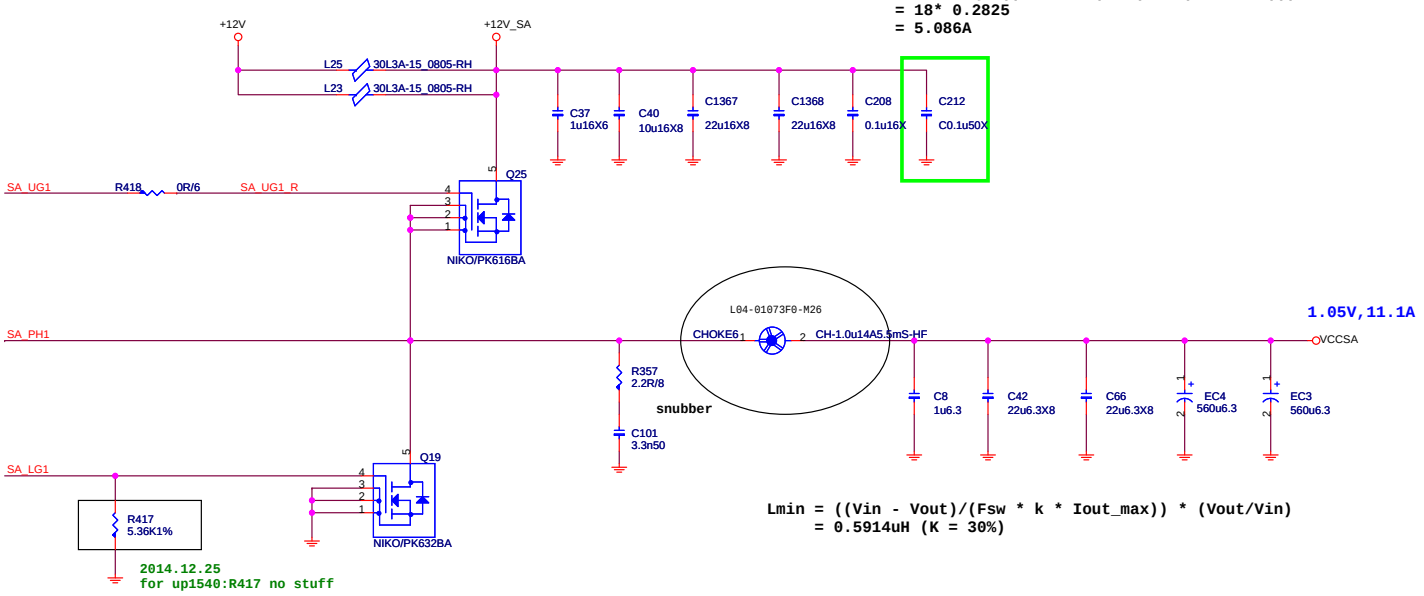
*OCP =11.1A*1.4=15.54A*
*Rocs(R417)=OCP*Rdson(Low side)3.4mohm]/10uA*
=15.54(3.4)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm



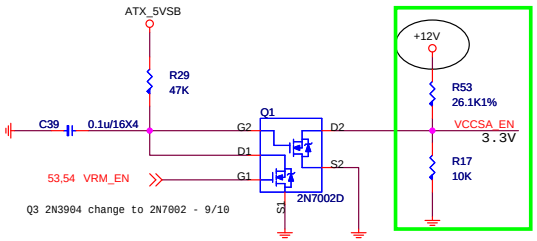
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 18* 0.2825
= 5.086A



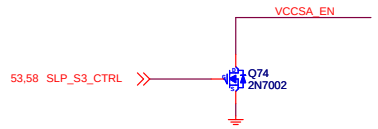
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

VRM_EN線路update

Pull up by layout&Check level



EN:VIH2.4V
EN pin Maximum:6.5V



SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

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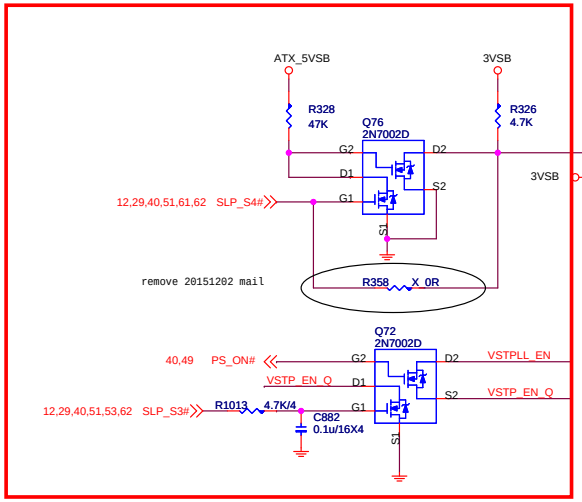
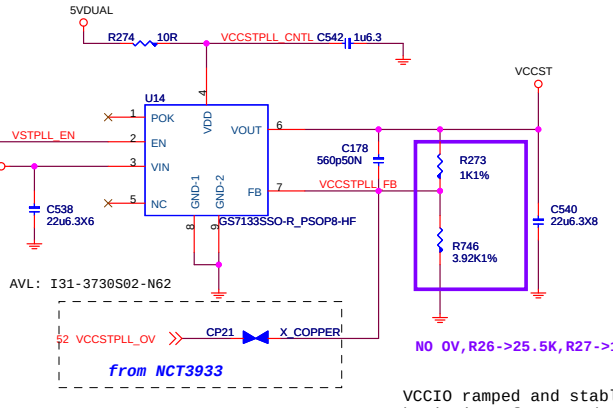
VCCST

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO and H110





NO OV,R26->25.5K,R27->100K, C178 unstuff

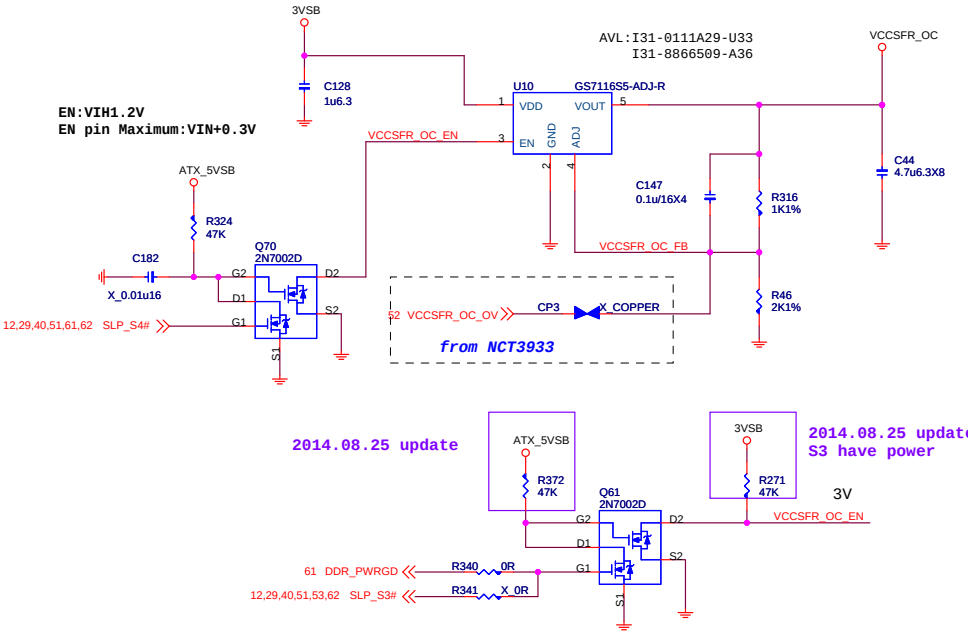
VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

VCCPLL_OC

1.2V; 110mA

2014.08.21 update



2014.08.25 update

2014.08.25 update
S3 have power

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DDR4_1.2V 2.5A+9.5A+1.2A=13.5A

2.8A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

OCP =13.5A*1.5=20.25A

Rocs(R3)=OCP*Rdson[(Low side)]/10uA

=20.25A*(4.6)mohm/10uA

=9.315Kohm

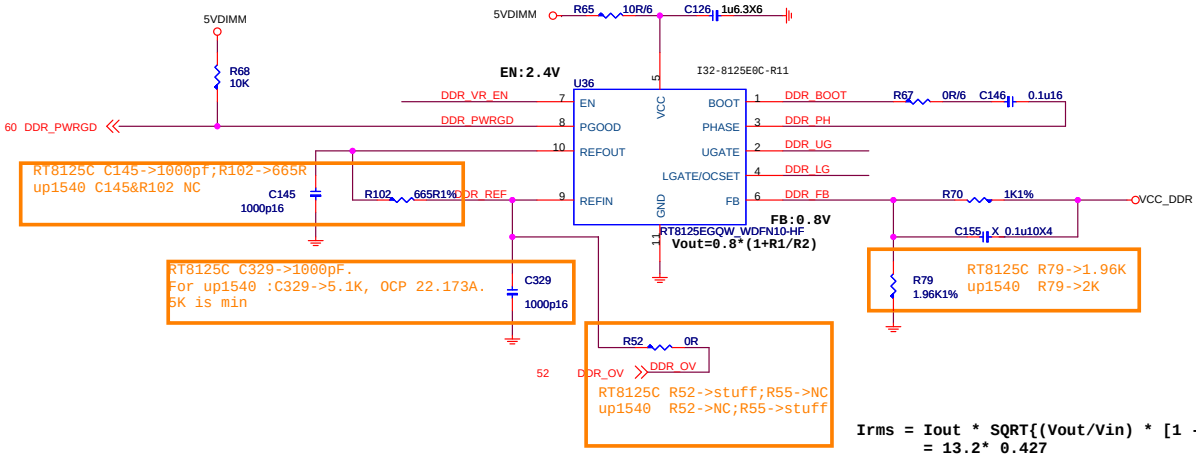
Rocpset:7.32K

OCP=Rocset*Rdson(Low side)/10uA

=7.32K*3.6mohm/10uA

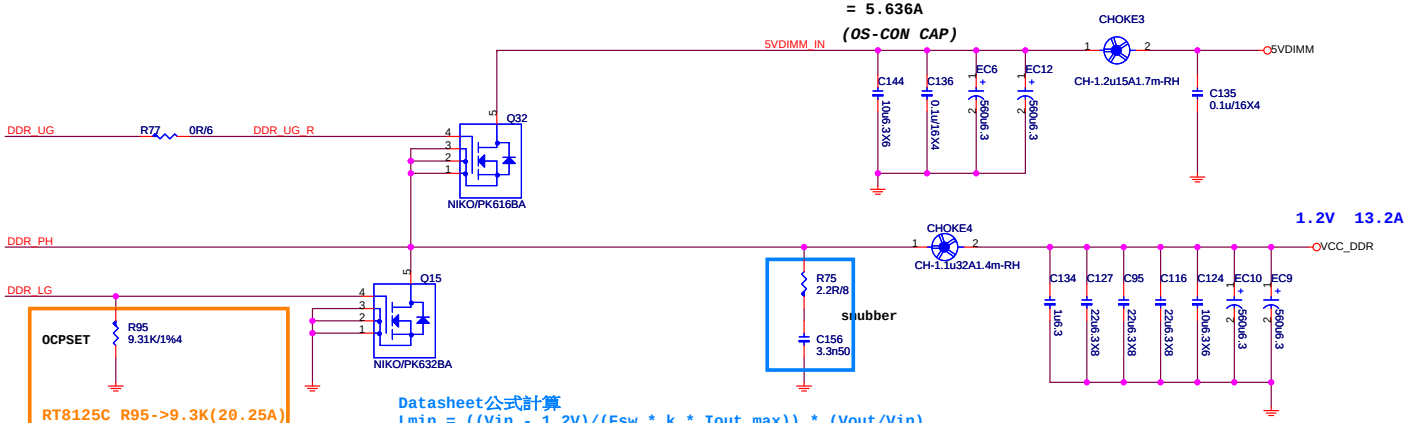
=20.3A

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm



Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A

(OS-CON CAP)



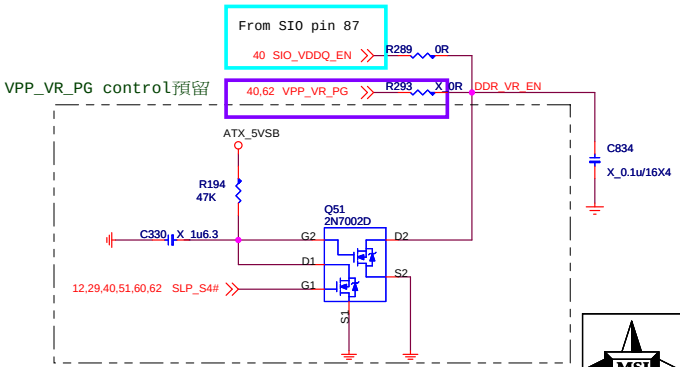
Datasheet公式計算

Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)

= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH＜L＜1.2897uH

2014.12.17 update



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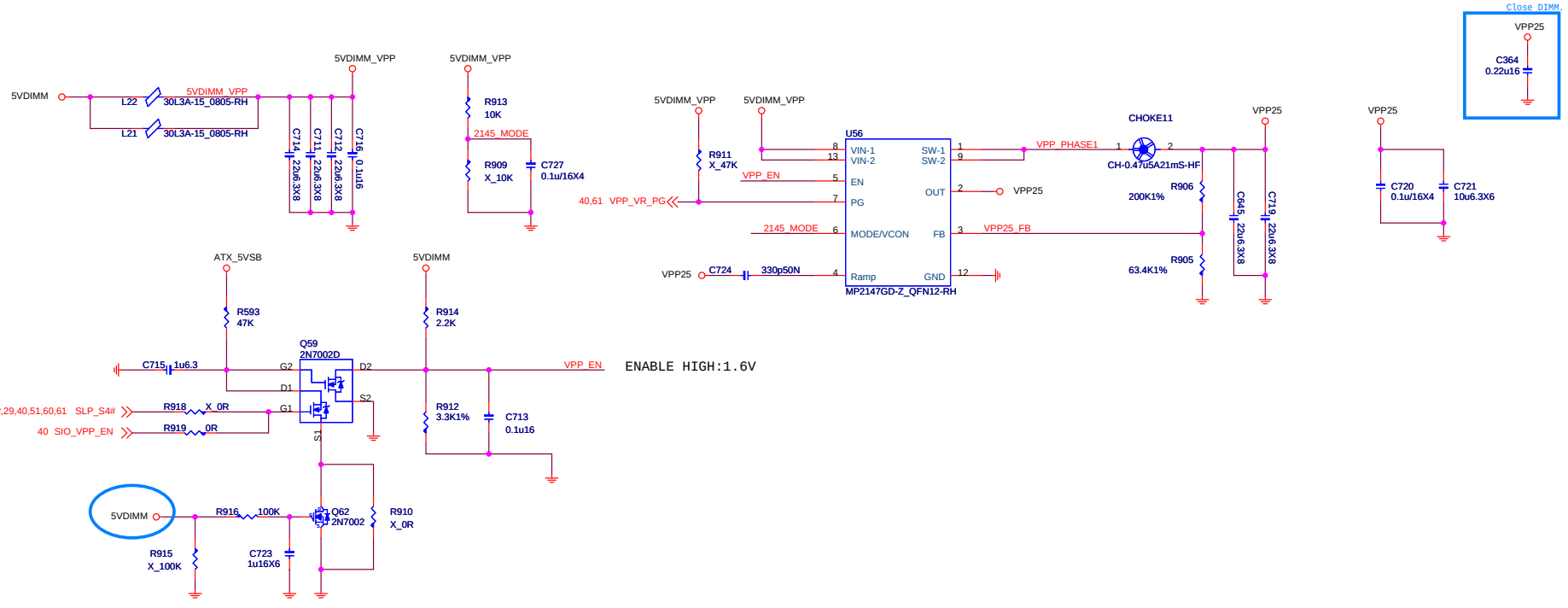
4DIMM :2.84A FOR DDR VPP2.5V

VPP25 Power

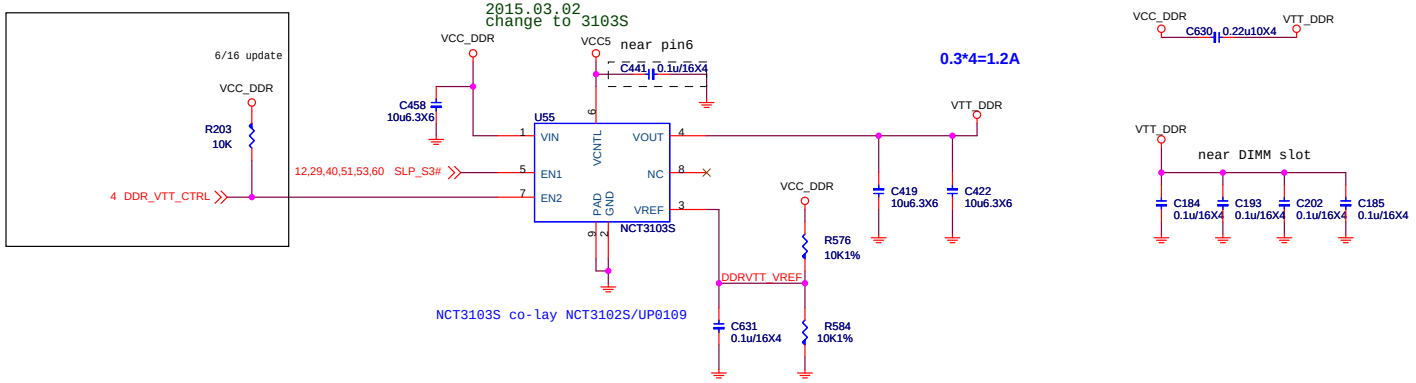
2.5V; 2.24A



ENABLE HIGH:1.6V

To make sure VPP EN after 5VDIMM stable

DDR VTT Power



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PCH_1VSB

1.0V; 11.83A

Rdson(low)4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

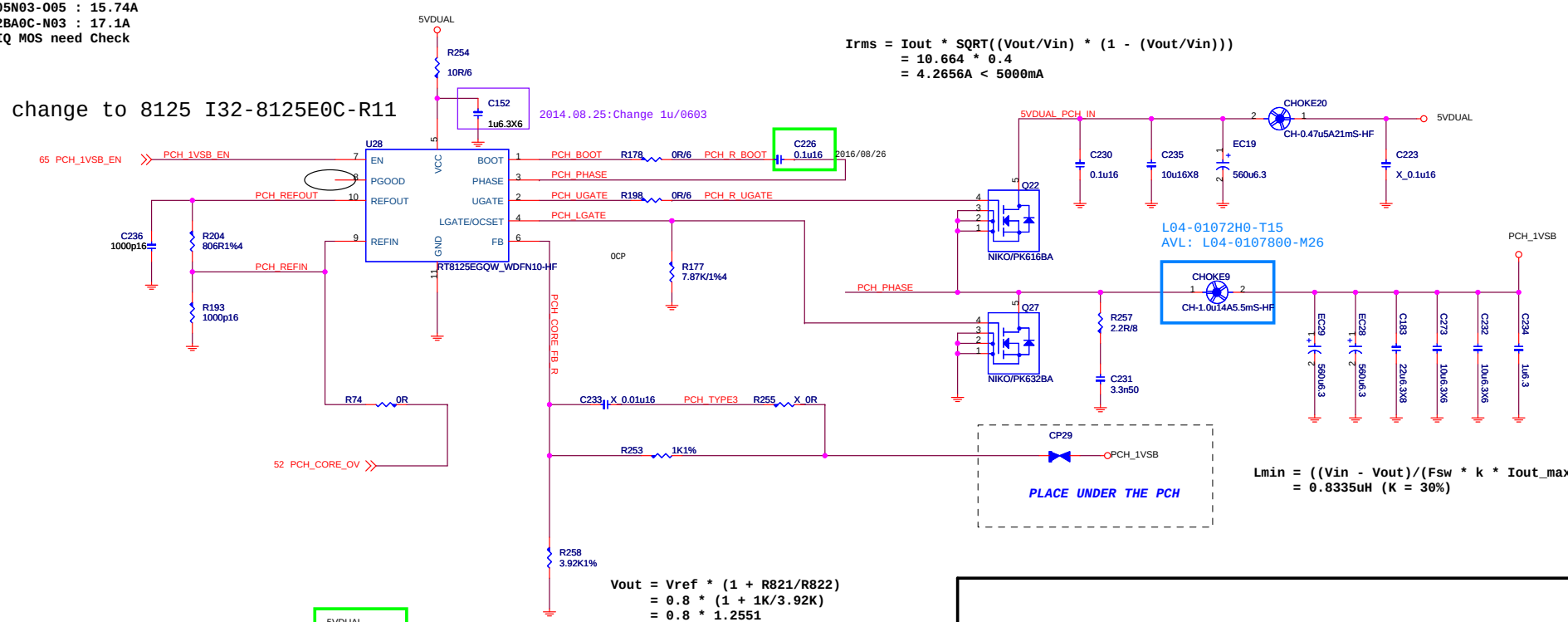
OCP = 17.745A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 11.83 * 4.6mohm / 10uA
= 8.16K

Rocs:7.87K,OCP:
D03-4C05N03-005 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

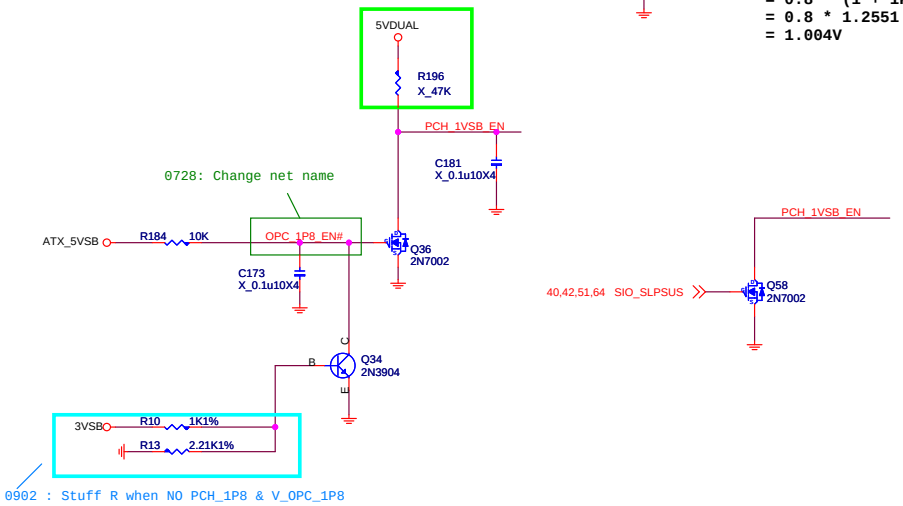
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

1504 change to 8125 I32-8125E0C-R11



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V



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MS-7A59	
Size: Custom	Document Description: PCH Core Power-RT8125
Rev: 2.1	
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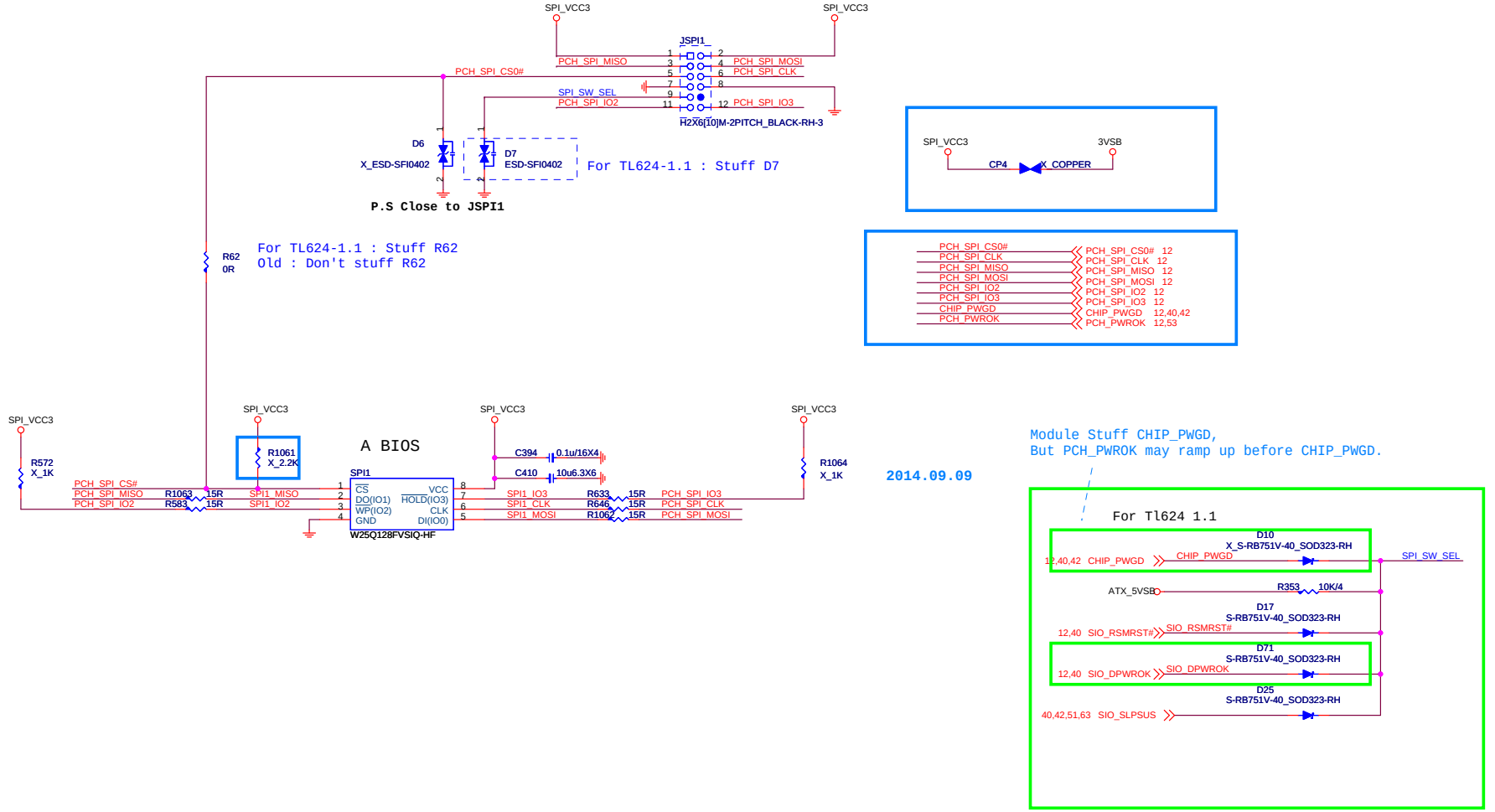

MICRO-STAR INT'L CO.,LTD

MS-7A59

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Custom	BIOS	2.1

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Co-Lay NOT USE U1 , R150 STUFF

RTCRST# R150 X_0R/4 RTCRST# D

If STUFF R150 Please Check RTCRST# Double Pull High

20160629

2016/08/29

CLR_CMOS#

R44 X_100K/4

CUT_VBAT

R55 X_100K/4

JBAT1

H1X2M_BLACK-RH

RTCRST# D

R1094 20K

C607 1u6.3X6

D72 ESD-SFI0402

SIO_3VA

R233 X_4.7K/4

40 CLR_CMOS#

CLR_CMOS#

RTCRST# D

2016/08/29

SIO_3VA

R330 X_4.7K

40 CUT_VBAT

CUT_VBAT

DIS_CHARGE

R232 100K/4

VBAT

C739 0.1u/16X4

U12

VDD

CLR_CMOS function 1

INPUT1 CLR_CMOS#

INPUT2 RTCRST#_D

RTCRST#_PCH OUTPUT1

11 RTCRST# RTCRST# 12

CUT_VBAT function 2

INPUT3 CUTVBAT

POWER_OFF OUTPUT2

12 POWER_OFF

INPUT4 DIS_CHARGE

RTCRST#_SIO OUTPUT3

13 RTCRST# D RTCRST#_D 41

LOW SWITCH

VIN VBAT

VBAT_PCH(POWER) VOUT

7 VBAT_PCH

NC-1 NC-2 GND-1 GND-2

SLG4B41231V_STQFN14-HF

if has cut other power,please use output 2.

if has discharge function R232 NC.

Co-Lay NOT USE U1 , ALL UNSTUFF

ATX_5VSB

2016/08/29

R130 4.7K/4

3VA_OFF#

3VA_OFF# 51

POWER_OFF

Q11

N-2N7002

3VDSW

R188 9.1K/1%/4

3VSB_EN

3VSB_EN 51

POWER_OFF

Q13

N-2N7002

3VSB

DCPRTC

DCPRTC 16

R142 5.6K/1%

PCH_1VSB_EN

PCH_1VSB_EN 63

POWER_OFF

Q12

N-2N7002

PCH_1VSB

POWER_OFF R162 2.2K/4

Q14

N-2N7002

PCH_TIME

C27 0.1u/16X4

VBAT

3VDSW

VBAT

20mil

2016/08/29

R113 3K1%/4

C26 1u6.3X6

D3 S-BAT54C_SOT23

R329 45.3K1%

R115 1K1%

VBAT1

BAT1

BAT-2P-RH-1

Co-Lay NOT U1 , Stuff R18

VBAT_PCH R236 X_0R VBAT

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Size Custom

Document Description Clear CMOS

Rev 2.1

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PCB

PCB1

7A59_20

PD0-07A5921-G37
PD0-07A5921-E48

CPU_H1
CPU 鍍座
CPU_H1

BAT1_X1
BAT-BCR2032P-RH

Mounting Holes

MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9
X_MH001

C466 0.1u/16X4
C510 0.1u/16X4

LAN001
LAN+ USB20
X_LANCONN

R001
10K
X_10K

PCIE001 PCIE SLOT X_PCIESLOTX16
PCIE002 PCIE SLOT X_PCIESLOTX8
PCIE003 PCIE SLOT X_PCIESLOTX16
PCIE004 PCIE SLOT X_PCIESLOTX8

LED001
LED RED
X_LED04-[BR]-50mA2.35V_1608-RH

DIMM001
DIMM
X_DDRIV

AMI_LABLE1
AMI_BIOS LABLE
BIOS_LABLE

HDMI_LA1
HDMI LABLE
HDMI LABEL

CFOS_LA1
CFOS
CFOS LABEL

NAH_LA1
NAHIMIC
NAH_LABEL

XSP_LA1
XSPLIT
XSP_LABEL

SSE_LA1
SSE
SSE_LABEL

LED002
LED RED
X_LED04-[BR]-25mA2.35V_1711-RH

M002
M2
X_M2

MKT_LA1
MKT LABLE
MKT LABEL

HS_AUDIO1
Audio Cover
E21-7978010-RH

MKTLA001
MKT LABLE
X_MKT LABEL

HS_MOS1
MEC1 MEC2 MEC3 MEC4 MEC5 MEC6 MEC7
mosheatsink

PCH_HS1
MEC1 MEC2
HS-0408570-HF

Simulation

SIM1 SIM2
X_PIN1*2

Test point

VCORE VCORE1
VGT VGT1
VCC_DDR VCC_DDR1
VCCSA VCCSA1
VCCIO VCCIO1
PCH_1VSB PCH_1VSB1
VCCST VCCST1
VCCSFR_OC VCCSFR1
VTT_DDR VTT_DDR1
VPP25 VPP1

Optical Fiducial Marks-120

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8
X_FM

VR_COVER1
VR Cover
E21-7976010-RH

USB001
USB CONN
X_USBAM_RED
TYPE-A

DDR_COVER1
DDR COVER
E21-7A63010-RH

To POWER 2015/02/03

MICRO-STAR INT'L CO.,LTD

MS-7A59

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Custom	Manual parts	2.1

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