MS-7A59

ATX

Ver: 1.0

Intel -Kabylake plamform Z270

CPU:

kabylake-S

System Chipset:

Z270

Onboard Chip:

HD Audio Codec:ALC1220
LAN:INTEL I219
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X8) Slot *1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*M2 * 3*

Other:

SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 *2*
*REAR USB2.0 *2*
REAR USB TYPE A+C

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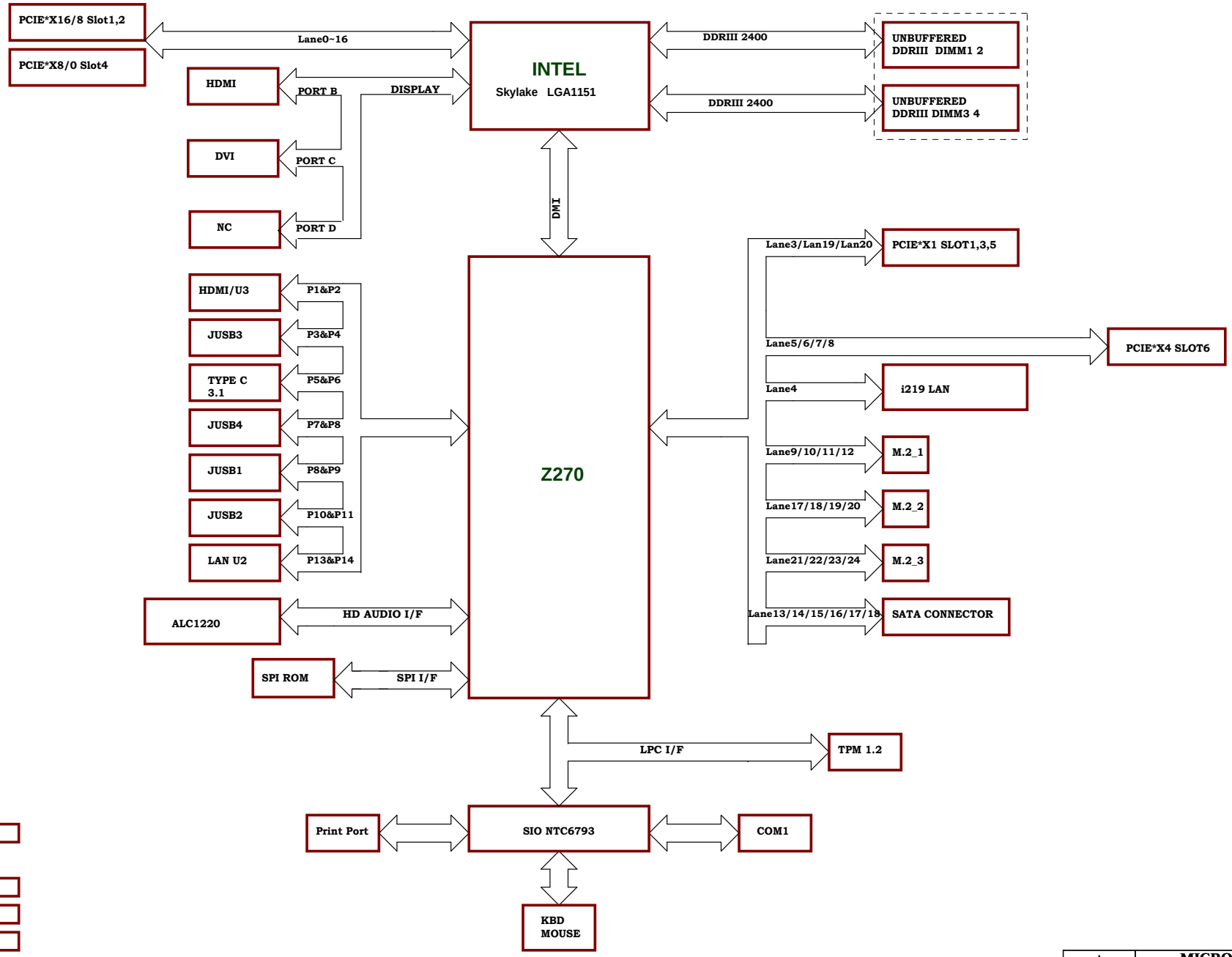
MS-7A59

Size: Custom | Document Description: Cover Sheet | Rev: 2.0

Date: Monday, September 12, 2016 | Sheet 1 of 70

MS-7A59 Block Diagram



Slot Sequence:

- M.2
- PCIE X1
- PCIE X16
- PCIE X1 / M.2
- PCIE X8
- PCIE X1 / M.2
- PCIE X4

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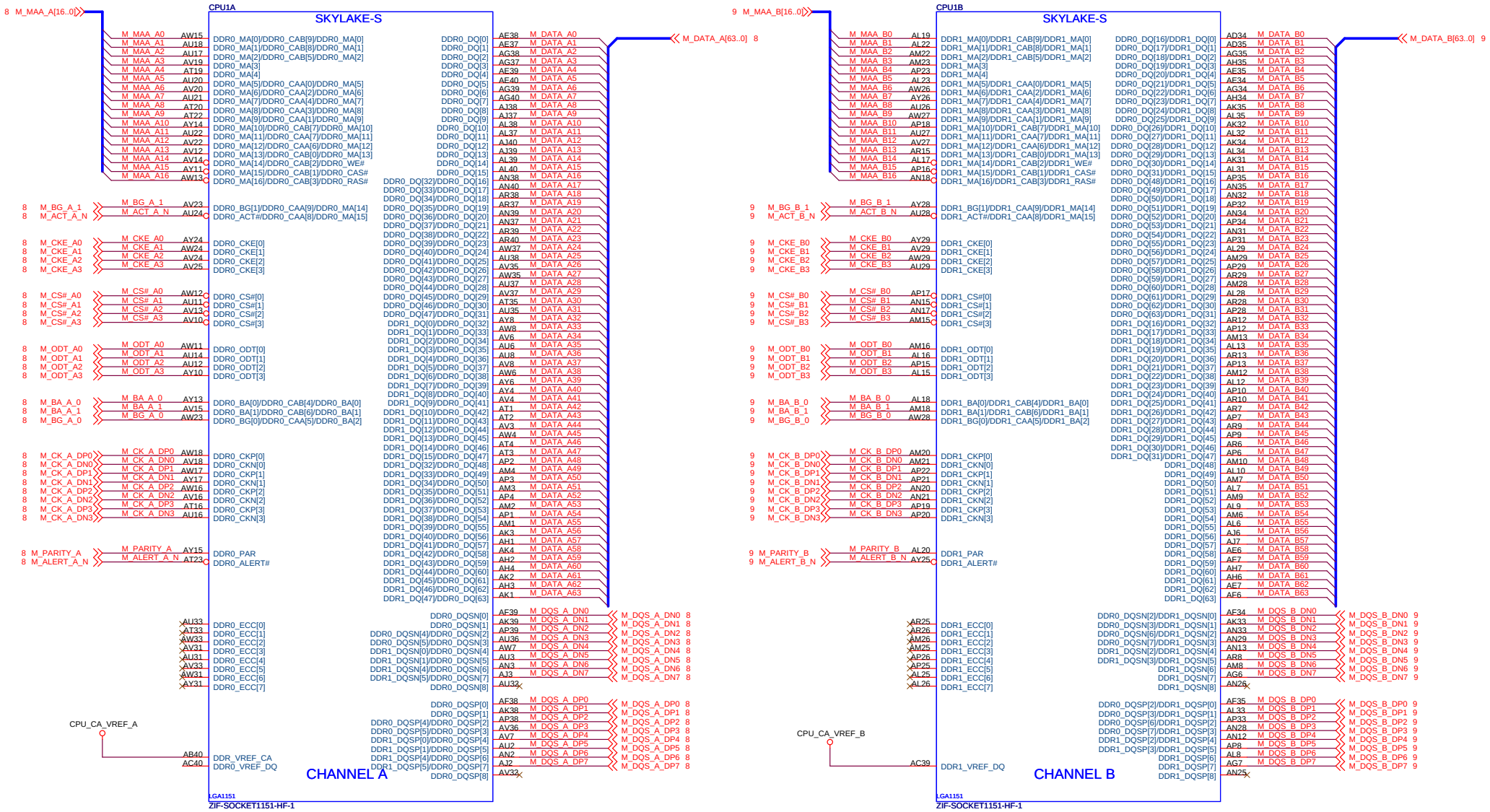
MS-7A59

Size	Document Description	Rev
Custom	Block Diagram	2.0

Date: Monday, September 12, 2016 | Sheet 2 of 70



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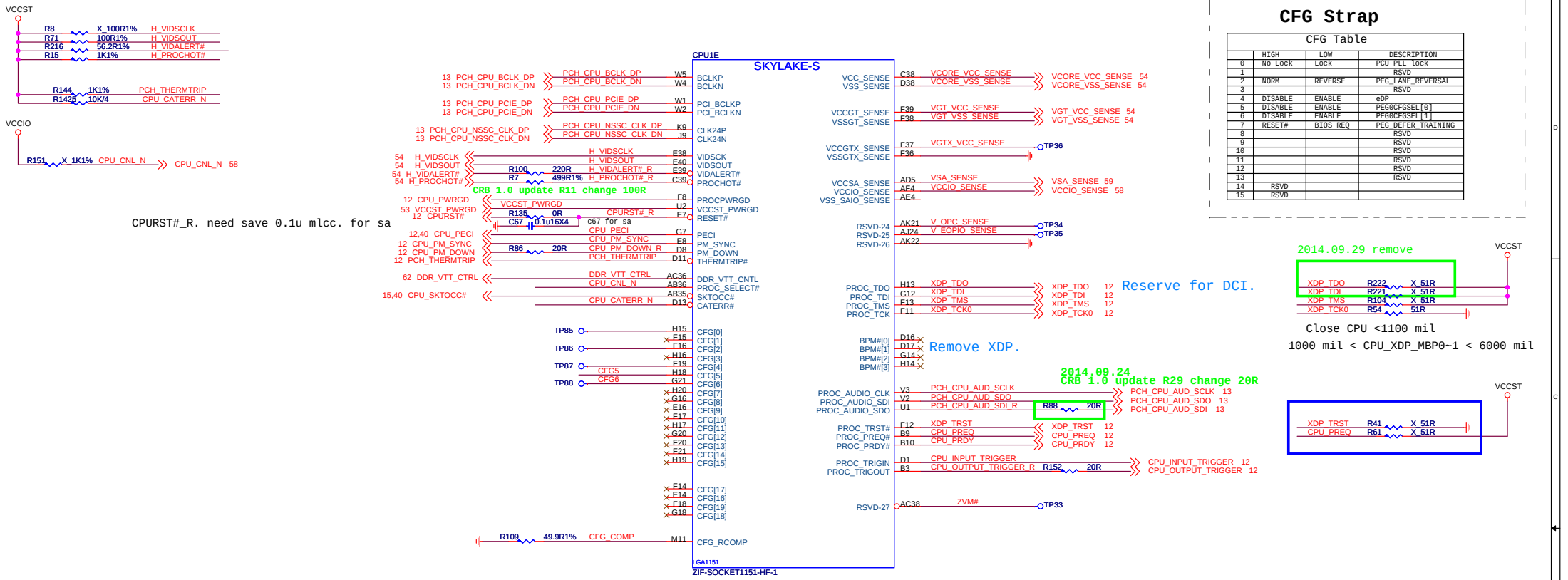
MS-7A59

Size	Document Description	Rev
Custom	CPU-Memory	2.0

Date: Monday, September 12, 2016 Sheet 3 of 70



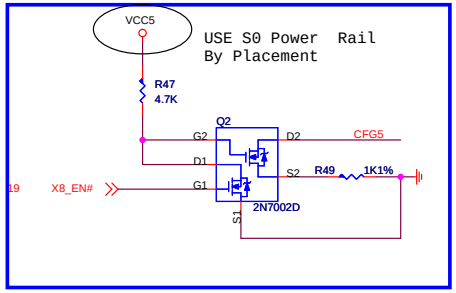
CFG Strap

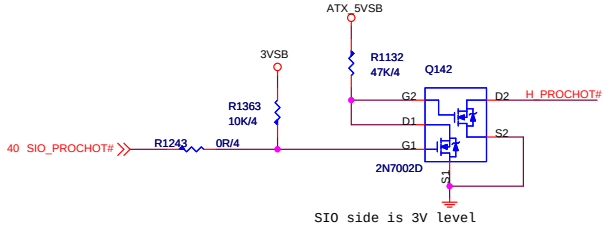
CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

X8 Ctrl

ENABLE# X8	SLOT1	SLOT4
0	X8	X8
1	X16	X0





CFG Strap

CFG Table

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0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

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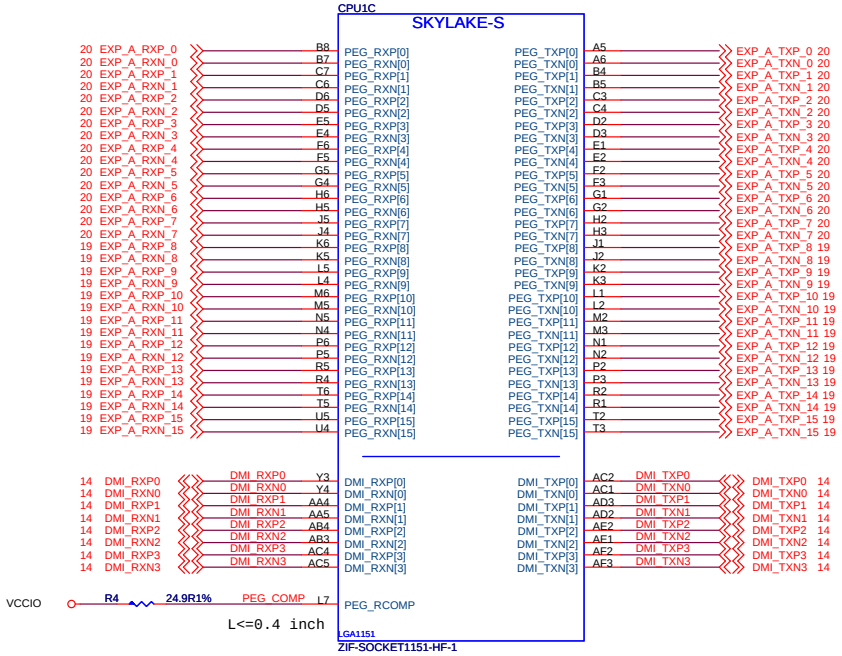
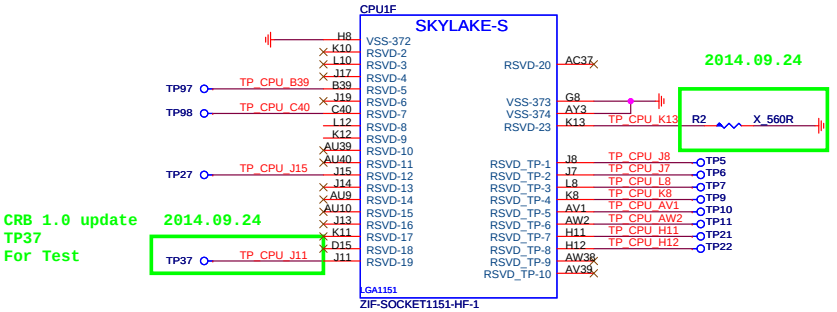
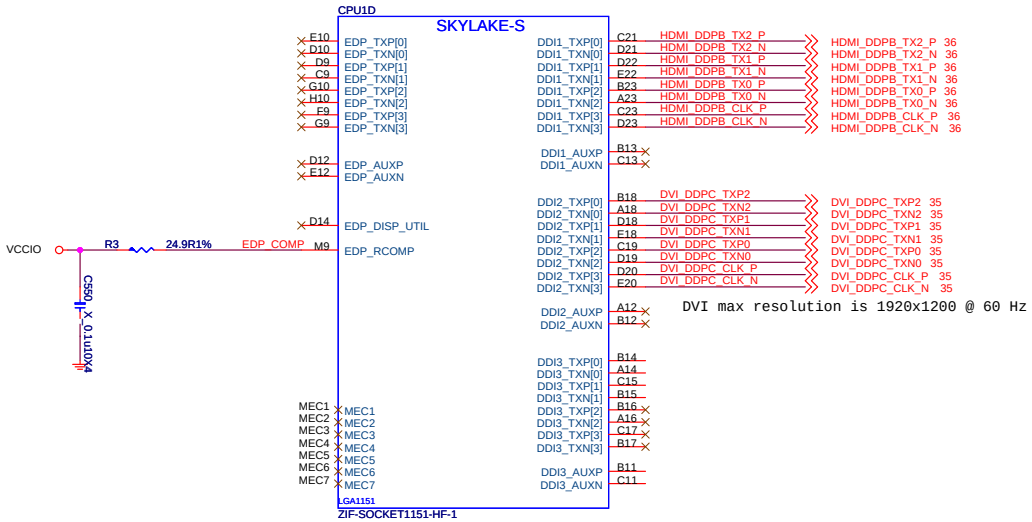
MS-7A59

Size: Custom | Document Description: CPU-Control/MISC/CFG/Audio | Rev: 2.0

Date: Monday, September 12, 2016 | Sheet 4 of 70







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MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A59	
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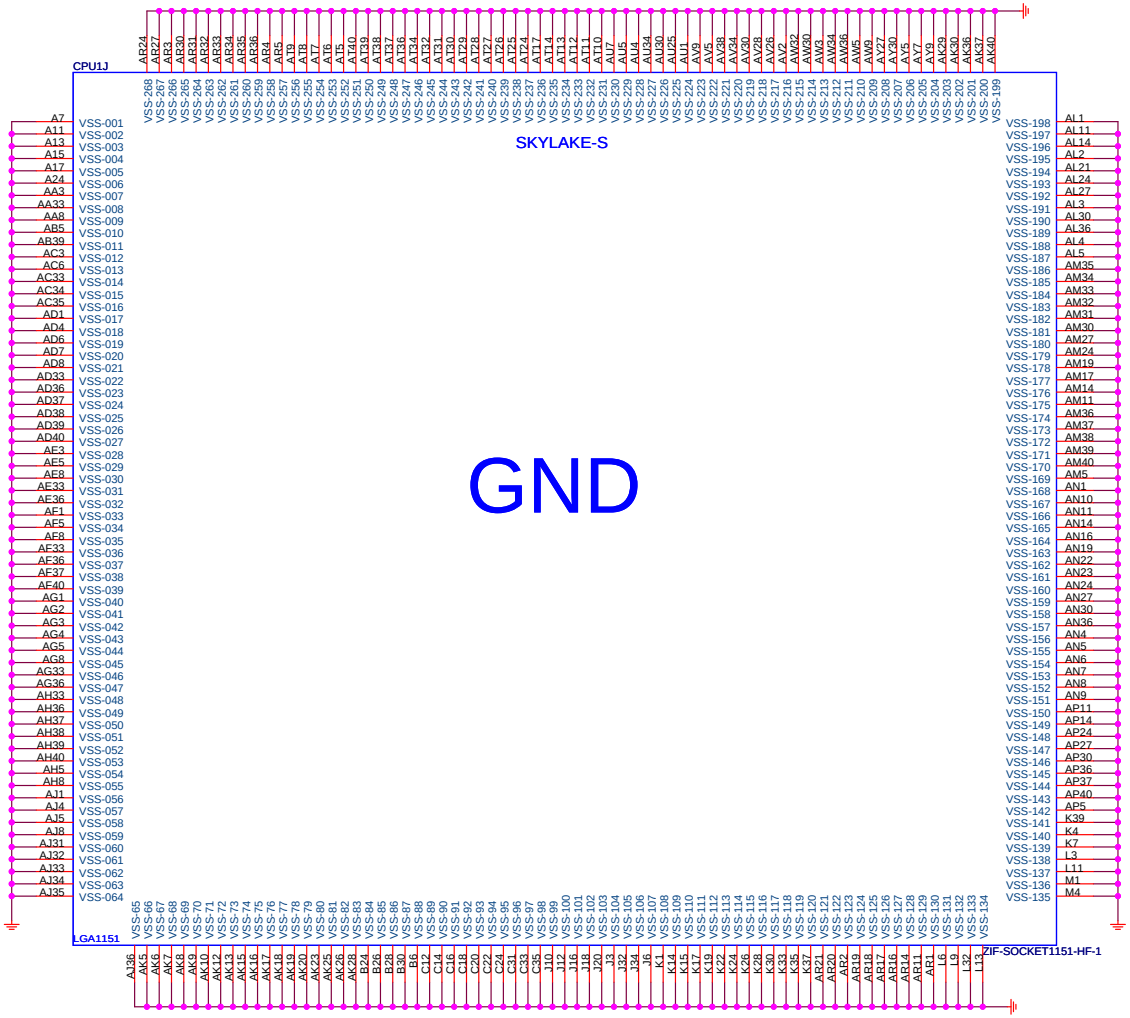
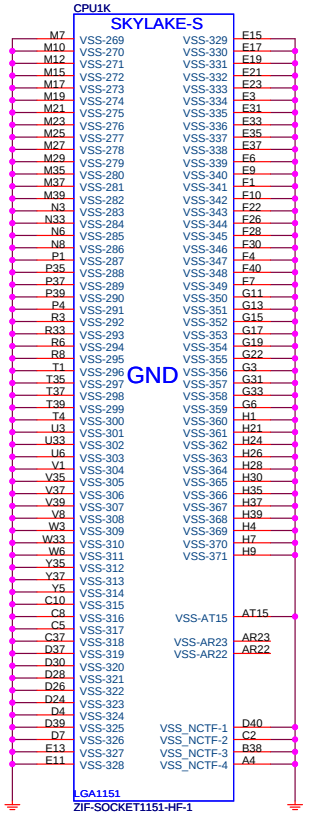
Date: Monday, September 12, 2016	Sheet 5 of 70	





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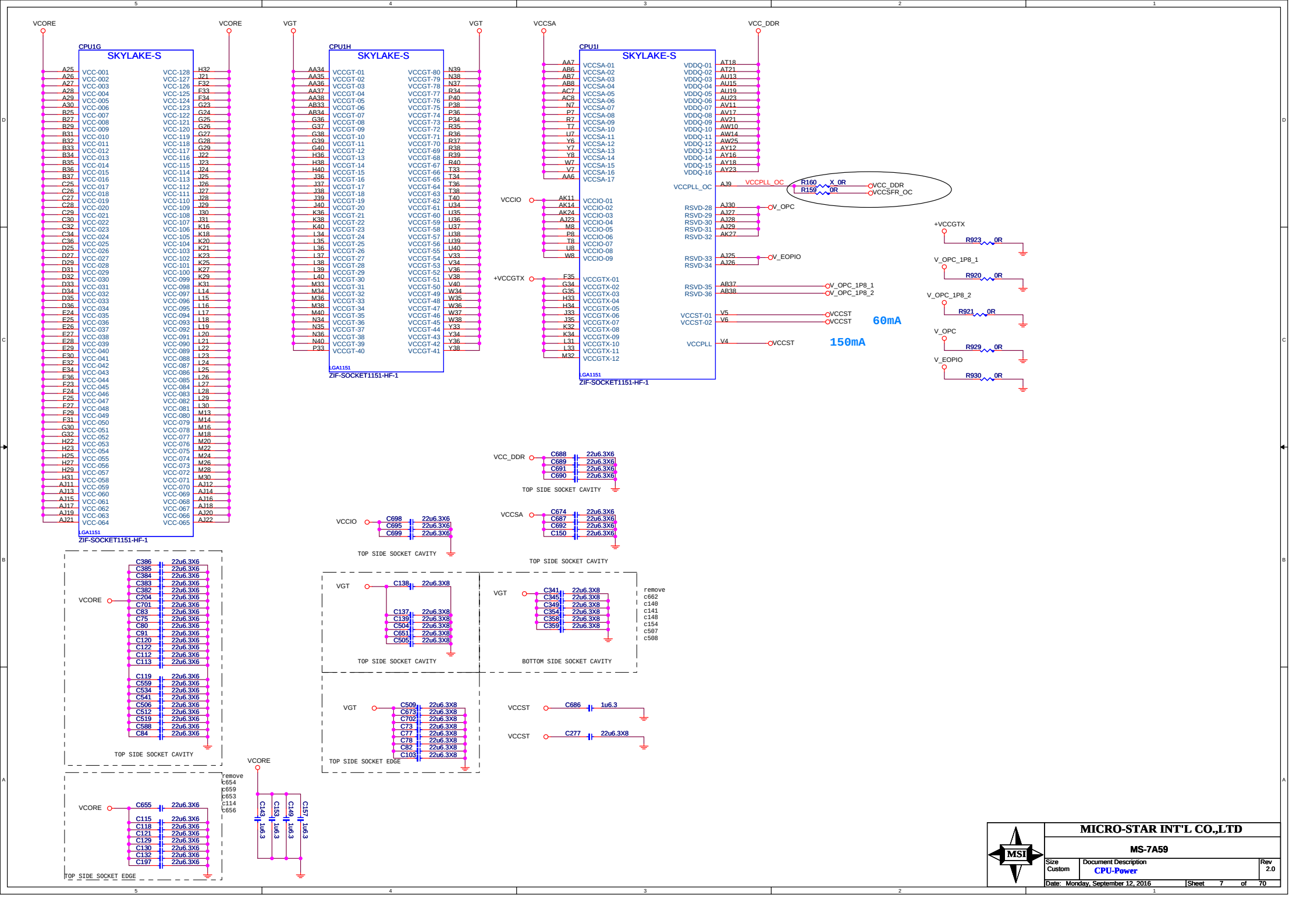
VCORE
CPU1G
SKYLAKE-S
VCC-001 VCC-002 VCC-003 VCC-004 VCC-005 VCC-006 VCC-007 VCC-008 VCC-009 VCC-010 VCC-011 VCC-012 VCC-013 VCC-014 VCC-015 VCC-016 VCC-017 VCC-018 VCC-019 VCC-020 VCC-021 VCC-022 VCC-023 VCC-024 VCC-025 VCC-026 VCC-027 VCC-028 VCC-029 VCC-030 VCC-031 VCC-032 VCC-033 VCC-034 VCC-035 VCC-036 VCC-037 VCC-038 VCC-039 VCC-040 VCC-041 VCC-042 VCC-043 VCC-044 VCC-045 VCC-046 VCC-047 VCC-048 VCC-049 VCC-050 VCC-051 VCC-052 VCC-053 VCC-054 VCC-055 VCC-056 VCC-057 VCC-058 VCC-059 VCC-060 VCC-061 VCC-062 VCC-063 VCC-064
VCC-065 VCC-066 VCC-067 VCC-068 VCC-069 VCC-070 VCC-071 VCC-072 VCC-073 VCC-074 VCC-075 VCC-076 VCC-077 VCC-078 VCC-079 VCC-080 VCC-081 VCC-082 VCC-083 VCC-084 VCC-085 VCC-086 VCC-087 VCC-088 VCC-089 VCC-090 VCC-091 VCC-092 VCC-093 VCC-094 VCC-095 VCC-096 VCC-097 VCC-098 VCC-099 VCC-100 VCC-101 VCC-102 VCC-103 VCC-104 VCC-105 VCC-106 VCC-107 VCC-108 VCC-109 VCC-110 VCC-111 VCC-112 VCC-113 VCC-114 VCC-115 VCC-116 VCC-117 VCC-118 VCC-119 VCC-120 VCC-121 VCC-122 VCC-123 VCC-124 VCC-125 VCC-126 VCC-127 VCC-128
LGA1151
ZIF-SOCKET1151-HF-1
VGT
CPU1H
SKYLAKE-S
VCCGT-01 VCCGT-02 VCCGT-03 VCCGT-04 VCCGT-05 VCCGT-06 VCCGT-07 VCCGT-08 VCCGT-09 VCCGT-10 VCCGT-11 VCCGT-12 VCCGT-13 VCCGT-14 VCCGT-15 VCCGT-16 VCCGT-17 VCCGT-18 VCCGT-19 VCCGT-20 VCCGT-21 VCCGT-22 VCCGT-23 VCCGT-24 VCCGT-25 VCCGT-26 VCCGT-27 VCCGT-28 VCCGT-29 VCCGT-30 VCCGT-31 VCCGT-32 VCCGT-33 VCCGT-34 VCCGT-35 VCCGT-36 VCCGT-37 VCCGT-38 VCCGT-39 VCCGT-40
VCCGT-41 VCCGT-42 VCCGT-43 VCCGT-44 VCCGT-45 VCCGT-46 VCCGT-47 VCCGT-48 VCCGT-49 VCCGT-50 VCCGT-51 VCCGT-52 VCCGT-53 VCCGT-54 VCCGT-55 VCCGT-56 VCCGT-57 VCCGT-58 VCCGT-59 VCCGT-60 VCCGT-61 VCCGT-62 VCCGT-63 VCCGT-64 VCCGT-65 VCCGT-66 VCCGT-67 VCCGT-68 VCCGT-69 VCCGT-70 VCCGT-71 VCCGT-72 VCCGT-73 VCCGT-74 VCCGT-75 VCCGT-76 VCCGT-77 VCCGT-78 VCCGT-79 VCCGT-80
LGA1151
ZIF-SOCKET1151-HF-1
VCCSA
VCC_DDR
CPU1I
SKYLAKE-S
VCCSA-01 VCCSA-02 VCCSA-03 VCCSA-04 VCCSA-05 VCCSA-06 VCCSA-07 VCCSA-08 VCCSA-09 VCCSA-10 VCCSA-11 VCCSA-12 VCCSA-13 VCCSA-14 VCCSA-15 VCCSA-16 VCCSA-17
VDDQ-01 VDDQ-02 VDDQ-03 VDDQ-04 VDDQ-05 VDDQ-06 VDDQ-07 VDDQ-08 VDDQ-09 VDDQ-10 VDDQ-11 VDDQ-12 VDDQ-13 VDDQ-14 VDDQ-15 VDDQ-16
VCCPLL_OC
VCCIO
VCCIO-01 VCCIO-02 VCCIO-03 VCCIO-04 VCCIO-05 VCCIO-06 VCCIO-07 VCCIO-08 VCCIO-09
RSVD-28 RSVD-29 RSVD-30 RSVD-31 RSVD-32
RSVD-33 RSVD-34
+VCCGTX
VCCGTX-01 VCCGTX-02 VCCGTX-03 VCCGTX-04 VCCGTX-05 VCCGTX-06 VCCGTX-07 VCCGTX-08 VCCGTX-09 VCCGTX-10 VCCGTX-11 VCCGTX-12
RSVD-35 RSVD-36
VCCST-01 VCCST-02
VCCPLL
R160 X_0R
R159 0R
VCCPLL_OC
VCC_DDR
VCCSFR_OC
V_OPC
V_EOPIO
V_OPC_1P8_1
V_OPC_1P8_2
VCCST
60mA
150mA
LGA1151
ZIF-SOCKET1151-HF-1
+VCCGTX
R923 0R
V_OPC_1P8_1
R920 0R
V_OPC_1P8_2
R921 0R
V_OPC
R929 0R
V_EOPIO
R930 0R
VCC_DDR
C688 C689 C691 C690 22u6.3X6
TOP SIDE SOCKET CAVITY
VCCIO
C698 C695 C699 22u6.3X6
TOP SIDE SOCKET CAVITY
VCCSA
C674 C687 C692 C150 22u6.3X6
TOP SIDE SOCKET CAVITY
VCORE
C386 C385 C384 C383 C382 C204 C701 C83 C75 C80 C91 C120 C122 C112 C113 22u6.3X6
C119 C559 C534 C541 C506 C512 C519 C588 C84 22u6.3X6
TOP SIDE SOCKET CAVITY
VGT
C138 22u6.3X8
C137 C139 C504 C651 C505 22u6.3X8
TOP SIDE SOCKET CAVITY
VGT
C341 C345 C349 C354 C356 C359 22u6.3X8
BOTTOM SIDE SOCKET CAVITY
remove
c662
c140
c141
c148
c154
c507
c508
VGT
C509 C673 C702 C73 C77 C78 C82 C103 22u6.3X8
TOP SIDE SOCKET EDGE
VCCST
C686 1u6.3
VCCST
C277 22u6.3X8
VCORE
C655 C115 C118 C121 C129 C130 C132 C197 22u6.3X6
TOP SIDE SOCKET EDGE
remove
c654
c659
c653
c114
c656
VCORE
C143 C153 C149 C157 1u6.3
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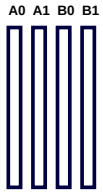
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size
Custom
Document Description
CPU-Power
Rev
2.0
Date: Monday, September 12, 2016
Sheet 7 of 70



VCC_DDR

DIMMA1A

M_DATA_A[63..0] 3

DQS17P DQS17N DQS16P DQS16N DQS15P DQS15N DQS14P DQS14N DQS13P DQS13N DQS12P DQS12N DQS11P DQS11N DQS10P DQS10N DQS9P DQS9N DQS8P DQS8N

DQS7P DQS7N DQS6P DQS6N DQS5P DQS5N DQS4P DQS4N DQS3P DQS3N DQS2P DQS2N DQS1P DQS1N DQS0P DQS0N

M_DQS_A_DP7 M_DQS_A_DN7 M_DQS_A_DP6 M_DQS_A_DN6 M_DQS_A_DP5 M_DQS_A_DN5 M_DQS_A_DP4 M_DQS_A_DN4 M_DQS_A_DP3 M_DQS_A_DN3 M_DQS_A_DP2 M_DQS_A_DN2 M_DQS_A_DP1 M_DQS_A_DN1 M_DQS_A_DP0 M_DQS_A_DN0

M_CK_A_DP1 M_CK_A_DN1 M_CK_A_DP0 M_CK_A_DN0

CK1P CK1N CK0P CK0N

C2 S3_N_C1 S2_N_C0

M_CS#_A1 M_CS#_A0 M_CKE_A1 M_CKE_A0 M_ODT_A1 M_ODT_A0

S1_N S0_N CKE1 CKE0 ODT-1 ODT-0

CB-7 CB-6 CB-5 CB-4 CB-3 CB-2 CB-1 CB-0

DIMM_RESET# DIMM1_EVENT M_ALERT_A_N M_ACT_A_N M_PARITY_A

RESET_N EVENT_N ALERT_N ACT_N PAR

SAVE_N_NC

RFU-0 RFU-1 RFU-2

M_BG_A_1 M_BG_A_0 M_BA_A_1 M_BA_A_0

BG-1 BG-0 BA-1 BA-0

M_MAA_A[16..0] M_MAA_A[16..0] 3

A17 A16_RAS_N A15_CAS_N A14_WE_N A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

SMB_CLK_DIMM SMB_DATA_DIMM

SCL SDA

SA-2 SA-1 SA-0

DDRIV-288P_BLACK-RH-21

DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

VCC_DDR

DIMM1_EVENT R72 240R1%
DIMM2_EVENT R126 240R1%

VCC_DDR

R1621 470R1%

12 DRAM_RESET# R90 0R DIMM_RESET# DIMM_RESET# 9

C106 X_0.1u10X4

12,54 SMBCLK_VCC SMBCLK_VCC R73 0R SMB_CLK_DIMM SMB_CLK_DIMM 9
12,54 SMBDATA_VCC SMBDATA_VCC R161 0R SMB_DATA_DIMM SMB_DATA_DIMM 9

VCC_DDR

DIMMA2A

M_DQS_A_DP7 M_DQS_A_DN7 M_DQS_A_DP6 M_DQS_A_DN6 M_DQS_A_DP5 M_DQS_A_DN5 M_DQS_A_DP4 M_DQS_A_DN4 M_DQS_A_DP3 M_DQS_A_DN3 M_DQS_A_DP2 M_DQS_A_DN2 M_DQS_A_DP1 M_DQS_A_DN1 M_DQS_A_DP0 M_DQS_A_DN0

M_CK_A_DP3 M_CK_A_DN3 M_CK_A_DP2 M_CK_A_DN2

M_CS#_A3 M_CS#_A2 M_CKE_A3 M_CKE_A2 M_ODT_A3 M_ODT_A2

DIMM_RESET# DIMM2_EVENT M_ALERT_A_N M_ACT_A_N M_PARITY_A

VDDSPD

DDRIV-288P_BLACK-RH-21

DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

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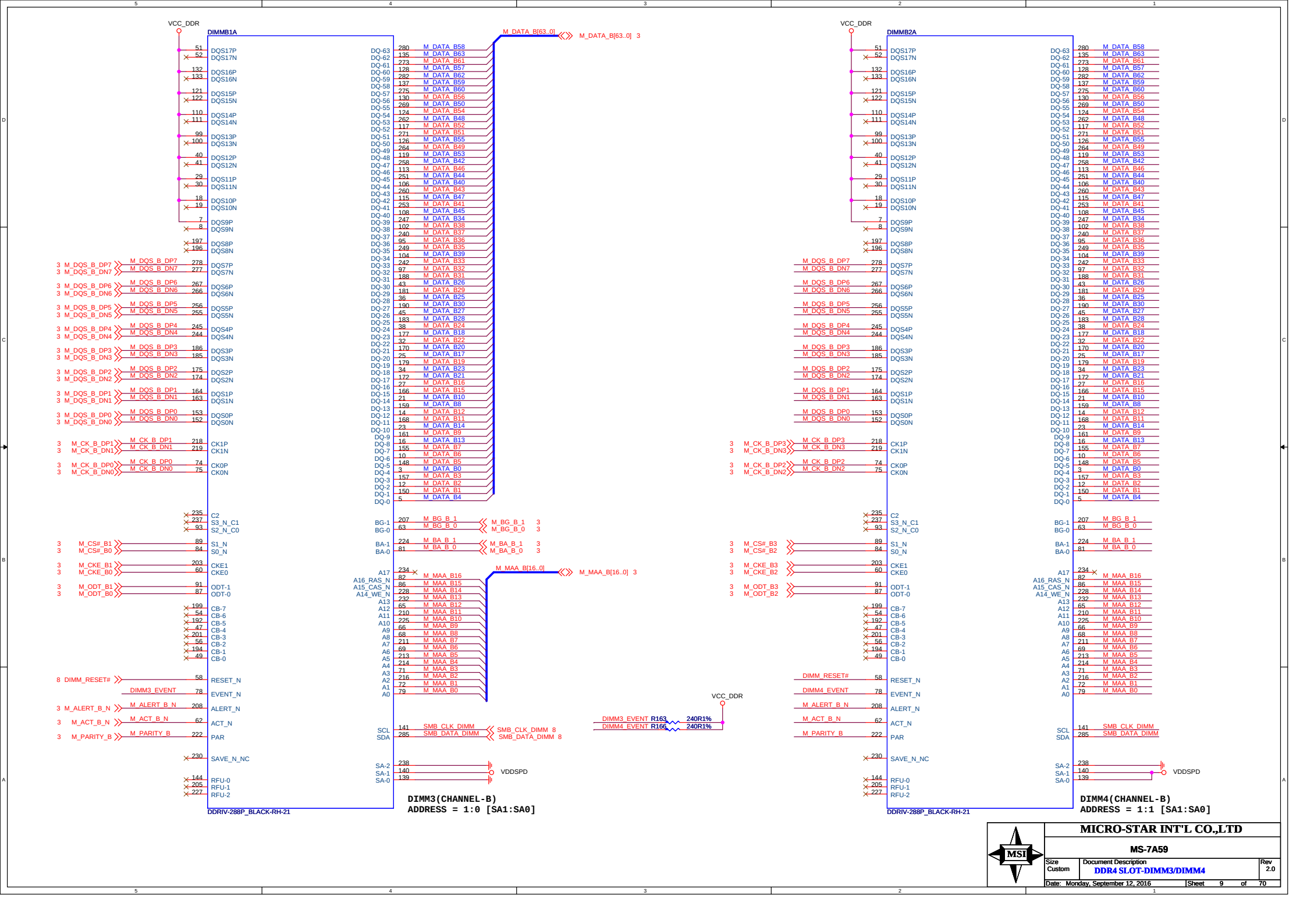
MS-7A59

Size	Document Description	Rev
Custom	DDR4 SLOT-DIMM1/DIMM2	2.0

Date: Monday, September 12, 2016 Sheet 8 of 70



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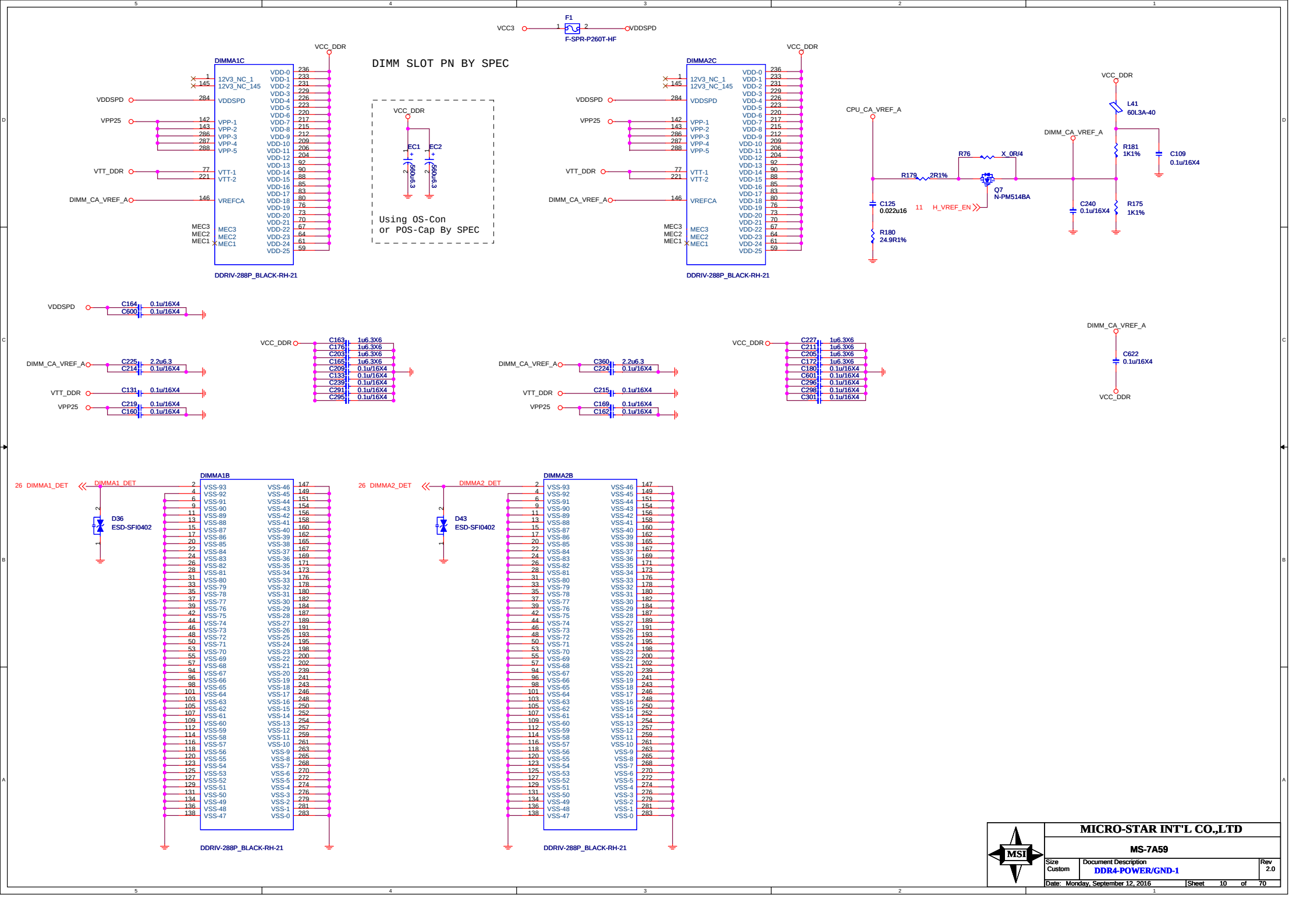
Rev: 2.0	
Date: Monday, September 12, 2016	Sheet 9 of 70


F1
VCC3
VDDSPD
F-SPR-P260T-HF
DIMM SLOT PN BY SPEC
DIMMA1C
DIMMA2C
VCC_DDR
VDDSPD
VPP25
VTT_DDR
DIMM_CA_VREF_A
DDRIV-288P_BLACK-RH-21
EC1
EC2
560u6.3
Using OS-Con
or POS-Cap By SPEC
CPU_CA_VREF_A
L41
60L3A-40
R181
1K1%
C109
0.1u/16X4
R76
X_0R/4
R179
2R1%
Q7
N-PM514BA
C125
0.022u16
11
H_VREF_EN
R180
24.9R1%
C240
0.1u/16X4
R175
1K1%
C164
C600
0.1u/16X4
C225
C214
2.2u6.3
C131
C219
C160
C163
C176
C203
C165
C209
C133
C239
C291
C295
1u6.3X6
C360
C224
C215
C169
C162
C227
C211
C205
C172
C180
C601
C296
C298
C301
C622
26 DIMMA1_DET
DIMMA1_DET
D36
ESD-SFI0402
DIMMA1B
26 DIMMA2_DET
DIMMA2_DET
D43
ESD-SFI0402
DIMMA2B
MICRO-STAR INT'L CO.,LTD
MS-7A59
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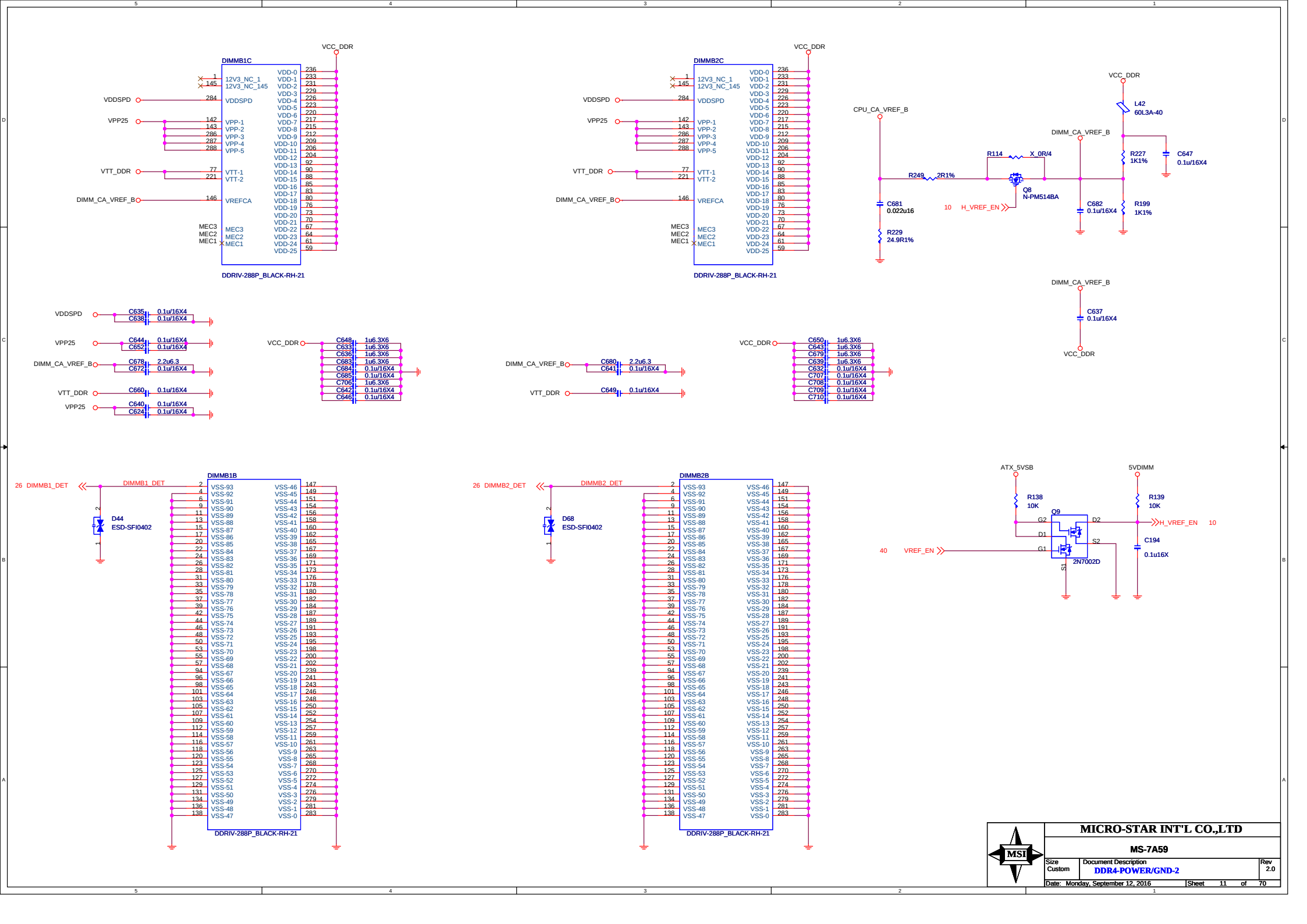
DDR4-POWER/GND-1
Rev
2.0
Date: Monday, September 12, 2016
Sheet 10 of 70



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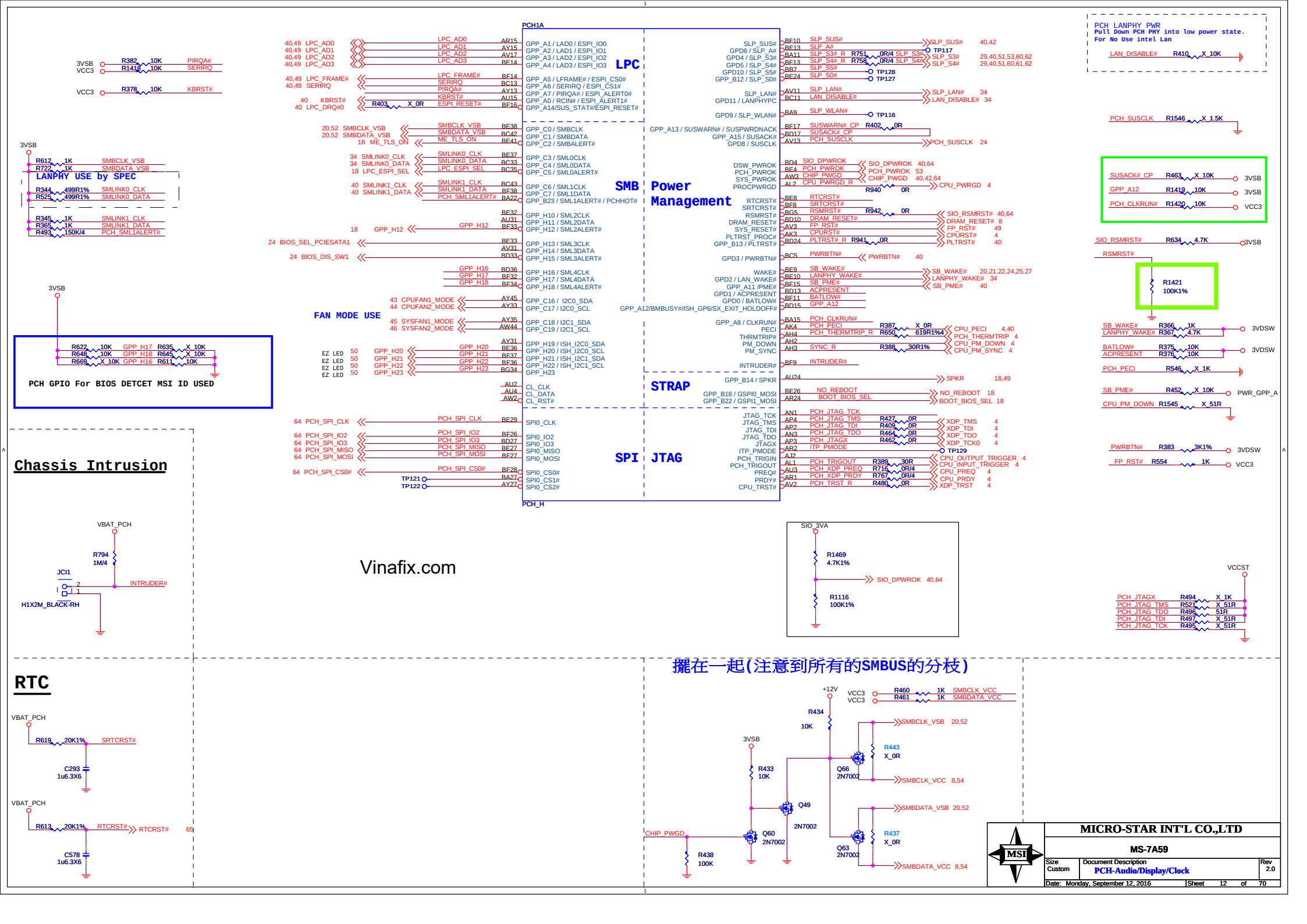
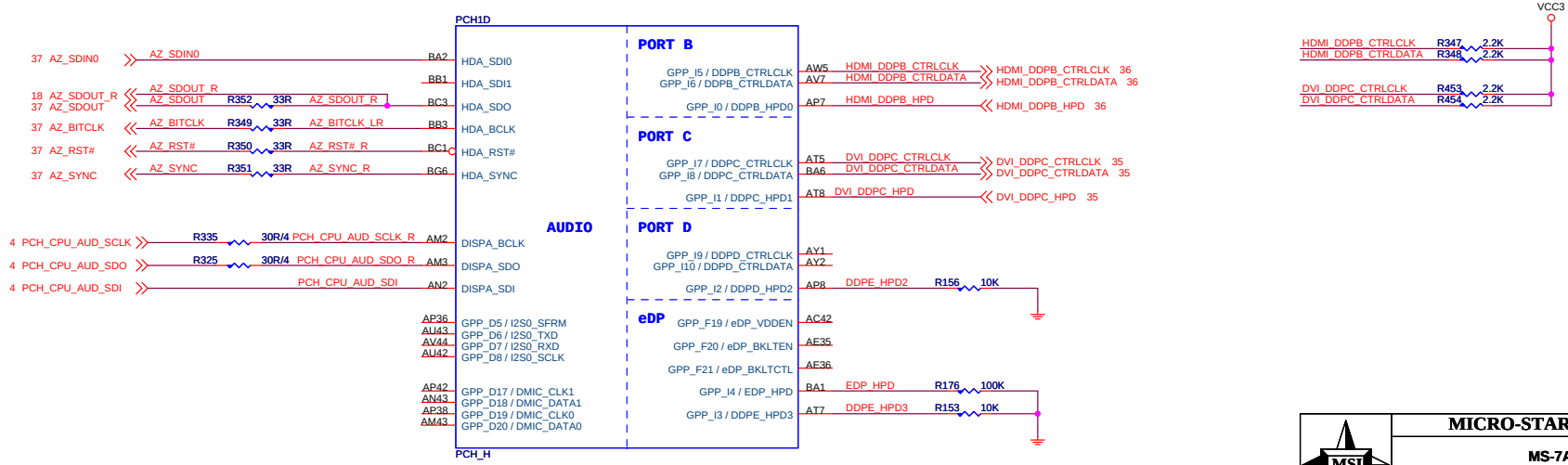
Date: Monday, September 12, 2016	Sheet 11 of 70	


PCH1A
LPC
SMB
Power Management
STRAP
SPI
JTAG
PCH_H
LANPHY USE by SPEC
FAN MODE USE
PCH GPIO For BIOS DETCET MSI ID USED
Chassis Intrusion
RTC
Vinafix.com
擺在一起(注意到所有的SMBUS的分枝)
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
MICRO-STAR INT'L CO.,LTD
MS-7A59
PCH-Audio/Display/Clock
Monday, September 12, 2016

PCH_CLK

RTC Block

Close to PCH



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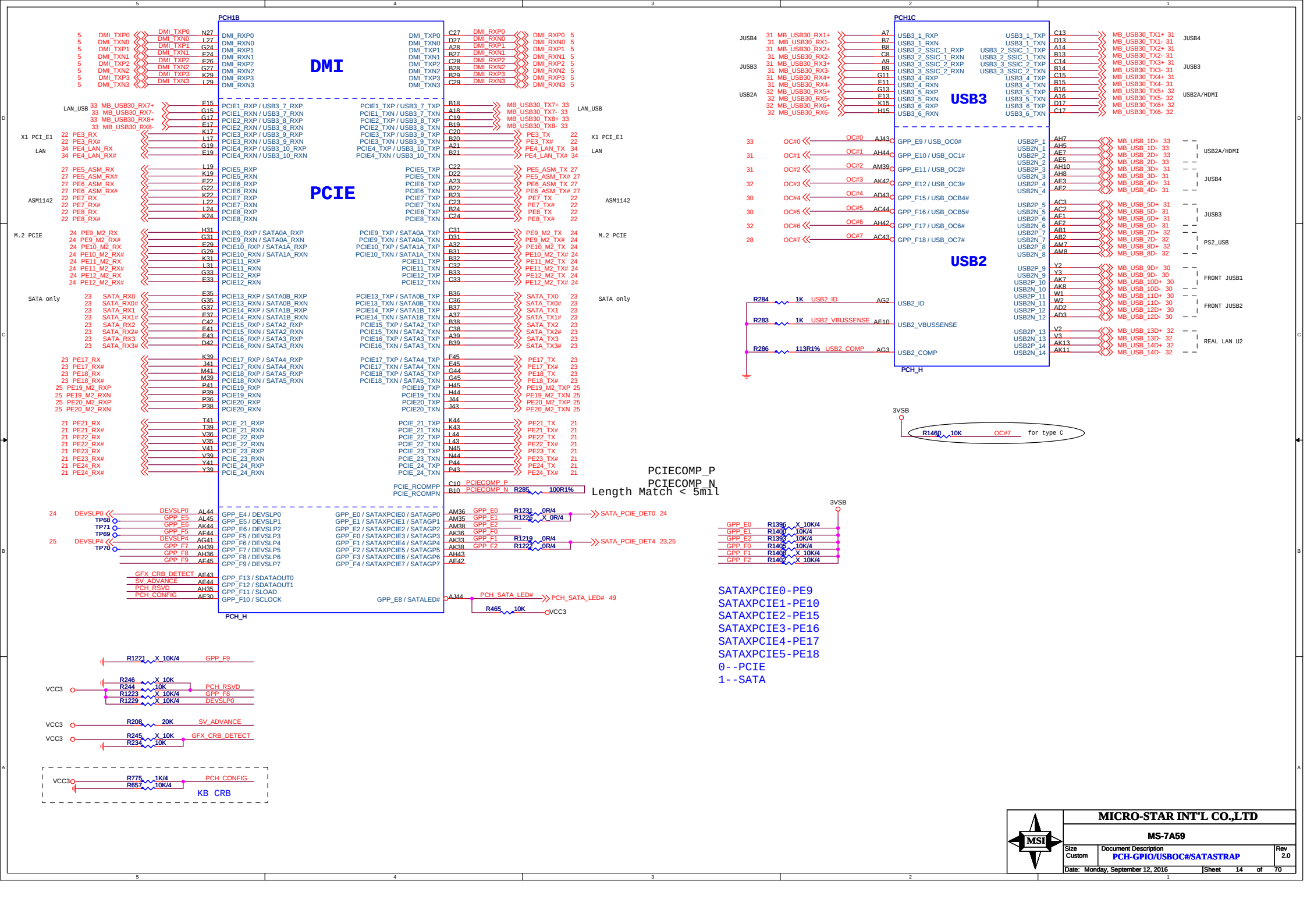
Date: Monday, September 12, 2016	Sheet 13 of 70	



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MS-7A59	
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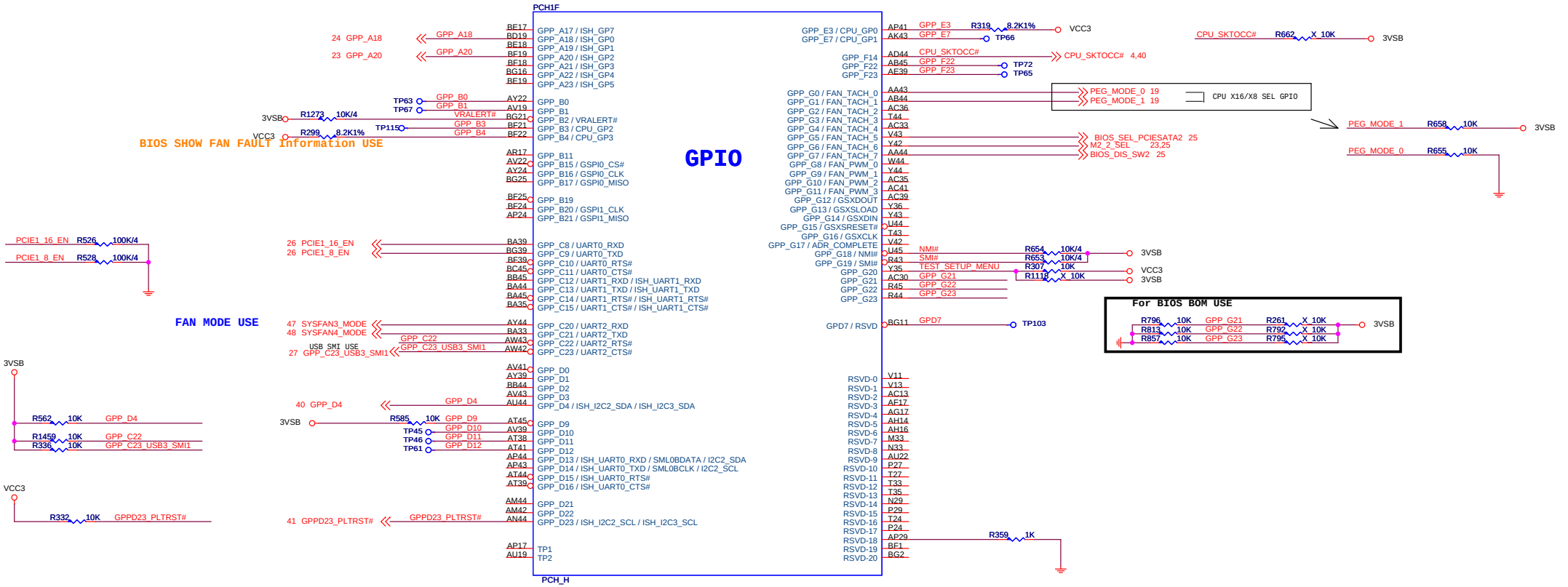
Rev: 2.0	
Date: Monday, September 12, 2016	Sheet 14 of 70



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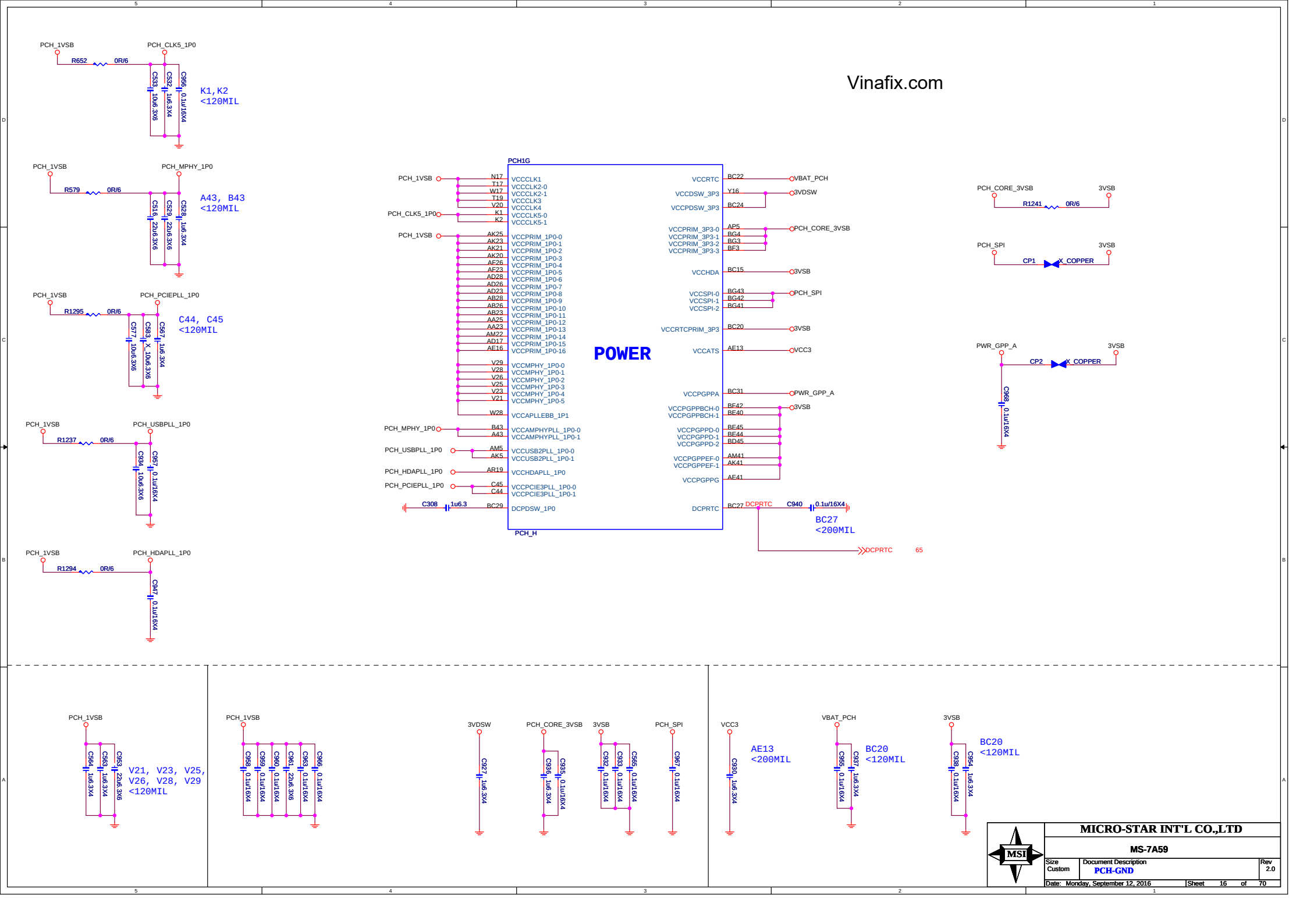
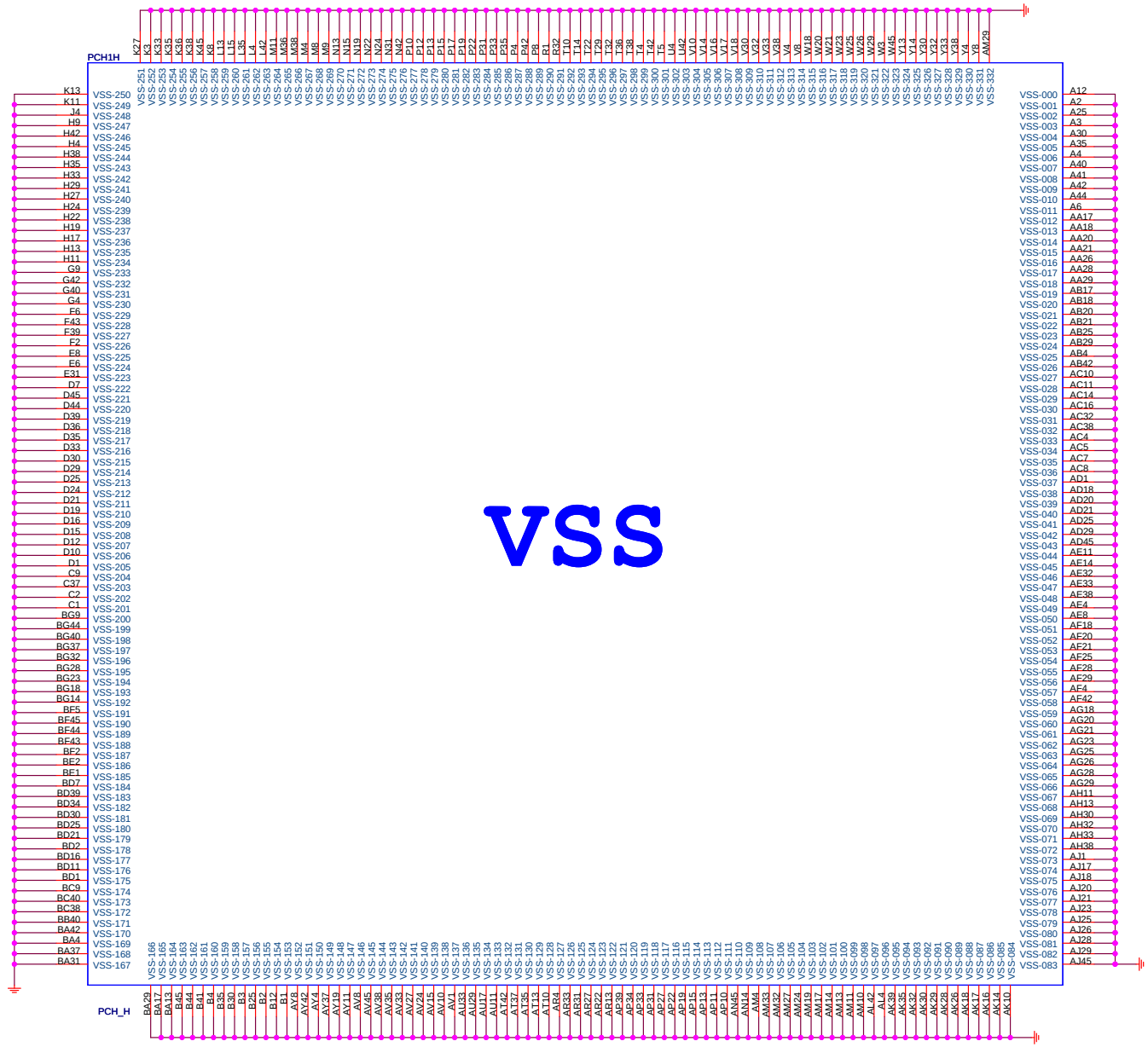
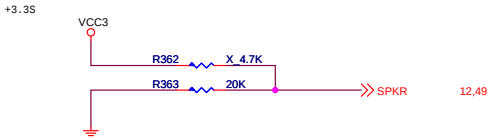
Date: Monday, September 12, 2016	Sheet 15 of 70	


Vinafix.com
PCH_1VSB
PCH_CLK5_1P0
R652
0R/6
C533
10u6.3X6
C532
1u6.3X4
C956
0.1u/16X4
K1,K2
<120MIL
PCH_1VSB
PCH_MPHY_1P0
R579
0R/6
C516
22u6.3X6
C529
22u6.3X6
C528
1u6.3X4
A43, B43
<120MIL
PCH_1VSB
PCH_PCIEPLL_1P0
R1295
0R/6
C577
10u6.3X6
C583
X_10u6.3X6
C567
1u6.3X4
C44, C45
<120MIL
PCH_1VSB
PCH_USBPLL_1P0
R1237
0R/6
C934
10u6.3X6
C957
0.1u/16X4
PCH_1VSB
PCH_HDAPLL_1P0
R1294
0R/6
C947
0.1u/16X4
PCH1G
POWER
PCH_H
PCH_1VSB
PCH_CLK5_1P0
PCH_1VSB
PCH_MPHY_1P0
PCH_USBPLL_1P0
PCH_HDAPLL_1P0
PCH_PCIEPLL_1P0
C308
1u6.3
VCCCLK1
VCCCLK2-0
VCCCLK2-1
VCCCLK3
VCCCLK4
VCCCLK5-0
VCCCLK5-1
VCCPRIM_1P0-0
VCCPRIM_1P0-1
VCCPRIM_1P0-2
VCCPRIM_1P0-3
VCCPRIM_1P0-4
VCCPRIM_1P0-5
VCCPRIM_1P0-6
VCCPRIM_1P0-7
VCCPRIM_1P0-8
VCCPRIM_1P0-9
VCCPRIM_1P0-10
VCCPRIM_1P0-11
VCCPRIM_1P0-12
VCCPRIM_1P0-13
VCCPRIM_1P0-14
VCCPRIM_1P0-15
VCCPRIM_1P0-16
VCCMPHY_1P0-0
VCCMPHY_1P0-1
VCCMPHY_1P0-2
VCCMPHY_1P0-3
VCCMPHY_1P0-4
VCCMPHY_1P0-5
VCCAPLLEBB_1P1
VCCAMPHYPLL_1P0-0
VCCAMPHYPLL_1P0-1
VCCUSB2PLL_1P0-0
VCCUSB2PLL_1P0-1
VCCHDAPLL_1P0
VCCPCIE3PLL_1P0-0
VCCPCIE3PLL_1P0-1
DCPDSW_1P0
VCCRTC
VCCDSW_3P3
VCCPDSW_3P3
VCCPRIM_3P3-0
VCCPRIM_3P3-1
VCCPRIM_3P3-2
VCCPRIM_3P3-3
VCCHDA
VCCSPI-0
VCCSPI-1
VCCSPI-2
VCCRTCPRIM_3P3
VCCATS
VCCPGPPA
VCCPGPPBCH-0
VCCPGPPBCH-1
VCCPGPPD-0
VCCPGPPD-1
VCCPGPPD-2
VCCPGPPEF-0
VCCPGPPEF-1
VCCPGPPG
DCPRTC
VBAT_PCH
3VDSW
PCH_CORE_3VSB
3VSB
PCH_SPI
VCC3
DCPRTC
C940
0.1u/16X4
BC27
<200MIL
DCPRTC
65
PCH_CORE_3VSB
3VSB
R1241
0R/6
PCH_SPI
3VSB
CP1
X_COPPER
PWR_GPP_A
3VSB
CP2
X_COPPER
C968
0.1u/16X4
PCH_1VSB
C564
1u6.3X4
C563
1u6.3X4
C953
22u6.3X6
V21, V23, V25,
V26, V28, V29
<120MIL
PCH_1VSB
C958
0.1u/16X4
C959
0.1u/16X4
C960
0.1u/16X4
C961
22u6.3X6
C963
0.1u/16X4
C966
0.1u/16X4
3VDSW
C927
1u6.3X4
PCH_CORE_3VSB
C936
1u6.3X4
C935
0.1u/16X4
3VSB
C932
0.1u/16X4
C933
0.1u/16X4
C965
0.1u/16X4
PCH_SPI
C967
0.1u/16X4
VCC3
C930
1u6.3X4
AE13
<200MIL
VBAT_PCH
C955
0.1u/16X4
C937
1u6.3X4
BC20
<120MIL
3VSB
C938
0.1u/16X4
C954
1u6.3X4
BC20
<120MIL
MSI
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size
Custom
Document Description
PCH-GND
Rev
2.0
Date: Monday, September 12, 2016
Sheet 16 of 70



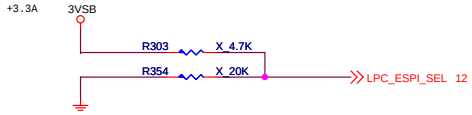
MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: PCH-Power
Rev: 2.0	
Date: Monday, September 12, 2016	Sheet 17 of 70

TOP Swap



Internal pull-down is disabled after PLTRST#

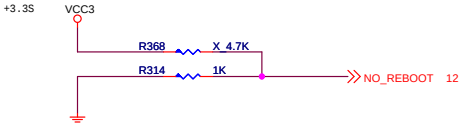
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

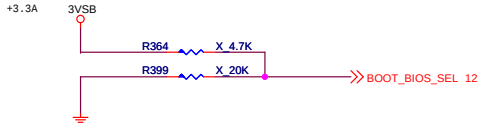
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

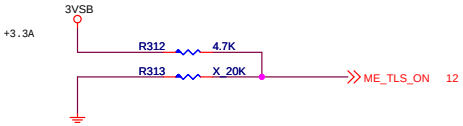
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

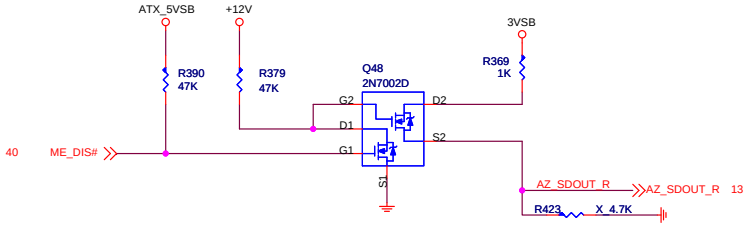
AMT and SBA with confidentiality



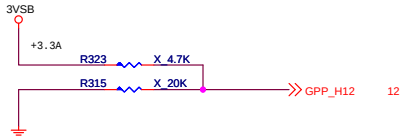
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



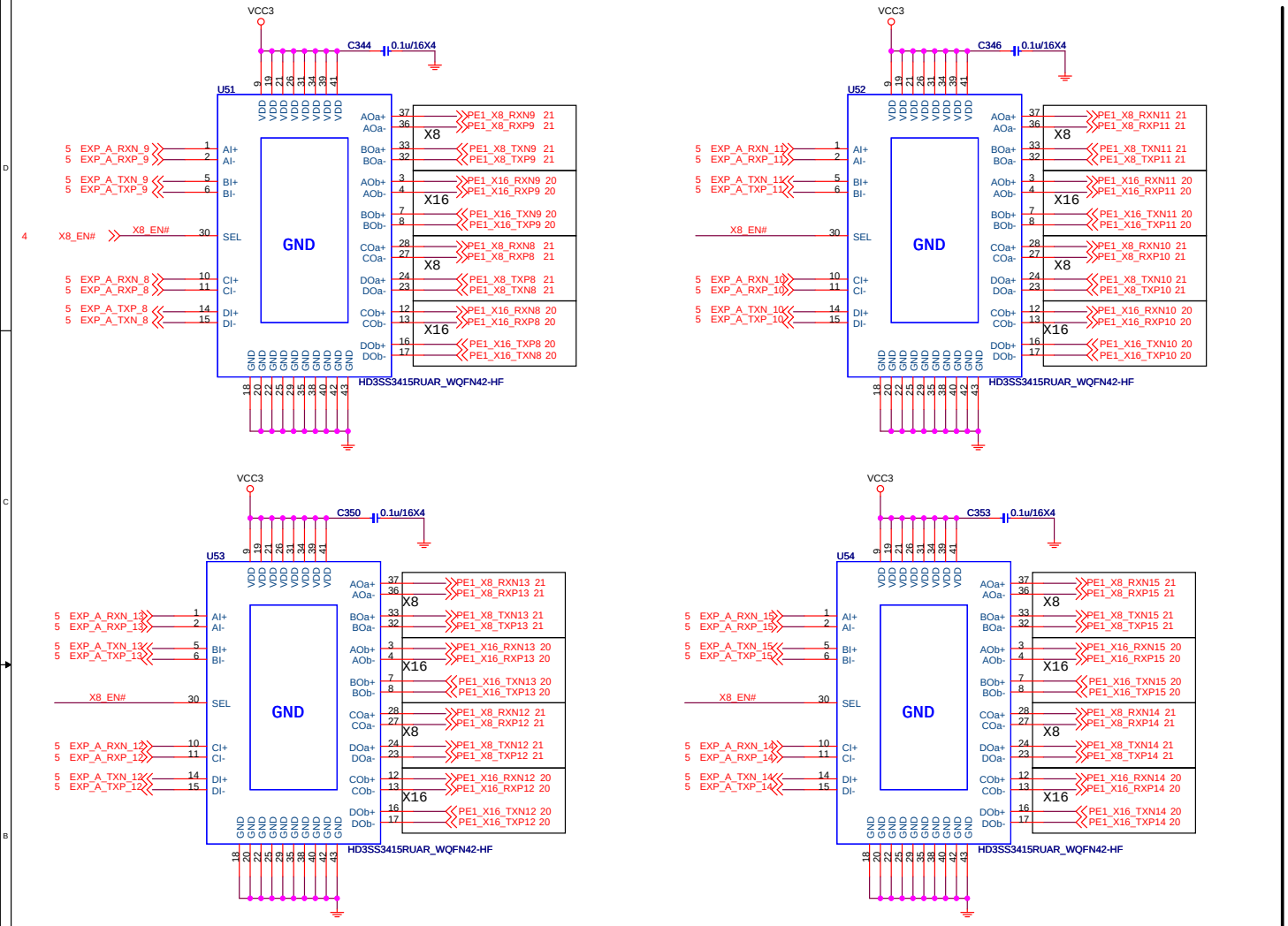
ESPI FLASH SHARING MODE



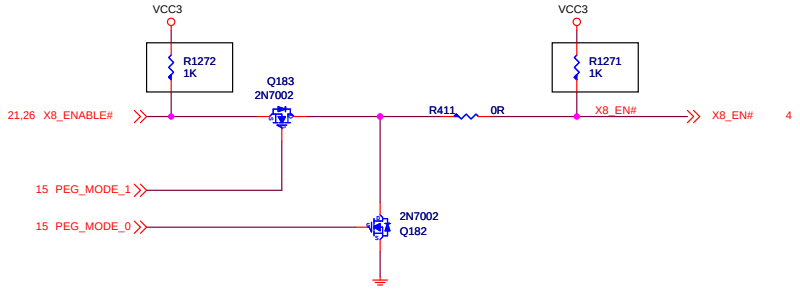
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: PCH-Strap	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 18 of 70	



Vinafix.com



MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

MODE_1/3

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0/2	MODE_1
AUTO	0	1

MICRO-STAR INT'L CO.,LTD

MS-7A59

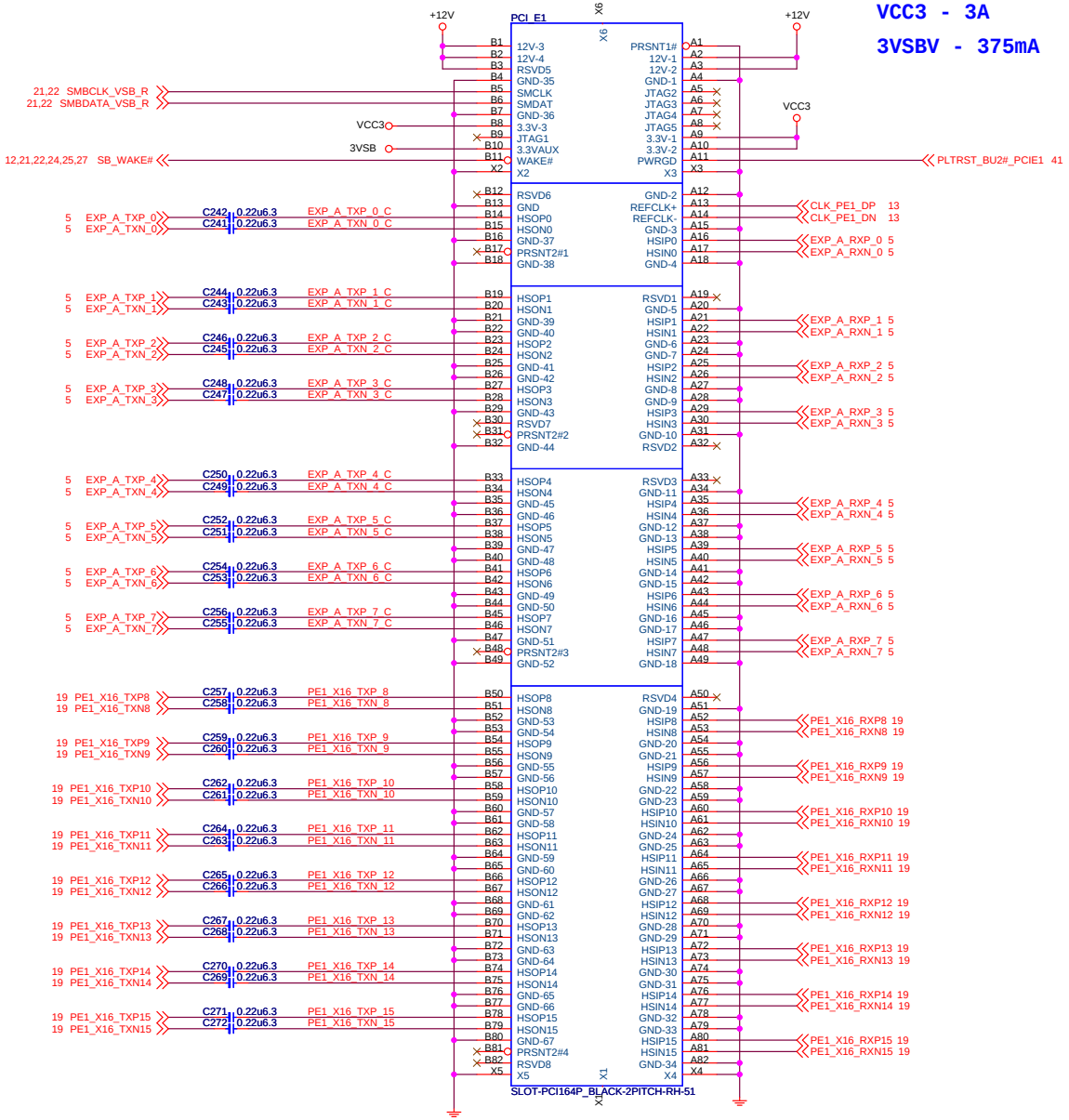
Size: Custom | Document Description: PCIE SWITCH | Rev: 2.0

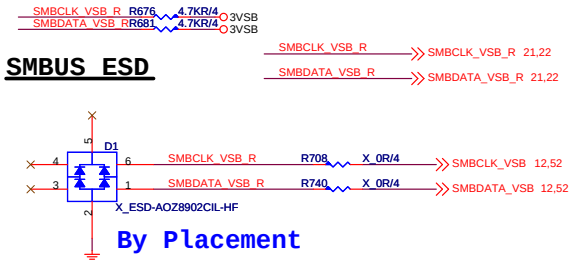
Date: Monday, September 12, 2016 | Sheet 19 of 70

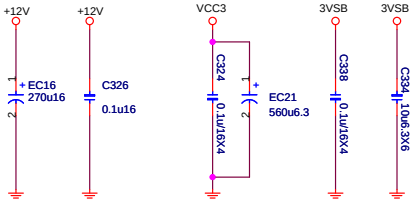
12V - 5.5A

VCC3 - 3A

3VSBV - 375mA



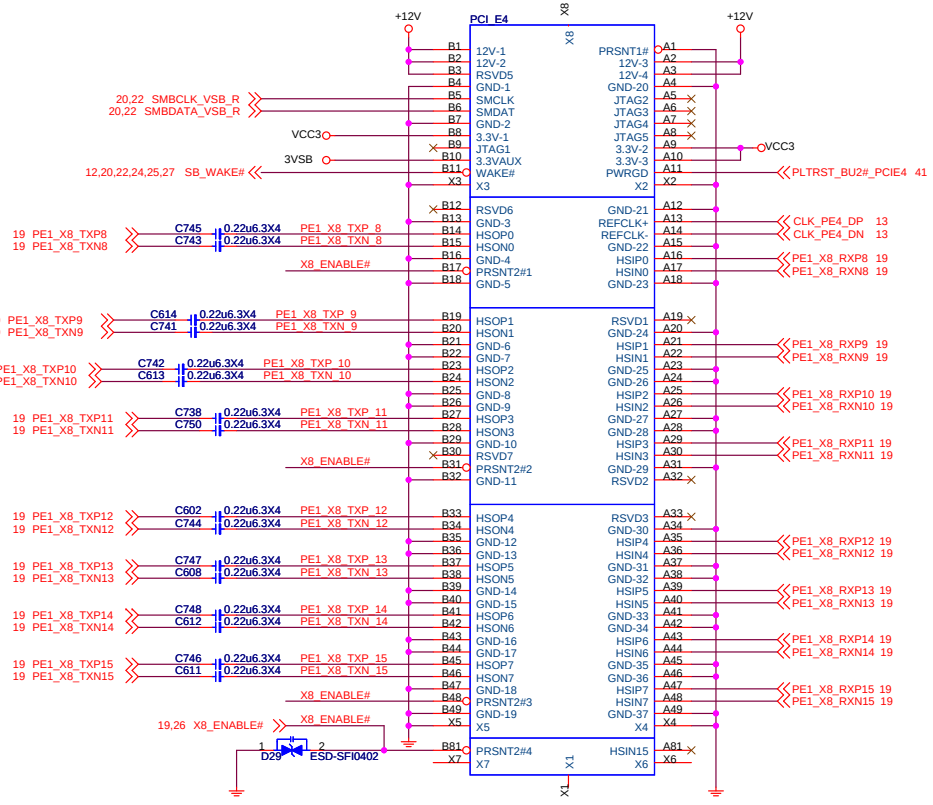


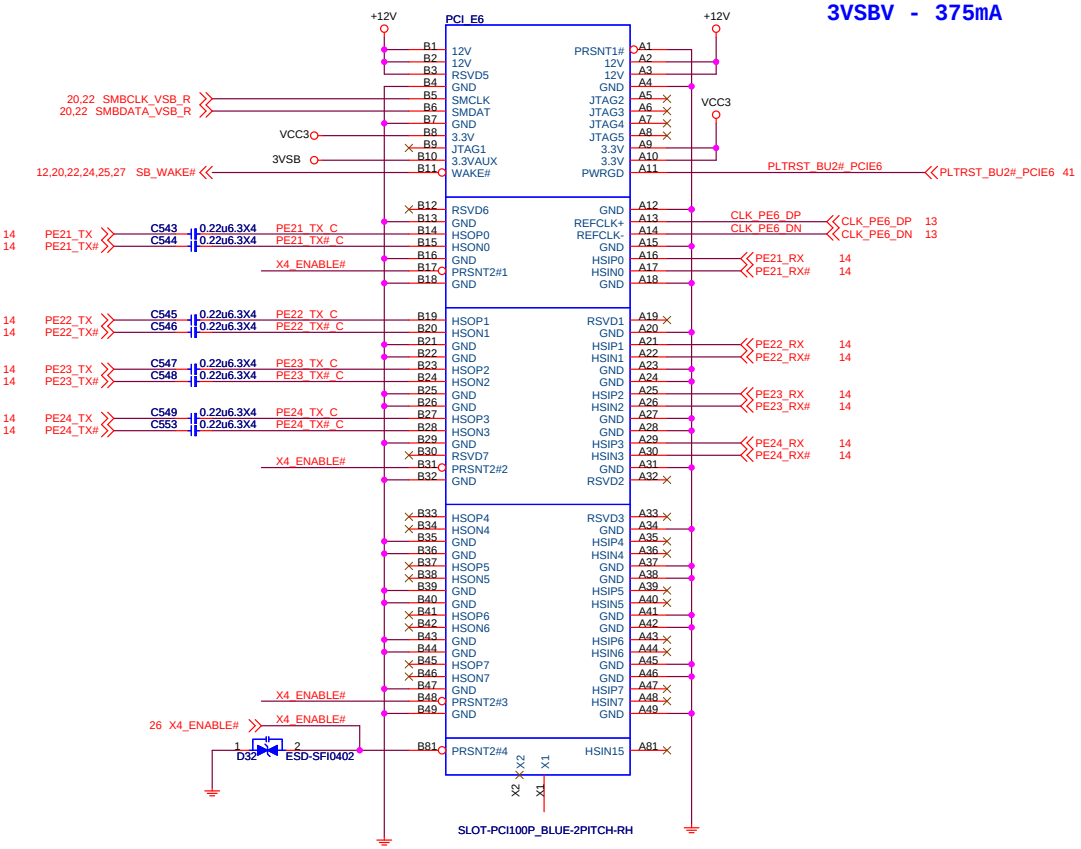


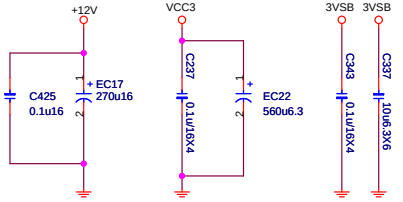
MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 2.0	
Date: Monday, September 12, 2016	Sheet 20 of 70

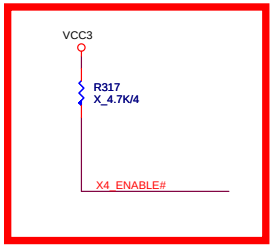
PCI_Express X4 Slot

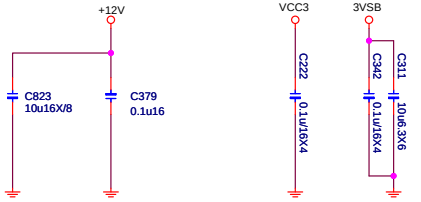
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA



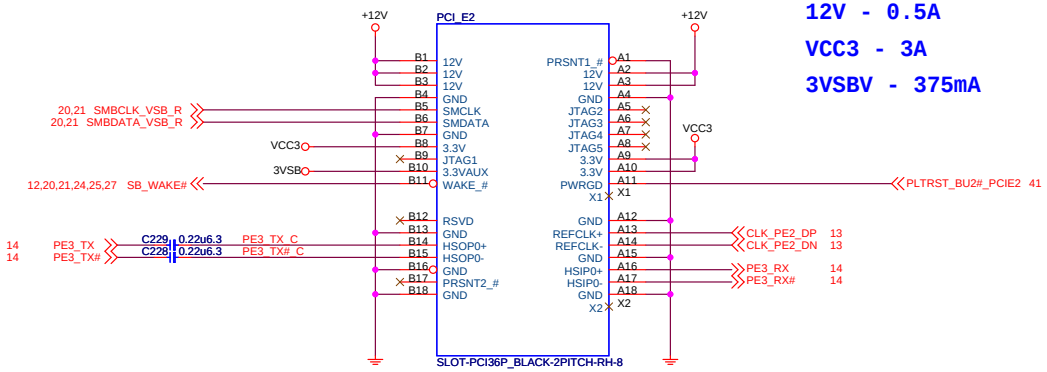




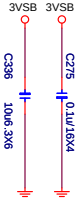


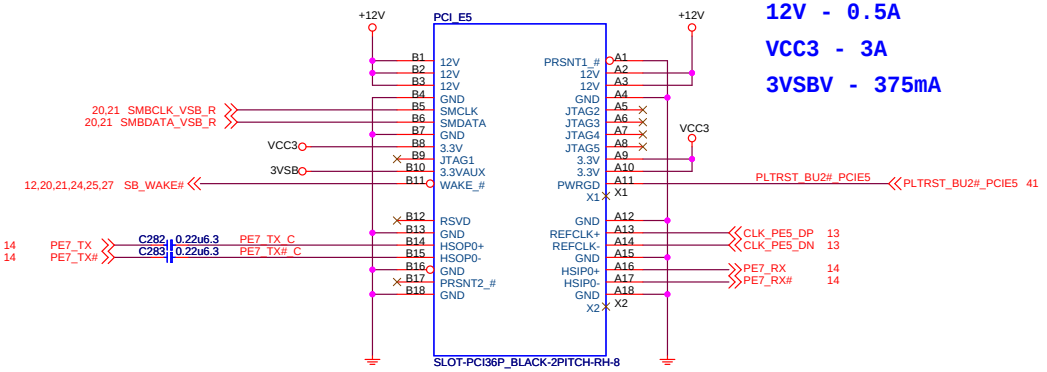


MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: PCIE SLOT (X4)	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 21 of 70	

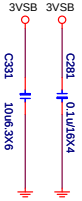


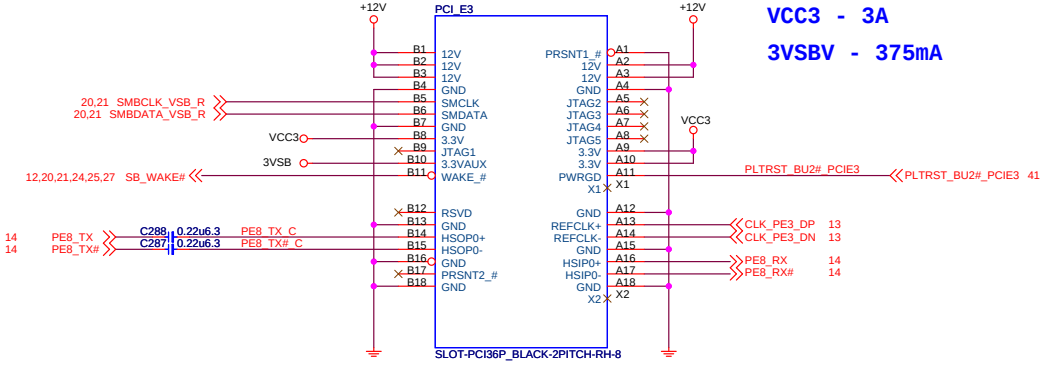
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



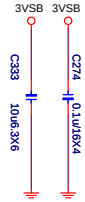


12V - 0.5A
VCC3 - 3A
3VSBV - 375mA





12V - 0.5A
VCC3 - 3A
3VSBV - 375mA

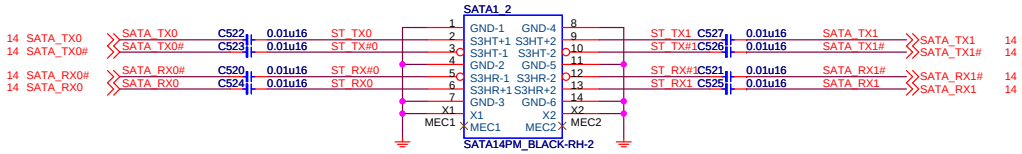


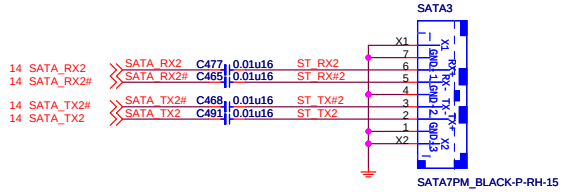
MICRO-STAR INT'L CO.,LTD

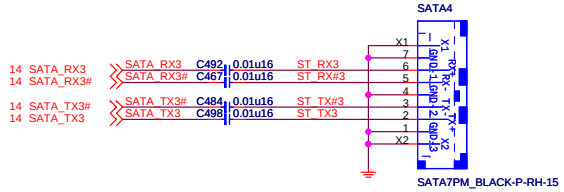
MS-7A59

Size	Document Description	Rev
Custom	PCIE SLOT (X1)	2.0

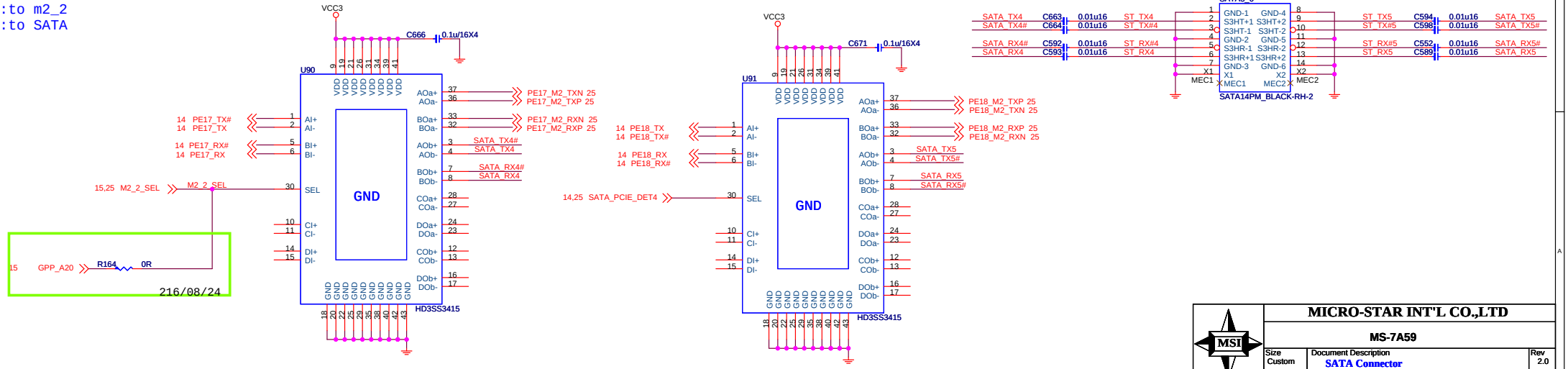
Date: Monday, September 12, 2016 | Sheet 22 of 70



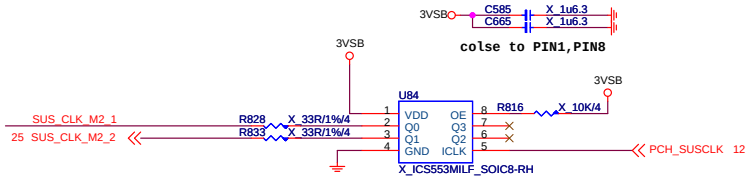


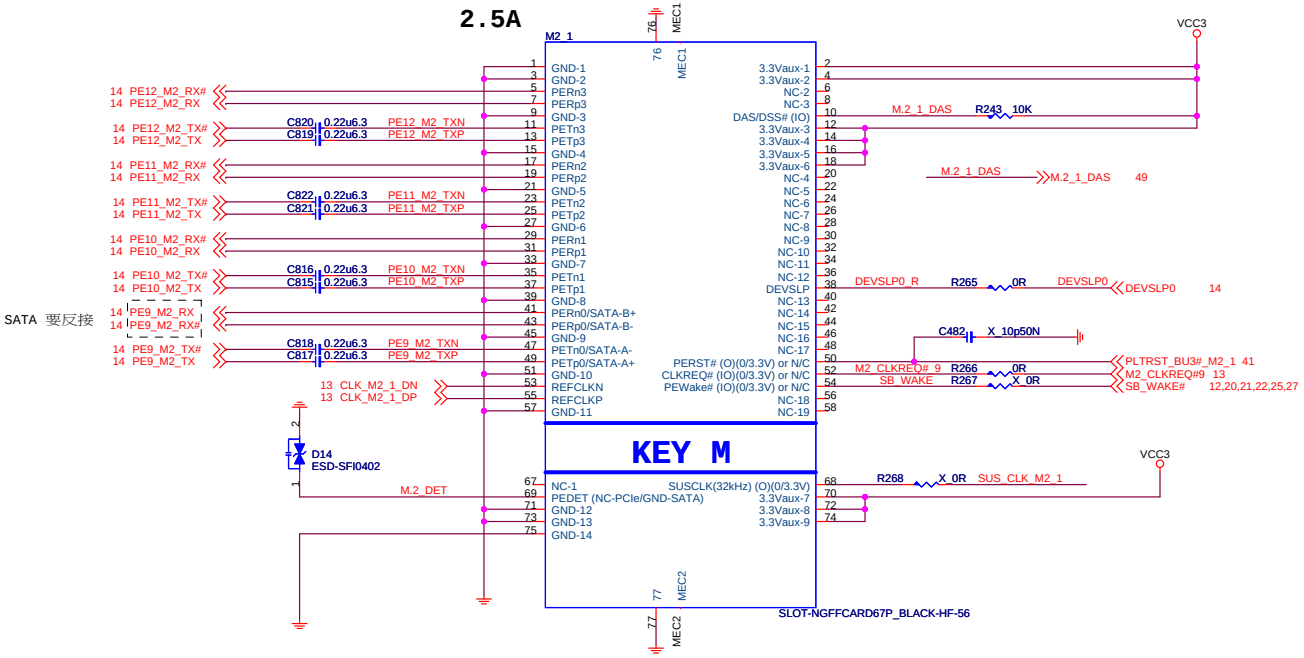


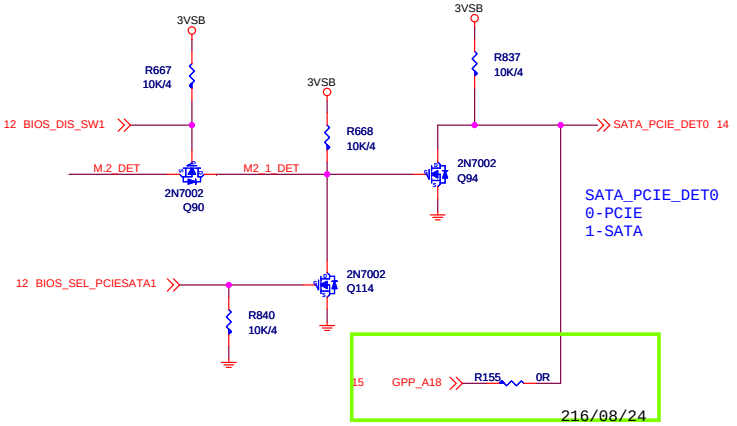
M2_2_SEL
0:to m2_2
1:to SATA



MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: SATA Connector	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 23 of 70	

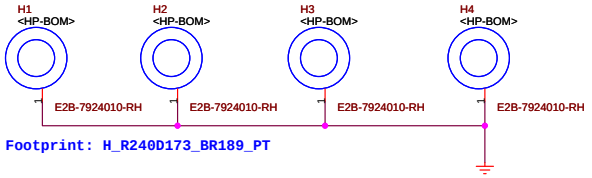


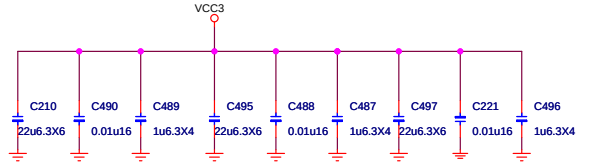




BIOS_MODE

BIOS_DIS_SW	*BIOS_SEL_PCIESATA1*	*Mode*
0	*1*	*M2-SATA*
0	*0*	*M2-PCIE*
GPI	*GPI*	*AUTO*



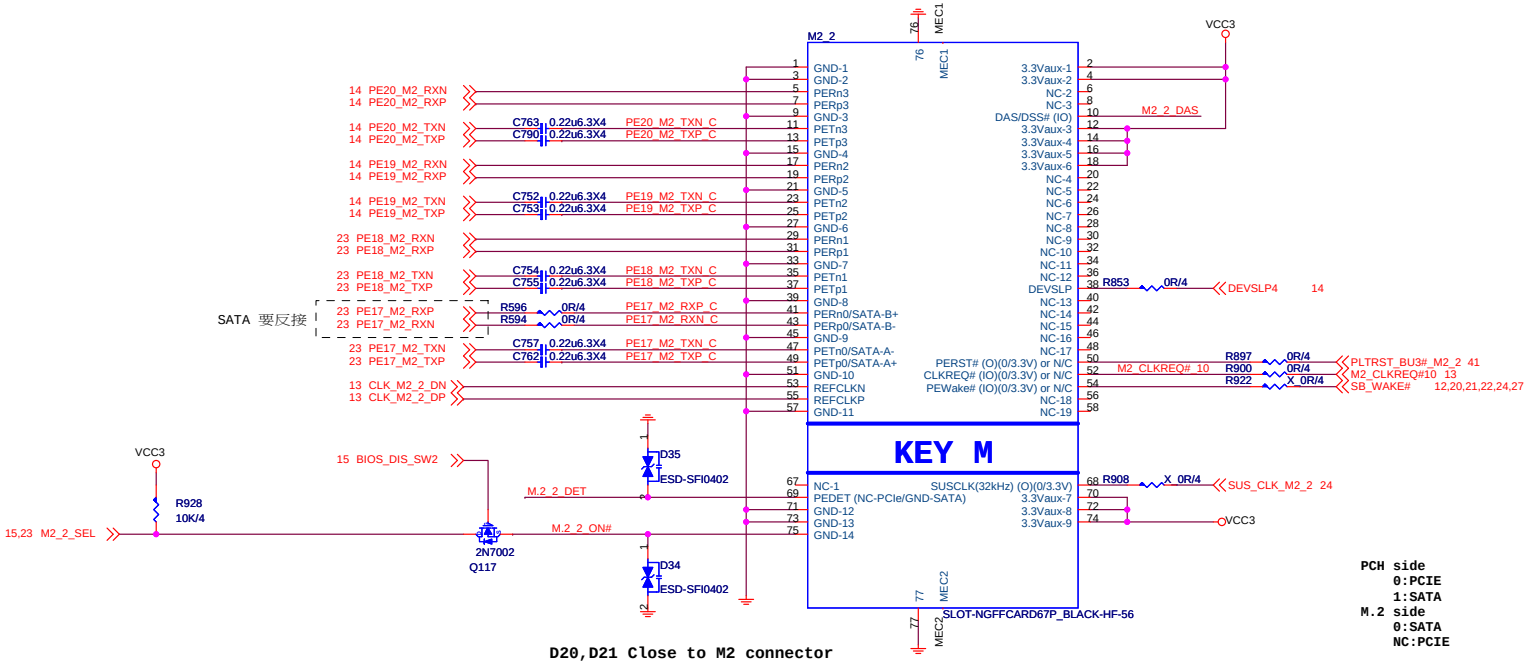


MICRO-STAR INT'L CO.,LTD

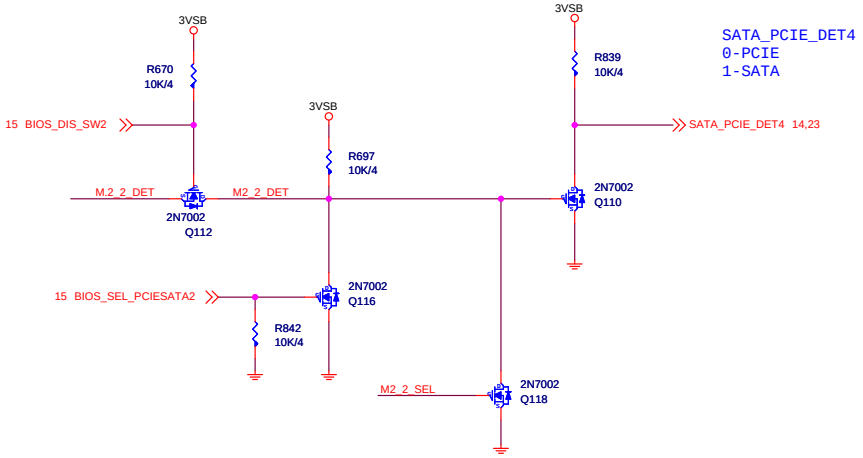
MS-7A59

Size	Document Description	Rev
Custom	M.2-SLOT1	2.0

Date: Monday, September 12, 2016 | Sheet 24 of 70

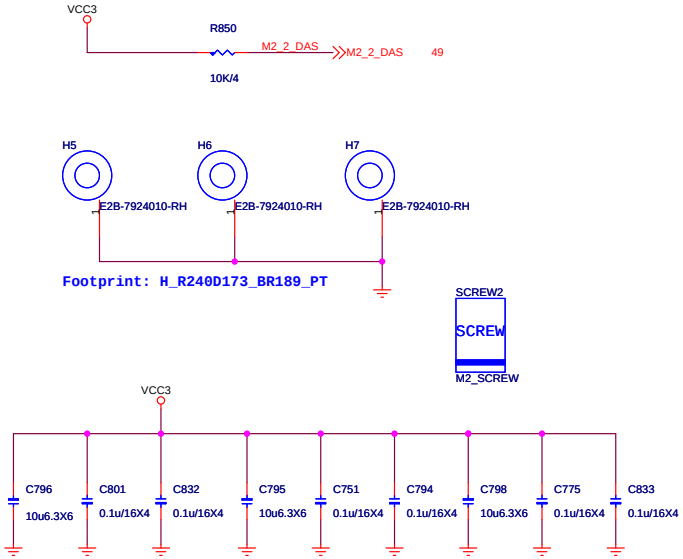


D20,D21 Close to M2 connector



BIOS_MODE

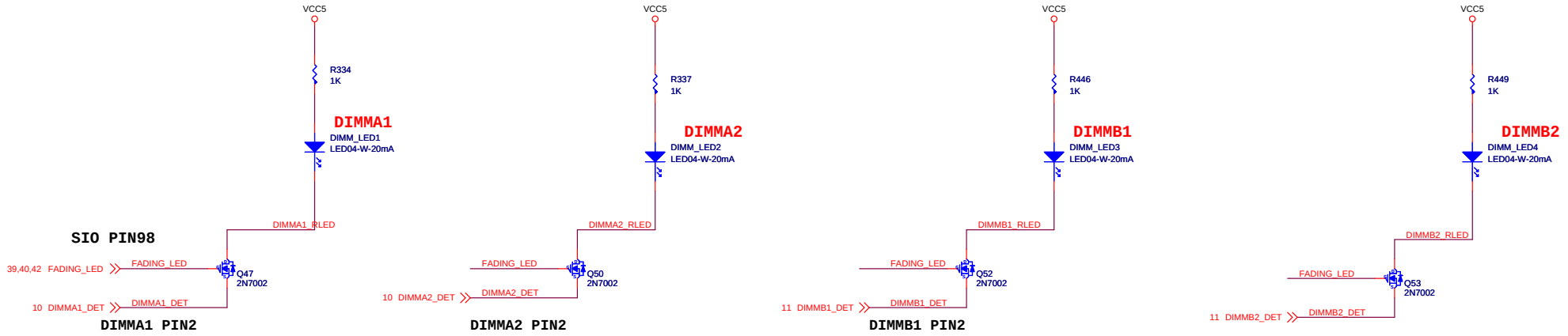
BIOS_DIS_SW	*M2_2_SEL*	*BIOS_SEL_PCIESATA2*	*Mode*
GPI(1)	*GPI(1)*	*GPI(0)*	*AUTO*
0	*1*	*0*	*SATA*
0	*0*	*1*	*M2-SATA*
0	*0*	*0*	*M2-PCIE*



MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: M.2-SLOT2	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 25 of 70	

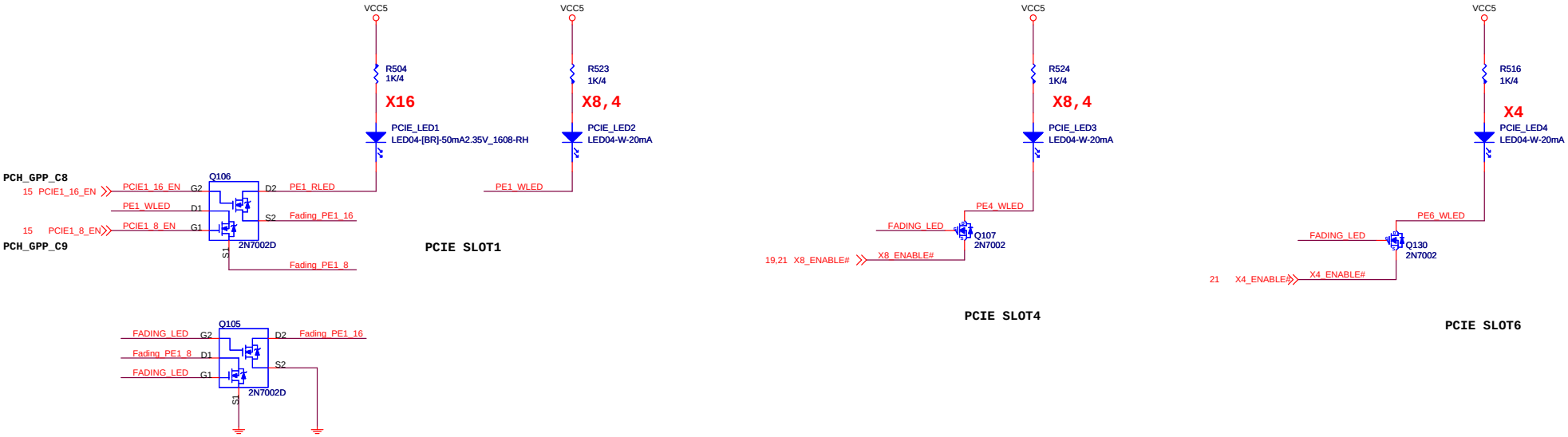
DIMM_SLOT

KRAIT GAMING LED >>WHITE:DOC-040S200-E07



LED 命名請以DIMM_LEDn n為數字

PCIE SLOT LED



MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: M.2-SLOT3	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 26 of 70	

Minimun gap should be greater of
>15mil with other signal.

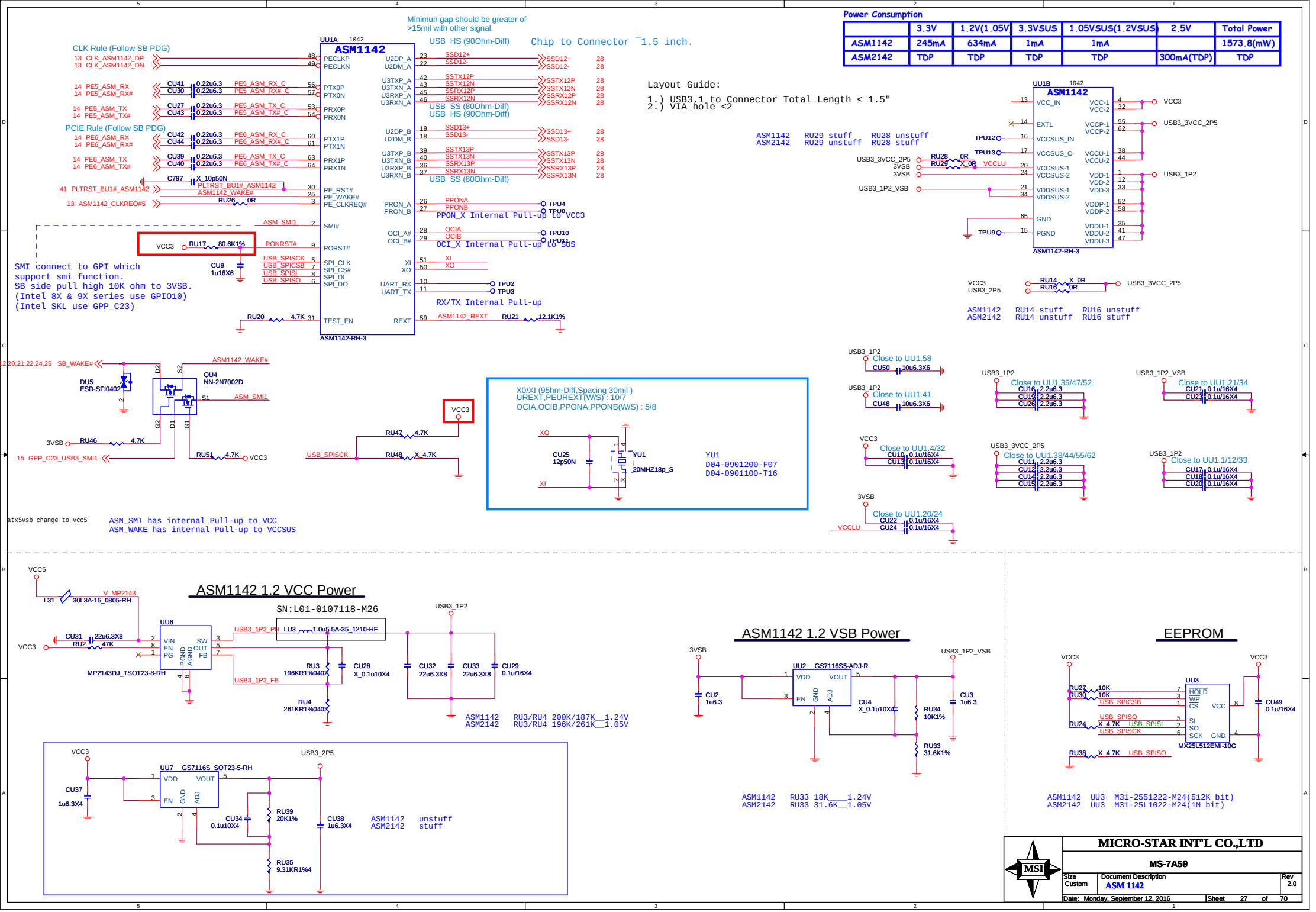
USB HS (90Ohm-Diff) Chip to Connector 1.5 inch.

Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA		1573.8(mW)
ASM2142	TDP	TDP	TDP	TDP	300mA(TDP)	TDP

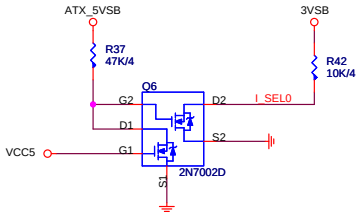
Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2



MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: ASM 1142
Rev: 2.0	
Date: Monday, September 12, 2016	Sheet 27 of 70

Current Mode

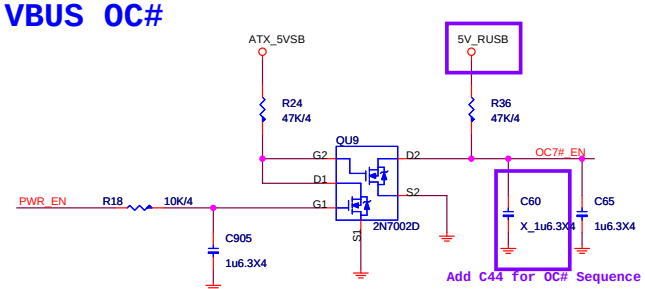


I_SEL0 : I_SEL1

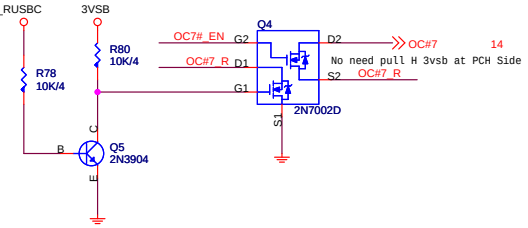
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

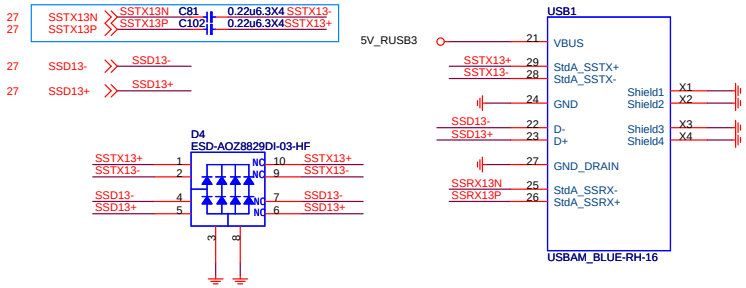
VBUS OC#

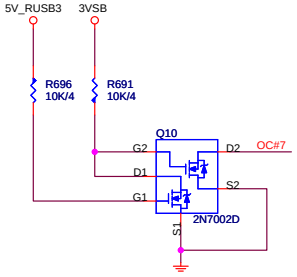


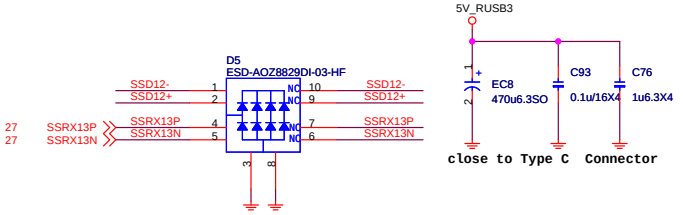
Add C44 for OC# Sequence



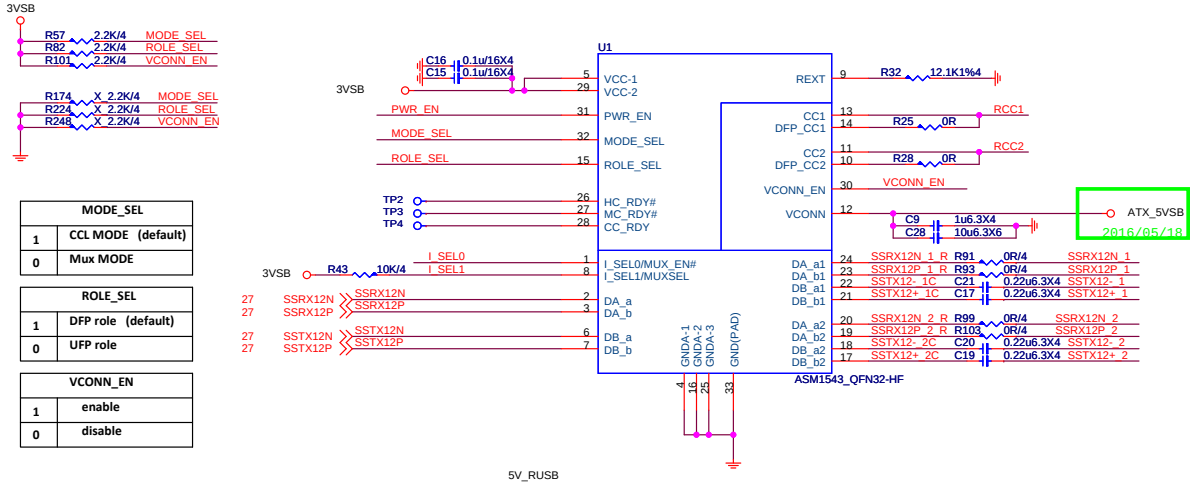
TYPE-A







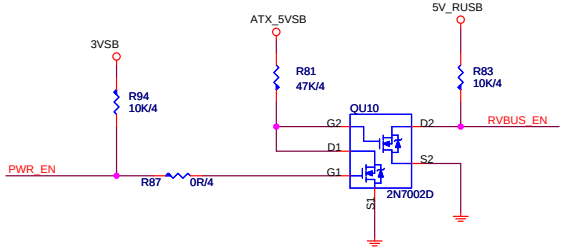
USB Type-C MUX with Configuration Channel (CC)

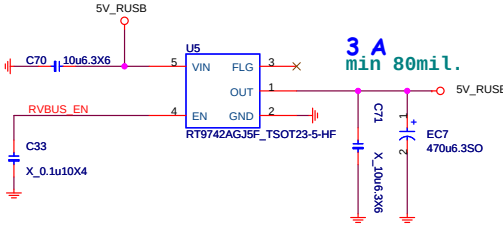


MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

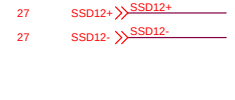
VCONN_EN	
1	enable
0	disable



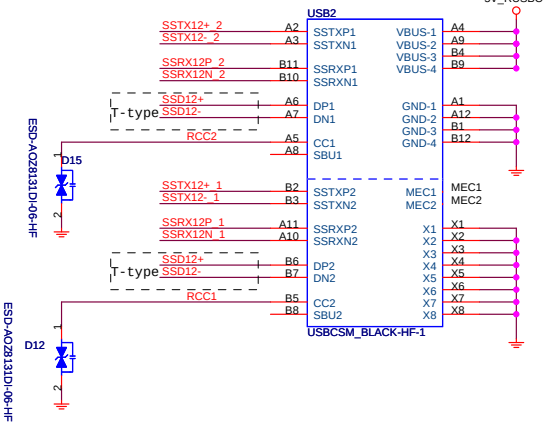


3 A
min 80mil.

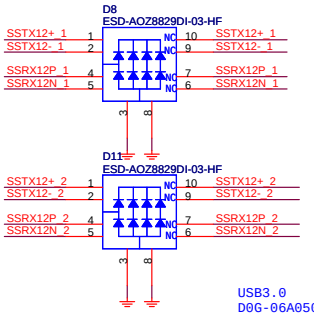
TYPE-C



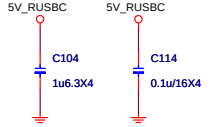
T-type 分支需小於140mils



ESD Protection
NEAR CONNECTOR



close to Type C Connector



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL

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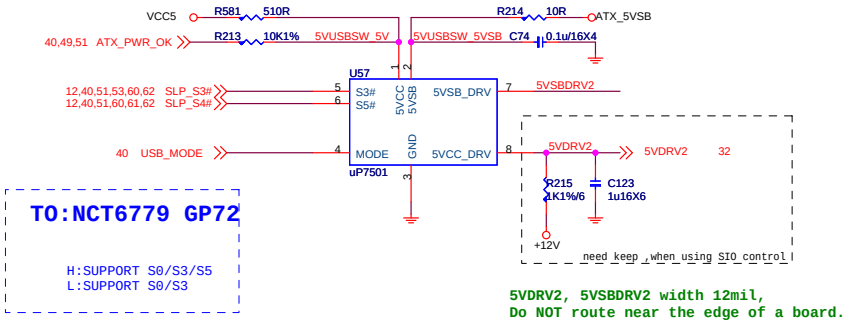
MS-7A59

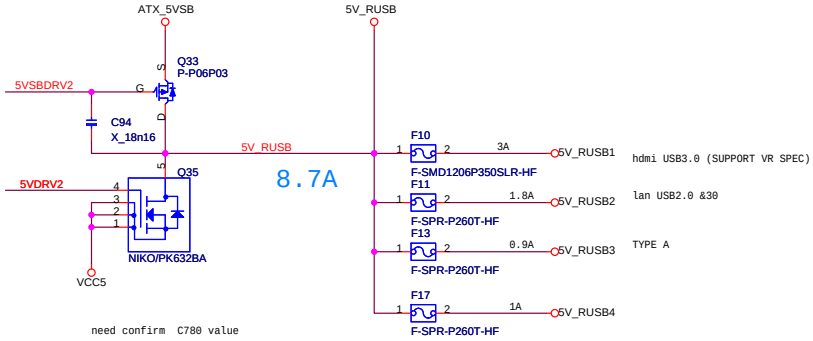
Size	Document Description	Rev
Custom	USB TYPE C	2.0

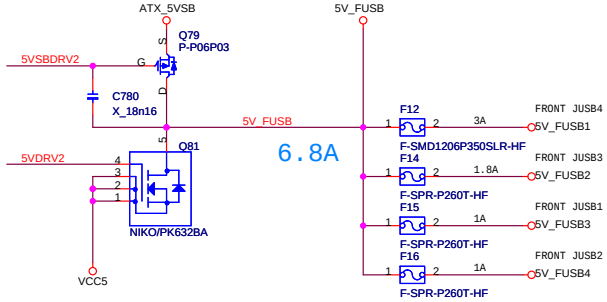
Date: Monday, September 12, 2016 Sheet 28 of 70

USB PORT POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



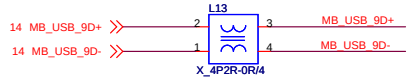


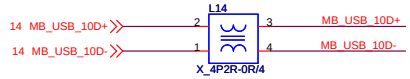
P-MOS
D03-06P0319-N03

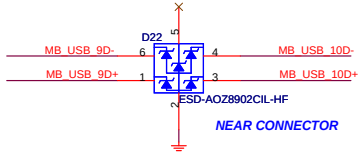
N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)

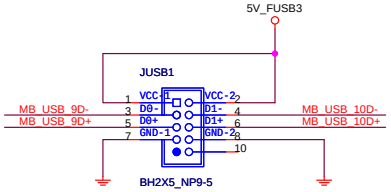
MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: USB POWER UP7501	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 29 of 70	



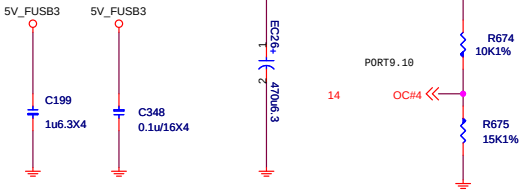


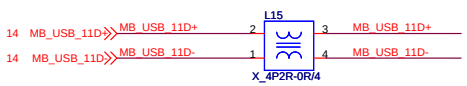


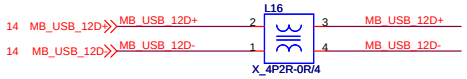
1.0A

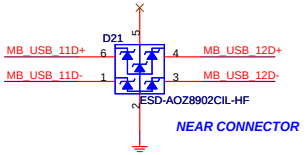


EMI Cap near Connector.

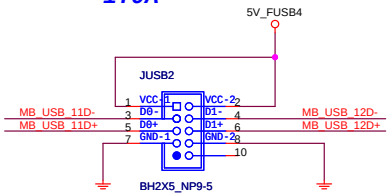




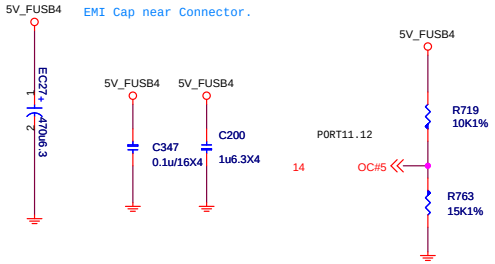




1.0A



EMI Cap near Connector.



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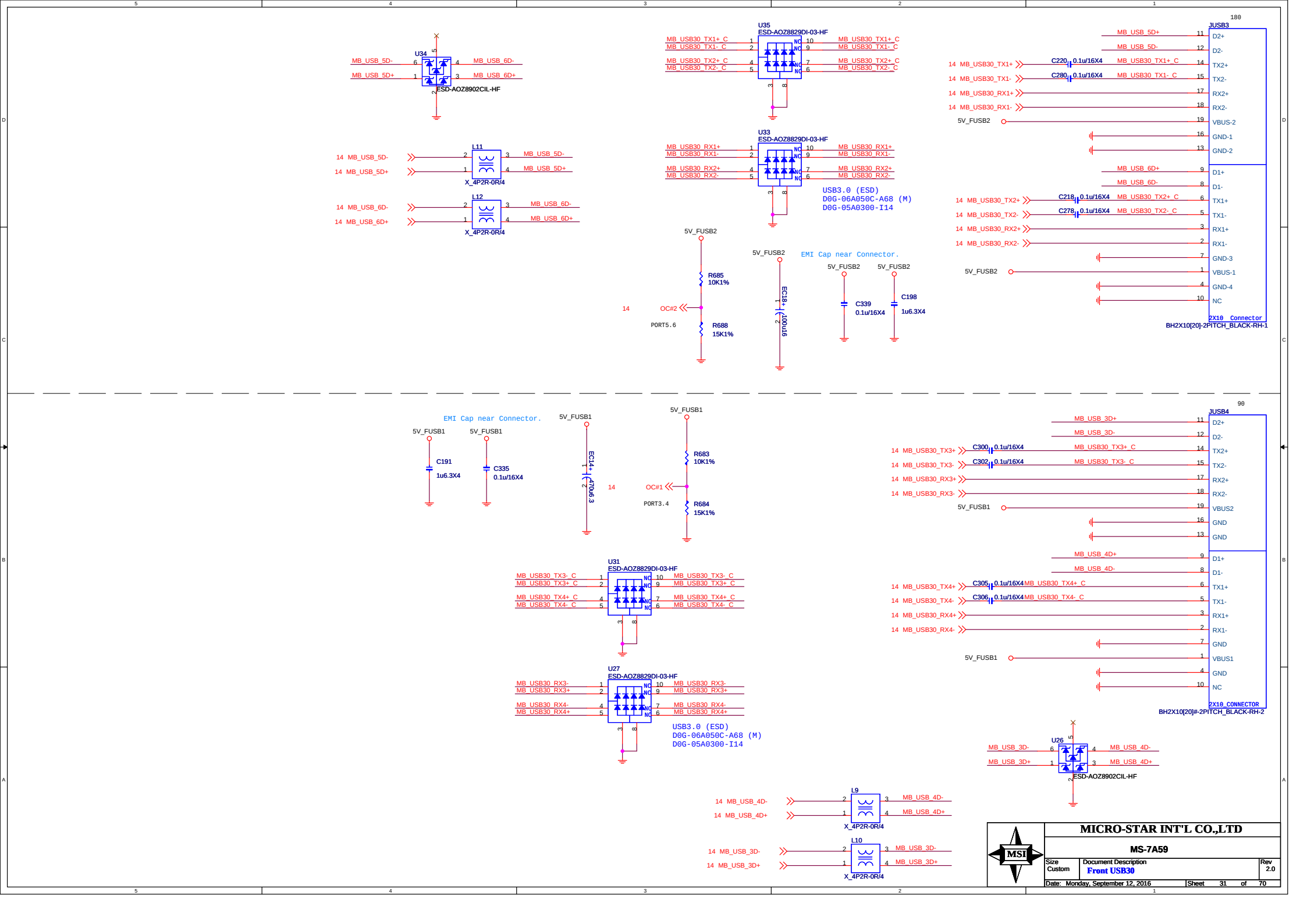
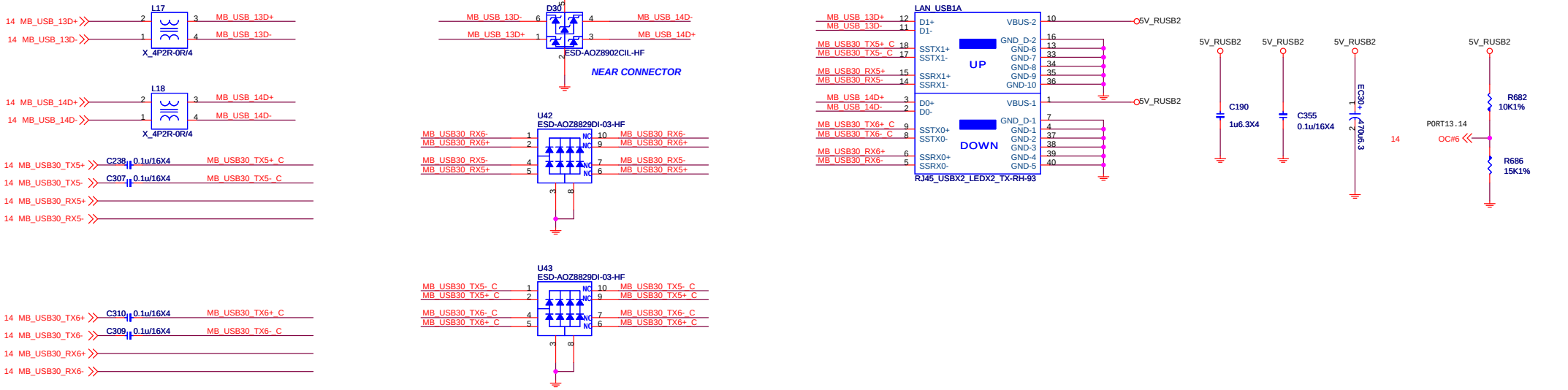
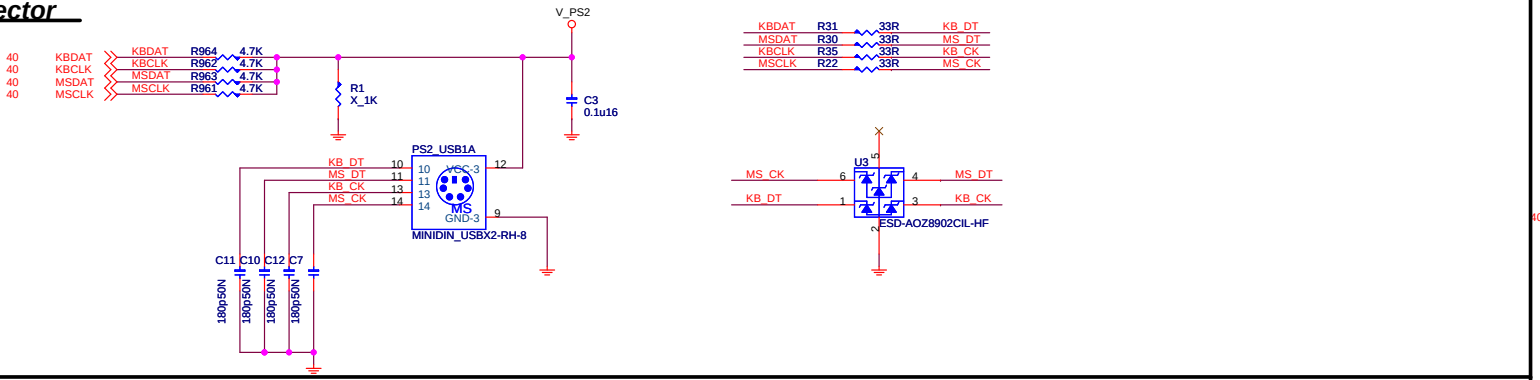
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A59	
Size: Custom	Document Description: Front USB20	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 30 of 70	


U34
MB_USB_5D-
MB_USB_5D+
MB_USB_6D-
MB_USB_6D+
ESD-AOZ8902CIL-HF
L11
14 MB_USB_5D-
14 MB_USB_5D+
MB_USB_5D-
MB_USB_5D+
X_4P2R-0R/4
L12
14 MB_USB_6D-
14 MB_USB_6D+
MB_USB_6D-
MB_USB_6D+
X_4P2R-0R/4
U35
ESD-AOZ8829DI-03-HF
MB_USB30_TX1+_C
MB_USB30_TX1-_C
MB_USB30_TX2+_C
MB_USB30_TX2-_C
U33
ESD-AOZ8829DI-03-HF
MB_USB30_RX1+
MB_USB30_RX1-
MB_USB30_RX2+
MB_USB30_RX2-
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
5V_FUSB2
R685
10K1%
14
OC#2
PORT5.6
R688
15K1%
EC18+
470u16
EMI Cap near Connector.
C339
0.1u/16X4
C198
1u6.3X4
180
JUSB3
MB_USB_5D+
MB_USB_5D-
14 MB_USB30_TX1+
14 MB_USB30_TX1-
14 MB_USB30_RX1+
14 MB_USB30_RX1-
C220 0.1u/16X4
C280 0.1u/16X4
MB_USB30_TX1+_C
MB_USB30_TX1-_C
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS-2
GND-1
GND-2
MB_USB_6D+
MB_USB_6D-
14 MB_USB30_TX2+
14 MB_USB30_TX2-
14 MB_USB30_RX2+
14 MB_USB30_RX2-
C218 0.1u/16X4
C278 0.1u/16X4
MB_USB30_TX2+_C
MB_USB30_TX2-_C
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND-3
VBUS-1
GND-4
NC
2X10 Connector
BH2X10[20]-2PITCH_BLACK-RH-1
EMI Cap near Connector.
C191
1u6.3X4
C335
0.1u/16X4
EC14+
470u6.3
R683
10K1%
OC#1
PORT3.4
R684
15K1%
U31
ESD-AOZ8829DI-03-HF
MB_USB30_TX3-_C
MB_USB30_TX3+_C
MB_USB30_TX4+_C
MB_USB30_TX4-_C
U27
ESD-AOZ8829DI-03-HF
MB_USB30_RX3-
MB_USB30_RX3+
MB_USB30_RX4-
MB_USB30_RX4+
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
90
JUSB4
MB_USB_3D+
MB_USB_3D-
14 MB_USB30_TX3+
14 MB_USB30_TX3-
14 MB_USB30_RX3+
14 MB_USB30_RX3-
C300 0.1u/16X4
C302 0.1u/16X4
MB_USB30_TX3+_C
MB_USB30_TX3-_C
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND
GND
MB_USB_4D+
MB_USB_4D-
14 MB_USB30_TX4+
14 MB_USB30_TX4-
14 MB_USB30_RX4+
14 MB_USB30_RX4-
C305 0.1u/16X4
C306 0.1u/16X4
MB_USB30_TX4+_C
MB_USB30_TX4-_C
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND
VBUS1
GND
NC
2X10_CONNECTOR
BH2X10[20]#-2PITCH_BLACK-RH-2
U26
MB_USB_3D-
MB_USB_3D+
MB_USB_4D-
MB_USB_4D+
ESD-AOZ8902CIL-HF
L9
14 MB_USB_4D-
14 MB_USB_4D+
MB_USB_4D-
MB_USB_4D+
X_4P2R-0R/4
L10
14 MB_USB_3D-
14 MB_USB_3D+
MB_USB_3D-
MB_USB_3D+
X_4P2R-0R/4
MICRO-STAR INT'L CO.,LTD
MS-7A59
Size
Custom
Document Description
Front USB30
Rev
2.0
Date: Monday, September 12, 2016
Sheet 31 of 70

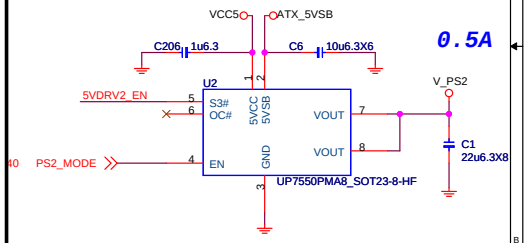
LAN USB2.0 &3.0

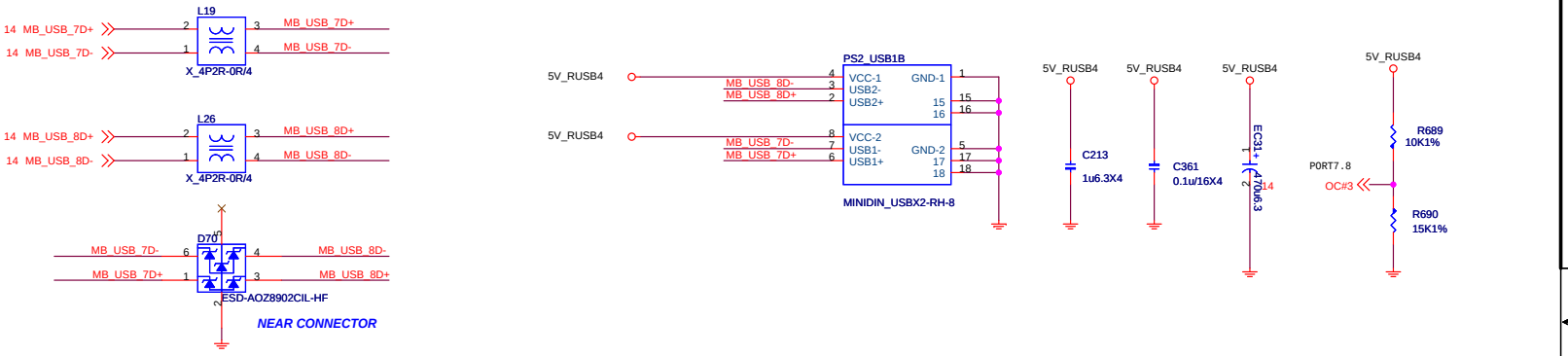


PS2 Connector

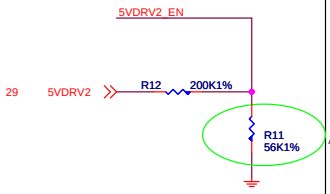


PS2 Power





USB MODE



MICRO-STAR INT'L CO.,LTD	
MS-7A59	
Size: Custom	Document Description: Real USB&PS2
Rev: 2.0	
Date: Monday, September 12, 2016	Sheet 32 of 70

HDMI USB3.0

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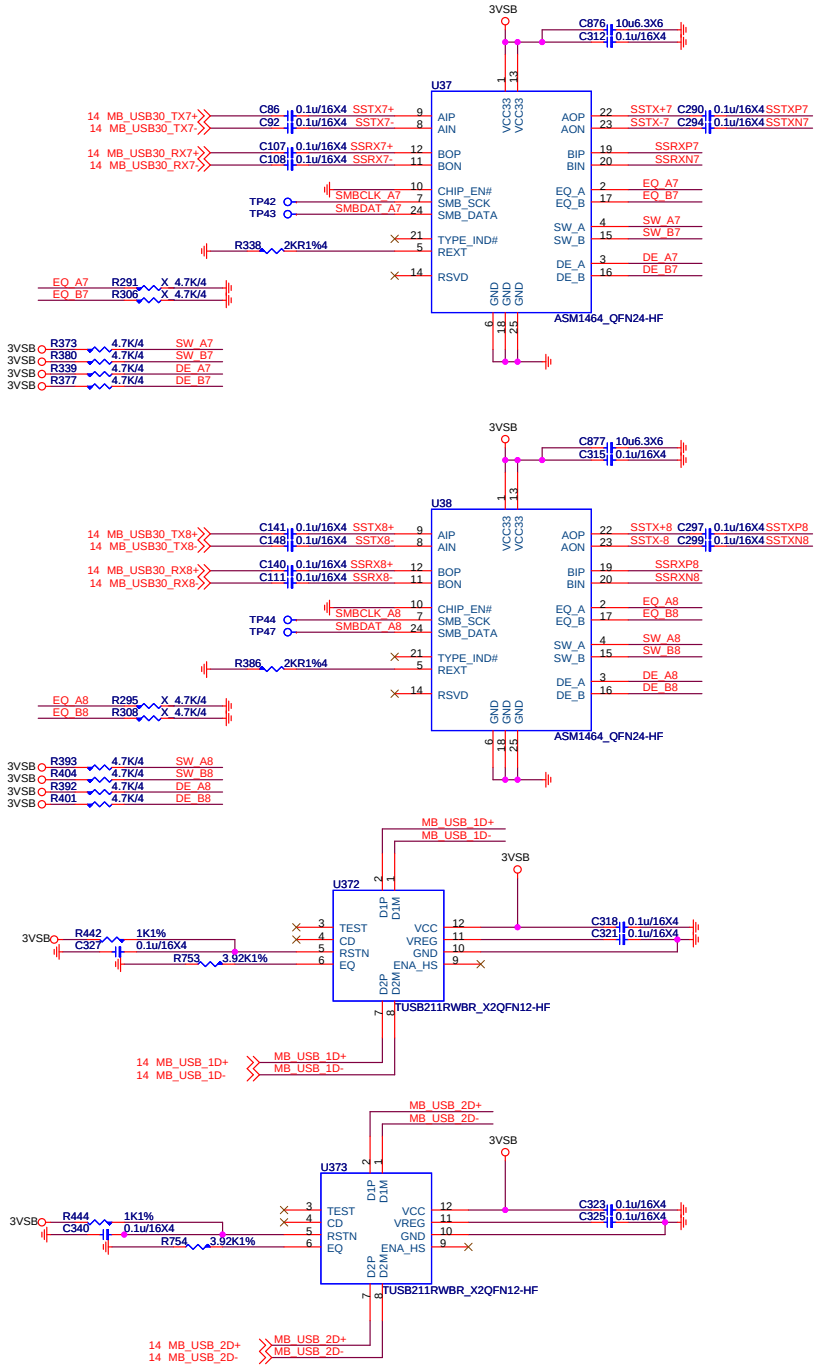
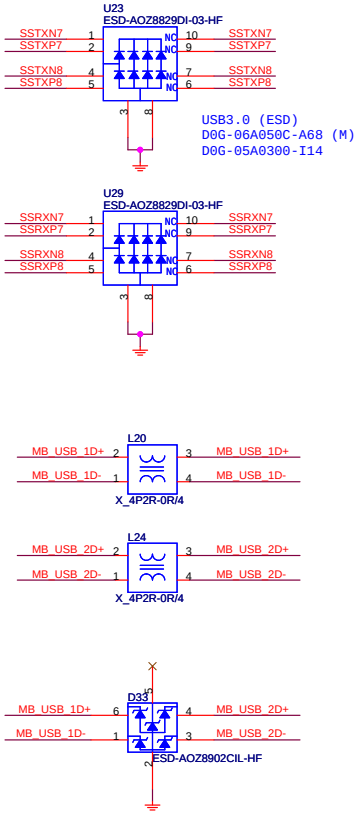
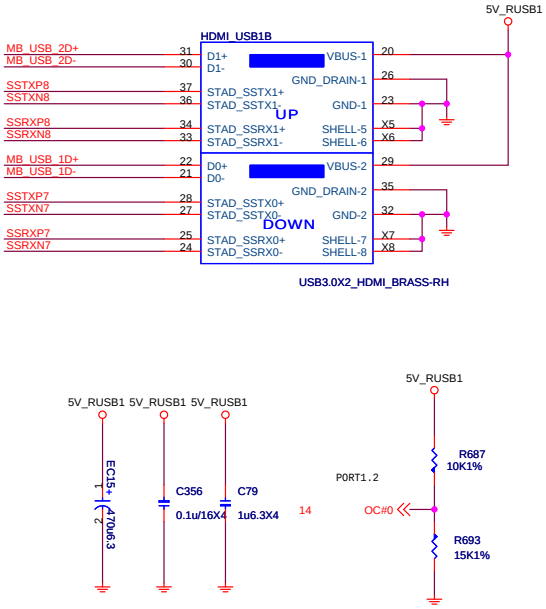


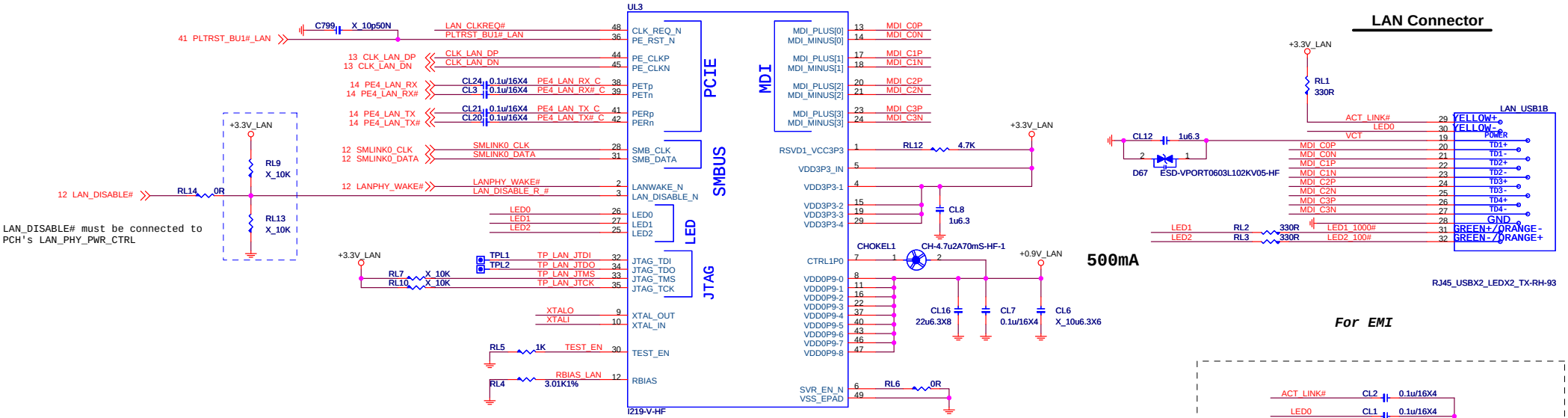




MICRO-STAR INT'L CO.,LTD			
MS-7A59			
Size: Custom	Document Description: Real USB&PS2		Rev: 2.0
Date: Monday, September 12, 2016		Sheet 33 of 70	

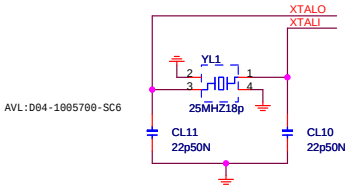
Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



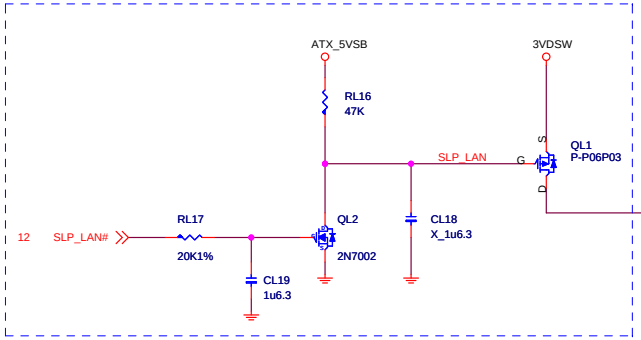
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N
is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well
of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



Note:These caps closed to PHY

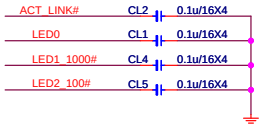
+3.3V_LAN
I218:132mA
I219:542mW

LAN Connector

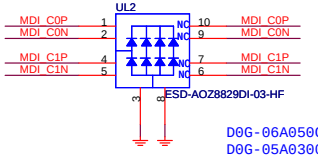
RJ45_USBX2_LEDX2_TX-RH-93

500mA

For EMI



UL2&UL3 close to connector



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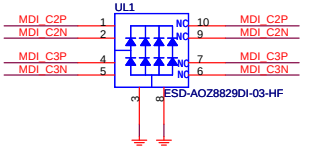
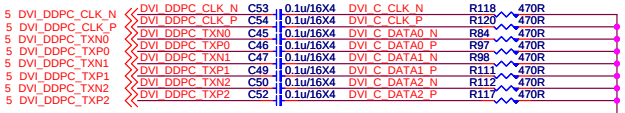
D0G-05A0300-I14

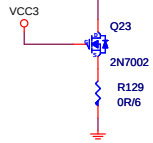


Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue).
Otherpairing combination is ok.

MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: Intel Lan- i219	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 34 of 70	

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)





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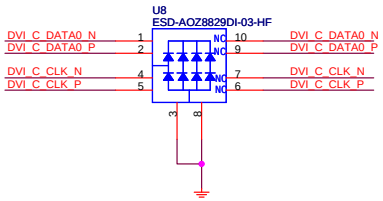

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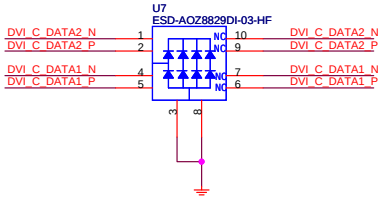
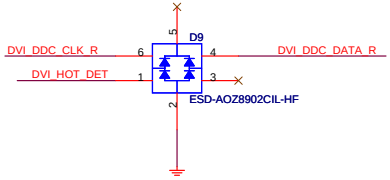
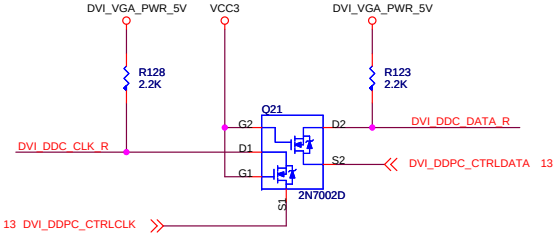
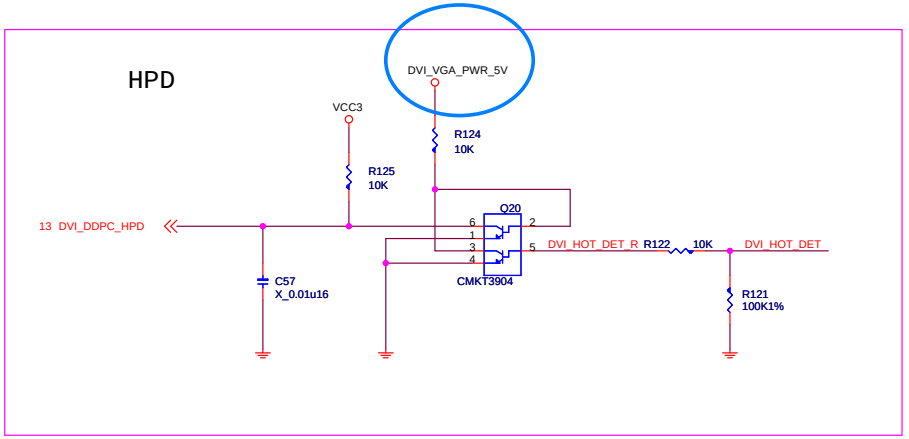
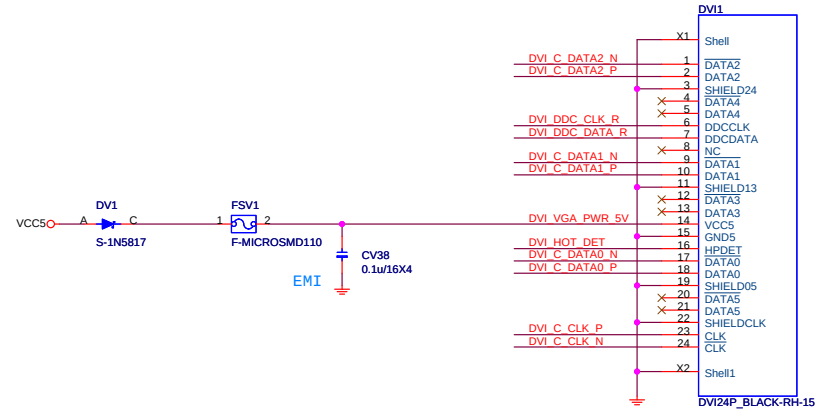
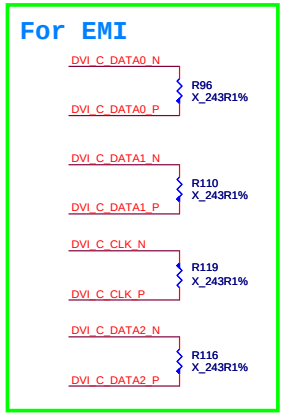


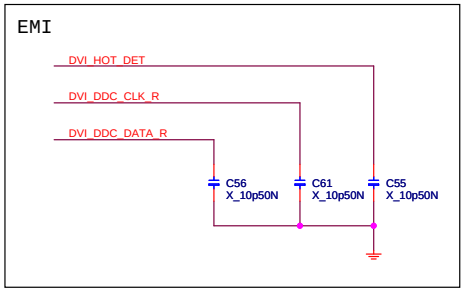






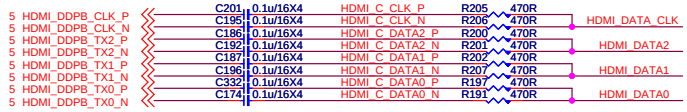


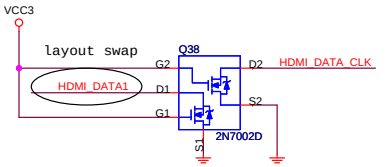


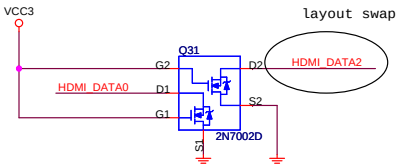


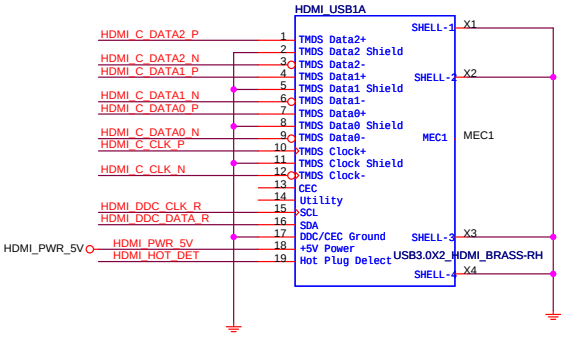
MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: DVI Connector	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 35 of 70	

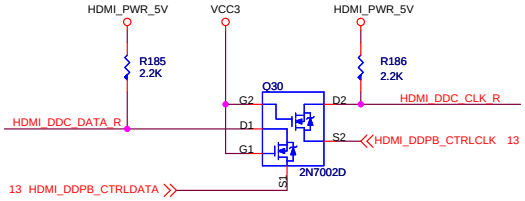
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

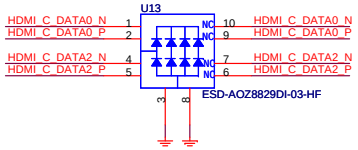


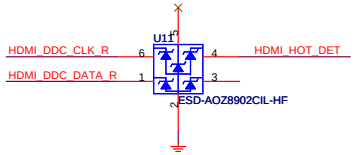


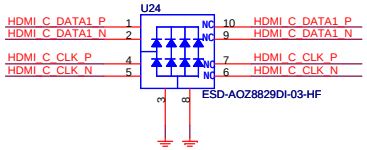


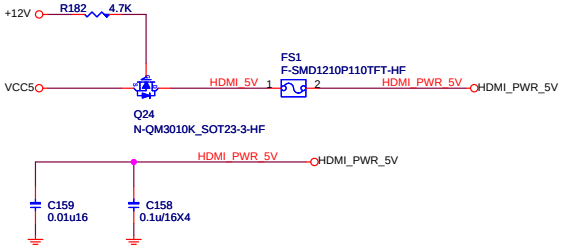


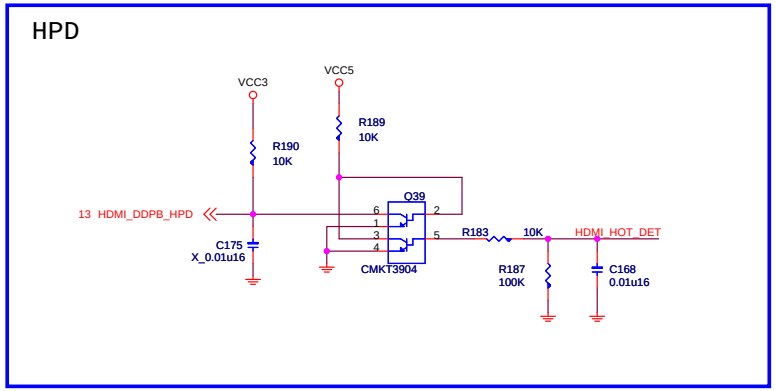


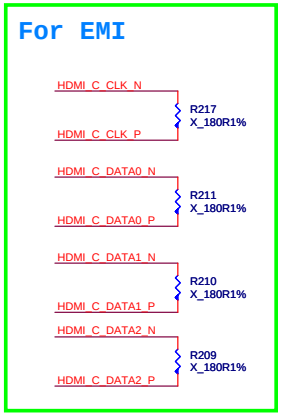












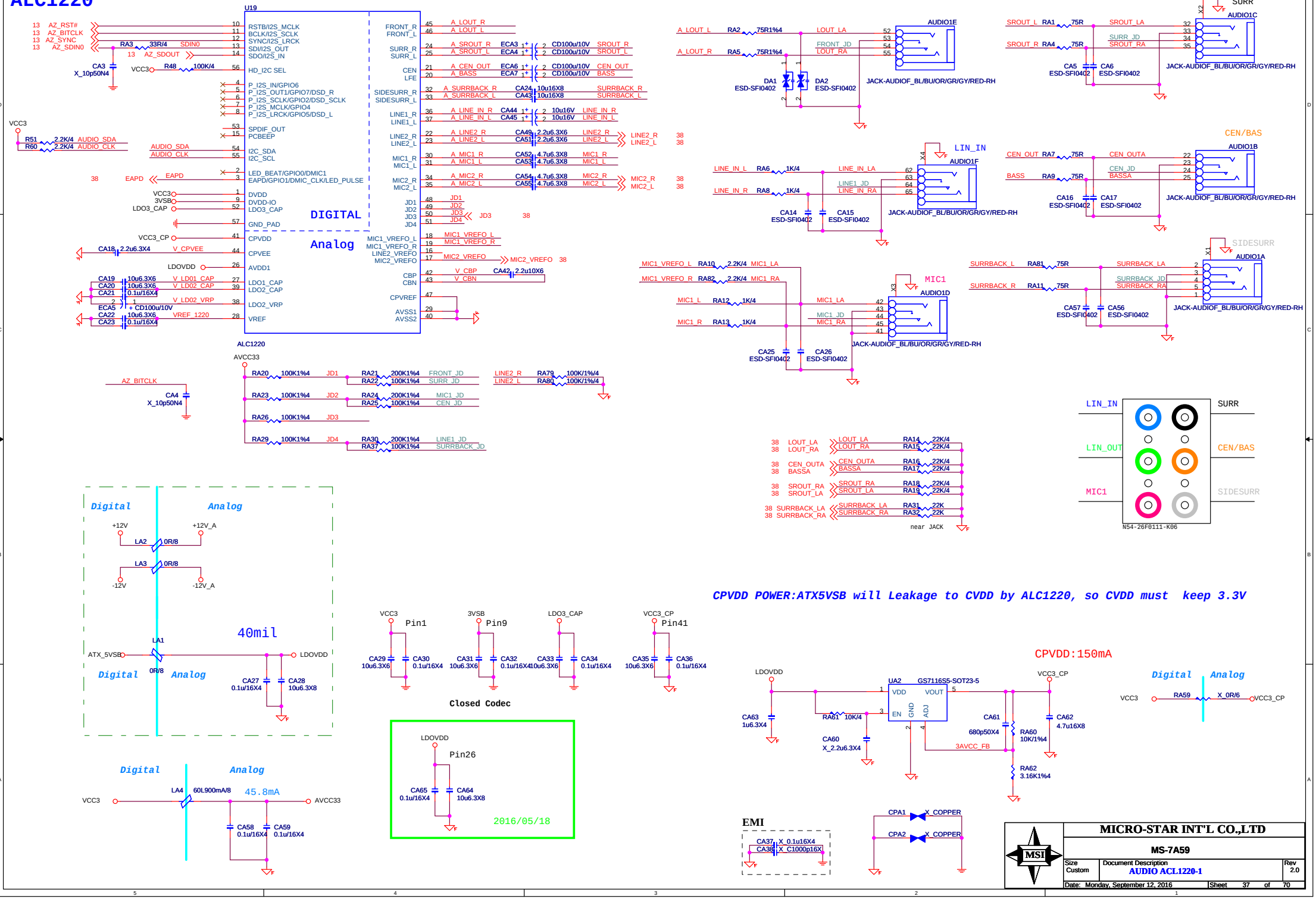
MICRO-STAR INT'L CO.,LTD

MS-7A59

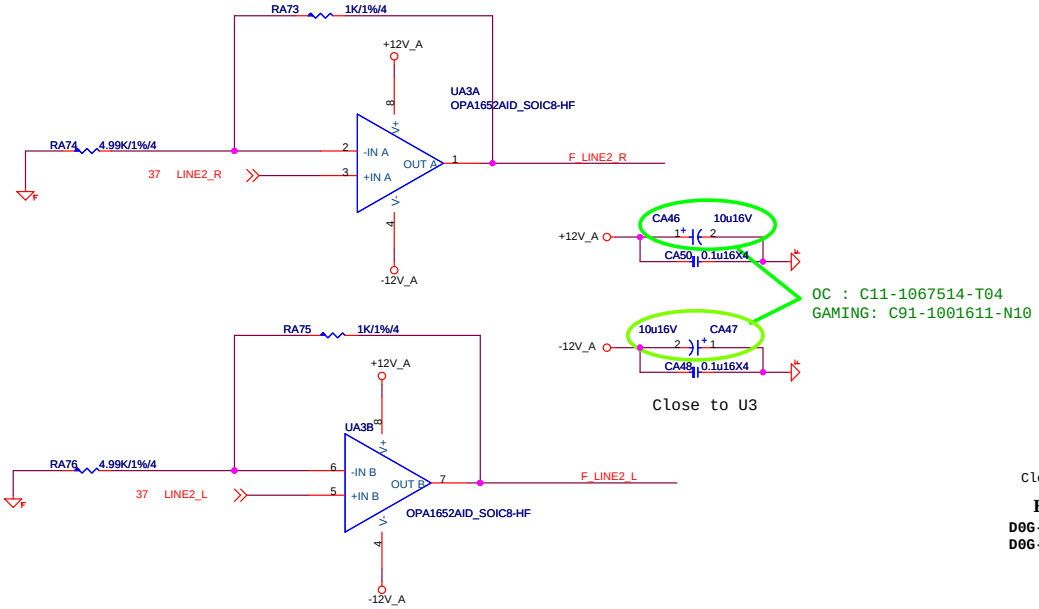
Size	Document Description	Rev
Custom	HDMI Connector	2.0

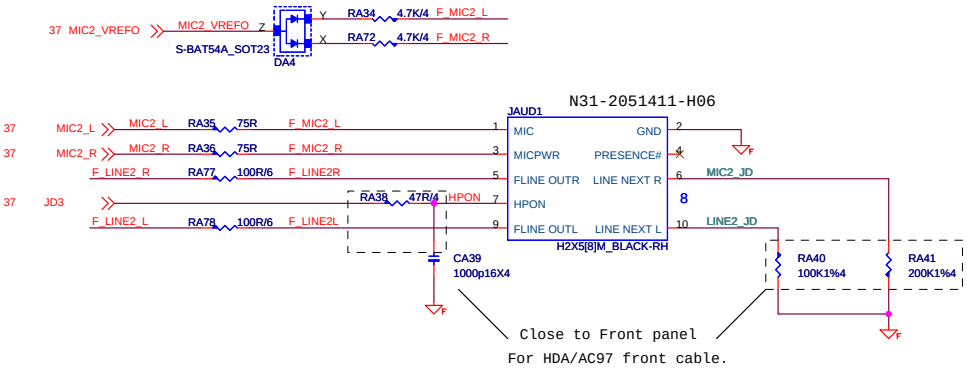
Date: Monday, September 12, 2016 Sheet 36 of 70

ALC1220



CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V



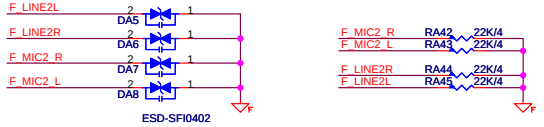


Close to Jack

ESD protect

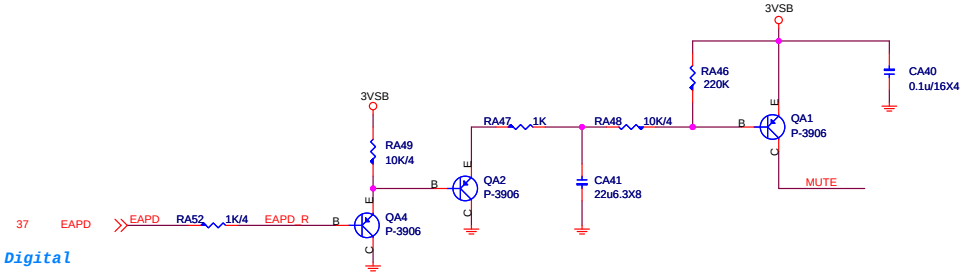
D0G-2950500-SI0

D0G-3010510-I05



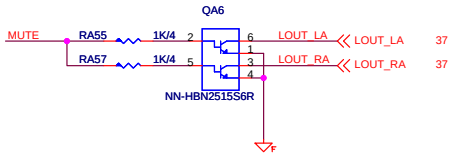
Rear Line OUT De-POP circuit

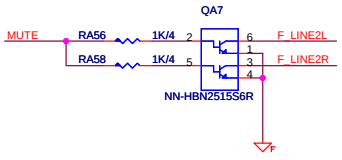
(De-pop circuit for Rear Line out & Front Headphone out)



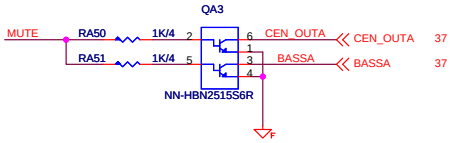
Digital

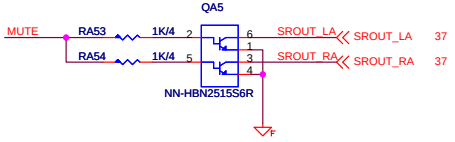
Analog

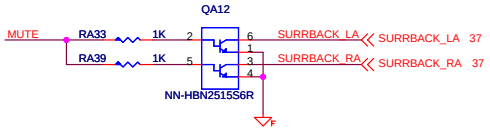




(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)







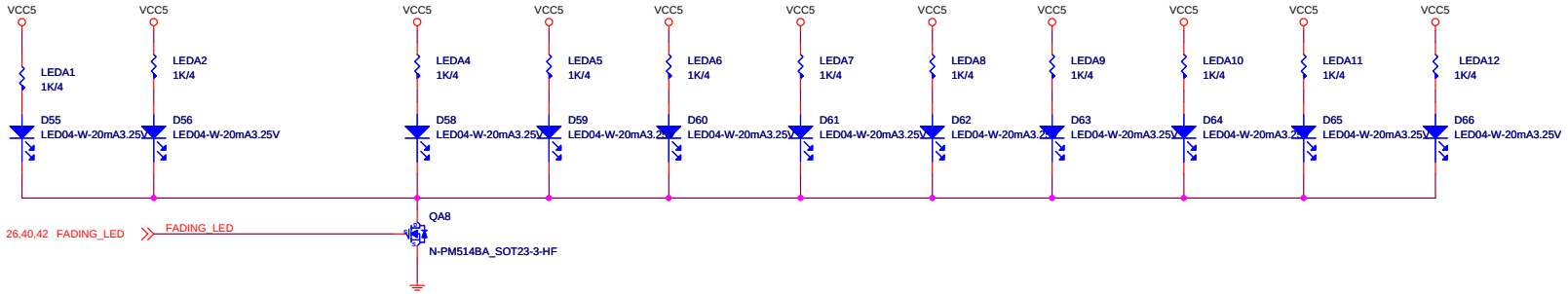
MICRO-STAR INT'L CO.,LTD

MS-7A59

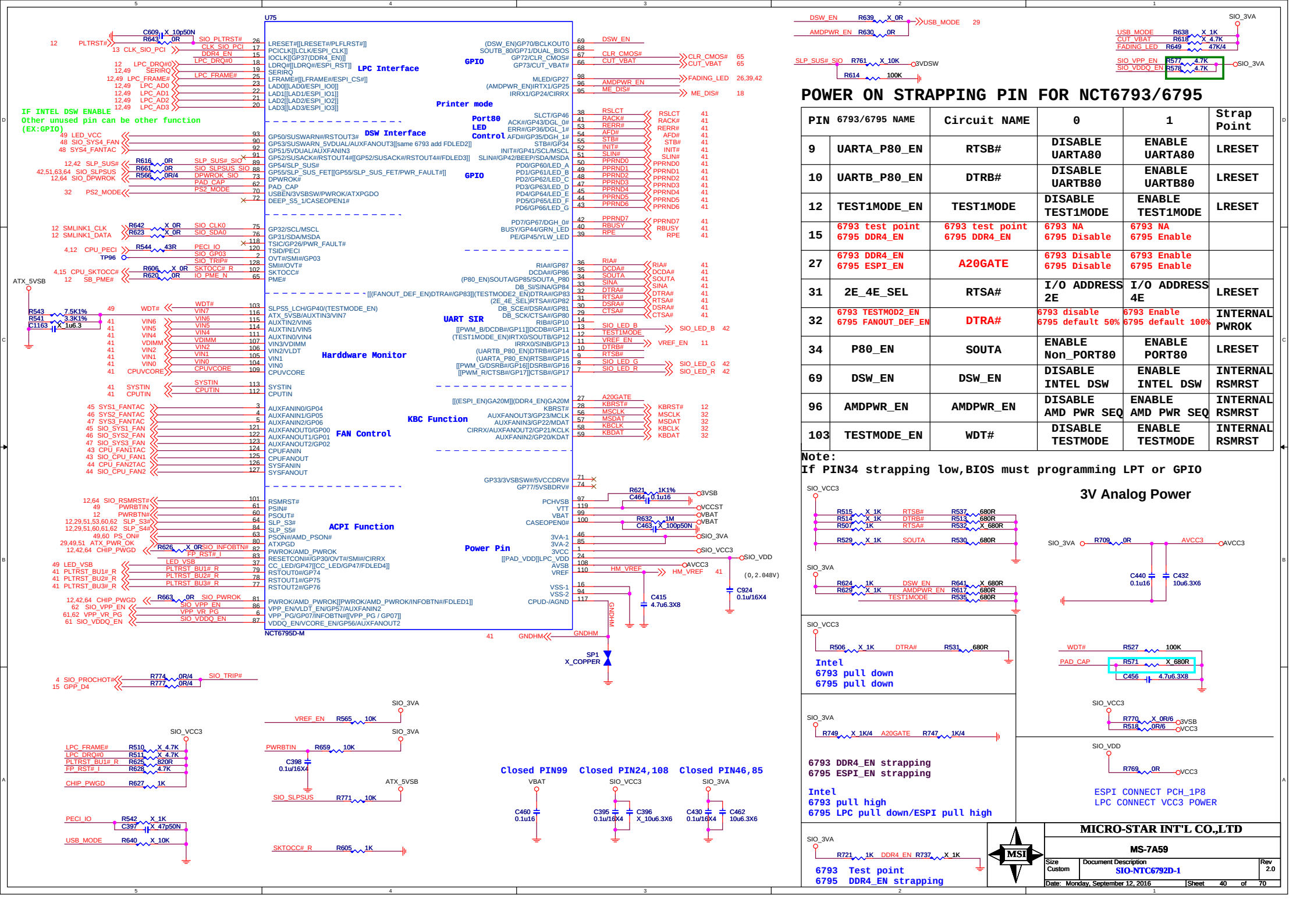
Size: Custom | Document Description: AUDIO ACL1220-2 | Rev: 2.0

Date: Monday, September 12, 2016 | Sheet 38 of 70

Audio moat is transparent and width 40mil



MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: AUDIO ACL1220-3	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 39 of 70	

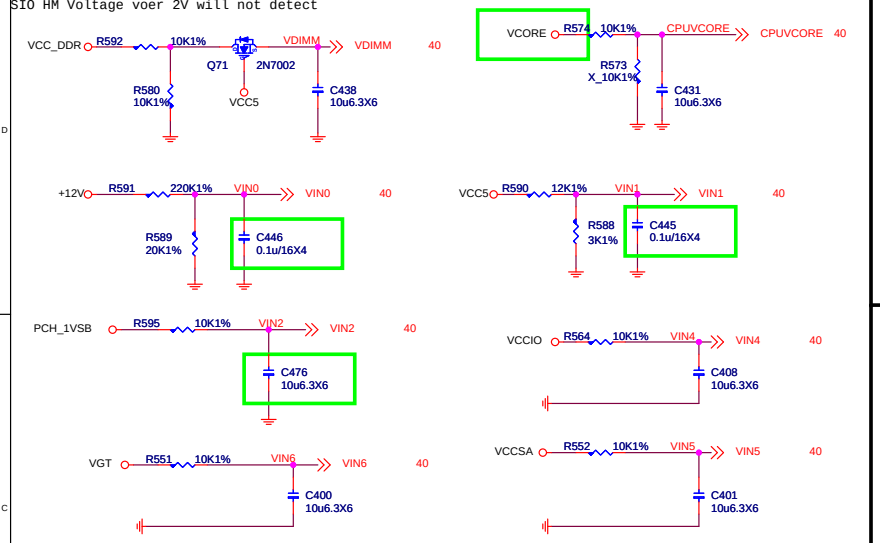


PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7A59
Size	Custom
Document Description	SIO-NTC6792D-1
Rev	2.0
Date	Monday, September 12, 2016
Sheet	40 of 70

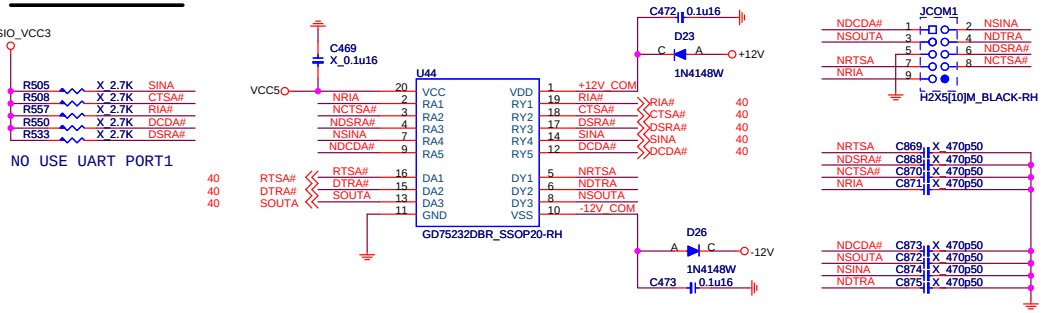
HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect

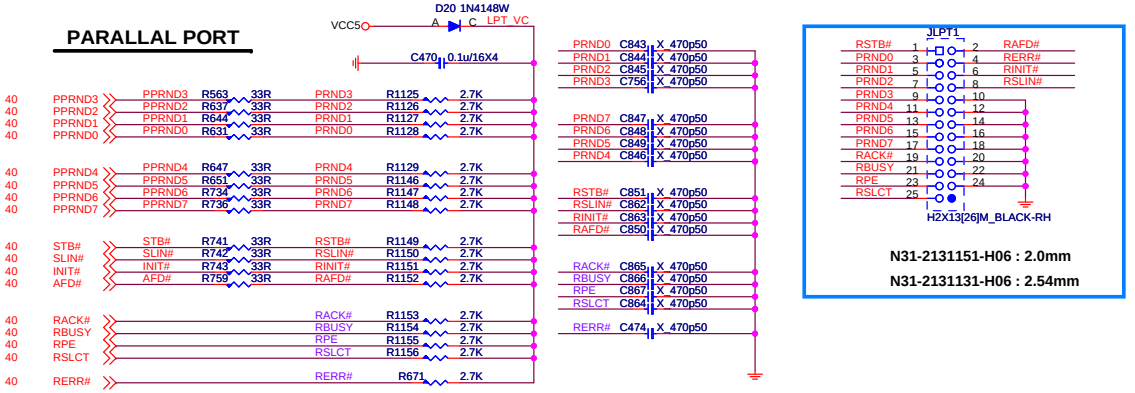


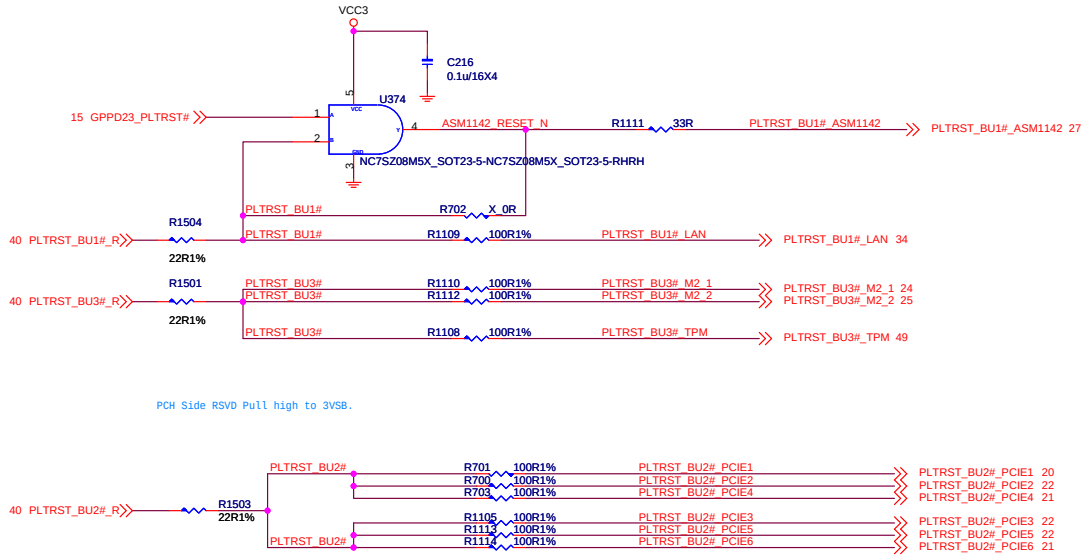
Thermal Monitor

SERIAL PORT 1

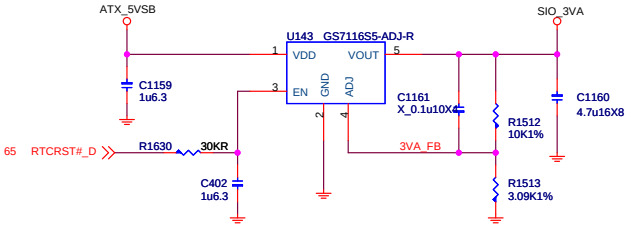


PARALLAL PORT





Vinafix.com



MICRO-STAR INT'L CO.,LTD

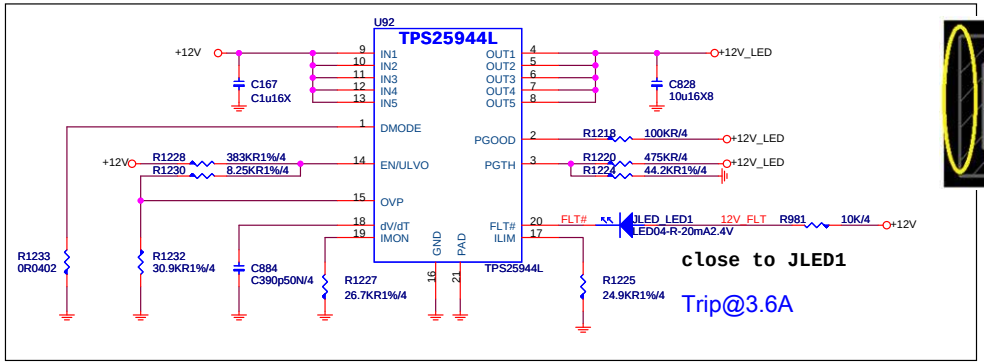
MS-7A59

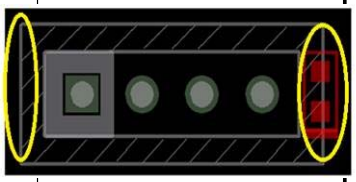
Size: Custom | Document Description: SIO-NTC6792D-2 | Rev: 2.0

Date: Monday, September 12, 2016 | Sheet 41 of 70

LED Control by SIO

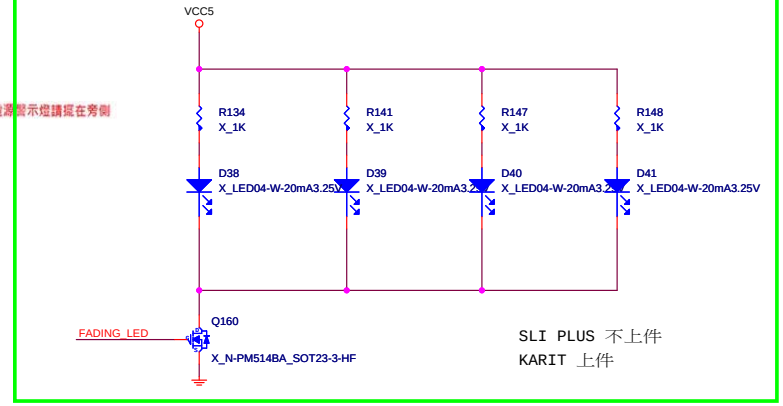
2016.07.06 Use TPS25944L

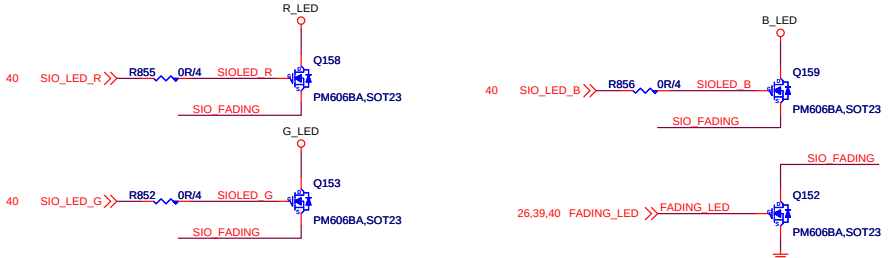




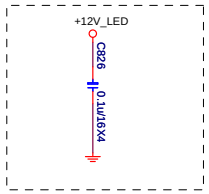
JLED1电源显示燈請擺在旁側

PCH LED

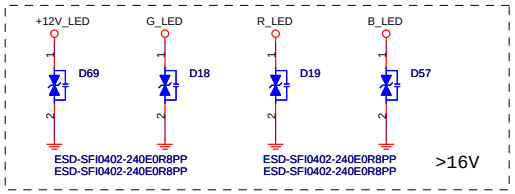


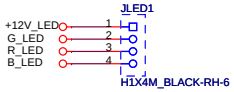


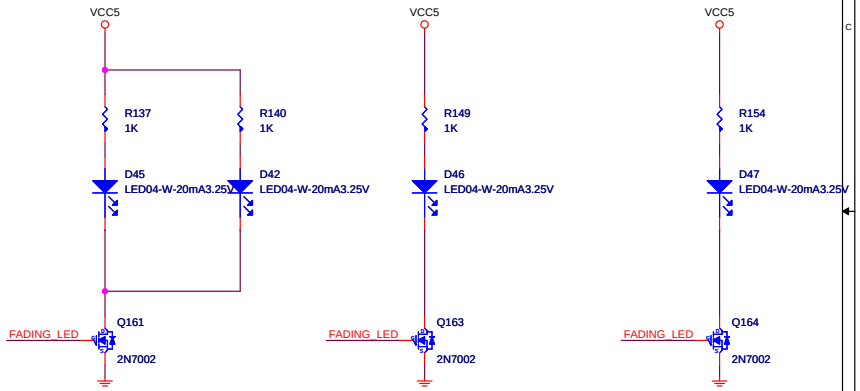
2016.08.02 Add +12V_LED 0.1uF



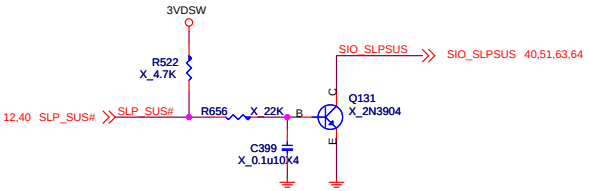
2016.08.02 stuff ESD

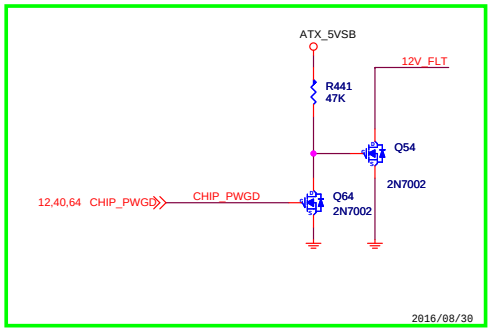


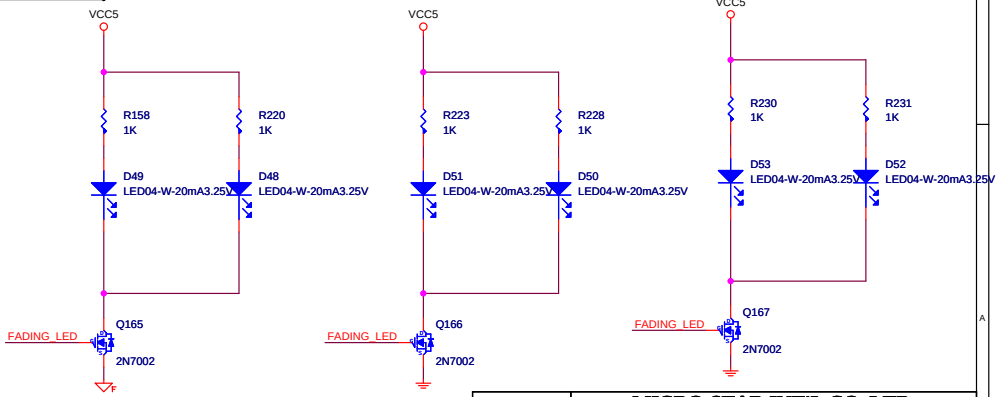




SLP_SUS Co-lay circuit





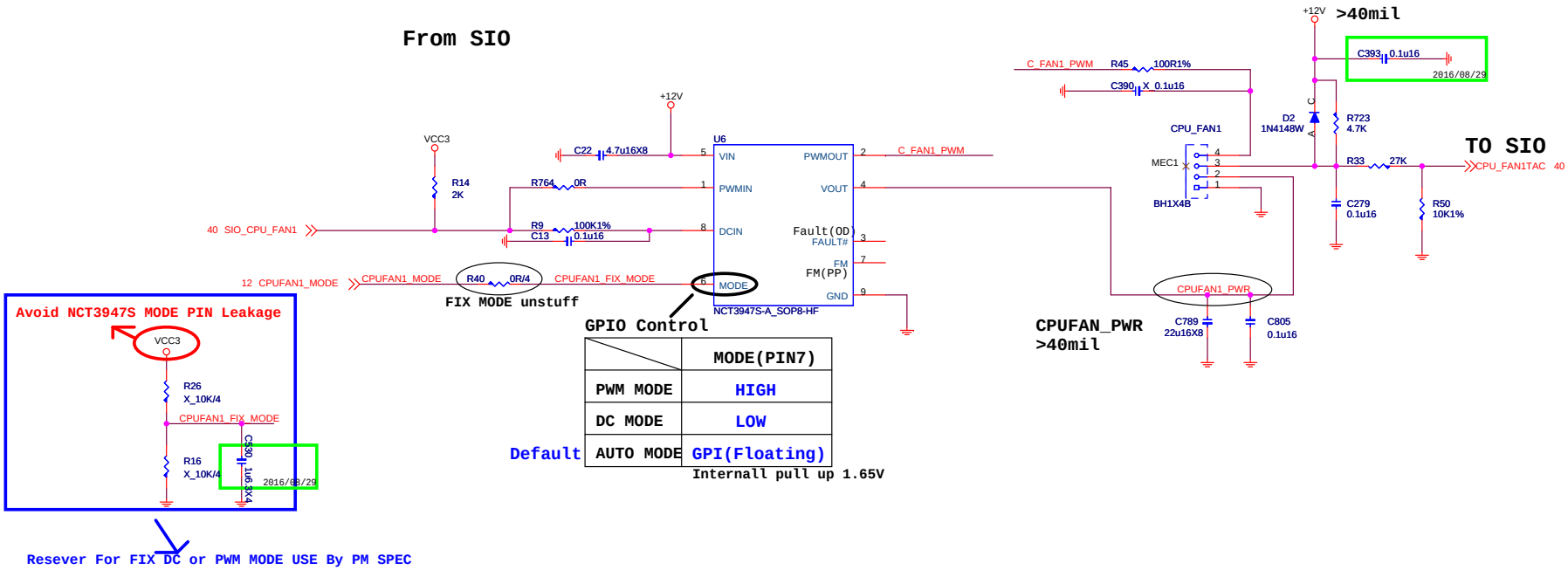


MICRO-STAR INT'L CO.,LTD

MS-7A59

Size	Document Description	Rev
Custom	SIO-NTC6792D-2	2.0

Date: Monday, September 12, 2016 Sheet 42 of 70



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

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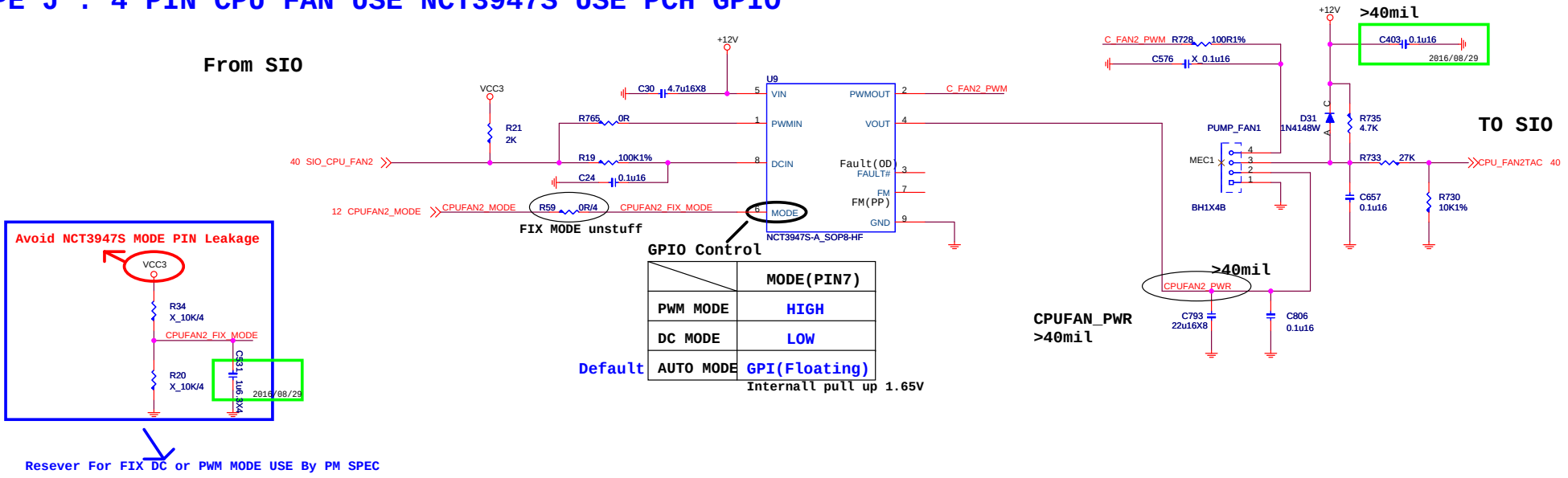
Size	Document Description	Rev
Custom	CPU FAN1	2.0

Date: Monday, September 12, 2016 Sheet 43 of 70

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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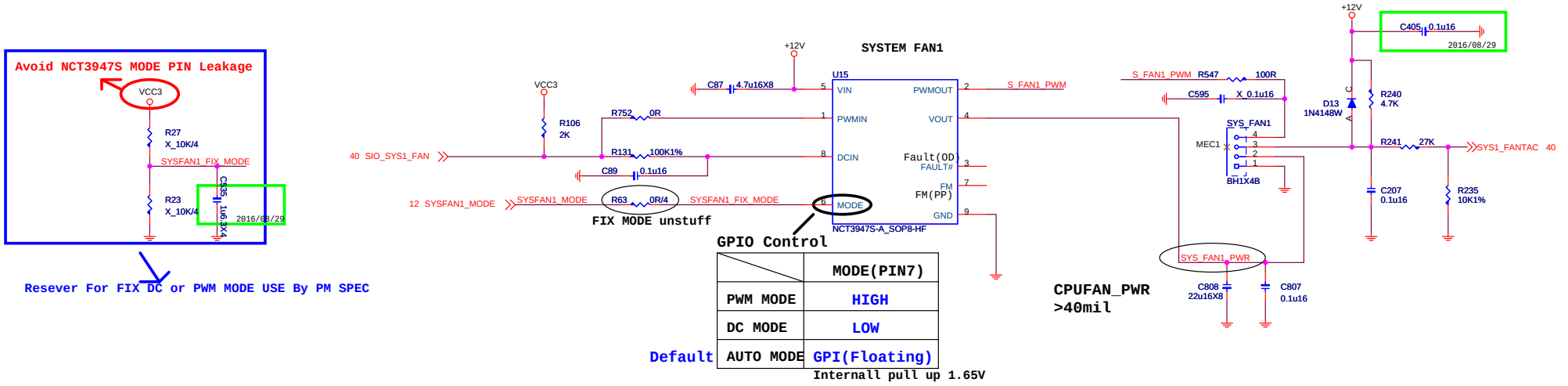
Size: Custom	Document Description: CPU FAN2	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 44 of 70	



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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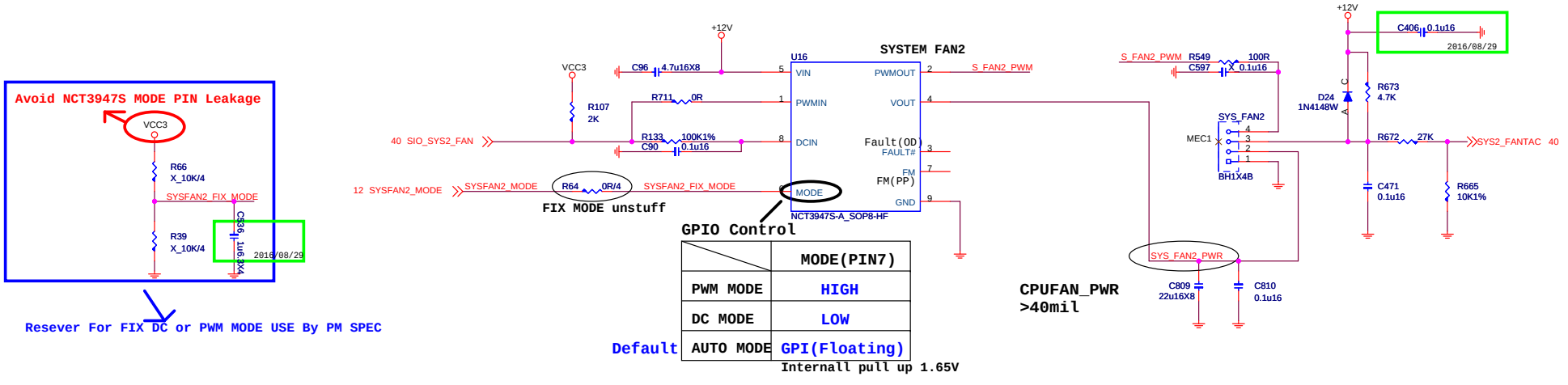
Size	Document Description	Rev
Custom	SYSTEM FAN1	2.0

Date: Monday, September 12, 2016 Sheet 45 of 70



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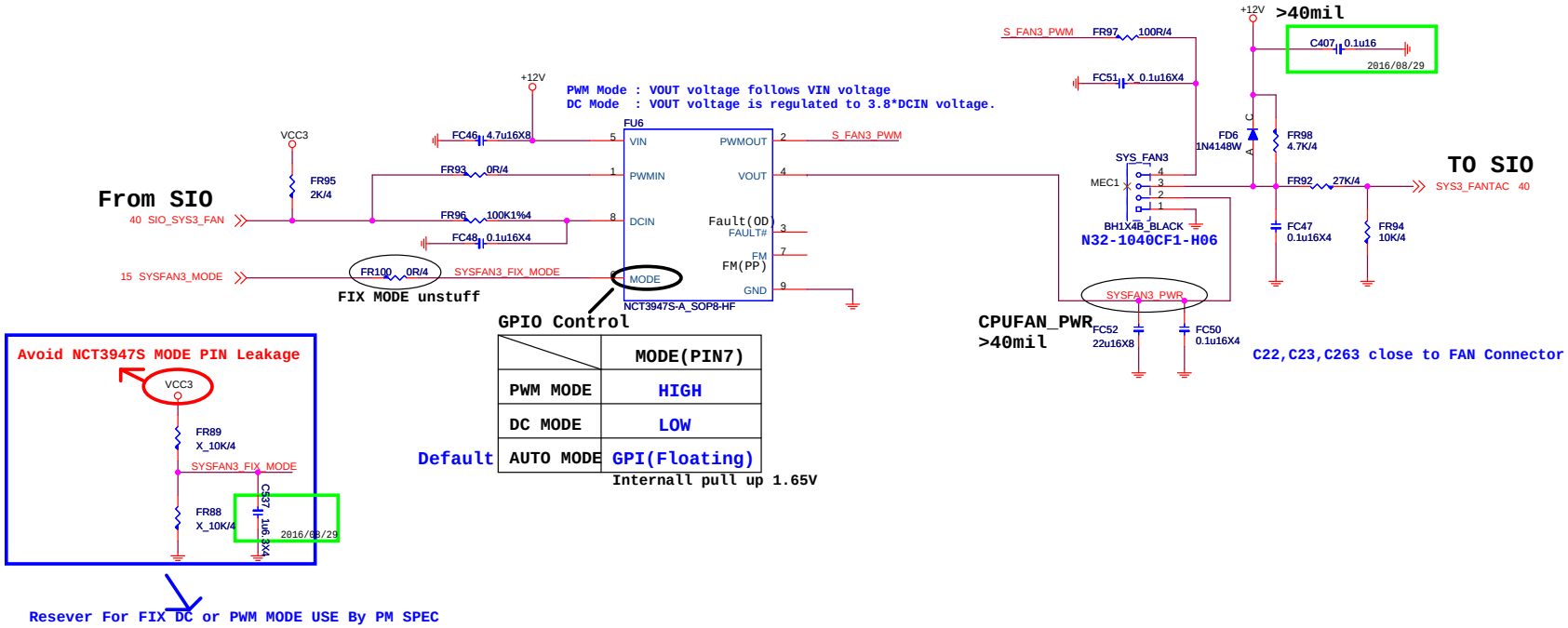
MS-7A59		
Size: Custom	Document Description: SYSTEM FAN2 teknisi indonesia	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 46 of 70	

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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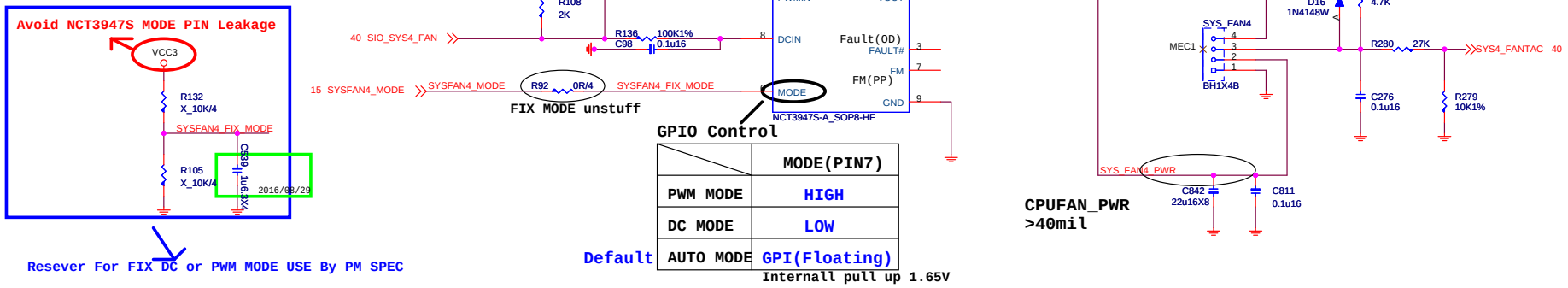
MS-7A59		
Size: Custom	Document Description: SYSTEM FAN3	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 47 of 70	

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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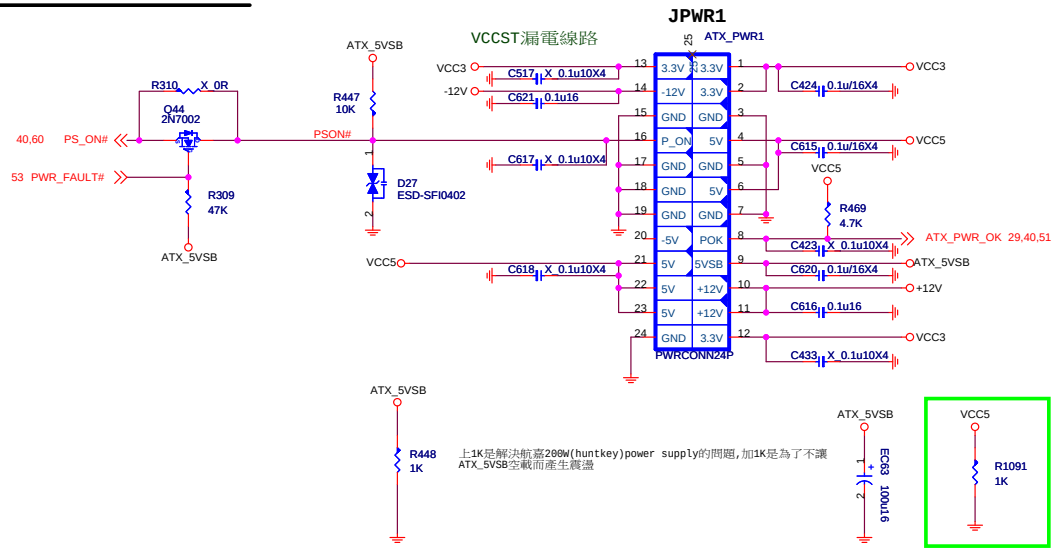
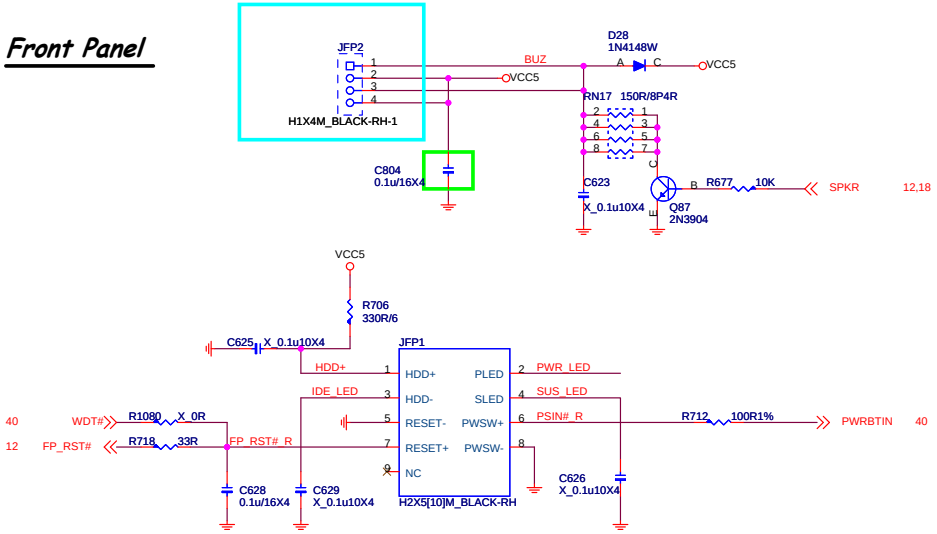
Size: Custom | Document Description: SYSTEM FAN4 | Rev: 2.0

Date: Monday, September 12, 2016 | Sheet 48 of 70

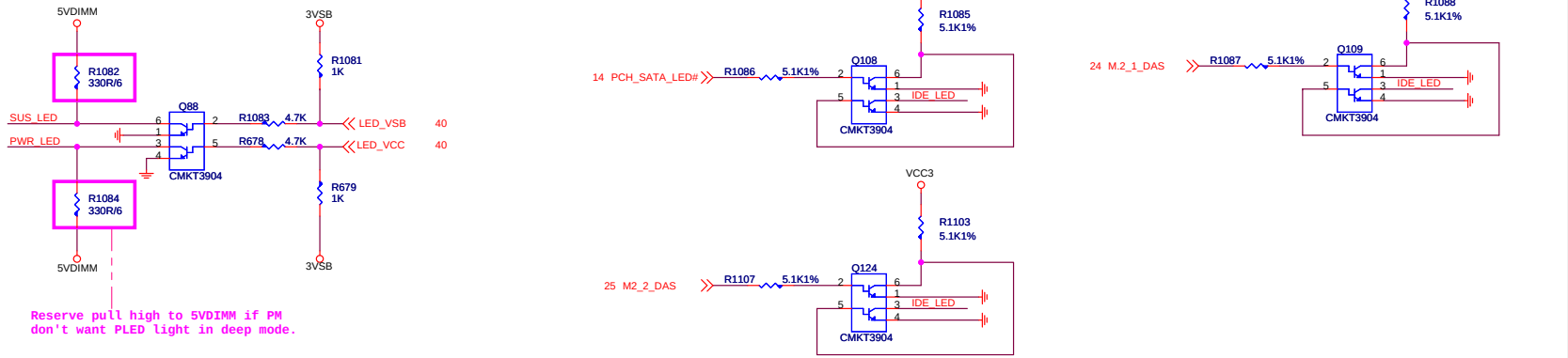
ATX POWER CONNECTOR



Front Panel

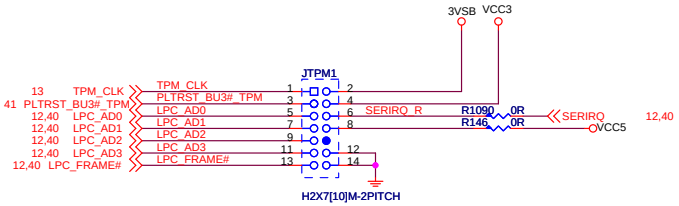


LED

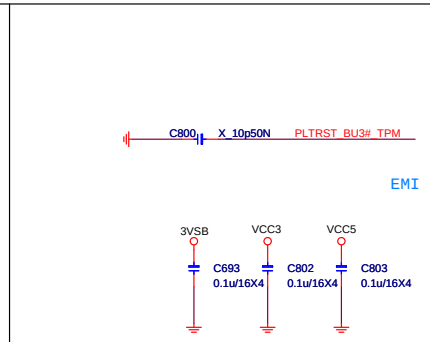


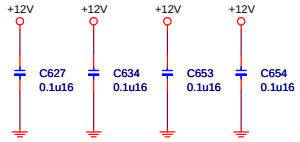
TPM

Confirm ESPI TPM card and TPM card pin difine (Not ready)



Vinafix.com





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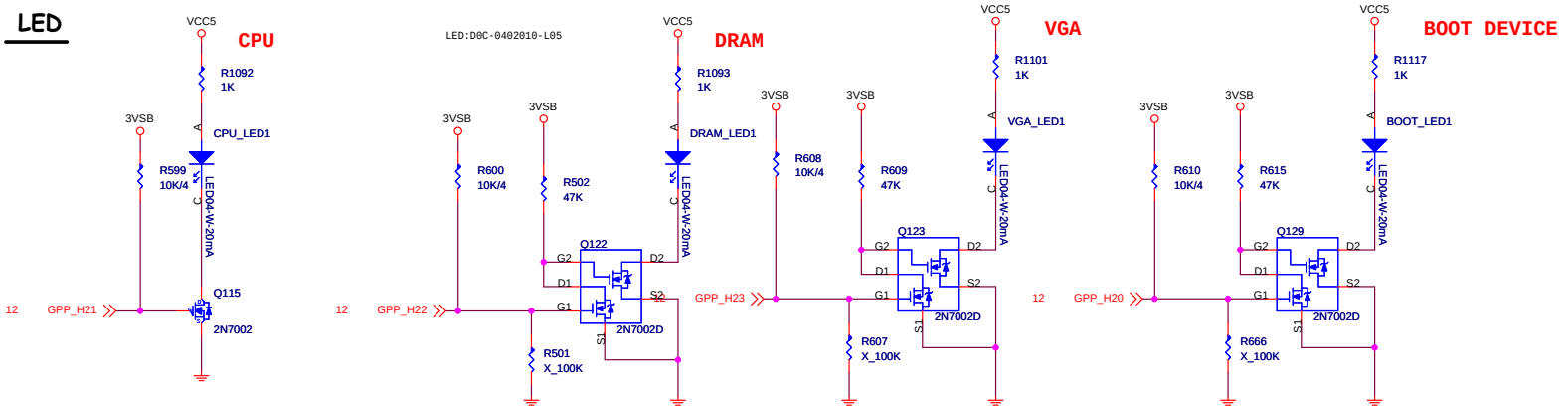
MS-7A59	
Size: Custom	Document Description: ATX Power/F_Panel
Rev: 2.0	
Date: Monday, September 12, 2016	Sheet 49 of 70

LED



KRAIT GAMING LED >>WHITE:D0C-040S200-E07

關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。
   （系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

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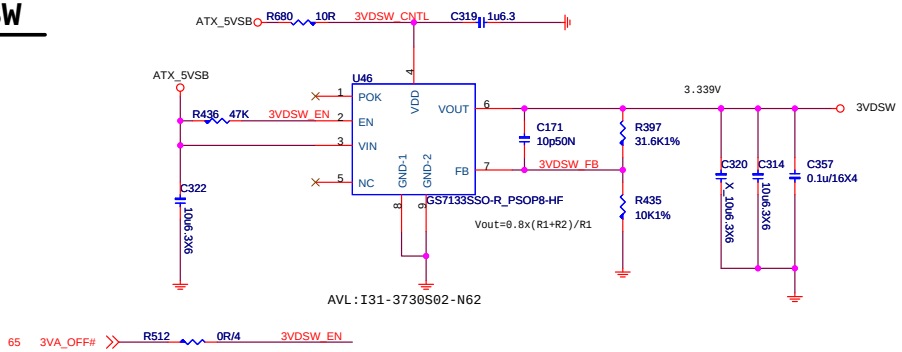
MS-7A59

Size: Custom | Document Description: ATX Power/F_Panel | Rev: 2.0

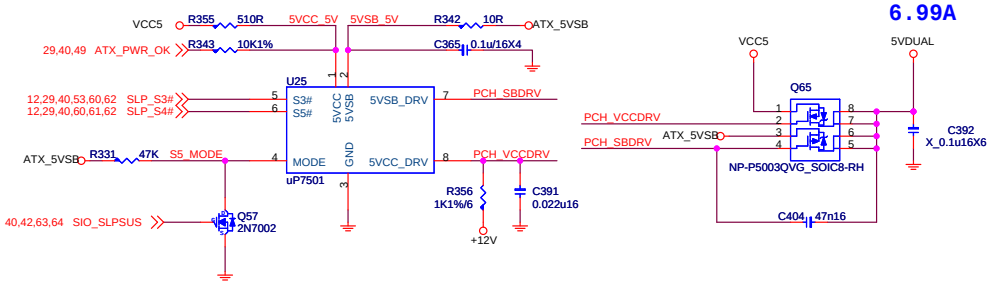
Date: Monday, September 12, 2016 | Sheet 50 of 70

3VDSW

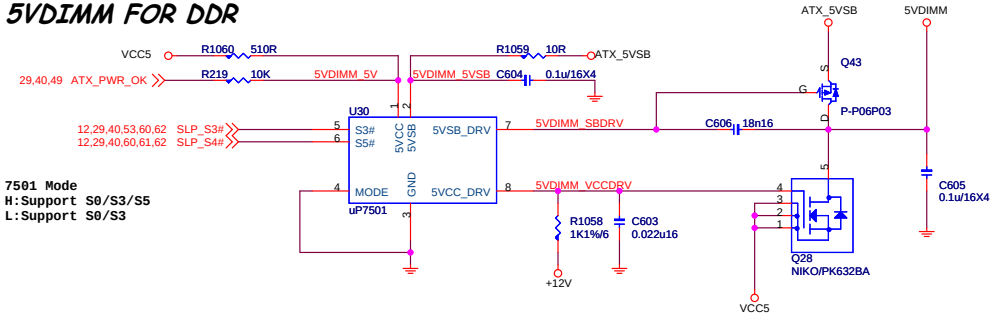


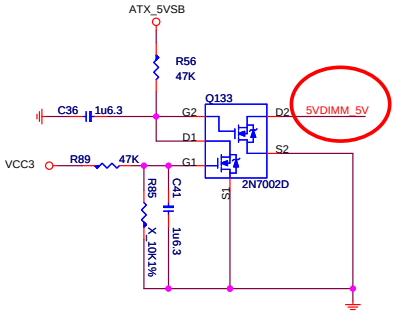
5VDUAL

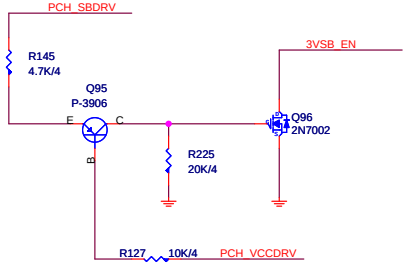
5VDUAL is power source of 1P0SB



5VDIMM FOR DDR

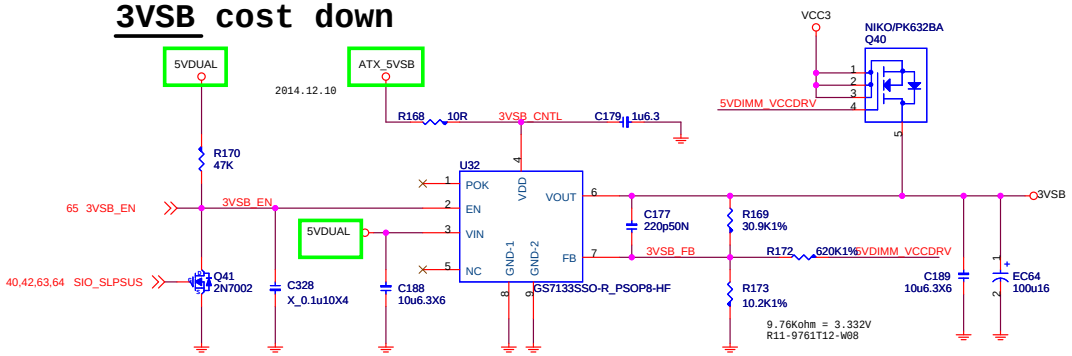






防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

3VSB cost down



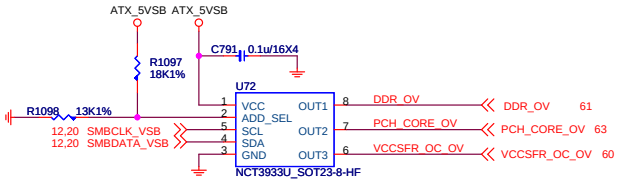
AVL:I31-3730S02-N62 2014.10.15 update

VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

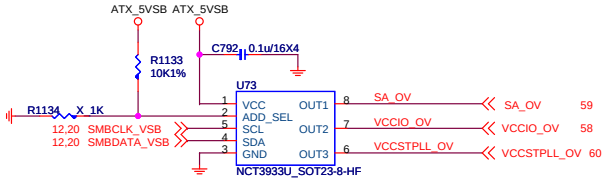
MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: ACPI UPI	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 51 of 70	

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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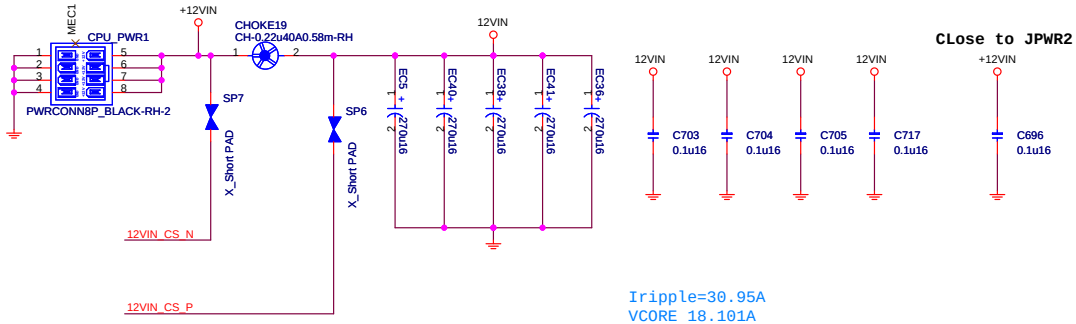
MS-7A59

Size: Custom | Document Description: OV-NCT3933/GPIO-NCT5605 | Rev: 2.0

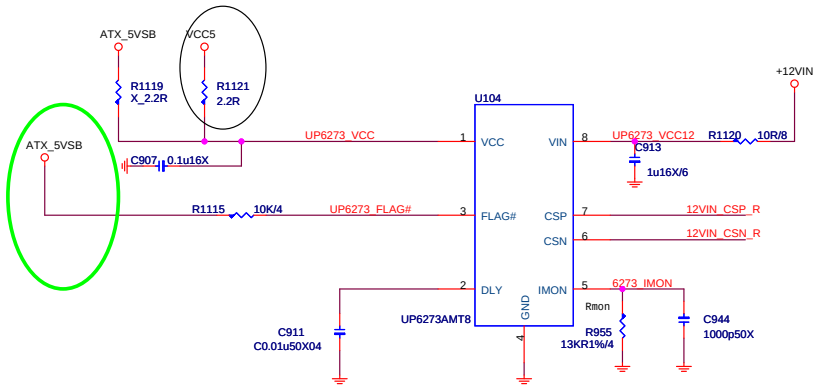
Date: Monday, September 12, 2016 | Sheet 52 of 70



CLose to JPWR2

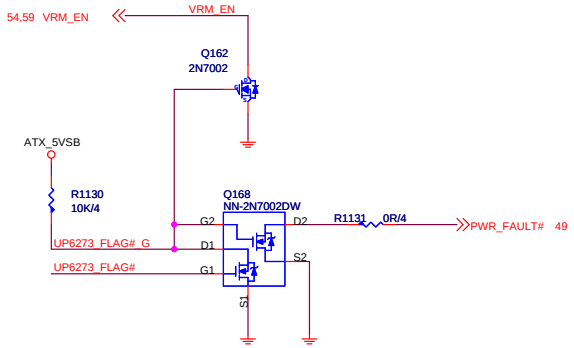
Iripple=30.95A
VCORE 18.101A
VGT 8.457A
VCCSA 4.392A

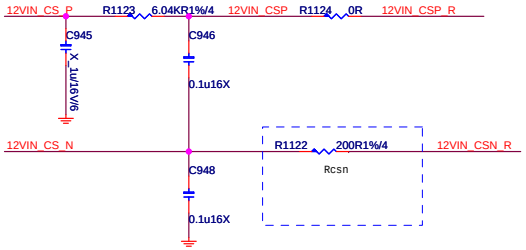
POWER METER
OCP: 120A



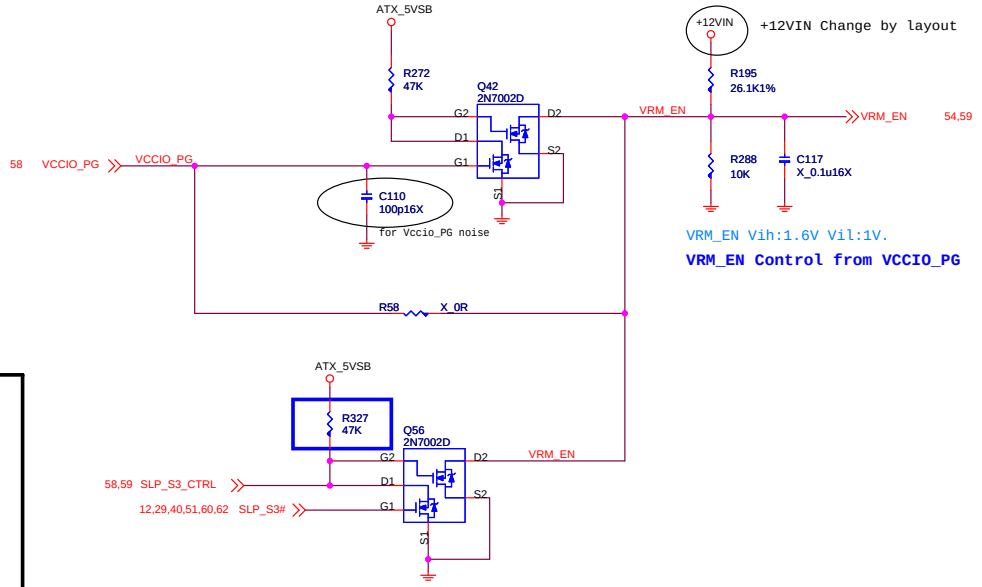
Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon

(1.2 * 0.2) / (10K* 0.3m) = 80A



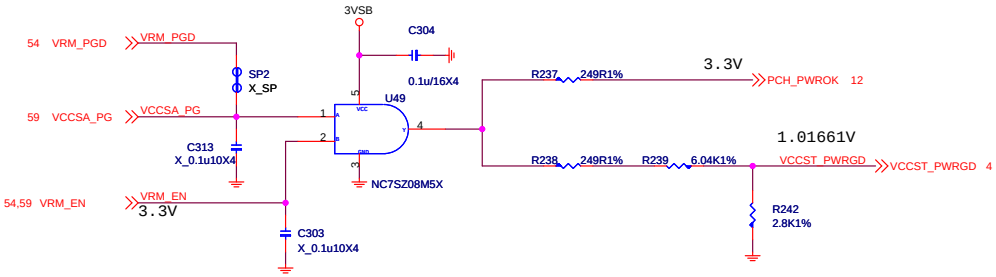


VRM_EN Control from VCCIO_PG



PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PGD

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



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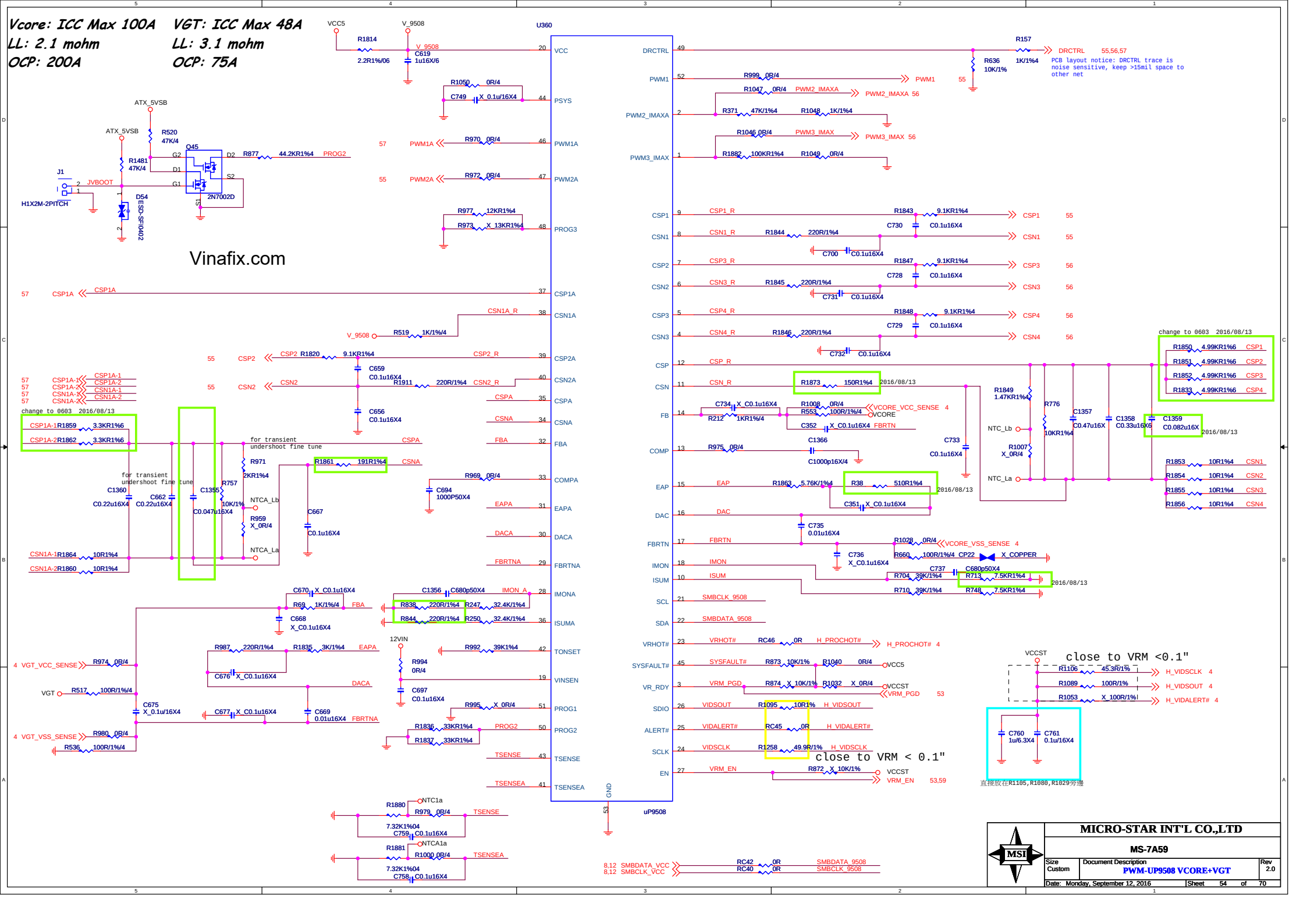
MS-7A59		
Size: Custom	Document Description: Rear I/O PS2	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 53 of 70	

Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 200A

VGT: ICC Max 48A
LL: 3.1 mohm
OCP: 75A



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MS-7A59

Size	Document Description	Rev
Custom	PWM-UP9508 VCORE+VGT	2.0

Date: Monday, September 12, 2016 | Sheet 54 of 70

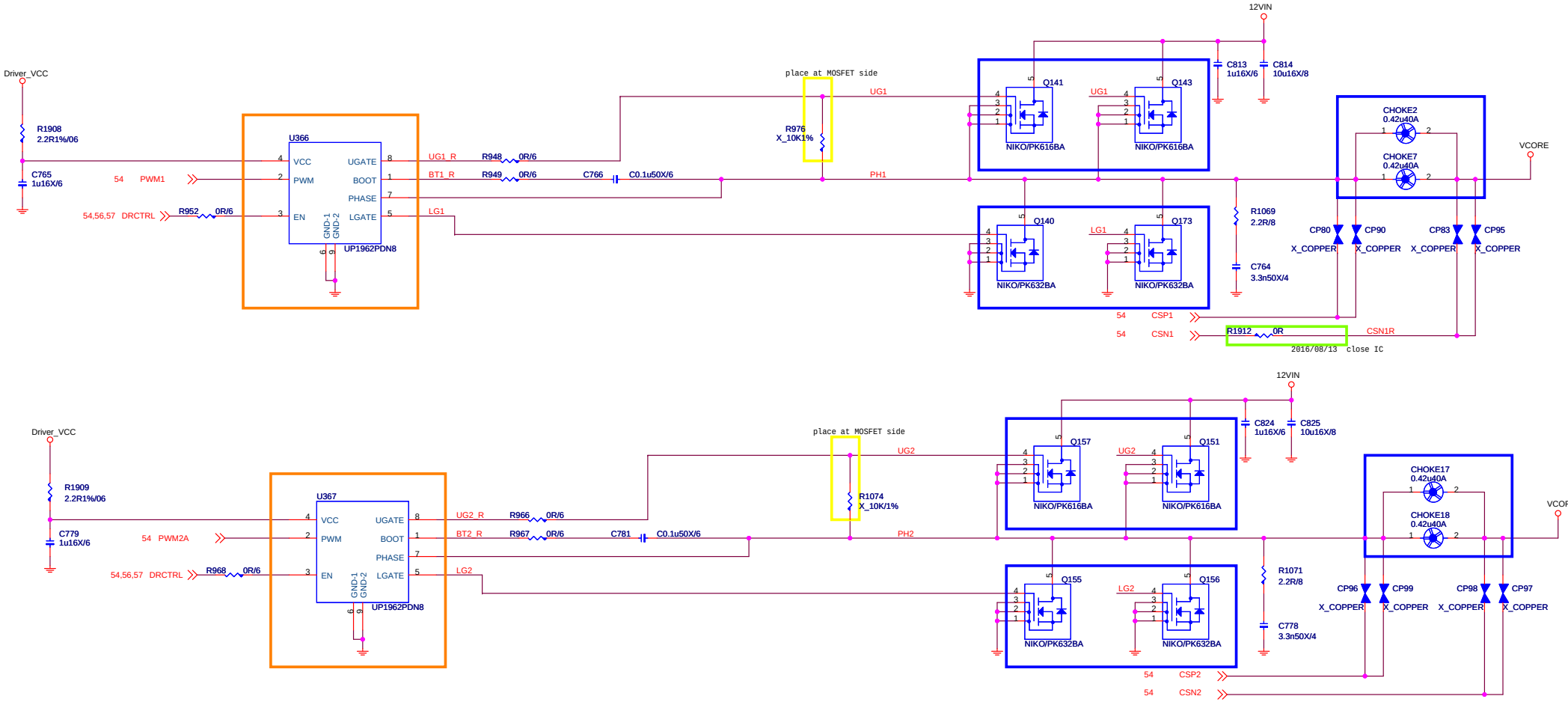
RT9 放在CHOKE2與CHOKE7中間

12VIN R705 0R/6
+12VIN R707 X_0R/6 Driver_VCC

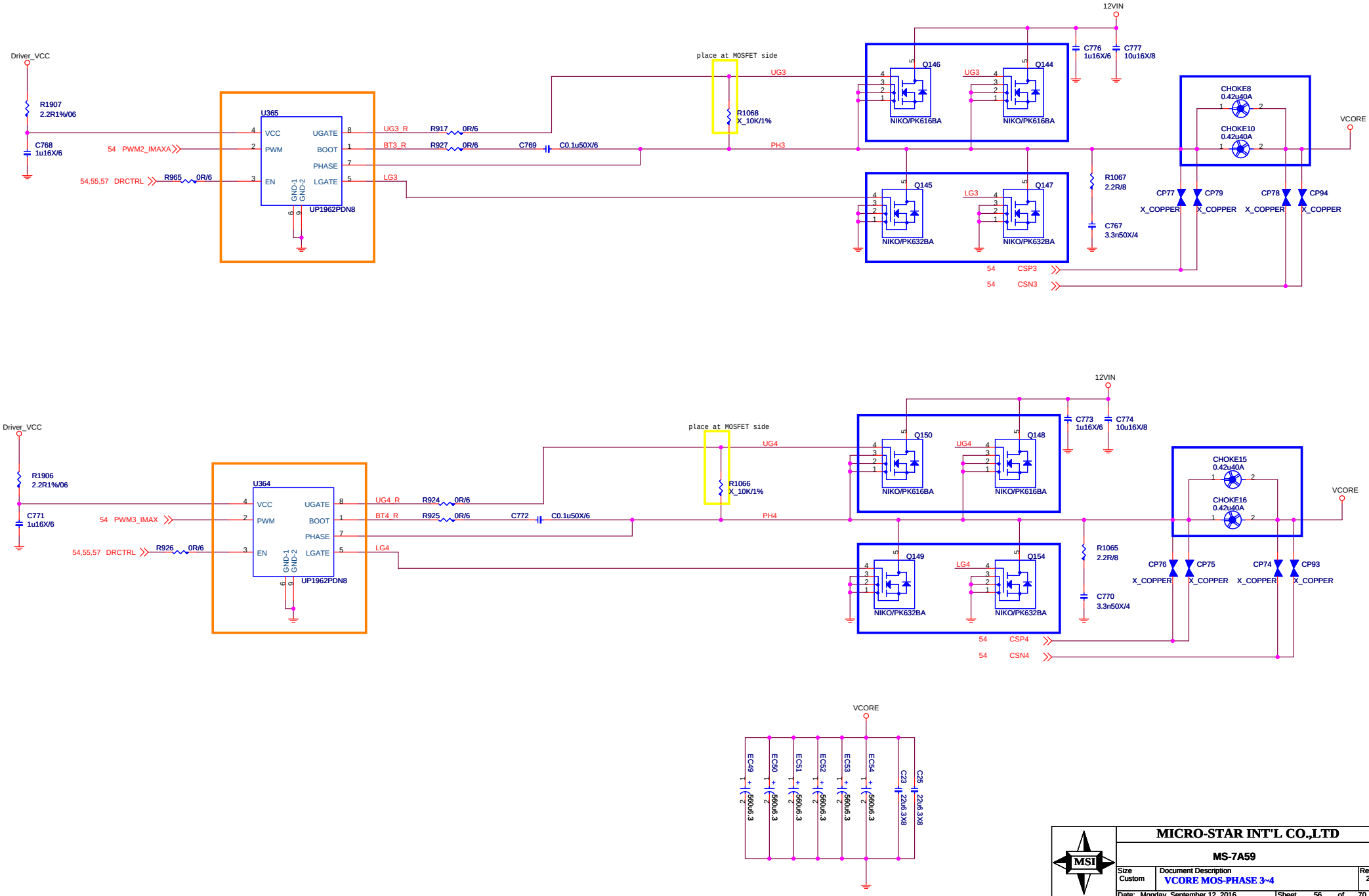
NTC1a RT6 100KRT1%4

NTC_Lb NTC_La RT9 10KRT1%/4

RT6放置在VccCORE 這組switching power 最熱的地方



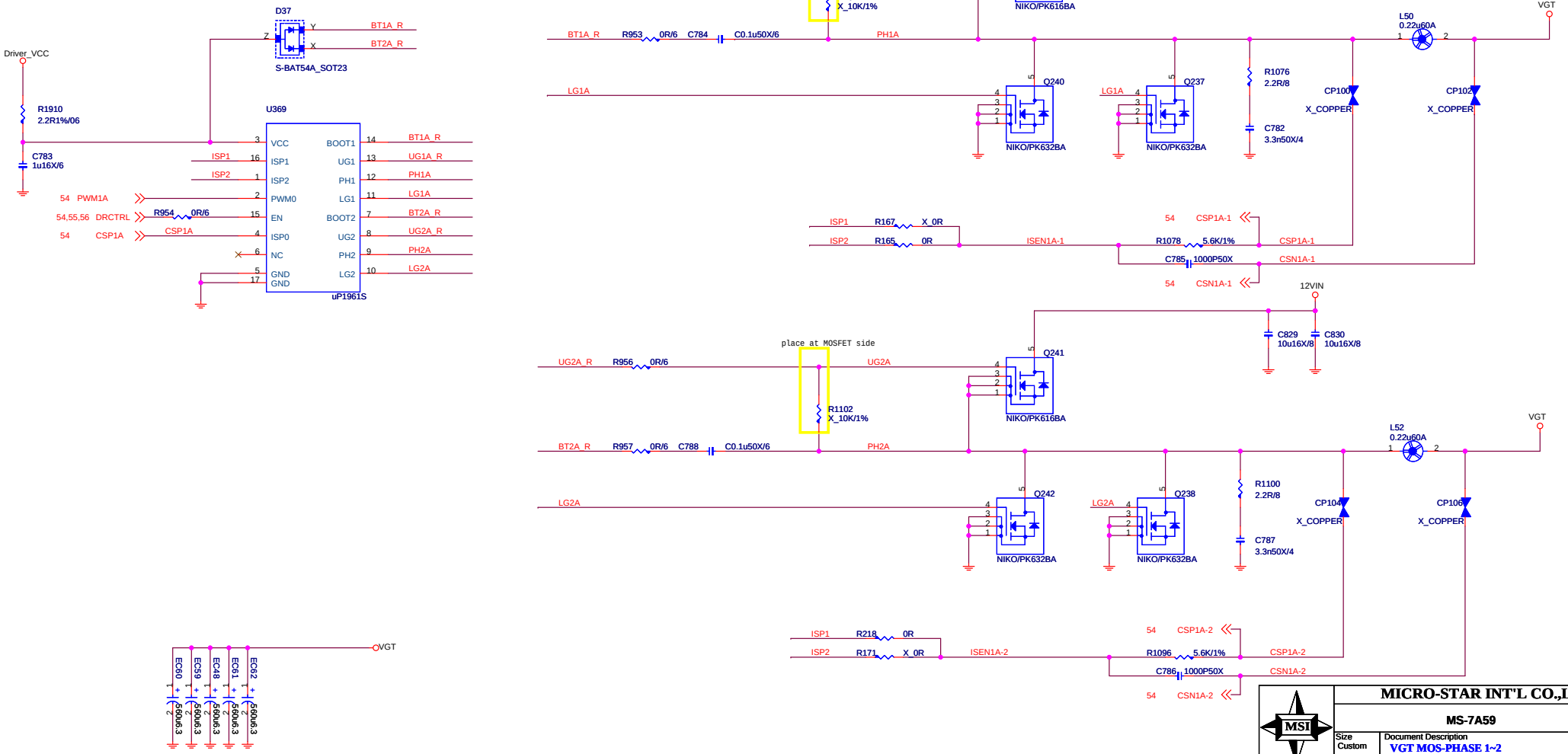
MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: VCORE MOS-PHASE 1~2	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 55 of 70	



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A59	
Size: Custom	Document Description: VCORE MOS-PHASE 3~4	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 56 of 70	

RT7 放在L50與L52中間

RT8放置在VccGT 這組switching power 最熱的地方



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MS-7A59

Size	Document Description	Rev
Custom	VGT MOS-PHASE 1~2	2.0

Date: Monday, September 12, 2016 Sheet 57 of 70

VCCIO

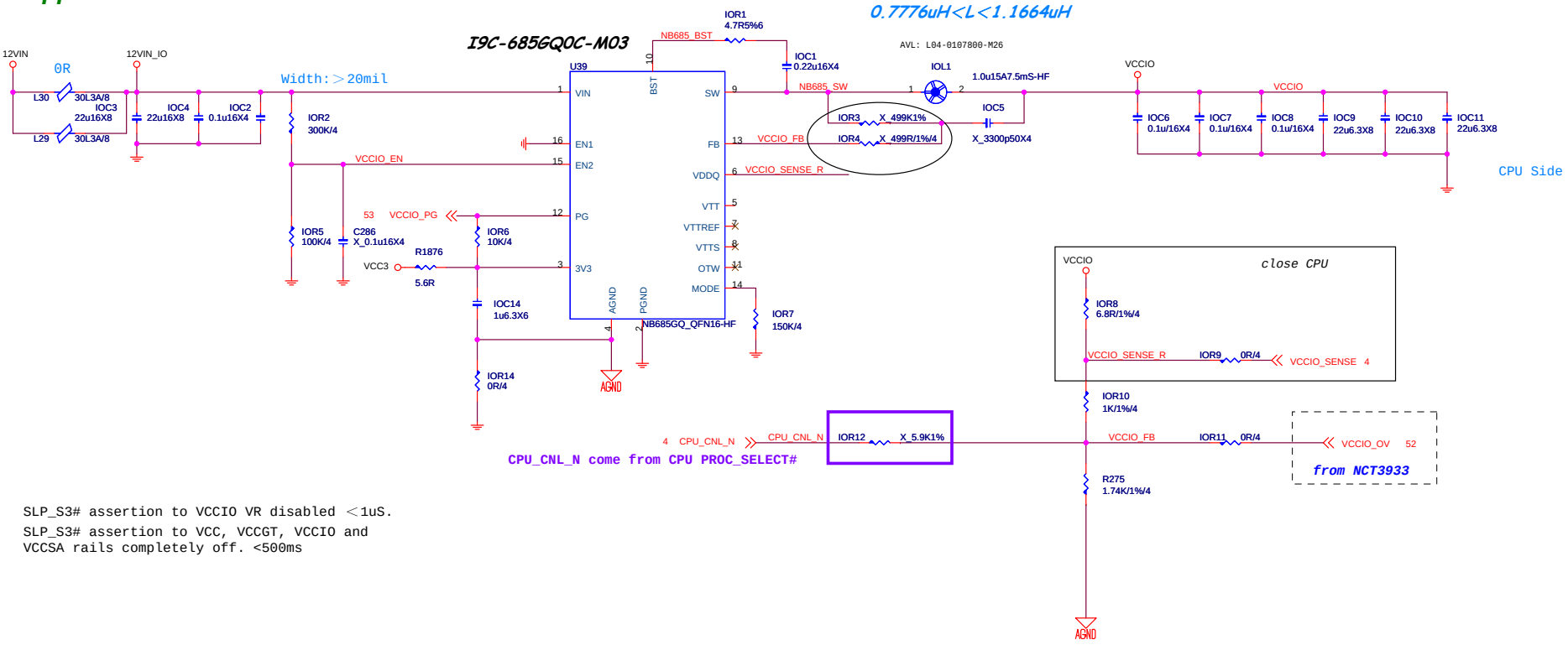
0.95V; 5.5A

IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*

support 0V=>NB685

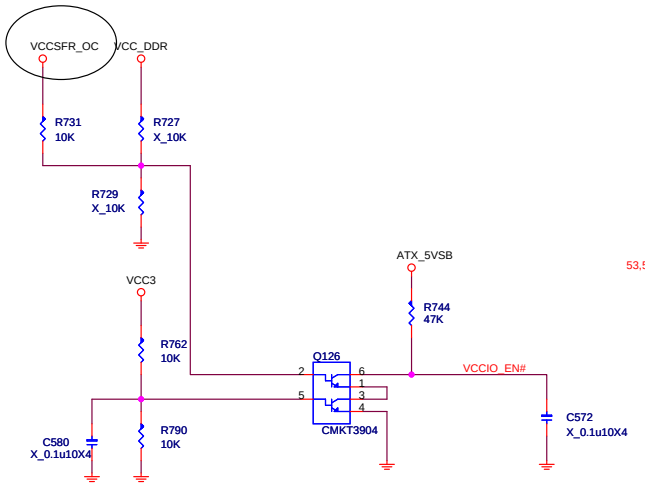
0.7776uH<L<1.1664uH

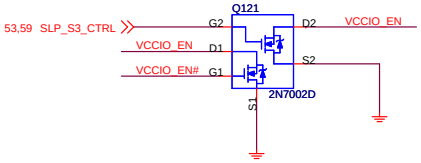
I9C-685GQ0C-M03



CPU_CNL_N come from CPU PROC_SELECT#

SLP_S3# assertion to VCCIO VR disabled ＜1uS.
SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms





SLP_S3# assertion to VR disabled
max:1us

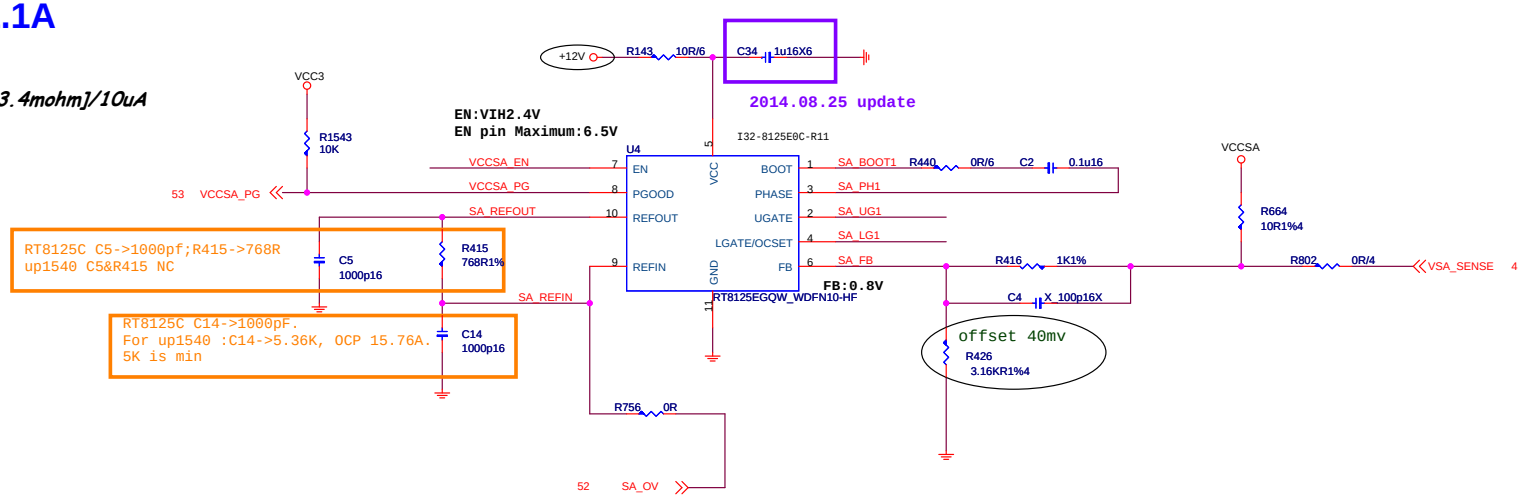
MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: CPU PWR_VCCIO	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 58 of 70	

SA Power:1.05V,11.1A

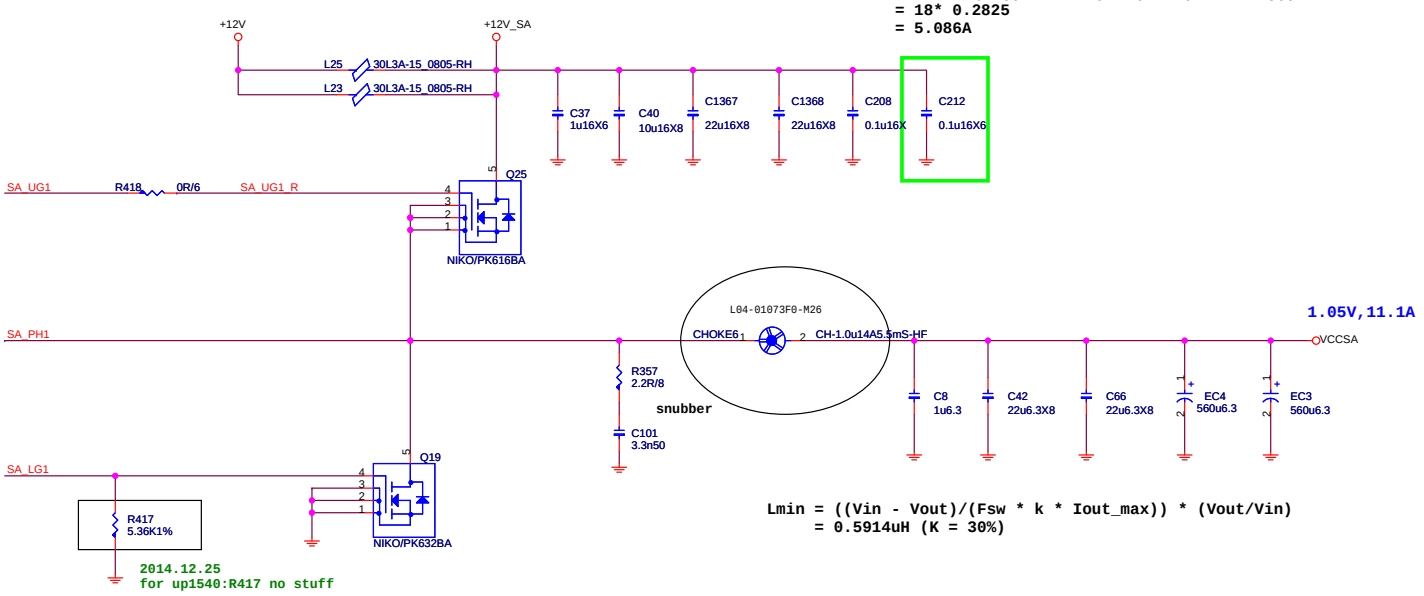
*OCP =11.1A*1.4=15.54A*
*Rocs(R417)=OCP*Rdson(Low side)3.4mohm]/10uA*
=15.54(3.4)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm



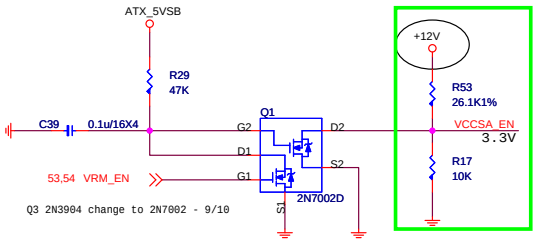
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 18* 0.2825
= 5.086A



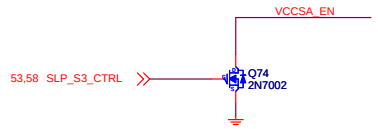
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

VRM_EN線路update

Pull up by layout&Check level



EN:VIH2.4V
EN pin Maximum:6.5V



SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

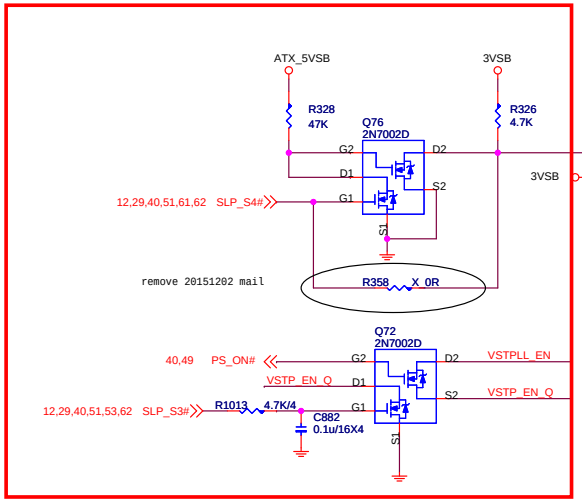
MICRO-STAR INT'L CO.,LTD			
MS-7A59			
Size: Custom	Document Description: CPU PWR_SA-RT8125C		Rev: 2.0
Date: Monday, September 12, 2016	Sheet 59 of 70		

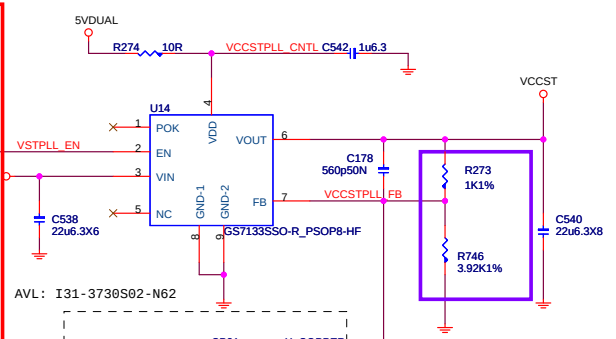
VCCST

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO and H110





NO OV,R26->25.5K,R27->100K, C178 unstuff

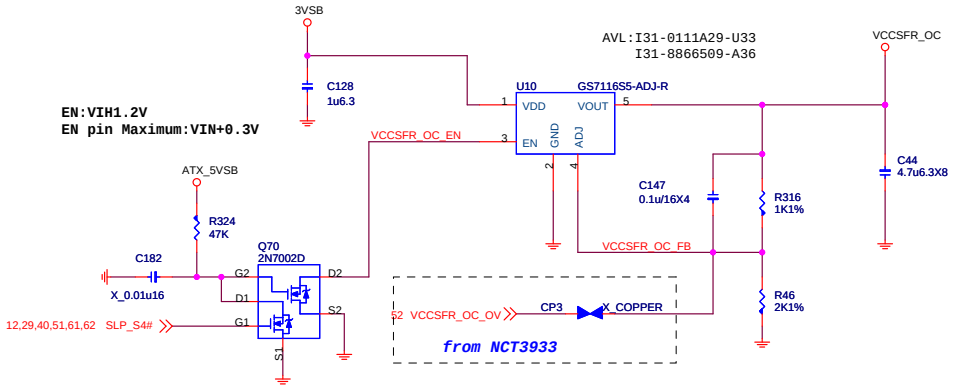
VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

VCCPLL_OC

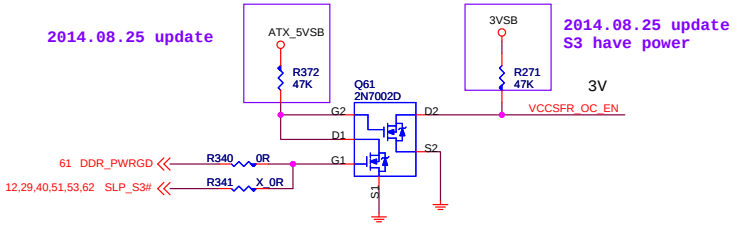
1.2V; 110mA

2014.08.21 update



EN:VIH1.2V
EN pin Maximum:VIN+0.3V

2014.08.25 update



2014.08.25 update
S3 have power

MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: CPU PWR_ST/PLL	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 60 of 70	

DDR4_1.2V 2.5A+9.5A+1.2A=13.5A

2.8A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

OCP =13.5A*1.5=20.25A

Rocs(R3)=OCP*Rdson[(Low side)]/10uA

=20.25A*(4.6)mohm/10uA

=9.315Kohm

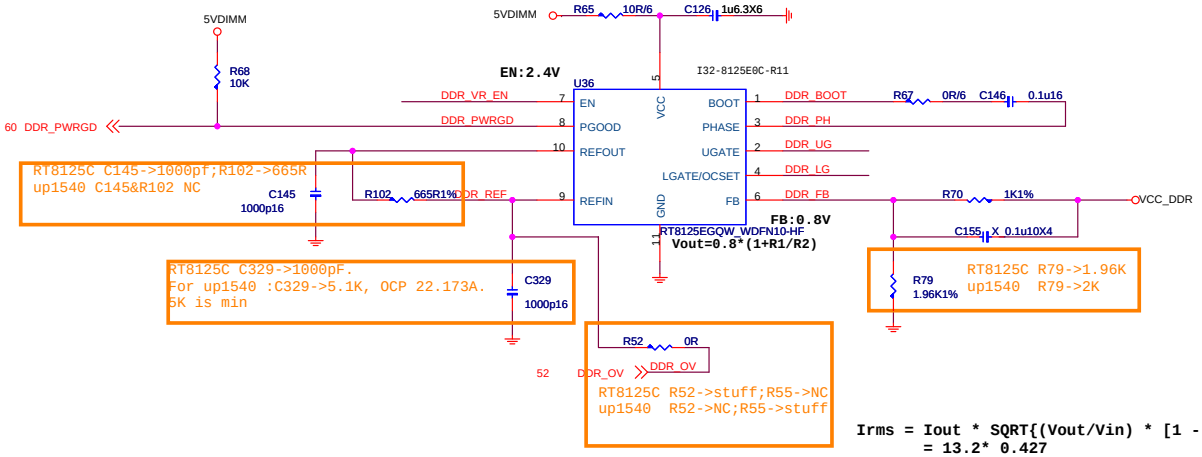
Rocpset:7.32K

OCP=Rocset*Rdson(Low side)/10uA

=7.32K*3.6mohm/10uA

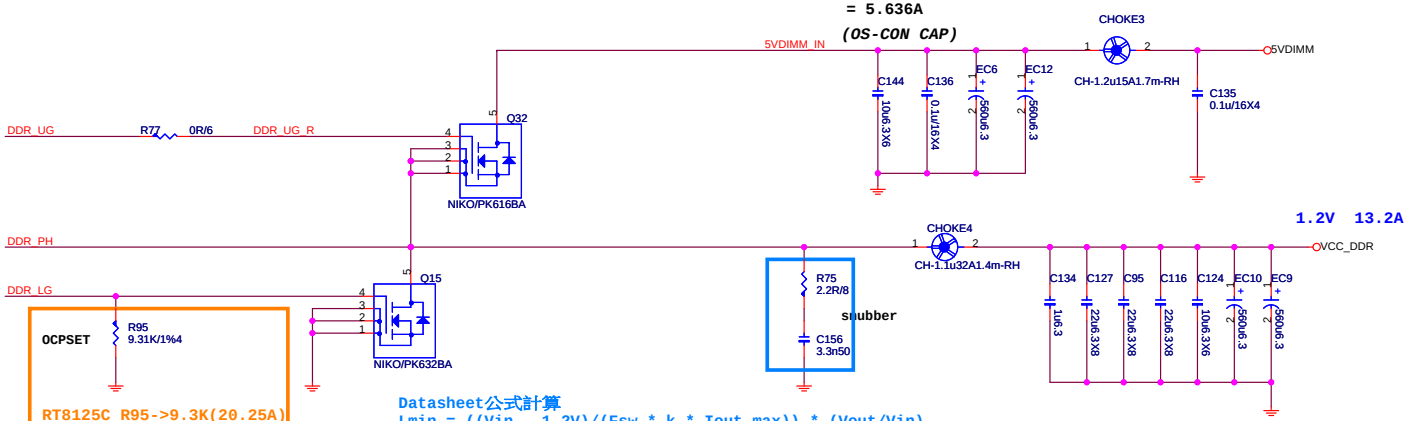
=20.3A

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm



Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A

(OS-CON CAP)



1.2V 13.2A

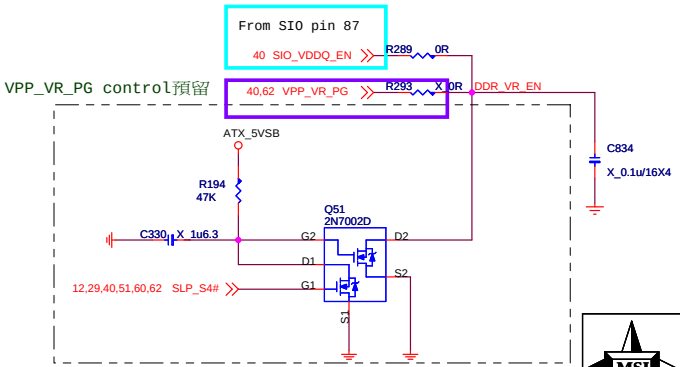
Datasheet公式計算

Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)

= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH＜L＜1.2897uH

2014.12.17 update



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MS-7A59

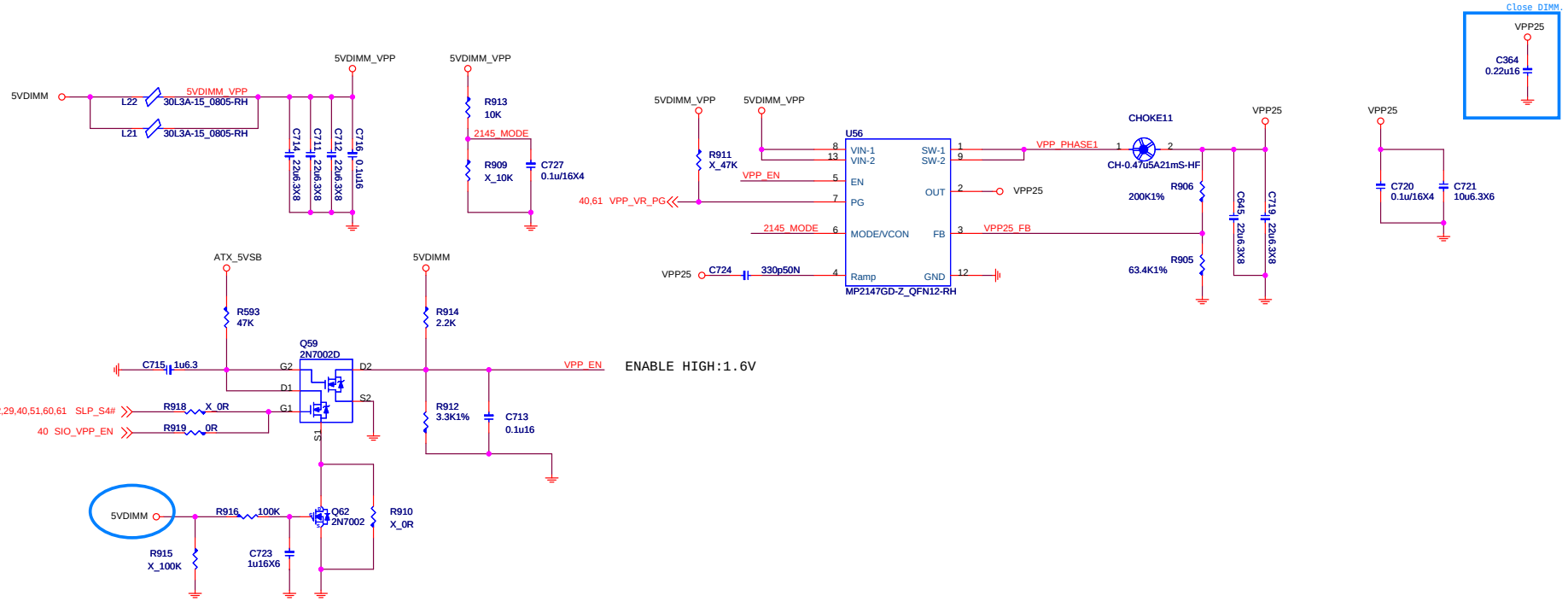
Size	Document Description	Rev
Custom	DDR4 Power-RT8125C	2.0

Date: Monday, September 12, 2016 Sheet 61 of 70

4DIMM :2.84A FOR DDR VPP2.5V

VPP25 Power

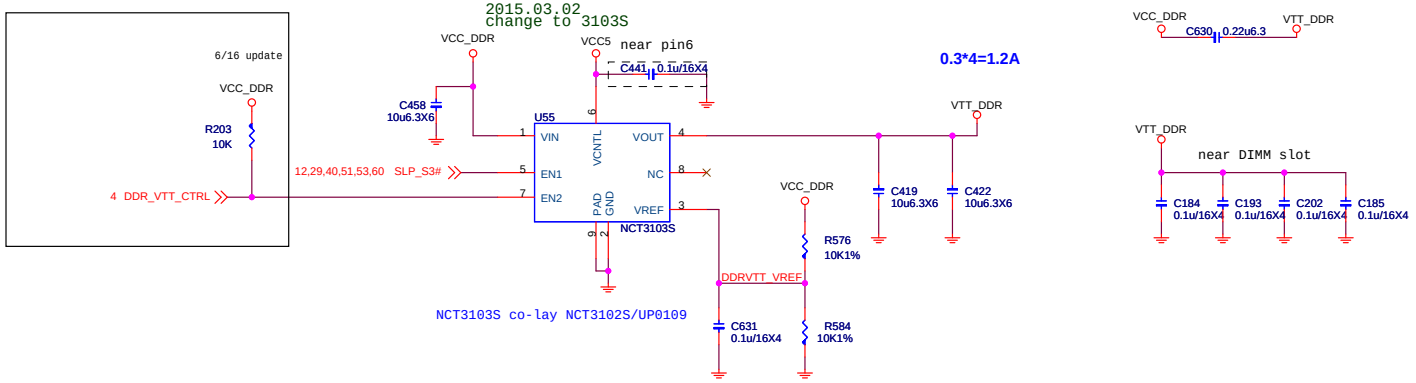
2.5V; 2.24A



ENABLE HIGH:1.6V

To make sure VPP EN after 5VDIMM stable

DDR VTT Power



MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size: Custom	Document Description: DDR4 Power-VPP25	Rev: 2.0
Date: Monday, September 12, 2016	Sheet 62 of 70	

PCH_1VSB

1.0V; 11.83A

Rdson(low)4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

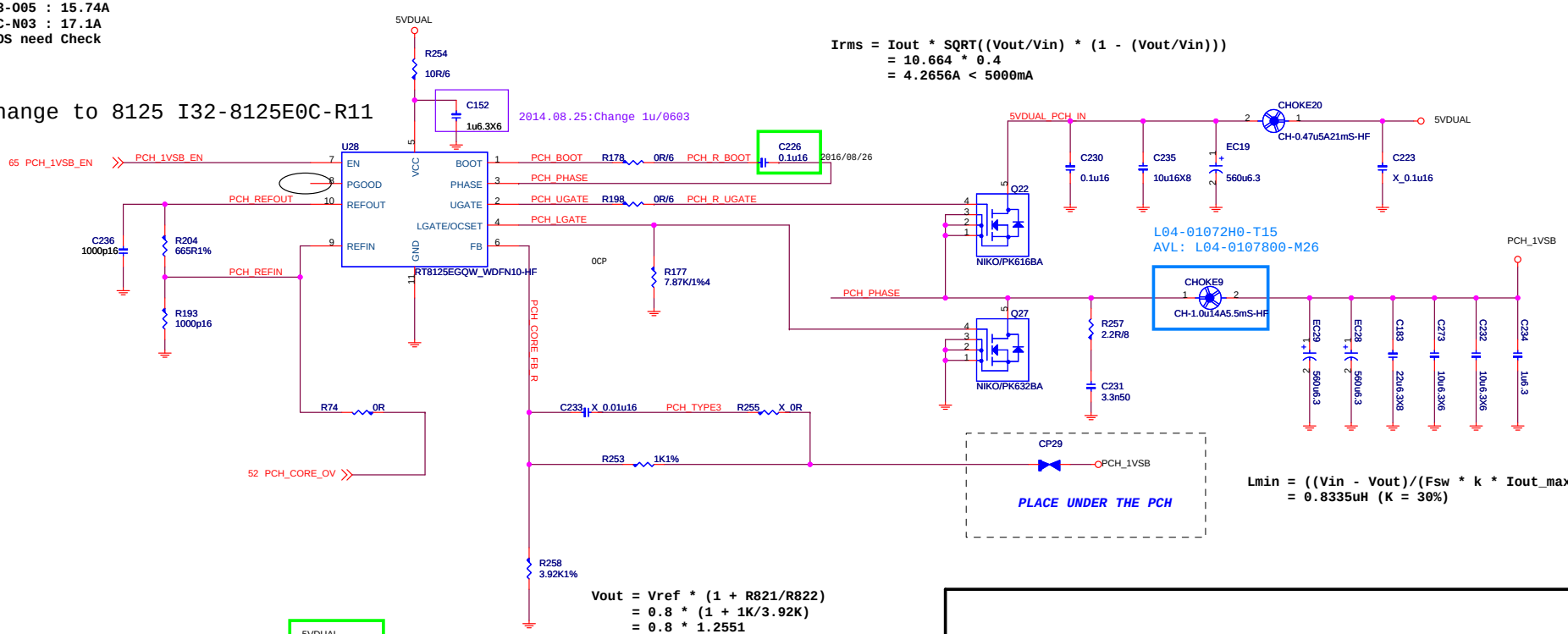
OCP = 17.745A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 11.83 * 4.6mohm / 10uA
= 8.16K

Rocs:7.87K,OCP:
D03-4C05N03-005 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

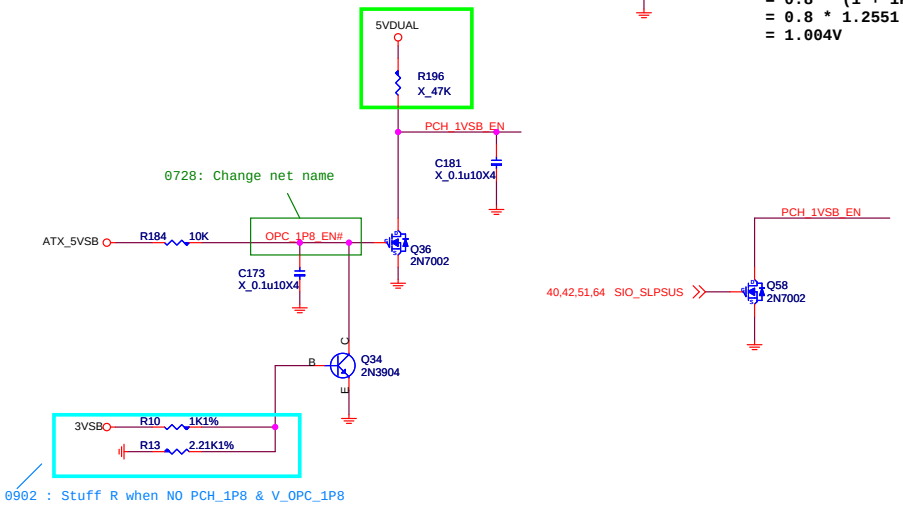
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

1504 change to 8125 I32-8125E0C-R11



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

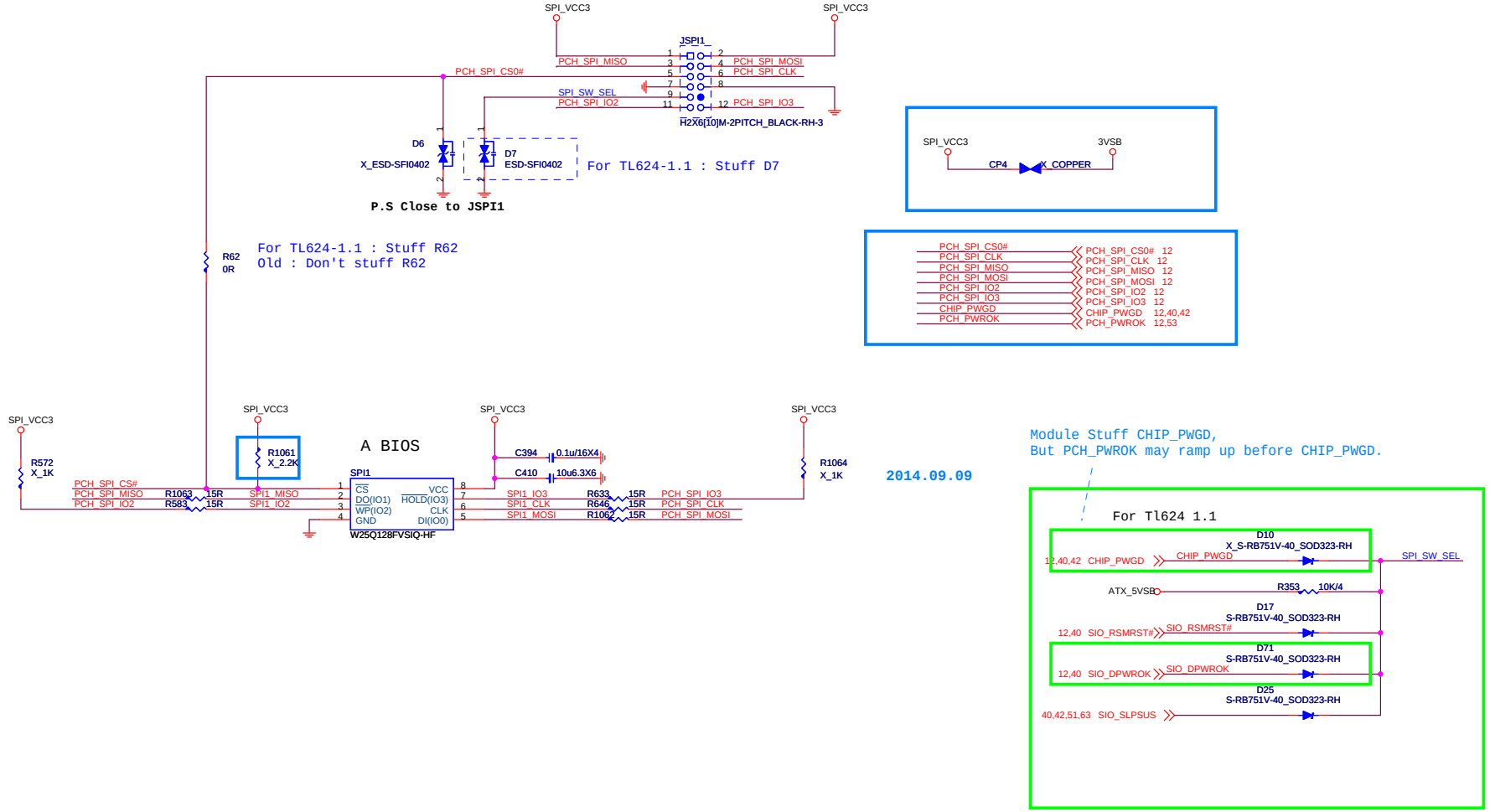


MICRO-STAR INT'L CO.,LTD

MS-7A59

Size	Document Description	Rev
Custom	PCH Core Power-RT8125	2.0

Date: Monday, September 12, 2016 | Sheet 63 of 70



MICRO-STAR INT'L CO.,LTD

MS-7A59

Size	Document Description	Rev
Custom	BIOS	2.0

Date: Monday, September 12, 2016 Sheet 64 of 70

Co-Lay NOT USE U1 , R150 STUFF

RTCRST# R150 X_0R/4 RTCRST# D

If STUFF R150 Please Check RTCRST# Double Pull High

20160629

2016/08/29

CLR_CMOS# R44 X_100K/4

CUT_VBAT R55 X_100K/4

JBAT1 H1X2M_BLACK-RH

VBAT R1094 20K

C607 1u6.3X6

D72 ESD-SFI0402

RTCRST# D

SIO_3VA R233 X_4.7K/4

40 CLR_CMOS# CLR_CMOS#

SIO_3VA R330 X_4.7K

40 CUT_VBAT CUT_VBAT

DIS_CHARGE

R232 100K/4

VBAT C739 0.1u/16X4

U12

CLR_CMOS function 1

INPUT1 CLR_CMOS# RTCRST#_PCH OUTPUT1 11 RTCRST# RTCRST 12

INPUT2 RTCRST#_D

CUT_VBAT function 2

INPUT3 CUTVBAT POWER_OFF OUTPUT2 12 POWER_OFF

INPUT4 DIS_CHARGE RTCRST#_SIO OUTPUT3 13 RTCRST# D RTCRST#_D 41

LOW SWITCH

VIN VBAT VBAT_PCH(POWER) VOUT 7 VBAT_PCH

NC-1 NC-2 GND-1 GND-2

X_SLG4B41231V_STQFN14-HF

if has cut other power,please use output 2.

if has discharge function R232 NC.

Co-Lay NOT U1 , Stuff R18

VBAT_PCH R236 X_0R VBAT

VBAT

3VDSW R113 3K1%/4

20mil

VBAT C26 1u6.3X6

D3 S-BAT54C_SOT23

R329 45.3K1%

R115 1K1%

VBAT1

BAT1 BAT-2P-RH-1

Co-Lay NOT USE U1 , ALL UNSTUFF

ATX_5VSB

R130 4.7K/4

R188 9.1K/1%/4

POWER_OFF

3VA_OFF# 3VA_OFF# 51

Q11 N-2N7002 3VDSW

3VSB_EN 3VSB_EN 51

Q13 N-2N7002 3VSB

PCH_1VSB_EN PCH_1VSB_EN 63

Q12 N-2N7002 PCH_1VSB

DCPRTC DCPRTC 16

R142 5.6K/1%

R162 2.2K/4

C27 0.1u/16X4

Q14 N-2N7002 PCH_TIME

MICRO-STAR INT'L CO.,LTD

MS-7A59

Size Custom | Document Description Clear CMOS | Rev 2.0

Date: Monday, September 12, 2016 | Sheet 65 of 70

PCB

PCB1

7A59_20

PD0-07A5920-G37
PD0-07A5920-E48

CPU_H1
CPU
鐵座
CPU_H1

BAT1_X1
BAT-BCR2032P-RH

LAN001
LAN+ USB20
X_LANCONN

R001
10K
X_10K

PCIE001
PCIE SLOT
X_PCIESLOTX16

PCIE002
PCIE SLOT
X_PCIESLOTX8

HS_AUDIO1
Audio Cover
E21-7978010-RH

LED001
LED RED
X_LED04-[BR]-50mA2.35V_1608-RH

DIMM001
DIMM
X_DDRIV

AMI_LABLE1
AMI_BIOS LABLE
BIOS_LABLE

HDMI_LA1
HDMI LABLE
HDMI LABEL

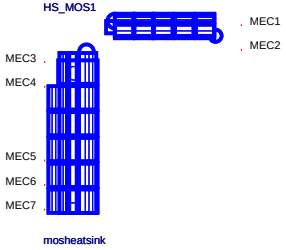
MKT_LA1
MKT LABLE
MKT LABEL

LED002
LED RED
X_LED04-[BR]-25mA2.35V_1711-RH

M002
M2
X_M2

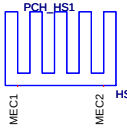
MKTLA001
MKT LABLE
X_MKT LABEL

HS_MOS1



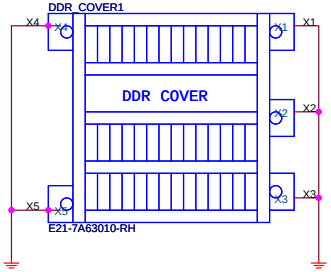
mosheatsink

PCH_HS1



HS-0407760-RH

DDR_COVER1

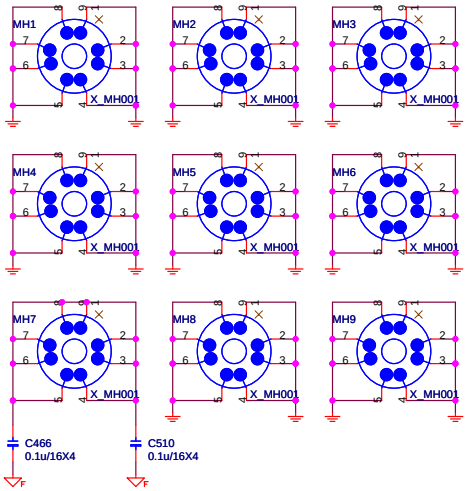


E21-7A63010-RH

VR_COVER1
VR Cover
E21-7976010-RH

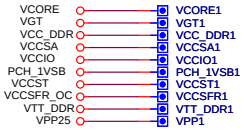
USB001
USB CONN
X_USBAM_RED
TYPE-A

Mounting Holes

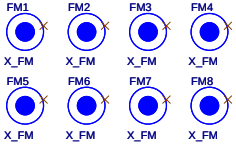


Simulation

Test point



Optical Fiducial Marks-120



To POWER 2015/02/03

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MS-7A59

Size	Document Description	Rev
Custom	Manual parts	2.0

Date: Monday, September 12, 2016 | Sheet 66 of 70