NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

COVINI

2018.12.27

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			
FILE NAME			
PCB P/N	60.xxxxx.xxxx	PCB VER	XXX

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
	MAIN BOARD

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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SMALL BOARD1&2

SMALL BOARD3

FOR 17 SMALL BOARD1&2

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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
TABLE OF THE CONTENT

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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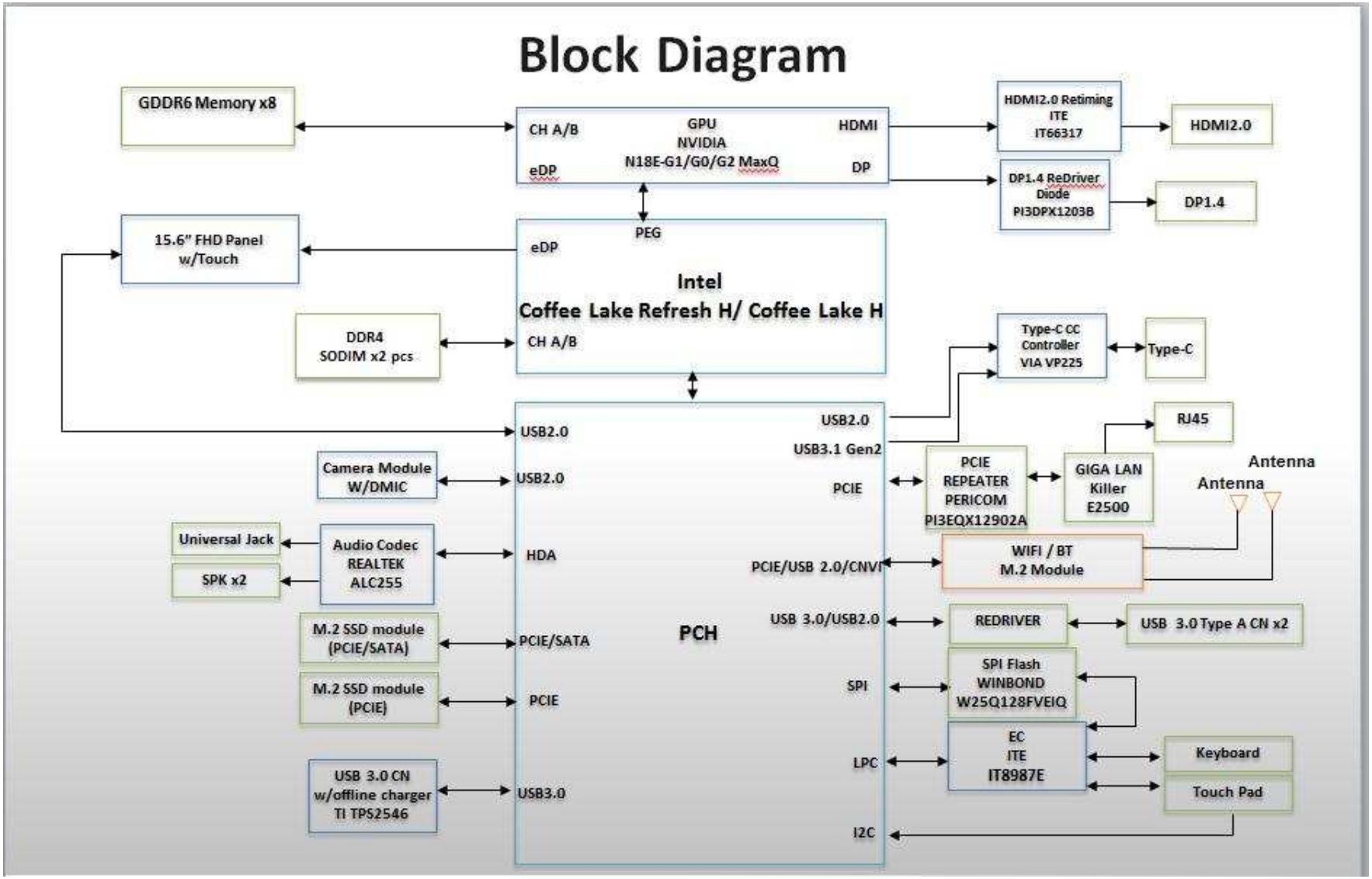
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

Block Diagram



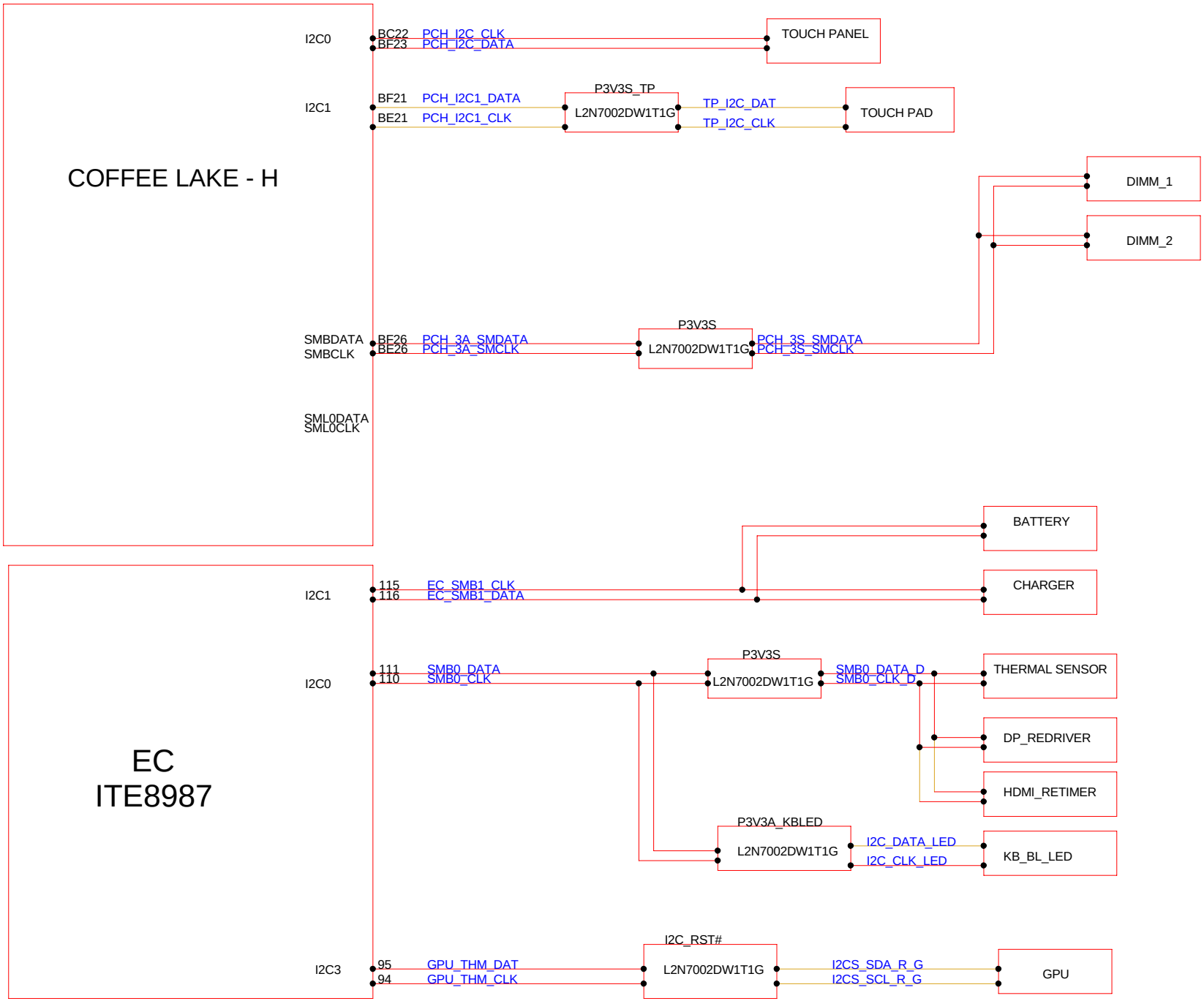
INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 3 of 130



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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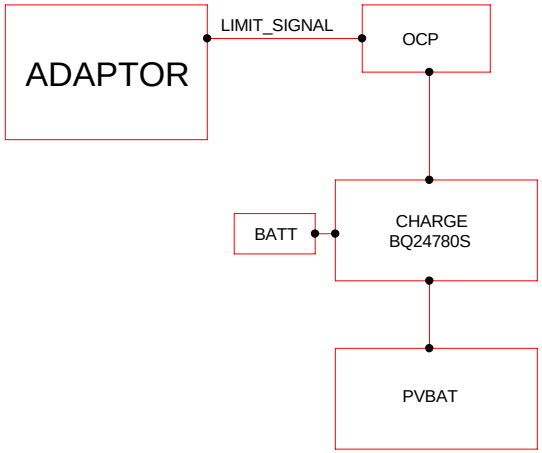
POWER BLOCK



IN/EN		OUT
PVBAT, EN_5V	SY8288CRAC	P5V0DS
PVBAT, EN_5V0	SY8284CRAC	P5V0
PVBAT, EN_3V	NB680AGD	P3V3DS
PVBAT, EN_VDDQ, EN_VTT	NB685AGQ	P1V2, P0V6S
PVBAT, EN_1V05V	SY8288CRAC	P1V05A
PVBAT, EN_VCCIO	NB681GD	PVCCIO
PVBAT, EN_PVCORE	NCP81215MNTXG	PVCORE
PVBAT, VRACPU_DRVON	NCP81151MNTBG	PVCCGT
PVBAT, VRACPU_DRVON	NCP81253MNTBG	PVCCSA

IN/EN		OUT
P5V0DS, EN_2V5	RT8097ALGE	P2V5
P3V3DS, EN_1V8	SY8088AAC	P1V8A
P3V3DS, P3V3A_5A_PWEN, CORE_PWEN	APL3523A	P3V3A, P3V3S
P5V0DS, CORE_PWEN, P1V8A, CORE_PWEN	APL3523A	P5V0S, P1V8S
P1V2, VCCPLL_OC_EN	PM514BA	VCCPLL_OC
P1V05A, RESUME_PWEN, CORE_PWEN	APL3523A	PVCCSTG, PVCCST

CHANGE by	XXX	DATE	21-OCT-2002
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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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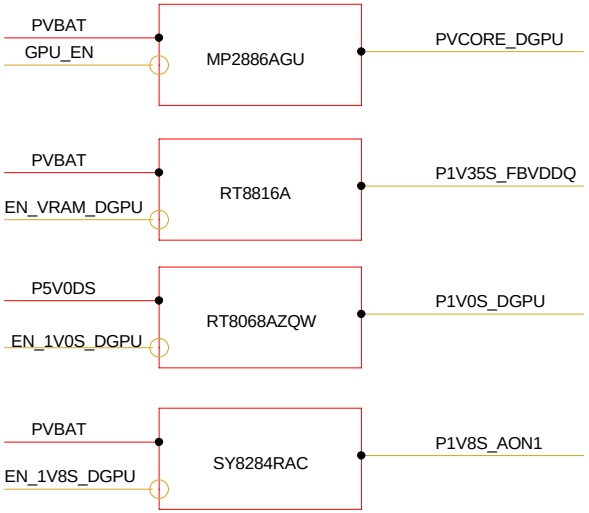
GPU POWER BLOCK

IN/EN OUT



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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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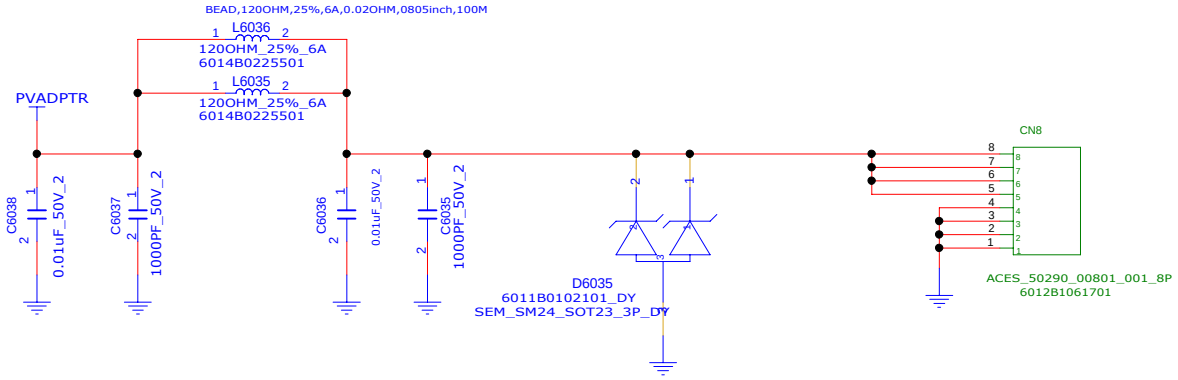

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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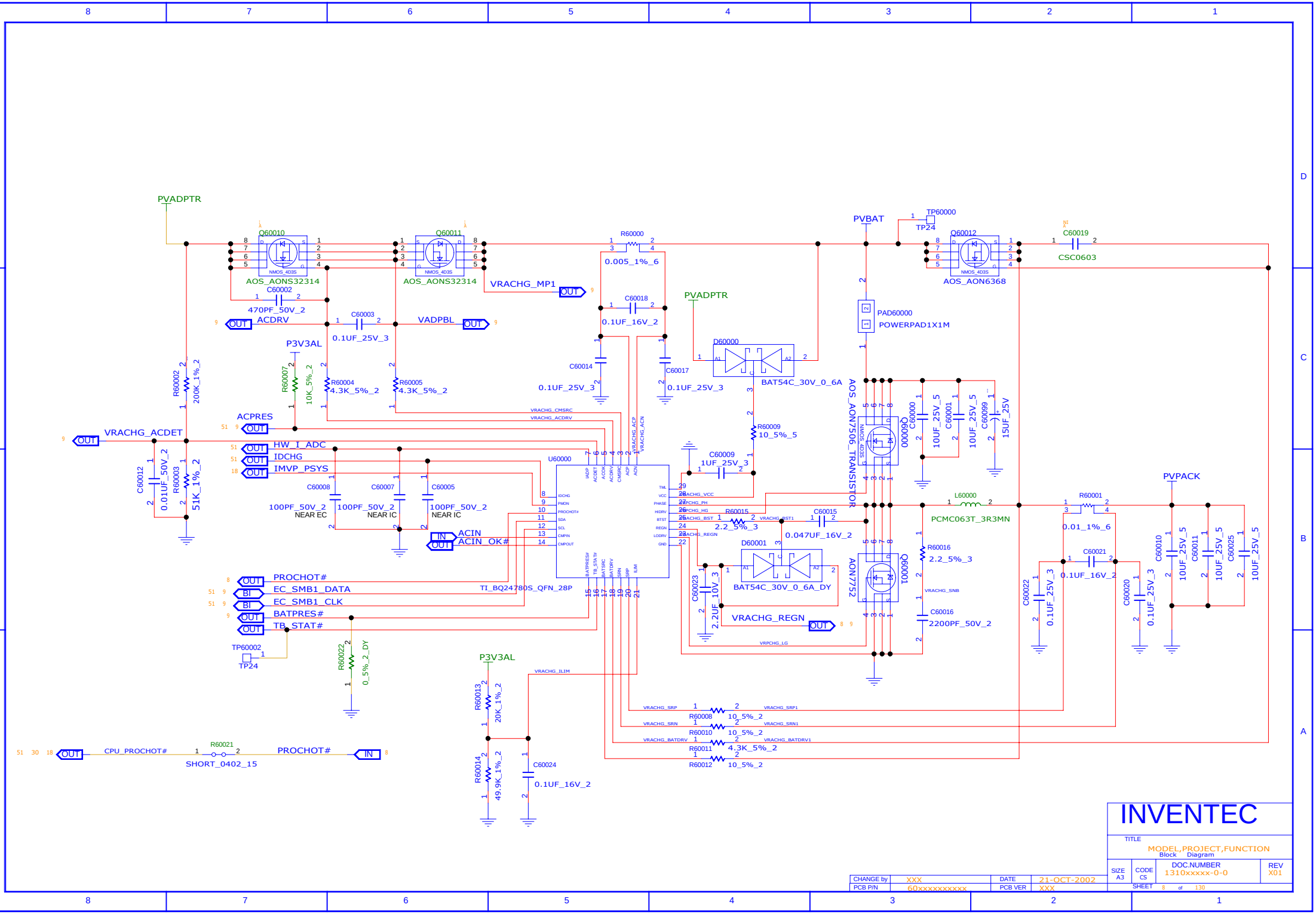
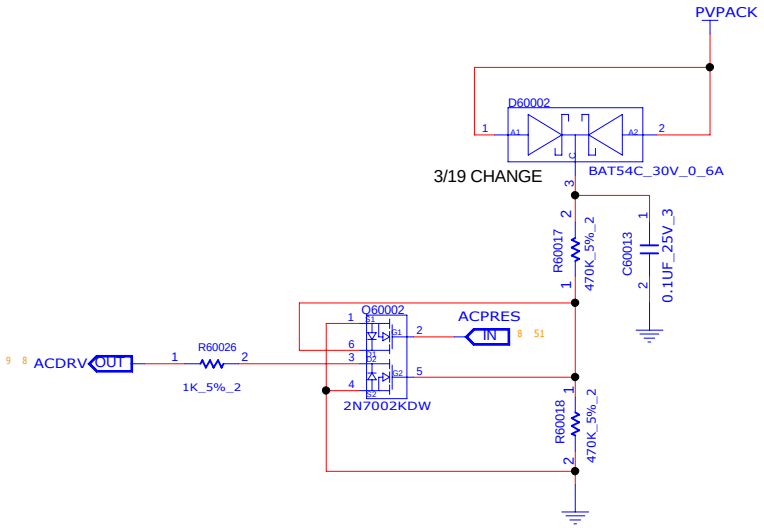


FOR CHARGER

SCP



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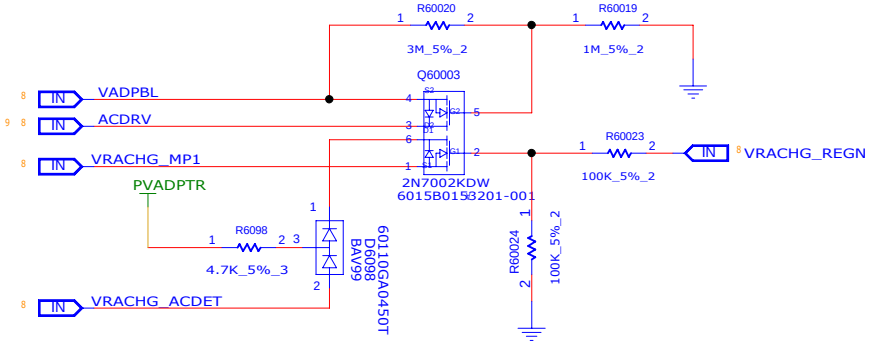

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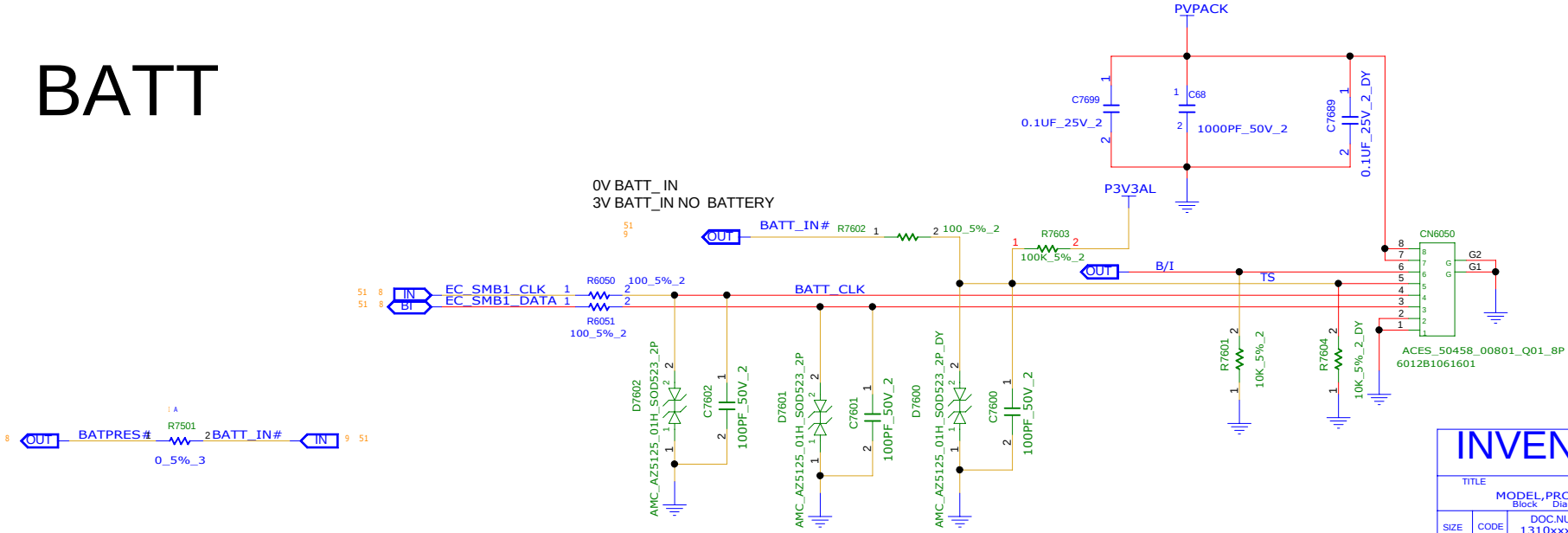
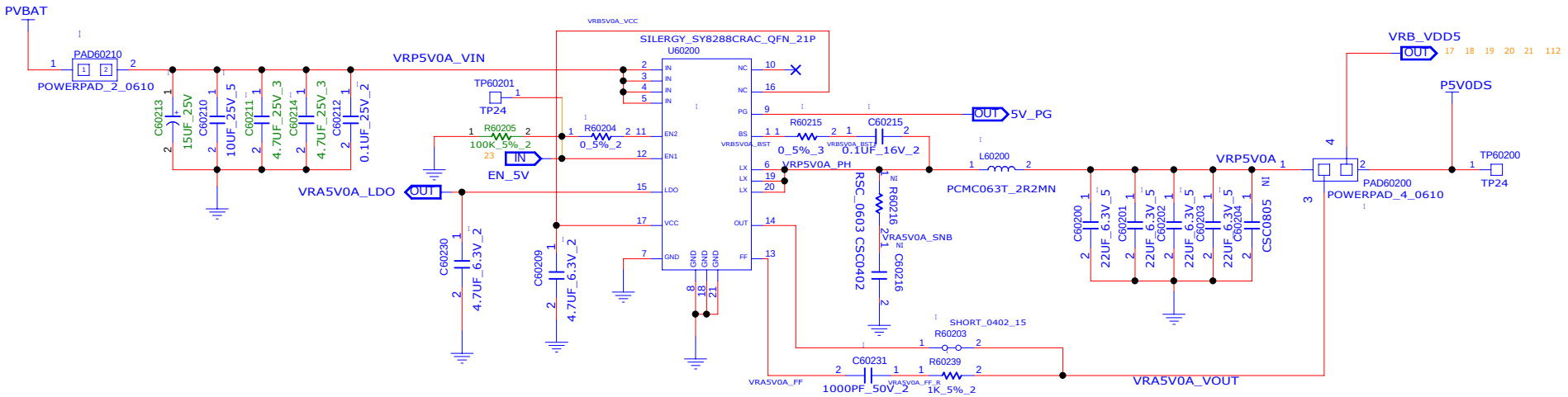


CHANGE by	XXX	DATE	21-OCT-2002	INVENTEC		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	TITLE: MODEL,PROJECT,FUNCTION Block Diagram		
				SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0 / REV X01
				SHEET 9 of 130		



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P5V0DS		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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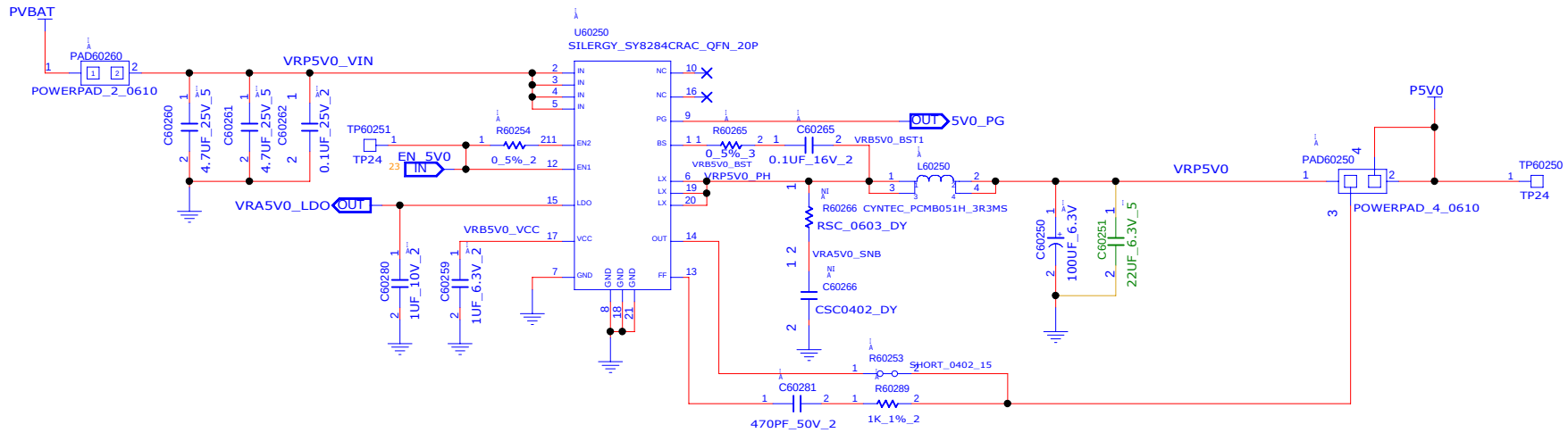
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE	MODEL_PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		REV X01	
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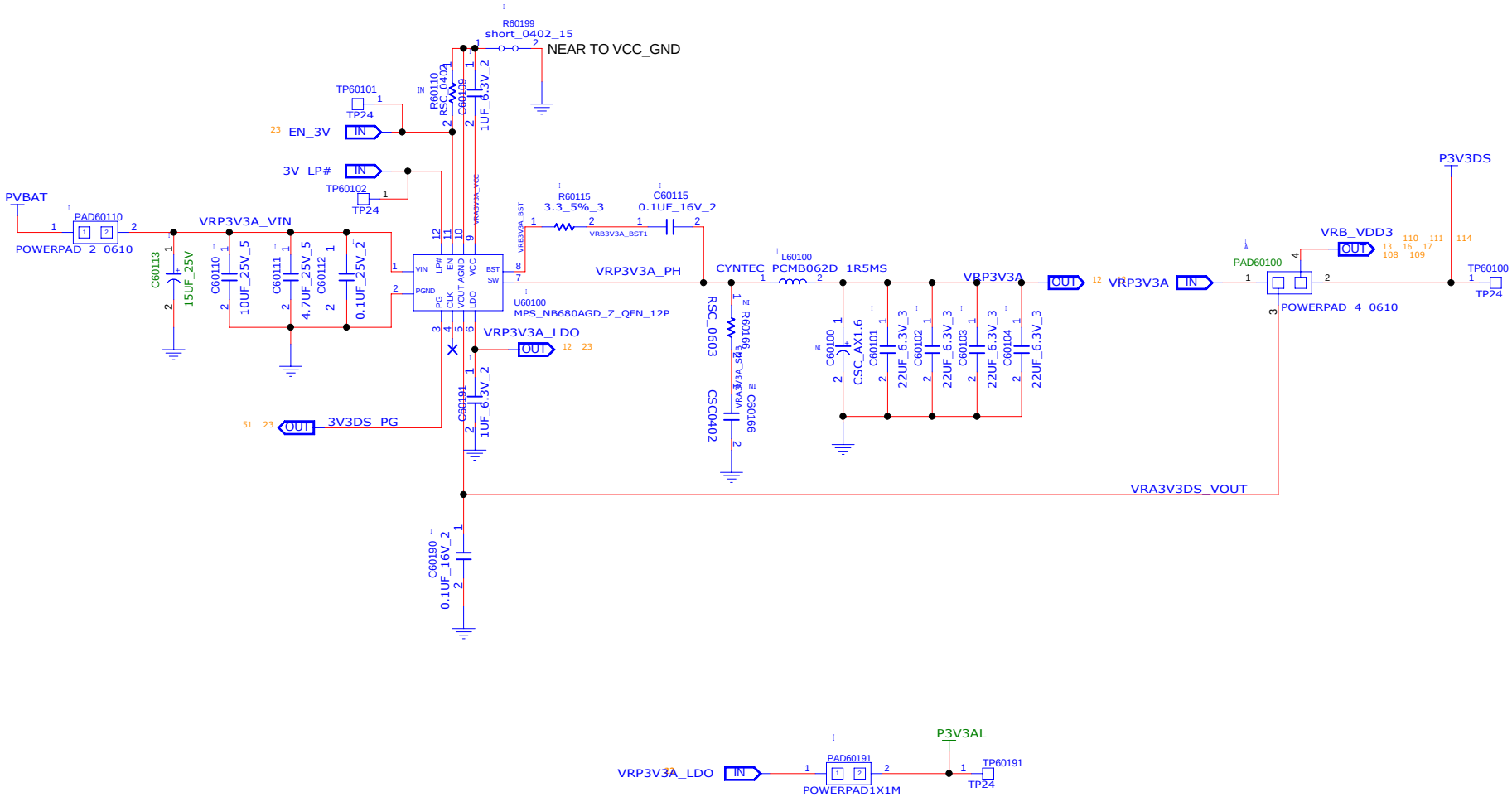

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P3V3DS_NB680A		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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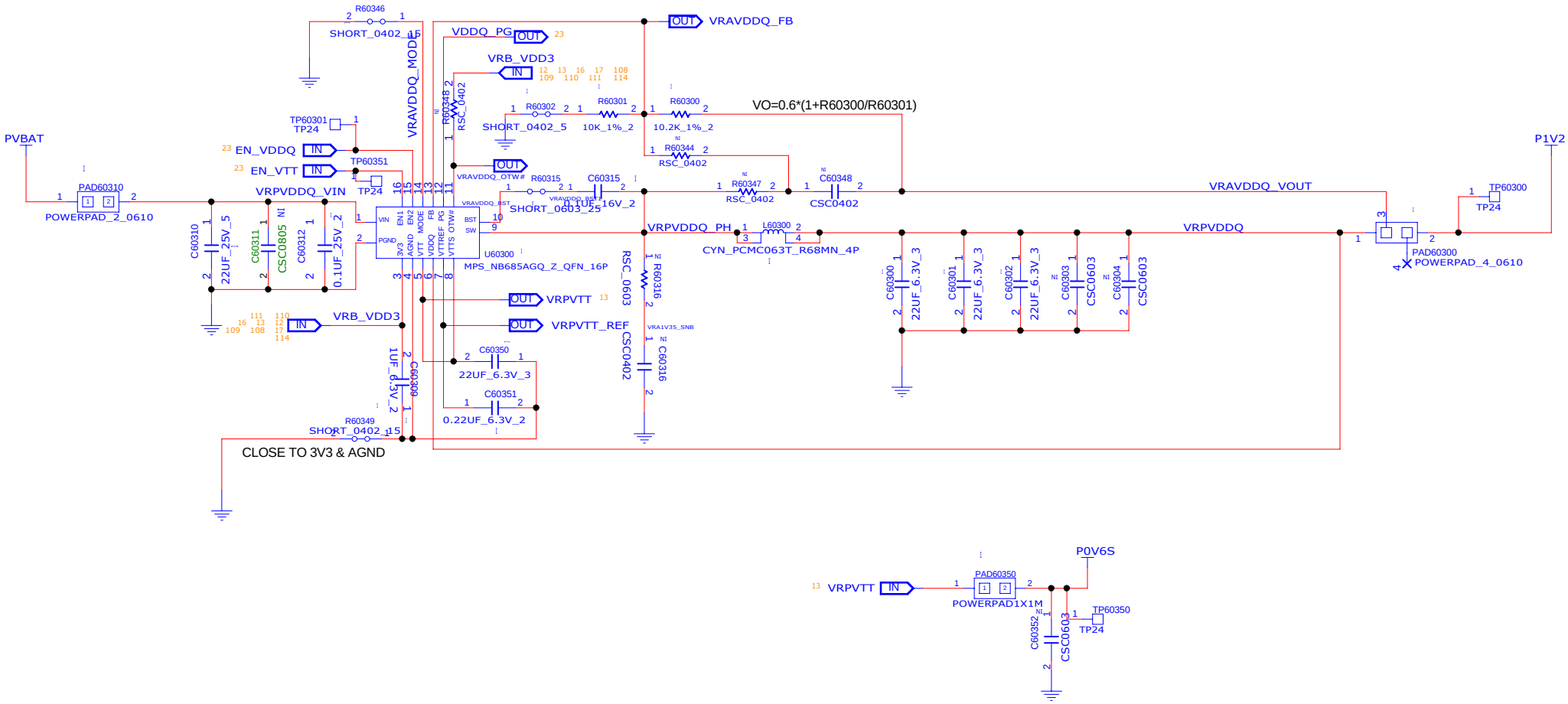
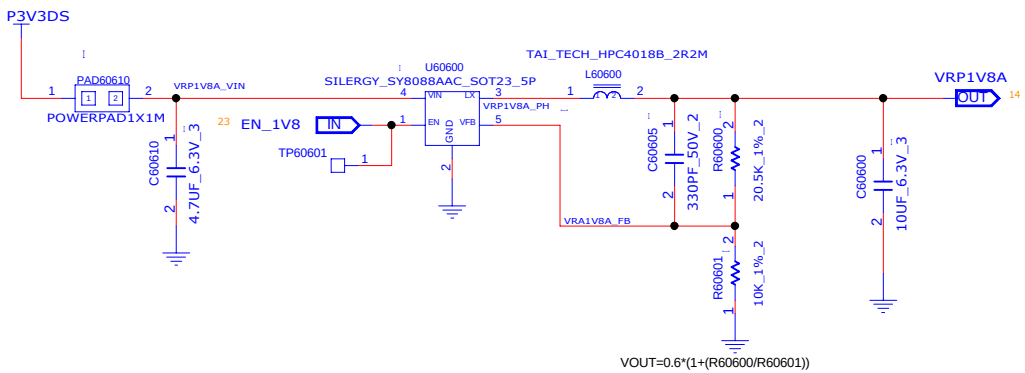
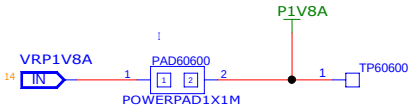
Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF







INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P1V8DS		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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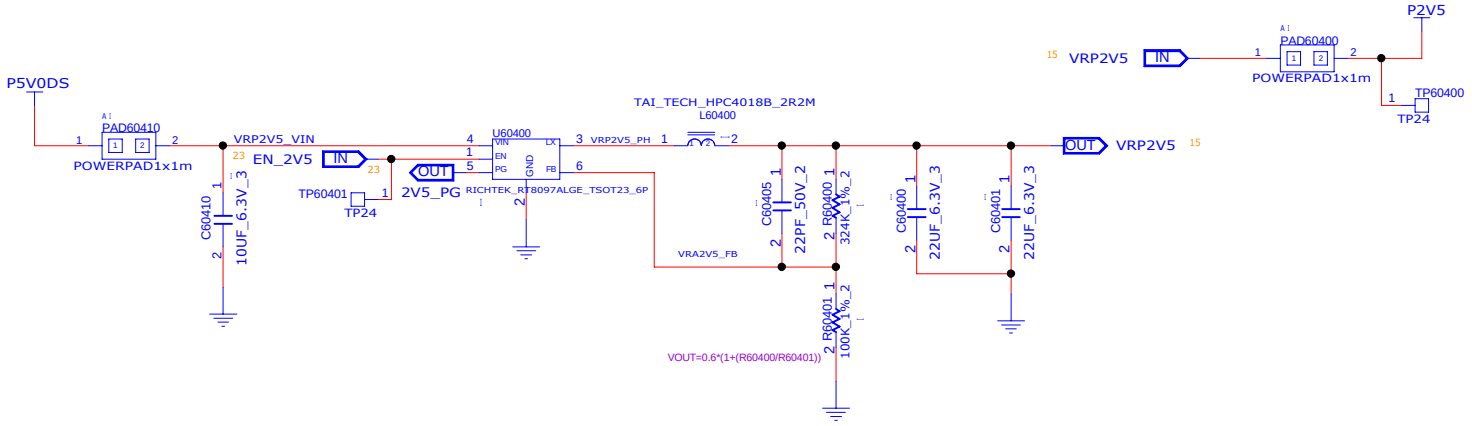
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
P2V5

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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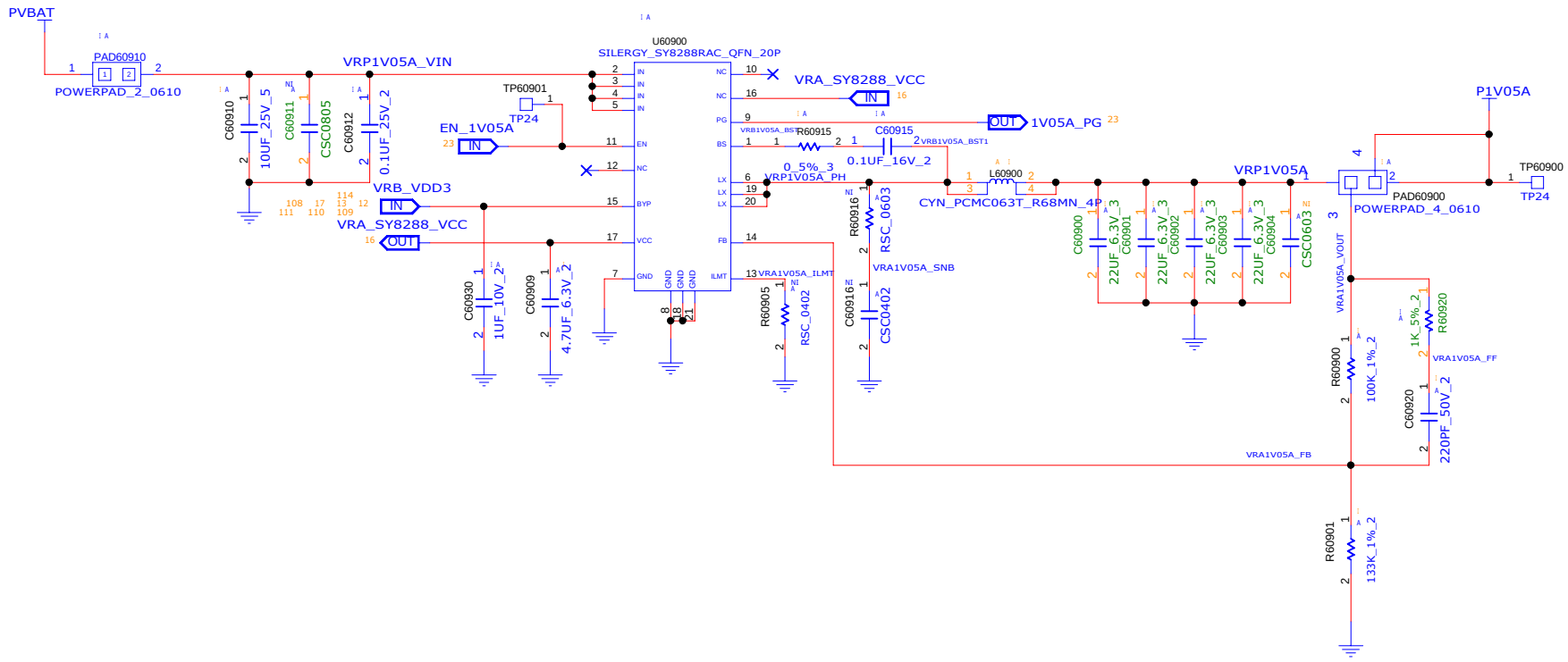

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P1V0A

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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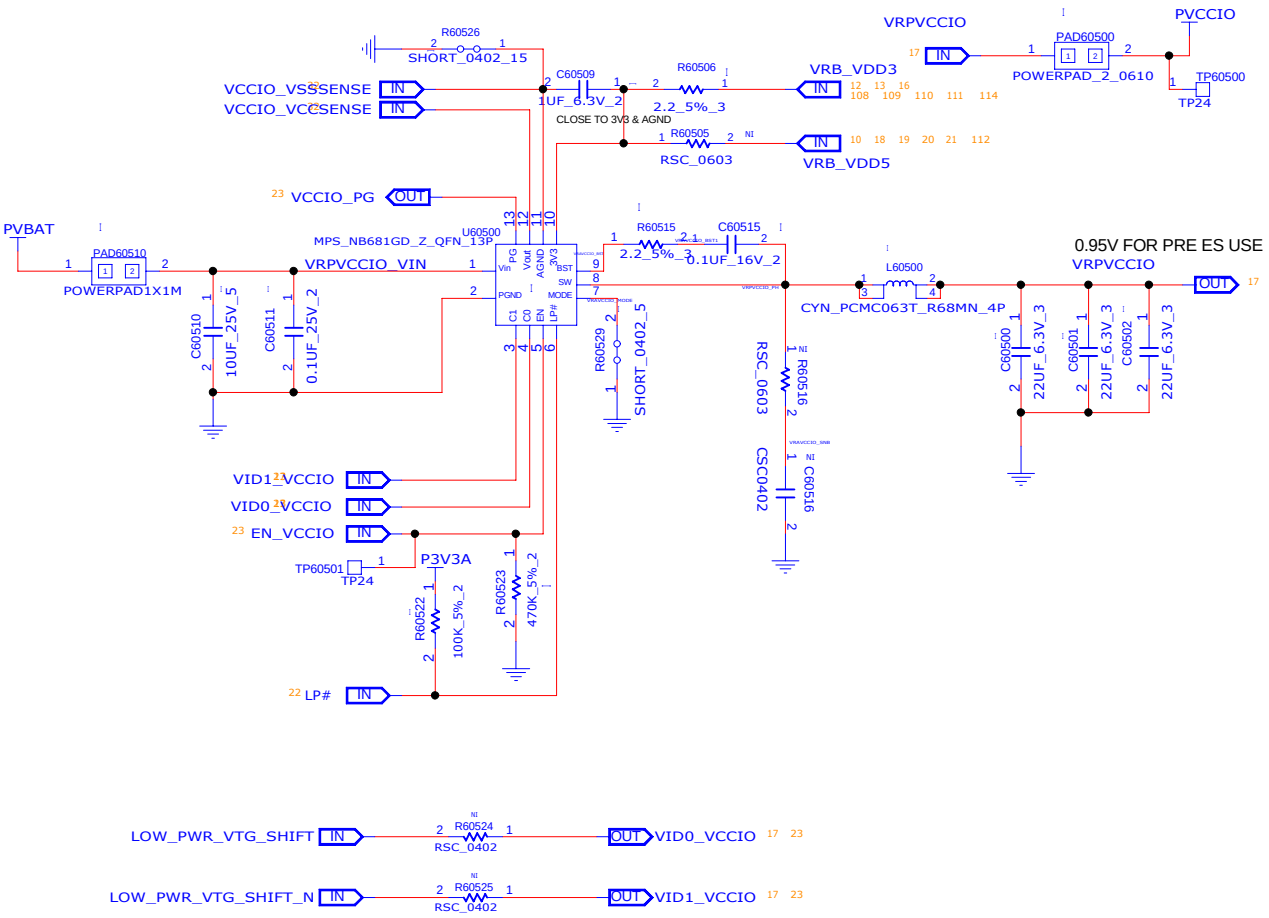
MODE	VR Rail	Resistor to GND (1% accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230 K
M3	EDRAM/V1.0A/EOPIO	100 K
M4	Others	150 K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PVCCIO		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
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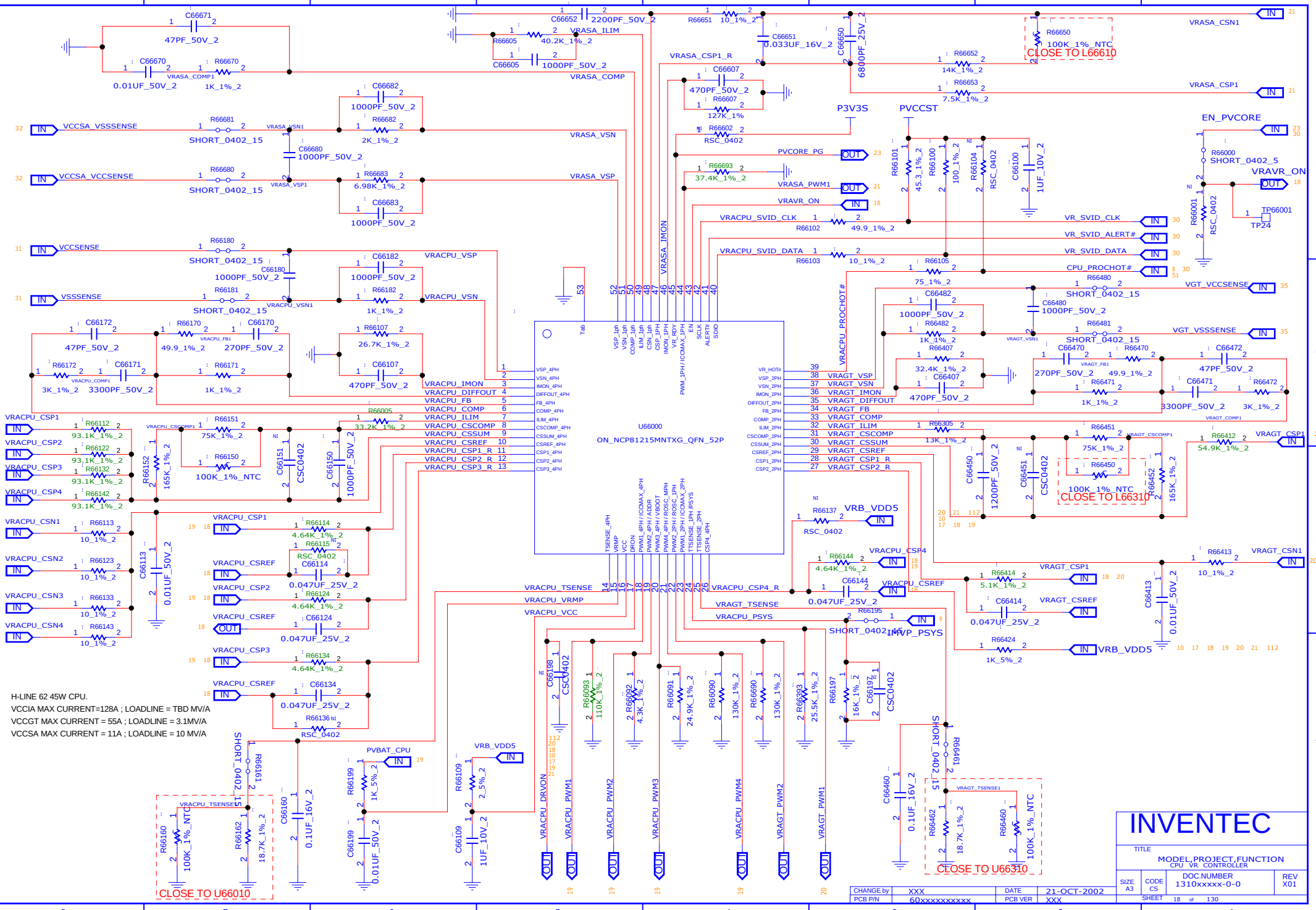

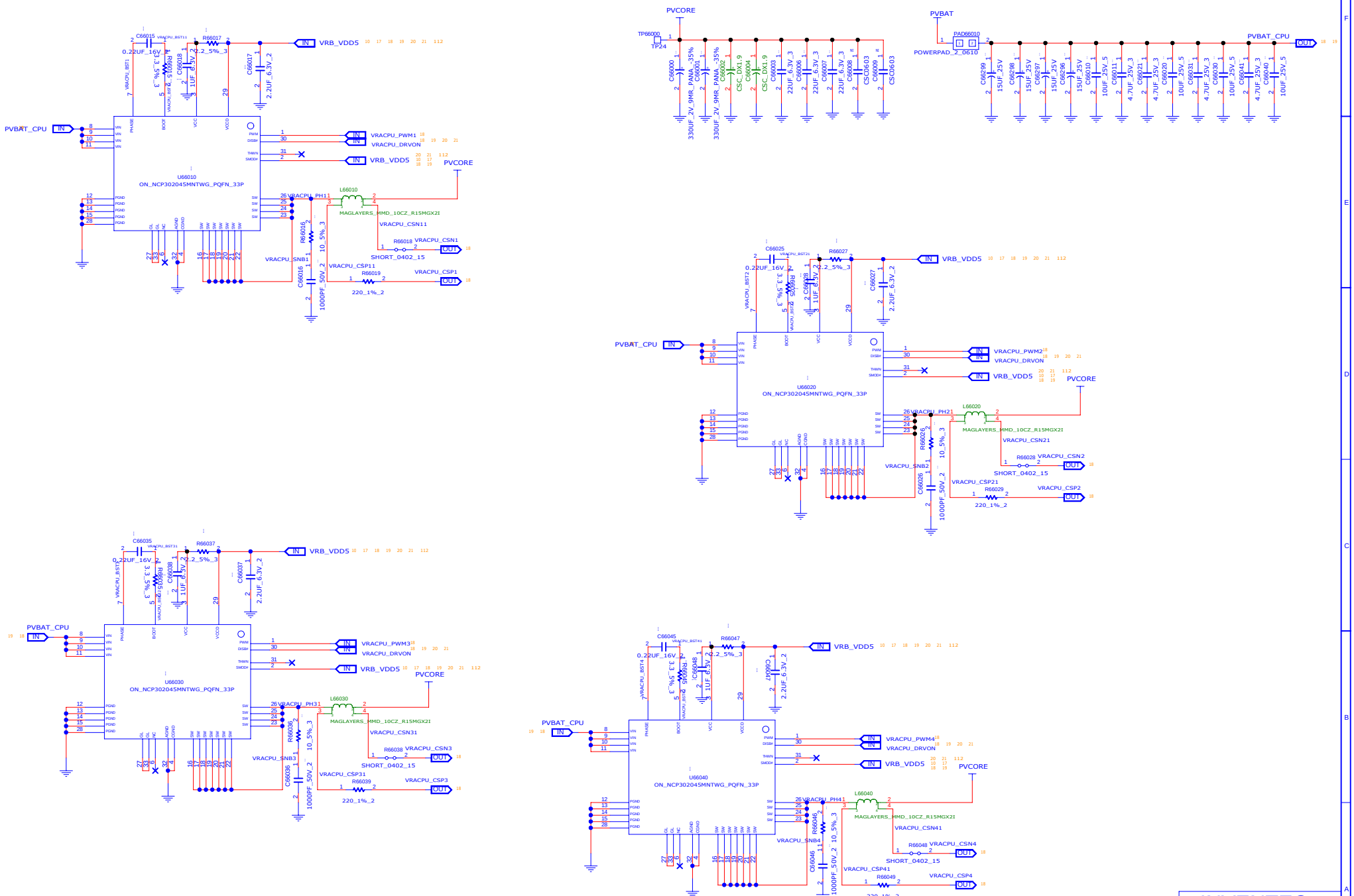

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCORE

SIZE	CODE	DOC NUMBER	REV
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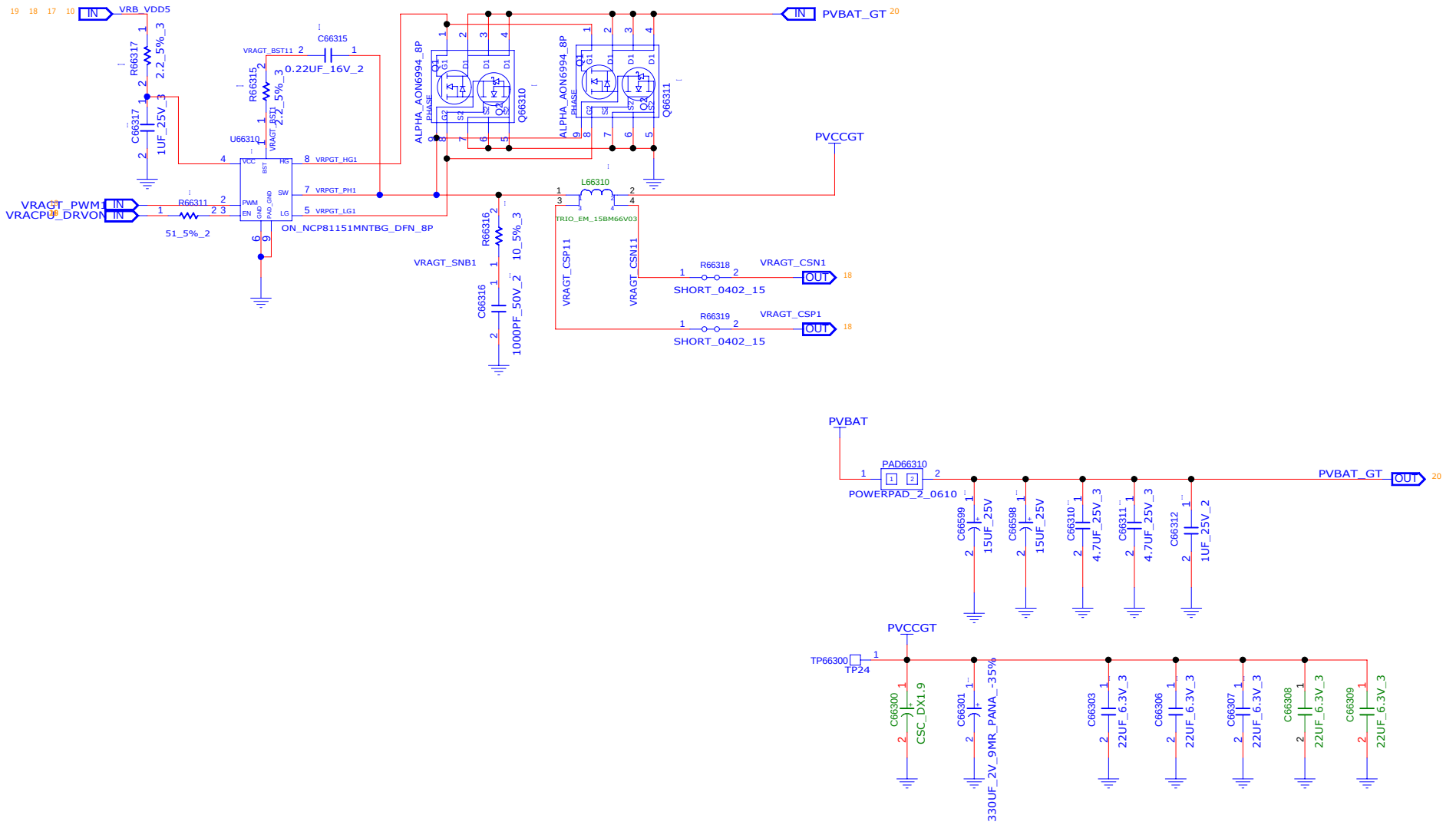

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PVCCGT		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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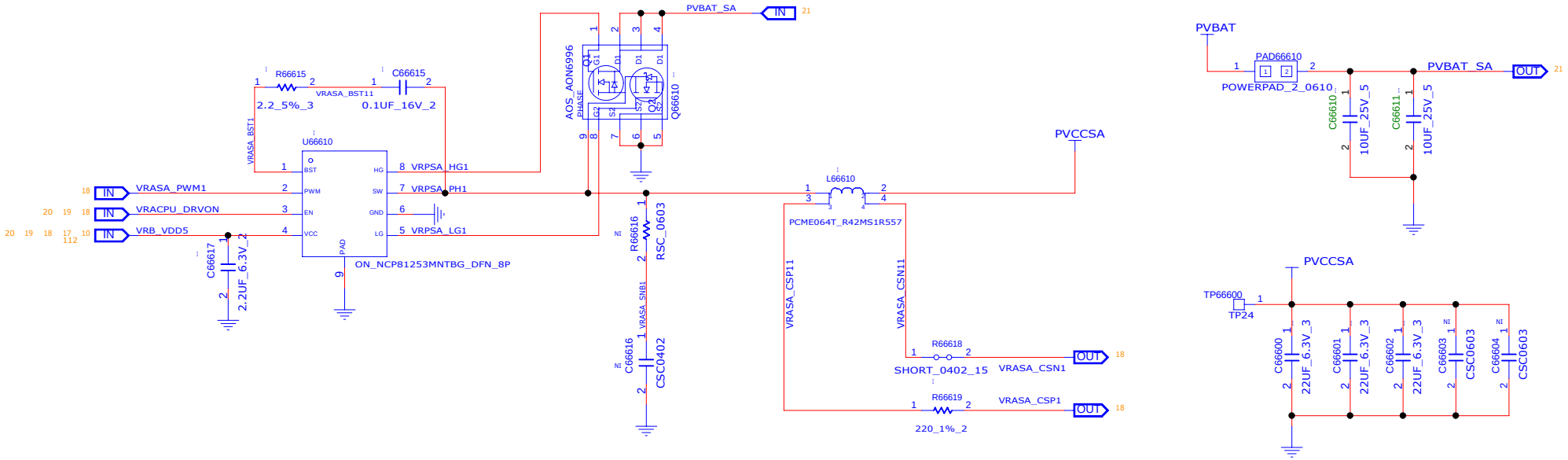

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCSA

SIZE	CODE	DOC.NUMBER	REV
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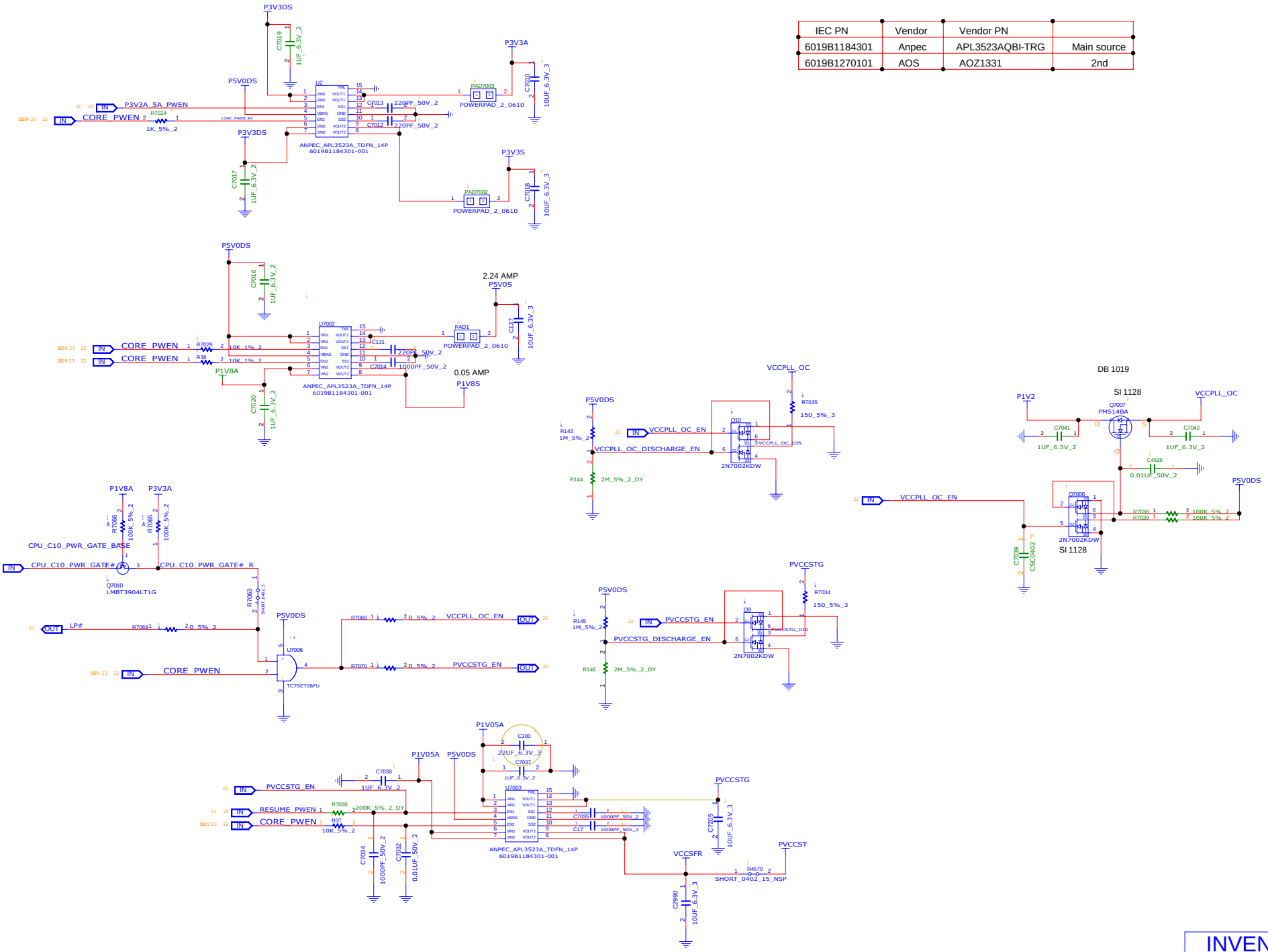
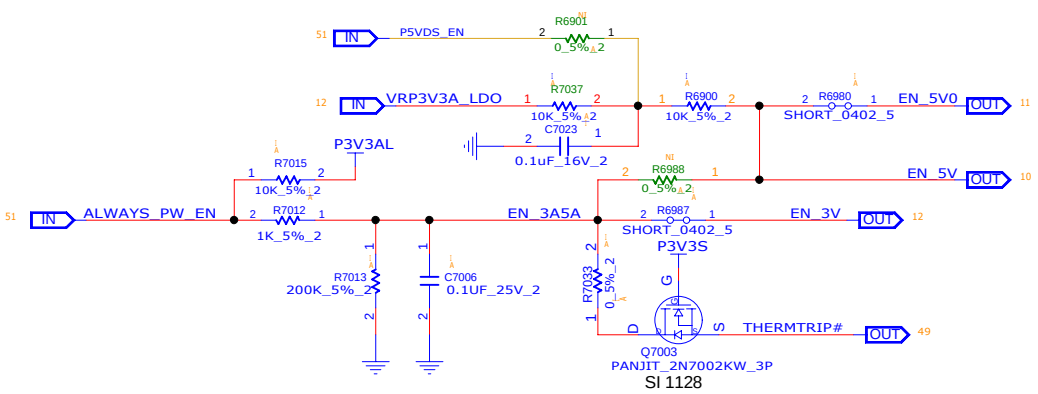
IEC PN	Vendor	Vendor PN	
6019B1184301	Anpec	APL3523AQBI-TRG	Main source
6019B1270101	AOS	AOZ1331	2nd

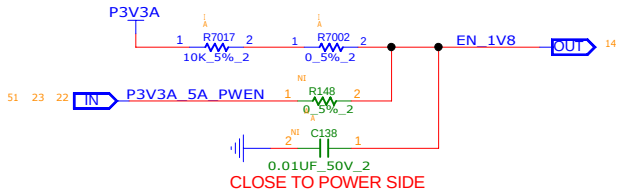


1. P3V3DS / P5V0DS



SI 1128

2. P1V0A / P1V8A / P3V3A



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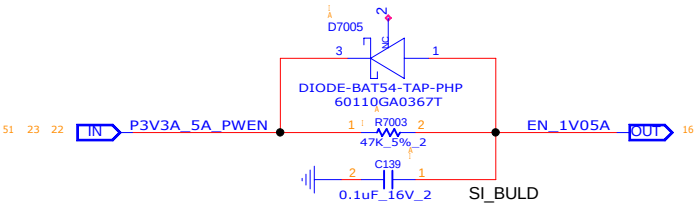

SI_BULD

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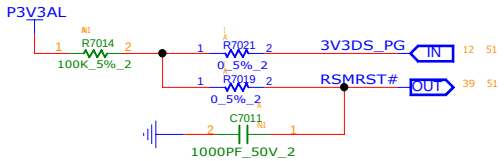
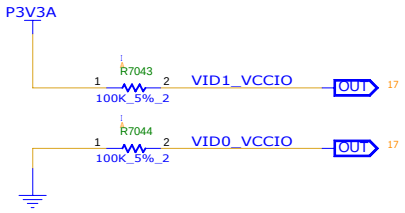
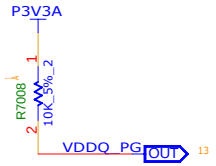
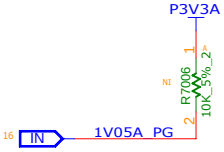
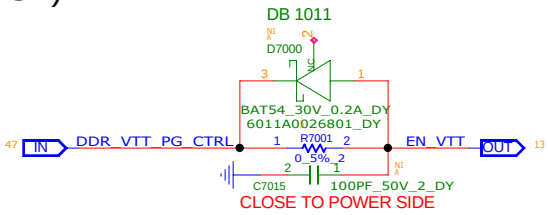




3. P1V2 / P1V8 / VCCSFR(PVCCST)







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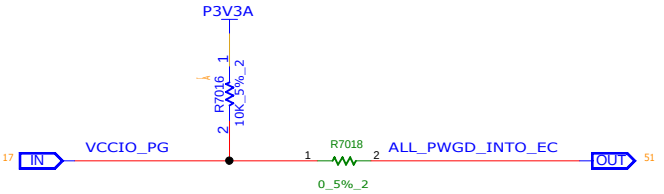

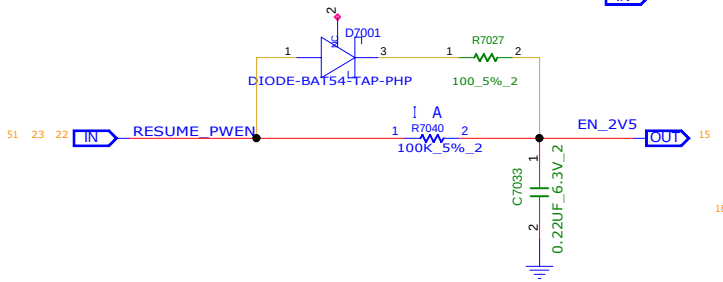

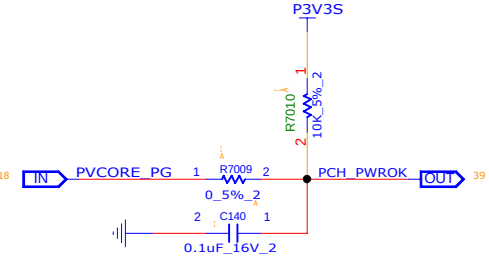

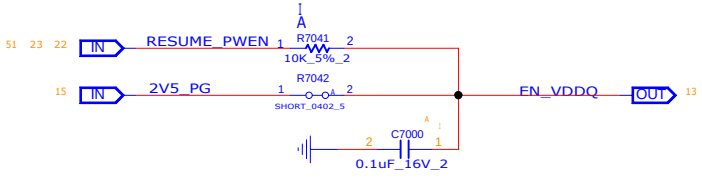

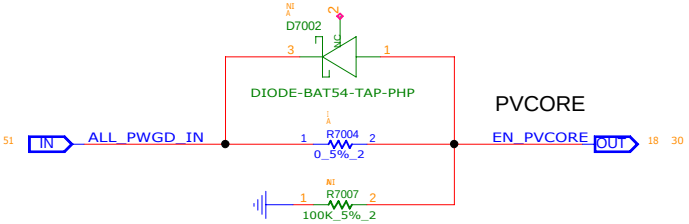

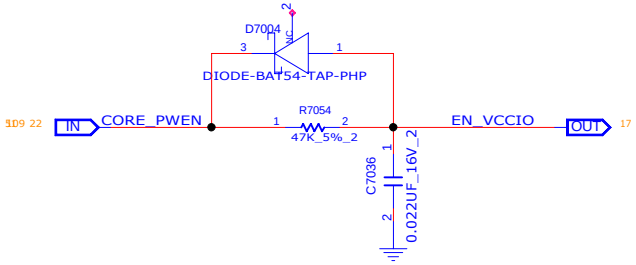

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV X01

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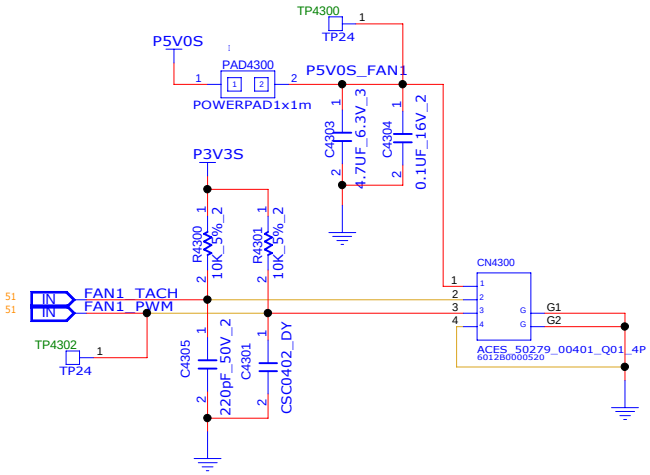
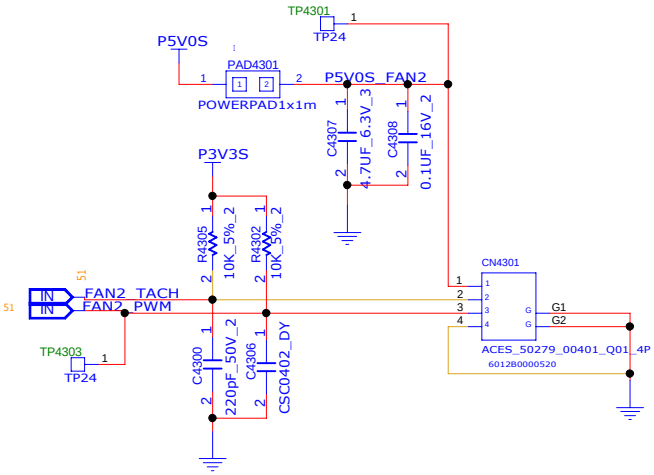
REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION FAN & THERMAL		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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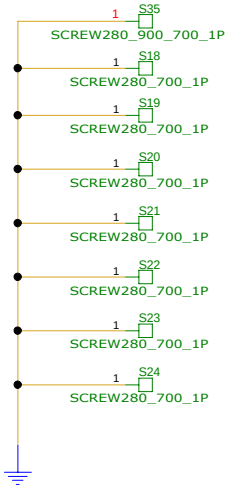
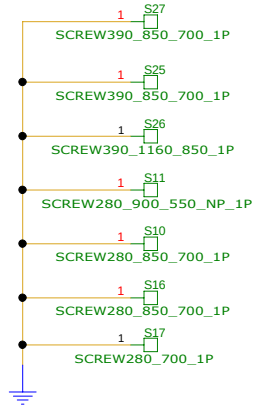
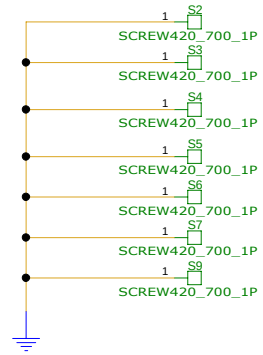
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

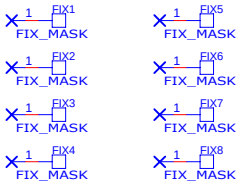
REFERENCE 0~49(PCB SCREW)





PCB





INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
XDP & ME CONN.

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 25 of 130

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

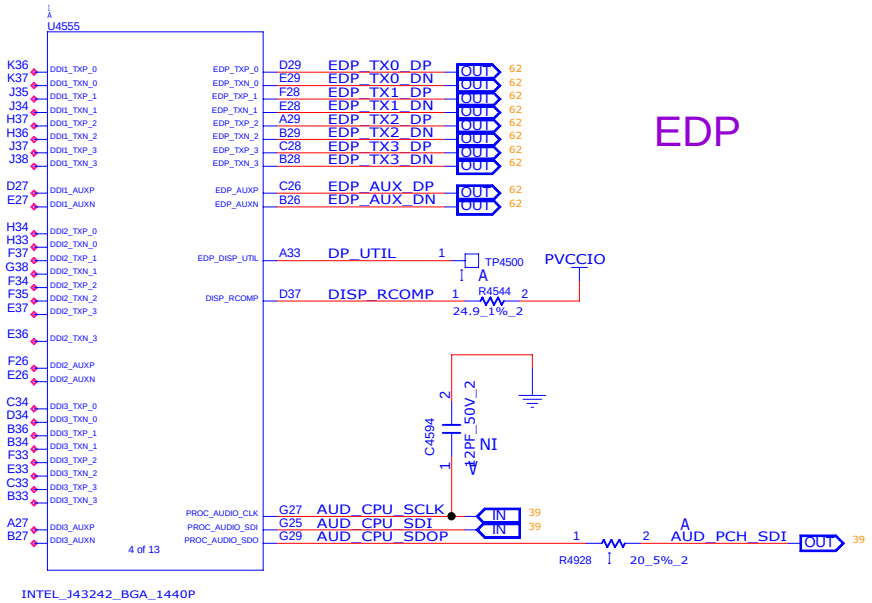
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE1_H-PEG,HDMI

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 26 of 130



EDP

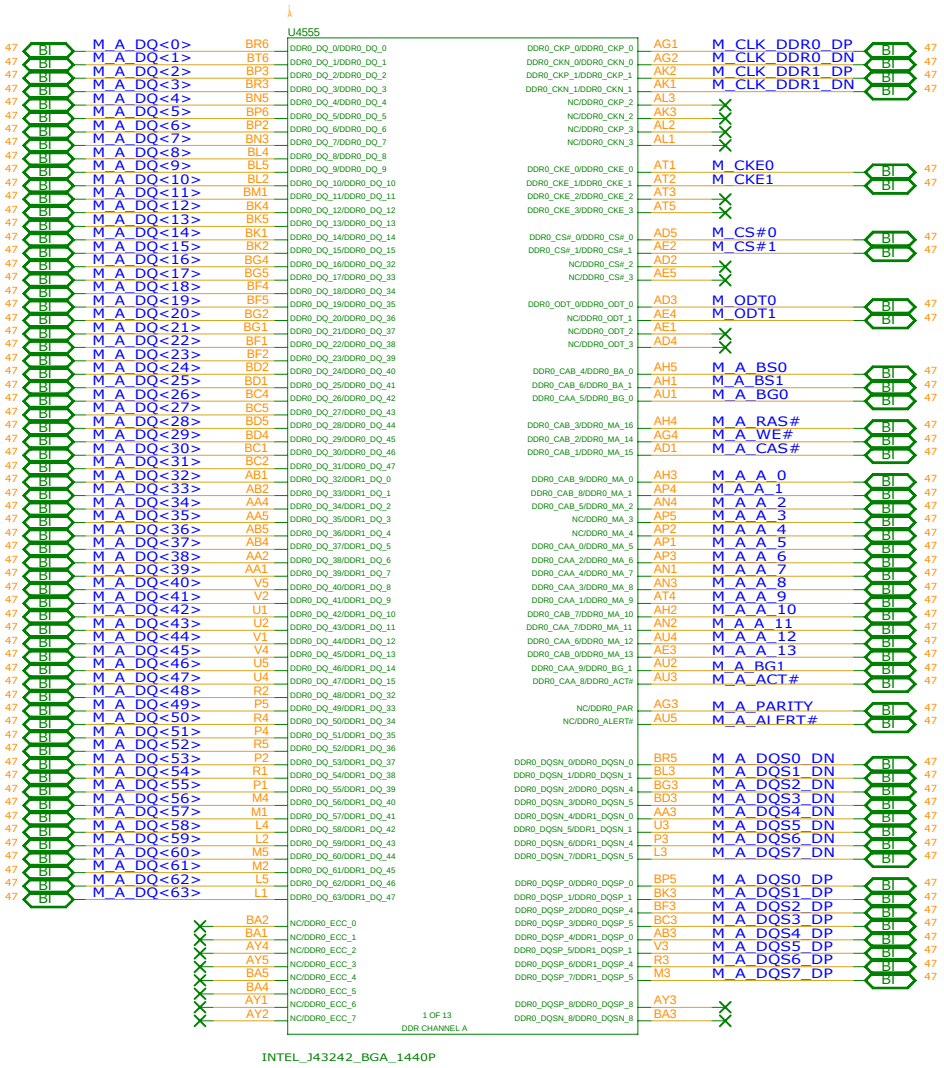
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE2_H-DDI,EDP

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 27 of 130



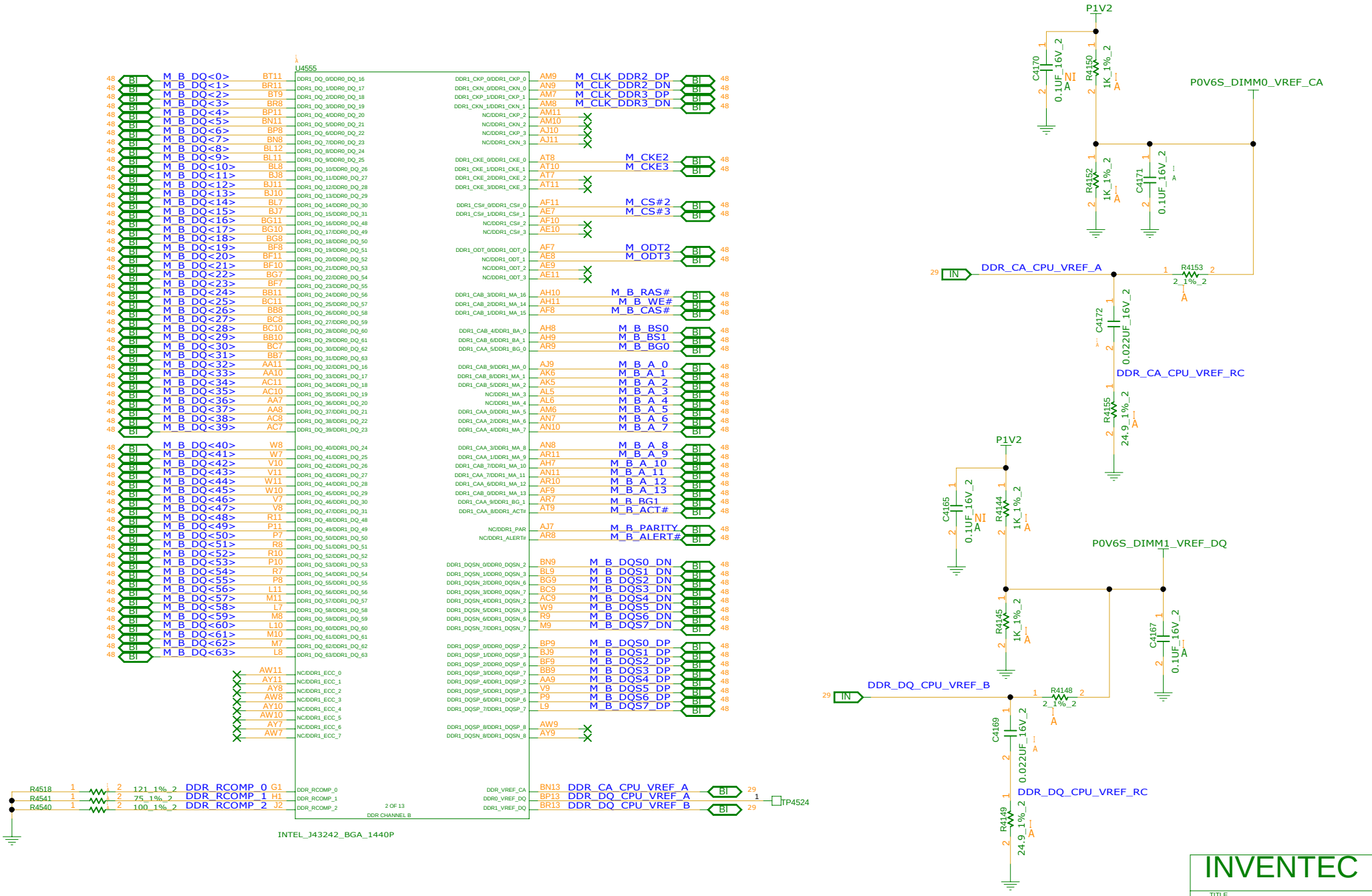
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE_H-DDR-1

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 28 of 130



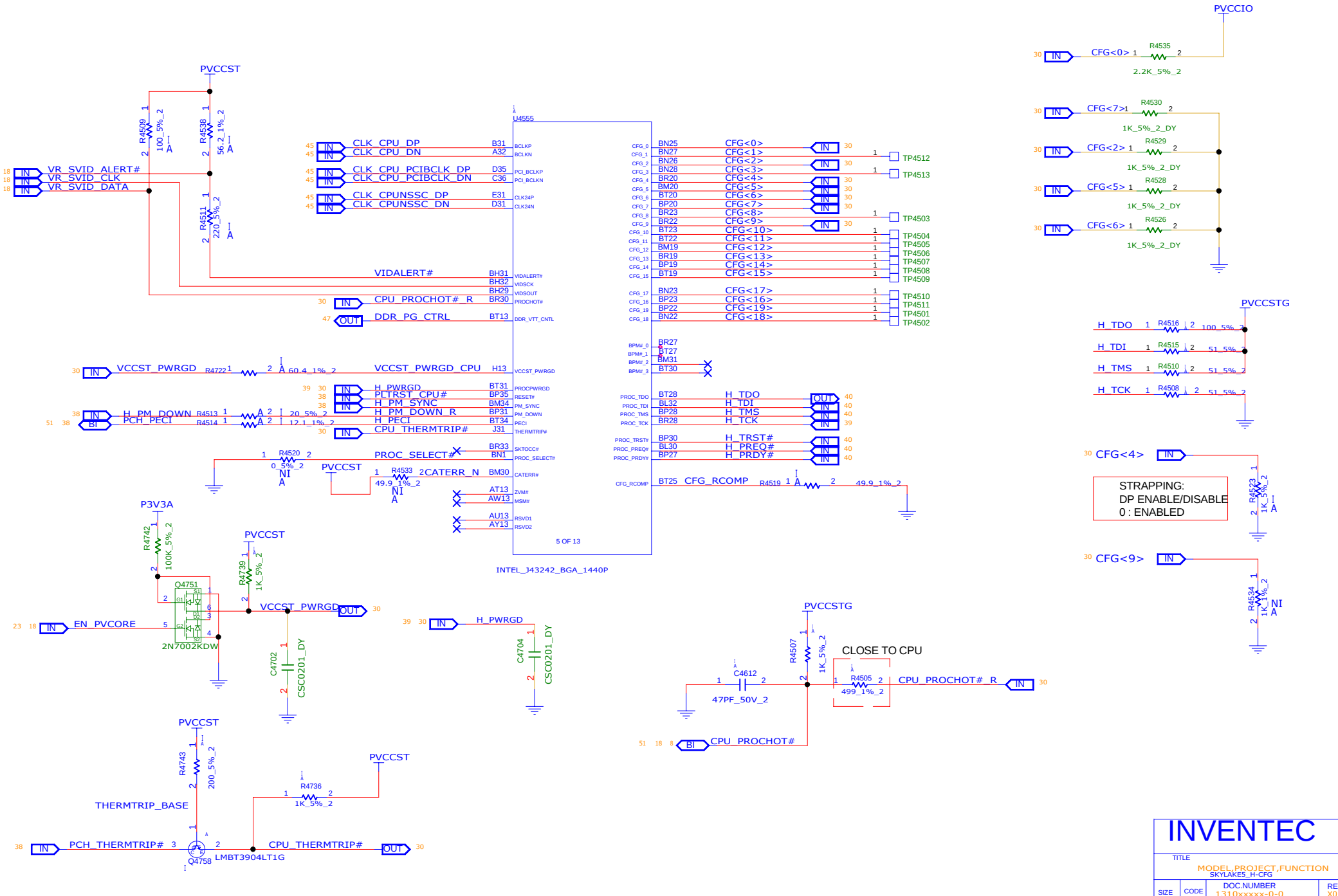
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE4_H-DDR-2

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 29 of 130



EDS VER0.7

PVCORE
47UF X 5 22UF X 12
10UF X 21 1UF X 24

PLACE IN BACK SIDE

PLACE IN BOTTOM SIDE

INTEL_J43242_BGA_1440P

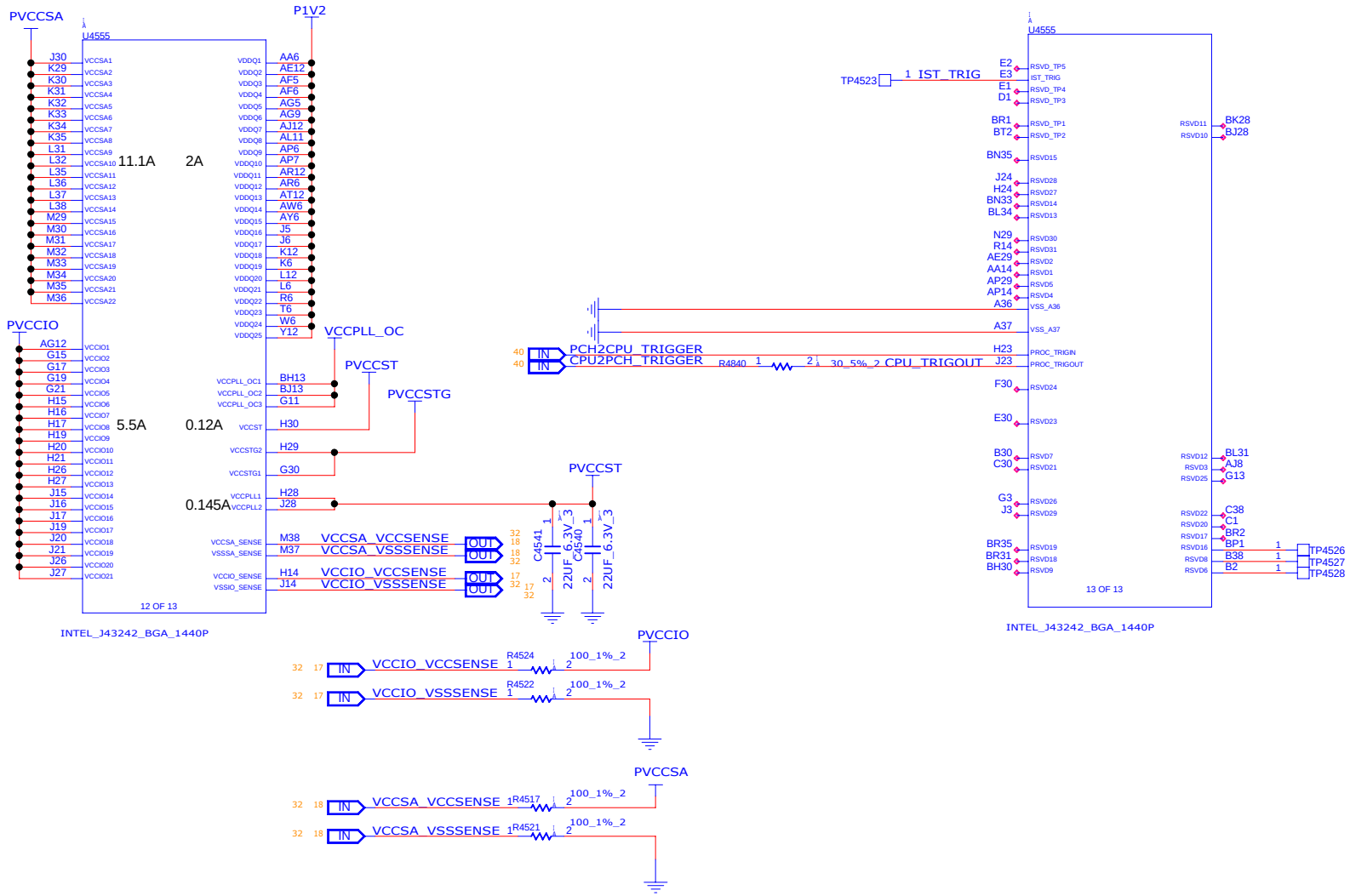
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE6_H-POWER

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SHEET 31 of 130



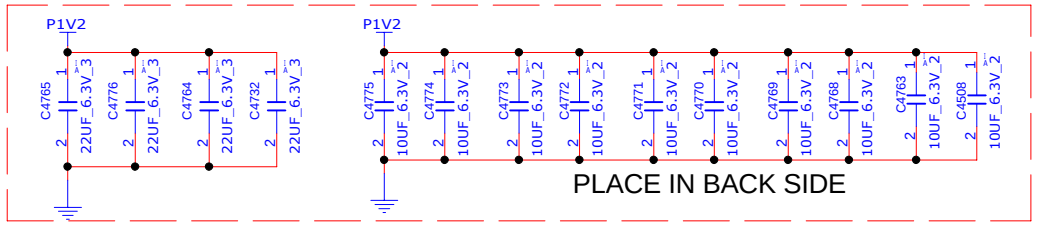
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

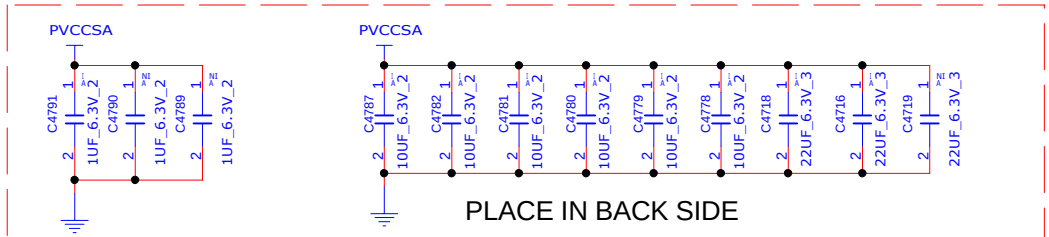
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE7_H-POWER

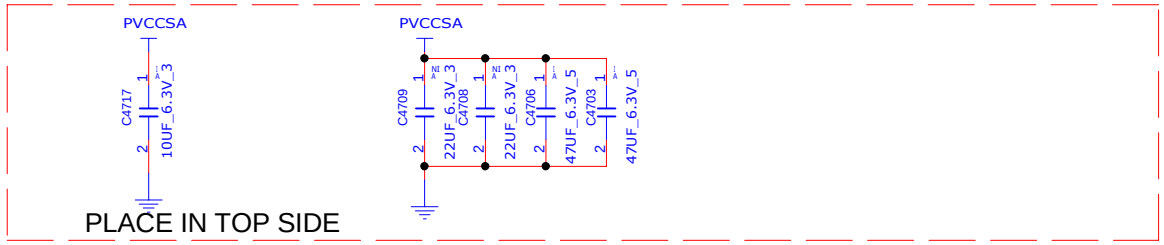
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

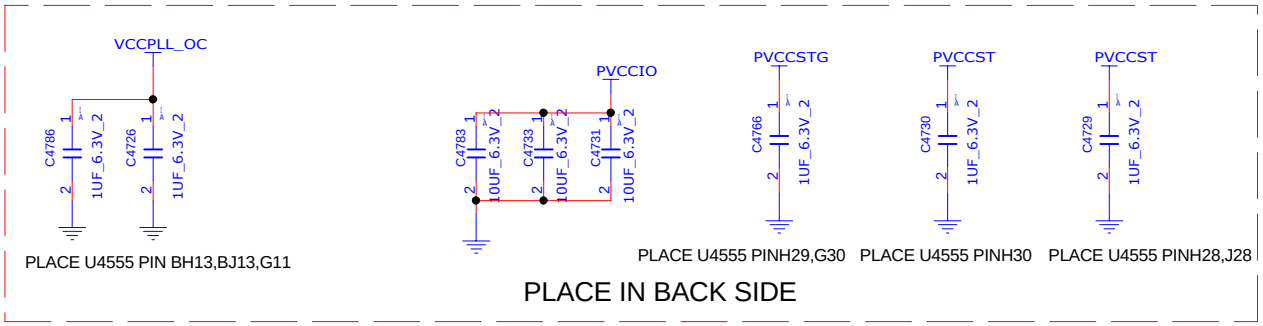
SHEET 32 of 130





EDS VER0.7	
P1V2	
10UF X 11	22UF X 4
PVCCSA	
47UF X 2	22UF X 2
10UF X 7	1UF X 1





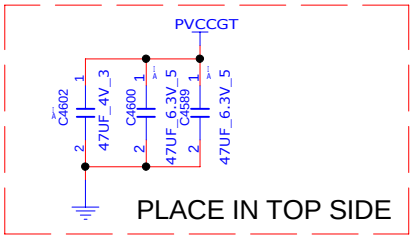
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION SKYLAKE8_H-DECOUPLING			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 33 of 130			

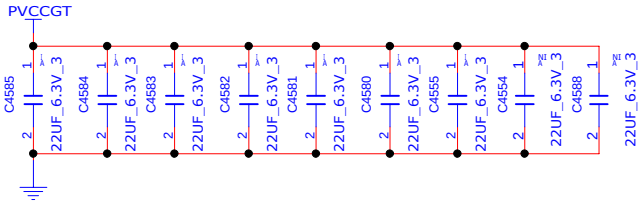
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

EDS VER0.7

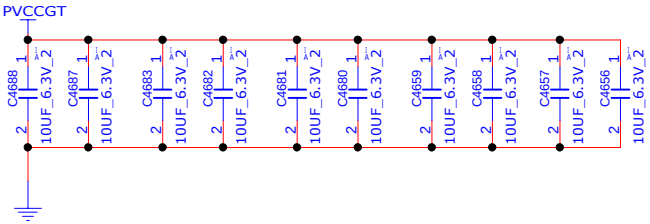
PVCCGT
47UF X 3 22UF X 7
10UF X 10 1UF X 12

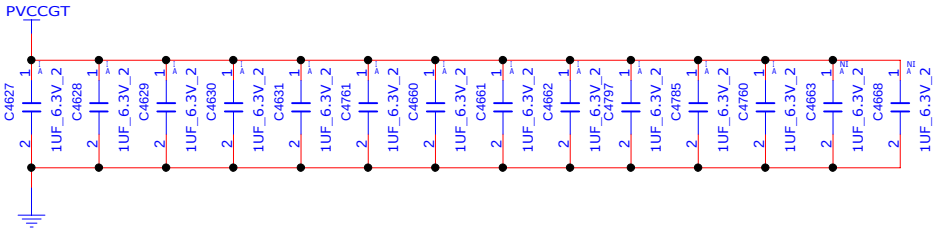


PLACE IN TOP SIDE

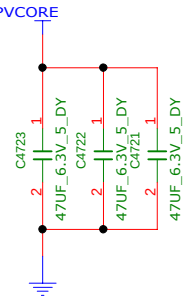


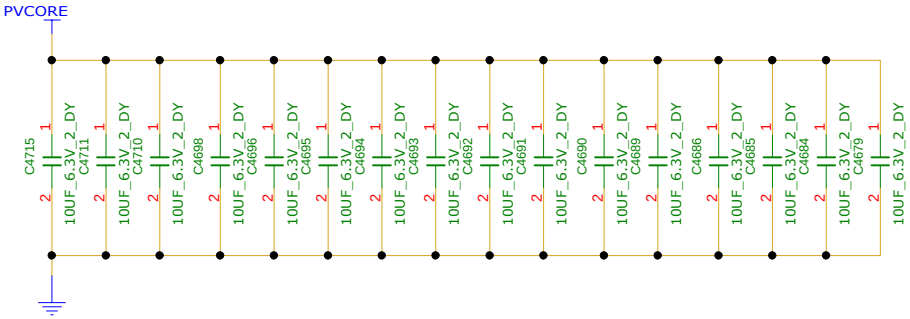
PLACE IN BACK SIDE

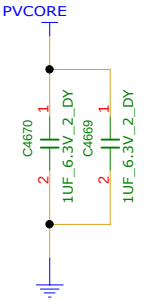




H82 CPU

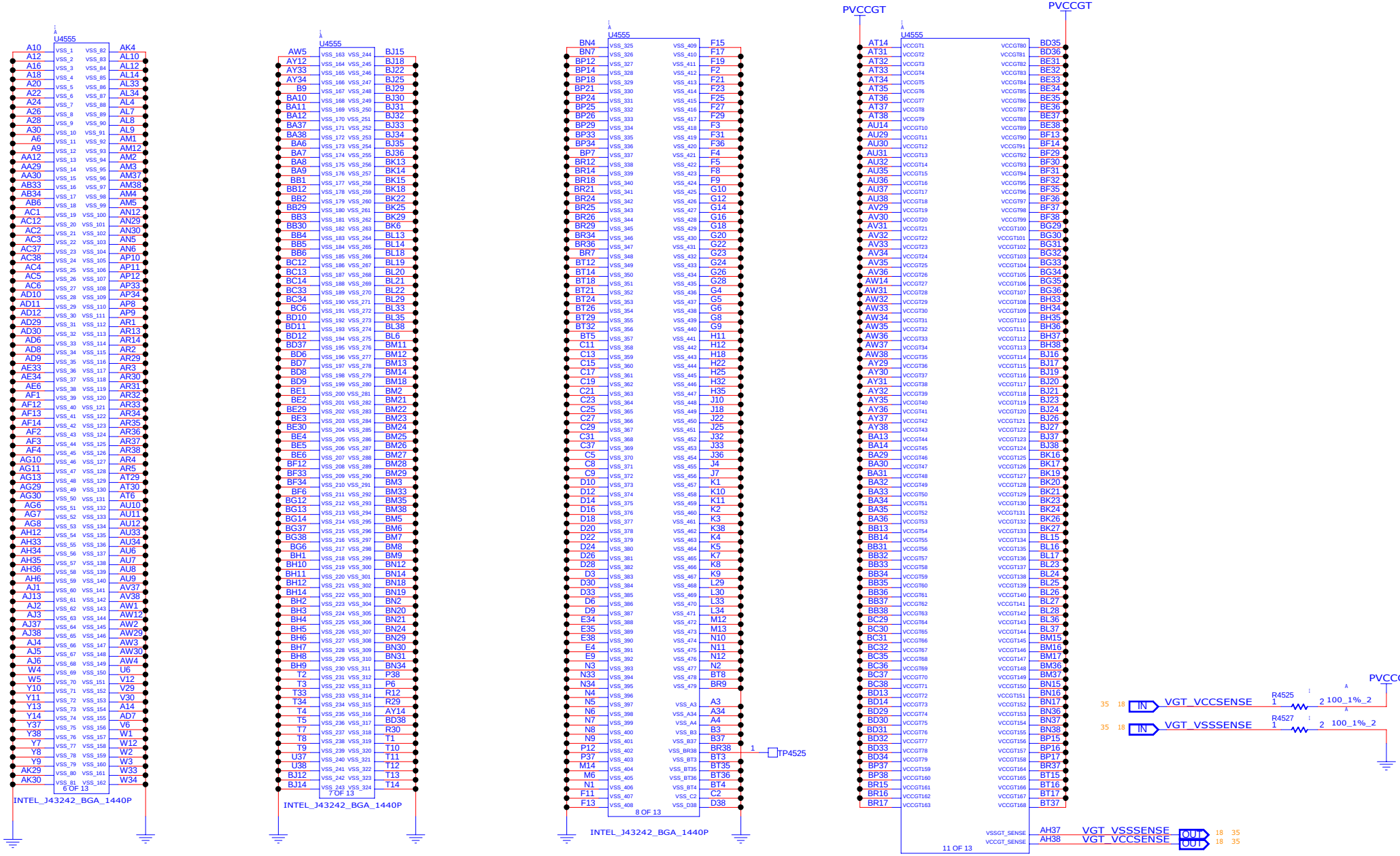






INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SKYLAKE9_H-GT *DECOUPLING		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	
SHEET 34 of 130			



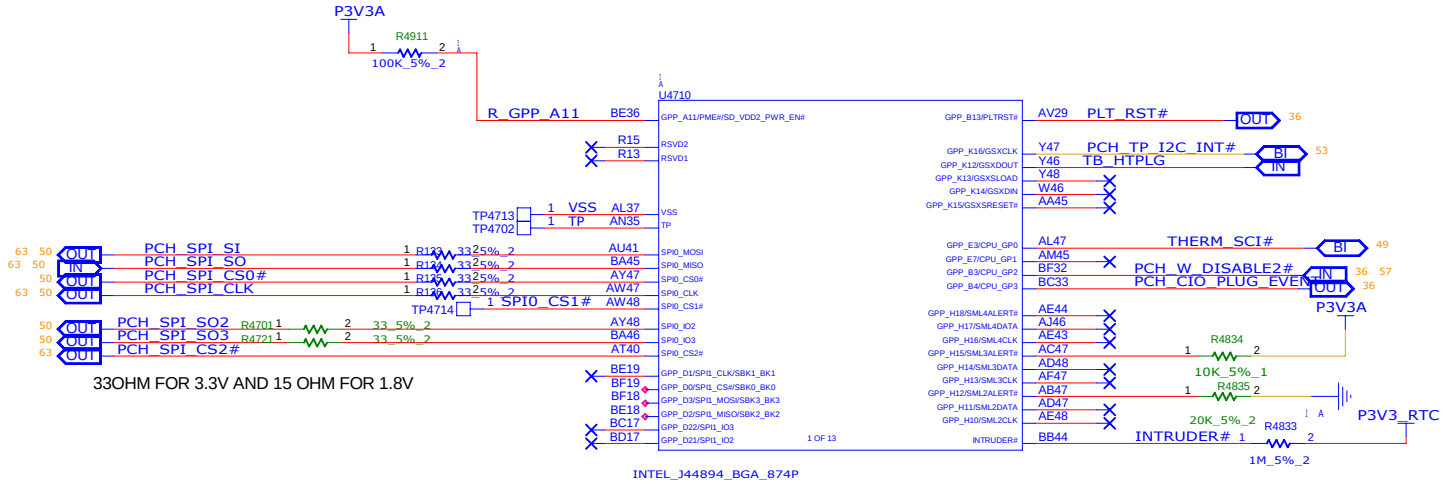
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

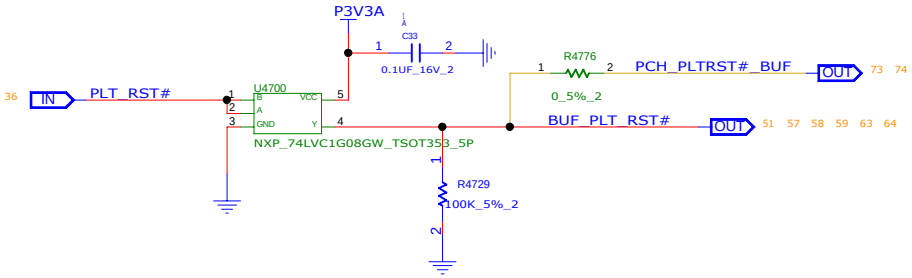
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE10_H-GND

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 35 of 130





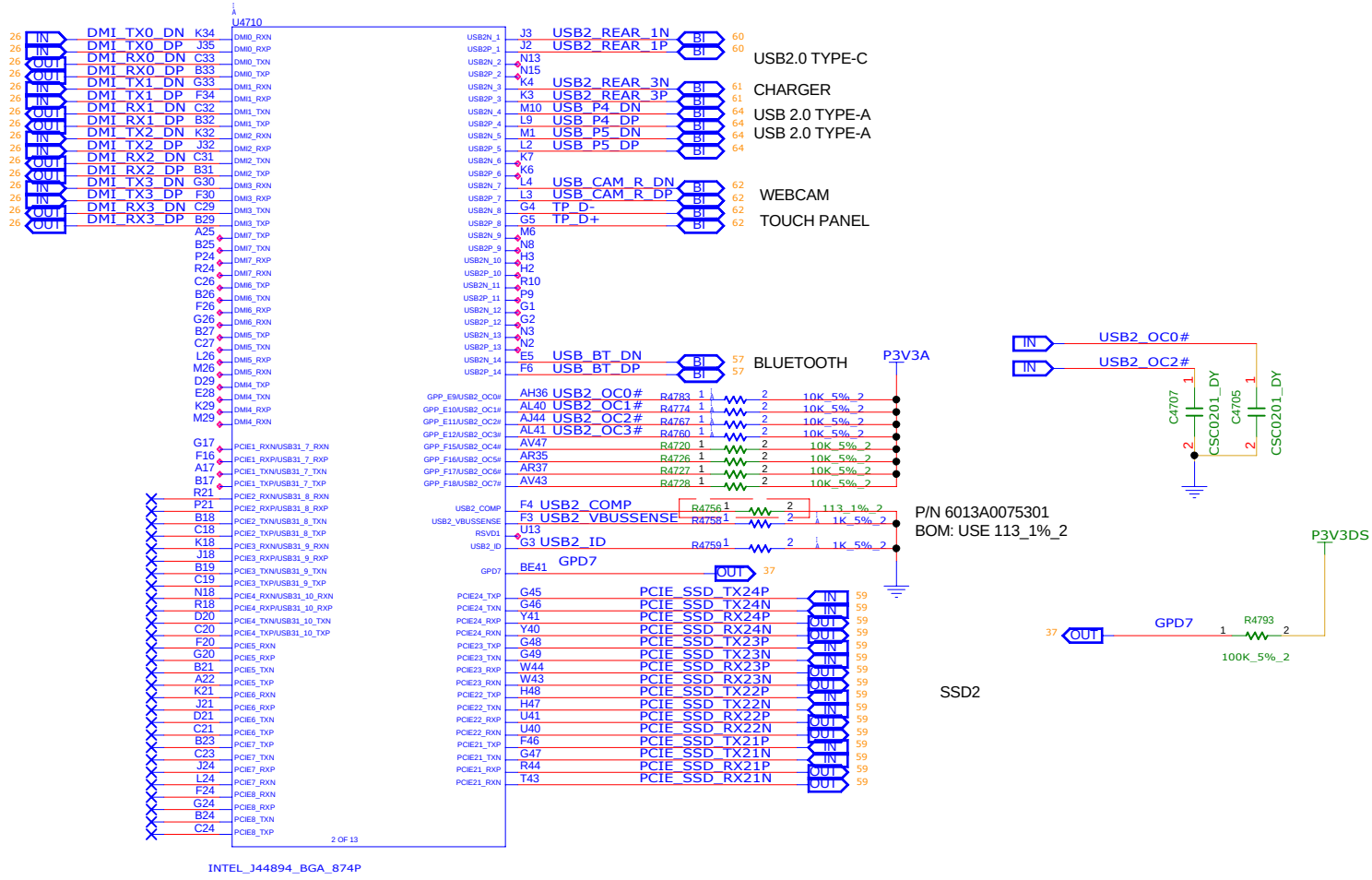
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-SPI,GPP

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

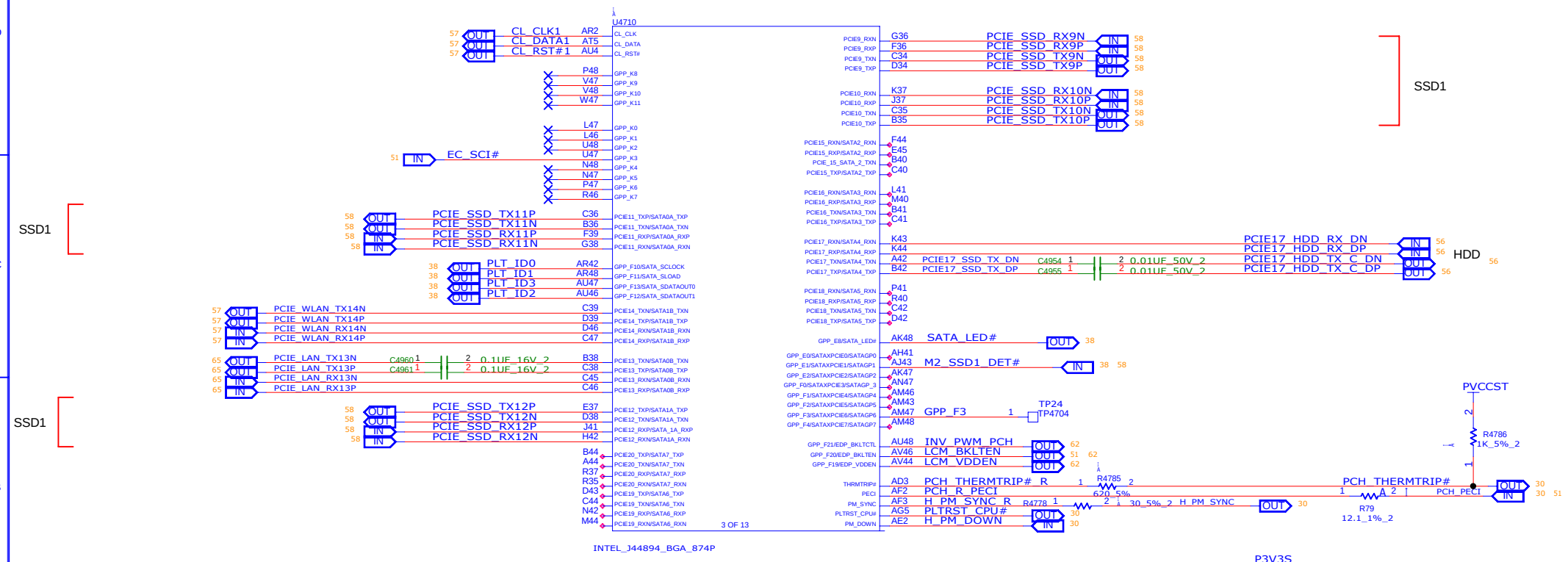
SHEET 36 of 130



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PCH-DMI,USB2,USB3		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 37 of 130			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



	PLT_ID0	PLT_ID1	GPU
GPU	0	0	N18E-G2
	0	1	N18E-G1
	1	0	N18E-G0

	PLT_ID2	PLT_ID3	Size
VRAM	0	0	8G
	0	1	6G

	GPP_F14	Panel
GPU	0	15"
	1	17"

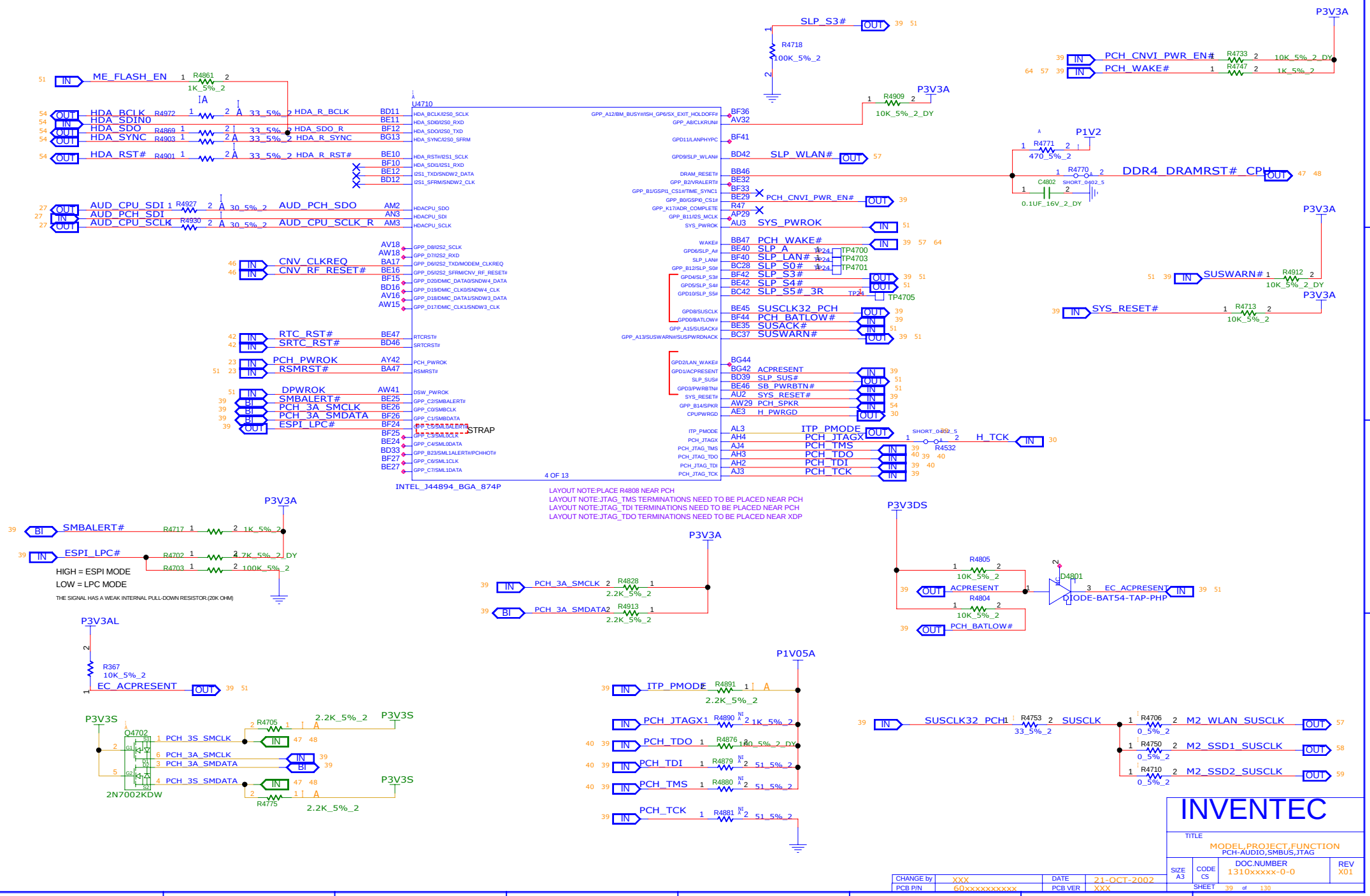
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-CLINK,FAN,PCIE/SATA,HOST

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 38 of 130

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PCH-AUDIO,SMBUS,JTAG		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 39 of 130			

TYPE_C

TYPE_A_L2

CHARGER

TYPE_A_L1

U4710

INTEL_J44894_BGA_874P

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P3V3A

WHEN USED AS DEVSLP, NO EXTERNAL PULL-UP OR PULLDOWN TERMINATION REQUIRED FROM SATA HOST DEVSLP

INVENTEC

TITLE

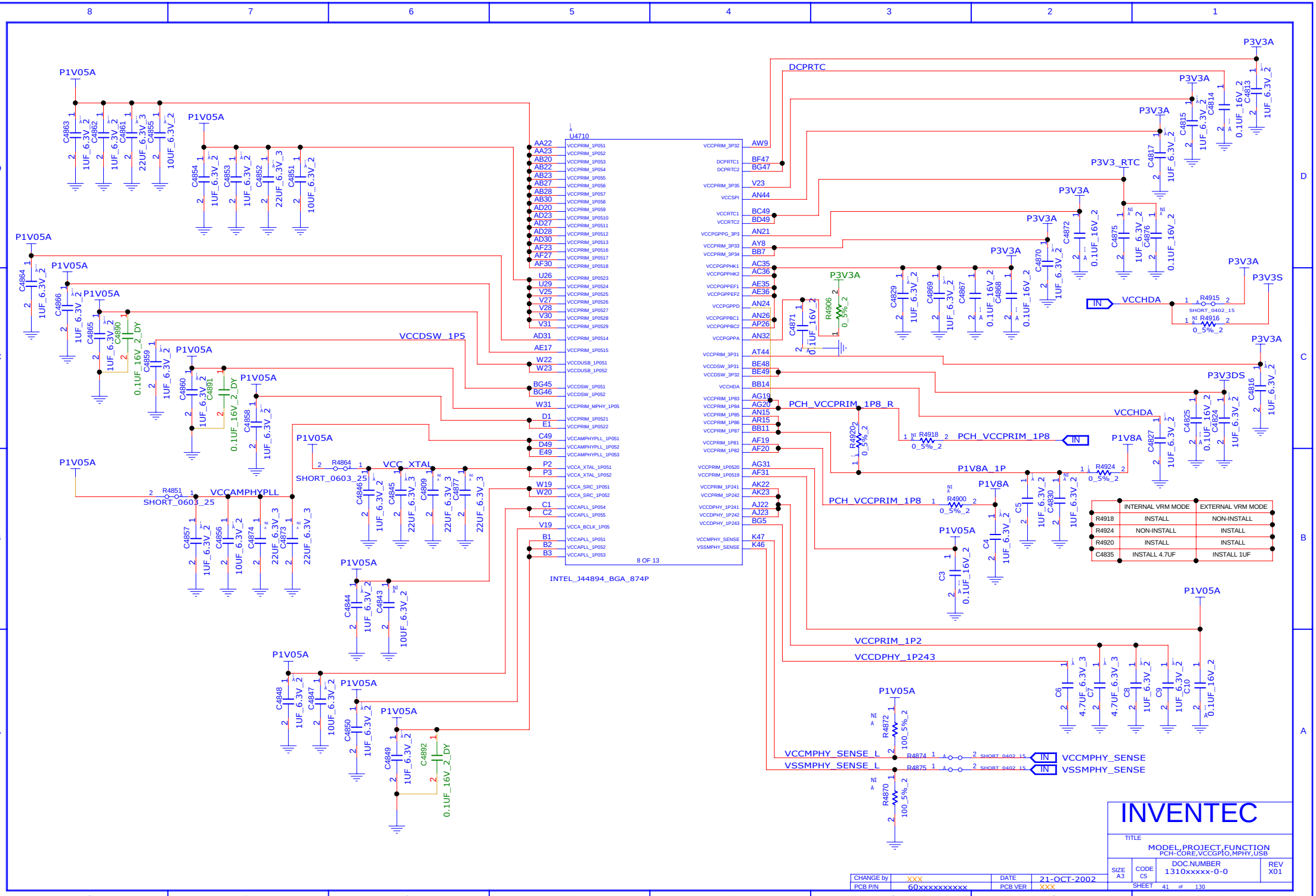
MODEL,PROJECT,FUNCTION

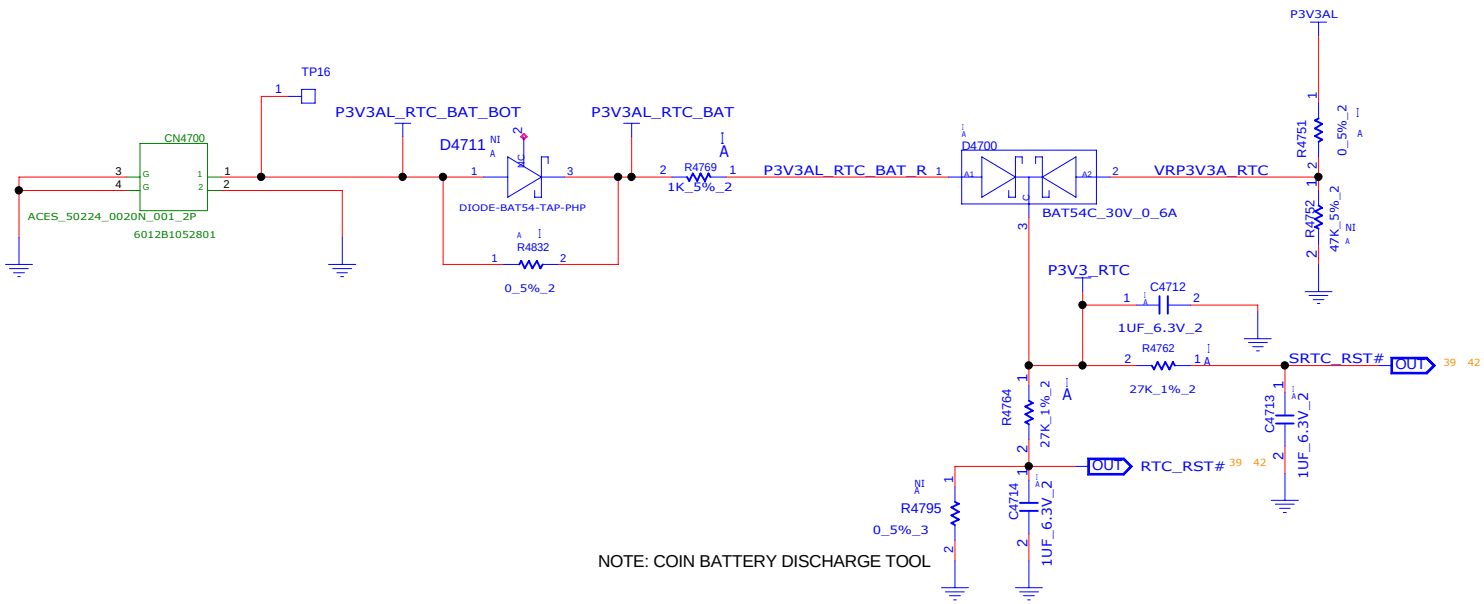
PCH-LPC/ESPI,USB,SATA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 40 of 130

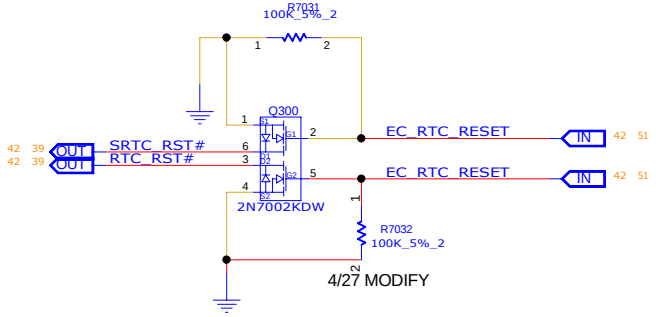
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX





NOTE: COIN BATTERY DISCHARGE TOOL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R4710	INSTAL	UNINSTAL
R4709	UNINSTAL	INSTAL



4/27 MODIFY

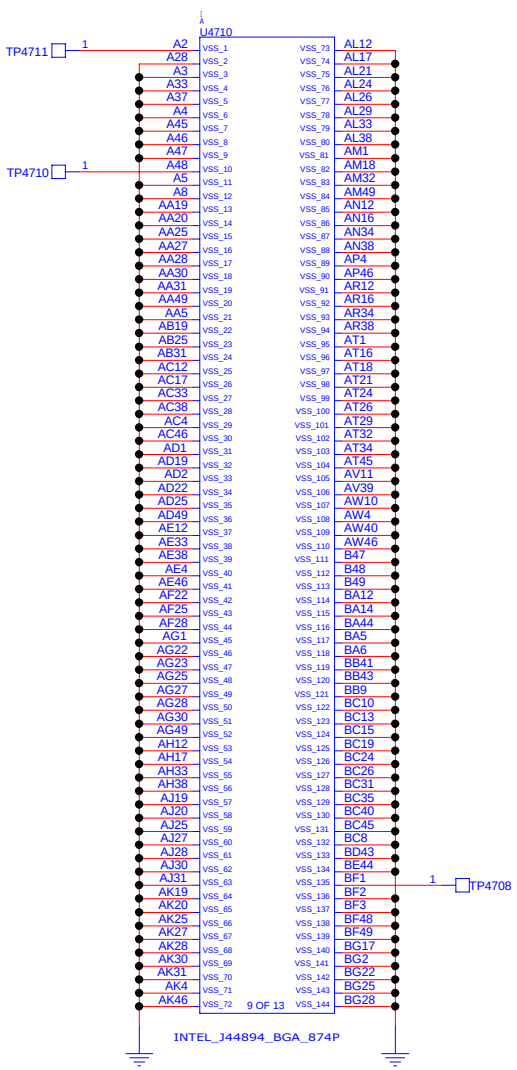
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

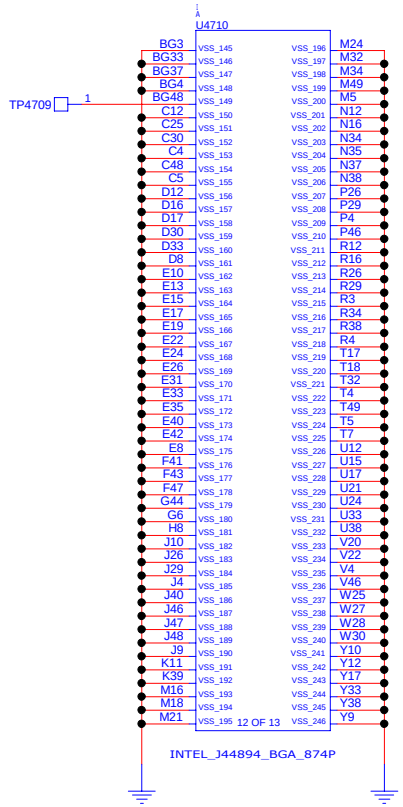
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 42 of 130





INVENTEC

TITLE	MODEL,PROJECT,FUNCTION		
	PCH-GND		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 43 of 130			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

STARPPING

DDPB_CTRLDATA:PORT B DETECT 0:DISABLE
DDPC_CTRLDATA:PORT C DETECT 1:ENABLE

PORTB/PORTC:TBT
PORTD:HDMI

U4710

INTEL_J44894_BGA_874P

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11 OF 13

Q4 L2N7002WT1G

P3V3S P3V3A P1V8A

DP_P1_HPD DP_P2_HPD EDP_HPD PCH_DGPU_PWR_EN# DGPU_PWR_EN

HDMI_HPDET TPM_PIRQ# TP4807 TP24

DPB_DDCCLK DPB_DDCDATA DPC_DDCCLK DPC_DDCDATA HDMI_DDCCLK HDMI_DDCDATA

GPP_F14 FGC6_FB_EN EVENT_PCH# GC6_FB_EN_PCH1

GC6_FB_EN_PCH GPU_EVENT_PCH#

EVENT_PCH# PCH_DGPU_PWR_EN#

GPP_B22 PCH_DGPU_PWR_EN# PCH_HOLD_RST# DGPU_PWROK

ALERT_PCH# PCH_HOLD_RST#

UART0_TXD UART0_RXD

RUNSCI# TOUCH_INT# TOUCH_PWR_EN

PCH_I2C1_CLK PCH_I2C1_DATA PCH_I2C_CLK PCH_I2C_DATA

HPGP_W_DISABLE# GPP_H20 GPP_H19

BRD_ID3 BRD_ID2 BRD_ID1 BRD_ID0 DP_MA_HPD# HDMI_MB_HPD# TOUCH_RST#

IRMT_HOLD_RST# PCH_HOLD_RST#

INTEL_J44894_BGA_874P

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-GPP

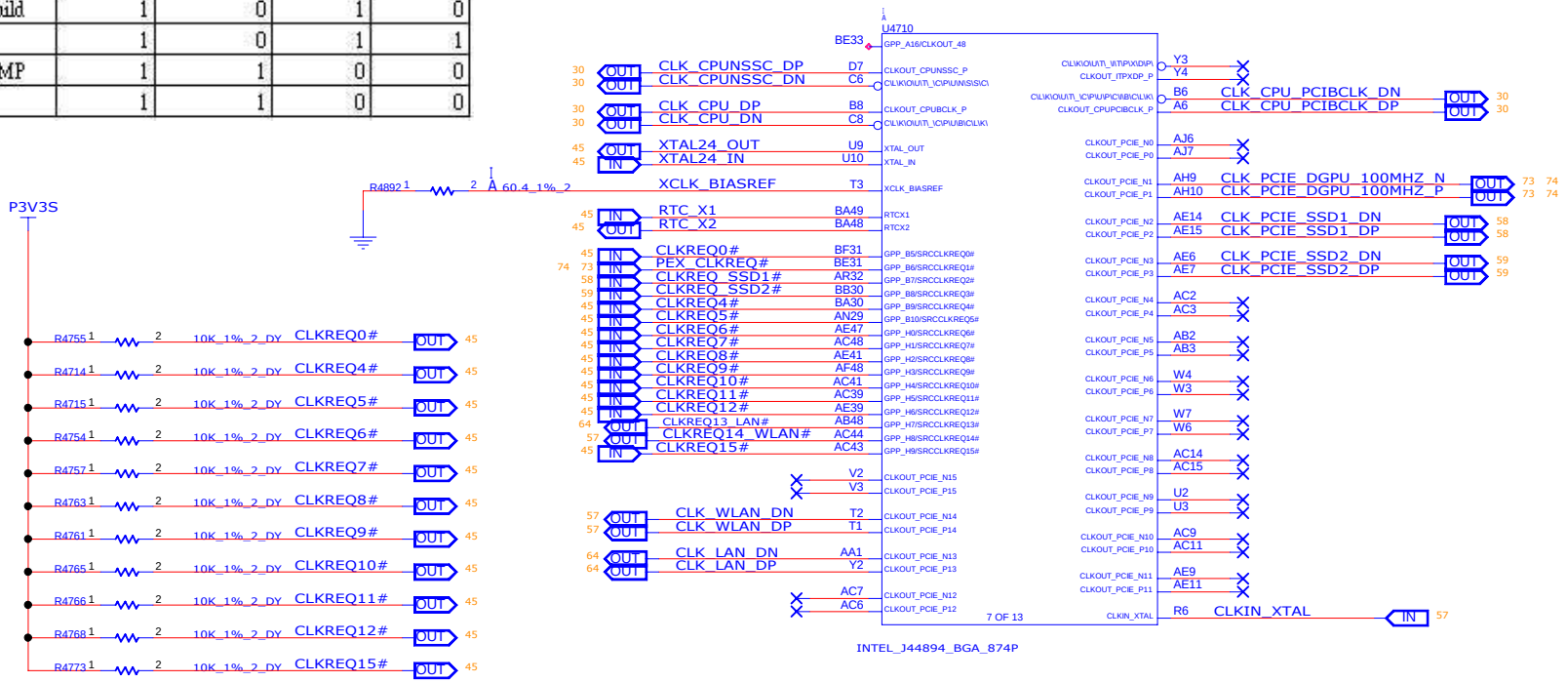
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

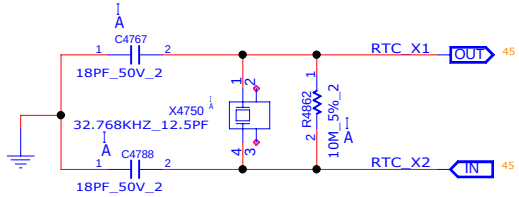
SHEET 44 of 130

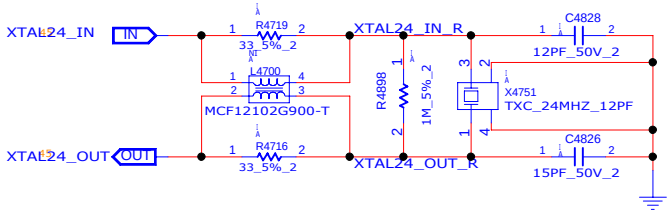
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	0	1
D build	1	0	1	0
	1	0	1	1
Pre-MP	1	1	0	0
MP	1	1	0	0

1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs







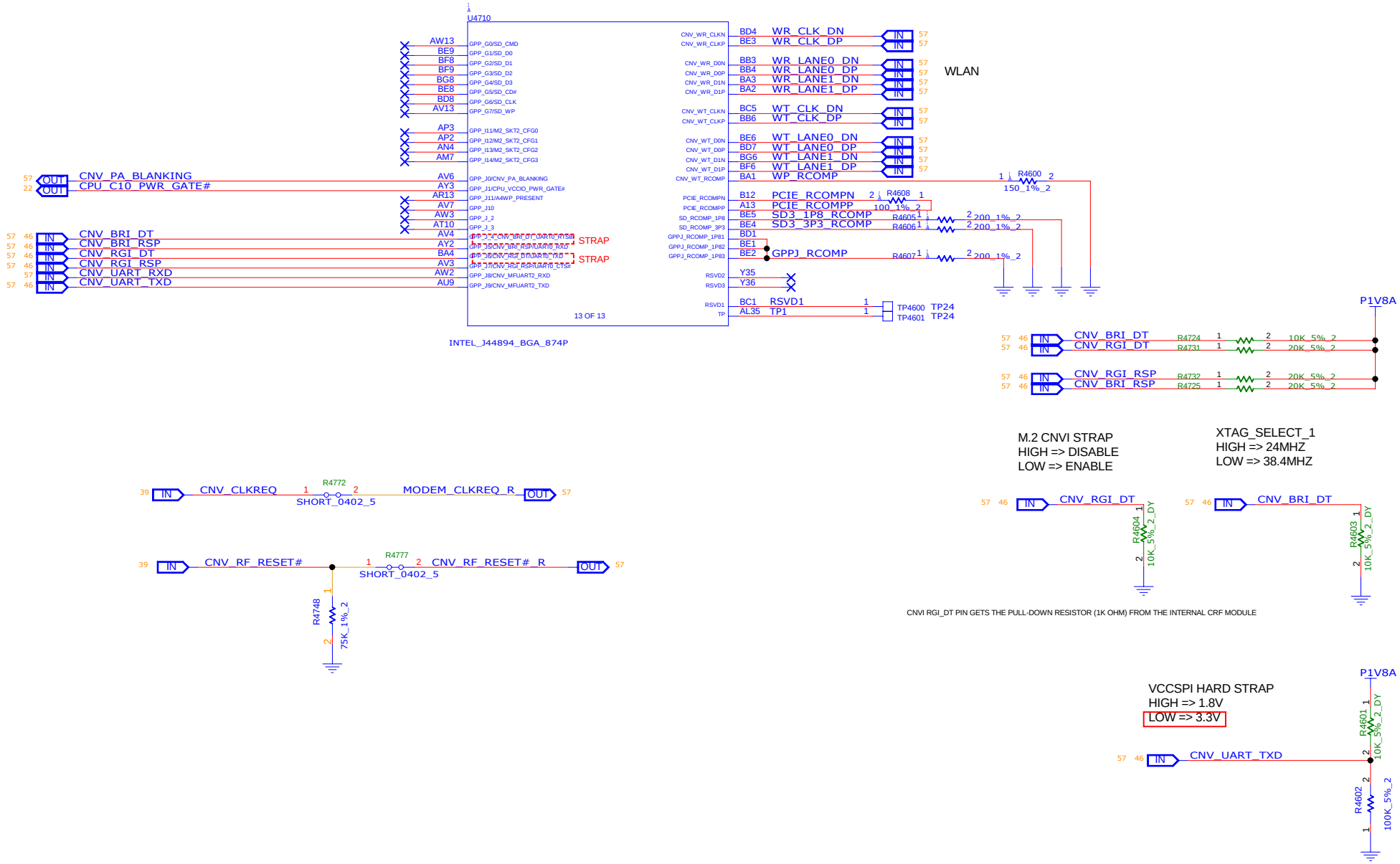
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-GPP,CLKOUT

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

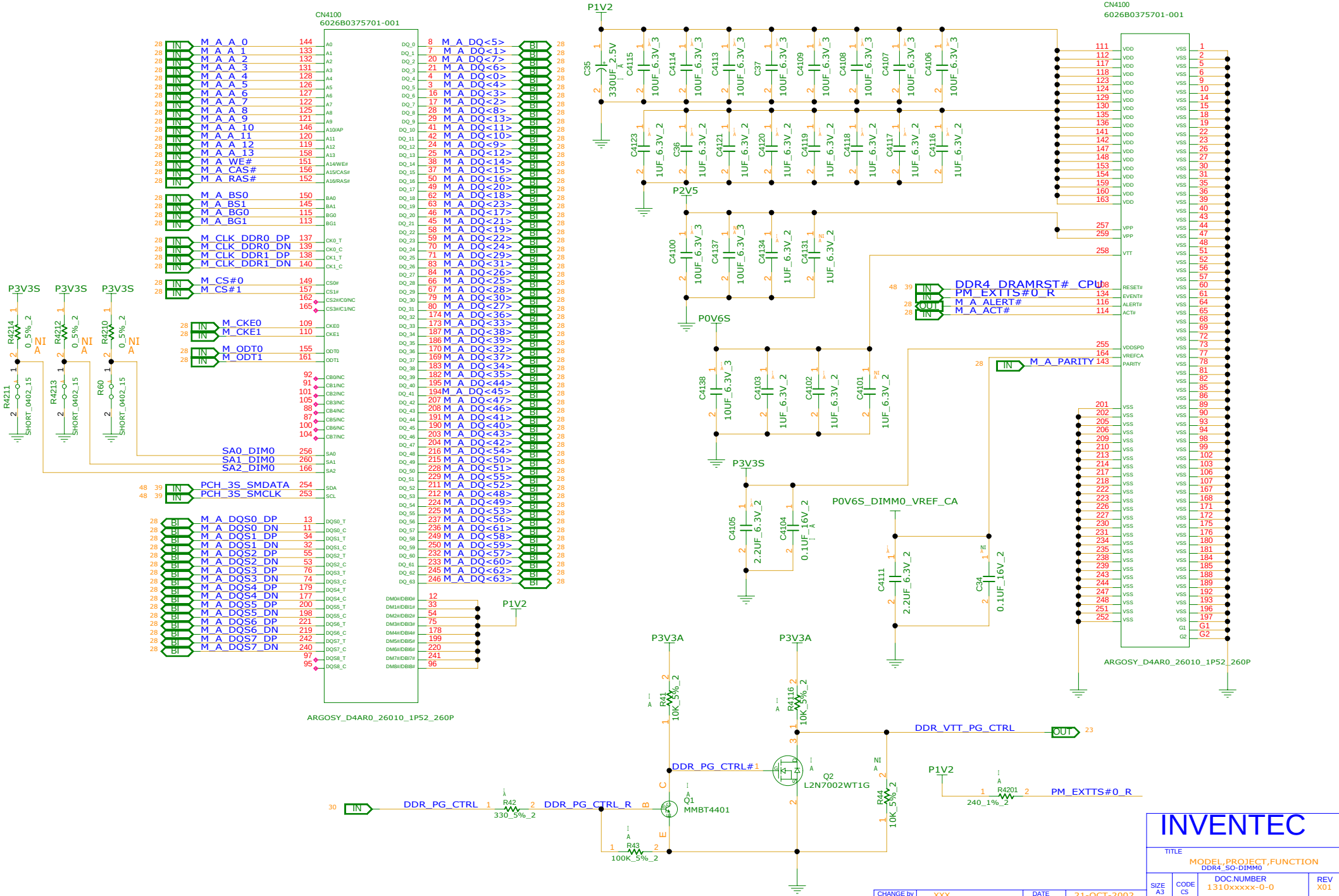
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

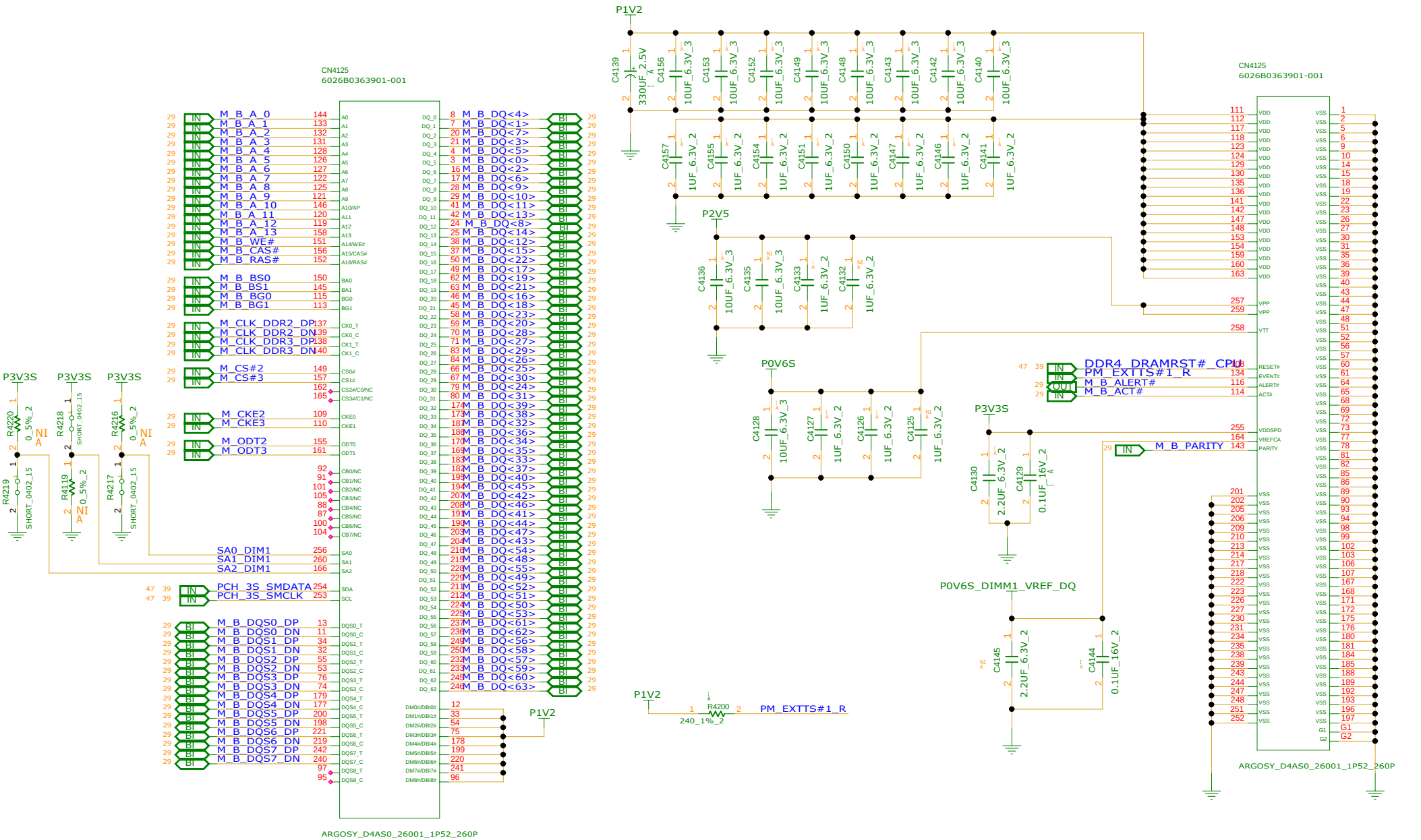
SHEET 45 of 130



INVENTEC

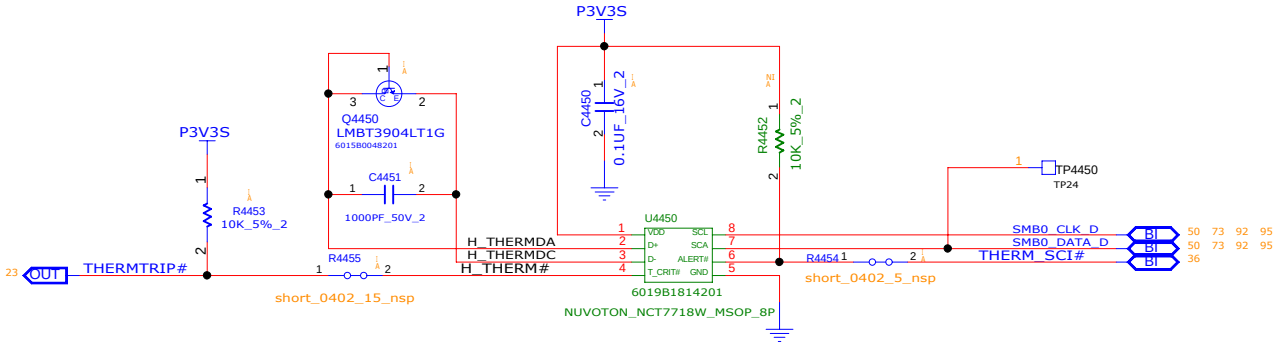
TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 46 of 130	
PCB P/N 60xxxxxxxxxx	PCB VER XXX		





REFERENCE NUMBER:4450~4499

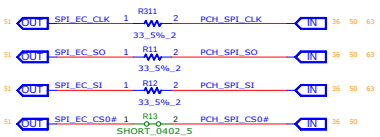
THERM SENSOR

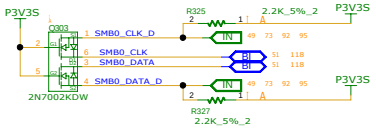


INVENTEC

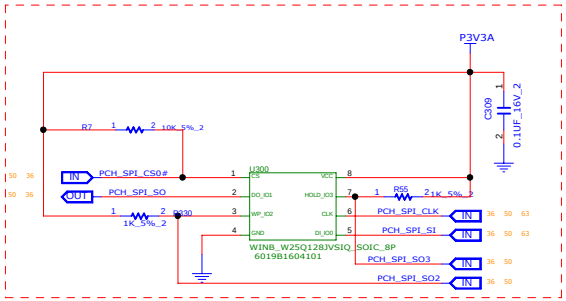
TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		REV X01	
CHANGE by	XXX	DATE	21-OCT-2002	SHEET 49 of 130	
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

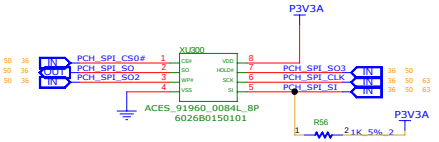
REFERENCE 300~389(KBC)





THERMAL SENSOR
HDMI
DP





R390 FOR INTEL DEBUG

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60Jxxxxxxxxx	PCB VER	XXX

EC

Location 300 ~ 389

2013EE1B

Ver.05_20120824

	VCC(1.8V OR 3.3V)	VSTBY_FSPI(1.8V OR 3.3V)
IT8987E_CX	PIN13 : LPCCLK/GPM4(3) PIN10 : LAD0/GPM0(3) PIN9 : LAD1/GPM1(3) PIN8 : LAD2/GPM2(3) PIN7 : LAD3/GPM3(3) PIN6 : LFRAME#/GPM5(3)	PIN5 : SERIRQ/GPM6(3) PIN105 : FSCK/GPG7 PIN101 : FSCE#/GPG3 PIN102 : FMOSI/GPG4 PIN103 : FMISO/GPG5

U1

ITE_IT8987E_CX_LQFP_128P_HP

6019B1650401

LPC

GPIO

SM BUS

PS/2

CIR

PWM

UART port

WAKE UP

EXTERNAL SERIAL FLASH

SPI ENABLE

A/D D/A

KBMX

CLOCK

Intel DS3 function support

FOR DPTF

noise cap

For Intel platform

Platform	Intel	AMD
R319,R318	10KΩ	NA

Platform	Intel	AMD
R315	330Ω	0Ω

INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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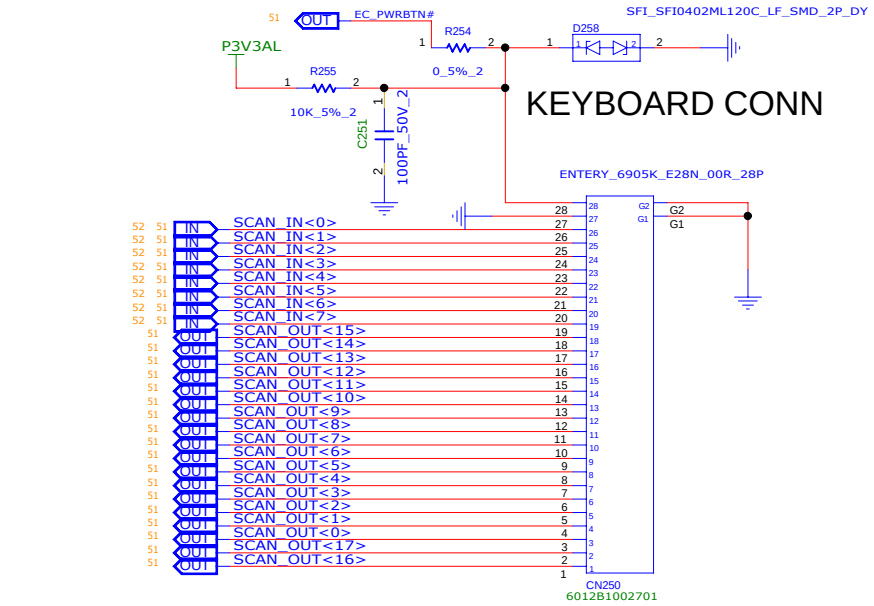
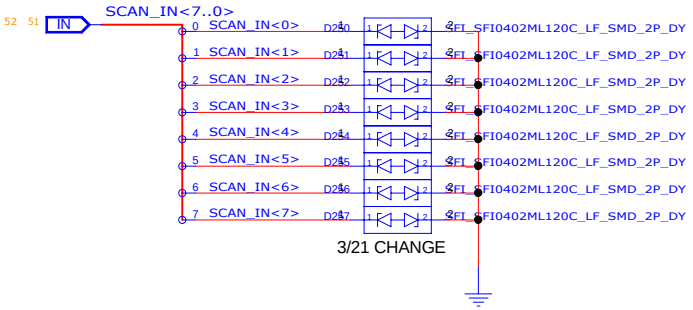
CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	50xxxxxxxxx	PCB VER	XXX

REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)

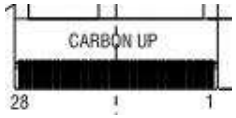


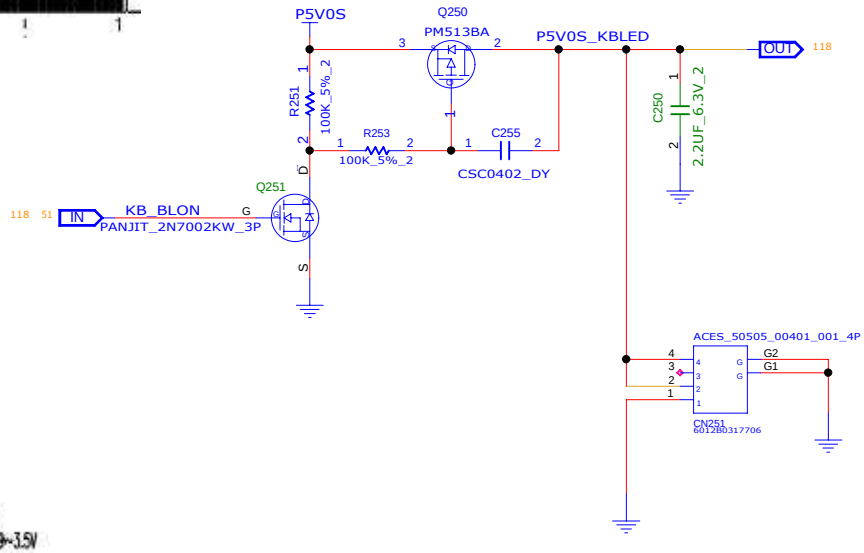
NEE TO CHANGE 6012B1002701
5/2 REVERSE

	14"
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



3/21 CHANGE





KEYBOARD LED CONN

VCC : +5V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 52 of 130	
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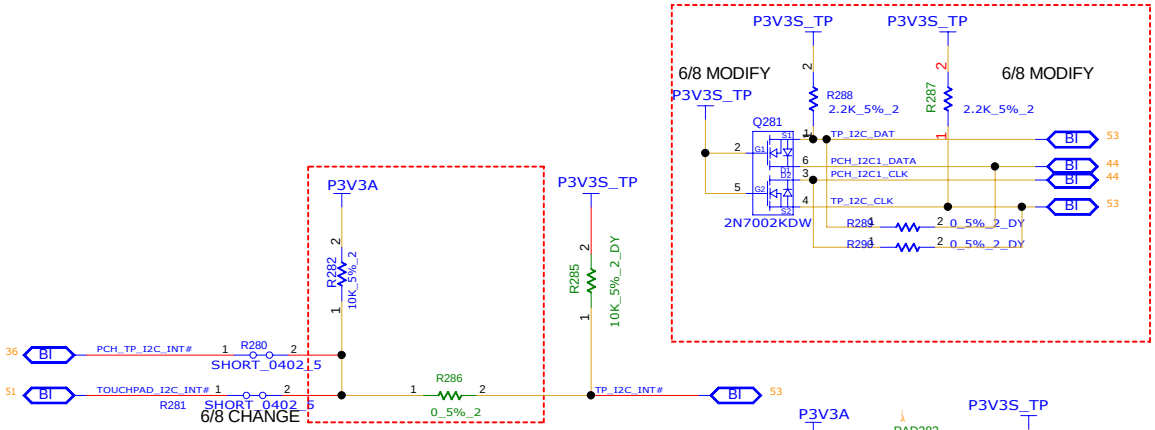

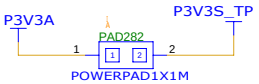

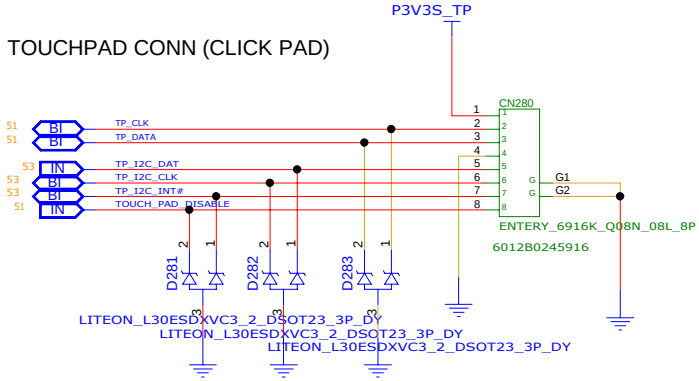

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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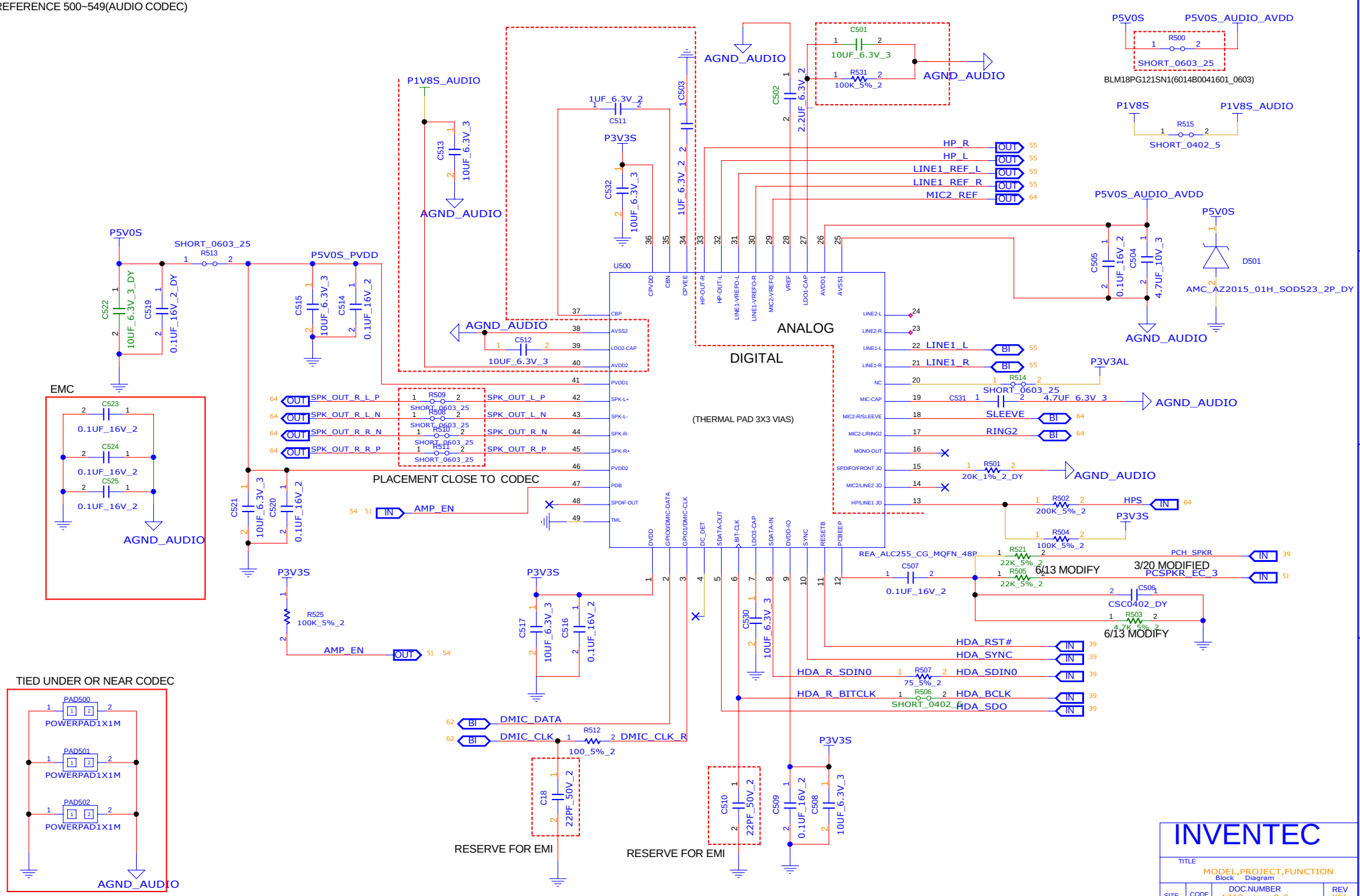
REFERENCE 500~549(AUDIO CODEC)



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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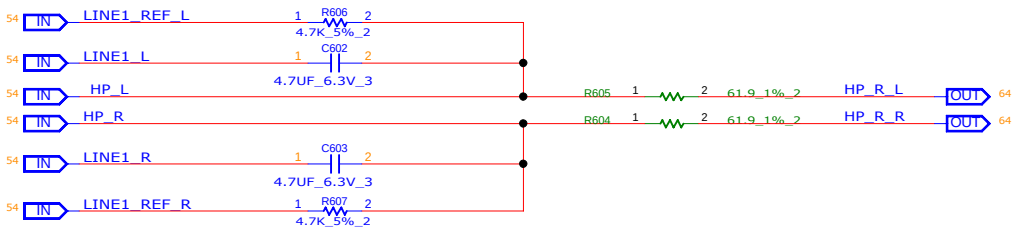
REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



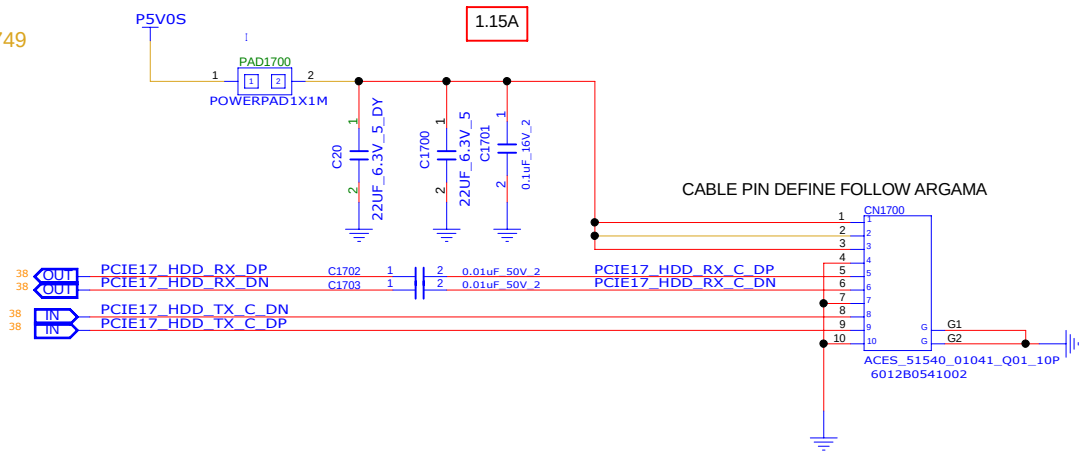
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxx	PCB VER	XXX			SHEET 55 of 130	

SATA HDD CABLE CONN on MB

SATA HDD
Location 1700 ~ 1749



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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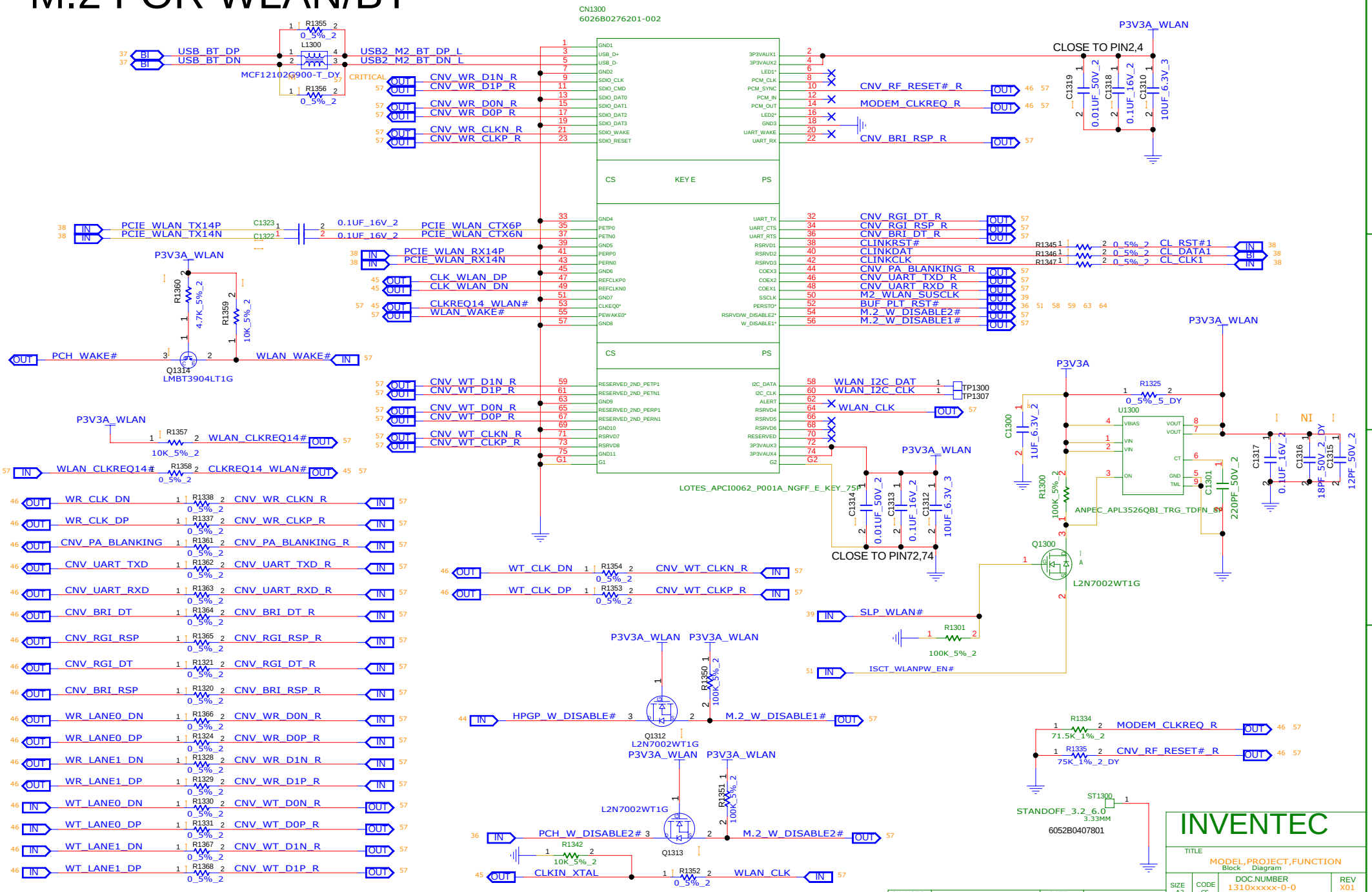
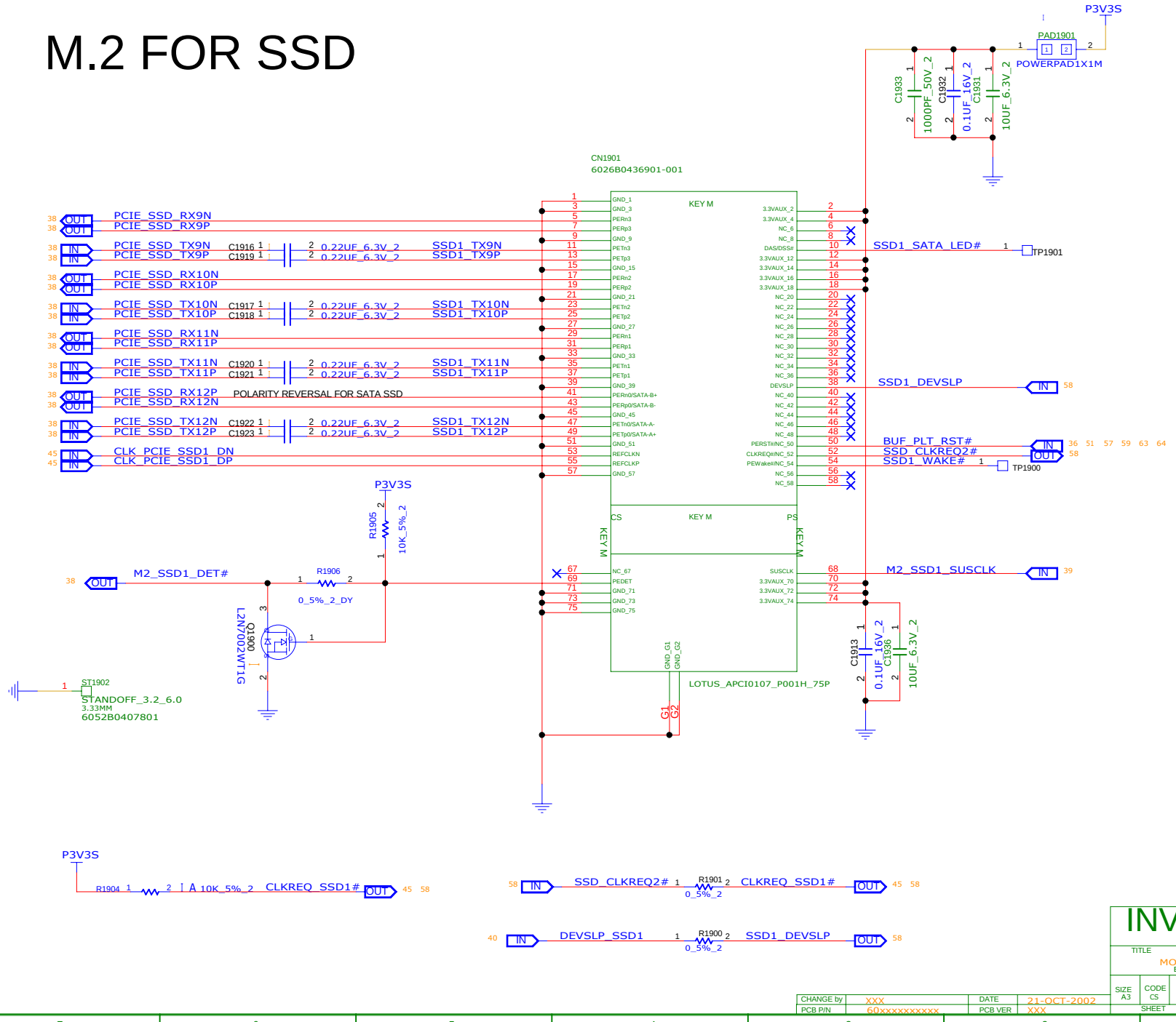
M.2 FOR WLAN/BT



M.2 FOR SSD



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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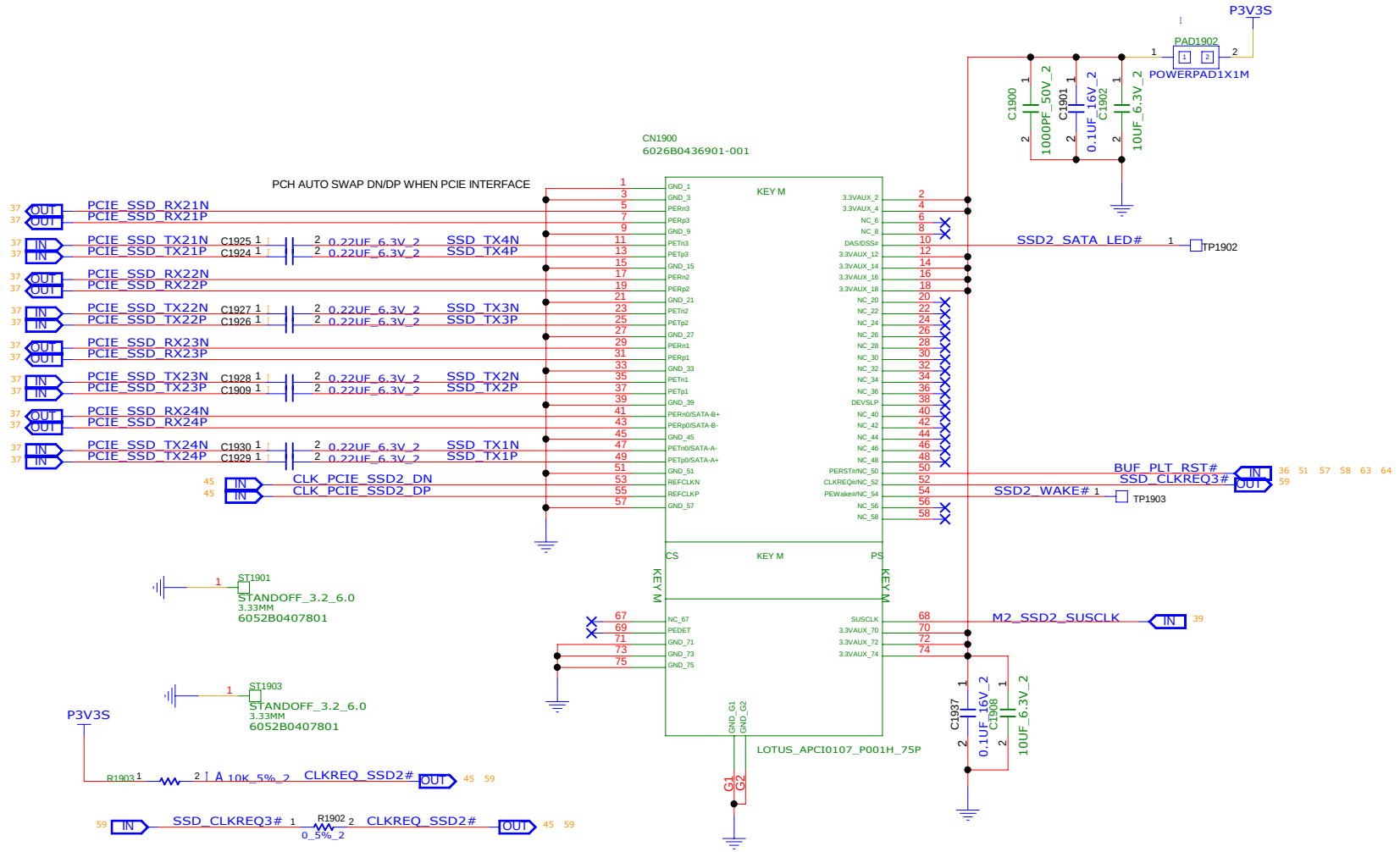
NGFF SSD2(PCIE/SATA 2X)



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

REFERENCE NUMBER:1950~1999

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SATA HDD CONN.		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
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TYPE C OVP

P3V3A
P5V0DS
U8 CRITICAL
R2403 4.7K_5%_2_DY
R2402 10K_5%_2
R2401 10K_5%_2_DY
120K_1%_2 R2410
VBUS_EN
TP2400 1POLARITY
C2403 10UF_6.3V_3
C2402 0.1UF_16V_2
VIA_VP225_DFN_10P
C87 220PF_50V_2
C88 220PF_50V_2
TYPEC_3A
TYPEC_1A5
R2400 10K_1%_2_DY
TYPEC_CC1
TYPEC_CC2

P3V3DS
P5V0DS
USBPWR_EN
VBUS_EN
U2502
NXP_74LVC1G08GW_TSOT353_5P
U2500
TYPEC_SET
GMT_G518B1TP1U_TSOT23_6P
3.5A
R2411 10K_5%_2
C2549 1UF_6.3V_2
PUSB3_PWR2
C2548 10UF_25V_5
C2547 10UF_25V_5
C2551 10UF_25V_5
C2552 100UF_6.3V_DY

USB3_TX1P
USB3_TX1N
C2503 0.22UF_25V_2
C2502 0.22UF_25V_2
USB3_C_TX1P
USB3_C_TX1N
R2514 0_5%_3
R2515 0_5%_3
USB3_L_TX1P
USB3_L_TX1N
USB3_TX2P
USB3_TX2N
C2501 0.22UF_25V_2
C2504 0.22UF_25V_2
USB3_C_TX2P
USB3_C_TX2N
R2503 0_5%_3
R2502 0_5%_3
USB3_L_TX2P
USB3_L_TX2N

TYPEC_SET
Q5 PANJIT_2N7002KW_3P
Q6 PANJIT_2N7002KW_3P
TYPEC_3A
TYPEC_1A5
R2649 8.45K_1%_2
R2680 21K_1%_2
R2681 21K_1%_2
4/27 MODIFY

USB3_RX1N
USB3_RX1P
C2500 0.33UF_25V_2
C2511 0.33UF_25V_2
R2512 0_5%_3
R2513 0_5%_3
R2509 220K_5%_2
R2508 220K_5%_2
USB3_L_RX1N
USB3_L_RX1P

USB2_CN_1P
USB2_CN_1N
D7503 CRITICAL
6011B0172501
AMAZING_AZ1045_04F_R7G_10P
TYPEC_CC2
TYPEC_CC1

USB3_RX2N
USB3_RX2P
C2510 0.33UF_25V_2
C2509 0.33UF_25V_2
R2504 0_5%_3
R2505 0_5%_3
R2507 220K_5%_2
R2506 220K_5%_2
USB3_L_RX2N
USB3_L_RX2P

USB3_L_RX2N
USB3_L_RX2P
D7504 CRITICAL
6011B0172501
AMAZING_AZ1045_04F_R7G_10P
USB3_L_TX1P
USB3_L_TX1N

USB3_L_TX2N
USB3_L_TX2P
D7505 CRITICAL
6011B0172501
AMAZING_AZ1045_04F_R7G_10P
USB3_L_RX1P
USB3_L_RX1N

USB2_REAR_1P
USB2_REAR_1N
0_5%_2_DY R2510
L2500 MCF12102G900-T 6014B0247601
R2511 0_5%_2_DY
USB2_CN_1P
USB2_CN_1N

EMI
C7583 0.1UF_16V_2
C7555 0.1UF_16V_2
C7553 0.1UF_16V_2
C7554 0.1UF_16V_2
DGND_CHASSIS2

PUSB3_PWR2
CN2500
SINGATRON_2UB3C02_101211F_24P
6012B0909301
DGND_CHASSIS2
TYPEC_CC1
USB2_CN_1P
USB2_CN_1N
USB2_CN_2N
USB3_L_TX1P
USB3_L_TX1N
USB3_L_RX2N
USB3_L_RX2P
USB3_L_RX1P
USB3_L_RX1N
USB3_L_TX2N
USB3_L_TX2P
TYPEC_CC2

INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
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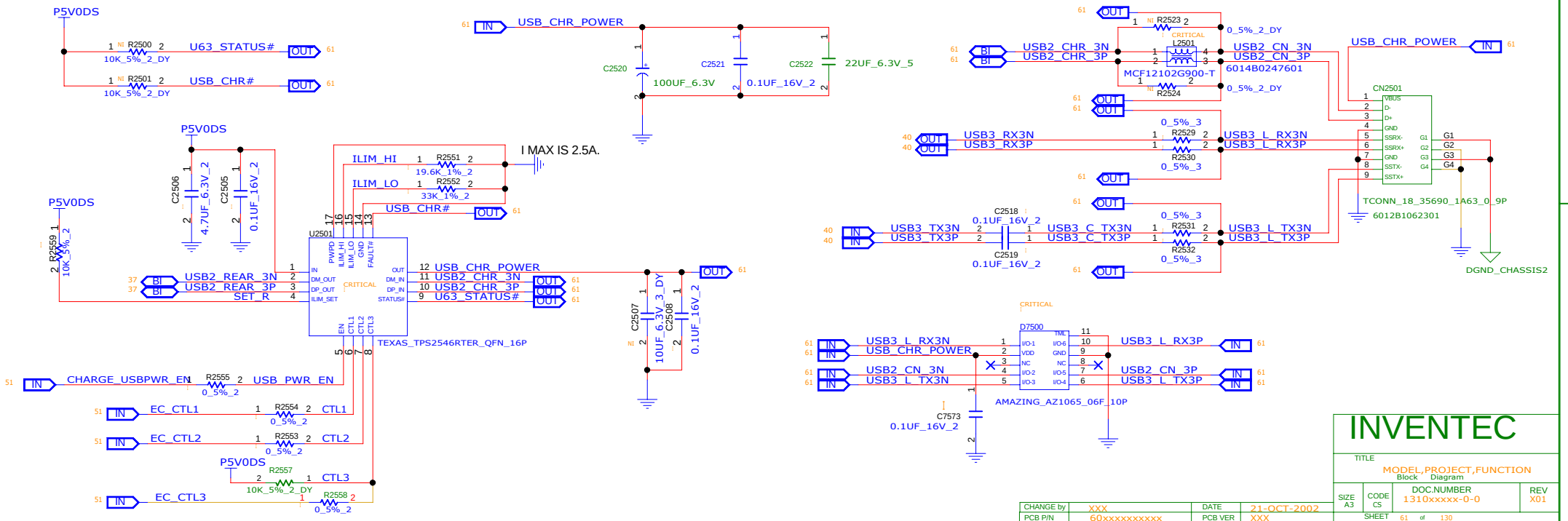
CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

USB CHARGER

USB Faster Charger in S4/S5	USB Charger controller: TI2546	Ctrl-Pin (CTL1/CTL2/CTL3/ILIM_SEL)	Mode	ILIM	Note
Enable	S0	1/1/1/1	CDP	ILIM=2510mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
Disable	S0	1/1/1/1	CDP	ILIM=1525mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/0/0	Turn off switch	ILIM=1525mA	No support charger



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
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SIZE	CODE	DOC.NUMBER	REV
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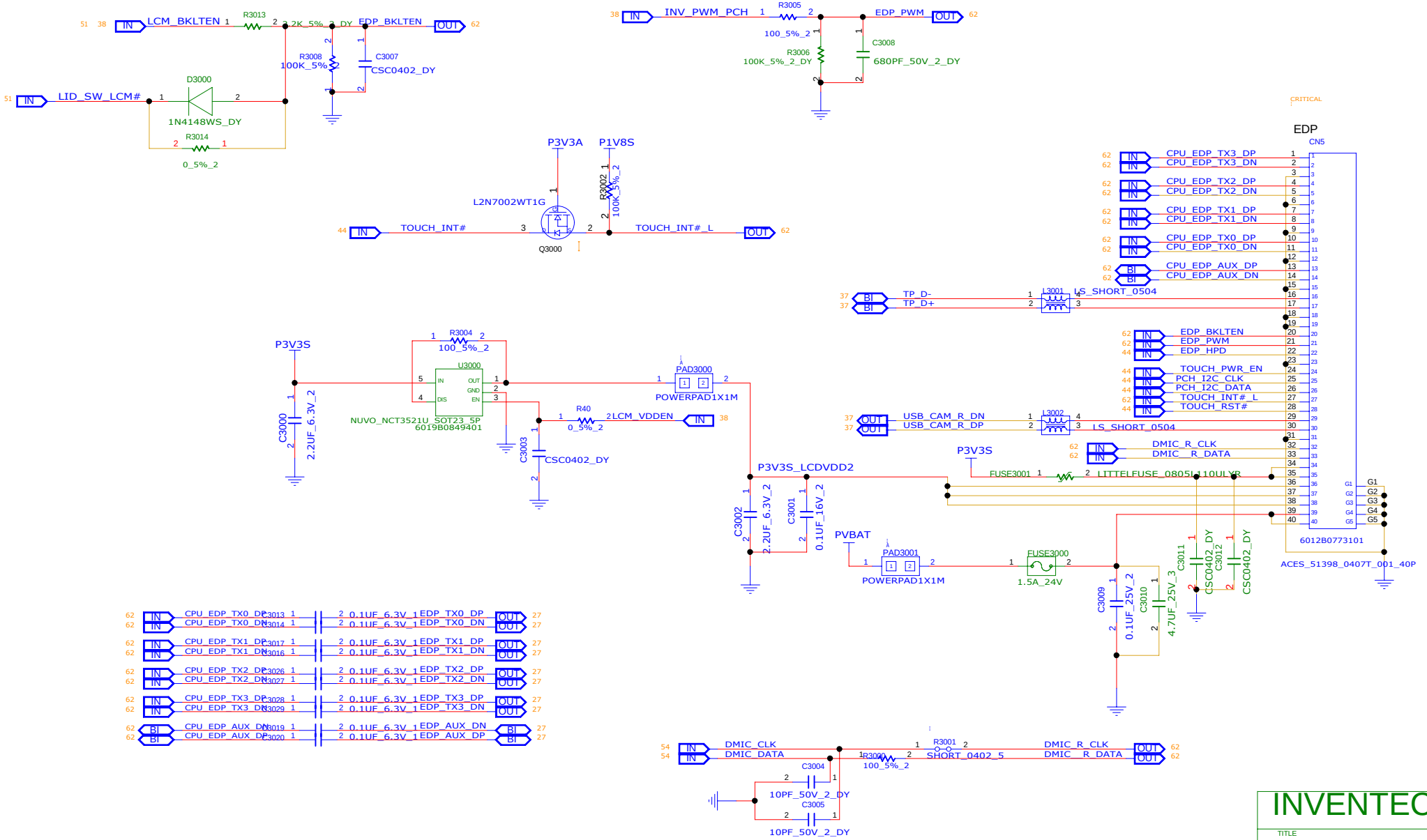
REFFERENCE 3000~3049(LCM)

EDP CONN



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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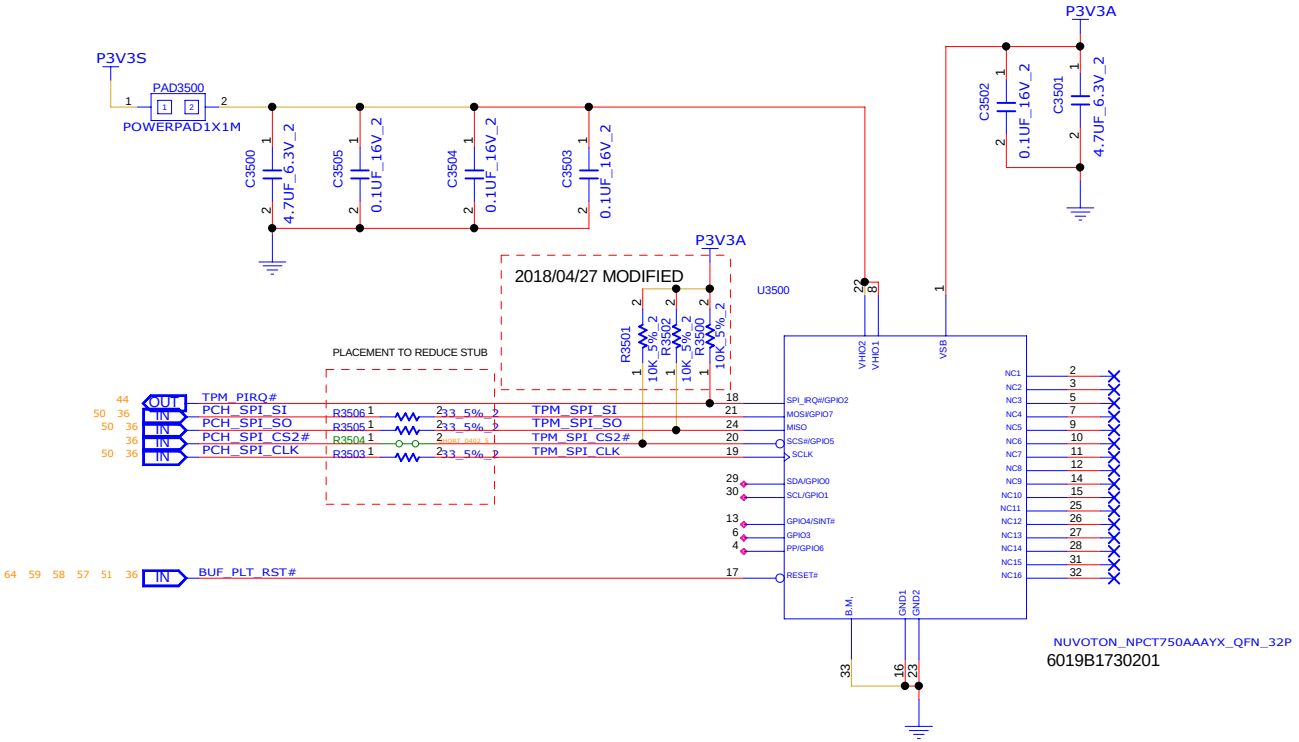

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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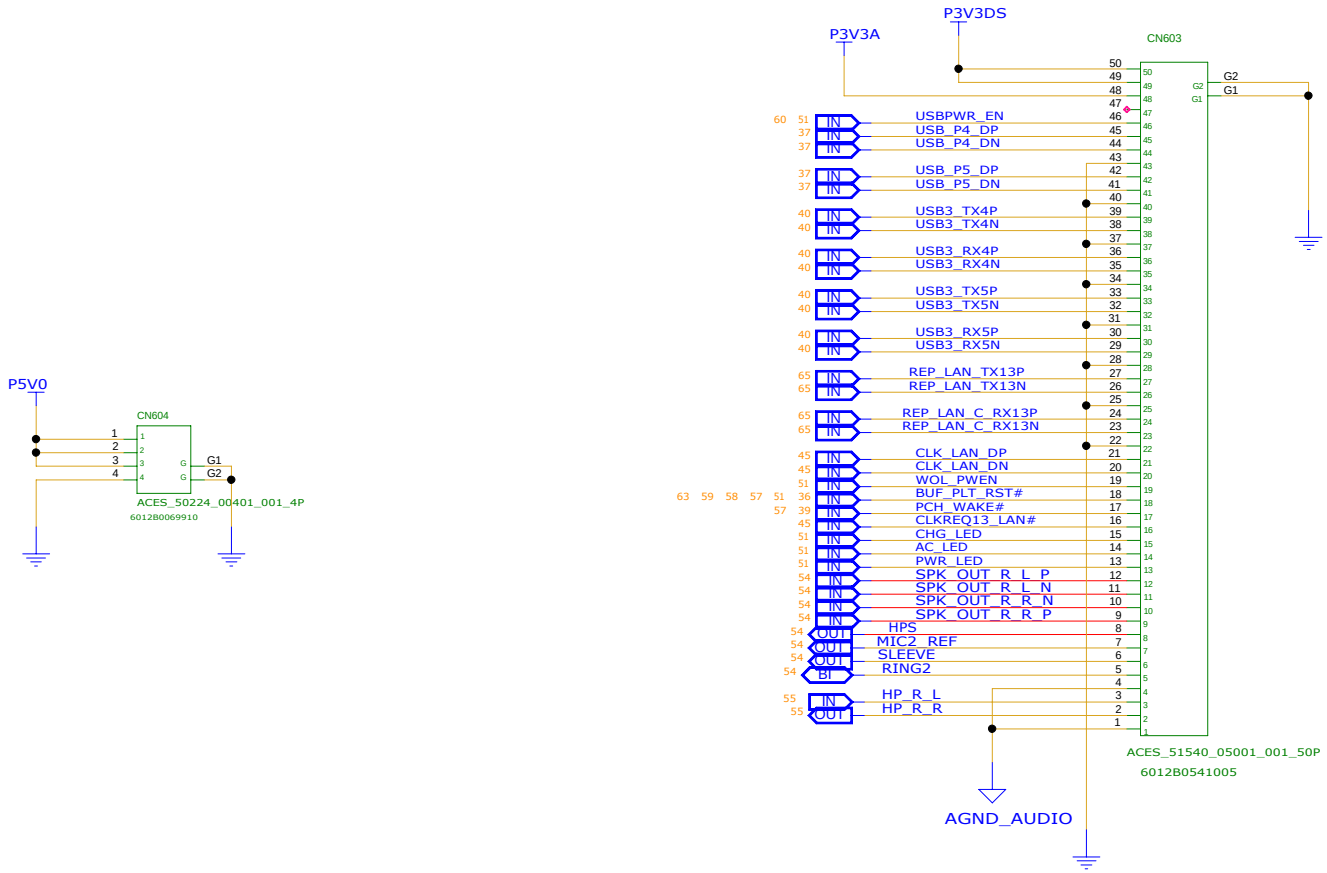

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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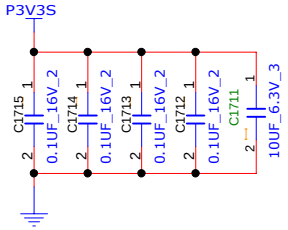
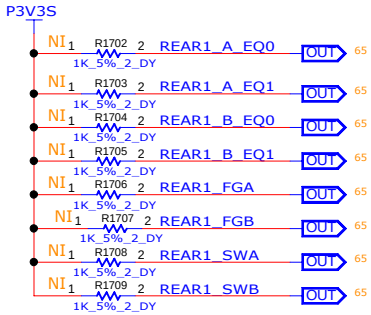
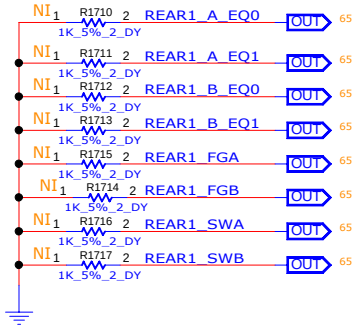
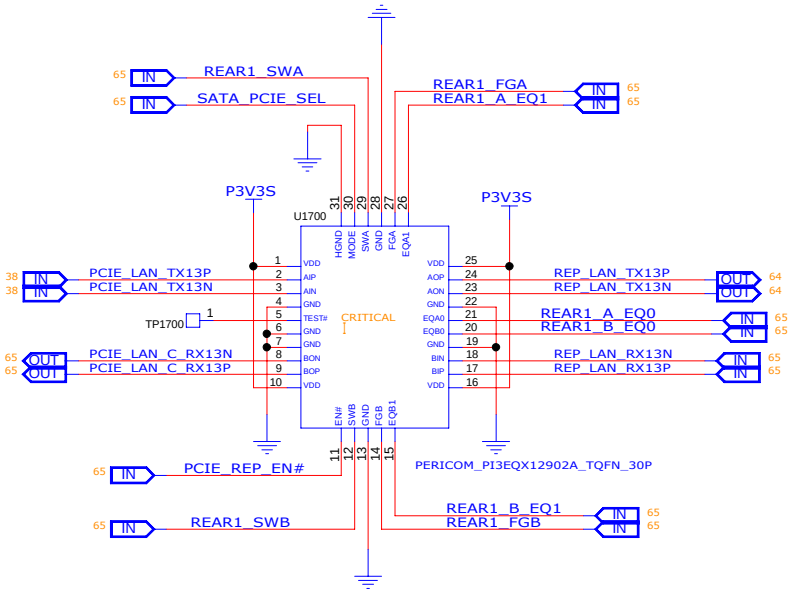
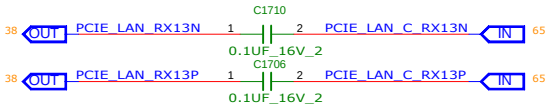
PCIE REPEATER

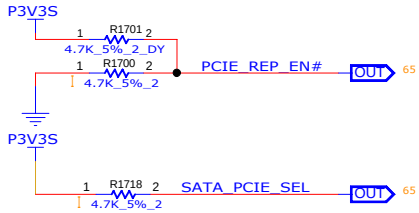


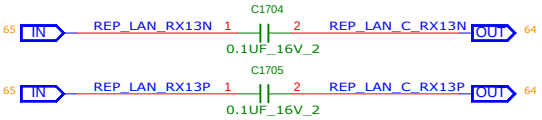












INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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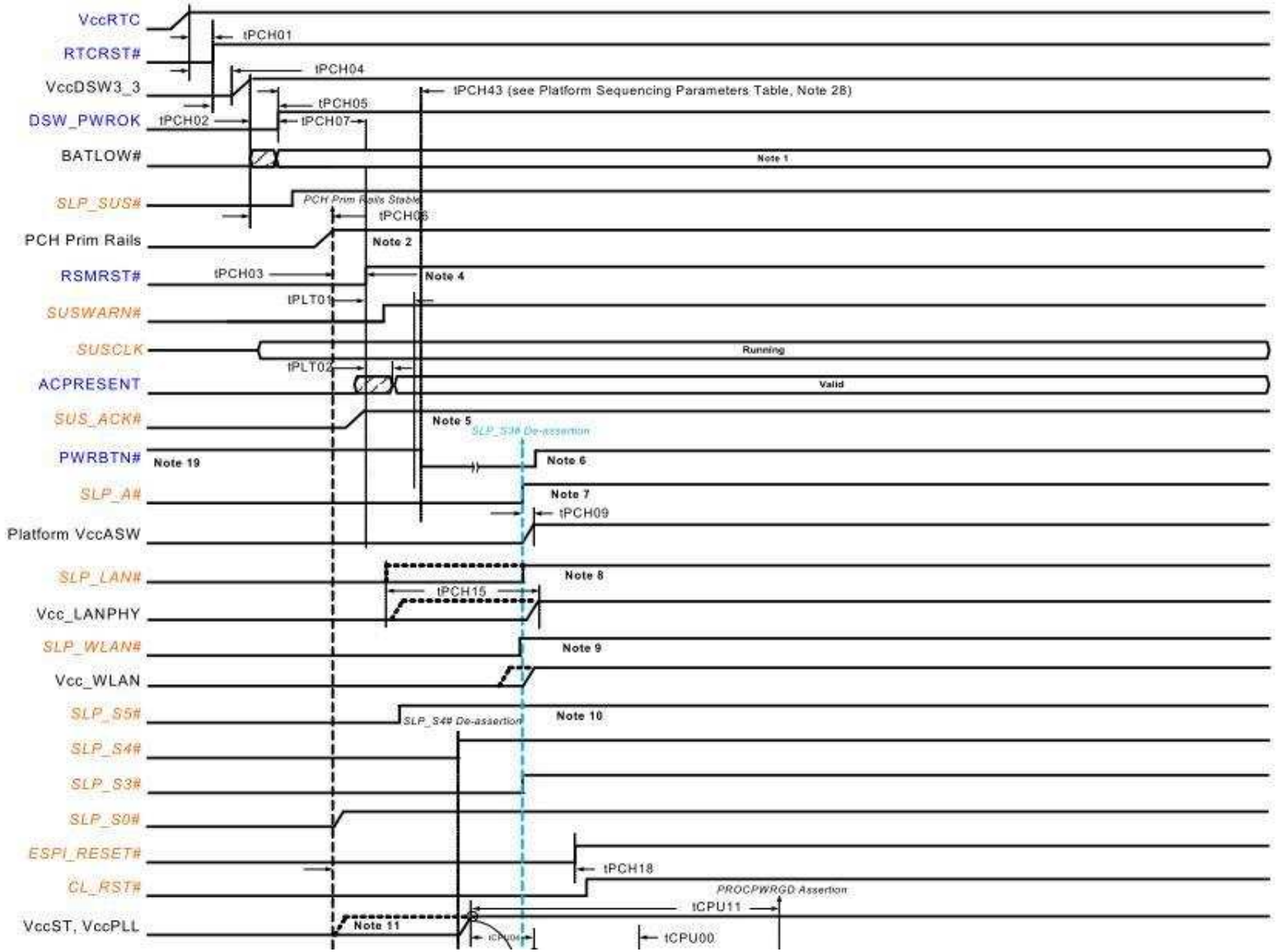

INVENTEC

TITLE
MODEL_PROJECT_FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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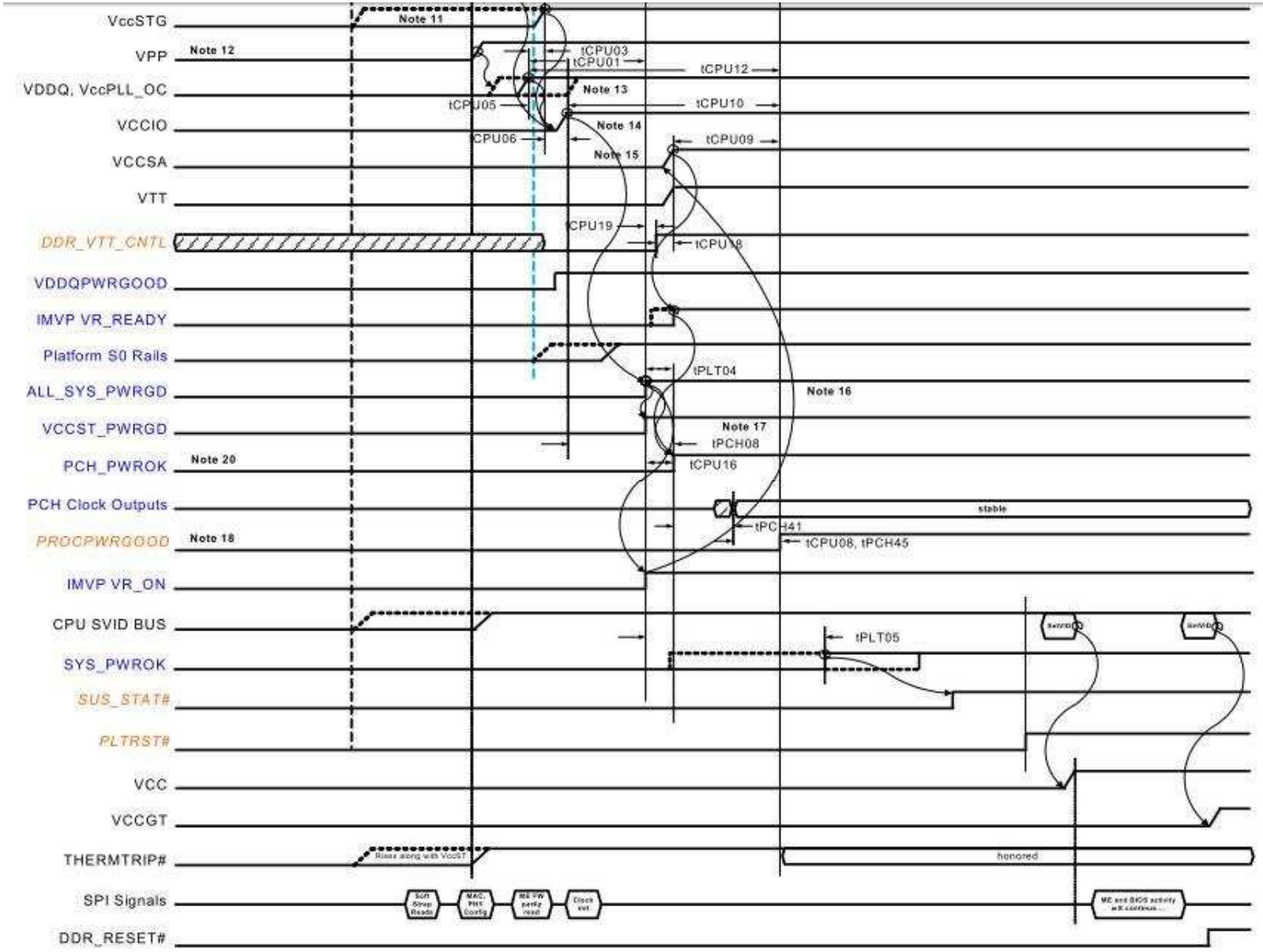

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		REV X01	
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CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

07e3020d0714280027008b3c1a003fc1

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
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Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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07e3020d0714280027008b3c1a003fc1

07e3020d0714280027008b3c1a003fc1

N18E-G0
N18E-G1
N18E-G2 MAX-Q

8GB DDR5 256M X 16 X 2 X6

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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PCA CODE NAME： N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001
G1 : 6019B1849201
G2 MAXQ:6019B1849301

PCB VERSION：X01
BOARD SIZE:

SCH P/N:
PCB P/N:
PCA P/N:

SHEET	CONTENT	SHEET	CONTENT
71	TITLE	101	GPU 1V8_AON DECOUPLING
72	INDEX	102	GPU NVDD DECOUPLING
73	VGA CONNECTION WITH MAINBOARD	103	GPU FBVDD DECOUPLING
74	GPU PCI-E GEN3 X 16	104	GPU GND
75	GPU MEMORY PARTITION A	105	GPU POWER SEQUENCE
76	GPU MEMORY PARTITION B	106	GPU POWER DISCHARGE
77	GPU MEMORY PARTITION C	107	GPU 1V8_MAIN
78	GPU MEMORY PARTITION D	108	GPU_NVVDD/NVVDDS (MP2886A)
79	GPU MEMORY FBA PARTITION 31-0	109	PVCORE_DGPU (MP86941_1-2P)
80	GPU MEMORY FBA PARTITION 63-32	110	PVCORE_DGPU (MP86941_3-4P)
81	GPU MEMORY FBB PARTITION 31-0	111	PVCORE_DGPU (MP86941_5-6P)
82	GPU MEMORY FBB PARTITION 63-32	112	P1V35S_DGPU (RT8816A_2P)
83	GPU MEMORY FBC PARTITION 31-0	113	P1V0S_DGPU (RT8068A)
84	GPU MEMORY FBC PARTITION 63-32	114	P1V8S_DGPU (RT8068A)
85	GPU MEMORY FBD PARTITION 31-0	115	NOTES
86	GPU MEMORY FBD PARTITION 63-32	116	HISTORY
87	GPU 27 MHZ XTAL	117	
88	GPU VBIOS, STRAPS	118	
89	GPU GPIOS	119	
90	GPU IFP_AB	120	
91	GPU DP IFP_CD	121	
92	GPU DP REDRIVER PI3DPX1203ZHEX	122	
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94	GPU HDMI IFP_EF	124	
95	GPU HDMI RETIMER IT66317	125	
96	GPU HDMI CONNECTOR	126	
97	GPU NVHS	127	
98	OVR-M	128	
99	GPU NVDD	129	
100	GPU FBVDD	130	

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL
NI: NON-INSTALL
DY: NON-INSTALL
MP: PRODUCTION
PROTO: PRE-PRODUCTION
CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14
6019B1847601

MICRON MT61K256M32JE-14:A
6019B1847701

INVENTEC

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CONNECTION TO MAINBOARD

74 45 CLK_PCIE_DGPU_100MHZ_P
74 45 CLK_PCIE_DGPU_100MHZ_N

74 26 PCIE_DGPU_RX15P
74 26 PCIE_DGPU_RX15N
74 26 PCIE_DGPU_TX15P
74 26 PCIE_DGPU_TX15N
74 26 PCIE_DGPU_RX14P
74 26 PCIE_DGPU_RX14N
74 26 PCIE_DGPU_TX14P
74 26 PCIE_DGPU_TX14N
74 26 PCIE_DGPU_RX13P
74 26 PCIE_DGPU_RX13N
74 26 PCIE_DGPU_TX13P
74 26 PCIE_DGPU_TX13N
74 26 PCIE_DGPU_RX12P
74 26 PCIE_DGPU_RX12N
74 26 PCIE_DGPU_TX12P
74 26 PCIE_DGPU_TX12N
74 26 PCIE_DGPU_RX11P
74 26 PCIE_DGPU_RX11N
74 26 PCIE_DGPU_TX11P
74 26 PCIE_DGPU_TX11N
74 26 PCIE_DGPU_RX10P
74 26 PCIE_DGPU_RX10N
74 26 PCIE_DGPU_TX10P
74 26 PCIE_DGPU_TX10N
74 26 PCIE_DGPU_RX9P
74 26 PCIE_DGPU_RX9N
74 26 PCIE_DGPU_TX9P
74 26 PCIE_DGPU_TX9N
74 26 PCIE_DGPU_RX8P
74 26 PCIE_DGPU_RX8N
74 26 PCIE_DGPU_TX8P
74 26 PCIE_DGPU_TX8N
74 26 PCIE_DGPU_RX7P
74 26 PCIE_DGPU_RX7N
74 26 PCIE_DGPU_TX7P
74 26 PCIE_DGPU_TX7N
74 26 PCIE_DGPU_RX6P
74 26 PCIE_DGPU_RX6N
74 26 PCIE_DGPU_TX6P
74 26 PCIE_DGPU_TX6N
74 26 PCIE_DGPU_RX5P
74 26 PCIE_DGPU_RX5N
74 26 PCIE_DGPU_TX5P
74 26 PCIE_DGPU_TX5N
74 26 PCIE_DGPU_RX4P
74 26 PCIE_DGPU_RX4N
74 26 PCIE_DGPU_TX4P
74 26 PCIE_DGPU_TX4N
74 26 PCIE_DGPU_RX3P
74 26 PCIE_DGPU_RX3N
74 26 PCIE_DGPU_TX3P
74 26 PCIE_DGPU_TX3N
74 26 PCIE_DGPU_RX2P
74 26 PCIE_DGPU_RX2N
74 26 PCIE_DGPU_TX2P
74 26 PCIE_DGPU_TX2N
74 26 PCIE_DGPU_RX1P
74 26 PCIE_DGPU_RX1N
74 26 PCIE_DGPU_TX1P
74 26 PCIE_DGPU_TX1N
74 26 PCIE_DGPU_RX0P
74 26 PCIE_DGPU_RX0N
74 26 PCIE_DGPU_TX0P
74 26 PCIE_DGPU_TX0N

105 93 91 44 DGPU_PWR_EN

GPU PWR ENABLE COME FROM PCH/EC
MAKE SURE 10K P3V3S PULL UP

74 36 PCH_PLTRST#_BUF

PCH PLATFORM RESET#
MAKE SURE 100K PULL TO GND

74 44 IRMT_HOLD_RST#

PCH HOLD RESET#
MAKE SURE 100K PULL TO GND

TO PCH

89 44 GPU_EVENT_PCH#

PCH INFORM GPU WILL EXIT GC6 MODS

89 51 DGPU_PWRLEVEL

15.3.2 PWR_LEVEL* (GPIO12)

The POWER_LEVEL input signal triggers an immediate GPU hardware slow-down, followed by the driver capping the GPU power state to the appropriate limit. There are two events that can trigger this signal assertion: AC to battery power transition or total system power overdraw event.

74 45 PEX_CLKREQ#

PCIE CLK REQUESTD#

105 51 ALL_POWER_GOOD

GPU ALL S RAIL GOOD
MAKE SURE 10K P3V3S PULL UP

93 44 DP_MA_HPD#

DP HPD TO MAINBOARD
MAKE SURE 10K P3V3S PULL UP

95 92 73 50 49 SMB0_DATA_D
95 92 73 50 49 SMB0_CLK_D

DP REDRIVER I2C CONNECT TO MOBARD
MAINBOARD NEED TO PULL UP

95 44 HDMI_MB_HPD#

HDMI HPD TO MB

95 92 73 50 49 SMB0_DATA_D
SMB0_CLK_D

HDMI RETIMER I2C TO MB
MAINBOARD NEED TO PULL UP

89 51 GPU_OVERT_EC#

3.3V LEVEL
OVER TEMPERATURE TO PCH OR EC

105 89 44 GC6_FB_EN_PCH

3.3V LEVEL
GC6 ENABLE SIGNAL TO PCH OR EC

EC

89 51 EC_SMBDATA0
89 51 EC_SMBCLK0

GPU I2C, COMMUNCATED WITH EC
THIS SIGNAL REQUIRE AN EXTERNAL PULL UP

INVENTEC

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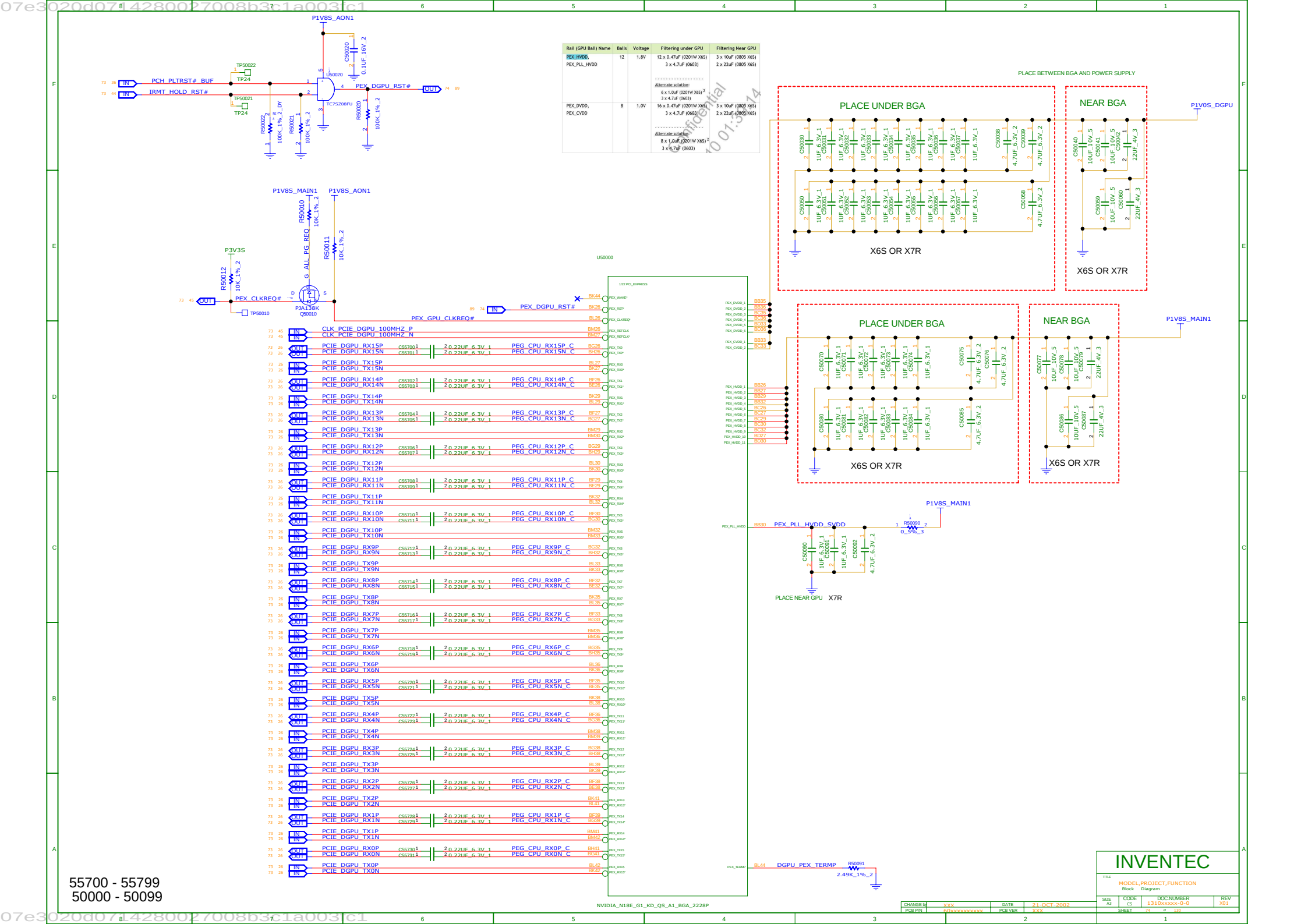
PCB P/N	60xxxxxxxxx	PCB VER	XXX



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD, PEX_PLL_HVDD	12	1.8V	12 x 0.47uF (0201W X6S) 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
			Alternate solution: 6 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	
PEX_DVDD, PEX_CVDD	8	1.0V	16 x 0.47uF (0201W X6S) 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
			Alternate solution: 8 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	

CHANGE ID	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-D-D	X01
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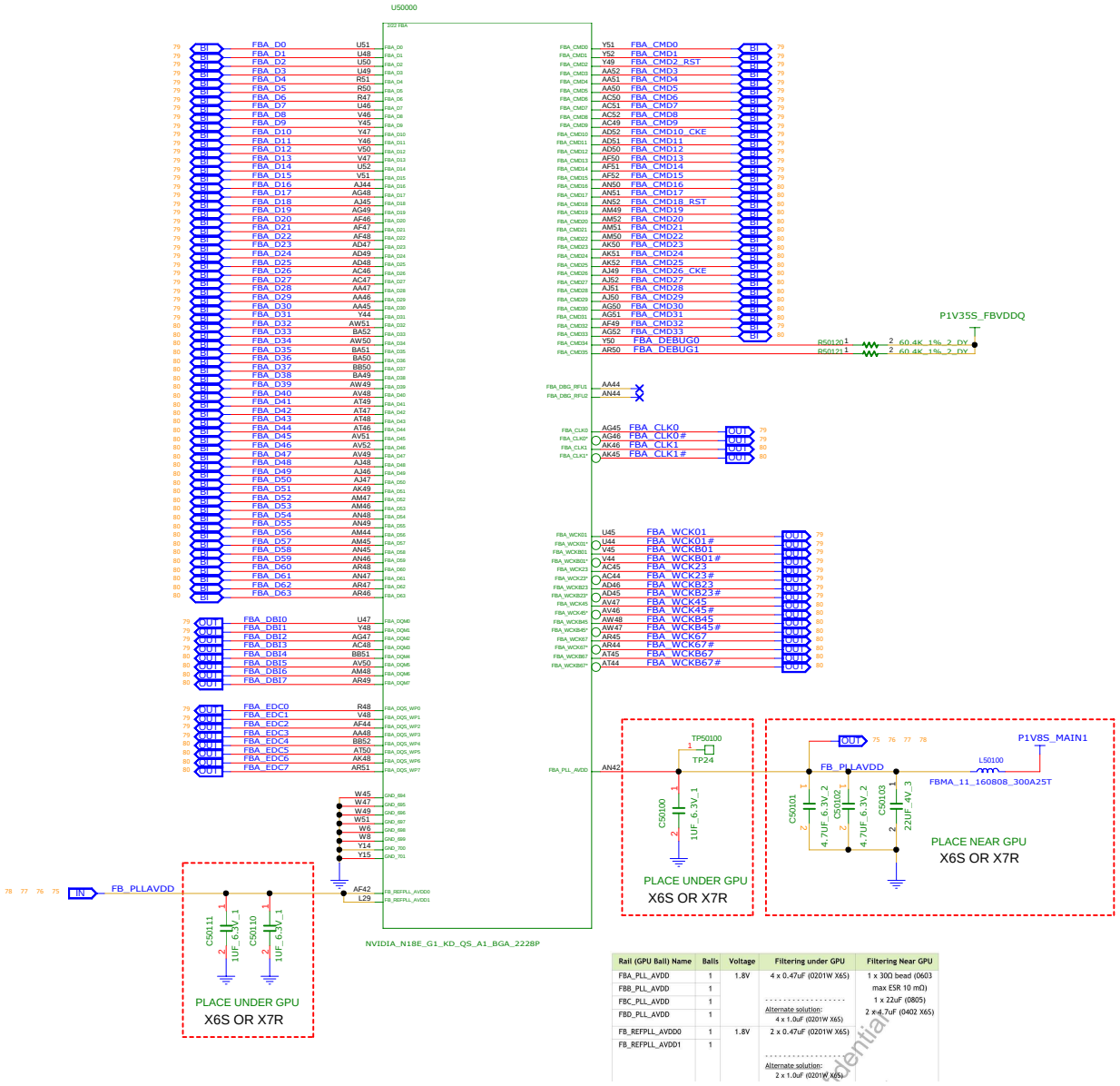
GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603
FBB_PLL_AVDD	1			max ESR 10 mΩ)
FBC_PLL_AVDD	1		- - - - - - - - - - - - - - - - -	1 x 22uF (0805)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	2 x 4.7uF (0402 X6S)
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		- - - - - - - - - - - - - - - - - Alternate solution: 2 x 1.0uF (0201W X6S)	



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603
FBB_PLL_AVDD	1			max ESR 10 mΩ)
FBC_PLL_AVDD	1		- - - - - - - - - - - - - - - - -	1 x 22uF (0805)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	2 x 4.7uF (0402 X6S)
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		- - - - - - - - - - - - - - - - - Alternate solution: 2 x 1.0uF (0201W X6S)	

50100 - 50199

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-D-D	X01
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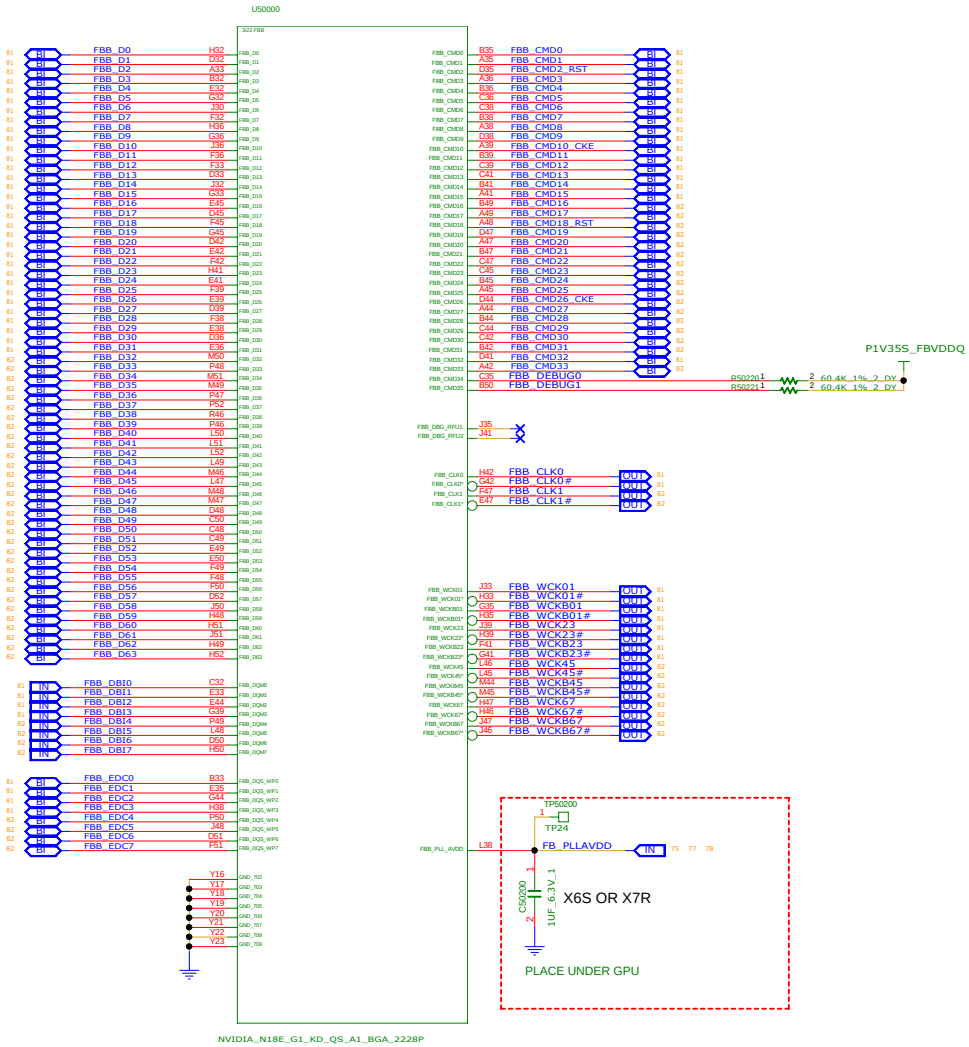
GPU FRAME BUFFER B



50200 - 50299

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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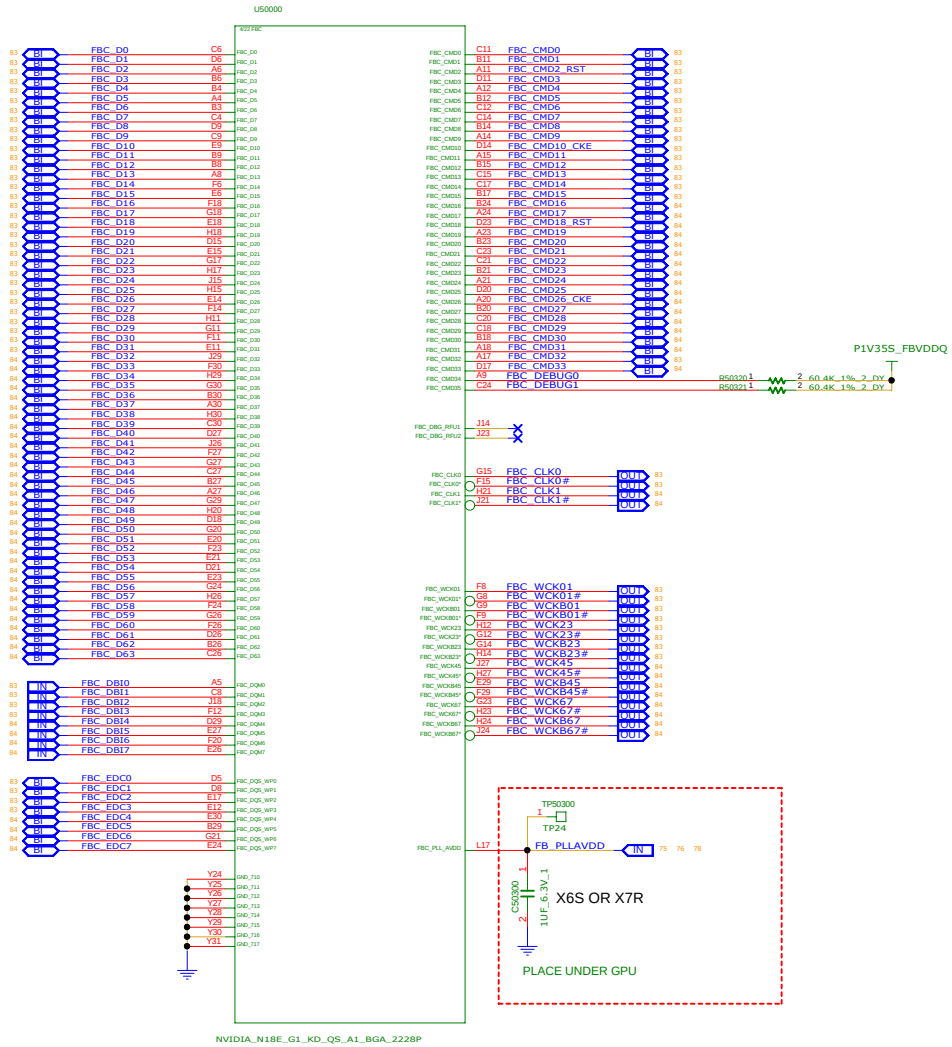
GPU FRAME BUFFER C



50300 - 50399

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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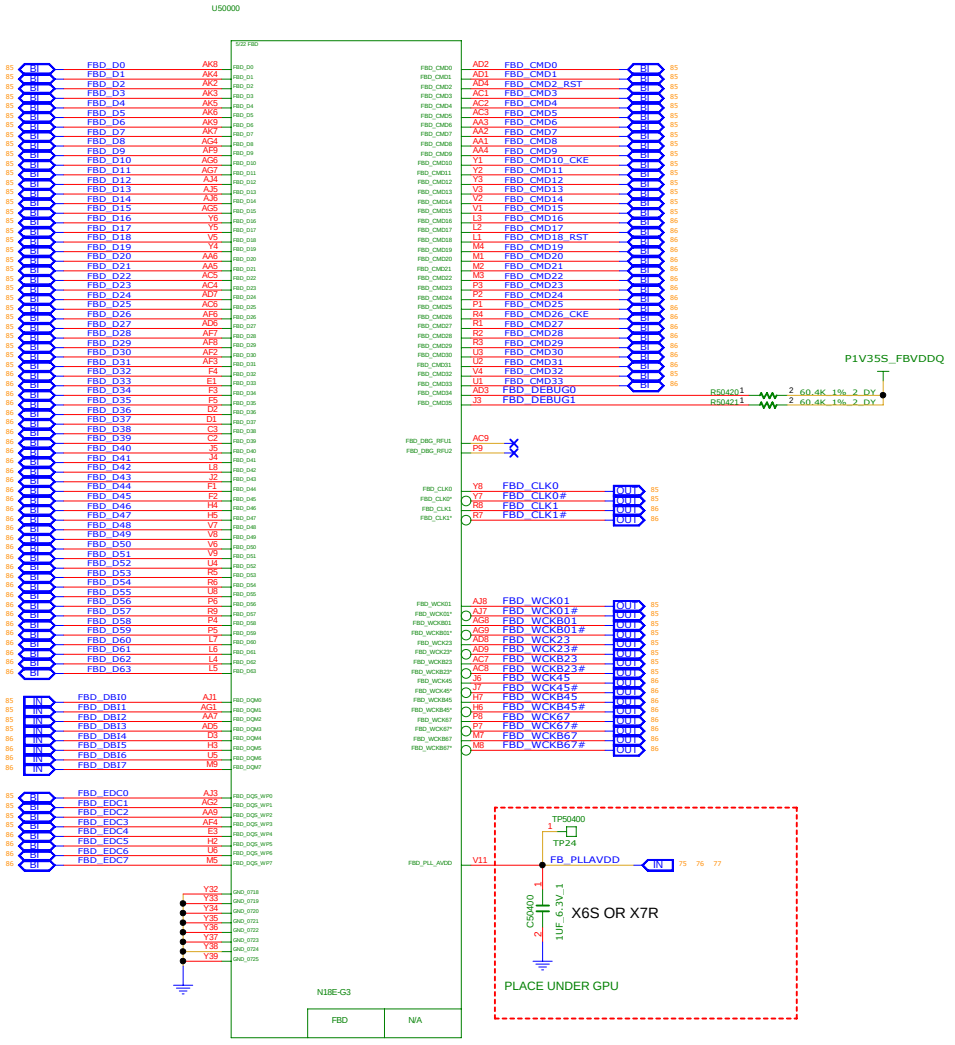
GPU FRAME BUFFER D



50400 - 50499

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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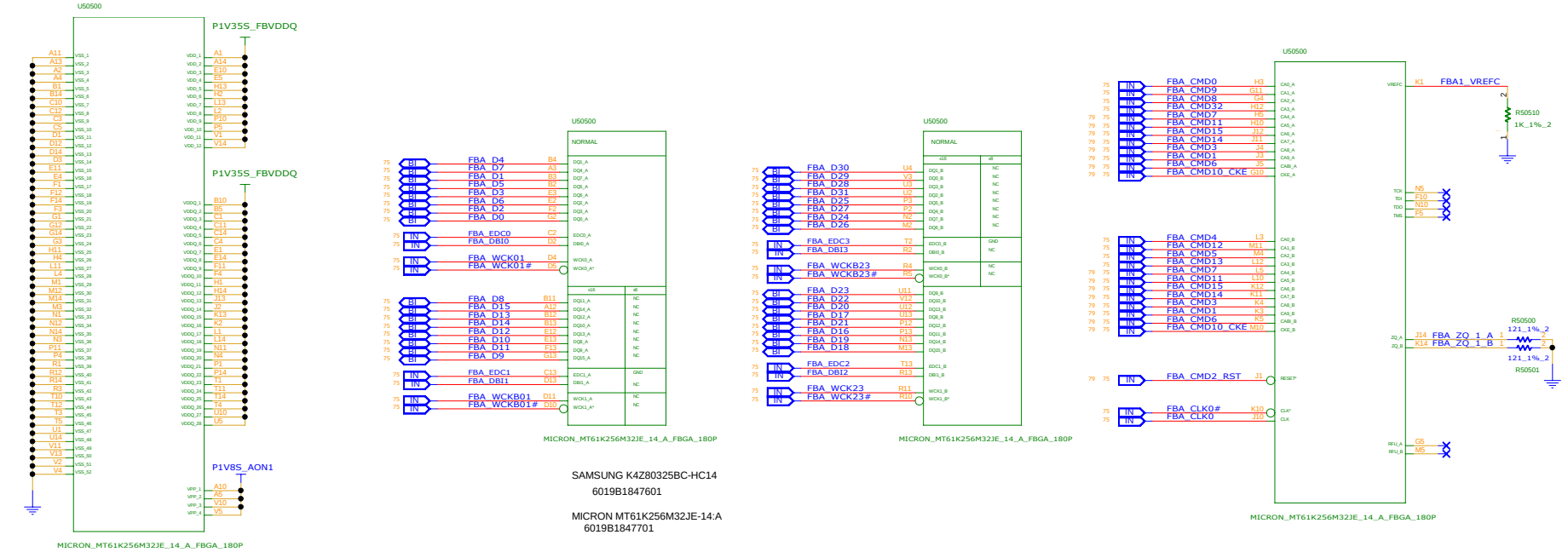
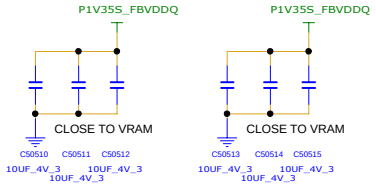
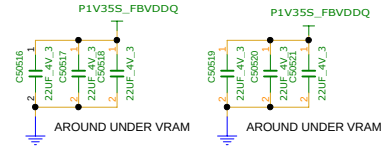
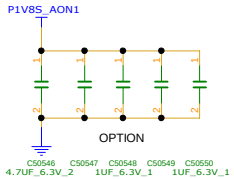
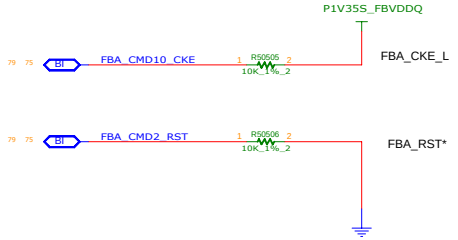
CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

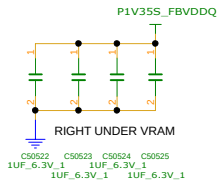


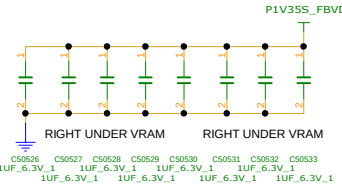


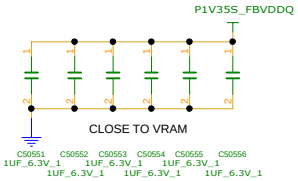


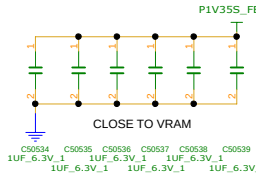


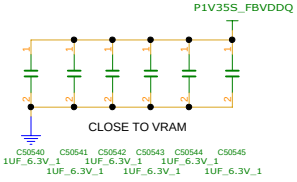












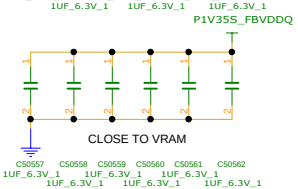


Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF NOTE 2	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Around DRAM
22 uF	X6S [0603]	6	
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

NOTE 1: NVIDIA reference designs use and recommend 0204 or 0201W capacitors where needed. PCB design teams should ensure that component placement equipment can support the smaller package size.

NOTE 2: Alternatively, instead of using 36 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 18 capacitors of value 1.0 uF (X6S, 0201W).

NOTE 3: Alternatively, instead of using 4 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 4 capacitors of value 1.0uF (X6S, 0201W), one per VPP ball.

50500 - 50599

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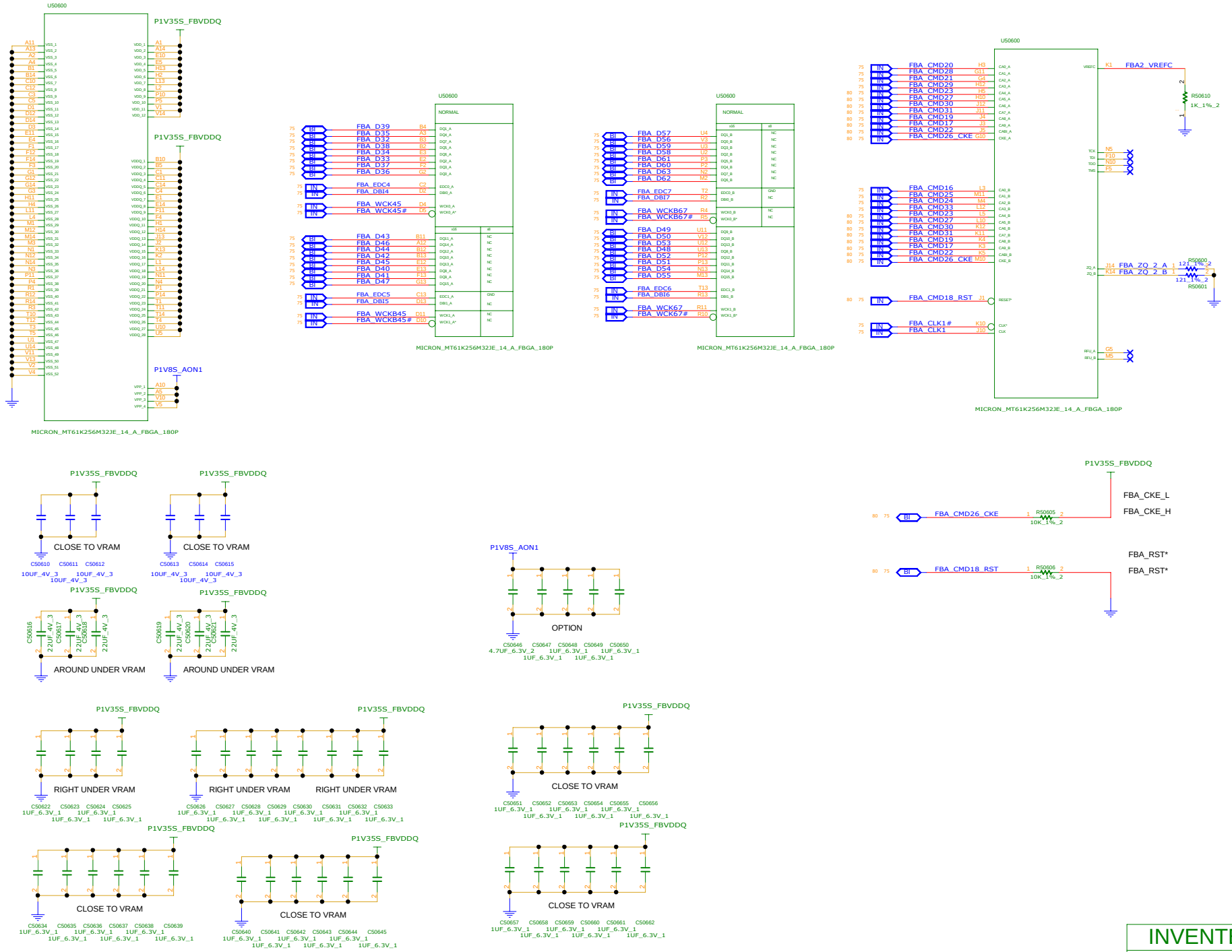
CHANGE ID	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



50600 - 50699

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MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE NO	XXX	DATE	21-OCT-2002
PCB P/N	60Xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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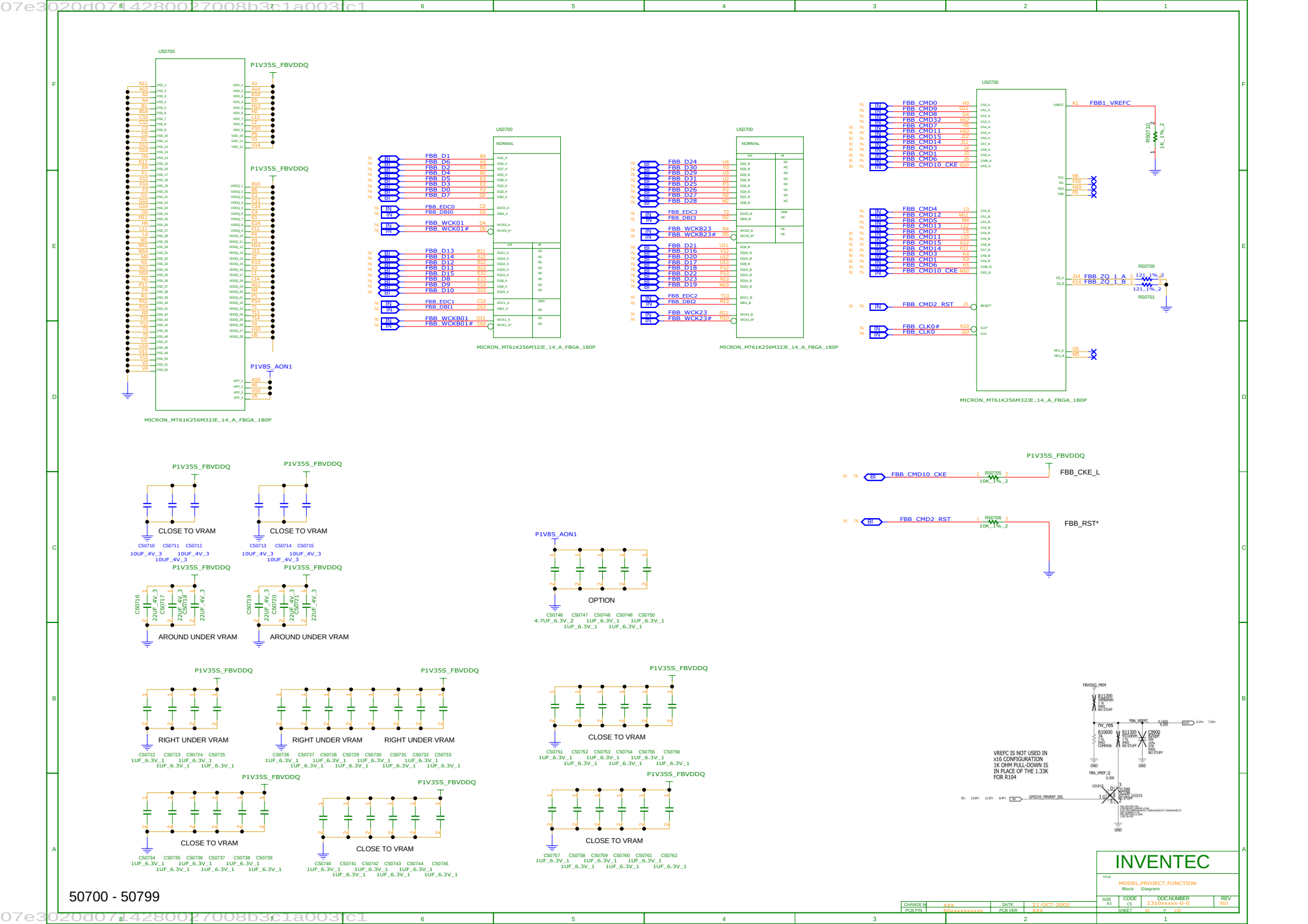
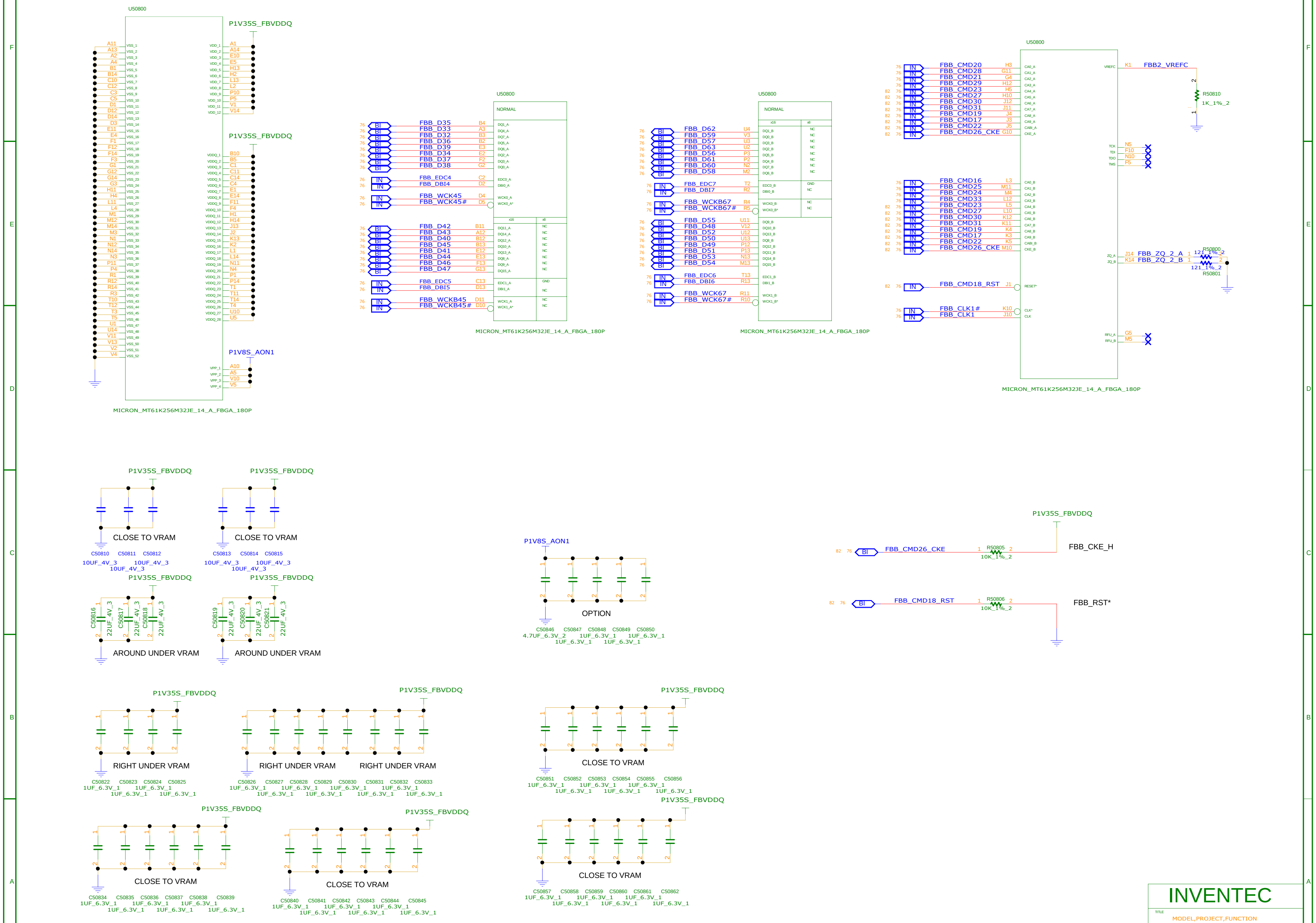

U50700
P1V35S_FBVDDQ
P1V8S_AON1
MICRON_MT61K256M32JE_14_A_FBGA_180P
FBB_D1
FBB_D6
FBB_D2
FBB_D4
FBB_D5
FBB_D3
FBB_D0
FBB_D7
FBB_EDC0
FBB_DBI0
FBB_WCK01
FBB_WCK01#
FBB_D13
FBB_D14
FBB_D12
FBB_D11
FBB_D15
FBB_D8
FBB_D9
FBB_D10
FBB_EDC1
FBB_DBI1
FBB_WCKB01
FBB_WCKB01#
FBB_D24
FBB_D30
FBB_D29
FBB_D31
FBB_D25
FBB_D26
FBB_D27
FBB_D28
FBB_EDC3
FBB_DBI3
FBB_WCKB23
FBB_WCKB23#
FBB_D21
FBB_D16
FBB_D20
FBB_D17
FBB_D18
FBB_D22
FBB_D23
FBB_D19
FBB_EDC2
FBB_DBI2
FBB_WCK23
FBB_WCK23#
FBB_CMD0
FBB_CMD9
FBB_CMD8
FBB_CMD32
FBB_CMD7
FBB_CMD11
FBB_CMD15
FBB_CMD14
FBB_CMD3
FBB_CMD1
FBB_CMD6
FBB_CMD10_CKE
FBB_CMD4
FBB_CMD12
FBB_CMD5
FBB_CMD13
FBB_CMD7
FBB_CMD11
FBB_CMD15
FBB_CMD14
FBB_CMD3
FBB_CMD1
FBB_CMD6
FBB_CMD10_CKE
FBB_CMD2_RST
FBB_CLK0#
FBB_CLK0
FBB1_VREFC
R50710
1K_1%_2
R50700
121_1%_2
FBB_ZQ_1_A
FBB_ZQ_1_B
R50701
FBB_CKE_L
FBB_RST*
R50705
10K_1%_2
R50706
10K_1%_2
CLOSE TO VRAM
AROUND UNDER VRAM
OPTION
RIGHT UNDER VRAM
VREFC IS NOT USED IN x16 CONFIGURATION 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R104
GPIO10_FBVREF_SEL
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
50700 - 50799



50800 - 50899

INVENTEC					
TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		
SIZE	CODE	DOC.NUMBER	REV		
A3	CS	1310xxxxx-0-0	X01		
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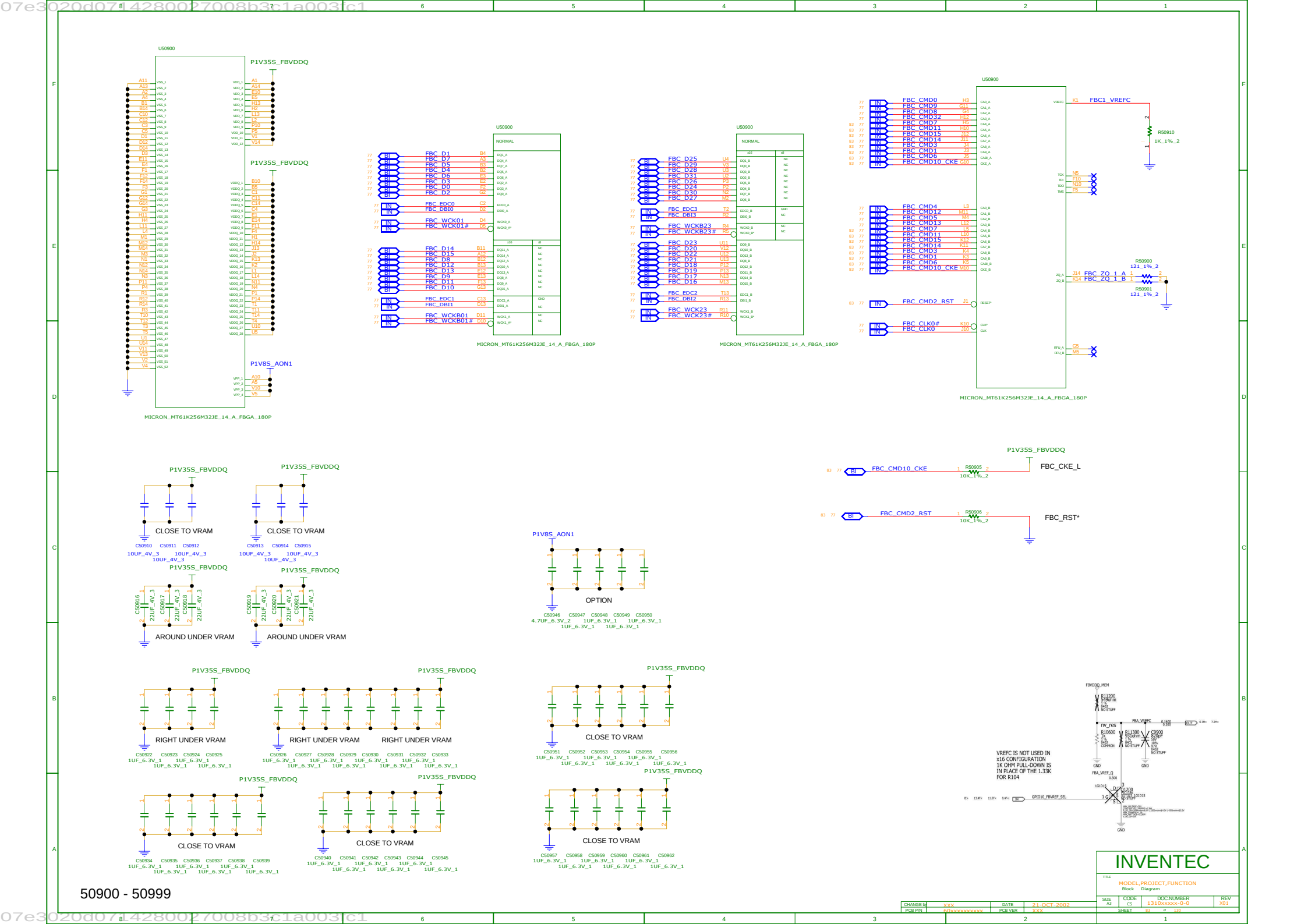
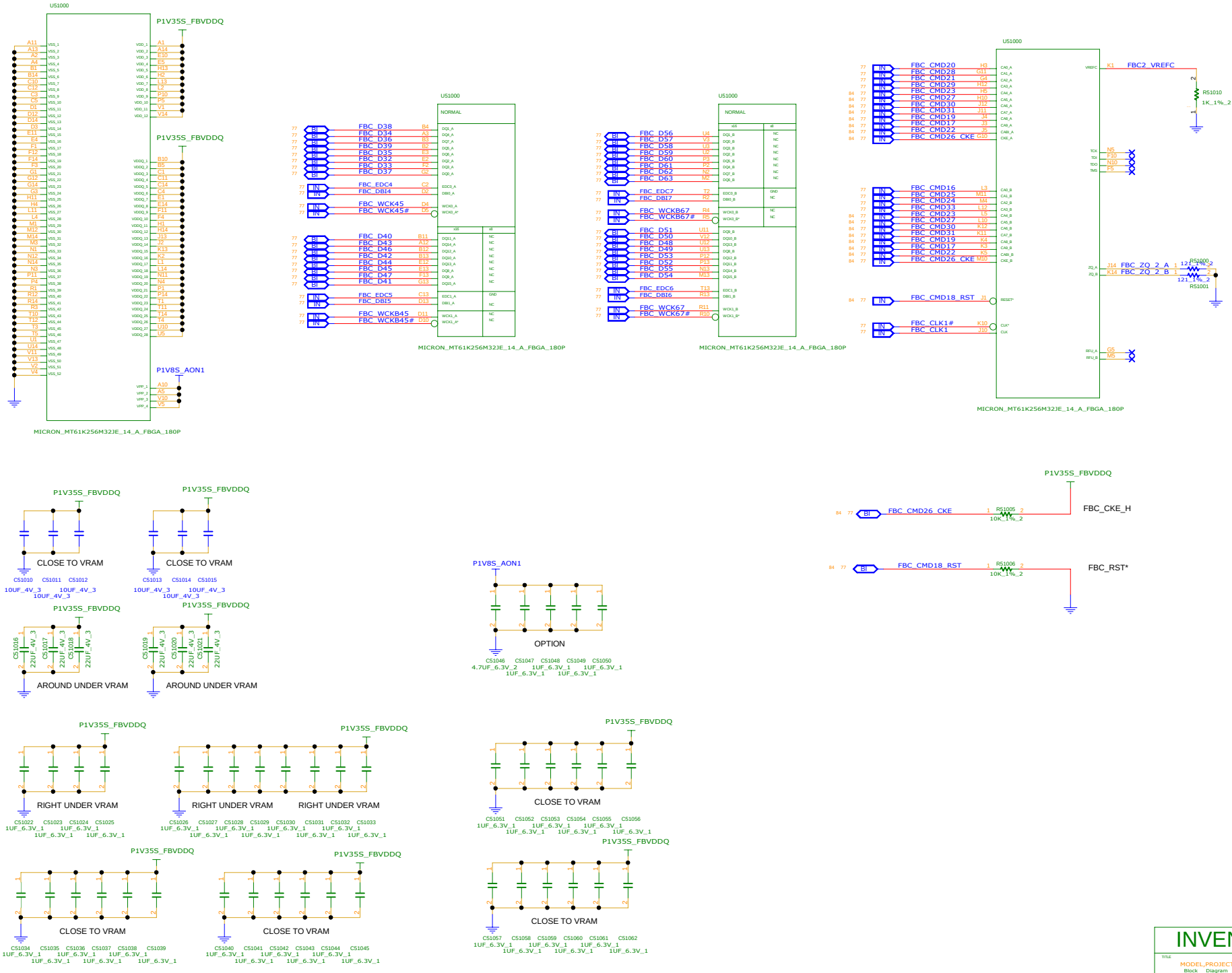

U50900
P1V35S_FBVDDQ
P1V8S_AON1
MICRON_MT61K256M32JE_14_A_FBGA_180P
FBC_D1
FBC_D7
FBC_D5
FBC_D4
FBC_D6
FBC_D3
FBC_D0
FBC_D2
FBC_EDC0
FBC_DBI0
FBC_WCK01
FBC_WCK01#
FBC_D14
FBC_D15
FBC_D8
FBC_D12
FBC_D13
FBC_D9
FBC_D11
FBC_D10
FBC_EDC1
FBC_DBI1
FBC_WCKB01
FBC_WCKB01#
FBC_D25
FBC_D29
FBC_D28
FBC_D31
FBC_D26
FBC_D24
FBC_D30
FBC_D27
FBC_EDC3
FBC_DBI3
FBC_WCKB23
FBC_WCKB23#
FBC_D23
FBC_D20
FBC_D22
FBC_D21
FBC_D18
FBC_D19
FBC_D17
FBC_D16
FBC_EDC2
FBC_DBI2
FBC_WCK23
FBC_WCK23#
FBC_CMD0
FBC_CMD9
FBC_CMD8
FBC_CMD32
FBC_CMD7
FBC_CMD11
FBC_CMD15
FBC_CMD14
FBC_CMD3
FBC_CMD1
FBC_CMD6
FBC_CMD10_CKE
FBC_CMD4
FBC_CMD12
FBC_CMD5
FBC_CMD13
FBC_CMD7
FBC_CMD11
FBC_CMD15
FBC_CMD14
FBC_CMD3
FBC_CMD1
FBC_CMD6
FBC_CMD10_CKE
FBC_CMD2_RST
FBC_CLK0#
FBC_CLK0
FBC1_VREFC
R50910
1K_1%_2
R50900
121_1%_2
R50901
121_1%_2
FBC_ZQ_1_A
FBC_ZQ_1_B
CLOSE TO VRAM
C50910 C50911 C50912
10UF_4V_3 10UF_4V_3
10UF_4V_3
C50913 C50914 C50915
10UF_4V_3 10UF_4V_3
10UF_4V_3
AROUND UNDER VRAM
C50916 C50917 C50918
22UF_4V_3
C50919 C50920 C50921
22UF_4V_3
OPTION
C50946 C50947 C50948 C50949 C50950
4.7UF_6.3V_2 1UF_6.3V_1 1UF_6.3V_1
1UF_6.3V_1 1UF_6.3V_1
RIGHT UNDER VRAM
C50922 C50923 C50924 C50925
1UF_6.3V_1 1UF_6.3V_1
1UF_6.3V_1 1UF_6.3V_1
C50926 C50927 C50928 C50929 C50930 C50931 C50932 C50933
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
CLOSE TO VRAM
C50951 C50952 C50953 C50954 C50955 C50956
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
C50934 C50935 C50936 C50937 C50938 C50939
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
C50940 C50941 C50942 C50943 C50944 C50945
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
C50957 C50958 C50959 C50960 C50961 C50962
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
1UF_6.3V_1 1UF_6.3V_1 1UF_6.3V_1
FBC_CKE_L
FBC_RST*
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104
GPIO10_FBVREF_SEL
50900 - 50999
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
DOC NUMBER
1310xxxxx-D-D
SHEET


U51000
P1V35S_FBVDDQ
P1V8S_AON1
MICRON_MT61K256M32JE_14_A_FBGA_180P
FBC_D38
FBC_D34
FBC_D36
FBC_D39
FBC_D35
FBC_D32
FBC_D33
FBC_D37
FBC_EDC4
FBC_DBI4
FBC_WCK45
FBC_WCK45#
FBC_D40
FBC_D43
FBC_D46
FBC_D42
FBC_D44
FBC_D45
FBC_D47
FBC_D41
FBC_EDC5
FBC_DBI5
FBC_WCK845
FBC_WCK845#
FBC_D56
FBC_D57
FBC_D58
FBC_D59
FBC_D60
FBC_D61
FBC_D62
FBC_D63
FBC_EDC7
FBC_DBI7
FBC_WCKB67
FBC_WCKB67#
FBC_D51
FBC_D50
FBC_D48
FBC_D49
FBC_D53
FBC_D52
FBC_D55
FBC_D54
FBC_EDC6
FBC_DBI6
FBC_WCK67
FBC_WCK67#
FBC_CMD20
FBC_CMD28
FBC_CMD21
FBC_CMD29
FBC_CMD23
FBC_CMD27
FBC_CMD30
FBC_CMD31
FBC_CMD19
FBC_CMD17
FBC_CMD22
FBC_CMD26_CKE
FBC_CMD16
FBC_CMD25
FBC_CMD24
FBC_CMD33
FBC_CMD23
FBC_CMD27
FBC_CMD30
FBC_CMD31
FBC_CMD19
FBC_CMD17
FBC_CMD22
FBC_CMD26_CKE
FBC_CMD18_RST
FBC_CLK1#
FBC_CLK1
FBC2_VREFC
R51010
1K_1%_2
FBC_ZQ_2_A
FBC_ZQ_2_B
R51000
121_1%_2
R51001
CLOSE TO VRAM
AROUND UNDER VRAM
RIGHT UNDER VRAM
OPTION
FBC_CKE_H
FBC_RST*
R51006
10K_1%_2
51000 - 51099
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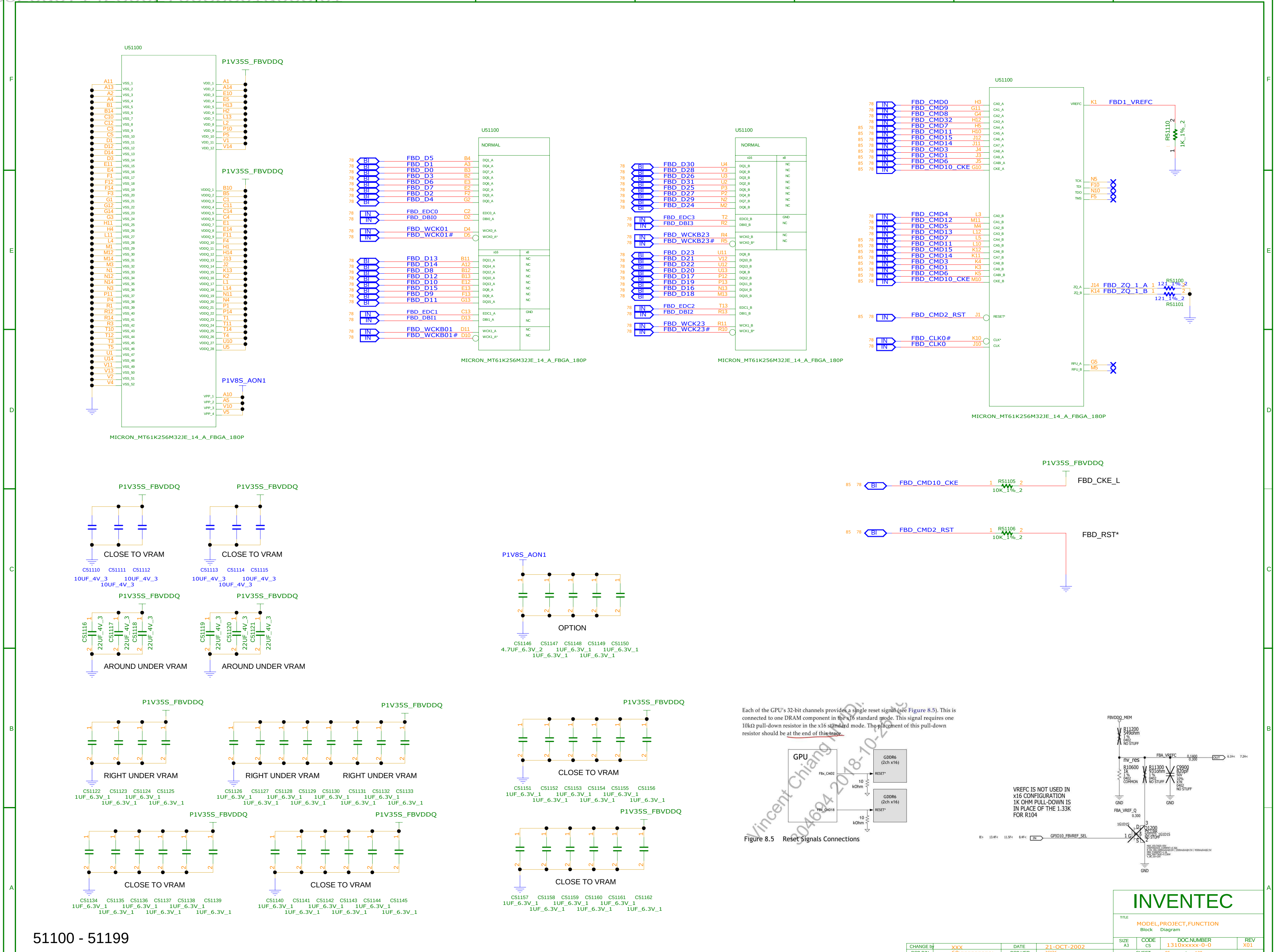
MODEL,PROJECT,FUNCTION
Block Diagram
DOC.NUMBER
1310xxxxx-D-D
21-OCT-2002



Each of the GPU's 32-bit channels provides a single reset signal (see Figure 8.5). This is connected to one DRAM component in the x16 standard mode. This signal requires one 10kΩ pull-down resistor in the x16 standard mode. The placement of this pull-down resistor should be at the end of this trace.

Figure 8.5 Reset Signals Connections

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION — Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	CODE	DOC.NUMBER	REV
PCB P/N	60XXXXXXXXXX	PCB VER	XXX	A3	CS	1310xxxx-0-0	X01

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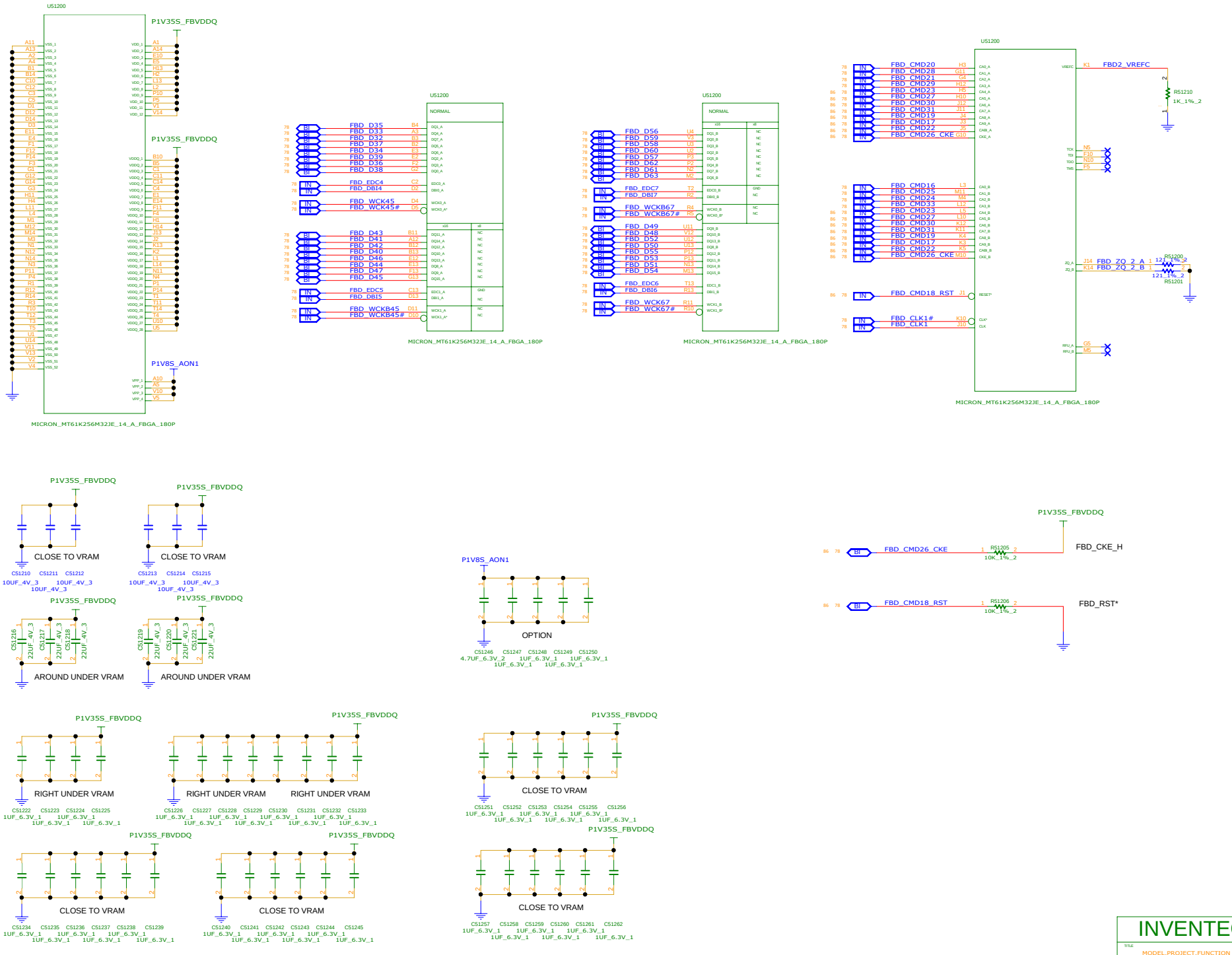
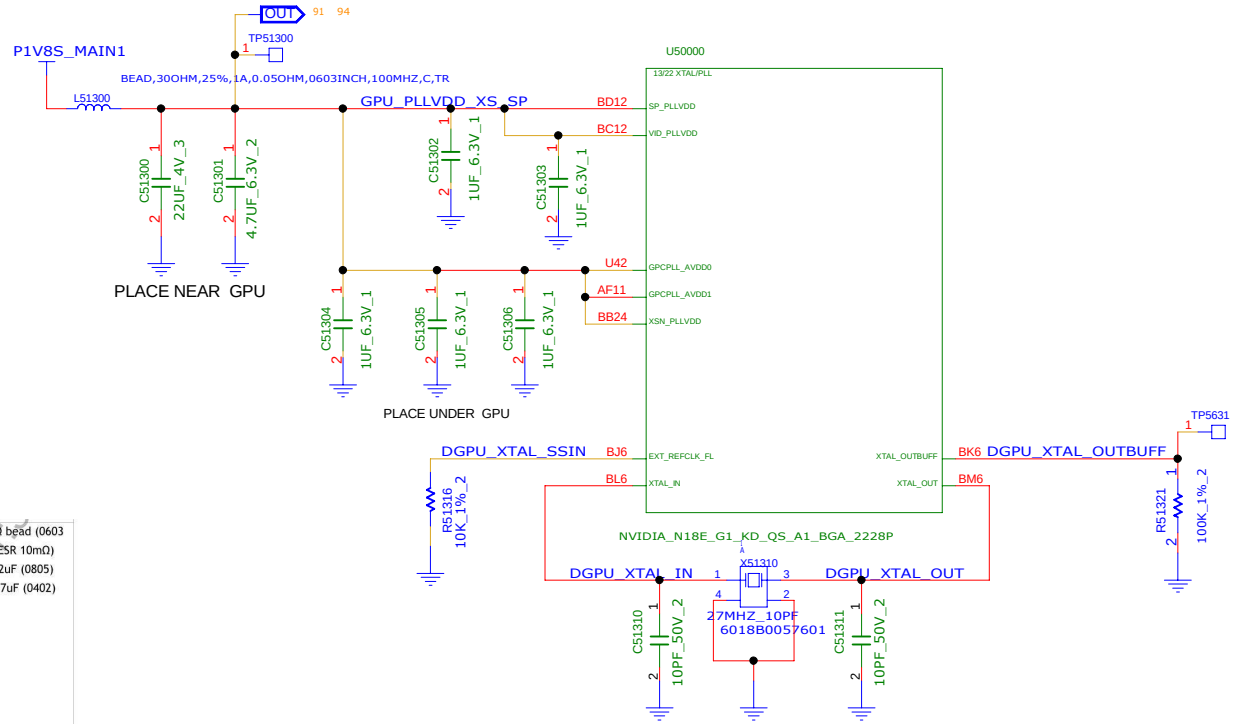

U51200
P1V35S_FBVDDQ
P1V8S_AON1
MICRON_MT61K256M32JE_14_A_FBGA_180P
NORMAL
FBD_D35
FBD_D33
FBD_D32
FBD_D37
FBD_D34
FBD_D39
FBD_D36
FBD_D38
FBD_EDC4
FBD_DBI4
FBD_WCK45
FBD_WCK45#
FBD_D43
FBD_D41
FBD_D42
FBD_D40
FBD_D46
FBD_D44
FBD_D47
FBD_D45
FBD_EDC5
FBD_DBI5
FBD_WCKB45
FBD_WCKB45#
FBD_D56
FBD_D59
FBD_D58
FBD_D60
FBD_D57
FBD_D62
FBD_D61
FBD_D63
FBD_EDC7
FBD_DBI7
FBD_WCKB67
FBD_WCKB67#
FBD_D49
FBD_D48
FBD_D52
FBD_D50
FBD_D55
FBD_D53
FBD_D51
FBD_D54
FBD_EDC6
FBD_DBI6
FBD_WCK67
FBD_WCK67#
FBD_CMD20
FBD_CMD28
FBD_CMD21
FBD_CMD29
FBD_CMD23
FBD_CMD27
FBD_CMD30
FBD_CMD31
FBD_CMD19
FBD_CMD17
FBD_CMD22
FBD_CMD26_CKE
FBD_CMD16
FBD_CMD25
FBD_CMD24
FBD_CMD33
FBD_CMD23
FBD_CMD27
FBD_CMD30
FBD_CMD31
FBD_CMD19
FBD_CMD17
FBD_CMD22
FBD_CMD26_CKE
FBD_CMD18_RST
FBD_CLK1#
FBD_CLK1
FBD2_VREFC
R51210
1K_1%_2
FBD_ZQ_2_A
FBD_ZQ_2_B
R51200
121_1%_2
R51201
FBD_CMD26_CKE
R51205
10K_1%_2
FBD_CKE_H
FBD_CMD18_RST
R51206
10K_1%_2
FBD_RST*
CLOSE TO VRAM
AROUND UNDER VRAM
OPTION
RIGHT UNDER VRAM
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
51200 - 51299

27 MHZ XTAL



CL=2*10-(5+3)=12

$CL\_trim = 2 \times CLoad - (Cstray + Ci)$

Where:

- C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
- C_{stray} is ~ 3pF (Stray capacitance of XTAL pads and any significant trace routing)
- C_i is pin capacitance (5 pF)

Typical CL_trim = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10mΩ) 1 x 22uF (0805) 1 x 4.7uF (0402)
IFPCD_PLLVDD	1			
IFPEF_PLLVDD	1		Alternate solution: 3 x 1.0uF (0201W X6S)	
GPCPLL_AVDDx XSN_PLLVDD	3		3 x 0.47uF (0201W X6S) Alternate solution: 3 x 1.0uF (0201W X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	

51300 - 51399

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 87 of 130	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

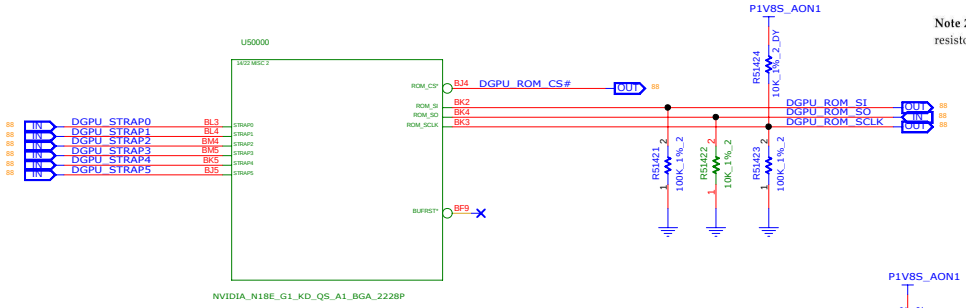
GPU VBIOS, EXTERNAL STRAPS

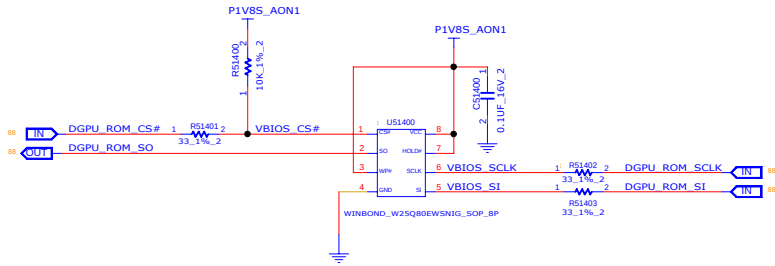
Table 12.4 FS_OVERT* Strap Enablement

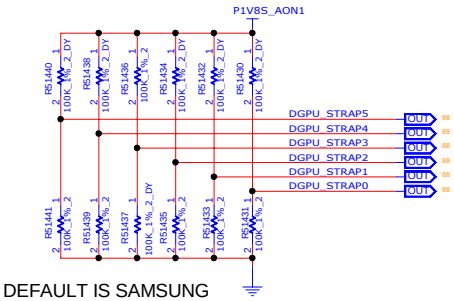
Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.







DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14
6019B1847601
STRAP 0X0=000
SAMSUNG:R51431 STUFF
R51430 NOT STUFF

MICRON MT61K256M32JE-14:A
6019B1847701
STRAP 0X1=001
MICRON :R51430 STUFF
R51431 NOT STUFF

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	M		1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1
H	L	M				
H	M	L				
H	M	H				
H	H	M				
L	M	M				
M	L	M				
M	M	L				
M	M	H				
M	H	M				
H	M	M				
M	M	M				

Reserved

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[1]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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GPU GPIO

Table 7.1 Thermal Specifications

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
Thermal Resistance (Junction to Case, R_{JC})	0.014	0.017	0.017	TBD	°C/W
Thermal Resistance (Junction to PCB Board, R_{JB})	0.64	0.96	0.96	TBD	°C/W
GPU Shutdown Temperature (OVERT) [1]	99	99	99	TBD	°C
GPU Slowdown Temperature (THERM_ALERT) [2]	94	94	94	TBD	°C

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
GPU Maximum Operating Temperature [3]	89	89	89	TBD	°C
GPU Target Temperature	87 (Default) 75 (Min)	87 (Default) 75 (Min)	87 (Default) 75 (Min)	TBD	°C

Notes:
1. OVERT results in an 87.5% (±8) hardware clock slowdown.
2. THERM_ALERT results in a 50% (±2) hardware clock slowdown.
3. The GPU maximum operating temperature is the maximum GPU temperature at which the GPU is guaranteed to operate at the target performance (base clocks) under the total board power level.

OVERT#
3.3V LEVEL

3.3V LEVEL OVERHEAT TO EC

13.3.2.1 I2CS Slave Addre

The default I2CS address is (0x9E)

NVIDIA_N18E_G1_KD_QS_A1_BGA_2228P

HPD PULL UP

GPIO PULL UP

GPIO PULL DOWN

GC6_FB_EN
LEVEL SHIFTER

1.8V LEVEL

3.3V LEVEL

GC6_FB_EN
LEVEL SHIFTER

1.8V LEVEL

3.3V LEVEL

53900 - 54199

51500 - 51599

INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

CHANGE ID	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-D	X01

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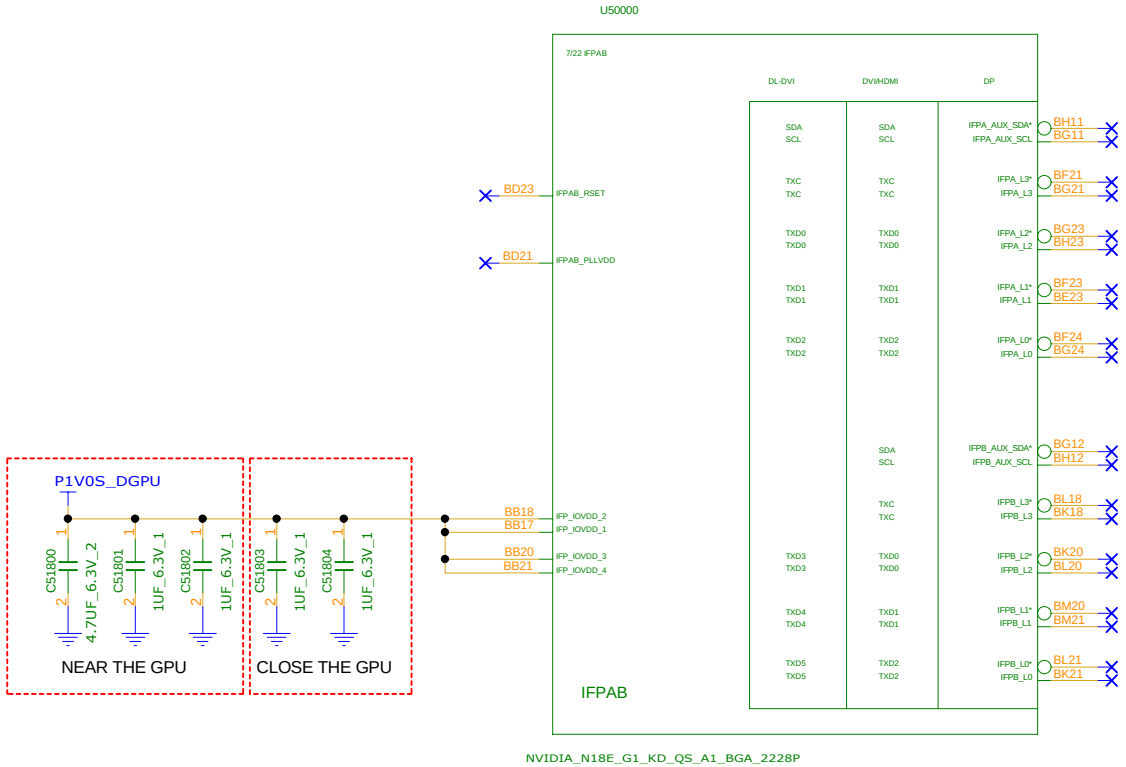
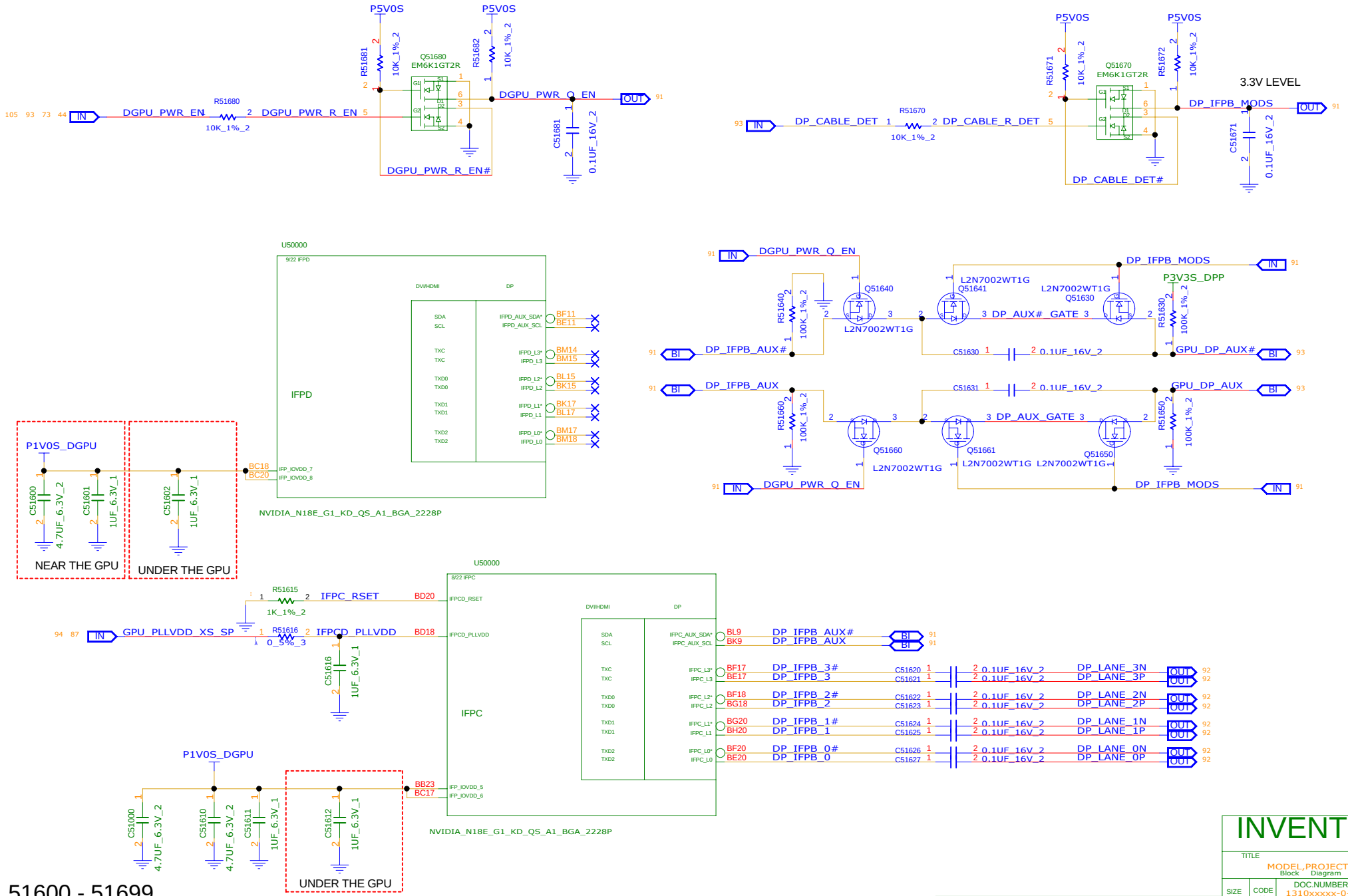


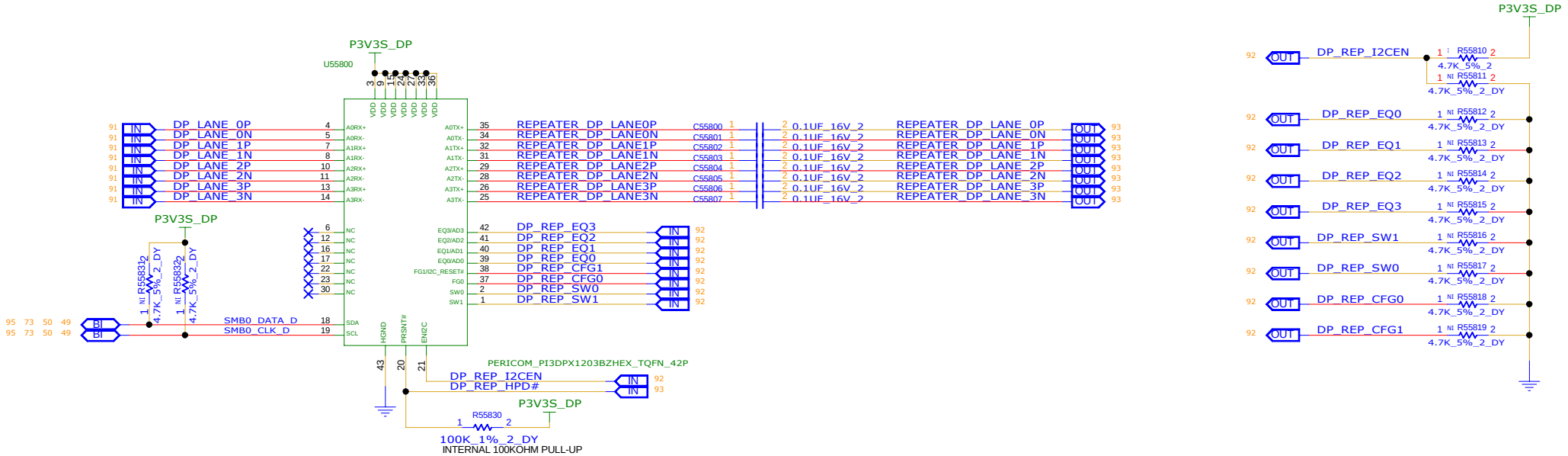
51800 - 51899

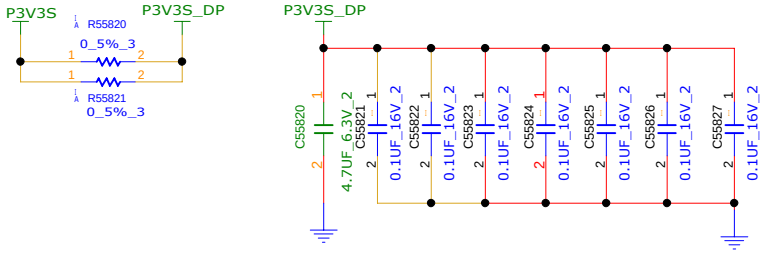
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	
SHEET 90 of 130			



DP REDRIVER





55800 - 55999 56000 - 56199

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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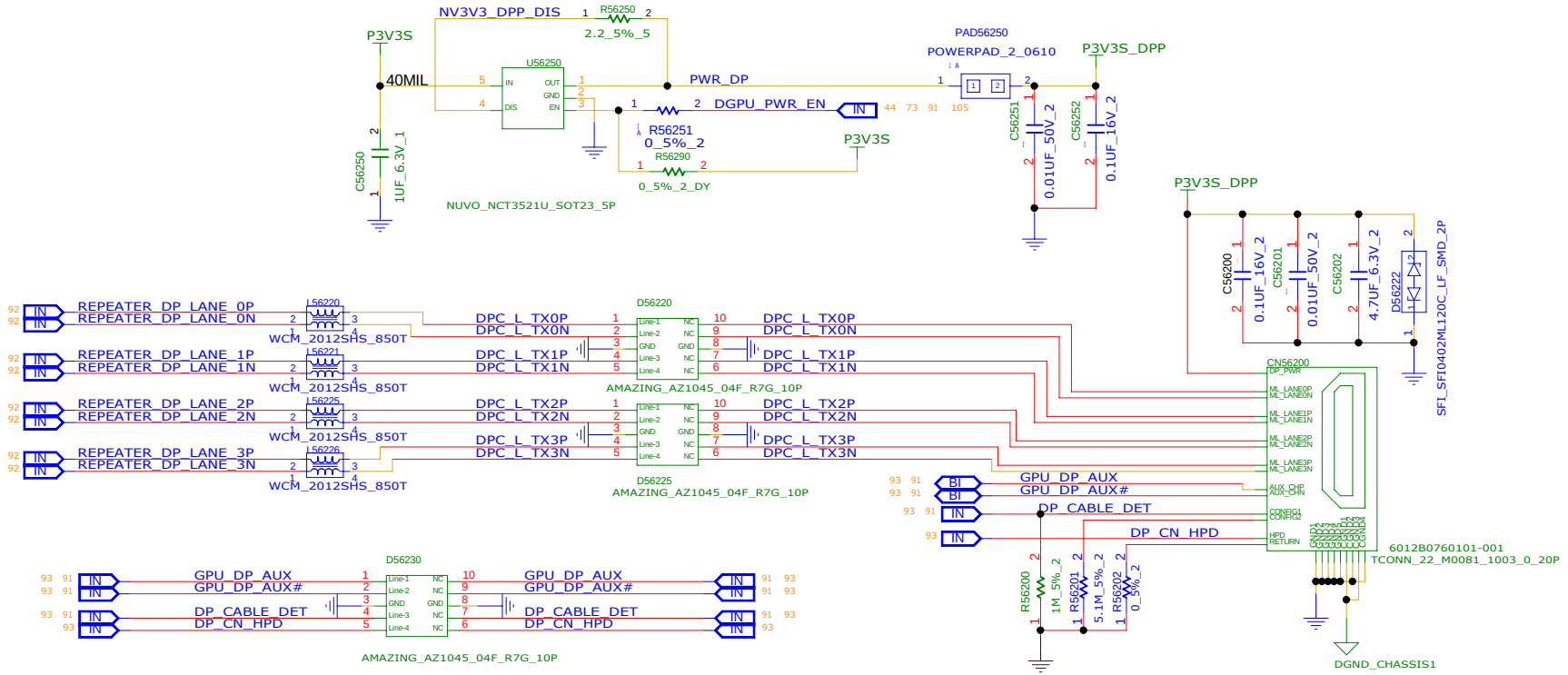

56200 - 56399

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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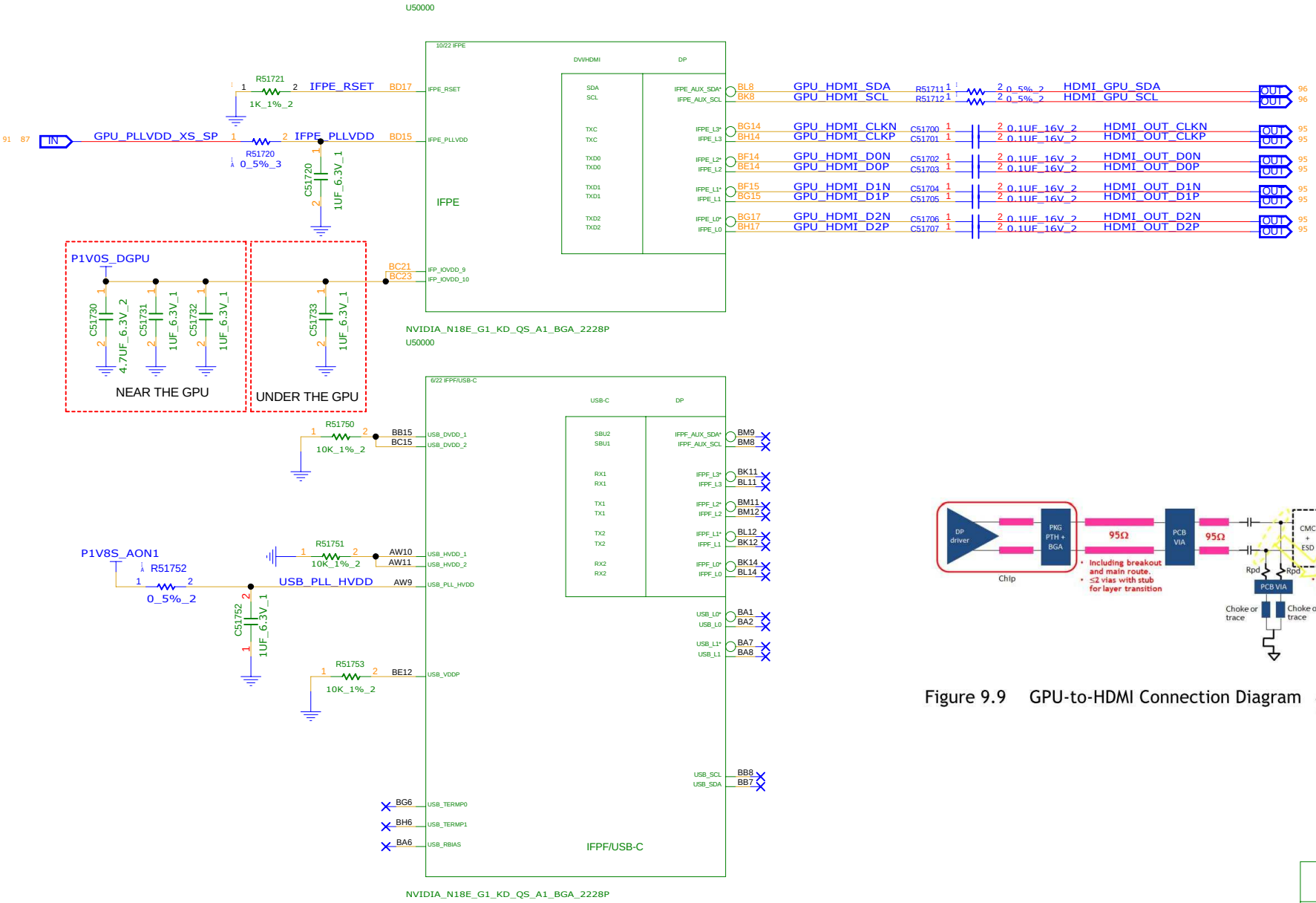

Figure 9.9 GPU-to-HDMI Connection Diagram

51700 - 51799

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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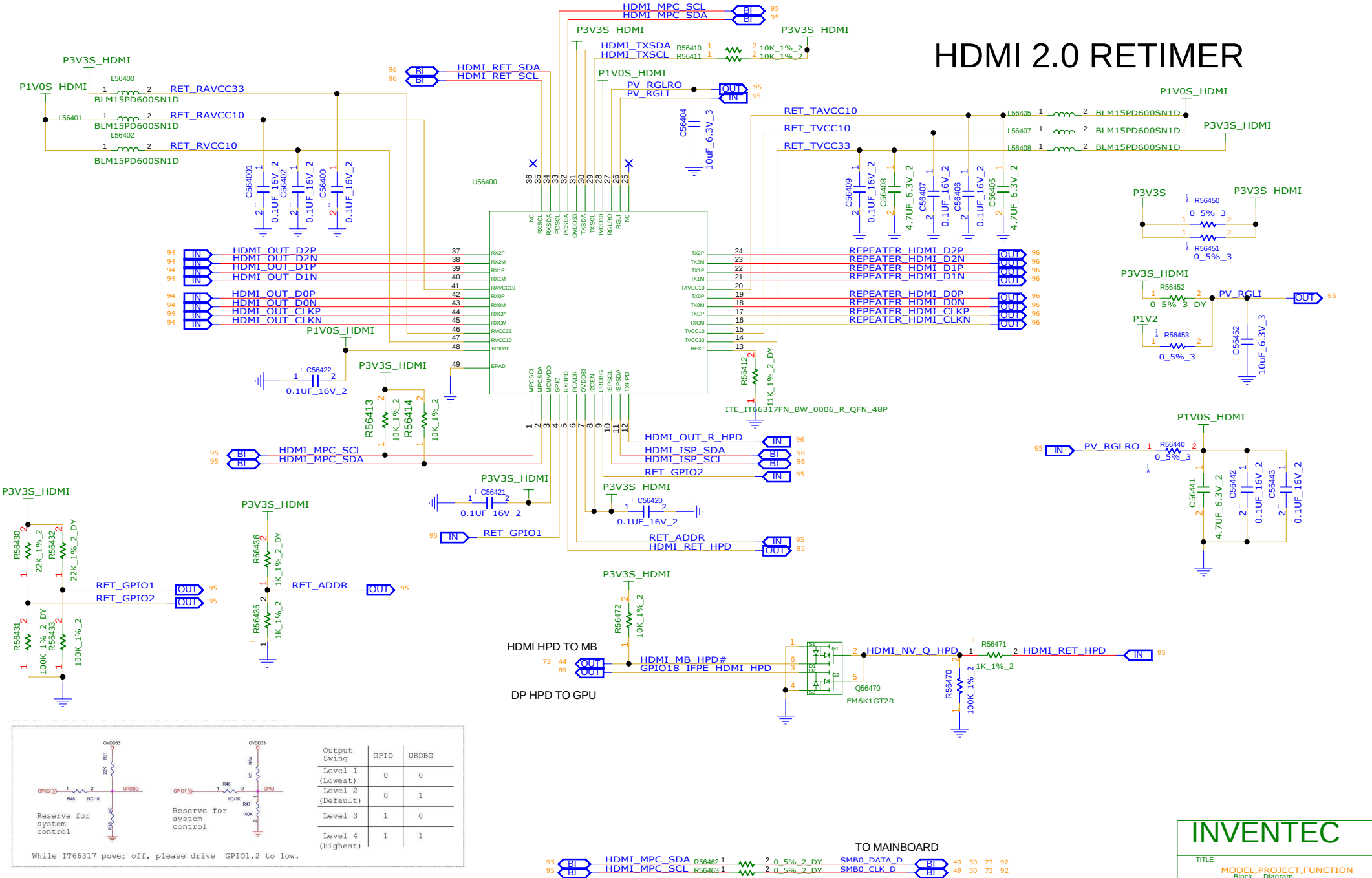
HDMI 2.0 RETIMER

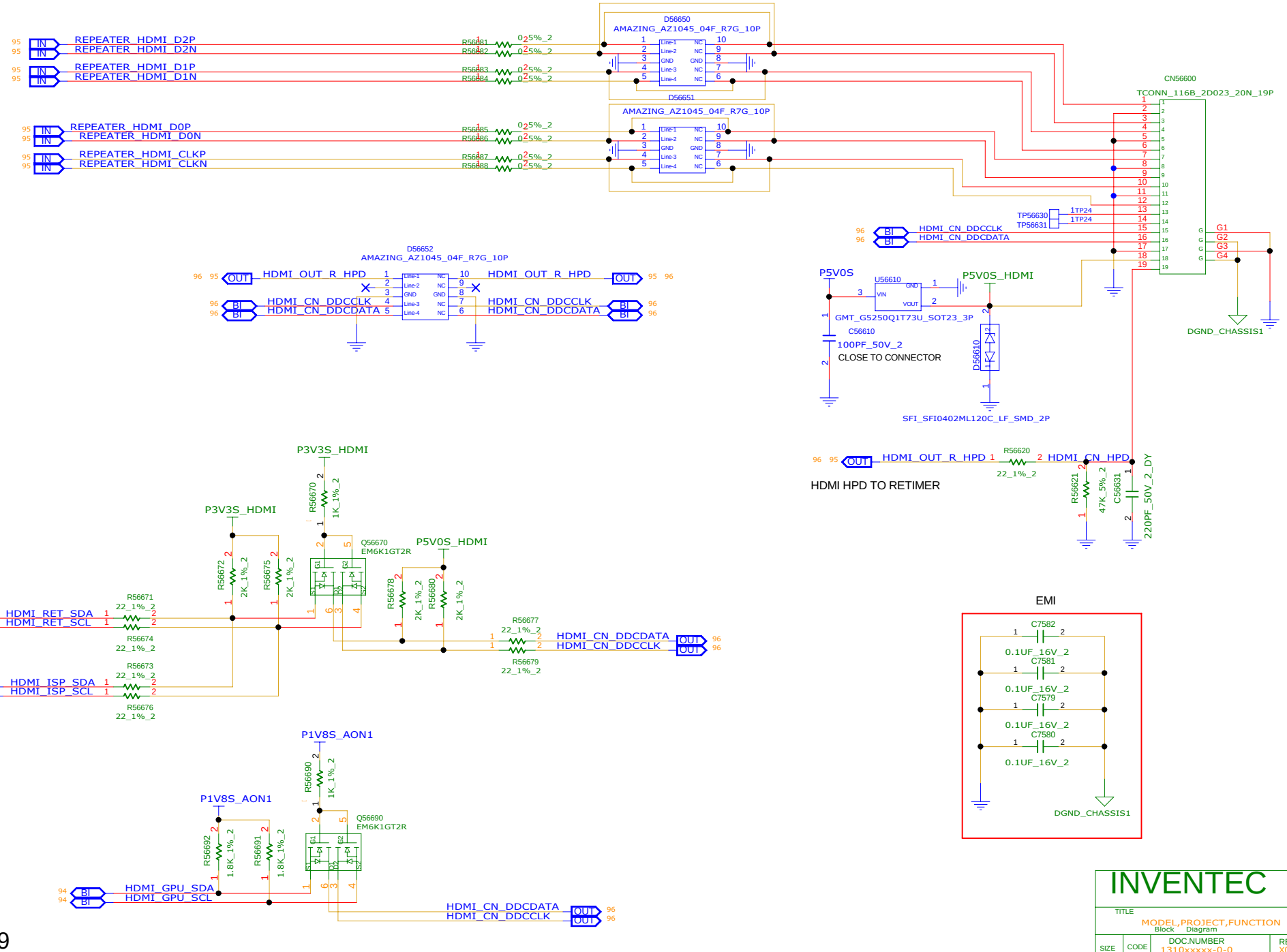


Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

56400 - 56599

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxx		PCB VER XXX	
SHEET 95 of 130			



56600 - 56799

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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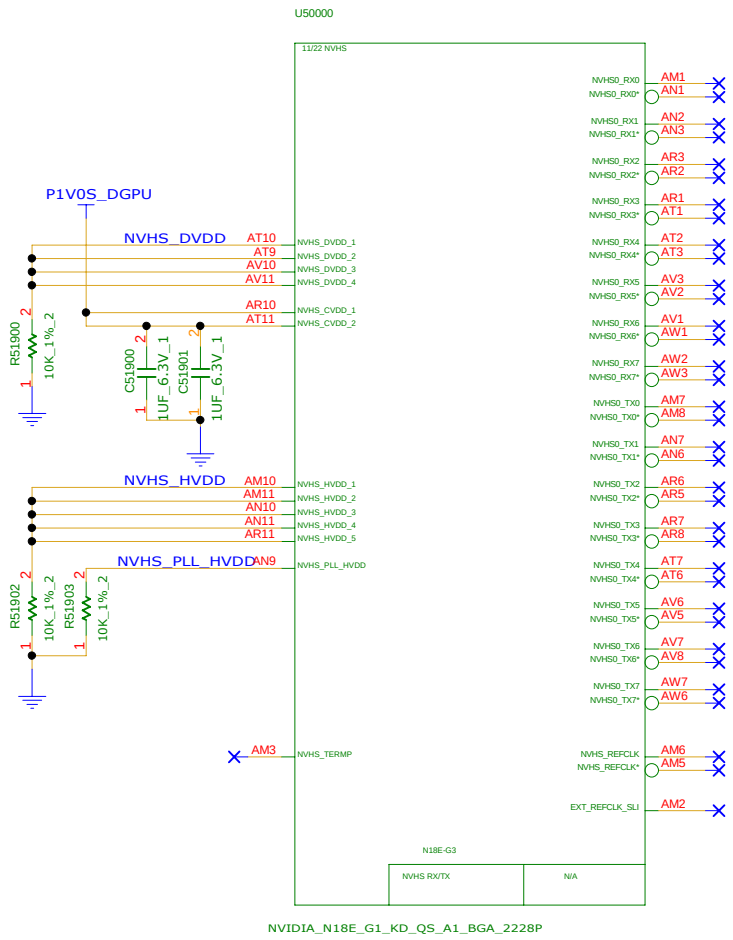

51900 - 51999

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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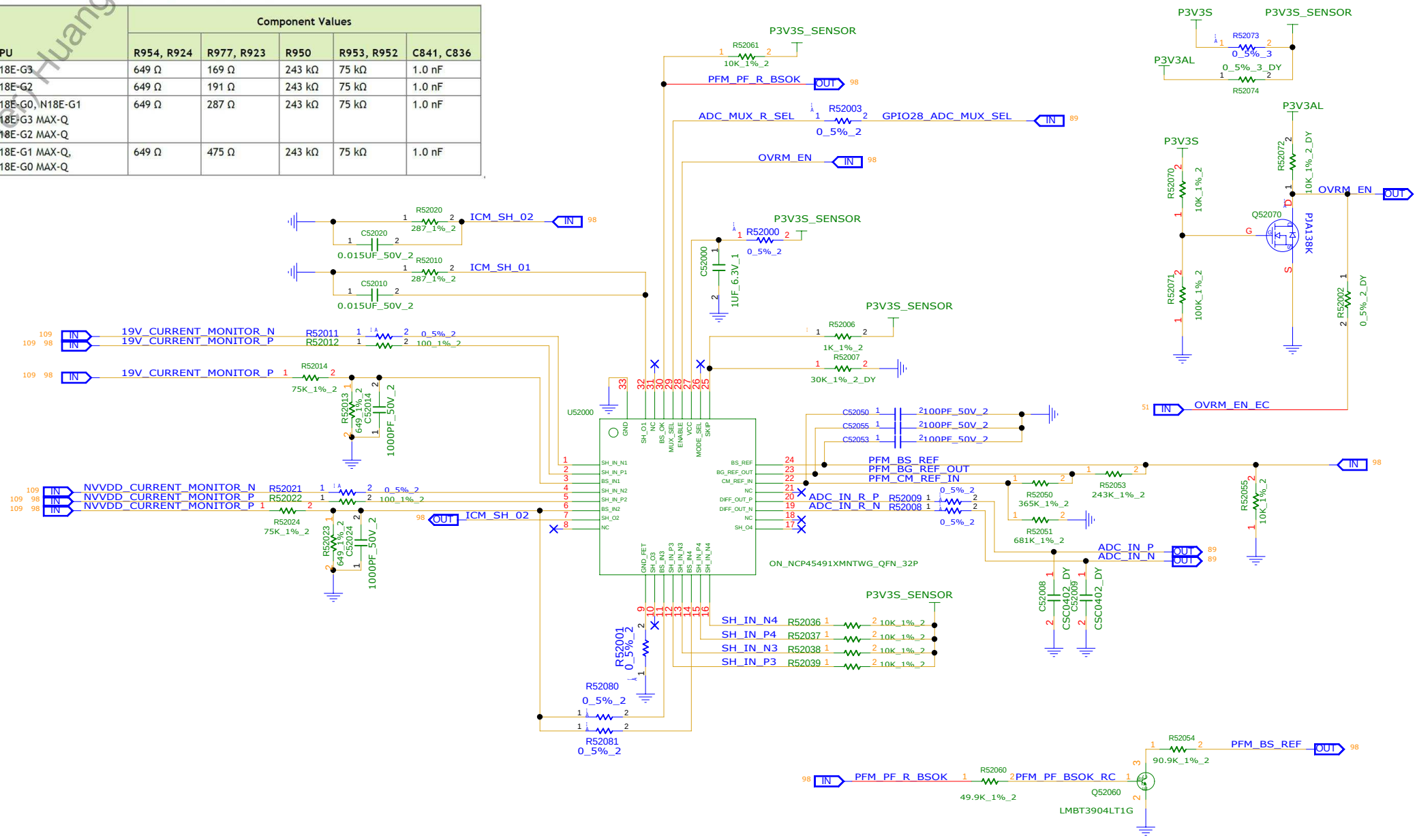
Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G2	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G0, N18E-G1 N18E-G3 MAX-Q N18E-G2 MAX-Q	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G1 MAX-Q, N18E-G0 MAX-Q	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF



52000 - 52099

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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The required subcircuit is shown in detail in Figure 15.6.

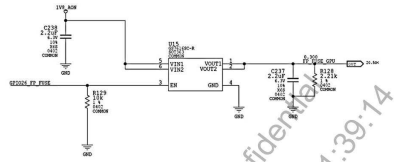
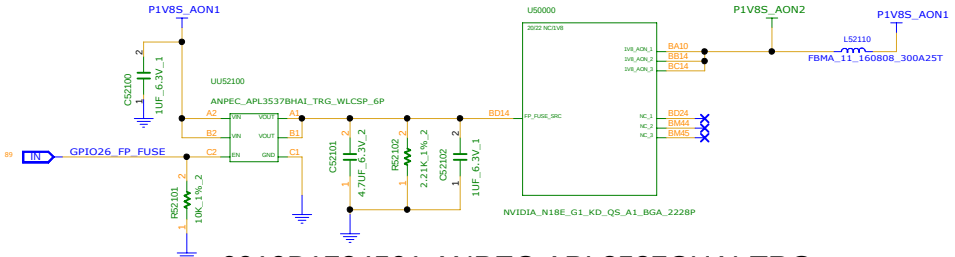


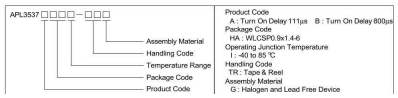
Figure 15.6 Subcircuit Schematic

In Figure 15.6, the component labeled "U15" is an active switch; devices equivalent to the G576165C-R are acceptable as long as they meet the following requirements:

- The active switch must be capable of driving 100mA or more.
- The timing delay from GPIO26_FP_FUSE assertion to FP_FUSE_GPU (active switch output) must be 100msec or less.
- There must be no glitch during power up or CG6/GC-OFF entry or exit.
- The FP_FUSE_GPU (output) trace width must be 0.25 mm (10 mil) or greater.



6019B1724501 ANPEC APL3537CHAI-TRG



52100 - 52199

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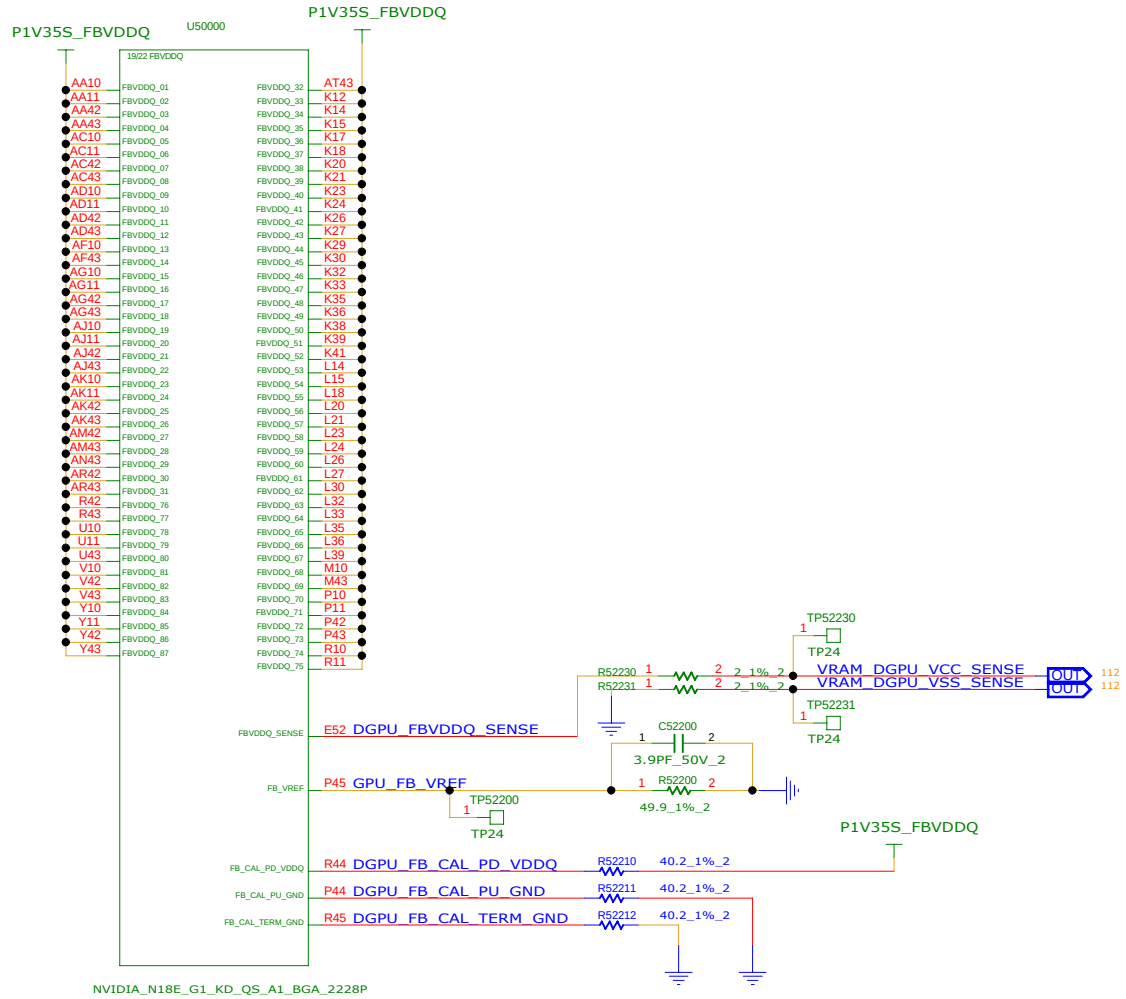

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52200 - 52299

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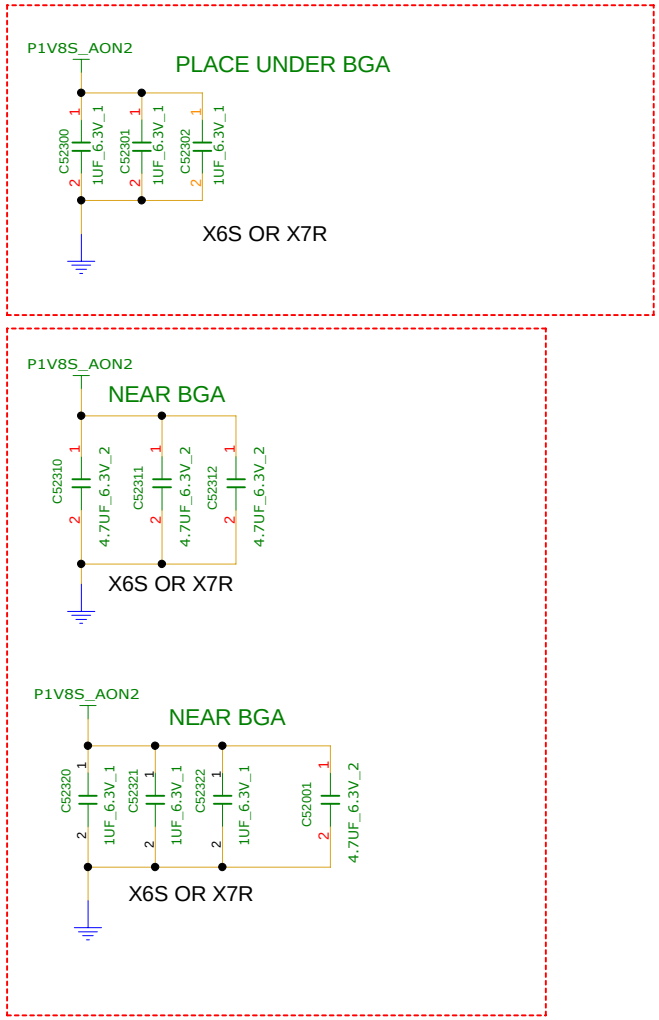
GPU 1V8_AON DECOUPLING



1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S) 3 x 1uF (0402 X6S) 3 x 4.7uF (0603 X6S) --- Alternate solution: 3 x 1.0uF (0201W X6S)

52300 - 52399

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SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV X01

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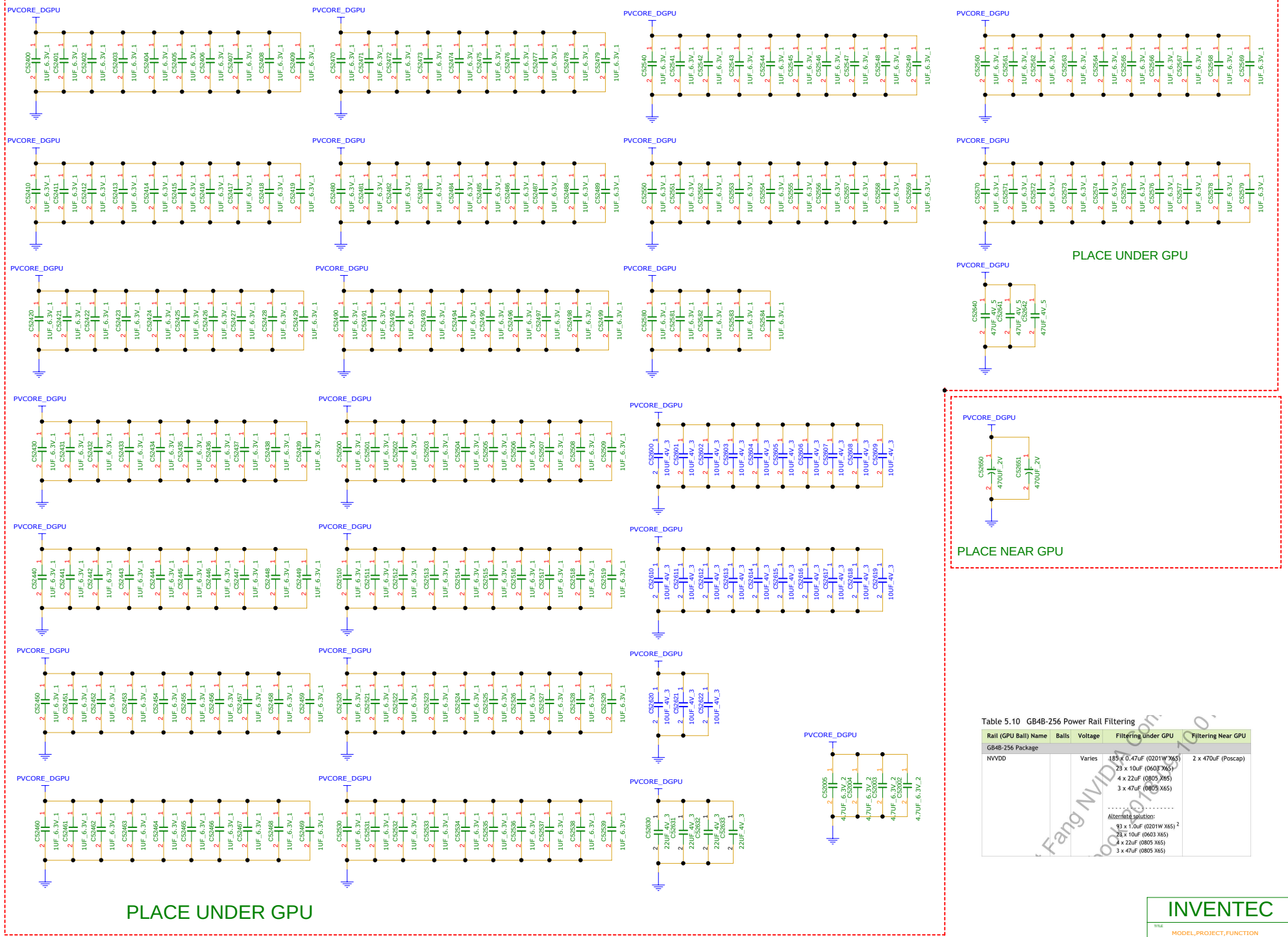

Table 5.10 GB4B-256 Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 x 0.47uF (0201W X6S) 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S) --- Alternate solution: 93 x 1.0uF (0201W X6S) [2] 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S)	2 x 470uF (Poscap)

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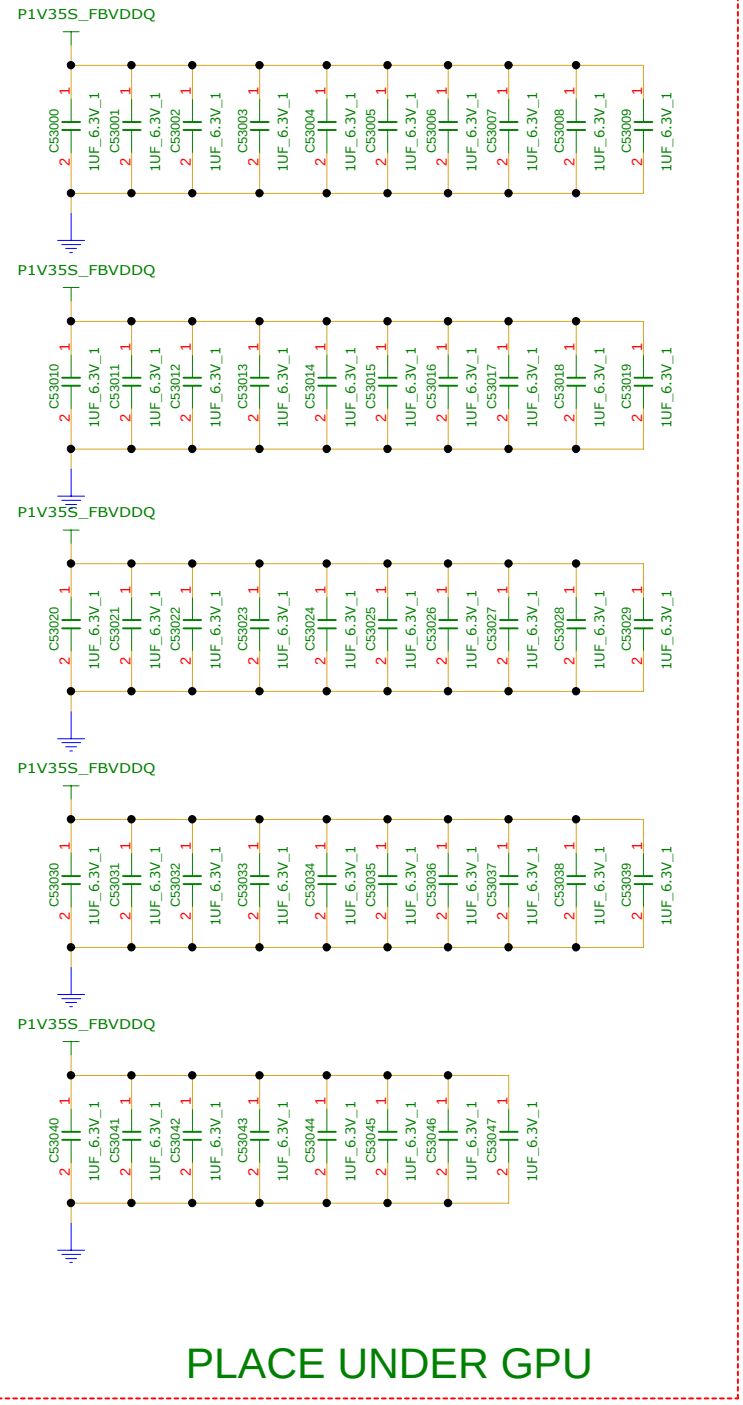
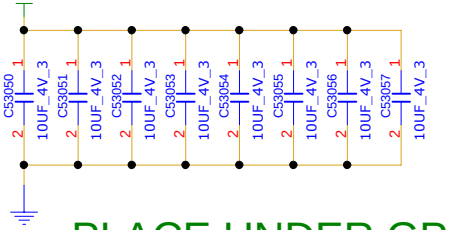
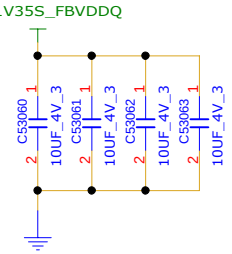


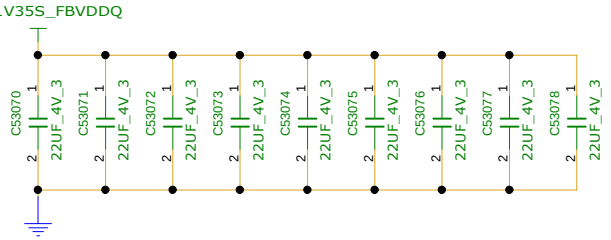
PLACE UNDER GPU



PLACE UNDER GPU



PLACE NEAR GPU



FBVDDQ (GPU side)[1]	1.25V 1.35V	48 x 0.47uF (0201W X6S) 8 x 10uF (0603 X6S) - - - - - - - - - - - - - - - - - - Alternate solution: 24 x 1.0uF (0201W X6S)[2] 8 x 10uF (0603 X6S)	4 x 10uF (0603 X6S) 9 x 22uF (0603 X6S)

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CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS
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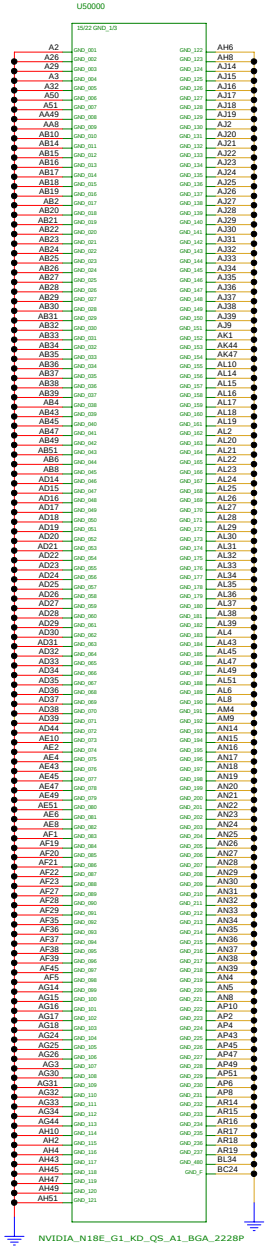
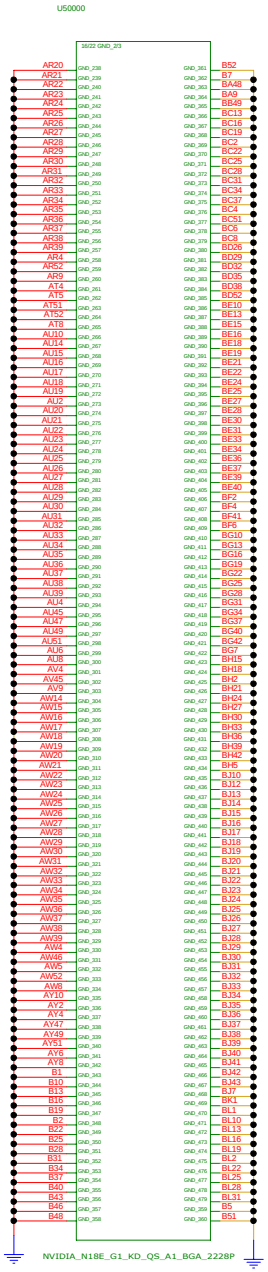
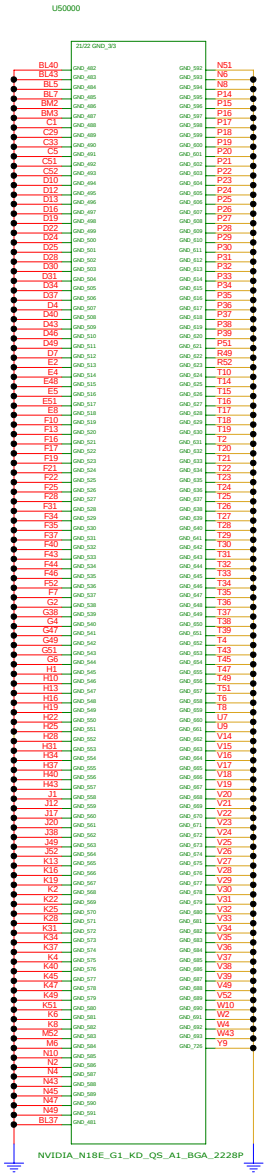
GND







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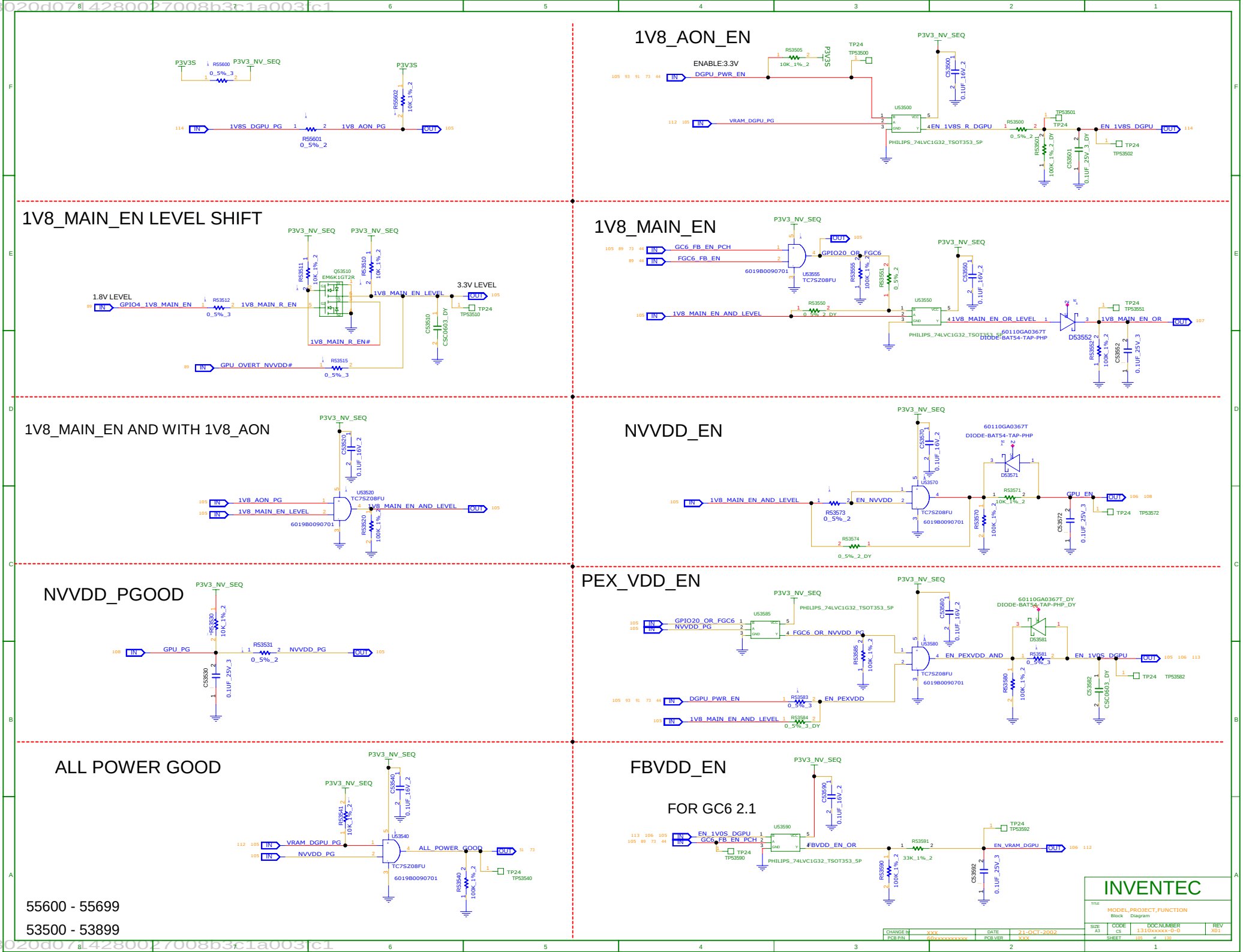
1V8_AON_EN
ENABLE:3.3V
DGPU_PWR_EN
VRAM_DGPU_PG
EN_1V8S_R_DGPU
EN_1V8S_DGPU
1V8S_DGPU_PG
1V8_AON_PG
1V8_MAIN_EN LEVEL SHIFT
1.8V LEVEL
3.3V LEVEL
GPIO4_1V8_MAIN_EN
1V8_MAIN_R_EN
1V8_MAIN_R_EN#
1V8_MAIN_EN_LEVEL
GPU_OVERT_NVVDD#
1V8_MAIN_EN
GC6_FB_EN_PCH
FGC6_FB_EN
GPIO20_OR_FGC6
1V8_MAIN_EN_AND_LEVEL
1V8_MAIN_EN_OR_LEVEL
1V8_MAIN_EN_OR
1V8_MAIN_EN AND WITH 1V8_AON
NVVDD_EN
EN_NVVDD
GPU_EN
NVVDD_PGOOD
GPU_PG
NVVDD_PG
PEX_VDD_EN
GPIO20_OR_FGC6
NVVDD_PG
FGC6_OR_NVVDD_PG
EN_PEXVDD_AND
EN_PEXVDD
DGPU_PWR_EN
1V8_MAIN_EN_AND_LEVEL
ALL POWER GOOD
VRAM_DGPU_PG
NVVDD_PG
ALL_POWER_GOOD
FBVDD_EN
FOR GC6 2.1
EN_1V0S_DGPU
GC6_FB_EN_PCH
FBVDD_EN_OR
EN_VRAM_DGPU
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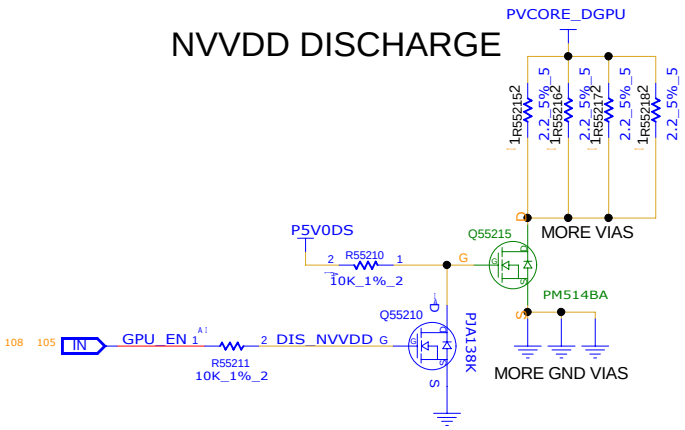
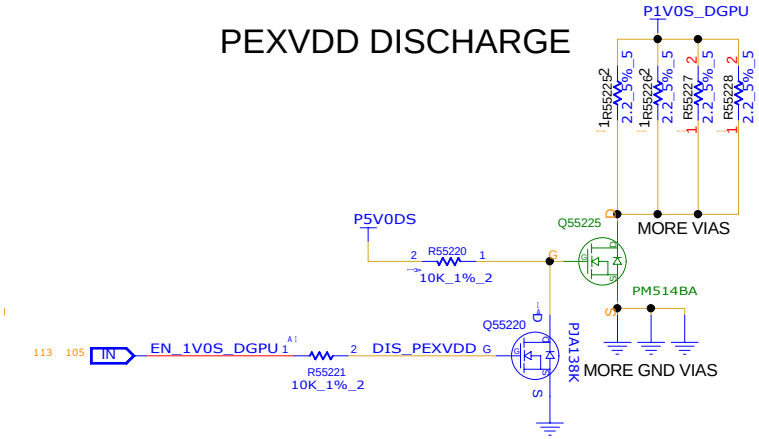
DISCHARGE CIRCUIT

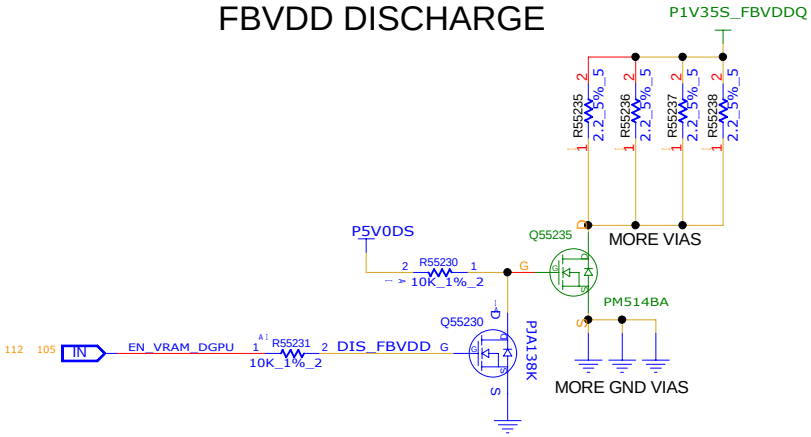
NVVDD DISCHARGE



PEXVDD DISCHARGE



FBVDD DISCHARGE



55200 - 55299

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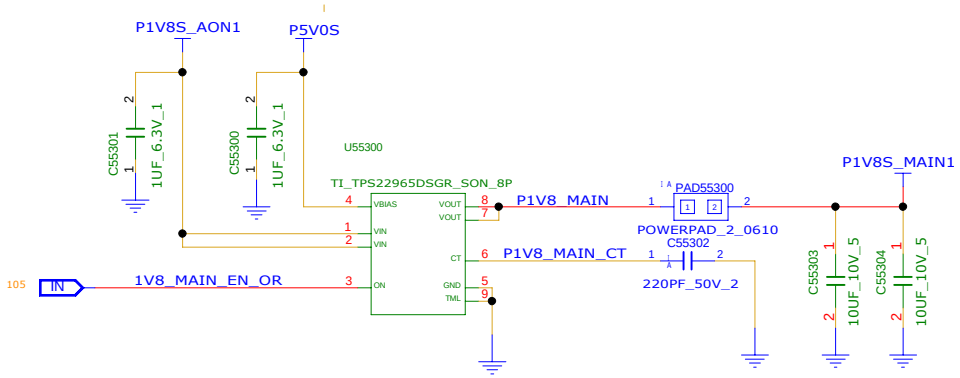
1V8_MAIN



55300 - 55399

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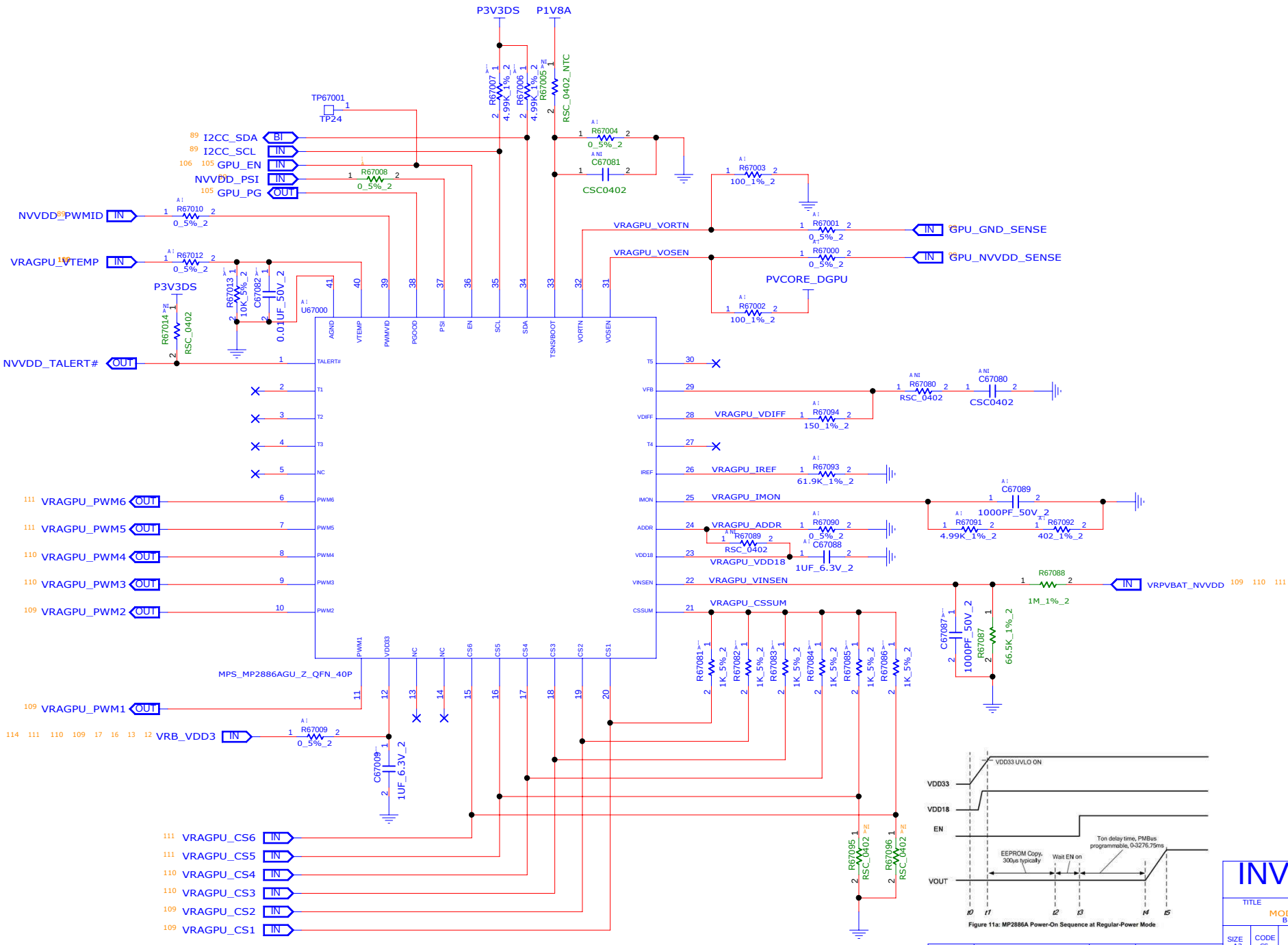

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VRPVBAT_DGPU OUT R67099 PVBAT_IMON IN
0.005_1%_6
OUT 19V_CURRENT_MONITOR_P
OUT 19V_CURRENT_MONITOR_N

VRPVBAT_NVVDD OUT R67199 IN VRPVBAT_DGPU
0.005_1%_6
OUT NVVDD_CURRENT_MONITOR_P
OUT NVVDD_CURRENT_MONITOR_N

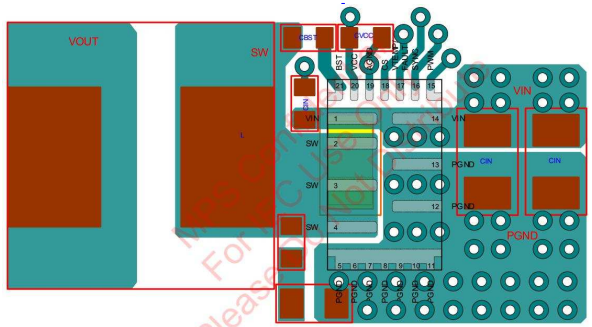
VRB_VDD3 IN
C67019 1UF_6.3V_2
U67010
VRAGPU_PWM1 IN
VRAGPU_VTEMP OUT
VRB_VDD3 IN R67017 2K_5%_2 VRAGPU_SYNC1
VRAGPU_CS1 OUT
VCC AGND PWM VTEP/FLT SYNC CS
VIN1 VIN2 BST SW1 SW2 SW3 PGND9 PGND8 PGND7 PGND6 PGND1 PGND2 PGND3 PGND4 PGND5
MPS_MP86941GQVT_Z_TQFN_21P

VRPVBAT_NVVDD IN
C67010 10UF_25V_5
C67011 10UF_25V_5
C67012 1UF_25V_3
C67013 15UF_25V
1UF CLOSE PIN1
C67015 0.22UF_16V_2
VRPGPU_BST1
VRPGPU_SW1
L67010 TRIO_EM_22BM66V04
R67016 RSC_0603
C67016 CSC0402
C67000 330UF_2V_9MR_PANA_35%
C67090 22UF_6.3V_3
PVCORE_DGPU
TP67000 TP24
IN CORE_PWEN R5001 0_5%_2 Q5001 L2N7002WT1G
PVBAT
Q5000 PMOS_4D3S SYNNEX_SM3303PSQG
R5000 100K_5%_2
PVBAT_IMON OUT

VRB_VDD3 IN
C67029 1UF_6.3V_2
U67020
VRAGPU_PWM2 IN
VRAGPU_VTEMP OUT
VRB_VDD3 IN R67027 2K_5%_2 VRAGPU_SYNC2
VRAGPU_CS2 OUT
VCC AGND PWM VTEP/FLT SYNC CS
VIN1 VIN2 BST SW1 SW2 SW3 PGND9 PGND8 PGND7 PGND6 PGND1 PGND2 PGND3 PGND4 PGND5
MPS_MP86941GQVT_Z_TQFN_21P

VRPVBAT_NVVDD IN
C67020 10UF_25V_5
C67021 10UF_25V_5
C67022 1UF_25V_3
C67023 15UF_25V
1UF CLOSE PIN1
C67025 0.22UF_16V_2
VRPGPU_BST2
VRPGPU_SW2
L67020 TRIO_EM_22BM66V04
R67026 RSC_0603
C67026 CSC0402
C67001 330UF_2V_9MR_PANA_35%
C67091 22UF_6.3V_3
PVCORE_DGPU

PVCORE_DGPU
C67006 330UF_2V_9MR_PANA_35%
C67096 22UF_6.3V_3
C67097 CSC0603



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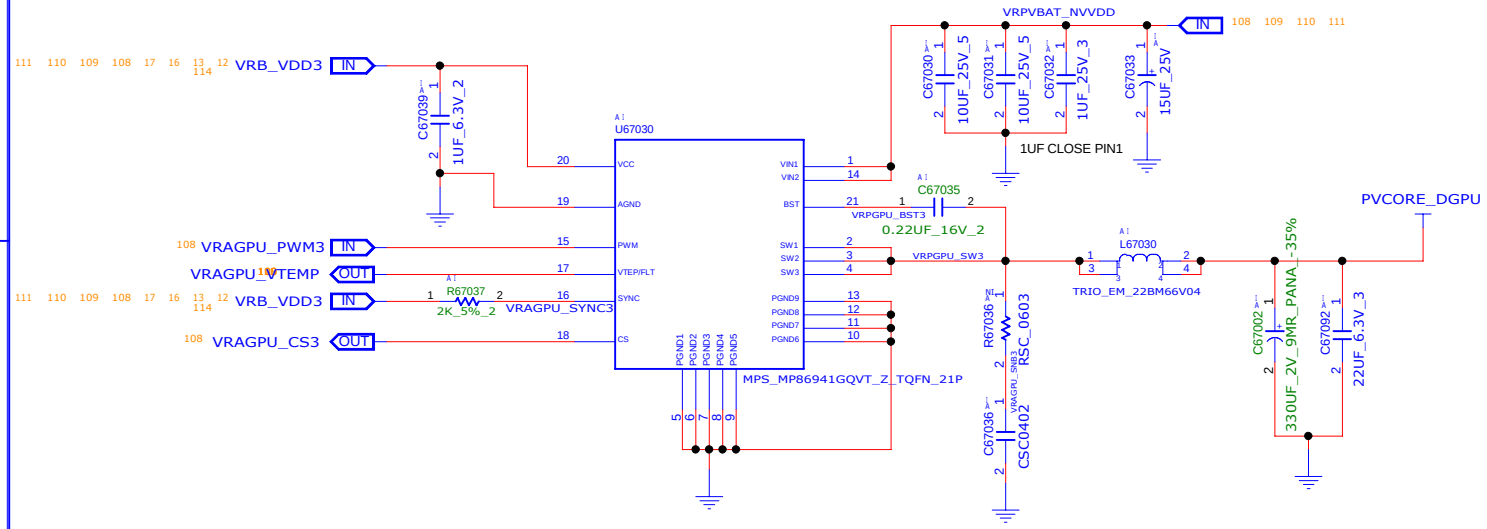

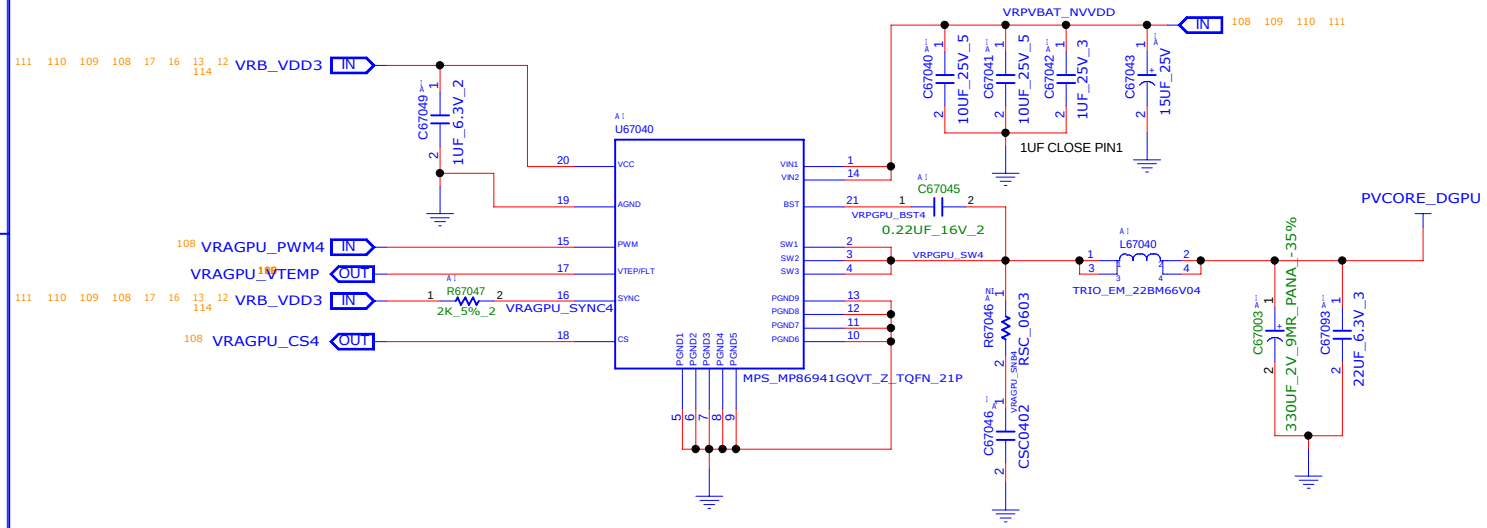

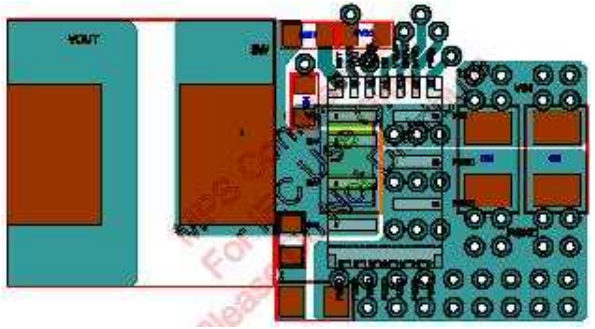

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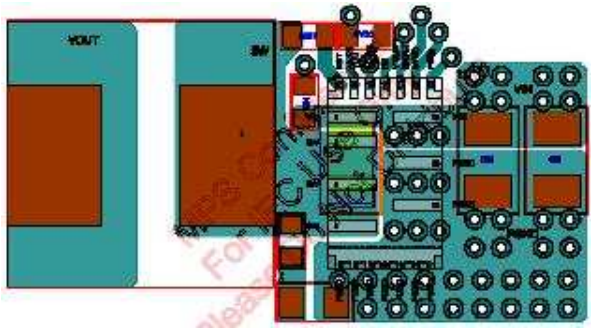
VRB_VDD3 IN
VRAGPU_PWM5 IN
VRAGPU_VTEMP OUT
VRB_VDD3 IN
VRAGPU_CS5 OUT
U67050
MPS_MP86941GQVT_Z_TQFN_21P
VRPVBAT_NVVDD
1UF CLOSE PIN1
VRPGPU_BST5
VRPGPU_SW5
VRAGPU_SYNC5
R67057 2K_5%_2
C67055 0.22UF_16V_2
L67050 TRIO_EM_22BM66V04
PVCORE_DGPU
330UF_2V_9MR_PANA_35%
22UF_6.3V_3
R67056 RSC_0603
C67056 CSC0402

VRB_VDD3 IN
VRAGPU_PWM6 IN
VRAGPU_VTEMP OUT
VRB_VDD3 IN
VRAGPU_CS6 OUT
U67060
MPS_MP86941GQVT_Z_TQFN_21P
VRPVBAT_NVVDD
1UF CLOSE PIN1
VRPGPU_BST6
VRPGPU_SW6
VRAGPU_SYNC6
R67067 2K_5%_2
C67065 0.22UF_16V_2
L67060 TRIO_EM_22BM66V04
PVCORE_DGPU
330UF_2V_9MR_PANA_35%
22UF_6.3V_3
R67066 RSC_0603
C67066 CSC0402



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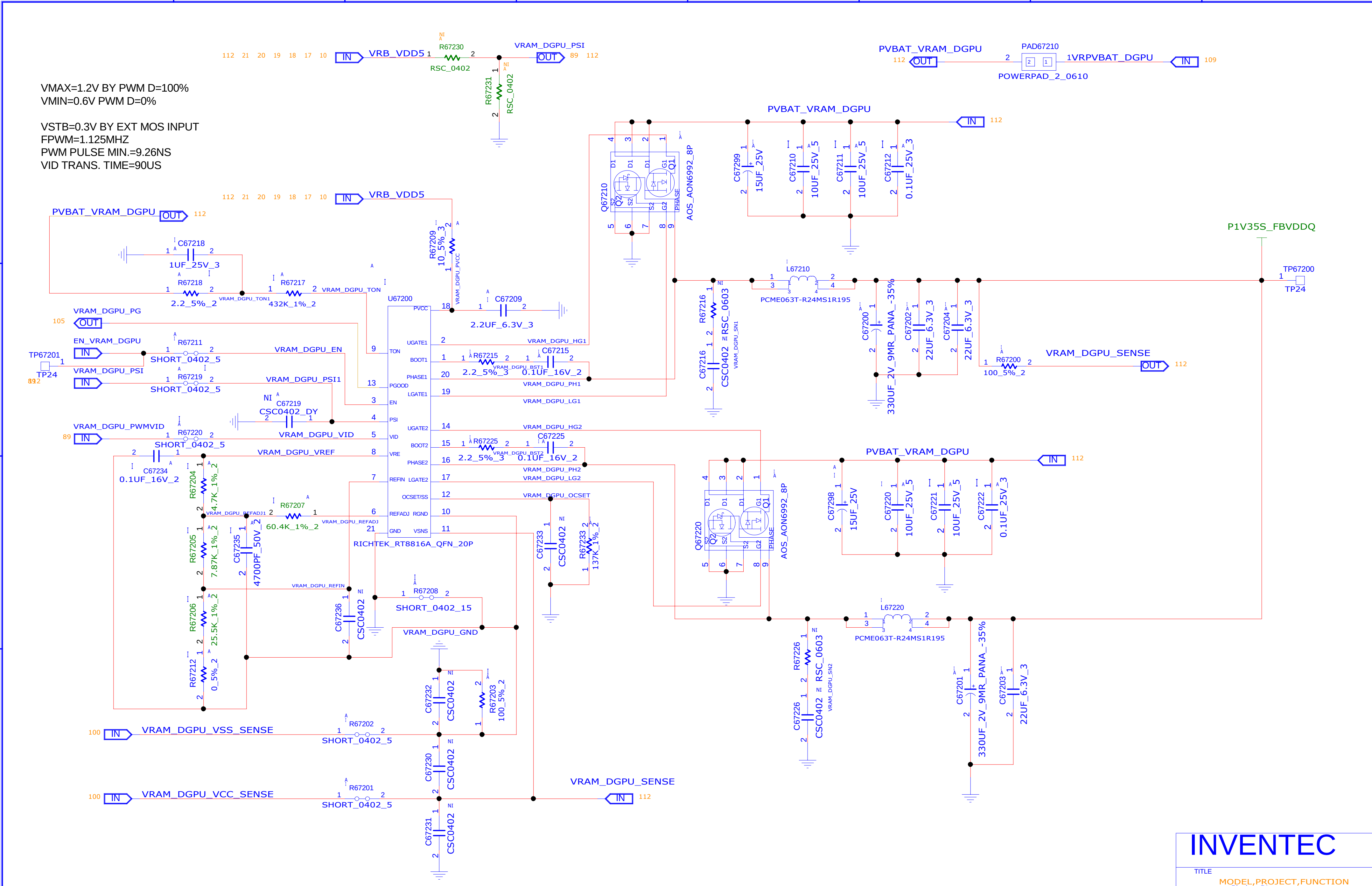

VMAX=1.2V BY PWM D=100%
VMIN=0.6V PWM D=0%
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=90US
VRB_VDD5
R67230
RSC_0402
VRAM_DGPU_PSI
R67231
PVBAT_VRAM_DGPU
PAD67210
1VRPVBAT_DGPU
POWERPAD_2_0610
Q67210
AOS_AON6992_8P
C67299 15UF_25V
C67210 10UF_25V_5
C67211 10UF_25V_5
C67212 0.1UF_25V_3
P1V35S_FBVDDQ
TP67200
TP24
C67218 1UF_25V_3
R67218 2.2_5%_2
R67217 432K_1%_2
VRAM_DGPU_TON
R67209 10_5%_3
C67209 2.2UF_6.3V_3
U67200
VRAM_DGPU_PG
EN_VRAM_DGPU
R67211 SHORT_0402_5
VRAM_DGPU_EN
TP67201
VRAM_DGPU_PSI
R67219 SHORT_0402_5
VRAM_DGPU_PSI1
C67219 CSC0402_DY
VRAM_DGPU_PWMVID
R67220 SHORT_0402_5
VRAM_DGPU_VID
C67234 0.1UF_16V_2
VRAM_DGPU_VREF
R67215 2.2_5%_3
C67215 0.1UF_16V_2
VRAM_DGPU_HG1
VRAM_DGPU_PH1
VRAM_DGPU_LG1
R67225 2.2_5%_3
C67225 0.1UF_16V_2
VRAM_DGPU_HG2
VRAM_DGPU_PH2
VRAM_DGPU_LG2
VRAM_DGPU_OCSET
L67210 PCME063T-R24MS1R195
R67216 RSC_0603
C67216 CSC0402
C67200 330UF_2V_9MR_PANA_-35%
C67202 22UF_6.3V_3
C67204 22UF_6.3V_3
R67200 100_5%_2
VRAM_DGPU_SENSE
R67204 4.7K_1%_2
R67207 60.4K_1%_2
R67205 7.87K_1%_2
C67235 4700PF_50V_2
R67206 25.5K_1%_2
R67212 0_5%_2
RICHTEK_RT8816A_QFN_20P
C67236 CSC0402
R67208 SHORT_0402_15
VRAM_DGPU_GND
C67233 CSC0402
R67233 137K_1%_2
Q67220 AOS_AON6992_8P
C67298 15UF_25V
C67220 10UF_25V_5
C67221 10UF_25V_5
C67222 0.1UF_25V_3
L67220 PCME063T-R24MS1R195
R67226 RSC_0603
C67226 CSC0402
C67201 330UF_2V_9MR_PANA_-35%
C67203 22UF_6.3V_3
C67232 CSC0402
R67203 100_5%_2
VRAM_DGPU_VSS_SENSE
R67202 SHORT_0402_5
C67230 CSC0402
VRAM_DGPU_VCC_SENSE
R67201 SHORT_0402_5
C67231 CSC0402

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
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CHANGE by XXX	DATE 21-OCT-2002	SHEET 112 of 130	
PCB P/N 60xxxxxxxxxx	PCB VER XXX		

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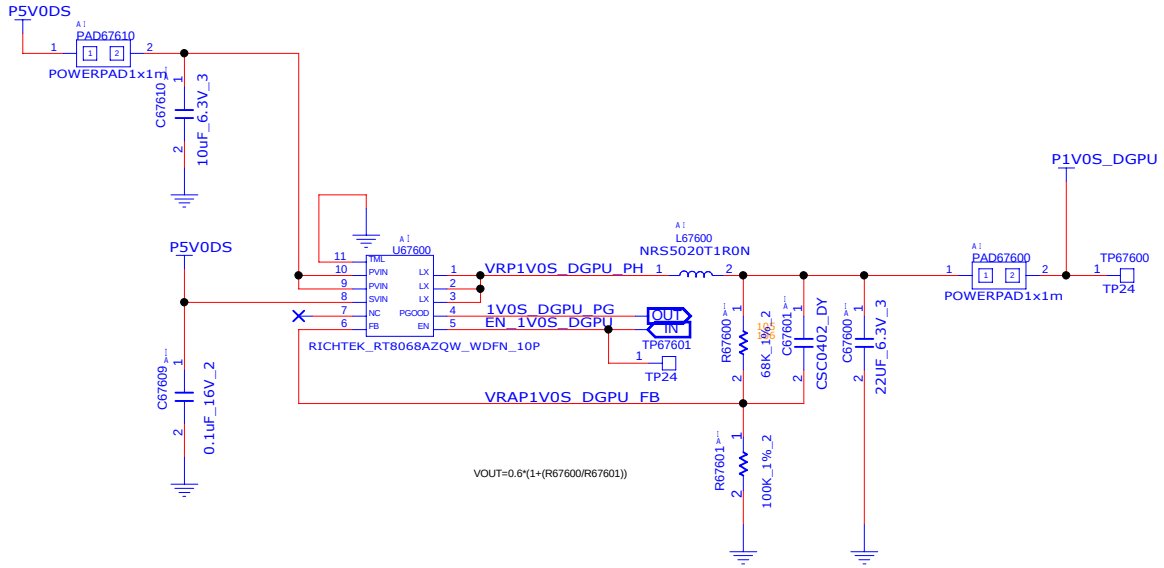

INVENTEC

TITLE
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Block Diagram

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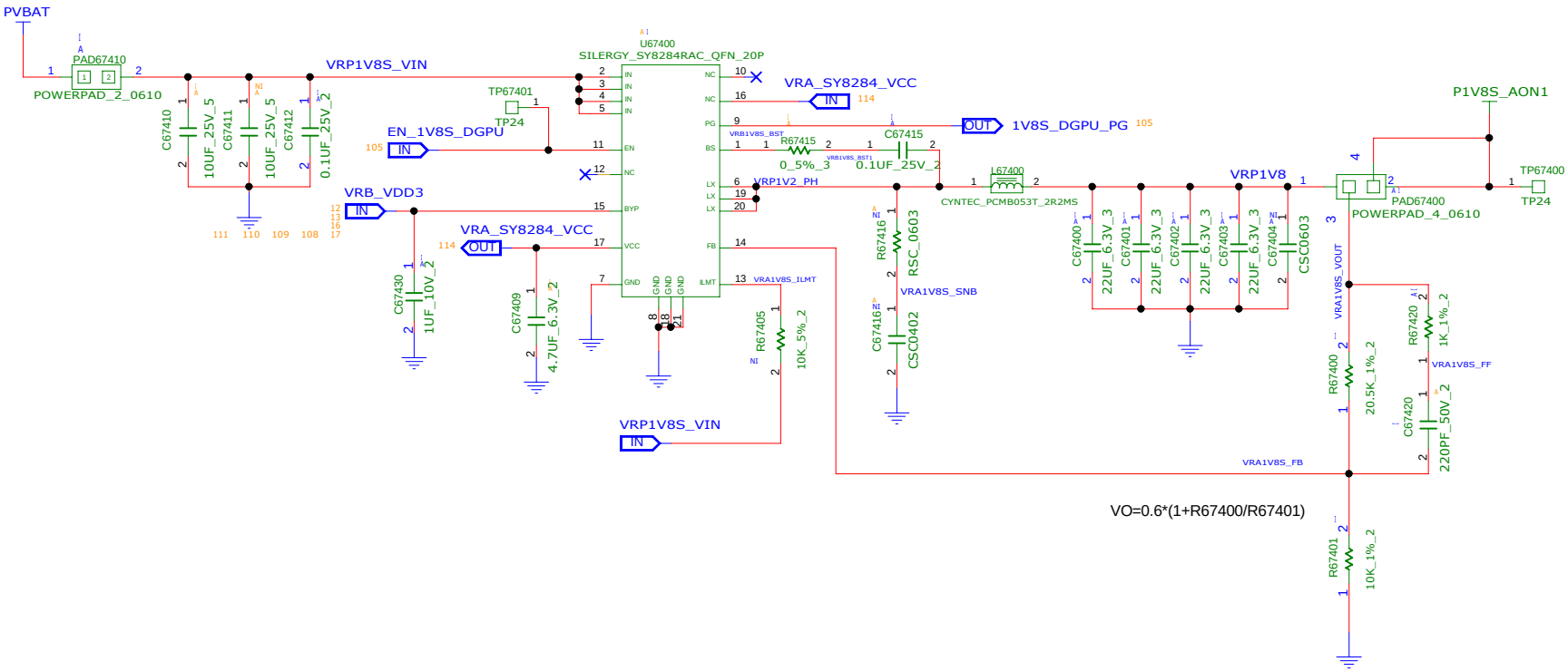

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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Table 12. Output EDP-Continuous

Product	TGP (W)	NVVDD — (A)	FB TOTAL[5] 1.35V[3, 4] (A)	1.0V Total[1] 1.0V[3] (A)	1.8V Total[2] 1.8V[3] (A)
N18E-G3	150	144	46	1.6	2.3
	160	152			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms)[2] (A)	Input EDPp (5ms)[2] (A)	Input EDPc (1sec)[1] (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$Input\ EDPc\ Current\ (A) = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$Input\ EDPp\ (A) at\ V_{new} = Input\ EDPp(A)\ at\ 19V x\ \frac{19V}{V_{new}(V)}$$

Table 14. Output EDP-Peak

Product	TGP (W)	NVVDD - (A)	FB TOTAL[4] 1.35V[2, 3] (A)	1.0V Total[1] 1.0V[2] (A)	1.8V Total[2] 1.8V[5] (A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

INVENTEC

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HISTORY

SCHEMATIC MODIFY HISTORY

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SIZE	CODE	DOC.NUMBER	REV
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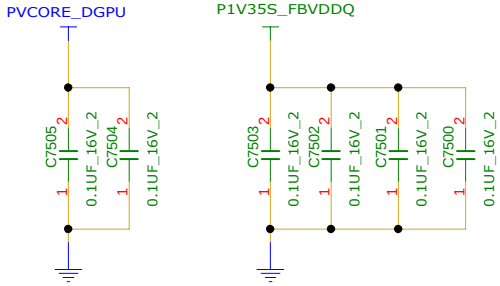
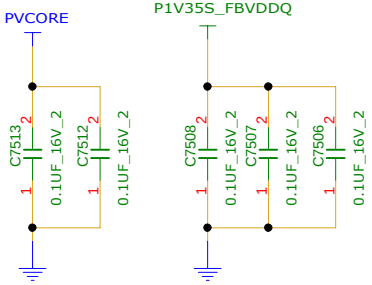
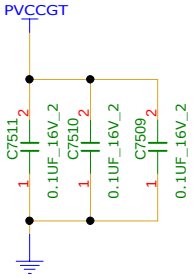
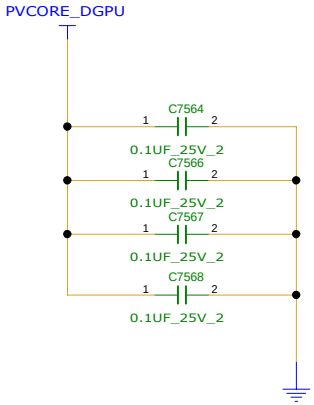
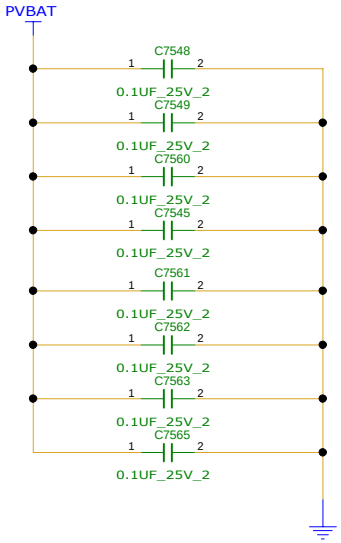
EMI

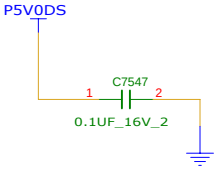


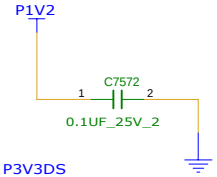


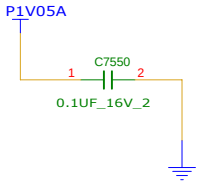


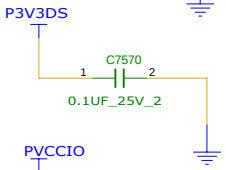


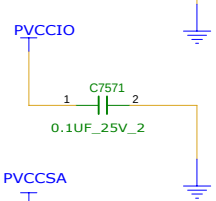


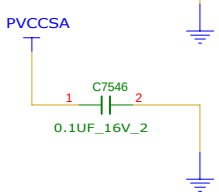


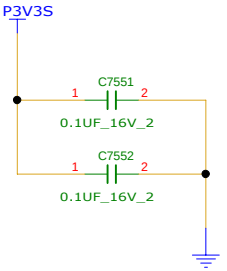












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NFC CNNN.

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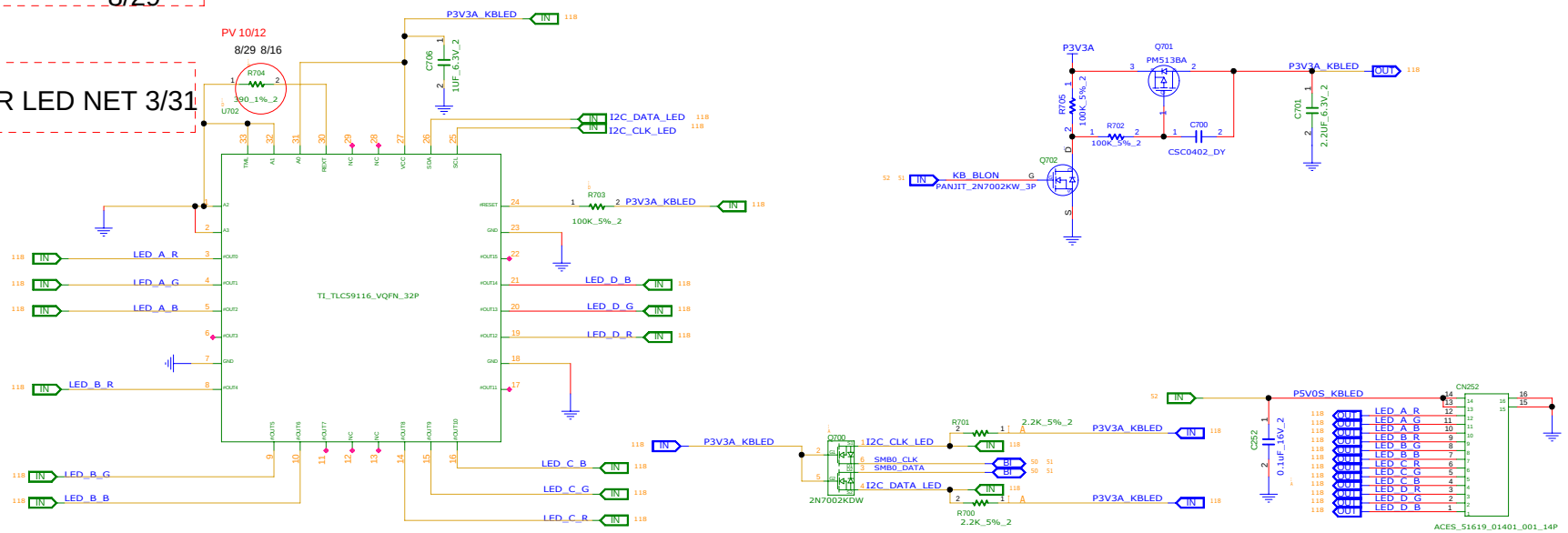
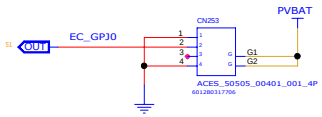
ADJUST LED RES 8/16
8/29

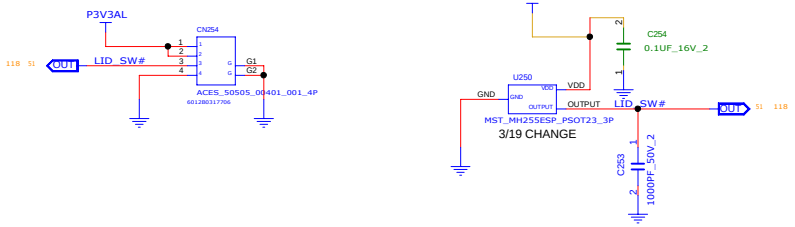
RE-ORDER LED NET 3/31



TURBO#



HALL_SENSOR



REFERENCE NUMBER:700~800

INVENTEC
MODEL,PROJECT,FUNCTION
RING LED

HALL SENSOR BOARD

TURBO# BOARD

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Block Diagram

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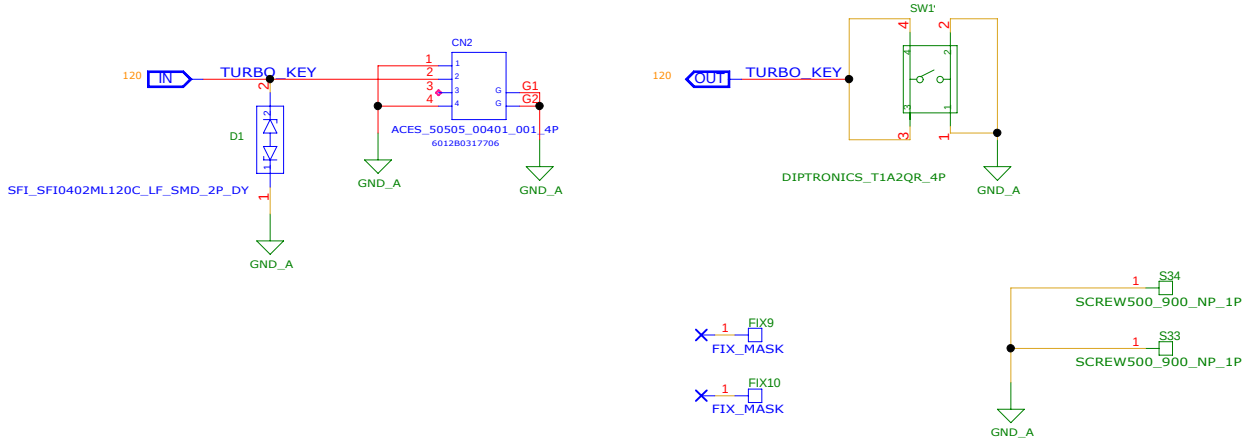
TURBO#



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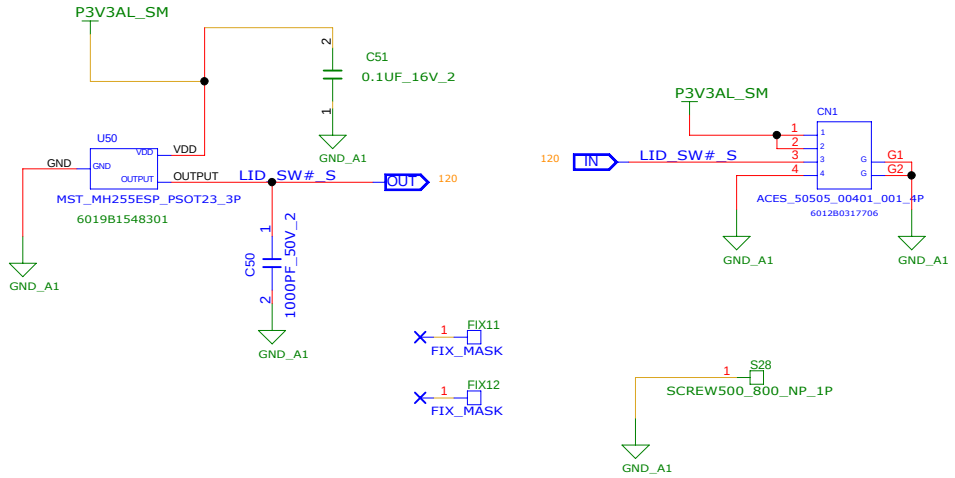

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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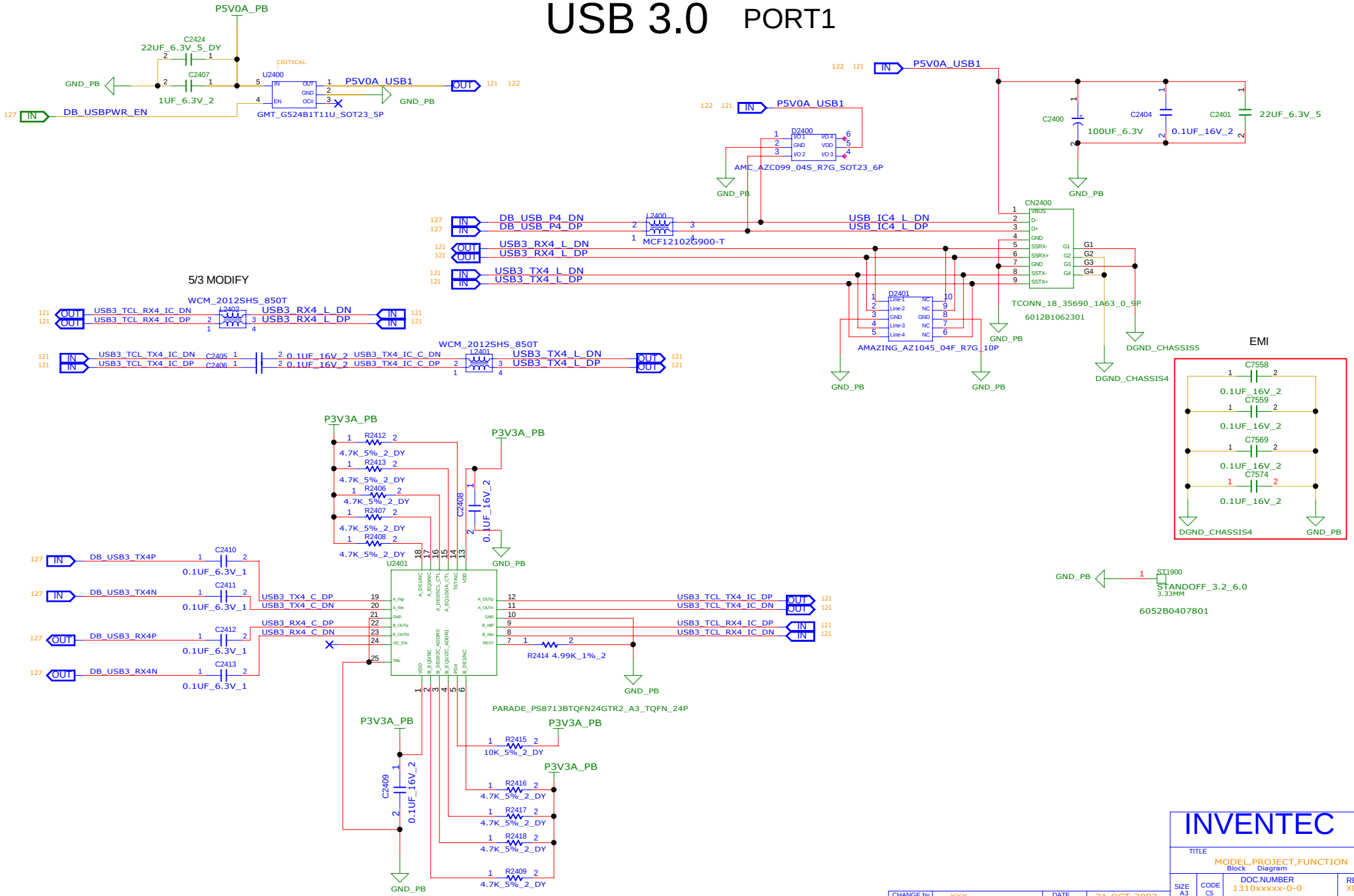
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



CHANGE by	XXX	DATE	21-OCT-2002
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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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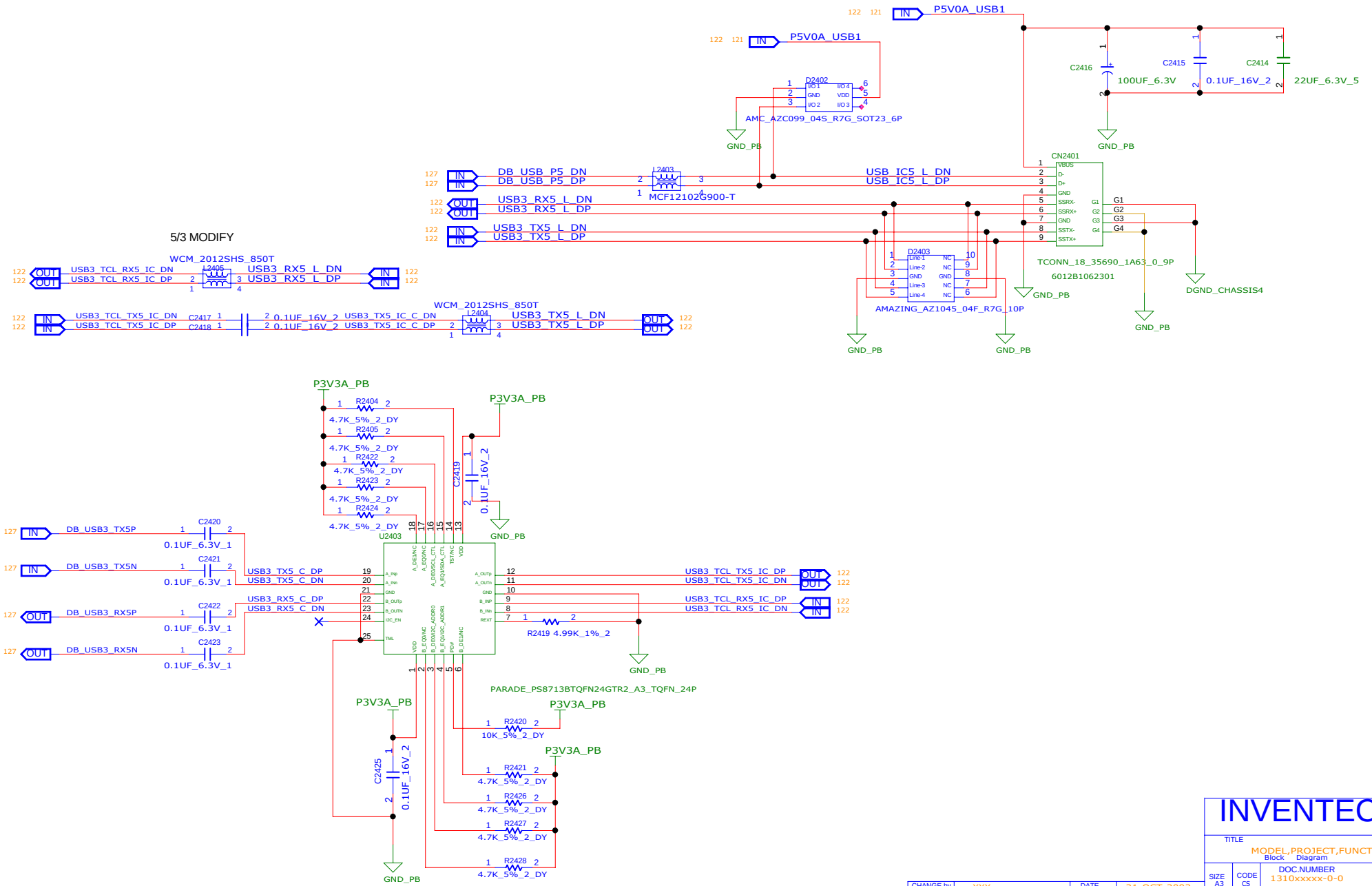
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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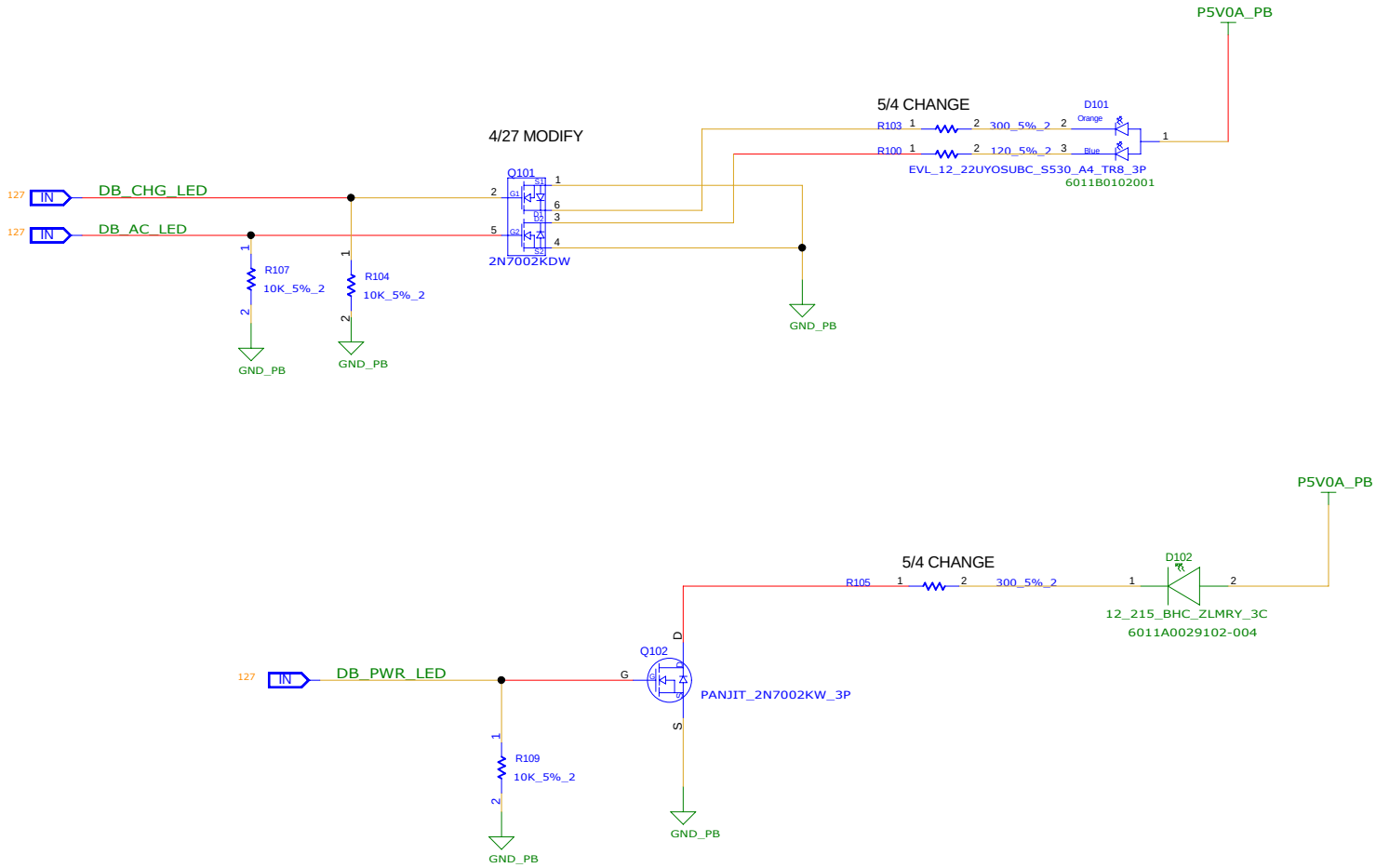

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Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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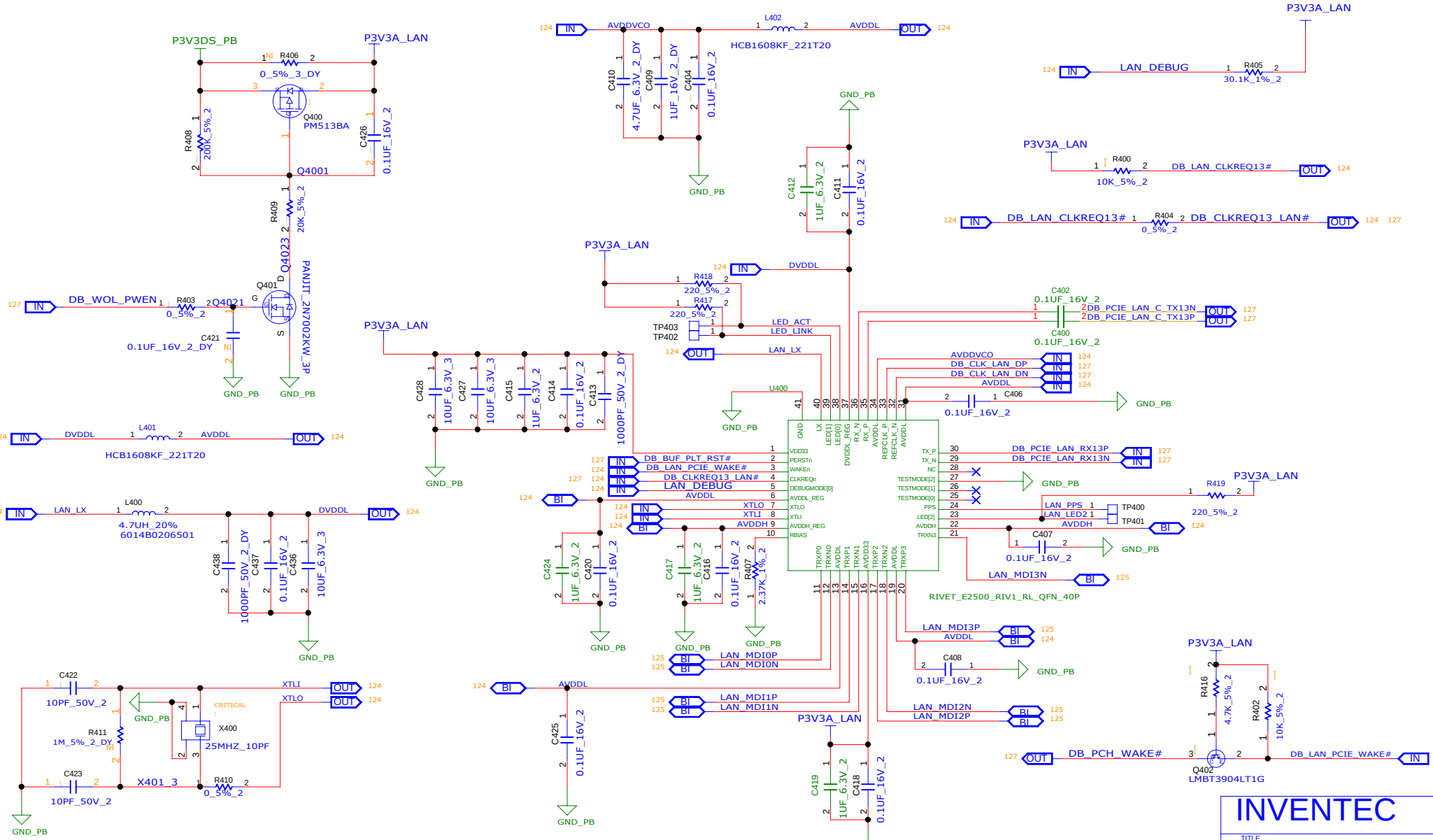
LAN (CONTROLLER)
E2500



CHANGE by	XXX	DATE	21-OCT-2002
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TITLE: MODEL,PROJECT,FUNCTION
USB/DP DE-MUX

SIZE	CODE	DOC.NUMBER	REV
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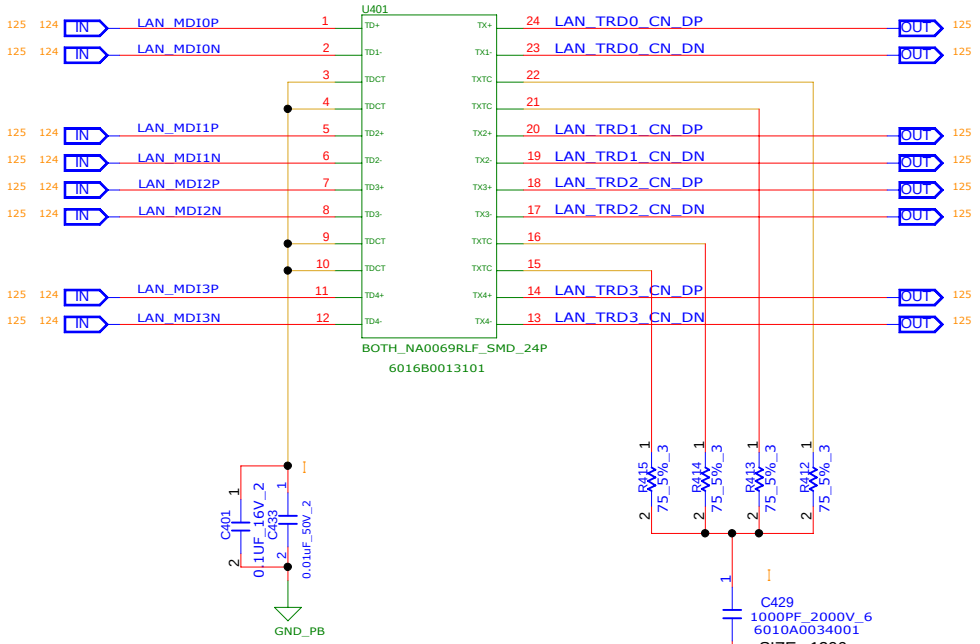
TRANSFORMER



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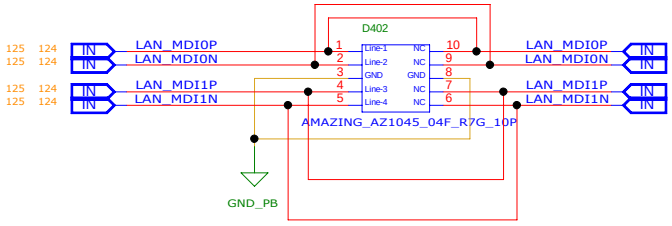
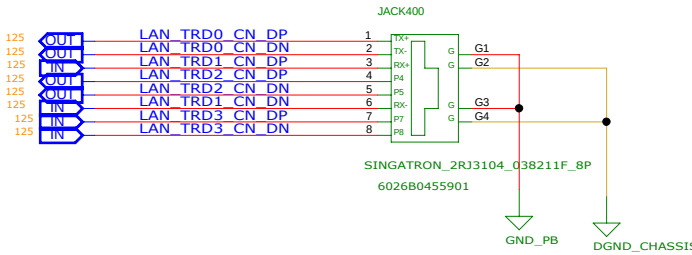
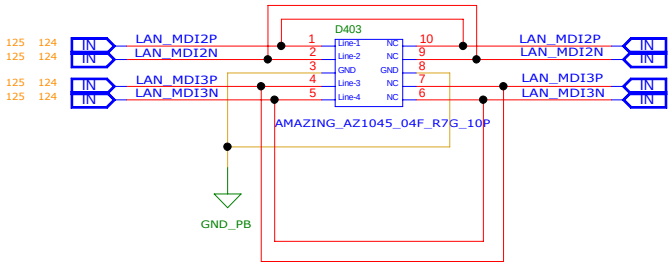
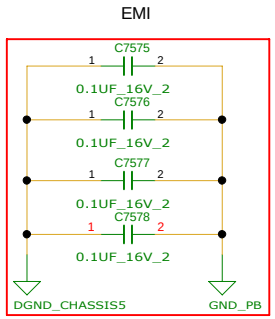


RJ-45







INVENTEC

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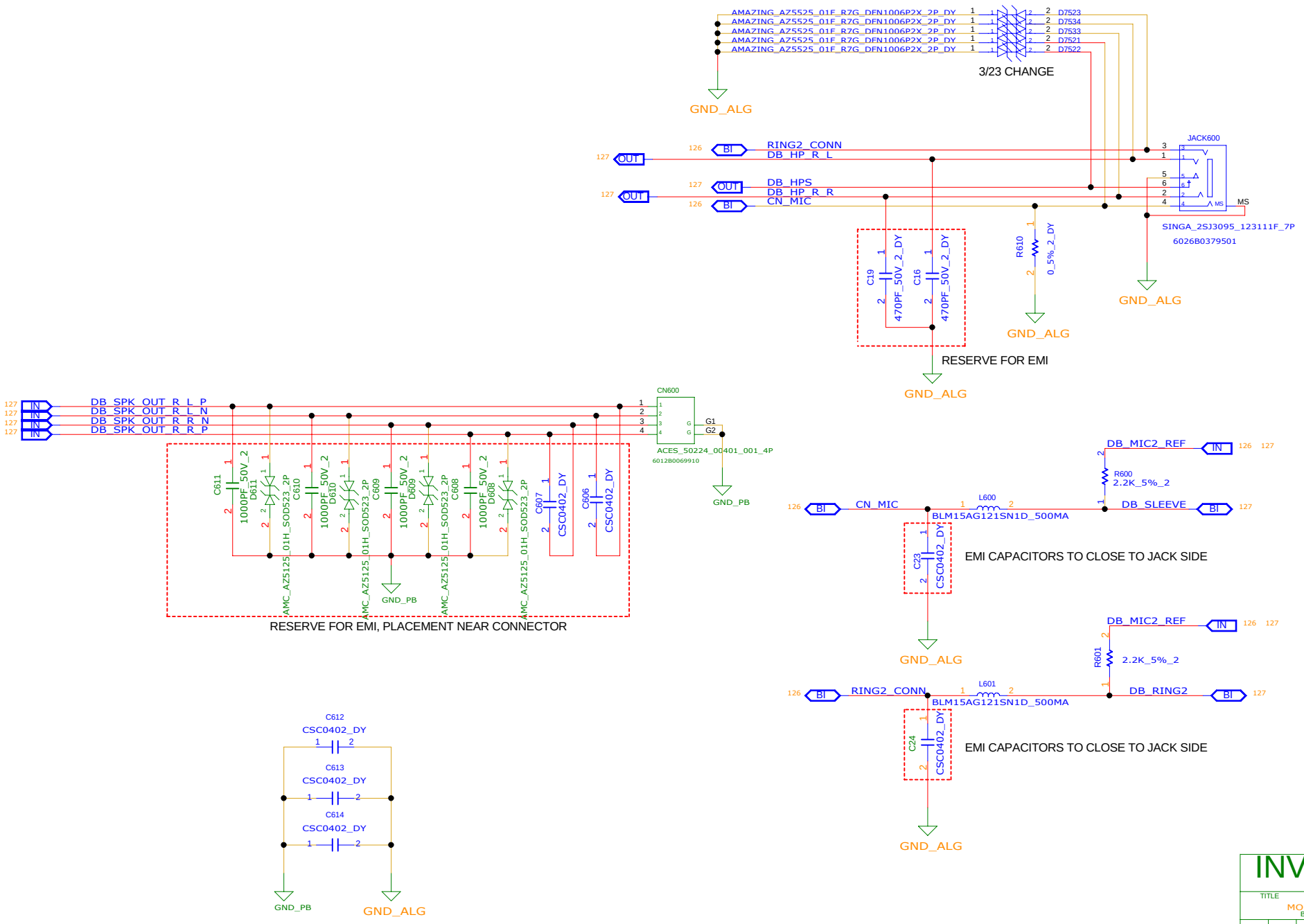

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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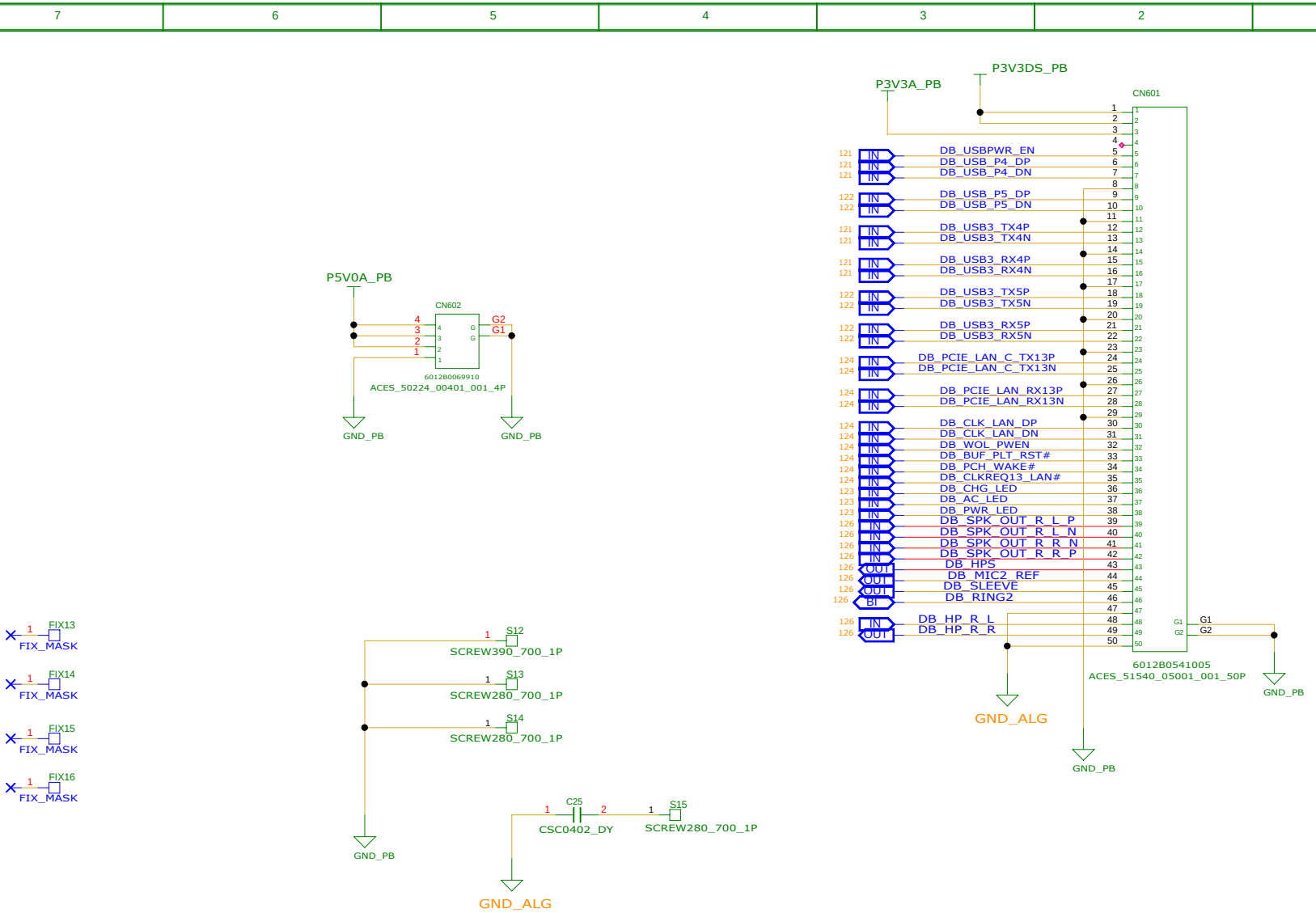

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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FOR 17 SMALL BOARD

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Block Diagram

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8	7	6	5	4	3	2	1

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INVENTEC

TITLE
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07e3020d0714280027008b3c1a003fc1