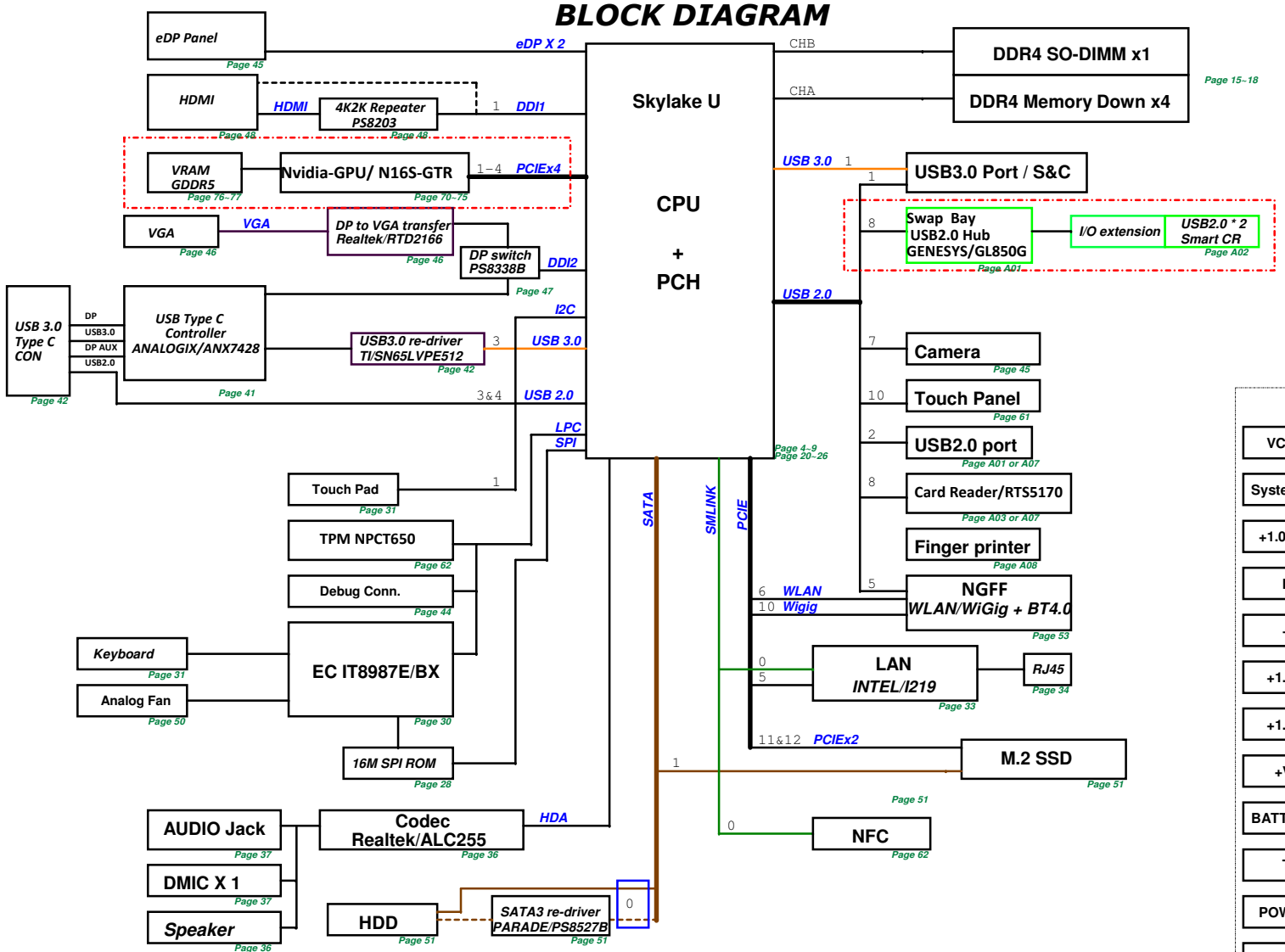
P4 Skylake U (2+2) Rev1.0

SYSTEM PAGE REF.

BLOCK DIAGRAM



Power

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- System (5V & 3.3V) — Page 81
- +1.0VSUS & 2.5V — Page 82
- DDR & VTT — Page 83
- +1.8VSUS — Page 84
- +1.35VS_VGA — Page 85
- +1.05VS_VGA — Page 86
- +VGA_VCORE — Page 87
- BATTERY CHARGER — Page 88
- Type-C PD — Page 89
- POWER DETECT — Page 90
- LOAD SWITCH — Page 91
- Power Protect — Page 92

D.B.

- Swap Bay DB — Page A01~A03
- IO DB — Page A07
- LED DB — Page A04
- TP DB — Page A05
- KB LED DB — Page A06

- Discharge Circuit — Page 57
- DC & BATT. Conn. — Page 60
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<Variant Name>

PEGATRON
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Title : Block Diagram

Engineer: Bill Yang

Size	Project Name	Rev
BG1/HW3	P4	1.0
Custom		

Date: Tuesday, September 06, 2016 Sheet 1 of 108

<Variant Name>

PEGATRON Title :

Engineer:

Size | Project Name | Rev
1.1

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SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

+VCCIO +VCCIO 7,57,91
+VCCST_CPU +VCCST_CPU 5,7,9,25
+VCCSTG +VCCSTG 5,7
+3VS +3VS 4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

DDI Port 1: HDMI

DDI Port 2: DP Switch

U0301A

DDI

EDP

DISPLAY SIDEBANDS

eDP x 2

Pull down at connector side

940432
01V010000015

U0301D

CPU MISC

JTAG

940432
01V010000015

R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result),預留0ohm是調整空間

DDPB_CTRLDATA has pull high at connector side

DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
1 : port is deteccted

Table 5-10. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect

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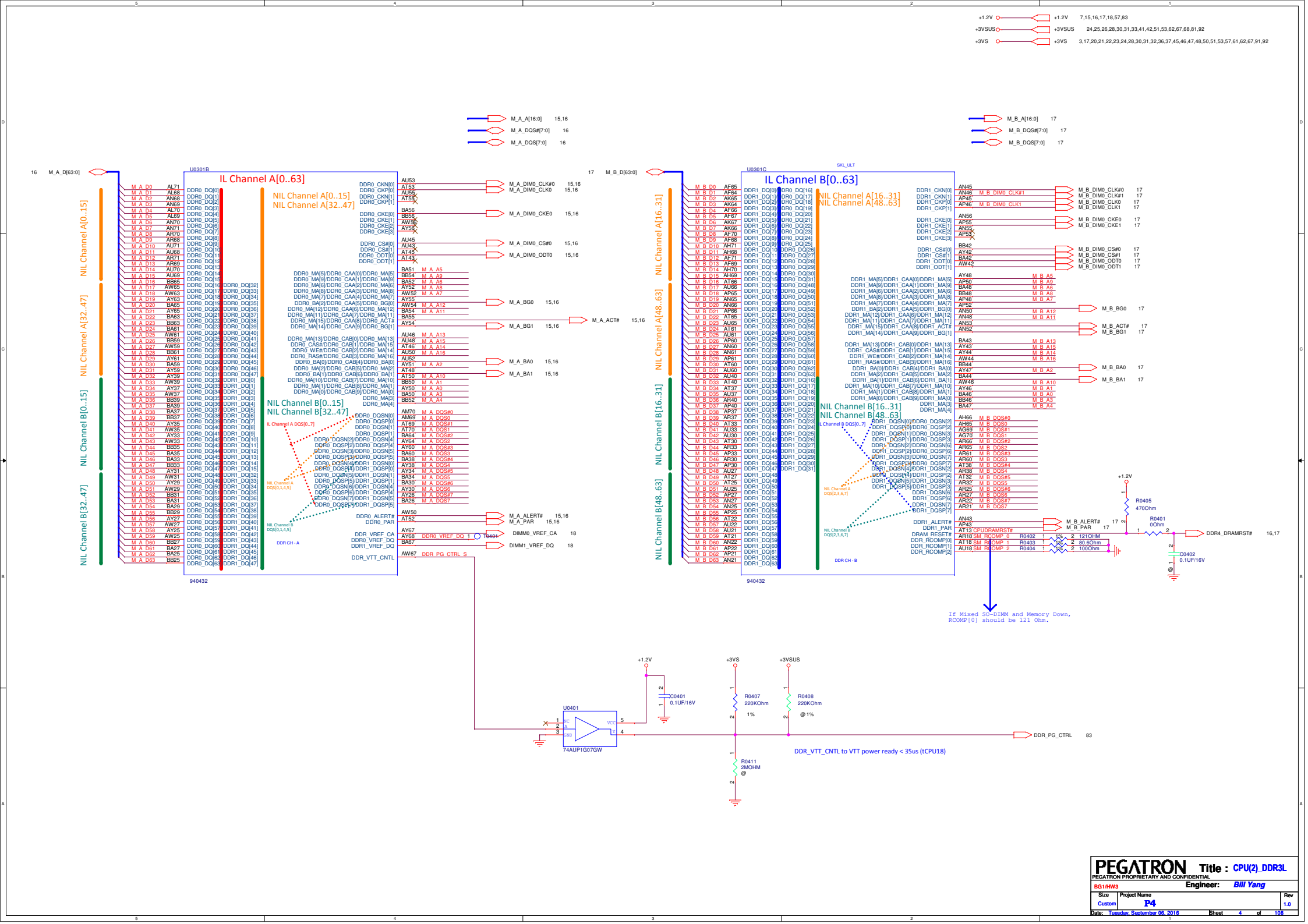
Title : CPU(1)_DDI/eDP

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 3 of 108



PEGATRON
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Title : CPU(2)_DDR3L

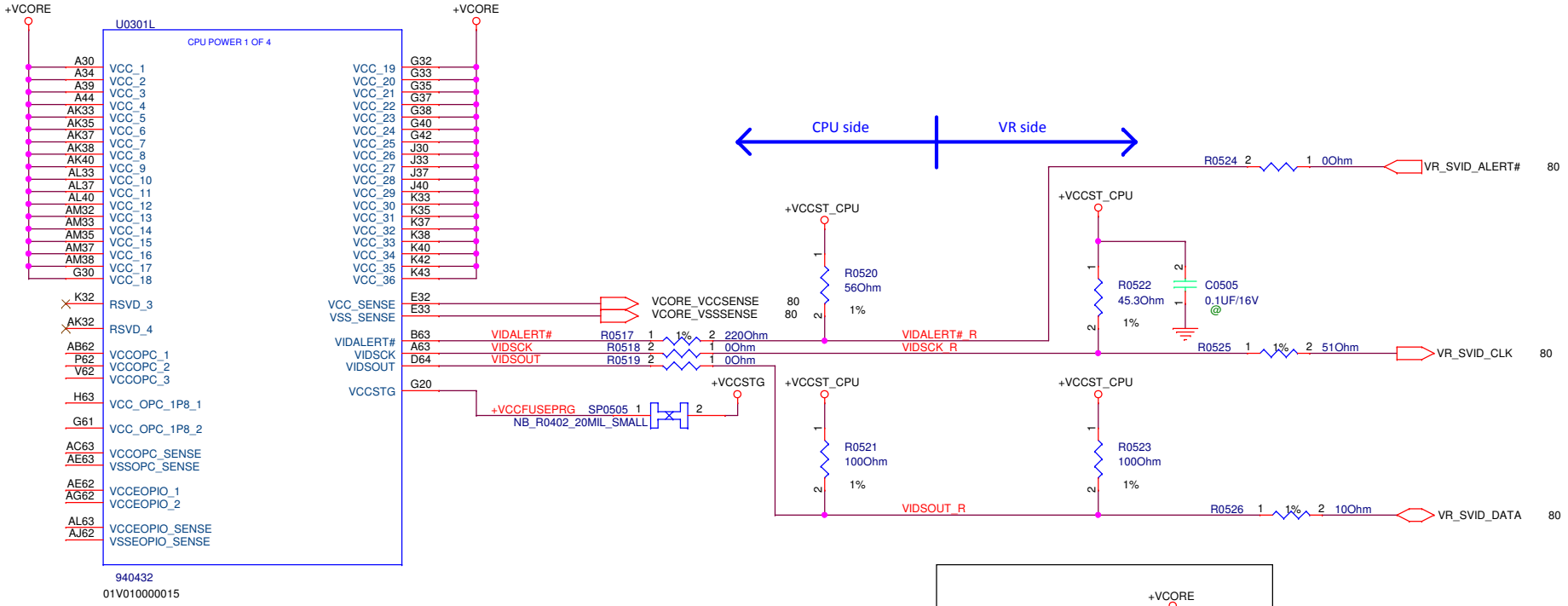
BG1/HW3

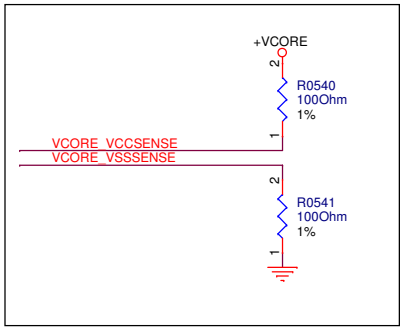
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

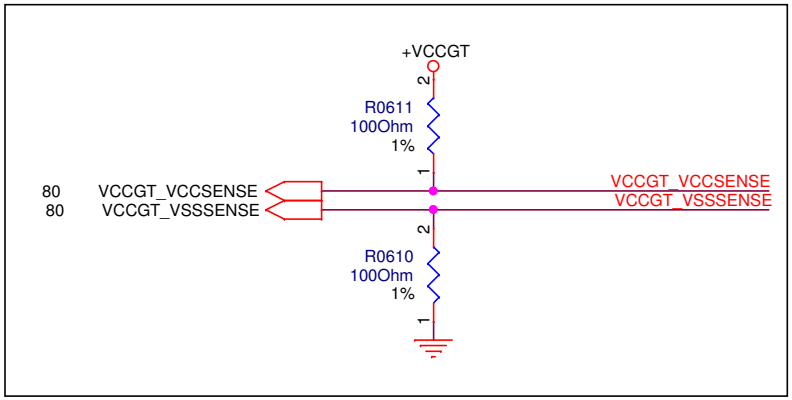
Date: Tuesday, September 06, 2016 Sheet 4 of 108

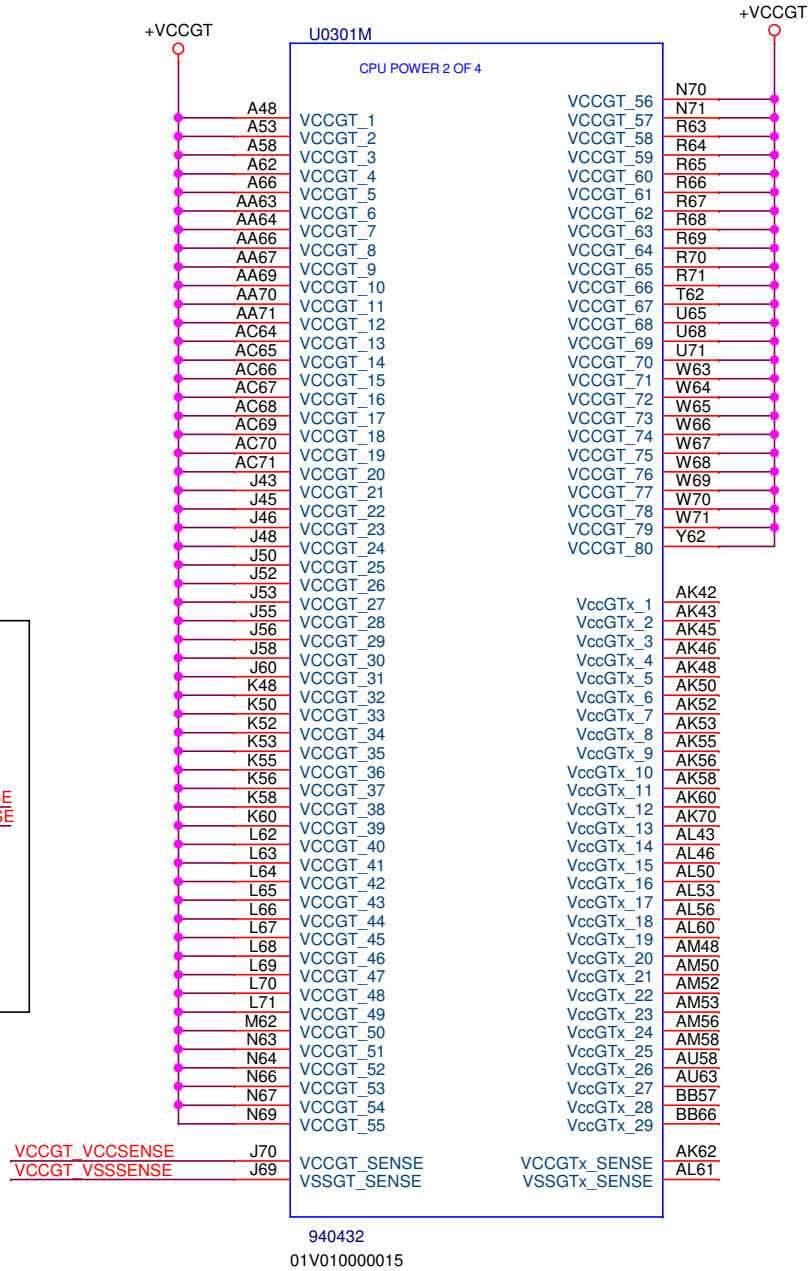
+VCORE +VCORE 57,80
+VCCSTG +VCCSTG 3,7
+VCCST_CPU +VCCST_CPU 3,7,9,25





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CPU(3)_+VCCCORE
BG1/HW3
Engineer: Bill Yang
Size: Custom
Project Name: P4
Rev: 1.0
Date: Tuesday, September 06, 2016
Sheet 5 of 108





PEGATRON
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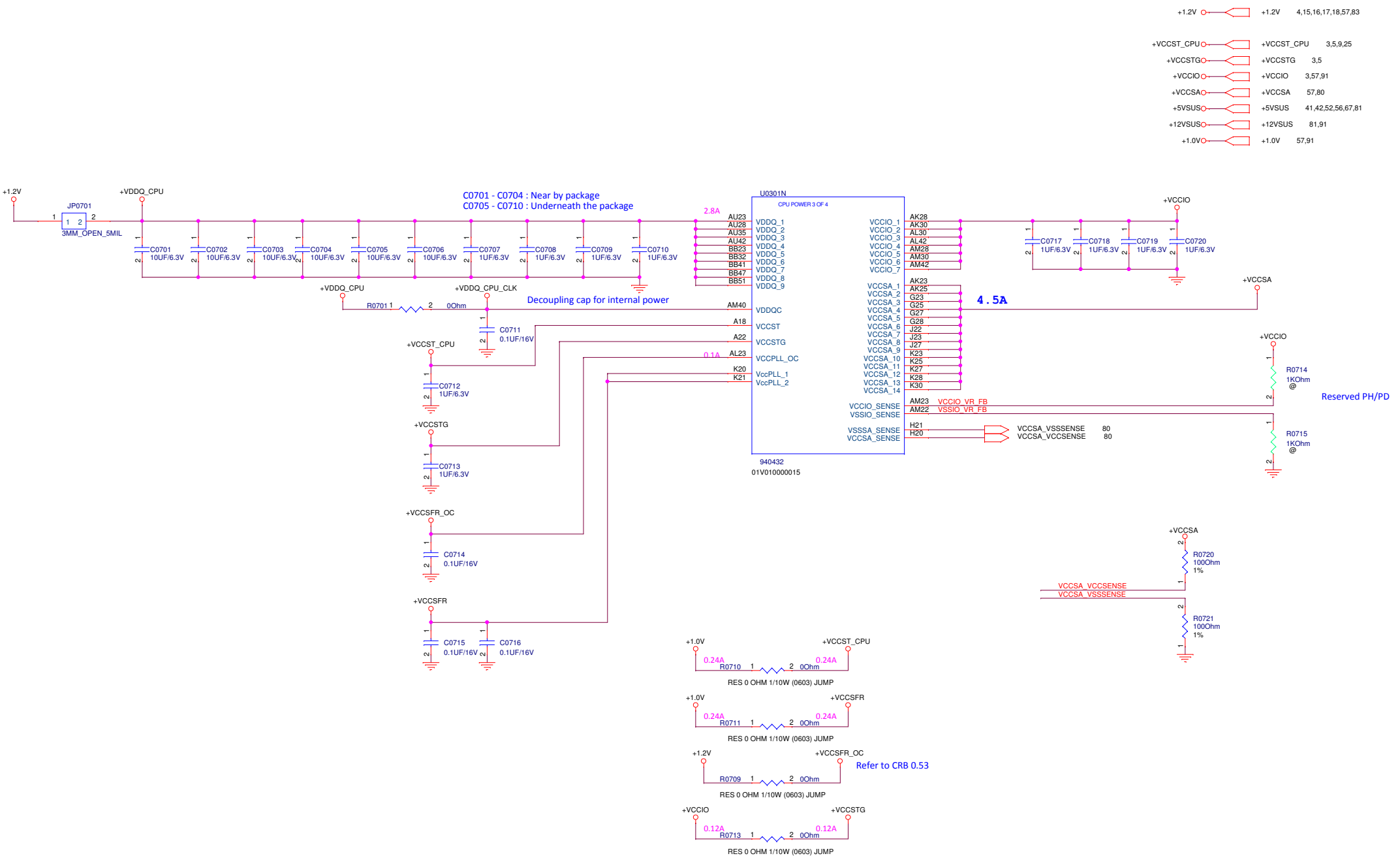
Title : CPU(4)_+VCCGT

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 6 of 108



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

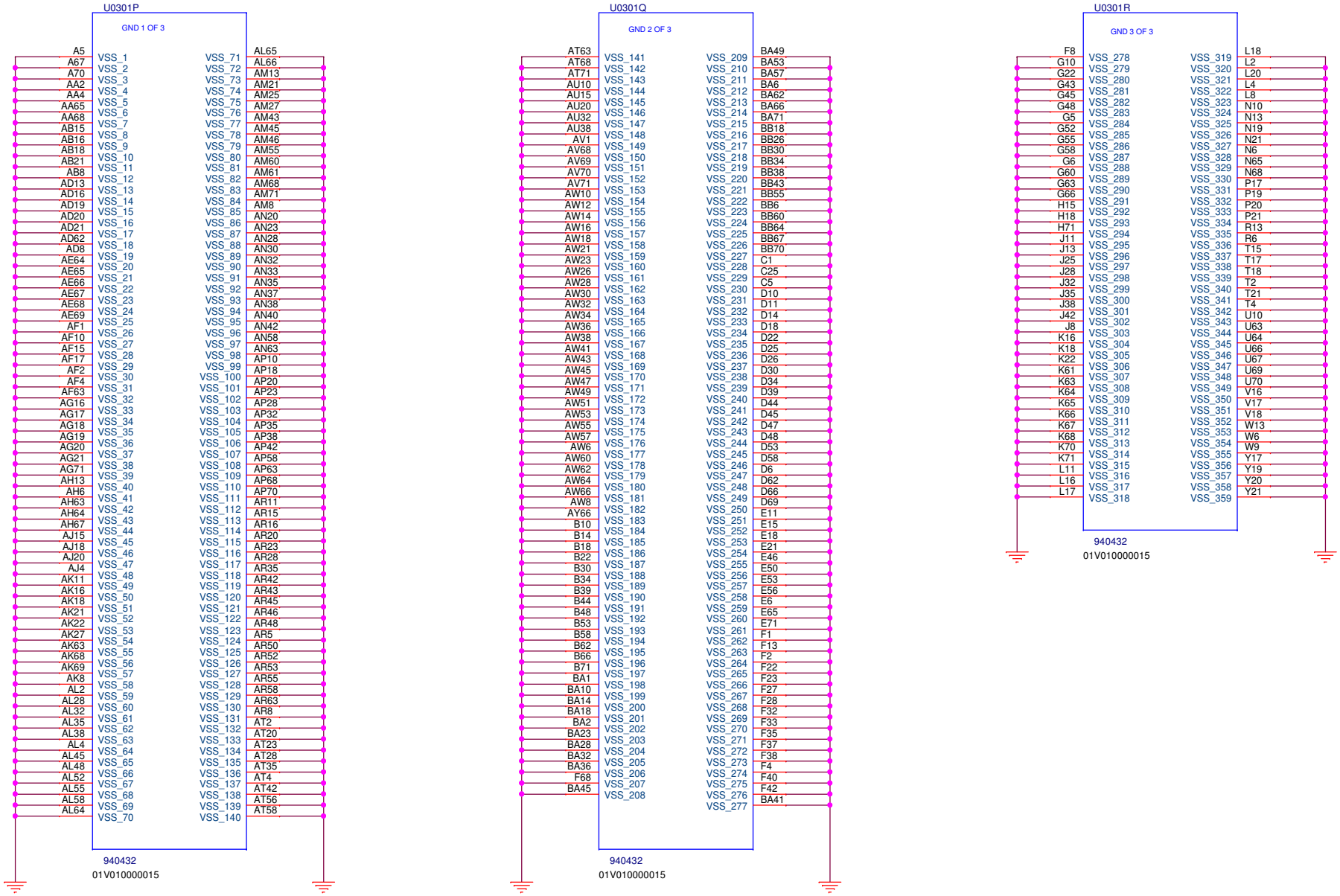
Title: CPU(5)_+VDDQ/IO/SA

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 7 of 108



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : CPU(6)_CPU GND

BG1/HW3

Engineer: Bill Yang

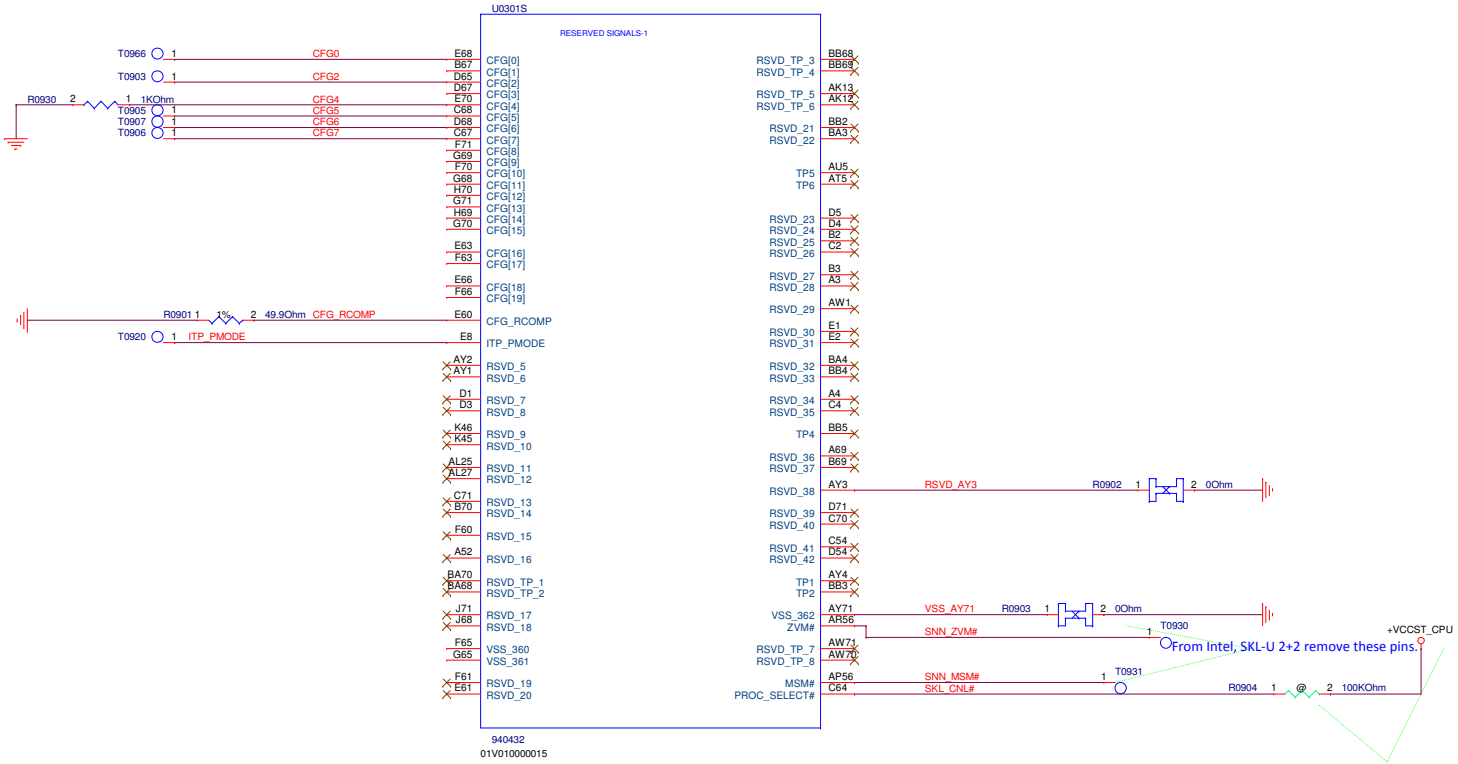
Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 8 of 108

6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.



1.3.2 [U] Skylake-U and Cannonlake-U Compatibility Decoupling Requirement

Two reserve pins (U11 and U12) for 1.8V were added to Skylake-U PCH to support Cannonlake-U PCH compatibility. For Skylake-U, the following changes will be made to Table 52-8 in the Skylake U/Y Platform Design Guide (IBP#543016).

Table 52-8 – Decoupling and Power Connection Requirement for Skylake-U PCH

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)ionway / (E)dge	Place capacitor(s) near ball(s)
V1.8A	VccPGPPF	AF16	-	-	-	-	-
	VccATS	AA1	1 uF	0402	1	E (<10 mm)	AA1
	Vcc_1P8	U11, U12	1 uF	0402	1	E (<10 mm)	U11, U12 (Note 1 & 5)

PEGATRON
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Title :CPU(7)_CFG/RSVD
BG1/HW3
Engineer: Bill Yang
Size: Custom | Project Name: P4 | Rev: 1.0
Date: Tuesday, September 06, 2016 | Sheet 9 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

Size	Project Name	Rev
		1.1

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<Variant Name>

PEGATRON Title :

Engineer:

Size	Project Name	Rev
		1.1

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Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
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Title	<Title>
Size: A	Document Number: <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
Sheet	13 of 108

<Variant Name>

PEGATRON Title :

Engineer:

Size	Project Name	Rev
		1.1

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DDR4(0)_Termination

+0.6VS — +0.6VS 17,57,83

+1.2V — +1.2V 4,7,16,17,18,57,83

+0.6VS

1	34.8Ohm 2	R1501 1%	M0_MA0	M_A_A0 4,16
1	34.8Ohm 2	R1502 1%	M0_MA1	M_A_A1 4,16
1	34.8Ohm 2	R1503 1%	M0_MA2	M_A_A2 4,16
1	34.8Ohm 2	R1504 1%	M0_MA3	M_A_A3 4,16
1	34.8Ohm 2	R1505 1%	M0_MA4	M_A_A4 4,16
1	34.8Ohm 2	R1506 1%	M0_MA5	M_A_A5 4,16
1	34.8Ohm 2	R1507 1%	M0_MA6	M_A_A6 4,16
1	34.8Ohm 2	R1508 1%	M0_MA7	M_A_A7 4,16
1	34.8Ohm 2	R1509 1%	M0_MA8	M_A_A8 4,16
1	34.8Ohm 2	R1510 1%	M0_MA9	M_A_A9 4,16
1	34.8Ohm 2	R1511 1%	M_A_A10_AP	M_A_A10 4,16
1	34.8Ohm 2	R1512 1%	M0_MA11	M_A_A11 4,16
1	34.8Ohm 2	R1513 1%	M0_MA12	M_A_A12 4,16
1	34.8Ohm 2	R1514 1%	M0_MA13	M_A_A13 4,16
1	34.8Ohm 2	R1515 1%	M_A_A14_WE_N	M_A_A14 4,16
1	34.8Ohm 2	R1516 1%	M_A_A15_CAS_N	M_A_A15 4,16
1	34.8Ohm 2	R1529 1%	M_A_A16_RAS_N	M_A_A16 4,16

+0.6VS

4,16	M_A_DIM0_CS#0	1% R1521 1	2 34.8Ohm	vx_r0402_small
4,16	M_A_DIM0_CKE0	1% R1522 1	2 34.8Ohm	vx_r0402_small

+0.6VS

4,16	M_A_BG0	1% R1523 2	1 34.8Ohm	vx_r0402_small
4,16	M_A_BG1	1% R1538 2	/DDR 1 34.8Ohm	vx_r0402_small
4,16	M_A_BA0	1% R1524 2	1 34.8Ohm	vx_r0402_small
4,16	M_A_BA1	1% R1525 2	1 34.8Ohm	vx_r0402_small
4,16	M_A_DIM0_ODT0	1% R1530 2	1 34.8Ohm	vx_r0402_small
4,16	M_A_ACT#	1% R1532 2	1 34.8Ohm	vx_r0402_small
4,16	M_A_PAR	1% R1534 2	1 34.8Ohm	vx_r0402_small

+0.6VS

4,16	M_A_DIM0_CLK#0	5% R1536 1	2 36Ohm	vx_r0402_small
4,16	M_A_DIM0_CLK0	5% R1537 1	2 36Ohm	vx_r0402_small

+1.2V

4,16	M_A_ALERT#	1% R1535 1	2 49.9Ohm	vx_r0402_small

Average placed close to +VDDQ_VTT power plane

+0.6VS

C1501	1UF/6.3V X5R/10%	vx_c0402_small
C1502	1UF/6.3V X5R/10%	vx_c0402_small
C1053	1UF/6.3V X5R/10%	vx_c0402_small
C1504	1UF/6.3V X5R/10%	vx_c0402_small
C1505	1UF/6.3V X5R/10%	vx_c0402_small
C1506	1UF/6.3V X5R/10%	vx_c0402_small
C1507	1UF/6.3V X5R/10%	vx_c0402_small
C1508	1UF/6.3V X5R/10%	vx_c0402_small

+0.6VS

C1509	10UF/6.3V
C1510	10UF/6.3V

PEGATRON Title : DDR4(1)_Termination

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BG1-NB4 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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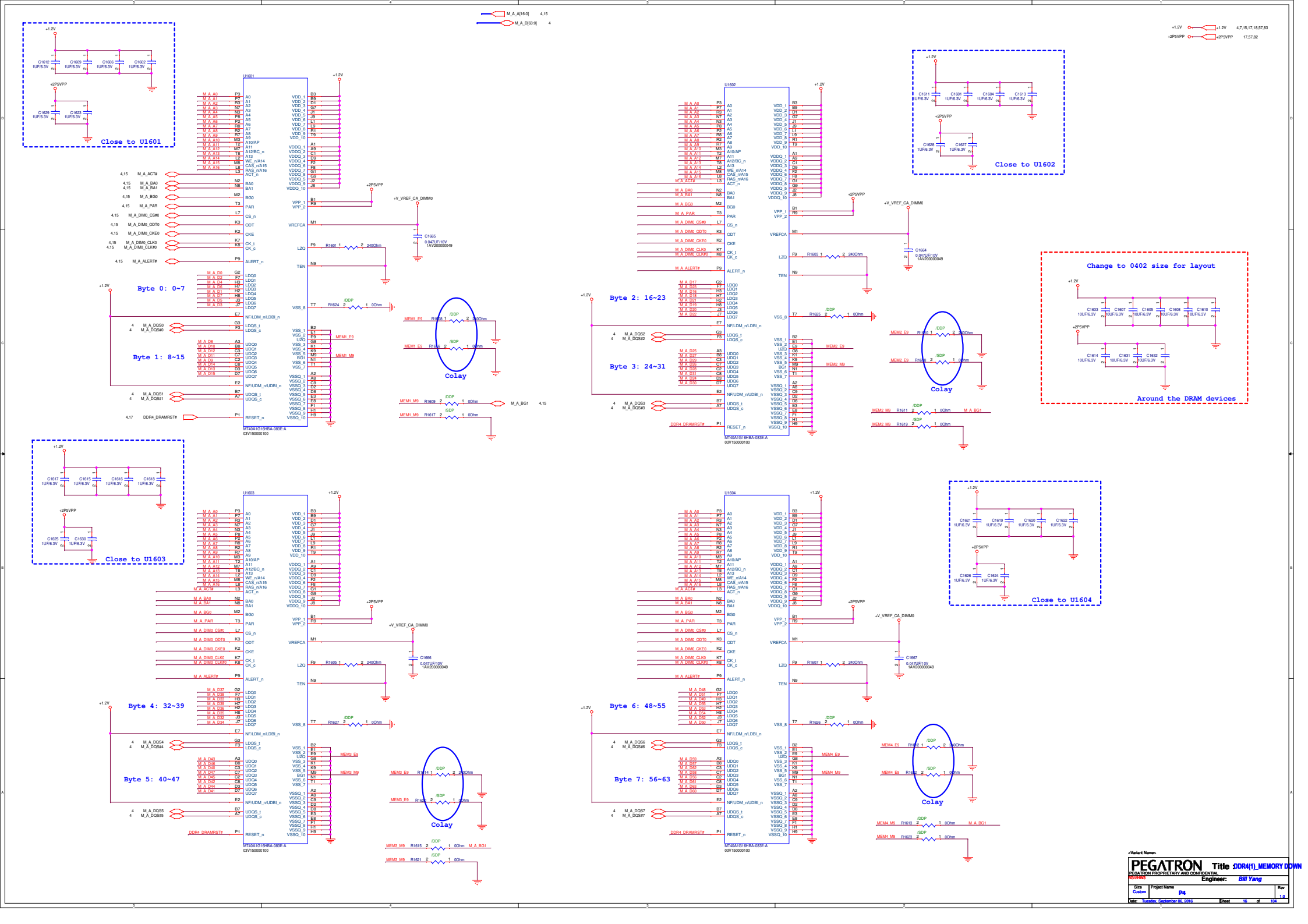
M_A_A[16:0] 4,15
M_A_D[63:0] 4
+1.2V 4,7,15,17,18,57,83
+2P5VPP 17,57,82
Close to U1601
Close to U1602
Close to U1603
Close to U1604
Change to 0402 size for layout
Around the DRAM devices
U1601
U1602
U1603
U1604
MT40A1G16HBA-083E:A
03V150000100
Byte 0: 0~7
Byte 1: 8~15
Byte 2: 16~23
Byte 3: 24~31
Byte 4: 32~39
Byte 5: 40~47
Byte 6: 48~55
Byte 7: 56~63
+V_VREF_CA_DIMM0
Colay
DDR4_DRAMRST#
M_A_ACT#
M_A_ALERT#
M_A_PAR
M_A_BG0
M_A_BA0
M_A_BA1
M_A_DIM0_CS#0
M_A_DIM0_ODT0
M_A_DIM0_CKE0
M_A_DIM0_CLK0
M_A_DIM0_CLK#0
M_A_DQS0
M_A_DQS#0
M_A_DQS1
M_A_DQS#1
M_A_DQS2
M_A_DQS#2
M_A_DQS3
M_A_DQS#3
M_A_DQS4
M_A_DQS#4
M_A_DQS5
M_A_DQS#5
M_A_DQS6
M_A_DQS#6
M_A_DQS7
M_A_DQS#7
M_A_BG1
MEM1_E9
MEM1_M9
MEM2_E9
MEM2_M9
MEM3_E9
MEM3_M9
MEM4_E9
MEM4_M9
/DDP
/SDP
0Ohm
240Ohm
0.047UF/10V
1AV200000049
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :DDR4(1)_MEMORY DOWN
Engineer: Bill Yang
Size Custom
Project Name P4
Rev 1.0
Date: Tuesday, September 06, 2016
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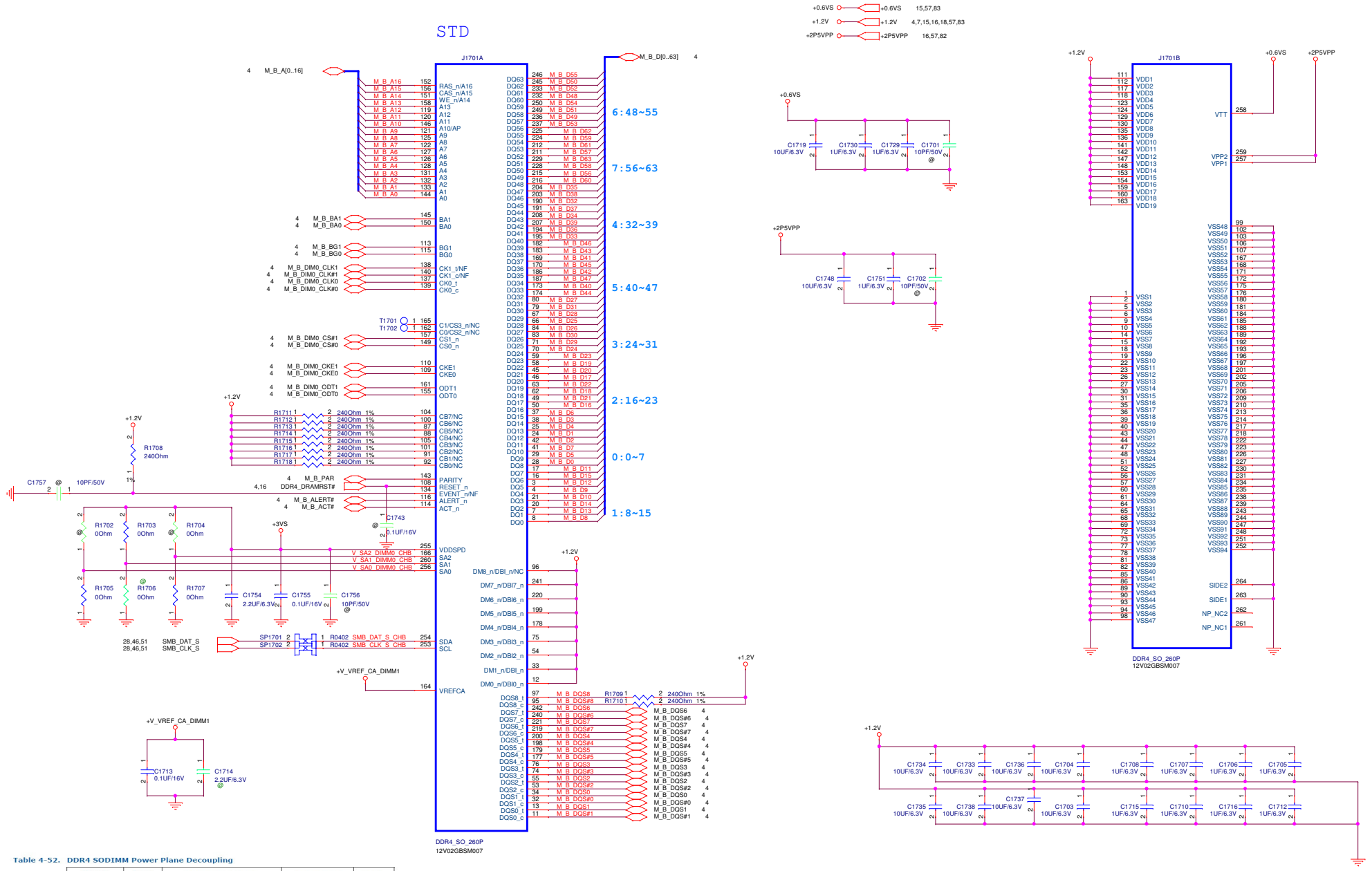

Table 4-52. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

Notes:
1. Total quantity is referring to 2 channels.

<Variant Name>

PEGATRON
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Title :DDR4(1)_SO-DIMM
BG1/HW3
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

+1.2V — +1.2V 4,7,15,16,17,57,83
+V_VREF_CA_DIMM0 — +V_VREF_CA_DIMM0 16
+V_VREF_CA_DIMM1 — +V_VREF_CA_DIMM1 17

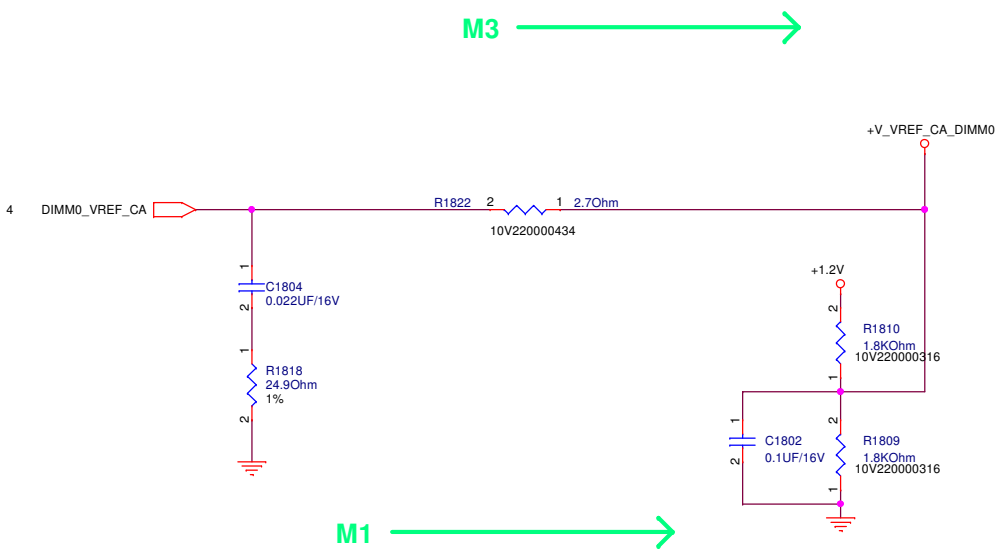
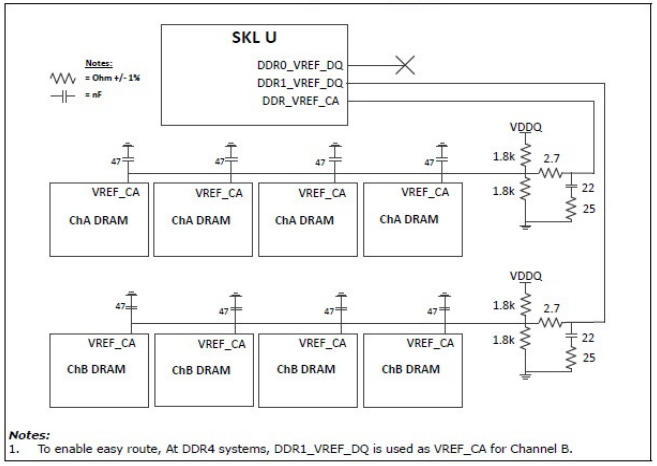


Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down V_{REF-CA} Overview



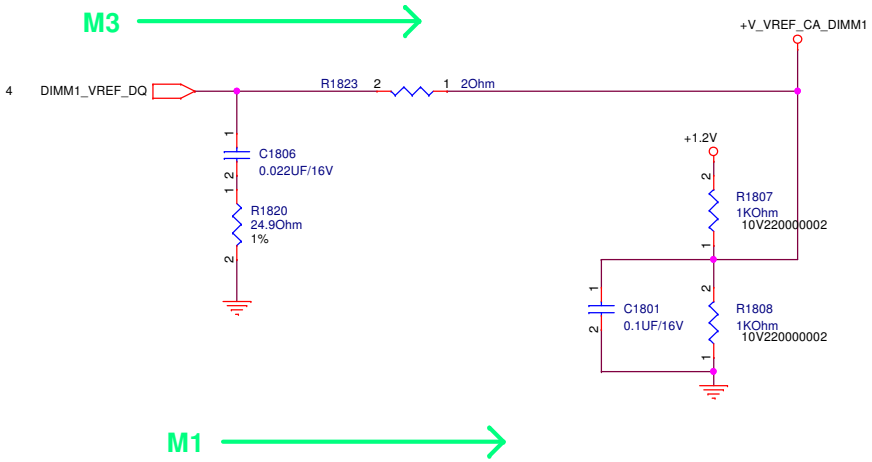
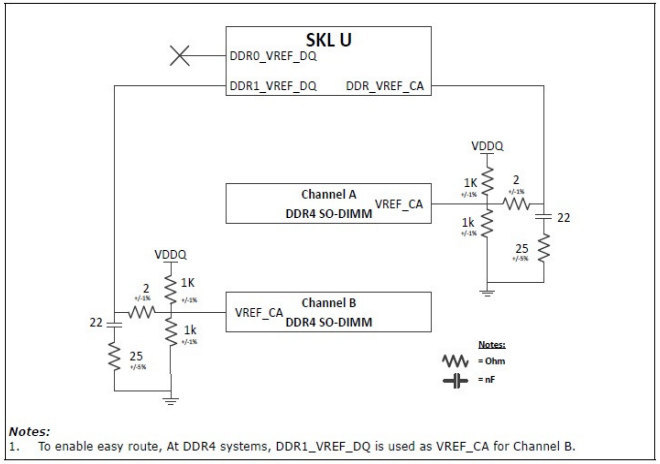


Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(3)_CA/DQ Voltag
Engineer: Bill Yang
BG1/HW3
Size: Custom | Project Name: P4 | Rev: 1.0
Date: Tuesday, September 06, 2016 | Sheet 18 of 108

<Variant Name>

PEGATRON Title :

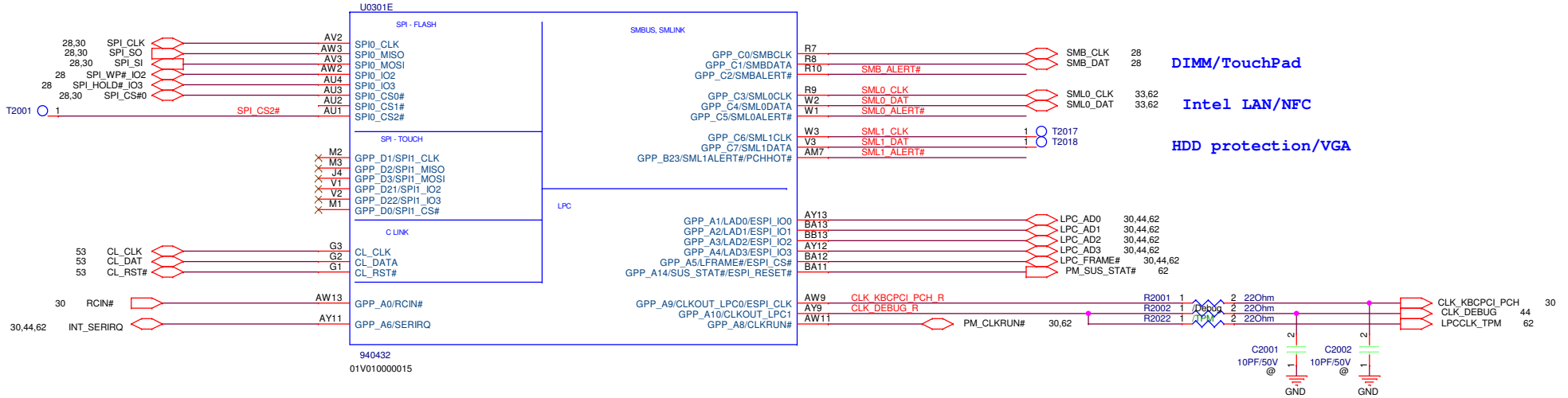
Engineer:

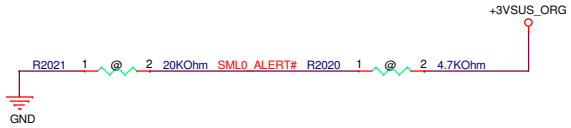
Size	Project Name	Rev
		1.1

Date: Tuesday, September 06, 2016 Sheet 19 of 103

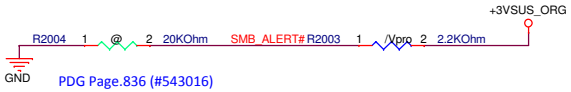
+3VS +3VS 3,4,17,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

+3VSUS_ORG +3VSUS_ORG 21,22,23,25,26





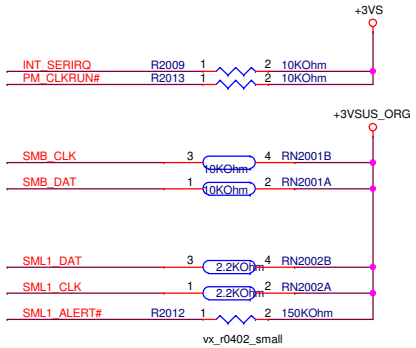
SML0ALERT# - Internal weak pull down
0 : LPC EC (default)
1 : eSPI EC



SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable

PDG Page.836 (#543016)

SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(1)_SMB,LPC

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

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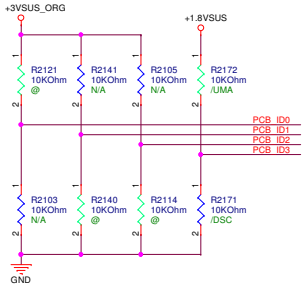
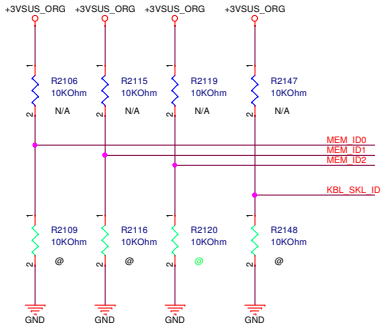
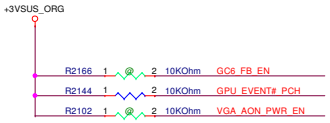


ID2	ID1	ID0	PCB Rev.
0	0	0	R1.0
0	0	1	R1.1
0	1	0	R2.0
0	1	1	R2.1
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

MEM_ID0	MEM_ID1	MEM_ID2	Memory Setting
0	0	0	SAMSUNG/K4A4G165WD-BCPB 4Gb 256Mb*16 0315-01C70PB
1	0	0	HYNIX/H5AN4G6NAFR-UHC 4G 256Mb*16 b0315-01EK0PB
0	1	0	SAMSUNG/K4A8G165WB-BCPB 8Gb 512Mb*16 0315-01HF0PB
1	1	0	HYNIX 8G
0	0	1	SAMSUNG/K4A8G165WB-BCRC 2400 512Mb*16 0315-01C80PB
1	0	1	SK HYNIX/H5AN8G6NAFR-UHC 2400 512Mb*16 0315-01W60PB
0	1	1	MICRON/MT40A512M16JY-083E:B 2400 512Mb*16 0315-01W90PB
1	1	1	DR4 2400 1Gb*16 1.2V FBGA96 MICRON/MT40A1G16WBU-083E:B 0315-01YC0PB

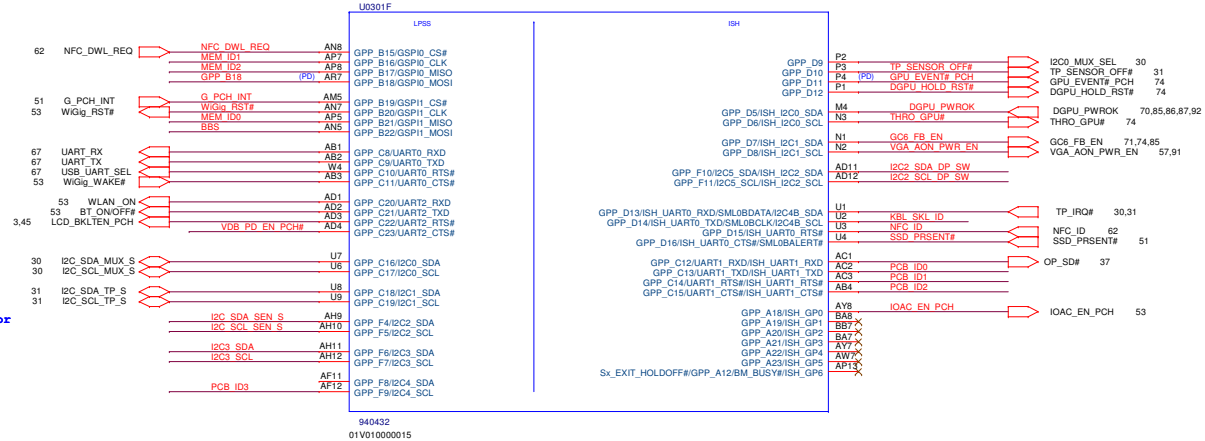
KBL_SKL_ID	SSD_PRSENT#	NFC_ID	PCB_ID3
1:SKL	1: No SSD	1: No NFC	1: UMA
0: KBL	0: SSD	0: NFC	0: DSC

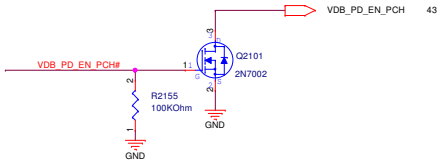


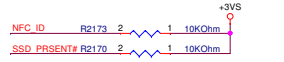


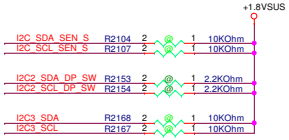
GPIO need to pull high to power with 10Kohm if unused

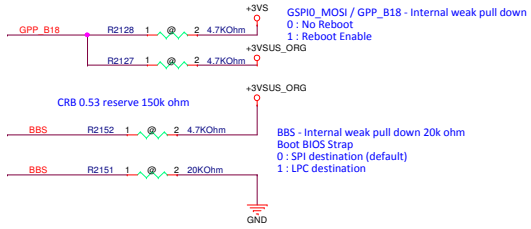
G Sensor

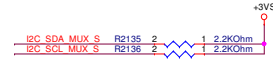












<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

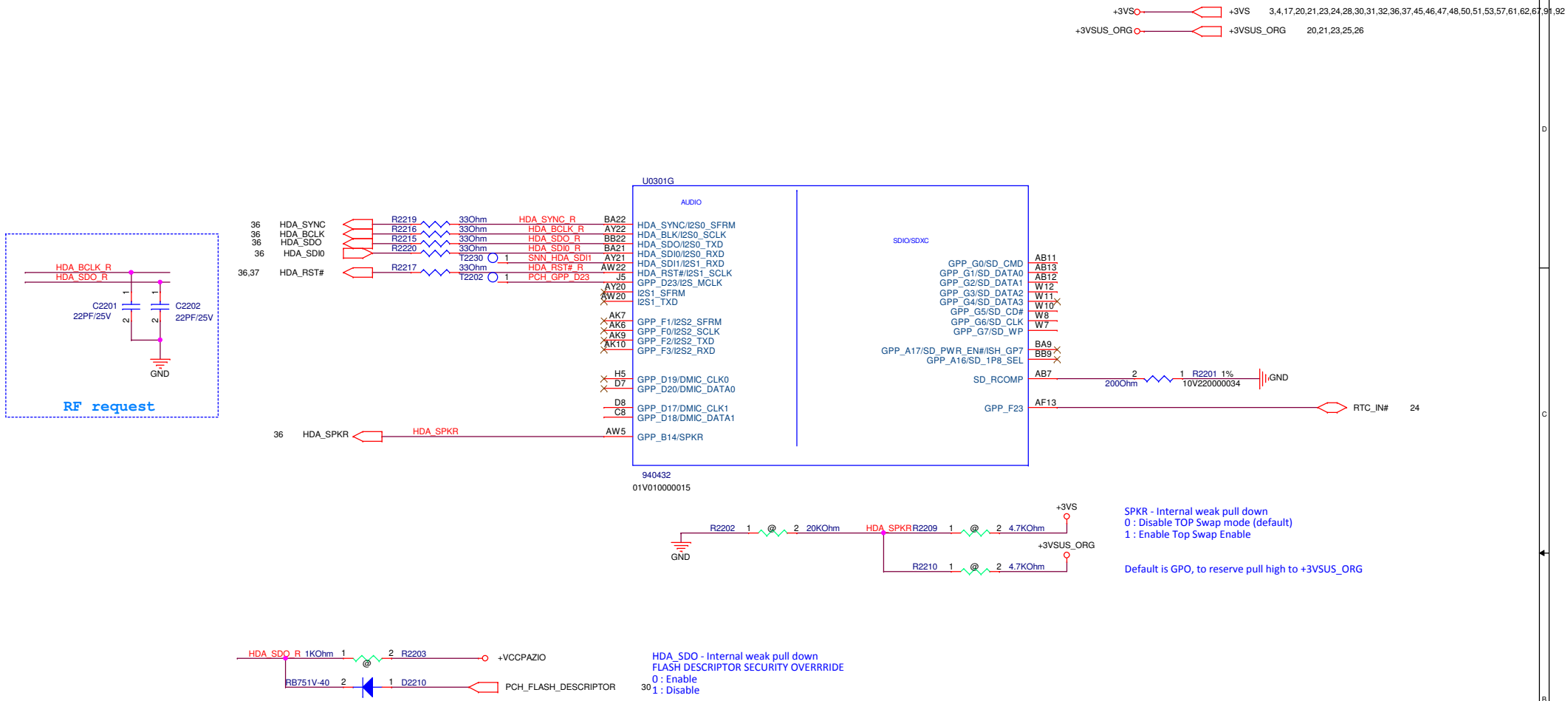
Title : PCH(2) LPSS,ISH

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 21 of 108



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

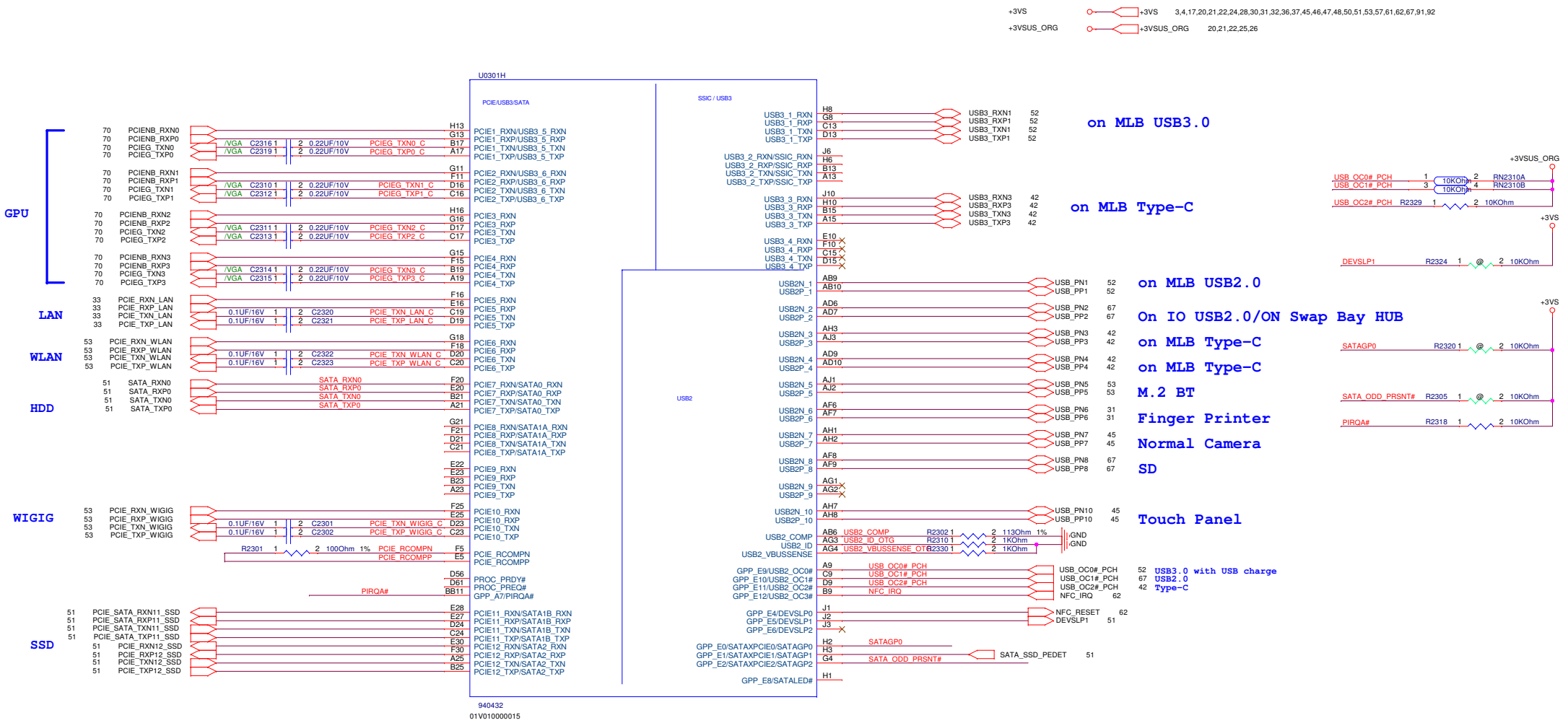
Title : PCH(3),HDA,SDIO

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 22 of 108



3.4.1 SKL PCH U Flexible I/O

Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

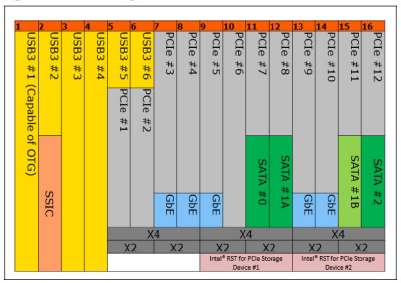
Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Figure 3-1. HSIO Muxing on SKL PCH U



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

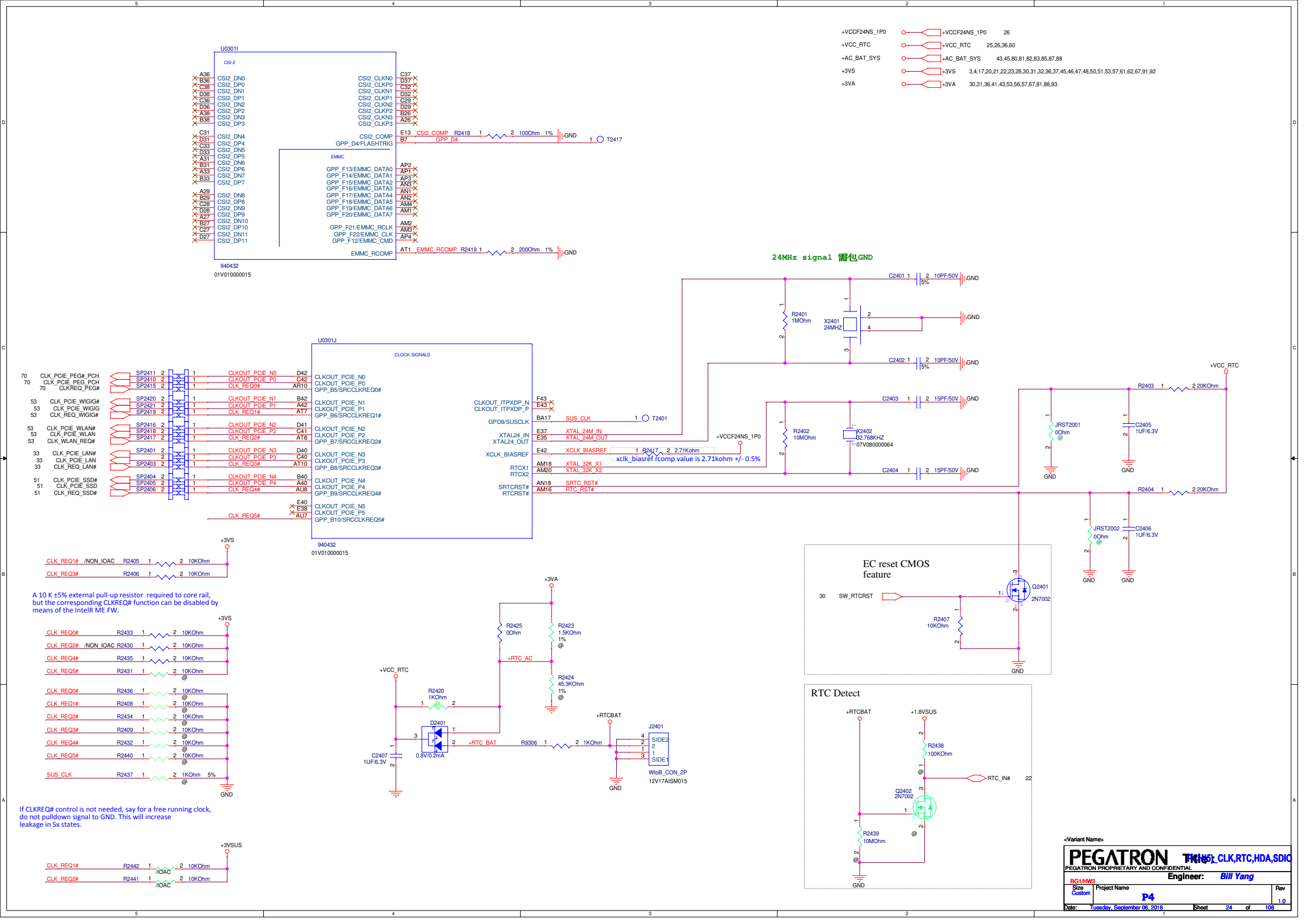
Title : PCH(4) _PCIE,SATA,USB,

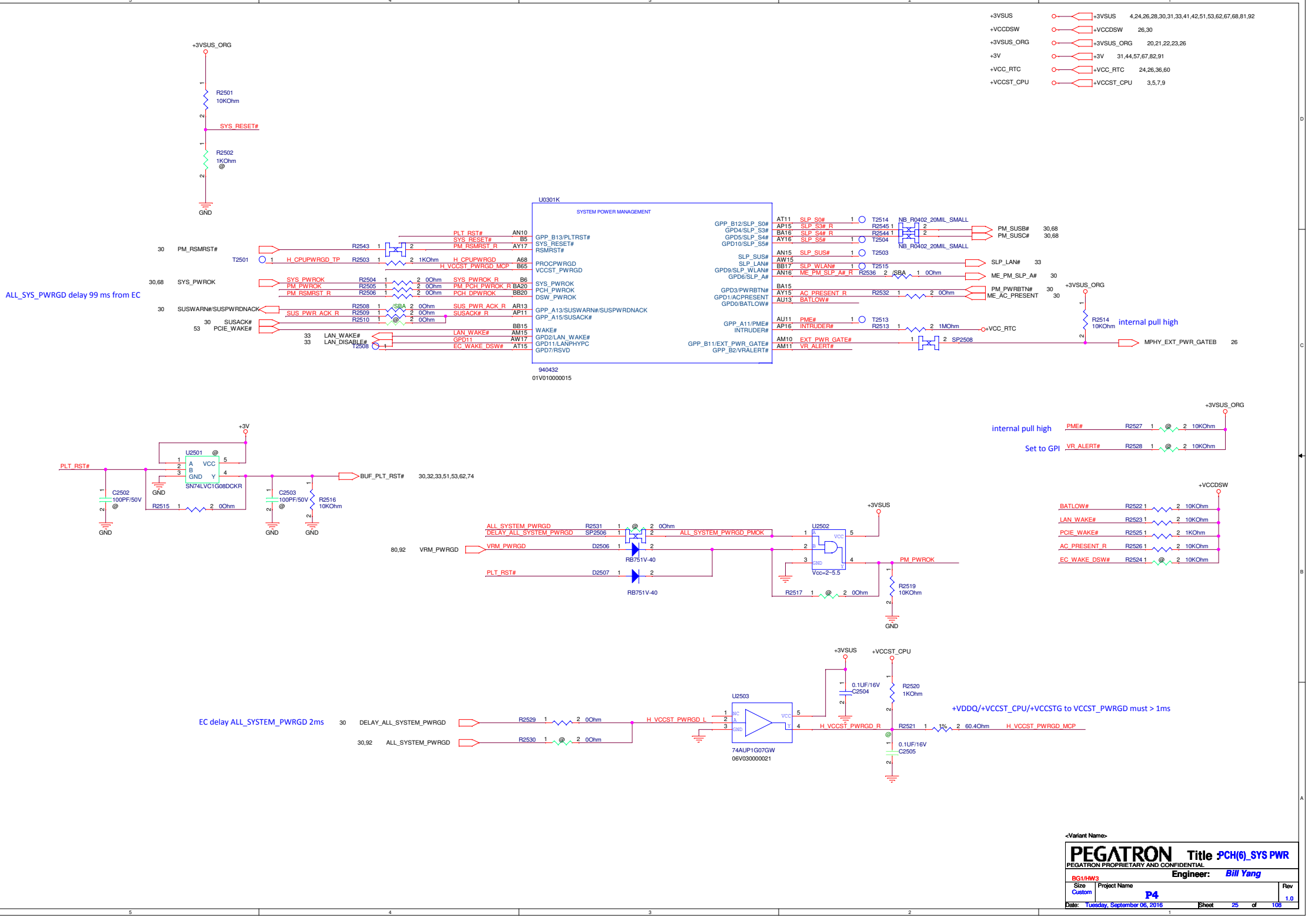
Engineer: Bill Yang

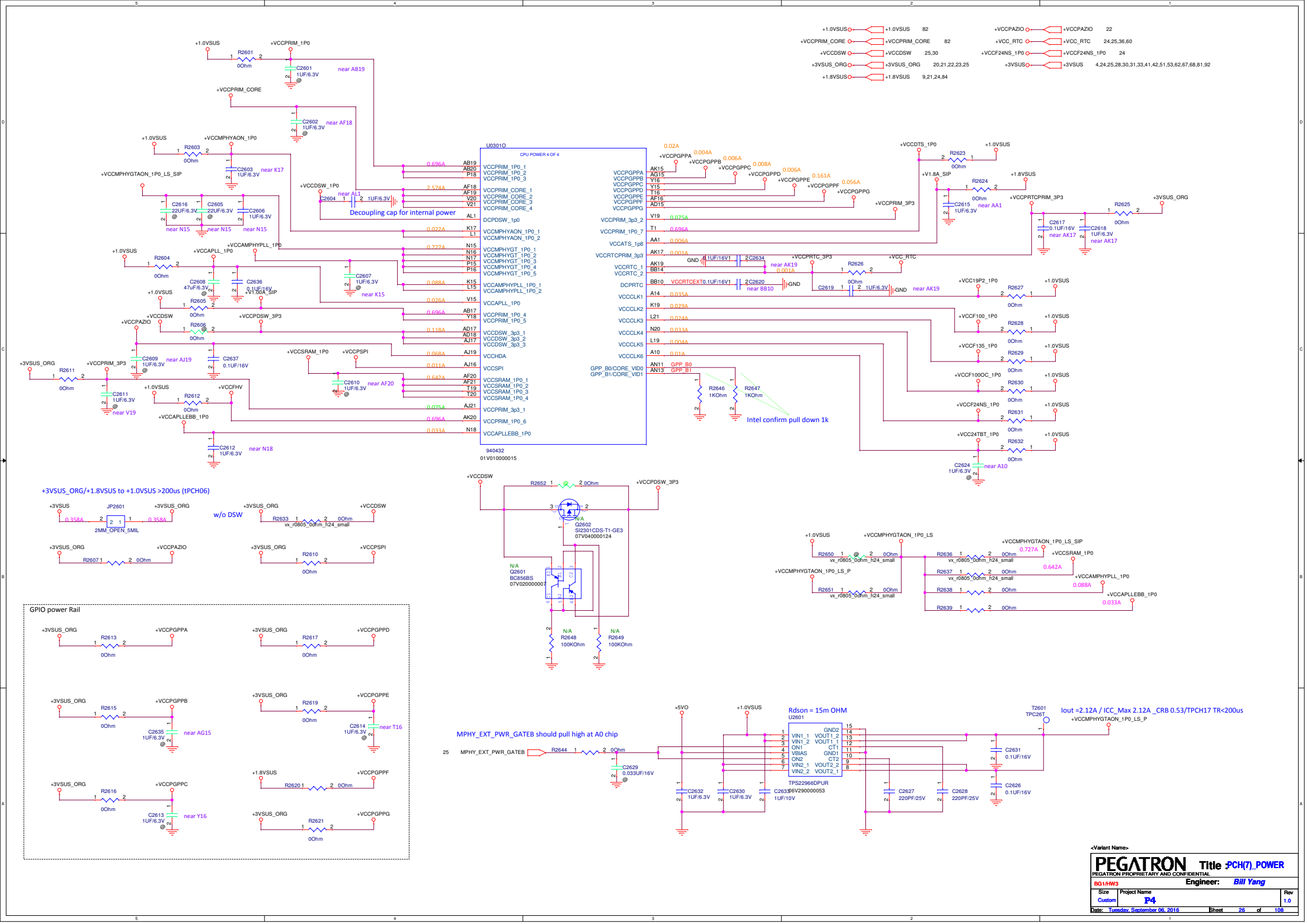
BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 23 of 108


+VCCF24NS_1P0 +VCCF24NS_1P0 26
+VCC_RTC +VCC_RTC 25,26,36,60
+AC_BAT_SYS +AC_BAT_SYS 43,45,80,81,82,83,85,87,88
+3VS +3VS 3,4,17,20,21,22,23,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+3VA +3VA 30,31,36,41,43,53,56,57,67,81,88,93
U0301I
CSI-2
CSI2_DN0 CSI2_DP0 CSI2_DN1 CSI2_DP1 CSI2_DN2 CSI2_DP2 CSI2_DN3 CSI2_DP3
CSI2_DN4 CSI2_DP4 CSI2_DN5 CSI2_DP5 CSI2_DN6 CSI2_DP6 CSI2_DN7 CSI2_DP7
CSI2_DN8 CSI2_DP8 CSI2_DN9 CSI2_DP9 CSI2_DN10 CSI2_DP10 CSI2_DN11 CSI2_DP11
CSI2_CLKN0 CSI2_CLKP0 CSI2_CLKN1 CSI2_CLKP1 CSI2_CLKN2 CSI2_CLKP2 CSI2_CLKN3 CSI2_CLKP3
CSI2_COMP GPP_D4/FLASHTRIG
CSI2_COMP R2418 100Ohm 1% GND
GPP_D4 T2417
EMMC
GPP_F13/EMMC_DATA0 GPP_F14/EMMC_DATA1 GPP_F15/EMMC_DATA2 GPP_F16/EMMC_DATA3 GPP_F17/EMMC_DATA4 GPP_F18/EMMC_DATA5 GPP_F19/EMMC_DATA6 GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK GPP_F22/EMMC_CLK GPP_F12/EMMC_CMD
EMMC_RCOMP EMMC_RCOMP R2419 200Ohm 1% GND
940432
01V010000015
24MHz signal 需包GND
U0301J
CLOCK SIGNALS
CLK_PCIE_PEG# CLK_PCIE_PEG CLKREQ_PEG#
SP2411 SP2410 SP2415
CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 CLK_REQ0# D42 C42 AR10
CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
CLK_PCIE_WIGIG# CLK_PCIE_WIGIG CLK_REQ_WIGIG#
SP2420 SP2421 SP2419
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 CLK_REQ1# B42 A42 AT7
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
CLK_PCIE_WLAN# CLK_PCIE_WLAN CLK_WLAN_REQ#
SP2416 SP2418 SP2417
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 CLK_REQ2# D41 C41 AT8
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#
CLK_PCIE_LAN# CLK_PCIE_LAN CLK_REQ_LAN#
SP2401 SP2403
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 CLK_REQ3# D40 C40 AT10
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#
CLK_PCIE_SSD# CLK_PCIE_SSD CLK_REQ_SSD#
SP2404 SP2405 SP2406
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 CLK_REQ4# B40 A40 AU8
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#
CLK_REQ5# E40 E38 AU7
CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P
GPD8/SUSCLK SUS_CLK T2401
XTAL24_IN XTAL24_OUT XTAL_24M_IN XTAL_24M_OUT
XCLK_BIASREF XCLK_BIASREF R2417 2.71Kohm
xclk_biasref rcomp value is 2.71kohm +/- 0.5%
RTCX1 RTCX2 XTAL_32K_X1 XTAL_32K_X2
SRTCRST# RTCRST# SRTC_RST# RTC_RST#
940432
01V010000015
C2401 10PF/50V 5% GND
R2401 1MOhm
X2401 24MHZ
C2402 10PF/50V 5% GND
C2403 15PF/50V GND
R2402 10MOhm
X2402 32.768KHZ 07V080000064
C2404 15PF/50V GND
+VCCF24NS_1P0
+VCC_RTC
R2403 20KOhm
JRST2001 0Ohm @
C2405 1UF/6.3V
R2404 20KOhm
JRST2002 0Ohm @
C2406 1UF/6.3V
GND
+3VS
CLK_REQ1# /NON_IOAC R2405 10KOhm
CLK_REQ3# R2406 10KOhm
A 10 K ±5% external pull-up resistor required to core rail, but the corresponding CLKREQ# function can be disabled by means of the IntelR ME FW.
+3VS
CLK_REQ0# R2433 10KOhm
CLK_REQ2# /NON_IOAC R2430 10KOhm
CLK_REQ4# R2435 10KOhm
CLK_REQ5# R2431 10KOhm @
CLK_REQ0# R2436 10KOhm @
CLK_REQ1# R2408 10KOhm @
CLK_REQ2# R2434 10KOhm @
CLK_REQ3# R2409 10KOhm @
CLK_REQ4# R2432 10KOhm @
CLK_REQ5# R2440 10KOhm @
SUS_CLK R2437 1KOhm 5% @ GND
If CLKREQ# control is not needed, say for a free running clock, do not pulldown signal to GND. This will increase leakage in Sx states.
+3VSUS
CLK_REQ1# R2442 /IOAC 10KOhm
CLK_REQ2# R2441 /IOAC 10KOhm
+3VA
R2425 0Ohm
R2423 1.5KOhm 1% @
+RTC_AC
R2424 45.3KOhm 1% @
+VCC_RTC
R2420 1KOhm @
D2401 0.8V/0.2mA
+RTC_BAT
R9306 1KOhm
C2407 1UF/6.3V
+RTCBAT
J2401 SIDE2 SIDE1
WtoB_CON_2P
12V17AISM015
GND
EC reset CMOS feature
30 SW_RTCRST
Q2401 2N7002
R2407 10KOhm
GND
RTC Detect
+RTCBAT
+1.8VSUS
R2438 100KOhm
RTC_IN# 22
Q2402 2N7002
R2439 10MOhm
GND
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: CLK,RTC,HDA,SDIO
Engineer: Bill Yang
BG1/MW3
Size Custom
Project Name P4
Rev 1.0
Date: Tuesday, September 06, 2016
Sheet 24 of 108


+3VSUS +3VSUS 4,24,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+VCCDSW +VCCDSW 26,30
+3VSUS_ORG +3VSUS_ORG 20,21,22,23,26
+3V +3V 31,44,57,67,82,91
+VCC_RTC +VCC_RTC 24,26,36,60
+VCCST_CPU +VCCST_CPU 3,5,7,9
+3VSUS_ORG
R2501 10KOhm
SYS_RESET#
R2502 1KOhm @
GND
U0301K
SYSTEM POWER MANAGEMENT
940432
01V010000015
ALL_SYS_PWRGD delay 99 ms from EC
PM_RSMRST#
T2501
H_CPUPWRGD_TP
R2543
R2503 1KOhm
PLT_RST#
SYS_RESET#
PM_RSMRST_R
H_CPUPWRGD
H_VCCST_PWRGD_MCP
SYS_PWROK
PM_PWROK
PM_RSMRST_R
R2504 R2505 R2506 0Ohm
SYS_PWROK_R
PM_PCH_PWROK_R
PCH_DPWROK
SUSWARN#/SUSPWRDNACK
SUS_PWR_ACK_R
R2508 R2509 R2510 SBA
SUS_PWR_ACK_R
SUSACK#_R
SUSACK#
PCIE_WAKE#
LAN_WAKE#
LAN_DISABLE#
T2508
GPD11
EC_WAKE_DSW#
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
SLP_S0# SLP_S3# SLP_S4# SLP_S5#
T2514 T2545 T2544 T2504
NB_R0402_20MIL_SMALL
PM_SUSB# PM_SUSC#
SLP_SUS# T2503
SLP_LAN# SLP_WLAN# T2515
ME_PM_SLP_A# R2536 SBA
ME_PM_SLP_A#
PM_PWRBTN#
AC_PRESENT_R R2532 0Ohm
ME_AC_PRESENT
BATLOW#
PME# T2513
INTRUDER# R2513 1MOhm
+VCC_RTC
EXT_PWR_GATE# SP2508
VR_ALERT#
R2514 10KOhm
internal pull high
MPHY_EXT_PWR_GATEB
+3V
U2501
SN74LVC1G08DCKR
PLT_RST#
BUF_PLT_RST#
C2502 100PF/50V @
C2503 100PF/50V @
R2515 0Ohm
R2516 10KOhm
internal pull high
Set to GPI
PME# R2527 10KOhm
VR_ALERT# R2528 10KOhm
+VCCDSW
BATLOW# R2522 10KOhm
LAN_WAKE# R2523 10KOhm
PCIE_WAKE# R2525 1KOhm
AC_PRESENT_R R2526 10KOhm
EC_WAKE_DSW# R2524 10KOhm
ALL_SYSTEM_PWRGD R2531 0Ohm
DELAY_ALL_SYSTEM_PWRGD SP2506
ALL_SYSTEM_PWRGD_PMOK
VRM_PWRGD
VRM_PWRGD D2506
PLT_RST# D2507
RB751V-40
RB751V-40
U2502
Vcc=2~5.5
PM_PWROK
R2517 0Ohm
R2519 10KOhm
EC delay ALL_SYSTEM_PWRGD 2ms
DELAY_ALL_SYSTEM_PWRGD
ALL_SYSTEM_PWRGD
R2529 R2530 0Ohm
H_VCCST_PWRGD_L
U2503
74AUP1G07GW
06V030000021
0.1UF/16V C2504
R2520 1KOhm
H_VCCST_PWRGD_R
R2521 60.4Ohm
H_VCCST_PWRGD_MCP
0.1UF/16V C2505
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :PCH(6)_SYS PWR
Engineer: Bill Yang
BG1/HW3
Size Custom
Project Name P4
Rev 1.0
Date: Tuesday, September 06, 2016
Sheet 25 of 108



+1.0VSUS	+1.0VSUS 82	+VCCPAZIO	+VCCPAZIO 22
+VCCPRIM_CORE	+VCCPRIM_CORE 82	+VCC_RTC	+VCC_RTC 24,25,36,60
+VCCDSW	+VCCDSW 25,30	+VCCF24NS_1P0	+VCCF24NS_1P0 24
+3VSUS_ORG	+3VSUS_ORG 20,21,22,23,25	+3VSUS	+3VSUS 4,24,25,28,30,31,33,41,42,51,53,62,67,68,81,92
+1.8VSUS	+1.8VSUS 9,21,24,84		

<Variant Name>

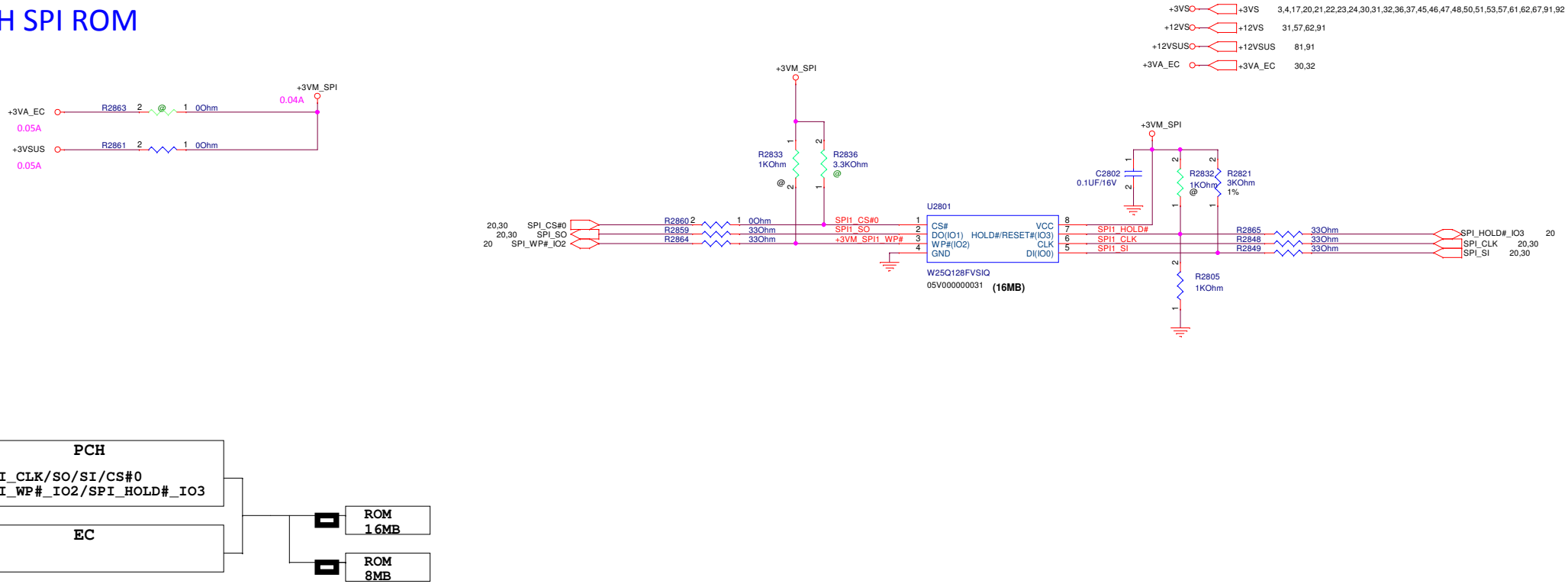
PEGATRON Title :

Engineer:

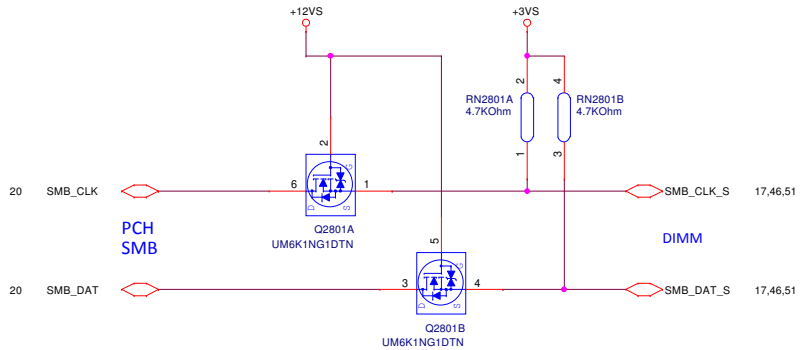
Size	Project Name	Rev
		1.1

Date: Tuesday, September 06, 2016 Sheet 27 of 103

PCH SPI ROM



PCH SMBus



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: PCH(8)_SPI,SMB

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 28 of 108

<Variant Name>

PEGATRON Title :

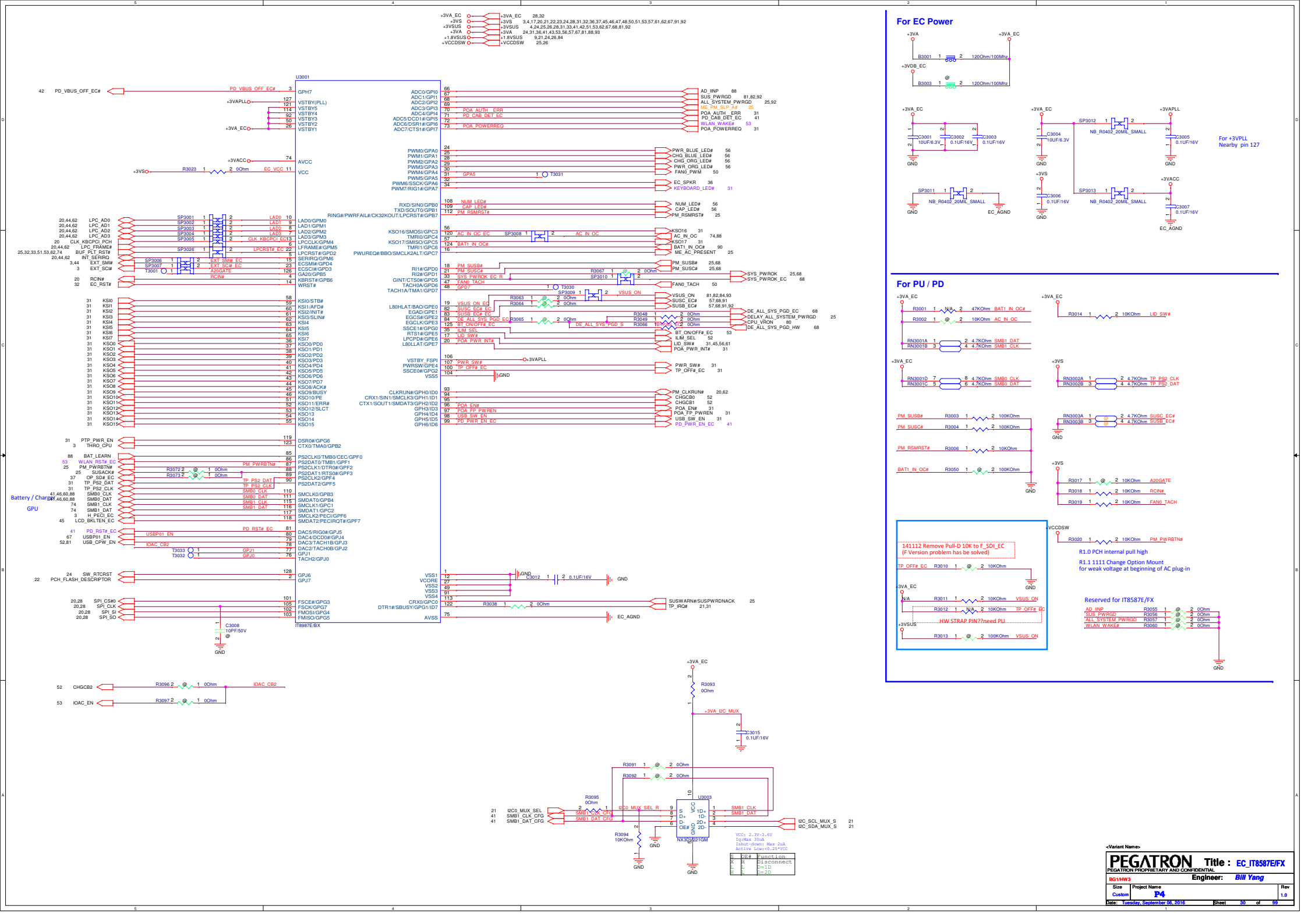
PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

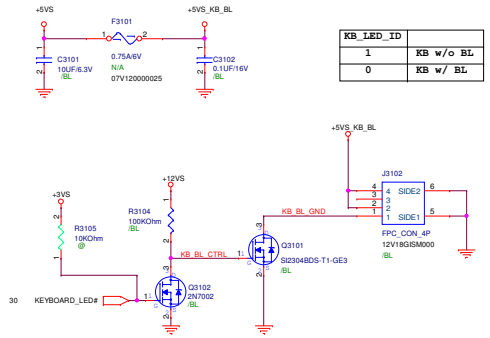
Date: Tuesday, September 06, 2016 Sheet 29 of 108



For EC Power

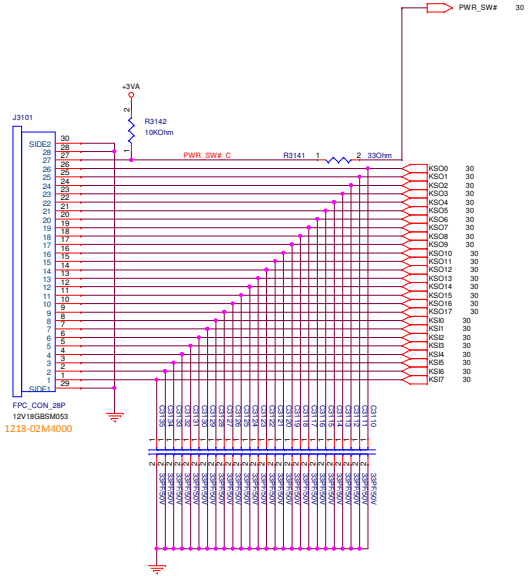
For PU / PD

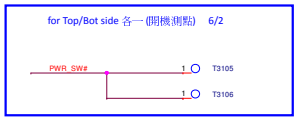
Keyboard LED

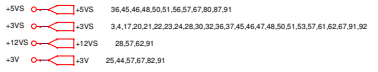


KB_LED_ID	
1	KB w/o BL
0	KB w/ BL

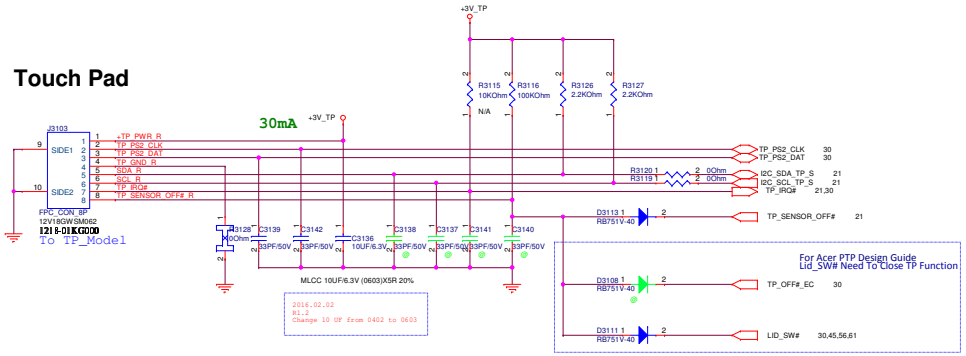
Keyboard

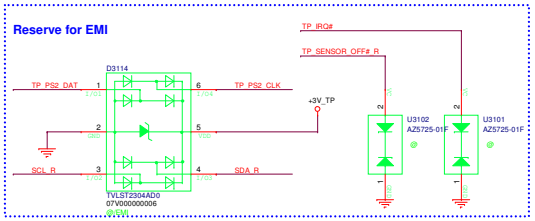


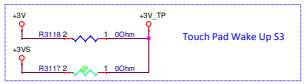


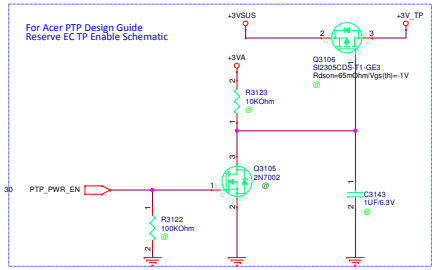


Touch Pad

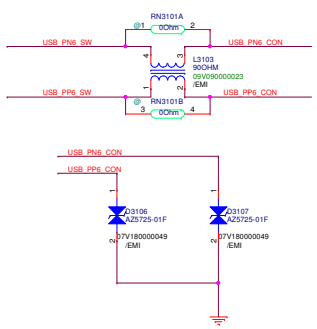


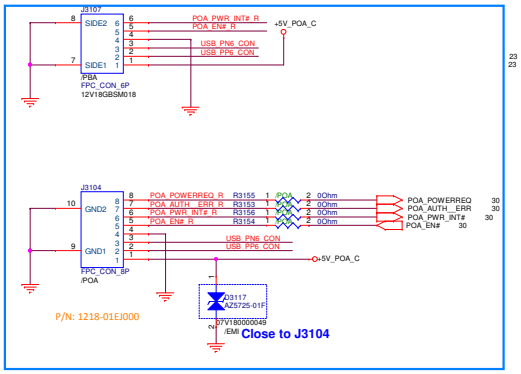




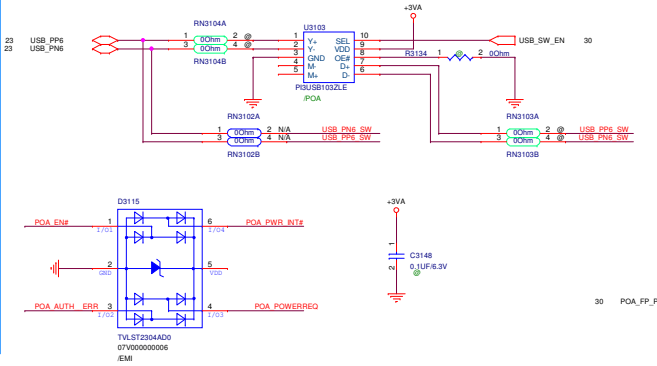


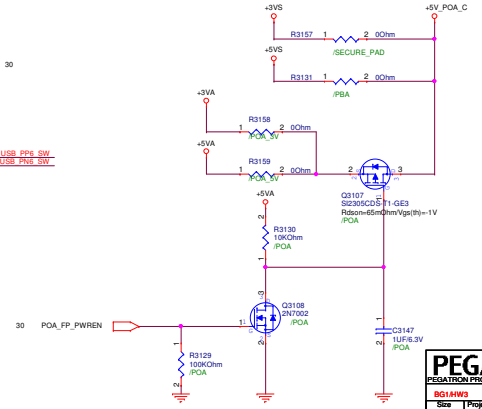
Finger Print





J3107.1 and J3104.1 colay





PEGATRON Title : TP / KB / FP

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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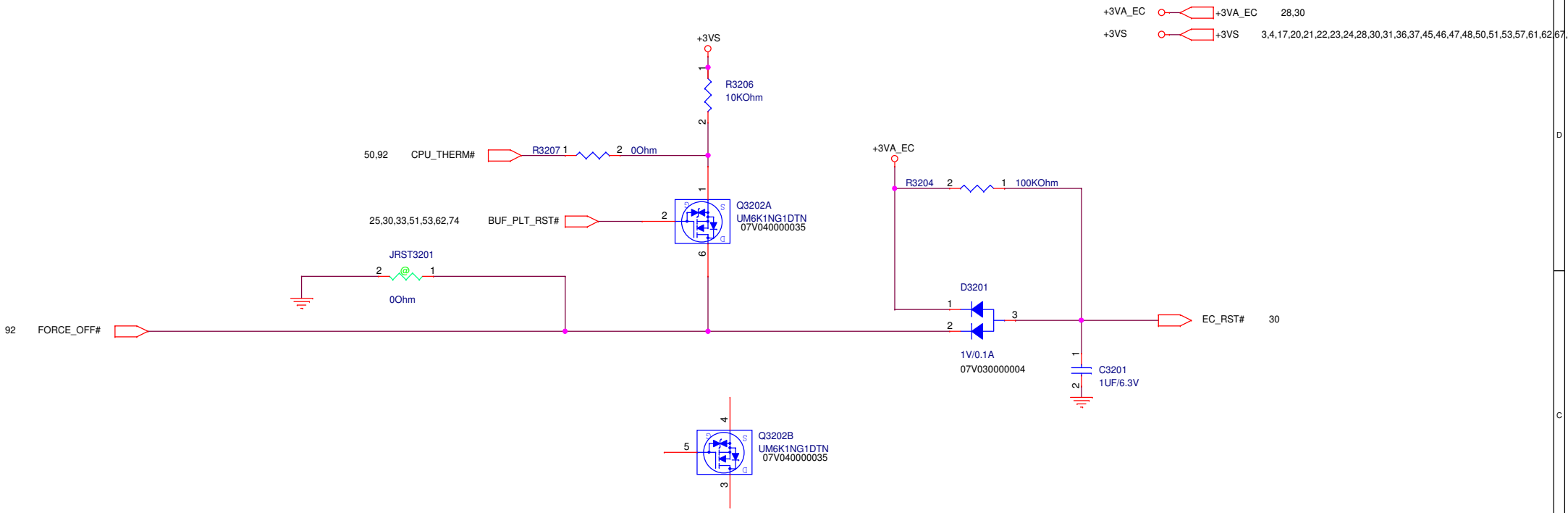


Remove 10s RTC reset

PEGATRON PROPRIETARY AND CONFIDENTIAL

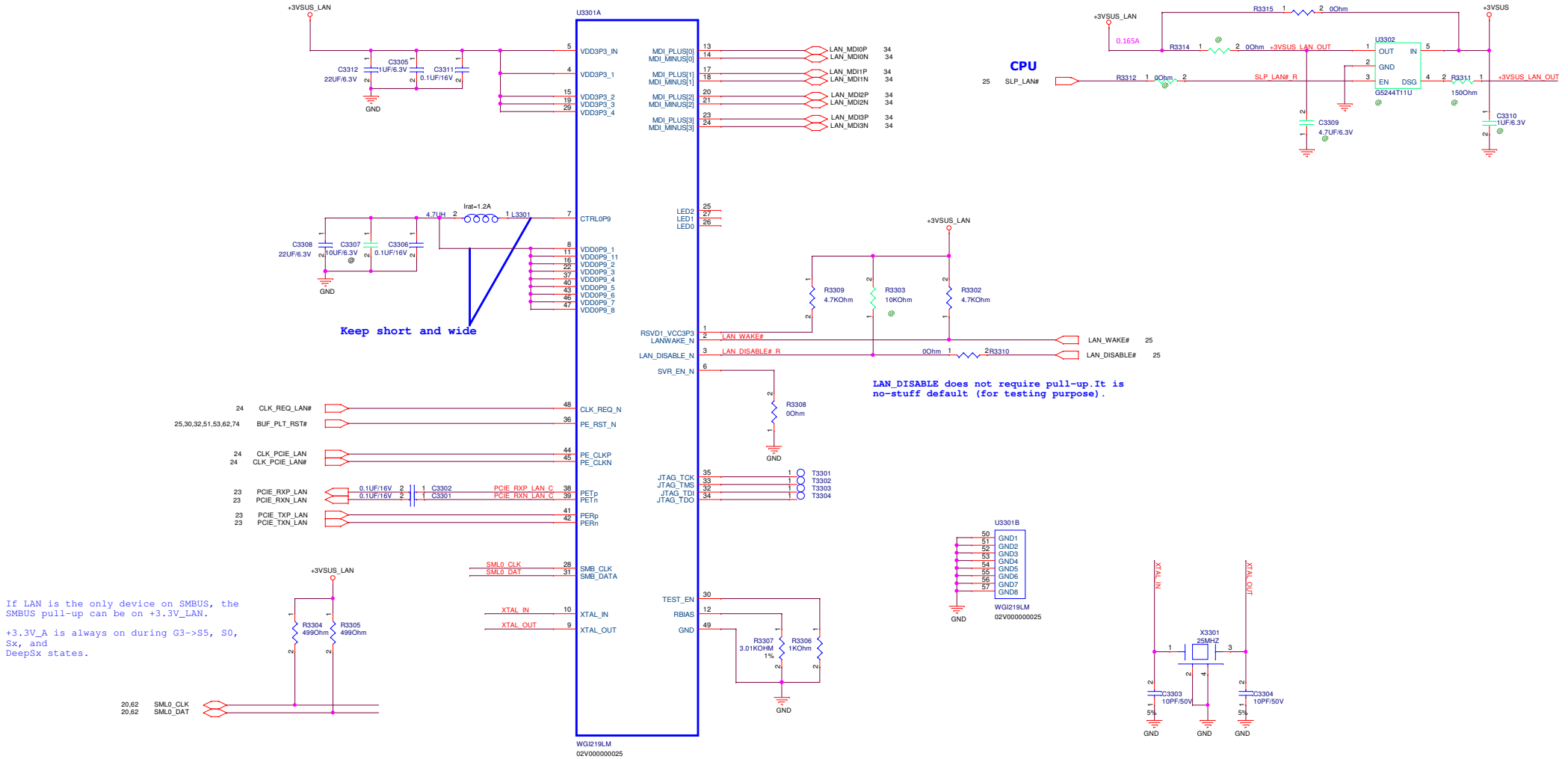
PEGATRON Title : RST_Reset Circuit

Engineer: Bill Yang

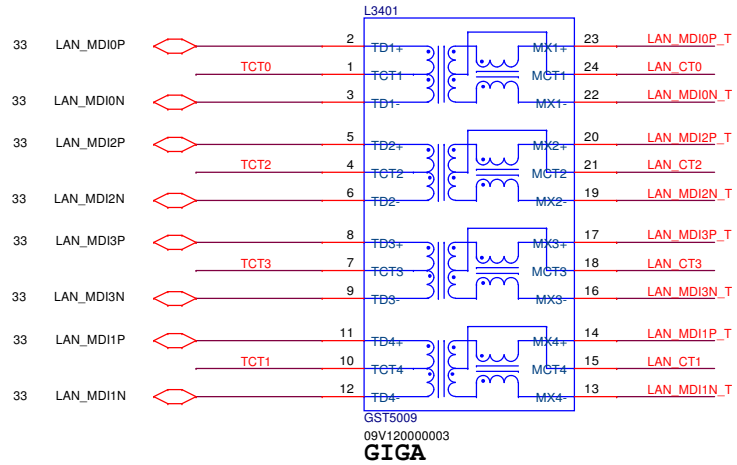
BG1/HW3

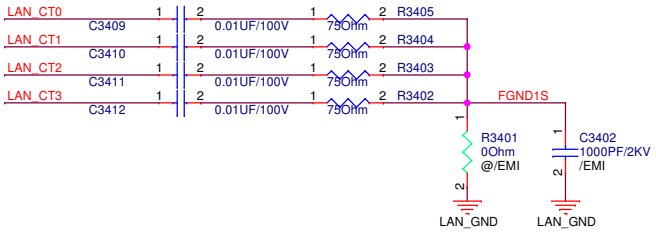
Size	Project Name	Rev
Custom	P4	1.0

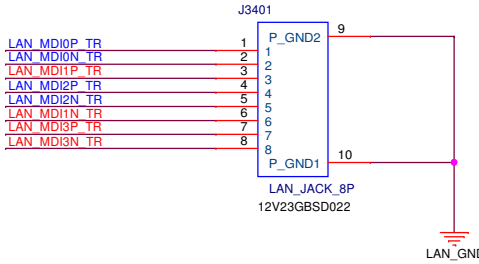
Date: Tuesday, September 06, 2016 Sheet 32 of 108

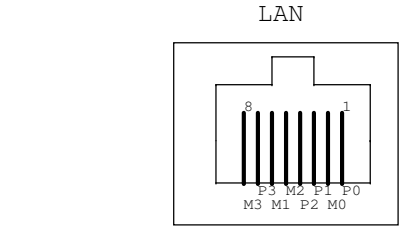


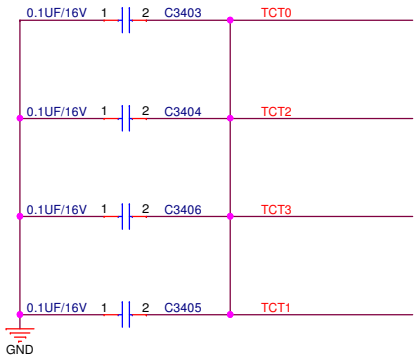
PEGATRON	Title : Intel/I219		
BG1\HW3	Engineer: Bill Yang		
Size: Custom	Project Name: P4		Rev: 1.0
	P/N		
Date: Tuesday, September 06, 2016	Sheet 33 of 108		

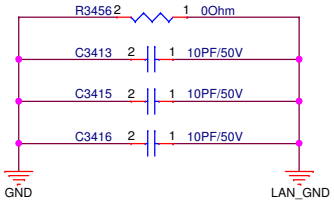


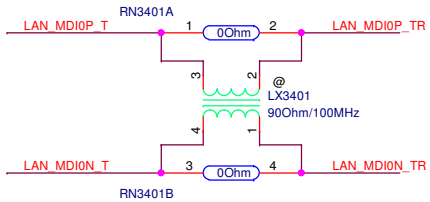


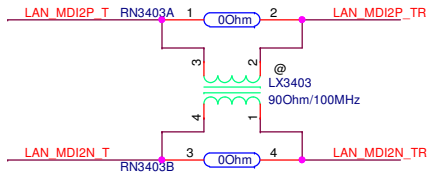


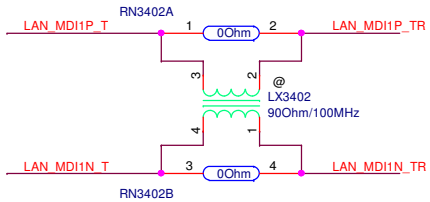


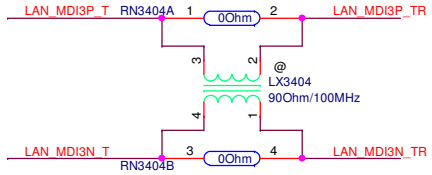


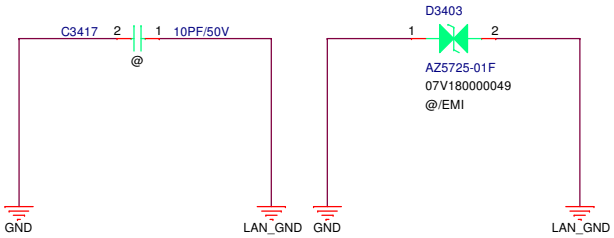












Place near chassis GND

PEGATRON	Title : RJ45	
BG1\HW3	Engineer: Bill Yang	
Size: Custom	Project Name: P4	Rev: 1.0
	P/N	
Date: Tuesday, September 06, 2016	Sheet 34 of 108	

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

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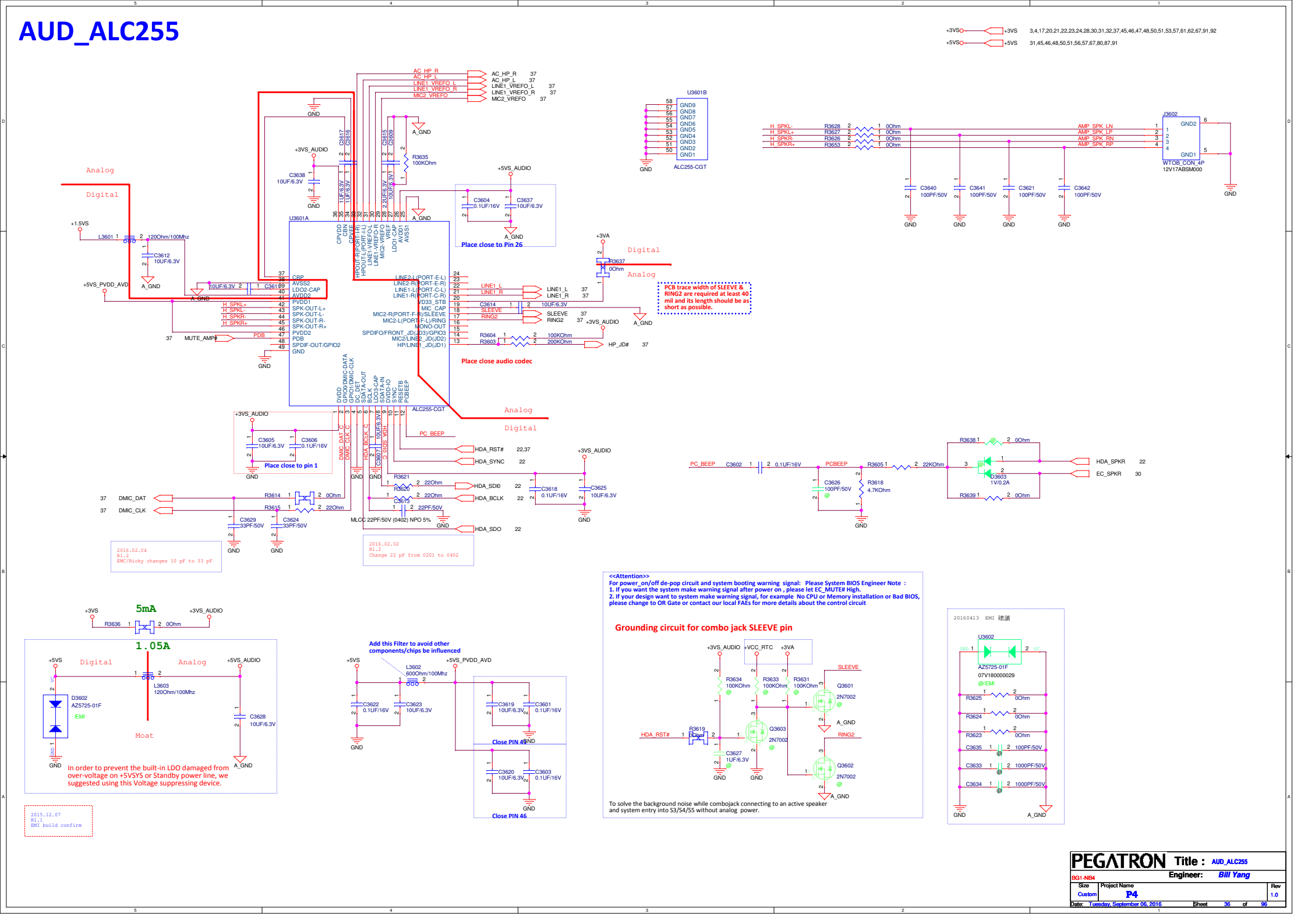
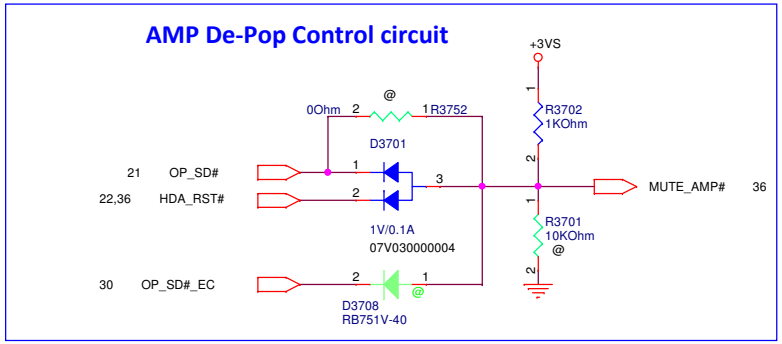
AUD_ALC255

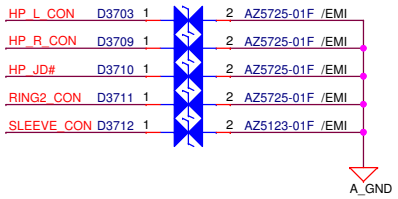


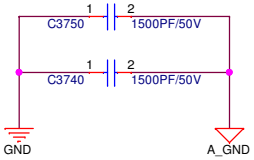
PEGATRON	Title : AUD_ALC255		
BG1-NB4	Engineer: Bill Yang		
Size: Custom	Project Name: P4		Rev: 1.0
Date: Tuesday, September 06, 2016	Sheet 36 of 96		

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,45,46,47,48,50,51,53,57,61,62,67,91,92

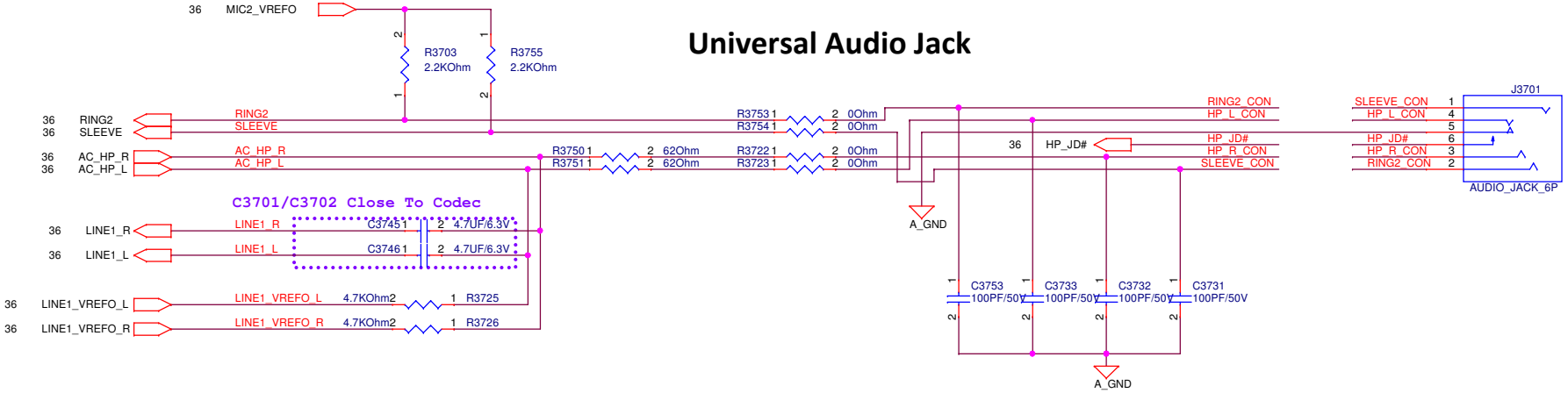
AMP De-Pop Control circuit



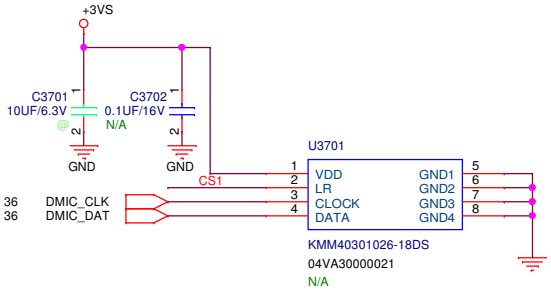




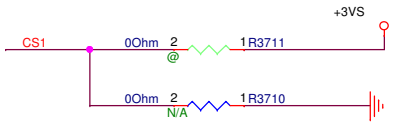
Universal Audio Jack

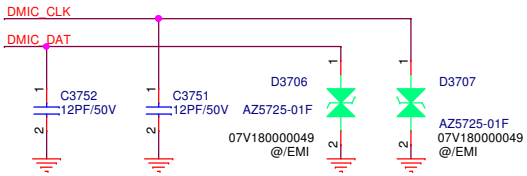


DMIC



Single MIC	Left Channel	Right Channel
CS Pin	Pull Down	Pull Up





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : COMBO_JACK

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 37 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

Date: Tuesday, September 06, 2016 Sheet 38 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

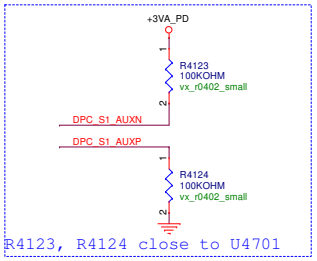
Engineer:

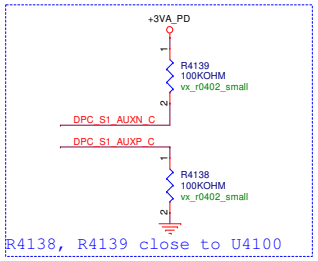
Size	Project Name	Rev
C	KTKUG_25W	1.1

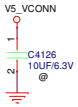
Date: Tuesday, September 06, 2016 Sheet 39 of 108

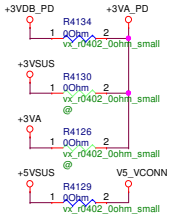
Title	<Title>
Size: A	Document Number: <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
Sheet	40 of 108

ANX7428









VBUS_USB_TYPE_C	VBUS_USB_TYPE_C	42,43
+3VA	+3VA	24,30,31,36,43,53,56,57,67,81,88,93
+3VA_PD	+3VA_PD	42
+3VSUS	+3VSUS	4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92
+3VDB_PD	+3VDB_PD	43

The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.

V5_VCONN is the power source for VCONN(UTC_B5_CC2 or UTC_A5_CC1).
Please make sure:
1) VCONN Voltage range [4.75V, 5.5V]
2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.

Reverse voltage protection is required.
It might be necessary to add a diode to protect the power supply.

Requirement of Q3:
1) Id >= 500mA (Vgs = - 4.5V).
2) Ron < 120 mOhm (Vgs = - 4.5V).
3) Max Vds >= -10V

Connect to DP Source

Connect to USB3.0 signals

Connect to USB Type-C connector

M_SDA/GPIO_5 pin:
Connect to AP/CPU/Charge IC as a charge mode indicator.

Logic 0: Fast Charger Mode, charge voltage > 5V or charge current >= 1.5A.

Logic 1: Normal Charger Mode, charge voltage = 5V and charge current <1.5A.

DRP_EN pin:
Logic 1: DRP Mode.
Logic 0: DFP Mode.

INTP_OUT pin: interrupt output.
Connect to AP or CPU.

If AP or GPU's interrupt is low level triggered, set R16 = 4.7K, leave R22 not installed;
else if is high level triggered, set R22 =4.7K, leave R16 not installed.

Change to 0650-007L000

I2C_ADR_1/GPIO_3 pin: Connected to AP or CPU as UART TXD
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used as software UART output after OCM boot.

CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.

Note:
1. Set R21 = 100K, C15 = 22nF to filter the short high toggle pulse in DRP mode when cable is unplugged in ES chip.
2. Set R21 to 0R, C15 to DNP when this is fixed in CS chip.

I2C_ADR_0/INTP_IN/GPIO_2:
Connect to AP or CPU to control the discharge of VBUS.
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used for VBUS discharge control after OCM boot.

PWR_EN pin:
Controlled by AP or CPU
Logic 1: to power up the chip.
Logic 0: to power down the chip.

I2C Address Selection:

I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

I2C_ADR_1 and I2C_ADR_0 pin:
1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

<Variant Name>

PEGATRON
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Title : POWER_FLOWCHART
Engineer: Bill Yang

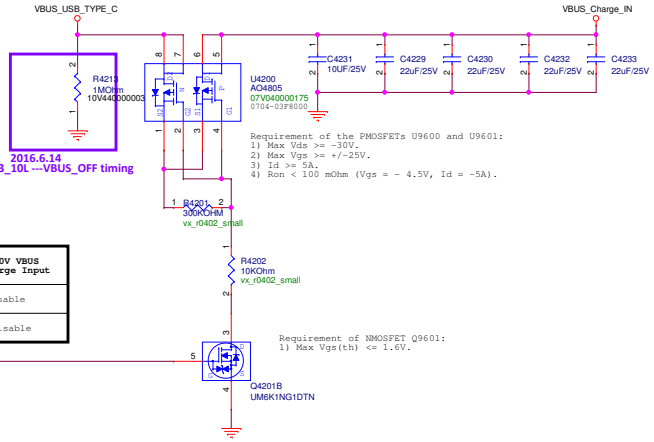
Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 41 of 97

VBUS Control

Optional:
If PMIC can detect VBUS presence and disable/enable VBUS, the VBUS control circuit can be removed.

5V VBUS Output Control



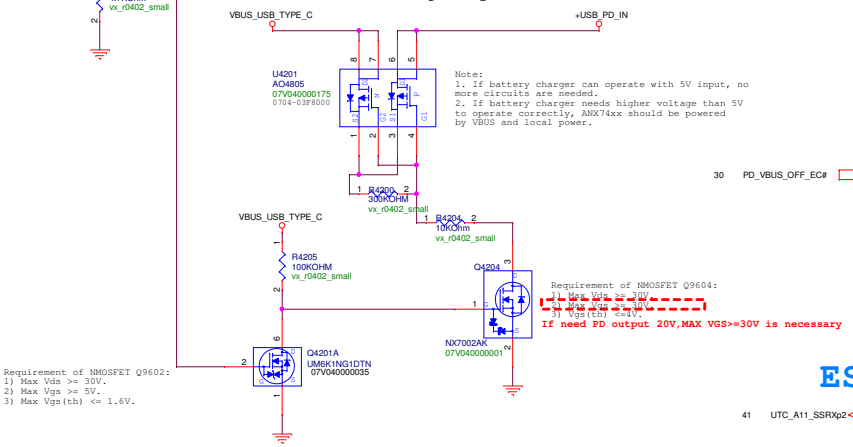
VBUS_CTRL Function:

VBUS_CTRL	5V VBUS Output	5~20V VBUS Charge Input
Logic 0	Disable	Enable
Logic 1	Enable	Disable

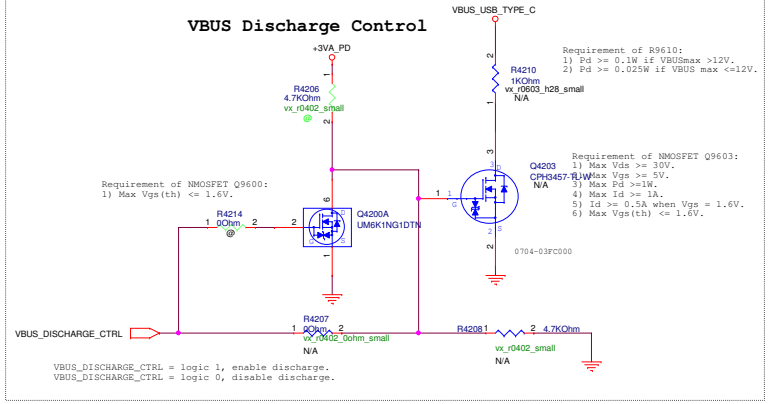
41,89 PD_VBUS_CTRL

R4203 4.7KOhm vx_r0402_small

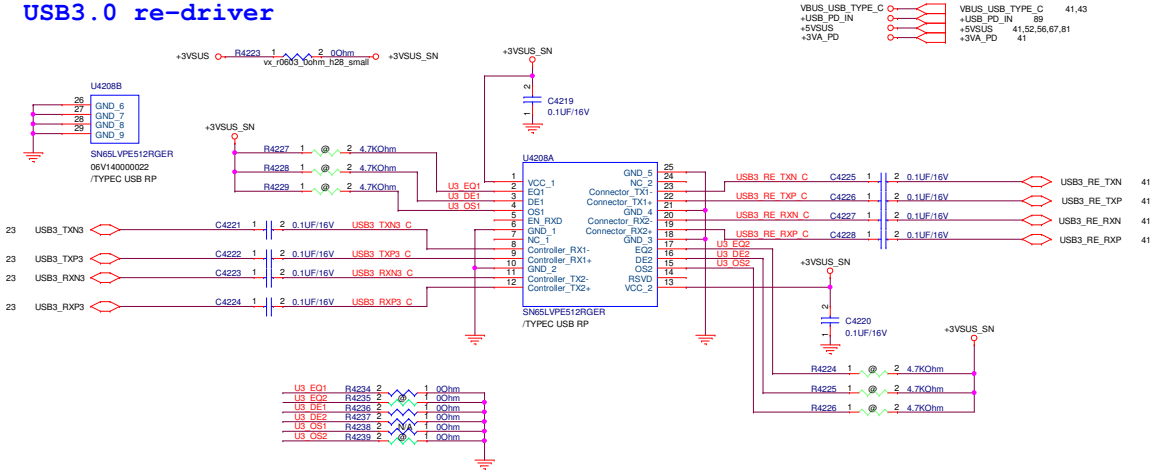
5~20V VBUS Charge Input Control

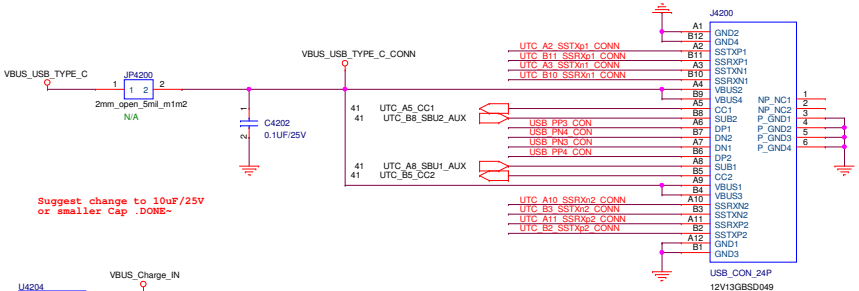


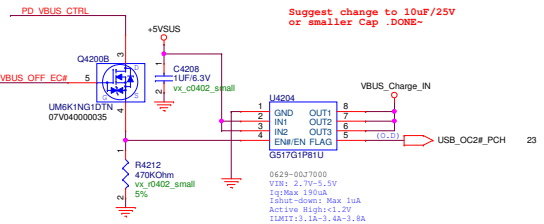
VBUS Discharge Control



USB3.0 re-driver



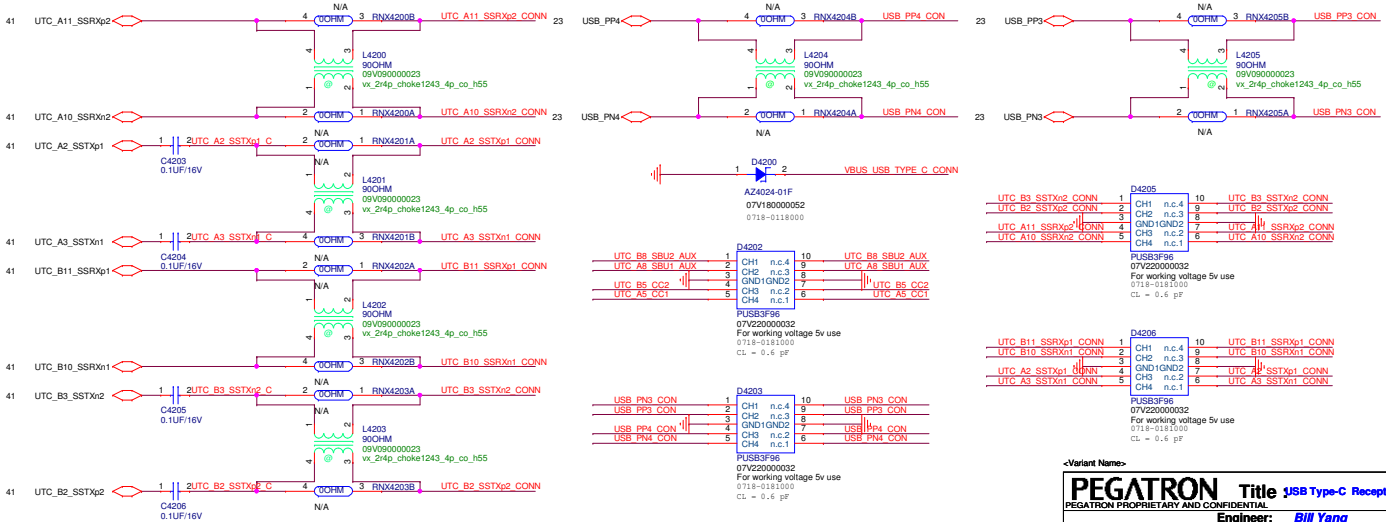




USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

ESD

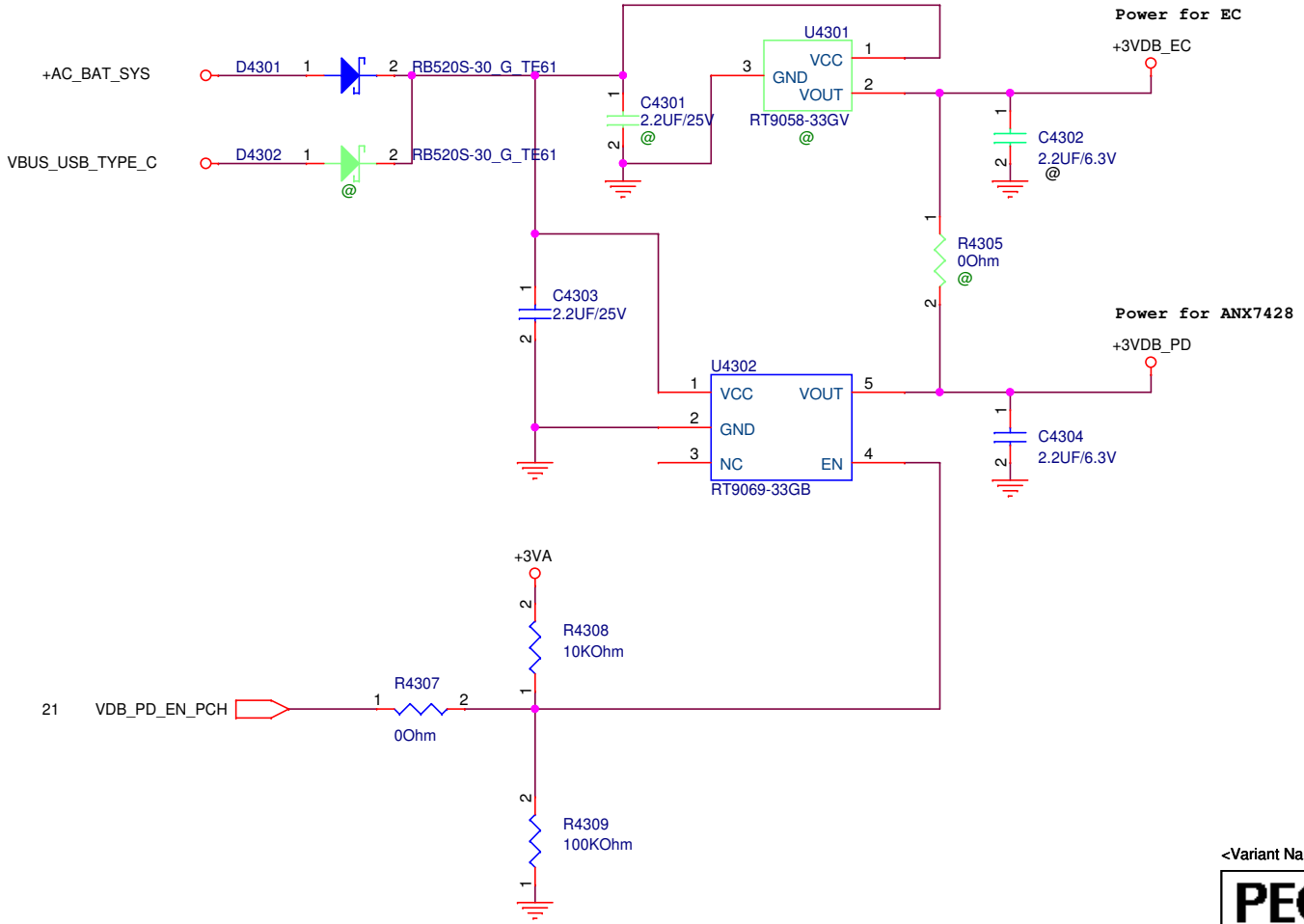


Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C	VBUS_USB_TYPE_C	41,42	
+AC_BAT_SYS	+AC_BAT_SYS	45,80,81,82,83,85,87,88	
+3VDB_EC	+3VDB_EC	30	
+3VDB_PD	+3VDB_PD	41	

Requirement of U1:
1) Vin range: 4V~30V.
2) Vout: EC's operating voltage + Vf of D1
3) Output current >= EC's operating current.



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

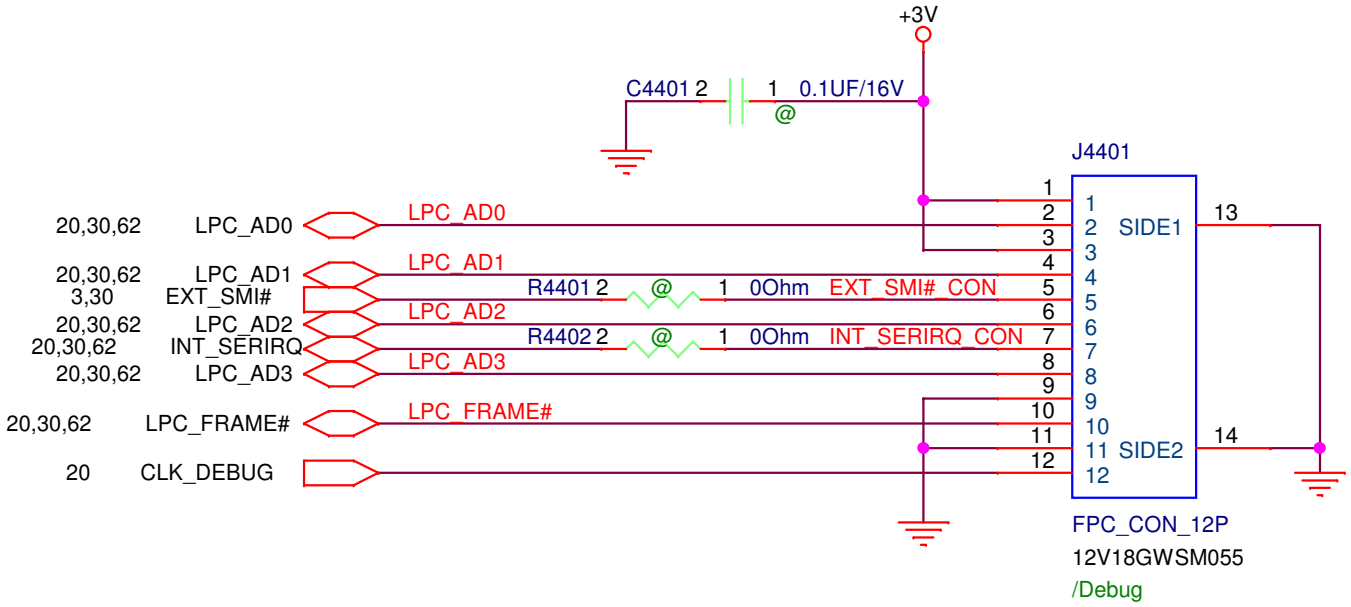
Title : Dead Battery

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 43 of 97

+3V +3V 25,31,57,67,82,91



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : BUG_Debug

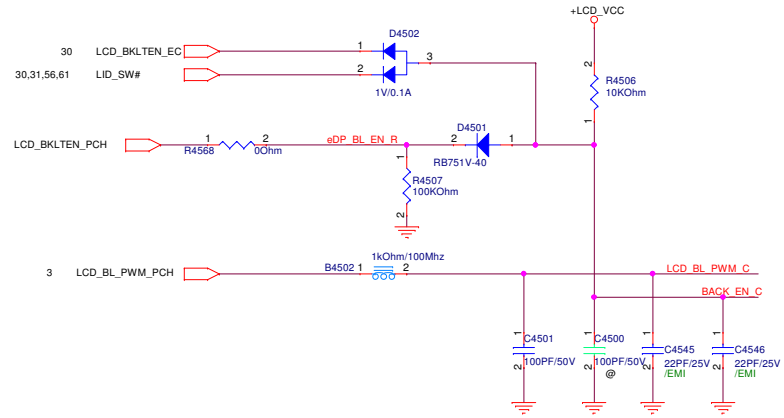
Engineer: Bill Yang

BG1/HW3

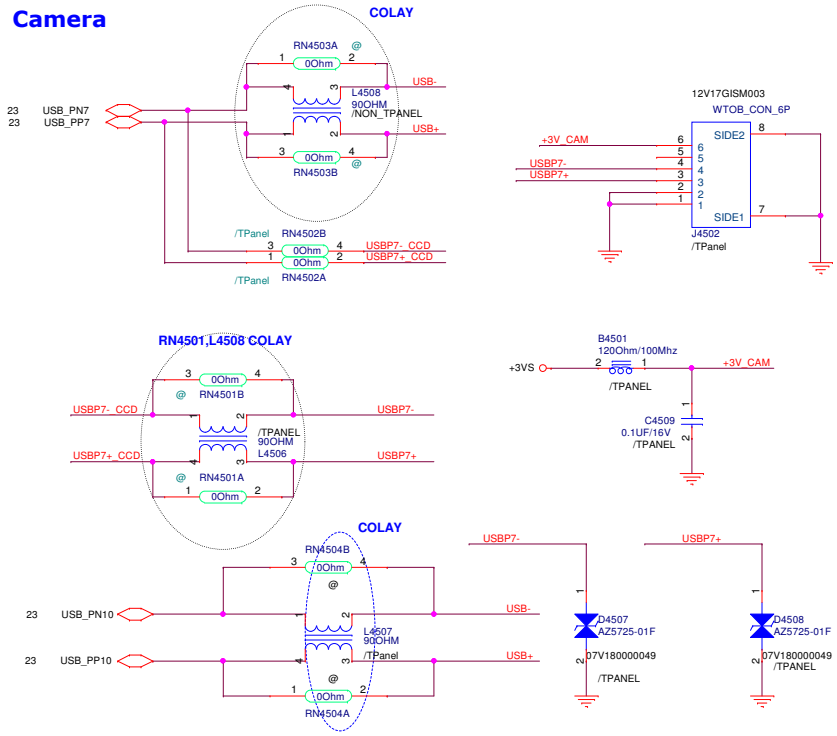
Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 44 of 108

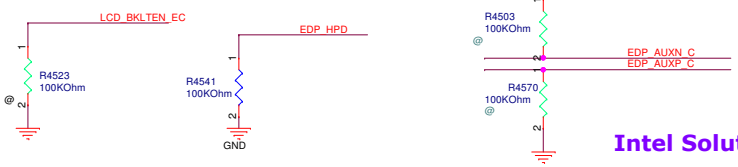
Controller circuit

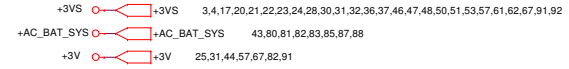


Camera

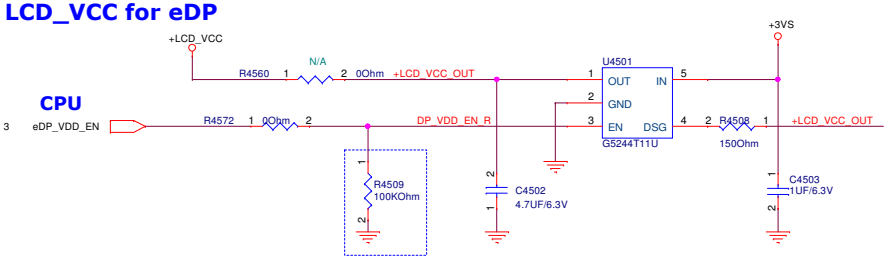


eDP HPD

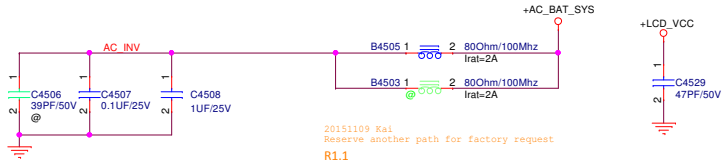




LCD_VCC for eDP

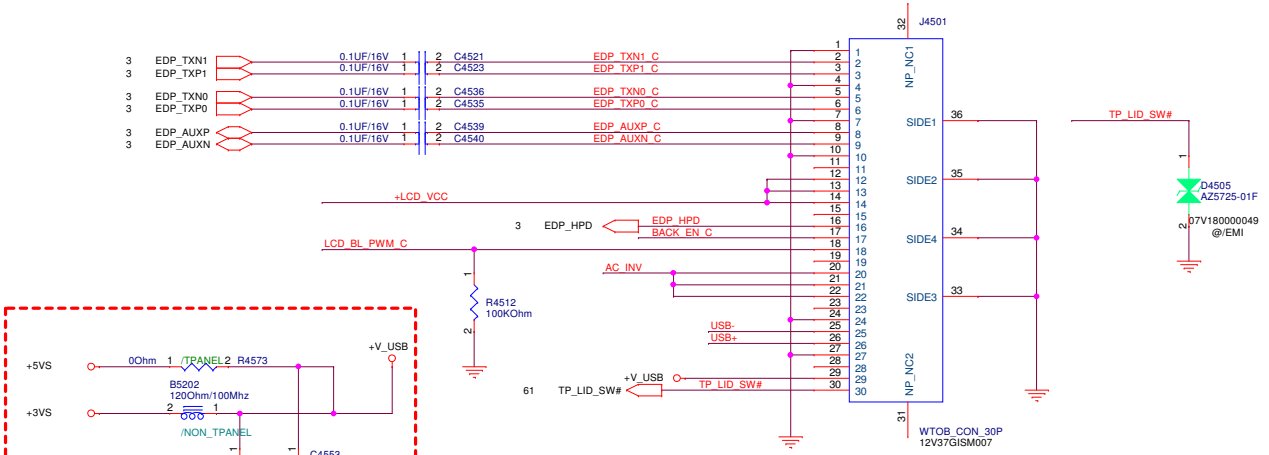


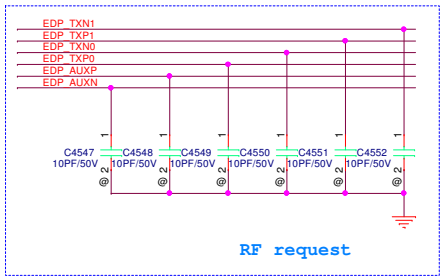
Check PCH/FCH or CPU PD

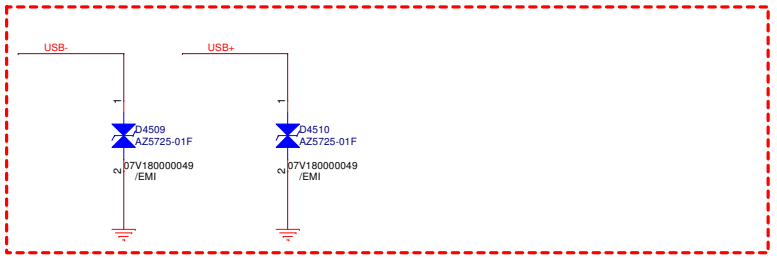


eDP Connector

NOTE:
Entire trace of Panel_VCC & LCD_VCC should be wider than 80-mil







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LVDS Out

BG1\HW3

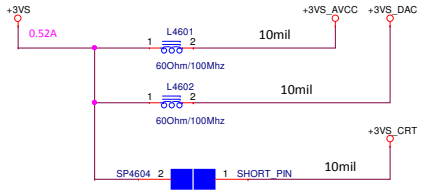
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 45 of 108

DP2VGA Realtek RTD2166

Power



Rom / Flash Mode :

		POL1 (Pin10)	
		0	1
POL2 (Pin9)	0	No Use	No Use
	1	**(V) Rom mode**	Ext Flash mode

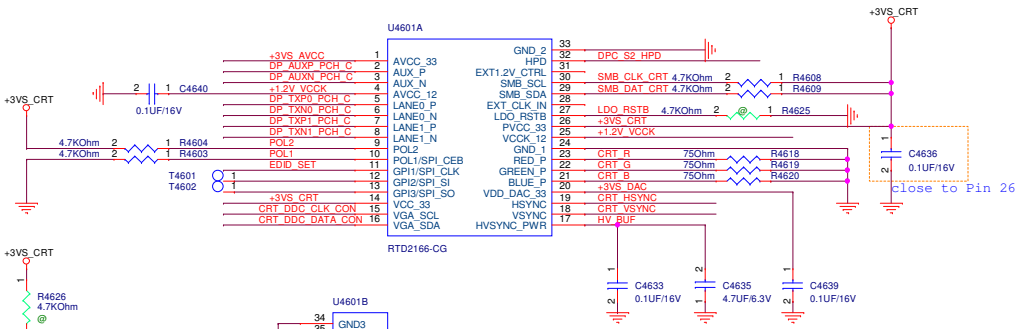
Embedded EDID setting :

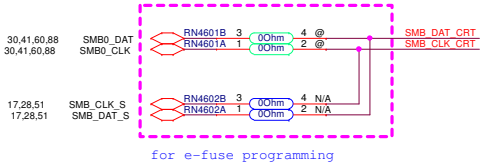
EDID_SET (Pin11)	Mode
0 or NC	**(V) Disable RTD2166 Embedded EDID**
1	Enable RTD2166 Embedded EDID

LDO Mode :

LDO_RSTB (Pin27)	Mode
1 or NC	**(V) embedded LD0 Mode**
0	External 1.2V Mode

1: Pull High 0: Pull Down

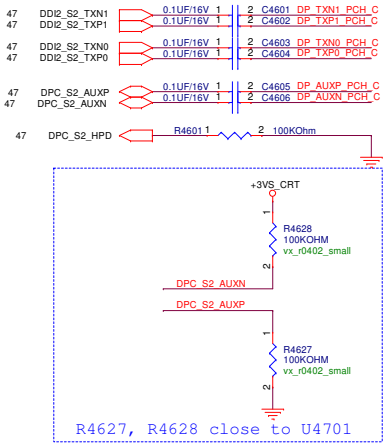




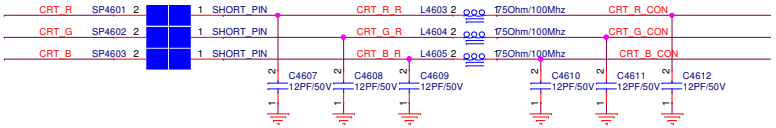
CRT_HV Sync Voltage setting :
R4605 : 5V
R4606 : 3.3V

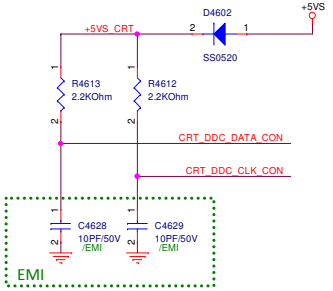
CPU Interface

DP main link total length < 8 inch
VIA < 2

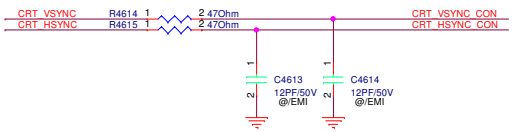


Max mismatch between RGB signal < 200 mil,
total trace length < 6 inch

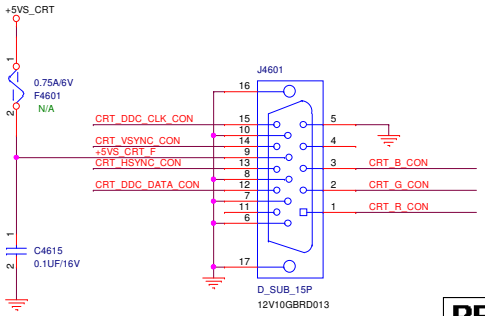




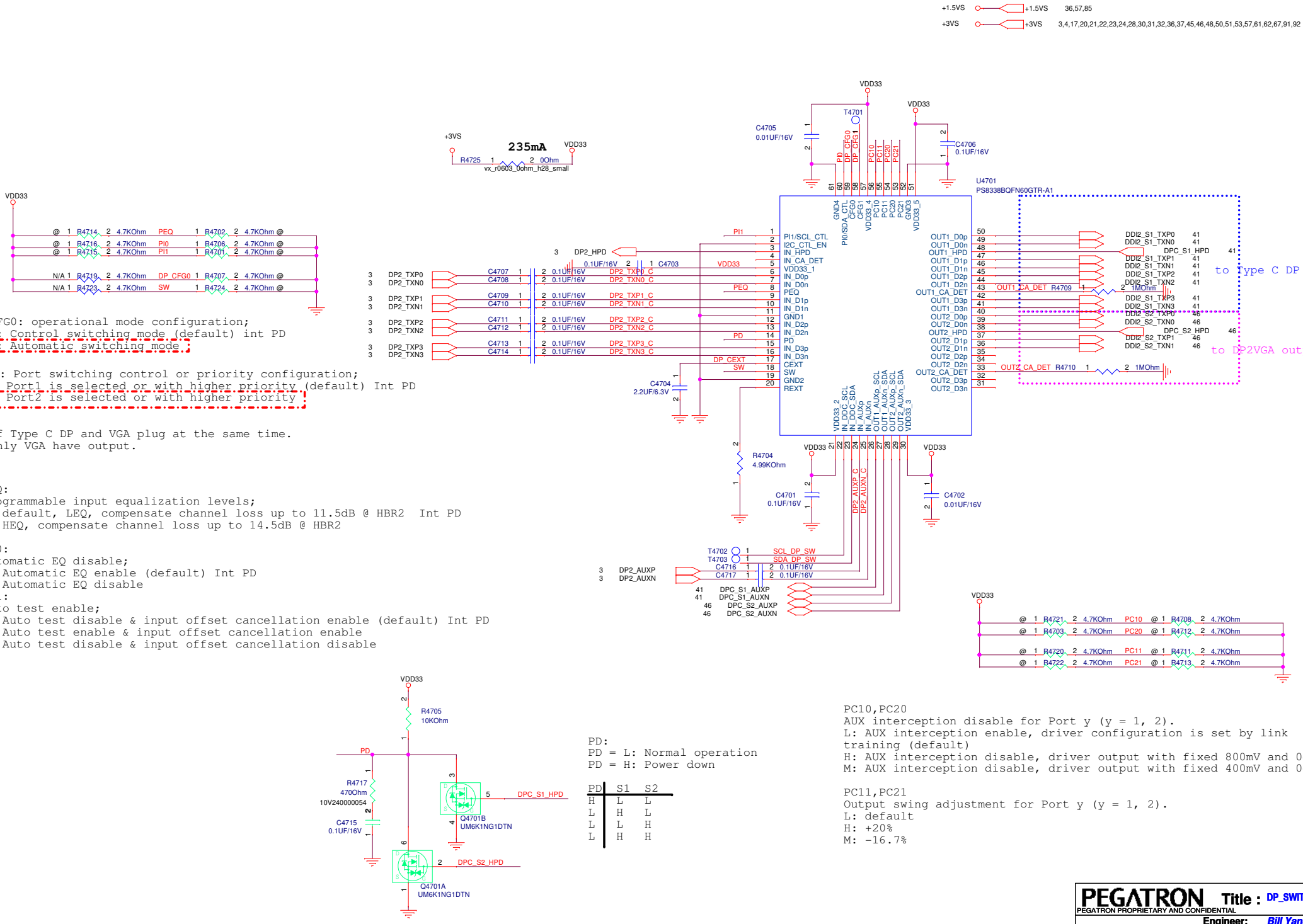
CRT_HV Sync total trace length < 6 inch



D-SUB Connector



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CRT RTD2166
Engineer: Bill Yang
<OrgName>
Size: Custom | Project Name: P4 | Rev: 1.0
Date: Tuesday, September 06, 2016 | Sheet 46 of 104



PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title : DP_SWITCH

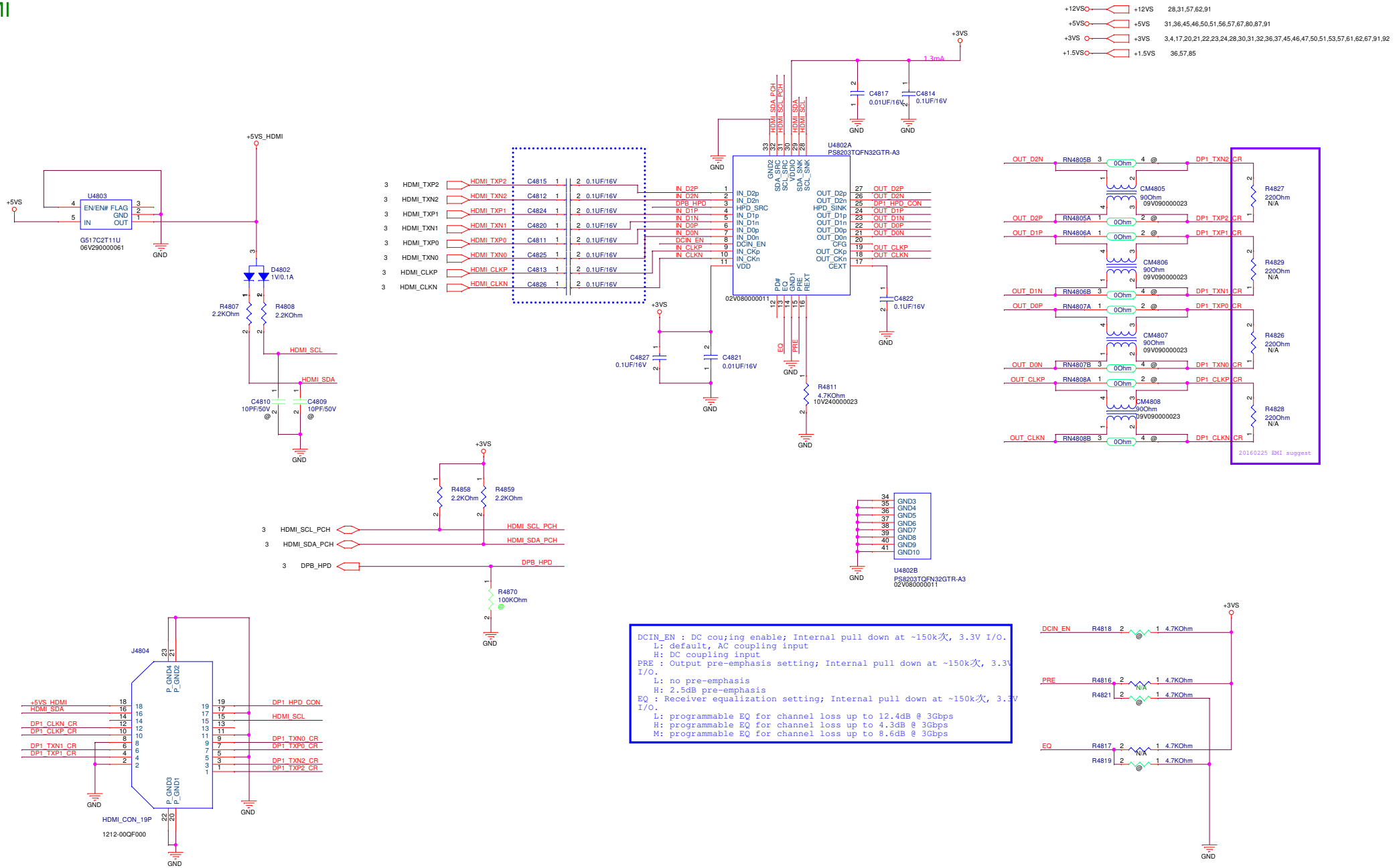
Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 47 of 108

HDMI




```
DCIN_EN : DC cou;ing enable; Internal pull down at ~150k次, 3.3V I/O.
   L: default, AC coupling input
   H: DC coupling input
PRE : Output pre-emphasis setting; Internal pull down at ~150k次, 3.3V
I/O.
   L: no pre-emphasis
   H: 2.5dB pre-emphasis
EQ : Receiver equalization setting; Internal pull down at ~150k次, 3.3V
I/O.
   L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
   H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
   M: programmable EQ for channel loss up to 8.6dB @ 3Gbps
```

<Variant Name>

PEGATRON Title : HDMI-4K2K

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 48 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

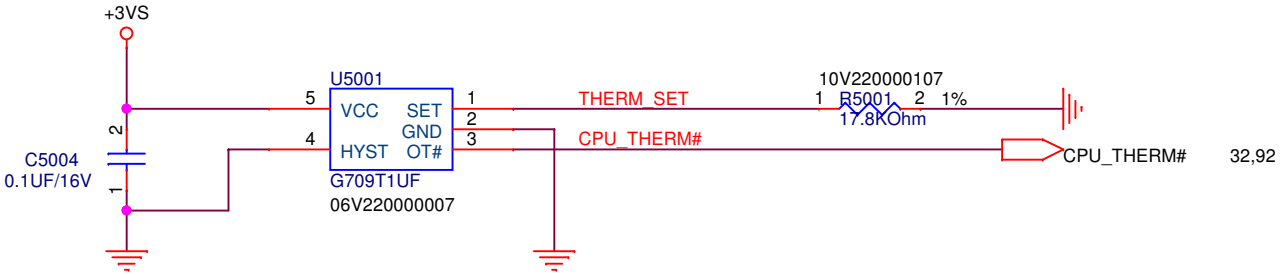
Engineer:

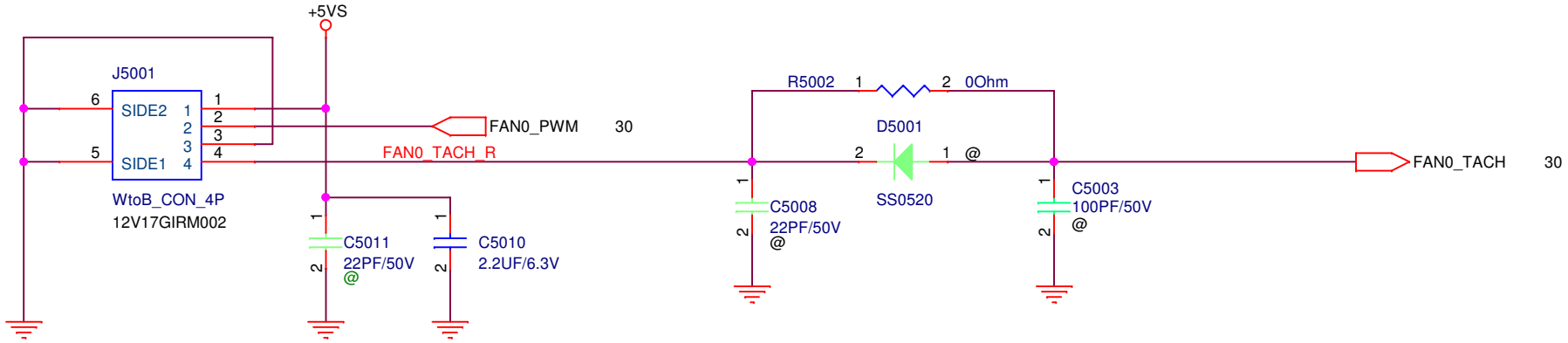
Size	Project Name	Rev
C	KTKUG_25W	1.1

Date: Tuesday, September 06, 2016 Sheet 49 of 108

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,51,53,57,61,62,67,91,92

+5VS +5VS 31,36,45,46,48,51,56,57,67,80,87,91





PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title THERMAL/ FAN

Engineer: Bill Yang

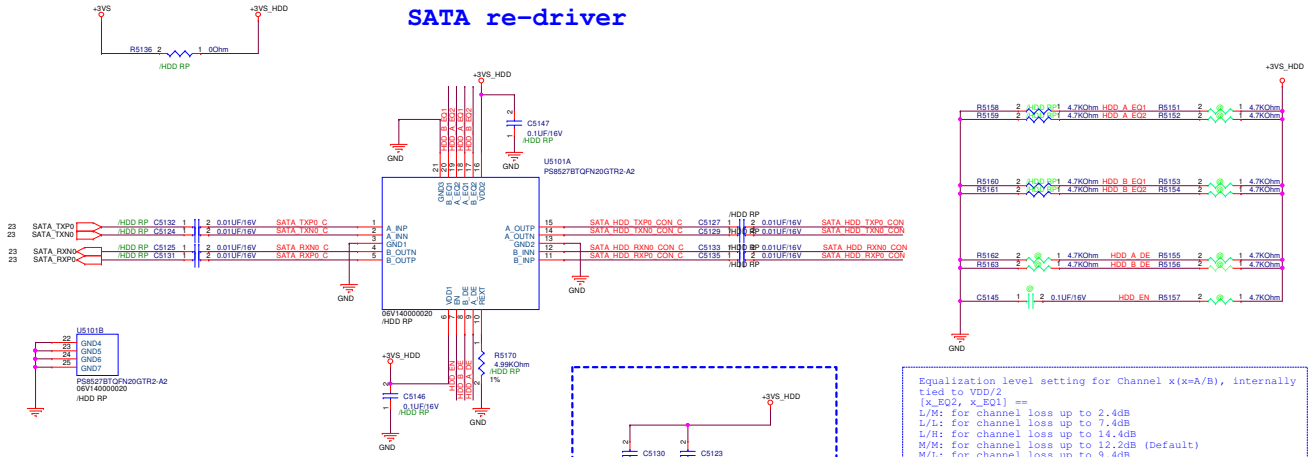
BG1/HW3

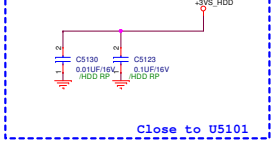
Size Custom | Project Name P4 | Rev 1.0

Date: Tuesday, September 06, 2016 | Sheet 50 of 108

HDD

SATA re-driver

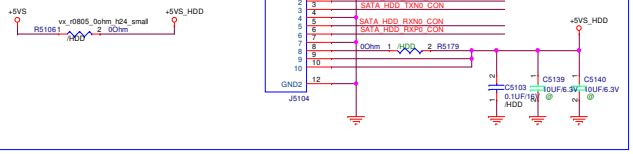




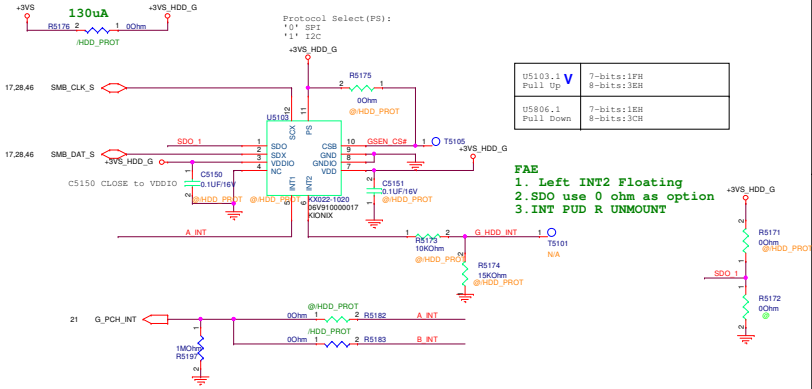
Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
[x_EQ2, x_EQ1] ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB (Default)
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
[x_DE] ==
M: -3.5dB (Default)
L: 0dB
H: -6dB

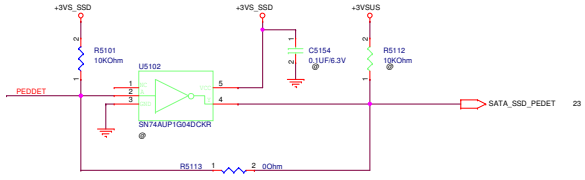
To HDD module



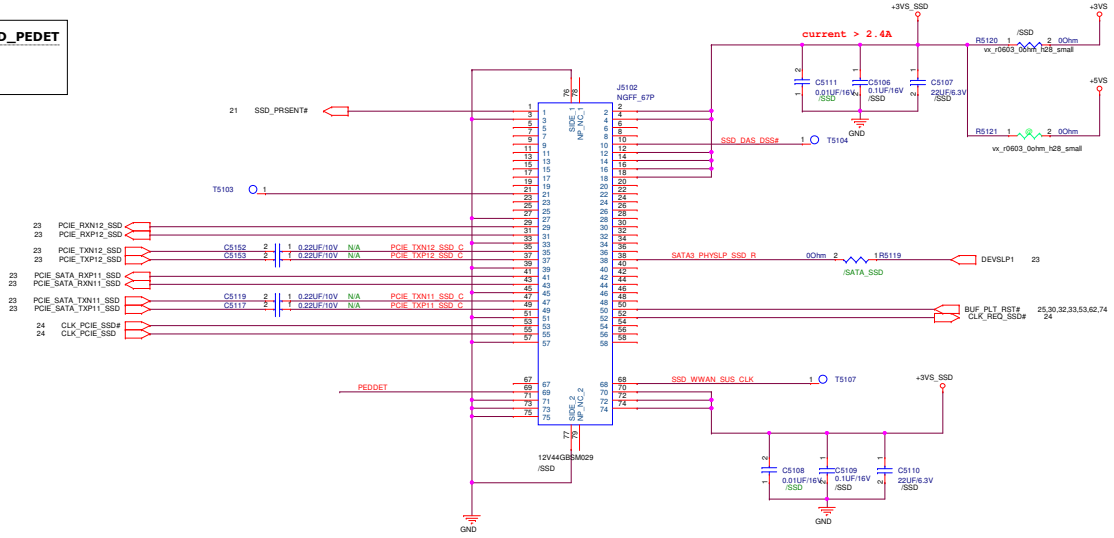
HDD G-Sensor



SSD(SATA/PCIE x2) NGFF socket (M-key)

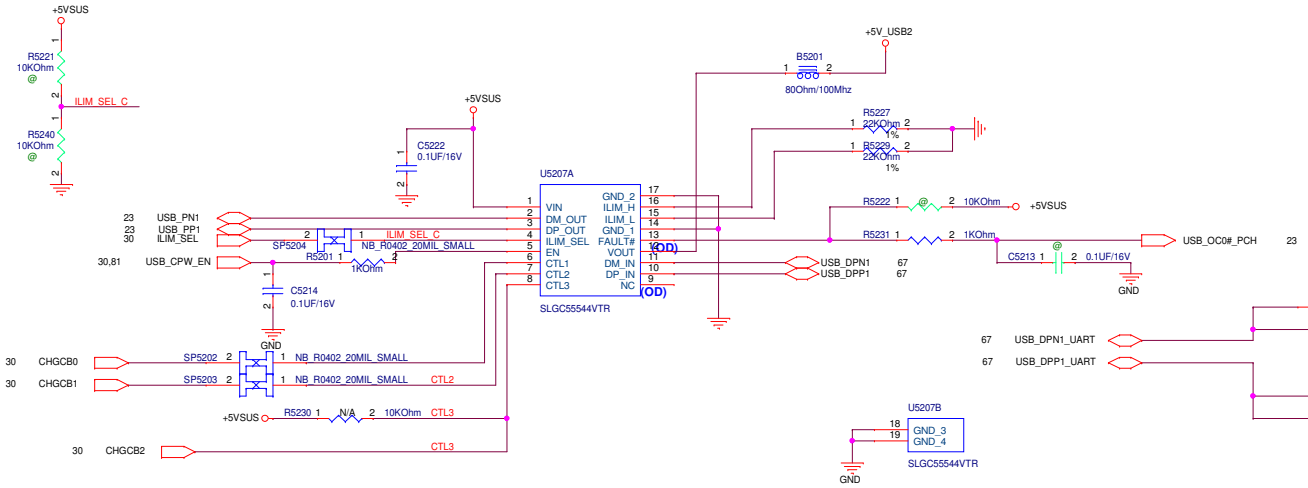


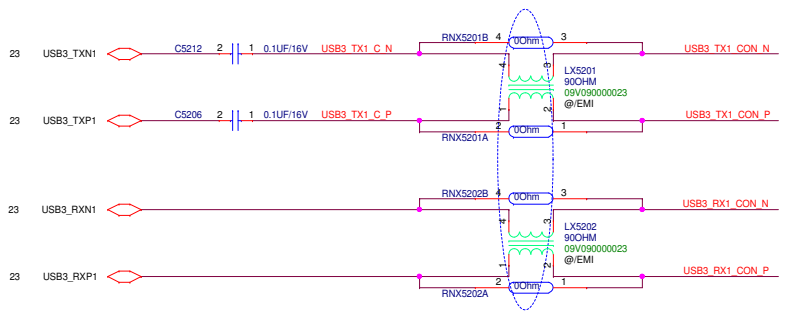
SATA_SSD_PEDET
0: SATA
1: PCIE

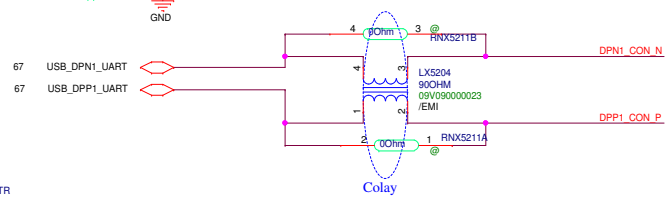


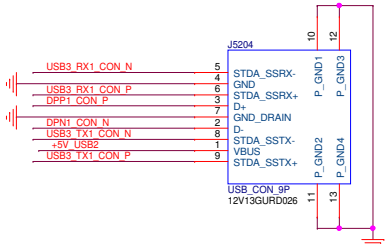
USB 3.0 ports x 1 with Sleep & Charge Left_Down

TPS2544 Device True Table

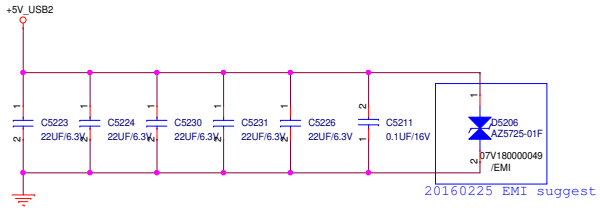


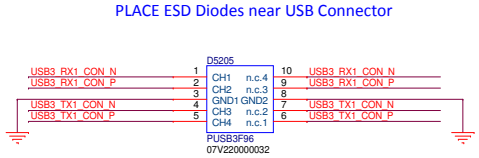


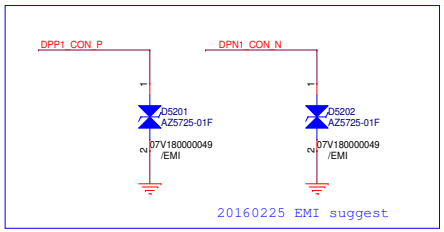




System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO







PEGATRON Title : USB JACK

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 52 of 108

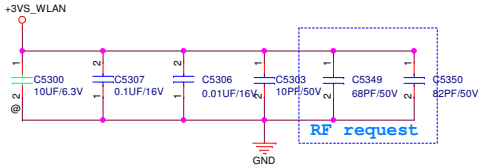
WLAN/ WiGig / BT

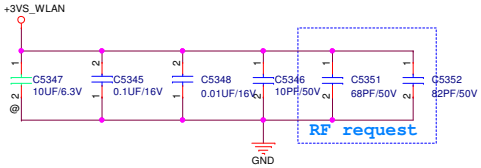
+3V_WLAN_WP1 bypass capactor:
Place 0.1UF near pin 2,4

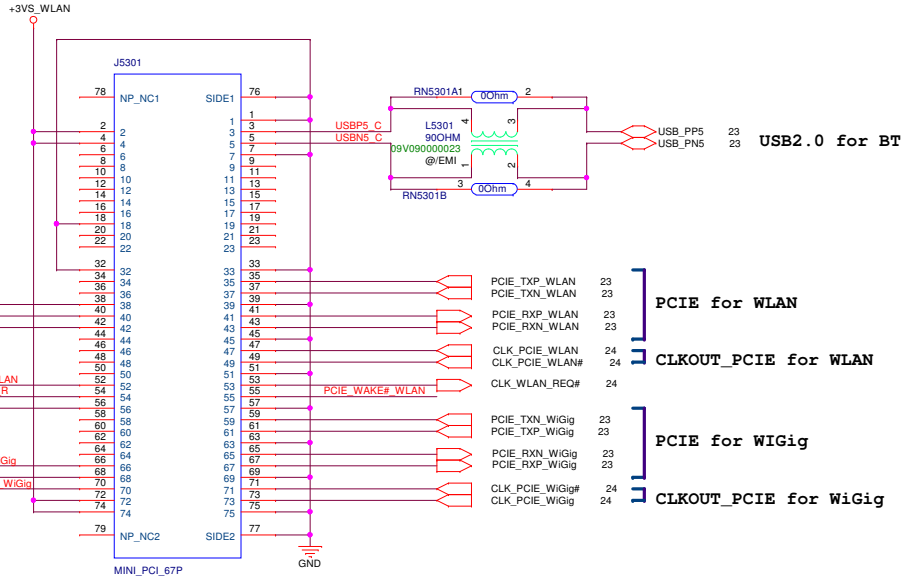
Place 10UF near +3V_WLAN_WP1 source side.

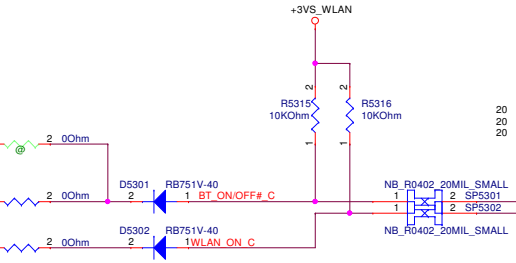
+3V_WLAN_WP1 bypass capactor:
Place 0.1UF near pin 72,74.

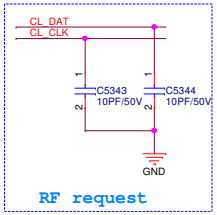
Place 10UF near +3V_WLAN_WP1 source side.

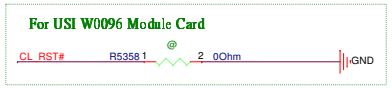


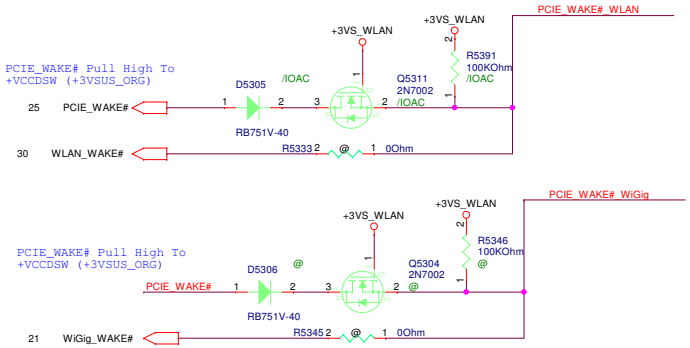


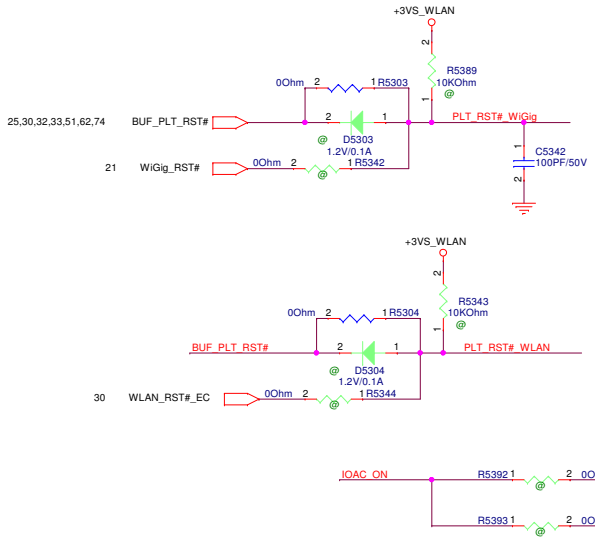


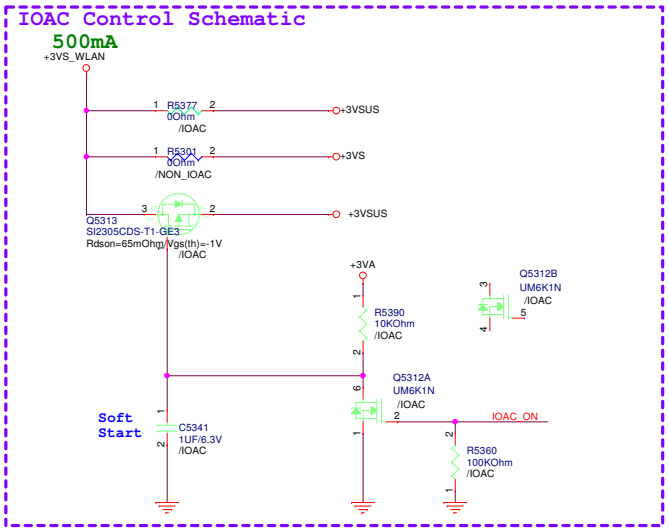












<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : WLAN/ WiGig / BT
BG1/HW4
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 53 of 108

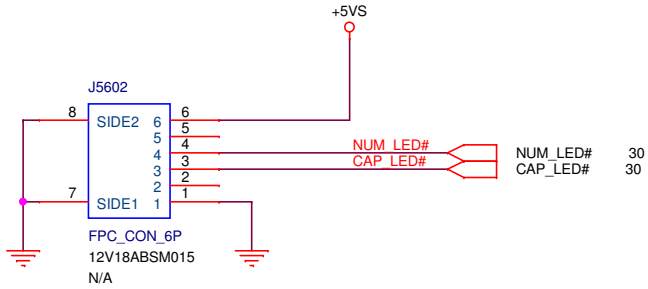
Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
Sheet	54 of 108

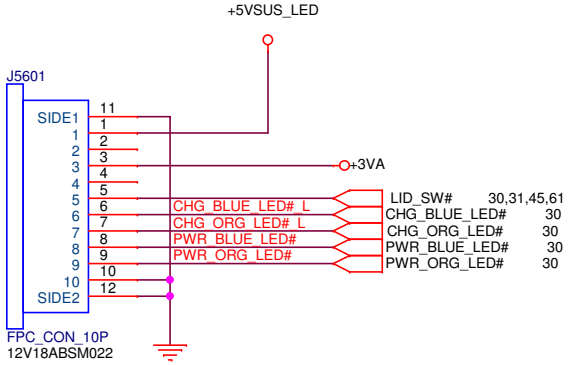
Title	<Title>
Size: A	Document Number: KTKUG_25W
Rev: 1.1	
Date: Tuesday, September 06, 2016	Sheet 55 of 108

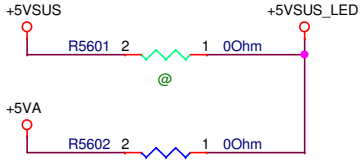
+5VS +5VS 31,36,45,46,48,50,51,57,67,80,87,91

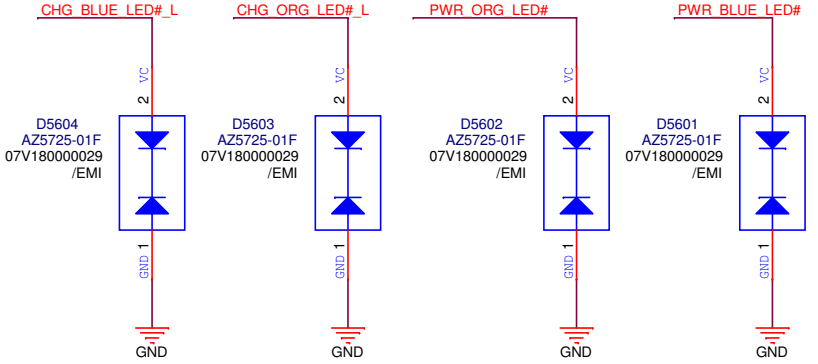
+5VSUS +5VSUS 41,42,52,67,81

+3VA +3VA 24,30,31,36,41,43,53,57,67,81,88,93









PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title : LED

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

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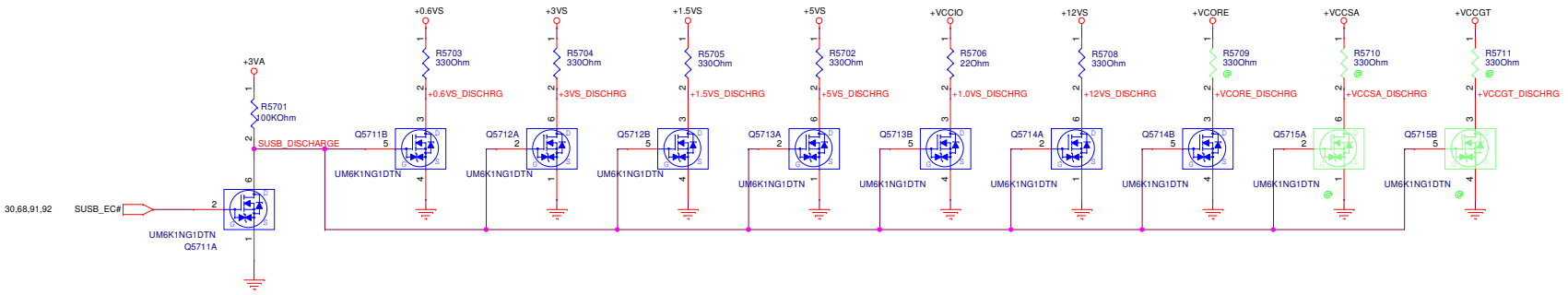

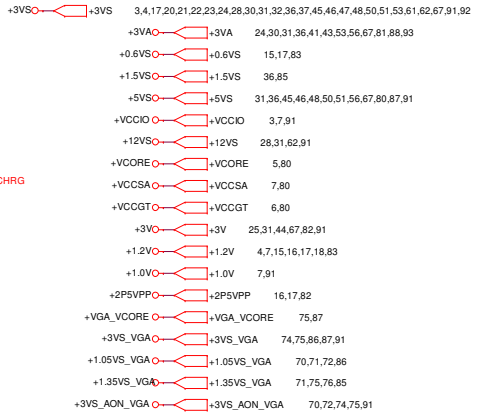

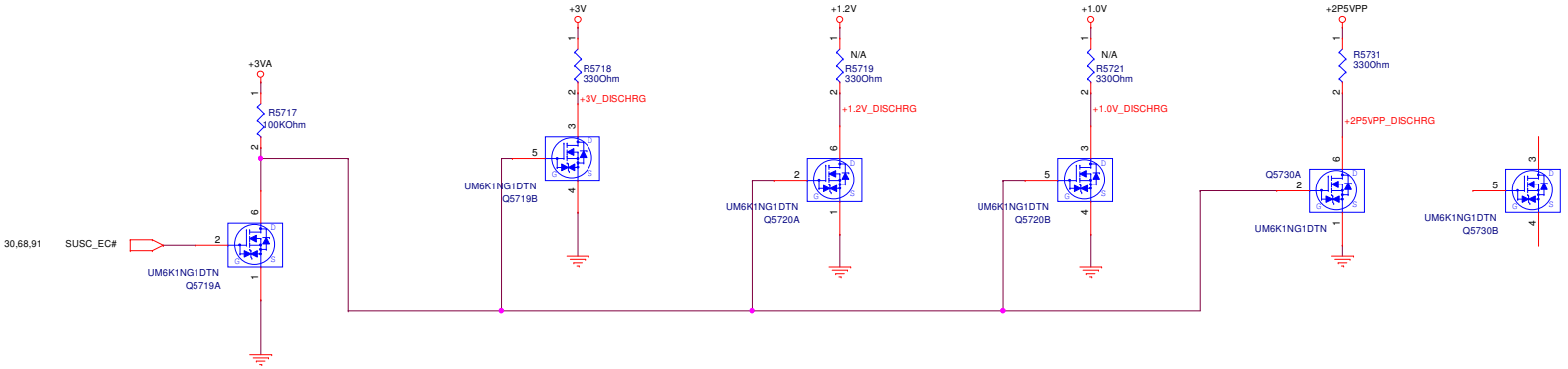

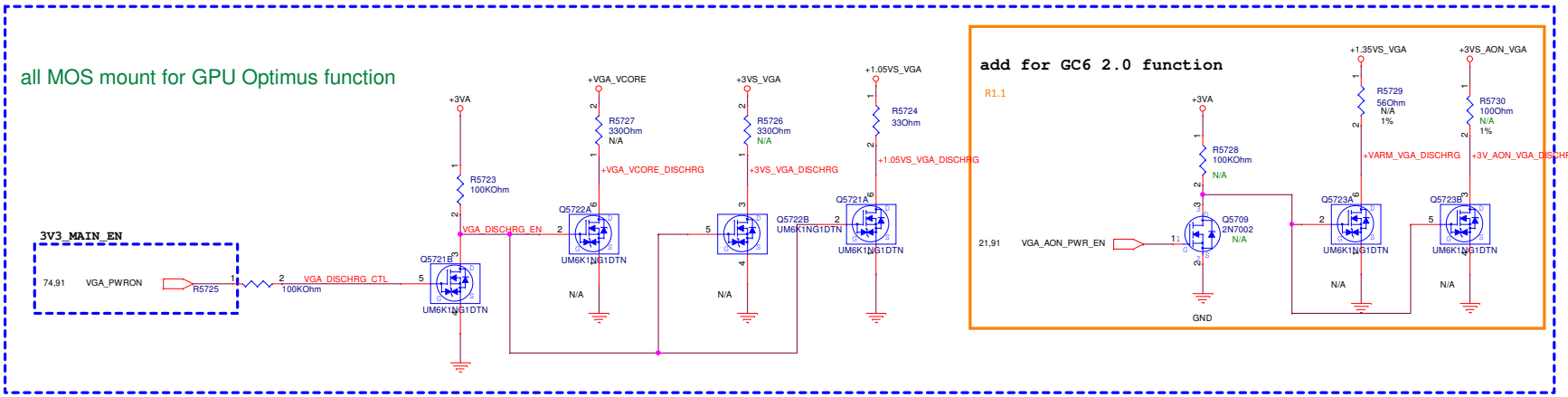

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DSG_Discharge
Engineer: Bill Yang
Size: C(Custom)
Project Name: P4
Rev: 1.0
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Size: A	Document Number: <Doc>
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<Variant Name>

PEGATRON Title :

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<Title>

Engineer:

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C	KTKUG_25W	1.1

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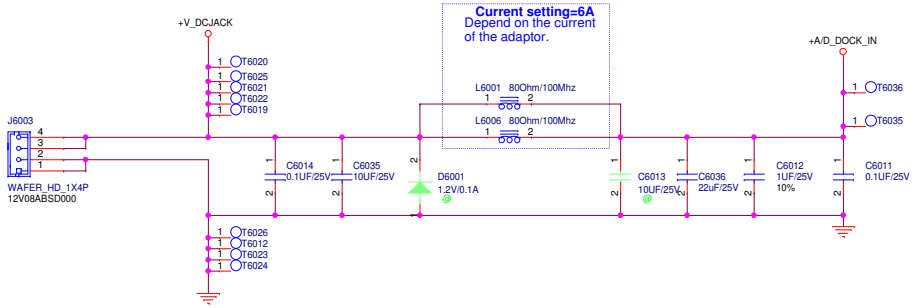
DC_BAT_CONN

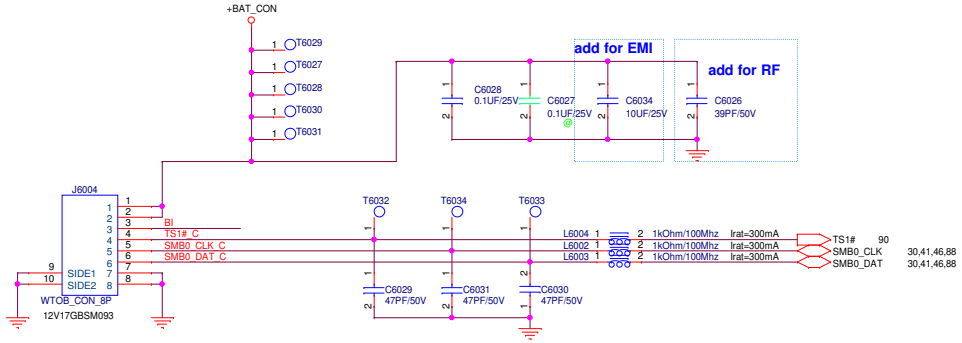
+VCC_RTC — +VCC_RTC 24,25,26,36
+3VA_EC — +3VA_EC 28,30,32
+3VA — +3VA 24,30,31,36,41,43,53,56,57,67,81,88,93
+5VA — +5VA 31,56,81
+1.0VSUS — +1.0VSUS 26,82
+1.8VSUS — +1.8VSUS 9,21,24,26,84
+3VSUS — +3VSUS 4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+5VSUS — +5VSUS 41,42,52,56,67,81
+12VSUS — +12VSUS 81,91
+3V — +3V 25,31,44,57,67,82,91
+12V — +12V 91

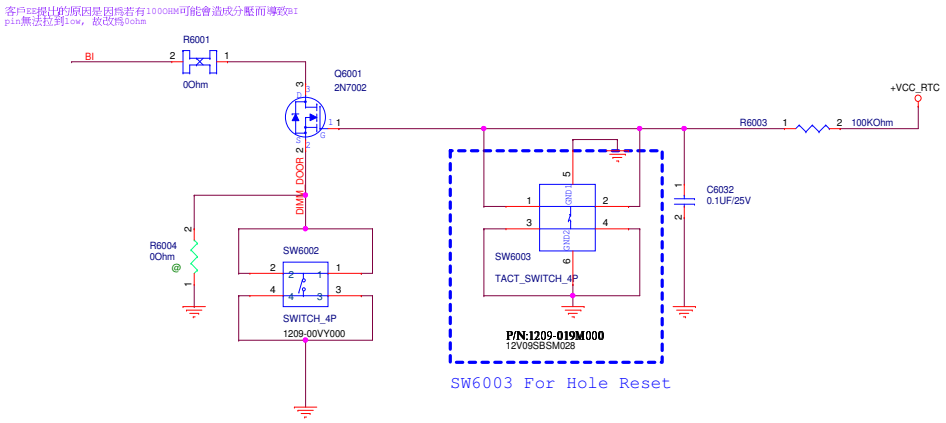
+3VS — +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+5VS — +5VS 31,36,45,46,48,50,51,56,57,67,80,87,91
+12VS — +12VS 28,31,57,62,91
+AC_BAT_SYS — +AC_BAT_SYS 43,45,80,81,82,83,85,87,88
+A/D_DOCK_IN — +A/D_DOCK_IN 89
+BAT_CON — +BAT_CON 88
+VCORE — +VCORE 5,57,80
+VCCGT — +VCCGT 6,57,80
+VCCSA — +VCCSA 7,57,80
+VCCIO — +VCCIO 3,7,57,91
+RTCBAT — +RTCBAT 24

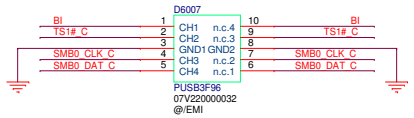
DC Jack WTB CONN

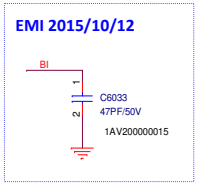


Battery Connector





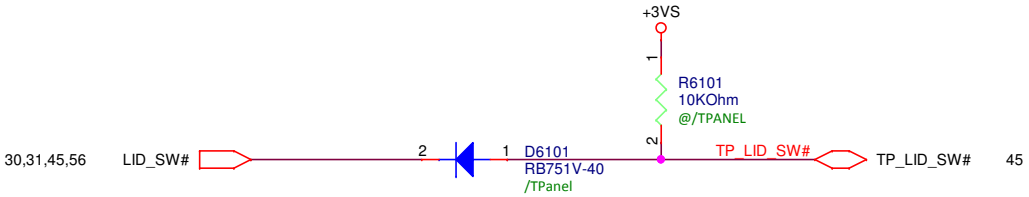




PEGATRON Title : DC_BAT_CONN
BG1-HW3 Engineer: Bill Yang
Size: Custom | Project Name: P4 | Rev: 1.0
Date: Tuesday, September 06, 2016 | Sheet 60 of 108

+5VS +5VS 31,36,45,46,48,50,51,56,57,67,80,87,91

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,62,67,91,92



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PEGATRON Title : Touch Panel Conn

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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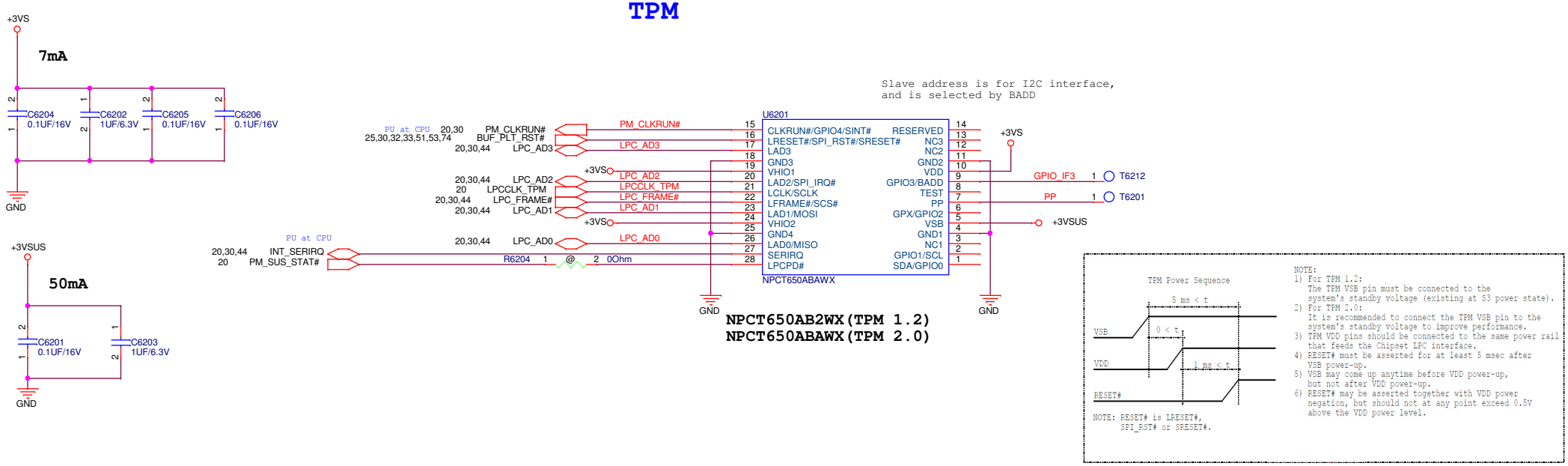
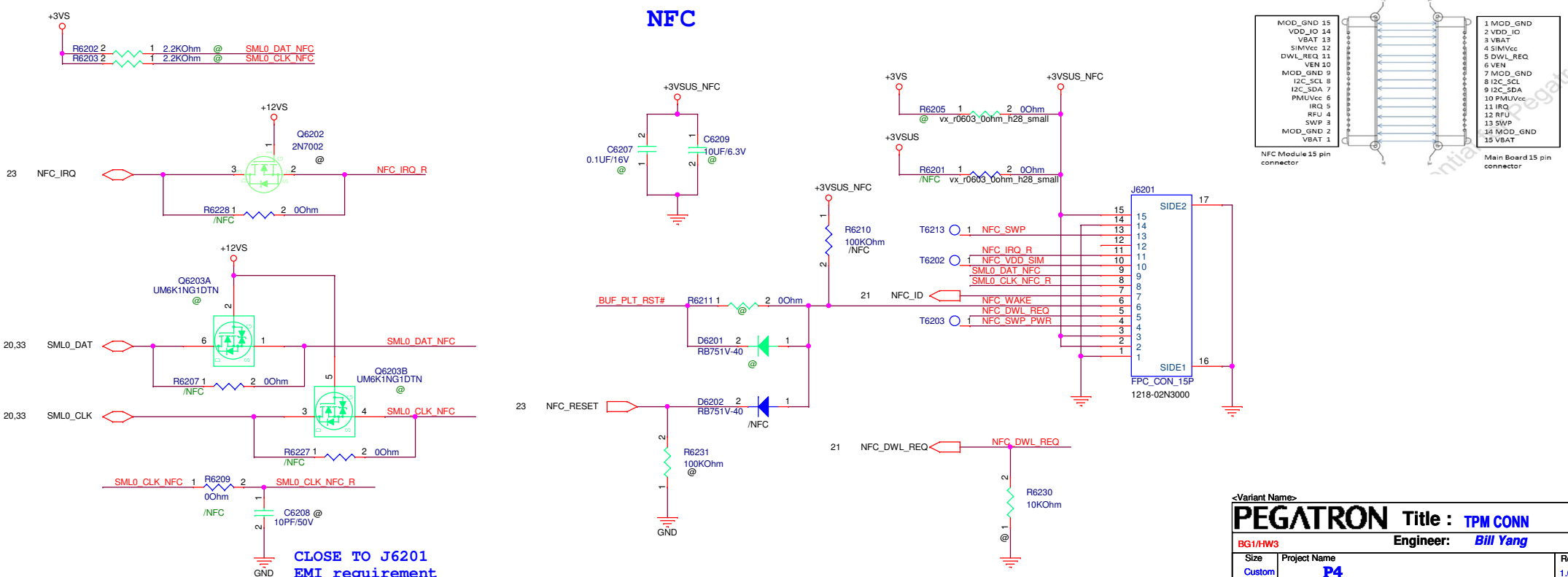
TPM



NFC



<Variant Name>

PEGATRON Title : TPM CONN

BG1/HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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Size: A	Document Number: KTKUG_25W
Rev: 1.1	
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Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
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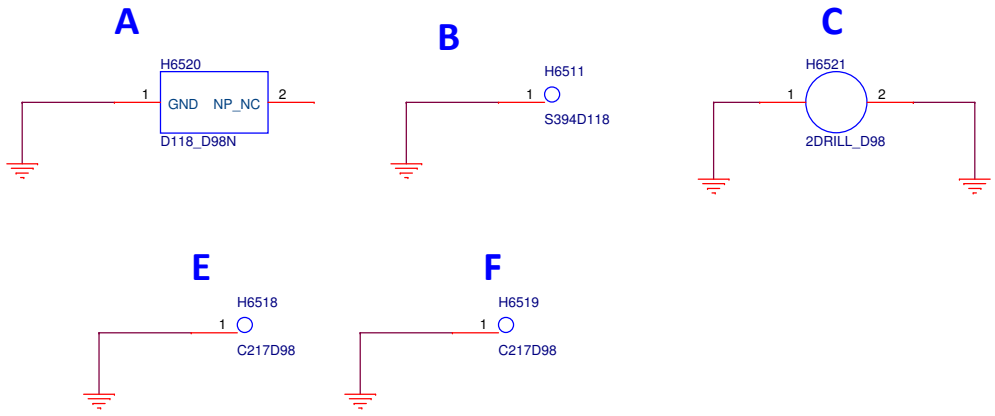

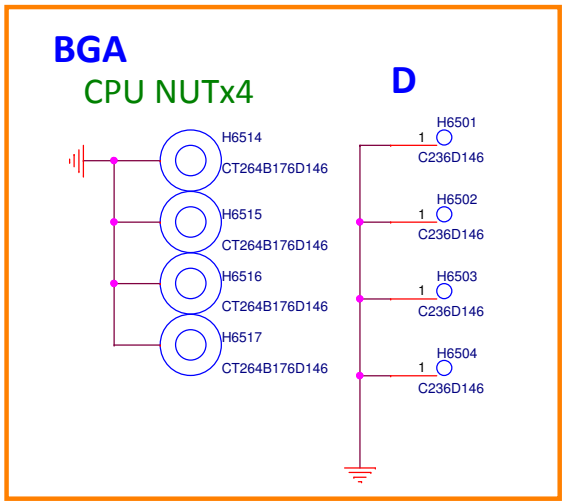

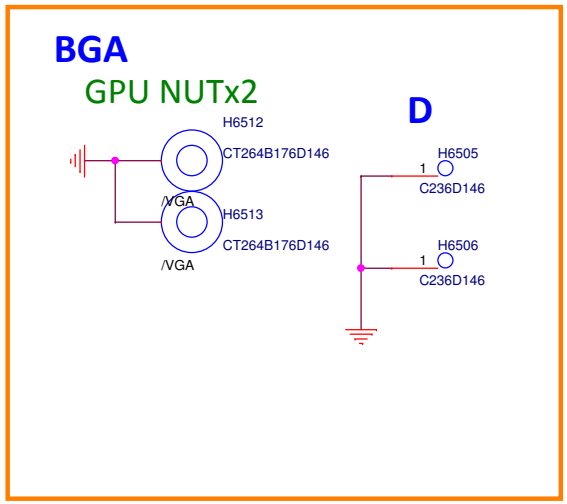

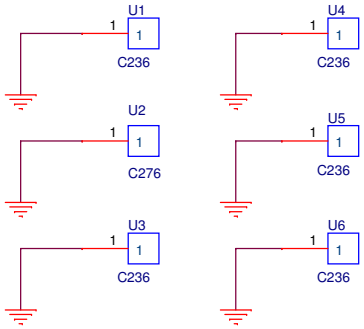

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: ME_CONN,Skew Hole

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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+5VSUS +5VSUS 41,42,52,56,81
+3V +3V 25,31,44,57,82,91
+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,91,92

+3VS
R6708 49.9KOhm 1% vx_r0402_small @/UART
R6707 49.9KOhm 1% vx_r0402_small @/UART
21 UART_RX
21 UART_TX
/NON_UART
0Ohm R6709 USB_PN1_N
0Ohm R6710 USB_PP1_N
0Ohm /NON_UART @/UART
0Ohm R6703 USB_PN1_U
0Ohm R6704 USB_PP1_U
0Ohm @/UART
52 USB_DPN1
52 USB_DPP1
Pin 2 Colay
U6702
HSD2-
HSD2+
HSD1+
HSD1-
GND
D-
D+
OE#
VCC
S
USB_PN1_C
USB_PP1_C
0Ohm R6711
0Ohm R6712
/NON_UART @/UART
0Ohm R6705
0Ohm R6706
0Ohm @/UART
USB_DPN1_UART 52
USB_DPP1_UART 52
Pin 2 Colay
NX3DV42GU
06V150000026
@/UART
+3VA
C6704 0.1UF/16V @/UART
+3VSUS
R6715 10KOhm @/UART
21 USB_UART_SEL
@/UART
2N7002
Q6777
20150417
For layout limitation

RNX6709B @
0Ohm
23 USB_PN2
23 USB_PP2
LX6706
90OHM
09V090000023
/EMI
DPN2_CON_N
DPP2_CON_P
0Ohm
RNX6709A @

RNX6708B 0Ohm @
23 USB_PN8
23 USB_PP8
LX6708
90OHM
09V090000023
/EMI
DPN8_CON_N
DPP8_CON_P
0Ohm
RNX6708A @

SD
Swaybay Hub
J6701
DPP8_CON_P
DPN8_CON_N
DPP2_CON_P
DPN2_CON_N
23 USB_OC1#_PCH
30 USBP01_EN
USB_OC1#_PCH
USBP01_EN
+3VS
+3V
+5VSUS
+5VSUS
+5VS
SIDE1
SIDE2
31
32
FPC_CON_30P
12V18ABSM028
/W SB

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : MLB to IO
Engineer: Bill Yang
BG1/HW3
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+3VSUS +3VSUS 4,24,25,26,28,30,31,33,41,42,51,53,62,67,81,

+3VA +3VA 24,30,31,36,41,43,53,56,57,67,81,88,93

25,30 PM_SUSB# R6801 1 2 0Ohm /BYPAS_EC SUSB_EC# 30,57,91,92

25,30 PM_SUSC# R6802 1 2 0Ohm /BYPAS_EC SUSC_EC# 30,57,91

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

Delay By EC(2ms+ EC processing time (3ms~33ms)

30 DE_ALL_SYS_PGD_EC R6809 1 2 0Ohm /BYPAS_EC

+3VSUS

U6802
1 A VCC 5
PM_SUSB# 2 B
3 GND Y 4
Vcc=2~5.5
/BYPAS_EC

For shut down Sequence

R6808 1 2
@ 100KOhm
10V240000005

C6804 1 2
0.1UF/16V
@

GND GND

DE_ALL_SYS_PGD_HW 30

+3VSUS

U6803
PM_SUSB# 1 A VCC 5
SYS_PWROK_EC_G 2 B
3 GND Y 4
Vcc=2~5.5
/BYPAS_EC

30 SYS_PWROK_EC SP6802 1 2

For shut down Sequence

R6806 1 2
@ 100KOhm
10V240000005

GND

R6804 1 2 0Ohm /BYPAS_EC SYS_PWROK 25,30

<Variant Name>

PEGATRON
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Title : BYPASS EC SEQUENCE

Engineer: Bill Yang

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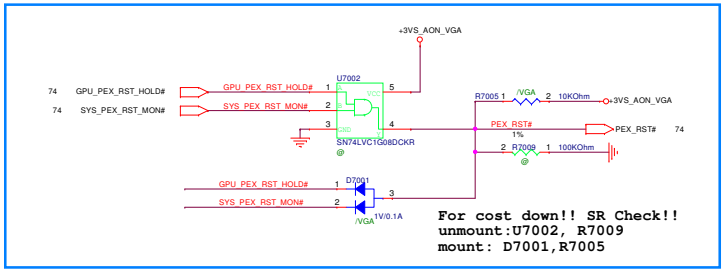
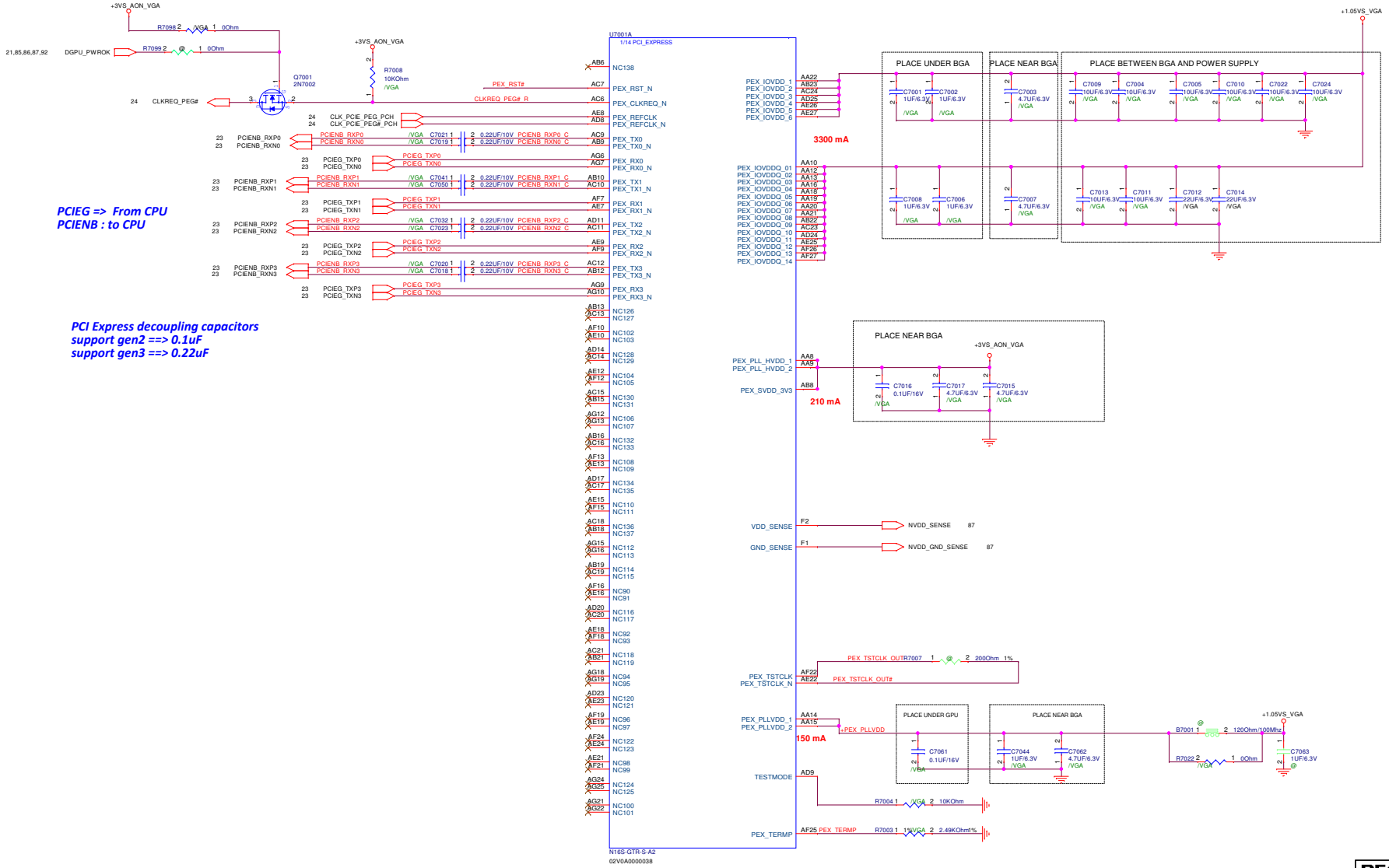
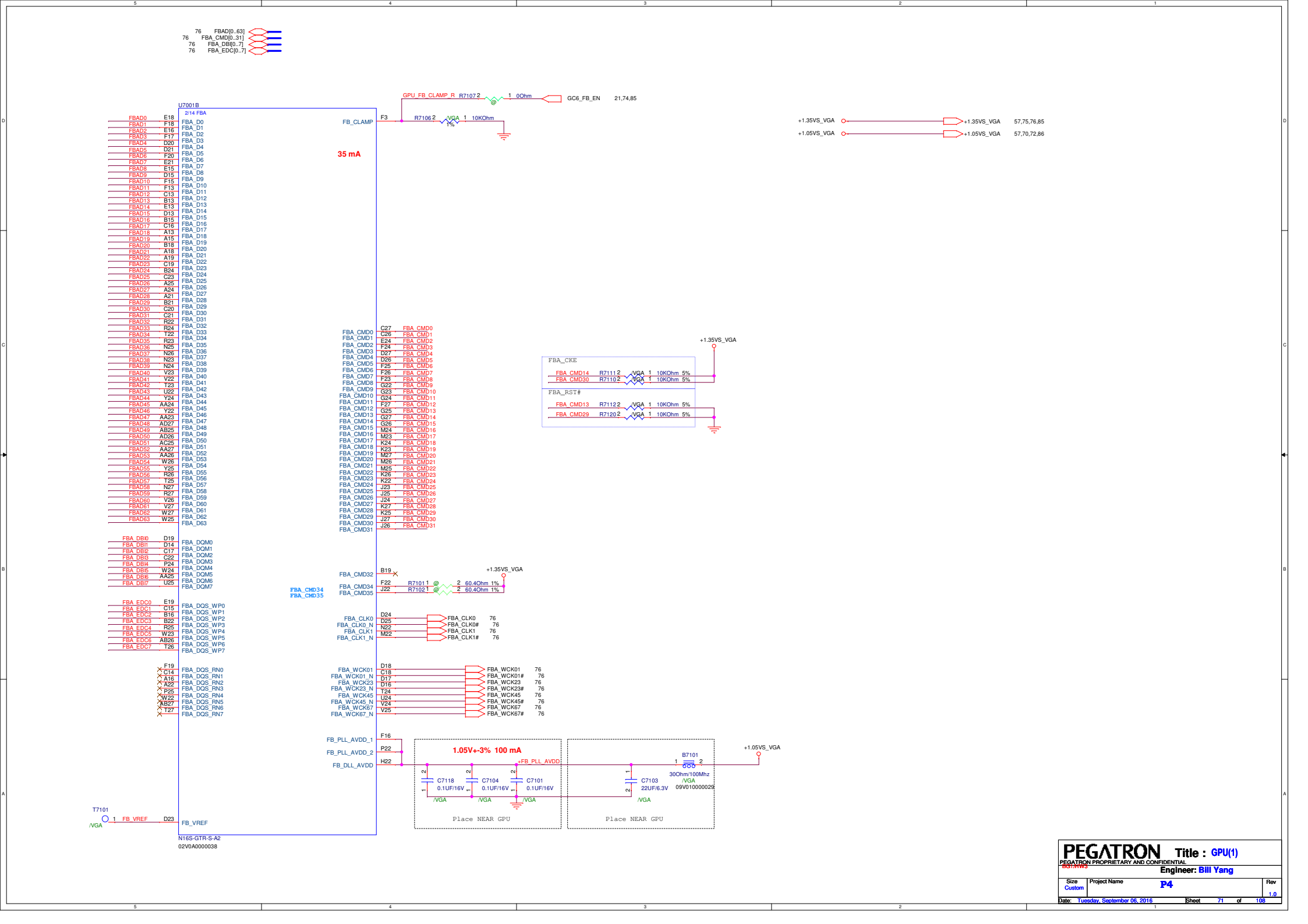

+3VS_AON_VGA
74 GPU_PEX_RST_HOLD#
74 SYS_PEX_RST_MON#
GPU_PEX_RST_HOLD#
SYS_PEX_RST_MON#
U7002
SN74LVC1G08DCKR
R7005 1 /VGA 2 10KOhm
+3VS_AON_VGA
PEX_RST#
1%
PEX_RST# 74
2 R7009 1 100KOhm
@
D7001
1V/0.1A
/VGA
For cost down!! SR Check!!
unmount:U7002, R7009
mount: D7001,R7005


+3VS_AON_VGA
+3VS_AON_VGA 57,72,74,75,91
+1.05VS_VGA
+1.05VS_VGA 57,71,72,86


+3VS_AON_VGA
R7098 2 /VGA 1 0Ohm
21,85,86,87,92 DGPU_PWROK
R7099 2 @ 1 0Ohm
Q7001
2N7002
24 CLKREQ_PEG#
+3VS_AON_VGA
R7008
10KOhm
/VGA
PEX_RST#
CLKREQ_PEG# R
24 CLK_PCIE_PEG_PCH
24 CLK_PCIE_PEG#_PCH
PCIENB_RXP0
PCIENB_RXN0
PCIEG_TXP0
PCIEG_TXN0
PCIENB_RXP1
PCIENB_RXN1
PCIEG_TXP1
PCIEG_TXN1
PCIENB_RXP2
PCIENB_RXN2
PCIEG_TXP2
PCIEG_TXN2
PCIENB_RXP3
PCIENB_RXN3
PCIEG_TXP3
PCIEG_TXN3
0.22UF/10V
U7001A
1/14 PCI_EXPRESS
PEX_RST_N
PEX_CLKREQ_N
PEX_REFCLK
PEX_REFCLK_N
PEX_TX0
PEX_TX0_N
PEX_RX0
PEX_RX0_N
PEX_TX1
PEX_TX1_N
PEX_RX1
PEX_RX1_N
PEX_TX2
PEX_TX2_N
PEX_RX2
PEX_RX2_N
PEX_TX3
PEX_TX3_N
PEX_RX3
PEX_RX3_N
N16S-GTR-S-A2
02V0A0000038
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDD_6
3300 mA
PEX_IOVDDQ_01
PEX_IOVDDQ_02
PEX_IOVDDQ_03
PEX_IOVDDQ_04
PEX_IOVDDQ_05
PEX_IOVDDQ_06
PEX_IOVDDQ_07
PEX_IOVDDQ_08
PEX_IOVDDQ_09
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PLACE UNDER BGA
PLACE NEAR BGA
PLACE BETWEEN BGA AND POWER SUPPLY
+1.05VS_VGA
PEX_PLL_HVDD_1
PEX_PLL_HVDD_2
PEX_SVDD_3V3
210 mA
VDD_SENSE
GND_SENSE
NVDD_SENSE 87
NVDD_GND_SENSE 87
PEX_TSTCLK_OUT
PEX_TSTCLK
PEX_TSTCLK_N
PEX_PLLVDD_1
PEX_PLLVDD_2
+PEX_PLLVDD
150 mA
PLACE UNDER GPU
TESTMODE
PEX_TERMP
PEX_TERM
R7004 1 /VGA 2 10KOhm
R7003 1 1%/VGA 2 2.49KOhm1%
PCI Express decoupling capacitors
support gen2 ==> 0.1uF
support gen3 ==> 0.22uF
PCIEG => From CPU
PCIENB : to CPU



PEGATRON Title : GPU(1)

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Engineer: Bill Yang

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Custom	P4	1.0

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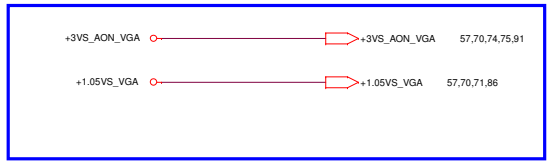
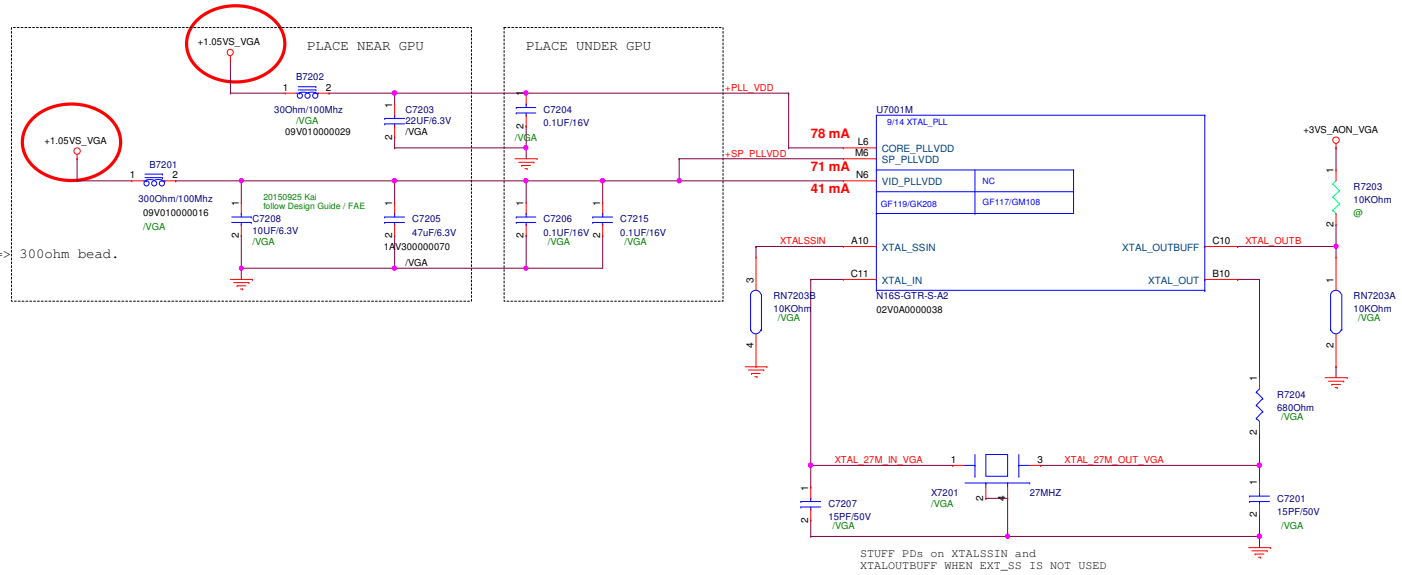
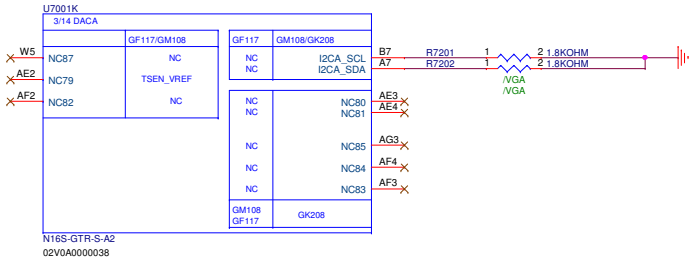


20141024 Chris





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : GPU(1)
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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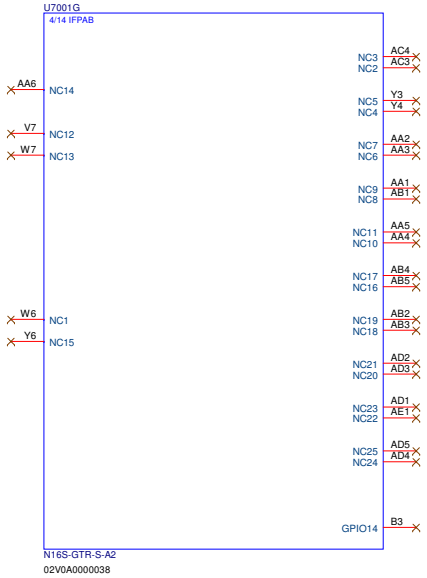
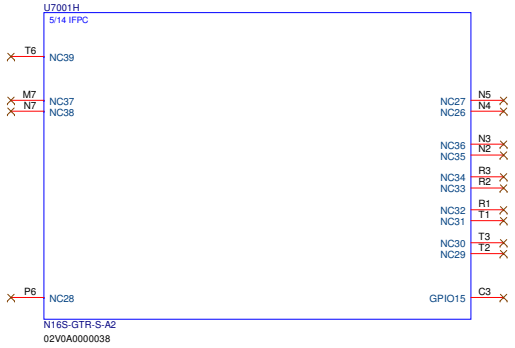
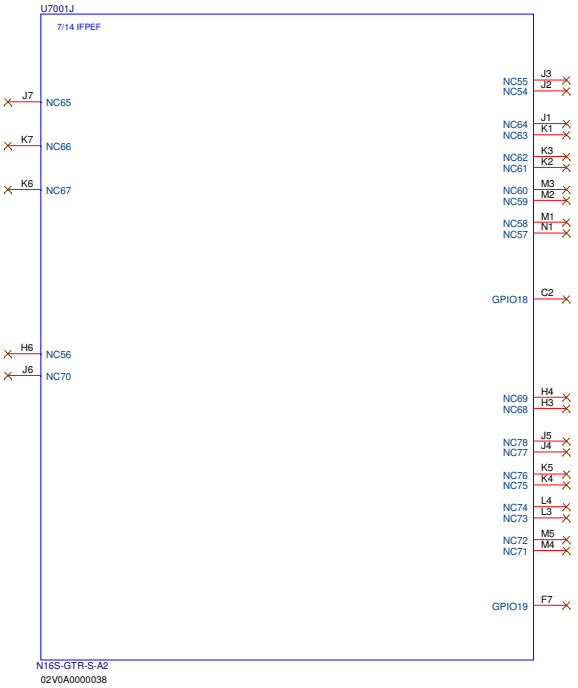
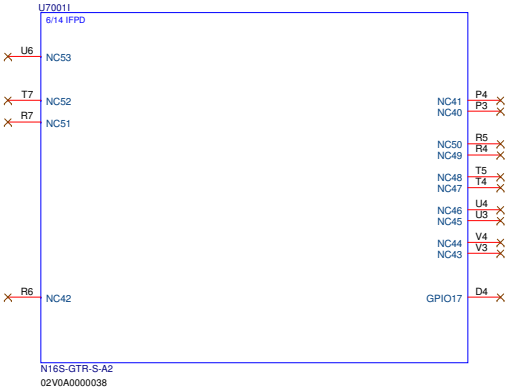
LVDS









Title : GPU(1)

Engineer: Bill Yang

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Custom	P4	1.0

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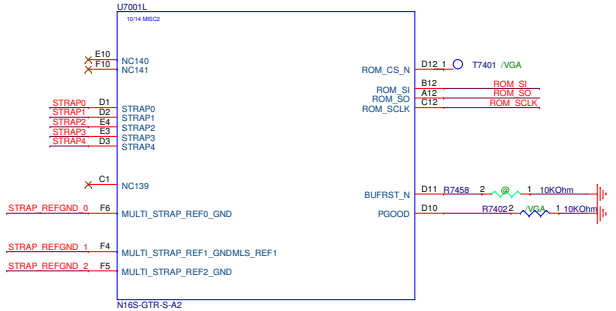
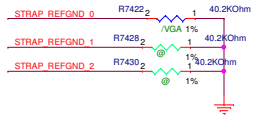
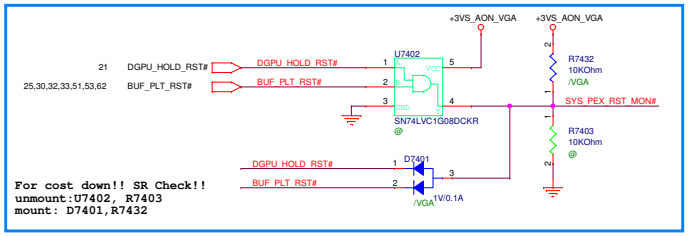
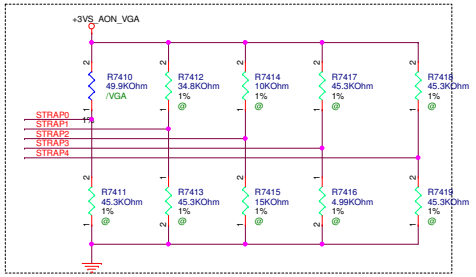
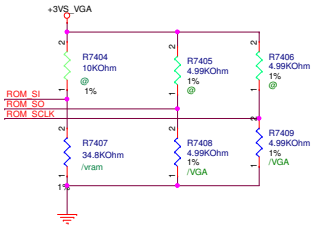








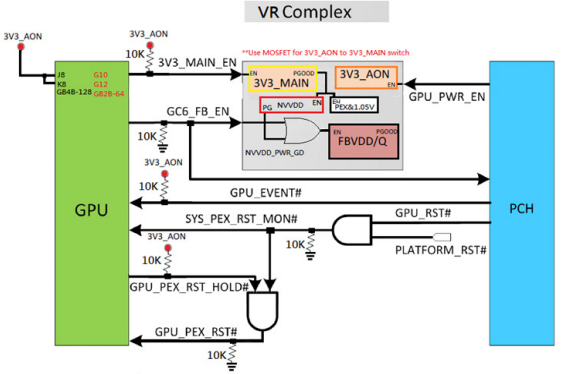


Strapping:

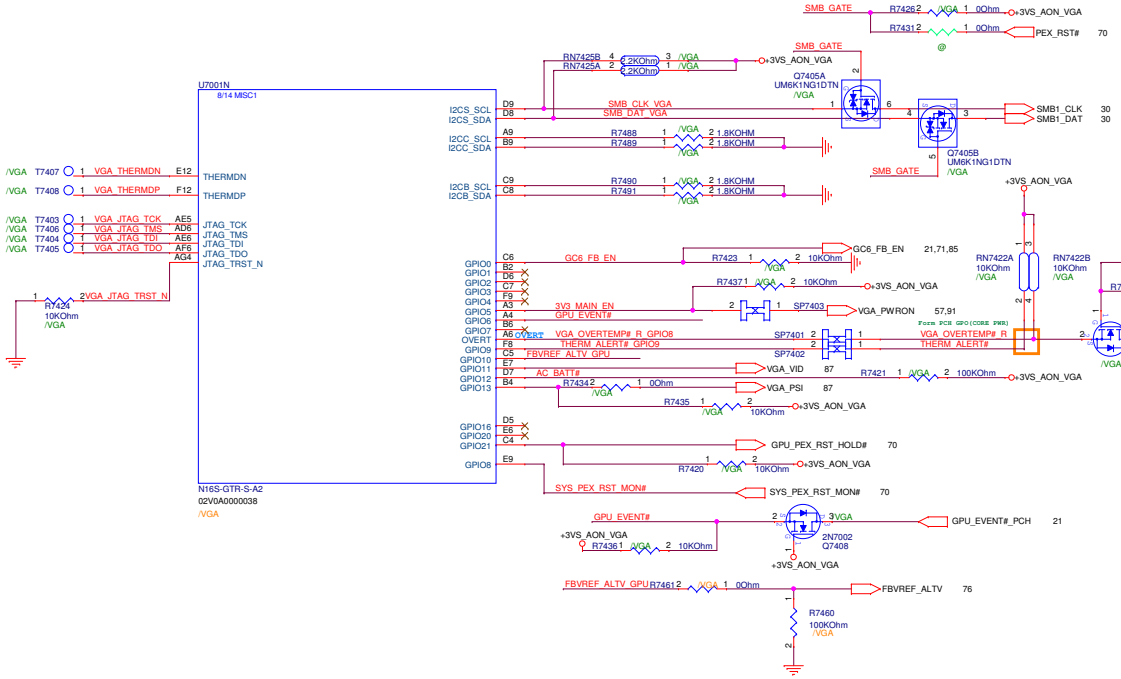
4.99K PU 1000 PD 0000		
10.0K PU 1001 PD 0001		
15.0K PU 1010 PD 0010		
20.0K PU 1011 PD 0011		
24.9K PU 1100 PD 0100		
30.1K PU 1101 PD 0101		
34.8K PU 1110 PD 0110		
45.3K PU 1111 PD 0111		
4.99K	10V220000077	
10.0K	10V220000003	
15.0K	10V220000023	
20.0K	10V220000036	
24.9K	10V220000049	
30.1K	10V220000119	
34.8K	10V220000061	
45.3K	10V220000073	

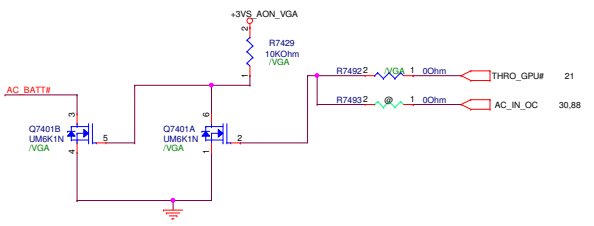
N16V-GTR

1.SAMSUNG: 0X0 (R7407 PD 5K 10V220000077)
2.MICRON: 0x1 (R7407 PD 10K 10V220000073)



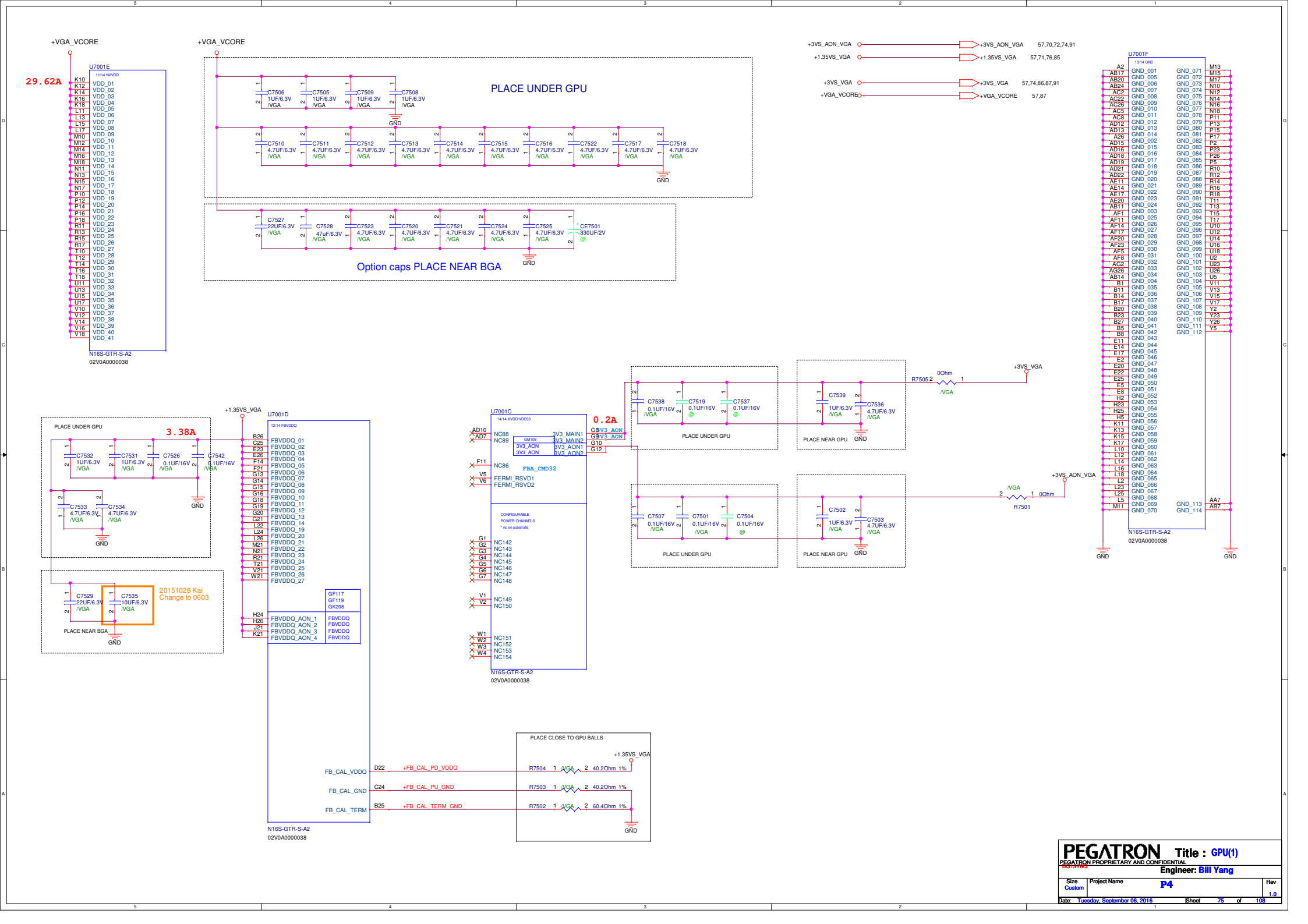
GC6 2.0 High-level Signal Connections





ROM_SI		ROM_SO		ROM_SCLK	
R7404	R7407	R7405	R7408	R7406	R7409
20k	N	4.99K	N	4.99K	N
N	45.3k	4.99K	N	4.99K	N
34.8k	N	4.99K	N	4.99K	N
N	30.1k	4.99K	N	4.99K	N
10k	N	N	4.99K	N	4.99K
20k	N	N	4.99K	N	4.99K
N	20k	N	4.99K	N	4.99K
N	30.1k	N	4.99K	N	4.99K

PEGATRON Title : GPU(1)
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
Size: Custom | Project Name: P4 | Rev: 1.0
Date: Tuesday, September 06, 2016 | Sheet 74 of 108


+VGA_VCORE
29.62A
U7001E
11/14 NVVDD
K10 K12 K14 K16 K18 L11 L13 L15 L17 M10 M12 M14 M16 M18 N11 N13 N15 N17 P10 P12 P14 P16 P18 R11 R13 R15 R17 T10 T12 T14 T16 T18 U11 U13 U15 U17 V10 V12 V14 V16 V18
VDD_01 VDD_02 VDD_03 VDD_04 VDD_05 VDD_06 VDD_07 VDD_08 VDD_09 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14 VDD_15 VDD_16 VDD_17 VDD_18 VDD_19 VDD_20 VDD_21 VDD_22 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31 VDD_32 VDD_33 VDD_34 VDD_35 VDD_36 VDD_37 VDD_38 VDD_39 VDD_40 VDD_41
N16S-GTR-S-A2
02V0A0000038
+VGA_VCORE
PLACE UNDER GPU
C7506 1UF/6.3V /VGA
C7505 1UF/6.3V /VGA
C7509 1UF/6.3V /VGA
C7508 1UF/6.3V /VGA
GND
C7510 4.7UF/6.3V /VGA
C7511 4.7UF/6.3V /VGA
C7512 4.7UF/6.3V /VGA
C7513 4.7UF/6.3V /VGA
C7514 4.7UF/6.3V /VGA
C7515 4.7UF/6.3V /VGA
C7516 4.7UF/6.3V /VGA
C7522 4.7UF/6.3V /VGA
C7517 4.7UF/6.3V /VGA
C7518 4.7UF/6.3V /VGA
GND
C7527 22UF/6.3V /VGA
C7528 47uF/6.3V /VGA
C7523 4.7UF/6.3V /VGA
C7520 4.7UF/6.3V /VGA
C7521 4.7UF/6.3V /VGA
C7524 4.7UF/6.3V /VGA
C7525 4.7UF/6.3V /VGA
CE7501 330UF/2V @
GND
Option caps PLACE NEAR BGA
+3VS_AON_VGA
+1.35VS_VGA
+3VS_VGA
+VGA_VCORE
+3VS_AON_VGA 57,70,72,74,91
+1.35VS_VGA 57,71,76,85
+3VS_VGA 57,74,86,87,91
+VGA_VCORE 57,87
U7001F
13/14 GND
A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 AD14 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11
GND_001 GND_005 GND_006 GND_007 GND_008 GND_009 GND_010 GND_011 GND_012 GND_013 GND_014 GND_002 GND_015 GND_016 GND_017 GND_018 GND_019 GND_020 GND_021 GND_022 GND_023 GND_024 GND_025 GND_026 GND_027 GND_028 GND_029 GND_030 GND_031 GND_032 GND_033 GND_034 GND_004 GND_035 GND_036 GND_037 GND_038 GND_039 GND_040 GND_041 GND_042 GND_043 GND_044 GND_045 GND_046 GND_047 GND_048 GND_049 GND_050 GND_051 GND_052 GND_053 GND_054 GND_055 GND_056 GND_057 GND_058 GND_059 GND_060 GND_061 GND_062 GND_063 GND_064 GND_065 GND_066 GND_067 GND_068 GND_069 GND_070
M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5
GND_071 GND_072 GND_073 GND_074 GND_075 GND_076 GND_077 GND_078 GND_079 GND_080 GND_081 GND_082 GND_083 GND_084 GND_085 GND_086 GND_087 GND_088 GND_089 GND_090 GND_091 GND_092 GND_093 GND_094 GND_095 GND_096 GND_097 GND_098 GND_099 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114
AA7 AB7
N16S-GTR-S-A2
02V0A0000038
GND
GND
PLACE UNDER GPU
3.38A
C7532 1UF/6.3V /VGA
C7531 1UF/6.3V /VGA
C7526 0.1UF/16V /VGA
C7542 0.1UF/16V /VGA
C7533 4.7UF/6.3V /VGA
C7534 4.7UF/6.3V /VGA
GND
C7529 22UF/6.3V /VGA
C7535 10UF/6.3V /VGA
20151028 Kai Change to 0603
PLACE NEAR BGA
GND
+1.35VS_VGA
U7001D
12/14 FBVDDQ
B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 L22 L24 L26 M21 N21 R21 T21 V21 W21
FBVDDQ_01 FBVDDQ_02 FBVDDQ_03 FBVDDQ_04 FBVDDQ_05 FBVDDQ_06 FBVDDQ_07 FBVDDQ_08 FBVDDQ_09 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26 FBVDDQ_27
H24 H26 J21 K21
FBVDDQ_AON_1 FBVDDQ_AON_2 FBVDDQ_AON_3 FBVDDQ_AON_4
GF117 GF119 GK208
FBVDDQ FBVDDQ FBVDDQ FBVDDQ
N16S-GTR-S-A2
02V0A0000038
U7001C
14/14 XVDD/VDD33
0.2A
AD10 AD7
NC88 NC89
GM108
3V3_AON 3V3_AON
3V3_MAIN1 3V3_MAIN2 3V3_AON1 3V3_AON2
G8 G9 G10 G12
F11
NC86
FBA_CMD32
V5 V6
FERMI_RSVD1 FERMI_RSVD2
CONFIGURABLE POWER CHANNELS
* nc on substrate
G1 G2 G3 G4 G5 G6 G7
NC142 NC143 NC144 NC145 NC146 NC147 NC148
V1 V2
NC149 NC150
W1 W2 W3 W4
NC151 NC152 NC153 NC154
N16S-GTR-S-A2
02V0A0000038
C7538 0.1UF/16V /VGA
C7519 0.1UF/16V @
C7537 0.1UF/16V @
PLACE UNDER GPU
C7539 1UF/6.3V /VGA
C7536 4.7UF/6.3V /VGA
PLACE NEAR GPU
GND
R7505 0Ohm /VGA
+3VS_VGA
C7507 0.1UF/16V /VGA
C7501 0.1UF/16V /VGA
C7504 0.1UF/16V @
PLACE UNDER GPU
C7502 1UF/6.3V /VGA
C7503 4.7UF/6.3V /VGA
PLACE NEAR GPU
GND
/VGA
R7501 0Ohm
+3VS_AON_VGA
FB_CAL_VDDQ D22 +FB_CAL_PD_VDDQ R7504 1 /VGA 2 40.2Ohm 1%
FB_CAL_GND C24 +FB_CAL_PU_GND R7503 1 /VGA 2 40.2Ohm 1%
FB_CAL_TERM B25 +FB_CAL_TERM_GND R7502 1 /VGA 2 60.4Ohm 1%
PLACE CLOSE TO GPU BALLS
+1.35VS_VGA
GND
PEGATRON
Title : GPU(1)
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
Size Custom
Project Name P4
Rev 1.0
Date: Tuesday, September 06, 2016
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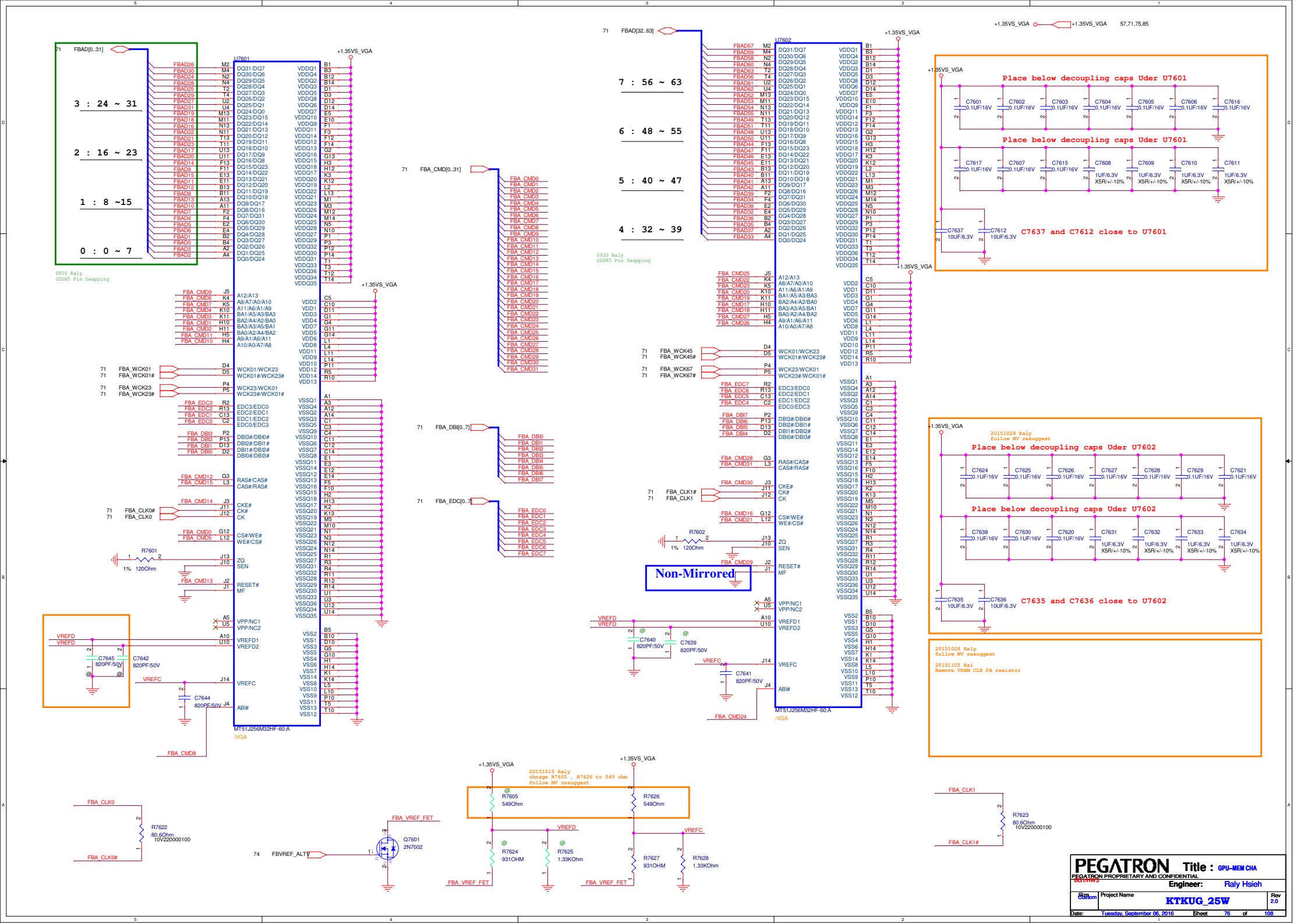
FBAD[0..31]
3 : 24 ~ 31
2 : 16 ~ 23
1 : 8 ~15
0 : 0 ~ 7
0930 Raly
GDDR5 Pin Swapping
U7601
MT51J256M32HF-60:A
/VGA
+1.35VS_VGA
FBA_CMD[0..31]
FBA_DBI[0..7]
FBA_EDC[0..7]
FBA_WCK01
FBA_WCK01#
FBA_WCK23
FBA_WCK23#
FBA_CLK0
FBA_CLK0#
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
FBA_CMD27
FBA_CMD28
FBA_CMD29
FBA_CMD30
FBA_CMD31
FBA_DBI0
FBA_DBI1
FBA_DBI2
FBA_DBI3
FBA_DBI4
FBA_DBI5
FBA_DBI6
FBA_DBI7
FBA_EDC0
FBA_EDC1
FBA_EDC2
FBA_EDC3
FBA_EDC4
FBA_EDC5
FBA_EDC6
FBA_EDC7
R7601
1% 120Ohm
R7602
1% 120Ohm
C7642
820PF/50V
C7644
820PF/50V
C7645
820PF/50V
R7622
80.6Ohm
10V220000100
Q7601
2N7002
FBA_VREF_FET
FBVREF_ALTY
R7605
549Ohm
R7624
931OHM
R7625
1.33KOhm
R7626
549Ohm
R7627
931OHM
R7628
1.33KOhm
20151015 Raly
chnage R7605 , R7626 to 549 ohm
follow NV resuggest
U7602
MT51J256M32HF-60:A
/VGA
7 : 56 ~ 63
6 : 48 ~ 55
5 : 40 ~ 47
4 : 32 ~ 39
FBAD[32..63]
Non-Mirrored
C7640
820PF/50V
C7639
820PF/50V
C7641
820PF/50V
R7623
80.6Ohm
10V220000100
Place below decoupling caps Uder U7601
C7601 0.1UF/16V
C7602 0.1UF/16V
C7603 0.1UF/16V
C7604 0.1UF/16V
C7605 0.1UF/16V
C7606 0.1UF/16V
C7616 0.1UF/16V
C7617 0.1UF/16V
C7607 0.1UF/16V
C7615 0.1UF/16V
C7608 1UF/6.3V X5R/+/-10%
C7609 1UF/6.3V X5R/+/-10%
C7610 1UF/6.3V X5R/+/-10%
C7611 1UF/6.3V X5R/+/-10%
C7637 10UF/6.3V
C7612 10UF/6.3V
C7637 and C7612 close to U7601
20151028 Raly
follow NV resuggest
Place below decoupling caps Uder U7602
C7624 0.1UF/16V
C7625 0.1UF/16V
C7626 0.1UF/16V
C7627 0.1UF/16V
C7628 0.1UF/16V
C7629 0.1UF/16V
C7621 0.1UF/16V
C7638 0.1UF/16V
C7630 0.1UF/16V
C7620 0.1UF/16V
C7631 1UF/6.3V X5R/+/-10%
C7632 1UF/6.3V X5R/+/-10%
C7633 1UF/6.3V X5R/+/-10%
C7634 1UF/6.3V X5R/+/-10%
C7635 10UF/6.3V
C7636 10UF/6.3V
C7635 and C7636 close to U7602
20151028 Raly
follow NV resuggest
20151105 Kai
Remove VRAM CLK PH resistor
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : GPU-MEM CHA
Engineer: Raly Hsieh
Size: Custom
Project Name: KTKUG_25W
Rev: 2.0
Date: Tuesday, September 06, 2016
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Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
Sheet	77 of 108

PEGATRON

Title : ****

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Raly Hsieh*

Size	Project Name	Rev
A	KTKUG_25W	1.0

Date: Tuesday, September 06, 2016 Sheet 78 of 99

PEGATRON

Title : ****

PEGATRON PROPRIETARY AND CONFIDENTIAL

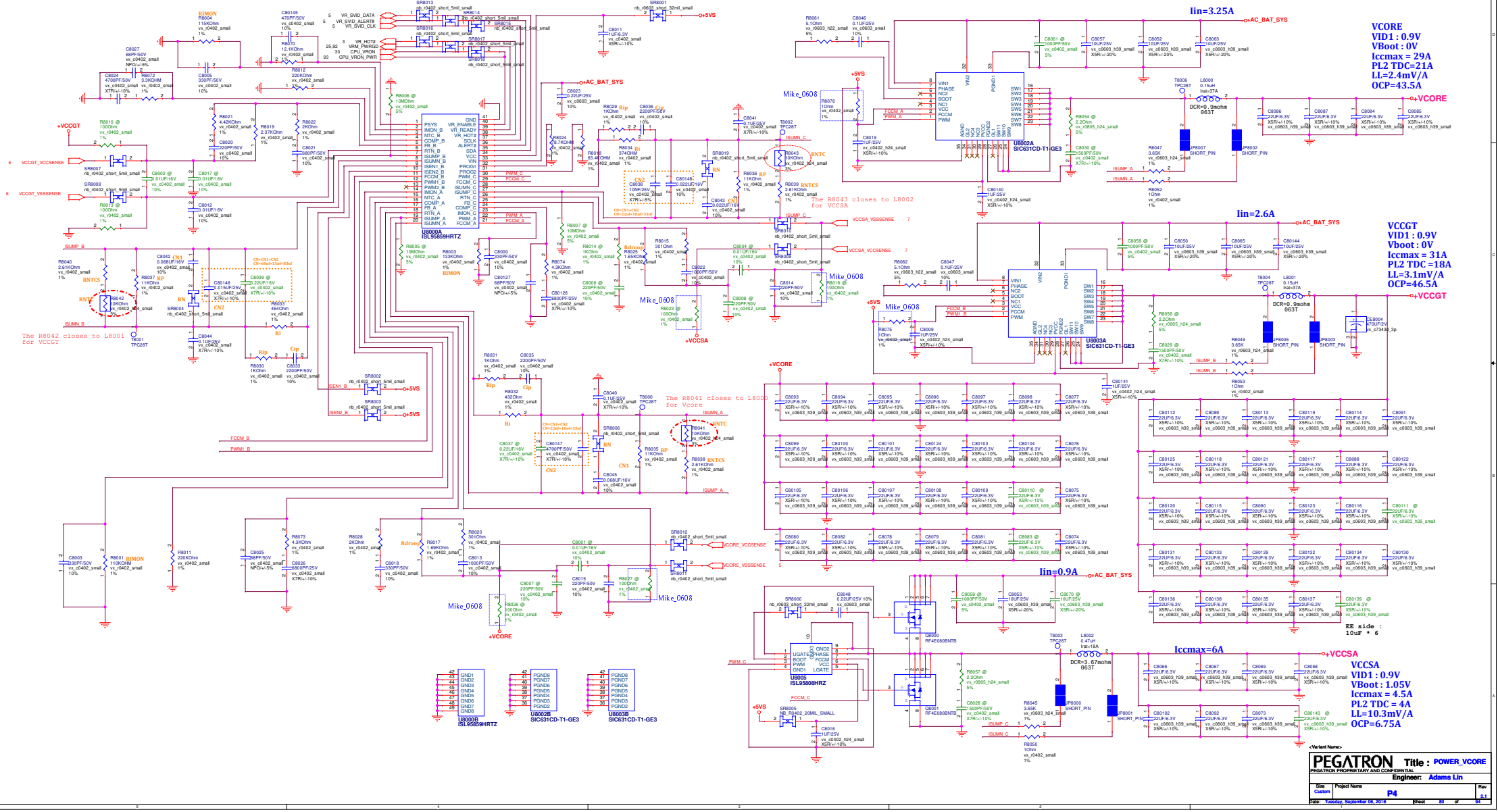
BG1/HW3

Engineer: *Raly Hsieh*

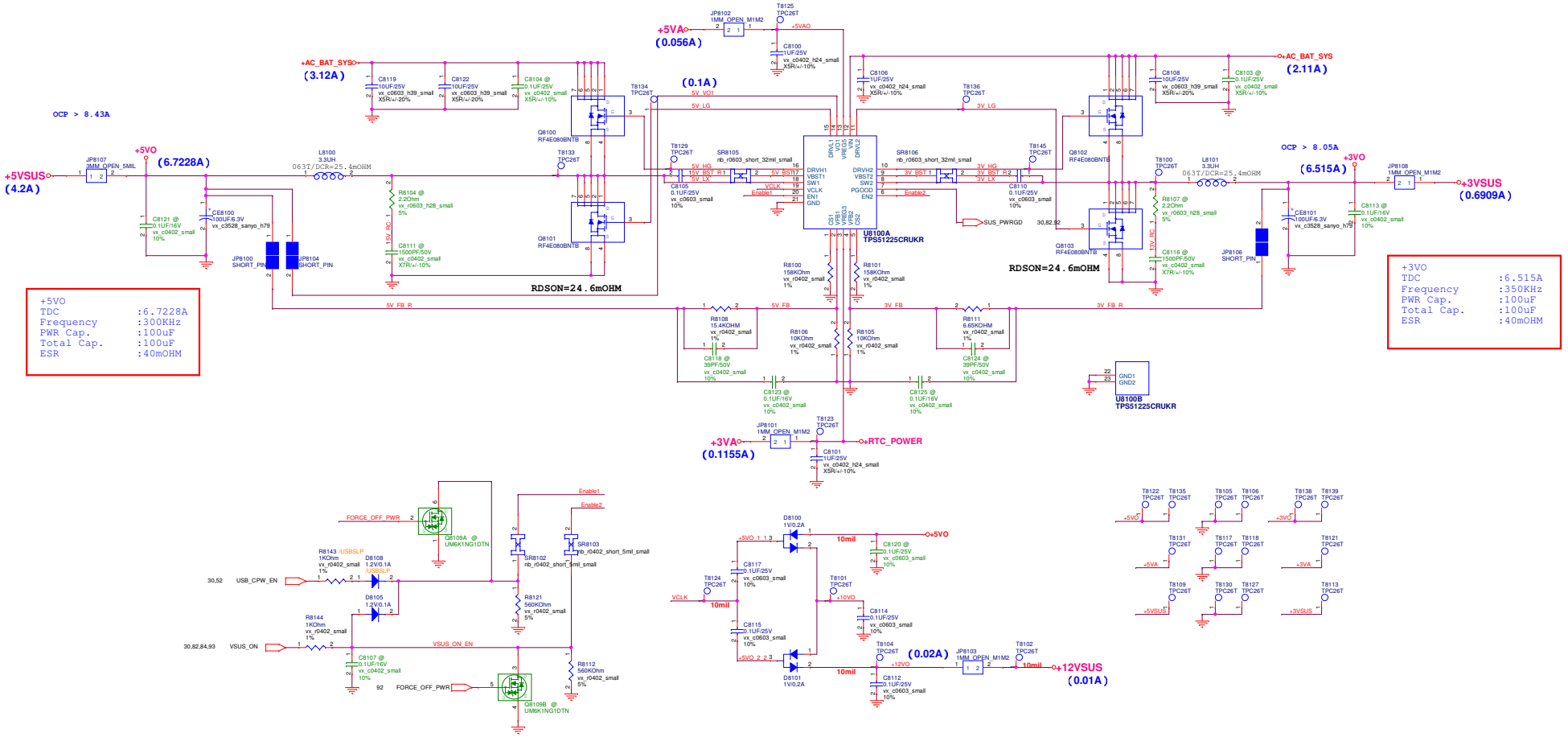
Size	Project Name	Rev
A	KTKUG_25W	1.0

Date: Tuesday, September 06, 2016 Sheet 79 of 99

VCORE & VCCGT & VCCSA POWER SUPPLY



5VO & 3VO POWER SUPPLY



PEGATRON Title : POWER_SYSTEM

PEGATRON PROPRIETARY AND CONFIDENTIAL

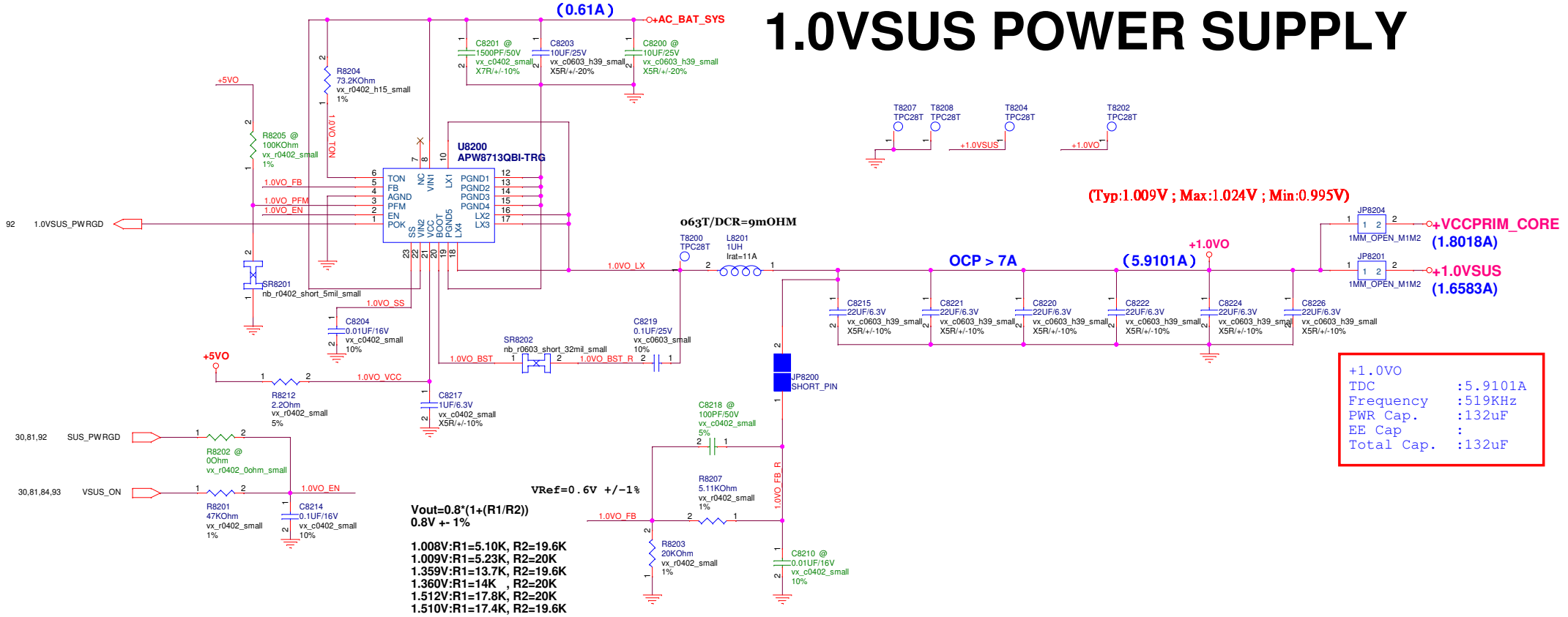
Engineer: Adams Lin

PG1-POWER

Size	Project Name	Rev
Custom	P4	0.1

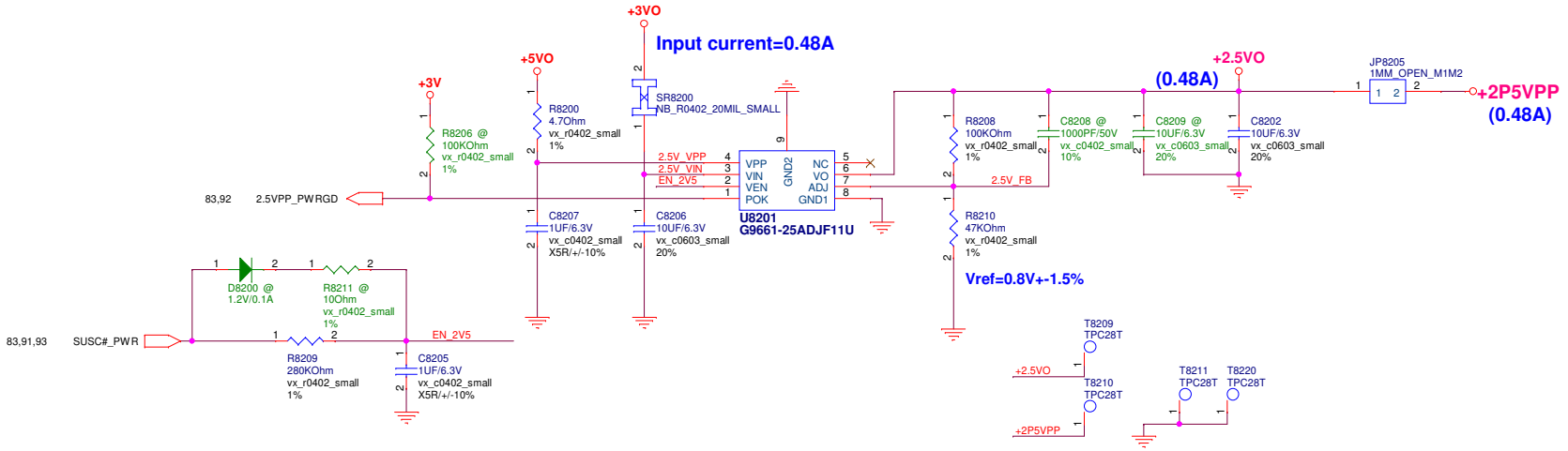
Date: Tuesday, September 06, 2016 Sheet 81 of 94

1.0VSUS POWER SUPPLY



+1.0VO	
TDC	:5.9101A
Frequency	:519KHz
PWR Cap.	:132uF
EE Cap	:
Total Cap.	:132uF

2.5V POWER SUPPLY



+2.5VO	
TDC	:0.48A
OCP	:3A
PWR Cap.	:20uF
EE Cap.	:10uF
Total Cap.	:30uF

<Variant Name>

PEGATRON
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Title : P82_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

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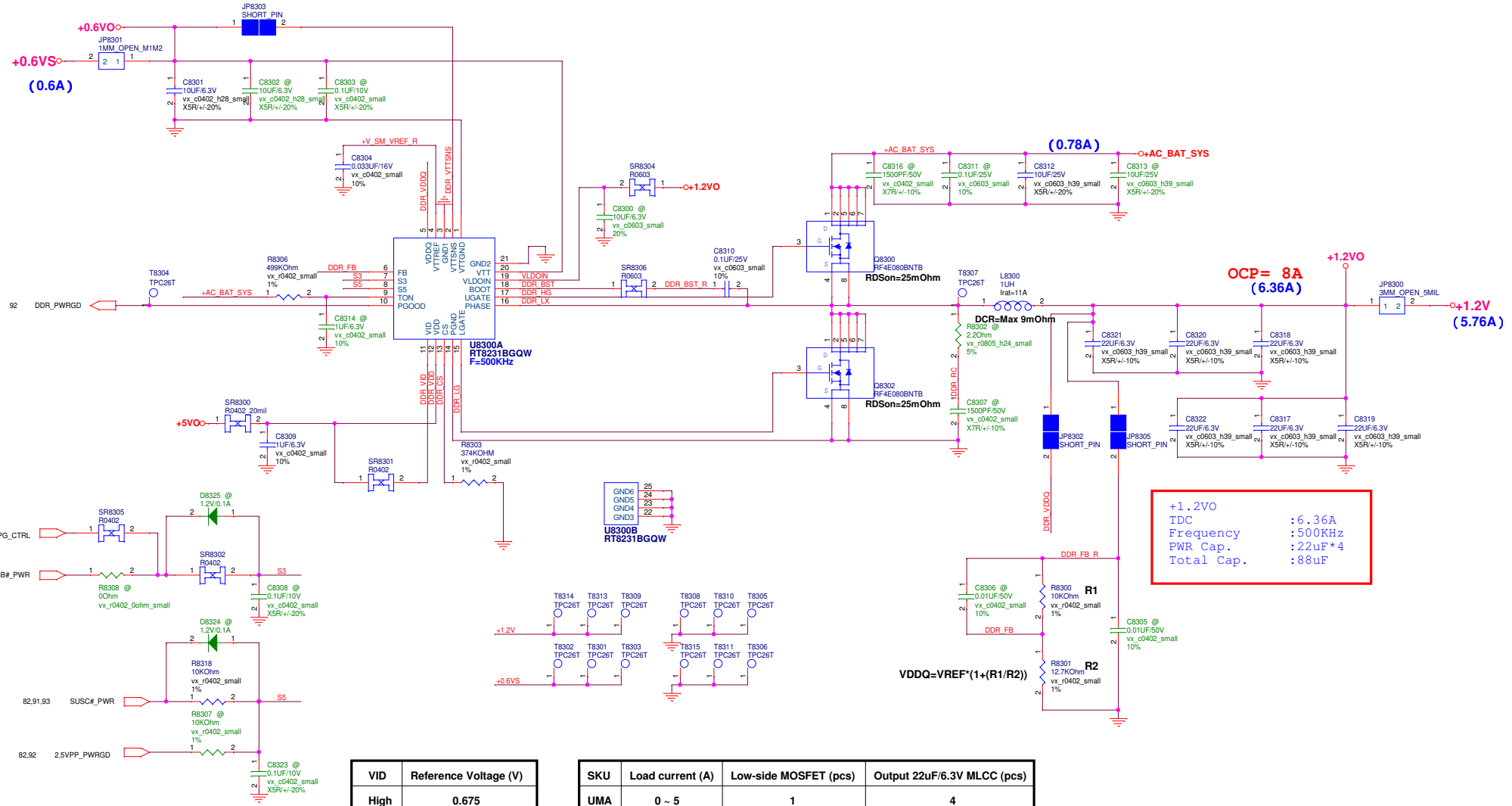
DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON Title : POWER_DDR & VTT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

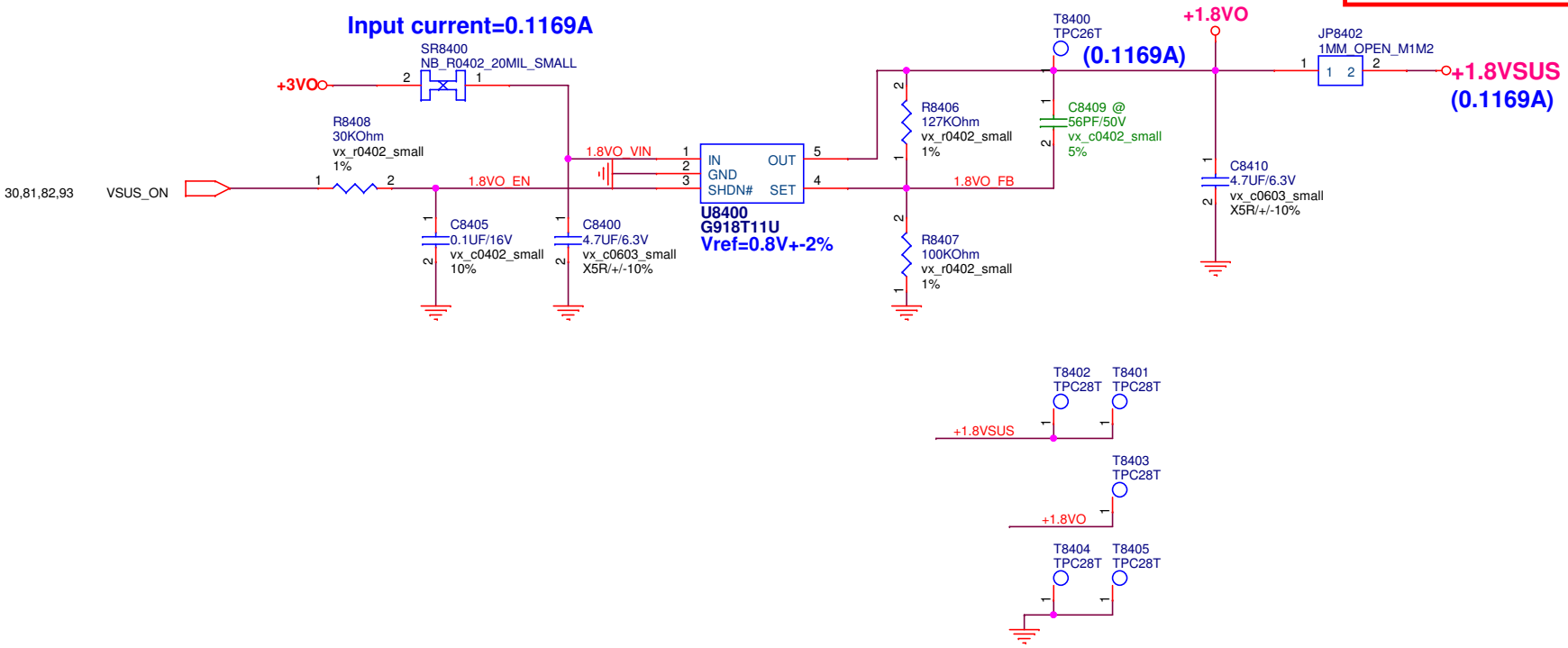
BG1-POWER

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 83 of 94

1.8VSUS POWER SUPPLY

+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

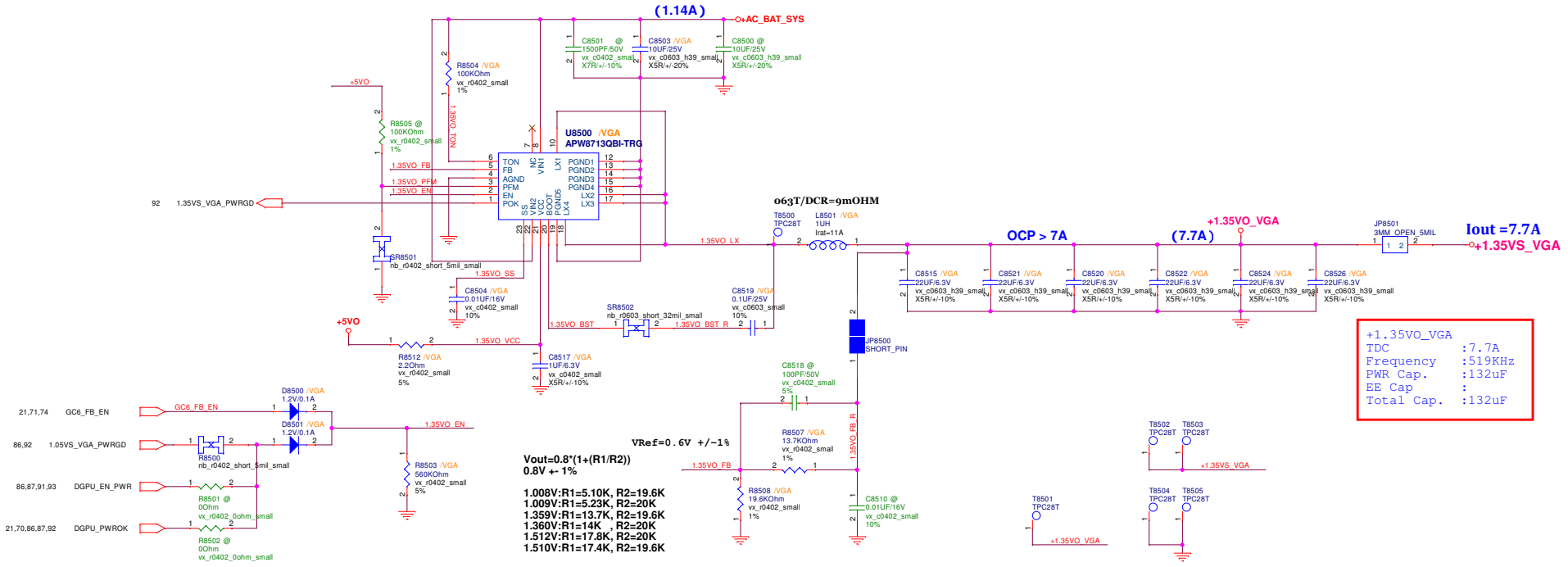
Title : POWER_+1.8VSUS

Engineer: Adams Lin

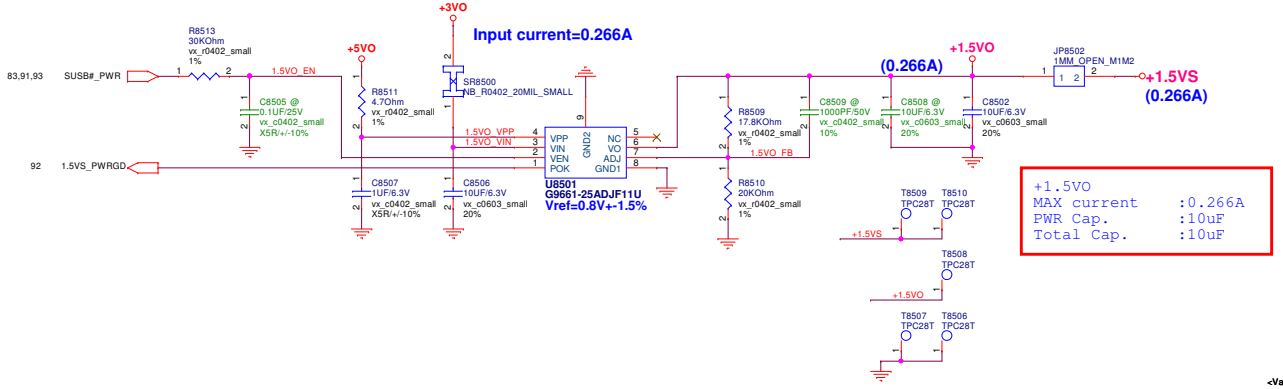
Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 84 of 94

1.35VS_VGA POWER SUPPLY



1.5VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+1.5VS

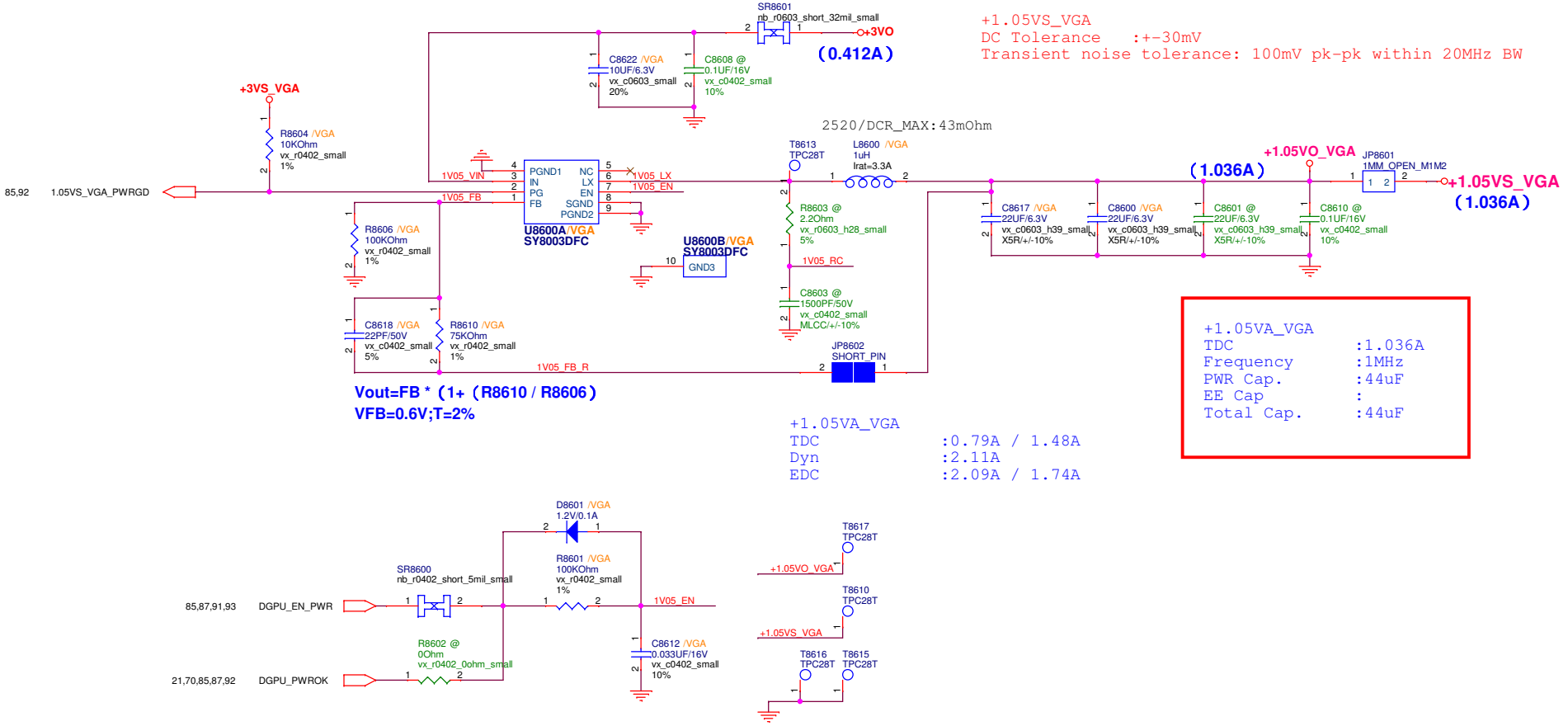
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 85 of 94

1.05VS_VGA POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : +1.05VS_VGA

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 86 of 94

VGA_CORE POWER SUPPLY

+VGA_VCORE(Package type:N16VS-GT)
DC Tolerance :+-20mV

Overshoot/undershoot
Transient noise tolerance: -10% ~ +20% within 20MHz BW
High frequency noise: 400mV pk-pk within 1GHz BW

VID:0.6V ~ 1.2V
Number of programmable Volt: 96 levels
Programmable volt steps: 6.25mV
Settling Time: < 100us for rising, no restriction on falling

	N16	N16S_GT
R8723	39K	20K
R8721	39K	20K
R8716	1.5K	2K
R8713	31.5K	18K
C8720	>1.8nF	2.7nF
Vstep	6.25mV	6.25mV
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.875V	0.9V
openVR Config	A	B

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

2 PHASE 25W
N16S-GT
EDP=51A
TDC=26A
DYN= A
OCP:62A

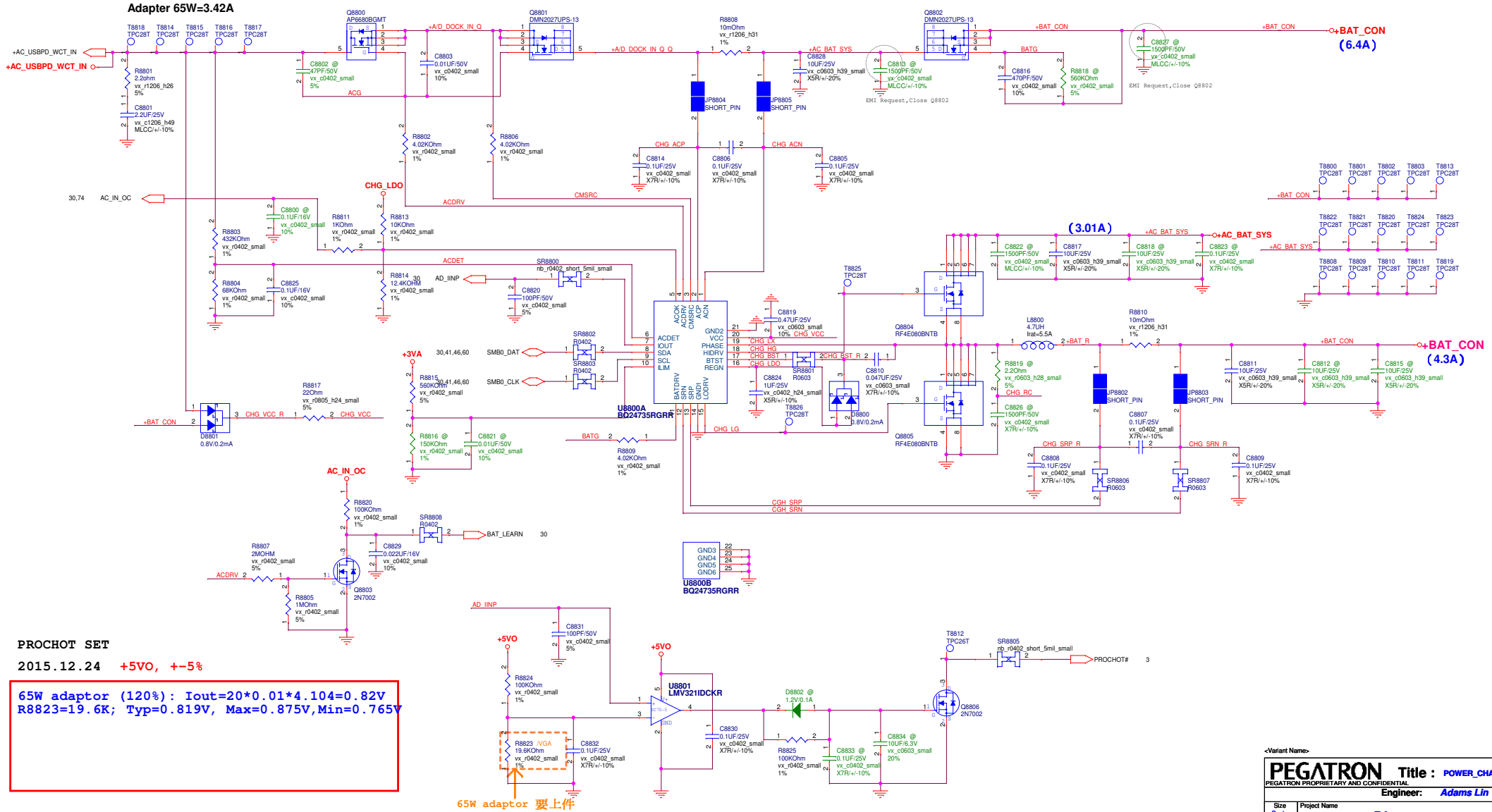
+VGA_VCORE (2 Phase)
TDC :30A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

EE side pull high OHM check

<Variant Name>

PEGATRON Title : +VGA_VCORE
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin
Size Custom | Project Name P4 | Rev 2.1
Date: Tuesday, September 06, 2016 | Sheet 87 of 94

BATTERY CHARGER



<variant_name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

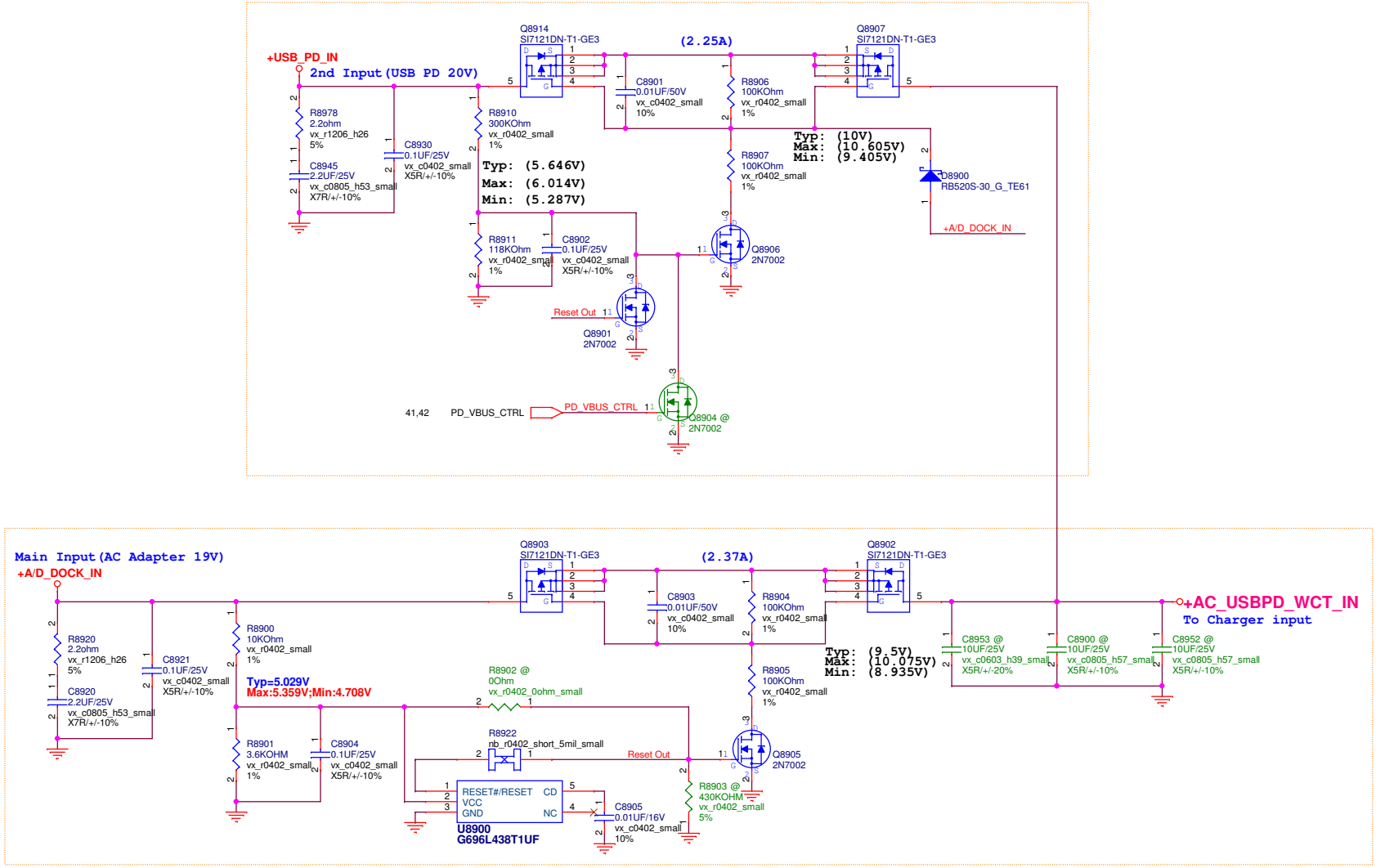
Title : POWER_CHARGER

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 88 of 94

2 Input switch Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

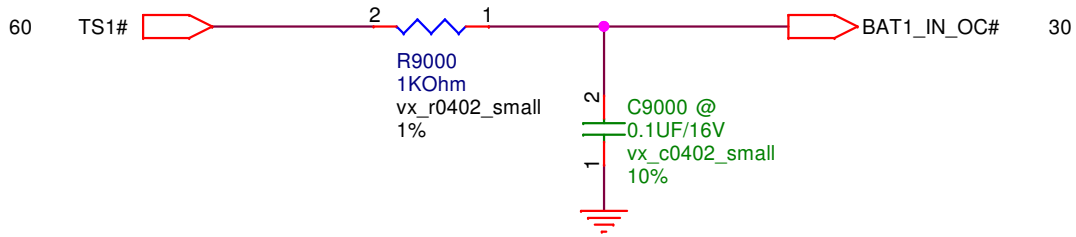
Title : AC&PD S.W.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 89 of 94

BATTERY IN DETECT



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

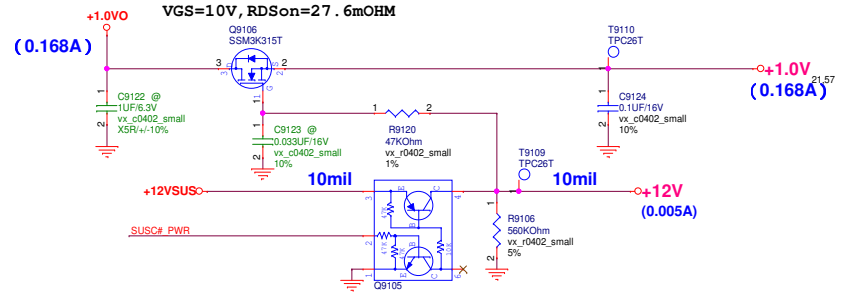
Title : POWER_DETECT

Engineer: Adams Lin

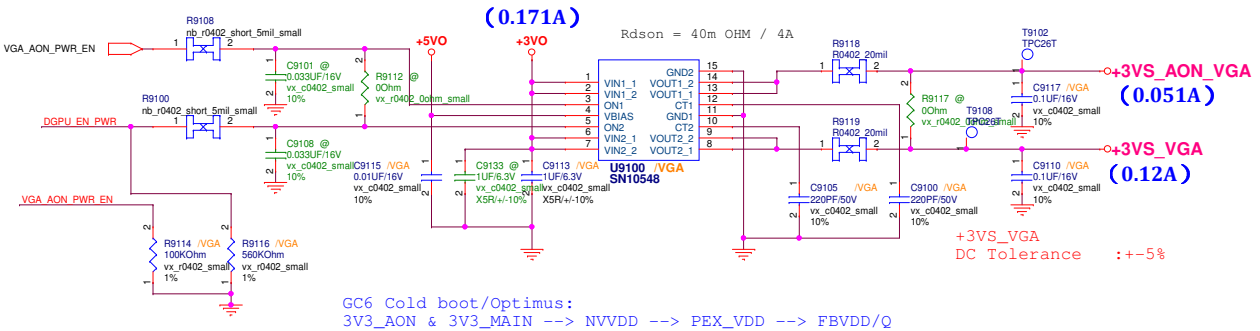
Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 90 of 94

SUSC#_PWR POWER SUSB#_PWR POWER

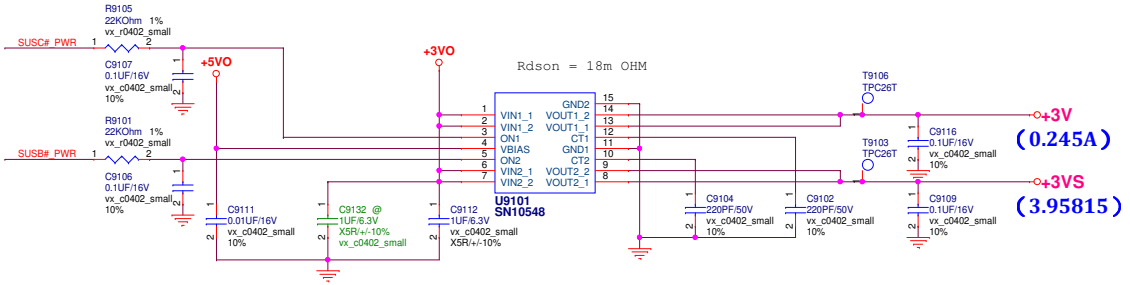


DSC_VGA_PWR POWER



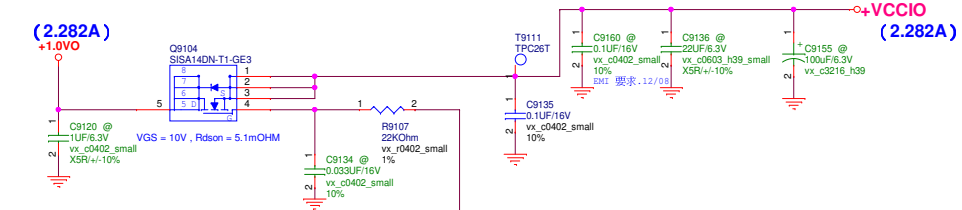
GC6 Cold boot/Optimus:
3V3_AON & 3V3_MAIN --> NVVDD --> PEX_VDD --> FBVDD/Q

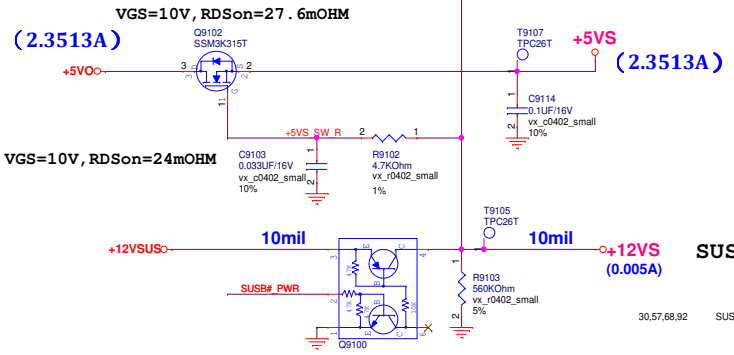
GC6 2.0 Exit:
3V3_MAIN --> NVVDD --> PEX_VDD



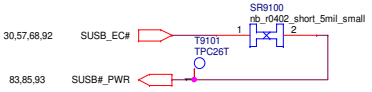
Power up Sequencing
1.The ramp time for any rail must be 40us and
  is recommended to be less than 2ms
2.The previous power rail must ramp up to 90%
  before the next power rail can start ramping up

Power down Sequencing
1.There is no specific power down sequence
2.Residual voltage from power down must not violate ther power up sequence
  when back to back GPU power down and power up event take place



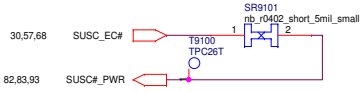


SUSB#_PWR POWER Control



DSC_VGA_PWR POWER Control

SUSC#_PWR POWER Control



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

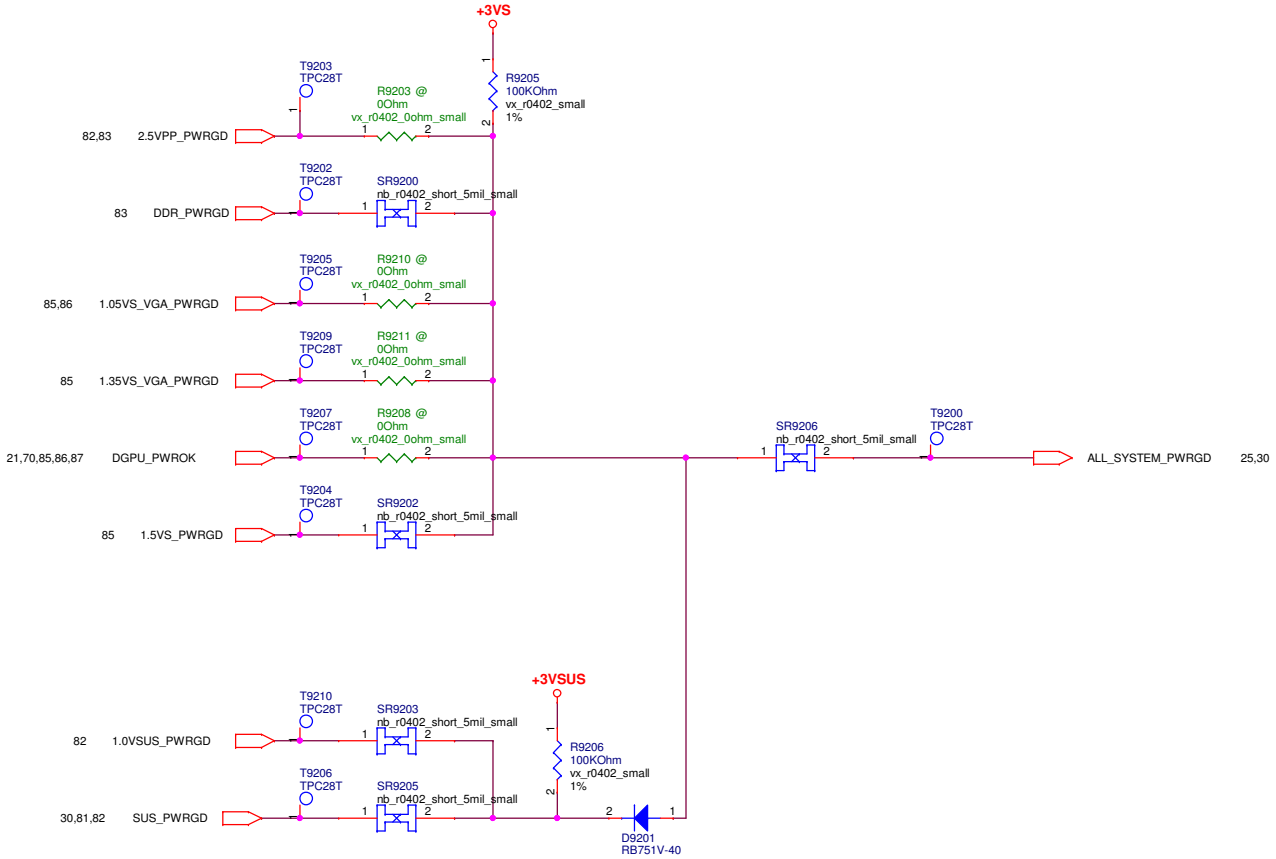
Title : POWER_LOAD SWITCH

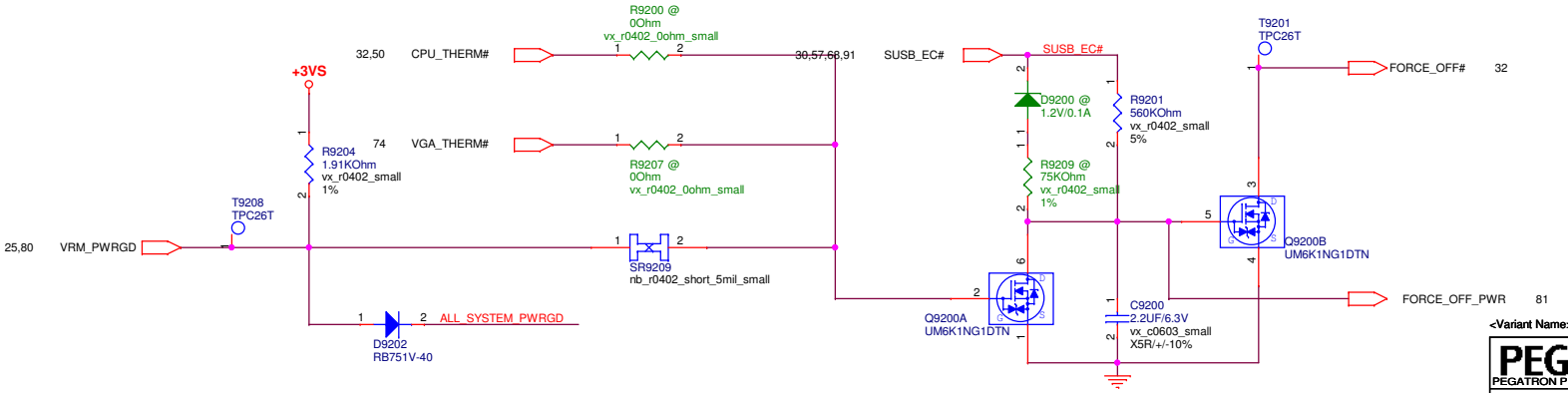
Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 91 of 94

POWER GOOD DETECTER





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 92 of 94

+USB_PD_IN → +USB_PD_IN 42,89
+A/D_DOCK_IN → +A/D_DOCK_IN 60,89
+AC_USBPD_WCT_IN → +AC_USBPD_WCT_IN 88,89
+AC_BAT_SYS → +AC_BAT_SYS 43,45,80,81,82,83,85,87,88
+BAT_CON → +BAT_CON 60,88
+RTC_POWER → +RTC_POWER 81

+5VA → +5VA 31,56,81
+3VA → +3VA 24,30,31,36,41,43,53,56,57,67,81,88

+5VO → +5VO 26,81,82,83,85,88,91
+3VO → +3VO 81,82,84,85,86,91
+2.5VO → +2.5VO 82
+1.8VO → +1.8VO 84
+1.5VO → +1.5VO 85

+1.2VO → +1.2VO 83
+1.05VO_VGA → +1.05VO_VGA 86
+1.0VO → +1.0VO 82,91
+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91
+5VSUS → +5VSUS 41,42,52,56,67,81
+3VSUS → +3VSUS 4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+1.8VSUS → +1.8VSUS 9,21,24,26,84
+1.0VSUS → +1.0VSUS 26,82

+12V → +12V 91
+2P5VPP → +2P5VPP 16,17,57,82
+1.2V → +1.2V 4,7,15,16,17,18,57,83
+1.0V → +1.0V 7,57,91

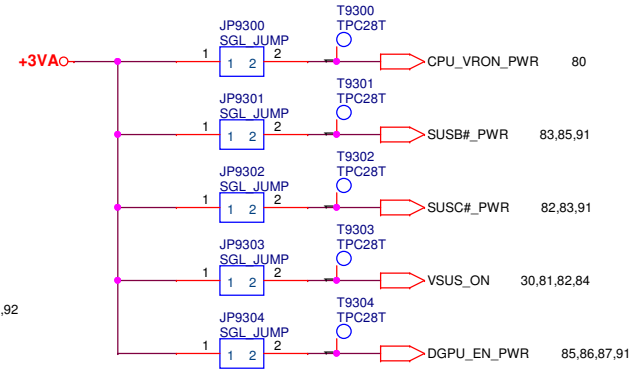
+12VS → +12VS 28,31,57,62,91
+5VS → +5VS 31,36,45,46,48,50,51,56,57,67,80,87,91
+3VS → +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

+1.5VS → +1.5VS 36,57,85

+1.05VS_VGA → +1.05VS_VGA 57,70,71,72,86
+0.6VS → +0.6VS 15,17,57,83

+VCORE → +VCORE 5,57,80
+VCCGT → +VCCGT 6,57,80
+VCCSA → +VCCSA 7,57,80
+VCCIO → +VCCIO 3,7,57,91
+VCCPRIM_CORE → +VCCPRIM_CORE 26,82
+VGA_VCORE → +VGA_VCORE 57,75,87

FOR POWER TEST



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

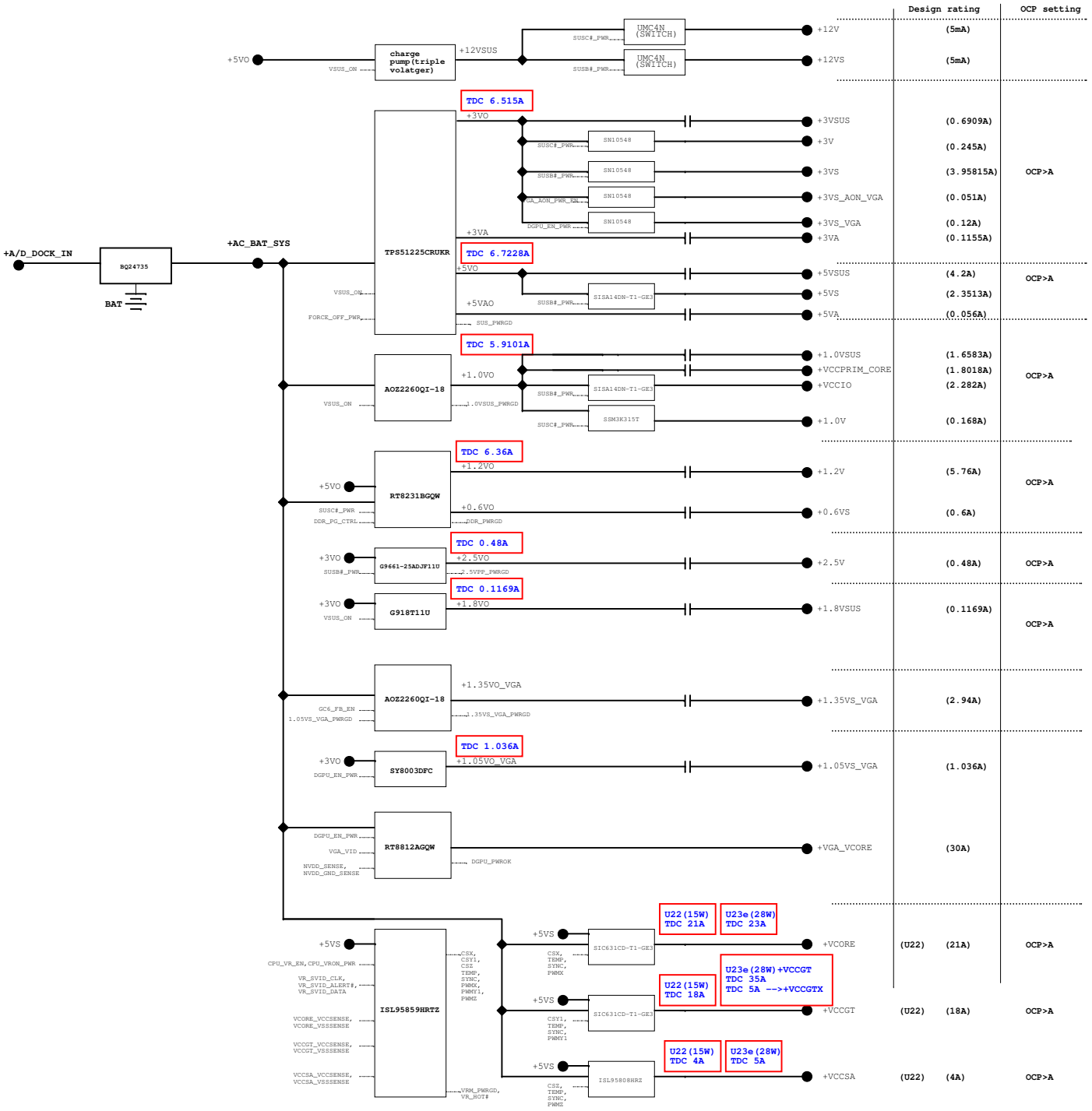
Title : POWER_SIGNAL

BG1-POWER

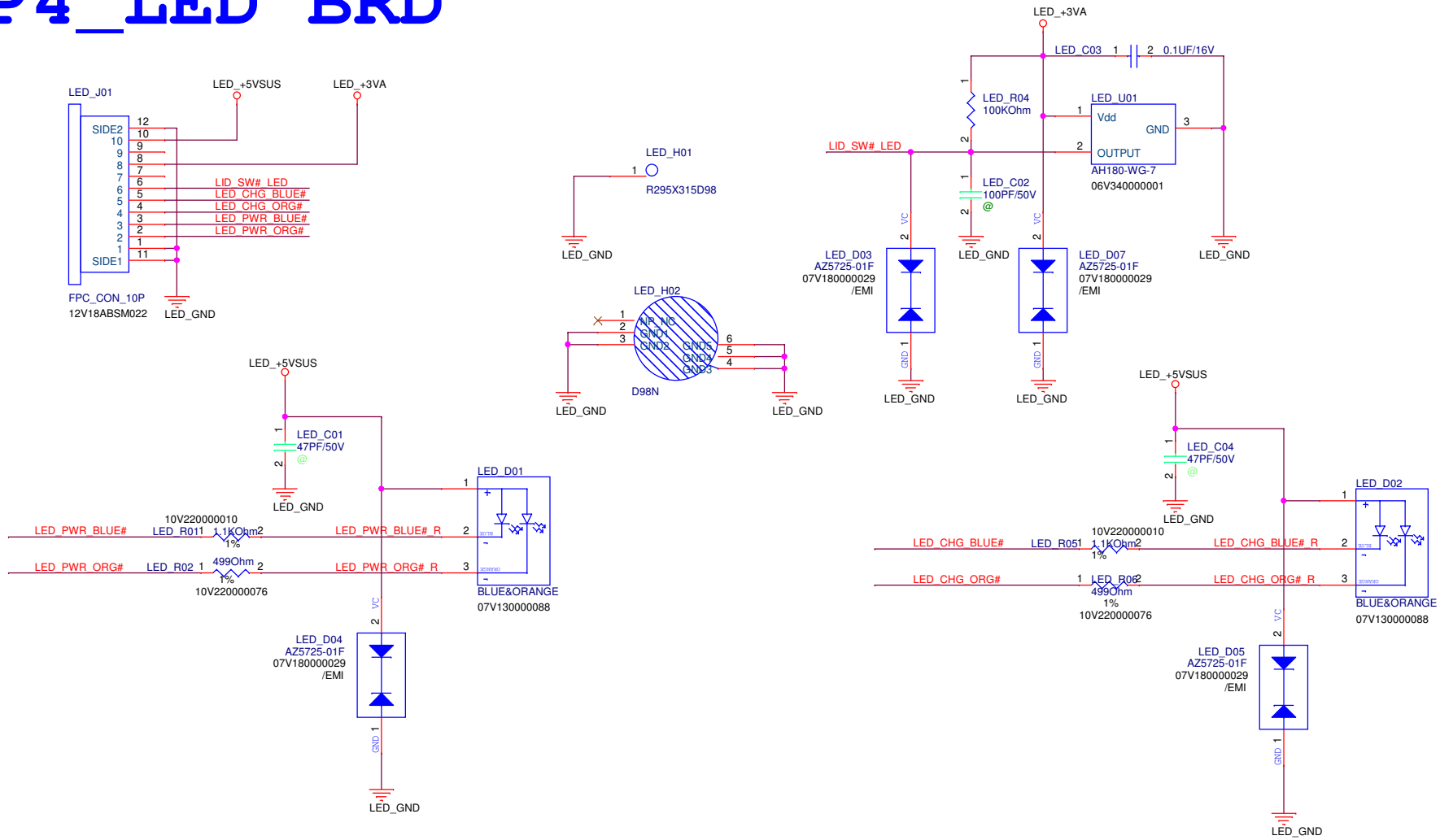
Engineer: Adams Lin

Size	Project Name	Rev
B	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 93 of 94


Design rating
OCP setting
+A/D_DOCK_IN
BQ24735
BAT
+AC_BAT_SYS
+5VO
VSUS_ON
charge pump(triple volatger)
+12VSUS
SUSC#_PWR
UMC4N (SWITCH)
SUSB#_PWR
UMC4N (SWITCH)
+12V
(5mA)
+12VS
(5mA)
TPS51225CRUKR
TDC 6.515A
+3VO
SUSC#_PWR
SN10548
SUSB#_PWR
SN10548
SN10548
DGPU_EN_PWR
SN10548
+3VSUS
(0.6909A)
+3V
(0.245A)
+3VS
(3.95815A)
OCP>A
+3VS_AON_VGA
(0.051A)
+3VS_VGA
(0.12A)
+3VA
TDC 6.7228A
+5VO
+5VSUS
(4.2A)
OCP>A
+5VS
(2.3513A)
SUSB#_PWR
SISA14DN-T1-GE3
+5VAO
FORCE_OFF_PWR
SUS_PWRGD
+5VA
(0.056A)
AOZ2260QI-18
TDC 5.9101A
+1.0VO
VSUS_ON
1.0VSUS_PWRGD
SUSB#_PWR
SISA14DN-T1-GE3
SUSC#_PWR
SSM3K315T
+1.0VSUS
(1.6583A)
+VCCPRIM_CORE
(1.8018A)
+VCCIO
(2.282A)
OCP>A
+1.0V
(0.168A)
RT8231BGQW
TDC 6.36A
+5VO
+1.2VO
SUSC#_PWR
DDR_PG_CTRL
+0.6VO
DDR_PWRGD
+1.2V
(5.76A)
OCP>A
+0.6VS
(0.6A)
G9661-25ADJF11U
TDC 0.48A
+3VO
SUSB#_PWR
+2.5VO
2.5VPP_PWRGD
+2.5V
(0.48A)
OCP>A
G918T11U
TDC 0.1169A
+3VO
VSUS_ON
+1.8VO
+1.8VSUS
(0.1169A)
OCP>A
AOZ2260QI-18
+1.35VO_VGA
GC6_FB_EN
1.05VS_VGA_PWRGD
1.35VS_VGA_PWRGD
+1.35VS_VGA
(2.94A)
SY8003DFC
TDC 1.036A
+3VO
DGPU_EN_PWR
+1.05VO_VGA
+1.05VS_VGA
(1.036A)
RT8812AGQW
DGPU_EN_PWR
VGA_VID
NVDD_SENSE,
NVDD_GND_SENSE
DGPU_PWROK
+VGA_VCORE
(30A)
ISL95859HRTZ
+5VS
CPU_VR_EN,CPU_VRON_PWR
VR_SVID_CLK,
VR_SVID_ALERT#,
VR_SVID_DATA
VCORE_VCCSENSE,
VCORE_VSSSENSE
VCCGT_VCCSENSE,
VCCGT_VSSSENSE
VCCSA_VCCSENSE,
VCCSA_VSSSENSE
CSX,
CSY1,
CSZ,
TEMP,
SYNC,
PWMX,
PWMY1,
PWMZ
VRM_PWRGD,
VR_HOT#
SIC631CD-T1-GE3
CSX,
TEMP,
SYNC,
PWMX
U22(15W)
TDC 21A
U23e(28W)
TDC 23A
+VCORE
(U22)
(21A)
OCP>A
SIC631CD-T1-GE3
CSY1,
TEMP,
SYNC,
PWMY1
U22(15W)
TDC 18A
U23e(28W)+VCCGT
TDC 35A
TDC 5A -->+VCCGTX
+VCCGT
(U22)
(18A)
OCP>A
ISL95808HRZ
CSZ,
TEMP,
SYNC,
PWMZ
U22(15W)
TDC 4A
U23e(28W)
TDC 5A
+VCCSA
(U22)
(4A)
OCP>A

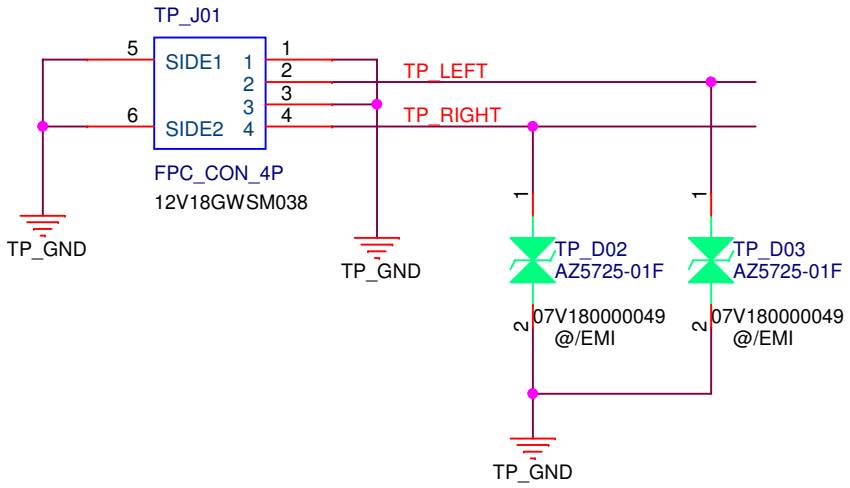
P4_LED BRD

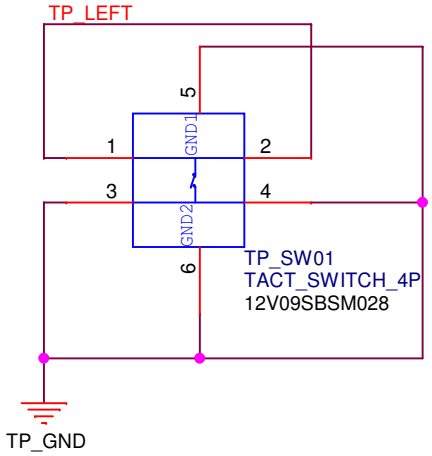


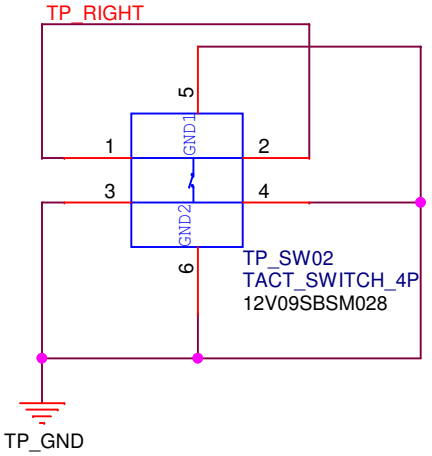
PEGATRON	Title : P4_LED BRD		
BG1/HW3	Engineer: Bill Yang		
Size: Custom	Project Name: P4	P/N	Rev: 1.0
Date: Tuesday, September 06, 2016	Sheet 104 of 110		

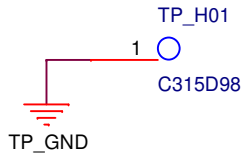
P4_TP-button BRD

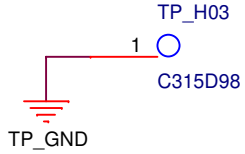
TP_BRD to TP_Model

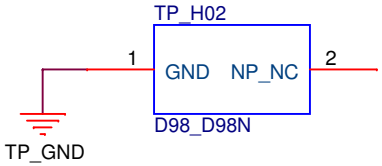


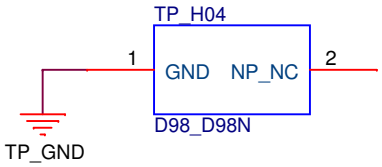




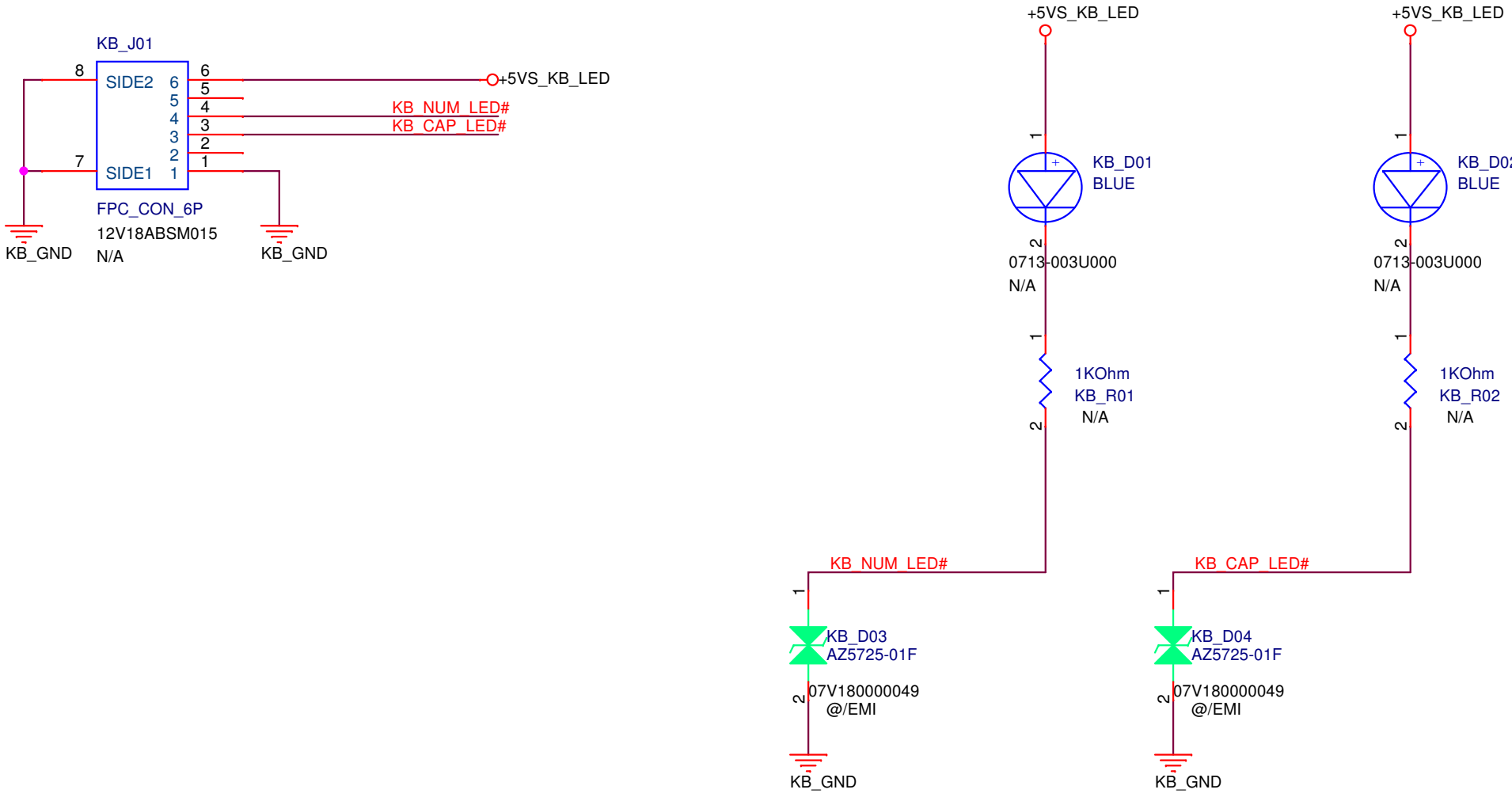








PEGATRON	Title : P4_TP-button BRD	
BG1/HW3	Engineer: Bill Yang	
Size: Custom	Project Name: P4	Rev: 1.0
	P/N:	
Date: Tuesday, September 06, 2016	Sheet 105 of 110	



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : P4_KB LED

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.1

Date: Tuesday, September 06, 2016 Sheet 106 of 108