PCB NO :DAB0007Z000

SIF BOM P/N : 431AP231L01

ARK BOM P/N : 431AP231L09

Compal Confidential

TGL-H MB Schematic Document

LA-K452P

Rev: 1.0

2021.03.19

ZZZ

PCB 36U LA-K452P REV0 M/B GN20E 1 S
DAB0007Z000
PCB@

@ : Un-pop Component
DIS@/UMA@ : GPU Support
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CONN@ : Connector Component
SW@ : Debug PWR Button

CNV@/@CNV@ : CNVi Support
G3@ : EC G3 Flash Sharing
BBY@ : For SIF BBY Function Detect
XMP@ : For XMP DRAM

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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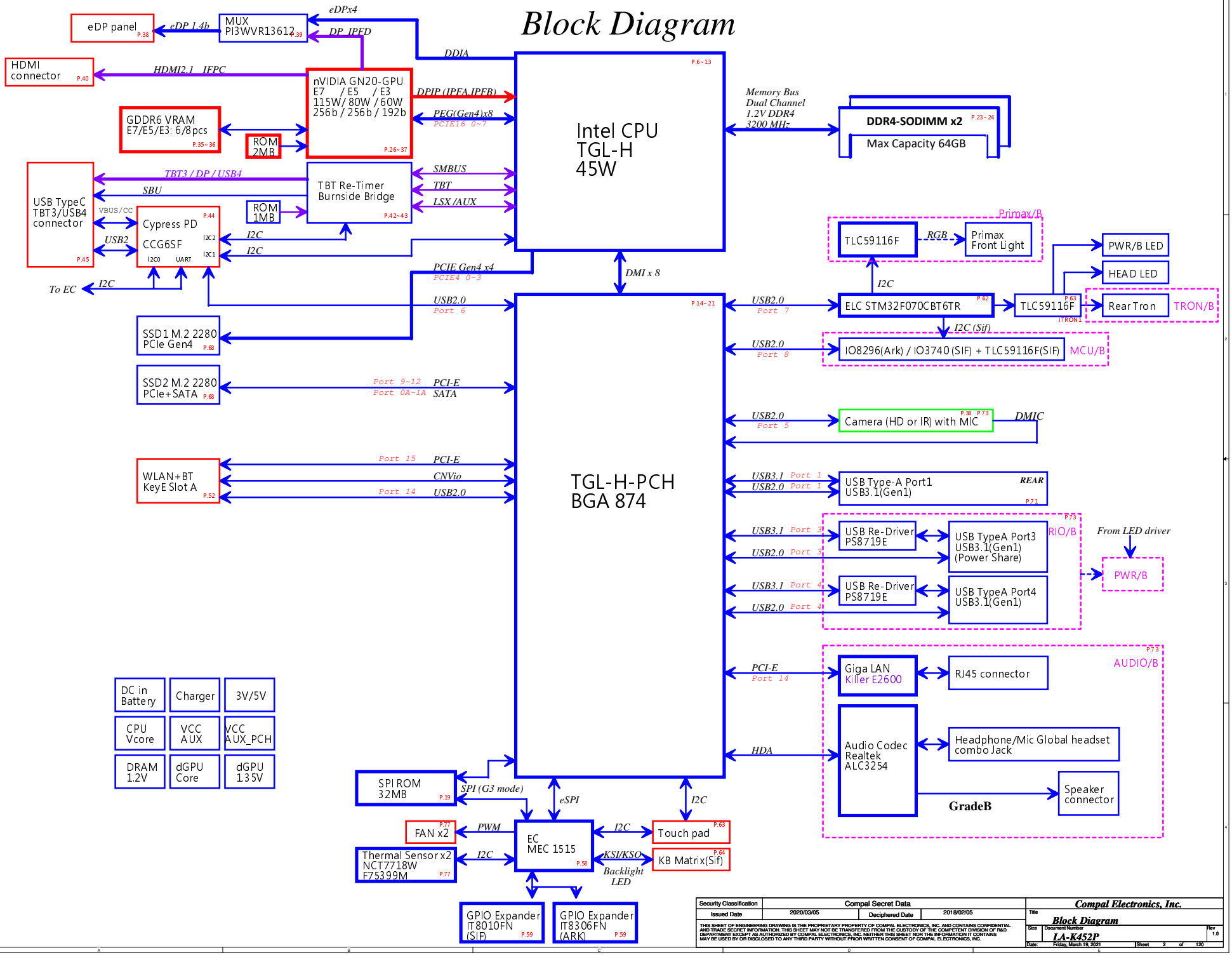
Title: Cover Sheet			
Size: Custom	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 1 of 120		

Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Title: Block Diagram			
Size	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 2 of 120		

Board ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	
2	100	17.8K	2.801	EVT
3	100	27K	2.598	
4	100	37.4K	2.402	DVT1
5	100	49.9K	2.201	DVT2
6	100	64.9K	2.001	
7	100	82.5K	1.808	Pilot
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Port	Power Rail	Device	Address
PCH_SMBCLK PCH_SMBDATA	+3VALW_PCH	JDIMM1	
		JDIMM2	

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address
GPU_THM_SMBCLK GPU_THM_SMBDAT	+3VS	MCU	0xC2
		Thermal 1 Thermal 2	0x98h 0x9Ah
		GPU	TBD
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT	+3VALW_EC	BAT	
		CHGR	
DAT_TP_SIO_I2C_CLK CLK_TP_SIO_I2C_DAT	+TP_VDD	Touch Pad	TBD
	+3VALW_EC	IT8010	0x40 0x42
UPD1_SMBCLK UPD1_SMBDAT	+3V_VSYS	CCG6	0x08

TGL-H-PCH HM570

HSIO	USB3.1	PCIe	SATA3	Function
0	1			JUSB
1	2			JUSB
2	3			JUSB
3	4			JUSB
4	5			
5	6			
6	7	1		
7	8	2		
8	9	3		
9	10	4		
10		5		
11		6		
12		7		
13		8		
14				DMI x8
15				
16				
17				
18				
19				
20				
21				
22		9		JSSD2 , 2280 SATA x2 / PCIe x4
23		10		
24		11	0A	
25		12	1A	
26		13	0B	
27		14	1B	LAN
28		15	2	WLAN
29		16	3	

USB2	Function
1	JUSB
2	JUSB
3	JUSB
4	JUSB
5	HD+IR CAM
6	CPU side Type C
7	ELC MCU
8	Per key MCU
9	Finger Print
10	
11	
12	
13	
14	Bluetooth

Symbol Note :

Digital Ground

Analog Ground

60 mils/1A = 1/3 oz
40 mils/1A = 0.5 oz
20 mils/1A = 1 oz
10 mils/1A = 2 oz

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+12.6V_BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCCIN	CPU FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX	PCH FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX_PCH	PCH power supply	ON	OFF	OFF	OFF	OFF
+3.3V_BAT_LDO	RTC power	ON	ON	ON	ON	ON
+RTC_CELL	+3.3V_BAT_LDO/+3VLP for suspend power	ON	ON	ON	ON	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW Primary Power Well for PCH	ON	ON	ON	ON*	OFF
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.05VO_OUT_FET	System +1.05V power rail	ON	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+2.5V_MEM	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF	OFF
+1.05V_VCCSTG	Gated version of VCCST	ON	OFF	OFF	OFF	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+1.8V_RUN	System +1.8VS power rail	ON	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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Compal Electronics, Inc.

Title: Notes List

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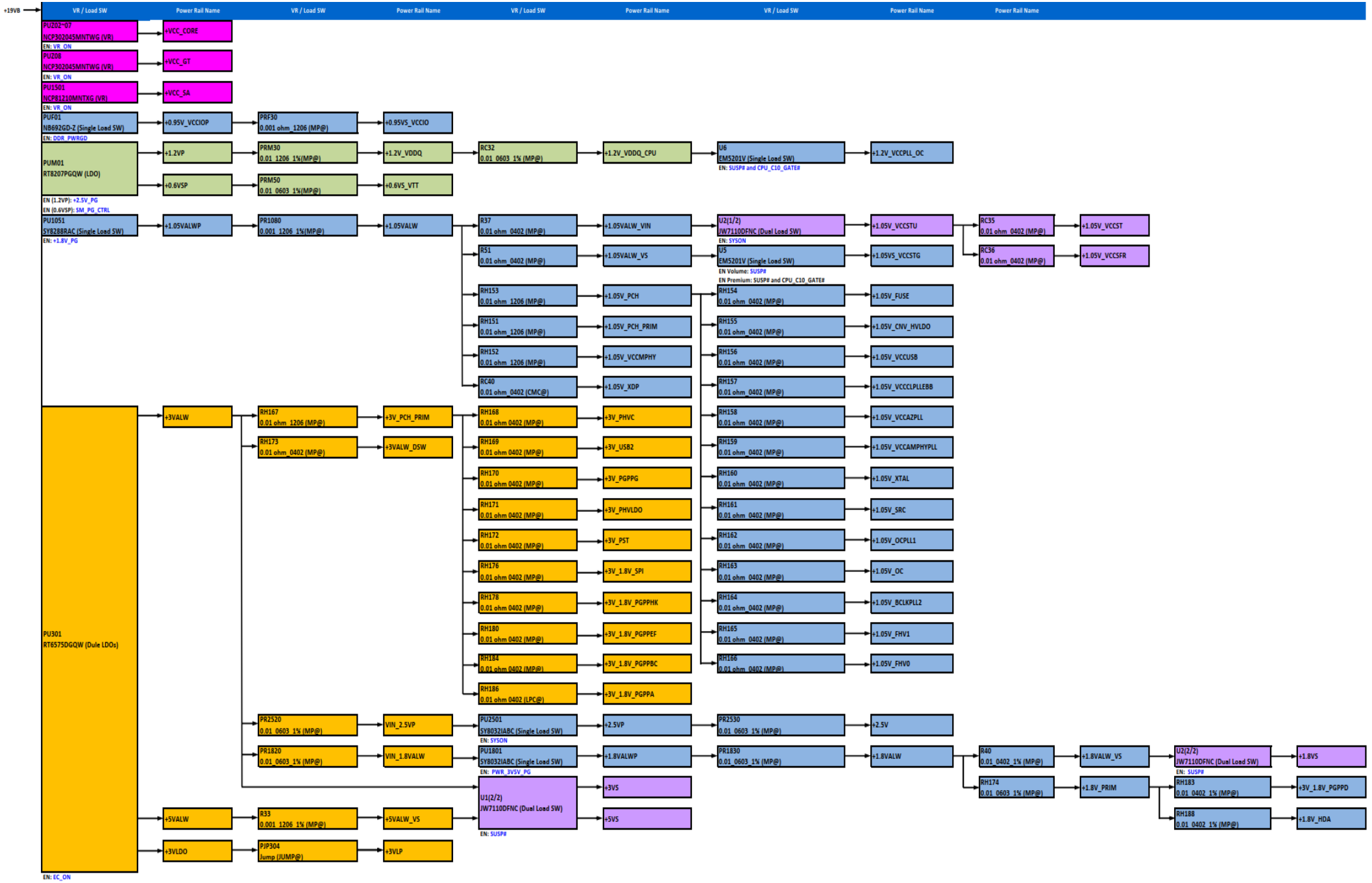
Date: Friday, March 19, 2021 | Sheet 3 of 120



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Issued Date	2020/03/05	Deciphered Date	2021/12/31

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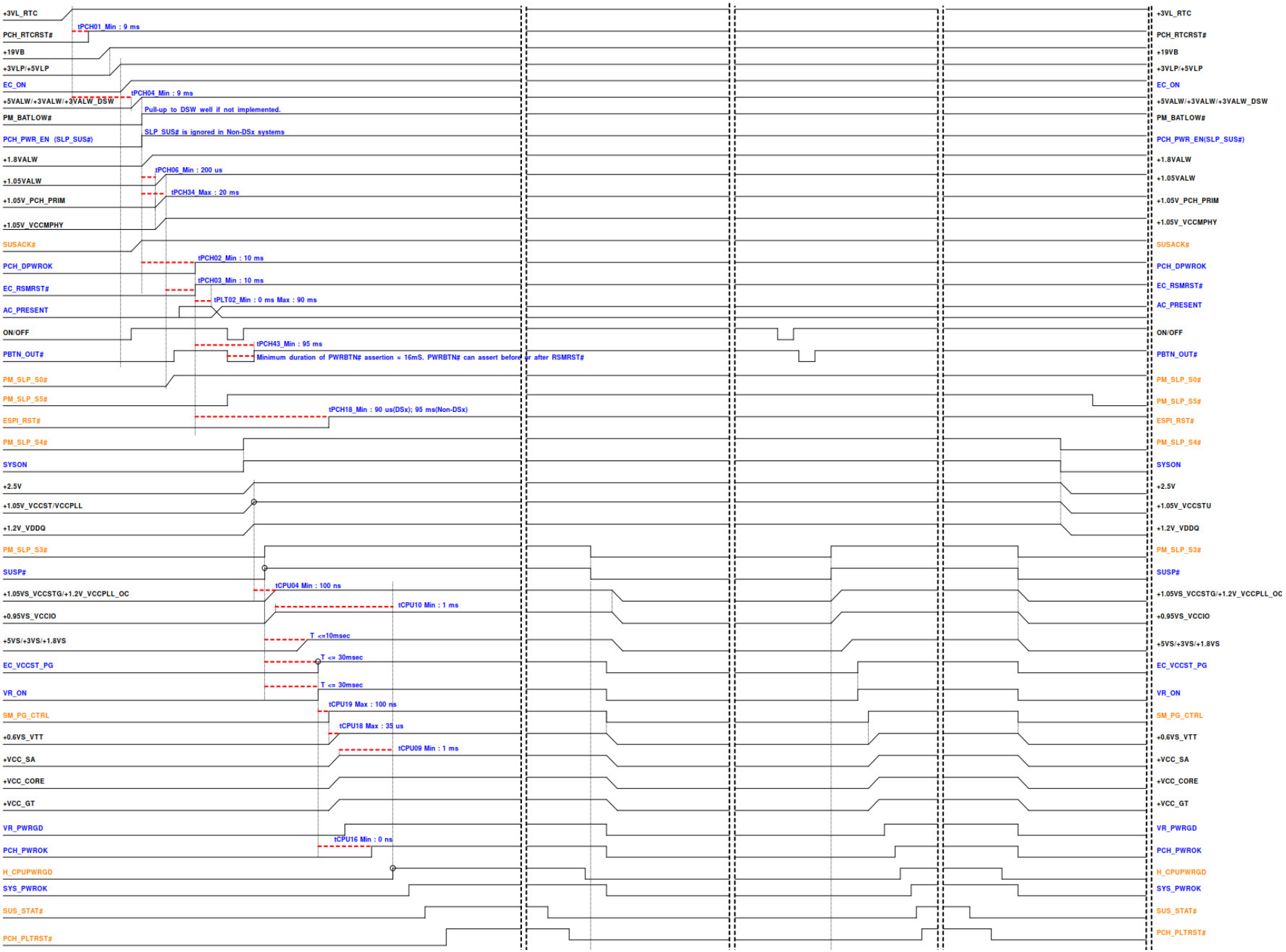
Compal Electronics, Inc.

Title: Power Map

Size	Document Number	Rev
Custom	LA-K452P	1.0

Date: Friday, March 19, 2021 Sheet 4 of 120



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Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 5 of 120

UC1 CPU@

TGL-H i7
SA0000DYK0L

10/19 DVT1 update

CPU DVT1:

UC1 CPU_I7_I9@

S IC A31 CL8069004569206 QWCB P0 2.6G S
SA0000E4K0L

UC1 CPU_I5@

S IC A31 CL8069004569204 QWCC P0 1.8G S
SA0000DYU1L

01/22 DVT2 update

CPU DVT2:

UC1 CPU_I5_QS@

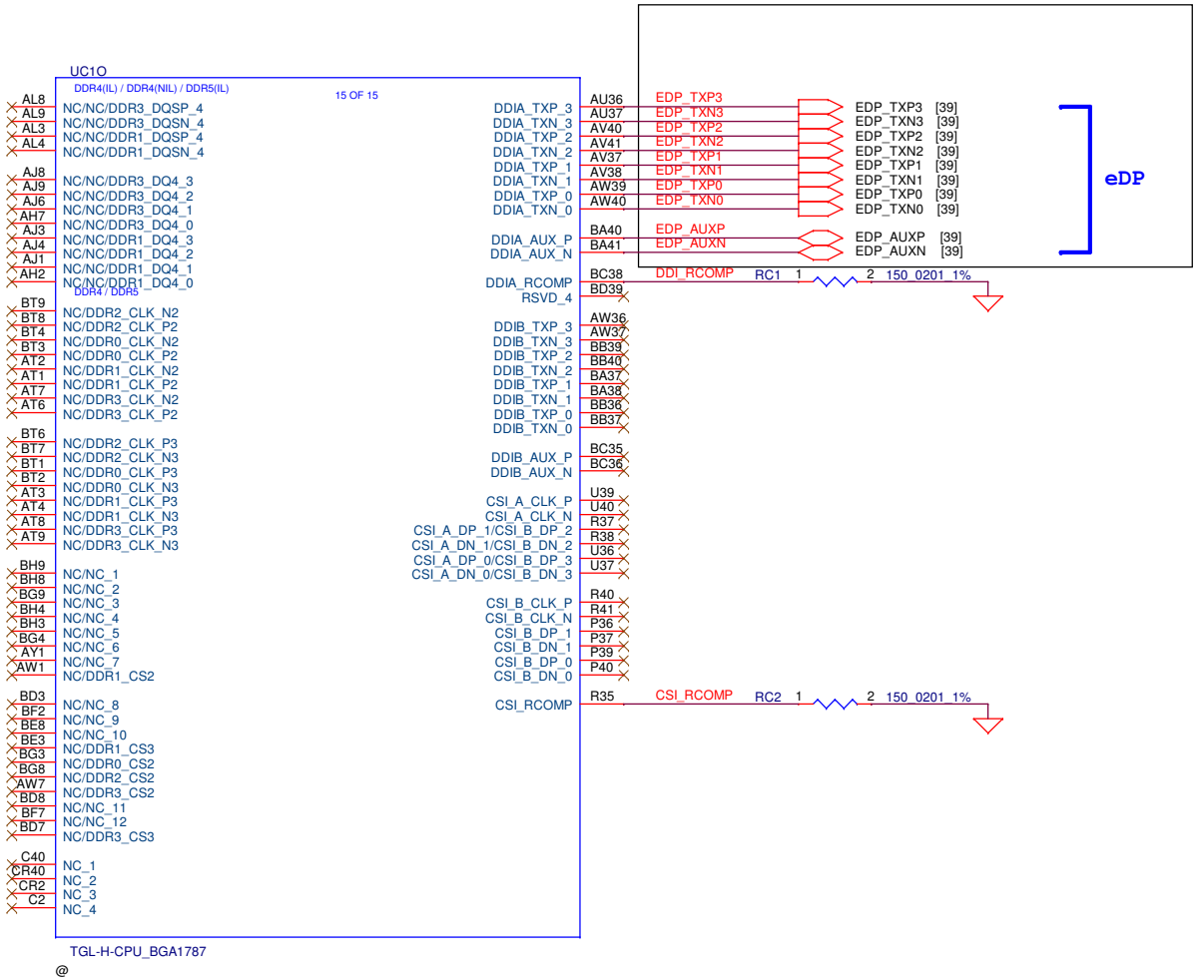
S IC FH8069004351613 QXJ1 R0 2.7G BGA S
SA0000EDJ00

UC1 CPU_I7_QS@

IC FH8069004352018 QXHY R0 2.3G BGA S
SA0000EDK00

UC1 CPU_I9_QS@

S IC FH8069004352617 QXD0 R0 2.5G BGA S
SA0000EDL00



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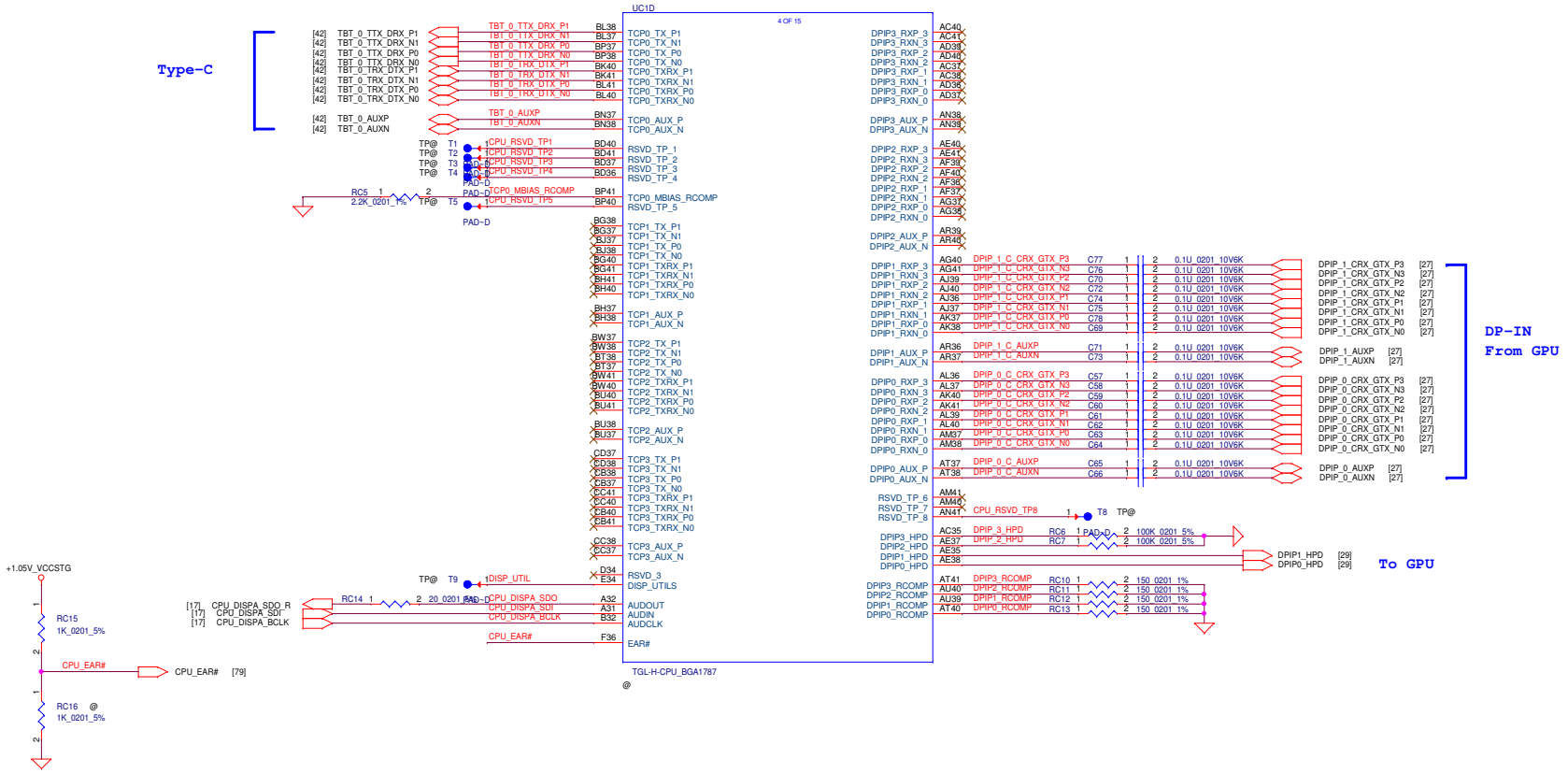
Compal Electronics, Inc.

Title: TGL-H(1/8)DDI/CSI/Memory

Size: B | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 6 of 120



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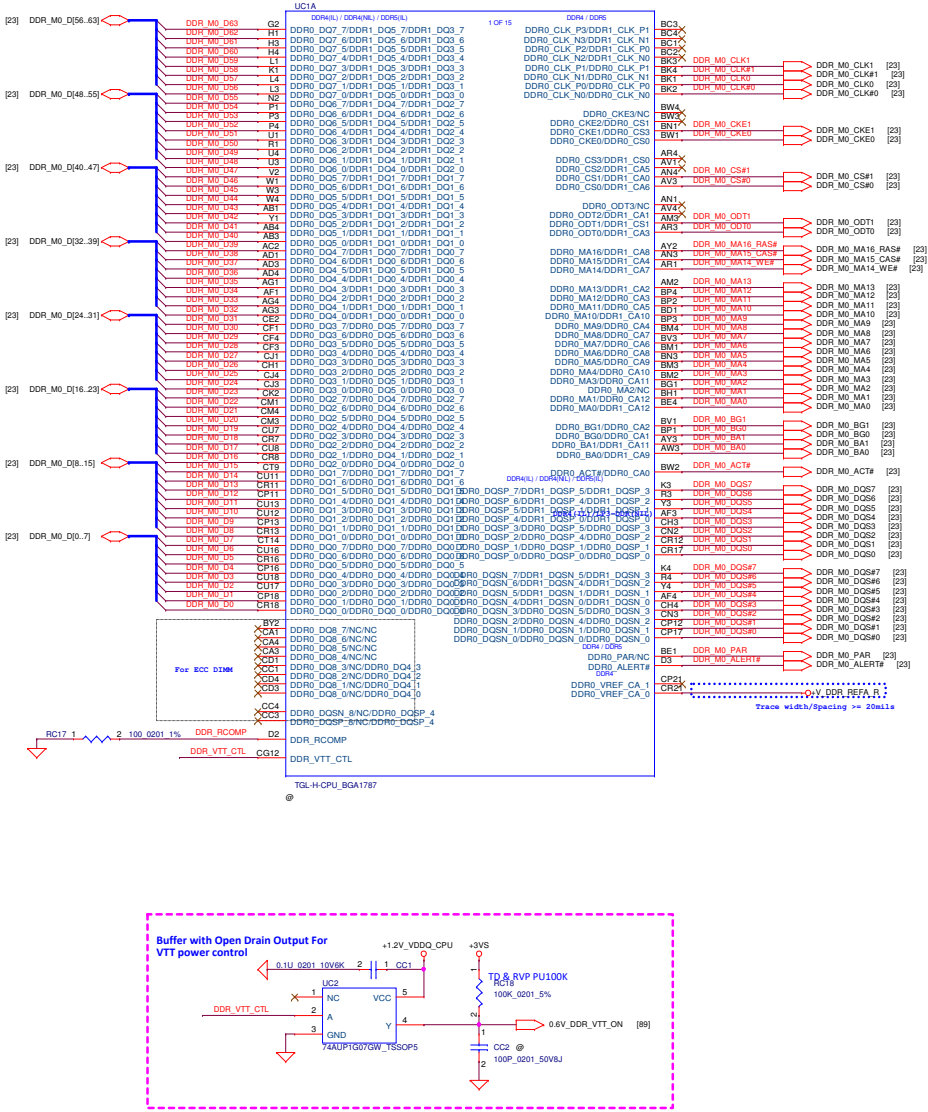
Compal Electronics, Inc.

Title: TGL-H(2/8)TCP/DPIP

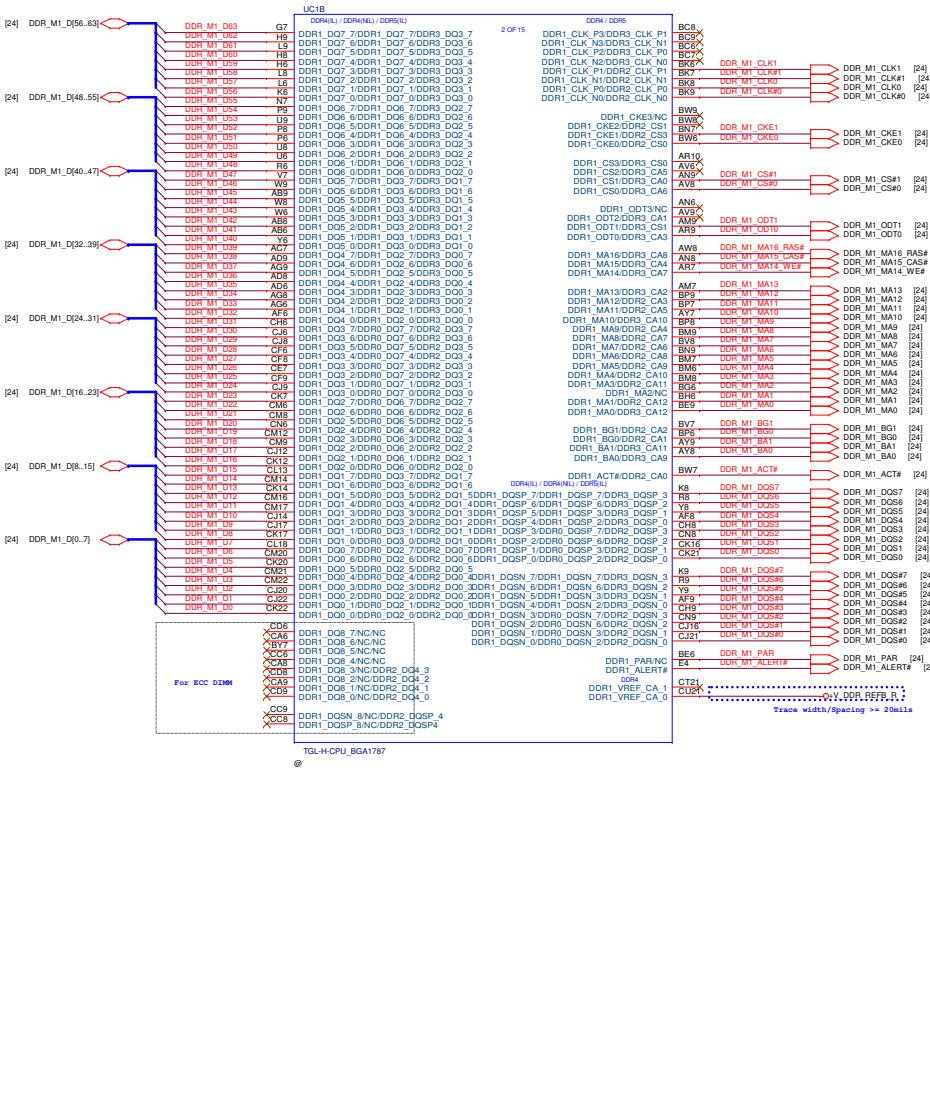
Size	Document Number	Rev
C	LA-K452P	1.0

Date: Friday, March 19, 2021 Sheet 7 of 120

CHANNEL-A
Interleaved Memory



CHANNEL-B
Interleaved Memory



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Issued Date	2020/03/05	Deciphered Date	2021/12/31

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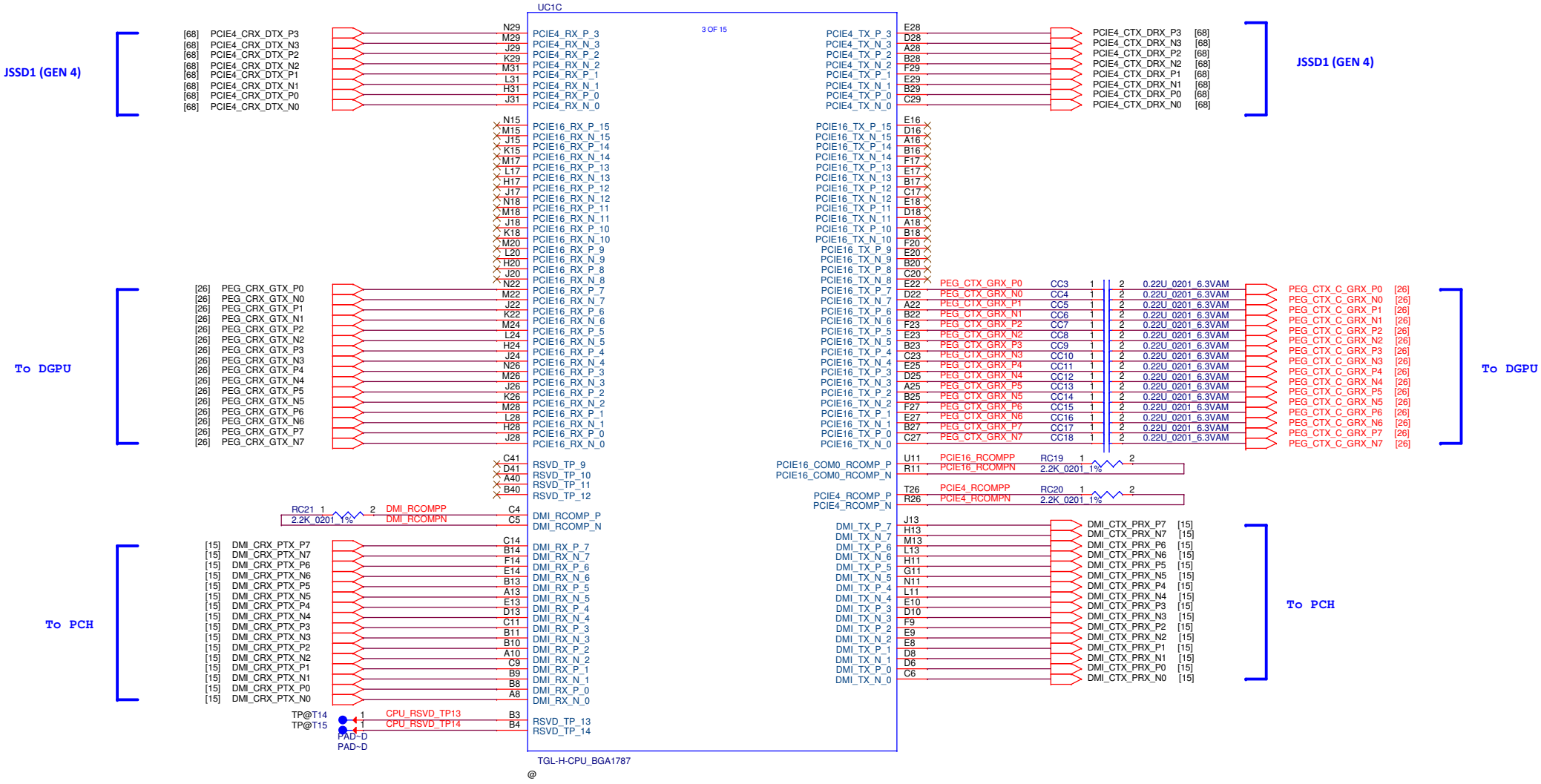
Compal Electronics, Inc.	
Title	TGL-H(3/8)DDR4-Memory
Size: Custom	Document Number: LA-K452P
Rev	1.0
Date: Friday, March 19, 2021	Sheet 8 of 120



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Compal Electronics, Inc.

Title: TGL-H(4/8)PCIE16/DMI

Size: Custom | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 9 of 120

+1.05V_VCCSTG

RC22 1 2 H_PROCHOT# 1K_0201_5%

CC182 1 2 100P_0201_50V8J @

Reserve 7/8 LA-K301PR02_0708B

+1.05V_VCCST

RC24 1 2 H_CATERR# 1K_0201_5%

RC25 1 2 H_THERMTRIP#_R 1K_0201_5%

RC27 1 @ 2 H_CPUPWRGD 1K_0201_5%

+1.05V_VCCIO_OUT

RC31 1 2 10K_0201_5% XDP_BPM#0

RC32 1 2 10K_0201_5% XDP_BPM#1

RC33 1 2 10K_0201_5% XDP_BPM#2

RC34 1 2 10K_0201_5% XDP_BPM#3

RC40 2 @ 1 H_PM_DOWN_R 1K_0201_5%

CC189 2 1 8.2P_0201_25V8D @

Place near CPU

CC185 2 1 8.2P_0201_25V8D H_PM_SYNC_R @

Place near CPU side

+3VALW_PCH

CPU_ID 10K_0201_5% 2 1 RC23

+1.05V_VCCIO_OUT

XDP_PRDY# 100_0201_1% 1 2 RC58

0919 DVT1 modify RC341 place near by CPU

UC1E

5 OF 15

[14] PCH_CPU_BCLK_P_R — PCH_CPU_BCLK_P_R C36 — BCLK_P

[14] PCH_CPU_BCLK_N_R — PCH_CPU_BCLK_N_R D36 — BCLK_N

[14] PCH_CPU_PCIBCLK_P_R — PCH_CPU_PCIBCLK_P_R C37 — PCI_BCLKN

[14] PCH_CPU_PCIBCLK_N_R — PCH_CPU_PCIBCLK_N_R B37 — PCI_BCLKP

Follow RVP

CPU_SVID_DAT D32 — VIDSOUT

CPU_SVID_CLK E32 — VIDSCK

CPU_SVID_ALERT# F32 — VIDALERT#

[58,82,85,97] H_PROCHOT# — RC26 1 2 499_0201_1% — H_PROCHOT# H35 — PROCHOT#

[14] PCH_CPU_CPURTC — RC28 1 2 0_0201_1% — PCH_CPU_CPURTC R CR22 — RTC_CLK

H_THERMTRIP#_R F34 — THERMTRIP#

[19] H_PM_SYNC_R — RC341 1 2 0_0201_1% — H_PM_SYNC_CPU CR23 — PM_SYNC

[18] H_PM_DOWN_R — RC29 1 2 20_0201_5% — H_PM_DOWN CR24 — PM_DOWN

[18] PLTRST_CPU# — PLTRST_CPU# CR25 — RESET#

[18,58] H_PECI — CP25 — PECI

[14] H_CPUPWRGD_R — RC30 1 2 0_0201_1% — H_CPUPWRGD CT25 — PROCPWRGD

H_CATERR# H36 — CATERR#

XDP_BPM#3 H39 — BPM#_3

XDP_BPM#2 H40 — BPM#_2

XDP_BPM#1 G38 — BPM#_1

XDP_BPM#0 H37 — BPM#_0

[14,79] CPU_XDP_TRST# — E40 — PROC_TRST#

[17,79] CPU_XDP_TMS — G41 — PROC_TMS

[17,79] CPU_XDP_TDO — G39 — PROC_TDO

[17,79] CPU_XDP_TDI — F39 — PROC_TDI

[17,79] CPU_XDP_TCK0 — G40 — PROC_TCK

F37 — RSVD_1

E37 — RSVD_2

RC39 1 2 150_0201_1% — TC_RCOMPP BR41 — TC_RCOMP_P

TC_RCOMPN BR40 — TC_RCOMP_N

[14] PCH_CPU_NESSC_CLK_P_R — PCH_CPU_NESSC_CLK_P_R C39 — CLK_XTAL_P

[14] PCH_CPU_NESSC_CLK_N_R — PCH_CPU_NESSC_CLK_N_R D39 — CLK_XTAL_N

TGL-H-CPU_BGA1787

@

CPU_ID CT3 — CPU_ID

CFG_15 J40 — MIPI60_CFG15# [79]

CFG_14 L41 — MIPI60_CFG14# [79]

CFG_13 J41 — MIPI60_CFG13# [79]

CFG_12 N41 — MIPI60_CFG12# [79]

CFG_11 L40 — MIPI60_CFG11# [79]

CFG_10 N40 — MIPI60_CFG10# [79]

CFG_9 M39 — MIPI60_CFG9# [79]

CFG_8 J37 — MIPI60_CFG8# [79]

CFG_7 M38 — MIPI60_CFG7# [79]

CFG_6 J38 — MIPI60_CFG6# [79]

CFG_5 J35 — MIPI60_CFG5# [79]

CFG_4 N39 — MIPI60_CFG4# [79]

CFG_3 L37 — MIPI60_CFG3# [79]

CFG_2 M35 — MIPI60_CFG2# [79]

CFG_1 M37 — MIPI60_CFG1# [79]

CFG_0 N36 — MIPI60_CFG0# [79]

CFG Signals

(For Strap & CMC)

CFG_17 M41 — MIPI60_CFG17# — TP@TH73

CFG_16 L39 — MIPI60_CFG16# — TP@TH72

PAD~D

PROC_PREQ# H34 — PAD~D XDP_PREQ# [18,79]

PROC_PRDY# G36 — XDP_PRDY# — XDP_PRDY# [18,79]

CFG_RCOMP A34 — CFG_RCOMP — RC35 1 2 49.9_0201_1%

Trace Width/Space: 12 mil/ 12 mil

Max Trace Length: 500 mil

VCCSTPWRGOOD_TCSS CP23 — VCCSTPWRGOOD_TCSS — RC36 1 2 0_0201_1% — VCCST_OVERRIDE [10,20]

VCCST_PWRGD CP24 — VCCST_PWRGD_R — RC41 1 2 60.4_0201_1% — VCCST_PWRGD [78]

SKTOCC# CR3 — SKTOCC# — RC37 1 2 0_0201_1% — SKTOCC#_R [16]

C10_WAKE CU23 — CPU_C10_WAKE — RC38 1 2 0_0201_1% — CPU_PCH_C10_WAKE [14]

PLTRST_CPU#

CH195 1 2 ESD@ 0.1U_0201_10V6K

close to CPU Side

@RF@

CC19 2 1 10P_0201_25V8 CPU_SVID_CLK

ESD@

CC20 2 1 100P_0201_50V8J VCCST_PWRGD_R

0115 : CC20 BOM Cfg change to pop /ESD request

ESD@

CC21 2 1 100P_0201_50V8J H_CPUPWRGD

ESD@

CC22 2 1 0.1U_0201_10V6K H_PROCHOT#_R

ESD@

CC23 2 1 0.1U_0201_10V6K H_THERMTRIP#_R

Place near CPU side

EC_VCCST_PG_R pull high 1K 0201 to +1.05V_VCCST on page. 78

Reserve 7/8 LA-K301PR02_0708B
9/7 DVT1 mount

+3VALW_PCH

RC44 100K_0201_5%

[17] VCCIN_AUX_VRALERT#_R — DC1 — H_PROCHOT# — RB751S-40_SOD523-2-X

+3VALW_PCH

CZ38 @ 1 2 0.1U_0201_10V6K

UZ13

[16,95] CORE_VID0

[16,95] CORE_VID1

RZ30 — AUX_CORE_VID — AUX_CORE_VID [11]

74LVC1G32GW_TSSOP5

RZ31 @ 100K_0201_5%

+1.05V_VCCST

SVID ALERT

[97] VR_SVID_ALERT# — VR_SVID_ALERT# — RC45 56_0201_1% — RC46 1 2 0_0201_1% — CPU_SVID_ALERT#

+1.05V_VCCST

SVID DATA

[97] VR_SVID_DATA — VR_SVID_DATA — RC47 100_0201_5% — RC48 1 2 0_0201_1% — CPU_SVID_DAT

+1.05V_VCCST

SVID CLK

[97] VR_SVID_CLK — VR_SVID_CLK — RC49 @ 43_0201_5% — RC50 1 2 0_0201_1% — CPU_SVID_CLK

Layout trace need to avoid PWR

+3VALW_PCH

RZ22 100K_0201_5%

3.3V_VCCST_OVRD — 3.3V_VCCST_OVRD [11]

+3VALW_PCH

RZ24 100K_0201_5%

From XDP

[79] VCCST_OVERRIDE#_R — QZ3A 2N7002KDW_SOT-363-6-X

[20] VCCST_OVERRIDE — QZ3B 2N7002KDW_SOT-363-6-X

RZ26 100K_0201_5%

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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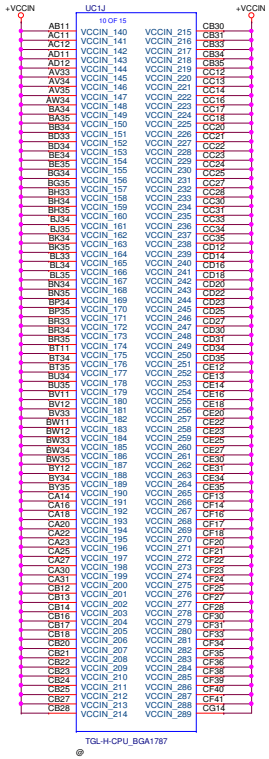
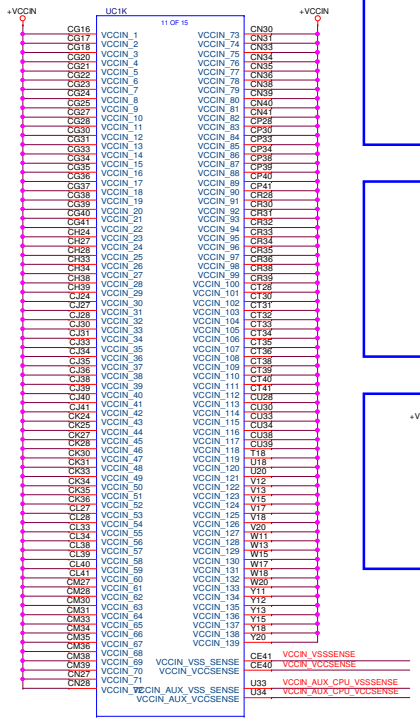
Compal Electronics, Inc.

Title: TGL-H(5/8)CFG/Sideband

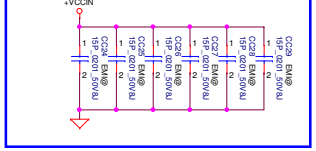
Size: Custom | Document Number: LA-K452P | Rev: 1.0

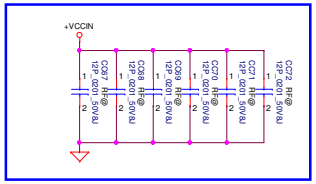
Date: Friday, March 19, 2021 | Sheet 10 of 120

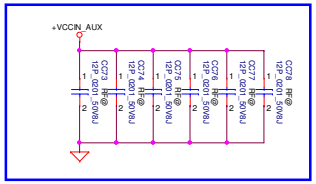


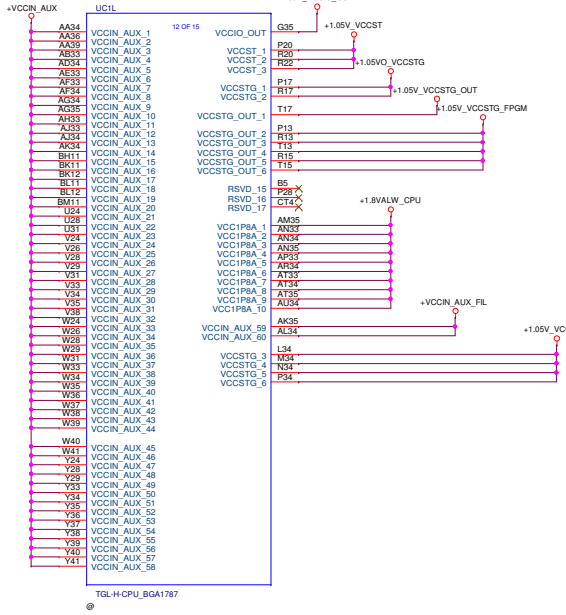


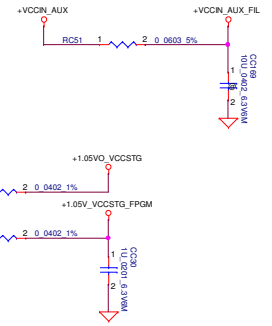
EMC CAPS-PLACE
< 5mm from SOC VCCIN





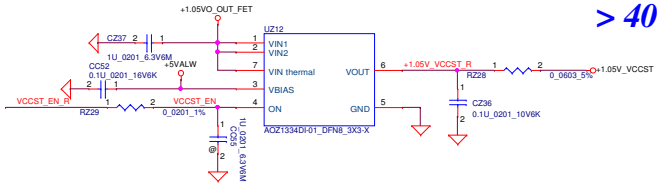


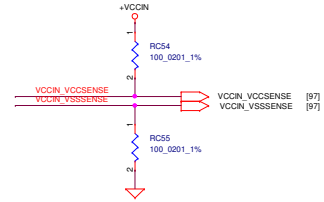




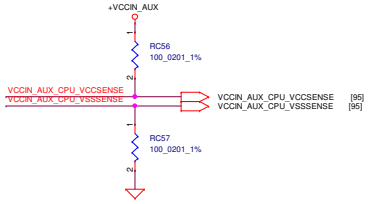
VCCST

> 40 mil



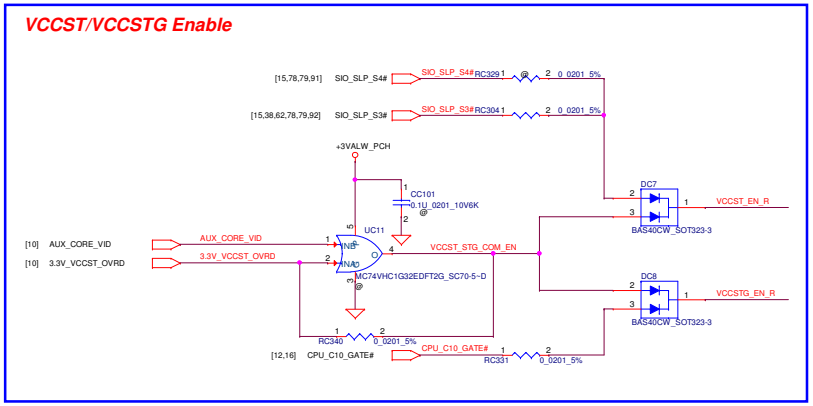


1. VCCIN_VCCSENSE/ VCCIN_VSSSENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC26, RC27 should be placed within 2 inches (50.8 mm) of CPU

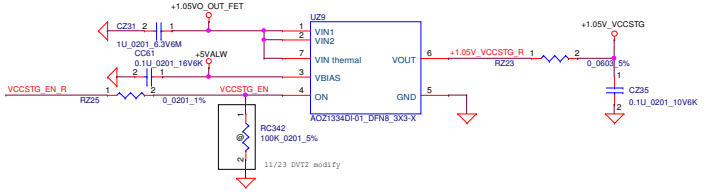


1. VCCIN_AUX_VSSSENSE / VCCIN_AUX_VCCSENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC28, RC29 should be placed within 2 inches (50.8 mm) of CPU

VCCST/VCCSTG Enable



VCCSTG



Use CPU_C10_GATE# to instead of SIO_SLP_S3#
For S0ix power saving

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Issued Date	2020/03/05	Deciphered Date	2021/12/31

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Compal Electronics, Inc.	
Title	TGL-H(6/8)VCCIN/VCCIN AUX
Size: Custom	Document Number: LA-K452P
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Date: Friday, March 19, 2021	Sheet 11 of 120

UC1N

14 OF 15

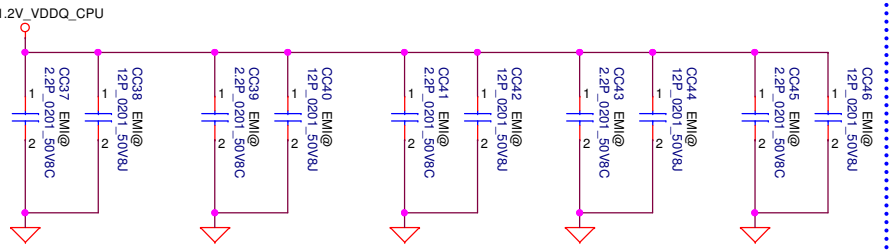
+1.2V_VDDQ_CPU

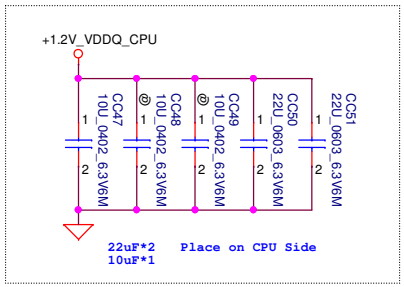
L15	VSS_572	VDD2_1	AH11
L18	VSS_573	VDD2_2	AH12
L2	VSS_574	VDD2_3	AJ11
L22	VSS_575	VDD2_4	AJ12
L26	VSS_576	VDD2_5	AL11
L29	VSS_577	VDD2_6	AM11
L33	VSS_578	VDD2_7	AM12
L35	VSS_579	VDD2_8	AN11
L36	VSS_580	VDD2_9	AN12
L38	VSS_581	VDD2_10	AR11
L5	VSS_582	VDD2_11	AR5
L7	VSS_583	VDD2_12	AT11
M33	VSS_584	VDD2_13	AT12
M36	VSS_585	VDD2_14	AT5
M40	VSS_586	VDD2_15	AV10
N1	VSS_587	VDD2_16	AV11
N10	VSS_588	VDD2_17	AW10
N13	VSS_589	VDD2_18	AW11
N17	VSS_590	VDD2_19	AW12
N20	VSS_591	VDD2_20	AW5
N24	VSS_592	VDD2_21	AY11
N28	VSS_593	VDD2_22	AY5
N3	VSS_594	VDD2_23	BA11
N31	VSS_595	VDD2_24	BC10
N33	VSS_596	VDD2_25	BC11
N35	VSS_597	VDD2_26	BC12
N37	VSS_598	VDD2_27	BD10
N38	VSS_599	VDD2_28	BD11
N4	VSS_600	VDD2_29	BD5
N5	VSS_601	VDD2_30	BE11
N6	VSS_602	VDD2_31	BE5
N8	VSS_603	VDD2_32	BF11
N9	VSS_604	VDD2_33	BF12
P10	VSS_605	VDD2_34	BG10
P11	VSS_606	VDD2_35	BG11
P15	VSS_607	VDD2_36	BH10
P18	VSS_608	VDD2_37	BH5
P2	VSS_609	VDD2_38	BK5
P22	VSS_610	VDD2_39	BM10
P26	VSS_611	VDD2_40	BN10
P29	VSS_612	VDD2_41	BN5
P33	VSS_613	VDD2_42	BP5
P35	VSS_614	VDD2_43	BT10
P38	VSS_615	VDD2_44	BV10
P41	VSS_616	VDD2_45	BV5
P5	VSS_617	VDD2_46	BW5
P7	VSS_618		
R10	VSS_619	VSS_652	V37
R18	VSS_620	VSS_653	V39
R2	VSS_621	VSS_654	V4
R33	VSS_622	VSS_655	V40
R34	VSS_623	VSS_656	V41
R36	VSS_624	VSS_657	V5
R39	VSS_625	VSS_658	V6
R5	VSS_626	VSS_659	V8
R7	VSS_627	VSS_660	V9
T20	VSS_628	VSS_661	W10
T22	VSS_629	VSS_662	W2
T24	VSS_630	VSS_663	W22
T28	VSS_631	VSS_664	W5
T31	VSS_632	VSS_665	W7
U10	VSS_633	VSS_666	Y10
U13	VSS_634	VSS_667	Y17
U15	VSS_635	VSS_668	Y2
U17	VSS_636	VSS_669	Y22
U2	VSS_637	VSS_670	Y26
U22	VSS_638	VSS_671	Y31
U26	VSS_639	VSS_672	Y5
U29	VSS_640	VSS_673	Y7
U35	VSS_641		
U38	VSS_642		
U41	VSS_643		
U5	VSS_644		
U7	VSS_645		
V1	VSS_646		
V10	VSS_647		
V11	VSS_648		
V22	VSS_649		
V3	VSS_650		
V36	VSS_651		

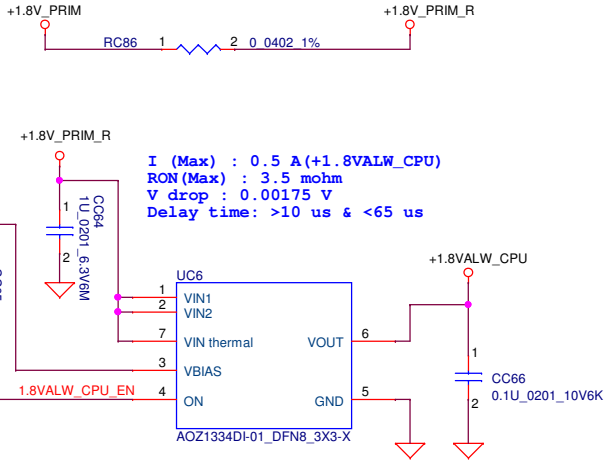
TGL-H-CPU_BGA1787

@

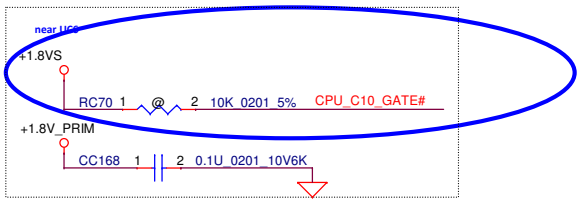
EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)







Follow TD team
0706



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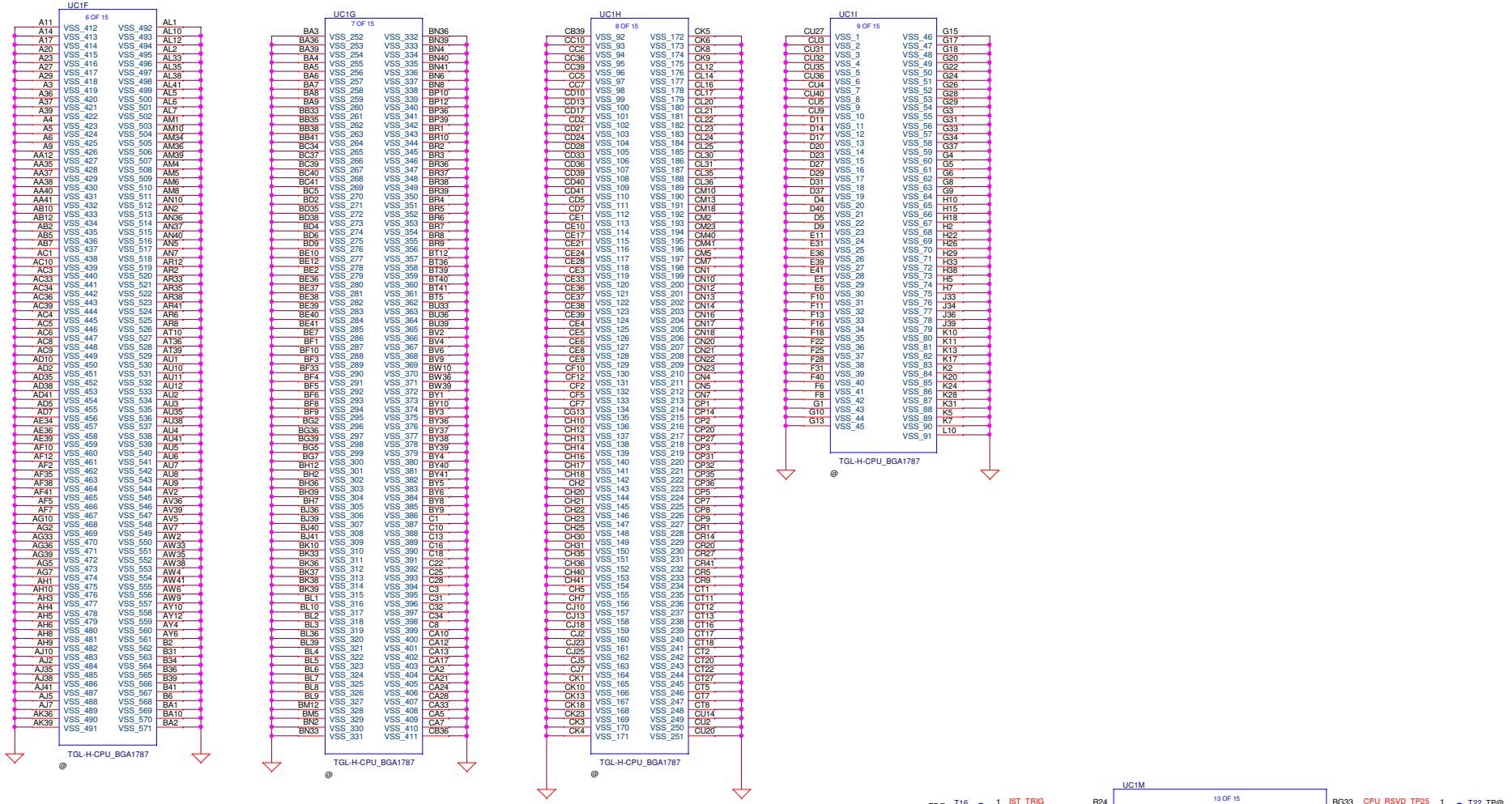
Compal Electronics, Inc.

Title: TGL-H(7/8)Power VDDQ

Size: B | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 12 of 120



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Title	Compal Electronics, Inc.		
	CFL-H(8/8)GND/RSVD		
Size: Custom	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 13 of 120		

10/8 DVT1 modify Please careful with the placement as close as possible to the RH3, RH4

10/19 DVT1 update

PCH DVT1:

UH1 PCH@

TIGER LAKE PCH
SA0000D3F2L

UH1 PCH_ES2@

S IC A31 FHSSKU_MBL QVTB A0 FCBGA ES2 S
SA0000D3F3L

01/22 DVT2 update

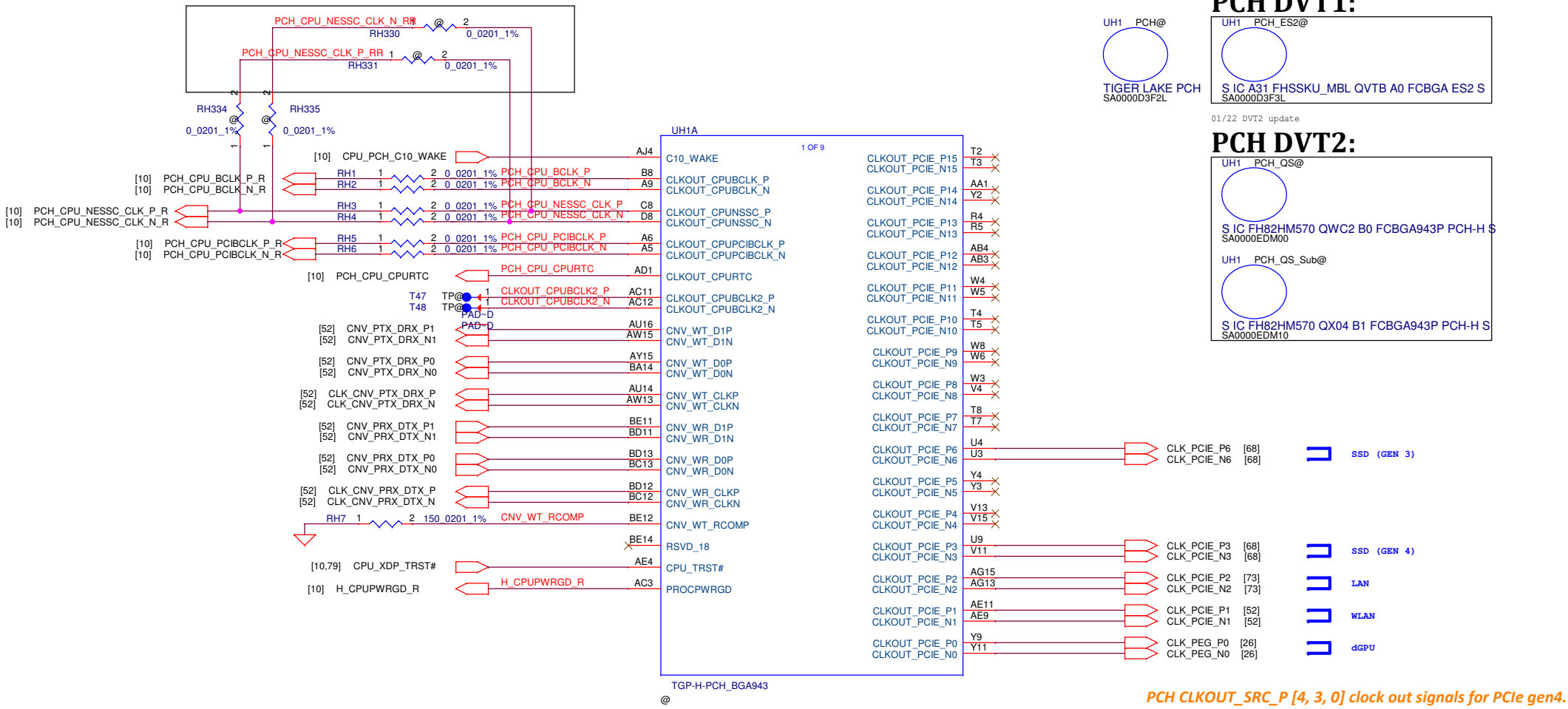
PCH DVT2:

UH1 PCH_QS@

S IC FH82HM570 QWC2 B0 FCBGA943P PCH-H S
SA0000EDM00

UH1 PCH_QS_Sub@

S IC FH82HM570 QX04 B1 FCBGA943P PCH-H S
SA0000EDM10



PCH CLKOUT_SRC_P [4, 3, 0] clock out signals for PCIe gen4.

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Issued Date	2020/03/05	Deciphered Date	2021/12/31

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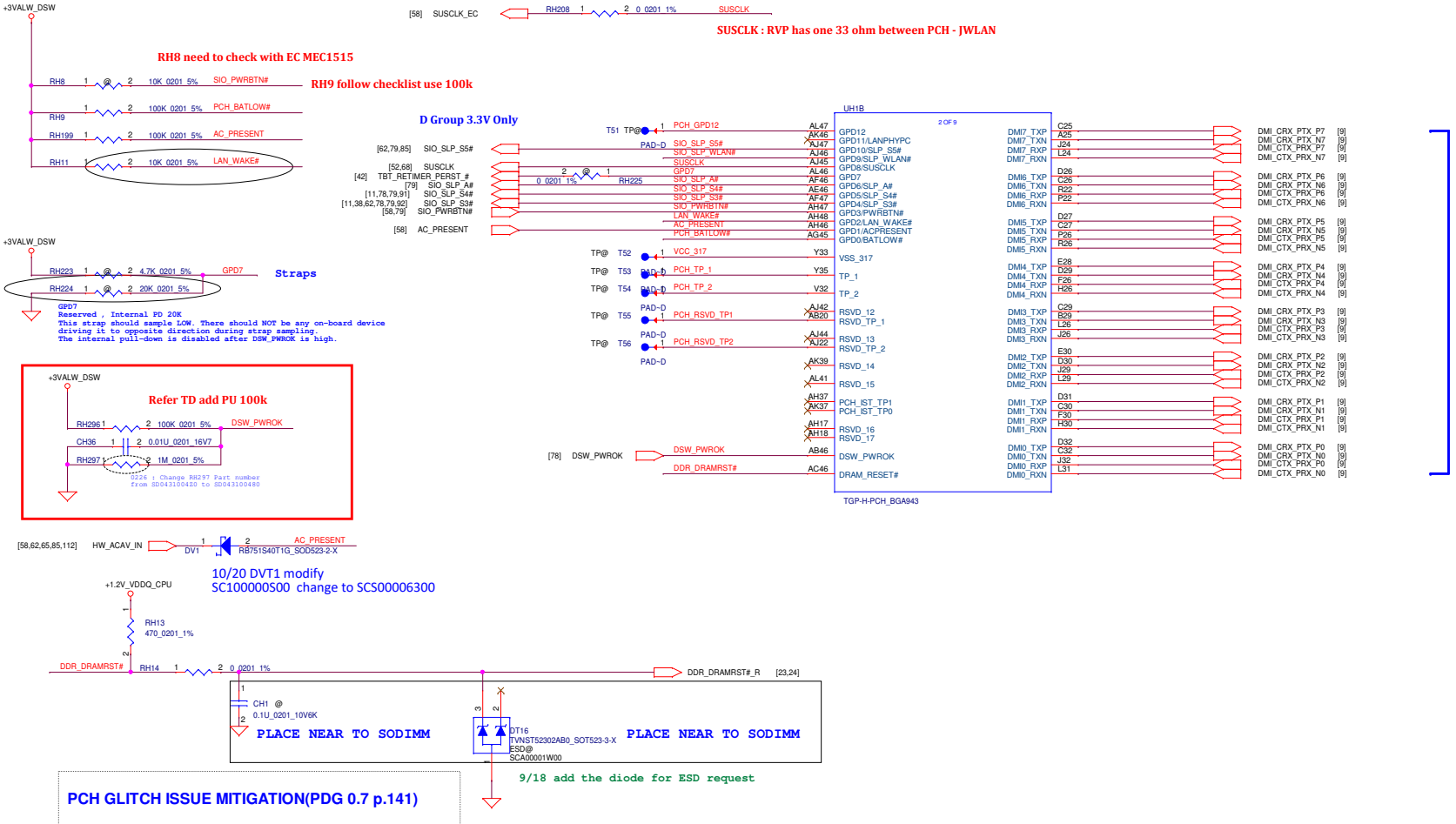
Compal Electronics, Inc.

Title: PCH(1/8)Clock/CNVi

Size: B | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 14 of 120



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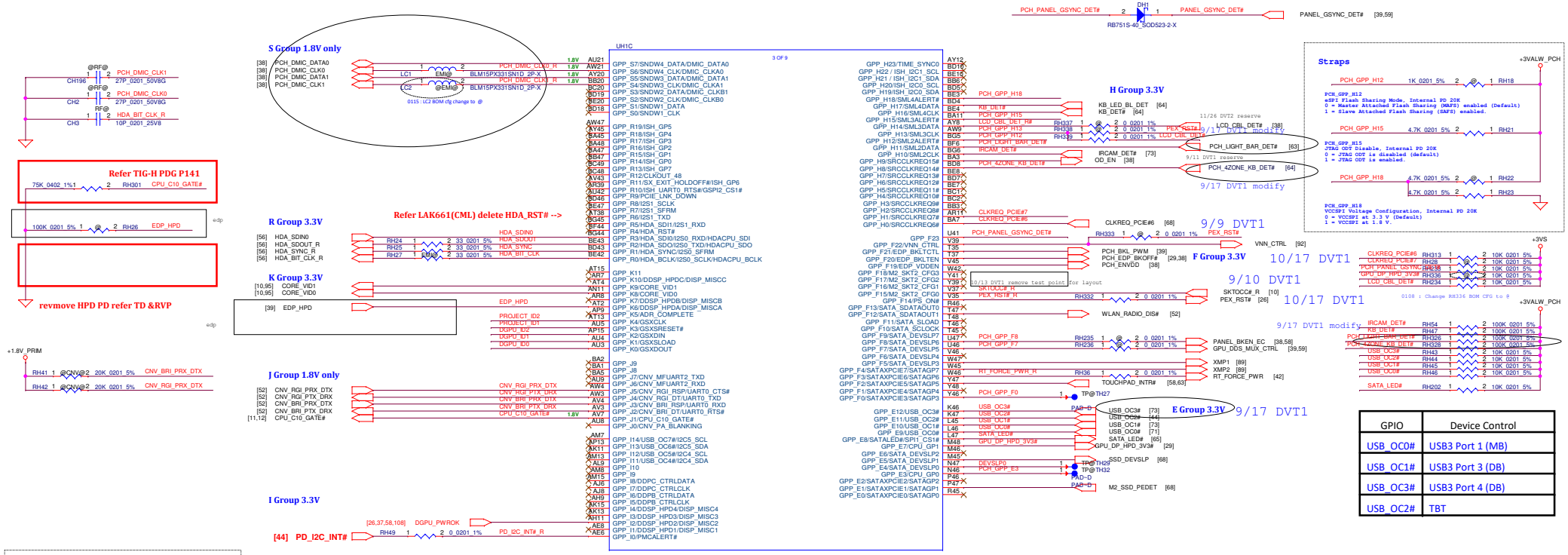
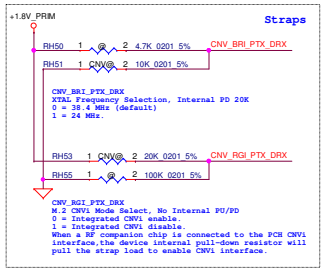
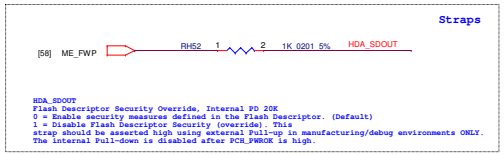
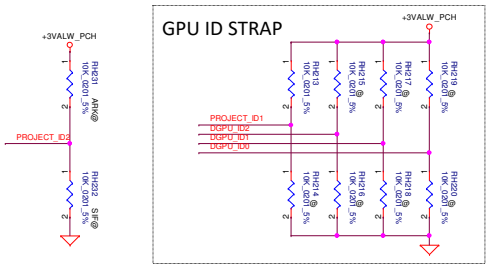
Compal Electronics, Inc.			
Title: PCH(2/8)DMI			
Size: C	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 15 of 120		







0918 DVT1 Modify
Remove ISH_I2C0_SCL & ISH_I2C0_SDA level shift & 1K pull up



GPIO	Device Control
USB_OC0#	USB3 Port 1 (MB)
USB_OC1#	USB3 Port 3 (DB)
USB_OC3#	USB3 Port 4 (DB)
USB_OC2#	TBT

	DGPU_ID2 (AP15)	DGPU_ID1 (AU4)	DGPU_ID0 (AU3)
GN20-E3 MP	L	L	X
GN20-E4 MP	L	H	X
GN20-E5 MP	H	L	X
GN20-E7 MP	H	H	X

	PROJECT_ID2 (AT13)	PROJECT_ID1 (AU5)
SIF	L	H
ARK	H	H

The high level features of GPIO:

- Per-group voltage configurable (3.3 V or 1.8 V) on certain GPIO groups: GPP_B, GPP_C, GPP_D, GPP_E, GPP_F, GPP_H, GPP_I, GPP_K, and GPP_R
- Per-pad voltage configuration (3.3 V of 1.8 V) on certain GPIO groups: GPP_A and GPP_G
- Fixed voltage on certain GPIO groups: GPD (3.3 V), GPP_J and GPP_S (1.8 V)
- Configurable as an input or output signal.
- Configurable GPIO pad ownership by host, ME, or ISH.
- SCI (GPE) and IOAPIC interrupt capable on all GPIOs
- NMI and SMI capability capable (on selected GPIOs).
- PWM, Serial Blink capable (on selected GPIOs).
- Programmable hardware debouncer (on GPD3/PWRBTN# pin)

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Issued Date	2020/03/05	Deciphered Date	2021/12/31

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Compal Electronics, Inc.

Title: PCH(3/8)GPIO

Size: Custom | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 16 of 120

0914 DVT1 Modify

+1.8V_PRIM

PCH_SML1CLK → QH8B LBSS139DW1T1G_SOT363-6 → PD_I2C_SCL [44]

PCH_SML1DATA → QH8A LBSS139DW1T1G_SOT363-6 → PD_I2C_SDA [44]

To PD

0914 DVT1 Modify

+1.8V_PRIM

PCH_SML0CLK → QH7B LBSS139DW1T1G_SOT363-6 → TCP_SML0CLK [42]

PCH_SML0DATA → QH7A LBSS139DW1T1G_SOT363-6 → TCP_SML0DATA [42]

To BB

+3VS

RH65 UART_2_PCTS_DRTS
RH66 UART_2_PRTS_DCTS
RH68 UART_2_PTXD_DRXD
RH70 UART_2_PRXD_DTXD
RH212 CNV_RF_RESET#
RH221 CLKREQ_CNV#

And an optional Clock request for the 38.4M clock (CNVi reference clock, requires a pecific SKU, used by jfp not supported/used by HrP) have PD in the CRF

Need to check keypart

+1.8V_PRIM

RH92 PCH_SML0CLK
RH93 PCH_SML0DATA
RH94 PCH_SML1CLK
RH95 PCH_SML1DATA

+3VALW_PCH

RH90 PCH_SMBDATA
RH91 PCH_SMBCLK
RH96 SIO_SLP_S0#
RH48 SPK_ID1
RH316 SPK_ID2

+3VS

RH100 CLKREQ_PEG#0
RH314 CLKREQ_PCIE#1
RH101 CLKREQ_PCIE#2
RH102 CLKREQ_PCIE#3
RH104 DGPU_PWR_EN

RH315 DGPU_PWR_EN

0908 DVT1

0918 DVT1 Modify

D Group 1.8/3.3V
+1.8V_VCCPGPPD

[29] GC6_FB_EN_MCP

C Group 1.8/3.3V
+3V_VCCPGPPBC

[52] CLKREQ_CNV#
[52] CNV_RF_RESET#
PCH_SML1DATA
PCH_SML0DATA
PCH_SML0CLK

[79] UART_2_PTXD_DRXD
[79] UART_2_PRXD_DTXD
[63] I2C_1_SCL
[63] I2C_1_SDA

UART_2_PCTS_DRTS
UART_2_PRTS_DCTS
UART_2_PTXD_DRXD
UART_2_PRXD_DTXD

CML "HDMI_HPD_PCH"connect to GPP_C14

[40] HDMI_HPD_PCH

TH63 TH64 TH65 TH67 PAD-D

PCH_GPP_C11
PCH_GPP_C10
PCH_GPP_C9
PCH_GPP_C8

[56] SPK_ID2

PCH_SML0ALERT#

To MEM

B Group 1.8/3.3V
+3V_VCCPGPPBC

[37] DGPU_PWR_EN
[62] ELC_BOOT_MODE
[62] ELC_RESET
[56,58] HDA_SPKR
[26] PCH_PLTRST#
[79] SIO_SLP_S0#

PCH_GPP_B18
DGPU_PWR_EN
HDA_SPKR
PCH_PLTRST#
SIO_SLP_S0#

[68] CLKREQ_PCIE#3
[73] CLKREQ_PCIE#2
[52] CLKREQ_PCIE#1
[26] CLKREQ_PEG#0

CLKREQ_PCIE#3
CLKREQ_PCIE#2
CLKREQ_PCIE#1
CLKREQ_PEG#0

[52] BT_RADIO_DIS#
[10] VCCIN_AUX_VRALERT#_R
RH111 0_0201_1%
VCCIN_AUX_VRALERT#

UH1D

4 OF 9

GPP_D23/UART3_CTS#/THC1_SPI2_INT#
GPP_D22/UART3_RTS#/THC1_SPI2_RST#
GPP_D21/UART3_TXD/THC1_SPI2_IO3
GPP_D20/UART3_RXD/THC1_SPI2_IO2
GPP_D19/GSPI3_MOSI/THC1_SPI2_IO1
GPP_D18/GSPI3_MISO/THC1_SPI2_IO0
GPP_D17/GSPI3_CLK/THC1_SPI2_CLK
GPP_D16/GSPI3_CS0#/THC1_SPI2_CS#
GPP_D15/SML1DATA
GPP_D14 / THC0_SPI1_IO3
GPP_D13 / THC0_SPI1_IO2
GPP_D12/ISH_UART0_CTS#
GPP_D11
GPP_D10/SML0DATA
GPP_D9/SML0CLK
GPP_D8/ISH2_SCLK/THC0_SPI1_INT#
GPP_D7/ISH2_RXD/THC0_SPI1_RST#
GPP_D6/ISH2_TXD/MODEM_CLKREQ
GPP_D5/ISH2_SFRM/CNV_RF_RESET#
GPP_D4/SML1CLK
GPP_D3 / THC0_SPI1_IO0 / SBK 3 / BK3
GPP_D2 / THC0_SPI1_IO1 / SBK2 / BK2
GPP_D1 / THC0_SPI1_CLK / SBK1 / BK1
GPP_D0 / THC0_SPI1_CS# / SBK0 / BK0
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C7/ISH_I2C2_SCL/I2C3_SCL
GPP_C6/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4
GPP_C5/SML0ALERT#
GPP_C4/ISH_UART0_TXD/I2C2_SCL
GPP_C3/ISH_UART0_RXD/I2C2_SDA
GPP_C2/SML1ALERT#
GPP_C1/SMBDATA
GPP_C0/SMBCLK
GPP_B23/SML1ALERT#/PCHHOT#
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS0#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS0#
GPP_B14/SPKR
GPP_B13/PLTRST#
GPP_B12/SLP_S0#
GPP_B11/I2S_MCLK
GPP_B10/SRCCLKREQ5#
GPP_B9/SRCCLKREQ4#
GPP_B8/SRCCLKREQ3#
GPP_B7/SRCCLKREQ2#
GPP_B6/SRCCLKREQ1#
GPP_B5/SRCCLKREQ0#
GPP_B4 / CPU_GP3
GPP_B3/CPU_GP2
GPP_B2/VRALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B0 / GSPI0_CS1# / IMGCLKOUT1

TGP-H-PCH_BGA943

GPP_A14 / IMGCLKOUT0 PCH_GPP_A14
GPP_A13/ESPI_ALERT3# PCH_GPP_A13
GPP_A12/ESPI_ALERT2#
GPP_A11/ESPI_ALERT1#
GPP_A10/ESPI_ALERT0# PCH_GPP_A9
GPP_A9/ESPI_CS3# PCH_GPP_A8
GPP_A8/ESPI_CS2#
GPP_A7/ESPI_CS1# ESPI_RESET#
GPP_A6/ESPI_RESET# ESPI_CLK_R RH76 33_0201_5%
GPP_A5/ESPI_CLK ESPI_CS#
GPP_A4/ESPI_CS0# ESPI_IO3_R RH79 33_0201_5%
GPP_A3/ESPI_IO3/SUSACK# ESPI_IO2_R RH81 33_0201_5%
GPP_A2/ESPI_IO2/SUSWARN#/SUSPWRDNACK ESPI_IO1_R RH83 33_0201_5%
GPP_A1/ESPI_IO1 ESPI_IO0_R RH86 33_0201_5%
GPP_A0/ESPI_IO0

ESPI_RESET# [58]
ESPI_CLK [58]
ESPI_CS# [58]
ESPI_IO3 [58]
ESPI_IO2 [58]
ESPI_IO1 [58]
ESPI_IO0 [58]

A Group 1.8/3.3V
+1.8V_VCCPGPPA

10/20 DVT1 update.

ESPI_RESET# RC66 75K_0201_5%

GPP_G15/DDP2_CTRLDATA/TBT_LSX1_RXD
GPP_G14/DDP2_CTRLCLK/TBT_LSX1_TXD
GPP_G13/DDP1_CTRLDATA/TBT_LSX0_RXD
GPP_G12/DDP1_CTRLCLK/TBT_LSX0_TXD
GPP_G11/ISH_SPI_MOSI/DDP4_CTRLDATA/GSPI2_MOSI/TBT_LSX3_RXD
GPP_G10/ISH_SPI_MISO/DDP4_CTRLCLK/GSPI2_MISO/TBT_LSX3_TXD
GPP_G9/ISH_SPI_CLK/DDP3_CTRLDATA/GSPI2_CLK/TBT_LSX2_RXD
GPP_G8/ISH_SPI_CS#/DDP3_CTRLCLK/GSPI2_CS0#/TBT_LSX2_TXD

TBT_1_LSX_RX
TBT_0_LSX_RX R RH299 0_0201_1%
TBT_0_LSX_TX R RH300 0_0201_1%
TBT_1_LSX_TX
TBT_2_LSX_RX
TBT_2_LSX_TX

TBT_0_LSX_RX [42]
TBT_0_LSX_TX [42]

G Group Per-pad 1.8/3.3V
VCCPRIM_3P3 or VCCPRIM_1P8

GPP_G7 STRAP3 PCH [30]
GPP_G6 STRAP5_PCH [30]
GPP_G5/SLP_DRAM# PCH_GPP_G3
GPP_G4
GPP_G3
GPP_G2/DNX_FORCE_RELOAD
GPP_G1/DDPA_CTRLDATA
GPP_G0/DDPA_CTRLCLK

Jason0720 Note-Viper-MLK
STRAP_PCH
Connect to Page-030 GPU STRAP

GPP_RCOMP RH97 200_0201_1%
PCIE_RCOMPP
PCIE_RCOMPN
CL_RST#
CL_DATA
CL_CLK

PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
DBG_PMODE
INTRUDER#
HDACPU_SDO
HDACPU_BCLK

CPU_XDP_TCK0 [10,79]
CPU_XDP_TMS [10,79]
CPU_XDP_TDO [10,79]
CPU_XDP_TDI [10,79]
PCH_JTAG_TCK1 [79]
XDP_ITP_PMODE [79]
SM_INTRUDER#
CPU_DISPA_SDI RH107 30_0201_5%
CPU_DISPA_SDO_R RH108 30_0201_5%

CPU_DISPA_SDI [7]
CPU_DISPA_SDO_R [7]
CPU_DISPA_BCLK [7]

+3VL_RTC

SM_INTRUDER# RH112 1M_0201_5%
CH7 0.1U_0201_10V6K

INTRUDER# should have a weak external pull-up to VccRTC. (PDG)

Straps

RH120 PCH_SMBALERT#

PCH_SMBALERT#
TLS Confidentiality, Internal PD 20K
0 = Disable Intel CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS

RH121 PCH_SML0ALERT#
RH122 20K_0201_5%

PCH_SML0ALERT#
eSPI Disable, Internal PD 20K
0 = Enable eSPI. (Default)
1 = Disable eSPI.

RH123 PCH_SML1ALERT#

PCH_SML1ALERT#
CPUMISC Clock Frequency, Internal PD 20K
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)

Straps

RH116 HDA_SPKR

HDA_SPKR
Top Swap Override , Internal PD 20K
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

RH117 PCH_GPP_B18

PCH_GPP_B18
No Reboot, Internal PD 20K
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

RH118 PCH_GPP_B22
RH119 20K_0201_5%

PCH_GPP_B22
Boot BIOS Strap (BBS), Internal PD 20K
0 = BIOS fetches are routed to SPI (NAF) or the eSPI Flash Channel (SAF)
1 = BIOS fetches are routed to the eSPI Peripheral Channel

Straps

TBT_0_LSX_RX
The Pin VCC Configuration , Internal PD 20K
0 = Pin at 1.8V
1 = Pin at 3.3V

TBT_1_LSX_RX
The Pin VCC Configuration , Internal PD 20K
0 = Pin at 1.8V
1 = Pin at 3.3V

TBT_2_LSX_RX
The Pin VCC Configuration , Internal PD 20K
0 = Pin at 1.8V
1 = Pin at 3.3V

TBT_3_LSX_RX
The Pin VCC Configuration , Internal PD 20K
0 = Pin at 1.8V
1 = Pin at 3.3V

TBT_0_LSX_RX_R
TBT_1_LSX_RX
TBT_2_LSX_RX
TBT_3_LSX_RX

+3VS

PCH_PLTRST# → ESD@ CC83 0.1U_0201_10V6K → U23 MC74VHC1G08DFT2G_SC70-5-X → PLTRST# [42,52,68,73,79]

RC75 100K_0201_5%
RC76 100K_0201_5%

10/20 DVT1 modify
SA00000OH00 change to SA0000BIP00

9/14 DVT1 add level shift to avoid leakage

+3VS

RH321 MEM_SMBCLK
RH320 MEM_SMBDATA

PCH_SMBCLK → QH9A 2N7002KDW_SOT-363-6-X → MEM_SMBCLK → MEM_SMBCLK [23,24]

PCH_SMBDATA → QH9B 2N7002KDW_SOT-363-6-X → MEM_SMBDATA → MEM_SMBDATA [23,24]

To DDR, XDP

MEM_SMBCLK → ESD@ CC198 15P_0201_50V8J
MEM_SMBDATA → ESD@ CC199 15P_0201_50V8J

01.12 : ESD Request.
0115 : CC198 CC199 BOM cfg change to pop /ESD request

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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Compal Electronics, Inc.

Title: PCH(4/8)UART/SMB/JTAG/eSPI

Size: Custom | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 17 of 120

CC187 2 1 8.2P_0201_25V8D H_PM_SYNC_R

Place near by PCH

RH124 2 @ 1 1K_0201_5% PLTRST_CPU#

9/8 DVT1 Modify

0919 DVT1 modify RH329 place near by PCH

CC188 2 1 8.2P_0201_25V8D H_PM_DOWN_R

Place near by PCH

9/8 DVT1 Modify

UH1E

5 OF 9

[10,79] XDP_PRDY# → AF3 PRDY#

[10,79] XDP_PREQ# → AF4 PREQ#

[10] H_PM_SYNC_R — RH126 30_0201_5% — H_PM_SYNC → AH4 PM_SYNC

[10] H_PM_DOWN_R — RH329 0_0201_1% — H_PM_DOWN_PCH → AH2 PM_DOWN

[10] PLTRST_CPU# → AE3 PLTRST_CPU#

[10,58] H_PECI — RH127 13_0201_5% — PCH_PECI → AH3 PECI

V29 RSVD_10

V28 RSVD_11

H45 PCIE24_TXP
G45 PCIE24_TXN
T42 PCIE24_RXP
T43 PCIE24_RXN

J46 PCIE23_TXP
J47 PCIE23_TXN
P35 PCIE23_RXP
P37 PCIE23_RXN

G47 PCIE22_TXP
F47 PCIE22_TXN
R39 PCIE22_RXP
P41 PCIE22_RXN

E48 PCIE21_TXP
E49 PCIE21_TXN
N43 PCIE21_RXP
N42 PCIE21_RXN

B44 PCIE20_TXP/SATA7_TXP
A44 PCIE20_TXN/SATA7_TXN
M37 PCIE20_RXP/SATA7_RXP
M35 PCIE20_RXN/SATA7_RXN

D43 PCIE19_TXP/SATA6_TXP
C43 PCIE19_TXN/SATA6_TXN
L41 PCIE19_RXP/SATA6_RXP
N39 PCIE19_RXN/SATA6_RXN

C42 PCIE18_TXP/SATA5_TXP
B42 PCIE18_TXN/SATA5_TXN
L42 PCIE18_RXP/SATA5_RXP
K43 PCIE18_RXN/SATA5_RXN

E41 PCIE17_TXP/SATA4_TXP
D42 PCIE17_TXN/SATA4_TXN
G43 PCIE17_RXP/SATA4_RXP
F44 PCIE17_RXN/SATA4_RXN

C40 PCIE16_TXP/SATA3_TXP
D40 PCIE16_TXN/SATA3_TXN
C47 PCIE16_RXP/SATA3_RXP
D46 PCIE16_RXN/SATA3_RXN

WLAN (GEN 2)

[52] PCIE_PTX_DRX_P15 → D39 PCIE15_TXP/SATA 2_TXP
[52] PCIE_PTX_DRX_N15 → C39 PCIE15_TXN/SATA2_TXN
[52] PCIE_PRX_DTX_P15 → C46 PCIE15_RXP/SATA2_RXP
[52] PCIE_PRX_DTX_N15 → D45 PCIE15_RXN/SATA2_RXN

LAN (Gen2)

[73] PCIE_PTX_DRX_P14 → E38 PCIE14_TXP/SATA1B_TXP
[73] PCIE_PTX_DRX_N14 → D38 PCIE14_TXN/SATA1B_TXN
[73] PCIE_PRX_DTX_P14 → H42 PCIE14_RXP/SATA1B_RXP
[73] PCIE_PRX_DTX_N14 → J41 PCIE14_RXN/SATA1B_RXN

B37 PCIE13_TXP/SATA0B_TXP
C38 PCIE13_TXN/SATA0B_TXN
C39 PCIE13_RXP/SATA0B_RXP
H38 PCIE13_RXN/SATA0B_RXN

TGP-H-PCH_BGA943

PCIE12_TXP/SATA1A_TXP C36 → PCIE_PTX_DRX_P12 [68]
PCIE12_TXN/SATA1A_TXN D36 → PCIE_PTX_DRX_N12 [68]
PCIE12_RXP/SATA1A_RXP L36 → PCIE_PRX_DTX_P12 [68]
PCIE12_RXN/SATA1A_RXN J37 → PCIE_PRX_DTX_N12 [68]

PCIE11_TXP/SATA0A_TXP D35 → PCIE_PTX_DRX_P11 [68]
PCIE11_TXN/SATA0A_TXN C35 → PCIE_PTX_DRX_N11 [68]
PCIE11_RXP/SATA0A_RXP C36 → PCIE_PRX_DTX_P11 [68]
PCIE11_RXN/SATA0A_RXN H35 → PCIE_PRX_DTX_N11 [68]

PCIE10_TXP D34 → PCIE_PTX_DRX_P10 [68]
PCIE10_TXN E34 → PCIE_PTX_DRX_N10 [68]
PCIE10_RXP J35 → PCIE_PRX_DTX_P10 [68]
PCIE10_RXN L34 → PCIE_PRX_DTX_N10 [68]

JSSD2 (GEN3)

PCIE9_TXP C33 → PCIE_PTX_DRX_P9 [68]
PCIE9_TXN B33 → PCIE_PTX_DRX_N9 [68]
PCIE9_RXP G33 → PCIE_PRX_DTX_P9 [68]
PCIE9_RXN H33 → PCIE_PRX_DTX_N9 [68]

PCIE8_TXP B21
PCIE8_TXN A22
PCIE8_RXP P24
PCIE8_RXN H24

PCIE7_TXP C23
PCIE7_TXN D23
PCIE7_RXP P19
PCIE7_RXN R19

PCIE6_TXP E20
PCIE6_TXN D20
PCIE6_RXP J21
PCIE6_RXN L21

PCIE5_TXP D21
PCIE5_TXN C21
PCIE5_RXP F20
PCIE5_RXN H20

PCIE4_TXP/USB31_10_TXP D19
PCIE4_TXN/USB31_10_TXN C20
PCIE4_RXP/USB31_10_RXP P17
PCIE4_RXN/USB31_10_RXN R17

PCIE3_TXP/USB31_9_TXP E17
PCIE3_TXN/USB31_9_TXN D17
PCIE3_RXP/USB31_9_RXP H17
PCIE3_RXN/USB31_9_RXN G17

PCIE2_TXP/USB31_8_TXP C18
PCIE2_TXN/USB31_8_TXN D18
PCIE2_RXP/USB31_8_RXP J18
PCIE2_RXN/USB31_8_RXN L19

PCIE1_TXP/USB31_7_TXP C17
PCIE1_TXN/USB31_7_TXN B17
PCIE1_RXP/USB31_7_RXP J15
PCIE1_RXN/USB31_7_RXN L16

PCH_PWROK AB47 ← PCH_PWROK → PCH_PWROK [97]

RTCRST# AM45 ← PCH_RTCRST# → PCH_RTCRST# [79]
RSMRST# AA45 ← PCH_RSMRST#_AND → PCH_RSMRST#_AND [65,78,79]

RTCX2 AM48 → PCH_RTCX2
RTCX1 AM46 → PCH_RTCX1

PCH_RSMRST#_AND — RH131 10K_0201_5% — PCH_PWROK — RH132 10K_0201_5% — ESD@ CC197 100P_0201_50V8J

0111 : ESD Request

0115 : CC197 BOM cfg change to pop /ESD request

+3VL_RTC

RH125 20K_0201_1% PCH_RTCRST#

CH8 1U_0201_6.3V6M

CLRP1 JP@1 SHORT PADS

Generated from VBAT with a RC delay of 18~25 ms.

PCH_RTCX2

PCH_RTCX1

RH128 10M_0201_5%

RH129 0_0201_1% PCH_RTCX1

RH130 0_0201_1% PCH_RTCX2

YH1 32.768KHZ_12.5PF_X1A00014100-X

CH10 15P_0201_50V8J

CH11 15P_0201_50V8J

0105 : CH10/11 change from 18p to 15p

Trace Width / Space: 50 ohm /DATA: 8mil CLK: 70mil
Max Trace Length: 1000 mil

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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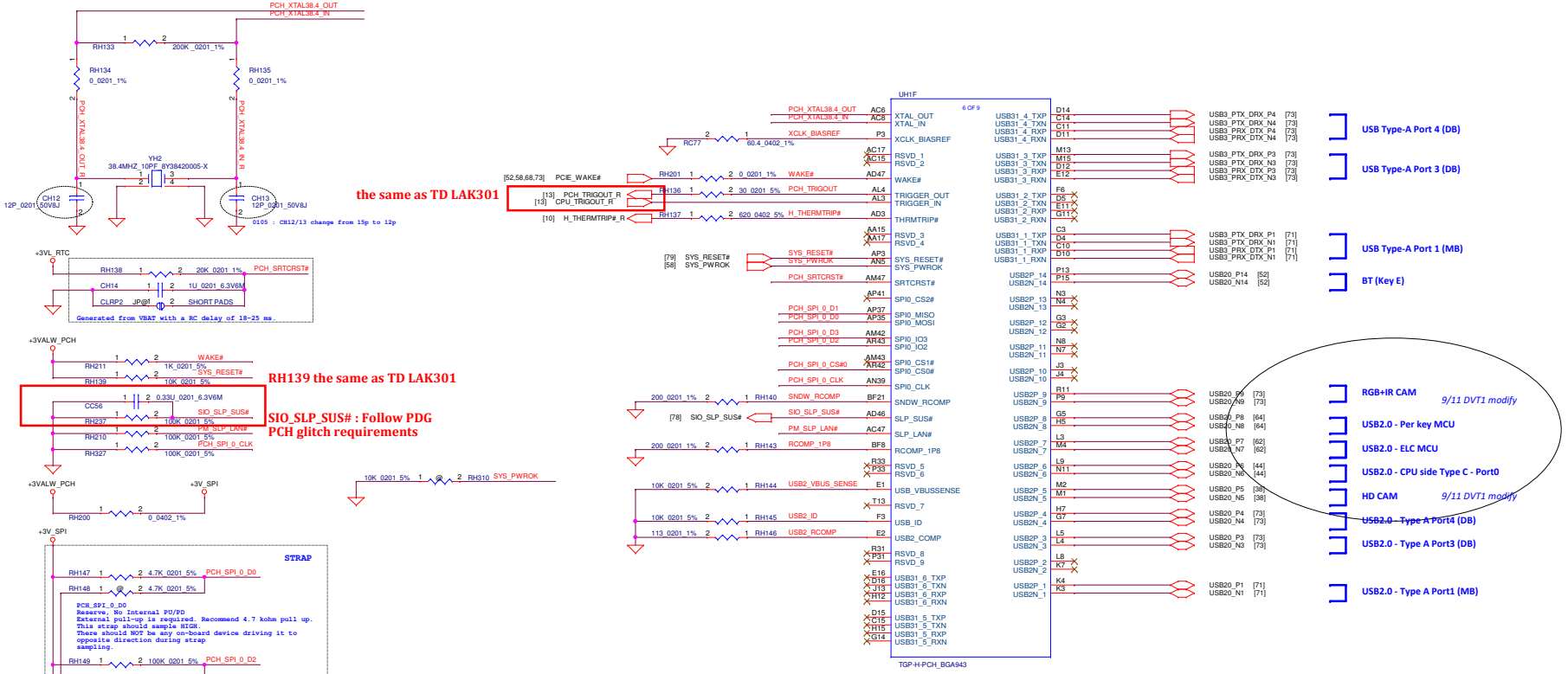
Compal Electronics, Inc.

Title: PCH(5/8)PCIE/SATA

Size	Document Number	Rev
C	LA-K452P	1.0

Date: Friday, March 19, 2021 Sheet 18 of 120



Signal Name	Pull-down Resistor Implementation	
	3.3V Signaling Mode	1.8V Signaling Mode
GPD9 / SLP_WLAN#		
GPP_J1 / CPU_C10_GATE#	N/A	75K
SLP_SUS# SLP_LAN#	100K	N/A
SPI0_CLK	100K	75K

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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Compal Electronics, Inc.	
Title	PCH(6/8)USB2&3/SPI
Size	Custom
Document Number	LA-K452P
Rev	1.0
Date:	Friday, March 19, 2021
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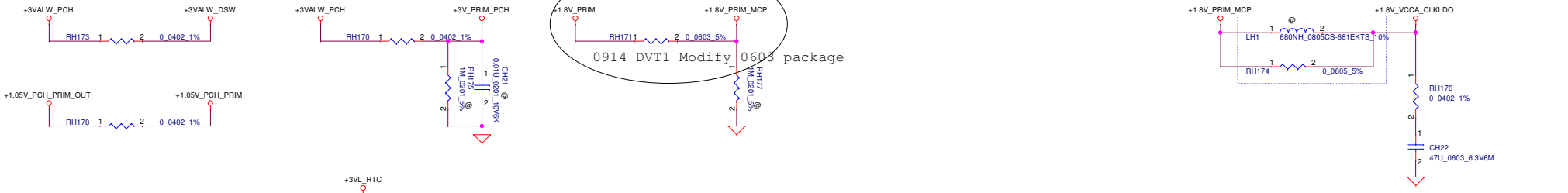
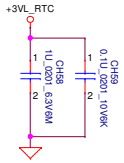
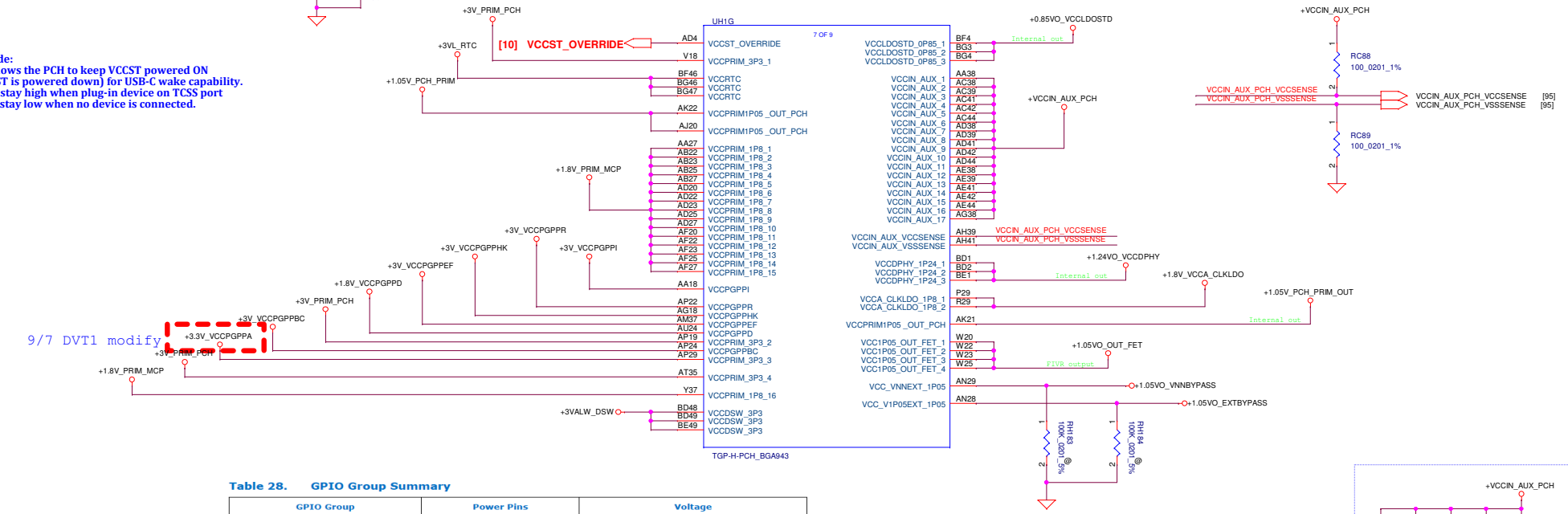
Check Current Value





VccST Override:
Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability.
-->Signal will stay high when plug-in device on TCSS port
-->signal will stay low when no device is connected.



9/7 DVT1 modify

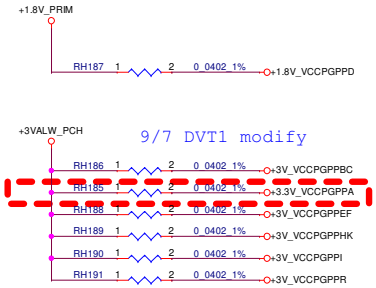
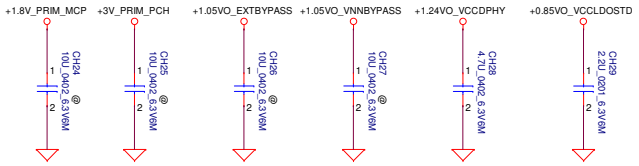


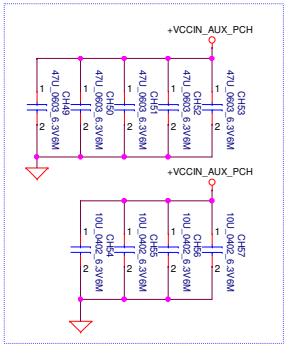
Table 28. GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C)	VCCPGPPBC	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group D (GPP_D)	VCCPGPPD	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPPEF	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group I (GPP_I)	VCCPGPPI	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8 V Only
Primary Well Group R (GPP_R)	VCCPGPPR	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group S (GPP_S)	VCCPRIM_1P8	1.8 V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: For GPIO groups that support Per-group voltage configuration, the voltage is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage.

Note: For GPIO groups that support Per-pad voltage configuration, each pin voltage is selected by setting the corresponding voltage select soft strap of the pin.





Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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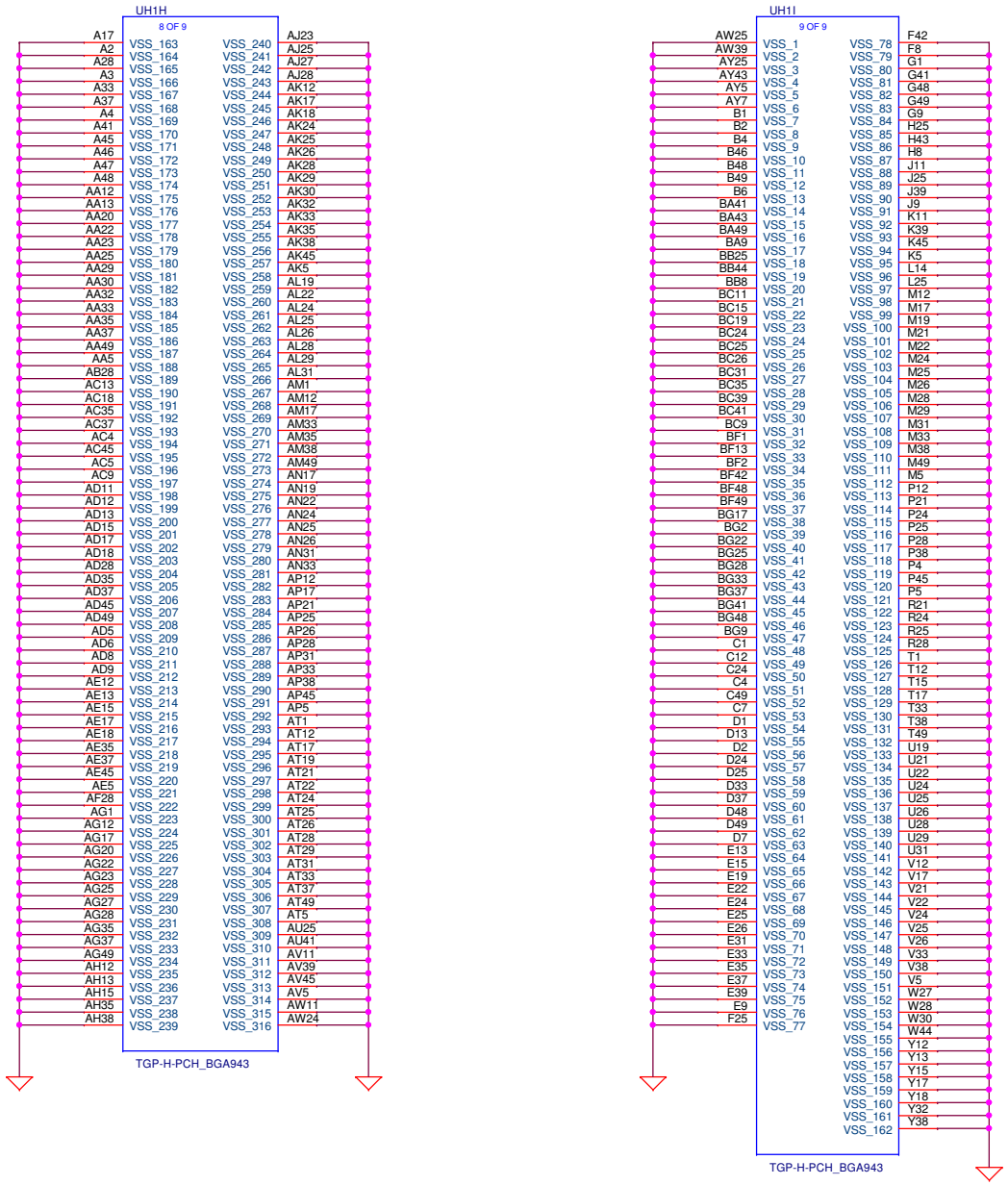
Title	Compal Electronics, Inc.		
	PCH(7/8)Power		
Size: Custom	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 20 of 120		



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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Compal Electronics, Inc.

Title: **PCH(8/8)GND**

Size	Document Number	Rev
Custom	LA-K452P	1.0

Date: Friday, March 19, 2021 Sheet 21 of 120

Main Function:

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: RSV

Size	Document Number	Rev
	LA-K452P	1.0

Date: Friday, March 19, 2021 | Sheet 22 of 120

Main Func = DDR

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

Interleaved Memory

REVERSE TYPE (4 mm)

Part Number: SP07001CW0L
Part Value: S SOCKET DEREN 40-42271-26001RHF DDR A31

For ECC DIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:
READ ADDRESS:
SA0 = _ SA1 = _ SA2 = _

Layout Note:
PLACE THE CAP near JDIMM1. 164

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: DDR4 DIMMA_RVS

Size: | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 23 of 120

Main Func = DDR

Layout Note:
Place near JDIMM2.258

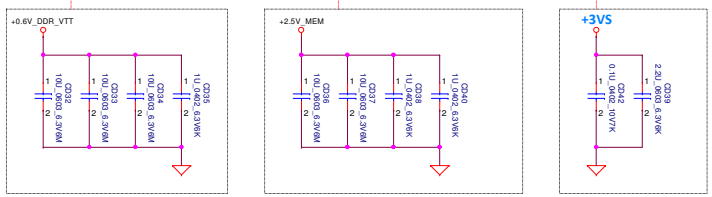
Layout Note:
Place near JDIMM2.257,259

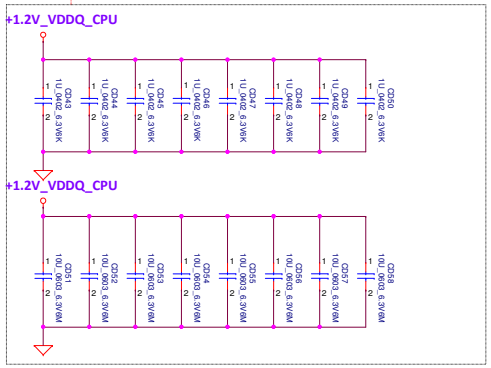
Layout Note:
Place near JDIMM2.255

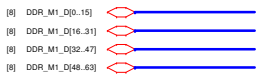
Layout Note:
Place near JDIMM2

Interleaved Memory

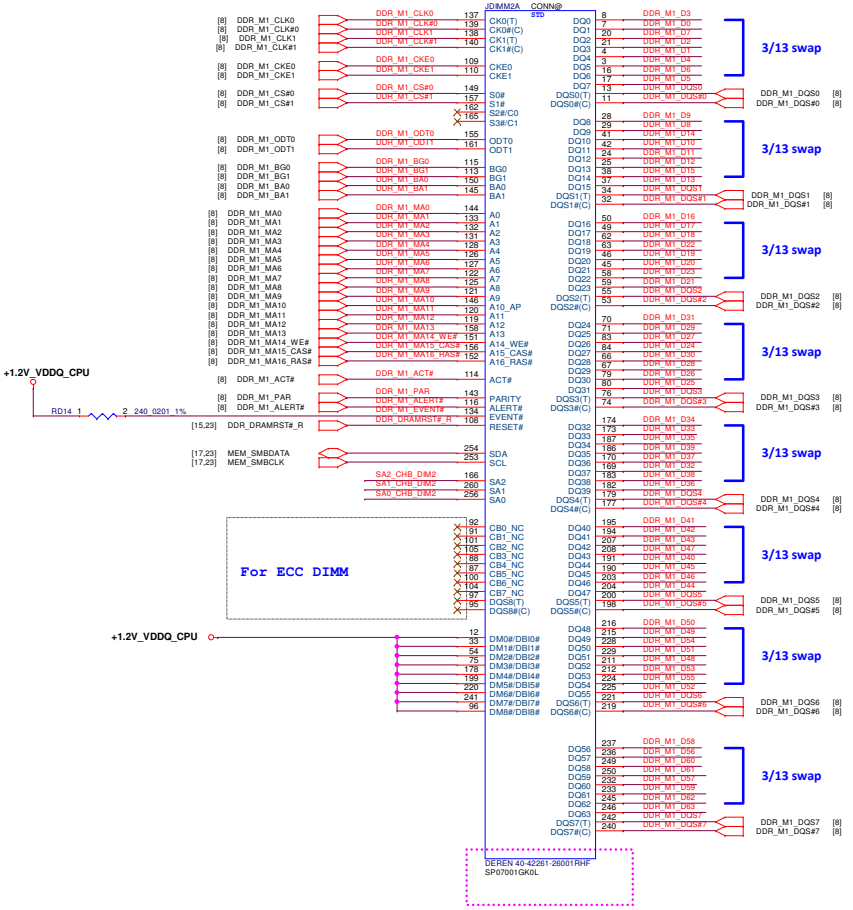
STD (4 mm)

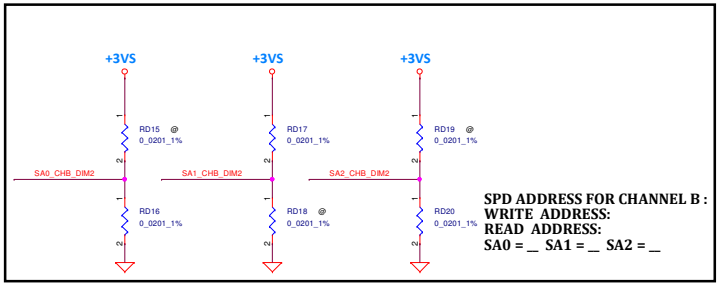




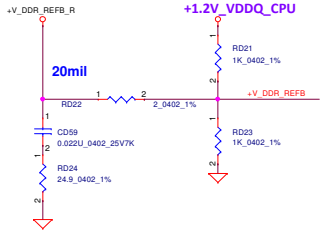


Part Number: SP07001GK0L
Part Value: S SOCKET DEREN 40-42261-26001RHF A31

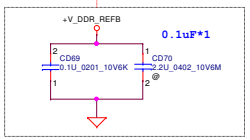


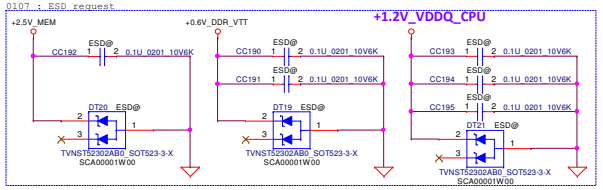


SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:
READ ADDRESS:
SA0 = _ SA1 = _ SA2 = _



Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title: DDR4 DIMMB_STD
			Size: Document Number: LA-K452P Rev: 1.0
			Date: Friday, March 19, 2021 Sheet 24 of 120

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Main Function:

VRAM X76:

ZZZ X76S6G@

ALT_GROUP PARTS VRAM 6G SAM GDP50
X7691031L01

ZZZ X76S8G@

ALT_GROUP PARTS VRAM 8G SAM GDP50
X7691031L04

8G bit GDDR6

Micron 6GB SKU		Samsung 6GB SKU		Hynix 6GB SKU	
R1	R3	R1	R3	R1	R3
	UM1 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM9 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM2 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM10 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM3 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM11 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM4 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM12 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L		UM1 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM9 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM2 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM10 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM3 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM11 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM4 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM12 VS6GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L		UM1 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM9 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM2 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM10 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM3 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM11 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM4 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM12 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L

8G bit GDDR6

Micron 8GB SKU		Samsung 8GB SKU		Hynix 8GB SKU	
R1	R3	R1	R3	R1	R3
	UM1 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM9 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM2 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM10 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM3 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM11 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM4 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM12 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L		UM1 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM9 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM2 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM10 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM3 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM11 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM4 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L UM12 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L	UM1 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM9 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM2 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM10 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM3 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM11 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM4 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM12 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L	UM1 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM9 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM2 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM10 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM3 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM11 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM4 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM12 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L

RG80 VM@ 100K +-5% 0201 SD043100380
RG83 VM@ 100K +-5% 0201 SD043100380
RG85 VM@ 100K +-5% 0201 SD043100380

RG81 VS@ 100K +-5% 0201 SD043100380
RG83 VS@ 100K +-5% 0201 SD043100380
RG85 VS@ 100K +-5% 0201 SD043100380

RG81 VH@ 100K +-5% 0201 SD043100380
RG82 VH@ 100K +-5% 0201 SD043100380
RG85 VH@ 100K +-5% 0201 SD043100380

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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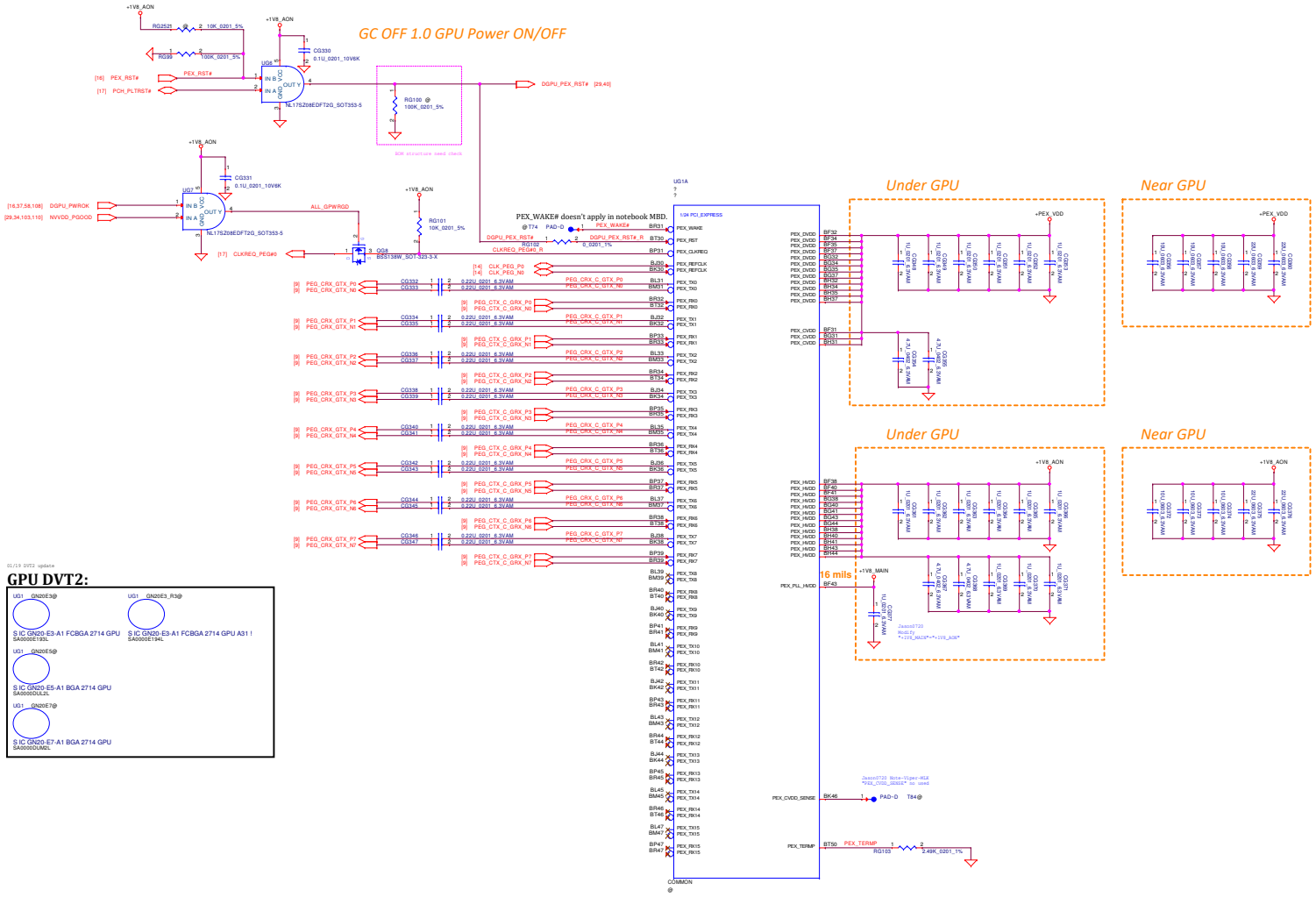
Compal Electronics, Inc.

Title: RSV

Size | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 25 of 120



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

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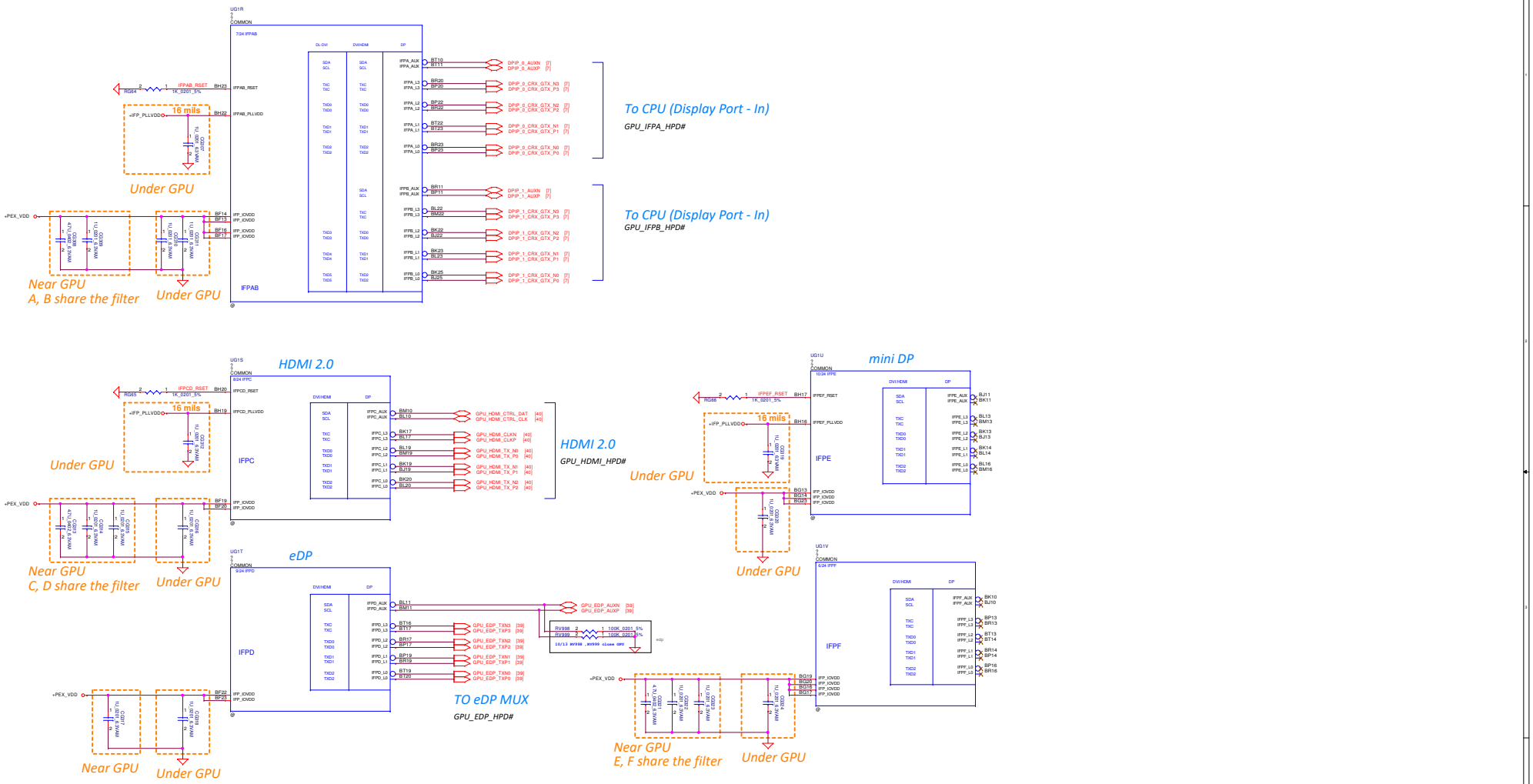
Compal Electronics, Inc.	
Title	NV(1/8) PCI EXPRESS
Size	Document Number: LA-K452P
Rev	1.0
Date: Friday, March 19, 2021	Sheet 26 of 120



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

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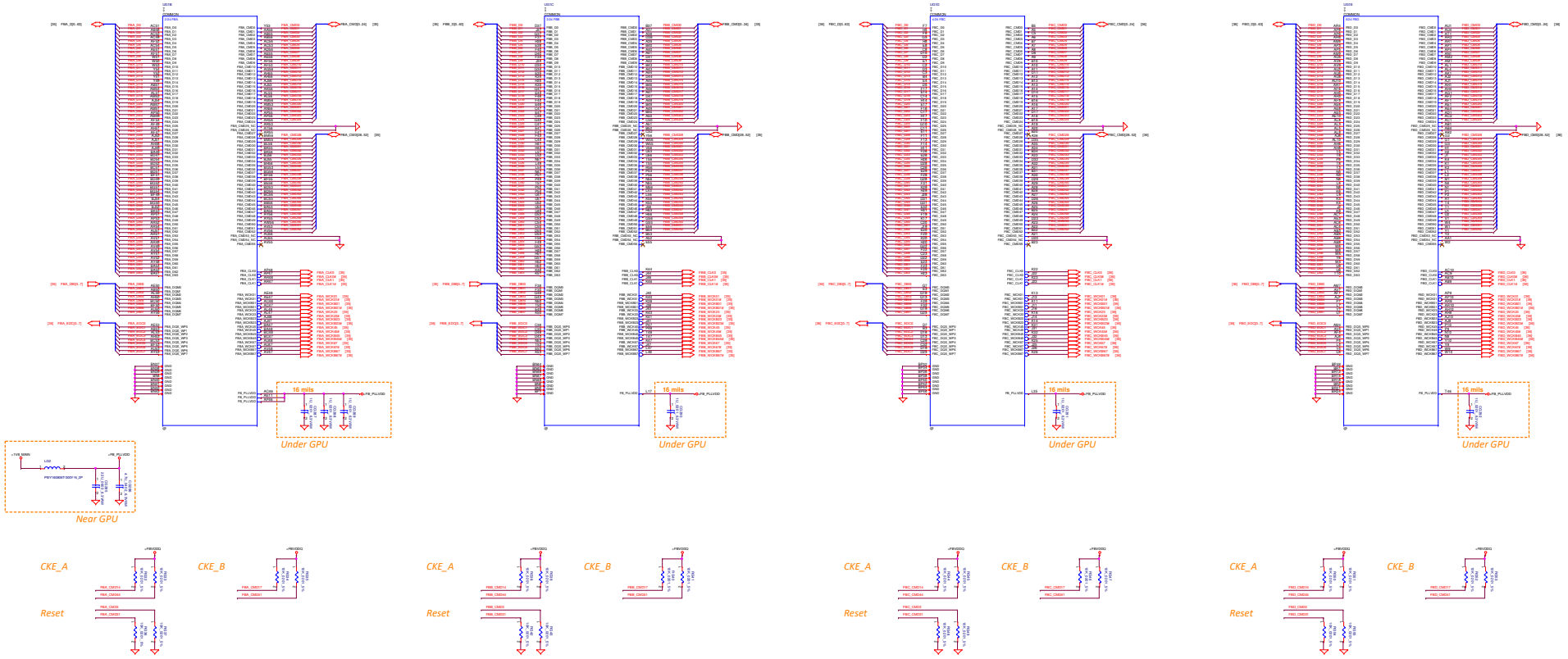
Compal Electronics, Inc.

Title: **NV(2/8) IFP ABCDEF**

Size: Document Number: **LA-K452P** Rev: 1.0

Date: Friday, March 19, 2021 Sheet 27 of 120



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/08/07	Deciphered Date	2016/08/07	Title: NVV(M) MEMORY_FB_ABCD
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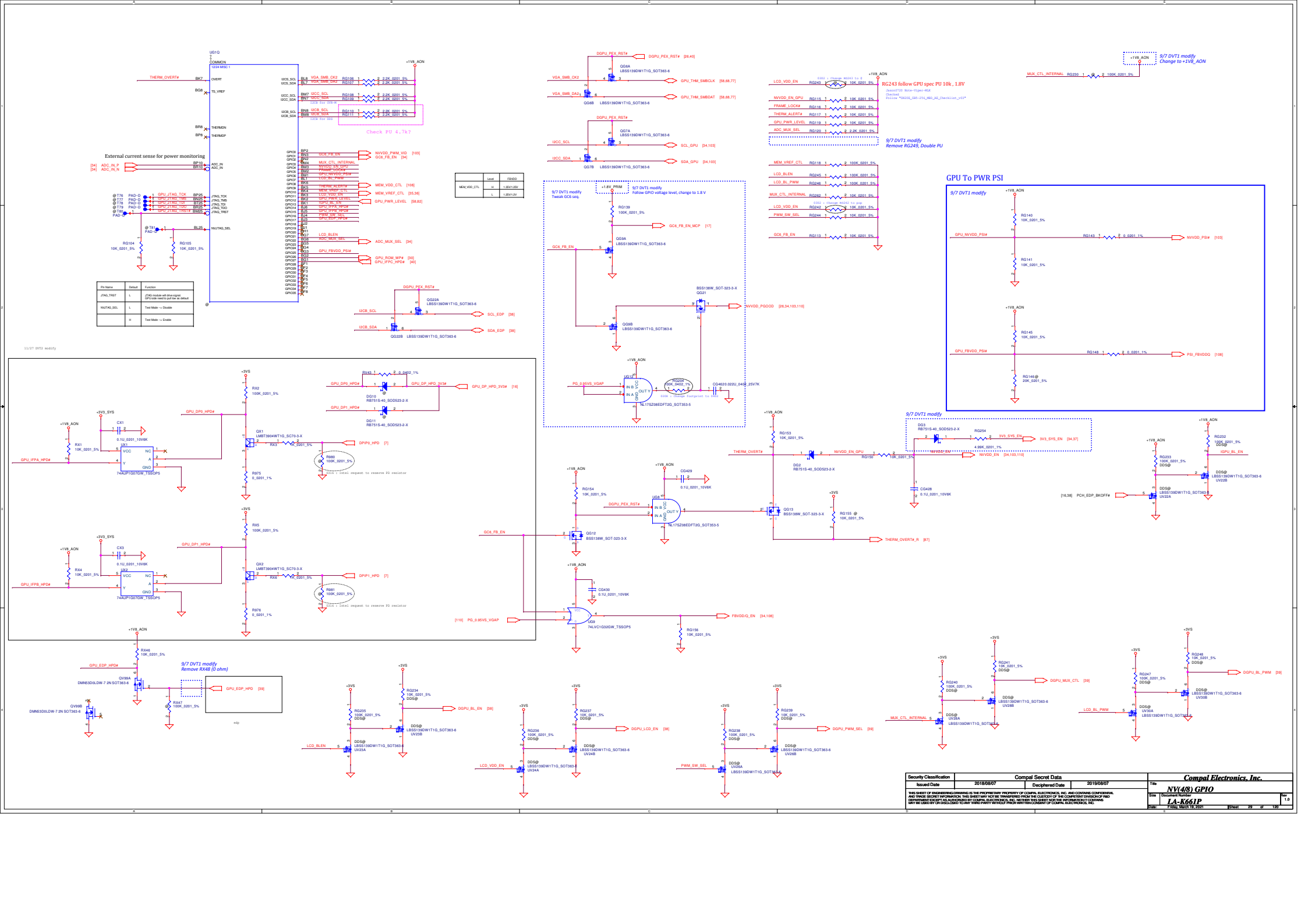
			Date: Monday, May 16, 2016	Sheet: 36 of 100


External current sense for power monitoring
Check PU 4.7k?
9/7 DVT1 modify
Remove RG249, Double PU
RG243 follow GPU spec PU 10k , 1.8V
9/7 DVT1 modify
Change to +1V8_AON
GPU To PWR PSI
9/7 DVT1 modify
Tweak GC6 seq.
9/7 DVT1 modify
Follow GPIO voltage level, change to 1.8 V
9/7 DVT1 modify
Remove RX48 (0 ohm)
9/7 DVT1 modify
11/27 DVT2 modify
Compal Secret Data
Compal Electronics, Inc.
NV(4/8) GPIO
LA-K661P
Friday, March 19, 2021
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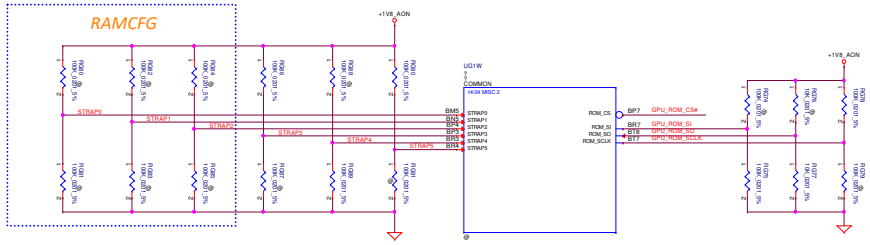

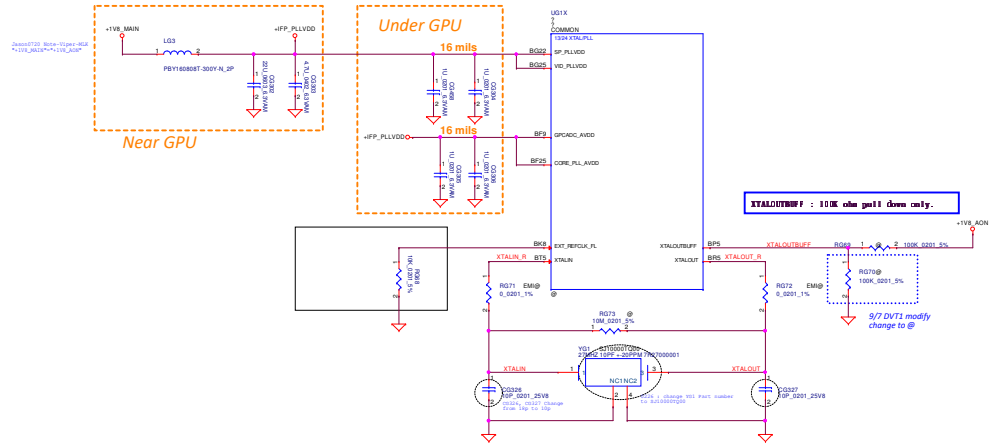

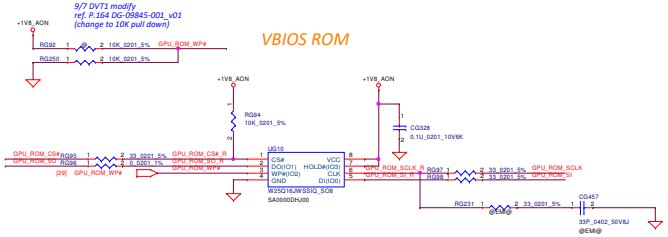

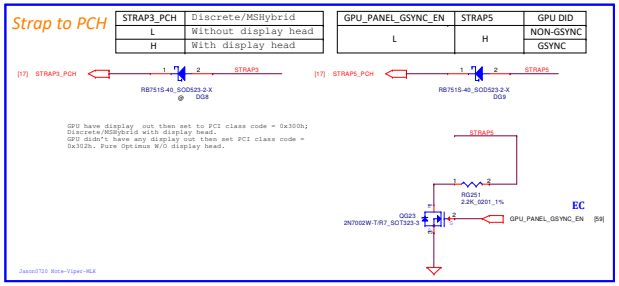

STRAP3_PCH	Discrete/MSHybrid
L	Without display head
H	With display head

GPU_PANEL_GSYNC_EN	STRAP5	GPU DID
L	H	NON-GSYNC
		GSYNC

GPU have display out then set to PCI class code = 0x300;
Discrete/MSHybrid with display head.
GPU didn't have any display out then set PCI class code = 0x302h. Pure Optimus W/O display head.

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Table 1. GN20-E7 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x7	14 Gbps	2026	Full	Production candidate
			Micron	TBD	TBD	0x8	14 Gbps	N/A	Full	Production candidate
			Hynix	TBD	TBD	0xB	14 Gbps	N/A	Full	Production candidate
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened for 11 Gbps @ 1.2V supports Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened for 11 Gbps @ 1.2V supports Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E7, the maximum allowable memory case temperature is 95 °C.

Table 3. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened for 11 Gbps @ 1.2V supports Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened for 11 Gbps @ 1.2V supports Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E3, the maximum allowable memory case temperature is 95 °C.

Table 2. GN20-E5/E4 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened for 11 Gbps @ 1.2V supports Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened for 11 Gbps @ 1.2V supports Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E5/E4, the maximum allowable memory case temperature is 95 °C.

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 [0x0000]
L	L	H	1 [0x0001]
L	H	L	2 [0x0002]
L	H	H	3 [0x0003]
H	L	L	4 [0x0004]
H	L	H	5 [0x0005]
H	H	L	6 [0x0006]
H	H	H	7 [0x0007]
L	L	M	8 [0x0008]
L	M	L	9 [0x0009]
L	M	H	10 [0x000A]
L	H	M	11 [0x000B]
M	L	L	12 [0x000C]
M	L	H	13 [0x000D]
M	H	L	14 [0x000E]
M	H	H	15 [0x000F]

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
H	L	M	16 [0x0010]
H	M	L	17 [0x0011]
H	M	H	18 [0x0012]
H	H	M	19 [0x0013]
L	M	M	20 [0x0014]
M	L	M	21 [0x0015]
M	M	L	22 [0x0016]
M	M	H	23 [0x0017]
M	H	M	24 [0x0018]
H	M	M	25 [0x0019]
M	M	M	26 [0x001A]

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	For DDS unify VBIOS used
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

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Edward_Chen NV Dell Notebook 2020/06/04 19:45:27

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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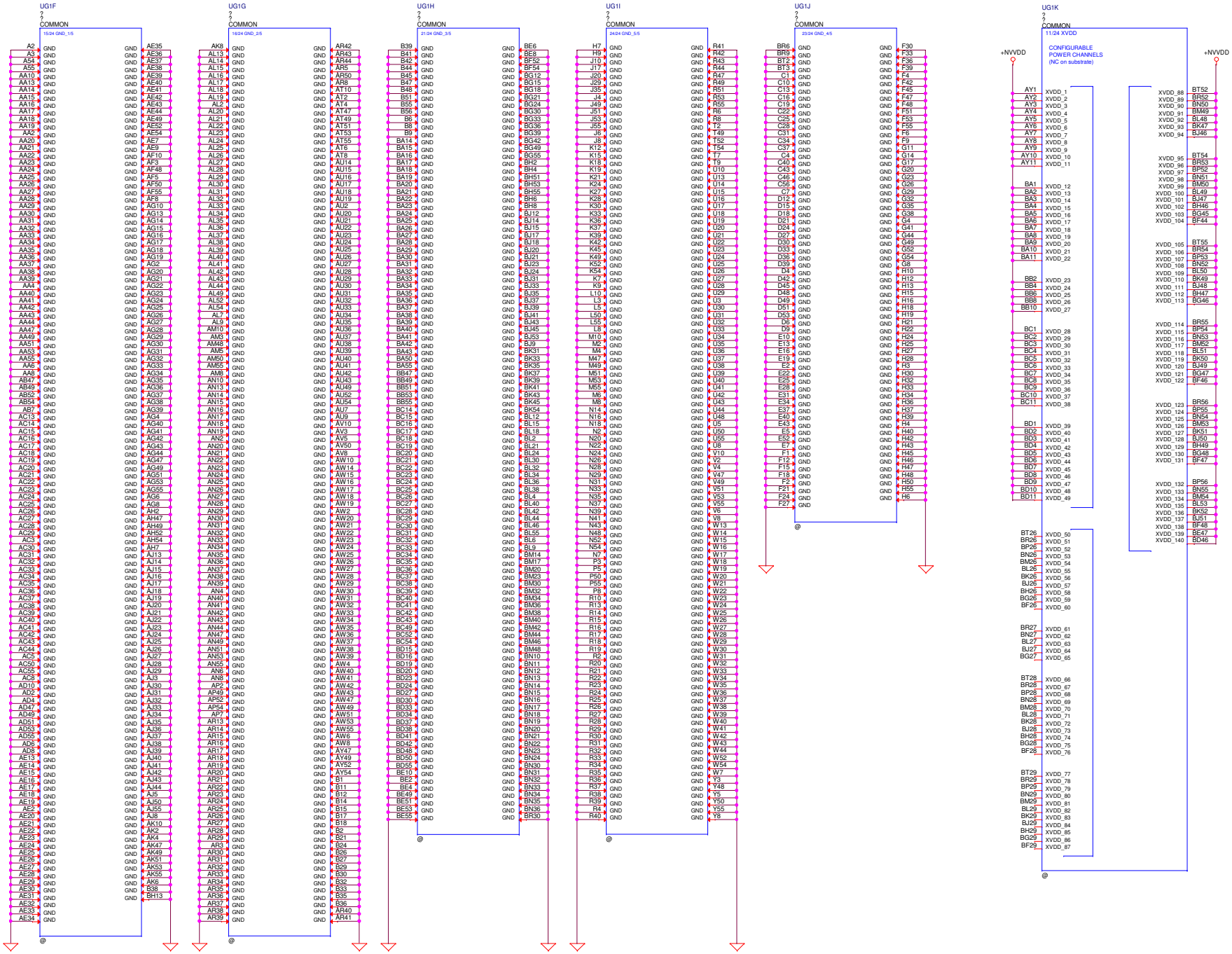
Compal Electronics, Inc.		
Title: NV(4/8) STRAP, ROM, XTAL		
Size: D	Document Number: LA-K661P	Rev: 1.0
Date: Friday, March 19, 2021	Sheet 30 of 120	



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

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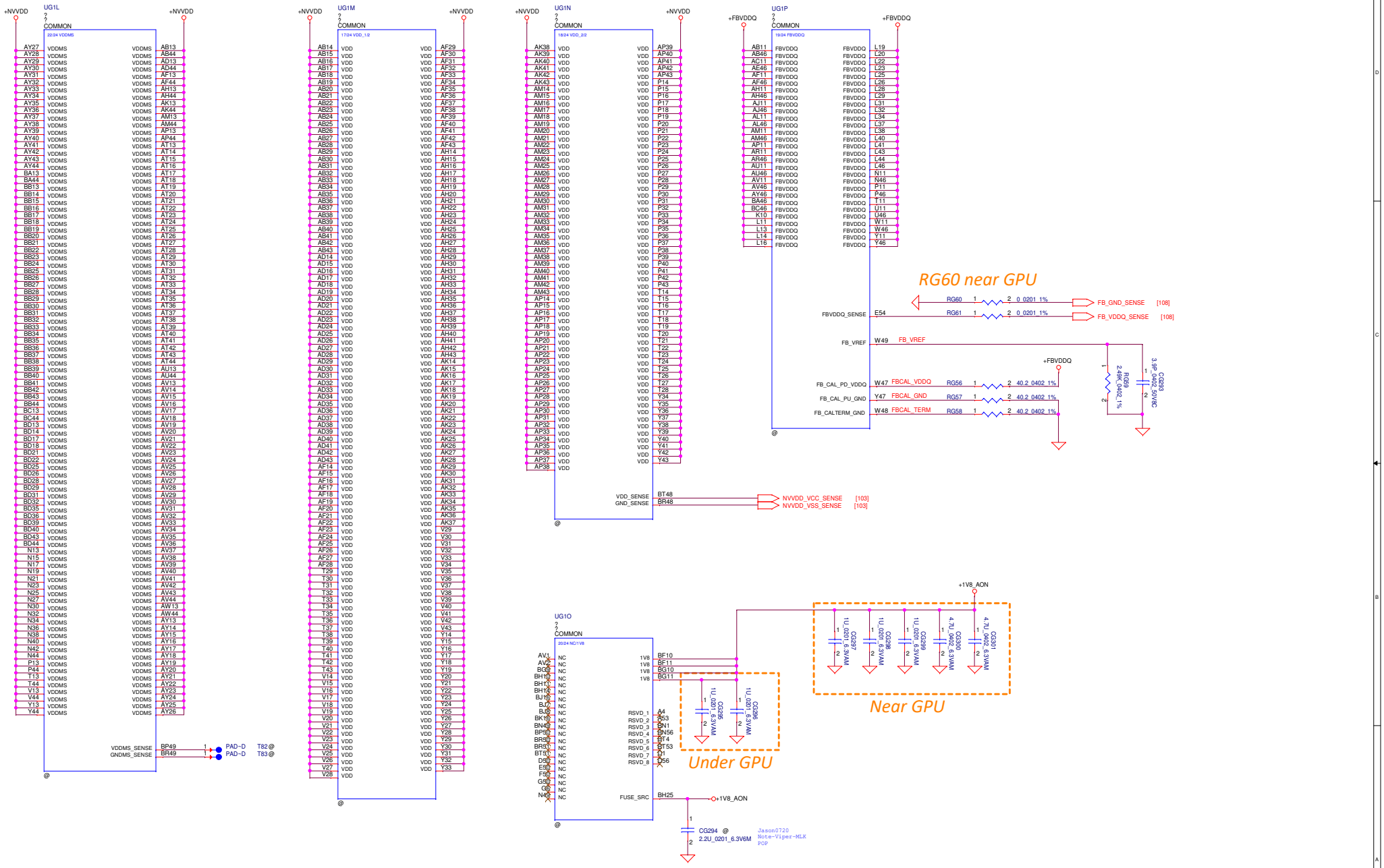
Compal Electronics, Inc.

Title: **NV(6/8) GND, RFUs**

Size	Document Number	Rev
	LA-K661P	1.0

Date: Friday, March 19, 2021 | Sheet 31 of 120



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

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Compal Electronics, Inc.

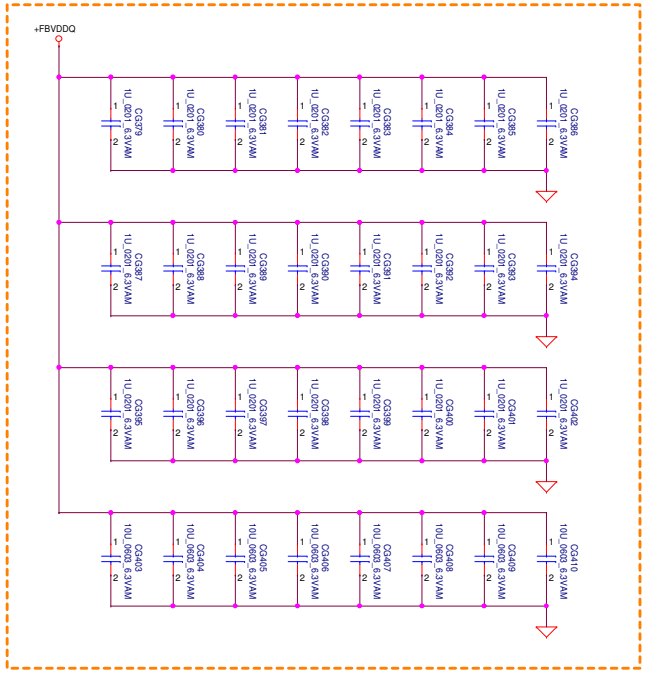
Title: **NV(7/8) POWERS**

Size	Document Number	Rev
	LA-K661P	1.0

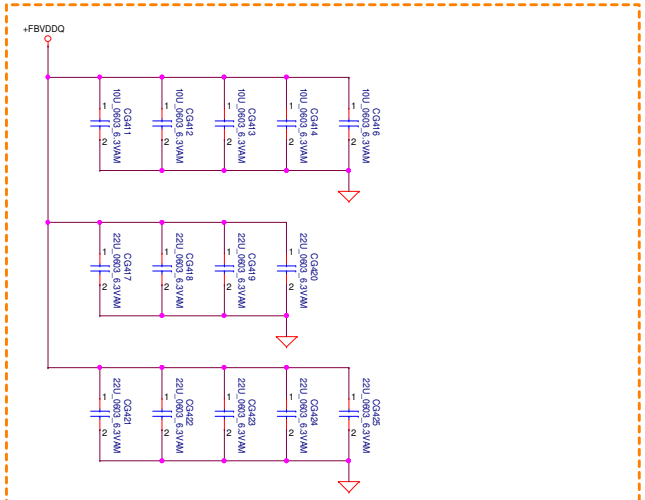
Date: Friday, March 19, 2021 | Sheet 32 of 120

FBVDDQ_GPU

Under GPU



Near GPU



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

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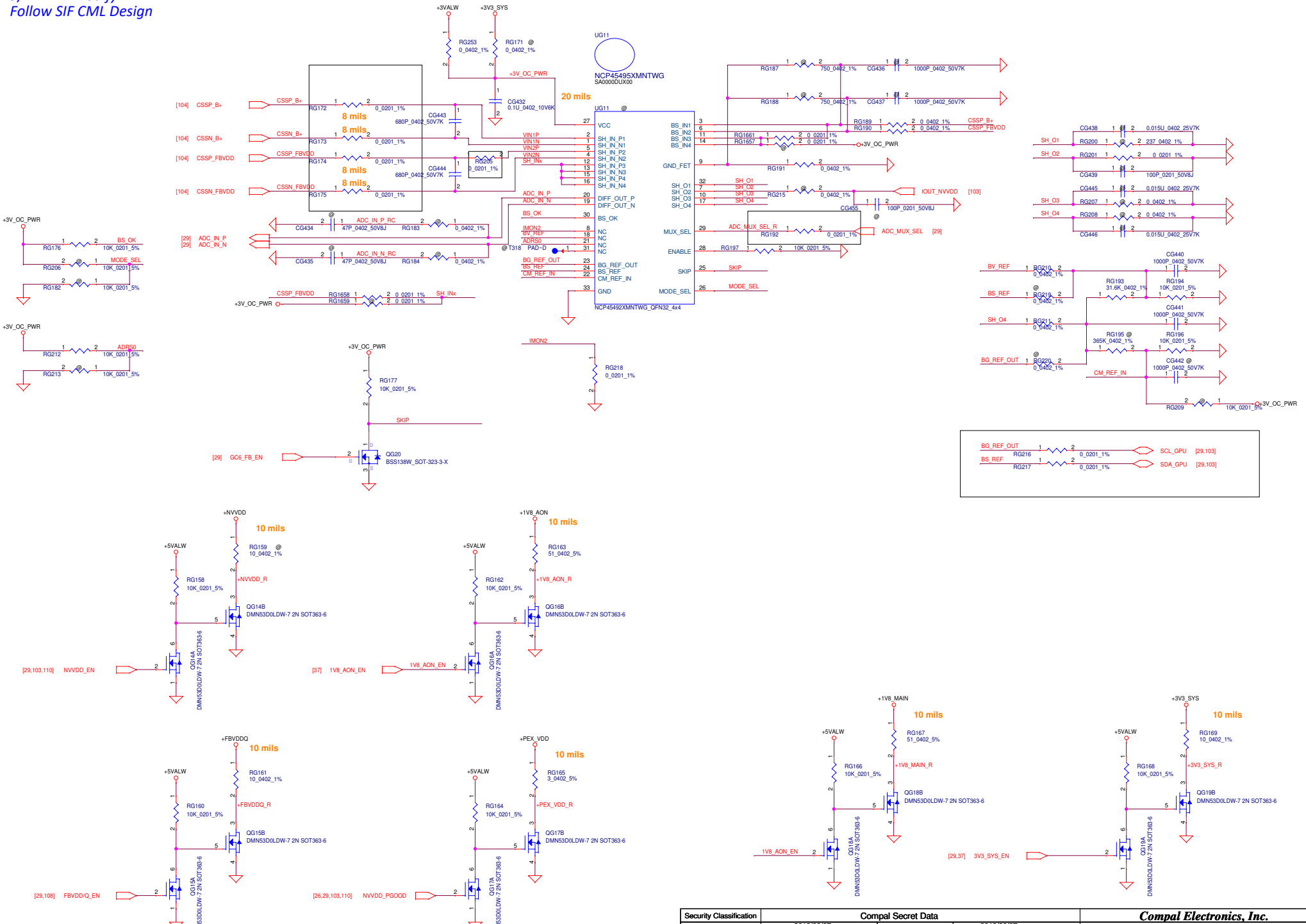
Compal Electronics, Inc.		
Title: NV(8/8) GPU DECOUPLING		
Size	Document Number: LA-K452P	Rev: 1.0
Date: Friday, March 19, 2021	Sheet 33 of 120	

9/7 DVT1 modify
Follow SIF CML Design



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

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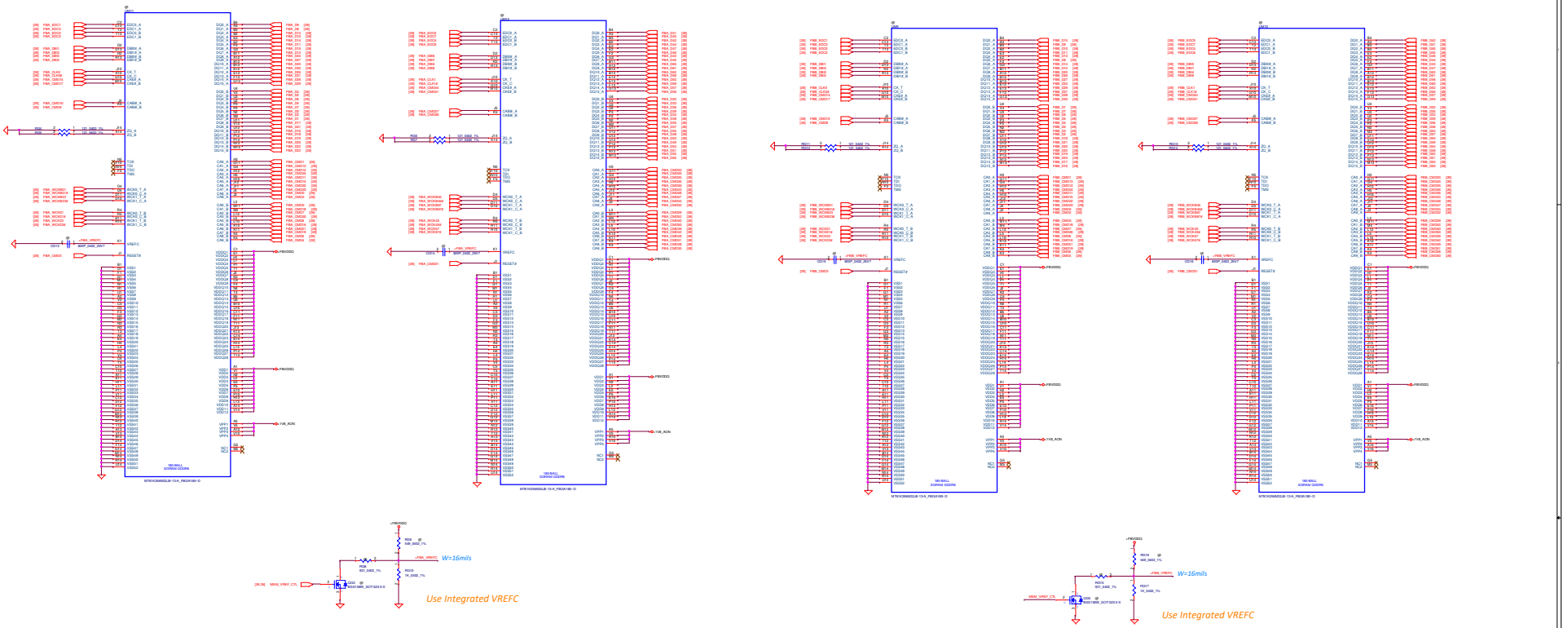
Compal Electronics, Inc.

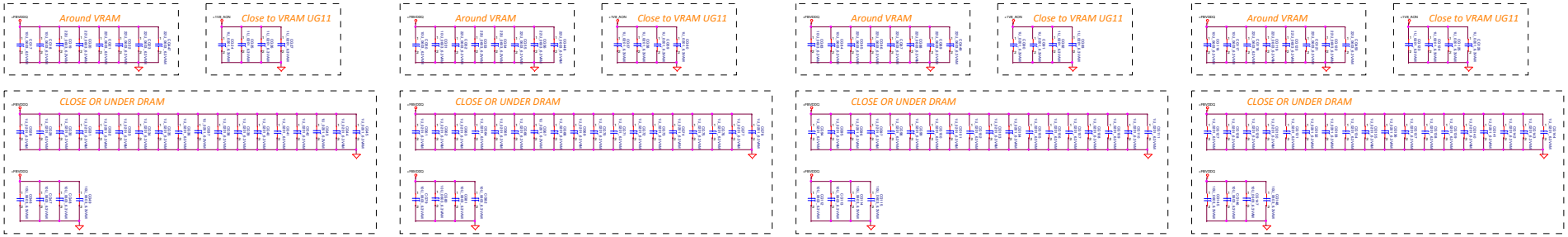
Title: **OC, Discharging**

Size	Document Number	Rev
	LA-K452P	1.0

Date: Friday, March 19, 2021 | Sheet 34 of 120



UM11 UM12 UM9 UM10



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/08/27	Deciphered Date	2015/08/27	Title: VRAM_GDDR5_AB

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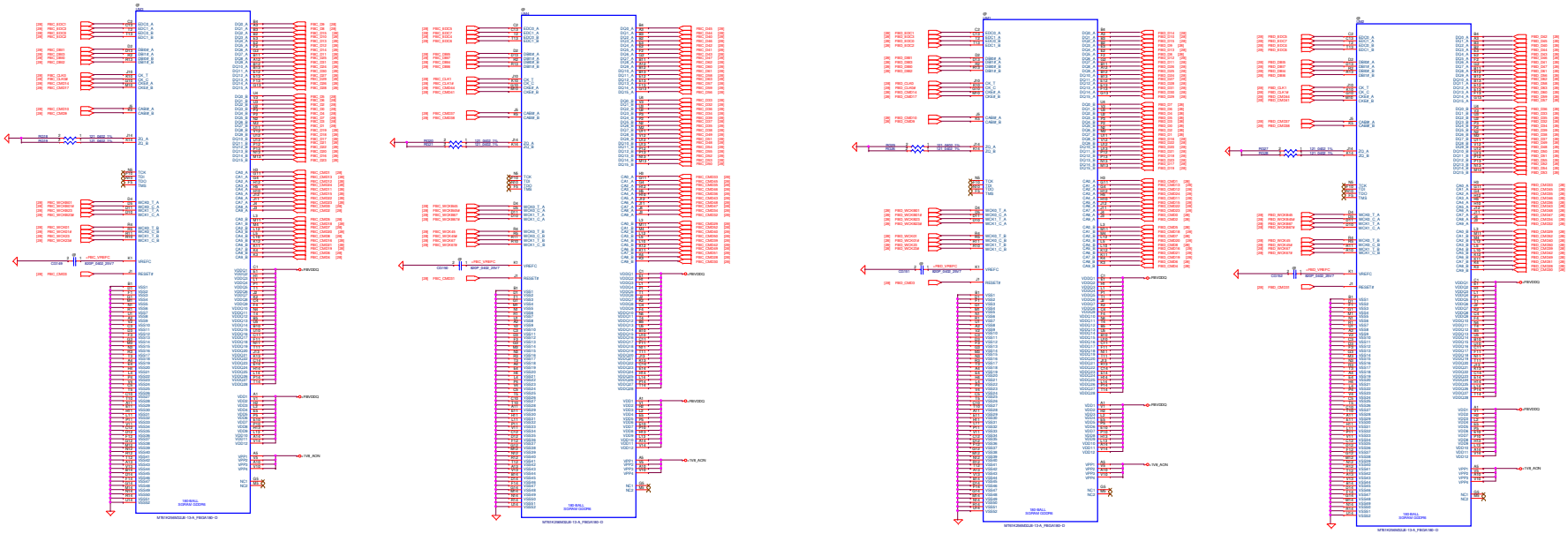
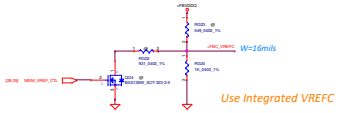
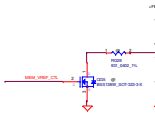
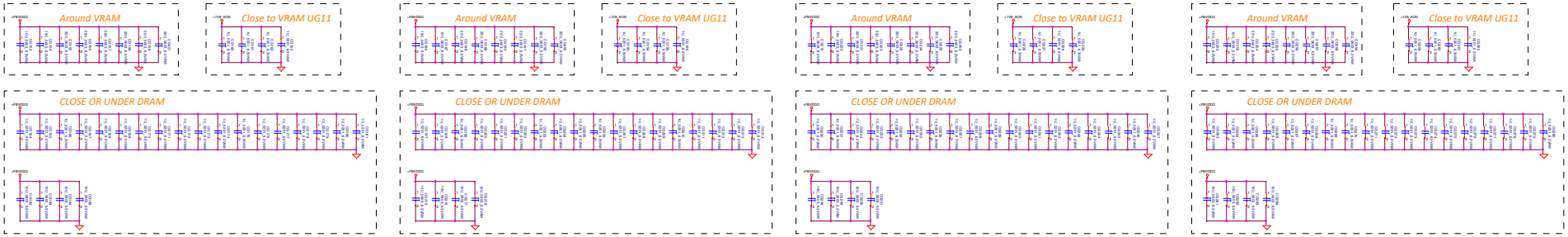
Size: B	Project Code: LA-K661P	Rev: 1A	Sheet: 36 of 58







UM3 UM4 UM1 UM2



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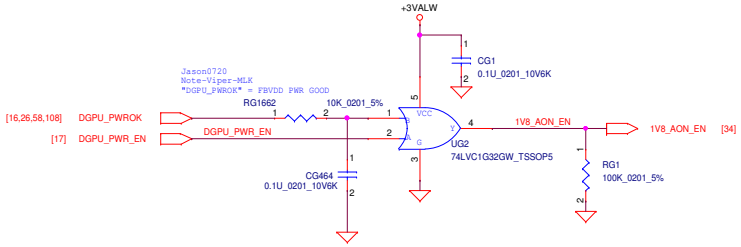
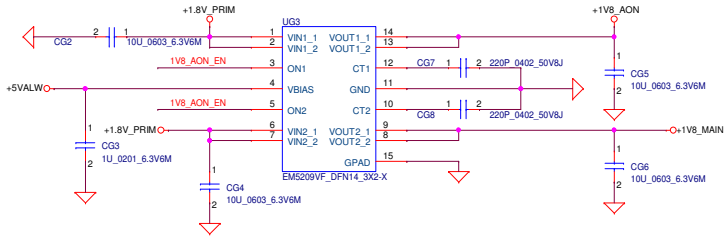
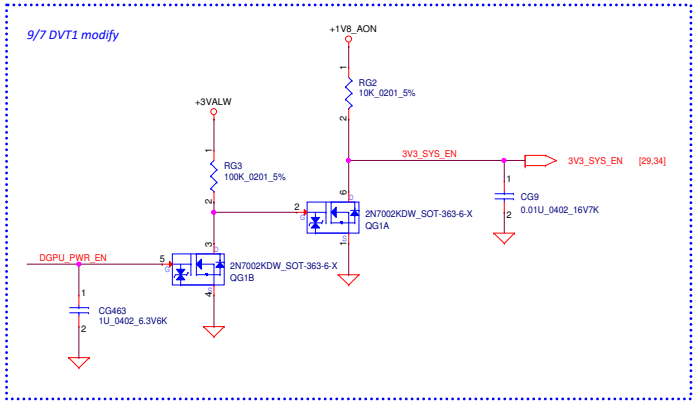
Issued Date	2016/08/07	Deciphered Date 2016/08/07	Title VRAM_GDDR5_CD
			Document Number LA-K661P
			Rev 1A
			Date: Monday, May 08, 2017 Sheet 36 of 58

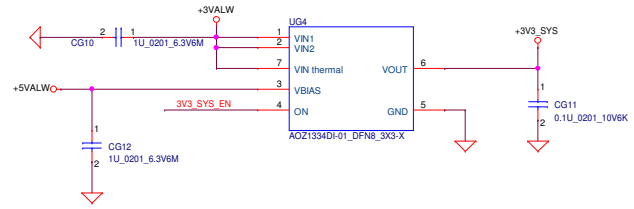
+1V8_AON / +1V8_MAIN(PLL)



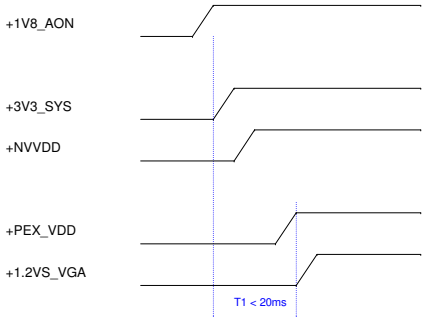




NV_3V3(For Sequence)

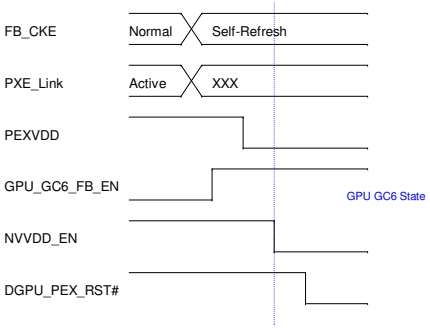


GPU Power Up Sequence



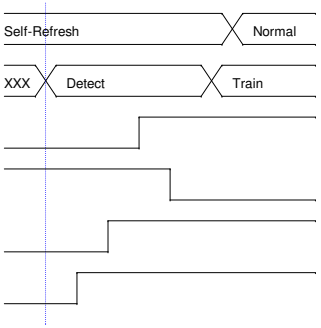
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

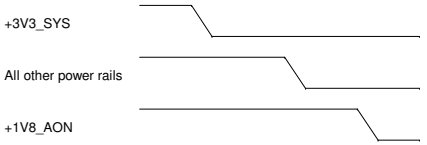


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



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Compal Electronics, Inc.

Title: DGPU_DC/DC Interface

Size	Document Number	Rev
	LA-K661P	1.0

Date: Friday, March 19, 2021 | Sheet 37 of 120

Main Func = LCD

BL_EN

PCH [16,29] PCH_EDP_BKOFF#

GPU [29] DGPU_BL_EN

DDS_BL_EN

DV3 output Discharge

EC DDS EC_BKOFF

EC

DDS_PANEL_BKEN_EC

DDS_BL_EN

ENBKL_D

Need to check 6/23

10/20 DVT1 modify
SA0003R000 change to SA0000BIP00

EC (BIST MODE)

PANEL_BKEN_EC

ENBKL

EC (BIST MODE)

LCD_TST

LCD_TST_C

10/13 Modify close JEDP

W=60 mils

W=60 mils

1.5A

Pin 30
RSV for NV/non-NV

2020/07/10 modify,
for LCDVDD discharge

Main Func = DMIC

10/5 DVT1 modify
Separate ARK/SIF DMIC Signal
Reference Horizen

DMIC 1.8V POWER

DMIC 3.3V POWER

To PCH

From Module

DATA OUTPUT

DATA INPUT

0115 : Change patr on DMIC to IO Path BOM cfg to @

9/7 DVT1 modify

From Module

Main Func = LCDVDD monitor

For BL_PWR_SRC & LCDVDD monitor

10/20 DVT1 modify
SC100000500 change to SCS00006300

10/20 DVT1 modify
SC100000500 change to SCS00006300

Main Func = Hinge up protection

LCD_EN

PCH [16] PCH_ENVDD

GPU [29] DGPU_LCD_EN

DV6 output Discharge

EC-DDS
Panel RST

EC [59] DDS_PANEL_RESET#

10/20 DVT1 modify
SA0003R000 change to SA0000BIP00

EC (BIST MODE)

LCD_VCC_TEST_EN

9/7 DVT1 modify

to EC

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Compal Electronics, Inc.

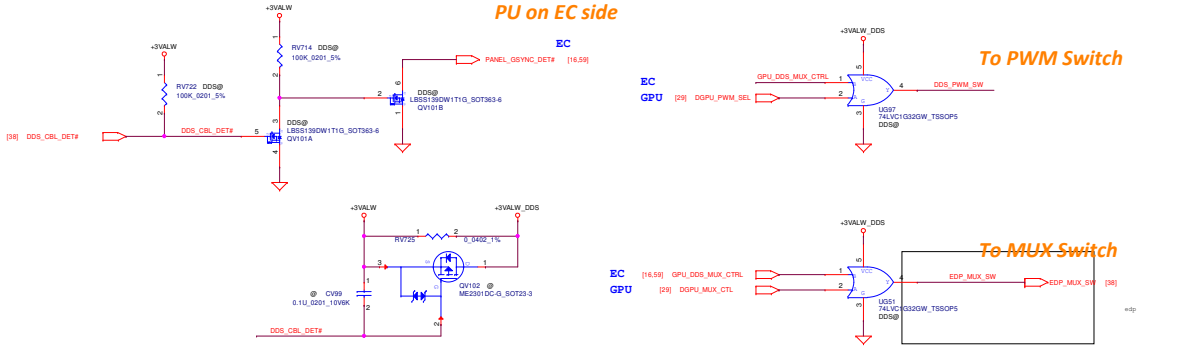
Title: eDP/Camera

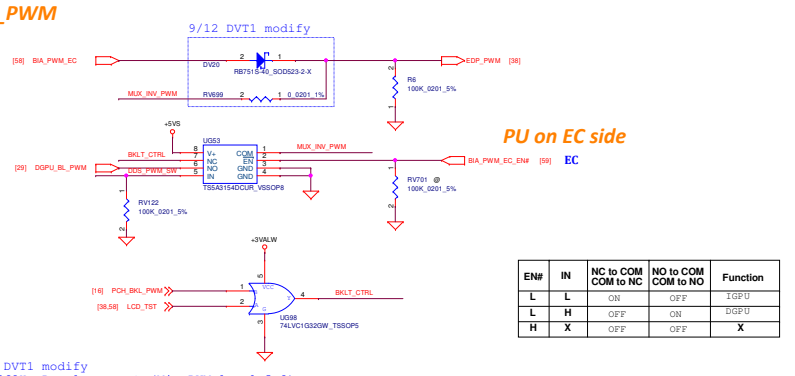
Size: Document Number: LA-K452P Rev: 1.0

Date: Friday, March 19, 2021 Sheet 38 of 120

Main Func = eDP DDS PWM

9/12 DVT1 modify
Change DDS detect logic to "Low" (EC)

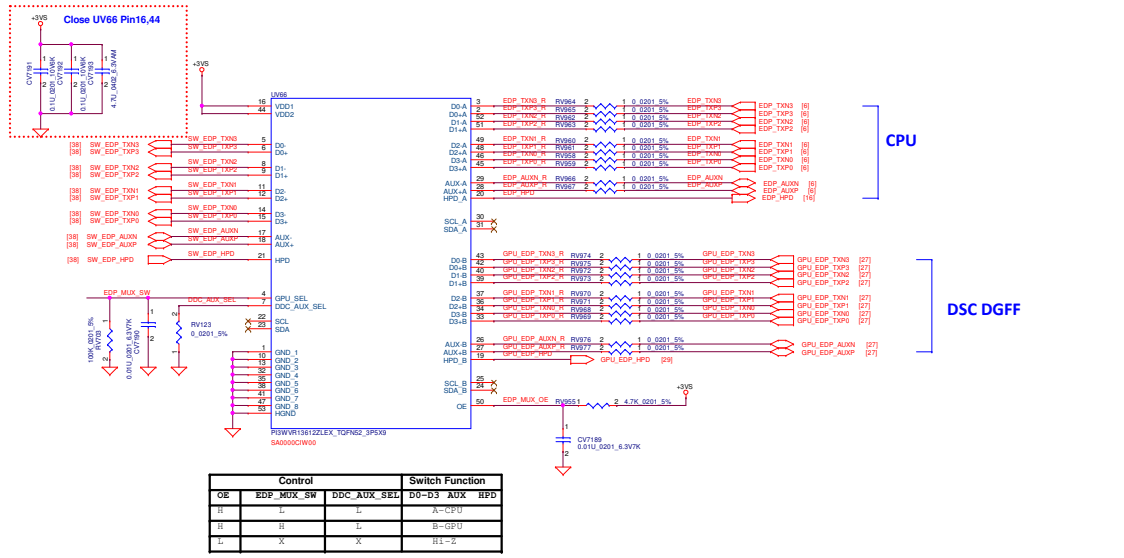




EN#	IN	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	IGPU
L	H	OFF	ON	DGPU
H	X	OFF	OFF	X

9/16 DVT1 modify
For 360Hz Panel support (Min PWM level 3.0)

Main Func = eDP DDS MUX



Control			Switch Function
OE	EDP_MUX_SW	DDC_AUX_SEL	D0-D3 AUX HPD
H	L	L	A-CPU
H	H	L	B-GPU
L	X	X	Hi-Z

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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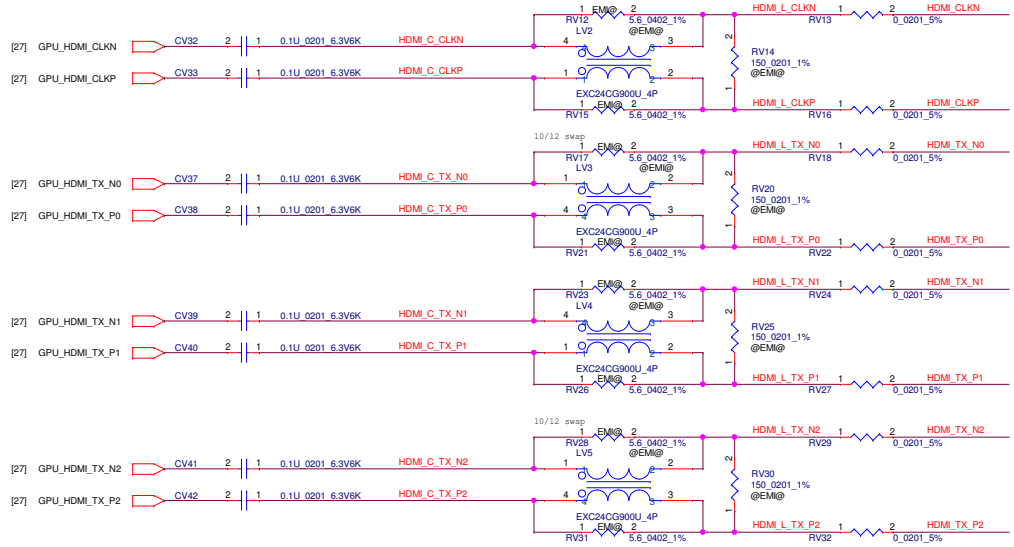
Compal Electronics, Inc.

Title: eDP MUX/DDS

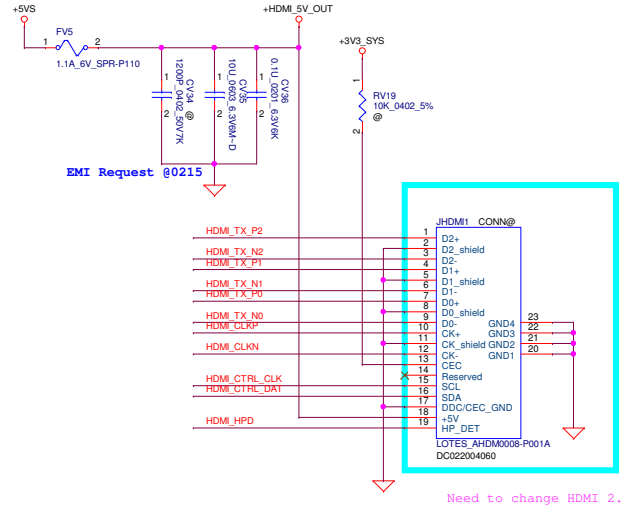
Size: Document Number: LA-K452P Rev: 1.0

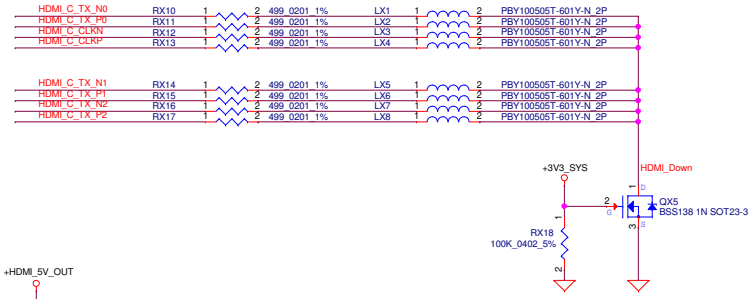
Date: Friday, March 19, 2021 Sheet 39 of 120

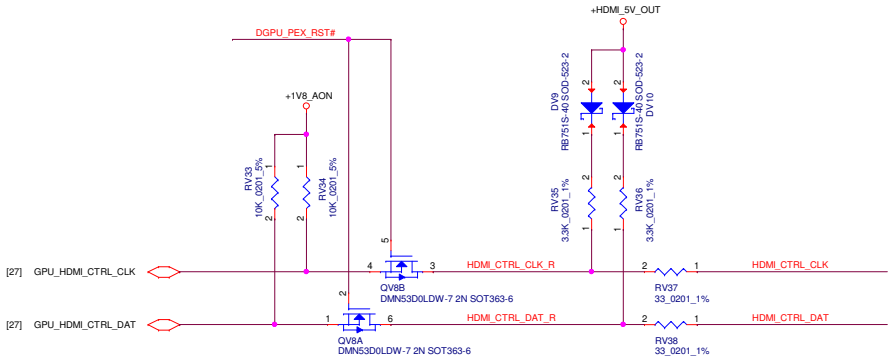
20200720
BOM change:
i. Reserve Resistor 12pcs:
5.6ohm *8pcs, 150ohm *4pcs
ii. Add EMI chokes *4pcs(change choke to SM070002R00)

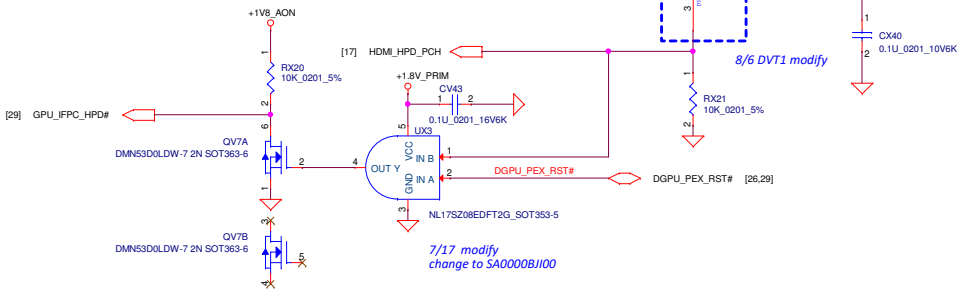


0312 : Change LV2~LV5 footprint to -NPM
20200720 modify SM070003V00 to SM070002R00









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Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Title: **HDMI**

Size | Document Number: **LA-K452P** | Rev: 1.0

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Issued Date	2020/03/05	Deciphered Date	2019/04/01

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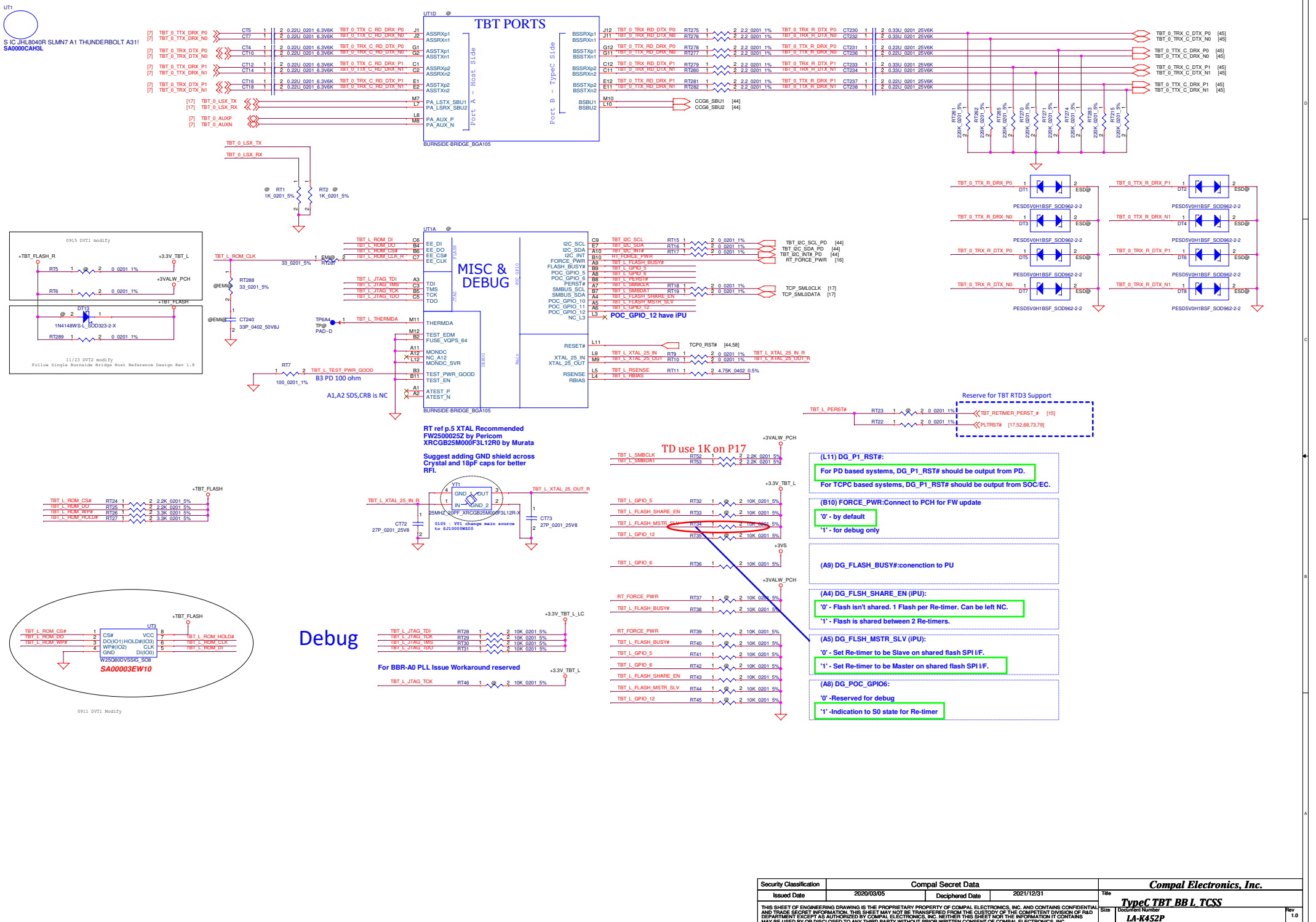
Title: RSV

Size | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 41 of 120



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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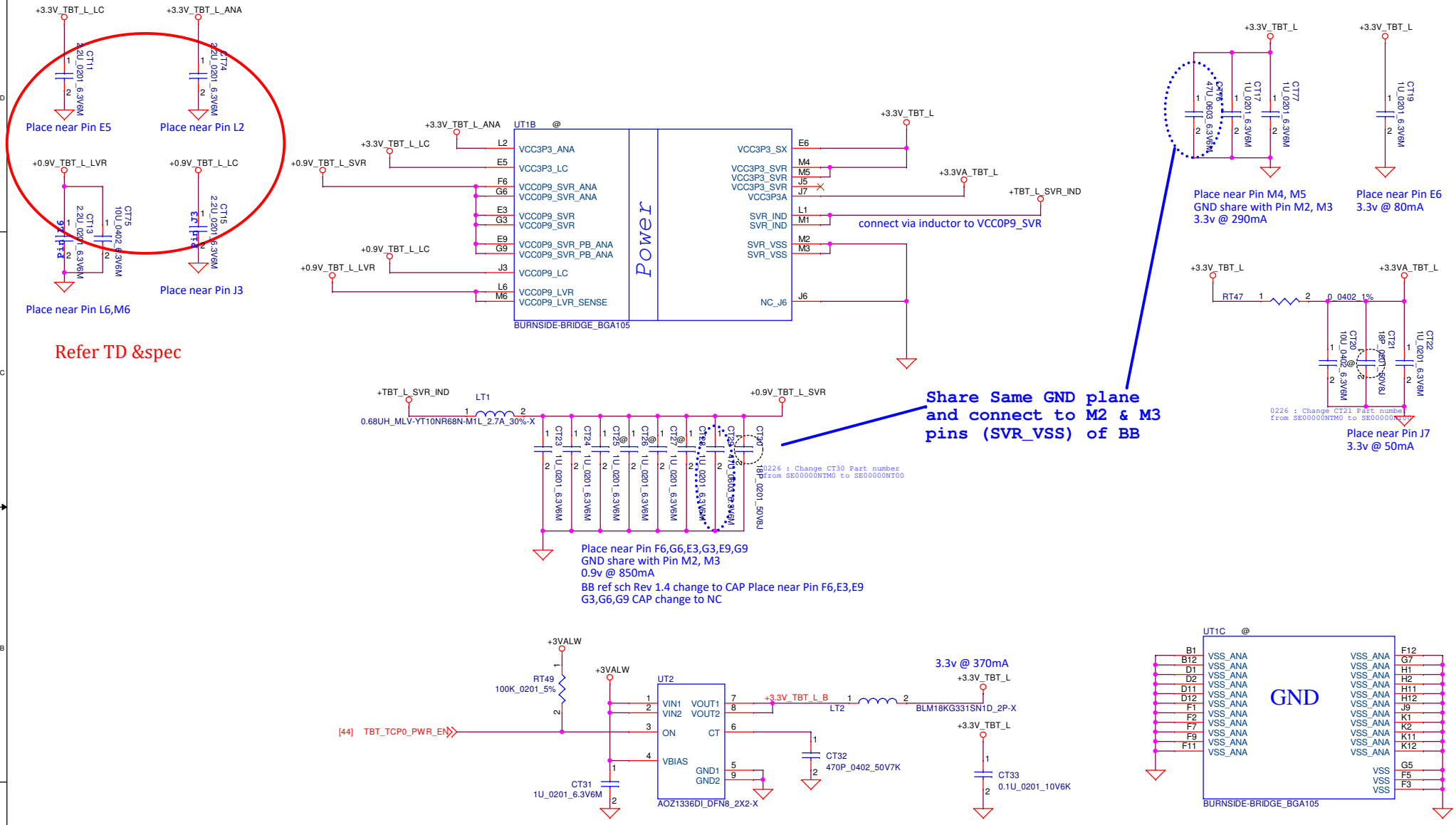
Compal Electronics, Inc.			
Title: TypeC TBT BB L TCSS			
Size	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 42 of 120		



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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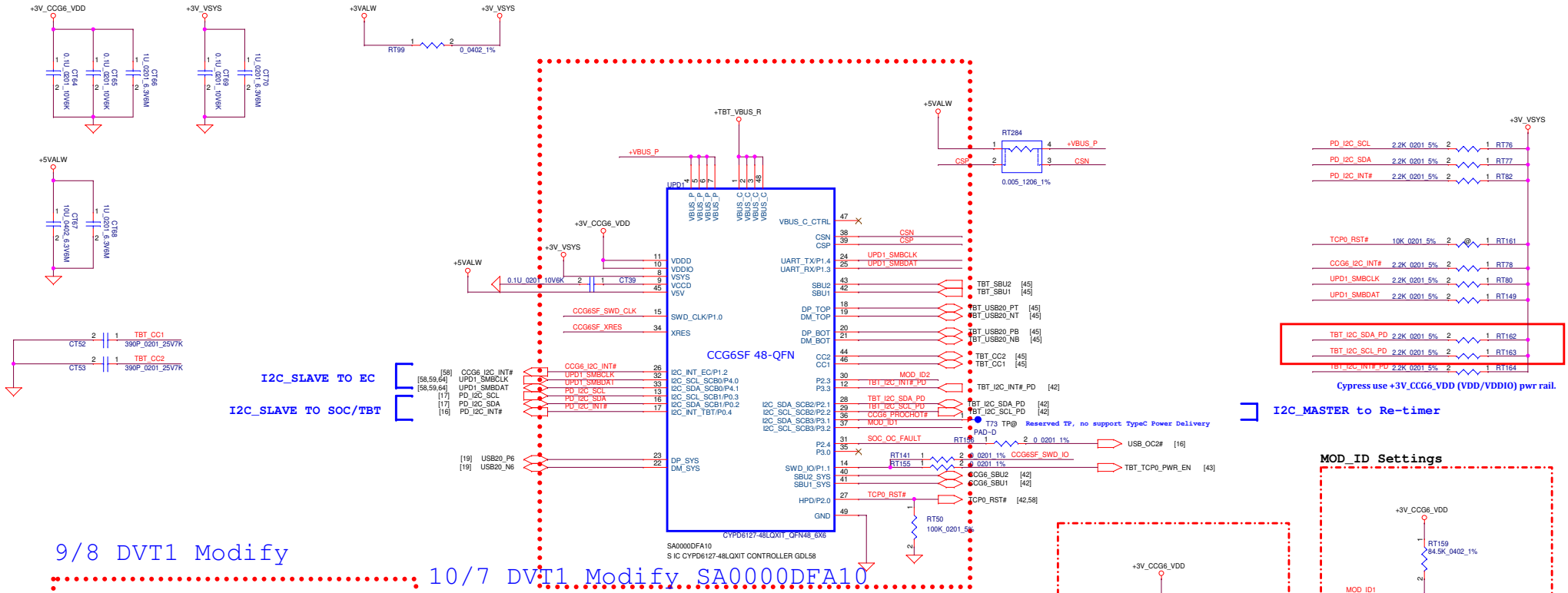
Compal Electronics, Inc.

Title: TypeC TBT_BB L_PWR,GND

Size | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 43 of 120



MOD_ID Settings

Voltage Levels	MOD_ID1	MOD_ID2	Description
L0 = 0V	L0	NA	TBT Config1 (with BB Retimer)
L1 = VDDD/8	L1	NA	TBT Config2 (with BB Retimer)
L2 = 2*VDDD/8	L2	NA	non-TBT Config1 (with BB Retimer)
L3 = 3*VDDD/8	L3	NA	non-TBT Config2 (with BB Retimer)
L4 = 4*VDDD/8	L4	Reserved	Reserved
L5 = 5*VDDD/8	L5	Reserved	Reserved
L6 = 6*VDDD/8	L6	Mux1: L0 - L3 Mux2: L4 - L7	non-TBT Mux1 & Mux2 Configs
L7 = 7*VDDD/8	L7	Mux3: L0 - L3 Mux4: L4 - L7	non-TBT Mux3 & Mux4 Configs

Dell TGL Platform MOD_ID Options

MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	N/A	TBT Configuration w/BB Retimer
BB8010R	L2	N/A	non-TBT Configuration w/BB Retimer
TUSB546/1046	L6	L0	TUSB546 Equalizer config #1
TUSB546/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

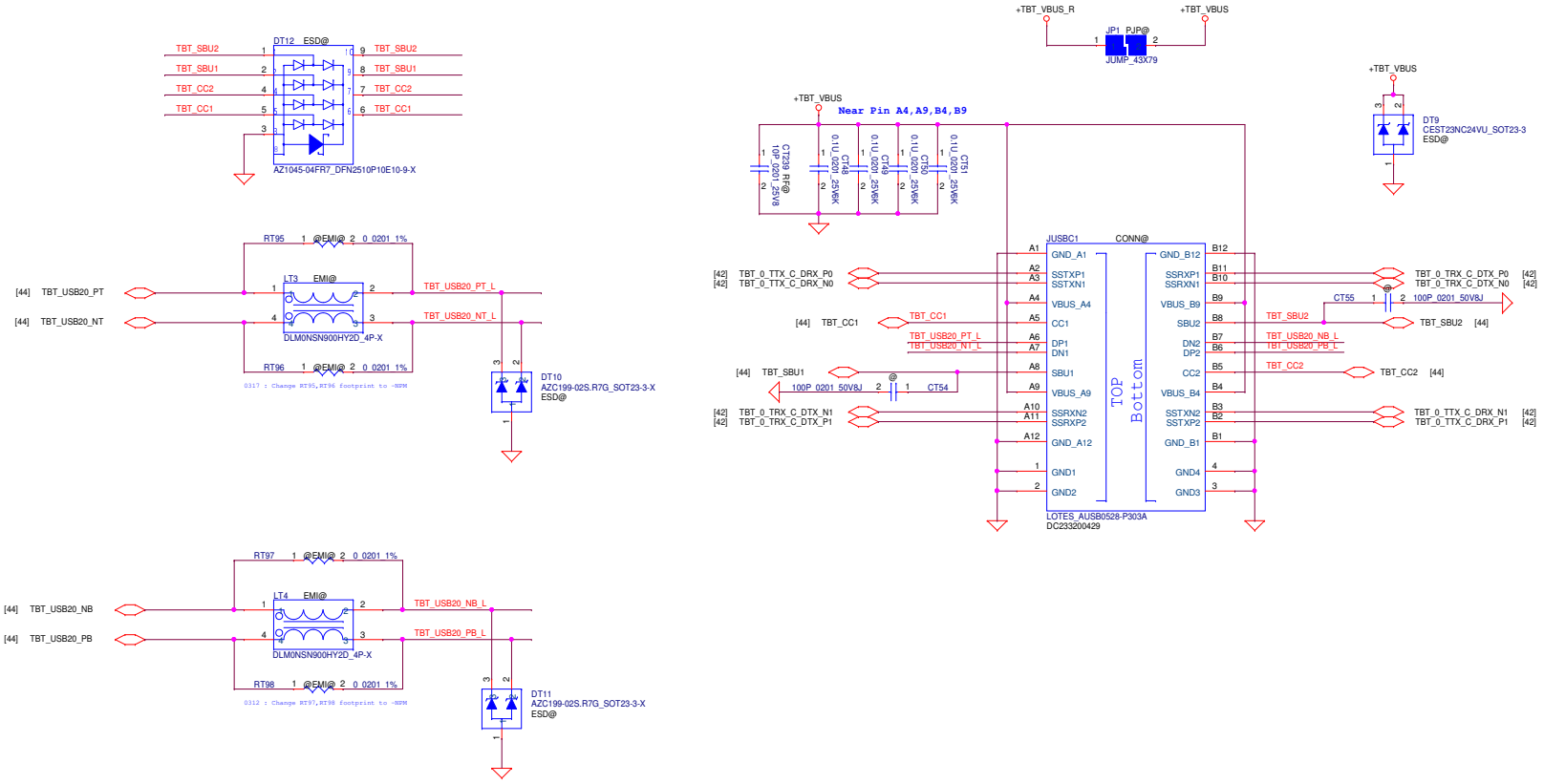
Compal Electronics, Inc.

Title: TypeC PD_CCG6SF

Size: | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 44 of 120

Main Function:



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Title: **TypeC CONN**

Size	Document Number	Rev
	LA-K452P	1.0

Date: Friday, March 19, 2021 Sheet 45 of 120

Main Function:

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 46 of 120

Main Function:

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

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Main Function:

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Date: Friday, March 19, 2021 | Sheet 48 of 120

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 49 of 120

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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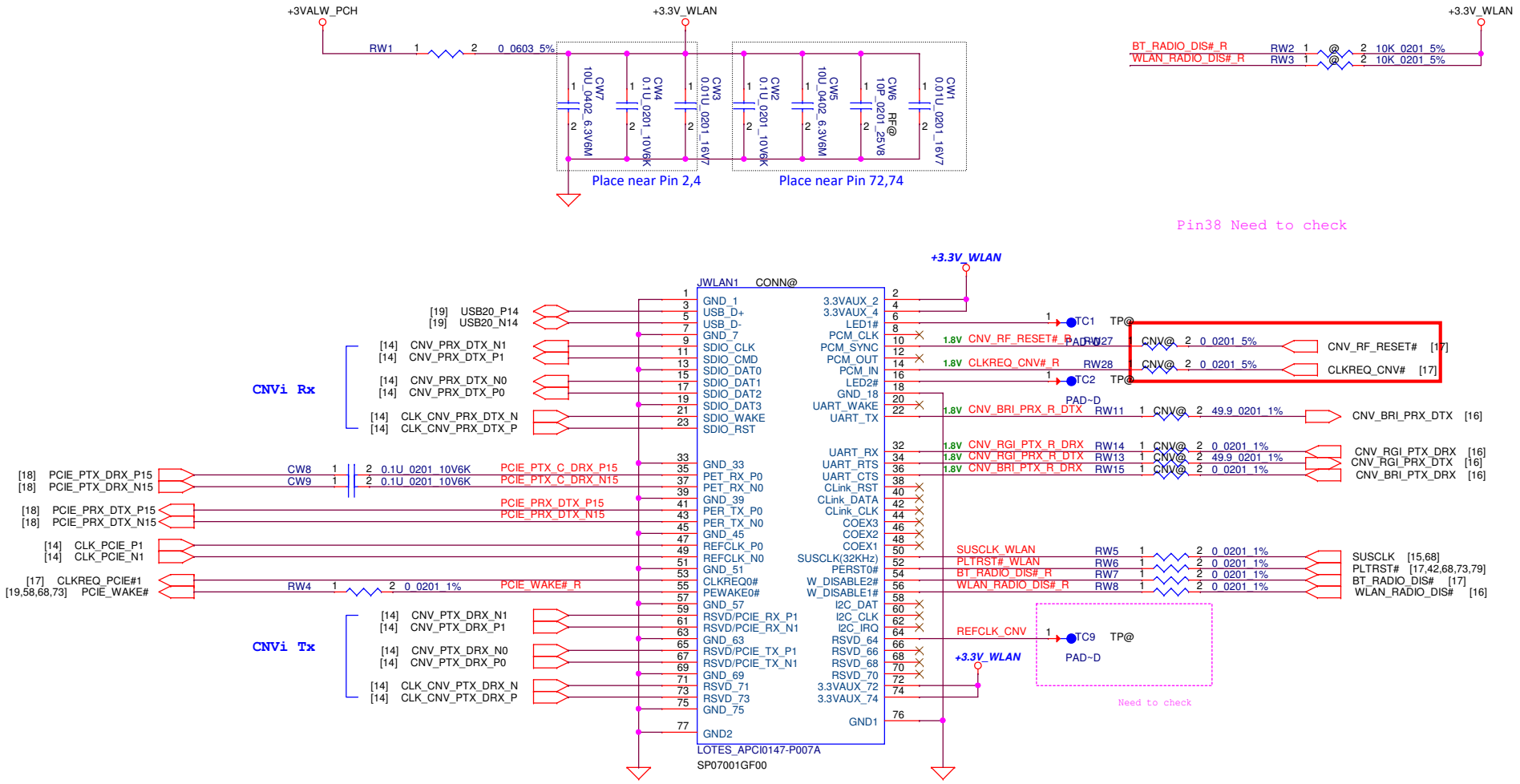
Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 51 of 120

Main Func = WLAN M.2



E Key CONN

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

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Compal Electronics, Inc.			
Title: WLAN/BT (w/ CNVi) M.2			
Size	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 52 of 120		

Main Function:

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Title: *RSV*

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Date: Friday, March 19, 2021 | Sheet 53 of 120

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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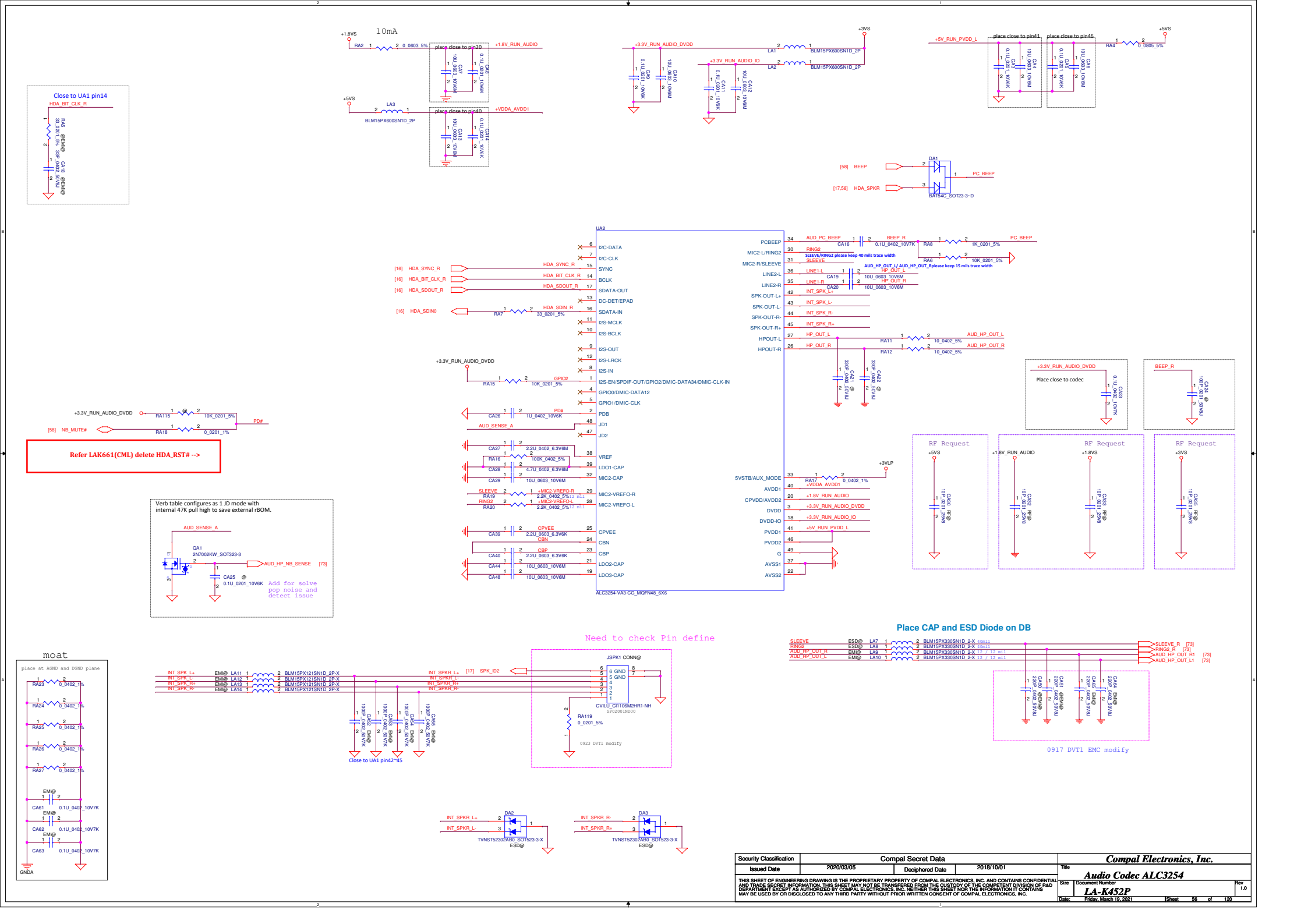
Date: Friday, March 19, 2021 | Sheet 55 of 120



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Issued Date	2020/03/05	Deciphered Date	2018/10/01

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Compal Electronics, Inc.			
Title: Audio Codec ALC3254			
Size	Document Number: LA-K452P		Rev: 1.0
Date: Friday, March 19, 2021	Sheet 56 of 120		

Main Function:

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 57 of 120

Main Func = EC

VTR3 (1.8V)

GPIO011
GPIO061
GPIO063
GPIO064
GPIO065
GPIO066
GPIO070
GPIO071
GPIO072
GPIO073

Every 0.1uF decoupling capacitor should close to designated UE1 power pin

Model ID

10K_0402_1%	17.8K_0402_1%	
SD034100280	SD034178280	
27K_0402_1%	37.4K_0402_1%	
SD034270280	SD034374280	

For Model ID Select

GN20-E4 MP	10K	GN20-P0	49.9K
GN20-E7 MP	17.8K	GN20-P1	64.9K
GN20-E5 MP	27K	N18-P	82.5K
GN20-E5 MP	37.4K		

Board ID

49.9K_0402_1%	
SD034499280	

For Board ID Select

Pre-EVT	10K
EVT	17.8K
DVT1	27.0K
DVT2	37.4K
Pilot	49.9K

9/8 DVT1 Modify

MEC1515

Group 1.8V

PCH Reserved

CR strap

BSS strap

MCU/Thermal
BATT/Charger
Touch Pad
Type C PD/EXPANDER

Close to UE1 pin A37

Close to UE1 pin A61

ESR <100m ohms

JESPI1

JDEG1

32.768KHz Oscillator

JTAG strap

Place close to JESPI1

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO170	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VTR1
GPIO104	VTR2_STRAP	Voltage Level strap is used to determine if the Shared Flash interface must be configured for 3.3V or 1.8V operation 1= 3.3V Operation 0= 1.8V Operation	VTR1
GPIO045	CR_STRAP	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Keyscan connector Note: This pin requires an external pull-up for normal operation.	VTR1
GPIO207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in EFUSE 0=Hardware Default (GPIO input) 1=Comparator 0 Enabled	VTR1
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot	VTR2
GPIO227/SHD_IO2	PWRGD_STRAP	Primary Power rails good 1 = Primary power rails are good 0 = Primary power rails not stable	VTR2

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Issued Date	2020/03/05	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: EC_MEC1515

Size: | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 58 of 126

Main Func = GPIO Expander

Control Byte

0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Write
R/W = 1 = Read
SMbus address 0x40

UE5
S IC IT8010FN/CX(R1) QFN20 EXTERNAL GPIO
SA00009VL10
SIF@

1006 DVT1 modify

[44,58,64] UPD1_SMBCLK
[44,58,64] UPD1_SMBDAT

IT8010FN-BX(R)_QFN20_4X4
SA00009VL00

9/9 DVT1 modify
9/16 DVT1 modify

PCH Reserved
Jason0720 Note-Viper-MLK
GPU_PANEL_GSYNC_EN
Connect to Page-030 GPU STRAP

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

WDT

SN74LVC1G123DCUR_VSSOP8-X

S5 LID CLOSE

10/20 DVT1 modify
SC100000S00 change to SCS00006300

IT8306FN-CX-R_QFN28_4X4

place close to UE4.14

10/20 DVT1 modify
SC100000S00 change to SCS00006300

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Issued Date	2020/03/05	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: GPIO Expander/WDT/S5 LID

Size	Document Number	Rev
	LA-K452P	1.0

Date: Friday, March 19, 2021 Sheet 59 of 120

Main Function:

Reserve

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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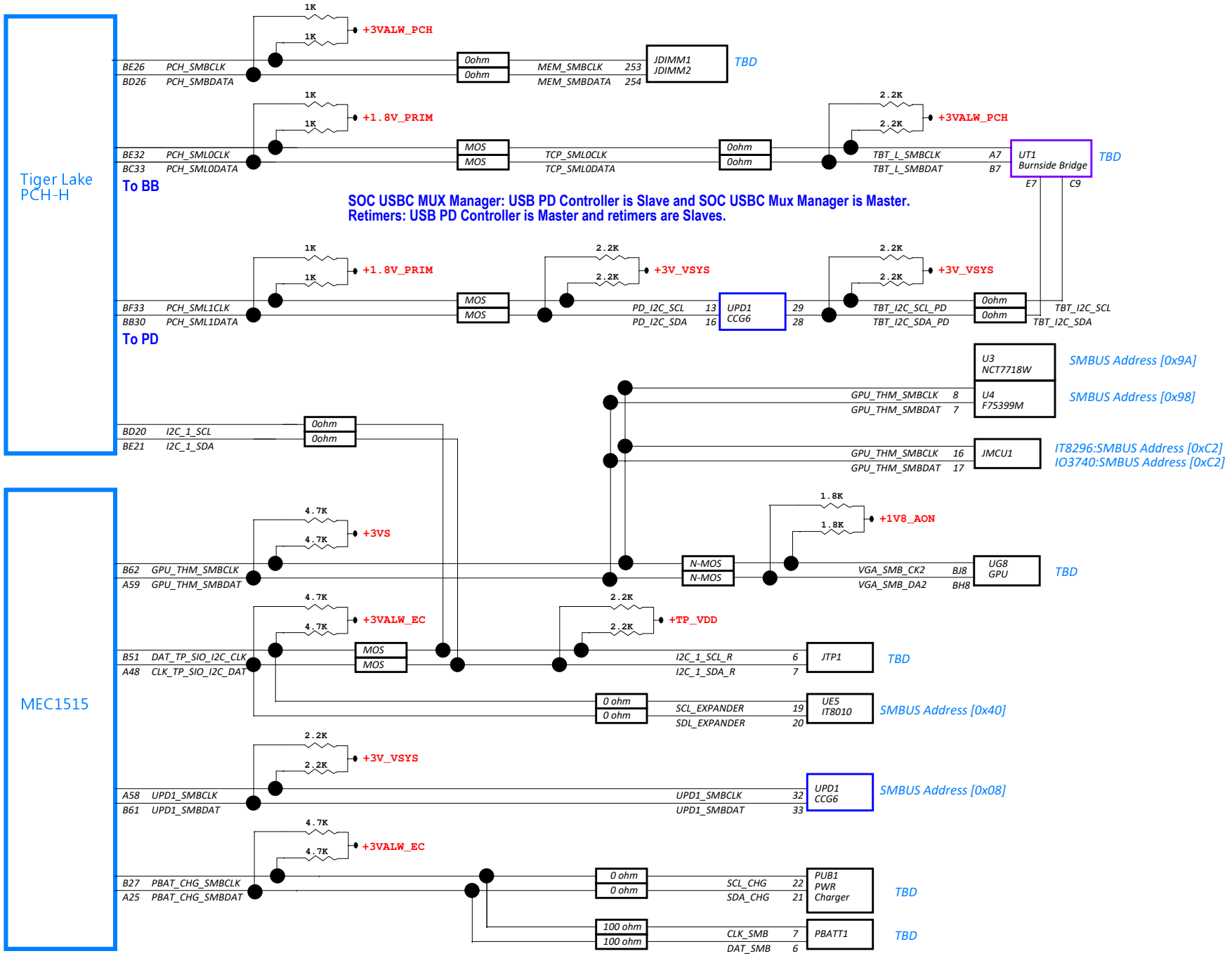
Title: *RSV*		
Size	Document Number: *LA-K452P*	Rev: 1.0
Date: Friday, March 19, 2021	Sheet 60 of 120	



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Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Title: **SMBus Block Diagram**

Size	Document Number	Rev
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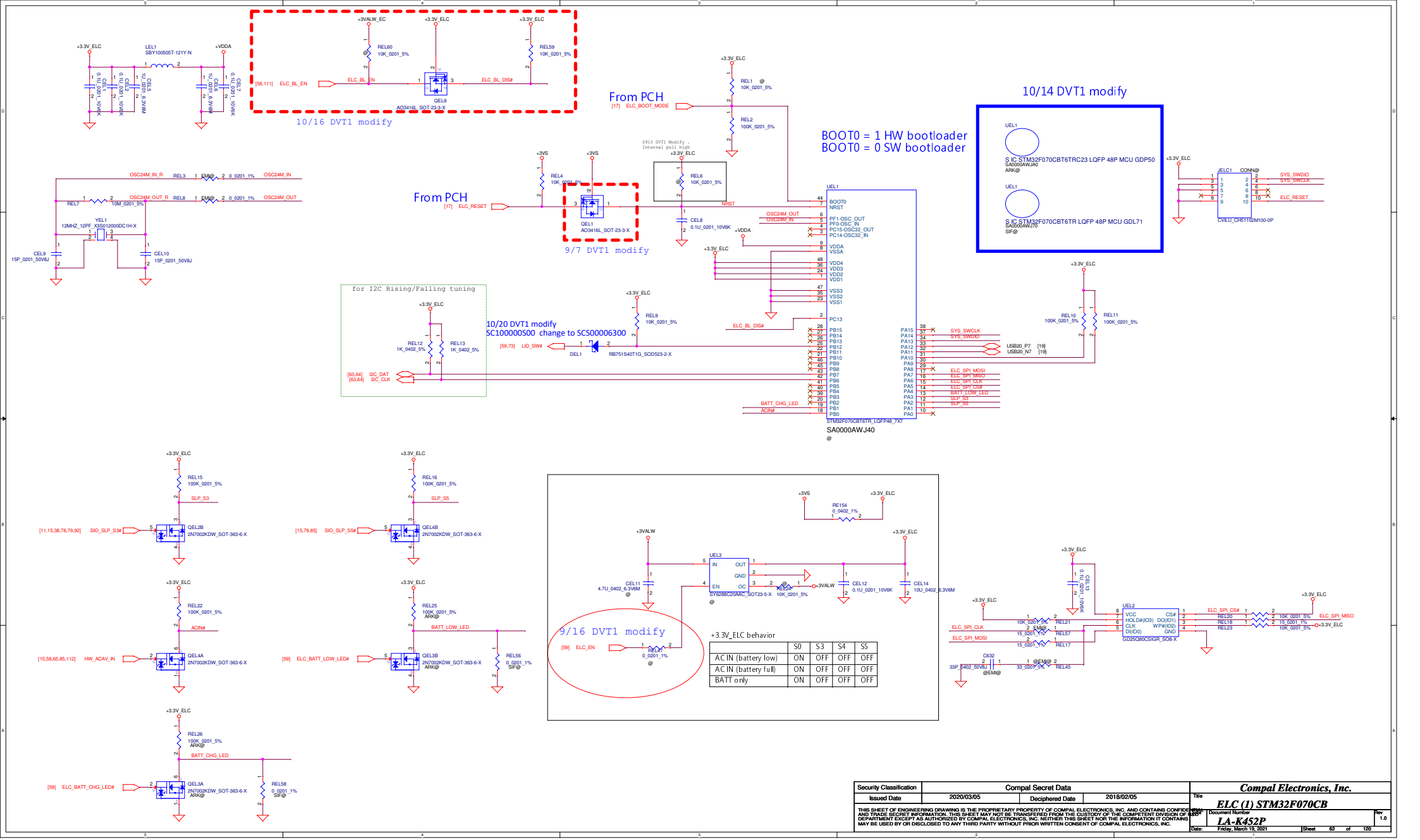
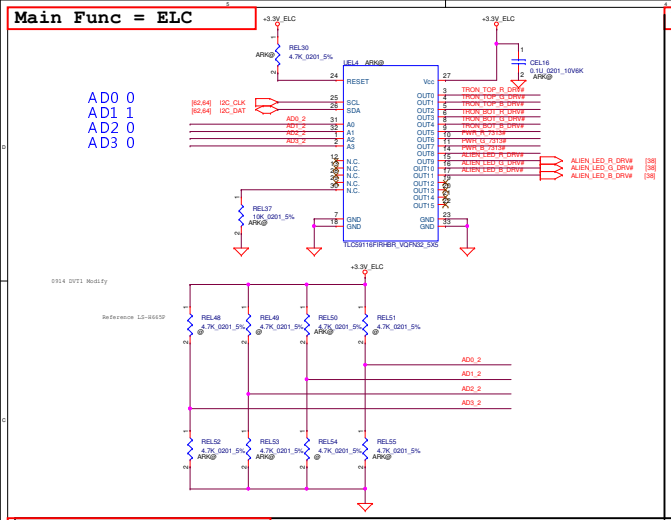
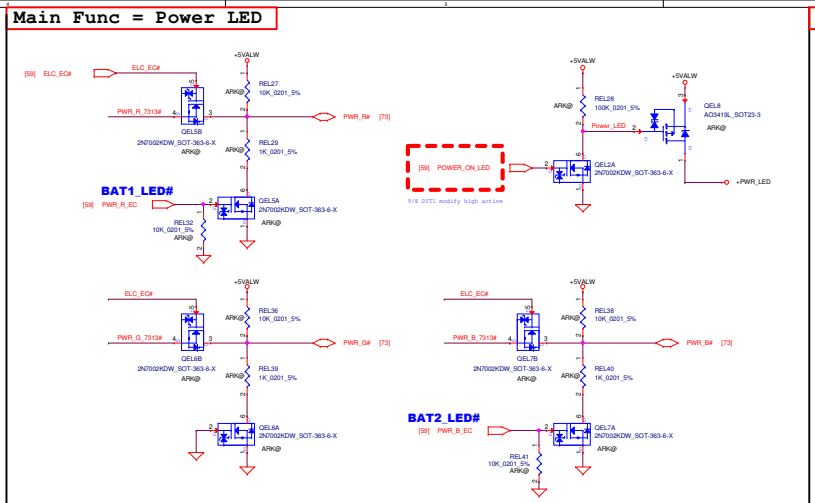

10/16 DVT1 modify
From PCH
10/14 DVT1 modify
BOOT0 = 1 HW bootloader
BOOT0 = 0 SW bootloader
9/7 DVT1 modify
for I2C Rising/Falling tuning
10/20 DVT1 modify
SC100000S00 change to SCS00006300
9/16 DVT1 modify
+3.3V_ELC behavior
S0 S3 S4 S5
AC IN (battery low) ON OFF OFF OFF
AC IN (battery full) ON OFF OFF OFF
BATT only ON OFF OFF OFF
SA0000AWJ40
SA0000AWJA0
SA0000AWJ70
Compal Electronics, Inc.
ELC (1) STM32F070CB
LA-K452P
Compal Secret Data
2020/03/05
2018/02/05
Friday, March 19, 2021

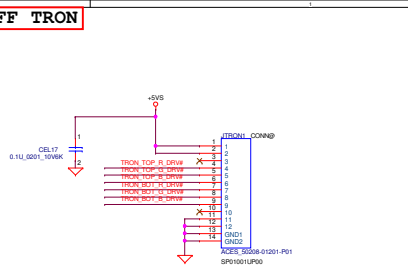
Main Func = ELC



Main Func = Power LED

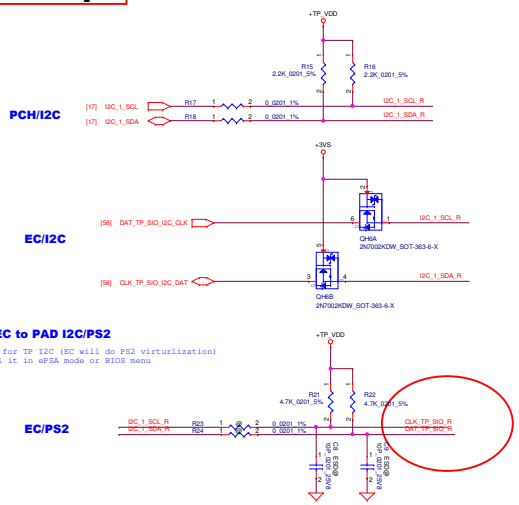


Main Func = ON/OFF TRON



ISPD SP01001UP00 and SP010020U00 are substitute

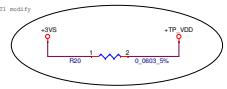
Main Func = Touch pad

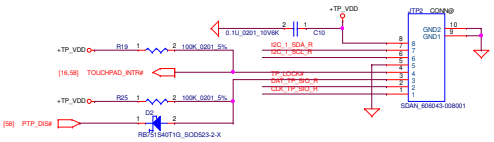


Co-lay EC to PAD I2C/PS2

it's used for TP I2C (EC will do PS2 virturlization) as control it in ePSA mode or BIOS menu

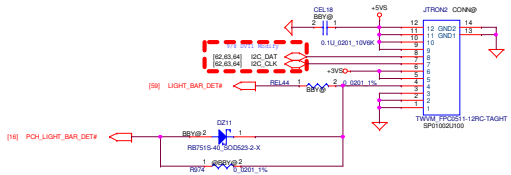
0922 DVT1 modify





10/20 DVT1 modify
SC100000S00 change to SCS00006300

Main Func = Primax Front Lighting



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/02/05	Title: ELC (2) TP/PWR/TRON

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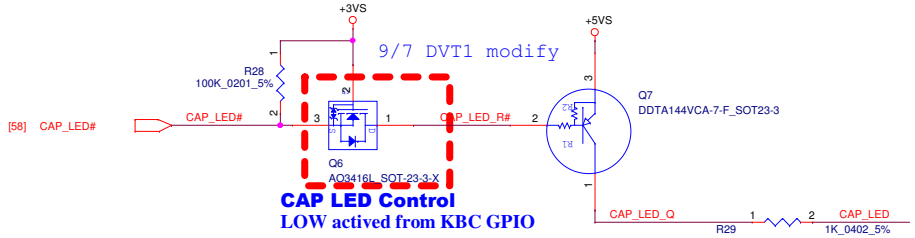
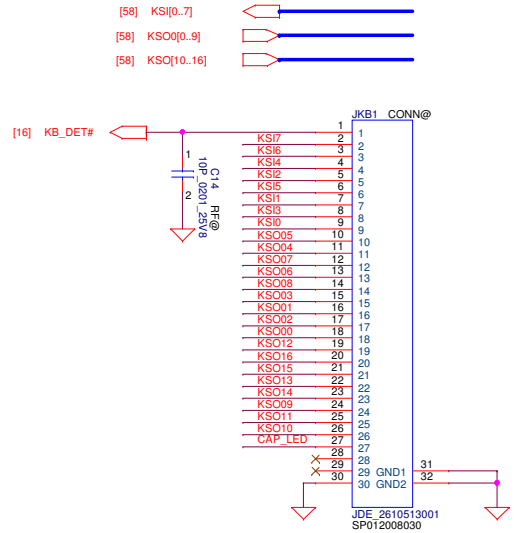
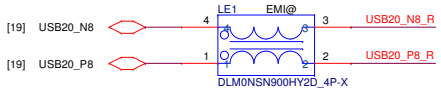
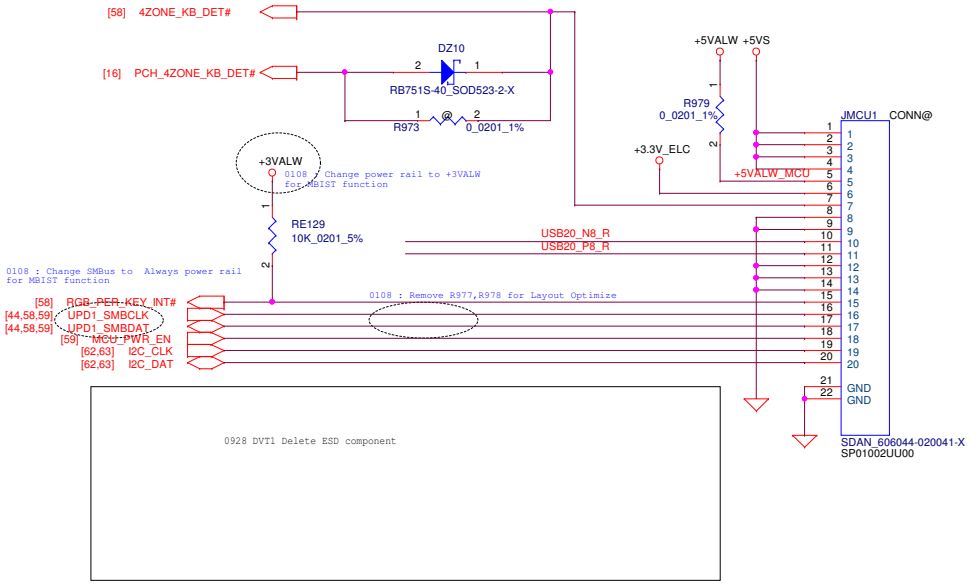
Main Func = KB/KBBL



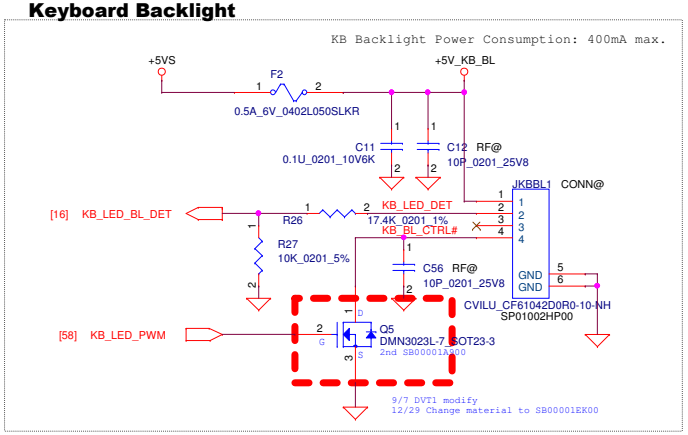




Need to confirm



Keyboard Backlight



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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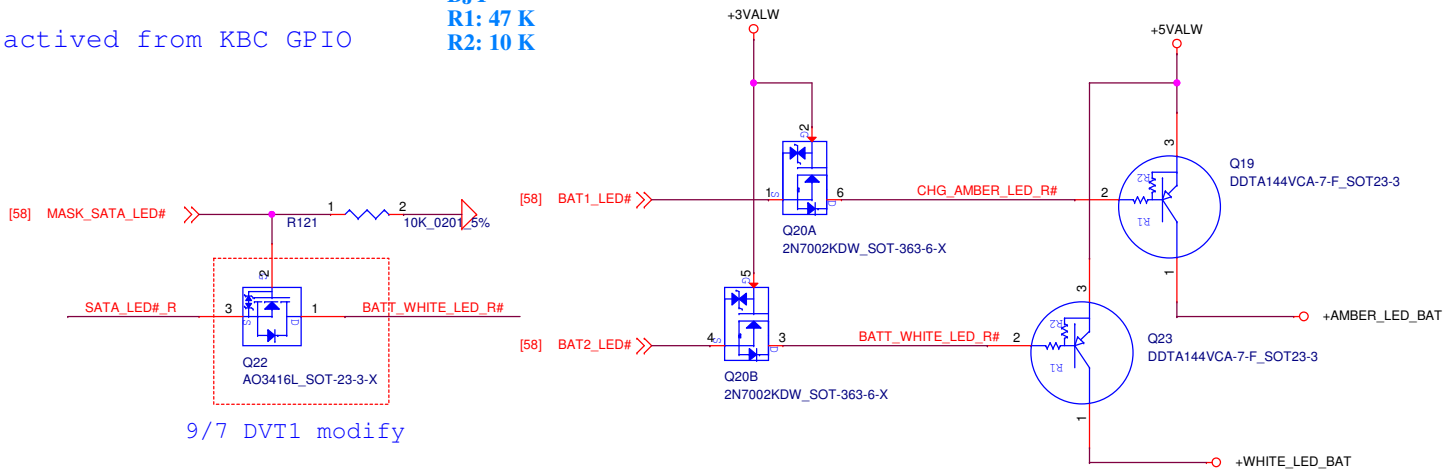
Compal Electronics, Inc.			
Title	MCU Per Key/4 Zone KB		
Size	Document Number	LA-K452P	Rev 1.0
Date:	Friday, March 19, 2021	Sheet	64 of 120

Main Func = Battery LED

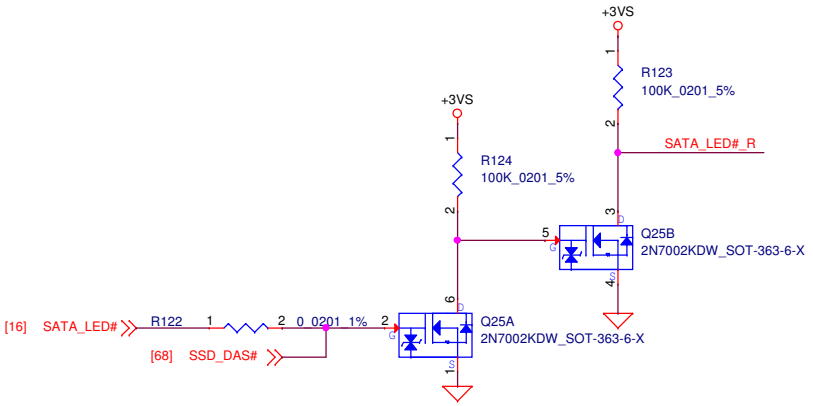
Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K

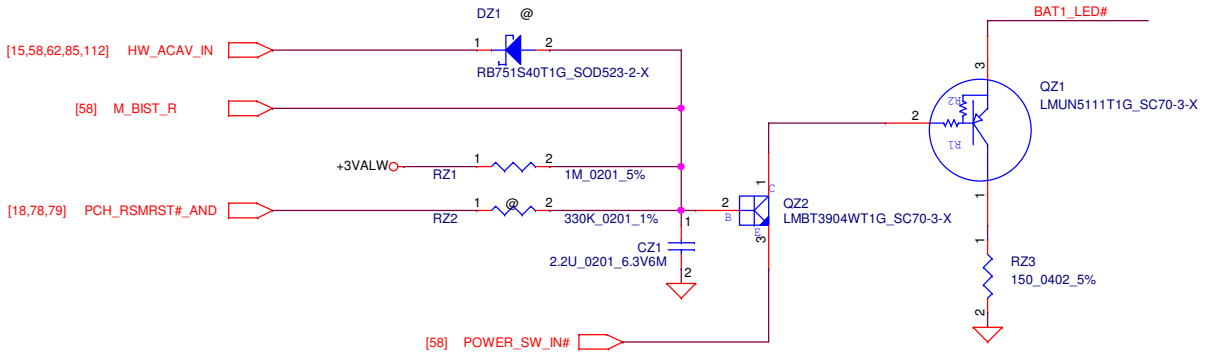


9/7 DVT1 modify

Main Func = M_BIST



10/20 DVT1 modify
SC100000S00 change to SCS00006300



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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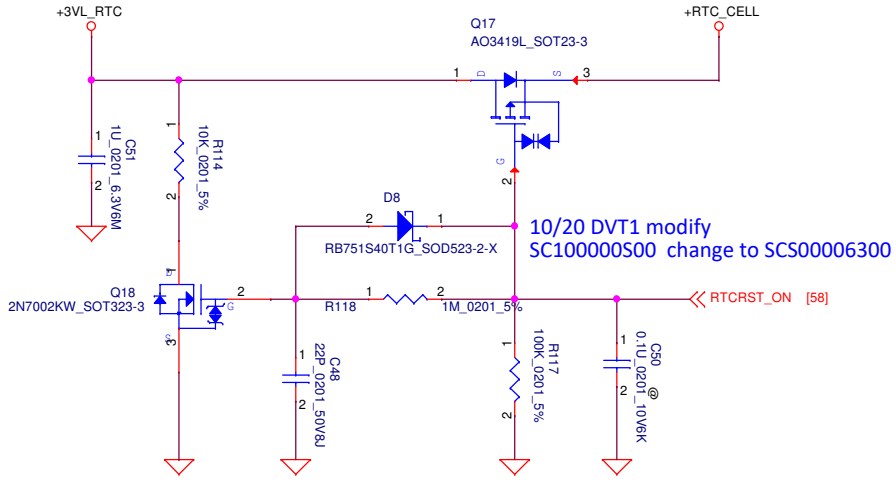
Compal Electronics, Inc.

Title: LED (SIF)

Size | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 65 of 120

Main Func = RTC Gen9



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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Compal Electronics, Inc.

Title: RTC Gen9

Size | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 66 of 120

Main Function:

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Issued Date	2020/03/05	Deciphered Date	2017/01/06

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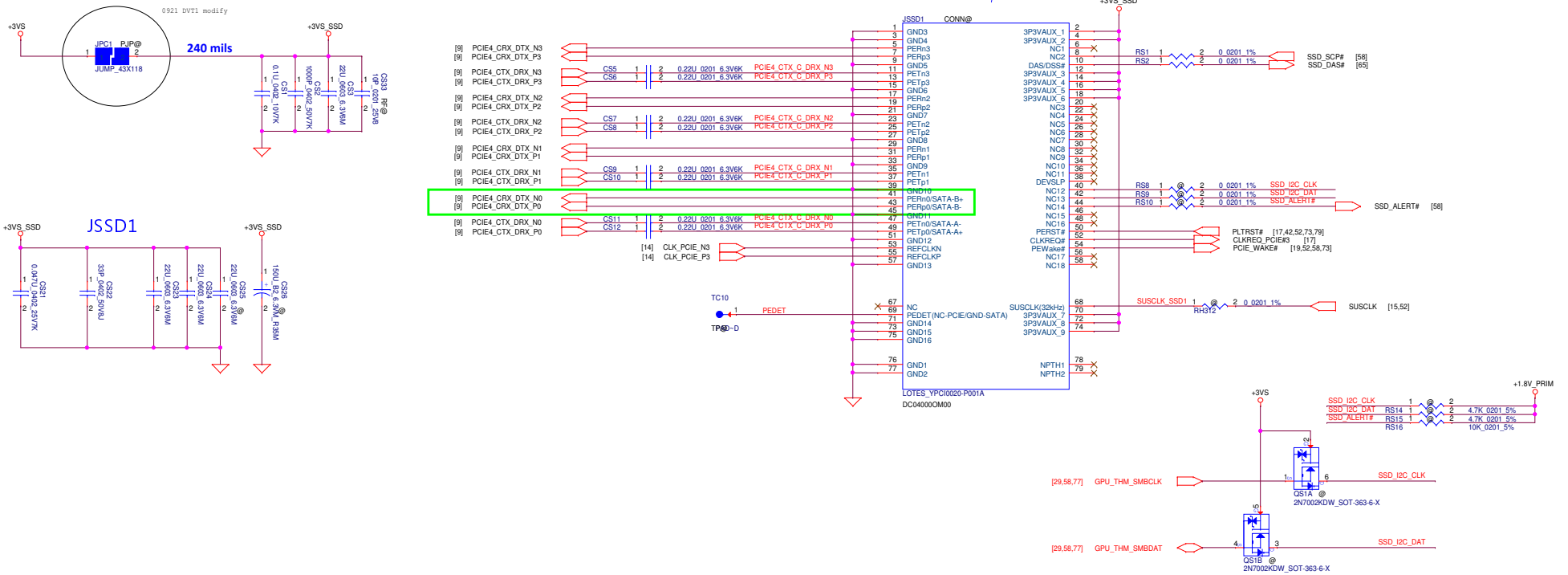
Compal Electronics, Inc.

Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 67 of 120



PEDET	Module Type
0	SATA
1	PCIe

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Compal Electronics, Inc.

Title: **NGFF SSD x2**

Size	Document Number	Rev
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Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Main Function:

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

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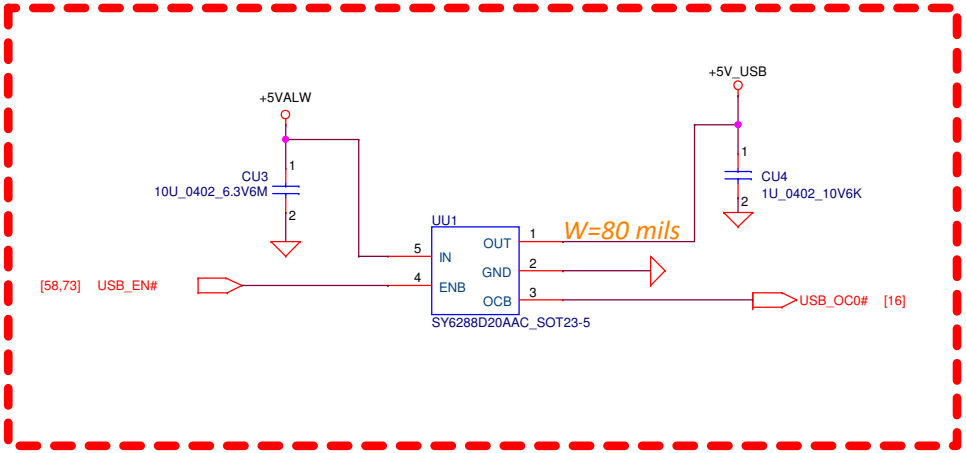
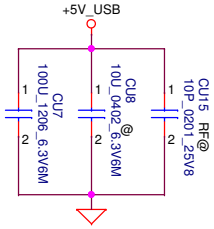
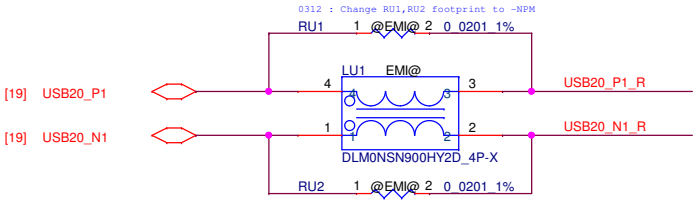
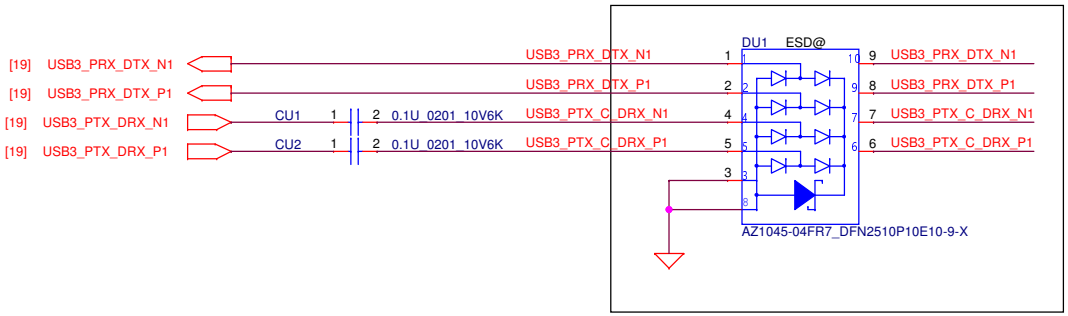
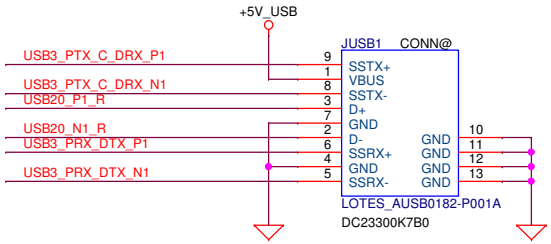


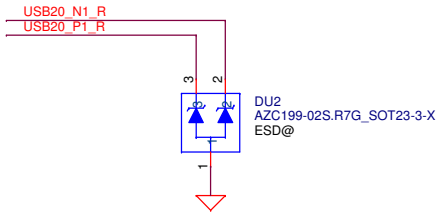


9/7 DVT1 modify









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Compal Electronics, Inc.

Title: **USB3.1 TypeA Gen1**

Size | Document Number: **LA-K452P** | Rev: 1.0

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Main Function:

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

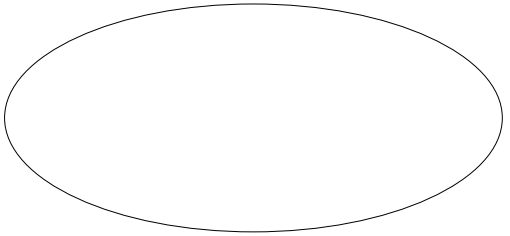
Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

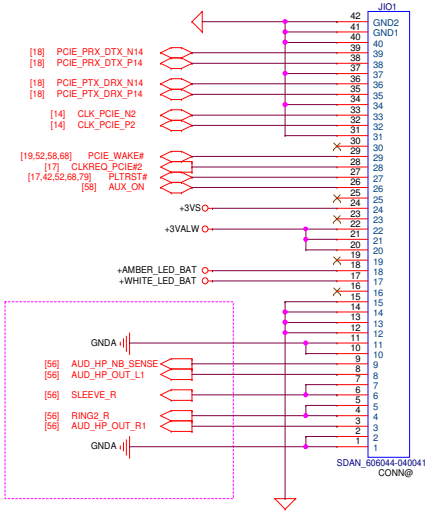
Date: Friday, March 19, 2021 | Sheet 72 of 120

Main Func = IO Board

0918 DVT1 Modify
remove PX_INX# , ALC_INT# , PX_DIS# , ISH_I2C0_SCL_R , ISH_I2C0_SDA_R 10K pull high



7/28 SWAP



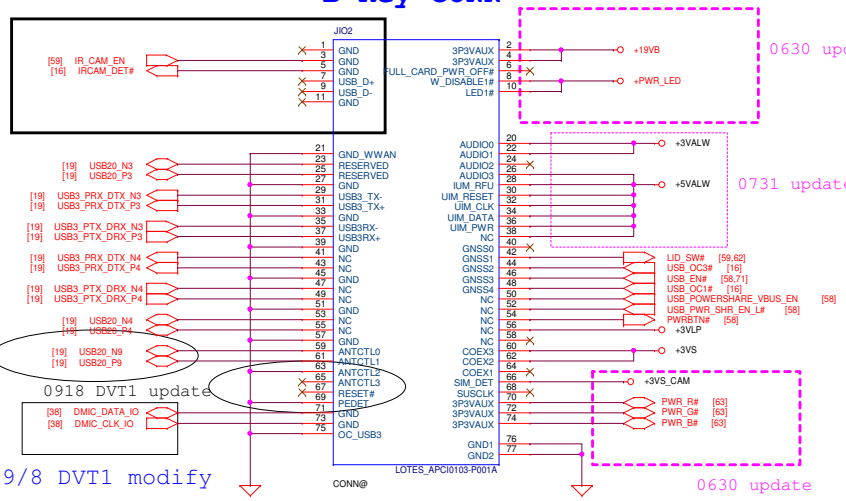
Modify 7/17

JIO1 change symbol 7/25
SP01002TO00

For LAN DB CONN

B Key CONN

0918 DVT1 update



0630 update

0731 update

9/11 DVT1 modify

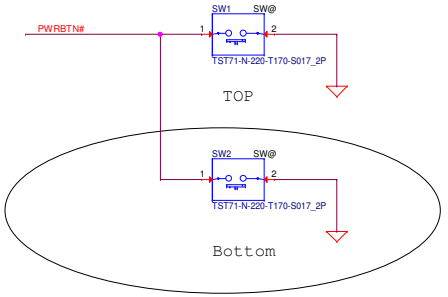
0918 DVT1 update

9/8 DVT1 modify

0630 update

For USB DB CONN

JIO2 change symbol 7/25
SP07001BL00



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Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Title	IO Board CONN		
Size	Document Number		Rev
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Date:	Friday, March 19, 2021	Sheet	73 of 120

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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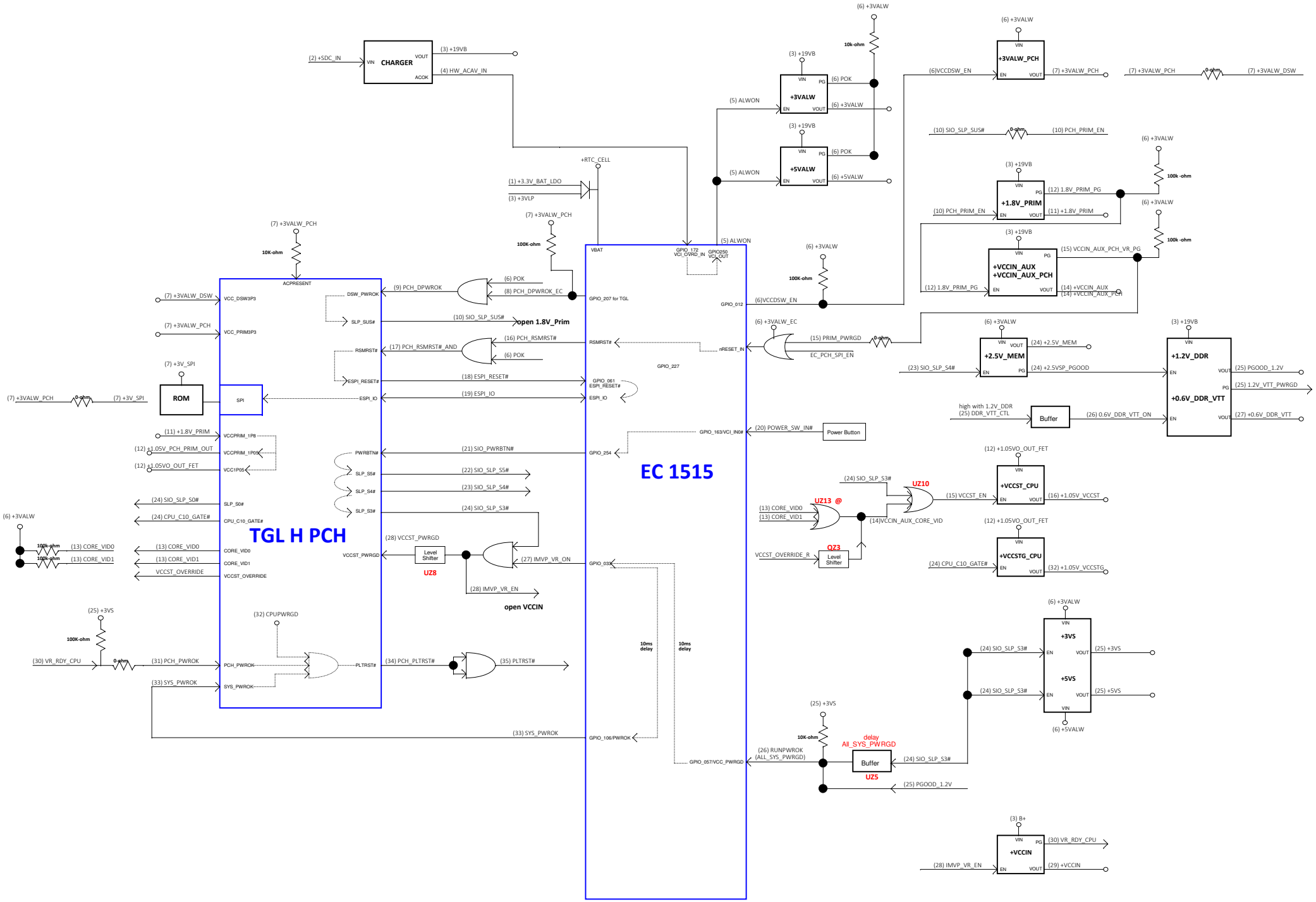
Compal Electronics, Inc.

Title: DOCK(RSVD)

Size | Document Number: LA-K452P | Rev: 1.0

Date: Friday, March 19, 2021 | Sheet 74 of 120



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title: Power Sequence Diagram
Size	Document Number		Rev
	LA-K452P		1.0
Date: Friday, March 19, 2021	Sheet 75 of 135		

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Main Function:

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: *RSV*

Size | Document Number: *LA-K452P* | Rev: 1.0

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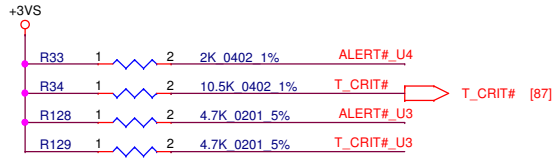
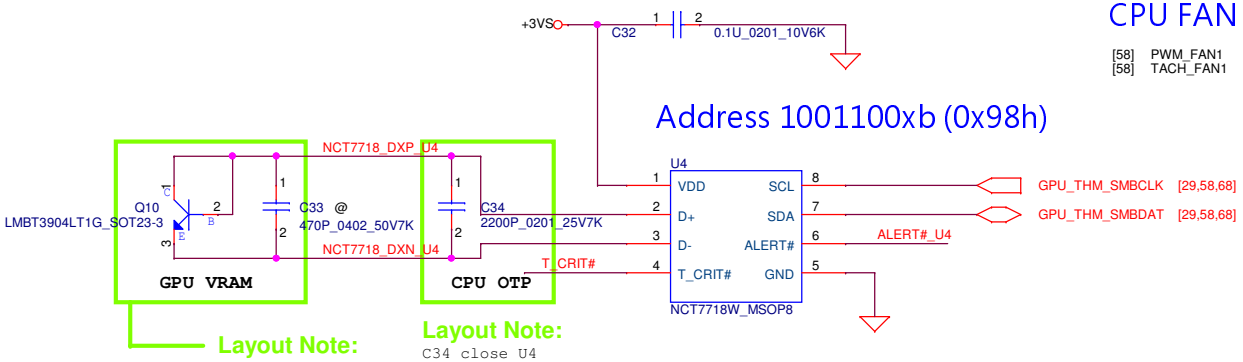
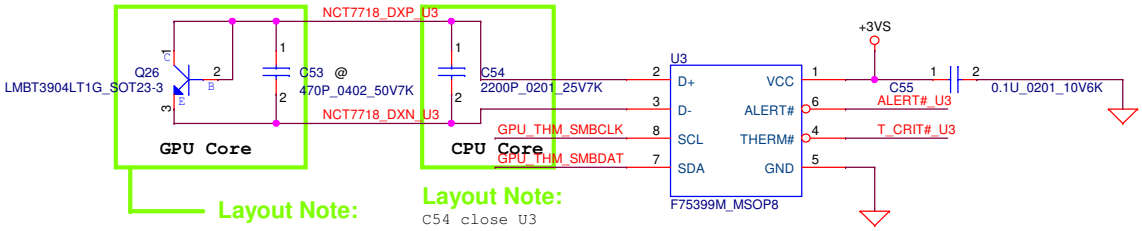




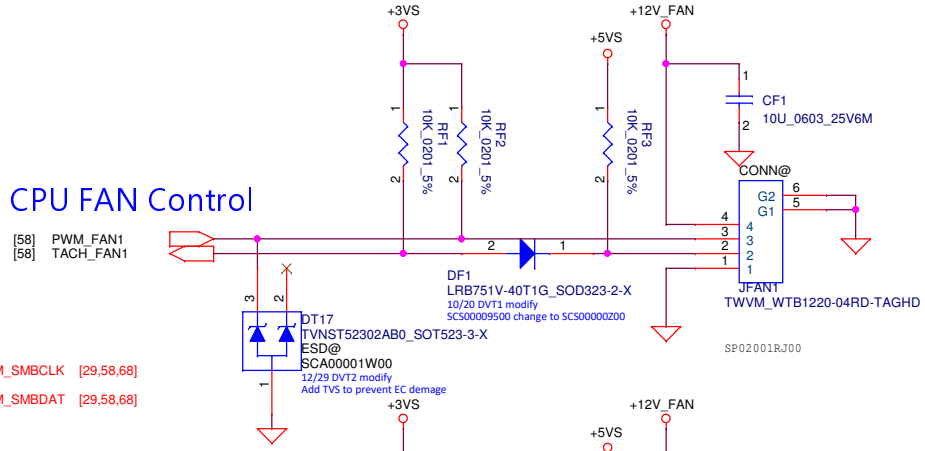
DXN and DXP routing width and spacing is 10 mil / 10 mil.



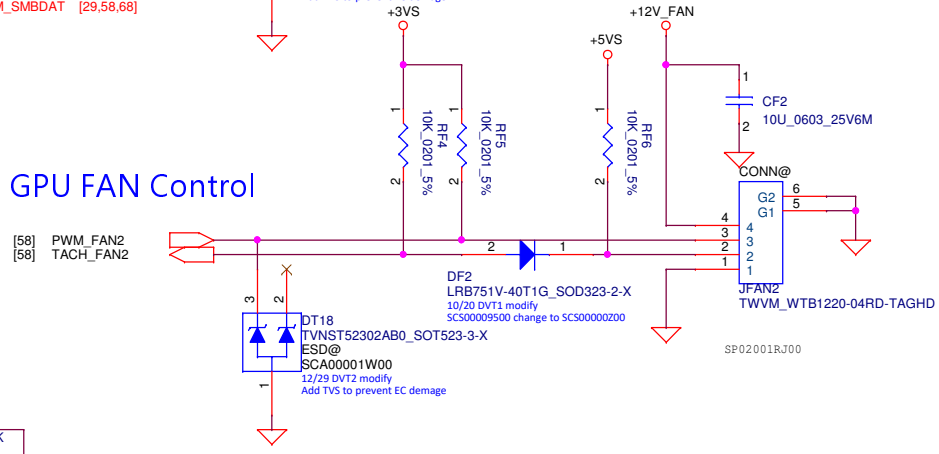
DXN and DXP routing width and spacing is 10 mil / 10 mil.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

CPU FAN Control



GPU FAN Control



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Issued Date	2020/03/05	Deciphered Date	2018/02/05	Title: FAN/Thermal
				Size: Document Number: LA-K452P Rev: 1.0
				Date: Friday, March 19, 2021 Sheet 77 of 120

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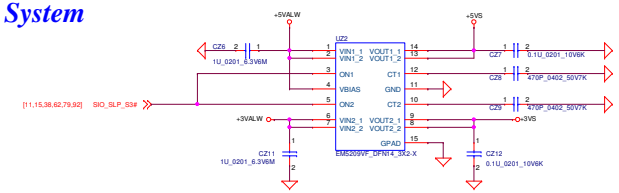
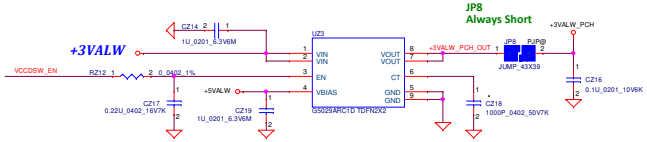
Main Func = DC/DC

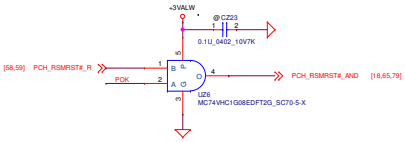
+5VS / +3VS for System



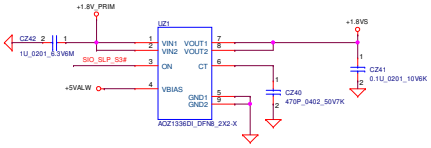
+3VALW TO +3VALW_PCH



RSMRST circuit

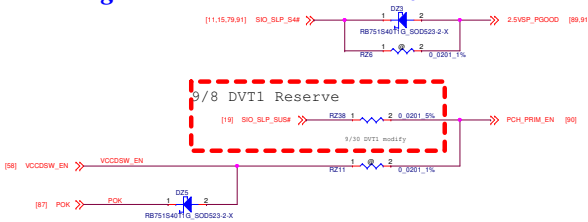


+1.8VS for System



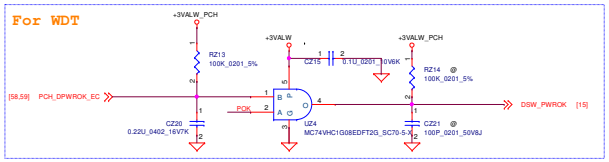
Sequence Logic

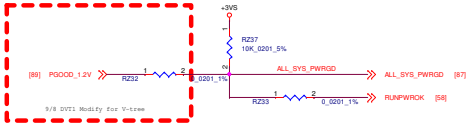
10/20 DVT1 modify
SC100000500 change to SCS00006300



10/20 DVT1 modify
SC100000500 change to SCS00006300

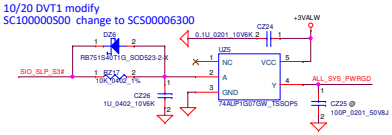
IMVP_VR_ON&VCCST_PWRGD

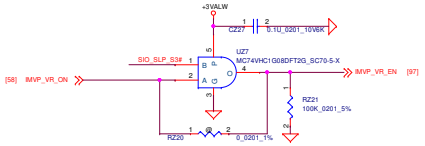




Buffer with Open Drain Output For ALL_SYS_PWRGD

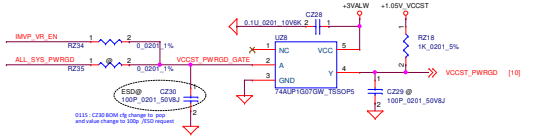
10/20 DVT1 modify
SC100000500 change to SCS00006300





10/20 DVT1 modify
SA00000OH00 change to SA0000BIP00

Buffer with Open Drain Output For H_VCCST_PWRGD



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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Compal Electronics, Inc.			
Title	DC/DC Interface		
Size	Document Number	LA-K452P	Rev 1.0
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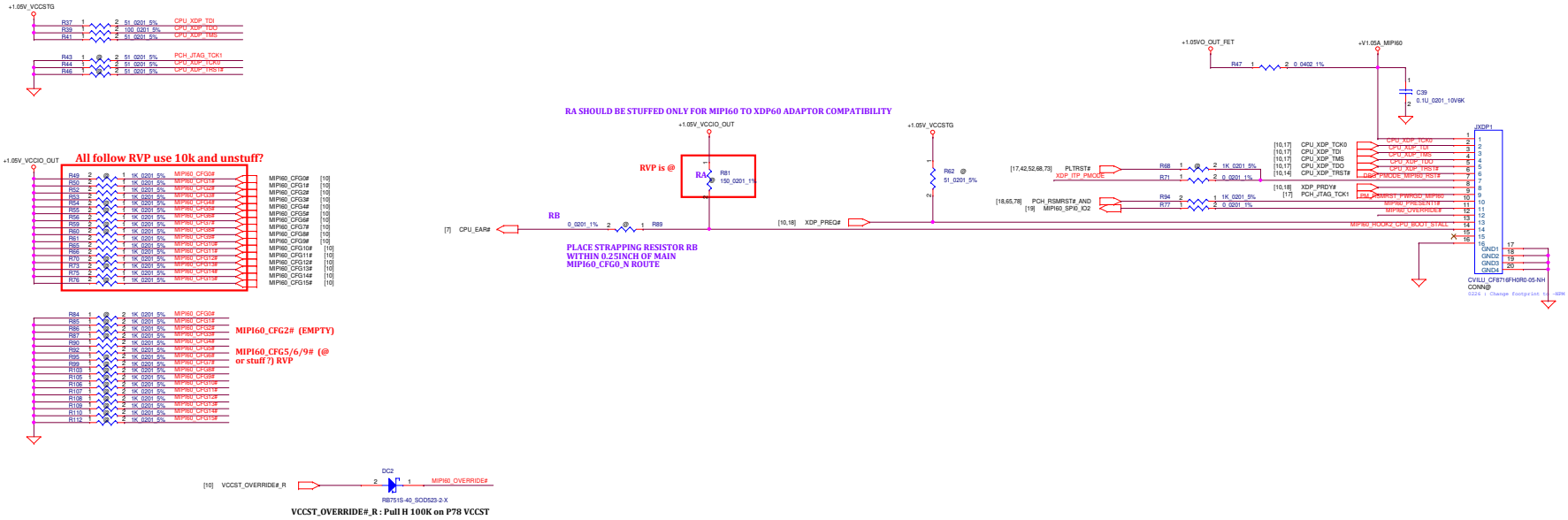
MIPI 60



Singal : CFG2
Usage : PCI express static LANE reversal for all PEG ports
LOW : LANE Reversal
HIGH : (Defailt) Normal Operation

Singal : CFG3
Usage : DFX Enabled bit in debug Interface MSR
LOW : Enable
HIGH : Disable (Default)

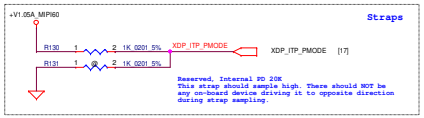
Singal : CFG4
Usage : Display port presence strap
LOW : Enable
An external display port device is connected to the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

Singal : CFG[6,5] :
Usage : PCIE Port Bifurcatin Straps
00 : Device 1 Function 1 Enabled, Device 1 Function 2 Enabled
01 : Device 1 Function 1 Disabled, Device 1 Function 2 Enabled
10 : Device 1 Function 1 Enabled, Device 1 Function 2 Disabled
11 : Device 1 Function 1, Device 1 Function 2 Disabled

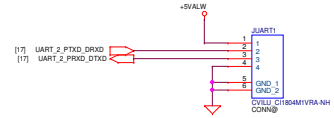
Singal : CFG7
Usage : PEG DEFER TRAINING
LOW :
PEG wair for BIOS for training
HIGH (Default) :
PEG train immediately following XXRESETB de-assertion

Singal : CFG9
Usage : No SVID Protocl Capable VR Connected
LOW : No VR supporting SVID is present.
HIGH : VRS supporting SVID protocol are present.

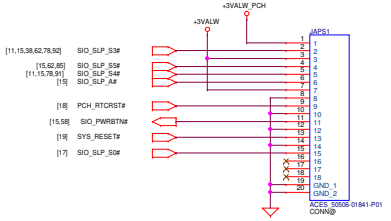
Singal : CFG14
Usage : PEG60 (PCIE4) Lanes reserver
LOW : Enable
HIGH : Disable (Default)



BIOS UART Debug



APS



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/10/01	Title: Debug APS,DEG
			Size: Document Number: LA-K452P Rev: 1.0
			Date: Friday, March 19, 2021 Sheet 79 of 120

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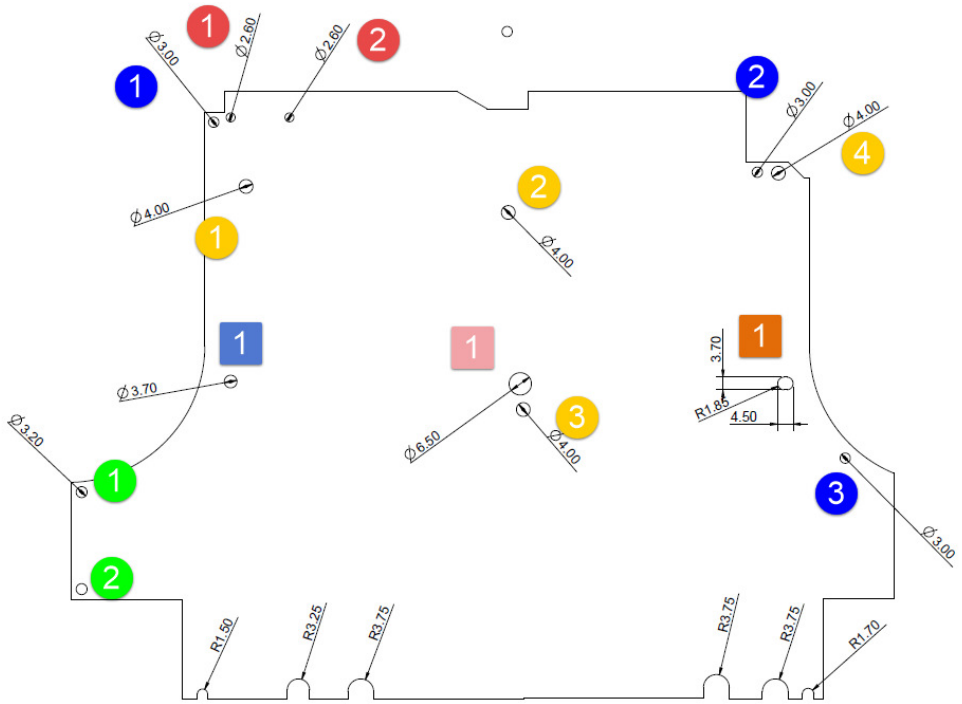

CPU & GPU

1125 DVT2 Modify change to V18D10

H1 H_4P0-G-V
H2 H_4P0-G-V
H3 H_4P0-G-V
H4 H_4P0-G-V
H5 H_4P5X3P7
H6 H_3P7-G-V

1125 DVT2 Modify change to V18D10

SHIELDING CASE

CLIP1
CLIP_10P2X7P2_SHIELDING_CASE1
EC26M000600
@

PTH

1125 DVT2 Modify change to V18D10

H7 H_2P1-G-V
H8 H_2P5-G-V
H9 H_3P0-G-V
H10 H_3P0-G-V
H18 H_2P4-G-V
H11 H_2P6-G-V
H12 H_2P6-G-V
H13 H_2P6-G-V
H14 H_2P6-G-V

1124 DVT2 Modify

NPTH

H19 H_2P1N

0105 : Add NPTH hole

Stand-off

H15 H_3P3
H16 H_3P3

0914 DVT1 Modify

Fiducial Mark

FD1 @FIDUCIAL
FD2 @FIDUCIAL
FD3 @FIDUCIAL
FD4 @FIDUCIAL
FD5 @FIDUCIAL
FD6 @FIDUCIAL

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Compal Electronics, Inc.

Title: Screw Hole

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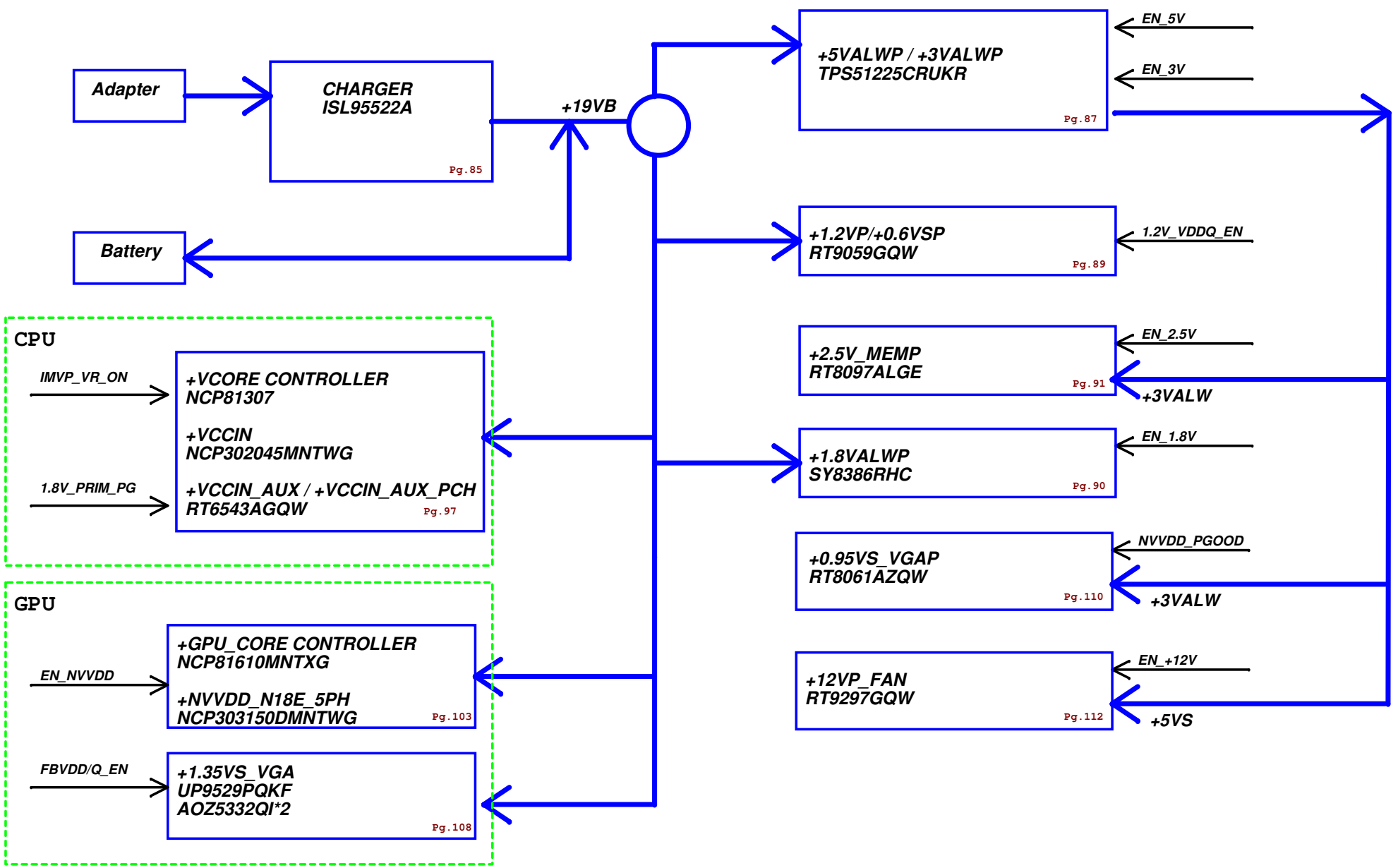
Date: Friday, March 19, 2021 | Sheet 80 of 120

Power block



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/08/01

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Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Document Number: LA-K452P

Rev: 0.1

Date: Friday, March 19, 2021

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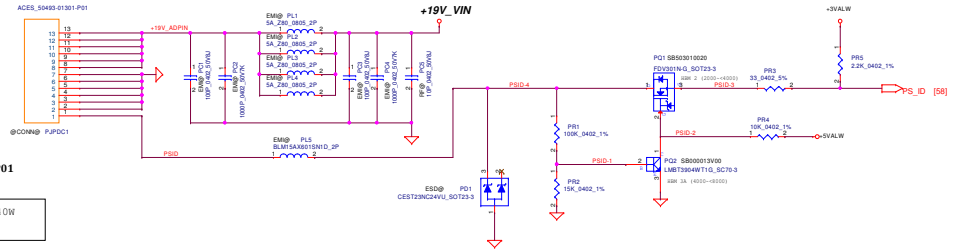
Main Func = DCIN CONN

Adapter Connector

Adapter Bot Side

PIN1 PSID
PIN2 GND
PIN3 GND
PIN4 GND
PIN5 GND
PIN6 GND
PIN7 GND
PIN8 ADPIN
PIN9 ADPIN
PIN10 ADPIN
PIN11 ADPIN
PIN12 ADPIN
PIN13 ADPIN
ACES_50493-01301-P01

Adapter 180W / 240W
240W/19V=12.63A



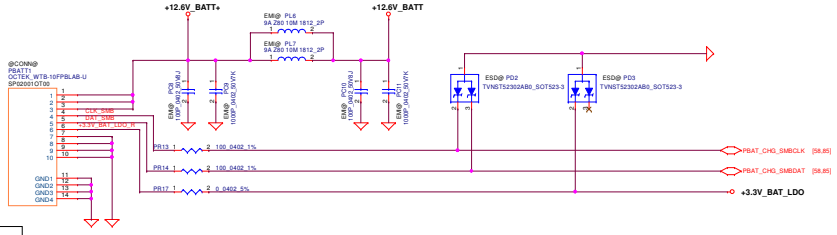
Main Func = BATT CONN

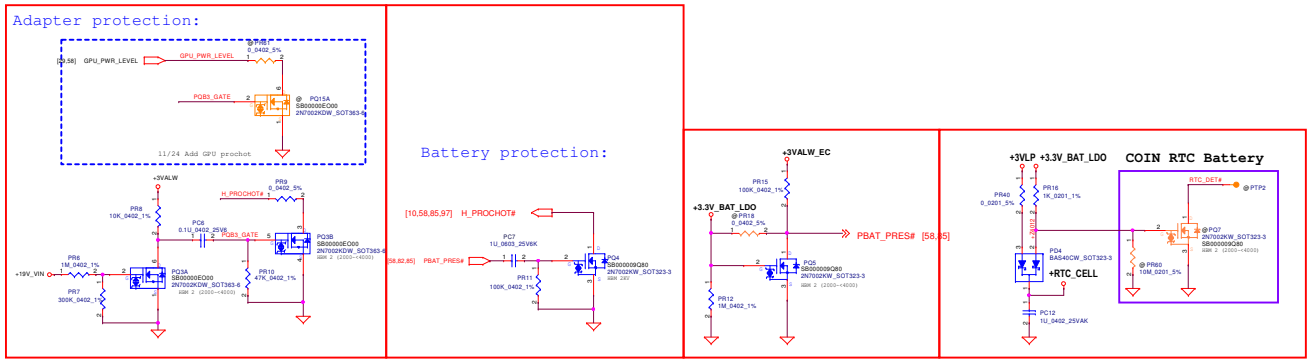
Battery Connector

Battery Bot Side

PIN10 GND
PIN09 GND
PIN08 GND
PIN07 SYS_PRES#
PIN06 BATT_PRS#
PIN05 DAT_SMB
PIN04 CLK_SMB
PIN03 BATT+
PIN02 BATT+
PIN01 BATT+
SP07001R500

Battery 56W
56W/11.4V=4.91A
Battery 86W
86W/11.4V=7.54A





Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.			
Title	PWR-DCIN / OTP / BATT CONN / RTC		
Size	Document Number		Rev 0.1
	LA-K452P		
Date: Friday, March 19, 2021	Sheet 82 of 120		

Reserve

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR-Reserve

Size | Document Number: LA-K452P | Rev: 0.1

Date: Friday, March 19, 2021 | Sheet 83 of 120

Reserve

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR-Reserve

Size | Document Number: LA-K452P | Rev: 0.1

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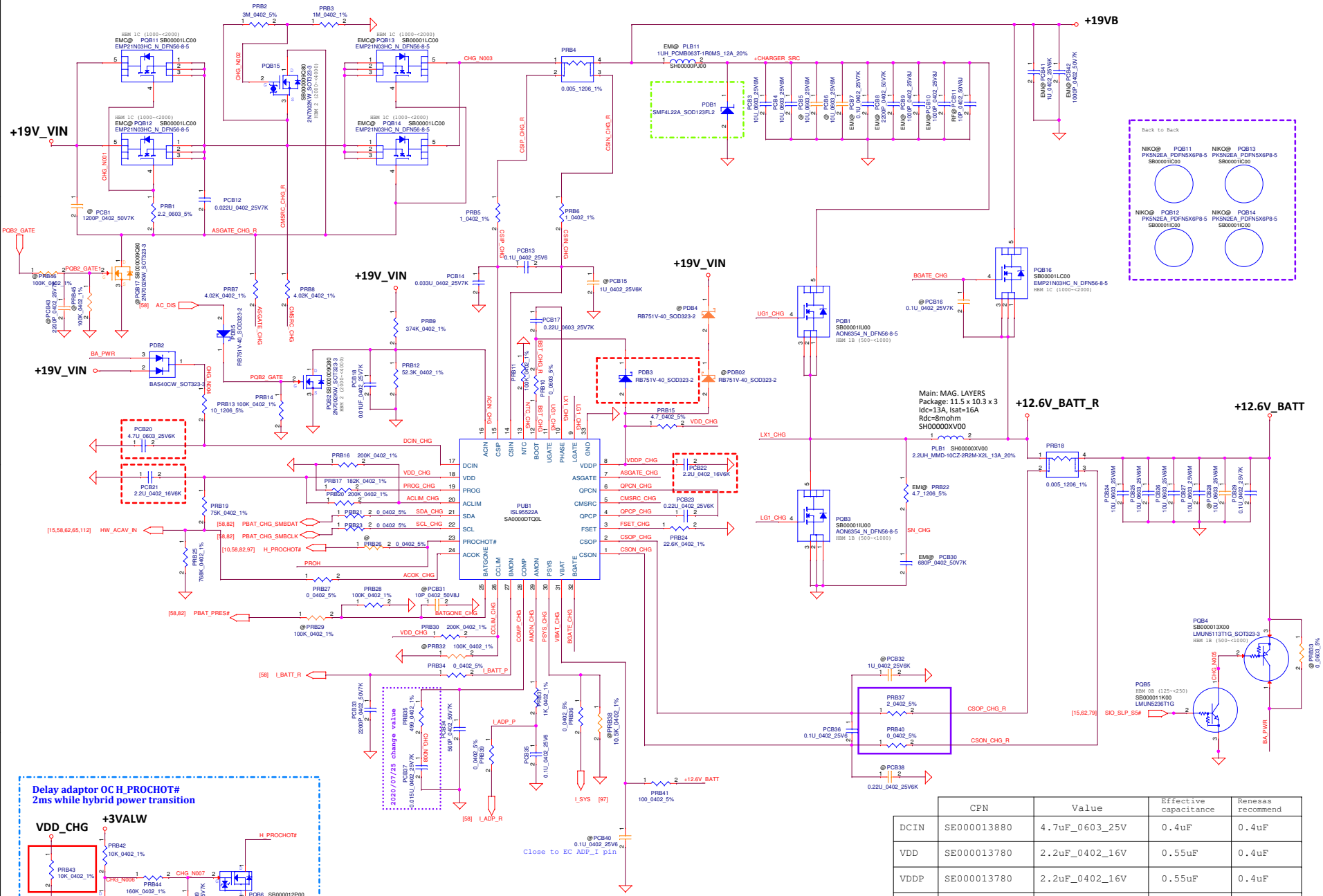
Main Func = CHARGER



	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: PWR_CHARGER

Size: | Document Number: LA-K452P | Rev: 0.1

Date: Friday, March 19, 2021 | Sheet 85 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title

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Main Func = 3.3VALWP / 5VALWP

3.3VALWP
Vout=3.4V
TDC 9.7A
Peak Current 13.7A(0.95V include)
OCP current A
OVP=3.824V~3.994V(112.5%~117.5%)
UVP=1.869V~2.209V(55%~65%)
FSW=355kHz

MOS (VGS = 4.5V)

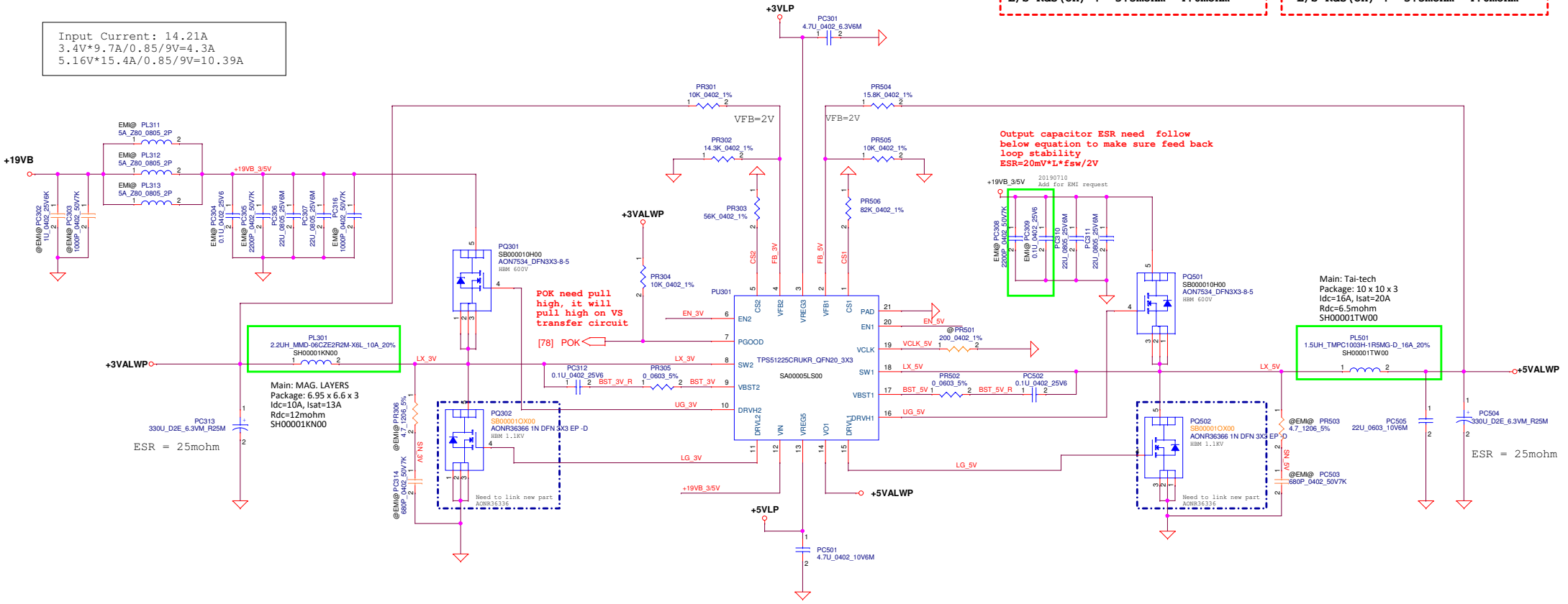
	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	3.5mohm	4.6mohm

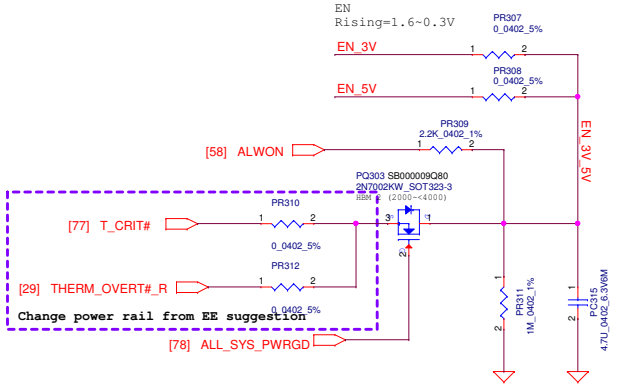
5VALWP
Vout= 5.16V
TDC =15.4A
Peak Current 18.48A
OCP current A
OVP=5.805V~6.063V(112.5%~117.5%)
UVP=2.838V~3.354V(55%~65%)
FSW=300kHz

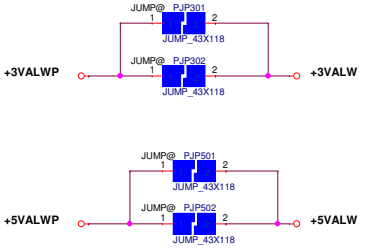
MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	3.5mohm	4.6mohm

Input Current: 14.21A
3.4V*9.7A/0.85/9V=4.3A
5.16V*15.4A/0.85/9V=10.39A







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/12/31	Title: PWR_+3.3VALWP/+5VALWP
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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.			
Title			
Size	Document Number		Rev 0.1
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Main Func = 1.2VP / 0.6VSP / 2.5V_MEMP

Input Current: 1.012A

1.203V*5.92A/0.85/9V=0.93A

0.6V*1.05A/0.85/9V=0.082A

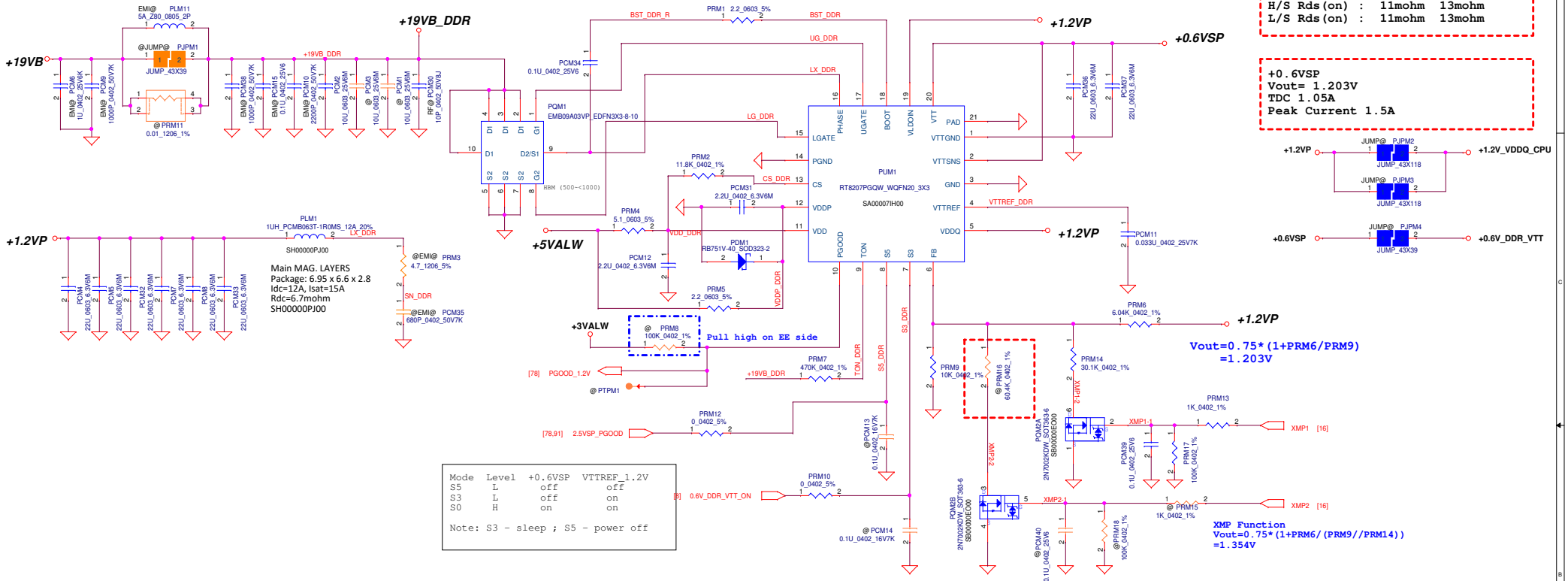
+1.2VP
Vout= 1.203V
TDC 5.92A
Peak Current 8.46A
OCP current 10.12A
OVP=1.36V~1.44V(113%~120%)
UVP=0.72V~0.96V(60%~80%)
FSW= ~538 Hz

MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	11mohm	13mohm
L/S Rds(on) :	11mohm	13mohm

+0.6VSP
Vout= 1.203V
TDC 1.05A
Peak Current 1.5A

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title: PWR_1.2VP/0.6VSP/+2.5V

Size | Document Number: LA-K452P | Rev: 0.1

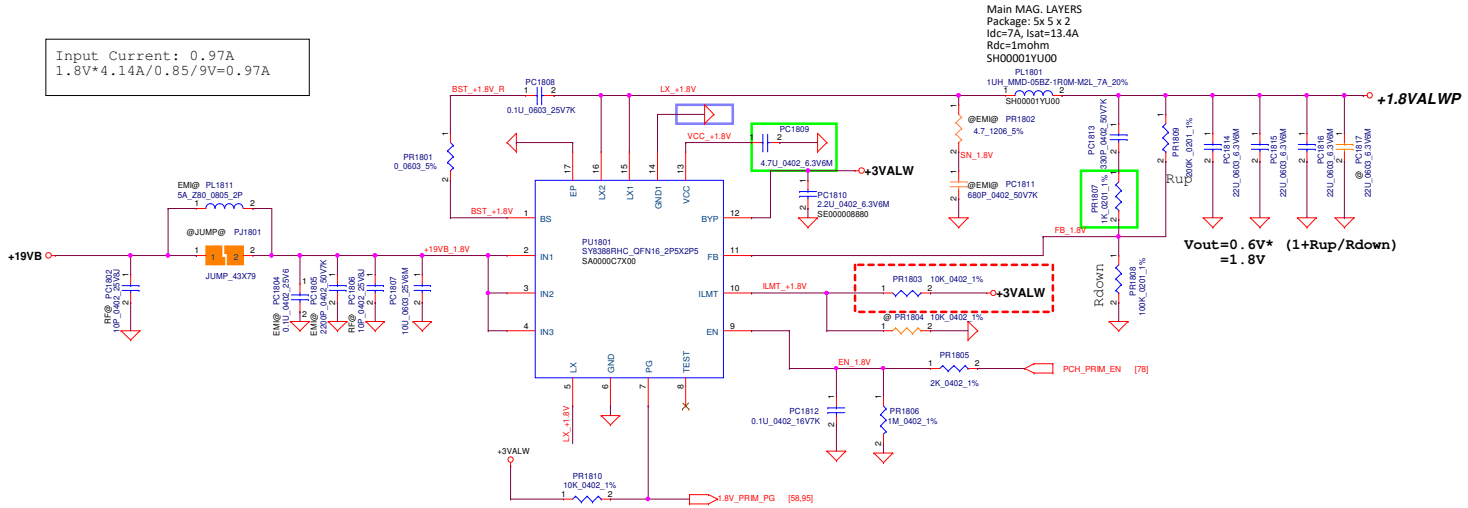
Date: Friday, March 19, 2021 | Sheet 89 of 120

Main Func = 1.8VALWP

Input Current: 0.97A
1.8V*4.14A/0.85/9V=0.97A

Main MAG. LAYERS
Package: 5x 5 x 2
Idc=7A, Isat=13.4A
Rdc=1mohm
SH00001YU00

+1.8VALWP
TDC = 7.049A
Peak Current = 9.505 A
OVP=2.106V~2.214V(117%~123%)
OCP=12A
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz



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Issued Date	2020/03/05	Deciphered Date 2021/08/01	Title: PWR-+1.8V
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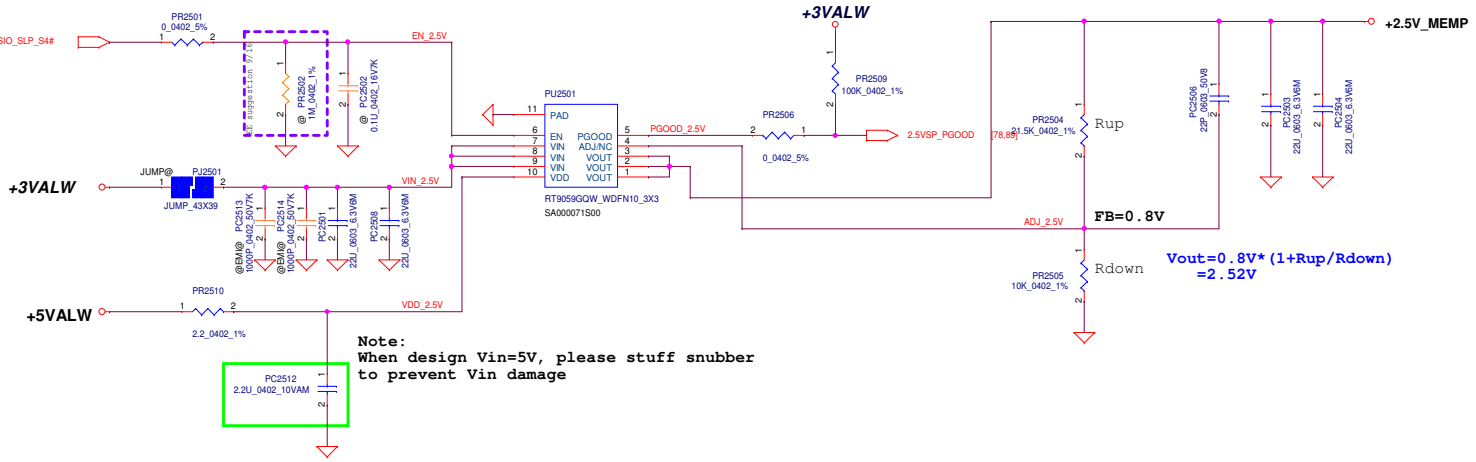
			Date: Friday, March 19, 2021 Sheet 90 of 120

Main Func =2.5V_MEMP

Input Current: 0.12A

2.52V*0.37A/0.85/3V=0.366A



+2.5V_MEMP
Vout= 2.52 V
TDC 0.37 A
Peak Current 0.528 A
Current limit 3.6A

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.			
Title	PWR_1.2VP/0.6VSP/+2.5V		
Size	Document Number		Rev
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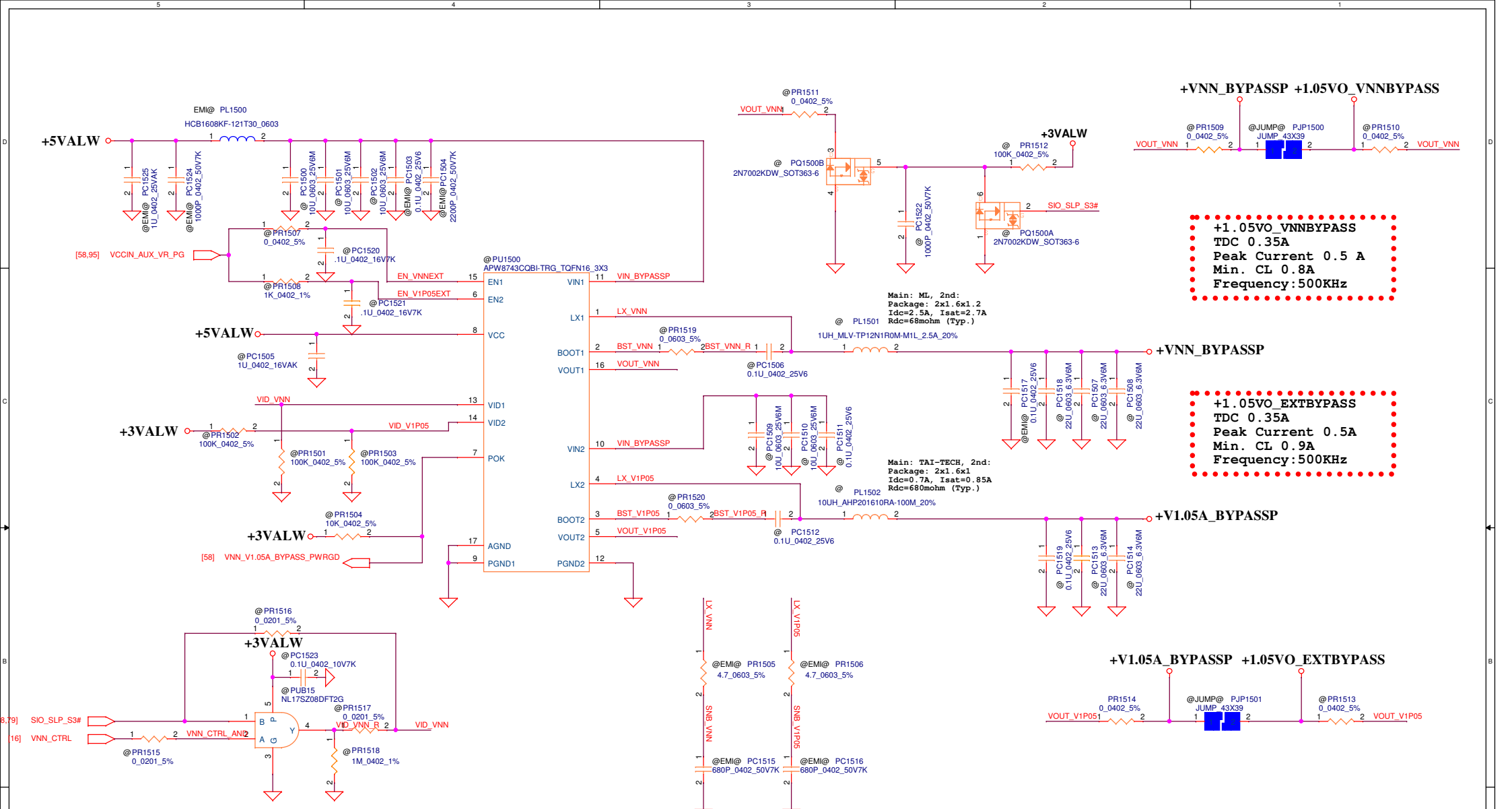
Date:	Friday, March 19, 2021	Sheet 91 of 120	



Part Number	VID=0(VNN)	VID=1(VNN)	VID=0(V1P05A)	VID=1(V1P05A)
APW8743CQBI(QBGI)	1.05V	0.78V	1.05V	0.96V
APW8743DQBI(QBGI)	0.78V	0.7V	1.05V	0.96V
APW8743EQBI(QBGI)	1.05V	0.7V	1.05V	0.96V

Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

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Title: PWR_BYPASS (APW8743C)

Size | Document Number: LA-K471P | Rev: 0.1

Date: Friday, March 19, 2021 | Sheet 92 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Title			
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Date: Friday, March 19, 2021		Sheet 93 of 120	

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K452P	0.1

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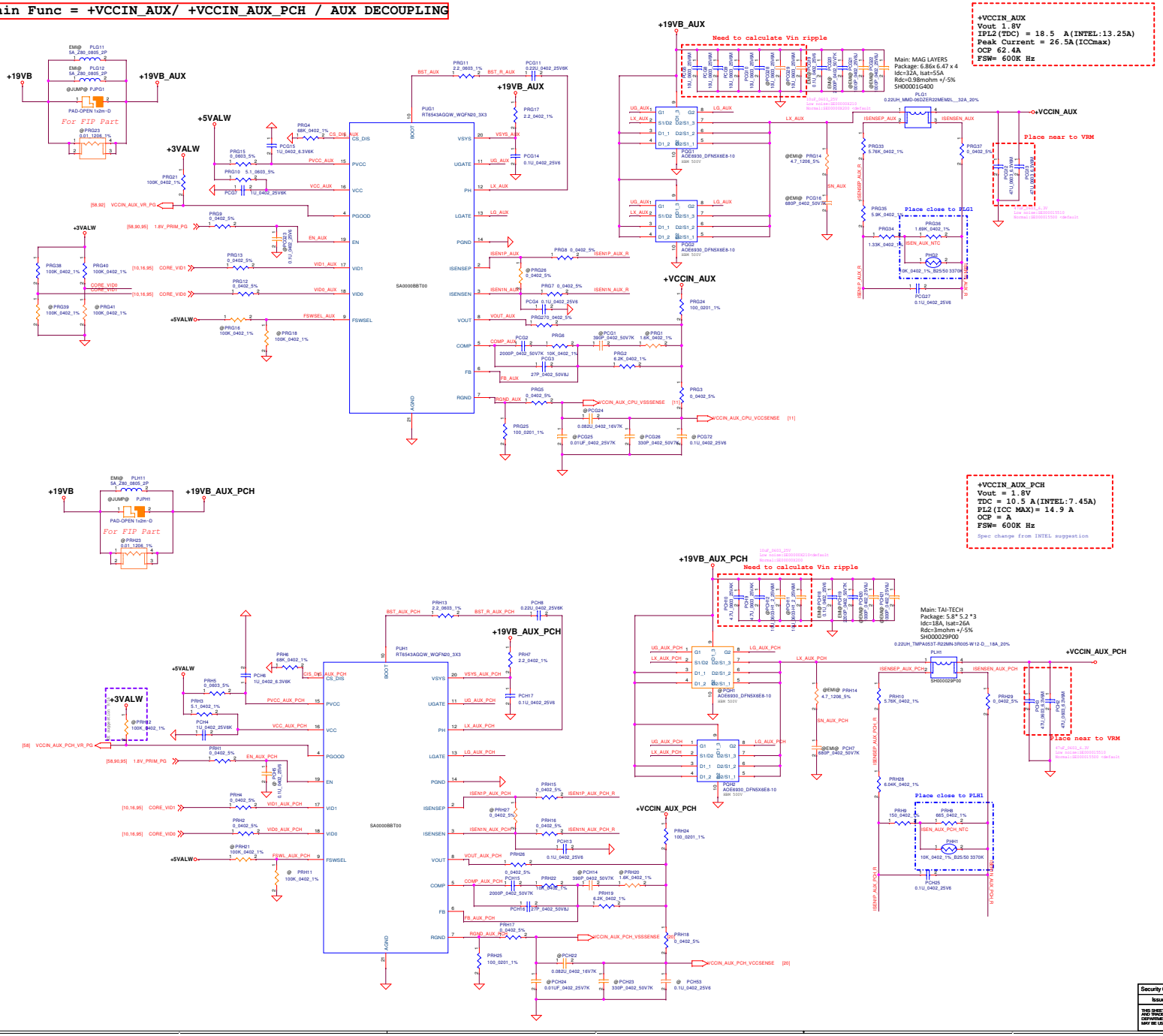
Main Func = +VCCIN_AUX/ +VCCIN_AUX_PCH / AUX DECOUPLING



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date	2018/12/31
Title			
Size	Document Number		Rev 0.1
	LA-K452P		
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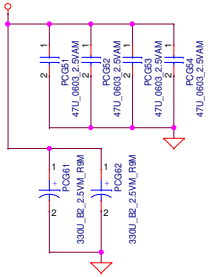
+VCCIN_AUX Decoupling Cap

CPU Primary Side

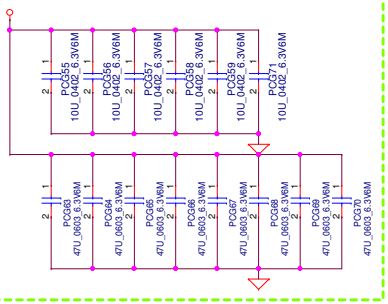
+VCCIN_AUX



For FIVR solution
15pF_0201 *6
12pF_0402 *6
on EE side (20200214)

CPU Secondary side

+VCCIN_AUX



Follow Intel PDG Rev0.5 excel
+VCCIN_AUX Output CAP :

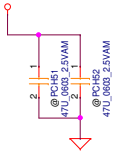
CPU Primary Side:
330uF_B2 *2pcs
47uF_0603 *4 pcs

CPU Secondary side:
10uF_0402 *6pcs
47uF_0603 *8pcs

+VCCIN_AUX_PCH Decoupling Cap

CPU Primary side

+VCCIN_AUX_PCH



Follow Intel PDG Rev0.5 excel
+VCCIN_AUX_PCH Output CAP :

CPU Primary Side:
47uF_0603 *5 pcs (Near PCH)
10uF_0402 *4 pcs (Near PCH)

on EE side (20200214)

reserve 47uF_0603 *2 pcs on PWR side (20200406)

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Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title

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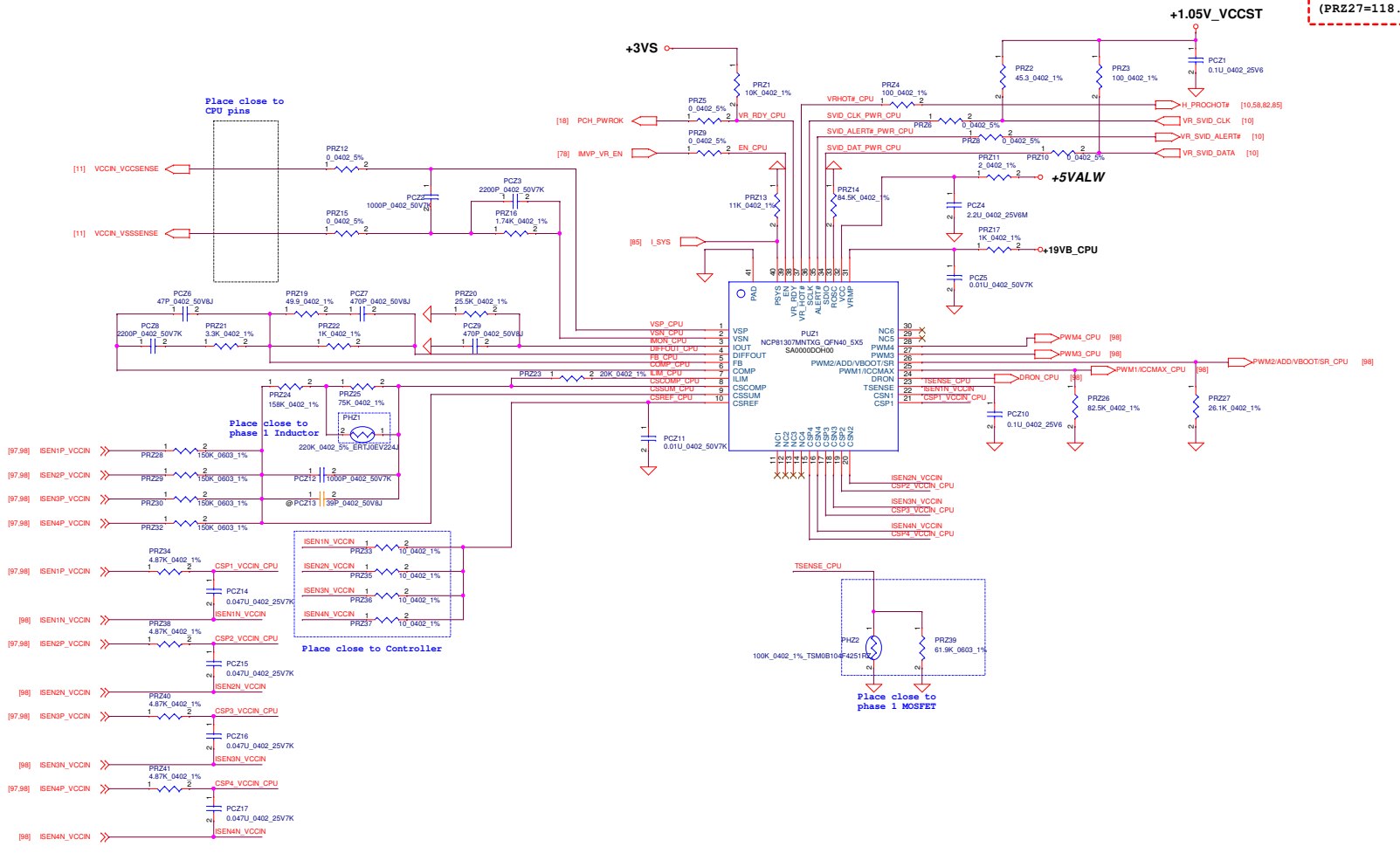
Date: Friday, March 19, 2021 | Sheet 96 of 120

Main Func = CPU

+VCCIN
Vout = 2.05V
IPL2 = 61A
Peak Curren = 105A(ICCmax)
DC Load line:NA
AC Load line:NA
Current limit = A(OCP)
FSW= 600K Hz
Initial Vboot = 0V (INTEL PDG)
(Initial PRZ27=26.1K_ADD=0 SR=48 Vboot=0)
For Debug only setting as below
Vboot = 1.8V
(PRZ27=118.3_ADD=0 SR=48 Vboot=0)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title: +VCORE_NCP81305
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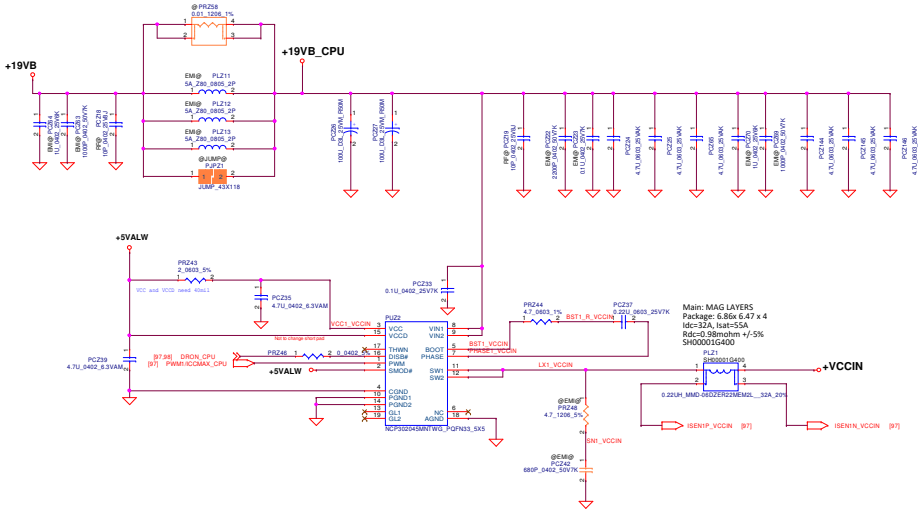
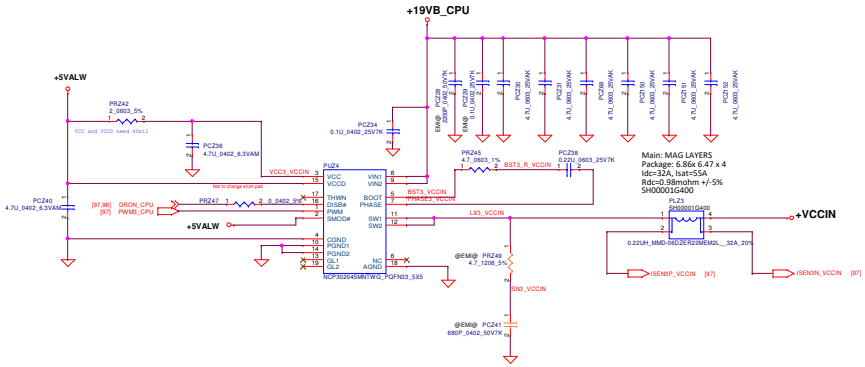
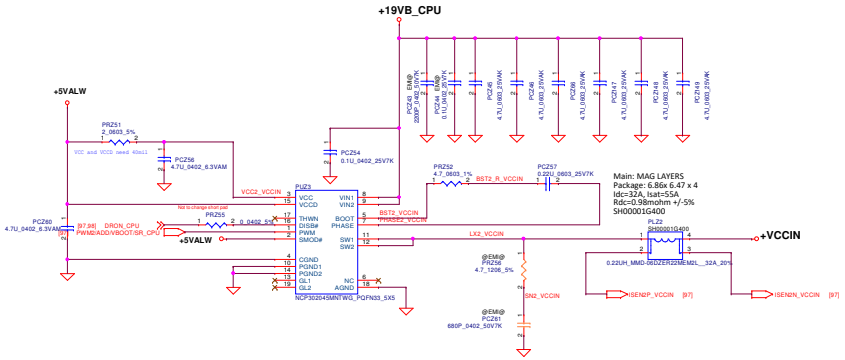
			Date: Friday, March 19, 2021 Sheet 97 of 120

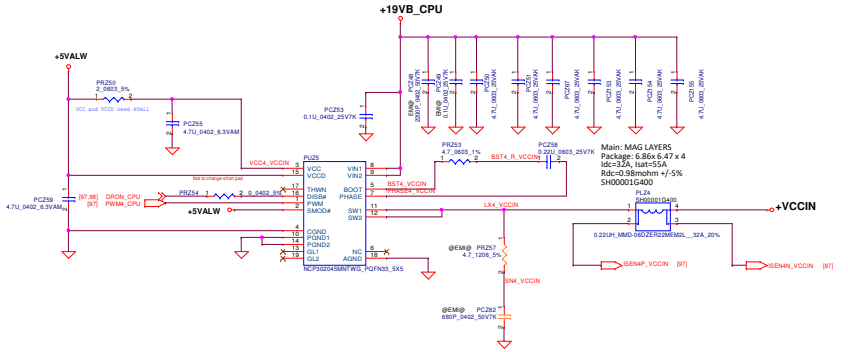
Main Func = +VCCIN

+VCCIN
Vout(max) = 2.05V
IPL2 = 61A
Peak Current = 105A(ICCmax)
DC Load line:NA
AC Load line:NA
Current limit = A(OCP)
FSW= 600K Hz









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Issued Date	2020/03/05	Deciphered Date	2017/01/06
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			Size: Document Number: LA-K452P Rev: 0.1
			Date: Friday, March 19, 2021 Sheet 98 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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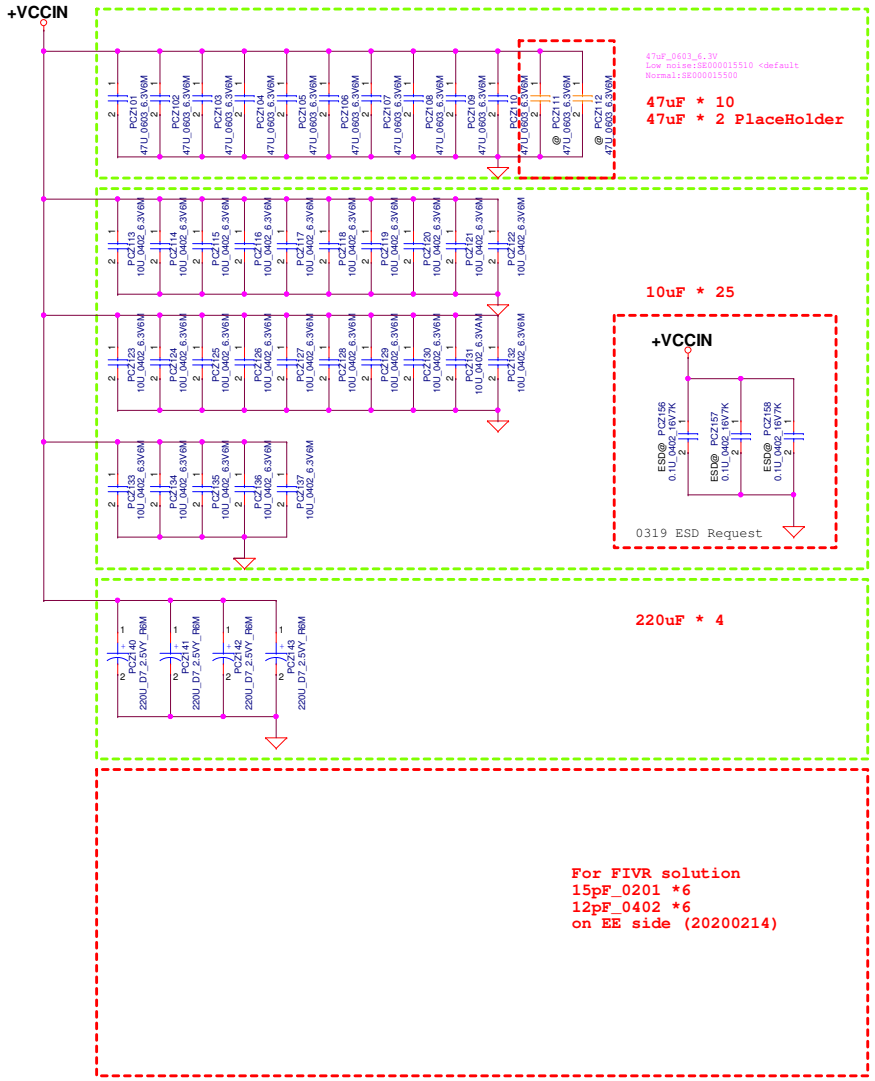
Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K452P	0.1

Date: Friday, March 19, 2021 Sheet 100 of 120

Main Func = +VCCIN DECOUPLING



Follow Intel PDG Rev0.5 excel
+VCCIN Output CAP :
47uF_0603 *10 pcs + reserved *2pcs
10uF_0402 *25 pcs
220uF_D7 *4pcs

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.			
Title	PWR_CPU DECOUPLING		
Size	Document Number		Rev
	LA-J743P		0.1
Date:	Friday, March 19, 2021	Sheet	101 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.		
Title		
Size	Document Number	Rev 0.1
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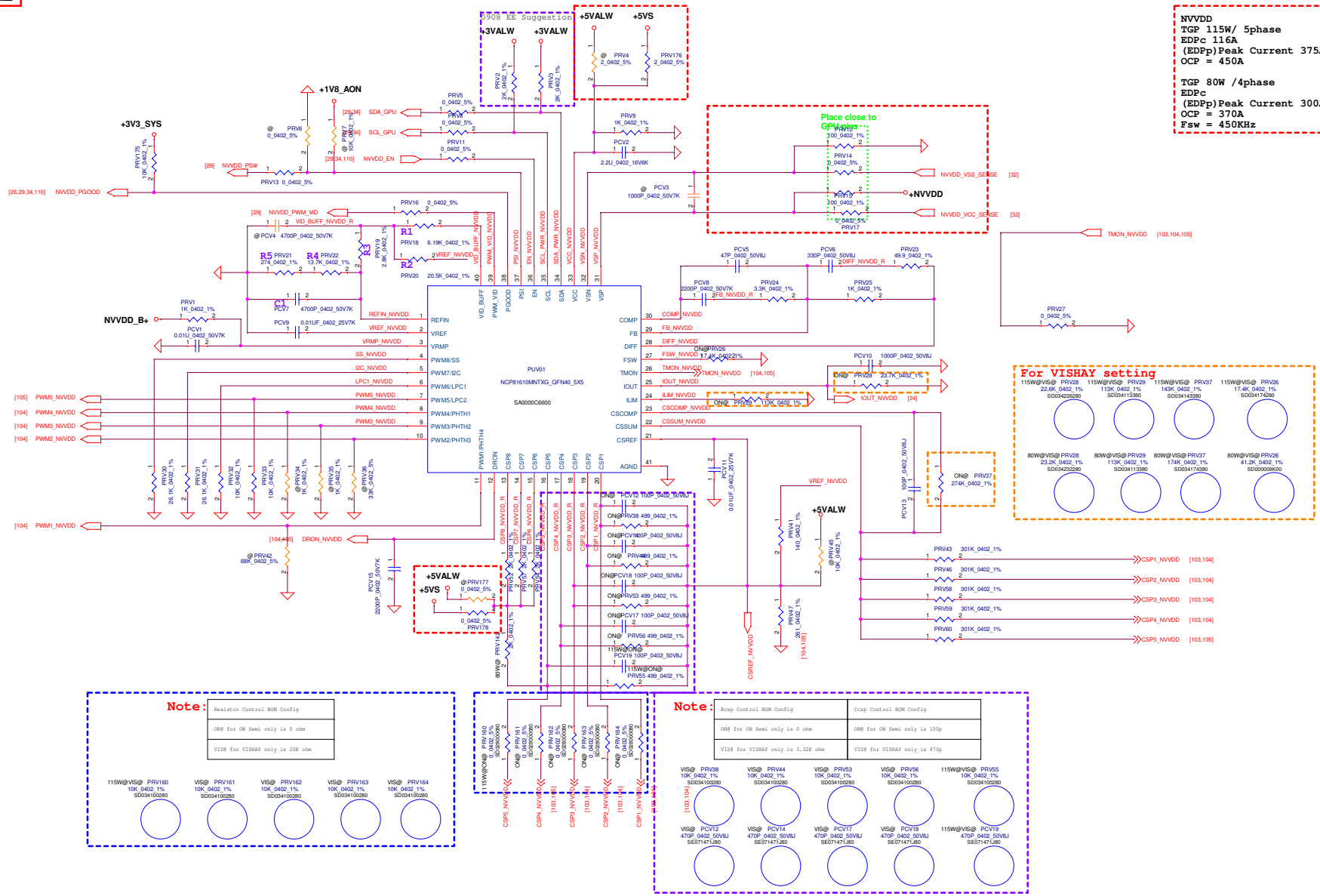
Date: Friday, March 19, 2021	Sheet 102 of 120	

Main Func = VGA CORE

Config	
Vmin	0.3
Vmax	1.3
Vboot	0.75
R1	6.19K
R2	20.5K
R3	2.8K
R4	13.7K
R5	0.274K
C	4.7n

NVDDD
TGP 115W/ 5phase
EDPc 116A
(EDPp)Peak Current 375A
OCP = 450A

TGP 80W /4phase
EDPc
(EDPp)Peak Current 300A
OCP = 370A
Fsw = 450KHz



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

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Compal Electronics, Inc.

Title: PWR_VGA_NCP81611MNTXG

Size: C | Document Number: LA-K452P | Rev: 0.1

Date: Friday, March 19, 2021 | Sheet 103 of 120

Main Func = GPU_CORE SW(1-4PH)

Note:

MOS Control BOM Config
ONS for ON Semi MOS only
VIS@ for VISHAY MOS only

VIS@ PUV2 SIC830ED SA0000ED2Z00 | VIS@ PUV3 SIC830ED SA0000ED2Z00 | VIS@ PUV4 SIC830ED SA0000ED2Z00 | VIS@ PUV5 SIC830ED SA0000ED2Z00

Note
EVT Used NCP303150D CPN"SA0000CU000"
DVT1 Used NCP303152 CPN "SA0000DIL00"

+NVVDD
TGP 115W
EDPc 105A
Peak Current 375A
Fsw=450K

+19VB — EMI@ PLV11 / PLV12 / PLV13 / PLV14 5A_Z80_0805_2P — GPU_B+ — PRV81 0.005_2512_1% — NVVDD_B+ — PRV82 0.005_2512_1% — FBVDD_B+

[34] CSSP_B+ [34] CSSN_B+ [34] CSSP_FBVDD [34] CSSN_FBVDD

Close to controller (PUV1) pin3

Phase 1 — PUV2 NCP303152MNTWG_PQFN41_5X6 SA0000DIL00

Main: MAG LAYERS
Package: 13.1 x 8.1 x 4
Idc=45A, Isat=77A
Rdc=0.48mohm +/-5%
SH00001QL00

Use 0805 size

Phase 2 — PUV3 NCP303152MNTWG_PQFN41_5X6 SA0000DIL00

Main: MAG LAYERS
Package: 13.1 x 8.1 x 4
Idc=45A, Isat=77A
Rdc=0.48mohm +/-5%
SH00001QL00

Use 0805 size

Phase 3 — PUV4 NCP303152MNTWG_PQFN41_5X6 SA0000DIL00

Main: MAG LAYERS
Package: 13.1 x 8.1 x 4
Idc=45A, Isat=77A
Rdc=0.48mohm +/-5%
SH00001QL00

Use 0805 size

Phase 4 — PUV5 NCP303152MNTWG_PQFN41_5X6 SA0000DIL00

Main: MAG LAYERS
Package: 13.1 x 8.1 x 4
Idc=45A, Isat=77A
Rdc=0.48mohm +/-5%
SH00001QL00

Use 0805 size

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

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Compal Electronics, Inc.

Title: **PWR_VGA_NCP30315**

Size: — Document Number: **LA-K452P** — Rev: 0.1

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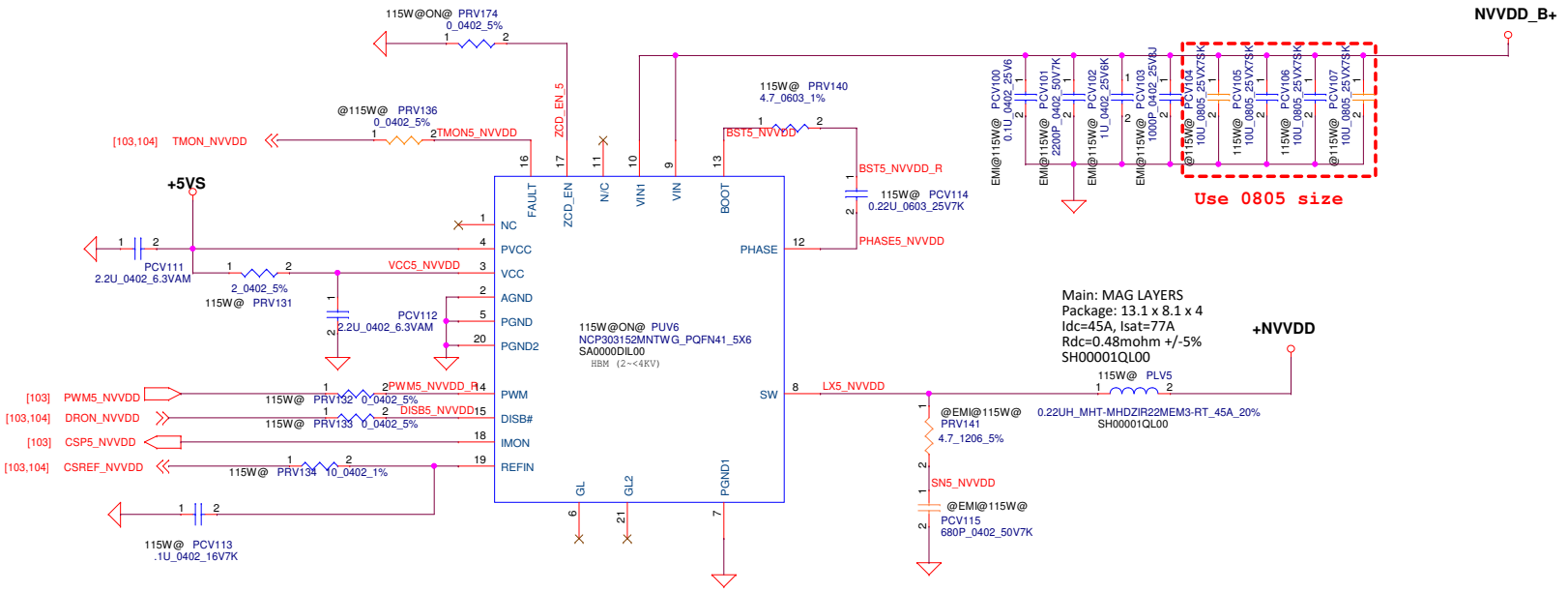
Main Func = GPU_CORE SW(5PH)

Note:

MOS Control BOM Config
ON@ for ON Semi MOS only
VIS@ for VISHAY MOS only

115W@VIS@ PUV6
SIC830ED
SA0000E0Z00

Note
EVT Used NCP303150D CPN"SA0000CUO00"
DVT1 Used NCP303152 CPN "SA0000DIL00"



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: *PWR- Reserve for PWR*

Size | Document Number: *LA-K452P* | Rev: 0.1

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title

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Main Func = VGA CORE DECOUPLING

+NVVDD / +MSVDD
330UF X 8
1UF_0402 X 66
4.7UF_0603 X 2
10UF_0603 X 23
47UF_0805 X7

DG-09845-001_v01
+NVVDD
330UF X 3
1UF_0402 X 37
4.7UF_0603 X 2
10UF_0603 X 12
47UF_0805 X 4

+MSVDD
330UF X 1
1UF_0402 X 29
10UF_0603 X 11
47UF_0805 X 2

+NVVDD

Place near GPU

Place under GPU

MSVDD

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

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Compal Electronics, Inc.

Title: PWR_NVVDD DECOUPLING

Size: | Document Number: LA-K452P | Rev: 0.1

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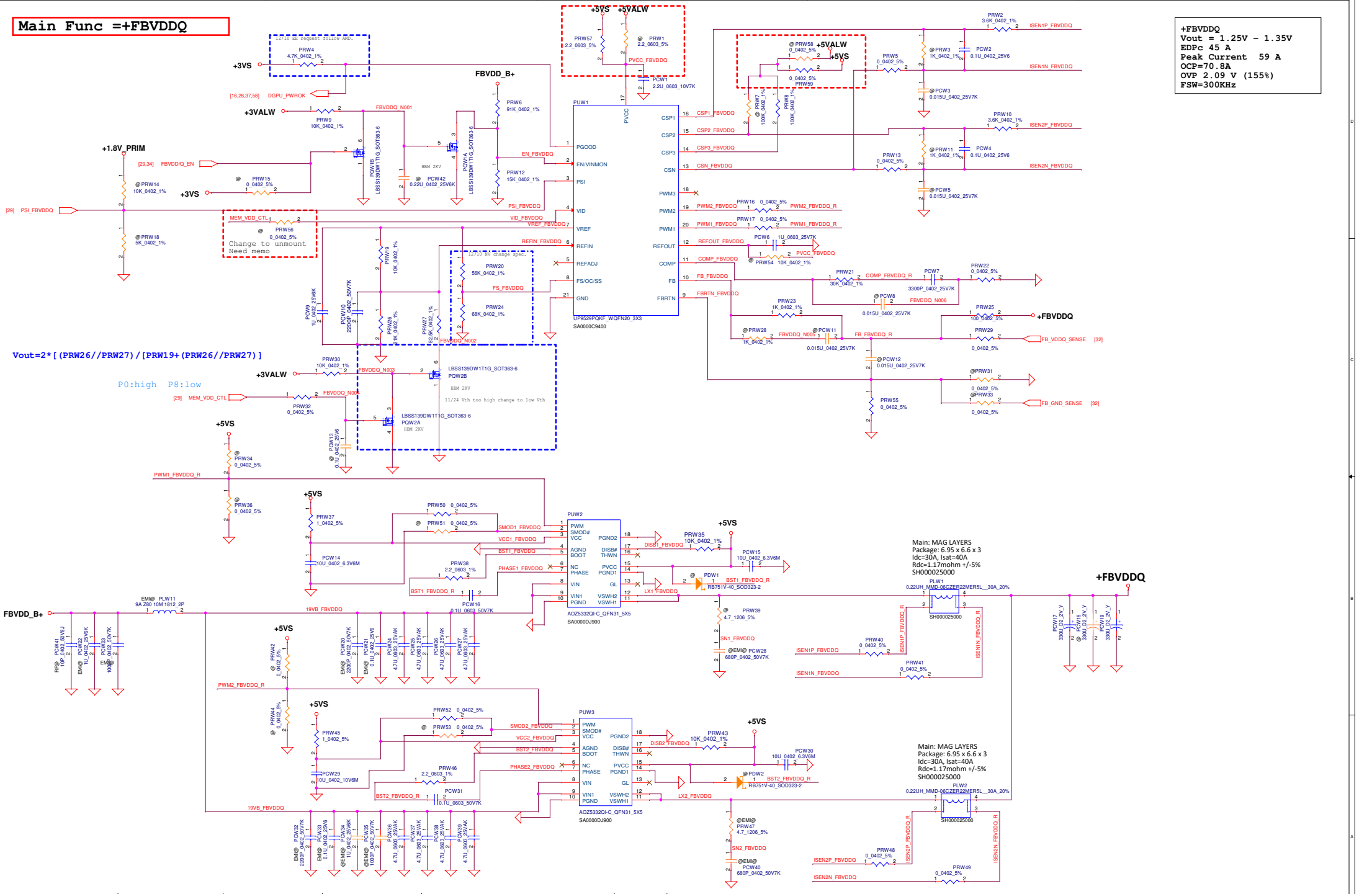
Main Func =+FBVDDQ

+FBVDDQ
Vout = 1.25V ~ 1.35V
EDPc 45 A
Peak Current 59 A
OCP=70.8A
OVP 2.09 V (155%)
FSW=300KHz

Vout=2*[(PRW26//PRW27)/[PRW19+(PRW26//PRW27)]

P0:high P8:low



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW30	PRW31
	GN20E			1.25V	16.9K	
				1.2V	16.9K	133K

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

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Compal Electronics, Inc.

Title: PWR +1.35VRAM

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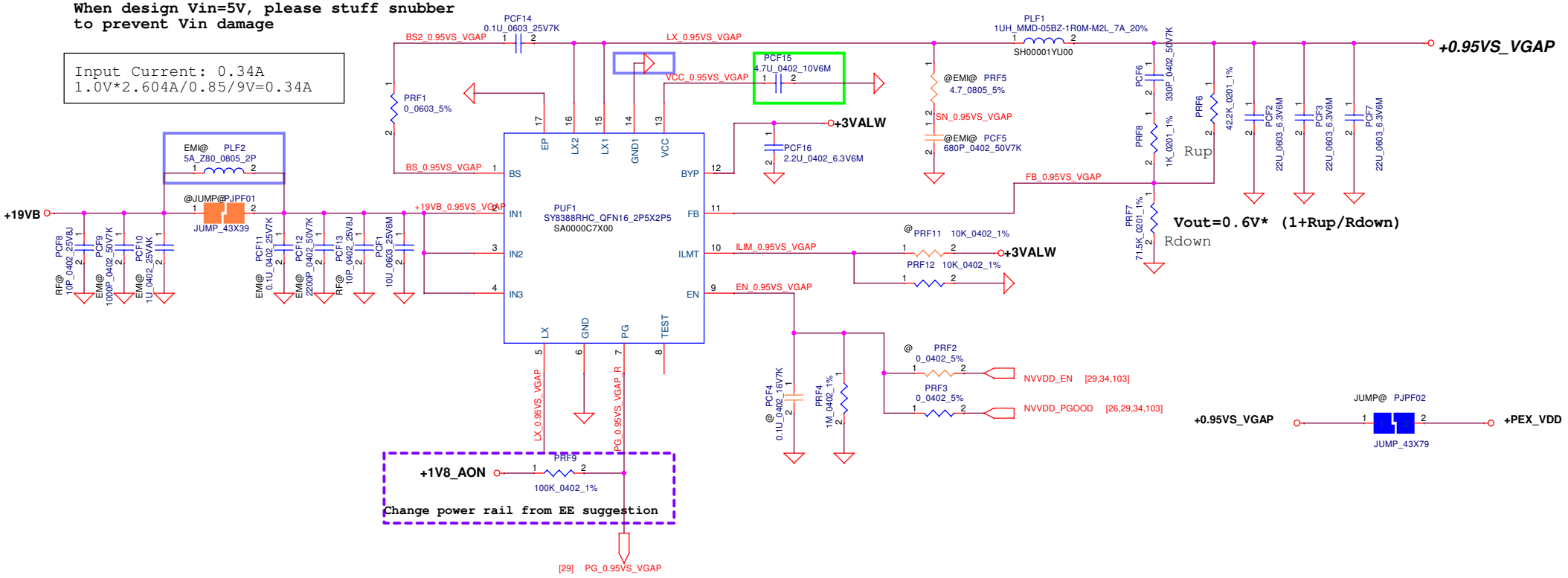
Main Func =+0.95VS_VGAP

M1_CYNTEC_PCMB053T-1R0MS
M3_MAG LAYERS_MMD-05CZ-1R0M-M7L
M4_CHILISIN_MHCI05030C-1R0M-R8
Package: 5.2 x 4.9 x 3
Idc=7A, Isat=11A
Rdc=13mohm +/-5%
SH00000Z200

+0.95VS_VGAP
TDC = 4.12A
Peak Current = 4.42A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Input Current: 0.34A
1.0V*2.604A/0.85/9V=0.34A



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/08/01

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Compal Electronics, Inc.

Title: PWR-+1.0VS_VGAP

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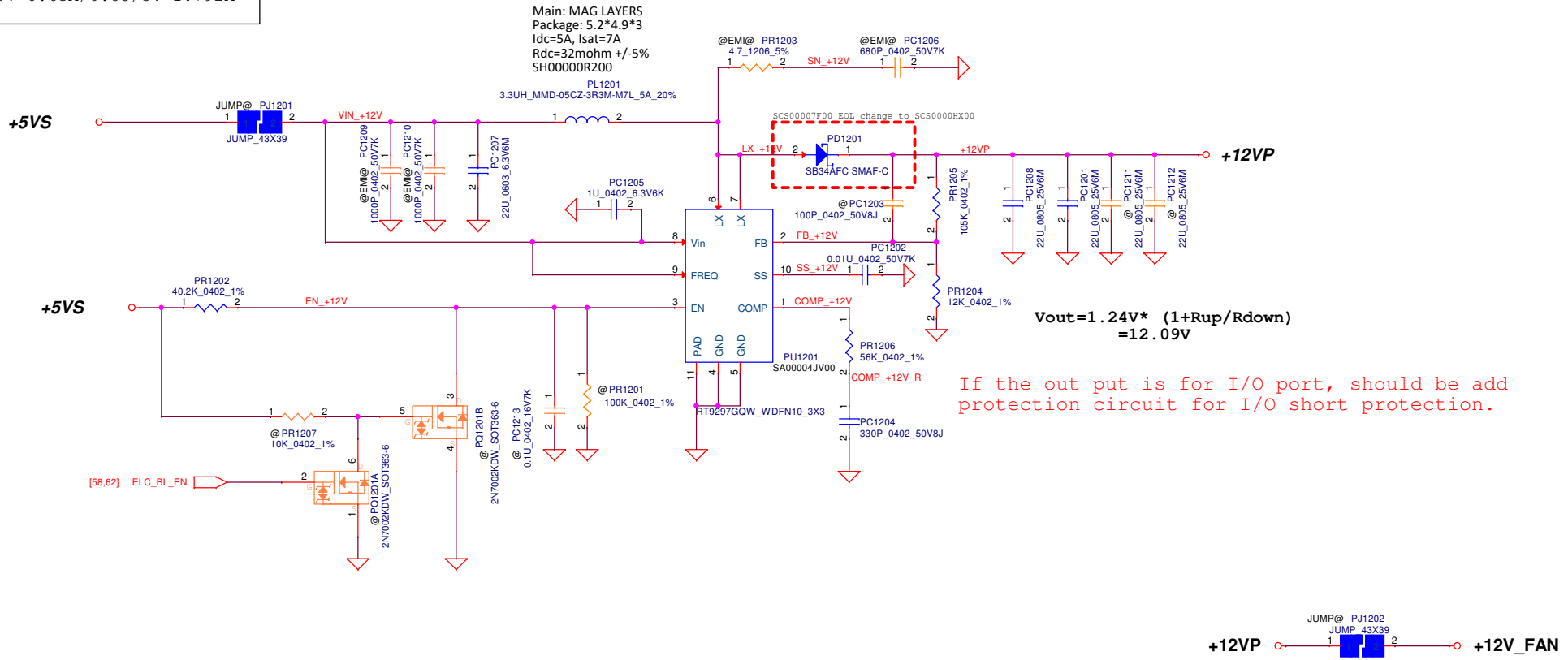
Main Func =+12VP_FAN

+12VP
Vout = 12.09 V
TDC 0.63A
Peak Current 0.9A
Current limit 3A
FSW=1.24MHz

Add a switch circuit to turn off the +12V_VIN if need.

Input Current: 1.792A
12.09V*0.63A/0.85/5V=1.792A



If the out put is for I/O port, should be add protection circuit for I/O short protection.

EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3

FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz

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Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.			
Title: PWR_+12VP_FAN			
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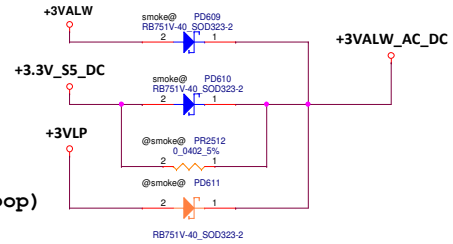
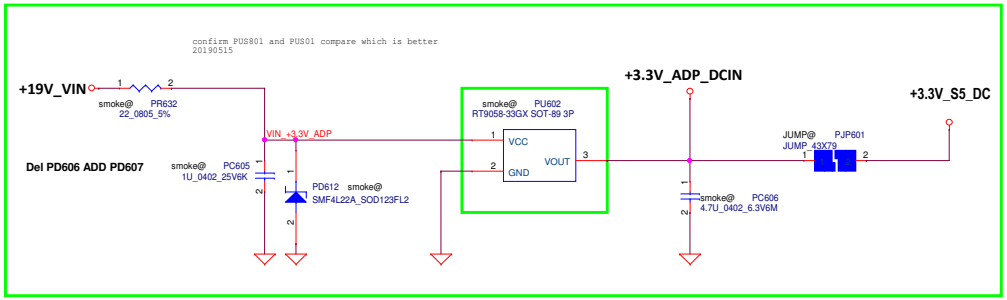
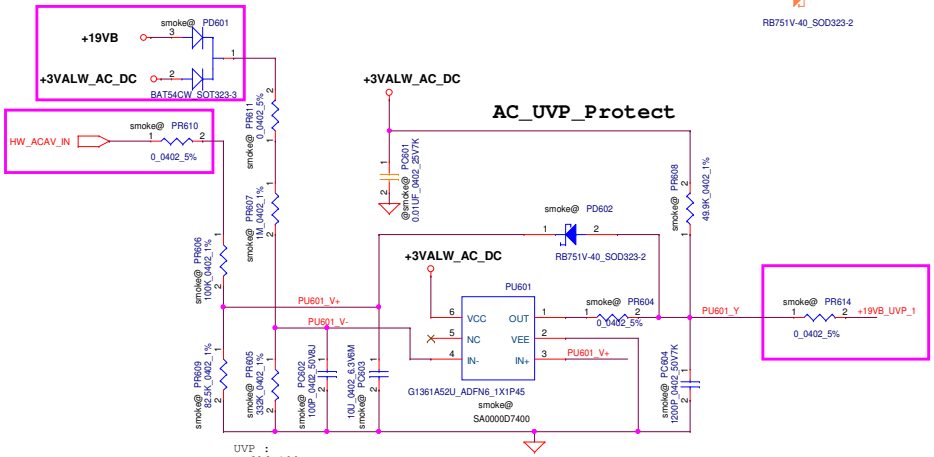
Main Func = Smokeless UVP

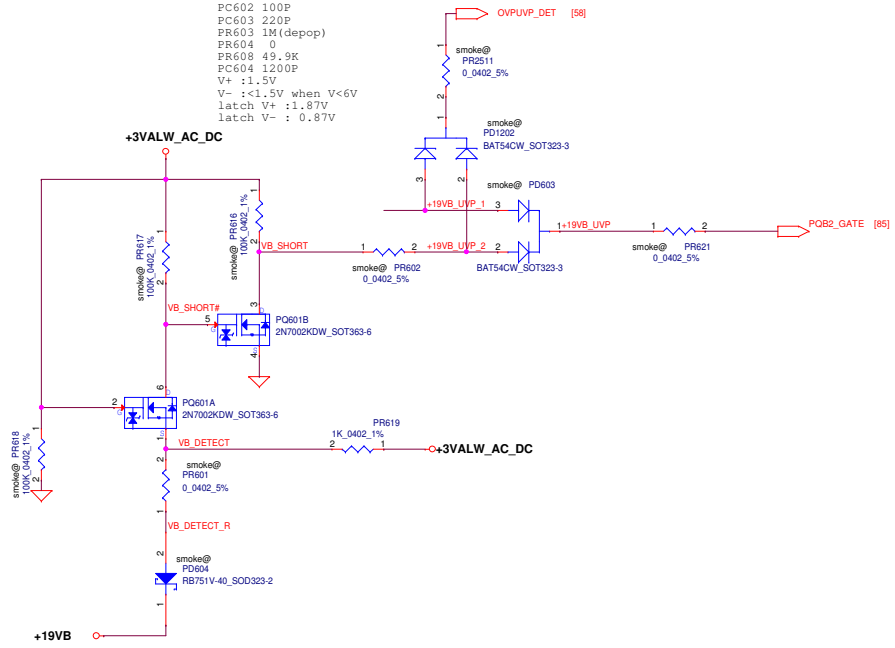


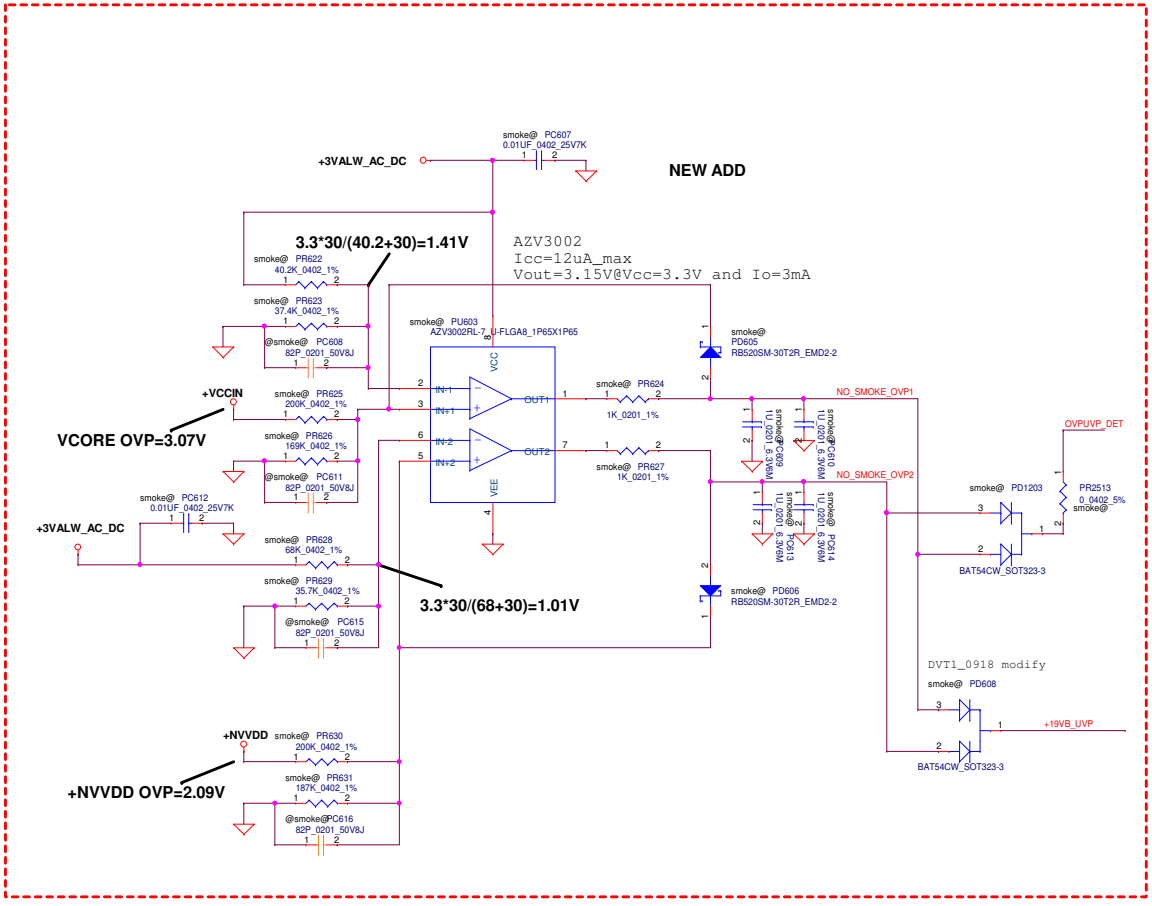


AC_UVP_Protect
Barrel disconncet detect (co-lay unpop)



UVP :
PR606 100K
PR609 82.5K
PR607 1M
PR605 332K
PC602 100P
PC603 220P
PR603 1M(depop)
PR604 0
PR608 49.9K
PC604 1200P
V+ :1.5V
V- :<1.5V when V<6V
latch V+ :1.87V
latch V- : 0.87V





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Title	PWR- Smokeless UVP/OVP
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P095	Change Choke Material shortage	2021 03/04	buyer	Material Shortage :SH00001RV00	Change Choke to SH000029P00	X02
2							X01
3							X01
4							X01
5							X01
6							X01
7							X01
8							X01
9							X01
10							X01

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Title: PWR_PIR

Size | Document Number: LA-K452P | Rev: 0.1

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Reserve

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