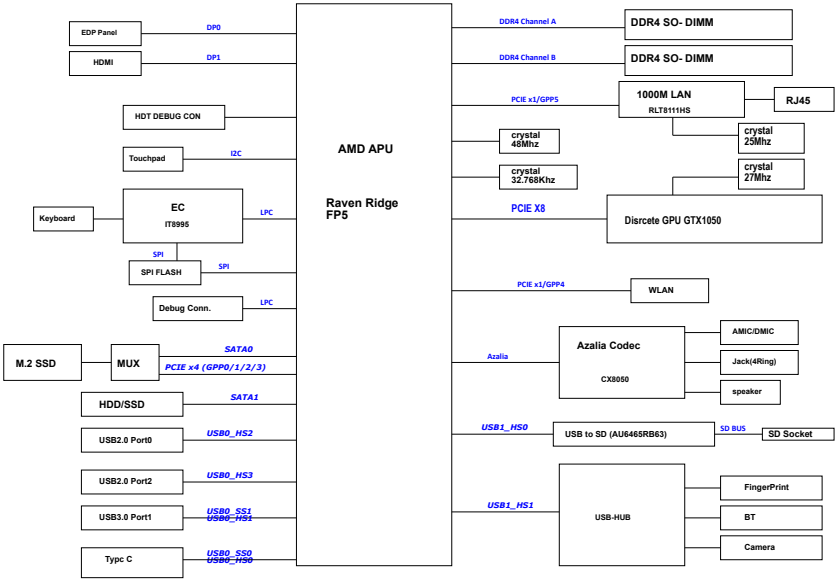
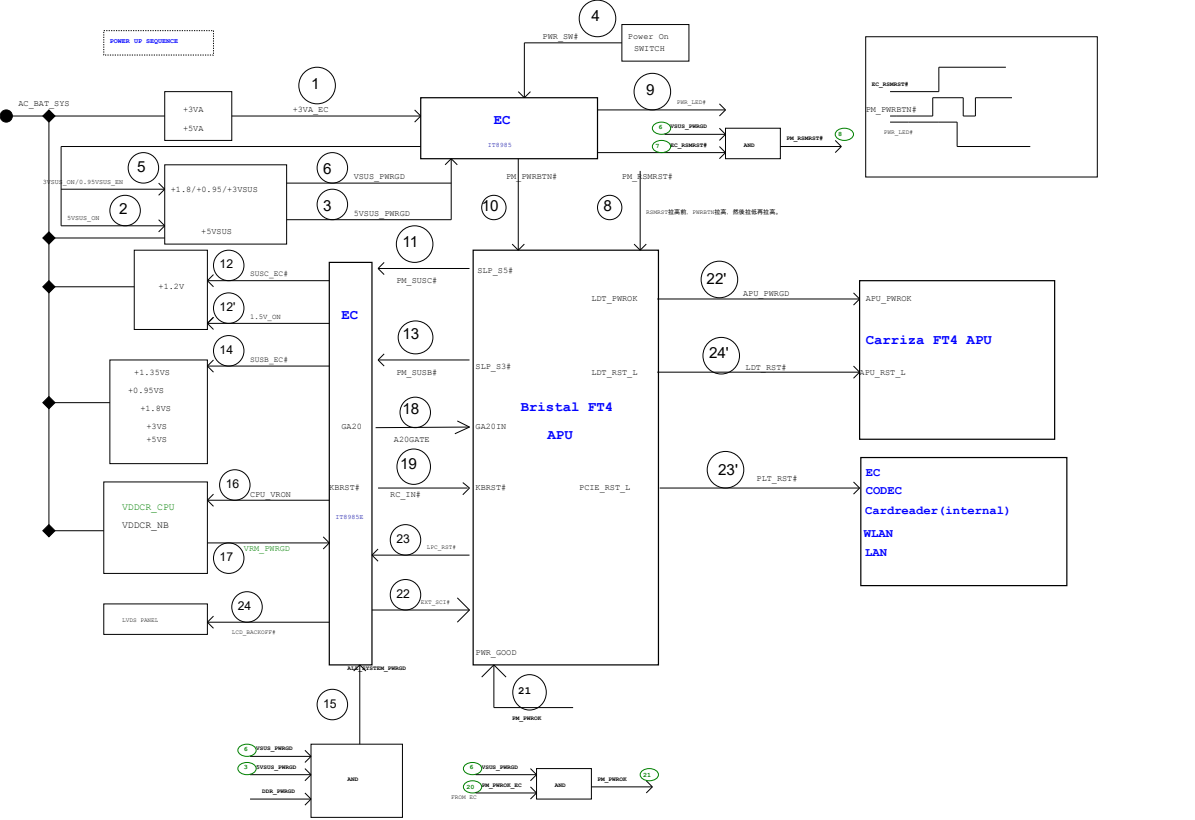
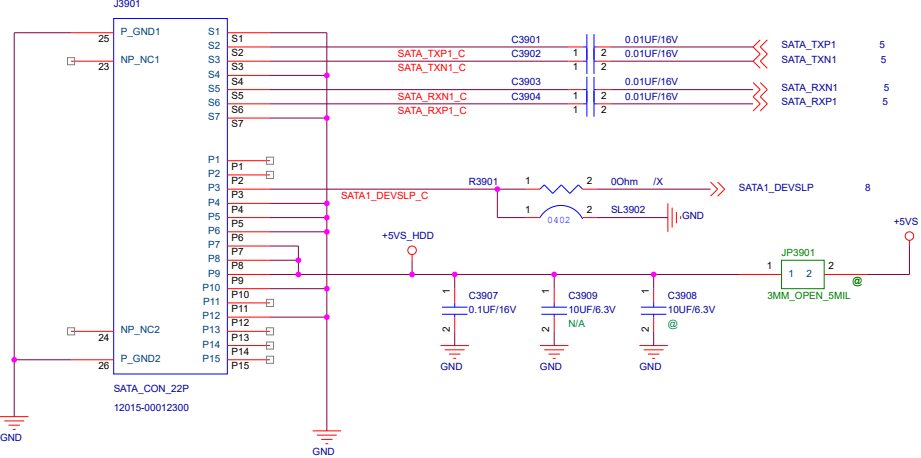
X570ZD Schematic R1.0

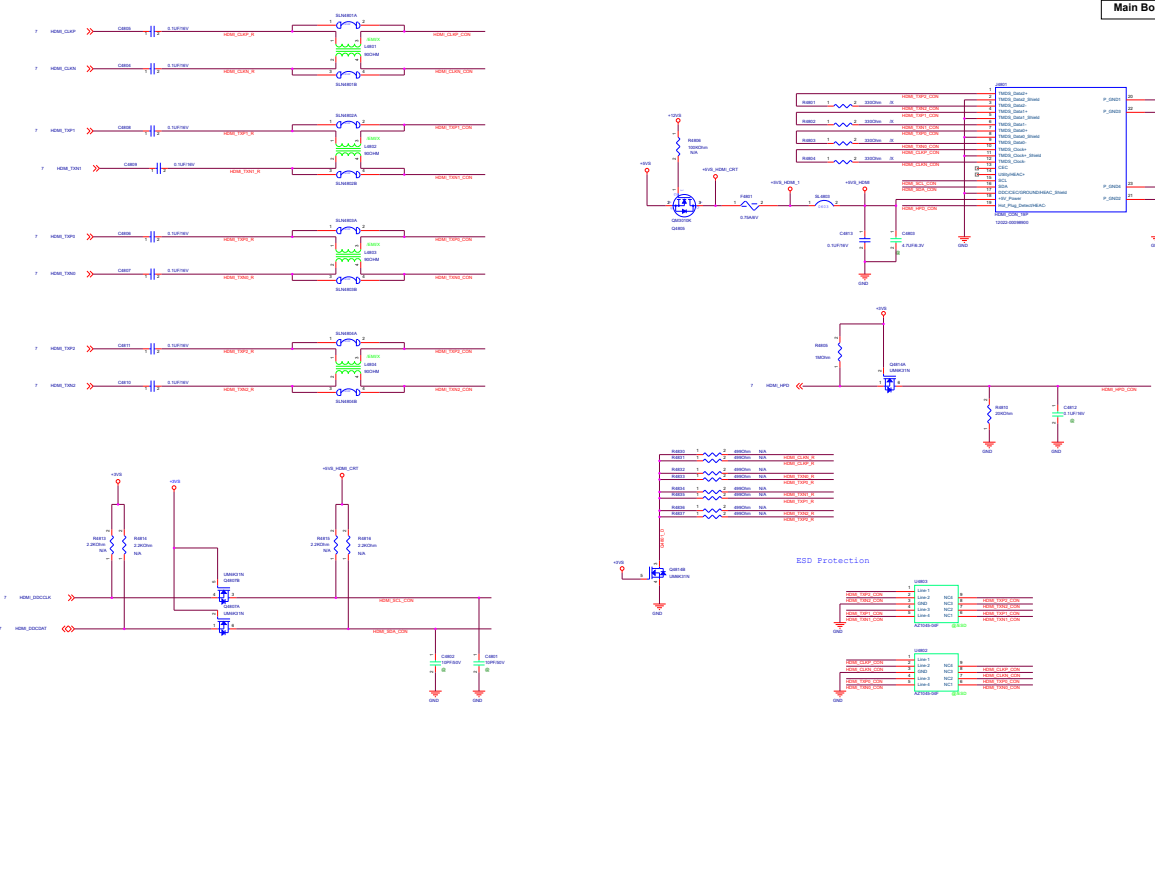


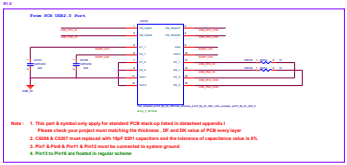

POWER UP SEQUENCE
AC_BAT_SYS
+3VA
+5VA
+3VA_EC
EC
IT8985
PWR_SW#
Power On
SWITCH
PWR_LED#
VSUS_PWRGD
EC_RSMRST#
AND
PM_RSMRST#
RC_RSMRST#
PM_PWRBTN#
PWR_LED#
VSUS_ON/0.95VSUS_EN
5VSUS_ON
+1.8/+0.95/+3VSUS
+5VSUS
VSUS_PWRGD
5VSUS_PWRGD
PM_PWRBTN#
PM_RSMRST#
RSMRST拉高前，PWRBTN拉高，然後拉低再拉高。
+1.2V
SUSC_EC#
1.5V_ON
SUSB_EC#
+1.35VS
+0.95VS
+1.8VS
+3VS
+5VS
EC
GA20
KBRST#
IT8985E
PM_SUSC#
PM_SUSB#
A20GATE
RC_IN#
LPC_RST#
EXT_SCI#
ALL_SYSTEM_PWRGD
SLP_S5#
SLP_S3#
GA20IN
KBRST#
PWR_GOOD
Bristal FT4
APU
LDT_PWROK
LDT_RST_L
PCIE_RST_L
APU_PWRGD
LDT_RST#
PLT_RST#
APU_PWROK
Carriza FT4 APU
APU_RST_L
EC
CODEC
Cardreader(internal)
WLAN
LAN
VDDCR_CPU
VDDCR_NB
CPU_VRON
VRM_PWRGD
LVDS PANEL
LCD_BACKOFF#
PM_PWROK
VSUS_PWRGD
5VSUS_PWRGD
DDR_PWRGD
AND
VSUS_PWRGD
PM_PWROK_EC
FROM EC
AND
PM_PWROK
1
2
3
4
5
6
8
9
10
11
12
12'
13
14
15
16
17
18
19
21
22
22'
23
23'
24
24'

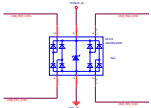


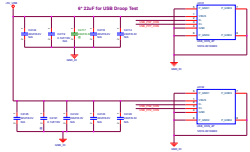
<Variant Name>

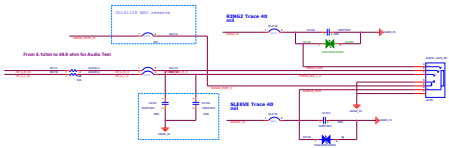
ASUSTeK COMPUTER INC. NB3	Title : SATA_HDD	
	Engineer: SZ-NB	
Size: A	Project Name: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 39 of 102	

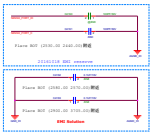

ESD Protection



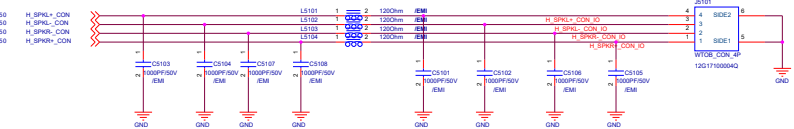






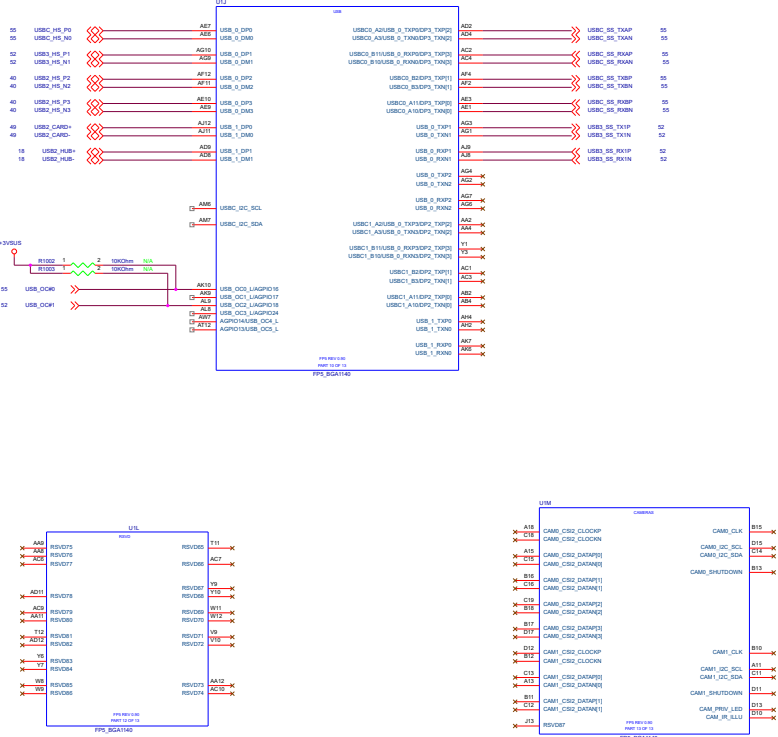


Quanta Computer		Title :	IO Board_USB Conn_HP		
Size	Document Number			Rev	
			X07501D		
Date: Monday, February 09, 2015		Sheet	of		



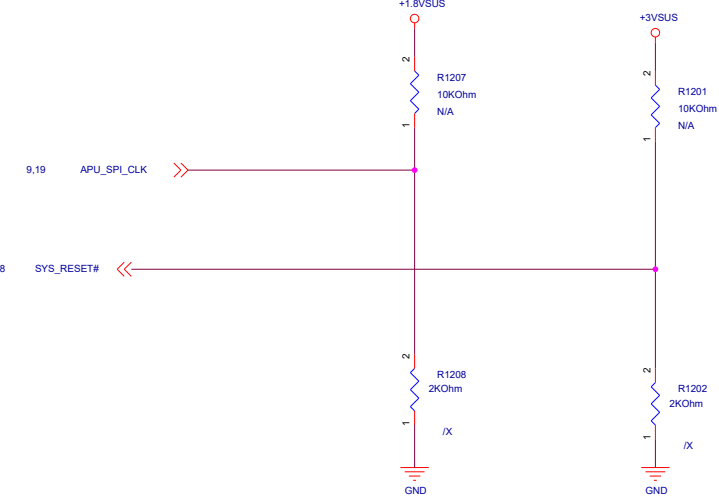
<Variant Name>

ASUS	Project Name: X505ZN	Rev: R0.1
Title :		
Size: B	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, May 07, 2018	Sheet: 51 of 99	


U1J
USB
USBC_HS_P0
USBC_HS_N0
USB3_HS_P1
USB3_HS_N1
USB2_HS_P2
USB2_HS_N2
USB2_HS_P3
USB2_HS_N3
USB2_CARD+
USB2_CARD-
USB2_HUB+
USB2_HUB-
AE7
AE6
AG10
AG9
AF12
AF11
AE10
AE9
AJ12
AJ11
AD9
AD8
USB_0_DP0
USB_0_DM0
USB_0_DP1
USB_0_DM1
USB_0_DP2
USB_0_DM2
USB_0_DP3
USB_0_DM3
USB_1_DP0
USB_1_DM0
USB_1_DP1
USB_1_DM1
USBC0_A2/USB_0_TXP0/DP3_TXP[2]
USBC0_A3/USB_0_TXN0/DP3_TXN[2]
USBC0_B1/USB_0_RXP0/DP3_TXP[3]
USBC0_B10/USB_0_RXN0/DP3_TXN[3]
USBC0_B2/DP3_TXP[1]
USBC0_B3/DP3_TXN[1]
USBC0_A11/DP3_TXP[0]
USBC_SS_TXAP
USBC_SS_TXAN
USBC_SS_RXAP
USBC_SS_RXAN
USBC_SS_TXBP
USBC_SS_TXBN
USBC_SS_RXBP
USBC_SS_RXBN
USB_0_TXP1
USB_0_TXN1
USB_0_RXP1
USB_0_RXN1
USB_0_TXP2
USB_0_TXN2
USB_0_RXP2
USB_0_RXN2
USB_0_TXP3
USB_0_RXN3
USBC_I2C_SCL
USBC_I2C_SDA
USBC1_A2/USB_0_TXP3/DP2_TXP[2]
USBC1_A3/USB_0_TXN3/DP2_TXN[2]
USBC1_B1/USB_0_RXP3/DP2_TXP[3]
USBC1_B10/USB_0_RXN3/DP2_TXN[3]
USBC1_B2/DP2_TXP[1]
USBC1_B3/DP2_TXN[1]
USBC1_A11/DP2_TXP[0]
USBC1_A10/DP2_TXN[0]
USB_1_TXP0
USB_1_TXN0
USB_1_RXP0
USB_1_RXN0
AD2
AD4
AC2
AC4
AF4
AF2
AE3
AE1
AG3
AG1
AJ9
AJ8
AG4
AG2
AG7
AG6
AA2
AA4
AC1
AC3
AB2
AB4
AH4
AH2
AK7
AK6
AM6
AM7
AK10
AK9
AL9
AL8
AW7
AT12
Y1
Y3
FP5 REV 0.80
PART 10 OF 13
FP5_BGA1140
+3VSUS
R1002
R1003
10KOhm
N/A
USB_OC#0
USB_OC#1
USB_OC0_LIAGPIO16
USB_OC1_LIAGPIO17
USB_OC2_LIAGPIO18
USB_OC3_LIAGPIO24
AGPIO14/USB_OC4_L
AGPIO13/USB_OC5_L

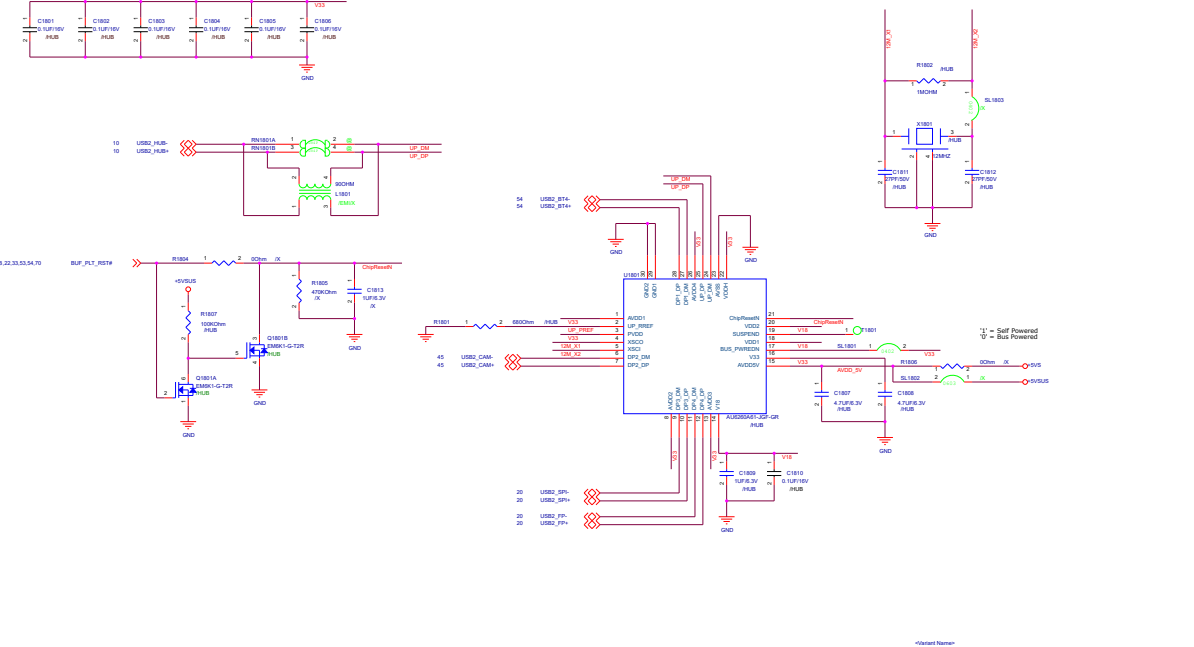
U1L
RSVD
RSVD75
RSVD76
RSVD77
RSVD78
RSVD79
RSVD80
RSVD81
RSVD82
RSVD83
RSVD84
RSVD85
RSVD86
RSVD87
RSVD88
RSVD89
RSVD70
RSVD71
RSVD72
RSVD73
RSVD74
RSVD55
RSVD56
RSVD57
RSVD58
RSVD59
RSVD60
FP5 REV 0.80
PART 12 OF 13
FP5_BGA1140

U1M
CAMERAS
CAM0_CSI2_CLOCKP
CAM0_CSI2_CLOCKN
CAM0_CSI2_DATAP[0]
CAM0_CSI2_DATAN[0]
CAM0_CSI2_DATAP[1]
CAM0_CSI2_DATAN[1]
CAM0_CSI2_DATAP[2]
CAM0_CSI2_DATAN[2]
CAM0_CSI2_DATAP[3]
CAM0_CSI2_DATAN[3]
CAM1_CSI2_CLOCKP
CAM1_CSI2_CLOCKN
CAM1_CSI2_DATAP[0]
CAM1_CSI2_DATAN[0]
CAM1_CSI2_DATAP[1]
CAM1_CSI2_DATAN[1]
RSVD87
CAM0_CLK
CAM0_I2C_SCL
CAM0_I2C_SDA
CAM0_SHUTDOWN
CAM1_CLK
CAM1_I2C_SCL
CAM1_I2C_SDA
CAM1_SHUTDOWN
CAM_PRIV_LED
CAM_IR_ILLU
FP5 REV 0.80
PART 13 OF 13
FP5_BGA1140

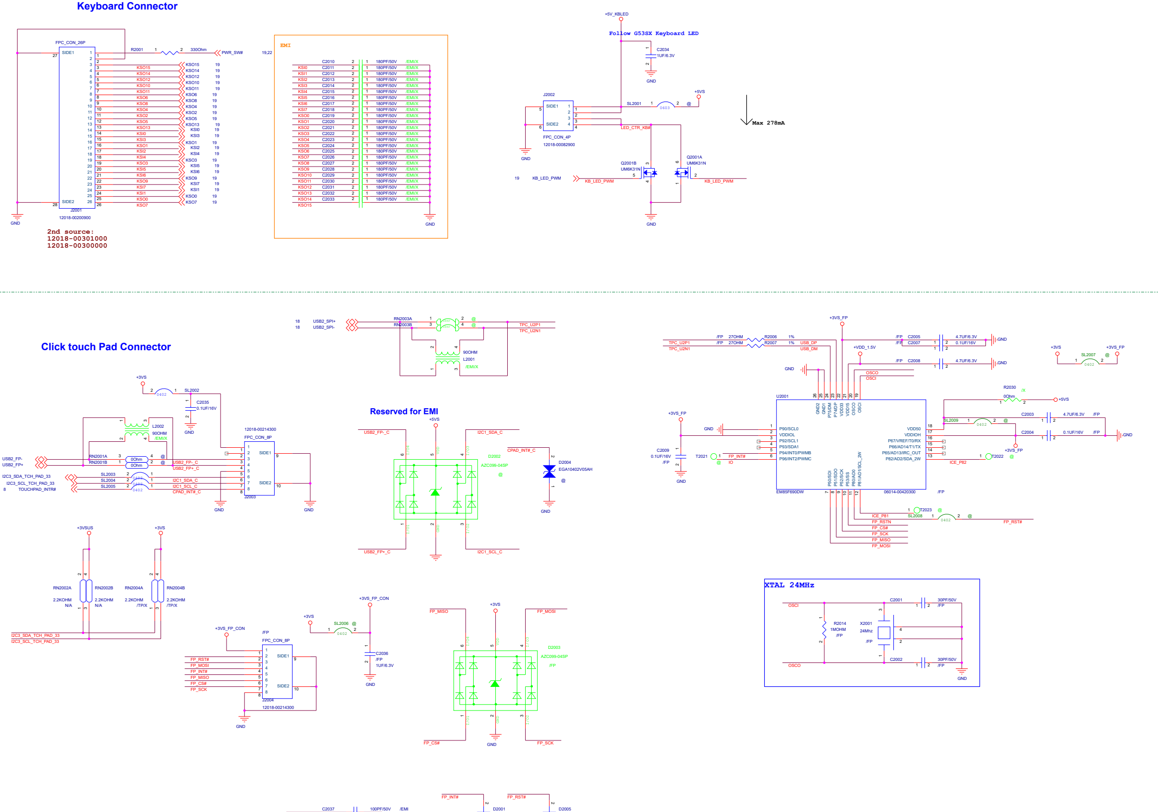


<Variant Name>

ASUS	Project Name: X505ZN	Rev: R0.1
Title :		
Size: A	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, May 07, 2018	Sheet 12 of 99	



Main Board



<Variant Name>

Title : KBC_KB & TP&FP

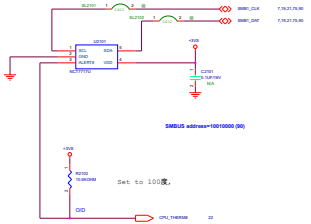
ASUSTeK COMPUTER INC. NB1

Engineer: SZNB

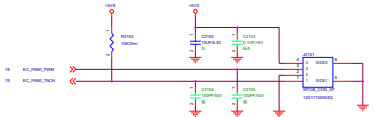
Size	Project Name	Rev
C	X570UD	R1.0

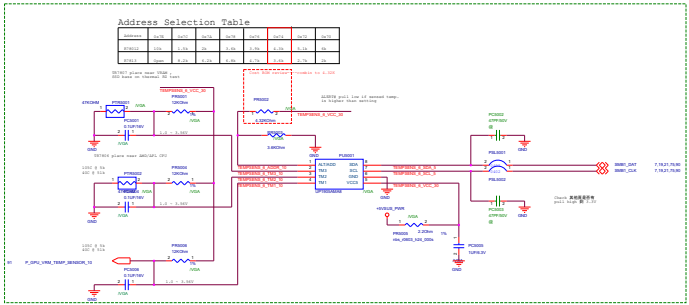
Date: Monday, May 07, 2018 Sheet 20 of 102

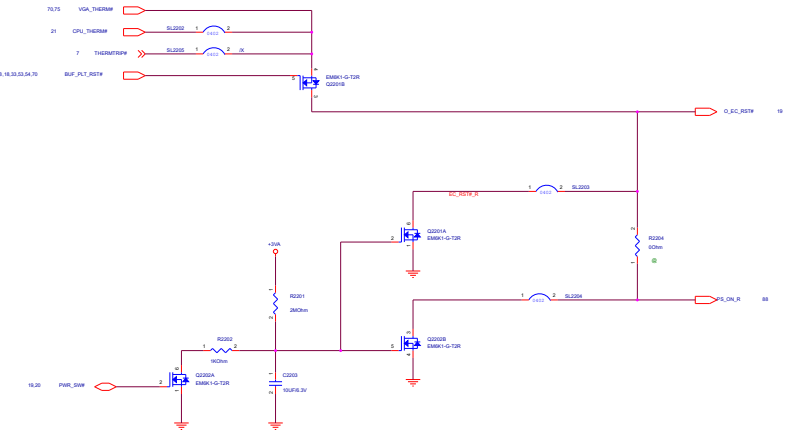
CPU Thermal Sensor

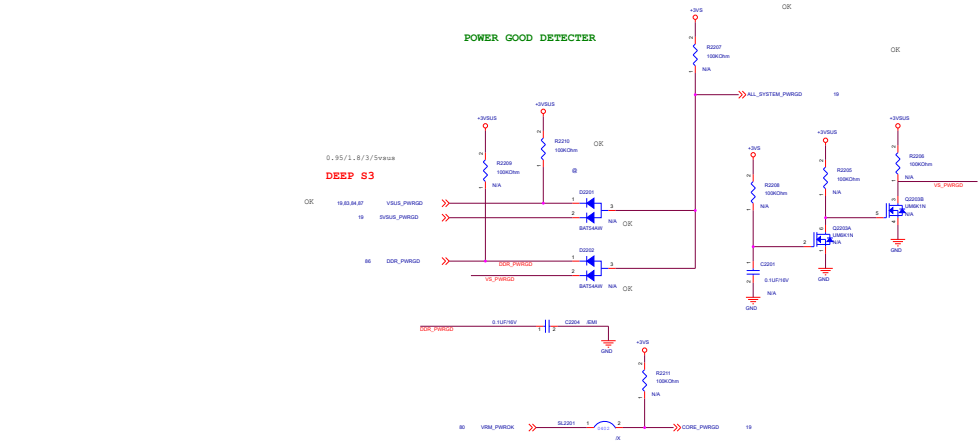


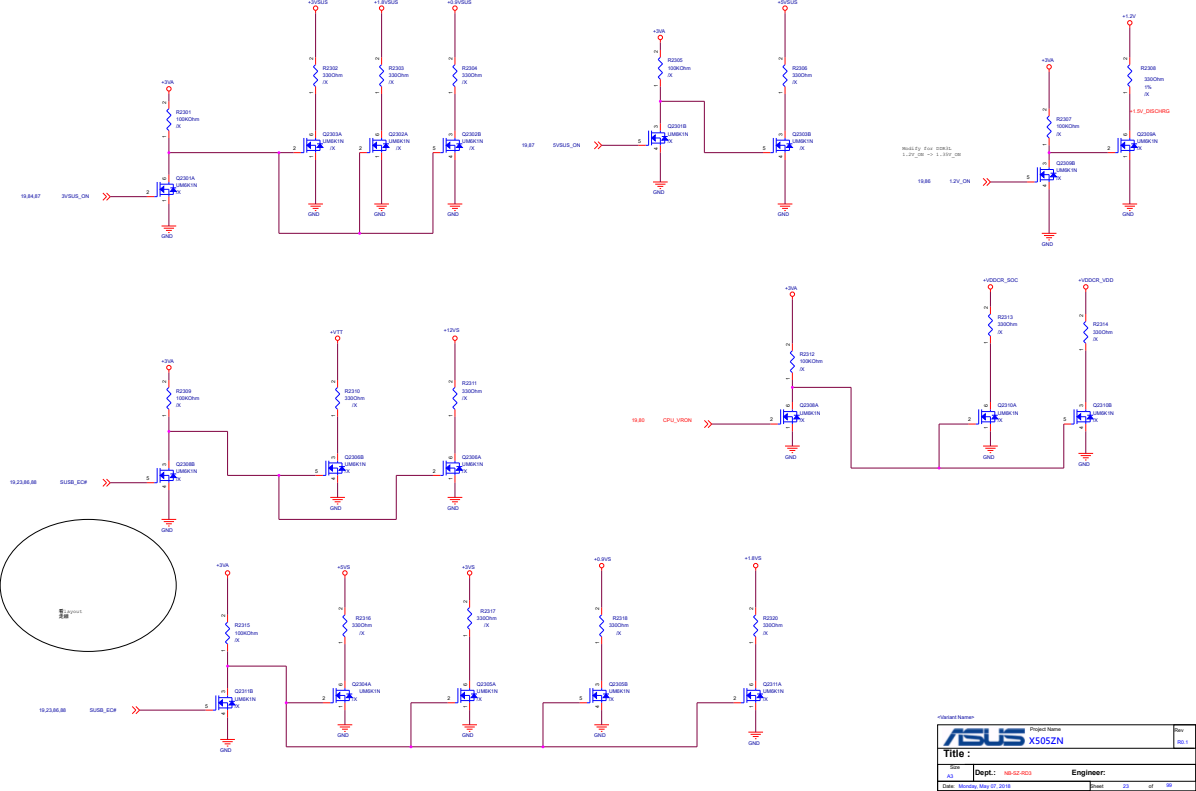
DC FAN 0



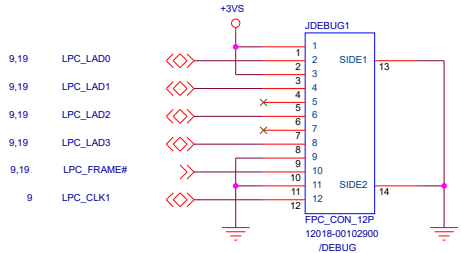



70,75 VGA_THERM#
21 CPU_THERM#
7 THERMTRIP#
0,18,33,53,54,70 BUF_PLT_RST#
SL2202
SL2205
EMBK1-G-T2R
Q2201B
O_EC_RST#
19
EC_RSTF_R
SL2203
Q2201A
EMBK1-G-T2R
R2204
0Ohm
+3VA
R2201
2MOhm
SL2204
PS_ON_R
88
R2202
1MOhm
Q2202B
EMBK1-G-T2R
Q2202A
EMBK1-G-T2R
C2203
10UF/6.3V
19,20 PWR_SW#


POWER GOOD DETECTER
OK
0.95/1.8/3/5vaux
DEEP S3
+3VS
R2207
100KOhm
N/A
ALL_SYSTEM_PWRGD
19
+3VSUS
R2210
100KOhm
R2209
100KOhm
N/A
19,83,84,87 VSUS_PWRGD
19 SVSUS_PWRGD
D2201
BAT54AW
N/A
86 DDR_PWRGD
D2202
BAT54AW
N/A
DDR_PWRGD
VS_PWRGD
R2208
100KOhm
N/A
C2201
0.1UF/16V
N/A
GND
R2205
100KOhm
N/A
Q2203A
UMBK1N
N/A
R2206
100KOhm
N/A
Q2203B
UMBK1N
N/A
VS_PWRGD
0.1UF/16V
C2204 /EMI
R2211
100KOhm
N/A
80 VRM_PWROK
SL2201
CORE_PWRGD
19

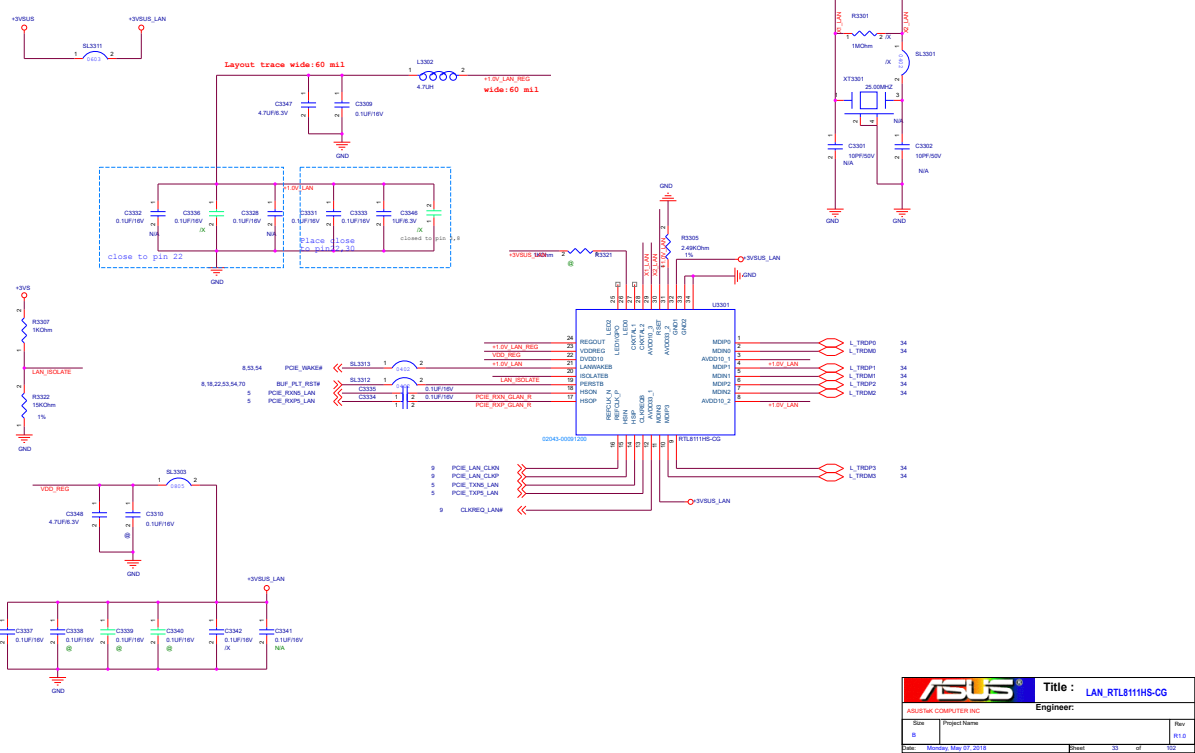

+3VA
+3VSUS
+1.8VSUS
+0.9VSUS
R2301 100KOhm /K
R2302 330Ohm /K
R2303 330Ohm /K
R2304 330Ohm /K
Q2301A UM6K1N /K
Q2303A UM6K1N /K
Q2302A UM6K1N /K
Q2302B UM6K1N /K
GND
19,84,87 3VSUS_ON
+3VA
+0.9VSUS
R2305 100KOhm /K
R2306 330Ohm /K
Q2301B UM6K1N /K
Q2303B UM6K1N /K
19,87 SVSUS_ON
GND
+3VA
+1.2V
R2307 100KOhm /K
R2308 330Ohm 1% /K
Q2309B UM6K1N /K
Q2309A UM6K1N /K
+1.5V_DISCHRG
Modify for DDR3L 1.2V_GM -> 1.35V_GM
19,86 1.2V_ON
GND
+3VA
+VTT
+12VS
R2309 100KOhm /K
R2310 330Ohm /K
R2311 330Ohm /K
Q2306B UM6K1N /K
Q2306A UM6K1N /K
19,23,86,88 SUSB_EC#
GND
+3VA
+VDDCR_SOC
+VDDCR_VDD
R2312 100KOhm /K
R2313 330Ohm /K
R2314 330Ohm /K
Q2308A UM6K1N /K
Q2310A UM6K1N /K
Q2310B UM6K1N /K
19,80 CPU_VRON
GND
+3VA
+5VS
+3VS
+0.9VS
+1.8VS
R2315 100KOhm /K
R2316 330Ohm /K
R2317 330Ohm /K
R2318 330Ohm /K
R2320 330Ohm /K
Q2311B UM6K1N /K
Q2304A UM6K1N /K
Q2305A UM6K1N /K
Q2305B UM6K1N /K
Q2311A UM6K1N /K
19,23,86,88 SUSB_EC#
GND
<Variant Name>
Project Name X505ZN
Rev 0G.1
Title :
Size A3
Dept.: NB-S2-803
Engineer:
Date: Monday, May 07, 2018
Sheet 23 of 99

LPC Debug Port

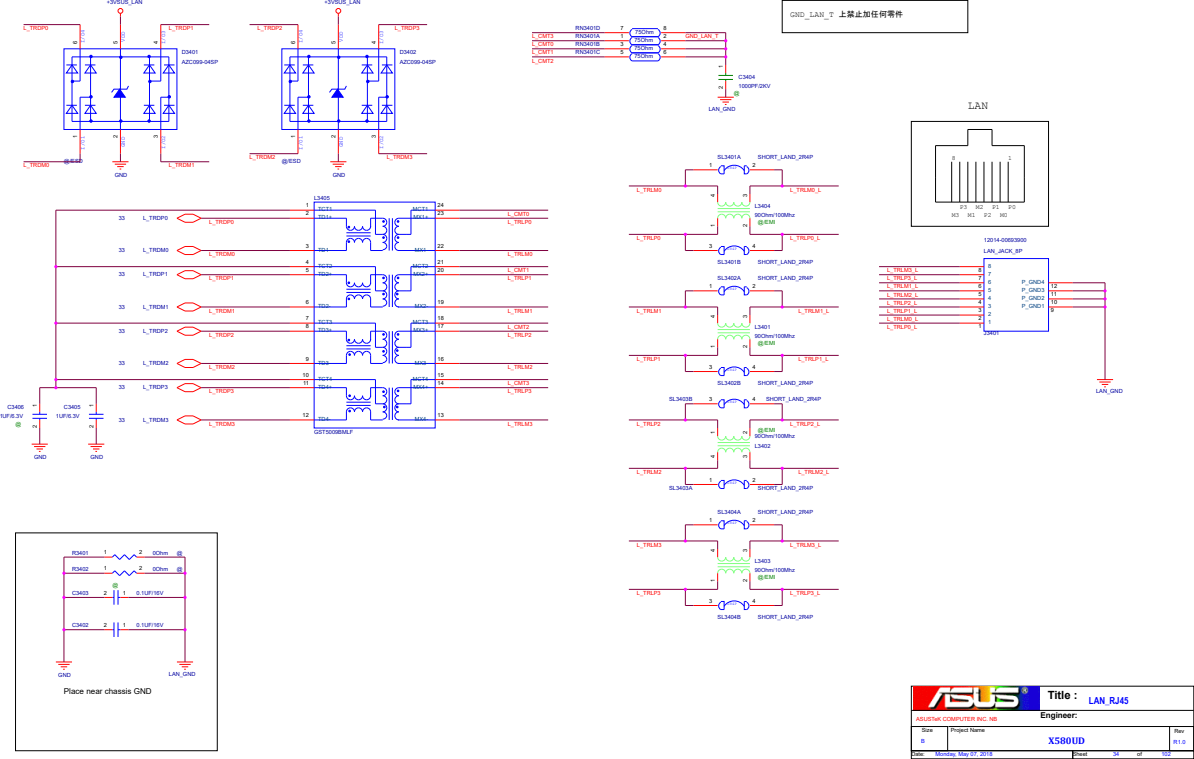


<Variant Name>

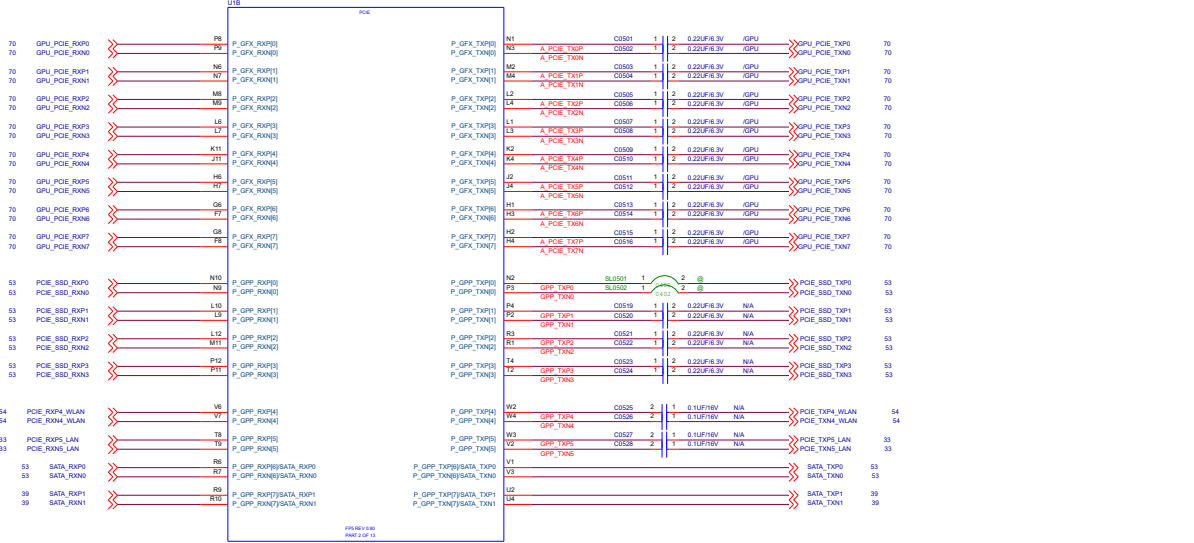
ASUSTeK COMPUTER INC.	Title : SB_DEBUG_LPC	
	Engineer: SZNB2	
Size: A	Project Name: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 24 of 102	



ASUSTeK COMPUTER INC	Title :	LAN_RTL8111HS-CG	
	Engineer:		
Size: B	Project Name:		Rev: R1.0
Date: Monday, May 07, 2018	Sheet 33 of 102		

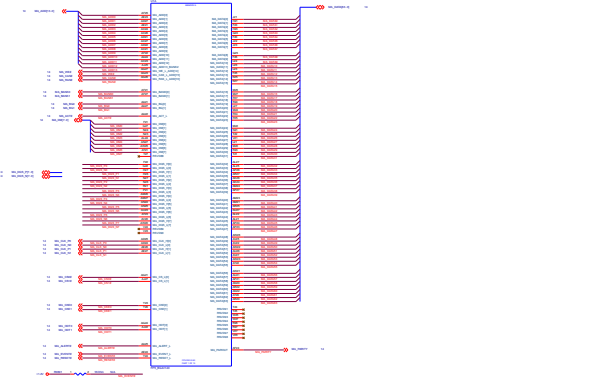


ASUSTeK COMPUTER INC. NB	Title :	LAN_RJ45	
	Engineer:		
Size: B	Project Name:	X580UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet: 34	of: 162	

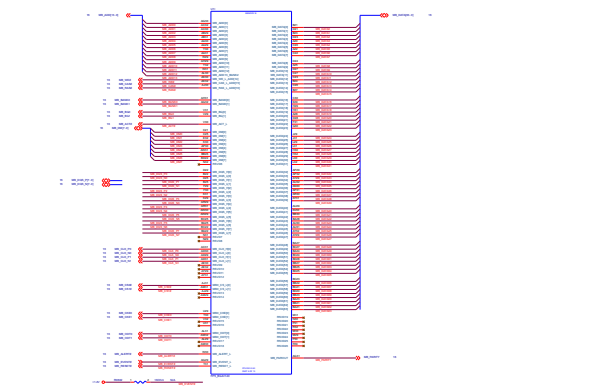


<Variant Name>

ASUS	Project Name: X505ZN	Rev: R0.1
Title :		
Size: B	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, May 07, 2018	Sheet 5 of 99	



EVENT 1K pull up should install, 0328



EVENT 1K pull up should install, 0328

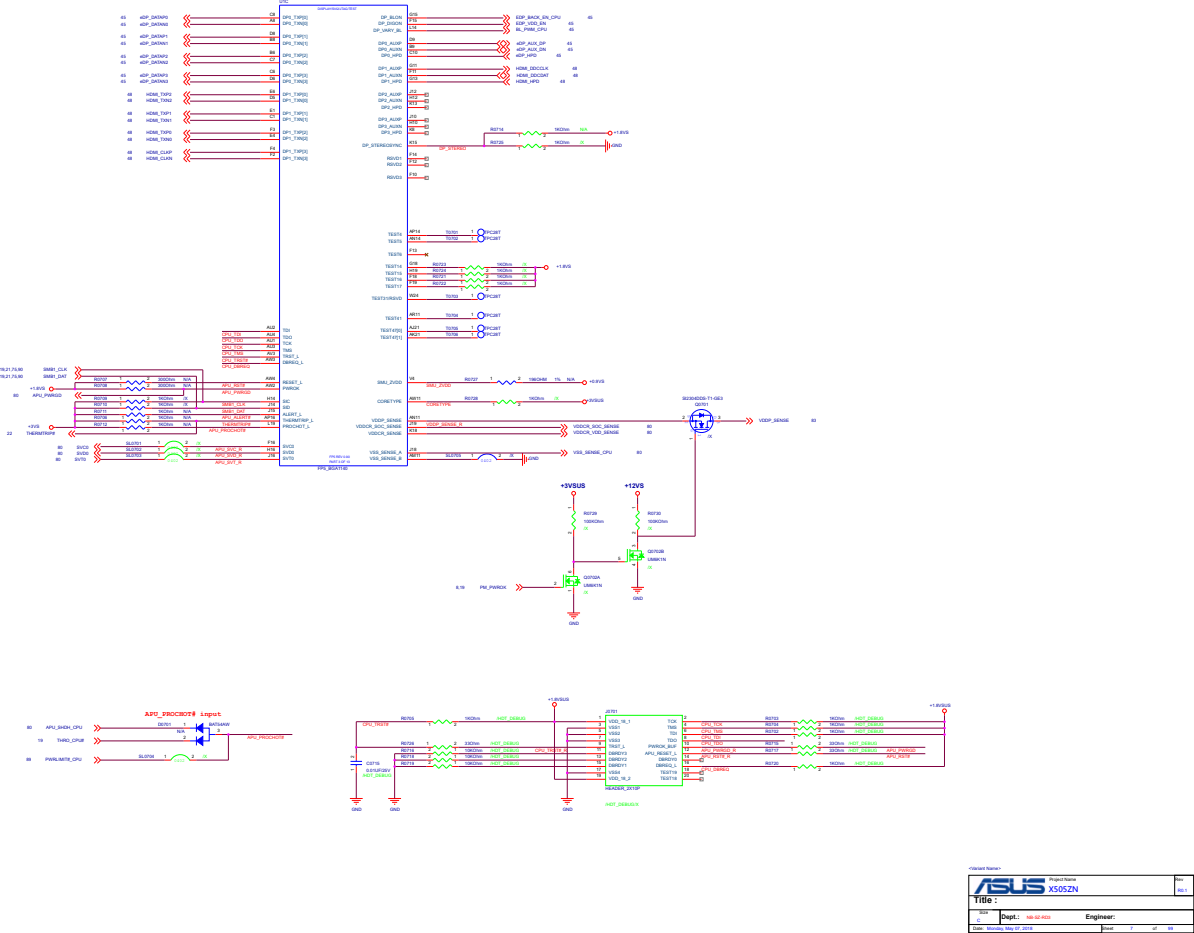
Internal Revision

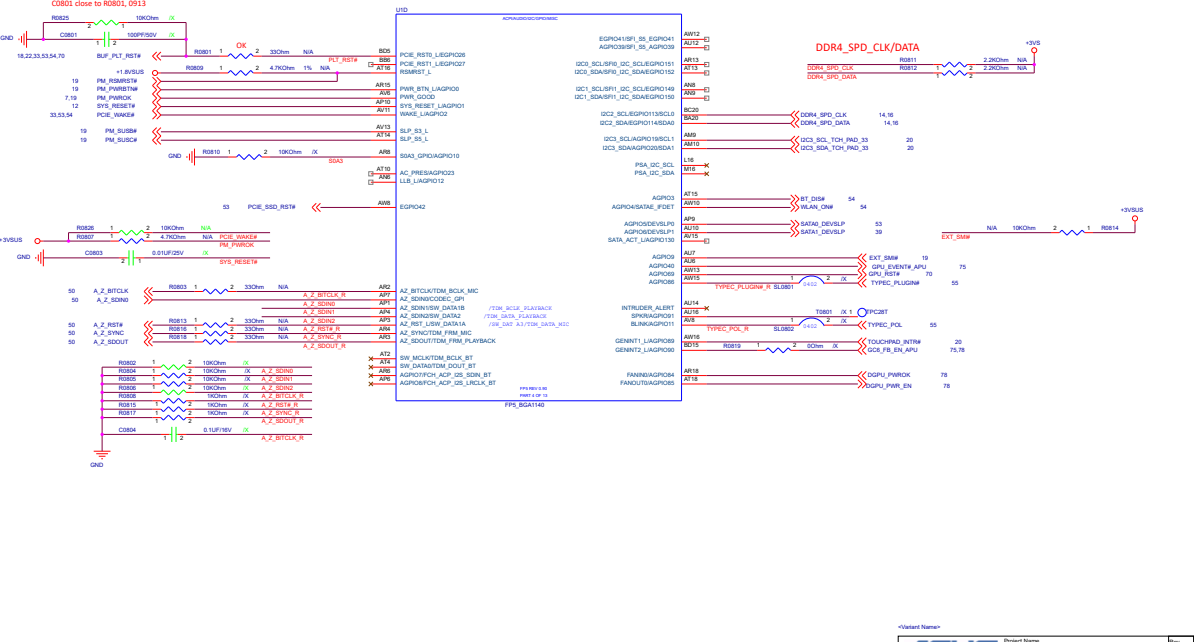
ASUSTeK Computer Inc.

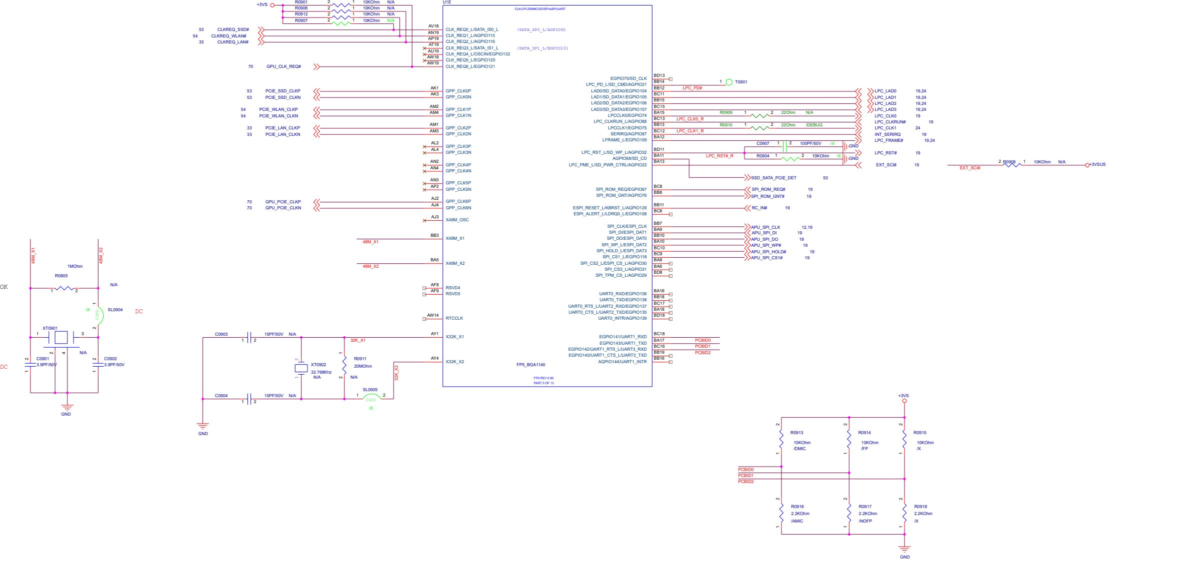
Title :

Size: Project: Rev.XXXX Engineer:

Date: Monday, March 28, 2016 Sheet of

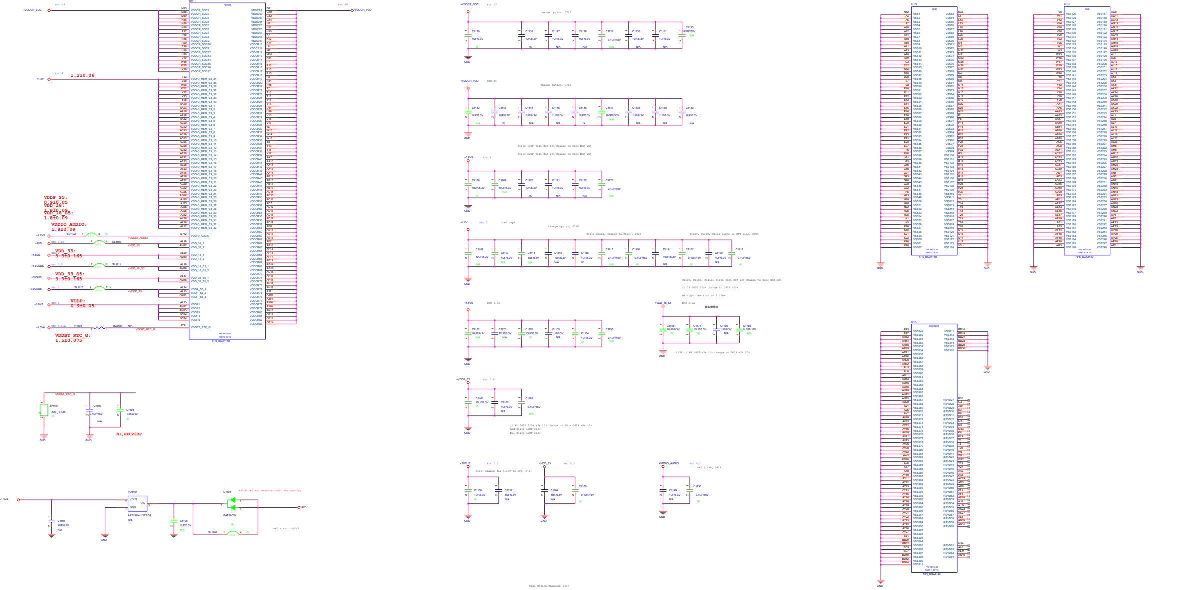

DTC
ADP_DATAP0
ADP_DATAN0
ADP_DATAP1
ADP_DATAN1
ADP_DATAP2
ADP_DATAN2
ADP_DATAP3
ADP_DATAN3
HDMI_TXP2
HDMI_TXN2
HDMI_TXP1
HDMI_TXN1
HDMI_TXP0
HDMI_TXN0
HDMI_CLKP
HDMI_CLKN
DP_TXP[3]
DP_TXN[3]
DP_TXP[2]
DP_TXN[2]
DP_TXP[1]
DP_TXN[1]
DP_TXP[0]
DP_TXN[0]
DP_AUXP
DP_AUXN
DP_HPD
DP_STEREOSYNC
RSVD1
RSVD2
RSVD3
EDP_BACK_EN_CPU
EDP_VDD_EN
BL_PWM_CPU
ADP_AUX_DP
ADP_HPD
HDMI_DDCCLK
HDMI_DDCDAT
HDMI_HPD
TEST4
TEST5
TEST6
TEST14
TEST15
TEST16
TEST17
TEST37/RSVD
TEST41
TEST47[0]
TEST47[1]
SMB_DVDD
CORETYPE
VDDP_SENSE
VDDCR_SOC_SENSE
VDDCR_SENSE
VSS_SENSE_A
VSS_SENSE_B
VDDCR_SOC_SENSE
VDDCR_VDD_SENSE
VSS_SENSE_CPU
VDDP_SENSE
SM3240ADS-T1-GE3
+3VSUS
+12VS
Q57028
UM6K31N
Q57029A
UM6K31N
PM_PWROK
APU_PROCHOT# input
APU_SHDN_CPU
THRO_CPU#
PWRLIMITE_CPU
APU_PROCHOT#
CPU_TEST8
CPU_TCK
CPU_TMS
CPU_TDO
CPU_TDI
APU_RESET_L
APU_PWRGD
SMB1_CLK
SMB1_DAT
SIC
SID
ALERT_L
THERMTRIP_L
PROCHOT_L
APU_PROCHOT#
THERMTRIPPM
SVC
SVD
SVTO
APU_SVC_R
APU_SVD_R
APU_SVT_R
PPVCC_S0A3_CPU
PPVDD_S0A3_CPU
PPVDDCR_S0A3_CPU
PPVDDCR_SOC_S0A3_CPU
PPVDDP_S0A3_CPU
PPVDDCR_S0A3_CPU
PPVDDCR_SOC_S0A3_CPU
PPVDDP_S0A3_CPU
JDT01
HEADER_2X10P
+1.8VSUS
+1.8VSUSB
CSTT5
0.01UF/25V
HOT_DEBUG
HOT_DEBUG/X
Project Name
X505ZN
Rev
R0.1
Title :
Dept.:
Engineer:
Date: Monday, May 07, 2018
Sheet 7 of 59


C0801 close to R0801, 0913
UTID
ACPI/AUDIO/I2C/GPIO/MISC
FP5_BGA1140
DDR4_SPD_CLK/DATA
+3VS
+3VSUS
PLT_RST#
SYS_RESET#
PM_PWROK
PCIE_WAKE#
SDA3
PCIE_SSD_RST#
A_Z_BITCLK
A_Z_SDIN0
A_Z_SDIN1
A_Z_SDIN2
A_Z_RST#
A_Z_SYNC
A_Z_SDOUT
GND



<Variant Name>

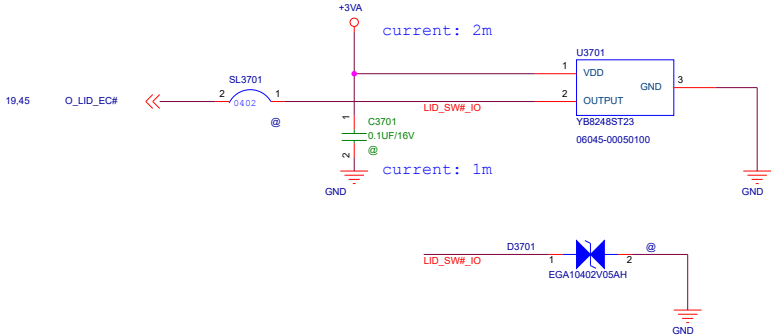
ASUS	Project Name X505ZN	Rev R0.1
Title :		
Size C	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, May 07, 2018	Sheet 9 of 99	



<Variant Name>

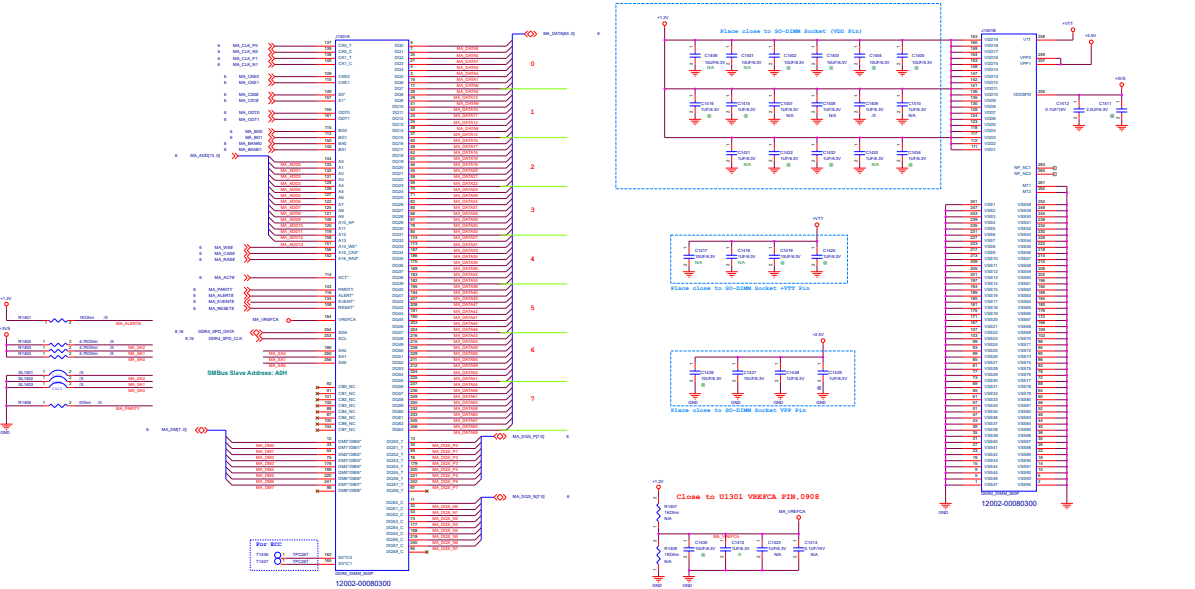
ASUS	Project Name X505ZN	Rev R0.1
Title :		
Size D	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, May 07, 2018	Sheet 11 of 99	

Hall effect switch



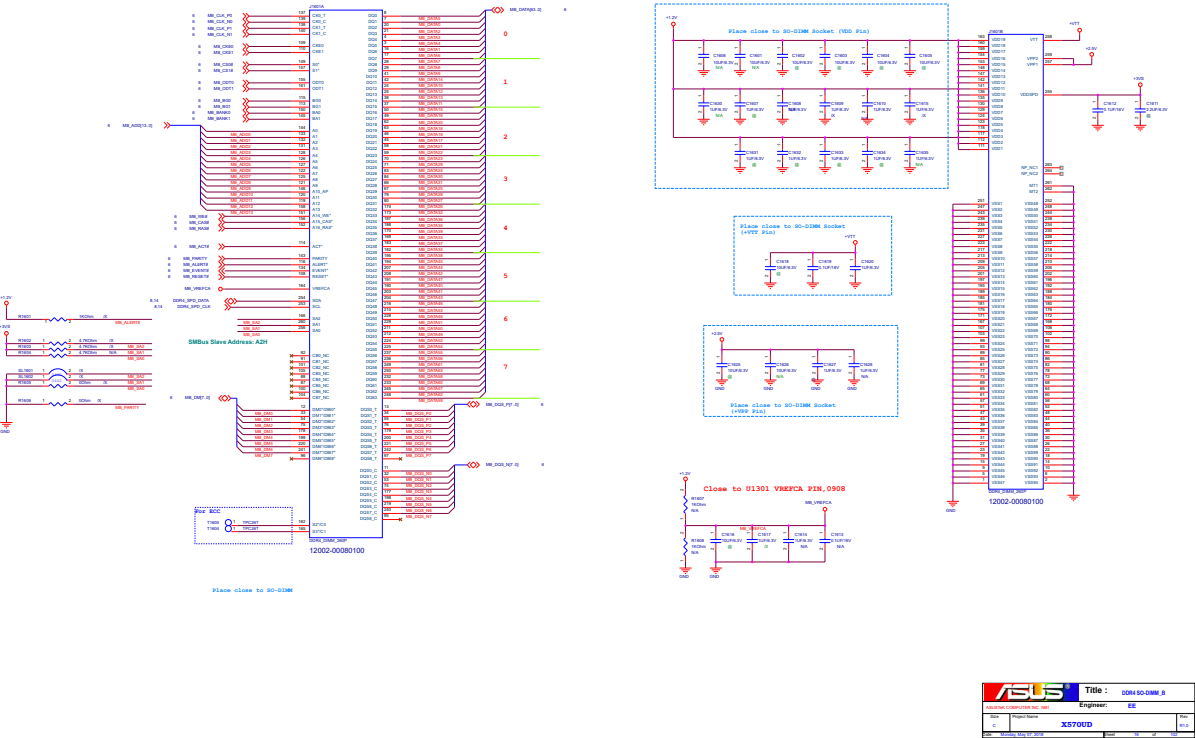
ASUSTeK COMPUTER INC.	Title : Hall sensor		
	Engineer: SZNB1		
Size: A	Project Name: X570UD		Rev: R1.0
Date: Monday, May 07, 2018	Sheet 37 of 102		

DIMM A STD 12002-00080300

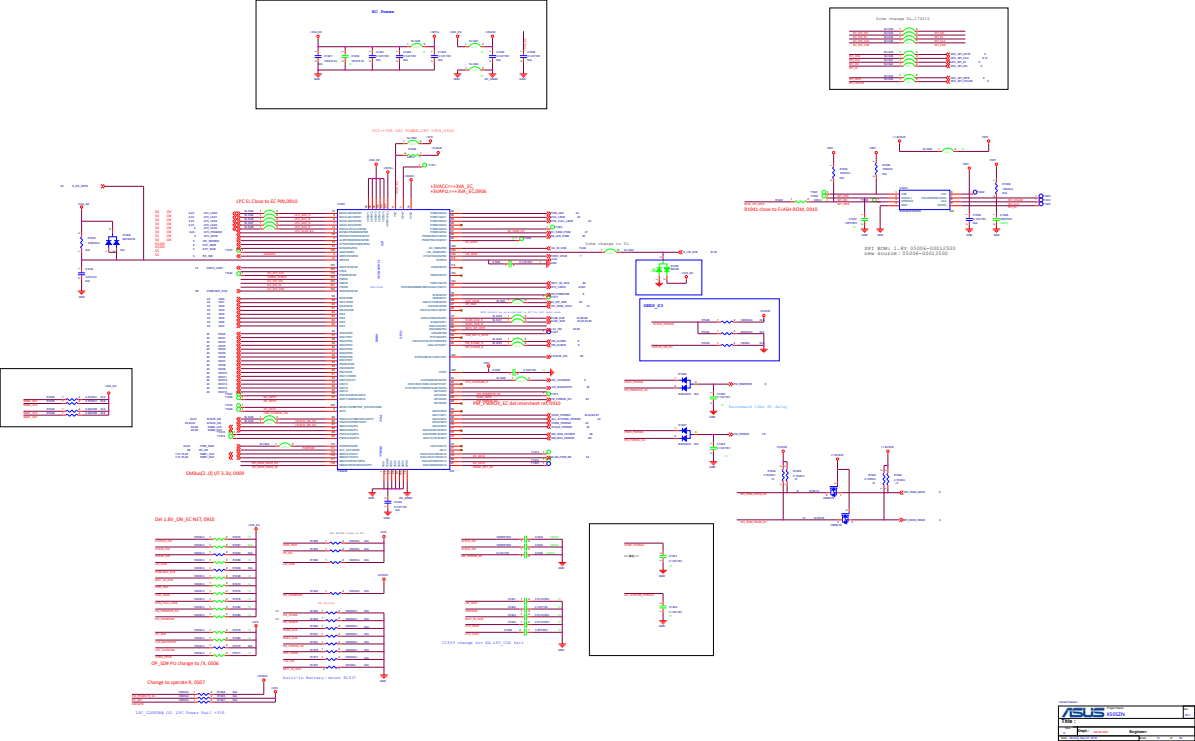


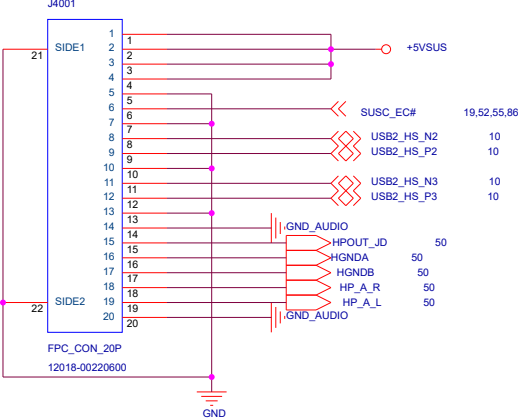
ASUSTeK COMPUTER INC.	Title :	DDR4 SO-DIMM-A	
	Engineer:	EE	
Size	Project Name		Rev
A	X570UD		R3.0
Date: Monday, May 07, 2018	Sheet	16 of 56	

DIMM B rev 12002-00080100



Title :	DDR4 SO-DIMM_B
Engineer:	EE
Size	C
Project Name	XS70UD
Rev	AY.0
Date:	Monday, May 07, 2018
Sheet	10 of 100

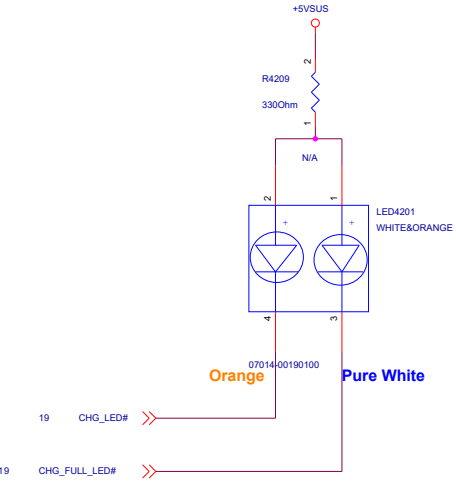

EC Power
Color change ECL170210
VCC=+3V EC POWER,CPU =3V3_S5V0
+3VALW_EC
+3VSPI_EC
LPC SL Close to EC PIN,0910
R1041 close to FLASH ROM, 0910
SPI ROM: 1.8V 05004-00012500
new source: 05004-00013500
Color change to ECL
DEBUG_EC
Recommend 10ms RC delay
HOT PINBOX_EC dot interchart with CPU
SMBus(2..0) UP 3.3V, 0908
Dot 1.8V_ON_EC NOT, 0910
OP_SDM Pin change to 7K, 0506
Change to operate R, 0507
Built-in Battery: remove 80407
CLOCK change for Dot LPC CLK fail
LPC_CLKRUN# GL LPC Power Rail: +3VS



<Variant Name>

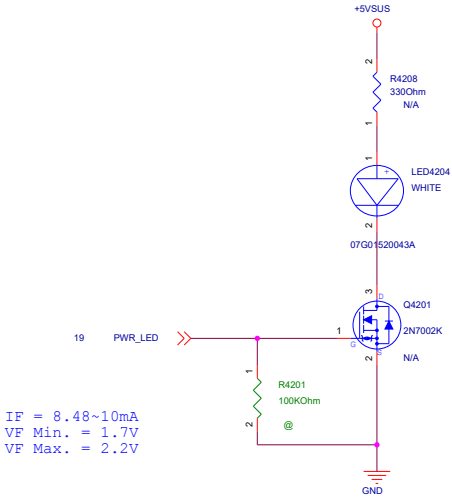
ASUS	Project Name: X570UD	Rev: R1.0
Title : MB_IO_CONN		
Size: A	Dept.: ASUSTeK COMPUTER INC. (ENG)	Engineer: SZ-NB2
Date: Monday, May 07, 2018	Sheet 40 of 102	

Charger LED

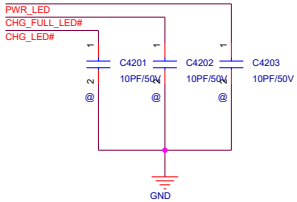


IF = 25mA
VF Min. = 1.7V
VF Max. = 2.4V

POWER LED

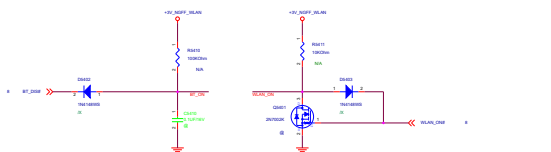


IF = 8.48~10mA
VF Min. = 1.7V
VF Max. = 2.2V

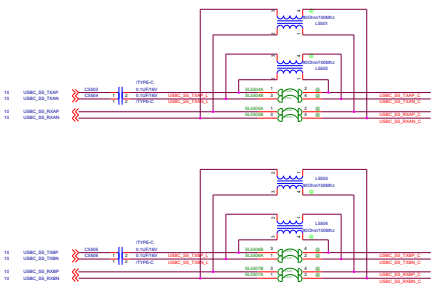


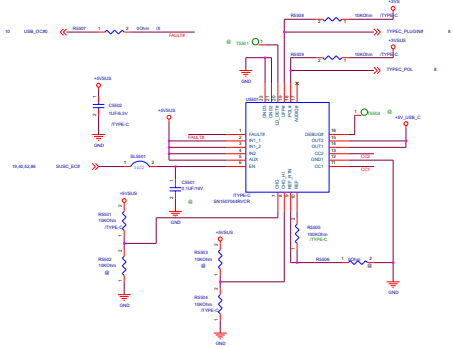
ASUSTeK COMPUTER INC. NB3	Title : MB_LED	
	Engineer: SZNB2	
Size: A	Project Name: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 42 of 102	

NGFF KEYA WIFI



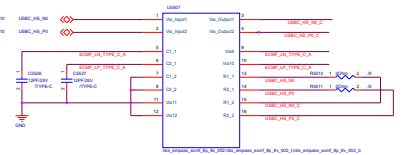
74	3.3Vaux	RESERVED	75
72	3.3Vaux	RESERVED	73
70	RESERVED	GND	69
68	RESERVED	Reserved/2nd Lane PERn1	67
66	RESERVED	Reserved/2nd Lane PERp1	65
64	GPIO0/NFC Reset# (MGPIO7) (O)(I)/(3.3V)	GND	63
62	NFC I2C IRQ (MGPIO5) (I)(I)/3.3)	Reserved/2nd Lane PETn1	61
60	NFC I2C SKY (CLK (O)(I)/3.3)	Reserved/2nd Lane PETp1	59
58	NFC I2C SM DATA (I(O)(I)/3.3)	GND	57
56	W_DISABLE#1 (O)(I)/3.3V)	PERstA#(O)(I)/3.3V)	55
54	Reserved/W_DISABLE#2 (O)(I)/3.3V)	CLKREQ#(I(O)(I)/3.3V)	53
52	PERST#(I)(I)/3.3V)	GND	51
50	SUSCLK(32kHz) (O)(I)/3.3V)	REFCLKN0	49
48	COEX1 (?)(I)/1.8V)	REFCLKP0	47
46	COEX2(?)(O)/1.8V)	GND	45
44	COEX3(?)(O)/1.4V)	PERn0	43
42	CLink CLK	PERp0	41
40	CLink DATA	GND	39
38	CLink RESET (O)(I)/1.8V)	PETn0	37
36	UART CTS (I)(O)/1.8V)	PETp0	35
34	UART RTS (I)(O)/1.8V)	GND	33
32	UART Tx (O)(I)/1.8V)	Key	
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I)(O)/1.8V)	SDIO Reset(O)(I)/1.8V)	23
20	UART Wake (I)(O)/3.3V)	SDIO Wake#(I)(O)/1.8V)	21
18	GND	SDIO DATA(4)(I)(O)/1.8V)	19
16	LED#2 (I)(OD)	SDIO DATA(2)(I)(O)/1.8V)	17
14	PCM_OUT (I)(O)/1.8V)	SDIO DATA(3)(I)(O)/1.8V)	15
12	PCM_IN (O)(I)/1.8V)	SDIO DATA(1)(I)(O)/1.8V)	13
10	PCM_SYNC (I)(O)/1.8V)	SDIO CMD(I)(O)/1.8V)	11
8	PCM_CLK (I)(O)/1.8V)	SDIO CLK(I)(O)/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3Vaux	USB_D-	5
2	3.3Vaux	USB_D+	3
		GND	1

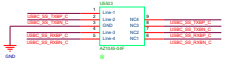


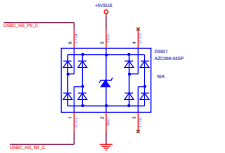


CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

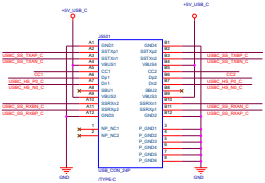
USB2.0 EMI-Protection E-CMPASS Filter





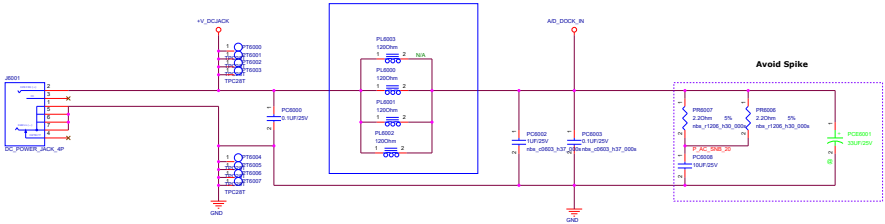


TypeC Conn.

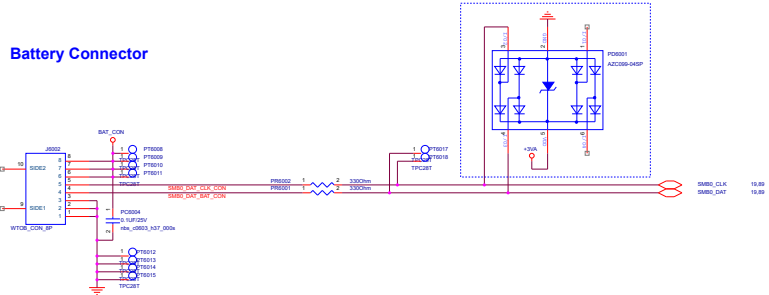


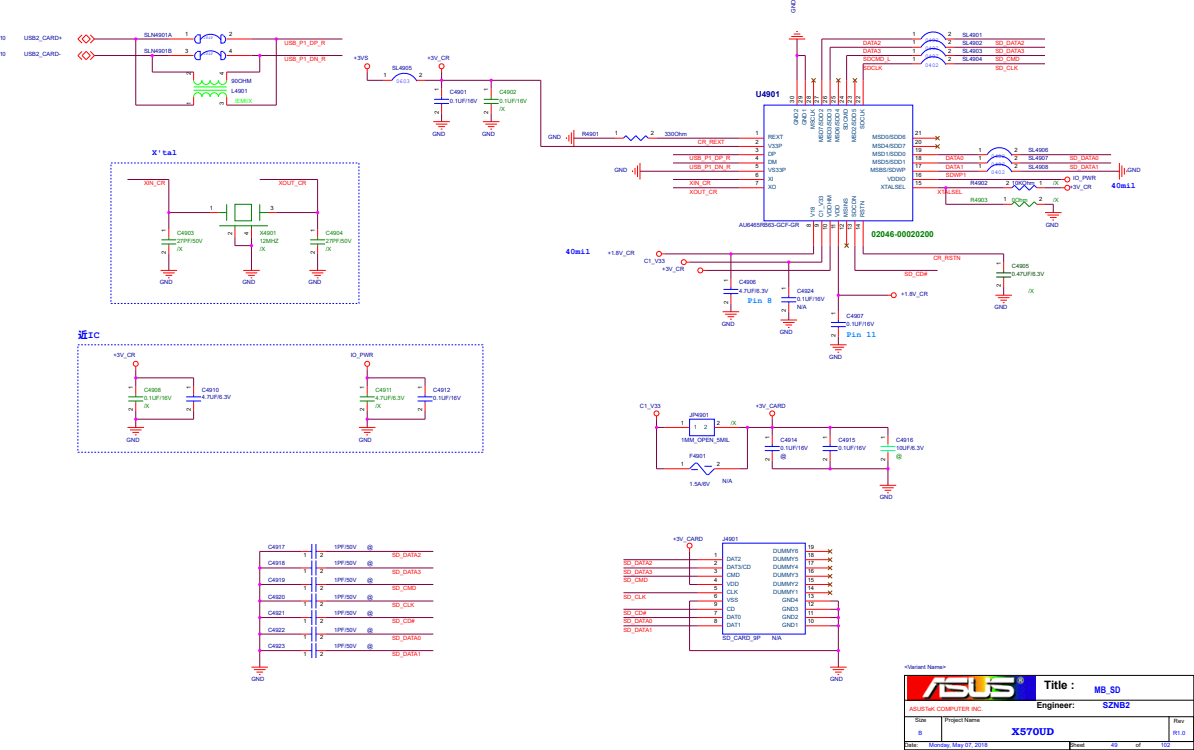
0603 Bead rule:
33W:Bead*2;
45W,65W : bead* 3;
90W,120W,150W:Bead*4;
180W,230W: bead*6

DC Jack

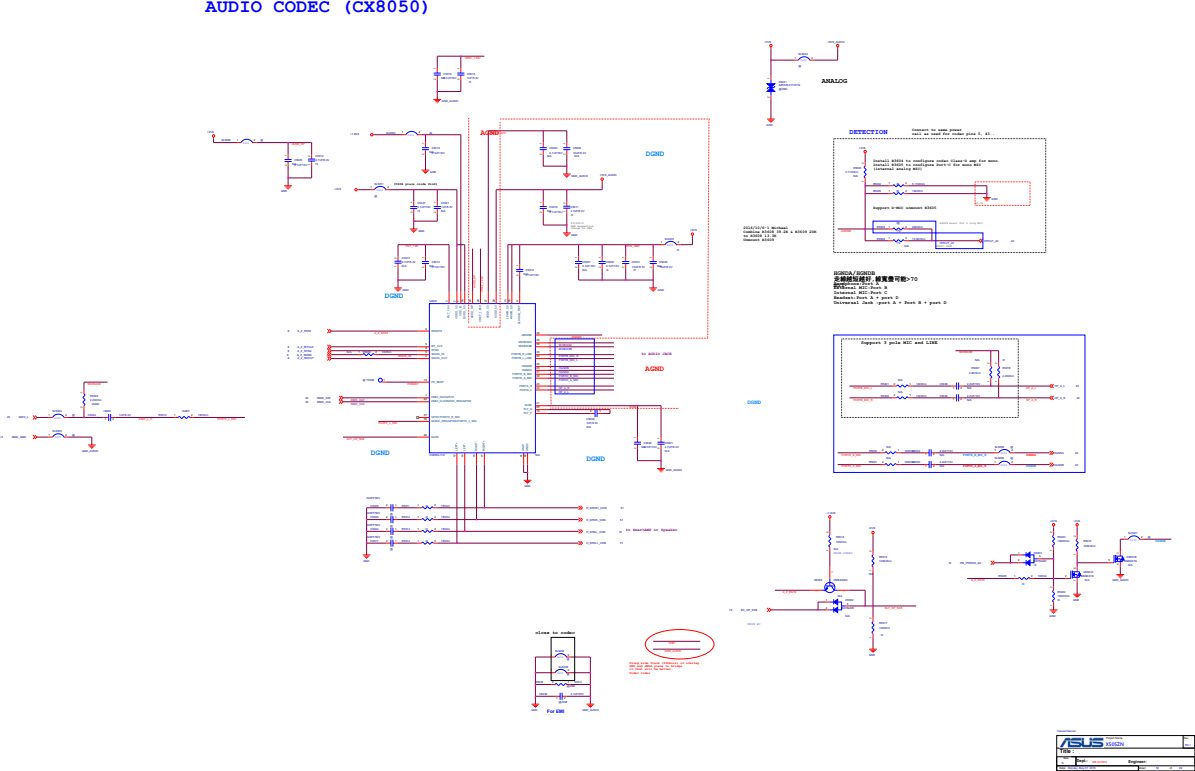


Battery Connector



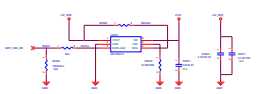

USB2_CARD+
USB2_CARD-
SLN4901A
SLN4901B
90OHM
L4901
/EMIX
USB_P1_DP_R
USB_P1_DN_R
+3VS
SL4905
+3V_CR
C4901
0.1UF/16V
C4902
0.1UF/16V
GND
U4901
R4901
330Ohm
CR_REXT
USB_P1_DP_R
USB_P1_DN_R
XIN_CR
XOUT_CR
DATA2
DATA3
SDCMD_L
SDCLK
SL4901
SL4902
SL4903
SL4904
SD_DATA2
SD_DATA3
SD_CMD
SD_CLK
MSD0/SDD6
MSD4/SDD7
MSD1/SDD0
MSD5/SDD1
MSB5/SDWP
VDDIO
XTALSEL
SDWP1
R4902
R4903
IO_PWR
3V_CR
40mil
AU6465RBS3-GCF-GR
02046-00020200
X'tal
C4903
27PF/50V
X4901
12MHZ
C4904
27PF/50V
+1.8V_CR
C1_V33
C4906
4.7UF/6.3V
Pin 8
C4924
0.1UF/16V
N/A
C4907
0.1UF/16V
Pin 11
CR_RSTN
SD_CD#
C4905
0.47UF/6.3V
+1.8V_CR
EMIC
C4908
0.1UF/16V
C4910
4.7UF/6.3V
C4911
4.7UF/6.3V
C4912
0.1UF/16V
JP4901
1MM_OPEN_SMIL
+3V_CARD
C4914
0.1UF/16V
C4915
0.1UF/16V
C4916
10UF/6.3V
F4901
1.5A/6V
N/A
C4917
C4918
C4919
C4920
C4921
C4922
C4923
15PF/50V
SD_DATA2
SD_DATA3
SD_CMD
SD_CLK
SD_CD#
SD_DATA0
SD_DATA1
J4901
SD_CARD_9P
DUMMY6
DUMMY5
DUMMY4
DUMMY3
DUMMY2
DUMMY1
GND4
GND3
GND2
GND1

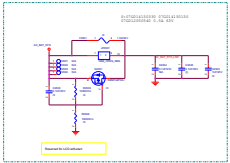
AUDIO CODEC (CX8050)

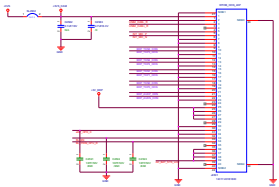


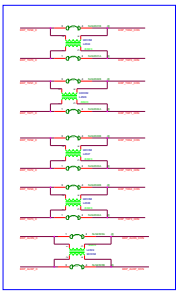
Current Limit vs. R_{LIM} Values

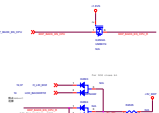
R_{LIM} (Ω)	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
7.68k	2430	2700	2970
8.20k	2250	2500	2750
9.53k	1980	2200	2420
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1350	1500	1650
17.4k	1060	1200	1320
21k	900	1000	1100
34.8k	500	600	700

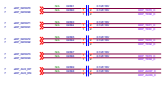


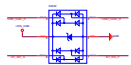


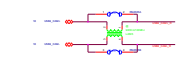












Title :	USB_HDP		
Engineer:	EDMT		
Check	Approved	Rev	
2021/10/20			
Size	Document Number		
A3			

CRT DAC_A

DP(link C)

DVI(link D)

LVDS IFPA/B

LVDS IFPE/F

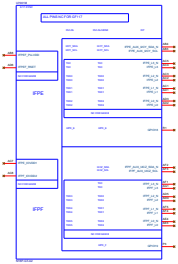


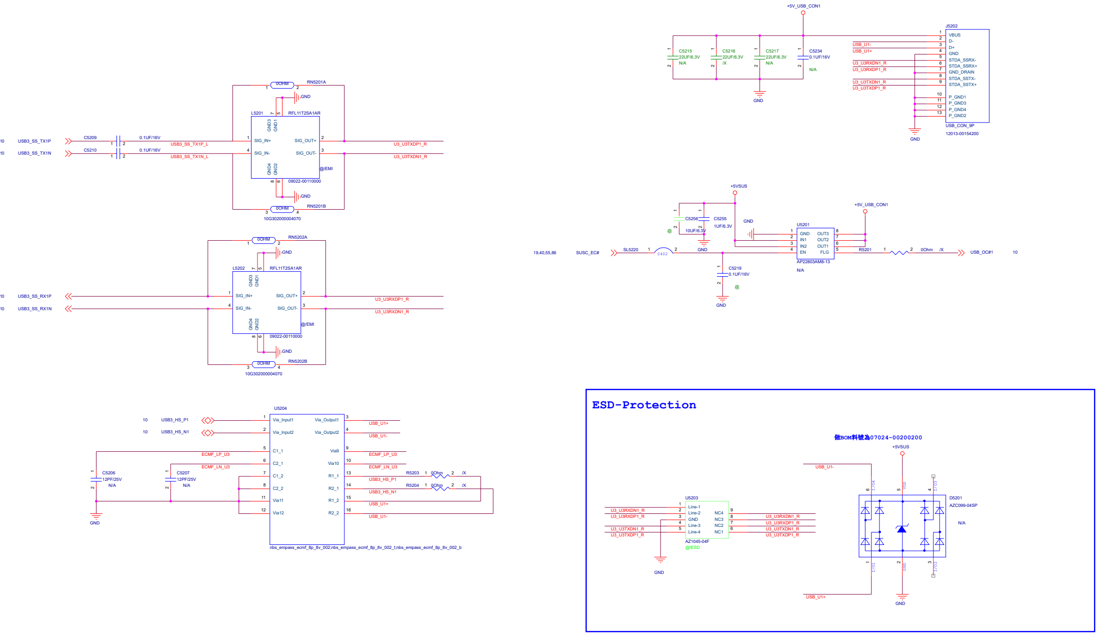
Table 12. N16/GB4B-128 and N17/GB4C-128 GPIO Differences

GPIO Pin	N16 GPU Function	N16 GPU Function on Co-Design	N17 GPU Function	Comments
GPIO0	GC6_FB_EN	PWM_VID	PWM_VID	H17 PWM_VID for HVVDD supply
GPIO1	MEM_VDD_CTL	GC6_FB_EN	GC6_FB_EN	
GPIO2	LCD_BL_PWM	GPU_EVENT#	GPU_EVENT#	
GPIO3	LCD_VCC	TBD	HVVDD5_PWM	H17 PWM_VID for HVVDD5 supply
GPIO4	LCD_BLEH	3V3_MAIN_EH	1V8_MAIN_EH	
GPIO5	3V3_MAIN_EH	FRAME_LOCK#	FRAME_LOCK#	
GPIO6	GPU_EVENT#	PSI	PSI	H17 PSI for HVVDD supply
GPIO7	3D VISION	LCD_BL_PWM	LCD_BL_PWM	
GPIO8	SYS_PEX_RST_IN0 R#	IFPF_HPD	MEM_VDD_CTL	
GPIO9	THERM_ALERT	THERM_ALERT	THERM_ALERT	Same
GPIO10	MEM_VREF_CTL	MEM_VREF_EN	MEM_VREF_CTL	Same
GPIO11	PWM_VID	LCD_VDD	LCD_VDD	
GPIO12	PWR_LEVEL	PWR_LEVEL	PWR_LEVEL	Same
GPIO13	PSI	LCD_BLEH	LCD_BLEH	
GPIO14	HPD_IFPA	GPU_IRTA	HPD_IFPA	Same
GPIO15	HPD_IFPC	HPD_IFPB	HPD_IFPB	
GPIO16	FRAME_LOCK#	SYS_PEX_RST_IN0 R#	RESERVED	
GPIO17	HPD_IFPD	HPD_IFPD	HPD_IFPD	Same
GPIO18	HPD_IFPE	HPD_IFPE	HPD_IFPE	Same
GPIO19	HPD_IFPF or HPD_IFPB	3D VISION	3D VISION	
GPIO20	RESERVED	GPU_HPD	RESERVED	
GPIO21	GPU_PEX_RST_HOLD#	GPU_PEX_RST_HOLD#	RESERVED (OC_WARN)	
GPIO22	-	-	RESERVED	New H17 GPIO
GPIO23	-	-	RESERVED	New H17 GPIO
GPIO24	-	-	HPD_IFPF	New H17 GPIO
GPIO25	-	-	RESERVED	New H17 GPIO
GPIO26	-	-	RESERVED	New H17 GPIO
GPIO27	-	-	HPD_IFPC	New H17 GPIO

I2C ADDRESS: 0x9Eh

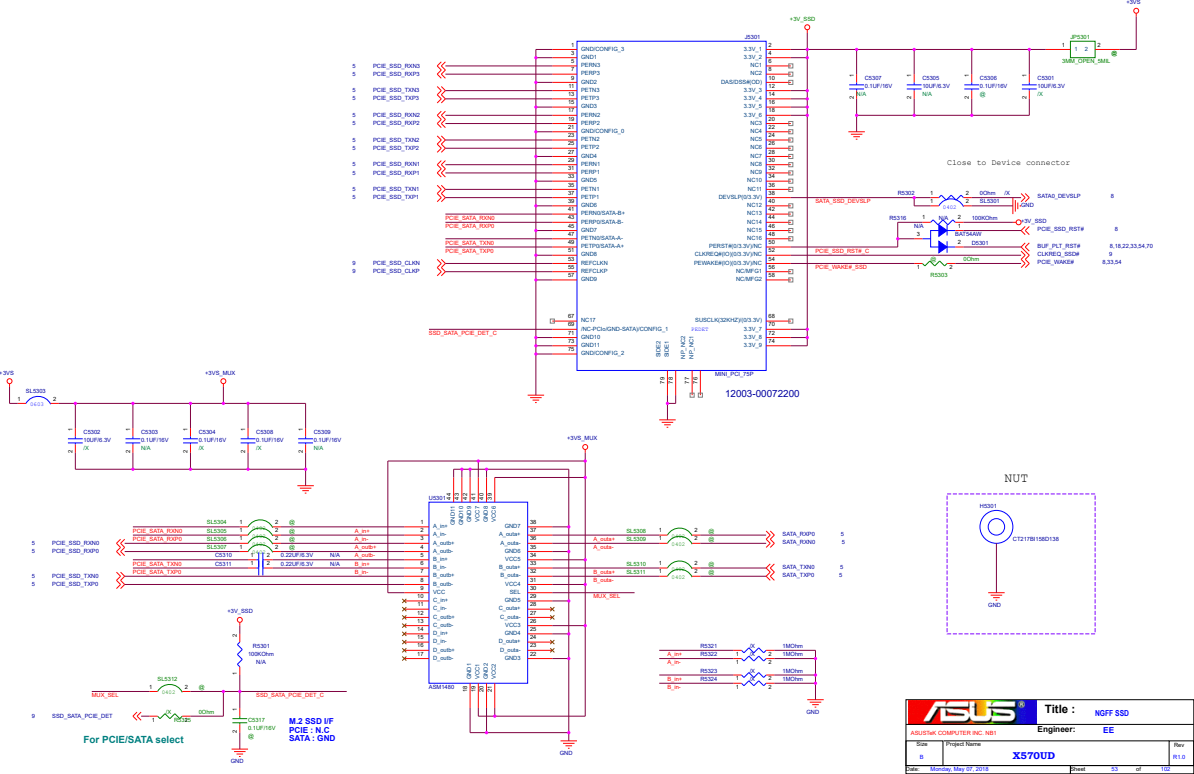
HVVDD POWER GOOD LOOPBACK

USB3.0_Port 0

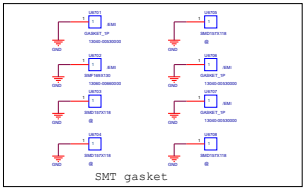


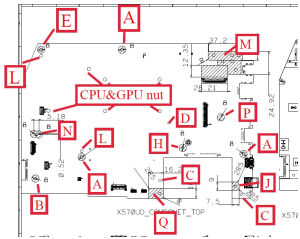
<Variant Name>

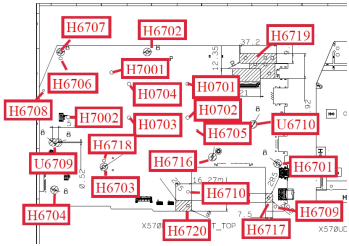
Title :	USB3.0 Port	
ASUSTeK COMPUTER INC. NB4	Engineer:	SZNB1
Size: C	Project Name: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 52 of 102	

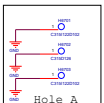


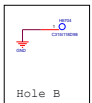
ASUSTeK COMPUTER INC. NB1	Title :	NGFF SSD	
	Engineer:	EE	
Size: B	Project Name: X570UD		Rev: R1.0
Date: Monday, May 07, 2018	Sheet: 53	of: 102	

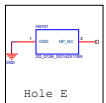


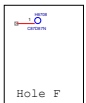


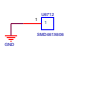


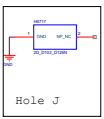


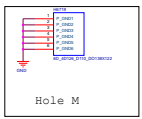


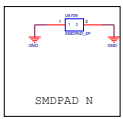


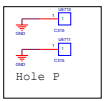


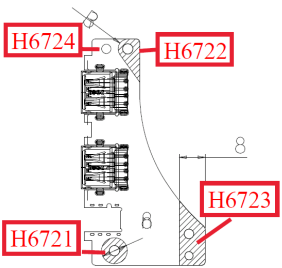


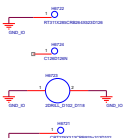


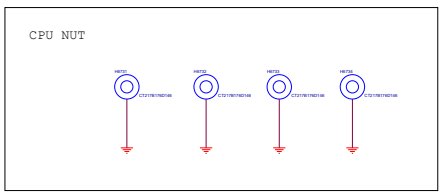


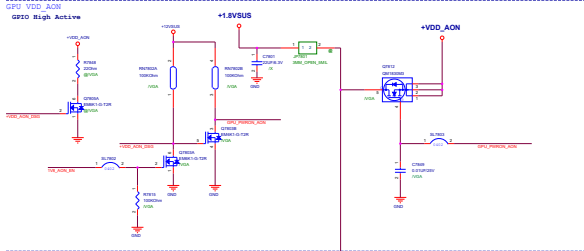


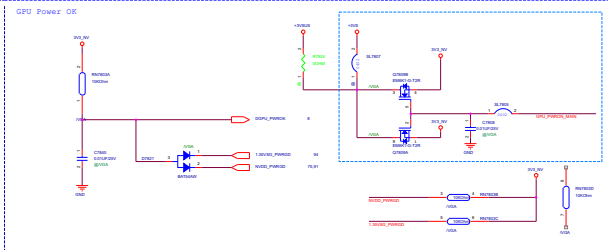


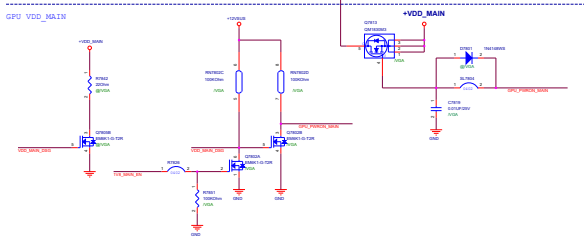


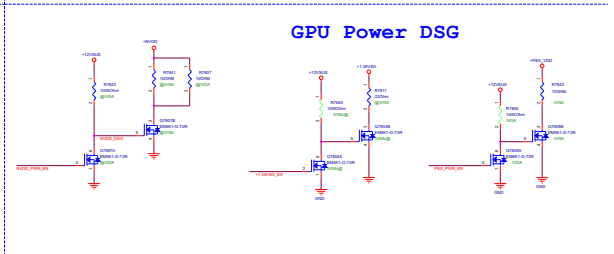




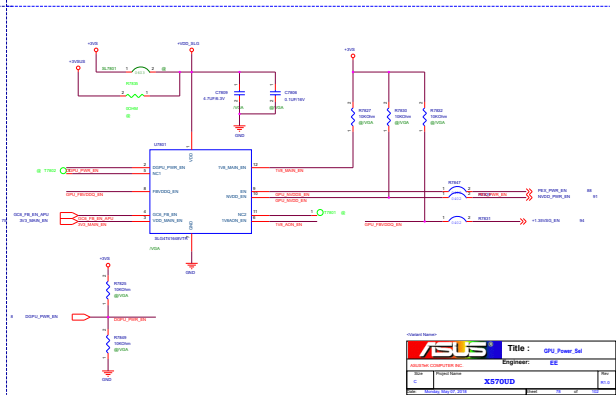

GPU VDD_AON
GPIO High Active
+1.8VSUS
+VDD_AON
+12VSUS
+VDD_AON
GPU_PWRGN_AON
GPU_PWRGN_AON
GPU_PWRGN_AON
GND


GPU Power OK
3V3_RV
+12VSUS
+3VS
3V3_RV
3V3_RV
GPU_PWRGN_MAIN
DGPU_PWRGN
7.35V/5D_PWRGD
5V/3D_PWRGD
5V/3D_PWRGD
7.35V/5D_PWRGD
+3VS
GND


GPU VDD_MAIN
+12VSUS
+VDD_MAIN
VDD_MAIN_EN
GPU_PWRGN_MAIN
GND


GPU Power DSG
+12VSUS
+VDDD
+12VSUS
+1.35VSO
+PEX_VDD
+12VSUS
+PEX_VDD
GND


NVDDS & PEX_VDD ENABLE


+3VS
+VDD_BLU3
+3VSUS
+3VS
U7801
DGPU_PWR_EN
VID_MAIN_EN
GPU_FBVDDQ_EN
FBVDDQ_EN
GPU_AVDDQ_EN
GPU_MVDDQ_EN
GPU_FBVDDQ_EN
VID_AVDDQ_EN
VID_MVDDQ_EN
VID_MAIN_EN
VID_AVDDQ_EN
GPU_PWR_EN
GPU_PWR_EN
+1.35VSO_EN
+3VS
GND

Title : GPU_Power_Sel
Engineer: EE
ASUSTeK COMPUTER INC.
X570UD
Size
Project Name
Rev
Date: Monday, May 07, 2018
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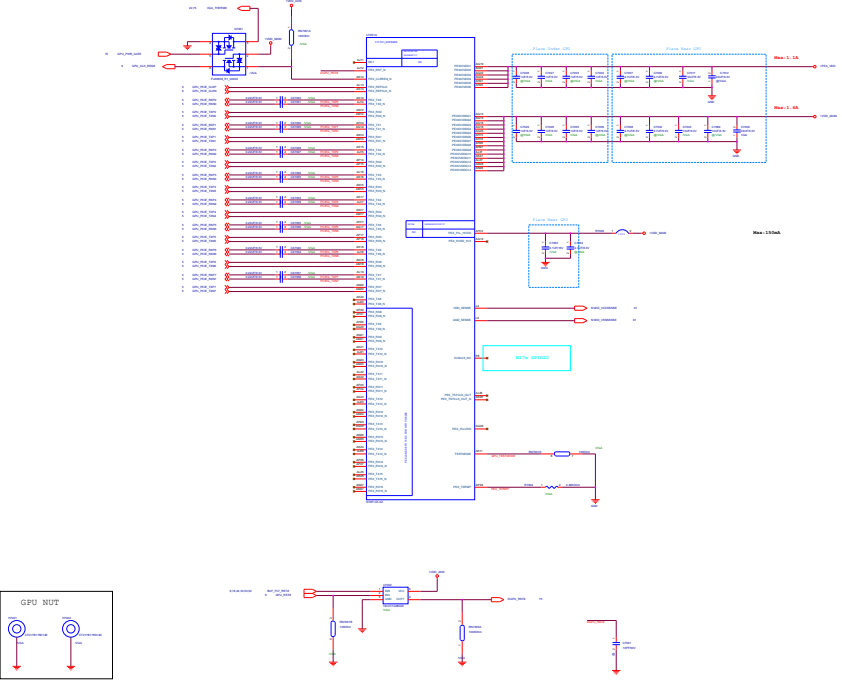


Table 7. N16 and N17 PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_IVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply

Table 8. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail					
GB4B-128	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB4B-128	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB4B-128, GB4C-128	0.1 µF	X2R	0402	1	1	Near GPU

GPU MEMORY INTERFACE: PARTITION A

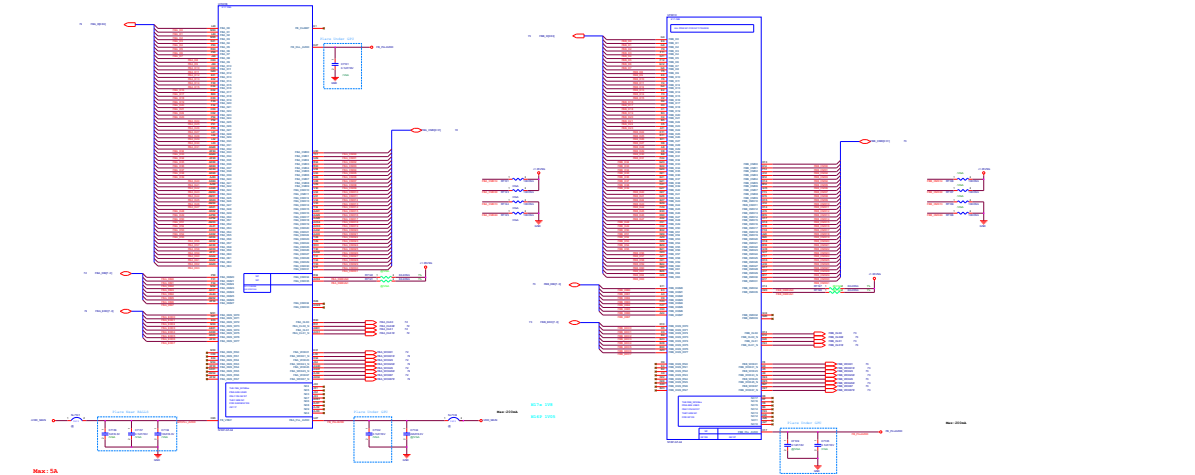


Table 5. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDDQ Supply Rail for GDDR5					
GB4B-128, GB4C-128	0.1 µF	X6S	0402	4	0	Under GPU
	1 µF	X6S	0402	4	12	Under GPU
	4.7 µF	X6S	0603	4	8	Under GPU
	10 µF	X6S	0603	0	4	Under GPU
	10 µF	X6S	0603	2	0	Near GPU
	22 µF	X6S	0603M	0	10	Near GPU

Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_AUX	0.1µF	16V	0402	2	2	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB1-256		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64	3V3_AON	0.1µF	16V	0402	1	1	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB1-256		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-N1I mode. For N1I mode, please refer to the MIO Decoupling table.

FBA Partition Memory (1 of 2)

FBA Partition Memory (2 of 2)

CMD mapping mode H

GB2-64 GB4-128*	CH0 0...31
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	ABI#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#

MF=0 Normal

MF=1 Mirror

CMD mapping mode H

GB2-64 GB4-128*	CH1 32...63
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	ABI#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#

MF=1 Mirror

03008-00030300

03008-00030300

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	VDDQ	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

ASUS

Title : GPU GDDR5A

Engineer: EE

ASUSTeK COMPUTER INC. TEL

X570UD

Size: C | Project Name | Rev: REV:X

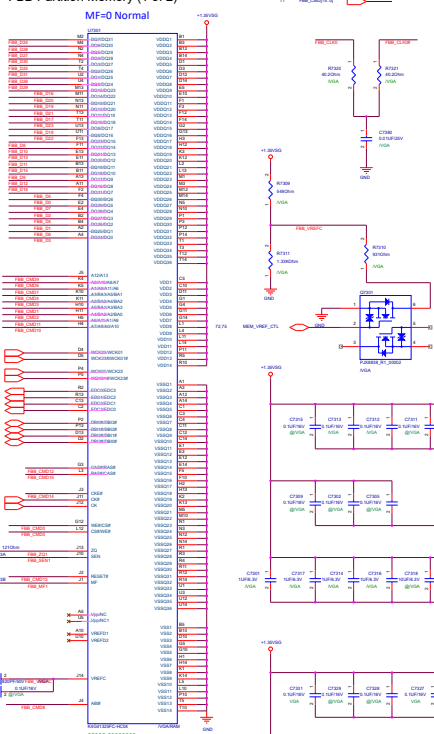
Date: Monday, May 07, 2018 | Sheet 12 of 100

FBB Partition Memory (1 of 2)

MF=0 Normal

CMD mapping mode H

GB2-64 GB4-128*	CH0 0....31
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	ABI#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#

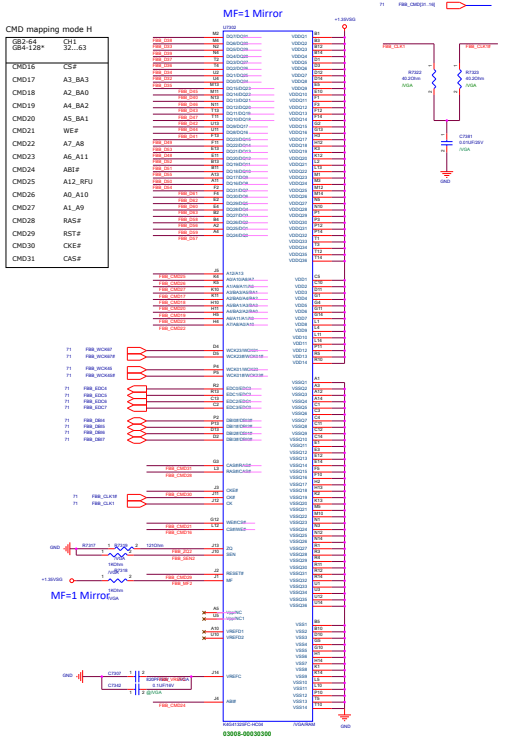


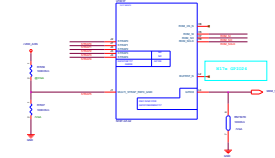
FBB Partition Memory (2 of 2)

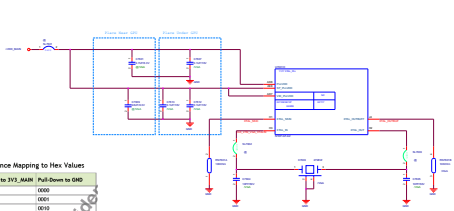
MF=1 Mirror

CMD mapping mode H

GB2-64 GB4-128*	CH1 32...63
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	ABI#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#







N17P Strap PU/PD Resistor must be 100Kohm

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

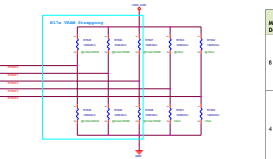


Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Data Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	H/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	H/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	H/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V[2]	Samsung	K4G41325FE-HC28	E-die	0x5	7 Gbps	H/A	Full	Production candidate
		1.35V and 1.5V[2]	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	H/A	Full	Production candidate
		1.35V and 1.55V[2]	Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	H/A	Full	Post production candidate

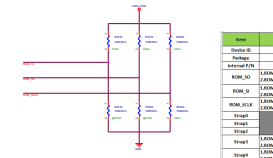
Notes:

1. For N17P-Gx, the maximum allowable memory case temperature is 85 °C.
2. N17P-Gx runs WCLK up to 3000 MHz with FBVDD = 1.35V. DVS is required to run WCLK > 3000 MHz.

GDDR5 RAM_CFG										
GPU SKU	GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memory configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grad	Memory SVC Milestone	Strap	Strap2	Strap1	Strap0	Notes
N17P-G0/G1	G000FS	1.35V and 1.5V	8Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	7 Gbps	N/A	0x0	L	L	L	L	Production Candidate
					Micron	MT51J256M32HF-70:A	A-die	7 Gbps	N/A	0x1	L	L	L	H	Production Candidate
					Hynix	H5GC8H24MJR-R0C	M-die	7 Gbps	N/A	0x2	L	L	H	L	Post Production Candidate
		1.35V and 1.5V			Samsung	K4G41325FE-HC28	E-die	7 Gbps	N/A	0x5	H	H	H	H	Post Production Candidate
N17P-G0/G1	G000FC	1.35V and 1.5V	4Gb	128Mx32	Hynix	H5GC4H24AJR-R0C	A-die	7 Gbps	N/A	0x6	H	H	L	L	Post Production Candidate
		1.35V and 1.55V			Micron	EDW4032BABG-70-F	A-die	7 Gbps	N/A	0x8	L	L	L	H	Post Production Candidate

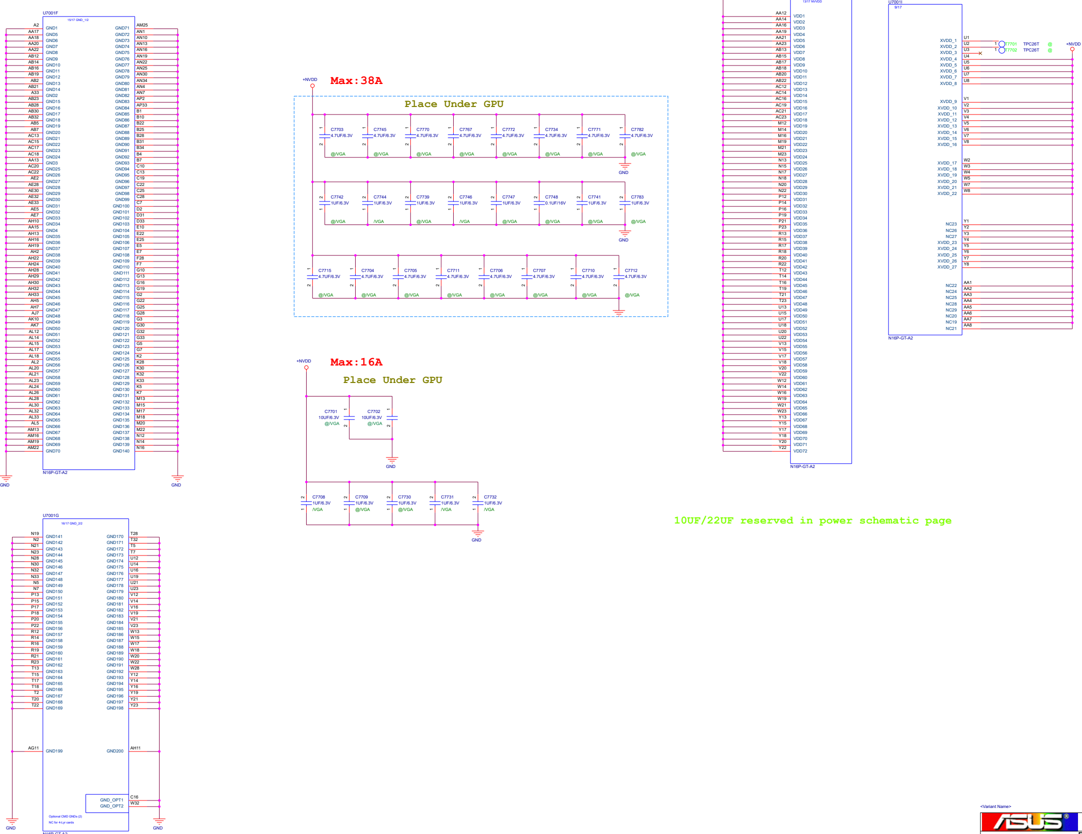
Notes:

3. For N17P-Gx, the maximum allowable memory case temperature is 85 °C.
4. N17P-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.



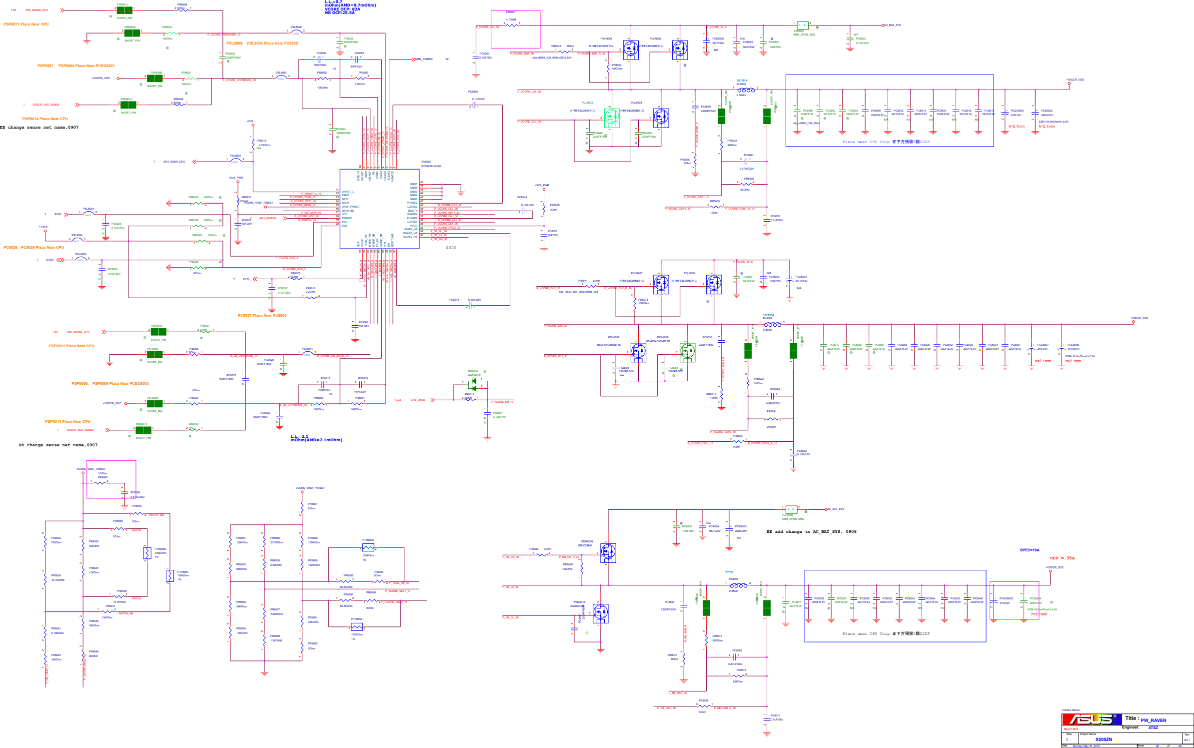
Item	N17P-G0	Options Mode	Discrete Mode
Device ID	0x1C8D, 0x1CC0		
Package	GB4C-256		
Internal PJTK	GP107-725-A1		
ROM_SO	1.8OM Option for 100K PU to 1V8_AON 2.8OM Option for 100K PD to GND	H	TBD
ROM_SI	1.8OM Option for 100K PU to 1V8_AON 2.8OM Option for 100K PD to GND	H	TBD
ROM_SCLK	1.8OM Option for 100K PU to 1V8_AON 2.8OM Option for 100K PD to GND	M	TBD
Strap0	Refer to N17x_RAM_Straps table		
Strap1			
Strap2			
Strap3	1.8OM Option for 100K PU to 1V8_AON 2.8OM Option for 100K PD to GND	L	TBD
Strap4	1.8OM Option for 100K PU to 1V8_AON 2.8OM Option for 100K PD to GND	L	TBD
Strap5	1.8OM Option for 100K PU to 1V8_AON 2.8OM Option for 100K PD to GND	L	TBD
Boot Voltage	0.8V		

NVVDD GROUND



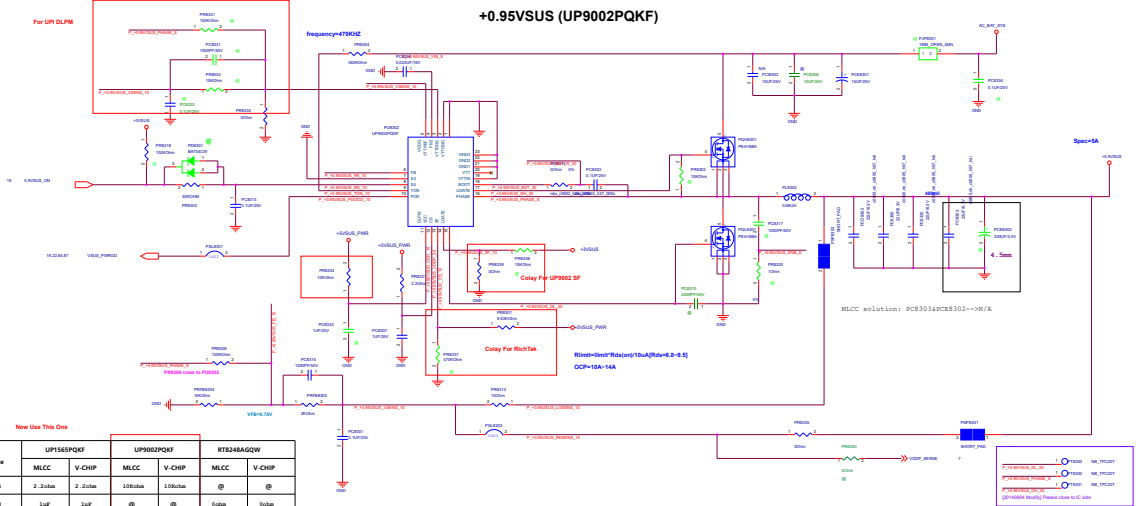
<Variant Name>

ASUSTek Computer Inc.	Title : VGA PWR_GND	
	Engineer: EE	
Size: C	Project Name: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 77 of 102	



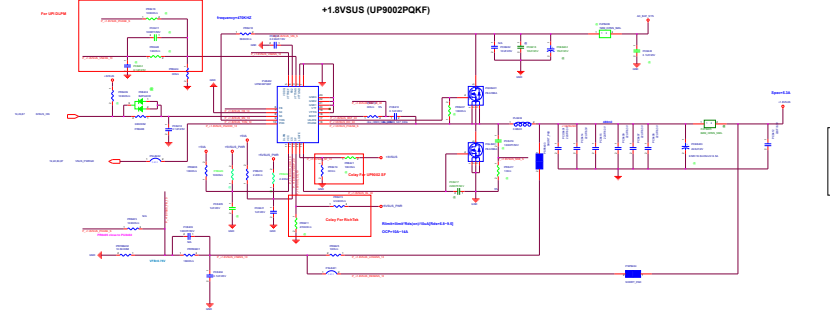
L.L.=0.7
mOhm(AMD=0.7mOhm)
VCORE OCP: 82A
NB OCP:25.5A
PSP8011 Place Near CPU
PSL8008, PSL8000 Place Near PU8000
PSP8007, PSP8006 Place Near PCEO8001
PSP8014 Place Near CPU
EE change sense net name,0907
PC8026, PC8029 Place Near CPU
PC8037 Place Near PU8000
PU8000
RT3662AHGQW
0620
PSP8012 Place Near CPU
PSP8008, PSP8009 Place Near PCEO8003
PSP8013 Place Near CPU
EE change sense net name,0907
L.L.=2.1
mOhm(AMD=2.1mOhm)
Place near CPU Chip 正下方預留5個22UF
EE add change to AC_BAT_SYS, 0908
SPEC=10A
OCP = 35A
Place near CPU Chip 正下方預留5個22UF
Title : PW_RAVEN
Engineer: ATSZ
Project Name
X505ZN
Monday, May 07, 2018

+0.95VSUS (UP9002PQKF)



Part Reference	UP1565PQKF		UP9002PQKF		RT8248AGQW	
	MLCC	V-CHIP	MLCC	V-CHIP	MLCC	V-CHIP
R8334	2.2ohm	2.2ohm	10Kohm	10Kohm	@	@
PC8333	1uF	1uF	@	@	0ohm	0ohm
R8337	@	@	@	@	300Kohm	300Kohm
R8304	820Kohm	820Kohm	560Kohm	560Kohm	620Kohm	620Kohm
R8306	178Kohm	402Kohm	100Kohm	@	178Kohm	@
PC8315	820pF	820pF	1000pF	@	820pF	@
R8301	15Kohm	15Kohm	15Kohm	15Kohm	@	@

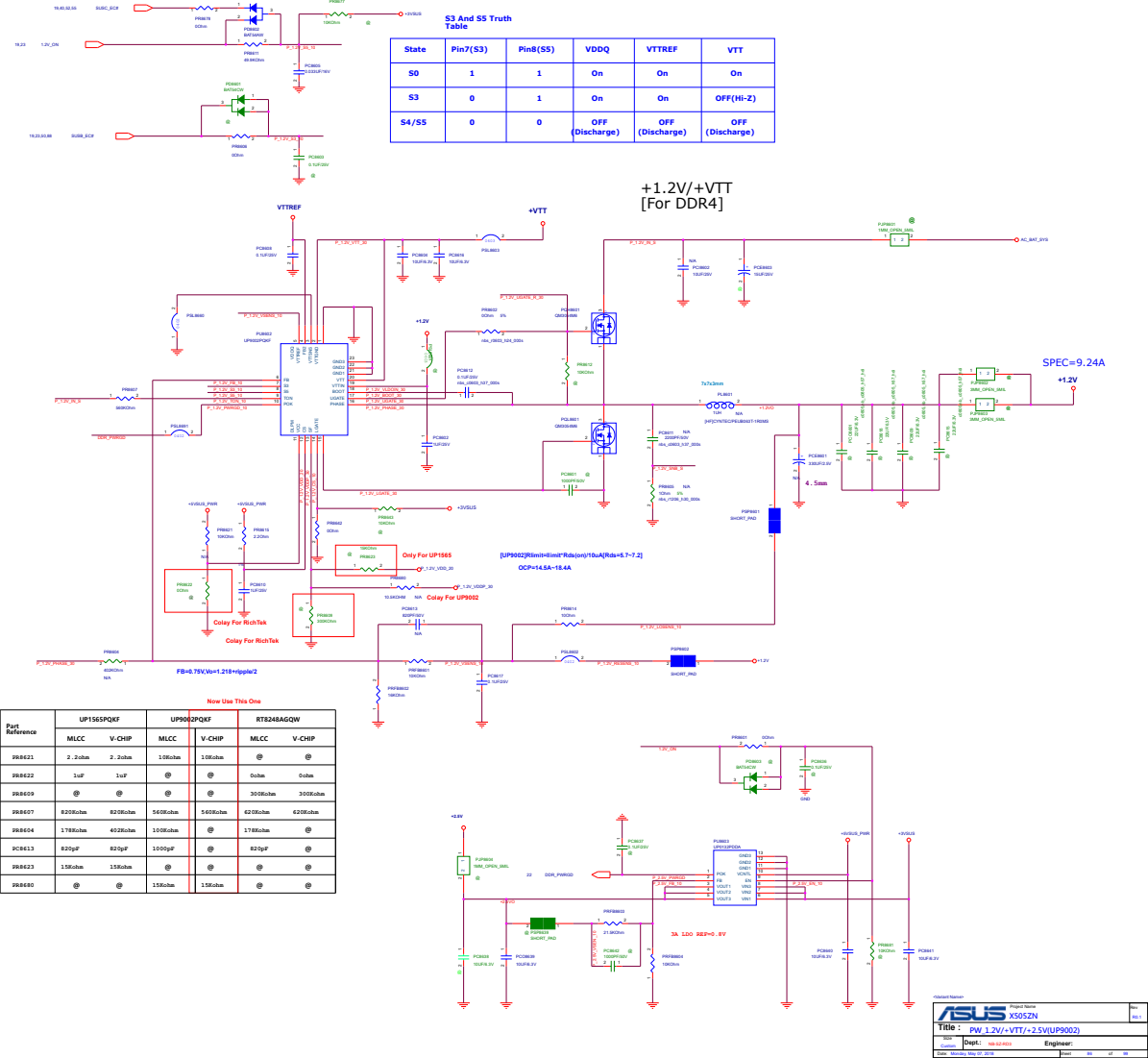
Project Name: X505ZN			Rev: 3.0.1
Title: PW_+1.0VSUS / +1.8VSUS			
Size:	Dept.: MB SZ RD3	Engineer: ATSZ	
Date: Monday, May 07, 2018	Sheet: 60	of: 66	



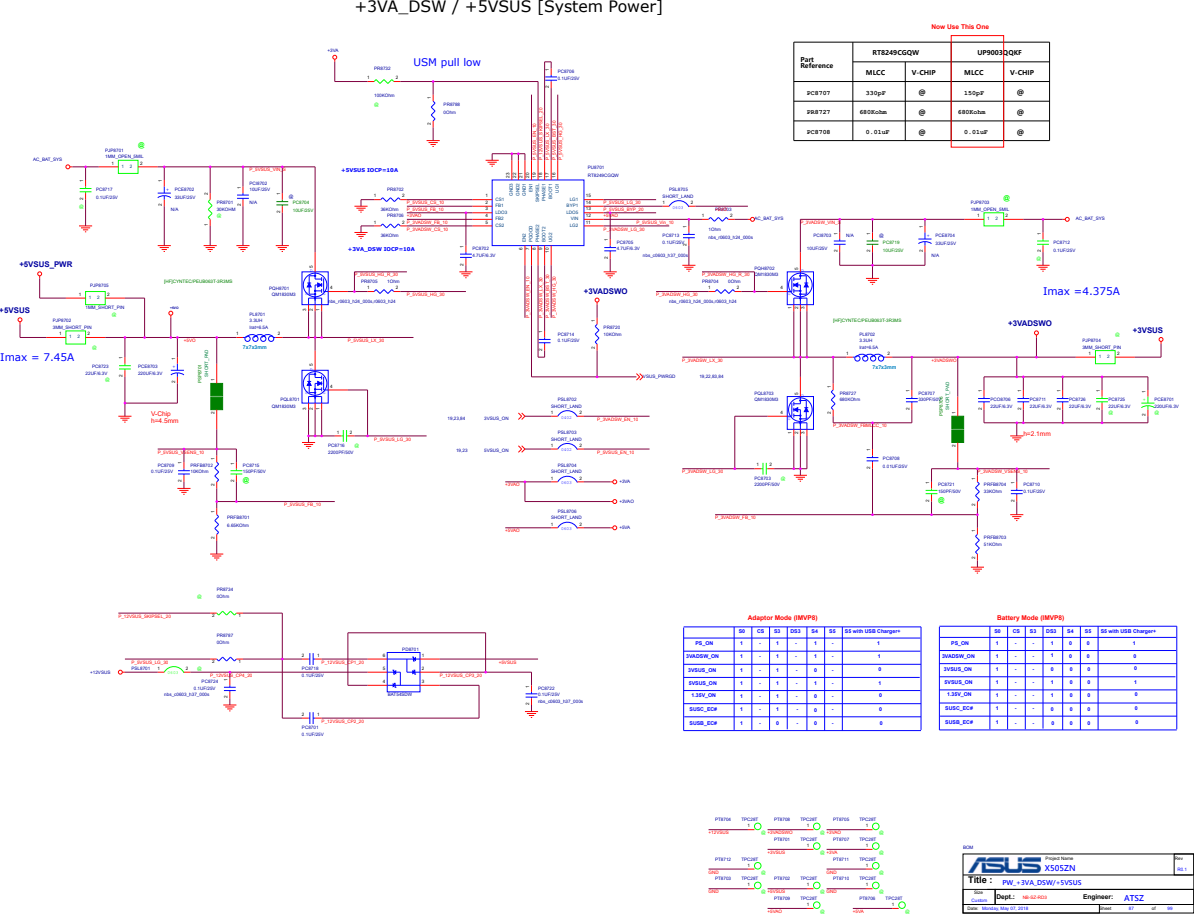
Need 3 be Thin One

Part Reference	UP1536PQKF		UP9002PQKF		RT8268AGQW	
	MLCC	V-CHIP	MLCC	V-CHIP	MLCC	V-CHIP
#48534	4 - 3mm	4 - 3mm	3.9Ohm/m	3.9Ohm/m	@	@
#53023	1nF	1nF	@	@	2n2m	2n2m
#48537	@	@	@	@	330Ohm/m	330Ohm/m
#48534	510Ohm/m	510Ohm/m	750Ohm/m	750Ohm/m	620Ohm/m	620Ohm/m
#48535	4.7Ohm/m	4.02Ohm/m	10Ohm/m	@	4.7Ohm/m	@
#48533	47n/pF	47n/pF	47n/pF	@	47n/pF	@
#48531	1.5Ohm/m	1.5Ohm/m	2.2Ohm/m	2.2Ohm/m	@	@

ASUS	Project Name: X505ZN		Rev:
Title:			
Size:	Document Number:		Rev:
Date:	Sheet of	Engineer	


S3 And S5 Truth Table
State | Pin7(S3) | Pin8(S5) | VDDQ | VTTREF | VTT
S0 | 1 | 1 | On | On | On
S3 | 0 | 1 | On | On | OFF(Hi-Z)
S4/S5 | 0 | 0 | OFF (Discharge) | OFF (Discharge) | OFF (Discharge)
+1.2V/+VTT [For DDR4]
SPEC=9.24A
+1.2V
4.5mm
VTTREF
+VTT
+1.2V
UP9022QKF
UP1565PQKF
Only For UP1565
Colay For UP9002
Colay For RichTek
Colay For RichTek
[UP9002]Rlimit=Rlimit*Rds(on)/10uA[Rds=5.7~7.2]
OCP=14.5A~18.4A
FB=0.75V,Vo=1.218+ripple/2
Now Use This One
3A LDO REF=0.8V
Part Reference | UP1565PQKF | | UP9002PQKF | | RT8248AGQW | |
MLCC | V-CHIP | MLCC | V-CHIP | MLCC | V-CHIP
PR8621 | 2.2ohm | 2.2ohm | 10Kohm | 10Kohm | @ | @
PR8622 | 1uF | 1uF | @ | @ | 0ohm | 0ohm
PR8609 | @ | @ | @ | @ | 300Kohm | 300Kohm
PR8607 | 820Kohm | 820Kohm | 560Kohm | 620Kohm | 620Kohm | 620Kohm
PR8604 | 178Kohm | 402Kohm | 100Kohm | @ | 178Kohm | @
PC8613 | 820pF | 820pF | 1000pF | @ | 820pF | @
PR8623 | 15Kohm | 15Kohm | @ | @ | @ | @
PR8680 | @ | @ | 15Kohm | 15Kohm | @ | @
ASUS
Project Name: X505ZN
Rev: REV:1
Title: PW 1.2V/+VTT/+2.5V(UP9002)
Size: Custom
Dept.:
Engineer:
Date: Monday, May 07, 2018
Sheet: 66 of 99

+3VA_DSW / +5VSUS [System Power]

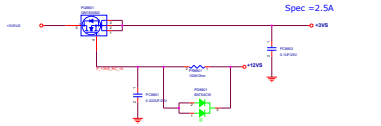


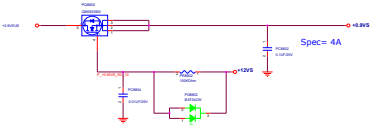
Part Reference	RT8249CGQW		UP9003QQKF	
	MLCC	V-CHIP	MLCC	V-CHIP
PC8707	330pF	@	150pF	@
PR8727	680Kohm	@	680Kohm	@
PC8708	0.01uF	@	0.01uF	@

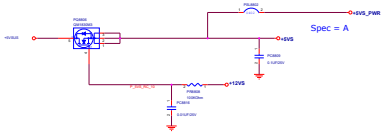
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

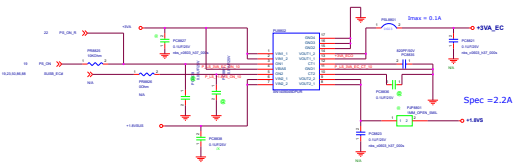
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

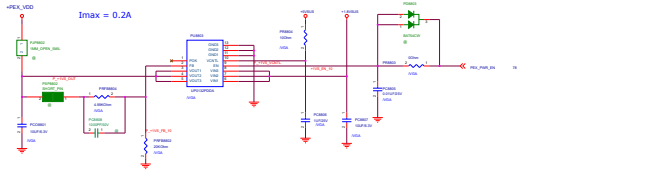
Load Switch

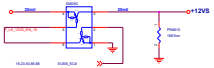












ASUS	Project Name: X555ZN		Rev: REV:0
Title :			
Size:	Dept.: MB-SZ-RD1	Engineer:	
Date: Monday, May 07, 2018		Sheet 66	of 99

ADP	<=65W	>=90W	Layout issue
PQ8901	QM3058M6AC	QM3056M6AC	QM3016M3
PQ8902	QM0930M3	QM3056M6AC	QM3016M3

	<=40W	C=120W	>=120W
PR8B901	25m	10m	5m
	25C	5b	0

ADP	<=65W	>=90W	Layout issue
PQ8903	QM0930M3	QM3056M6AC	QM3016M3

AD : 17.8V

98B903 SET
x : 0V >>0 OHM
30W: 0.4V >>14k
40W: 0.8V >>32k
45W: 1.2V >>57.6k
65W: 2.0V >>113k
90W: 2.4V >>210k
120W: 2.8V >>562k
x : 3.3V >>0

SYS短路保護線路

Change
20171108

0603

Place close to DCJACK

V-Chip
h=1.3mm

EL-CAP
h=4.5mm

VGA_ALERT_P# --> GPIO9
dGPU_PD# --> GPD12

EE Change Net Name, 0910

Project Name: X505ZN
Rev: 00.1
Title: PIN_DIAGRAM
Size: Custom
Doc#: MB-NEW2
Engineer: ATSZ
Date: Monday, May 01, 2017
Sheet 88 of 90

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

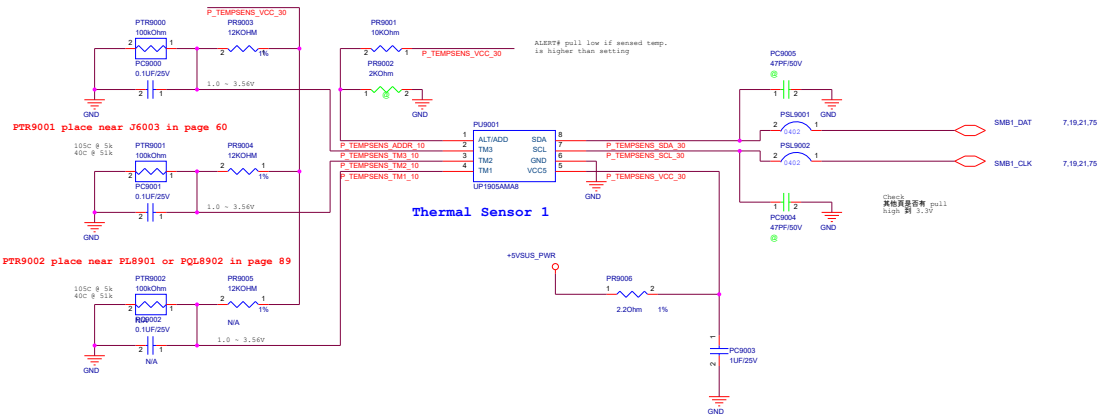
Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

PTR9000 place near PQ8901 in page 89

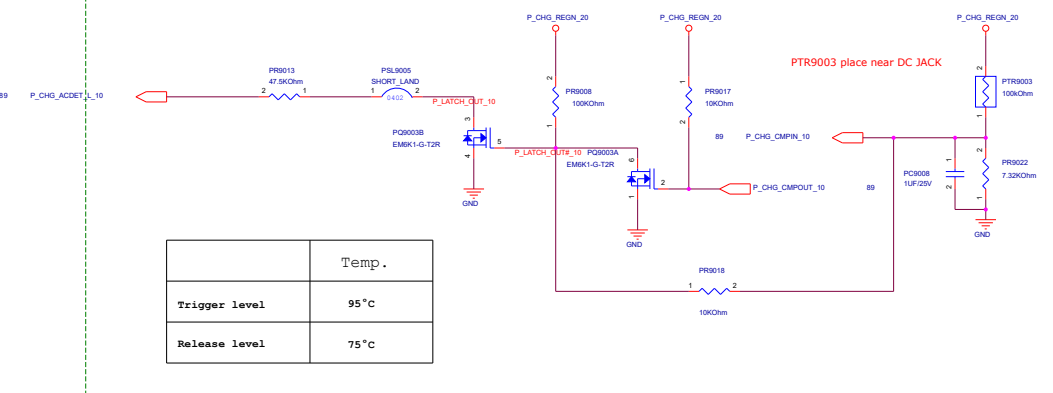
PTR9001 place near J6003 in page 60

PTR9002 place near PL8901 or PQL8902 in page 89



Thermal Sensor 1

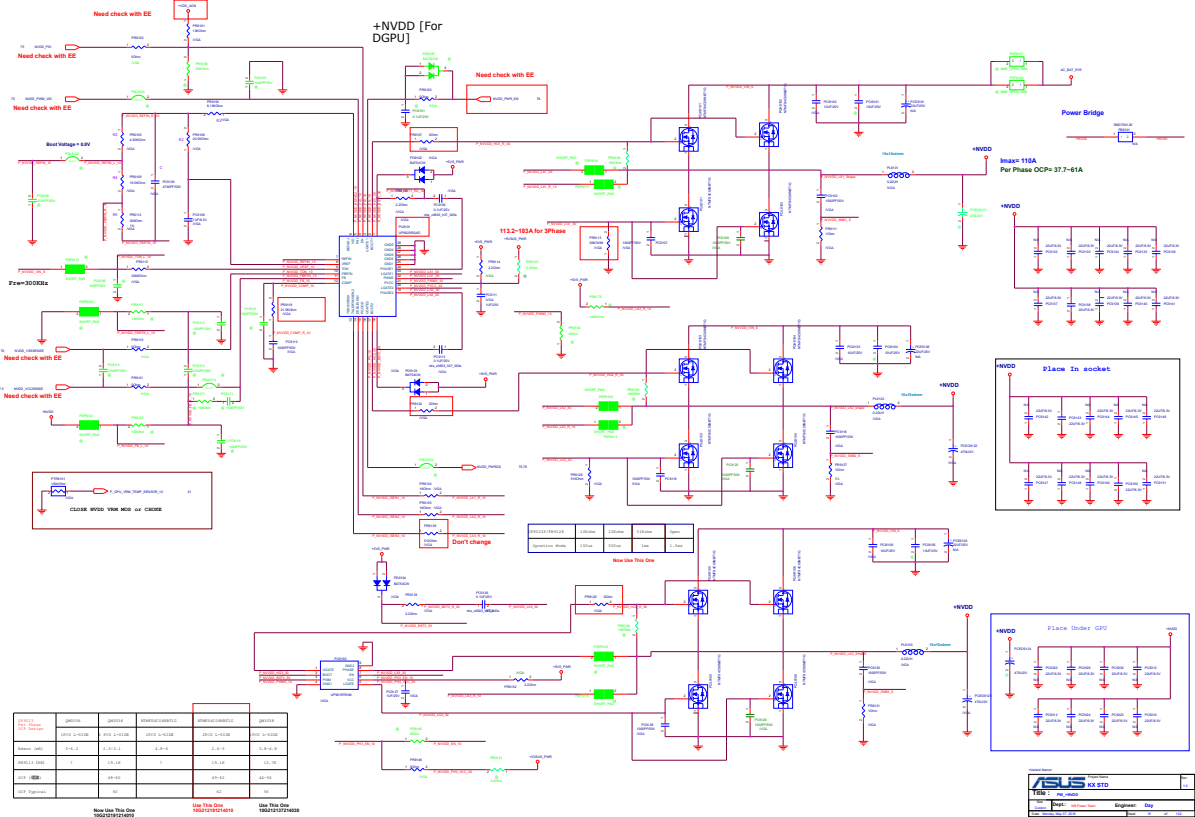
DC Jack Thermal Latch



	Temp.
Trigger level	**95°C**
Release level	**75°C**

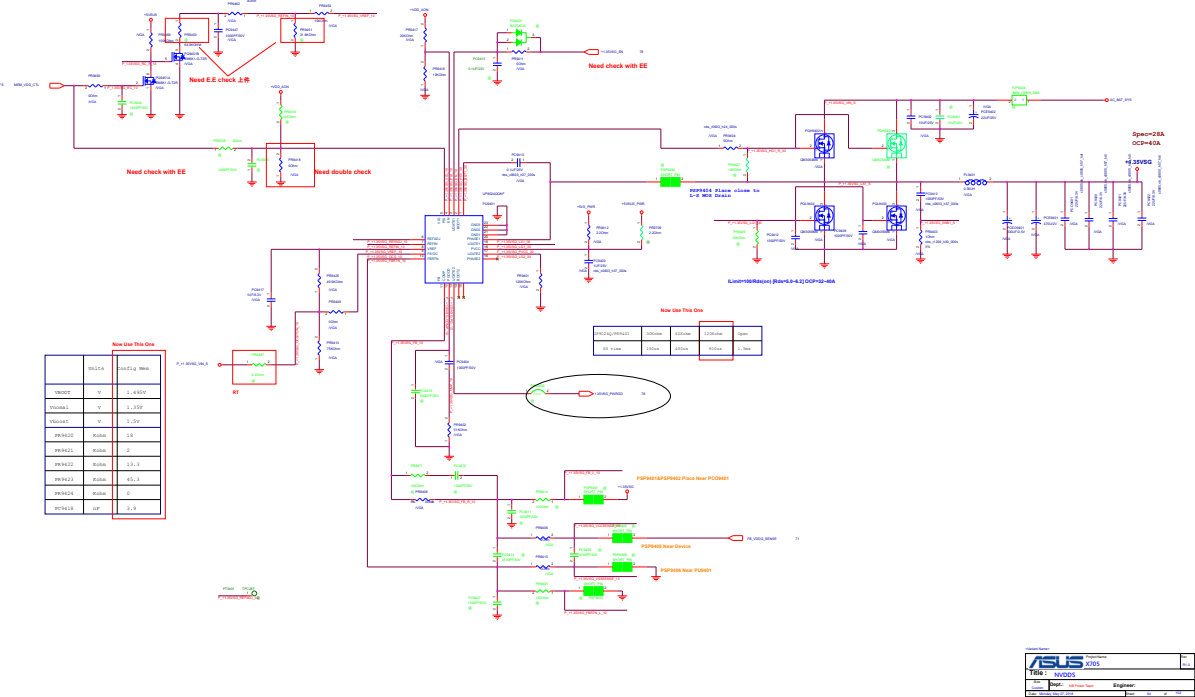
<Variant Name>

ASUS	Project Name: X505ZN	Rev: R0.1
Title : PW_PROTECTION		
Size: Custom	Dept.: NB-SZ-RD3	Engineer: ATSZ
Date: Monday, May 07, 2018	Sheet 90 of 99	



DPROG Pin Phase OCP Design	QM0006	QM3004	MEM5816C004R11G	MEM5816C004R11G	QM3008
	IMON 1-0336	IMON 1-0336	IMON 1-0336	IMON 1-0336	IMON 1-0336
Rdroop (mΩ)	3-4.2	2.5-3.1	4.8-6	2.4-3	3.4-4.4
PHASE DRV	3	3&2&	3	3&2&	3&2&
OCP (A)		44-60		49-62	44-56
OCP Typical		60		62	56
		Now Use This One 100Q121Q121Q1010	Use This One 100Q121Q121Q1010	Use This One 100Q121Q121Q4030	

Title:	PWR_VNDDS		
Size:	Project:	Rev:	
Custom	Dept.: NB Power Team	Engineer: Ray	
Date: Monday, May 07, 2018	Sheet 32 of 132		



	Units	Config Mess
VNOUT	V	1.495V
Vsense1	V	1.29V
Vsense1	V	1.29V
R93420	Kohm	10
R93421	Kohm	2
R93422	Kohm	13.3
R93423	Kohm	45.3
R93424	Kohm	0
RC9419	nF	3.9

PR9432@/PR9433	220mOhm	4.07mOhm	1.235Ohm	Open
DC 1.1ms	1.51ms	1.61ms	9.01ms	1.1ms

Quanta Computer Inc.					
ASUS	Project Name: X705				Rev: 0.1
Title : NVDD5					
Size: Custom	Doc#:	Date: Friday, May 07, 2021		Sheet: 66 of 68	Engineer:

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(pull up to +3VSUS)

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

T0=20ms (spec.>=10ms)

T1<200ms(check)

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(to EC) 8 PWR_SW#

(falling edge)

T2=50ms

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power) +1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

T3=2ms (spec.>=1ms)

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

T4=1.25ms

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD (power to CPU)

GFX_VID

+VGFX_CORE

T5=60us(typ.)

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

T6=110ms (spec.>=99ms)

(EC to power) CPU_VRON

19 +VCCIN

T7=10~100us

CLK_PWRGD (inversion of CLK_EN#)

T8=3~20ms

(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

T9=10ms

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#

ASUS	Project Name: X570UD		Rev: REV.0
Title : Power On Timing			
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Power	
Date: Monday, May 07, 2018		Sheet 100 of 100	

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(pull up to +3VSUS)

(PCH to EC) 4 ME_SusPwrDnAck

T0=20ms (spec.>=10ms)

(power to EC) 5 SUS_PWRGD

T1<200ms(check)

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(falling edge)

(to EC) 8 PWR_SW#

T2=50ms

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power) +1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

T3=2ms (spec.>=1ms)

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

T4=1.25ms

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD (power to CPU)

GFX_VID

+VGFX_CORE

T5=60us(typ.)

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

T6=110ms (spec.>=99ms)

(EC to power) CPU_VRON

19 +VCCIN

T7=10~100us

CLK_PWRGD

(inversion of CLK_EN#)

T8=3~20ms

(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

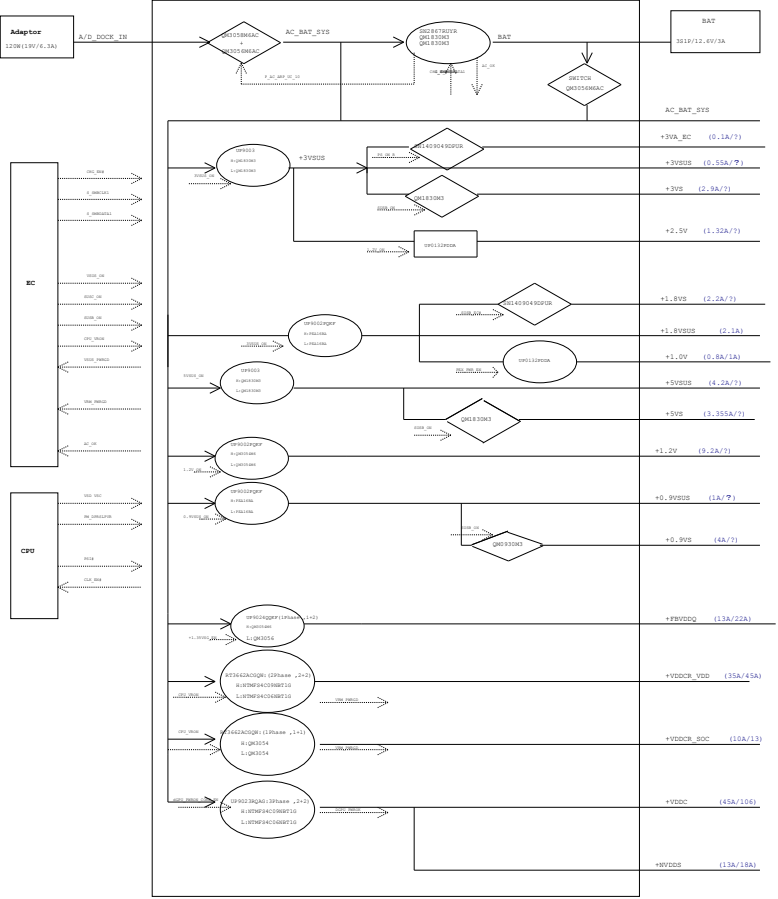
T9=10ms

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#

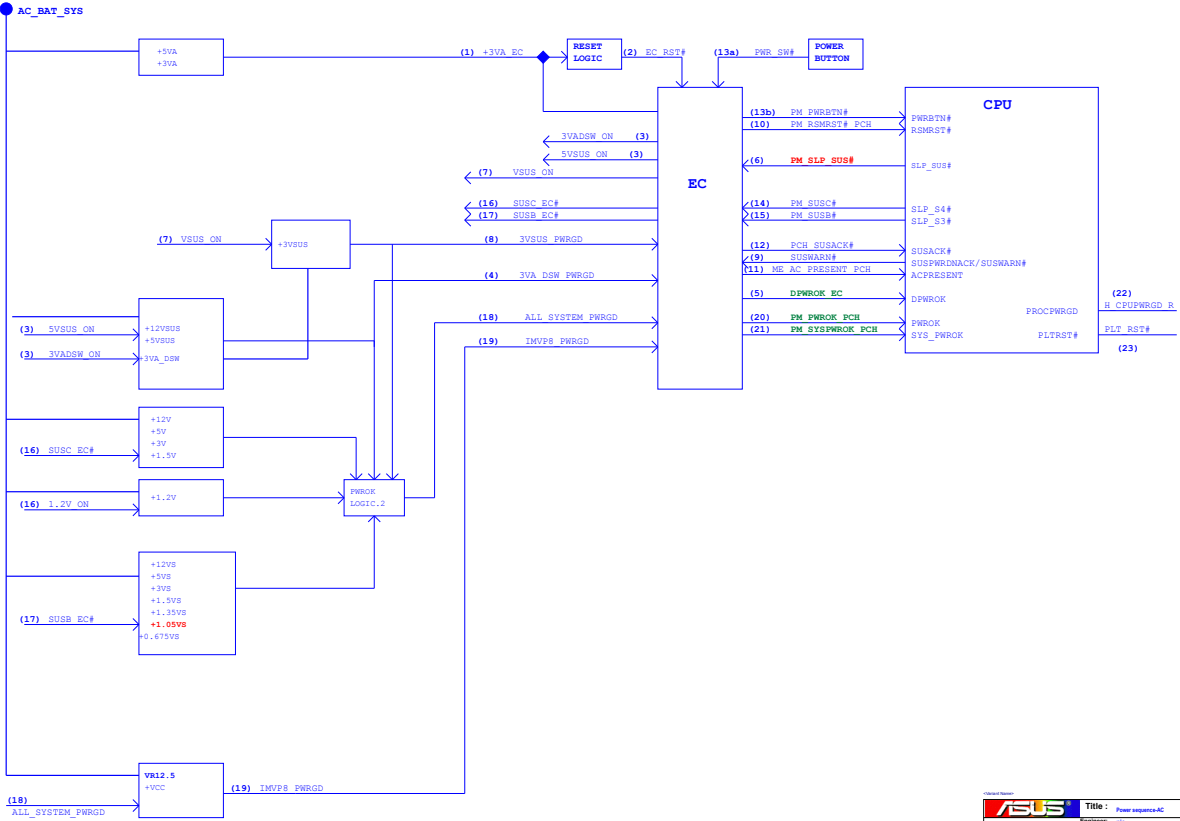
ASUS	Project Name: X570UD		Rev: REV.0
Title :	Power On Timing		
Size:	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Power
Date: Monday, May 07, 2018		Sheet: 101 of 102	



ASUS	Project Name: X505ZN		Rev: REV:1
Title :			
Last Modified: Thursday, May 07, 2015	Sheet: 66 of 69	Engineer:	

AC-IN Mode

X556U Power On Sequence Diagram



Title : Power sequence-AC

Engineer: mic

ASUSTeK Computer Inc.

X570UD

Size: C | Project Name | Rev: REV.0

Date: Monday, May 07, 2018 | Sheet 102 of 102

<Variant Name>

ASUSTeK COMPUTER INC. NB3	Title : DSG_Discharge	
	Engineer: SZNB2	
Size: C	Project Name: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 57 of 102	

Title	<Title>	
Size: A	Document Number: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 65 of 102	

Title	<Title>	
Size: A	Document Number: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 38 of 102	

Title	<Title>	
Size: A	Document Number: X570UD	Rev: R1.0
Date: Monday, May 07, 2018	Sheet 35 of 102	

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size A2	**Dept.:** NB-SZ-RD3	**Engineer:**

Date: Monday, May 07, 2018	Sheet	81	of	99

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size E	**Dept.:** NB-SZ-RD3	**Engineer:**

Date: Monday, May 07, 2018	Sheet	82	of	99

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size A	**Dept.:** NB-SZ-RD3	**Engineer:**

Date: Monday, May 07, 2018	Sheet	98	of	99

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size A	**Dept.:** NB-SZ-RD3	**Engineer:**

Date: Monday, May 07, 2018	Sheet	97	of	99

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size		
A	**Dept.:** NB-SZ-RD3	**Engineer:**

Date: Monday, May 07, 2018	Sheet	85	of	99

<Variant Name>

	Project Name X705	Rev R1.0

Title : NVDDS

Size		
C	**Dept.:** NB Power Team	**Engineer:**

Date: Monday, May 07, 2018	Sheet	93	of	102

/ISUS	Project Name **X705**	Rev 0.9

Title : POWER_+VGFX_CORE

Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER INC.	EE

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size C	**Dept.:** NB-SZ-RD3	**Engineer:**

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size		
A	**Dept.:** NB-SZ-RD3	**Engineer:**

Date: Monday, May 07, 2018	Sheet	3	of	99

<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size A	**Dept.:** NB-SZ-RD3	**Engineer:**

Date: Monday, May 07, 2018	Sheet	96	of	99

<Variant Name>

/ISUS	Project Name **X570UD**	Rev R1.0

Title : AUDIO_CODEC

Size		
A	**Dept.:** ASUSTeK COMPUTER INC. NB2	**Engineer:** SZNB1

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<Variant Name>

	Project Name X505ZN	Rev R0.1

Title :

Size A	**Dept.:** NB-SZ-RD3	**Engineer:**

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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: SZNB2	
Size: B	Project Name: X570UD	Rev: R1.0
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<Variant Name>

Title :

ASUSTeK COMPUTER INC.

Engineer: SZNB2

Size	Project Name	Rev
C	X570UD	R1.0

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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: SZNB2	
Size: A	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: SZNB2	
Size: Custom	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: SZNB2	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title : <Title>	
	Engineer: SZNB1	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : <Title>	
	Engineer: EE	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: SZNB2	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC. NB3	Title : <Title>	
	Engineer: SZNB2	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : *****	
	Engineer: SZNB2	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

	Title : <Title>	
ASUSTeK COMPUTER INC. NB1	**Engineer:** SZNB2	
Size: C	Project Name: **X570UD**	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: SZNB2	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: SZNB2	
Size: C	Project Name: X570UD	Rev: R1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : SB_DEBUG_LPC	
	Engineer: SZNB2	
Size: A	Project Name: X570UD	Rev: R1.0
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