Optimus/UMA Schematics Document

Sandy Bridge

Intel PCH

2010-11-09

REV : SD

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 1 of 103

Block Diagram (UMA/Optimus co-lay)

USB BD

POWER BD
48.4IH03.0SA

Finger Printer BD
48.4IH04.0SA

IO BD
48.4IH02.0SA

LED BD

##OnMainBoard

VRAM
1GB/512MB
88,89,90,91

DDR3
800MHz

NVIDIA
N12P-GE/GV
83.84,85,86,87

PCIe x 16
(Discrete only)

Intel CPU
Sandy Bridge
DDRIII: 1066/1333/1666 MHz
4,5,6,7,8,9,10

DDRIII 1066/1333/1666 Channel A

DDRIII Slot 0
1066/1333/1666 14

DDRIII 1066/1333/1666 Channel B

DDRIII Slot 1
1066/1333/1666 15

Project code : 91.4IH01.001
PCB P/N : 48.4IH01.0SA
Revision : 10254-SA

HDMI 51

LCD 49

CRT 50

FDI x 4 x 2
(UMA only)

DMI x 4

HDMI

LVDS

RGB CRT

Intel
PCH
Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25

PCIE x 1

GLAN
RTL8111E 31

RJ45
CONN 59

PCIE x 1/USB2.0 x 1

Mini-Card
WLAN 65

PCIE x 1/USB2.0 x 1

Mini-Card
WWAN 66

SIM 66

USB 2.0 x 1

MB
USB x 1

USB 2.0 x 1/SATA x 1

E-SATA/USB
comb 57

SATA x 2

HDD 56

ODD 56

BD
USB x 2

Bluetooth 63

CAMERA 49

Finger Print 64

USB2.0 x 5

SD/MMC+/MS/
MS Pro/xD 74

CardReader
Realtek
RTS5139

USB 2.0 x 1

AZALIA

SPI

LPC Bus

Flash ROM
4MB 60

LPC debug port 71

I/O BD

Internal DMIC

HP1

MIC IN

Azalia
CODEC
CONEXANT
CX20671 29

2CH SPEAKER

KBC
NUVOTON
NPCE795P 27

SMBus

G-Sensor 79

Touch
PAD 69

Int.
KB 69

Thermal
EMC2103-2-AP 28

Fan 28

SYSTEM DC/DC RT8208B 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6111CQHC 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6111C 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

LDO RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER	
L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

<Core Design>

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Title: Block Diagram

Size: A3 | Document Number: Huron River | Rev: SD

Date: Friday, December 10, 2010 | Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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Title: Table of Content

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 3 of 103

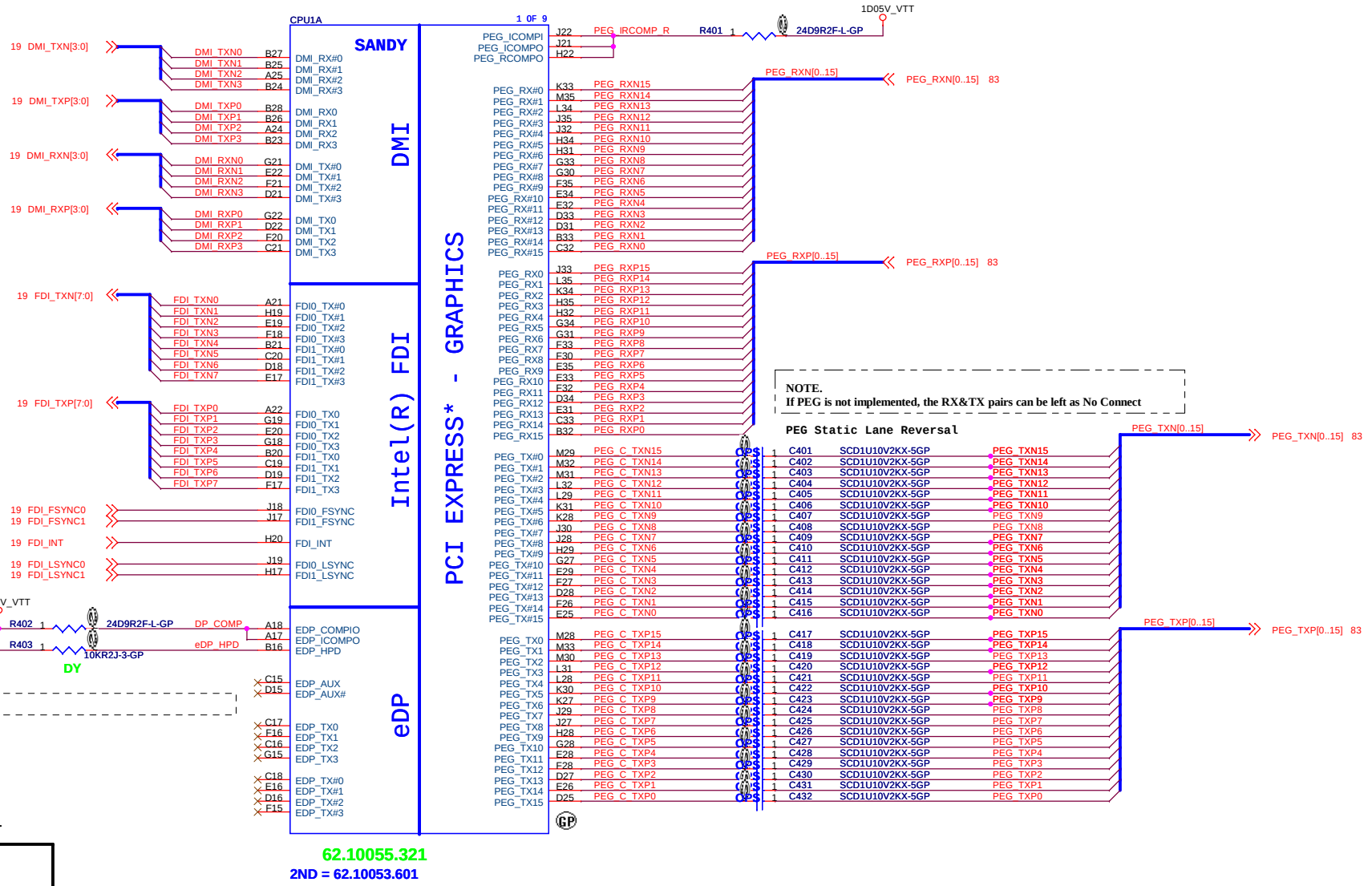
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.



Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

62.10055.321
2ND = 62.10053.601

delete R404&RN 401 @20100630

<Core Design>

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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 4 of 103

SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

RN502 CLK_DP_N_R CLK_DP_P_R 1D05V_VTT SRN1KJ-7-GP DY

20100722 SA confirm.

CPU1B 2 OF 9 SANDY

MISC: SNB_IVB# (C26), SKTOCC# (AN34)
CLOCKS: BCLK (A28), BCLK# (A27), DPLL_REF_SSCLK (A16), DPLL_REF_SSCLK# (A15)
THERMAL: CATERR# (AL33), PECI (AN33), PROCHOT# (AL32), THERMTRIP# (AN32)
DDR3 MISC: SM_DRAMRST# (R8), SM_RCOMP0 (AK1), SM_RCOMP1 (A5), SM_RCOMP2 (A4)
PWR MANAGEMENT: PM_SYNC (AM34), UNCOREPWRGOOD (AP33), SM_DRAMPWROK (V8), RESET# (AR33)
JTAG & BPM: PRDY# (AP29), PREQ# (AP27), TCK (AR26), TMS (AR27), TRST# (AP30), TDI (AR28), TDO (AP26), DBR# (AL35), BPM#0 (AT28), BPM#1 (AR29), BPM#2 (AR30), BPM#3 (AT30), BPM#4 (AP32), BPM#5 (AR31), BPM#6 (AT31), BPM#7 (AR32)

1D05V_VTT R501 62R2J-GP H_PROCHOT# C502 SC47P50V2JN-3GP

18 H_SNB_IVB#
TPAD14-GP TP501 SKTOCC#_R
TPAD14-GP TP502 H_CATERR#
22,27 H_PECI
27,42 H_PROCHOT# R513 56R2J-4-GP H_PROCHOT#_R
22,36 H_THERMTRIP#

Connect EC to PROCHOT# through inverting OD buffer.

R502 4K99R2F-L-GP SM_DRAMRST# 37

SM_RCOMP0 R506 140R2F-GP
SM_RCOMP1 R507 25D5R2F-GP
SM_RCOMP2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

R503 10KR2J-3-GP H_CPUPWRGD_R

19 H_PM_SYNC
11,22,36,97 H_CPUPWRGD R504 H_CPUPWRGD_R
19,37 PM_DRAM_PWRGD R505 0R0402-RAD DY 0R2J-2-GP VDDPWRGOOD
37 VDDPWRGOOD
BUF_CPU_RST#

XDP_PRDY# XDP_PREQ# XDP_TCLK XDP_TMS XDP_TRST# XDP_TDI XDP_TDO XDP_DBRESET#
XDP_BPM0 XDP_BPM1 XDP_BPM2 XDP_BPM3 XDP_BPM4 XDP_BPM5 XDP_BPM6 XDP_BPM7

62.10055.321
2ND = 62.10053.601

1210 follow Astro stuff buffer

3D3V_S0 1D05V_VTT C503 SC1U6D3V2KX-GP R512 75R2J-1-GP R510 43R2J-GP R509 750R2F-GP DY R517 DY 0R2J-2-GP
U501 74LVC1G07DC-GP (NC#1, A, GND, VCC, Y)
,18,27,31,35,36,65,66,71,83,97 PLT_RST#
BUFO_CPU_RST# BUF_CPU_RST#

XDP_PREQ# XDP_PRDY# → XDP_PREQ# 11, XDP_PRDY# 11
XDP_BPM0 … XDP_BPM7 → XDP_BPM0 11 … XDP_BPM7 11
XDP_TDO XDP_TDI XDP_TRST# XDP_TCLK XDP_TMS → XDP_TDO 11, XDP_TDI 11, XDP_TRST# 11, XDP_TCLK 11, XDP_TMS 11
XDP_DBRESET# → XDP_DBRESET# 11,19

1D05V_VTT RN501 XDP_TMS XDP_TDI XDP_TDO XDP_TCLK SRN51J-1-GP XDP_TRST# R511 51R2J-2-GP

3D3V_S0 XDP_DBRESET# R516 1KR2J-1-GP

<Core Design>

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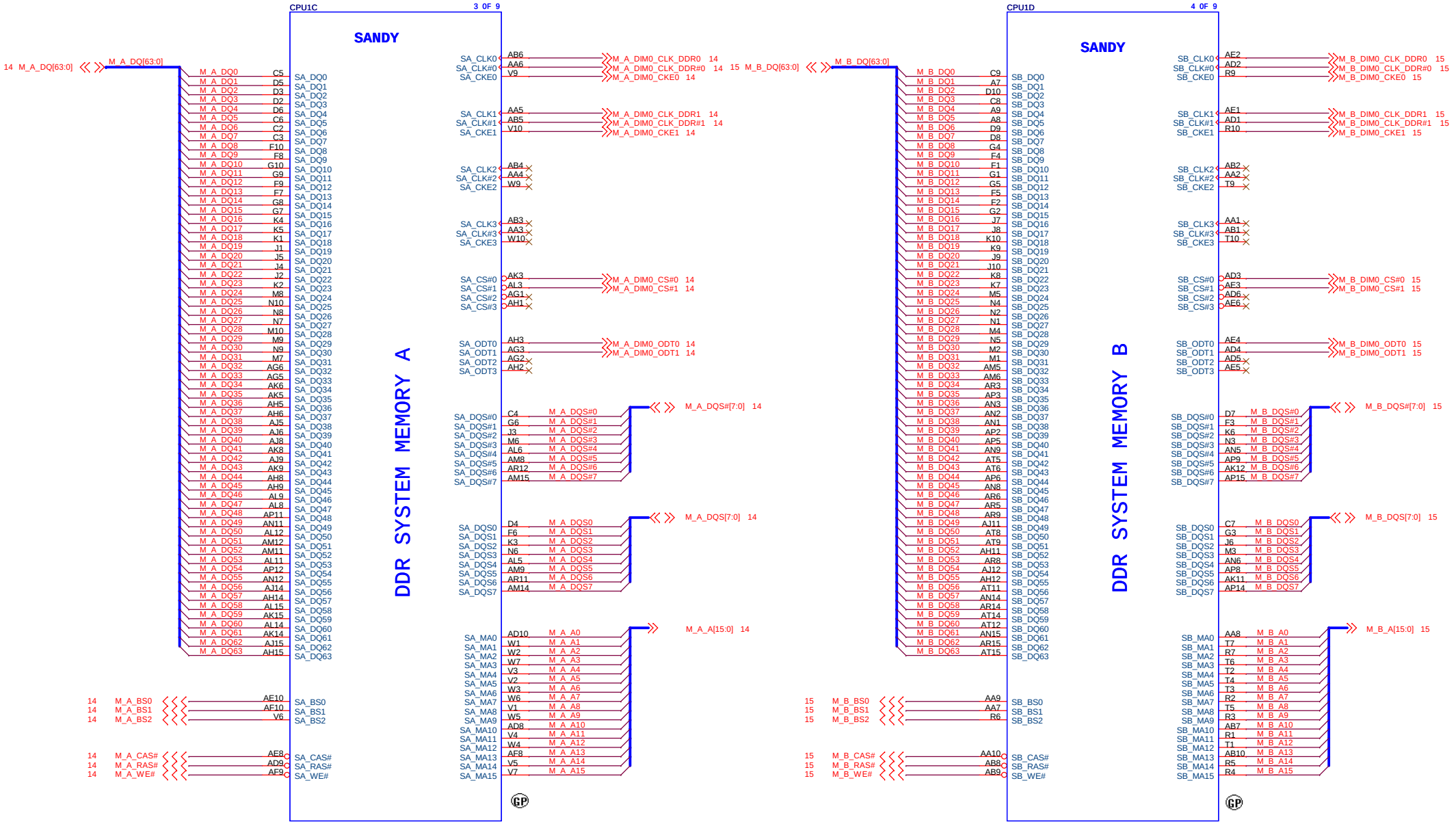
Title	CPU (THERMAL/CLOCK/PM)		
Size A3	Document Number LA57		Rev SD
Date: Friday, December 10, 2010	Sheet 5 of 103		

SSID = CPU



<Core Design>

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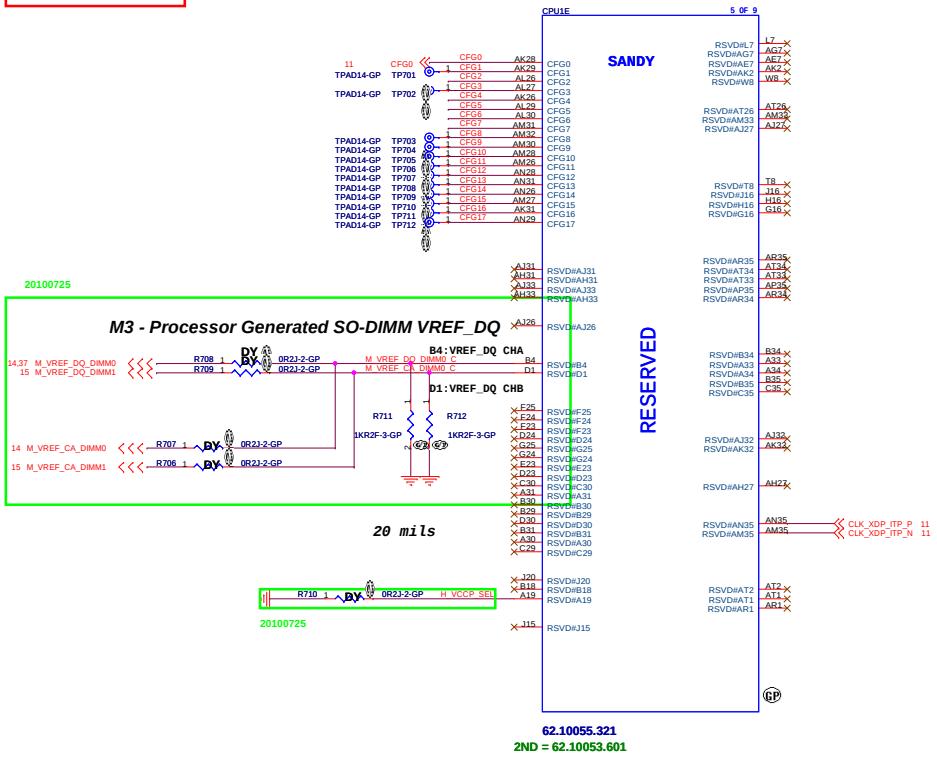
Title: **CPU (DDR)**

Size	Document Number	Rev
A3	LA57	SD

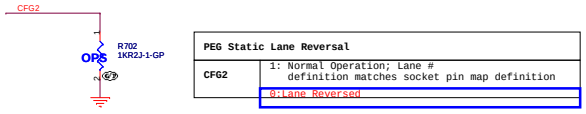
Date: Friday, December 10, 2010 Sheet 6 of 103

SSID = CPU

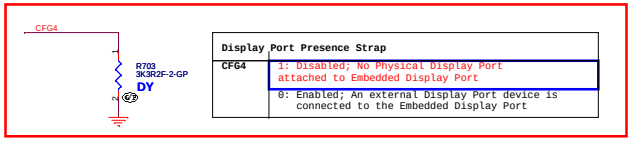


62.10055.321

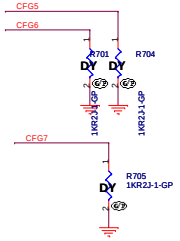
2ND = 62.10053.601



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

<Core Design>

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Title: CPU (RESERVED)

Size	Document Number	Rev
A2	LA57	SD

Date: Friday, December 10, 2010 Sheet 7 of 103

SSID = CPU

POWER

CPU1F

6 OF 9

SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR CORE POWER

53A

VCC_CORE

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP
C803 SC10U6D3V5KX-1GP
C804 SC10U6D3V5KX-1GP
C811 SC10U6D3V5KX-1GP

C815 SC10U6D3V5KX-1GP
C817 SC10U6D3V5KX-1GP
C818 SC10U6D3V5KX-1GP
C819 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 SC10U6D3V5KX-1GP
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

VCCIO: E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

C812 C813 C814 C829 C830 C842 C843 C844 C845 SC10U6D3V5KX-1GP

R804 need to close to CPU

1D05V_VTT

H_CPU_SVIDDAT R804 1 130R2F-1-GP

S-HS_20100610 V1.0

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

VR_SVID_ALERT# 42
H_CPU_SVIDCLK 42
H_CPU_SVIDDAT 42

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35
VSS_SENSE AJ34

VCCSENSE 42
VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10
VSSIO_SENSE A10

VCCIO_SENSE 45
VSSIO_SENSE 45

<Core Design>

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 8 of 103

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

CPU1G — 7 OF 9 — SANDY

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 C902 C903 C904 C905 C906 — SC10U6D3V5KX-1GP
C907 C908 C918 C919 C920 C921 — SC10U6D3V5KX-1GP

VAXG: AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

SENSE LINES

VAXG_SENSE — AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

DDR3 -1.5V RAILS

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 C915 C917 — SC10U6D3V5KX-1GP
TC903 ST330U2VDM-4-GP — DY

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0
DY — R902 10R2J-2-GP — Notice:pull-high 100k or 10k

SA RAIL

VCCSA_SENSE — H23 — VCCSA_SENSE — VCCSA_SENSE 48

FC_C22 — C22 — H_FC_C22 — H_FC_C22 48
VCCSA_VID1 — C24 — VCCSA_SEL — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

DY — TC902 ST330U2VDM-4-GP
C923 — SC10U6D3V5KX-1GP
C922 C924 — SC1U10V2KX-1GP

VCCPLL: B6 A6 A2

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

MISC

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

Close to CPU

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

S-HR_20100609 V1.0

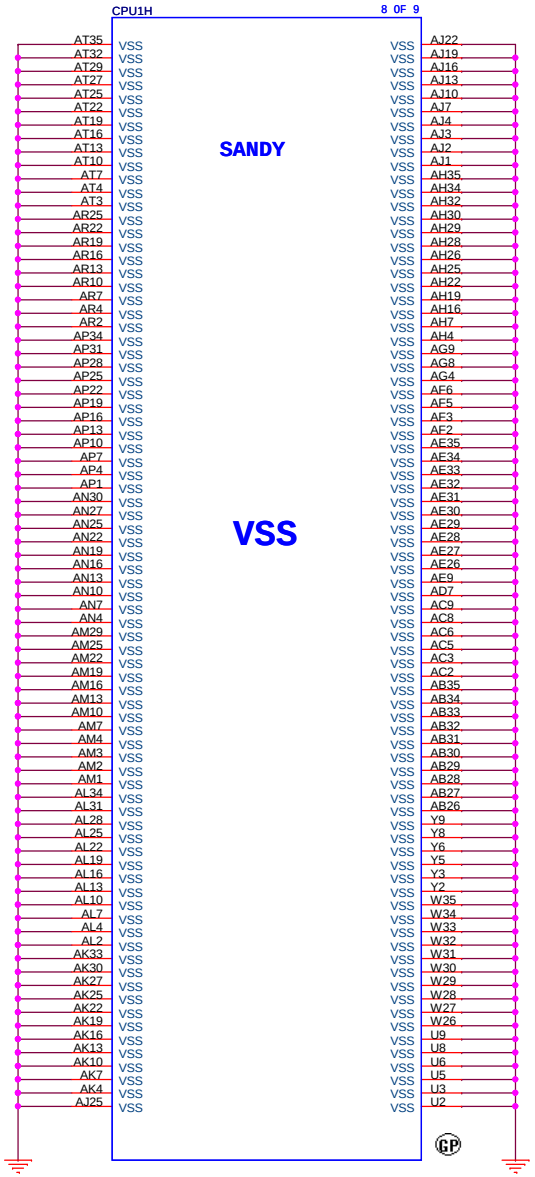
20100721 standard schematic update

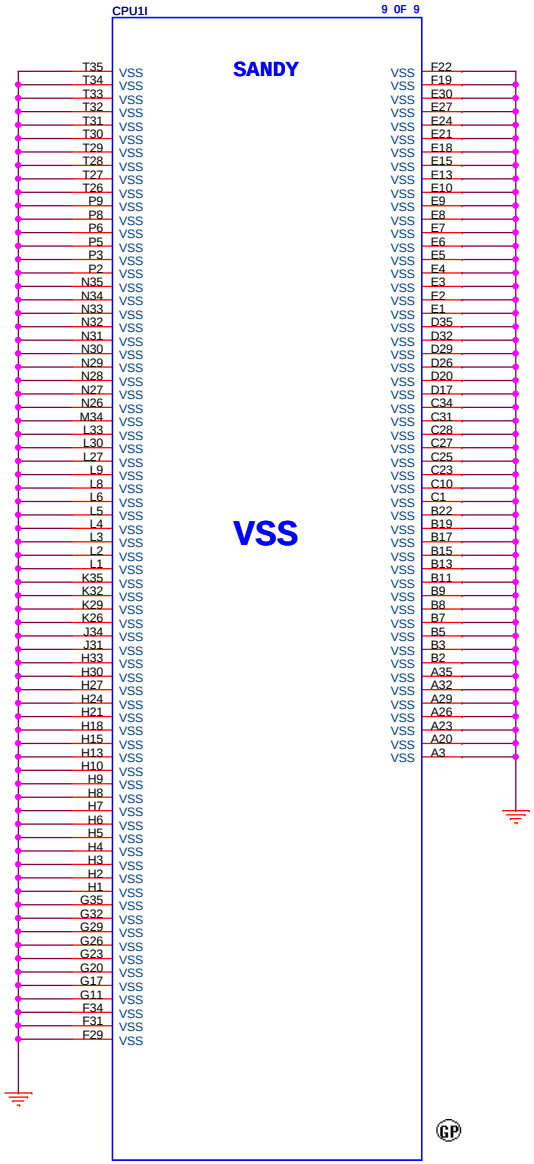
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: A3 | Document Number: LA57 | Rev: SD
Date: Friday, December 10, 2010 | Sheet 9 of 103

SSID = CPU





<Core Design>

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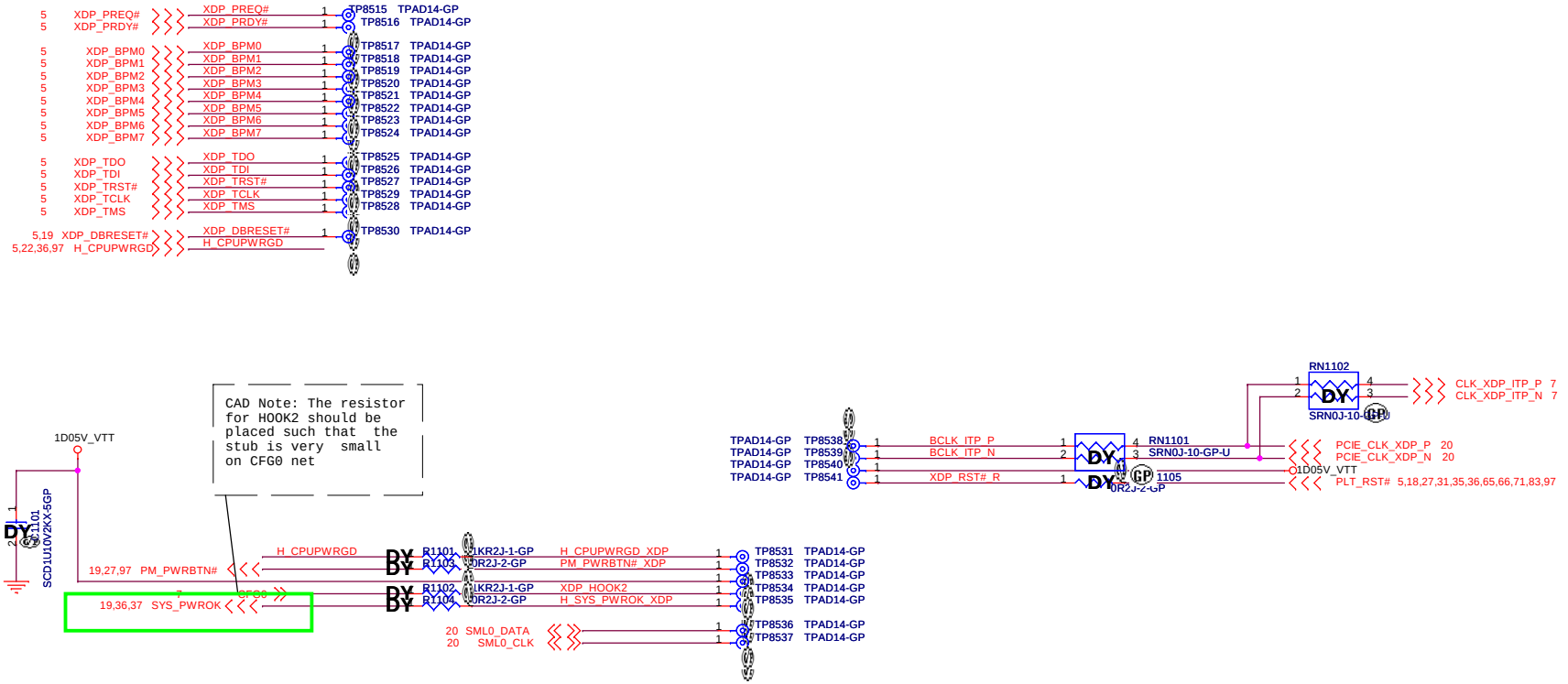
Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 10 of 103



<Core Design>

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Title: XDP		
Size: A3	Document Number: LA57	Rev: SD
Date: Friday, December 10, 2010	Sheet 11 of 103	

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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 12 of 103

(Blanking)

<Core Design>

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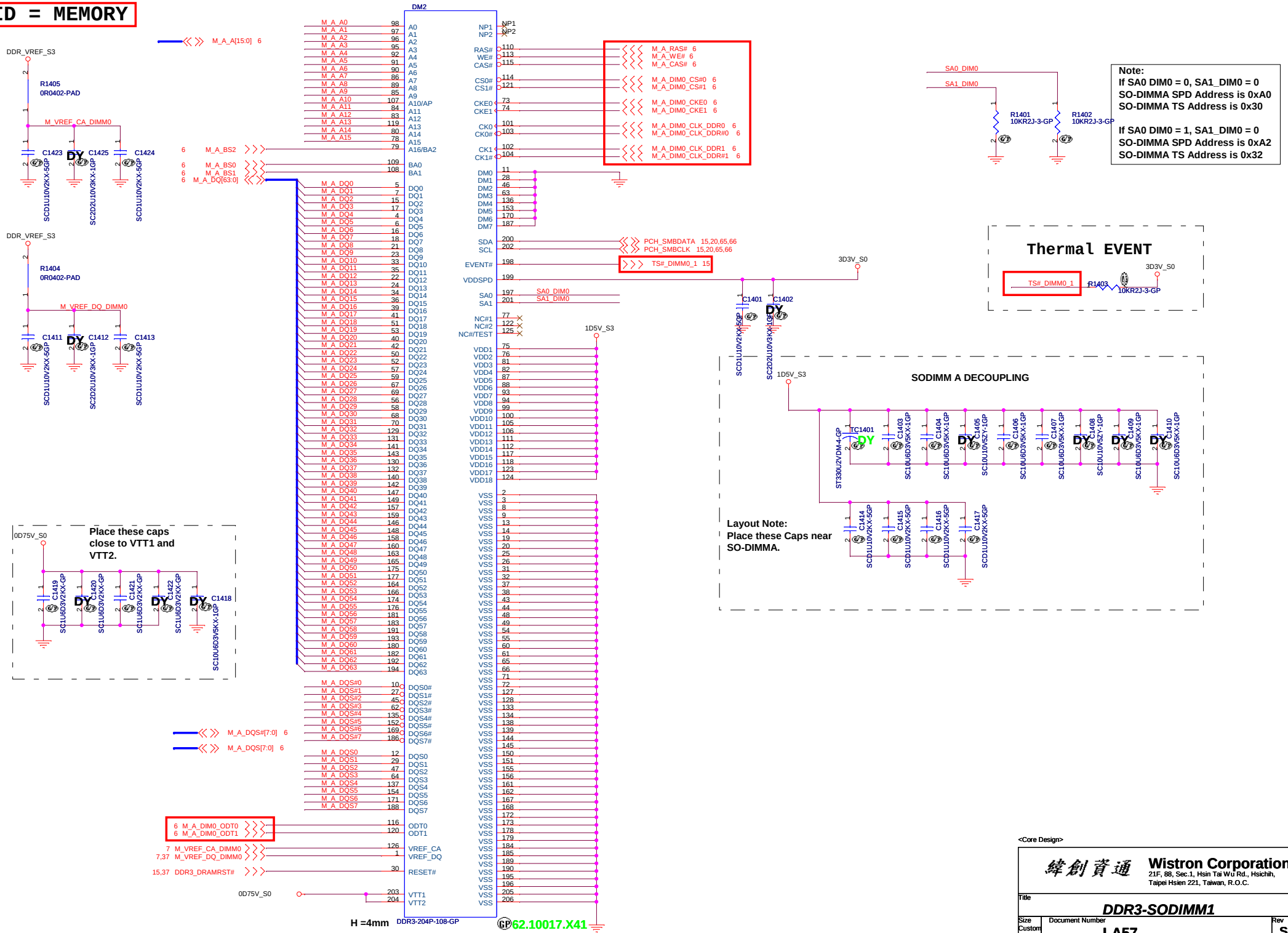
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 13 of 103

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

TS#_DIMM0_1 — R1403 10KR2J-3-GP — 3D3V_S0

SODIMM A DECOUPLING

1D5V_S3

ST330U2VDM-4-GP TC1401 DY

C1403 C1404 C1405 C1406 C1407 C1408 C1409 C1410
SC10U6D3V5KX-1GP
SC10U10V5ZY-1GP

C1414 C1415 C1416 C1417
SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

62.10017.X41
2ND = 62.10017.M51

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
Custom	LA57	SD

Date: Friday, December 10, 2010 Sheet 14 of 103

SSID = MEMORY

DM1

M_B_A[15:0] 6

M_B_BS2 6

M_B_BS0 6
M_B_BS1 6
M_B_DQ[63:0] 6

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6
M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6
M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6
M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6
M_B_DIM0_CLK_DDR1 6
M_B_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65,66
PCH_SMBCLK 14,20,65,66

TS#_DIMM0_1 14

SA0_DIM1
SA1_DIM1

M_B_DQS#[7:0] 6
M_B_DQS[7:0] 6

M_B_DIM0_ODT0 6
M_B_DIM0_ODT1 6

7 M_VREF_CA_DIMM1
7 M_VREF_DQ_DIMM1

14,37 DDR3_DRAMRST#

0D75V_S0

3D3V_S0

1D5V_S3

DDR_VREF_S3

R1504 0R0402-PAD
R1503 0R0402-PAD

M_VREF_CA_DIMM1
M_VREF_DQ_DIMM1

C1523 SCD1U10V2KX-5GP
C1524 SC2D2U10V3KX-1GP
C1522 SCD1U10V2KX-5GP
C1515 SCD1U10V2KX-5GP
C1516 SC2D2U10V3KX-1GP
C1517 SCD1U10V2KX-5GP

DY

Place these caps close to VTT1 and VTT2.

C1518 SC1U6D3V2KX-GP
C1519 SC1U6D3V2KX-GP
C1520 SC1U6D3V2KX-GP
C1521 SC1U6D3V2KX-GP

R1501 10KR2J-3-GP
R1502 10KR2J-3-GP

C1501 SCD1U10V2KX-5GP
C1502 SC2D2U10V3KX-1GP

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

SODIMM B DECOUPLING

C1503 SC10U10V5ZY-1GP
C1504 SC10U10V5ZY-1GP
C1505 SC10U6D3V5KX-1GP
C1506 SC10U6D3V5KX-1GP
C1507 SC10U6D3V5KX-1GP
C1508 SC10U10V5ZY-1GP
C1509 SC10U6D3V5KX-1GP
C1510 SC10U6D3V5KX-1GP

C1511 SCD1U10V2KX-5GP
C1512 SCD1U10V2KX-5GP
C1513
C1514 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED

62.10017.X51
2ND = 62.10017.R91

H = 8mm

DDR3-204P-109-GP

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 15 of 103

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<Core Design>

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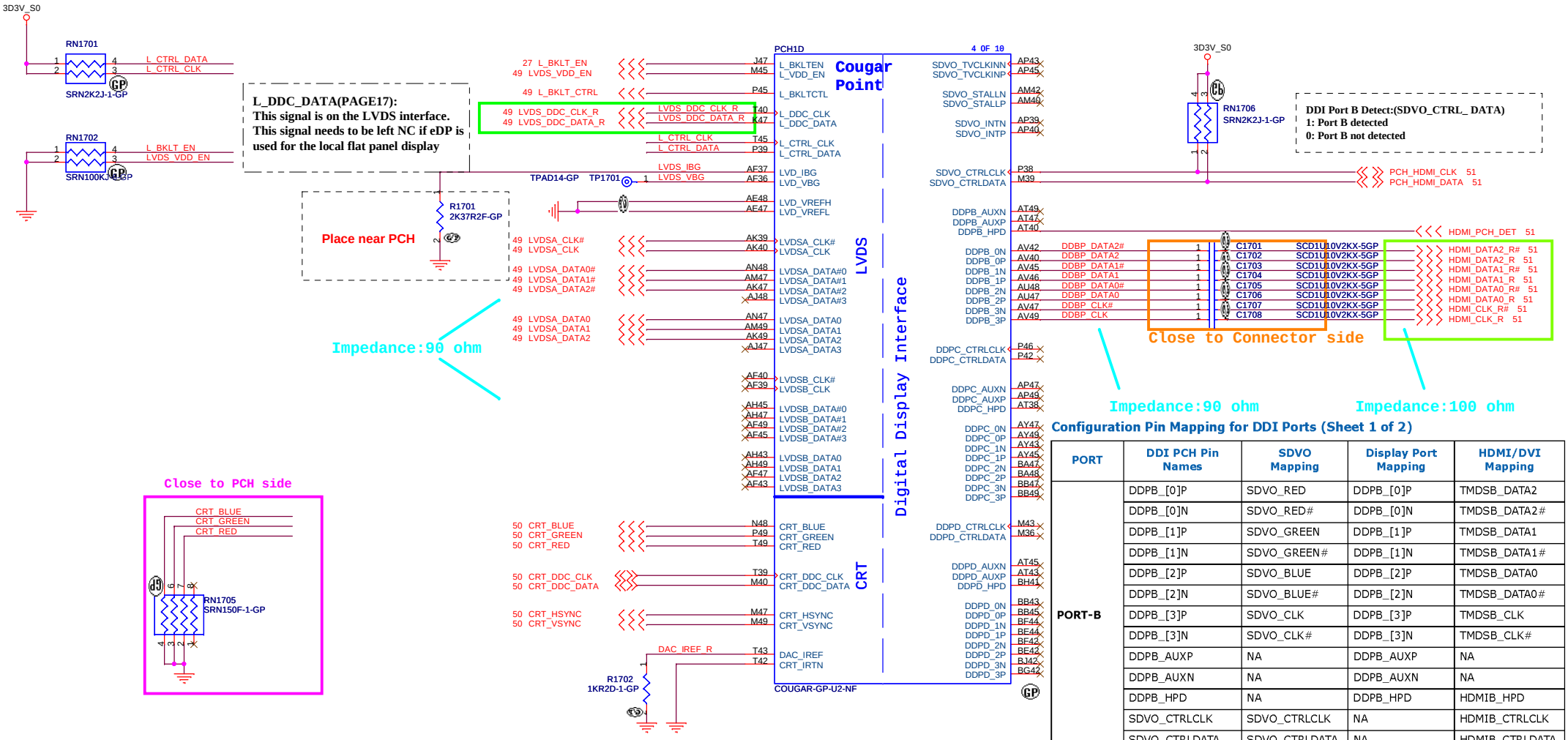
Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 16 of 103



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

<Core Design>

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Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 17 of 103

SSID = PCH

20100725 Annie modify

CRB : 2.2K
CEKLT: 1K

+V_NVRAM_VCCQ
R1808 2K2R2J-2-GP
NV_CLE — R1809 1KR2J-1-GP — H_SNB_IVB# 5

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

RN1801 SRN8K2J-2-GP
INT_PIRQA# INT_PIRQE# INT_PIRQC# INT_PIRQB# INT_PIRQH# INT_PIRQG# INT_PIRQD# INT_PIRQF#
3D3V_S0

R1801 4K7R2J-2-GP PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803 SRN10KJ-5-GP
DGPU_HOLD_RST#
DGPU_PWR_EN#

R1802 1KR2J-1-GP BBS_BIT1
R1803 1KR2J-1-GP BBS_BIT0 — BBS_BIT0 21

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

20100720 SW

PCH1E — 5 OF 10 — Cougar Point — COUGAR-GP-U2-NF

RSVD: TP1–TP40
NVRAM: RSVD#AY7, RSVD#AV7, RSVD#AU3, RSVD#BG4, RSVD#AT10, RSVD#BC8, RSVD#AU2, RSVD#AT4, RSVD#AT3, RSVD#AT1, RSVD#AY3, RSVD#AT5, RSVD#AV3, RSVD#AV1, RSVD#BB1, RSVD#BA3, RSVD#BB5, RSVD#BB3, RSVD#BB7, RSVD#BE8, RSVD#BD4, RSVD#BF6, RSVD#AV5, DF_TVS, RSVD#AV10, RSVD#AT8, RSVD#AY5, RSVD#BA2, RSVD#AT12, RSVD#BF3
NV_ALE, NV_CLE, NV_RCOMP — TP1803 TPAD14-GP

+V_NVRAM_VCCQ
Danbury Technology:
Disabled when Low.
Enable when High.
R1810 1KR2J-1-GP DY
NV_ALE

USB Ext. port 1 (HS)
External debug port use on Huron river platform

PCI: PIRQA#, PIRQB#, PIRQC#, PIRQD#, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#

USB: USBP0N/P … USBP13N/P, USBRBIAS#, USBRBIAS, OC0#/GPIO59, OC1#/GPIO40, OC2#/GPIO41, OC3#/GPIO42, OC4#/GPIO43, OC5#/GPIO9, OC6#/GPIO10, OC7#/GPIO14

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD)
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

R1811 22D6R2F-L1-GP

SW programing USB_OC#12_13 for USB 9

R1819 8K2R2J-3-GP 8L
R1820 8K2R2J-3-GP 6L
20101019 modify

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

R1814 8K2R2J-3-GP DY
R1818 0R0402-PAD
R1813 0R2J-2-GP
R1815 0R0402-PAD
R1817 0R0402-PAD
TP1801 TP1802 TP1804 TP1805 TPAD14-GP

R1804 R1805 R1806 22R2J-2-GP DY
CLK_PCI_LPC_R CLK_PCI_FB_R CLK_PCI_KBC_R
CLKOUT_PCI0 … CLKOUT_PCI4

EC1801 EC1802 SC47P50V2CN-1GP DY
KBC CLK EMI

U1801 74LVC1G08GW-1-GP 73.01G08.L04
PLT_RST# — PCI_PLTRST#
R1807 0R2J-2-GP
R1816 10K2R2J-3-GP DY
C1801 C1802 SC220P50V2KX-3GP DY
20100629

RN1802 SRN10KJ-L3-GP
USB_OC#2_3 USB_OC#4_5 USB_OC#6_7 USB_OC#10_11 — USB_OC#12_13 USB_OC#8_9 USB_OC#0_1

<Core Design>

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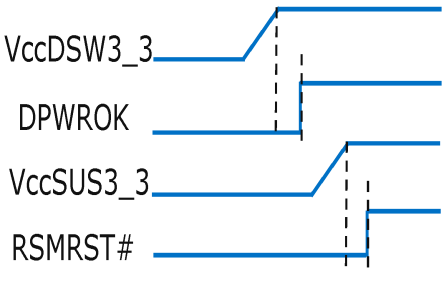
Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: LA57 | Rev: SD
Date: Friday, December 10, 2010 | Sheet 18 of 103

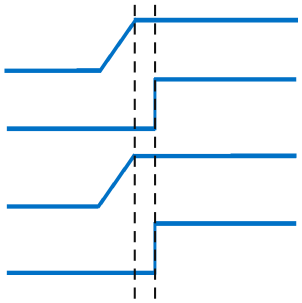
SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

Deep S4/S5 Supported



Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — Cougar Point — 3 OF 10

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP, DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#, DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29

COUGAR-GP-U2-NF

1D05V_VTT
R1901 49D9R2F-GP DMI_COMP_R
R1902 750R2F-GP RBIAS_CPY

DY R1926 SYS_PWROK
DY R1904 PWROK
SUS_PWR_ACK — R1903 0R0402-PAD — SUSACK#
DY R1925 0R2J-2-GP SYS_RESET#
5,11 XDP_DBRESET#
3D3V_S0
11,36,37 SYS_PWROK
R1905 10KR2J-3-GP
DY R1923 0R2J-2-GP
27,36 S0_PWR_GOOD — R1924 0R0402-PAD — PWROK
36,37,45,46,47 RUNPWROK — R1906 0R0402-PAD — R1907 0R2J-2-GP DY — MEPWROK
5,37 PM_DRAM_PWRGD

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

PM_RSMRST# — R1910 0R0402-PAD — DY R1911 10KR2J-3-GP — RTC_AUX_S5
PCH_DPWROK
PCIE_WAKE# 31,35,65,66
PM_CLKRUN# 27
PM_SUS_STAT# — TP1901 TPAD14-GP
SUS_CLK — R1913 0R0402-PAD — PCH_SUSCLK_KBC 27
PM_SLP_S5# — TP1902 TPAD14-GP
SLP_S4#_R — R1914 0R0402-PAD — PM_SLP_S4# 27,46
SLP_S3#_R — R1915 0R0402-PAD — PM_SLP_S3# 27,36,37,47,92
PM_SLP_A# — TP1903 TPAD14-GP
PM_SLP_SUS# — TP1904 TPAD14-GP
H_PM_SYNC — H_PM_SYNC 5
PM_SLP_LAN# — TP1905 TPAD14-GP

20,27 SUS_PWR_ACK
11,27,97 PM_PWRBTN#
27 AC_PRESENT
20 BATLOW#
PM_RI#

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1917 330KR2J-L1-GP
DSWODVREN — R1918 DY 330KR2J-L1-GP

3D3V_S0
PM_CLKRUN# — R1919 8K2R2J-3-GP

3D3V_S5
RN1901 SRN10KJ-6-GP
PCIE_CLK_LAN_RQ1# — PCIE_CLK_LAN_RQ1# 20,31
AC_PRESENT
PM_RI#
R1921 10KR2J-3-GP PCIE_WAKE#
DY R1922 10KR2J-3-GP PM_PWRBTN#
PM_SLP_LAN#
R1920 10KR2J-3-GP

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

20100729

PWRBTN#
This signal has an internal pull-up resistor

R1908 10KR2J-3-GP — PM_RSMRST#

3D3V_AUX_S5
R1909 100KR2J-1-GP
R1916 10KR2J-3-GP
Q1901 2N7002KDW-GP
3V_5V_POK_# — 3V_5V_POK 41
PM_RSMRST# — R1912 1KR2J-1-GP — RSMRST#_KBC 27

84.2N702.A3F
2nd = 84.DM601.03F

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: **LA57** | Rev: **SD**
Date: Friday, December 10, 2010 | Sheet 19 of 103

SSID = PCH

20100705_Standard

PCH1B

2 OF 10

Cougar Point

W-WAN
WLAN
Card Reader
LAN
USB3.0
Intel GBE LAN
Dock
NEW CARD

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

COUGAR-GP-U2-NF

WWAN CLK
WLAN CLK
LAN CLK
USB3.0 CLK

PCIECLKRQ1# and PCIECLKRQ2# support S0 power only

S-HR_20100614 V1.1

20100729 follow CRB change to 1K

2nd = 84.DM601.03F
84.2N702.A3F
2N7002KDW-GP

R2008 and C2008 CO-LAY

UMA_DISCRETE#
UMA: 1 1
DIS : 0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

R2017 RN9407 RN9408 RN9406 need very close to PCH

<Core Design>

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
if more than 2 PCI clocks + PCI loopback are routed.

20100706

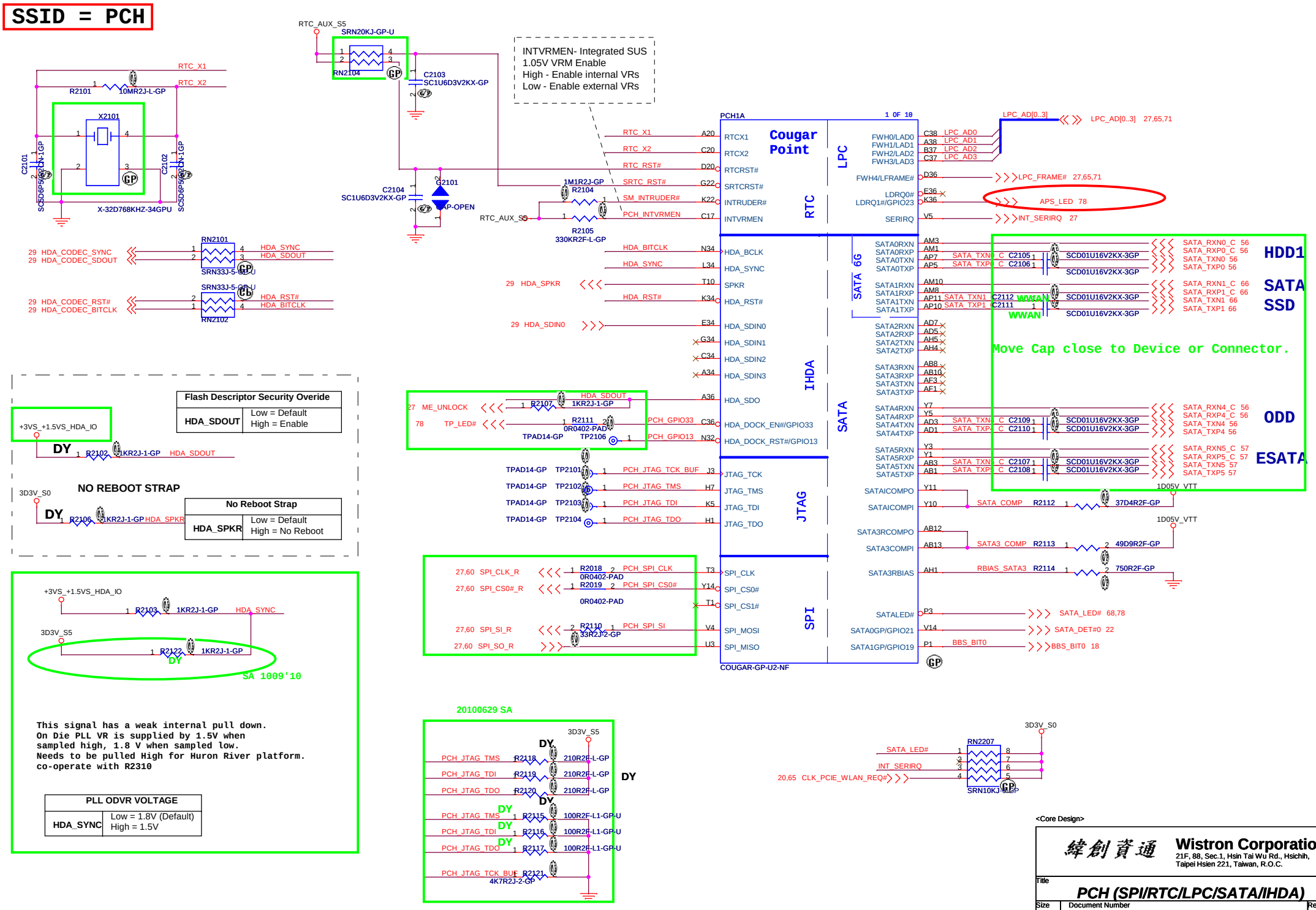
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 20 of 103

SSID = PCH



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 21 of 103

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — R2202 1 — 200KR2F-L-GP — SATA_ODD_PRSNT#

3D3V_S0 — SRN10KJ-5-GP RN2203 — H_A20GATE, H_RCIN#

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

3D3V_S0 — R2226 10KR2J-3-GP (DY) — PCH_GPIO27
3D3V_S0 — R2224 10KR2J-3-GP — PCH_TEMP_ALERT#
R2223 10KR2J-3-GP (DY)
R2225 10KR2J-3-GP (DY)

3D3V_S0 — RN2201 SRN10KJ-5-GP: EC_SCI#, DGPU_HPD_INTR#, EC_SMI#
RN2103 SRN10KJ-5-GP: PSW_CLR#, PCH_GPIO48, MFG_MODE, SATA_DET#0
RN2202 SRN10KJ-5-GP: S_GPIO, PCH_GPIO22

3D3V_S5 — RN2205 SRN10KJ-5-GP: PCH_GPIO24, PCH_GPIO12, USB3_PWR_ON
20 PEG_B_CLKRQ#
PLL_ODVR_EN — R2227 10KR2J-3-GP
PCH_GPIO15 — R2201 1KR2J-1-GP

20100720 SW
49 Color_Engine# — R2221 0R0402-PAD — TPAD14-GP TP2202

NC_FP_DET# — R2220 10KR2J-3-GP — LAB57
20100725

PCH1F — 6 OF 10 — Cougar Point

GPIO:
- S_GPIO — R2218 100R2J-2-GP — GPIO0 T7
- EC_SMI# A42
- DGPU_HPD_INTR# H36
- 27 EC_SCI# — EC_SCI# E38
- ICC_EN# C10
- PCH_GPIO12 C4
- PCH_GPIO15 G2
- 56 SATA_ODD_PRSNT# — R2213 0R0402-PAD — PCH_GPIO16 U2
- 92,93 DGPU_PWROK — DGPU_PWROK D40
- 49 Color_Engine# — R2221 0R0402-PAD — PCH_GPIO22 T5
- TPAD14-GP TP2202 — PCH_GPIO24 E8
- PCH_GPIO27 E16
- PLL_ODVR_EN P8
- PSW_CLR# — TPAD14-GP TP2204 — NC_FP_DET# K4
- DMI_OVRVLTG V8
- FDI_OVRVLTG M5
- MFG_MODE N2
- GFX_CRB_DET M3
- PCH_GPIO48 V13
- TPAD14-GP TP2205 — PCH_TEMP_ALERT# V3
- 35 USB3_PWR_ON — USB3_PWR_ON D6

GAP-OPEN G2201

GPIO pins: BMBUSY#/GPIO0, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, LAN_PHY_PWR_CTRL/GPIO12, GPIO15, SATA4GP/GPIO16, TACH0/GPIO17, SCLOCK/GPIO22, GPIO24/MEM_LED, GPIO27, GPIO28, STP_PCI#/GPIO34, GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SATA5GP/GPIO49, GPIO57

CPU/MISC:
- TACH4/GPIO68 C40 — SATA_ODD_PWRGT 56
- TACH5/GPIO69 B41 — UMA_DIS# — UMA_DIS# 20
- TACH6/GPIO70 C41 — VRAM_SIZE1
- TACH7/GPIO71 A40 — VRAM_SIZE2
- A20GATE P4 — H_A20GATE 27
- PECI AU16 — H_PECI R — R2203 DY 62R2J-2-GP — H_PECI 5,27
- RCIN# P5 — H_RCIN# 27
- PROCPWRGD AY11 — H_CPUPWRGD 5,11,36,97
- THRMTRIP# AY10 — PCH_THERMTRIP_R — R2204 390R2J-1-GP — H_THERMTRIP# 5,36
- INIT3_3V# T14 — INIT3_3V# — TP2201 TPAD14-GP

TS_VSS: AH8, AK11, AH10, AK10 — TS_VSS 1 — R2219 0R0402-PAD — 2
NC#P37 P37

NCTF_VSS: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49
NCTF_VSS: BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49
NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49 / BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

COUGAR-GP-U2-NF

3D3V_S0 — R2205 10KR2J-3-GP (DY) — GFX_CRB_DET — R2206 100KR2J-1-GP

PCH_THERMTRIP_R — R2222 DY 56R2J-4-GP — 1D05V_VTT

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

20100729 follow Annie CRB

3D3V_S0 — R2207 10KR2J-3-GP (DY) — FDI_OVRVLTG
R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2209 10KR2J-3-GP (DY) — DMI_OVRVLTG
R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

ICC_EN#1 — R2211 1KR2J-1-GP

3D3V_S0 — R2214 10KR2J-3-GP (2G) — R2216 10KR2J-3-GP (1G)
[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G
VRAM_SIZE1
VRAM_SIZE2
R2215 10KR2J-3-GP (1G_512M) — R2217 10KR2J-3-GP (512M_2G)

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY 1 — R2212 1KR2J-1-GP

<Core Design>

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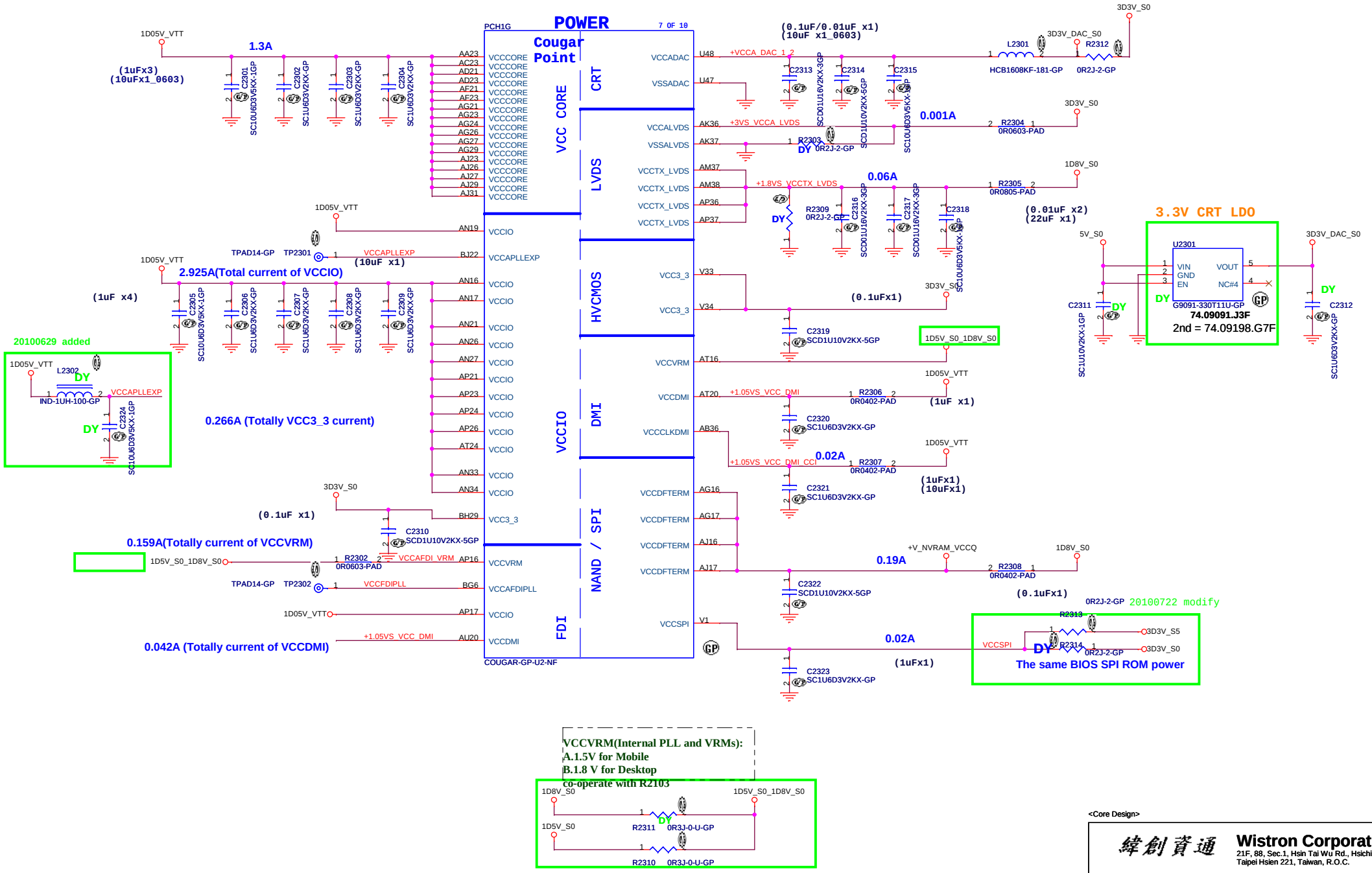
Title: PCH (GPIO/CPU)
Size: A3 | Document Number: LA57 | Rev: SD
Date: Friday, December 10, 2010 | Sheet 22 of 103

SSID = PCH 6A



<Core Design>

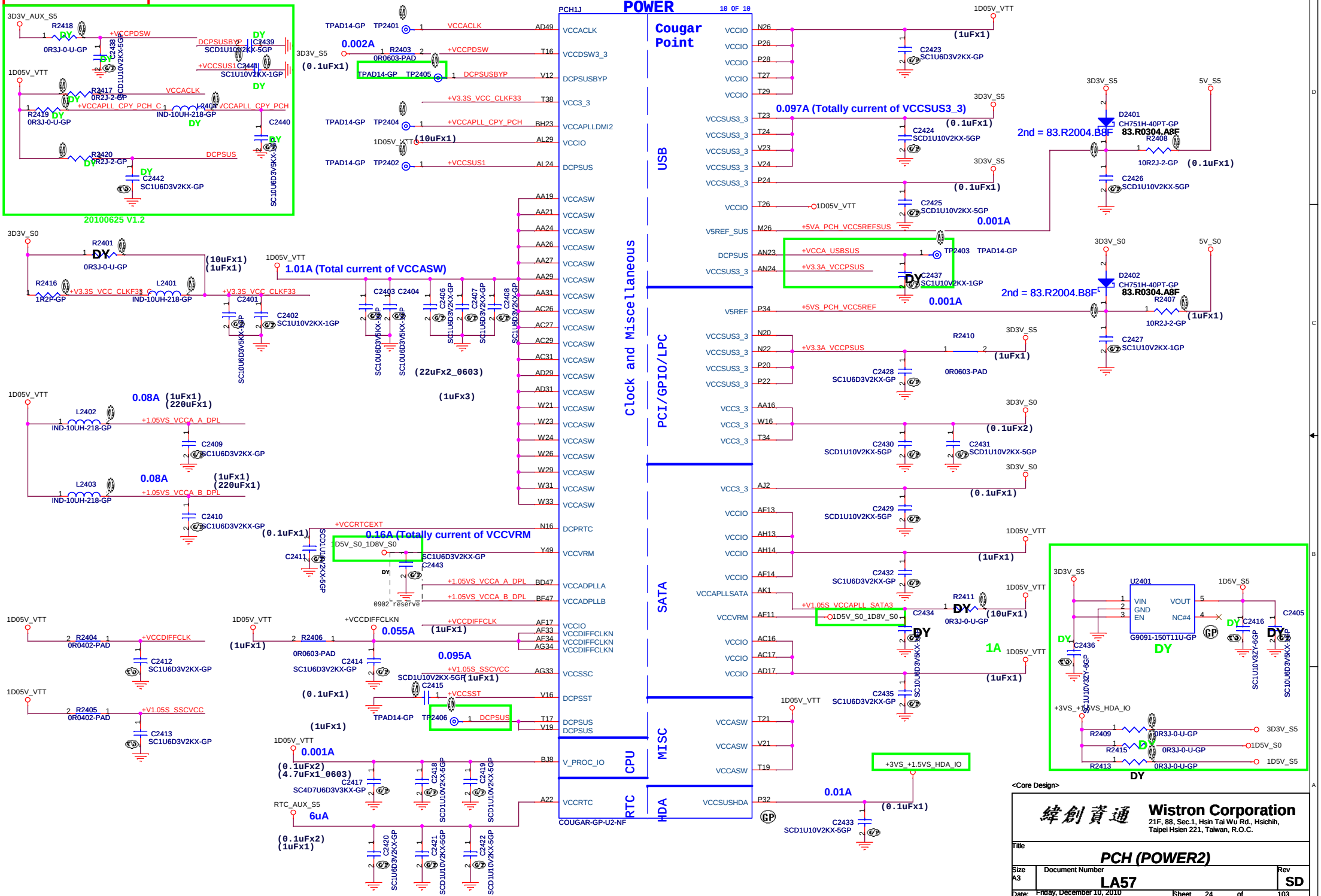
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

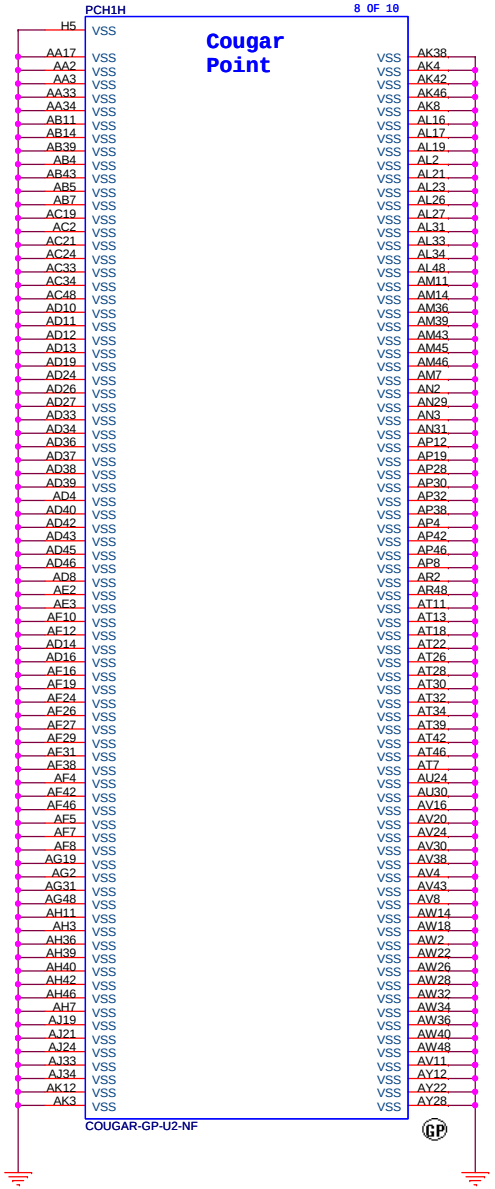
Size	Document Number	Rev
A3	LA57	SD

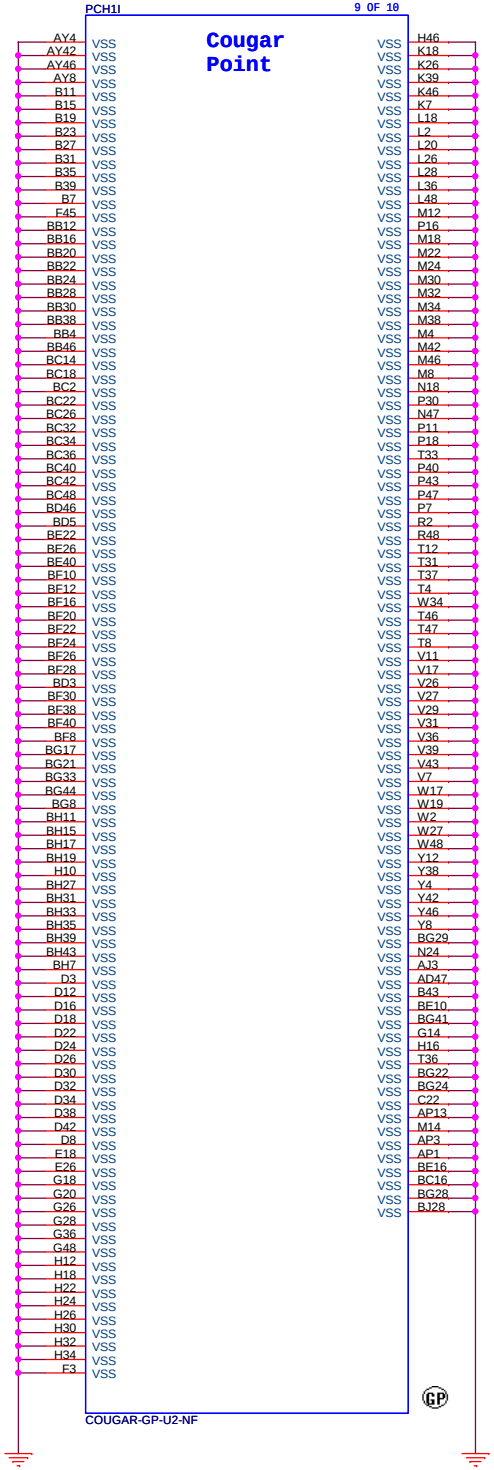
Date: Friday, December 10, 2010 Sheet 23 of 103

SSID = PCH


POWER
Cougar Point
PCH1J
10 OF 10
COUGAR-GP-U2-NF
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
20100625 V1.2
0.002A
1.01A (Total current of VCCASW)
0.08A (1uFx1) (220uFx1)
0.08A (1uFx1) (220uFx1)
0.16A (Totally current of VCCVRM
0.055A
0.095A
0.001A
6uA
0.097A (Totally current of VCCSUS3_3)
0.001A
0.001A
1A
0.01A
2nd = 83.R2004.B8F
83.R0304.A8F
2nd = 83.R2004.B8F
83.R0304.A8F
+3VS_+1.5VS_HDA_IO
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (POWER2)
Size A3
Document Number LA57
Rev SD
Date: Friday, December 10, 2010
Sheet 24 of 103

SSID = PCH





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 25 of 103

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<Core Design>

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Title: ***Power Button***

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 26 of 103

SSID = KBC

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3DV_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

G Sensor ID:
High: ST
Low : ADI

71.00795.A0G support G-sensor

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

<-------- TP
<-------- BATTERY / CHARGER
<-------- PCH / eDP

Need very close to EC

EC GPIO standard PH/PL

Prevent BIOS data loss solution

EC_GPIO47 High Active

LILI Multi GPIO setting

BOM ctl Model_ID UMA=64.64925.6DL

MODEL_ID_AD(Pin100)	Pull-Low Register	Pull-High Register	Voltage
V/B 57 UMA	100.0 K	64.9 K: 64.64925.6DL	2.001 V
V/B 57 OPTIMUS	100.0 K	76.8 K: 64.76825.6DL	1.867 V
Z 57 UMA	100.0 K	100.0 K	1.650 V
Z 57 OPTIMUS	100.0 K	150.0 K(63.15434.L0L)	1.32 V

<Core Design>
蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: KBC Nuvoton NPCE795
Size: A3 | Document Number: LA57 | Rev: SD
Date: Friday, December 30, 2010 | Sheet 27 of 103

SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA 0905 change to 390p

3 — Q6 MMBT3904WT1G-GP — C183 SC390P50V2KX-GP

2 — Q42 MMBT3904WT1G-GP — C434 SC390P50V2KX-GP DY — 2200p close to smsc2103 chip — C569 SC2200P50V2KX-2GP — REMOTE2- / REMOTE2+

between CPU, VGA and DIMM on bottom side

T8

1 — Q9 MMBT3904WT1G-GP — 2200p close to smsc2103 chip — C389 SC2200P50V2KX-2GP — H_THERMDA / H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

3D3V_S0 — R280 6K8R2J-GP — SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0 — R260 68R2-GP — 2103_VDD — C388 SCD1U10V2KX-4GP

U31 EMC2103-2-AP-GP

VDD, DP1, DN1, DP2/DN3, ND2/DP3, SYS_SHDN#, ALERT#, SMCLK, SMDATA, GND, GND, TRIP_SET, SHDN_SEL, TACH, PWM, GPIO1, GPIO2

H_THERMDA, H_THERMDC, REMOTE2+, REMOTE2-

SC 1203

THERM_SCI# — TP66 TPAD14-GP

THERM_SYS_SHDN# — THERM_SCI#_R — R272 0R0402-PAD

27,78,86 SMBC_THERM

27,78,86 SMBD_THERM

2103_4 — TP65 TPAD14-GP

2103_5 — TP67 TPAD14-GP

FAN_TACH_R — RN49 SRN10KJ-5-GP — 3D3V_S0

TRIP_SET R276 — 2K05R2F-GP — T8 = 105

SHDN_SEL

D2802 CH551H-30PT-GP — FAN_TACH / FAN_PWM

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

83.R5003.C8F

pin6, ALERT# OD

pin7, SYS_SHDN# OD

Close to connector

5V_S0 — AFTP1133

D2801 CH551H-30PT-GP — 83.R5003.C8F — 2ND = 83.R5003.H8H — 3rd = 83.5R003.08F — DY

C39 SC4D7U6D3V3KX-GP — SA 0905

R426 10KR2J-3-GP

FAN_TACH

FAN_PWM — R427 0R0402-PAD — FAN_PWM_C

ACES-CON4-4-GP FAN1

4 WIRE PWM Fan Control circuit

EC2801 SC1KP50V2KX-1GP — EC2802 SC1KP50V2KX-1GP — DY — 20101019 DY EC2802

AFTP1134

20.F0765.004

2ND = 20.F1426.004

FAN_TACH — AFTP1128

FAN_PWM_C — AFTP1131

3D3V_AUX_S5 — D2803 BAT54PT-GP — 83.00054.T81 — 2ND = 83.BAT54.D81 — 3rd = 83.BAT54.S81 — DY

27,36,86 PURE_HW_SHUTDOWN#

R2812 10KR2J-3-GP — DY

C2811 SCD1U10V2KX-4GP — DY

Q2802 2N7002A-7-GP — D — S — G — THERM_SYS_SHDN#

3D3V_S0 — R2809 100KR2J-1-GP

IMVP_PWRGD_G

R2810 0R2J-2-GP — DY — 3D3V_S0

R2811 0R2J-2-GP — IMVP_PWRGD 36,42

84.2N702.E31

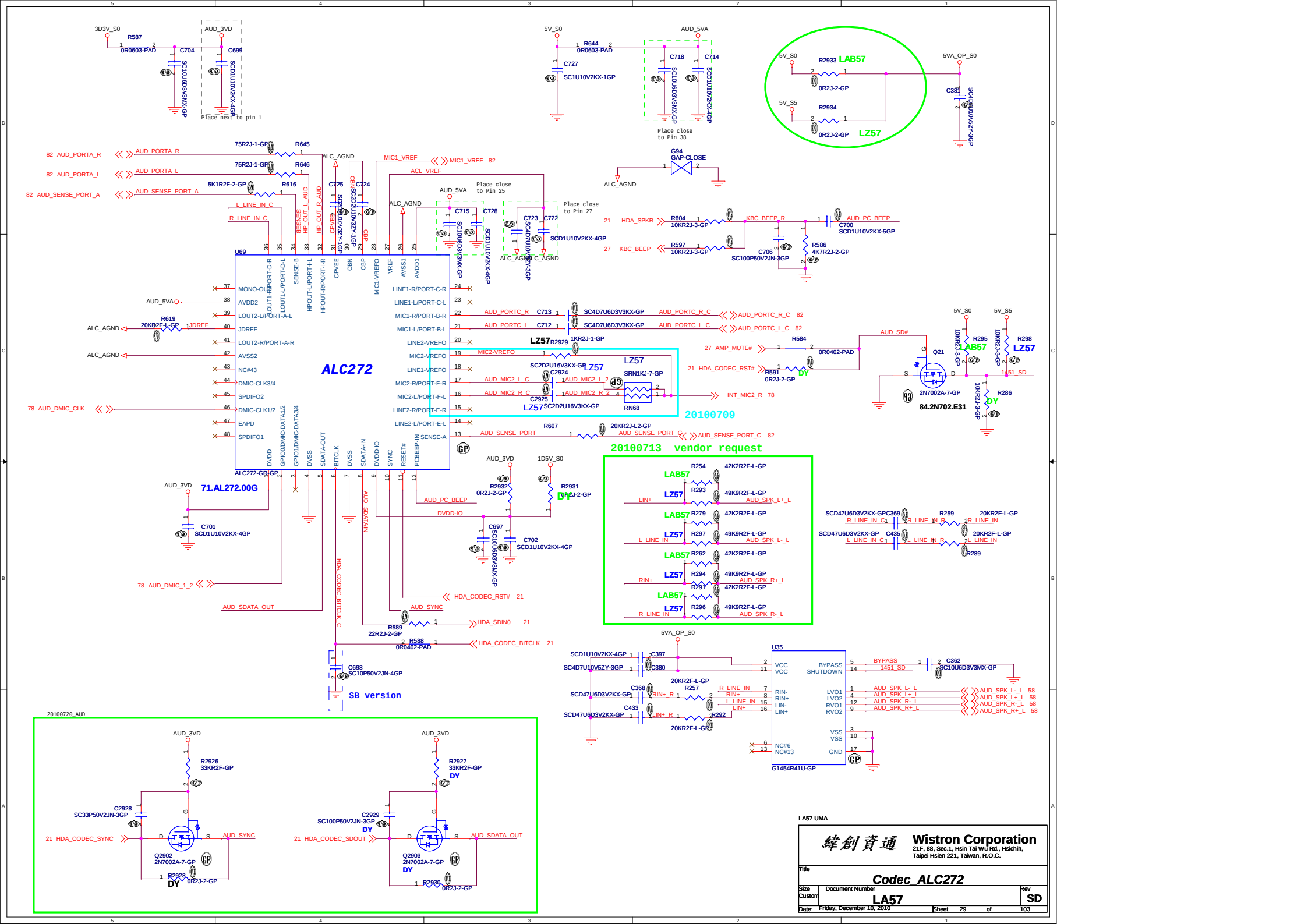
LA57 UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 28 of 103


ALC272
ALC272-GP.GP
U69
71.AL272.00G
20100709
20100713 vendor request
SB version
20100720_AUD
LA57 UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Codec_ALC272
Size
Custom
Document Number
LA57
Rev
SD
Date: Friday, December 10, 2010
Sheet 29 of 103

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LA57 UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 30 of 103

25MHz XTAL

X2 XTAL-25MHZ-102-GP
2ND = 82.30020.791
R3130 1MR3J-L-GP
C3103 SC15P50V2JN-2-GP
C3148 SC12P50V2JN-3GP

Pin-XTAL2 is External Clock Input Pin.
R3121 is need when using external clock source.

R3123 2K49R2F-GP

U9304 RTL8111E-VB-GR-GP

R3125 0R0402-PAD
R3124 0R2J-2-GP

R3135 0R3J-0-U-GP
Q3103 AO3419L-GP
Q3104 2N7002A-7-GP 84.2N702.E31
C3150 SC22U10V2KX-1GP
C3151 SCD1U10V2KX-4GP
C3152 SC1U10V2KX-1GP
C3153 SCD22U10V2KX-1GP

L1 IND-4D7UH-192-GP
C3146 SC22U4V3MX-GP
C3129 SCD1U10V2KX-4GP

Layout Note: Close to U3101 pin C3106 ~ C3112

C3130 C3131 C3132 C3133 C3134 C3138 C3139 SCD1U16V2ZY-2GP

R3131 0R0402-PAD
C3128 SC1U10V2KX-1GP
C3149 SCD1U16V2ZY-2GP

Layout Note: Close to U3101 pin C3113&C3114
C3113 value modify to 1uF capacitor

R3134 0R0603-PAD
C3135 C3140 C3141 C3142 C3143 C3144 SCD1U16V2ZY-2GP
C3136 SCD1U25V3KX-GP
C3137 SC4D7U6D3V3KX-GP

Layout Note: Close to U3101 pin C3115 ~ C3120
C3122 change to 4.7uF X5R type capacitor

Make sure PCIE_Wake# & PCIE_CLK_LAN_RQ1#connected to 10K resistor pull high close to PCH side

R3136 1KR2J-1-GP
R3119 15KR2J-1-GP
R3120 1KR2J-1-GP
R3122 10KR2J-3-GP
R3126 10KR2J-3-GP
R3128 10KR2J-3-GP
R3127 0R0402-PAD
R3129 0R0402-PAD

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111E
Size: A3 | Document Number: LA57 | Rev: SD
Date: Friday, December 10, 2010 | Sheet 31 of 103

<Core Design>

緯創資通 **Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

RTS5159 (CARD READER)

Size	Document Number	Rev
A3	**LA57**	**SD**

Date: Friday, December 10, 2010 Sheet 32 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 33 of 103

(Blanking)

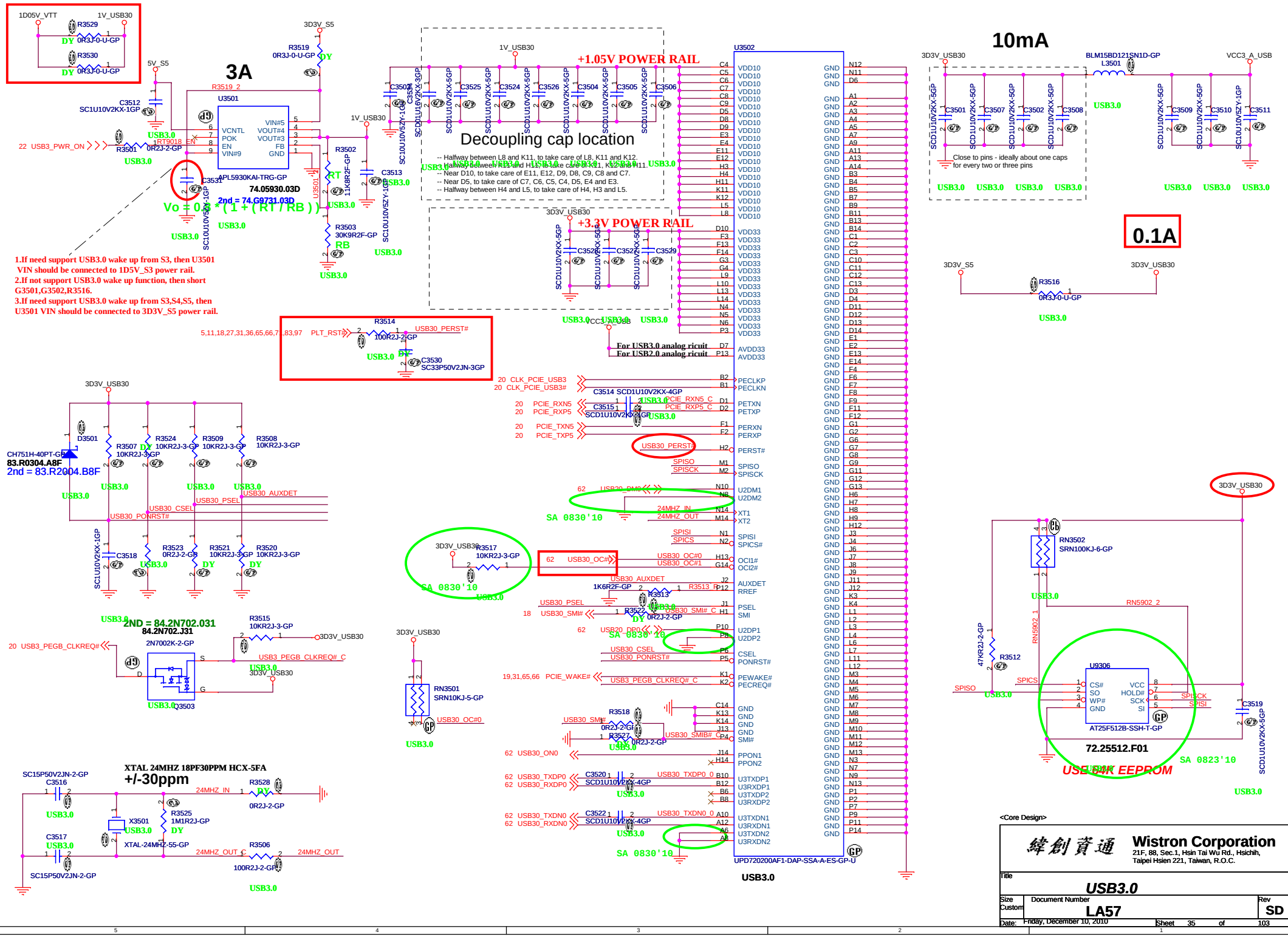
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

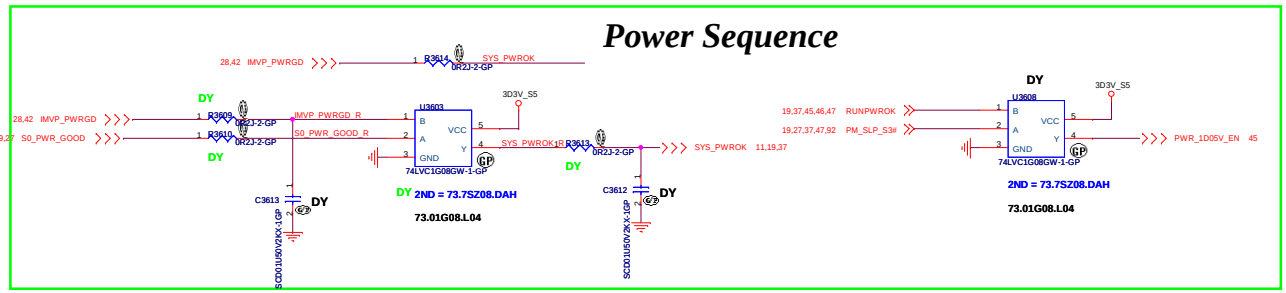
Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 34 of 103

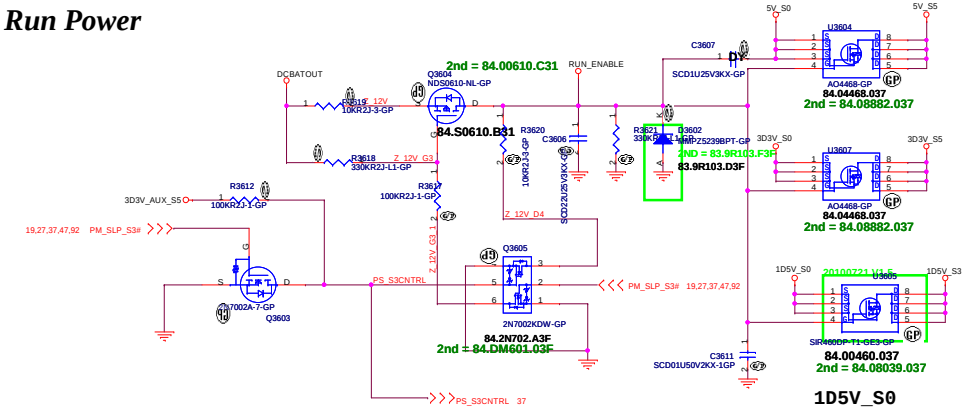

1D05V_VTT
1V_USB30
R3529
0R3J-0-U-GP
R3530
0R3J-0-U-GP
3A
5V_S5
3D3V_S5
R3519
0R3J-0-U-GP
R3519_2
U3501
C3512
SC1U10V2KX-1GP
VCNTL
POK
EN
VIN#9
VIN#5
VOUT#4
VOUT#3
FB
GND
APL5930KAI-TRG-GP
74.05930.03D
2nd = 74.G9731.03D
22 USB3_PWR_ON
R3501
0R2J-2-GP
RT9018_EN
C3531
SC10U10V5ZY-1GP
Vo = 0.8 * (1 + (RT / RB))
R3502
1K8R2F-GP
RT
R3503
30K9R2F-GP
RB
C3513
SC10U10V5ZY-1GP
1V_USB30
+1.05V POWER RAIL
C3507
C3525
C3524
C3526
C3504
C3505
C3506
SCD1U10V2KX-5GP
SC10U10V5ZY-1GP
Decoupling cap location
-- Halfway between L8 and K11, to take care of L8, K11 and K12.
-- Halfway between K12 and H11, to take care of K12, K11 and H11.
-- Near D10, to take care of E11, E12, D9, D8, C9, C8 and C7.
-- Near D5, to take care of C7, C6, C5, C4, D5, E4 and E3.
-- Halfway between H4 and L5, to take care of H4, H3 and L5.
3D3V_USB30
+3.3V POWER RAIL
C3528
C3527
C3529
U3502
VDD10
VDD33
AVDD33
GND
For USB3.0 analog ricuit
For USB2.0 analog ricuit
UPD720200AF1-DAP-SSA-A-ES-GP-U
USB3.0
10mA
3D3V_USB30
BLM15BD121SN1D-GP
L3501
VCC3_A_USB
C3501
C3507
C3502
C3508
C3509
C3510
C3511
SC1U10V5ZY-1GP
Close to pins - ideally about one caps for every two or three pins
0.1A
3D3V_S5
R3516
0R3J-0-U-GP
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 1D5V_S3 power rail.
2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.
R3514
100R2J-2-GP
PLT_RST
USB30_PERST#
C3530
SC33P50V2JN-3GP
CH751H-40PT-GP
83.R0304.A8F
2nd = 83.R2004.B8F
D3501
R3507
10KR2J-3-GP
R3524
10KR2J-3-GP
R3509
10KR2J-3-GP
R3508
10KR2J-3-GP
USB30_AUXDET
USB30_CSEL
USB30_PSEL
USB30_PONRST#
C3518
SC1U10V2KX-1GP
R3523
0R2J-2-GP
R3521
10KR2J-3-GP
R3520
10KR2J-3-GP
2ND = 84.2N702.031
84.2N702.J31
2N7002K-2-GP
Q3503
R3515
10KR2J-3-GP
20 USB3_PEGB_CLKREQ#
USB3_PEGB_CLKREQ# C
R3517
10KR2J-3-GP
62 USB30_OC#
USB30_OC#0
USB30_OC#1
SA 0830'10
RN3501
SRN10KJ-5-GP
USB30_OC#0
20 CLK_PCIE_USB3
20 CLK_PCIE_USB3#
C3514 SCD1U10V2KX-4GP
C3515 SCD1U10V2KX-4GP
20 PCIE_RXN5
20 PCIE_RXP5
PCIE_RXN5_C
PCIE_RXP5_C
20 PCIE_TXN5
20 PCIE_TXP5
USB30_PERST#
SPISO
SPISCK
62 USB20_DM0
24MHZ_IN
24MHZ_OUT
SPISI
SPICS
SPICS#
1K6R2F-GP
R3513
USB30_PSEL
18 USB30_SMI#
USB30_SMI#_C
R3522
0R2J-2-GP
62 USB20_DP0
USB30_CSEL
USB30_PONRST#
19,31,65,66 PCIE_WAKE#
USB3_PEGB_CLKREQ#_C
R3518
0R2J-2-GP
USB30_SMI#
R3527
0R2J-2-GP
USB30_SMIB#_C
62 USB30_ON0
62 USB30_TXDP0
62 USB30_RXDP0
C3520 SCD1U10V2KX-4GP
USB30_TXDP0_0
62 USB30_TXDN0
62 USB30_RXDN0
C3522 SCD1U10V2KX-4GP
USB30_TXDN0_0
XTAL 24MHZ 18PF30PPM HCX-5FA
+/-30ppm
SC15P50V2JN-2-GP
C3516
C3517
SC15P50V2JN-2-GP
24MHZ_IN
R3528
0R2J-2-GP
R3525
1M1R2J-GP
X3501
XTAL-24MHZ-55-GP
24MHZ_OUT
R3506
100R2J-2-GP
24MHZ_OUT
3D3V_USB30
RN3502
SRN100KJ-6-GP
RN5902_2
RN5902_1
47KR2J-2-GP
R3512
SPICS
SPISO
U9306
CS#
SO
WP#
GND
VCC
HOLD#
SCK
SI
AT25F512B-SSH-T-GP
SPISCK
SPISI
C3519
SCD1U10V2KX-5GP
72.25512.F01
SA 0823'10
USE 64K EEPROM
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB3.0
Size
Custom
Document Number
LA57
Rev
SD
Date:
Friday, December 10, 2010
Sheet
35
of
103

Power Sequence



SSID = Reset.Suspend

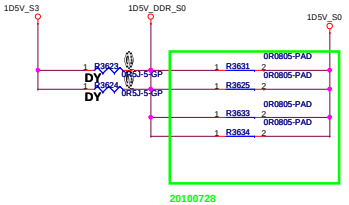
Run Power

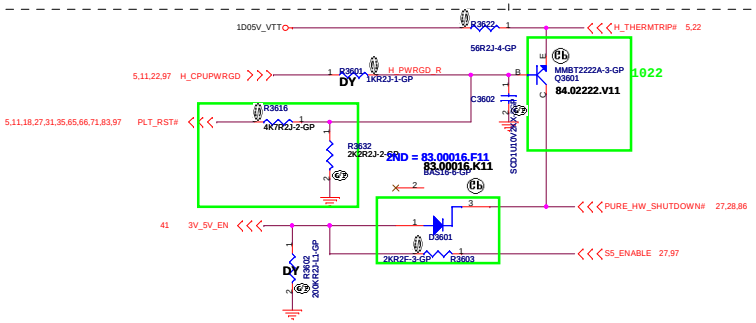


1D5V_S0

SIR460, SO-8
VGS=10V, Qg=16.8nC
Rdson=4.7m ohm

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A





LA57 UMA

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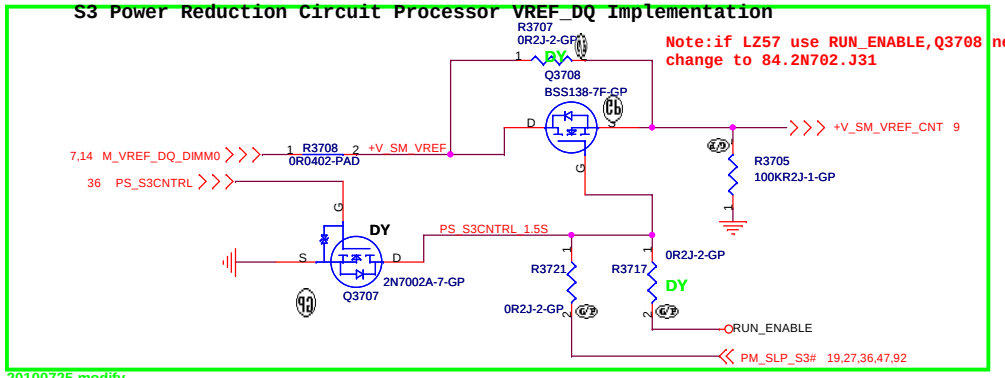
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A2	LA57	SD

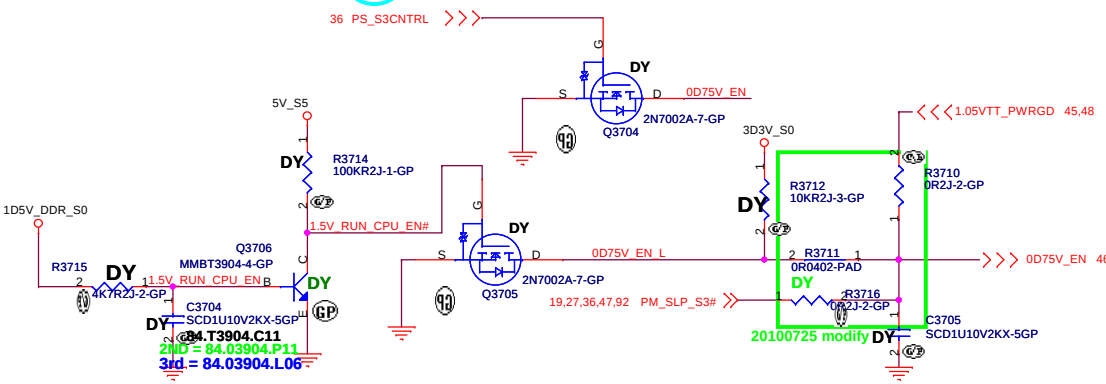
Date: Friday, December 10, 2010 Sheet 36 of 103

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

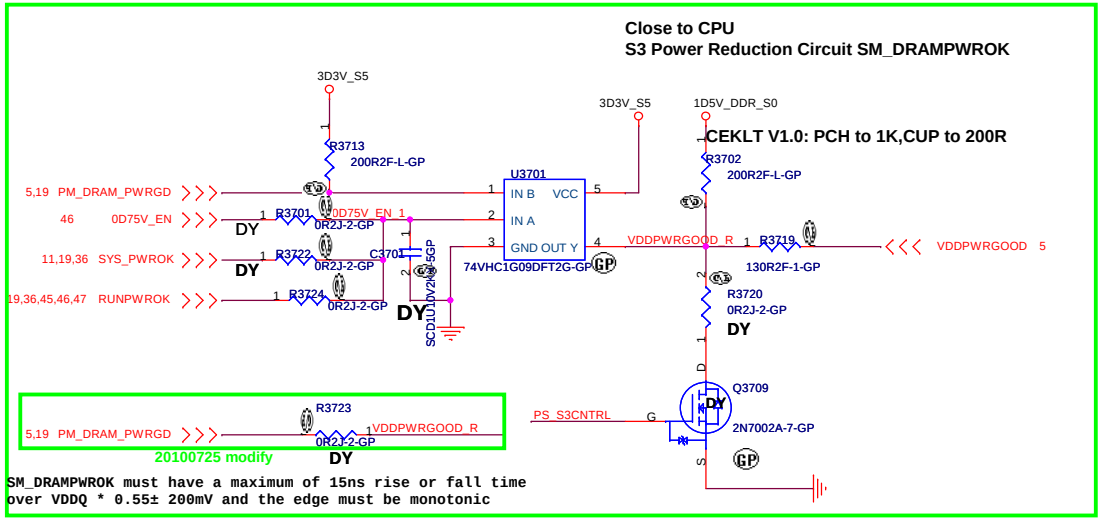


20100725 modify

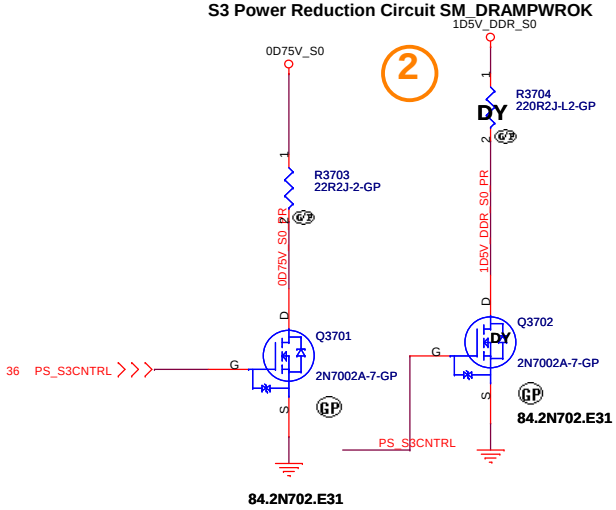
5 S3 Power Reduction X01 20091111



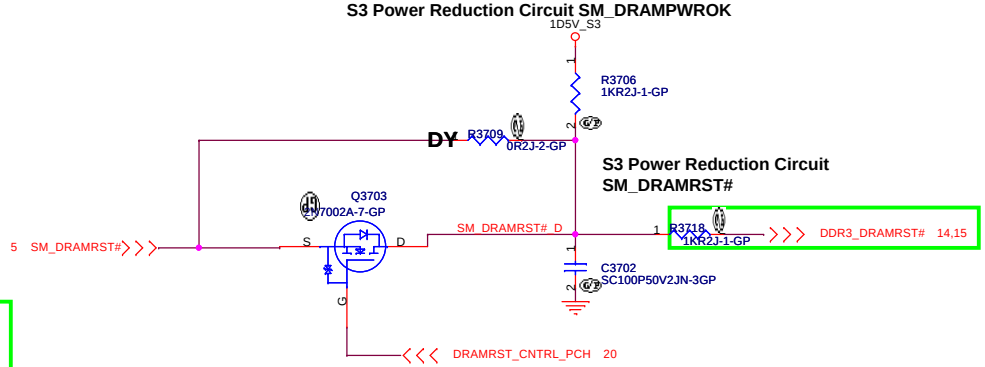
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

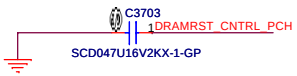


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK





<Core Design>

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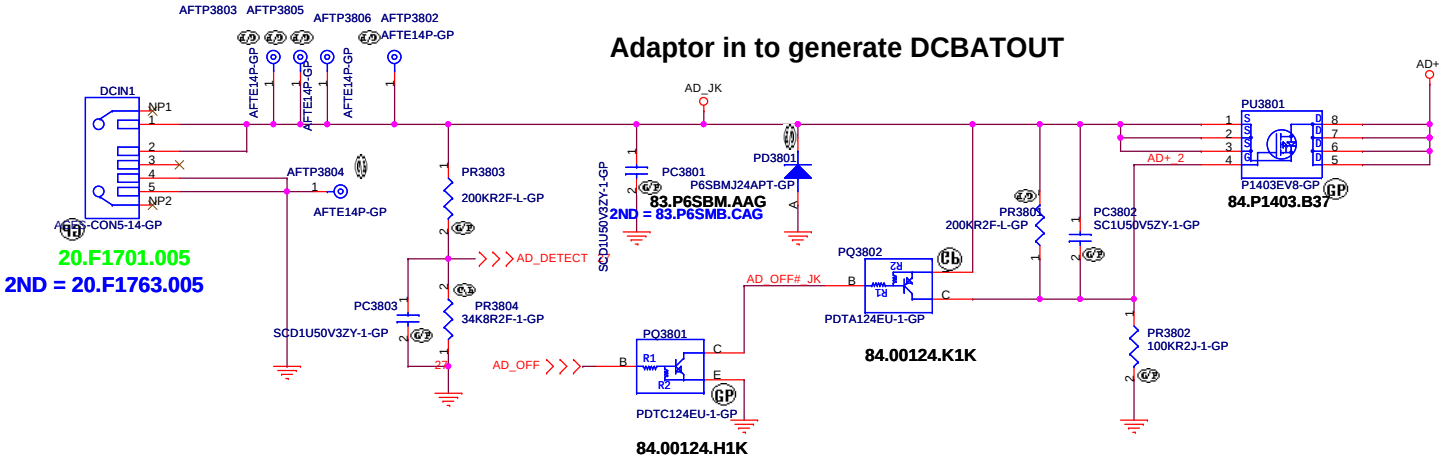
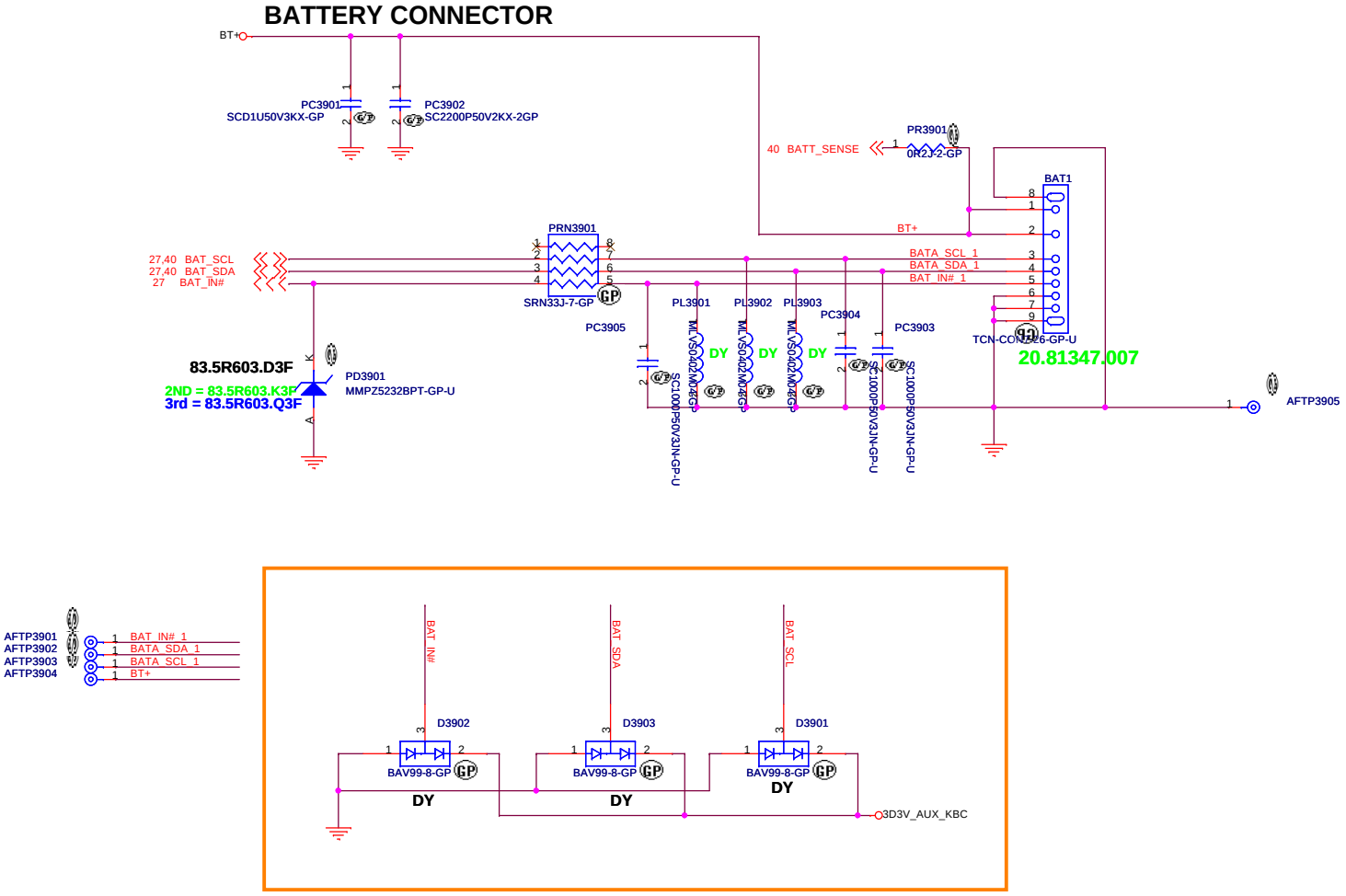
Title: **ADAPTER**		
Size: A3	Document Number: **LA57**	Rev: **SD**
Date: Friday, December 10, 2010	Sheet 37 of 103	



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN_JACK*		
Size	Document Number: LA57	Rev: SD
Date: Friday, December 10, 2010	Sheet 38 of 103	

BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
Size	Document Number LA57	Rev SD
Date: Friday, December 10, 2010	Sheet 39 of 103	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k			

NEAR

AD+

PU4001 P1403EV8-GP 84.P1403.B37

PR4002 100KR2J-1-GP

AD+_G_2

PR4001 10KR2F-2-GP

PR4003 49K9R2F-L-GP

AD+_G_1

DC_IN_D

PQ4001 2N7002KDW-GP 84.2N702.A3F

2nd = 84.DM601.03F

BQ24745_ACOK

PR4006 316KR3F-2-GP

PD4001 1SS400GPT-GP 83.00400.C1F 2nd = 83.1S400.B2F

PC4001 SC1U25V5KX-1GP

BQ24745_VREF

R1 121KR2F-L-GP PR4007 *90W(65W=64.28735.6DL)

R2 PR4008 49K9R2F-L-GP

CHG_AGND

AD+_TO_SYS

PR4004 D01R3721F-GP-U

20100518 WAYNE

PG4001 GAP-CLOSE-PWR-3-GP

PG4002 GAP-CLOSE-PWR-3-GP

STOP_CHG# connects to KBC

3D3V_AUX_S5 PR4009 10KR2F-2-GP STOP_CHG#

STOP_CHG

DCBATOUT

PU4002 P1403EV8-GP 84.P1403.B37

PD4002 SMF18A-GP 83.SMF18.AAH

PR4005 470KR2J-2-GP

PU4003 BQ24745RHDR-GP

BQ24745_DCIN

BQ24745_ACIN

BQ24745_CSSP

BQ24745_CSSN

BQ24745_ICOUT

BQ24745_BST

BQ24745_VDDP

BQ24745_LX1

BQ24745_IINP

BQ24745_FBO_RC

BQ24745_FBO

BQ24745_EAI

BQ24745_EAO

BQ24745_VREF

BQ24745_CHG_ON

BQ24745_EAO_RC

DCIN ACIN VDDSMB ACOK SCL SDA NC#14 VICM FBO EAI EAO VREF CE GND ICREF CSSP CSSN ICOUT BOOT VDDP UGATE PHASE LGATE PGND CSOP CSON NC#16 VFB GND

74.24745.073

PC4003 SCD1U50V3KX-GP

PC4004 SCD1U50V3KX-GP

CHG_AGND

2ND = 84.00412.037

79.10712.L02

83.R0203.08F 2nd = 83.1R003.I8F

PR4012 0R0402-PAD

PD4003 CH520S-30PT-GP

PC4009 SC1U10V3KX-3GP

PU4004 P2003BEA-GP

PC4025 SE100U25VM-L1-GP

PC4022 SC10U25V6KX-2GP

PC4005 SC10U25V6KX-2GP

PC4006 SCD1U25V2ZY-1GP

24745_HIGH_G

24745_LOW_G

PC4017 SCD1U50V3KX-GP

2ND = 68.5R610.10X

PL4001 IND-5D6UH-39-GP 68.5R610.10P

PR4017 D01R3721F-GP-U

PU4005 P2003BEA-GP

PG4003 GAP-CLOSE-PWR-3-GP

PG4004 GAP-CLOSE-PWR-3-GP

PC4018 SC10U25V6KX-2GP

PC4019 SC10U25V6KX-2GP

PC4020 SC10U25V6KX-2GP

PC4021 SC10U25V6KX-2GP

PC4022 SCD1U50V3KX-GP

DY

2ND = 84.00412.037

20100518 WAYNE

PR4010 49K9R2F-L-GP

PC4007 SCD01U50V2KX-1GP

PC4008 SC1U10V3KX-3GP

AC_IN

PR4011 0R0402-PAD

27,39 BAT_SCL

27,39 BAT_SDA

3D3V_AUX_S5

PR4013 0R0402-PAD

AD_IA

PC4010 SC150P50V2JN-3GP

PR4014 4K7R2J-2-GP

PR4015 200KR2F-L-GP

PC4011 SC220P50V2KX-3GP

PC4012 SC2200P50V2KX-2GP

PR4016 7K5R2F-1-GP

PC4013 SC56P50V2JN-2GP

PC4014 SC1U10V3KX-3GP

PC4015 SCD1U25V2ZY-1GP

BATT_SENSE

BATT_SENSE 39

PC4016 SCD1U50V3KX-GP

MAX8731A_CSIP

MAX8731A_CSIN

PR4018 0R2J-2-GP

PRN4001 SRN100KJ-8-GP-U

AC_IN

CHG_ON#

PQ4002 2N7002A-7-GP 84.2N702.E31

C4001 SCD1U10V2KX-4GP

AC_IN to KBC

<Core Design>

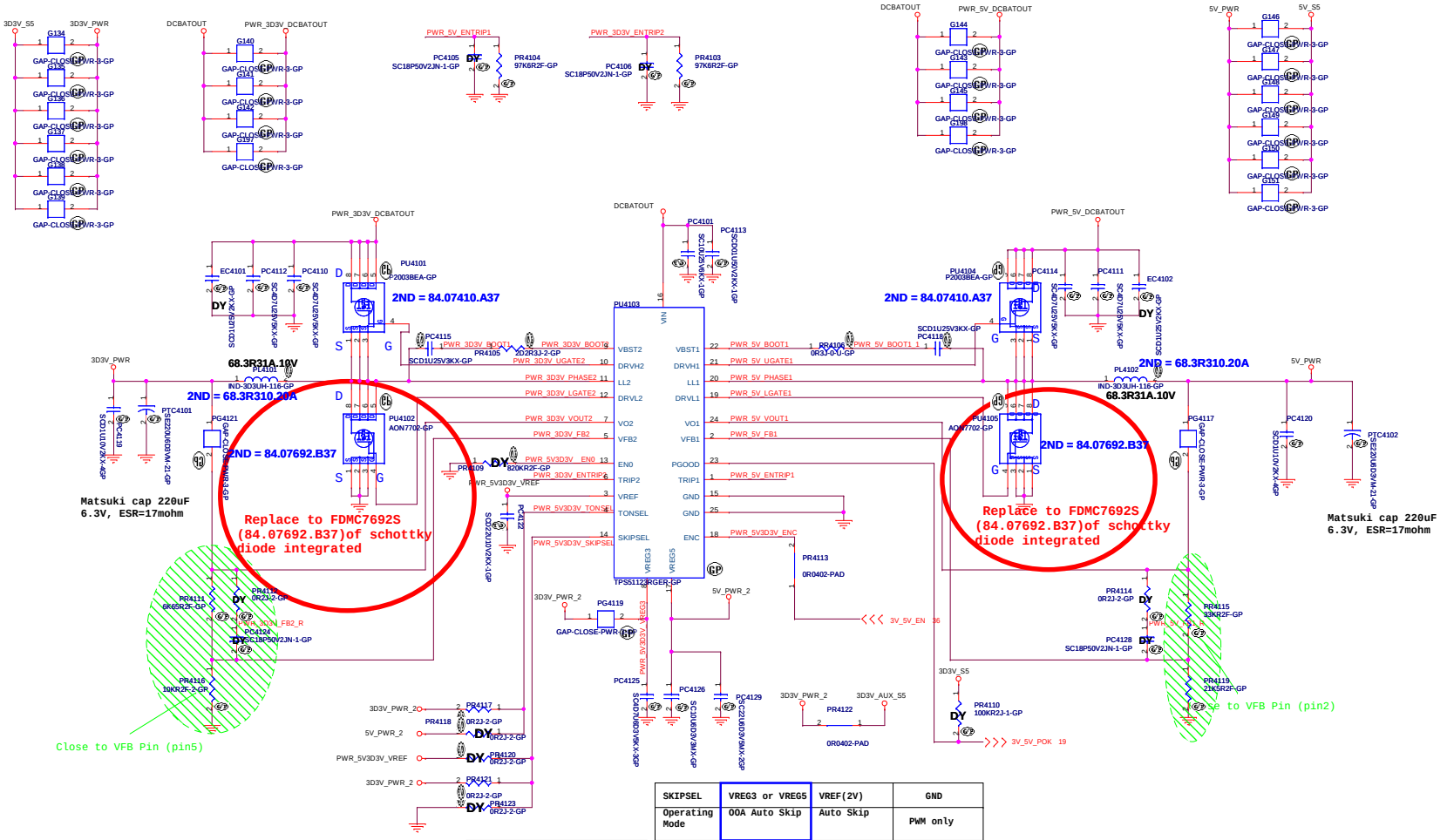
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24745

Size | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 40 of 103

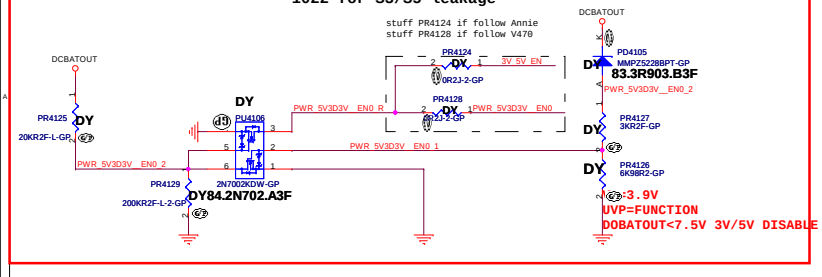
SSID = PWR.Plane.Regulator_5v3p3v



TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

1022 for S3/S5 leakage



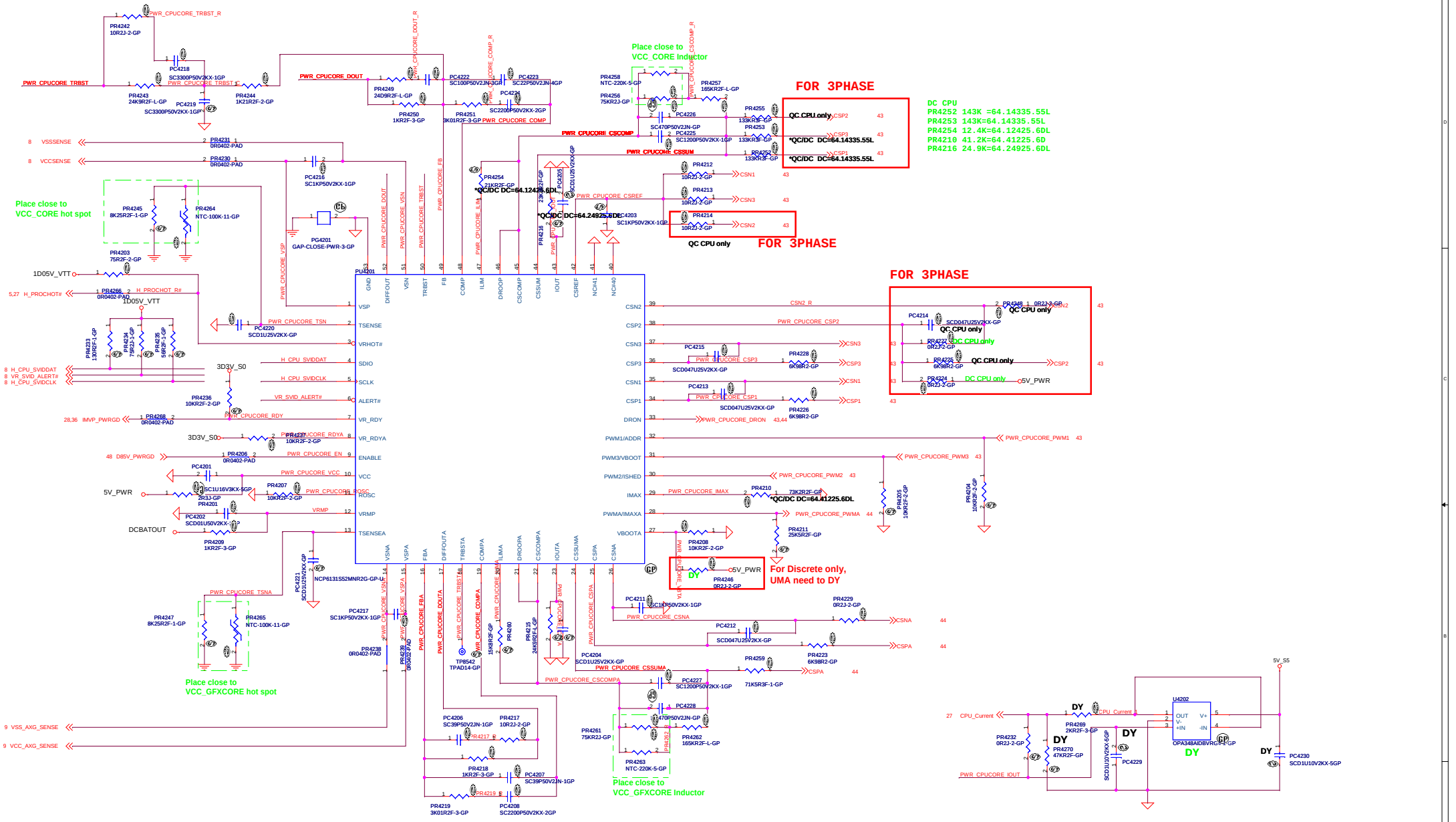
<Core Design>

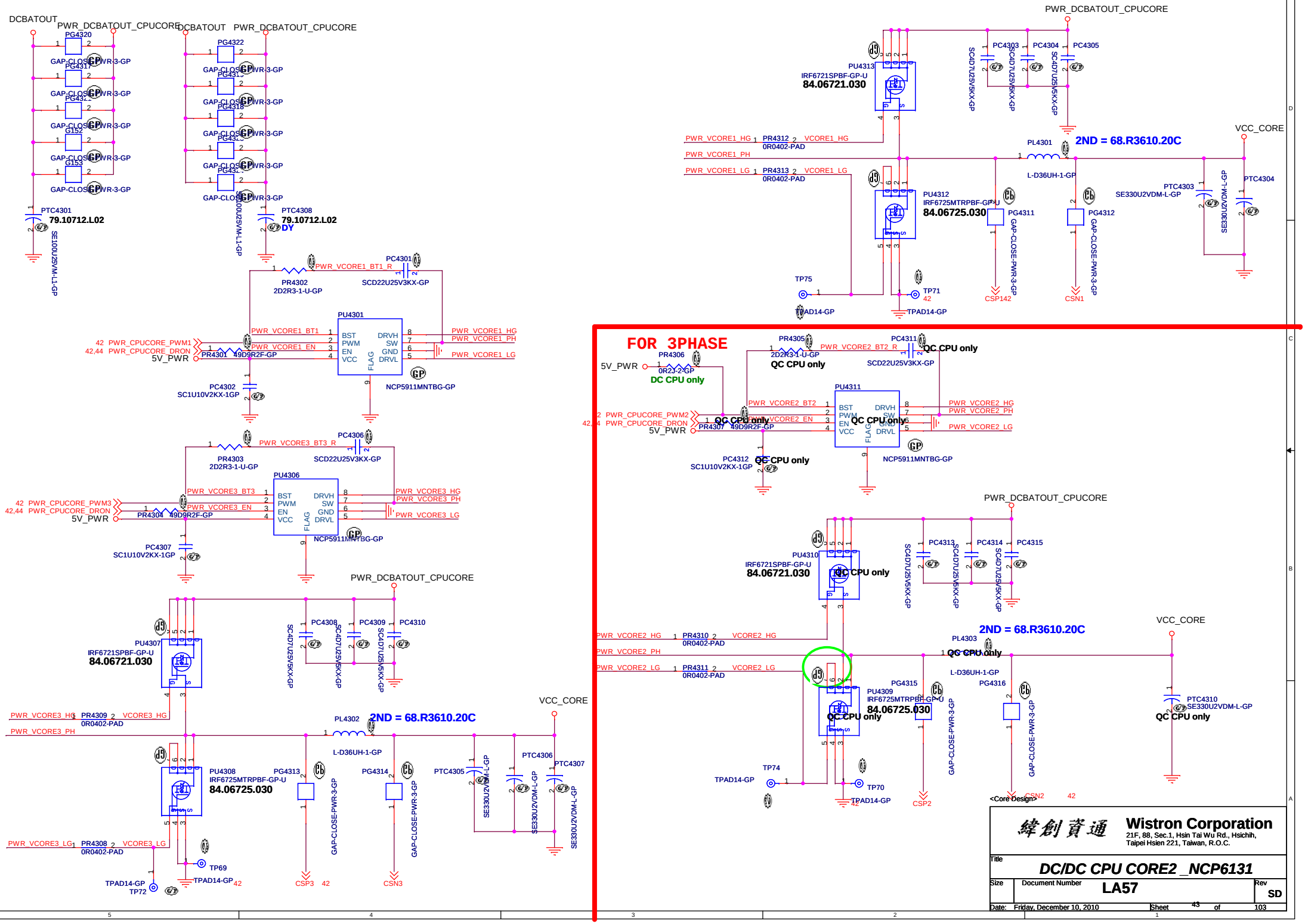
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

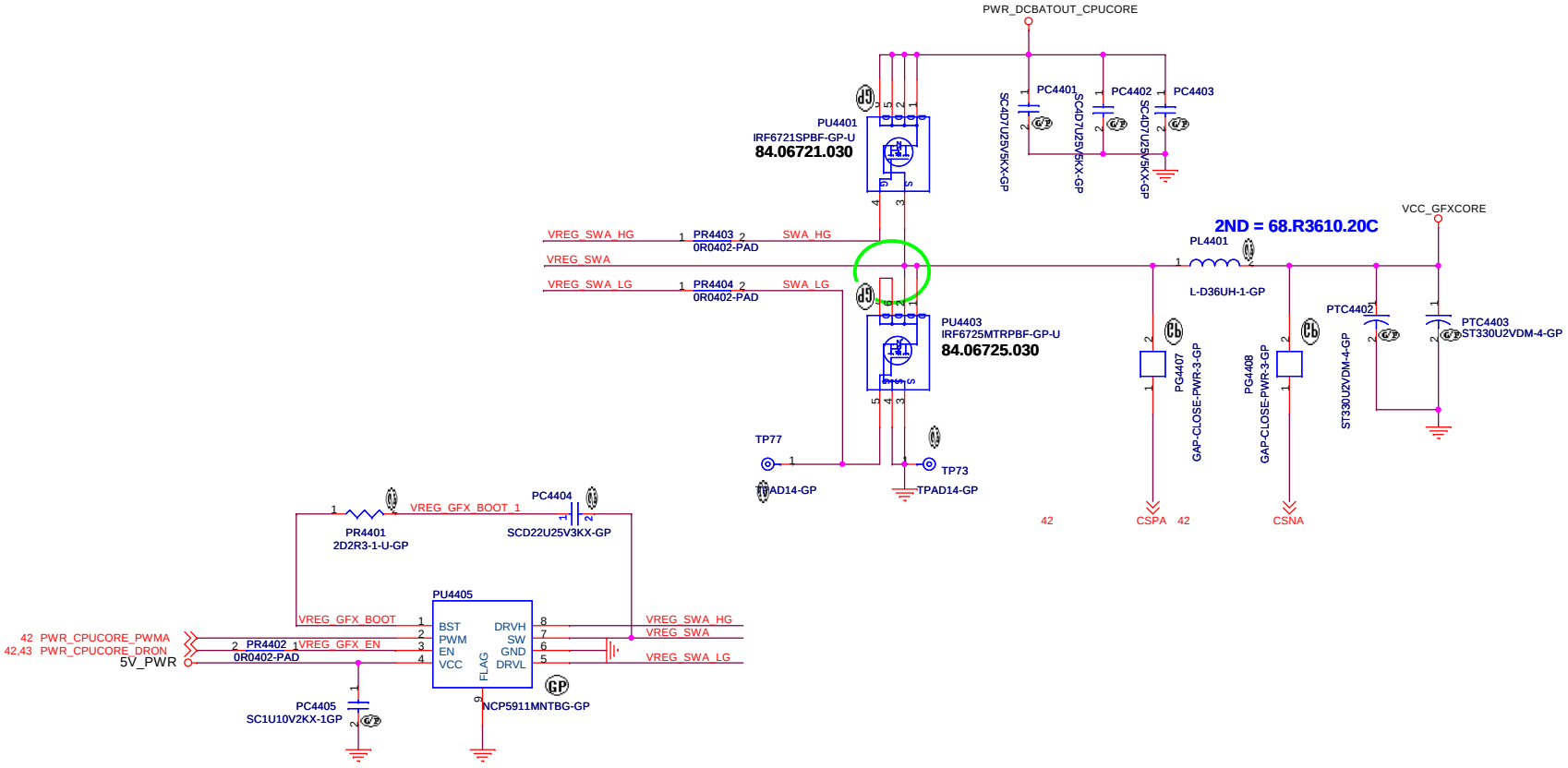
Title: DC/DC 3D3V5V

Size	Document Number	Rev
	LA470	SD

Date: Friday, December 10, 2010 Sheet 41 of 103


Place close to VCC_CORE Inductor
FOR 3PHASE
DC CPU
PR4252 143K =64.14335.55L
PR4253 143K=64.14335.55L
PR4254 12.4K=64.12425.6DL
PR4210 41.2K=64.41225.6D
PR4216 24.9K=64.24925.6DL
QC CPU only
*QC/DC DC=64.14335.55L
*QC/DC DC=64.12425.6DL
*QC/DC DC=64.24925.6DL
*QC/DC DC=64.41225.6DL
Place close to VCC_CORE hot spot
Place close to VCC_GFXCORE hot spot
Place close to VCC_GFXCORE Inductor
For Discrete only, UMA need to DY
DY
DC CPU only
NCP6131SS2MNR2G-GP-U
OPA348AIDBVRG4-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DC/DC CPU CORE1 _NCP6131
LA57
SD
Friday, December 10, 2010
42
103


DCBATOUT
PWR_DCBATOUT_CPUCORE
PG4320
PG4317
PG4321
PG4319
PG4322
PG4318
PG4323
PG4324
GAP-CLOSE-PWR-3-GP
PTC4301
79.10712.L02
SE100U25VM-L1-GP
PTC4308
79.10712.L02
DY
SE100U25VM-L1-GP
PR4302
2D2R3-1-U-GP
PC4301
SCD22U25V3KX-GP
PWR_VCORE1_BT1_R
PU4301
PWR_VCORE1_BT1
PWR_VCORE1_EN
PWR_VCORE1_HG
PWR_VCORE1_PH
PWR_VCORE1_LG
42 PWR_CPUCORE_PWM1
42,44 PWR_CPUCORE_DRON
5V_PWR
PR4301 49D9R2F-GP
BST
PWM
EN
VCC
DRVH
SW
GND
DRVL
FLAG
NCP5911MNTBG-GP
PC4302
SC1U10V2KX-1GP
PR4303
2D2R3-1-U-GP
PC4306
SCD22U25V3KX-GP
PWR_VCORE3_BT3_R
PU4306
PWR_VCORE3_BT3
PWR_VCORE3_EN
PWR_VCORE3_HG
PWR_VCORE3_PH
PWR_VCORE3_LG
42 PWR_CPUCORE_PWM3
42,44 PWR_CPUCORE_DRON
5V_PWR
PR4304 49D9R2F-GP
NCP5911MNTBG-GP
PC4307
SC1U10V2KX-1GP
PWR_DCBATOUT_CPUCORE
PU4307
IRF6721SPBF-GP-U
84.06721.030
PC4308
PC4309
PC4310
SC4D7U25V5KX-GP
PWR_VCORE3_HG
PR4309 2 VCORE3_HG
0R0402-PAD
PWR_VCORE3_PH
PL4302
2ND = 68.R3610.20C
L-D36UH-1-GP
VCC_CORE
PU4308
IRF6725MTRPBF-GP-U
84.06725.030
PG4313
PG4314
PTC4305
PTC4306
PTC4307
SE330U2VDM-L-GP
GAP-CLOSE-PWR-3-GP
PWR_VCORE3_LG
PR4308 2 VCORE3_LG
0R0402-PAD
TP69
TPAD14-GP
TP72
CSP3
CSN3
42
PWR_DCBATOUT_CPUCORE
PU4313
IRF6721SPBF-GP-U
84.06721.030
PC4303
PC4304
PC4305
SC4D7U25V5KX-GP
PWR_VCORE1_HG
PR4312 2 VCORE1_HG
0R0402-PAD
PWR_VCORE1_PH
PWR_VCORE1_LG
PR4313 2 VCORE1_LG
0R0402-PAD
PL4301
2ND = 68.R3610.20C
L-D36UH-1-GP
VCC_CORE
PU4312
IRF6725MTRPBF-GP-U
84.06725.030
PG4311
PG4312
PTC4303
PTC4304
SE330U2VDM-L-GP
TP75
TP71
42
TPAD14-GP
CSP142
CSN1
FOR 3PHASE
5V_PWR
PR4306
0R2J-2-GP
DC CPU only
PR4305
2D2R3-1-U-GP
QC CPU only
PC4311
SCD22U25V3KX-GP
PWR_VCORE2_BT2_R
PU4311
PWR_VCORE2_BT2
PWR_VCORE2_EN
PWR_VCORE2_HG
PWR_VCORE2_PH
PWR_VCORE2_LG
42 PWR_CPUCORE_PWM2
42,44 PWR_CPUCORE_DRON
PR4307 49D9R2F-GP
PC4312
SC1U10V2KX-1GP
NCP5911MNTBG-GP
PWR_DCBATOUT_CPUCORE
PU4310
IRF6721SPBF-GP-U
84.06721.030
PC4313
PC4314
PC4315
PWR_VCORE2_HG
PR4310 2 VCORE2_HG
0R0402-PAD
PWR_VCORE2_PH
PWR_VCORE2_LG
PR4311 2 VCORE2_LG
0R0402-PAD
PL4303
2ND = 68.R3610.20C
L-D36UH-1-GP
VCC_CORE
PU4309
IRF6725MTRPBF-GP-U
84.06725.030
PG4315
PG4316
PTC4310
SE330U2VDM-L-GP
TP74
TP70
TPAD14-GP
CSP2
CSN2
42
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC/DC CPU CORE2 _NCP6131
Size
Document Number
LA57
Rev
SD
Date: Friday, December 10, 2010
Sheet 43 of 103



<Core Design>

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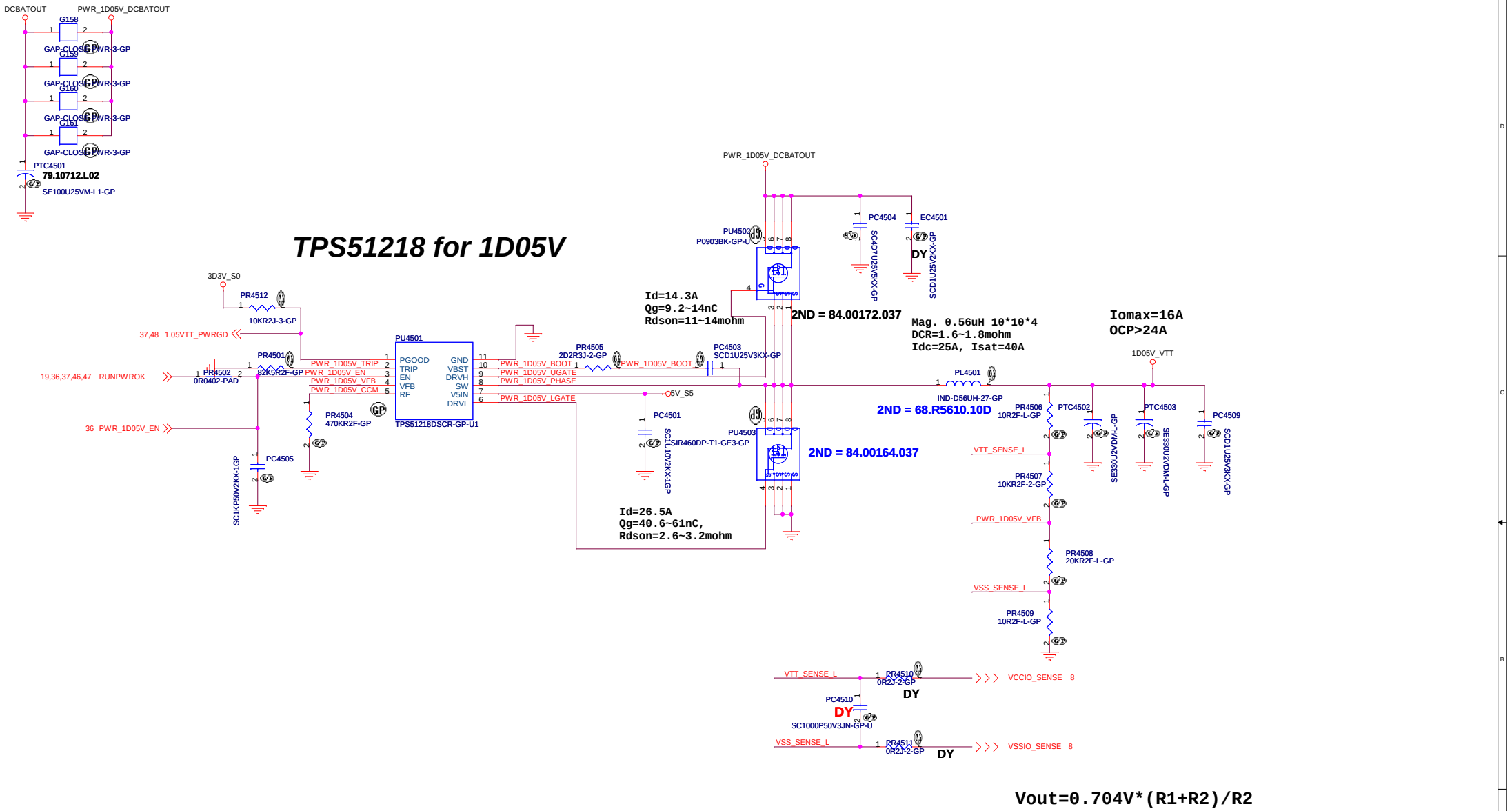
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC/DC CPU CORE3 _NCP6131***

Size	Document Number	Rev
	LA470	SD

Date: Friday, December 10, 2010 Sheet 44 of 103



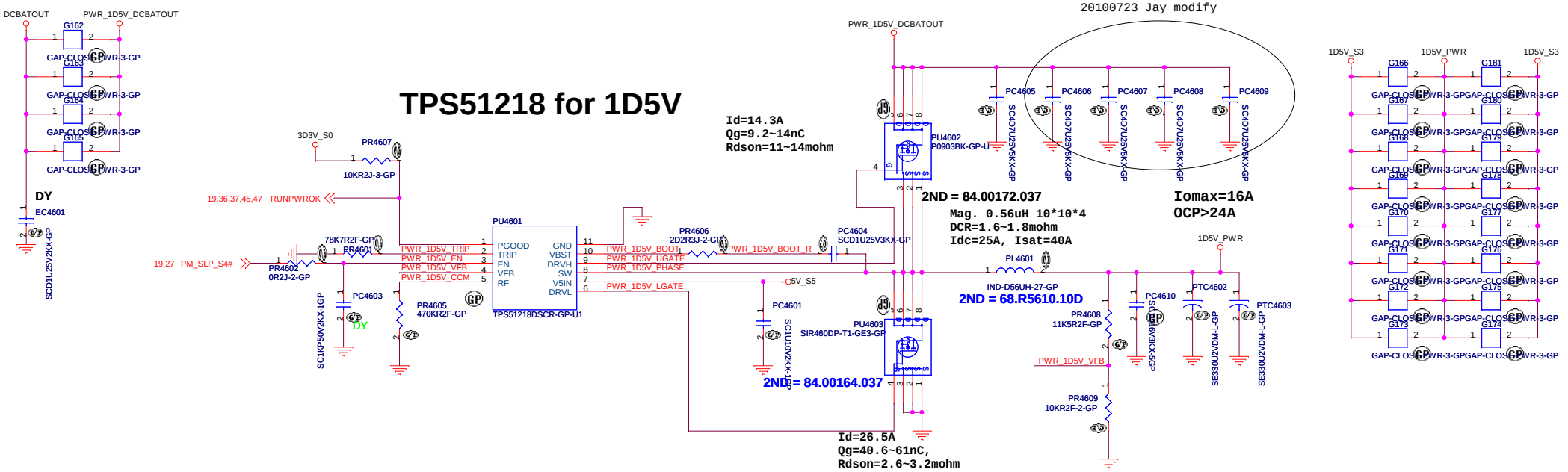
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

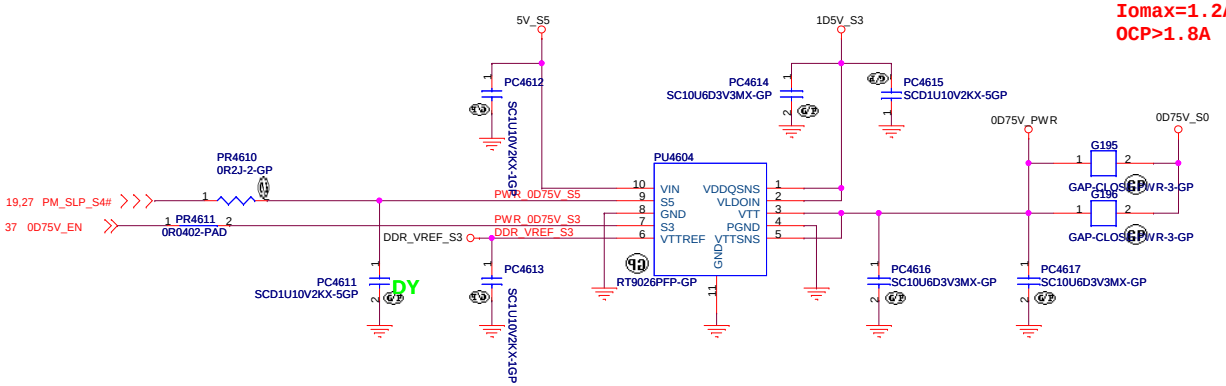
Title	TPS51218_1D05V	
Size	Document Number	Rev SD
Date: Friday, December 10, 2010	Sheet 45 of 103	

20100723 Jay modify

TPS51218 for 1D5V



RT9026 for 0D75V_S3



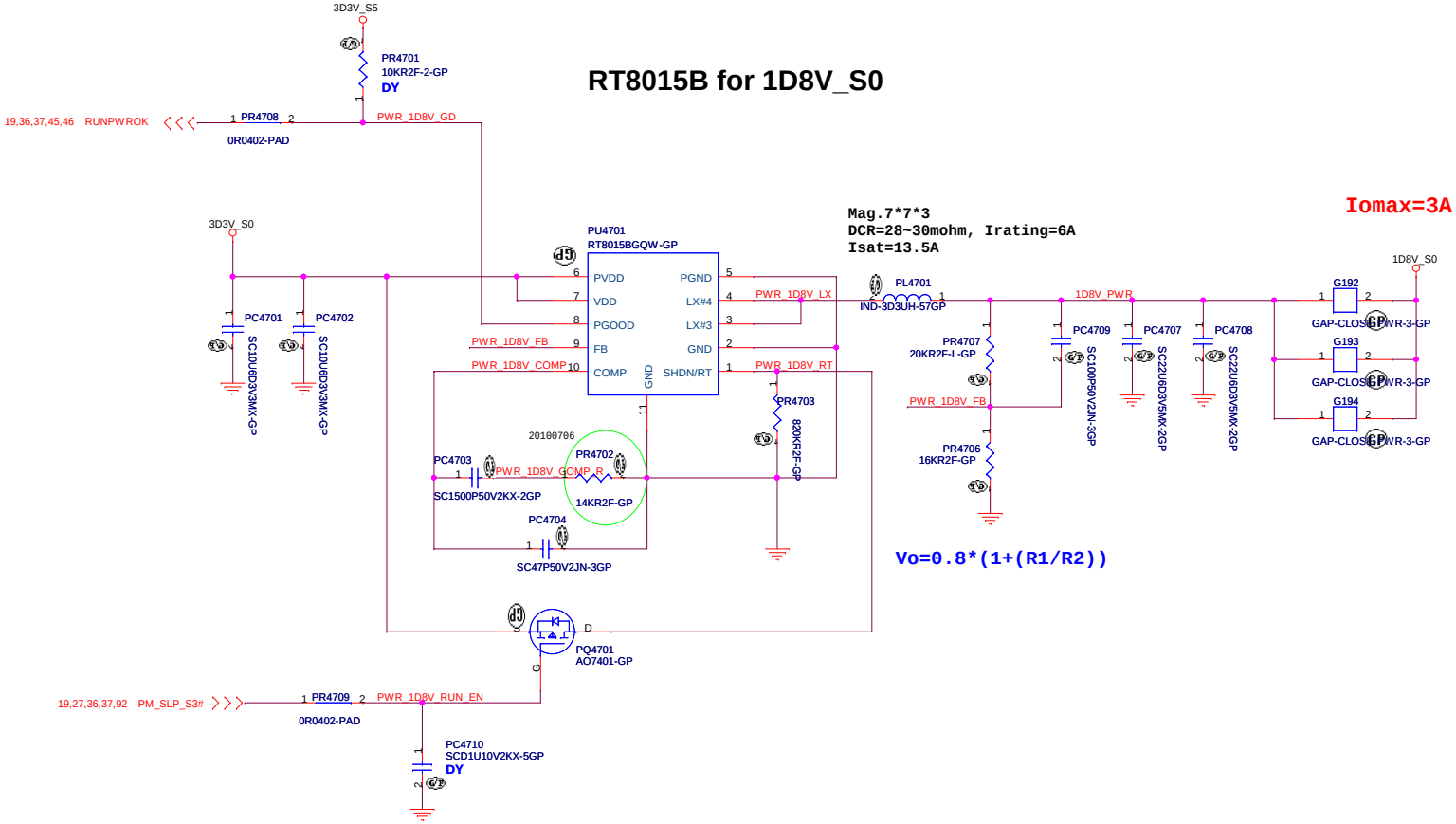
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		SD

Date: Friday, December 10, 2010 Sheet 46 of 103

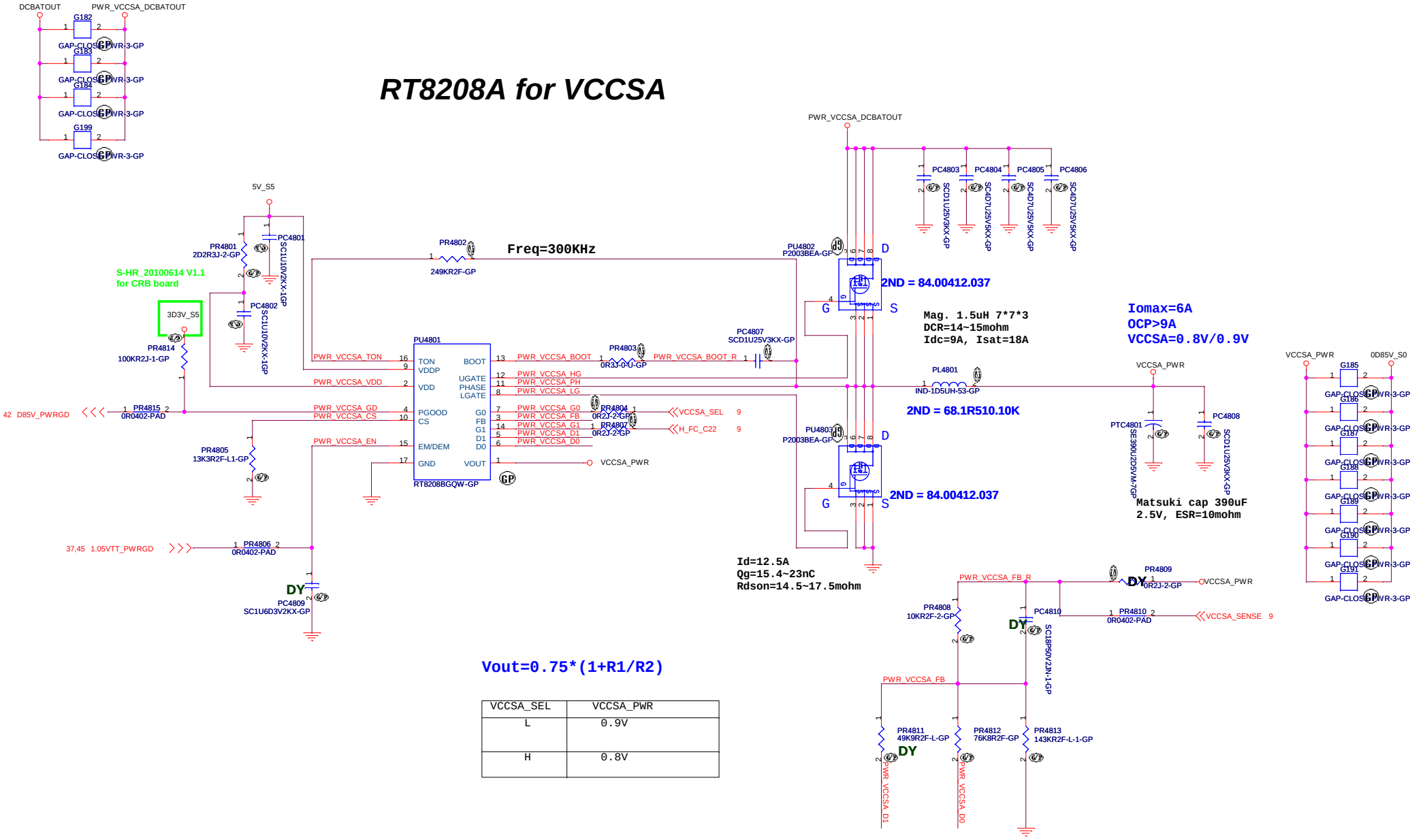


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D8V_RT9025	
Size	Document Number LA57	Rev SD
Date: Friday, December 10, 2010	Sheet 47 of 103	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

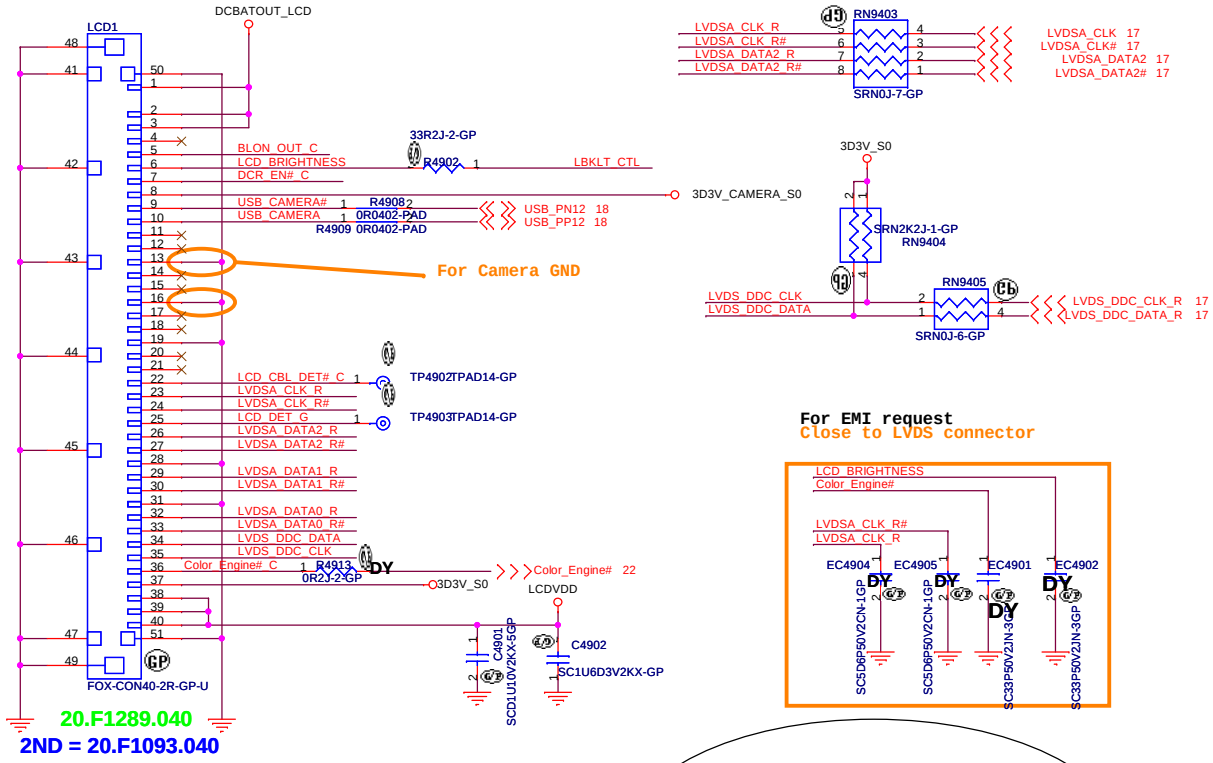
Title: RT8208B_VCCSA

Size | Document Number: LA57 | Rev: SD

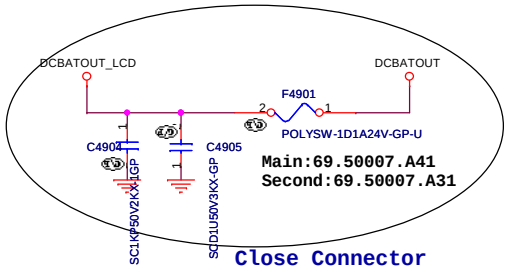
Date: Friday, December 10, 2010 | Sheet 48 of 103

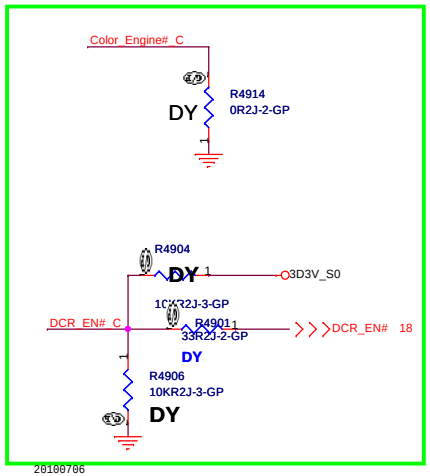
SSID = VIDEO

LVDS CONNECTOR

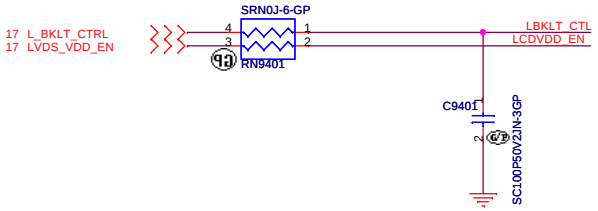


For EMI request
Close to LVDS connector

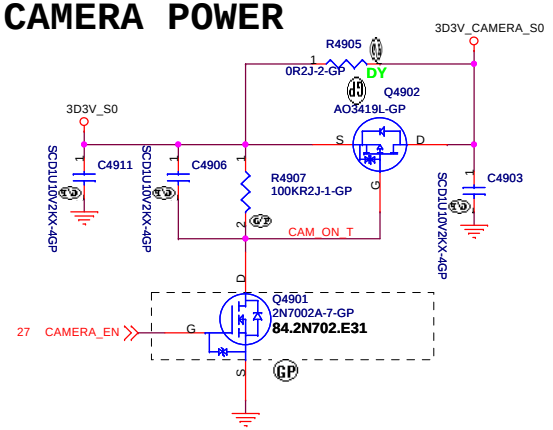




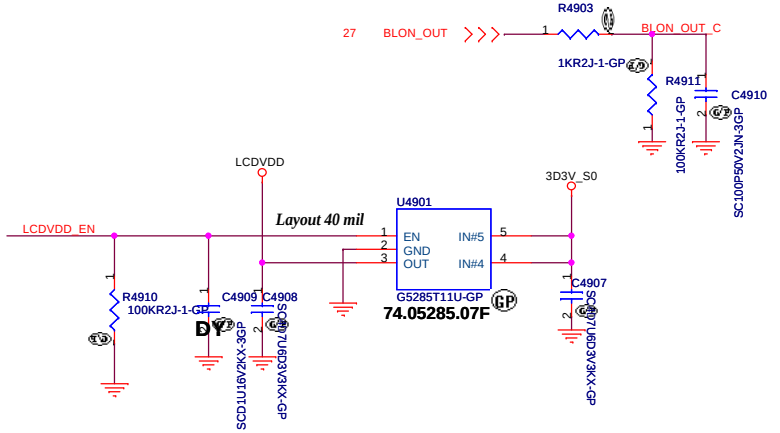
Panel BL brightness/Power En/BL En



CAMERA POWER



SSID = VIDEO



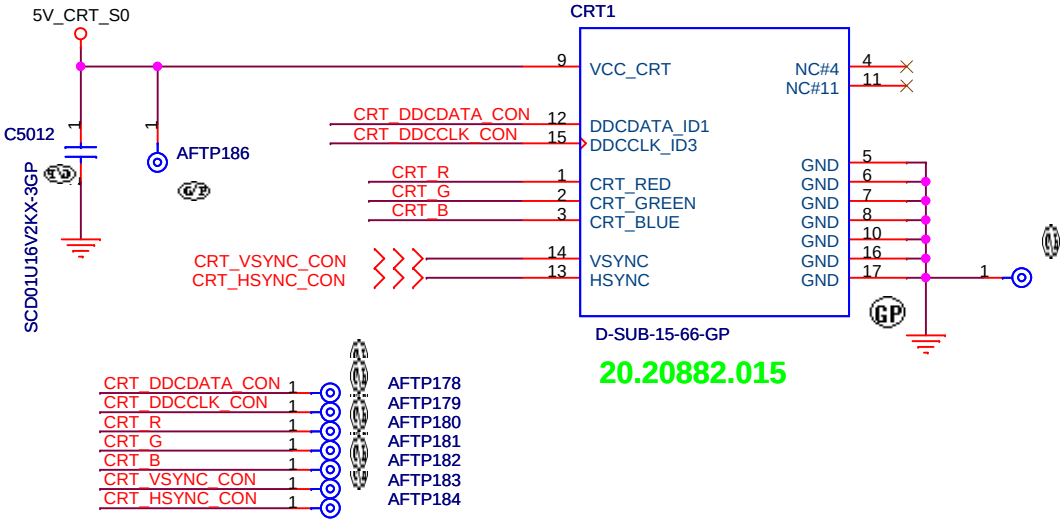
<Core Design>

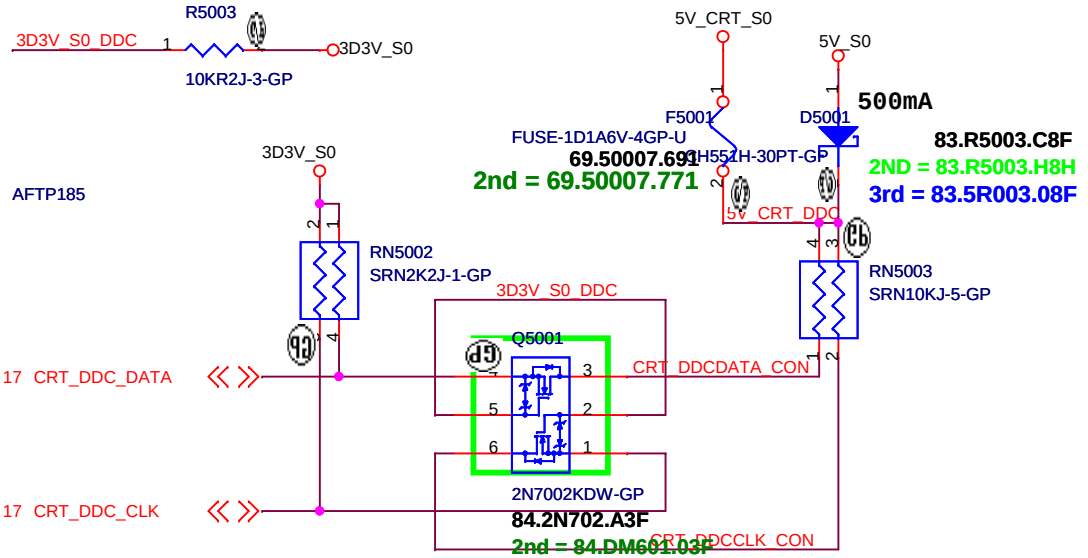
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector
Size: A3
Document Number: Huron River
Rev: SD
Date: Friday, December 10, 2010
Sheet 49 of 103

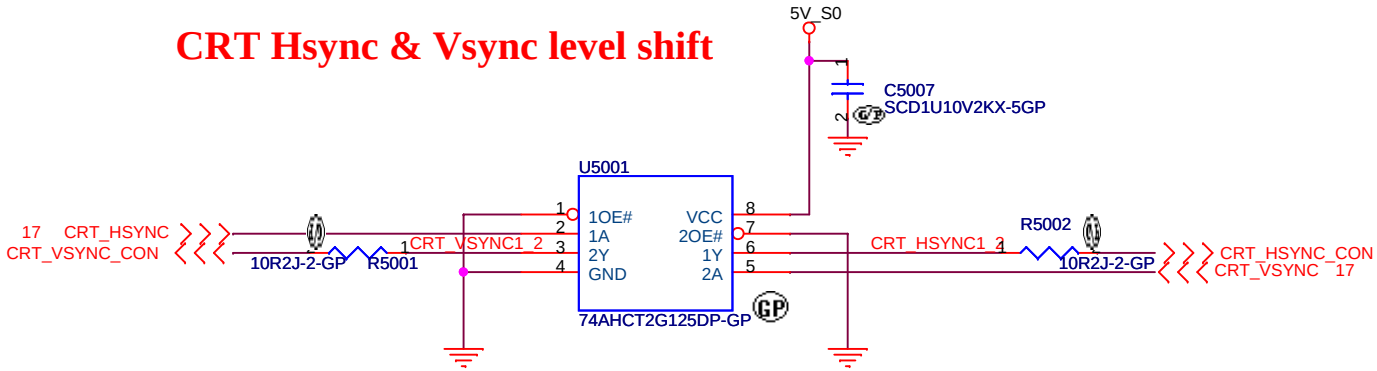
CRT DDCDATA & DDCCLK level shift

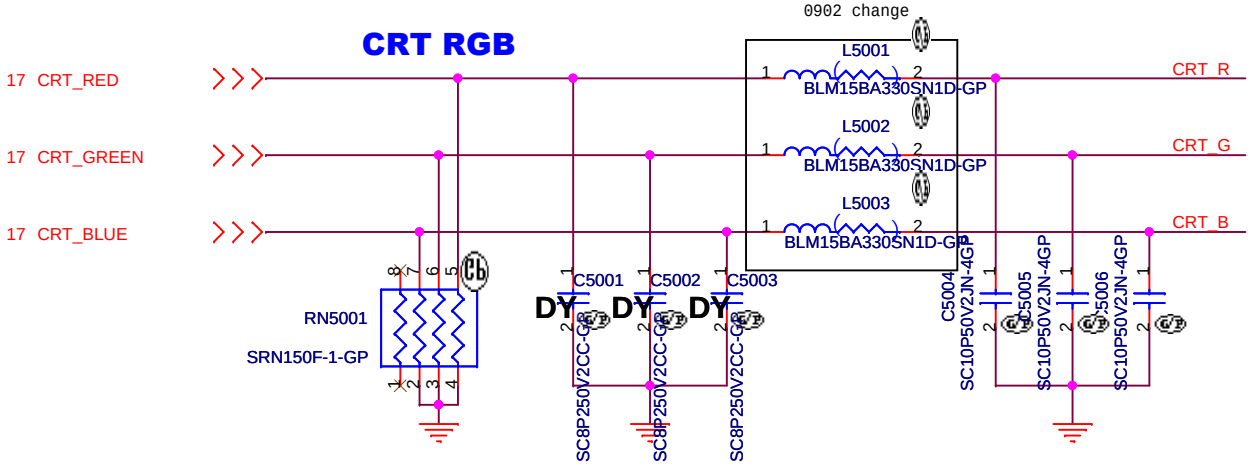
Pull High 5V Design on CRT Board

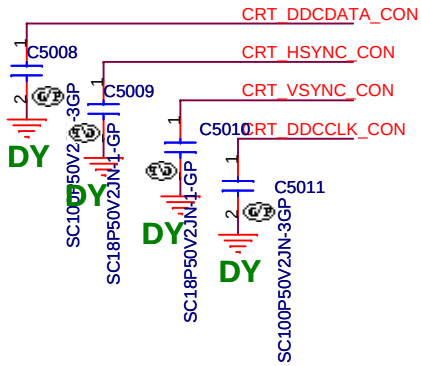




CRT Hsync & Vsync level shift







<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A4	Huron River	SD

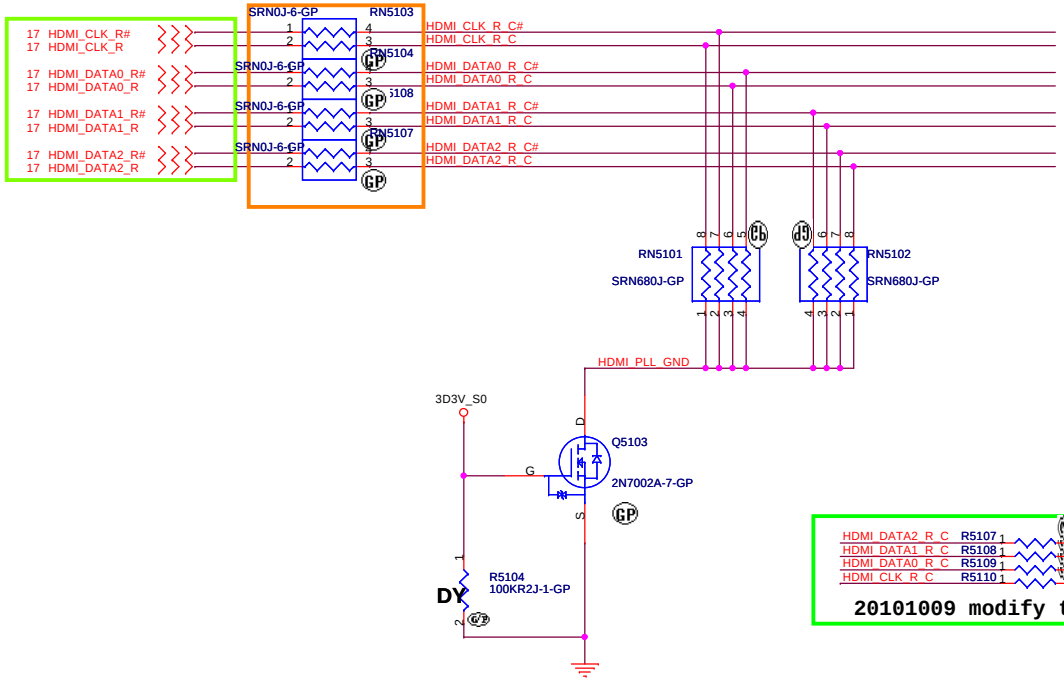
Date: Friday, December 10, 2010 Sheet 50 of 103

SSID = VIDEO

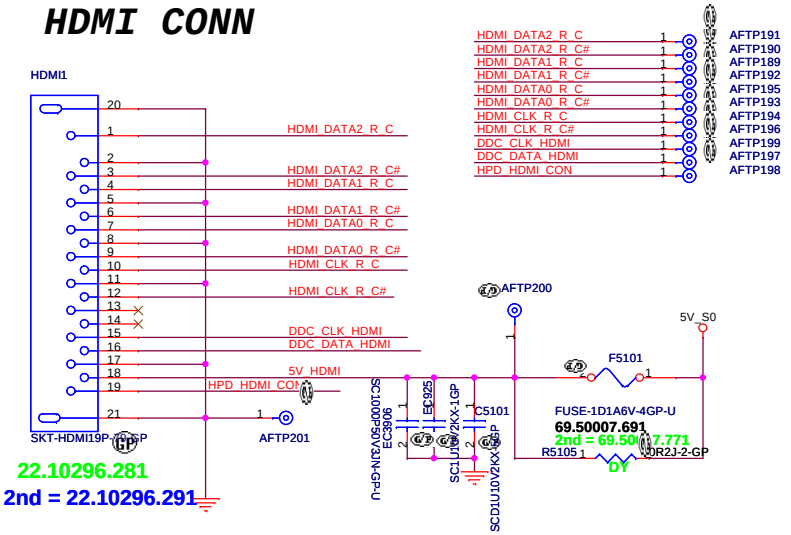
HDMI CONNECTOR

HDMI Passive Level Shifter

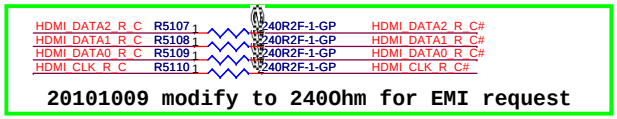
Close to HDMI Connector

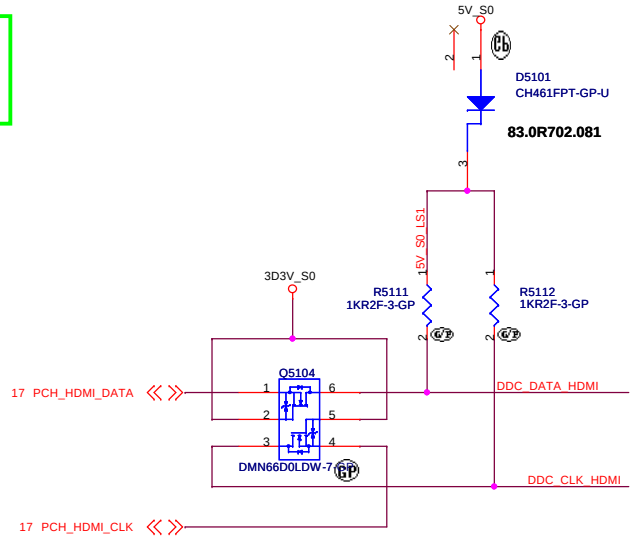


HDMI CONN

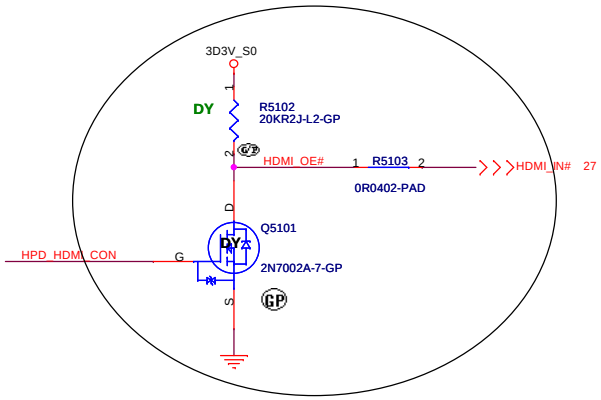


HDMI DDC Passive Level Shifter

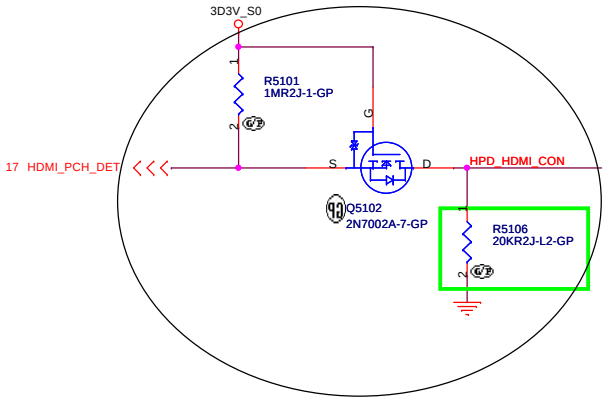




20100727 modify, KBC isn't use.



20100727 follow intel design guide



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Huron River	SD

Date: Friday, December 10, 2010 Sheet 51 of 103

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(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 53 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

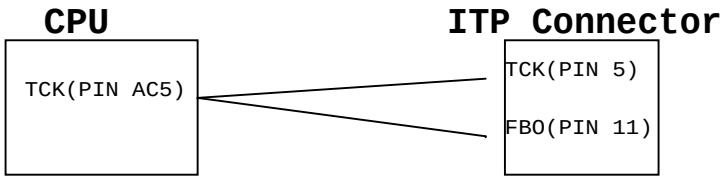
Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.

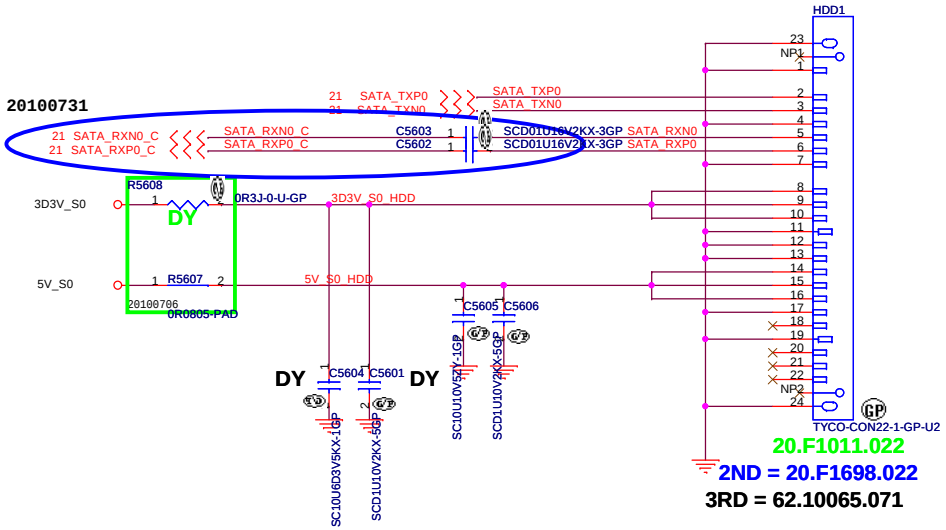


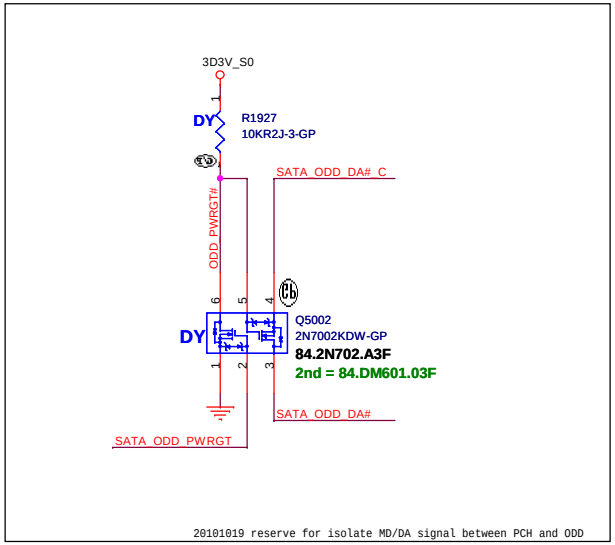
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ITP		
Size: A4	Document Number: LA57	Rev: SD
Date: Friday, December 10, 2010	Sheet 55 of 103	

SSID = SATA

SATA HDD Connector

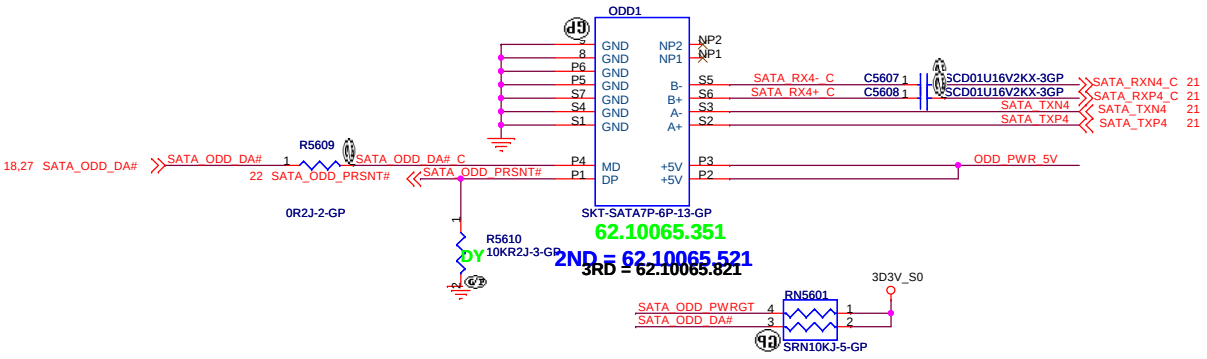




ODD Connector

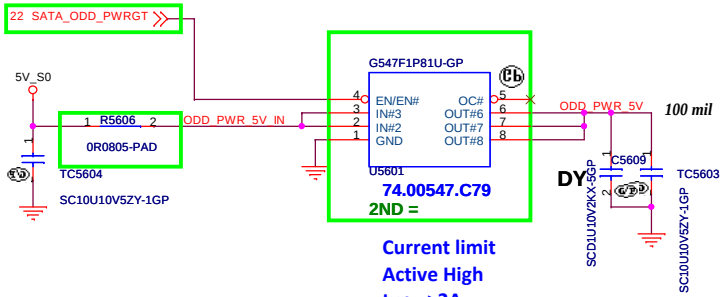
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SUPPORT ZERO SATA ODD

SATA Zero Power ODD



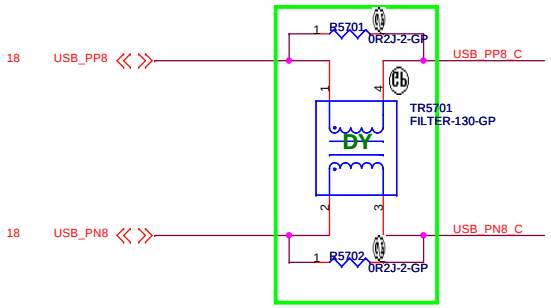
<Core Design>

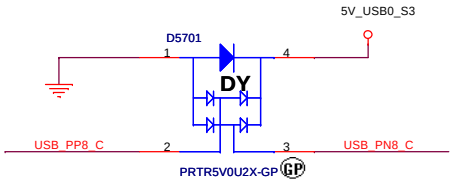
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

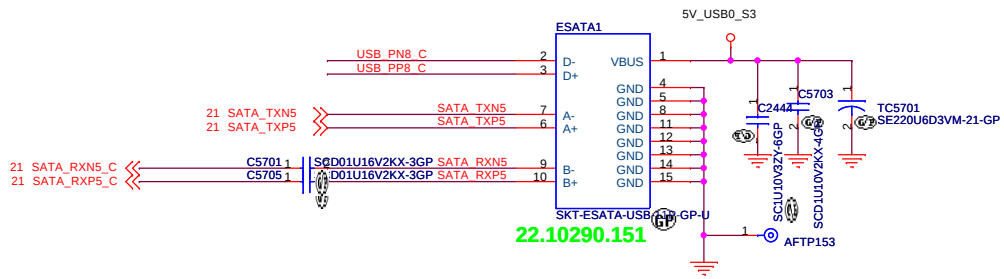
Title: HDD/ODD

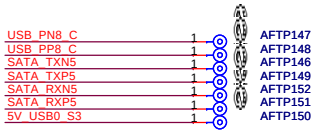
Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 56 of 103









<Core Design>

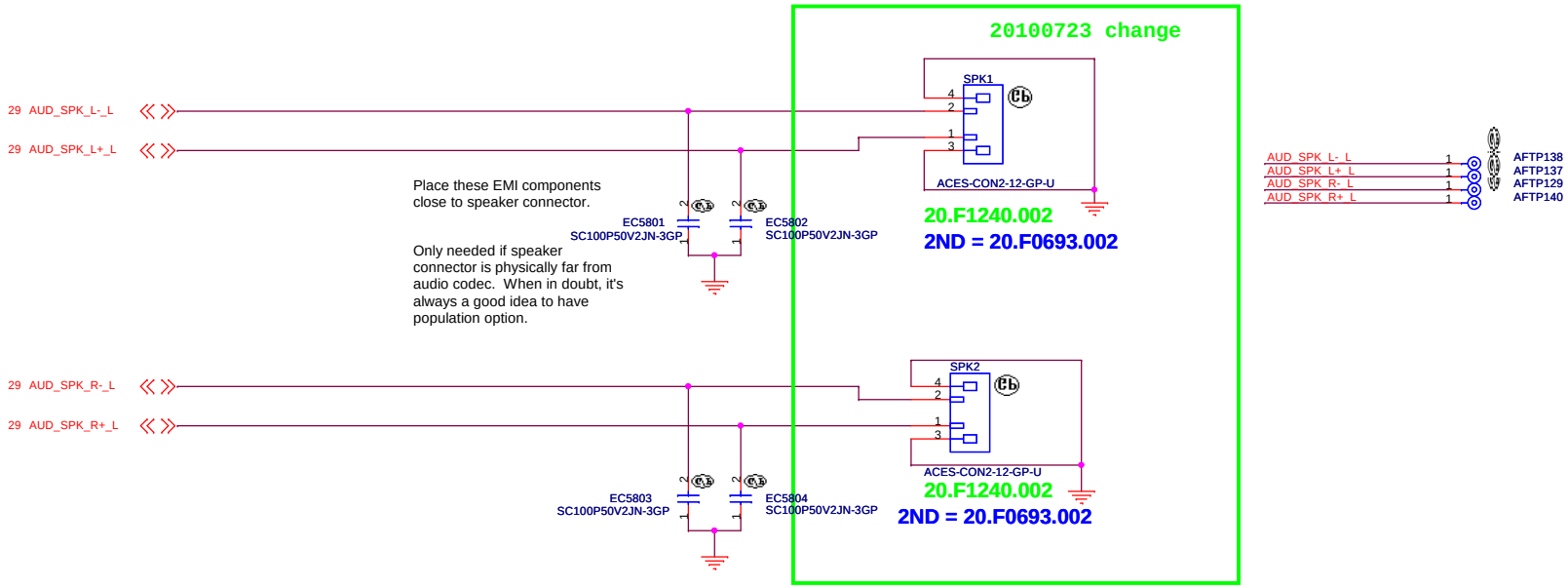
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA/LUSB

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 57 of 103

INTERNAL STEREO SPEAKERS



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 58 of 103

Reserved

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

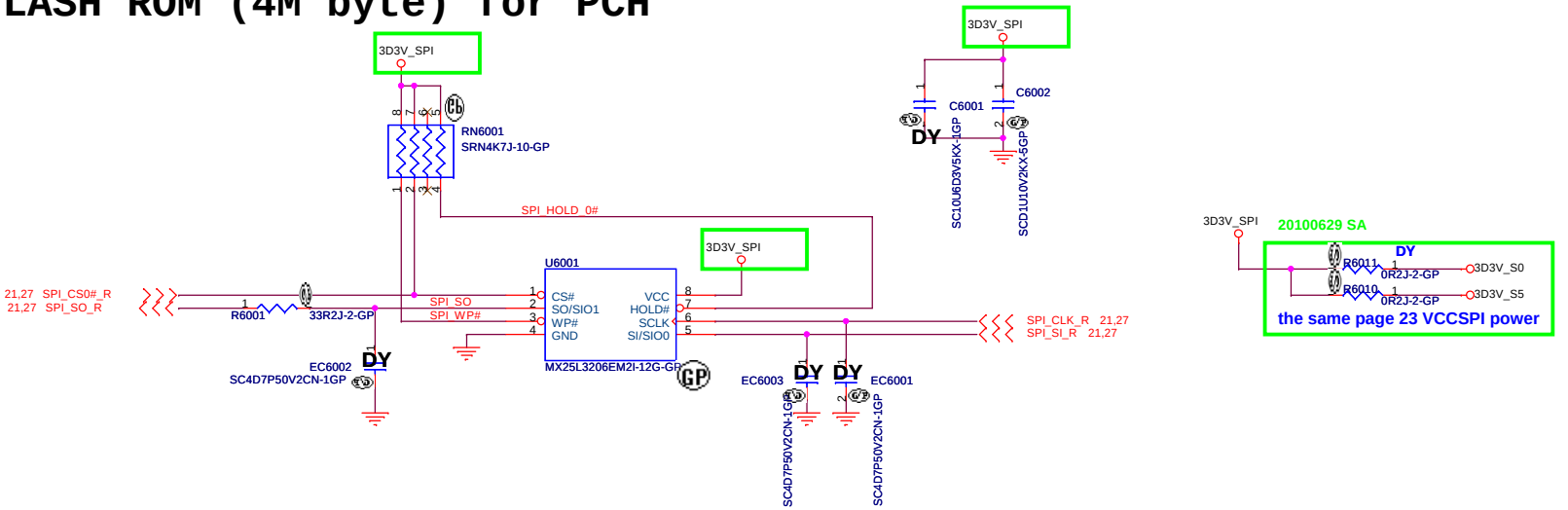
Title: ***Reserved***

Size	Document Number	Rev
A3	LA57	SD

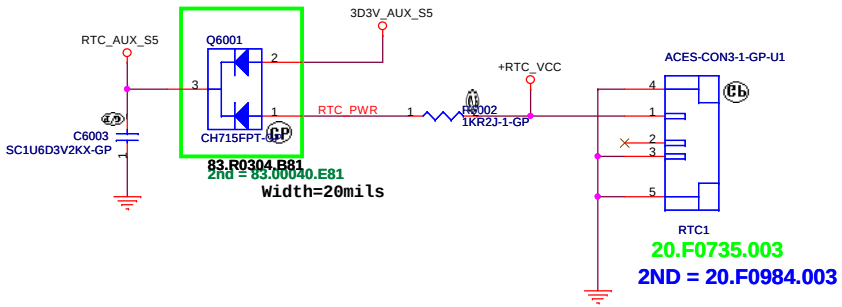
Date: Friday, December 10, 2010 Sheet 59 of 103

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

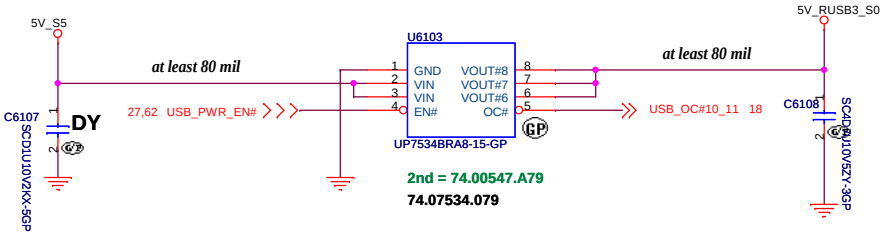
Title: Flash/RTC

Size	Document Number	Rev
A3	LA57	SD

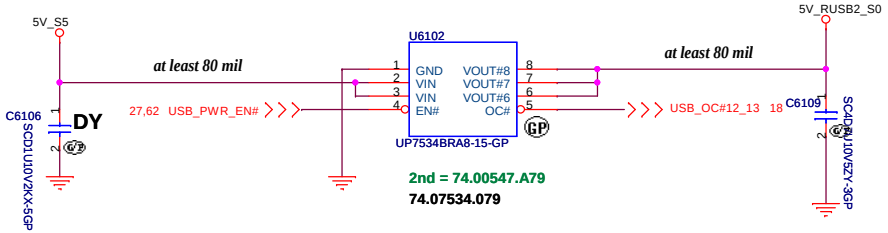
Date: Friday, December 10, 2010 Sheet 60 of 103

SSID = USB

RJ45_USB Board USB Power



I/O Board USB Power

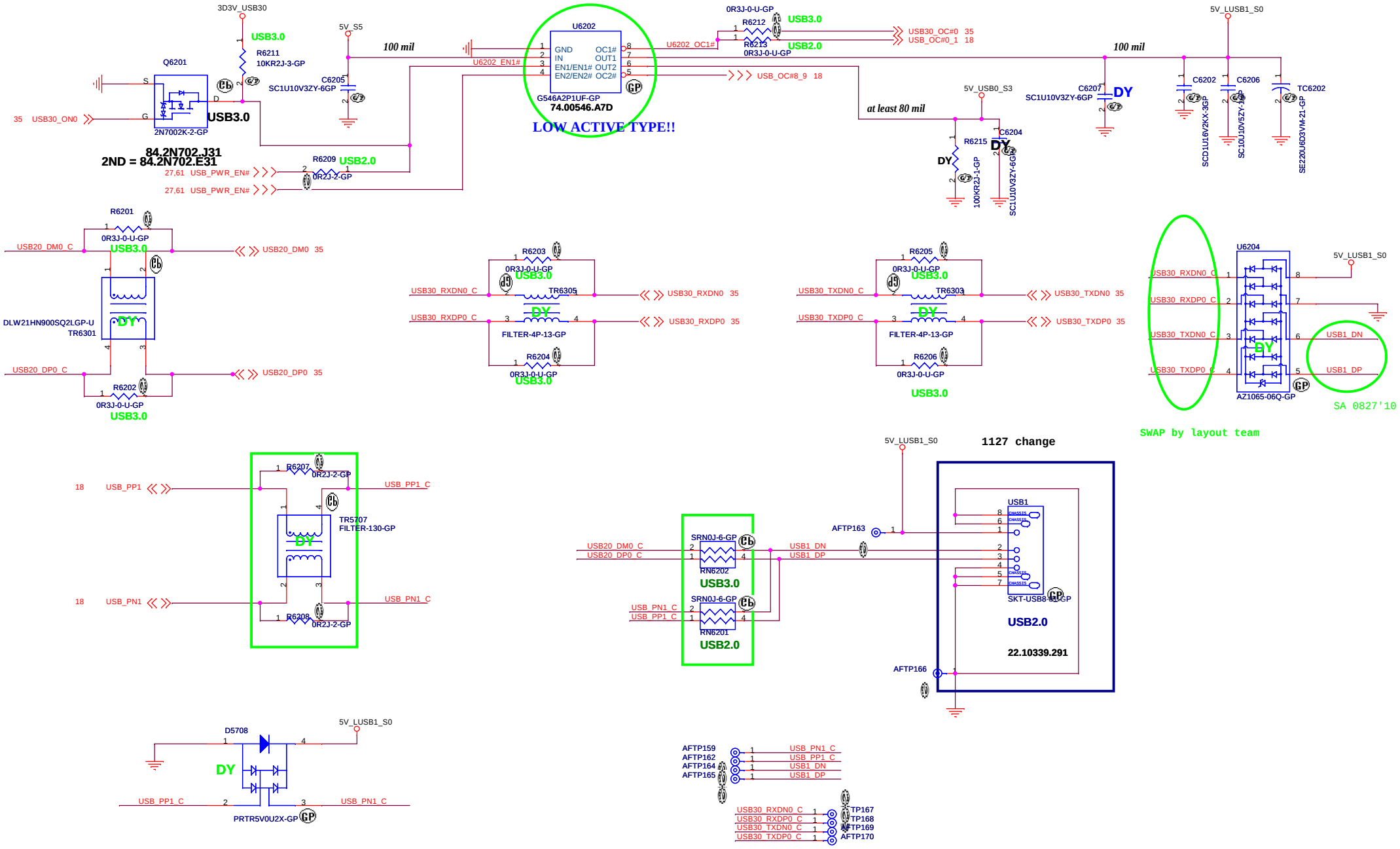


LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB Power SW***	
Size A3	Document Number **LA57**	Rev **SD**
Date: Friday, December 10, 2010	Sheet 61 of 103	

Left Side USB Power Switch

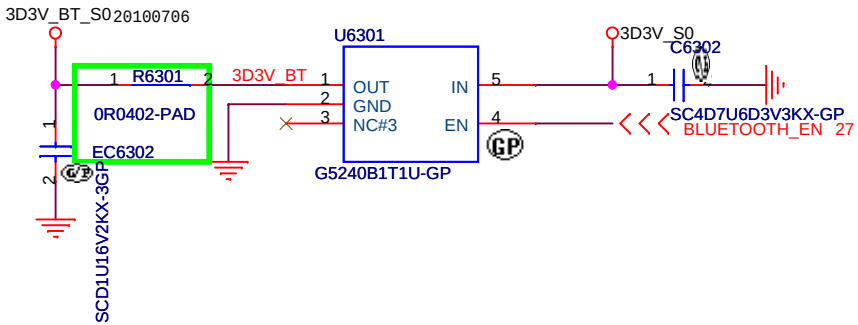


Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: USB 2.0/3.0 Port			
Size: A3	Document Number: LZ57	Rev: SD	
Date: Friday, December 10, 2010	Sheet 62 of 103		

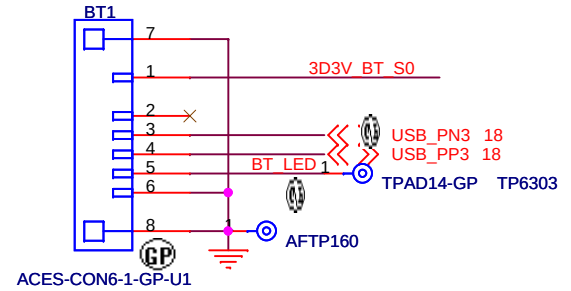
SSID = User.Interface

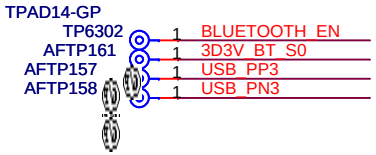
Bluetooth Module conn.

Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request





20.F0772.006

2ND = 20.F1804.006

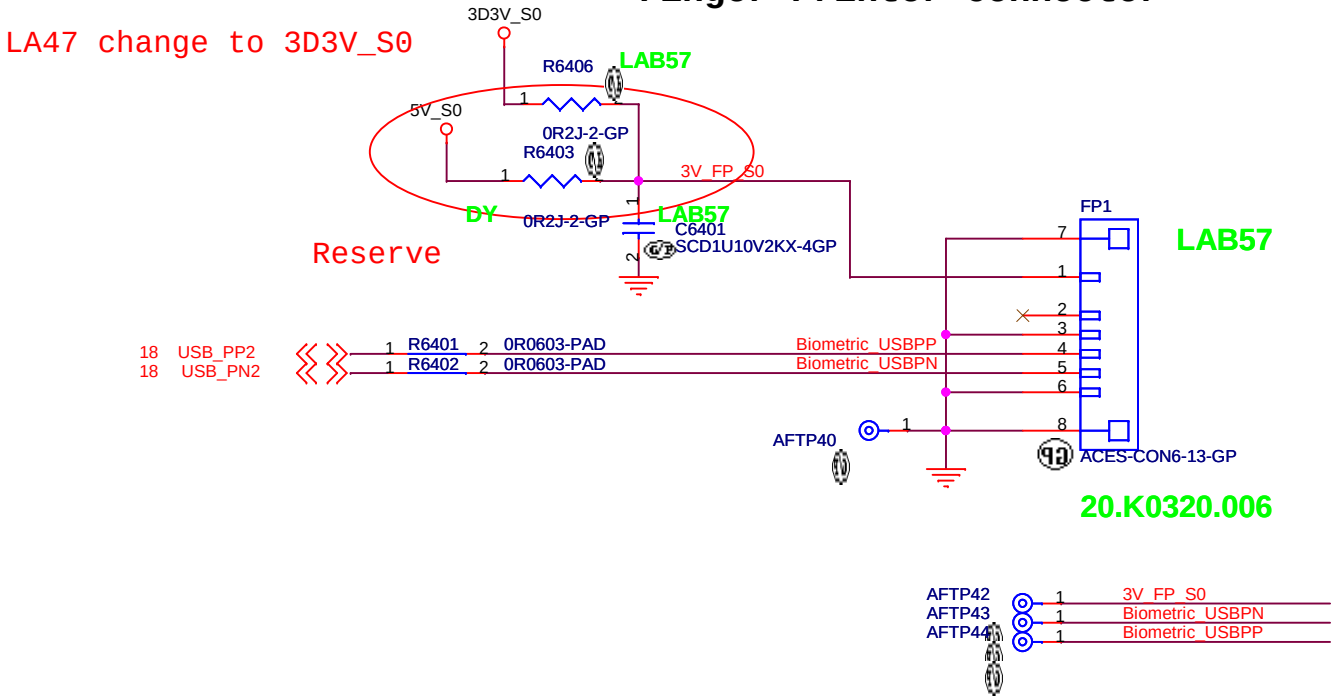
LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***		
Size: A4	Document Number: **LA57**	Rev: **SD**
Date: Friday, December 10, 2010	Sheet 63 of 103	

Finger Printer Connector

LA47 change to 3D3V_S0



LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

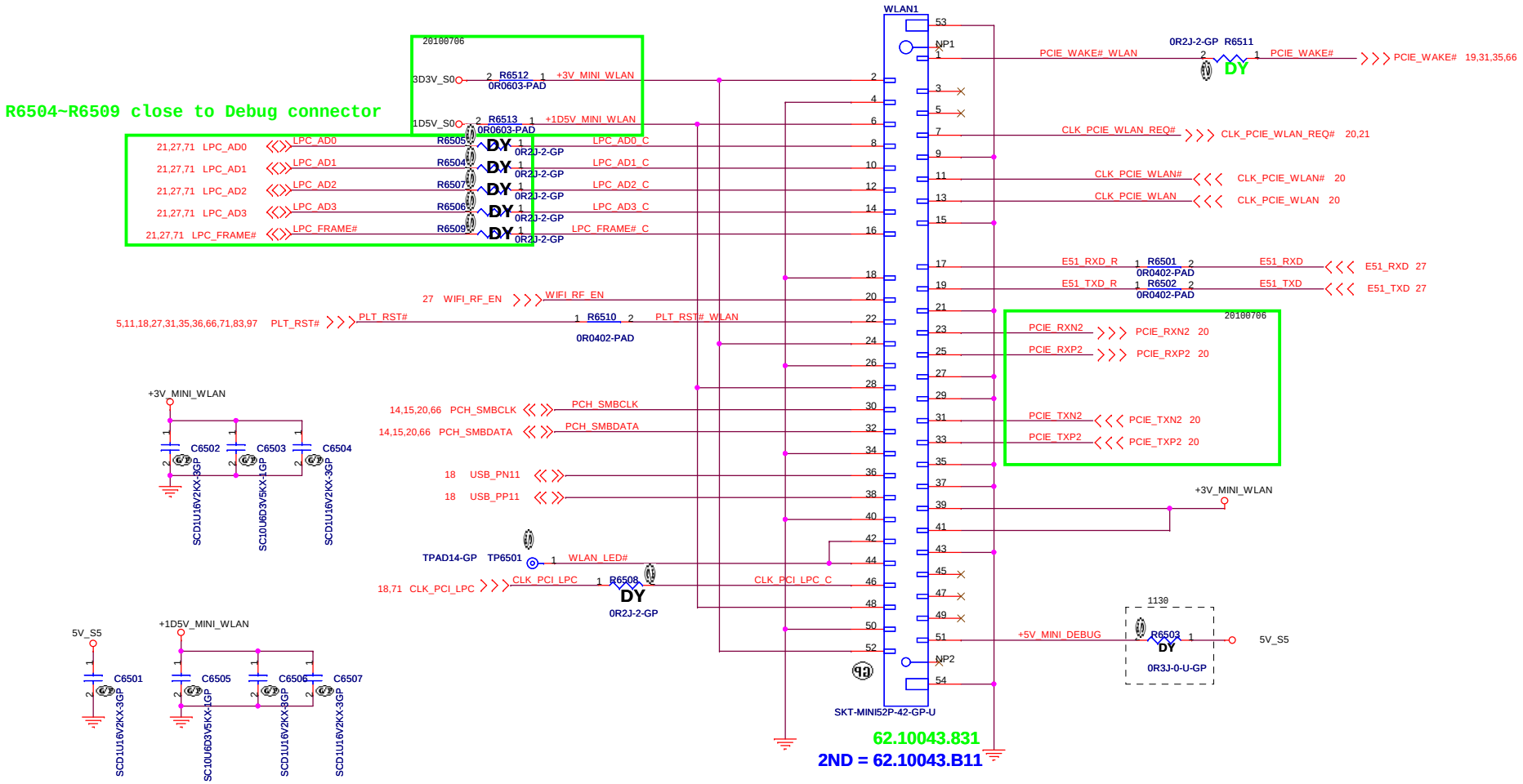
Title: ***RESERVED***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

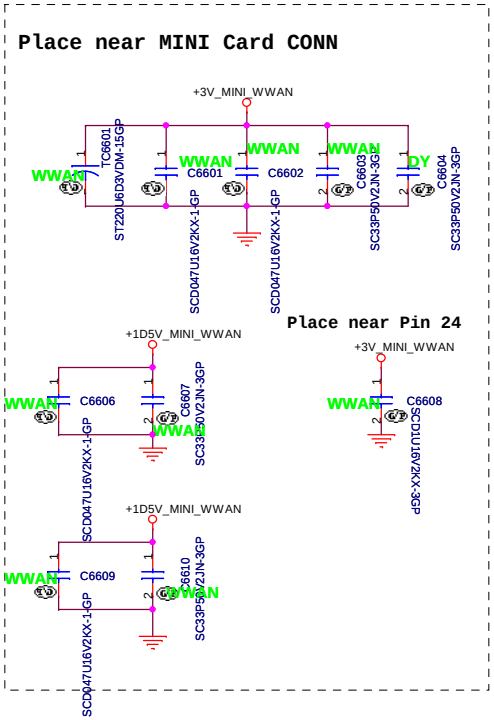


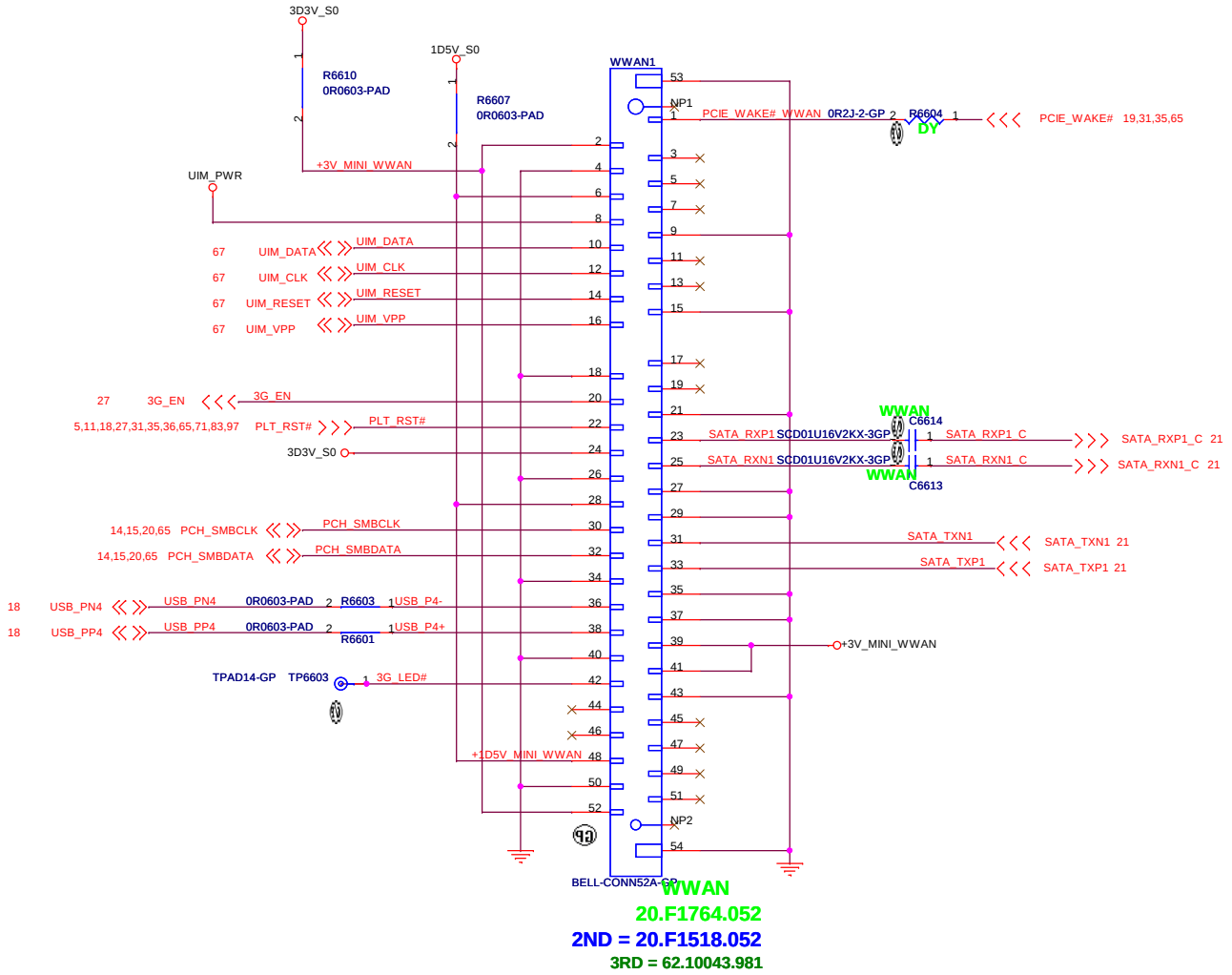
LA57 UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)/ITP CONN		
Size: A3	Document Number: LA57	Rev: SD
Date: Friday, December 10, 2010	Sheet 65 of 103	

SSID = Wireless

Mini Card Connector(WWAN)





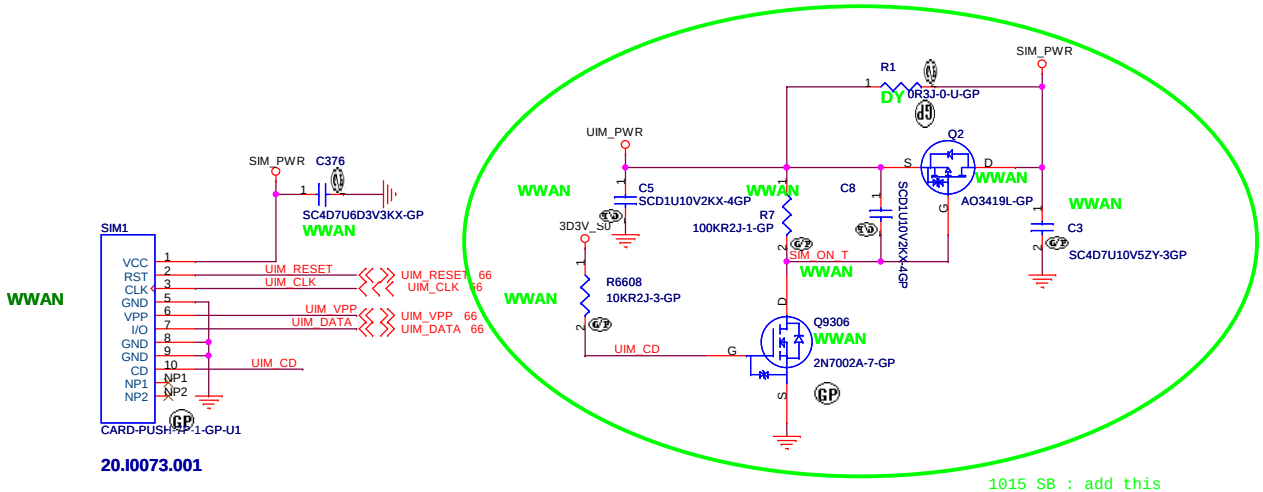
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WWAN Connector***

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 66 of 103



20.I0073.001

1015 SB : add this

<Core Design>

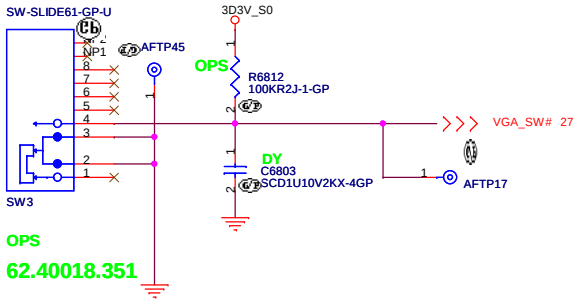
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIM_CARD

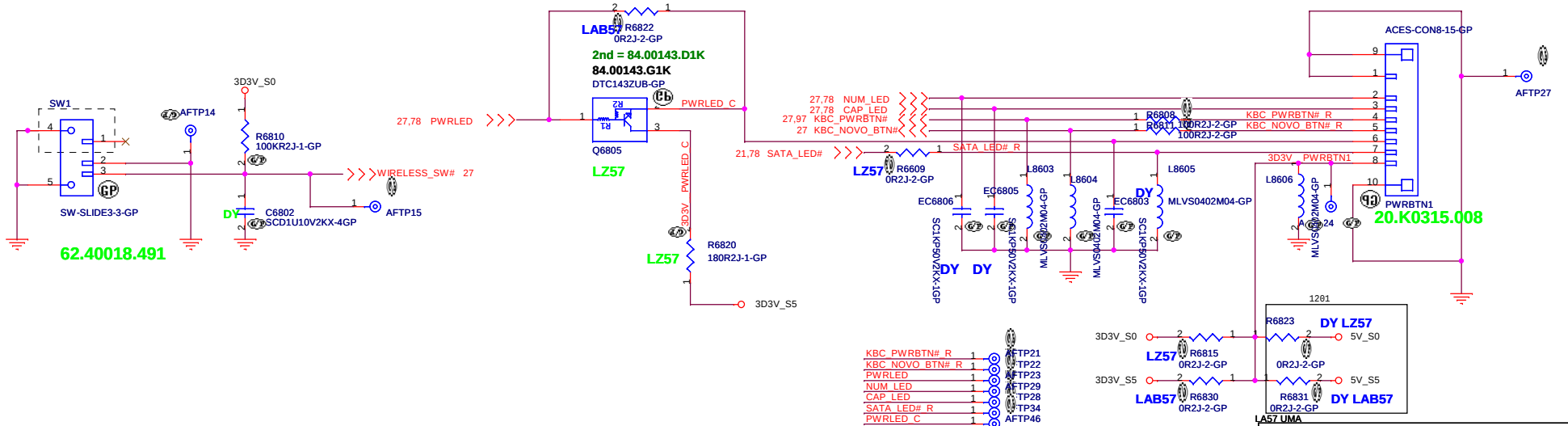
Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 67 of 103

SSID = User.Interface



Power button LED(White)



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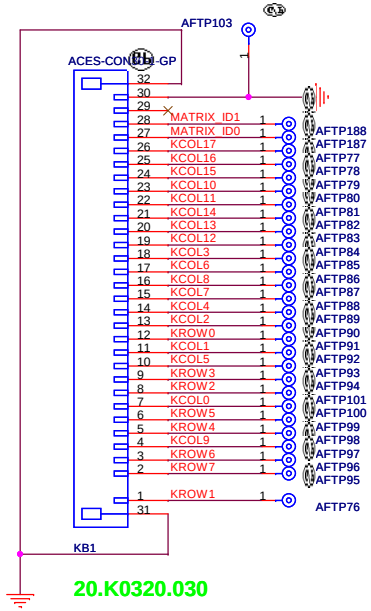
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED Bard/Power Button	
Size A3	Document Number LA57	Rev SD
Date: Friday, December 10, 2010	Sheet 68 of 103	

SSID = KBC

Internal KeyBoard Connector

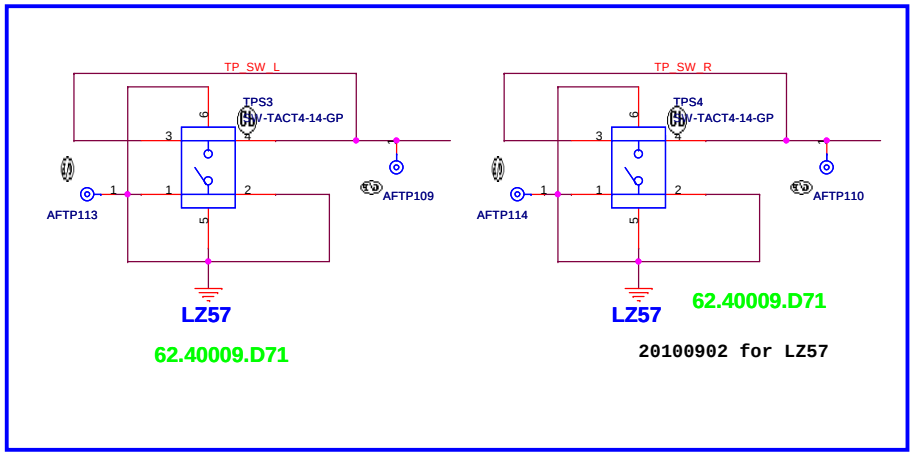


20.K0320.030

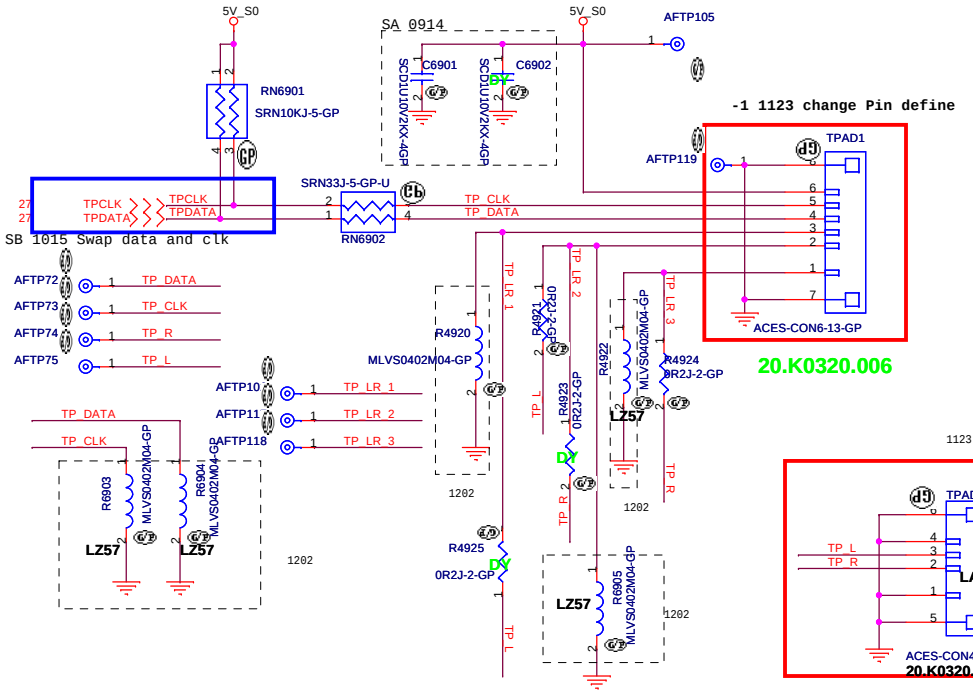
ID KEY MATRIX	SENSE			
	27	28	29	30
	ID0	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

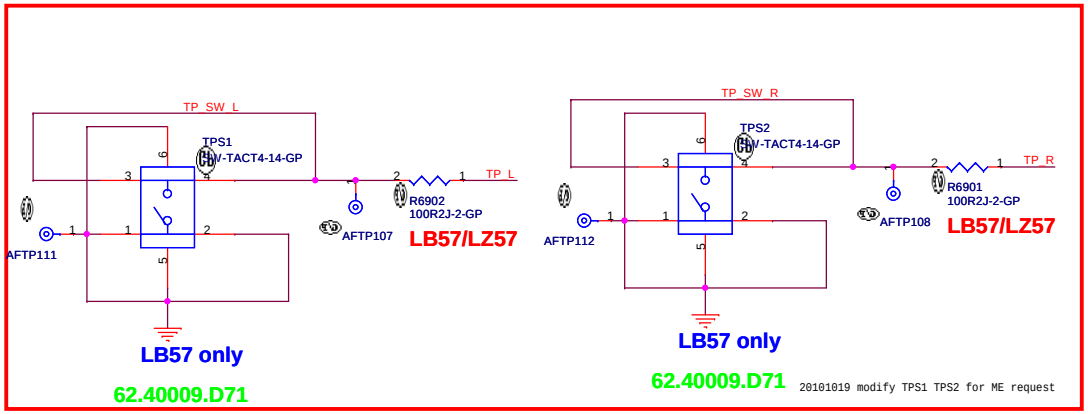
KROW[0..7] 27

KCOL[0..17] 27



SSID = Touch.Pad

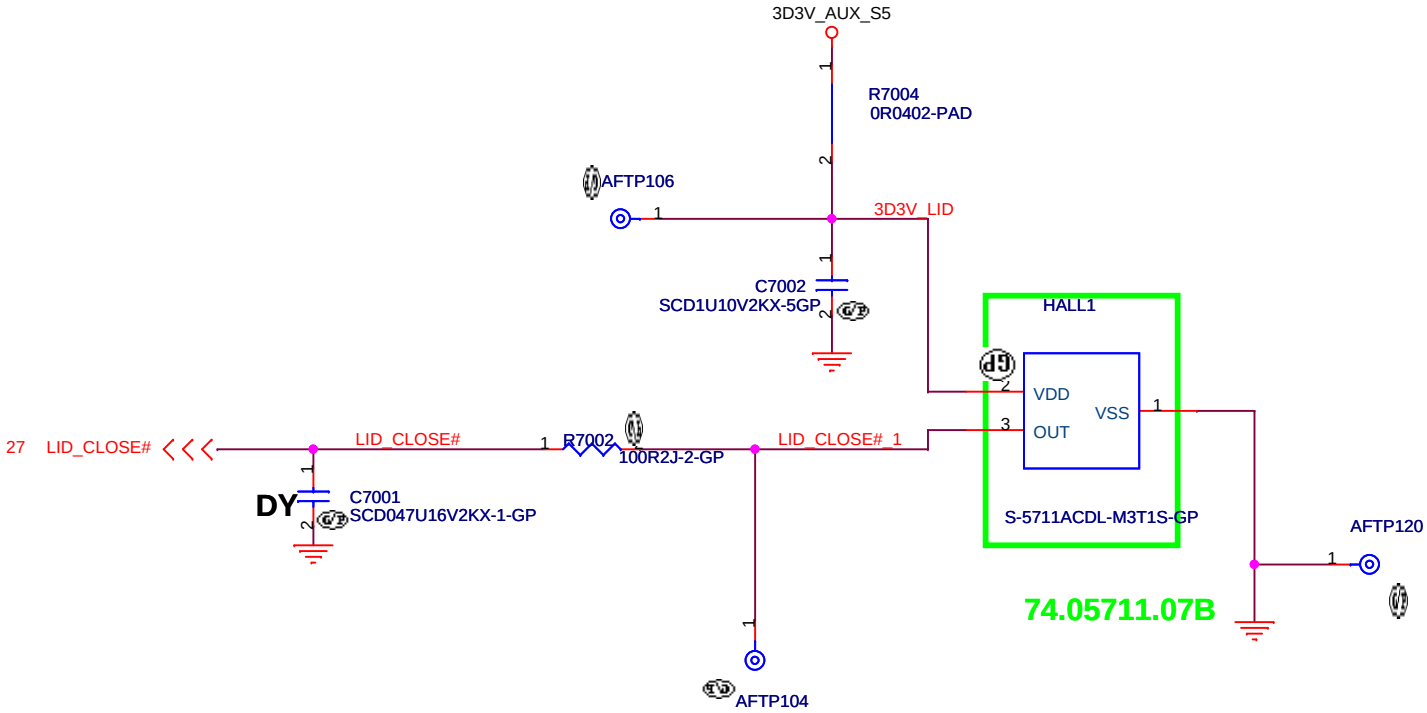




<Core Design>

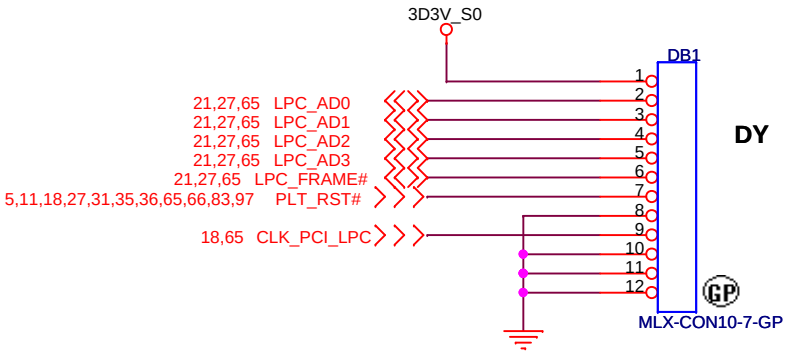
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
Size A3	Document Number LA57	Rev SD
Date: Friday, December 10, 2010	Sheet 69 of 103	



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Hall Sensor***	
Size A4	Document Number **LA57**	Rev **SD**
Date: Friday, December 10, 2010	Sheet 70 of 103	



LA57 UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 71 of 103

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LA57 UMA

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 72 of 103

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LA57 UMA

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Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 73 of 103

LA57 UMA

緯創資通

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Title

CARD Reader CONN

Size	Document Number	Rev
A4	**LA57**	**SD**

Date: Friday, December 10, 2010 Sheet 74 of 103

LA57 UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

New Card

Size	Document Number	Rev
A4	**LA57**	**SD**

Date: Friday, December 10, 2010 Sheet 75 of 103

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LA57 UMA

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **LA57**	Rev: **SD**
Date: Friday, December 10, 2010	Sheet 76 of 103	

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LA57 UMA

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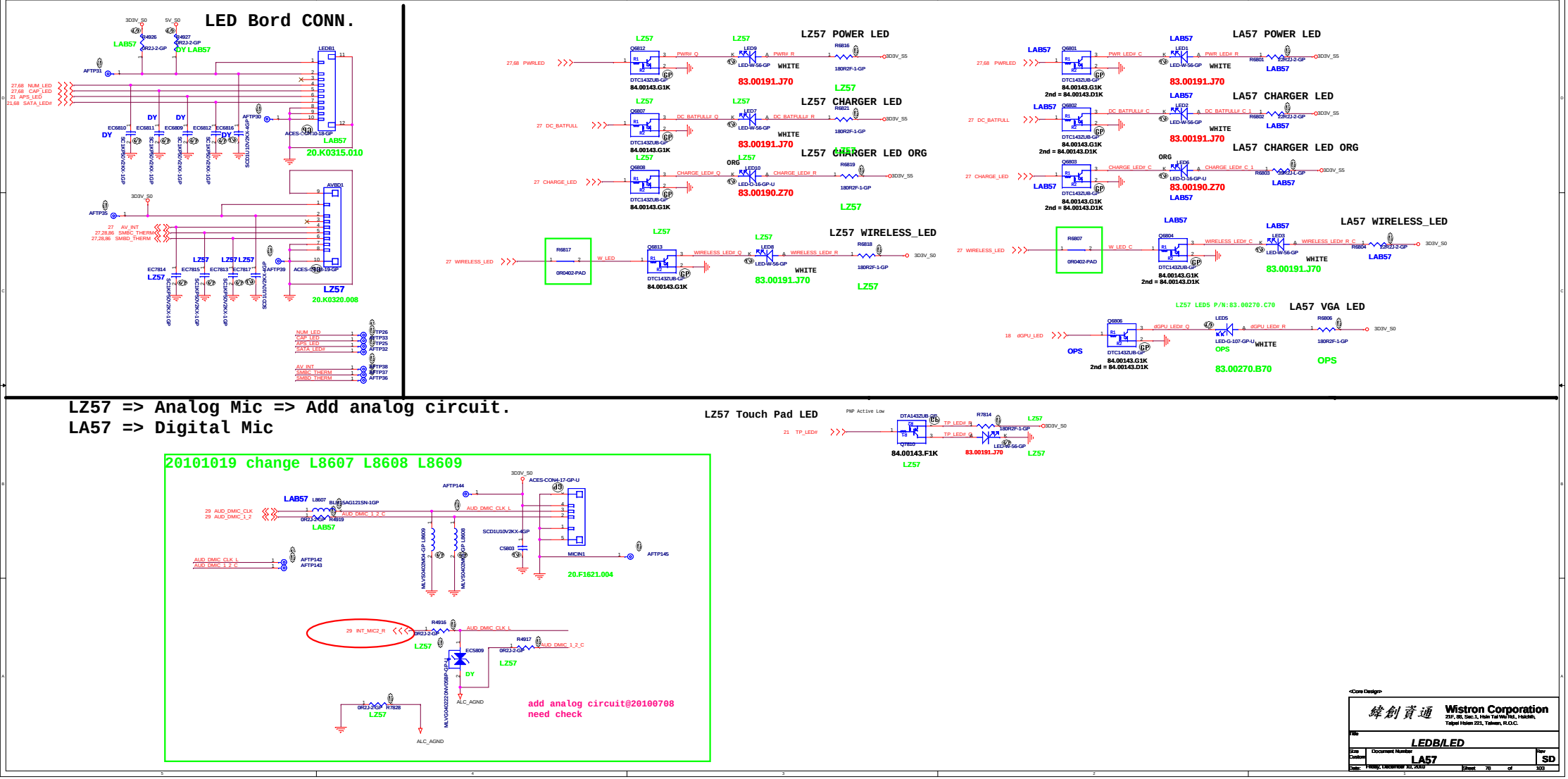
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 77 of 103



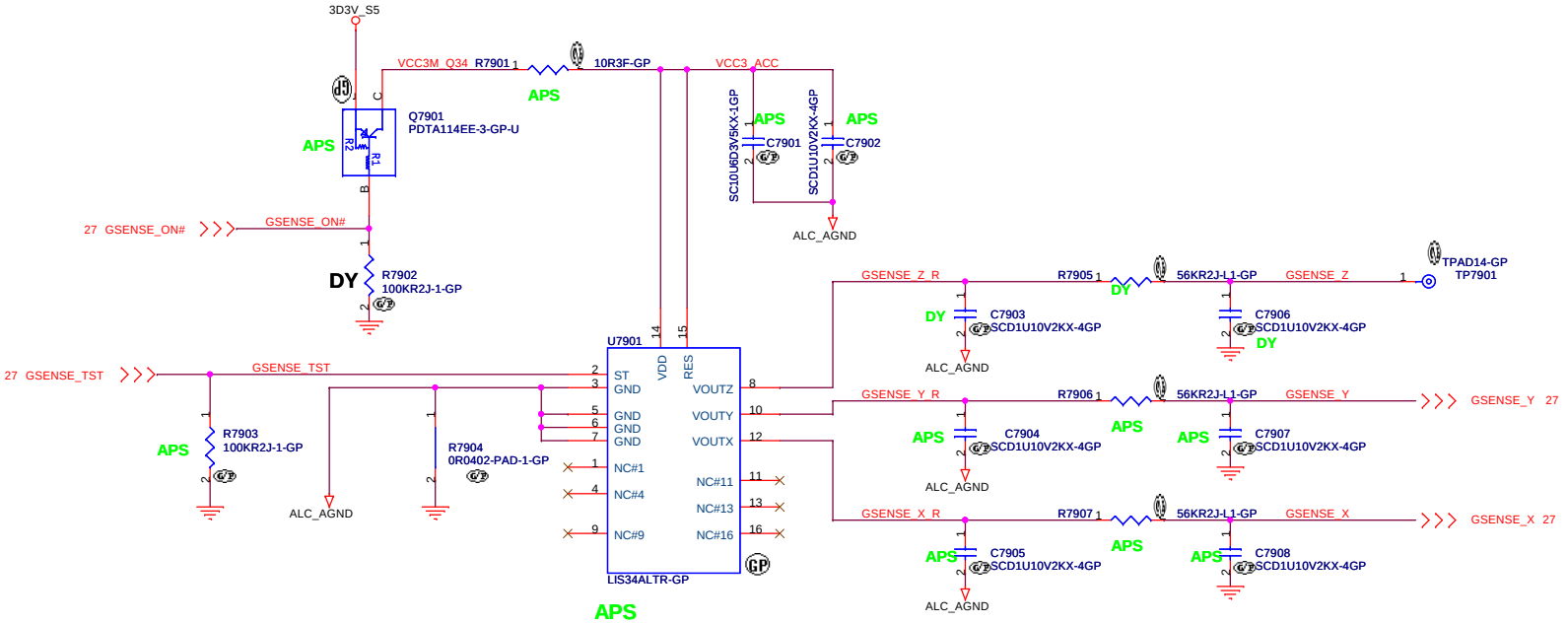
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LEDB/LED

Size	Document Number	Rev
Custom	LA57	SD

Date: Friday, December 10, 2010 Sheet 78 of 103

G-Sensor



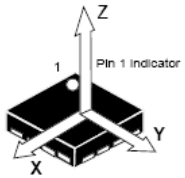
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



<Core Design>

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Title: *G-Sensor*		
Size: Custom	Document Number: LA57	Rev: SD
Date: Friday, December 10, 2010	Sheet 79 of 103	

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LA57 UMA

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Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 80 of 103

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LA57 UMA

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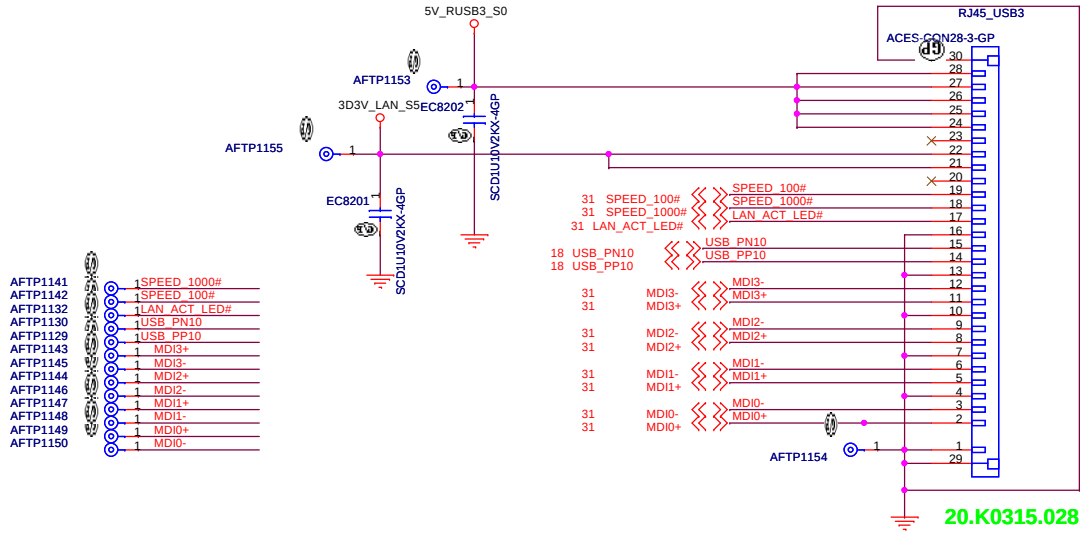
Title: ***Reserved***

Size	Document Number	Rev
A4	LA57	SD

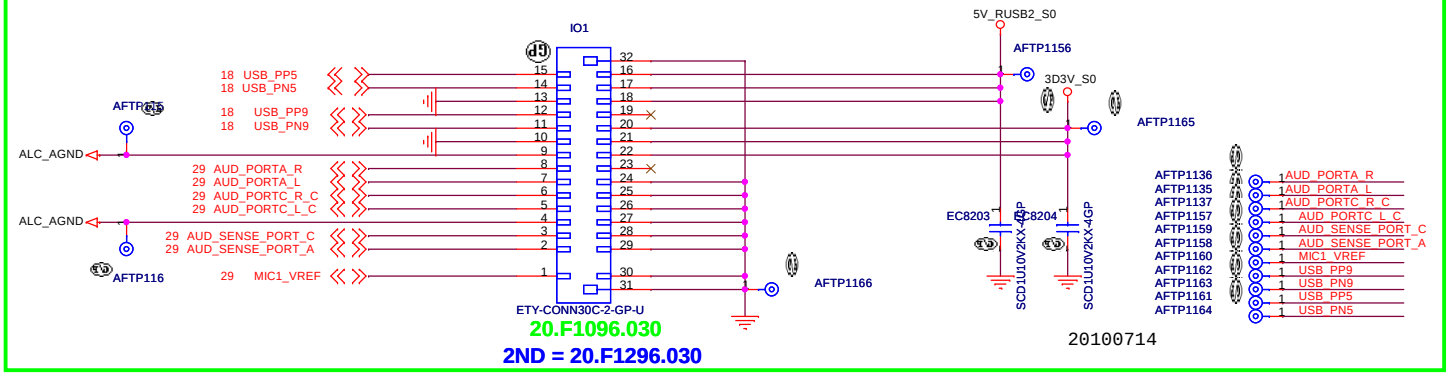
Date: Friday, December 10, 2010 Sheet 81 of 103

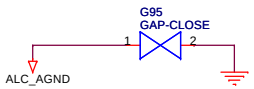
20100728 swap net

RJ45_USB CONN.



Card Reader Board CONN.





LA57 UMA

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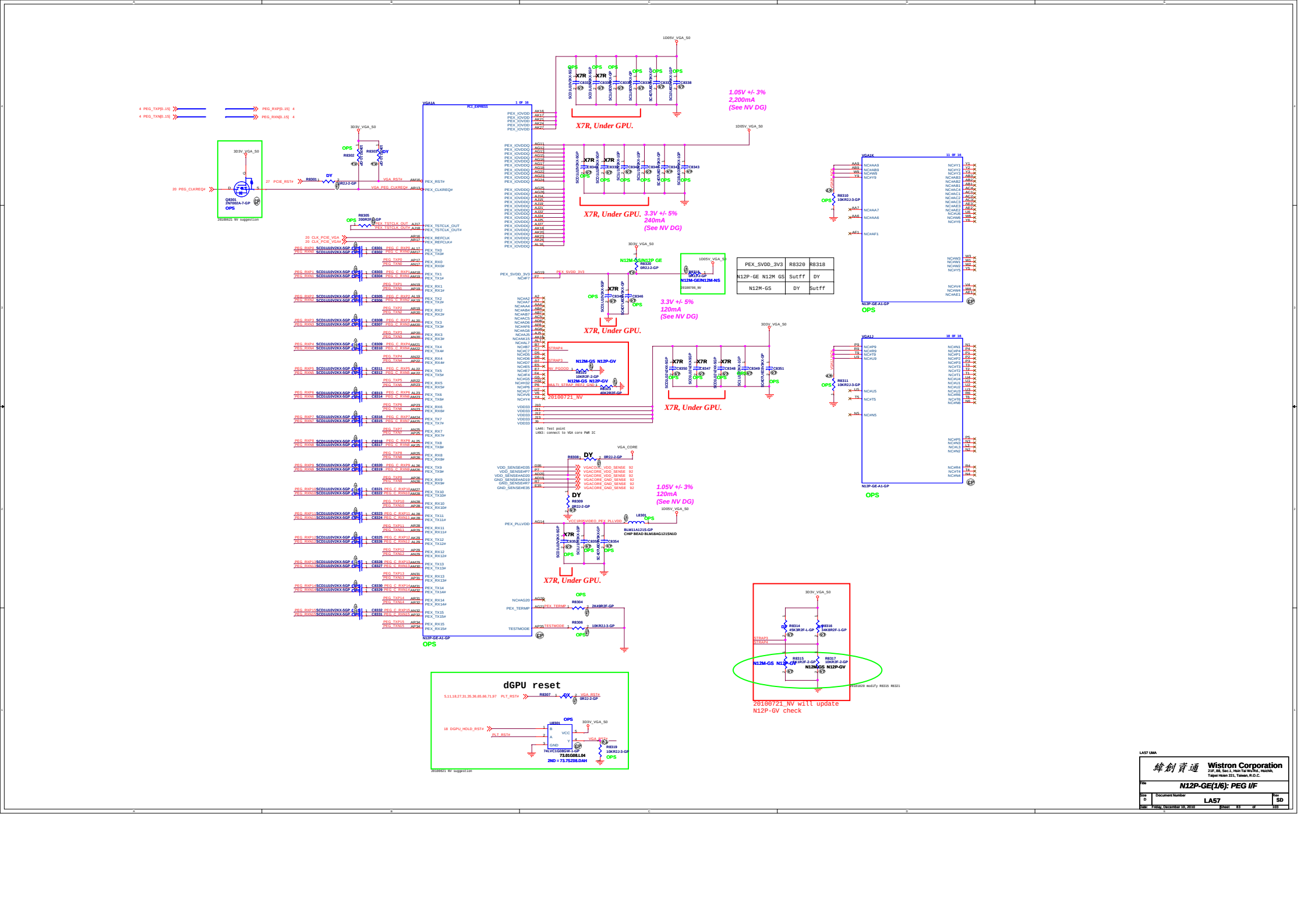
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 82 of 103



PEX_SVDD_3V3	R8320	R8318
N12P-GE N12M GS	Sutff	DY
N12M-GS	DY	Sutff

LA57 LMA

Wistron Corporation
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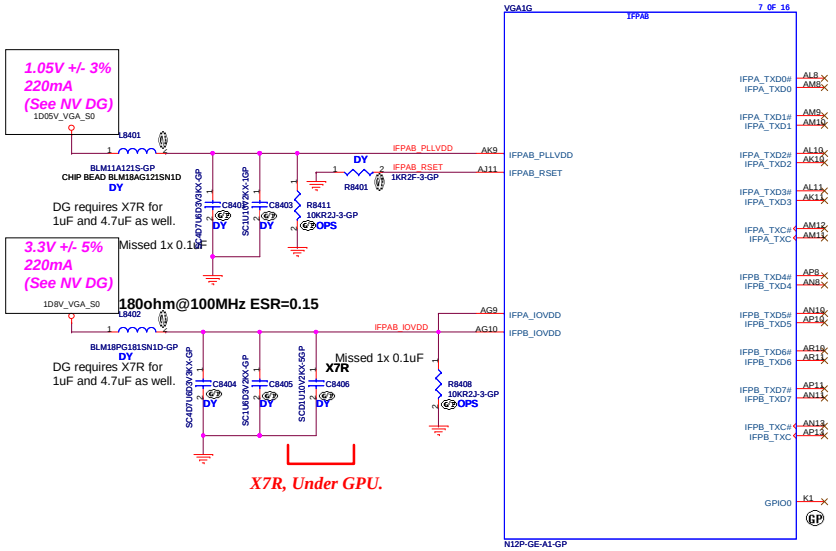
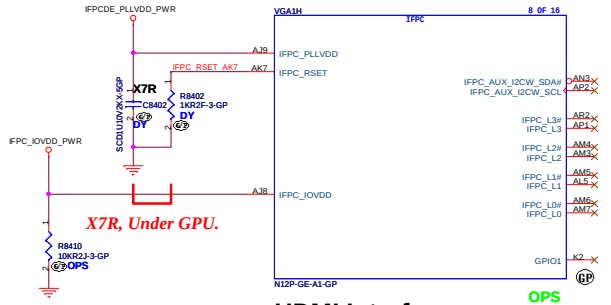
Title: N12P-GE(1/6): PEG I/F

Size	Document Number	Rev
D	LA57	SD

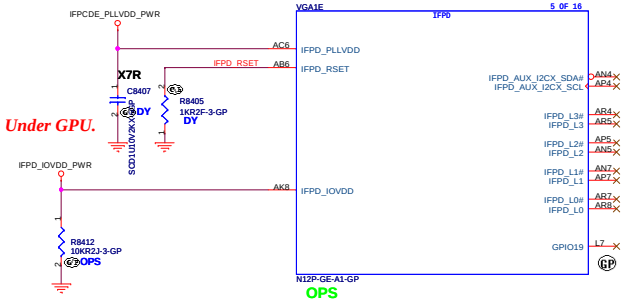
Date: Friday, December 10, 2010 Sheet 83 of 103

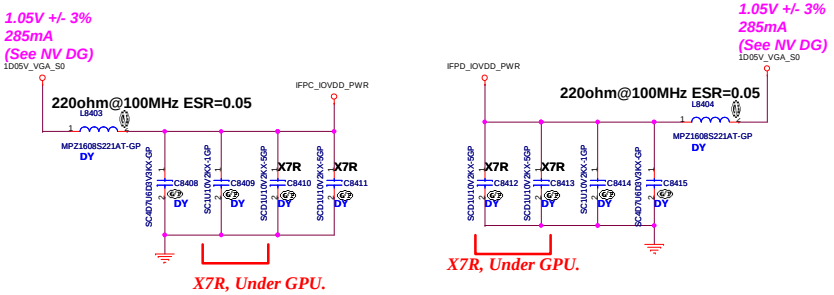
LVDS Interface

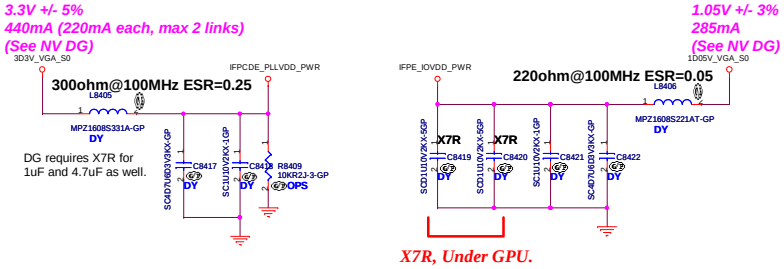


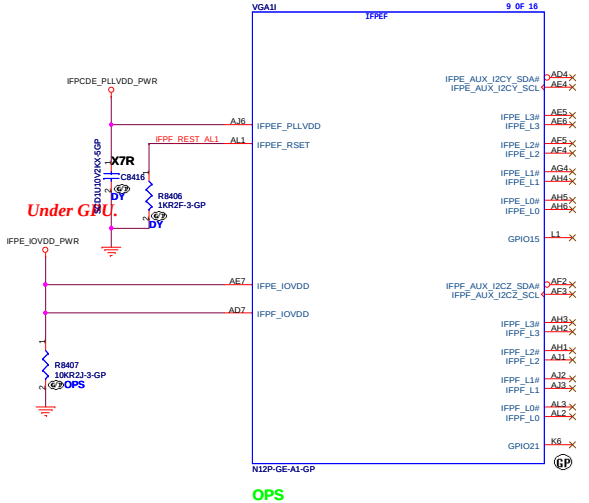


HDMI Interface









LA57 UMA

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P-Q1/Q3 (2/6): DIGITAL OUT

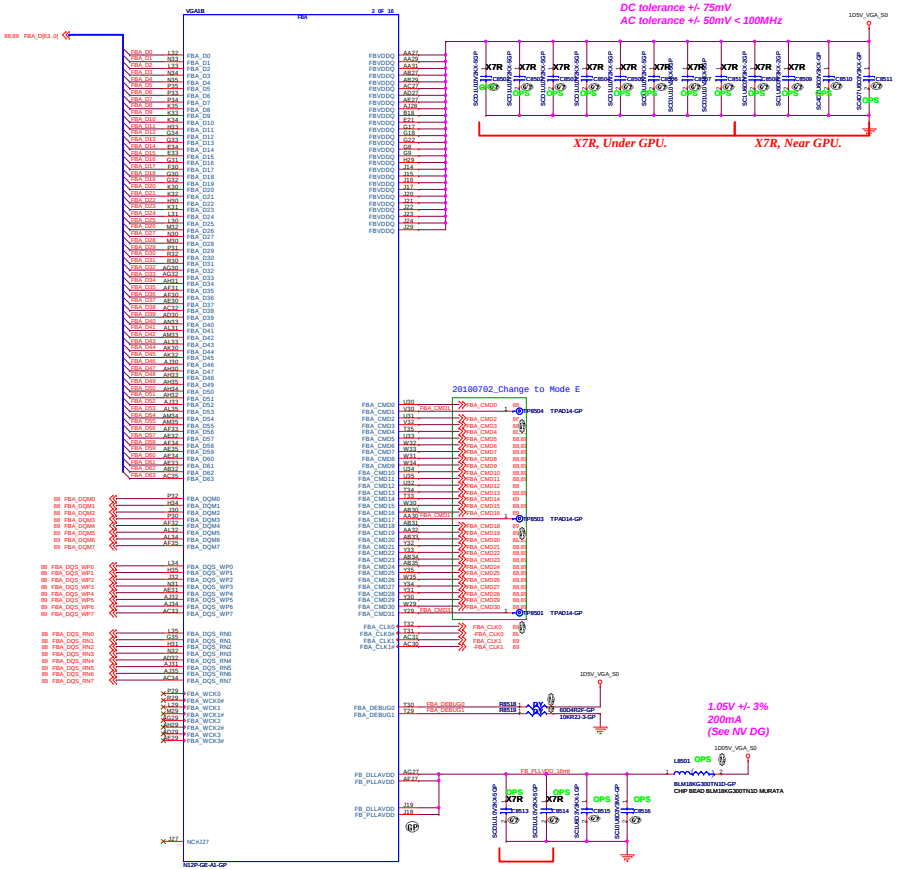
Size	Document Number	Rev
A2	LA57	SD

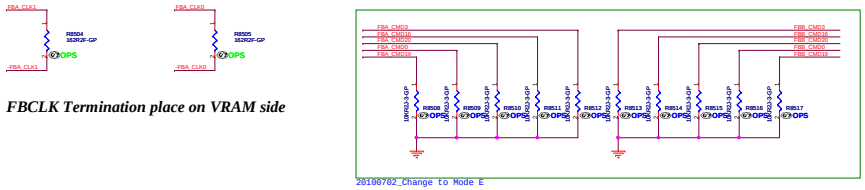
Date: Friday, December 10, 2010 Sheet 84 of 103

EDP 10A

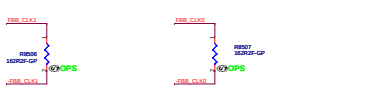
DC tolerance +/- 75mV

AC tolerance +/- 50mV < 100MHz

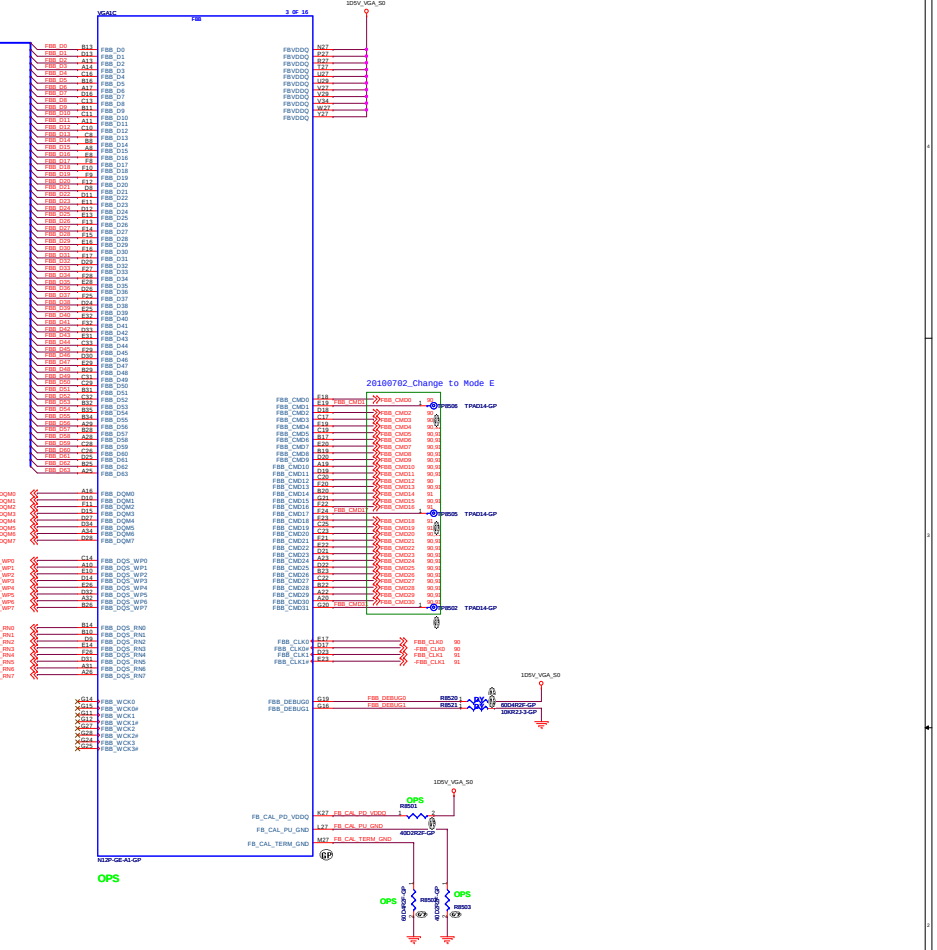




FBCLK Termination place on VRAM side

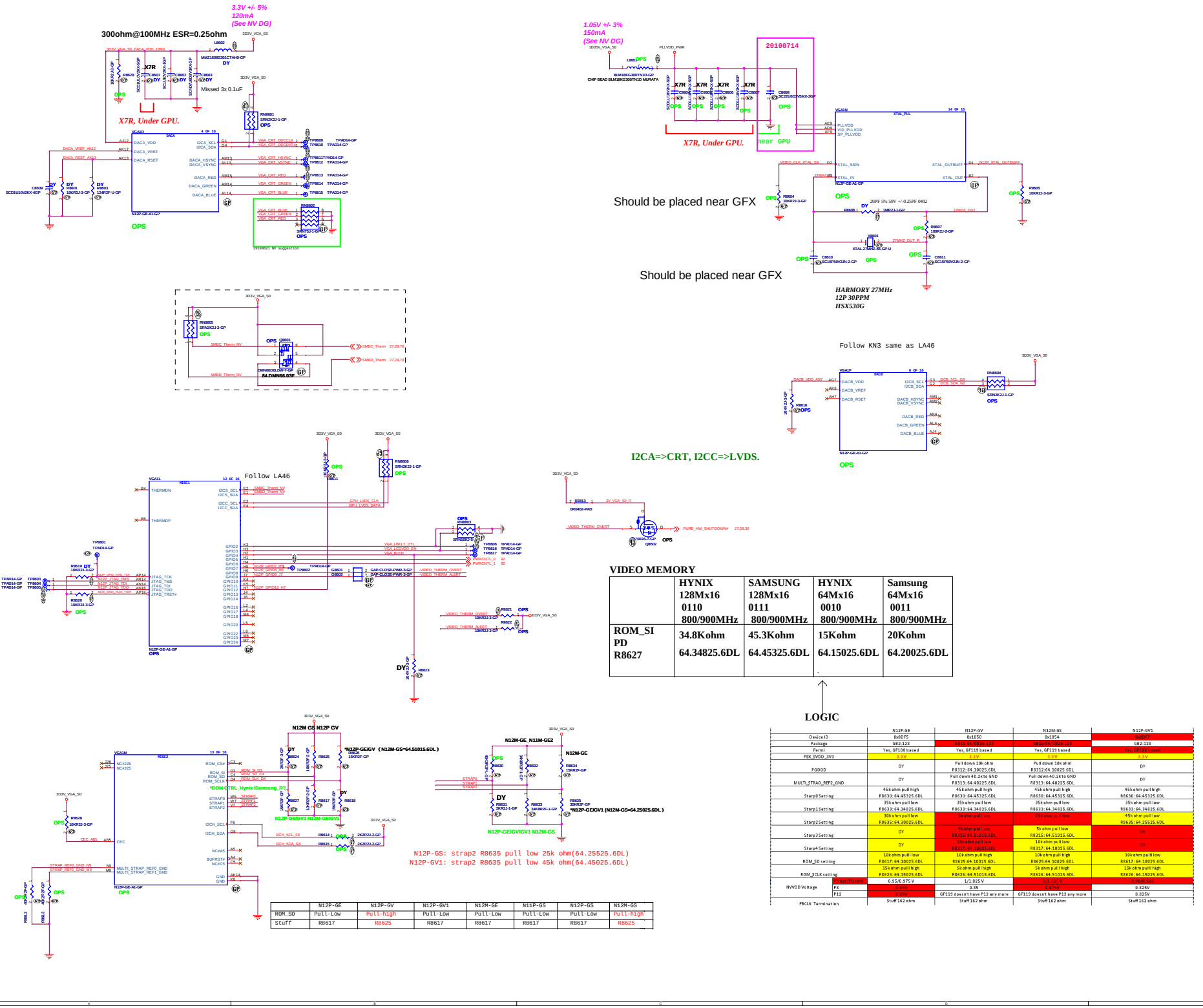


FBCLK Termination place on VRAM side



LA57 UMA

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	N12P-Q1/Q3 (3/6): VRAM I/F
Size: A1	Document Number: LA57
Rev: SD
Date: Friday, December 10, 2010	Sheet 85 of 103



VIDEO MEMORY

	HYNIX 128Mx16 0110 800/900MHz	SAMSUNG 128Mx16 0111 800/900MHz	HYNIX 64Mx16 0010 800/900MHz	Samsung 64Mx16 0011 800/900MHz
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

LOGIC

	N12P-GE	N12P-GV	N12M-GS	N12P-GV1
Device ID	0x0DF5	0x1050	0x1054	0x0DF7
Package	GB2-128	GB1b-64/GB2b-128	GB1b-64/GB2b-128	GB2-128
Fermi	Yes, GF100 based	Yes, GF119 based	Yes, GF119 based	Yes, GF108 based
PEX_VVDD_3V3	3.3V	3.3V	3.3V	3.3V
PGOOD	DY	Pull down 10k ohm R8312:64.10025.6DL	Pull down 10k ohm R8312:64.10025.6DL	DY
MULTI_STRAP_REF2_GND	DY	Pull down 40.2k to GND R8313:64.40225.6DL	Pull down 40.2k to GND R8313:64.40225.6DL	DY
Starp0Setting	45k ohm pull high R8630:64.45325.6DL	45k ohm pull high R8630:64.45325.6DL	45k ohm pull high R8630:64.45325.6DL	45k ohm pull high R8630:64.45325.6DL
Starp1Setting	35k ohm pull low R8633:64.34825.6DL	35k ohm pull low R8633:64.34825.6DL	35k ohm pull low R8633:64.34825.6DL	35k ohm pull low R8633:64.34825.6DL
Starp2Setting	30k ohm pull low R8635:64.30025.6DL	5k ohm pull low	25k ohm pull low	45k ohm pull low R8635:64.25525.6DL
Starp3Setting	DY	5k ohm pull low R8315:64.51015.6DL	5k ohm pull low R8315:64.51015.6DL	DY
Starp4Setting	DY	10k ohm pull low R8317:64.10025.6DL	10k ohm pull low R8317:64.10025.6DL	DY
ROM_S0 setting	10k ohm pull low R8617:64.10025.6DL	10k ohm pull high R8625:64.10025.6DL	10k ohm pull high R8625:64.10025.6DL	10k ohm pull low R8617:64.10025.6DL
ROM_SCLK setting	15k ohm pull high R8626:64.15025.6DL	5k ohm pull high R8626:64.51015.6DL	5k ohm pull high R8626:64.51015.6DL	15k ohm pull high R8626:64.15025.6DL
NVVDD Voltage	*P0 nvi./P0 conf.	0.95/0.975 V	1/1.025 V	0.90/0.925
	P8	0.85V	0.85	0.825V
	P12	0.85V	GF119 doesn't have P12 any more	0.825V
FBCLK Termination		Stuff 162 ohm	Stuff 162 ohm	Stuff 162 ohm

	N12P-GE	N12P-GV	N12P-GV1	N12M-GE	N11P-GS	N12P-GS	N12M-GS
ROM_S0	Pull-Low	Pull-high	Pull-Low	Pull-Low	Pull-Low	Pull-Low	Pull-high
Stuff	R8617	R8625	R8617	R8617	R8617	R8617	R8625

LA57 LIMA

Wistron Corporation
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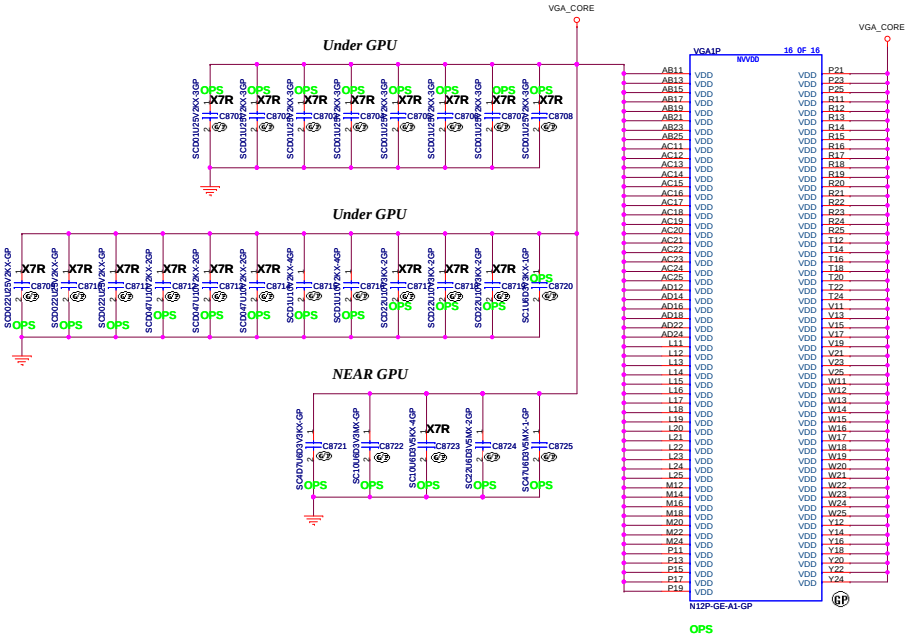
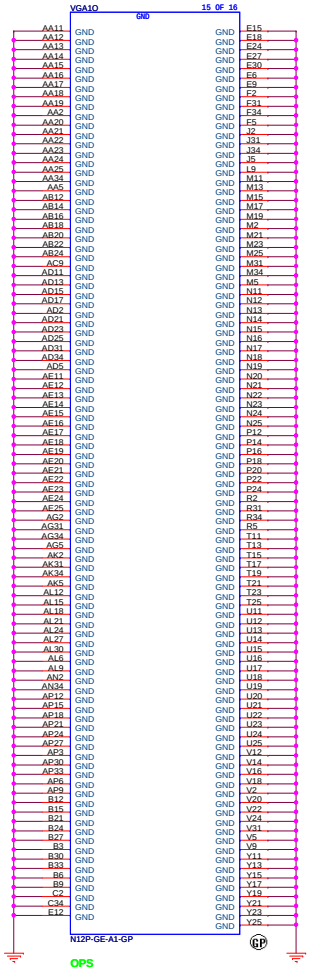
Title: N12P-Q1/Q3 (4/6): GPIO

Size: A1 | Document Number: LA57 | Rev: SD

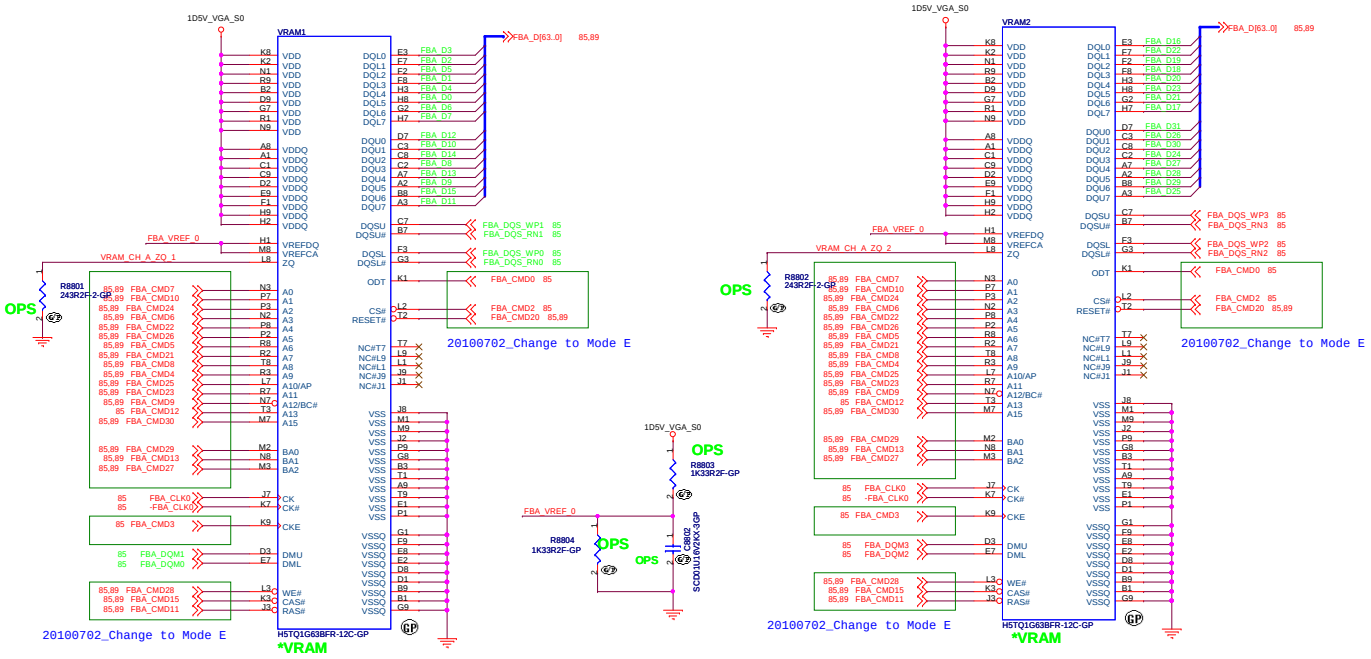
Date: Friday, December 10, 2010 | Sheet 86 of 103



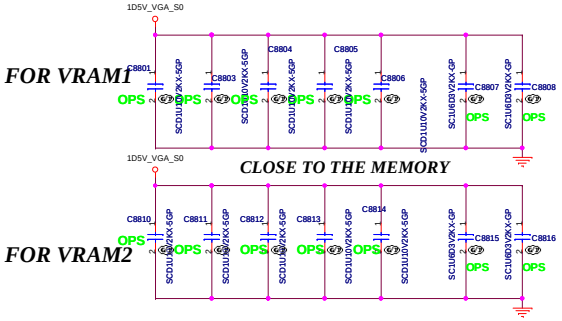


LA57 UMA

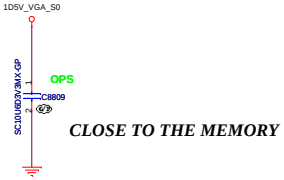
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *N12P-Q1/Q3 (5/6): POWER*		
Size: A2	Document Number: LA57	Rev: SD
Date: Friday, December 10, 2010	Sheet 87 of 103	



FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

LA57 UMA

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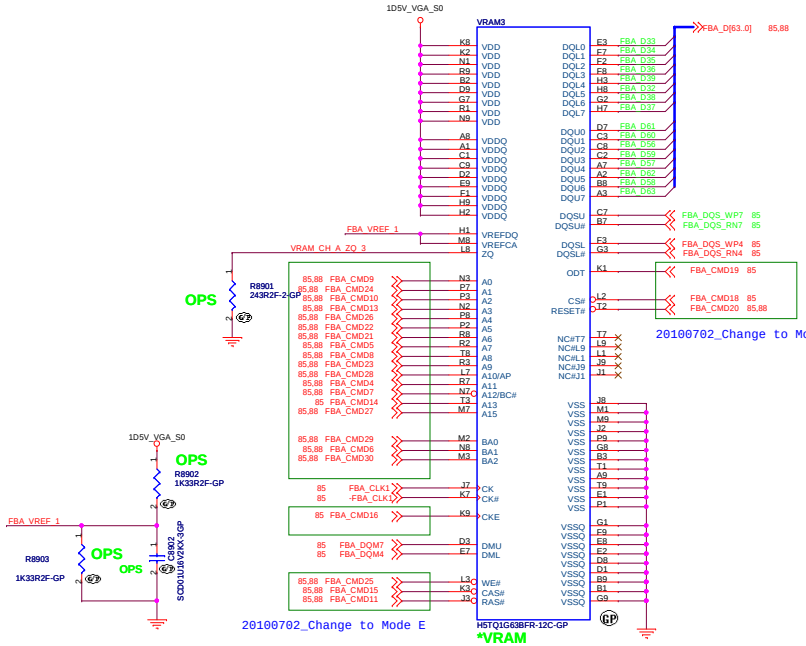
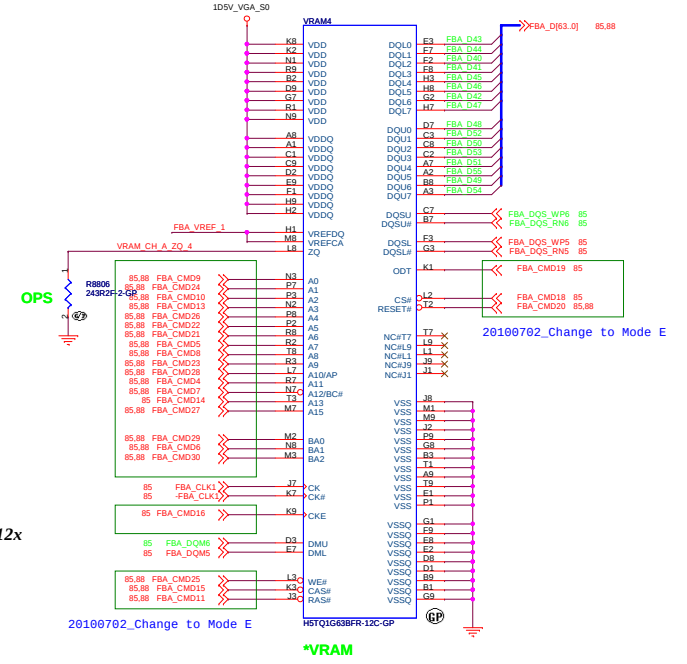
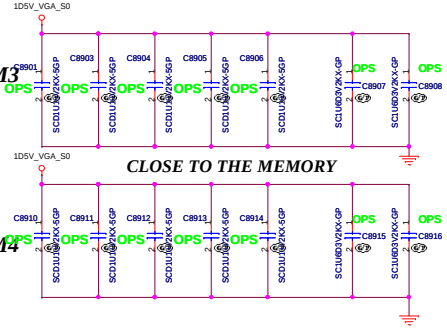
Title: *VRAM CHANNEL-A*		
Size: A2	Document Number: LA57	Rev: SD
Date: Friday, December 10, 2010	Sheet 88 of 103	





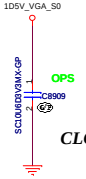
FB CMD mapping Mode D-N12x



FOR VRAM3

CLOSE TO THE MEMORY

FOR VRAM4



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

<Core Design>

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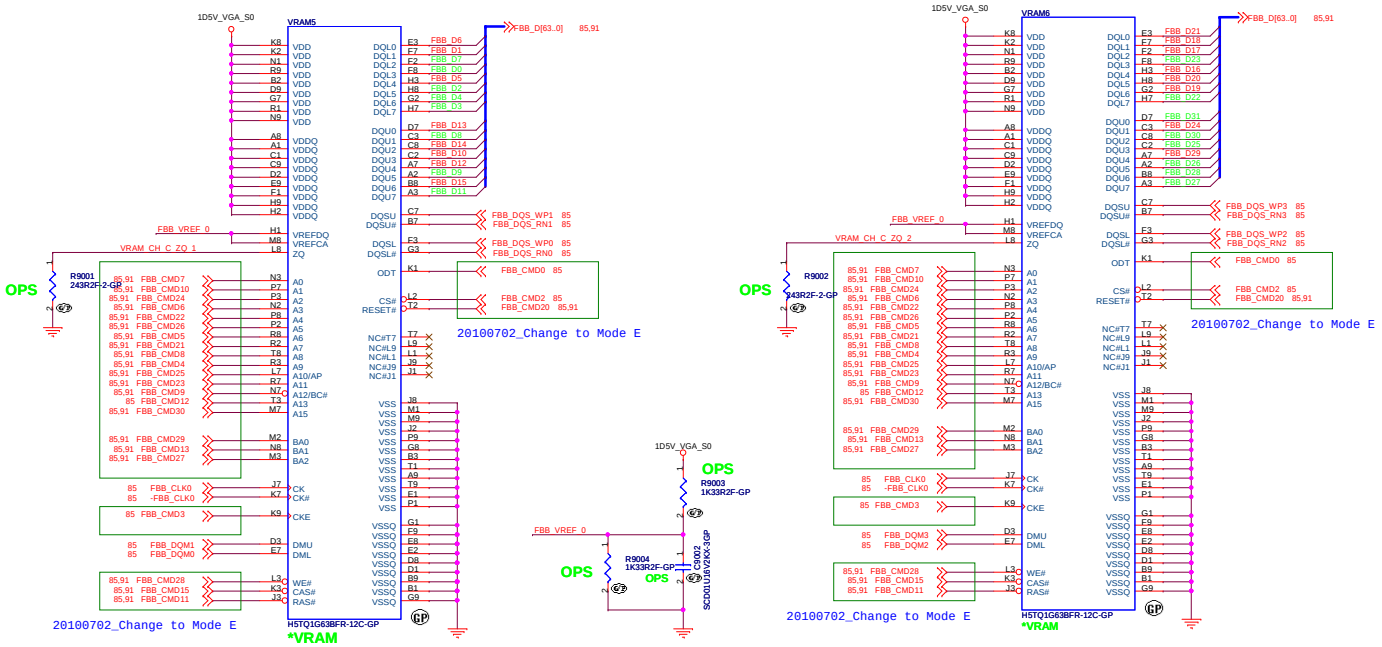
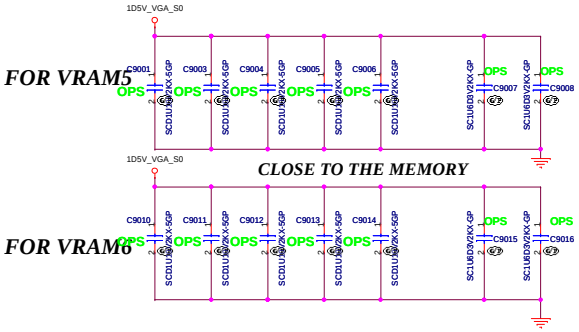
Title: **VRAM CHANNEL-A**

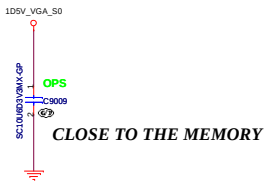
Size: A2 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 89 of 103



DG requires 4x0.1uF and 8x1.0uF per VRAM chip





VIDEO FRAME BUFFER PORT C

<Core Design>

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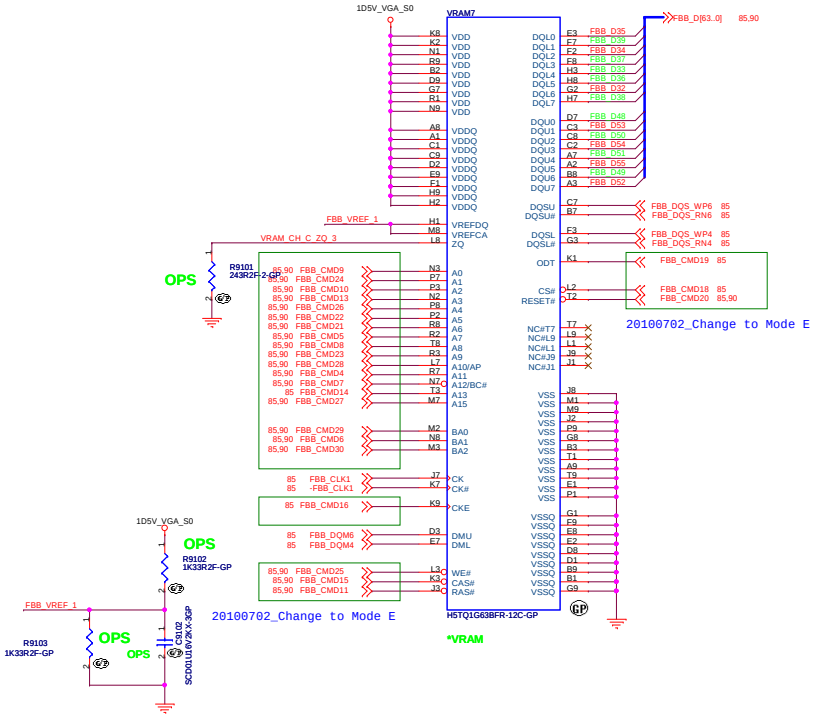
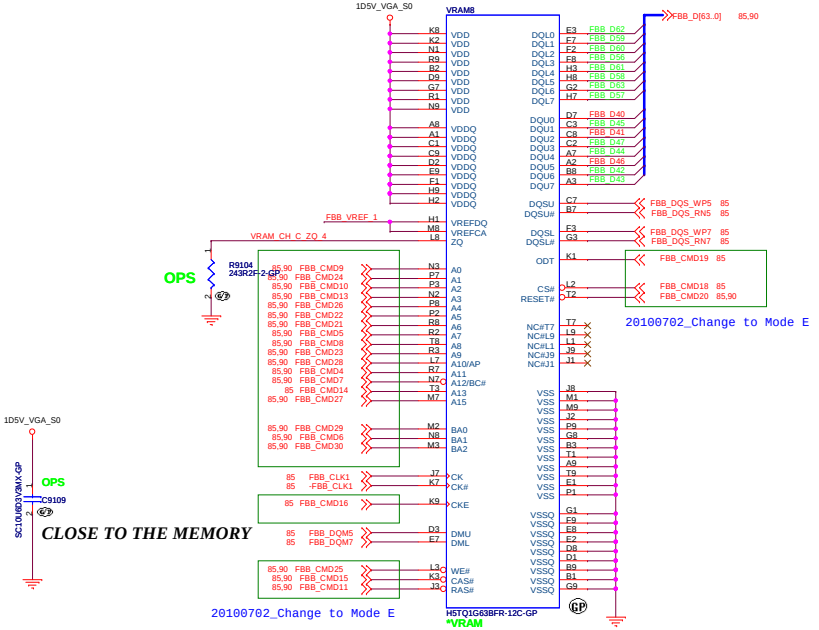
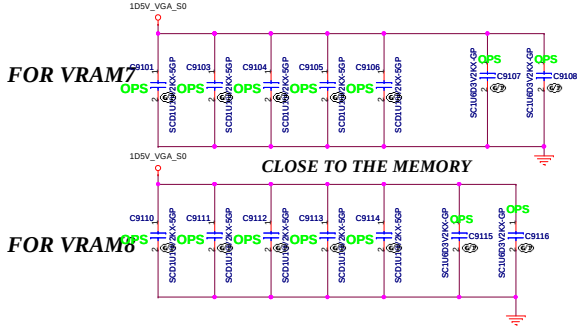
Title			
VRAM CHANNEL-C			
Size: A2	Document Number: LA57		Rev: SD
Date: Friday, December 10, 2010	Sheet 90 of 103		







VIDEO FRAME BUFFER PORT C

<Core Design>

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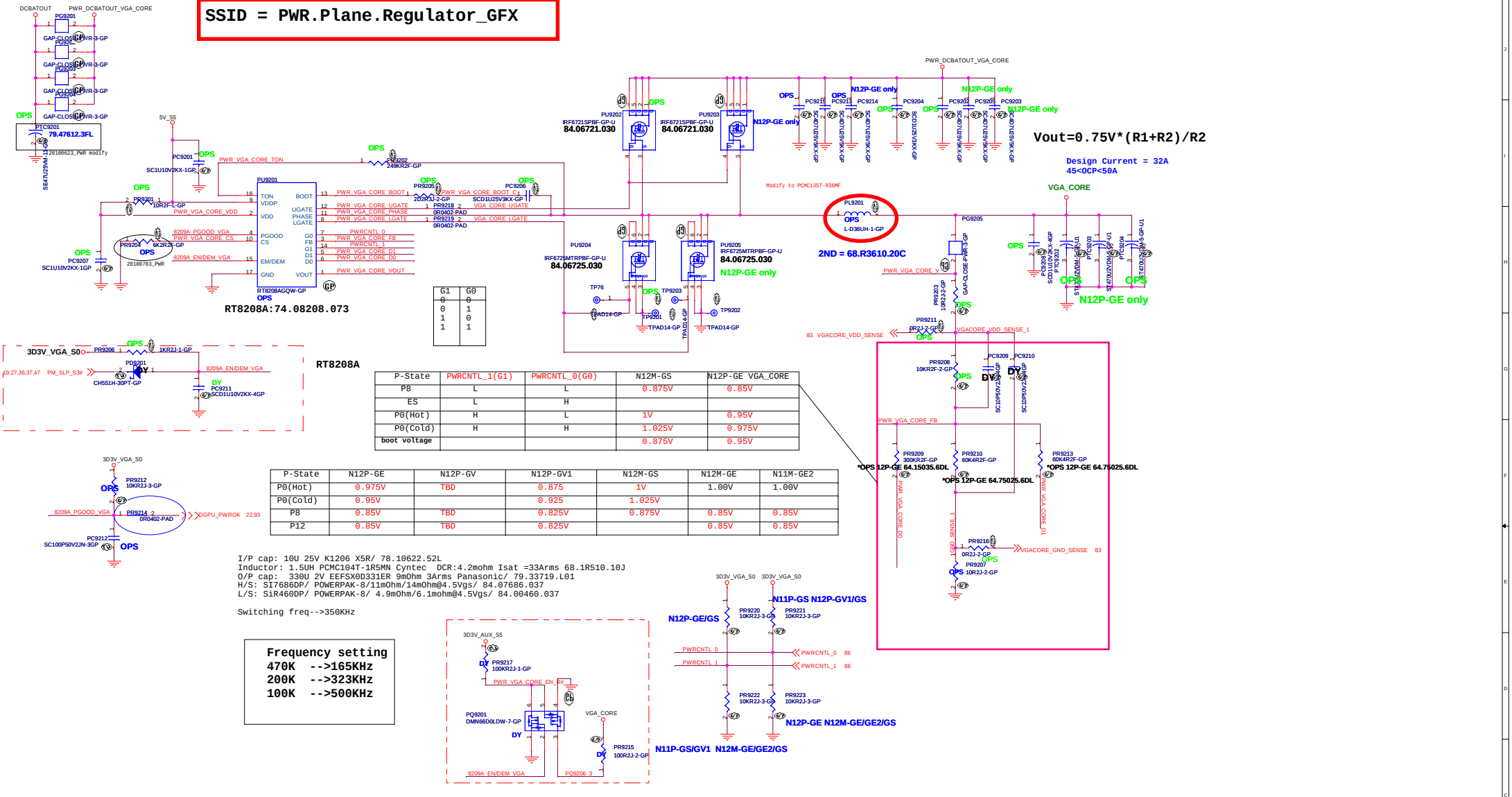
Title	VRAM CHANNEL-C	
Size A2	Document Number LA57	Rev SD
Date: Friday, December 10, 2010	Sheet 91 of 103	

SSID = PWR.Plane.Regulator_GFX



G1	G0
0	0
0	1
1	0
1	1

RT8208A

P-State	PWRCNTL_1(G1)	PWRCNTL_0(G0)	N12M-GS	N12P-GE VGA_CORE
P8	L	L	0.875V	0.85V
ES	L	H		
P0(Hot)	H	L	1V	0.95V
P0(Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
P0(Hot)	0.975V	TBD	0.875	1V	1.00V	1.00V
P0(Cold)	0.95V		0.925	1.025V		
P8	0.85V	TBD	0.825V	0.875V	0.85V	0.85V
P12	0.85V	TBD	0.825V		0.85V	0.85V

LA57 UMA

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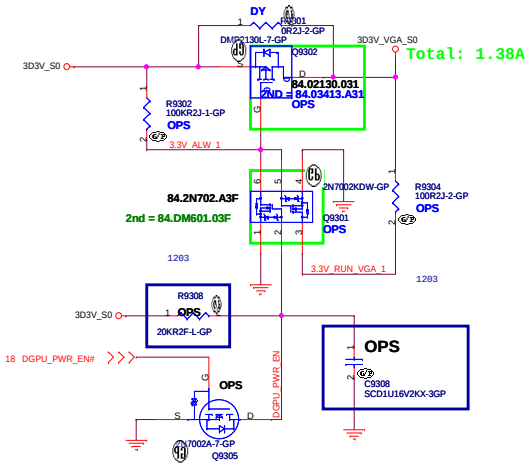
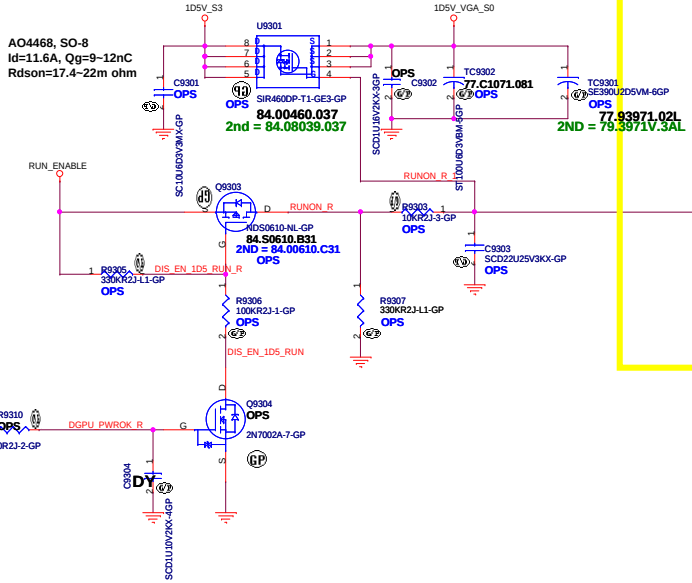
Title	DC/DC_VGA CORE_RT8208B	
Size	Document Number LA57	Rev SD
Date: Friday, December 10, 2010	Sheet 92 of 103	

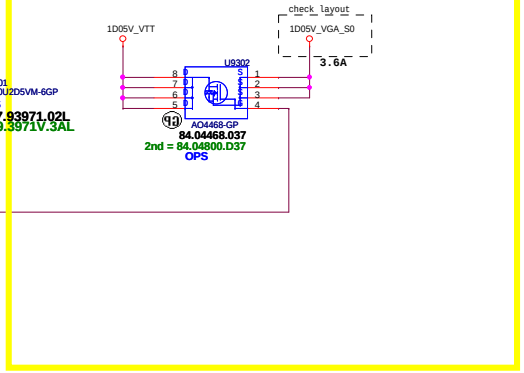
+3VS to 3.3V_DELAY Transfer



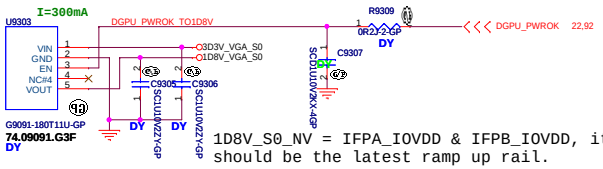
1D5V_VGA_S0



1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

LA57 UMA

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Title: DISCRETE VGA POWER

Size | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 93 of 103

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Title: *LVDS_Switch*

Size	Document Number	Rev
A2	LA57	SD

Date: Friday, December 10, 2010 Sheet 84 of 103

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LA57 UMA

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Title: CRT_Switch

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 10, 2010 | Sheet 95 of 103

LA57 UMA

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Title

TOUCH PANEL

Size	Document Number	Rev
A4	**LA57**	**SD**

Date: Friday, December 10, 2010 Sheet 96 of 103

CPU Plate

H13 HOLE276R178-GP — ZZ.00PAD.N11
H14 HOLE276R178-GP — ZZ.00PAD.N11
H15 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H10 STF237R128H42-GP — OPS — 34.4GD01.101
H11 STF237R128H42-GP — OPS — 34.4GD01.101

Check test point

3D3V_S0	TP8507	TPAD14-GP
3D3V_AUX_S5	TP8508	TPAD14-GP
3D3V_S5	TP8509	TPAD14-GP
5V_S5	TP8510	TPAD14-GP
11,19,27 PM_PWRBTN#	TP8511	TPAD14-GP
5,11,22,36 H_CPUPWRGD	TP8512	TPAD14-GP
27,36 S5_ENABLE	TP8513	TPAD14-GP
5,11,18,27,31,35,36,65,66,71,83 PLT_RST#	TP8514	TPAD14-GP

Test Point放在Dimm Door打開可量測處

Structure boss

H1 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H2 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H3 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H5 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H6 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H12 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H7 HOLE335R115-GP — ZZ.00PAD.D01
H8 HOLE335R115-GP — ZZ.00PAD.D01

MiniPCI Std-Off

H4 STF237R113H115-GP — 34.4V802.101

H16 GNDPAD — ZZ.NDPAD.XXX
H17 GNDPAD — ZZ.NDPAD.XXX

S1 SPRING-12-GP-U1 — 34.41Y19.001

S3 LZ57 SPRING-63-GP — 34.4Y806.001
S2 LZ57 SPRING-63-GP — 34.4Y806.001

1127 change

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN# — TP9701 TPAD40-GP, TP9700 TPAD40-GP

POWER TESTING POINT--Bottom

27,68 KBC_PWRBTN# — TP9702 TPAD40-GP, TP9703 TPAD40-GP

AD+

EC9708 SCD1U25V2KX-GP
EC9709 DY SCD1U25V2KX-GP
EC9710 SCD1U25V2KX-GP
EC9711 DY SCD1U25V2KX-GP
EC9712 DY SCD1U25V2KX-GP
EC9713 SCD1U25V2KX-GP

DCBATOUT

EC9714 SCD1U25V2KX-GP
EC9715 SCD1U25V2KX-GP
EC9716 SCD1U25V2KX-GP
EC9717 SCD1U25V2KX-GP
EC9718 SCD1U25V2KX-GP
EC9719 SCD1U25V2KX-GP

20100902 add for EMI request

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: LA57 | Rev: SD
Date: Friday, December 10, 2010 | Sheet 97 of 103

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Title: ***Change History***

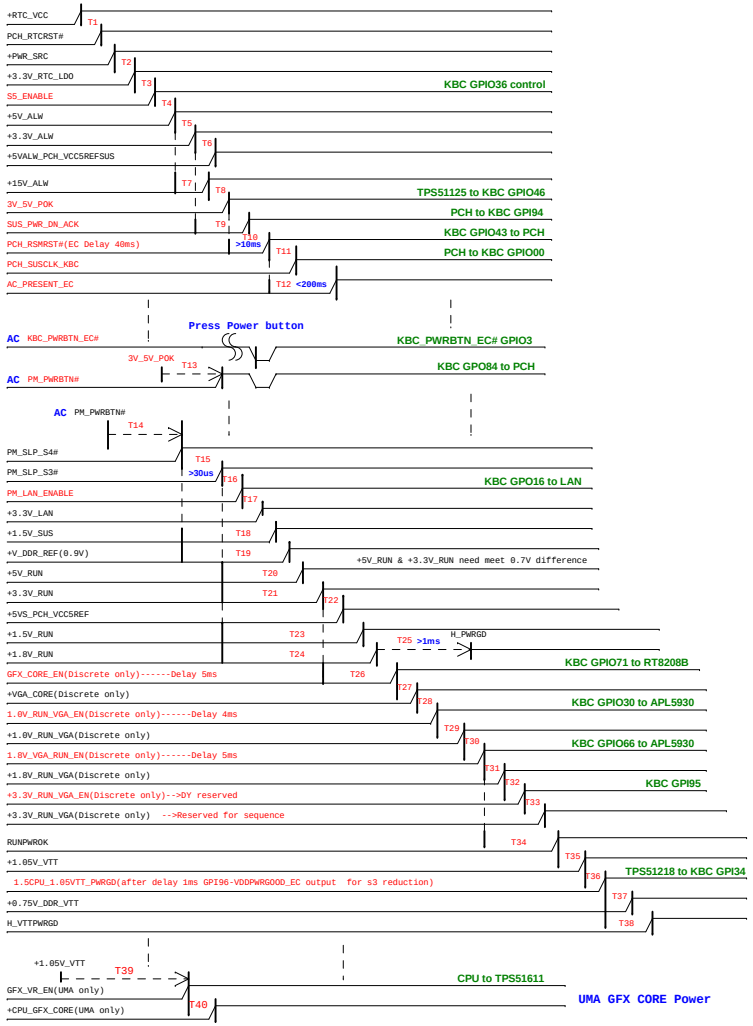
Size	Document Number	Rev
A4	LA57	SD

Date: Friday, December 10, 2010 Sheet 98 of 103

Intel-Power Up Sequence

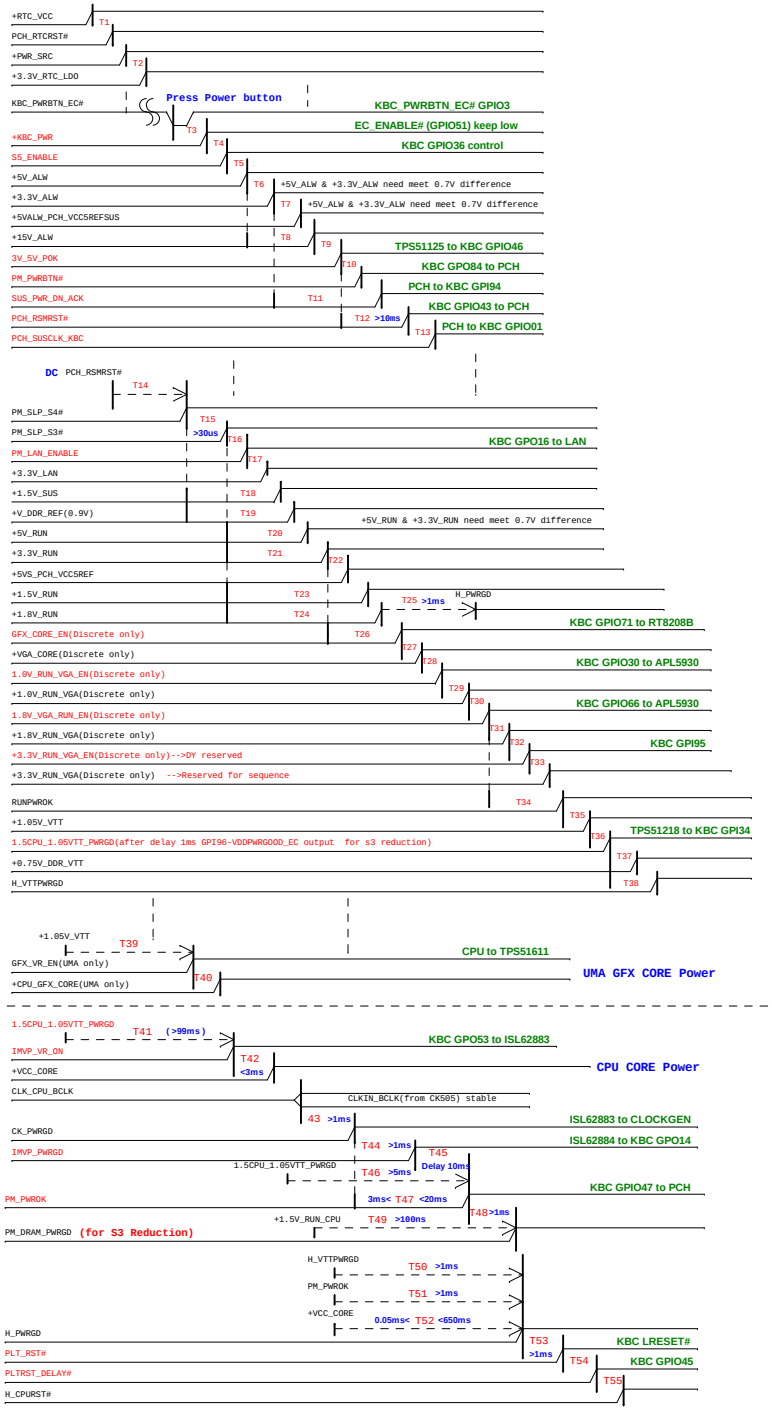
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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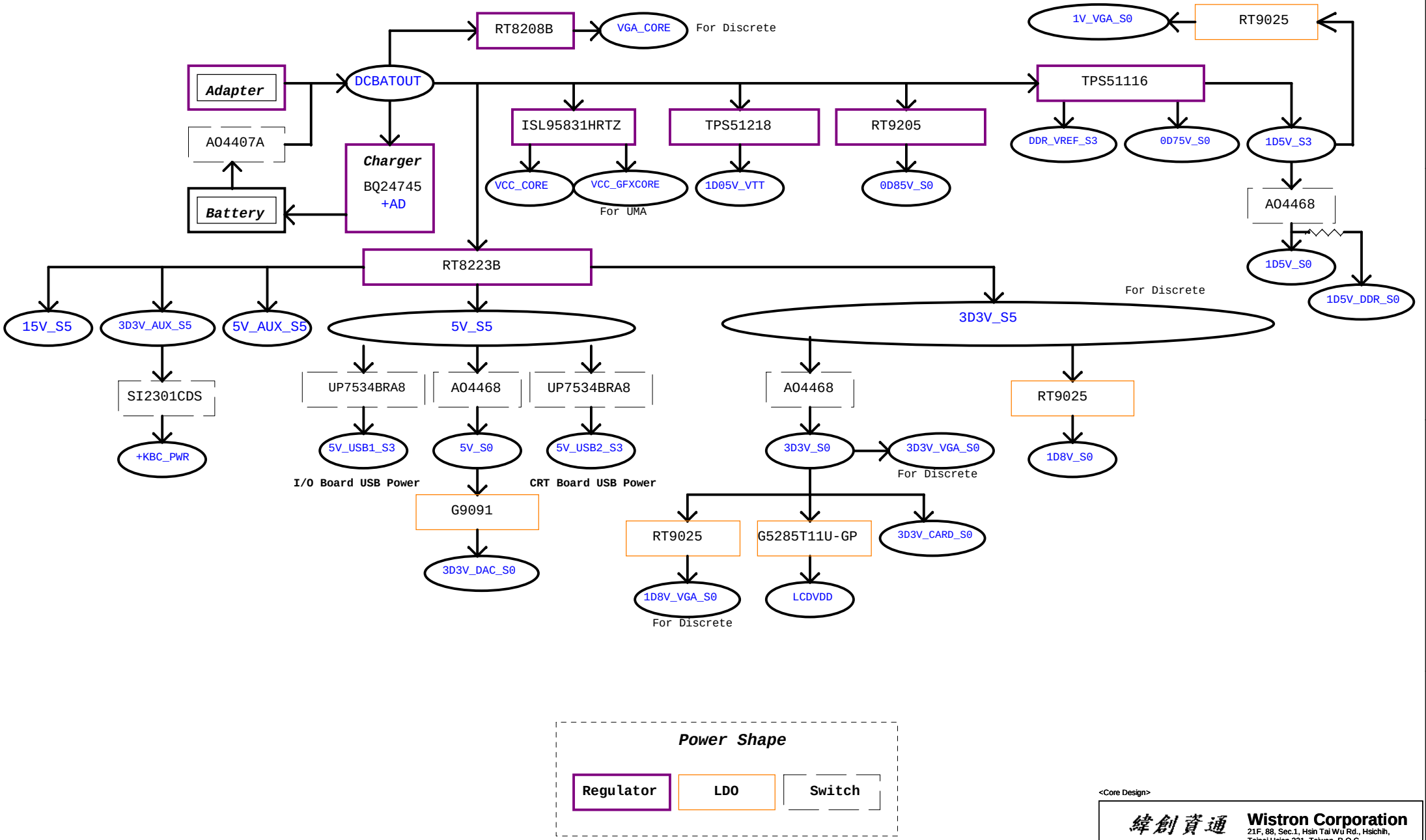
Title: Power Sequence

Size: A3 | Document Number: LA57 | Rev: SD

Date: Friday, December 30, 2005 | Sheet 59 of 103



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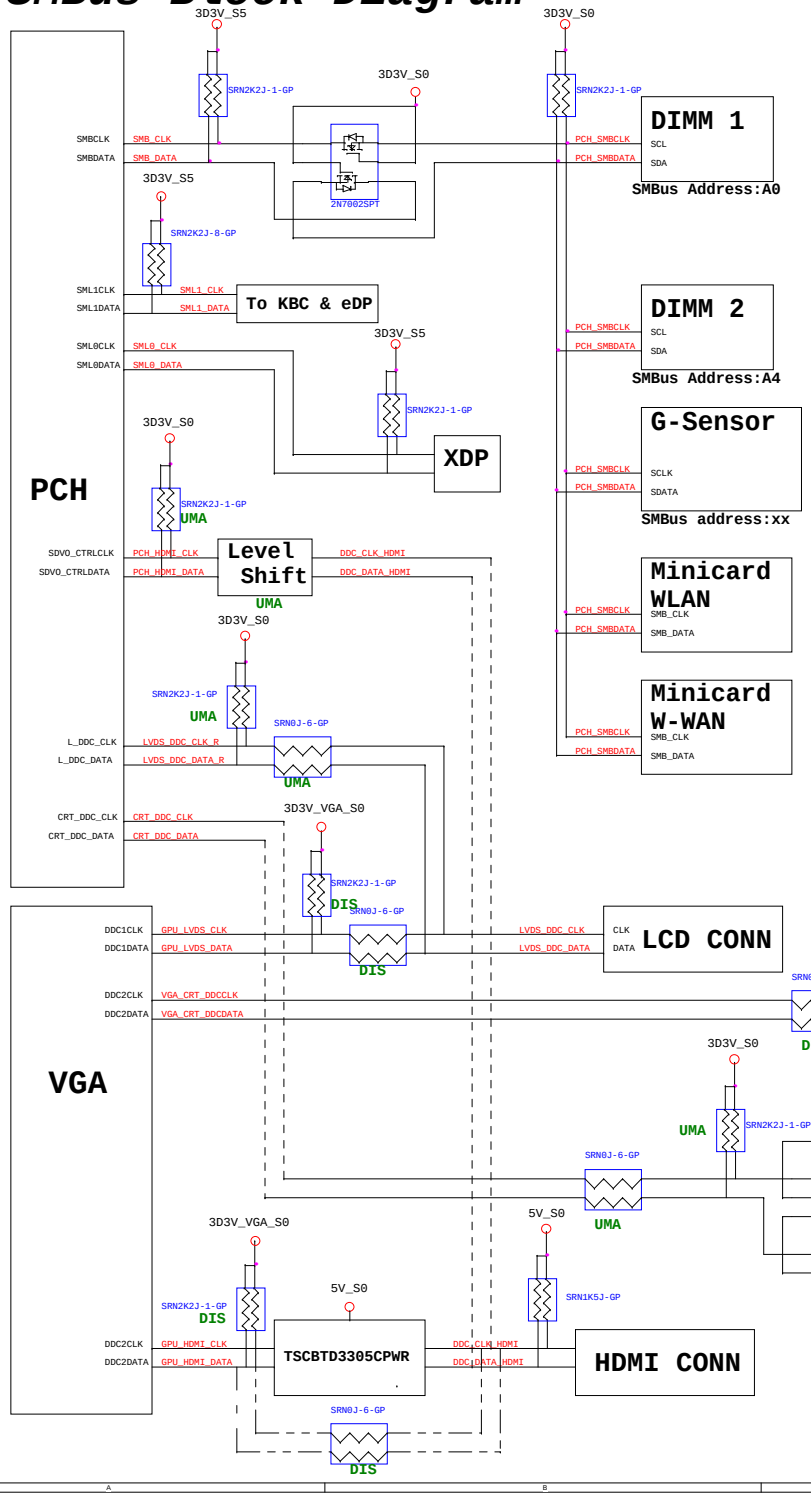
Title: Power Block Diagram

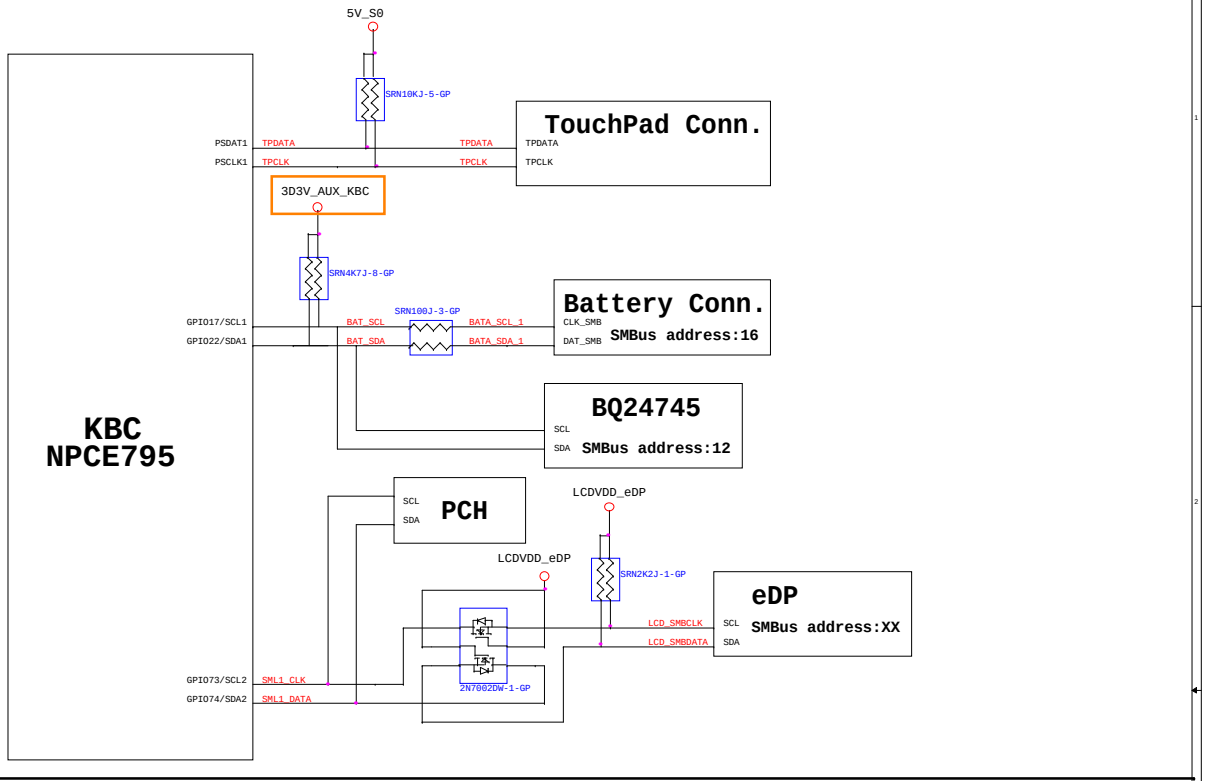
Size	Document Number	Rev
A3	LA57	SD

Date: Friday, December 10, 2010 Sheet 100 of 103

PCH SMBus Block Diagram



KBC SMBus Block Diagram



VGA

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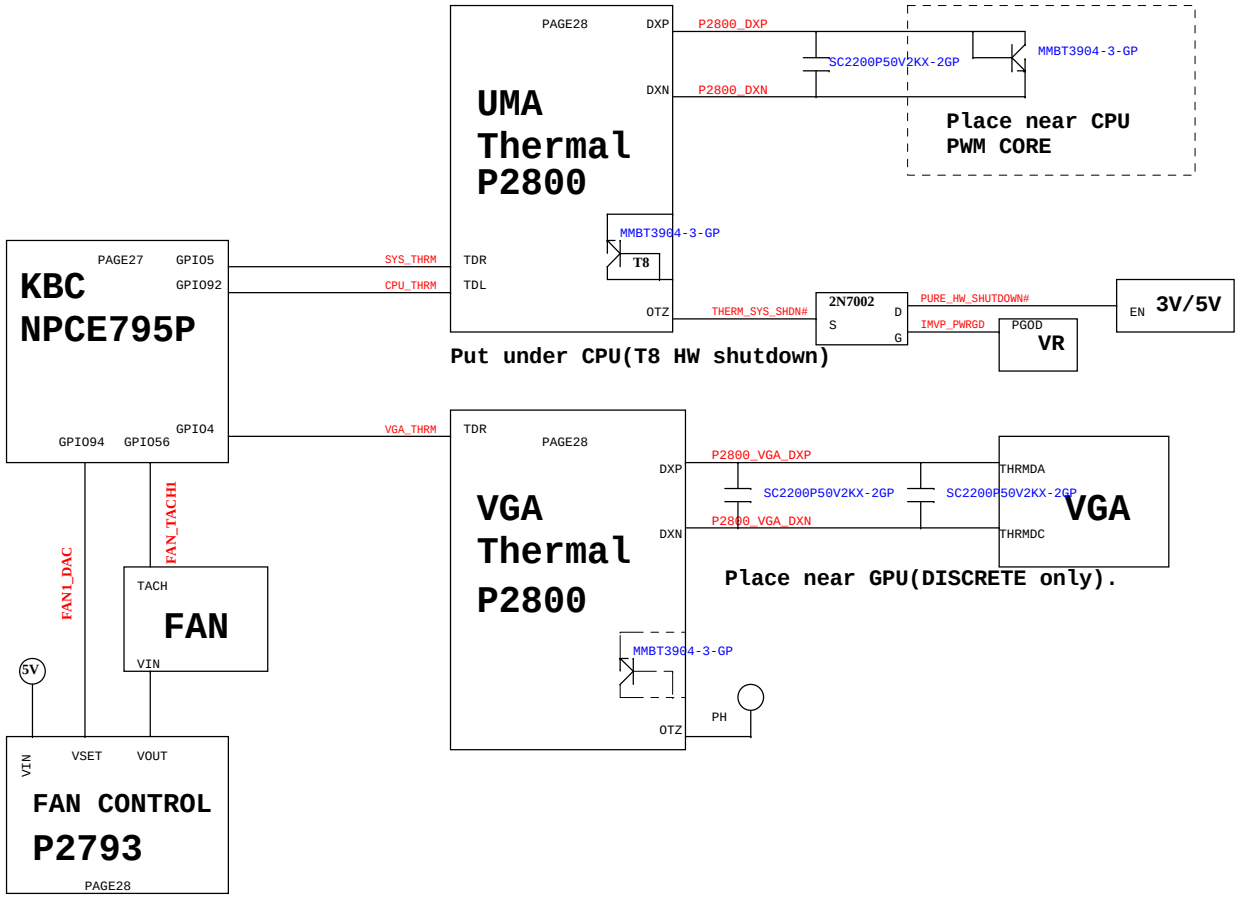
Title: SMBUS Block Diagram

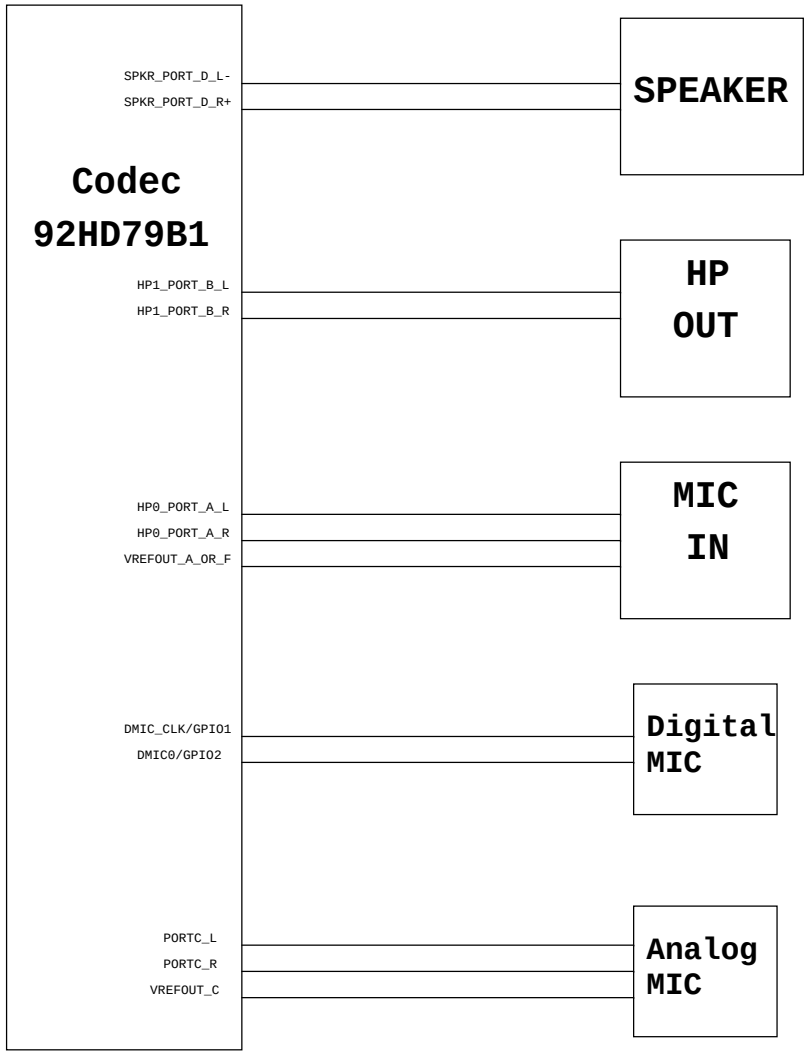
Size	Document Number	Rev
A2	LA57	SD

Date: Friday, December 10, 2010 Sheet 101 of 103

Thermal Block Diagram



Audio Block Diagram



<Core Design>

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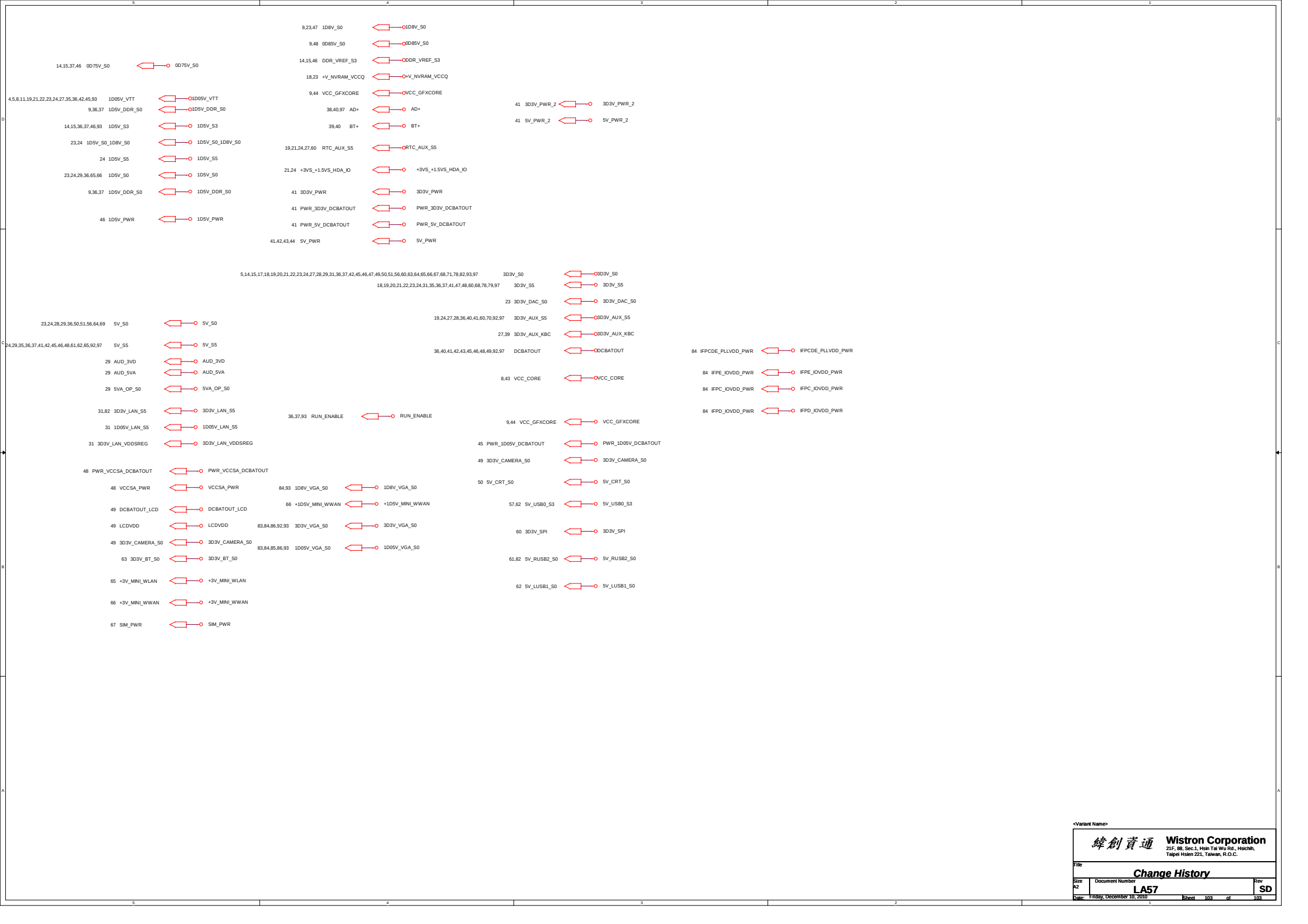
Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	LA57	SD

Date: Friday, December 10, 2010 Sheet 102 of 103



<Variant Name>

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Title: ***Change History***

Size	Document Number	Rev
A2	LA57	SD

Date: Friday, December 10, 2010 Sheet 103 of 103