NLA CFL-H & N17P SYSTEM DIAGRAM

01

Charge PG.40
DDR4 PG.43
CPU Core PG.46~48
+1.0V/+1.2VSUS PG.50
+3V/+5V S5 PG.42
+VGACORE PG.51~53
+1.35V_GFX PG.54

Config#3 SODIMM 1DPC

SODIMM1 Max. 8GB STD PG.17 — DDR4 2133MHz — Channel A
SODIMM2 Max. 8GB RSV PG.18 — DDR4 2133MHz — Channel B

INTEL Coffee Lake -H
Processor : Quad Core
Power : 45 (Wat t)
Package : BGA1440
Size : 42 x 28 (mm)
Die Size : 13.6 x 9.1 (mm)
PG.2~8

PEG X8 Lane → NVIDIA N17P-G0-A1
Package 29 x 29mm
40W
PG.19~23
27MHz PAGE 21

NVIDIA N17P-G0-A1 → VRAM gDDR5 x 4pcs
128M x32 / 256M x32
2.5GHz
PG.24~25

NVIDIA N17P-G0-A1 → HDMI v2.0 PG.27

eDP (5.4Gb/s) eDP → 15.6" eDP Panel HD/FHD/UHD PG.26

DMI

M.2 2280-D5 SSD PG.34 — SATA0 6GB/s SATA1A / PCIEx4 32GB/s LANE9,10,11,12

HDD PG.34 — SATA0 6GB/s SATA4

INTEL PCH
Lynx Point
Power : Wat t
Package : FCBGA837
Size : 23 x 23 (mm)
PG.9~16

USB 3.0
PORT1 → USB 3.0 Ports PG.30
PORT2 → USB 3.0 Ports (DB) PG.37
PORT4 → USB3.0 (TYPE C) PG.33

USB 2.0
PORT1 → USB 3.0 Ports PG.30
PORT2 → USB 3.0 Ports (DB) PG.37
PORT5 → HD CAM PG.26

PCI-E x 1 Gen1
LANE14 → LAN RTL8111HSH-CG. PG.36
LANE16 → Card Reader RTS5227S PG.37
LANE15 → WLAN BT COMBO PG.34

USB 2.0 PORT7 → WLAN BT COMBO PG.34

SPI → ROM PG.12

LPC → KBC ITE IT8987E/BX PG.37
KBC → KB PG.39
KBC → TP PG.39
KBC → FAN PG.39

Azalia → AUDIO CODEC ALC255-CG PG.28
Hp / MIC → Combo Jack (DB) PG.37
Speaker PG.28
Dual Digital MIC PG.26
INT CAM MIC PG.26

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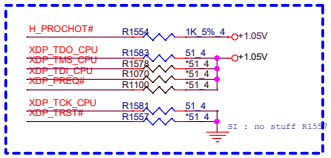
CFL-H Processor (CLK,MISC,JTAG)

02

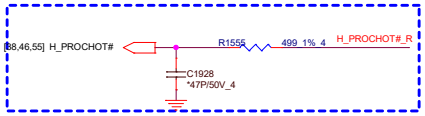
Processor pull-up (CPU)

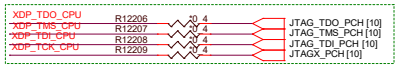


PROCHOT# (50ohm)

Trace Length <11 inches

Cb need placment near VR





Layout Notes:

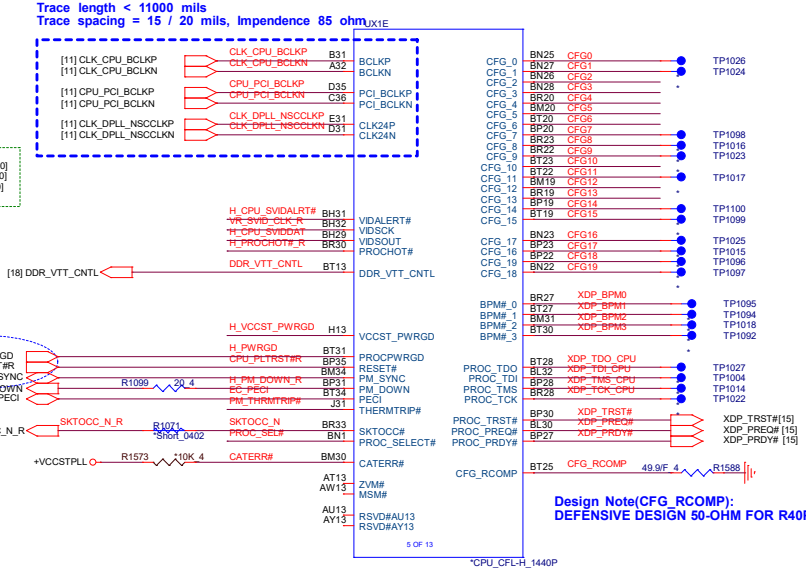
H_PWRGD (50ohm)
Trace Length: 1~11 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

Host CLK:

Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm



Design Note(CFG_RCOMP):

DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

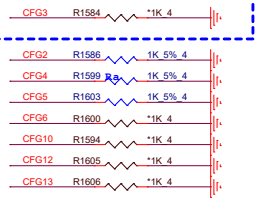
	CFG[4]	Ra
EDP Output from DGPU	Hi	Non Stuff
EDP Output from iGPU	Low	Stuff

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

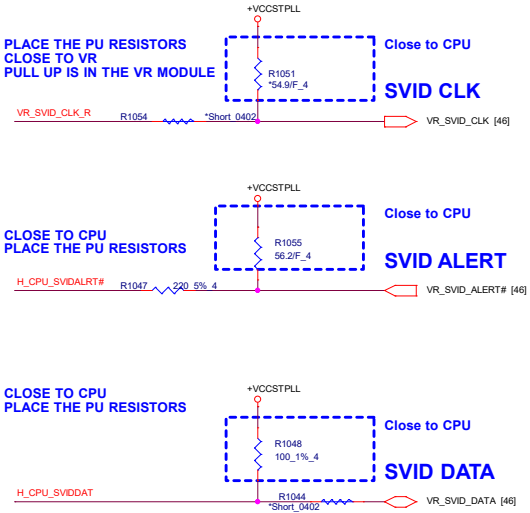
0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;



CPU CORE SVID

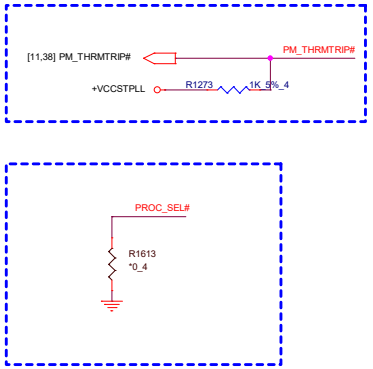
Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.



THERMTRIP# (50ohm)

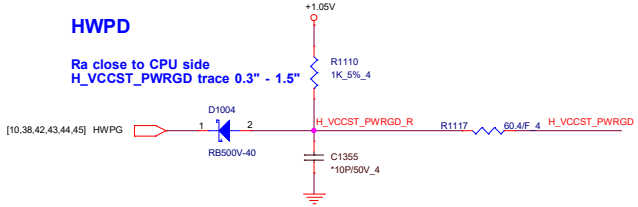
Trace Length: 1.1~12 inches

Rb need placment near PCH



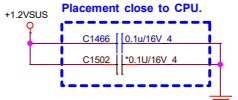
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OEM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

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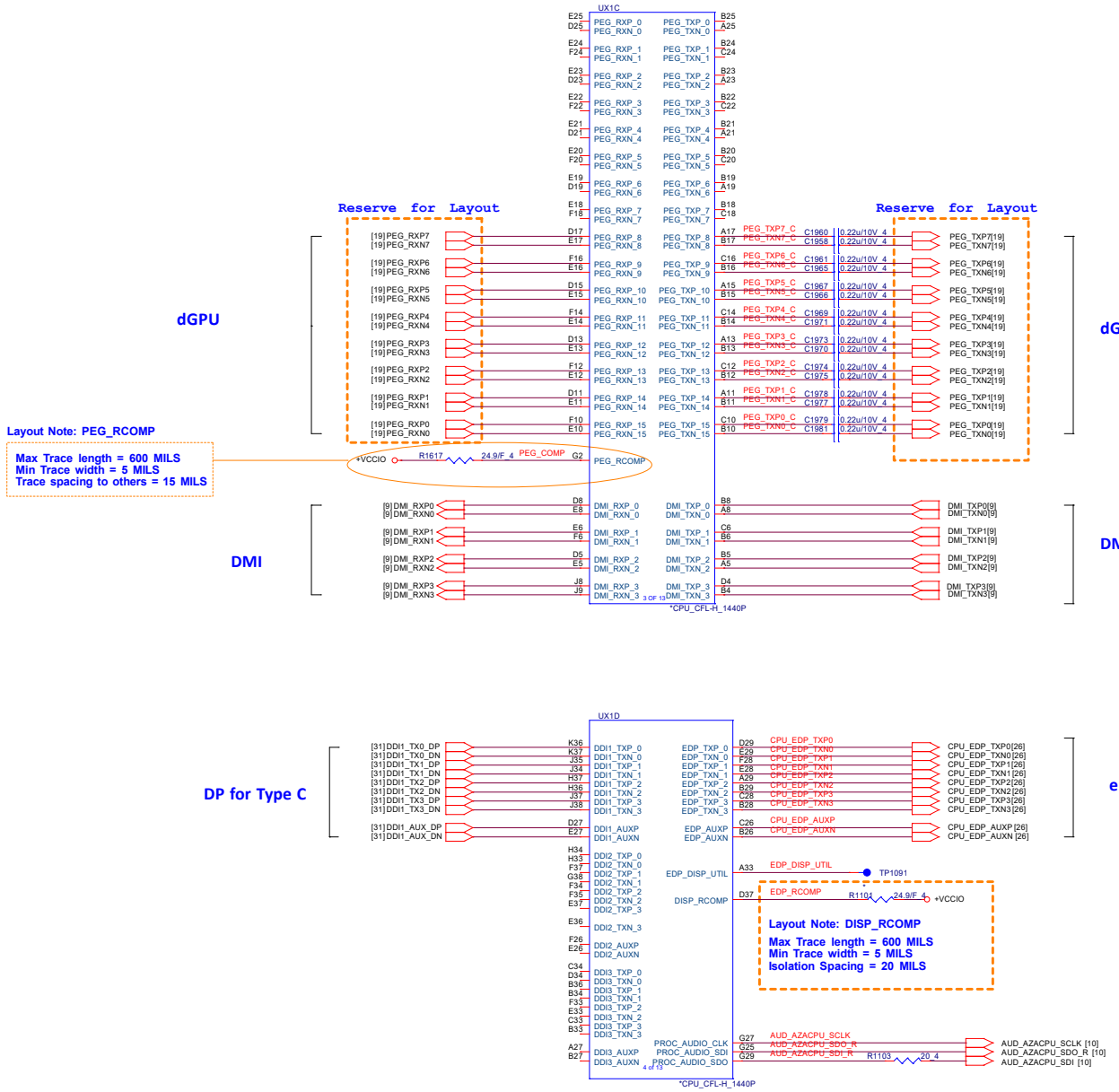
CFL-H Processor (DMI,PEG,FDI)

+1.2VSUS[2,6,10,17,18,43,45]
+3VSS[10,12,14,28,30,31,32,34,38,42,43,44,45,46,50,55]
+3V[9,10,11,13,14,16,17,18,21,22,26,28,29,34,35,36,37,38,39,46,49,50,54,55]



PROJECT : NLA
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Size	Document Number	Rev
Custom	CFL 2/7 (DMI/EDP/PEG)	1A

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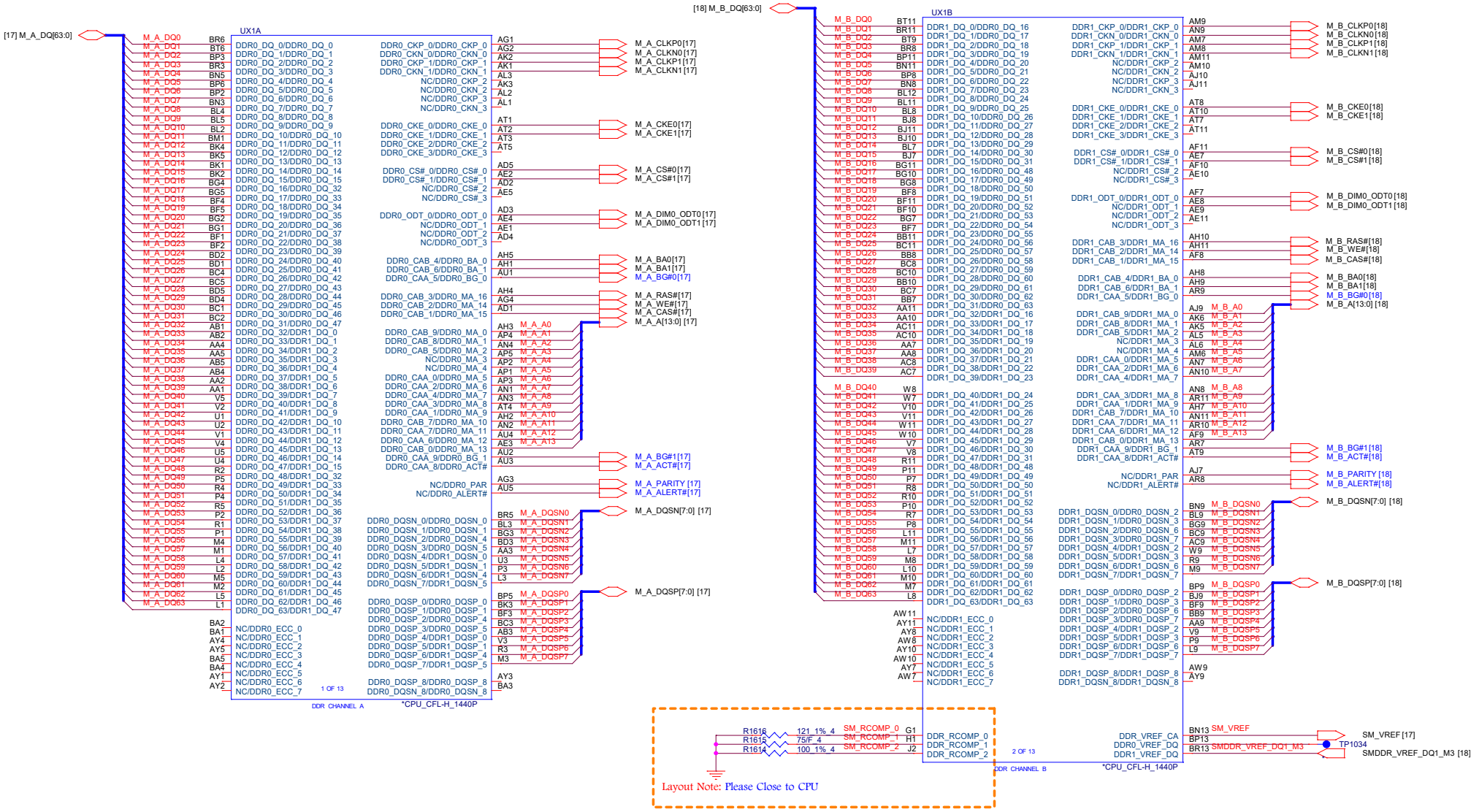
CFL-H Processor (DDR4)



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Size: Custom	Document Number: CFL 3/7 (DDR4 I/F)	Rev: 1A
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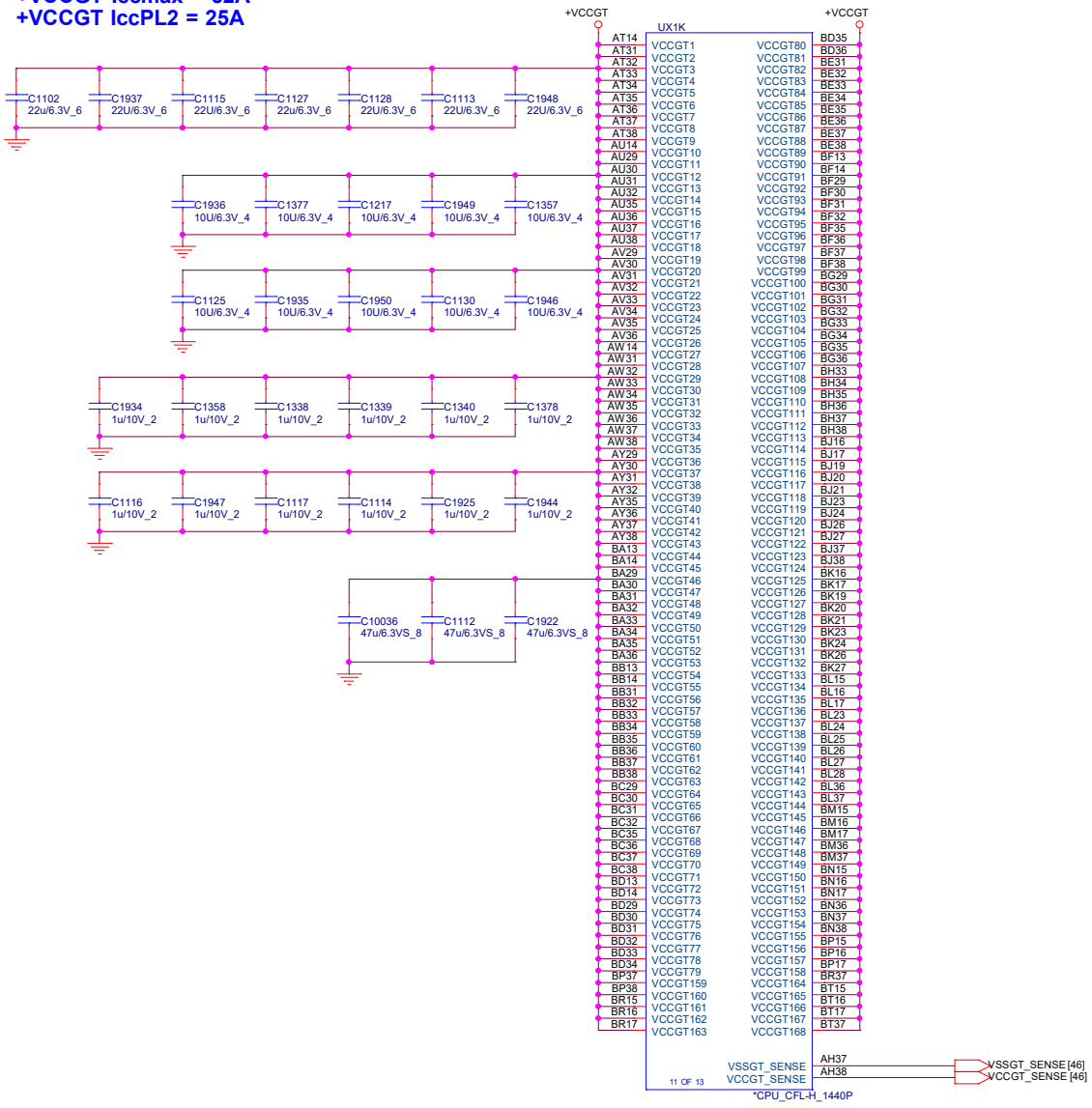
SKYLAKE Processor (POWER)

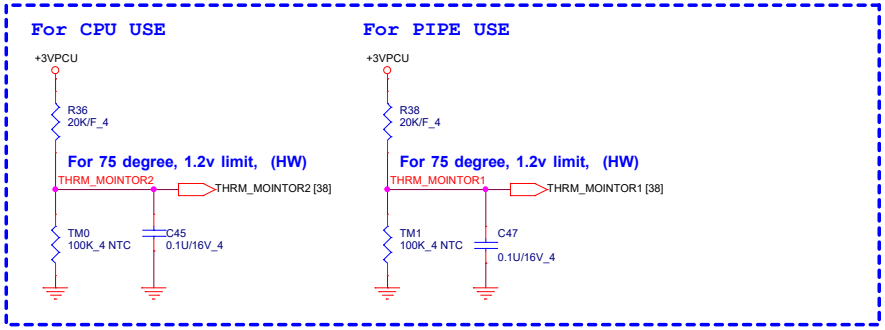
From CFL-H Power Map
+VCCGT Iccmax = 32A
+VCCGT IccPL2 = 25A



+VCCGT [46,49]
+1.2VSUS [2,6,10,17,18,43,45]

IO Thrm Protect

Location need thermal confirm



PROJECT : NLA
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Custom	CFL 4/7 (POWER)	1A
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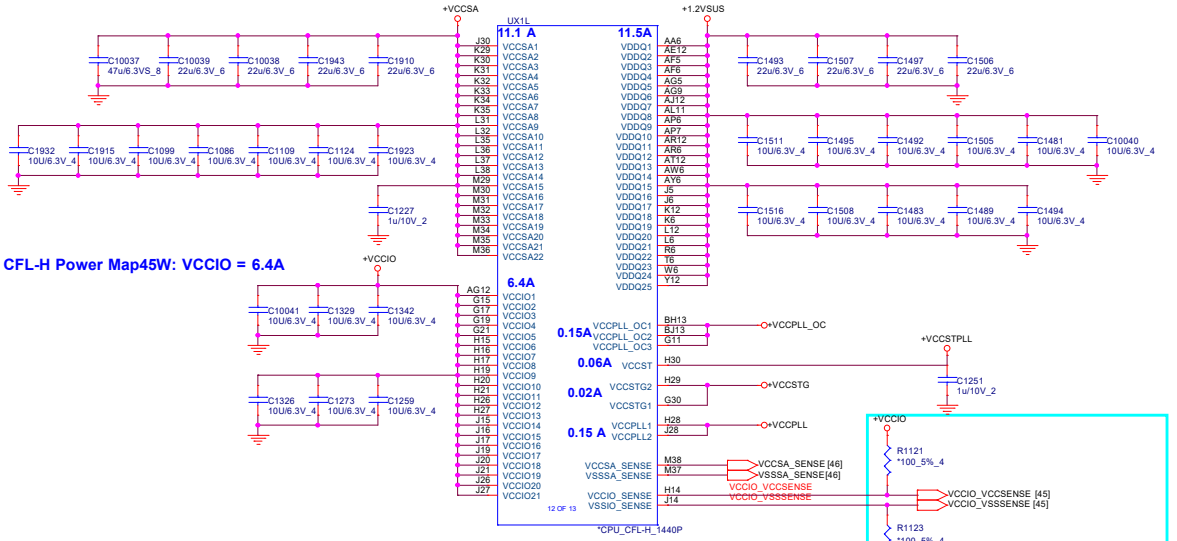
+VCCSA [46,49]
+VCCIO [3,45]
+1.2VSUS [2,10,17,18,43,45]

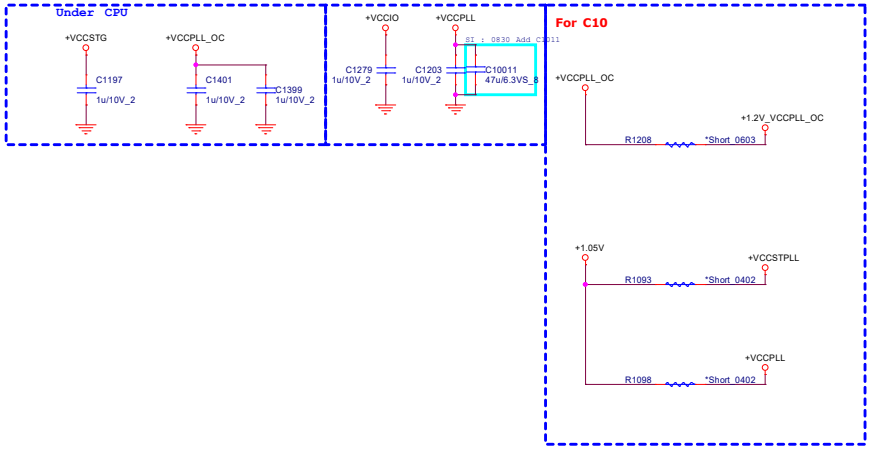
Follow CFL-H Power Map 45W(GT2): VCCSA=11.1A

Follow CFL-H Power Map 45W: VDDQ=11.5A



Follow CFL-H Power Map45W: VCCIO = 6.4A

Close CPU



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Custom	CFL 5/7 (POWER&GND)	1A

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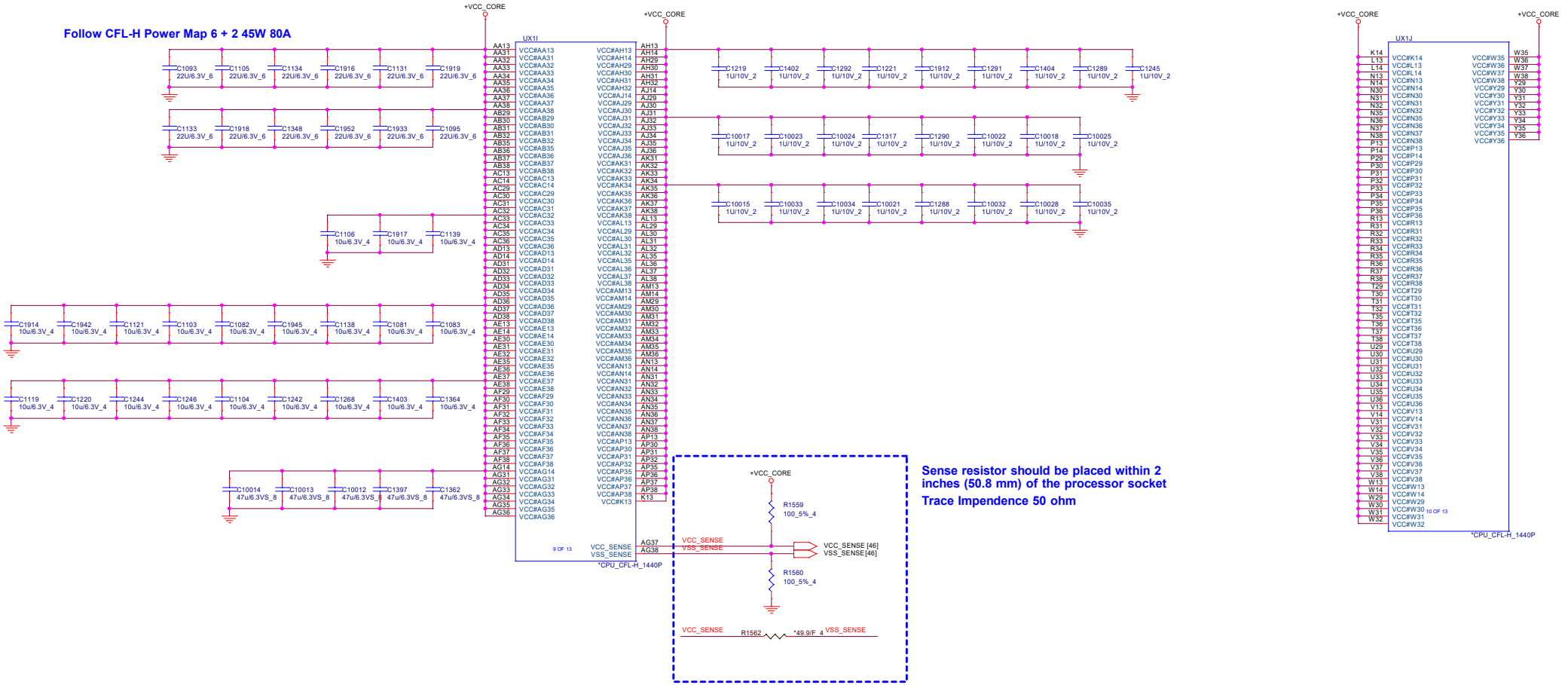
+VCC_CORE [46,47,48]

Follow CFL-H Power Map 6 + 2 45W 80A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

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Size	Document Number	Rev
Custom	CFL 6/7 (POWER&GND)	1A

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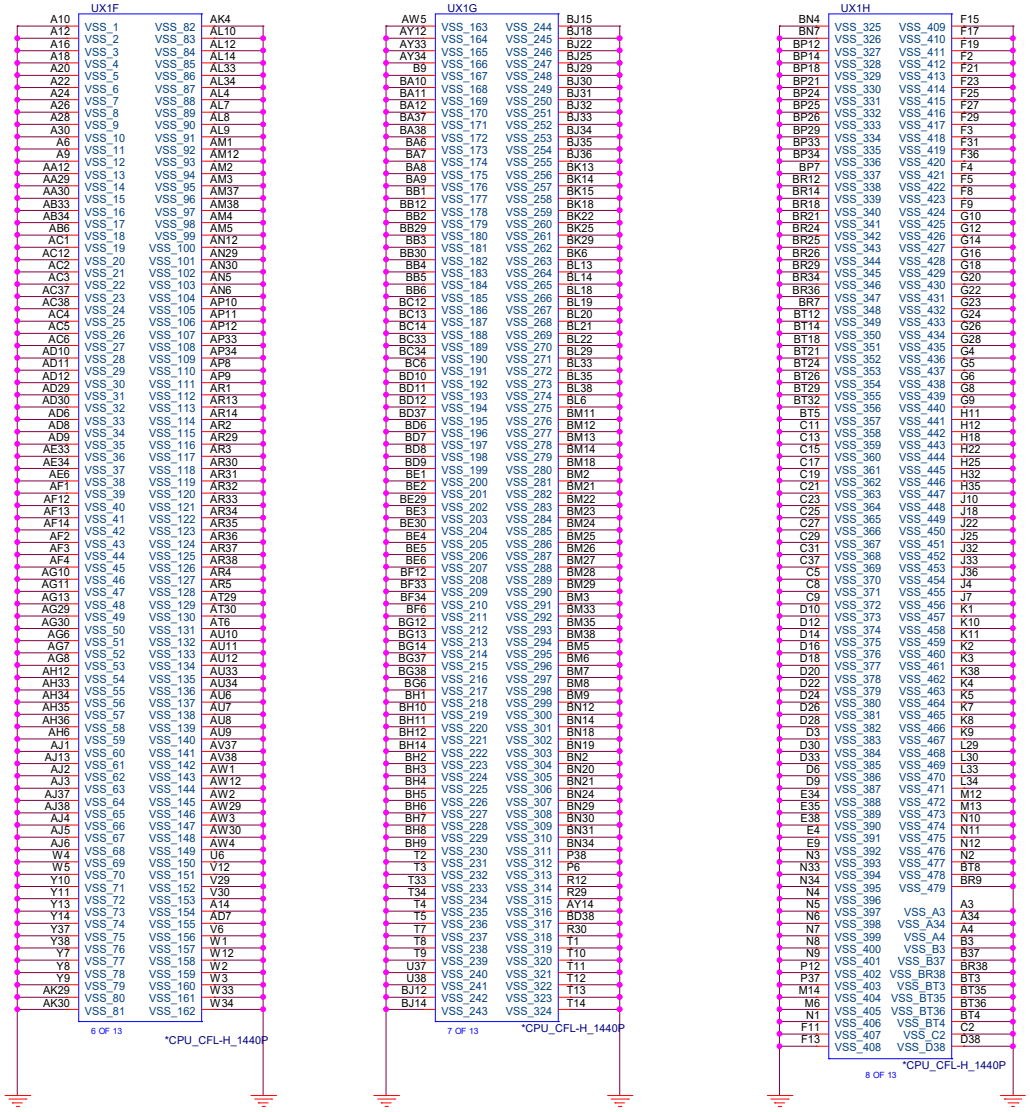

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Size	Document Number	Rev
Custom	CFL 7/7 (GND)	1A

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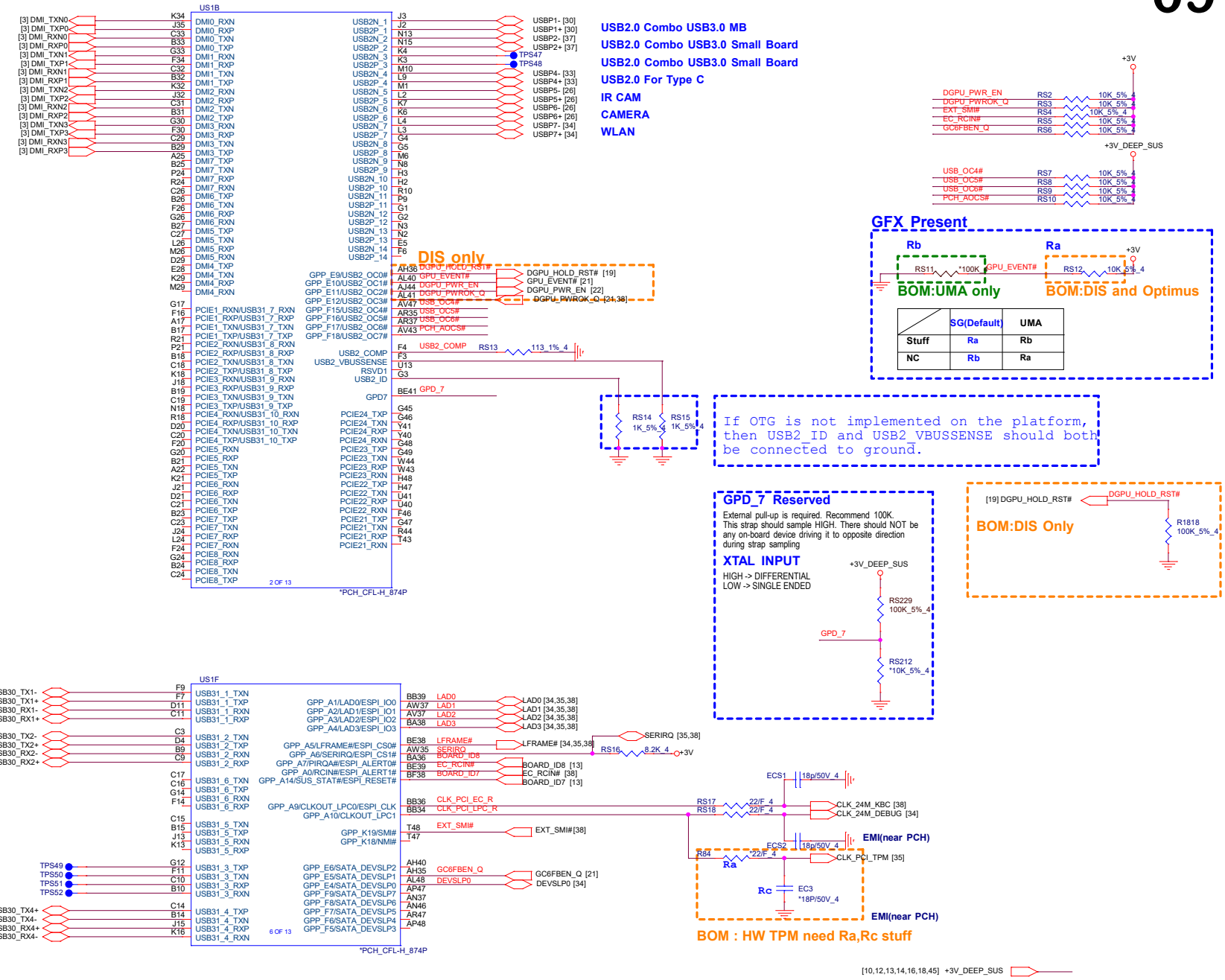
USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB-1
PORT3	NC
PORT4	USB2.0 For Type C
PORT5	IR CAM
PORT6	CAMERA
PORT7	WLAN
PORT8	NC
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB-1
PORT3	NC
PORT4	USB Typec w/o TBT



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Size: Custom	Document Number: PCH 1/7 (DMI/USB/PCIE)	Rev: 1A
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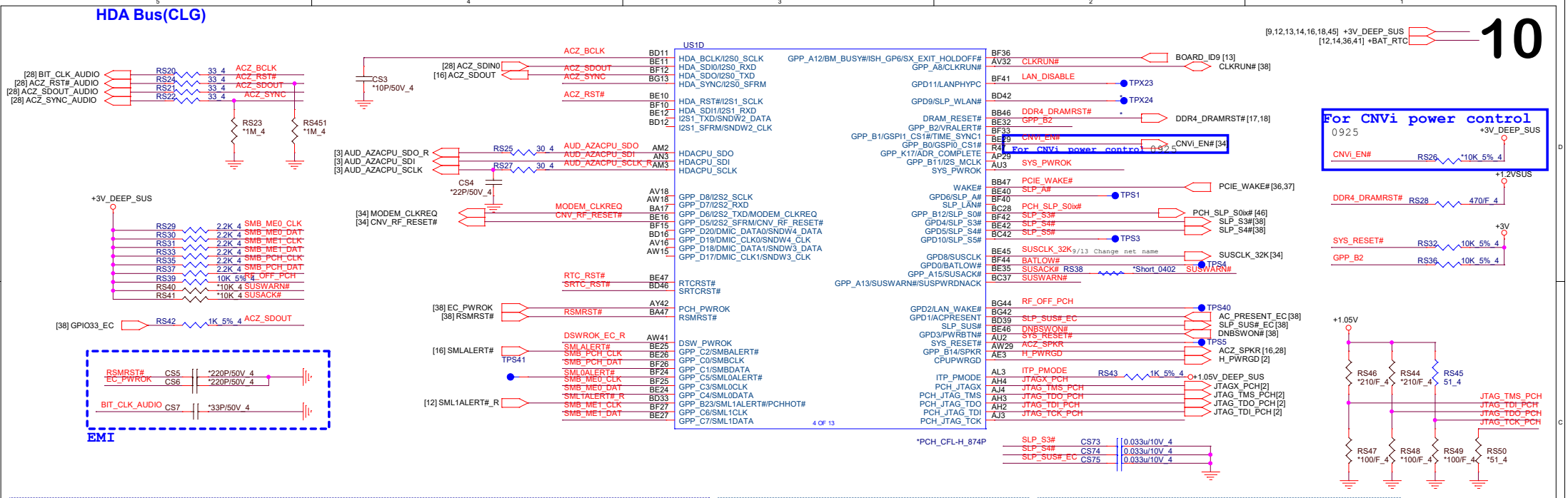
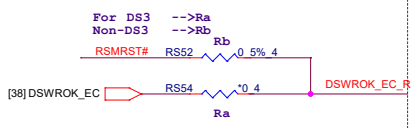
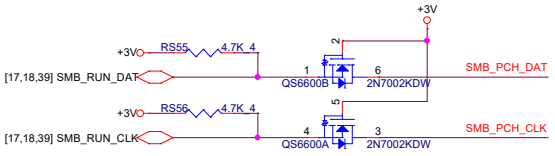
HDA Bus(CLG)



System PWR_OK(CLG)

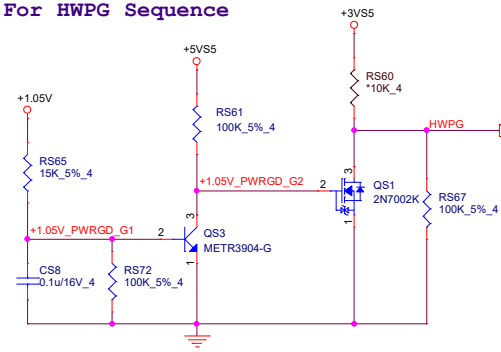
For DS3 Sequence

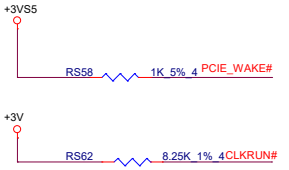




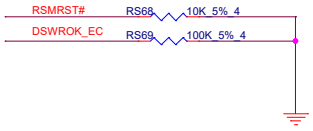
Touch Pad
XDP
DDR4

For HWPG Sequence

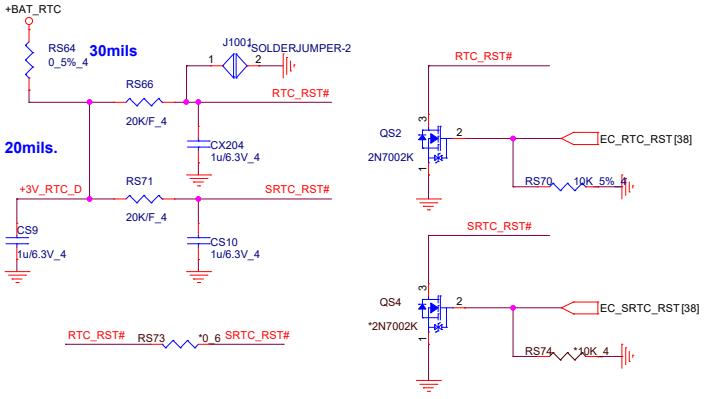


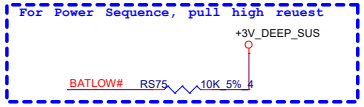


For Power Sequence.



RTC Circuitry(RTC)





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Size	Document Number	Rev
Custom	PCH 2/7 (HDA/SMBUS)	1A
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HSIO MUX PORT	
PCIE1-4	NC
PCIE5	NC
PCIE6	NC
PCIE7	NC
PCIE8	NC
PCIE9	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	LAN
PCIE15	Wlan
PCIE16	Cardreader
PCIE17	HDD1
PCIE18-20	NC

US1C

SSD PCIE x4 LANE

SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE

WLAN

CardReader

LAN

HDD1 (SATA2 6Gb/s)

SSD PCIE x4 LANE

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

For SSD Det (SATA0A)

BOM:SSD only

*PCH_CFL-H_874P

Please follow Intel CFL-H DG 571391 to meet Layout Requirment
"12.3.224 MHz Input Clock Routing Guidelines"

Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace

H_PECI (50ohm)
Trace Length: <0.5 iches
Ra,Ca need placement close to PCH.

US1G

LAN

WLAN

Card Reader

VGA

SSD

BOM:DIS only

BOM:SSD only

RTC Clock 32.768KHz

RS197 RS198 for Debug used.
Please do not change to Short pad

LS1

Close to PCH

PROJECT : NLA
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Size	Document Number	Rev
Custom	PCH 3/7 (SATA/LPC/CLK)	1A

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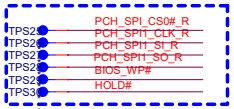
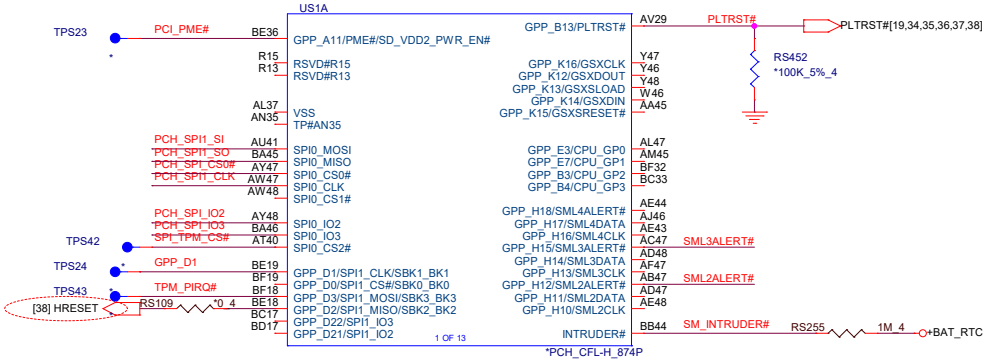
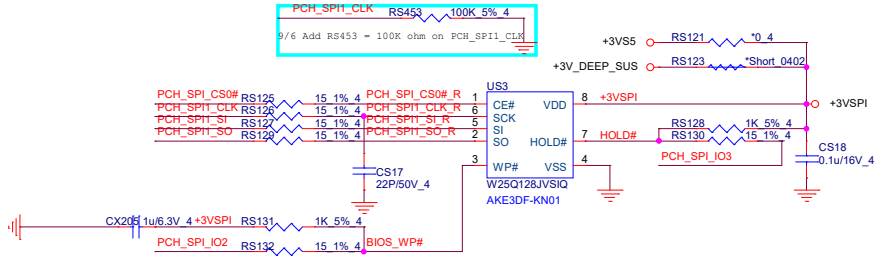
PCH SPI ROM(CLG)



Place to TOP



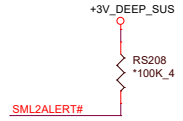


8/22 Update ROM parts list

Vender	Size	P/N
MAX	16MB	AKE3DZN0Z03 (MX25L12873FM2I-10G)
Winbond	16MB	AKE3DF-KN01 (W25Q128JVSIQ)
GigaDevice	16MB	AKE3DZN0Q02 (GD25B127DSIGR)
Socket		DFHS08FS023 (DG008000011)

ESPI FLASH SHARING MODE

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



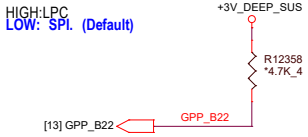
Pin Straps (Sheet 2 of 4)

Signal	Usage	When Sampled	Comment
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6: 0 = SPI (Default); 1 = LPC. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected (for EC). (Default) 1 = eSPI is selected (for EC). Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H15 / SML3ALERT#	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

BOOT SELECT STRAP

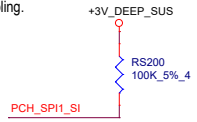
This Signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6).

HIGH:LPC
LOW: SPI. (Default)



RESERVED

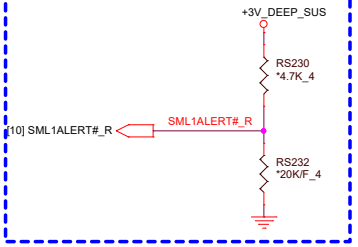
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



10/5 Del +1.8V_DEEP_SUS PULL HIGHT

RESERVED

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB



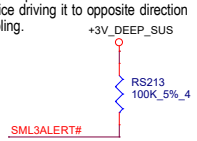
ESPI/LPC SELECT STRAP

HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)

10/5 Del

RESERVED

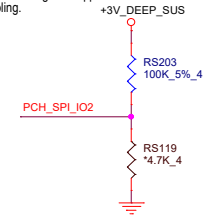
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



10/5 Del +1.8V_DEEP_SUS PULL HIGHT

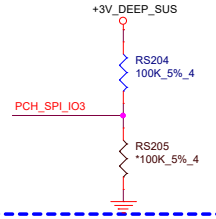
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



[9,10,12,14,16,18,45] +3V_DEEP_SUS

US1M

GPP_G0/SD_CMD
GPP_G1/SD_D0
GPP_G2/SD_D1
GPP_G3/SD_D2
GPP_G4/SD_D3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP

GPP_I11/M2_SKT2_CFG0
GPP_I12/M2_SKT2_CFG1
GPP_I13/M2_SKT2_CFG2
GPP_I14/M2_SKT2_CFG3

CNV_WR_CLKN / CNV_WR_CLKP
CNV_WR_D0N / CNV_WR_D0P / CNV_WR_D1N / CNV_WR_D1P
CNV_WT_CLKN / CNV_WT_CLKP
CNV_WT_D0N / CNV_WT_D0P / CNV_WT_D1N / CNV_WT_D1P
CNV_WT_RCOMP

For C10
CPU_VCCIO_PWR_GATE#

GPP_J0/CNV_PA_BLANKING
GPP_J1/CPU_VCCIO_PWR_GATE#
GPP_J11/A4WP_PRESENT
GPP_J10
GPP_J_2
GPP_J_3
GPP_J_4 CNV_BRI_DT_UART0_RTSB
GPP_J5/CNV_BRI_RSP/UART0_RXD
GPP_J6/CNV_RGI_DT/UART0_TXD
GPP_J7/CNV_RGI_RSP/UART0_CTS#
GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD

PCIECOMP_N / PCIECOMP_P
SD_RCOMP_1P8 / SD_RCOMP_3P3
GPPJ_RCOMP_1P81 / GPPJ_RCOMP_1P82 / GPPJ_RCOMP_1P83
RSVD2 / RSVD3
RSVD#BC1

RS139 100_1%_4
RS141 200_1%_4
RS142 200_1%_4
RS143 200_1%_4
RS140 150_1%_4

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*PCH_CFL-H_874P

[16,34] CNV_BRI_DT
[34] CNV_BRI_RSP
[16,34] CNV_RGI_DT
[34] CNV_RGI_RSP
[16] GPP_J9

CNV_BRI_RSP RS456 20K_4
CNV_RGI_RSP RS457 20K_4
+1.8V_DEEP_SUS

US1K

GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS0#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS0#

GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#

GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD

GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD

GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA

GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SPK4_BK4
GPP_D23/ISH_I2C2_SCL/I2C3_SCL

GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_D16/ISH_UART0_CTS#/CNV_WCEN
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D13/ISH_UART0_RXD/I2C2_SDA

GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA

GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7

*PCH_CFL-H_874P

[12] GPP_B22
[38] PCI_SERR#
RS135 100_5%_4
GPP_B22
PCI_SERR#_R

[17,18] PM_EXTTS#0
TPS55
[39] TP_INTH#
RS136 *0_4
PM_EXTTS#0_R
EXTTS#1
TP_INTH#

[38] SIO_EXT_SCI#
SIO_EXT_SCI#
TPS44 ACCEL_INTA#
TPS37 UART2_TXD
TPS38 UART2_RXD

[39] I2C1_SCL
[39] I2C1_SDA

TPS56
TPS57
ACC_LED#
SPK_ID
BT_OFF

	Codec Output
GPIO	GPP_D11
	SPK_ID
Definition	Hi : SABLE
	Low : VECO

BOARD_ID6
BOARD_ID5
BOARD_ID4
BOARD_ID3
BOARD_ID2
BOARD_ID1
BOARD_ID0

+3V_DEEP_SUS

ACC_LED# RS144 10K_5%_4
BT_OFF RS145 10K_5%_4
SPK_ID RS148 10K_5%_4
TCH_PNL_INT#_R RS151 10K_5%_4
SIO_EXT_SCI# RS154 10K_5%_4
UART2_TXD RS137 49.9K/F_4
UART2_RXD RS138 49.9K/F_4

For C10
+1.8V_DEEP_SUS
+3V_DEEP_SUS
R12464 100K/F_4
R12465 100K/F_4
Q9078 DMG1012T-7
CPU_VCCIO_PWR_GATE#
PWR_GATE#
PWR_GATE# [45]
RS455 *2.2K_4

+3V_DEEP_SUS

R222 *10K_4 BOARD_ID0 R223 10K_4
R224 *10K_4 BOARD_ID1 R225 10K_4
R228 *10K_4 BOARD_ID2 R229 10K_4
R231 10K_4 BOARD_ID3 R232 *10K_4
R233 10K_4 BOARD_ID4 R234 *10K_4
R235 *10K_4 BOARD_ID5 R236 10K_4
R237 10K_4 BOARD_ID6 R238 *10K_4
R239 *10K_4 BOARD_ID7 R240 10K_4
R241 10K_4 BOARD_ID8 R242 *10K_4
R124572 10K_4 BOARD_ID9 R124571 *10K_4

G1
G0

BOARD_ID7 [9]
BOARD_ID8 [9]
BOARD_ID9 [10]

NLA Board ID

Model	BOARD_ID[9]	BOARD_ID[8]	BOARD_ID[7]	Board ID [4]	Board ID [3]	BOARD_ID[2:1]	BOARD_ID[6:5:0]
	ID9	ID8	ID7	ID4	ID3	ID2;ID1	ID6:ID5:ID0
Definition	0 : Normal CAM 1 : IR CAM	0 : Normal CPU 1: Turbo CPU	0 : LG Customer 1: None LG Customer	Reserve Default = 0	Reserve Default = 0	00 : Reserve 01 : Reserve 10 : N17P-G1 (150W) 11 : N17P-G0 (120W)	000 : NL5 C 001 : NL5 T 010 : NL5 U 011 : NL A 100 : NL9 U

PCI_SERR# RS165 10K_5%_4
TCH_PNL_INT#_R RS168 10K_5%_4
+3V

Reserve EDP_HPD opposites circuit!

+3V
RS177 *10K/F_4
CPU_EDP_HPD
RS179 100K_5%_4

HPD0 ---> mDP
HPD1 ---> Type-C DP
HPD2 ---> HDMI

US1E

TPS46
TypeC1_DDI1_HPD_Q
DP_HPD_PCH_Q
HDMI_HPD_Q

GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DPPD_HPD2/DISP_MISC2
GPP_I3/DPPE_HPD3/DISP_MISC3
GPP_I4/EDP_HPD/DISP_MISC4

GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F23/DDPF_CTRLDATA
GPP_F22/DDPF_CTRLCLK
GPP_F14/EXT_PWR_GATE#/PS_ON#
GPP_K23/IMGCLKOUT1
GPP_K22/IMGCLKOUT0
GPP_K21
GPP_K20
GPP_H23/TIME_SYNC0

DDPC_CTRLDATA
SDVO_DATA
DDPC_CTRLDATA
SKTOCC_N_R

[26] CPU_EDP_HPD
CPU_EDP_HPD
SKTOCC_N_R [2]

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*PCH_CFL-H_874P

GPP_I6 / DDPB_CTRLDATA:
This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

GPP_I8 / DDPC_CTRLDATA:
This signal has a weak internal Pull-down.
0 = Port C is not detected. (Default)
1 = Port C is detected.

GPP_I10 /DDPD_CTRLDATA:
This signal has a weak internal pull-down.
0 = Port D is not detected. (Default)
1 = Port D is detected.

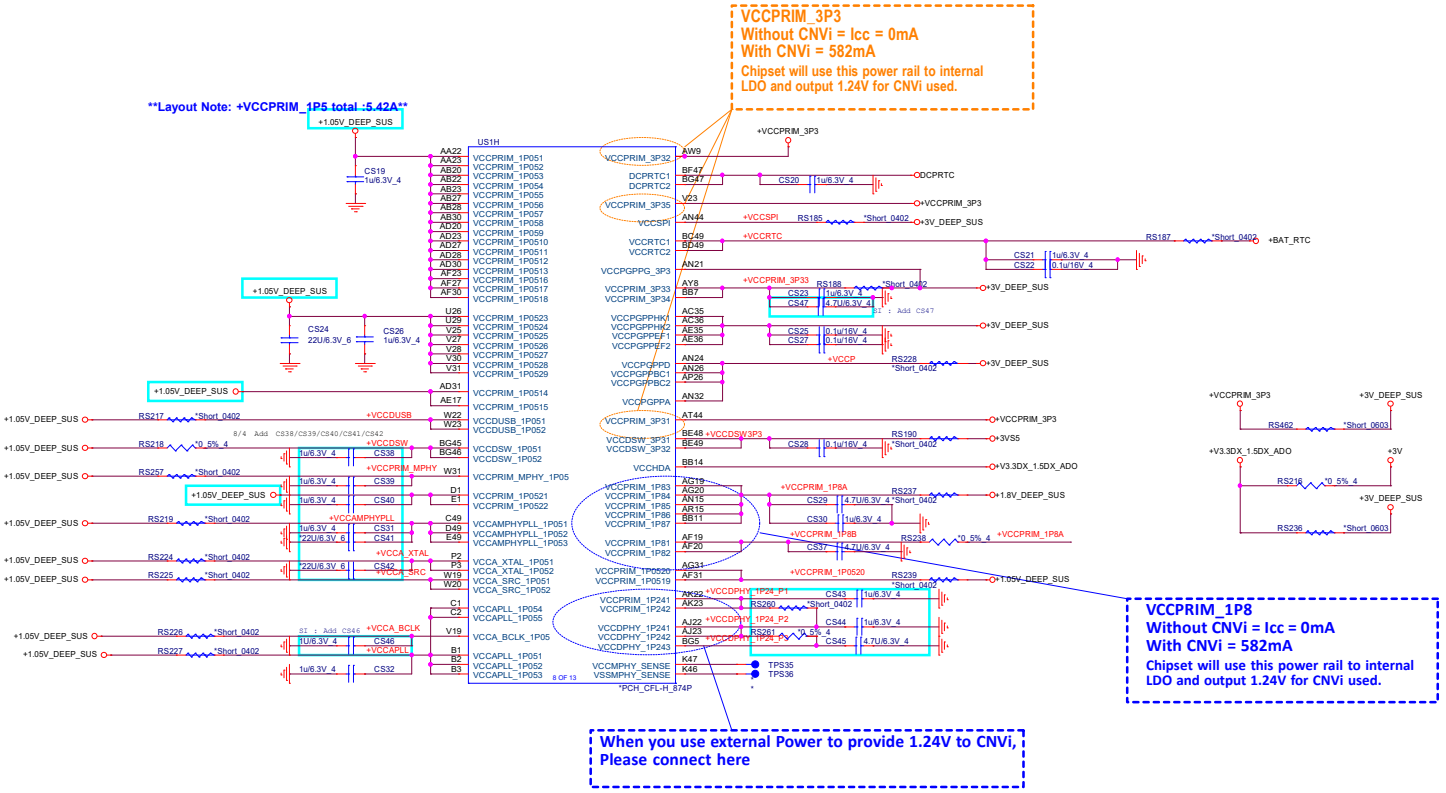
+3V
SDVO_DATA RS172 *2.2K_4
DDPC_CTRLDATA RS175 2.2K_4
DDPD_CTRLDATA RS178 *2.2K_4

+3V
RS459 1M_5%_4
8/3 QS5 swpa 1,3 pin
[31,32] TypeC1_DDI1_HPD
RS458 *Short_0402
QS5 2N7002K
TypeC1_DDI1_HPD_Q
[31] TypeC1_DDI1_HPD_R
TypeC1_DDI1_HPD_R RS259 *0_5%_4 TypeC1_DDI1_HPD_Q

+3V
RS461 1M_5%_4
[21,27] HDMI_HPD
QS7005 2N7002K
HDMI_HPD_Q

PROJECT : NLA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/7 (GPIO)	1A
Date: Monday, April 09, 2018	Sheet 13 of 56	

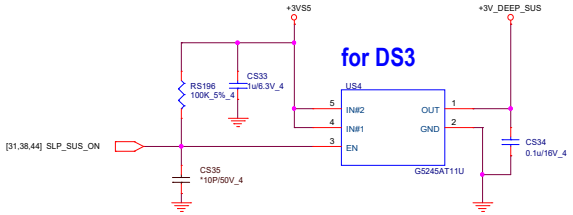


Please follow below table to check Layout

Table 10-4. PCH-H Estimated I_{cc}[3] with Integrated 1.8V VRM Mode OFF (H Mobile SKUs)

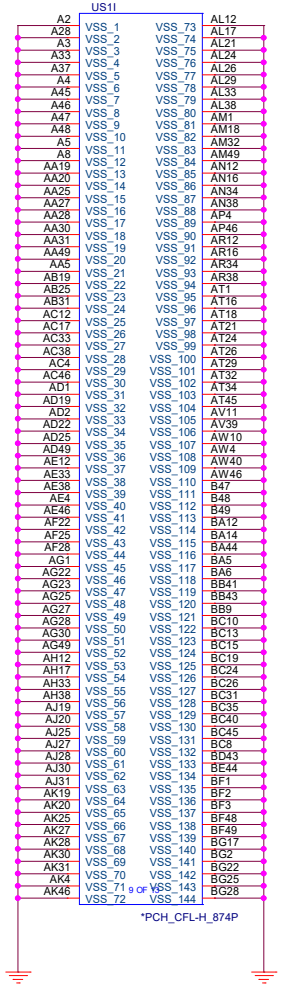
Voltage Rail	Voltage (V)	S0 Iccmax Current[2] (A)	Sx Icc Idle Current[4] (mA)	S0ix Icccmax Current (mA).	Deep Sx Icc Idle Current (mA)	G3 (µA)
VCCAPLL_1P05	1.05	0.034	0.2	0.801	0	0
VCCA_BCLK_1P05	1.05	0.007	0.1	0.087	0	0
VCCA_SRC_1P05	1.05	0.141	0.3	0.838	0	0
VCCA_XTAL_1P05	1.05	0.005	0.544	0.195	0	0
VCCAMPHYPLL_1P05	1.05	0.114	0.4	1.192	0	0
VCCPRIM_1P05	1.05	4.174 HSIO Lane Adder refer to Table 10-7 column HALO	40.344	0.477A	0	0
VCCPRIM_MPHY_1P05	1.05	0.088	0.2	1.22	0	0
VCCDSW_1P05	1.05	0.01	0.2	0.001	0.2	0
VCCDUSB_1P05	1.05	0.33	1.288	16.373	0	0
VCCHDA	3.3	0.007	0.1	4.908	0	0
VCCDSW_3P3	3.3	0.094	0.2	0.705	1.05	0
VCCPRIM_3P3	3.3	0.318	0.3	0.916	0	0
VCCPGPPA	3.3	0.085	0.1	0.103	0	0
VCCPGPPBC	3.3	0.286	0.2	0.232	0	0
VCCPGPPD	3.3	0.117	0.1	0.109	0	0
VCCPGPPEF	3.3	0.145	0.2	0.094	0	0
VCCPGPPG_3P3	3.3	0.121	0.1	0.072	0	0
VCCPGPPHK	3.3	0.219	0.2	0.138	0	0
VCCPRIM_1P8	1.8	0.152 CNVi Adder refer to Table 10-8, column HALO	6.607	9.411	0	0
VCCRTC[1]	3.0	0.31mA	0.299	0.075	0.316	6
VCCSPI	3.3	0.042	0.1	0.153	0	0

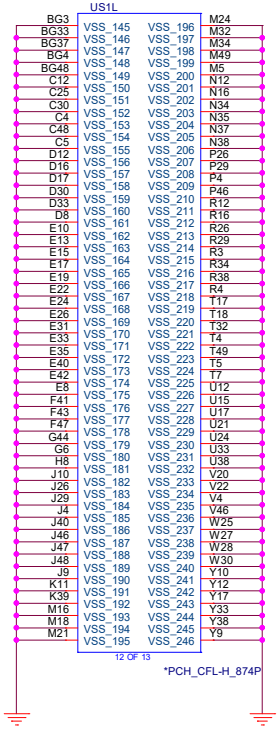
Notes:
1. The VCC rail ICC data is taken at 3.0V while the system is in a mechanical off (G3) state at room temperature.
2. Iccmax estimates assumes 110 °C.
3. The Iccmax value is a steady state current that can happen after respective power ok has asserted (or reset signal has de-asserted).
4. Sx Icc Idle assumes PCH is idle and ME is power gated.
5. Sx Icc at 3.3V level is assumed. Sx Icc data at the 1.8 V and/or 1.5V level not measured.

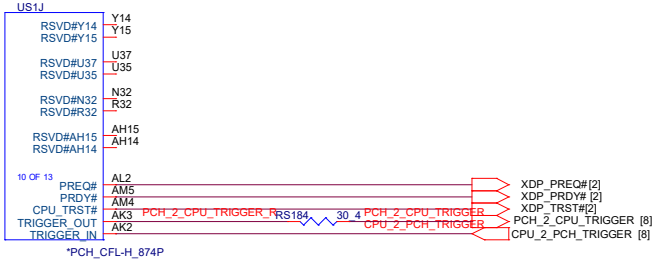


[10,12,36,41] +BAT_RTC
[9,10,12,13,16,18,45] +3V_DEEP_SUS

PROJECT : NLA
Quanta Computer Inc.
Size: Custom | Document Number: PCH 6/7 (POWER) | Rev: 1A
Date: Monday, April 09, 2018 | Sheet 14 of 56







PROJECT : NLA

Quanta Computer Inc.

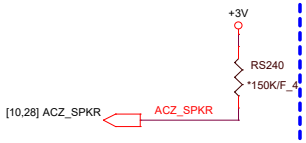
Size	Document Number	Rev
Custom	PCH 7/7 (GND)	1A
Date: Monday, April 09, 2018	Sheet 15 of 56	

Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

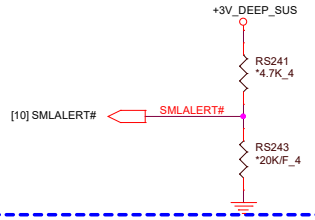
TOP SWAP OVERRIDE STRAP

The signal has a weak internal pull-down.
0 = Disable " Top Swap" mode (Default)
1 = Enable " Top Swap" mode. This inverts an address



TLS CONFIDENTIALITY ENABLED

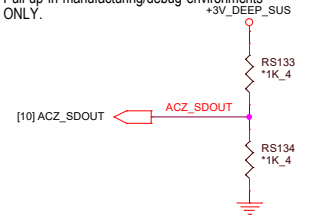
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.



NO REBOOT IF SAMPLED HIGH

The signal has a weak internal pull-down.
0 = Disable " No Reboot" mode (Default)
1 = Enable " No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.



Pin Straps (Sheet 3 of 4)

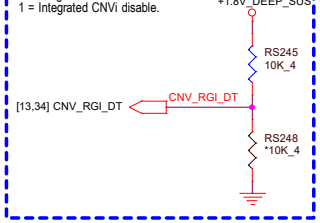
Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)**
GPP_I6 / DDPB_C-TRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_C-TRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

Pin Straps (Sheet 4 of 4)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

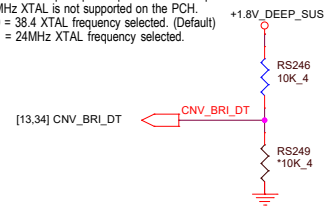
M.2 CNVi Mode Select

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.



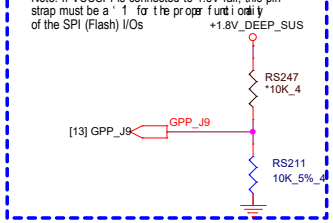
XTAL Frequency Select

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.



GPP_J9 1.8V VCCPSPI:

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a ' 1 ' for the proper functionality of the SPI (Flash) I/Os



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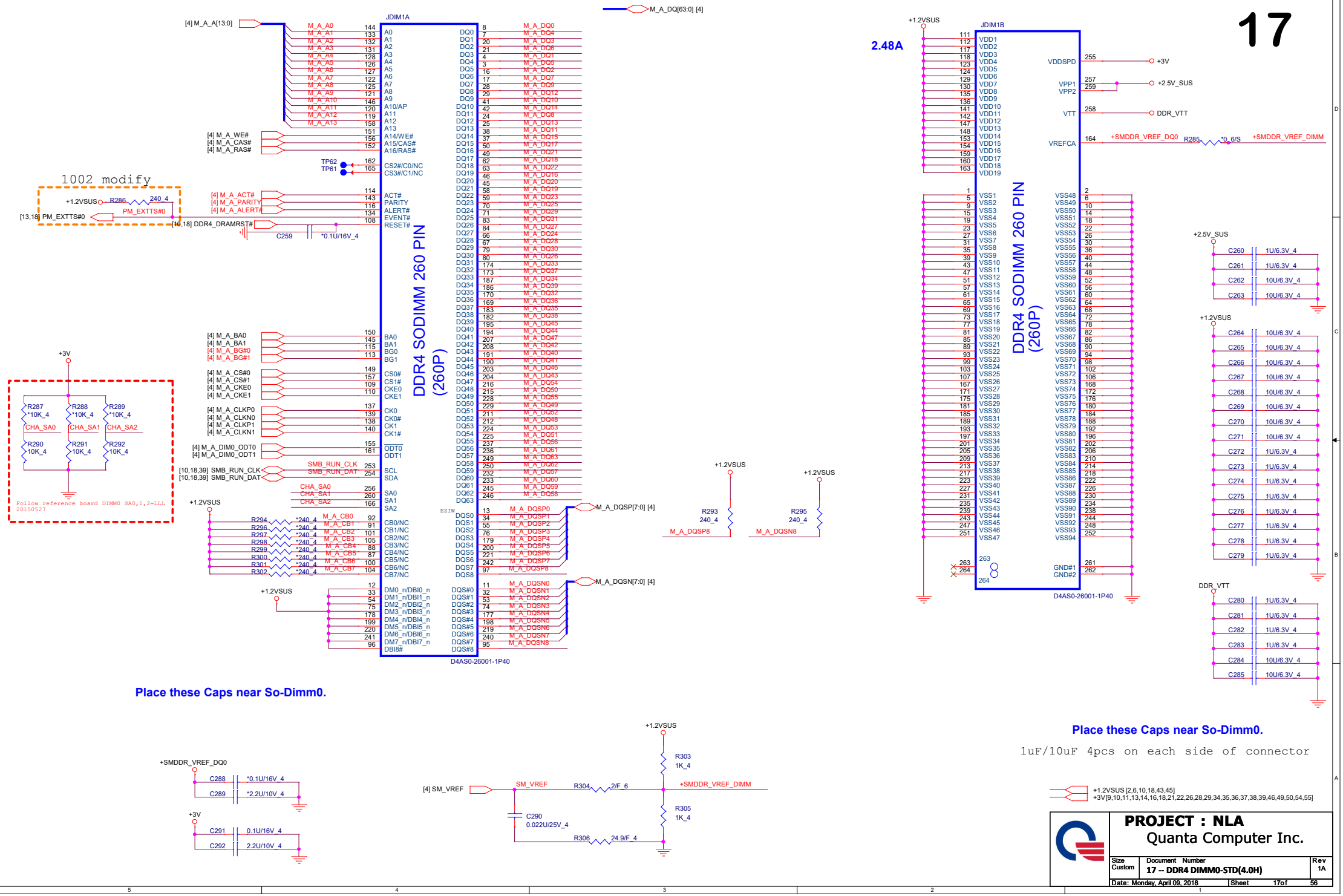

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Size: Custom	Document Number: 17 -- DDR4 DIMM0-STD(4.0H)
Rev:	1A
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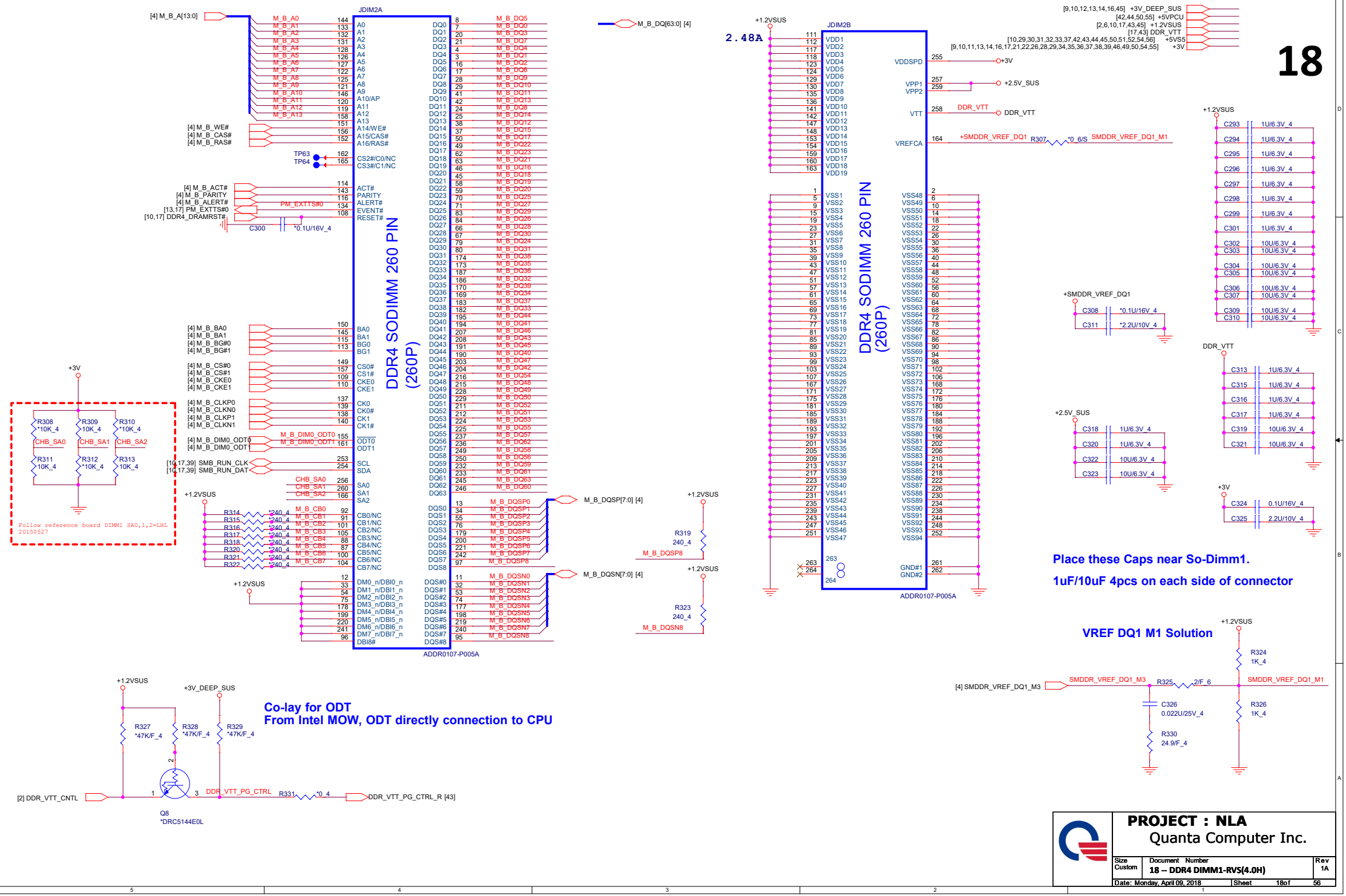

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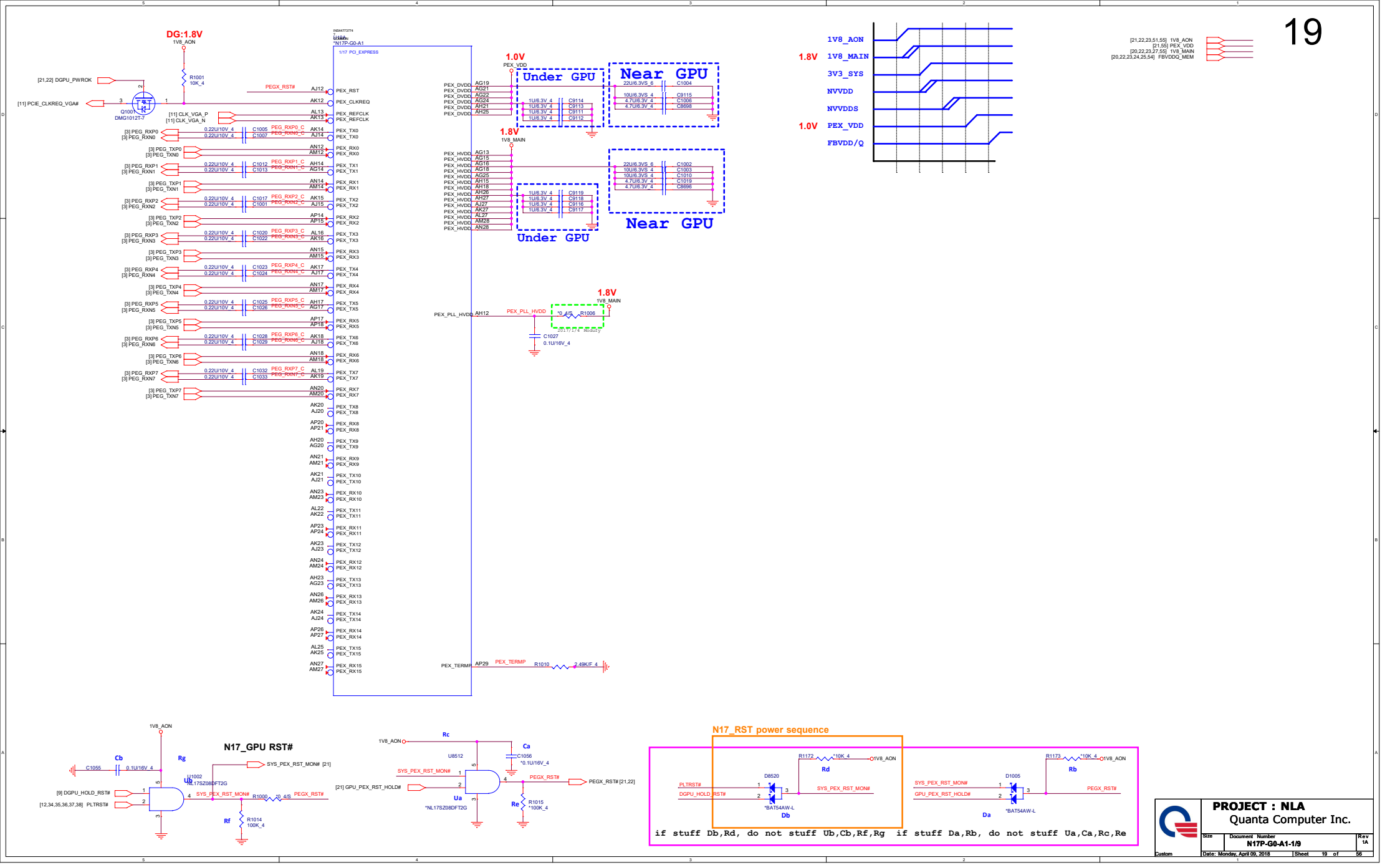

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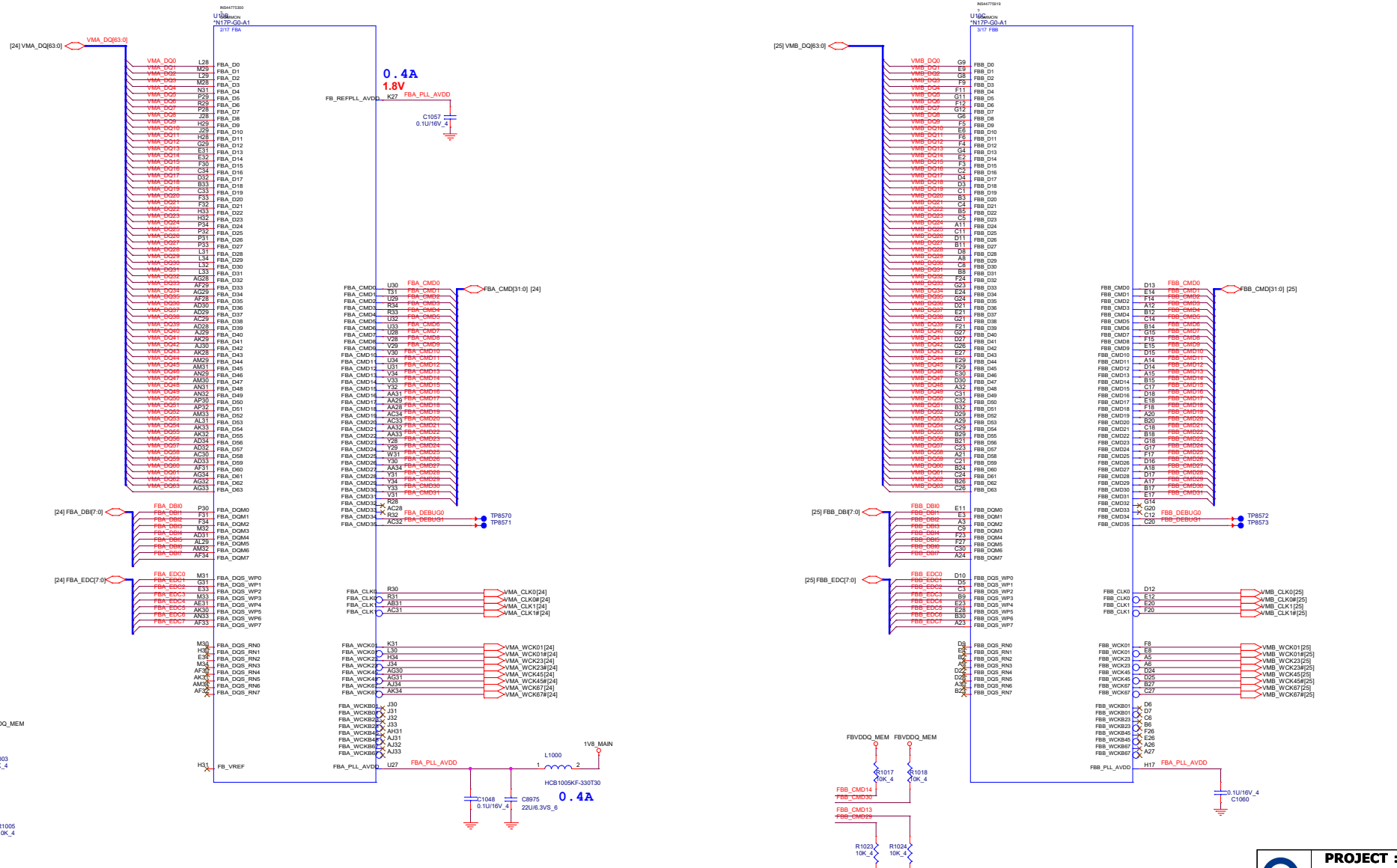
[19,22,23,27,55] 1V8_MAIN
[22,23,24,25,54] FBVDDQ_MEM



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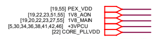


Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/ WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON

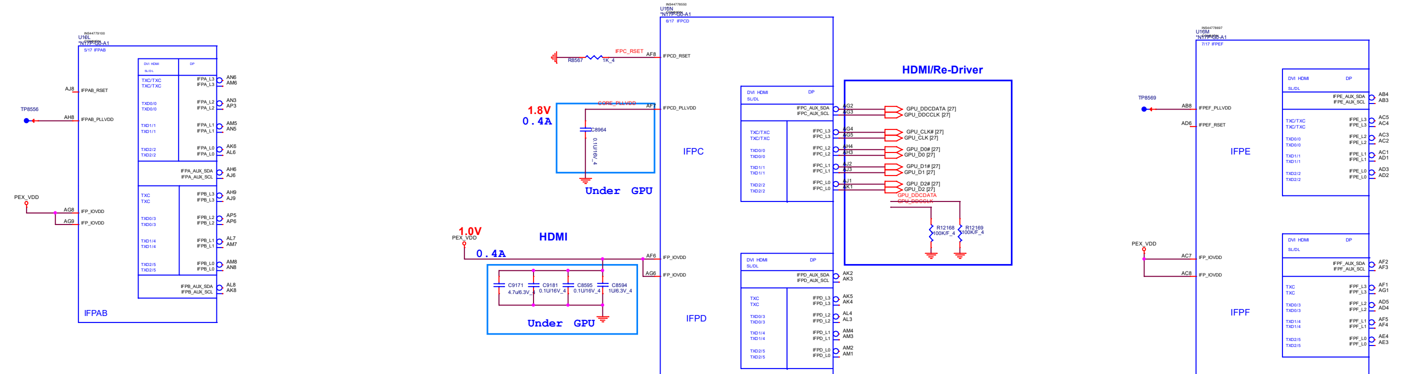
Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

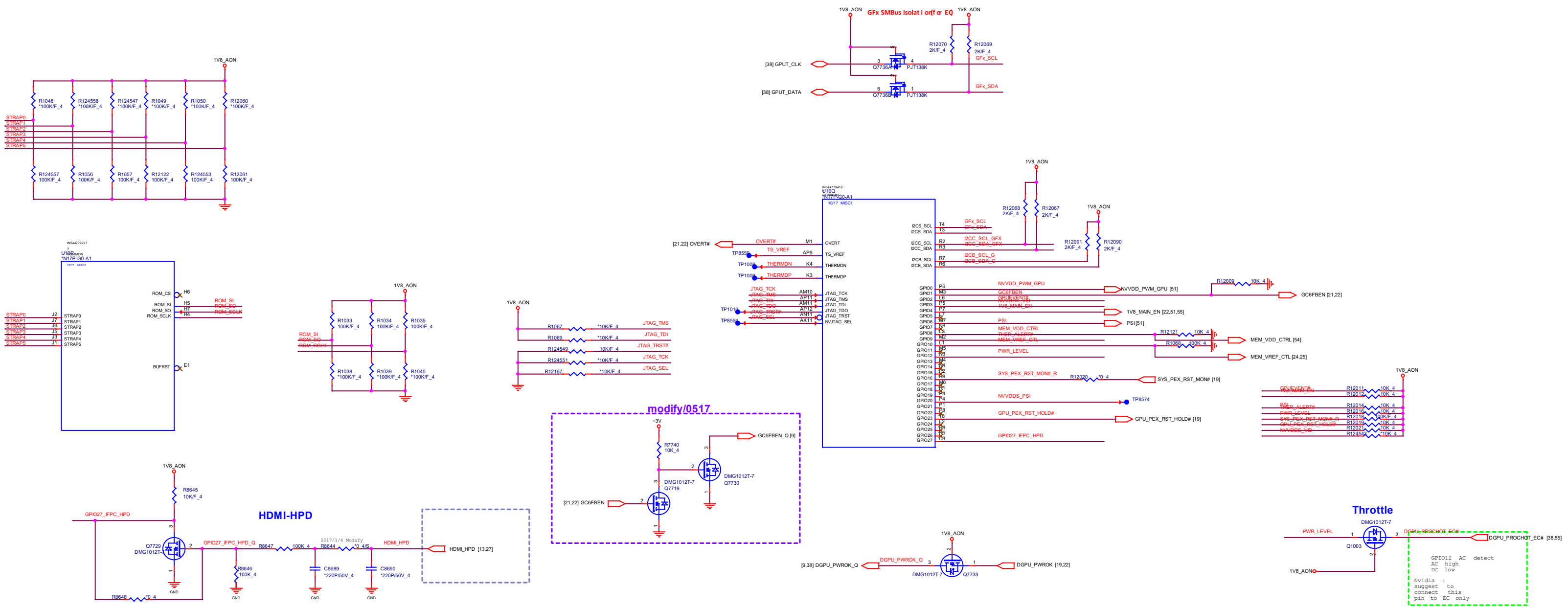
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GC6M: GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to a gated 3V3
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5

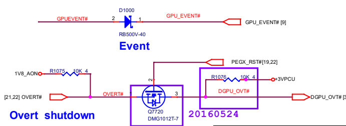
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON



STRAP[2:0] VRAM Table for N17P-G0/G1 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	Haier consign P/N	QB P/N	
0x0	GDDR5 256Mx32 8 GHz	Samsung B die	K4G80325FB-HC25	AKG58WWT505	AKD58WWT500	
0x2	GDDR5 256Mx32 8 GHz	Hynix M die	H5GQ8H24MJR-R4C	AKG5RF0TW03	AKD5RF0TW00	
0x0	GDDR5 256Mx32 7 GHz	Samsung B die	K4G80325FB-HC28	AKG5QGDT513	AKG5QGDT506	
0x2	GDDR5 256Mx32 7 GHz	Hynix M die	H5GC8H24MJR-R0C		AKG5QGUTW02	





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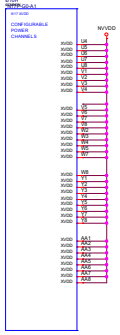
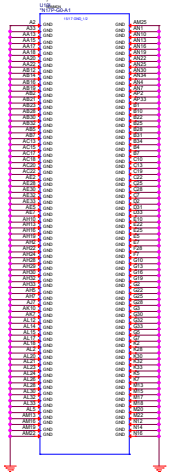
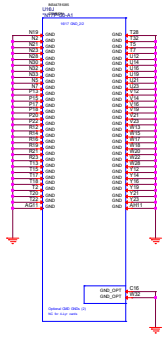
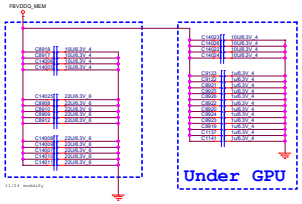


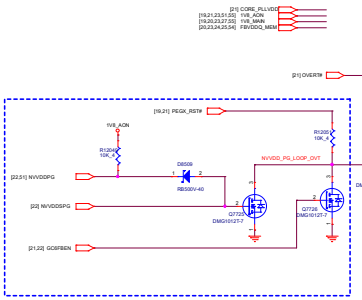




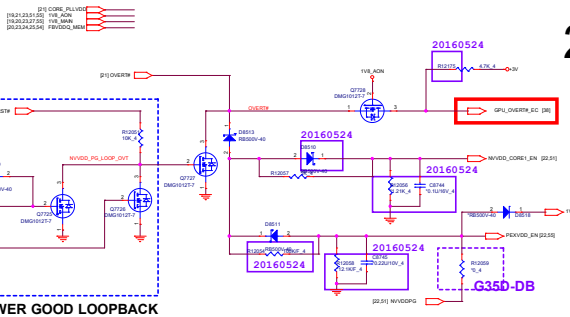
Near GPU



Under GPU

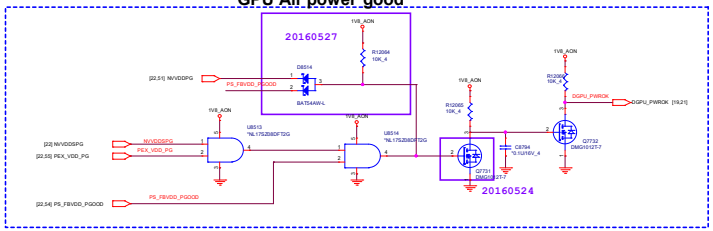


NVVDD POWER GOOD LOOPBACK

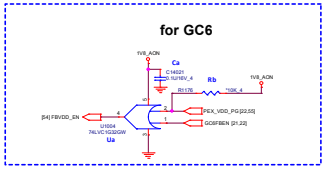


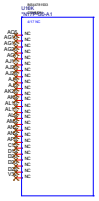
Overt temp ckt for NVVDD and NVVDDS

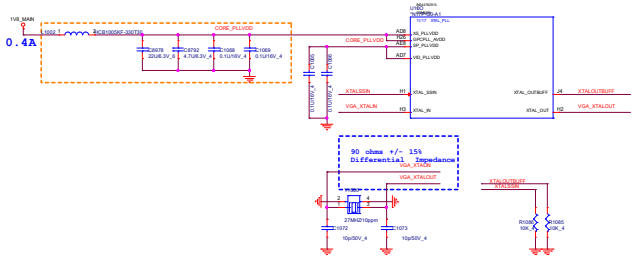
GPU All power good



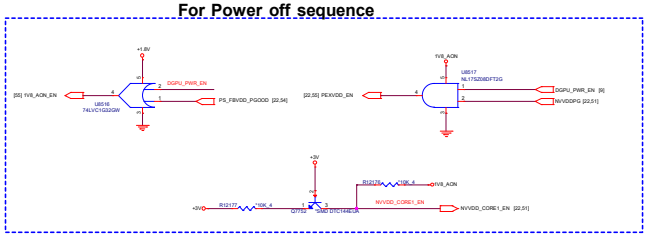
for GC6

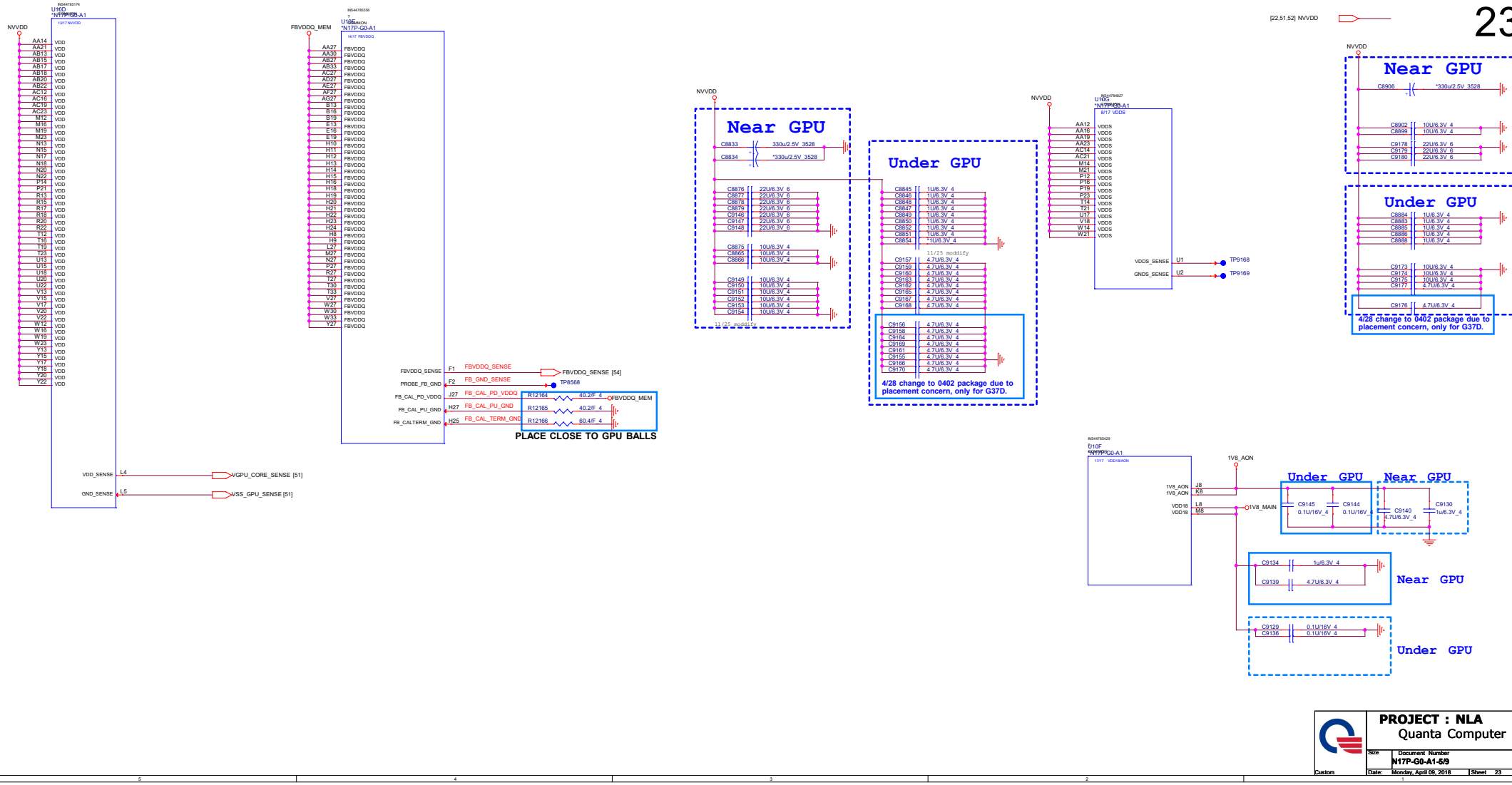






For Power off sequence





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CHANNEL A: 2G/4G GDDR5

[20,22,23,25,54] FBVDDQ_MEM

Channel 0 <0-31>

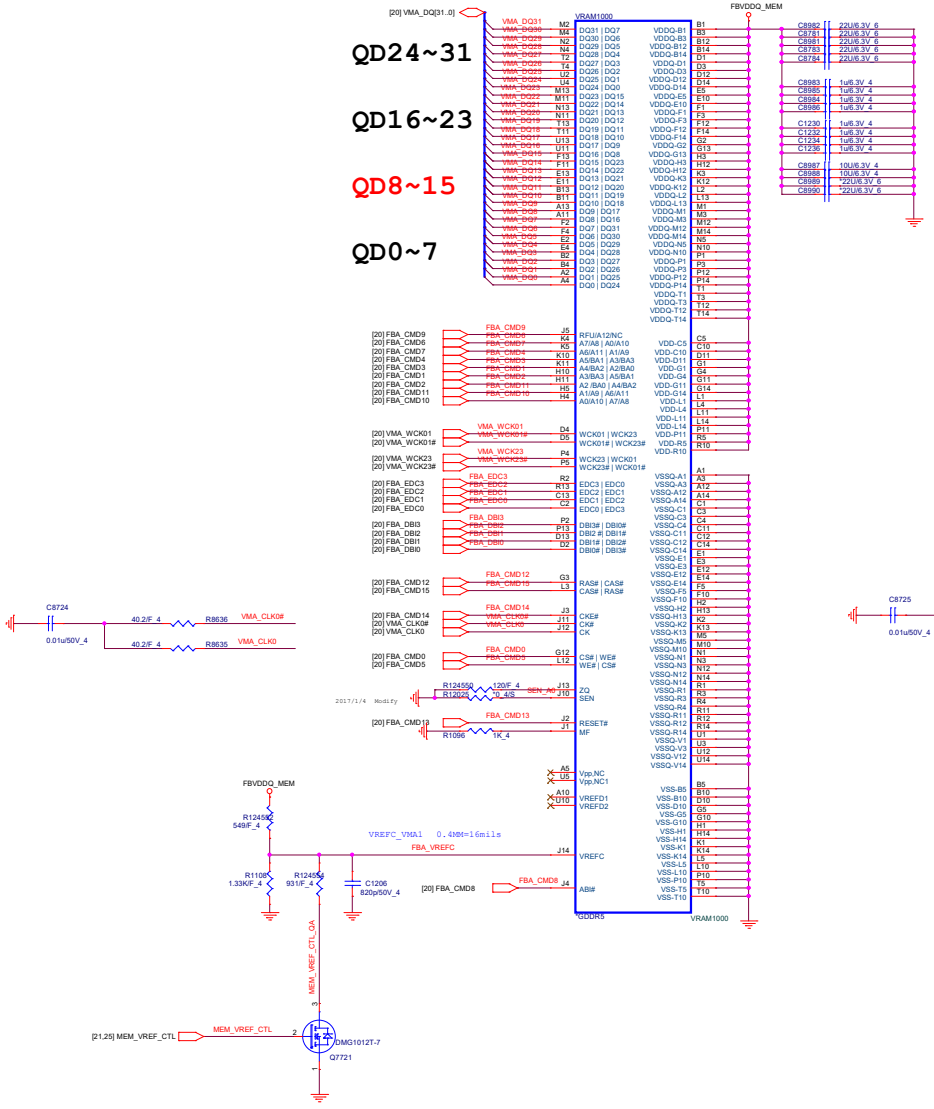
MF=0 Non-mirrored

QD24~31

QD16~23

QD8~15

QD0~7



Channel 1 <32-63>

MF=1 mirrored

QD32~39

QD40~47

QD48~55

QD56~63

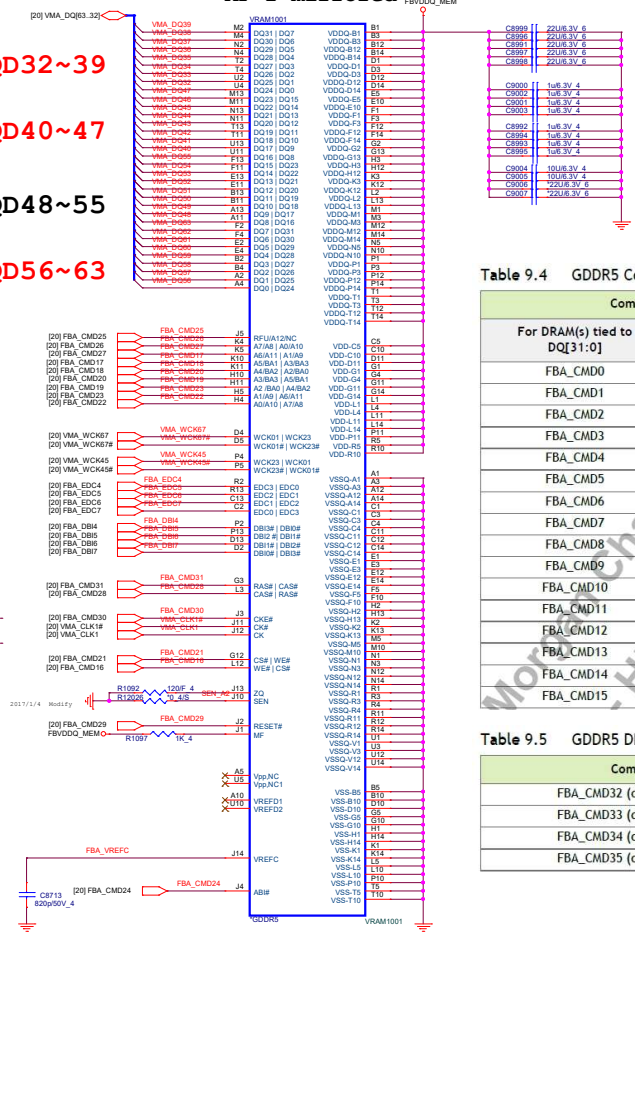


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

CHANNEL B: 2G/4G GDDR5

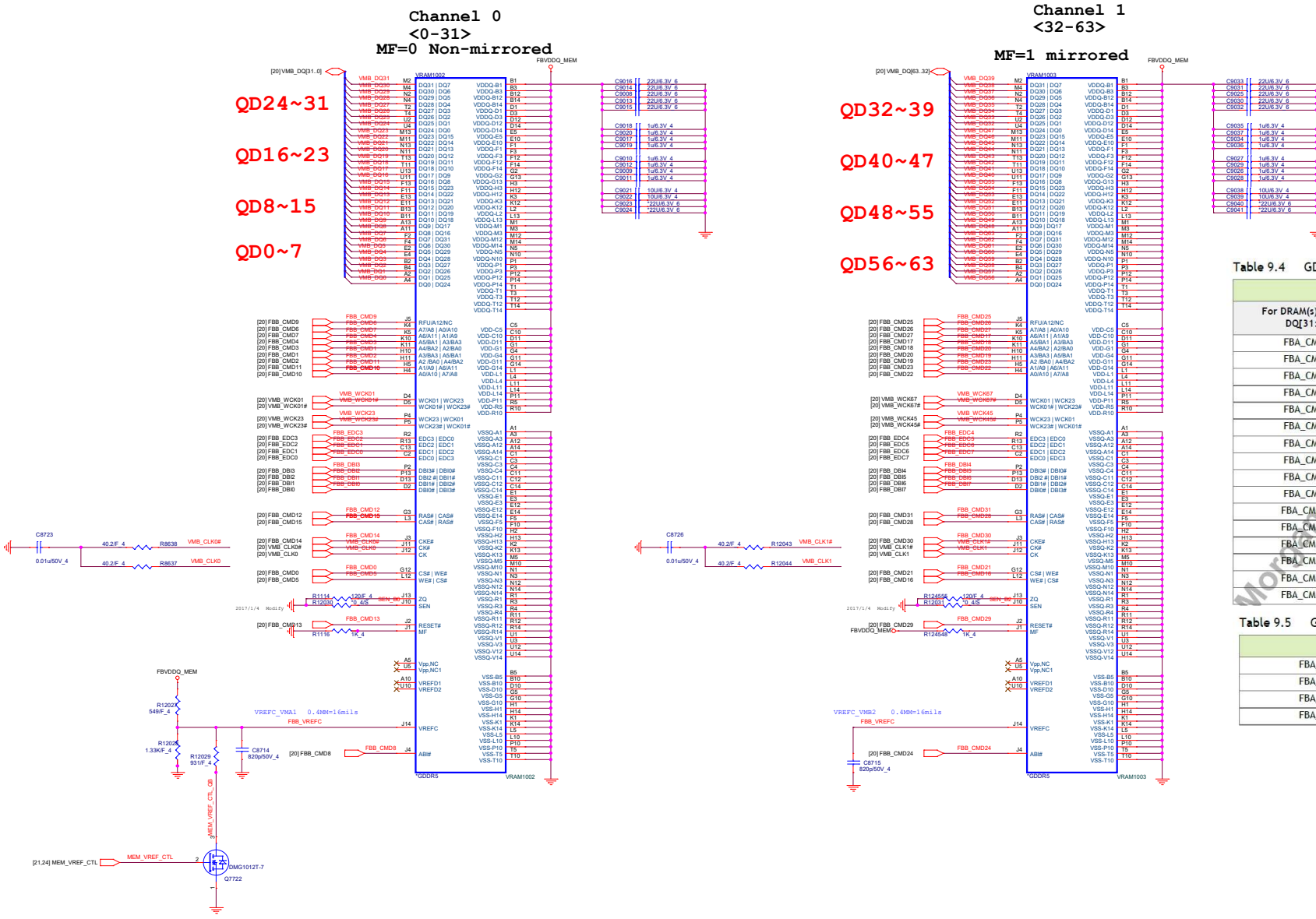


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
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FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

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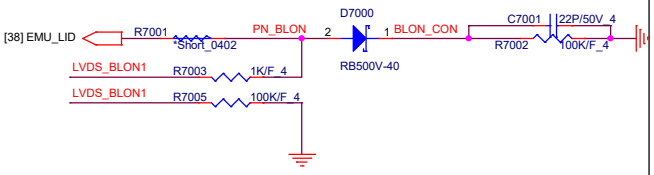
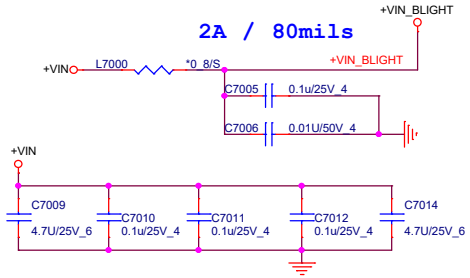
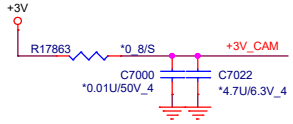
LID Switch





CAN

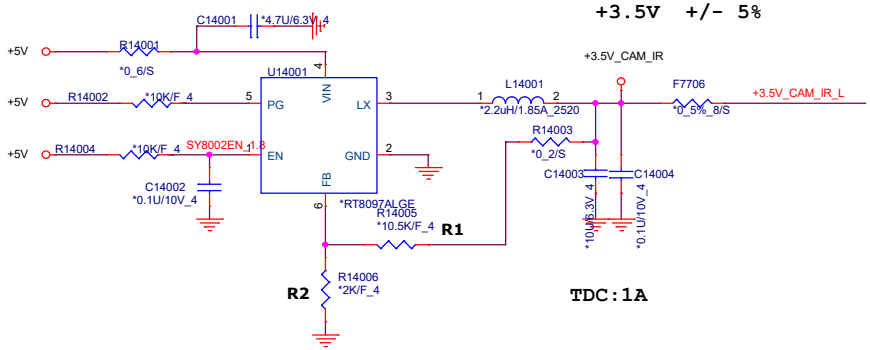


IR CAN

VO=(0.6(R1+R2)/R2)

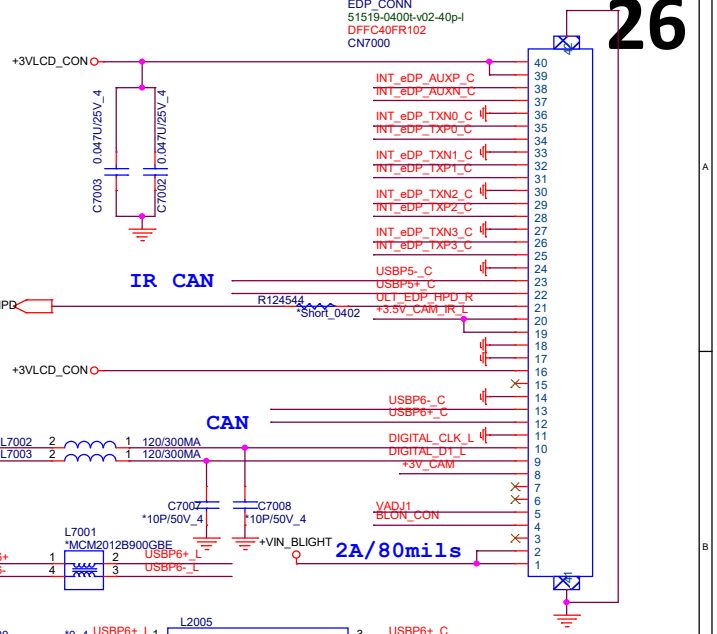
EDP:2A

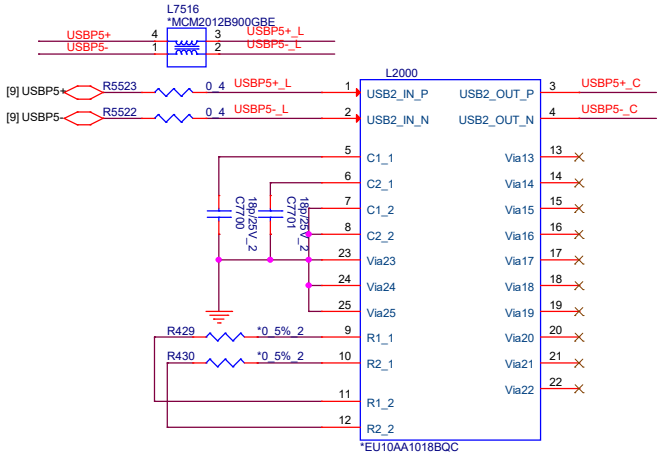
+3.5V +/- 5%

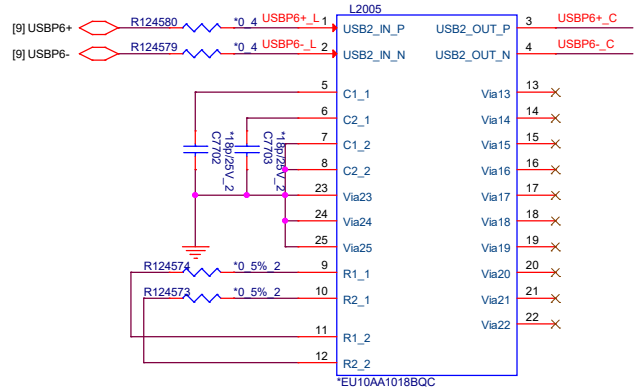


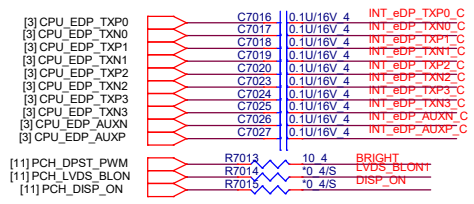
TDC:1A

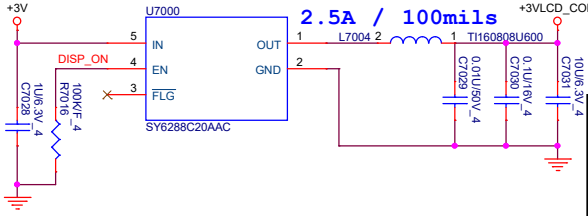
eDP Conn.

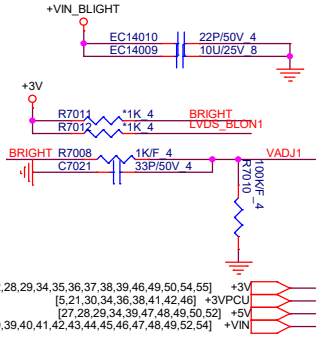












[9,10,11,13,14,16,17,18,21,22,28,29,34,35,36,37,38,39,46,49,50,54,55] +3V
[5,21,30,34,36,38,41,42,46] +3VPCU
[27,28,29,34,39,47,48,49,50,52] +5V
[29,39,40,41,42,43,44,45,46,47,48,49,52,54] +VIN

PROJECT : NLA
Quanta Computer Inc.

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Custom	LCD CONN/LID/CAM	1A
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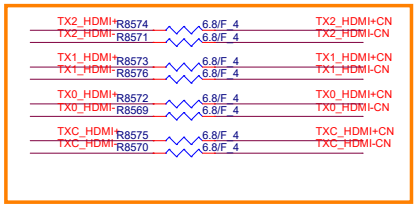
[9,10,11,13,14,16,17,18,21,22,26,28,29,34,35,36,37,38,39,46,49,50,54,55] +3V

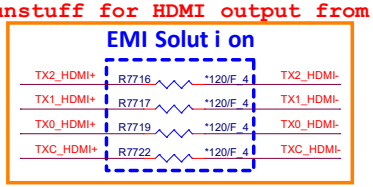
[26,28,29,34,39,47,48,49,50,52] +5V

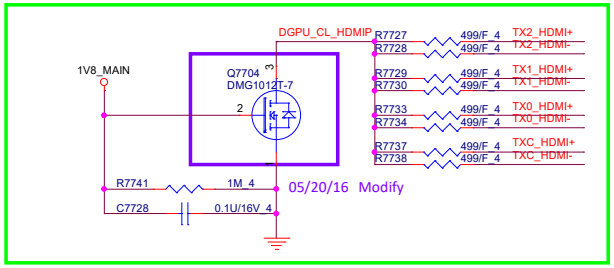
01/11 change to 0 ohm for NV suggest



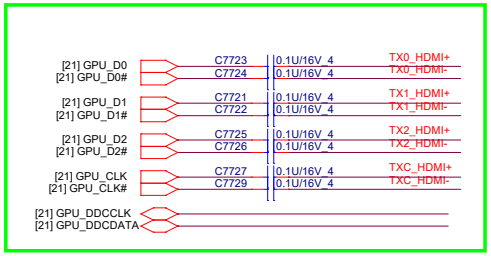
01/11 unstuff for HDMI output from GPU

EMI Solut i on

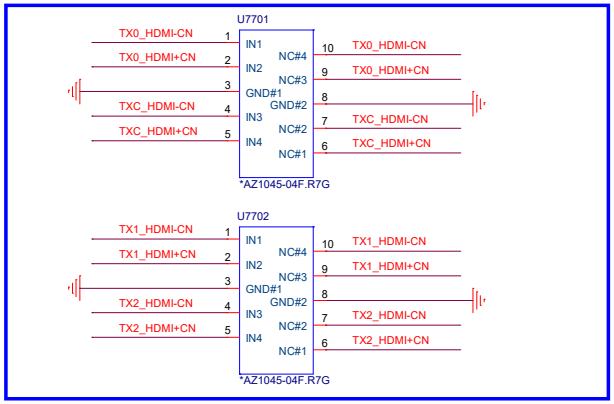




11/03 modify for HDMI2.0



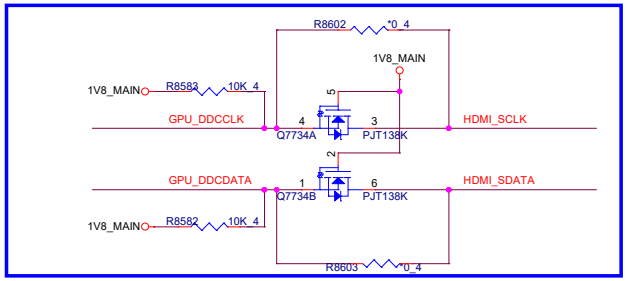
ESD

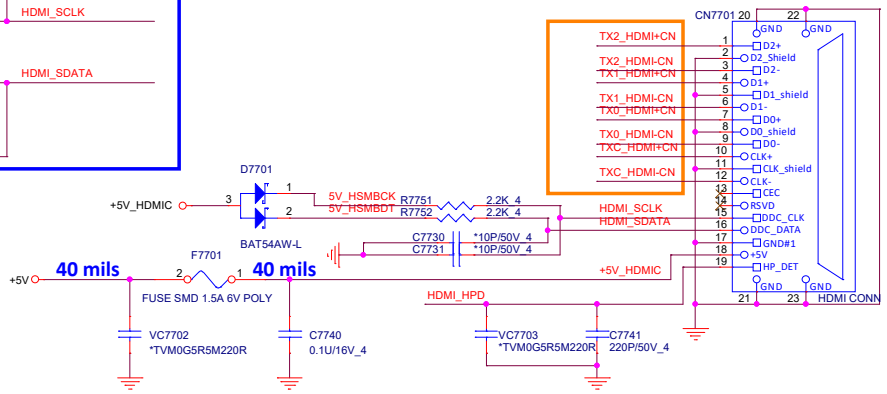


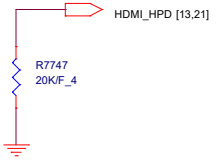
11/24 moddify

HDMI SMBus Isolat i on

Close to HDMI connector







PROJECT : NLA

Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 -- HDMI/HDMI REDRIVER	1A
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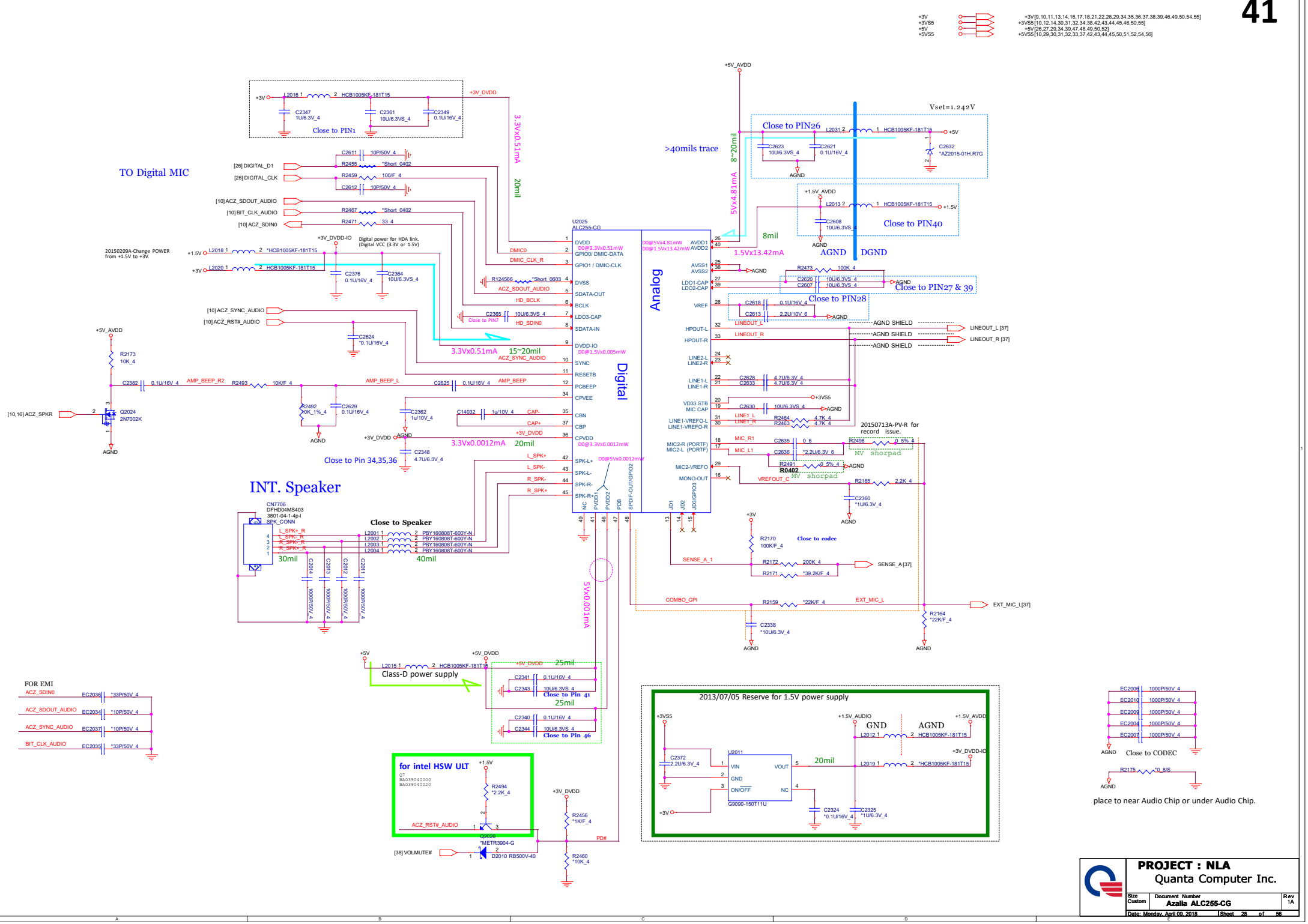
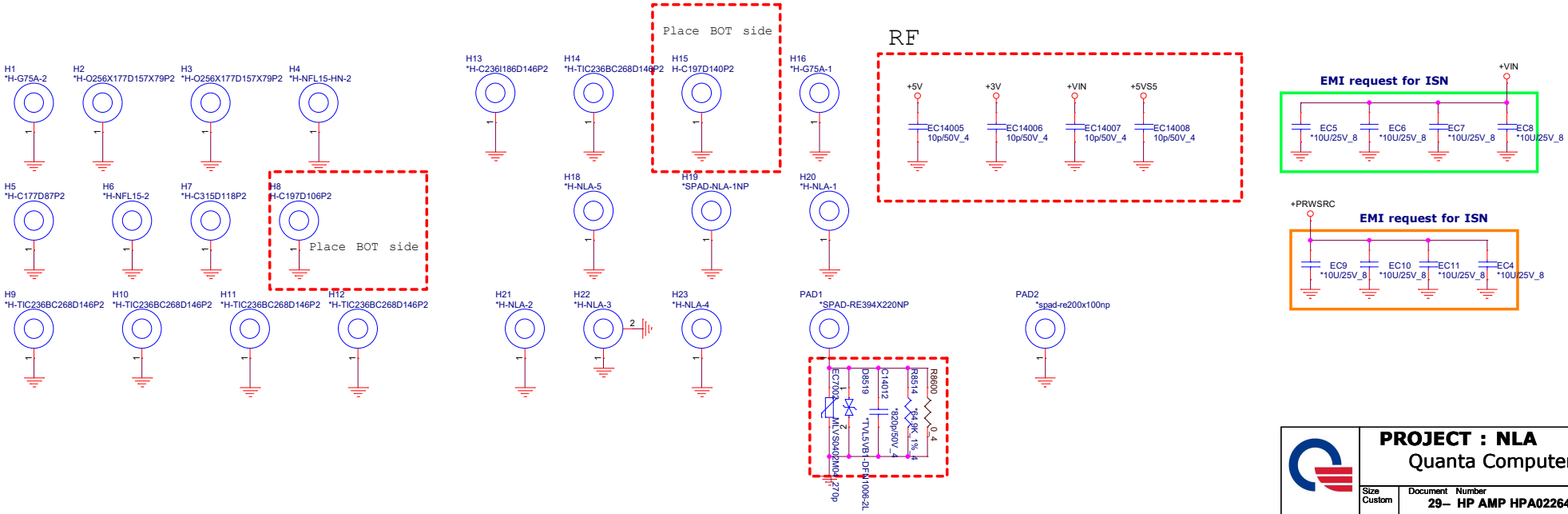


PROJECT : NLA	Quanta Computer Inc.
Size: Custom	Document Number: Azalia ALC255-CG
Rev: 1A	
Date: Monday, April 09, 2018	Sheet 28 of 56

Head Phone out

HOLE



PROJECT : NLA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	29– HP AMP HPA022642RTJR	1A

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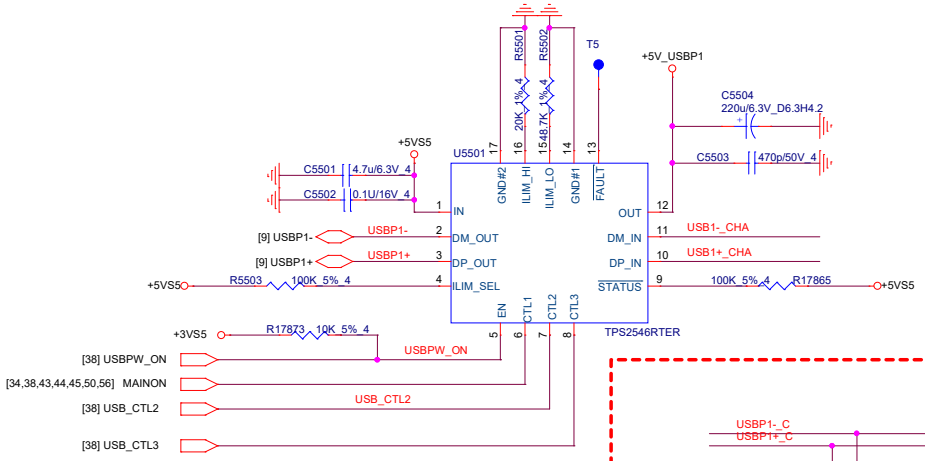
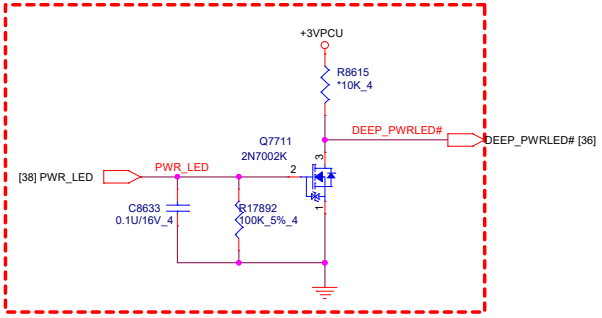
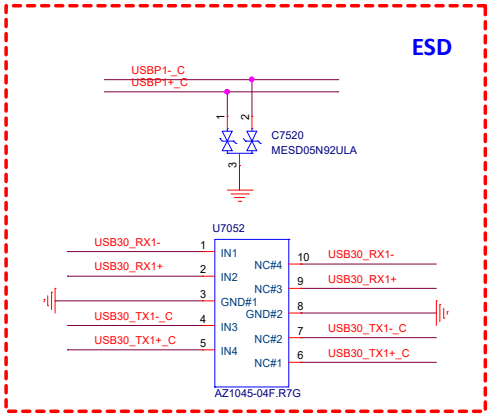


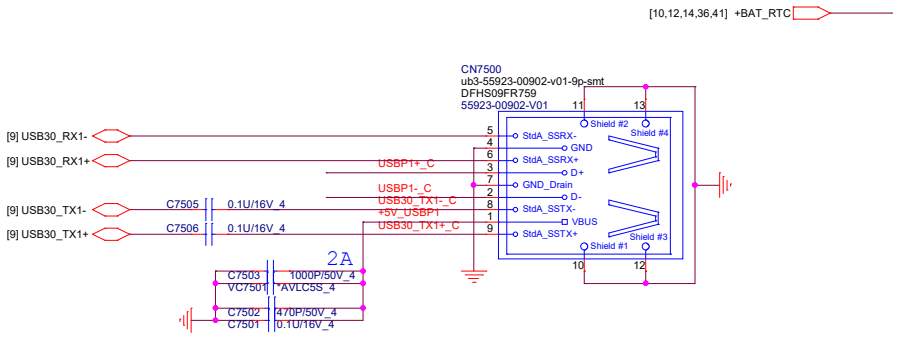
Daughter Board

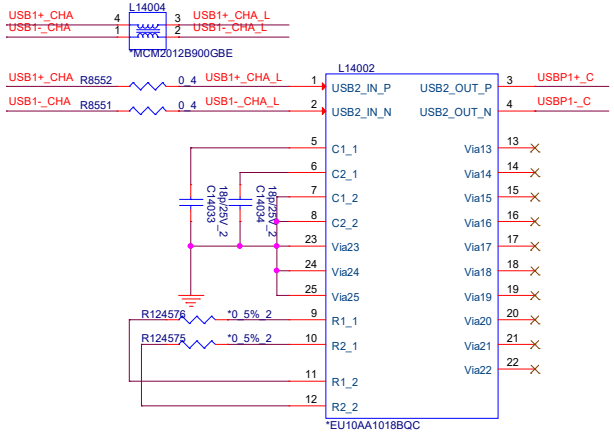
1123 Add PWR LED MOS Circuit





1125 Reserve ESD protection component





PROJECT : NLA

Quanta Computer Inc.

Size	Document Number	Rev
Custom	30 -- USB3.0/DB	1A

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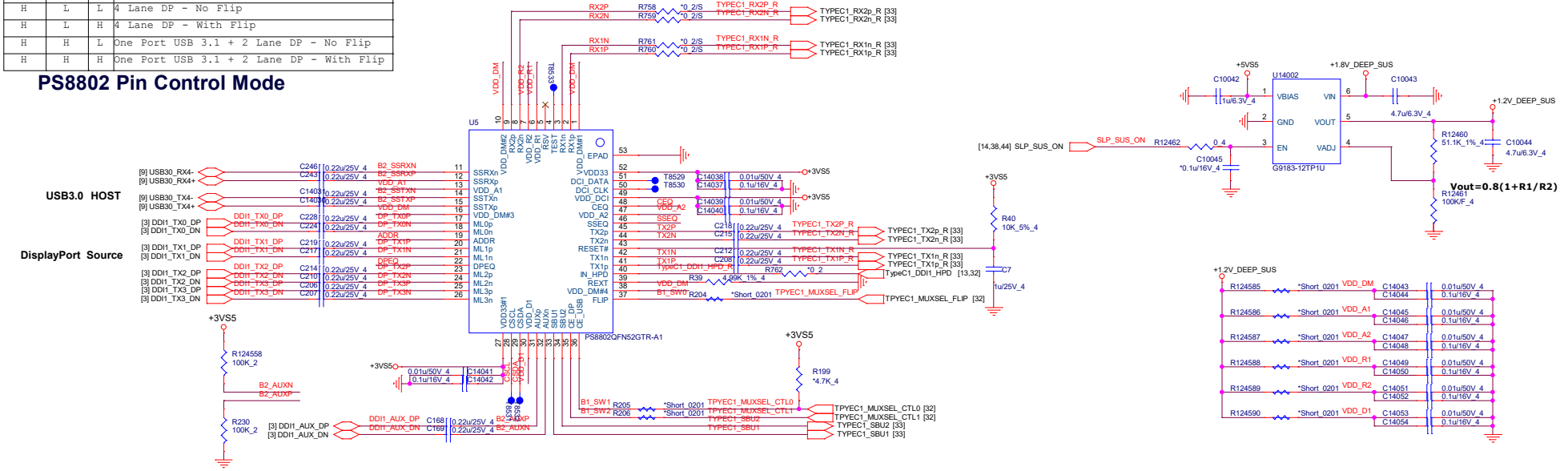
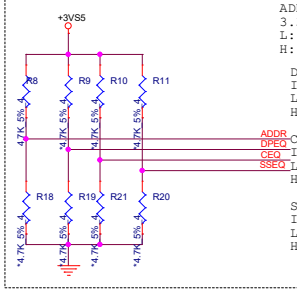
CE_DP	CE_USB	FLIP	PS8802 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

PS8802 Pin Control Mode



Strapping Pins

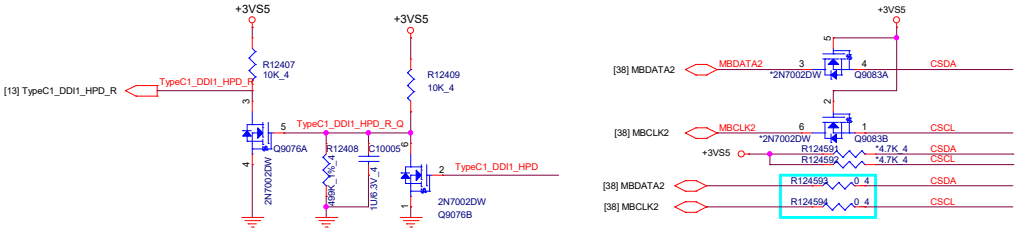


ADDR: I2C control bus address. Internally pull down at 150k欧 3.3V I/O.
L: Slave address 0x10-0x2F(default)
H: Slave address 0x30-0x4F

DPEQ:DP Receiver equalization setting; Internally pull down at 150k欧 3.3V I/O.
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB

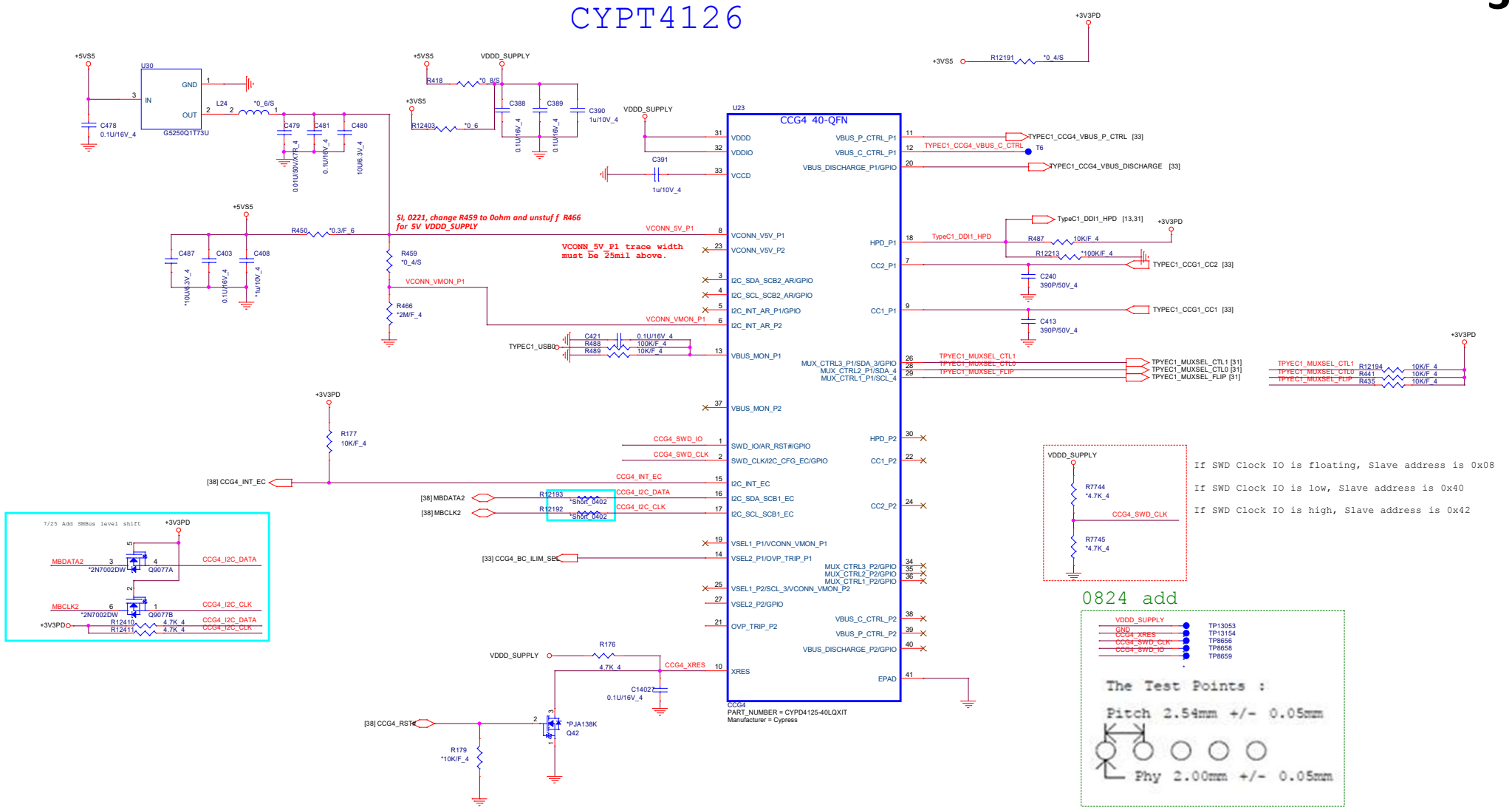
CEQ: USB Type-C connector facing Rx channel receiver equalization setting; Internally pull down at 150k欧 3.3V I/O.
L: Compensation for channel loss up to 16dB(Default)
H: Compensation for channel loss up to 18dB

SSEQ: USB Host facing Rx channel receiver equalization setting; Internally pull down at 150k欧 3.3V I/O.
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB



	PROJECT : NLA Quanta Computer Inc.	
Size	Document Number PORTA_TUSB546I MUX	Rev 1A
Date: Monday, April 09, 2018	Sheet 31of 56	

PN : ARNL9US0000
CYPT4126



PROJECT : NLA		
Quanta Computer Inc.		
Size	Document Number: Cypress CCG4- USB3.1 PD_A	Rev: 1A
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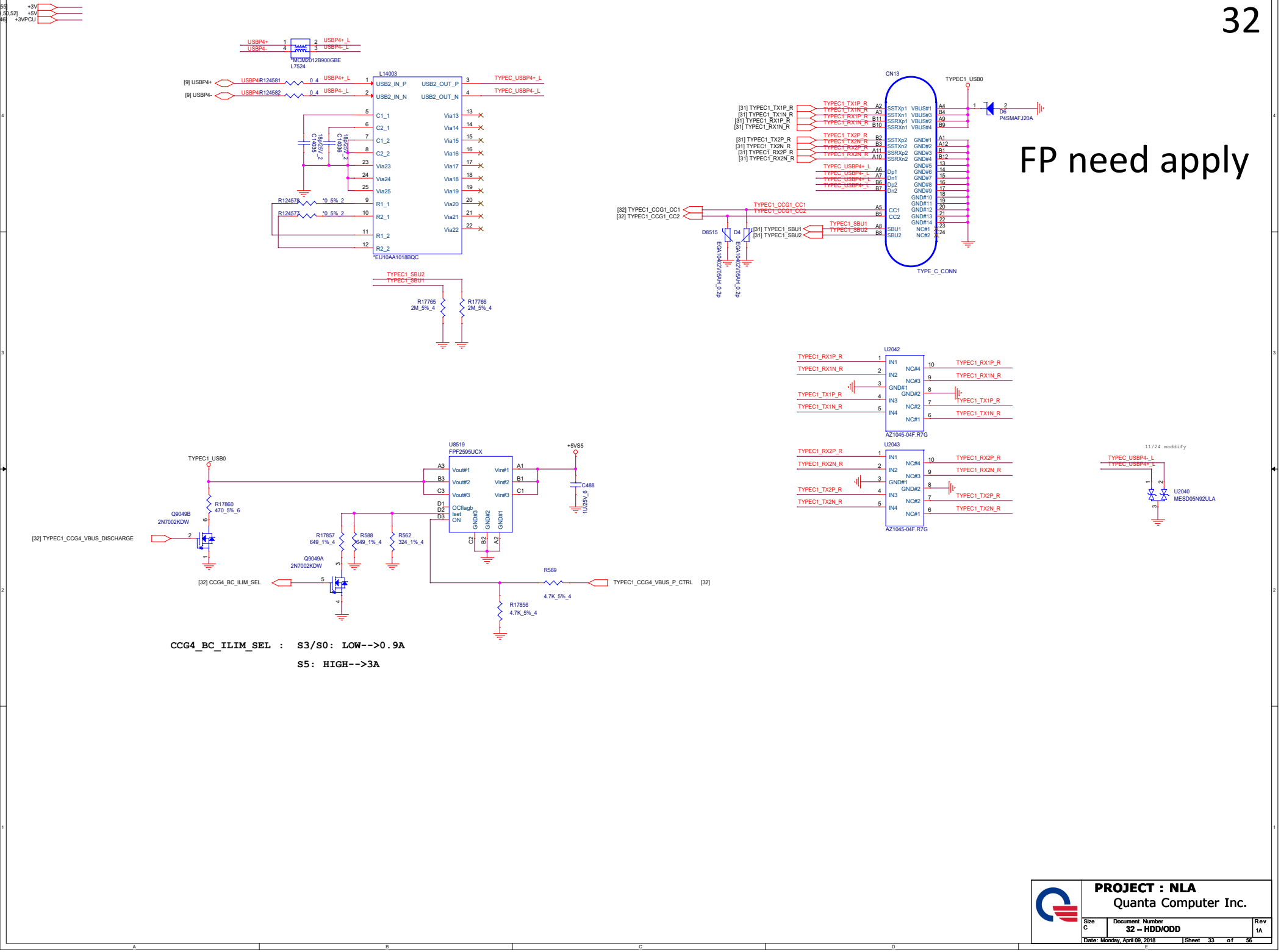
FP need apply



CCG4_BC_ILIM_SEL : S3/S0: LOW-->0.9A

S5: HIGH-->3A

PROJECT : NLA Quanta Computer Inc.		
Size C	Document Number 32 – HDD/ODD	Rev 1A
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SSD

CN4901
NASM0-S6701-TS40
DFHS75FR392
ngff-apci0107-p001a-75p-km

NGFF MKEY

2.5A

[11] PCIE_SATA_RXN9
[11] PCIE_SATA_RXP9
[11] PCIE_SATA_TXN9
[11] PCIE_SATA_TXP9
[11] PCIE_SATA_RXN10
[11] PCIE_SATA_RXP10
[11] PCIE_SATA_TXN10
[11] PCIE_SATA_TXP10
[11] PCIE_SATA_RXN11
[11] PCIE_SATA_RXP11
[11] PCIE_SATA_TXN11
[11] PCIE_SATA_TXP11
[11] PCIE_SATA_RXP12
[11] PCIE_SATA_RXN12
[11] PCIE_SATA_TXN12
[11] PCIE_SATA_TXP12
[11] CLK_PCIE_SSDN
[11] CLK_PCIE_SSDP

GND#1 GND#3 PETN3 PETP3 GND#7 PERN3 PERP3 GND#8 PETN2 PETP2 GND#2 PERN2 PERP2 GND#9 PETN1 PETP1 GND#10 PERN1 PERP1 GND#11 SATA B+/PETN0 SATA B-/PETP0 GND#12 SATA A-/PERN0 SATA A+/PERP0 GND#13 REFCLKN REFCLKP GND#14

3.3Vaux_1 3.3Vaux_2 NC#10 NC#11 DAS/DSS#(I)(OD) 3.3Vaux_3 3.3Vaux_4 3.3Vaux_5 3.3Vaux_6 NC#12 NC#13 NC#14 NC#15 NC#16 NC#17 NC#2 NC#3 NC#4 DEVSLP NC#5 NC#6 NC#7 NC#8 NC#9 PERST#/NC CLKREQ#/NC PEWAKE#/NC NC#18 NC#19

NC#1 PEDET(OC-PCIE/GND-SATA) GND#4 GND#5 GND#6 SUSCLK 3.3Vaux_7 3.3Vaux_8 3.3Vaux_9

+3V_SSD
SATA_LED#[11,36]
DEVSLP0 [9]
PLTRST#[12,19,35,36,37,38]
PCIE_CLKREQ_SSD# [11]
*PAD TP1125

R1831 *Short_0805 +3V
D8512 RB500V-40
R1824 10K_4
R1816 *0_4
R1805 *Short_0402
R1798 *Short_0402
R1828 *Short_0805 +3V

C2132 0.01U/50V_4
C2137 0.1U/16V_4
C2096 4.7U/6.3V_4
C2128 0.22U/10V_4
C2125 0.22U/10V_4
C2135 0.22U/10V_4
C2131 0.22U/10V_4
C2140 0.22U/10V_4
C2136 0.22U/10V_4
EC1054 470p/50V/X7R_4
EC1044 10U/6.3V_4
EC1045 10U/6.3V_4

R1769 100K/F_4 PEDET
[11] GPIO35 R1803 *Short_0402
Q1056 2N7002K

Mini Card
WLAN/BT(Opt i on)
PULSAR_38P4M_REFCLK_R1 R12470 *10K_5%_4
SUSCLK_32KHZ R12471 *100K/F_4
Near connector

HD4600
51625-01001-001-10p-l
DFFC10FR110
SATA_HDD

SATA_TXP1B_C C4600 0.01U/50V_4 SATA_TXP2[11]
SATA_TXN1B_C C4601 0.01U/50V_4 SATA_TXN2[11]
SATA_RXN1B_C C4602 0.01U/50V_4 SATA_RXN2[11]
SATA_RXP1B_C C4603 0.01U/50V_4 SATA_RXP2[11]
+5V
C4604 *10U/6.3VS_4
C4605 10U/6.3VS_4
C4606 0.1U/16V_4

HDD

0925 for CNVi power control

+3VPCU +3VPCU
R1188 10K_4
R124531 10K_4
R1187 200K_4
Q9079A 2N7002KDW
Q9079B 2N7002KDW
[10] CNVi_EN#
R23026 75K_1%_4
[30,38,43,44,45,50,56] MAINON

+3VS5 +3V_WLAN_P
Q1018 PJA3415
60mil
C1793 *0.022U/25V_4
C14013 0.1U/16V_4
+3V_WLAN_P
C14015 10U/6.3V_4
C14014 0.1U/16V_4

For EMI Suggest i on
CLK_24M_DEBUG R1715 *0_4 EC1037 *33P/50V_4
Support Wake Funct i on(Reserve)
[11] PCIE_CLKREQ_WLAN# R1333 *Short_0402 REQ_WLAN#

+3V_WLAN_P
C2072 0.1U/16V_4
C2071 0.01U/25V_4
C2068 10U/6.3V_4

CN1012
DFHS75FR119
ngff-nase0-s6701-tsh4-ke-smt
NASE0-S6701-TSH4

NGFF EKEY

1.5A

[9] USBP7+
[9] USBP7-
[13] CNV_WR_LANE1_DN
[13] CNV_WR_LANE1_DP
[13] CNV_WR_LANE0_DN
[13] CNV_WR_LANE0_DP
[13] CNV_WR_CLK_DN
[13] CNV_WR_CLK_DP

GND#3 USB_D+ USB_D- GND#4 SDIO CLK(O) SDIO CMD(IO) SDIO DAT0(IO) SDIO DAT1(IO) SDIO DAT2(IO) SDIO DAT3(IO) SDIO Wake(I) SDIO Reset

3.3Vaux#1 3.3Vaux#2 LED#1 PCM_CLK PCM_SYNC PCM_IN PCM_OUT LED#2 GND#13 UART Wake UART Rx

[11] PCIE_TXP6_WLAN
[11] PCIE_TXN6_WLAN
C2083 0.1U/16V_4 PCIE_TXP6_WLAN_C
C2080 0.1U/16V_4 PCIE_TXN6_WLAN_C
[11] PCIE_RXP6_WLAN
[11] PCIE_RXN6_WLAN
[11] CLK_PCIE_WLANP
[11] CLK_PCIE_WLANN
TP1058 *PAD REQ_WLAN# MINICAR_PME#
[13] CNV_WT_LANE1_DN
[13] CNV_WT_LANE1_DP
[13] CNV_WT_LANE0_DN
[13] CNV_WT_LANE0_DP
[13] CNV_WT_CLK_DN
[13] CNV_WT_CLK_DP

GND#5 PETp0 PETn0 GND#6 PERp0 PERn0 GND#7 REFCLKP0 REFCLKN0 GND#8 CLKREQ0# PEWake0# GND#9 PETp1 PETn1 GND#10 PERp1 PERn1 GND#11 Reserved1 Reserved2 GND#12

UART Tx UART RTS UART CTS Clink RESET CLink DATA CLink CLK COEX3 COEX2 COEX1 SUSCLK(32KHz) PERST0# W_DISABLE2# W_DISABLE1# NFC_I2C_SM_DATA NFC_I2C_SM_CLK NFC_I2C_IRQ GPIO0_NFC_RESET# UIM_SWP/PERST1# UIM_POWER_SNK UIM_POWER_SRC 3.3Vaux#3 3.3Vaux#4

WLAN_LED# R1635 4.7K_4 +3V_WLAN_P
R1640 0_5%_4
CNV_RF_RESET#_L
MODEM_CLKREQ_L
CNV_BRI_RSP_L R12475 22/F_4 CNV_BRI_RSP [13]
CNVi RBI_RSP, RGI_RSP 22 Ohm, to be placed close to the connector.
CNVi RBI_DT, RGI_DT 33 Ohm, to be placed close to the PCH.
CNV_RGI_RSP_L R12476 33_4 CNV_RGI_DT [13,16]
R12477 22/F_4 CNV_RGI_RSP [13]
R124532 33_4 CNV_BRI_DT [13,16]
SUSCLK_32KHZ R12443 *0_2 SUSCLK_32K SUSCLK_32K [10]
9/13 Change net name
PLTRST#
INT_BT_OFF#
INT_RF_OFF#
R1690 10K_4
R1693 10K_4 +3V_WLAN_P
LAD0
CLK_24M_DEBUG
LFRAME#
PULSAR_38P4M_REFCLK_R1
R12421 *Short_0201 PULSAR_38P4M_REFCLK [11]
LAD1
LAD2
LAD3
LAD0 [9,35,38]
CLK_24M_DEBUG [9]
LFRAME# [9,35,38]
LAD1 [9,35,38]
LAD2 [9,35,38]
LAD3 [9,35,38]

Pin71 and 73 need connect to CNV WT CLK
But it will impact Debug Card signal
Need verify it.

+1.8V_DEEP_SUS
Q9080
NL17SZ08DFT2G
MODEM_CLKREQ_L
MODEM_CLKREQ [10]
R124534 75K_1%_4
R124533 10K_4

+1.8V_DEEP_SUS
Q9081
NL17SZ08DFT2G
CNV_RF_RESET#_L
CNV_RF_RESET# [10]
R124535 75K_1%_4
R124536 10K_4

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Quanta Computer Inc.

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Custom	33 -- SSD/WLAN	1A
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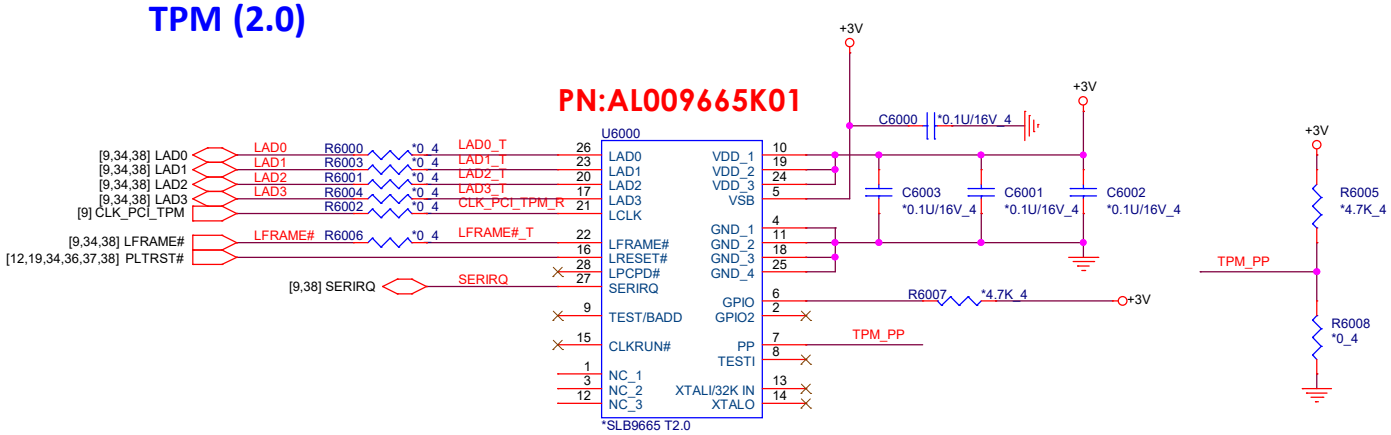
TPM (2.0)



Accelerometer Sensor

PROJECT : NLA		
Quanta Computer Inc.		
B	34 - TPM/Sensor	Document Number 1A Rev
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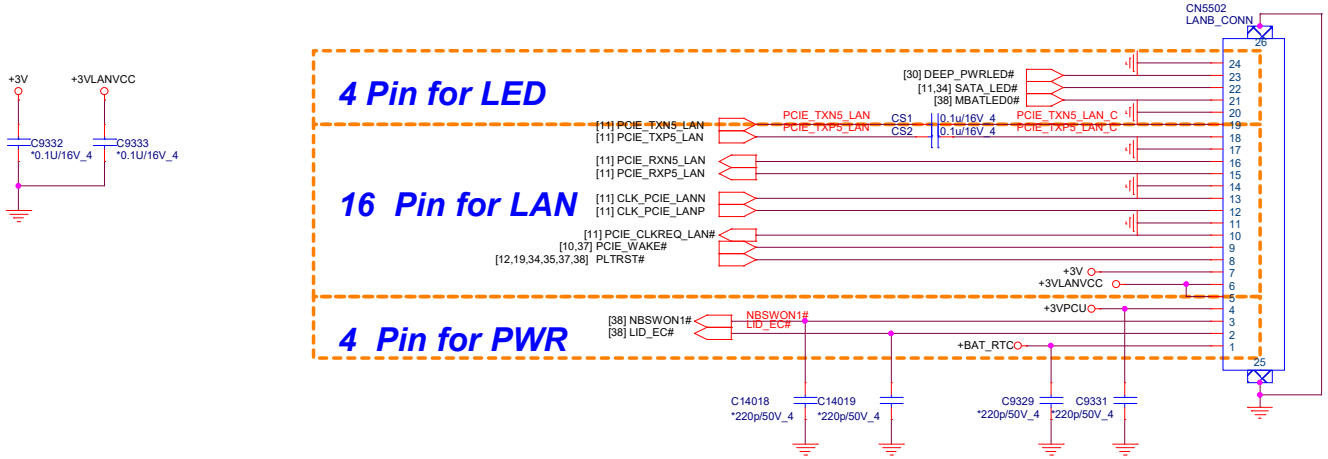
LAN Daughter Board



PROJECT : NLA

Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 -- LAN RTL8107ESH-CG/RJ45	1A

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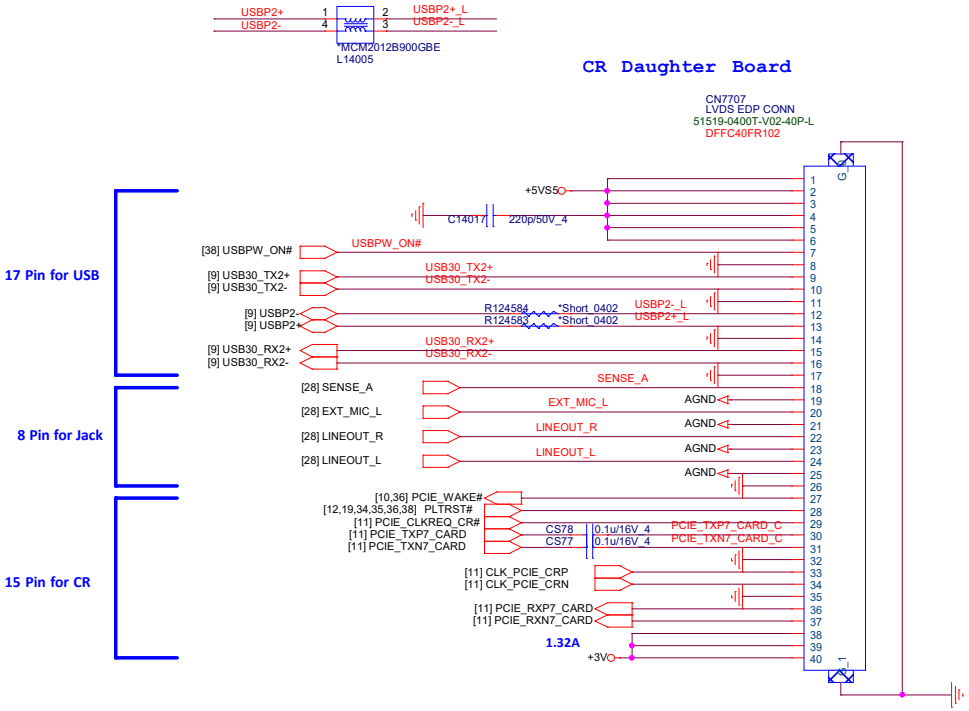
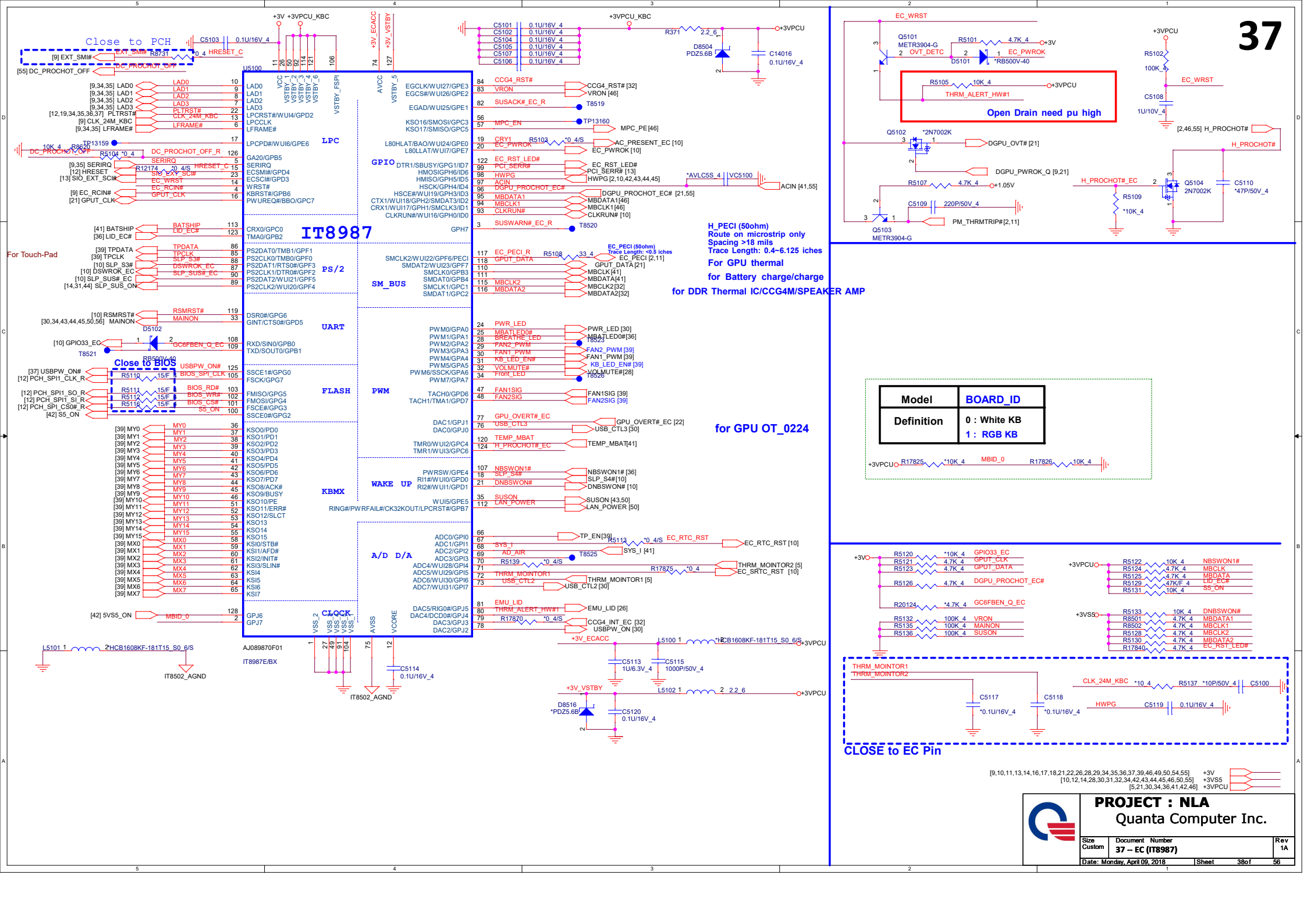
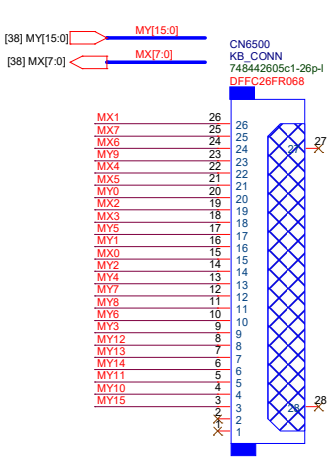
RTS5237S PCIE CARD READER Controller



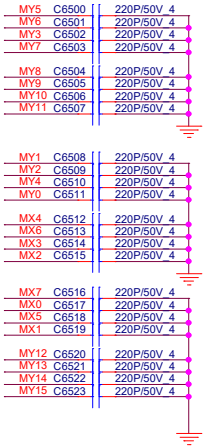
PROJECT : NLA	
Quanta Computer Inc.	
Size: Custom	Document Number: 36 -- CR RTS5237S/CR SOCKET
Rev: 1A	
Date: Monday, April 09, 2018	Sheet 37 of 56


37
Close to PCH
IT8987
U5100
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
Close to BIOS
For Touch-Pad
Open Drain need pu high
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
For GPU thermal
for Battery charge/charge
for DDR Thermal IC/CCG4M/SPEAKER AMP
for GPU OT_0224
Model
BOARD_ID
Definition
0 : White KB
1 : RGB KB
CLOSE to EC Pin
PROJECT : NLA
Quanta Computer Inc.
Size Custom
Document Number
37 -- EC (IT8987)
Rev 1A
Date: Monday, April 09, 2018
Sheet 38of 56

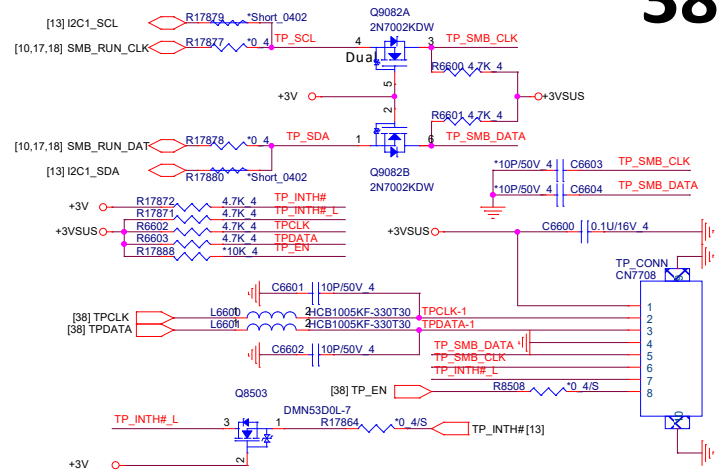
KEYBOARD Con.



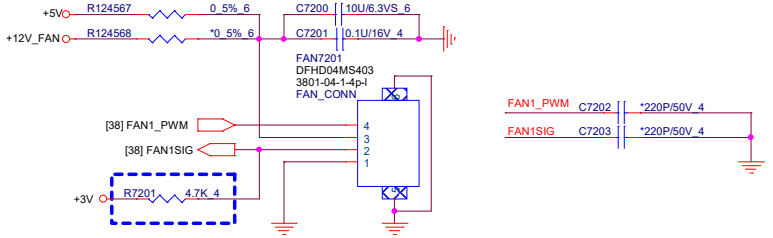
KEYBOARD PULL-UP



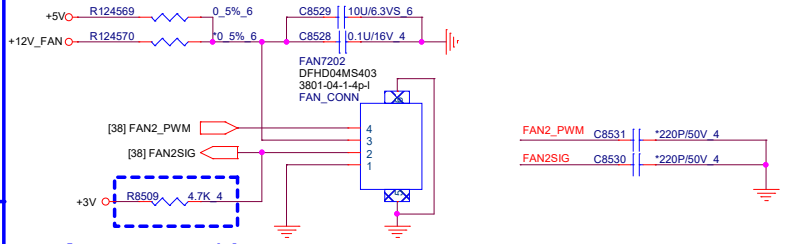
Touch Pad Connector



FAN

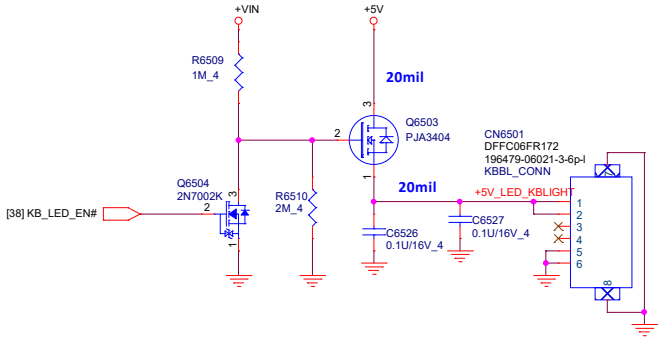


Close to EC Side



Close to EC Side

KB LIGHT CONN



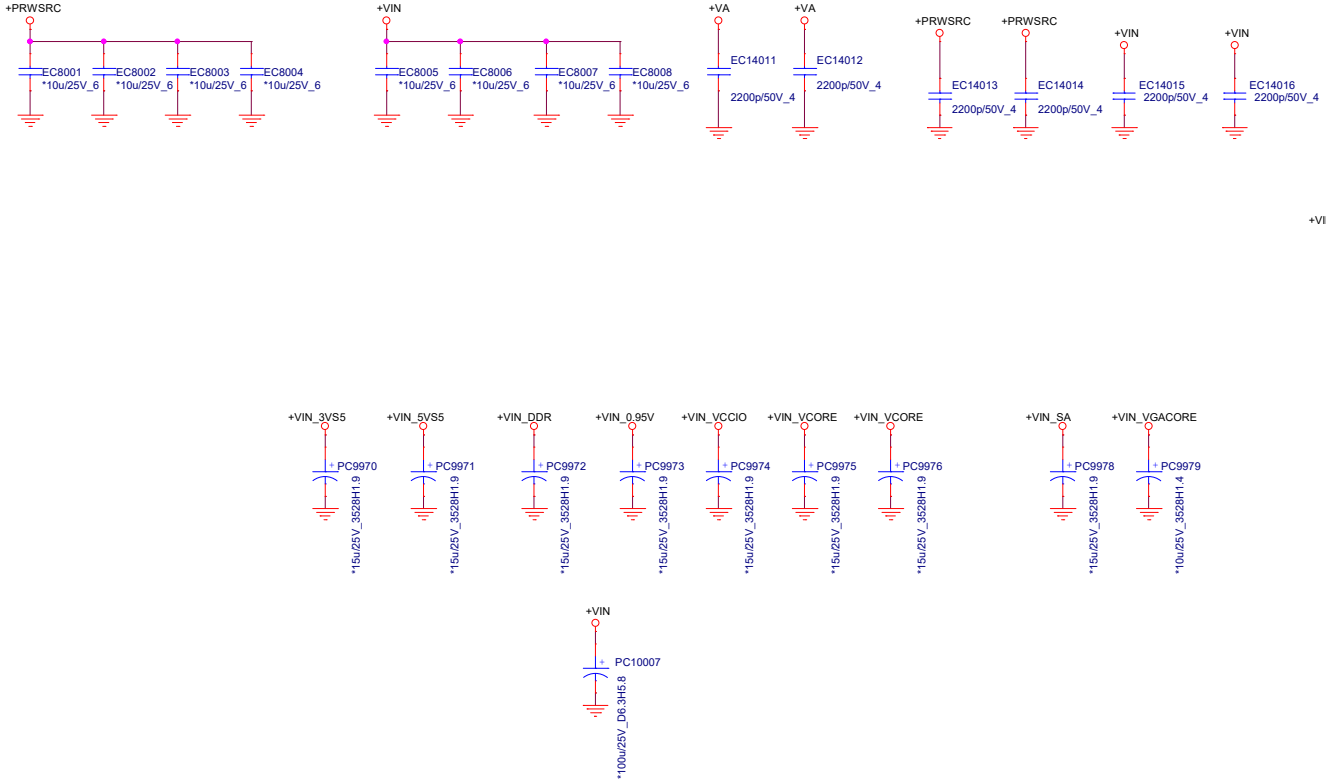
PROJECT : NLA

Quanta Computer Inc.

Size	Document Number	Rev
Custom	38 -- KB/TP/FAN/HOLE	1A

Date: Monday, April 09, 2018 | Sheet 39 of 56

[29,41] +PRWSRC
[26,29,39,41,42,43,44,45,46,47,48,49,52,54] +VIN
[41] +VA



NB5	**PROJECT : G3BD** Quanta Computer Inc.	
Size	Document Number **EMI**	Rev 1A
Date: Monday, April 09, 2018	Sheet 40 of 56	

150W/19.5V/7.7A
DC_JACK

NLA CFL+ N17P 1214 , 2nd ok

Do Not add test pad on BATDIS_G signal

Idss< 5uA

Do Not add test pad on BQBATDRV/BATDIS_ID_DOD signal

ZVS close to DC jack

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

3S1P 52.5Whr

ACDET=13V

MIN. BATV=7.2V

Set MAX charge I to 5A

DC_JACK
CN1001
VDD1 VDD2 VDD3 VDD10 VDD11 VDD12
GND4 GND5 GND6 GND7 GND8 GND9
DC-IN_CONN_12P

PQ1015 AP0203GMT-HF
PQ1003 AP0203GMT-HF
PQ1002 QM3092M6
PQ1001 QM3092M6
PQ1006 QM3002M3
PQ1007 QM3002M3
PQ1010 2N7002K
PQ1009 2N7002K
PQ1011 METR3904-G
2N7002K PQ1004
PD1002 P4SMAF-J20A
PD1003 *P4SMAF-J20A
PD1012 BAS316
PD1013 BAS316
PD1005 RB500V-40
PD1006 *RB500V-40
PD1001 PD1004 *PDZ5.6B
PD1 *PDZ5.6B

PU1001
BQ24738HRGRR
CMSRC ACDRV ACPRES VCC SDA SCL
ACP ACN REGN
HIDRV BTST PHASE LODRV GND#1 GND#2 SRP SRN BATDRV
ACDET ILIM IOUT

BAT1001
BTJ-08KVBRZB

PL9018 PL9019 PL1001 4.7uH_7x7x3

+VA_AC +VA +VAD +PRWSRC +VIN +BATCHG +BAT_RTC BATT+ +3VPCU +3VPCU
REGN6V +VA +VAD +VIN +BATCHG +BATCHG +BATCHG +BATCHG

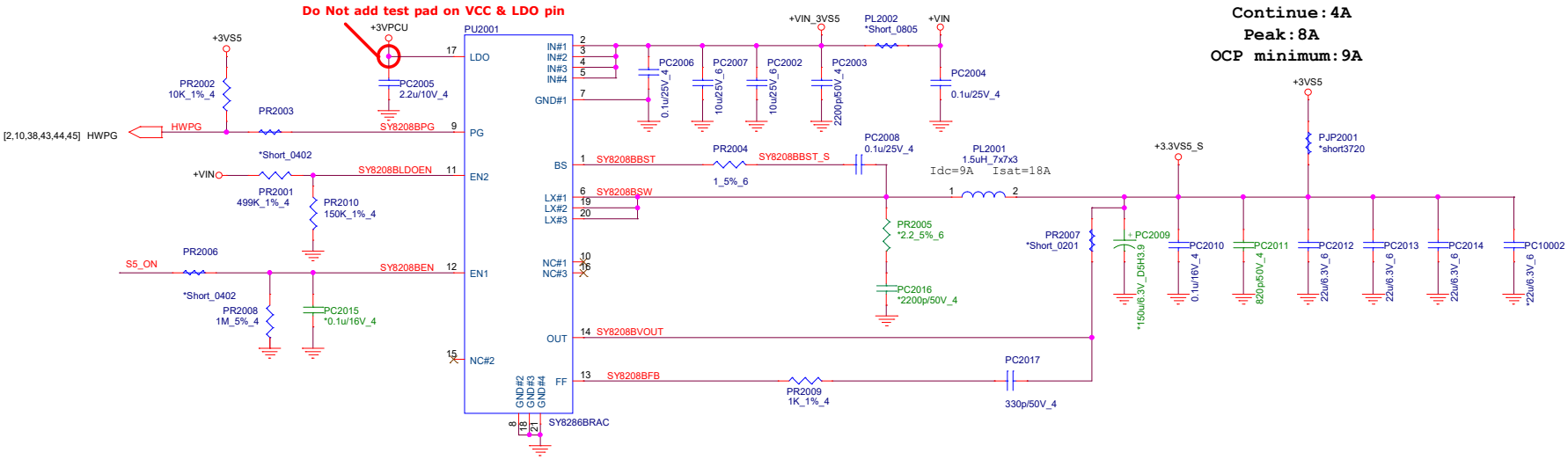
BATDIS_G BQBATDRV BATDIS_ID_DOD
BQACDRV BQCMSRC BQHIDRV BQB_1 BQB_2 BQBPHASE BQLODRV BQLR
BQVCC BQDATA BQCLK BQSRP BQSRN BQBATDRV
MBDATA MBCLK
ACIN CSOP CSON SNCHG
ACDET0 ACDET ACDET1 ACDET2 ILIM
SYS_I [38]
[38] BATSHIP SHIPNET
[38] MBDATA [38] MBCLK
TEMP_MBAT[38]

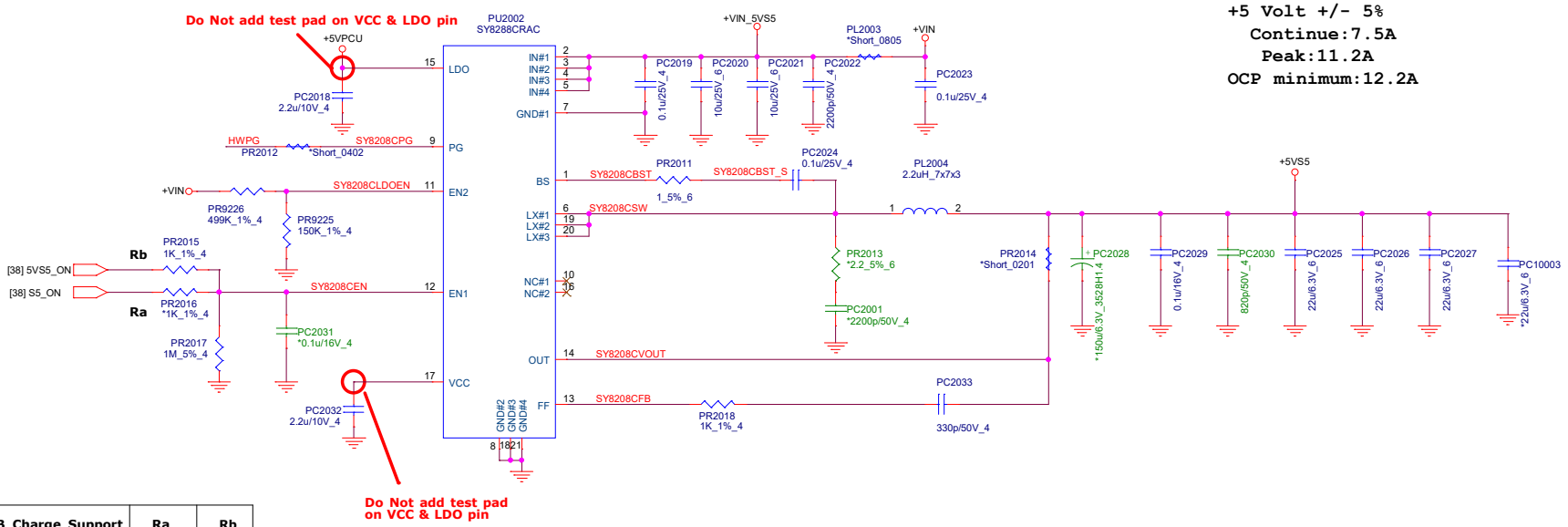
[10,12,14,36] +BAT_RTC
[26,29,39,40,42,43,44,45,46,47,48,49,52,54] +VIN
[29,40] +PRWSRC
[5,21,30,34,36,38,42,46] +3VPCU

NB5

PROJECT : G74(P15-BPA)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	1A
Date: Monday, April 09, 2018	Sheet 41 of 56	





USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

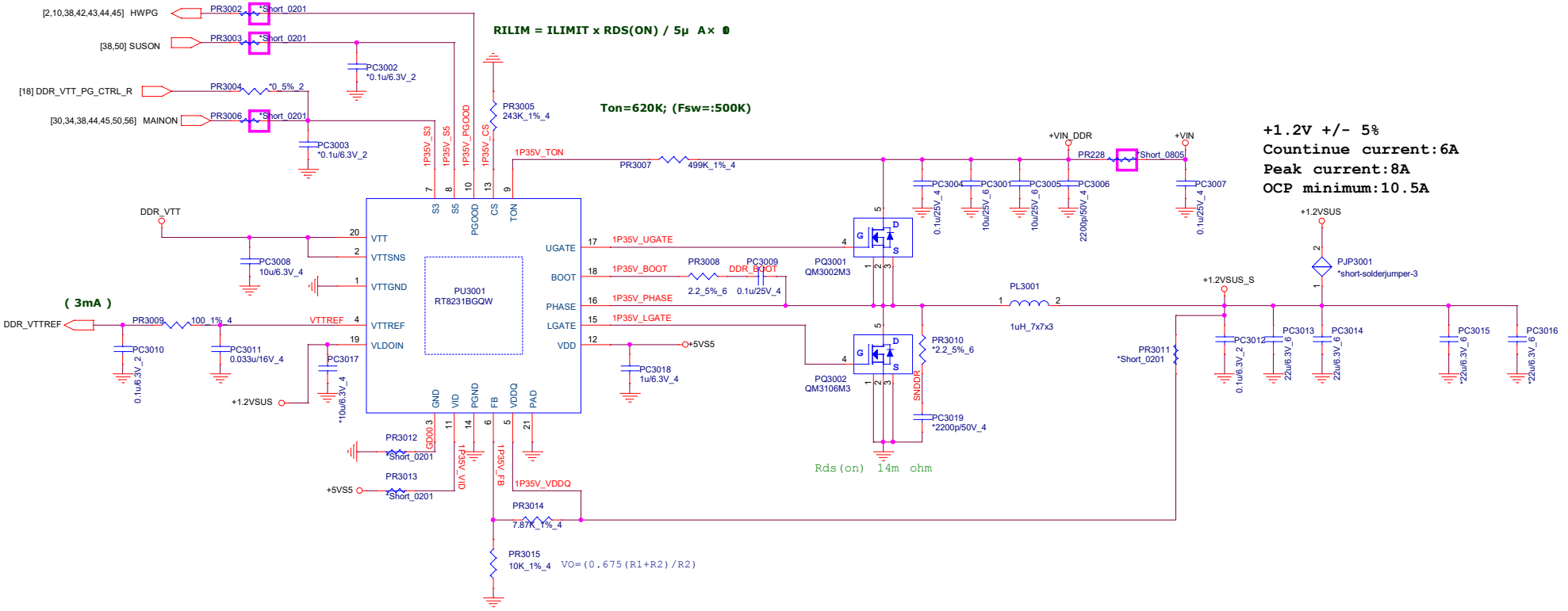
+VIN [26,29,39,40,41,43,44,45,46,47,48,49,52,54]
+3VS5 [10,12,14,28,30,31,32,34,38,43,44,45,46,50,55]
+5VS5 [10,29,30,31,32,33,37,43,44,45,50,51,52,54,56]
+3VPCU [5,21,30,34,36,38,41,46]
+5VPCU [44,50,55]

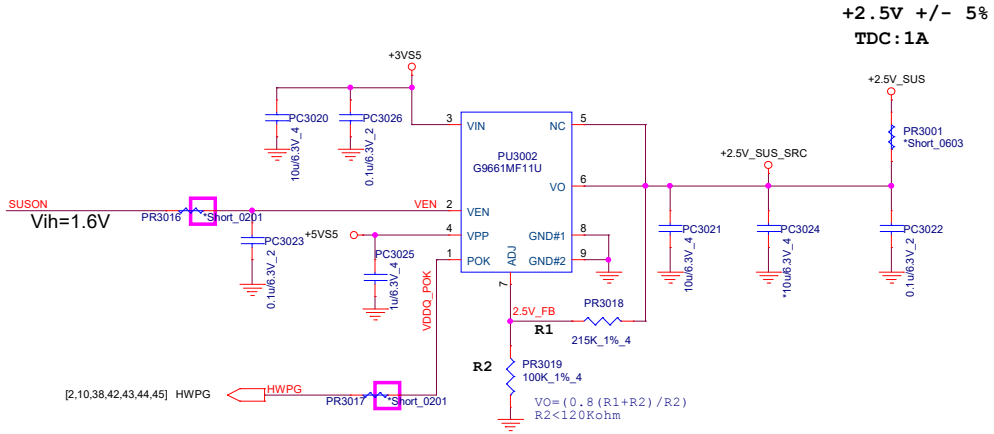
NB5

PROJECT : X1F
Quanta Computer Inc.

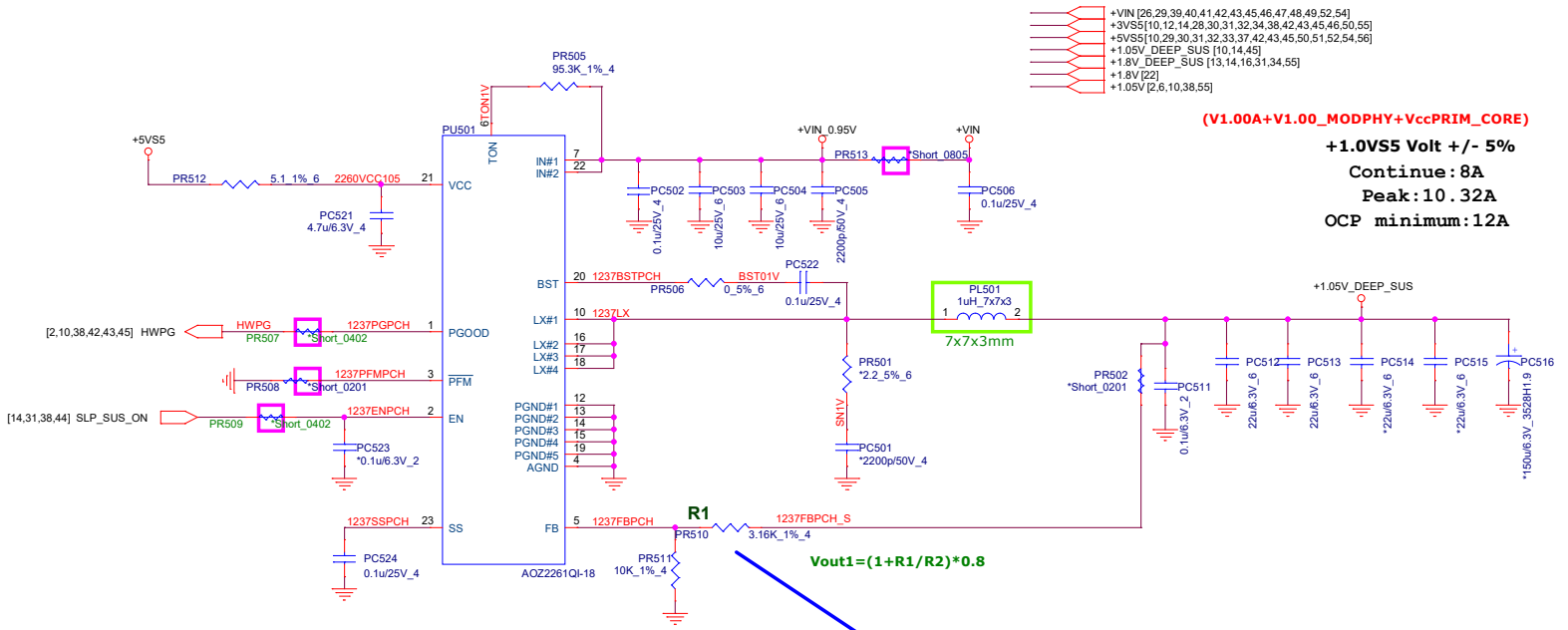
Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Monday, April 09, 2018	Sheet 42 of 56	

[26,29,39,40,41,42,44,45,46,47,48,49,52,54] +VIN
[17,18] DDR_VTT
[10,29,30,31,32,33,37,42,44,45,50,51,52,54,56] +5VS5
[10,12,14,28,30,31,32,34,38,42,44,45,46,50,55] +3VS5
[2,6,10,17,18,45] +1.2VSUS
[17,18] +2.5V_SUS





NB5	PROJECT : G74(P15-BPA) Quanta Computer Inc.		
	Size: Custom	Document Number: DDR/2.5VSUS(RT8231B)	Rev: 1A
	Date: Monday, April 09, 2018	Sheet 43 of 56	



(V1.00A+V1.00_MODPHY+VccPRIM_CORE)

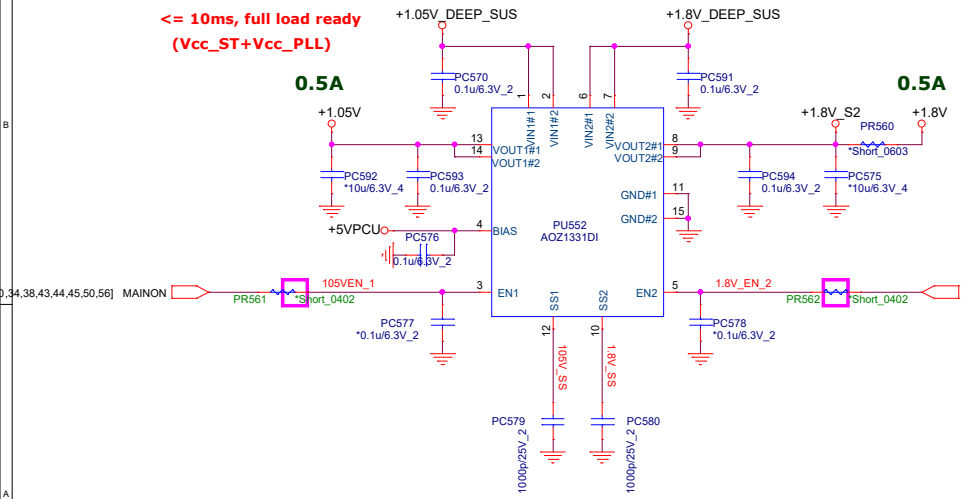
+1.0VS5 Volt +/- 5%
Continue:8A
Peak:10.32A
OCP minimum:12A

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

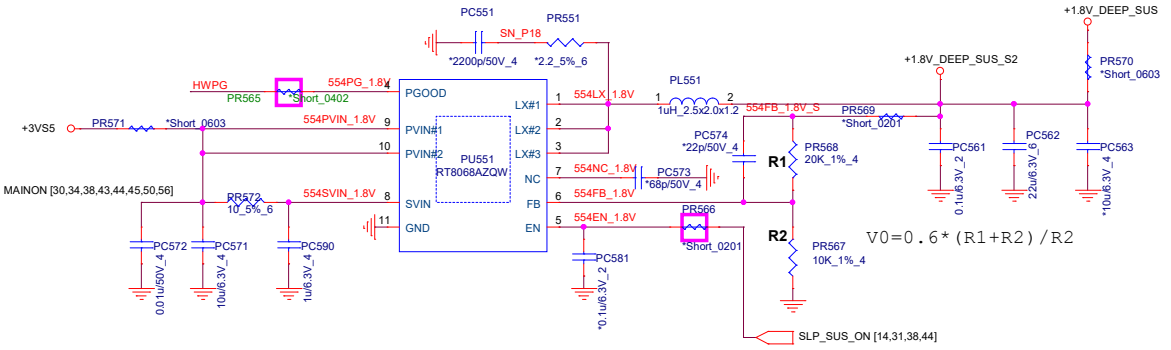
	1.91K	CS21912FB13	0.95V
SKL/KBL		CS22612FB15	1V
CNL/CFL	3.16K	CS23162FB04	1.05V

Volume Segment
+VCCSTPLL: 0.06A
Vcc_STG: 0.02A
Vcc_PLL: 0.15A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)



1.8VS5 +/- 3%
TDC:3A
EDP:4A



PROJECT : G3AA -CFL
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	+1V_DEEP_SUS/1.8V(AOZ2261)	1A
Date: Monday, April 09, 2018	Sheet 44 of 56	

Volume Segment

SKY/KBY-U22/U42/U23e
Vcc_IO: 3.4A/1V
Stuff PU601

Volume Segment

SKY/KBY-H 22/42/44e
Vcc_IO: 5.5A/0.95V
Stuff PU601 & merge 1V_deep_sus

Volume Segment

CNL U22
Vcc_IO: 5.1A/0.95V
Vcc_IO: Can merge +1.05V_deep_sus
Unstuff PU603
Unstuff PU601

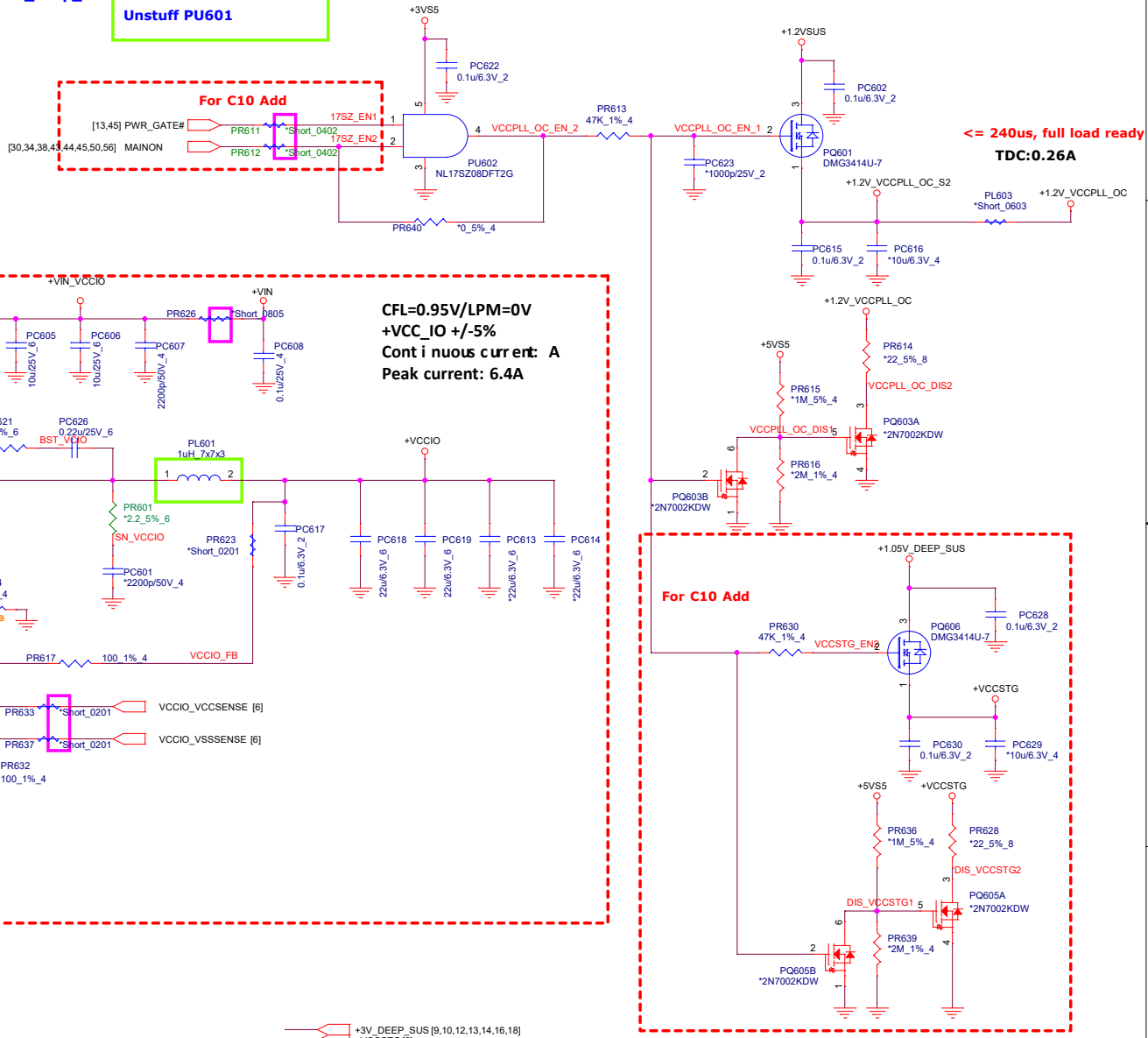
Default setting

Volume Segment

CFL H6/H4
Vcc_IO: 6.4A/0.95V
Stuff PU603
Unstuff PU601

Unstuff PU601=G5027

C10: turn off VCCPLL_OC , VCCIO , VCCSTG



VID0_VCCIO	VID1_VCCIO	LP#	VCCIO
X	X	0	0V
0	0	1	0.85V
1	0	1	0.875V
0	1(IC internal PU High)	1	0.95V

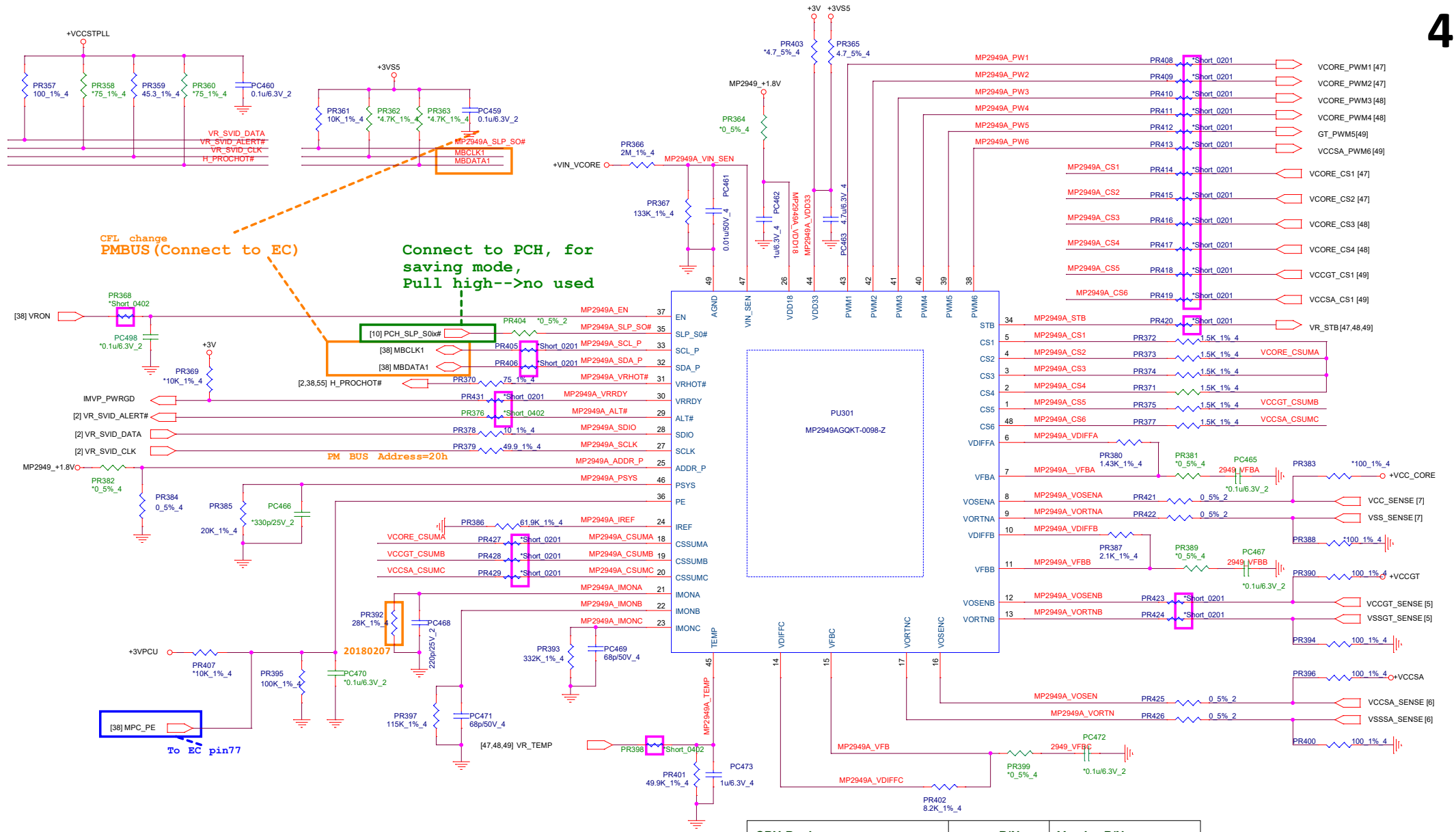
Default setting

+3V_DEEP_SUS [9,10,12,13,14,16,18]
+VCCSTG [6]
+3VS5[10,12,14,28,30,31,32,34,38,42,43,44,46,50,55]
+5VS5[10,29,30,31,32,33,37,42,43,44,50,51,52,54,56]
+VCCIO [3,6]
+1.05V_DEEP_SUS [10,14,44]
+1.2V_VCCPLL_OC [6]
+1.2VSUS [2,6,10,17,18,43]
+VIN [26,29,39,40,41,42,43,44,46,47,48,49,52,54]

NB5

PROJECT : Drax (N17-EX)
Quanta Computer Inc.

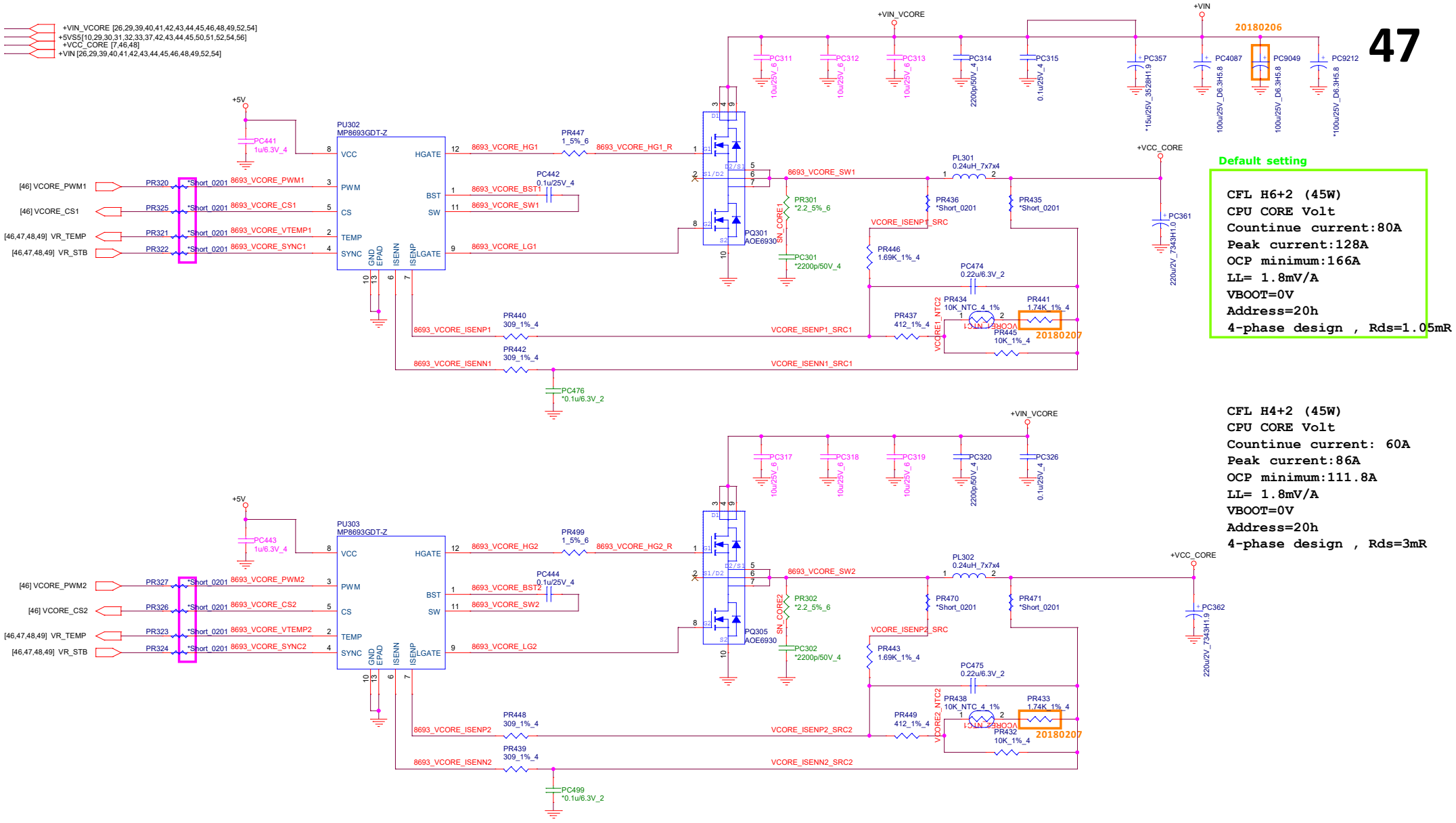
Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL/+VCCIO	1A
Date: Monday, April 09, 2018	Sheet 45 of 56	



CPU Design	P/N	Vender P/N
4+1+1 (CORE,GT,SA)=4+1+1	AL002949018	MP2949AGQKT-0098-Z
3+2+1 (CORE,GT,SA)=3+2+1	AL002949019	MP2949AGQKT-0099-Z

+VIN_VCORE [26,29,39,40,41,42,43,44,45,47,48,49,52,54]
+3VPCU [5,21,30,34,36,38,41,42]
+3VS5[10,12,14,28,30,31,32,34,38,42,43,44,45,50,55]
+5VS5[10,29,30,31,32,33,37,42,43,44,45,50,51,52,54,56]
+VCCSTPLL [2,6]
+VCC_CORE [7,47,48]
+VCCGT [5,49]
+VCCSA [6,49]

PROJECT : X1F
Quanta Computer Inc.
NB5
Size | Document Number: DDR3 (RT8231B) | Rev 1A
Monday, April 09, 2018 | Sheet 46 of 56



	ALL POWER CLIP		Cout
CFL H6+2	4 phase BAM69300003 ; AOE6930 ;1.05mR		????????
CFL H4+2	4 phase BAM69360000 ; AOE6936 ;3mR		????????

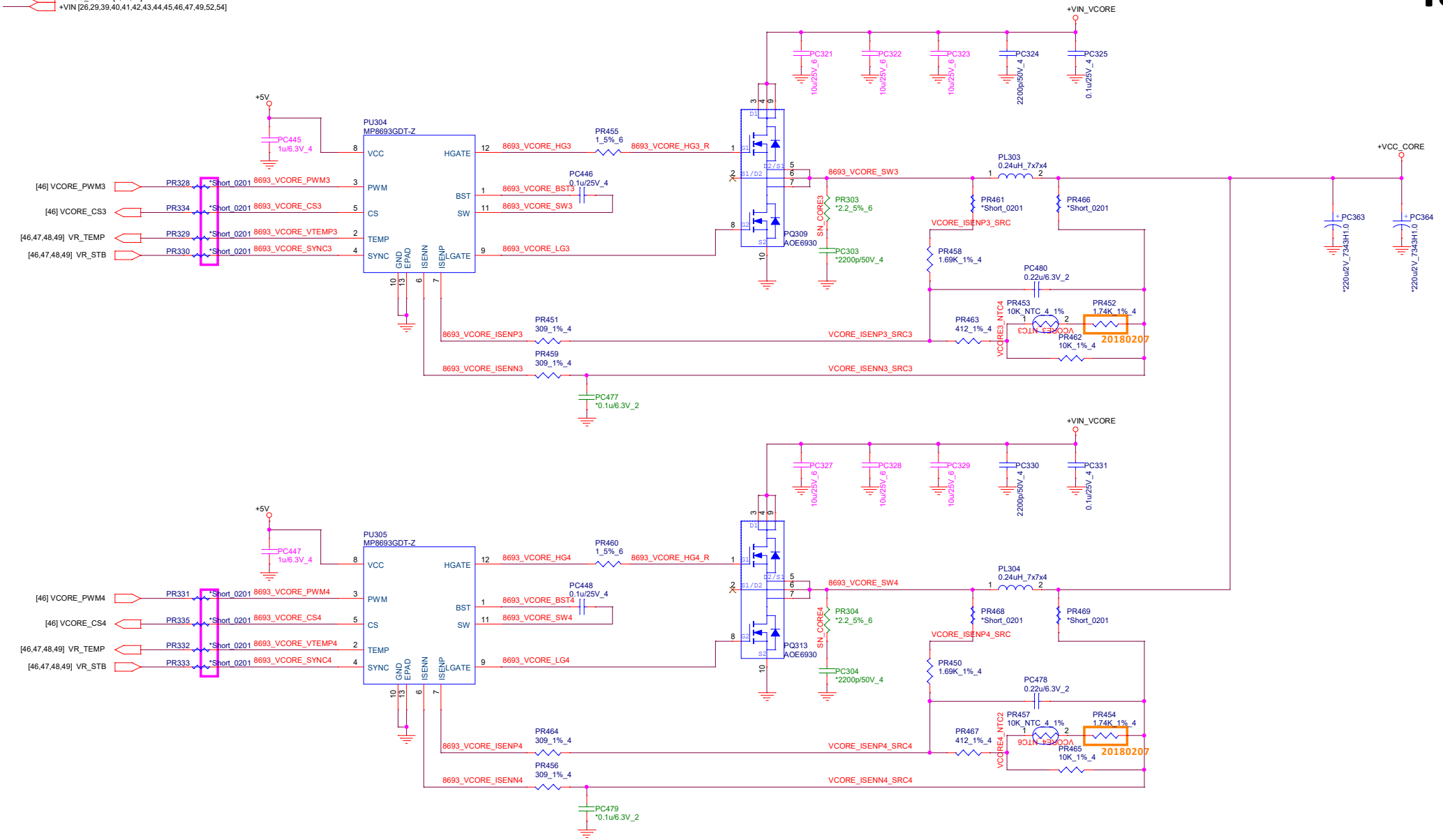
Default setting

NB5

PROJECT : G3AA -CFL
Quanta Computer Inc.

Size	Document Number	Rev
Custom	85 -- +VCC_CORE (MP86903-C)	1A
Date: Monday, April 09, 2018	Sheet 47 of 56	

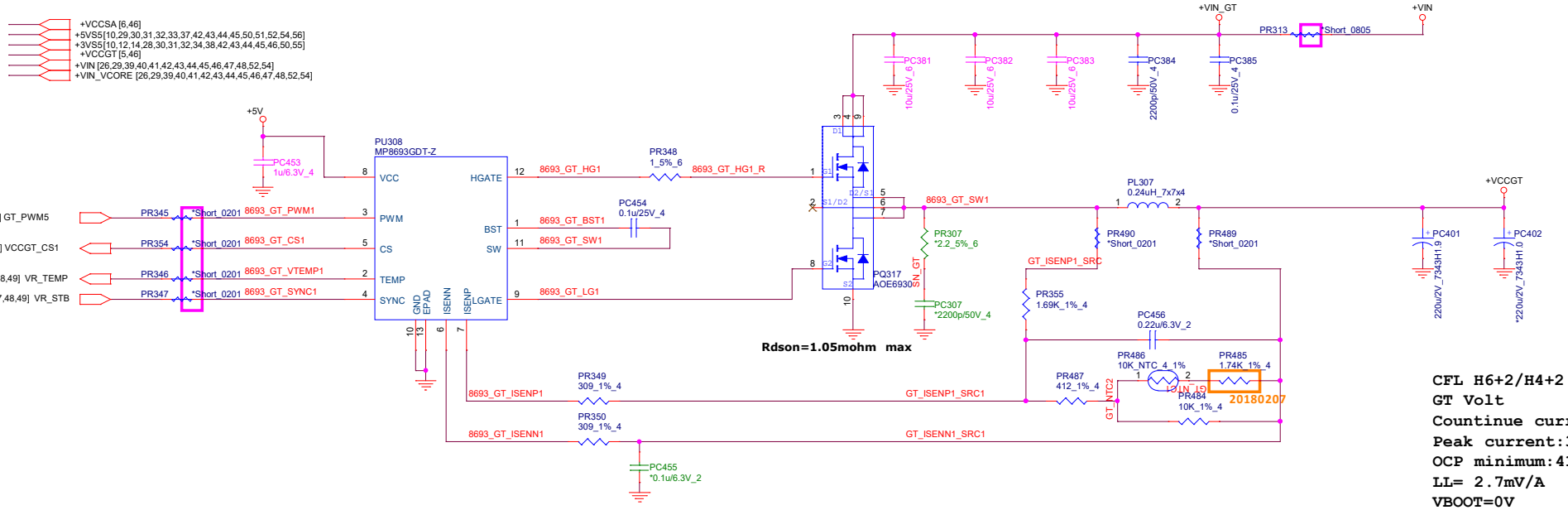
+VIN_VCORE [26,29,39,40,41,42,43,44,45,46,47,49,52,54]
+5VS5[10,29,30,31,32,33,37,42,43,44,45,50,51,52,54,56]
+VCC_CORE [7,46,47]
+VIN [26,29,39,40,41,42,43,44,45,46,47,49,52,54]



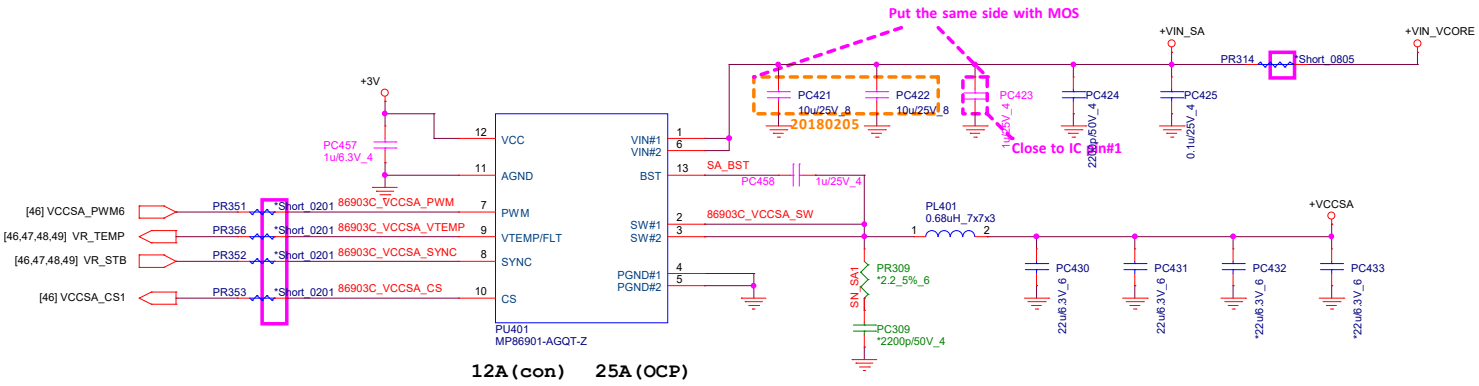
PROJECT : G3AA -CFL
Quanta Computer Inc.

Size	Document Number	Rev
Custom	85 -- +VCC_CORE (MP86903-C)	1A
Date: Monday, April 09, 2018	Sheet 48 of 56	

NB5



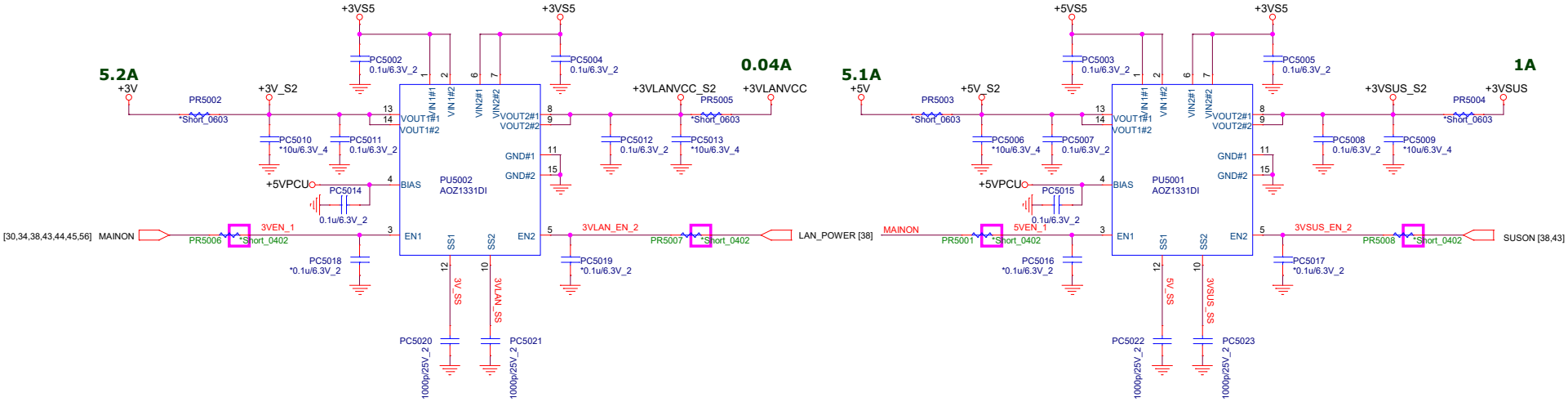
CFL H6+2/H4+2 (45W)
GT Volt
Countinue current: 25A
Peak current:32A
OCP minimum:41.6A
LL= 2.7mV/A
VBOOT=0V
Address=01h



CFL H6+2/H4+2 (45W)
VCCSA Volt
Countinue current: 10A
Peak current:11.1A
OCP minimum:16A
LL= 11.4mV/A
VBOOT=1.05V
Address=02h

NB5	PROJECT : G3AA -CFL Quanta Computer Inc.	
Size: Custom	Document Number: 86 -- +VCC_GT/+VCC_SA	Rev: 1A
Date: Monday, April 09, 2018	Sheet 49 of 56	

+3V[9,10,11,13,14,16,17,18,21,22,26,28,29,34,35,36,37,38,39,46,49,54,55]
+5VS5[10,29,30,31,32,33,37,42,43,44,45,51,52,54,56]
+3VS5[10,12,14,28,30,31,32,34,38,42,43,44,45,46,55]
+3VSUS [39]
+5V[26,27,28,29,34,39,47,48,49,52]
+3VLANVCC [36]
+5VPCU [42,44,55]

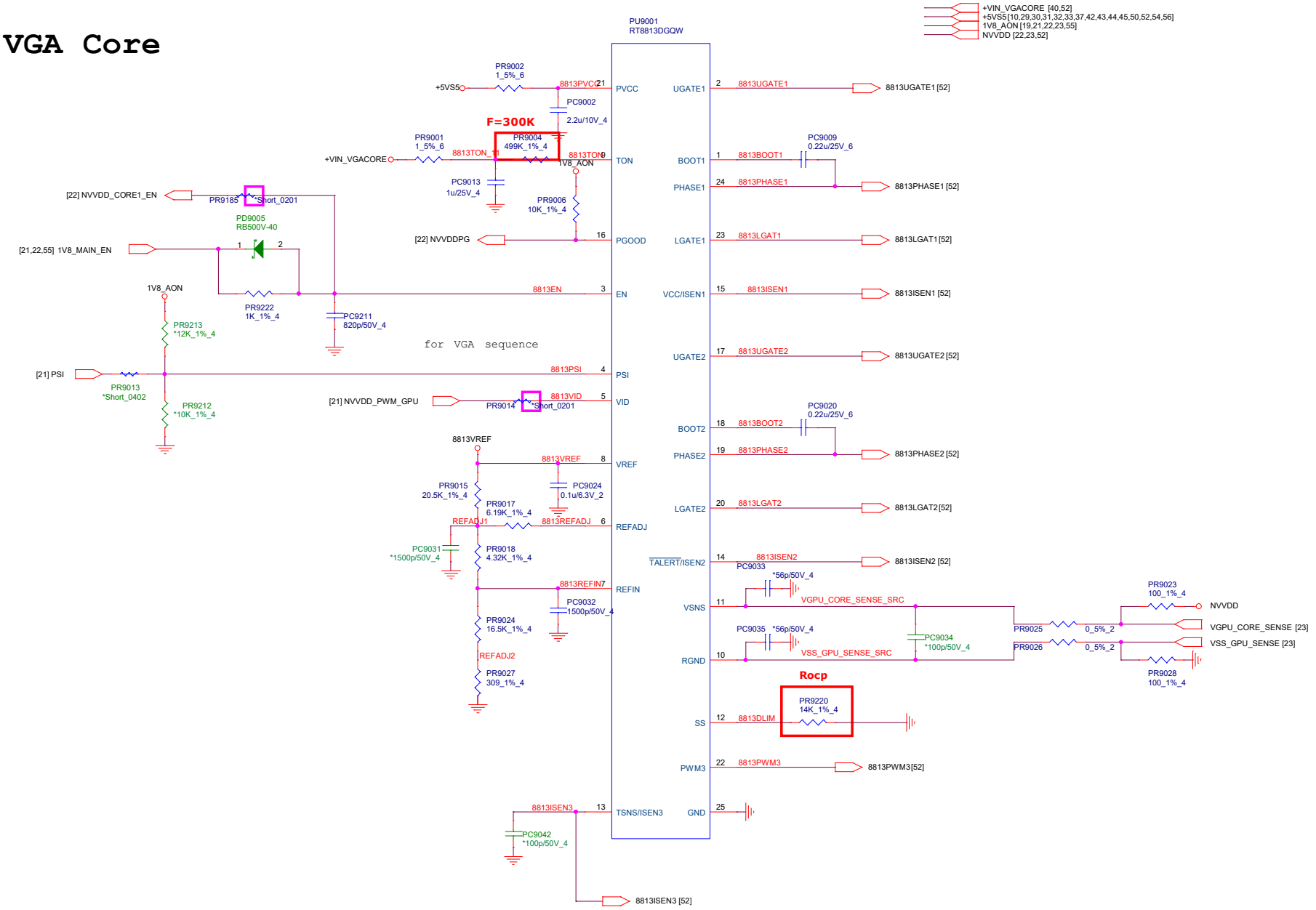


NB5

PROJECT : Y0HB
Quanta Computer Inc.

Size	Document Number	Rev
	Load switch IC(APL3523A)	1A
Date: Monday, April 09, 2018	Sheet 50 of 56	

VGA Core



NB5	**PROJECT : WBC** Quanta Computer Inc.	
Size: Custom	Document Number: **NVVDD (RT8813D)**	Rev: 1A
Date: Monday, April 09, 2018	Sheet 51 of 56	

+5V [26,27,28,29,34,39,47,48,49,50]
+5VS5 [10,29,30,31,32,33,37,42,43,44,45,50,51,54,56]
NVVDD [22,23,51]
+VIN_VGACORE [40,51]
+VIN [26,29,39,40,41,42,43,44,45,46,47,48,49,54]

	ALL POWER CLIP	Rocp	Cout	
N17P G0	BAM69360000 ; AOE6936 ;3mR	14K/110A	????????	
N17P G1	BAM69320002 ; AOE6932 ;1.8mR	10.5K/121A	????????	Default setting

Merge NVDD & NVDDS
N17P-G1 (50W) /N17P-G0(40W)
EDP-C: 58A/48A
EDP-P: 101A/92A
OCP minimum: 121A/110A
LL=0m V/A

Rdson=3m ohm

VGA Core: Vcore: 3*330uF/9m+30 *22uF/0603

Size	Custom
Document Number	NVVDD (RT8813D)
Rev	1A
Date:	Monday, April 09, 2018
Sheet	52 of 56

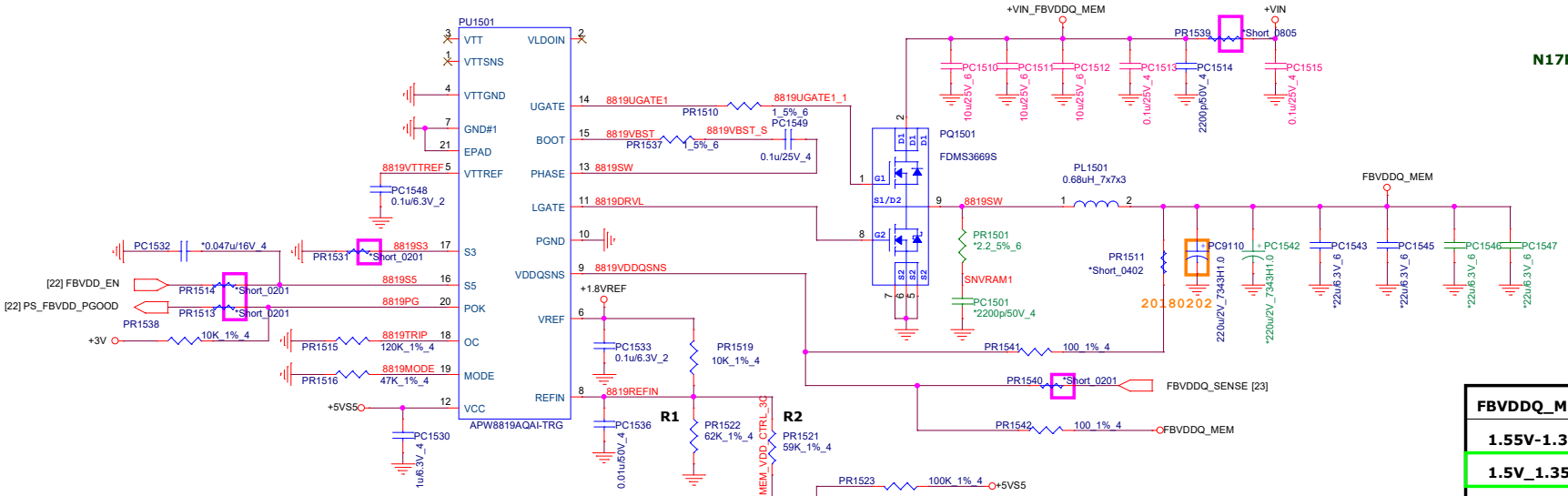
PROJECT : WBC
Quanta Computer Inc.
NB5

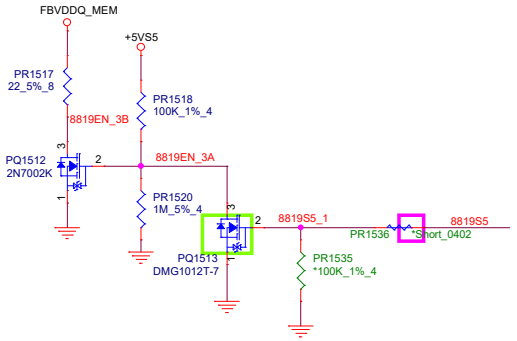
NB5

PROJECT : WBC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVVDDS (RT8816A)	1A
Date: Monday, April 09, 2018	Sheet 53 of 56	

+5VS5[10,29,30,31,32,33,37,42,43,44,45,50,51,52,54,56]
+3V[9,10,11,13,14,16,17,18,21,22,26,28,29,34,35,36,37,38,39,46,49,50,55]
FBVDDQ_MEM [20,22,23,24,25,54]
+VIN [26,29,39,40,41,42,43,44,45,46,47,48,49,52,54]





+VIN [26,29,39,40,41,42,43,44,45,46,47,48,49,52,54]
+5VS5[10,29,30,31,32,33,37,42,43,44,45,50,51,52,54,56]
FBVDDQ_MEM [20,22,23,24,25,54]

N17P-G0 MAX Q/N17P-G1 MAX Q (25W/30W/35W)
N17P-G0/N17P-G1 (40W/50W)
FBVDDQ_MEM=1.5V
EDP-C: 11A
EDP-P: 20A
OCP minimum: 24A
LL=0m V/A

FBVDDQ_MEM	R1	R2	
1.55V-1.35V	49.9K	75K	
1.5V_1.35V	62K	59K	Default setting
Fix 1.35V	30K	Open	
Fix 1.5V	50K	Open	

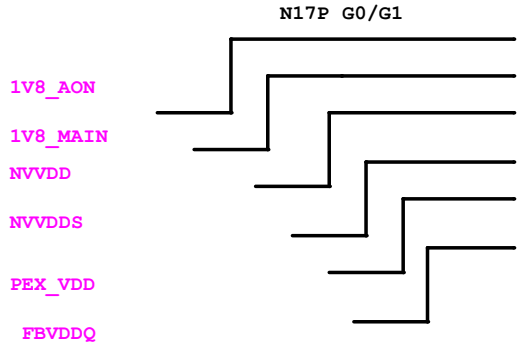
MEM_VDD_CTRL	FBVDDQ_MEM
1	1.5V_1.55V
0	1.35V

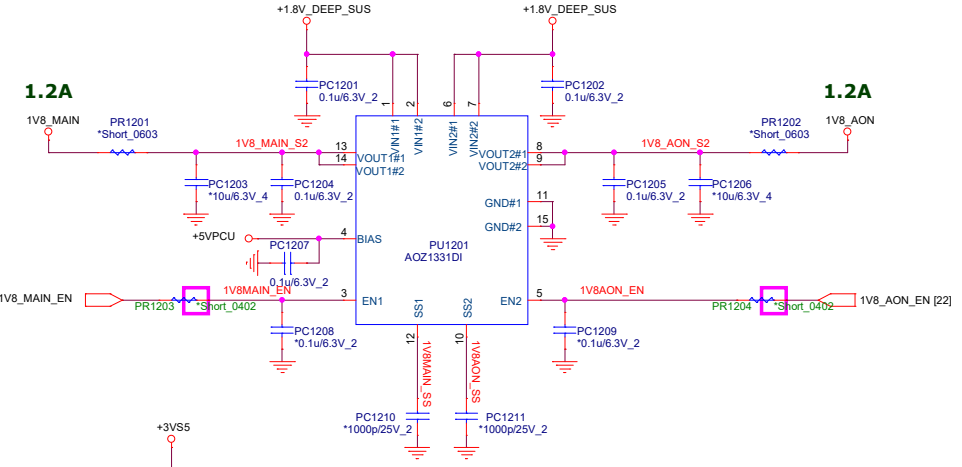
NB5

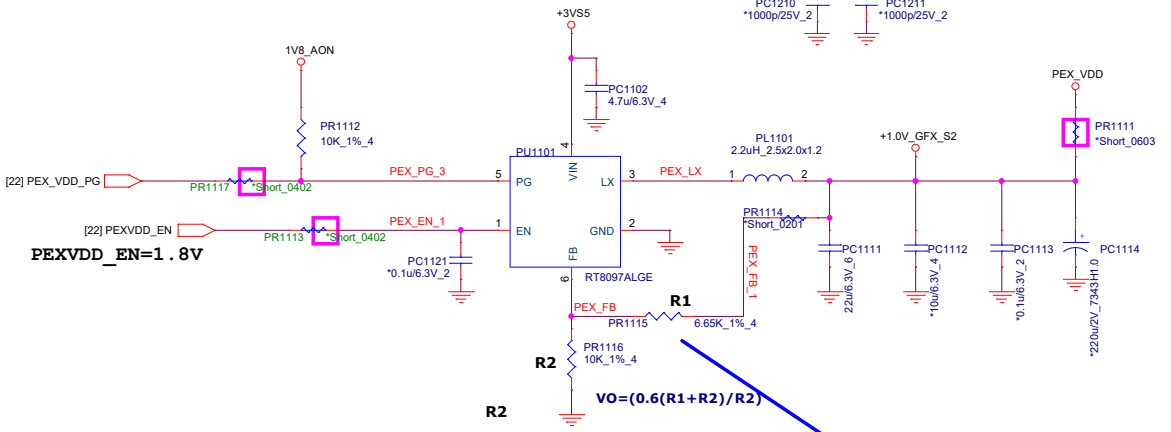
PROJECT : WBC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FBVDDQ_MEM(RT8816A)	1A
Date: Monday, April 09, 2018	Sheet 54 of 56	

+3VS5[10,12,14,28,30,31,32,34,38,42,43,44,45,46,50]
+5VS5[10,29,30,31,32,33,37,42,43,44,45,50,51,52,54,56]
1V8_MAIN [19,20,22,23,27]
1V8_AON [19,21,22,23,51]
PEX_VDD [19,21]





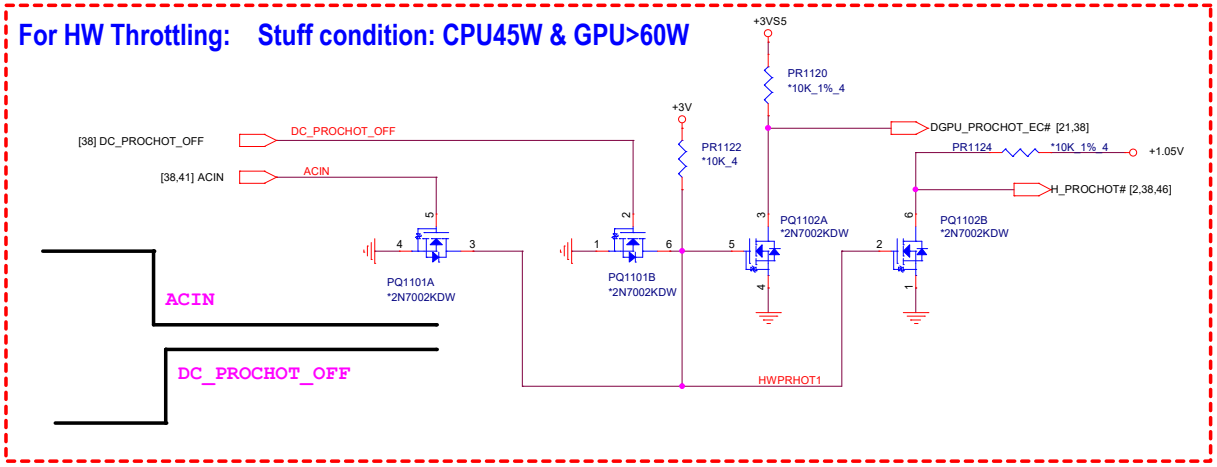


+1.0V_GFX Volt +/- 5%
EDP=3.31A
EDP_peak = TBD
+1.0V_GFX +/- 5%
TDC:0.4A
EDP:1A
OCP:3.2A

R2

	R1		
N17P N17S	6.65K	CS26652FB06	1V
N16S GTR	7.5K	CS27502FB11	1.05V

For HW Throttling: Stuff condition: CPU45W & GPU>60W



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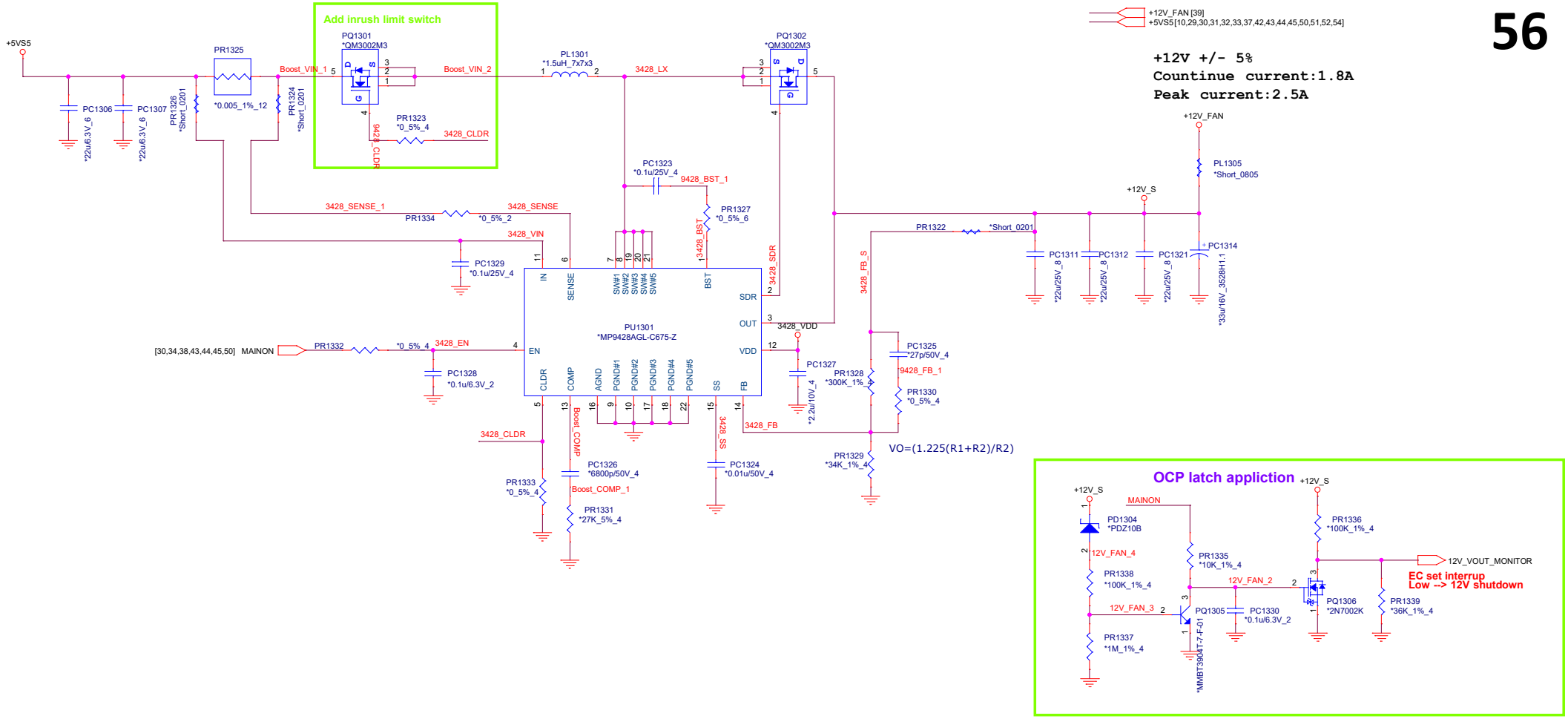
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: 1.05V_VGA/3V_VGA	Rev: 1A
Date: Monday, April 09, 2018	Sheet 55 of 56



NB5	**PROJECT : X1Q** Quanta Computer Inc.	
Size: Custom	Document Number: STORAGE MODE	Rev: 1A
Date: Monday, April 09, 2018	Sheet 56 of 56	