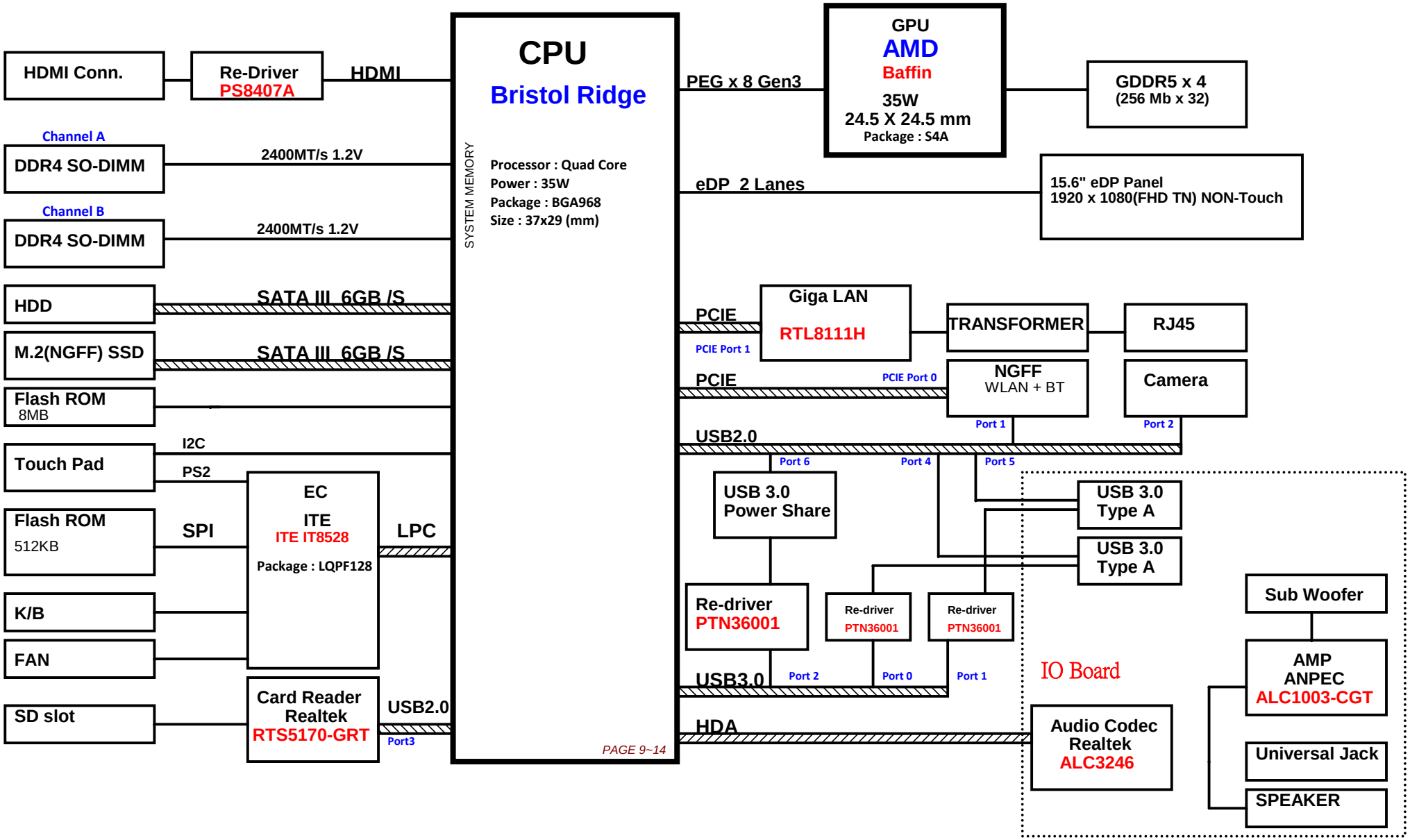
System Block Diagram – AMD Bristol Ridge



Quanta Computer Inc.		
PROJECT : AM9C		
Size	Document Number	Rev
	BLOCK DIAGRAM	A
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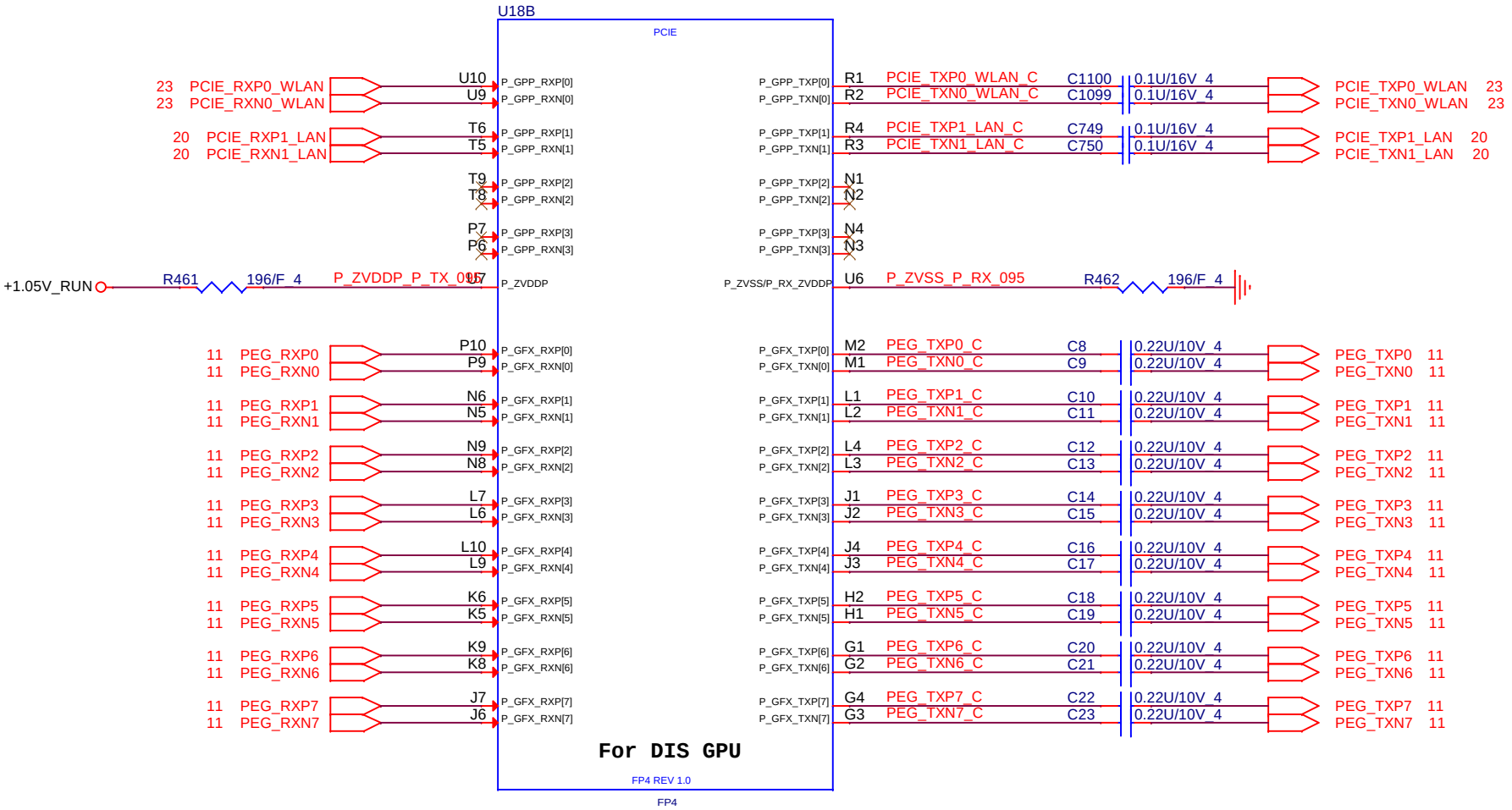

PCIE Table

Port	Function
GPP0	WLAN
GPP1	LAN
GPP2	--
GPP0	--
GFX0~7	GPU

Quanta Computer Inc.

PROJECT : AM9C

Size	Document Number	Rev
	BR & SR 1/7(PCIE)	A

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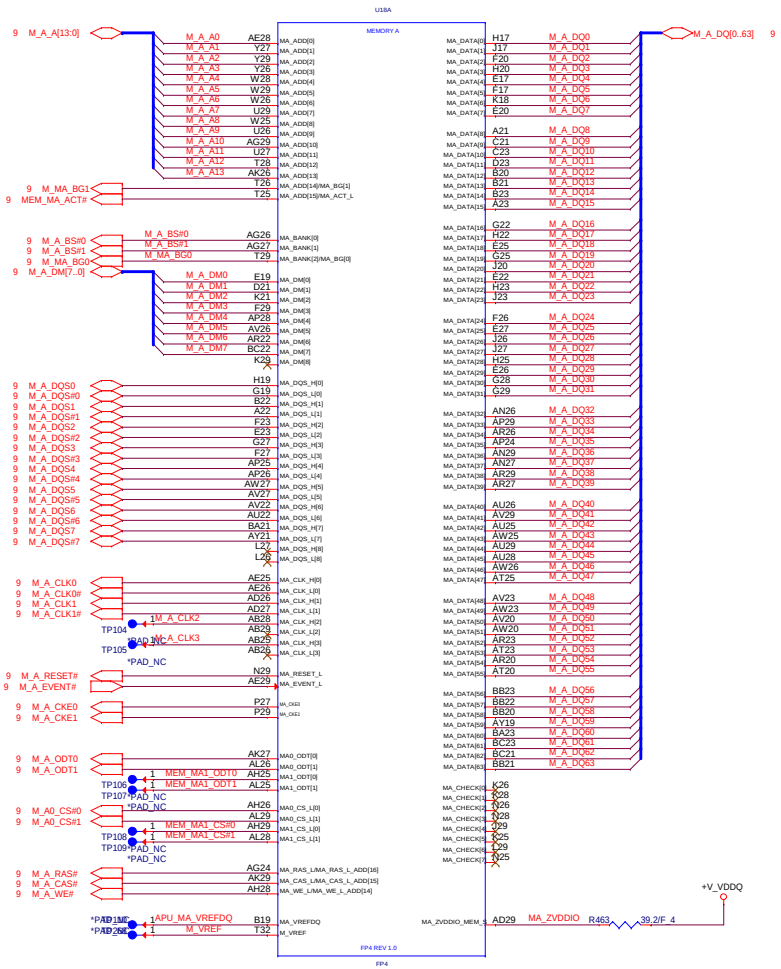

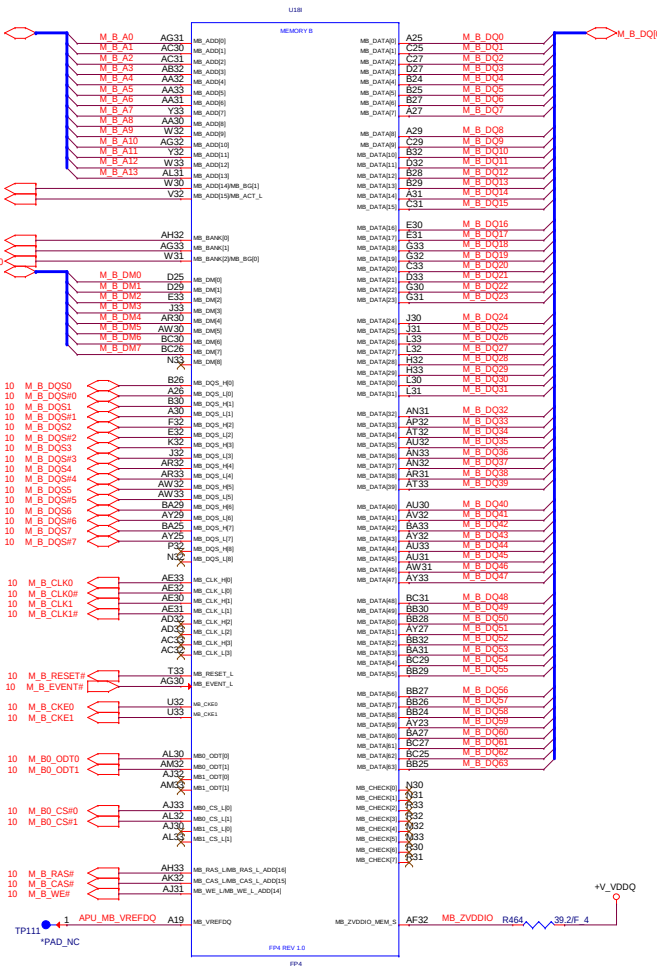

Quanta Computer Inc.			
PROJECT : AM9C			
Size	Document Number		Rev
	BR & SR 2/7(MEM)		A
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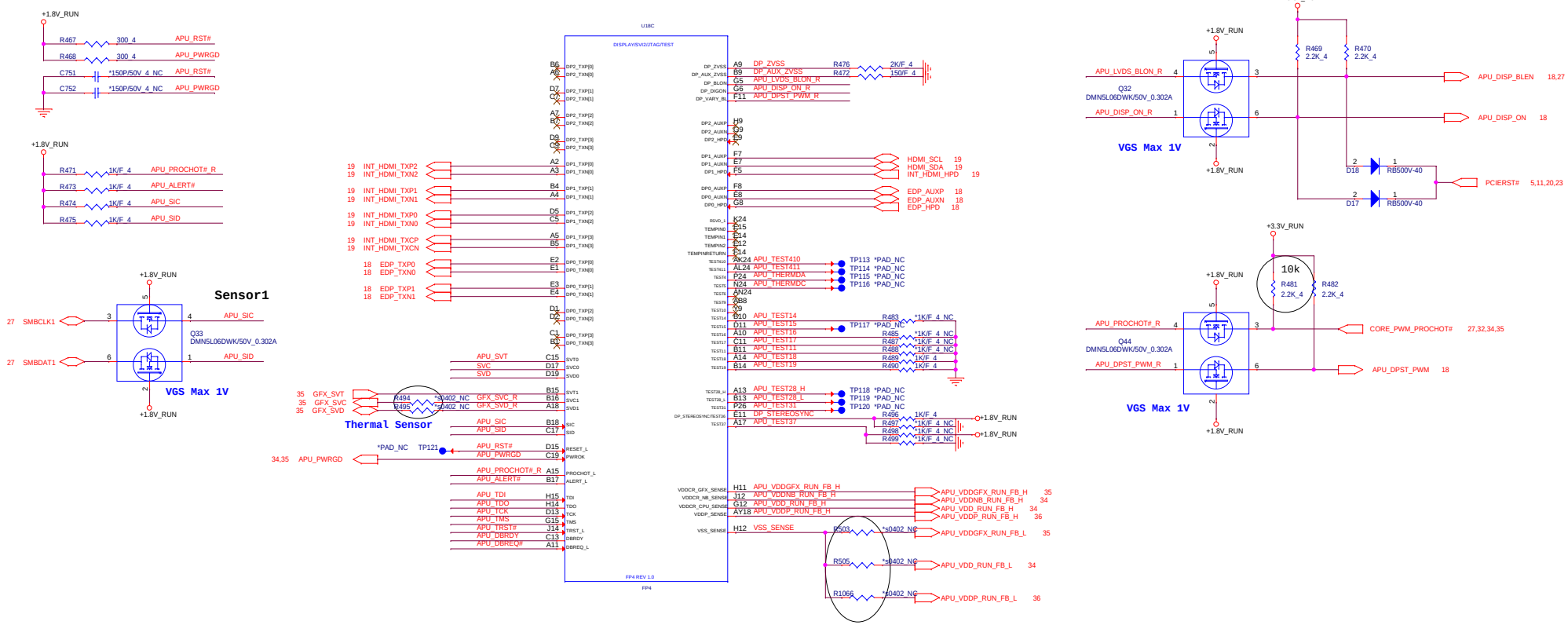
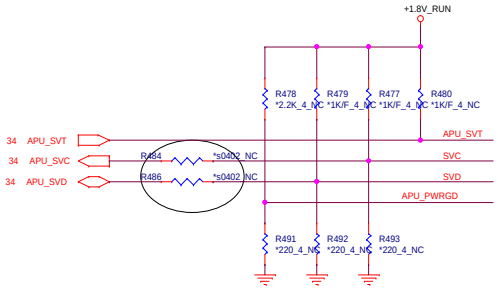
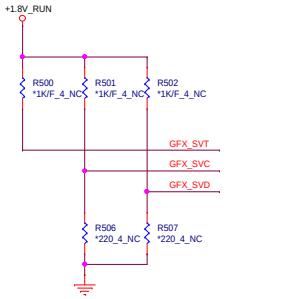




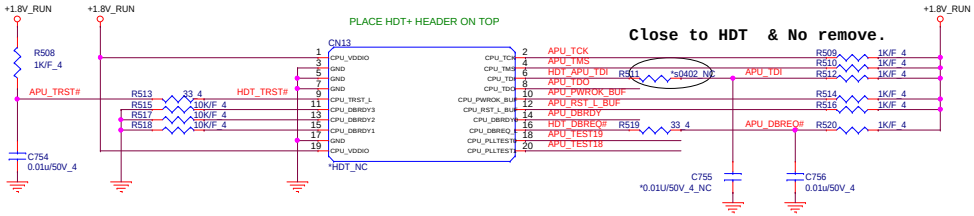
APU Serial VID

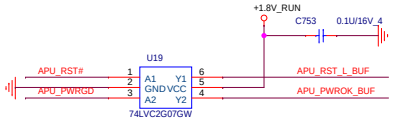


APU Serial VID (GFX)

HDT+ Connector for Debug only

Can remove on MP





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Size	Document Number: BR & SR 3/7(DIS/MISC)	Rev: A
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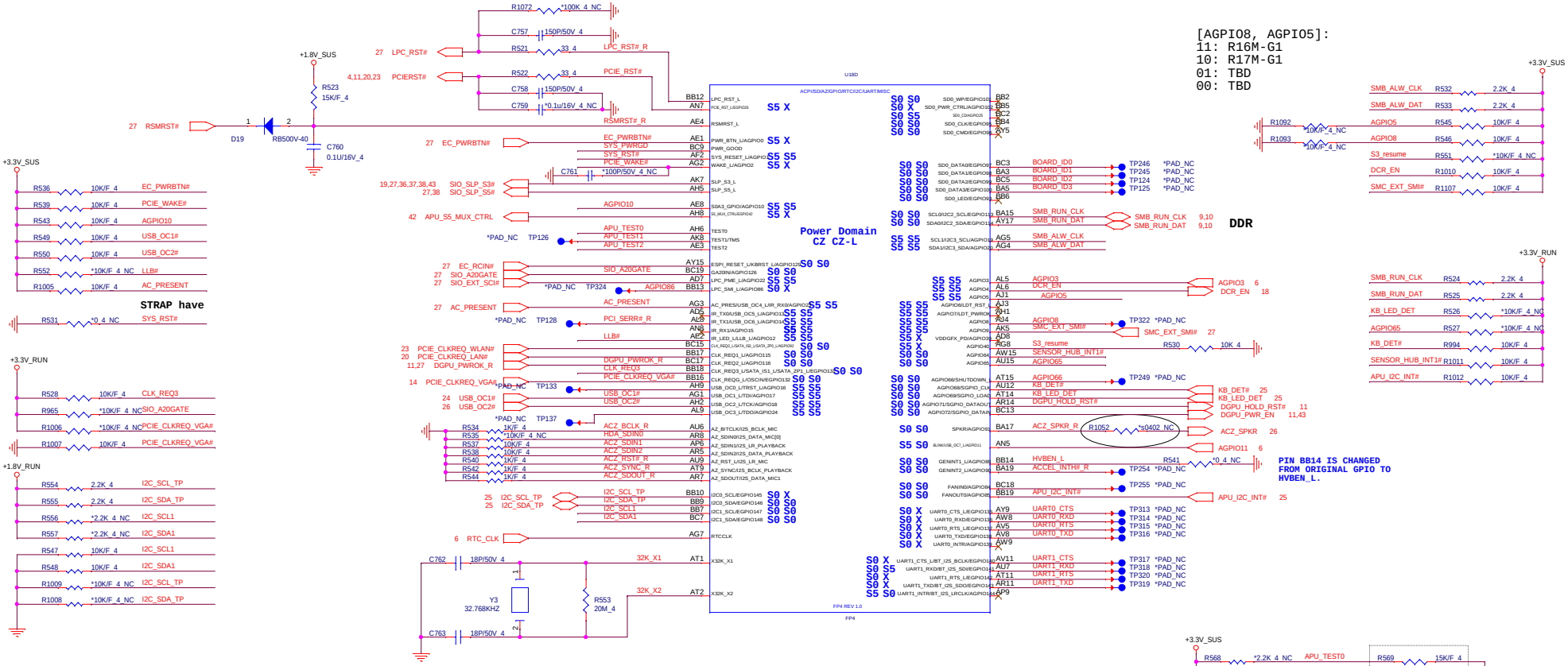
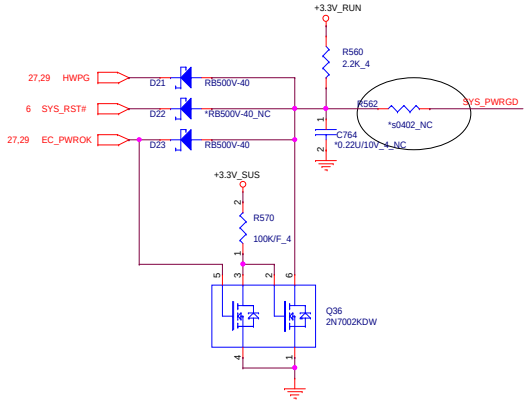
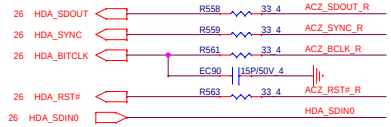


SYS PWRGD



HDA INTERFACE



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

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	BR & SR 4/7(GPIO/AZ/UART)	A

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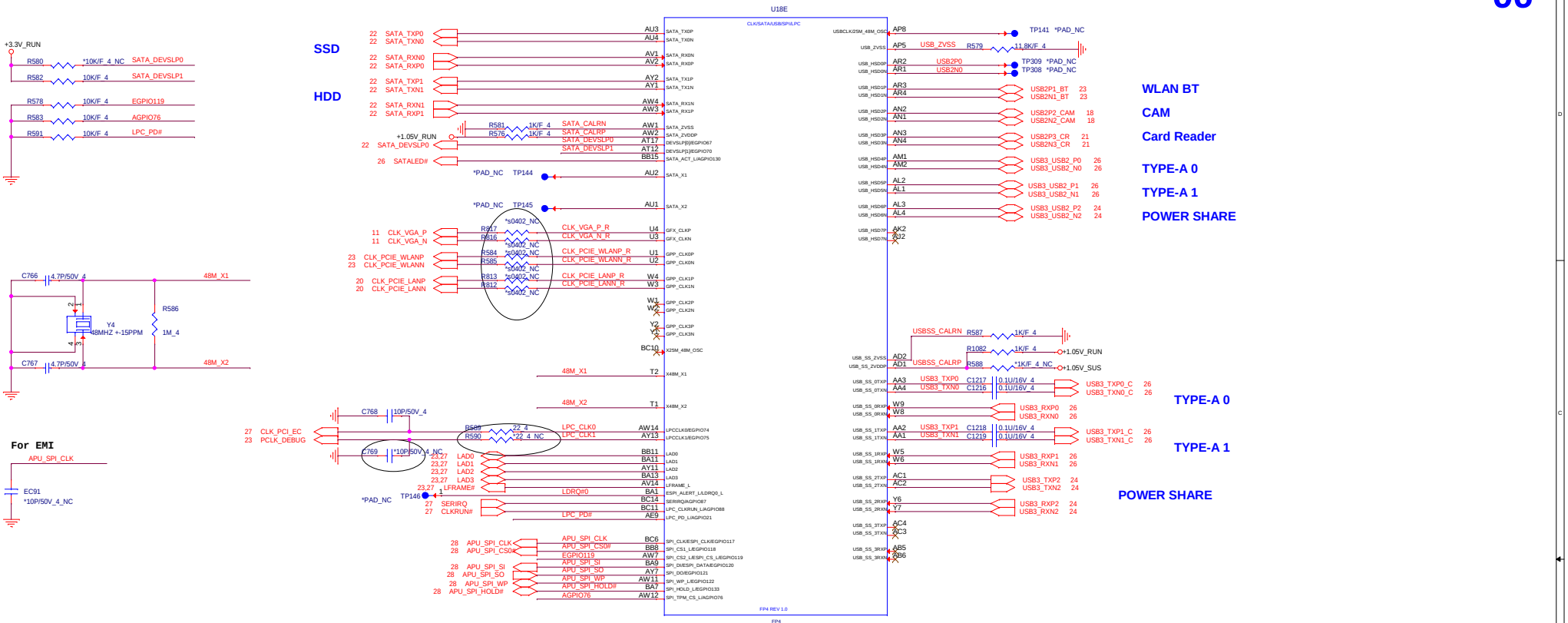
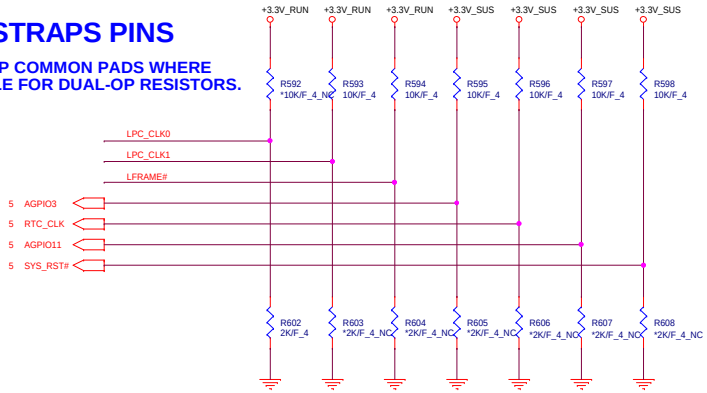


STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 (Int Pull-Up)		RTC_CLK (Int Pull-Up)	AGPIO11=BLINK (Int Pull-Up)	SYS_RST# (Int Pull-Up)
				CZ-L	BR & SR			
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks	SPI ROM	1.8V SPI ROM	Enhanced reset logic (for quicker S5 resume	Coin battery is on board.	LDT_RST#/LDT_PWRGD output to APU	normal reset mode
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM	Default to traditional reset logic	Coin battery is not on board.	LDT_RST#/LDT_PWRGD output to Pads	short reset mode

VDDIO_MEM_S3 :
22 uf*11
0.22 uf*10
180pf*3

VDDIO_MEM-DDR4:2.5A

+V_VDDQ

U18F

3A

22~39A

C785 22U/6.3V/X5R_6 C771 22U/6.3V/X5R_6 C786 22U/6.3V/X5R_6 C772 22U/6.3V/X5R_6 C773 22U/6.3V/X5R_6 C787 22U/6.3V/X5R_6 C788 22U/6.3V/X5R_6 C789 22U/6.3V/X5R_6 C790 22U/6.3V/X5R_6 C774 22U/6.3V/X5R_6 C775 22U/6.3V/X5R_6

C782 0.22U/10V_4 C798 0.22U/10V_4 C799 0.22U/10V_4 C783 0.22U/10V_4 C800 0.22U/10V_4 C784 0.22U/10V_4 C801 180P/50V_4

BOTTOM SIDE DECOUPLING UNDER APU

C811 0.22U/10V_4 C812 0.22U/10V_4 C813 0.22U/10V_4 C814 0.22U/10V_4 C815 180P/50V_4 C816 180P/50V_4

DECOUPLING BETWEEN PROCESSOR AND DIMMs
ACROSS VDDNB AND VSS SPLIT

P25 P28 T24 T27 U25 U28 V30 V33 W24 W27 Y25 Y28 Y30 AB24 AB27 AB30 AB33 AD25 AD28 AD30 AE24 AE27 AF30 AF33 AG25 AG28 AH24 AH27 AH30 AK25 AK28 AK30 AK33 AL27 AM30

+APU_VDDIO_AZ — AR19 — 0.2A
+VDDP_GFX — AE6 AE5 — 1.5A
+APU_VDD_33 — AP19 AP21 — 0.2A
+1.8V_RUN — AP16 AP18 — 1.5A
+1.8V_SUS — AP10 AR9 — 0.5A
+APU_VDD_33_S5 — AP15 AR15 — 0.2A
+VDDP_S5 — AN12 AP12 — 0.8A
+VDDCR_FCH_S5_R — AP13 AR12 — 0.2A
+1.05V_RUN — AW19 AU17 AU19 AV17 AV19 AW17 — 7A

AL12 AL13 AL15 AL18 AL21 AN13 AN16 AN19 AN22 — 12A

AR17 — +VDDBT_RTC

U8 W7 W12 W15 W18 V21 Y8 Y10 Y13 Y16 Y19 Y22 AB7 AB9 AB12 AB15 AB18 AB21 AD6 AD10 AD13 AD16 AD19 AD22 AE7 AE12 AK9 AG10 AK10 AG13 AK13 AG16 AK16 AG19 AK19 AG22 AH7 AE18 AE21 AH21 AG6 AH12 AN6 AH15 AH18 AL7 AK6 AE15

22~30A

L8 L13 L16 L19 L22 N7 N12 N15 N18 N21 P8 P13 P16 P19 P22 T7 F12 F15 G11 G14 J8 J9 J11 K7 K12 K13 K15 K16 T12 T15 T18 T21 U13 U16 U19 U22 K19

FP4 REV 1.0
FP4

+1.05V_RUN

BOTTOM SIDE DECOUPLING UNDER APU

VDDP :
10 uf*4
0.22 uf*6
180pf*1

C819 10U/6.3V_4 C820 10U/6.3V_4 C821 10U/6.3V_4 C822 10U/6.3V_4

C823 0.22U/10V_4 C824 0.22U/10V_4 C825 0.22U/10V_4 C826 0.22U/10V_4 C827 0.22U/10V_4 C828 0.22U/10V_4 C829 180P/50V_4

+VDDCR_NB

BOTTOM SIDE DECOUPLING UNDER APU

VDDCR_GFX :
47uf*4
22 uf*3
0.22 uf*8
180pf*1

C860 22U/6.3V/X5R_6 C862 22U/6.3V/X5R_6 C863 47U/4V/X5R_6

C1209 22U/6.3V/X5R_6 C864 0.22U/10V_4 C865 0.22U/10V_4 C866 0.22U/10V_4 C867 0.22U/10V_4 C868 0.22U/10V_4 C869 0.22U/10V_4 C870 0.22U/10V_4 C871 0.22U/10V_4 C872 180P/50V_4

C1200 47U/4V/X5R_6 C1202 47U/4V/X5R_6 C1206 47U/4V/X5R_6

+VDDCR_CPU

VDDCR_CPU :
47uf*6
22 uf*9
0.22 uf*8
180pf*1

C792 47U/4V/X5R_6 C793 47U/4V/X5R_6 C776 47U/4V/X5R_6 C777 22U/6.3V/X5R_6 C779 22U/6.3V/X5R_6 C1125 47U/4V/X5R_6

C802 0.22U/10V_4 C803 0.22U/10V_4 C804 0.22U/10V_4 C805 0.22U/10V_4 C806 0.22U/10V_4 C807 0.22U/10V_4 C808 0.22U/10V_4 C809 0.22U/10V_4 C810 180P/50V_4

C1108 47U/4V/X5R_6 C1107 22U/6.3V/X5R_6 C1111 47U/4V/X5R_6 C1109 22U/6.3V/X5R_6 C1110 22U/6.3V/X5R_6 C1112 22U/6.3V/X5R_6 C1113 22U/6.3V/X5R_6 C1122 22U/6.3V/X5R_6 C1123 22U/6.3V/X5R_6

BOTTOM SIDE DECOUPLING UNDER APU

+VDDCR_GFX

VDDCR_GFX :
22 uf*20
0.22 uf*9
180pf*1

C833 22U/6.3V/X5R_6 C834 22U/6.3V/X5R_6 C835 22U/6.3V/X5R_6 C836 22U/6.3V/X5R_6 C837 22U/6.3V/X5R_6 C838 22U/6.3V/X5R_6 C839 22U/6.3V/X5R_6 C840 22U/6.3V/X5R_6 C841 22U/6.3V/X5R_6 C1131 22U/6.3V/X5R_6

C845 0.22U/10V_4 C846 0.22U/10V_4 C847 0.22U/10V_4 C848 0.22U/10V_4 C849 0.22U/10V_4 C850 0.22U/10V_4 C851 0.22U/10V_4 C852 0.22U/10V_4 C853 0.22U/10V_4 C854 180P/50V_4

C1114 22U/6.3V/X5R_6 C1115 22U/6.3V/X5R_6 C1116 22U/6.3V/X5R_6 C1117 22U/6.3V/X5R_6 C1118 22U/6.3V/X5R_6 C1119 22U/6.3V/X5R_6 C1120 22U/6.3V/X5R_6 C1121 22U/6.3V/X5R_6 C1126 22U/6.3V/X5R_6 C1127 22U/6.3V/X5R_6

+VDDBT_RTC

R621 1K/F_4 +1.5V_RTC

27 EC_RTC_RST

R622 100K/F_4

Q37 2N7002K

C873 0.22U/10V_4 C875 1U/6.3V_4

+1.5V_SUS +APU_VDDIO_AZ **1.5V For HDA Only**

R618 *s0402_NC

C830 1U/6.3V_4 C831 1U/6.3V_4 C832 1U/6.3V_4

+3.3V_RUN +APU_VDD_33

R623 *s0402_NC

C882 10U/6.3V_4

+1.8V_SUS

C880 10U/6.3V_4 C881 0.22U/10V_4

+1.05V_SUS +VDDP_S5

R625 *s0603_NC

C885 10U/6.3V_4 C886 0.22U/10V_4

+5V_ALW C9376 0.1U/16V/X7R_4

+5V_ALW C9375 0.1U/16V/X7R_4

+PWR_SRC C9374 0.1U/25V_4

+1.05V_RUN +VDDP_GFX

R615 *s0402_NC
R616 *s0402_NC
R617 *s0402_NC

C817 10U/6.3V_4 C818 0.22U/10V_4

+1.8V_RUN

C878 10U/6.3V_4 C879 0.22U/10V_4

+3.3V_SUS +APU_VDD_33_S5

R624 *s0402_NC

C883 10U/6.3V_4 C884 0.22U/10V_4

+VDDCR_FCH_ALW +VDDCR_FCH_S5_R

R619 *s0402_NC

C842 10U/6.3V_4 C843 10U/6.3V_4 C844 0.22U/10V_4

+VDDCR_CPU

CS8 0.1U/16V/X7R_4

Stitching Cap (TOP)

CS1 0.1U/16V/X7R_4 +VDDCR_GFX +VDDCR_CPU
CS2 0.1U/16V/X7R_4 +VDDCR_CPU +VDDCR_NB
CS3 0.1U/16V/X7R_4 +V_VDDQ

Stitching Cap (BOT)

CS4 0.1U/16V/X7R_4 +VDDCR_NB
CS6 0.1U/25V_4 +PWR_SRC

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Size	Document Number	Rev
	BR & SR 6/7 (POWER)	A
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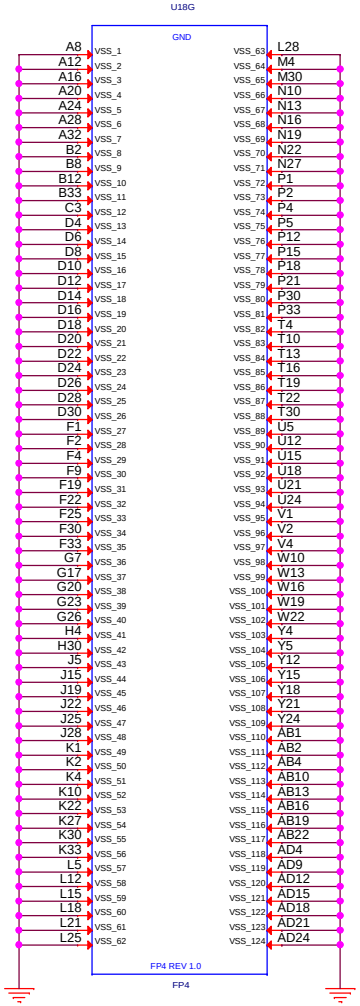

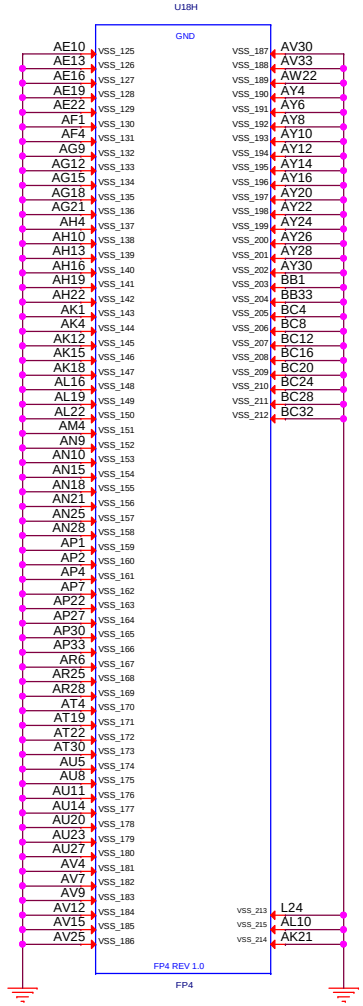

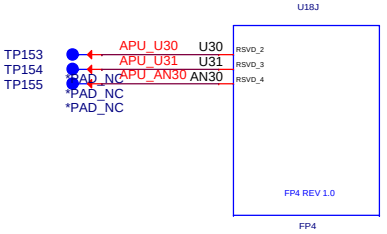

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Size	Document Number	Rev
	BR & SR 7/7 (GND)	A

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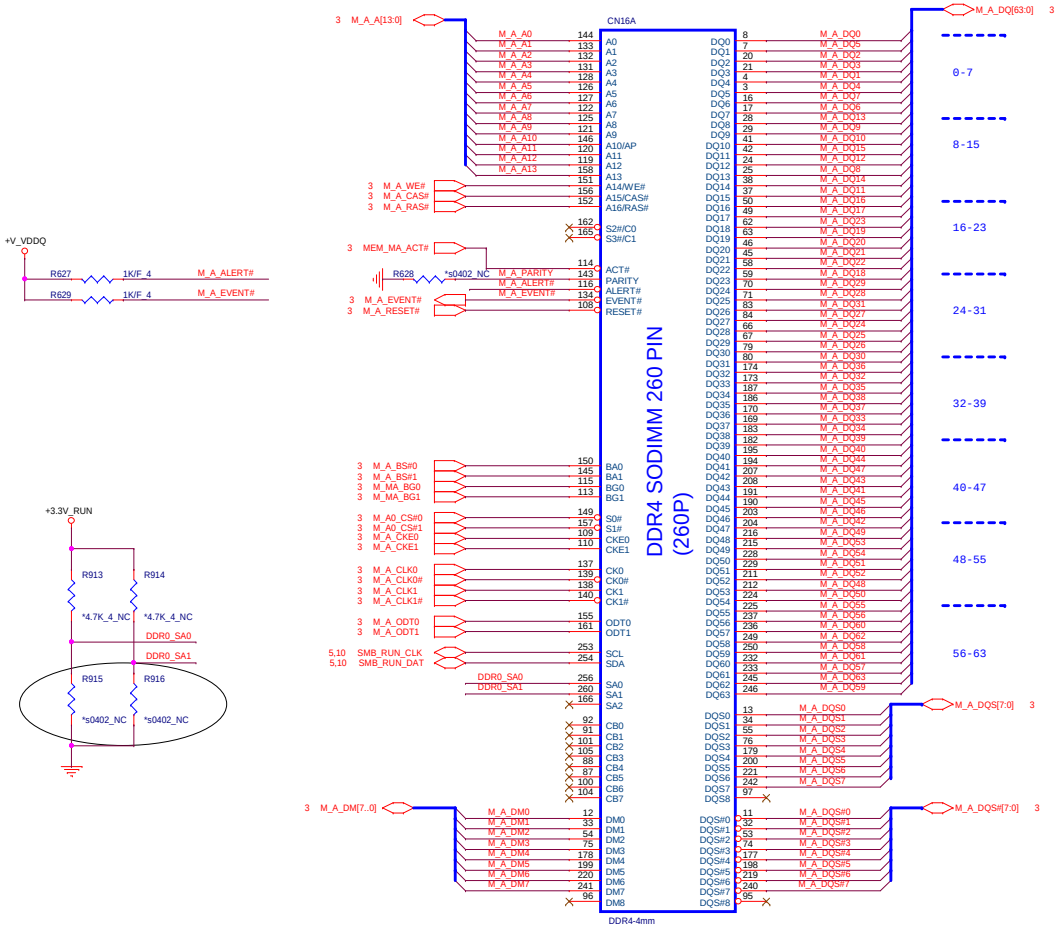
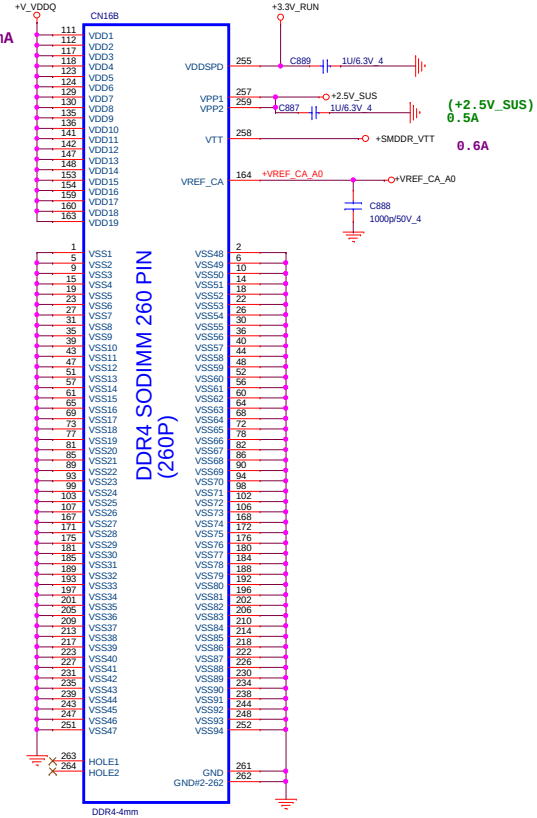
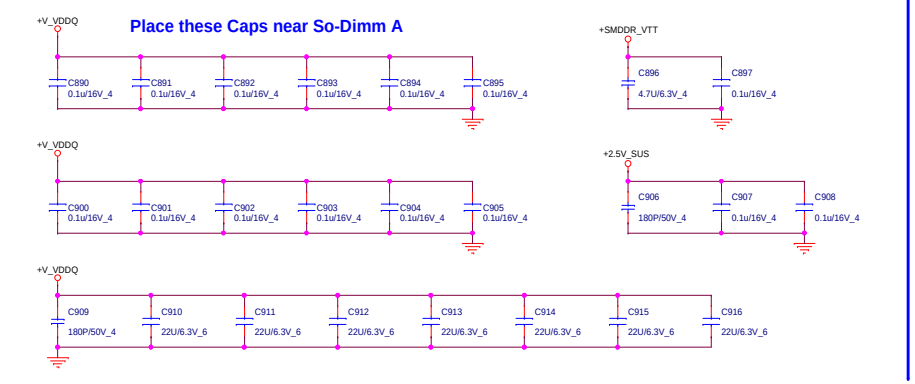
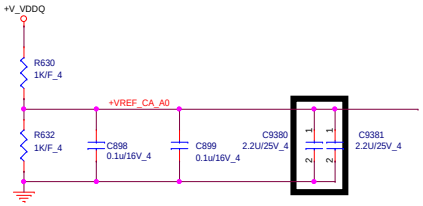
SODIMM (SDM) -4mm

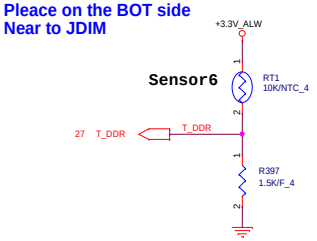
09











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Size	Document Number	Rev
	DDR4 DIMM A0	A

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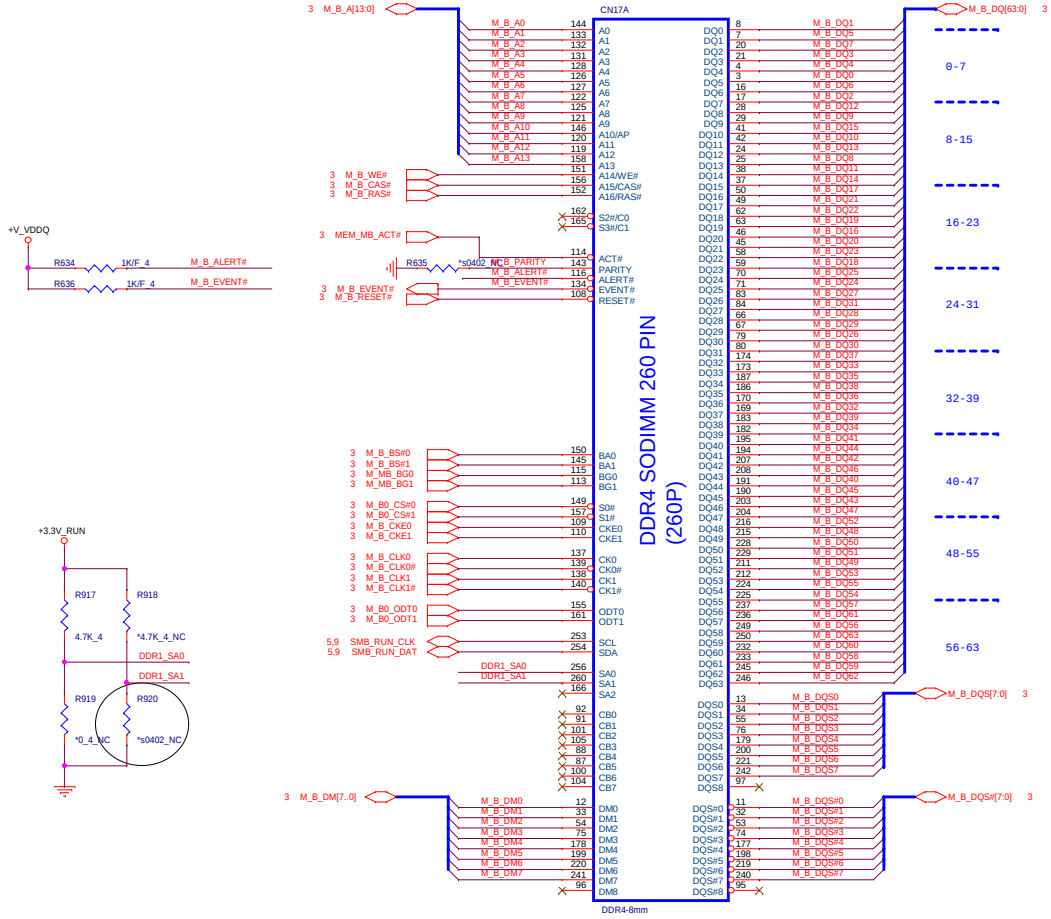
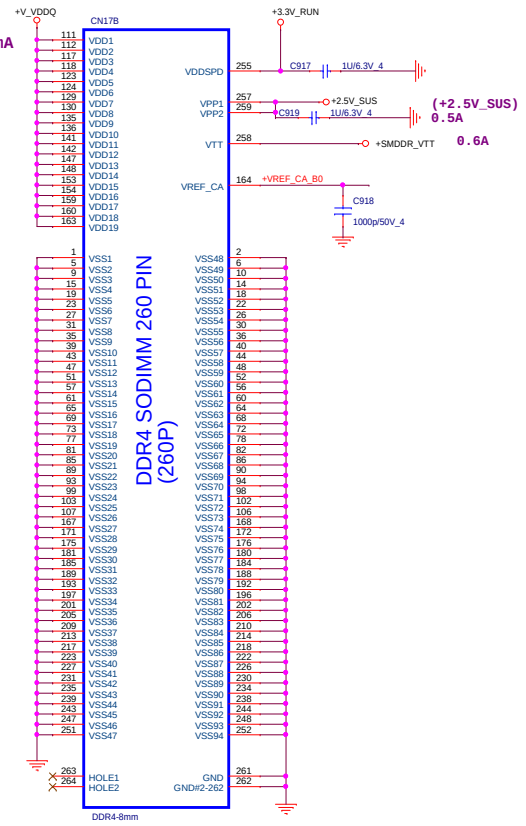
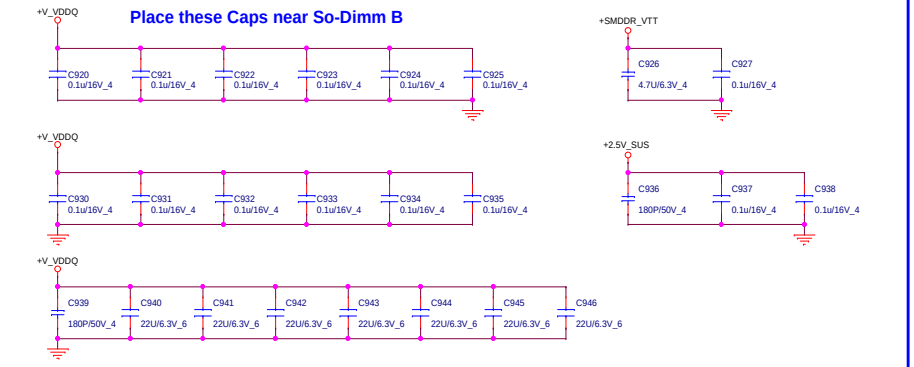
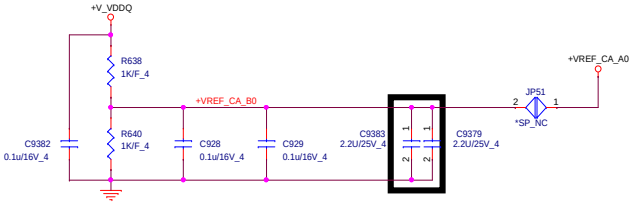
SODIMM (SDM)-8mm









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Size	Document Number	Rev
	DDR4 DIMM B0	A

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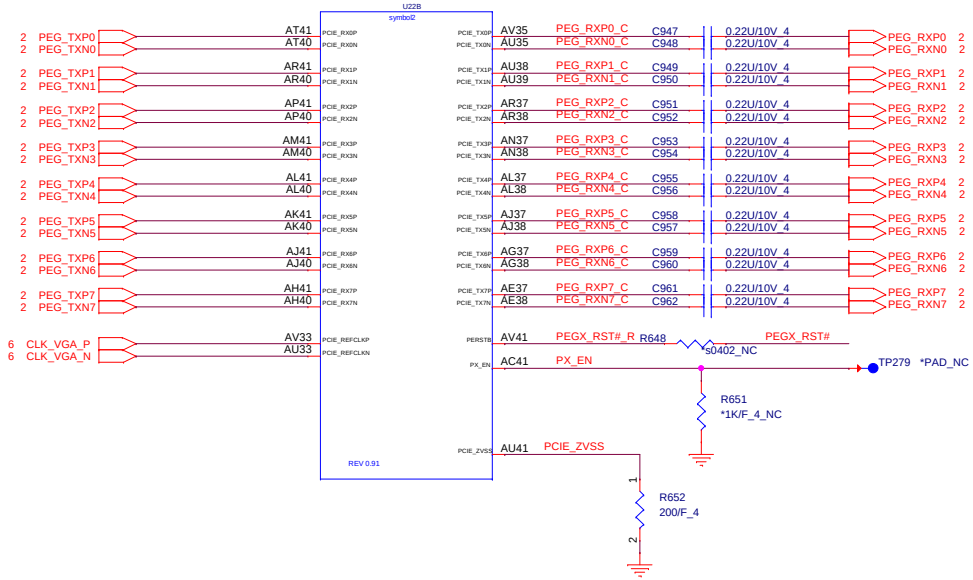
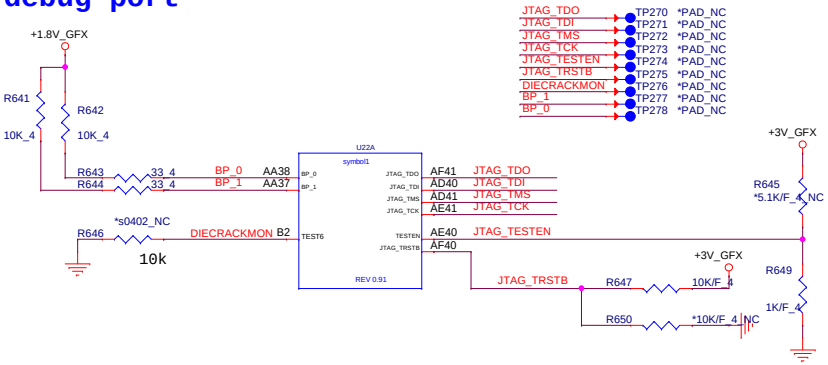
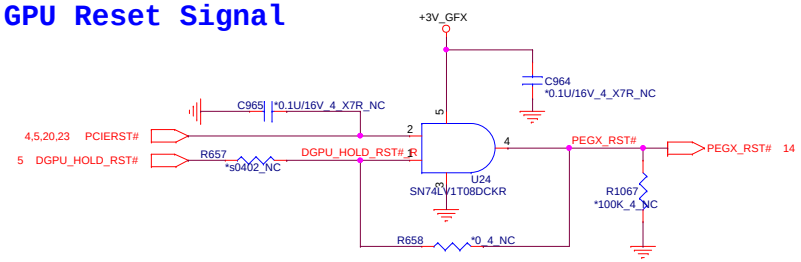


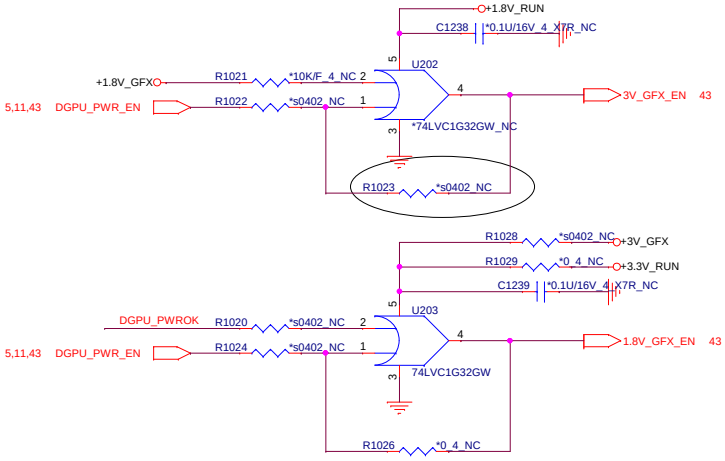
debug port

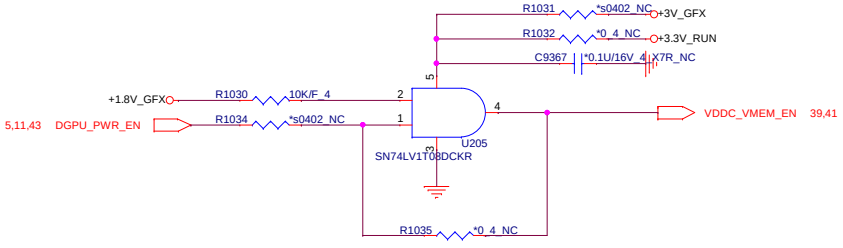


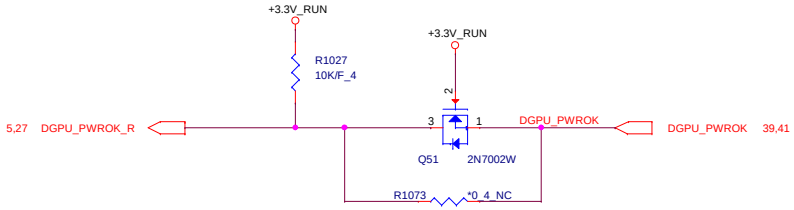
GPU Reset Signal



GPU Power Sequence Signal







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	R16M-G1-50 - 1/5 (PCIE)	A
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17 DQA0_[31..0]
17 DQB0_[31..0]
17 MAA0_[8..0]
17 MAB0_[8..0]
DQA1_[31..0] 17
DQB1_[31..0] 17
MAA1_[8..0] 17
MAB1_[8..0] 17

U22C
symbol3

DQA0_0	L34	DQA0_0	DQA1_0	B27	DQA1_0
DQA0_1	L37	DQA0_1	DQA1_1	A27	DQA1_1
DQA0_2	L38	DQA0_2	DQA1_2	B26	DQA1_2
DQA0_3	J35	DQA0_3	DQA1_3	A26	DQA1_3
DQA0_4	G37	DQA0_4	DQA1_4	A24	DQA1_4
DQA0_5	E38	DQA0_5	DQA1_5	B23	DQA1_5
DQA0_6	E35	DQA0_6	DQA1_6	A23	DQA1_6
DQA0_7	D35	DQA0_7	DQA1_7	B22	DQA1_7
DQA0_8	H41	DQA0_8	DQA1_8	B20	DQA1_8
DQA0_9	H40	DQA0_9	DQA1_9	A20	DQA1_9
DQA0_10	G41	DQA0_10	DQA1_10	B19	DQA1_10
DQA0_11	G40	DQA0_11	DQA1_11	A19	DQA1_11
DQA0_12	E40	DQA0_12	DQA1_12	B17	DQA1_12
DQA0_13	D41	DQA0_13	DQA1_13	A16	DQA1_13
DQA0_14	D40	DQA0_14	DQA1_14	B16	DQA1_14
DQA0_15	C41	DQA0_15	DQA1_15	A15	DQA1_15
DQA0_16	C40	DQA0_16	DQA1_16	B15	DQA1_16
DQA0_17	B39	DQA0_17	DQA1_17	A14	DQA1_17
DQA0_18	A39	DQA0_18	DQA1_18	B14	DQA1_18
DQA0_19	B38	DQA0_19	DQA1_19	B13	DQA1_19
DQA0_20	B36	DQA0_20	DQA1_20	A11	DQA1_20
DQA0_21	A36	DQA0_21	DQA1_21	B11	DQA1_21
DQA0_22	B35	DQA0_22	DQA1_22	A10	DQA1_22
DQA0_23	A35	DQA0_23	DQA1_23	B10	DQA1_23
DQA0_24	B33	DQA0_24	DQA1_24	B8	DQA1_24
DQA0_25	B32	DQA0_25	DQA1_25	A7	DQA1_25
DQA0_26	A32	DQA0_26	DQA1_26	B7	DQA1_26
DQA0_27	B31	DQA0_27	DQA1_27	A6	DQA1_27
DQA0_28	A30	DQA0_28	DQA1_28	A4	DQA1_28
DQA0_29	B29	DQA0_29	DQA1_29	B4	DQA1_29
DQA0_30	B28	DQA0_30	DQA1_30	A3	DQA1_30
DQA0_31	A28	DQA0_31	DQA1_31	B3	DQA1_31
MAA0_0	G25	MAA0_0	MAA1_0	E15	MAA1_0
MAA0_1	H25	MAA0_1	MAA1_1	H15	MAA1_1
MAA0_2	E27	MAA0_2	MAA1_2	G13	MAA1_2
MAA0_3	D27	MAA0_3	MAA1_3	D13	MAA1_3
MAA0_4	D29	MAA0_4	MAA1_4	H11	MAA1_4
MAA0_5	H27	MAA0_5	MAA1_5	H13	MAA1_5
MAA0_6	H23	MAA0_6	MAA1_6	H17	MAA1_6
MAA0_7	E23	MAA0_7	MAA1_7	G17	MAA1_7
MAA0_8	D25	MAA0_8	MAA1_8	D15	MAA1_8
H28		MAA0_9		E11	

17 WCKA0_0	WCKA0_0	D33	WCKA0_0	A22	WCKA1_0	WCKA1_0 17
17 WCKA0B_0	WCKA0B_0	E33	WCKA0B_0	B21	WCKA1B_0	WCKA1B_0 17
17 WCKA0_1	WCKA0_1	A34	WCKA0_1	A8	WCKA1_1	WCKA1_1 17
17 WCKA0B_1	WCKA0B_1	B34	WCKA0B_1	B9	WCKA1B_1	WCKA1B_1 17
17 EDCA0_0	EDCA0_0	G38	EDCA0_0	B24	EDCA1_0	EDCA1_0 17
17 EDCA0_1	EDCA0_1	F41	EDCA0_1	A18	EDCA1_1	EDCA1_1 17
17 EDCA0_2	EDCA0_2	B37	EDCA0_2	B12	EDCA1_2	EDCA1_2 17
17 EDCA0_3	EDCA0_3	A31	EDCA0_3	B6	EDCA1_3	EDCA1_3 17
17 DDBIA0_0	DDBIA0_0	J38	DDBIA0_0	B25	DDBIA1_0	DDBIA1_0 17
17 DDBIA0_1	DDBIA0_1	F40	DDBIA0_1	B18	DDBIA1_1	DDBIA1_1 17
17 DDBIA0_2	DDBIA0_2	A38	DDBIA0_2	A12	DDBIA1_2	DDBIA1_2 17
17 DDBIA0_3	DDBIA0_3	B30	DDBIA0_3	B5	DDBIA1_3	DDBIA1_3 17
17 ADBIA0	ADBIA0	H21	ADBIA0	H19	ADBIA1	ADBIA1 17
17 CSA0B_0	CSA0B_0	H31	CSA0B_0	E7	CSA1B_0	CSA1B_0 17
17 CASA0B	CASA0B	D23	CASA0B	D17	CASA1B	CASA1B 17
17 RASA0B	RASA0B	D21	RASA0B	D19	RASA1B	RASA1B 17
17 WEA0B	WEA0B	G29	WEA0B	D11	WEA1B	WEA1B 17
17 CKEA0	CKEA0	G21	CKEA0	E19	CKEA1	CKEA1 17
17 CLKA0	CLKA0	E31	CLKA0	D7	CLKA1	CLKA1 17
17 CLKA0B	CLKA0B	D31	CLKA0B	D9	CLKA1B	CLKA1B 17
R666 120/F_4	MEM_CALRA	K15	MVREFDA	K17	MVREFDA	

DRAM_A_RST R669 10/F_4 DRAM_RST_A_R L32 DRAM_RSTA
R674 5.1K/F_4
REV 0.91

+1.35V_GFX
R664 40.2/F_4
C1231 1U/6.3V_4
R670 100/F_4

U22D
symbol4

DQB0_0	C2	DQB0_0	DQB1_0	AH1	DQB1_0
DQB0_1	C1	DQB0_1	DQB1_1	AH2	DQB1_1
DQB0_2	D2	DQB0_2	DQB1_2	AJ2	DQB1_2
DQB0_3	D1	DQB0_3	DQB1_3	AK1	DQB1_3
DQB0_4	F1	DQB0_4	DQB1_4	AL2	DQB1_4
DQB0_5	G2	DQB0_5	DQB1_5	AM1	DQB1_5
DQB0_6	G1	DQB0_6	DQB1_6	AM2	DQB1_6
DQB0_7	H2	DQB0_7	DQB1_7	AN2	DQB1_7
DQB0_8	K2	DQB0_8	DQB1_8	AR1	DQB1_8
DQB0_9	K1	DQB0_9	DQB1_9	AR2	DQB1_9
DQB0_10	L2	DQB0_10	DQB1_10	AT1	DQB1_10
DQB0_11	L1	DQB0_11	DQB1_11	AT2	DQB1_11
DQB0_12	N2	DQB0_12	DQB1_12	AV2	DQB1_12
DQB0_13	P2	DQB0_13	DQB1_13	AW1	DQB1_13
DQB0_14	P1	DQB0_14	DQB1_14	AW2	DQB1_14
DQB0_15	R2	DQB0_15	DQB1_15	AY3	DQB1_15
DQB0_16	R1	DQB0_16	DQB1_16	BA3	DQB1_16
DQB0_17	T2	DQB0_17	DQB1_17	AY4	DQB1_17
DQB0_18	T1	DQB0_18	DQB1_18	BA4	DQB1_18
DQB0_19	U2	DQB0_19	DQB1_19	AY5	DQB1_19
DQB0_20	W1	DQB0_20	DQB1_20	BA7	DQB1_20
DQB0_21	W2	DQB0_21	DQB1_21	AY7	DQB1_21
DQB0_22	Y1	DQB0_22	DQB1_22	AY8	DQB1_22
DQB0_23	Y2	DQB0_23	DQB1_23	BA8	DQB1_23
DQB0_24	AB2	DQB0_24	DQB1_24	AR4	DQB1_24
DQB0_25	AC1	DQB0_25	DQB1_25	AR5	DQB1_25
DQB0_26	AC2	DQB0_26	DQB1_26	AU4	DQB1_26
DQB0_27	AD1	DQB0_27	DQB1_27	AU7	DQB1_27
DQB0_28	AF1	DQB0_28	DQB1_28	AN8	DQB1_28
DQB0_29	AF2	DQB0_29	DQB1_29	AV11	DQB1_29
DQB0_30	AG1	DQB0_30	DQB1_30	AU11	DQB1_30
DQB0_31	AG2	DQB0_31	DQB1_31	AP11	DQB1_31
MAB0_0	R5	MAB0_0	MAB1_0	AE7	MAB1_0
MAB0_1	R8	MAB0_1	MAB1_1	AE8	MAB1_1
MAB0_2	N7	MAB0_2	MAB1_2	AG5	MAB1_2
MAB0_3	N4	MAB0_3	MAB1_3	AG4	MAB1_3
MAB0_4	L8	MAB0_4	MAB1_4	AJ4	MAB1_4
MAB0_5	N8	MAB0_5	MAB1_5	AG8	MAB1_5
MAB0_6	U8	MAB0_6	MAB1_6	AC8	MAB1_6
MAB0_7	U7	MAB0_7	MAB1_7	AC5	MAB1_7
MAB0_8	R4	MAB0_8	MAB1_8	AE4	MAB1_8
L5		MAB0_9		AJ8	

17 WCKB0_0	WCKB0_0	H1	WCKB0_0	AP1	WCKB1_0	WCKB1_0 17
17 WCKB0B_0	WCKB0B_0	J2	WCKB0B_0	AP2	WCKB1B_0	WCKB1B_0 17
17 WCKB0_1	WCKB0_1	AB1	WCKB0_1	AN4	WCKB1_1	WCKB1_1 17
17 WCKB0B_1	WCKB0B_1	AA2	WCKB0B_1	AN5	WCKB1B_1	WCKB1B_1 17
17 EDCB0_0	EDCB0_0	F2	EDCB0_0	AL1	EDCB1_0	EDCB1_0 17
17 EDCB0_1	EDCB0_1	M2	EDCB0_1	AU2	EDCB1_1	EDCB1_1 17
17 EDCB0_2	EDCB0_2	V1	EDCB0_2	BA6	EDCB1_2	EDCB1_2 17
17 EDCB0_3	EDCB0_3	AD2	EDCB0_3	AV7	EDCB1_3	EDCB1_3 17
17 DDBIB0_0	DDBIB0_0	E2	DDBIB0_0	AK2	DDBIB1_0	DDBIB1_0 17
17 DDBIB0_1	DDBIB0_1	M1	DDBIB0_1	AV1	DDBIB1_1	DDBIB1_1 17
17 DDBIB0_2	DDBIB0_2	V2	DDBIB0_2	AY6	DDBIB1_2	DDBIB1_2 17
17 DDBIB0_3	DDBIB0_3	AE2	DDBIB0_3	AV9	DDBIB1_3	DDBIB1_3 17
17 ADBIB0	ADBIB0	W8	ADBIB0	AA8	ADBIB1	ADBIB1 17
17 CSB0B_0	CSB0B_0	G5	CSB0B_0	AL8	CSB1B_0	CSB1B_0 17
17 CASB0B	CASB0B	U4	CASB0B	AC4	CASB1B	CASB1B 17
17 RASB0B	RASB0B	W4	RASB0B	AA4	RASB1B	RASB1B 17
17 WEB0B	WEB0B	L4	WEB0B	AJ7	WEB1B	WEB1B 17
17 CKEB0	CKEB0	W5	CKEB0	AA7	CKEB1	CKEB1 17
17 CLKB0	CLKB0	G4	CLKB0	AL5	CLKB1	CLKB1 17
17 CLKB0B	CLKB0B	J4	CLKB0B	AL4	CLKB1B	CLKB1B 17
R667 120/F_4	MEM_CALRB	R10	MVREFDB	U10	MVREFDB	

DRAM_B_RST R672 10/F_4 DRAM_RST_B_R AM11 DRAM_RSTB
R675 5.1K/F_4
REV 0.91

+1.35V_GFX
R665 40.2/F_4
C1232 1U/6.3V_4
R673 100/F_4

17 DRAM_RST_A R668 49.9/F_4 DRAM_A_RST
C968 120P/50V_4

17 DRAM_RST_B R671 49.9/F_4 DRAM_B_RST
C969 120P/50V_4

Quanta Computer Inc.
PROJECT : AM9C

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	R16M-G1-50 - 2/5 (Memory)	A

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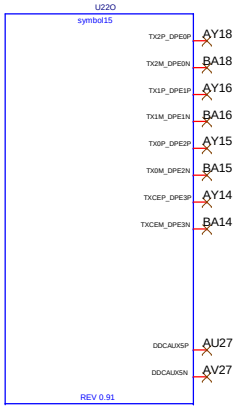
ASIC - TMDP (E)



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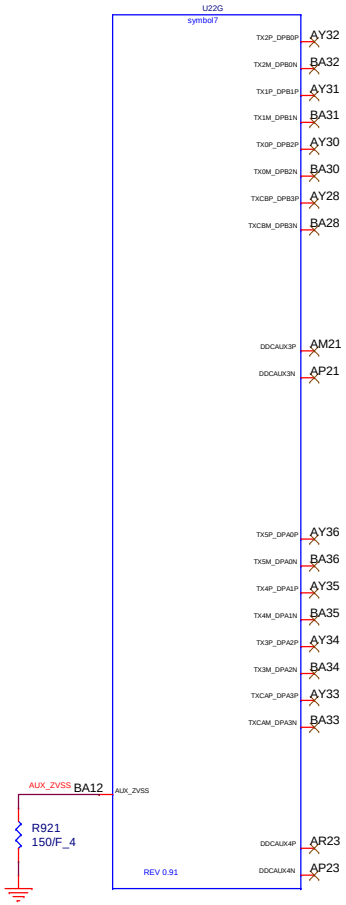
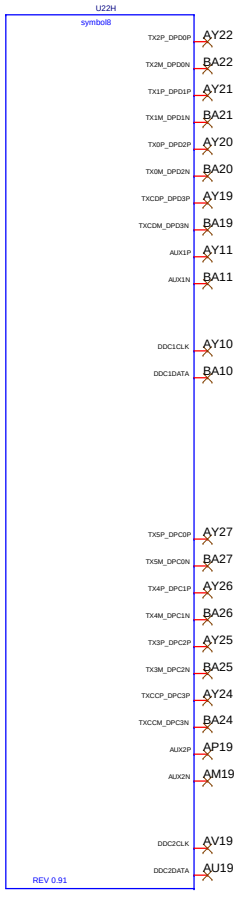


ASIC - TMDP (C/D)



Quanta Computer Inc.		
PROJECT : AM9C		
Size	Document Number: R16M-G1-5 - 3/5 (Display)	Rev: A
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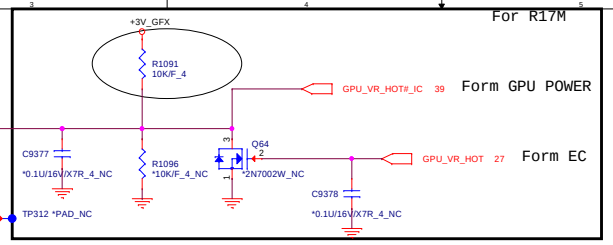
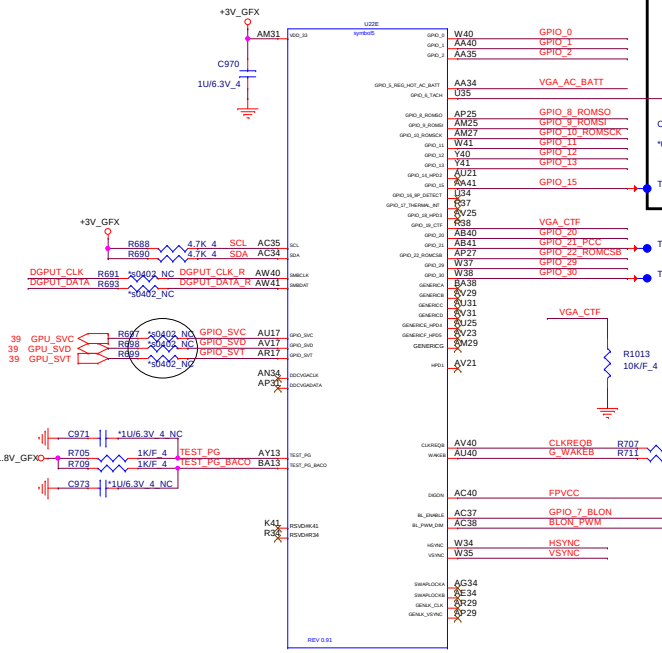
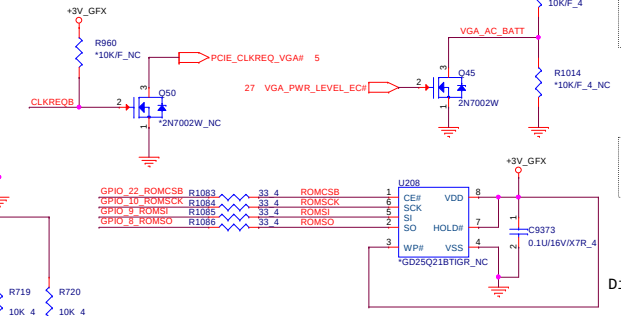
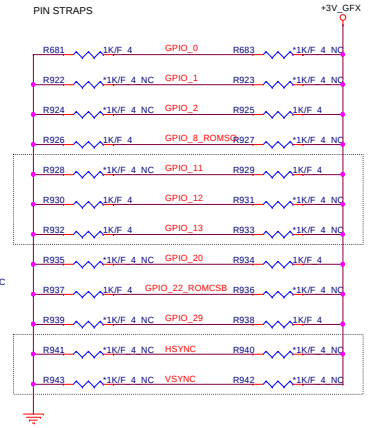
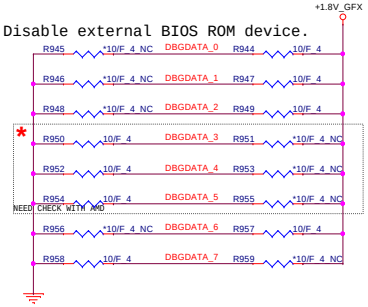


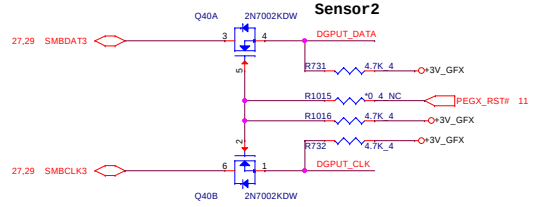


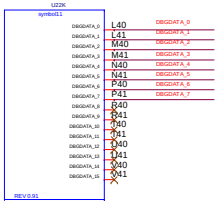




Disable external BIOS ROM device.





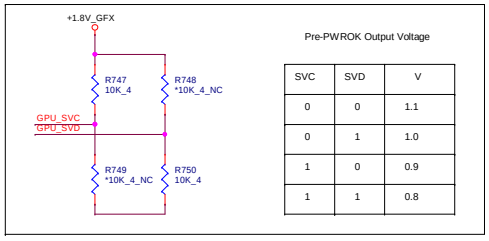


Strap Name	Pin Name	Description	GPU Default	Recommended Settings[1]
BIF_VGA_DIS	GPIO_29	Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).	0 (Internal pull-down)	Design dependent Provide a pull-up resistor option to VDD_33.
TX_DEEMPH_EN	GPIO_20	PCI Express transmitter de-emphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.	0 (Internal pull-down)	1 Through pull-up resistor to VDD_33.
TX_HALF_SWING	GPIO_0	Controls the transmitter full/half swing mode. 0: The transmitter full-swing is enabled. 1: The transmitter half-swing is enabled.	0 (Internal pull-down)	0 Provide a pull-up resistor option to VDD_33.

ROM_CONFIG[2:0]	GPIO_13 GPIO_12 GPIO_11	a) If BIOS_ROM_EN = 1, then ROM_CONFIG[2:0] defines the ROM type. See ROM Configurations (p. 42) for details. b) If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 42) for details.	101 (Internal pull-up/pull-down)	Design dependent. Provide a pull-down resistor option to GND on the PCB for GPIO_13. Provide a pull-up resistor option to VDD_33 on the PCB for GPIO_12. Provide a pull-down resistor option to GND on the PCB for GPIO_11.
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device. **Note:** When an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low).	1 (Internal pull-up)	Design dependent. Provide a pull-down resistor option to GND on the PCB.

Special Usage [1] Special Usage [0]	HSYNC VSYNC	Special usage	0 (Internal pull-down)	Design dependent. Refer to application note order #55739 on the special usage. Provide a pull-up resistor option to VDD_33 on the PCB for each pin.
AUD_PORT_CONN [2:0]	DBGDATA_2 DBGDATA_1 DBGDATA_0	Determine the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the GPU itself, the number and type of connectors on the board (DP/HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. 111: No usable endpoints 110: One usable endpoint 101: Two usable endpoints 100: Three usable endpoints 011: Four usable endpoints 010: Five usable endpoints 001: Six usable endpoints 000: All endpoints are usable	0 (Internal pull-down)	Design dependent, see description. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin.

BOARD_CONFIG [2:0]	DBGDATA_5 DBGDATA_4 DBGDATA_3	Provides an option to specify certain board-level specifics to the VBIOS or driver.	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin.
SMBUS_ADDR [1:0]	DBGDATA_7 DBGDATA_6	Provide a strap option to change the SMBUS slave address of the GPU. 00: 0×40 01: 0×41 10: 0×42 11: 0×43	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin. Strap on the PCB the address **to 0×41** if it does not cause address conflict on the platform.
BIF_GEN3_EN_A	GPIO_2	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.	1 (Internal pull-up)	Design dependent. Provide a pull-down resistor option to GND on the PCB.
BIF_CLK_PN_EN	GPIO_8_ROMSO	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.	0 (Internal pull-down)	1 Provide a pull-up resistor option to VDD_33 on the PCB.
Reserved	GPIO_15	Reserved	0 (Internal pull-down)	Must default to 0 for production. Provide a pull-up resistor option to VDD_33 on the PCB.
Reserved	GPIO_9_ROMSI	Reserved	0 (Internal pull-down)	Must default to 0 for production. Provide a pull-up resistor option to VDD_33 on the PCB.



Pre-PWROK Output Voltage

SVC	SVD	V
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VRAM Table of AMD R16M

VRAM DBGDATA (5~3)	DESCRIPTION	Vendor	DELL P/N	QCI P/N
010	H5GC8H24MJR-R0C (029XX)	Hynix	N/A	AKG5QGUTW02
001	K4G80325FB-HC28 (N1MMH)	Samsung	N/A	AKG5QGDT506
* 000	MT51J256M32HF-70:A (V15MH)	Micron	N/A	AKG5QGUTL08

Quanta Computer Inc.
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	R16M-G1-50 - 4/5 (MISC)	A

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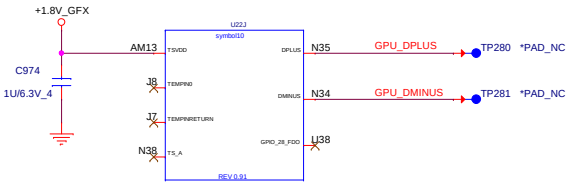
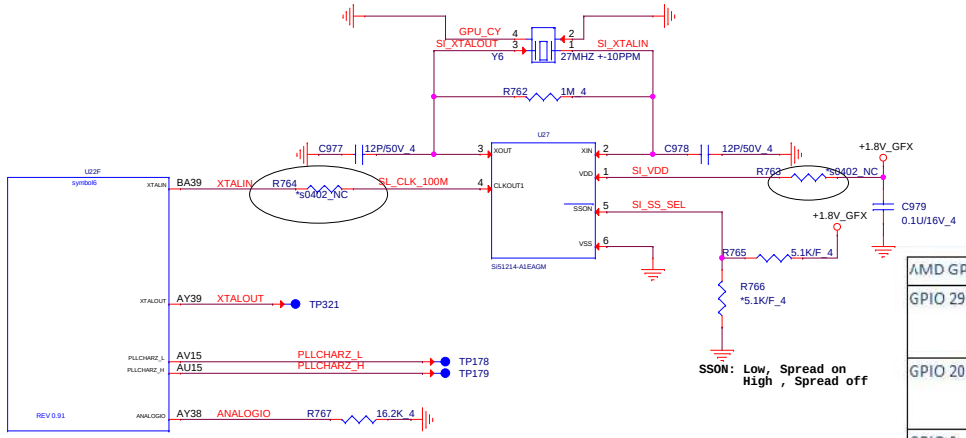
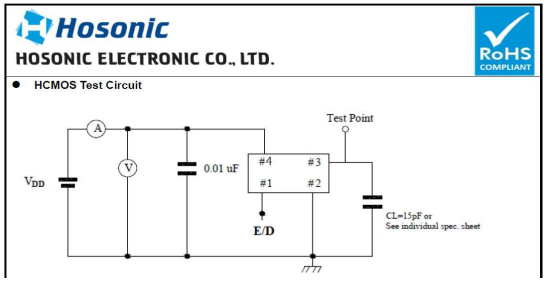


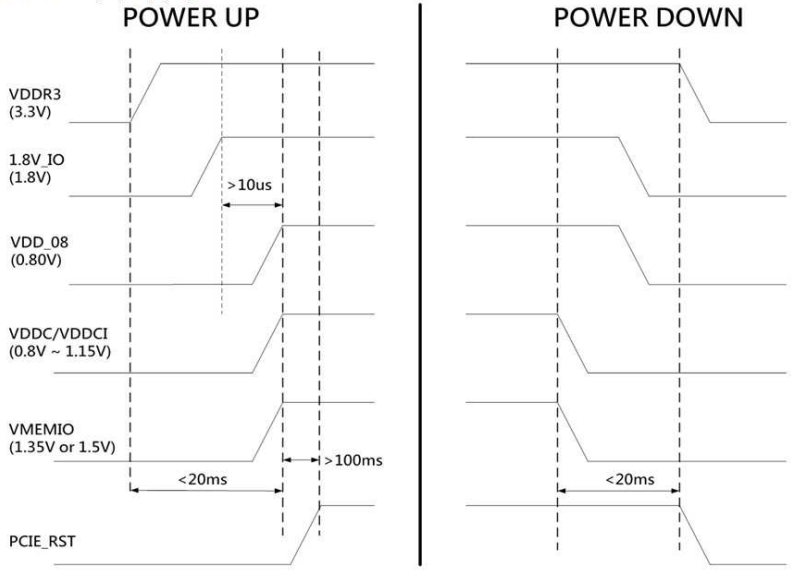


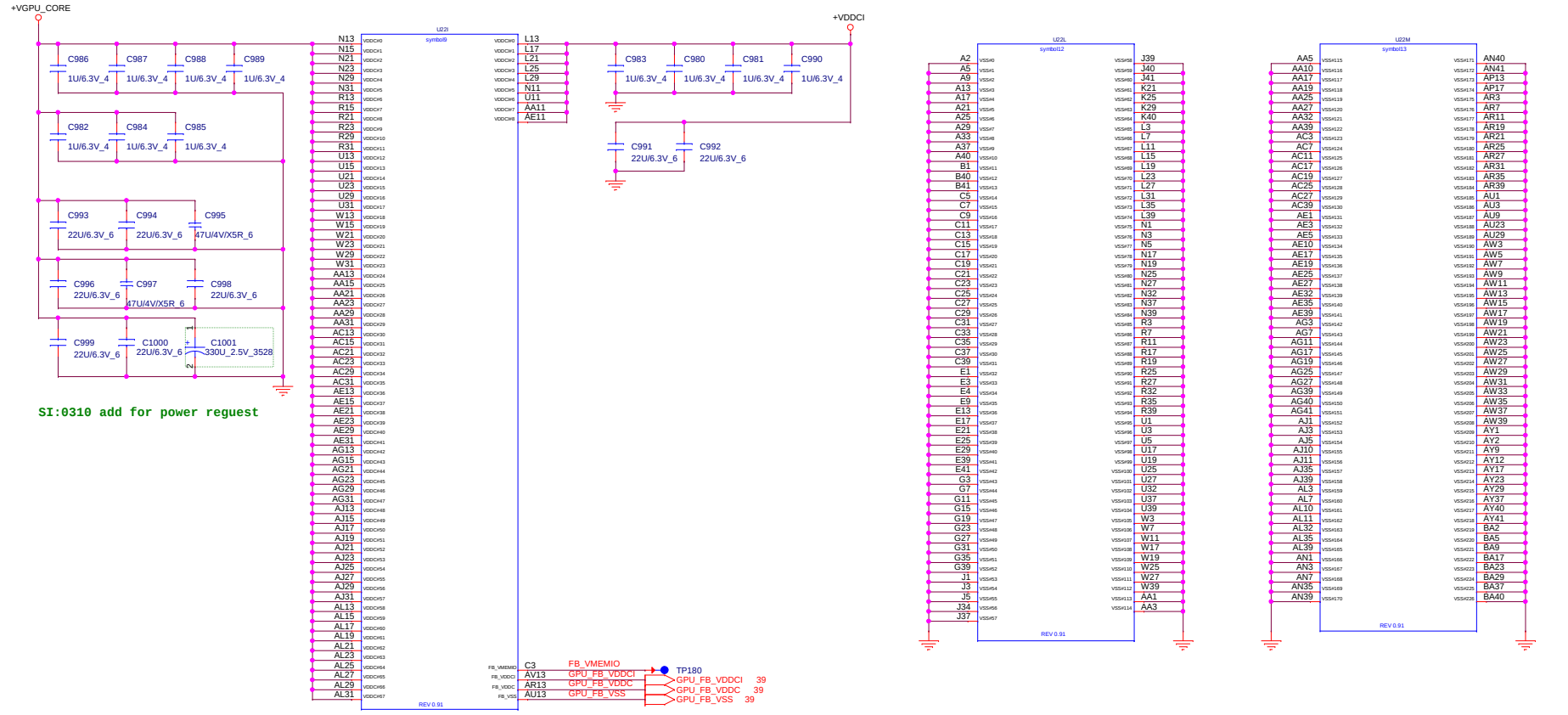


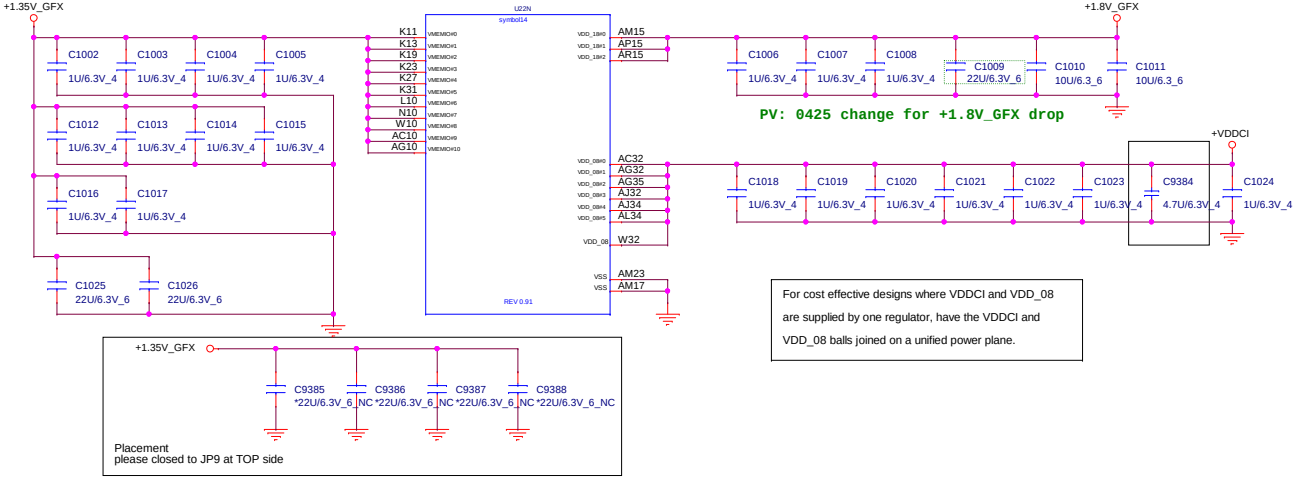
AMD GPIO Straping	Setting	Name	Description
GPIO 29	Pull low 10K ohm	BIF_VGA_DIS	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).
GPIO 20	Pull up 10K ohm	TX_DEEMPH_EN	PCI Express transmitter deemphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.
GPIO 0	Pull up 10K ohm	TX_HALF_SWING	Controls the transmitter full/half swing mode. 0: The transmitter full swing is enabled. 1: The transmitter half swing is enabled.
GPIO 22	Pull low 10K ohm	BIOS_ROM_EN	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.
GPIO 11	Pull up 10K ohm	ROM_CONFIG[2:0]	b) If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. GPIO_[13:12:11]=001=256MB
GPIO 12	Pull low 10K ohm		
GPIO 13	Pull low 10K ohm		
Hysnc	NC	Reserve	Reserve
Vsync	NC		

DBGDATA2	Pull up 10K ohm	AUD_PORT_CONN [2:0]	Determine the maximum number of digital display audio endpoints 101: Two usable endpoints
DBGDATA1	Pull low 10K ohm		
DBGDATA0	Pull up 10K ohm		
GPIO 1	Pull up 10K ohm	SMBUS_ADDR	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0x40 1: 0x41
GPIO 2	Pull up 10K ohm	BIF_GEN3_EN_A	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.
GPIO 8	connect CLKREQ#_GPU and add pull up / down resistor	BIF_CLK_PM_EN (Reserve)	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.
WAKEB	Pull low 10K ohm	OBFF	0: Disable
SVI2_SVC	Pull up 1Kohm	Boot up voltage	SVC:SVD=[1:0]=0.90V
SVI2_SVD	Pull low 1K ohm		

R16M-G1-70 Power up sequence for you refer.







Quanta Computer Inc.

PROJECT : AM9C

Size	Document Number	Rev
	R16M-G1-50 - 5/5 (Power)	A

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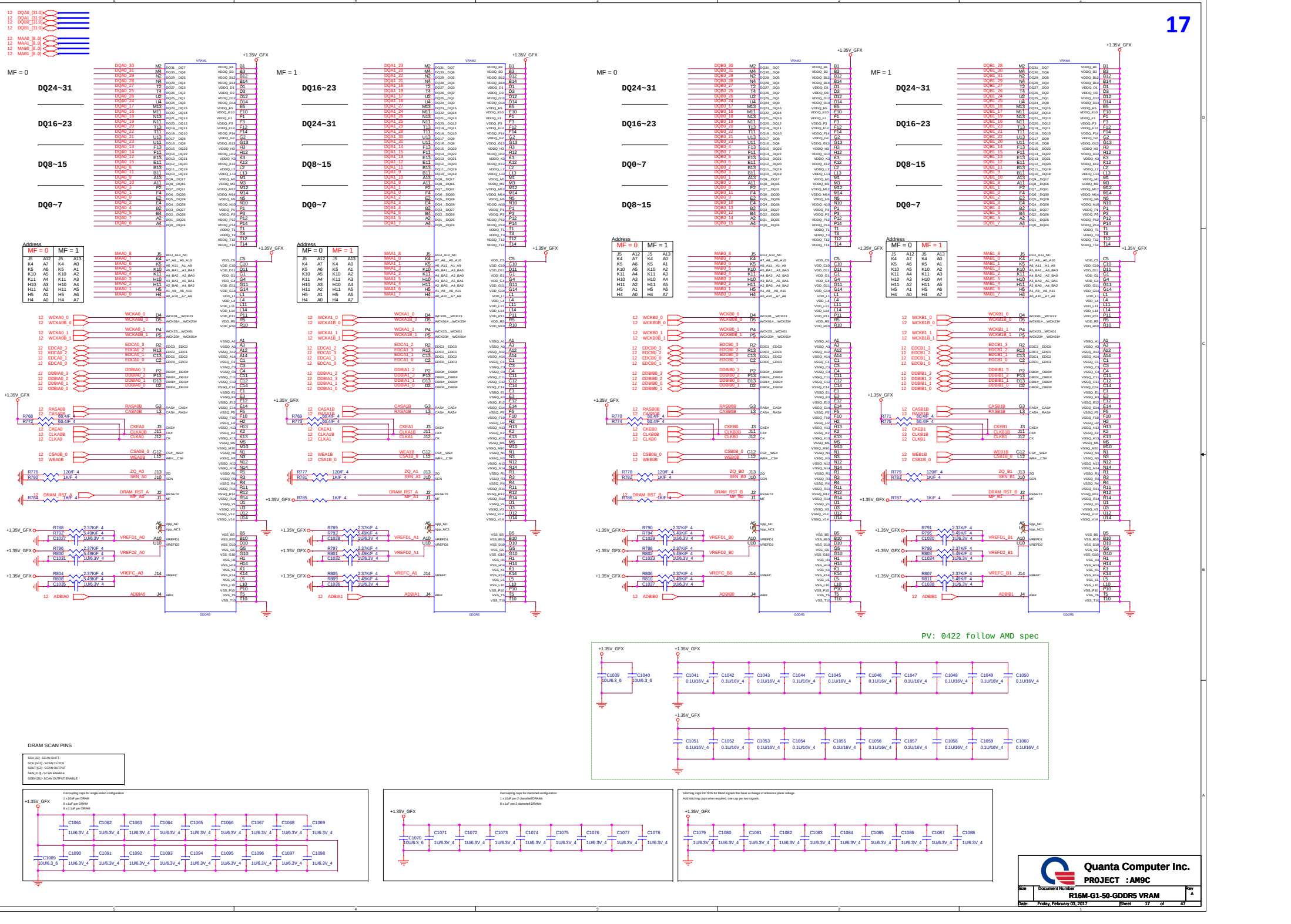

Quanta Computer Inc.

PROJECT : AM9C

Size	Document Number	Rev
	R16M-G1-50-GDDR5 VRAM	A

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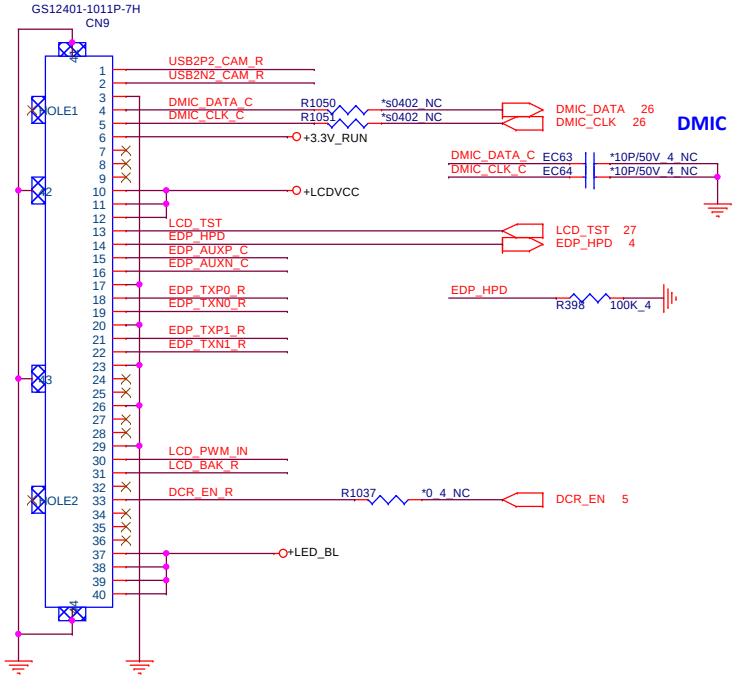
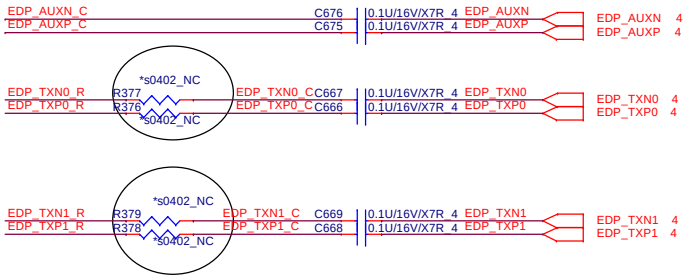
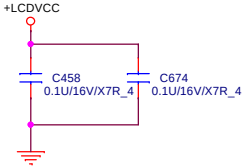
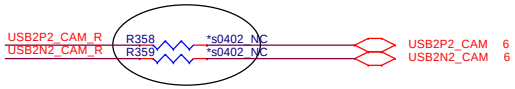
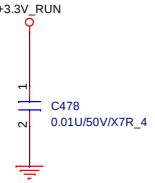


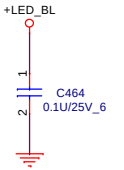




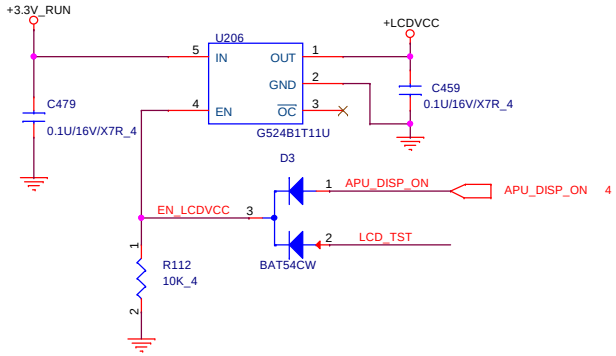


CAMERA

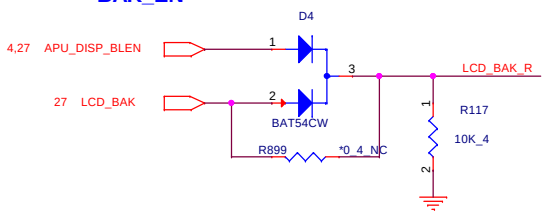




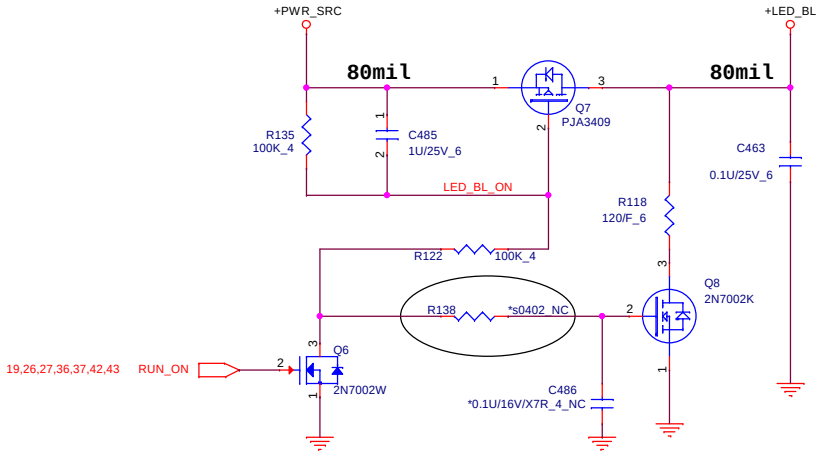
LCD_VCC



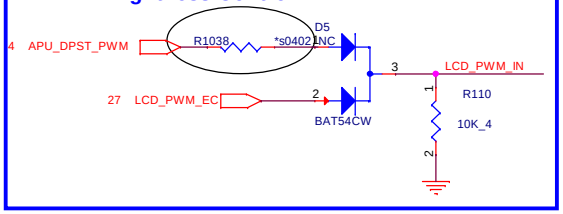
BAK_EN



Brightness Power



Brightness Control



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PROJECT : AM9C

Size	Document Number	Rev
	eDP/ Camera Conn	A

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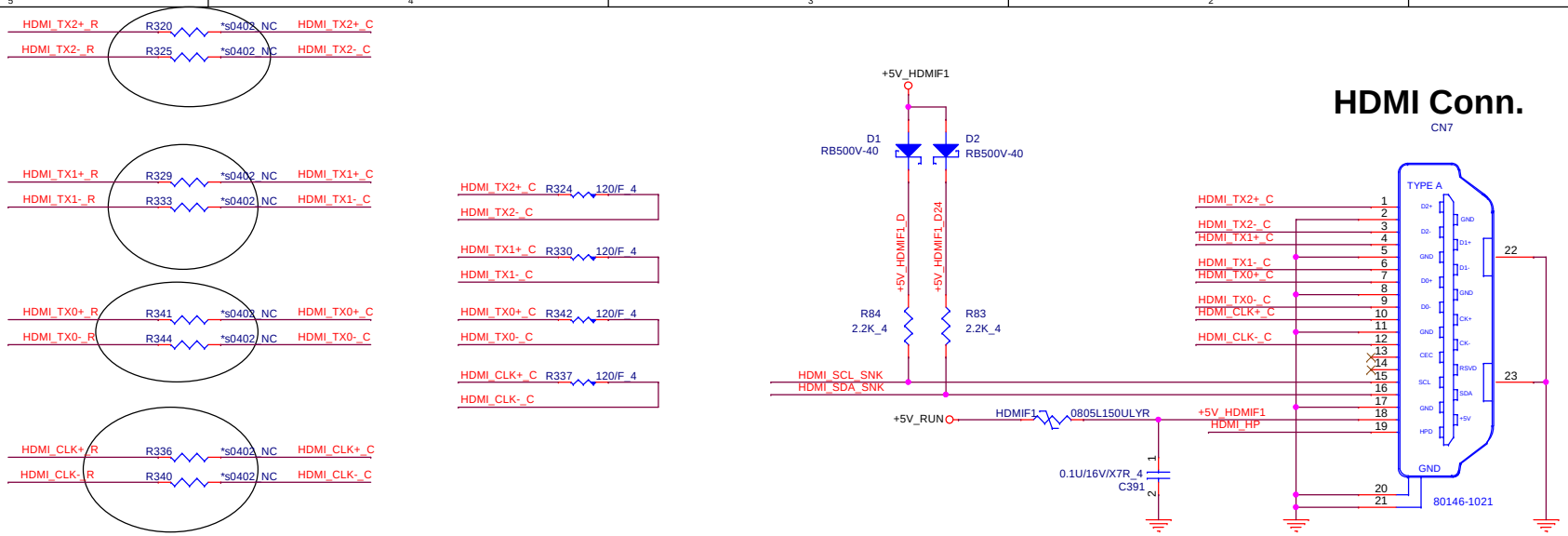
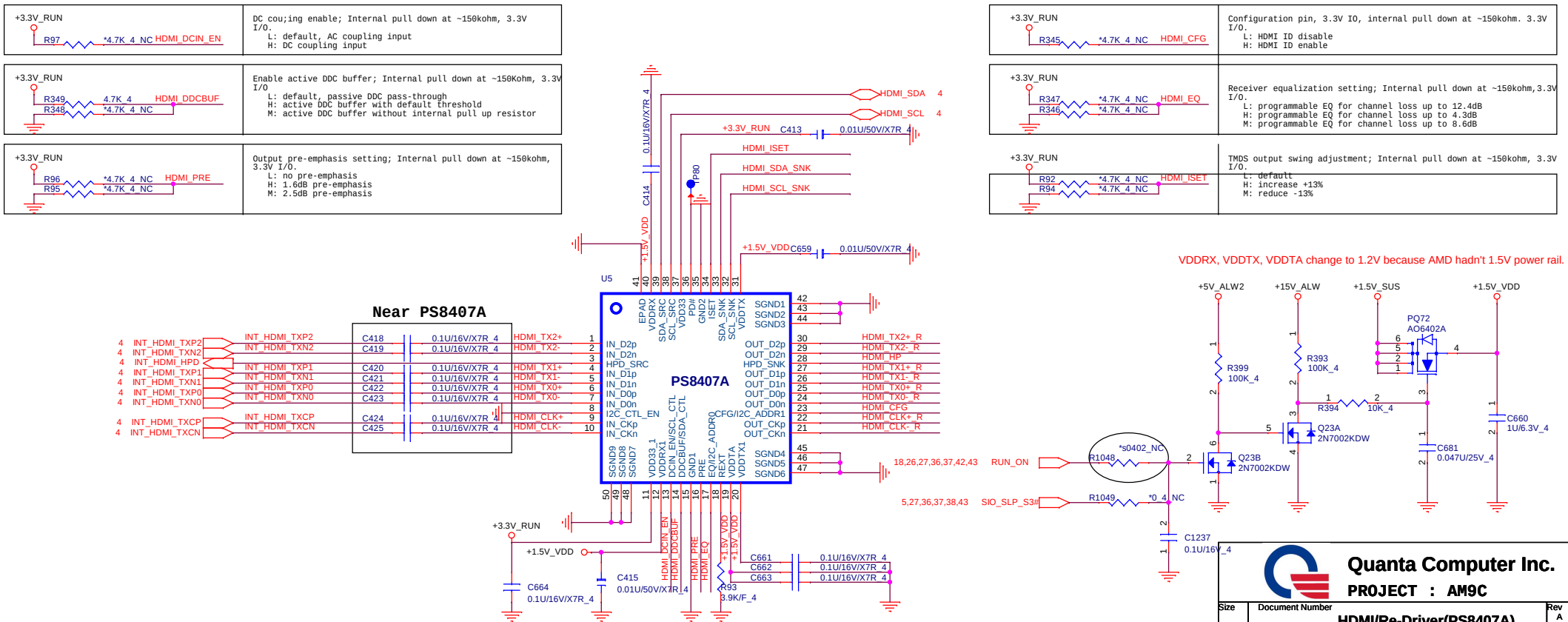
HDMI Conn.

CN7



HDMI HPD :
1. PS8407A internal PD 150kohm
2. PS8407A has implement level shifter



Quanta Computer Inc.			
PROJECT : AM9C			
Size	Document Number		Rev
	HDMI/Re-Driver(PS8407A)		A
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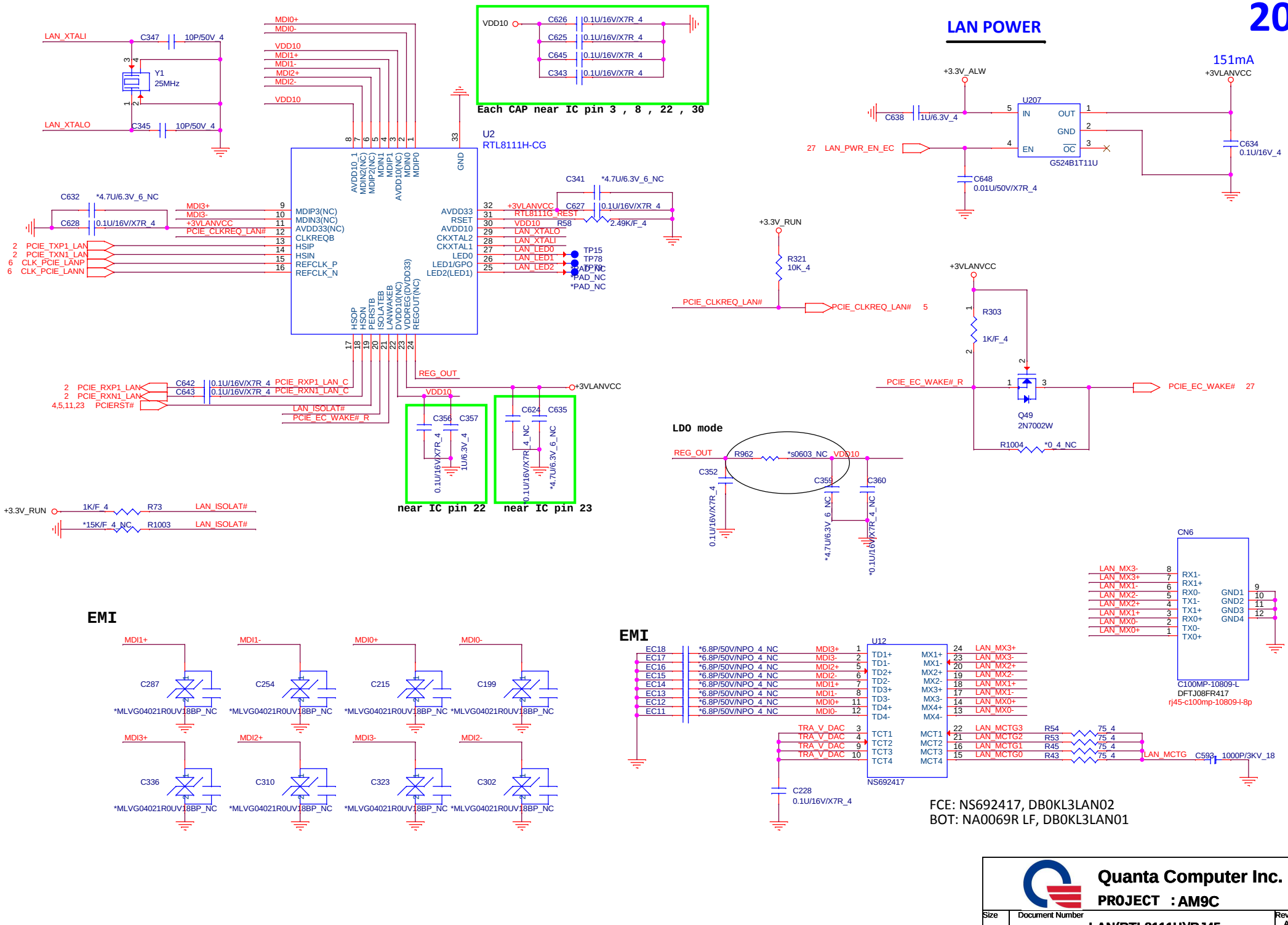
LAN POWER

151mA



FCE: NS692417, DB0KL3LAN02
BOT: NA0069R LF, DB0KL3LAN01

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PROJECT : AM9C

Size	Document Number	Rev
	LAN(RTL8111H)/RJ45	A
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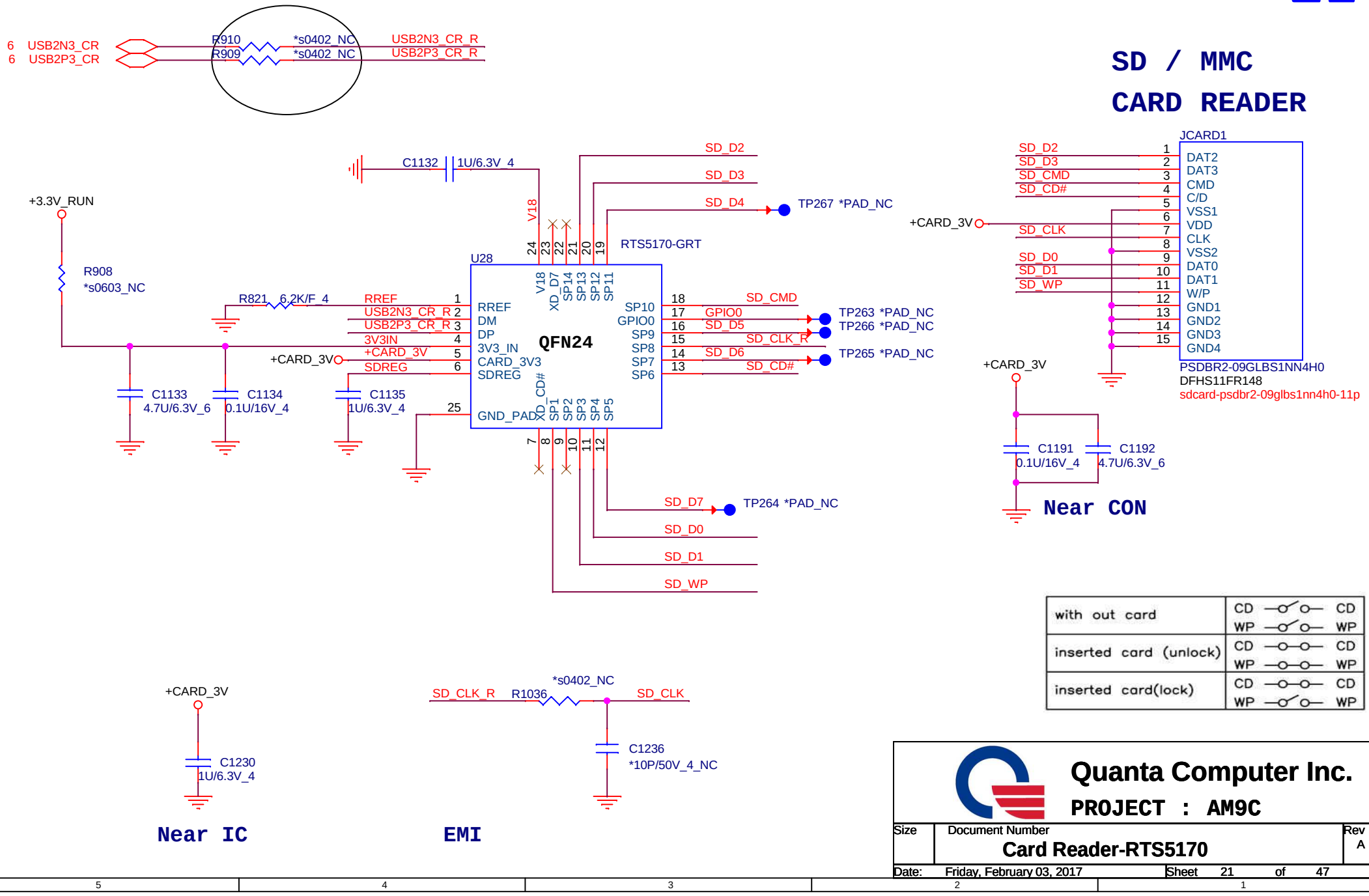
SD / MMC CARD READER



with out card	CD — CD, WP — WP
inserted card (unlock)	CD — CD, WP — WP
inserted card(lock)	CD — CD, WP — WP

Quanta Computer Inc.

PROJECT : AM9C

Size	Document Number	Rev
	Card Reader-RTS5170	A
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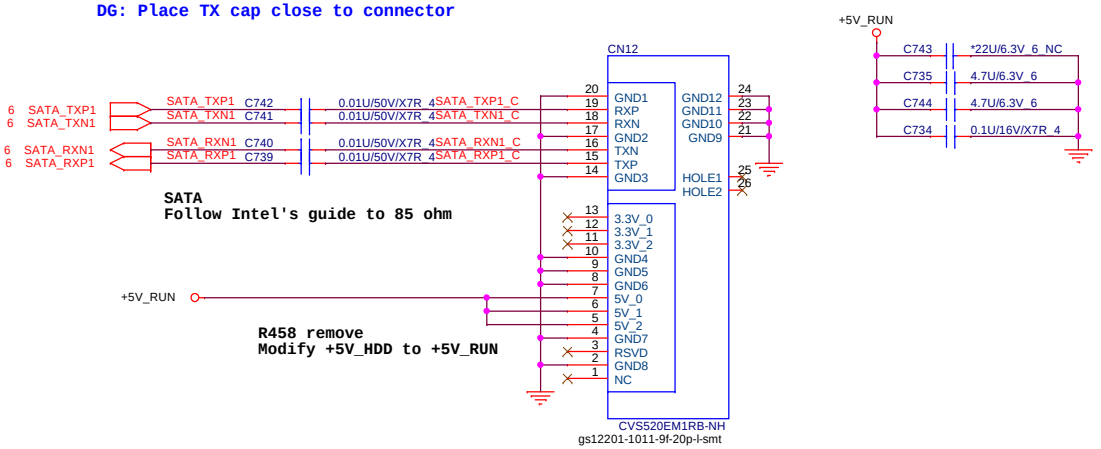
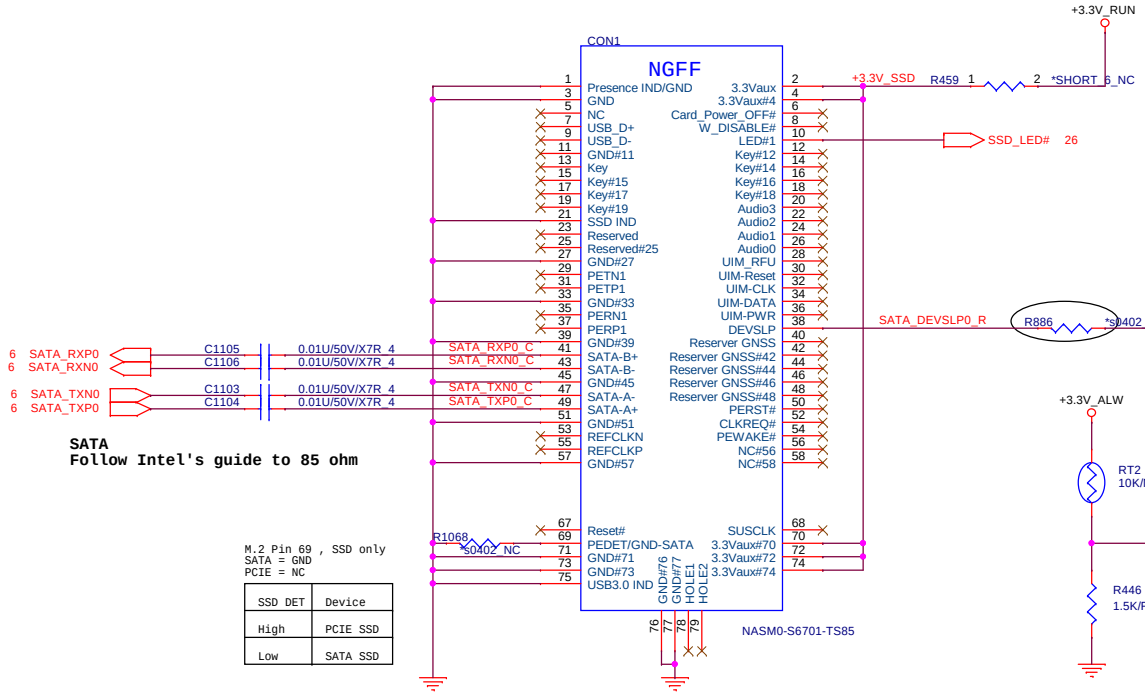
SATA HDD Connector

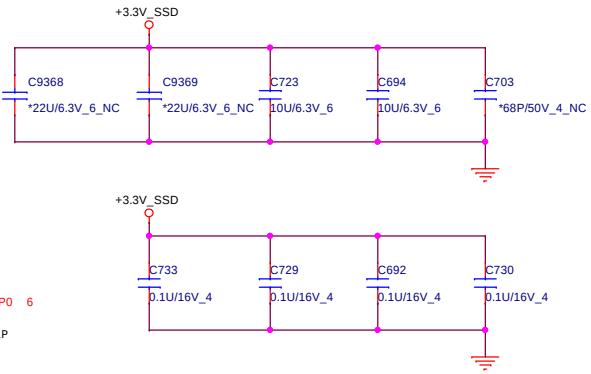
DG: Place TX cap close to connector



NGFF M.2 SATA SSD

Place caps close to connector.





Quanta Computer Inc.			
PROJECT : AM9C			
Size	Document Number		Rev
	HDD/M.2(NGFF)		A
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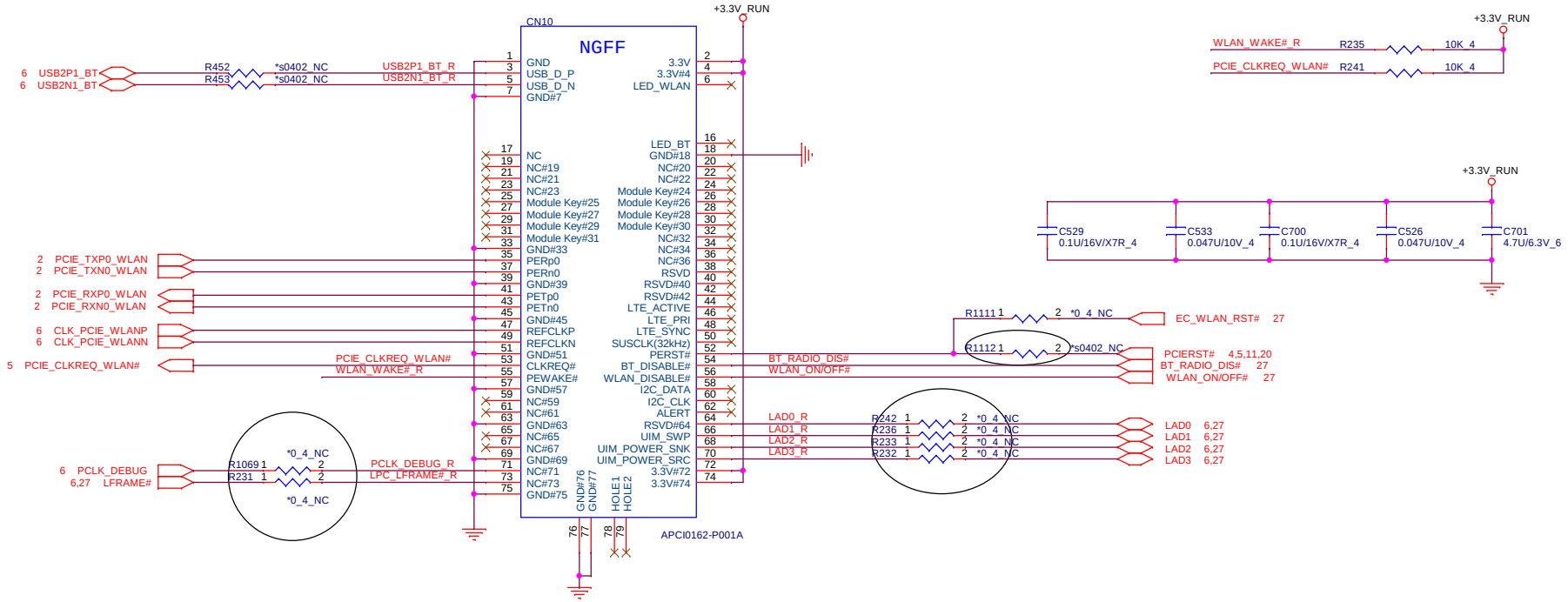
M.2 (NGFF) A-KEY
WLAN/BT(Option)



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PROJECT : AM9C		
Size	Document Number: WLAN/BT	Rev: A
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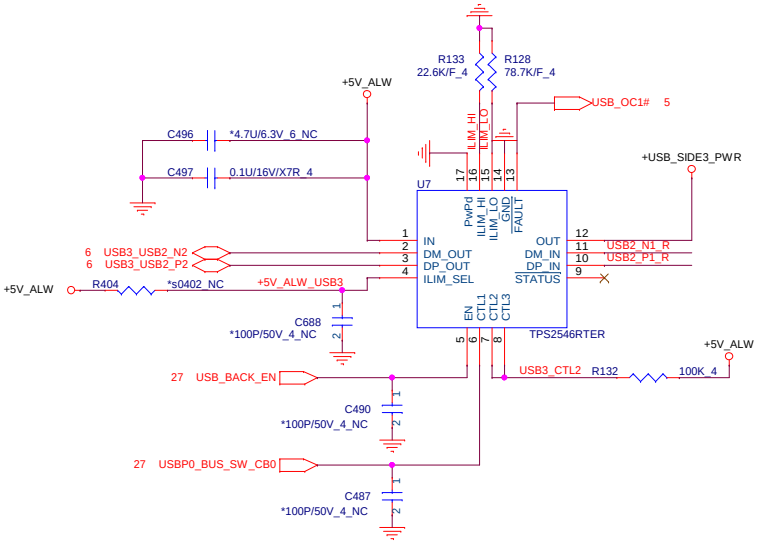
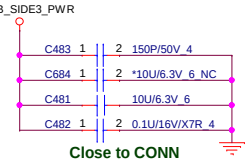
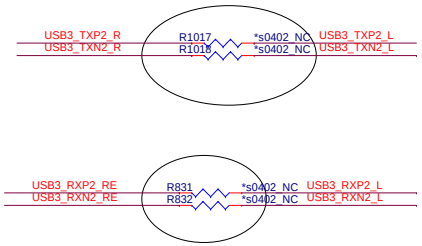
USB Power share

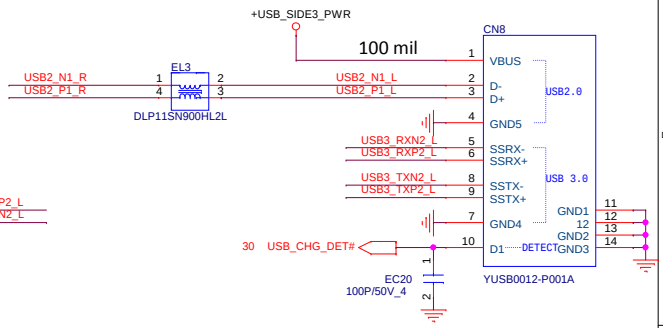
USB3.0/2.0 COMBO X 1

USBP0_BUS_SW_CB0	Mode	Operating at
High	CDP	S0, 1.5 A
Low	DCP, Auto-detect	S3/S4/S5, 2.1/1.5 A



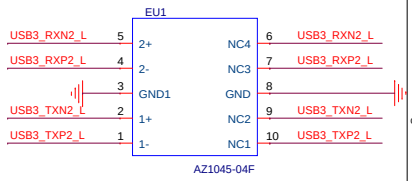


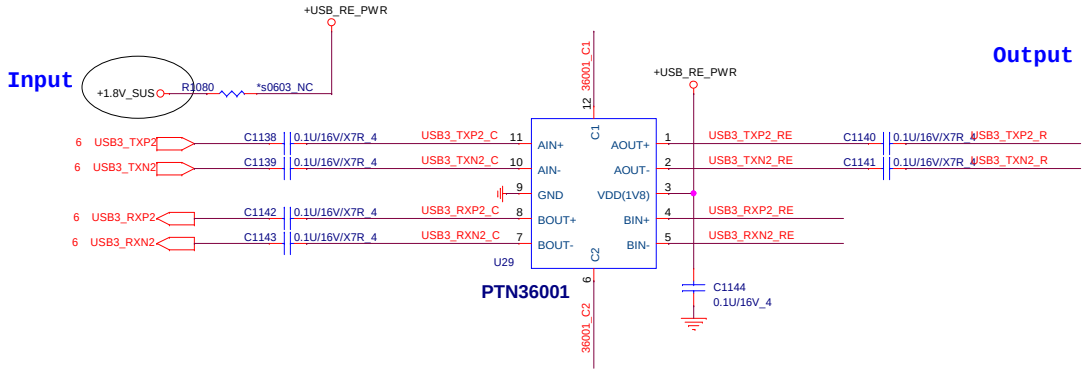




	R89	mA
OC limitation	22.6k ohm	2224
	23.2k ohm	2167

Need closed to CN9





Output

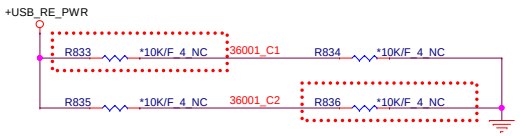


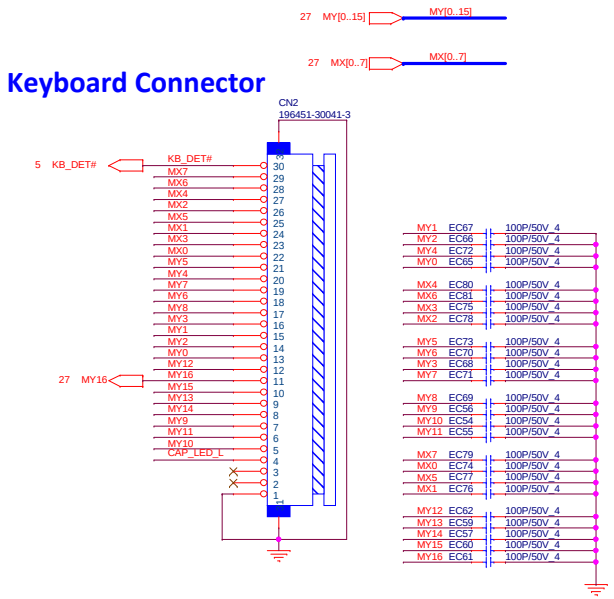
Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

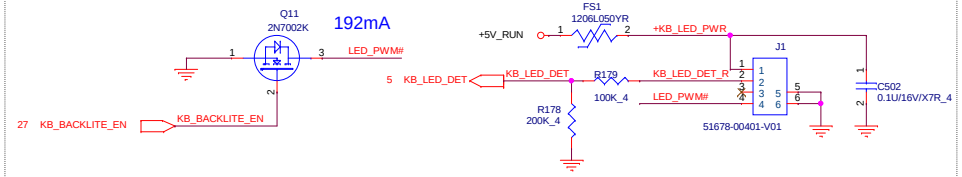
State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

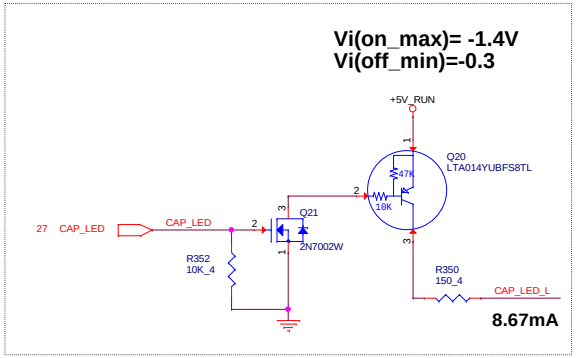
Keyboard Connector



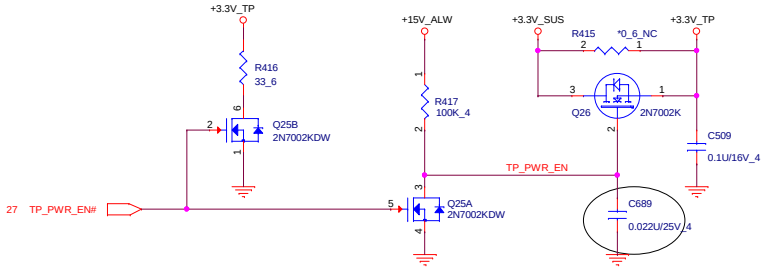
Key board illumination

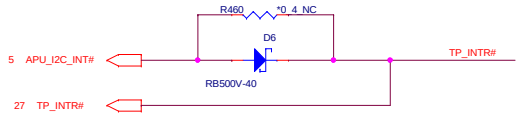
+KB_LED power trace width >10 mil

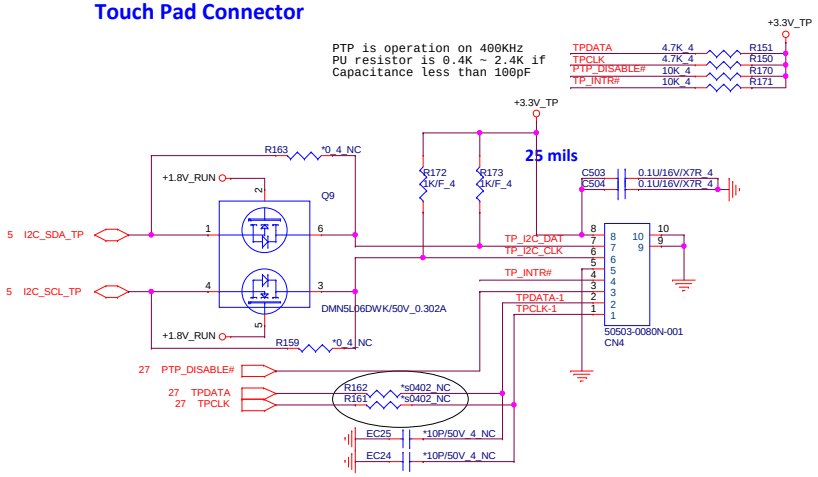




Touch Pad Connector







Quanta Computer Inc.		
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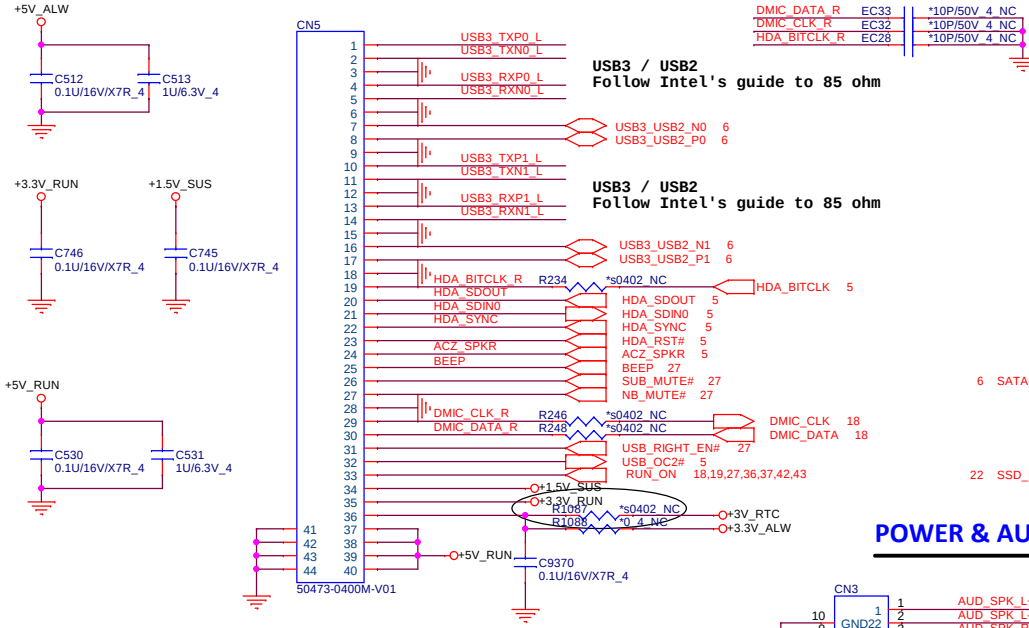
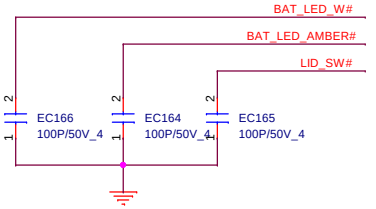
MB to IO Connector

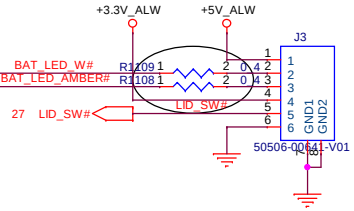


USB3 / USB2
Follow Intel's guide to 85 ohm

USB3 / USB2
Follow Intel's guide to 85 ohm

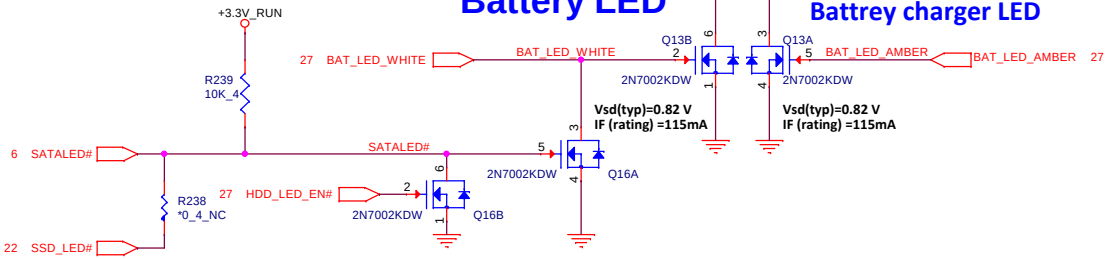


LED Board CONN

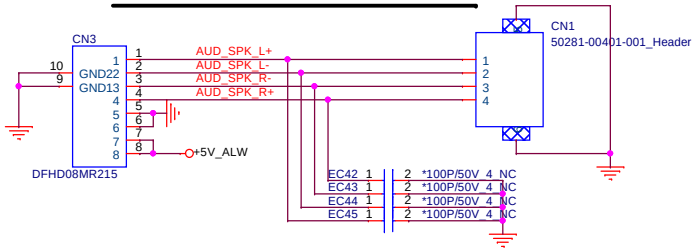


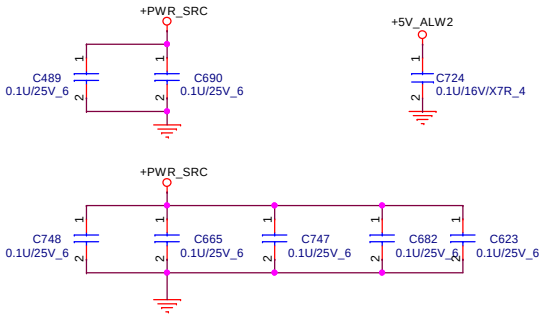
Battery LED

Battrey charger LED



POWER & AUDIO SPEAKER CON





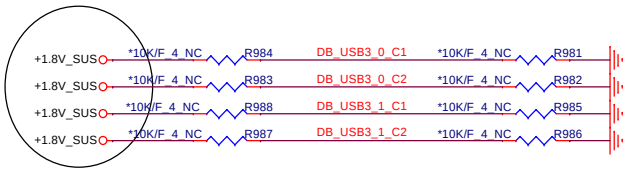
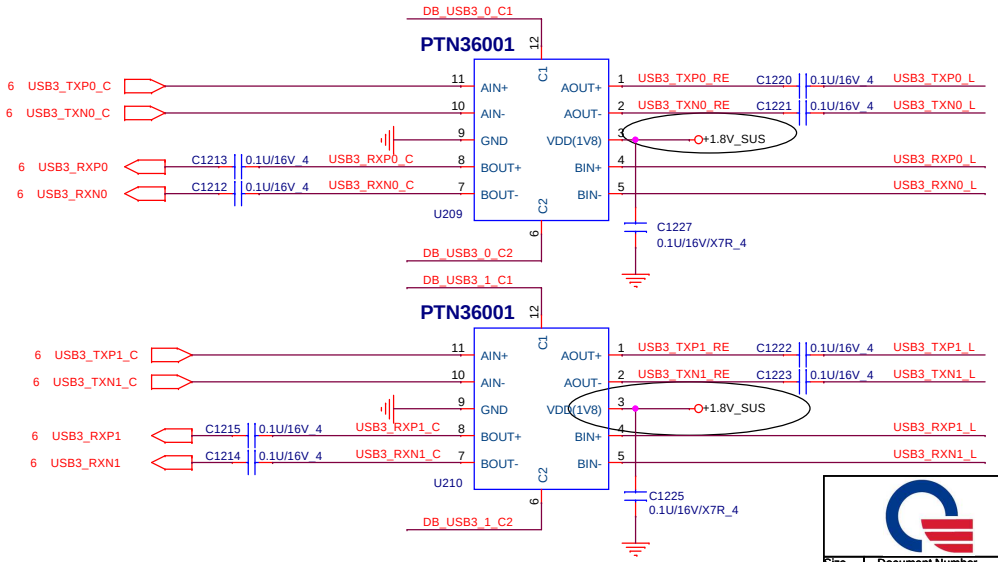


Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V



Quanta Computer Inc.
PROJECT : AM9C

Size	Document Number	Rev
	IO BD CONN/LED	A

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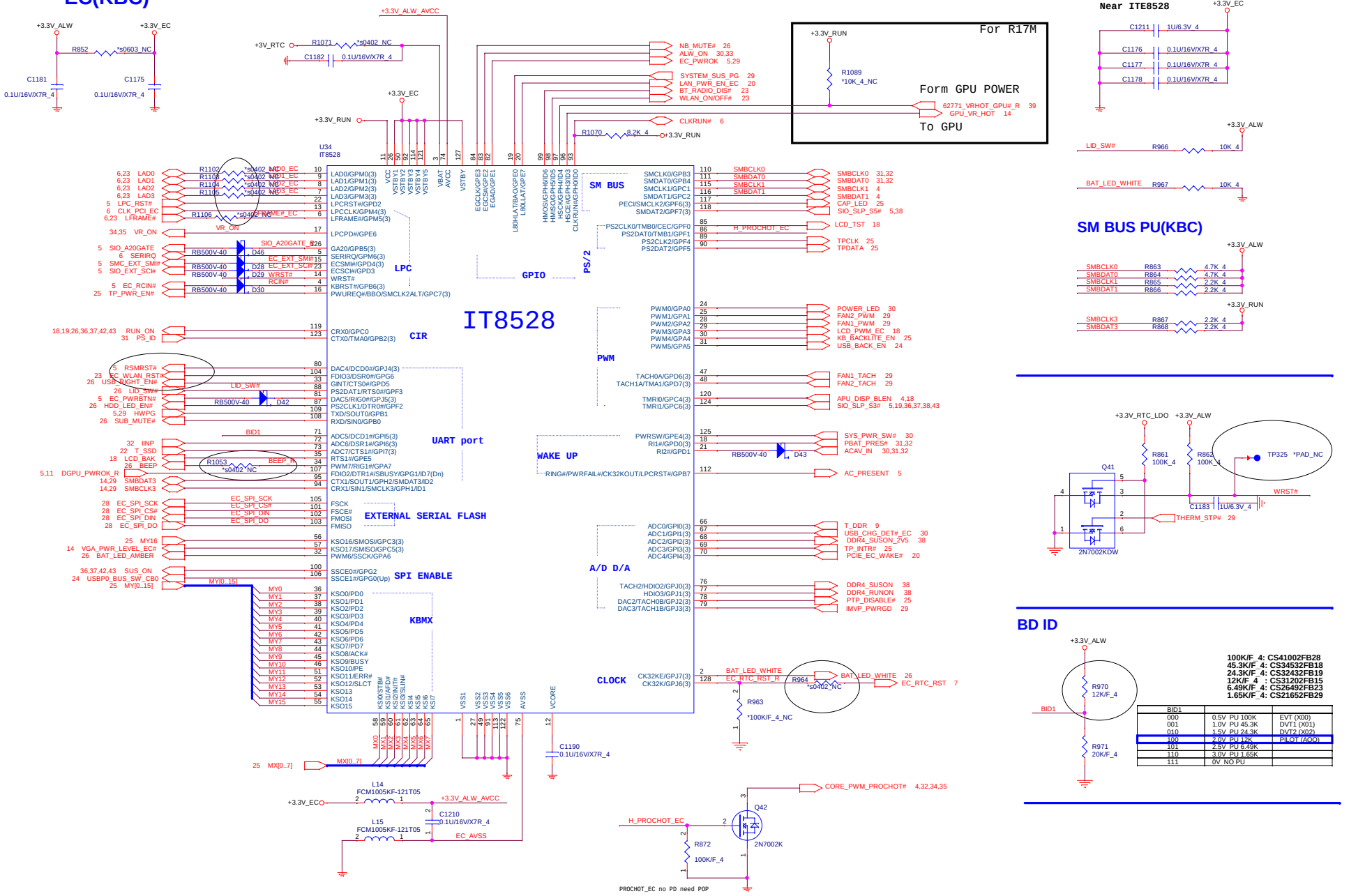
EC(KBC)



BID1		
000	0.5V PU 100K	EVT (X00)
001	1.0V PU 45.3K	DVT1 (X01)
010	1.5V PU 24.3K	DVT2 (X02)
100	2.0V PU 12K	PILOT (AG0)
101	2.5V PU 6.49K	
110	3.0V PU 1.65K	
111	0V NO PU	

Quanta Computer Inc.

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Size	Document Number	Rev
	KBC IT8528	A

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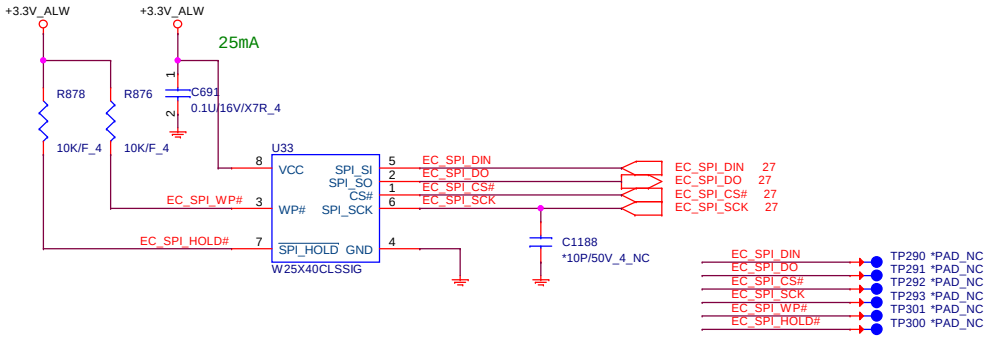
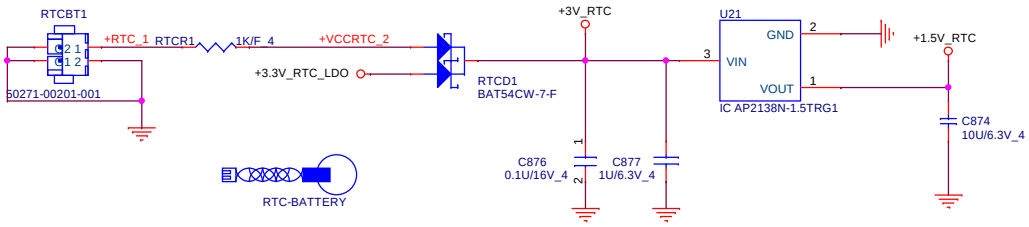
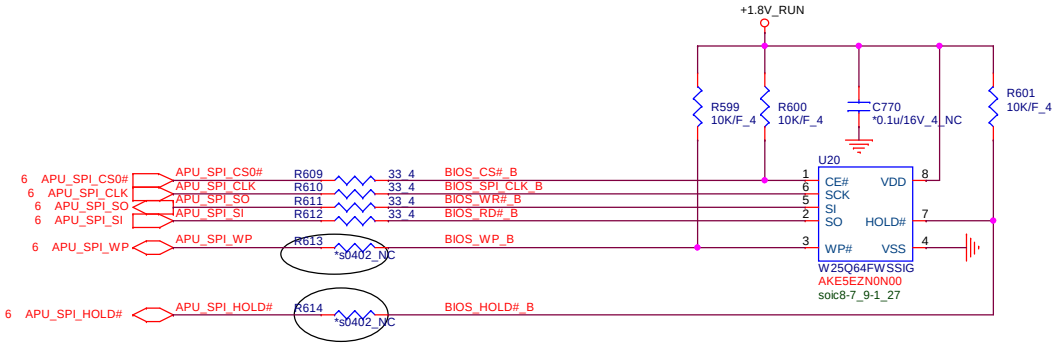
For EC (512K Byte)



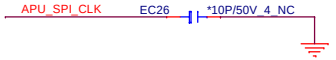
20MIL



For PCH ME 64Mbit (8M Byte)



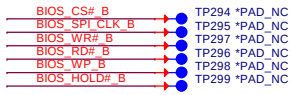
EMI



APU SPI ROM

Vender	Size	P/N (1.8V)
WND	8M	AKE5EZN0N00
EON	8M	AKE5EFN0Q00
Socket	DG008000002	

TPs need place to all TOP or all BOT



Quanta Computer Inc.
PROJECT : AM9C

Size	Document Number	Rev
	FLASH / RTC	A

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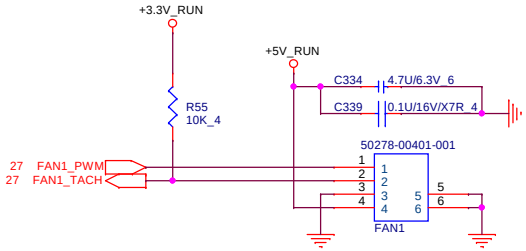
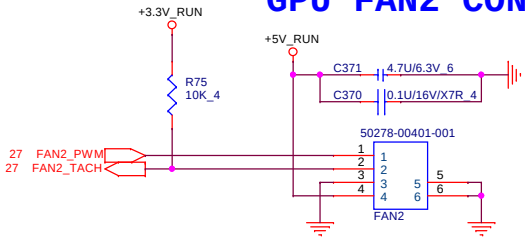
CPU FAN1 CONN

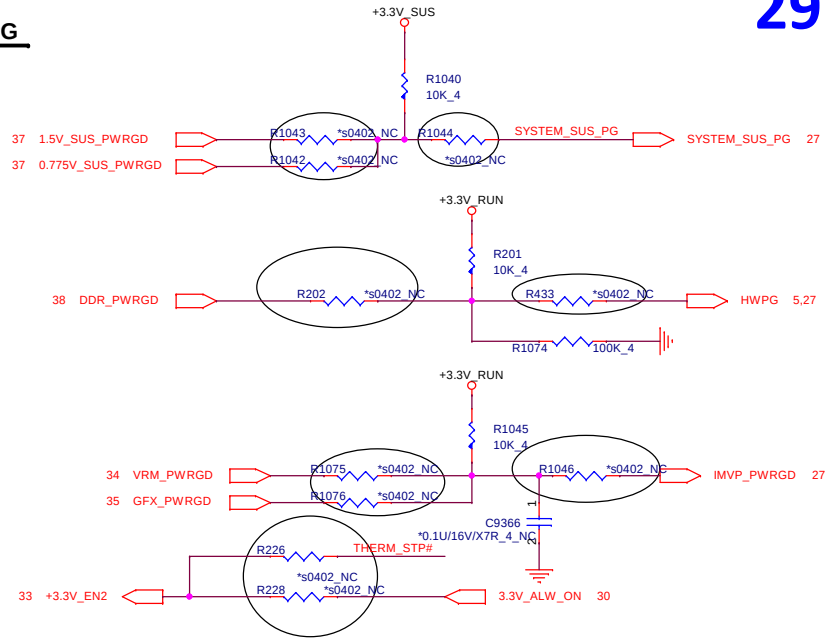
+5V_FAN
Max Current : 400 mA



GPU FAN2 CONN



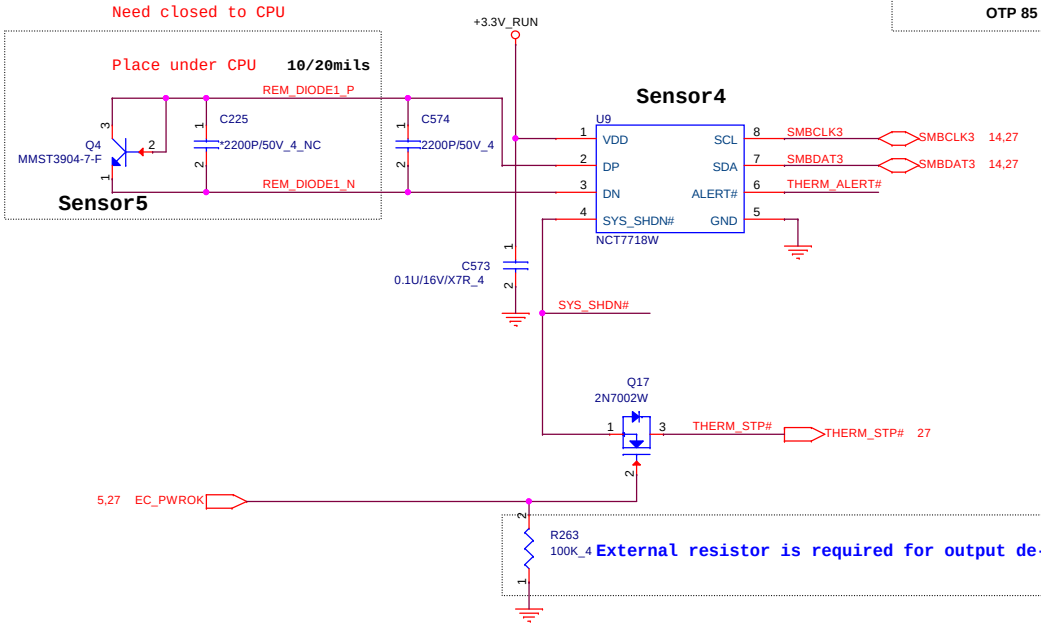
HWPG



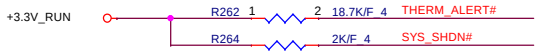
THERMAL IC

Need closed to CPU

Place under CPU **10/20mils**



OTP 85 degree C



OTP 85 degree : R526= 18.7K, R527= 2K

SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

Quanta Computer Inc.
PROJECT : AM9C

Size	Document Number	Rev
	Thermal FAN/HWPG	A

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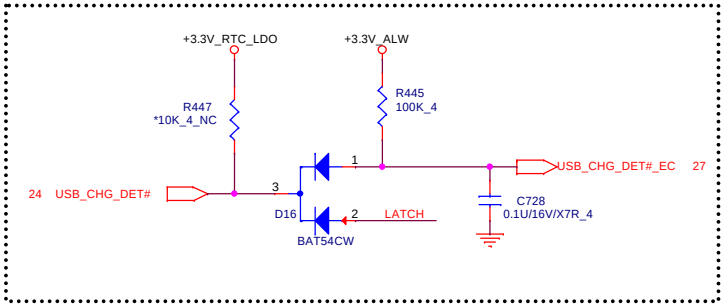
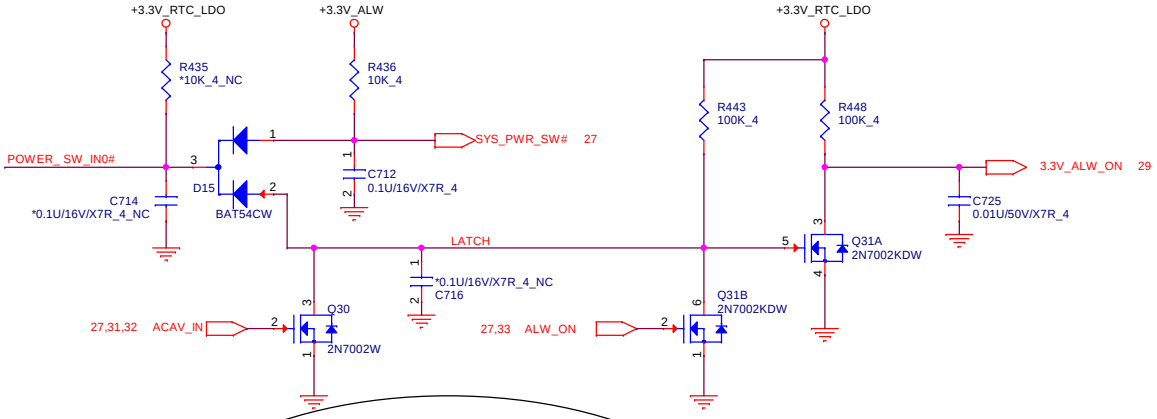
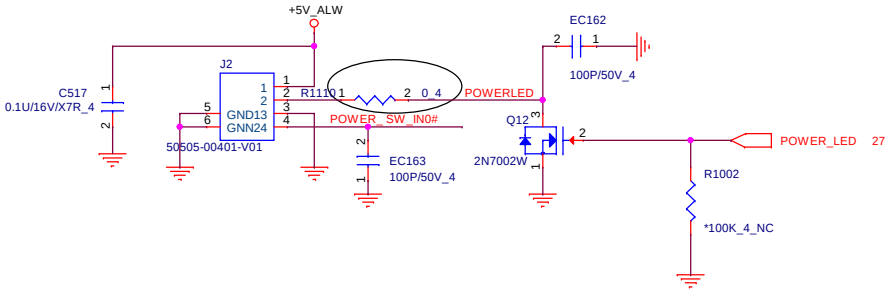
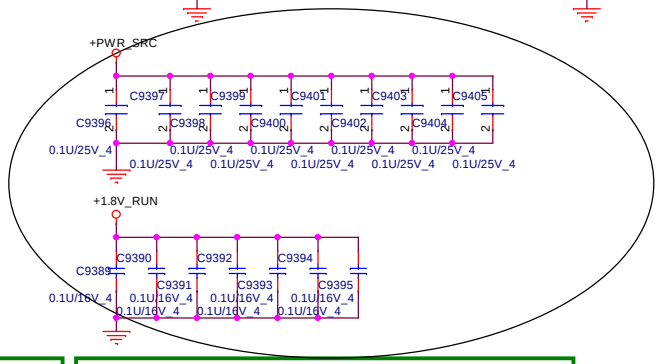
3VALW_ON POWER LOGIC

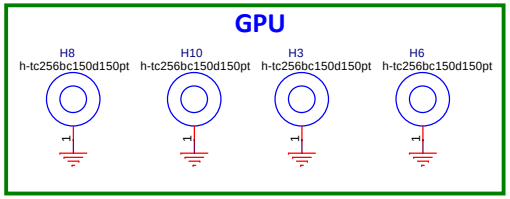


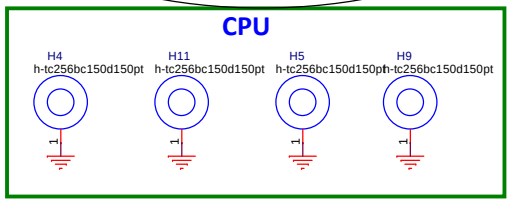


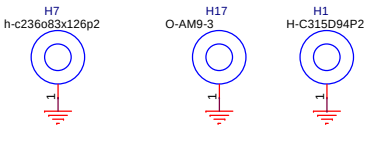
POWER BOARD CONN

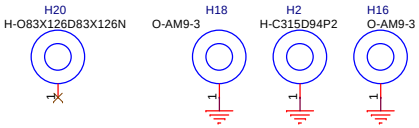


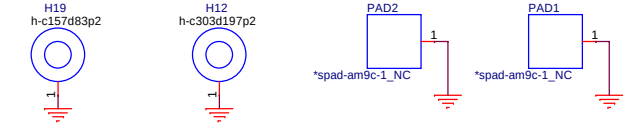










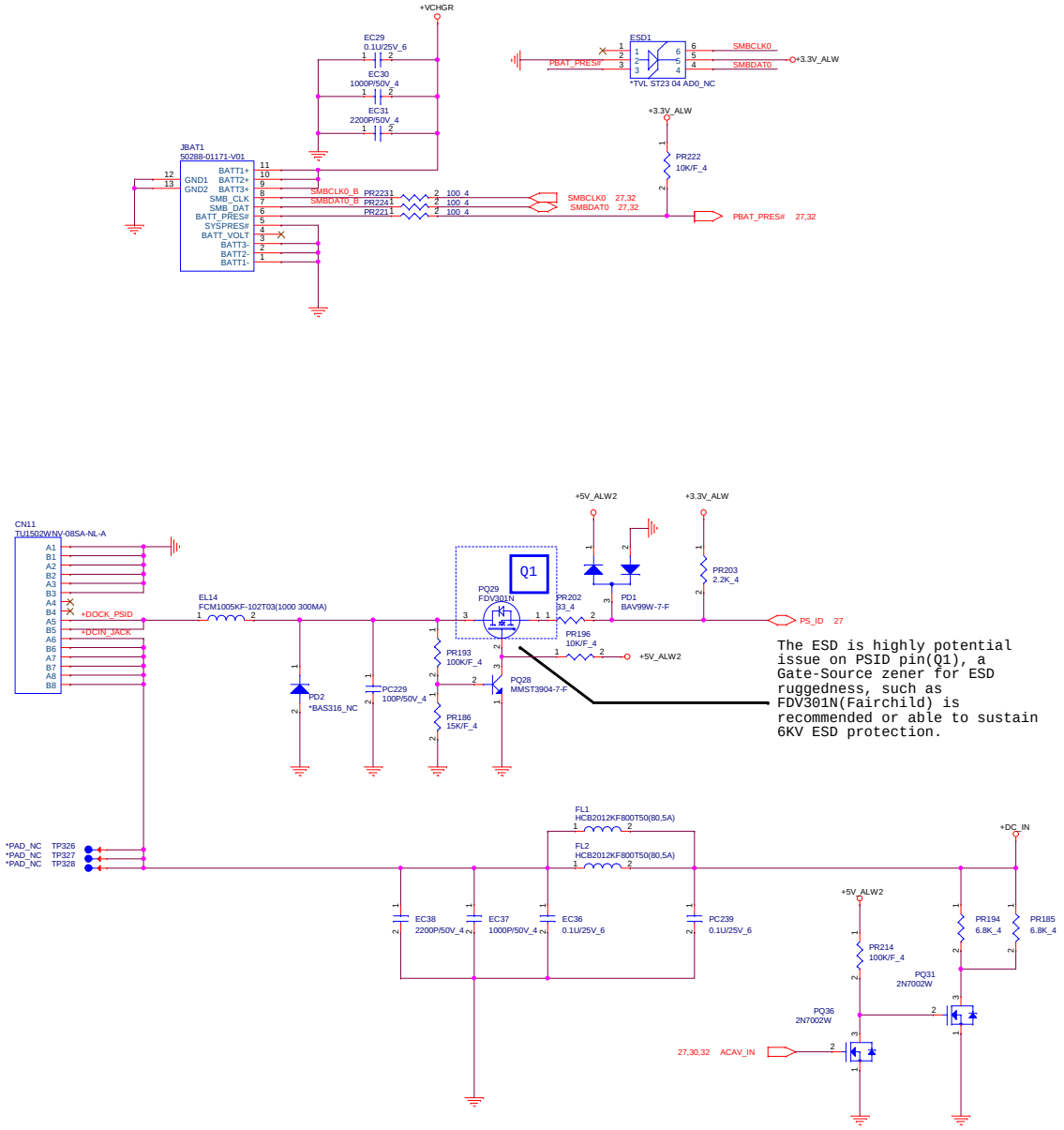


Quanta Computer Inc.

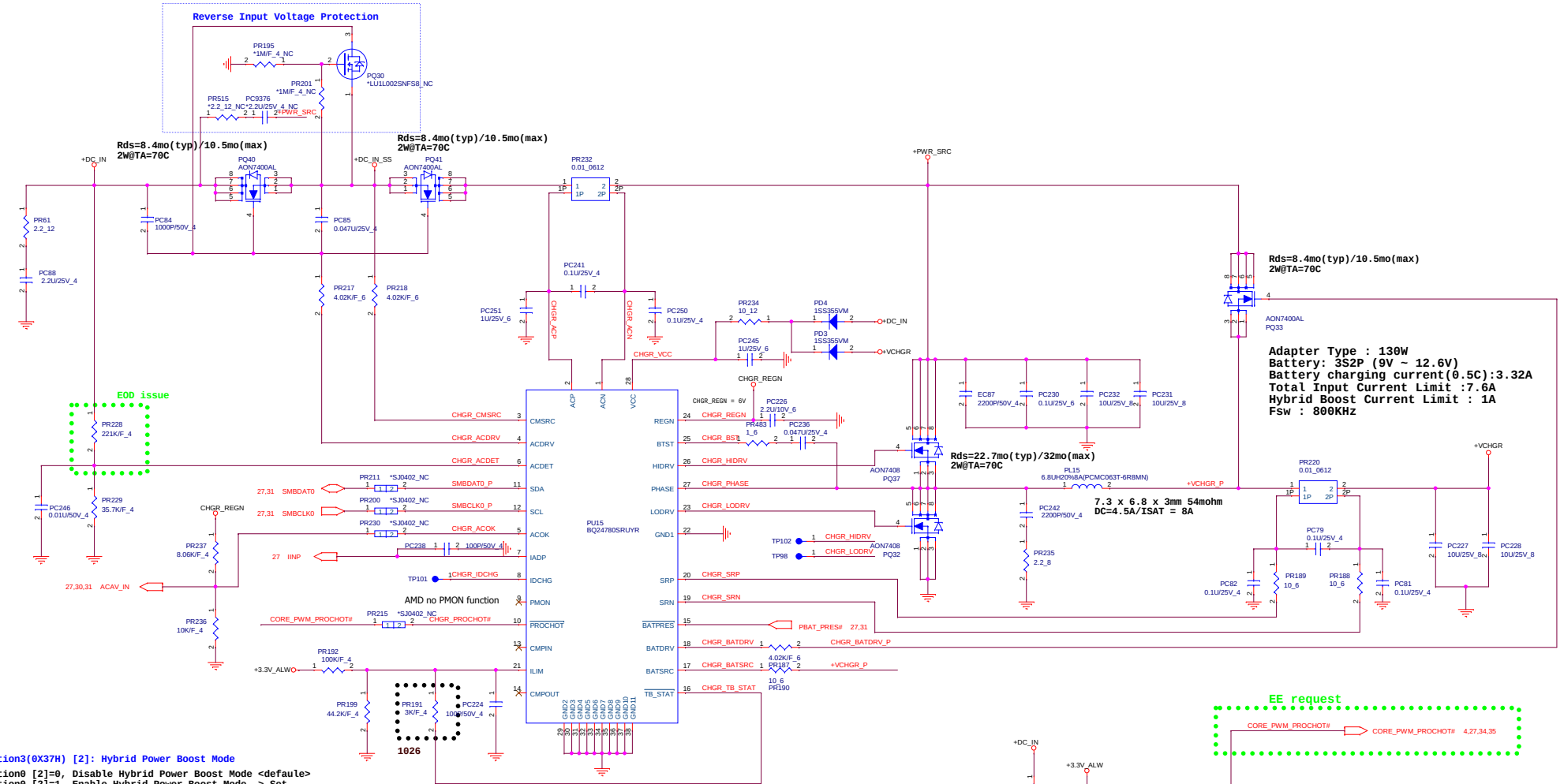
PROJECT : AM9C

Size	Document Number	Rev
	3VALW ON/PWR BTN/HOLE	A

Date: Friday, February 03, 2017 Sheet 30 of 47



Quanta Computer Inc.		
PROJECT : AM9C		
Size	Document Number: DCin & Bat	Rev: A
Date: Monday, February 06, 2017	Sheet 31 of 47	



ChargeOption3(0X37H) [2]: Hybrid Power Boost Mode

ChargeOption0 [2]=0, Disable Hybrid Power Boost Mode <defaule>
ChargeOption0 [2]=1, Enable Hybrid Power Boost Mode--> Set

ChargeOption0(0X12H) [9:8]: Switching Freq Setting

ChargeOption0 [9:8]=00, 600KHz
ChargeOption0 [9:8]=01, 800KHz <defaule> --> Set
ChargeOption0 [9:8]=10, 1MHz

ChargeOption0(0X12H) [4]: IADP Amplifier Gain

ChargeOption0 [4]=0, 20X <default> --> Set
ChargeOption0 [4]=1, 40X
IADP : Buffered Adapter Current Output VADP=20 OR 40* (VACP-VACN)

ChargeOption0(0X12H) : IDCHG Amplifier Gain

ChargeOption0 [3]=0, 8x with discharge current regulation range 0-32A
ChargeOption0 [3]=1, 16x with discharge current regulation range 0 – 16A <default> --> Set
IDCHG : Buffered Discharge Current Output VDCHG=8 OR 16* (VSRN-VSRP)

ProchotOption0(0X3CH) [15:11]:ICRIT Threshold

ProchotOption0 [15:11]=00101, 130% IDPM in REG0x3F() --> set
IDPM : Input Current (Threshold =100% of adapter rating +19.5W(with HW delay 250us))

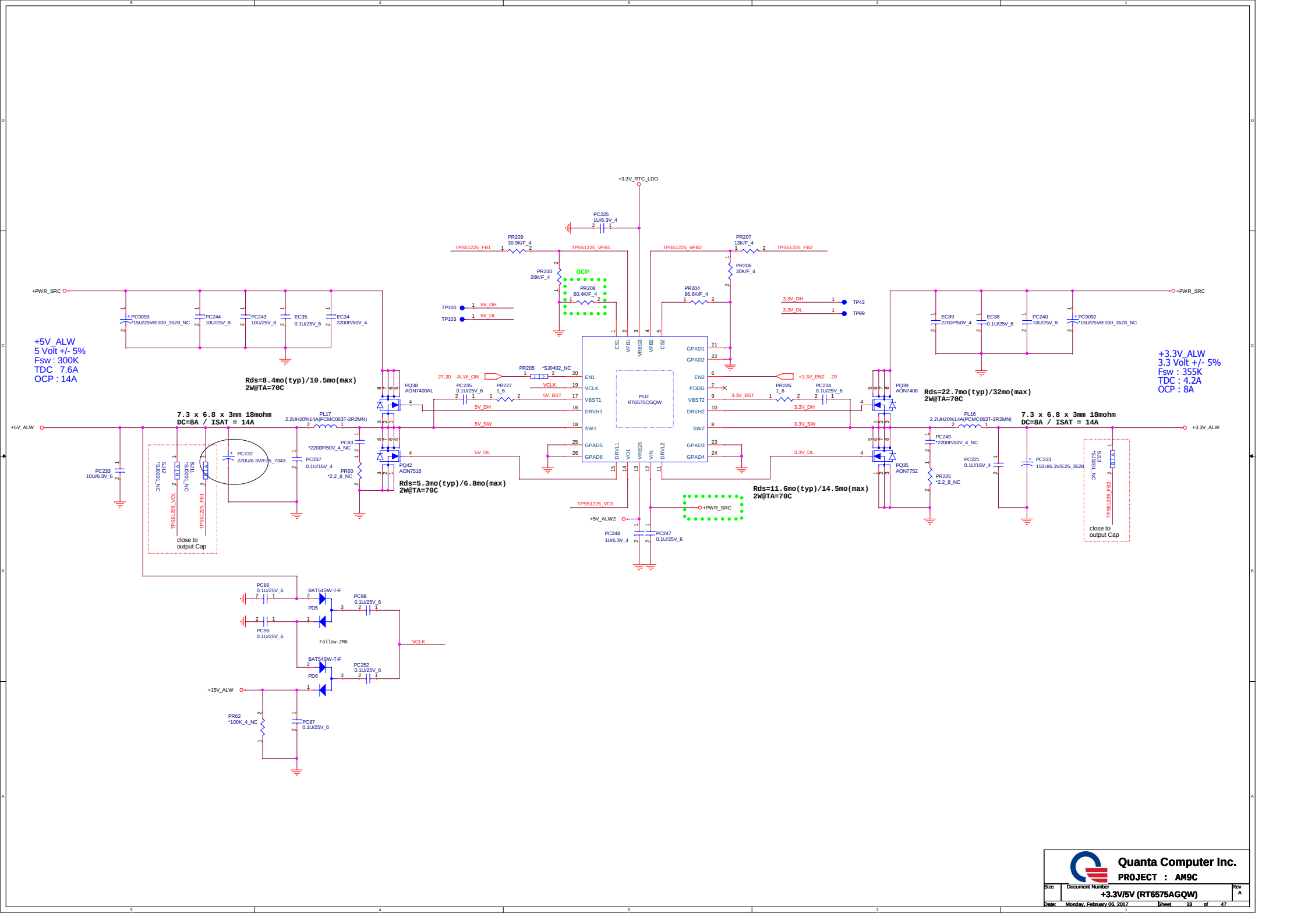
ProchotOption0(0X3CH) [10:9]:ICRIT Deglitch time

ProchotOption0 [10:9]=10, 400us ICRIT deglitch time --> set
IDPM : Input Current delay time

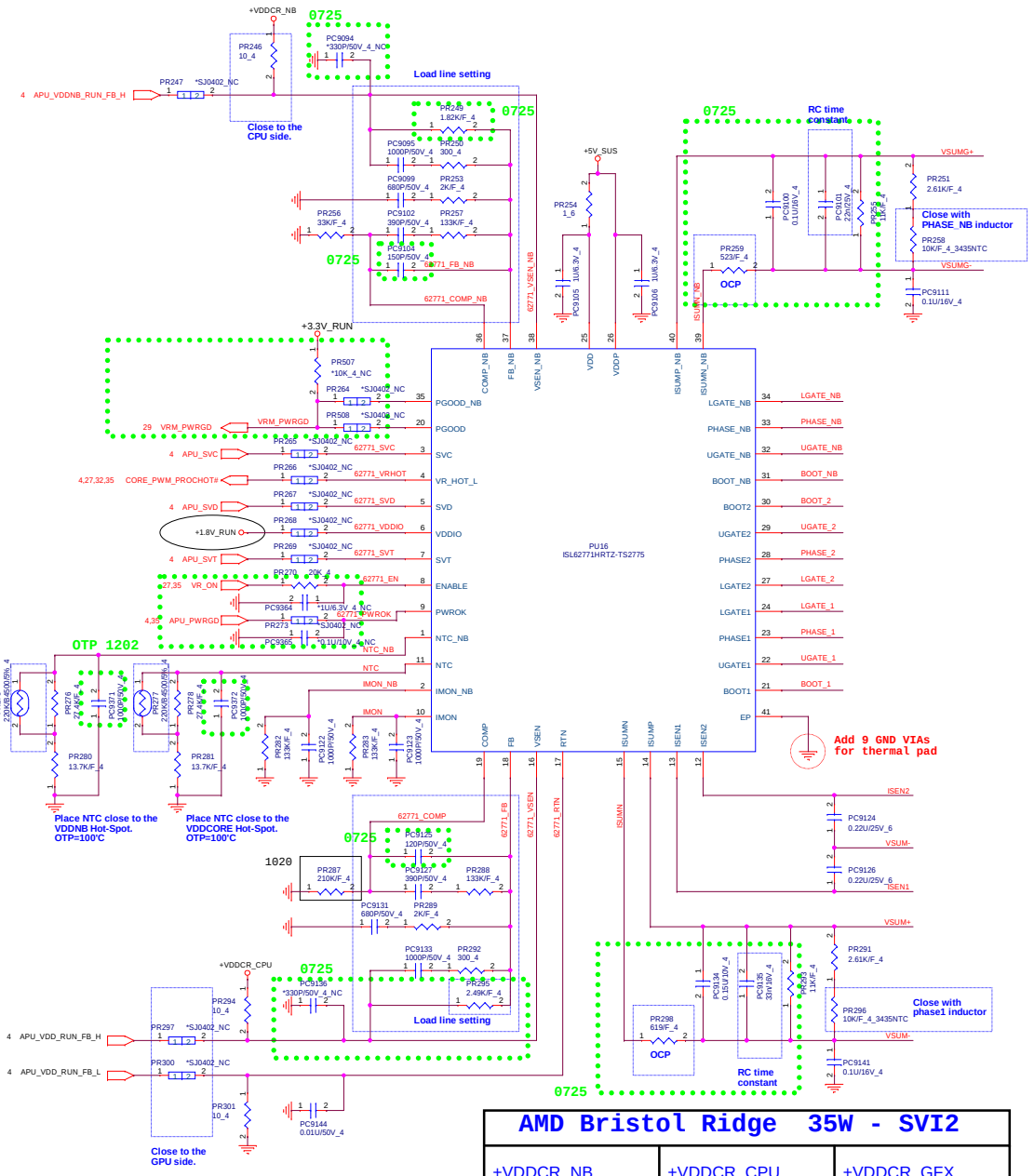
Pin16 TB_STAT#
Low : IC operating in boost mode
Hight : IC operating in normal buck mode

ILIM : VILIM=20*(VSRP-VSRN) for charge current limit (5A)
VILIM =5*(VSRN-VSRP) for discharge current limit.(20A)

Quanta Computer Inc.		
PROJECT : AM9C		
Size	Document Number: Charger (bq24780S)	Rev: A
Date: Monday, February 06, 2017	Sheet 32 of 47	



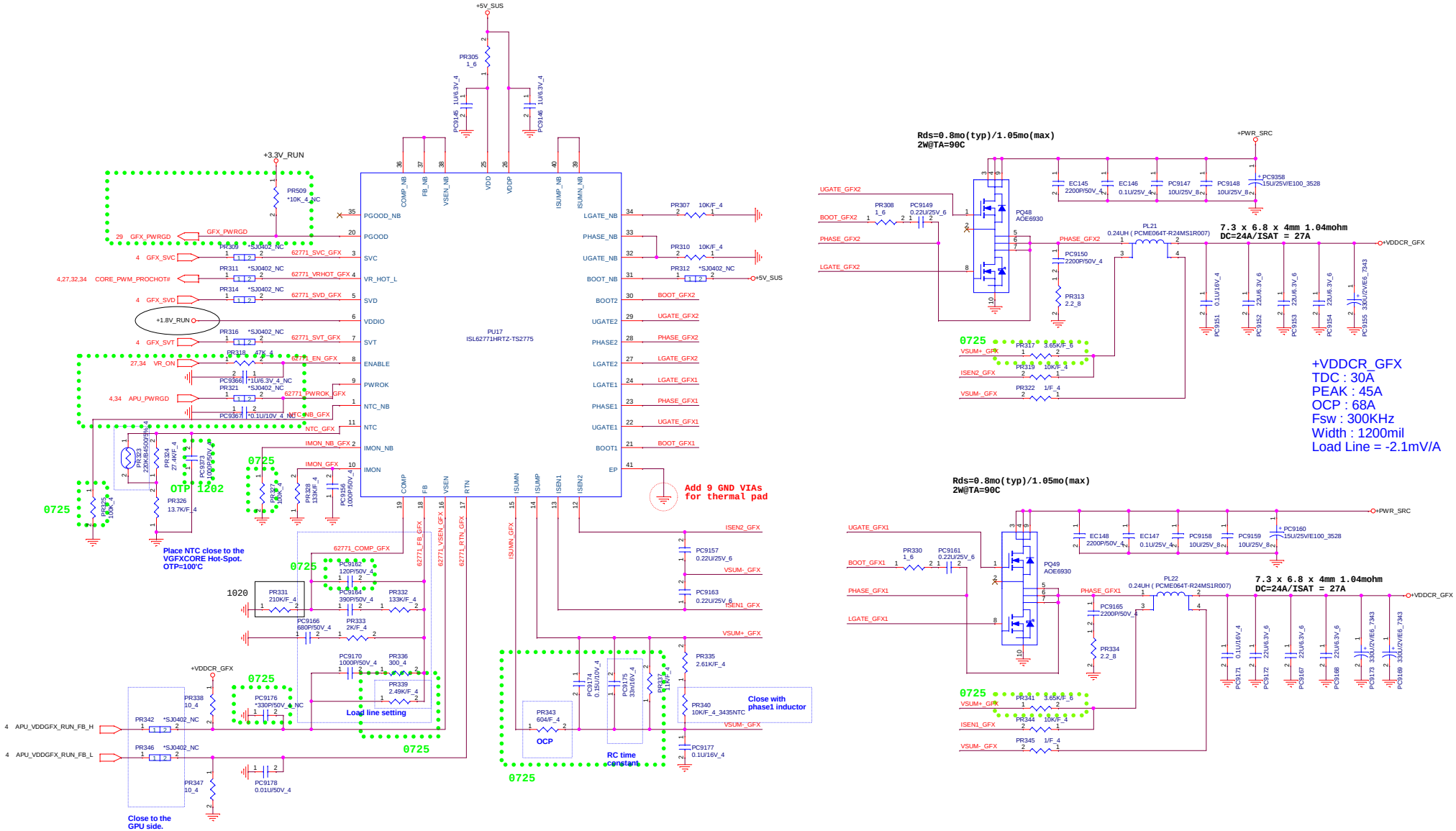
Quanta Computer Inc.			
PROJECT : AM9C			
Size	Document Number		Rev
	+3.3V/5V (RT6575AGQW)		A
Date: Monday, February 06, 2017	Sheet 33	of 47	



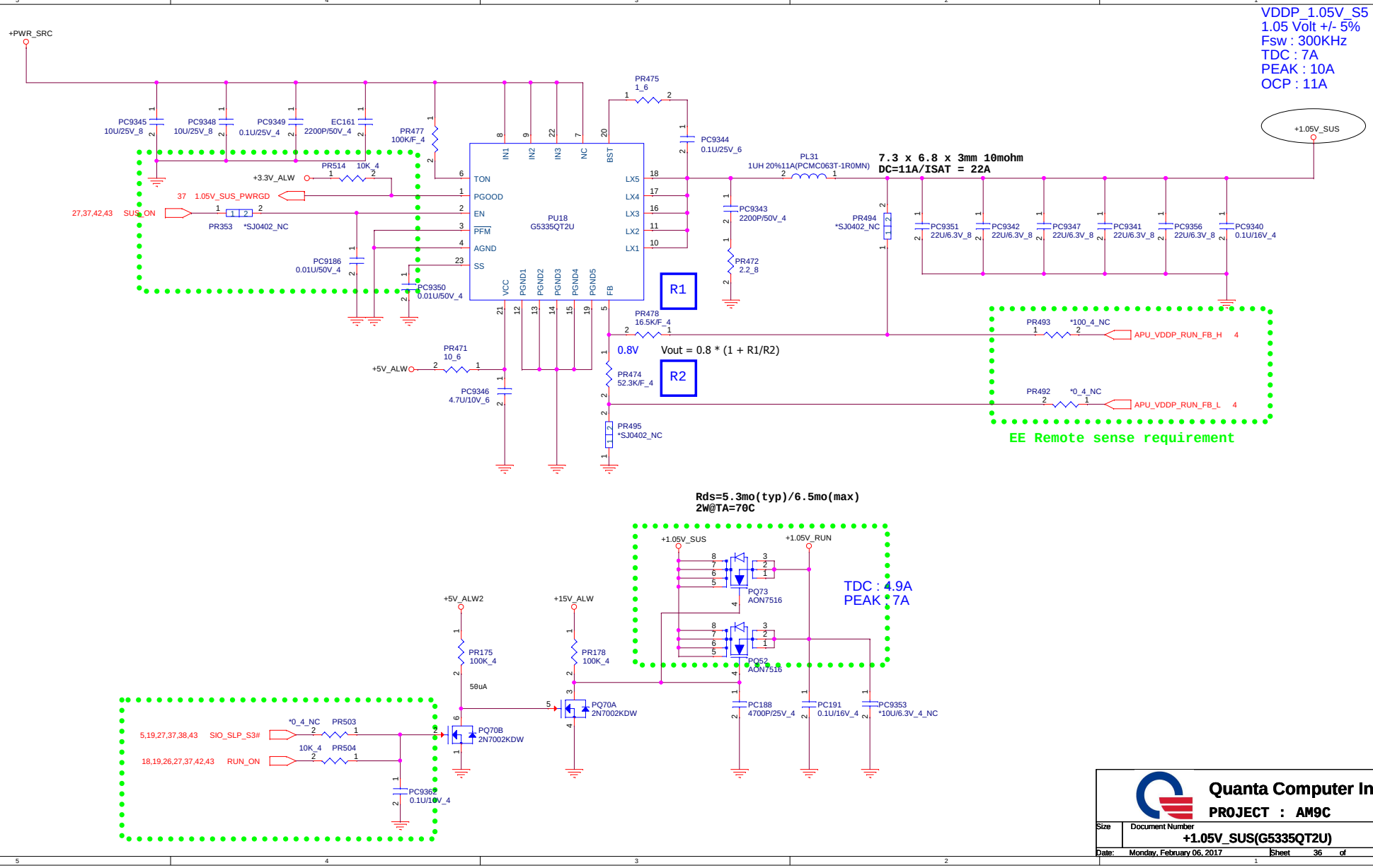
AMD Bristol Ridge 35W - SVI2		
+VDDCR_NB TDC : 12A PEAK : 17A OCP : 26A Width : 600mil Load Line = -4mV/A	+VDDCR_CPU TDC : 39A PEAK : 60A OCP : 70A Width : 1600mil Load Line = -2.1mV/A	+VDDCR_GFX TDC : 30A PEAK : 45A OCP : 68A Width : 1200mil Load Line = -2.1mV/A

Quanta Computer Inc.
PROJECT : AM9C

Size	Document Number	Rev
	+VDDCR_CPU(ISL62771)	A
Date: Monday, February 06, 2017	Sheet 34 of 47	



Quanta Computer Inc.			
PROJECT : AM9C			
Size	Document Number		Rev
	+VDDCR_GFX(ISL62771)		A
Date: Monday, February 06, 2017	Sheet 35 of 47		


VDDP_1.05V_S5
1.05 Volt +/- 5%
Fsw : 300KHz
TDC : 7A
PEAK : 10A
OCP : 11A
+PWR_SRC
+1.05V_SUS
PC9345 10U/25V_8
PC9348 10U/25V_8
PC9349 0.1U/25V_4
EC161 2200P/50V_4
PR477 100K/F_4
PR514 10K_4
+3.3V_ALW
37 1.05V_SUS_PWRGD
27,37,42,43 SUS_ON
PR353 *SJ0402_NC
PC9186 0.01U/50V_4
PC9350 0.01U/50V_4
PU18 G5335QT2U
IN1
IN2
IN3
NC
BST
TON
PGOOD
EN
PFM
AGND
SS
VCC
PGND1
PGND2
PGND3
PGND4
PGND5
FB
LX5
LX4
LX3
LX2
LX1
PR475 1_6
PC9344 0.1U/25V_6
PL31 1UH 20%11A(PCMC063T-1R0MN)
7.3 x 6.8 x 3mm 10mohm
DC=11A/ISAT = 22A
PC9343 2200P/50V_4
PR472 2.2_8
PR494 *SJ0402_NC
PC9351 22U/6.3V_8
PC9342 22U/6.3V_8
PC9347 22U/6.3V_8
PC9341 22U/6.3V_8
PC9356 22U/6.3V_8
PC9340 0.1U/16V_4
R1
PR478 16.5K/F_4
0.8V
Vout = 0.8 * (1 + R1/R2)
R2
PR474 52.3K/F_4
PR495 *SJ0402_NC
PR471 10_6
+5V_ALW
PC9346 4.7U/10V_6
PR493 *100_4_NC
APU_VDDP_RUN_FB_H 4
PR492 *0_4_NC
APU_VDDP_RUN_FB_L 4
EE Remote sense requirement
Rds=5.3mo(typ)/6.5mo(max)
2W@TA=70C
+1.05V_SUS
+1.05V_RUN
TDC : 4.9A
PEAK : 7A
PQ73 AON7516
PQ52 AON7516
+5V_ALW2
+15V_ALW
PR175 100K_4
PR178 100K_4
50uA
PQ70A 2N7002KDW
PQ70B 2N7002KDW
PC188 4700P/25V_4
PC191 0.1U/16V_4
PC9353 *10U/6.3V_4_NC
*0_4_NC PR503
5,19,27,37,38,43 SIO_SLP_S3#
10K_4 PR504
18,19,26,27,37,42,43 RUN_ON
PC9362 0.1U/16V_4
Quanta Computer Inc.
PROJECT : AM9C
Size
Document Number
+1.05V_SUS(G5335QT2U)
Rev A
Date: Monday, February 06, 2017
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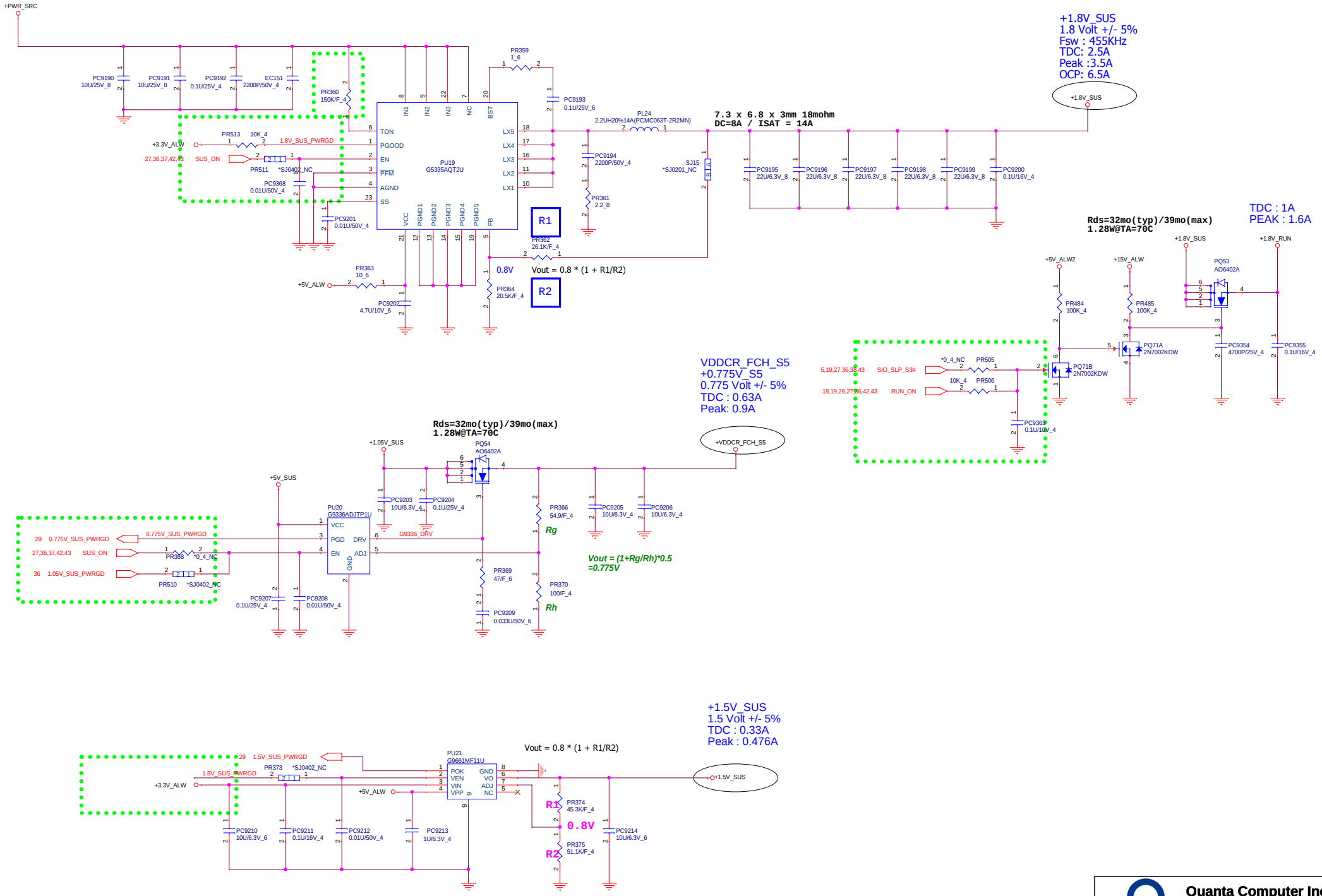
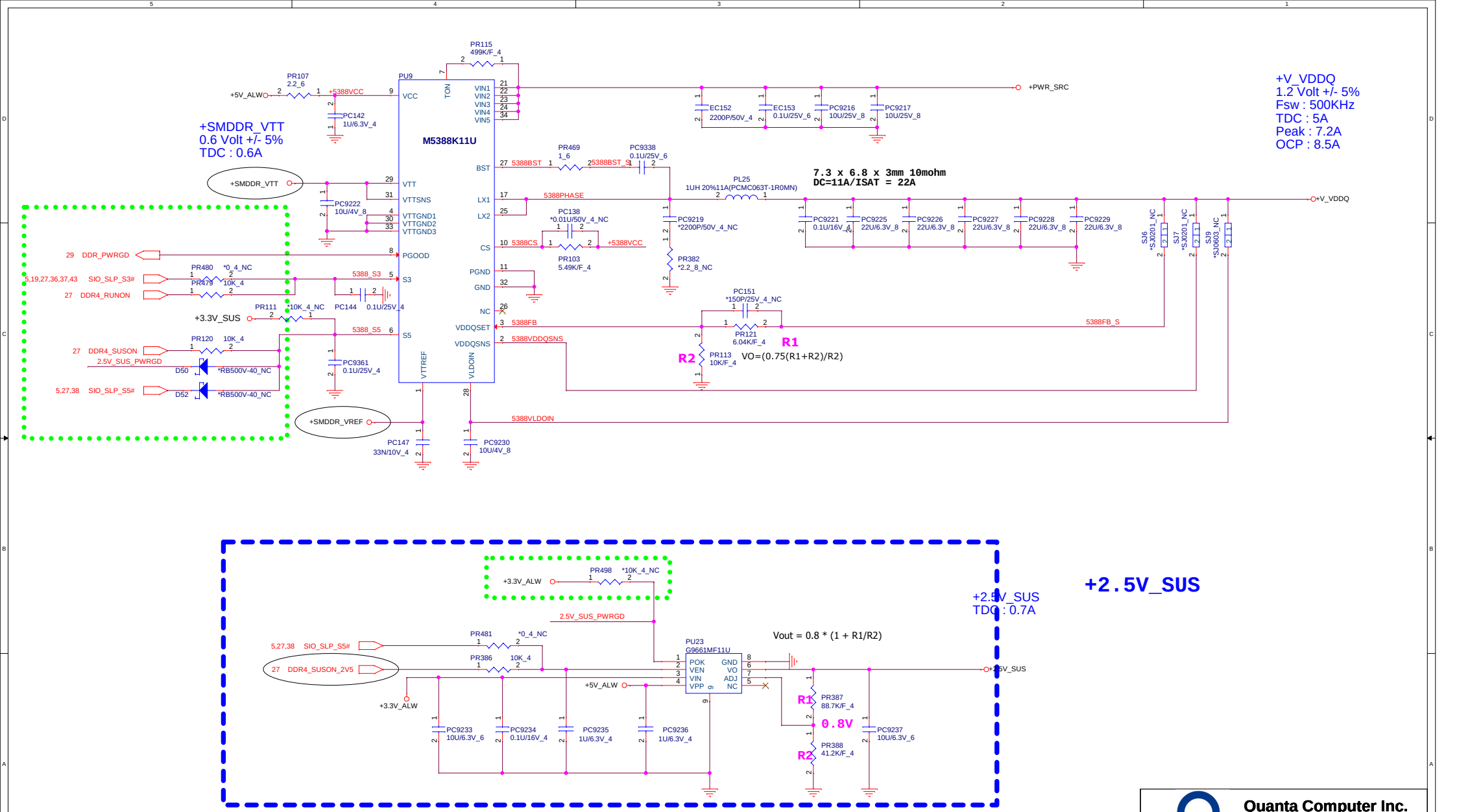

+1.8V_SUS
1.8 Volt +/- 5%
Fsw : 455KHz
TDC: 2.5A
Peak :3.5A
OCP: 6.5A
+PWR_SRC
PU19
G5335AQT2U
7.3 x 6.8 x 3mm 18mohm
DC=8A / ISAT = 14A
Vout = 0.8 * (1 + R1/R2)
0.8V
TDC : 1A
PEAK : 1.6A
Rds=32mo(typ)/39mo(max)
1.28W@TA=70C
VDDCR_FCH_S5
+0.775V_S5
0.775 Volt +/- 5%
TDC : 0.63A
Peak: 0.9A
PU20
G9336ADJTP1U
Vout = (1+Rg/Rh)*0.5
=0.775V
+1.5V_SUS
1.5 Volt +/- 5%
TDC : 0.33A
Peak : 0.476A
PU21
G9661MF11U
Quanta Computer Inc.
PROJECT : AM9C
+1.8V/+0.775V/+1.5V
Monday, February 06, 2017


+SMDDR_VTT
0.6 Volt +/- 5%
TDC : 0.6A
M5388K11U
PU9
+V_VDDQ
1.2 Volt +/- 5%
Fsw : 500KHz
TDC : 5A
Peak : 7.2A
OCP : 8.5A
7.3 x 6.8 x 3mm 10mohm
DC=11A/ISAT = 22A
PL25
1UH 20%11A(PCMC063T-1R0MN)
+PWR_SRC
+V_VDDQ
+SMDDR_VTT
+SMDDR_VREF
+3.3V_SUS
+5V_ALW
+5388VCC
DDR_PWRGD
DDR4_RUNON
DDR4_SUSON
2.5V_SUS_PWRGD
SIO_SLP_S3#
SIO_SLP_S5#
5388FB
5388VDDQSNS
5388VLDOIN
5388PHASE
5388BST
5388CS
5388_S3
5388_S5
5388FB_S
R1
R2
VO=(0.75(R1+R2))/R2)
+2.5V_SUS
+2.5V_SUS
TDC : 0.7A
Vout = 0.8 * (1 + R1/R2)
0.8V
PU23
G9661MF11U
DDR4_SUSON_2V5
Quanta Computer Inc.
PROJECT : AM9C
Document Number
VDDQ/VTT (M5388K11U)
Size
Rev
A
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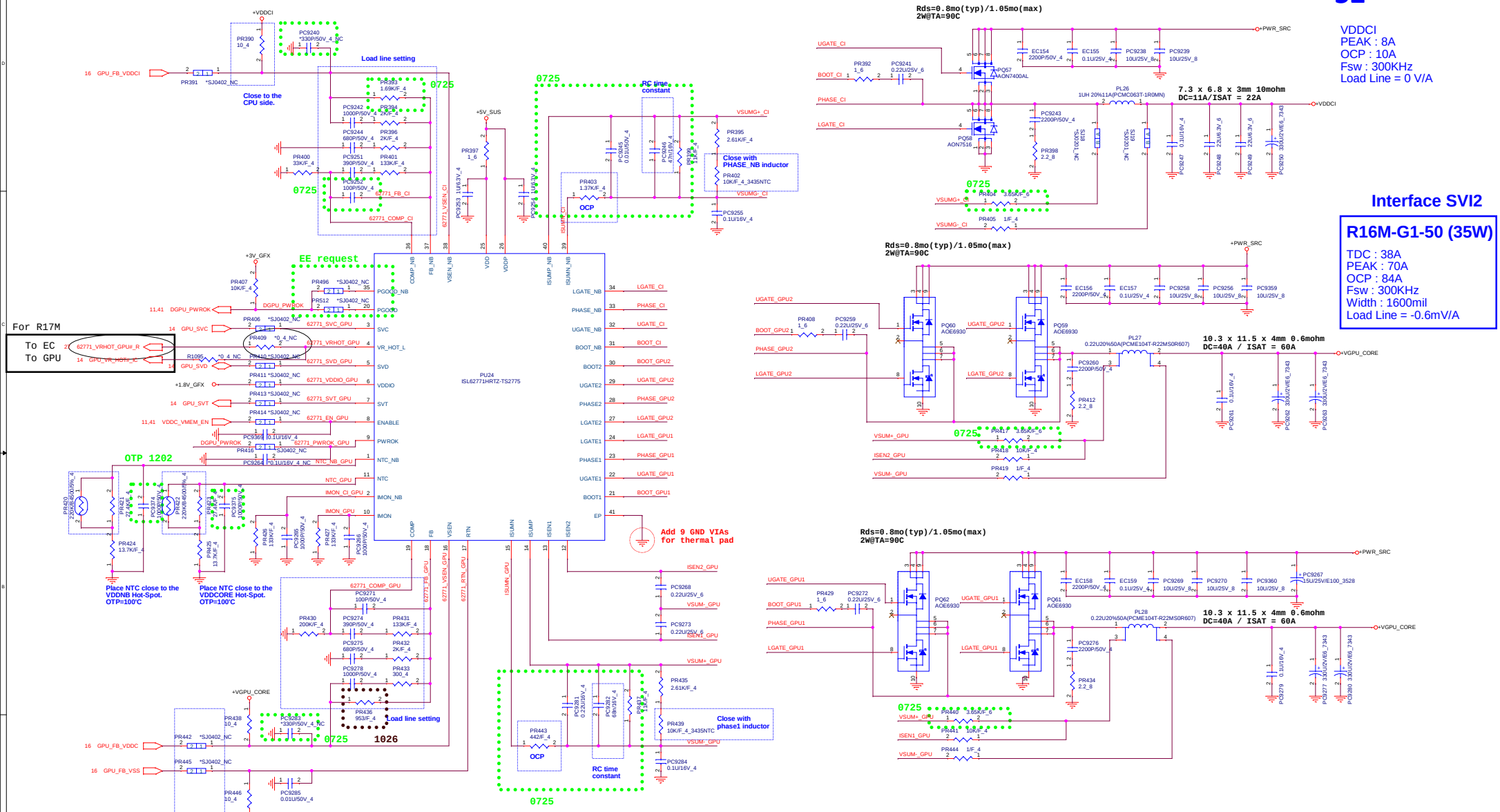
VDDCI
PEAK : 8A
OCP : 10A
Fsw : 300KHz
Load Line = 0 V/A

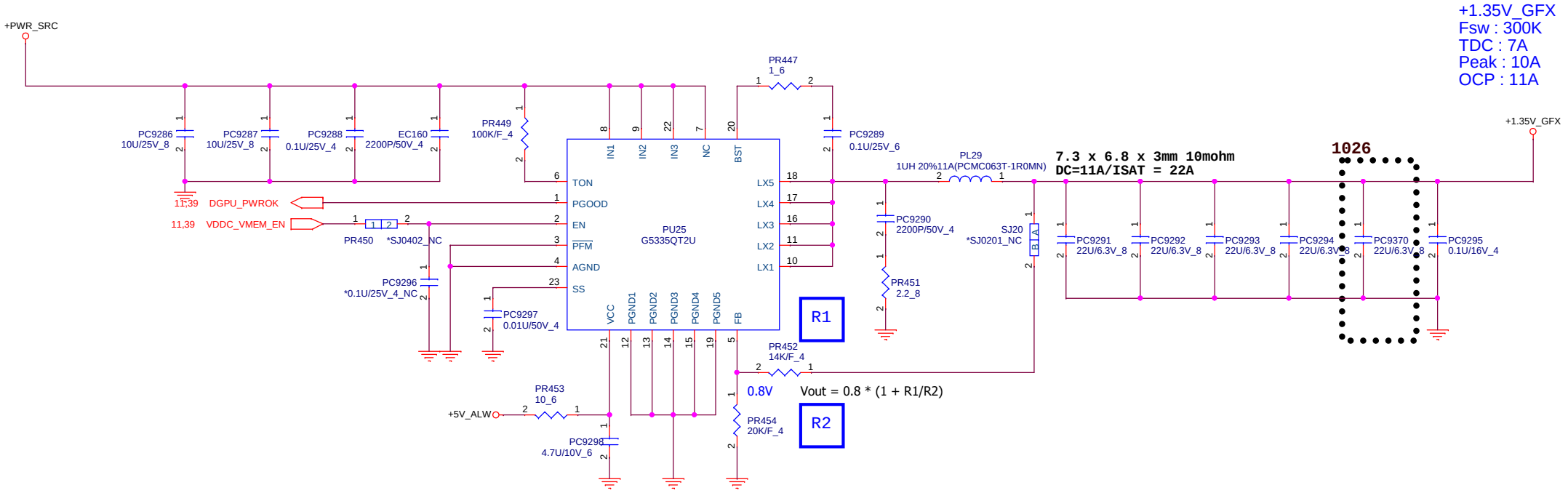
Interface SVI2

R16M-G1-50 (35W)

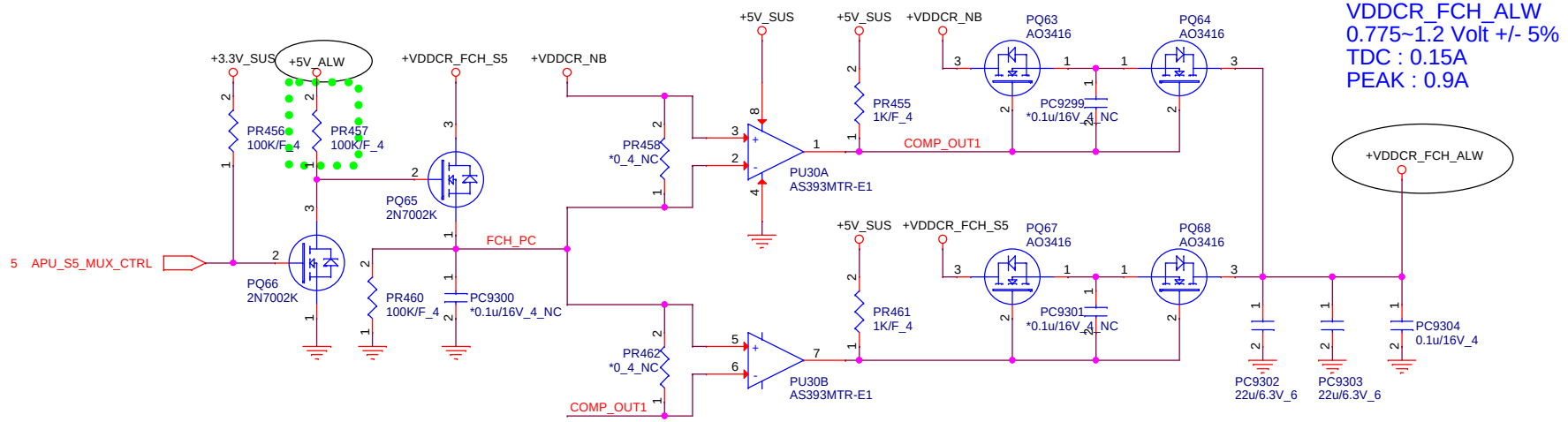
TDC : 38A
PEAK : 70A
OCP : 84A
Fsw : 300KHz
Width : 1600mil
Load Line = -0.6mV/A



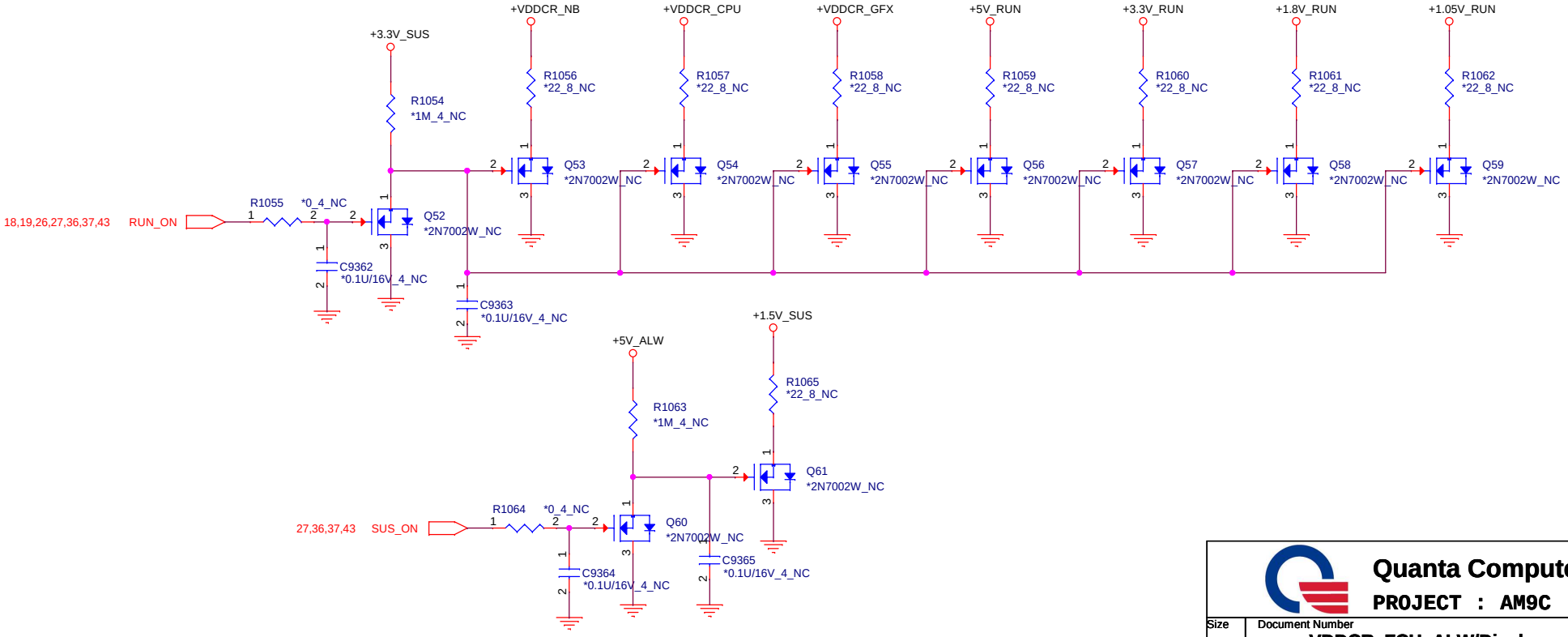
Quanta Computer Inc.	
PROJECT : AM9C	
Size	Document Number: +VGPU CORE (ISL62771) — Rev A
Date: Monday, February 06, 2017	Sheet 39 of 47



Quanta Computer Inc.		
PROJECT : AM9C		
Size	Document Number: +1.35V_GFX (G5335QT2U)	Rev: A
Date: Monday, February 06, 2017	Sheet 41 of 47	

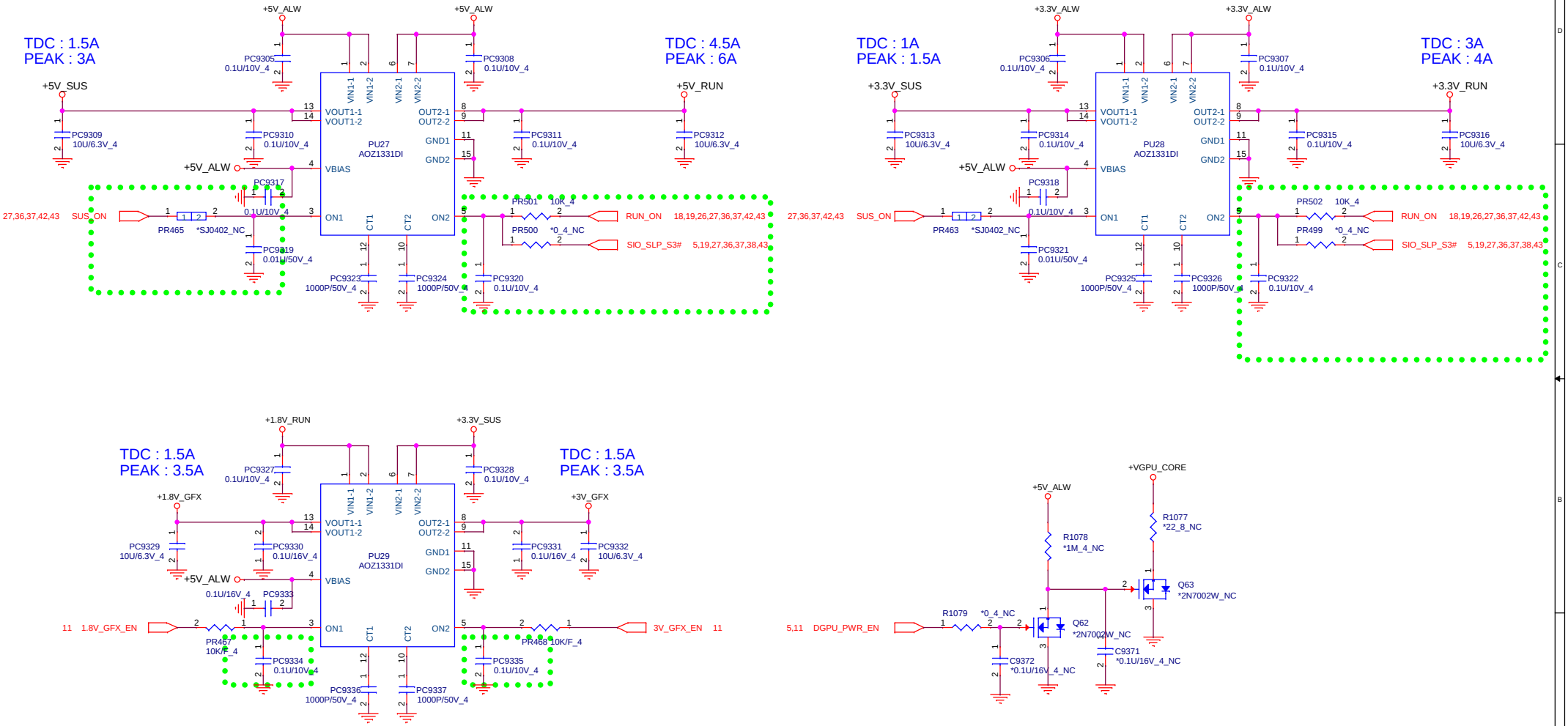


APU_S5_MUX_CTRL = High --> +VDDCR_FCH_ALW =+VDDCR_NB
APU_S5_MUX_CTRL = Low --> +VDDCR_FCH_ALW =+VDDCR_NB (+VDDCR_NB > 0.775V)
APU_S5_MUX_CTRL = Low --> +VDDCR_FCH_ALW =+VDDCR_FCH_S5 (+VDDCR_NB < 0.775V)

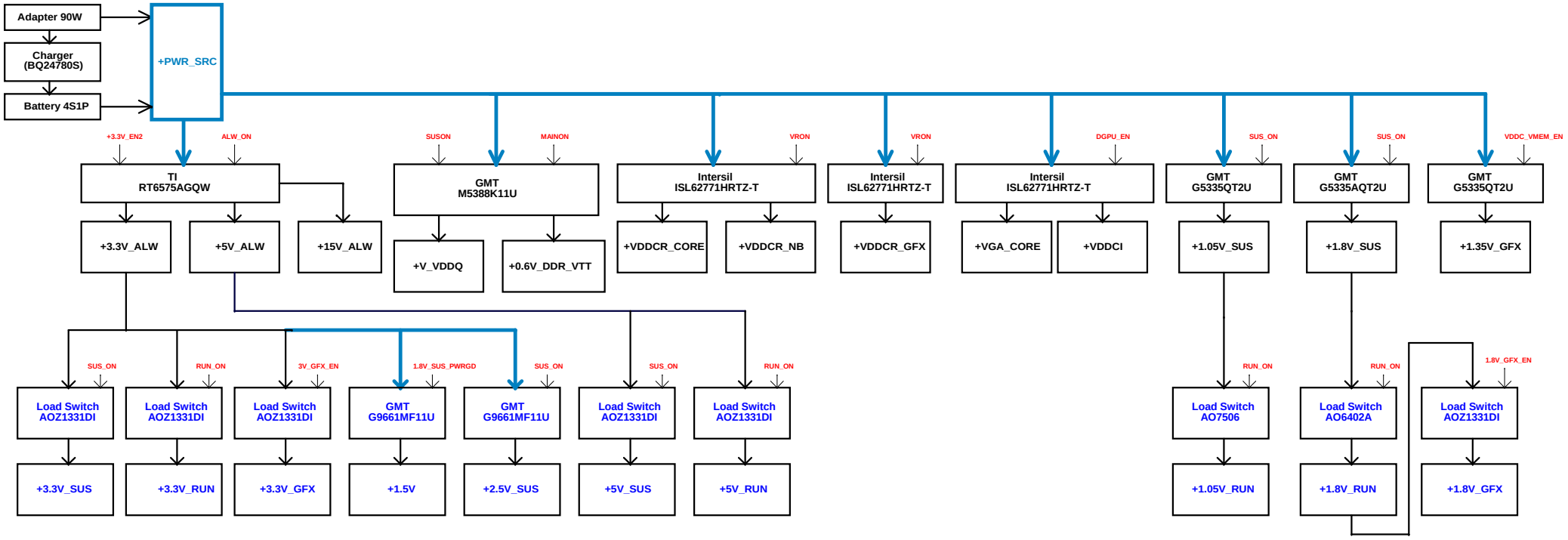


Quanta Computer Inc.
PROJECT : AM9C

Size	Document Number	Rev
	VDDCR_FCH_ALW/Discharge	A
Date: Monday, February 06, 2017	Sheet 42 of 47	



Quanta Computer Inc.		
PROJECT : AM9C		
Size	Document Number: Load Switch (SUS/RUN/GFX)	Rev: A
Date: Monday, February 06, 2017	Sheet 43 of 47	



Quanta Computer Inc.

PROJECT : AM9C

Size	Document Number	Rev
	Power Block Diagram	A

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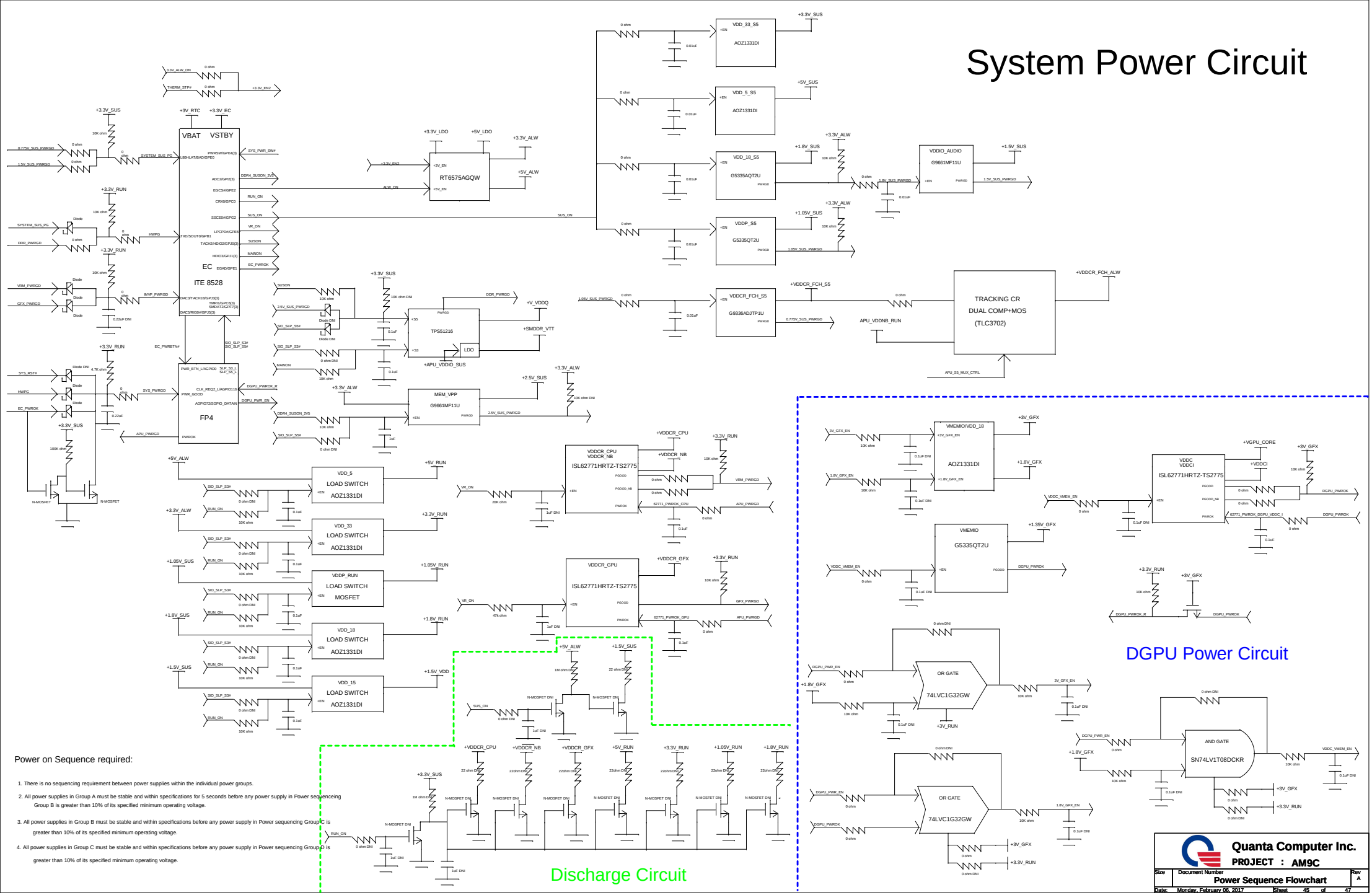
System Power Circuit



Power on Sequence required:

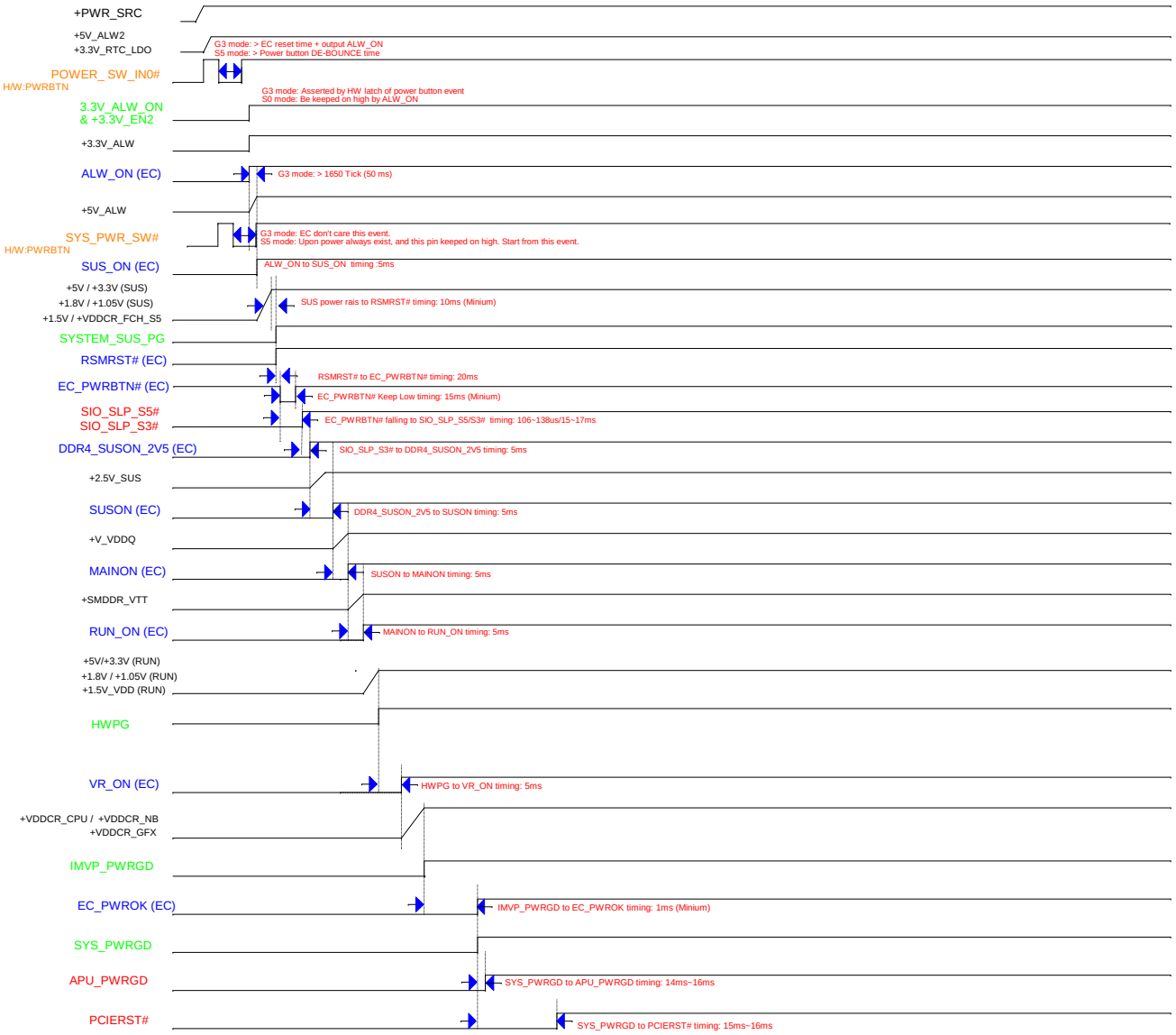
1. There is no sequencing requirement between power supplies within the individual power groups.
2. All power supplies in Group A must be stable and within specifications for 5 seconds before any power supply in Power sequencing Group B is greater than 10% of its specified minimum operating voltage.
3. All power supplies in Group B must be stable and within specifications before any power supply in Power sequencing Group C is greater than 10% of its specified minimum operating voltage.
4. All power supplies in Group C must be stable and within specifications before any power supply in Power sequencing Group D is greater than 10% of its specified minimum operating voltage.

Discharge Circuit

DGPU Power Circuit

Quanta Computer Inc.			
PROJECT : AM9C			
Size	Document Number		Rev
	Power Sequence Flowchart		A
Date: Monday, February 06, 2017	Sheet 45 of 47		

Pandora15 Sequence G3 to S0



Quanta Computer Inc.		
PROJECT : AM9C		
Size	Document Number: PSeq_G3 to S0	Rev A
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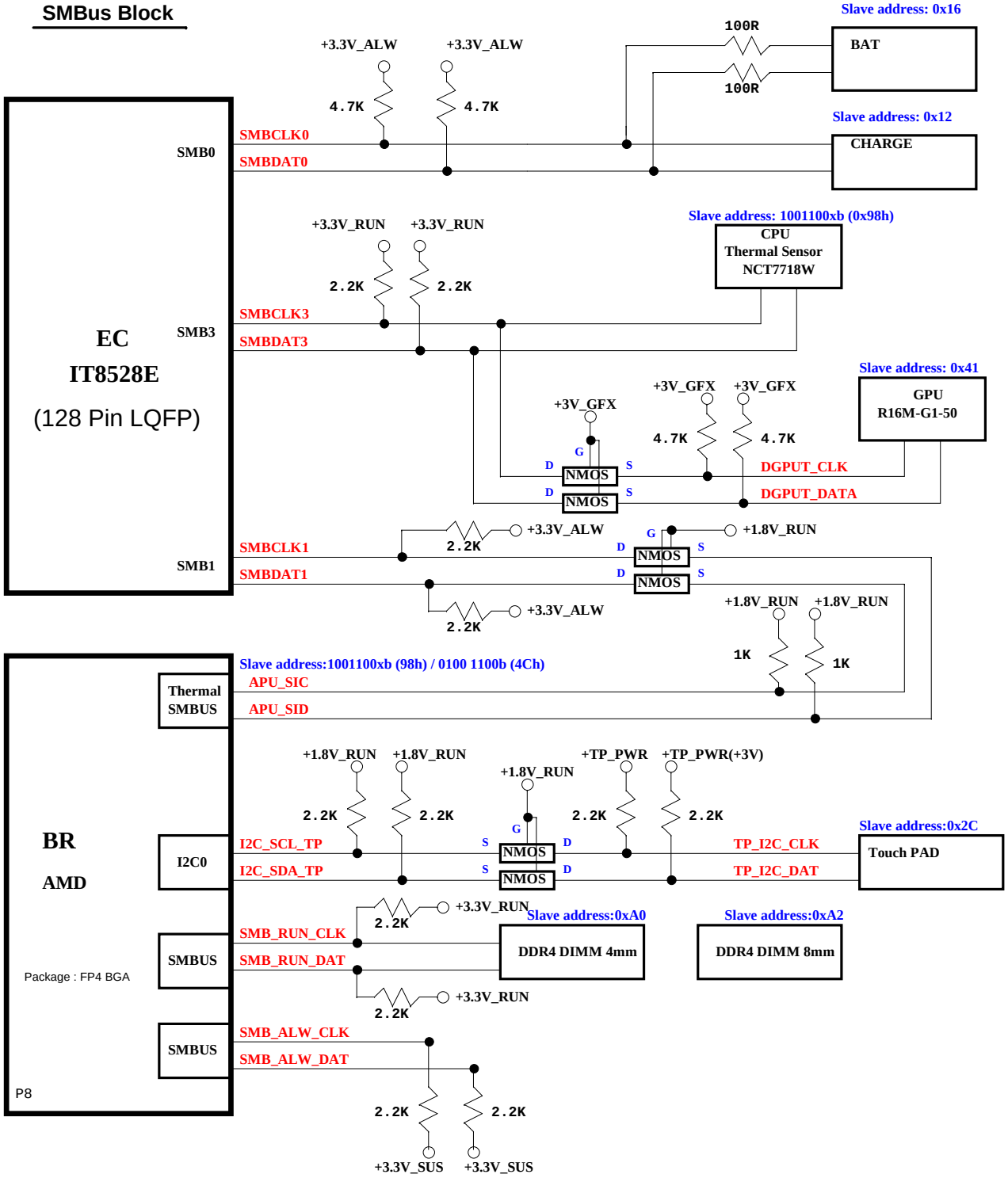
SMBus Block



PCIE	
PORT 0	NGFF WLAN
PORT 1	LAN
PORT 2	X
PORT 3	X

PCIe CLKOUT	
PORT 0	NGFF WLAN
PORT 1	LAN
PORT 2	X
PORT 3	X

SATA	
PORT 0	SSD
PORT 1	HDD
PORT 2	X
PORT 3	X

USB3.0	
PORT 0	TYPE-A 0
PORT 1	TYPE-A 1
PORT 2	POWER SHARE
PORT 3	

USB 2.0	
PORT 0	
PORT 1	WLAN BT
PORT 2	CAM
PORT 3	Card Reader
PORT 4	TYPE-A 0
PORT 5	TYPE-A 1
PORT 6	POWER SHARE
PORT 7	

Display port	
PORT 0	eDP
PORT 1	HDMI
PORT 2	

Quanta Computer Inc.
PROJECT : AM9C

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	SMBus Block	A

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