1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J64 MLB_2C

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0002902719	ENGINEERING RELEASED	2014-06-17

Tue Jun 17 14:50:55 2014

DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-1907	1	SCH,MLB_2C,J64	SCH		
820-5509	1	PCBF,MLB_2C,J64	MLB		
639-6870 "FWY2"		PCBA,MLB_2C,GD,J64			
685-00009	1	PCBA,MLB_2C,COMMON PARTS,J64	CBOM		CMN_PARTS_BOM
085-00321	1	PD PARTS,POST SMT,MLB,J64	PSMT		POST_SMT_PARTS
985-1874	1	DEV PARTS,PCBA,MLB_2C,J64	DEV1		DEVELOPMENT_LIST

DRAWING
TITLE=SHORTSTACK
ABBREV=DRAWING

DRAWING TITLE: SCHEM,MLB 2C,J64

Apple Inc.

DRAWING NUMBER: 051-1907 | SIZE: D
REVISION: 4.0.0
BRANCH:
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CPU / PCH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4526	1	HSWULT,SR16L,PRQ,C0,1.4,15W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:1.4G_OLD
337S00011	1	HSWULT,SR16T,PRQ,C0,1.4,15W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:1.4G
337S4596	1	HSWULT,SR18A,PRQ,C0,2.4,28W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:2.4G_OLD
998-00522	1	HSWULT,QGZS,QS,C0,2.6,28W,2+3,1.1,3M,BGA	U1000	CRITICAL	CPU_HSW:2.6G_NEW
337S00049	1	HSWULT,SR1ZV,PRQ,C0,2.6,28W,2+3,1.1,3M,BGA	U1000	CRITICAL	CPU_HSW:2.6G_PRQ
337S4597	1	HSWULT,SR189,PRQ,C0,2.6,28W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:2.6G_OLD
998-00521	1	HSWULT,QGZR,QS,C0,2.8,28W,2+3,1.1,3M,BGA	U1000	CRITICAL	CPU_HSW:2.8G_NEW
337S00048	1	HSWULT,SR1ZU,PRQ,C0,2.8,28W,2+3,1.2,3M,BGA	U1000	CRITICAL	CPU_HSW:2.8G_PRQ
337S4598	1	HSWULT,SR188,PRQ,C0,2.8,28W,2+3,4M,BGA	U1000	CRITICAL	CPU_HSW:2.8G_OLD
998-00520	1	HSWULT,QGZQ,QS,C0,3.0,28W,2+3,1.2,4M,BGA	U1000	CRITICAL	CPU_HSW:3.0G_NEW
337S00047	1	HSWULT,SR1ZT,PRQ,C0,3.0,28W,2+3,1.2,4M,BGA	U1000	CRITICAL	CPU_HSW:3.0G_PRQ

TBT CONTROLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U9000	CRITICAL	

PROGRAMMED PARTS

EFIROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341S00041	1	IC,EFI,V0163,J64	U2600	CRITICAL	BOOTROM:J64-POC	BASE: 335S0807,335S0812
341S00054	1	IC,EFI,V0171,J64	U2600	CRITICAL	BOOTROM:J64-LQ	

SMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S1214	1	IC,SMC12-B1,BLANK,157BGA	U4900	CRITICAL	SMC:BLANK	
341S00027	1	IC,SMC-B1,EXT,V2.21A43,POC/CM,J64	U4900	CRITICAL	SMC:J64_POC	BASE: 338S1214
341S00061	1	IC,SMC-B1,EXT,V2.22A0,EVT,J64	U4900	CRITICAL	SMC:J64_EVT	

IR

341S3647	1	IC,IR CONTROLLER,V1.0,J50	U4700	CRITICAL	IR_FRMWR:J50_PVT	BASE: 338S0375

ENET

341S00038	1	IC,ENET ROM,NUMONYX,V1.15,J64	U3690	CRITICAL	ENET_ROM:J64_POC	BASE: 335S0854
341S00039	341S00038	U3690	IC,ENET ROM,ADESTO,V1.15,J64	ENET_ROM:J64_POC	BASE: 335S1025	

TBT

335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	U9090	CRITICAL	TBTROM:BLANK	
341S00035	1	IC,EPROM,T29,FALCON RIDGE(V23.1),J64	U9090	CRITICAL	TBTROM:J64_POC	BASE: 335S0915
341S00060	1	IC,EPROM,T29,FALCON RIDGE(V24.4),J64	U9090	CRITICAL	TBTROM:J64_EVT	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0787	4	IC,SDRAM,29nm,8Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:HYNIX_4GB
333S0785	4	IC,SDRAM,29nm,16Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:HYNIX_8GB
333S0783	4	IC,SDRAM,25nm,32Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:HYNIX_16GB
333S0793	4	IC,SDRAM,25nm,8Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:MICRON_4GB
333S0791	4	IC,SDRAM,25nm,16Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:MICRON_8GB
333S0789	4	IC,SDRAM,25nm,32Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:MICRON_16GB
333S00001	4	IC,SDRAM,23nm,8Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:SAMSUNG_4GB
333S00003	4	IC,SDRAM,23nm,16Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:SAMSUNG_8GB

RAMCFG<3..2>	RAMCFG<1..0>
00 : HYNIX	00 : 4GB
01 : MICRON (ELPIDA)	01 : 8GB
10 : SAMSUNG	10 : 16GB
11 : RESERVED	11 : RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	0	RES,100K,5,MF,1/20W,0201			RAM_TYPE:HYNIX_4GB
117S0007	4	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2281,R2280		RAM_TYPE:HYNIX_4GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2292		RAM_TYPE:MICRON_4GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2284,R2281,R2280		RAM_TYPE:MICRON_4GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2294		RAM_TYPE:SAMSUNG_4GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2282,R2281,R2280		RAM_TYPE:SAMSUNG_4GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2290		RAM_TYPE:HYNIX_8GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2281		RAM_TYPE:HYNIX_8GB
117S0008	2	RES,100K,5,MF,1/20W,0201	R2292,R2290		RAM_TYPE:MICRON_8GB
117S0007	2	RES,10K,5,MF,1/20W,0201	R2284,R2281		RAM_TYPE:MICRON_8GB
117S0008	2	RES,100K,5,MF,1/20W,0201	R2294,R2290		RAM_TYPE:SAMSUNG_8GB
117S0007	2	RES,10K,5,MF,1/20W,0201	R2282,R2281		RAM_TYPE:SAMSUNG_8GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2291		RAM_TYPE:HYNIX_16GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2280		RAM_TYPE:HYNIX_16GB
117S0008	2	RES,100K,5,MF,1/20W,0201	R2292,R2291		RAM_TYPE:MICRON_16GB
117S0007	2	RES,10K,5,MF,1/20W,0201	R2284,R2280		RAM_TYPE:MICRON_16GB
117S0008	4	RES,100K,5,MF,1/20W,0201	R2294,R2292,R2291,R2290		RAM_TYPE:RESERVED
117S0007	4	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2281,R2280		RAM_TYPE:RESERVED

ALL THE RESISTERS MUST BE IN AT LEAST ONE TABLE OR BOMTOOL FLAGS AN ERROR.

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
104S0046	104S0047	ALT_CMN		ALTERNATE
107S00016	107S0118	ALT_CMN		ALTERNATE
107S0255	107S0240	ALT_CMN		ALTERNATE
107S0254	107S0241	ALT_CMN		ALTERNATE
107S0372	107S00011	ALT_CMN		ALTERNATE
127S0164	127S0162	ALT_CMN		ALTERNATE
128S0398	128S0220	ALT_CMN		ALTERNATE
128S0364	128S0264	ALT_CMN		ALTERNATE
128S0371	128S0376	ALT_CMN		ALTERNATE
128S0375	128S0378	ALT_CMN		ALTERNATE
128S0377	128S0378	ALT_CMN		ALTERNATE
132S00012	132S0401	ALT_CMN		ALTERNATE
138S0630	138S0541	ALT_CMN		ALTERNATE
138S0648	138S0652	ALT_CMN		ALTERNATE
138S0739	138S0706	ALT_CMN		ALTERNATE
138S1103	138S0719	ALT_CMN		ALTERNATE
138S00012	138S0771	ALT_CMN		ALTERNATE
138S00013	138S0772	ALT_CMN		ALTERNATE
138S0860	138S0775	ALT_CMN		ALTERNATE
138S00015	138S0777	ALT_CMN		ALTERNATE
138S00016	138S0812	ALT_CMN		ALTERNATE
138S0786	138S0847	ALT_CMN		ALTERNATE
152S1876	152S1804	ALT_CMN		ALTERNATE
152S1447	152S1873	ALT_CMN		ALTERNATE
155S0578	155S0367	ALT_CMN		ALTERNATE
197S0479	197S0478	ALT_CMN		ALTERNATE
197S0481	197S0480	ALT_CMN		ALTERNATE
197S0542	197S0544	ALT_CMN		ALTERNATE
197S0545	197S0544	ALT_CMN		ALTERNATE
197S0399	197S0392	ALT_CMN		ALTERNATE
311S00008	311S0271	ALT_CMN		ALTERNATE
311S00007	311S0426	ALT_CMN		ALTERNATE
311S00013	311S0508	ALT_CMN		ALTERNATE
311S00014	311S0515	ALT_CMN		ALTERNATE
353S00095	353S3328	ALT_CMN		ALTERNATE
353S4376	353S3384	ALT_CMN		ALTERNATE
353S3814	353S3812	TBT_MUX_ALT_TI		ALTERNATE
376S0926	376S0610	ALT_CMN		ALTERNATE
376S0972	376S0612	ALT_CMN		ALTERNATE
376S1017	376S0612	ALT_CMN		ALTERNATE
376S0572	376S0659	ALT_CMN		ALTERNATE
376S0977	376S0859	ALT_CMN		ALTERNATE
376S1129	376S0859	ALT_CMN		ALTERNATE
376S1089	376S1128	ALT_CMN		ALTERNATE
377S0155	377S0104	ALT_CMN		ALTERNATE
900-0064	870-2198	ALT_CMN		ALTERNATE
900-0089	870-2198	ALT_CMN		ALTERNATE

NON-SCHEMATIC PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
946-4345	1	MLB UV EDGE BOND,J50I	UVEB	CRITICAL		0.51 GRAM
946-3190	1	MLB ADHESIVE,LOCTITE	ADHS	CRITICAL		0.51 GRAM
						0.048GRAM

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-15

PAGE TITLE: COMMON PARTS TABLE

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

BRANCH:

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"G3" RAILS

ON WHEN UNIT HAS BATTERY POWER

BATTERY 3.3V G3

PPVBATT_G3_RTC — OUT 19 78 81

DIODES 3.3V G3

PP3V3_G3_RTC — OUT 9 13 14 19 78

FET 3.3V ENET

PP3V3_ENET — OUT 28 29 78

VR 1.2V ENET

PP1V2_ENET — OUT 28 29 78

"G3H" RAILS

ON WHEN UNIT HAS AC POWER

PSU 12V G3H

PP12V_G3H_PSU — OUT 44 61 77 81

PP12V_G3H — OUT 44 51 55 59 60 61 77

PP12V_G3H_CPU — OUT 44 57 58 77

PP12V_G3H_DDR — OUT 44 56 77

PP12V_G3H_TBT — OUT 44 66 67 77

LDO 5V G3H

PP5V_G3H — OUT 38 39 41 55 60 78

VR 3.3V G3H

PP3V3_G3H — OUT 3 19 29 32 34 36 39 40 41 52 53 55 56 64 66 67 78

"S5" RAILS

STANDARD STANDBY STATE.

FET 3.3V S5

PP3V3_S5 — OUT 9 12 14 15 16 17 18 19 52 53 54 69 78 81

GND

PP3V3_S4 — 70 54 53 52 41 38 32 31 16 4 78

PP3V3_G3H — 52 41 40 39 36 34 32 29 19 3 78 67 66 64 56 55 53

R0600 200 1% 1/16W MF-LF 2402

ITS_PLUGGED_IN NO_TEST=TRUE

LED0600 GREEN-3.6MCD 2.0X1.25MM-SM DEVELOPMENT

PP3V3_G3H — 78 67 66 64 52 41 40 39 36 34 32 29 19 3 56 55 53

R0602 200 1% 1/16W MF-LF 2402

ITS_ALIVE NO_TEST=TRUE

LED0602 GREEN-3.6MCD 2.0X1.25MM-SM DEVELOPMENT

PP3V3_G3H — 78 67 66 64 52 41 40 39 36 34 32 29 19 3 56 55 53

R0603 200 1% 1/16W MF-LF 2402

ITS_BREATHING NO_TEST=TRUE

LED0603 GREEN-3.6MCD 2.0X1.25MM-SM DEVELOPMENT

ITS_BREATHING_Q

Q0603 SSM3K15FV SOD-VESM-HF DEVELOPMENT

SMC_SYS_LED — IN 40 39

PP3V3_S0 — 78 69 68 65 63 61 54 53 52 51 33 29 19 17 16 14 13 12 8 49 47 46 45 44 43 42 41 35 34 81

R0605 200 1% 1/16W MF-LF 2402

CATERR_LED_R

R0615 100K 5% 1/16W MF-LF 2402

LED0605 RED-631NM-0.02A-112MCD LTST-C171KRKT-SM

CATERR_LED — 82

Q0605 DMB53D0UV SOT-563

CATERR_R

R0616 20K 5% 1/16W MF-LF 402

CPU_CATERR_L — IN 74 40 7

CPU_CATERR_RL

Q0605 DMB53D0UV SOT-563

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE

POWER FLOW, DIAG LEDS

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

BRANCH

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"S4" RAILS

ON IN RUN AND SLEEP

VR 5V S4

PP5V_S4_REG → OUT 43 55 78

PP5V_S4 → OUT 36 37 39 43 52 56 59 60 70 78

FET 3.3V S4

PP3V3_S4 → OUT 3 16 31 32 38 41 52 53 54 70 78

"S3" RAILS

ON IN RUN AND SLEEP

FET 1.8V SW

PP1V8_S3_REG → OUT 43 56 78

PP1V8_S3 → OUT 23 24 25 26 43 60 78

FET 1.2V SW

PP1V2_S3_REG → OUT 43 56 78

PP1V2_S3_MEM → OUT 9 11 22 23 24 25 26 43 53 61 78

VR 0.6V S3

PP0V6_S3_DDRVTT → OUT 27 56 77

"S0" RAILS

ON IN RUN ONLY

FET 5V S0

PP5V_S0 → OUT 17 18 19 35 46 50 52 54 57 58 78 81

FET 3.3V S0

PP3V3_S0 → OUT 52 53 54 61 63 65 68 69 78 81 3 9 12 13 14 16 17 19 20 33 34 35 41 42 43 44 45 46 47 49 51

LDO 1.5V S0

PP1V5_S0 → OUT 9 12 19 35 47 60 61 69 78

VR 1.05V S0

PP1V05_S0 → OUT 7 9 12 16 17 19 41 43 57 59 78 81

VR CPU-CORE S0

PPVCC_S0_CPU → OUT 9 11 43 58 78

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE

POWER FLOW CONT.

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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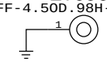
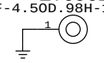
CPU / PCH HEATSINK MOUNTING HOLES / NUTS

ZT0960
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0961
STDOFF-4.5OD.98H-1.1-3.48-TH



ZT0962
STDOFF-4.5OD.98H-1.1-3.48-TH



ZT0966
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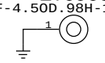


860-0988

FINSTACK END MOUNT

ZT0915
4.0OD1.9H-M1.6X0.35

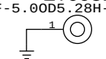
860-00012

SPEAKER BOSSES

ZT0950
STDOFF-4.0OD4.56H-1.3-2.22-TH
SHORT

860-00010

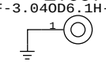
ZT0951
STDOFF-5.0OD5.28H-1.3-2.22-TH
TALL



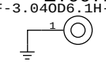
860-00098

BLOWER SUPPORT POSTS

ZT0970
STDOFF-3.04OD6.1H-1.3-1.9-TH1



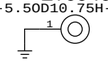
ZT0971
STDOFF-3.04OD6.1H-1.3-1.9-TH1



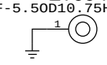
452-2349

ENCLOSURE/MLB MOUNTING POSTS

ZT0940
STDOFF-5.5OD10.75H-1.1-3.48-TH



ZT0941
STDOFF-5.5OD10.75H-1.1-3.48-TH



860-1299

CONNECTOR RETAINING CLIP BOSSES

ZT0980
3.5OD2.0H-SM-J64

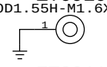
ZT0981
3.5OD2.0H-SM-J64

ZT0982
3.5OD2.0H-SM-J64

860-00085

REAR I/O FENCE MOUNTING BOSS

ZT0910
4.0OD1.55H-M1.6X0.35-ST



ZT0912
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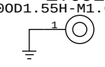
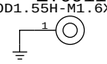
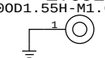


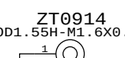
ZT0911
4.0OD1.55H-M1.6X0.35-ST



ZT0913
4.0OD1.55H-M1.6X0.35-ST



ZT0914
4.0OD1.55H-M1.6X0.35-ST

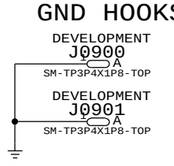


860-1438

GND HOOKS

DEVELOPMENT
J0900
SM-TP3P4X1P8-TOP

DEVELOPMENT
J0901
SM-TP3P4X1P8-TOP



PLACE ONE ON EACH SIDE OF BOARD IN EASILY ACCESSIBLE LOCATION. LABEL "GND".

REMINDER TO SPRINKLE GND VIAS AROUND THE BOARD.

ZH0933
HOLE-VIA

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
MECHANICAL STAND-OFFS, BOSSES, ETC.

Apple Inc.

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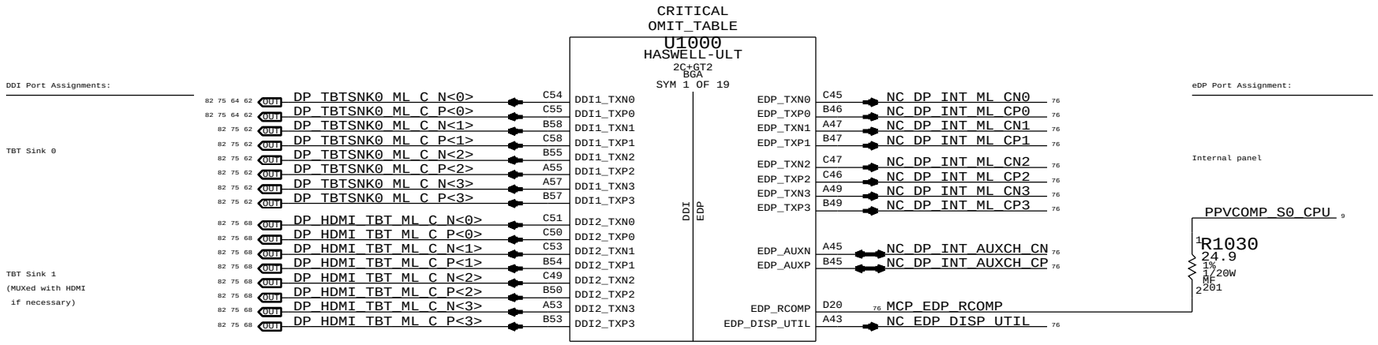

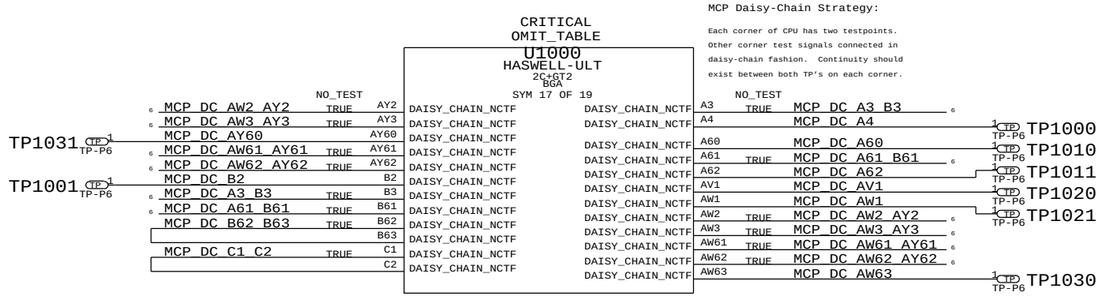

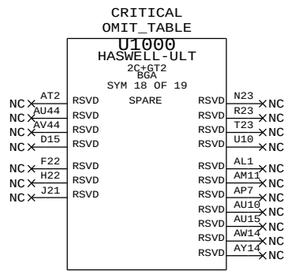

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16

PAGE TITLE: CPU GFX/NCTF/RSVD

Apple Inc.

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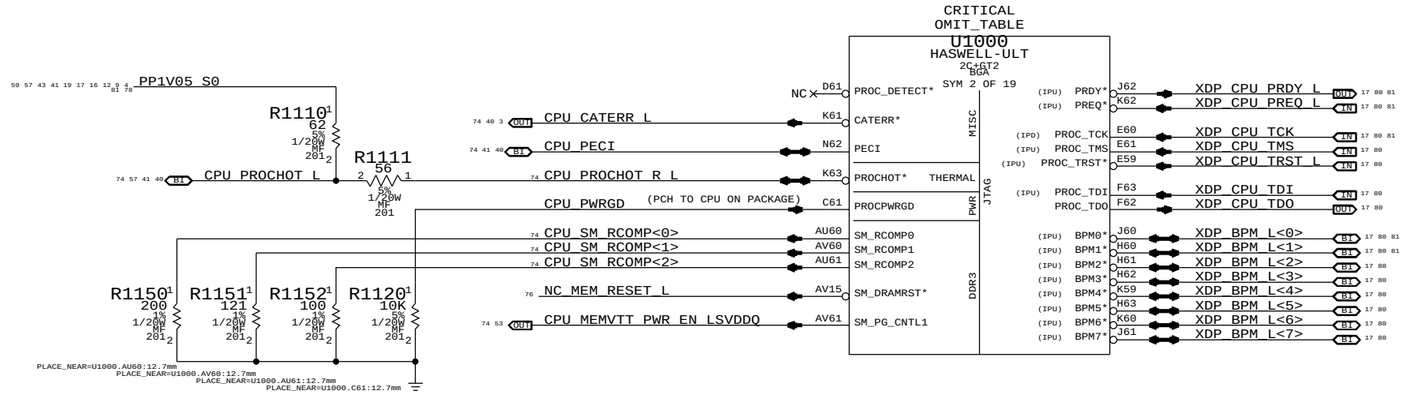
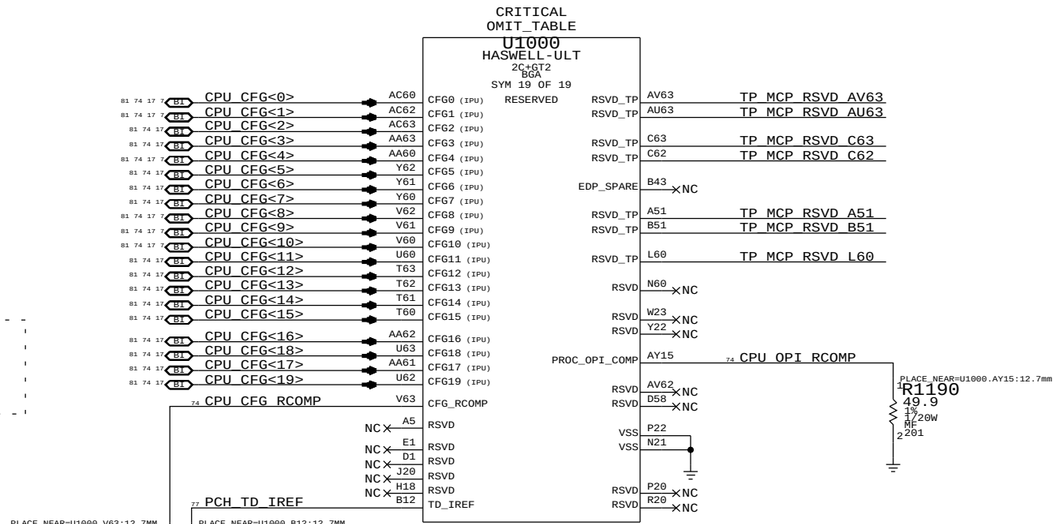
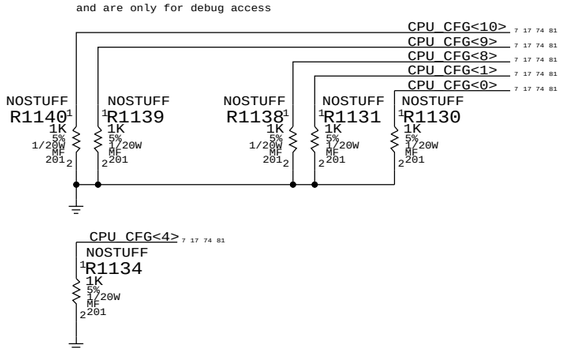




CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

THESE CAN BE PLACED CLOSE TO J2400
and are only for debug access



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16

PAGE TITLE

CPU Misc/JTAG/CFG/RSVD

Apple Inc.

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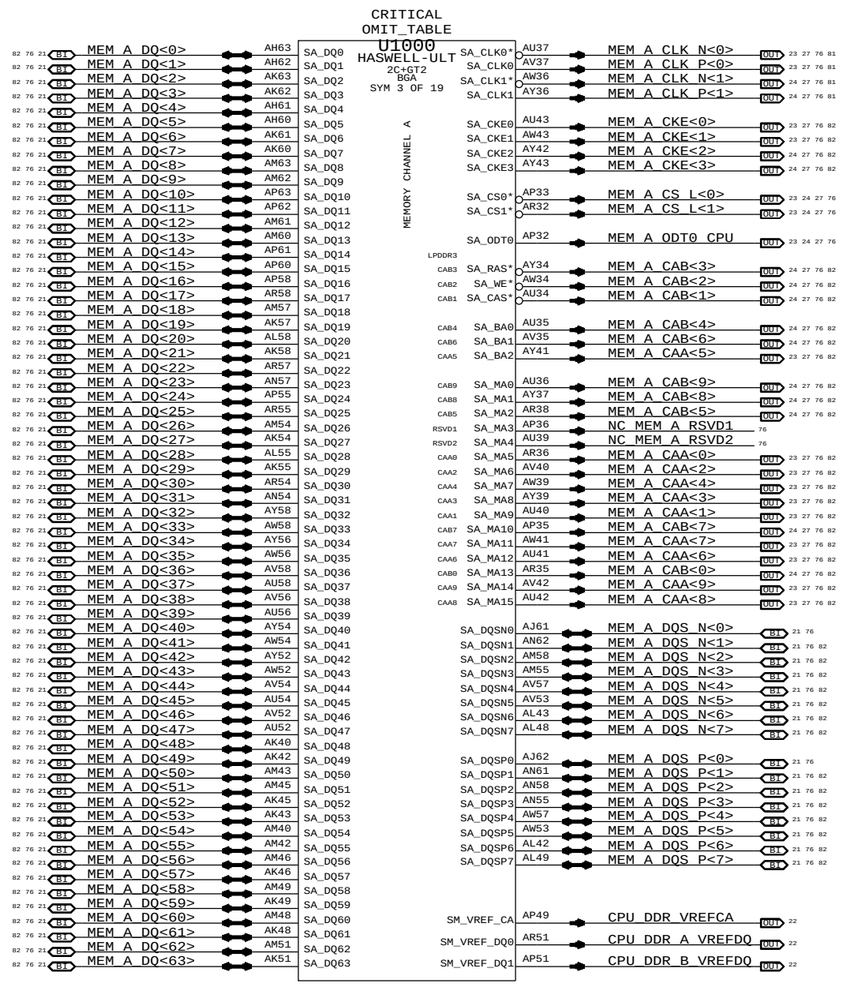

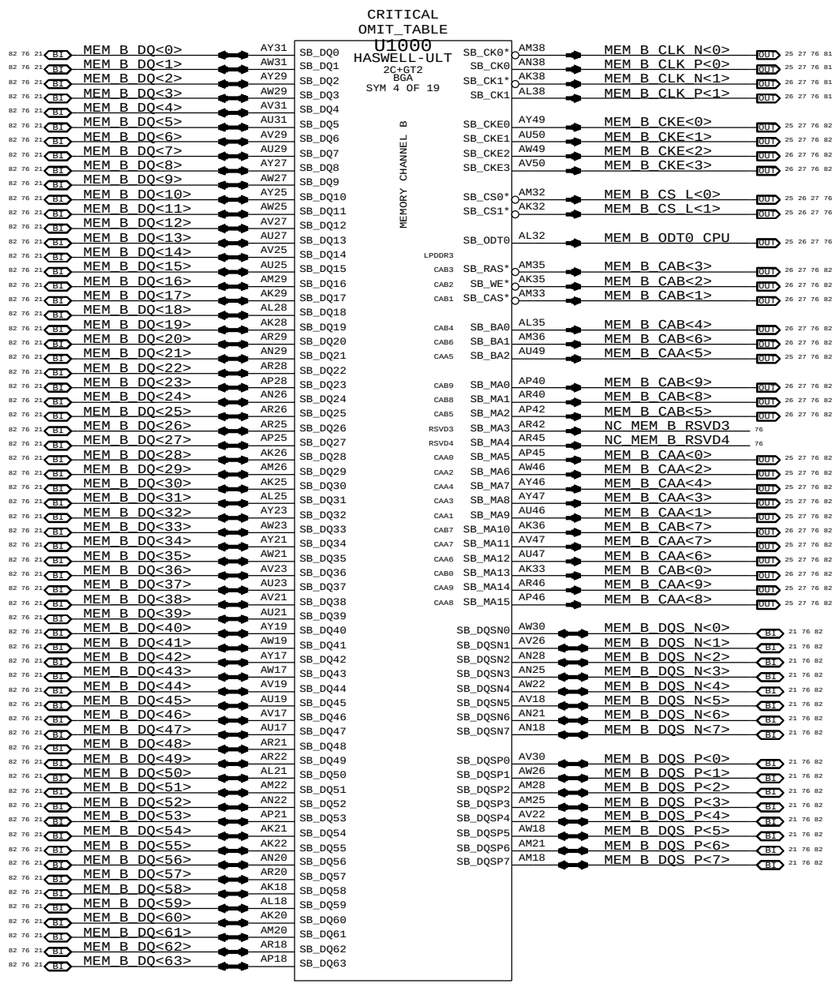

SYNC_MASTER=J70_DINI SYNC_DATE=2014-01-17

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CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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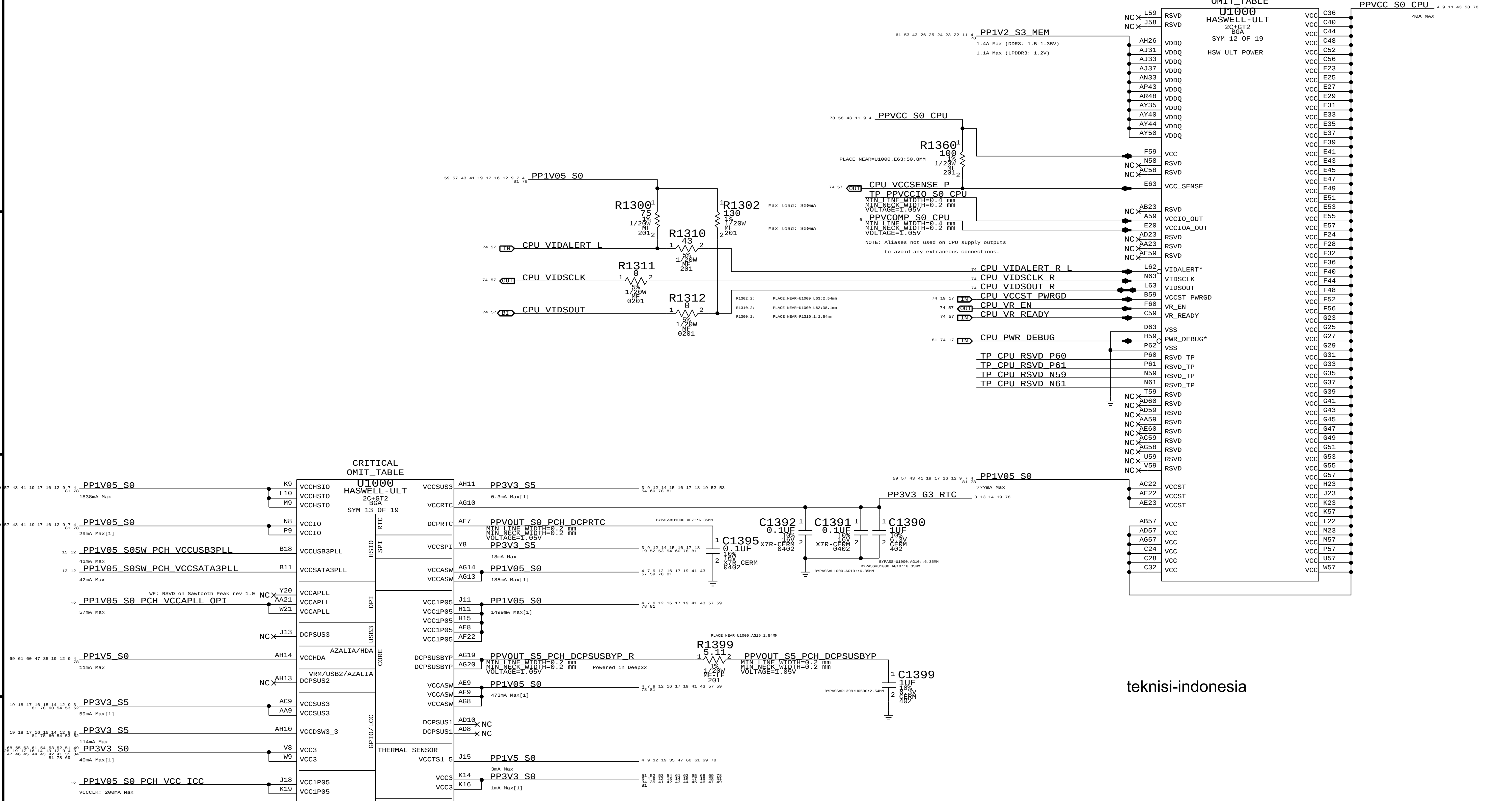
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



CRITICAL
OMIT_TABLE
U1000
HASWELL-ULT
2C+GT2
BGA
SYM 12 OF 19
HSW ULT POWER
PPVCC_S0_CPU
40A MAX
PP1V2_S3_MEM
1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)
VDDQ
VCC
RSVD
VCC_SENSE
VCCIO_OUT
VCCIOA_OUT
PPVCC_S0_CPU
R1360
100
1%
1/20W
MF
201
PLACE_NEAR=U1000.E63:50.8MM
CPU_VCCSENSE_P
TP_PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
PPVCOMP_S0_CPU
NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.
PP1V05_S0
R1300
75
1%
1/20W
MF
201
R1302
130
1%
1/20W
MF
201
Max load: 300mA
R1310
43
5%
1/20W
MF
201
R1311
0
5%
1/20W
MF
0201
R1312
0
5%
1/20W
MF
0201
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R1302.2: PLACE_NEAR=U1000.L63:2.54mm
R1310.2: PLACE_NEAR=U1000.L62:38.1mm
R1300.2: PLACE_NEAR=R1310.1:2.54mm
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCST_PWRGD
CPU_VR_EN
CPU_VR_READY
CPU_PWR_DEBUG
TP_CPU_RSVD_P60
TP_CPU_RSVD_P61
TP_CPU_RSVD_N59
TP_CPU_RSVD_N61
VIDALERT*
VIDSCLK
VIDSOUT
VCCST_PWRGD
VR_EN
VR_READY
VSS
PWR_DEBUG*
RSVD_TP
VCCST
PP1V05_S0
???mA Max
PP3V3_G3_RTC
C1392
0.1UF
10%
16V
X7R-CERM
0402
C1391
0.1UF
10%
16V
X7R-CERM
0402
C1390
1UF
10%
6.3V
CERM
402
C1395
0.1UF
10%
16V
X7R-CERM
0402
BYPASS=U1000.AE7::6.35MM
BYPASS=U1000.AG10::6.35MM
CRITICAL
OMIT_TABLE
U1000
HASWELL-ULT
2C+GT2
BGA
SYM 13 OF 19
LPT LP POWER
PP1V05_S0
1838mA Max
VCCHSIO
VCCIO
20mA Max[1]
PP1V05_S0SW_PCH_VCCUSB3PLL
VCCUSB3PLL
41mA Max
PP1V05_S0SW_PCH_VCCSATA3PLL
VCCSATA3PLL
42mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP1V05_S0_PCH_VCCAPLL_OPI
VCCAPLL
57mA Max
DCPSUS3
PP1V5_S0
VCCHDA
11mA Max
DCPSUS2
PP3V3_S5
VCCSUS3
59mA Max[1]
VCCDSW3_3
114mA Max
PP3V3_S0
VCC3
40mA Max[1]
PP1V05_S0_PCH_VCC_ICC
VCC1P05
VCCCLK: 200mA Max
PP1V05_S0_PCH_VCCACLKPLL
VCCACLKPLL
31mA Max
VCCCLK
3.3mA Max[1]
HSIO
SPI
OPI
USB3
AZALIA/HDA
VRM/USB2/AZALIA
CORE
GPIO/LCC
THERMAL SENSOR
SERIAL IO
SUS OSCILLATOR
ICC
USB2
PP3V3_S5
VCCSUS3
0.3mA Max[1]
VCCRTC
PPVOUT_S0_PCH_DCPRTC
DCPRTC
VCCSPI
18mA Max
VCCASW
185mA Max[1]
VCC1P05
1499mA Max[1]
DCPSUSBYP
PPVOUT_S5_PCH_DCPSUSBYP_R
Powered in DeepSx
R1399
5.11
1%
1/20W
MF-LF
201
PLACE_NEAR=U1000.AG19:2.54MM
PPVOUT_S5_PCH_DCPSUSBYP
C1399
1UF
10%
6.3V
CERM
402
BYPASS=R1399:U0500:2.54MM
473mA Max[1]
DCPSUS1
VCCTS1_5
3mA Max
1mA Max[1]
VCCSDIO
17mA Max
DCPSUS4
VCCAPLL
WF: RSVD on Sawtooth Peak rev 1.0
213mA Max[1]
teknisi-indonesia

SYNC_MASTER=J41 SYNC_DATE=2014-01-13

PAGE TITLE

CPU/PCH POWER

Apple Inc.

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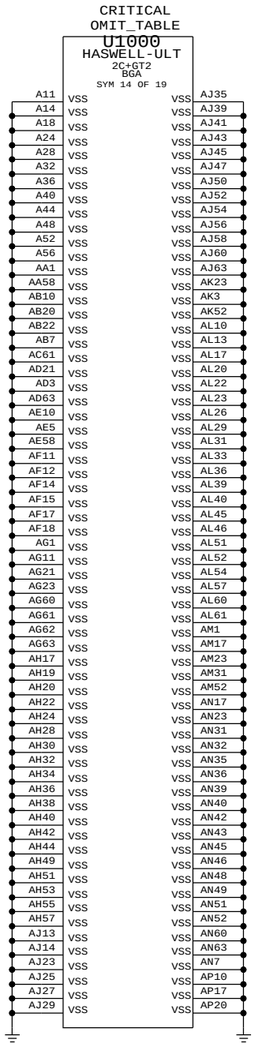

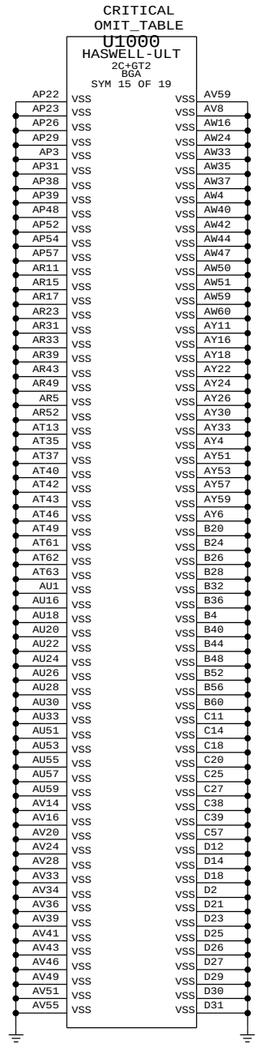

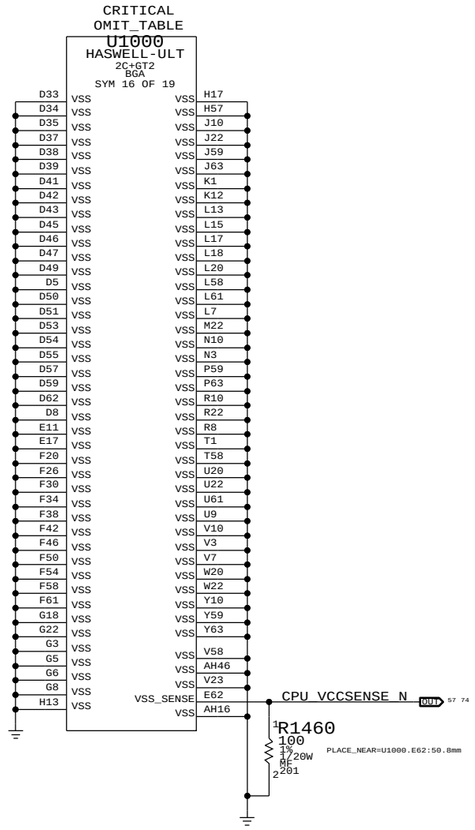

SYNC_MASTER=J41 SYNC_DATE=2014-01-17

PAGE TITLE

CPU/PCH GROUNDS

Apple Inc.

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CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff

78 58 43 9 4 PPVCC_S0_CPU

NOSTUFF CRITICAL C1600 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1601 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1602 10UF 20% 10V X6S 0402
CRITICAL C1603 10UF 20% 10V X6S 0402
CRITICAL C1604 10UF 20% 10V X6S 0402
CRITICAL C1608 10UF 20% 10V X6S 0402
CRITICAL C1609 10UF 20% 10V X6S 0402
CRITICAL C1610 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1611 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1612 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1614 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C165A 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C165B 10UF 20% 10V X6S 0402
CRITICAL C165C 10UF 20% 10V X6S 0402
CRITICAL C165D 10UF 20% 10V X6S 0402
CRITICAL C165E 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C165F 10UF 20% 10V X6S 0402

CRITICAL C1618 10UF 20% 10V X6S 0402
CRITICAL C1619 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1620 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1621 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1630 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C164E 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C164F 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C166D 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C166E 10UF 20% 10V X6S 0402

NOSTUFF CRITICAL C1670 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1672 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1673 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1674 10UF 20% 10V X6S 0402
CRITICAL C1675 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1677 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1681 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1682 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1683 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1684 10UF 20% 10V X6S 0402

NOSTUFF CRITICAL C1685 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1686 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1687 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1688 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1689 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1690 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1691 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1692 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1693 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1694 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1695 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1696 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1697 10UF 20% 10V X6S 0402

NOSTUFF CRITICAL C1622 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1623 10UF 20% 10V X6S 0402
CRITICAL C1624 10UF 20% 10V X6S 0402
CRITICAL C1625 10UF 20% 10V X6S 0402
CRITICAL C1626 10UF 20% 10V X6S 0402
CRITICAL C1627 10UF 20% 10V X6S 0402
CRITICAL C1628 10UF 20% 10V X6S 0402
CRITICAL C1629 10UF 20% 10V X6S 0402
CRITICAL C1632 10UF 20% 10V X6S 0402
CRITICAL C1633 10UF 20% 10V X6S 0402
CRITICAL C1634 10UF 20% 10V X6S 0402
CRITICAL C1635 10UF 20% 10V X6S 0402
CRITICAL C1636 10UF 20% 10V X6S 0402
CRITICAL C1637 10UF 20% 10V X6S 0402
CRITICAL C1638 10UF 20% 10V X6S 0402

CRITICAL C1639 10UF 20% 10V X6S 0402
CRITICAL C1644 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1645 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1646 10UF 20% 10V X6S 0402
CRITICAL C1647 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1648 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1649 10UF 20% 10V X6S 0402

NOSTUFF CRITICAL C1656 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1657 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1658 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1659 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1662 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1663 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1664 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1665 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1666 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1667 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1668 10UF 20% 10V X6S 0402
CRITICAL C1669 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1698 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C1699 10UF 20% 10V X6S 0402
CRITICAL C169A 10UF 20% 10V X6S 0402

CRITICAL C169B 10UF 20% 10V X6S 0402
CRITICAL C169C 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C169D 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C169E 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C169F 10UF 20% 10V X6S 0402
CRITICAL C168A 10UF 20% 10V X6S 0402
CRITICAL C168B 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C168C 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C168D 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C168E 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C168F 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C167A 10UF 20% 10V X6S 0402
NOSTUFF CRITICAL C167B 10UF 20% 10V X6S 0402

CRITICAL C1631 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603

78 63 53 43 26 25 24 23 22 9 4 PP1V2_S3_MEM

CRITICAL C1640 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1642 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1643 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1650 10UF 20% 6.3V X6S 0402
CRITICAL C1651 10UF 20% 6.3V X6S 0402
NOSTUFF CRITICAL C164A 10UF 20% 6.3V X6S 0402
CRITICAL C1654 10UF 20% 6.3V X6S 0402
CRITICAL C1655 10UF 20% 6.3V X6S 0402
NOSTUFF CRITICAL C166A 10UF 20% 6.3V X6S 0402
NOSTUFF CRITICAL C164D 10UF 20% 6.3V X6S 0402
CRITICAL C1653 10UF 20% 6.3V X6S 0402
NOSTUFF CRITICAL C164C 10UF 20% 6.3V X6S 0402

CRITICAL C1641 2.2UF 20% 10V X6S-CERM 0402

NOSTUFF CRITICAL C166B 10UF 20% 6.3V X6S 0402
NOSTUFF CRITICAL C164B 10UF 20% 6.3V X6S 0402
CRITICAL C1652 10UF 20% 6.3V X6S 0402
NOSTUFF CRITICAL C166C 10UF 20% 6.3V X6S 0402

CRITICAL C1660 270UF-0.006OHM 20% 2V TANT CASE-D2

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-20

PAGE TITLE: CPU Decoupling

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NOSTUFF C1800 1UF 10% 6.3V CERM 402
BYPASS=U1000.AH10::6.35MM

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_S5
NOSTUFF C1802 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U1000.Y8::6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_S5
CRITICAL C1804 22UF 20% 6.3V X5R-CERM2 0603
BYPASS=U1000.AC9::12.7MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_S5
C1806 1UF 10% 6.3V CERM 402
BYPASS=U1000.AH11::6.35MM

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1808 1UF 10% 6.3V CERM 402
BYPASS=U1000.U8::6.35MM

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0
C1810 1UF 10% 6.3V CERM 402
BYPASS=U1000.AH14::6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
CRITICAL C1812 22UF 20% 6.3V X5R-CERM2 0603
BYPASS=U1000.V8::12.7MM

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1814 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U1000.K14::6.35MM

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NOSTUFF C1850 22UF 20% 6.3V X5R-CERM2 0603
C1851 1UF 10% 6.3V CERM 402
BYPASS=U1000.AE9::12.7MM
BYPASS=U1000.AE9::6.35MM

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1855 10UF 20% 6.3V X5R 603
C1856 1UF 10% 6.3V CERM 402
C1857 1UF 10% 6.3V CERM 402
BYPASS=U1000.J11::12.7MM
BYPASS=U1000.J11::6.35MM
BYPASS=U1000.AE8::6.35MM

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0
C1860 1UF 10% 6.3V CERM 402
C1861 1UF 10% 6.3V CERM 402
CRITICAL C1862 10UF 20% 6.3V CERM-X5R 0402-2
BYPASS=U1000.K9::6.35MM
BYPASS=U1000.L10::6.35MM
BYPASS=U1000.M9::6.35MM

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1864 1UF 10% 6.3V CERM 402
BYPASS=U1000.AG16::6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1866 1UF 10% 6.3V CERM 402
C1867 1UF 10% 6.3V CERM 402
BYPASS=U1000.J17::6.35MM
BYPASS=U1000.R21::6.35MM

PP1V05_S0
??mA Max
R1870 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
CRITICAL L1870 2.2UH-240MA-0.221OHM 0603
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max
CRITICAL C1870 47UF 20% 4V CERM-X5R 0805-1
CRITICAL C1871 47UF 20% 4V CERM-X5R 0805-1
C1872 1UF 10% 10V X5R 402-1
BYPASS=U1000.A20::12.7MM
BYPASS=U1000.A20::12.7MM
BYPASS=U1000.A20::6.35MM

R1875 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
CRITICAL L1875 2.2UH-240MA-0.221OHM 0603
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
CRITICAL C1875 47UF 20% 4V CERM-X5R 0805-1
CRITICAL C1876 47UF 20% 4V CERM-X5R 0805-1
C1877 1UF 10% 10V X5R 402-1
BYPASS=U1000.J18::12.7MM
BYPASS=U1000.J18::12.7MM
BYPASS=U1000.J18::6.35MM

R1880 0 5% 1/16W MF-LF 402
CRITICAL NOSTUFF L1880 2.2UH-240MA-0.221OHM 0603
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max
CRITICAL NOSTUFF C1880 47UF 20% 4V CERM-X5R 0805-1
CRITICAL NOSTUFF C1881 47UF 20% 4V CERM-X5R 0805-1
C1882 1UF 10% 10V X5R 402-1
BYPASS=U1000.AA21::12.7MM
BYPASS=U1000.AA21::12.7MM
BYPASS=U1000.AA21::6.35MM

PP1V05_S0
83mA Max
CRITICAL L1890 2.2UH-240MA-0.221OHM 0603
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max
CRITICAL C1890 47UF 20% 4V CERM-X5R 0805-1
CRITICAL NOSTUFF C1891 47UF 20% 4V CERM-X5R 0805-1
C1892 1UF 10% 10V X5R 402-1
BYPASS=U1000.B11::12.7MM
BYPASS=U1000.B11::12.7MM
BYPASS=U1000.B11::6.35MM

CRITICAL L1895 2.2UH-240MA-0.221OHM 0603
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max
CRITICAL C1895 47UF 20% 4V CERM-X5R 0805-1
CRITICAL NOSTUFF C1896 47UF 20% 4V CERM-X5R 0805-1
C1897 1UF 10% 10V X5R 402-1
BYPASS=U1000.B18::12.7MM
BYPASS=U1000.B18::12.7MM
BYPASS=U1000.B18::6.35MM

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J41 SYNC_DATE=2014-01-17
PAGE TITLE: PCH Decoupling
Apple Inc.
DRAWING NUMBER: 051-1907
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REVISION: 4.0.0
BRANCH:
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PCIECLKRQ SIGNALS MUST MATCH PCIE PORT ASSIGNEMENTS!
CLKRQ0 IS FOR PCIE PORT 1, CLKRQ1 FOR PORT 2, ETC.

CLOCK FOR PCIE
BUS ANALYZER.

PCIe Port assignments:

SATA Port assignments:

PRIMARY HDD

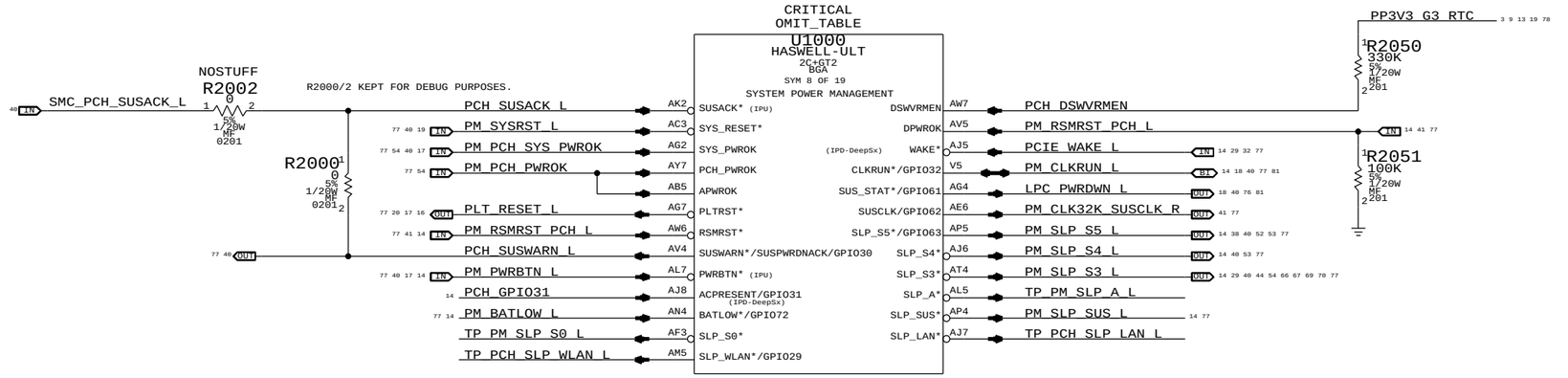
(SPARE SATA)

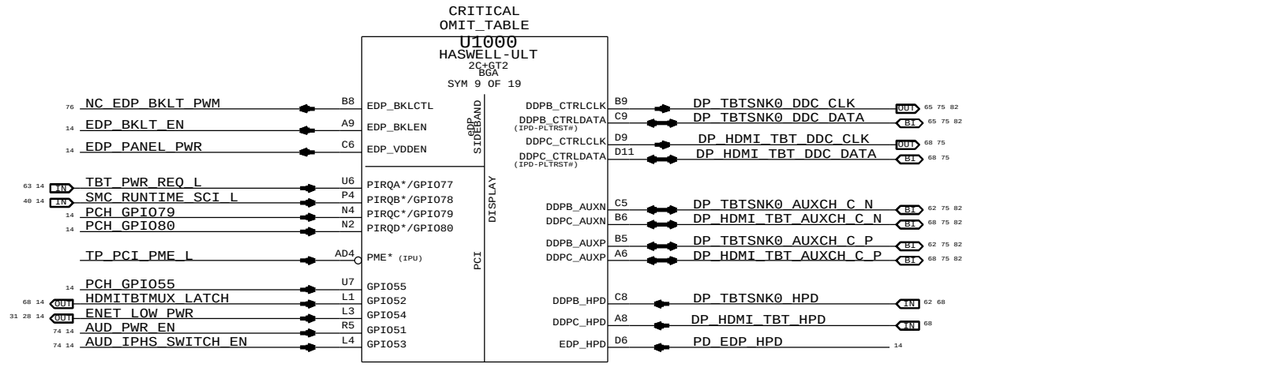
SSD Lane 1

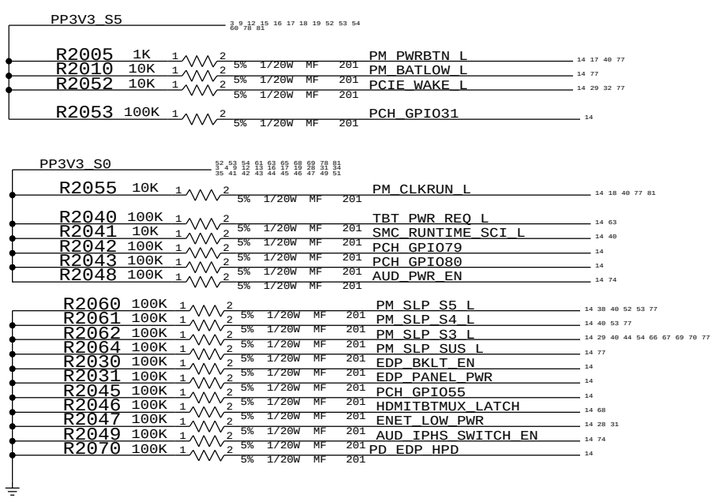
SSD Lane 0

NOT USED PER DEBUG PORT DESIGN GUIDE.

SYNC_MASTER=J41	SYNC_DATE=2014-01-17
PAGE TITLE	PCH Audio/JTAG/SATA/CLK
Apple Inc.	DRAWING NUMBER 051-1907 · SIZE D · REVISION 4.0.0 · BRANCH · PAGE 19 OF 500 · SHEET 13 OF 83







SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-16
PAGE TITLE	PCH PM/PCI/GFX
Apple Inc.	DRAWING NUMBER 051-1907 · SIZE D
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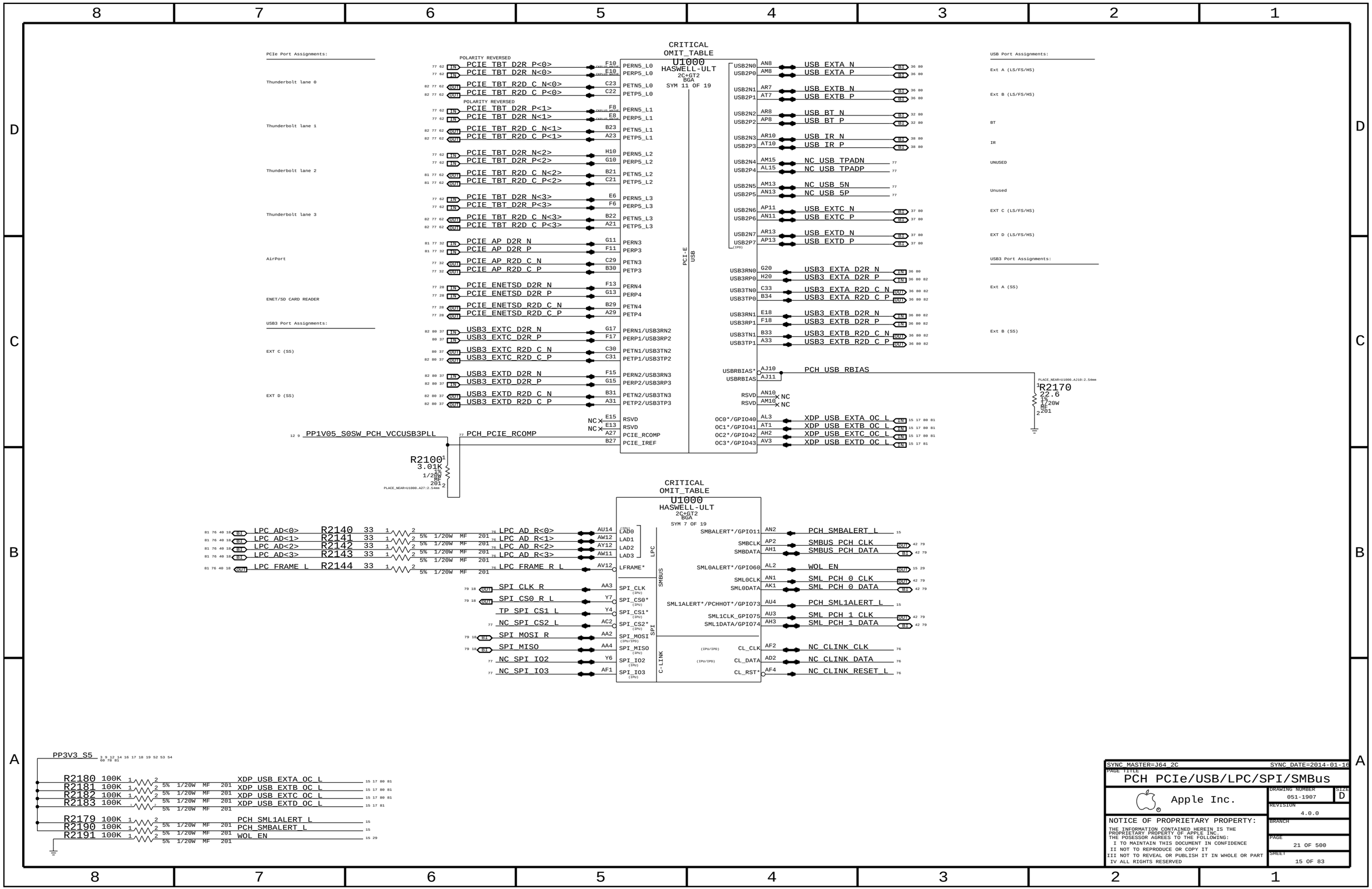
PCIe Port Assignments:
Thunderbolt lane 0
Thunderbolt lane 1
Thunderbolt lane 2
Thunderbolt lane 3
AirPort
ENET/SD CARD READER
USB3 Port Assignments:
EXT C (SS)
EXT D (SS)
POLARITY REVERSED
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_ENETSD_D2R_N
PCIE_ENETSD_D2R_P
PCIE_ENETSD_R2D_C_N
PCIE_ENETSD_R2D_C_P
USB3_EXTC_D2R_N
USB3_EXTC_D2R_P
USB3_EXTC_R2D_C_N
USB3_EXTC_R2D_C_P
USB3_EXTD_D2R_N
USB3_EXTD_D2R_P
USB3_EXTD_R2D_C_N
USB3_EXTD_R2D_C_P
CRITICAL
OMIT_TABLE
U1000
HASWELL-ULT
2C+GT2
BGA
SYM 11 OF 19
PCI-E
USB
PERN5_L0
PERP5_L0
PETN5_L0
PETP5_L0
PERN5_L1
PERP5_L1
PETN5_L1
PETP5_L1
PERN5_L2
PERP5_L2
PETN5_L2
PETP5_L2
PERN5_L3
PERP5_L3
PETN5_L3
PETP5_L3
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN1/USB3RN2
PERP1/USB3RP2
PETN1/USB3TN2
PETP1/USB3TP2
PERN2/USB3RN3
PERP2/USB3RP3
PETN2/USB3TN3
PETP2/USB3TP3
RSVD
RSVD
PCIE_RCOMP
PCIE_IREF
USB2N0
USB2P0
USB2N1
USB2P1
USB2N2
USB2P2
USB2N3
USB2P3
USB2N4
USB2P4
USB2N5
USB2P5
USB2N6
USB2P6
USB2N7
USB2P7
USB_EXTA_N
USB_EXTA_P
USB_EXTB_N
USB_EXTB_P
USB_BT_N
USB_BT_P
USB_IR_N
USB_IR_P
NC_USB_TPADN
NC_USB_TPADP
NC_USB_5N
NC_USB_5P
USB_EXTC_N
USB_EXTC_P
USB_EXTD_N
USB_EXTD_P
USB3RN0
USB3RP0
USB3TN0
USB3TP0
USB3RN1
USB3RP1
USB3TN1
USB3TP1
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
USB3_EXTB_D2R_N
USB3_EXTB_D2R_P
USB3_EXTB_R2D_C_N
USB3_EXTB_R2D_C_P
USBRBIAS*
USBRBIAS
PCH_USB_RBIAS
RSVD
RSVD
NC
NC
OC0*/GPIO40
OC1*/GPIO41
OC2*/GPIO42
OC3*/GPIO43
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
R2170
22.6
1%
1/20W
MF
201
PLACE_NEAR=U1000.AJ10:2.54mm
USB Port Assignments:
Ext A (LS/FS/HS)
Ext B (LS/FS/HS)
BT
IR
UNUSED
Unused
EXT C (LS/FS/HS)
EXT D (LS/FS/HS)
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
PP1V05_S0SW_PCH_VCCUSB3PLL
PCH_PCIE_RCOMP
R2100
3.01K
1%
1/20W
MF
201
PLACE_NEAR=U1000.AJ27:2.54mm
CRITICAL
OMIT_TABLE
U1000
HASWELL-ULT
2C+GT2
BGA
SYM 7 OF 19
LPC
SPI
C-LINK
SMBUS
LAD0
LAD1
LAD2
LAD3
LFRAME*
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_CS2*
SPI_MOSI
SPI_MISO
SPI_IO2
SPI_IO3
CL_CLK
CL_DATA
CL_RST*
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO73
SML1CLK_GPIO75
SML1DATA/GPIO74
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
R2140 33
R2141 33
R2142 33
R2143 33
R2144 33
5% 1/20W MF 201
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
NC_SPI_CS2_L
SPI_MOSI_R
SPI_MISO
NC_SPI_IO2
NC_SPI_IO3
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
WOL_EN
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH_SML1ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
NC_CLINK_CLK
NC_CLINK_DATA
NC_CLINK_RESET_L
PP3V3_S5
R2180 100K
R2181 100K
R2182 100K
R2183 100K
R2179 100K
R2190 100K
R2191 100K
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
PCH_SML1ALERT_L
PCH_SMBALERT_L
WOL_EN
SYNC_MASTER=J64_2C
SYNC_DATE=2014-01-16
PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus
Apple Inc.
DRAWING NUMBER
051-1907
SIZE
D
REVISION
4.0.0
BRANCH
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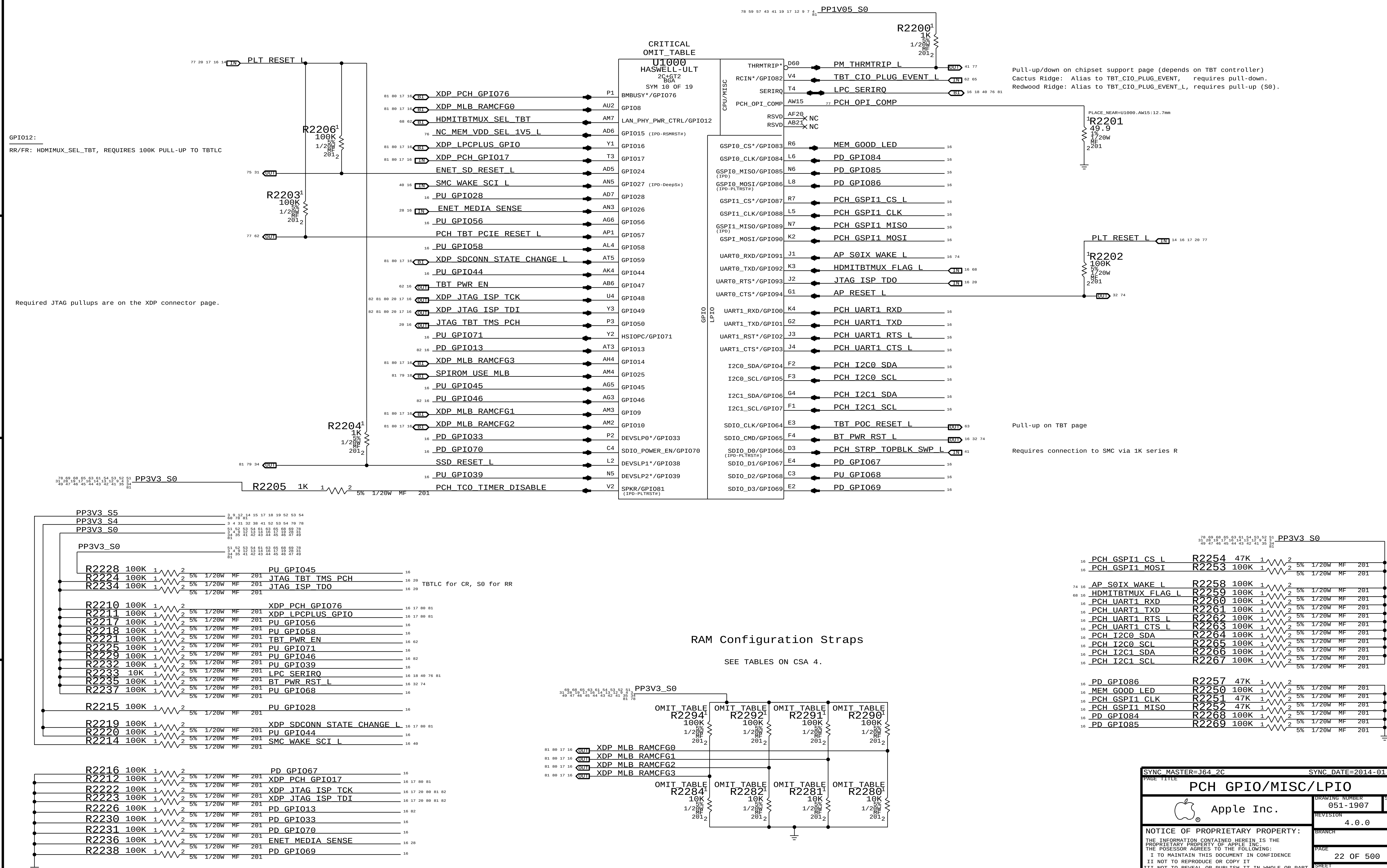

SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-16
PAGE TITLE	PCH GPIO/MISC/LPIO
Apple Inc.	DRAWING NUMBER 051-1907, SIZE D
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Extra BPM Testpoints

XDP_BPM_L<2> → TP2402
XDP_BPM_L<3> → TP2403
XDP_BPM_L<4> → TP2404
XDP_BPM_L<5> → TP2405
XDP_BPM_L<6> → TP2406
XDP_BPM_L<7> → TP2407
(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

R2430 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J2400
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: THIS IS NOT THE STANDARD XDP CONNECTOR.
MIRRORING OF PIN NUMBERS IS CORRECT.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>

XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4 → NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5 → NC
	VCC_OBS_AB	VCC_OBS_CD
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7
SMB_CPU_XDP_SDA	SDA	TDO
SMB_CPU_XDP_SCL	SCL	TRSTn
XDP_PCH_TCK	TCK1	TDI
	TCK0	TMS
		XDP_PRESENT#

NOT USED PER DEBUG PORT DESIGN GUIDE.

CPU_VCCST_PWRGD — R2400 1K 5% 1/20W MF 201 — XDP
PLACE_NEAR=U2772.4:5MM

PM_PWRBTN_L — R2402 0 5% 1/20W MF 0201 — XDP

PM_PCH_SYS_PWROK — R2404 220 5% 1/16W MF-LF 402 — XDP
(REDUCE GLITCH AT HOT-PLUG)

XDP_CPU_TCK

PCH_JTAGX — R2435 0 5% 1/20W MF 0201 — XDP
PLACE_NEAR=J2400.58:28mm

XDP_CPURST_L → R2405 1K 5% 1/20W MF 201 → PLT_RESET_L
PLACE_NEAR=U1000.AG7:5MM

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page
XDP_DBRESET_L

XDP_TRST_L

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

XDP_PRESENT# → XDP_CPU_PRESENT_L

C2404 0.1UF 10% 6.3V CERM-X5R 0201 — XDP
R2431 1K 5% 1/16W MF-LF 402 — XDP
C2400 0.1UF 10% 6.3V CERM-X5R 0201 — XDP
518S0847
C2401 0.1UF 10% 6.3V CERM-X5R 0201 — XDP
C2406 0.1UF 10% 6.3V CERM-X5R 0201 — XDP

CRITICAL XDP Q2440 SSM6N37FEAPE SOT563
XDP_CPU_TDO
PLACE_NEAR=J2400.51:28mm

CRITICAL XDP Q2440 SSM6N37FEAPE SOT563
XDP_CPUPCH_TRST_L
MAKE_BASE=TRUE
XDP_CPU_TRST_L
XDP_PCH_TRST_L
PLACE_NEAR=J2400.53:28mm

CRITICAL XDP Q2442 SSM6N37FEAPE SOT563
XDP_CPU_TDI
PLACE_NEAR=J2400.55:28mm

CRITICAL XDP Q2442 SSM6N37FEAPE SOT563
XDP_CPU_TMS
PLACE_NEAR=J2400.57:28mm

R2410 49.9 1% 1/20W MF 201 — XDP — XDP_CPU_TDO
PLACE_NEAR=U1000.F62:28mm

R2413 49.9 1% 1/20W MF 201 — XDP — XDP_CPU_TCK
PLACE_NEAR=U1000.E60:28mm
1% FOR BOM CONSOLIDATION.

TDI and TMS are terminated in CPU.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD

C2445 0.1UF 10% 6.3V CERM-X5R 0201
U2445 74LVC1G07GF SOT891 (VCC, A, Y, GND, NC, NC, Q)
CRITICAL
R2445 330K 5% 1/20W MF 201

XDP_JTAG_CPU_ISOL_L

teknisi-indonesia

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals

XDP_MLB_RAMCFG0 → TP2470
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
XDP_SDCONN_STATE_CHANGE_L
(MAKE_BASE=TRUE)
XDP_MLB_RAMCFG1 → TP2476
XDP_MLB_RAMCFG2 → TP2477
XDP_MLB_RAMCFG3 → TP2478
(TP-P6)

XDP_JTAG_ISP_TCK

PP3V3_S0

NOSTUFF R2486 10K / R2481 10K — XDP_SSD_PCIE3_SEL_L
NOSTUFF R2487 10K / R2482 10K — XDP_SSD_PCIE2_SEL_L
NOSTUFF R2488 10K / R2483 10K — XDP_SSD_PCIE1_SEL_L
NOSTUFF R2489 10K / R2484 10K — XDP_SSD_PCIE0_SEL_L
(5% 1/20W MF 201)

XDP_LPCPLUS_GPIO → LPCPLUS_GPIO
(MAKE_BASE=TRUE)
XDP_PCH_GPIO17 → TP2486
XDP_PCH_GPIO76 → TP2487
(TP-P6)

XDP_JTAG_ISP_TDI

Non-XDP Signals

USB_EXTA_OC_L
USB_EXTB_OC_L
USB_EXTC_OC_L
USB_EXTD_OC_L
SDCONN_STATE_CHANGE_L

PP1V05_S5_XDP

NOSTUFF R2499 1K 5% 1/20W MF 201 — PCH_JTAGX
PLACE_NEAR=U1000.AE63:28mm

XDP R2490 49.9 1% 1/20W MF 201 — XDP_PCH_TDO
PLACE_NEAR=U1000.AE61:28mm

XDP R2491 49.9 1% 1/20W MF 201 — XDP_PCH_TDI
PLACE_NEAR=U1000.AD61:28mm

XDP R2492 49.9 1% 1/20W MF 201 — XDP_PCH_TMS
PLACE_NEAR=U1000.AD62:28mm

NOSTUFF R2496 49.9 1% 1/20W MF 201 — XDP_PCH_TCK
PLACE_NEAR=U1000.AE62:28mm

NOSTUFF R2497 49.9 1% 1/20W MF 201 — XDP_PCH_TRST_L
PLACE_NEAR=U1000.AU62:28mm
1% FOR BOM CONSOLIDATION.

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16
PAGE TITLE: CPU/PCH Merged XDP
Apple Inc.
DRAWING NUMBER: 051-1907 SIZE: D
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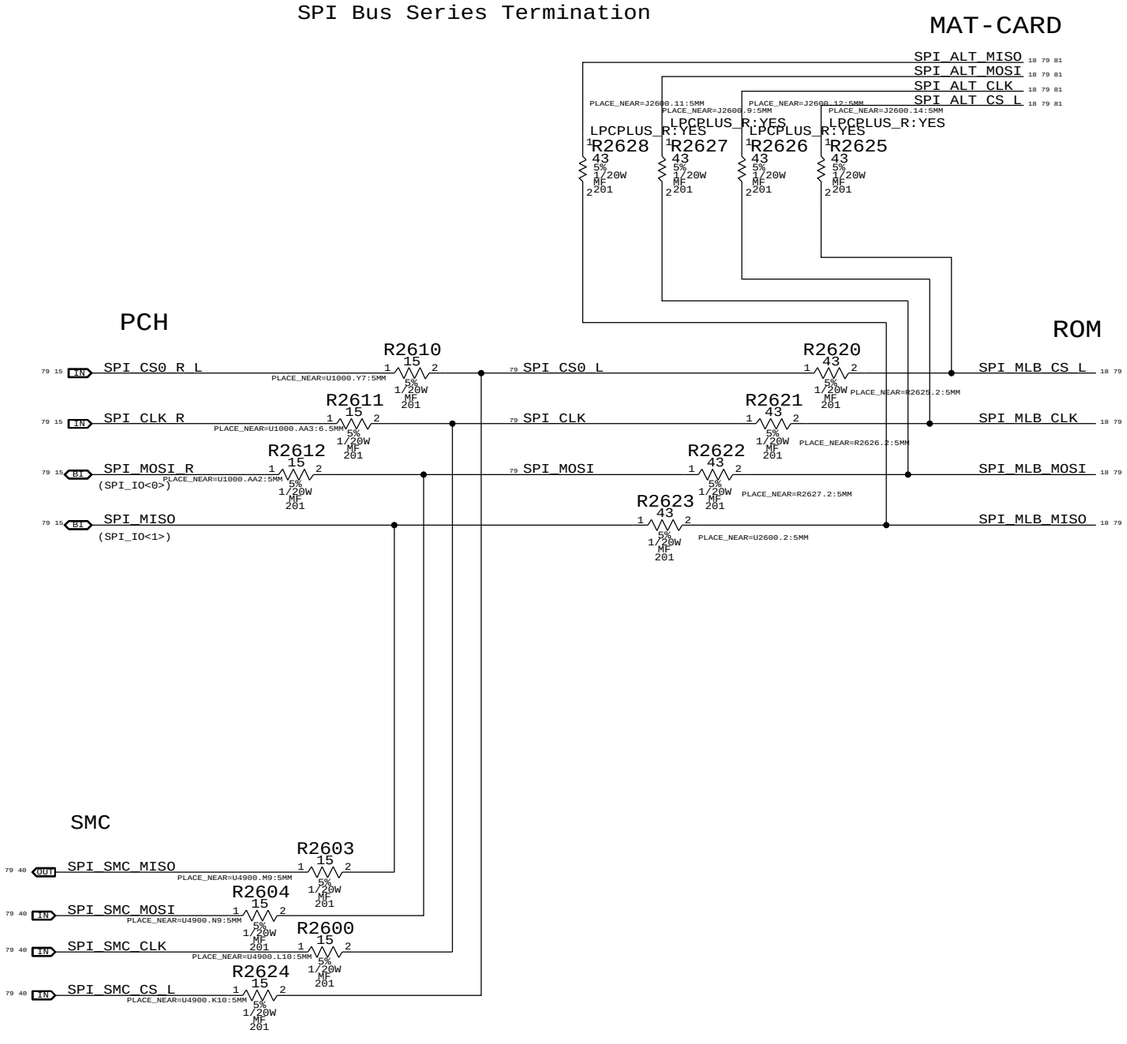
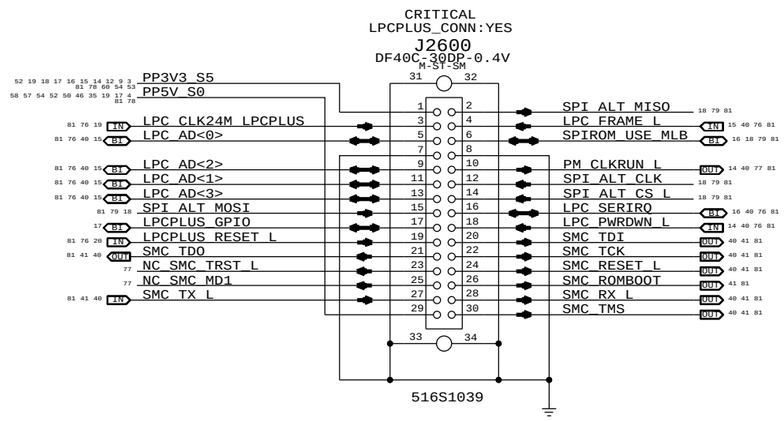
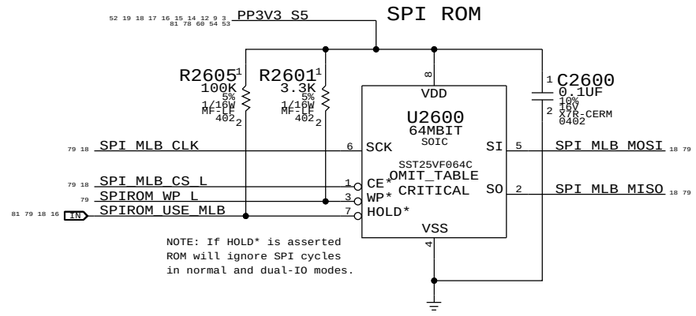
SPI Bus Series Termination



LPC+SPI Connector



SPI ROM



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-17

PAGE TITLE
SPI ROM / LPC+SPI Conn.

Apple Inc.

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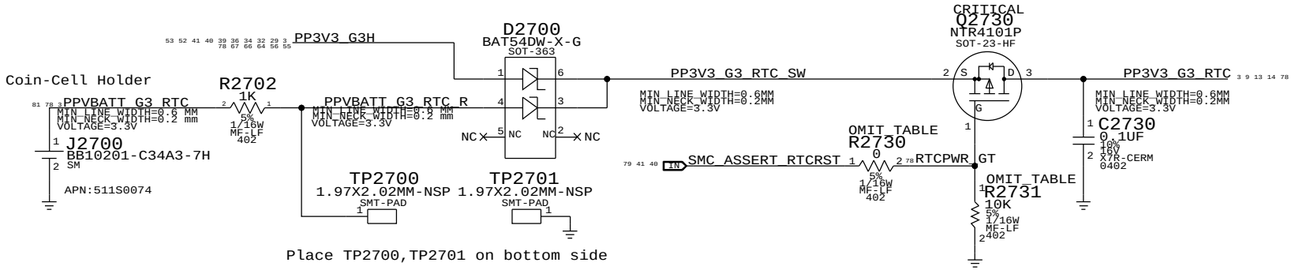
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0062	1	BAT,LI/CF,BR2032,3V,190MAH	BAT	CRITICAL	

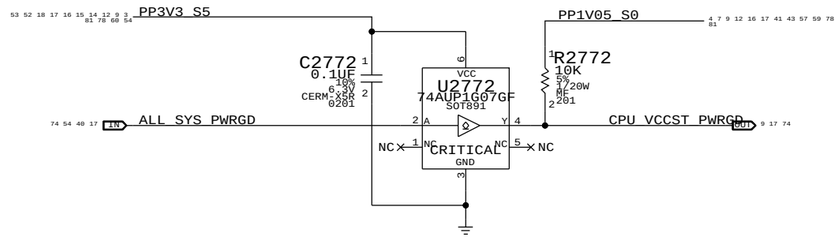
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
742-0080	742-0062	ALT_CMN		ALTERNATE

RTC POWER SOURCES

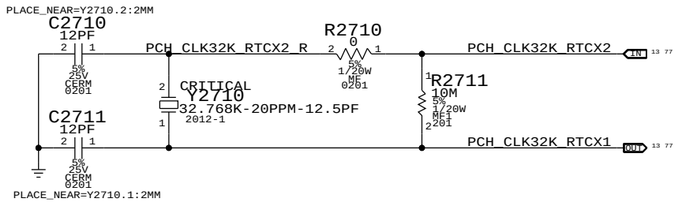


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K OHM,402	R2730	RTCRST:Y
132S0333	1	CAP,0.1 UF,402	R2731	RTCRST:Y
116S0004	1	RES,0 OHM,402	R2730	RTCRST:N
116S0090	1	RES,10K OHM,402	R2731	RTCRST:N

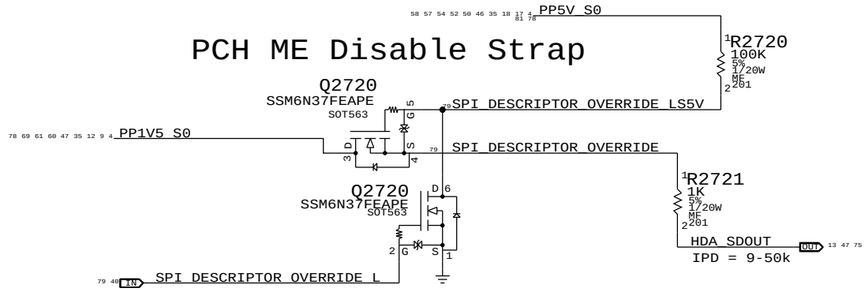
ALL_SYS_PWRGD/CPU_VCCST_PWRGD Level-Shifter



PCH RTC Crystal

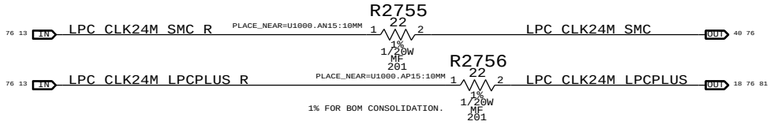


PCH ME Disable Strap

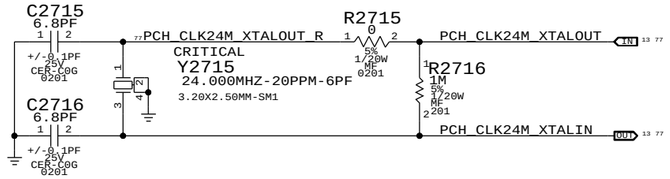


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

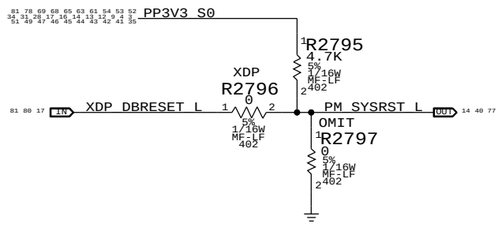
Clock series termination



PCH 24MHz Crystal



PCH Reset Button



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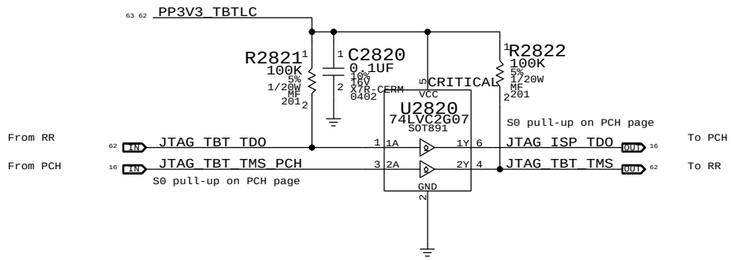
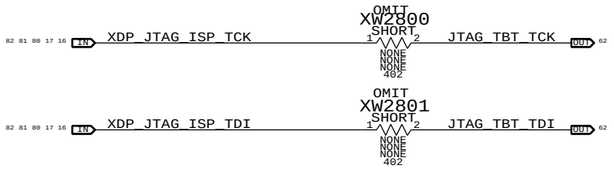
FALCONRIDGE JTAG ISOLATION

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

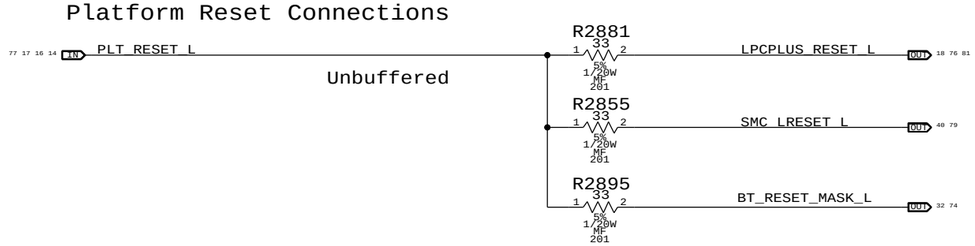


NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.



Platform Reset Connections



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16

PAGE TITLE
Project Chipset Support

Apple Inc.

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Memory Bit/Byte Swizzle

CPU	MAKE_BASE	Memory ICs
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MEM_A_DQ<1>	TRUE	=MEM_A_DQ<12>
MEM_A_DQ<2>	TRUE	=MEM_A_DQ<10>
MEM_A_DQ<3>	TRUE	=MEM_A_DQ<11>
MEM_A_DQ<4>	TRUE	=MEM_A_DQ<13>
MEM_A_DQ<5>	TRUE	=MEM_A_DQ<15>
MEM_A_DQ<6>	TRUE	=MEM_A_DQ<9>
MEM_A_DQ<7>	TRUE	=MEM_A_DQ<14>
MEM_A_DQ<8>	TRUE	=MEM_A_DQ<4>
MEM_A_DQ<9>	TRUE	=MEM_A_DQ<5>
MEM_A_DQ<10>	TRUE	=MEM_A_DQ<7>
MEM_A_DQ<11>	TRUE	=MEM_A_DQ<3>
MEM_A_DQ<12>	TRUE	=MEM_A_DQ<1>
MEM_A_DQ<13>	TRUE	=MEM_A_DQ<6>
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MEM_A_DQ<24>	TRUE	=MEM_A_DQ<18>
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MEM_A_DQ<26>	TRUE	=MEM_A_DQ<17>
MEM_A_DQ<27>	TRUE	=MEM_A_DQ<22>
MEM_A_DQ<28>	TRUE	=MEM_A_DQ<19>
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MEM_A_DQS_P<7>	TRUE	=MEM_A_DQS_P<7>
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CPU	MAKE_BASE	Memory ICs
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MEM_B_DQ<1>	TRUE	=MEM_B_DQ<12>
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Memory EMI Shield Can Pads

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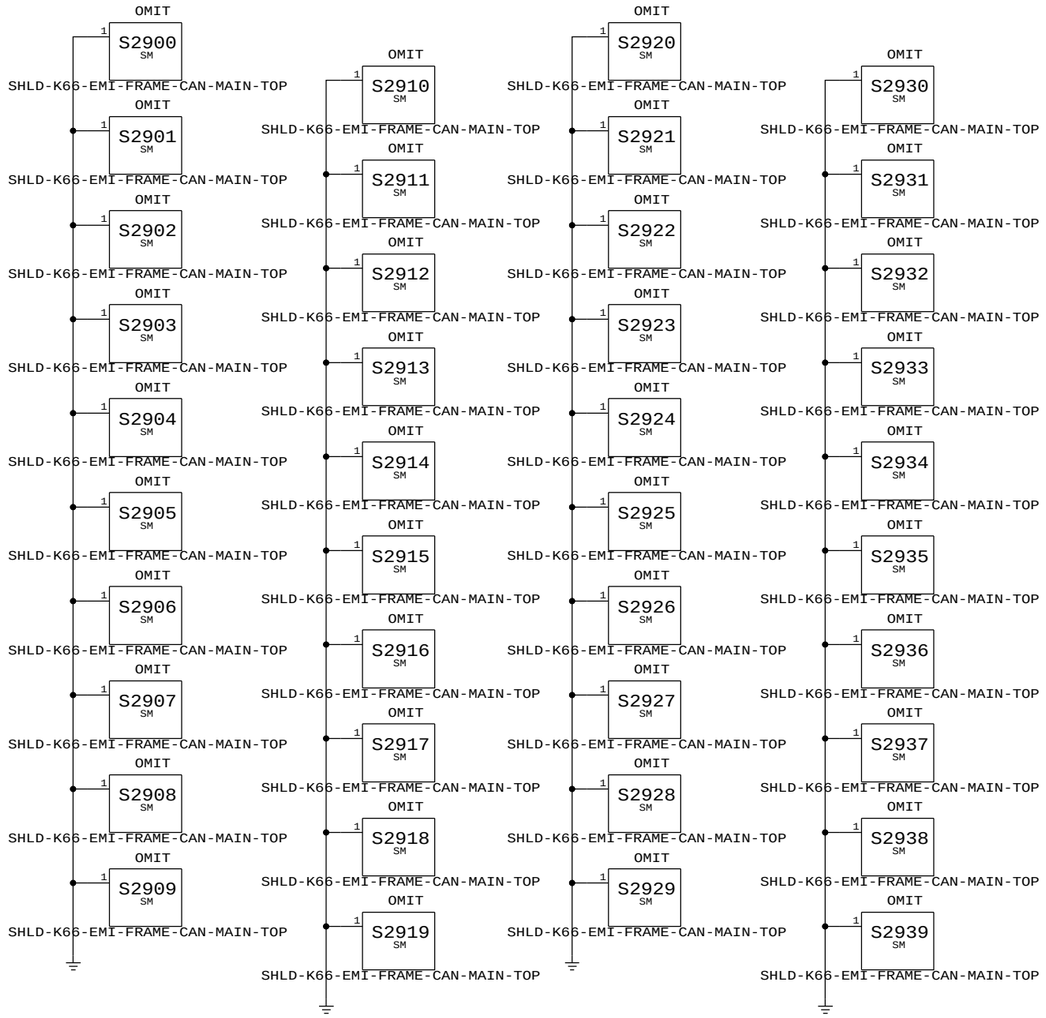
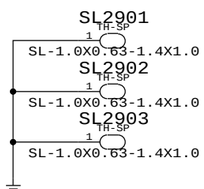


SLOTS FOR SHIELD CAN TABS



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SYNC_MASTER=MASTER SYNC_DATE=2014-01-17

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DDR3 SIGNAL ALIASES, EMI CAN

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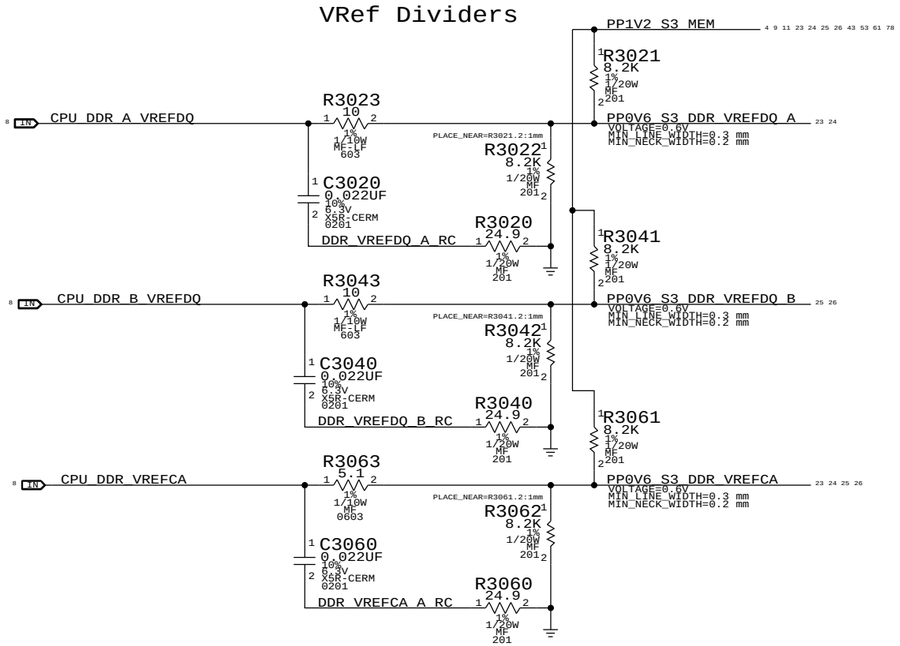

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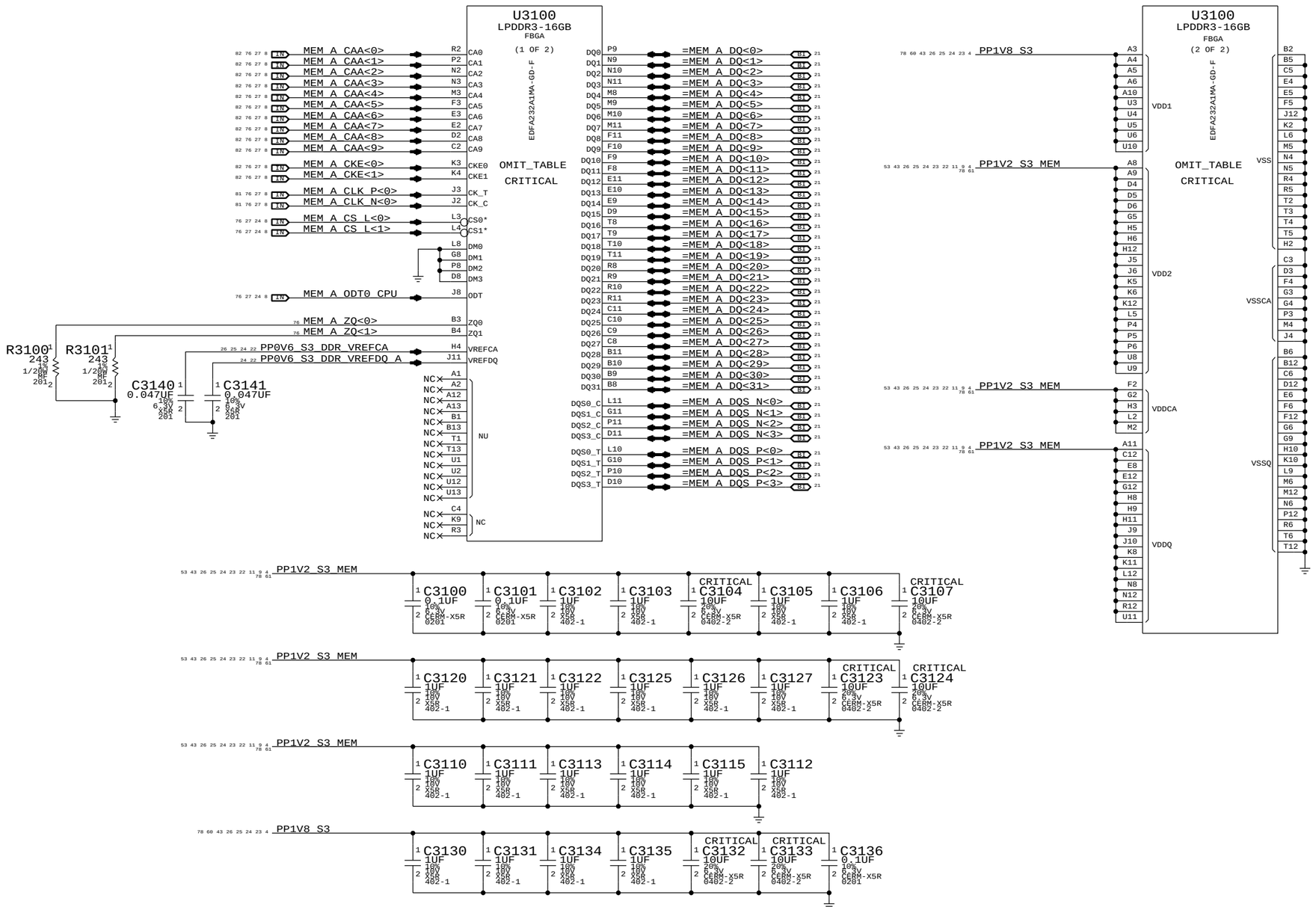
LPDDR3 CHANNEL A (0-31)



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LPDDR3 DRAM Channel A (0-31)

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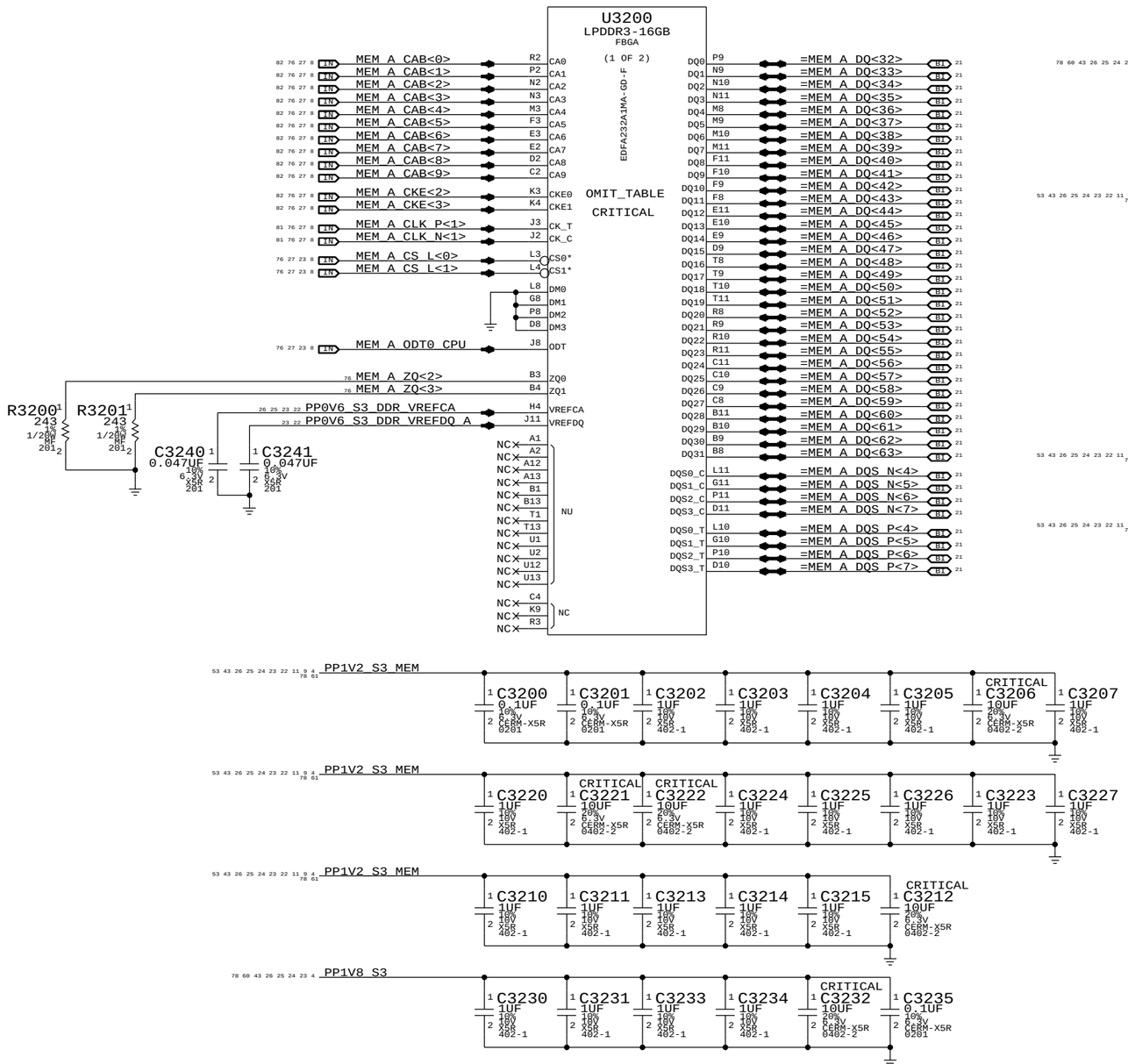
LPDDR3 CHANNEL A (32-63)



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PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

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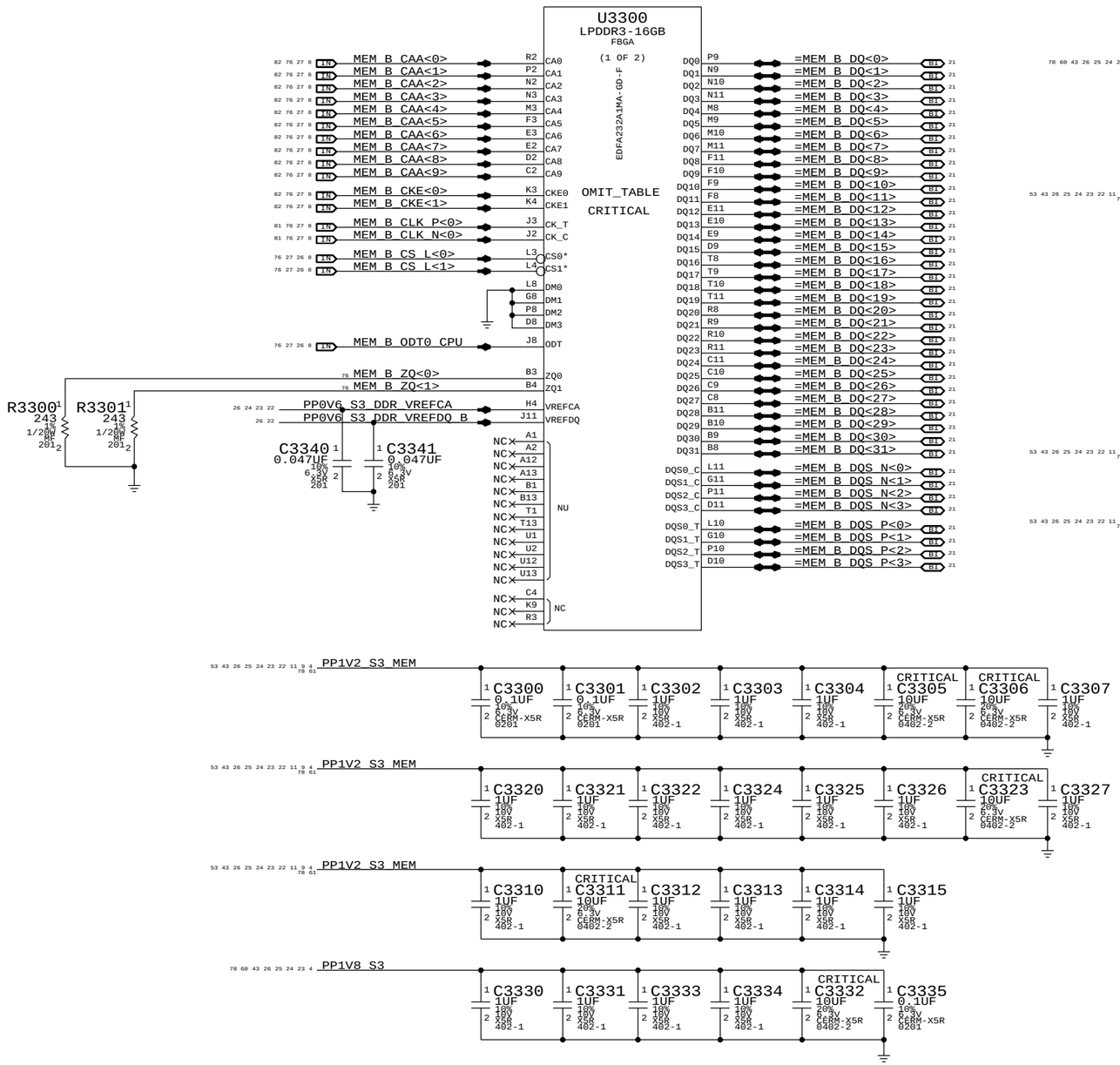
LPDDR3 CHANNEL B (0-31)



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	Apple Inc.
DRAWING NUMBER	051-1907
SIZE	D
REVISION	4.0.0
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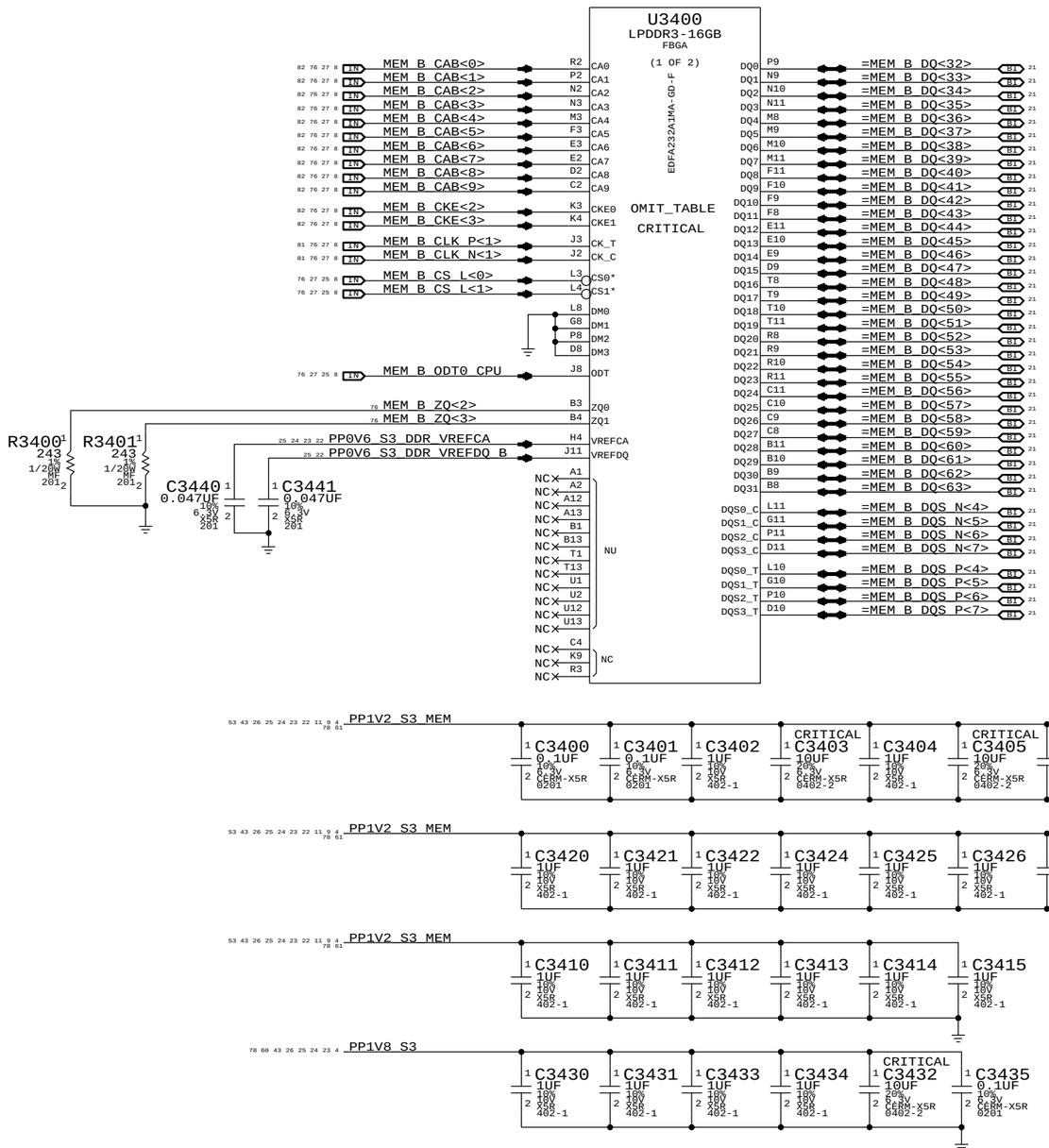
LPDDR3 CHANNEL B (32-63)



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LPDDR3 DRAM Channel B (32-63)

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Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

77 56 27 4 PP0V6_S3_DDRVTT

82 76 23 8	IN	MEM_A_CAA<9>	RP3501	56	4	5	5% 1/32W 4X0201-HF
82 76 23 8	IN	MEM_A_CAA<8>	RP3501	56	3	6	5% 1/32W 4X0201-HF
82 76 23 8	IN	MEM_A_CAA<6>	RP3501	56	2	7	5% 1/32W 4X0201-HF
82 76 23 8	IN	MEM_A_CAA<7>	RP3501	56	1	8	5% 1/32W 4X0201-HF
82 76 23 8	IN	MEM_A_CAA<5>	R3500	56	1	2	5% 1/20W 201 MF
81 76 23 8	IN	MEM_A_CLK_P<0>	R3501	39	1	2	5% 1/20W 201 MF
81 76 23 8	IN	MEM_A_CLK_N<0>	R3502	39	1	2	5% 1/20W 201 MF
82 76 23 8	IN	MEM_A_CKE<1>	R3503	82	1	2	5% 1/20W 201 MF
82 76 23 8	IN	MEM_A_CKE<0>	R3504	82	1	2	5% 1/20W 201 MF
82 76 23 8	IN	MEM_A_CAA<4>	R3505	56	1	2	5% 1/20W 201 MF
82 76 23 8	IN	MEM_A_CAA<3>	R3506	56	1	2	5% 1/20W 201 MF
82 76 23 8	IN	MEM_A_CAA<2>	RP3503	56	4	5	5% 1/32W 4X0201-HF
82 76 23 8	IN	MEM_A_CAA<1>	RP3503	56	3	6	5% 1/32W 4X0201-HF
82 76 23 8	IN	MEM_A_CAA<0>	RP3503	56	2	7	5% 1/32W 4X0201-HF
82 76 24 8	IN	MEM_A_CAB<9>	R3525	56	1	2	5% 1/20W 201 MF
82 76 24 8	IN	MEM_A_CAB<8>	RP3507	56	4	5	5% 1/32W 4X0201-HF
82 76 24 8	IN	MEM_A_CAB<6>	RP3507	56	3	6	5% 1/32W 4X0201-HF
82 76 24 8	IN	MEM_A_CAB<7>	RP3507	56	2	7	5% 1/32W 4X0201-HF
82 76 24 8	IN	MEM_A_CAB<5>	RP3507	56	1	8	5% 1/32W 4X0201-HF
81 76 24 8	IN	MEM_A_CLK_P<1>	R3507	39	1	2	5% 1/20W 201 MF
81 76 24 8	IN	MEM_A_CLK_N<1>	R3508	39	1	2	5% 1/20W 201 MF
82 76 24 8	IN	MEM_A_CKE<2>	R3509	82	1	2	5% 1/20W 201 MF
82 76 24 8	IN	MEM_A_CKE<3>	R3520	82	1	2	5% 1/20W 201 MF
82 76 24 8	IN	MEM_A_CAB<4>	R3521	56	1	2	5% 1/20W 201 MF
82 76 24 8	IN	MEM_A_CAB<2>	RP3504	56	4	5	5% 1/32W 4X0201-HF
82 76 24 8	IN	MEM_A_CAB<3>	RP3504	56	3	6	5% 1/32W 4X0201-HF
82 76 24 8	IN	MEM_A_CAB<1>	RP3504	56	2	7	5% 1/32W 4X0201-HF
82 76 24 8	IN	MEM_A_CAB<0>	RP3504	56	1	8	5% 1/32W 4X0201-HF
76 27 24 23 8	IN	MEM_A_CS_L<0>	R3522	82	1	2	5% 1/20W 201 MF
76 27 24 23 8	IN	MEM_A_CS_L<1>	R3523	82	1	2	5% 1/20W 201 MF
76 27 24 23 8	IN	MEM_A_ODT0_CPU	R3524	82	1	2	5% 1/20W 201 MF

C3500 0.47UF 20% 4V CERM-X5R-1 201
C3501 0.47UF 20% 4V CERM-X5R-1 201
C3502 0.47UF 20% 4V CERM-X5R-1 201
C3503 0.47UF 20% 4V CERM-X5R-1 201
C3504 0.47UF 20% 4V CERM-X5R-1 201
C3505 0.47UF 20% 4V CERM-X5R-1 201
C3506 0.47UF 20% 4V CERM-X5R-1 201
C3507 0.47UF 20% 4V CERM-X5R-1 201
C3508 0.47UF 20% 4V CERM-X5R-1 201
C3509 0.47UF 20% 4V CERM-X5R-1 201

Spare
RP3503
56
NC 1 8 NC
5%
1/32W
4X0201-HF

PLACE_NEAR=RP3504.8:4MM
CRITICAL
C3520 22UF 20% 6.3V X5R-CERM2 0603

EXPLICIT VIAS TO MARK ROUTING T POINT.

V3510 HOLE-VIA-P5RP25
76 27 24 23 8 IN MEM_A_CS_L<0>

V3511 HOLE-VIA-P5RP25
76 27 24 23 8 IN MEM_A_CS_L<1>

V3512 HOLE-VIA-P5RP25
76 27 24 23 8 IN MEM_A_ODT0_CPU

77 56 27 4 PP0V6_S3_DDRVTT

82 76 25 8	IN	MEM_B_CAA<9>	RP3512	56	4	5	5% 1/32W 4X0201-HF
82 76 25 8	IN	MEM_B_CAA<8>	RP3512	56	3	6	5% 1/32W 4X0201-HF
82 76 25 8	IN	MEM_B_CAA<7>	RP3512	56	2	7	5% 1/32W 4X0201-HF
82 76 25 8	IN	MEM_B_CAA<6>	RP3512	56	1	8	5% 1/32W 4X0201-HF
82 76 25 8	IN	MEM_B_CAA<5>	R3510	56	1	2	5% 1/20W 201 MF
81 76 25 8	IN	MEM_B_CLK_P<0>	R3511	39	1	2	5% 1/20W 201 MF
81 76 25 8	IN	MEM_B_CLK_N<0>	R3512	39	1	2	5% 1/20W 201 MF
82 76 25 8	IN	MEM_B_CKE<1>	R3513	82	1	2	5% 1/20W 201 MF
82 76 25 8	IN	MEM_B_CKE<0>	R3514	82	1	2	5% 1/20W 201 MF
82 76 25 8	IN	MEM_B_CAA<4>	R3515	56	1	2	5% 1/20W 201 MF
82 76 25 8	IN	MEM_B_CAA<2>	R3516	56	1	2	5% 1/20W 201 MF
82 76 25 8	IN	MEM_B_CAA<3>	RP3513	56	4	5	5% 1/32W 4X0201-HF
82 76 25 8	IN	MEM_B_CAA<1>	RP3513	56	3	6	5% 1/32W 4X0201-HF
82 76 25 8	IN	MEM_B_CAA<0>	RP3513	56	2	7	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CAB<9>	R3535	56	1	2	5% 1/20W 201 MF
82 76 26 8	IN	MEM_B_CAB<8>	RP3517	56	4	5	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CAB<7>	RP3517	56	3	6	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CAB<6>	RP3517	56	2	7	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CAB<5>	RP3517	56	1	8	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CLK_N<1>	R3517	39	1	2	5% 1/20W 201 MF
81 76 26 8	IN	MEM_B_CLK_P<1>	R3518	39	1	2	5% 1/20W 201 MF
82 76 26 8	IN	MEM_B_CKE<2>	R3519	82	1	2	5% 1/20W 201 MF
82 76 26 8	IN	MEM_B_CKE<3>	R3530	82	1	2	5% 1/20W 201 MF
82 76 26 8	IN	MEM_B_CAB<4>	R3531	56	1	2	5% 1/20W 201 MF
82 76 26 8	IN	MEM_B_CAB<2>	RP3514	56	4	5	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CAB<3>	RP3514	56	3	6	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CAB<1>	RP3514	56	2	7	5% 1/32W 4X0201-HF
82 76 26 8	IN	MEM_B_CAB<0>	RP3514	56	1	8	5% 1/32W 4X0201-HF
76 27 26 25 8	IN	MEM_B_CS_L<0>	R3532	82	1	2	5% 1/20W 201 MF
76 27 26 25 8	IN	MEM_B_CS_L<1>	R3533	82	1	2	5% 1/20W 201 MF
76 27 26 25 8	IN	MEM_B_ODT0_CPU	R3534	82	1	2	5% 1/20W 201 MF

C3510 0.47UF 20% 4V CERM-X5R-1 201
C3511 0.47UF 20% 4V CERM-X5R-1 201
C3512 0.47UF 20% 4V CERM-X5R-1 201
C3513 0.47UF 20% 4V CERM-X5R-1 201
C3514 0.47UF 20% 4V CERM-X5R-1 201
C3515 0.47UF 20% 4V CERM-X5R-1 201
C3516 0.47UF 20% 4V CERM-X5R-1 201
C3517 0.47UF 20% 4V CERM-X5R-1 201
C3518 0.47UF 20% 4V CERM-X5R-1 201
C3519 0.47UF 20% 4V CERM-X5R-1 201

Spare
RP3513
56
NC 1 8 NC
5%
1/32W
4X0201-HF

PLACE_NEAR=RP3507.8:4.5MM
CRITICAL
C3540 22UF 20% 6.3V X5R-CERM2 0603

EXPLICIT VIAS TO MARK ROUTING T POINT.

V3520 HOLE-VIA-P5RP25
76 27 26 25 8 IN MEM_B_CS_L<0>

V3521 HOLE-VIA-P5RP25
76 27 26 25 8 IN MEM_B_CS_L<1>

V3522 HOLE-VIA-P5RP25
76 27 26 25 8 IN MEM_B_ODT0_CPU

SYNC_MASTER=J41_MLB SYNC_DATE=2014-01-17

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D
REVISION 4.0.0
BRANCH
PAGE 35 OF 500
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
IF ENABLED: SR_VDD/SR_VDDP CONNECT TO PP3V3_ENET (ADD BYPASSING), LX CONNECTS TO INDUCTOR.
SPECIAL STAR ROUTING NEEDED ON THESE PINS. DECOUPLING ON PG 40.

78 29 28 3 PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

SEE CAPS ON NEXT PAGE FOR THESE PINS.

VDD for Card Reader I/O
28 PP3V3R1V8_ENET_LR_OUT

ENET_SR_LX 29
ENET_SR_VFB 29 82

PP1V2_ENET 3 29 78
???mA (1000base-T, Caesar V)

CRITICAL L3600 FERR-600-OHM-0.5A SM — PP3V3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V
C3615 4.7UF 20% 6.3V X5R-CERM1 402; C3616 0.1UF 10% 6.3V CERM-X5R 0201; C3600 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL L3605 FERR-600-OHM-0.5A SM — PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V
C3605 0.1UF 10% 6.3V CERM-X5R 0201

C3617 0.1UF 10% 6.3V CERM-X5R 0201; C3618 0.1UF 10% 6.3V CERM-X5R 0201; C3619 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL L3610 FERR-600-OHM-0.5A SM — PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V
R3610 4.7K 5% 1/10W MF-LF 402; C3610 0.1UF 10% 6.3V CERM-X5R 0201; C3611 0.1UF 10% 6.3V CERM-X5R 0201; C3612 0.1UF 10% 6.3V CERM-X5R 0201

R3640 4.7K 5% 1/20W MF 201; R3641 4.7K 5% 1/20W MF 201

C3603 0.01UF 10% 16V X5R-CERM 0201; C3604 0.01UF 10% 16V X5R-CERM 0201

42 AVDDH; 48 37 BIASVDDH; 17 XTALVDDH; 7 20 56 62 VDDO; VDD_CR; 14 SR_VDD; 15 SR_VDDP; 16 SR_LX; 13 SR_VFB; 39 45 51 AVDDL; 29 PCIE_PLLVDDL; 32 36 GPHY_PLLVDDL; 35 61 VDDC

CRITICAL U3600 BCM57766A1KMLKG QFN-8X8

PP1V2_ENET_PHY_AVDDL: C3623 0.1UF 10% 6.3V CERM-X5R 0201; C3622 0.1UF 10% 6.3V CERM-X5R 0201; C3621 0.1UF 10% 6.3V CERM-X5R 0201; CRITICAL L3620 FERR-600-OHM-0.5A; C3620 4.7UF 20% 6.3V X5R-CERM1 402
PP1V2_ENET_PHY_PCIEPLL: C3627 0.1UF 10% 6.3V CERM-X5R 0201; C3626 0.1UF 10% 6.3V CERM-X5R 0201; CRITICAL L3625 FERR-600-OHM-0.5A; C3625 4.7UF 20% 6.3V X5R-CERM1 402
PP1V2_ENET_PHY_GPHYPLL: C3631 0.1UF 10% 6.3V CERM-X5R 0201; CRITICAL L3630 FERR-600-OHM-0.5A; C3630 4.7UF 20% 6.3V X5R-CERM1 402
C3637 0.1UF 10% 6.3V CERM-X5R 0201; C3636 0.1UF 10% 6.3V CERM-X5R 0201; CRITICAL C3635 10UF 20% 6.3V CERM-X5R 0402-2

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3600 pin 20.

81 78 69 68 65 63 61 54 53 52 34 31 19 17 16 14 13 12 9 4 1 51 49 47 46 45 44 43 42 41 35 PP3V3_S0

R3642 1K 5% 1/20W MF 201 Current Limiting Resistor

C3650 0.1UF 10% 6.3V CERM-X5R 0201; C3651 0.1UF 10% 6.3V CERM-X5R 0201; C3655 0.1UF 10% 6.3V CERM-X5R 0201; C3656 0.1UF 10% 6.3V CERM-X5R 0201

77 15 OUT PCIE_ENETSD_D2R_N
77 15 OUT PCIE_ENETSD_D2R_P
77 15 IN PCIE_ENETSD_R2D_C_P
77 15 IN PCIE_ENETSD_R2D_C_N

R3643 0 5% 1/10W MF-LF 402; C3690 0.1UF 10% 6.3V CERM-X5R 0201

75 29 OUT ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

NOSTUFF R3644 10K 5% 1/10W MF-LF 402
78 29 28 3 PP3V3_ENET

ENET_VMAIN_PRSNT — 58 VMAIN_PRSNT (IPO)
77 PCIE_ENETSD_D2R_C_N — 27 PCIE_TXD_N
77 PCIE_ENETSD_D2R_C_P — 28 PCIE_TXD_P
77 PCIE_ENETSD_R2D_P — 33 PCIE_RXD_P
77 PCIE_ENETSD_R2D_N — 34 PCIE_RXD_N
77 13 IN PCIE_CLK100M_ENETSD_P — 31 PCIE_REFCLK_P
77 13 IN PCIE_CLK100M_ENETSD_N — 30 PCIE_REFCLK_N
74 31 IN CIV_ENET_RESET_L — 11 PERST* (IPD)
13 OUT ENETSD_CLKREQ_L — 12 CLKREQ* (OD)
ENET_WAKE_R_L — 3 WAKE* (OD)
31 14 IN ENET_LOW_PWR — 4 LOW_PWR (IPD)
PU_ENET_ASF_SMB_CLK — 6 SMB_CLK
PU_ENET_ASF_SMB_DATA — 10 SMB_DATA (IPD)
75 28 ENET_SCLK — 66 SCLK_SPD1000LED*
75 28 ENET_MISO — 64 SI/EEDATA
75 28 ENET_MOSI — 65 SO_LINKLED*
75 28 ENET_CS_L — 63 CS*/EECLK
PU_ENET_SPD100LED_L — 2 SPD100LED*/SERIAL_DO (OD)
29 OUT ENET_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)
75 29 IN ENET_CLK25M_XTALI — 18 XTALI
75 29 OUT ENET_CLK25M_XTALO — 19 XTALO
ENET_RDAC — 38 RDAC

R3665 1.24K 1% 1/10W MF-LF 402

THRM_PAD 69

TRD0_P 40 ENET_MDI_P<0> BI 30 75
TRD0_N 41 ENET_MDI_N<0> BI 30 75
TRD1_P 44 ENET_MDI_P<1> BI 30 75
TRD1_N 43 ENET_MDI_N<1> BI 30 75
TRD2_P 46 ENET_MDI_P<2> BI 30 75
TRD2_N 47 ENET_MDI_N<2> BI 30 75
TRD3_P 50 ENET_MDI_P<3> BI 30 75
TRD3_N 49 ENET_MDI_N<3> BI 30 75

PP3V3R1V8_ENET_LR_OUT 28 — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V
CRITICAL C3670 4.7UF 20% 6.3V X5R-CERM 402; C3671 0.1UF 10% 6.3V CERM-X5R 0201; C3672 0.1UF 10% 6.3V CERM-X5R 0201

NOSTUFF R3630 3.3K 5% 1/16W MF-LF 402

(IPD) GPIO_0/CR_ACT_LED* 5 — ENET_ASF_GPIO_R
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 — ENET_MEDIA_SENSE — OUT 16
(IPU) SD_DETECT 1 — ENET_CR_DETECT_L — IN 31 75
CR_CMD 26 — 75 ENET_CR_CMD — R3674 33 5% 1/20W MF 201 (PLACE_NEAR=U3500.26:3 MM) — SDCONN_CMD — IN 31 79
CR_CLK 21 — 75 ENET_CR_CLK — R3671 33 5% 1/20W MF 201 (PLACE_NEAR=U3500.21:3 MM) — SDCONN_CLK — OUT 31 79
(IPU) CR_DATA0 25 — 75 ENET_CR_DATA<0> — R3650 33 — SDCONN_DATA<0> — BI 31 79
CR_DATA1 24 — 75 ENET_CR_DATA<1> — R3651 33 — SDCONN_DATA<1> — BI 31 79
CR_DATA2 23 — 75 ENET_CR_DATA<2> — R3652 33 — SDCONN_DATA<2> — BI 31 79
CR_DATA3 22 — 75 ENET_CR_DATA<3> — R3653 33 — SDCONN_DATA<3> — BI 31 79
CR_DATA4 52 — 75 ENET_CR_DATA<4> — R3675 33 — SDCONN_DATA<4> — BI 31 79
CR_DATA5 53 — 75 ENET_CR_DATA<5> — R3676 33 — SDCONN_DATA<5> — BI 31 79
CR_DATA6 54 — 75 ENET_CR_DATA<6> — R3677 33 — SDCONN_DATA<6> — BI 31 79
CR_DATA7 55 — 75 ENET_CR_DATA<7> — R3678 33 — SDCONN_DATA<7> — BI 31 79
(IPU) MS_INS* 59 — NC_ENET_CE_L_MS_INS_L — 76
(IPU) CR_LED*/CR_BUS_PWR 60 — ENET_CR_PWREN — OUT 31 75
CR_WP* 57 — SDCONN_WP — IN 31 79
SR_DISABLE 68 — ENET_SR_DISABLE — R3680 1K 5% 1/20W MF 201

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET 1.2V SR IS ENABLED IF SR_DISABLE is PULLed-DOWN.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET supports both active-levels for WP.

PHY Non-Volatile Memory
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.

78 29 28 3 PP3V3_ENET
C3690 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL U3690 AT45DB021E-SS SOIC
OMIT_TABLE
75 28 ENET_SCLK — SCK
75 28 ENET_CS_L — CS*
WP*
RESET*
VCC
GND
SI — ENET_MOSI 28 75
SO — ENET_MISO 28 75
NOSTUFF R3690 4.7K 5% 1/20W MF 201
NOSTUFF R3697 4.7K 5% 1/20W MF 201

NOTE: PULL-DOWN ON MISO PLUS INTERNAL PULL-UPS ON OTHER 3 SPI PINS CONFIGURES ENET FOR THE NVRAM AUTO-SENSE

SYNC MASTER=J64_2C
SYNC_DATE=2014-01-14
PAGE TITLE
ETHERNET PHY (CAESAR IV+)
Apple Inc.
DRAWING NUMBER 051-1907
SIZE D
REVISION 4.0.0
BRANCH
PAGE 36 OF 500
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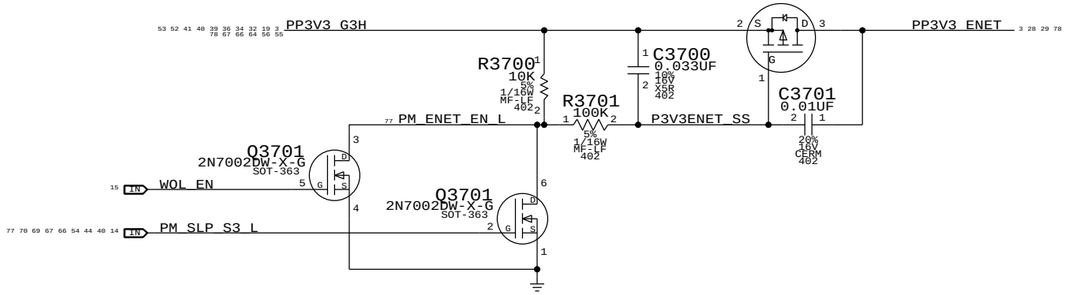
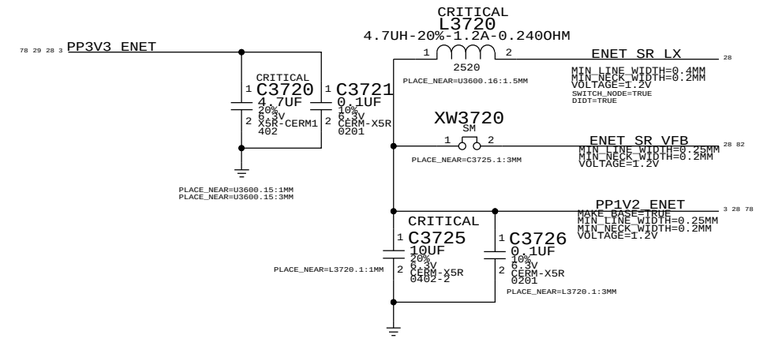
ENET Enable Generation

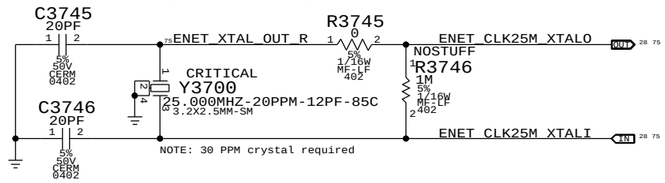


CAESAR IV 1.2V INT.VR CMPTS

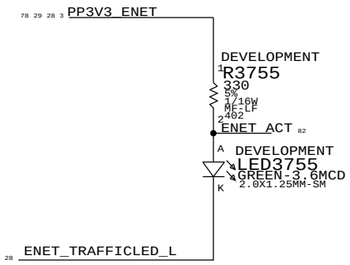


CRYSTAL

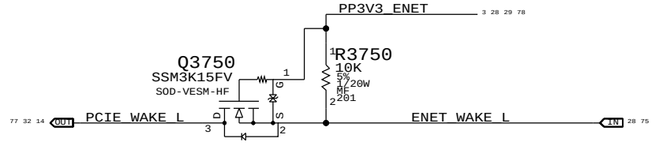
Ethernet 25MHz Clock



CAESAR IV ACTIVITY LED



Ethernet WAKE# Isolation



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-14

PAGE TITLE: ETHERNET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

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PLACE ONE CAP NEAR EACH PINS 3 AND 4 OF T3801 AND T3802

ENET_CONN_CTAP

C3800 0.1UF 10% 16V X7R-CERM 0402
C3801 0.1UF 10% 16V X7R-CERM 0402
C3802 0.1UF 10% 16V X7R-CERM 0402
C3803 0.1UF 10% 16V X7R-CERM 0402

ETHERNET CONNECTOR

ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_N<3>
ENET_MDI_P<3>

CRITICAL
T3801
SM
TX
LFE8904CF
RX

CRITICAL
T3802
SM
TX
LFE8904CF
RX

ENET_MDI_TRAN_N<2>
ENET_MDI_TRAN_P<2>
ENET_CENTER_TAP<1>
ESD_HOT
ENET_CENTER_TAP<3>
ESD_HOT
ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>
ENET_MDI_TRAN_P<0>
ENET_MDI_TRAN_N<0>
ENET_CENTER_TAP<2>
ESD_HOT
ENET_CENTER_TAP<0>
ESD_HOT
ENET_MDI_TRAN_N<3>
ENET_MDI_TRAN_P<3>

TRANSFORMERS SHOULD BE MIRRORED ON OPPOSITE SIDES OF BOARD.

R3800 75 1% 1/16W MF-LF 0402
R3801 75 1% 1/16W MF-LF 0402
R3802 75 1% 1/16W MF-LF 0402
R3803 75 1% 1/16W MF-LF 0402
ENET_CMODE_REF
ESD_HOT

CRITICAL
C3810
1000PF 10% 2KV CERM 1206

CRITICAL
J3800
RJ45-J40
F-R-TH

ESD_HOT
ENET_MDI
TRAN_P0
TRAN_N0
TRAN_P1 *
TRAN_P2
TRAN_N2
TRAN_N1 *
TRAN_P3
TRAN_N3
SHIELD PINS

*SPLIT PAIR

514-0785

REQUIRES 2150VDC ISOLATION!

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE: ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-1907
SIZE: D
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BRANCH:
PAGE: 38 OF 500
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EMI CAPS

PLACE NEXT TO J3900

NOSTUFF C3911 10PF 1 2 SDCONN_CMD_R
NOSTUFF C3912 10PF 1 2 SDCONN_DATA_R<0>
NOSTUFF C3913 10PF 1 2 SDCONN_DATA_R<1>
NOSTUFF C3914 10PF 1 2 SDCONN_DATA_R<2>
NOSTUFF C3915 10PF 1 2 SDCONN_DATA_R<3>
NOSTUFF C3916 10PF 1 2 SDCONN_DATA_R<4>
NOSTUFF C3917 10PF 1 2 SDCONN_DATA_R<5>
NOSTUFF C3918 10PF 1 2 SDCONN_DATA_R<6>
NOSTUFF C3919 10PF 1 2 SDCONN_DATA_R<7>
NOSTUFF C3920 10PF 1 2 SDCONN_WP
NOSTUFF C3921 10PF 1 2 SDCONN_DETECT

(5% 25V CER 0201)

Caesar IV Support

TPS2065-1 HAS ACTIVE LOAD DISCHARGE SO R3905 IS NOSTUFF.

1.0A LIMIT

U3900 TPS2065-1 (DGN)
IN0, IN1, EN, GND, PAD, THRM PAD, OUT0, OUT1, OUT2, OC*

PP3V3_S0 → CRITICAL C3901 10UF 20% 6.3V CERM X5R 0402-2; C3900 0.1UF 10% 10V CERM 0402; R3902 10K 5% 1/16W MF-LF 402
ENET_CR_PWREN
PU_SDCONN_OC_L
CRITICAL C3907 10UF 20% 6.3V CERM X5R 0402-2; C3905 0.1UF 10% 10V CERM 0402
MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3V MAKE_BASE=TRUE
PP3V3_SW_SD_PWR
NOSTUFF R3905 39.2K 1% 1/16W MF-LF 402

PLACE AT CONNECTOR.

L3951 43NH-5%-100MA-0.81OHM 0402
SDCONN_CLK (IN)
NOSTUFF C3951 15PF 5% 50V C0G 0201
NOSTUFF C3950 22PF 5% 25V C0G 0201

(ALSO SEE ESD CAPS AT LEFT)

SDCONN_CMD	R3955	0	5%	1/20W	MF	0201
SDCONN_DATA<0>	R3960	0	5%	1/20W	MF	0201
SDCONN_DATA<1>	R3961	0	5%	1/20W	MF	0201
SDCONN_DATA<2>	R3962	0	5%	1/20W	MF	0201
SDCONN_DATA<3>	R3963	0	5%	1/20W	MF	0201
SDCONN_DATA<4>	R3964	0	5%	1/20W	MF	0201
SDCONN_DATA<5>	R3965	0	5%	1/20W	MF	0201
SDCONN_DATA<6>	R3966	0	5%	1/20W	MF	0201
SDCONN_DATA<7>	R3967	0	5%	1/20W	MF	0201

SDCONN_CLK_R
SDCONN_CMD_R
SDCONN_DATA_R<0>
SDCONN_DATA_R<1>
SDCONN_DATA_R<2>
SDCONN_DATA_R<3>
SDCONN_DATA_R<4>
SDCONN_DATA_R<5>
SDCONN_DATA_R<6>
SDCONN_DATA_R<7>
SDCONN_DETECT
SDCONN_WP (OUT)

CRITICAL J3900 SD-CARD-K40-K41 F-RT-TH

3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW (NC SWITCH)
15	CARD_DETECT_GND (OPEN = CARD INSERTED)
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

516-0230

SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.

PP3V3_S4
R3915 10K 5% 1/16W MF-LF 402
CRITICAL C3930 1UF 10% 10V X5R 402-1

U3930 SLG4AP026V TDFN
VDD, LOW_PWR, RST_IN* (450mV hyst), DET_IN (IPU), DET_LVL, GND, RST_OUT*, DET_CH_EN*, DET_CHNGD* (OD), DET_OUT (OD), RST LOGIC, DLY, THRM PAD

When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regradless of RST_IN# state. Otherwise RST_OUT# follows RST_IN#

ENET_SD_RESET_L (IN) → FROM PCH GPIO
R3911 0 5% 1/16W MF-LF 402
NOSTUFF R3910 10K 5% 1/16W MF-LF 402
ENET_LOW_PWR (IN)
SLG_ENET_RESET_L
SDCONN_DETECT FROM SD CONN ->
SDCONN_DETECT_LVL
SD_DETECT NEEDS TO BE INVERTED.
SLG_ENET_RESET_R_L
R3914 0 5% 1/16W MF-LF 402
CIV_ENET_RESET_L (OUT)
SDCONN_STATE_CHANGE_L_S1R
R3931 0 5% 1/16W MF-LF 402
SDCONN_STATE_CHANGE_L (OUT) → TO PCH GPIO
ENET_CR_DETECT_L (OUT) → TO ENET CHIP
NOSTUFF R3912 0 5% 1/16W MF-LF 402

DLY block is 20ms nominal

SYNC_MASTER	J64 2C
SYNC_DATE	2014-01-16
PAGE TITLE	SD CARD READER
DRAWING NUMBER	051-1907
SIZE	D
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BRANCH	
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Apple Inc.

AIRPORT

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN")

NOTE: S4 TERM IS GUARANTEED BY S4 PULL-UP ON OPEN-DRAIN AP_PWR_EN SIGNAL.

Supervisor & CLKREQ# Isolation

BLUETOOTH

WAKE DETECT FOR G3STANDBY

P3V3_BT_EN = PM_SLP_G3S_EN & (BT_PWRRST_L & BT_PWRRST_EN | BT_PWRRST_EN#)

SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-15
PAGE TITLE: WIRELESS,BT CONNECTOR	
Apple Inc.	DRAWING NUMBER 051-1907 D
	REVISION 4.0.0
	BRANCH
	PAGE 41 OF 500
	SHEET 32 OF 83

ANTENNA CABLE ROUTING

ZT4220
4.0OD1.55H-M1.6X0.35-ST

ZT4221
4.0OD1.55H-M1.6X0.35-ST

ZT4222
4.0OD1.55H-M1.6X0.35-ST

860-1438

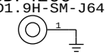
ZT4230
4.0OD2.81H-M1.6X0.35-ST

ZT4231
4.0OD2.81H-M1.6X0.35-ST

860-00023

STANDOFFS FOR X28 CARD

SDF4200
4.5OD1.9H-SM-J64



860-00086

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-15

PAGE TITLE
WIRELESS MECHANICAL

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

BRANCH

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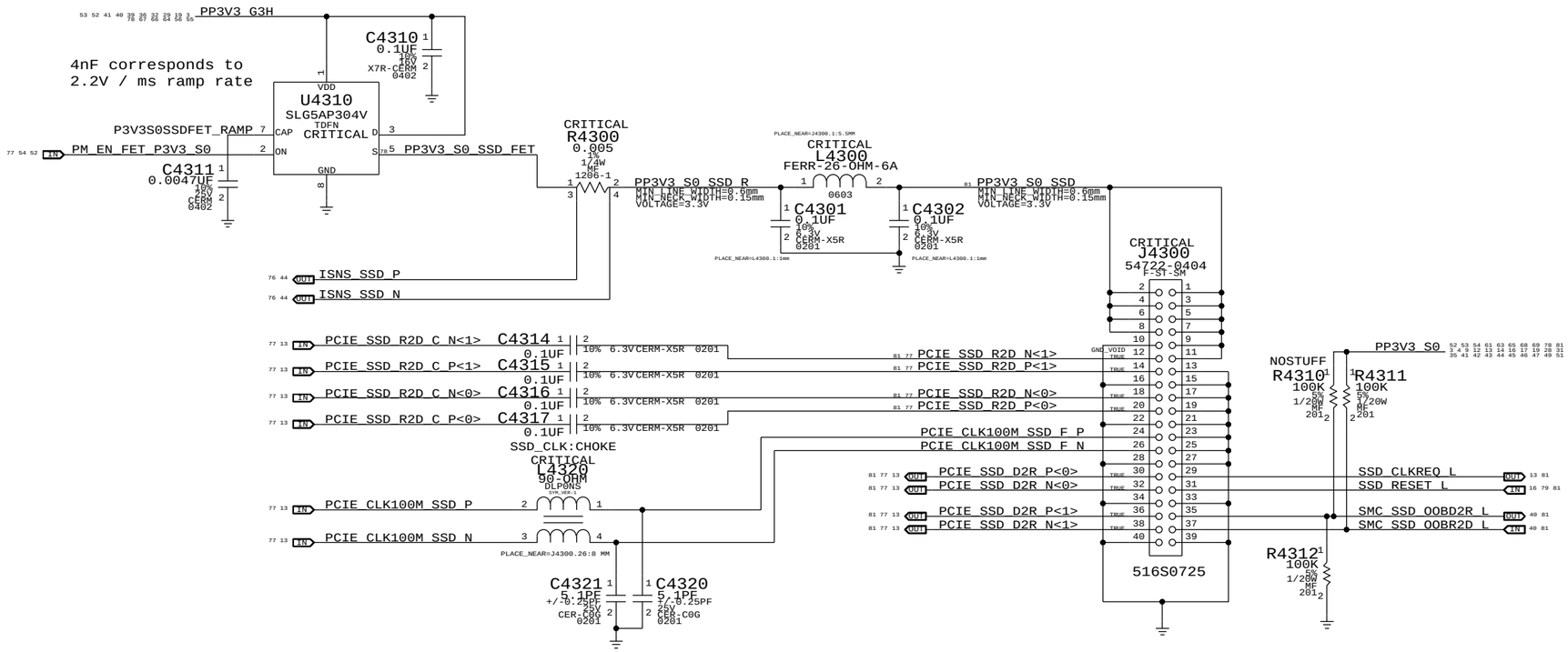

BYPASS CHOKE WITH 2X ZERO-OHM RESISTERS.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	2	RES,0.0,5,1A,0201,BLACK	L4320A,L4320B		SSD_CLK:NO_CHOKE

SYNC MASTER=J64_2C SYNC DATE=2014-01-17

PAGE TITLE

SSD Connector

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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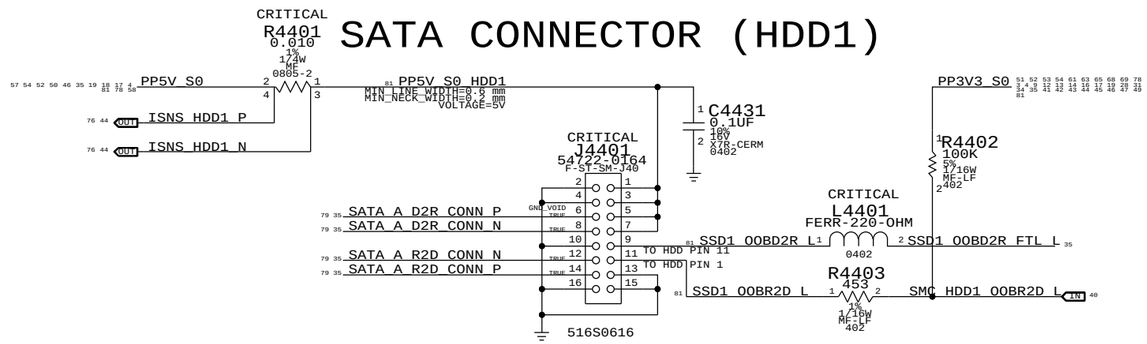
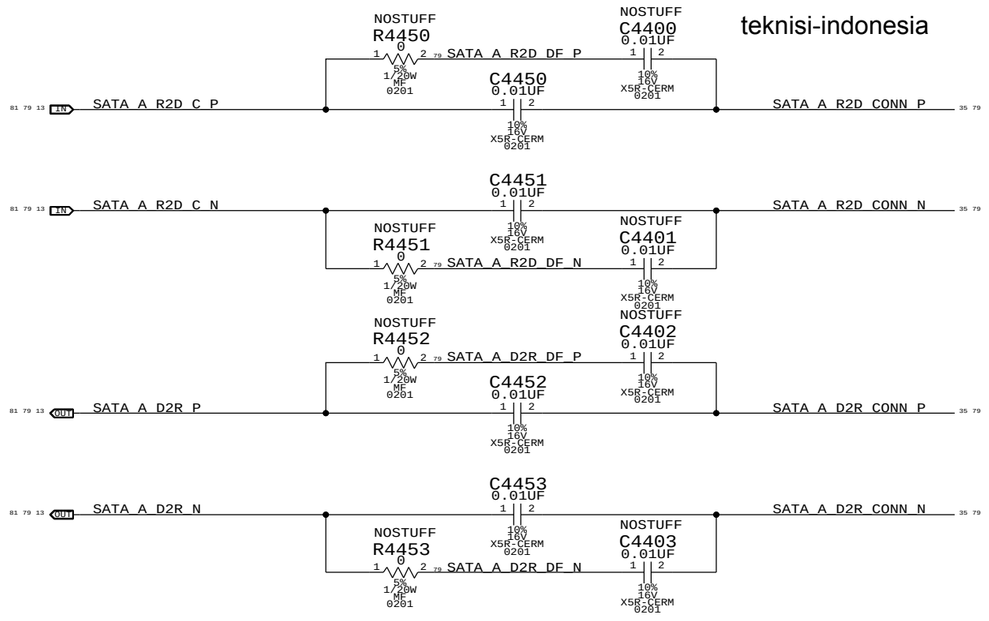
SATA CONNECTOR (HDD1)

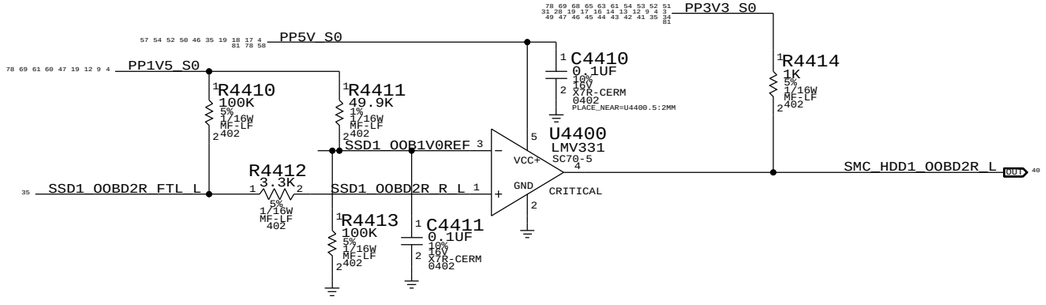




teknisi-indonesia

SATA OOB Comparator

Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD



SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-15
PAGE TITLE: HDD SATA CONNECTOR	
Apple Inc.	DRAWING NUMBER: 051-1907 SIZE: D
	REVISION: 4.0.0
	BRANCH:
	PAGE: 44 OF 500
	SHEET: 35 OF 83

LEFT MOST LOOKING AT BACK OF SYSTEM

EXT PORT A

EXT PORT B

REDUNDANCY FOR SAFETY

SIGNAL_MODEL=PI3USB102_TQFN_PI3USB102ZLE_MOJO

POLARITY REVERSED!

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4504,L4505		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,80OHM,25%,100MA	L4504,L4505		USB3_CHOKE:CHOKE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4514,L4515		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,80OHM,25%,100MA	L4514,L4515		USB3_CHOKE:CHOKE

514-0847

514-0847

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE

USB EXTERNAL PORTS A & B

Apple Inc.

DRAWING NUMBER 051-1907

SIZE D

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BRANCH

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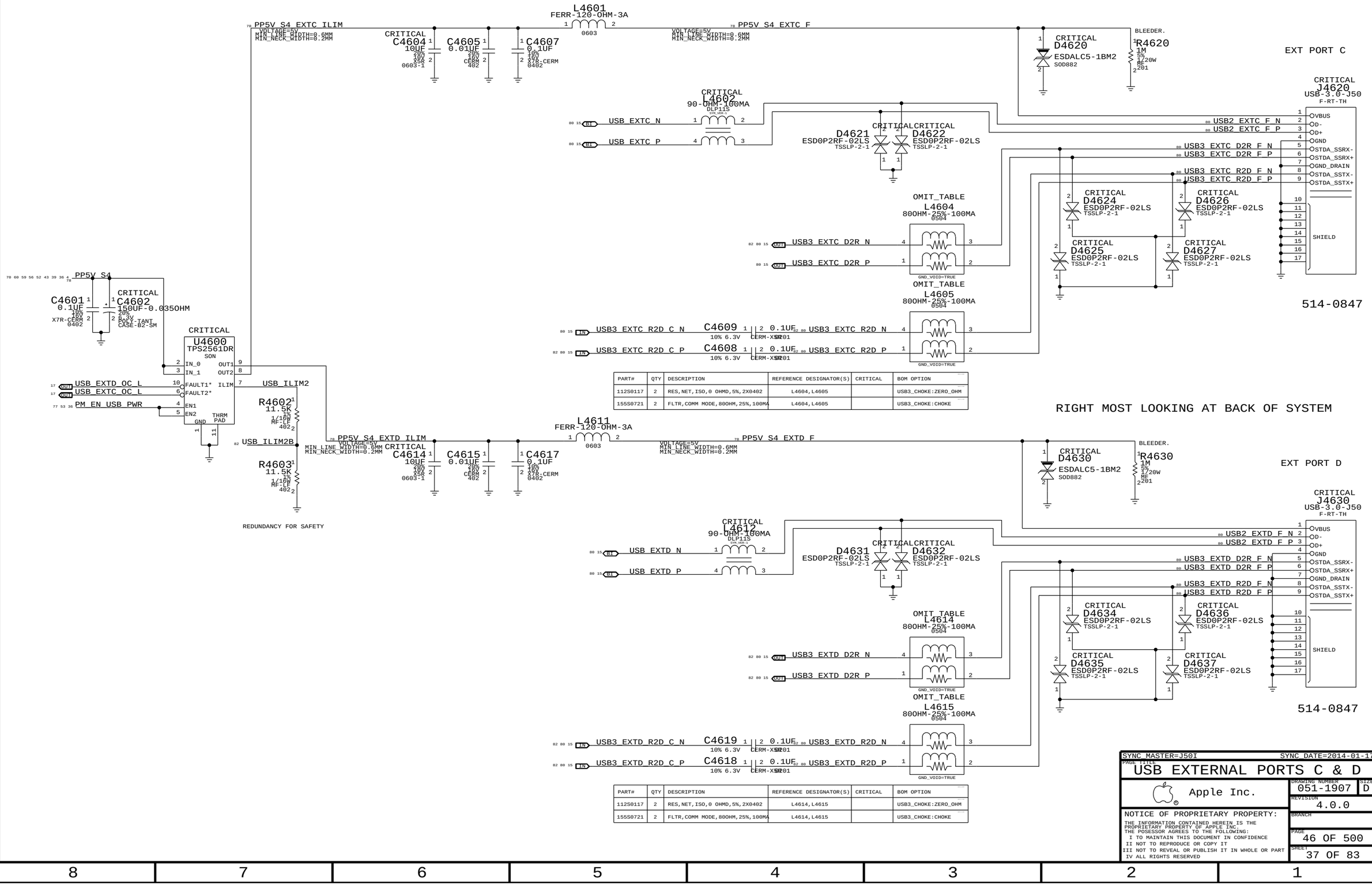

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4604,L4605		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,80OHM,25%,100MA	L4604,L4605		USB3_CHOKE:CHOKE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4614,L4615		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,80OHM,25%,100MA	L4614,L4615		USB3_CHOKE:CHOKE

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
USB EXTERNAL PORTS C & D

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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BRANCH

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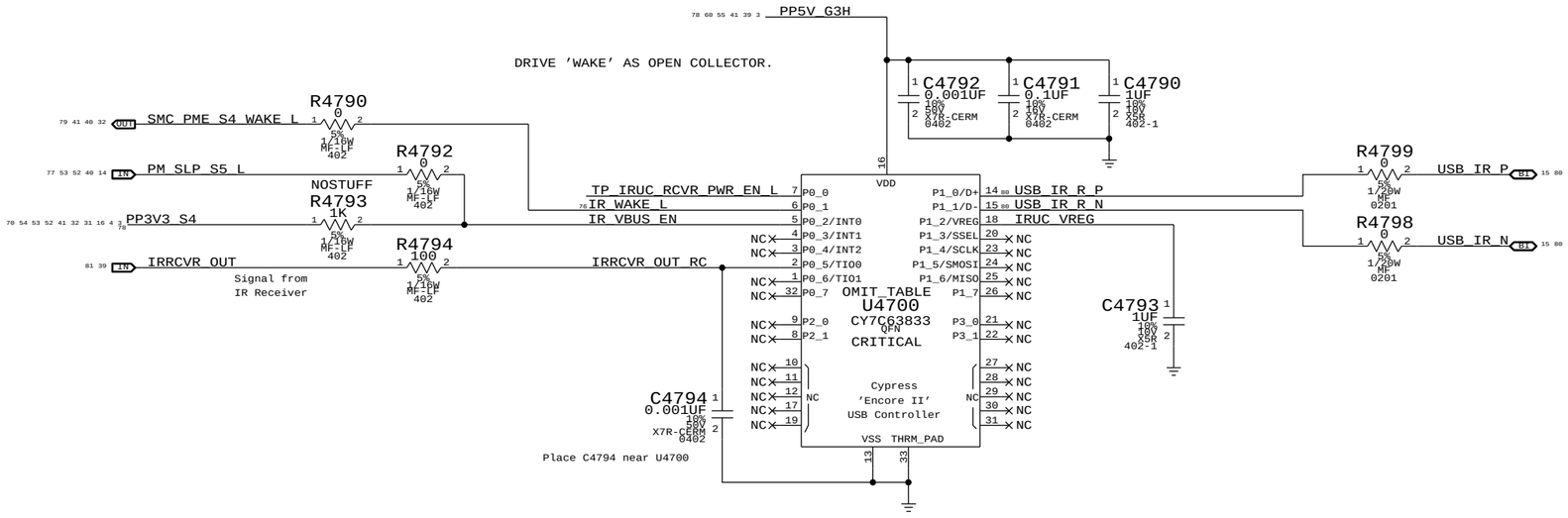
IR Controller



SYNC_MASTER=J50I	SYNC_DATE=2014-01-17
PAGE TITLE	IR CONTROLLER
Apple Inc.	DRAWING NUMBER 051-1907 · SIZE D
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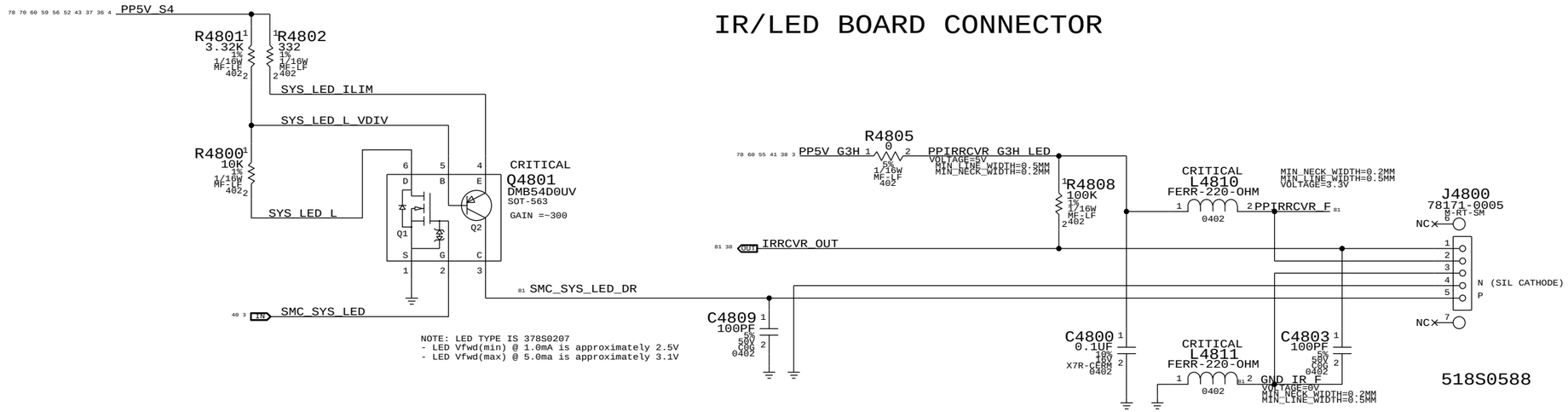
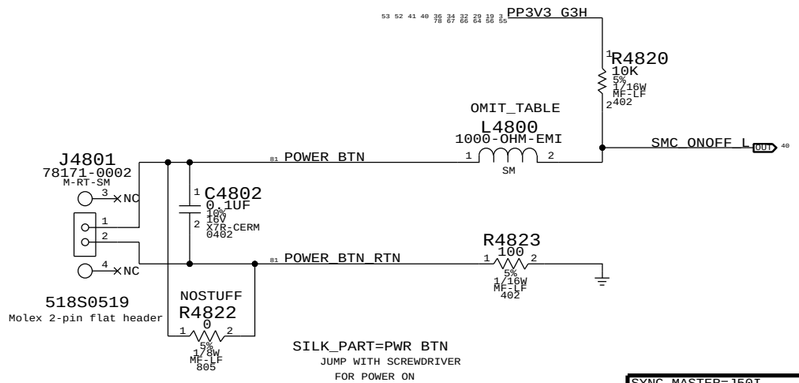
IR/LED BOARD CONNECTOR



SIL LED DRIVE CIRCUIT

Power Button Header



PLACE IN ACCESSIBLE PART OF BOARD.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0806	1	FLTR,EMI,1KOHM,1A,0603,SM	L4800		

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE: IR/SIL, PWR BTTN

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

BRANCH:

PAGE: 48 OF 500

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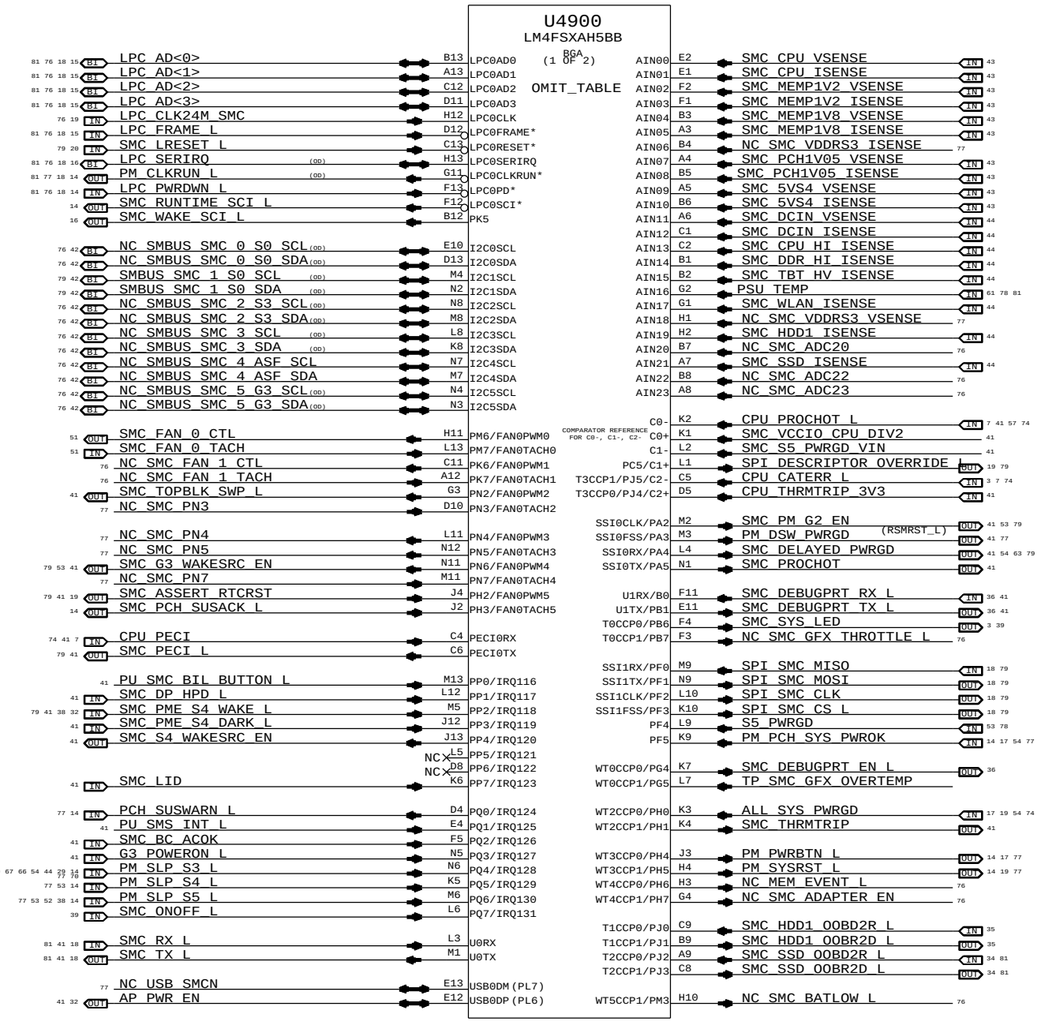
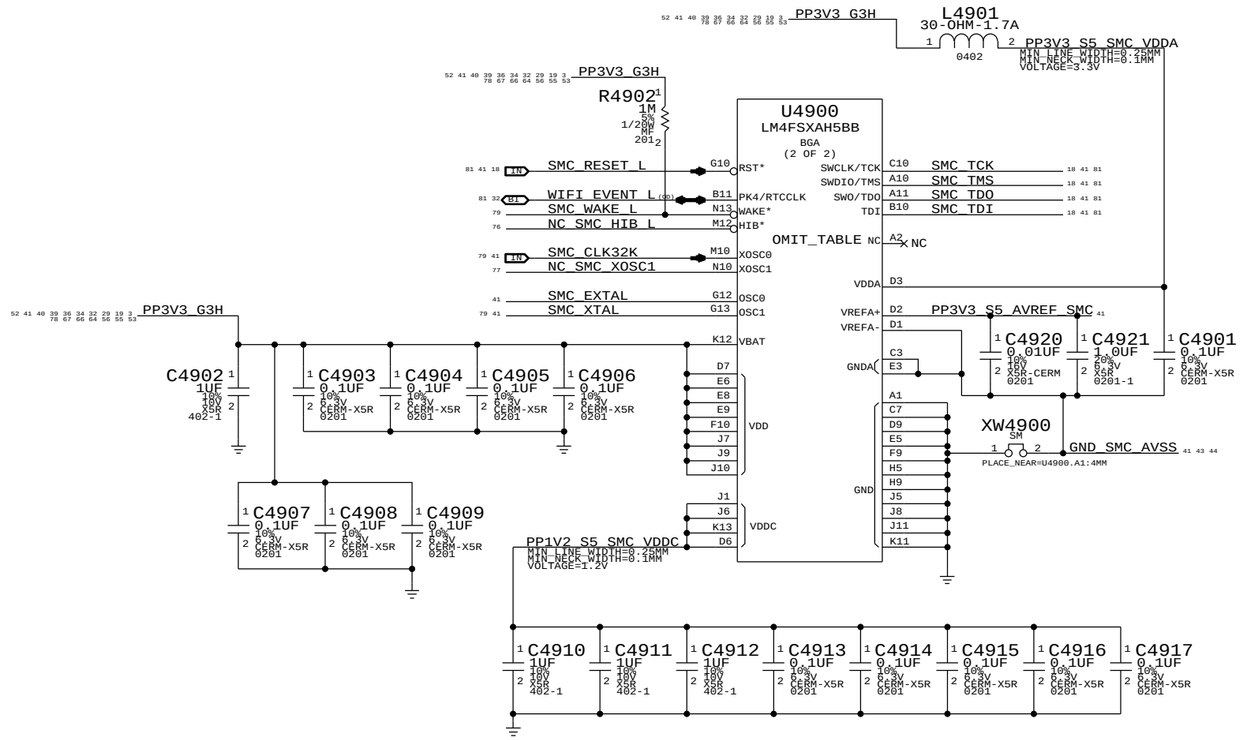


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-21
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER 051-1907 · SIZE D
	REVISION 4.0.0
	BRANCH
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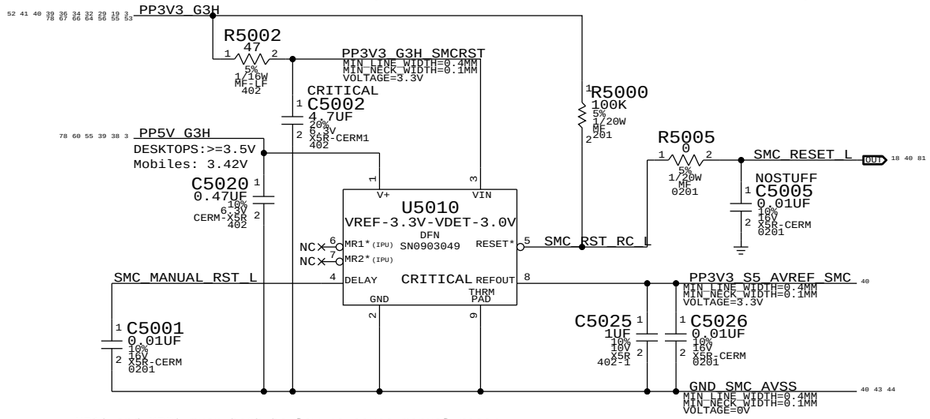
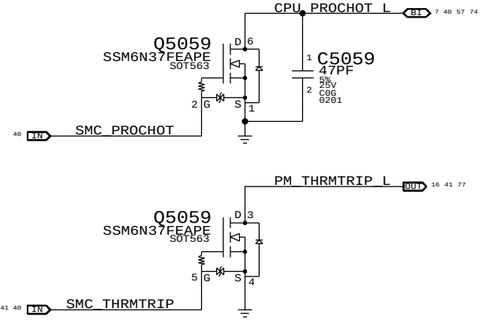
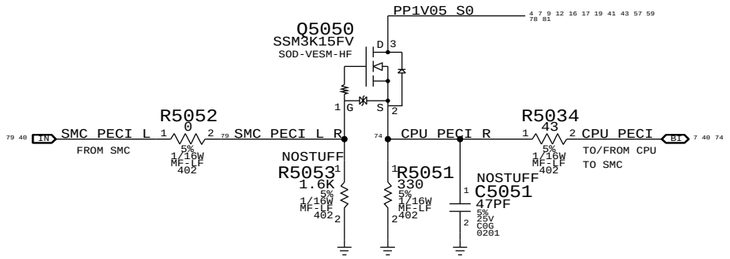
SMC Reset "Button", Supervisor & AVREF Supply

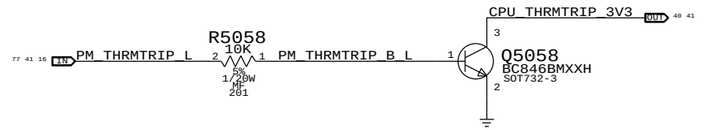


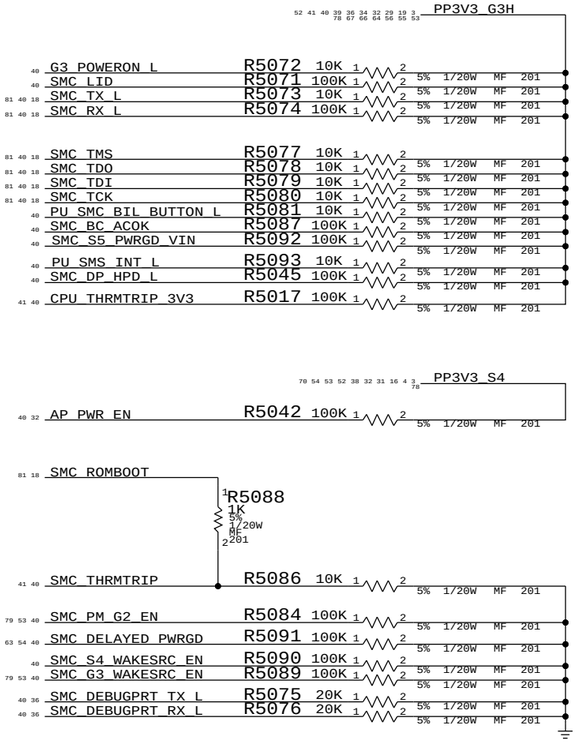
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.



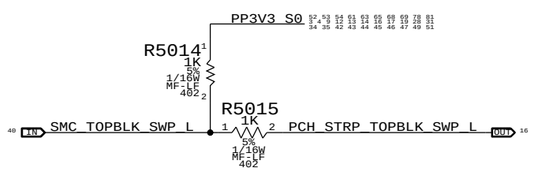
SMC12 PECI Support

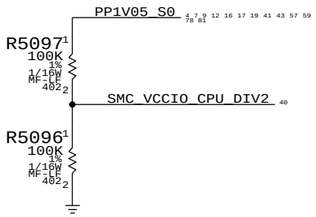




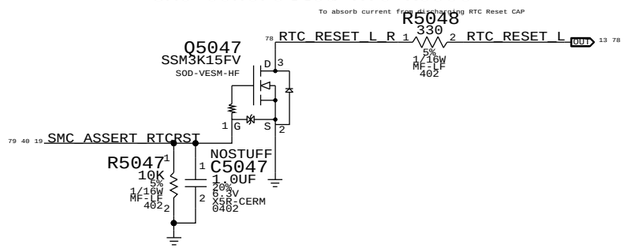


SMC Crystal Circuit

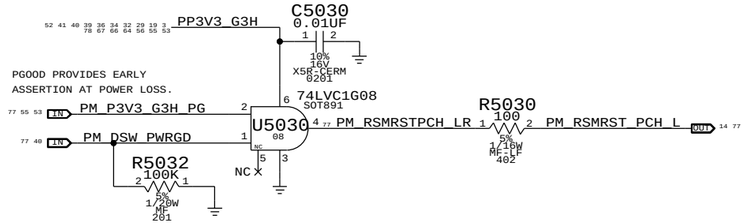




SMC Controlled RTC Reset

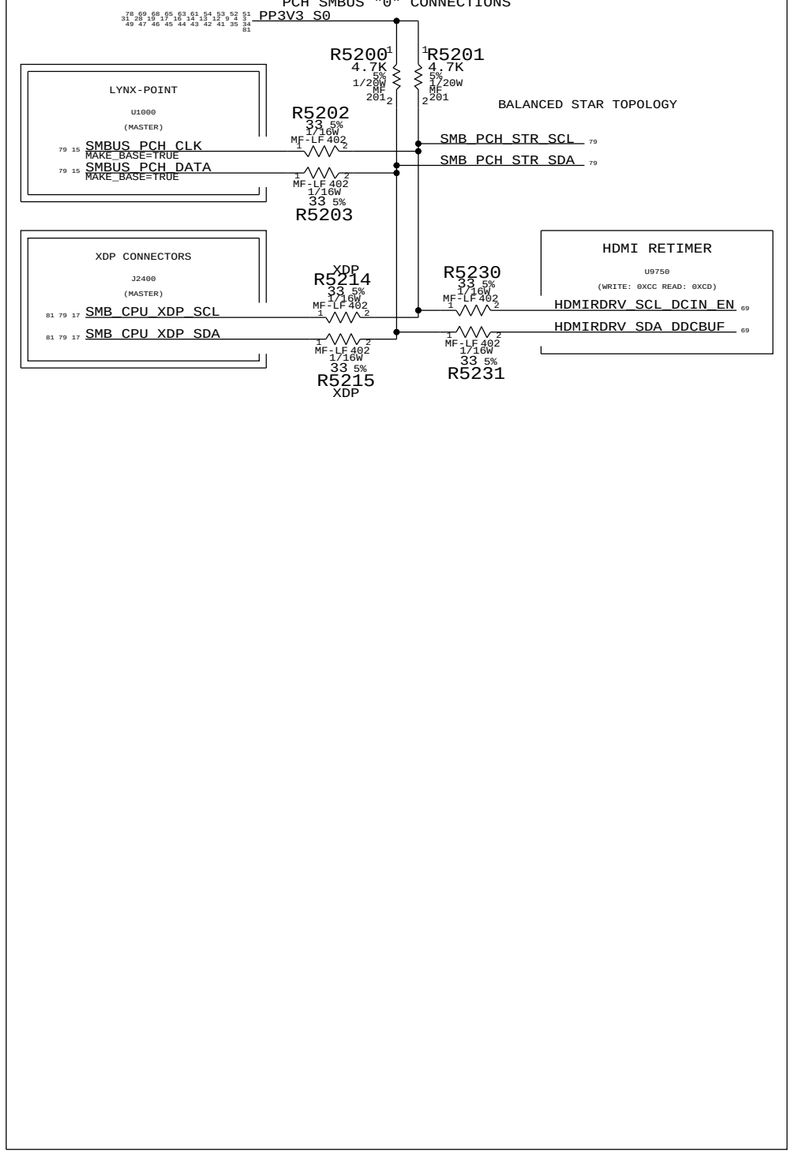


RESUME RESET LOGIC

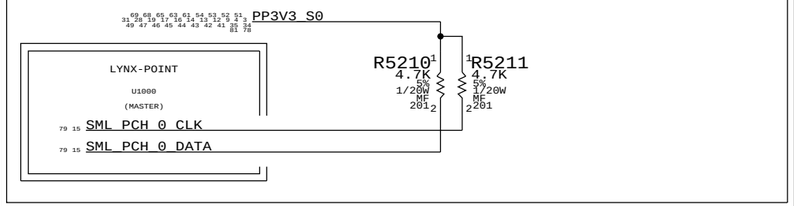


SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-21
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-1907 SIZE D
	REVISION 4.0.0
	BRANCH
	PAGE 50 OF 500
	SHEET 41 OF 83

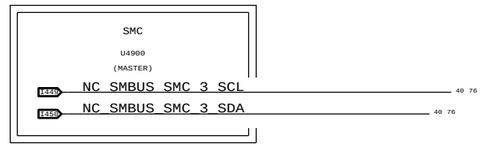
PCH SMBUS "0" CONNECTIONS



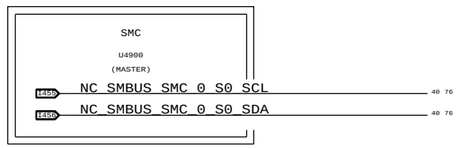
PCH "SMLINK 0" CONNECTIONS



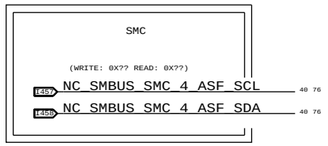
SMC "3" SMBUS CONNECTIONS



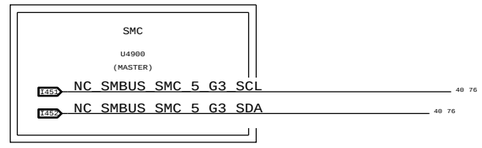
SMC "0" SMBUS CONNECTIONS



SMC "4" SMBUS CONNECTIONS

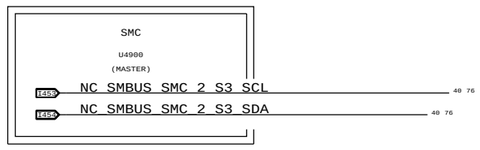


SMC "5" SMBUS CONNECTIONS

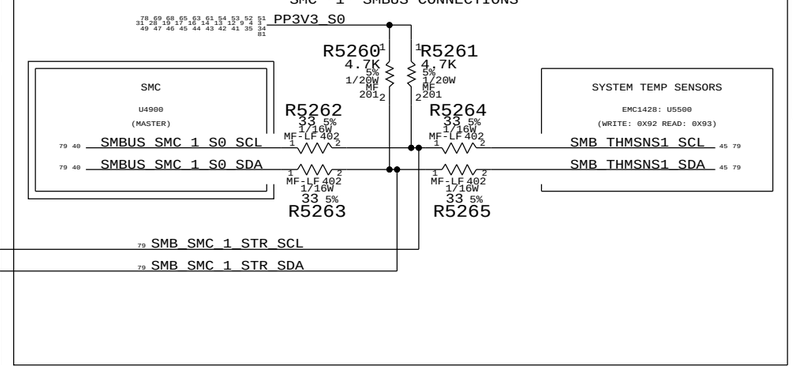


SMC "2" SMBUS CONNECTIONS

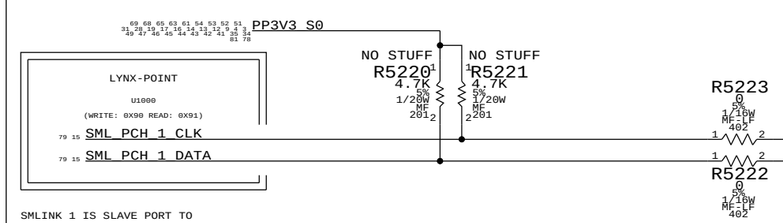
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE



SMC "1" SMBUS CONNECTIONS



PCH "SMLINK 1" CONNECTIONS



SMLINK 1 IS SLAVE PORT TO
ACCESS PCH & CPU VIA PECI.

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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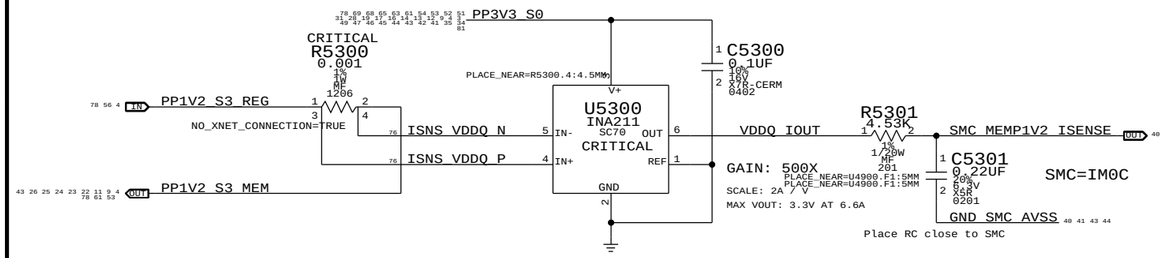
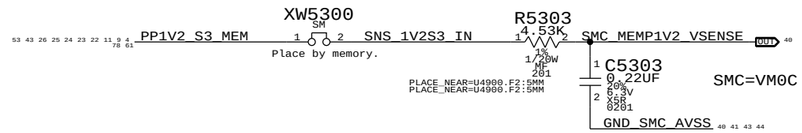
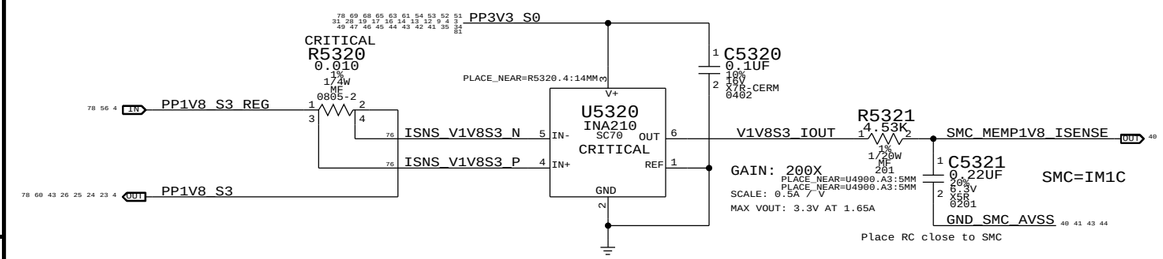
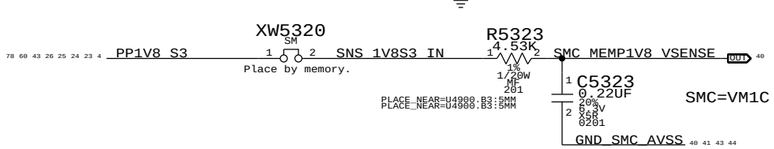
CPU/MEMORY VDDQ CURRENT SENSE FILTER



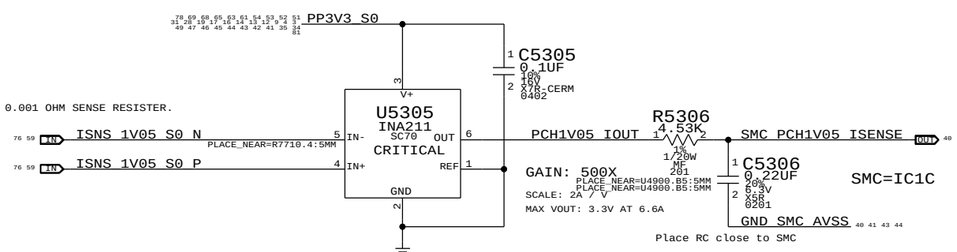


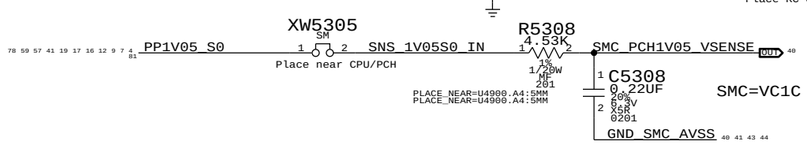
MEMORY 1.8V CURRENT SENSE FILTER



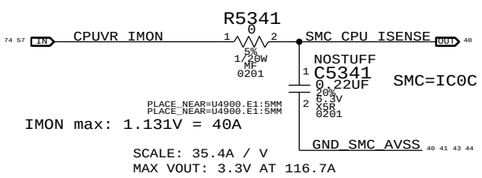


PCH 1.05V CURRENT SENSE FILTER

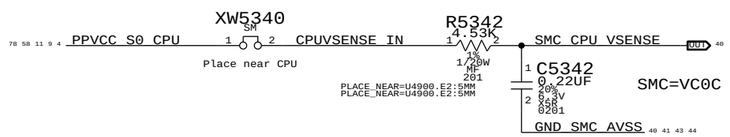




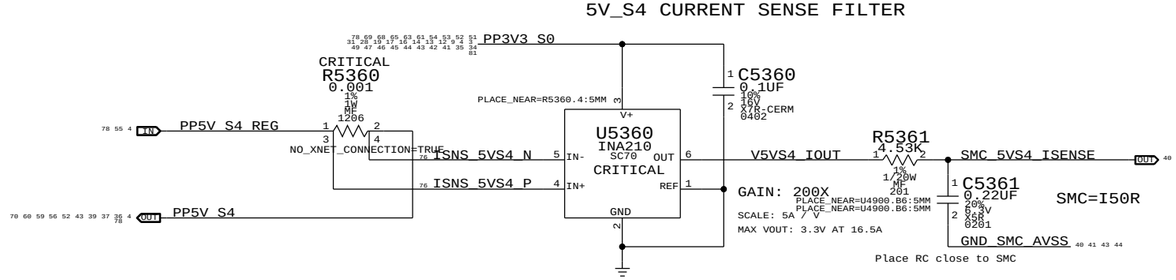
CPU VCORE IMON CURRENT SENSE / FILTER

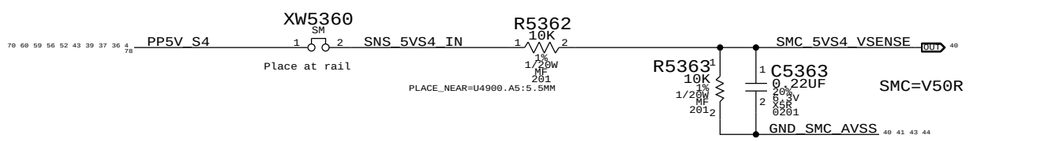


CPU Vcore Voltage Sense / Filter



5V_S4 CURRENT SENSE FILTER





SYNC MASTER=J64_2C SYNC_DATE=2014-01-15

PAGE TITLE

Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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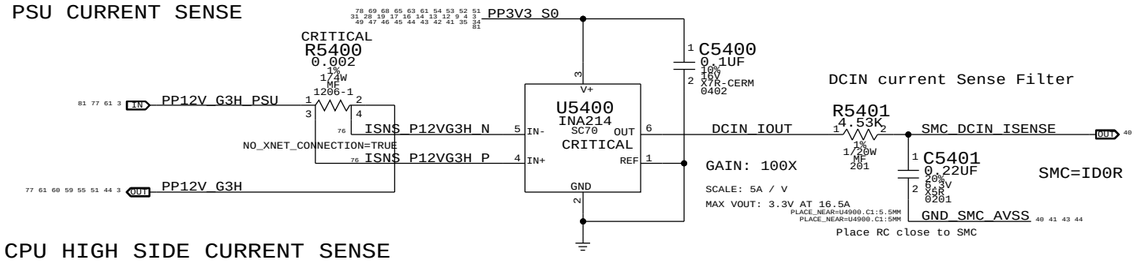
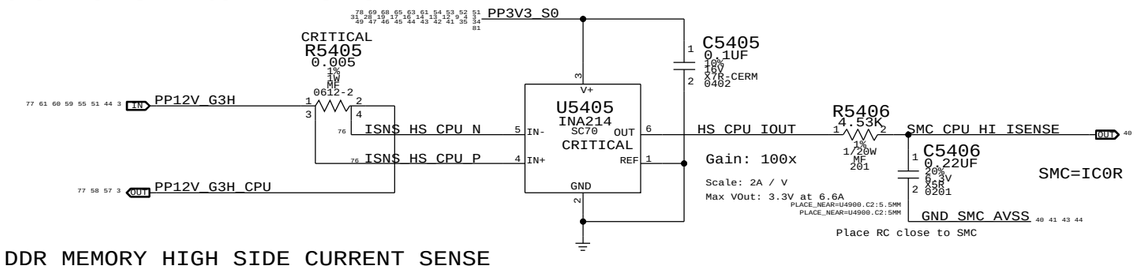
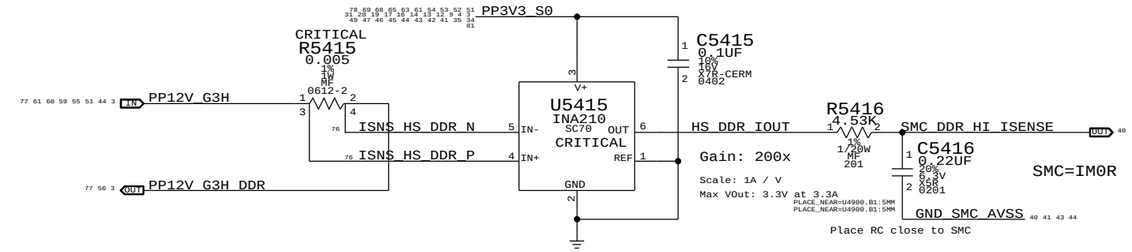
PSU CURRENT SENSE



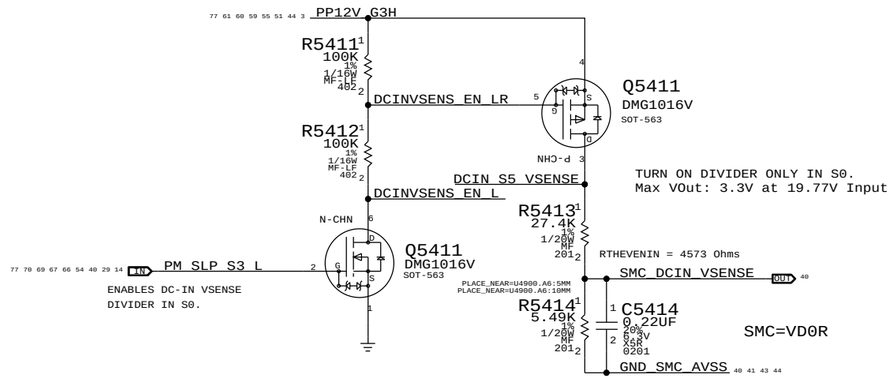
CPU HIGH SIDE CURRENT SENSE



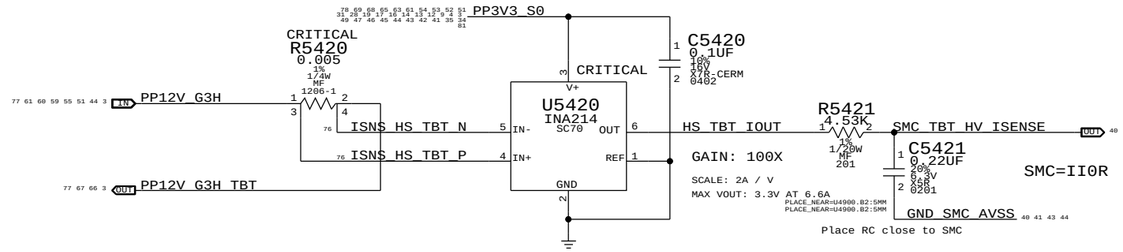
DDR MEMORY HIGH SIDE CURRENT SENSE



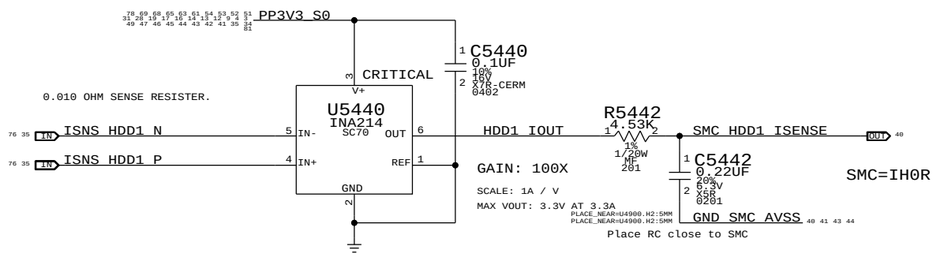
DC-In Voltage Sense Enable & Filter



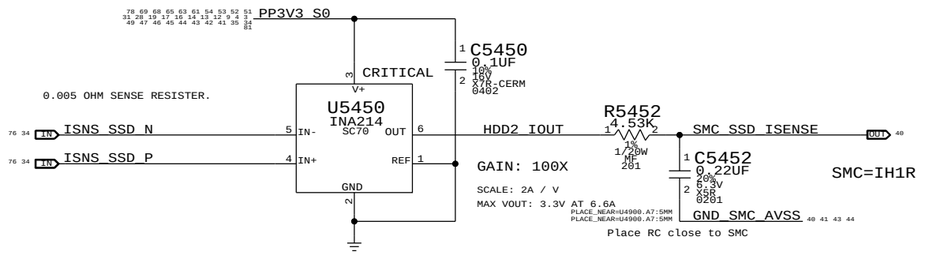
TBT HV BUS CURRENT SENSE



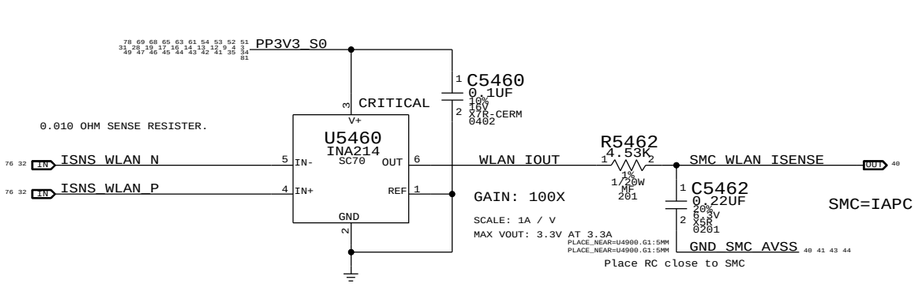
HDD1 CURRENT SENSE



SSD CURRENT SENSE



AIRPORT CURRENT SENSE



SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE: High Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D
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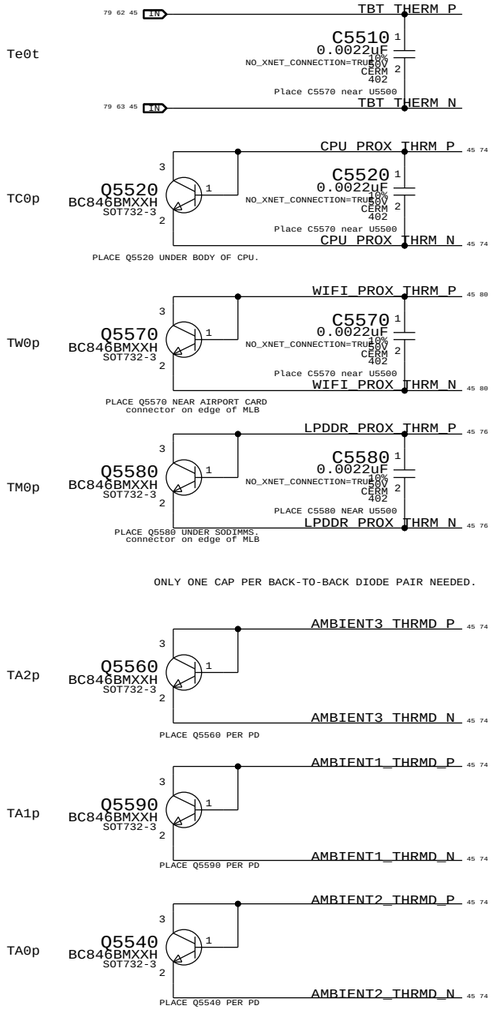

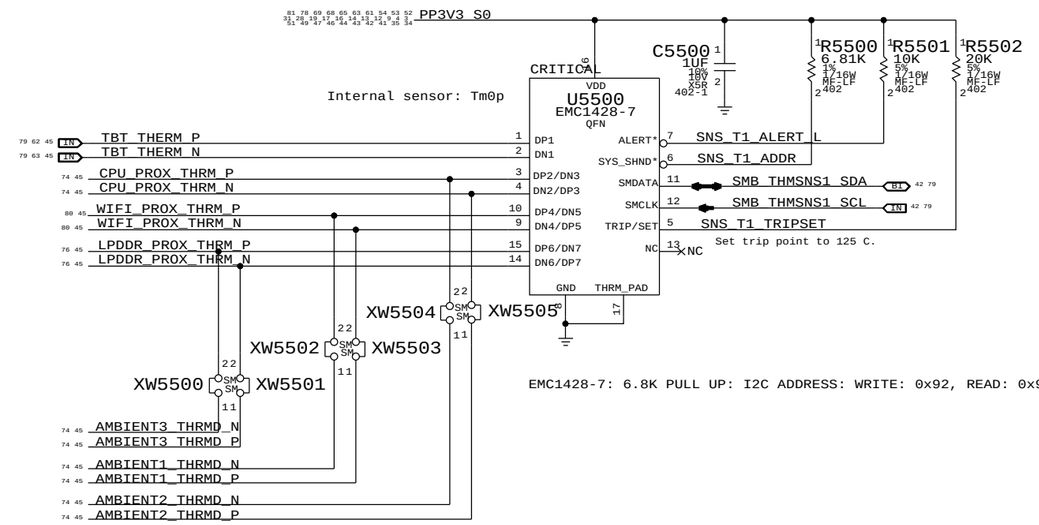

SYNC_MASTER=J64 2C SYNC_DATE=2014-01-23

PAGE TITLE: THERMAL SENSORS

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

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AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080

PP3V3_S0_AUDIO_ANALOG

PP4V5_AUDIO_ANALOG

L5601 FERR-22-OHM-1A-0.055OHM 0201 — PP3V3_S0

C5614 0.1UF 10% 16V X7R-CERM 0402

C5613 CRITICAL 10UF 20% 10V TANT-POLY 0402-7

GND_AUDIO_CODEC

C5618 0.1UF 10% 16V X7R-CERM 0402

C5616 0.1UF 10% 16V X7R-CERM 0402

C5617 CRITICAL 10UF 20% 10V TANT-POLY 0805-LLP-1

BYPASS=U5601.H12:L10:5 MM

BYPASS=U5601.M13:M11:5 MM

C5612 0.1UF 10% 16V X7R-CERM 0402

BYPASS=U5601.A1:A2:5 MM

C5619 CRITICAL 22UF 20% 6.3V X5R-CERM2 0603

BYPASS=U5601.A11:A10:3 MM

C5615 CRITICAL 10UF 20% 10V TANT-POLY 0805-LLP-1

BYPASS=U5601.H12:H13:5 MM

C5622 CRITICAL 22UF 20% 6.3V X5R-CERM2 0603

BYPASS=U5601.A8:B10:3 MM

CODEC_FLYP

CODEC_FLYN

MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.10 MM

U5601 CS4208-CRZR VFBGA ANALOG SYM 1 OF 2 CRITICAL

VA_REF H12 · VA_HP A9 · VA_PLL A1 · VA N13

VREF_DAC H13 · VHP_FILT- N11 · FLYP A8 · FLYN B10 · FLYN B11

AUD_CODEC_LI_L_P — C5640 100PF 5% 50V C0G 0402 — LINEIN_L+ N10 · LINEIN_L- M10

AUD_CODEC_LI_L_N

AUD_CODEC_LI_R_P — C5641 100PF 5% 50V C0G 0402 — LINEIN_R+ N9 · LINEIN_R- M9

AUD_CODEC_LI_R_N

MICBIAS1_L L8 · MICBIAS1_R L7 · MICBIAS2_L L5 · MICBIAS2_R L4

C5629 0.1UF 10% 16V X5R-CERM 0201 — MICIN1

C5630 0.1UF 10% 16V X5R-CERM 0201 — MICIN2

GND_AUDIO_CODEC

MICIN1_L+ M8 · MICIN1_L- · MICIN1_R+ N7 · MICIN1_R- M7

MICIN2_L+ N5 · MICIN2_L- M5 · MICIN2_R+ N4 · MICIN2_R- M4

AUD_HSBIAS_IN — R5606 2.21K 1% 1/20W MF 201

AUD_HSBIAS — C5620 1UF 20% 16V CER-X5R 0201

AUD_HSBIAS_REF — C5621 CRITICAL 4.7UF 20% 10V X5R-CERM 0402 — AUD_HSBIAS_FILT

HSBIAS_IN L12 · HSBIAS L13 · HSBIAS_REF M13 · HSBIAS_FILT N11

HPOUT_L A12 · HPOUT_R A13 · SENSE_A1 C11 · SENSE_A2 D12 · HS3 C13 · HS4 C12 · HS3_REF B13 · HS4_REF B12 · HSIN+ N6 · HSIN- M6 · SENSE_B1 E11 · SENSE_B2 D11 · SENSE_C M3 · SENSE_D L3

AUD_CODEC_HPO_L — MIN_LINE_WIDTH=0.20 MM MIN_NECK_WIDTH=0.10 MM — R5660 28 1% 1/16W MF-LF 402 — AUD_HPO_L OUT

AUD_CODEC_HPO_R — MIN_LINE_WIDTH=0.20 MM MIN_NECK_WIDTH=0.10 MM — R5661 28 1% 1/16W MF-LF 402 — AUD_HPO_R OUT

AUD_HPO_TIPDET1 IN · AUD_HPO_TIPDET2 IN

XW5611 SM — AUD_HS_MICN

XW5610 SM — AUD_HS_MICP

PLACE_NEAR=U5601.C13:4MM NO_XNET_CONNECTION=TRUE

PLACE_NEAR=U5601.C12:4MM NO_XNET_CONNECTION=TRUE

AUD_US_HS_GND IN · AUD_CH_HS_GND IN · AUD_HPO_REFUS IN · AUD_HPO_REFCH IN

AUD_CODEC_HS_MICP — AUD_CODEC_HS_MICN

AUD_LI_TIPDET IN

TP_AUD_SENSEB2

AUD_HPO_TYPEDET IN · AUD_LI_TYPEDET IN

C5624 1UF 20% 16V CER-X5R 0201 — AUD_FILT_HS_MICP

C5625 1UF 20% 16V CER-X5R 0201 — AUD_FILT_HS_MICN

HP AMP. SIG. SOURCE

LINEOUT1_L+ E12 · LINEOUT1_L- E13 · LINEOUT1_R+ F11 · LINEOUT1_R- F12 · LINEOUT2_L+ F13 · LINEOUT2_L- G11 · LINEOUT2_R+ G12 · LINEOUT2_R- G13 · LINEOUT3_L+ H11 · LINEOUT3_L- J11 · LINEOUT3_R+ J12 · LINEOUT3_R- J13 · LINEOUT4_L+ K11 · LINEOUT4_L- K12 · LINEOUT4_R+ K13 · LINEOUT4_R- L11 — all NC

AUD_LO2_L_P · AUD_LO2_L_N

L5611 CRITICAL FERR-1000-OHM 0402 — AUD_SPKR_P OUT

L5610 CRITICAL FERR-1000-OHM 0402 — AUD_SPKR_N OUT

SPKR AMP. SIG. SOURCE

VCOM M12 CODEC_VCOM · VREF_ADC N12 CODEC_VREF_ADC

AGND M11 · AGND L6 · AGND L9 · AGND L10 · HPGND A10 · HPGND C8 · HPGND C10 · HSGND D13 · PLLGND A2

C5610 CRITICAL 1UF-10OHM 20% 25V TANT 0603-LLP

C5611 CRITICAL 10UF 20% 10V TANT-POLY 0805-LLP-1

GND_AUDIO_CODEC

4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2281

PLACE XW5601 NEAR 5V SOURCE

XW5601 SM — PP5V_S0 — PP5V_S0_AUDIO_XW

L5600 CRITICAL 120-OHM-25%-1.3A 0402 — 4V5_REG_IN

U5600 TPS71745 SON — IN · OUT → PP4V5_AUDIO_ANALOG · NR/FB → 4V5_NR · EN ← 4V5_REG_EN · GND · NC

4V5_REG_EN

R5603 2.2K 5% 1/20W MF 201

NOSTUFF R5600 2.2K 5% 1/20W MF 201 — PP3V3_S0

C5600 1UF 10% 10V X5R 402-1

C5601 1UF 10% 10V X5R 402-1

XW5600 SM

C5602 0.01UF 10% 16V X5R-CERM 0201

C5603 CRITICAL 1.0UF 20% 10V X5R-CERM 0201-1

GND_AUDIO_CODEC

PLACE XW5600 BENEATH U5600, BETWEEN PINS 2 & 5

MIC FILTER

AUD_FILT_HS_MICP — R5650 2.2K 1% 1/20W MF 201 — AUD_HS_MICP

R5656 100K 5% 1/20W MF 201 · C5650 CRITICAL 3300PF 10% 10V X7R-CERM 0201 · C5658 CRITICAL 27PF 5% 25V C0G 0201

AUD_FILT_HS_MICN — R5659 2.2K 1% 1/20W MF 201 — AUD_HS_MICN

R5659&R/C5650 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)

SYNC_MASTER=SUPER_IO SYNC_DATE=2014-06-16

PAGE TITLE: AUDIO:CODEC 1

Apple Inc.

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AUDIO CODEC, DIGITAL BLOCKS

L5700
FERR-22-OHM-1A-0.055OHM
0201

PP1V5_S0
PP1V5_S0_AUDIO_DIG

CRITICAL
C5700 4.7UF 20% 6.3V X5R-CERM 402
C5701 0.1UF 10% 10V X7R-CERM 0402
BYPASS=U5601.J2:J1:5 MM
C5702 0.1UF 10% 10V X7R-CERM 0402
BYPASS=U5601.E1:F1:5 MM

PP3V3_S0
C5703 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U5601.G1:F1:5 MM
C5704 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U5601.K1:K3:5 MM
CRITICAL
C5705 10UF 20% 10V X5R-CERM 0402-7
CRITICAL
C5706 10UF 20% 10V X5R-CERM 0402-7
C5707 0.1UF 10% 10V X5R-CERM 0201
PP3V3_S0
BYPASS=U5601.A7:E3:6 MM

OMIT
R5726 SHORT 201
OMIT
R5724 SHORT 201
OMIT
R5723 SHORT 201
R5722 100K 5% 1/20W MF 201
R5725 100K 5% 1/20W MF 201

R5701 0 5% 1/16W MF-LF 402
AUD_SPDIF_IN
R5702 33 5% 1/16W MF-LF 402
AUD_SPDIF_OUT

U5601
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2
CRITICAL

AUD_SPKR_SHDN
PD_CODEC_GPIO1
PD_CODEC_GPIO2
PD_CODEC_GPIO3
DFET_OPENUS
DFET_OPENCH
HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
R5700 22 1% 1/20W MF 201
CS4208_HDA_SDOUT0_R
CS4208_SPDIF_IN
CS4208_SPDIF_OUT

PD_CODEC_SDA
PD_CODEC_SCL
OMIT
R5721 SHORT 201
OMIT
R5720 SHORT 201

SYNC_MASTER=SUPER_IO SYNC_DATE=2014-06-16
PAGE TITLE: AUDIO:CODEC 2
Apple Inc.
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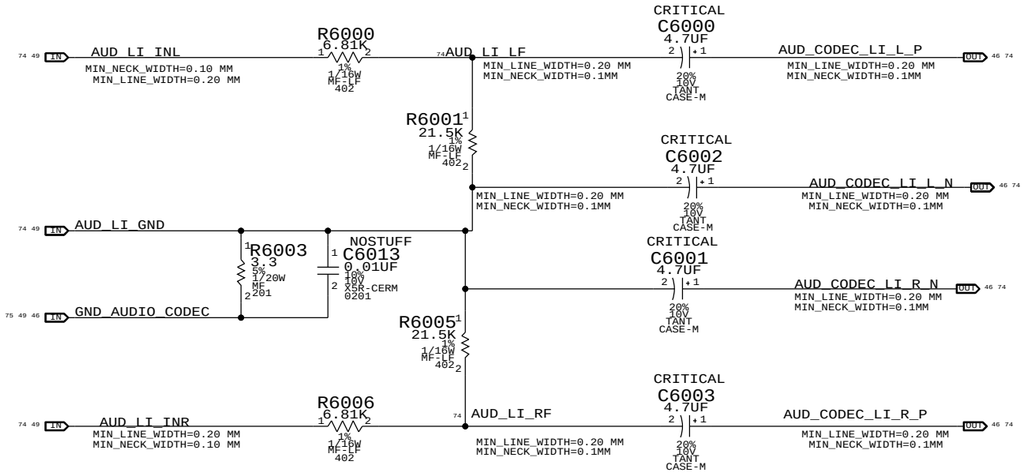
CODEC NOM SE RIN = 33K OHMS, +/-10%
FC, LP = 3 HZ MAX
FC, HP (WITH C5640/C5641) = 290 KHZ MAX
SYSTEM VIN FS = 2VRMS, CODEC VIN FS PSEUDODIFF = 1.3 VRMS TYP



SYNC_MASTER=J50I SYNC_DATE=2014-06-16

PAGE TITLE
AUDIO:LINE IN PATH

Apple Inc.

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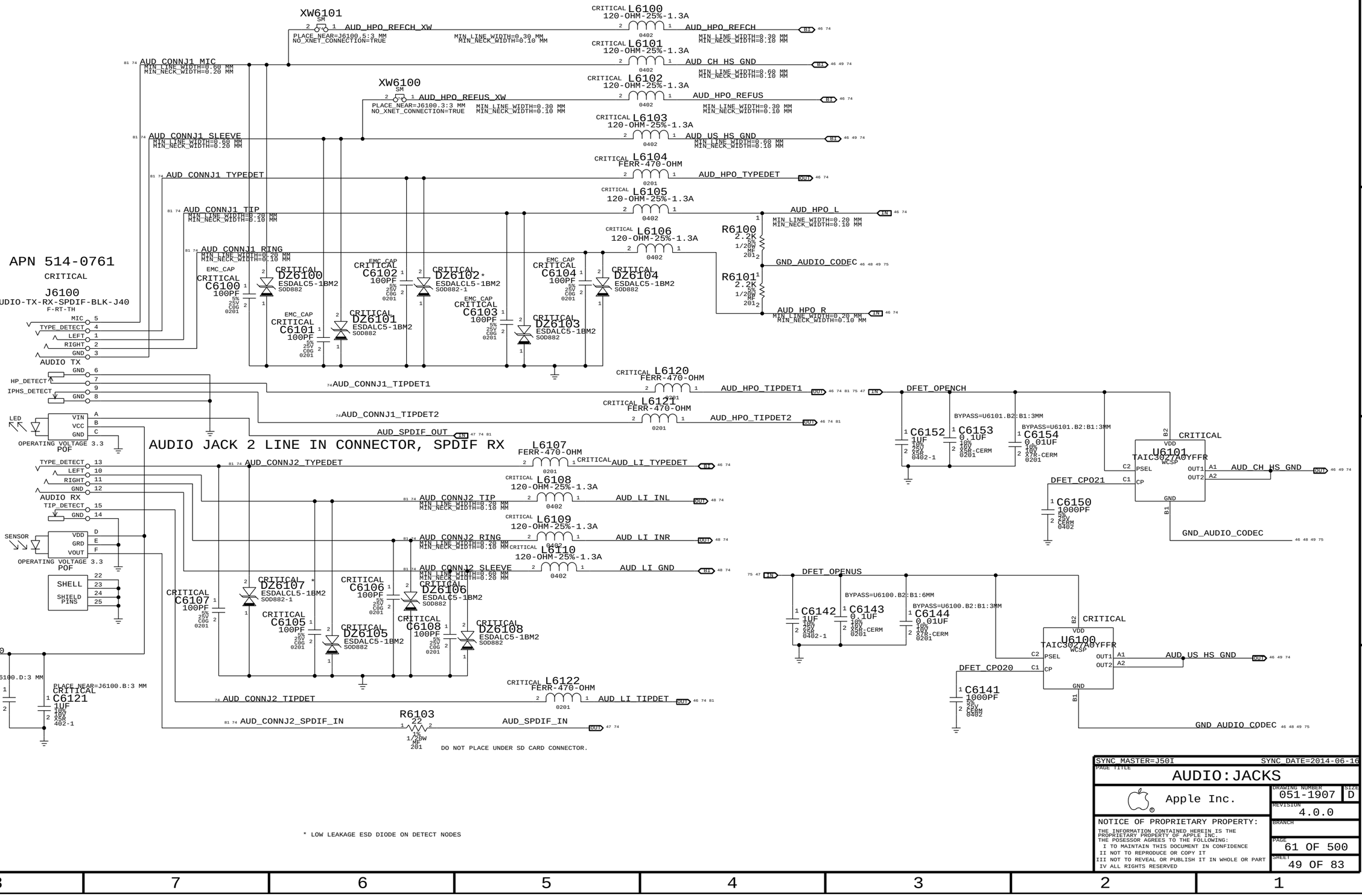
AUDIO JACK 1 LO/HP CONNECTOR, SPDIF TX



* LOW LEAKAGE ESD DIODE ON DETECT NODES

SYNC_MASTER=J50I SYNC_DATE=2014-06-16

PAGE TITLE
AUDIO:JACKS

Apple Inc.

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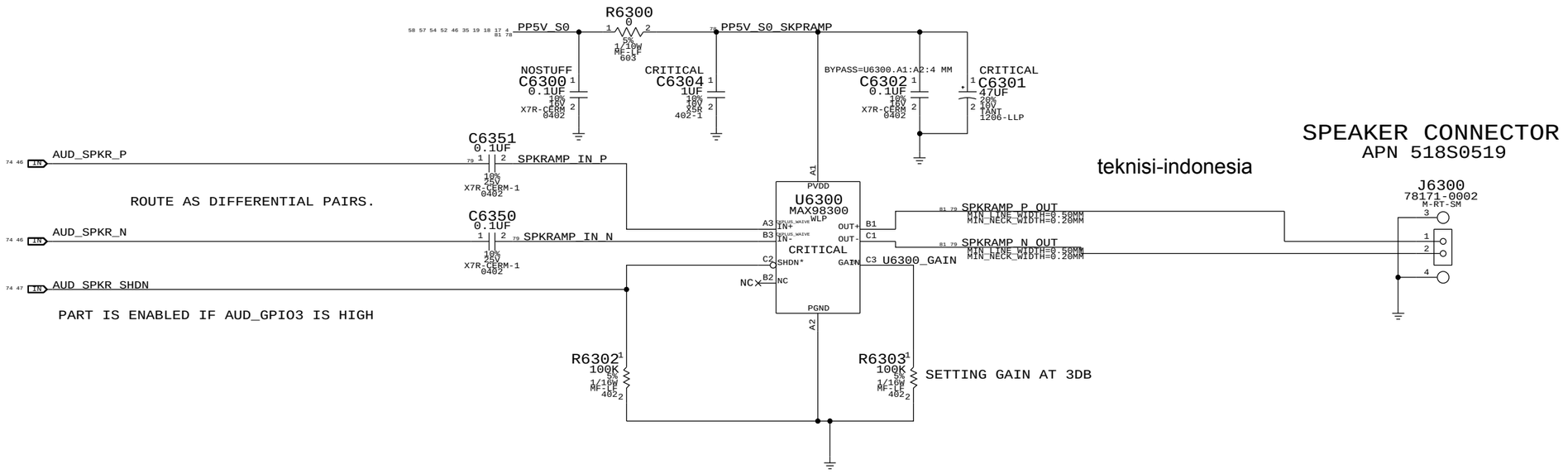
MONO SPEAKER AMPLIFIER

APN 353S2888

GAIN = 3 DB NOM TO ALLOW A LITTLE MORE THAN 1% THD POWER = 2.1W AT 4OHMS.
FC = ~114 HZ. RIN AT 3DB IS 28K.



SPEAKER CONNECTOR

APN 518S0519

SYNC_MASTER=J50I	SYNC_DATE=2014-06-16
PAGE TITLE	AUDIO:SPEAKER AMP
Apple Inc.	DRAWING NUMBER 051-1907 · SIZE D
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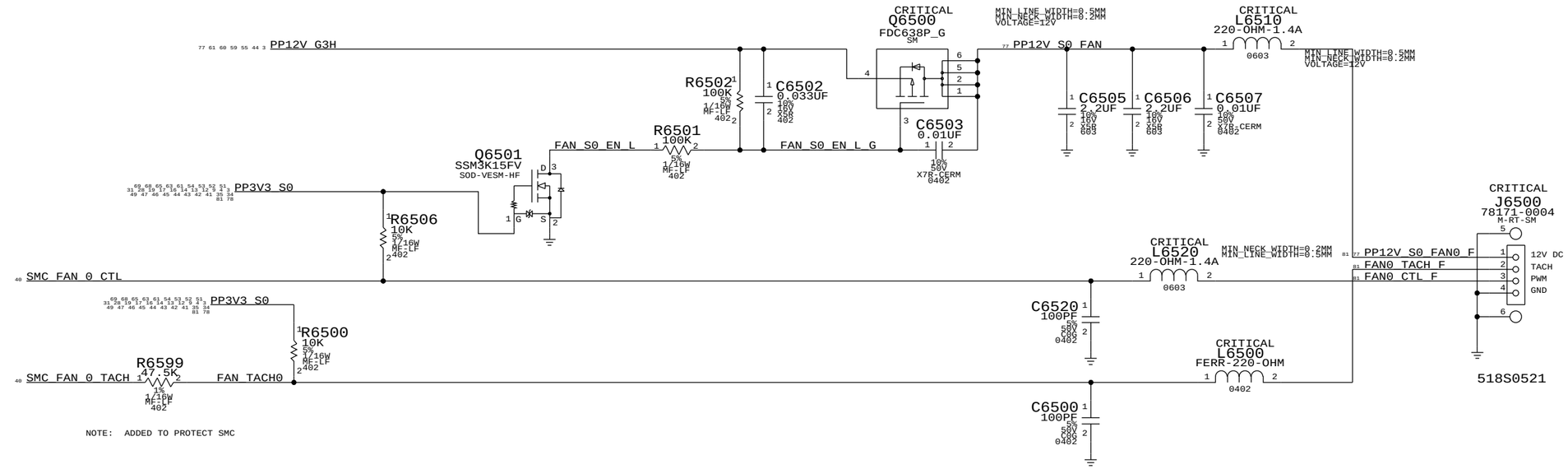
FAN CONTROL CIRCUIT



SYNC_MASTER=J50I	SYNC_DATE=2014-01-17
PAGE TITLE: Fan Control Circuit	
Apple Inc.	DRAWING NUMBER: 051-1907 SIZE: D
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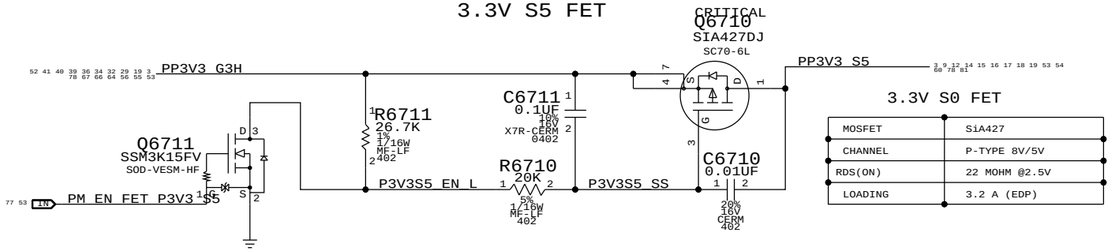
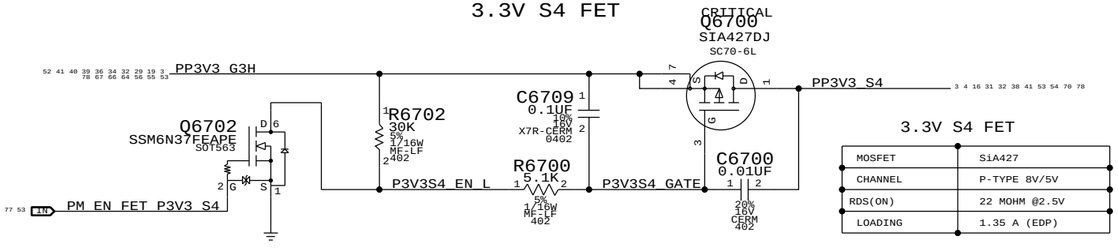
3.3V S5 FET



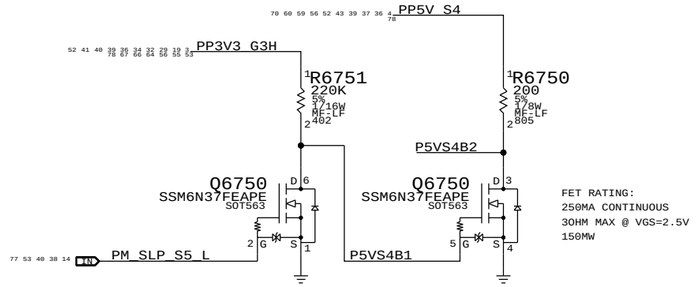
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	22 MOHM @2.5V
LOADING	3.2 A (EDP)

3.3V S4 FET

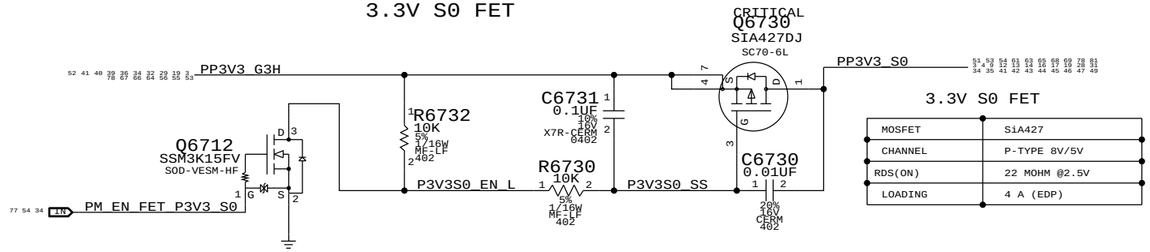


MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	22 MOHM @2.5V
LOADING	1.35 A (EDP)

5.0V S4 BLEEDER

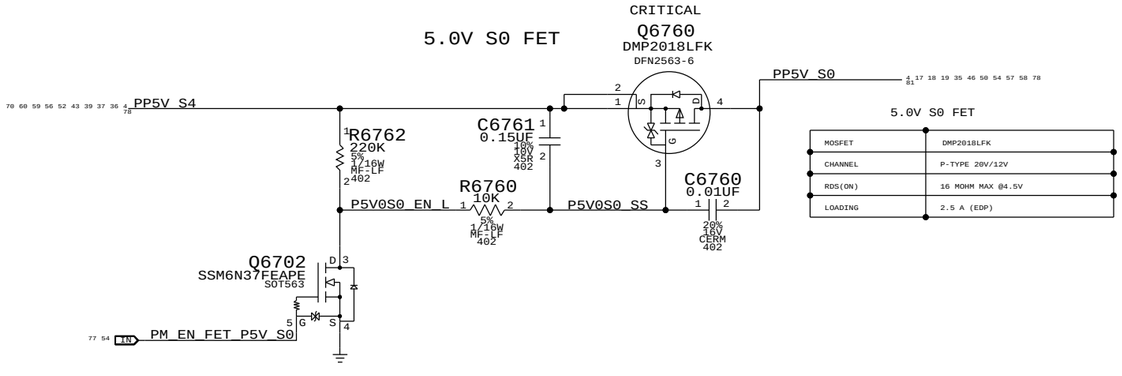


3.3V S0 FET



MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	22 MOHM @2.5V
LOADING	4 A (EDP)

5.0V S0 FET



MOSFET	DMP2018LFK
CHANNEL	P-TYPE 20V/12V
RDS(ON)	16 MOHM MAX @4.5V
LOADING	2.5 A (EDP)

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-15

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

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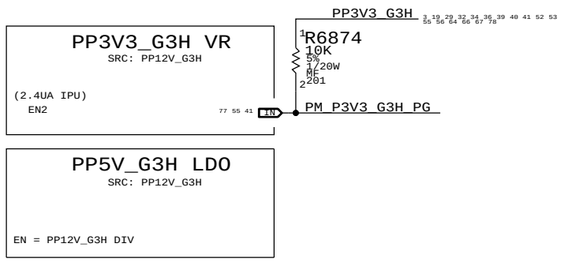
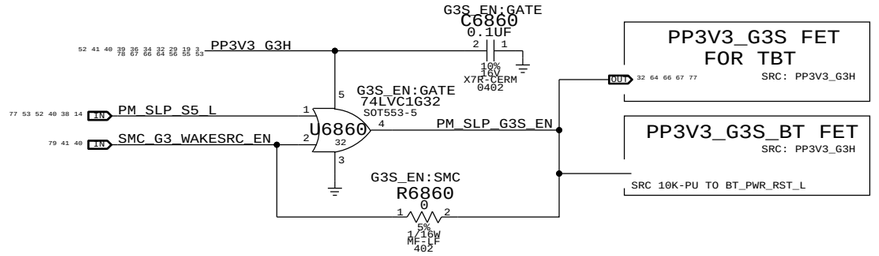
G3H VRS

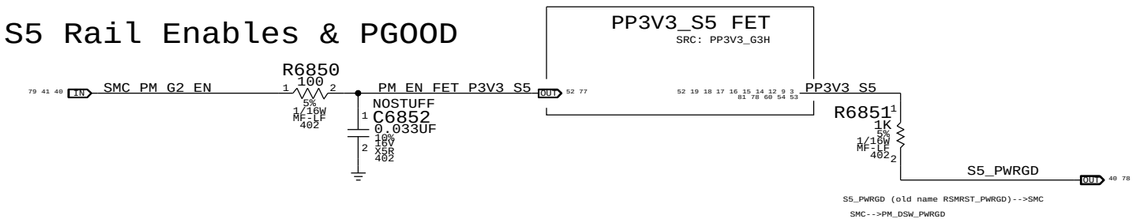


G3STANDBY DEVICE ENABLE

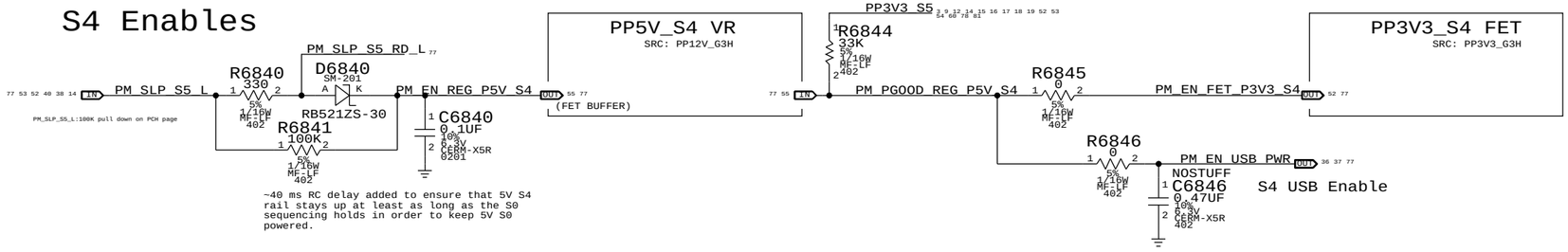


State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
RUN (S0)	1	1	1	1
SLEEP (S3)	1	1	1	0
DEEP SLEEP/HIBERNATE (S4)	1	1	0	0
OFF (S5)	1	0	0	0
AC POWER (G3HOT)	0	0	0	0

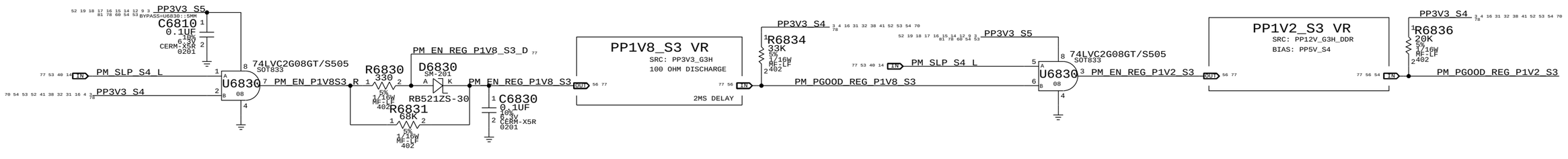
S5 Rail Enables & PGOOD



S4 Enables

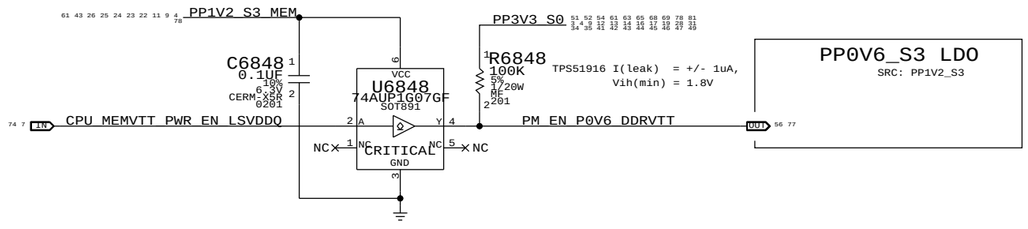


S3 Enables



Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).



SYNC MASTER=J64 2C SYNC DATE=2014-01-16

PAGE TITLE

POWER CONTROL 1: S5-S3

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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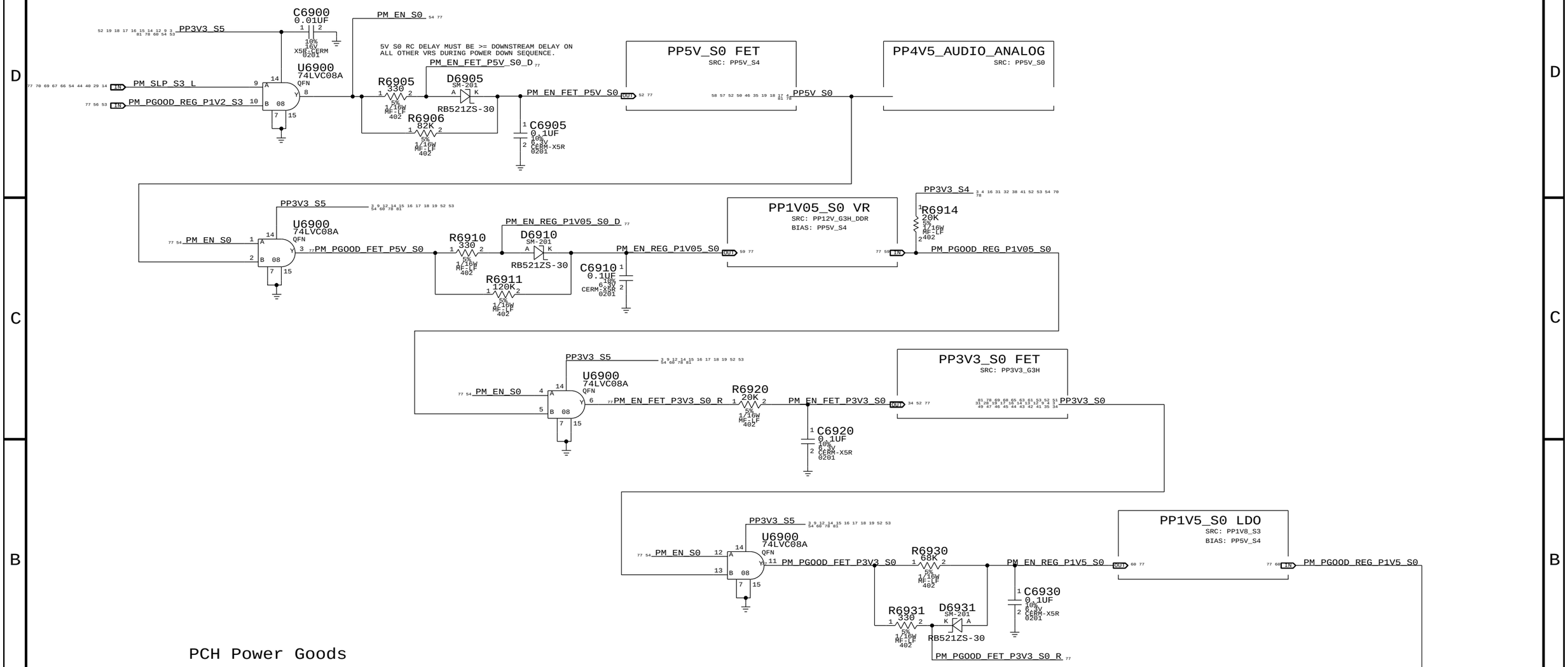
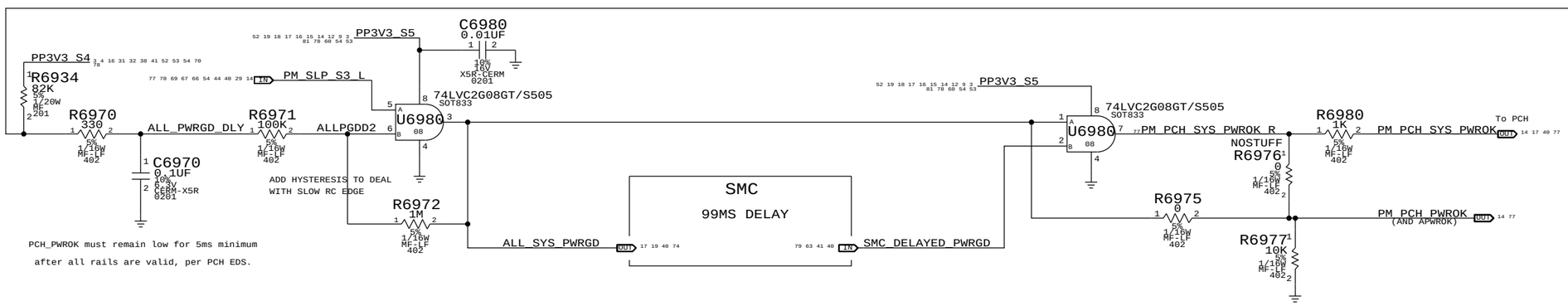
S0 Enables

Audio + PCH Sequencing Requirements:
5V (4.5V) -> 1.05V -> 3.3V -> 1.5V -> ALL SYS GOOD
POWER DOWN IN REVERSE ORDER.



PCH Power Goods



SYNC_MASTER=J64_2C SYNC_DATE=02/03/2014

PAGE TITLE
POWER CONTROL 2:S0

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D
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PAGE 69 OF 500
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PP12V_G3H
C7243 15UF 20% 16V TANT SM
C7244 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7242 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7241 1UF 10% 16V X5R 603-1
C7270 0.001UF 10% 50V X7R-CERM 0402
C7200 1UF 10% 25V X5R 603-1
PP5V_G3H:U7201
R7208 0 5% 1/10W MF-LF 402
PP5V_G3H
P5VP3V3_VREG5V
C7205 10UF 20% 10V X5R 0603-1
5V OUTPUT 100MA MAX OUTPUT
3.3V OUTPUT 10MA MAX OUTPUT
P5VP3V3_VREG3V3
P5VP3V3_VREF2
C7201 0.22UF 10% 25V X5R 402
C7203 2.2UF 20% 10V X5R-CERM 402
GND_5V3V3_AGND
THRESHOLD: 0.6 TO 1.2V
HYSTERESIS: 0.1 TO 0.3V
PP12V_G3H
R7203 511K 1% 1/20W MF 201
R7204 100K 1% 1/20W MF 201
TURN ON: 4.8 TO 7.4V
TURN OFF: 3.0 TO 6.7V
C7285 15UF 20% 16V TANT SM
C7280 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7282 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7281 1UF 10% 16V X5R 603-1
C7283 0.001UF 10% 50V X7R-CERM 0402
VOUT = 5.0V
11A MAX OUTPUT
F = 400 KHZ
PP5V_S4_REG
C7271 0.001UF 10% 50V X7R-CERM 0402
C7250 10UF 20% 6.3V X5R 805
L7220 1.0UH-20A IHLP4040DZ11-SM 152S0525
C7252 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7253 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
C7254 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
NOSTUFF C7255 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
P5VS4_VSW
XW7220 SM
XW7221 SM
XW7222 SM
Q7220 CSD58872Q5D SON5X6
P5VS4_VBST_R
C7224 0.1UF 10% 50V X7R 603-1
R7244 1 5% 1/10W MF-LF 402
R7247 10.5K 1% 1/10W MF-LF 402
R7256 3.09K 1% 1/10W MF-LF 402
NOSTUFF R7299 1 5% 1/10W MF-LF 603
P5VS4_SNUBR
NOSTUFF C7299 0.0033UF 10% 50V X7R-CERM 0402
P5VS4_CSP1_R
SKIP_5V3V3:INAUDIBLE
SKIP_5V3V3:AUDIBLE
R7200 0 5% 1/20W MF 0201
R7201 0 5% 1/20W MF 0201
P5VP3V3_SKIPSEL
CRITICAL U7201 TPS51980 QFN
SKIPSEL1
SKIPSEL2
OCSEL
VBST1
DRVH1
SW1
DRVL1
CSP1
CSN1
MODE
VFB1
COMP1
EN1 (IPU)
PGOOD1
GND
THRM_PAD
EN
VBST2
DRVH2
SW2
DRVL2
CSP2
CSN2
RF
VFB2
COMP2
EN2 (IPU)
PGOOD2
P5VP3V3G3H_REG_EN
P5VS4_VBST
P5VS4_DRVH
P5VS4_LL
P5VS4_DRVL
P5VS4_CSP1
P5VS4_CSN1
P5VS4_VFB1
P5VS4_COMP1
P5VS4_EN1
PM_PGOOD_REG_P5V_S4
C7218 0.15UF 10% 10V X5R 402
R7236 12.1K 1% 1/20W MF 201
C7237 470PF 10% 16V X5R-X7R-CERM 0201
R7237 10K 1% 1/20W MF 201
C7236 470PF 5% 50V NP0-C0G-CERM 0402
P5VS4_COMP1_R
XW7200 SM
R7238 4.02K 1% 1/20W MF 201
C7239 470PF 10% 16V X5R-X7R-CERM 0201
R7239 10K 1% 1/20W MF 201
C7238 0.0015UF 10% 25V X7R-CERM 0402-1
P3V3G3H_COMP2_R
P3V3G3H_EN_SS
C7215 0.0047UF 10% 25V CERM 0402
GND_5V3V3_AGND
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
P3V3G3H_VBST_R
R7263 0 5% 1/16W MF-LF 402
C7264 0.1UF 10% 50V X7R 603-1
CRITICAL Q7260 CSD58872Q5D SON5X6
P3V3G3H_VSW
P3V3G3H_SNUBR
NOSTUFF R7298 10 5% 1/16W MF-LF 603
NOSTUFF C7298 0.001UF 10% 50V X7R-CERM 0402
C7288 0.15UF 10% 10V X5R 402
R7206 249K 1% 1/16W MF-LF 402
R7246 8.25K 1% 1/16W MF-LF 402
R7216 3.32K 1% 1/16W MF-LF 402
P3V3G3H_CSP2_R
VOUT = 3.3V
14A MAX OUTPUT
F = 400 KHZ
PP3V3_G3H
C7290 10UF 20% 6.3V X5R 603
C7272 0.001UF 10% 50V X7R-CERM 0402
L7260 1.0UH-20A IHLP4040DZ11-SM 152S0525
C7292 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7293 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
C7294 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
XW7260 SM
XW7261 SM
XW7262 SM
P3V3G3H_VFB2_R2
P3V3G3H_VFB2_R
R7262 10 5% 1/20W MF 201
R7260 23.2K 1% 1/16W MF-LF 402
R7261 10K 1% 1/16W MF-LF 402
R7221 10K 1% 1/16W MF-LF 402
R7220 40.2K 1% 1/16W MF-LF 402
R7222 10 5% 1/20W MF 201
P5VS4_VFB1_R2
P5VS4_VFB1_R
PP5V_G3H
R7210 100K 5% 1/20W MF 201
Q7210 SSM6N37FEAPE SOT563
P5VS4_EN1
P5VS4_EN_L
PM_EN_REG_P5V_S4
SYNC_MASTER=J64_2C
SYNC_DATE=2014-01-21
PAGE TITLE
VR - 3.3V G3H AND 5V S4
Apple Inc.
DRAWING NUMBER 051-1907
SIZE D
REVISION 4.0.0
BRANCH
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SHEET 55 OF 83
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VDDQ 1.2V S3 Regulator

OC trip point: 13.2 A VDDQ (typical) = $\frac{\text{R7336} * 10e\text{-}6}{8 * \text{Rds(Q7310)}} + \frac{1.08}{\text{L7310} * \text{f(switch)}}$

2 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz

PP12V_G3H_DDR
PP1V2_S3_REG
PP5V_S4
C7302/C7303 are mirrored as a provision for acoustic noise
REG_BOOT_P1V2_S3_RC
REG_BOOT_P1V2_S3
REG_UGATE_P1V2_S3
REG_PHASE_P1V2_S3
REG_LGATE_P1V2_S3
PM_PGOOD_REG_P1V2_S3
REG_P1V2_S3_VDDQSNS
LDO_DDRVTTS0_SNS
REG_P1V2_S3_VTTREF
REG_P1V2_S3_VREF
REG_P1V2_S3_REFIN
REG_P1V2_S3_MODE
REG_P1V2_S3_TRIP
AGND_P1V2_S3
PGND_REG_P1V2_S3
PP0V6_S3_DDRVTT
REG_SNUBBER_P1V2_S3
REG_PHASE_P1V2_S3_L
PP1V2_S3_REG
PM_EN_P0V6_DDRVTT
PM_EN_REG_P1V2_S3
PM_EN_LDO_S3_DDRVTT_R
PM_EN_REG_P1V2_S3_R
REG_P1V2_V5IN

Critical:
Need copper around Q7310 to sink heat

Vout = 1.8V * (Rb / (Ra + Rb))

1.8V S3 REGULATOR

C7351 and C7356 must be mirrored.
PP3V3_G3H
PM_EN_REG_P1V8_S3
PM_PGOOD_REG_P1V8_S3
REG_P1V8_S3_EN
REG_SW_P1V8_S3
REG_FB_P1V8_S3
REG_FB_P1V8_S3_R
PP1V8_S3_REG

Vout = 1.794V
Max Current = 1.8A
Freq = 1 MHz
C7355 and C7357 must be mirrored.

Vout = 0.8V * (1 + Ra / Rb)

SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-23
PAGE TITLE	VR VDDQ S3 / 1.8V S3
Apple Inc.	DRAWING NUMBER 051-1907 · SIZE D
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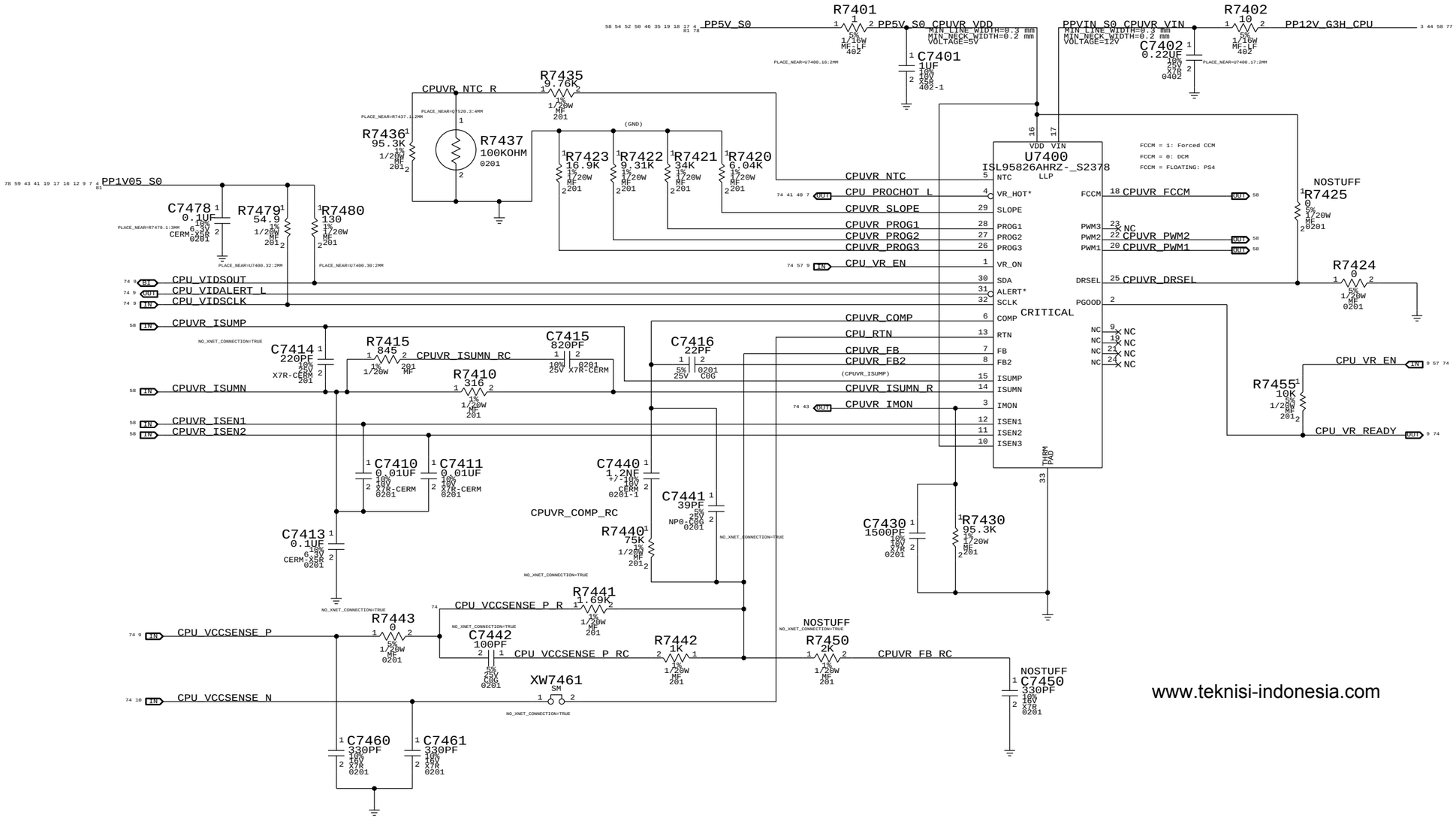

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-17

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

BRANCH

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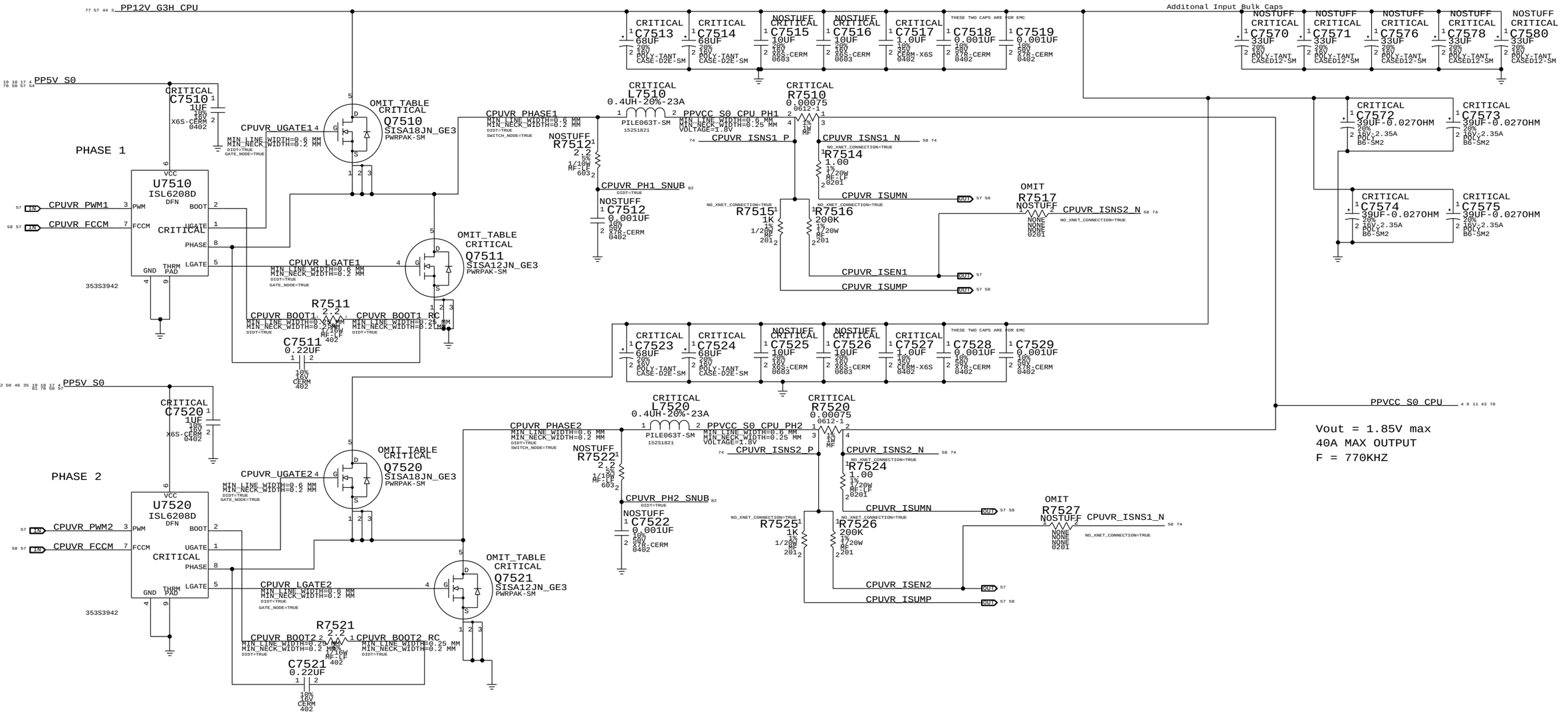

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7510,Q7520	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7511,Q7521	CRITICAL	VCORE_FET:VSHY
376S00036	2	MOSFET,N-CH,30V,52A,5.9M,3.3X3.3 DFN8	Q7510,Q7520	CRITICAL	VCORE_FET:ONSEMI
376S00037	2	MOSFET,N-CH,30V,64A,3.3M,3.3X3.3 DFN8	Q7511,Q7521	CRITICAL	VCORE_FET:ONSEMI

685-00028	1	COMP SET,VCORE FETS,VISHAY	VSET1	CRITICAL	VCORE_FET:ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00029	685-00028	VCORE_FET:ALTERNATES	VSET1	ALTERNATE

SYNC_MASTER=J41 SYNC_DATE=2014-01-17

PAGE TITLE
CPU VR12.6 VCC POWER STAGE

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D
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BRANCH
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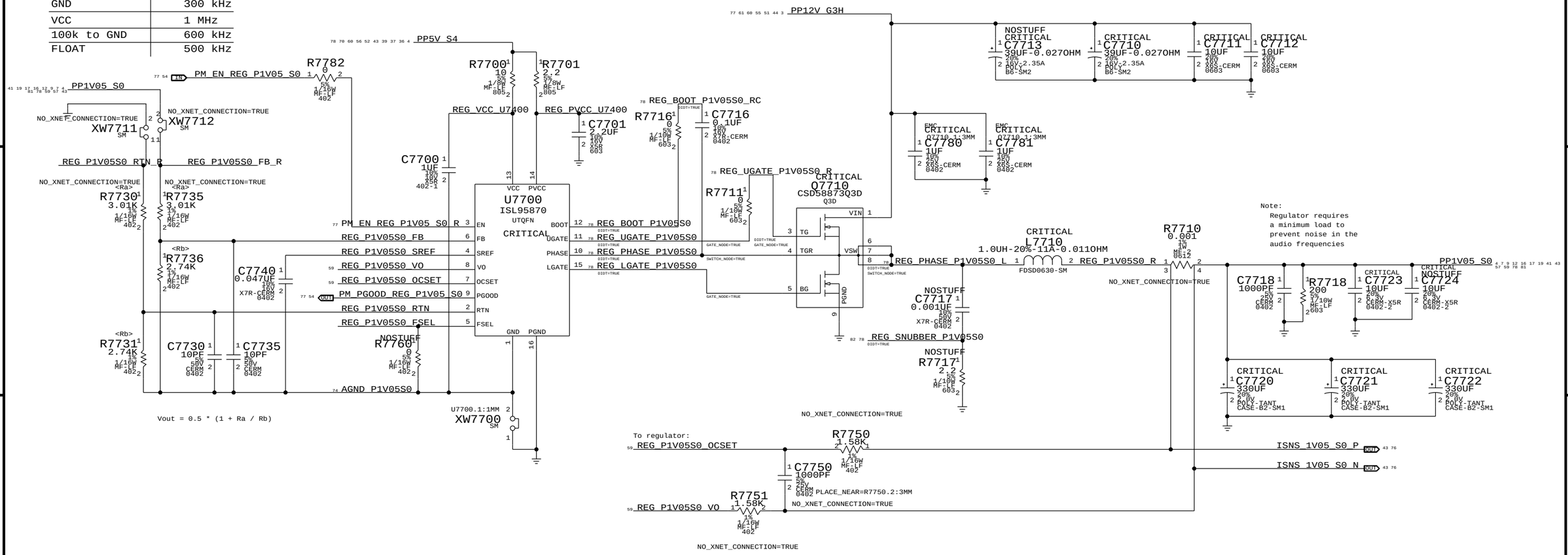
PCH (1.05V) S0 REGULATOR

Switching freq: 500 kHz OC trip point: 12.4 A = $\frac{R7750 * 8.5\ E\text{-}6}{R7710}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



SYNC_MASTER=J64_2C	SYNC_DATE=2014-02-04
PAGE TITLE	VR 1V05 S0
Apple Inc.	DRAWING NUMBER 051-1907 SIZE D
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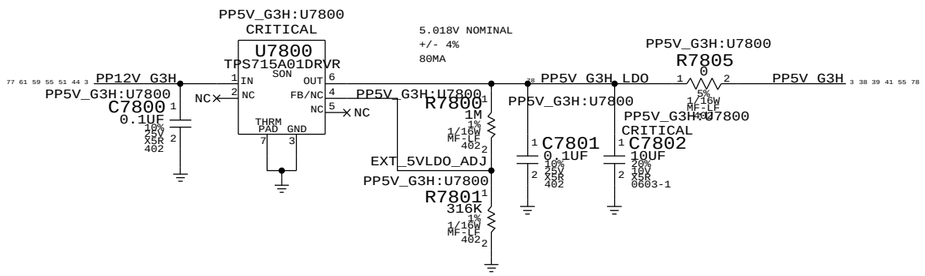
PP5V_G3H - LDO

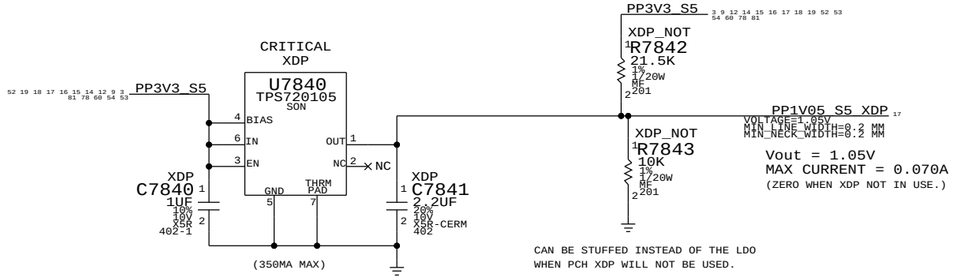
(PLAN B)

MAX DROPOUT 1120MV @ 80MA
OC LIMIT = 160 TO 1110 MA
0.62W @ TA = 85C.

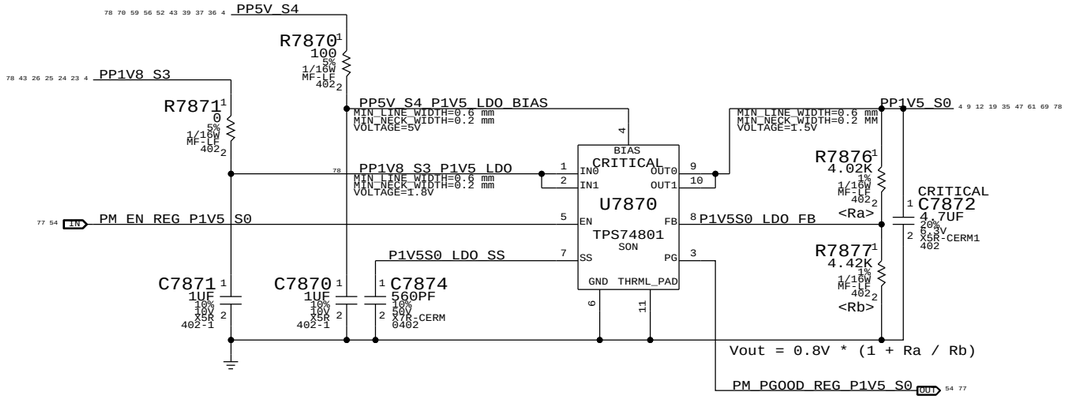


1.05V S5 XDP LDO

PANTHER-POINT REQUIRES JTAG PULL-UPS TO BE POWERED AT 1.05V WHEN SUS SUSPEND WELL IS ACTIVE.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 @ 0.5A, 0.8A PEAK



SYNC_MASTER=J50I	SYNC_DATE=2014-01-17
PAGE TITLE	VR - MISC
Apple Inc.	DRAWING NUMBER 051-1907 · SIZE D
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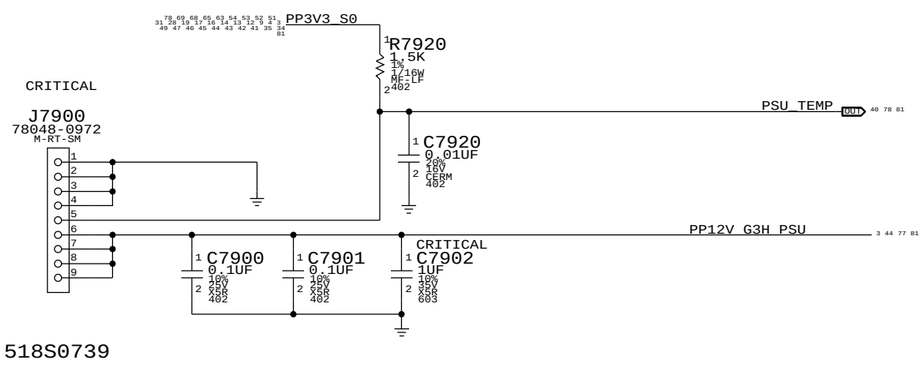
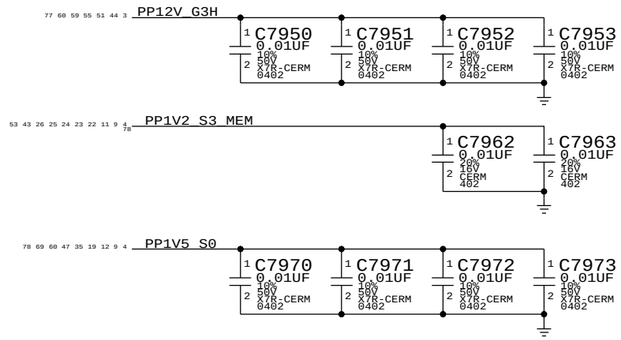
	BRANCH
	PAGE 78 OF 500
	SHEET 60 OF 83



PLACE CAPS AS CLOSE TO J7900 AS POSSIBLE.
BEST IF VIAS ARE AFTER THE CAPS.

SPRINKLE THESE CAPS SOMEWHAT EVENLY AROUND THE PLANES AND ROUTES FOR THESE RAILS.



SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE: PSU CONNECTOR, MISC CAPS

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

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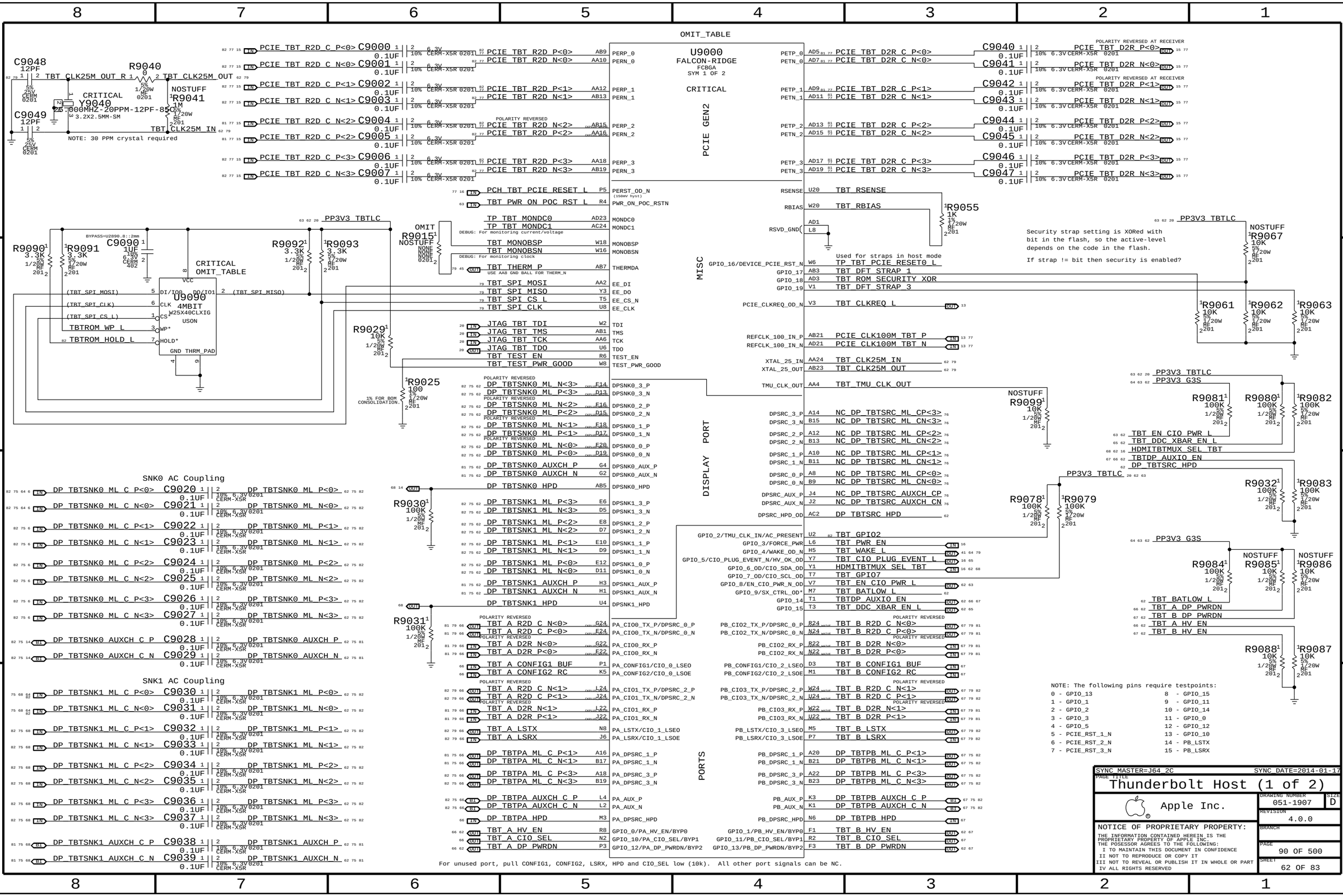
OMIT_TABLE
U9000
FALCON-RIDGE
FCBGA
SYM 1 OF 2
CRITICAL
PCIE GEN2
MISC
DISPLAY PORT
PORTS
C9048 12PF
R9040 0
TBT_CLK25M_OUT_R
TBT_CLK25M_OUT
NOSTUFF R9041 1M
CRITICAL Y9040 25.000MHZ-20PPM-12PF-85C
C9049 12PF
TBT_CLK25M_IN
NOTE: 30 PPM crystal required
PCIE_TBT_R2D_C_P<0> C9000 0.1UF
PCIE_TBT_R2D_C_N<0> C9001 0.1UF
PCIE_TBT_R2D_C_P<1> C9002 0.1UF
PCIE_TBT_R2D_C_N<1> C9003 0.1UF
PCIE_TBT_R2D_C_N<2> C9004 0.1UF
PCIE_TBT_R2D_C_P<2> C9005 0.1UF
PCIE_TBT_R2D_C_P<3> C9006 0.1UF
PCIE_TBT_R2D_C_N<3> C9007 0.1UF
POLARITY REVERSED
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PERP_0 AB9
PERN_0 AA10
PERP_1 AA12
PERN_1 AB13
PERP_2 AB15
PERN_2 AA16
PERP_3 AA18
PERN_3 AB19
PETP_0 AD5
PETN_0 AD7
PETP_1 AD9
PETN_1 AD11
PETP_2 AD13
PETN_2 AD15
PETP_3 AD17
PETN_3 AD19
POLARITY REVERSED AT RECEIVER
PCIE_TBT_D2R_C_P<0> C9040 0.1UF
PCIE_TBT_D2R_C_N<0> C9041 0.1UF
PCIE_TBT_D2R_C_P<1> C9042 0.1UF
PCIE_TBT_D2R_C_N<1> C9043 0.1UF
PCIE_TBT_D2R_C_P<2> C9044 0.1UF
PCIE_TBT_D2R_C_N<2> C9045 0.1UF
PCIE_TBT_D2R_C_P<3> C9046 0.1UF
PCIE_TBT_D2R_C_N<3> C9047 0.1UF
PCH_TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
PERST_OD_N (150mV Hyst)
PWR_ON_POC_RSTN
PP3V3_TBTLC
R9090 3.3K
R9091 3.3K
C9090 1UF
R9092 3.3K
R9093 3.3K
BYPASS=U2890.B::2mm
CRITICAL OMIT_TABLE
U9090 4MBIT W25X40CLXIG USON
(TBT_SPI_MOSI)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
OMIT R9015 NOSTUFF
TP_TBT_MONDC0
TP_TBT_MONDC1
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TBT_THERM_P
USE AA8 GND BALL FOR THERM_N
THERMDA
TBT_SPI_MOSI AA2
TBT_SPI_MISO Y3
TBT_SPI_CS_L T5
TBT_SPI_CLK U8
MONDC0 AD23
MONDC1 AC24
MONOBSP W18
MONOBSN W16
EE_DI
EE_DO
EE_CS_N
EE_CLK
R9029 10K
JTAG_TBT_TDI W2
JTAG_TBT_TMS AB1
JTAG_TBT_TCK AA6
JTAG_TBT_TDO U6
TBT_TEST_EN R6
TBT_TEST_PWR_GOOD W8
TDI
TMS
TCK
TDO
TEST_EN
TEST_PWR_GOOD
R9025 100 1% 1/20W MF 201
1% FOR BOM CONSOLIDATION.
RSENSE U20 TBT_RSENSE
RBIAS W20 TBT_RBIAS
R9055 1K 1% 1/20W MF 201
RSVD_GND AD1 L8
GPIO_16/DEVICE_PCIE_RST_N W6 TP_TBT_PCIE_RESET0_L
Used for straps in host mode
GPIO_17 AB3 TBT_DFT_STRAP_1
GPIO_18 AD3 TBT_ROM_SECURITY_XOR
GPIO_19 V1 TBT_DFT_STRAP_3
PCIE_CLKREQ_OD_N V3 TBT_CLKREQ_L
REFCLK_100_IN_P AB21 PCIE_CLK100M_TBT_P
REFCLK_100_IN_N AD21 PCIE_CLK100M_TBT_N
XTAL_25_IN AA24 TBT_CLK25M_IN
XTAL_25_OUT AB23 TBT_CLK25M_OUT
TMU_CLK_OUT AA4 TBT_TMU_CLK_OUT
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
PP3V3_TBTLC
NOSTUFF R9067 10K
R9061 10K
R9062 10K
R9063 10K
NOSTUFF R9099 10K
PP3V3_TBTLC
PP3V3_G3S
R9081 100K
R9080 100K
R9082 100K
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
PP3V3_TBTLC
R9078 100K
R9079 100K
R9032 100K
R9083 100K
PP3V3_G3S
R9084 100K
NOSTUFF R9085 10K
NOSTUFF R9086 10K
TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R9088 10K
R9087 10K
DPSRC_3_P A14 NC_DP_TBTSRC_ML_CP<3>
DPSRC_3_N B15 NC_DP_TBTSRC_ML_CN<3>
DPSRC_2_P A12 NC_DP_TBTSRC_ML_CP<2>
DPSRC_2_N B13 NC_DP_TBTSRC_ML_CN<2>
DPSRC_1_P A10 NC_DP_TBTSRC_ML_CP<1>
DPSRC_1_N B11 NC_DP_TBTSRC_ML_CN<1>
DPSRC_0_P A8 NC_DP_TBTSRC_ML_CP<0>
DPSRC_0_N B9 NC_DP_TBTSRC_ML_CN<0>
DPSRC_AUX_P J4 NC_DP_TBTSRC_AUXCH_CP
DPSRC_AUX_N J2 NC_DP_TBTSRC_AUXCH_CN
DPSRC_HPD_OD AC2 DP_TBTSRC_HPD
SNK0 AC Coupling
DP_TBTSNK0_ML_C_P<0> C9020 0.1UF
DP_TBTSNK0_ML_C_N<0> C9021 0.1UF
DP_TBTSNK0_ML_C_P<1> C9022 0.1UF
DP_TBTSNK0_ML_C_N<1> C9023 0.1UF
DP_TBTSNK0_ML_C_P<2> C9024 0.1UF
DP_TBTSNK0_ML_C_N<2> C9025 0.1UF
DP_TBTSNK0_ML_C_P<3> C9026 0.1UF
DP_TBTSNK0_ML_C_N<3> C9027 0.1UF
DP_TBTSNK0_AUXCH_C_P C9028 0.1UF
DP_TBTSNK0_AUXCH_C_N C9029 0.1UF
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
SNK1 AC Coupling
DP_TBTSNK1_ML_C_P<0> C9030 0.1UF
DP_TBTSNK1_ML_C_N<0> C9031 0.1UF
DP_TBTSNK1_ML_C_P<1> C9032 0.1UF
DP_TBTSNK1_ML_C_N<1> C9033 0.1UF
DP_TBTSNK1_ML_C_P<2> C9034 0.1UF
DP_TBTSNK1_ML_C_N<2> C9035 0.1UF
DP_TBTSNK1_ML_C_P<3> C9036 0.1UF
DP_TBTSNK1_ML_C_N<3> C9037 0.1UF
DP_TBTSNK1_AUXCH_C_P C9038 0.1UF
DP_TBTSNK1_AUXCH_C_N C9039 0.1UF
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK0_ML_P_N<3> E14
DP_TBTSNK0_ML_P_P<3> D13
DP_TBTSNK0_ML_P_N<2> E16
DP_TBTSNK0_ML_P_P<2> D15
DP_TBTSNK0_ML_P_N<1> E18
DP_TBTSNK0_ML_P_P<1> D17
DP_TBTSNK0_ML_P_N<0> E20
DP_TBTSNK0_ML_P_P<0> D19
DP_TBTSNK0_AUXCH_P G4
DP_TBTSNK0_AUXCH_N G2
DP_TBTSNK0_HPD AB5
DP_TBTSNK1_ML_P_P<3> E6
DP_TBTSNK1_ML_P_N<3> D5
DP_TBTSNK1_ML_P_P<2> E8
DP_TBTSNK1_ML_P_N<2> D7
DP_TBTSNK1_ML_P_P<1> E10
DP_TBTSNK1_ML_P_N<1> D9
DP_TBTSNK1_ML_P_P<0> E12
DP_TBTSNK1_ML_P_N<0> D11
DP_TBTSNK1_AUXCH_P H3
DP_TBTSNK1_AUXCH_N H1
DP_TBTSNK1_HPD U4
R9030 100K
R9031 100K
TBT_A_R2D_C_N<0> G24
TBT_A_R2D_C_P<0> F24
TBT_A_D2R_N<0> G22
TBT_A_D2R_P<0> F22
TBT_A_CONFIG1_BUF P1
TBT_A_CONFIG2_RC K5
TBT_A_R2D_C_N<1> L24
TBT_A_R2D_C_P<1> J24
TBT_A_D2R_N<1> L22
TBT_A_D2R_P<1> J22
TBT_A_LSTX N8
TBT_A_LSRX J6
DP_TBTPA_ML_C_P<1> A16
DP_TBTPA_ML_C_N<1> B17
DP_TBTPA_ML_C_P<3> A18
DP_TBTPA_ML_C_N<3> B19
DP_TBTPA_AUXCH_C_P L4
DP_TBTPA_AUXCH_C_N L2
DP_TBTPA_HPD M3
TBT_A_HV_EN R8
TBT_A_CIO_SEL N2
TBT_A_DP_PWRDN P3
DPSNK0_3_P
DPSNK0_3_N
DPSNK0_2_P
DPSNK0_2_N
DPSNK0_1_P
DPSNK0_1_N
DPSNK0_0_P
DPSNK0_0_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
DPSNK1_3_P
DPSNK1_3_N
DPSNK1_2_P
DPSNK1_2_N
DPSNK1_1_P
DPSNK1_1_N
DPSNK1_0_P
DPSNK1_0_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
PA_CIO0_TX_P/DPSRC_0_P
PA_CIO0_TX_N/DPSRC_0_N
PA_CIO0_RX_P
PA_CIO0_RX_N
PA_CONFIG1/CIO_0_LSEO
PA_CONFIG2/CIO_0_LSOE
PA_CIO1_TX_P/DPSRC_2_P
PA_CIO1_TX_N/DPSRC_2_N
PA_CIO1_RX_P
PA_CIO1_RX_N
PA_LSTX/CIO_1_LSEO
PA_LSRX/CIO_1_LSOE
PA_DPSRC_1_P
PA_DPSRC_1_N
PA_DPSRC_3_P
PA_DPSRC_3_N
PA_AUX_P
PA_AUX_N
PA_DPSRC_HPD
GPIO_0/PA_HV_EN/BYP0
GPIO_10/PA_CIO_SEL/BYP1
GPIO_12/PA_DP_PWRDN/BYP2
GPIO_2/TMU_CLK_IN/AC_PRESENT
GPIO_3/FORCE_PWR
GPIO_4/WAKE_OD_N
GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD
GPIO_6_OD/CIO_SDA_OD
GPIO_7_OD/CIO_SCL_OD
GPIO_8/EN_CIO_PWR_N_OD
GPIO_9/SX_CTRL_OD*
GPIO_14
GPIO_15
PB_CIO2_TX_P/DPSRC_0_P
PB_CIO2_TX_N/DPSRC_0_N
PB_CIO2_RX_P
PB_CIO2_RX_N
PB_CONFIG1/CIO_2_LSEO
PB_CONFIG2/CIO_2_LSOE
PB_CIO3_TX_P/DPSRC_2_P
PB_CIO3_TX_N/DPSRC_2_N
PB_CIO3_RX_P
PB_CIO3_RX_N
PB_LSTX/CIO_3_LSEO
PB_LSRX/CIO_3_LSOE
PB_DPSRC_1_P
PB_DPSRC_1_N
PB_DPSRC_3_P
PB_DPSRC_3_N
PB_AUX_P
PB_AUX_N
PB_DPSRC_HPD
GPIO_1/PB_HV_EN/BYP0
GPIO_11/PB_CIO_SEL/BYP1
GPIO_13/PB_DP_PWRDN/BYP2
TBT_GPIO2
TBT_PWR_EN
TBT_WAKE_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
TBT_BATLOW_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
TBT_B_R2D_C_N<0>
TBT_B_R2D_C_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_P<0>
TBT_B_CONFIG1_BUF
TBT_B_CONFIG2_RC
TBT_B_R2D_C_N<1>
TBT_B_R2D_C_P<1>
TBT_B_D2R_N<1>
TBT_B_D2R_P<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_C_N
DP_TBTPB_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J64_2C
SYNC_DATE=2014-01-17
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER 051-1907
SIZE D
REVISION 4.0.0
BRANCH
PAGE 90 OF 500
SHEET 62 OF 83
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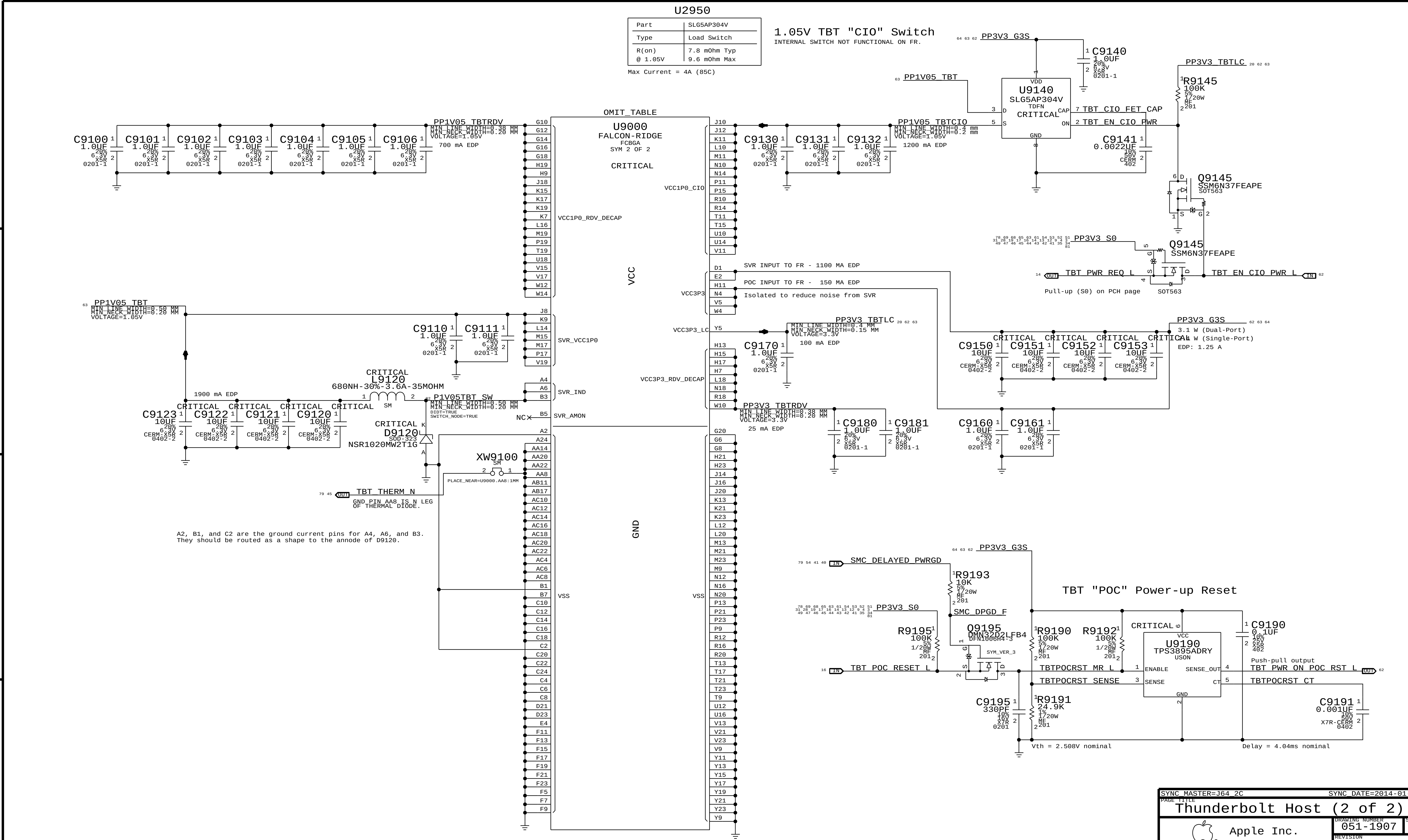


U2950
Part | SLG5AP304V
Type | Load Switch
R(on) @ 1.05V | 7.8 mOhm Typ / 9.6 mOhm Max
Max Current = 4A (85C)
1.05V TBT "CIO" Switch
INTERNAL SWITCH NOT FUNCTIONAL ON FR.
PP3V3_G3S
C9140 1.0UF 20% 6.3V X5R 0201-1
PP3V3_TBTLC
PP1V05_TBT
U9140 SLG5AP304V TDFN CRITICAL
VDD
CAP
ON
GND
TBT_CIO_FET_CAP
TBT_EN_CIO_PWR
R9145 100K 5% 1/20W MF 201
C9141 0.0022UF 10% 50V CERM 402
Q9145 SSM6N37FEAPE SOT563
PP3V3_S0
TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L
Pull-up (S0) on PCH page
OMIT_TABLE
U9000 FALCON-RIDGE FCBGA SYM 2 OF 2 CRITICAL
PP1V05_TBTRDV
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.05V
700 mA EDP
C9100 1.0UF 20% 6.3V X5R 0201-1
C9101 1.0UF 20% 6.3V X5R 0201-1
C9102 1.0UF 20% 6.3V X5R 0201-1
C9103 1.0UF 20% 6.3V X5R 0201-1
C9104 1.0UF 20% 6.3V X5R 0201-1
C9105 1.0UF 20% 6.3V X5R 0201-1
C9106 1.0UF 20% 6.3V X5R 0201-1
VCC1P0_RDV_DECAP
VCC1P0_CIO
PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
1200 mA EDP
C9130 1.0UF 20% 6.3V X5R 0201-1
C9131 1.0UF 20% 6.3V X5R 0201-1
C9132 1.0UF 20% 6.3V X5R 0201-1
VCC
SVR INPUT TO FR - 1100 MA EDP
POC INPUT TO FR - 150 MA EDP
Isolated to reduce noise from SVR
VCC3P3
VCC3P3_LC
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=3.3V
100 mA EDP
C9170 1.0UF 20% 6.3V X5R 0201-1
PP3V3_G3S
3.1 W (Dual-Port)
2.4 W (Single-Port)
EDP: 1.25 A
C9150 10UF 20% 6.3V CERM-X5R 0402-2
C9151 10UF 20% 6.3V CERM-X5R 0402-2
C9152 10UF 20% 6.3V CERM-X5R 0402-2
C9153 10UF 20% 6.3V CERM-X5R 0402-2
VCC3P3_RDV_DECAP
PP3V3_TBTRDV
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
25 mA EDP
C9180 1.0UF 20% 6.3V X5R 0201-1
C9181 1.0UF 20% 6.3V X5R 0201-1
C9160 1.0UF 20% 6.3V X5R 0201-1
C9161 1.0UF 20% 6.3V X5R 0201-1
PP1V05_TBT
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.05V
C9110 1.0UF 20% 6.3V X5R 0201-1
C9111 1.0UF 20% 6.3V X5R 0201-1
SVR_VCC1P0
CRITICAL
L9120 680NH-30%-3.6A-35MOHM SM
P1V05TBT_SW
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
DIDT=TRUE
SWITCH_NODE=TRUE
SVR_IND
SVR_AMON
NC
1900 mA EDP
C9123 10UF 20% 6.3V CERM-X5R 0402-2
C9122 10UF 20% 6.3V CERM-X5R 0402-2
C9121 10UF 20% 6.3V CERM-X5R 0402-2
C9120 10UF 20% 6.3V CERM-X5R 0402-2
CRITICAL D9120 SOD-323 NSR1020MW2T1G
XW9100 SM
PLACE_NEAR=U9000.AA8:1MM
TBT_THERM_N
GND PIN AA8 IS N LEG OF THERMAL DIODE.
A2, B1, and C2 are the ground current pins for A4, A6, and B3. They should be routed as a shape to the annode of D9120.
GND
VSS
TBT "POC" Power-up Reset
PP3V3_G3S
SMC_DELAYED_PWRGD
R9193 10K 5% 1/20W MF 201
PP3V3_S0
SMC_DPGD_F
R9195 100K 5% 1/20W MF 201
Q9195 DMN32D2LFB4 DFN1006H4-3
SYM_VER_3
TBT_POC_RESET_L
R9190 100K 5% 1/20W MF 201
R9192 100K 5% 1/20W MF 201
CRITICAL
U9190 TPS3895ADRY USON
VCC
ENABLE
SENSE
SENSE_OUT
CT
GND
C9190 0.1UF 10% 25V X5R 402
Push-pull output
TBT_PWR_ON_POC_RST_L
TBTPOCRST_MR_L
TBTPOCRST_SENSE
TBTPOCRST_CT
C9195 330PF 10% 16V X7R 0201
R9191 24.9K 1% 1/20W MF 201
C9191 0.001UF 10% 50V X7R-CERM 0402
Vth = 2.508V nominal
Delay = 4.04ms nominal

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-17

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

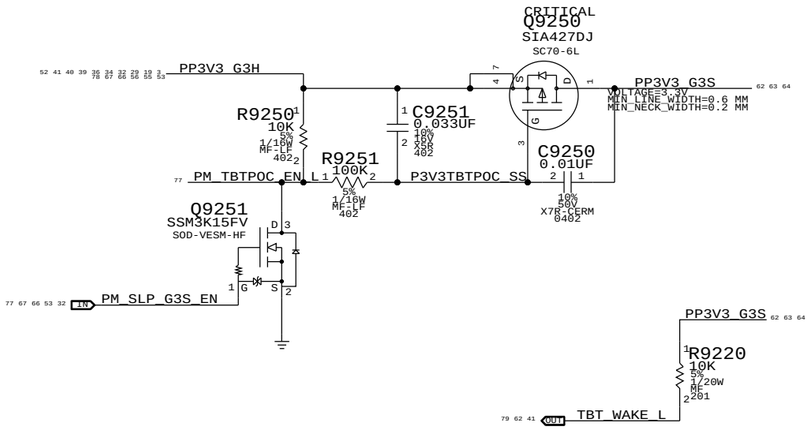
DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

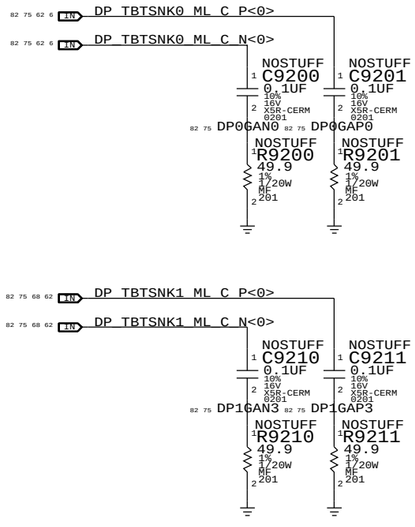
BRANCH

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

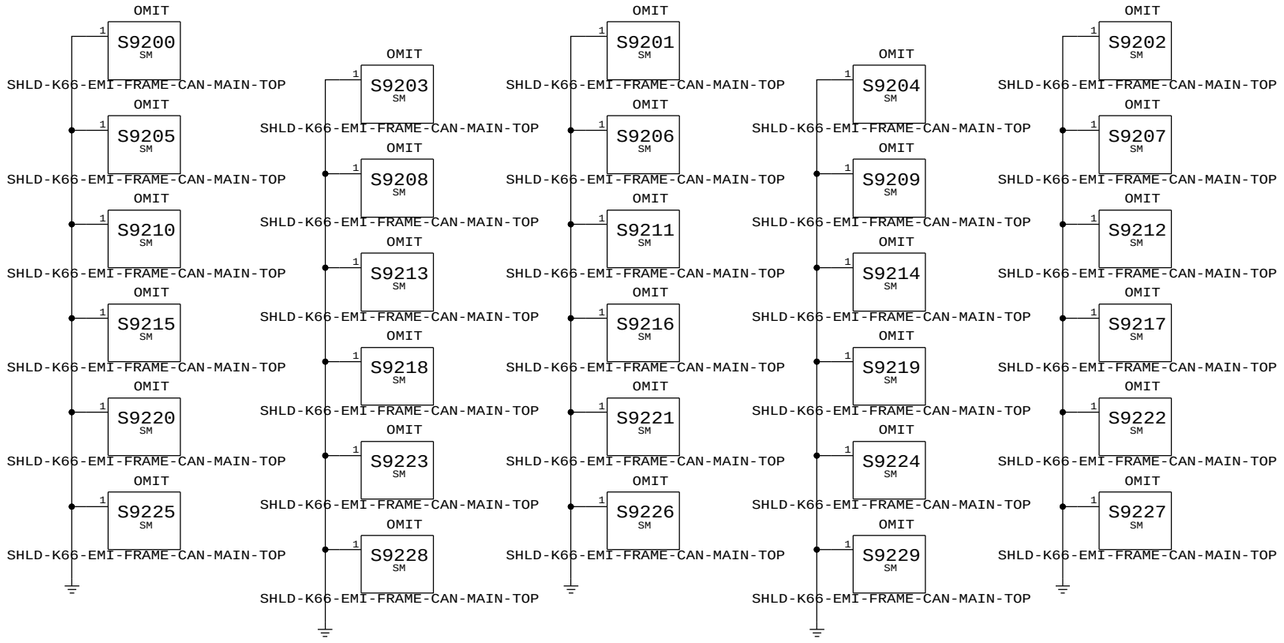
3.3V TBT POC FET



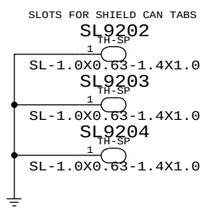
PROBE POINTS.



EMI CAN PADS, SLOTS



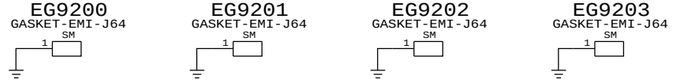
SLOTS FOR SHIELD CAN TABS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-00164	1	FRAME,EMI SHIELD,MLB,J64	SH9200	CRITICAL	?

teknisi-indonesia

EMI GASKET BUMPERS



725-00035

SYNC_MASTER=J64_2C SYNC_DATE=2013-08-14

PAGE TITLE: TBT POWER SUPPORT

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

BRANCH:

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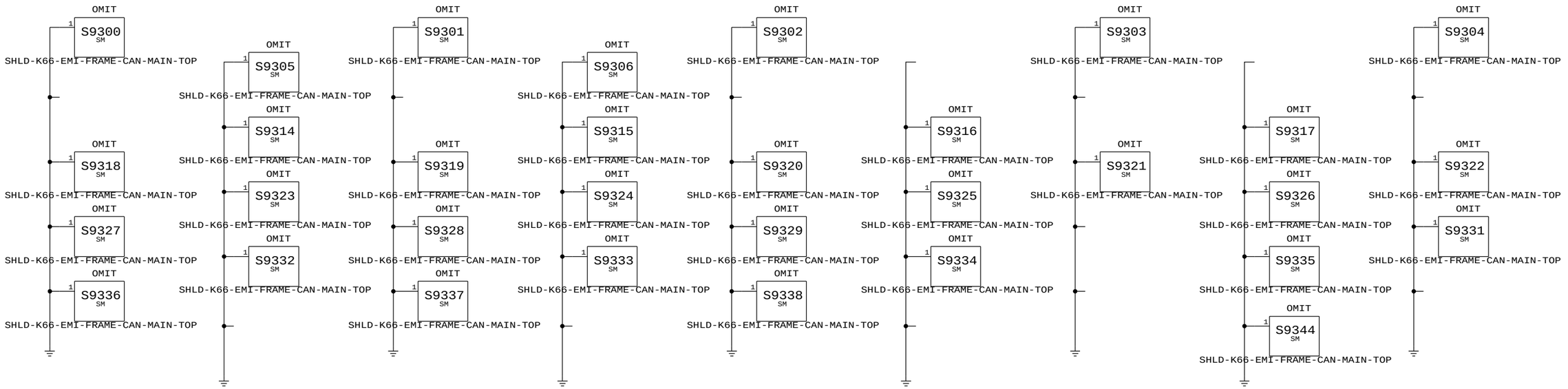


DDC Crossbar

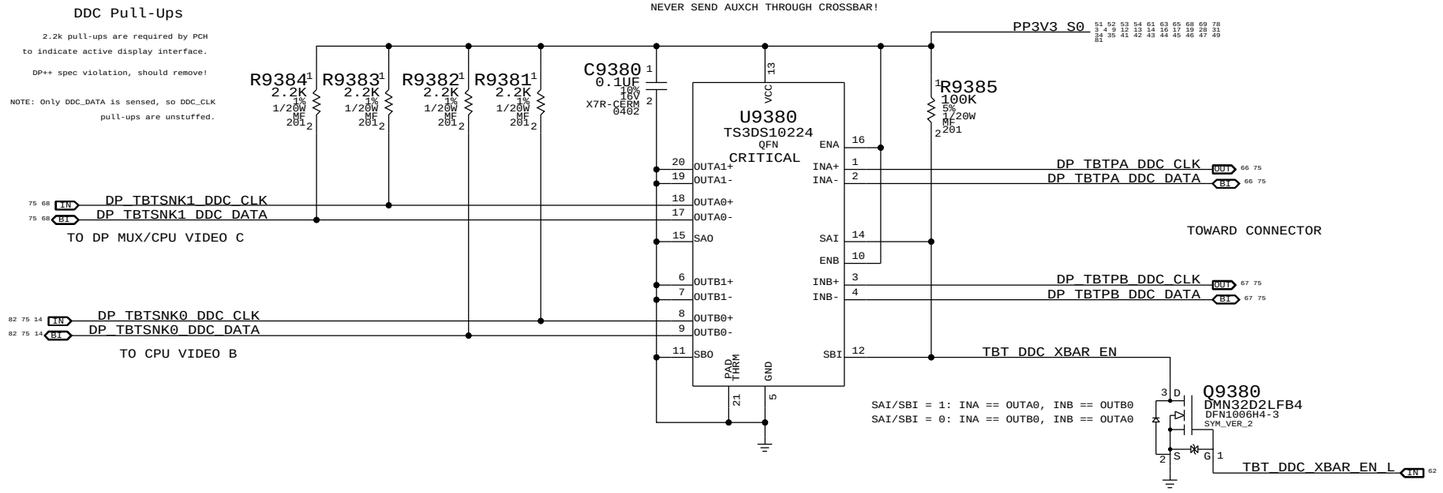
Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

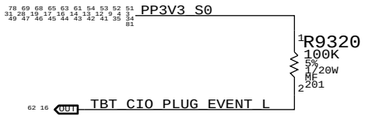
DDC Pull-Ups

2.2k pull-ups are required by PCH to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK pull-ups are unstuffed.





SYNC_MASTER=J64_2C SYNC_DATE=2014-01-14

PAGE TITLE: TBT MISC

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D
REVISION: 4.0.0
BRANCH:
PAGE: 93 OF 500
SHEET: 65 OF 83

V3P3 must be S4 to support
wake from Thunderbolt devices.

3.3V/HV Power MUX

PP3V3_G3H

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

TBT SPEC IS 12W MIN.
OVER 12V +/- 5%.

C9487 CRITICAL 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C9480 CRITICAL 22UF 20% 6.3V X5R-CERM 0603
C9481 0.1UF 10% 25V X5R CERM-X5R 0201

18V Max
PP12V_G3H_TBT
C9484 CRITICAL 4.7UF 10% 25V X5R-CERM 0603
C9482 0.1UF 10% 25V X5R 402

U9480 CRITICAL
CD3211A1RGP
QFN

Pin	Name
19, 20	V3P3
6, 7	VHV
16	ENHVU
5	EN
11	HV_EN
17	S0
18	V3P3OUT
12, 14	OUT
4	FAULTZ
8	ISET_V3P3
10	ISET_S0
9	ISET_S3
GND, THRM PAD	1, 2, 3, 13, 15, 21

PM_SLP_G3S_EN
TBT_A_HV_EN
PM_SLP_S3_L

PP3V3_SW_TBT_A_PWR
PPHV_SW_TBT_A_PWR

C9485 0.1UF 10% 6.3V CERM-X5R 0201
C9486 CRITICAL 10UF 20% 6.3V CERM-X5R 0402-2
C9483 0.1UF 10% 25V X5R 402

TBT_A_PWRSW_ISET_V3P3
TBT_A_PWRSW_ISET_S0
TBT_A_PWRSW_ISET_S3

R9480 17.8K 1% 1/20W MF 201 <RHVS3>
R9481 17.8K 1% 1/20W MF 201 <RHVS0>
R9482 36.5K 1% 1/20W MF 201 <RV3P3>

TBT_A_PWRSW_ISET_S3_R
TBT_A_PWRSW_ISET_S0_R

R9483 17.8K 1% 1/20W MF 201
R9484 17.8K 1% 1/20W MF 201

ILIM = 40000 / RISET

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBT_A_PWR (NO LANE REVERSALS ALLOWED.)

C9400 0.01UF 10% 50V X7R-CERM 0402
R9401 12 5% 1/20W MF 201
C9401 0.01UF 10% 25V X5R-CERM 0201

FR SIDE

PP3V3_SW_TBT_A_PWR

C9460 0.01UF 10% 10V X5R-CERM 0201
C9461 0.1UF 10% 6.3V CERM-X5R 0201

CONN SIDE

AUXIO_EN = H ENABLE THE TB MUX
NOTE: A SINGLE SIGNAL TO
ENABLE TBMUX IN 6 5024.

SIGNAL_MODEL=TBT_MUX_5024

U9460 CRITICAL
CBTL05024
HVQFN

TBT_RX1
TBT_A_D2R_N<1> — C9476 0.47UF 20% 4V CERM-X5R-1 201 — TBT_A_D2R_C_N<1>
TBT_A_D2R_P<1> — C9477 0.47UF 20% 4V CERM-X5R-1 201 — TBT_A_D2R_C_P<1>

DP_AUX
DP_TBTPA_AUXCH_C_N — C9466 0.1UF 10% 6.3V CERM-X5R 0201 — DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_C_P — C9467 0.1UF 10% 6.3V CERM-X5R 0201 — DP_TBTPA_AUXCH_P

DDC
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK

TBT_A_CONFIG1_BUF

DP<1>
DP_TBTPA_ML_C_P<1> — C9468 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_P<1>
DP_TBTPA_ML_C_N<1> — C9469 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_N<1>

TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD

U9460 pin	Name	Connects to
7	TB-	TBT_A_D2R_C_N<1>
8	TB+	TBT_A_D2R_C_P<1>
1	AUX-(100K PU)	DP_TBTPA_AUXCH_N
2	AUX+(100K PD)	DP_TBTPA_AUXCH_P
4	DDC_DAT	DP_TBTPA_DDC_DATA
5	DDC_CLK	DP_TBTPA_DDC_CLK
16	CA_DETOUT	TBT_A_CONFIG1_BUF
11	DP+	DP_TBTPA_ML_P<1>
10	DP-	DP_TBTPA_ML_N<1>
14	LSTX(10K PU)	TBT_A_LSTX
13	LSRX(1M PD)	TBT_A_LSRX
12	HPDOUT	DP_TBTPA_HPD
15	TB_ENA	TBT_A_CIO_SEL
24	AUXIO_EN	TBTDP_AUXIO_EN
6	DP_PD	TBT_A_DP_PWRDN
23	AUXIO-	TBT_A_D2R1_AUXDDC_N
22	AUXIO+	TBT_A_D2R1_AUXDDC_P
18	CA_DET	TBT_A_CONFIG1_RC
19	DPMLO+	DP_A_LSX_ML_P<1>
20	DPMLO-	DP_A_LSX_ML_N<1>
17	HPD	TBT_A_HPD

TBT: LSX_R2P/P2R (P/N)

DP_PD	DPMLO+/-
0	DP+,DP-
1	LSTX,LSRX

TB_ENA	CA_DET	AUXIO+/-
1	X	TB+/-
0	0	AUX+/-
0	1	DDC_CLK/_DAT

THUNDERBOLT CONNECTOR A
BACK WALL

RID = 0X0

TBT_TX0
DP_0

TBT_A_CONN_1_C
C9405 0.01UF 10% 25V X5R-CERM 0201 (0-20V)
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
TBT_A_CONN_7_C
C9406 0.01UF 10% 25V X5R-CERM 0201 (0-20V)

C9470 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<0>
C9471 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201

TBT_LSX
DP_1

DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

TBT_TX1
DP_2

TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1

C9472 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<1>
C9473 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_N<1>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection
on AC-coupled signals.

TBT_RX0
C9474 0.47UF 20% 4V CERM-X5R-1 201 — TBT_A_D2R_C_P<0>
C9475 0.47UF 20% 4V CERM-X5R-1 201 — TBT_A_D2R_C_N<0>
R9494 1K 5% 1/20W MF 201
R9495 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE

DP_3
C9478 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_P<3>
C9479 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_N<3>
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201
TBT: Unused

TBT_RX1/DP_AUX
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N

TBT_CFG
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R 0201
C9495 330PF 10% 16V X7R 0201
R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

J9400
MINIDSPLYPRT-PL-J40
F-RT-TH-1
CRITICAL

BOT ROW TH PINS		TOP ROW SM PINS
2	DP_HPD	1 GND
4	CONFIG1	3 ML_LANE0P
6	CONFIG2	5 ML_LANE0N
8	GND	7 GND
10	ML_LANE3P	9 ML_LANE1P
12	ML_LANE3N	11 ML_LANE1N
14	GND	13 GND
16	AUX_CHP	15 ML_LANE2P
18	AUX_CHN	17 ML_LANE2N
20	DP_PWR	19 RETURN

SHIELD PINS: 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21

514-0800

HPD	CFG1	CFG2	MODE	DIFF PAIRS MAPPING:					
0	0	0	NO_CABLE						
0	0	1	TBT	TX0	LSTX/LSRX	TX1		RX1	RX0
1	0	0	DP	DP_0	DP_1	DP_2	DP_3	DP_AUX	
1	1	0	DP_ADAPTER	TD2	TD1	TD0	TD_CLK	DDC_CLK/DDC_DAT	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-2198	12	SOLDER PREFORM 0201	SF9400,SF9401,SF9402,SF9403,SF9404,SF9405,SF9406,SF9407,SF9408,SF9409,SF9410,SF9411	CRITICAL	?

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-20

PAGE TITLE: TBT CONNECTOR A

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D
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V3P3 must be S4 to support
wake from Thunderbolt devices.

3.3V/HV Power MUX

PP3V3_G3H

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

TBT SPEC IS 12W MIN.
OVER 12V +/- 5%.

CRITICAL C9587 100UF 20% 6.3V POLY_TANT CASE-B2-SM; C9580 22UF 20% 25V X5R-CERM 0603; C9581 0.1UF 10% 25V X5R-CERM 0201

18V Max PP12V_G3H_TBT

CRITICAL C9584 4.7UF 10% 25V X5R-CERM 0603; C9582 0.1UF 10% 25V X5R 402

CRITICAL U9580 CD3211A1RGP QFN

19	V3P3	V3P3OUT	18
20			
6	VHV	OUT	14
7			
16	ENHVU	FAULTZ	4
5	EN	ISET_V3P3	8
11	HV_EN	ISET_S0	10
17	S0	ISET_S3	9
	GND	THRM PAD	

PP3V3_SW_TBT_B_PWR 67 78

PPHV_SW_TBT_B_PWR 78

CRITICAL C9585 0.1UF 10% 6.3V CERM-X5R 0201; C9586 10UF 20% 6.3V CERM-X5R 0402-2; C9583 0.1UF 10% 25V X5R 402

PM_SLP_G3S_EN 77 66 64 53 32 (IN)

TBT_B_HV_EN 62 (IN)

PM_SLP_S3_L 77 70 69 66 54 44 40 29 14 (IN)

TBT_B_PWRSW_ISET_V3P3 82

TBT_B_PWRSW_ISET_S0 82

TBT_B_PWRSW_ISET_S3 82

R9580 17.8K 1% 1/20W MF 201 <RHVS3>; R9581 17.8K 1% 1/20W MF 201 <RHVS0>; R9582 36.5K 1% 1/20W MF 201 <RV3P3>

TBT_B_PWRSW_ISET_S3_R 82

TBT_B_PWRSW_ISET_S0_R 82

R9583 17.8K 1% 1/20W MF 201; R9584 17.8K 1% 1/20W MF 201

ILIM = 40000 / RISET

L9500 FERR-120-OHM-3A 0603

PP3V3RHV_SW_TBT_B_PWR 78

C9500 0.01UF 10% 50V X7R-CERM 0402

R9501 12 5% 1/20W MF 201

TBT_B_CONN_20_RC 82

C9501 0.01UF 10% 25V X5R-CERM 0201

FR SIDE

PP3V3_SW_TBT_B_PWR 78 67

C9560 0.01UF 10% 16V X5R-CERM 0201; C9561 0.1UF 10% 6.3V CERM-X5R 0201

GND_VOID=TRUE

TBT_RX1

TBT_B_D2R_N<1>	C9576 0.47UF 20% 4V CERM-X5R-1 201	TBT_B_D2R_C_N<1>	82 78
TBT_B_D2R_P<1>	C9577 0.47UF 20% 4V CERM-X5R-1 201	TBT_B_D2R_C_P<1>	82 78

DP_AUX

DP_TBTPB_AUXCH_C_N	C9566 0.1UF 10% 6.3V CERM-X5R 0201	DP_TBTPB_AUXCH_N	82 75
DP_TBTPB_AUXCH_C_P	C9567 0.1UF 10% 6.3V CERM-X5R 0201	DP_TBTPB_AUXCH_P	82 75

DDC

DP_TBTPB_DDC_DATA		
DP_TBTPB_DDC_CLK		

DP<1>

DP_TBTPB_ML_C_P<1>	C9568 0.22UF 20% 6.3V X5R 0201	DP_TBTPB_ML_P<1>	75
DP_TBTPB_ML_C_N<1>	C9569 0.22UF 20% 6.3V X5R 0201	DP_TBTPB_ML_N<1>	75

TBT_B_LSTX	
TBT_B_LSRX	
DP_TBTPB_HPD	

U9560 CBTL05024 HVQFN

3	VDD		
7	TB-	TB_ENA	15
8	TB+	AUXIO_EN	24
		DP_PD	6
1	AUX-(100K PU)	AUXIO-	23
2	AUX+(100K PD)	AUXIO+	22
4	DDC_DAT		
5	DDC_CLK		
16	CA_DETOUT	CA_DET	18
11	DP+	DPMLO+	19
10	DP-	DPMLO-	20
14	LSTX(10K PU)		
13	LSRX(1M PD)		
12	HPDOUT	HPD	17
9	GND	THMPAD	21, 25

SIGNAL_MODEL=TBT_MUX_5024

CRITICAL

CONN SIDE

AUXIO_EN = H ENABLE THE TB MUX
NOTE: A SINGLE SIGNAL TO
ENABLE TBMUX IN 6 5024.

TBT_B_CIO_SEL (IN) 62

TBTDP_AUXIO_EN (IN) 62 66

TBT_B_DP_PWRDN (IN) 62

TBT_B_D2R1_AUXDDC_N 67 79 81

TBT_B_D2R1_AUXDDC_P 67 79 81

TBT: LSX_R2P/P2R (P/N)

TBT_B_CONFIG1_RC 67

DP_B_LSX_ML_P<1> 67 75 81

DP_B_LSX_ML_N<1> 67 75 81

TBT_B_HPD 67

DP_PD	DPMLO+/-
0	DP+,DP-
1	LSTX,LSRX

TB_ENA	CA_DET	AUXIO+/-
1	X	TB+/-
0	0	AUX+/-
0	1	DDC_CLK/_DAT

THUNDERBOLT CONNECTOR B
BACK WALL

RID = 0X0

(NO LANE REVERSALS ALLOWED.)

TBT_B_CONN_1_C 82

C9505 0.01UF 10% 25V X5R-CERM 0201 (0-20V) PLACE_NEAR=J9500.1:2MM

C9506 0.01UF 10% 25V X5R-CERM 0201 (0-20V) PLACE_NEAR=J9500.7:2MM

TBT: TX_0

TBT_B_CONN_7_C 82

DP Dir TBT Dir

TBT_B_R2D_P<0> 82 79

TBT_B_R2D_N<0> 82 79

TBT_TX0
DP_0

GND_VOID=TRUE (Both C's)

C9570 0.22UF 20% 6.3V X5R 0201 — TBT_B_R2D_C_P<0> (IN) 62 79 81

C9571 0.22UF 20% 6.3V X5R 0201 — TBT_B_R2D_C_N<0> (IN) 62 79 81

R9570 470K 5% 1/20W MF 201; R9571 470K 5% 1/20W MF 201

TBT_LSX
DP_1

DP_B_LSX_ML_P<1> 67 75 81

DP_B_LSX_ML_N<1> 67 75 81

TBT: LSX_R2P/P2R (P/N)

TBT_TX1
DP_2

TBT_B_R2D_P<1> 82 79

TBT_B_R2D_N<1> 82 79

TBT: TX_1

C9572 0.22UF 20% 6.3V X5R 0201 — TBT_B_R2D_C_P<1> (IN) 62 79 82

C9573 0.22UF 20% 6.3V X5R 0201 — TBT_B_R2D_C_N<1> (IN) 62 79 82

R9572 470K 5% 1/20W MF 201; R9573 470K 5% 1/20W MF 201

470k R's for ESD protection
on AC-coupled signals.

J9500 MINIDSPLYPRT-PL-J40 F-RT-TH-1 CRITICAL

FOR J9500 TBT_SMT PADS (3, 5, 17 & 19): GND_VOID=TRUE

BOT ROW TH PINS		TOP ROW SM PINS	
2	DP_HPD	GND	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
8	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	13
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19

SHIELD PINS 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21

514-0800

TBT_RX0

GND_VOID=TRUE (Both C's)

TBT_B_D2R_P<0>	C9574 0.47UF 20% 4V CERM-X5R-1 201	TBT_B_D2R_C_P<0>	81 79
TBT_B_D2R_N<0>	C9575 0.47UF 20% 4V CERM-X5R-1 201	TBT_B_D2R_C_N<0>	81 79

TBT Dir DP Dir

GND_VOID=TRUE

R9594 1K 5% 1/20W MF 201; R9595 1K 5% 1/20W MF 201

NO_XNET_CONNECTION=TRUE

R9578 470K 5% 1/20W MF 201

R9579 470K 5% 1/20W MF 201

DP_3

DP_TBTPB_ML_C_P<3>	C9578 0.22UF 20% 6.3V X5R 0201	DP_TBTPB_ML_P<3>	82 75
DP_TBTPB_ML_C_N<3>	C9579 0.22UF 20% 6.3V X5R 0201	DP_TBTPB_ML_N<3>	82 75

TBT: Unused

TBT_RX1/DP_AUX

TBT_B_D2R1_AUXDDC_P	81 79 67
TBT_B_D2R1_AUXDDC_N	81 79 67

TBT_CFG

TBT_B_HPD	67
TBT_B_CONFIG1_RC	67
TBT_B_CONFIG2_RC	62 (OUT)

R9552 1M 5% 1/20W MF 201; R9551 1M 5% 1/20W MF 201; C9594 330PF 10% 16V X7R 0201; C9595 330PF 10% 16V X7R 0201; R9541 100K 5% 1/20W MF 201

C9502 0.01UF 10% 16V X5R-CERM 0201 PLACE_NEAR=J9500.2:2MM

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

HPD	CFG1	CFG2	MODE	DIFF PAIRS MAPPING:					
0	0	0	NO_CABLE						
0	0	1	TBT	TX0	LSTX/LSRX	TX1		RX1	RX0
1	0	0	DP	DP_0	DP_1	DP_2	DP_3	DP_AUX	
1	1	0	DP_ADAPTER	TD2	TD1	TD0	TD_CLK	DDC_CLK/DDC_DAT	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-2198	12	SOLDER PREFORM 0201	SF9500,SF9501,SF9502,SF9503,SF9504,SF9505,SF9506,SF9507,SF9508,SF9509,SF9510,SF9511	CRITICAL	?

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-20

PAGE TITLE: TBT CONNECTOR B

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

BRANCH:

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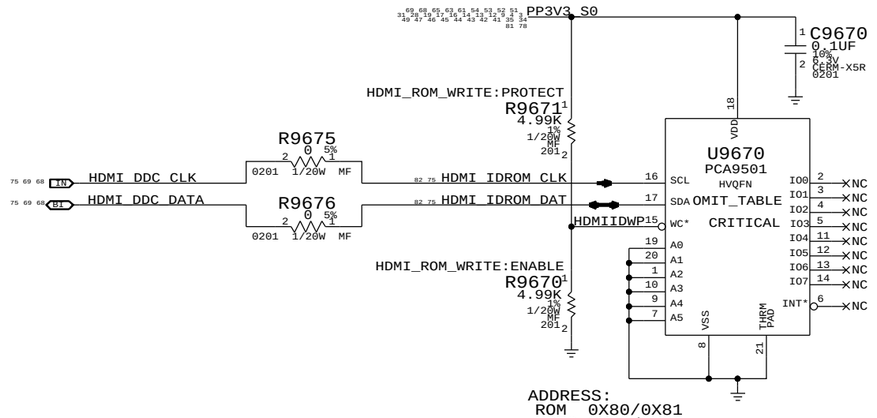
DISPLAY MUX: DP OR HDMI

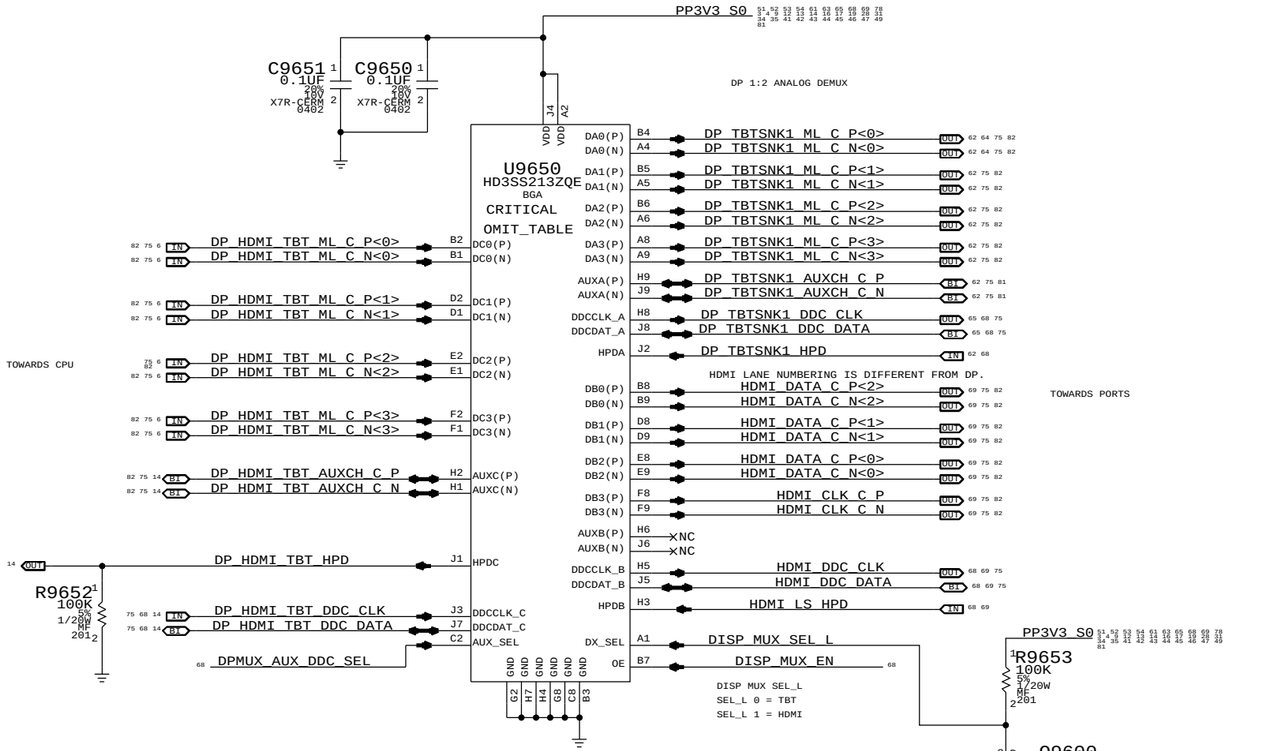
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
311S0642	1	IC,PCA9501BS/S544,20 HVQFN	U9670		

HDMI ADAPTER ID ROM

INFORM SOFTWARE OF DP++ TO HDMI ADAPTION

WHEN MUX IS SET TO HDMI PORT.



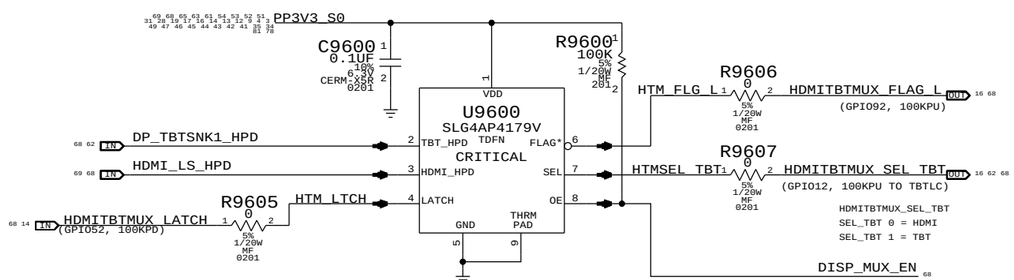


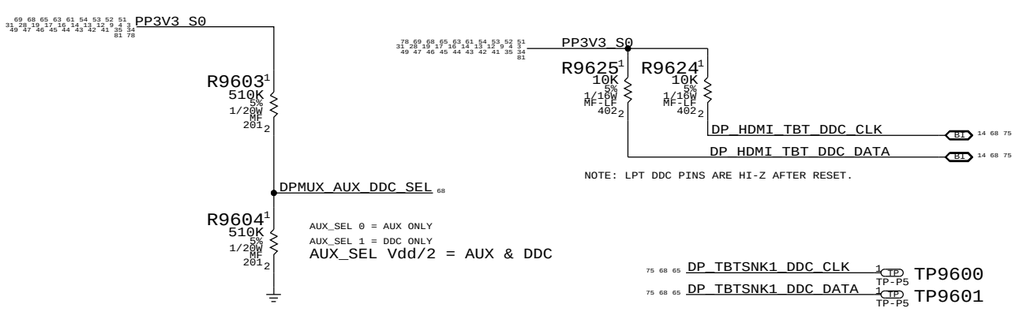
NOTE: HDMI ML SWIZZLED INTENTIONALLY AS PER TABLE 9-1 HASWELL-ULT PDG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4068	1	CB,TL06142F,DP/PCIE/HDMI 2:1,BGA50 U9650		CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4070	353S4068			PERICOM PI3WVR12612NEE
353S4069	353S4068			TI HD3SS213

DP_MUX CTLR





NOTE: LPT DDC PINS ARE HI-Z AFTER RESET.

DP_TBTSNK1_DDC_CLK — TP9600
DP_TBTSNK1_DDC_DATA — TP9601
HDMI_DDC_CLK — TP9602
HDMI_DDC_DATA — TP9603
DP_TBTSNK0_HPD — TP9604
DP_TBTSNK1_HPD — TP9605
HDMI_LS_HPD — TP9606
HDMITBTMUX_LATCH — TP9607
HDMITBTMUX_FLAG_L — TP9608
HDMITBTMUX_SEL_TBT — TP9609
DISP_MUX_EN — TP9610

SYNC_MASTER=J64 2C SYNC_DATE=2014-01-21

PAGE TITLE

DISPLAY MUX, HDMI DDC ID ROM

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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BRANCH

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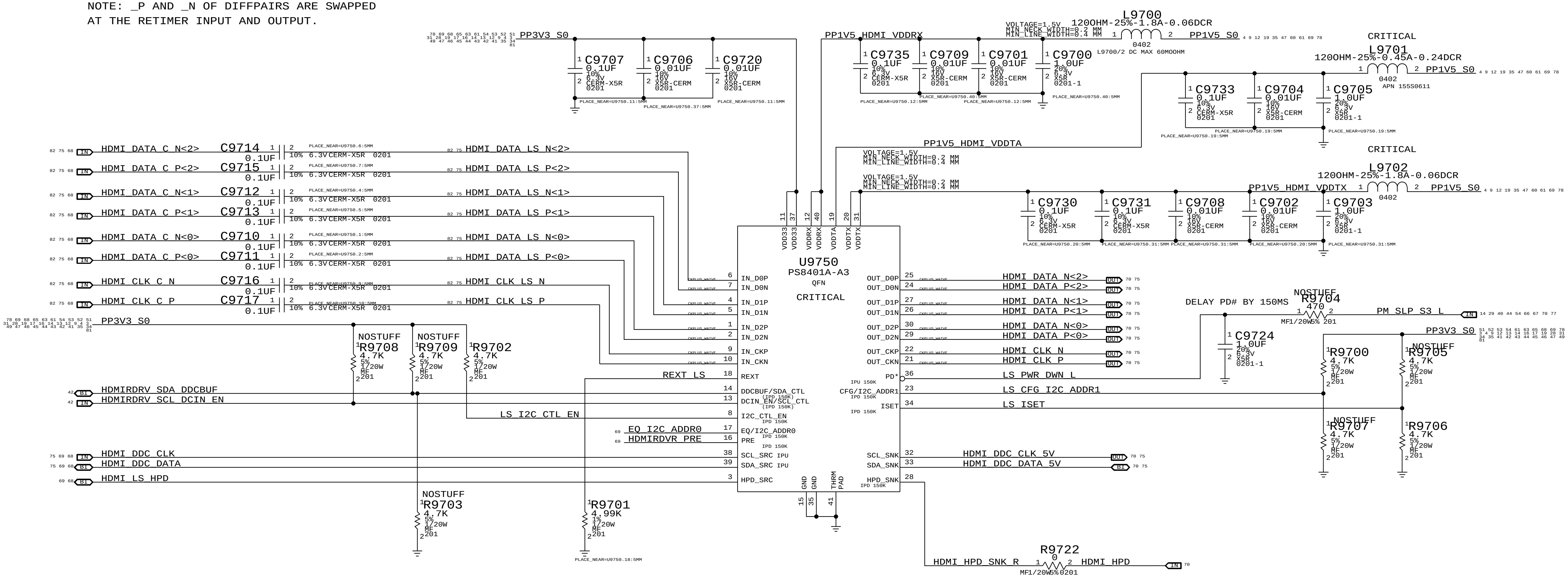
MAX 1.5V CURRENT <= 431MA
MAX 3.3V CURRENT <= 5MA

MAX 1.5V_VDDRX CURRENT <180MA
MAX 1.5V_VDDTX CURRENT <200MA
MAX 1.5V_VDDTA CURRENT <20MA

NOTE: _P AND _N OF DIFFPAIRS ARE SWAPPED
AT THE RETIMER INPUT AND OUTPUT.



PP3V3_S0
C9707 0.1UF
C9706 0.01UF
C9720 0.01UF
PP1V5_HDMI_VDDRX
C9735 0.1UF
C9709 0.01UF
C9701 0.01UF
C9700 1.0UF
CRITICAL
L9700
120OHM-25%-1.8A-0.06DCR
PP1V5_S0
CRITICAL
L9701
120OHM-25%-0.45A-0.24DCR
PP1V5_S0
C9733 0.1UF
C9704 0.01UF
C9705 1.0UF
PP1V5_HDMI_VDDTA
CRITICAL
L9702
120OHM-25%-1.8A-0.06DCR
PP1V5_HDMI_VDDTX
PP1V5_S0
C9730 0.1UF
C9731 0.1UF
C9708 0.01UF
C9702 0.01UF
C9703 1.0UF
HDMI_DATA_C_N<2>
HDMI_DATA_C_P<2>
HDMI_DATA_C_N<1>
HDMI_DATA_C_P<1>
HDMI_DATA_C_N<0>
HDMI_DATA_C_P<0>
HDMI_CLK_C_N
HDMI_CLK_C_P
C9714 C9715 C9712 C9713 C9710 C9711 C9716 C9717 0.1UF
HDMI_DATA_LS_N<2>
HDMI_DATA_LS_P<2>
HDMI_DATA_LS_N<1>
HDMI_DATA_LS_P<1>
HDMI_DATA_LS_N<0>
HDMI_DATA_LS_P<0>
HDMI_CLK_LS_N
HDMI_CLK_LS_P
U9750
PS8401A-A3
QFN
CRITICAL
NOSTUFF R9708 4.7K
NOSTUFF R9709 4.7K
R9702 4.7K
HDMIRDRV_SDA_DDCBUF
HDMIRDRV_SCL_DCIN_EN
LS_I2C_CTL_EN
REXT_LS
EQ_I2C_ADDR0
HDMIRDVR_PRE
HDMI_DDC_CLK
HDMI_DDC_DATA
HDMI_LS_HPD
NOSTUFF R9703 4.7K
R9701 4.99K
HDMI_DATA_N<2>
HDMI_DATA_P<2>
HDMI_DATA_N<1>
HDMI_DATA_P<1>
HDMI_DATA_N<0>
HDMI_DATA_P<0>
HDMI_CLK_N
HDMI_CLK_P
DELAY PD# BY 150MS
NOSTUFF R9704 470
PM_SLP_S3_L
C9724 1.0UF
PP3V3_S0
LS_PWR_DWN_L
LS_CFG_I2C_ADDR1
LS_ISET
R9700 4.7K
NOSTUFF R9705 4.7K
NOSTUFF R9707 4.7K
R9706 4.7K
HDMI_DDC_CLK_5V
HDMI_DDC_DATA_5V
HDMI_HPD_SNK_R
R9722 0
HDMI_HPD

PRE=L, NO PRE-EMP.
PRE=H, 1.6 DB PRE-EMP
PRE=M, 2.5 DB PRE-EMP.

ISET= L, OUTPUT SWING DEFAULT
ISET= H, OUTPUT SWING +13%
ISET= M, OUTPUT SWING -13%

PRE AND ISET AVAILABLE IN.
BOTH PIN AND I2C MODE.

I2C_CTL_EN=L, PIN CONTROL MODE
I2C_CTL_EN=H, I2C CONTROL MODE

DDCBUF=H, ACTIVE DDC BUFFER
DDCBUF=L, PASSIVE DDC PASS THROUGH
DDCBUF=M, ACTIVE DDC PASS THROUGH W/O IPU

DCIN_EN=H, DC COUPLING INPUT
DCIN_EN=L, AC COUPLING INPUT

NOTE: IN I2C CONTROL MODE,
PIN 13 AND PIN 14 FUNCTION
AS I2C CLK AND DATA,
NOT AS PIN STRAPS.

IN I2C CONTROL MODE
DDCBUFF AND DCIN_EN ARE CONFIGURED BY INTERNAL REGISTERS

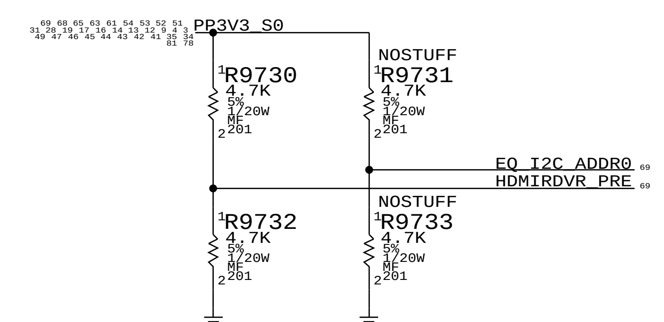
CFG=L, HDMI ID DISABLED
CFG=H, HDMI ID ENABLED

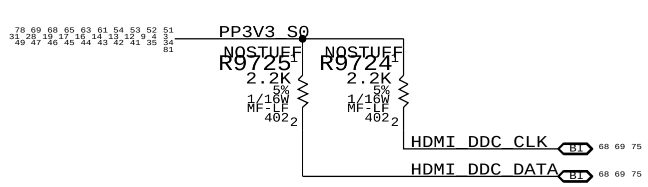
EQ=L, FOR CH. LOSS UP TO 12.4 DB
EQ=H, FOR CH. LOSS UP TO 4.3 DB
EQ=M, FOR CH. LOSS UP TO 8.6 DB

PD# =L, PS8401 POWER DOWN
PD# =H, PS8401 IN NORMAL MODE

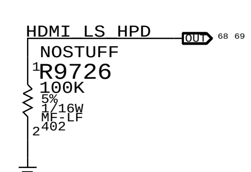
IN I2C CONTROL MODE
PIN 17 AND PIN 23 FUNCTION AS I2C ADDR

EQ AND CFG ARE CONFIGURED BY INTERNAL REGISTERS





8401 INTERNAL DDC PU 2.36K IS USED.



I2C control enabled when R9702 is stuffed

	I2C_ADDR1	I2C_ADDR0	I2C ADDRESS(W/R)
	L	L	0x4C/4D (default)
	L	H	0x5C/5D
J64	H	L	0xCC/CD
	H	H	0xEC/ED

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-20

PAGE TITLE

HDMI RETIMER

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

BRANCH

HDMI CONNECTOR

CRITICAL

PLACE NEAR J9830 CONNECTOR

L9860
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
152S1621
PLACE_NEAR=J9830.10:10MM

HDMI_CLK_P
HDMI_CLK_FLT_P
NOSTUFF R9860 100 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C9861 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9861
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
152S1621
PLACE_NEAR=J9830.10:10MM

HDMI_CLK_N
HDMI_CLK_FLT_N
C9863 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9893
35-OHM-50MA
TCM0605
155S0803

HDMI_CLK_CNR_P
R9830 0 5% 1/20W MF 0201
NOSTUFF R9864 511 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
PLACE_NEAR=J9830.10:7MM
CRITICAL D9820 ESD0P2RF-02LS TSSLP-2-1
HDMI_CLK_CONN_P

HDMI_CLK_CNR_N
R9831 0 5% 1/20W MF 0201
CRITICAL D9821 ESD0P2RF-02LS TSSLP-2-1
HDMI_CLK_CONN_N

LAYOUT HAS A MANUALLY ADDED
0.75 MM^2 COPPER SHAPE FOR 0.4PF
AT THE LEFT SIDE OF L676X.
ASSUMES 70MICRON DIELECTRIC, DK=4.15

CRITICAL L9862
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
PLACE_NEAR=J9830.7:10MM

HDMI_DATA_P<0>
HDMI_DATA_FLT_P<0>
NOSTUFF R9861 100 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C9865 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9863
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
PLACE_NEAR=J9830.7:10MM

HDMI_DATA_N<0>
HDMI_DATA_FLT_N<0>
C9867 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9890
35-OHM-50MA
TCM0605
155S0803

HDMI_DAT_CNR_P<0>
R9832 0 5% 1/20W MF 0201
NOSTUFF R9865 511 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
PLACE_NEAR=J9830.7:7MM
CRITICAL D9822 ESD0P2RF-02LS TSSLP-2-1
HDMI_DATA_CONN_P<0>

HDMI_DAT_CNR_N<0>
R9833 0 5% 1/20W MF 0201
CRITICAL D9823 ESD0P2RF-02LS TSSLP-2-1
HDMI_DATA_CONN_N<0>

CRITICAL L9864
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
PLACE_NEAR=J9830.4:10MM

HDMI_DATA_P<1>
HDMI_DATA_FLT_P<1>
NOSTUFF R9862 100 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C9869 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9865
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
PLACE_NEAR=J9830.4:10MM

HDMI_DATA_N<1>
HDMI_DATA_FLT_N<1>
C9871 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9891
35-OHM-50MA
TCM0605
155S0803

HDMI_DAT_CNR_P<1>
R9834 0 5% 1/20W MF 0201
NOSTUFF R9866 511 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
PLACE_NEAR=J9830.4:7MM
CRITICAL D9824 ESD0P2RF-02LS TSSLP-2-1
HDMI_DATA_CONN_P<1>

HDMI_DAT_CNR_N<1>
R9835 0 5% 1/20W MF 0201
CRITICAL D9825 ESD0P2RF-02LS TSSLP-2-1
HDMI_DATA_CONN_N<1>

teknisi-indonesia

CRITICAL L9866
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
PLACE_NEAR=J9830.1:10MM

HDMI_DATA_P<2>
HDMI_DATA_FLT_P<2>
NOSTUFF R9863 100 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C9873 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9867
2.9NH+/-0.1NH-0.5A-0.2OHM
0201
PLACE_NEAR=J9830.1:10MM

HDMI_DATA_N<2>
HDMI_DATA_FLT_N<2>
C9875 2.9PF +/-0.05PF 25V C0G-CERM 0201

CRITICAL L9892
35-OHM-50MA
TCM0605
155S0803

HDMI_DAT_CNR_P<2>
R9836 0 5% 1/20W MF 0201
NOSTUFF R9867 511 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
PLACE_NEAR=J9830.1:7MM
CRITICAL D9826 ESD0P2RF-02LS TSSLP-2-1
HDMI_DATA_CONN_P<2>

HDMI_DAT_CNR_N<2>
R9837 0 5% 1/20W MF 0201
CRITICAL D9827 ESD0P2RF-02LS TSSLP-2-1
HDMI_DATA_CONN_N<2>

ENABLE WITH A DIFFERENT RAIL
TO CUT OFF POTENTIAL BACK-FLOW.

HDMI SPEC IS 55MA TO 500MA
SWITCH CUTS OFF AT 101MA TO 142MA.

PP3V3_S4
R9802 10K 5% 1/20W MF 201
HDMI_EN

PP5V_S4
CRITICAL C9800 22UF 20% 6.3V X5R-CERM 0603
C9802 0.1UF 10% 10V X7R-CERM 0402
CRITICAL U9800 TPS2553 SON
IN, OUT, EN, ILIM, FAULT*, GND, THRML PAD
R9801 113K 1% 1/10W MF-LF 402
CRITICAL C9803 10UF 20% 6.3V X5R-CERM 0402-2
CRITICAL L9830 600-OHM-25%-0.5A-0.40OHM 0603
C9830 0.01UF 10% 16V X5R-CERM 0201
HDMI_ILIM
R9803 113K 1% 1/10W MF-LF 402
HDMI_ILIMB
R9800 10K 5% 1/20W MF 201
PU_HDMI_OC_L
REDUNDANCY FOR SAFETY

PP5V_HDMI_DDC_FUSE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM

J9830
HDMI-PLASTIC-J40
F-RT-SM1

HDMI_DATA_CONN_P<2>	1 TMDS_DATA2_P	TMDS_DATA2_SHLD1 2	
HDMI_DATA_CONN_N<2>	3 TMDS_DATA2_M	TMDS_DATA1_P 4	HDMI_DATA_CONN_P<1>
	5 TMDS_DATA1_SHLD1	TMDS_DATA1_M 6	HDMI_DATA_CONN_N<1>
HDMI_DATA_CONN_P<0>	7 TMDS_DATA0_P	TMDS_DATA0_SHLD1 8	
HDMI_DATA_CONN_N<0>	9 TMDS_DATA0_M	TMDS_CLK_P 10	HDMI_CLK_CONN_P
	11 TMDS_CLK_SHLD	TMDS_CLK_M 12	HDMI_CLK_CONN_N
NC	13 CEC	RSRVD 14	
HDMI_DDC_CLK_CONN	15 SCL	SDA 16	HDMI_DDC_DATA_CONN
HDMI_HPD_CONN	17 DDC_CED_GND	P_5V_PWR 18	PP5V_HDMI_DDC_CONN
	19 HOT_PLUG_DETECT		
	20 IO20	IO21 21	
	22 IO22	IO23 23	
	24 IO24	IO25 25	
	26 IO26	IO27 27	
	28 IO28	IO29 29	
	30 IO30	IO31 31	
	32 IO32	IO33 33	
	34 IO34		

CRITICAL
SHLD PINS

HDMI SPEC 1.4:
HPD H:2.0-5.3V
HPD L:0.0-0.4V

514-0799

max Current<7mA
IDSON:5 OHM

CRITICAL
APN 376S0974
Q9851 DFN1006H4-3 DMP210DUFB4
VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.4 MM
PP5V_HDMI_DDC_S0_F

PP5V_HDMI_DDC_FUSE
R9850 220K 1% 1/20W MF 201
NOSTUFF C9850 0.01UF 10% 16V X5R-CERM 0201
NOSTUFF C9852 0.01UF 10% 16V X5R-CERM 0201
R9851 1K 5% 1/20W MF 201
ENABLE_HDMI_DDC_S0_R
ENABLE_HDMI_DDC_S0

Q9850 SSM3K15FV SOD-VESM-HF
PM_SLP_S3_L

CRITICAL L9850 FERR-470-OHM-215MA-1.5OHM 0201
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
(PP5V_HDMI_DDC_S0_F)
PP5V_HDMI_DDC_S0
R9810 2.0K 5% 1/20W MF 201
R9812 2.0K 5% 1/20W MF 201
C9851 0.01UF 10% 16V X5R-CERM 0201
C9810 0.01UF 10% 16V X5R-CERM 0201

PLACE CAPS CLOSE
TO HDMI CONNECTOR

CRITICAL L9810 FERR-470-OHM-215MA-1.5OHM 0201
HDMI_DDC_CLK_CONN
C9811 18PF 5% 25V C0G 0201
HDMI_DDC_CLK_F
R9811 33 5% 1/20W MF 201
HDMI_DDC_CLK_5V

CRITICAL L9811 FERR-470-OHM-215MA-1.5OHM 0201
HDMI_DDC_DATA_CONN
C9813 18PF 5% 25V C0G 0201
HDMI_DDC_DATA_F
R9813 33 5% 1/20W MF 201
HDMI_DDC_DATA_5V

CRITICAL L9841 FERR-470-OHM-215MA-1.5OHM 0201
HDMI_HPD_CONN
C9814 220PF 10% 25V X7R-CERM 201
HDMI_HPD_F
R9814 1K 5% 1/20W MF 201
HDMI_HPD
150K PULL-DOWN IS BUILT IN PS8401

CRITICAL D9800 RCLAMP0504F SC70-6-1
NC
PP5V_HDMI_DDC_CONN

SYNC_MASTER=J64 2C	SYNC_DATE=2014-01-16
PAGE TITLE	HDMI CONNECTOR
Apple Inc.	DRAWING NUMBER 051-1907 SIZE D
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J64 12 LAYER BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.075 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.265 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.177 MM	0.075 MM			
40_OHM_SE	ISL3,ISL10	Y	0.145 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	0.135 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.075 MM			
50_OHM_SE	ISL3,ISL10	Y	0.092 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	*	Y	0.088 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.075 MM			
55_OHM_SE	ISL3,ISL10	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.183 MM	0.075 MM		0.120 MM	0.120 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.162 MM	0.075 MM	=STANDARD	0.180 MM	0.180 MM
70_OHM_DIFF	*	Y	0.155 MM	0.075 MM	=STANDARD	0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.075 MM		0.130 MM	0.130 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.150 MM	0.075 MM	=STANDARD	0.170 MM	0.170 MM
73_OHM_DIFF	*	Y	0.143 MM	0.075 MM	=STANDARD	0.170 MM	0.170 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.075 MM		0.130 MM	0.130 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.110 MM	0.075 MM	=STANDARD	0.160 MM	0.160 MM
85_OHM_DIFF	*	Y	0.105 MM	0.075 MM	=STANDARD	0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.075 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.104 MM	0.075 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	*	Y	0.099 MM	0.075 MM	=STANDARD	0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.096 MM	0.075 MM		0.180 MM	0.180 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.075 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	*	Y	0.077 MM	0.075 MM	=STANDARD	0.200 MM	0.200 MM

Memory Physical definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
MEM_40S	TOP,BOTTOM	Y	=40_OHM_SE	0.115 MM	10.000 MM	=STANDARD	=STANDARD	
MEM_40S	ISL3,ISL10	Y	=40_OHM_SE	0.092 MM	10.000 MM	=STANDARD	=STANDARD	40 ohm width with 50 ohm neck, for termination route
MEM_40S	*	Y	=40_OHM_SE	0.088 MM	10.000 MM	=STANDARD	=STANDARD	
MEM_70D	TOP,BOTTOM	Y	=70_OHM_DIFF	0.170 MM	10.000 MM	=70_OHM_DIFF	=73_OHM_DIFF	
MEM_70D	ISL3,ISL10	Y	=70_OHM_DIFF	0.150 MM	10.000 MM	=70_OHM_DIFF	=73_OHM_DIFF	70 ohm width with 73 ohm neck, for termination route
MEM_70D	*	Y	=70_OHM_DIFF	0.143 MM	10.000 MM	=70_OHM_DIFF	=73_OHM_DIFF	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1_1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HI_PWR	*	Y	0.600 MM	0.200 MM	=STANDARD	=STANDARD	=STANDARD
POWER	*	Y	0.400 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD
WIDE	*	Y	0.250 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_SP OVERRIDE	* OVERRIDE	0.200 MM OVERRIDE	? OVERRIDE
POWER_SP OVERRIDE	* OVERRIDE	0.200 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.070 MM	?
1:1_SPACING	*	0.067 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP,BOTTOM	0.070 MM	?
1X_DIELECTRIC	*	0.067 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P075MM	*	0.075 MM	?

Breakout Constraint Overrides

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

SYNC_MASTER=J50I SYNC_DATE=05/16/2011

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Spacing definitions

SATA and USB Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	TOP,BOTTOM	=9:1_SPACING	?
SATA_ISO	*	=7:1_SPACING	?
USB_ISO	TOP,BOTTOM	=4:1_SPACING	?
USB_ISO	*	=2:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?
USB3_ISO	*	=3.8:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
USB	*	*	USB_ISO
USB3	*	*	USB3_ISO

PCIE/DMI Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PE_ISO	TOP,BOTTOM	=4:1_SPACING	?
PE_ISO	*	=4:1_SPACING	?
PE2SELF_ISO	TOP,BOTTOM	=4:1_SPACING	?
PE2SELF_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PE_*	*	*	PE_ISO
PE_*	=SAME	*	PE2SELF_ISO

DP/HDMI Signals Specific Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	TOP,BOTTOM	=5.5:1_SPACING	?
DP_ISO	*	=4.5:1_SPACING	?
DP2SELF_ISO	TOP,BOTTOM	=5.5:1_SPACING	?
DP2SELF_ISO	*	=4.5:1_SPACING	?
TBT_ISO	TOP,BOTTOM	=7:1_SPACING	?
TBT_ISO	*	=5:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_*	*	*	DP_ISO
DP_*	=SAME	*	DP2SELF_ISO
TBT_*	*	*	TBT_ISO

Differential and single ended clock Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DIFF_CLK_ISO	TOP,BOTTOM	=7:1_SPACING	?
DIFF_CLK_ISO	*	=3:1_SPACING	?
CLK_ISO	TOP,BOTTOM	=5:1_SPACING	?
CLK_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DIFF_CLK	*	*	DIFF_CLK_ISO
CLK	*	*	CLK_ISO

ENET Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2KV_ISO	TOP,BOTTOM	1.27 MM	900
2KV_ISO	*	0.5 MM	900
ENET_ISO	TOP,BOTTOM	=7:1_SPACING	?
ENET_ISO	*	=6:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET	*	*	ENET_ISO
ENET_2KV	ENET_2KV	*	ENET_ISO
ENET_2KV	*	*	2KV_ISO
ENET_2KV	POWER_SP	*	2KV_ISO
ENET_2KV	GND_SP	*	2KV_ISO
ENET_2KV	*	*	2KV_ISO

lower speed Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	TOP,BOTTOM	=2.5:1_SPACING	?
SPI_ISO	*	=2:1_SPACING	?
SMB_ISO	TOP,BOTTOM	=2.5:1_SPACING	?
SMB_ISO	*	=2:1_SPACING	?
PECI_ISO	TOP,BOTTOM	=5:1_SPACING	?
PECI_ISO	*	=3:1_SPACING	?
SD_ISO	*	=3:1_SPACING	?
PM_ISO	*	=2:1_SPACING	?
HDA_ISO	*	=2.5:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO
SMB	*	*	SMB_ISO
PECI	*	*	PECI_ISO
SD	*	*	SD_ISO
PM	*	*	PM_ISO
HDA	*	*	HDA_ISO

CRITICAL SIGNALS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SVID_ISO	TOP,BOTTOM	=6:1_SPACING	?
SVID_ISO	*	=5:1_SPACING	?
RCOMP_ISO	*	=4:1_SPACING	?
RCOMP_LG_ISO	*	=9:1_SPACING	?
RCOMP_LG_SELF	*	=7:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SVID_SP	*	*	SVID_ISO
RCOMP_SP	*	*	RCOMP_ISO
RCOMP_LG	*	*	RCOMP_LG_ISO
RCOMP_LG	RCOMP_LG	*	RCOMP_LG_SELF
RCOMP_LG	RCOMP_SP	*	RCOMP_LG_SELF

AUDIO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO_ISO	*	=7:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	AUDIO_ISO
AUDIO	AUDIO	*	DEFAULT

VR physical and Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VR_PHASE	*	Y	1.000 MM	0.100 MM	10.000 MM	=STANDARD	=STANDARD
VR_GATE	*	Y	0.500 MM	0.100 MM	10.000 MM	=STANDARD	=STANDARD
VR_CTL	*	Y	0.300 MM	0.100 MM	10.000 MM	=STANDARD	=STANDARD
VR_SENSE	*	Y	0.300 MM	0.100 MM	10.000 MM	0.400 MM	0.200 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	0.6 MM	?
GATE_ISO	*	0.4 MM	?
VR_SENSE_ISO	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_PHASE	*	*	PHASE_ISO
VR_PHASE	VR_UG	*	STANDARD
VR_PHASE	POWER_SP	*	STANDARD
VR_PHASE	GND_SP	*	STANDARD
VR_UG	*	*	GATE_ISO
VR_UG	POWER_SP	*	STANDARD
VR_UG	GND_SP	*	STANDARD
VR_LG	*	*	GATE_ISO
VR_LG	POWER_SP	*	STANDARD
VR_LG	GND_SP	*	STANDARD
VR_SENSE	*	*	VR_SENSE_ISO

Route SMB as pseudo diff pair with 0.2 mm spacing

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50SE	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	0.2 MM	0.2 MM

Route Audio 0.6 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P6MM	*	Y	0.6MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.5 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P5MM	*	Y	0.5MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.4 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P4MM	*	Y	0.4MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.3 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P3MM	*	Y	0.3MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.2 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P2MM	*	Y	0.2MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio Spkr Diff Pair

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_SPKR	*	Y	0.5MM	0.1MM	10MM	0.5 MM	0.2 MM

Route RCOMP 0.38 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
RCOMP_PHYS	*	Y	0.380 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

Memory Spacing definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_SELF_ISO	*	=3:1_SPACING	?
MEM_MEM_ISO	*	=4.8:1_SPACING	?
MEM_DATA_ISO	*	=6.4:1_SPACING	?
MEM_PWR_ISO	*	=2:1_SPACING	900

DQ SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_SELF_ISO
MEM_*_DATA_*	MEM_*_DATA_*	*	MEM_MEM_ISO
MEM_*_DATA_*	MEM_*_DQS_*	*	MEM_MEM_ISO
MEM_CLK	MEM_*_DATA_*	*	MEM_DATA_ISO
MEM_CTRL	MEM_*_DATA_*	*	MEM_DATA_ISO
MEM_CMD	MEM_*_DATA_*	*	MEM_DATA_ISO
MEM_*_DATA_*	*	*	MEM_DATA_ISO

DQS SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQS_*	*	*	MEM_MEM_ISO

CMD SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_SELF_ISO
MEM_CMD	*	*	MEM_MEM_ISO

CTRL SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_SELF_ISO
MEM_CTRL	*	*	MEM_MEM_ISO

CLK SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_MEM_ISO

POWER SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER_SP	MEM_*	*	MEM_PWR_ISO
GND_SP	MEM_*	*	MEM_PWR_ISO

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MEMORY Constraints

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AGND_*

	Physical	Spacing	Voltage	Netname	
H5	VR_CTL	GND_SP	0V	AGND_P1V05S0	59
H6	VR_CTL	GND_SP	0V	AGND_P1V2_S3	56

ALL_*

	Physical	Spacing	Netname	
H5	50_OHM_SE	PM	ALL_PWRGD_DLY	54
H6	50_OHM_SE	PM	ALL_SYS_PWRGD	17 19 40 54

AMBIENT1_*

	Physical	Spacing	Netname	
H5	SMB_50SE	SMB	AMBIENT1_THRMD_N	45
H6	SMB_50SE	SMB	AMBIENT1_THRMD_P	45

AMBIENT2_*

	Physical	Spacing	Netname	
H7	SMB_50SE	SMB	AMBIENT2_THRMD_N	45
H8	SMB_50SE	SMB	AMBIENT2_THRMD_P	45

AMBIENT3_*

	Physical	Spacing	Netname	
H9	SMB_50SE	SMB	AMBIENT3_THRMD_N	45
H10	SMB_50SE	SMB	AMBIENT3_THRMD_P	45

AP_*

	Physical	Spacing	Netname	
H11	50_OHM_SE	PM	AP_RESET_L	16 32
H12	50_OHM_SE	PM	AP_S0IX_WAKE_L	16

AUD_*

	Physical	Spacing	Voltage	Netname	
H13		AUDIO		AUD_CH_HS_GND	46 49
H14		AUDIO		AUD_CODEC_HPO_L	46
H15		AUDIO		AUD_CODEC_HPO_R	46
H16		AUDIO		AUD_CODEC_HS_MICN	46
H17		AUDIO		AUD_CODEC_HS_MICP	46
H18	AUD_0P2MM	AUDIO		AUD_CODEC_LI_L_N	46 48
H19	AUD_0P2MM	AUDIO		AUD_CODEC_LI_L_P	46 48
H20	AUD_0P2MM	AUDIO		AUD_CODEC_LI_R_N	46 48
H21	AUD_0P2MM	AUDIO		AUD_CODEC_LI_R_P	46 48
H22		AUDIO		AUD_CONNJ1_MIC	49 81
H23		AUDIO		AUD_CONNJ1_RING	49 81
H24		AUDIO		AUD_CONNJ1_SLEEVE	49 81
H25		AUDIO		AUD_CONNJ1_TIP	49 81
H26		AUDIO		AUD_CONNJ1_TIPDET1	49
H27		AUDIO		AUD_CONNJ1_TIPDET2	49
H28		AUDIO		AUD_CONNJ1_TYPEDET	49 81
H29		AUDIO		AUD_CONNJ2_RING	49 81
H30		AUDIO		AUD_CONNJ2_SLEEVE	49 81
H31		AUDIO		AUD_CONNJ2_SPDIF_IN	49 81
H32		AUDIO		AUD_CONNJ2_TIP	49 81
H33		AUDIO		AUD_CONNJ2_TIPDET	49
H34		AUDIO		AUD_CONNJ2_TYPEDET	49 81
H35		AUDIO		AUD_FILT_HS_MICN	46
H36		AUDIO		AUD_FILT_HS_MICP	46
H37		AUDIO		AUD_HPO_L	46 49
H38		AUDIO		AUD_HPO_R	46 49
H39		AUDIO		AUD_HPO_REFCH	46 49
H40		AUDIO		AUD_HPO_REFCH_XW	49
H41		AUDIO		AUD_HPO_REFUS	46 49
H42		AUDIO		AUD_HPO_REFUS_XW	49
H43		AUDIO		AUD_HPO_TIPDET1	46 49 81
H44		AUDIO		AUD_HPO_TIPDET2	46 49 81
H45		AUDIO		AUD_HPO_TYPEDET	46 49
H46		AUDIO		AUD_HSBIAS	46
H47		AUDIO		AUD_HSBIAS_FILT	46
H48		AUDIO		AUD_HSBIAS_IN	46
H49		AUDIO		AUD_HSBIAS_REF	46
H50		AUDIO		AUD_HS_MICN	46
H51		AUDIO		AUD_HS_MICP	46
H52		AUDIO		AUD_IPHS_SWITCH_EN	14
H53		AUDIO	0V	AUD_LI_GND	48 49
H54		AUDIO		AUD_LI_INL	48 49
H55		AUDIO		AUD_LI_INR	48 49
H56		AUDIO		AUD_LI_LF	48
H57		AUDIO		AUD_LI_RF	48
H58		AUDIO		AUD_LI_TIPDET	46 49 81
H59		AUDIO		AUD_LI_TYPEDET	46 49
H60	1_1_DIFFPAIR	AUDIO		AUD_LO2_L_N	46
H61	1_1_DIFFPAIR	AUDIO		AUD_LO2_L_P	46
H62		AUDIO		AUD_PWR_EN	14
H63		AUDIO		AUD_SPDIF_IN	47 49
H64		AUDIO		AUD_SPDIF_OUT	47 49 81
H65	1_1_DIFFPAIR	AUDIO		AUD_SPKR_N	46 50
H66	1_1_DIFFPAIR	AUDIO		AUD_SPKR_P	46 50
H67		AUDIO		AUD_SPKR_SHDN	47 50
H68		AUDIO		AUD_US_HS_GND	46 49

BT_*

	Physical	Spacing	Netname	
H69	50_OHM_SE	PM	BT_PWR_RST_L	16 32
H70	50_OHM_SE	PM	BT_RESET_MASK_L	20 32
H71	50_OHM_SE	PM	BT_VBUS_EN	32

CIV_*

	Physical	Spacing	Netname	
H72	50_OHM_SE	PM	CIV_ENET_RESET_L	28 31

CODEC_*

	Spacing	Netname	
H73	AUDIO	CODEC_FLYN	46
H74	AUDIO	CODEC_FLYP	46
H75	AUDIO	CODEC_VCOM	46
H76	AUDIO	CODEC_VREF_ADC	46

CPUVR_*

	Physical	Spacing	Netname	
H77	50_OHM_SE	PM	CPUVR_IMON	43 57
H78	SMB_50SE	SMB	CPUVR_ISNS1_N	58
H79	SMB_50SE	SMB	CPUVR_ISNS1_P	58
H80	SMB_50SE	SMB	CPUVR_ISNS2_N	58
H81	SMB_50SE	SMB	CPUVR_ISNS2_P	58

CPU_*

	Physical	Spacing	Netname	
H82	50_OHM_SE	PM	CPU_CATERR_L	3 7 40
H83	50_OHM_SE	PM	CPU_CATERR_RL	3 82
H84	50_OHM_SE	PM	CPU_CFG<0..19>	7 17 81
H85	RCOMP_PHYS	RCOMP_SP	CPU_CFG_RCOMP	7
H86	50_OHM_SE	PM	CPU_MEMVTT_PWR_EN_LSVDDQ	7 53
H87	RCOMP_PHYS	RCOMP_SP	CPU_OPI_RCOMP	7
H88	50_OHM_SE	PECI	CPU_PECI	7 40 41
H89	50_OHM_SE	PECI	CPU_PECI_R	41
H90	50_OHM_SE	PM	CPU_PROCHOT_L	7 40 41 57
H91	50_OHM_SE	PM	CPU_PROCHOT_R_L	7
H92	SMB_50SE	SMB	CPU_PROX_THRM_N	45
H93	SMB_50SE	SMB	CPU_PROX_THRM_P	45
H94	50_OHM_SE	PM	CPU_PWR_DEBUG	9 17 81
H95	RCOMP_PHYS	RCOMP_LG	CPU_SM_RCOMP<0..2>	7
H96	VR_SENSE	VR_SENSE	CPU_VCCSENSE_N	10 57
H97	VR_SENSE	VR_SENSE	CPU_VCCSENSE_P	9 57
H98	VR_SENSE	VR_SENSE	CPU_VCCSENSE_P_R	57
H99	VR_SENSE	VR_SENSE	CPU_VCCSENSE_P_RC	57
H100	50_OHM_SE	PM	CPU_VCCST_PWRGD	9 17 19
H101	50_OHM_SE	SVID_SP	CPU_VIDALERT_L	9 57
H102	50_OHM_SE	SVID_SP	CPU_VIDALERT_R_L	9
H103	50_OHM_SE	SVID_SP	CPU_VIDSCLK	9 57
H104	50_OHM_SE	SVID_SP	CPU_VIDSCLK_R	9
H105	50_OHM_SE	SVID_SP	CPU_VIDSOUT	9 57
H106	50_OHM_SE	SVID_SP	CPU_VIDSOUT_R	9
H107	50_OHM_SE	PM	CPU_VR_EN	9 57
H108	50_OHM_SE	PM	CPU_VR_READY	9 57

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CS4208_*

	Spacing	Netname	
J4	AUDIO	CS4208_HDA_SDOUT0_R	47
J5	AUDIO	CS4208_SPDIF_IN	47
J6	AUDIO	CS4208_SPDIF_OUT	47

DFET_*

	Spacing	Netname	
J4	AUDIO	DFET_OPENCH	47 49
J5	AUDIO	DFET_OPENUS	47 49

DP0GAN0_*

	Physical	Spacing	Netname	
J6	85_OHM_DIFF	DP_DDI1	DP0GAN0	64 82

DP0GAP0_*

	Physical	Spacing	Netname	
J7	85_OHM_DIFF	DP_DDI1	DP0GAP0	64 82

DP1GAN3_*

	Physical	Spacing	Netname	
J8	85_OHM_DIFF	DP_TBTSNK1	DP1GAN3	64 82

DP1GAP3_*

	Physical	Spacing	Netname	
J9	85_OHM_DIFF	DP_TBTSNK1	DP1GAP3	64 82

DP_*

	Physical	Spacing	Netname	
J10	85_OHM_DIFF	TBT_PA	DP_A_LSX_ML_N<1>	66 81
J11	85_OHM_DIFF	TBT_PA	DP_A_LSX_ML_P<1>	66 81
J12	85_OHM_DIFF	TBT_PB	DP_B_LSX_ML_N<1>	67 81
J13	85_OHM_DIFF	TBT_PB	DP_B_LSX_ML_P<1>	67 81
J14	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_AUXCH_C_N	14 68 82
J15	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_AUXCH_C_P	14 68 82
J16	SMB_50SE	SMB	DP_HDMI_TBT_DDC_CLK	14 68
J17	SMB_50SE	SMB	DP_HDMI_TBT_DDC_DATA	14 68
J18	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_ML_C_N<0..3>	6 68 82
J19	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_ML_C_P<0..3>	6 68 82
J20	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_C_N	62 66 82
J21	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_C_P	62 66 82
J22	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_N	66 82

DP_*

	Physical	Spacing	Netname	
J23	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_P	66 82
J24	SMB_50SE	SMB	DP_TBTPA_DDC_CLK	65 66
J25	SMB_50SE	SMB	DP_TBTPA_DDC_DATA	65 66
J26	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_C_N<1..3>	62 66 81 82
J27	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_C_P<1..3>	62 66 81 82
J28	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_N<1..3>	66 82
J29	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_P<1..3>	66 82
J30	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_C_N	62 67 82
J31	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_C_P	62 67 82
J32	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_N	67 82
J33	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_P	67 82
J34	SMB_50SE	SMB	DP_TBTPB_DDC_CLK	65 67
J35	SMB_50SE	SMB	DP_TBTPB_DDC_DATA	65 67
J36	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_C_N<1..3>	62 67 82
J37	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_C_P<1..3>	62 67 82
J38	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_N<1..3>	67 82
J39	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_P<1..3>	67 82
J40	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_C_N	14 62 82
J41	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_C_P	14 62 82
J42	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_N	62 81
J43	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_P	62 81
J44	SMB_50SE	SMB	DP_TBTSNK0_DDC_CLK	14 65 82
J45	SMB_50SE	SMB	DP_TBTSNK0_DDC_DATA	14 65 82
J46	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_C_N<0..3>	6 62 64 82
J47	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_C_P<0..3>	6 62 64 82
J48	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_N<0..3>	62 82
J49	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_P<0..3>	62 82
J50	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_C_N	62 68 81
J51	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_C_P	62 68 81
J52	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_N	62 81
J53	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_P	62 81
J54	SMB_50SE	SMB	DP_TBTSNK1_DDC_CLK	65 68
J55	SMB_50SE	SMB	DP_TBTSNK1_DDC_DATA	65 68
J56	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_C_N<0..3>	62 64 68 82
J57	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_C_P<0..3>	62 64 68 82
J58	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_N<0..3>	62 82
J59	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_P<0..3>	62 82

ENET_*

	Physical	Spacing	Netname	
J60	50_OHM_SE	ENET_2KV	ENET_CENTER_TAP<0..3>	30
J61	50_OHM_SE	CLK	ENET_CLK25M_XTALI	28 29
J62	50_OHM_SE	CLK	ENET_CLK25M_XTALO	28 29
J63	WIDE	ENET_2KV	ENET_CMODE_REF	30
J64	WIDE	ENET	ENET_CONN_CTAP	30
J65	55_OHM_SE	SD	ENET_CR_CLK	28
J66	55_OHM_SE	SD	ENET_CR_CMD	28
J67	55_OHM_SE	SD	ENET_CR_DATA<0..7>	28
J68	55_OHM_SE	SD	ENET_CR_DETECT_L	28 31
J69	55_OHM_SE	SD	ENET_CR_PWREN	28 31
J70	50_OHM_SE	SPI	ENET_CS_L	28
J71	100_OHM_DIFF	ENET	ENET_MDI_N<0..3>	28 30
J72	100_OHM_DIFF	ENET	ENET_MDI_P<0..3>	28 30
J73	100_OHM_DIFF	ENET_2KV	ENET_MDI_TRAN_N<0..3>	30
J74	100_OHM_DIFF	ENET_2KV	ENET_MDI_TRAN_P<0..3>	30
J75	50_OHM_SE	SPI	ENET_MISO	28
J76	50_OHM_SE	SPI	ENET_MOSI	28
J77	50_OHM_SE	SPI	ENET_SCLK	28
J78	50_OHM_SE	PM	ENET_SD_RESET_L	16 31
J79	50_OHM_SE	PM	ENET_WAKE_L	28 29
J80	50_OHM_SE	CLK	ENET_XTAL_OUT_R	29

GND_*

	Physical	Spacing	Voltage	Netname	
J81	POWER	GND_SP	0V	GND	
J82	POWER	GND_SP	0V	GND_AUDIO_CODEC	46 48 49

HDA_*

	Physical	Spacing	Netname	
J83	50_OHM_SE	HDA	HDA_BIT_CLK	13 47
J84	50_OHM_SE	HDA	HDA_BIT_CLK_R	13
J85	50_OHM_SE	HDA	HDA_RST_L	13 47
J86	50_OHM_SE	HDA	HDA_RST_R_L	13
J87	50_OHM_SE	HDA	HDA_SDIN0	13 47
J88	50_OHM_SE	HDA	HDA_SDOUT	13 19 47
J89	50_OHM_SE	HDA	HDA_SDOUT_R	13
J90	50_OHM_SE	HDA	HDA_SYNC	13 47
J91	50_OHM_SE	HDA	HDA_SYNC_R	13

HDMI_*

	Physical	Spacing	Netname	
J92	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CNR_N	70 82
J93	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CNR_P	70 82
J94	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CONN_N	70
J95	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CONN_P	70
J96	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_C_N	68 69 82
J97	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_C_P	68 69 82
J98	100_OHM_DIFF	DP_HDMI	HDMI_CLK_FLT_N	70 82
J99	100_OHM_DIFF	DP_HDMI	HDMI_CLK_FLT_P	70 82
J100	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_LS_N	69 82
J101	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_LS_P	69 82
J102	100_OHM_DIFF	DP_HDMI	HDMI_CLK_N	69 70
J103	100_OHM_DIFF	DP_HDMI	HDMI_CLK_P	69 70
J104	100_OHM_DIFF	DP_HDMI	HDMI_DATA_CONN_N<0..2>	70 82
J105	100_OHM_DIFF	DP_HDMI	HDMI_DATA_CONN_P<0..2>	70 82
J106	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_C_N<0..2>	68 69 82
J107	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_C_P<0..2>	68 69 82
J108	100_OHM_DIFF	DP_HDMI	HDMI_DATA_FLT_N<0..2>	70 82
J109	100_OHM_DIFF	DP_HDMI	HDMI_DATA_FLT_P<0..2>	70 82
J110	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_LS_N<0..2>	69 82
J111	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_LS_P<0..2>	69 82
J112	100_OHM_DIFF	DP_HDMI	HDMI_DATA_N<0..2>	69 70
J113	100_OHM_DIFF	DP_HDMI	HDMI_DATA_P<0..2>	69 70
J114	100_OHM_DIFF	DP_HDMI	HDMI_DAT_CNR_N<0..2>	70 82
J115	100_OHM_DIFF	DP_HDMI	HDMI_DAT_CNR_P<0..2>	70 82
J116	SMB_50SE	SMB	HDMI_DDC_CLK	68 69
J117	SMB_50SE	SMB	HDMI_DDC_CLK_5V	69 70
J118	SMB_50SE	SMB	HDMI_DDC_CLK_CONN	70
J119	SMB_50SE	SMB	HDMI_DDC_CLK_F	70
J120	SMB_50SE	SMB	HDMI_DDC_DATA	68 69
J121	SMB_50SE	SMB	HDMI_DDC_DATA_5V	69 70
J122	SMB_50SE	SMB	HDMI_DDC_DATA_CONN	70
J123	SMB_50SE	SMB	HDMI_DDC_DATA_F	70
J124	SMB_50SE	SMB	HDMI_IDROM_CLK	68 82
J125	SMB_50SE	SMB	HDMI_IDROM_DAT	68 82

AUTO-CONSTRAINTS GENERATED Thu 03/20/14 04:41:10 PM

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Apple Inc.

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IR_*

	Physical	Spacing	Netname
I1	50_OHM_SE	PM	IR_WAKE_L 38

ISNS_*

	Physical	Spacing	Netname
I2	SMB_50SE	SMB	ISNS_1V05_S0_N 43 59
I3	SMB_50SE	SMB	ISNS_1V05_S0_P 43 59
I4	SMB_50SE	SMB	ISNS_5VS4_N 43
I5	SMB_50SE	SMB	ISNS_5VS4_P 43
I6	SMB_50SE	SMB	ISNS_HDD1_N 35 44
I7	SMB_50SE	SMB	ISNS_HDD1_P 35 44
I8	SMB_50SE	SMB	ISNS_HS_CPU_N 44
I9	SMB_50SE	SMB	ISNS_HS_CPU_P 44
I10	SMB_50SE	SMB	ISNS_HS_DDR_N 44
I11	SMB_50SE	SMB	ISNS_HS_DDR_P 44
I12	SMB_50SE	SMB	ISNS_HS_TBT_N 44
I13	SMB_50SE	SMB	ISNS_HS_TBT_P 44
I14	SMB_50SE	SMB	ISNS_P12VG3H_N 44
I15	SMB_50SE	SMB	ISNS_P12VG3H_P 44
I16	SMB_50SE	SMB	ISNS_SSD_N 34 44
I17	SMB_50SE	SMB	ISNS_SSD_P 34 44
I18	SMB_50SE	SMB	ISNS_V1V8S3_N 43
I19	SMB_50SE	SMB	ISNS_V1V8S3_P 43
I20	SMB_50SE	SMB	ISNS_VDDQ_N 43
I21	SMB_50SE	SMB	ISNS_VDDQ_P 43
I22	SMB_50SE	SMB	ISNS_WLAN_N 32 44
I23	SMB_50SE	SMB	ISNS_WLAN_P 32 44

LDO_*

	Physical	Spacing	Netname
I24	AUD_0P2MM	VR_SENSE	LDO_DDRVTTS0_SNS 56 82

LPCPLUS_*

	Physical	Spacing	Netname
I25	50_OHM_SE	PM	LPCPLUS_RESET_L 18 20 81

LPC_*

	Physical	Spacing	Netname
I26	50_OHM_SE	PM	LPC_AD<0..3> 15 18 40 81
I27	50_OHM_SE	PM	LPC_AD_R<0..3> 15
I28	50_OHM_SE	CLK	LPC_CLK24M_LPCPLUS 18 19 81
I29	50_OHM_SE	CLK	LPC_CLK24M_LPCPLUS_R 13 19
I30	50_OHM_SE	CLK	LPC_CLK24M_SMC 19 40
I31	50_OHM_SE	CLK	LPC_CLK24M_SMC_R 13 19
I32	50_OHM_SE	PM	LPC_FRAME_L 15 18 40 81
I33	50_OHM_SE	PM	LPC_FRAME_R_L 15
I34	50_OHM_SE	PM	LPC_PWRDWN_L 14 18 40 81
I35	50_OHM_SE	PM	LPC_SERIRQ 16 18 40 81

LPDDR_*

	Physical	Spacing	Netname
I36	SMB_50SE	SMB	LPDDR_PROX_THRM_N 45
I37	SMB_50SE	SMB	LPDDR_PROX_THRM_P 45

MCP_*

	Physical	Spacing	Netname
I38	RCOMP_PHYS	RCOMP_LG	MCP_EDP_RCOMP 6

MEM_*

	Physical	Spacing	EC set	Netname
I39	MEM_40S	MEM_CMD		MEM_A_CAA<0..9> 8 23 27 82
I40	MEM_40S	MEM_CMD		MEM_A_CAB<0..9> 8 24 27 82
I41	MEM_40S	MEM_CMD		MEM_A_CKE<0..3> 8 23 24 27 82
I42	MEM_70D	MEM_CLK		MEM_A_CLK_N<0..1> 8 23 24 27 81
I43	MEM_70D	MEM_CLK		MEM_A_CLK_P<0..1> 8 23 24 27 81
I44	MEM_40S	MEM_CTRL		MEM_A_CS_L<0..1> 8 23 24 27
I45	40_OHM_SE	MEM_A_DATA_0	MEM_A_DQ_BYTE0	MEM_A_DQ<0..7> 8 21 82
I46	40_OHM_SE	MEM_A_DATA_1	MEM_A_DQ_BYTE1	MEM_A_DQ<8..15> 8 21 82
I47	40_OHM_SE	MEM_A_DATA_2	MEM_A_DQ_BYTE2	MEM_A_DQ<16..23> 8 21 82
I48	40_OHM_SE	MEM_A_DATA_3	MEM_A_DQ_BYTE3	MEM_A_DQ<24..31> 8 21 82
I49	40_OHM_SE	MEM_A_DATA_4	MEM_A_DQ_BYTE4	MEM_A_DQ<32..39> 8 21 82
I50	40_OHM_SE	MEM_A_DATA_5	MEM_A_DQ_BYTE5	MEM_A_DQ<40..47> 8 21 82
I51	40_OHM_SE	MEM_A_DATA_5	MEM_A_DQ_BYTE6	MEM_A_DQ<48..55> 8 21 82
I52	40_OHM_SE	MEM_A_DATA_6	MEM_A_DQ_BYTE7	MEM_A_DQ<56..63> 8 21 82
I53	70_OHM_DIFF	MEM_A_DQS_0	MEM_A_DQS0	MEM_A_DQS_N<0> 8 21
I54	70_OHM_DIFF	MEM_A_DQS_1	MEM_A_DQS1	MEM_A_DQS_N<1> 8 21 82
I55	70_OHM_DIFF	MEM_A_DQS_2	MEM_A_DQS2	MEM_A_DQS_N<2> 8 21 82
I56	70_OHM_DIFF	MEM_A_DQS_3	MEM_A_DQS3	MEM_A_DQS_N<3> 8 21 82
I57	70_OHM_DIFF	MEM_A_DQS_4	MEM_A_DQS4	MEM_A_DQS_N<4> 8 21 82
I58	70_OHM_DIFF	MEM_A_DQS_5	MEM_A_DQS5	MEM_A_DQS_N<5> 8 21 82
I59	70_OHM_DIFF	MEM_A_DQS_6	MEM_A_DQS6	MEM_A_DQS_N<6> 8 21 82
I60	70_OHM_DIFF	MEM_A_DQS_7	MEM_A_DQS7	MEM_A_DQS_N<7> 8 21 82
I61	70_OHM_DIFF	MEM_A_DQS_0	MEM_A_DQS0	MEM_A_DQS_P<0> 8 21
I62	70_OHM_DIFF	MEM_A_DQS_1	MEM_A_DQS1	MEM_A_DQS_P<1> 8 21 82
I63	70_OHM_DIFF	MEM_A_DQS_2	MEM_A_DQS2	MEM_A_DQS_P<2> 8 21 82
I64	70_OHM_DIFF	MEM_A_DQS_3	MEM_A_DQS3	MEM_A_DQS_P<3> 8 21 82
I65	70_OHM_DIFF	MEM_A_DQS_4	MEM_A_DQS4	MEM_A_DQS_P<4> 8 21 82
I66	70_OHM_DIFF	MEM_A_DQS_5	MEM_A_DQS5	MEM_A_DQS_P<5> 8 21 82
I67	70_OHM_DIFF	MEM_A_DQS_6	MEM_A_DQS6	MEM_A_DQS_P<6> 8 21 82
I68	70_OHM_DIFF	MEM_A_DQS_7	MEM_A_DQS7	MEM_A_DQS_P<7> 8 21 82
I69	MEM_40S	MEM_CTRL		MEM_A_ODT0_CPU 8 23 24 27
I70	WIDE			MEM_A_ZQ<0..3> 23 24
I71	MEM_40S	MEM_CMD		MEM_B_CAA<0..9> 8 25 27 82
I72	MEM_40S	MEM_CMD		MEM_B_CAB<0..9> 8 26 27 82
I73	MEM_40S	MEM_CMD		MEM_B_CKE<0..3> 8 25 26 27 82
I74	MEM_70D	MEM_CLK		MEM_B_CLK_N<0..1> 8 25 26 27 81
I75	MEM_70D	MEM_CLK		MEM_B_CLK_P<0..1> 8 25 26 27 81
I76	MEM_40S	MEM_CTRL		MEM_B_CS_L<0..1> 8 25 26 27
I77	40_OHM_SE	MEM_B_DATA_0	MEM_B_DQ_BYTE0	MEM_B_DQ<0..7> 8 21 82
I78	40_OHM_SE	MEM_B_DATA_1	MEM_B_DQ_BYTE1	MEM_B_DQ<8..15> 8 21 82
I79	40_OHM_SE	MEM_B_DATA_2	MEM_B_DQ_BYTE2	MEM_B_DQ<16..23> 8 21 82
I80	40_OHM_SE	MEM_B_DATA_3	MEM_B_DQ_BYTE3	MEM_B_DQ<24..31> 8 21 82
I81	40_OHM_SE	MEM_B_DATA_4	MEM_B_DQ_BYTE4	MEM_B_DQ<32..39> 8 21 82
I82	40_OHM_SE	MEM_B_DATA_5	MEM_B_DQ_BYTE5	MEM_B_DQ<40..47> 8 21 82
I83	40_OHM_SE	MEM_B_DATA_5	MEM_B_DQ_BYTE6	MEM_B_DQ<48..55> 8 21 82
I84	40_OHM_SE	MEM_B_DATA_6	MEM_B_DQ_BYTE7	MEM_B_DQ<56..63> 8 21 82
I85	70_OHM_DIFF	MEM_B_DQS_0	MEM_B_DQS0	MEM_B_DQS_N<0> 8 21 82
I86	70_OHM_DIFF	MEM_B_DQS_1	MEM_B_DQS1	MEM_B_DQS_N<1> 8 21 82
I87	70_OHM_DIFF	MEM_B_DQS_2	MEM_B_DQS2	MEM_B_DQS_N<2> 8 21 82
I88	70_OHM_DIFF	MEM_B_DQS_3	MEM_B_DQS3	MEM_B_DQS_N<3> 8 21 82
I89	70_OHM_DIFF	MEM_B_DQS_4	MEM_B_DQS4	MEM_B_DQS_N<4> 8 21 82
I90	70_OHM_DIFF	MEM_B_DQS_5	MEM_B_DQS5	MEM_B_DQS_N<5> 8 21 82
I91	70_OHM_DIFF	MEM_B_DQS_6	MEM_B_DQS6	MEM_B_DQS_N<6> 8 21 82
I92	70_OHM_DIFF	MEM_B_DQS_7	MEM_B_DQS7	MEM_B_DQS_N<7> 8 21 82
I93	70_OHM_DIFF	MEM_B_DQS_0	MEM_B_DQS0	MEM_B_DQS_P<0> 8 21 82

MEM_*

	Physical	Spacing	EC set	Netname
I94	70_OHM_DIFF	MEM_B_DQS_1	MEM_B_DQS1	MEM_B_DQS_P<1> 8 21 82
I95	70_OHM_DIFF	MEM_B_DQS_2	MEM_B_DQS2	MEM_B_DQS_P<2> 8 21 82
I96	70_OHM_DIFF	MEM_B_DQS_3	MEM_B_DQS3	MEM_B_DQS_P<3> 8 21 82
I97	70_OHM_DIFF	MEM_B_DQS_4	MEM_B_DQS4	MEM_B_DQS_P<4> 8 21 82
I98	70_OHM_DIFF	MEM_B_DQS_5	MEM_B_DQS5	MEM_B_DQS_P<5> 8 21 82
I99	70_OHM_DIFF	MEM_B_DQS_6	MEM_B_DQS6	MEM_B_DQS_P<6> 8 21 82
I100	70_OHM_DIFF	MEM_B_DQS_7	MEM_B_DQS7	MEM_B_DQS_P<7> 8 21 82
I101	MEM_40S	MEM_CTRL		MEM_B_ODT0_CPU 8 25 26 27
I102	WIDE			MEM_B_ZQ<0..3> 25 26

NC_*

	Physical	Spacing	No test	Netname
I103	SMB_50SE	SMB	TRUE	NC_CLINK_CLK 15
I104	SMB_50SE	SMB	TRUE	NC_CLINK_DATA 15
I105			TRUE	NC_CLINK_RESET_L 15
I106			TRUE	NC_DP_INT_AUXCH_CN 6
I107			TRUE	NC_DP_INT_AUXCH_CP 6
I108			TRUE	NC_DP_INT_ML_CN0 6
I109			TRUE	NC_DP_INT_ML_CN1 6
I110			TRUE	NC_DP_INT_ML_CN2 6
I111			TRUE	NC_DP_INT_ML_CN3 6
I112			TRUE	NC_DP_INT_ML_CP0 6
I113			TRUE	NC_DP_INT_ML_CP1 6
I114			TRUE	NC_DP_INT_ML_CP2 6
I115			TRUE	NC_DP_INT_ML_CP3 6
I116			TRUE	NC_DP_TBTSRC_AUXCH_CN 62
I117			TRUE	NC_DP_TBTSRC_AUXCH_CP 62
I118			TRUE	NC_DP_TBTSRC_ML_CN<0..3> 62
I119			TRUE	NC_DP_TBTSRC_ML_CP<0..3> 62
I120			TRUE	NC_EDP_BKLT_PWM 14
I121			TRUE	NC_EDP_DISP_UTIL 6
I122			TRUE	NC_ENET_CE_L_MS_INS_L 28
I123			TRUE	NC_ITPXDP_CLK100MN 13
I124			TRUE	NC_ITPXDP_CLK100MP 13
I125			TRUE	NC_MEM_A_RSVD1 8
I126			TRUE	NC_MEM_A_RSVD2 8
I127			TRUE	NC_MEM_B_RSVD3 8
I128			TRUE	NC_MEM_B_RSVD4 8
I129			TRUE	NC_MEM_EVENT_L 40
I130			TRUE	NC_MEM_RESET_L 7
I131			TRUE	NC_MEM_VDD_SEL_1V5_L 16
I132			TRUE	NC_PCH_I2S1_SCLK 13
I133			TRUE	NC_PCH_I2S1_SFRM 13
I134			TRUE	NC_PCH_I2S1_TXD 13
I135			TRUE	NC_PCIE_CLK100M_CAMERAN 13
I136			TRUE	NC_PCIE_CLK100M_CAMERAP 13
I137			TRUE	NC_SATA_B_D2RN 13
I138			TRUE	NC_SATA_B_D2RP 13
I139			TRUE	NC_SATA_B_R2D_CN 13
I140			TRUE	NC_SATA_B_R2D_CP 13
I141			TRUE	NC_SMBUS_SMC_0_S0_SCL 40 42
I142			TRUE	NC_SMBUS_SMC_0_S0_SDA 40 42
I143			TRUE	NC_SMBUS_SMC_2_S3_SCL 40 42
I144			TRUE	NC_SMBUS_SMC_2_S3_SDA 40 42
I145			TRUE	NC_SMBUS_SMC_3_SCL 40 42
I146			TRUE	NC_SMBUS_SMC_3_SDA 40 42
I147			TRUE	NC_SMBUS_SMC_4_ASF_SCL 40 42
I148			TRUE	NC_SMBUS_SMC_4_ASF_SDA 40 42
I149			TRUE	NC_SMBUS_SMC_5_G3_SCL 40 42
I150			TRUE	NC_SMBUS_SMC_5_G3_SDA 40 42
I151			TRUE	NC_SMC_ADAPTER_EN 40
I152			TRUE	NC_SMC_ADC20 40
I153			TRUE	NC_SMC_ADC22 40
I154			TRUE	NC_SMC_ADC23 40
I155			TRUE	NC_SMC_BATLOW_L 40
I156			TRUE	NC_SMC_FAN_1_CTL 40
I157			TRUE	NC_SMC_FAN_1_TACH 40
I158			TRUE	NC_SMC_GFX_OVERTEMP
I159			TRUE	NC_SMC_GFX_THROTTLE_L 40
I160			TRUE	NC_SMC_HIB_L 40

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NC_*

	Physical	Spacing	No test	Netname	
H1			TRUE	NC_SMC_MD1	18
H4			TRUE	NC_SMC_PN3	40
H5			TRUE	NC_SMC_PN4	40
H6			TRUE	NC_SMC_PN5	40
H8			TRUE	NC_SMC_PN7	40
H9			TRUE	NC_SMC_TRST_L	18
H7			TRUE	NC_SMC_VDDRS3_ISENSE	40
H3			TRUE	NC_SMC_VDDRS3_VSENSE	40
H2			TRUE	NC_SMC_XOSC1	40
H10			TRUE	NC_SPI_CS2_L	15
H11			TRUE	NC_SPI_IO2	15
H12			TRUE	NC_SPI_IO3	15
H13			TRUE	NC_USB_5N	15
H14			TRUE	NC_USB_5P	15
H15			TRUE	NC_USB_SMCN	40
H16			TRUE	NC_USB_TPADN	15
H17			TRUE	NC_USB_TPADP	15

PCH_*

	Physical	Spacing	Netname	
H18	50_OHM_SE	CLK	PCH_CLK24M_XTALIN	13 19
H19	50_OHM_SE	CLK	PCH_CLK24M_XTALOUT	13 19
H20	50_OHM_SE	CLK	PCH_CLK24M_XTALOUT_R	19
H21	50_OHM_SE	CLK	PCH_CLK32K_RTCX1	13 19
H22	50_OHM_SE	CLK	PCH_CLK32K_RTCX2	13 19
H23	50_OHM_SE	CLK	PCH_CLK32K_RTCX2_R	19
H24	50_OHM_SE	PM	PCH_JTAGX	13 17
H25	RCOMP_PHYS	RCOMP_SP	PCH_OPI_COMP	16
H26	RCOMP_PHYS	RCOMP_SP	PCH_PCIE_RCOMP	15
H27	RCOMP_PHYS	RCOMP_SP	PCH_SATA_RCOMP	13
H28	50_OHM_SE	CLK	PCH_SRTCRST_L	13
H29	50_OHM_SE	PM	PCH_SUSWARN_L	14 40
H30	50_OHM_SE	PM	PCH_TBT_PCIE_RESET_L	16 62
H31	RCOMP_PHYS	RCOMP_SP	PCH_TD_IREF	7

PCIE_*

	Physical	Spacing	Netname	
H32	85_OHM_DIFF	PE_AP2CPU	PCIE_AP_D2R_N	15 32 81
H33	85_OHM_DIFF	PE_AP2CPU	PCIE_AP_D2R_P	15 32 81
H34	85_OHM_DIFF	PE_CPU2AP	PCIE_AP_R2D_C_N	15 32
H35	85_OHM_DIFF	PE_CPU2AP	PCIE_AP_R2D_C_P	15 32
H36	85_OHM_DIFF	PE_CPU2AP	PCIE_AP_R2D_N	32 81
H37	85_OHM_DIFF	PE_CPU2AP	PCIE_AP_R2D_P	32 81
H38	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_ANA_N	13
H39	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_ANA_P	13
H40	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_AP_CONN_N	32 81
H41	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_AP_CONN_P	32 81
H42	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_AP_N	13 32
H43	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_AP_P	13 32
H44	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_ENETSD_N	13 28
H45	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_ENETSD_P	13 28
H46	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_SSD_F_N	34 81
H47	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_SSD_F_P	34 81
H48	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_SSD_N	13 34
H49	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_SSD_P	13 34
H50	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_TBT_N	13 62
H51	85_OHM_DIFF	DIFF_CLK	PCIE_CLK100M_TBT_P	13 62
H52	85_OHM_DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_C_N	28
H53	85_OHM_DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_C_P	28
H54	85_OHM_DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_N	15 28
H55	85_OHM_DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_P	15 28
H56	85_OHM_DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_C_N	15 28
H57	85_OHM_DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_C_P	15 28
H58	85_OHM_DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_N	28

PCIE_*

	Physical	Spacing	Netname	
H59	85_OHM_DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_P	28
H60	85_OHM_DIFF	PE_SSD2CPU	PCIE_SSD_D2R_N<0..1>	13 34 81
H61	85_OHM_DIFF	PE_SSD2CPU	PCIE_SSD_D2R_P<0..1>	13 34 81
H62	85_OHM_DIFF	PE_CPU2SSD	PCIE_SSD_R2D_C_N<0..1>	13 34
H63	85_OHM_DIFF	PE_CPU2SSD	PCIE_SSD_R2D_C_P<0..1>	13 34
H64	85_OHM_DIFF	PE_CPU2SSD	PCIE_SSD_R2D_N<0..1>	34 81
H65	85_OHM_DIFF	PE_CPU2SSD	PCIE_SSD_R2D_P<0..1>	34 81
H66	85_OHM_DIFF	PE_TBT2CPU	PCIE_TBT_D2R_C_N<0..3>	62 81
H67	85_OHM_DIFF	PE_TBT2CPU	PCIE_TBT_D2R_C_P<0..3>	62 81
H68	85_OHM_DIFF	PE_TBT2CPU	PCIE_TBT_D2R_N<0..3>	15 62
H69	85_OHM_DIFF	PE_TBT2CPU	PCIE_TBT_D2R_P<0..3>	15 62
H70	85_OHM_DIFF	PE_CPU2TBT	PCIE_TBT_R2D_C_N<0..3>	15 62 81 82
H71	85_OHM_DIFF	PE_CPU2TBT	PCIE_TBT_R2D_C_P<0..3>	15 62 81 82
H72	85_OHM_DIFF	PE_CPU2TBT	PCIE_TBT_R2D_N<0..3>	62 82
H73	85_OHM_DIFF	PE_CPU2TBT	PCIE_TBT_R2D_P<0..3>	62 82
H74	50_OHM_SE	PM	PCIE_WAKE_L	14 29 32

PD_*

	Physical	Spacing	Netname	
H75		AUDIO	PD_CODEC_GPIO1	47
H76		AUDIO	PD_CODEC_GPIO2	47
H77		AUDIO	PD_CODEC_GPIO3	47
H78	SMB_50SE	AUDIO	PD_CODEC_SCL	47
H79	SMB_50SE	AUDIO	PD_CODEC_SDA	47

PGND_*

	Physical	Spacing	Voltage	Netname	
H80	VR_CTL	GND_SP	0V	PGND_REG_P1V2_S3	56

PLT_*

	Physical	Spacing	Netname	
H81	50_OHM_SE	PM	PLT_RESET_L	14 16 17 20

PM_*

	Physical	Spacing	Netname	
H82	50_OHM_SE	PM	PM_BATLOW_L	14
H83	50_OHM_SE	PM	PM_CLK32K_SUSCLK_R	14 41
H84	50_OHM_SE	PM	PM_CLKRUN_L	14 18 40 81
H85	50_OHM_SE	PM	PM_DSW_PWRGD	40 41
H86	50_OHM_SE	PM	PM_ENET_EN_L	29
H87	50_OHM_SE	PM	PM_EN_FET_P3V3_S0	34 52 54
H88	50_OHM_SE	PM	PM_EN_FET_P3V3_S0_R	54
H89	50_OHM_SE	PM	PM_EN_FET_P3V3_S4	52 53
H90	50_OHM_SE	PM	PM_EN_FET_P3V3_S5	52 53
H91	50_OHM_SE	PM	PM_EN_FET_P5V_S0	52 54
H92	50_OHM_SE	PM	PM_EN_FET_P5V_S0_D	54
H93	50_OHM_SE	PM	PM_EN_LDO_S3_DDRVTT_R	56
H94	50_OHM_SE	PM	PM_EN_P0V6_DDRVTT	53 56
H95	50_OHM_SE	PM	PM_EN_P1V8S3_R	53
H96	50_OHM_SE	PM	PM_EN_REG_P1V05_S0	54 59
H97	50_OHM_SE	PM	PM_EN_REG_P1V05_S0_D	54
H98	50_OHM_SE	PM	PM_EN_REG_P1V05_S0_R	59

PM_*

	Physical	Spacing	Netname	
H99	50_OHM_SE	PM	PM_EN_REG_P1V2_S3	53 56
H100	50_OHM_SE	PM	PM_EN_REG_P1V2_S3_R	56
H101	50_OHM_SE	PM	PM_EN_REG_P1V5_S0	54 60
H102	50_OHM_SE	PM	PM_EN_REG_P1V8_S3	53 56
H103	50_OHM_SE	PM	PM_EN_REG_P1V8_S3_D	53
H104	50_OHM_SE	PM	PM_EN_REG_P5V_S4	53 55
H105	50_OHM_SE	PM	PM_EN_S0	54
H106	50_OHM_SE	PM	PM_EN_USB_PWR	36 37 53
H107	50_OHM_SE	PM	PM_P3V3_G3H_PG	41 53 55
H108	50_OHM_SE	PM	PM_PCH_PWROK	14 54
H109	50_OHM_SE	PM	PM_PCH_SYS_PWROK	14 17 40 54
H110	50_OHM_SE	PM	PM_PCH_SYS_PWROK_R	54
H111	50_OHM_SE	PM	PM_PGOOD_FET_P3V3_S0	54
H112	50_OHM_SE	PM	PM_PGOOD_FET_P3V3_S0_R	54
H113	50_OHM_SE	PM	PM_PGOOD_FET_P5V_S0	54
H114	50_OHM_SE	PM	PM_PGOOD_REG_P1V05_S0	54 59
H115	50_OHM_SE	PM	PM_PGOOD_REG_P1V2_S3	53 54 56
H116	50_OHM_SE	PM	PM_PGOOD_REG_P1V5_S0	54 60
H117	50_OHM_SE	PM	PM_PGOOD_REG_P1V8_S3	53 56
H118	50_OHM_SE	PM	PM_PGOOD_REG_P5V_S4	53 55
H119	50_OHM_SE	PM	PM_PWRBTN_L	14 17 40
H120	50_OHM_SE	PM	PM_RSMRSTPCH_LR	41
H121	50_OHM_SE	PM	PM_RSMRST_PCH_L	14 41
H122	50_OHM_SE	PM	PM_SLP_G3S_EN	32 53 64 66 67
H123	50_OHM_SE	PM	PM_SLP_S3_L	14 29 40 44 54 66 67 69 70
H124	50_OHM_SE	PM	PM_SLP_S4_L	14 40 53
H125	50_OHM_SE	PM	PM_SLP_S5_L	14 38 40 52 53
H126	50_OHM_SE	PM	PM_SLP_S5_RD_L	53
H127	50_OHM_SE	PM	PM_SLP_SUS_L	14
H128	50_OHM_SE	PM	PM_SYSRST_L	14 19 40
H129	50_OHM_SE	PM	PM_TBTPOC_EN_L	64
H130	50_OHM_SE	PM	PM_THRMTRIP_B_L	41
H131	50_OHM_SE	PM	PM_THRMTRIP_L	16 41
H132	50_OHM_SE	PM	PM_WLAN_EN_L	32

PP0V6_*

	Physical	Spacing	Voltage	Netname	
H133	WIDE	POWER_SP	0.6V	PP0V6_S3_DDRVTT	4 27 56

PP12V_*

	Physical	Spacing	Voltage	Netname	
H134	HI_PWR	POWER_SP	12V	PP12V_G3H	3 44 51 55 59 60 61
H135	HI_PWR	POWER_SP	12V	PP12V_G3H_CPU	3 44 57 58
H136	HI_PWR	POWER_SP	12V	PP12V_G3H_DDR	3 44 56
H137	HI_PWR	POWER_SP	12V	PP12V_G3H_PSU	3 44 61 81
H138	HI_PWR	POWER_SP	12V	PP12V_G3H_TBT	3 44 66 67
H139	POWER	POWER_SP	12V	PP12V_S0_FAN	51
H140	POWER	POWER_SP	12V	PP12V_S0_FAN0_F	51 81

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PP1V05_*

	Physical	Spacing	Voltage	Netname	
I4	POWER	POWER_SP	1.05V	PP1V05_S0	81 2 7 9 12 16 17 19 41 43 57 66

PP4V5_*

	Physical	Spacing	Voltage	Netname	
F23	POWER	POWER_SP	4.5V	PP4V5_AUDIO_ANALOG	46

PSU_*

	Physical	Spacing	Netname	
H47	50_OHM_SE	PM	PSU_TEMP	40 61 81

PP1V2_*

	Physical	Spacing	Voltage	Netname	
I2	WIDE	POWER_SP	1.2V	PP1V2_ENET	3 28 29
I3	POWER	POWER_SP	1.2V	PP1V2_S3_MEM	4 9 11 22 23 24 25 26 43 53 61
I4	POWER	POWER_SP	1.2V	PP1V2_S3_REG	4 43 56

PP5V_*

	Physical	Spacing	Voltage	Netname	
F24	WIDE	POWER_SP	5V	PP5V_G3H	3 38 39 41 55 60
F25	WIDE	POWER_SP	5V	PP5V_G3H_LDO	60
F26	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_CONN	70
F27	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_FUSE	70
F28	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_S0	70
F29	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_S0_F	70
F30	POWER	POWER_SP	5V	PP5V_S0	58 81 2 17 18 19 35 46 50 52 54 57
I31	POWER	POWER_SP	5V	PP5V_S0_AUDIO_XW	46
I32	POWER	POWER_SP	5V	PP5V_S0_SKPRAMP	50
I33	POWER	POWER_SP	5V	PP5V_S4	4 36 37 39 43 52 56 59 69 70
I34	WIDE	POWER_SP	5V	PP5V_S4_EXTA_F	36
I35	WIDE	POWER_SP	5V	PP5V_S4_EXTA_ILIM	36
I36	WIDE	POWER_SP	5V	PP5V_S4_EXTB_F	36
I37	WIDE	POWER_SP	5V	PP5V_S4_EXTB_ILIM	36
I38	WIDE	POWER_SP	5V	PP5V_S4_EXTC_F	37
I39	WIDE	POWER_SP	5V	PP5V_S4_EXTC_ILIM	37
I40	WIDE	POWER_SP	5V	PP5V_S4_EXTD_F	37
I41	WIDE	POWER_SP	5V	PP5V_S4_EXTD_ILIM	37
I42	POWER	POWER_SP	5V	PP5V_S4_REG	4 43 55

REG_*

	Physical	Spacing	Di/Dt	Netname	
H48	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V05S0	59
H49	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V05S0_RC	59
H50	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V2_S3	56
H51	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V2_S3_RC	56
H52	VR_GATE	VR_LG	TRUE	REG_LGATE_P1V05S0	59
H53	VR_GATE	VR_LG	TRUE	REG_LGATE_P1V2_S3	56
H54	50_OHM_SE			REG_P1V2_S3_MODE	56
H55	VR_CTL			REG_P1V2_S3_REFIN	56
H56	50_OHM_SE			REG_P1V2_S3_TRIP	56
H57	VR_CTL			REG_P1V2_S3_VDDQSNS	56
H58	VR_CTL			REG_P1V2_S3_VREF	56
H59	VR_CTL			REG_P1V2_S3_VTTREF	56
H60	VR_CTL			REG_P1V2_V5IN	56
H61	VR_PHASE	VR_PHASE	TRUE	REG_PHASE_P1V05S0	59
H62	VR_PHASE	VR_PHASE	TRUE	REG_PHASE_P1V05S0_L	59
H63	AUD_0P5MM	VR_PHASE	TRUE	REG_PHASE_P1V2_S3	56
H64	AUD_0P5MM	VR_PHASE	TRUE	REG_PHASE_P1V2_S3_L	56
H65	VR_CTL	VR_PHASE	TRUE	REG_SNUBBER_P1V05S0	59 82
H66	VR_PHASE	VR_PHASE	TRUE	REG_SNUBBER_P1V2_S3	56
H67	VR_GATE	VR_UG	TRUE	REG_UGATE_P1V05S0	59
H68	VR_GATE	VR_UG	TRUE	REG_UGATE_P1V05S0_R	59
H69	VR_GATE	VR_UG	TRUE	REG_UGATE_P1V2_S3	56

PP1V5_*

	Physical	Spacing	Voltage	Netname	
I6	POWER	POWER_SP	1.5V	PP1V5_S0	4 9 12 19 35 47 60 61 69
I8	WIDE	POWER_SP	1.5V	PP1V5_S0_AUDIO_DIG	47

PP1V8_*

	Physical	Spacing	Voltage	Netname	
I7	POWER	POWER_SP	1.8V	PP1V8_S3	4 23 24 25 26 43 60
I9	POWER	POWER_SP	1.8V	PP1V8_S3_P1V5_LDO	60
I5	POWER	POWER_SP	1.8V	PP1V8_S3_REG	4 43 56

PPHV_*

	Physical	Spacing	Voltage	Netname	
F45	WIDE	POWER_SP	12V	PPHV_SW_TBT_A_PWR	66
F44	WIDE	POWER_SP	12V	PPHV_SW_TBT_B_PWR	67

RTCPWR_*

	Physical	Spacing	Netname	
H70	50_OHM_SE	PM	RTCPWR_GT	19

PP3V3RHV_*

	Physical	Spacing	Voltage	Netname	
H10	WIDE	POWER_SP	12V	PP3V3RHV_SW_TBT_A_PWR	66
H11	WIDE	POWER_SP	12V	PP3V3RHV_SW_TBT_B_PWR	67

PPVBATT_*

	Physical	Spacing	Voltage	Netname	
F49	WIDE	POWER_SP	3.3V	PPVBATT_G3_RTC	3 19 81

RTC_*

	Physical	Spacing	Netname	
H73	50_OHM_SE	PM	RTC_RESET_L	13 41
H72	50_OHM_SE	PM	RTC_RESET_L_R	41

PP3V3_*

	Physical	Spacing	Voltage	Netname	
H12	POWER	POWER_SP	3.3V	PP3V3_ENET	3 28 29
H13	POWER	POWER_SP	3.3V	PP3V3_G3H	52 53 55 56 64 66 67 3 19 29 32 34 36 39 40 41
H14	WIDE	POWER_SP	3.3V	PP3V3_G3_RTC	13 14 19
H15	POWER	POWER_SP	3.3V	PP3V3_S0	61 63 65 68 69 81 24 35 41 42 43 3 4 9 12 33 34 I46
H16	WIDE	POWER_SP	3.3V	PP3V3_S0_AUDIO_ANALOG	46
H17	POWER	POWER_SP	3.3V	PP3V3_S0_SSD_FET	34
H18	POWER	POWER_SP	3.3V	PP3V3_S4	3 4 16 31 32 38 41 52 53 54 70
H19	POWER	POWER_SP	3.3V	PP3V3_S5	3 9 12 14 15 16 17 18 19 52 53 54 60 81
H20	WIDE	POWER_SP	3.3V	PP3V3_SW_SD_PWR	31
H21	WIDE	POWER_SP	3.3V	PP3V3_SW_TBT_A_PWR	66
H22	WIDE	POWER_SP	3.3V	PP3V3_SW_TBT_B_PWR	67

PPVCC_*

	Physical	Spacing	Voltage	Netname	
F46	POWER	POWER_SP	1.25V	PPVCC_S0_CPU	4 9 11 43 58

S5_*

	Physical	Spacing	Netname	
H71	50_OHM_SE	PM	S5_PWRGD	40 53

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SATA_*

	Physical	Spacing	Netname	
H1	85_OHM_DIFF	SATA	SATA_A_D2R_CONN_N	35
H2	85_OHM_DIFF	SATA	SATA_A_D2R_CONN_P	35
H3	85_OHM_DIFF	SATA	SATA_A_D2R_DF_N	35
H4	85_OHM_DIFF	SATA	SATA_A_D2R_DF_P	35
H5	85_OHM_DIFF	SATA	SATA_A_D2R_N	13 35 81
H6	85_OHM_DIFF	SATA	SATA_A_D2R_P	13 35 81
H7	85_OHM_DIFF	SATA	SATA_A_R2D_CONN_N	35
H8	85_OHM_DIFF	SATA	SATA_A_R2D_CONN_P	35
H9	85_OHM_DIFF	SATA	SATA_A_R2D_C_N	13 35 81
H10	85_OHM_DIFF	SATA	SATA_A_R2D_C_P	13 35 81
H11	85_OHM_DIFF	SATA	SATA_A_R2D_DF_N	35
H12	85_OHM_DIFF	SATA	SATA_A_R2D_DF_P	35

SDCONN_*

	Physical	Spacing	Netname	
H13	55_OHM_SE	SD	SDCONN_CLK	28 31
H14	55_OHM_SE	SD	SDCONN_CLK_R	31
H15	55_OHM_SE	SD	SDCONN_CMD	28 31
H16	55_OHM_SE	SD	SDCONN_CMD_R	31
H17	55_OHM_SE	SD	SDCONN_DATA<0..7>	28 31
H18	55_OHM_SE	SD	SDCONN_DATA_R<0..7>	31
H19	55_OHM_SE	SD	SDCONN_DETECT	31
H20	55_OHM_SE	SD	SDCONN_DETECT_LVL	31
H21	55_OHM_SE	SD	SDCONN_WP	28 31

SLG_*

	Physical	Spacing	Netname	
H22	50_OHM_SE	PM	SLG_ENET_RESET_L	31
H23	50_OHM_SE	PM	SLG_ENET_RESET_R_L	31

SMBUS_*

	Physical	Spacing	Netname	
H24	SMB_50SE	SMB	SMBUS_PCH_CLK	15 42
H25	SMB_50SE	SMB	SMBUS_PCH_DATA	15 42
H26	SMB_50SE	SMB	SMBUS_SMC_1_S0_SCL	40 42
H27	SMB_50SE	SMB	SMBUS_SMC_1_S0_SDA	40 42

SMB_*

	Physical	Spacing	Netname	
H28	SMB_50SE	SMB	SMB_CPU_XDP_SCL	17 42 81
H29	SMB_50SE	SMB	SMB_CPU_XDP_SDA	17 42 81
H30	SMB_50SE	SMB	SMB_PCH_STR_SCL	42
H31	SMB_50SE	SMB	SMB_PCH_STR_SDA	42
H32	SMB_50SE	SMB	SMB_SMC_1_STR_SCL	42
H33	SMB_50SE	SMB	SMB_SMC_1_STR_SDA	42
H34	SMB_50SE	SMB	SMB_THMSNS1_SCL	42 45
H35	SMB_50SE	SMB	SMB_THMSNS1_SDA	42 45

SMC_*

	Physical	Spacing	Netname	
H36	50_OHM_SE	PM	SMC_ASSERT_RTCRST	19 40 41
H37	50_OHM_SE	CLK	SMC_CLK32K	40 41
H38	50_OHM_SE	PM	SMC_DELAYED_PWRGD	40 41 54 63
H39	50_OHM_SE	PM	SMC_G3_WAKESRC_EN	40 41 53
H40	50_OHM_SE	PM	SMC_LRESET_L	20 40
H41	50_OHM_SE	PECI	SMC_PECI_L	40 41
H42	50_OHM_SE	PECI	SMC_PECI_L_R	41
H43	50_OHM_SE	PM	SMC_PME_S4_WAKE_L	32 38 40 41
H44	50_OHM_SE	PM	SMC_PM_G2_EN	40 41 53
H45	50_OHM_SE	PM	SMC_WAKE_L	40
H46	50_OHM_SE	CLK	SMC_XTAL	40 41
H47	50_OHM_SE	CLK	SMC_XTAL_R	41

SML_*

	Physical	Spacing	Netname	
H48	SMB_50SE	SMB	SML_PCH_0_CLK	15 42
H49	SMB_50SE	SMB	SML_PCH_0_DATA	15 42
H50	SMB_50SE	SMB	SML_PCH_1_CLK	15 42
H51	SMB_50SE	SMB	SML_PCH_1_DATA	15 42

SPIROM_*

	Physical	Spacing	Netname	
H52	50_OHM_SE	SPI	SPIROM_USE_MLB	16 18 81
H53	50_OHM_SE	SPI	SPIROM_WP_L	18

SPI_*

	Physical	Spacing	Netname	
H54	50_OHM_SE	SPI	SPI_ALT_CLK	18 81
H55	50_OHM_SE	SPI	SPI_ALT_CS_L	18 81
H56	50_OHM_SE	SPI	SPI_ALT_MISO	18 81
H57	50_OHM_SE	SPI	SPI_ALT_MOSI	18 81
H58	50_OHM_SE	SPI	SPI_CLK	18
H59	50_OHM_SE	SPI	SPI_CLK_R	15 18
H60	50_OHM_SE	SPI	SPI_CS0_L	18
H61	50_OHM_SE	SPI	SPI_CS0_R_L	15 18
H62	50_OHM_SE	SPI	SPI_DESCRIPTOR_OVERRIDE	19
H63	50_OHM_SE	SPI	SPI_DESCRIPTOR_OVERRIDE_L	19 40
H64	50_OHM_SE	SPI	SPI_DESCRIPTOR_OVERRIDE_LS5V	19
H65	50_OHM_SE	SPI	SPI_MISO	15 18
H66	50_OHM_SE	SPI	SPI_MLB_CLK	18
H67	50_OHM_SE	SPI	SPI_MLB_CS_L	18
H68	50_OHM_SE	SPI	SPI_MLB_MISO	18
H69	50_OHM_SE	SPI	SPI_MLB_MOSI	18
H70	50_OHM_SE	SPI	SPI_MOSI	18
H71	50_OHM_SE	SPI	SPI_MOSI_R	15 18
H72	50_OHM_SE	SPI	SPI_SMC_CLK	18 40
H73	50_OHM_SE	SPI	SPI_SMC_CS_L	18 40
H74	50_OHM_SE	SPI	SPI_SMC_MISO	18 40
H75	50_OHM_SE	SPI	SPI_SMC_MOSI	18 40

SPKRAMP_*

	Physical	Spacing	Netname	
H76	1_1_DIFFPAIR	AUDIO	SPKRAMP_IN_N	50
H77	1_1_DIFFPAIR	AUDIO	SPKRAMP_IN_P	50
H78	AUD_0P5MM		SPKRAMP_N_OUT	50 81
H79	AUD_0P5MM		SPKRAMP_P_OUT	50 81

SSD_*

	Physical	Spacing	Netname	
H80	50_OHM_SE	PM	SSD_RESET_L	16 34 81

TBT_*

	Physical	Spacing	Netname	
H81	85_OHM_DIFF	TBT_PA	TBT_A_D2R1_AUXDDC_N	66 81
H82	85_OHM_DIFF	TBT_PA	TBT_A_D2R1_AUXDDC_P	66 81
H83	85_OHM_DIFF	TBT_PA	TBT_A_D2R_C_N<0..1>	66 81 82
H84	85_OHM_DIFF	TBT_PA	TBT_A_D2R_C_P<0..1>	66 81 82
H85	85_OHM_DIFF	TBT_PA	TBT_A_D2R_N<0..1>	62 66 81
H86	85_OHM_DIFF	TBT_PA	TBT_A_D2R_P<0..1>	62 66 81
H87	50_OHM_SE	SMB	TBT_A_LSRX	62 66 82
H88	50_OHM_SE	SMB	TBT_A_LSTX	62 66 82
H89	85_OHM_DIFF	TBT_PA	TBT_A_R2D_C_N<0..1>	62 66 81 82
H90	85_OHM_DIFF	TBT_PA	TBT_A_R2D_C_P<0..1>	62 66 81 82
H91	85_OHM_DIFF	TBT_PA	TBT_A_R2D_N<0..1>	66 82
H92	85_OHM_DIFF	TBT_PA	TBT_A_R2D_P<0..1>	66 82
H93	85_OHM_DIFF	TBT_PB	TBT_B_D2R1_AUXDDC_N	67 81
H94	85_OHM_DIFF	TBT_PB	TBT_B_D2R1_AUXDDC_P	67 81
H95	85_OHM_DIFF	TBT_PB	TBT_B_D2R_C_N<0..1>	67 81 82
H96	85_OHM_DIFF	TBT_PB	TBT_B_D2R_C_P<0..1>	67 81 82
H97	85_OHM_DIFF	TBT_PB	TBT_B_D2R_N<0..1>	62 67 81
H98	85_OHM_DIFF	TBT_PB	TBT_B_D2R_P<0..1>	62 67 81
H99	50_OHM_SE	SMB	TBT_B_LSRX	62 67 82
H100	50_OHM_SE	SMB	TBT_B_LSTX	62 67 82
H101	85_OHM_DIFF	TBT_PB	TBT_B_R2D_C_N<0..1>	62 67 81 82
H102	85_OHM_DIFF	TBT_PB	TBT_B_R2D_C_P<0..1>	62 67 81 82
H103	85_OHM_DIFF	TBT_PB	TBT_B_R2D_N<0..1>	67 82
H104	85_OHM_DIFF	TBT_PB	TBT_B_R2D_P<0..1>	67 82
H105	50_OHM_SE	CLK	TBT_CLK25M_IN	62
H106	50_OHM_SE	CLK	TBT_CLK25M_OUT	62
H107	50_OHM_SE	CLK	TBT_CLK25M_OUT_R	62 82
H108	50_OHM_SE	SPI	TBT_SPI_CLK	62
H109	50_OHM_SE	SPI	TBT_SPI_CS_L	62
H110	50_OHM_SE	SPI	TBT_SPI_MISO	62
H111	50_OHM_SE	SPI	TBT_SPI_MOSI	62
H112	SMB_50SE	SMB	TBT_THERM_N	45 63
H113	SMB_50SE	SMB	TBT_THERM_P	45 62
H114	50_OHM_SE	PM	TBT_WAKE_L	41 62 64

TP_*

	Spacing	Netname	
H115	AUDIO	TP_AUD_SENSEB2	46

U6300_*

	Spacing	Netname	
H116	AUDIO	U6300_GAIN	50

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USB2_*

	Physical	Spacing	Netname	
I41	85_OHM_DIFF	USB	USB2_EXTA_F_N	36
I42	85_OHM_DIFF	USB	USB2_EXTA_F_P	36
I43	85_OHM_DIFF	USB	USB2_EXTA_MUXED_N	36
I44	85_OHM_DIFF	USB	USB2_EXTA_MUXED_P	36
I45	85_OHM_DIFF	USB	USB2_EXTB_F_N	36
I46	85_OHM_DIFF	USB	USB2_EXTB_F_P	36
I47	85_OHM_DIFF	USB	USB2_EXTC_F_N	37
I48	85_OHM_DIFF	USB	USB2_EXTC_F_P	37
I49	85_OHM_DIFF	USB	USB2_EXTD_F_N	37
I410	85_OHM_DIFF	USB	USB2_EXTD_F_P	37

USB3_*

	Physical	Spacing	Netname	
I411	85_OHM_DIFF	USB3	USB3_EXTA_D2R_F_N	36
I412	85_OHM_DIFF	USB3	USB3_EXTA_D2R_F_P	36
I413	85_OHM_DIFF	USB3	USB3_EXTA_D2R_N	15 36
I414	85_OHM_DIFF	USB3	USB3_EXTA_D2R_P	15 36 82
I415	85_OHM_DIFF	USB3	USB3_EXTA_R2D_C_N	15 36 82
I416	85_OHM_DIFF	USB3	USB3_EXTA_R2D_C_P	15 36 82
I417	85_OHM_DIFF	USB3	USB3_EXTA_R2D_F_N	36
I418	85_OHM_DIFF	USB3	USB3_EXTA_R2D_F_P	36
I419	85_OHM_DIFF	USB3	USB3_EXTA_R2D_N	36 82
I420	85_OHM_DIFF	USB3	USB3_EXTA_R2D_P	36 82
I421	85_OHM_DIFF	USB3	USB3_EXTB_D2R_F_N	36
I422	85_OHM_DIFF	USB3	USB3_EXTB_D2R_F_P	36
I423	85_OHM_DIFF	USB3	USB3_EXTB_D2R_N	15 36 82
I424	85_OHM_DIFF	USB3	USB3_EXTB_D2R_P	15 36 82
I425	85_OHM_DIFF	USB3	USB3_EXTB_R2D_C_N	15 36 82
I426	85_OHM_DIFF	USB3	USB3_EXTB_R2D_C_P	15 36 82
I427	85_OHM_DIFF	USB3	USB3_EXTB_R2D_F_N	36
I428	85_OHM_DIFF	USB3	USB3_EXTB_R2D_F_P	36
I429	85_OHM_DIFF	USB3	USB3_EXTB_R2D_N	36 82
I430	85_OHM_DIFF	USB3	USB3_EXTB_R2D_P	36 82
I431	85_OHM_DIFF	USB3	USB3_EXTC_D2R_F_N	37
I432	85_OHM_DIFF	USB3	USB3_EXTC_D2R_F_P	37
I433	85_OHM_DIFF	USB3	USB3_EXTC_D2R_N	15 37 82
I434	85_OHM_DIFF	USB3	USB3_EXTC_D2R_P	15 37
I435	85_OHM_DIFF	USB3	USB3_EXTC_R2D_C_N	15 37
I436	85_OHM_DIFF	USB3	USB3_EXTC_R2D_C_P	15 37 82
I437	85_OHM_DIFF	USB3	USB3_EXTC_R2D_F_N	37
I438	85_OHM_DIFF	USB3	USB3_EXTC_R2D_F_P	37
I439	85_OHM_DIFF	USB3	USB3_EXTC_R2D_N	37 82
I440	85_OHM_DIFF	USB3	USB3_EXTC_R2D_P	37 82
I441	85_OHM_DIFF	USB3	USB3_EXTD_D2R_F_N	37
I442	85_OHM_DIFF	USB3	USB3_EXTD_D2R_F_P	37
I443	85_OHM_DIFF	USB3	USB3_EXTD_D2R_N	15 37 82
I444	85_OHM_DIFF	USB3	USB3_EXTD_D2R_P	15 37 82
I445	85_OHM_DIFF	USB3	USB3_EXTD_R2D_C_N	15 37 82
I446	85_OHM_DIFF	USB3	USB3_EXTD_R2D_C_P	15 37 82
I447	85_OHM_DIFF	USB3	USB3_EXTD_R2D_F_N	37
I448	85_OHM_DIFF	USB3	USB3_EXTD_R2D_F_P	37
I449	85_OHM_DIFF	USB3	USB3_EXTD_R2D_N	37 82
I450	85_OHM_DIFF	USB3	USB3_EXTD_R2D_P	37 82

USB_*

	Physical	Spacing	Netname	
I451	85_OHM_DIFF	USB	USB_BT_CONN_N	32 81
I452	85_OHM_DIFF	USB	USB_BT_CONN_P	32 81
I453	85_OHM_DIFF	USB	USB_BT_N	15 32
I454	85_OHM_DIFF	USB	USB_BT_P	15 32
I455	85_OHM_DIFF	USB	USB_BT_SW_N	32
I456	85_OHM_DIFF	USB	USB_BT_SW_P	32
I457	85_OHM_DIFF	USB	USB_EXTA_N	15 36
I458	85_OHM_DIFF	USB	USB_EXTA_P	15 36
I459	85_OHM_DIFF	USB	USB_EXTB_N	15 36
I460	85_OHM_DIFF	USB	USB_EXTB_P	15 36
I461	85_OHM_DIFF	USB	USB_EXTC_N	15 37
I462	85_OHM_DIFF	USB	USB_EXTC_P	15 37
I463	85_OHM_DIFF	USB	USB_EXTD_N	15 37
I464	85_OHM_DIFF	USB	USB_EXTD_P	15 37
I465	85_OHM_DIFF	USB	USB_IR_N	15 38
I466	85_OHM_DIFF	USB	USB_IR_P	15 38
I467	85_OHM_DIFF	USB	USB_IR_R_N	38
I468	85_OHM_DIFF	USB	USB_IR_R_P	38

WIFI_*

	Physical	Spacing	Netname	
I469	SMB_50SE	SMB	WIFI_PROX_THRM_N	45
I470	SMB_50SE	SMB	WIFI_PROX_THRM_P	45
I471	50_OHM_SE	PM	WIFI_WAKE_L	32 81

XDP_*

	Physical	Spacing	Netname	
I472	50_OHM_SE	PM	XDP_BPM_L<0..7>	7 17 81
I473	50_OHM_SE	PM	XDP_CPUPCH_TRST_L	17
I474	50_OHM_SE	PM	XDP_CPURST_L	17 81
I475	50_OHM_SE	PM	XDP_CPU_PRDY_L	7 17 81
I476	50_OHM_SE	PM	XDP_CPU_PREQ_L	7 17 81
I477	50_OHM_SE	PM	XDP_CPU_PRESENT_L	17 81
I478	50_OHM_SE	PM	XDP_CPU_PWRBTN_L	17 81
I479	50_OHM_SE	PM	XDP_CPU_TCK	7 17 81
I480	50_OHM_SE	PM	XDP_CPU_TDI	7 17
I481	50_OHM_SE	PM	XDP_CPU_TDO	7 17
I482	50_OHM_SE	PM	XDP_CPU_TMS	7 17
I483	50_OHM_SE	PM	XDP_CPU_TRST_L	7 17
I484	50_OHM_SE	PM	XDP_CPU_VCCST_PWRGD	17 81
I485	50_OHM_SE	PM	XDP_DBRESET_L	17 19 81
I486	50_OHM_SE	PM	XDP_JTAG_CPU_ISOL_L	17
I487	50_OHM_SE	PM	XDP_JTAG_ISP_TCK	16 17 20 81 82
I488	50_OHM_SE	PM	XDP_JTAG_ISP_TDI	16 17 20 81 82
I489	50_OHM_SE	PM	XDP_LPCPLUS_GPIO	16 17 81
I490	50_OHM_SE	PM	XDP_MLB_RAMCFG0	16 17 81
I491	50_OHM_SE	PM	XDP_MLB_RAMCFG1	16 17 81
I492	50_OHM_SE	PM	XDP_MLB_RAMCFG2	16 17 81
I493	50_OHM_SE	PM	XDP_MLB_RAMCFG3	16 17 81
I494	50_OHM_SE	PM	XDP_PCH_GPIO17	16 17 81
I495	50_OHM_SE	PM	XDP_PCH_GPIO76	16 17 81
I496	50_OHM_SE	PM	XDP_PCH_TCK	13 17 81
I497	50_OHM_SE	PM	XDP_PCH_TDI	13 17 81
I498	50_OHM_SE	PM	XDP_PCH_TDO	13 17 81
I499	50_OHM_SE	PM	XDP_PCH_TMS	13 17 81
I4100	50_OHM_SE	PM	XDP_PCH_TRST_L	13 17
I4101	50_OHM_SE	PM	XDP_SDCONN_STATE_CHANGE_L	16 17 81
I4102	50_OHM_SE	PM	XDP_SSD_PCIE0_SEL_L	13 17 81
I4103	50_OHM_SE	PM	XDP_SSD_PCIE1_SEL_L	13 17 81
I4104	50_OHM_SE	PM	XDP_SSD_PCIE2_SEL_L	13 17 81
I4105	50_OHM_SE	PM	XDP_SSD_PCIE3_SEL_L	13 17 81
I4106	50_OHM_SE	PM	XDP_SYS_PWROK	17 81
I4107	50_OHM_SE	PM	XDP_TRST_L	17 81
I4108	50_OHM_SE	PM	XDP_USB_EXTA_OC_L	15 17 81

XDP_*

	Physical	Spacing	Netname	
I4109	50_OHM_SE	PM	XDP_USB_EXTB_OC_L	15 17 81
I4110	50_OHM_SE	PM	XDP_USB_EXTC_OC_L	15 17 81

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FUNCTIONAL TEST POINTS

AIRPORT/BT CONN. (J4100)

FUNC_TEST			
TRUE	PP3V3_G3S_BT_F	32	1 TP
TRUE	PP3V3_WLAN_FET	32	3 TPS
TRUE	AP_CLKREQ_Q_L	32	
TRUE	AP_RESET_CONN_L	32	
TRUE	PCIE_AP_D2R_N	15 32 77	
TRUE	PCIE_AP_D2R_P	15 32 77	
TRUE	PCIE_AP_R2D_N	32 77	
TRUE	PCIE_AP_R2D_P	32 77	
TRUE	PCIE_CLK100M_AP_CONN_N	32 77	
TRUE	PCIE_CLK100M_AP_CONN_P	32 77	
TRUE	USB_BT_CONN_N	32 80	
TRUE	USB_BT_CONN_P	32 80	
TRUE	WIFI_EVENT_L	32 40	
TRUE	WIFI_WAKE_L	32 80	
TRUE	GND		4 TPS

HDD CONNECTOR (J4401)

FUNC_TEST			
TRUE	PP5V_S0_HDD1	35	4 TPS
TRUE	SATA_A_D2R_N	13 35 79	
TRUE	SATA_A_D2R_P	13 35 79	
TRUE	SATA_A_R2D_C_N	13 35 79	
TRUE	SATA_A_R2D_C_P	13 35 79	
TRUE	SSD1_OOBD2R_L	35	
TRUE	SSD1_OOBR2D_L	35	
TRUE	GND		6 TPS

SSD CONNECTOR (J4300)

FUNC_TEST			
TRUE	PP3V3_S0_SSD	34	10 TPS
TRUE	PCIE_CLK100M_SSD_F_N	34 77	
TRUE	PCIE_CLK100M_SSD_F_P	34 77	
TRUE	PCIE_SSD_D2R_N<0>	13 34 77	
TRUE	PCIE_SSD_D2R_N<1>	13 34 77	
TRUE	PCIE_SSD_D2R_P<0>	13 34 77	
TRUE	PCIE_SSD_D2R_P<1>	13 34 77	
TRUE	PCIE_SSD_R2D_N<0>	34 77	
TRUE	PCIE_SSD_R2D_N<1>	34 77	
TRUE	PCIE_SSD_R2D_P<0>	34 77	
TRUE	PCIE_SSD_R2D_P<1>	34 77	
TRUE	SMC_SSD_OOBD2R_L	34 40	
TRUE	SMC_SSD_OOBR2D_L	34 40	
TRUE	SSD_CLKREQ_L	13 34	
TRUE	SSD_RESET_L	16 34 79	
TRUE	GND		16 TPS

IR/LED CONNECTOR (J4800)

FUNC_TEST			
TRUE	PPIRRCVR_F	39	1 TP
TRUE	IRRCVR_OUT	38 39	
TRUE	SMC_SYS_LED_DR	39	
TRUE	GND_IR_F	39	
TRUE	GND		1 TP

POWER BUTTON CONNECTOR (J4801)

FUNC_TEST			
TRUE	POWER_BTN	39	
TRUE	POWER_BTN_RTN	39	

AUDIO JACKS (J6100)

FUNC_TEST			
TRUE	PP3V3_S0	60 70 78 44 46 48 28 31 34 35 3 4 9 12 13 14 16 17 19 47 49 51 52 53 54 61 63 65	2 TPS
	AUD_CONNJ1_MIC	49 74	
	AUD_CONNJ1_RING	49 74	
	AUD_CONNJ1_SLEEVE	49 74	
	AUD_CONNJ1_TIP	49 74	
	AUD_CONNJ1_TYPEDET	49 74	
	AUD_CONNJ2_RING	49 74	
	AUD_CONNJ2_SLEEVE	49 74	
	AUD_CONNJ2_SPDIF_IN	49 74	
	AUD_CONNJ2_TIP	49 74	
	AUD_CONNJ2_TYPEDET	49 74	
	AUD_HPO_TIPDET1	46 49 74	
	AUD_HPO_TIPDET2	46 49 74	
	AUD_LI_TIPDET	46 49 74	
	AUD_SPDIF_OUT	47 49 74	
TRUE	GND		9 TPS

SPEAKER CONNECTOR (J6300)

FUNC_TEST			
TRUE	SPKRAMP_P_OUT	50 79	
TRUE	SPKRAMP_N_OUT	50 79	

FAN CONNECTOR (J6500)

FUNC_TEST			
TRUE	PP12V_S0_FAN0_F	51 77	1 TP
TRUE	FAN0_CTL_F	51	
TRUE	FAN0_TACH_F	51	
TRUE	GND		1 TP

PSU CONNECTOR (J7900)

FUNC_TEST			
TRUE	PP12V_G3H_PSU	3 44 61 77	4 TPS
TRUE	PSU_TEMP	40 61 78	
TRUE	GND		4 TPS

BATTERY HOLDER (J2700)

FUNC_TEST			
TRUE	PPVBATT_G3_RTC	3 19 78	1 TP
TRUE	GND		1 TP

XDP CONNECTOR (J2400)

FUNC_TEST			
	PP1V05_S0	57 59 78 4 7 9 12 16 17 19 41 45	2 TPS
	CPU_CFG<19..0>	7 17 74	
	CPU_PWR_DEBUG	9 17 74	
	SMB_CPU_XDP_SCL	17 42 79	
	SMB_CPU_XDP_SDA	17 42 79	
	XDP_BPM_L<0>	7 17 80	
TRUE	XDP_BPM_L<1>	7 17 80	
	XDP_CPU_PRDY_L	7 17 80	
	XDP_CPU_PREQ_L	7 17 80	
	XDP_CPU_PRESENT_L	17 80	
	XDP_CPU_PWRBTN_L	17 80	
	XDP_CPU_TCK	7 17 80	
TRUE	XDP_CPU_VCCST_PWRGD	17 80	
	XDP_CPURST_L	17 80	
TRUE	XDP_DBRESET_L	17 19 80	
	XDP_PCH_TCK	13 17 80	
TRUE	XDP_PCH_TDI	13 17 80	
TRUE	XDP_PCH_TDO	13 17 80	
TRUE	XDP_PCH_TMS	13 17 80	
	XDP_SYS_PWROK	17 80	
	XDP_TRST_L	17 80	
TRUE	GND		17 TPS

MATT CARD CONNECTOR (J2600)

FUNC_TEST			
TRUE	PP3V3_S5	60 70 3 9 12 14 15 16 17 18 19 52 53 54	1 TP
	PP5V_S0	58 70 4 17 18 19 36 46 50 52 54 57	1 TP
TRUE	LPC_AD<3..0>	15 18 40 76	
TRUE	LPC_CLK24M_LPCPLUS	18 19 76	
TRUE	LPC_FRAME_L	15 18 40 76	
TRUE	LPC_PWRDWN_L	14 18 40 76	
TRUE	LPC_SERIRQ	16 18 40 76	
TRUE	LPCPLUS_RESET_L	18 20 76	
TRUE	PM_CLKRUN_L	14 18 40 77	
TRUE	SMC_RESET_L	18 40 41	
TRUE	SMC_ROMBOOT	18 41	
TRUE	SMC_RX_L	18 40 41	
TRUE	SMC_TCK	18 40 41	
TRUE	SMC_TDI	18 40 41	
TRUE	SMC_TDO	18 40 41	
TRUE	SMC_TMS	18 40 41	
TRUE	SMC_TX_L	18 40 41	
TRUE	SPI_ALT_CLK	18 79	
TRUE	SPI_ALT_CS_L	18 79	
TRUE	SPI_ALT_MISO	18 79	
TRUE	SPI_ALT_MOSI	18 79	
TRUE	SPIROM_USE_MLB	16 18 79	
TRUE	XDP_LPCPLUS_GPIO	16 17 80 81	
TRUE	GND		2 TPS

TEST POINTS REQUIRED

NEED_TP			NEED_TP			NEED_TP		
TRUE	XDP_PCH_GPIO76	16 17 80	TRUE	XDP_MLB_RAMCFG0	16 17 80	TRUE	XDP_MLB_RAMCFG1	16 17 80
TRUE	XDP_MLB_RAMCFG2	16 17 80	TRUE	XDP_MLB_RAMCFG3	16 17 80	TRUE	XDP_LPCPLUS_GPIO	16 17 80 81
TRUE	XDP_PCH_GPIO17	16 17 80	TRUE	XDP_JTAG_ISP_TCK	16 17 20 80 82	TRUE	XDP_JTAG_ISP_TDI	16 17 20 80 82
TRUE	XDP_SDCONN_STATE_CHANGE_L	16 17 80	TRUE	XDP_USB_EXTA_OC_L	15 17 80	TRUE	XDP_USB_EXTB_OC_L	15 17 80
TRUE	XDP_USB_EXTC_OC_L	15 17 80	TRUE	XDP_USB_EXTD_OC_L	15 17	TRUE	XDP_SSD_PCIE3_SEL_L	13 17 80
TRUE	XDP_SSD_PCIE2_SEL_L	13 17 80	TRUE	XDP_SSD_PCIE1_SEL_L	13 17 80	TRUE	XDP_SSD_PCIE0_SEL_L	13 17 80

BEAD-PROBES

TP0C02	NO_XNET_CONNECTION=TRUE	DP_TBTPA_ML_C_P<1>	62 66 75
TP0C03	NO_XNET_CONNECTION=TRUE	DP_TBTPA_ML_C_N<1>	62 66 75
TP0C06	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_C_P	62 68 75
TP0C07	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_C_N	62 68 75
TP0C08	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_P	62 75
TP0C09	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_N	62 75
TP0C10	NO_XNET_CONNECTION=TRUE	DP_TBTSNK0_AUXCH_P	62 75
TP0C11	NO_XNET_CONNECTION=TRUE	DP_TBTSNK0_AUXCH_N	62 75
TP0C16	NO_XNET_CONNECTION=TRUE	TBT_A_R2D_C_P<0>	62 66 79
TP0C17	NO_XNET_CONNECTION=TRUE	TBT_A_R2D_C_N<0>	62 66 79
TP0C20	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_C_P<0>	66 79
TP0C21	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_C_N<0>	66 79
TP0C24	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_P<0>	62 66 79
TP0C25	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_N<0>	62 66 79
TP0C22	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_P<1>	62 66 79
TP0C23	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_N<1>	62 66 79
TP0C26	NO_XNET_CONNECTION=TRUE	TBT_B_R2D_C_P<0>	62 67 79
TP0C27	NO_XNET_CONNECTION=TRUE	TBT_B_R2D_C_N<0>	62 67 79
TP0C30	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_C_P<0>	67 79
TP0C31	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_C_N<0>	67 79
TP0C34	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_P<0>	62 67 79
TP0C35	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_N<0>	62 67 79
TP0C32	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_P<1>	62 67 79
TP0C33	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_N<1>	62 67 79
TP0C40	NO_XNET_CONNECTION=TRUE	TBT_A_D2R1_AUXDDC_P	66 79
TP0C41	NO_XNET_CONNECTION=TRUE	TBT_A_D2R1_AUXDDC_N	66 79
TP0C42	NO_XNET_CONNECTION=TRUE	DP_A_LSX_ML_P<1>	66 75
TP0C43	NO_XNET_CONNECTION=TRUE	DP_A_LSX_ML_N<1>	66 75
TP0C44	NO_XNET_CONNECTION=TRUE	TBT_B_D2R1_AUXDDC_P	67 79
TP0C45	NO_XNET_CONNECTION=TRUE	TBT_B_D2R1_AUXDDC_N	67 79
TP0C46	NO_XNET_CONNECTION=TRUE	DP_B_LSX_ML_P<1>	67 75
TP0C47	NO_XNET_CONNECTION=TRUE	DP_B_LSX_ML_N<1>	67 75
TP0C50	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_P<0>	8 23 27 76
TP0C51	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_N<0>	8 23 27 76
TP0C52	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_P<1>	8 24 27 76
TP0C53	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_N<1>	8 24 27 76
TP0C54	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_P<0>	8 25 27 76
TP0C55	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_N<0>	8 25 27 76
TP0C56	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_P<1>	8 26 27 76
TP0C57	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_N<1>	8 26 27 76
TP0C60	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<0>	62 77
TP0C61	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<0>	62 77
TP0C62	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<1>	62 77
TP0C63	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<1>	62 77
TP0C64	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<2>	62 77
TP0C65	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<2>	62 77
TP0C66	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<3>	62 77
TP0C67	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<3>	62 77
TP0C74	NO_XNET_CONNECTION=TRUE	PCIE_TBT_R2D_C_P<2>	15 62 77
TP0C75	NO_XNET_CONNECTION=TRUE	PCIE_TBT_R2D_C_N<2>	15 62 77

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(NC_* NETS ARE ON AUTO-CONSTRAINT PAGES.)

MEMORY NETS

NO_TEST

E11	TRUE	MEM_A_DQ<0..63>	8 21 76
E85	TRUE	MEM_B_DQ<0..63>	8 21 76
E7	TRUE	MEM_A_CAA<0..9>	8 23 27 76
E34	TRUE	MEM_B_CAA<0..9>	8 25 27 76
E4	TRUE	MEM_A_CAB<0..9>	8 24 27 76
E35	TRUE	MEM_B_CAB<0..9>	8 26 27 76
E31	TRUE	MEM_A_CKE<0..3>	8 23 24 27 76
E32	TRUE	MEM_B_CKE<0..3>	8 25 26 27 76
E436	TRUE	MEM_A_DQS_P<1..7>	8 21 76
E438	TRUE	MEM_A_DQS_N<1..7>	8 21 76
E437	TRUE	MEM_B_DQS_P<0..7>	8 21 76
E440	TRUE	MEM_B_DQS_N<0..7>	8 21 76

DP NETS

NO_TEST

E45	TRUE	DP_HDMI_TBT_AUXCH_C_P	14 68 75
E43	TRUE	DP_HDMI_TBT_AUXCH_C_N	14 68 75
E64	TRUE	DP_HDMI_TBT_ML_C_P<0..3>	6 68 75
E66	TRUE	DP_HDMI_TBT_ML_C_N<0..3>	6 68 75
E54	TRUE	DP_TBTPA_AUXCH_C_P	62 66 75
E56	TRUE	DP_TBTPA_AUXCH_C_N	62 66 75
E41	TRUE	DP_TBTPA_AUXCH_P	66 75
E40	TRUE	DP_TBTPA_AUXCH_N	66 75
E446	TRUE	DP_TBTPA_ML_C_P<3>	62 66 75
E450	TRUE	DP_TBTPA_ML_C_N<3>	62 66 75
E52	TRUE	DP_TBTPA_ML_P<1,3>	66 75
E53	TRUE	DP_TBTPA_ML_N<1,3>	66 75
E60	TRUE	DP_TBTPB_AUXCH_C_P	62 67 75
E58	TRUE	DP_TBTPB_AUXCH_C_N	62 67 75
E39	TRUE	DP_TBTPB_AUXCH_P	67 75
E38	TRUE	DP_TBTPB_AUXCH_N	67 75
E448	TRUE	DP_TBTPB_ML_C_P<1,3>	62 67 75
E452	TRUE	DP_TBTPB_ML_C_N<1,3>	62 67 75
E50	TRUE	DP_TBTPB_ML_P<3>	67 75
E48	TRUE	DP_TBTPB_ML_N<3>	67 75
E62	TRUE	DP_TBTSNK0_AUXCH_C_P	14 62 75
E63	TRUE	DP_TBTSNK0_AUXCH_C_N	14 62 75
E67	TRUE	DP_TBTSNK0_DDC_CLK	14 65 75
E65	TRUE	DP_TBTSNK0_DDC_DATA	14 65 75
E454	TRUE	DP_TBTSNK0_ML_C_P<0..3>	6 62 64 75
E456	TRUE	DP_TBTSNK0_ML_C_N<0..3>	6 62 64 75
E44	TRUE	DP_TBTSNK0_ML_P<0..3>	62 75
E46	TRUE	DP_TBTSNK0_ML_N<0..3>	62 75
E444	TRUE	DP_TBTSNK1_ML_C_P<0..3>	62 64 68 75
E47	TRUE	DP_TBTSNK1_ML_C_N<0..3>	62 64 68 75
E59	TRUE	DP_TBTSNK1_ML_P<0..3>	62 75
E57	TRUE	DP_TBTSNK1_ML_N<0..3>	62 75

HDMI NETS

NO_TEST

E69	TRUE	HDMI_CLK_C_P	68 69 75
E67	TRUE	HDMI_CLK_C_N	68 69 75
E82	TRUE	HDMI_CLK_CNR_P	70 75
E84	TRUE	HDMI_CLK_CNR_N	70 75
E80	TRUE	HDMI_CLK_FLT_P	70 75
E81	TRUE	HDMI_CLK_FLT_N	70 75
E78	TRUE	HDMI_CLK_LS_P	69 75
E79	TRUE	HDMI_CLK_LS_N	69 75
E76	TRUE	HDMI_DAT_CNR_P<0..2>	70 75
E77	TRUE	HDMI_DAT_CNR_N<0..2>	70 75
E74	TRUE	HDMI_DATA_C_P<0..2>	68 69 75
E75	TRUE	HDMI_DATA_C_N<0..2>	68 69 75
E72	TRUE	HDMI_DATA_CONN_P<0..2>	70 75
E73	TRUE	HDMI_DATA_CONN_N<0..2>	70 75
E70	TRUE	HDMI_DATA_FLT_P<0..2>	70 75
E71	TRUE	HDMI_DATA_FLT_N<0..2>	70 75
E68	TRUE	HDMI_DATA_LS_P<0..2>	69 75
E66	TRUE	HDMI_DATA_LS_N<0..2>	69 75
E460	TRUE	HDMI_IDROM_CLK	68 75
E458	TRUE	HDMI_IDROM_DAT	68 75

PCIE NETS

NO_TEST

E442	TRUE	PCIE_TBT_R2D_C_P<0,1,3>	15 62 77
E462	TRUE	PCIE_TBT_R2D_C_N<0,1,3>	15 62 77
E464	TRUE	PCIE_TBT_R2D_P<0..3>	62 77
E466	TRUE	PCIE_TBT_R2D_N<0..3>	62 77

E130	TRUE	PCIE_CLK100_TBT_P	
E150	TRUE	PCIE_CLK100_TBT_N	

TBT NETS

NO_TEST

E84	TRUE	TBT_A_D2R_C_P<1>	66 79
E85	TRUE	TBT_A_D2R_C_N<1>	66 79
E104	TRUE	TBT_A_LSRX	62 66 79
E103	TRUE	TBT_A_LSTX	62 66 79
E100	TRUE	TBT_A_R2D_C_P<1>	62 66 79
E99	TRUE	TBT_A_R2D_C_N<1>	62 66 79
E98	TRUE	TBT_A_R2D_P<0,1>	66 79
E97	TRUE	TBT_A_R2D_N<0,1>	66 79
E96	TRUE	TBT_B_D2R_C_P<1>	67 79
E95	TRUE	TBT_B_D2R_C_N<1>	67 79
E94	TRUE	TBT_B_LSRX	62 67 79
E93	TRUE	TBT_B_LSTX	62 67 79
E92	TRUE	TBT_B_PWRSW_ISET_S0_R	67
E91	TRUE	TBT_B_PWRSW_ISET_S3_R	67
E90	TRUE	TBT_B_R2D_C_P<1>	62 67 79
E89	TRUE	TBT_B_R2D_C_N<1>	62 67 79
E88	TRUE	TBT_B_R2D_P<0,1>	67 79
E87	TRUE	TBT_B_R2D_N<0,1>	67 79
E86	TRUE	TBT_CLK25M_OUT_R	62 79

E165	TRUE	TBT_A_CONN_1_C	66
E164	TRUE	TBT_A_CONN_7_C	66
E163	TRUE	TBT_A_CONN_20_RC	66
E162	TRUE	TBT_B_CONN_1_C	67
E161	TRUE	TBT_B_CONN_7_C	67
E160	TRUE	TBT_B_CONN_20_RC	67
E159	TRUE	TBT_B_PWRSW_ISET_S3	67
E158	TRUE	TBT_DFT_STRAP3	
E157	TRUE	TBT_GPIO2	62
E156	TRUE	TBTROM_HOLD_L	62

USB NETS

NO_TEST

E137	TRUE	USB3_EXTA_D2R_P	15 36 80
E139	TRUE	USB3_EXTA_R2D_C_P	15 36 80
E136	TRUE	USB3_EXTA_R2D_C_N	15 36 80
E135	TRUE	USB3_EXTA_R2D_P	36 80
E134	TRUE	USB3_EXTA_R2D_N	36 80
E133	TRUE	USB3_EXTB_D2R_P	15 36 80
E132	TRUE	USB3_EXTB_D2R_N	15 36 80
E131	TRUE	USB3_EXTB_R2D_C_P	15 36 80
E130	TRUE	USB3_EXTB_R2D_C_N	15 36 80
E129	TRUE	USB3_EXTB_R2D_P	36 80
E128	TRUE	USB3_EXTB_R2D_N	36 80
E127	TRUE	USB3_EXTC_D2R_N	15 37 80
E126	TRUE	USB3_EXTC_R2D_C_P	15 37 80
E125	TRUE	USB3_EXTC_R2D_P	37 80
E124	TRUE	USB3_EXTC_R2D_N	37 80
E123	TRUE	USB3_EXTD_D2R_P	15 37 80
E122	TRUE	USB3_EXTD_D2R_N	15 37 80
E121	TRUE	USB3_EXTD_R2D_C_P	15 37 80
E120	TRUE	USB3_EXTD_R2D_C_N	15 37 80
E119	TRUE	USB3_EXTD_R2D_P	37 80
E118	TRUE	USB3_EXTD_R2D_N	37 80

MISC NETS

NO_TEST

E10	TRUE	CPU_CATERR_RL	3 74
E11	TRUE	DP0GAN0	64 75
E13	TRUE	DP0GAP0	64 75
E14	TRUE	DP1GAN3	64 75
E15	TRUE	DP1GAP3	64 75
E17	TRUE	ENET_ACT	29
E16	TRUE	ENET_SR_VFB	28 29
E18	TRUE	P1V05TBT_SW	63
E10	TRUE	USB_ILIM1B	36
E10	TRUE	USB_ILIM2B	37
E13	TRUE	XDP_JTAG_ISP_TCK	16 17 20 80 81
E13	TRUE	XDP_JTAG_ISP_TDI	16 17 20 80 81
E14	TRUE	CATERR_LED	3

MISC NETS

NO_TEST

E16	TRUE	CPUVR_PH1_SNUB	58
E16	TRUE	CPUVR_PH2_SNUB	58
E16	TRUE	REG_SNUBBER_P1V05S0	59 78
E16	TRUE	LDO_DDRVTTS0_SNS	56 76
E17	TRUE	PU_GPIO46	16
E17	TRUE	PD_GPIO13	16

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FORCES CROSS REFERENCE PAGES TO COME AFTER THIS.
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