MS-7619 Ver: 1.0 uATX(244mm X 244mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:Realtek RTM875N-606

HD Audio Codec:RTL888S-VC

LAN:RTL8111DL 10/100/1000

LAN:INTEL 82578 10/100/1000

IO: Fintek F71882

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

ONFI Slot *1

PWM:

Controller:ON NCP5395 4-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *5

eSATA(SATA2-300MB/s) *1

USB2.0 *12 (Rear*4 / Front*8)

on BOARD BUZZER

D-SUB *1

DVI PORT*1

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Size C | Document Description: Cover Sheet | Rev V10

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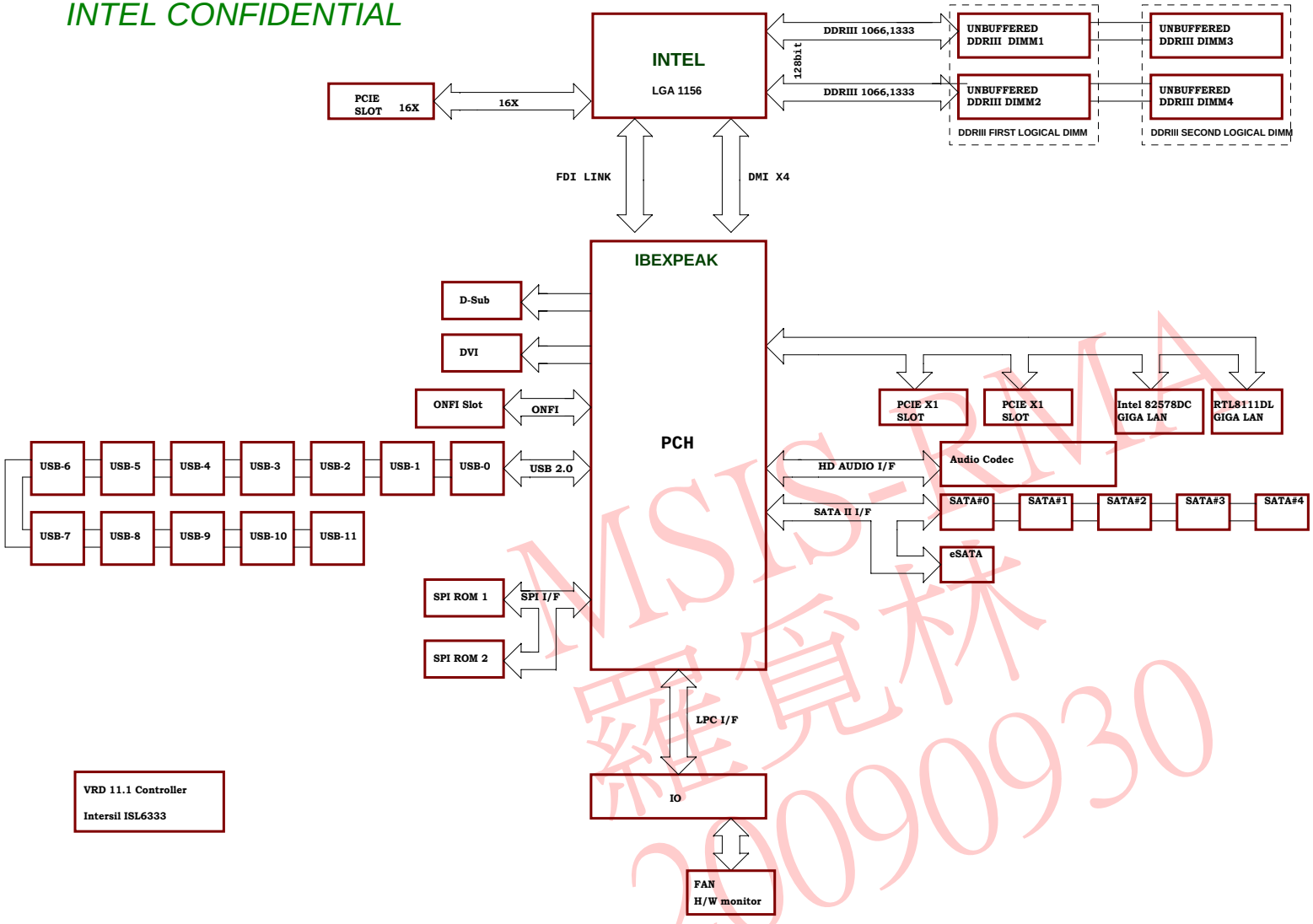

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Size	Document Description	Rev
C	Block Diagram	V10

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #x	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

Table 24-5. Power Delivery Summary for Intel® Management Engine

Rail	Sx/M3	Sx/Moff	Sx/Moff/ME WOL	Source	Enabled By	Power OK Indicator	What This Rail Powers
Common							
5 V DUAL[1]	On	On	On	5 V STBY (Sx) 5 V Main (S0)			• 1.5 VDDQ • 1.8 LAN
1.5 VDDQ	On	S3[2]	S3[2]	5 V DUAL	SLP_S4#		• DRAM
3.3 CK505				3.3 V Main	CKPWRGD		• CK505
1.05/1.1 VCORE				1.5 VDDQ		PWROK	• Ibex Peak
M3 Support + Intel® 82577							
1.05/1.1 ME	On			5 V STBY	SLP_M#	MEPWROK	• ME • Local RAM
3.3 LAN 1.8/1.2 LAN	On	On	On	3.3 V STBY	SLP_LAN#	SLP_LAN# + 40 sec	• Intel® 82577
3.3 SPI	On			3.3 V STBY	SLP_M#	MEPWROK	• SPI flash • Ibex Peak SPI interface
VCCLAN	On			5 V DUAL	SLP_M#	LAN_RST# (tie to MEPWROK)[3]	• Integrated LAN controller in Ibex Peak
No M3 Support + Intel® 82577							
1.05/1.1 ME				1.05 V Ibex Peak	SLP_M#	MEPWROK	• ME • Local RAM
3.3 LAN 1.8/1.2 LAN		On	On	3.3 V STBY	SLP_LAN#	SLP_LAN# + 40 sec	• Intel® 82577
3.3 SPI				3.3 V Main	SLP_M#	MEPWROK	• SPI flash • Ibex Peak SPI interface
VCCLAN				1.05 V Ibex Peak	SLP_M#	LAN_RST# (tie to PWROK)[3]	• Integrated LAN controller in Ibex Peak
No M3 Support + no Intel® 82577							
1.05/1.1 ME				1.05 V Ibex Peak	SLP_M#	MEPWROK	• ME • Local RAM
3.3 SPI				3.3 V Main	SLP_M#	MEPWROK	• SPI flash • Ibex Peak SPI interface
VCCLAN				Grounded			

Notes:

1. 5 V DUAL should be powered by 5 V STBY in S3, S4, S5. This rail should be powered by 5 V main in S0. This is because the 5 V STBY rail does not typically support high current.
2. Memory is in self-refresh in S3. No transactions to memory are occuring in this power state.
3. Check Ibex Peak Platform Reset Considerations for more details.

GPIO	POWER	I/O	Trace Name	Implementation
GPIO0	Main	I	BM_BUSY#	An external pull-up resistor to VCC3
GPIO1	Main	I		An external pull-up resistor to VCC3
GPIO2	Main	I	PIRQ#E	See PCA Spec.
GPIO3	Main	I	PIRQ#F	See PCA Spec.
GPIO4	Main	I	PIRQ#G	See PCA Spec.
GPIO5	Main	I	PIRQ#H	See PCA Spec.
GPIO6	Main	I		An external pull-up resistor to VCC3
GPIO7	Main	I		An external pull-up resistor to VCC3
GPIO8		O	PCH_GPIO8	
GPIO9	Standby	I	OC#5	An external pull-up resistor to 3VSB
GPIO10	Standby	I	USB_OC#6	An external pull-up resistor to 3VSB
GPIO11	Standby	I	PCH_SMBALERT#	An external pull-up resistor to 3VSB
GPIO12	Standby	I	LAN_DISABLE_N	An external pull-up resistor to 3VSB_LAN
GPIO13	Standby	O	USB_MODE	An external pull-up resistor to 3VSB
GPIO14	Standby	I	USB_OC#7	An external pull-up resistor to 3VSB
GPIO15	Standby	O	SPI_HOLD_GPO#	An external pull-up resistor to 3VSB
GPIO16	Standby	I	SATA4GP_PU	An external pull-up resistor to 3VSB
GPIO17	Main	I		An external pull-up resistor to VCC3
GPIO18	Main	O	PCH_GPI8	An external pull-up resistor to VCC3
GPIO19	Main	O	SATA1GP_PU	An external pull-up resistor to VCC3
GPIO20	Main	O	PCH_GP20	An external pull-up resistor to VCC3
GPIO21	Main	O	SATA0GP_PU	An external pull-up resistor to VCC3
GPIO22	Main	I	SCLOCK	An external pull-up resistor to VCC3
GPIO23	Main	I	LDRQ1#	An reserved external pull-up resistor to VCC3

GPIO	POWER	I/O	Trace Name	Implementation
GPIO24	Standby	I	GPIO24	An external pull-up resistor to 3VSB
GPIO25	Standby	I	PCICLKRQ3#	An external pull-up resistor to 3VSB
GPIO26	Standby	I	LED_SW	An external pull-up resistor to 3VSB
GPIO27	Standby	I	PCH_GPIO27	An external pull-up resistor to 3VSB
GPIO28	Standby	O	PCH_GP57	An external pull-up resistor to 3VSB
GPIO29	Standby	O	SLP_LAN#	
GPIO30	Standby	I	SUS_PWR_ACK	An external pull-up resistor to 3VSB
GPIO31	Standby	I	LAN_LED_GPIO	An external pull-up resistor to 3VSB
GPIO32	Standby	O	SPI_WP#	An external pull-up resistor to 3V_ME
GPIO33		I	PCH_GPIO33	An external pull-down resistor to ground
GPIO34	Standby	I	STP_PCI#	An external pull-up resistor to 3VSB
GPIO35			NC	
GPIO36	Main	O	SATA2GP_PU	An external pull-up resistor to VCC3
GPIO37	Main	O	SATA3GP_PU	An external pull-up resistor to VCC3
GPIO38	Main	I	PCH_GPIO38	An external pull-up resistor to VCC3
GPIO39	Main	I	PCH_GPIO39	An external pull-up resistor to VCC3
GPIO40	Standby	I	OC#1	An external pull-up resistor to 3VSB
GPIO41	Standby	I	OC#2	An external pull-up resistor to 3VSB
GPIO42	Standby	I	OC#3	An external pull-up resistor to 3VSB
GPIO43	Standby	I	OC#4	An external pull-up resistor to 3VSB
GPIO44	Standby	I	PCH_GPI44	An external pull-up resistor to 3VSB
GPIO45	Standby	I	PCH_GPI45	An external pull-up resistor to 3VSB
GPIO46			PCH_GPI46	
GPIO47			PCH_GPI47	
GPIO48	Main	I	PCH_GPIO48	An external pull-up resistor to VCC3

GPIO	POWER	I/O	Trace Name	Implementation
GPIO49	Main	O	SATA5GP_PU	An external pull-up resistor to VCC3
GPIO50	Main	I	PREQ#1	An external pull-up resistor to VCC3
GPIO51	Main	O	PGNT#1	An external pull-up resistor to VCC3
GPIO52	Main	I	PREQ#2	An external pull-up resistor to VCC3
GPIO53	Main	O	PGNT#2	
GPIO54	Main	I	PREQ#3	An external pull-up resistor to VCC3
GPIO55	Main	O	PGNT#3	
GPIO56	Standby	I	PCH_GPI56	An external pull-up resistor to 3VSB
GPIO57	Standby	I	TPM_PP	An external pull-up resistor to 3VSB
GPIO58	Standby	I	PCH_SML1ALERT#	An external pull-up resistor to 3VSB
GPIO59	Standby	I	OC#0	An external pull-up resistor to 3VSB
GPIO60	Standby	I	PCH_SML0ALERT#	An external pull-up resistor to 3VSB
GPIO61		O	GPIO61	
GPIO62		O	SUSCLK	
GPIO63			NC	
GPIO64			TP	
GPIO65			TP	
GPIO66			TP	
GPIO67			TP	
GPIO72	Standby	I	GPIO72	An external pull-up resistor to 3VSB
GPIO73	Standby	o	PCIECLKRQ0#	An external pull-up resistor to 3VSB
GPIO74	Standby	I	PCH_SML1ALERT#	An external pull-up resistor to 3VSB
GPIO75	Standby	I	PCH_SML1DATA	An external pull-up resistor to 3VSB

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Size: C | Document Description: PCH GPIO Table | Rev: V10

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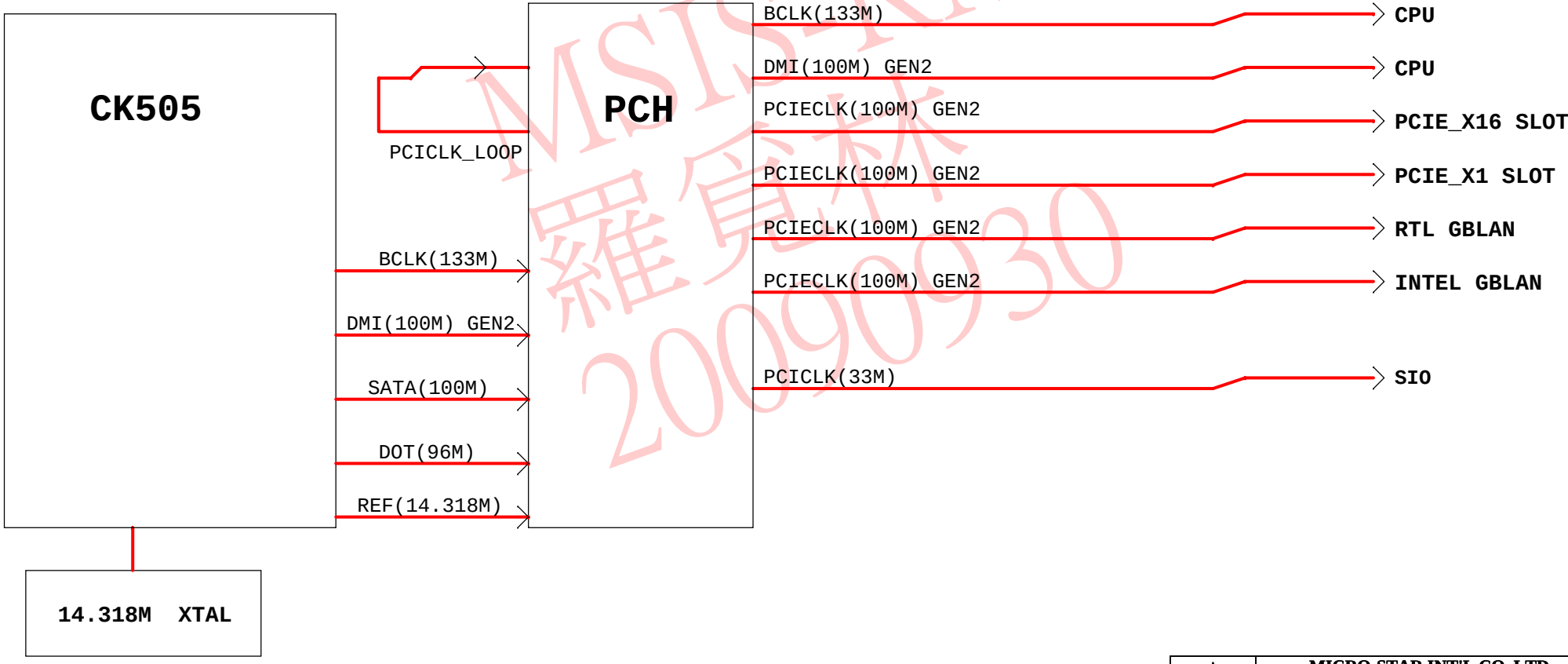

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Size	Document Description	Rev
Custom	Clock Distribution	V10

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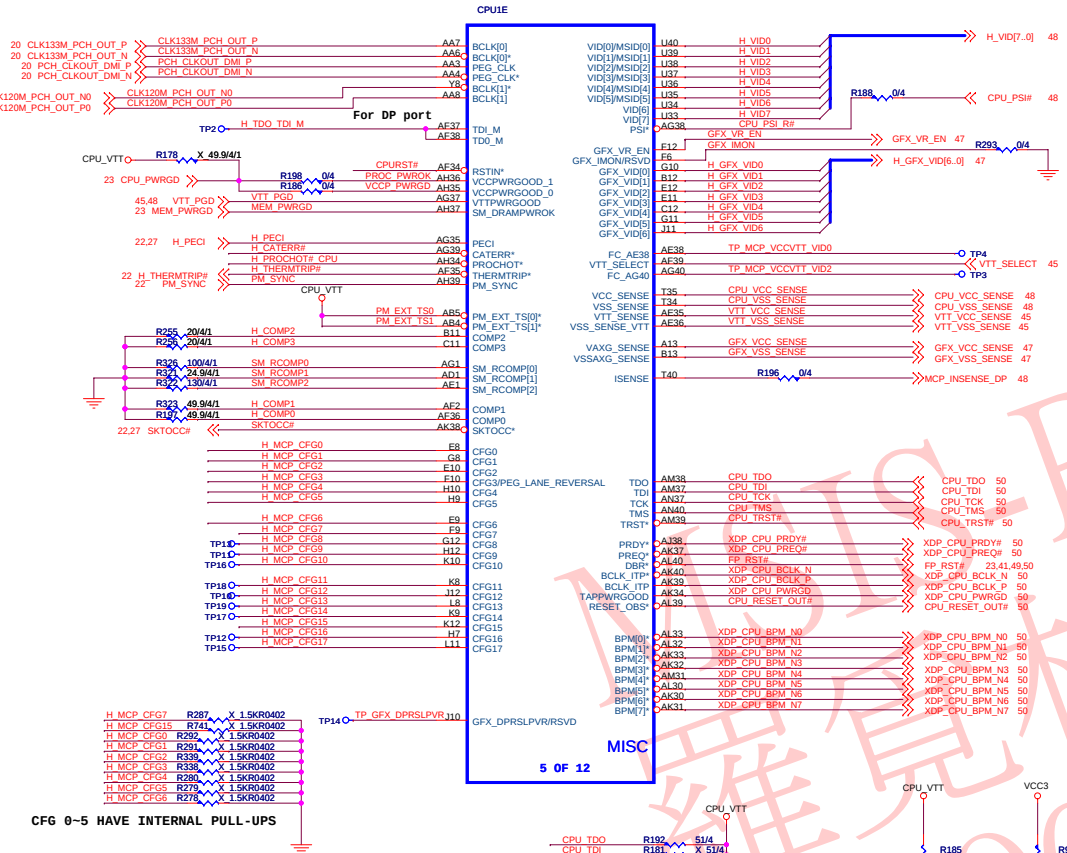
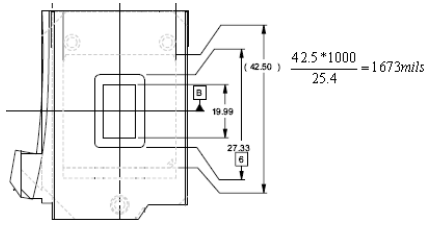
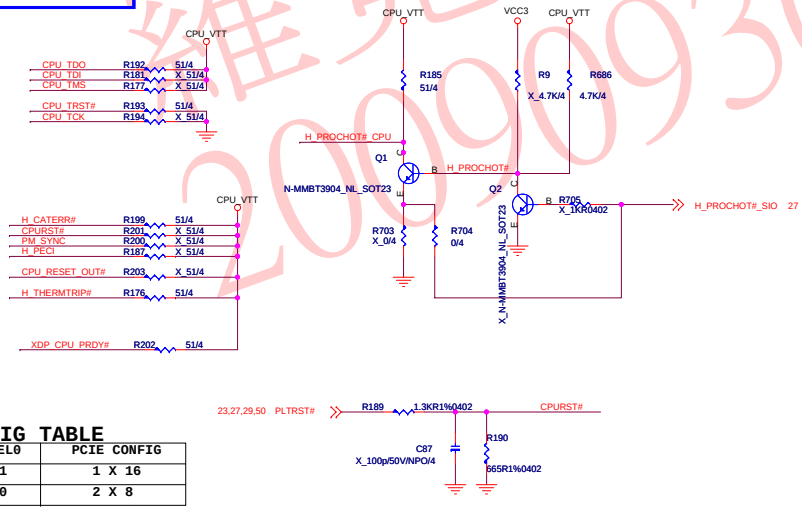






PEG CONFIG TABLE

CFG	H	L	DESCRIPTION
0	SEE PEG CONFIG TABLE		PEG SEL0
1	SEE PEG CONFIG TABLE		PEG SEL1
2	SEE PEG CONFIG TABLE		PEG SEL2
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLE	ENABLED	DP PRESENCE
5			

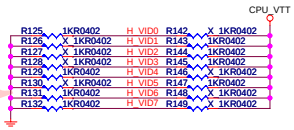
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

Signal Name	Description	Direction	Type
ISENSE	Current sense from VRD11.1 Compliant Regulator to the processor core.	I	Analog

Symbol	Alpha Group	Parameter	Min	Typ	Max	Units
V_{IL}	(ja),(qb)	Input Low Voltage			0.25 * V_{TT}	V
V_{IH}	(ja),(qb)	Input High Voltage	0.75 * V_{TT}			V

$V_{TT} = 1.1V$

Signal Group	Alpha Group	Type	Signals
Single Ended	(qb)	CMOS Input	RSTIN#



Power-On Configuration (POC[7:0]) Decode

Function	Bits	POC Settings		Description
VR_Key	VID[7]	0b for VR11.1		Electronic safety key distinguishing VR11.1
Spare	VID[6]	0b (default)		Reserved for future use
CSC[2:0]	VID[5:3]	-000 -001 -010 -011 -100 -101 -111	Feature Disabled ICC_MAX = 40A ICC_MAX = 50A[1] ICC_MAX = 80A ICC_MAX = 100A ICC_MAX = 120A ICC_MAX = 150A[2]	Current Sensor Configuration (CSC) programs the gain applied to the ISENSE A/D output. ISENSE data is then used to dynamically calculate current and power. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines* for further details on the IMON signal.
MSID[2:0]	VID[2:0]	-001 -011 -100 -101 -110	38W TDP / 40A ICC_MAX 60W TDP / 80A ICC_MAX 80W TDP / 100A ICC_MAX 95W TDP / 120A ICC_MAX 130W TDP / 150A ICC_MAX	MSID[2:0] signals are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or keying. See Figure 8-2 for platform timing requirements of the MSID[2:0] signals.

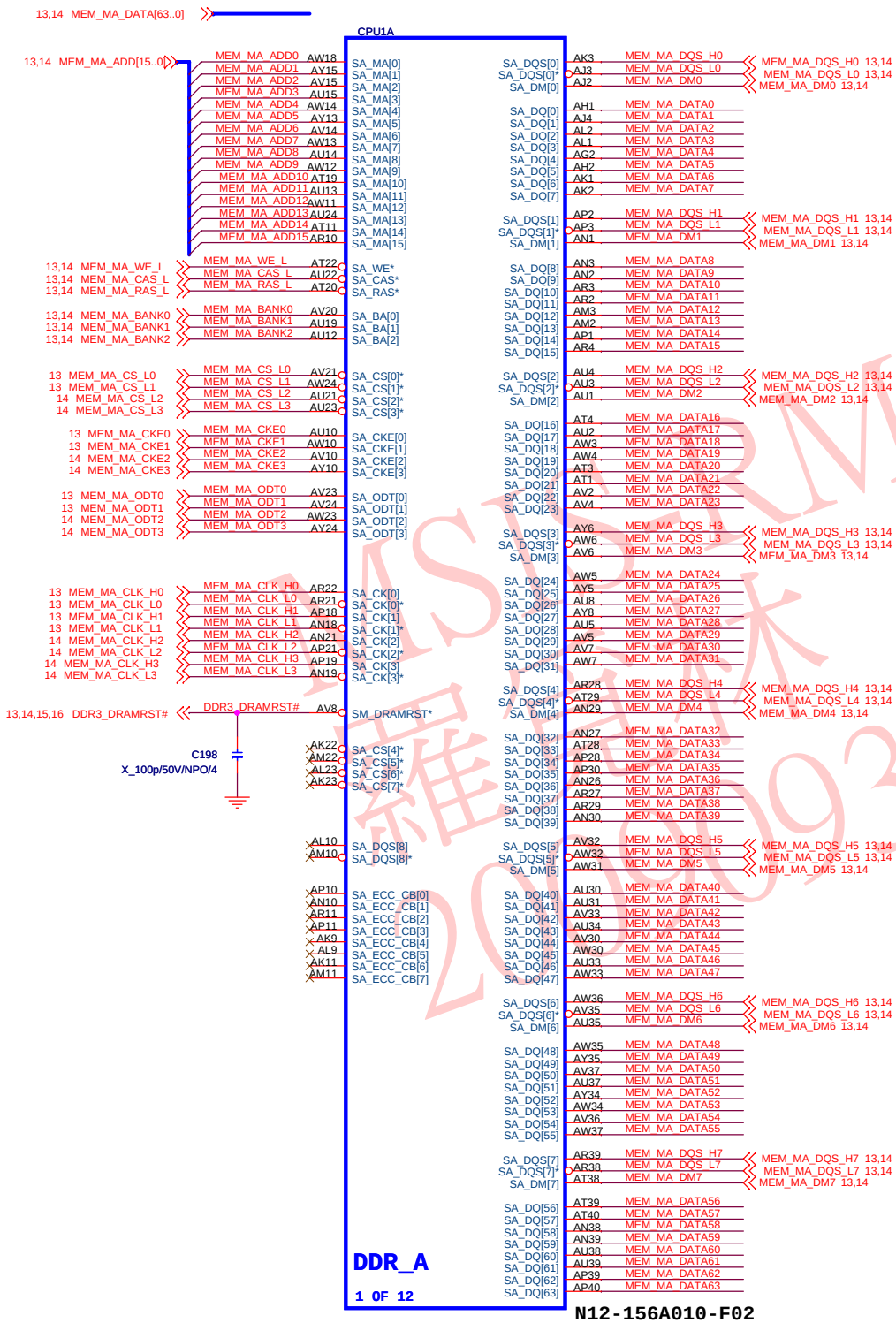
Notes:

1. This setting is defined for future use; no specific Intel Xeon processor 5500 series SKU is defined with ICC_MAX = 50A
2. General rule: Set PWM IMON slope to: 900mV=IMAX, where IMAX =IccMAX with one exception: for Intel® Xeon® Processor W5580 set IMON slope to 900mV=180A, but for all other SKUs they have to match, as shown above. Consult your PWM data sheet for the IMON slope setting.

Market Segment Selection Truth Table for MSID[2:0]

MSID2	MSID1	MSID0	Description[1]
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	2009A FMB processors supported [2]
1	1	0	2009B FMB processors supported [3]
1	1	1	Reserved

2. Processors specified for use with a 65W07 capable thermal solution. Refer to the *Clarkdale Processor, Havendale Processor & Lynnfield Processors and LGA1156 Socket Thermal/ Mechanical Specifications and Design Guidelines* for a list of SKUs.
3. Processors specified for use with a 95W07 (or 65W07) capable thermal solution. Refer to the *Clarkdale Processor, Havendale Processor & Lynnfield Processors and LGA1156 Socket Thermal/Mechanical Specifications and Design Guidelines* for a list of SKUs.



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Size	Document Description	Rev
Custom	CPU-Memory CH-A	V10

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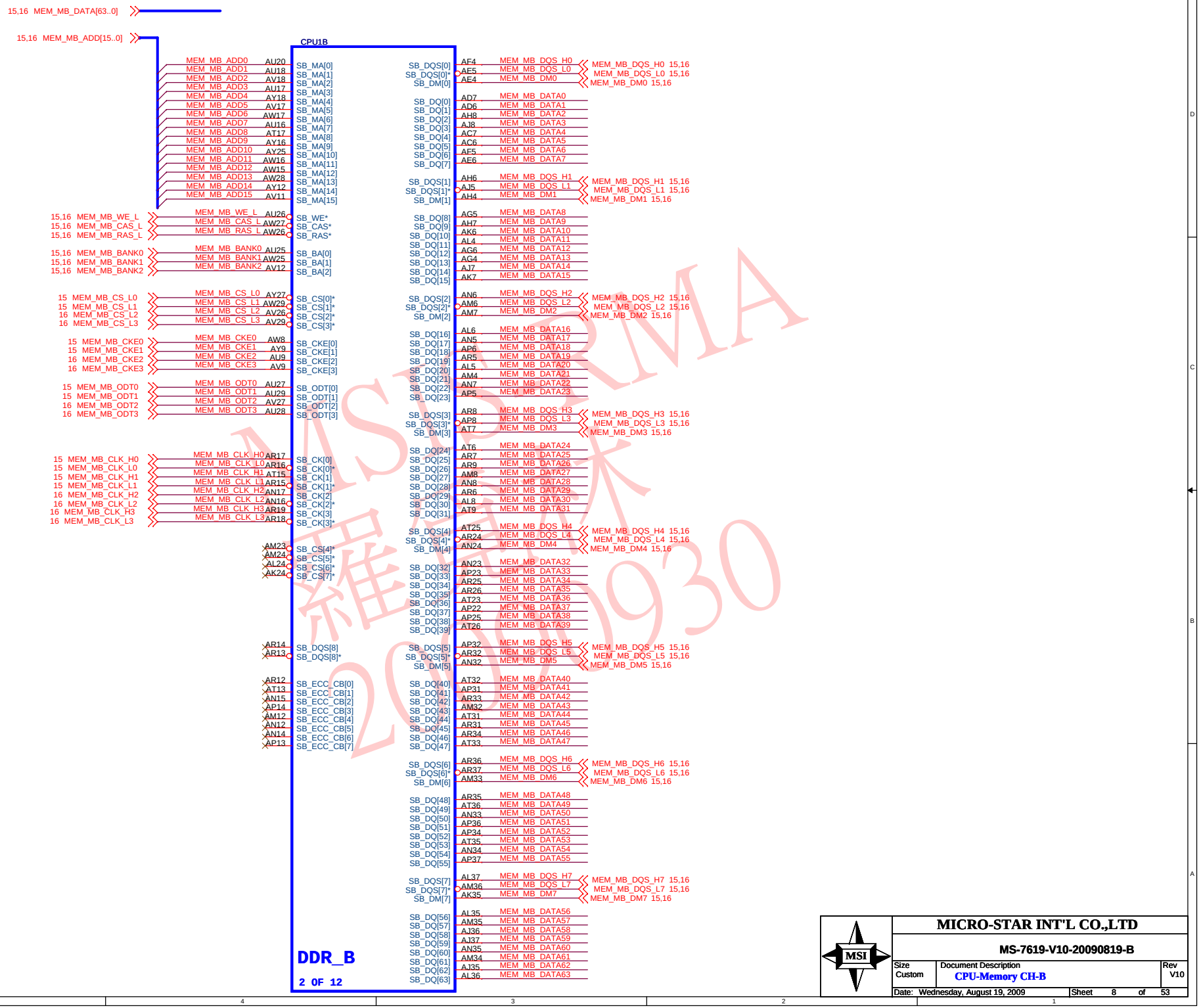

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Size	Document Description	Rev
Custom	CPU-Memory CH-B	V10

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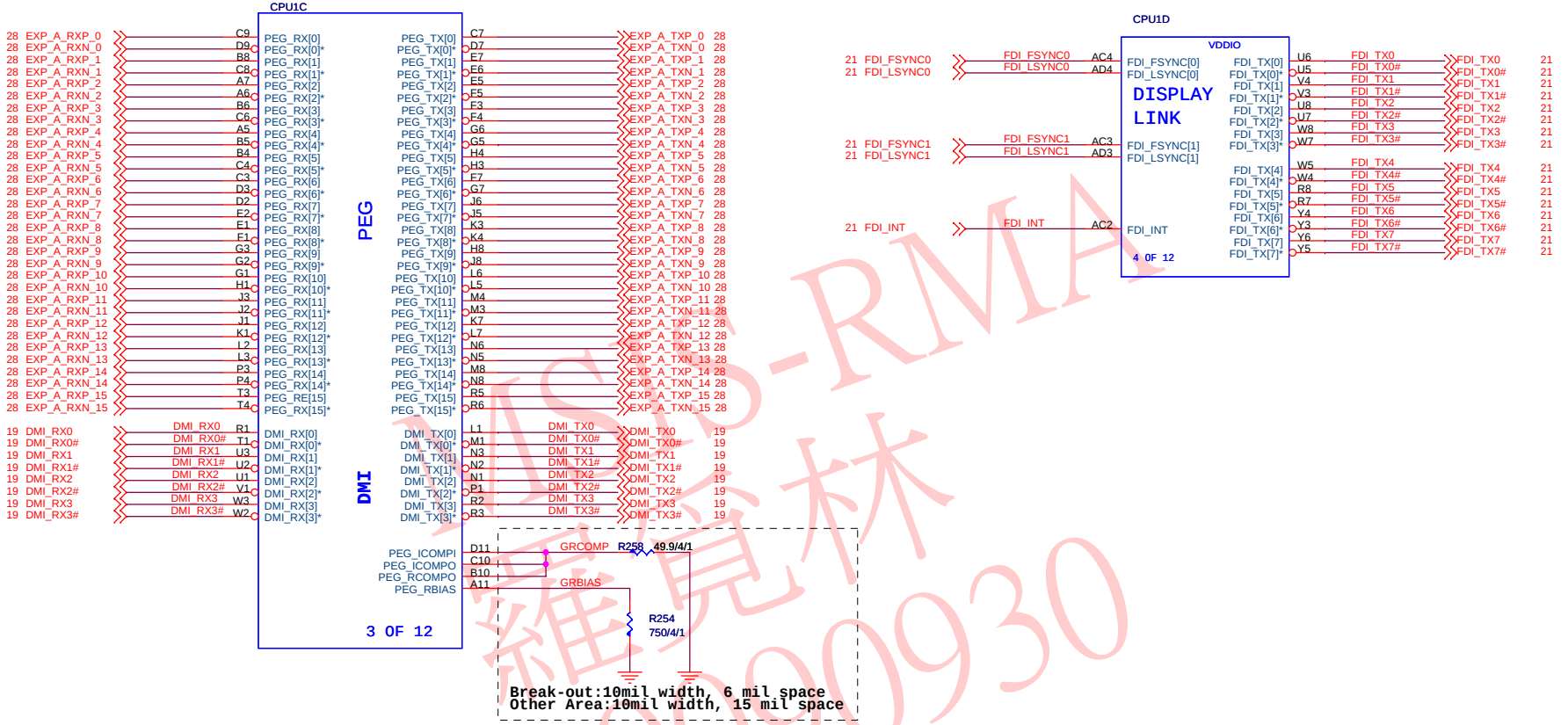

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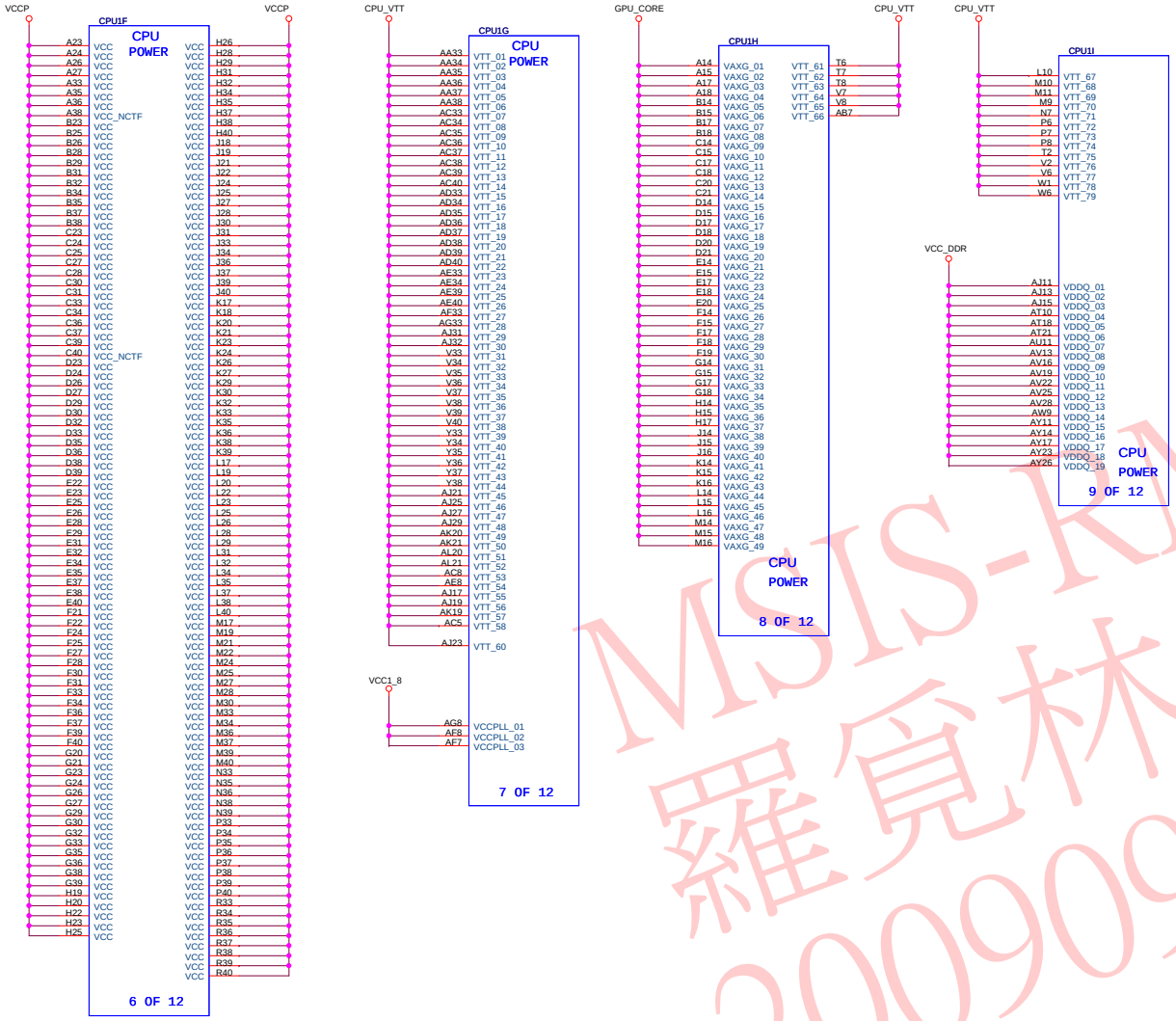
Date: Wednesday, August 19, 2009		Sheet 9 of 53	



Processor C-State Power Specifications

Package C-State[1]	130W	95W	80W[2]	60W[3]	38W
C1E	35 W	30 W	30/40 W	22 W	16 W
C3	30 W	26 W	26/35 W	18 W	12 W
C6	12 W	10 W	10/15 W	8 W	8 W

Notes:

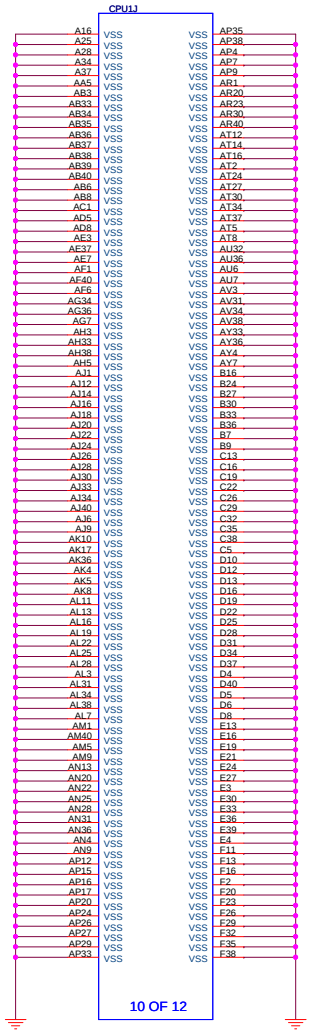
1. Specifications are at T_{case} = 50C with all cores in the specified C-State.
2. Standard/Basic SKUs.
3. Applies to Low Power SKU and Intel® Xeon® Processor L5518.

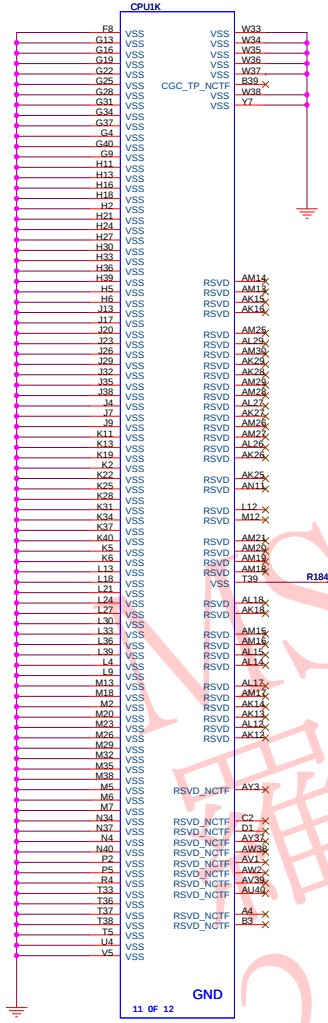
Processor Core Active and Idle Mode DC Voltage and Current Specifications

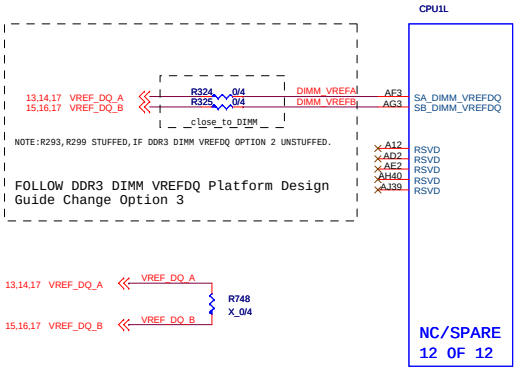
Symbol	Parameter	Min	Typ	Max	Unit
VID	VID Range	0.6500		1.4000	V
V_{CC}	V_{CC} for processor core	See Table 36 and Figure 12			V
$V_{CC,BOOT}$	Default V_{CC} voltage for initial power up	-	1.10	-	V
I_{CC}	2009A FMB I_{CC}; for Havendale and Clarkdale processors support	-	-	75	A
I_{CC}	2009B FMB I_{CC}; for Lynnfield, Havendale, and Clarkdale processors support	-	-	100	A
I_{CC_TDC}	2009A FMB Sustained I_{CC}; recommended design target for Havendale and Clarkdale processors support	-	-	60	A
I_{CC_TDC}	2009B FMB Sustained I_{CC}; recommended design target for supporting both Lynnfield, Havendale, and Clarkdale processors	-	-	90	A

Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Processor Core voltage with respect to Vss	-0.3	1.55	V
V_{TT}	Voltage for the memory controller and Shared Cache with respect to V_{SS}	-0.3	1.21	V
V_{DDQ}	Processor I/O supply voltage for DDR3 with respect to V_{SS}	-0.3	1.65	V
V_{CCPLL}	Processor PLL voltage with respect to V_{SS}	-0.3	1.98	V
V_{AXG}	Graphics voltage with respect to V_{SS}	-0.3	TBD	V
$T_{STORAGE}$	Storage temperature	-40	85	°C







Platform Design Guide DDR3 DIMM VREFDQ Change Summary

Option 1: Fixed DIMM VREFDQ Divider (Default Stuffing) – No Change

- Fixed voltage resistor divider placed on motherboard between channel A DIMM0 and B DIMM1 connectors
- Currently documented in latest platform design guide

Option 2: Programmable DIMM VREFDQ on motherboard – New Requirement

- Programmable divider placed next to option 1 on motherboard
  - Digital potentiometer & op amp on motherboard, controlled by Ibex Peak SMBUS
- Details will be added in next release of platform design guide

Option 3: Processor Generated DIMM VREFDQ – New Requirement

- Intel investigating future processor VREFDQ generation to replace options 1 and 2.
- Route processor signal balls AF3 and AG3 to DIMM connectors
- Details will be added in next release of platform design guide

2DPC DDR3 DIMM VREFDQ Requirements

"Dale" Processor/Platform Details

• Processors don't have DIMM VREFDQ capability

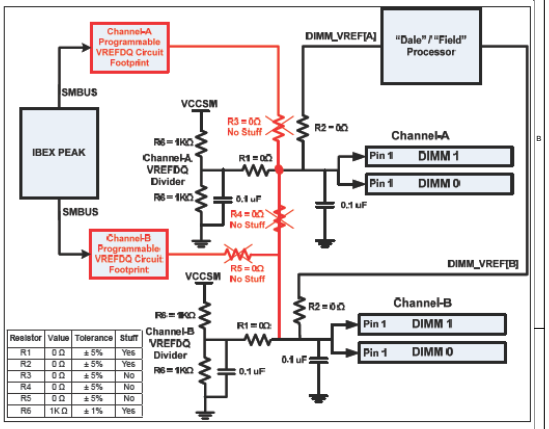
• Platforms will use VREFDQ generated from fixed motherboard voltage divider

"Field" Processor/Platform Details

• Processors will generate and drive VREFDQ and override fixed motherboard voltage divider

• Feature won't be fully enabled until a future release of MRC.

  • Current design will use fixed motherboard voltage dividers



Resistor	Value	Tolerance	Stuff
R1	0 Ω	± 5%	Yes
R2	0 Ω	± 5%	Yes
R3	0 Ω	± 5%	No
R4	0 Ω	± 5%	No
R5	0 Ω	± 5%	No
R6	1K Ω	± 1%	Yes

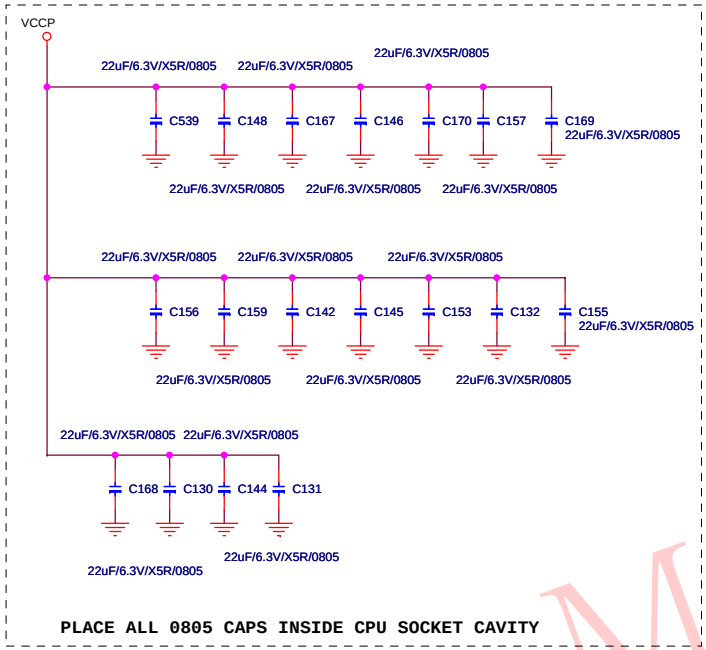
• Populate Channel A and B fixed DIMM VREFDQ Voltage Dividers placed on motherboard next to DIMM connectors

• Route processor DIMM_VREF[A] and [B] signals to DIMM connector VREFDQ pins

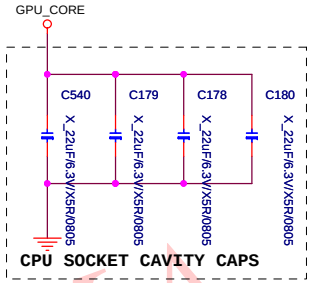
• Leave programmable DIMM VREFDQ circuit footprints on motherboard next to DIMM connectors

  – Digital potentiometer and op-amp controlled by Ibex Peak SMBUS
  – May be required at a later time if validation shows its needed

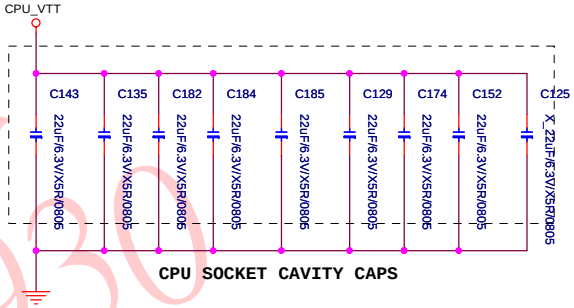
+CPU_VCCP-Decoupling

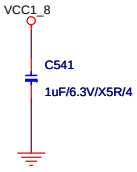


+CPU_GFX Decoupling

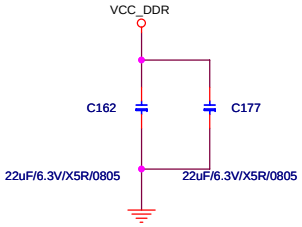


+CPU_VTT Decoupling





+1.5V_DDR3-Decoupling



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	MS-7619-V10-20090819-B	
Size: Custom	Document Description: CPU-Decoupling	Rev: V10
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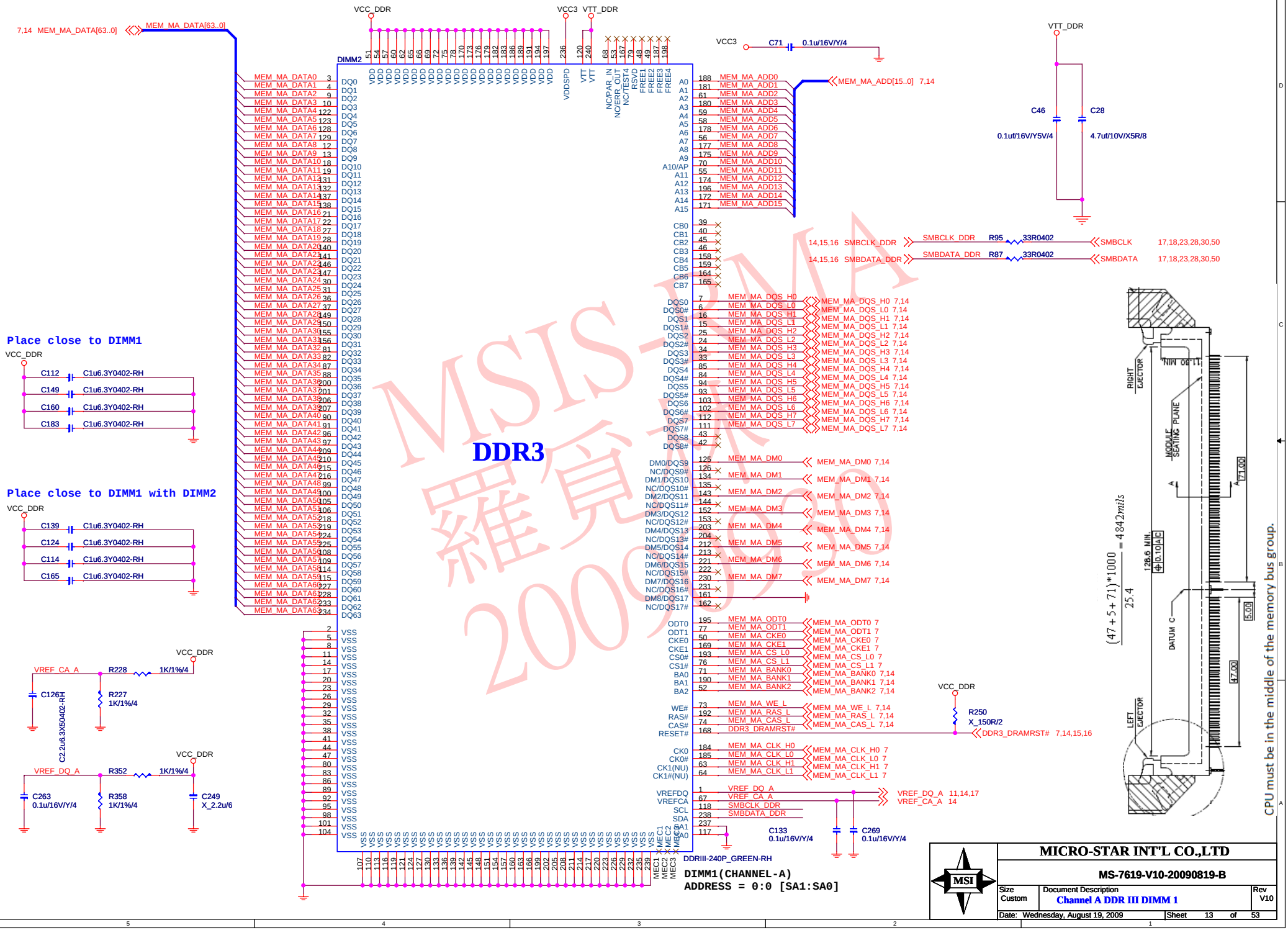
DDRIII DIMM_A1 (Revise History)



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MS-7619-V10-20090819-B	
Size: Custom	Document Description: Channel A DDR III DIMM 1
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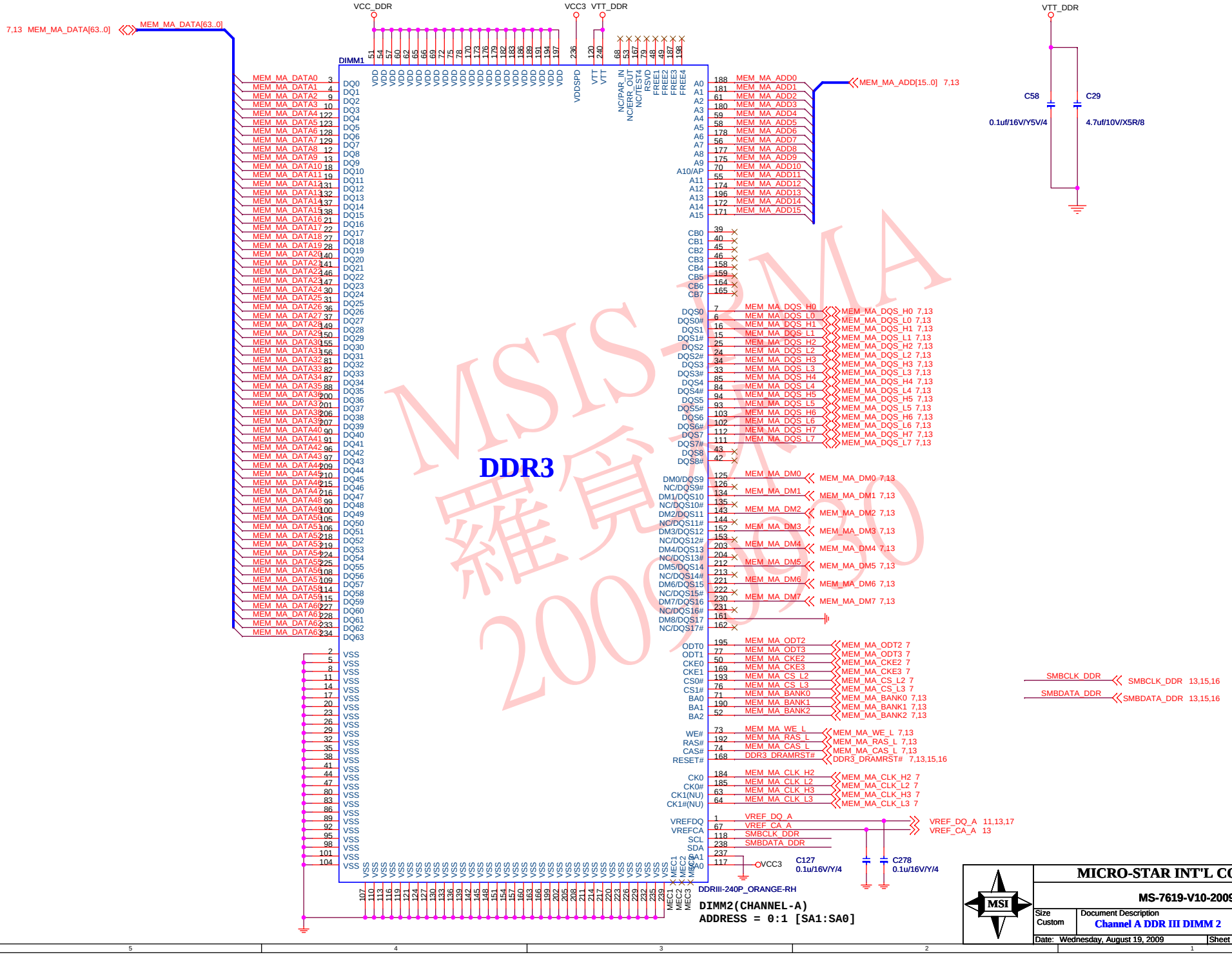
DDRIII DIMM_A2 (Revise History)



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MS-7619-V10-20090819-B	
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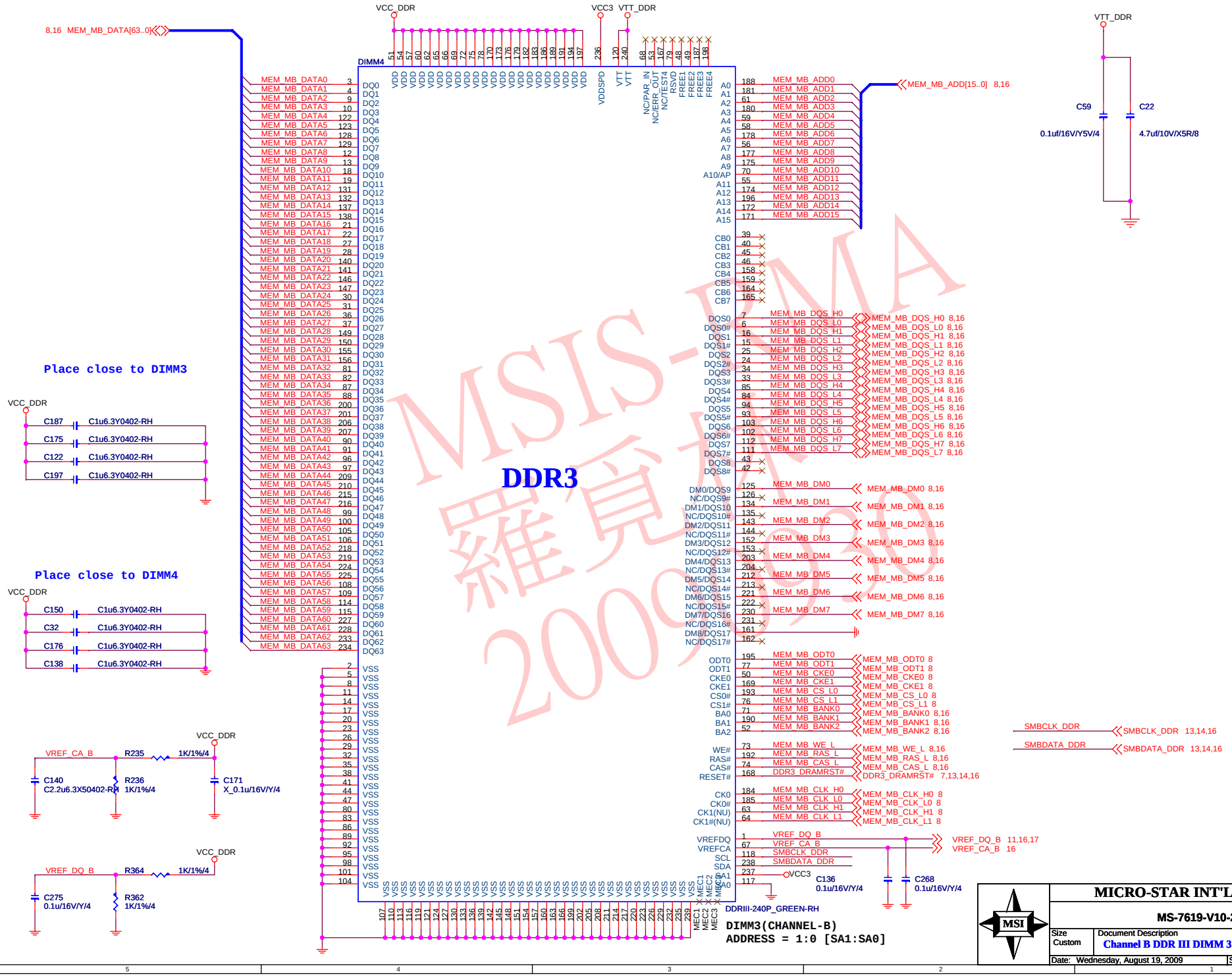
DDRIII DIMM_B1 (Revise History)



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Size: Custom	Document Description: Channel B DDR III DIMM 3		Rev: V10
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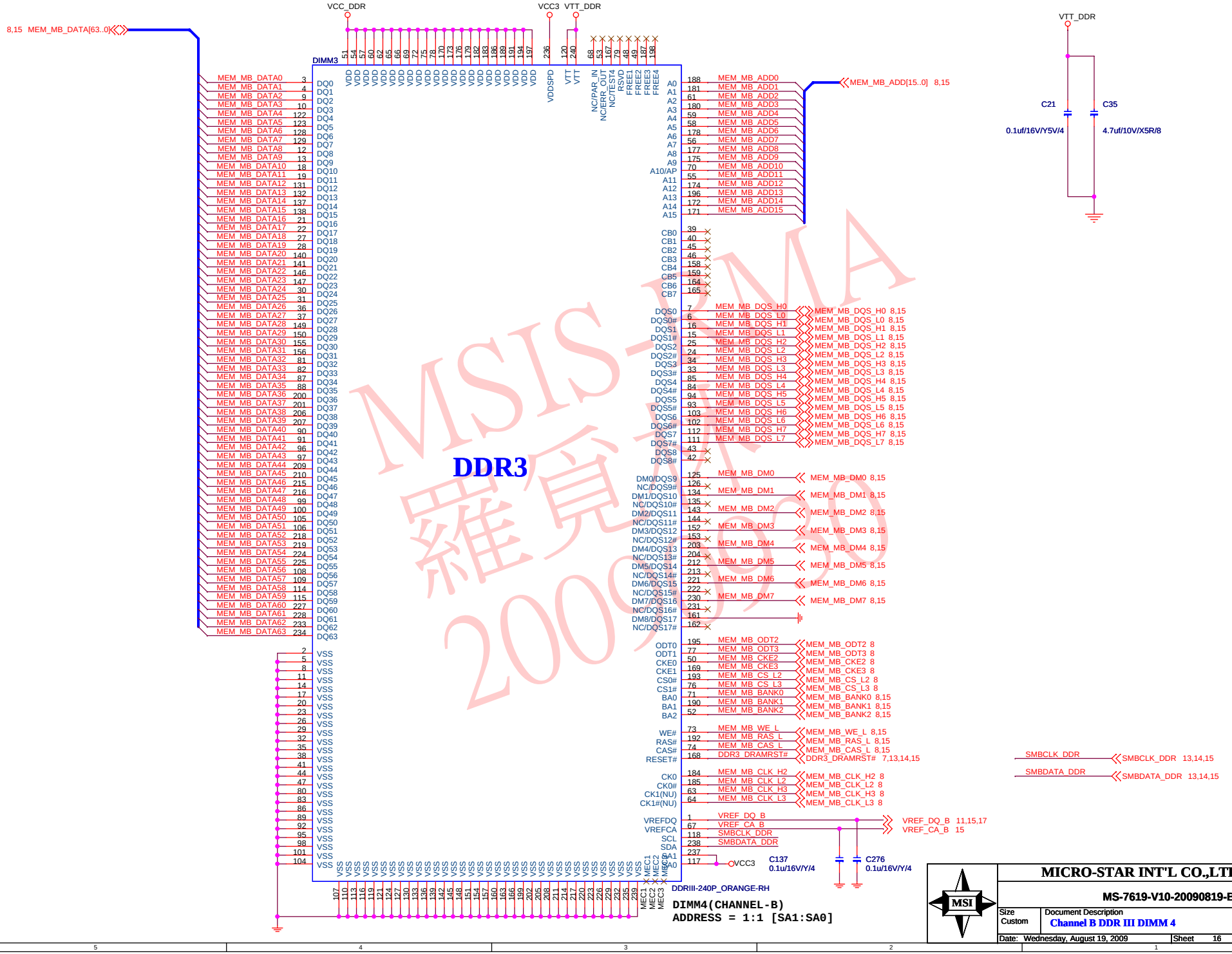
DDRIII DIMM_B2 (Revise History)



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Size: Custom	Document Description: Channel B DDR III DIMM 4	Rev: V10
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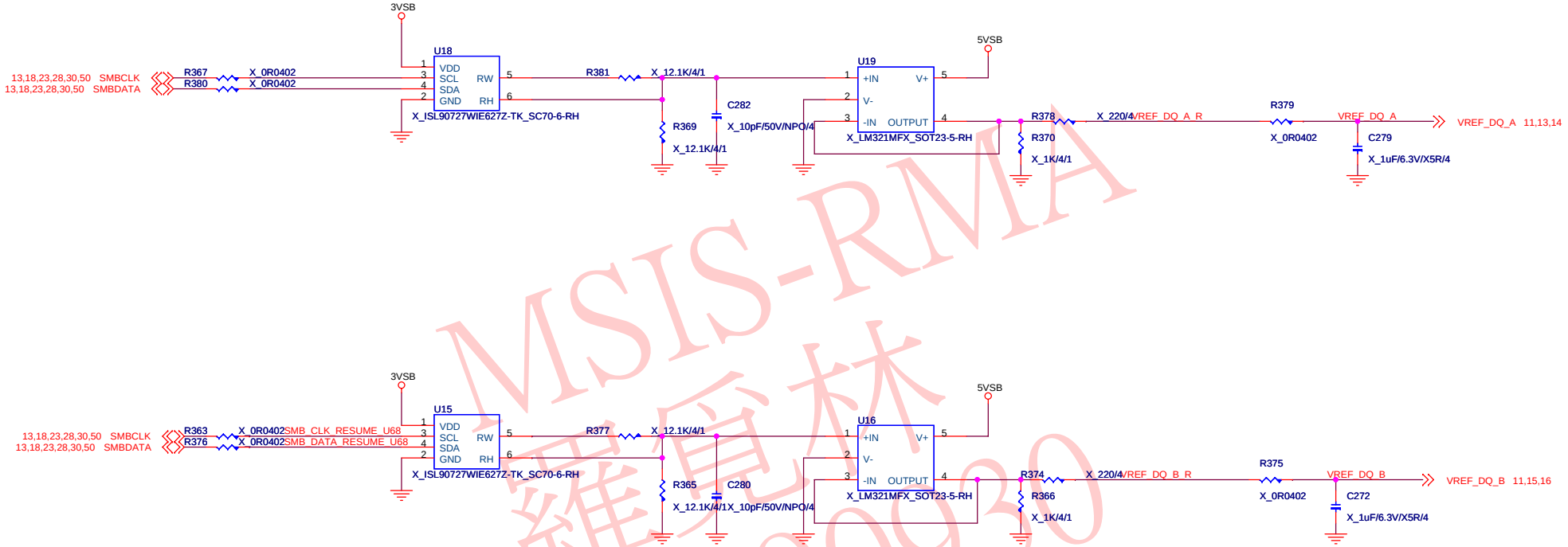

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DIMM VREF (Option)	Rev: V10
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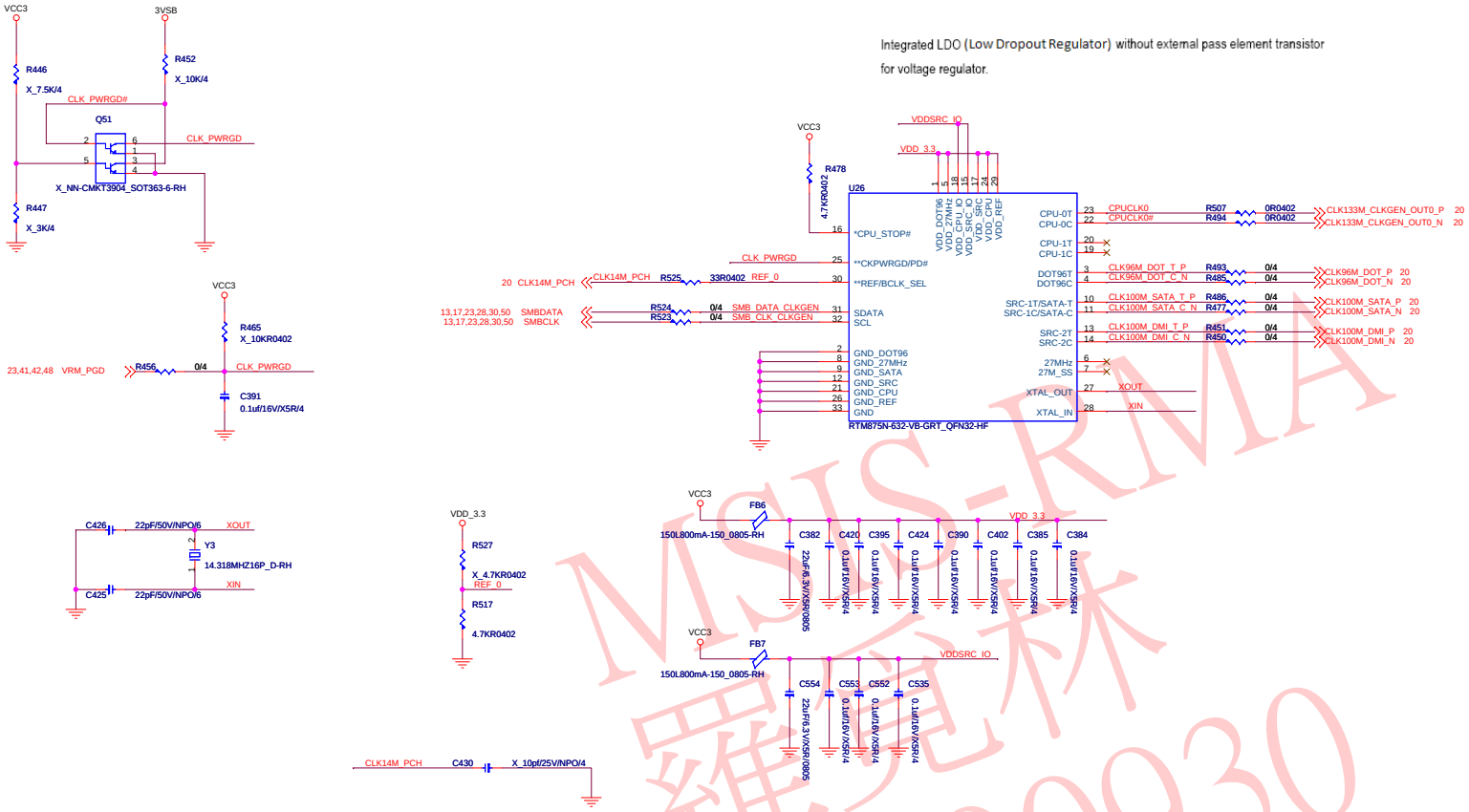

REF_0	CPU_0	CPU_1
0	133	133
1 (0.7~1.5V)	100	100

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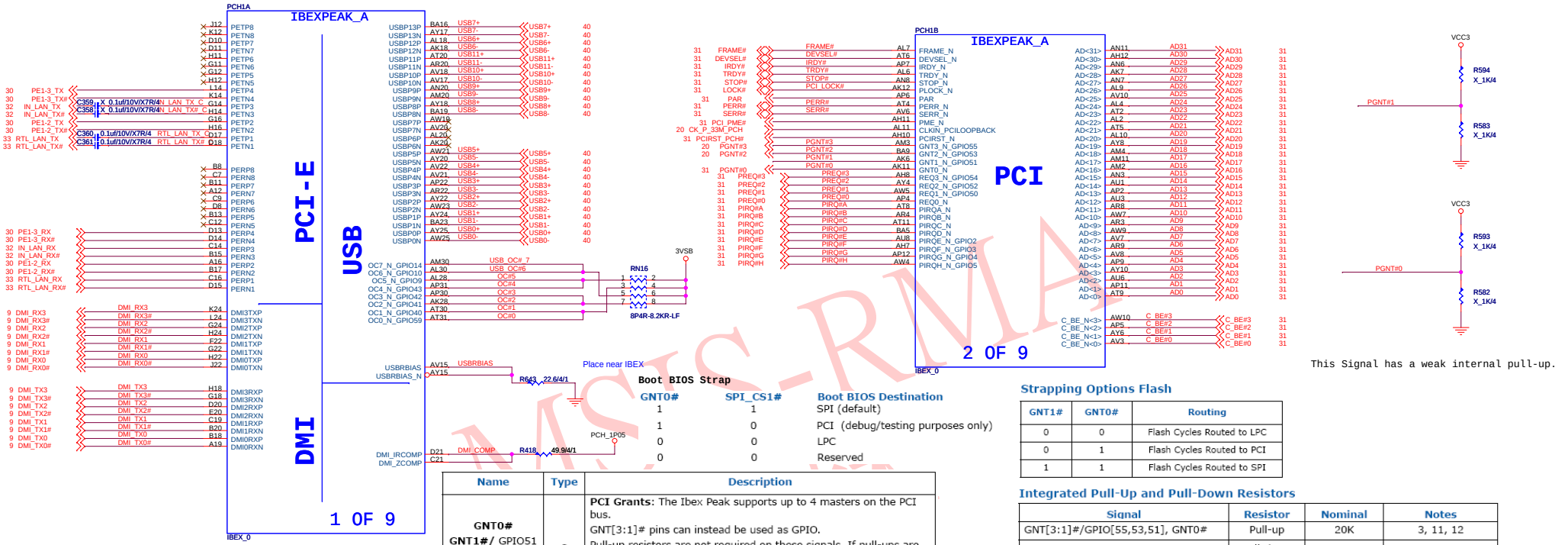


This Signal has a weak internal pull-up.

0B1-7613006-IY6

Boot BIOS Strap

GNT0#	SPI_CS1#	Boot BIOS Destination
1	1	SPI (default)
1	0	PCI (debug/testing purposes only)
0	0	LPC
0	0	Reserved

Name	Type	Description
GNT0# **GNT1#/** GPIO51 **GNT2#/** GPIO53 **GNT3#**/GPIO55	O	**PCI Grants:** The Ibex Peak supports up to 4 masters on the PCI bus. GNT[3:1]# pins can instead be used as GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. **NOTE:** GNT[3:0]# are sampled as a functional strap. See Section 2.30.1 for details.

Strapping Options Flash

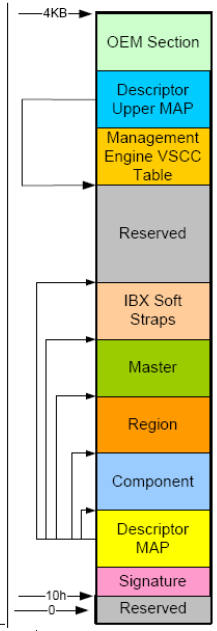
GNT1#	GNT0#	Routing
0	0	Flash Cycles Routed to LPC
0	1	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI

Integrated Pull-Up and Pull-Down Resistors

Signal	Resistor	Nominal	Notes
GNT[3:1]#/GPIO[55,53,51], GNT0#	Pull-up	20K	3, 11, 12
SPI_MOSI	Pull-down	20K	3,7
SPI_CS1#, SPI_MISO	Pull-up	20K	3

3. Simulation data shows that these resistor values can range from 15 kΩ to 40 kΩ.
7. The pull-up or pull-down on this signal is only enabled at boot/reset for strapping function.
11. The pull-up on this signal is not enabled when PCIRST# is high.
12. The pull-up on this signal is not enabled when PWROK is low.

Flash Descriptor



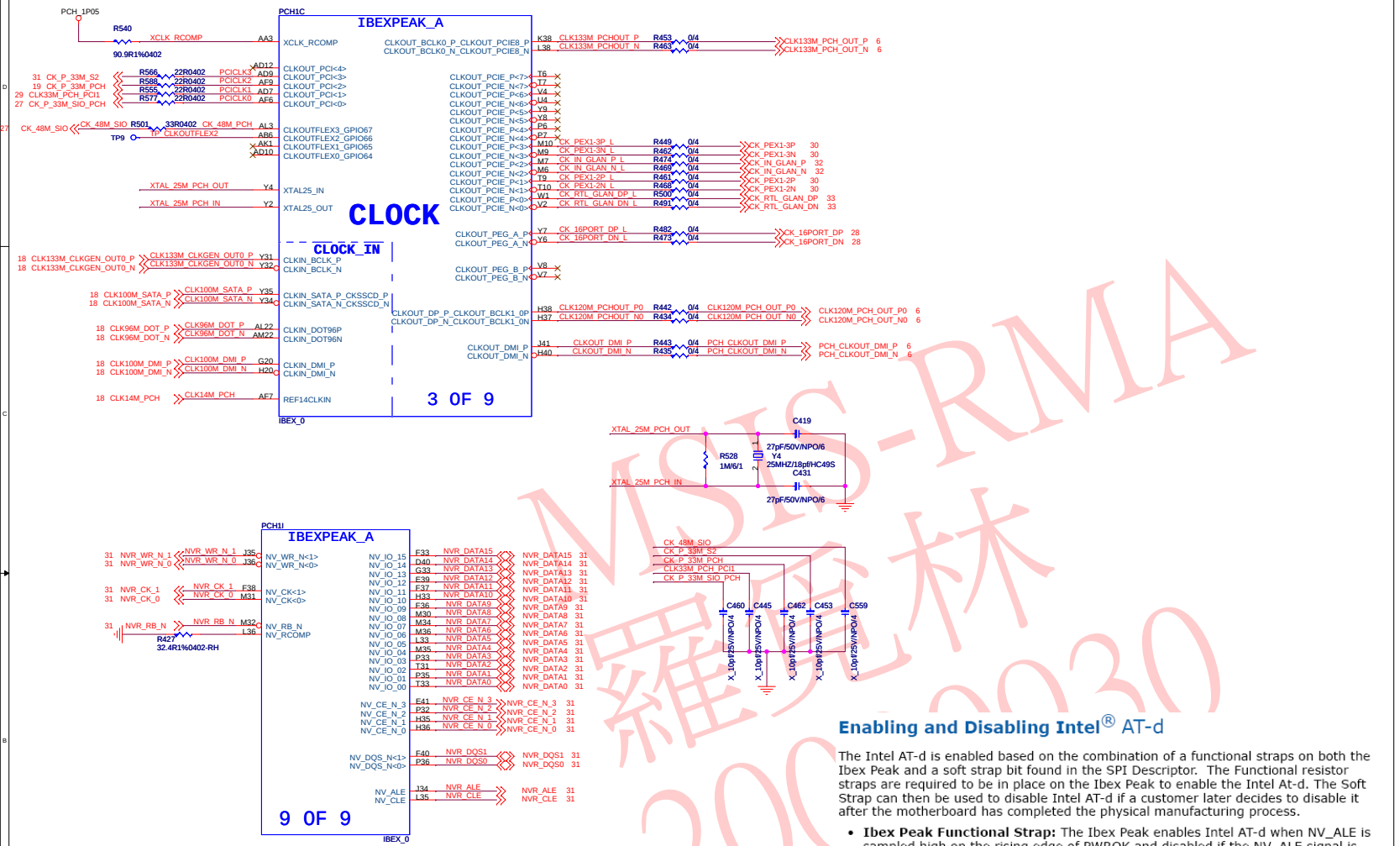
- The Flash signature at the bottom of the flash (offset 0) must be 0FF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, ME and GbE regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel® ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image. This table is NOT used by Intel® ME Ignition FW only. BIOS and GbE write and erase capabilities depend on LVSCC and UVSCC registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

Boot Flow for Ibex Peak

When booting from Global Reset the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 at address 0x0. The descriptor fetch is triggered whichever comes first, the assertion of MEPWROK or deassertion of LAN_RST#. If the signature is present and valid, then the PCH controller will boot in Descriptor mode. It will load up the descriptor into corresponding registers in the PCH. If the signature is NOT present the PCH will boot in non descriptor mode where integrated LAN and all Intel Management Firmware will be disabled. Whether there is a valid descriptor or not, the PCH will look to the GNT0# and SPI_CS1#1 (Boot BIOS Destination straps) to determine if BIOS is to be booted from Firmware hub or SPI flash.

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Ibex Peak based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers. The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

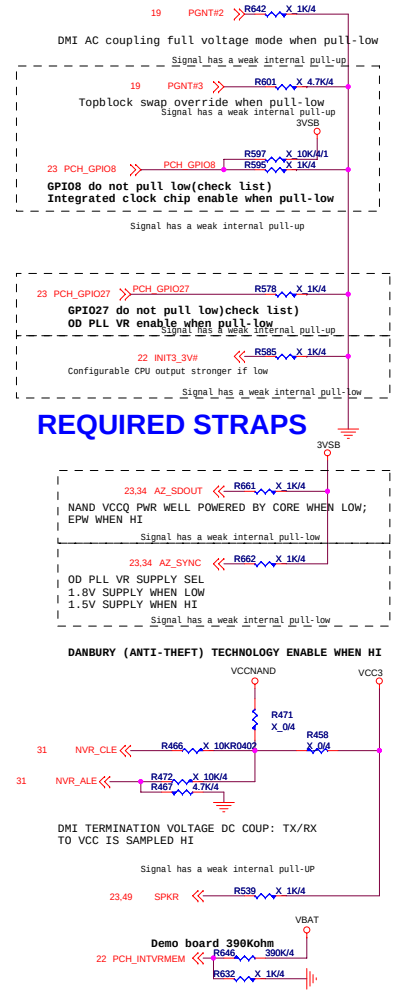
The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.



Enabling and Disabling Intel® AT-d

The Intel AT-d is enabled based on the combination of a functional straps on both the Ibex Peak and a soft strap bit found in the SPI Descriptor. The Functional resistor straps are required to be in place on the Ibex Peak to enable the Intel At-d. The Soft Strap can then be used to disable Intel AT-d if a customer later decides to disable it after the motherboard has completed the physical manufacturing process.

- **Ibex Peak Functional Strap:** The Ibex Peak enables Intel AT-d when NV_ALE is sampled high on the rising edge of PWROK and disabled if the NV_ALE signal is sampled low. See Section 2.29 for details.
- **Soft Strap:** The Intel AT-d Disable bit (bit 27) in the PCHSTRP0 register (FPSBA + 0h) within the flash descriptor can act as an override to the functional straps on both the Ibex Peak. When set, Intel AT-d will be disabled regardless of the values of the functional straps on the Ibex Peak. This bit along with the functional strap must be appropriately configured to enable Intel AT-d.



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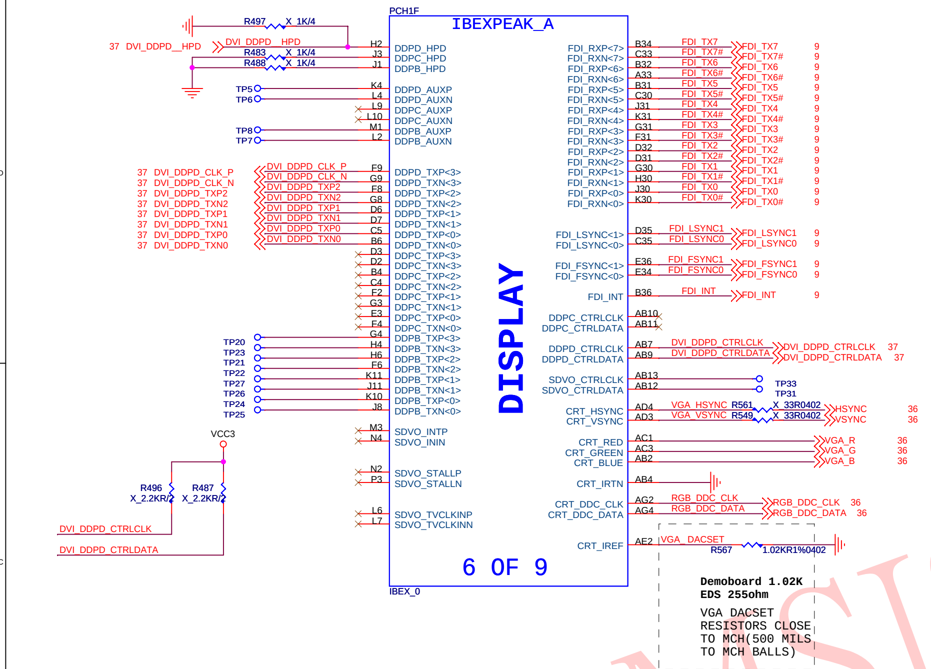


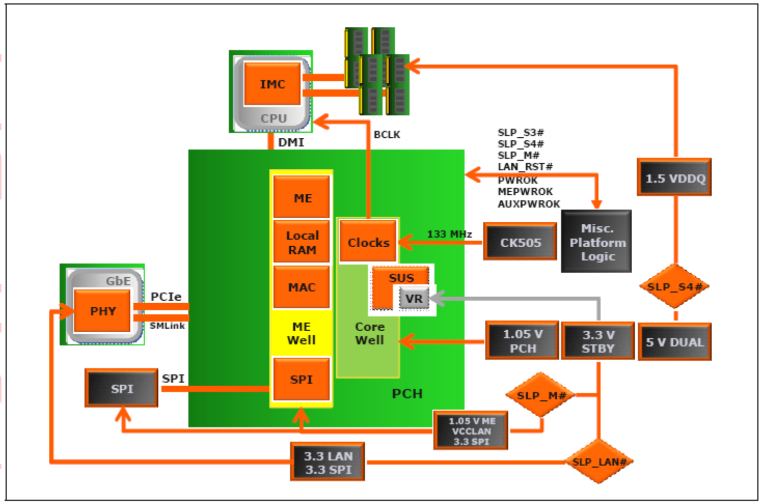
Intel® Management Engine Overview

The Intel® Management Engine is an integrated part of Ibex Peak. It operates by loading firmware code from SPI flash and executing it in memory. This firmware code allows the Intel® Management Engine to perform a variety of security and management related functions. Intel® Management Engine operates independent of the host processor and its execution capabilities are securely isolated from the main system's BIOS execution flow. This allows the Intel® Management Engine to operate as part of the Trusted Platform Environment, as well as independent of platform power states.

In the highest power state of the platform, S0, the Intel® Management Engine operates in the manageability power state M0. It pulls firmware code from SPI flash into main system memory, then inputs the utilized code through a caching algorithm so that it can more efficiently operate out of dedicated, protected SRAM internal to Ibex Peak, reducing the number of transactions with main memory and the memory controller inside the processor.

In lower power states, S3-S5, the Intel® Management Engine operates in manageability power state M3. It executes code exclusively off dedicated, protected SRAM in Ibex Peak, requiring neither main memory nor the memory controller inside the processor to be powered.

Figure 24-2. Intel® Management Engine System Voltage Regulator Control Block Diagram

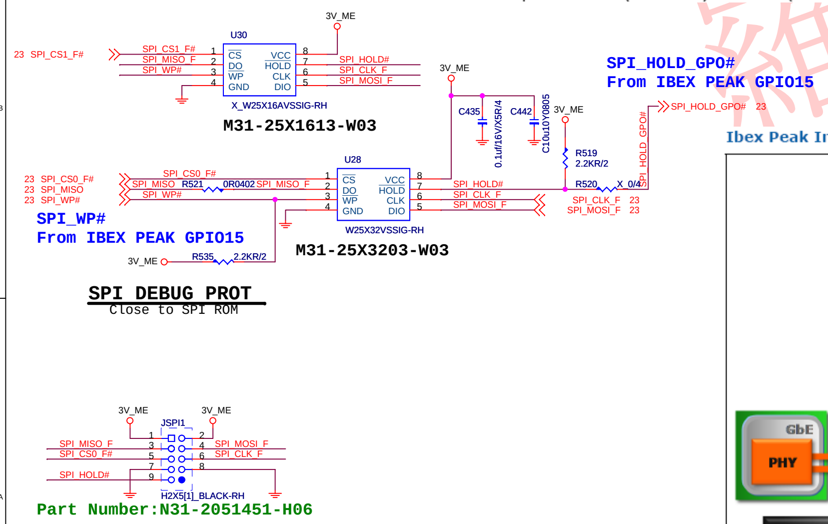


If having question, refer to chapter 24 of 376563_Piketon/Kings Creek and Foxhollow Platform Design Guide

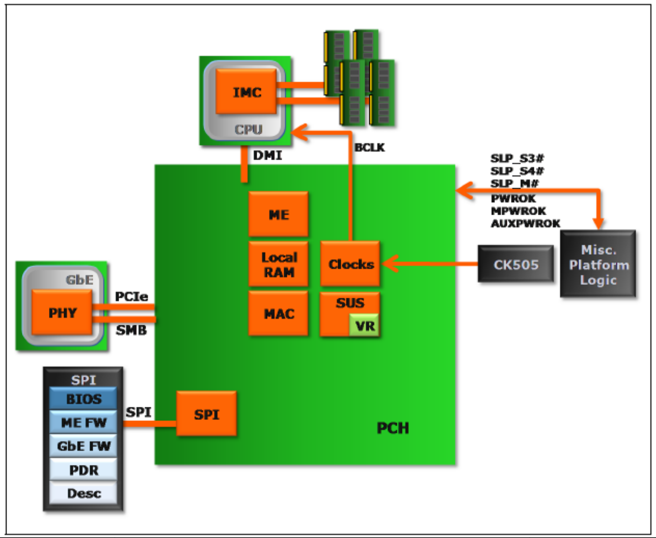
Flexible Display Interface

The Flexible Display Interface (Intel® FDI) is a bus technology that utilizes differential signaling to transport display data from a pixel source Havendale to a sink Ibex Peak. There are two Flexible Display Interface channels- A and B which are independently controlled. Each channel from Havendale include 4 Tx differential pairs comprising the data link, used for transporting pixel and framing data from the display engine. Two single-ended LineSync and FrameSync inputs. Single-ended DISP_INT is used for interrupts from sink (Ibex Peak) to source (Havendale).

SPI FLASH ROM



Ibex Peak Intel® Management Engine High-Level Block Diagram



Descriptor Master Region

The master region defines read and write access setting for each region of the SPI device. The master region recognizes three masters: BIOS, Gigabit Ethernet, and Management Engine. Each master is only allowed to do direct reads of its primary regions.

Region Access Control Table

	Master Read/Write Access		
Region	**CPU and BIOS**	**ME**	**GbE Controller**
Descriptor	N/A	N/A	N/A
BIOS	CPU and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Management Engine	Read / Write	ME can always read from and write to ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

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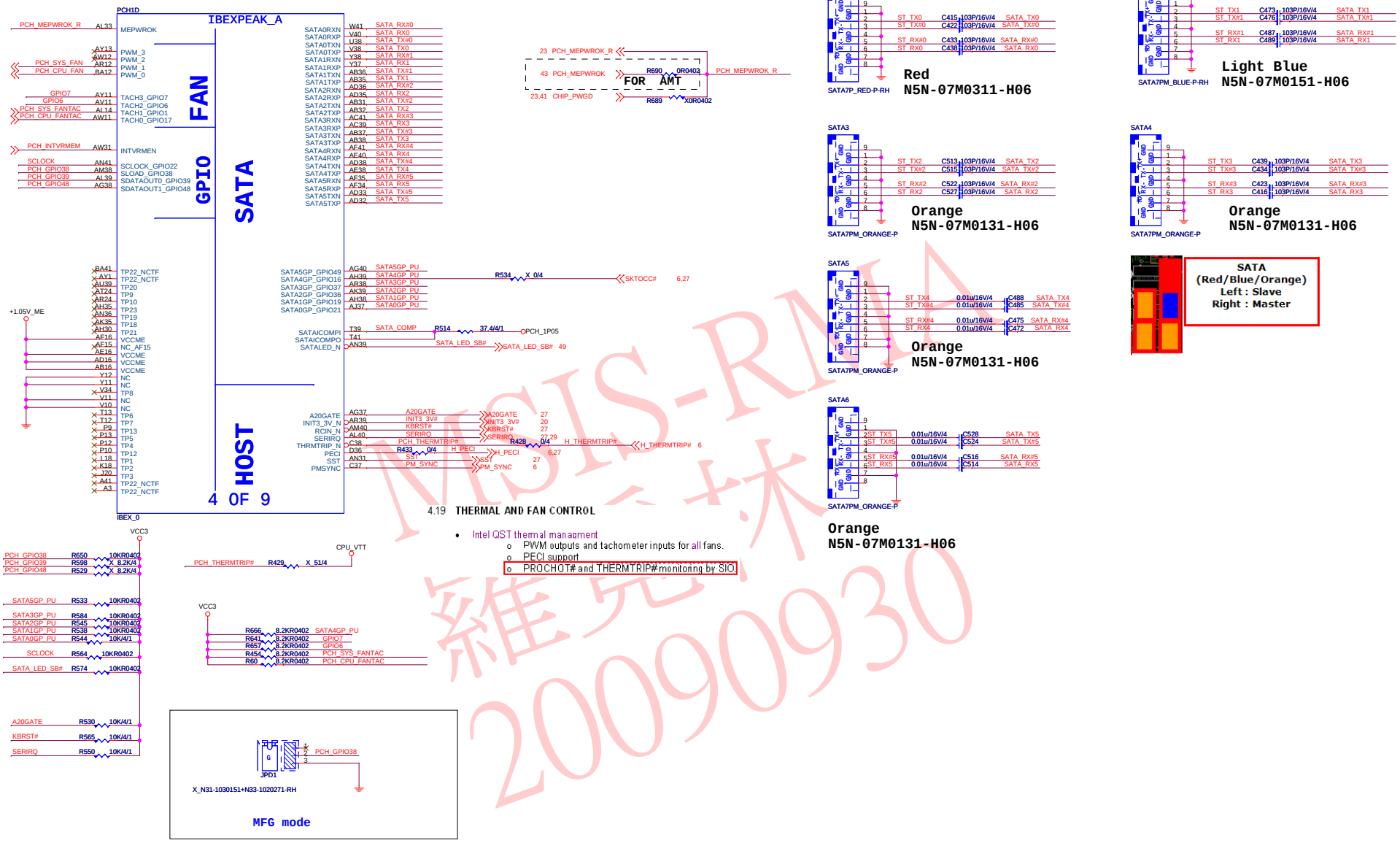
SATA connector



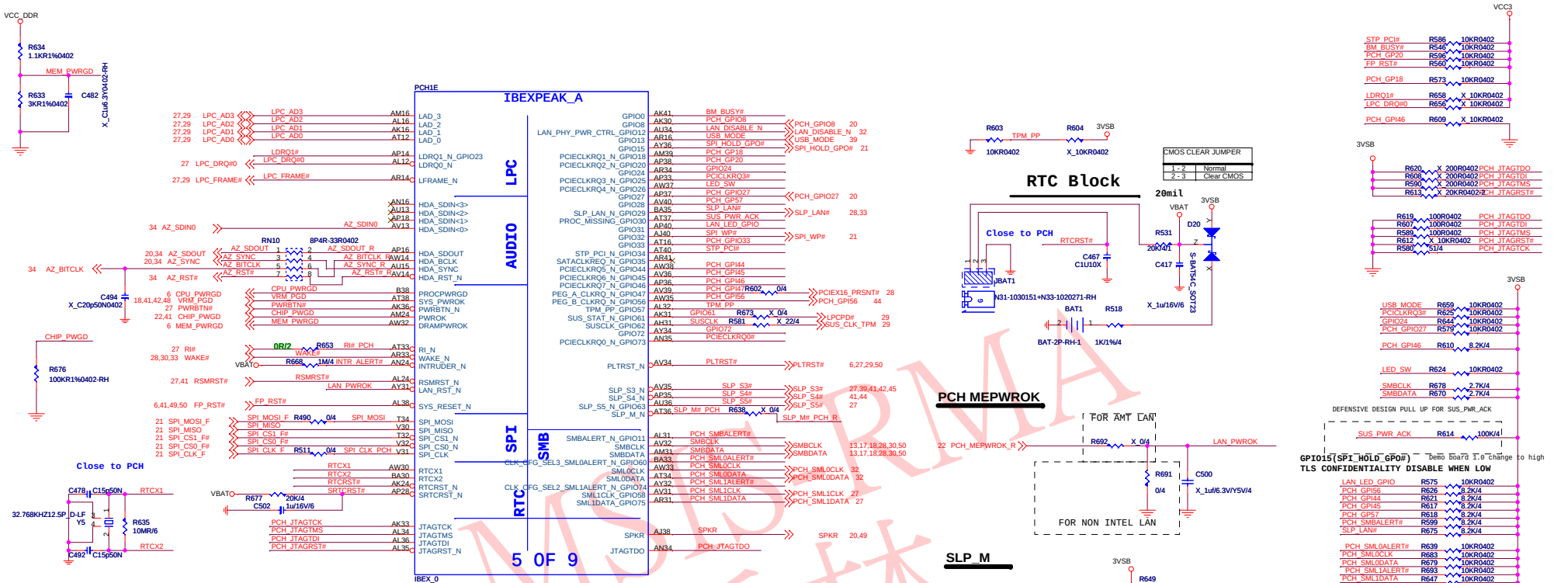
4.19 THERMAL AND FAN CONTROL

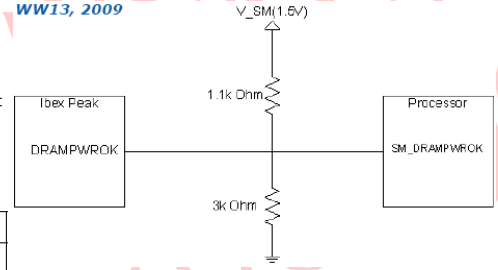
- Intel QST thermal management
  - PWM outputs and tachometer inputs for all fans.
  - PECI support
  - PROCHOT# and THERMTRIP# monitoring by SIO

Name	Type	Description
SLOAD/GPIO38	OD O	**SGPIO Load:** The controller drives a '1' at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SGPIO interface is not used, this signal can be used as a GPIO.

SGPIO Signals

During reset all SGPIO pins will be in tri-state state. The interface will continue to be in tri-state state after reset until the first transmission occurs when software programs the message buffer and sets the transmit bit CTL.TM. The SATA Host controller will initiate the transmission by driving SCLOCK and at the same time drive the SLOAD to '0' prior to the actual bit stream transmission. The Host will drive SLOAD low for at least 5 SCLOCK then only start the bit stream by driving the SLOAD to high. SLOAD will be driven high for 1 SCLOCK follow by vendor specific pattern that is default to "0000" if software has yet to program the value. A total of 21-bit stream from 7 ports (Port0, Port1, Port2, Port3, Port4 Port5 and Port6) of 3-bit per port LED message will be transmitted on SDATAOUT0 pin after the SLOAD is driven high for 1 SCLOCK. Only 3 ports (Port4, Port5 and Port6) of 9 bit total LED message follow by 12 bits of tri-state value will be transmitted out on SDATAOUT1 pin.





SLP_LAN# Usage Model

SLP_LAN# is a signal on Ibex Peak which indicates when the Intel LAN PHY device must be powered. This pin should be connected to a power switch to control the 3.3V and any other externally supplied voltages to the external Intel LAN PHY. SLP_LAN# is always deasserted when SLP_S3# and/or SLP_M# is deasserted. SLP_LAN# can also be configured by ME FW or host BIOS to indicate when the Intel LAN PHY should be powered in S3-S5 to support WOL (Host or ME).

Name	Type	Description
GPIO57/**TPM_PP**	I	Used to indicate TPM Physical Presence to the Management Engine, when pulled high.

Name	Type	Description
SUSCLK / GPIO62	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock. Pin may also be used as GPIO62.

Signal	Usage	When Sampled	Comment
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO13	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with HDA_DOCK_RST# (Mobile Only) (Note 4)
GPIO28	I/O	3.3 V	Suspend	GPI	Yes	Unmultiplexed
GPIO57	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO62	I/O	3.3 V	Suspend	Native	No	Multiplexed with SUSCLK

Resistor Stuffing Options

		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stuff	200 Ohms[1]	No Stuff
	R2	No Stuff	100 Ohms[1]	No Stuff
	R10	No Stuff	No Stuff	51 Ohms
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
	R11	No Stuff	No Stuff	51 Ohms
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
	R12	No Stuff	No Stuff	51 Ohms
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	20K Ohms	No Stuff
	R9	10K Ohms	10K Ohms	No Stuff
	R13	No Stuff	No Stuff	51 Ohms

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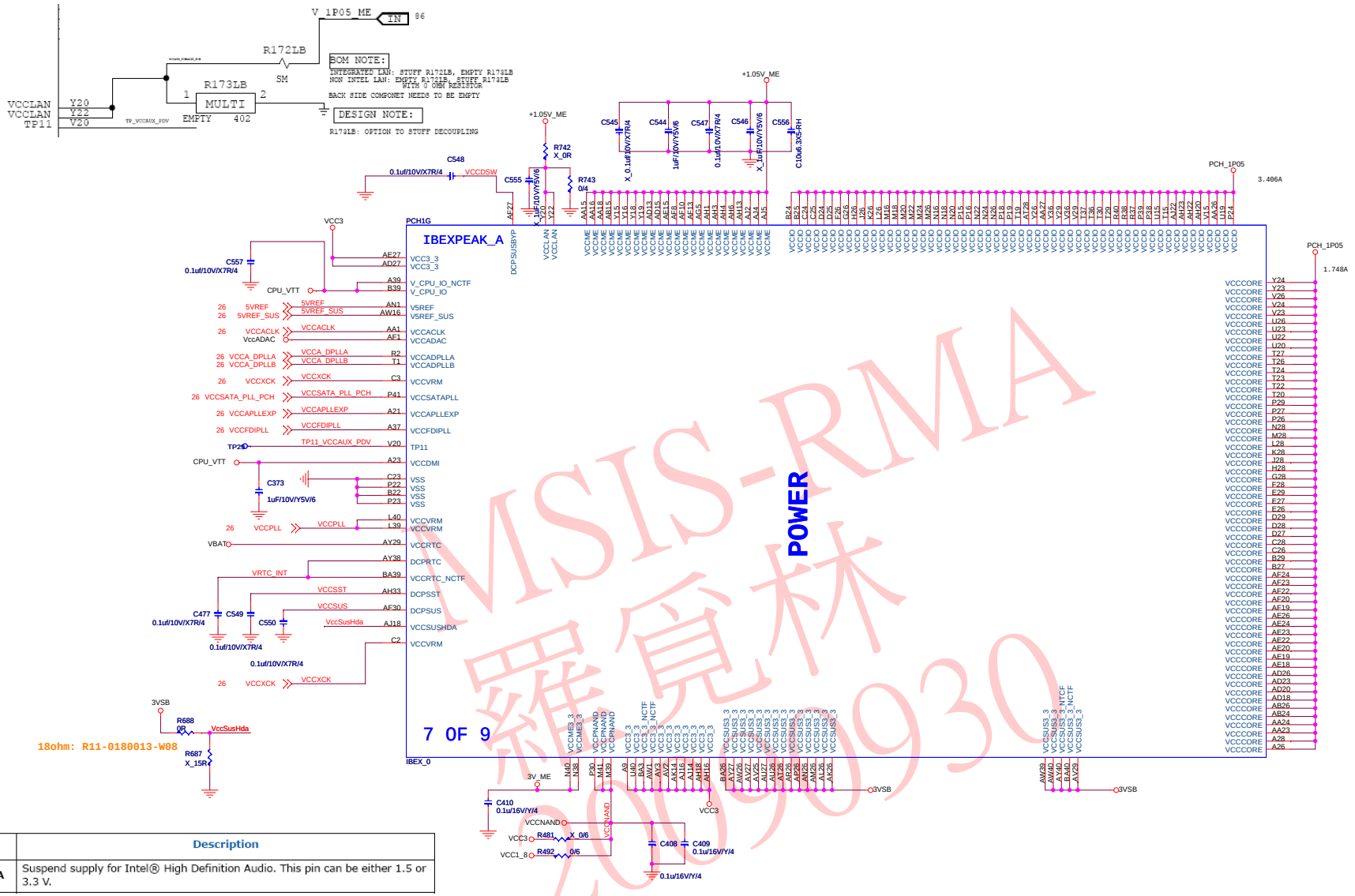

Name	Description
VccSusHDA	Suspend supply for Intel® High Definition Audio. This pin can be either 1.5 or 3.3 V.

Voltage Rail	Voltage	S0 Iccmax Current (A)	S0 Idle Current (A)	Sx Iccmax Current (A)	Sx Idle Current (A)
VccLAN	1.05	0.372	0.078	0.079	TBD
VccSusHDA	3.3	0.006	< 1 (mA)	< 1 (mA)	< 1 (mA)

Symbol	Parameter	Min	Nom	Max	Unit
VccSusHDA	High Definition Audio Controller Suspend Voltage	3.14	3.3	3.47	V
VccSusHDA (low voltage)	High Definition Audio Controller Low Voltage Mode Suspend Voltage	1.43	1.5	1.58	V

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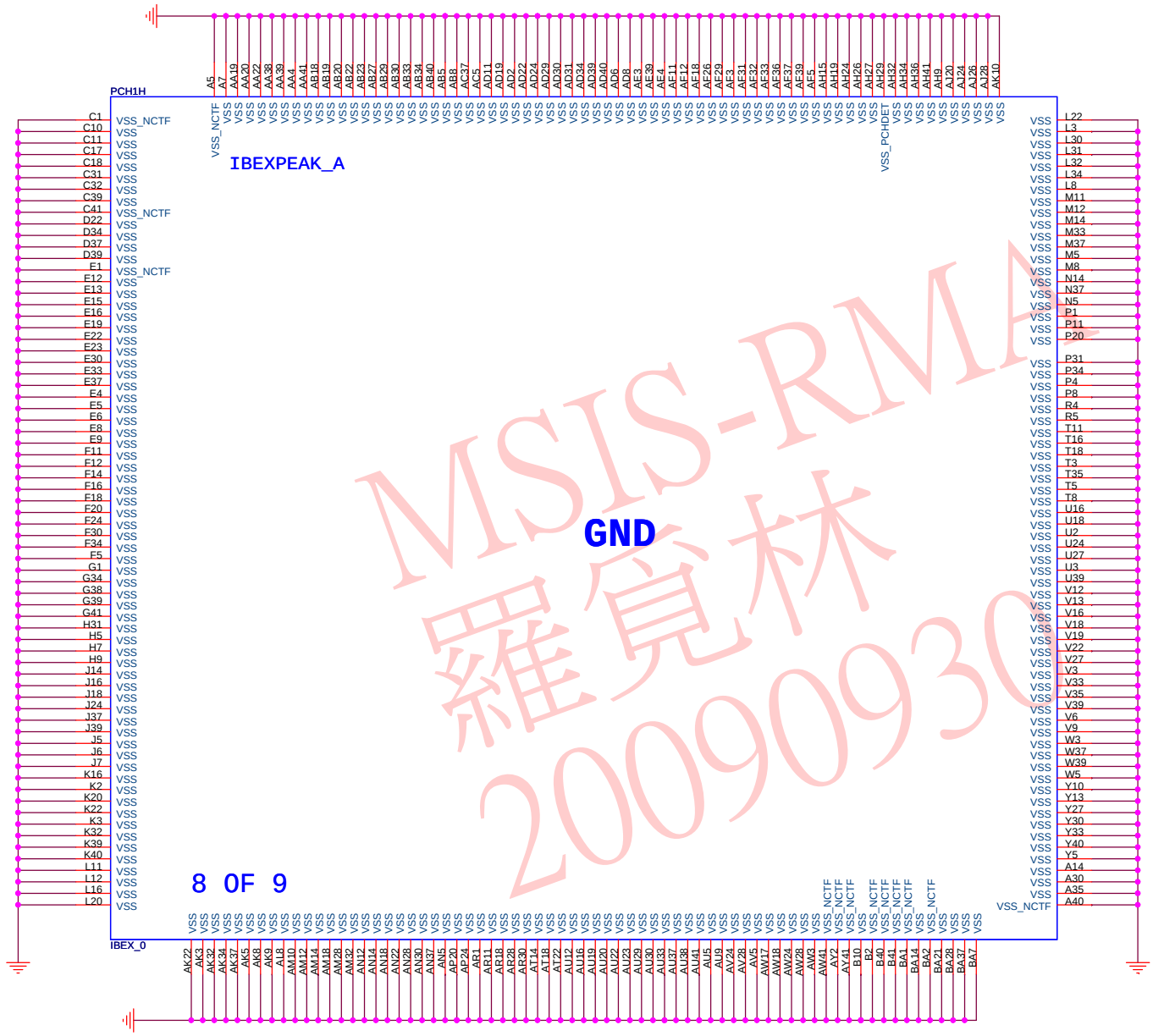

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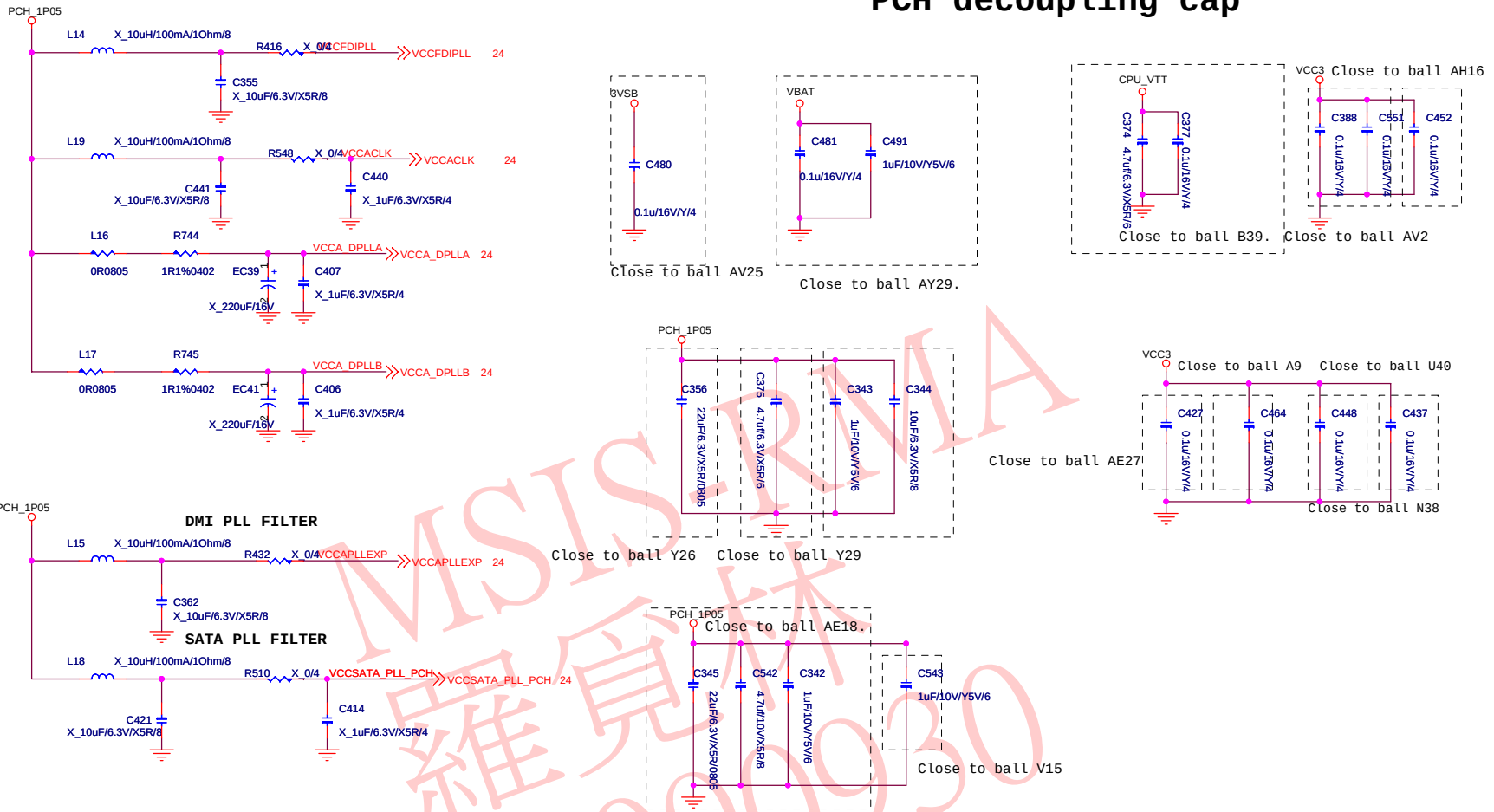
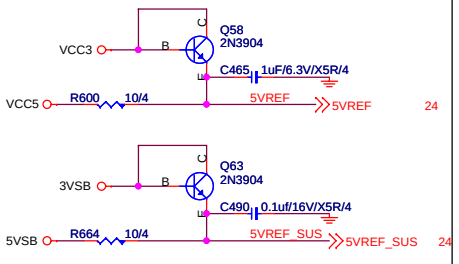
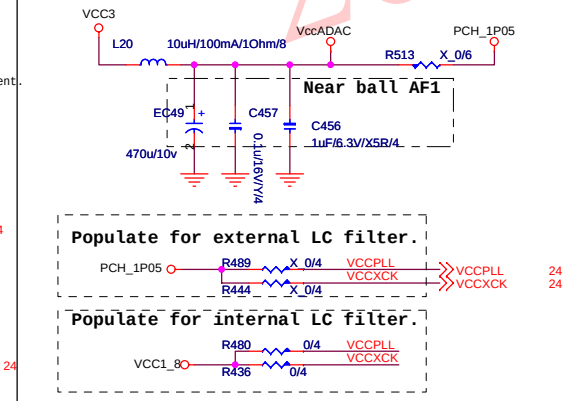
PCH decoupling cap



5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.





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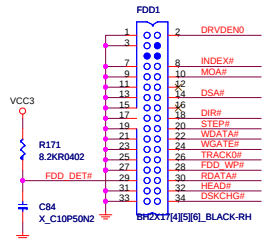
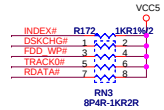
FLOPPY CONNECTOR

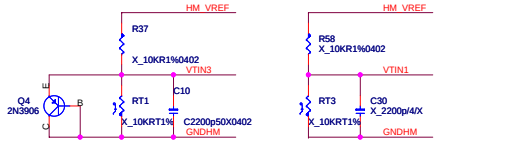




Parameter	Typ	Unit
Main Supply Average Current	5	mA
Main Supply Standby Current	2.5	mA
Standby Supply Average Current	1.0	mA
Battery Supply Current	0.24	uA

	Status		Result
R414	stuff	doesn't stuff	if there is no CPU on the socket, the system couldn't be powered on
R416	doesn't stuff	stuff	it could prevent the system from powering on when the power cable is plugged into the power supply

Thermal Resistor



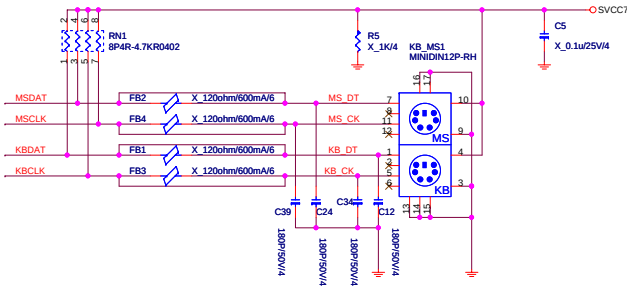
RT5 must be under the CPU socket

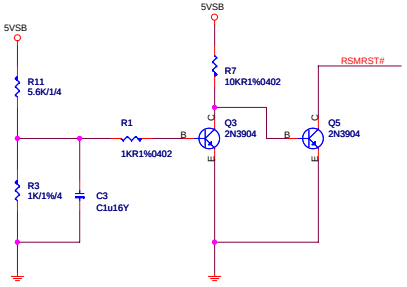
LPC I/O STRAPPING RESISTOR

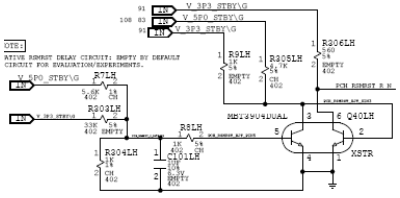
S I/O STRAP

DTRB# 1:BACKUP* 0:PRIMARY
SOUTB 1:DIS 0:EN*
SOUTA 1:4EN* 0:2En
DTRA# 1:60% 0:100%*
RTSA# 1:VIDO/VIDI* 0:GPIO/VIDIO
RTSB# 1:PWM FAN* 0:LNR FAN

PS2 KEYBOARD & MOUSE CONNECTOR







•BJT clamp forces RSMRST# assertion when 5VSTBY falls to ~4.5V. Circuit does not monitor VccSUS directly, but will trip RSMRST# before VccSUS drops below ~2.9V.

	MICRO-STAR INT'L CO.,LTD	
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Size: C	Document Description: IO-Fintek F71889	Rev: V10
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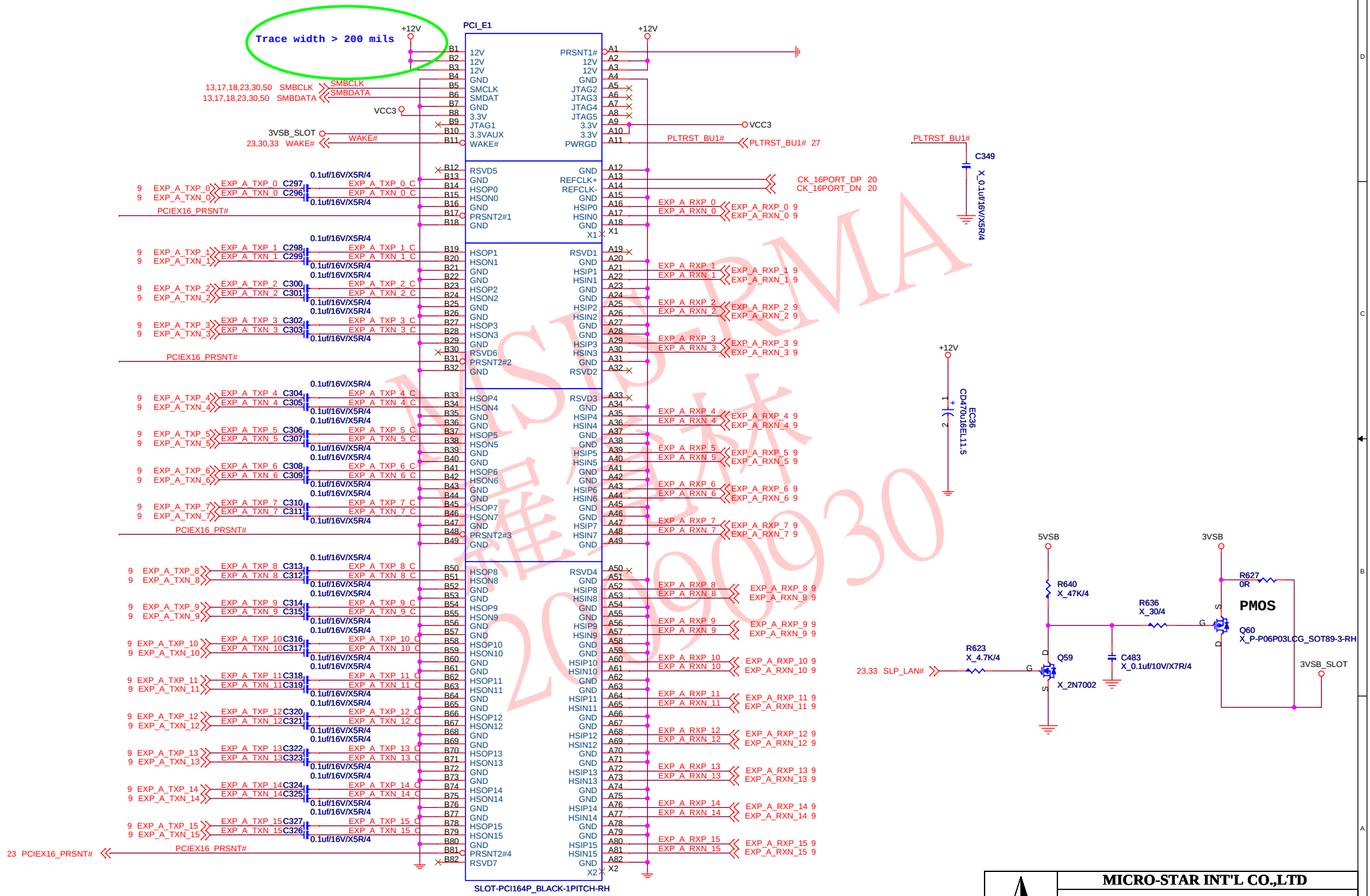
PCI_Express X16 Slot (Revise History)



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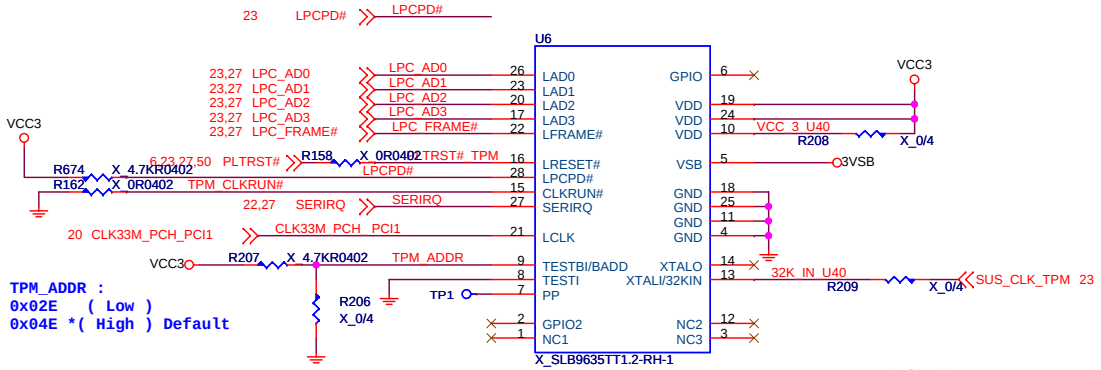
TPM 1.2

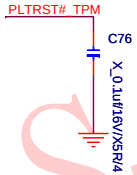
PN:B0C-0963532-IX4

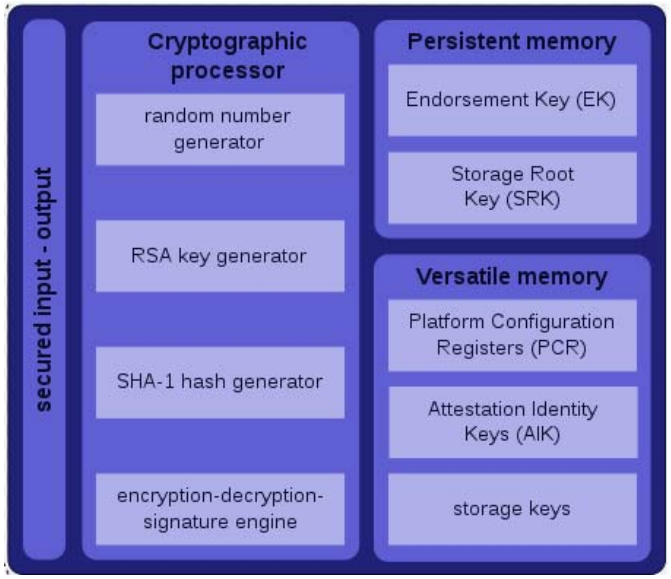


1.17 PP Pin

This pin should be connected to a jumper. The standard position of the jumper should connect the pin to GND. If the pin is connected to VDD, some special commands are enabled (for instance, the Force_Clear command, also refer to [6]).

If the physical presence feature is not used on the platform, the pin can be left unconnected (it has an internal pull-down).





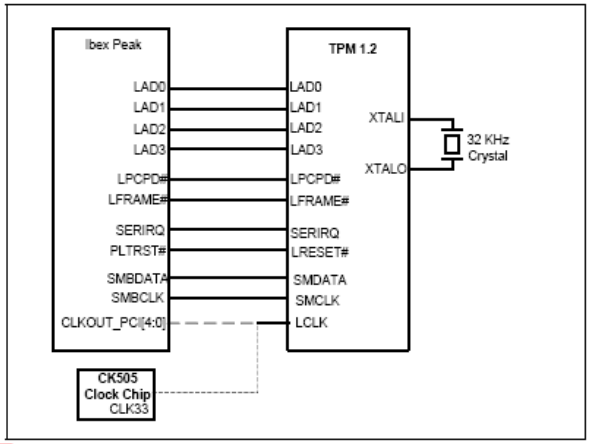
Trusted Platform Module (TPM) Overview

Trusted Platform Module(s) (TPM) are a Trusted Computing Group (TCG) low cost security solution to increase confidence on system security. The TPM is a device that resides on the motherboard and is connected to Ibex Peak using the Low Pin Count (LPC) bus to communicate with the rest of the platform.

Today most protection against computer viruses and unauthorized intrusions consists of adding and updating software that installs outer barriers and surveillance tools. The goal of Safer Computing is to go much deeper, integrating a level of trust into the actual hardware and pre-operating system environments. Applications intended for e-business are based on trust in the communication partner and the reliability of the connection.

The objective of the TPM is to establish a baseline of platform integrity and enhance system security. TPMs are available from several integrated circuit vendors in the form of a silicon component and accompanying software. When integrated into the PC, a TPM provides protected storage of platform data allowing for platform-level authentication toward the goal of making data files, transactions and communication more trustworthy.

TPM 1.2 / Intel® Ibex Peak Block Diagram



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	MS-7619-V10-20090819-B	
Size B	Document Description TPM	Rev V10
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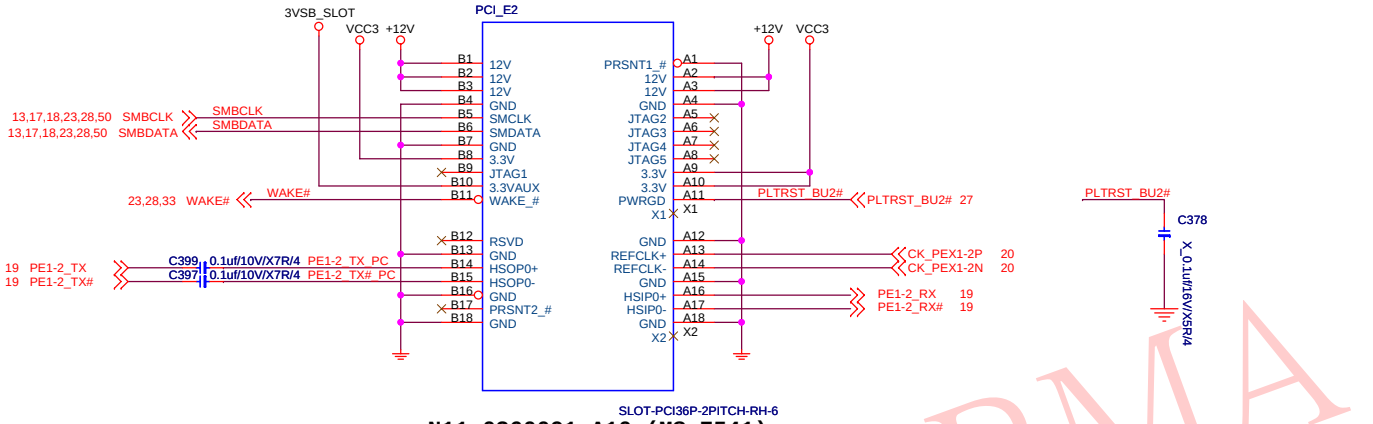
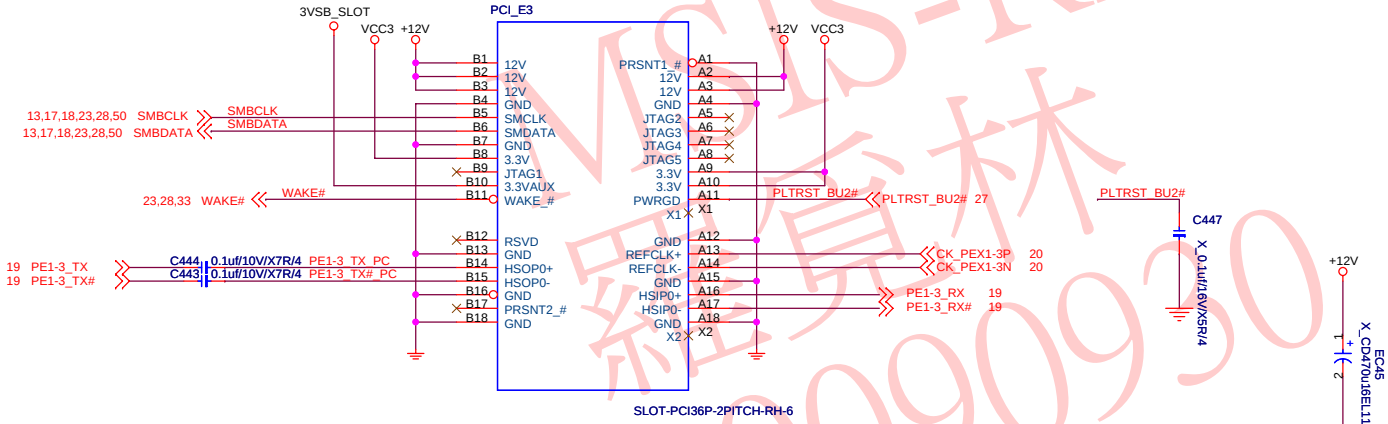
PCI EXPRESS x1-PORT1



N11-0360091-A10 (MS-7541)

PCI EXPRESS x1-PORT2



N11-0360091-A10 (MS-7541)

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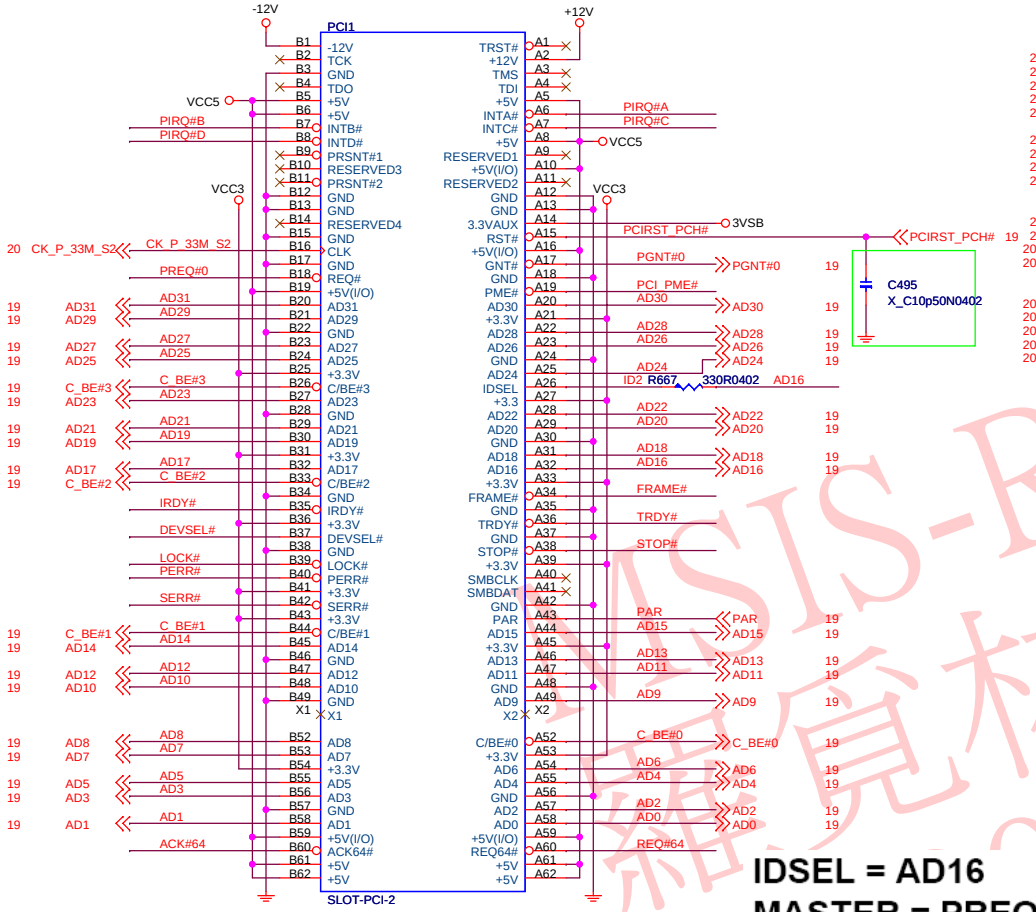
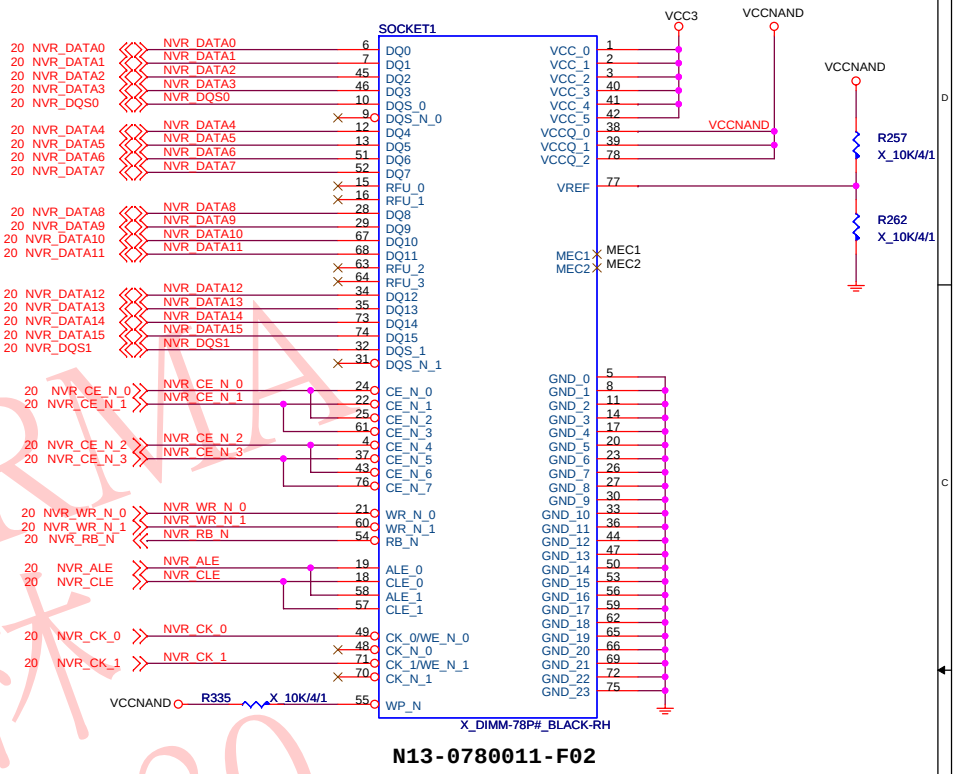
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

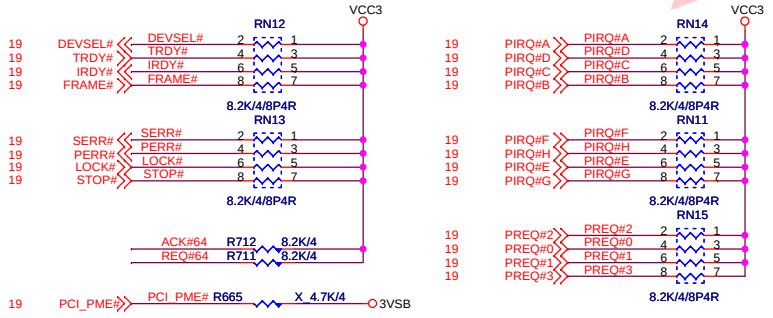


N11-1200171-F02 (MS-7541)

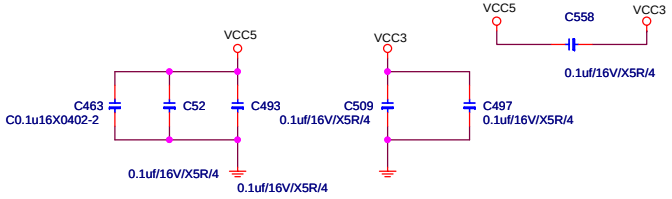


N13-0780011-F02

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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LVR Power and Control Pins

Pin Name	Pin #	Type	Name and Function
CTRL1P2	7	Analog	Connect to the base of the PNP.
VCT	6	Analog	Regulator output; connect to 1.8 V dc supply and a center tap, 1 µF capacitor.

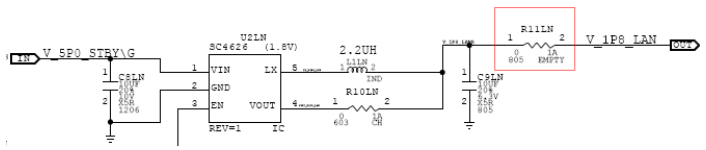
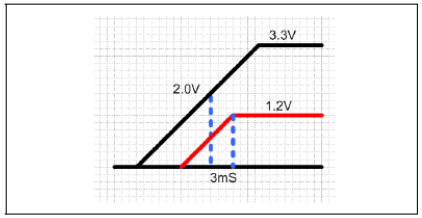


Figure 16-20.82578 Power Sequencing

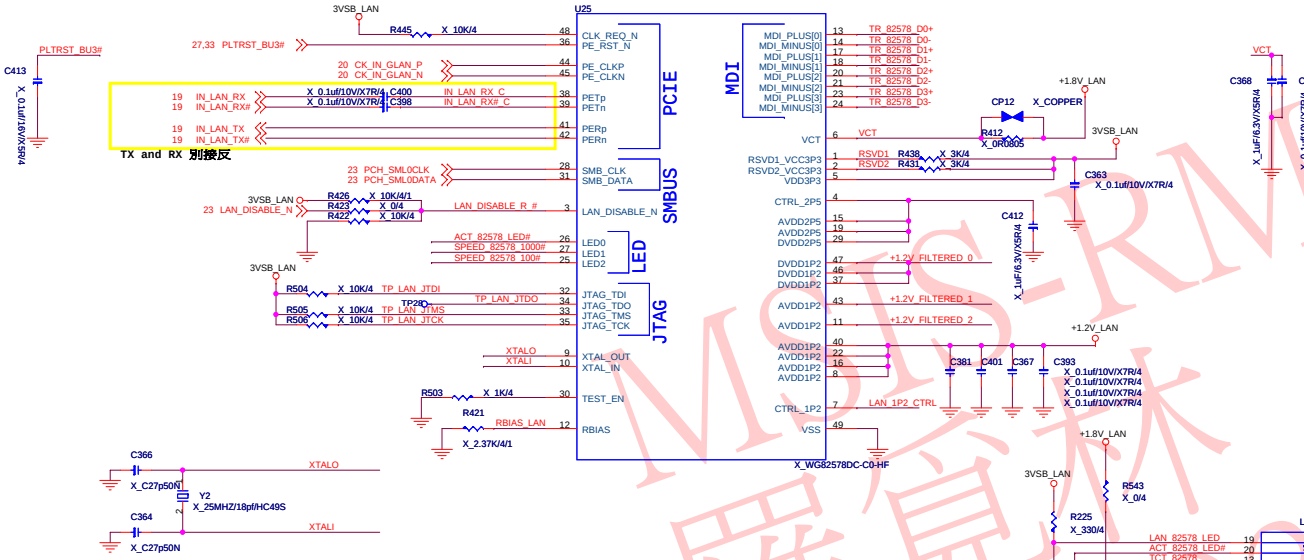


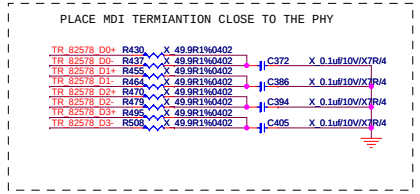
- Power up sequence: 3.3 V dc then 1.2 V dc.
- A minimum 3 ms delay is required from the time 3.3 V dc reaches 2.0 volts to 1.2 V dc reaching a steady state.
- Power down sequence 1.2 V dc then 3.3 V dc.

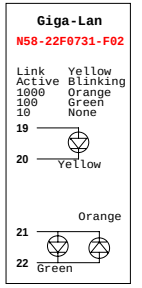
HANKSVILLE

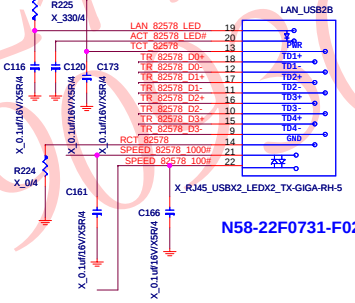
Device	Market Segment	Product Code
82577LM	Corporate mobile and workstation	WG82577LM
82577LC	Consumer mobile	WG82577LC
82578DM	Corporate desktop and workstation	WG82578DM
82578DC	Consumer desktop	WG82578DC

Method of enabling/disabling features in SKUs					Performance				Extended										
					Driver	Driver	MAC	PHY	Driver	PHY	Driver	Driver	Platform	Platform	BIOS	BIOS	Platform	FW
Link Speed	Platform	Segment	Description	Device ID	Jumbo Frames (up to 9k)	802.1Q & 802.1p	Receive Side Scaling (RSS) 2 Tx & 2 Rx Queues	Low Power Link Up (ALPLU)	Link Speed Battery Saver	Low Power Link up (LPLU)	Ability to Initiate a Team	Intel® Virtualization	Viiv (Home IT/ Convin Springs)	Link sec Hardware Ready	Intel® iSPP	PXE Boot	iSCSI Boot	Intel® iProt®
Gigabit	Mobile (Calpella)	Corporate	82577 for Corporate	10EA	X	X	X	X	X	X	X	X	X	X	X	X		X
		Consumer	82577 for Consumer	10EB		X			X	X	X		X			X		
Gigabit	Desktop (Piketon) Desktop (Kings Creek)	Corporate	82578 for Corporate	10EF	X	X	X	X	X		X	X	X	X	X	X	X	X
		Consumer	82578 for Consumer	10F0		X			X		X	X		X		X		







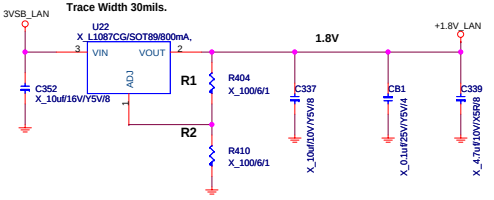


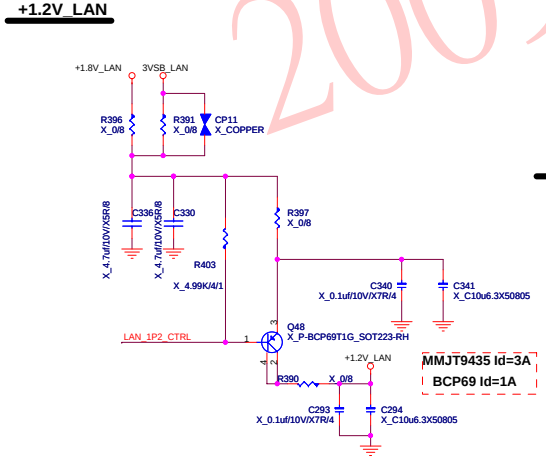
Maximum Trace Lengths Based on Trace Geometry and Board Stackup[1]

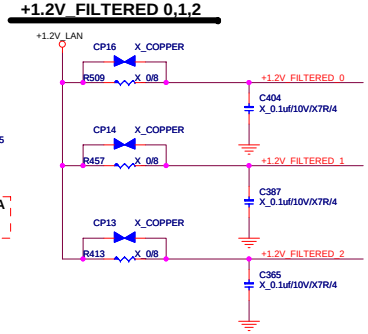
Dielectric Thickness (mils)	Dielectric Constant (DK) at 1 MHz	Width / Space/ Width (mils)	Pair-to-Pair Space (mils)	Nominal Impedance (Ohms)	Impedance Tolerance (+/-%)	Maximum Trace Length (inches)[1]
2.7	4.05	4/10/4	19	95[2]	17[2]	3.5
2.7	4.05	4/10/4	19	95[2]	15[2]	4
2.7	4.05	4/10/4	19	95	10	5
3.3	4.1	4.2/9/4.2	23	100[2]	17[2]	4
3.3	4.1	4.2/9/4.2	23	100	15	4.6
3.3	4.1	4.2/9/4.2	23	100	10	6
4	4.2	5/9/5	28	100[2]	17[2]	4.5
4	4.2	5/9/5	28	100	15	5.3
4	4.2	5/9/5	28	100	10	7

Notes:

1. Longer MDI trace lengths may be achievable, but may make it more difficult to achieve IEEE conformance. Simulations have shown deviations are possible if traces are kept short. Longer traces are possible; use cost considerations and stackup tolerance for differential pairs to determine length requirements.
2. Deviations from 100 Ω nominal and/or tolerances greater than 15% decrease the maximum length for IEEE conformance.







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Size C	Document Description 1394 Controller - VT6315N-CD		Rev V10
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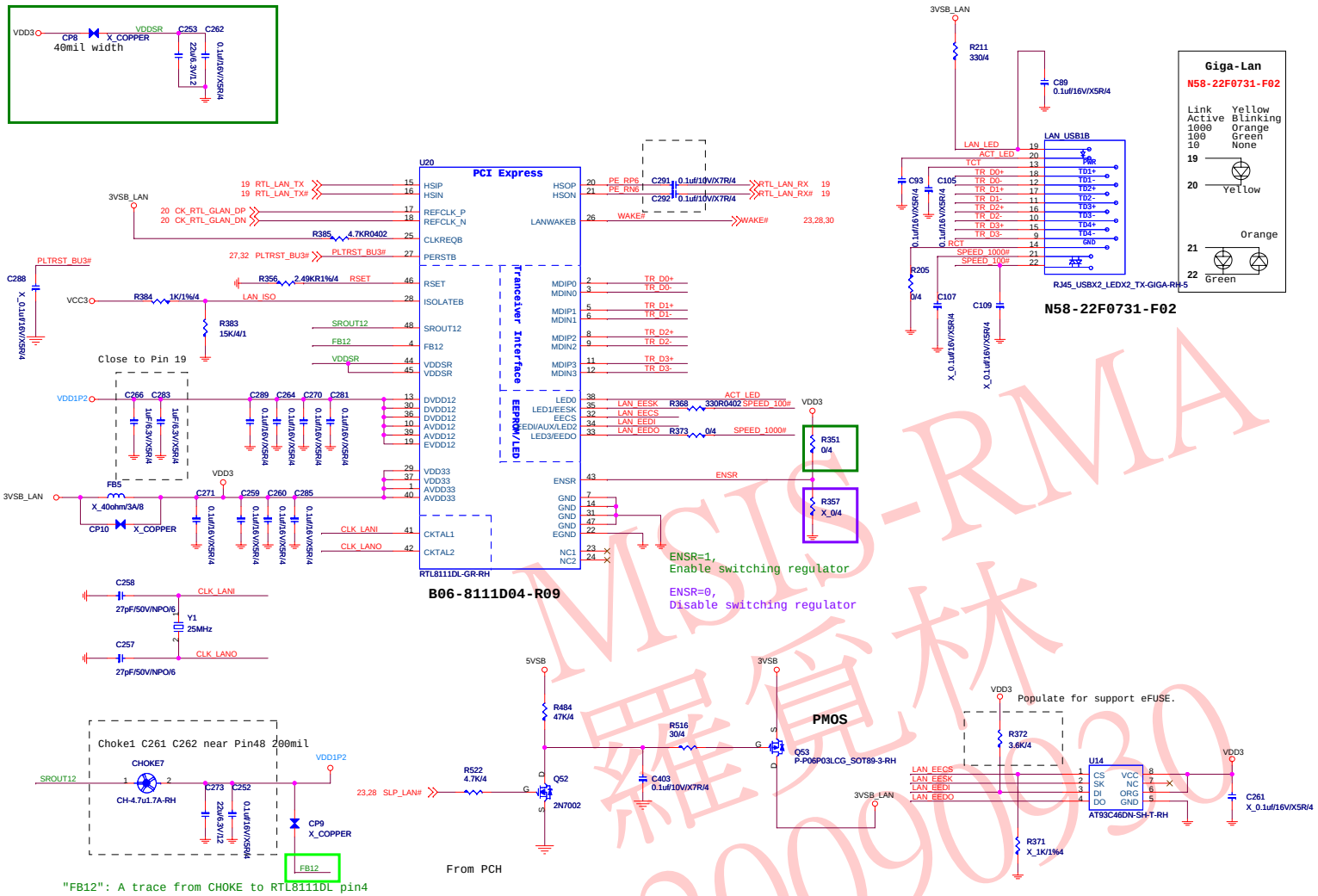

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33, AVDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
DVDD12, AVDD12	1.2V Supply Voltage	-	1.0	1.05	1.09	V
EVDD12	1.2V Supply Voltage	-	1.0	1.05	1.09	V
I_{in}	Input Current	Vin = VDD33 or GND	0	-	0.5	μA
Icc33	Average Operating Supply Current from 3.3V	At 1Gbps with heavy network traffic	-	58	-	mA
Icc12	Average Operating Supply Current from 1.2V	At 1Gbps with heavy network traffic	-	289	-	mA

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ ACT
LED1	LINK100	LINK10/ 100/1000	LINK	LINK100/ ACT
LED2	LINK10	LINK10/ 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 /ACT

EEPROM RTL8168D.cfg
CONFIG1裡面的值.預設是CF 一共對應四種模式
00 mode 填入 0F
01 mode 填入 4F
10 mode 填入 8F
11 mode 填入 CF

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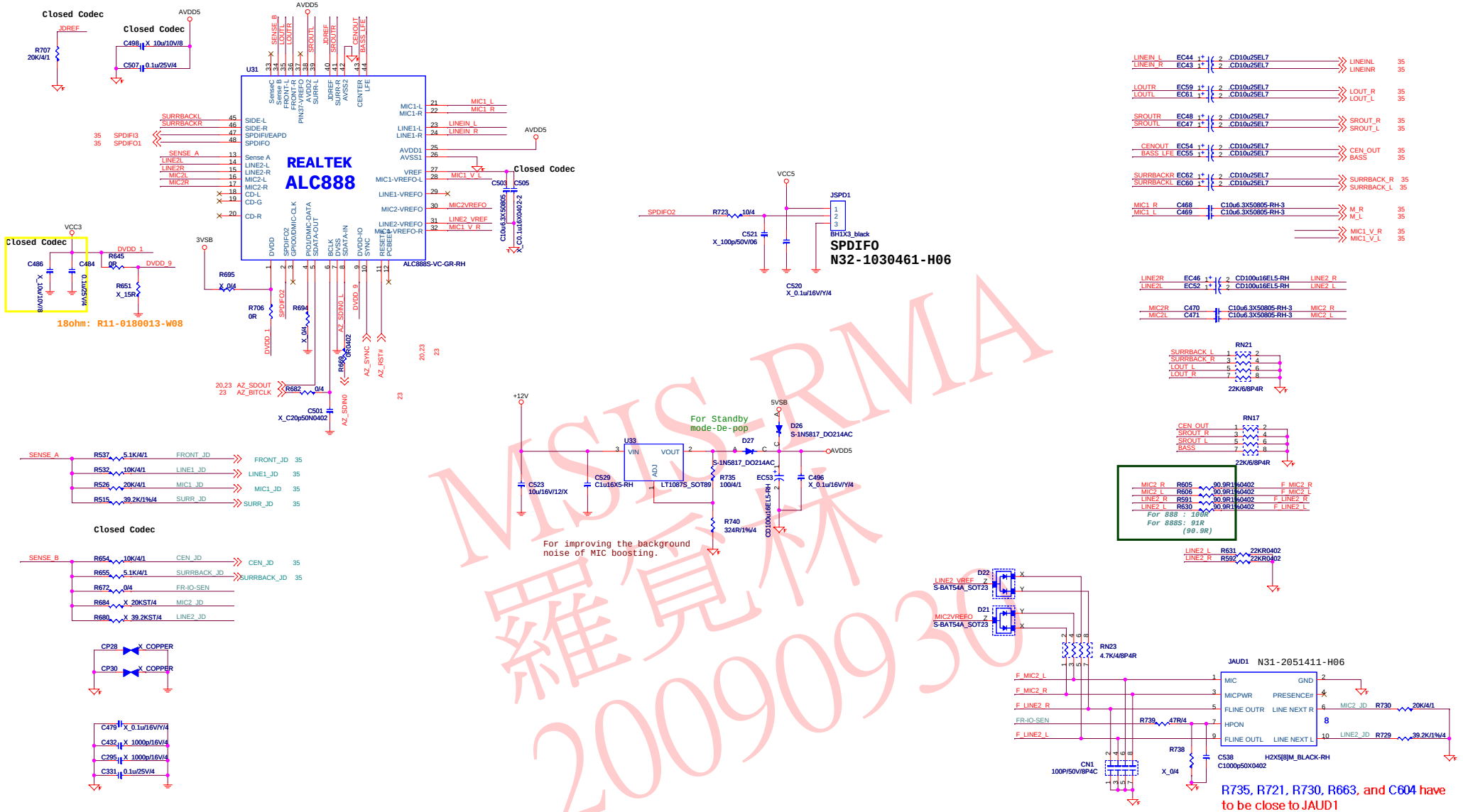

MICRO-STAR INT'L CO.,LTD	
MS-7619-V10-20090819-B	
Size: C	Document Description: Audio Codec ALC888S-VC2
Rev: V10	
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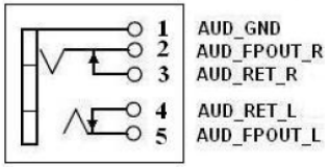
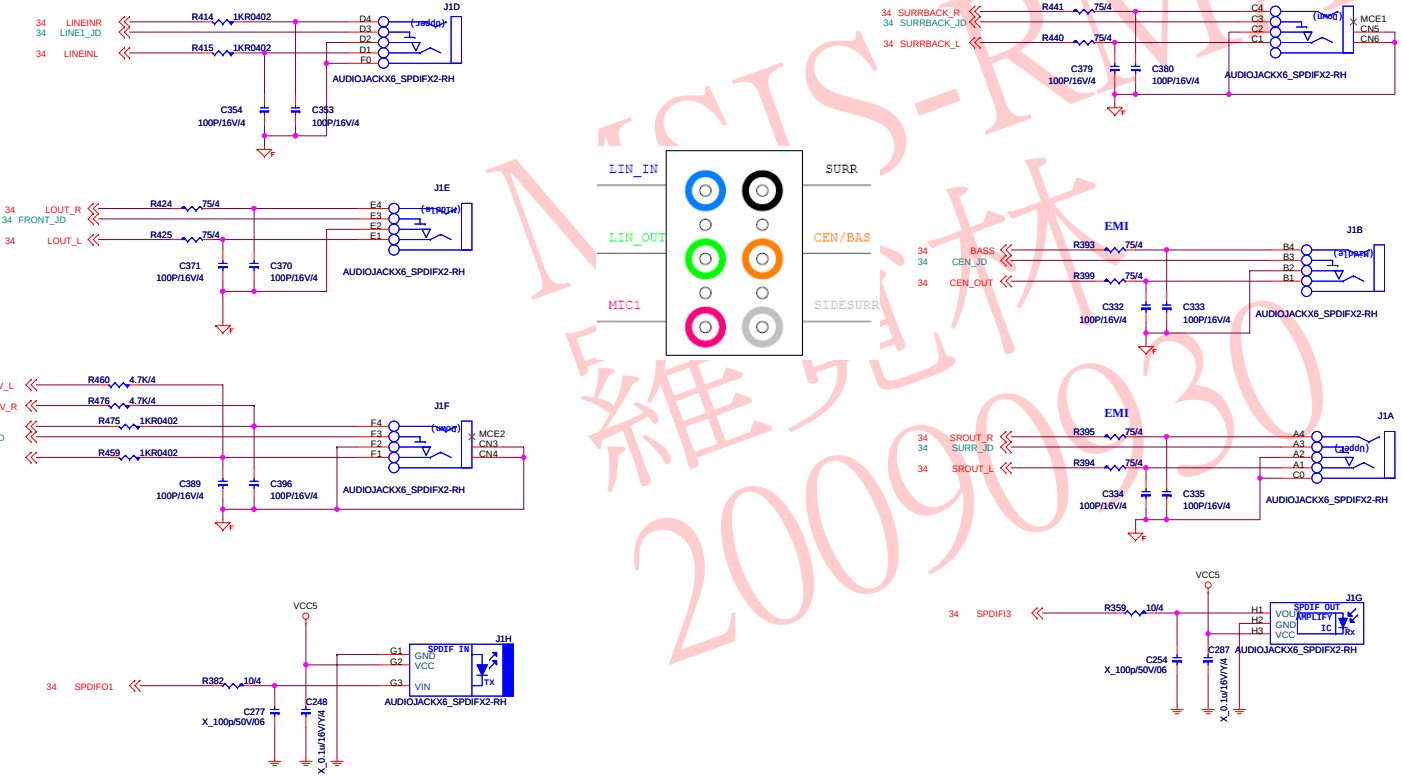


Line out the main function is to let the walkman connect to the external loudspeaker system. The main difference with Phone out are that Line out doesn't pass through the amplifying circuit, therefore the acoustic quality of the external loudspeaker system (must be power-supplied) is better than the one of Phone out. If there is the small loudspeaker without external power, it have to connect to Phone out.

N58-32F0011-S42 (MS-7541)



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7619-V10-20090819-B	
Size C	Document Description: AUDIO JACK	Rev V10
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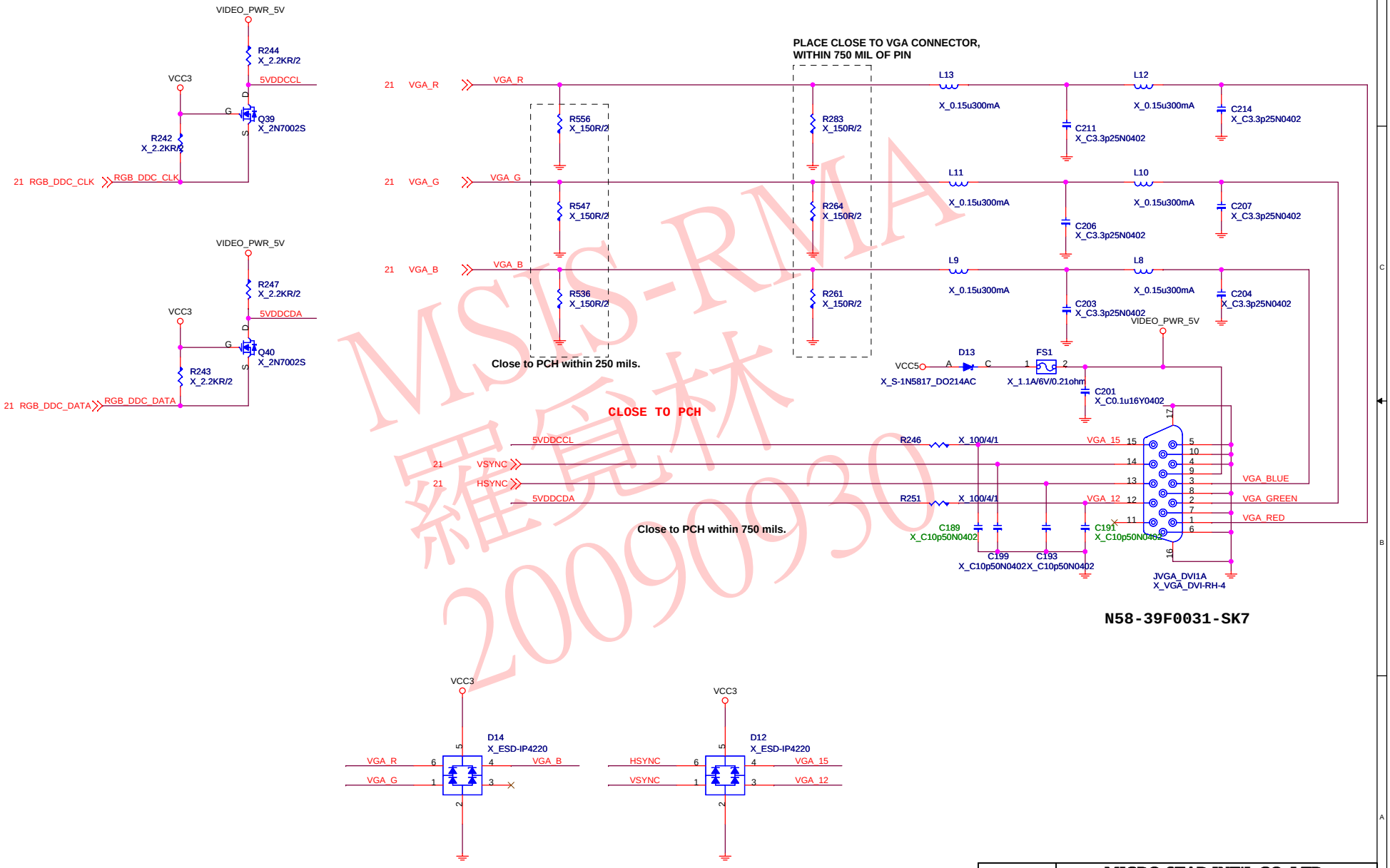
Video Connector



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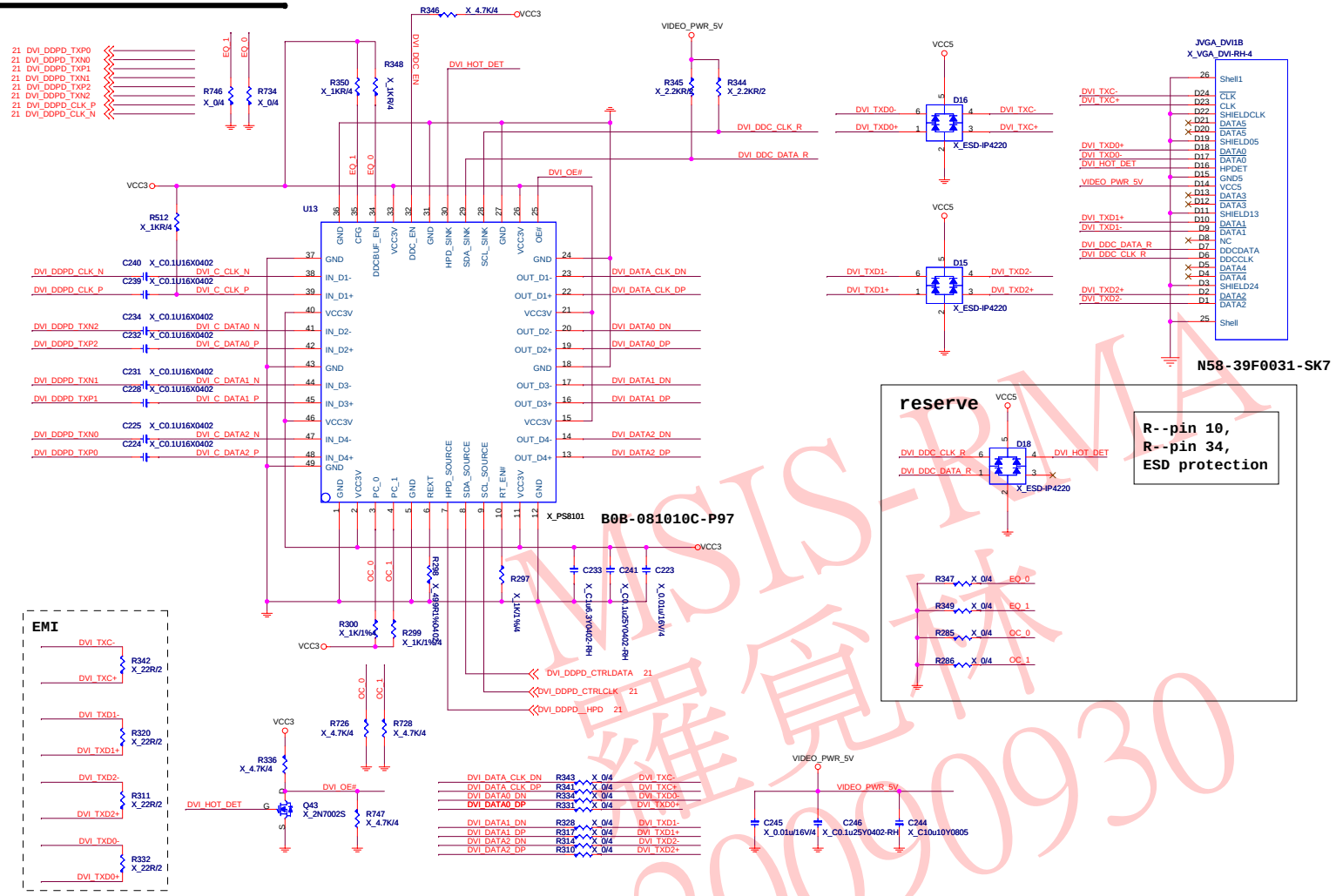
DVI level shifter



Parameter	Min	Typ	Max	Unit
Supply Voltage, VCC	3.0	3.3	3.6	V
Ambient Temperature	0		70	°C
Supply Current, Icc[1]		110	132	mA
Power Consumption[2]		422	528	mW
Power down current [3]		10	50	uA

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Size: C	Document Description: DVI transfer	Rev: V10
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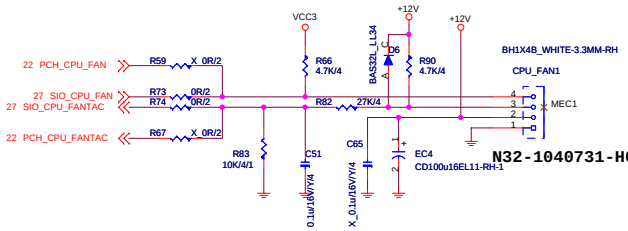
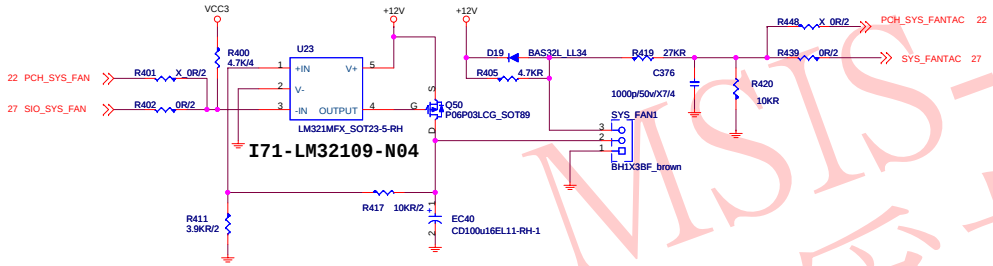
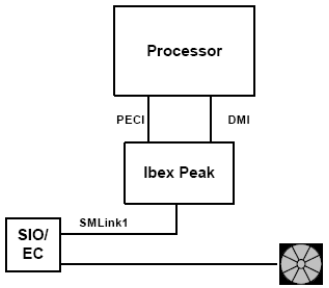
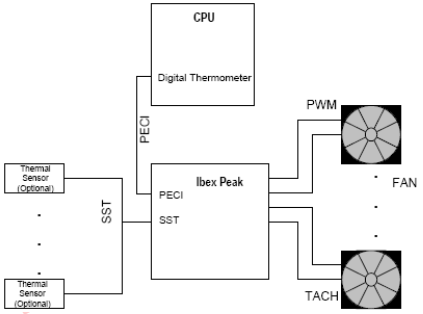
FAN-COUNTROL CIRCUIT







R363, R368, R419, R420, R504, R505 must stuff



R382, R213, R483, R492, R502, R506 must stuff
R660, R671 don't stuff

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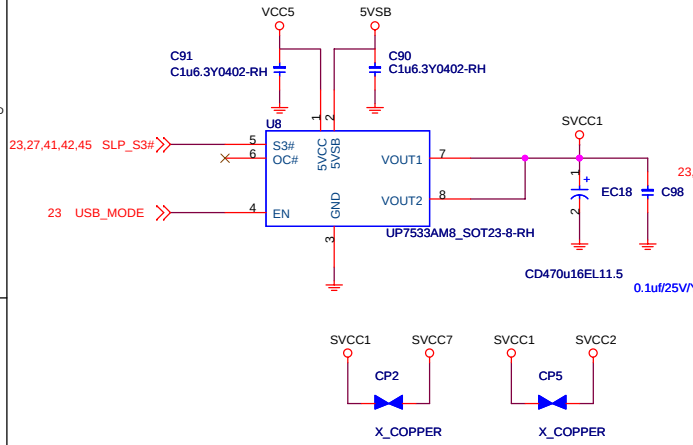
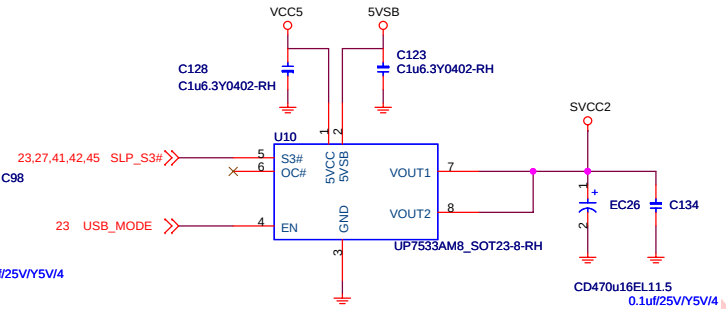
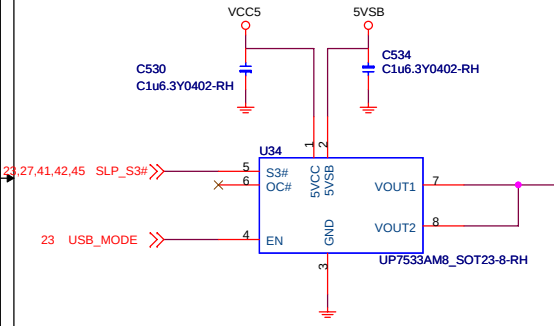
POWER CIRCUIT FOR USB PORT 10, 11



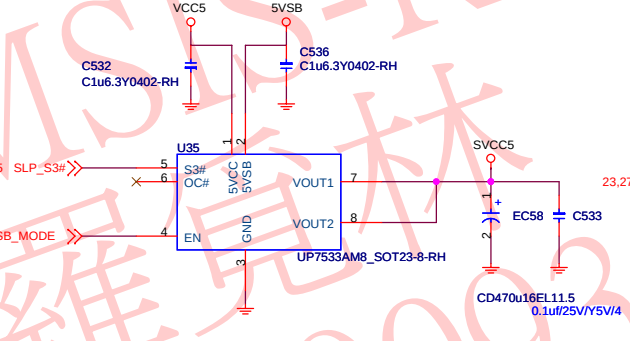
POWER CIRCUIT FOR USB PORT 4, 5

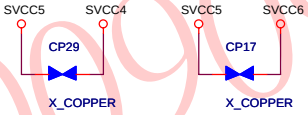


POWER CIRCUIT FOR USB PORT 2, 3

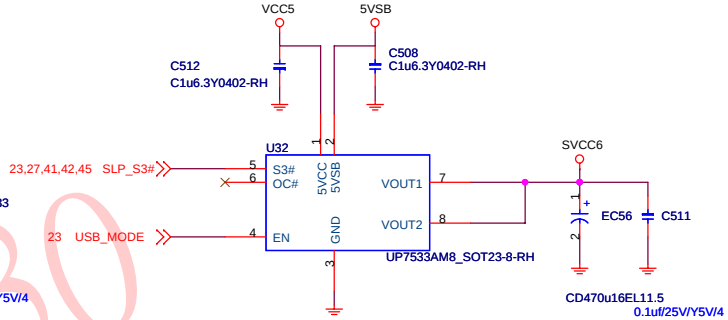


POWER CIRCUIT FOR USB PORT 6, 7

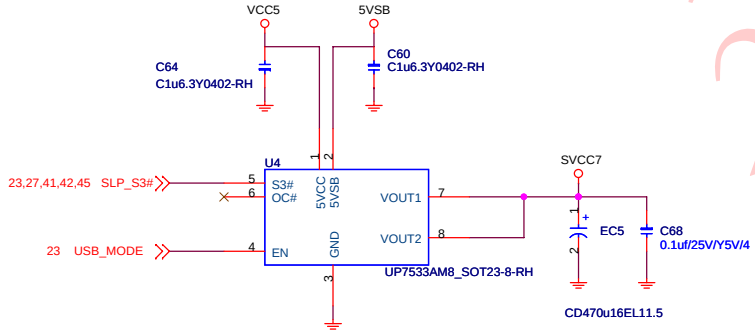




POWER CIRCUIT FOR USB PORT 8, 9



POWER CIRCUIT FOR USB PORT 0, 1



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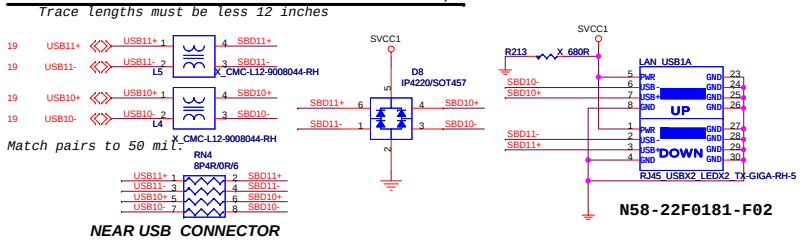
REAR PANEL USB CONNECTOR FOR USB PORT 10,11

Trace lengths must be less 12 inches



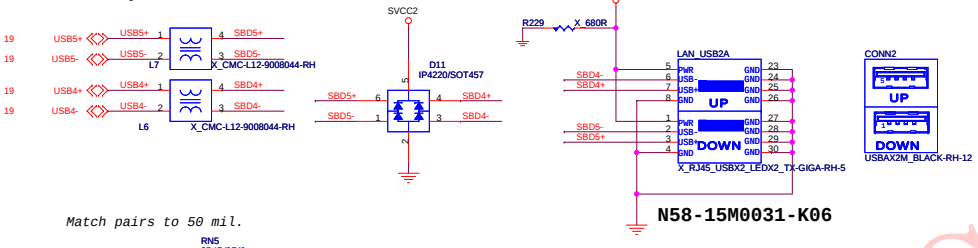
Match pairs to 50 mil.

N58-22F0181-F02

NEAR USB CONNECTOR

REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches



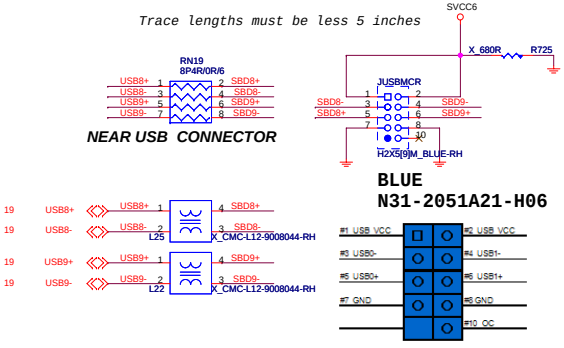
Match pairs to 50 mil.

N58-15M0031-K06

NEAR USB CONNECTOR

FRONT PANEL USB CONNECTOR FOR USB PORT 8, 9

Trace lengths must be less 5 inches

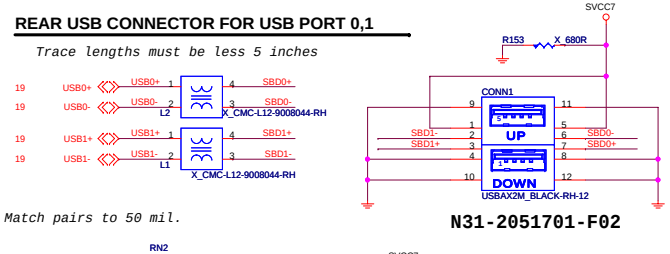


BLUE
N31-2051A21-H06

NEAR USB CONNECTOR

REAR USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 5 inches



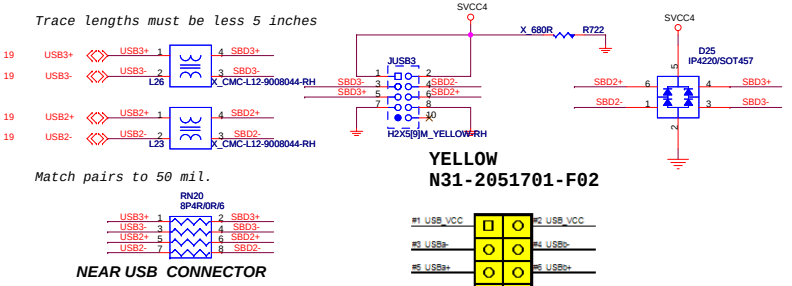
Match pairs to 50 mil.

N31-2051701-F02

NEAR USB CONNECTOR

FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 5 inches



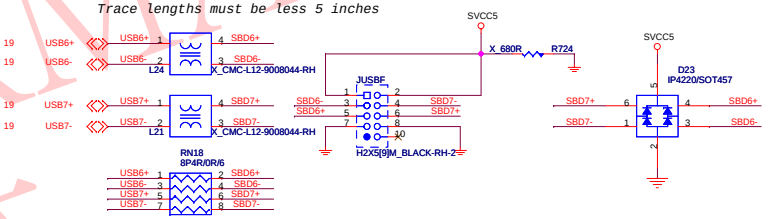
Match pairs to 50 mil.

YELLOW
N31-2051701-F02

NEAR USB CONNECTOR

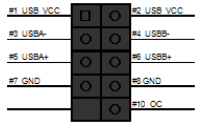
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

BLACK
N31-2051051-H06



USB1 (Yellow, 9P)	USB2 (Yellow, 9P)	USBF (Black, 9P)	USBMCR (Blue, 9P)

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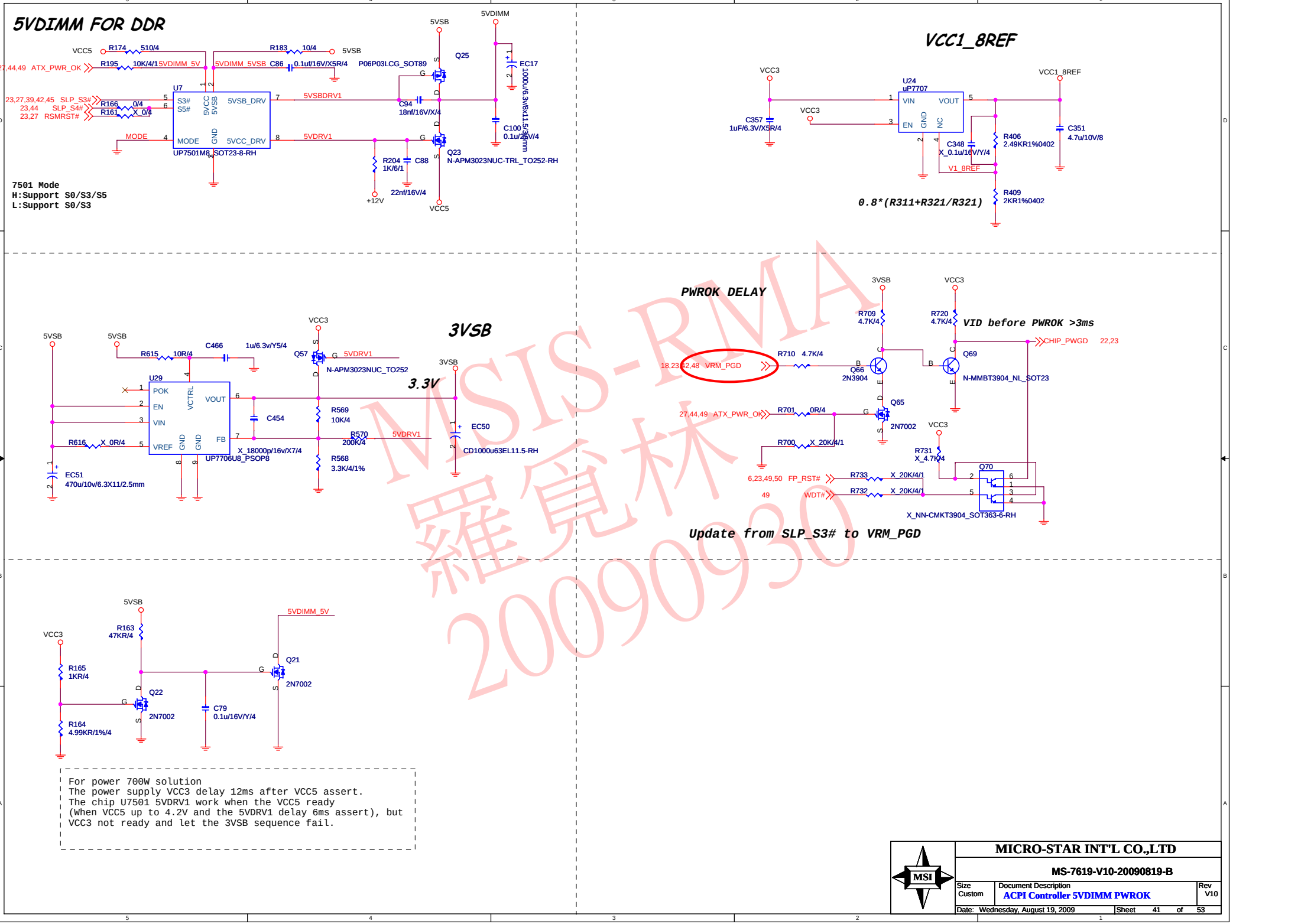
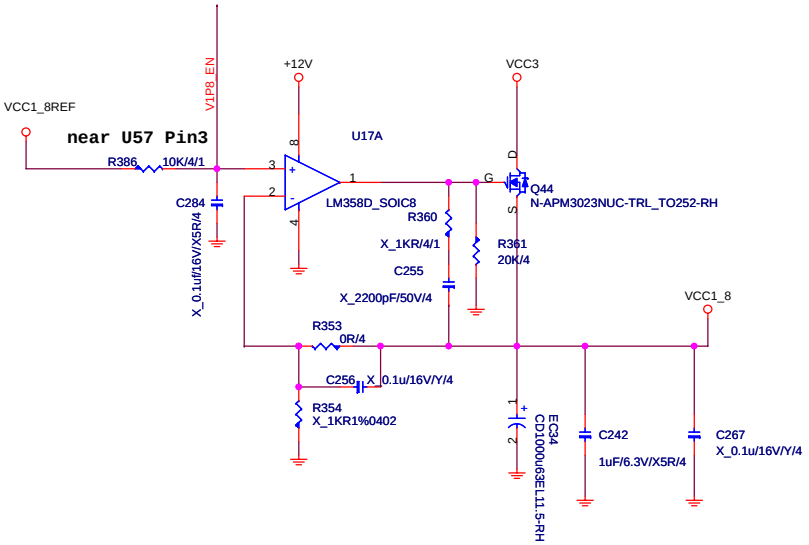
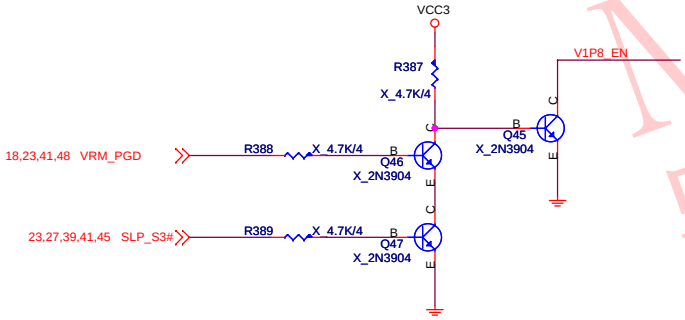
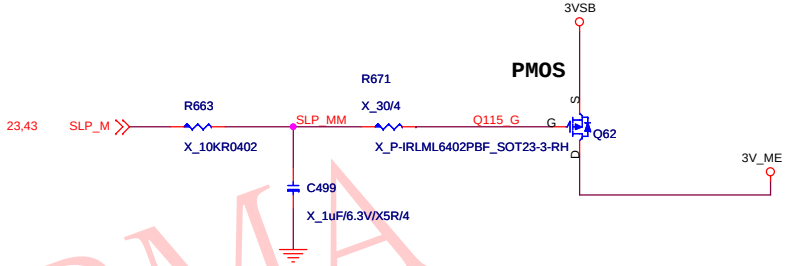


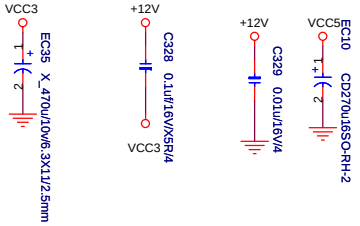


cpuvtt & pch vore wait 1.8v

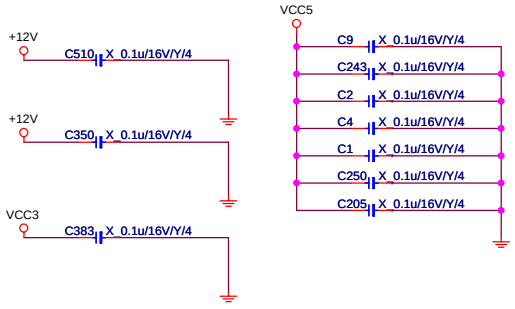


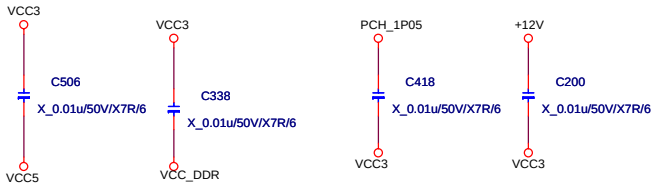
3V_ME





For EMI





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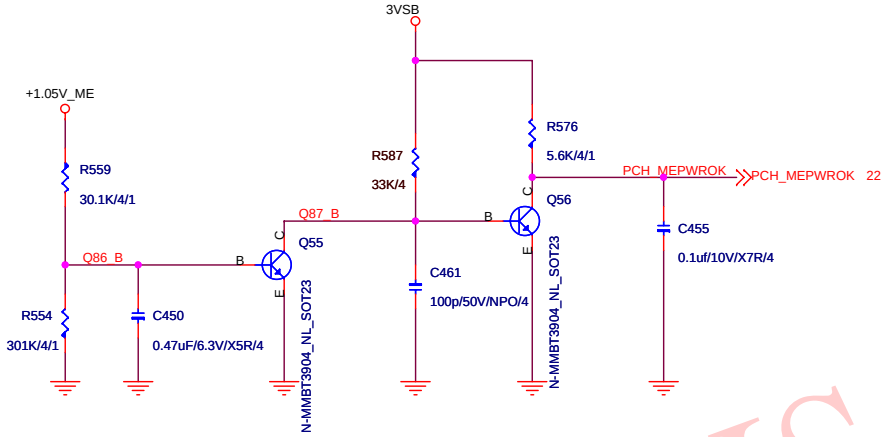
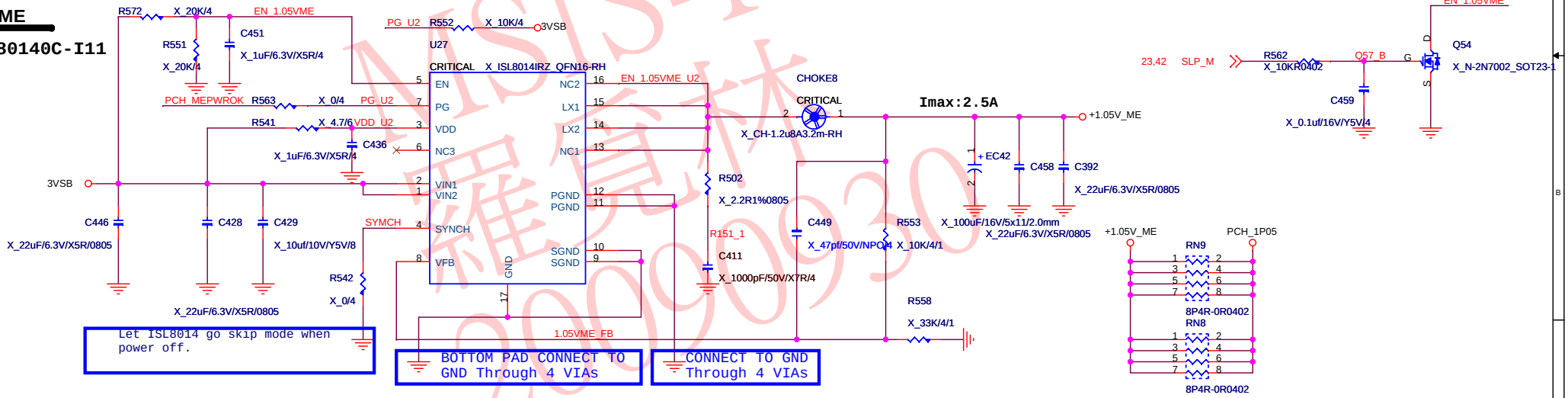
PCH_MEPWROK



+1.05V_ME

PN:I32-080140C-I11



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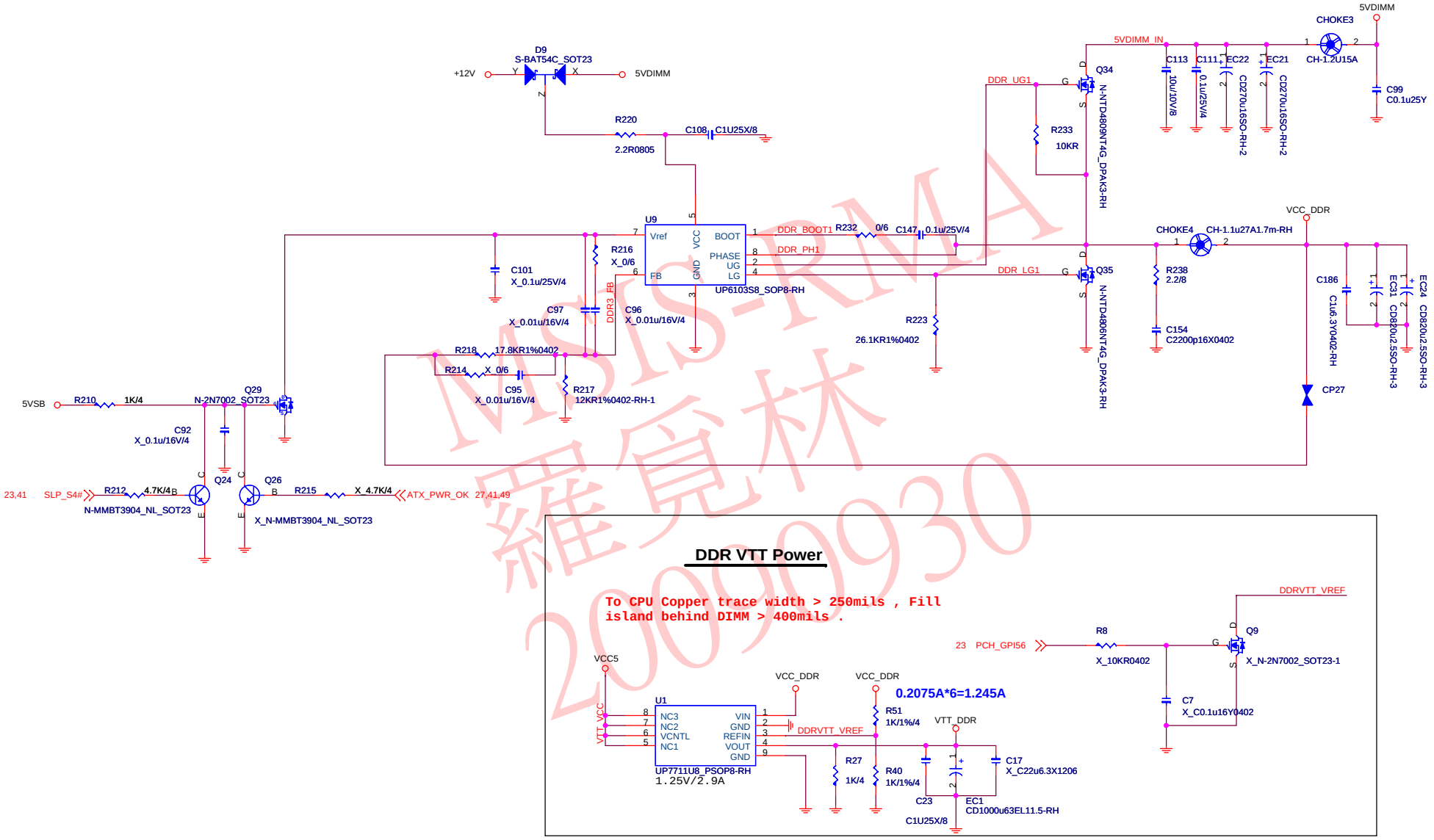
DDR3_1.5V

20A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

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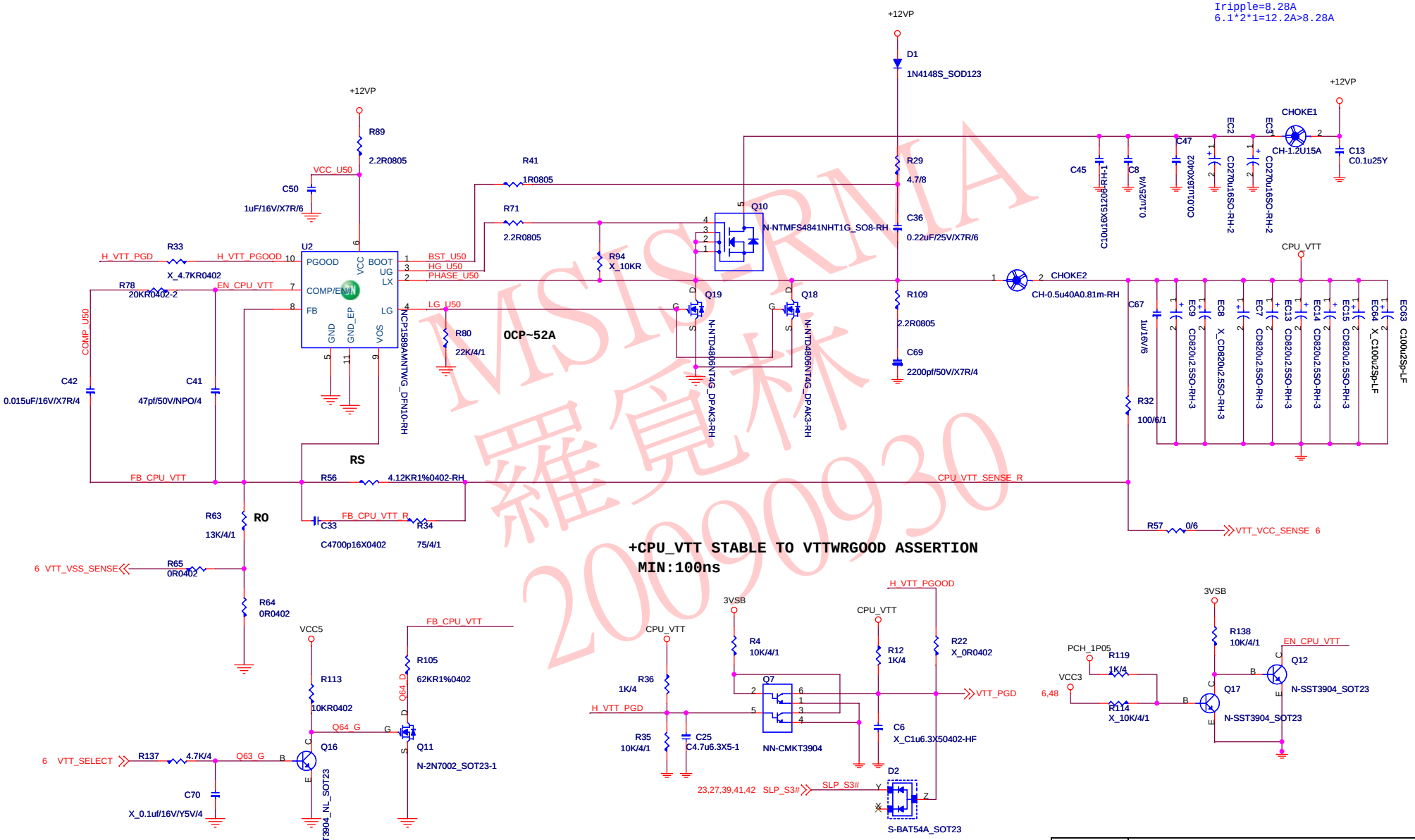
Signal Name	Description	Direction	Type
VTT	Processor power for the memory controller, shared cache and I/O (1.1 V).		PWR

CPU_VTT
30A

Iripple=8.28A
6.1*2*1=12.2A>8.28A



Because the PGOOD signal of U3 turns off too slow to keep energy, it connects to SLP_S3# to let turns off quickly and completely.

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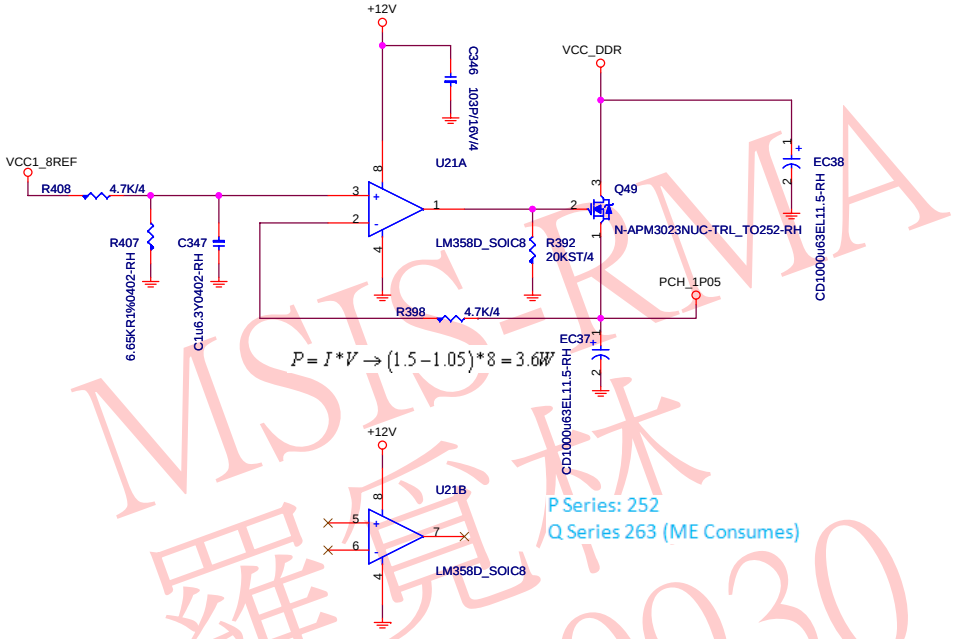
5.5A+2.5A(VCCME)=8A

PCH Core



Ibex Peak Power Supply Range

Power Supply	Minimum	Nominal	Maximum
1.05V	1.00 V	1.05 V	1.10 V
1.5 V	1.43 V	1.50 V	1.58 V
1.8 V	1.71 V	1.80 V	1.89 V
3.3 V	3.14 V	3.30 V	3.47 V
5 V	4.75 V	5.00 V	5.25 V

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=30 A, SMD version	-	7.6	9.5	mΩ
		V_{GS}=10 V, I_D=30 A, SMD version	-	4.9	5.9	

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Size: Custom	Document Description: PCH POWER - UPI6103_1-Phase	Rev: V10
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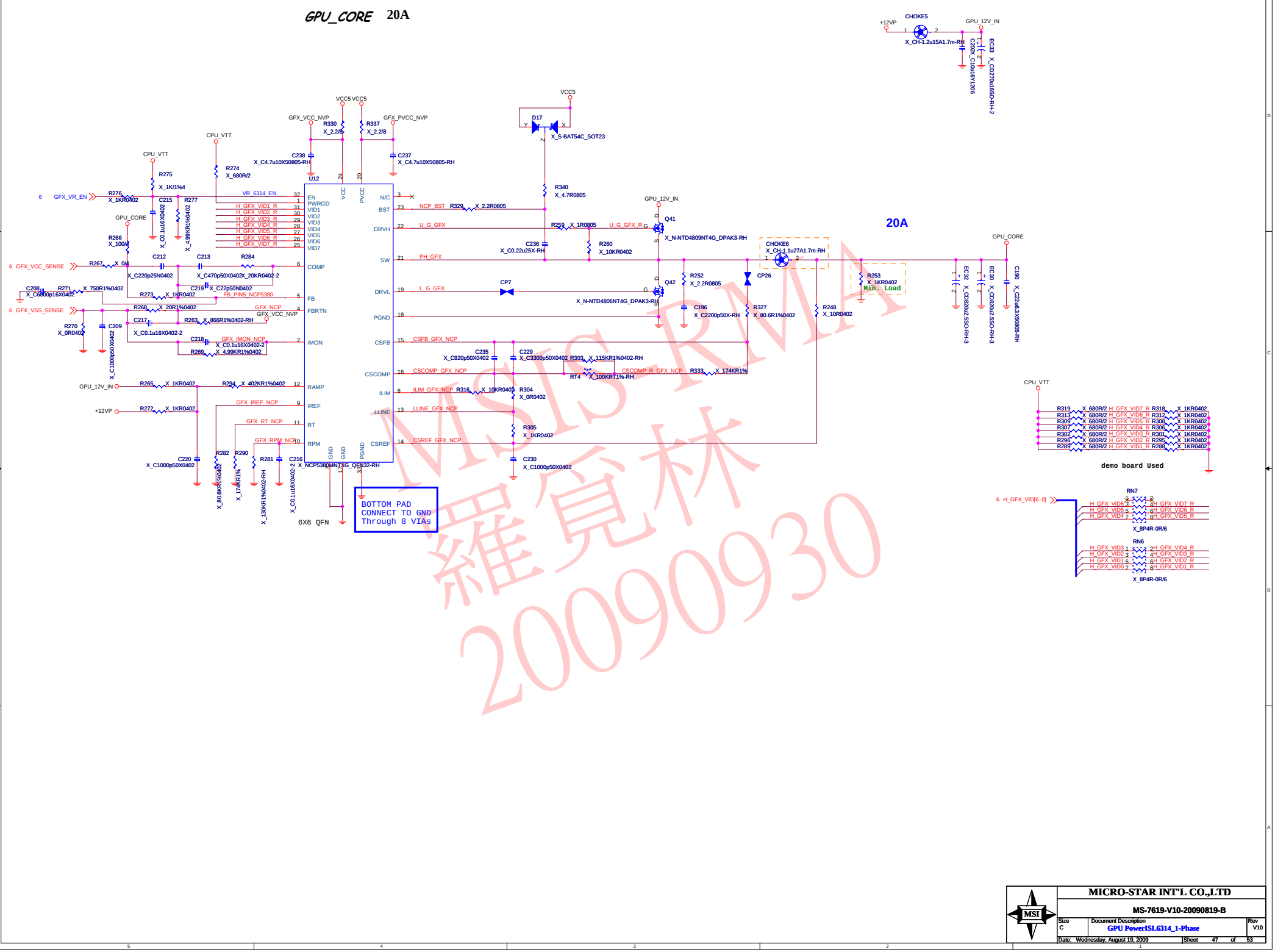

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Size: C	Document Description: GPU Power1SL6314_1-Phase		Rev: V10
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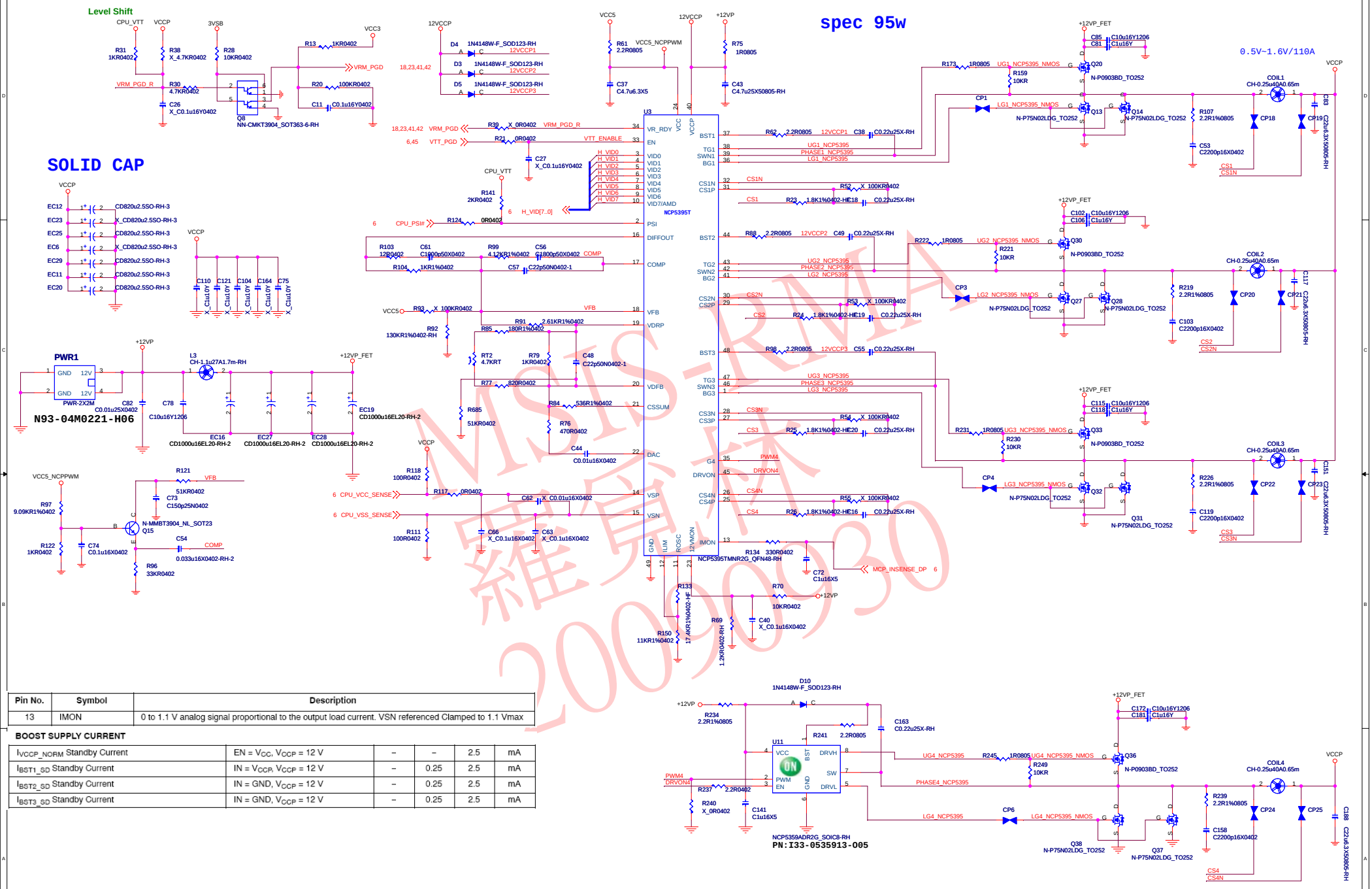
NCP5395 4Phase



Pin No.	Symbol	Description
13	IMON	0 to 1.1 V analog signal proportional to the output load current. VSN referenced Clamped to 1.1 Vmax

BOOST SUPPLY CURRENT

I_{VCCP_NORM} Standby Current	EN = V_{CC}, V_{CCP} = 12 V	–	–	2.5	mA
I_{BST1_SD} Standby Current	IN = V_{CCP}, V_{CCP} = 12 V	–	0.25	2.5	mA
I_{BST2_SD} Standby Current	IN = GND, V_{CCP} = 12 V	–	0.25	2.5	mA
I_{BST3_SD} Standby Current	IN = GND, V_{CCP} = 12 V	–	0.25	2.5	mA

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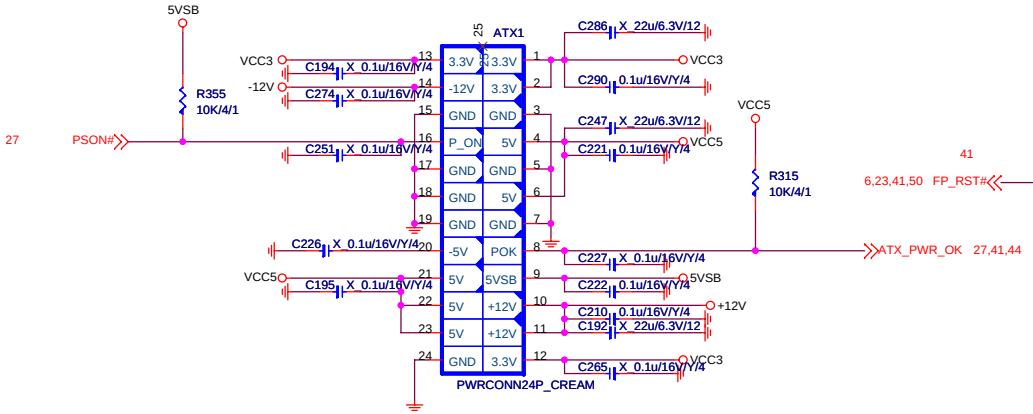
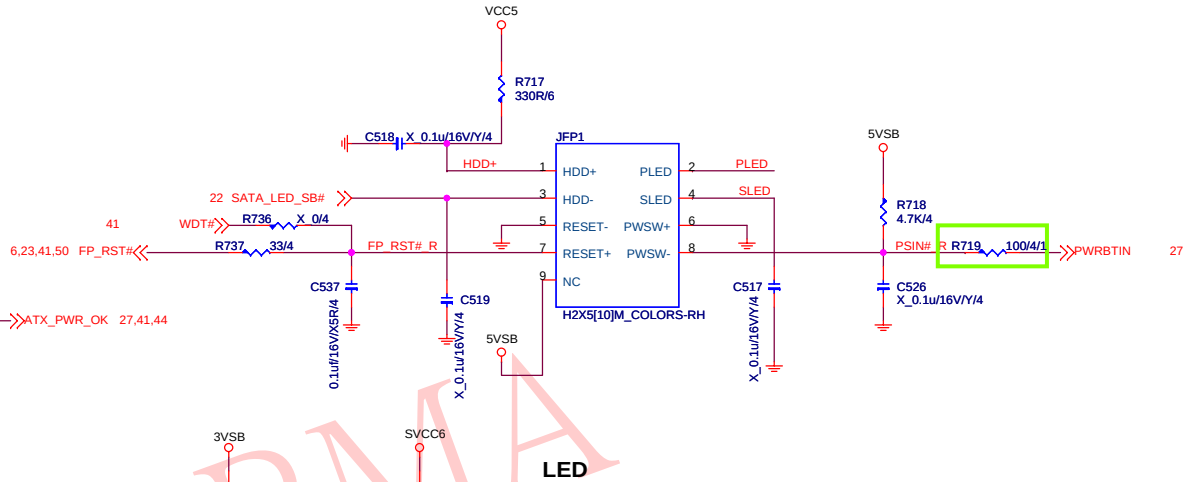
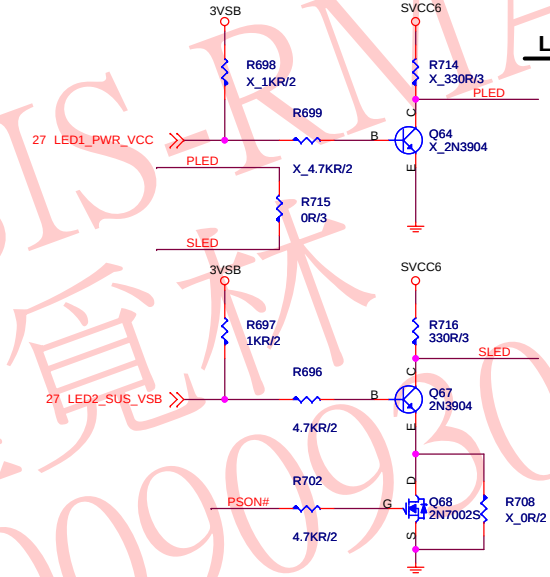
FRONT PANNEL

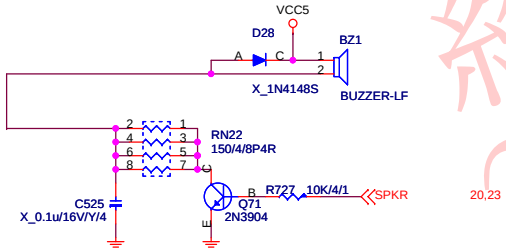
ATX POWER CONNECTOR





LED





	Single color LED		Dual color LED	
	PLED	SLED	PLED	SLED
S0	H	L	H	L
S1/S3	Blinking	Blinking	L	H
S4/S5	L	L	L	L

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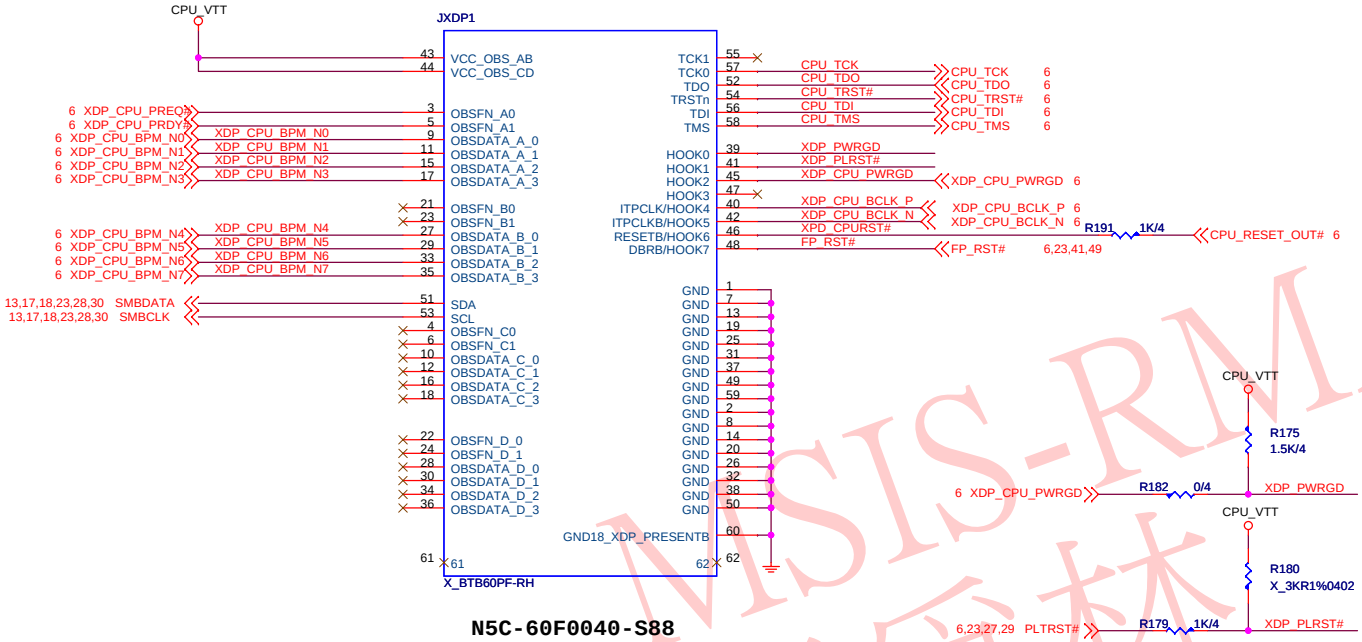
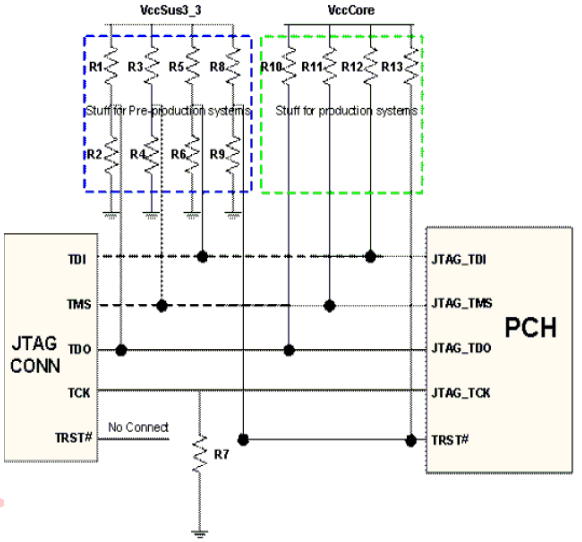
Reserve debug port



N5C-60F0040-S88



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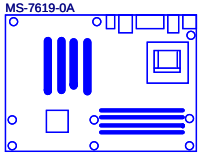
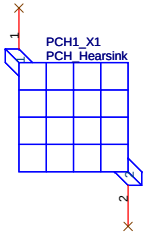
PCB

PCB1
MS-7619-0A



P30-076190B-G37,精成,33,崑山微盟廠(MSIK)
P30-076190B-E48,依頓,33,崑山微盟廠(MSIK)

PCH1_X1
PCH_Hearsink



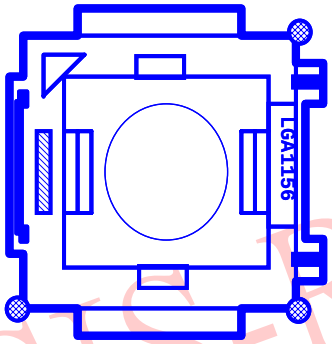
E31-0401634-K08

BAT1_X1

BAT-BCR2032P-RH

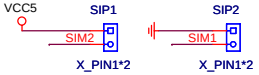
CPU SOCKET

CPU1_X1
CPU SOCKET

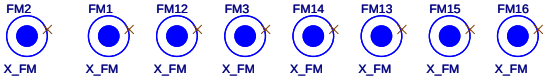


E21-7557010-F02

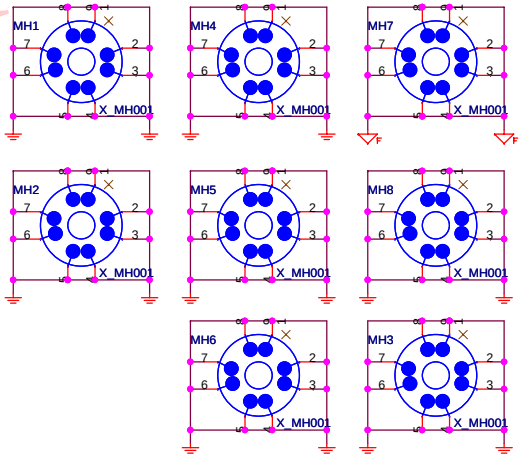
Simulation



Optical Fiducial Marks-120



Mounting Holes



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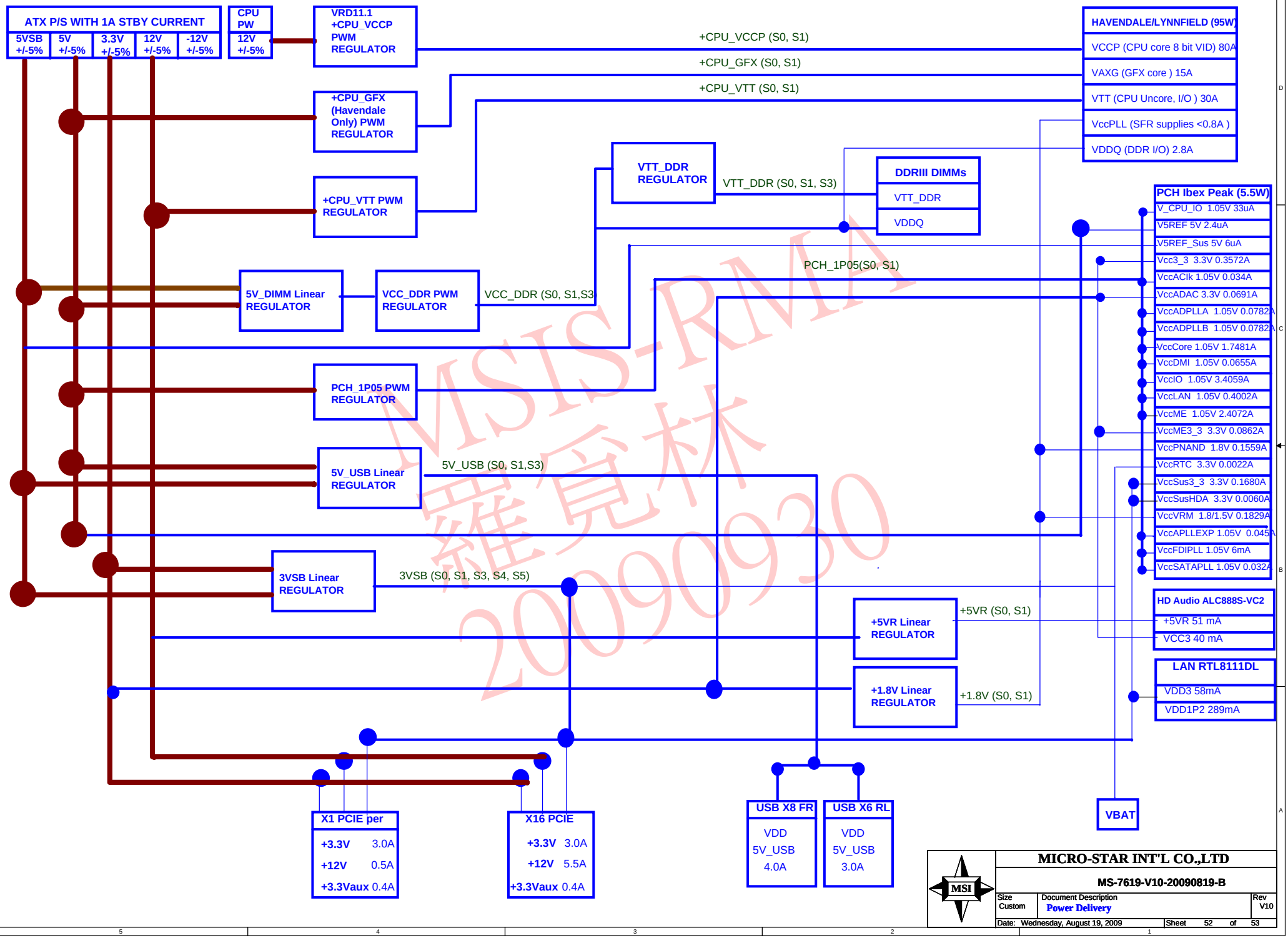

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寄件者: yumichen [yumichen@msi.com.tw]
寄件日期: 2009年4月15日 星期三 上午 11:37
收件者: jamescheng(程志鵬); lancelotsun(孫宏文)
主旨: FW: LGE IBX M/B spec

另外PCIEx16 & DDR3 用的slot料號如下

DDR3---N13-2400911-K06. N13-2400901-K06

PCIEx16--- N11-1640221-L06

Ver : 1.0

1. TOP text modify : for example V0B change to V10
2. DVI port of JVGA_DVI1: R73D43 change to R64D43 for production (only ring size modify)
3. JXDP1: remove BOT MASK
4. U25: pad width change form 9 mil to 8 mil
5. R7 change to 10K avoid RSMRST# abnormal actions
6. Add R748 (not stuff)between VREF_DQ_A and VREF_DQ_B for intel PDG rev1.5
7. For power consumption, remove R620, R608, R590
7. For Intel PDG rev1.5 stuff R324 R325

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