MS-7A40 Ver:11

CPU:
AMD AM4

System Chipset:
Promontory A320 / B350
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

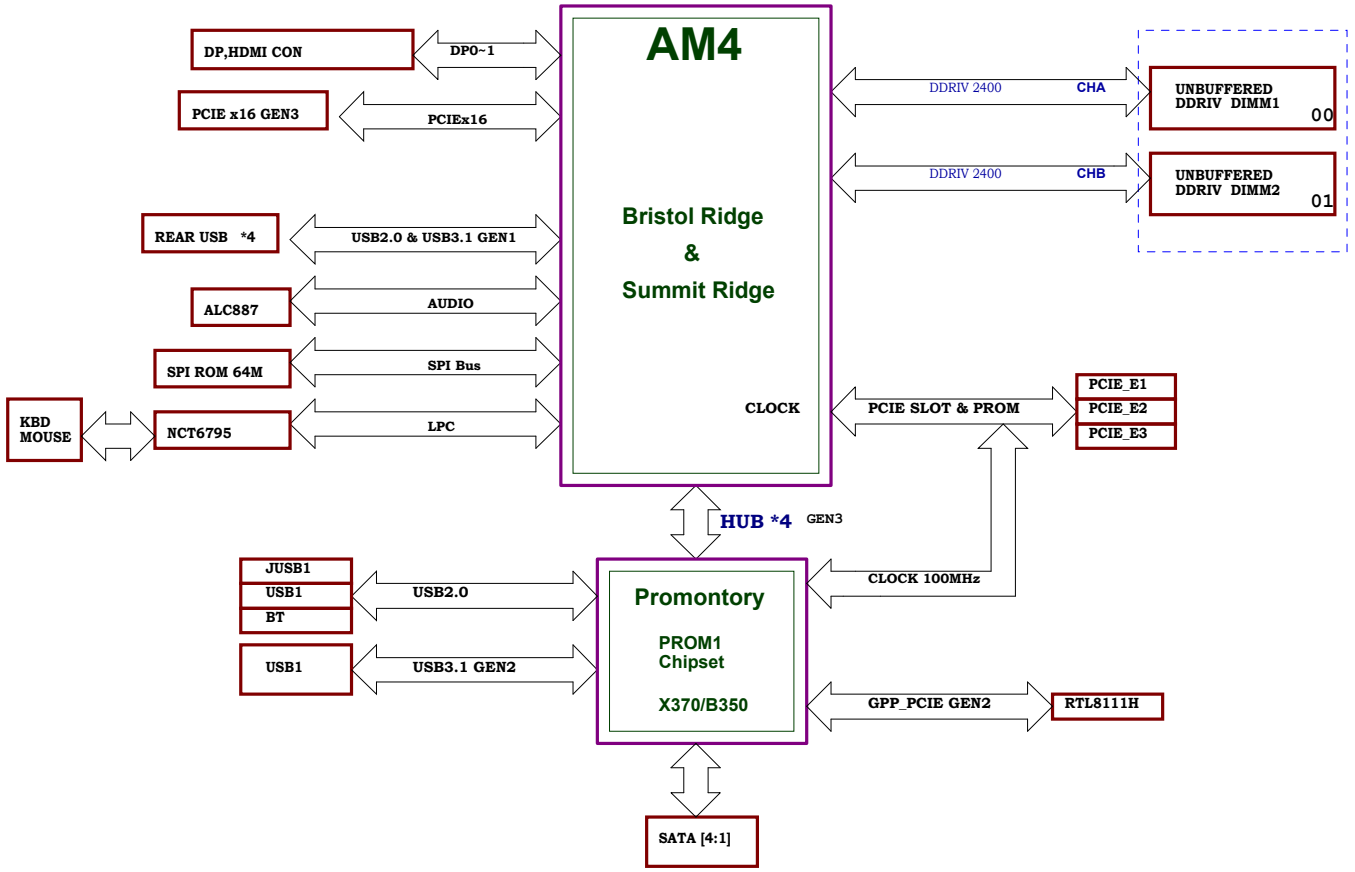
VRM
IR35201 6+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1

OCP IC:
RT9553

FUSION BLOCK DIAGRAM



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Title: Block Diagram		
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AMD AM4

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: COVER SHEET

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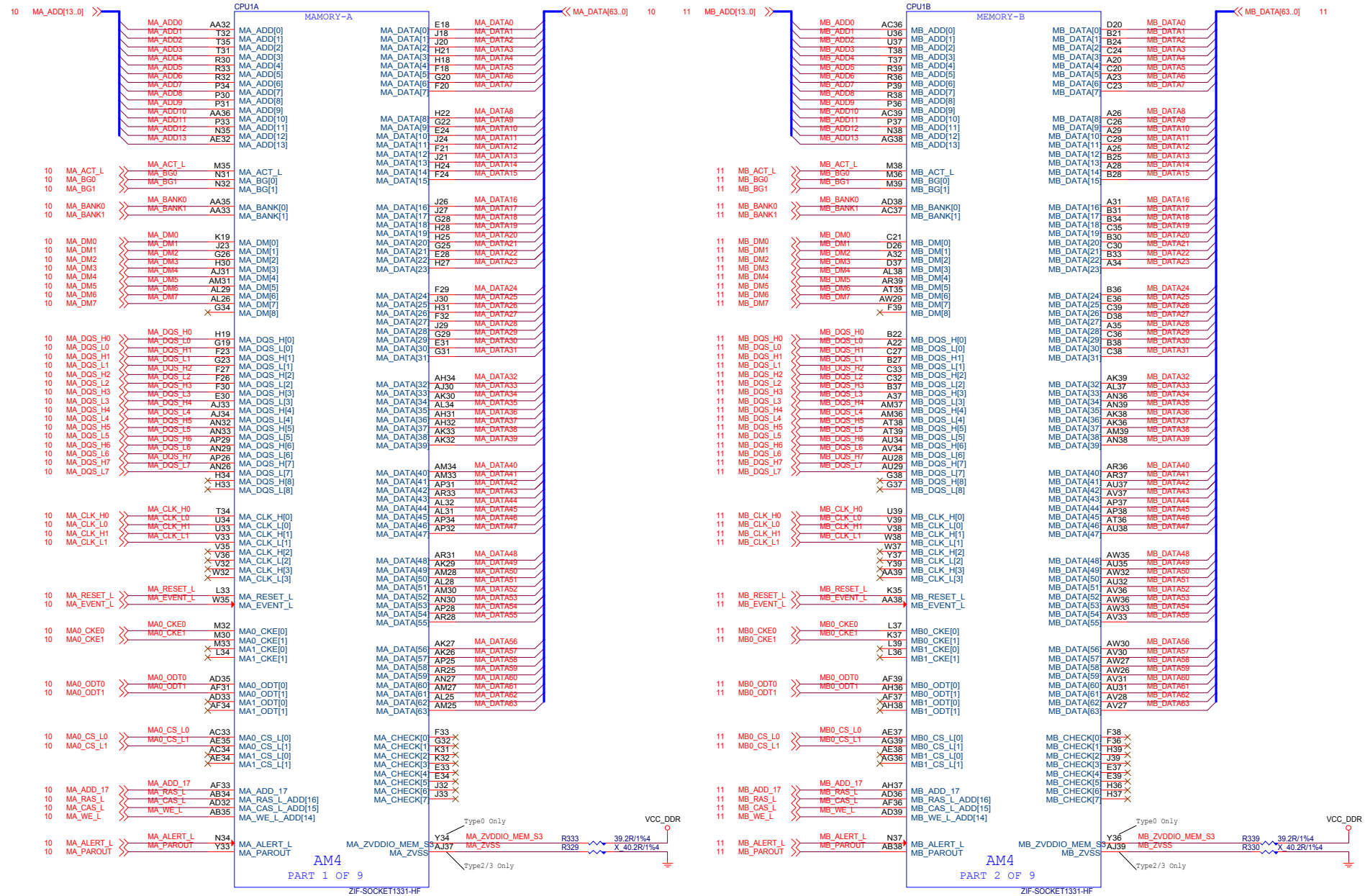

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Link to the Future

Title	AM4 DDR4 I/F	
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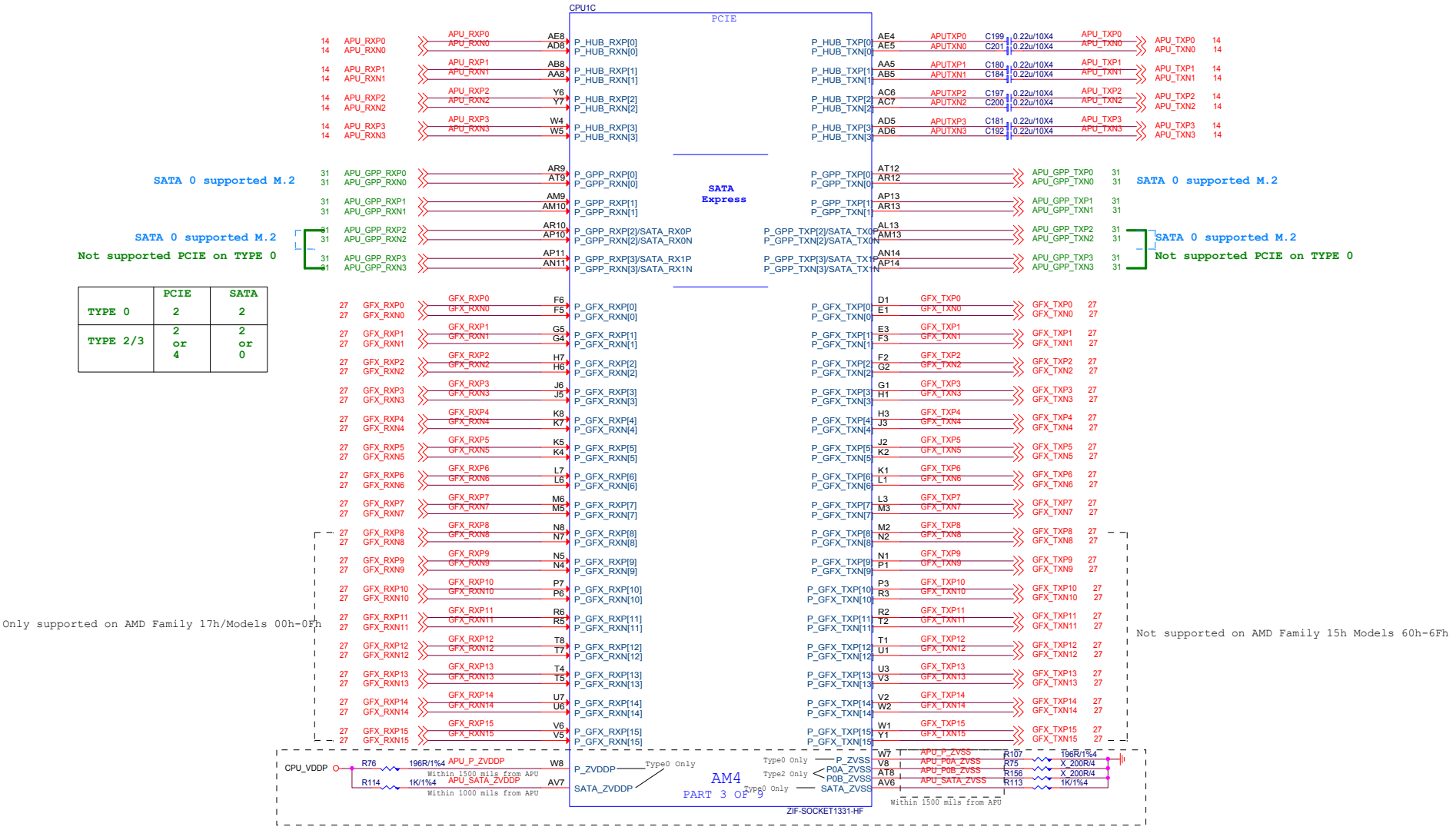

	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

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Link to the Future

Title	AM4 PCIE/SATAE	
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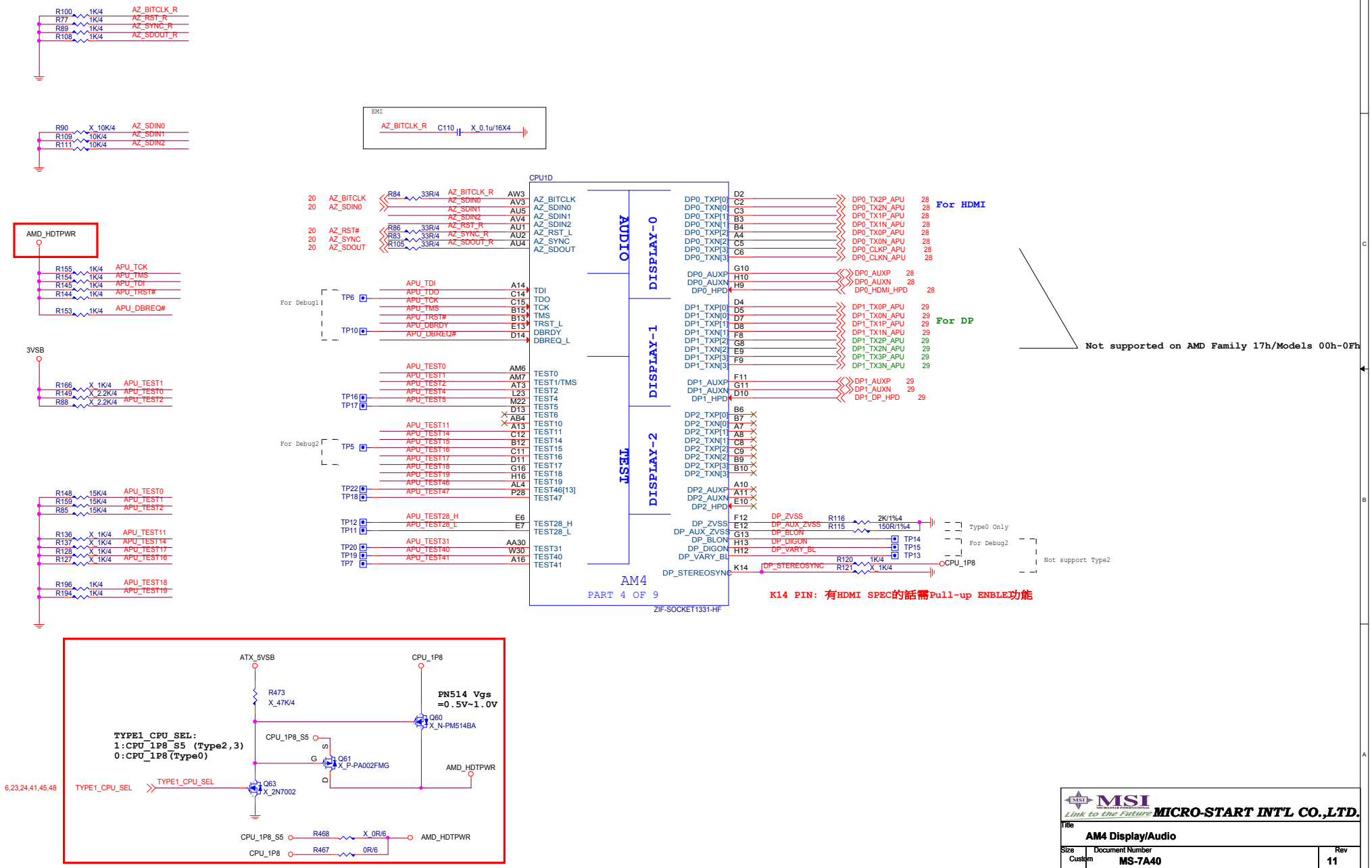

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Title	AM4 Display/Audio	
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AM4 CPU TYPE Circuit

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP

CORETYPE0
0:BR/SR
1:RV/ZP

Layout:Place x'tal within 1.5 inch of APU

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

Change by CRB rev. E

Follow CRB

For K TYPE FAN

GPIO97~100 for Debug LED

Modify USB_OC# circuit

Within 500mils

IB=(Vcc3-Vbe)/10k
(3.3-0.95)/10k=0.235mA

IC=(VCC2-Vce)/10k
(3.3-0.2)/10k=0.31mA

AMD Hardware Validated Boot (HVB)
0:Enable
1 or NC:Disable

PART 5 OF 9

ZIF-SOCKET1331-HF

Title	AM4 SVI/ACPI/GPIO
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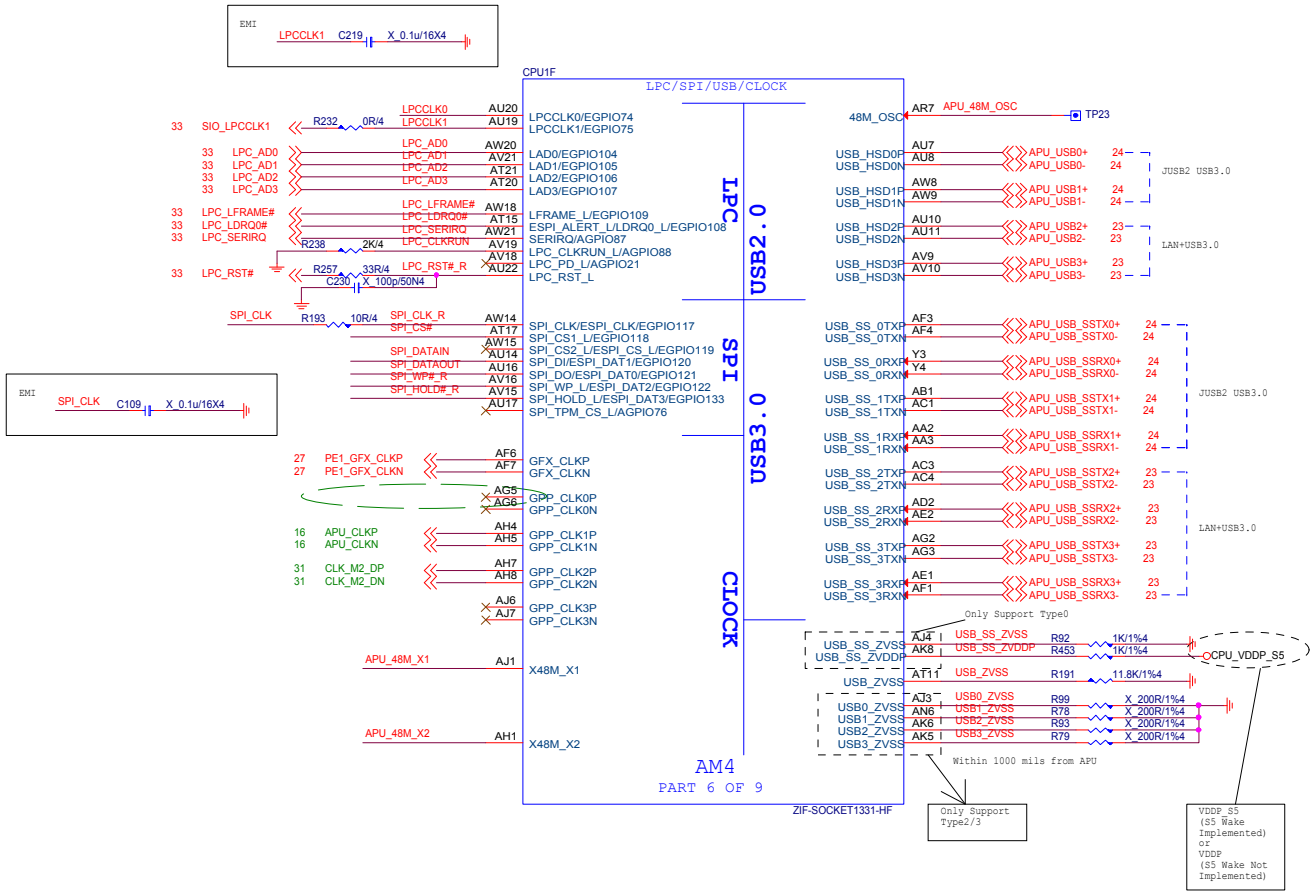
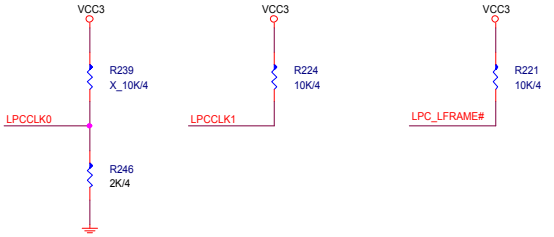
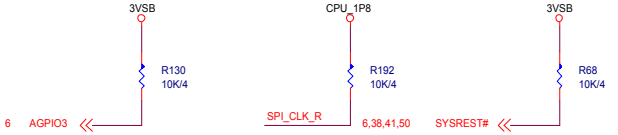
MICRO-START INT'L CO.,LTD.



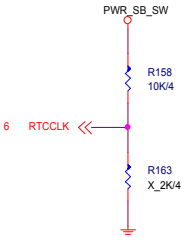
Strapping Options



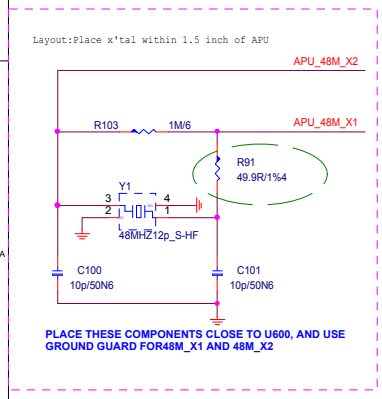
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



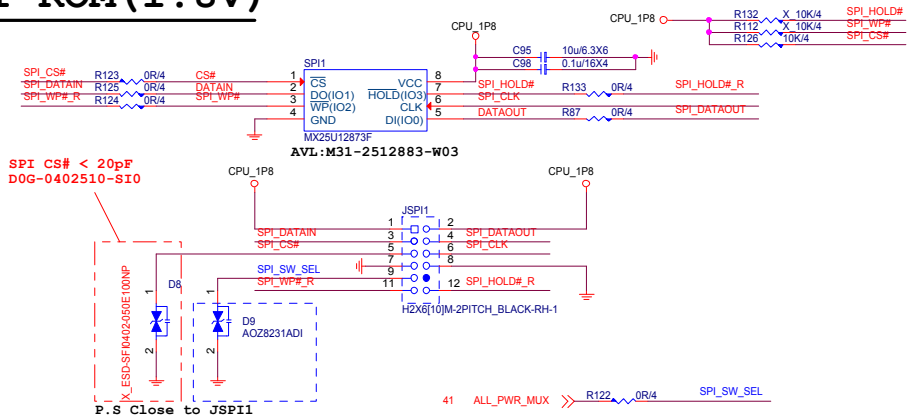
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board



SPI ROM(1.8V)



MSI MICRO-STAR INTERNATIONAL	MICRO-STAR INT'L CO.,LTD.
Title	AM4 LPC/SPI/USB/CLK/STRAP
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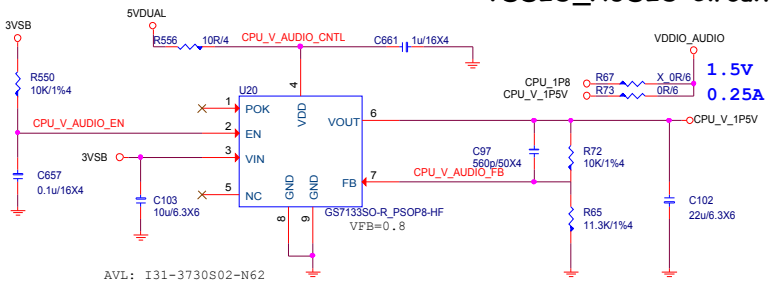
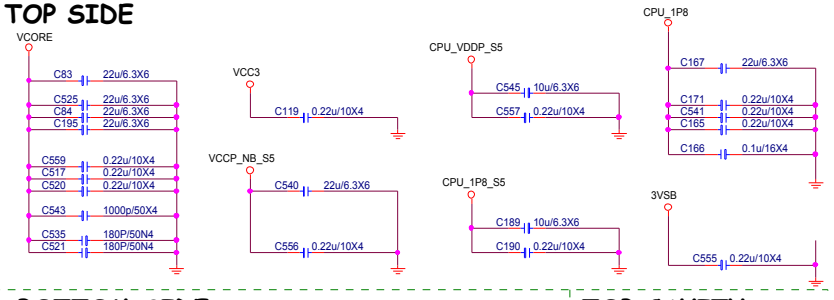
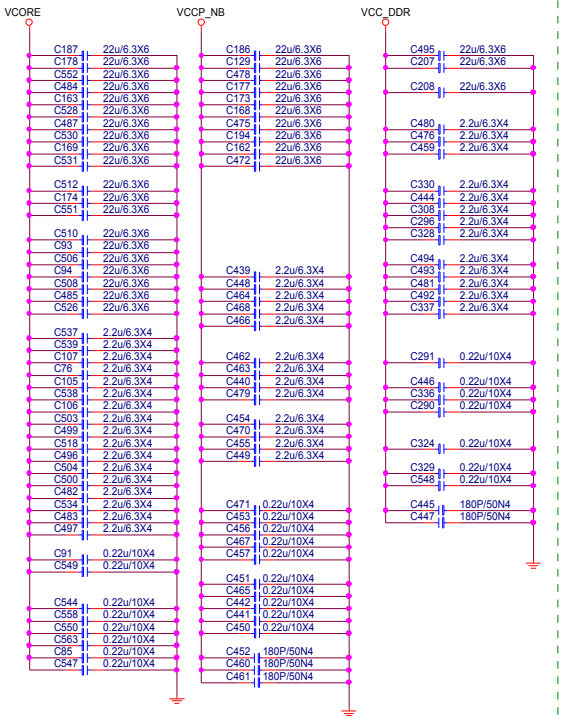
VDDIO_AUDIO Circuit



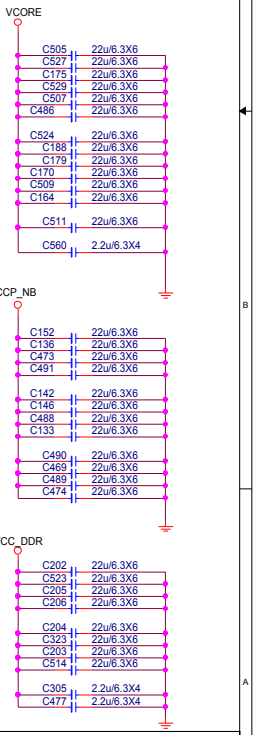
TOP SIDE

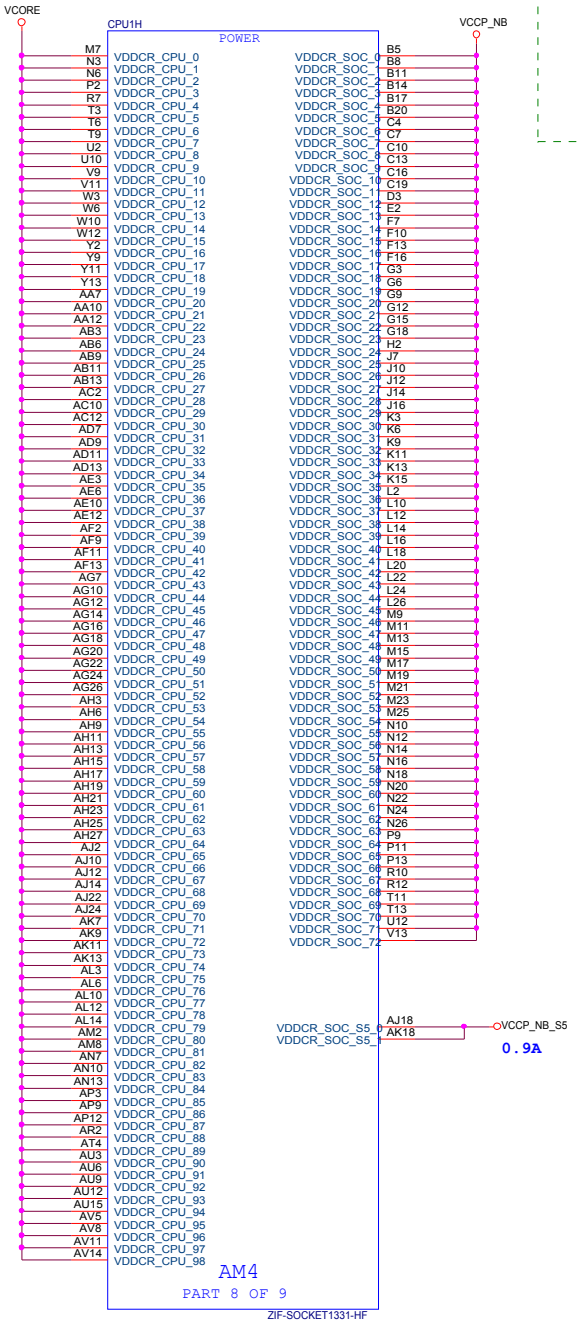


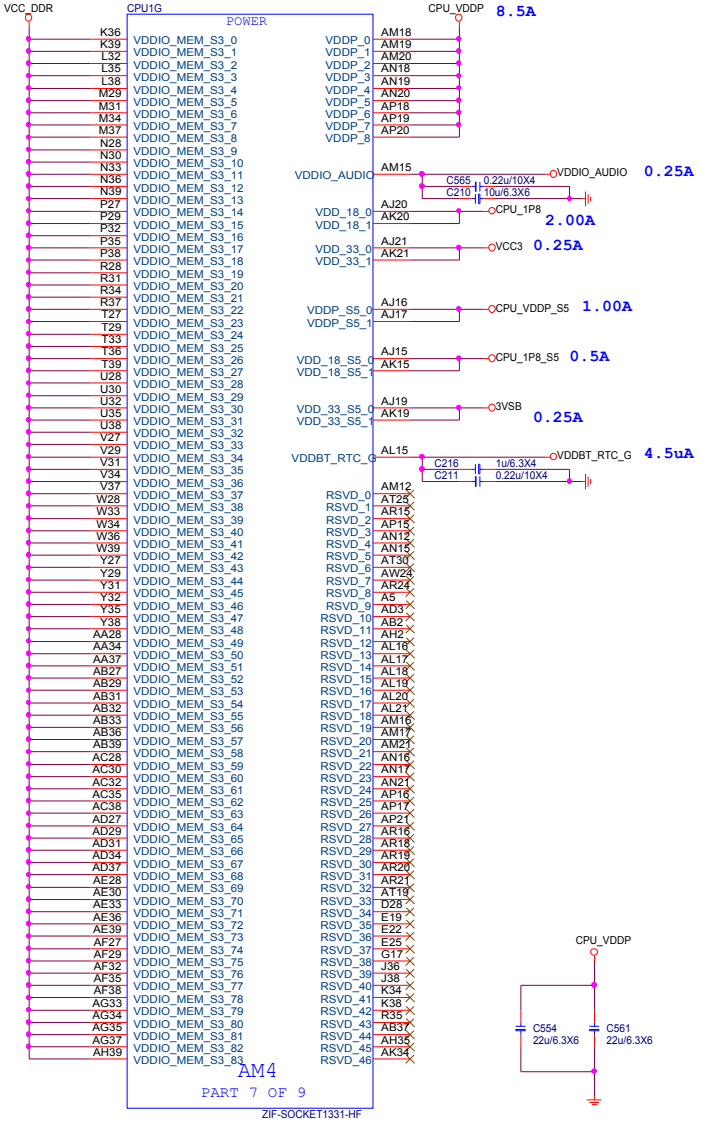
BOTTOM SIDE



TOP CAVITY







MICRO-START INT'L CO.,LTD.

Title	AM4 Power/RTC Power	
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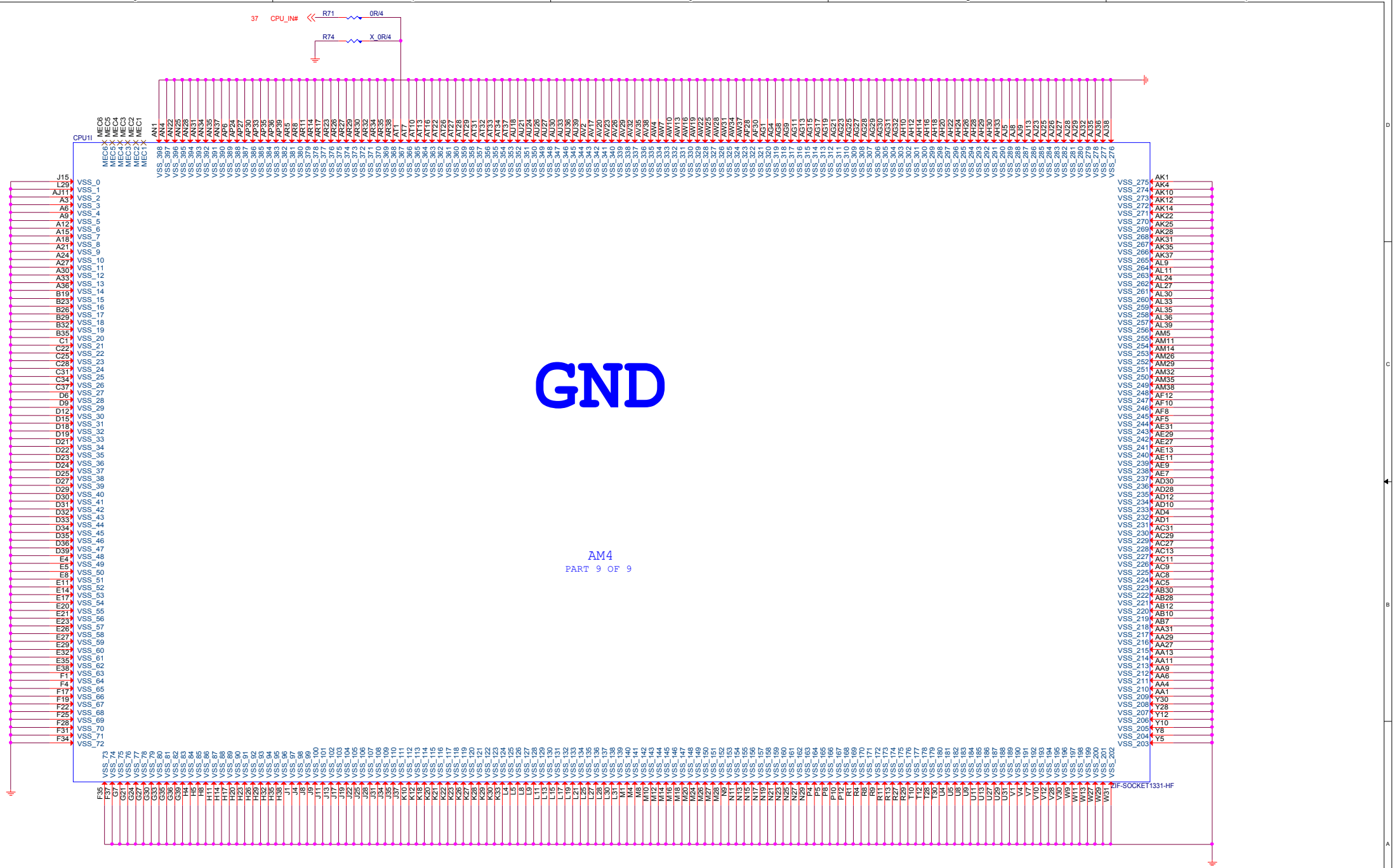

MSI MICRO-STAR INTERNATIONAL Link to the Future MICRO-START INT'L CO.,LTD.			
Title: AM4 GND			
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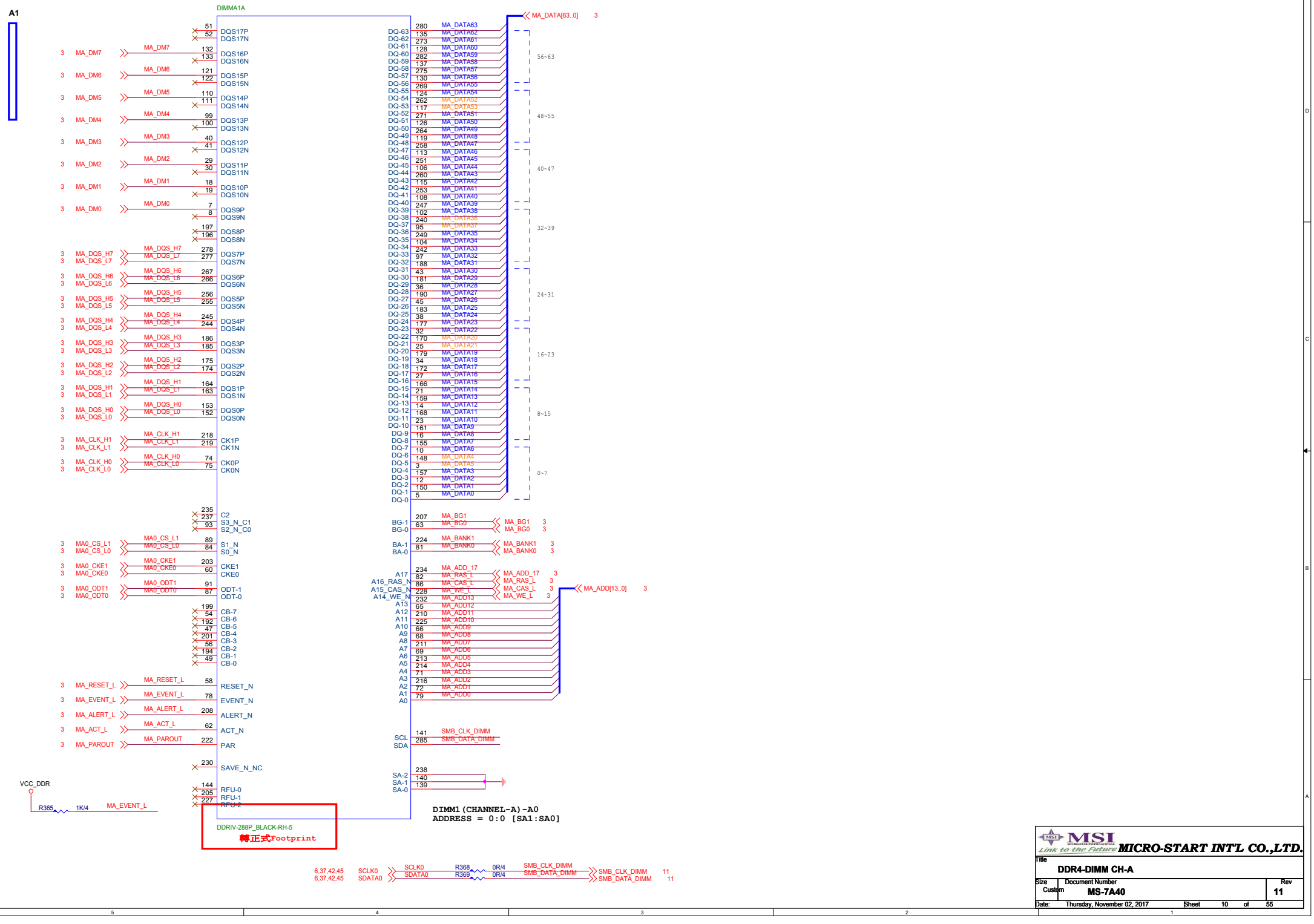
A1
DIMMA1A
MA_DATA[63..0] 3
MA_ADD[13..0] 3
MA_DM7
MA_DM6
MA_DM5
MA_DM4
MA_DM3
MA_DM2
MA_DM1
MA_DM0
MA_DQS_H7
MA_DQS_L7
MA_DQS_H6
MA_DQS_L6
MA_DQS_H5
MA_DQS_L5
MA_DQS_H4
MA_DQS_L4
MA_DQS_H3
MA_DQS_L3
MA_DQS_H2
MA_DQS_L2
MA_DQS_H1
MA_DQS_L1
MA_DQS_H0
MA_DQS_L0
MA_CLK_H1
MA_CLK_L1
MA_CLK_H0
MA_CLK_L0
MA0_CS_L1
MA0_CS_L0
MA0_CKE1
MA0_CKE0
MA0_ODT1
MA0_ODT0
MA_RESET_L
MA_EVENT_L
MA_ALERT_L
MA_ACT_L
MA_PAROUT
VCC_DDR
R365 1K/4 MA_EVENT_L
DDRIV-288P_BLACK-RH-5
轉正式Footprint
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
SMB_CLK_DIMM
SMB_DATA_DIMM
SCLK0
SDATA0
R368 0R/4
R369 0R/4
MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future
Title
DDR4-DIMM CH-A
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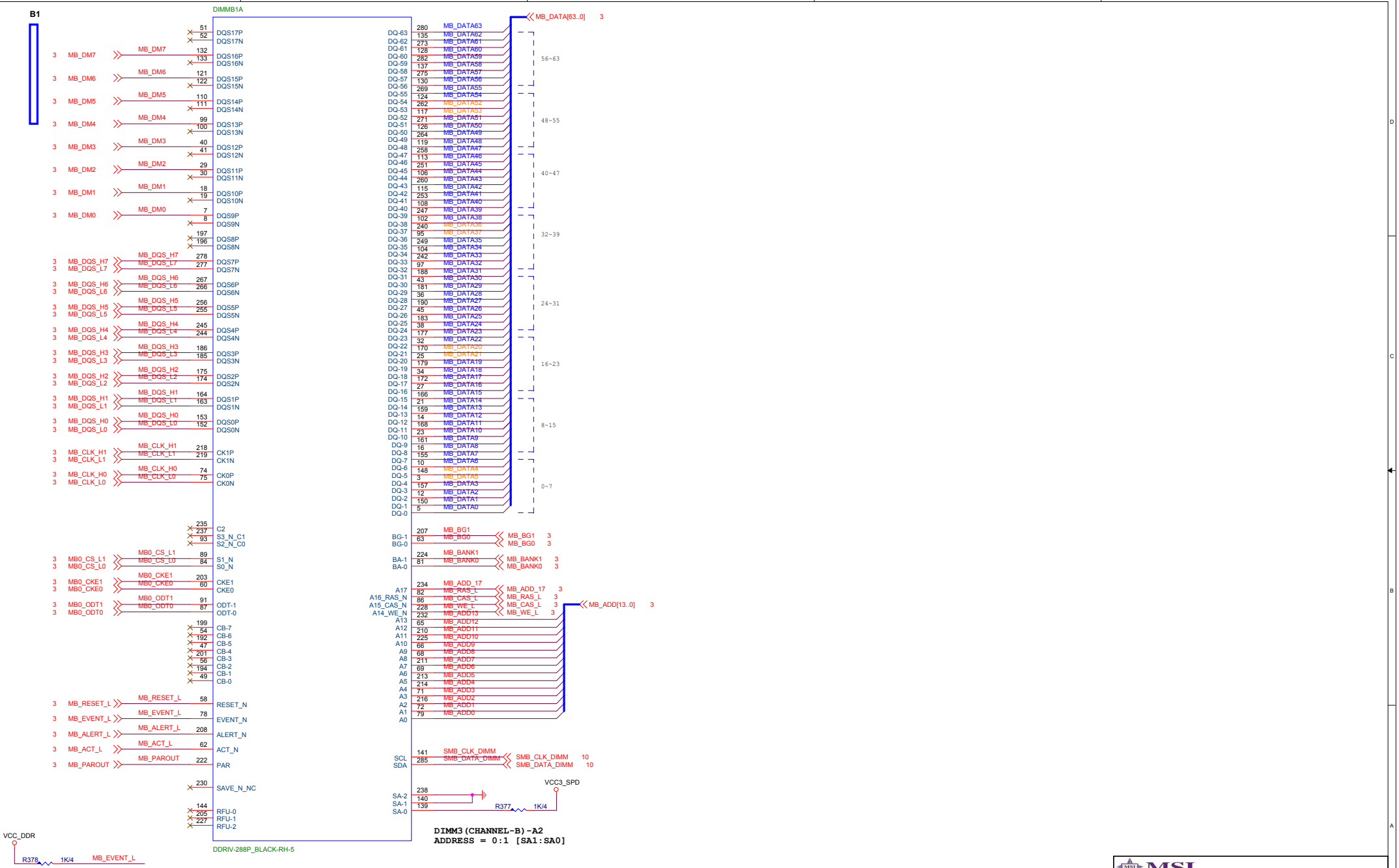

Title	DDR4-DIMM CH-B
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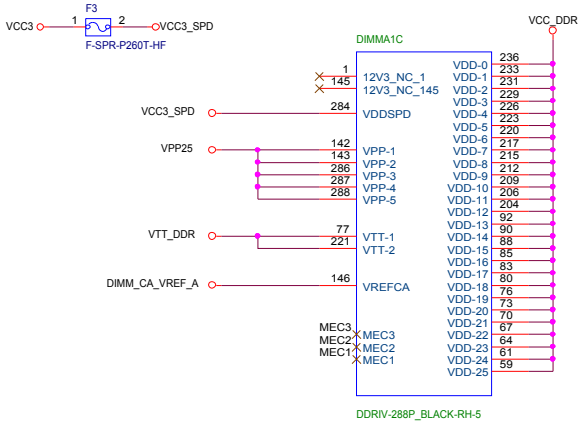
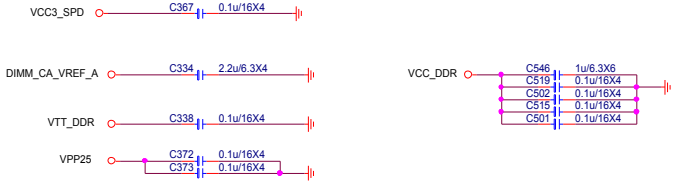
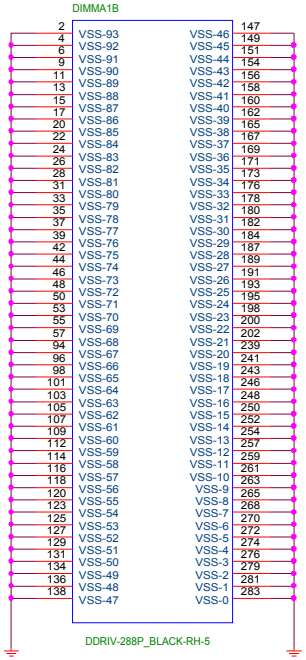
MICRO-START INT'L CO.,LTD.



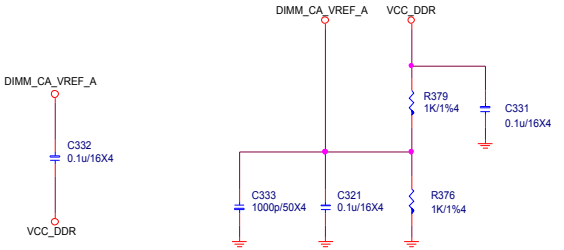
DIMM SLOT PN BY SPEC





DDR VREF

(place resistors close to DIMMs)



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Title: DDR4-POWER/GND-1		
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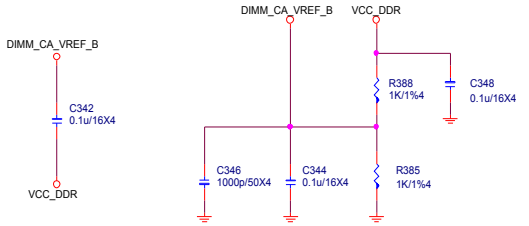
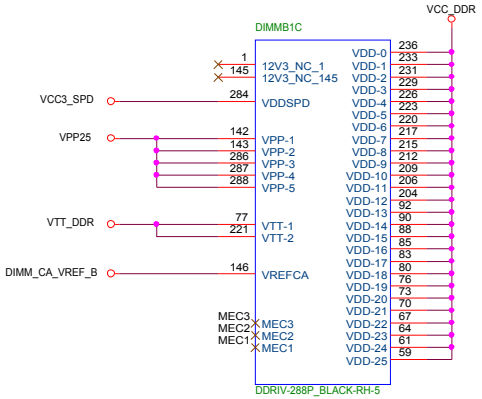
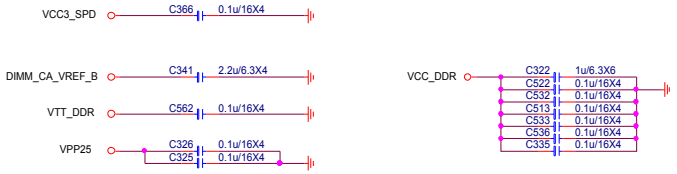
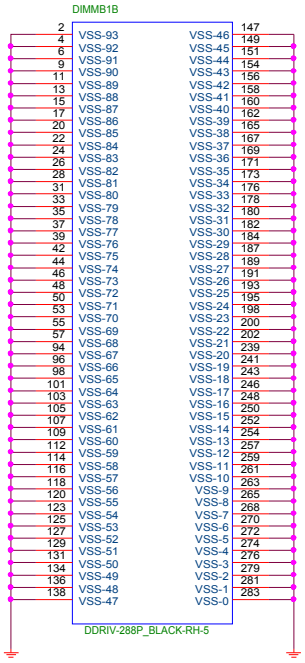
DDR VREF

(place resistors close to DIMMs)









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Link to the Future

Title: DDR4-POWER/GND-2		
Size: Custom	Document Number: MS-7A40	Rev: 11
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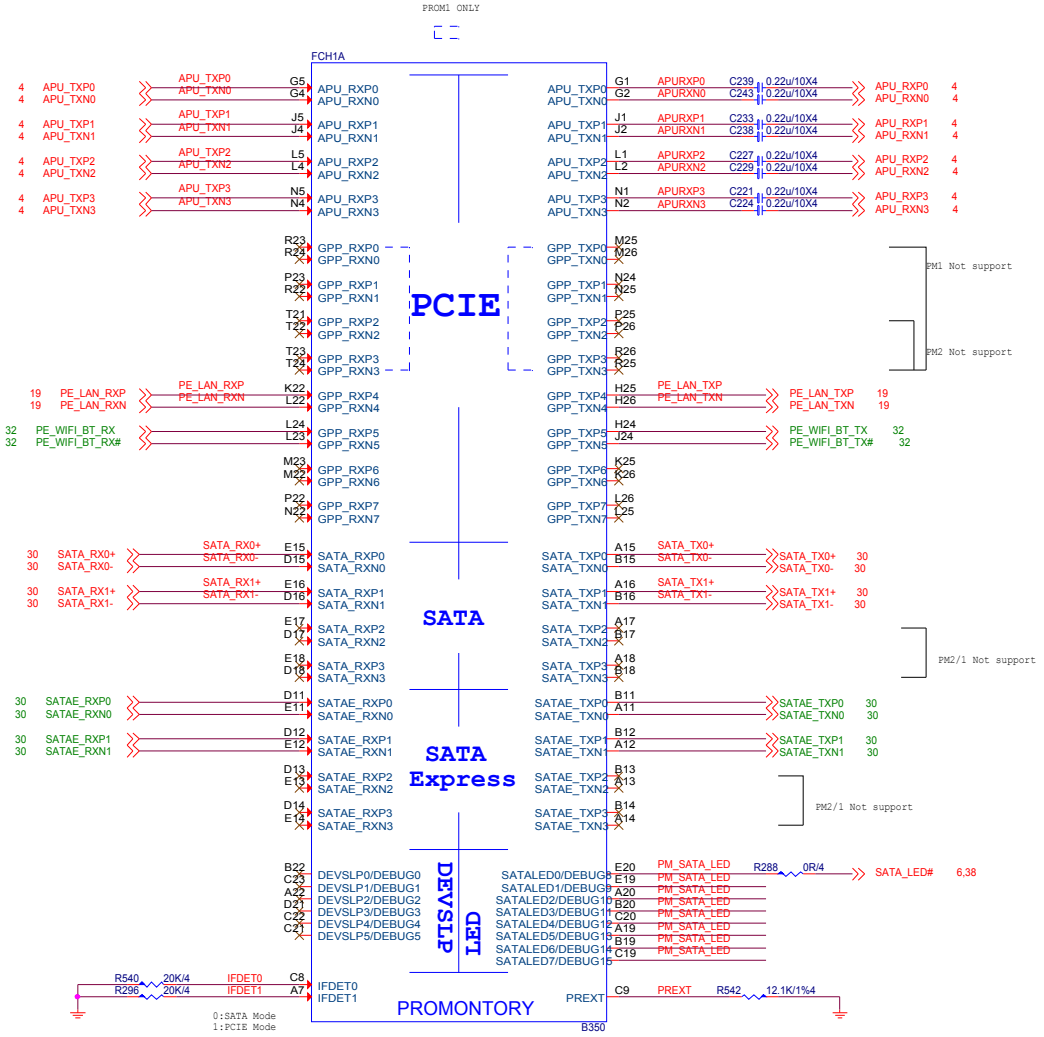

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: Promontory-PCIE/SATA/SATAE

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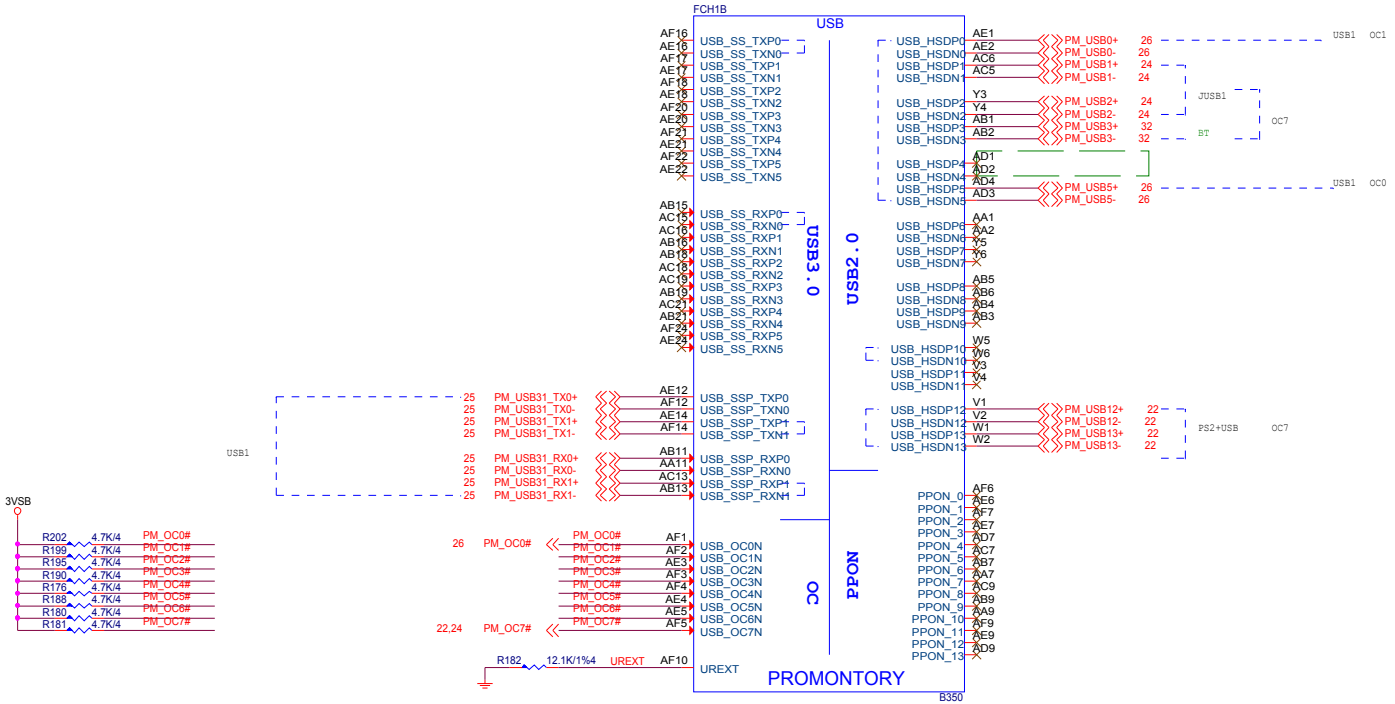

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

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Link to the Future

Title	Promontory-USB/OC	
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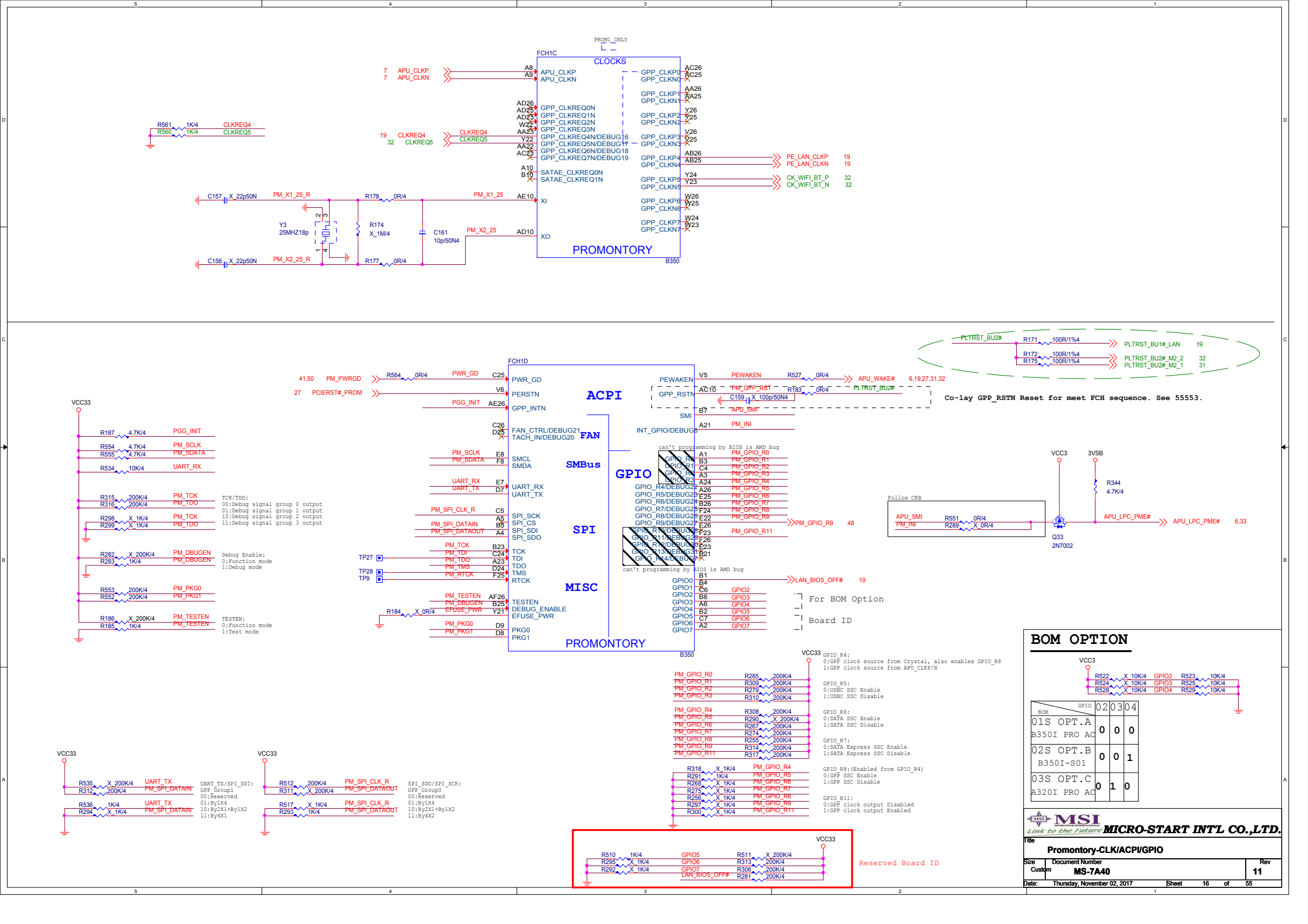
PROM1_ONLY
FCH1C
CLOCKS
APU_CLKP
APU_CLKN
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEBUG16
GPP_CLKREQ5N/DEBUG17
GPP_CLKREQ6N/DEBUG18
GPP_CLKREQ7N/DEBUG19
SATAE_CLKREQ0N
SATAE_CLKREQ1N
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
PE_LAN_CLKP
PE_LAN_CLKN
CK_WIFI_BT_P
CK_WIFI_BT_N
CLKREQ4
CLKREQ5
XI
XO
PM_X1_25
PM_X2_25
PROMONTORY
B350
ACPI
FAN
SMBus
GPIO
SPI
MISC
PWR_GD
PERSTN
GPP_INTN
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMCL
SMDA
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
TCK
TDI
TDO
TMS
RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PKG0
PKG1
PEWAKEN
GPP_RSTN
SMI
INT_GPIO/DEBUG8
PM_INI
PM_GPIO_R0
PM_GPIO_R1
PM_GPIO_R2
PM_GPIO_R3
PM_GPIO_R4
PM_GPIO_R5
PM_GPIO_R6
PM_GPIO_R7
PM_GPIO_R8
PM_GPIO_R9
PM_GPIO_R11
LAN_BIOS_OFF#
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
APU_WAKE#
PLTRST_BU2#
PLTRST_BU1#_LAN
PLTRST_BU2#_M2_2
PLTRST_BU2#_M2_1
APU_SMI
APU_LPC_PME#
Q33
2N7002
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
For BOM Option
Board ID
Reserved Board ID
BOM OPTION
01S OPT.A B350I PRO AC
02S OPT.B B350I-S01
03S OPT.C A320I PRO AC
MICRO-STAR INT'L CO.,LTD.
Promontory-CLK/ACPI/GPIO
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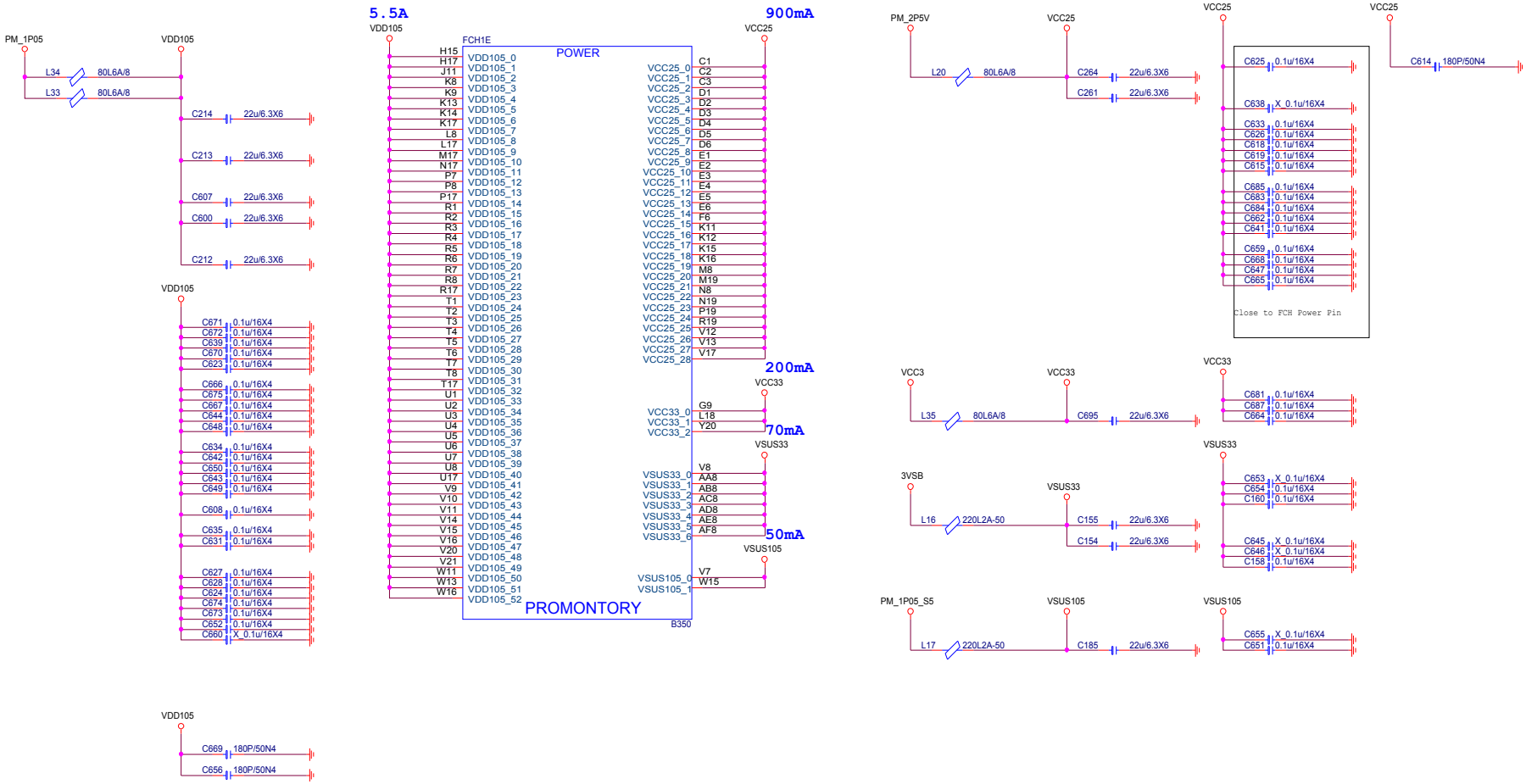
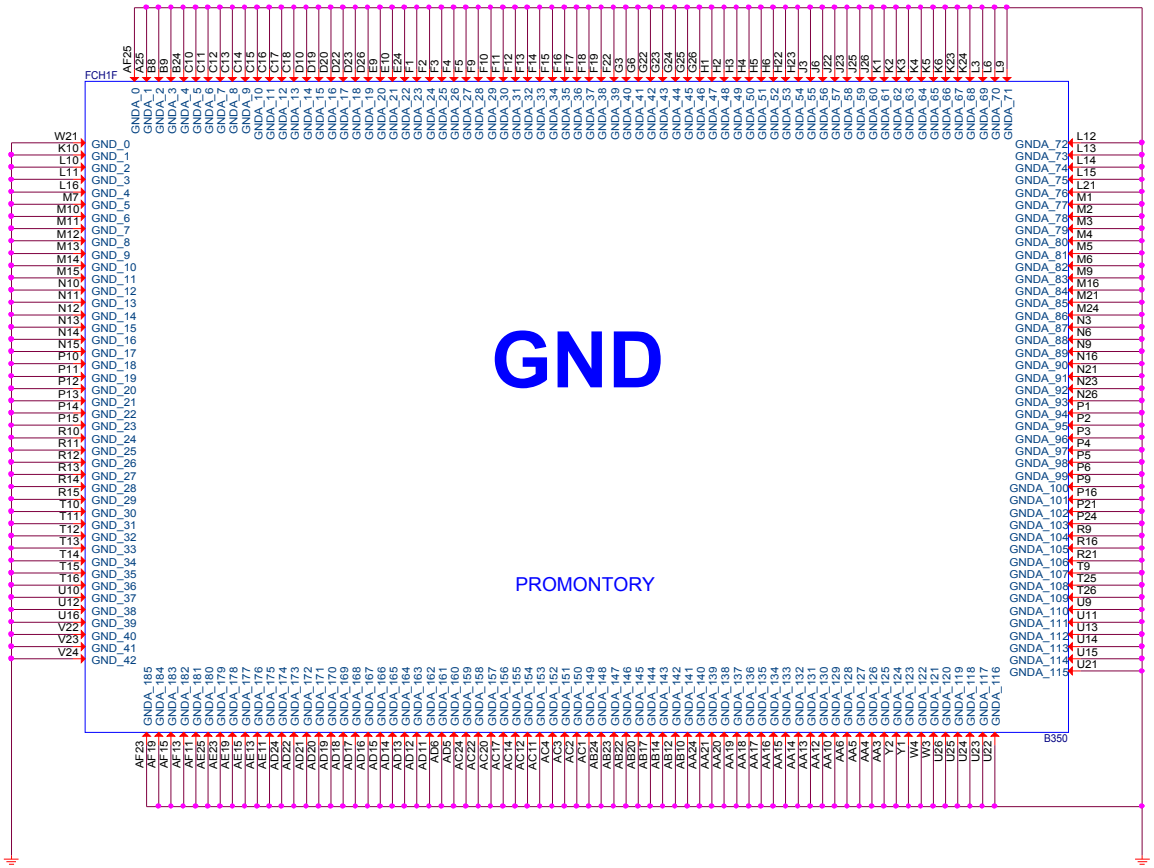

5.5A
900mA
200mA
70mA
50mA
FCH1E
POWER
PROMONTORY
B350
Close to FCH Power Pin
MICRO-STAR INT'L CO.,LTD.
Promontory-Power
MS-7A40
Thursday, November 02, 2017



MSI MICRO-STAR INT'L CO.,LTD.	
Title	Promontory-GND
Size: Custom	Document Number: MS-7A40
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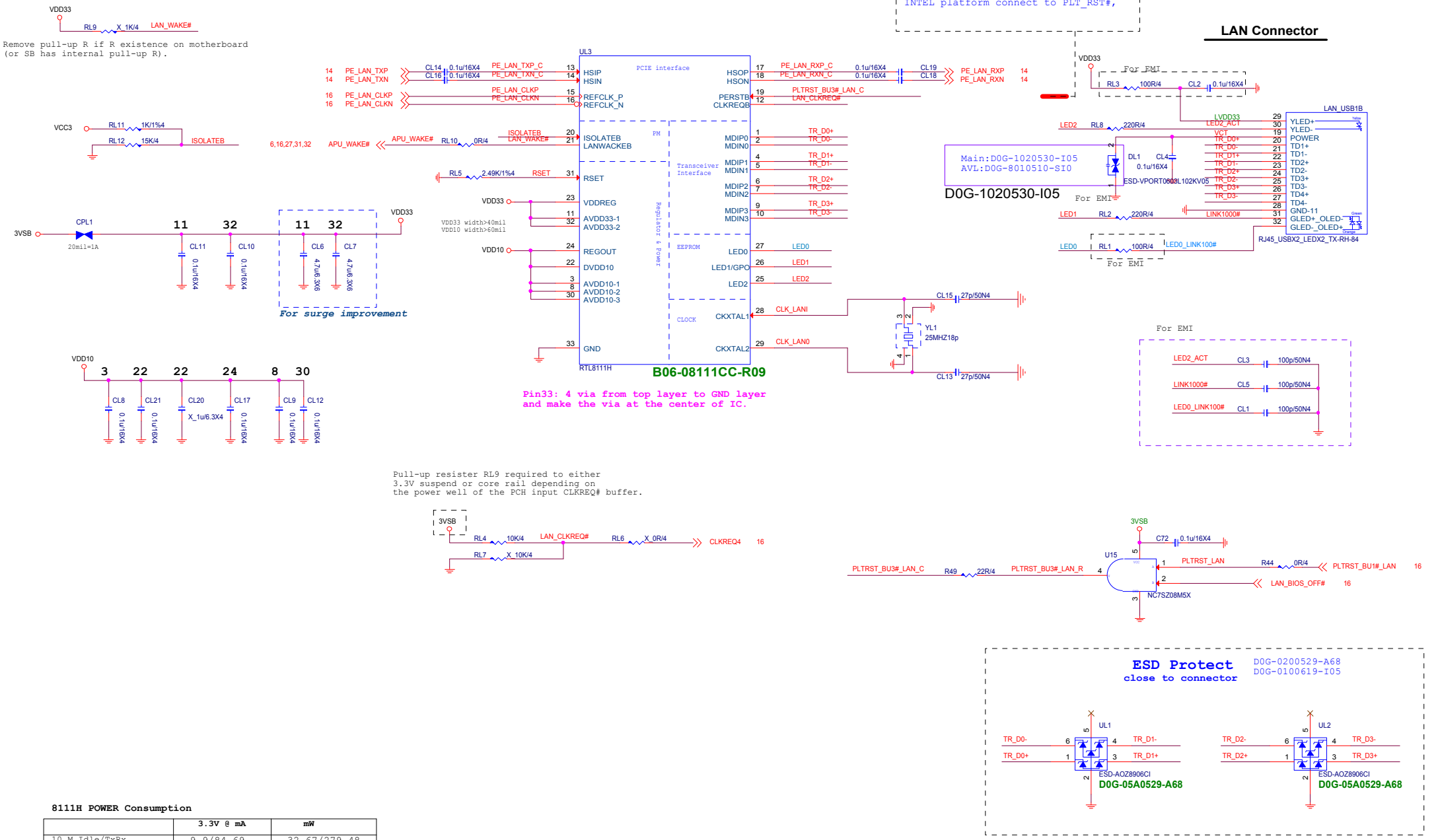
RTL8111H Giga LAN

3.3V@177.57mA



8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-START INT'L CO.,LTD.

Title: LAN-RLT 8111H		
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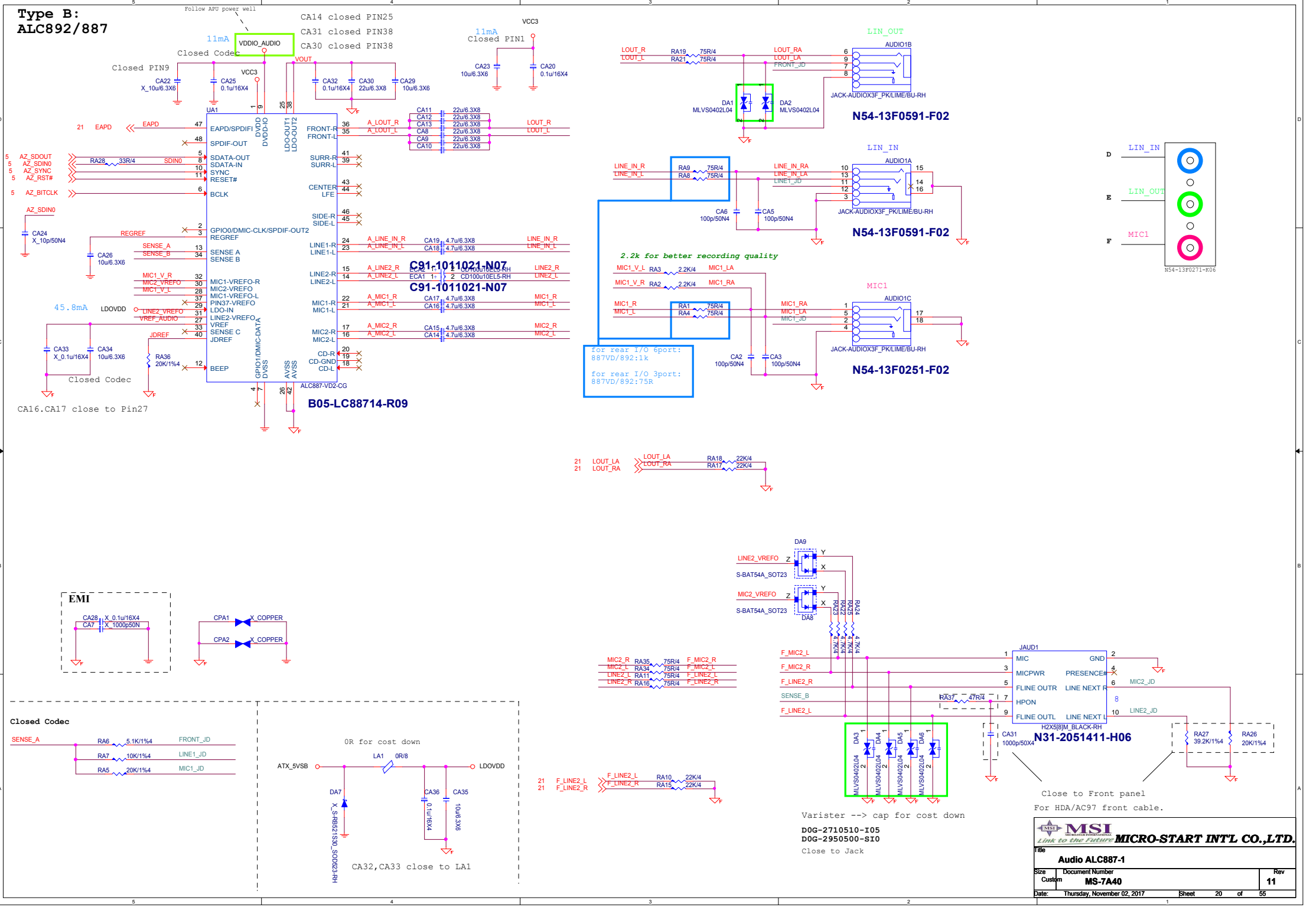
Type B: ALC892/887



MICRO-START INT'L CO.,LTD.

Title	Audio ALC887-1	
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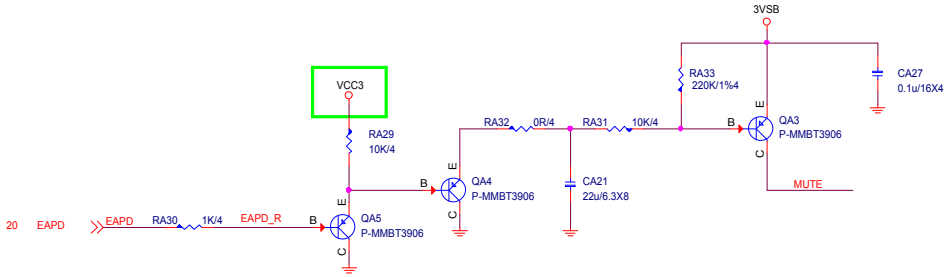
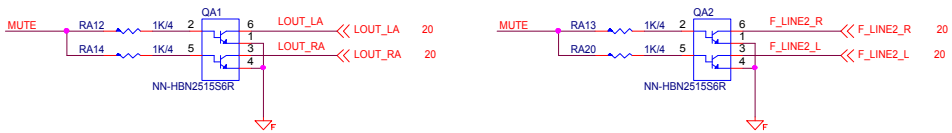
Rear Line OUT De-POP circuit

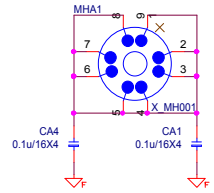
De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog





MICRO-START INT'L CO.,LTD.

Title: Audio ALC887-2

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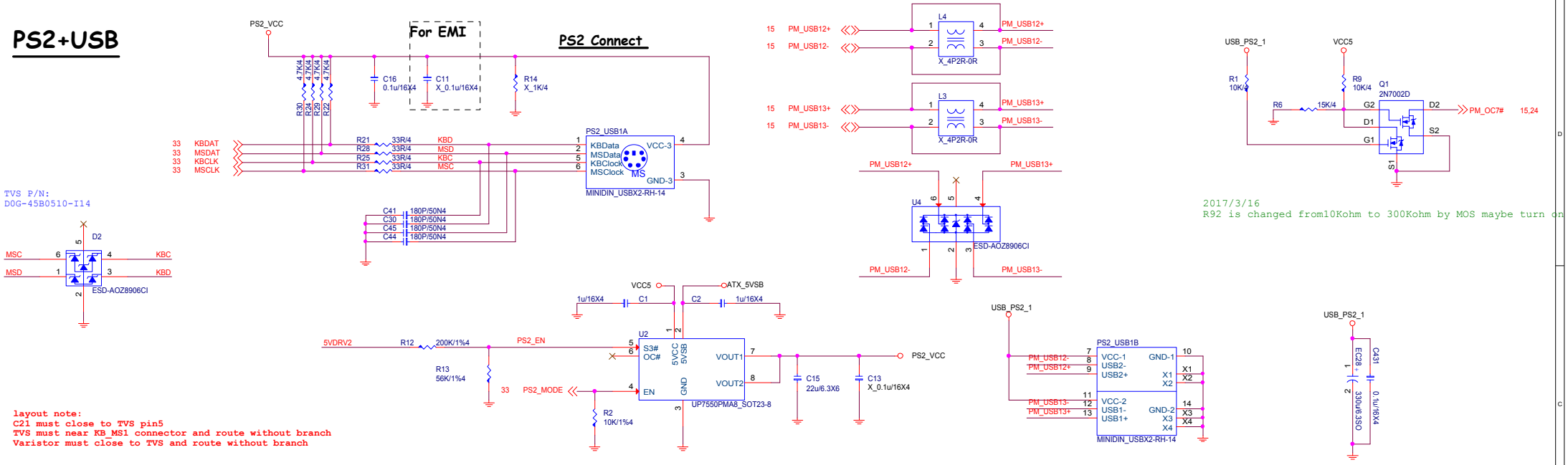
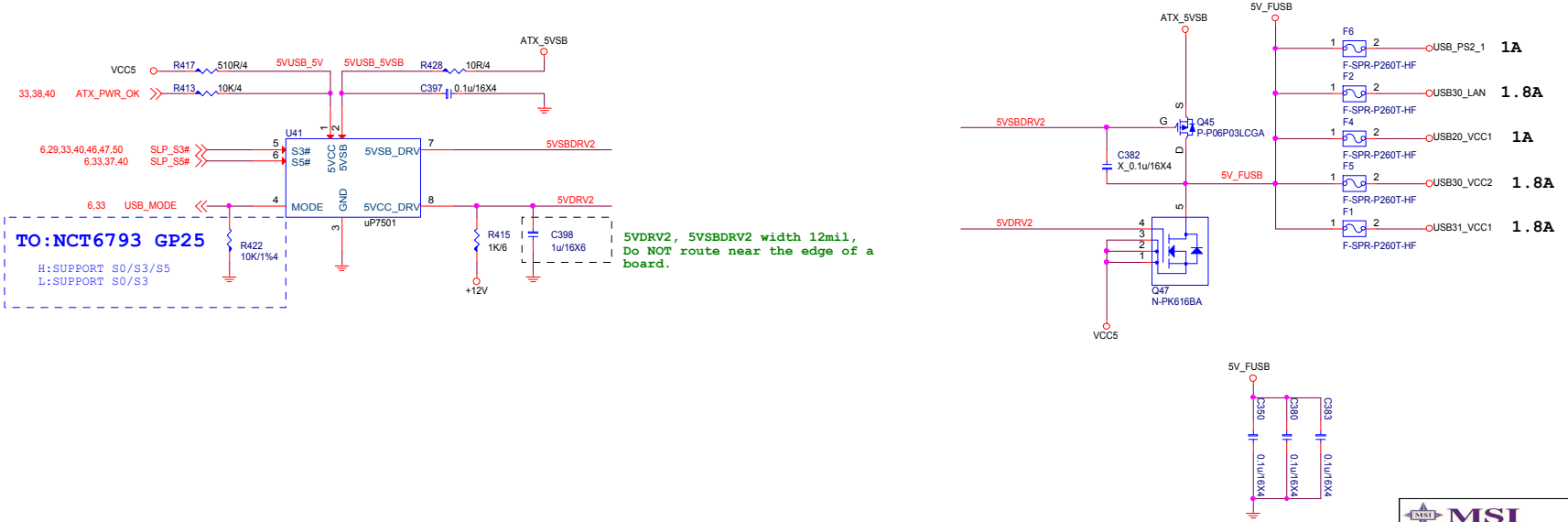
PS2+USB



layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

USB Power



MICRO-STAR INT'L CO.,LTD.

Title: USB Rear PS2+USB2.0

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Custom	MS-7A40	11

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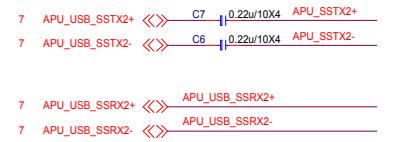
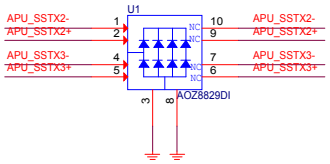
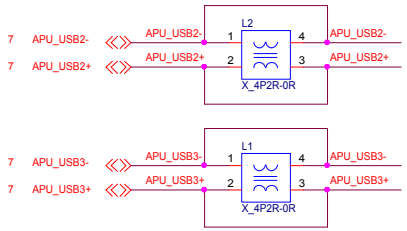
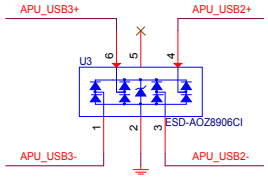
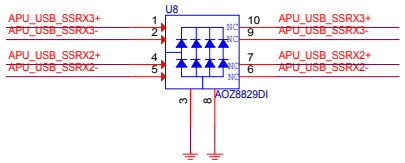
USB3.1 GEN1

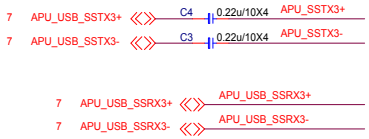




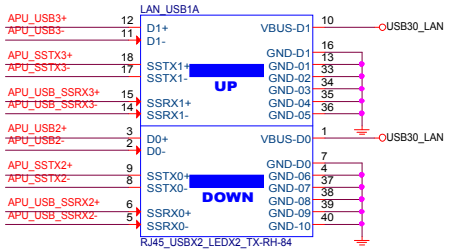


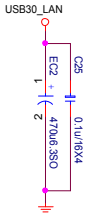


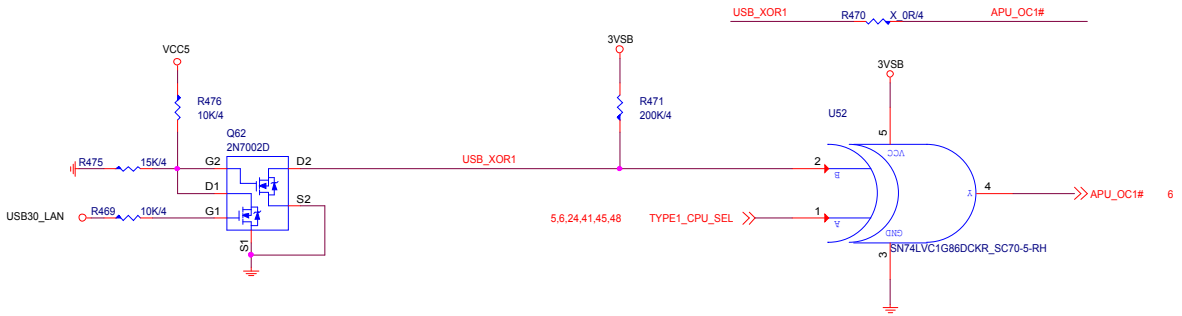




LAN+USB







Modify USB_OC# circuit

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	USB Rear LAN+USB3.1 GEN1	
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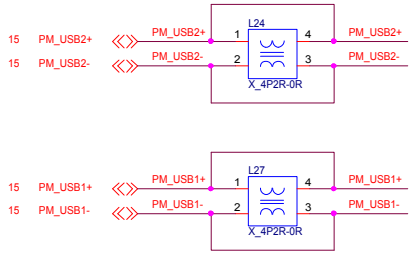
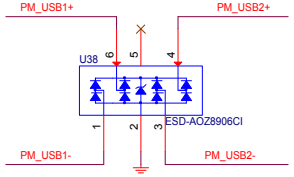
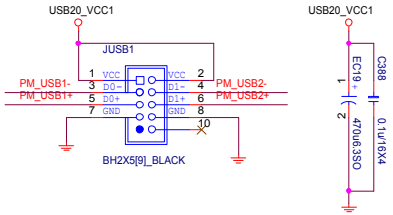
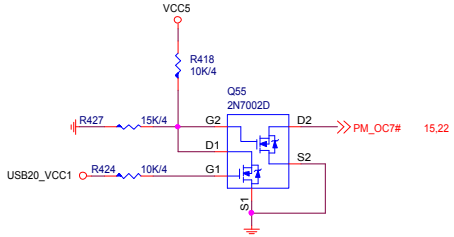
Front USB2.0



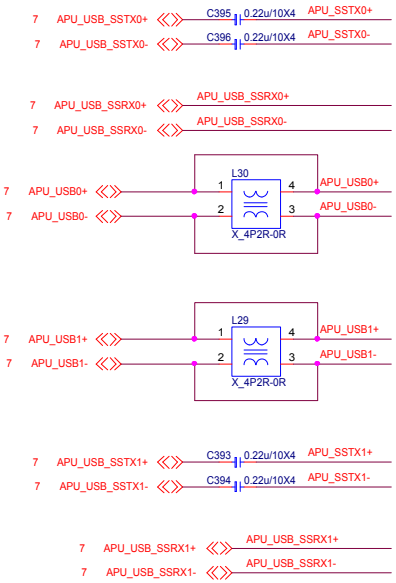


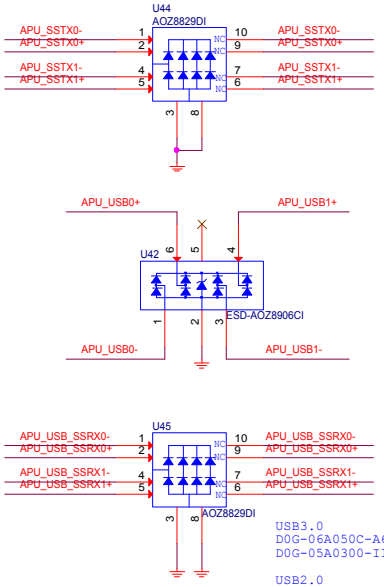


2017/3/16
R864 is changed from10Kohm to 300Kohm by MOS maybe turn on



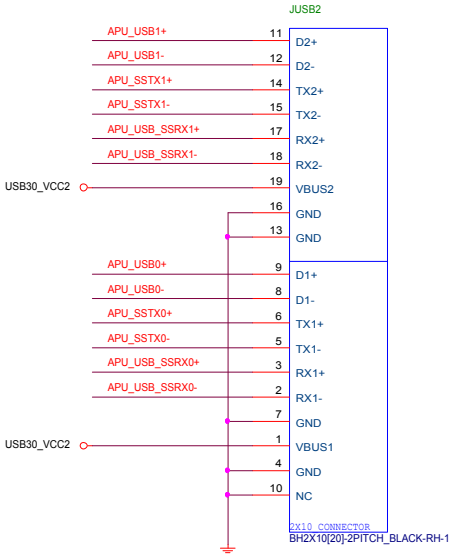
Front USB3.1 GEN1

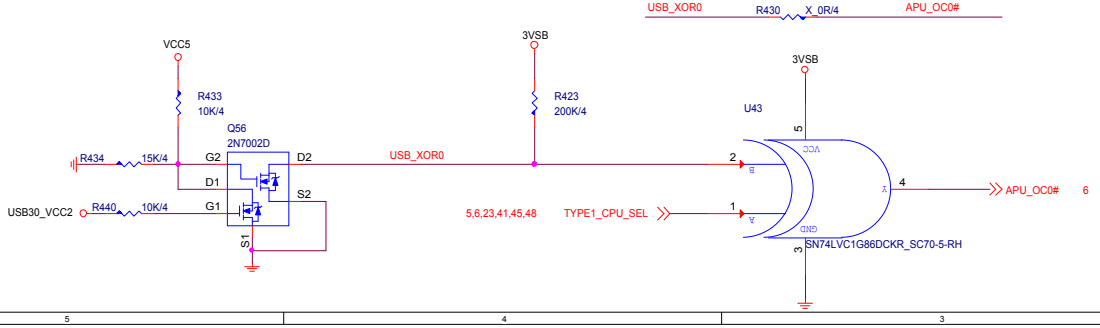


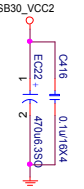


USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL







MSI MICRO-STAR INTERNATIONAL
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: USB Front Side		
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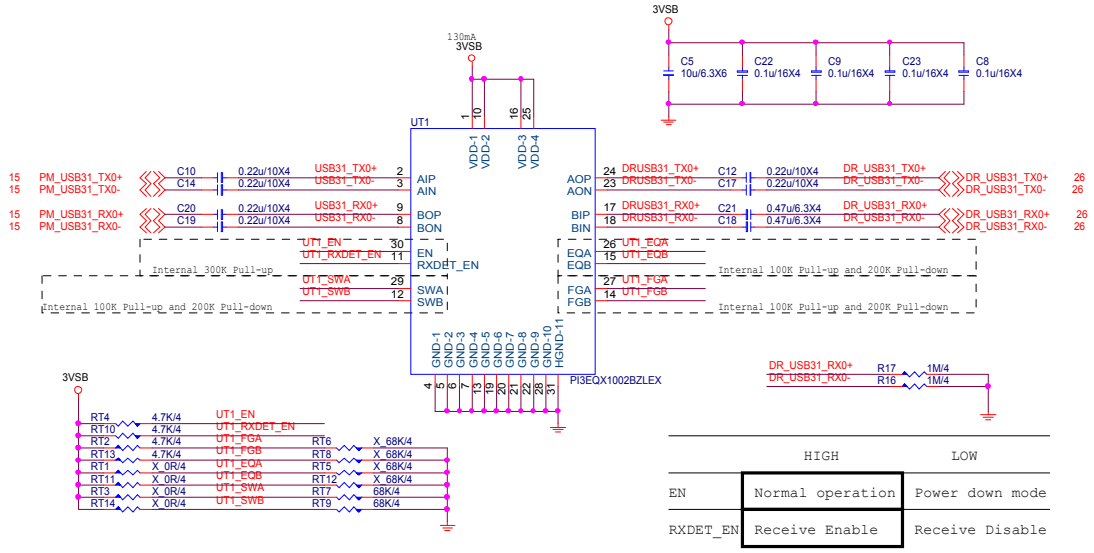
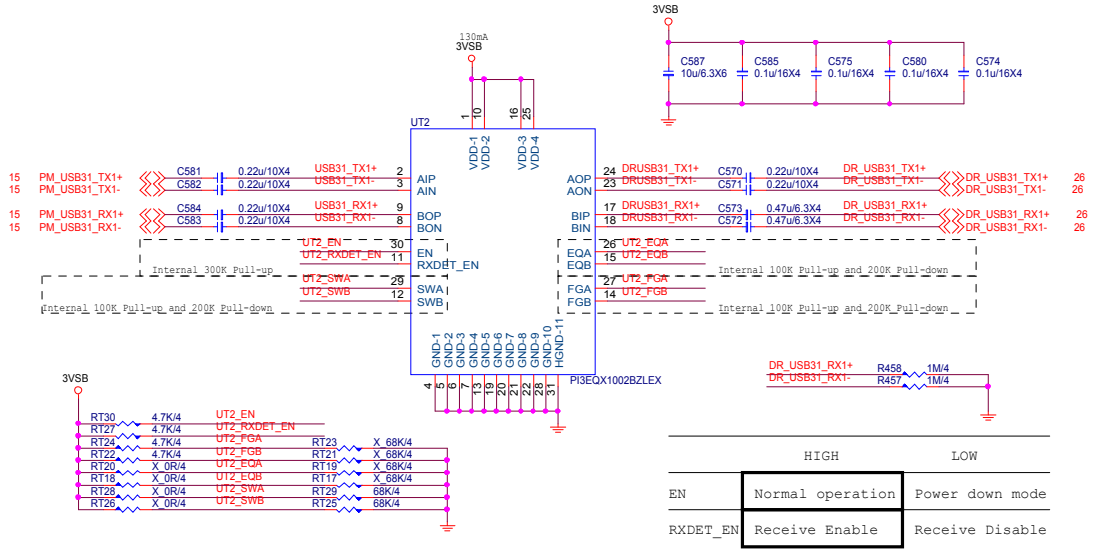


	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable



	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable

EQA/B are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B	*@2.5GHz*	*@5GHz*
0	5.1	10.9
R	1.9	6.7
F	3.5	8.9 (Default)
1	6.8	13.1

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

	Flat Gain Settings
FGA/B	*dB*
0	-3
R	-1.5
F	0 (Default)
1	+2

-1dB compression point linear Swing Setting:

SWA/B are the selection bits for the output linear swing setting

	Output Linear Swing Settings
SWA/B	*mVppd*
0	800
R	1200
F	1000 (Default)
1	1100

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Link to the Future

Title: USB 3.1 Gen2 redriver		
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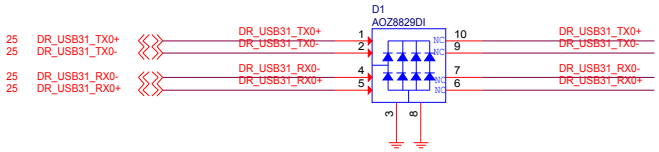

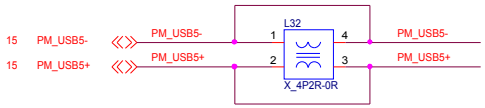

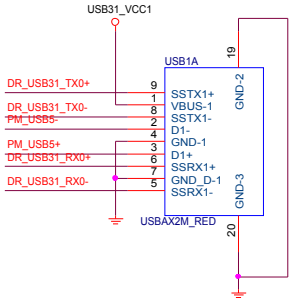

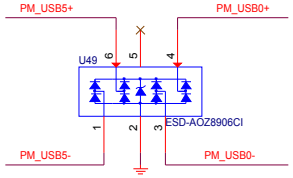

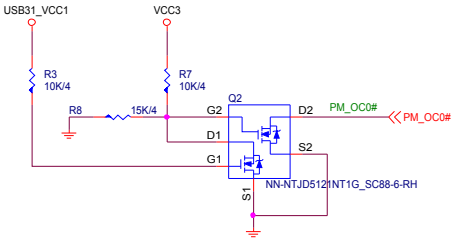

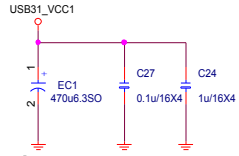

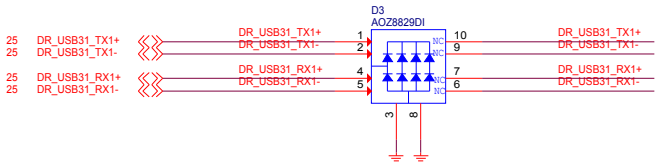

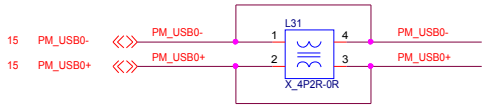

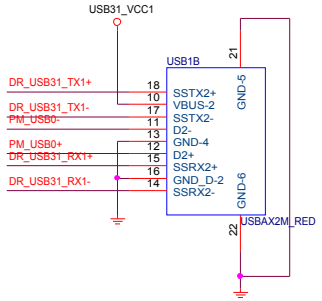

MICRO-STAR INT'L CO.,LTD.

Title: USB 3.1 GEN2 TYPE A*2

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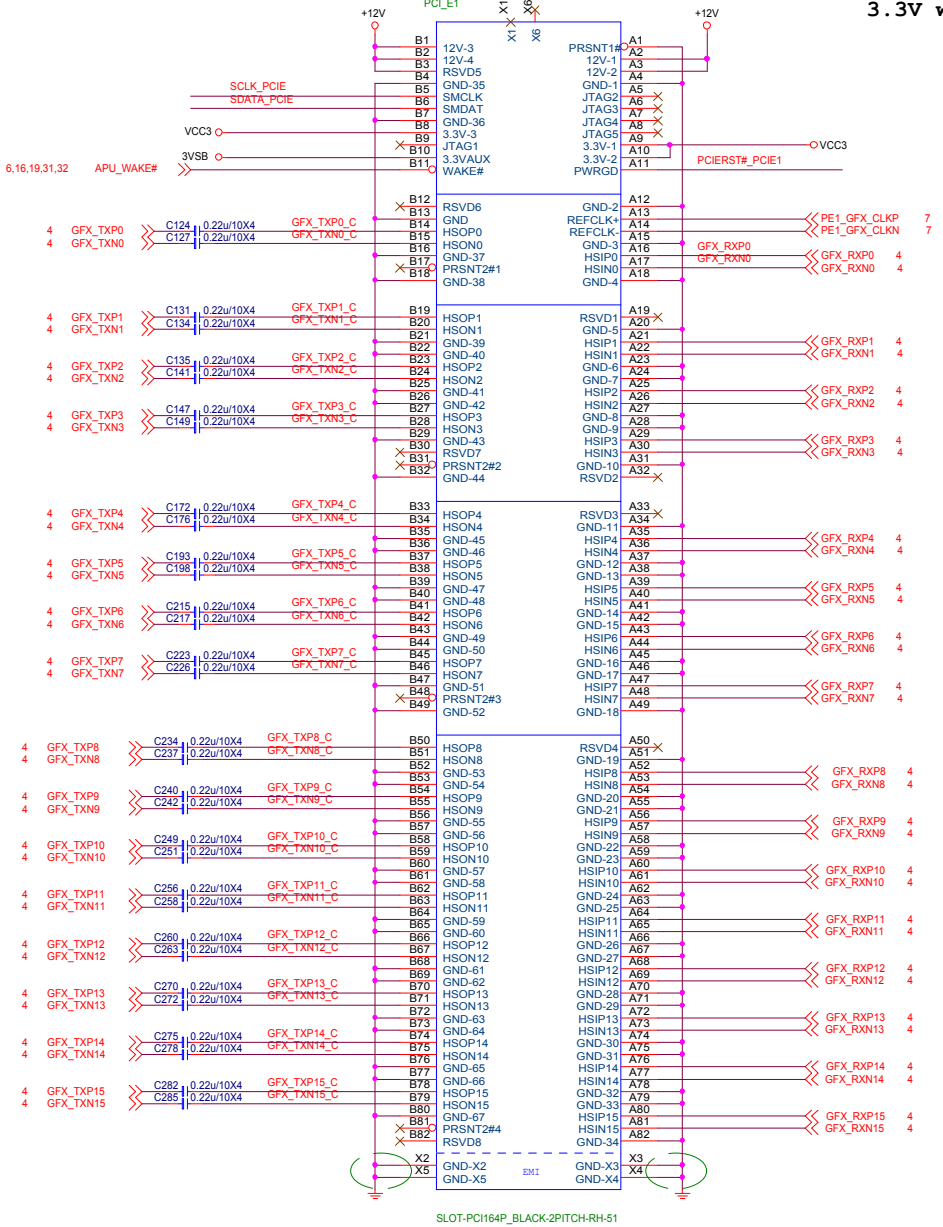
PCI EXPRESS x16 Slot

3.3V 3.0A
12V 5.5A

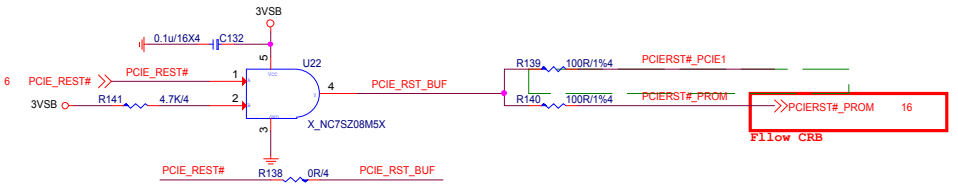
PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V 3.0A
12V 0.5A

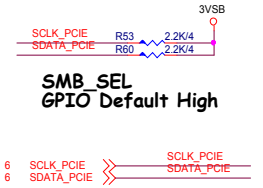


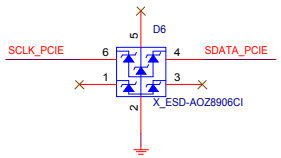
Remove PCIe x1 Slot

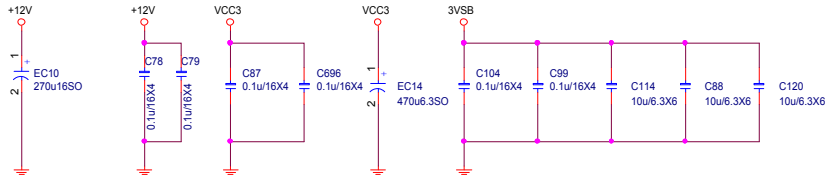
within 500mil



SMBus separate circuit







MICRO-START INT'L CO.,LTD.

Title	PCIE X16 SLOT	
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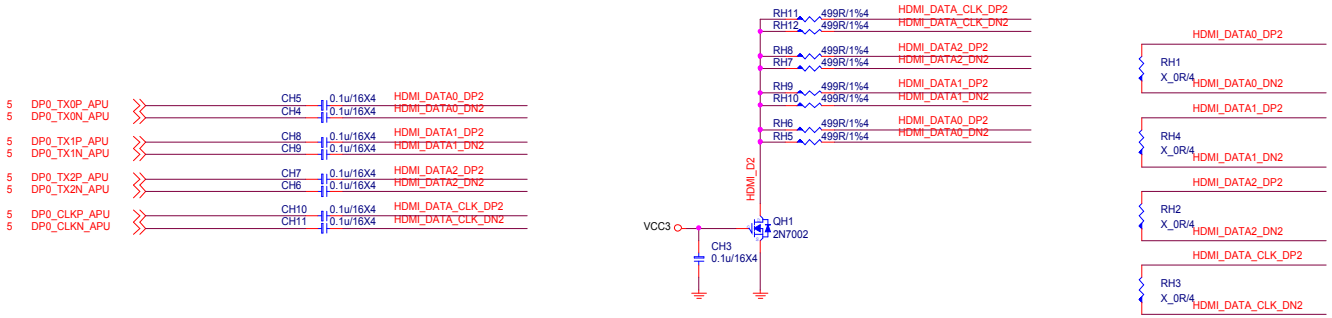
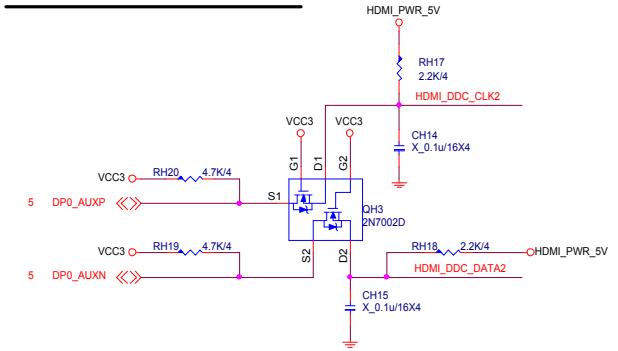
HDMI CONNECTOR

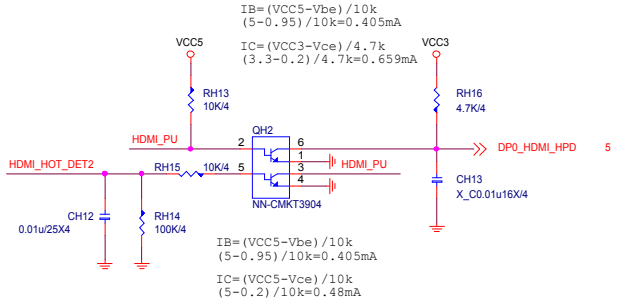
For HDMI 1.4



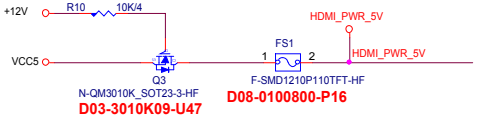
AUX Level Shifter



HPD Circuit

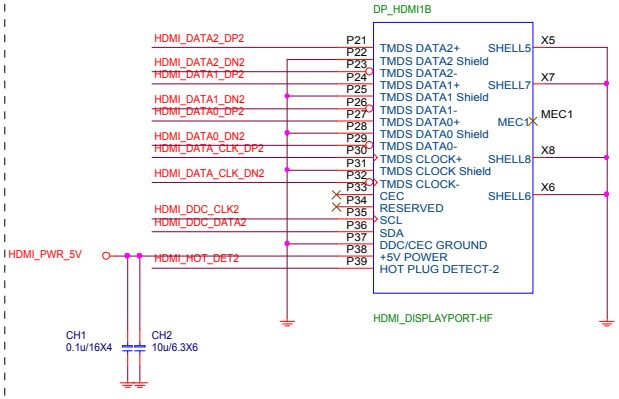


Connector Power

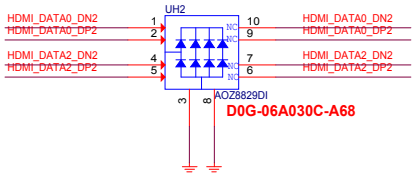


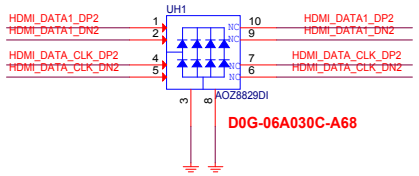
如果用DIODE SA測試電壓會不過

Connector

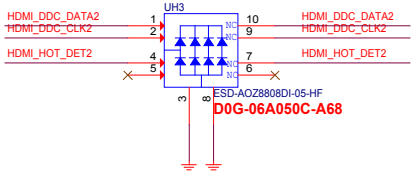


For EMI





注意:耐壓5V零件



MSI MICRO-STAR INT'L CO.,LTD.

Link to the Future

Title: HDMI Connector		
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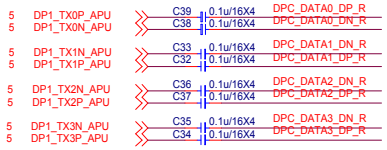
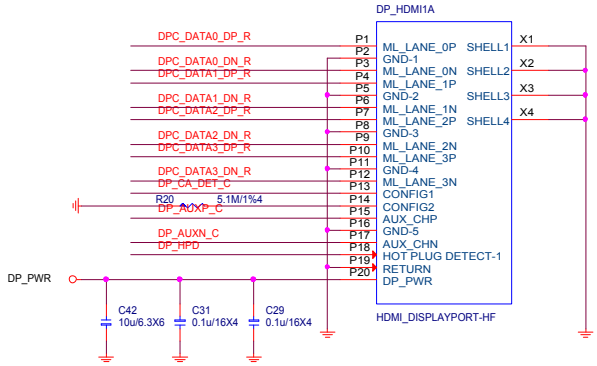
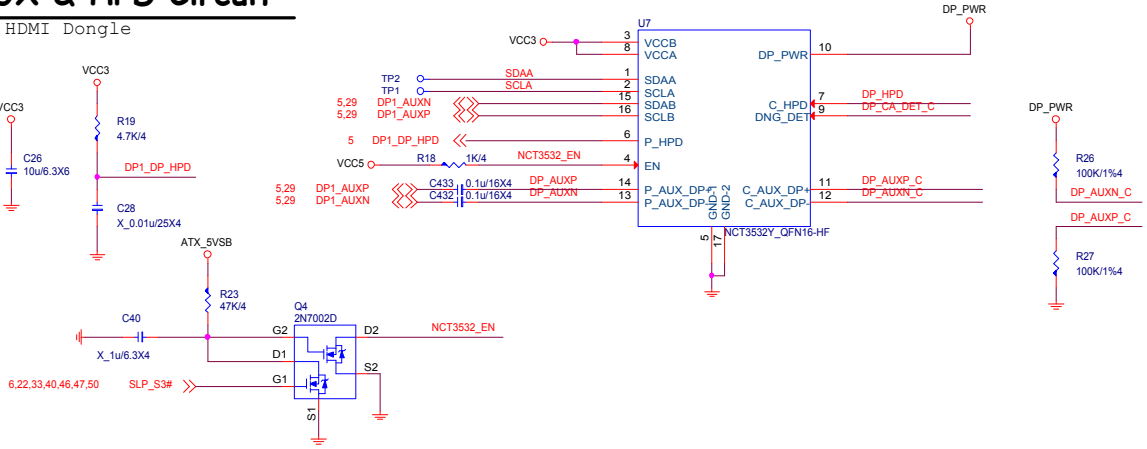
DP CONNECTOR



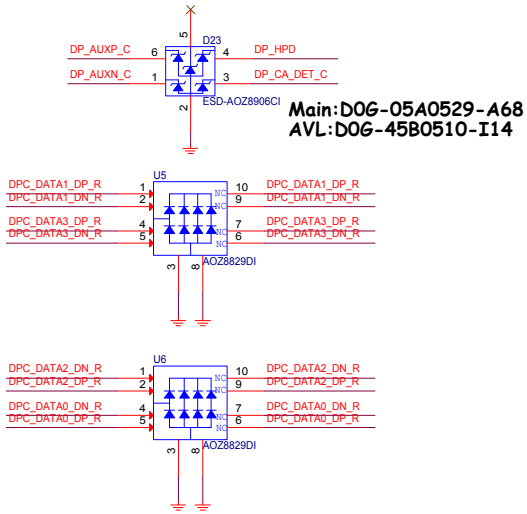


DP AUX & HPD Circuit

Support HDMI Dongle



ESD



MICRO-START INT'L CO.,LTD.

Title: DP Connector

Size	Document Number	Rev
Custom	MS-7A40	11

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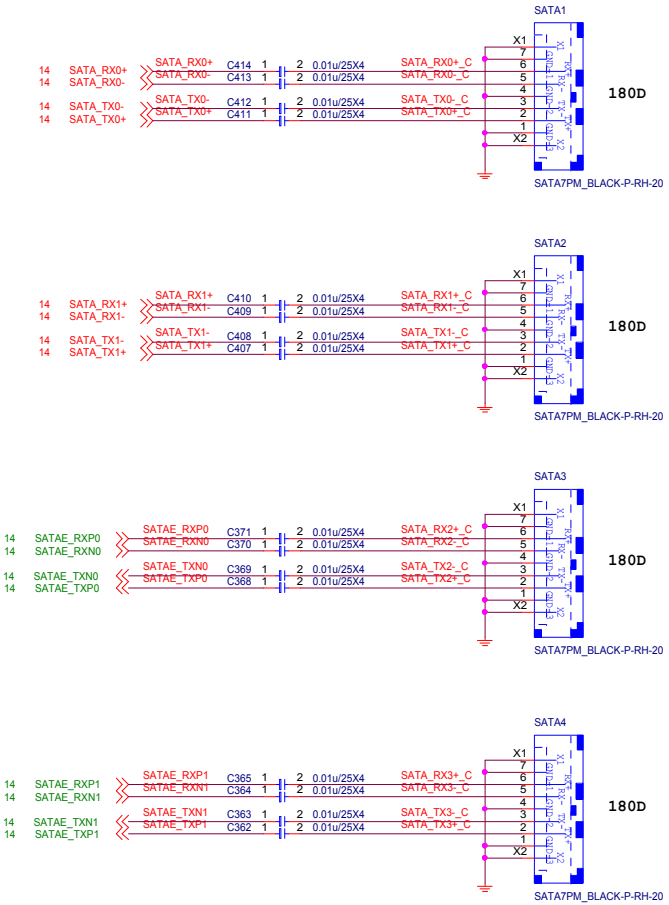
SATA Connector



Title	SATA Connector
Size	Custom
Document Number	MS-7A40
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Date:	Thursday, November 02, 2017
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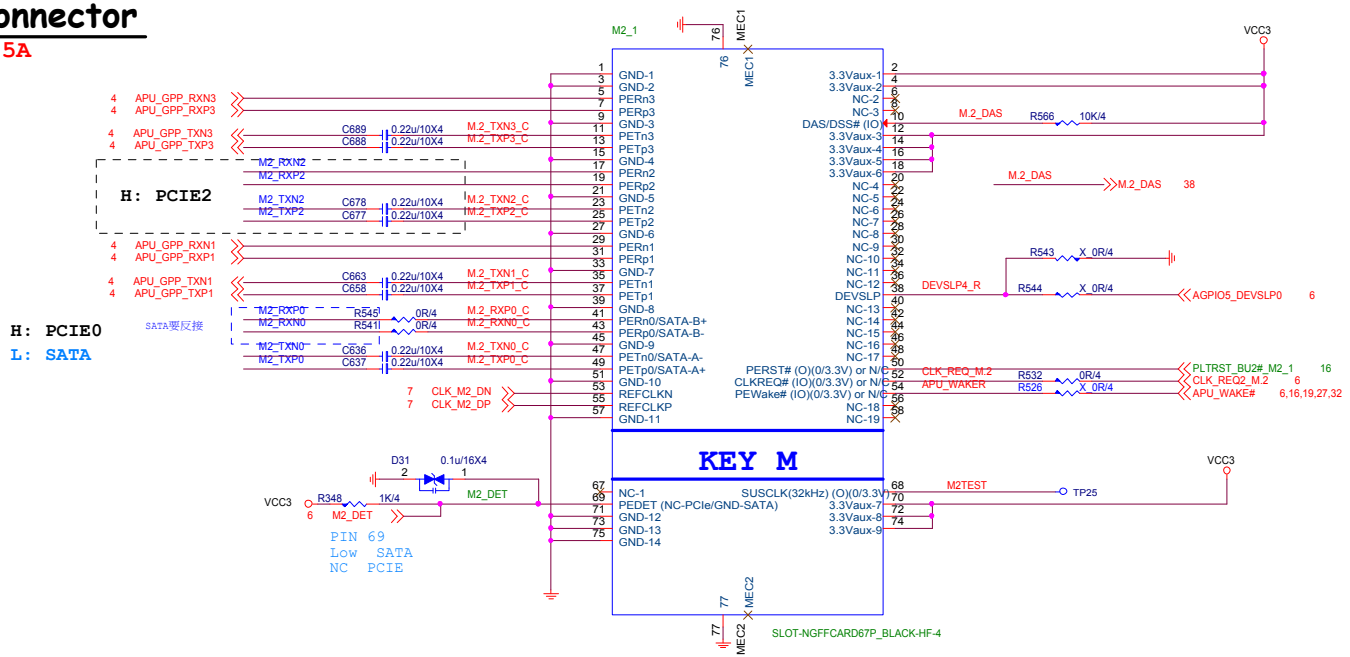
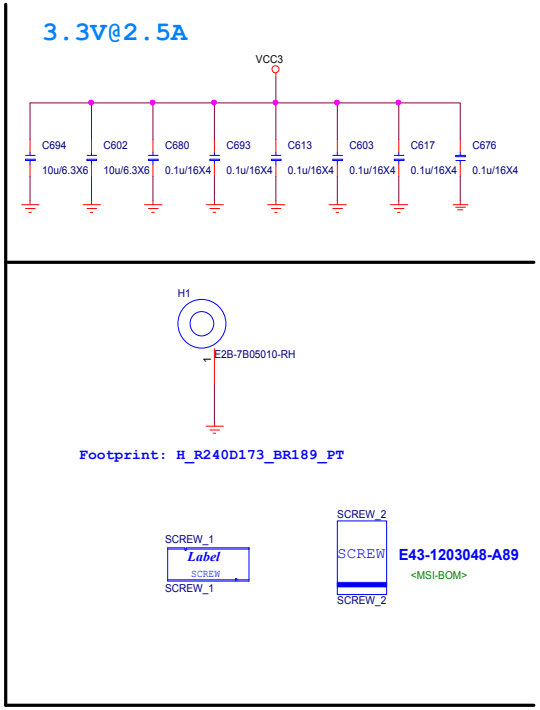
MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

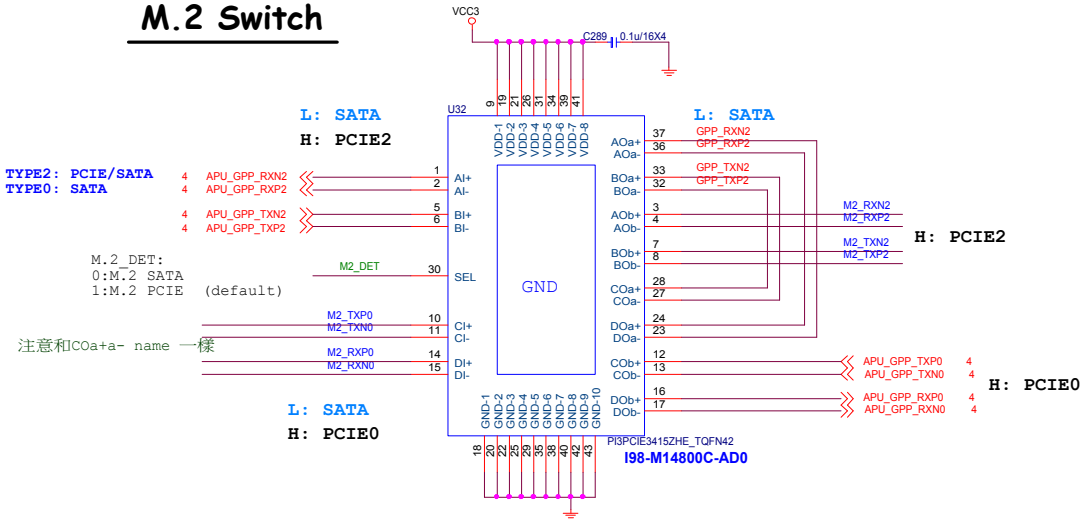
M.2 Connector

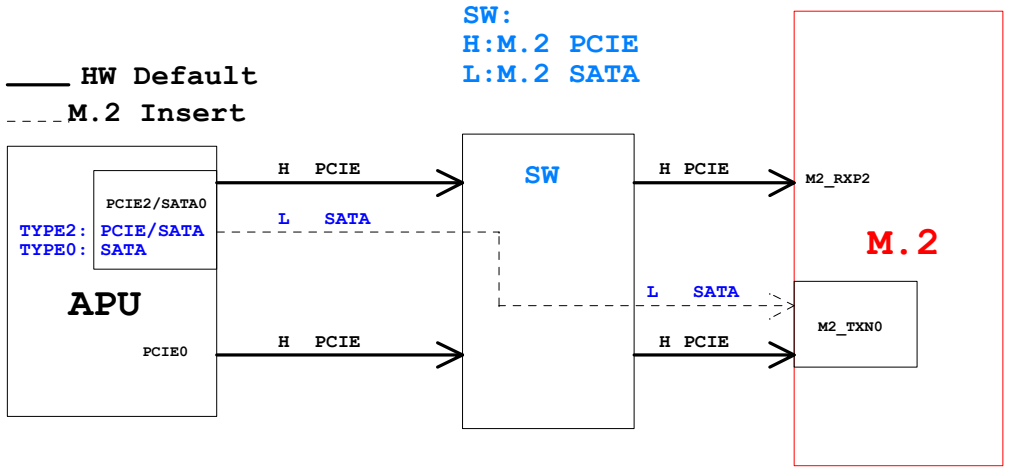
3.3V@2.5A





M.2 Switch





MSI MICRO-STAR INTERNATIONAL — Link to the Future — MICRO-START INT'L CO.,LTD.			
Title: M2_1			
Size: Custom	Document Number: MS-7A40		Rev: 11
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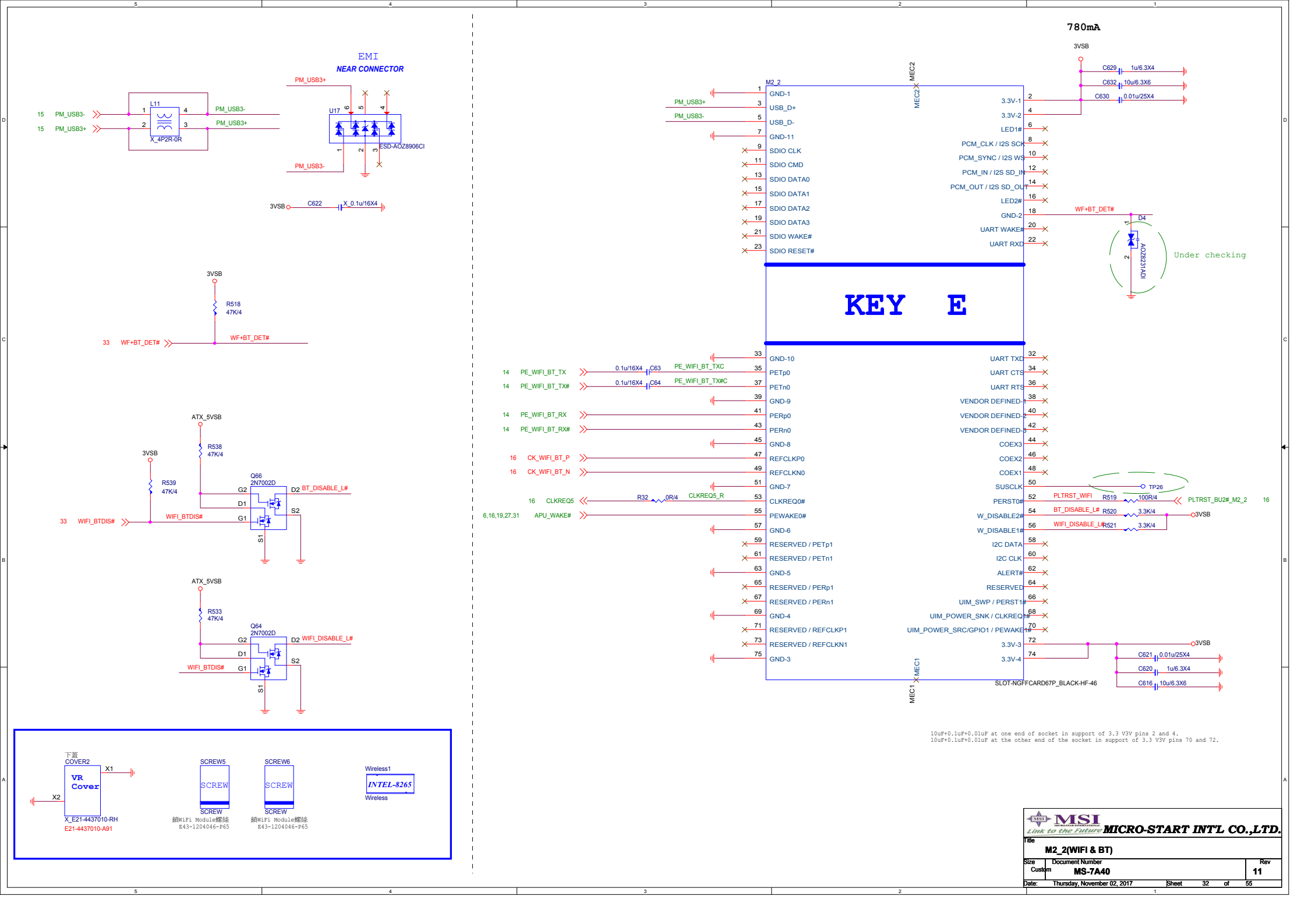

MICRO-START INT'L CO.,LTD.

Title: M2_2(WIFI & BT)

Size: Custom | Document Number: MS-7A40 | Rev: 11

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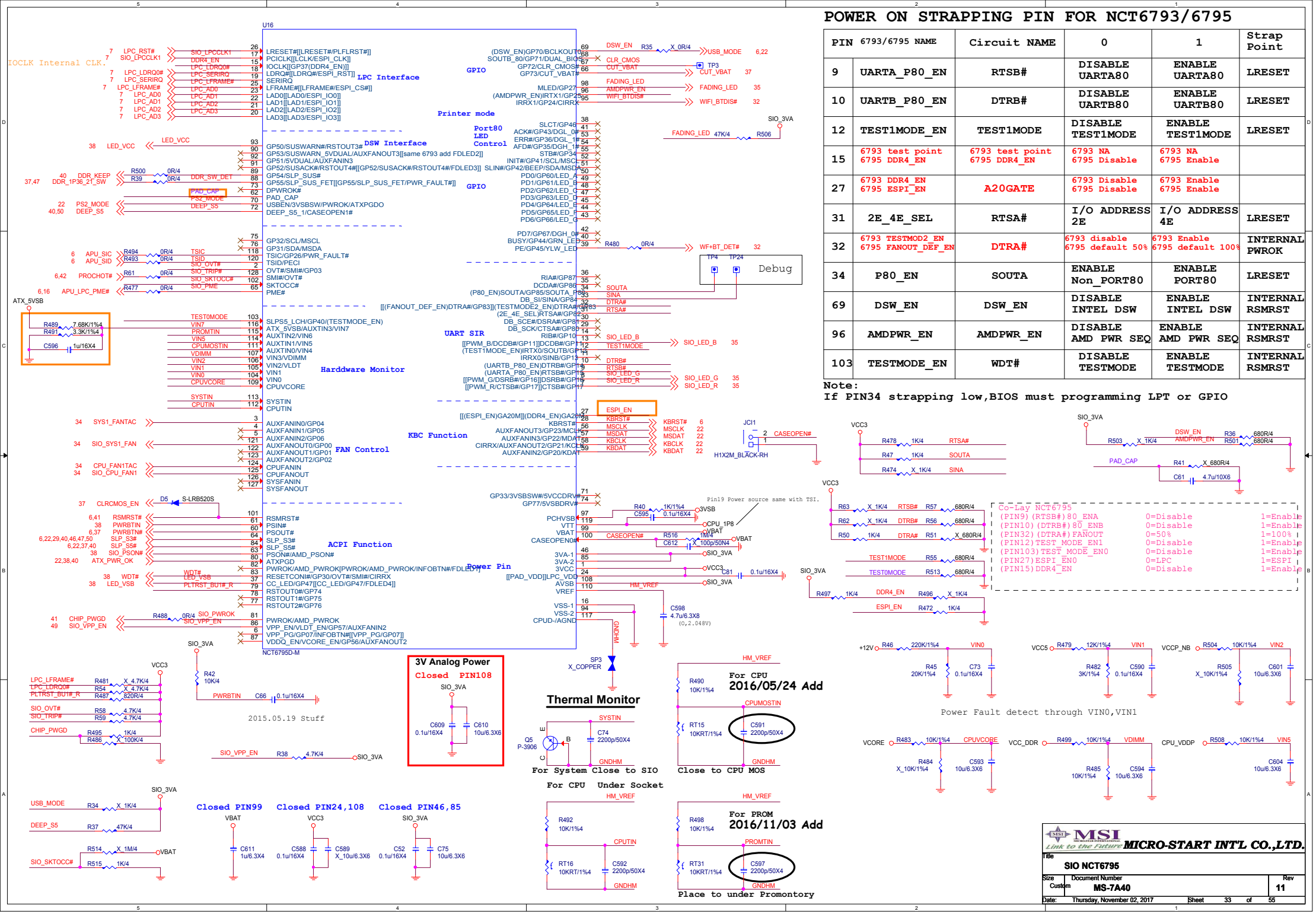

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

MICRO-START INT'L CO.,LTD.

Title	SIO NCT6795		
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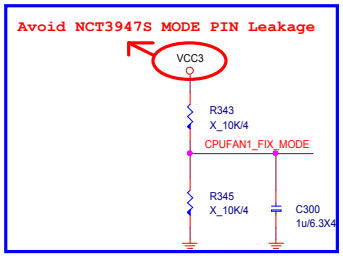
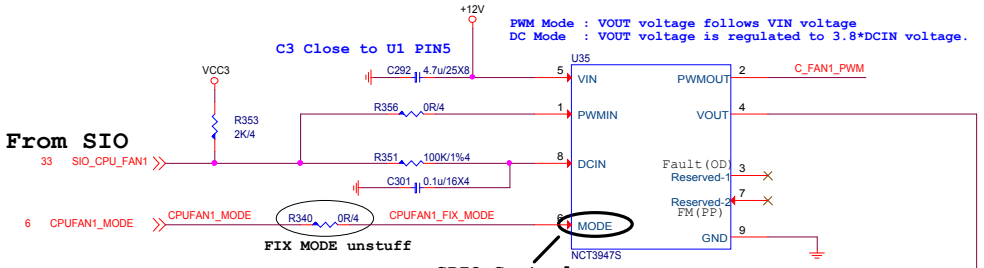
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切換 PWM/DC MODE

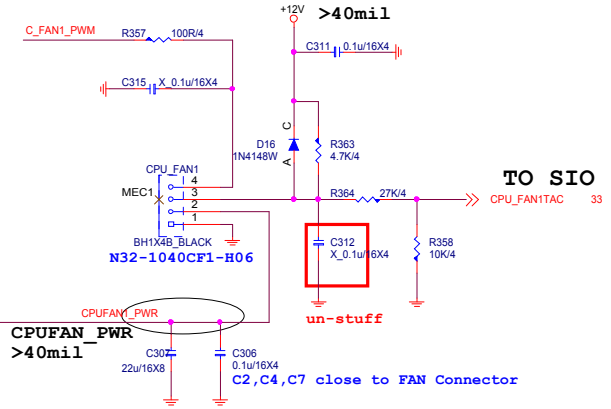


Resever For FIX DC or PWM MODE USE By PM SPEC

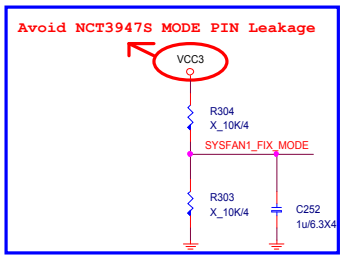


	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

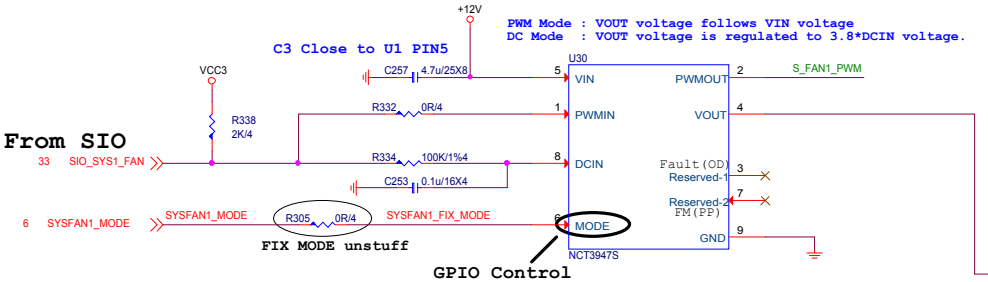
Internall pull up 1.65V



CPUFAN_PWR >40mil

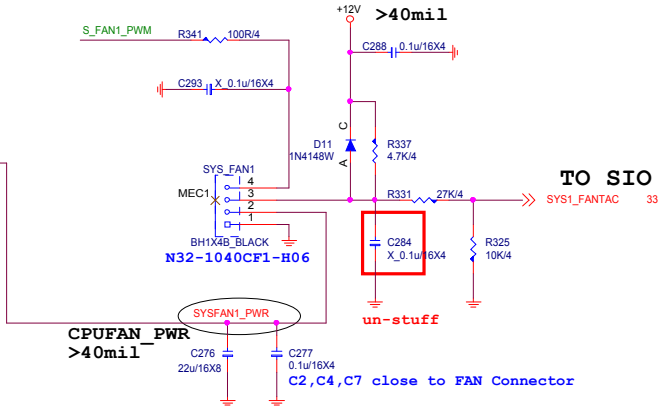


Resever For FIX DC or PWM MODE USE By PM SPEC



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



CPUFAN_PWR >40mil

MICRO-START INT'L CO.,LTD.

Title: CPU/SYS FAN Control TYPE K

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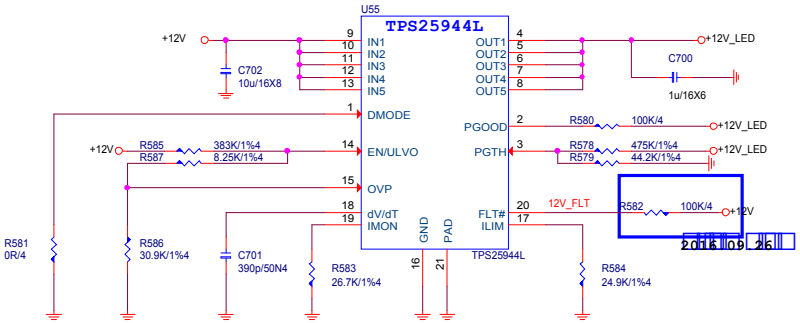
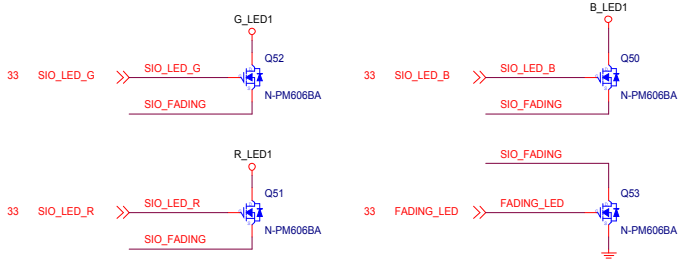
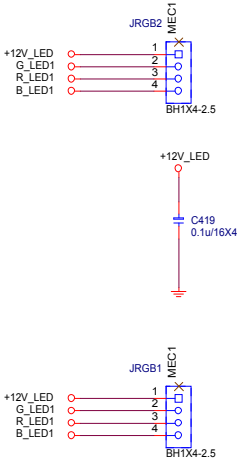
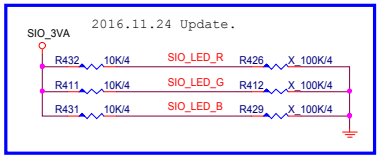
定義:外接LED 燈條
---- 彩色 : SIO 6795D-M(128pin) : OB2-7A58001
---- 單色 : SIO 5565(64pin) : B02-5565D04-N62
---- PCB 文字面 (JLED)
---- 手冊 註明接頭支援標準 5050 RGB or 單色 LED 共陽燈條 (12V+/G/R/B) or (12V+/-/S/-) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JLED



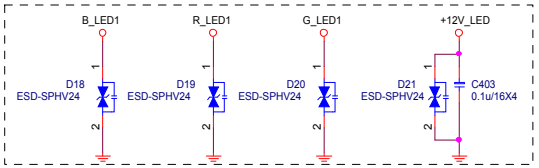




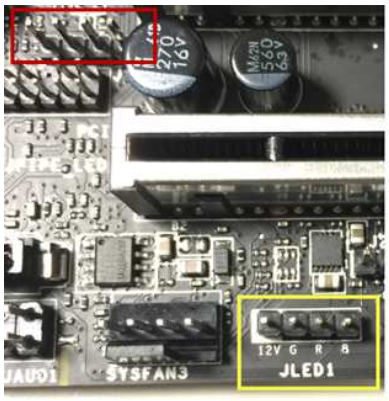


Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

2016.08.31 StuFF

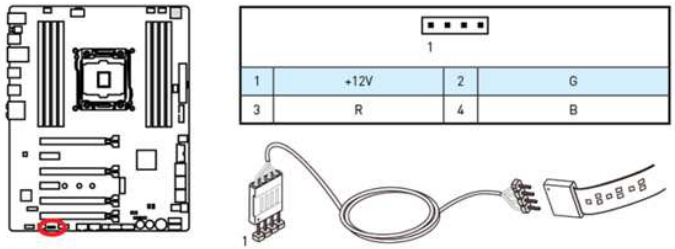


close to JLED2



JLED1: RGB LED connector

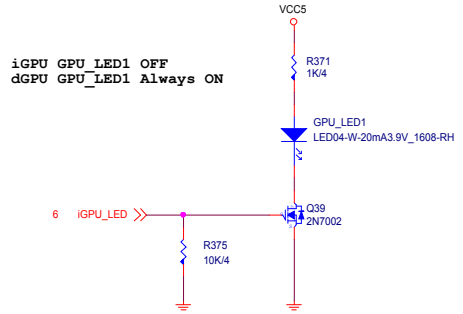
This connector allows you to connect the RGB LED strip.



Important

- *This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.*
- *Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.*
- *Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.*

AM4 APU Detect LED Circuit



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	6795 RGB LED	
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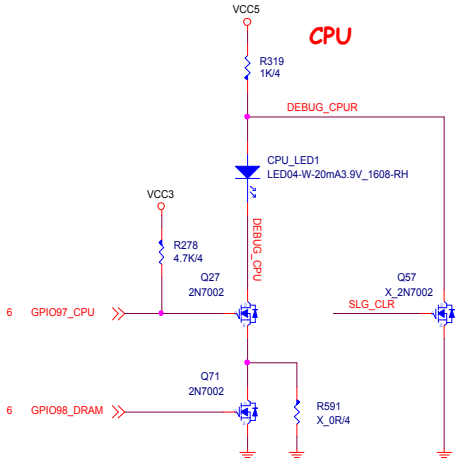
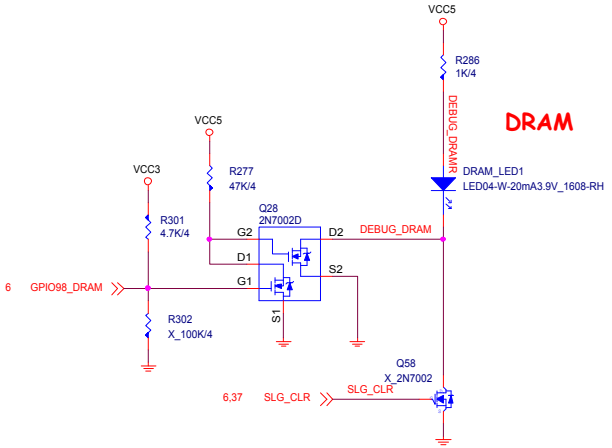
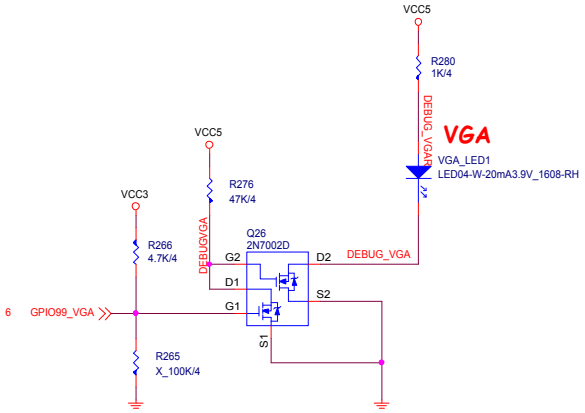
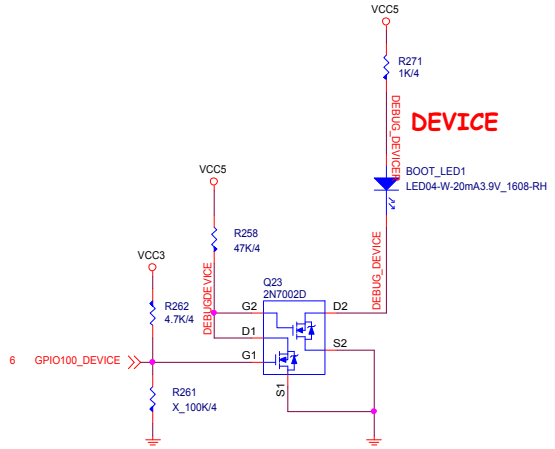
EZ Debug LED









LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

MSI MICRO-STAR INT'L CO.,LTD.
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Title	EZ Debug LED	
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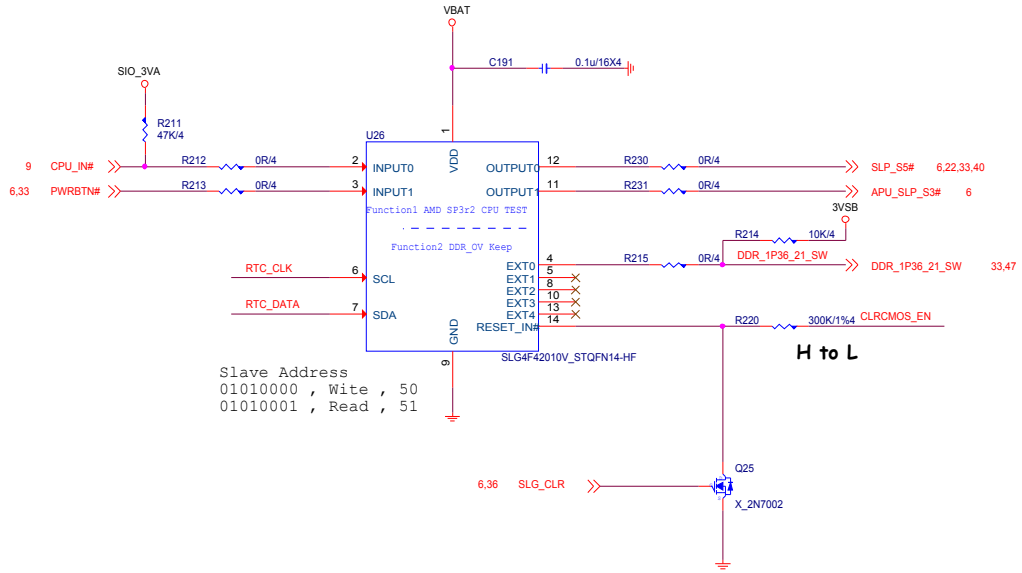
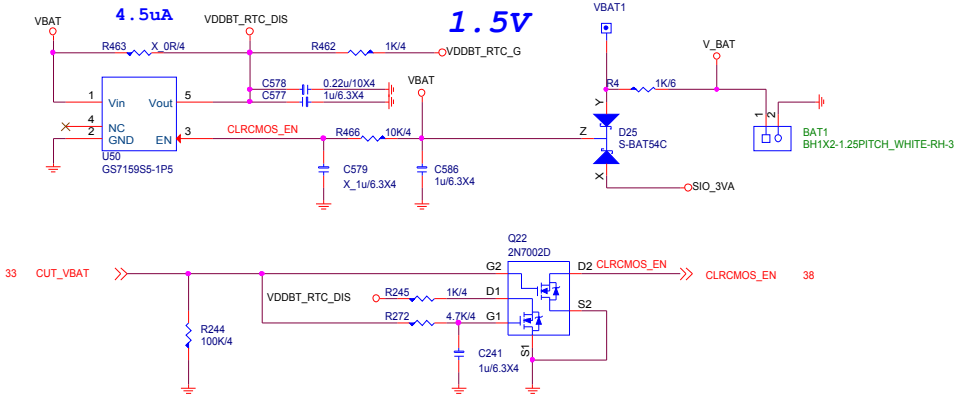
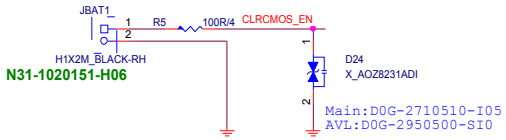
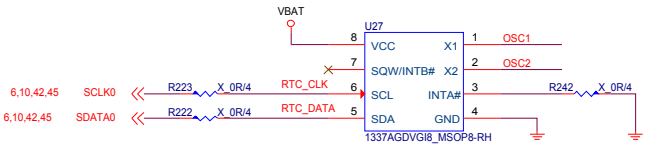


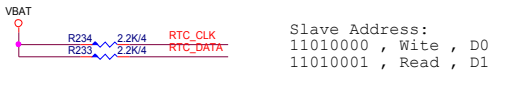
RTC & Clear CMOS Circuit

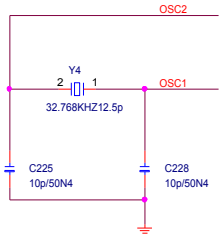
Placement Bottom Side

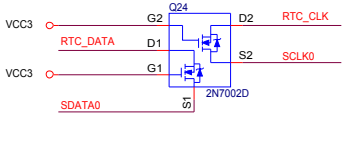












MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	RTC Circuit / Moat Cap		
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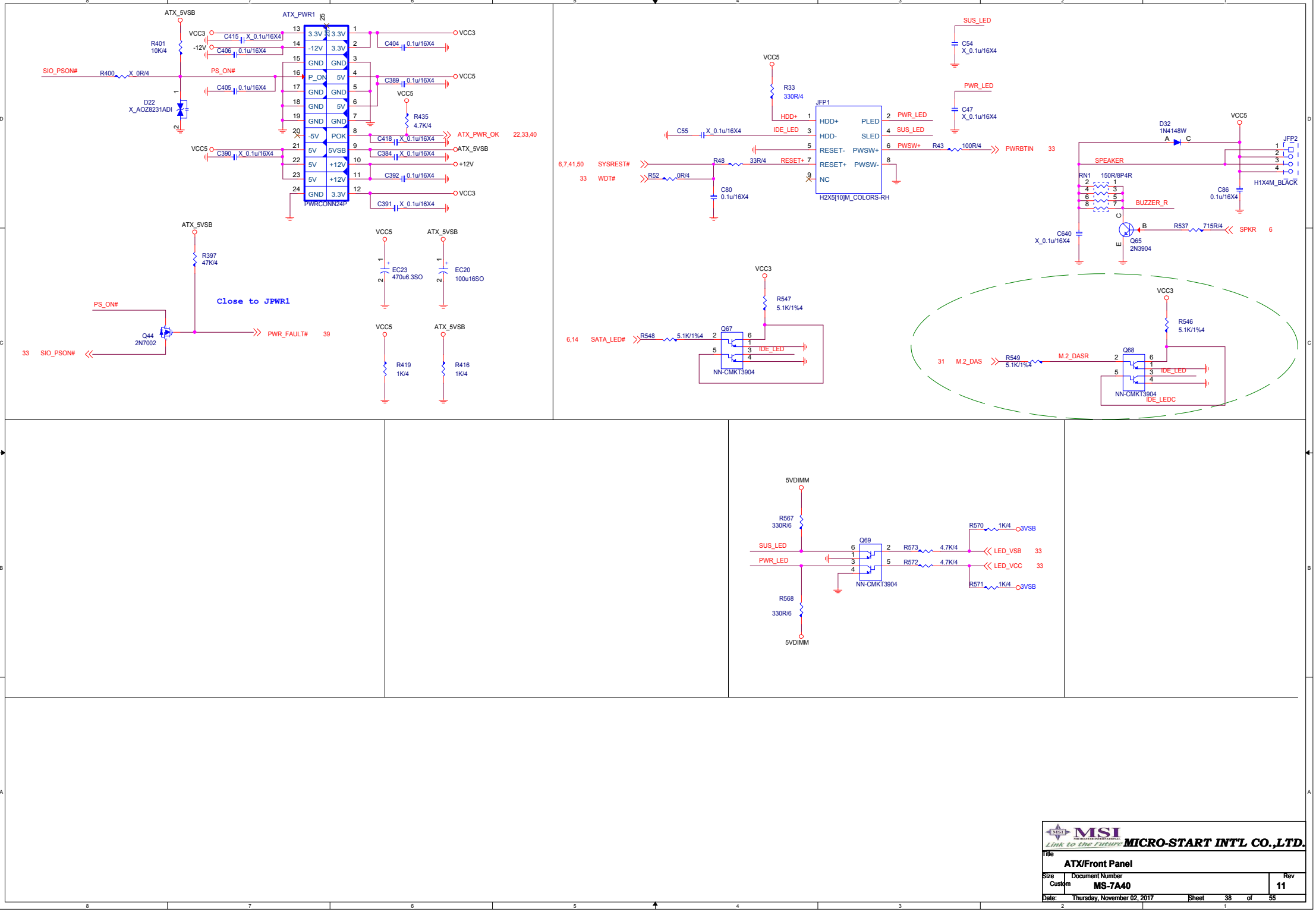

MICRO-STAR INT'L CO.,LTD.

Title: ATX/Front Panel

Size: Custom | Document Number: MS-7A40 | Rev: 11

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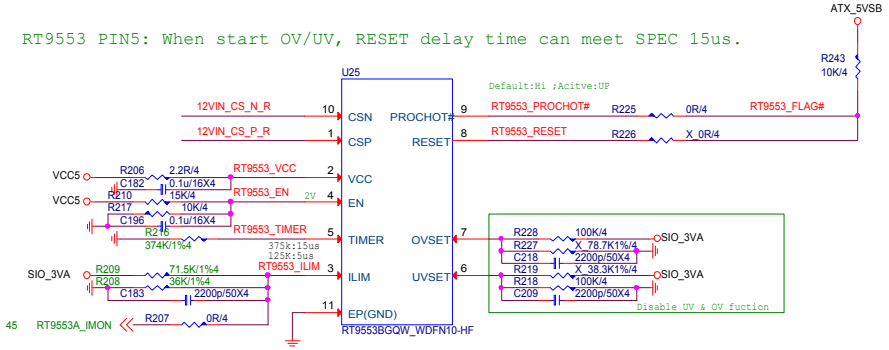
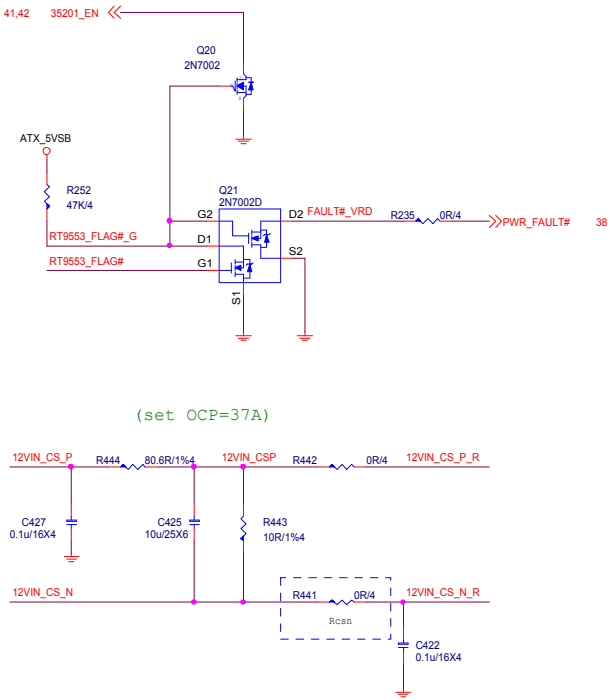
RT9553B CURRENT SENSE

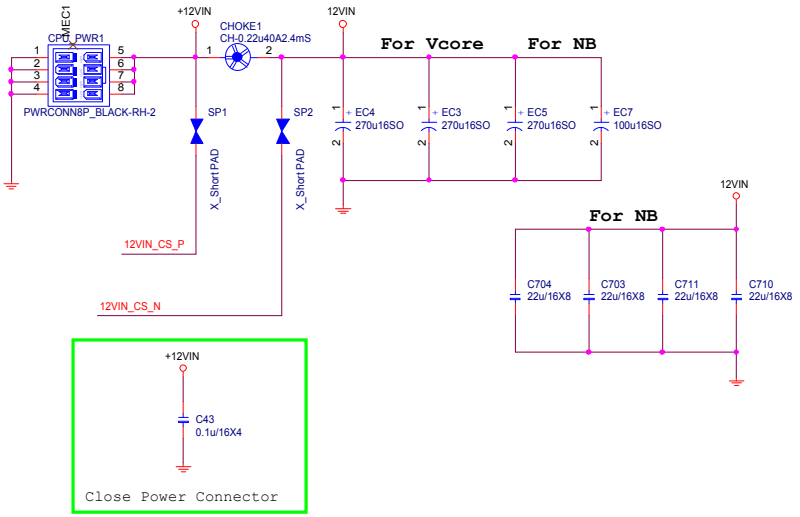
VCORE EDC MAC 125A

NB EDC MAX75A





CPU POWER CONNECTOR



D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.5	> output Vcore
D	=	0.125	

I o = Icore(max)*0.8			
I core(max)	=	125	> Vcore current
I avg.	=	100	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	4 ~~6~~	phase
I ripple	=	~~9.26/0.73~~	A

5.511982

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

CORE:
D = Vout/Vin
= 1.5/12
= 0.125
N = 6
Irms = Iout * [D/N - (D)^2]^(1/2)
= 125 * (0.02083 - 0.015625)^(1/2)
= 9.0182A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.2	> output Vcore
D	=	0.1	

I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	9	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

NB:
D = Vout/Vin
= 1.2/12
= 0.1
N = 2
Irms = Iout * [D/N - (D)^2]^(1/2)
= 75 * (0.05 - 0.01)^(1/2)
= 15A

MICRO-START INT'L CO.,LTD.

Title: RT9553 CURRENT SENSE

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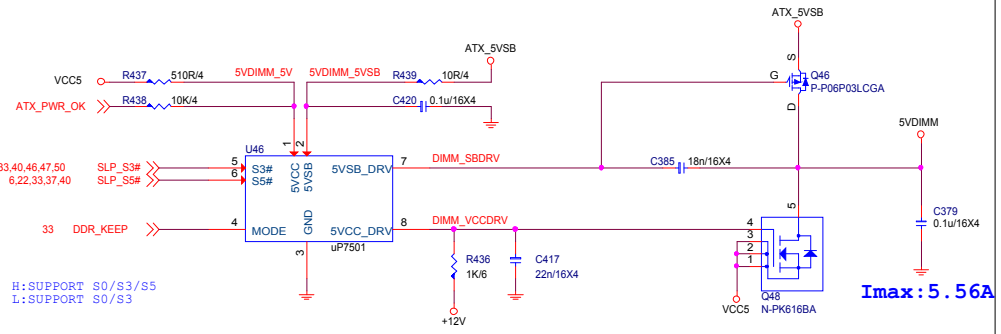
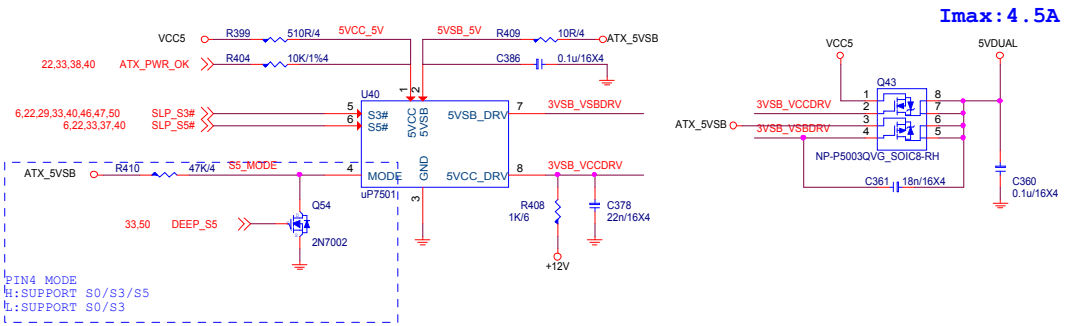
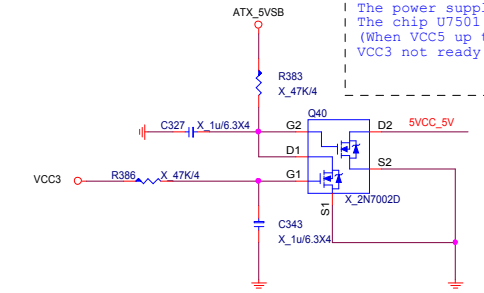
5VDIMM FOR DDR



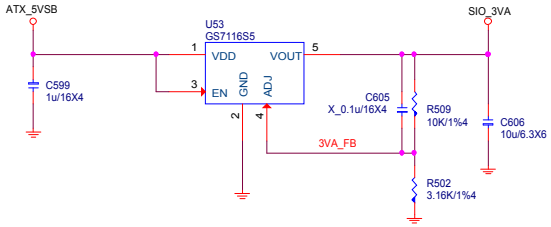
5VDUAL For 3VSB、CPU 1.8V 、 VDDP



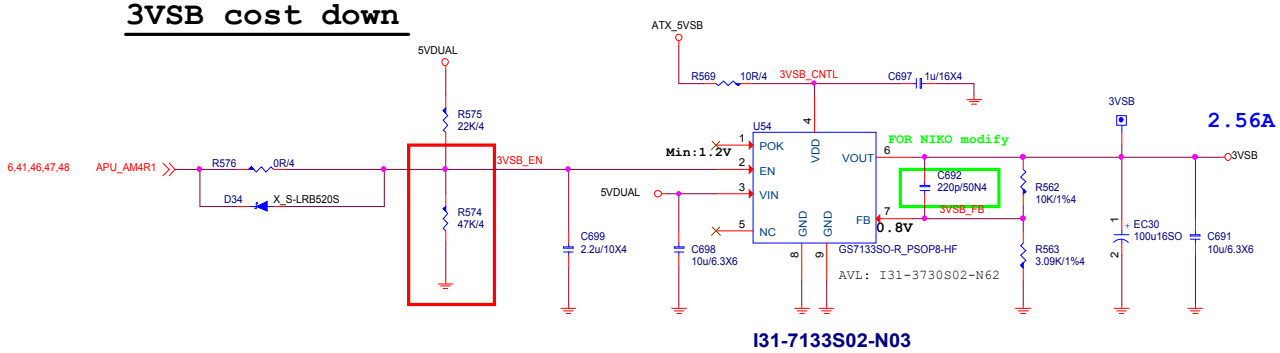
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



SIO_3VA



3VSB cost down



MICRO-STAR INT'L CO.,LTD.

Title: ACPI uPI-5VDIMM&3VSB

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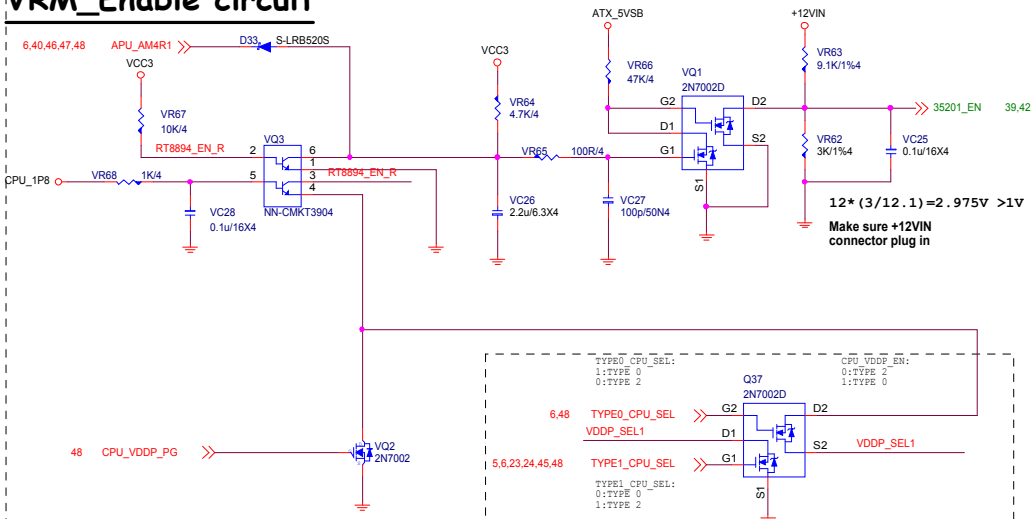
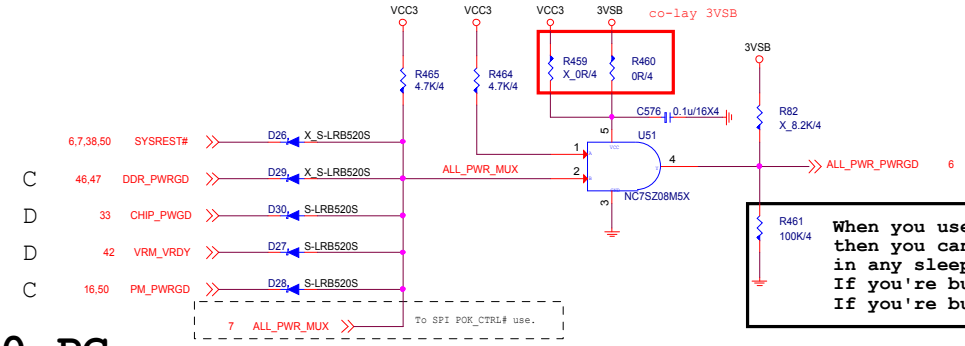
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

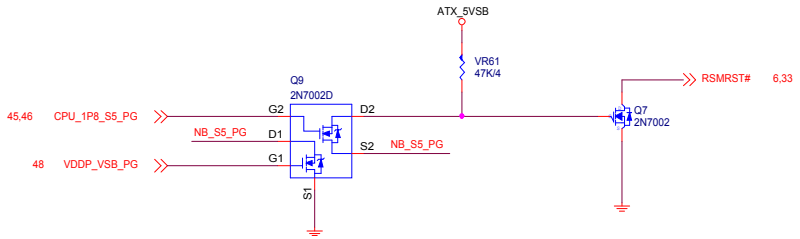
ALL POWER GOOD MUX



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



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Link to the Future

Title	PWR Sequence	
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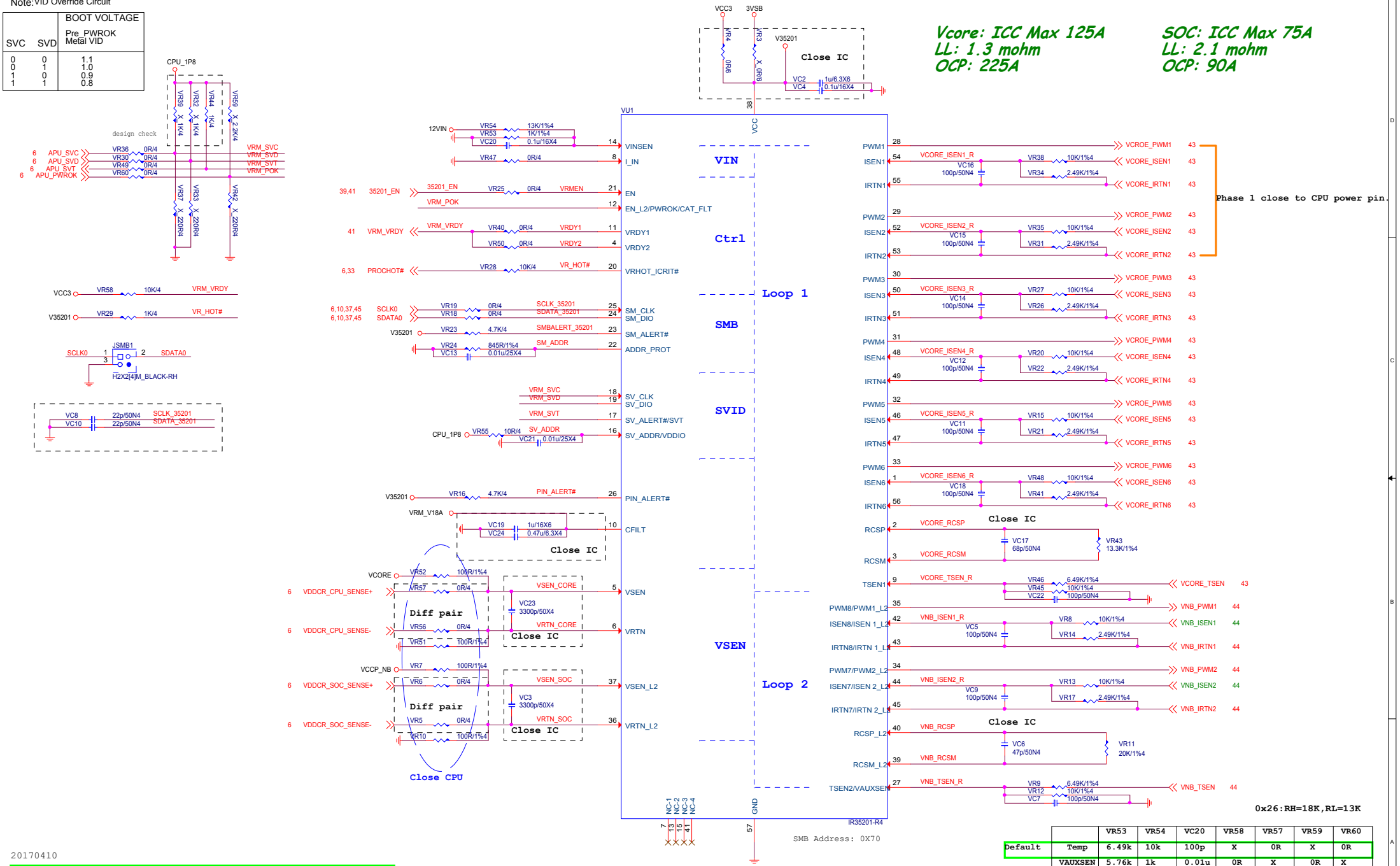
Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

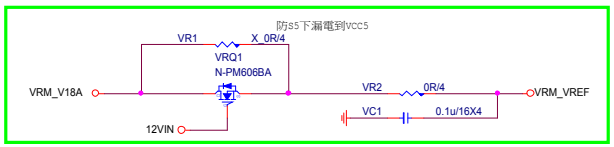
Vcore: ICC Max 125A
LL: 1.3 mohm
OCP: 225A

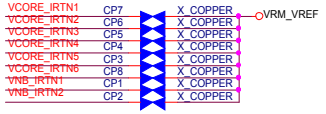
SOC: ICC Max 75A
LL: 2.1 mohm
OCP: 90A



		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

20170410





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Title: CPU Power IR35201 6+2 Phase

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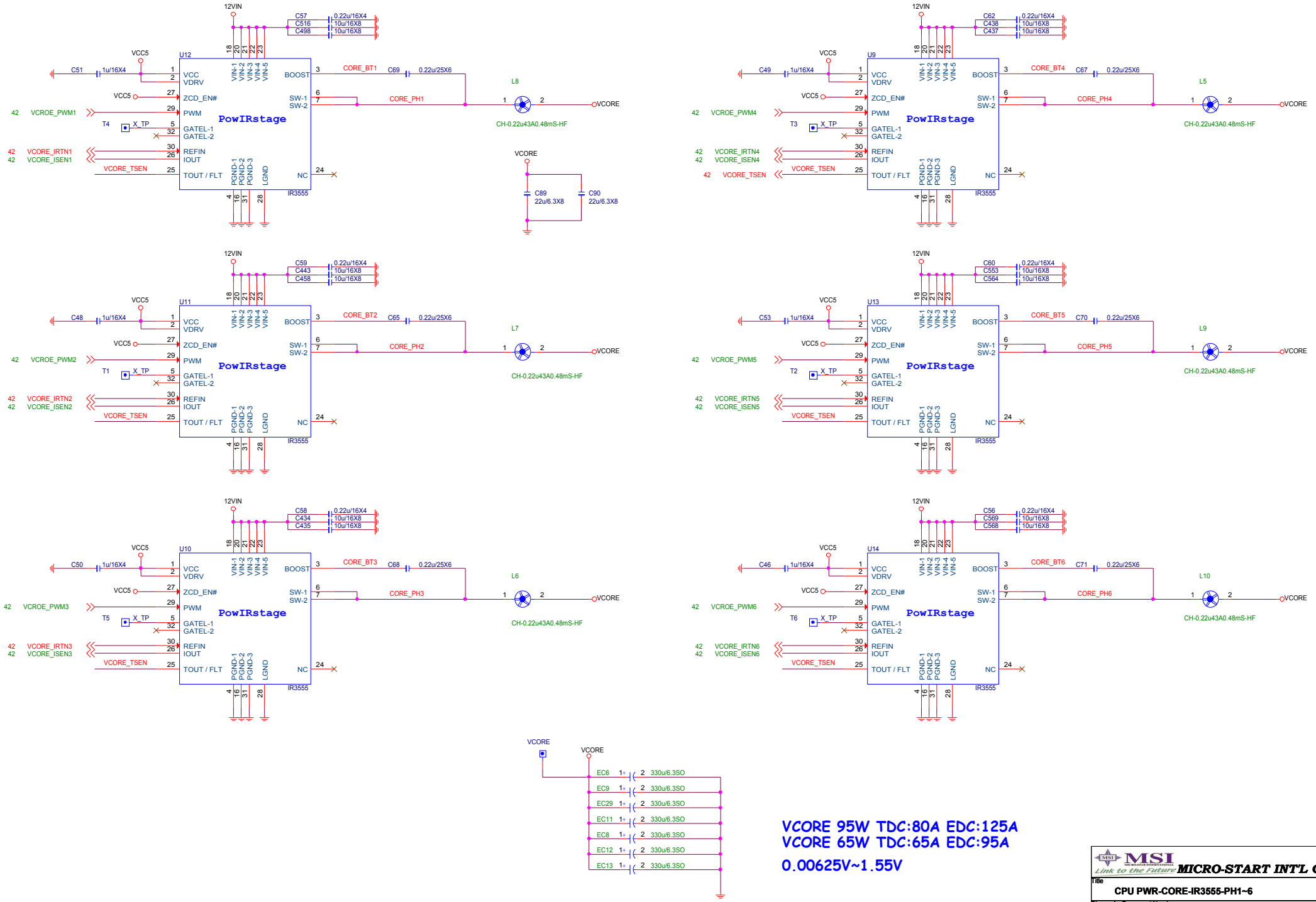

VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

0.00625V~1.55V

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Title: CPU PWR-CORE-IR3555-PH1~6

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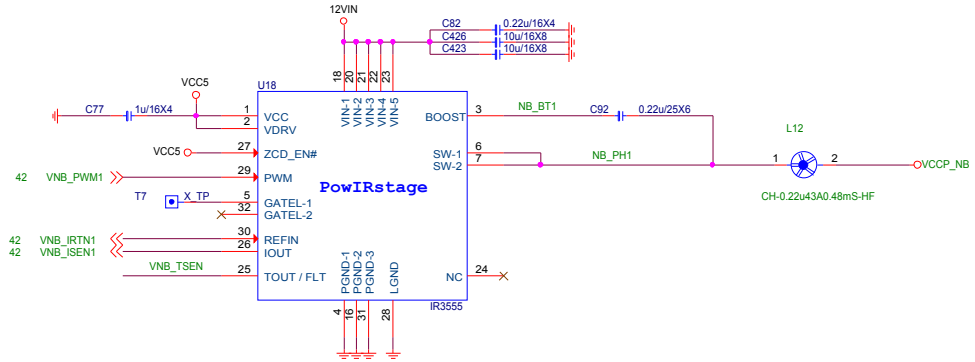
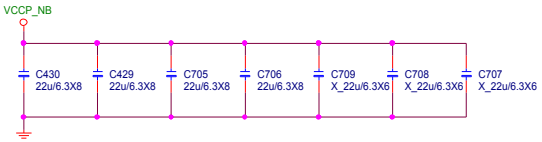
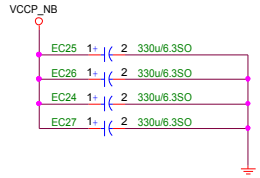
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

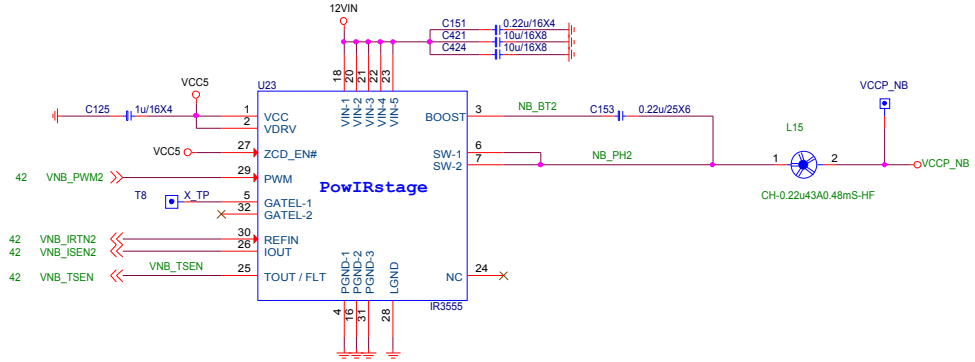
VCCP_NB OCP:100A



0.00625V~1.55V







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Title: CPU Power NB Phase 1-2		
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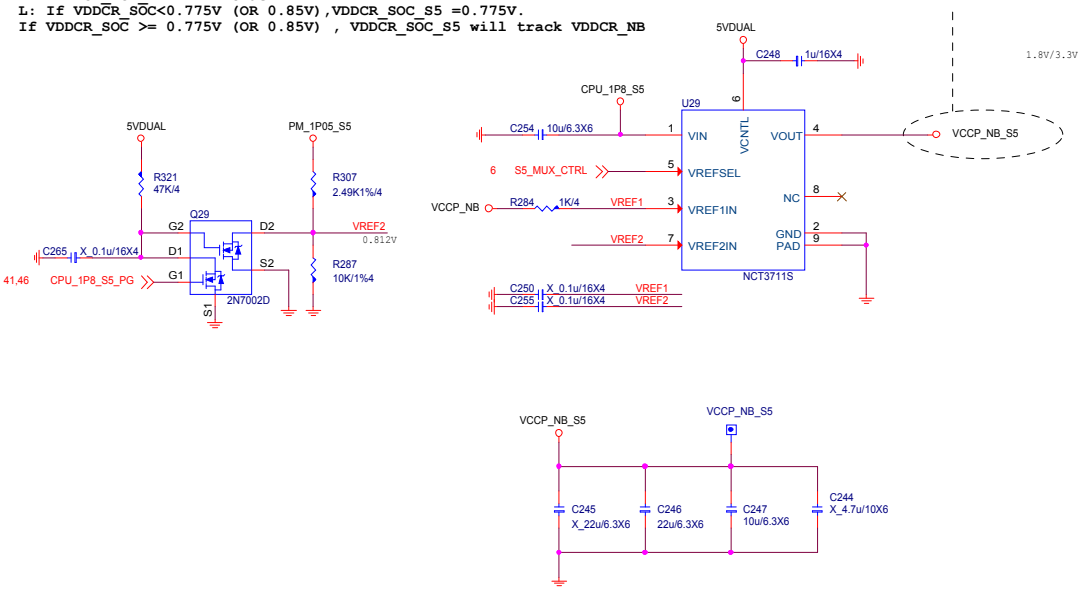
FOR
VCCP_SOC_s5
0.9A

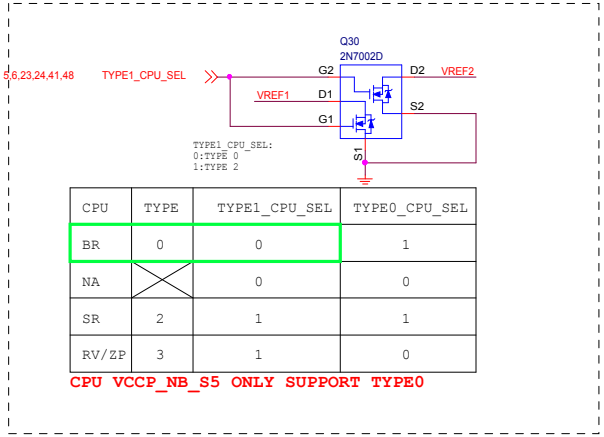
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0



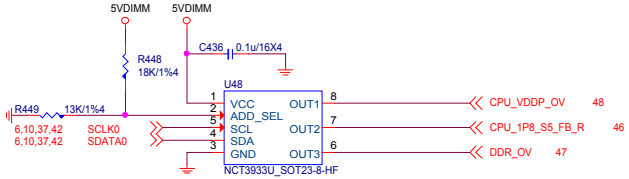


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

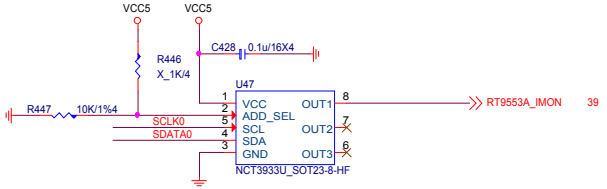
CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

0x26:RH=18K,RL=13K



0x2A:RH=OPEN,RL=10K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Title	CPU Power NB Switch/NCT3933	
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FOR CPU 1.8V S5

0.5A

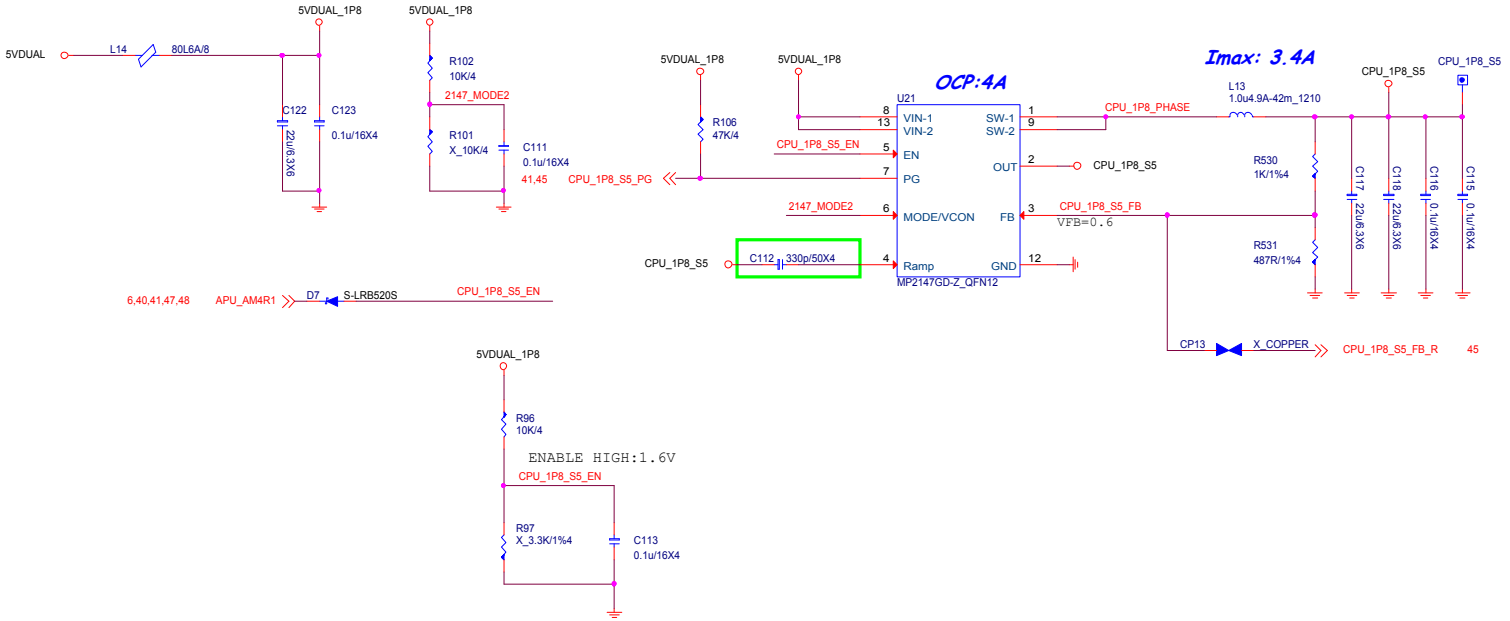
FOR VCCP_SOC_S5

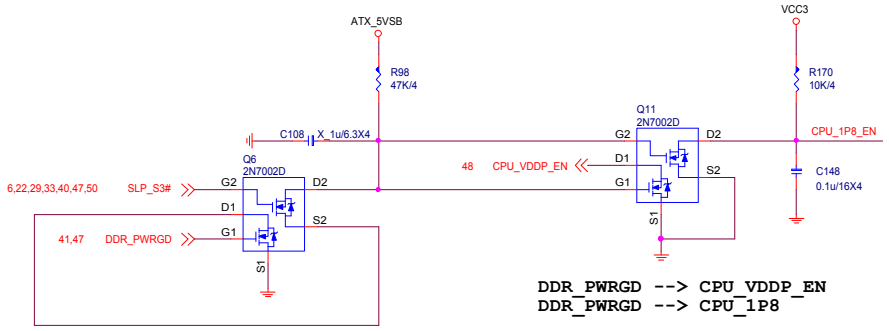
0.9A

FOR CPU 1.8V S0

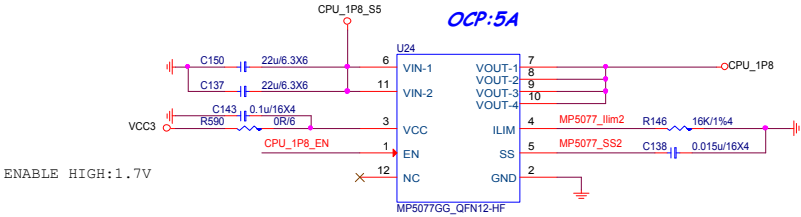
2.0A

0.5A + 2.0A + 0.9A =3.4A





DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



ENABLE HIGH:1.7V

```
Ilimit=(1/Rlimit)*S,S=80000,when VIN=1.8V
=(1/16)*80000=5.0375A

Tss=(1/3)*((Vout*Css)/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n)/9uA)=1mS
```

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Title	CPU Power 1P8V-MP2147	
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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM
0.6A FOR DDR VTT

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675 for 1.232V
L	0.75 for 1.369V

Imax: 20.85A

OCP:24A

By layout modify

f:400KHz

R178=90.9K for OCP(dc)=24A (typ)
and OCP(dc)=23.8A(min)

27.5A

FB:0.75V

I32-8231A0C-R11

default=1.36V

R195=1K, R181=1.21K,
Vo=0.75V*(1+R195/R181=1.369V

Close to PIN19

1.1uH change to 0.47uH

1.2V

0.1uFx1 per dimm

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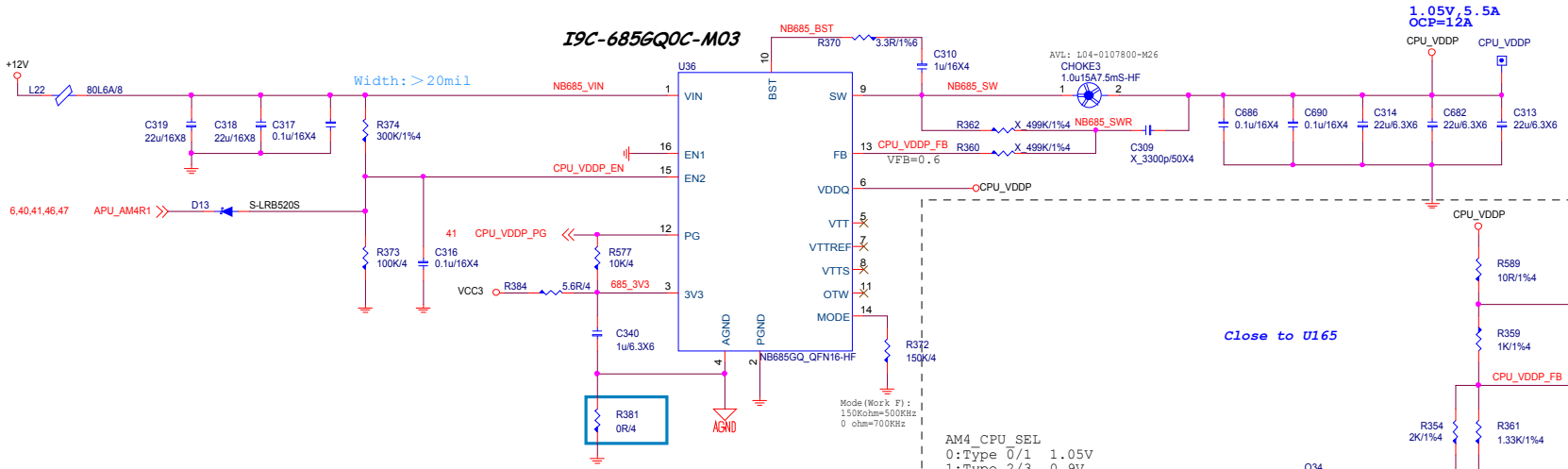
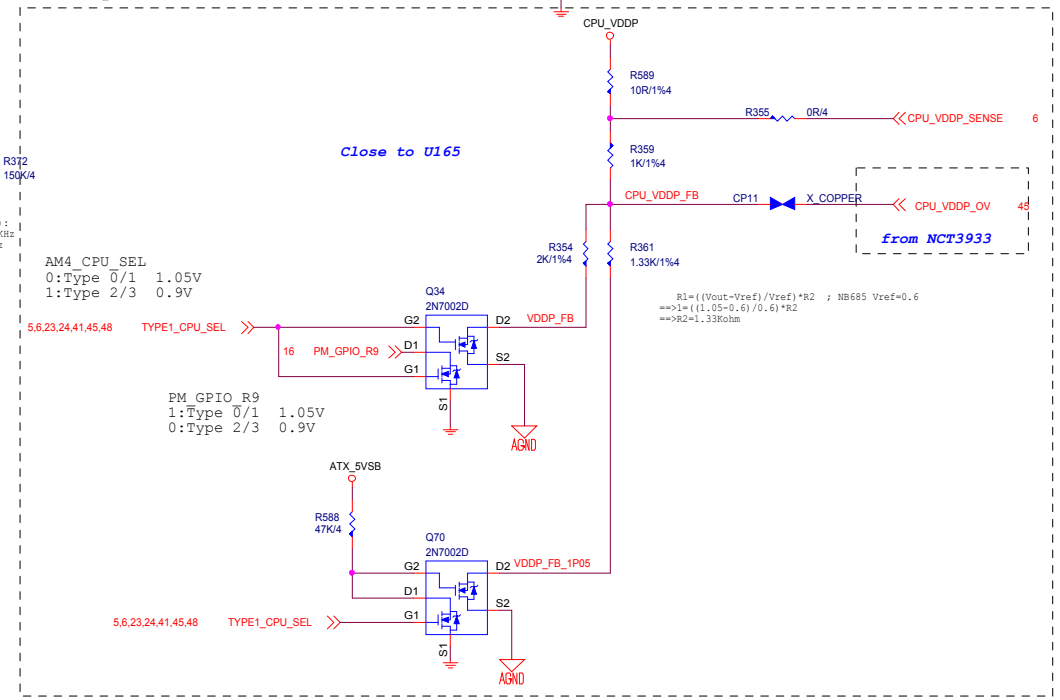
CPU_VDDP_S0

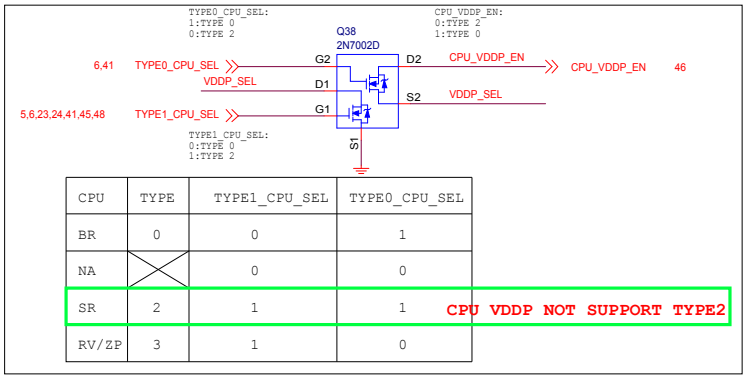
1.05V/0.9
S0:8.5A

OCP=15.45A

I9C-685GQ0C-M03





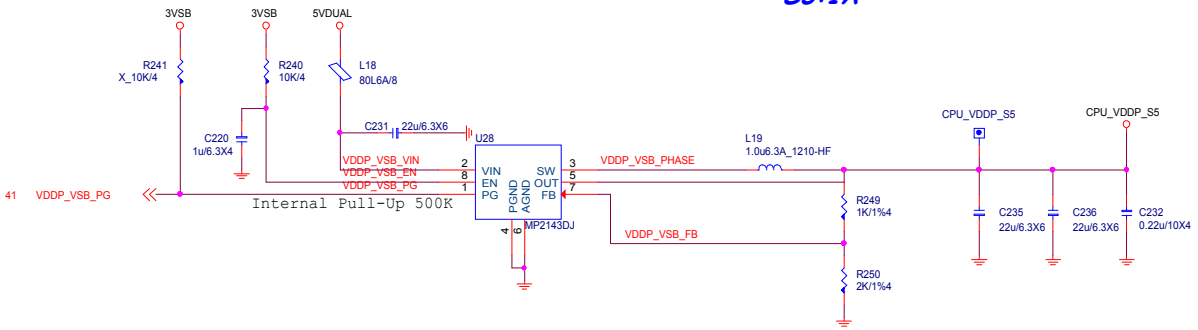


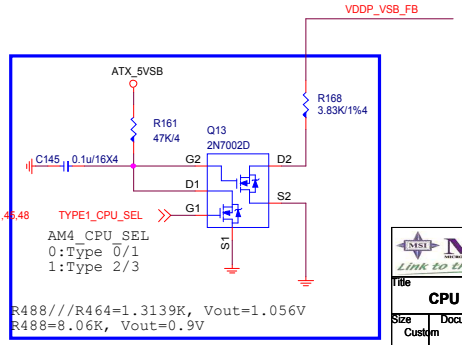
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

CPU_VDDP_S5

VDDP_S5
1.05V/0.9
S5:1A





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Title	CPU Power VDDP-NB685	
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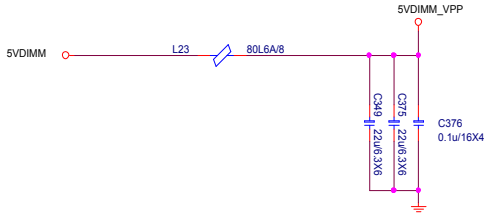
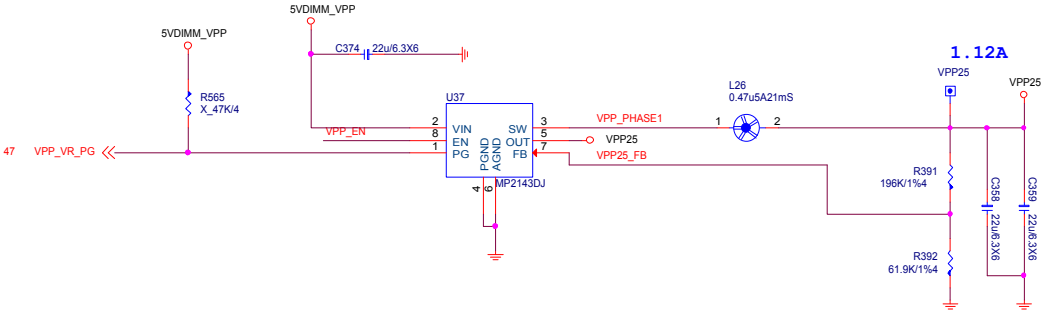
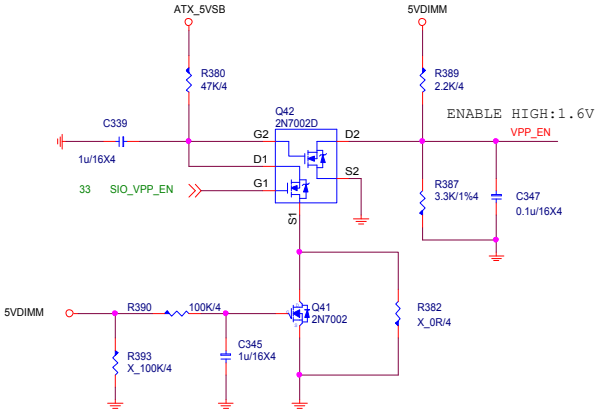
2DIMM :1.12A FOR DDR VPP2.5V







MICRO-START INT'L CO.,LTD.

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Title: DDR PWR VPP25/VTT-MP2143		
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FOR Promontory 1.05V_S0

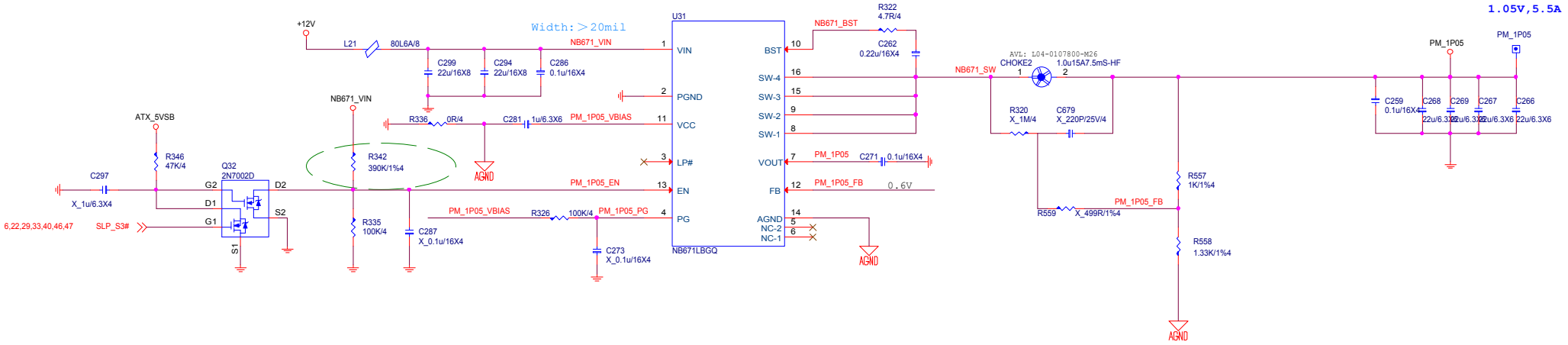
1.05V
S0:5.5A
S5:0.05A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH

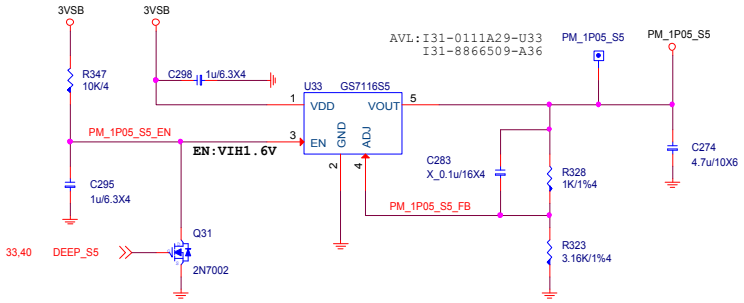
F:500K

1.05V,5.5A



FOR Promontory 1.05V_S5

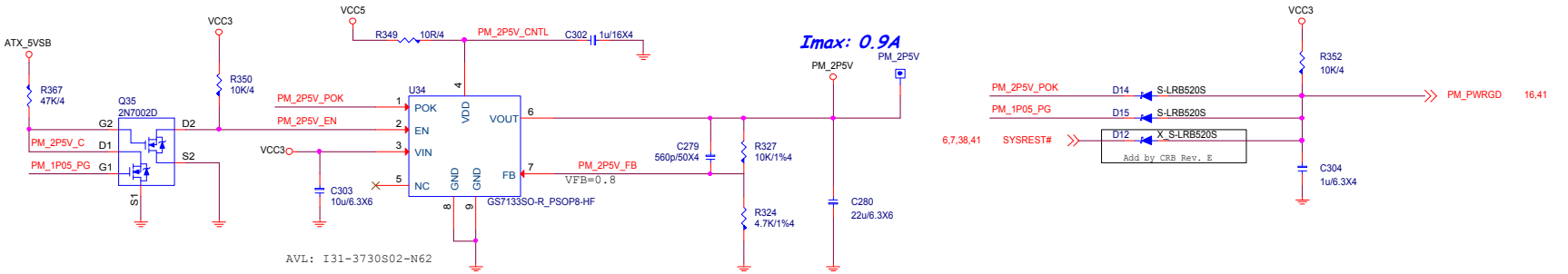
0.05A



Promontory-2.5V

2.5V; 900mA

Imax: 0.9A



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Title	PM-NB671-1.05V/GS7133-2.5V	
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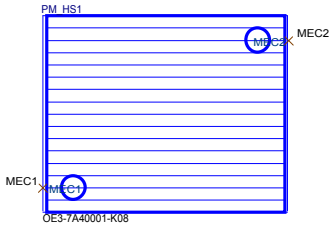
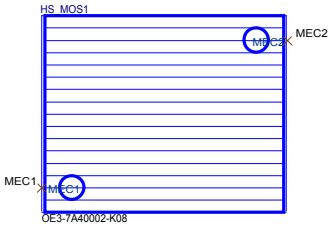
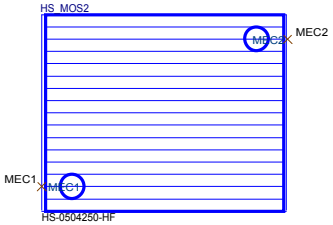
HEAT SINK



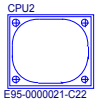
MOS HS(VCORE)



MOS HS(NB)

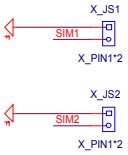


CPU Socket

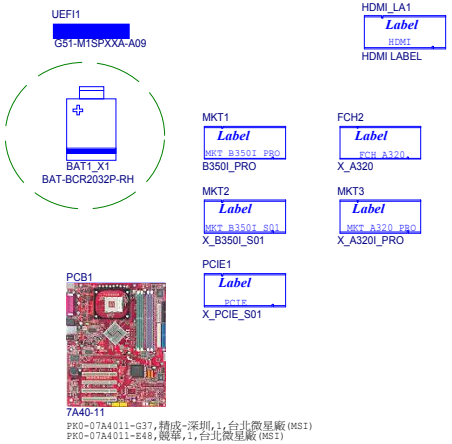


RETENTION MODULE

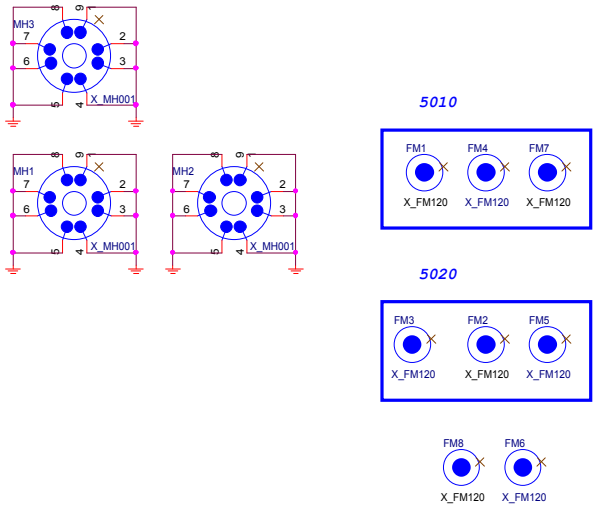
Simulation



MANUAL PART



Optics Orientation Holes



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