MS-7A40 Ver:10

CPU:
AMD AM4

System Chipset:
Promontory A320 / B350
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

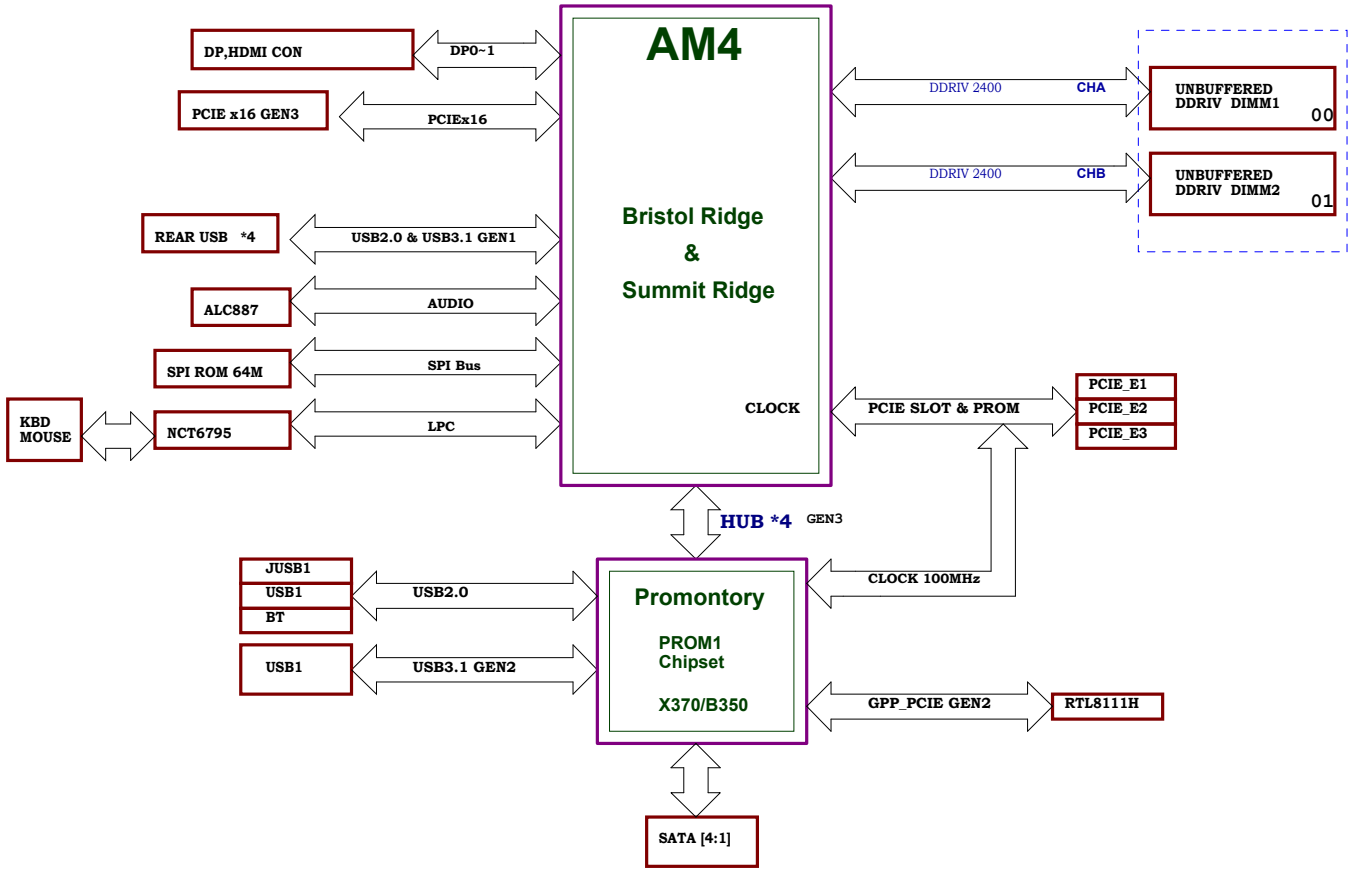
VRM
IR35201 6+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1

OCP IC:
RT9553

FUSION BLOCK DIAGRAM



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Title: Block Diagram		
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AMD AM4

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: COVER SHEET

Size: Custom | Document Number: MS-7A40.. | Rev: 0A

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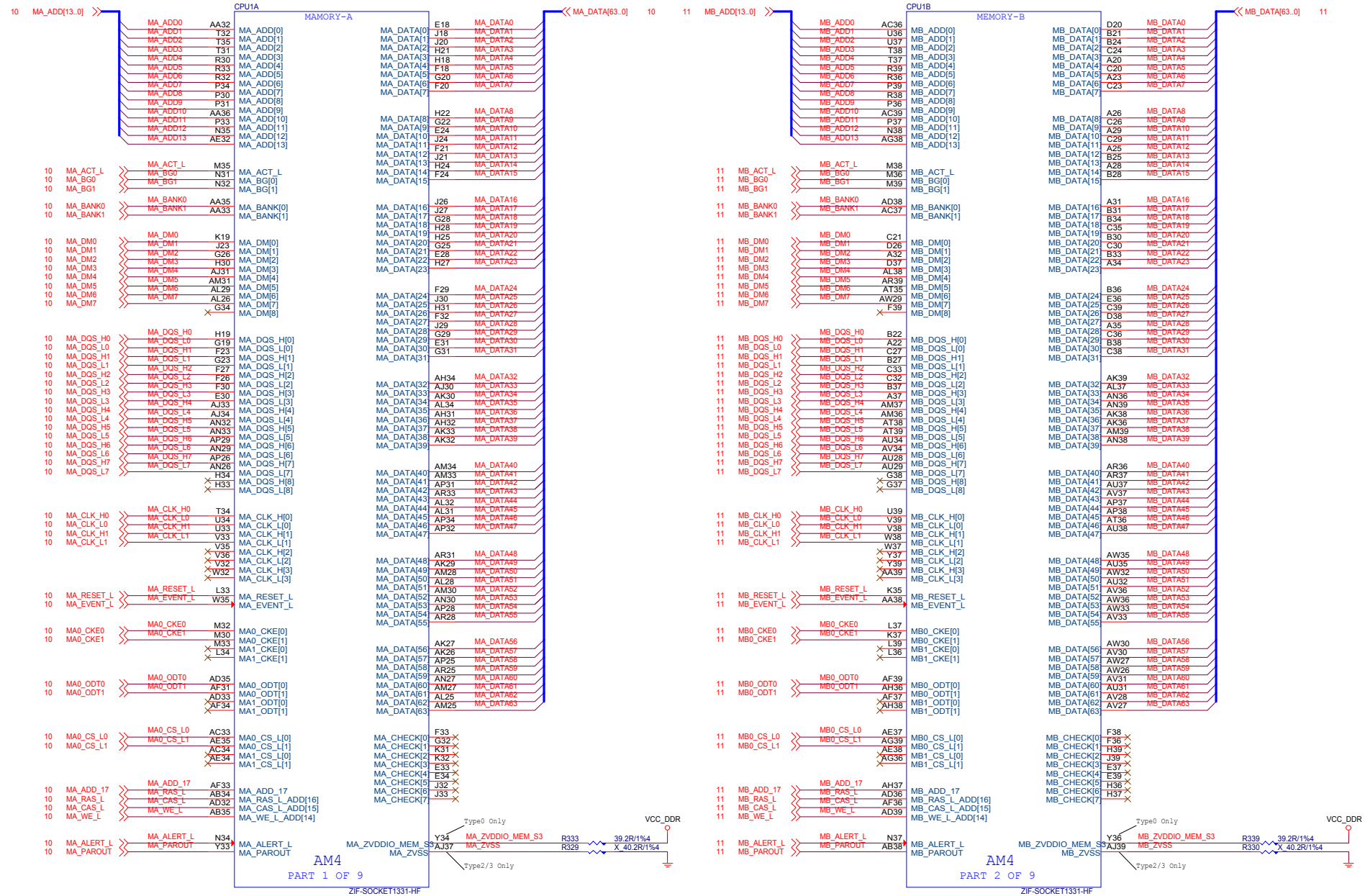

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Title	AM4 DDR4 I/F	
Size: Custom	Document Number: MS-7A40	Rev: 10
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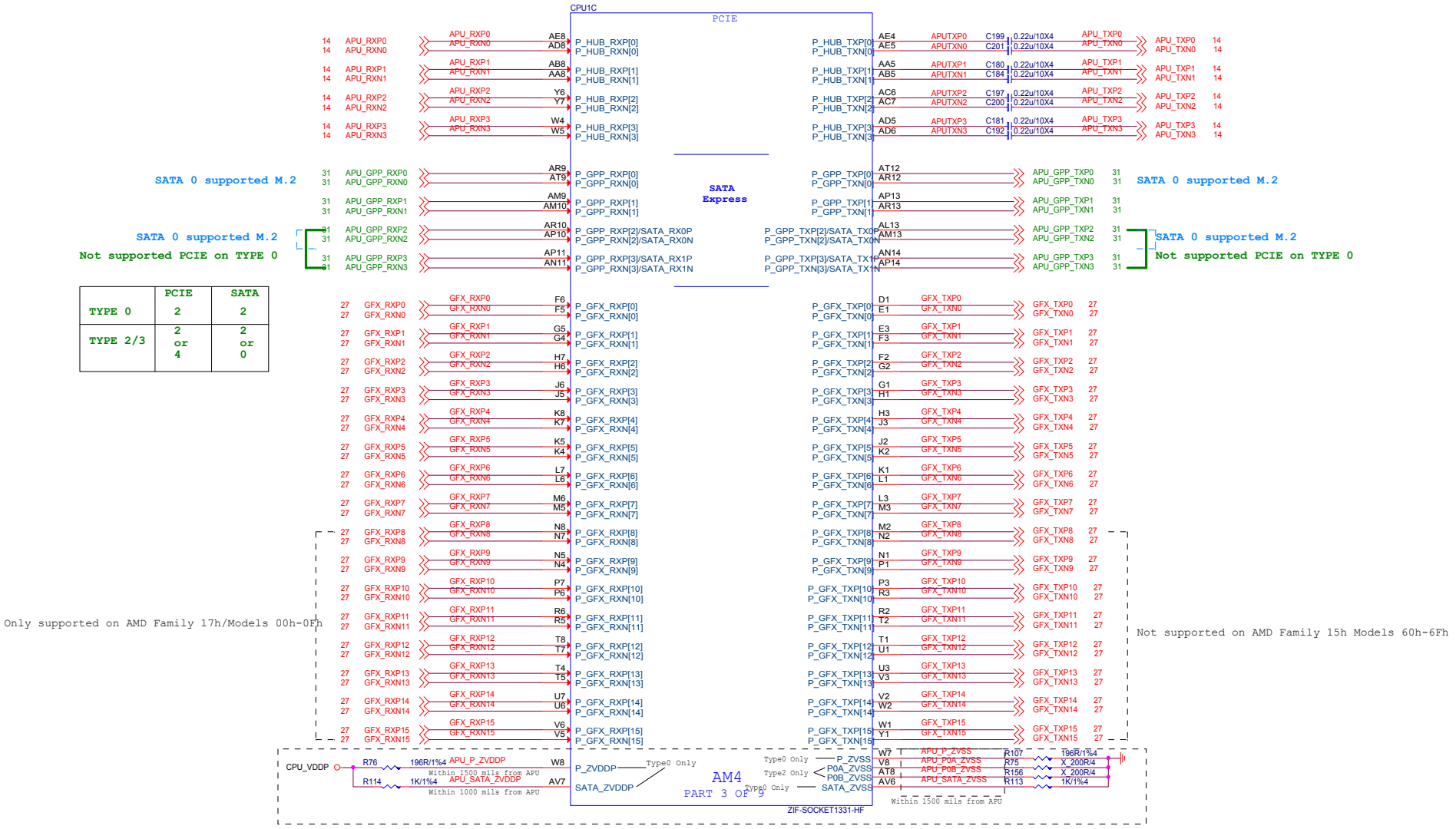

	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

Title	AM4 PCIE/SATAE
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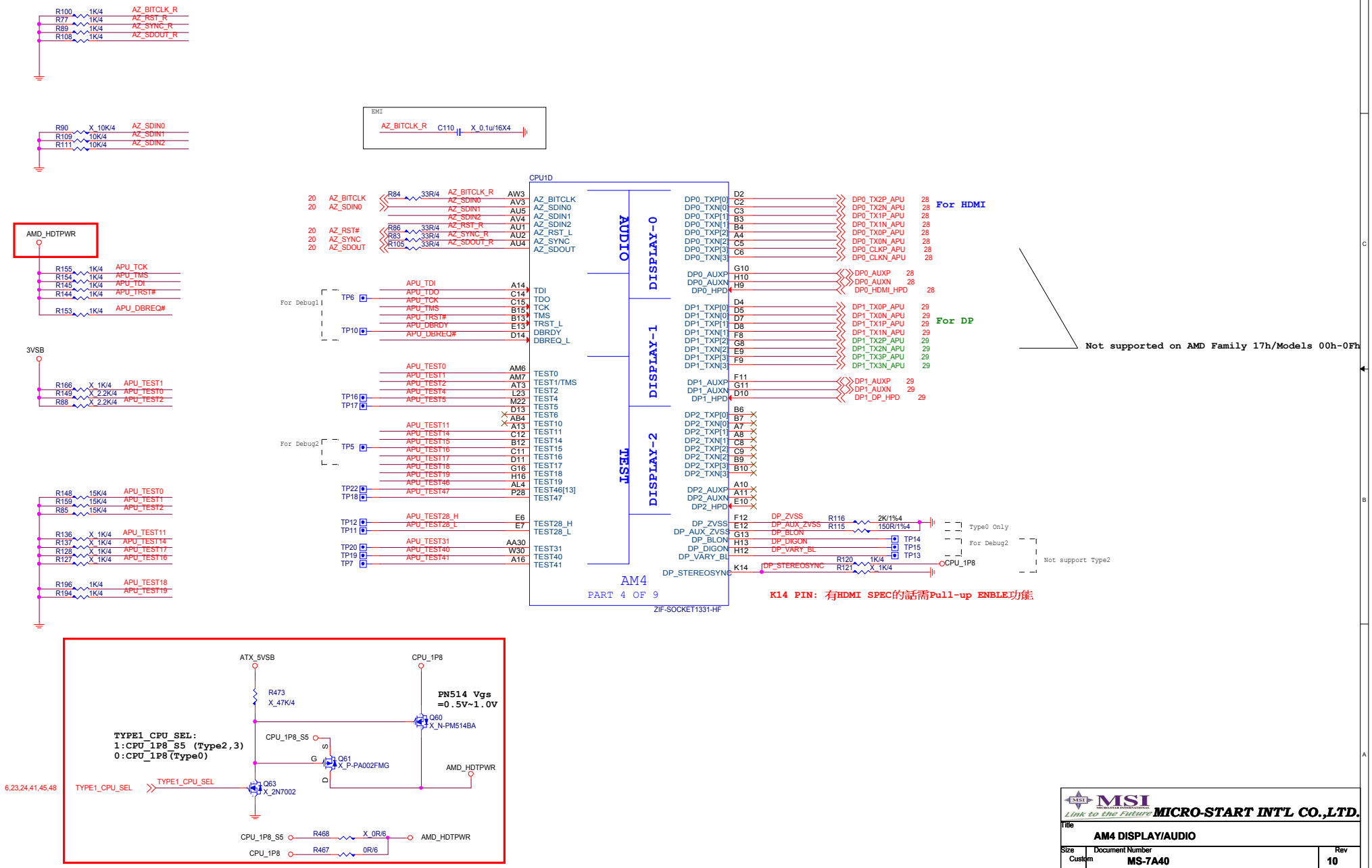

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Title	AM4 DISPLAY/AUDIO	
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AM4 CPU TYPE Circuit

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP

CORETYPE0
0:BR/SR
1:RV/ZP

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

Layout:Place x'tal within 1.5 inch of APU

Change by CRB rev. E

Follow CRB

Within 500mils

PART 5 OF 9

AM4

ZIF-SOCKET1331-HF

Modify USB_OC# circuit

For K TYPE FAN

GPIO97~100 for Debug LED

IB=(Vcc3-Vbe)/10k
(3.3-0.95)/10k=0.235mA

IC=(VCC2-Vce)/10k
(3.3-0.2)/10k=0.31mA

Title	AM4 SVI/ACPI/GPIO
Size	Custom
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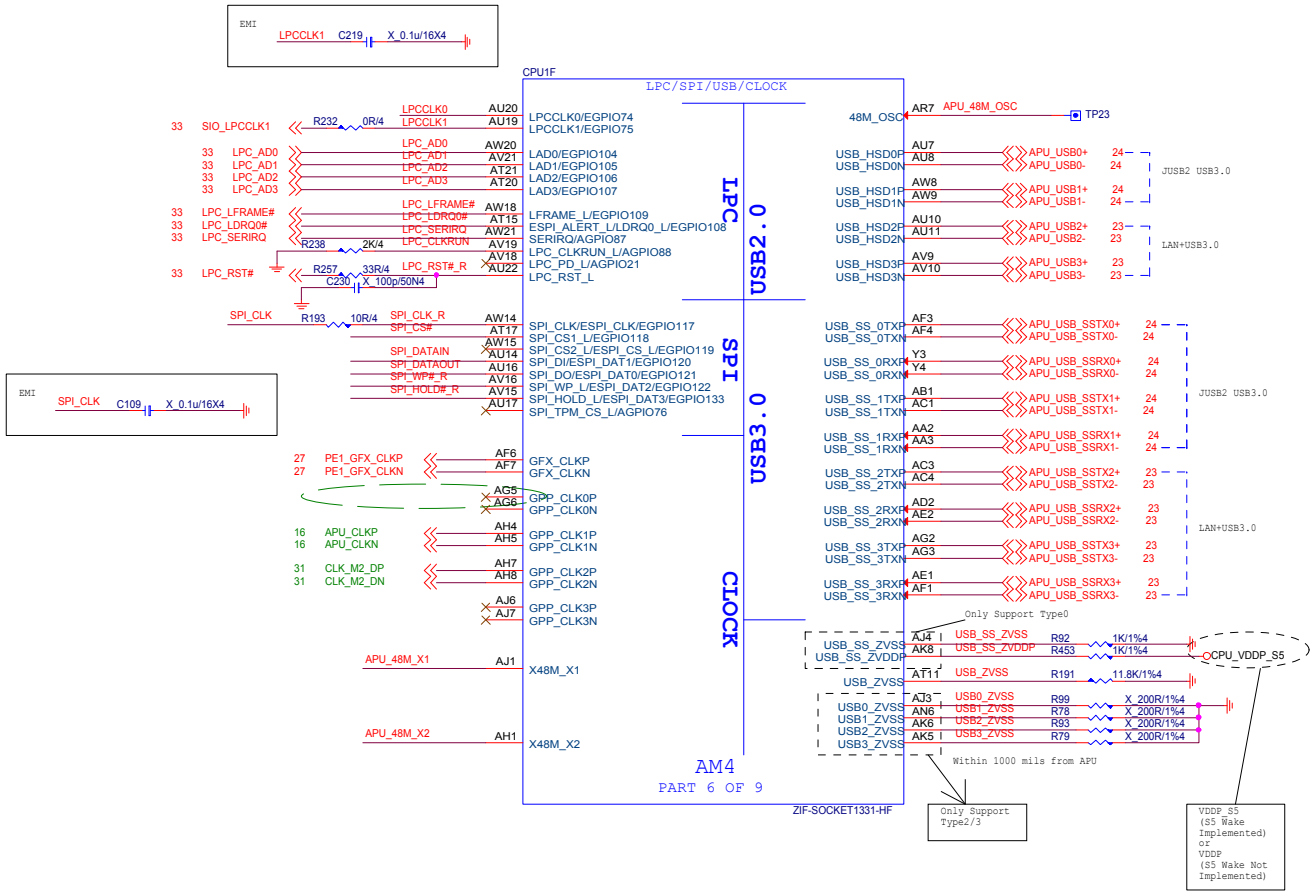
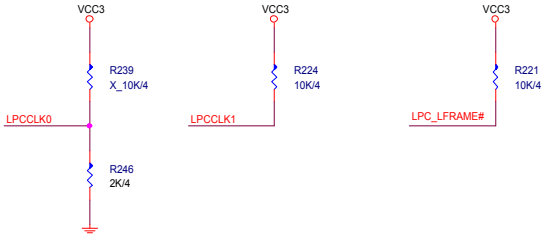
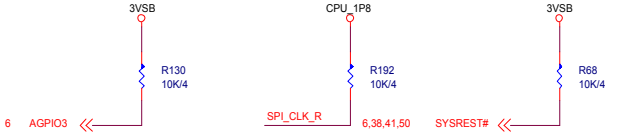
MICRO-START INT'L CO.,LTD.



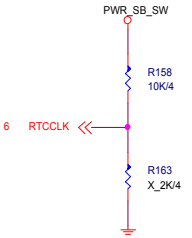
Strapping Options



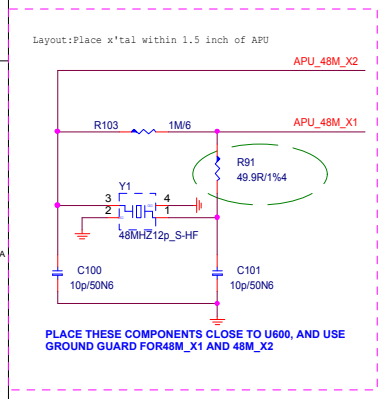
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



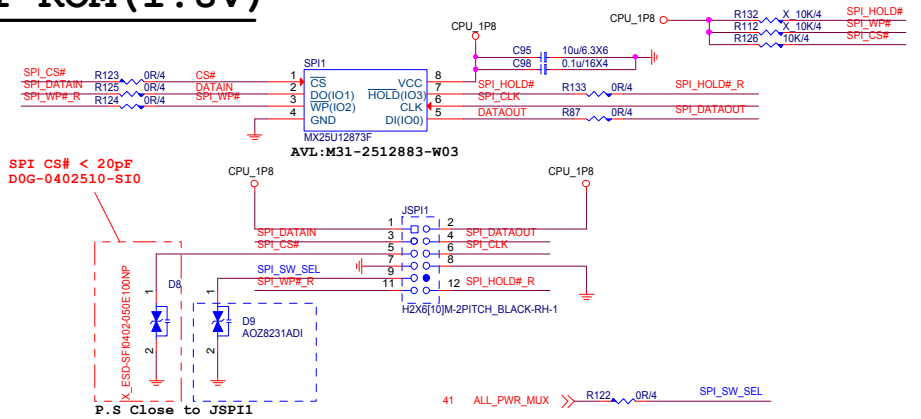
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board



SPI ROM(1.8V)



MICRO-START INT'L CO.,LTD.
Title: AM4 LPC/SPI/USB/CLK/STRAP
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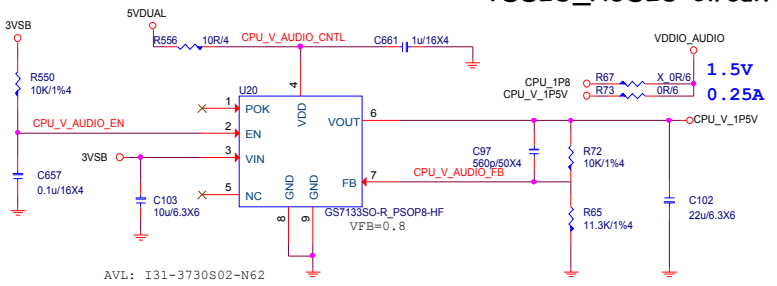
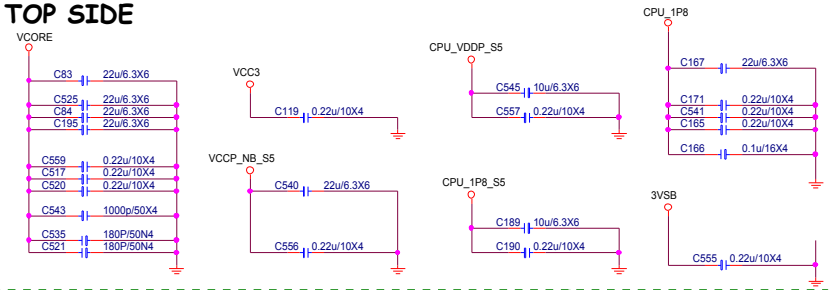
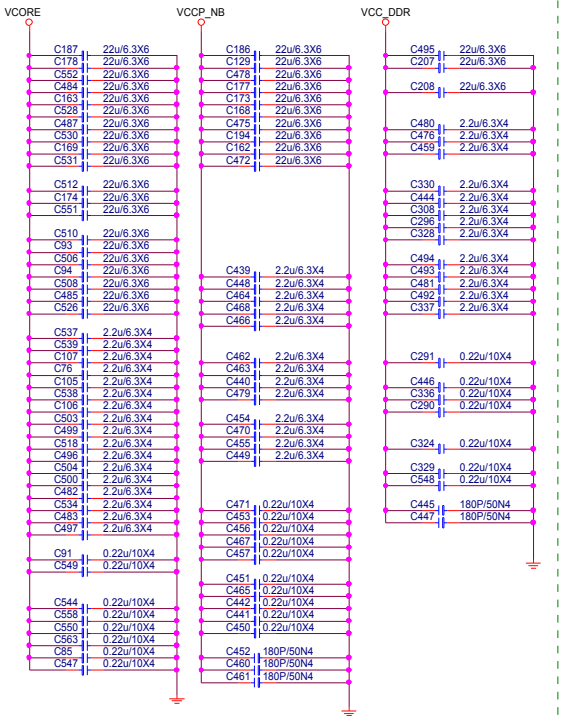
VDDIO_AUDIO Circuit



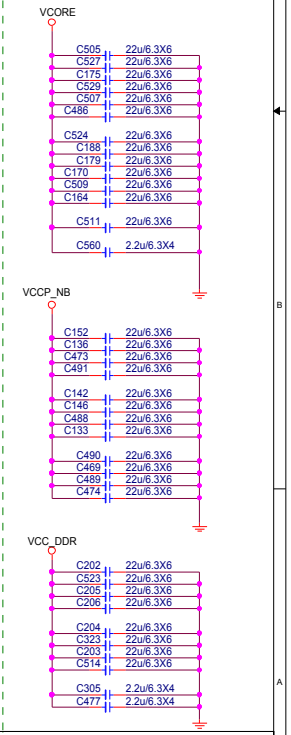
TOP SIDE

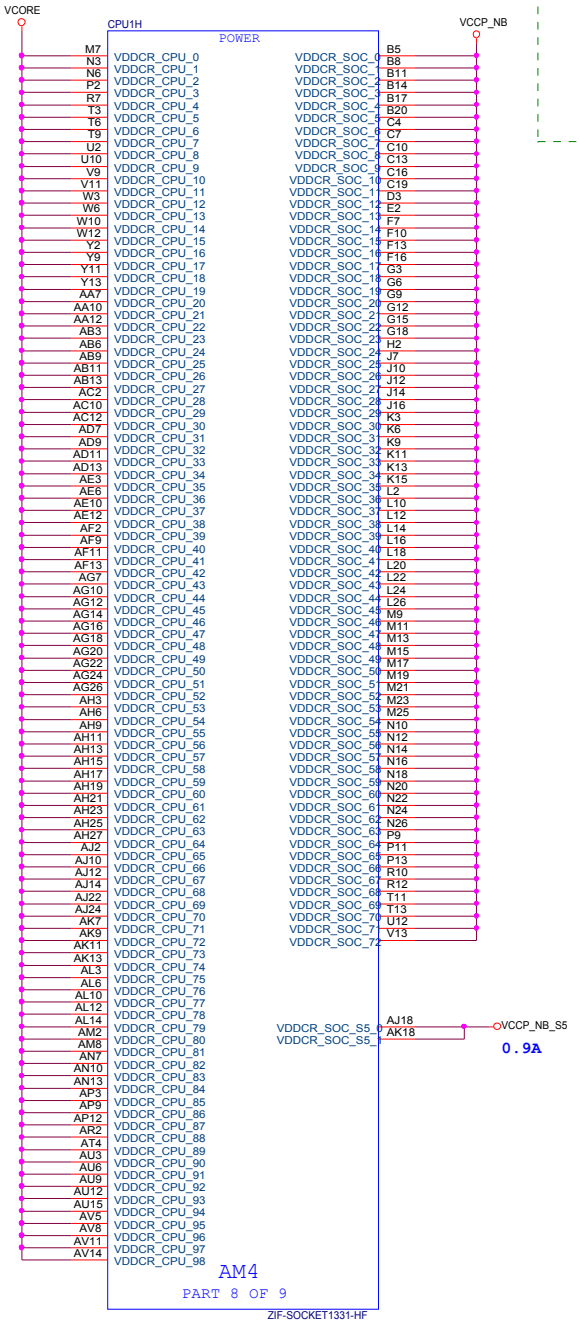


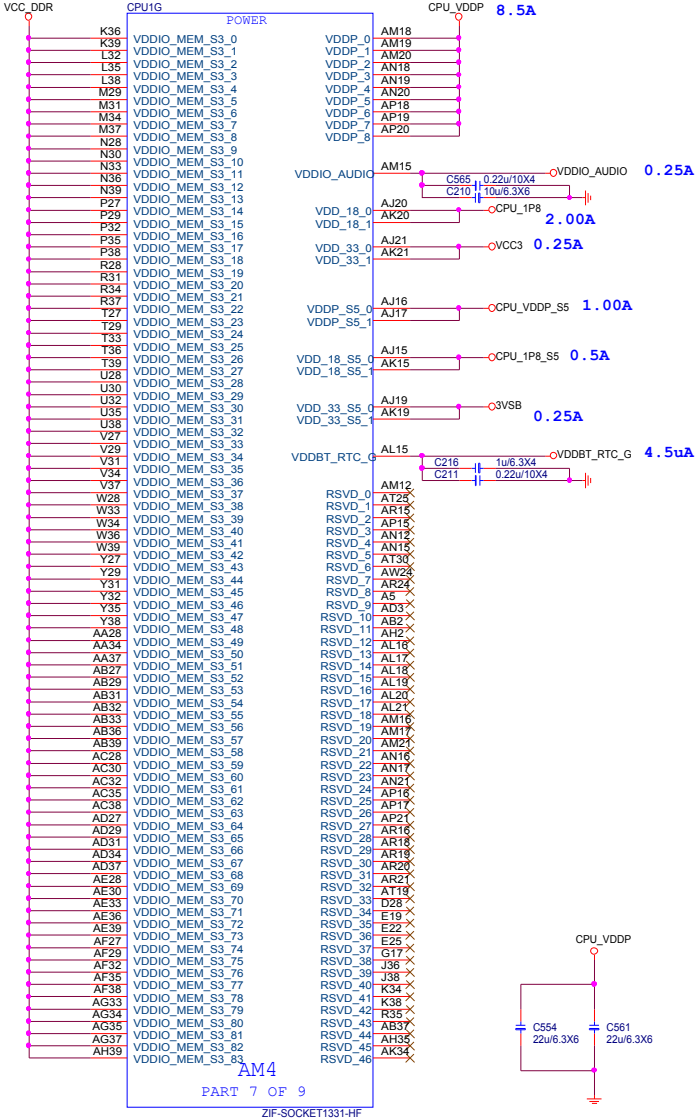
BOTTOM SIDE



TOP CAVITY







VDDCR_SOC_SS_0 / VDDCR_SOC_SS_1 — AJ18 / AK18 — VCCP_NB_S5 — 0.9A

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Link to the Future

Title	AM4 Power/RTC Power	
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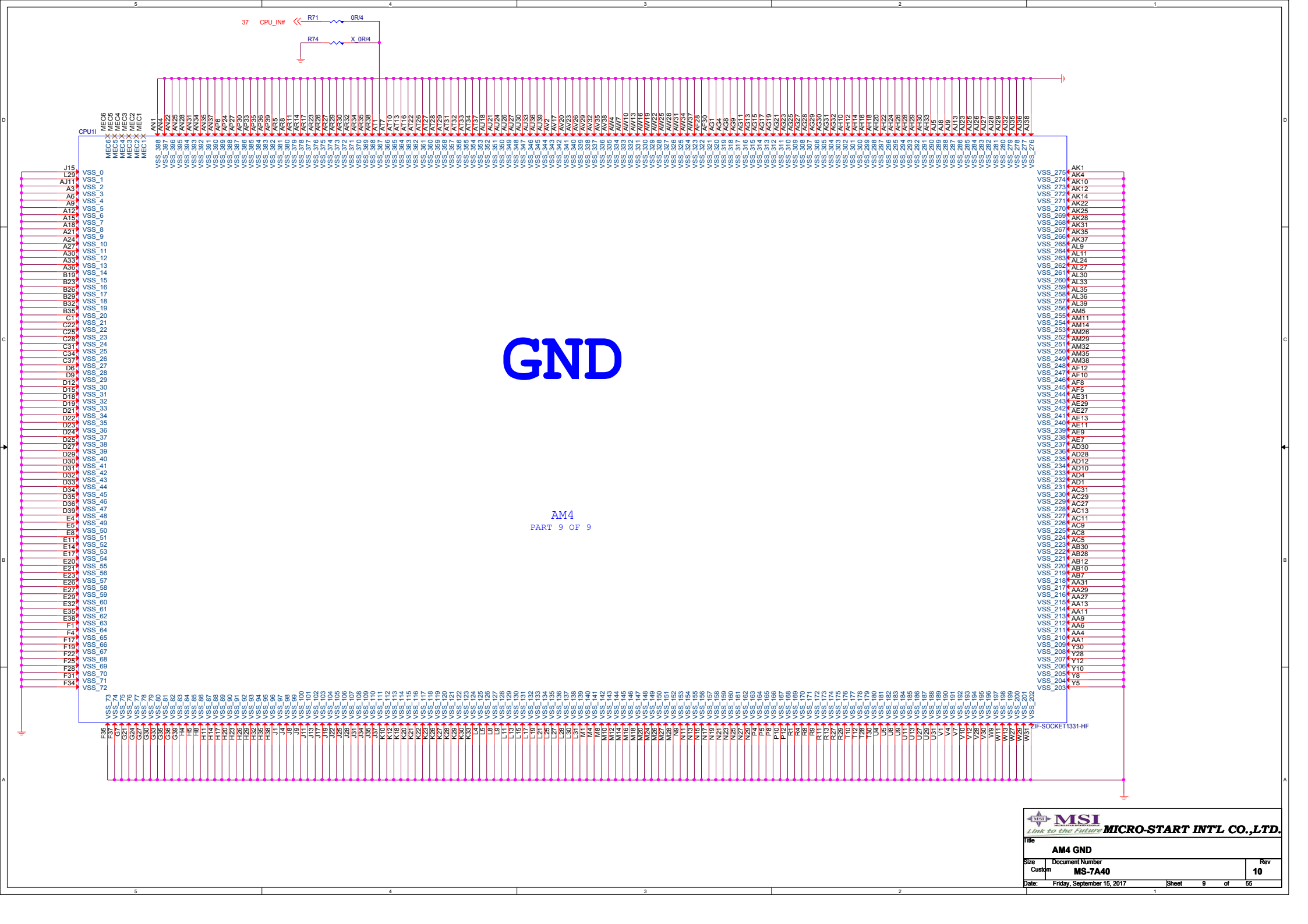

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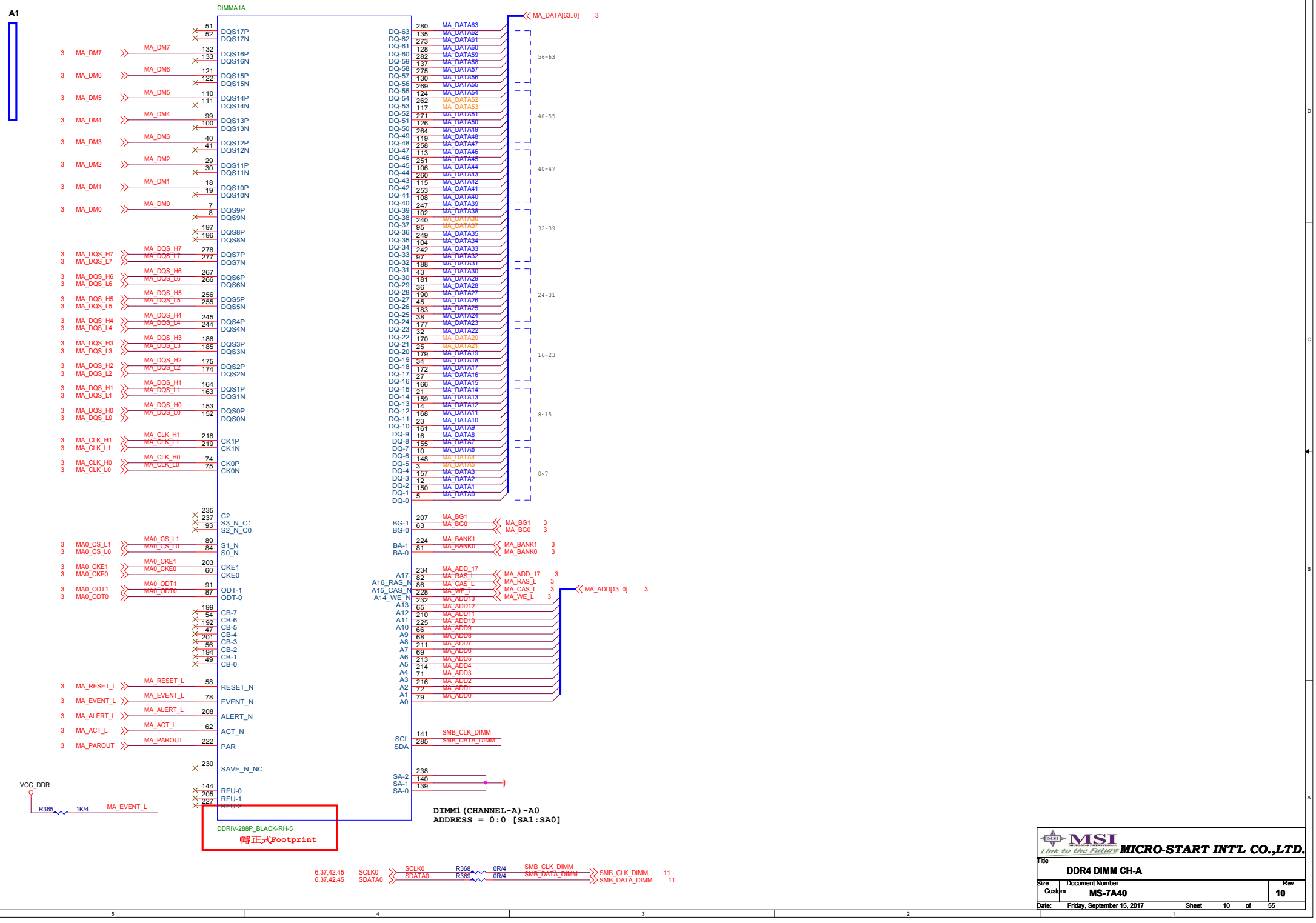
MICRO-START INT'L CO.,LTD.

Title	AM4 GND	
Size: Custom	Document Number: MS-7A40	Rev: 10
Date: Friday, September 15, 2017	Sheet 9 of 55	


A1
DIMMA1A
MA_DATA[63..0] 3
MA_ADD[13..0] 3
MA_DM7
MA_DM6
MA_DM5
MA_DM4
MA_DM3
MA_DM2
MA_DM1
MA_DM0
MA_DQS_H7
MA_DQS_L7
MA_DQS_H6
MA_DQS_L6
MA_DQS_H5
MA_DQS_L5
MA_DQS_H4
MA_DQS_L4
MA_DQS_H3
MA_DQS_L3
MA_DQS_H2
MA_DQS_L2
MA_DQS_H1
MA_DQS_L1
MA_DQS_H0
MA_DQS_L0
MA_CLK_H1
MA_CLK_L1
MA_CLK_H0
MA_CLK_L0
MA0_CS_L1
MA0_CS_L0
MA0_CKE1
MA0_CKE0
MA0_ODT1
MA0_ODT0
MA_RESET_L
MA_EVENT_L
MA_ALERT_L
MA_ACT_L
MA_PAROUT
SMB_CLK_DIMM
SMB_DATA_DIMM
VCC_DDR
R365 1K/4 MA_EVENT_L
DDRIV-288P_BLACK-RH-5
轉正式Footprint
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
SCLK0 R368 0R/4 SMB_CLK_DIMM
SDATA0 R369 0R/4 SMB_DATA_DIMM
MICRO-START INT'L CO.,LTD.
Link to the Future
DDR4 DIMM CH-A
MS-7A40
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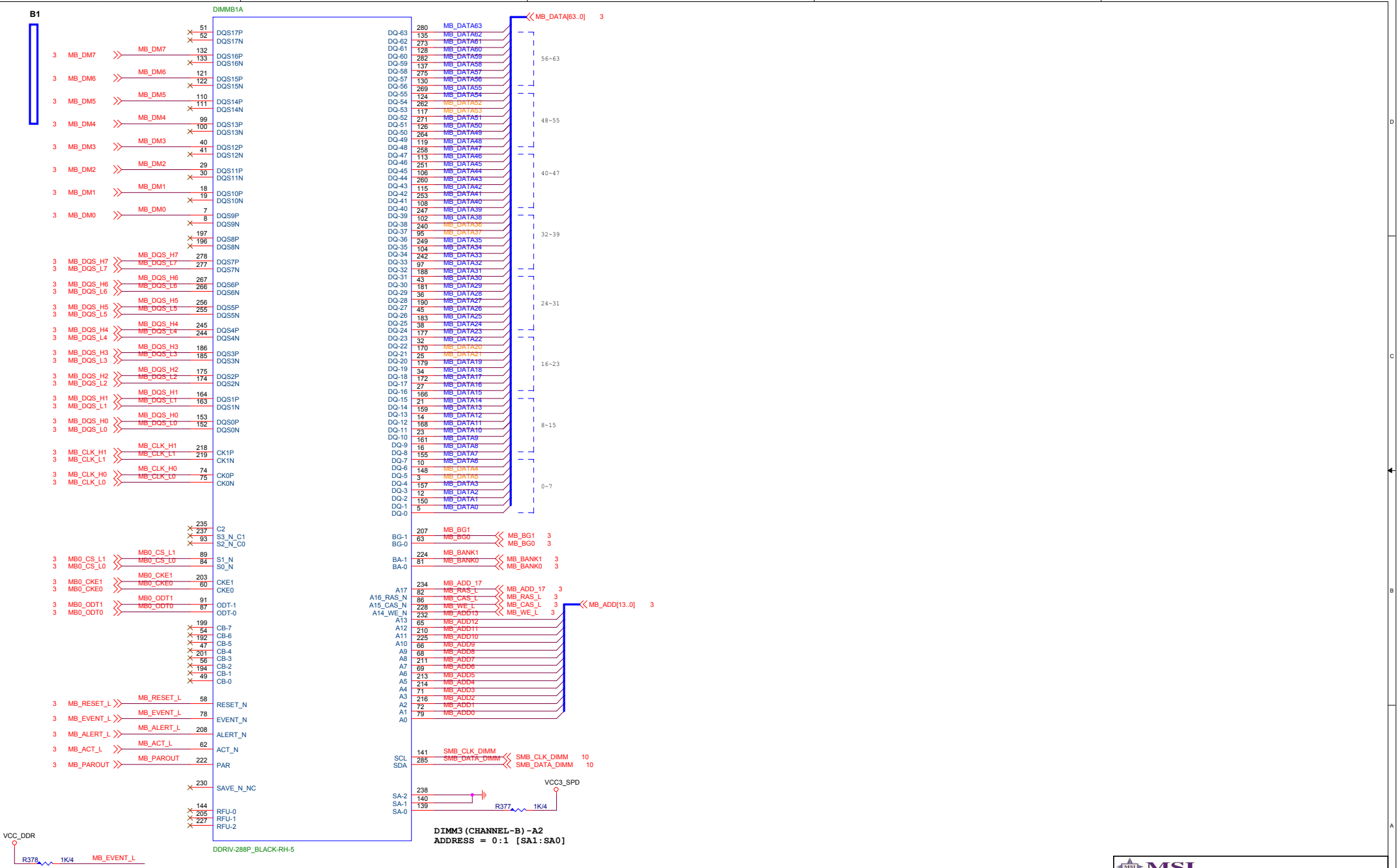

MICRO-START INT'L CO.,LTD.

Title: DDR4 DIMM CH-B		
Size: Custom	Document Number: MS-7A40	Rev: 10
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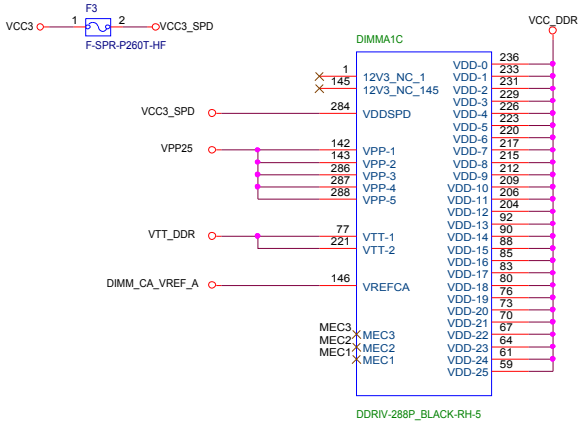
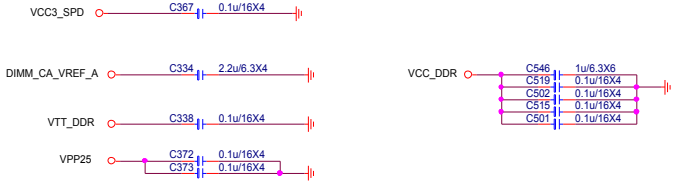
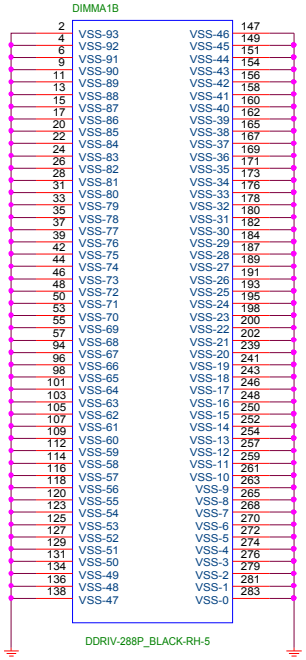


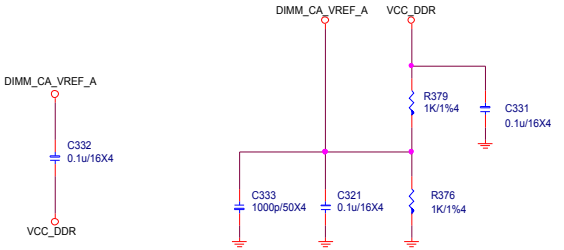
DIMM SLOT PN BY SPEC





DDR VREF

(place resistors close to DIMMs)



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MICRO-START INT'L CO.,LTD.

Title: DDR4-POWER/GND-1		
Size: Custom	Document Number: MS-7A40	Rev: 10
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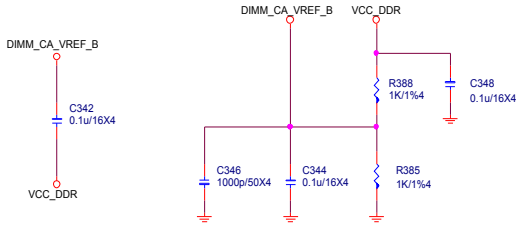
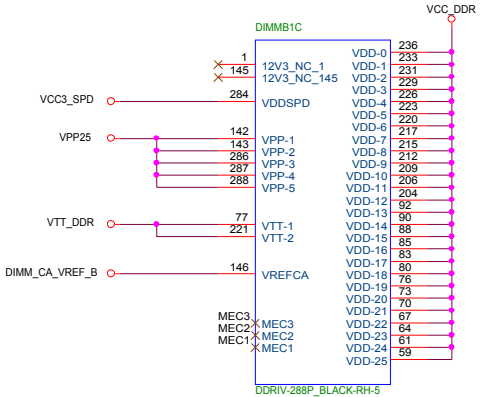
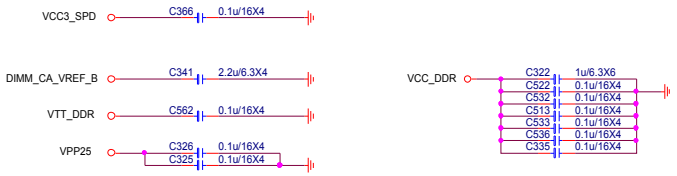
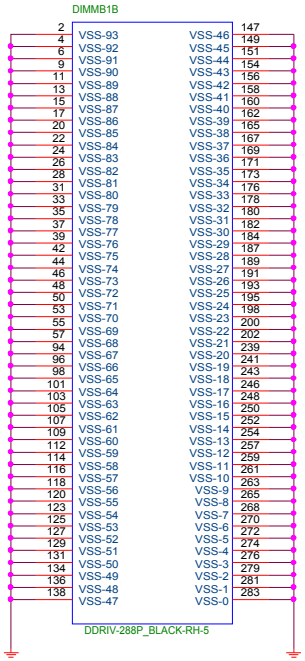
DDR VREF

(place resistors close to DIMMs)









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Link to the Future

Title: DDR4-POWER/GND-2		
Size: Custom	Document Number: MS-7A40	Rev: 10
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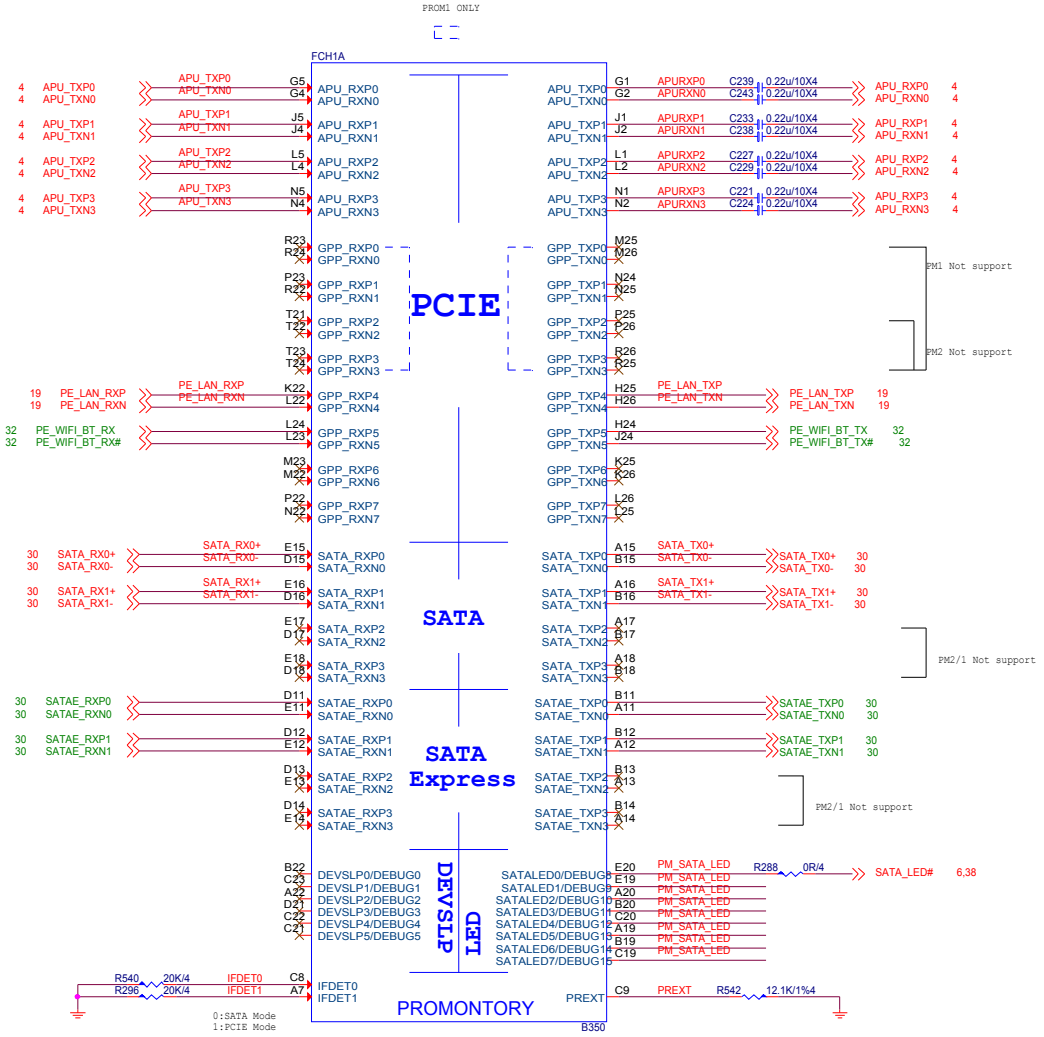

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

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Link to the Future

Title	Promontory-PCIE/SATA/SATAE	
Size: Custom	Document Number: MS-7A40	Rev: 10
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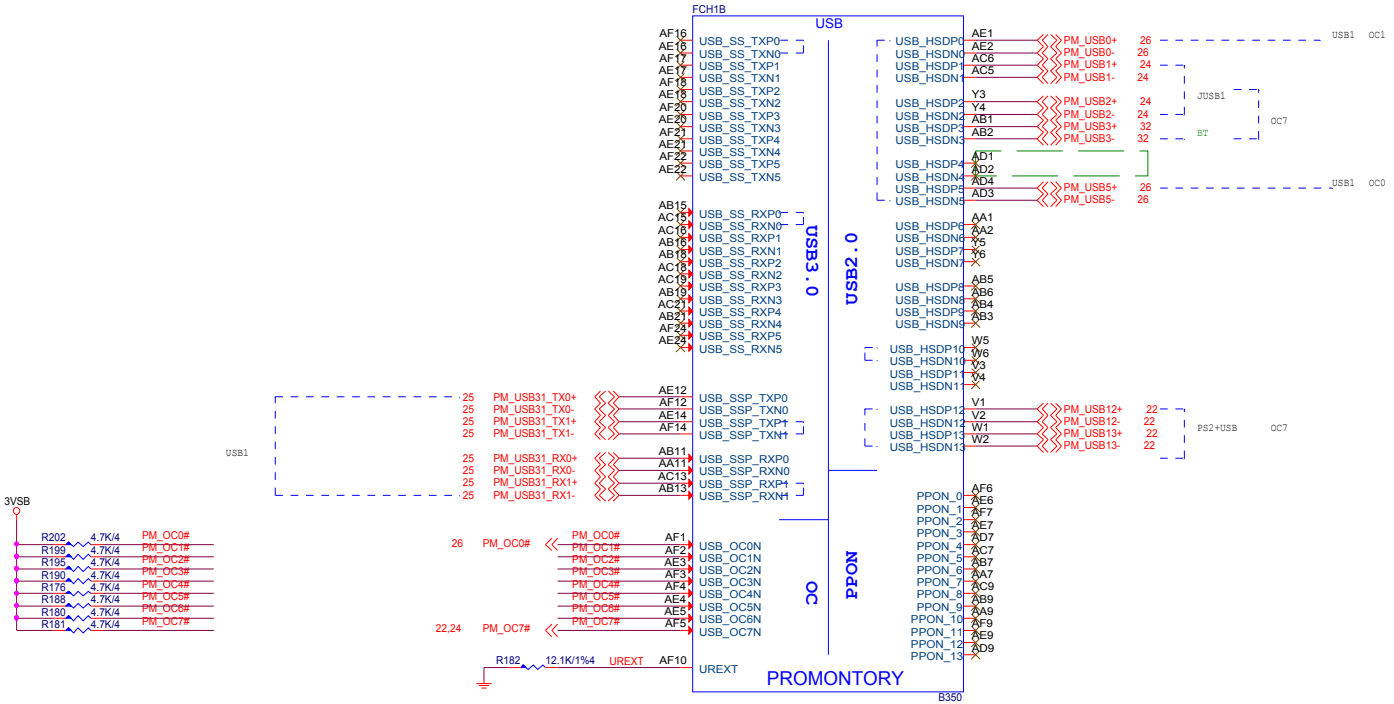

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

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Link to the Future

Title	Promontory-USB/OC	
Size: Custom	Document Number: MS-7A40	Rev: 10
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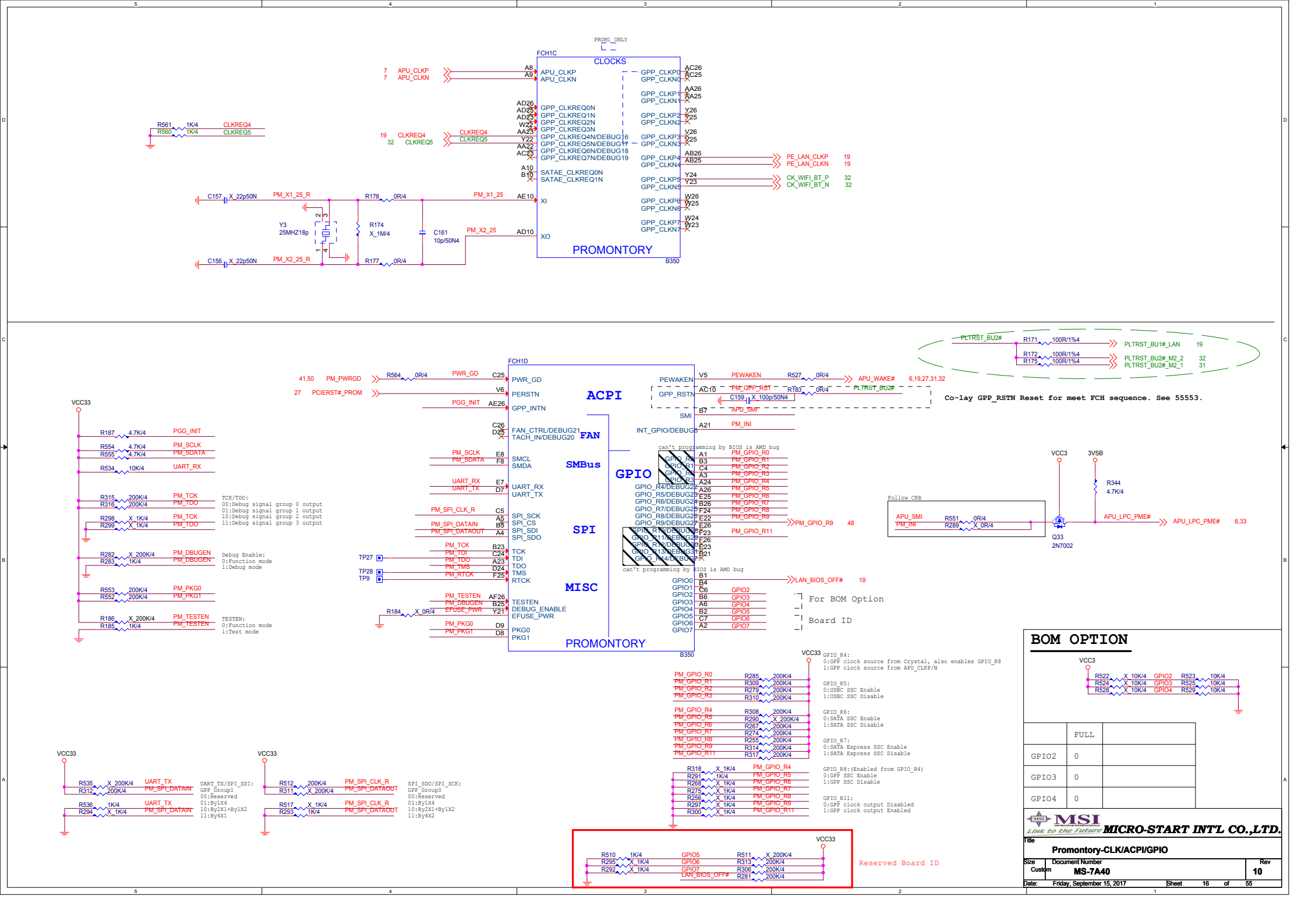
PROM1_ONLY
FCH1C
CLOCKS
APU_CLKP
APU_CLKN
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEBUG16
GPP_CLKREQ5N/DEBUG17
GPP_CLKREQ6N/DEBUG18
GPP_CLKREQ7N/DEBUG19
SATAE_CLKREQ0N
SATAE_CLKREQ1N
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
PE_LAN_CLKP
PE_LAN_CLKN
CK_WIFI_BT_P
CK_WIFI_BT_N
XI
XO
PROMONTORY
B350
Y3
25MHZ18p
R174
X_1M/4
C161
10p/50N4
C157
C156
X_22p50N
R178
R177
0R/4
PM_X1_25_R
PM_X2_25_R
PM_X1_25
PM_X2_25
R561
R560
1K/4
CLKREQ4
CLKREQ5
FCH1D
ACPI
FAN
SMBus
GPIO
SPI
MISC
PWR_GD
PERSTN
GPP_INTN
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMCL
SMDA
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
TCK
TDI
TDO
TMS
RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PKG0
PKG1
PEWAKEN
GPP_RSTN
SMI
INT_GPIO/DEBUG8
PM_INI
PM_GPIO_R0
PM_GPIO_R1
PM_GPIO_R2
PM_GPIO_R3
PM_GPIO_R4
PM_GPIO_R5
PM_GPIO_R6
PM_GPIO_R7
PM_GPIO_R8
PM_GPIO_R9
PM_GPIO_R11
LAN_BIOS_OFF#
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
PM_PWRGD
PCIERST#_PROM
PGG_INIT
PM_SCLK
PM_SDATA
PM_SPI_CLK_R
PM_SPI_DATAIN
PM_SPI_DATAOUT
PM_TCK
PM_TDI
PM_TDO
PM_TMS
PM_RTCK
PM_TESTEN
PM_DBUGEN
EFUSE_PWR
PM_PKG0
PM_PKG1
R564
R527
R183
C159
X_100p/50N4
APU_WAKE#
PLTRST_BU2#
APU_SMI
can't programming by BIOS is AMD bug
PLTRST_BU2#
R171
R172
R175
100R/1%4
PLTRST_BU1#_LAN
PLTRST_BU2#_M2_2
PLTRST_BU2#_M2_1
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
VCC33
3VSB
R344
4.7K/4
Follow CRB
APU_SMI
PM_INI
R551
R289
APU_LPC_PME#
Q33
2N7002
R187
R554
R555
R534
R315
R316
R298
R299
R282
R283
R553
R552
R186
R185
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
Debug Enable:
0:Function mode
1:Debug mode
TESTEN:
0:Function mode
1:Test mode
TP27
TP28
TP9
R184
For BOM Option
Board ID
GPIO_R4:
0:GPP clock source from Crystal, also enables GPIO_R8
1:GPP clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
R535
R312
R536
R294
R512
R311
R517
R293
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X1
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
R510
R295
R292
R511
R313
R306
R281
Reserved Board ID
BOM OPTION
R522
R524
R528
R523
R525
R529
GPIO2
GPIO3
GPIO4
FULL
0
MICRO-START INT'L CO.,LTD.
Promontory-CLK/ACPI/GPIO
MS-7A40
10
Friday, September 15, 2017
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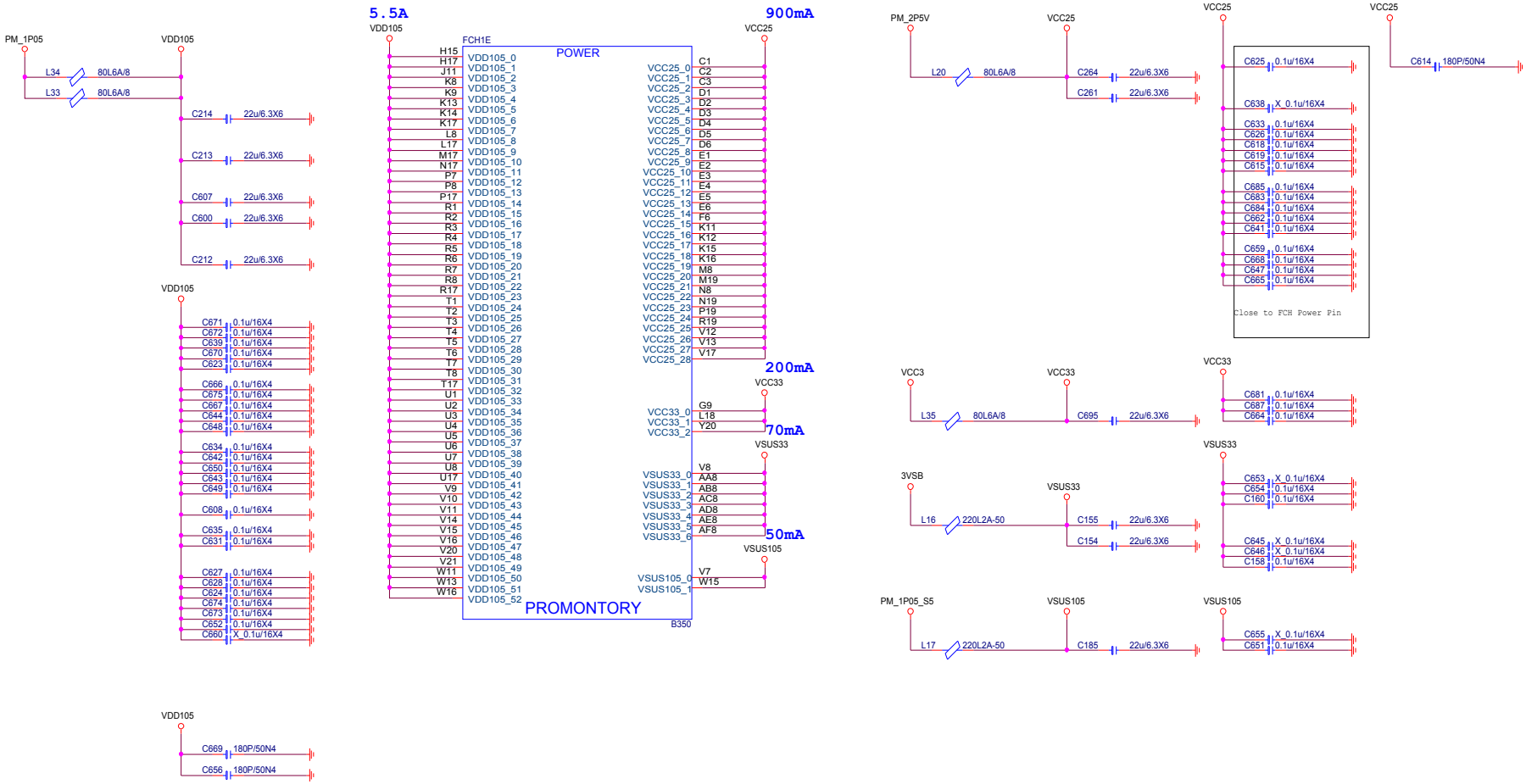
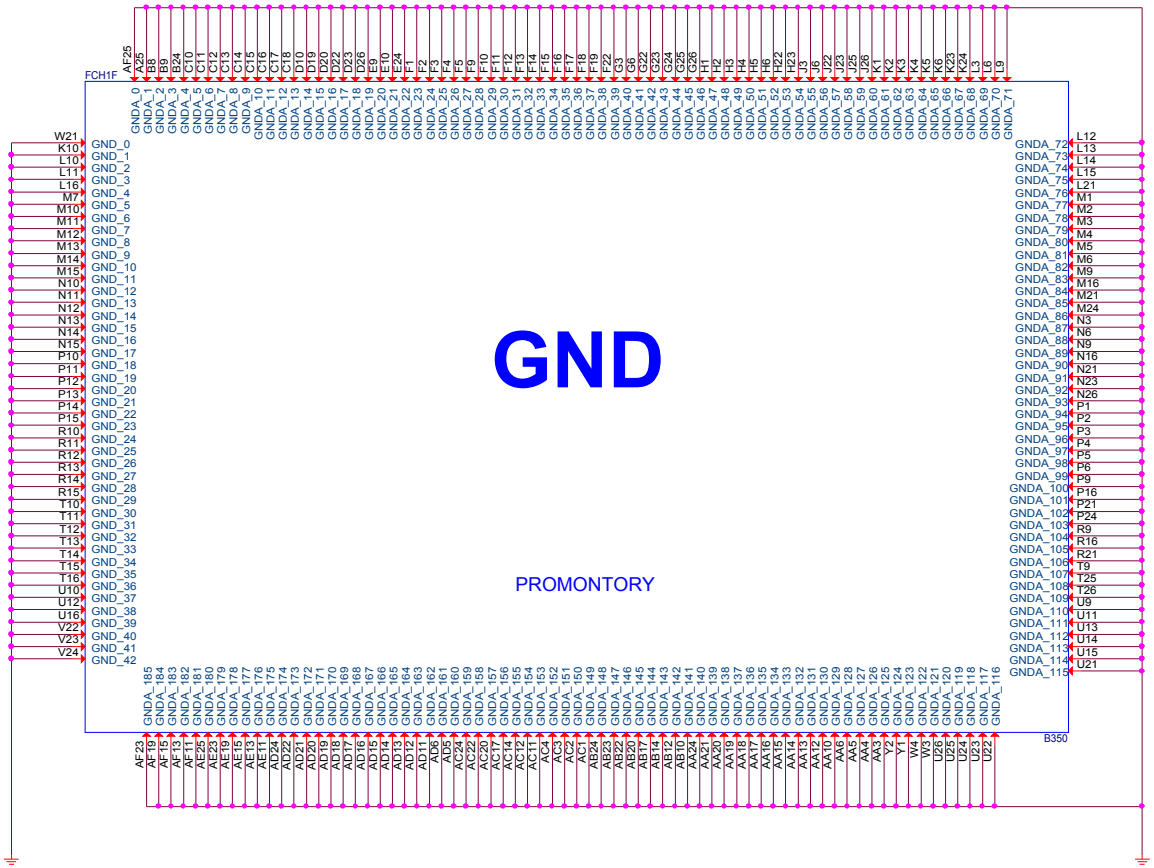


MICRO-START INT'L CO.,LTD.			
Title: Promontory-Power			
Size: Custom	Document Number: MS-7A40		Rev: 10
Date: Friday, September 15, 2017	Sheet 17 of 55		



MSI MICRO-STAR INT'L CO.,LTD.	
Title	Promontory-GND
Size: Custom	Document Number: MS-7A40
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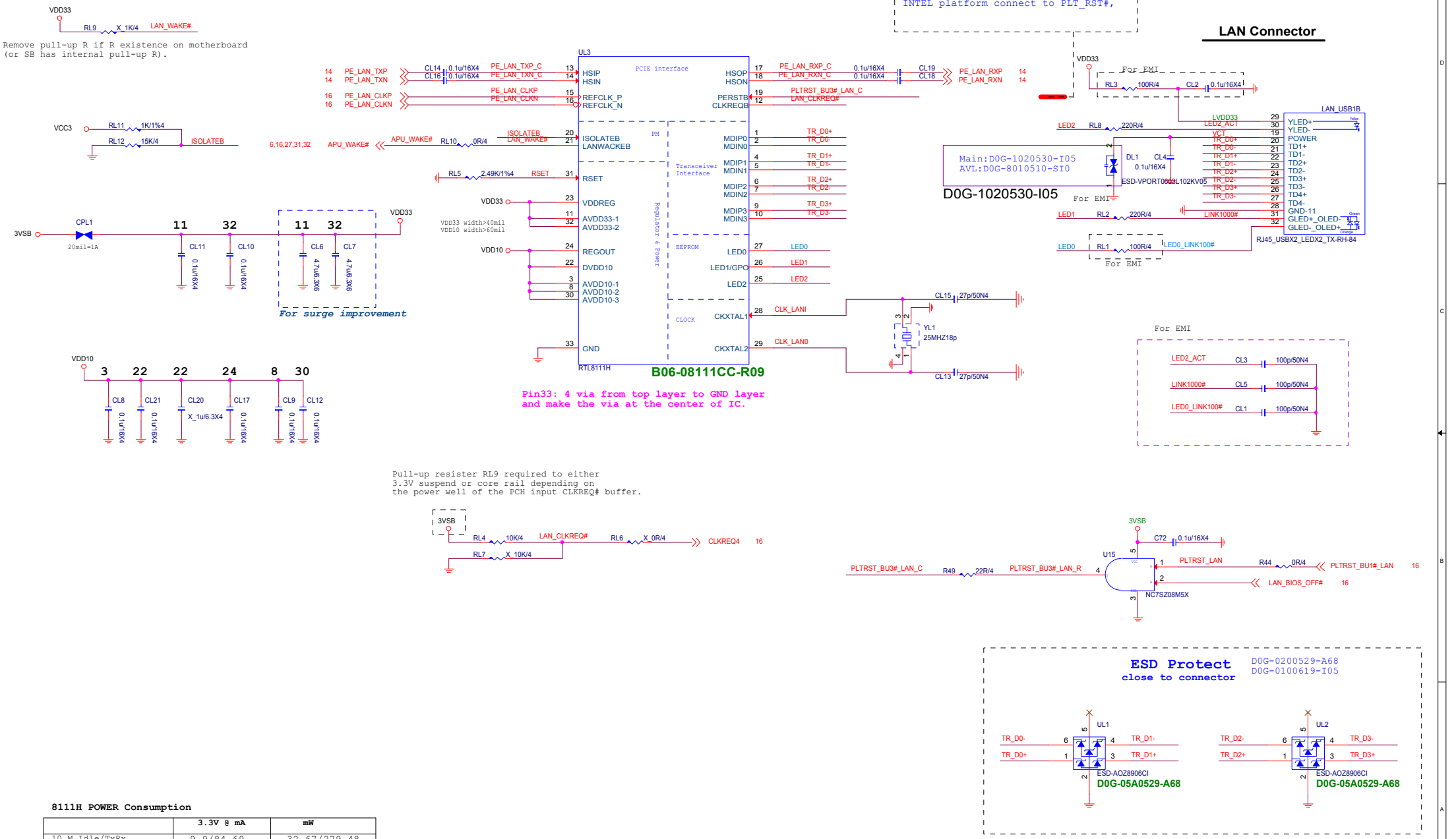
RTL8111H Giga LAN

3.3V@177.57mA



8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-START INT'L CO.,LTD.

Title: LAN-RLT 8111H

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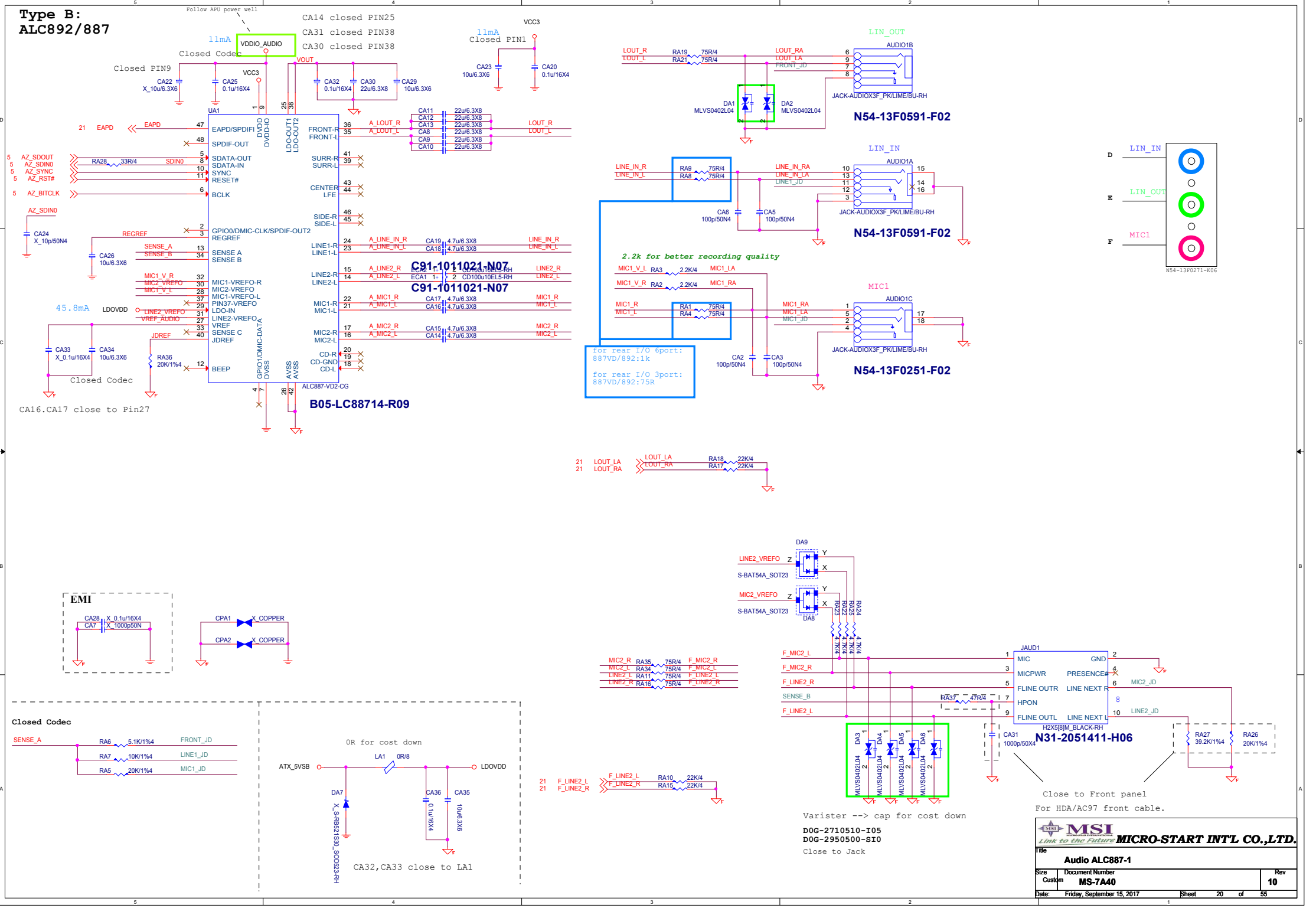
Type B:
ALC892/887



MICRO-START INT'L CO.,LTD.

Title	Audio ALC887-1	
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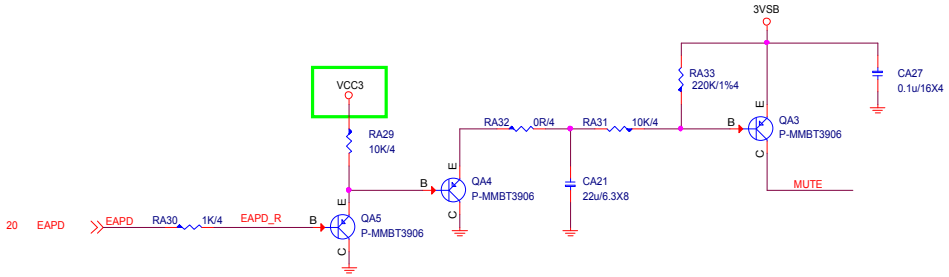
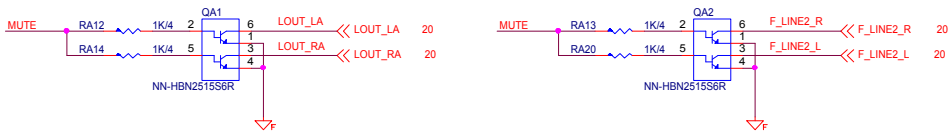
Rear Line OUT De-POP circuit

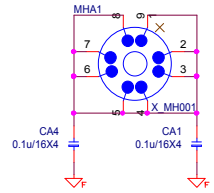
De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog





MICRO-START INT'L CO.,LTD.

Title: Audio ALC887-2

Size: Custom | Document Number: MS-7A40 | Rev: 10

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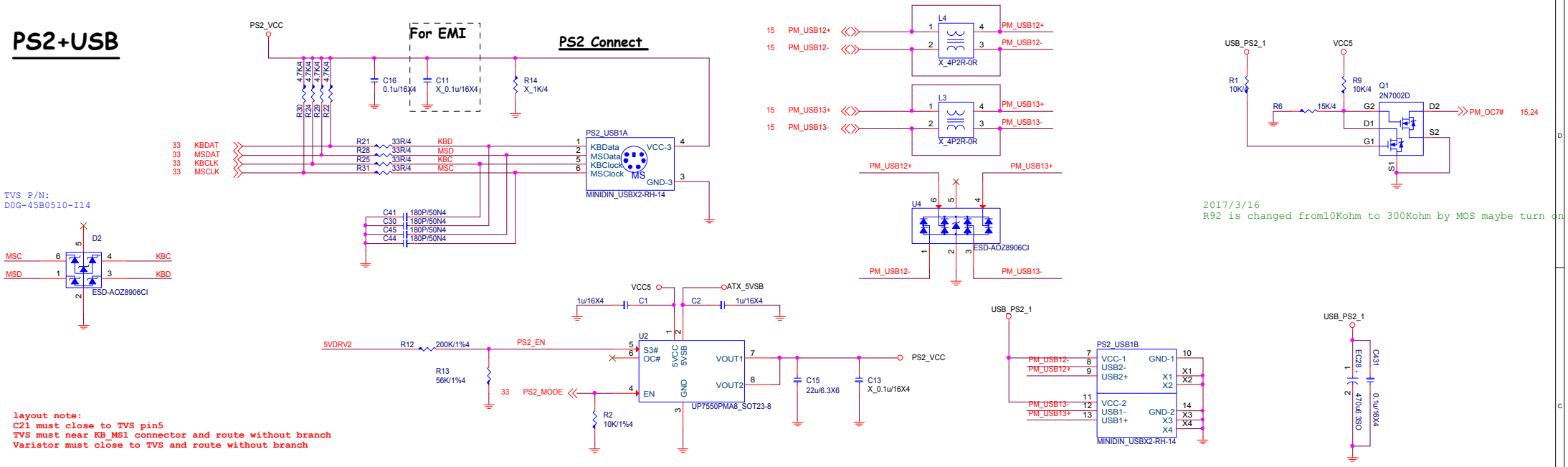
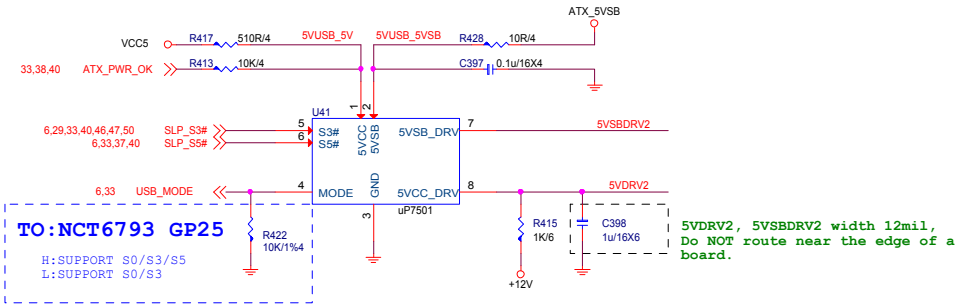
PS2+USB

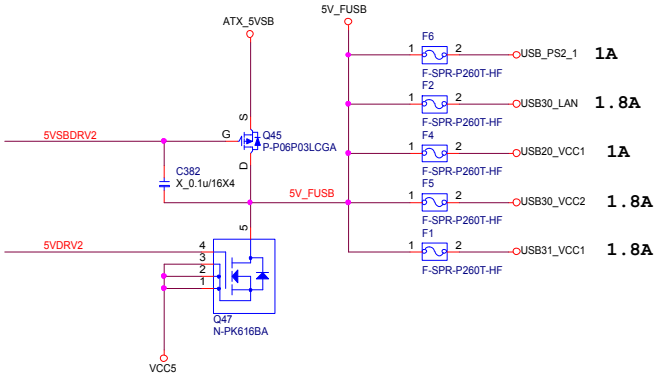


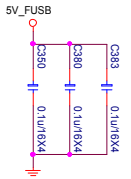
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

USB Power



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.





MICRO-START INT'L CO.,LTD.

Title	USB Rear PS2+USB2.0	
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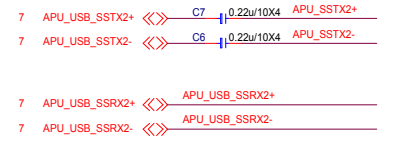
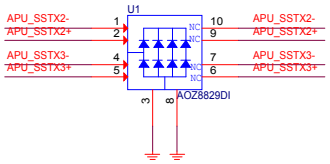
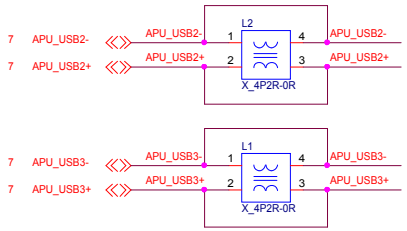
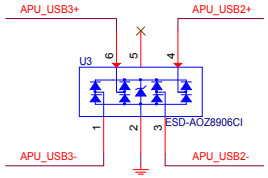
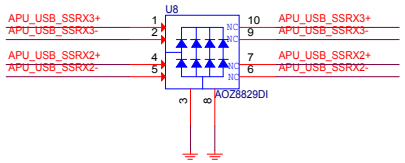
USB3.1 GEN1

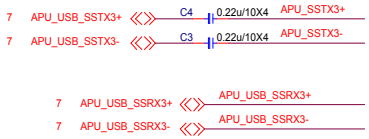




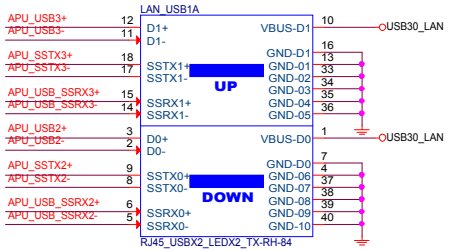


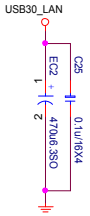


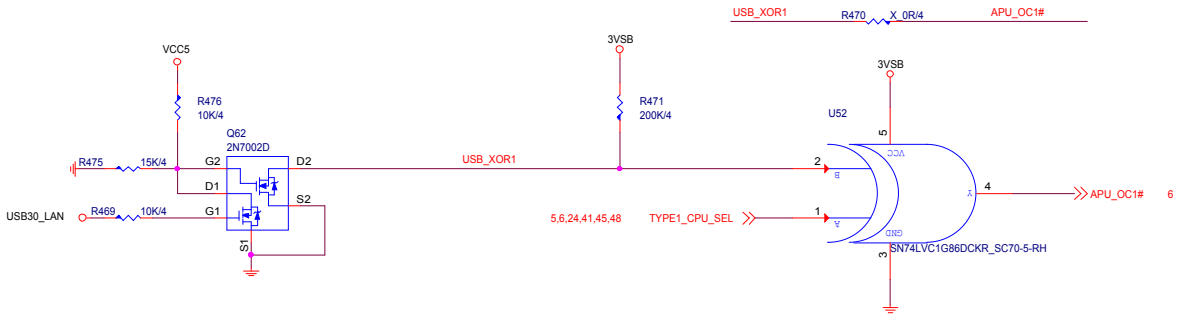




LAN+USB







Modify USB_OC# circuit

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	USB Rear LAN+USB3.1 GEN1	
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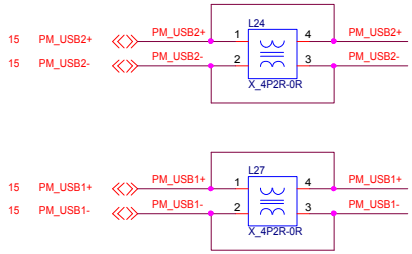
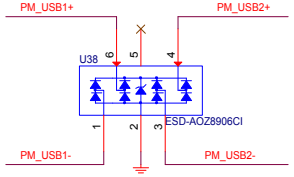
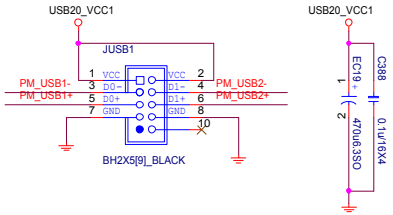
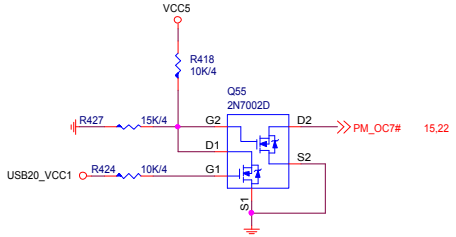
Front USB2.0



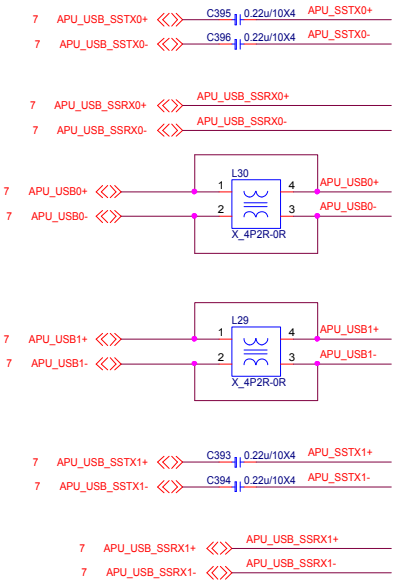


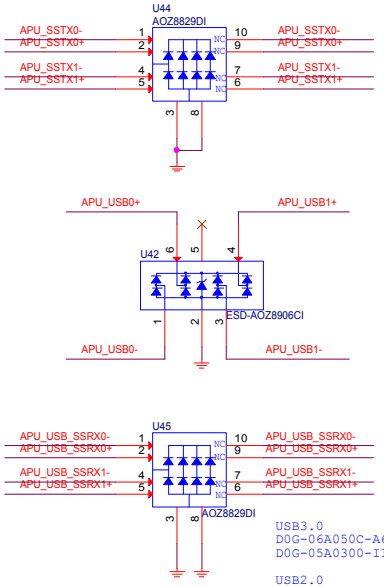


2017/3/16
R864 is changed from10Kohm to 300Kohm by MOS maybe turn on



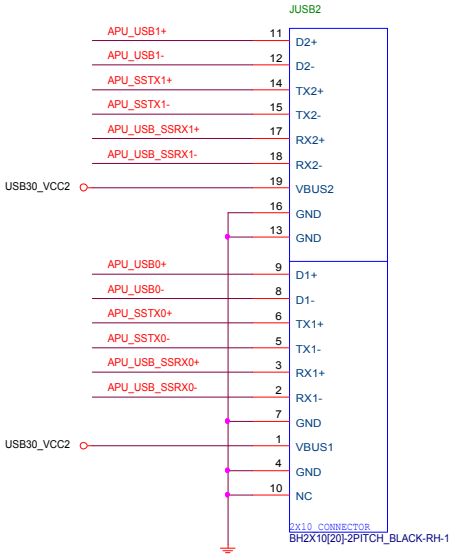
Front USB3.1 GEN1

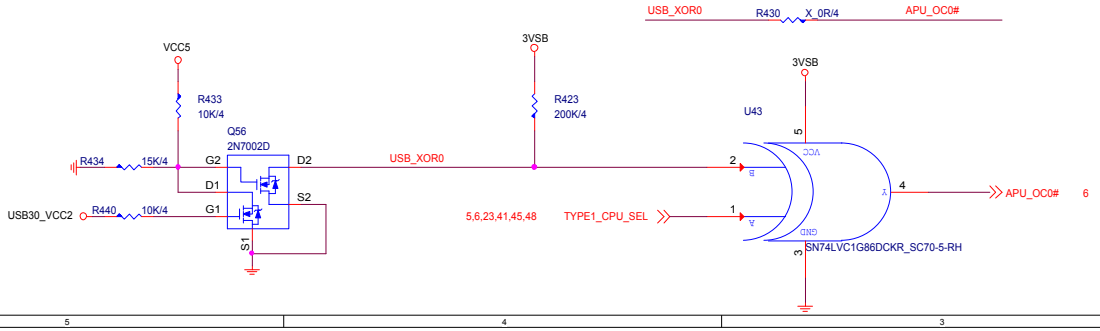


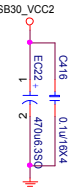


USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL







MICRO-START INT'L CO.,LTD.

Title: USB Front Side		
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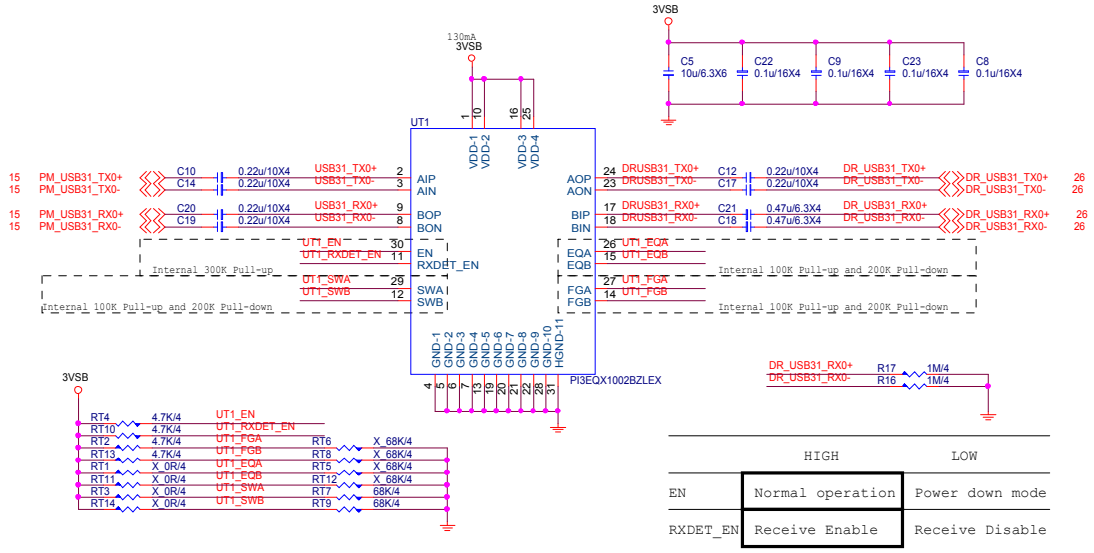

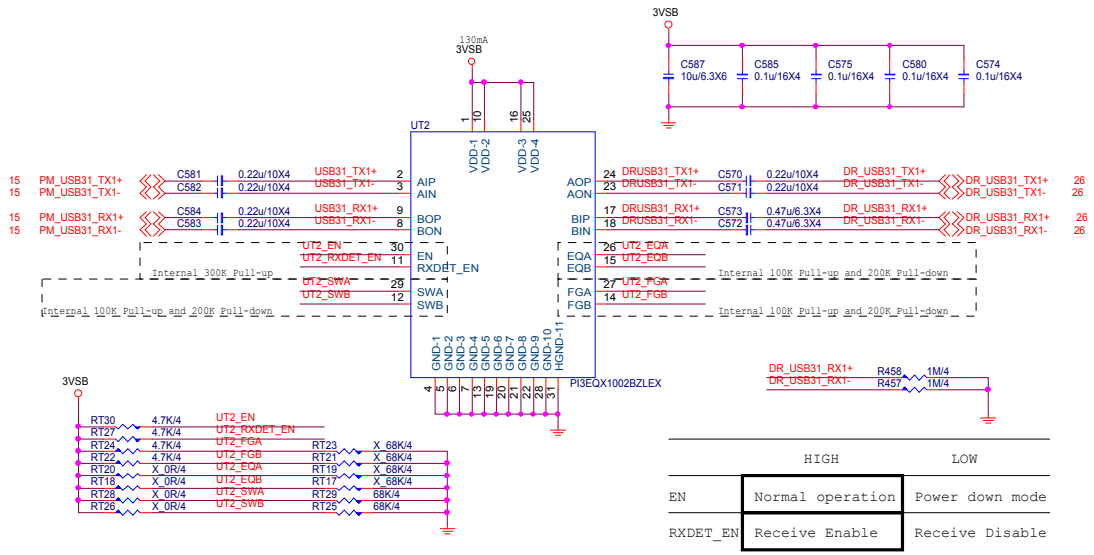

EQA/B are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B	*@2.5GHz*	*@5GHz*
0	5.1	10.9
R	1.9	6.7
F	3.5	8.9 (Default)
1	6.8	13.1

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

	Flat Gain Settings
FGA/B	*dB*
0	-3
R	-1.5
F	0 (Default)
1	+2

-1dB compression point linear Swing Setting:

SWA/B are the selection bits for the output linear swing setting

	Output Linear Swing Settings
SWA/B	*mVppd*
0	800
R	1200
F	1000 (Default)
1	1100

MICRO-STAR INT'L CO.,LTD

USB 3.1 Gen2 redriver

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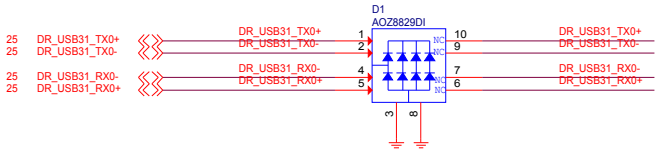

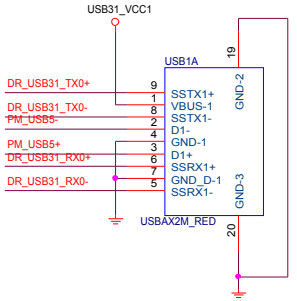

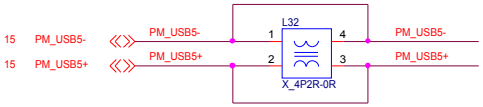

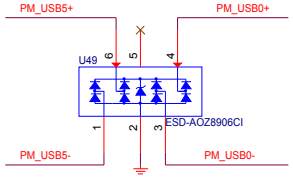

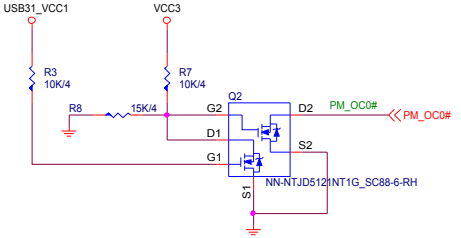

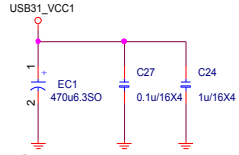

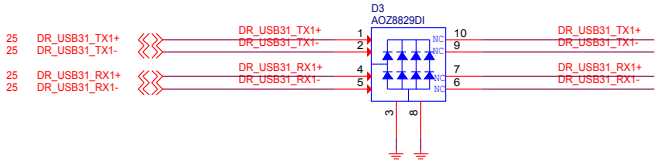

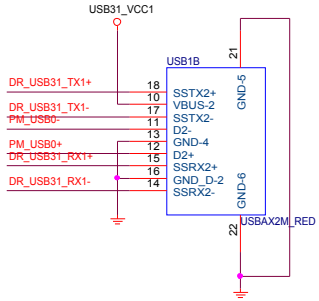

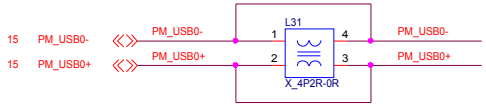

MICRO-STAR INT'L CO.,LTD

USB 3.1 GEN2 TYPE A*2

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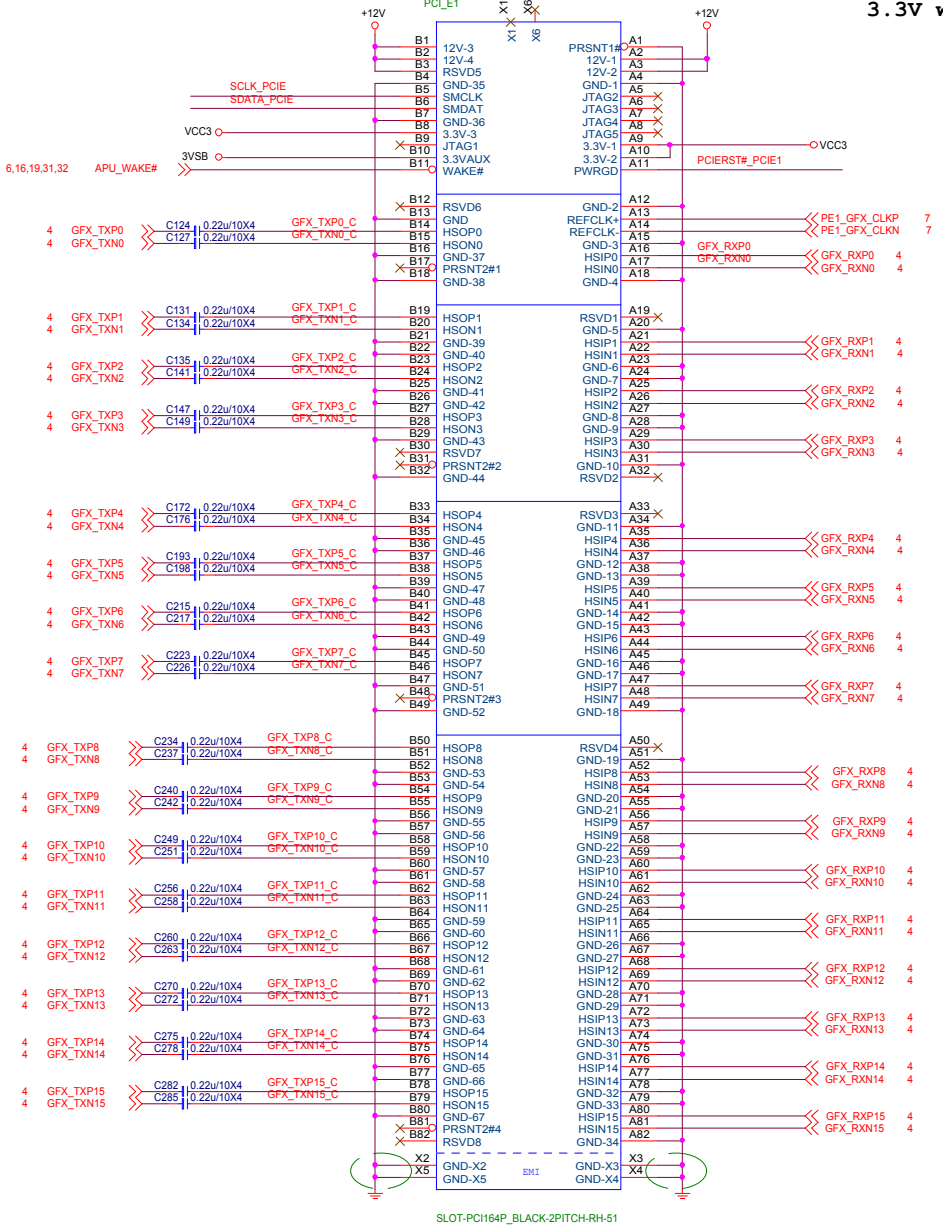
PCI EXPRESS x16 Slot

3.3V 3.0A
12V 5.5A

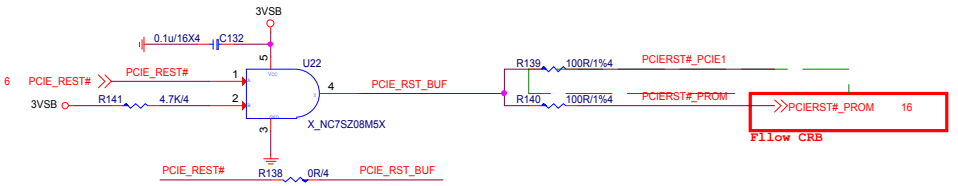
PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V 3.0A
12V 0.5A

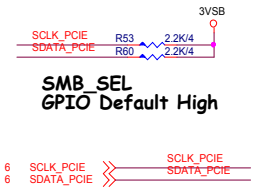


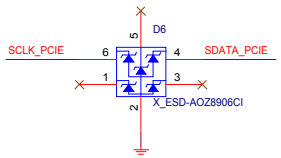
Remove PCIe x1 Slot

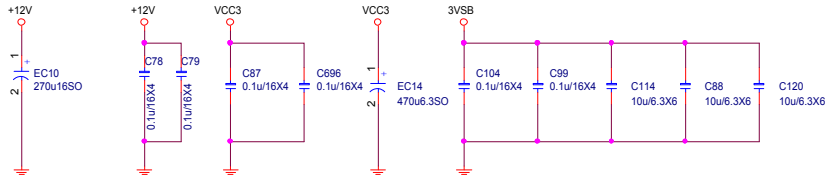
within 500mil



SMBus separate circuit







MICRO-START INT'L CO.,LTD.

Title	PCIE X16(X1*2) SLOT	
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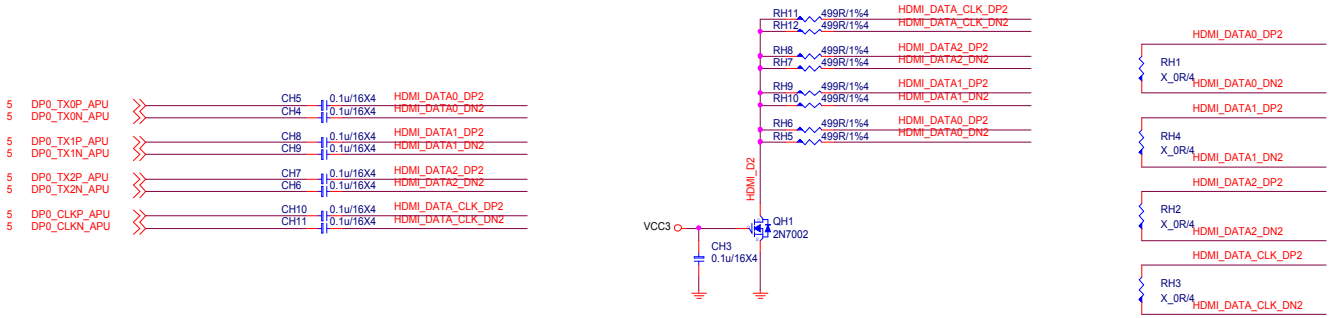
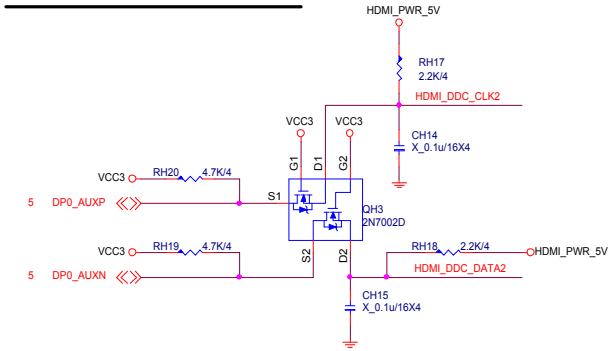
HDMI CONNECTOR

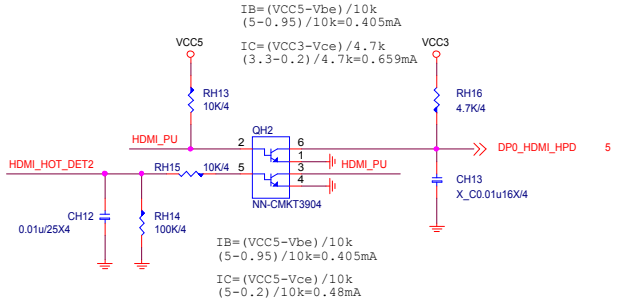
For HDMI 1.4



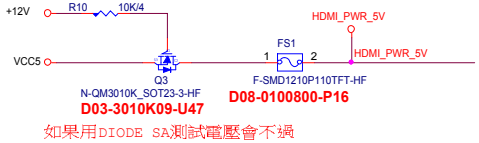
AUX Level Shifter



HPD Circuit

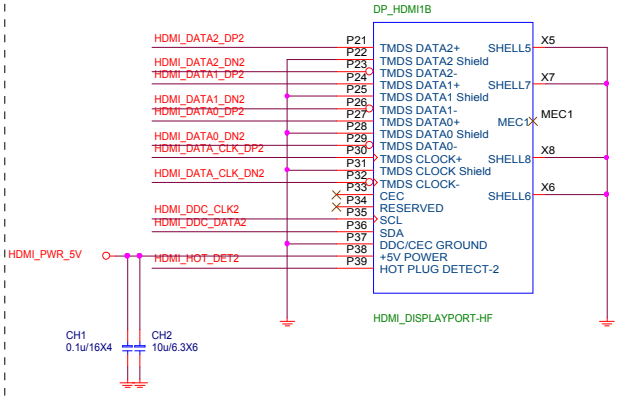


Connector Power

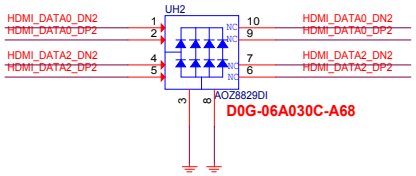


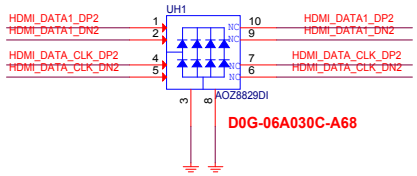
如果用DIODE SA測試電壓會不過

Connector

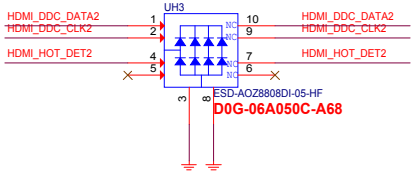


For EMI





注意:耐壓5V零件



MSI MICRO-START INT'L CO.,LTD.

Link to the Future

Title: HDMI Connector		
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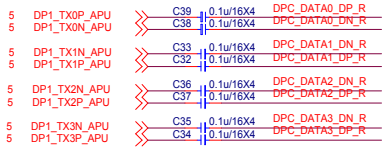
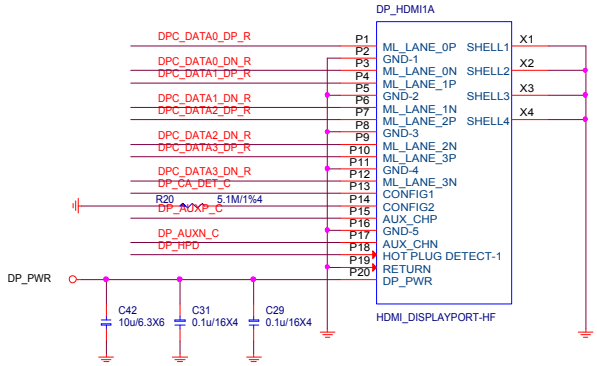
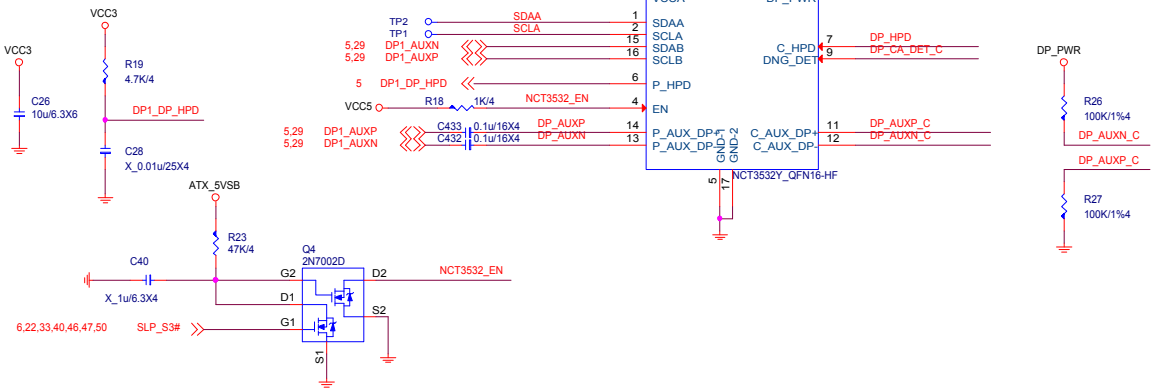
DP CONNECTOR



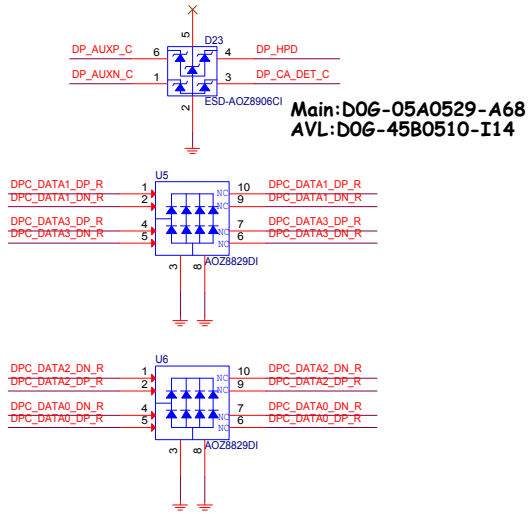


DP AUX & HPD Circuit

Support HDMI Dongle



ESD



MICRO-STAR INT'L CO.,LTD.

Title: DP Connector

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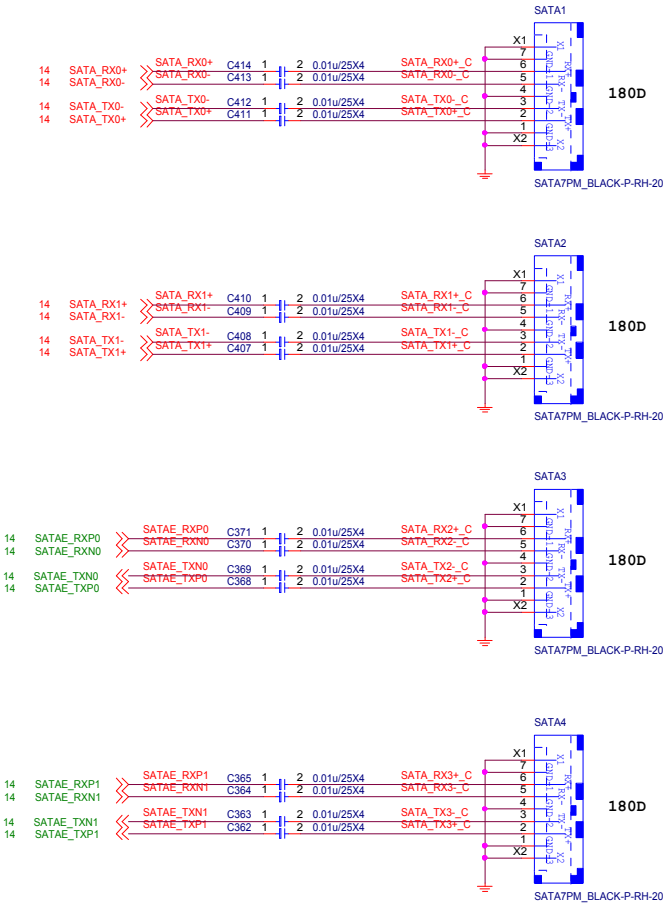
SATA Connector



Title	SATA Connector
Size	Custom
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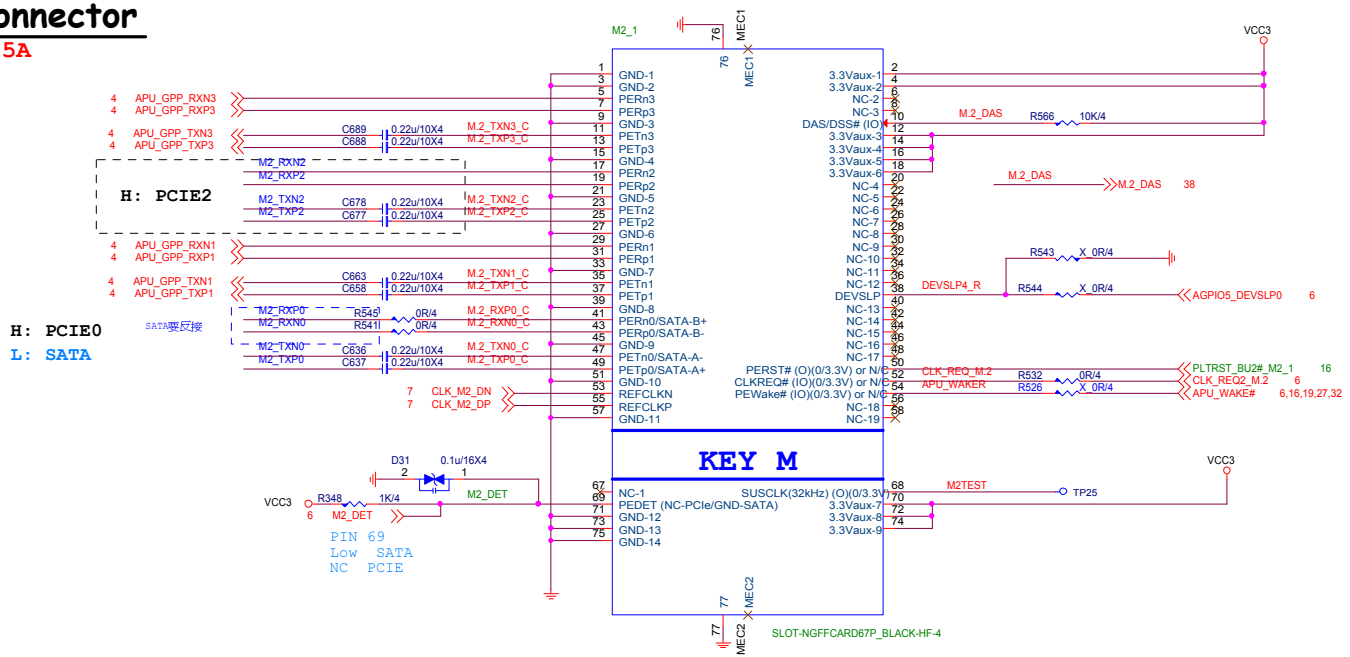
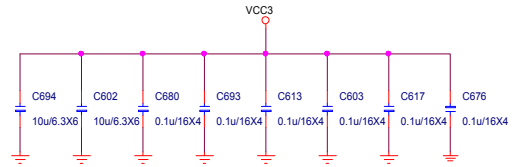
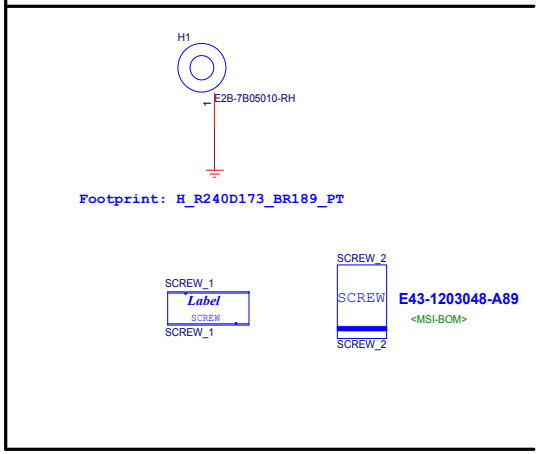
Link to the Future

M.2 Connector

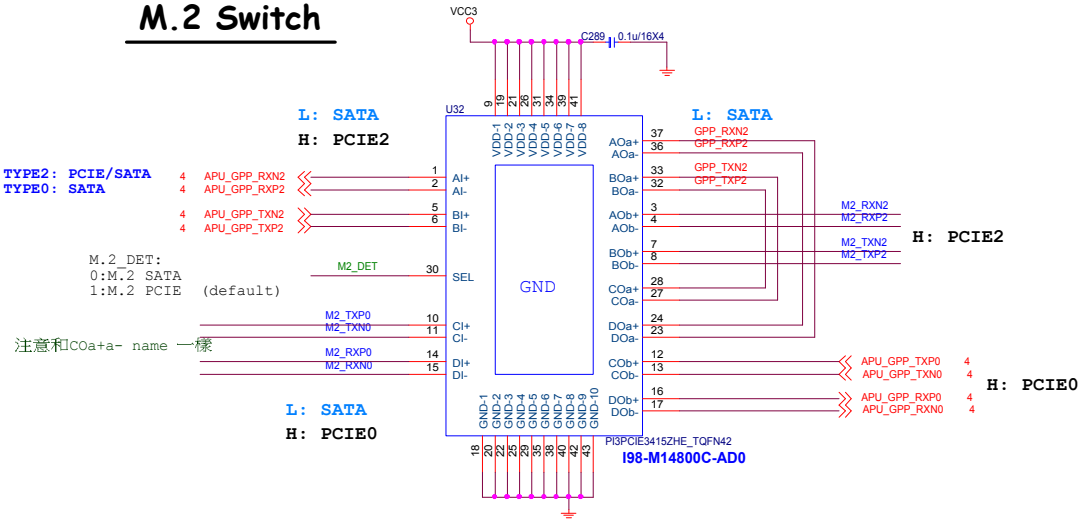
3.3V@2.5A

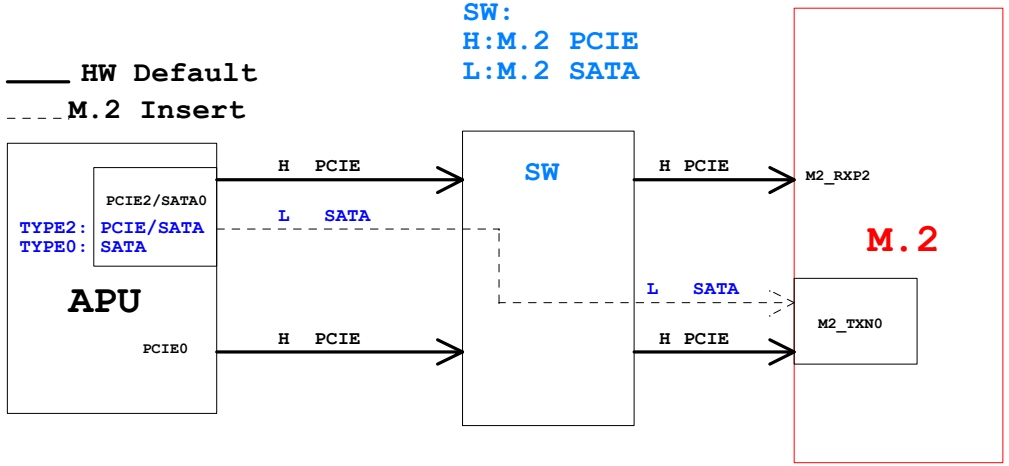






M.2 Switch





MSI MICRO-STAR INTERNATIONAL Link to the Future MICRO-START INT'L CO.,LTD.			
Title: M.2 Connector			
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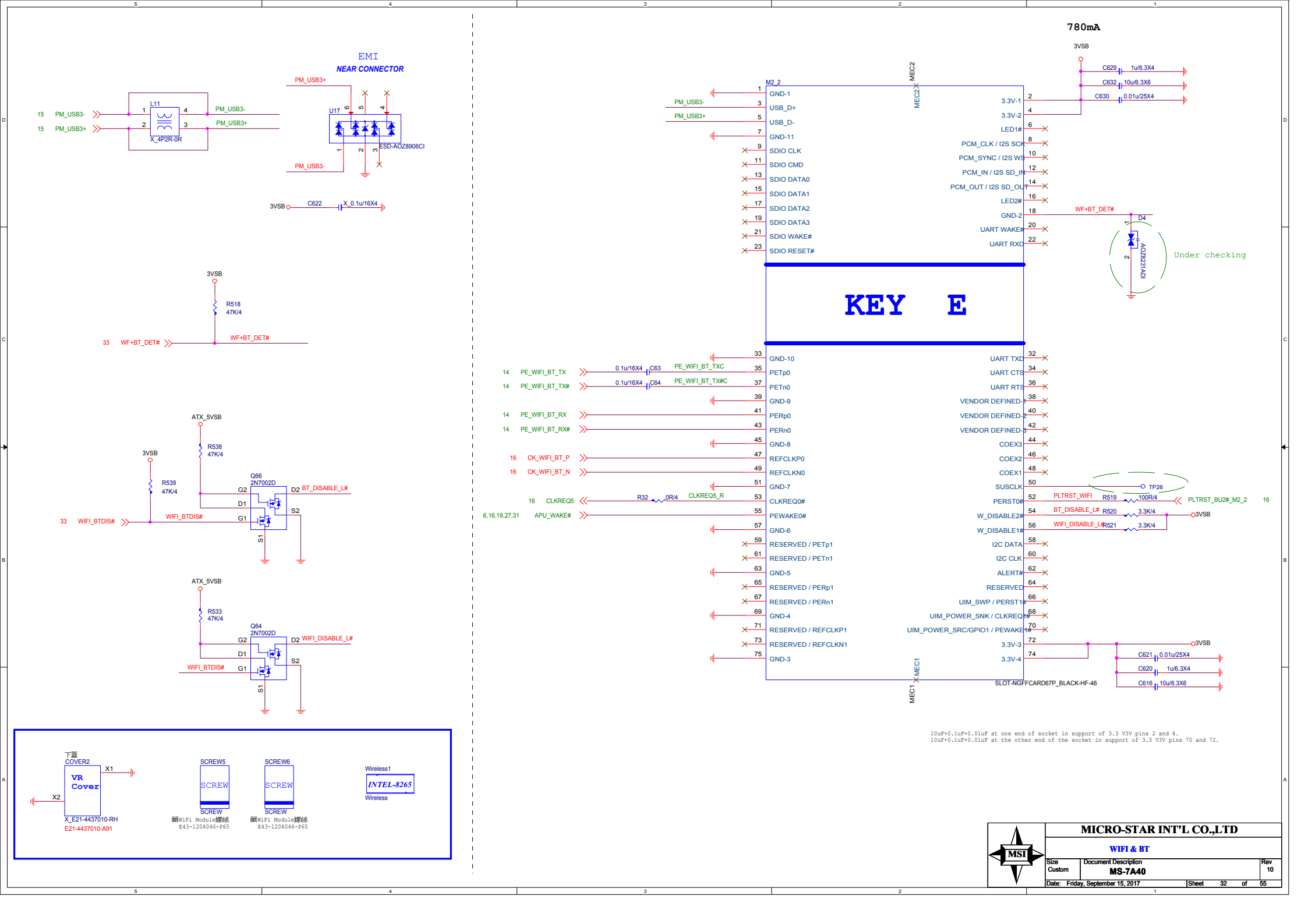

MICRO-STAR INT'L CO.,LTD	
WIFI & BT	
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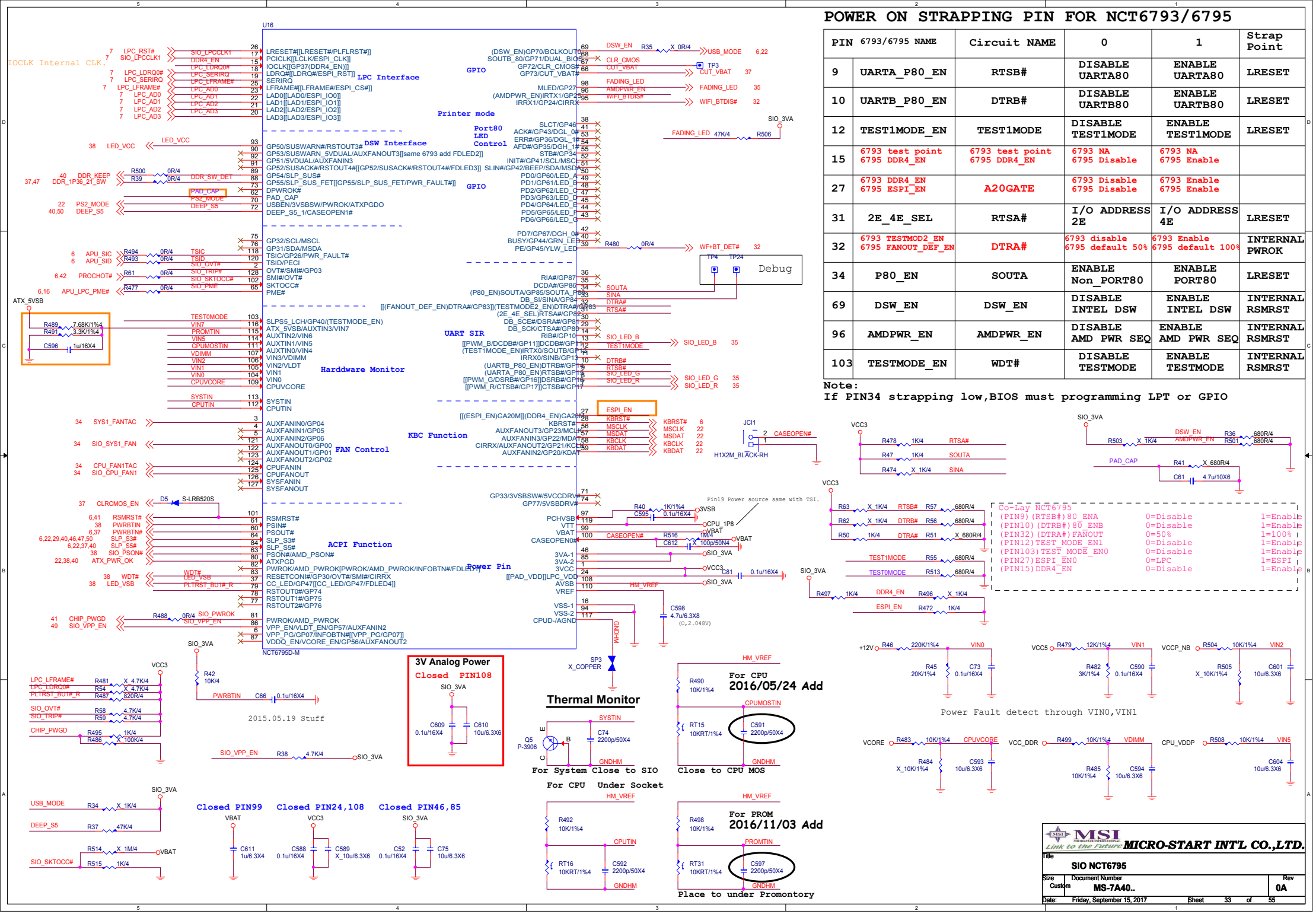

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Co-Lay NCT6795

(PIN9)(RTSB#)80_ENA	0=Disable	1=Enable
(PIN10)(DTRB#)80_ENB	0=Disable	1=Enable
(PIN32)(DTRA#)FANOUT	0=50%	1=100%
(PIN12)TEST_MODE_EN1	0=Disable	1=Enable
(PIN103)TEST_MODE_EN0	0=Disable	1=Enable
(PIN27)ESPI_EN0	0=LPC	1=ESPI
(PIN15)DDR4_EN	0=Disable	1=Enable

MICRO-START INT'L CO.,LTD.

Title	SIO NCT6795	
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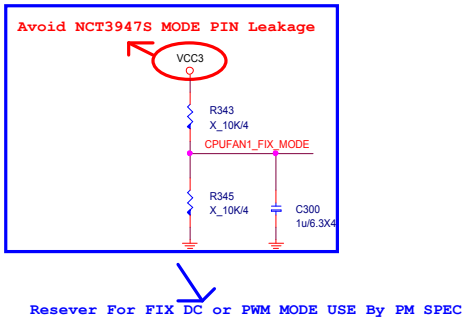
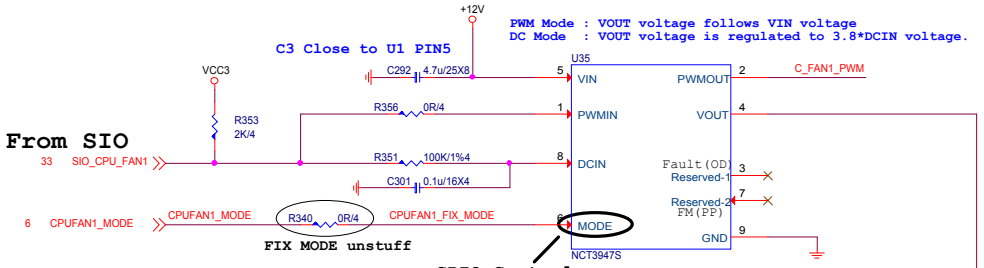
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE

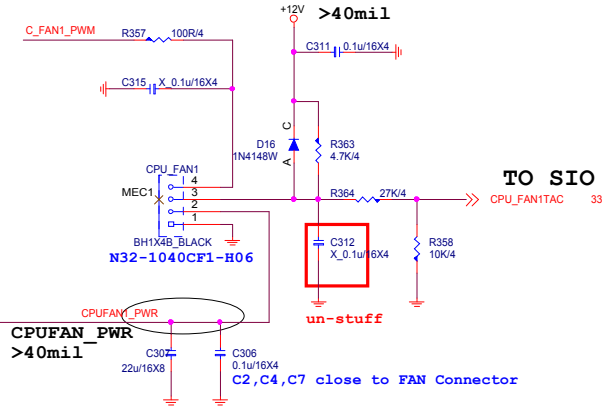


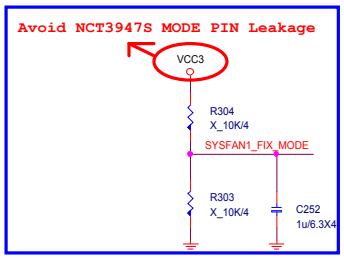
Resever For FIX DC or PWM MODE USE By PM SPEC



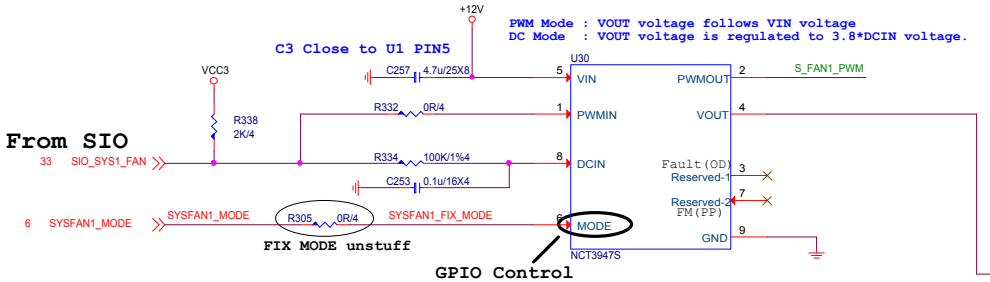
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



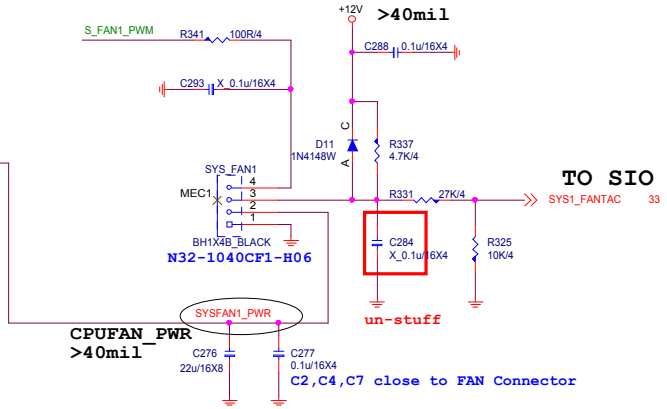


Resever For FIX DC or PWM MODE USE By PM SPEC



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



MSI MICRO-STAR INT'L CO.,LTD.

Link to the Future

Title: CPU FAN Control		
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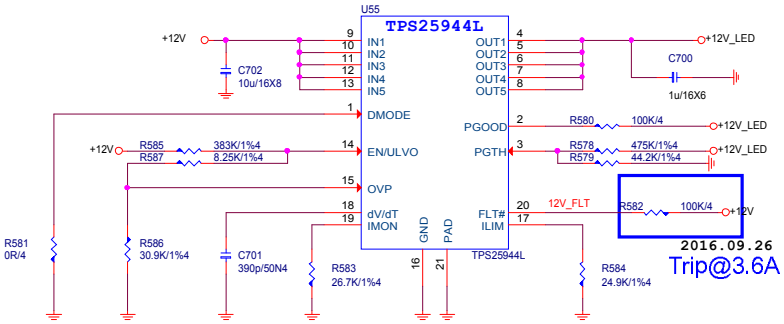
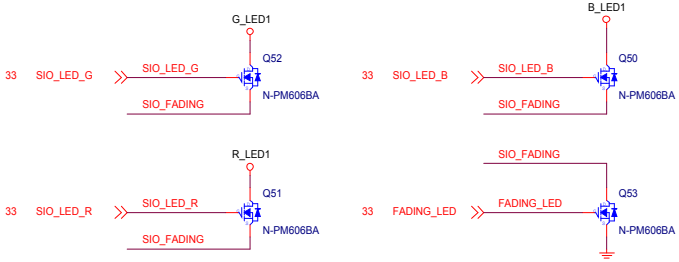
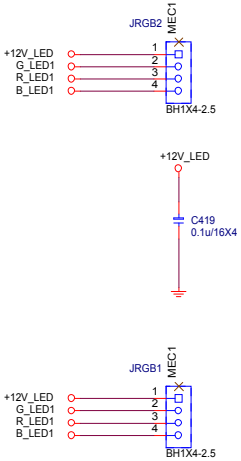
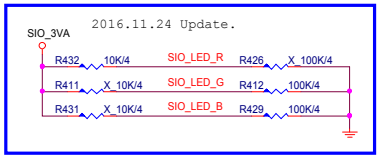
定義:外接LED 燈條
---- 彩色 : SIO 6795D-M(128pin) : OB2-7A58001
---- 單色 : SIO 5565(64pin) : B02-5565D04-N62
---- PCB 文字面 (JLED)
---- 手冊 註明接頭支援標準 5050 RGB or 單色 LED 共陽燈條 (12V+/G/R/B) or (12V+/-/S/-) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JLED



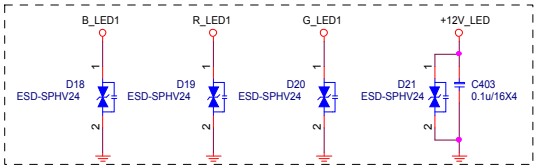




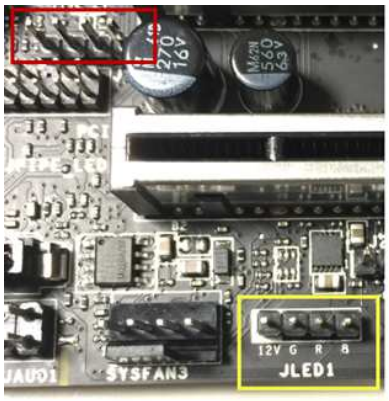


Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

2016.08.31 StuFF

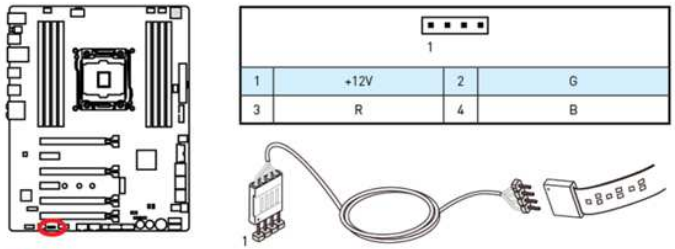


close to JLED2



JLED1: RGB LED connector

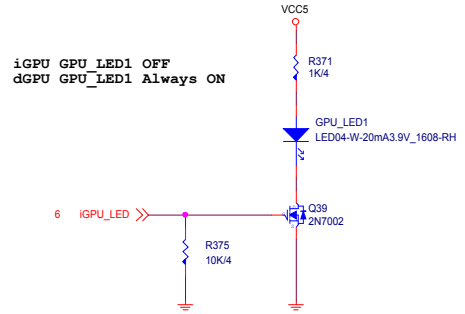
This connector allows you to connect the RGB LED strip.



Important

- *This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.*
- *Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.*
- *Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.*

AM4 APU Detect LED Circuit



MICRO-STAR INT'L CO.,LTD

6795 RGB LED

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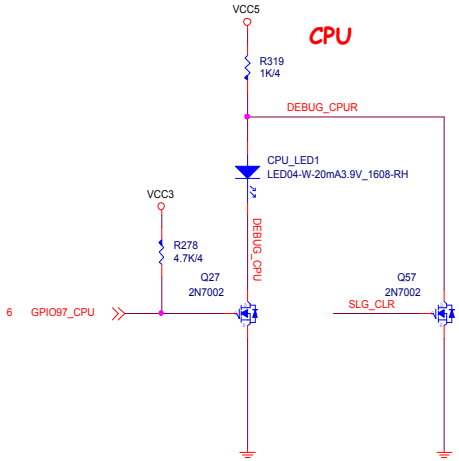
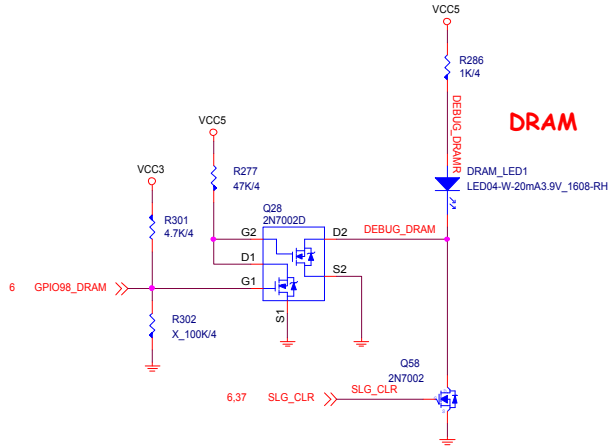
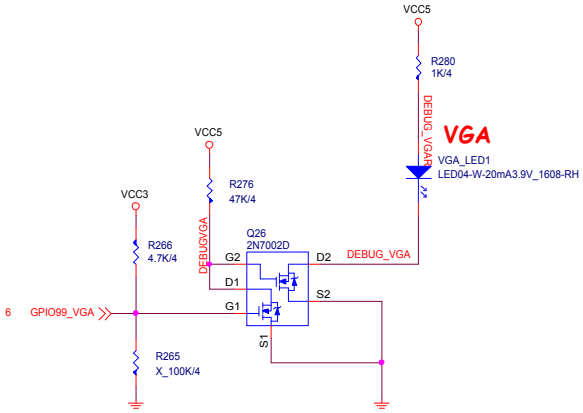
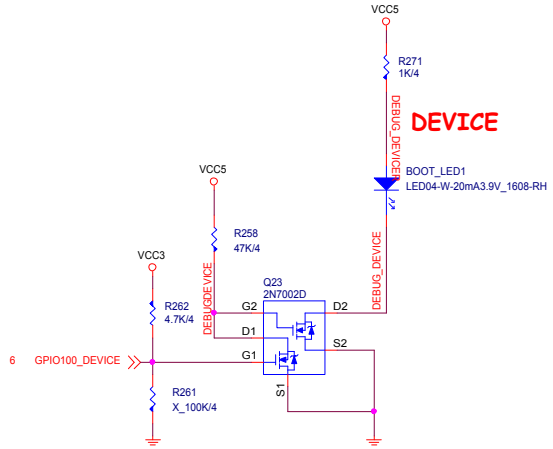
EZ Debug LED









LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

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Link to the Future

Title: DVI Connector		
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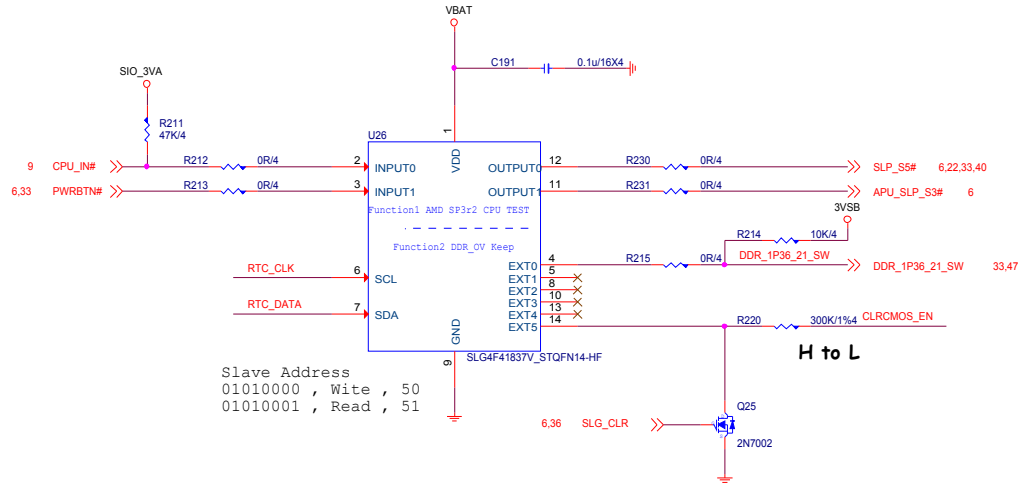
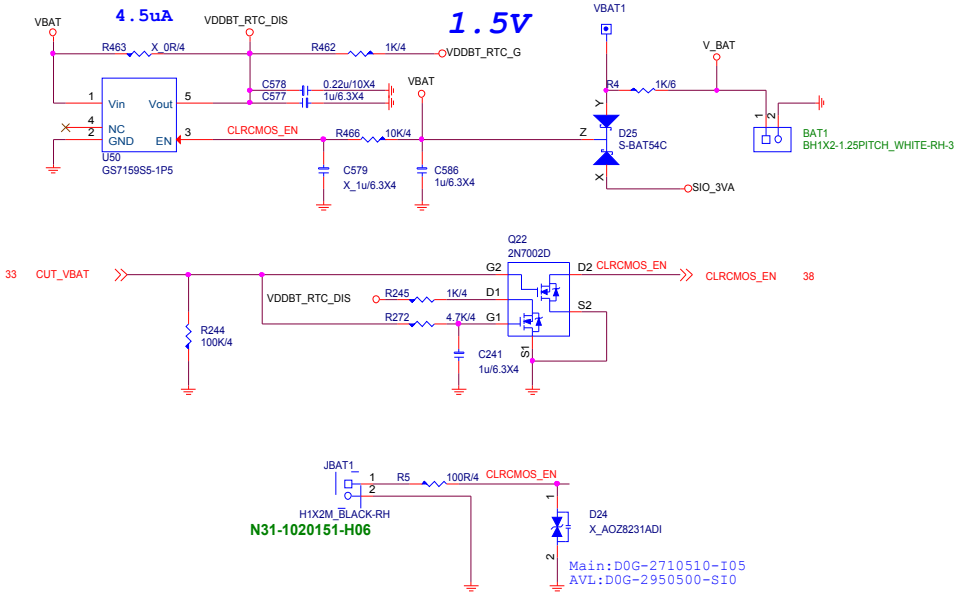
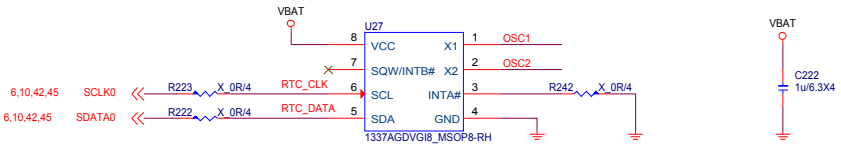


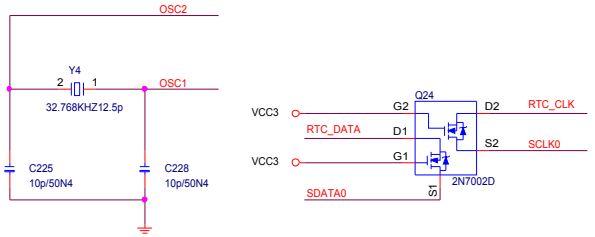
RTC & Clear CMOS Circuit

Placement Bottom Side





Slave Address:
11010000 , Wite , D0
11010001 , Read , D1



MICRO-START INT'L CO.,LTD.

Title: RTC Circuit		
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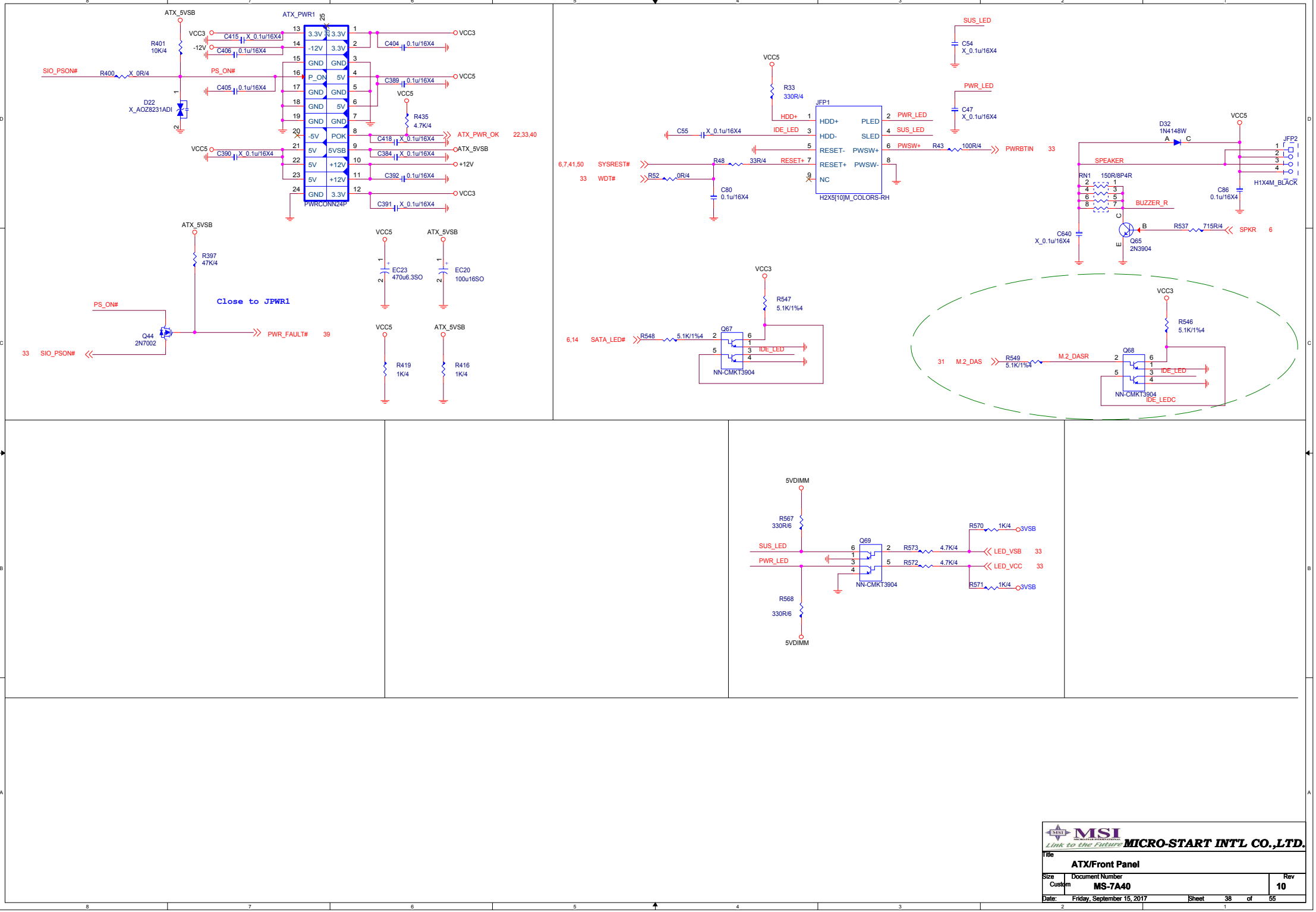

MICRO-START INT'L CO.,LTD.

Link to the Future

Title	ATX/Front Panel	
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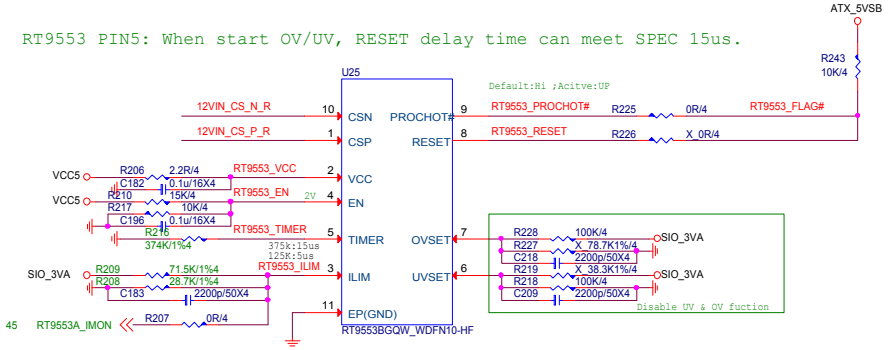
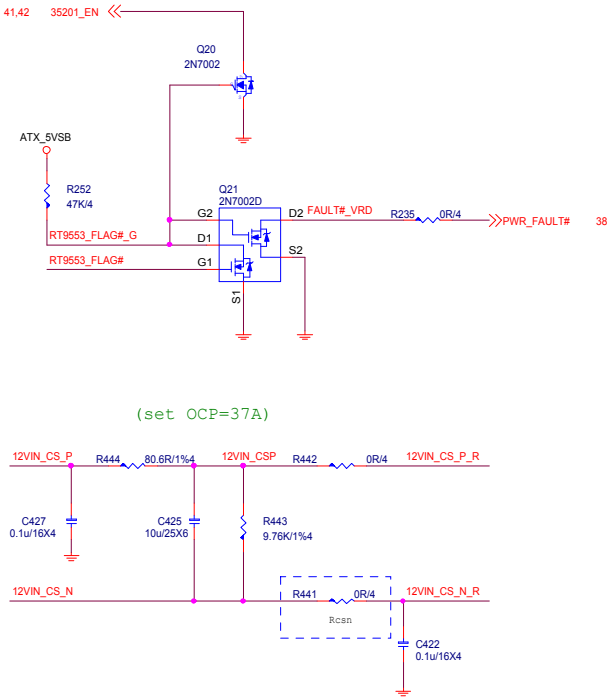
RT9553B CURRENT SENSE

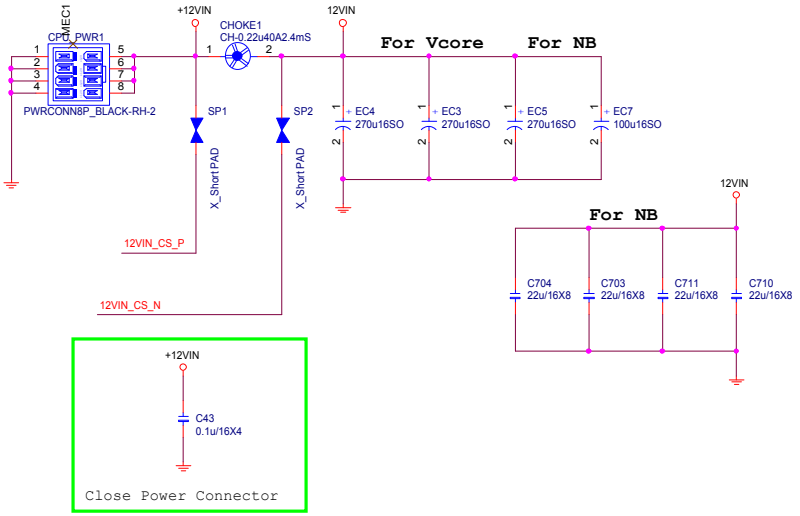
VCORE EDC MAC 125A

NB EDC MAX75A





CPU POWER CONNECTOR



D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.5	> output Vcore
D	=	0.125	

I o = Icore(max)*0.8			
I core(max)	=	125	> Vcore current
I avg.	=	100	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	4 6	phase
I ripple	=	[illegible]	A

5.511982

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

CORE:
D = Vout/Vin
= 1.5/12
= 0.125
N = 6
Irms = Iout * [D/N - (D)^2]^(1/2)
= 125 * (0.02083 - 0.015625)^(1/2)
= 9.0182A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.2	> output Vcore
D	=	0.1	

I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	9	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

NB:
D = Vout/Vin
= 1.2/12
= 0.1
N = 2
Irms = Iout * [D/N - (D)^2]^(1/2)
= 75 * (0.05 - 0.01)^(1/2)
= 15A

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Title			
uP6273 CURRENT SENSE			
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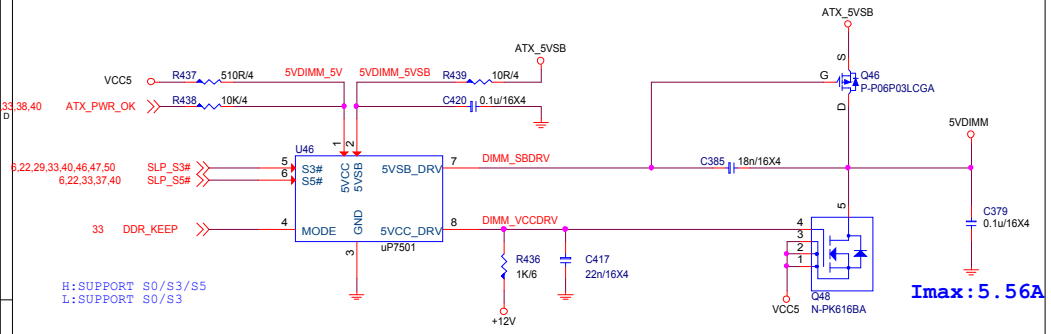
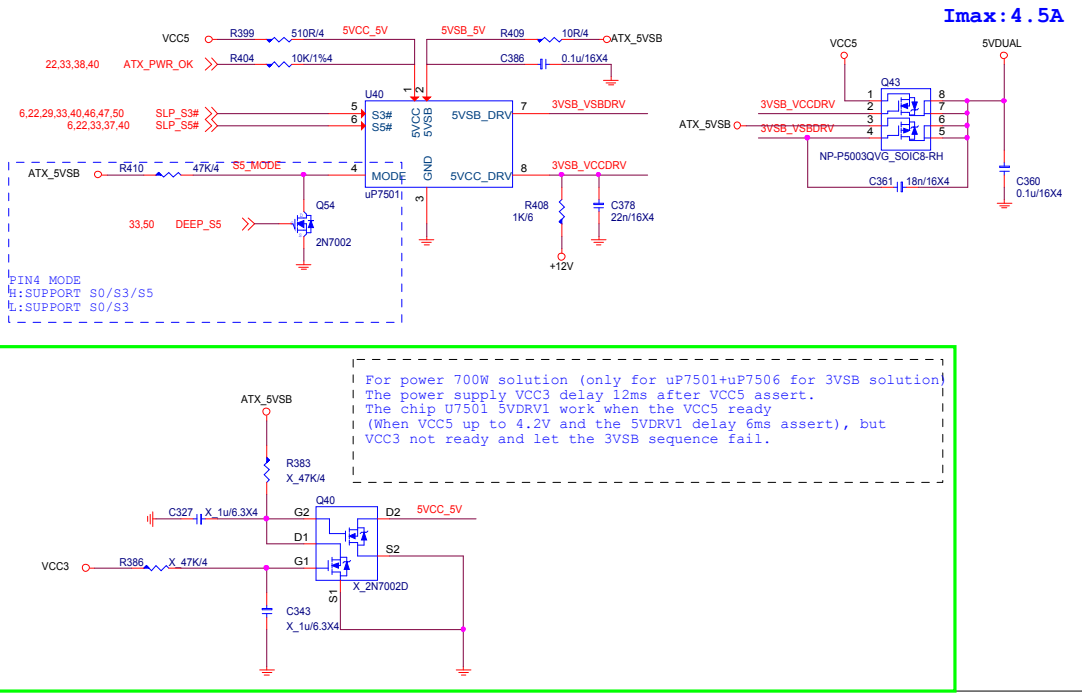
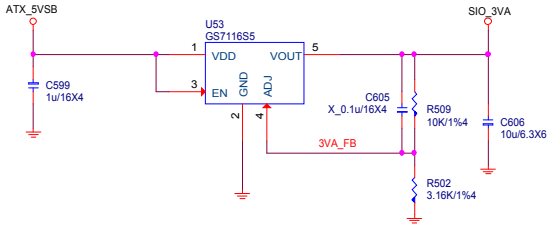
5VDIMM FOR DDR



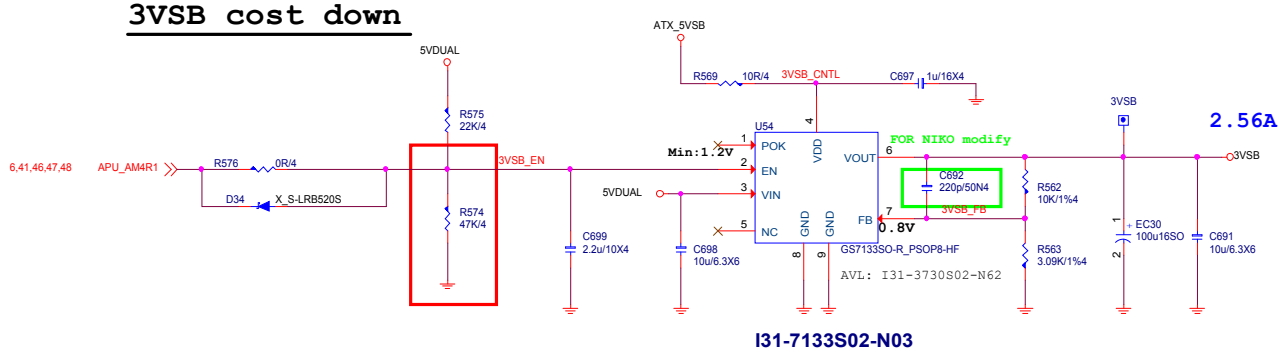
5VDUAL For 3VSB、CPU 1.8V 、 VDDP



SIO_3VA



3VSB cost down



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Title	ACPI uPI-5VDIMM&3VSB	
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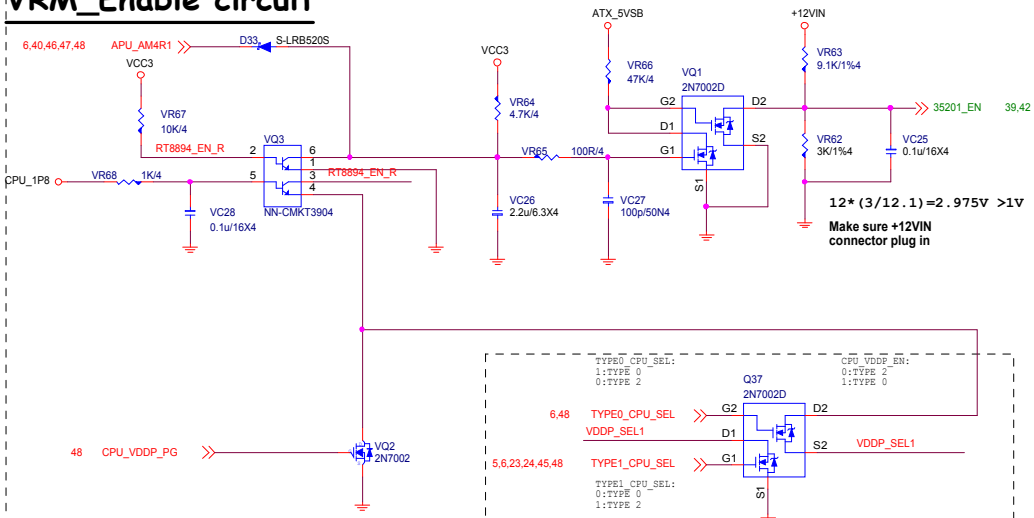
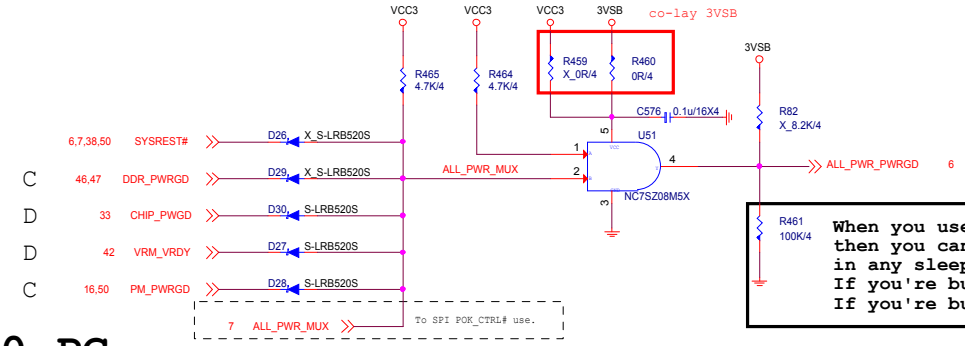
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

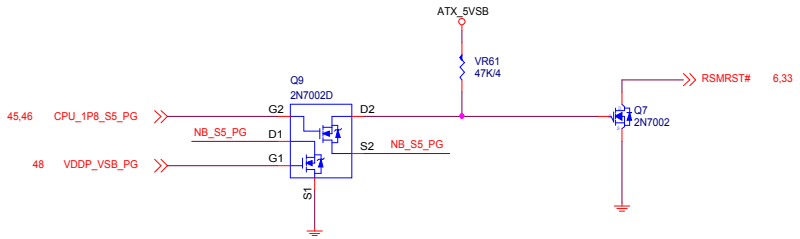
ALL POWER GOOD MUX



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



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Link to the Future

Title	CPU PWR-IR3599		
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Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vcore: ICC Max 125A
LL: 1.3 mohm
OCP: 225A

SOC: ICC Max 75A
LL: 2.1 mohm
OCP: 90A

CPU_1P8 — VR39 1K/4, VR32 1K/4, VR44 1K/4, VR59 2.2K/4 — design check

6 APU_SVC — VR36 0R/4 — VRM_SVC
6 APU_SVD — VR30 0R/4 — VRM_SVD
6 APU_SVT — VR49 0R/4 — VRM_SVT
6 APU_PWROK — VR60 0R/4 — VRM_POK

VR37 X_220R4, VR33 X_220R4, VR42 X_220R4

VCC3 — VR58 10K/4 — VRM_VRDY
V35201 — VR29 1K/4 — VR_HOT#

JSMB1: SCLK0, SDATA0 — H2X2[4]M_BLACK-RH

VC8 22p/50N4, VC10 22p/50N4 — SCLK_35201, SDATA_35201

VCC3, 3VSB — VR4 0R6, VR3 X_0R6 — V35201 Close IC — VC2 1u/6.3X6, VC4 0.1u/16X4

VU1 — VCC (38)

12VIN — VR54 13K/1%4, VR53 1K/1%4, VC20 0.1u/16X4 — VINSEN (14)
VR47 0R/4 — I_IN (8)

39,41 35201_EN — VR25 0R/4 — VRMEN — EN (21)
VRM_POK — EN_L2/PWROK/CAT_FLT (12)

41 VRM_VRDY — VR40 0R/4 — VRDY1 (11)
VR50 0R/4 — VRDY2 (4)

6,33 PROCHOT# — VR28 10K/4 — VR_HOT# — VRHOT_ICRIT# (20)

6,10,37,45 SCLK0 — VR19 0R/4 — SCLK_35201 — SM_CLK (25)
6,10,37,45 SDATA0 — VR18 0R/4 — SDATA_35201 — SM_DIO (24)
V35201 — VR23 4.7K/4 — SMBALERT_35201 — SM_ALERT# (23)
VR24 845R/1%4, VC13 0.01u/25X4 — SM_ADDR — ADDR_PROT (22)

VRM_SVC (18) — SV_CLK
VRM_SVD (19) — SV_DIO
VRM_SVT (17) — SV_ALERT#/SVT
CPU_1P8 — VR55 10R/4 — SV_ADDR — VC21 0.01u/25X4 — SV_ADDR/VDDIO (16)

V35201 — VR16 4.7K/4 — PIN_ALERT# — PIN_ALERT# (26)

VRM_V18A — VC19 1u/16X6, VC24 0.47u/6.3X4 — Close IC — CFILT (10)

VCORE — VR52 100R/1%4 — VR57 0R/4 — VSEN_CORE — VC23 3300p/50X4 — VSEN (5)
6 VDDCR_CPU_SENSE+
Diff pair
6 VDDCR_CPU_SENSE- — VR56 0R/4 — VR51 100R/1%4 — VRTN_CORE — Close IC — VRTN (6)

VCCP_NB — VR7 100R/1%4 — VR6 0R/4 — VSEN_SOC — VC3 3300p/50X4 — VSEN_L2 (37)
6 VDDCR_SOC_SENSE+
Diff pair
6 VDDCR_SOC_SENSE- — VR5 0R/4 — VR10 100R/1%4 — VRTN_SOC — Close IC — VRTN_L2 (36)

Close CPU

VIN | Ctrl | Loop 1 | SMB | SVID | VSEN | Loop 2

NC-1 (7), NC-2 (13), NC-3 (15), NC-4 (41), GND (57)

IR35201-R4

SMB Address: 0X70

Phase 1 close to CPU power pin.

PWM1 (28)	VCORE_ISEN1_R — VR38 10K/1%4, VC16 100p/50N4, VR34 2.49K/1%4	ISEN1 (54) — IRTN1 (55)
PWM2 (29)	VCORE_ISEN2_R — VR35 10K/1%4, VC15 100p/50N4, VR31 2.49K/1%4	ISEN2 (52) — IRTN2 (53)
PWM3 (30)	VCORE_ISEN3_R — VR27 10K/1%4, VC14 100p/50N4, VR26 2.49K/1%4	ISEN3 (50) — IRTN3 (51)
PWM4 (31)	VCORE_ISEN4_R — VR20 10K/1%4, VC12 100p/50N4, VR22 2.49K/1%4	ISEN4 (48) — IRTN4 (49)
PWM5 (32)	VCORE_ISEN5_R — VR15 10K/1%4, VC11 100p/50N4, VR21 2.49K/1%4	ISEN5 (46) — IRTN5 (47)
PWM6 (33)	VCORE_ISEN6_R — VR48 10K/1%4, VC18 100p/50N4, VR41 2.49K/1%4	ISEN6 (1) — IRTN6 (56)

VCROE_PWM1..6 (43) — VCORE_ISEN1..6 — VCORE_IRTN1..6

RCSP (2) — VCORE_RCSP — Close IC — VC17 68p/50N4, VR43 10.5K/1%4 — VCORE_RCSM — RCSM (3)

TSEN1 (9) — VCORE_TSEN_R — VR46 6.49K/1%4, VR45 10K/1%4, VC22 100p/50N4 — VCORE_TSEN (43)

PWM8/PWM1_L2 (35) — VNB_PWM1 (44)
ISEN8/ISEN 1_L2 (42) — VNB_ISEN1_R — VC5 100p/50N4, VR8 10K/1%4, VR14 2.49K/1%4 — VNB_ISEN1 (44)
IRTN8/IRTN 1_L2 (43) — VNB_IRTN1 (44)

PWM7/PWM2_L2 (34) — VNB_PWM2 (44)
ISEN7/ISEN 2_L2 (44) — VNB_ISEN2_R — VC9 100p/50N4, VR13 10K/1%4, VR17 2.49K/1%4 — VNB_ISEN2 (44)
IRTN7/IRTN 2_L2 (45) — VNB_IRTN2 (44)

Close IC

RCSP_L2 (40) — VNB_RCSP — VC6 47p/50N4, VR11 16.9K/1%4 — VNB_RCSM — RCSM_L2 (39)

TSEN2/VAUXSEN (27) — VNB_TSEN_R — VR9 6.49K/1%4, VR12 10K/1%4, VC7 100p/50N4 — VNB_TSEN (44)

0x26:RH=18K,RL=13K

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

VCORE_IRTN1 CP7, VCORE_IRTN2 CP6, VCORE_IRTN3 CP5, VCORE_IRTN4 CP4, VCORE_IRTN5 CP3, VCORE_IRTN6 CP8, VNB_IRTN1 CP1, VNB_IRTN2 CP2 — X_COPPER — VRM_VREF

20170410

防SS下漏電到VCC5

VR1 X_0R/4 — VRQ1 N-PM606BA — VR2 0R/4 — VRM_VREF
VRM_V18A
VC1 0.1u/16X4
12VIN

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Title	CPU Power-IR35201 6+2 Phase		
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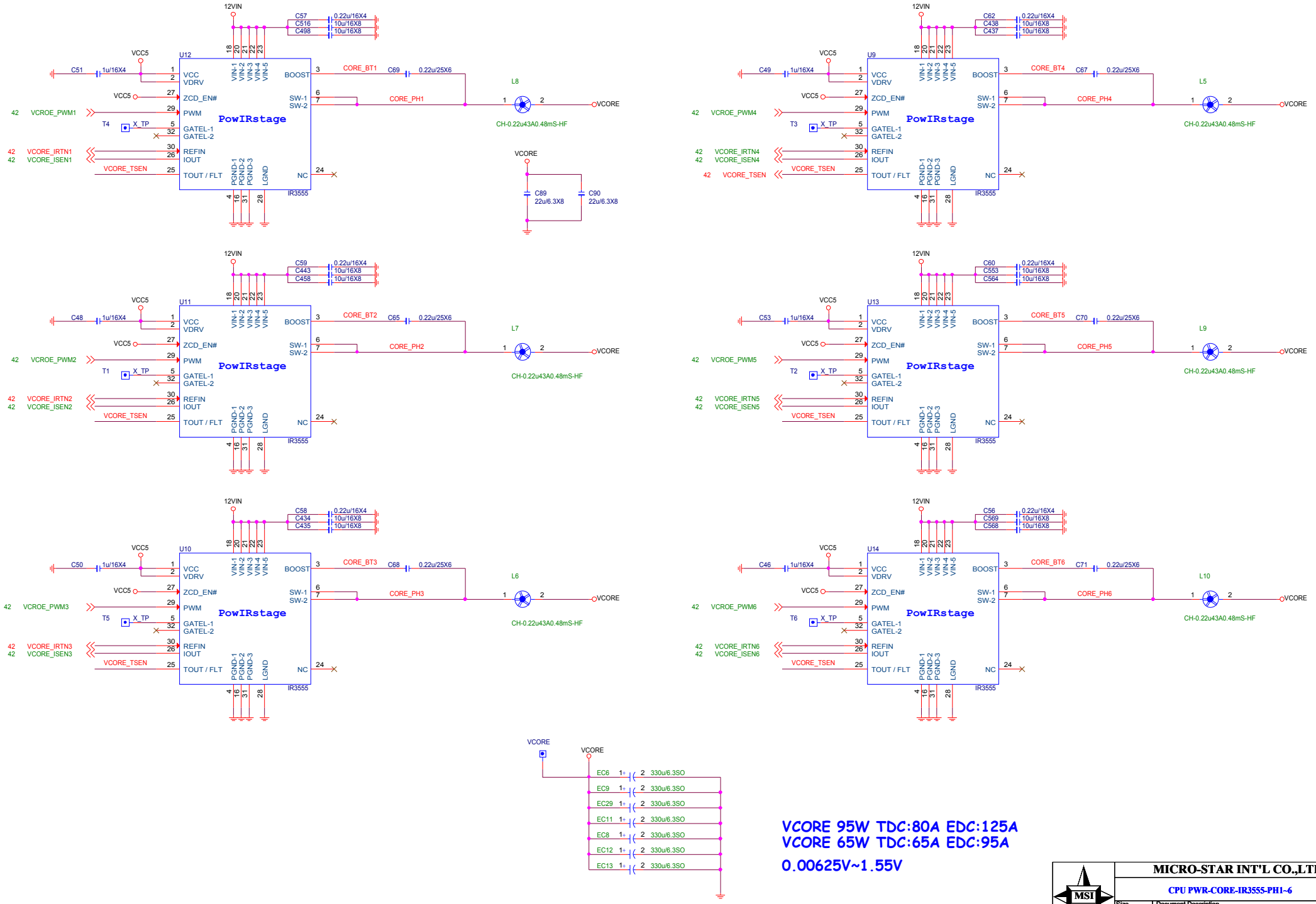

MICRO-STAR INT'L CO.,LTD		
CPU PWR-CORE-IR3555-PH1~6		
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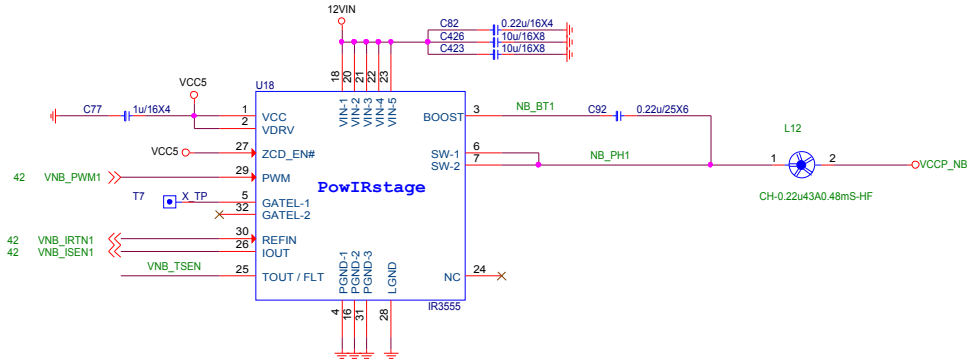
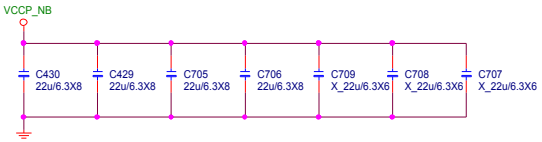
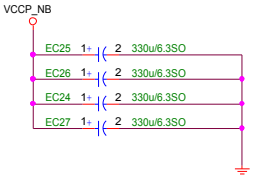
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

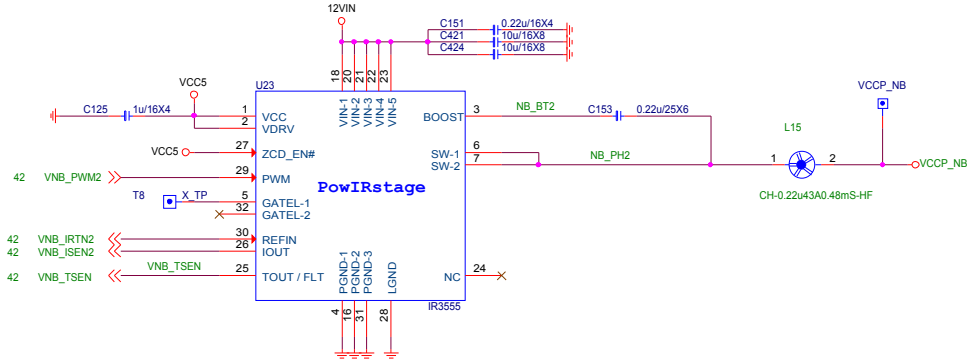
VCCP_NB OCP:100A



0.00625V~1.55V







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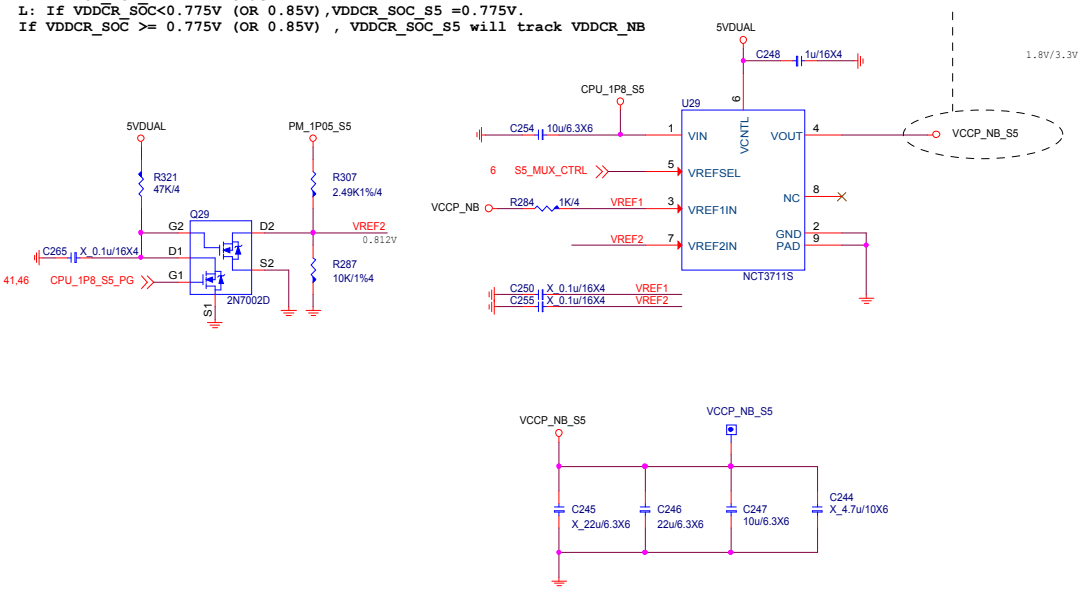
FOR
VCCP_SOC_s5
0.9A

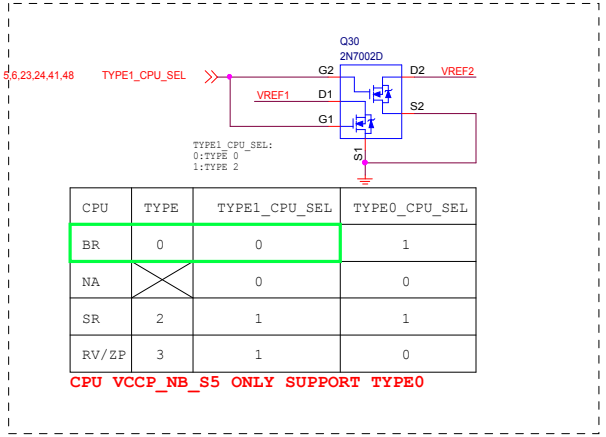
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0



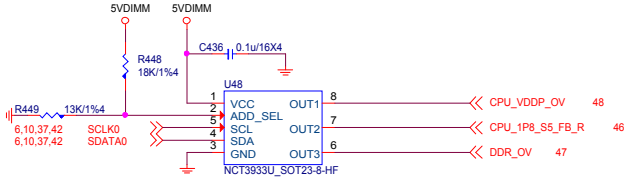


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

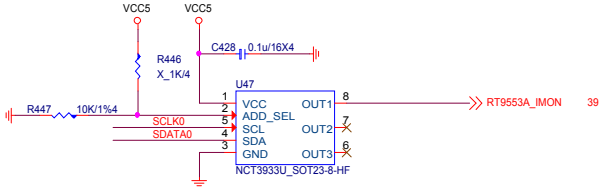
CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

0x26:RH=18K,RL=13K



0x2A:RH=OPEN,RL=10K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Title	CPU Power NB Switch / NCT3933 OV	
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FOR CPU 1.8V S5

0.5A

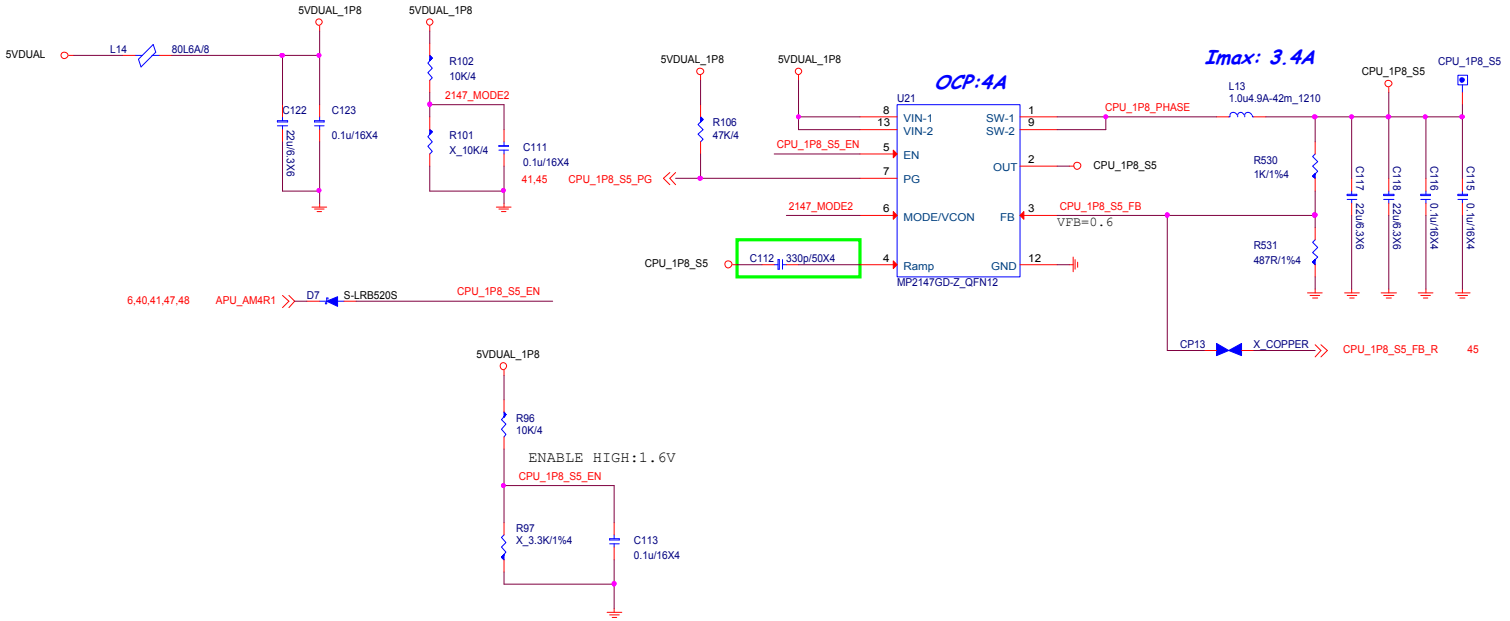
FOR VCCP_SOC_S5

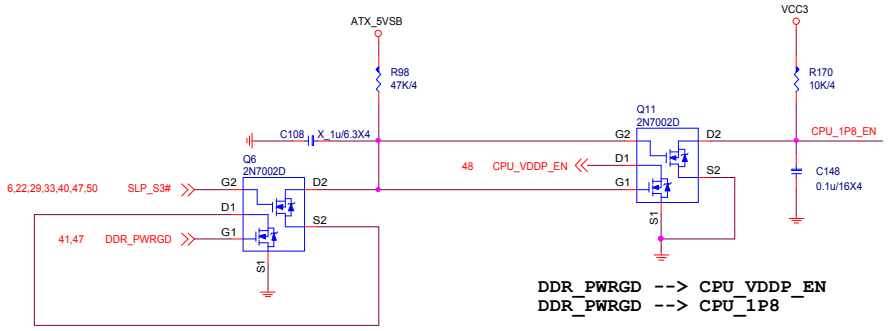
0.9A

FOR CPU 1.8V S0

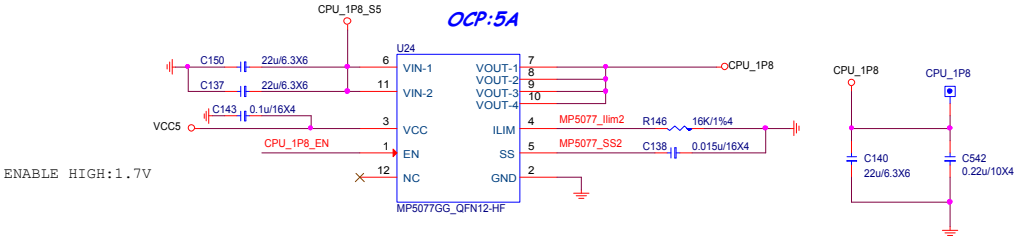
2.0A

0.5A + 2.0A + 0.9A =3.4A





DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



ENABLE HIGH:1.7V

```
Ilimit=(1/Rlimit)*S,S=80000,when VIN=1.8V
=(1/16)*80000=5.0375A

Tss=(1/3)*((Vout*Css)/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n)/9uA)=1mS
```

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Title	CPU Power 1P8V-MP2147	
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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM
0.6A FOR DDR VTT

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675 for 1.232V
L	0.75 for 1.369V

Imax: 20.85A

OCP:24A

By layout modify

f:400KHz

R178=90.9K for OCP(dc)=24A (typ)
and OCP(dc)=23.8A(min)

27.5A

FB:0.75V

Close to PIN19

I32-8231A0C-R11

default=1.36V

R195=1K, R181=1.21K,
Vo=0.75V*(1+R195/R181=1.369V

1.2V

1.1uH change to 0.47uH

0.1uFx1 per dimm

Title	DDR Power-RT8231AGQW
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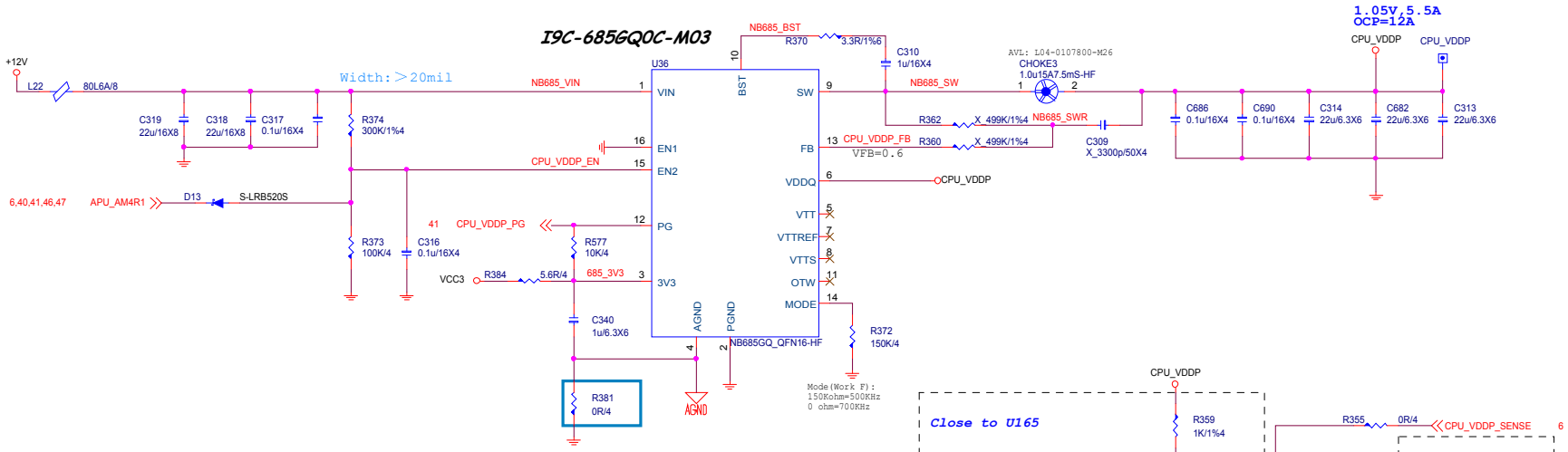
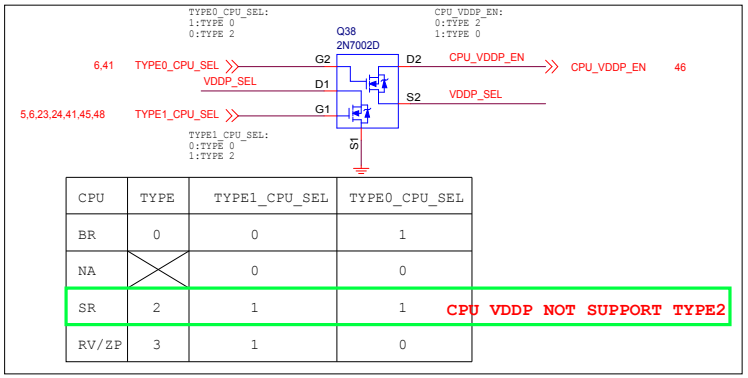
CPU_VDDP_S0

1.05V/0.9
S0:8.5A

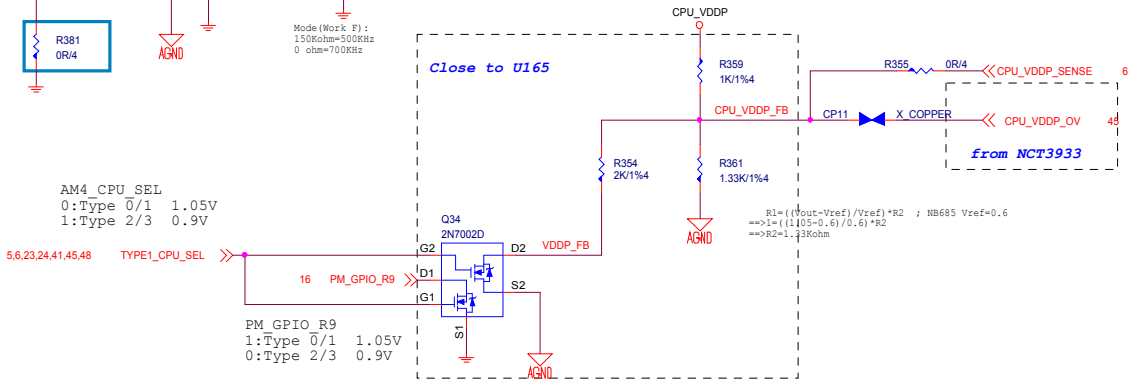
OCP=15.45A





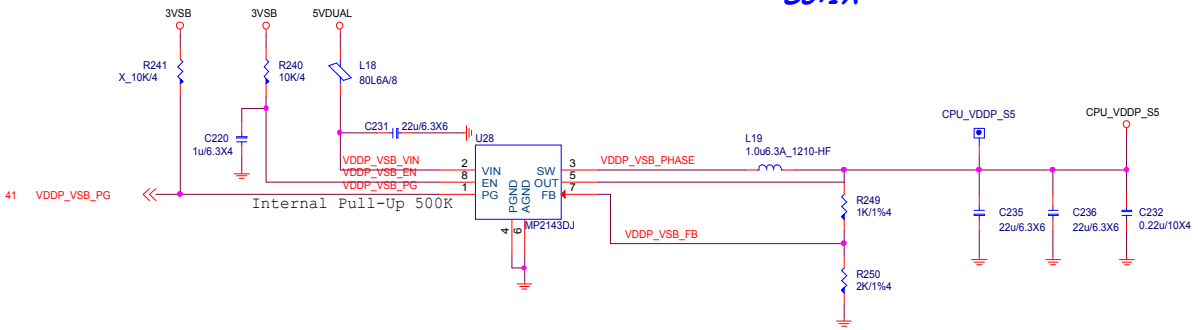
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

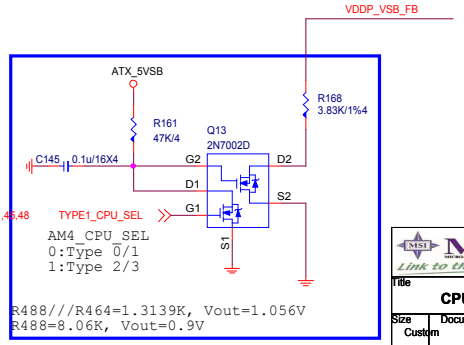
CPU VDDP NOT SUPPORT TYPE2



CPU_VDDP_S5

VDDP_S5
1.05V/0.9
S5:1A





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Title	CPU Power VDDP-RT8125E	
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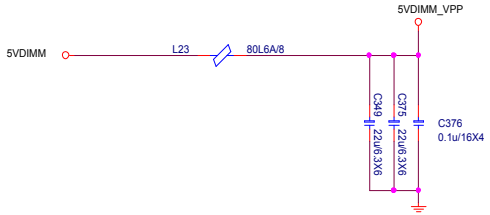
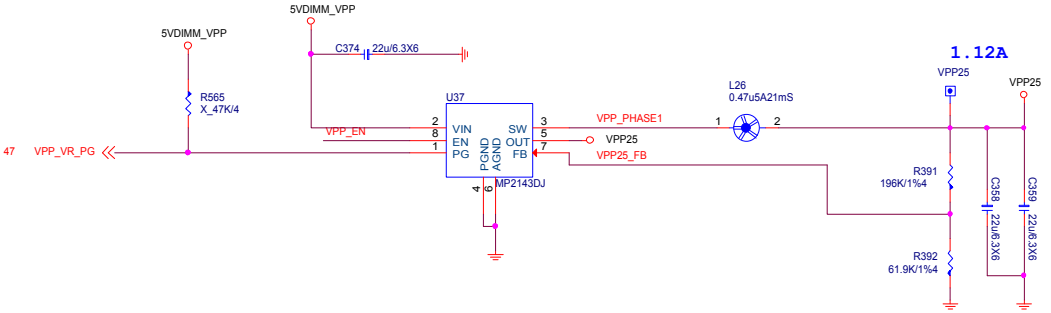
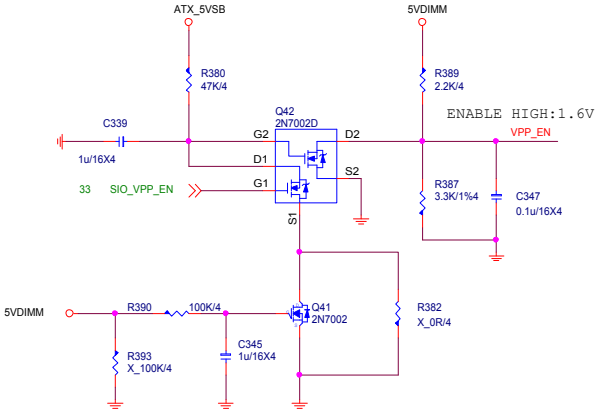
2DIMM :1.12A FOR DDR VPP2.5V







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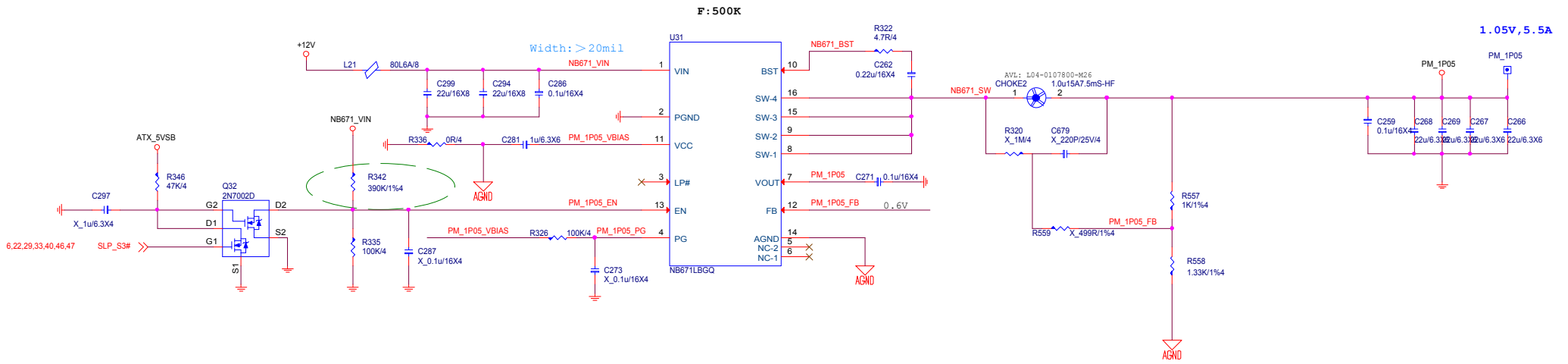
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

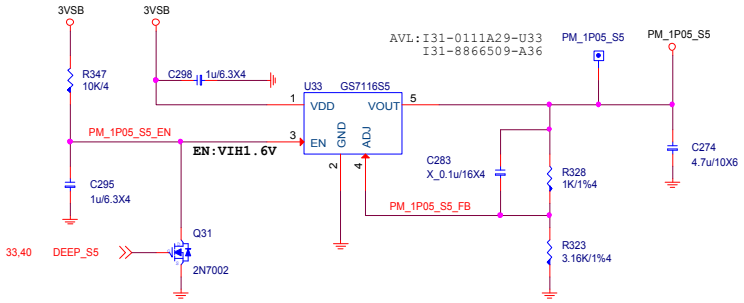
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH



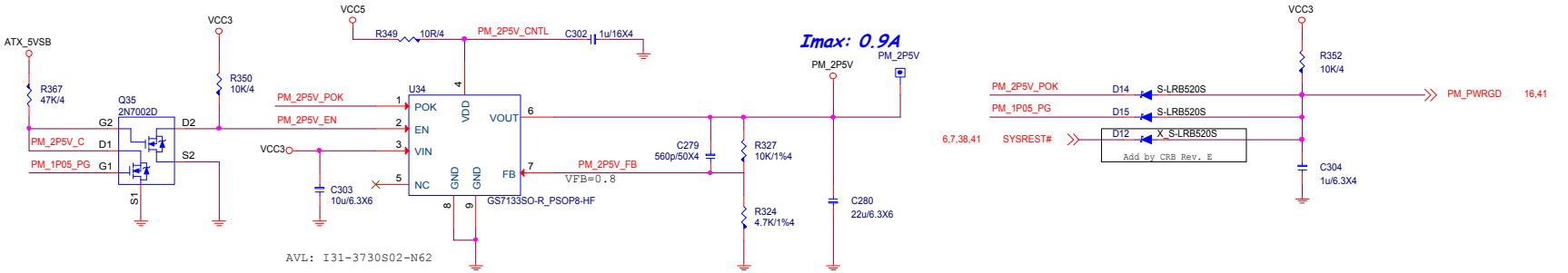
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

2.5V; 900mA



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HEAT SINK

PM_HS1
MEC2
MEC1
OE3-7A40001-K08

MOS HS(VCORE)

HS_MOS1
MEC2
MEC1
OE3-7A40002-K08

CPU Socket

CPU2
E95-0000021-C22

RETENTION MODULE

Simulation

X_JS1
SIM1
X_PIN1*2

X_JS2
SIM2
X_PIN1*2

MANUAL PART

UEFI1
G51-MTSPXXA-A09

HDMI_LA1
Label
HDMI
HDMI LABEL

BAT1_X1
BAT-BCR2032P-RH

MKT1
Label
MKT_B350I_PRO
B350I_PRO

FCH2
Label
FCH_A320.
X_A320

MKT2
Label
MKT_B350I_S01
X_B350I_S01

MKT3
Label
MKT_A320_PRO
X_A320I_PRO

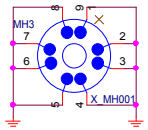
PCB1

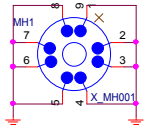
7A40-10
PK0-07A4010-G37,精成-深圳,1,台北微星廠(MSI)
PK0-07A4010-E48,毅華,1,台北微星廠(MSI)

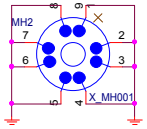
MOS HS(NB)

HS_MOS2
MEC2
MEC1
X_HS-0504250-HF

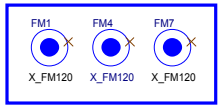
Optics Orientation Holes



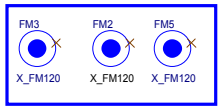




5010



5020



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