MS-7A40 Ver:20

CPU:
AMD AM4

System Chipset:
Promontory B450
(Value DIY or System Builder)

Main Memory:
DDR IV * 2   MAX:64 GB

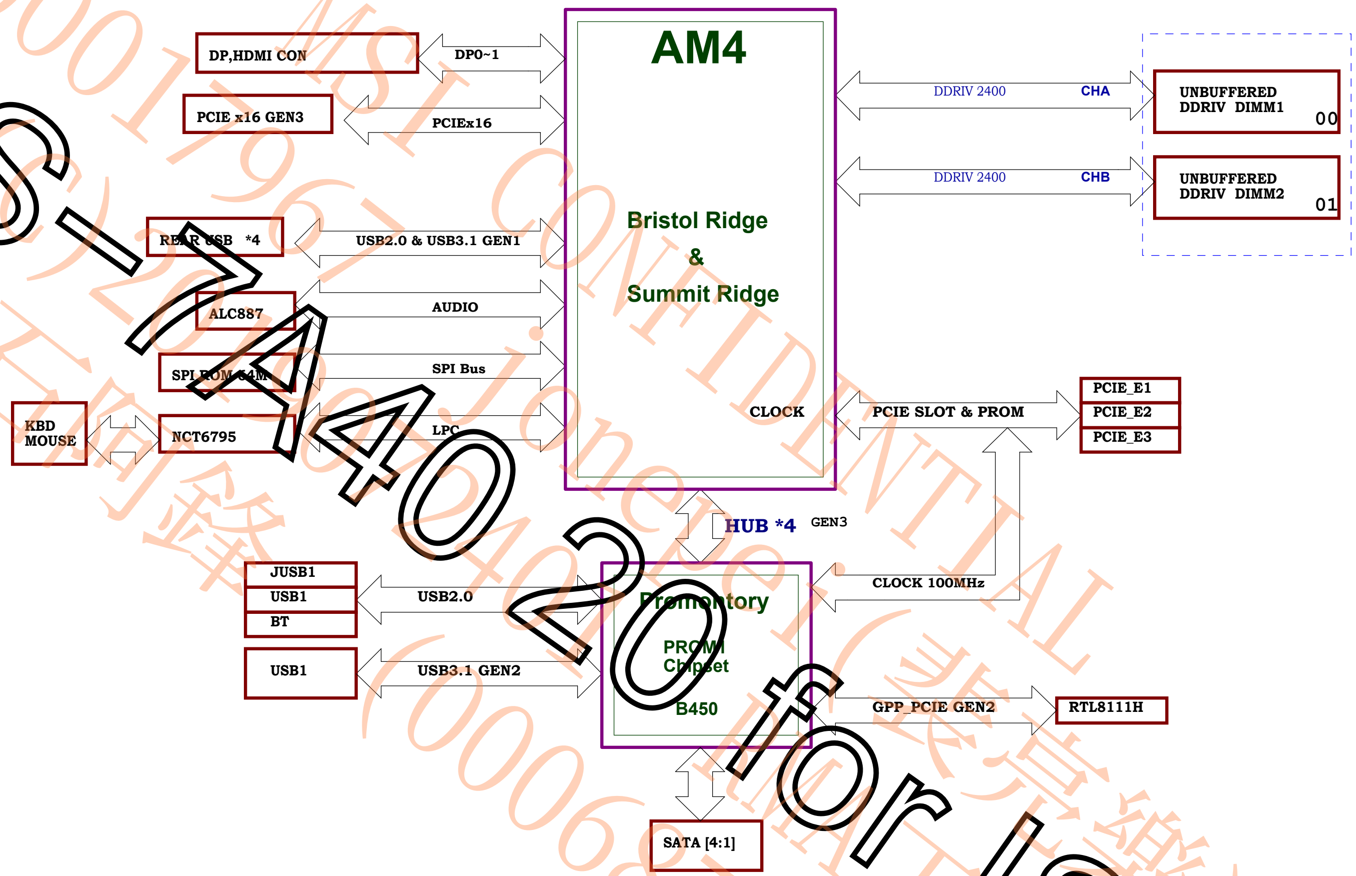
VRM
IR35201 6+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1

OCP IC:
RT9553

FUSION BLOCK DIAGRAM



MSI MICRO-START INT'L CO.,LTD.

Title	Block Diagram	
Size: Custom	Document Number: MS-7A40	Rev: 20
Date: Thursday, May 17, 2018	Sheet 1 of 55	

AMD
AM4

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Link to the Future

Title	COVER SHEET	
Size: Custom	Document Number: MS-7A40	Rev: 20
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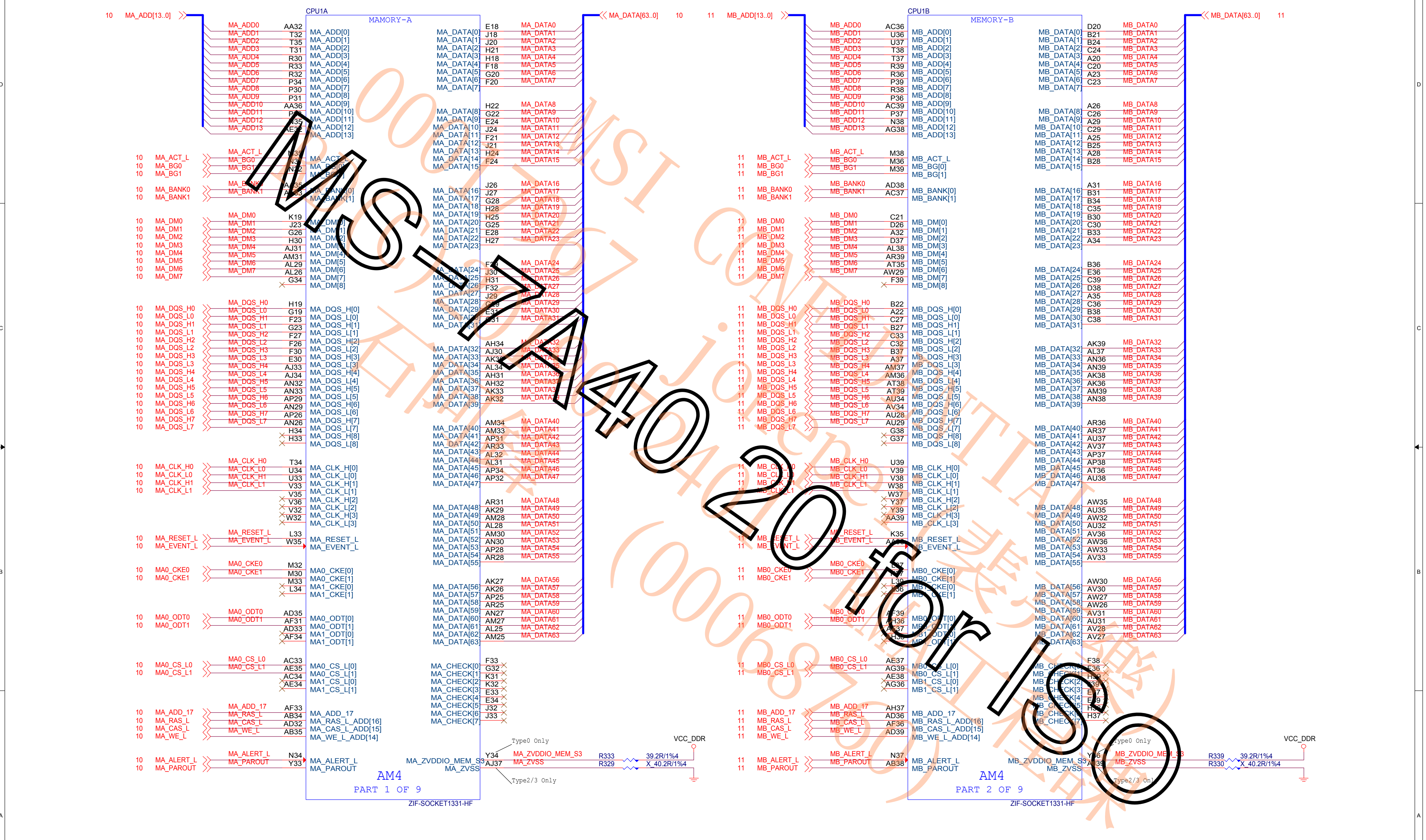
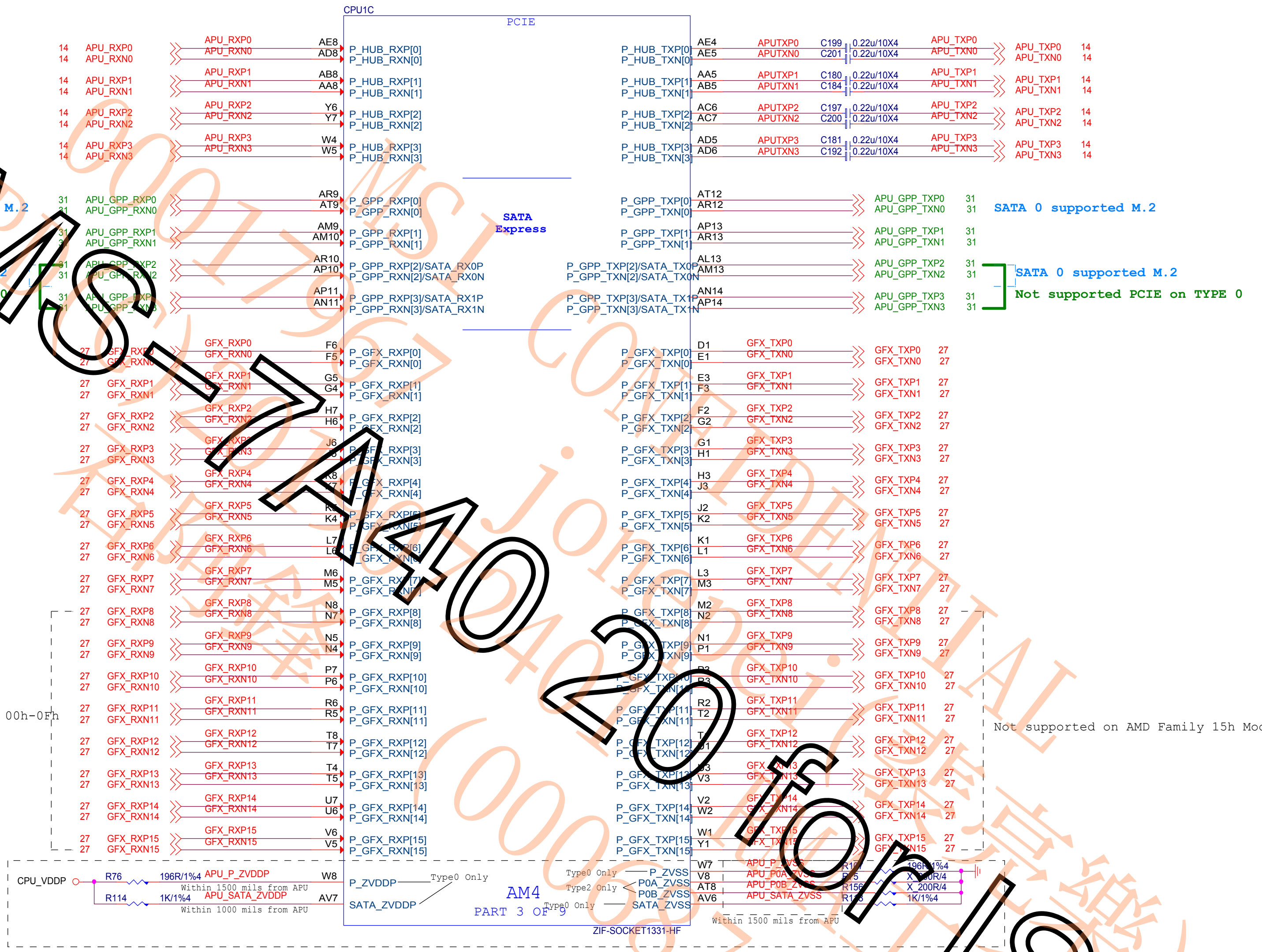


MSI MICRO-START INT'L CO.,LTD.

Title: AM4 DDR4 I/F

Size	Document Number	Rev
Custom	MS-7A40	20

Date: Thursday, May 17, 2018 Sheet 3 of 55



	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

Only supported on AMD Family 17h/Models 00h-0Fh

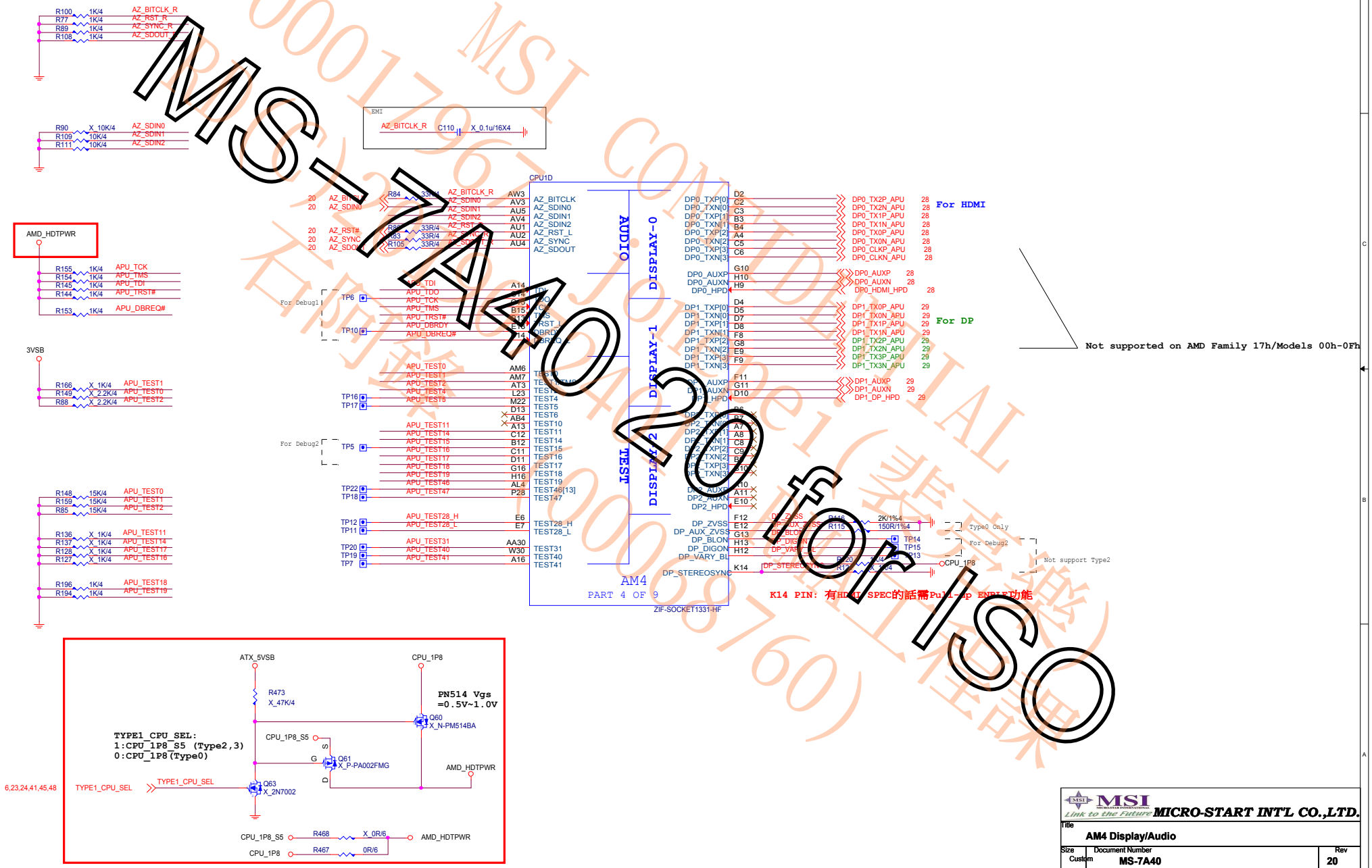
Not supported on AMD Family 15h Models 60h-6Fh

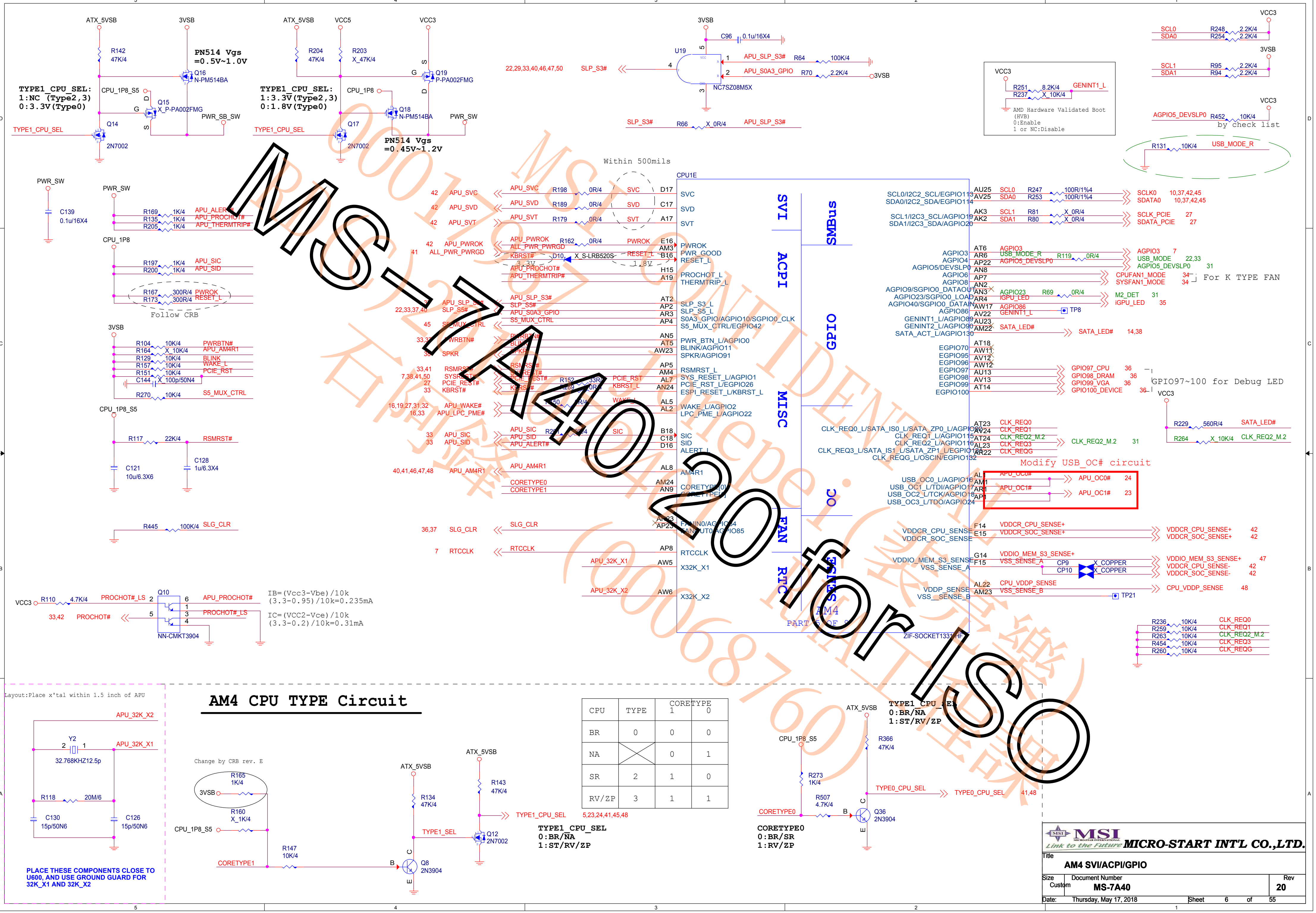
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: AM4 PCIE/SATAE

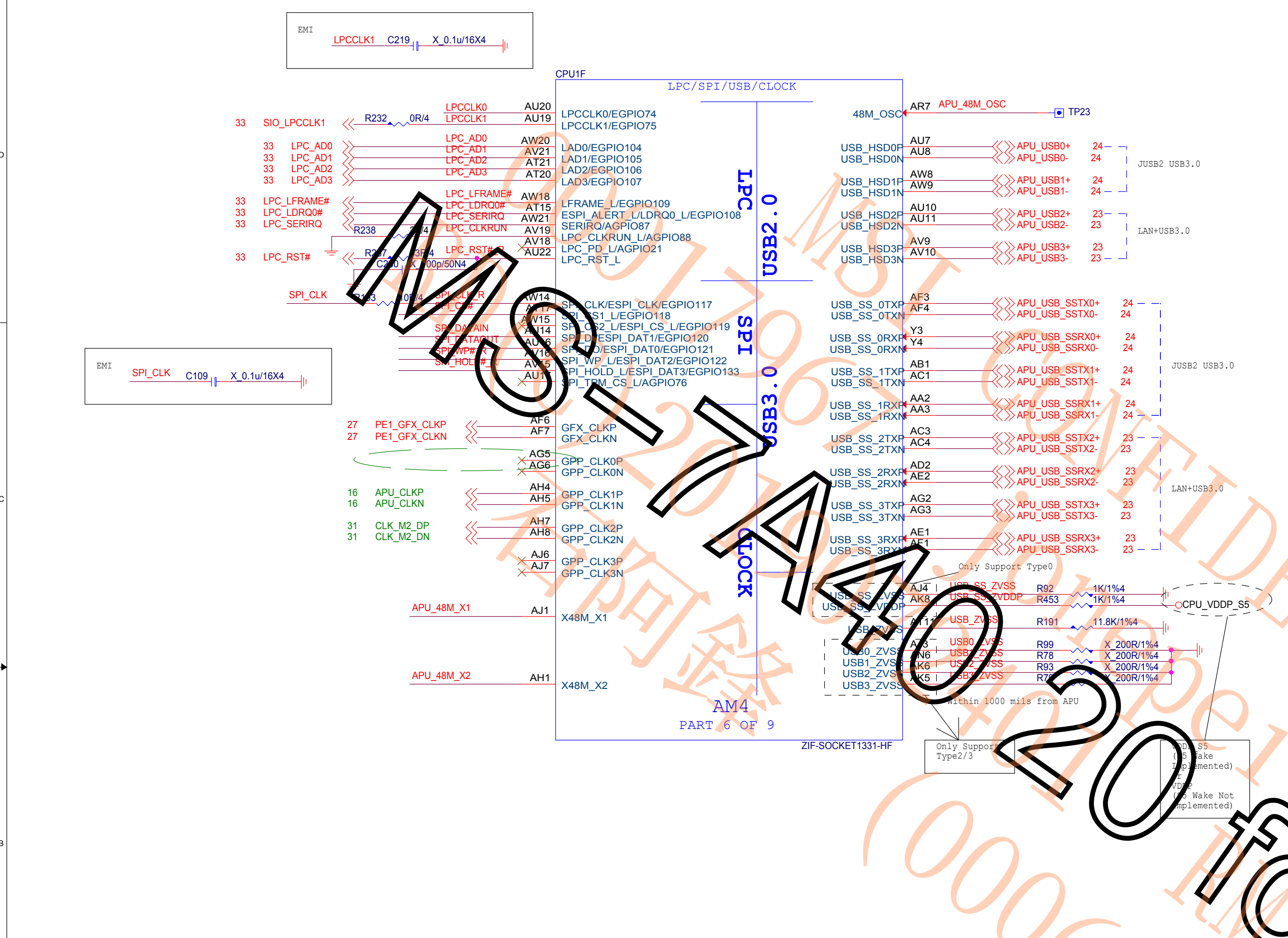
Size: Custom | Document Number: MS-7A40 | Rev: 20

Date: Thursday, May 17, 2018 | Sheet 4 of 55

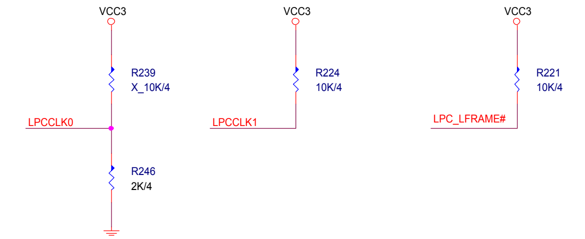

MS-7A40 20 for ISO
AMD_HDTPWR
3VSB
EMI
AZ_BITCLK_R
C110
X_0.1u/16X4
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
AM4
PART 4 OF 9
ZIF-SOCKET1331-HF
For HDMI
For DP
Not supported on AMD Family 17h/Models 00h-0Fh
K14 PIN: 有HDMI SPEC的話需Pull-up ENABLE功能
TYPE1_CPU_SEL:
1:CPU_1P8_S5 (Type2,3)
0:CPU_1P8(Type0)
PN514 Vgs
=0.5V~1.0V
ATX_5VSB
CPU_1P8
CPU_1P8_S5
AMD_HDTPWR
TYPE1_CPU_SEL
MICRO-START INT'L CO.,LTD.
Link to the Future
AM4 Display/Audio
MS-7A40
20
Thursday, May 17, 2018
Sheet 5 of 55



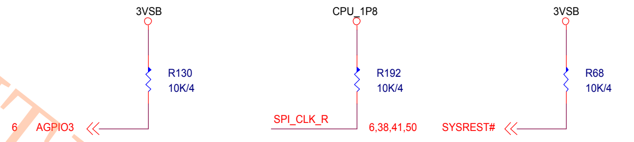
CPU	TYPE	CORETYPE 1	0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1



Strapping Options

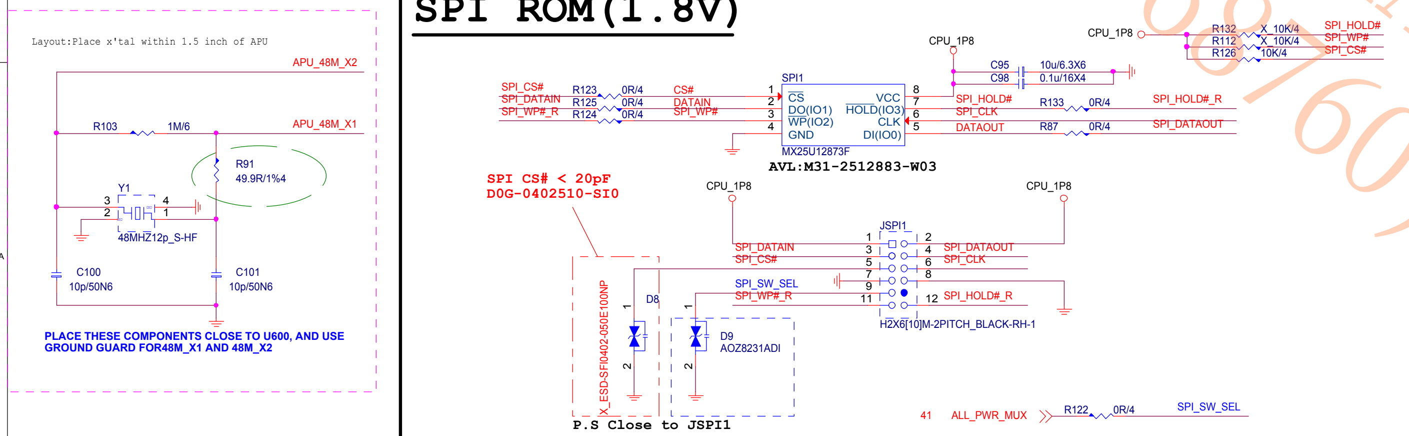


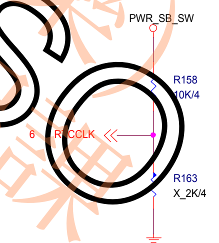
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ?????	LPC ROM



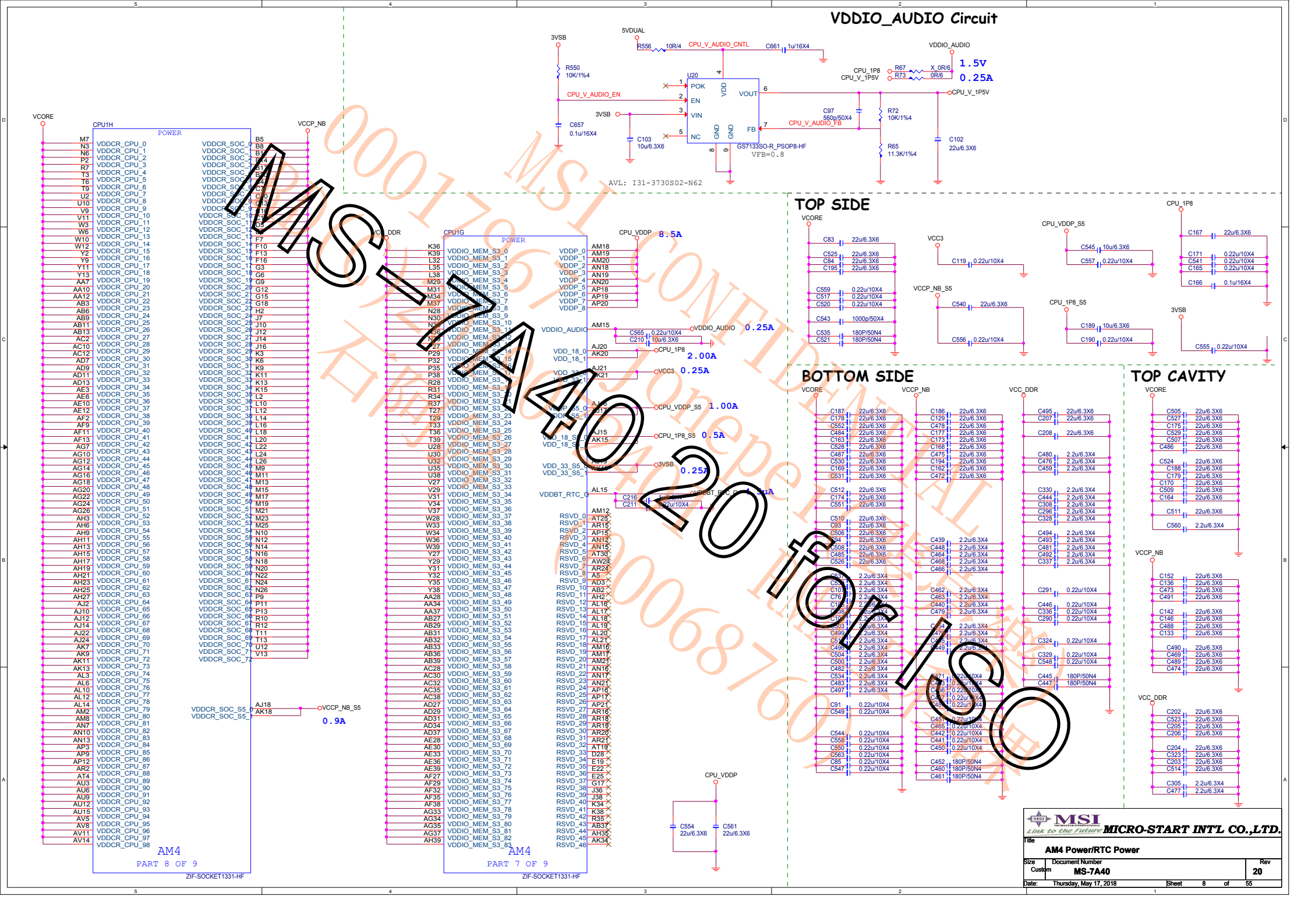
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

SPI ROM(1.8V)





	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board


VDDIO_AUDIO Circuit
5VDUAL
3VSB
R556 10R/4
CPU_V_AUDIO_CNTL
C661 1u/16X4
VDDIO_AUDIO
1.5V
0.25A
R550 10K/1%4
U20
POK
EN
VIN
NC
VOUT
FB
VDD
GND
CPU_V_AUDIO_EN
CPU_V_AUDIO_FB
C657 0.1u/16X4
C103 10u/6.3X6
C97 560p/50X4
R72 10K/1%4
R65 11.3K/1%4
C102 22u/6.3X6
CPU_1P8
CPU_V_1P5V
R67 X_0R/6
R73 0R/6
GS7133SO-R_PSOP8-HF
VFB=0.8
AVL: I31-3730S02-N62
TOP SIDE
BOTTOM SIDE
TOP CAVITY
VCORE
VCCP_NB
VCC_DDR
VCC3
VCCP_NB_S5
CPU_VDDP_S5
CPU_1P8_S5
CPU_VDDP
8.5A
2.00A
0.25A
1.00A
0.5A
0.9A
CPU1H
CPU1G
POWER
AM4
PART 8 OF 9
PART 7 OF 9
ZIF-SOCKET1331-HF
MSI-MS-7A40-20-ISO
MSI CONFIDENTIAL
MICRO-START INT'L CO.,LTD.
Title
AM4 Power/RTC Power
Size
Custom
Document Number
MS-7A40
Rev
20
Date:
Thursday, May 17, 2018
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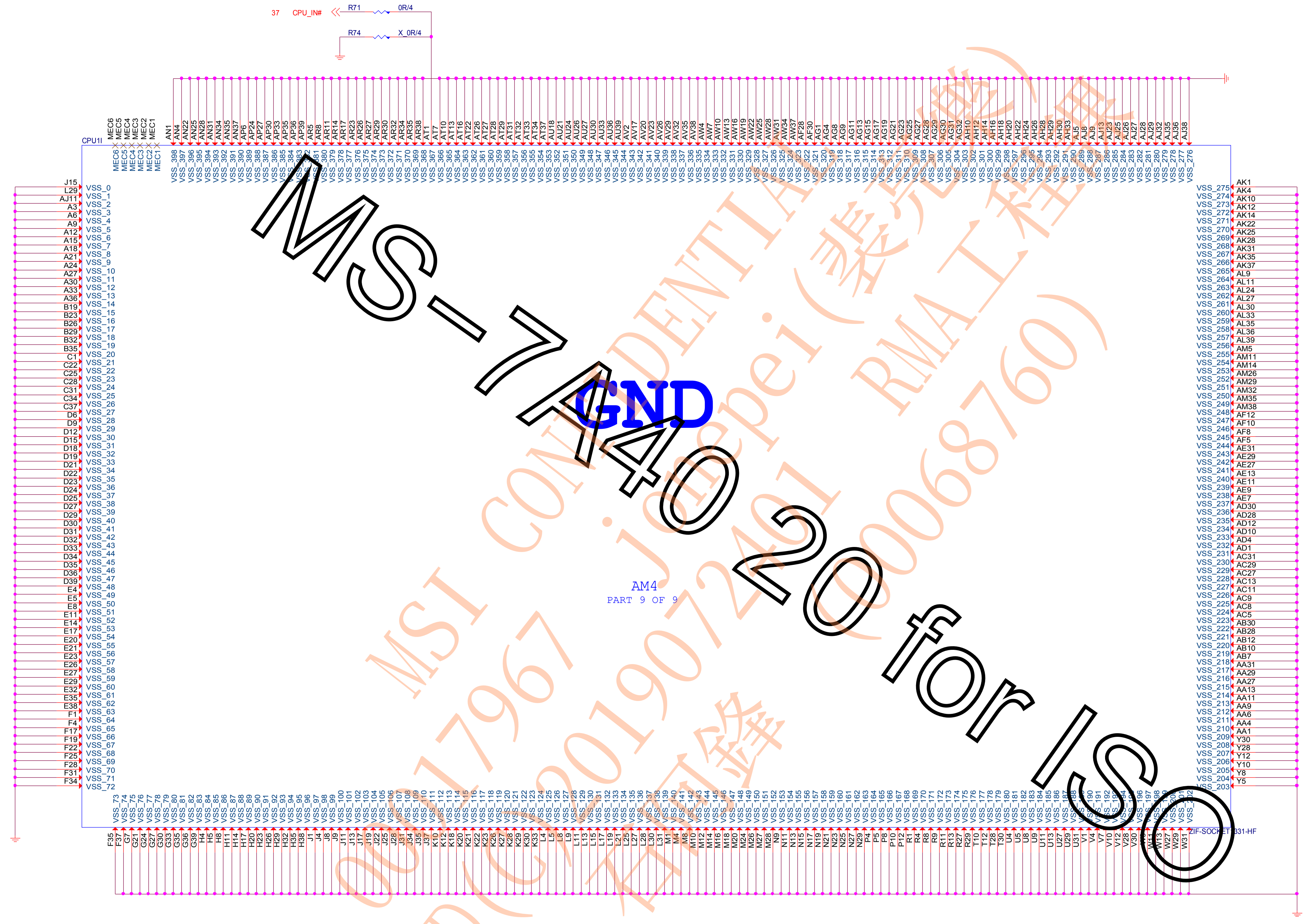
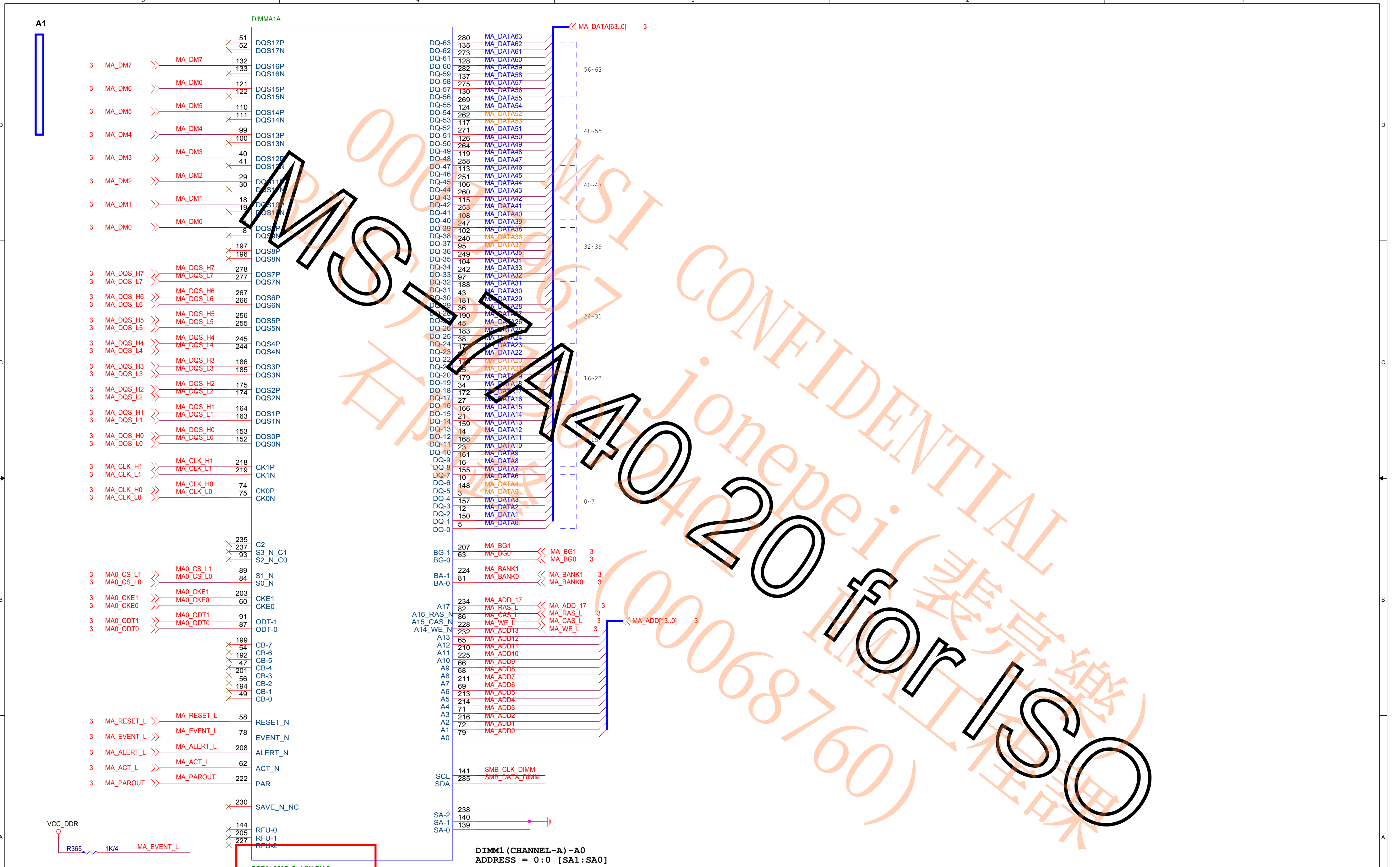
8
of
55



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	AM4 GND		
Size: Custom	Document Number: MS-7A40		Rev: 20
Date: Thursday, May 17, 2018	Sheet 9 of 55		

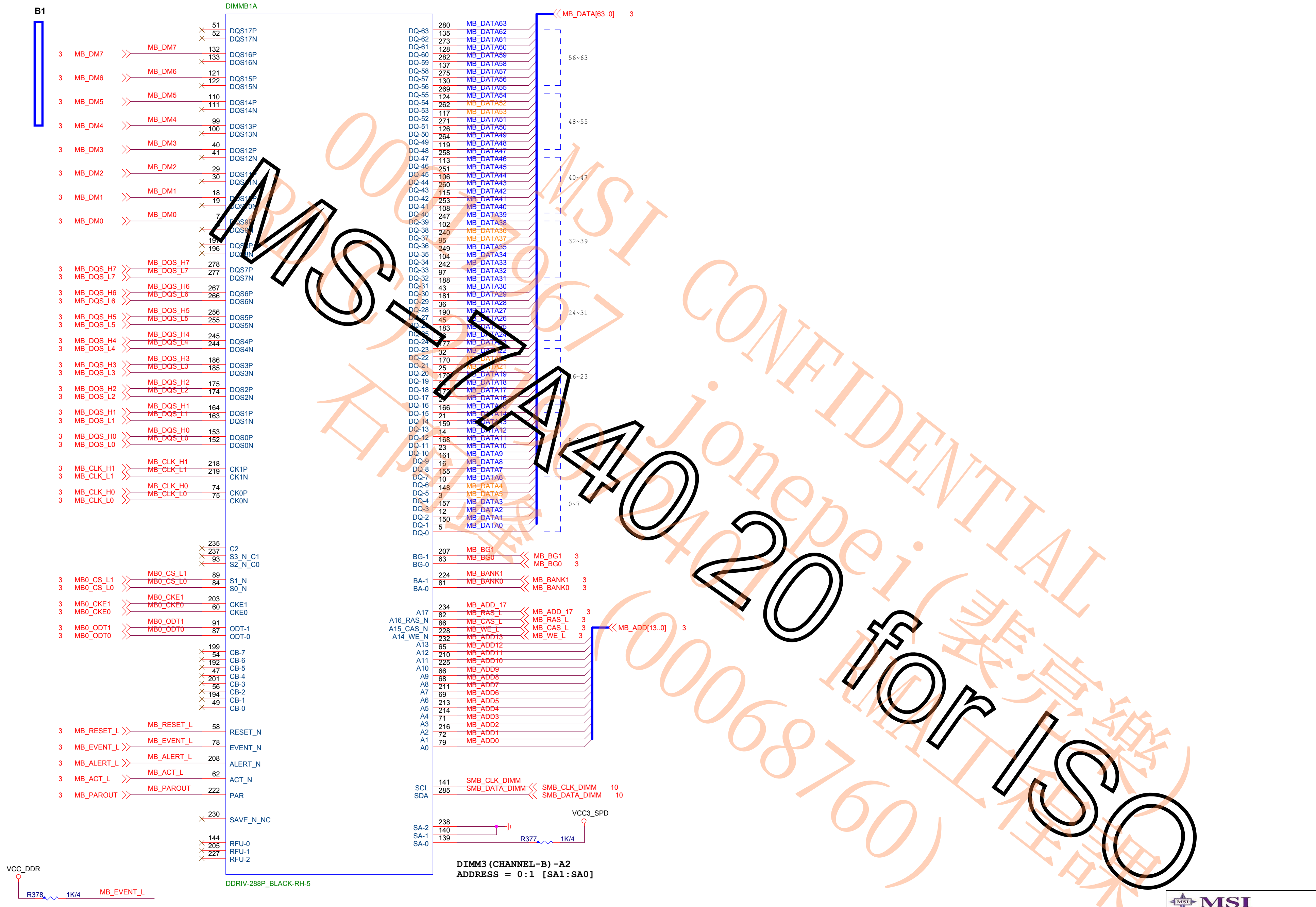


MICRO-START INT'L CO.,LTD.

Title: DDR4-DIMM CH-A

Size: Custom | Document Number: MS-7A40 | Rev: 20

Date: Thursday, May 17, 2018 | Sheet 10 of 55

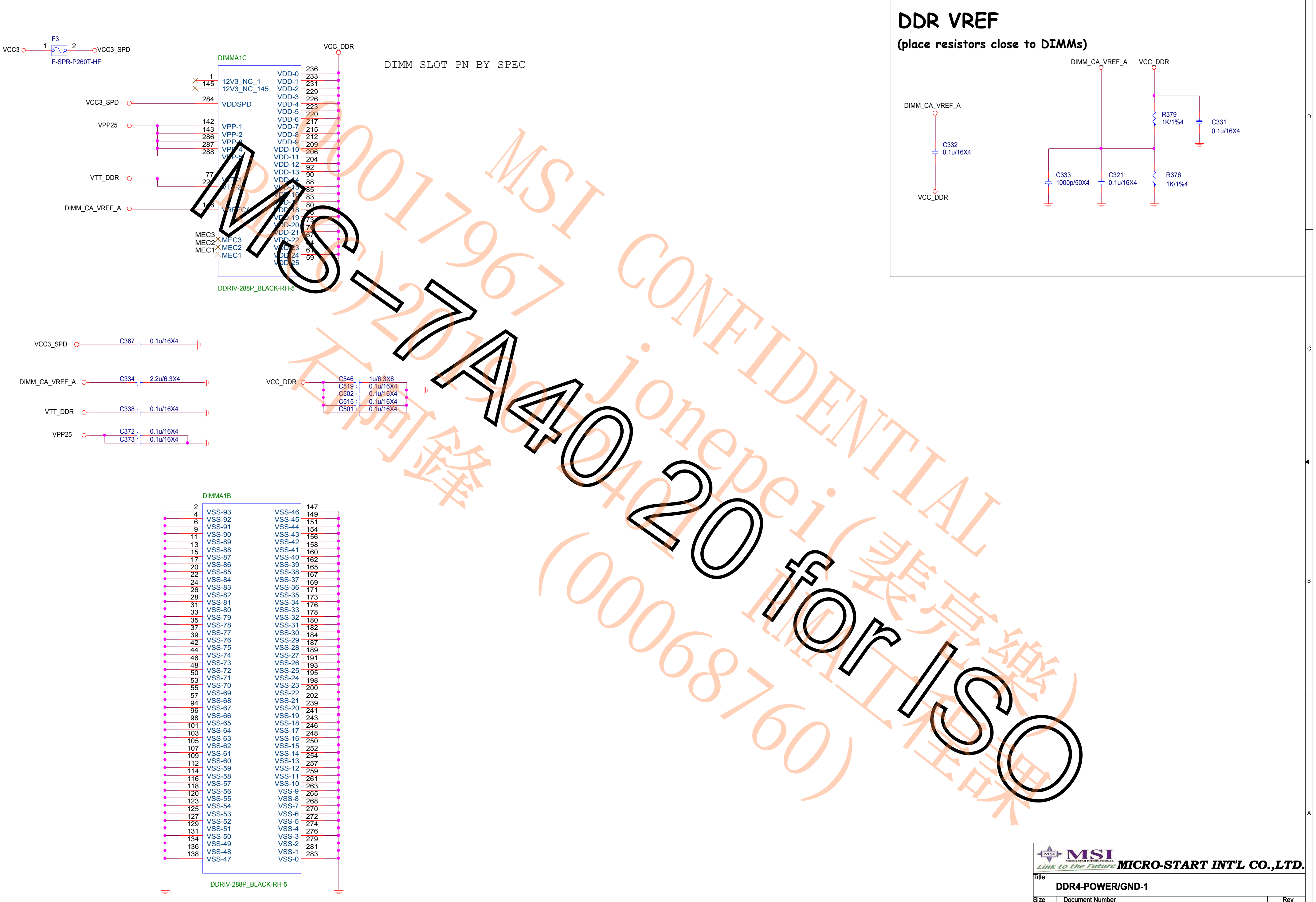


MICRO-START INT'L CO.,LTD.

Title: DDR4-DIMM CH-B

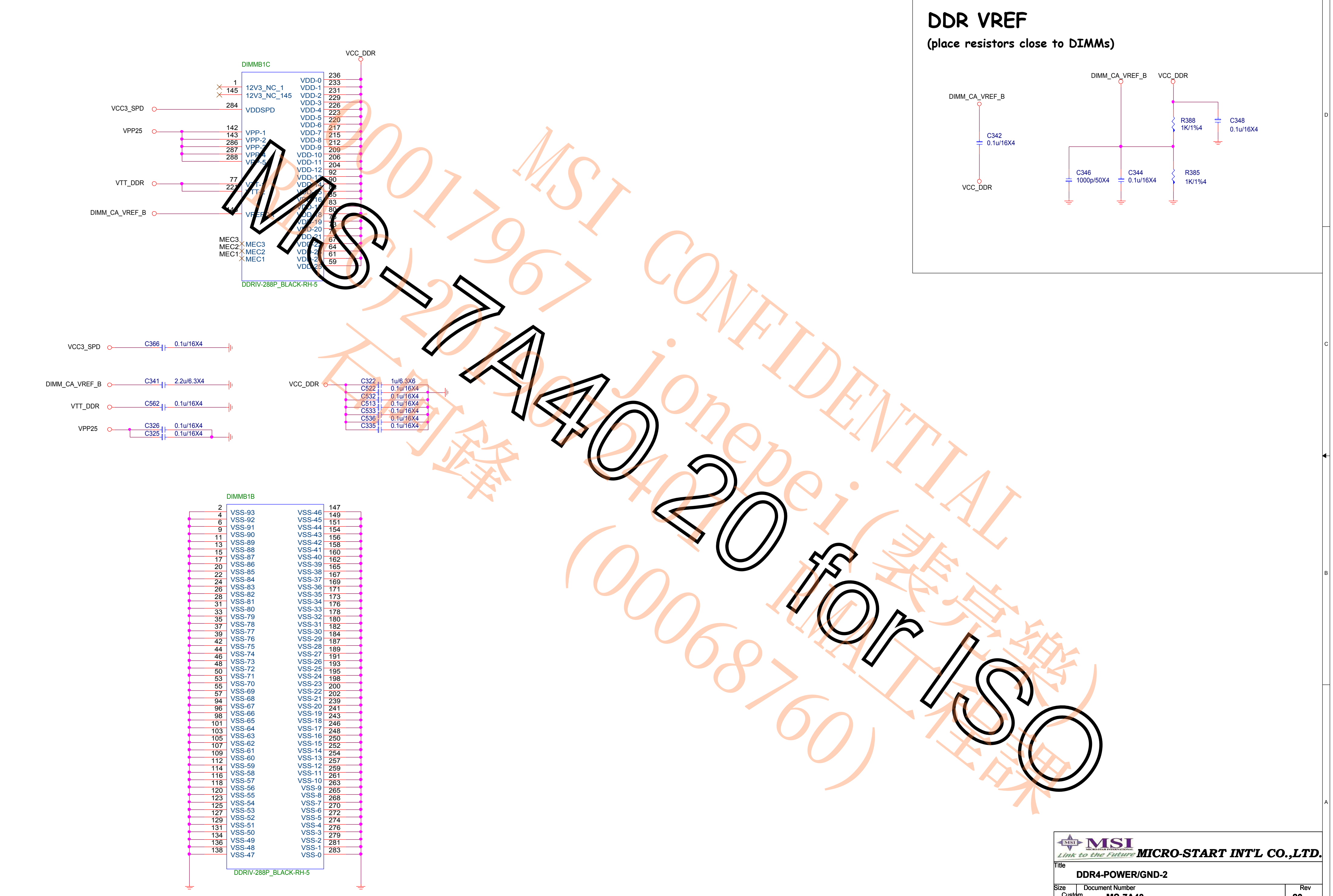
Size	Document Number	Rev
Custom	MS-7A40	20

Date: Thursday, May 17, 2018 — Sheet 11 of 55



MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title	DDR4-POWER/GND-1	
Size: Custom	Document Number: MS-7A40	Rev: 20
Date: Thursday, May 17, 2018	Sheet 12 of 55	

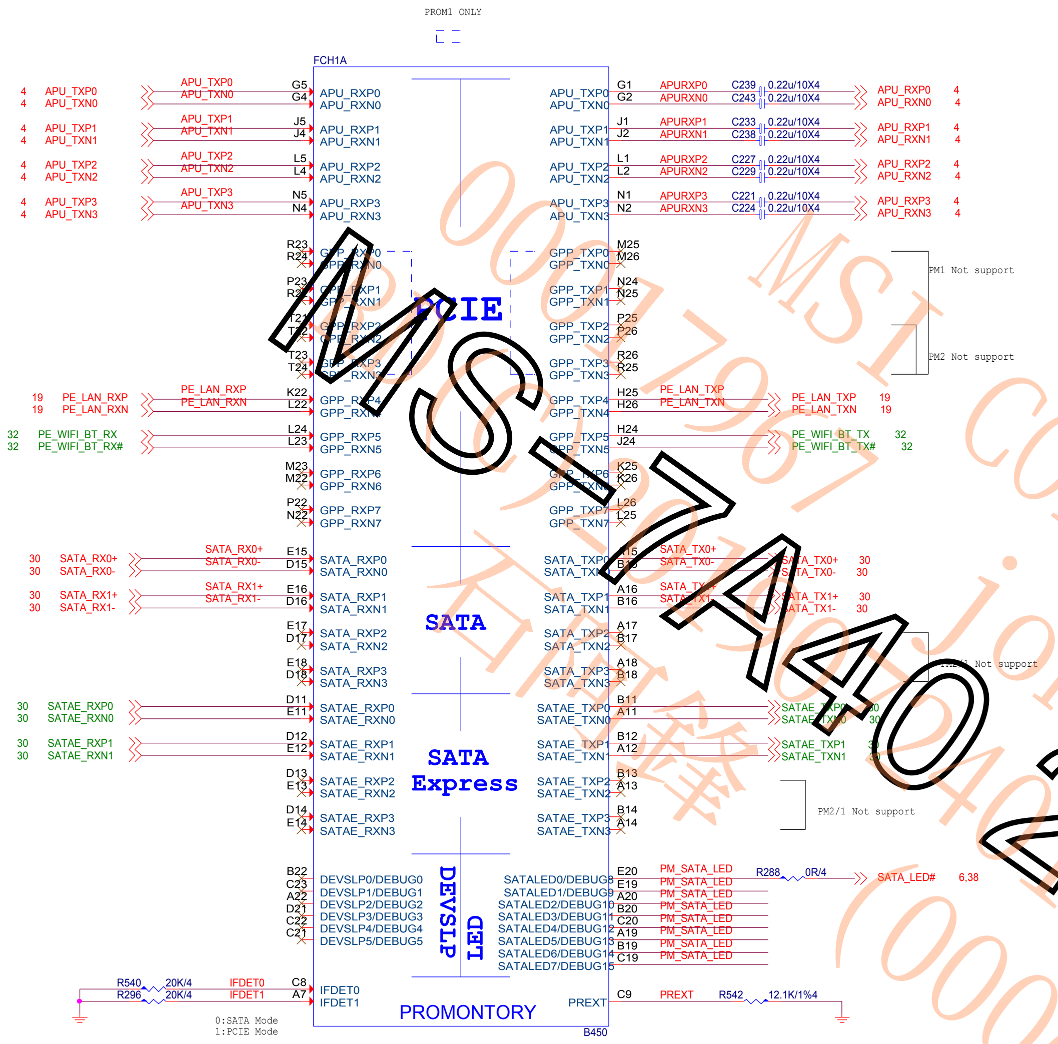


MSI MICRO-START INT'L CO.,LTD.

Title: DDR4-POWER/GND-2

Size	Document Number	Rev
Custom	MS-7A40	20

Date: Thursday, May 17, 2018 Sheet 13 of 55



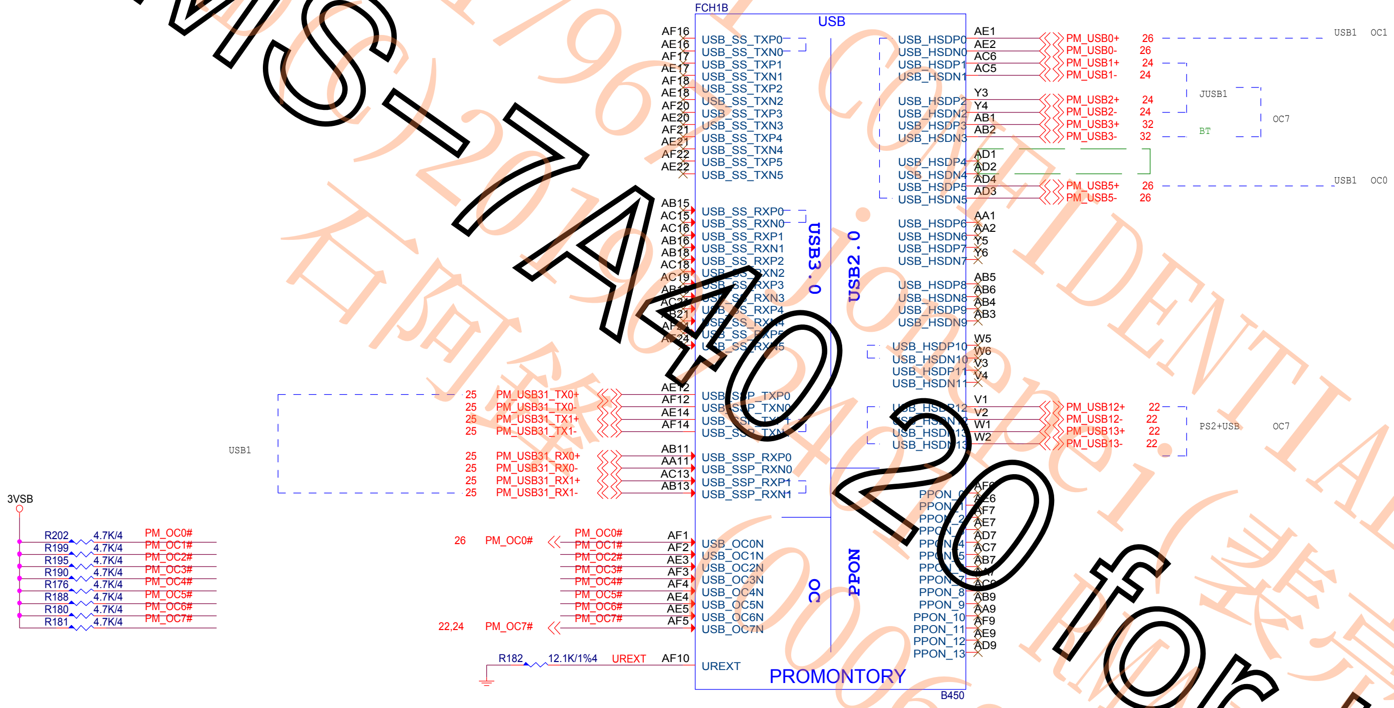
AMD *AMD Confidential—Advance Information*

AMD 300-Series Chipsets, "Promontory" Sub-Family Data Sheet 55553 Rev. 1.08 September 2016

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7



USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

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AMD 300-Series Chipsets, "Promontory" Sub-Family Data Sheet 55553 Rev. 1.08 September 2016

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~5	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Promontory-USB/OC

Size: Custom | Document Number: MS-7A40 | Rev: 20

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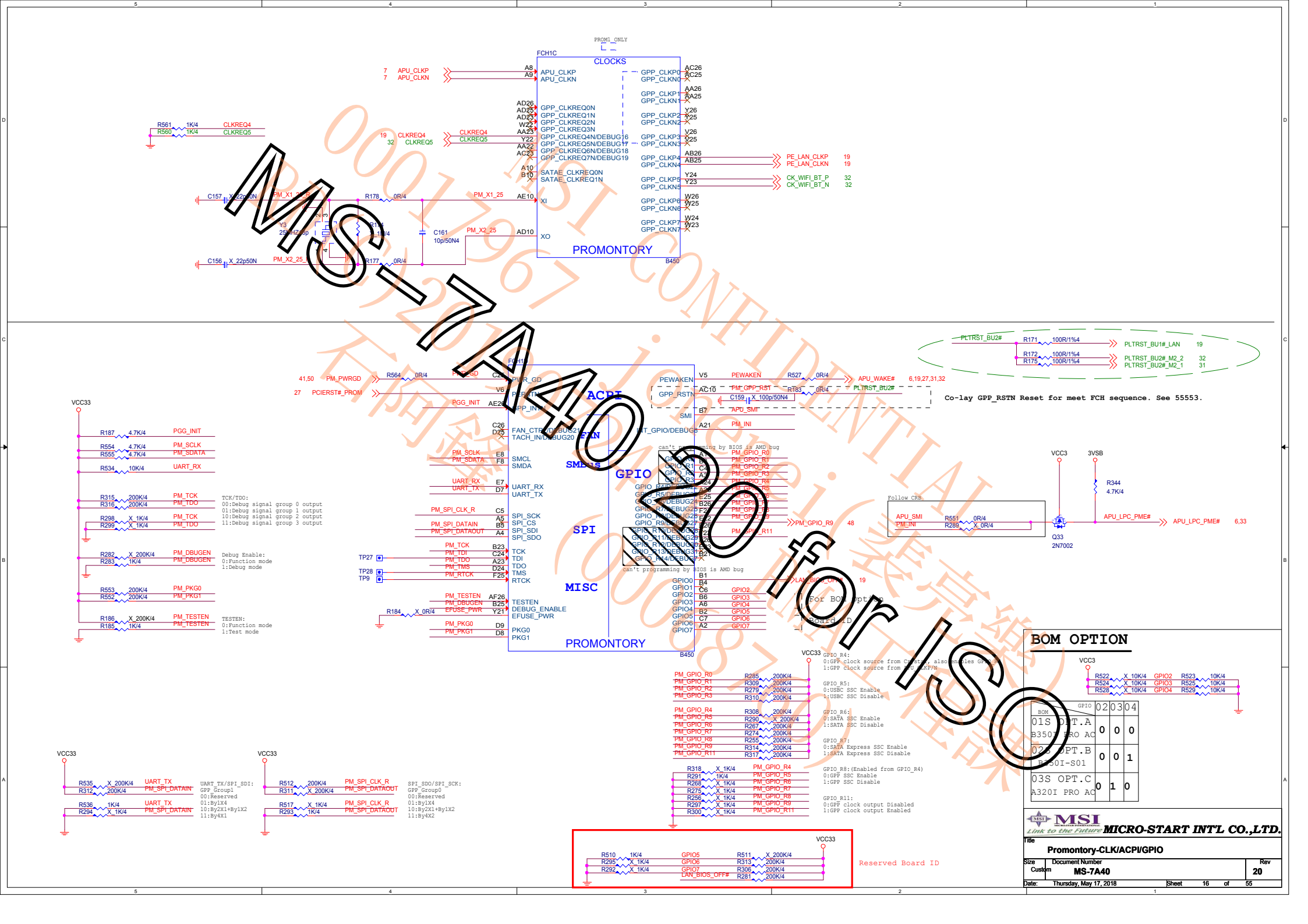
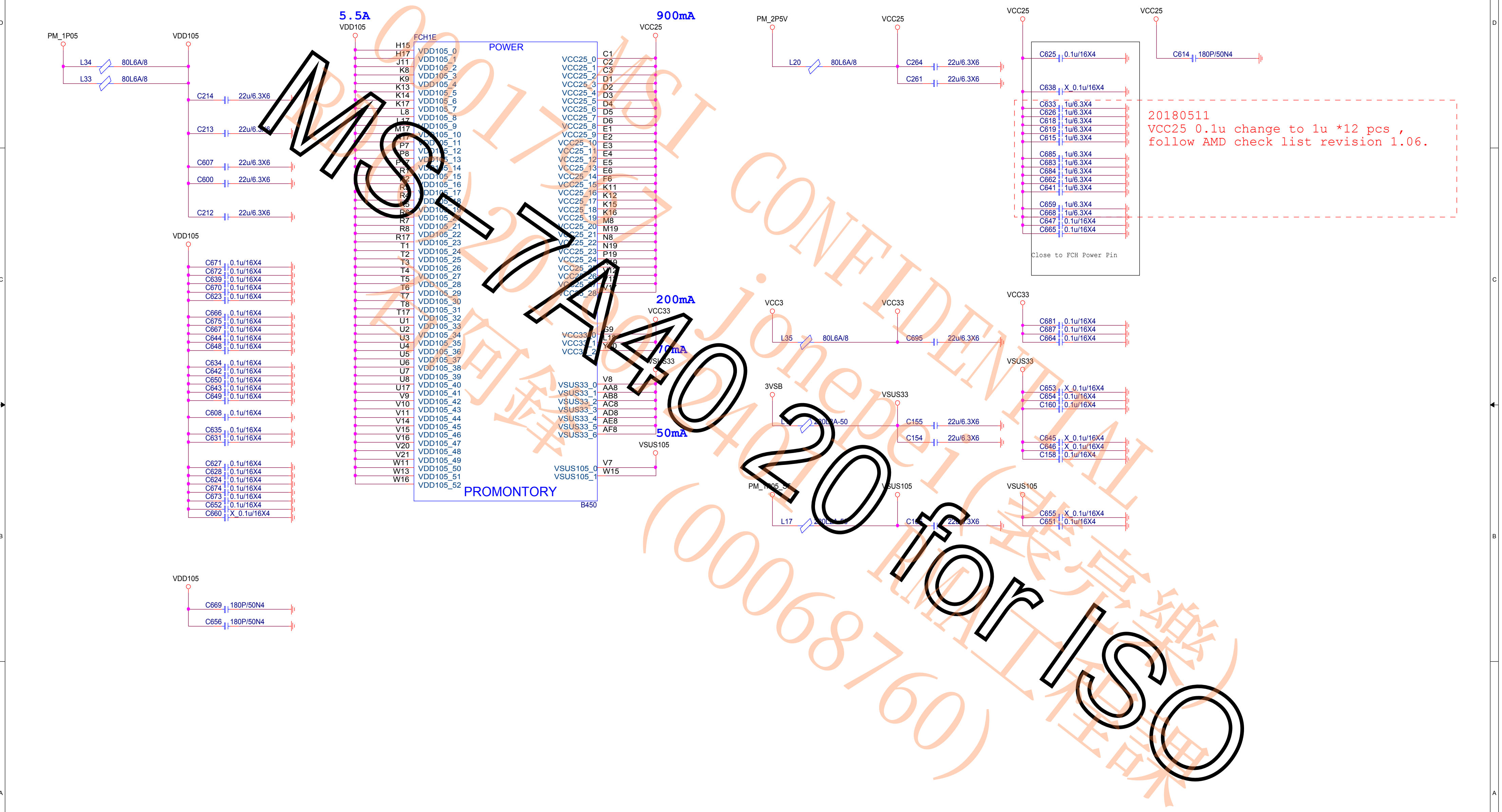
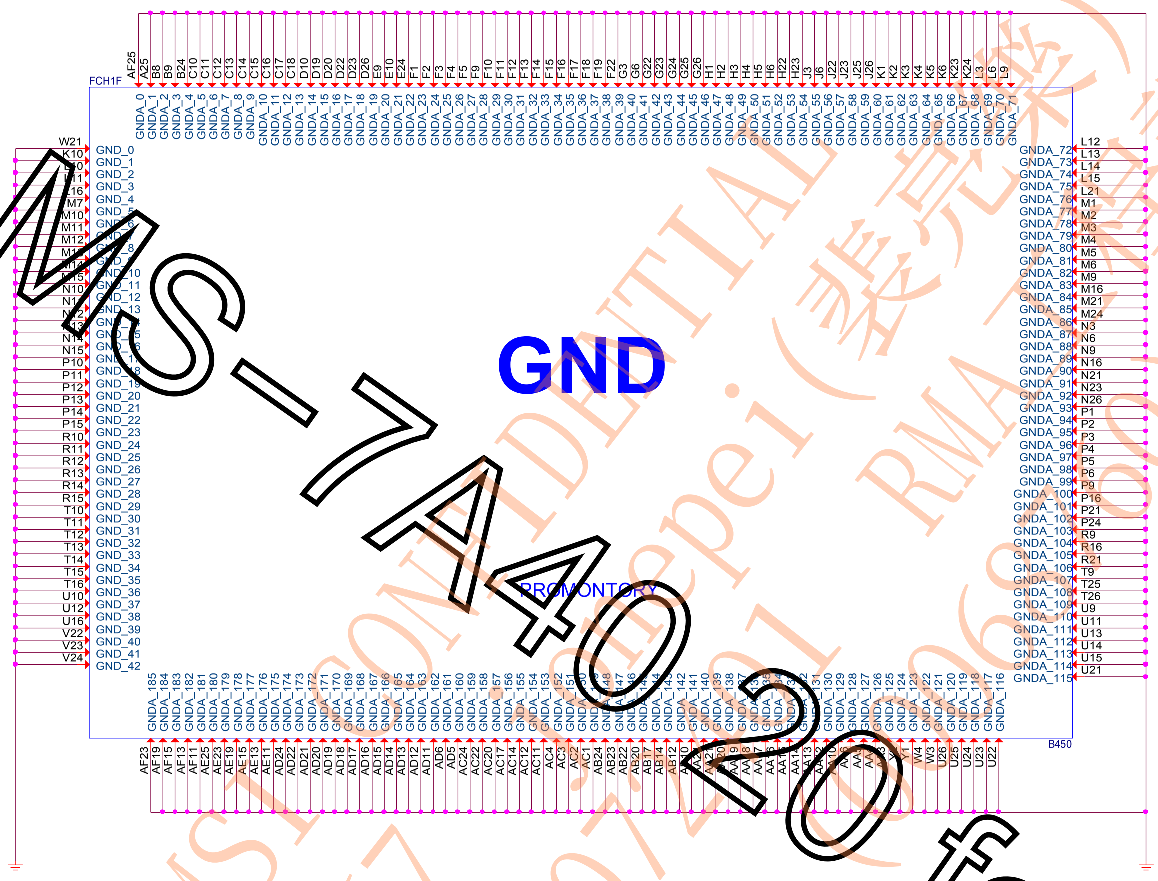

MS-7A40 for ISO
FCH1C
CLOCKS
PROMONTORY
B450
ACPI
FAN
SMBUS
GPIO
SPI
MISC
PROMONTORY
BOM OPTION
MICRO-START INT'L CO.,LTD.
Promontory-CLK/ACPI/GPIO
MS-7A40
Thursday, May 17, 2018



MICRO-START INT'L CO.,LTD.

Title	Promontory-Power	
Size: Custom	Document Number: MS-7A40	Rev: 20
Date: Thursday, May 17, 2018	Sheet 17 of 55	

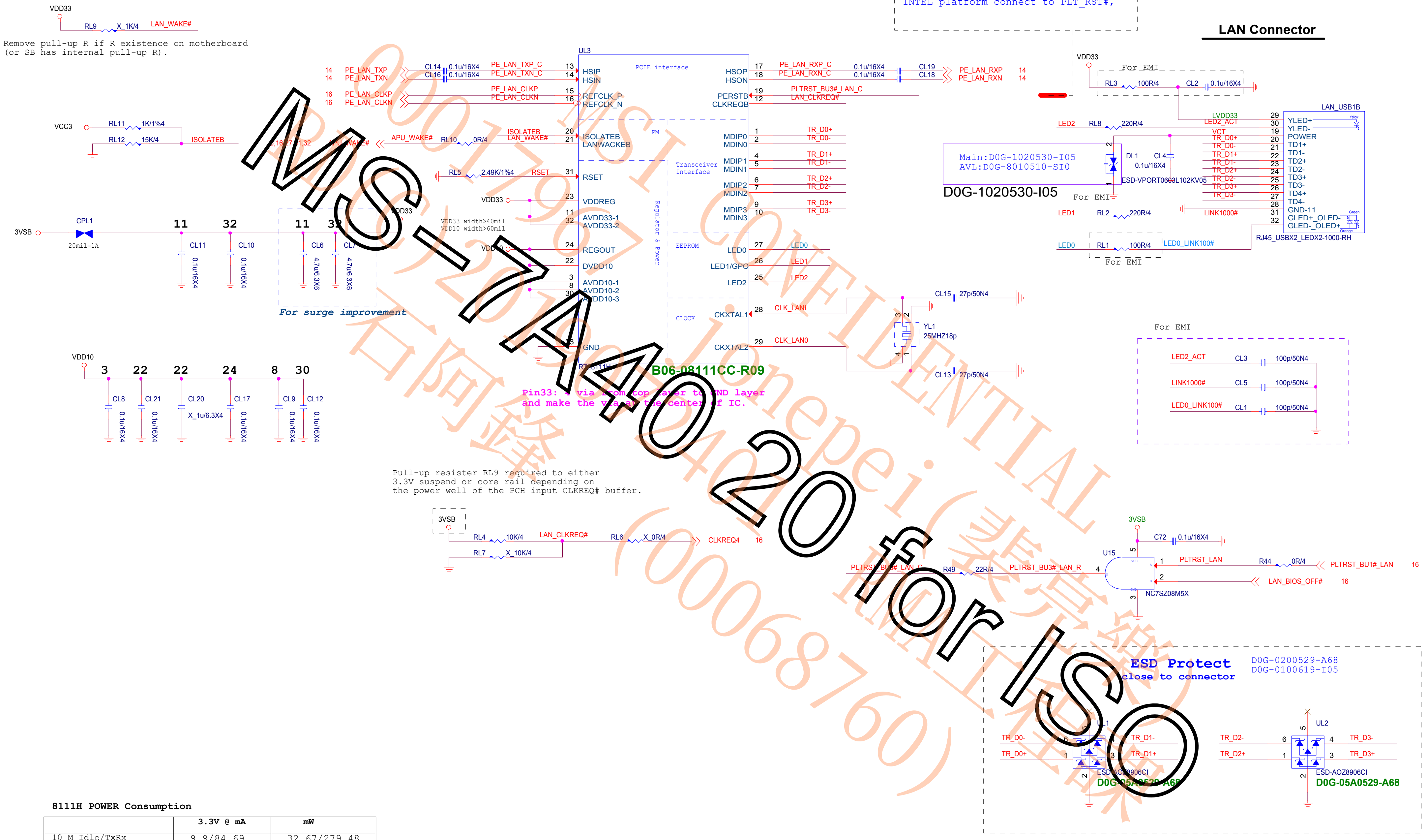


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	Promontory-GND		
Size: Custom	Document Number: MS-7A40		Rev: 20
Date: Thursday, May 17, 2018	Sheet 18 of 55		

RTL8111H Giga LAN

3.3V@177.57mA

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).



8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-START INT'L CO.,LTD.

Title: LAN-RLT 8111H

Size: Custom | Document Number: MS-7A40 | Rev: 20

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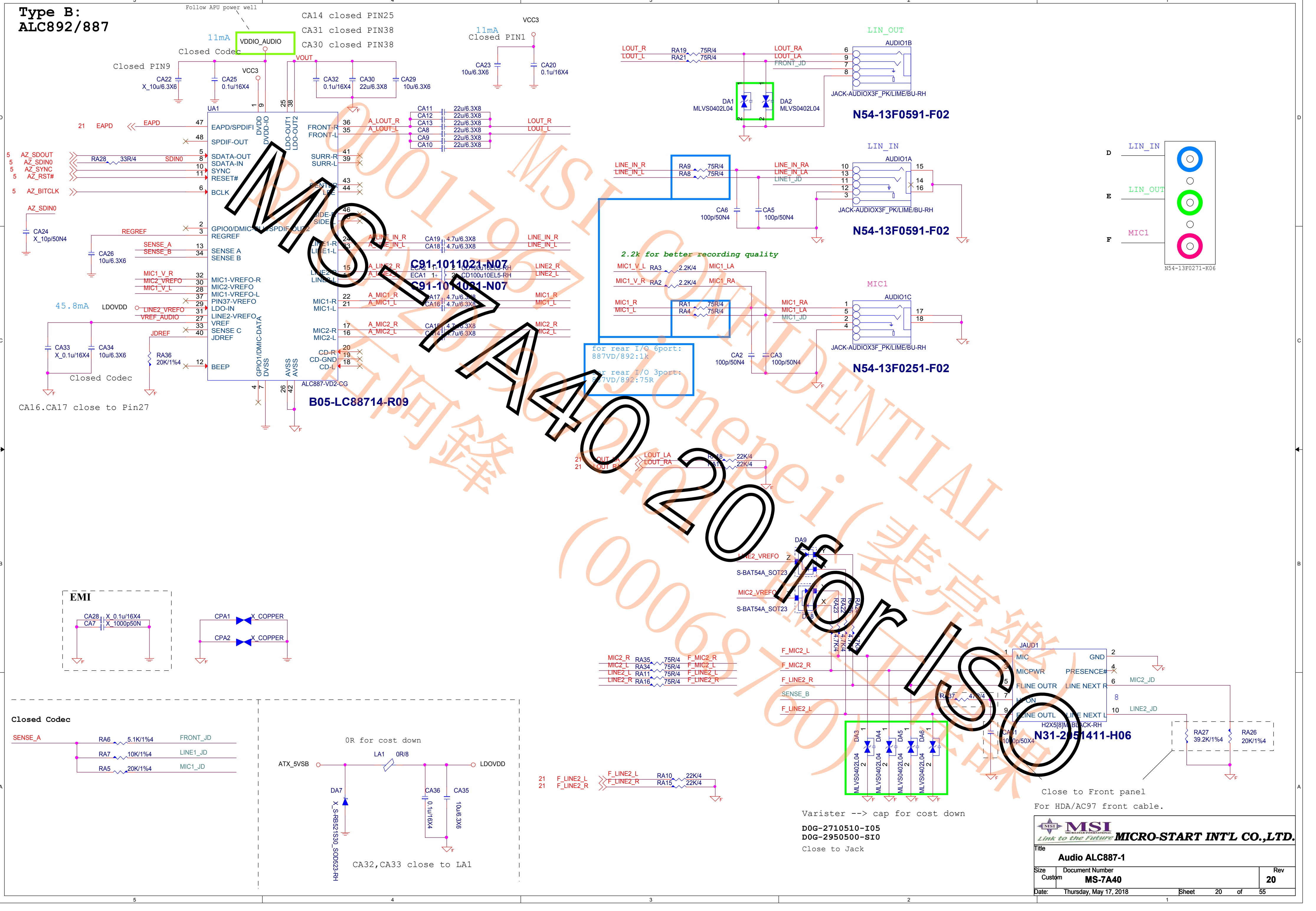
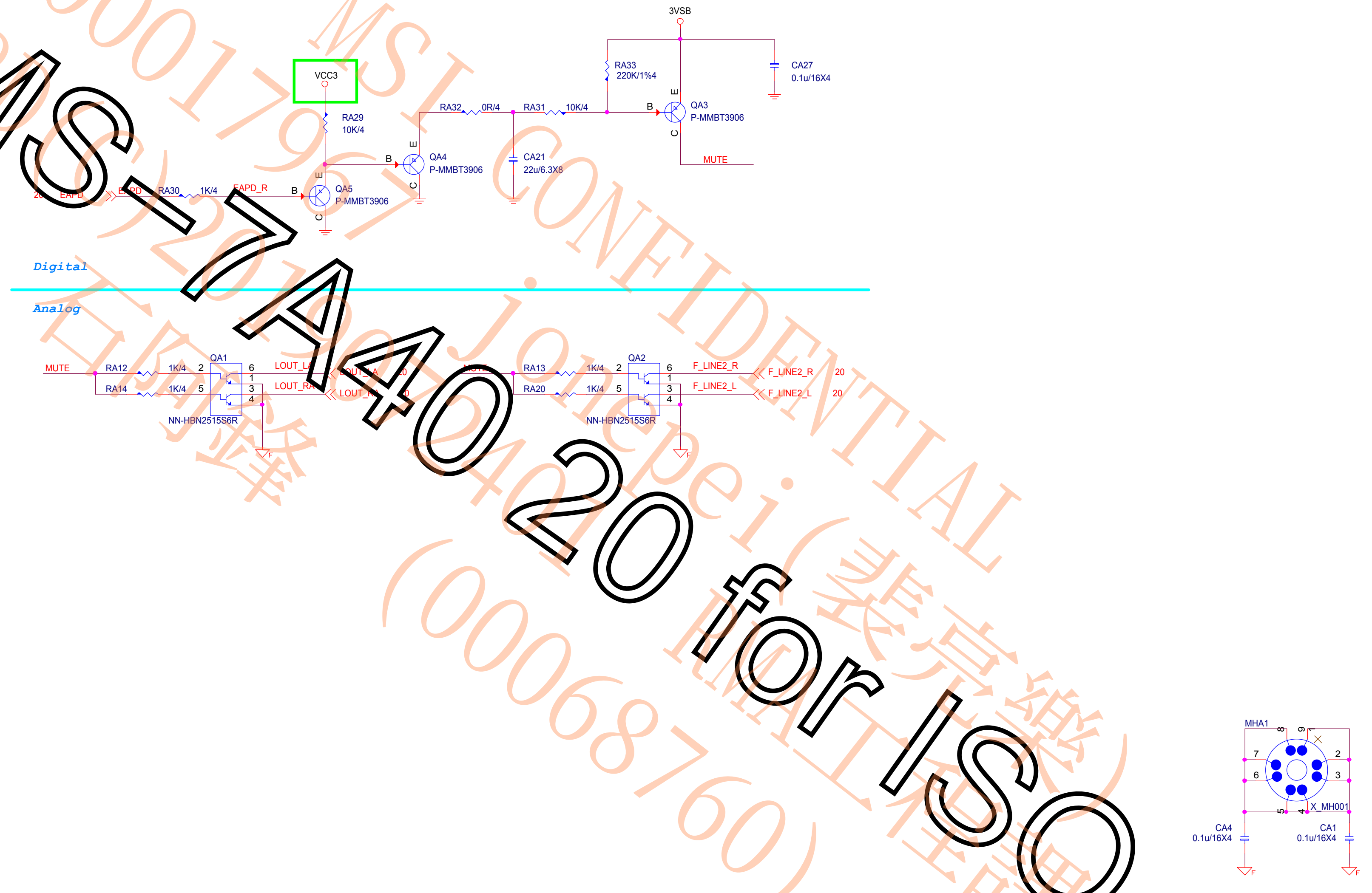


Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



MSI MICRO-START INT'L CO.,LTD.

Title	Audio ALC887-2	
Size: Custom	Document Number: MS-7A40	Rev: 20
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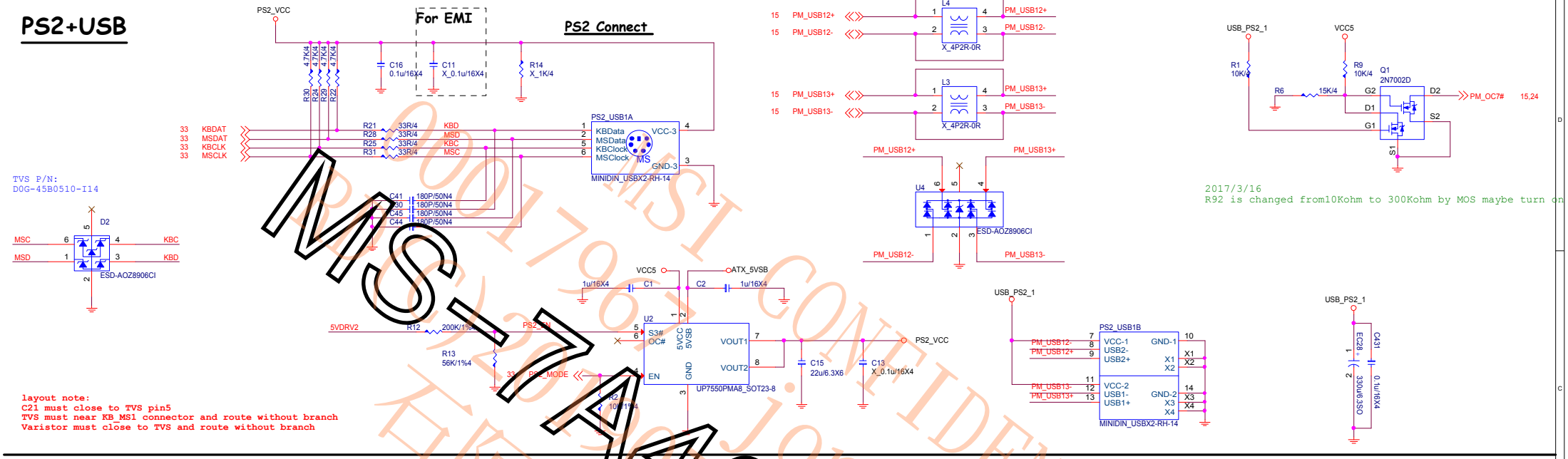
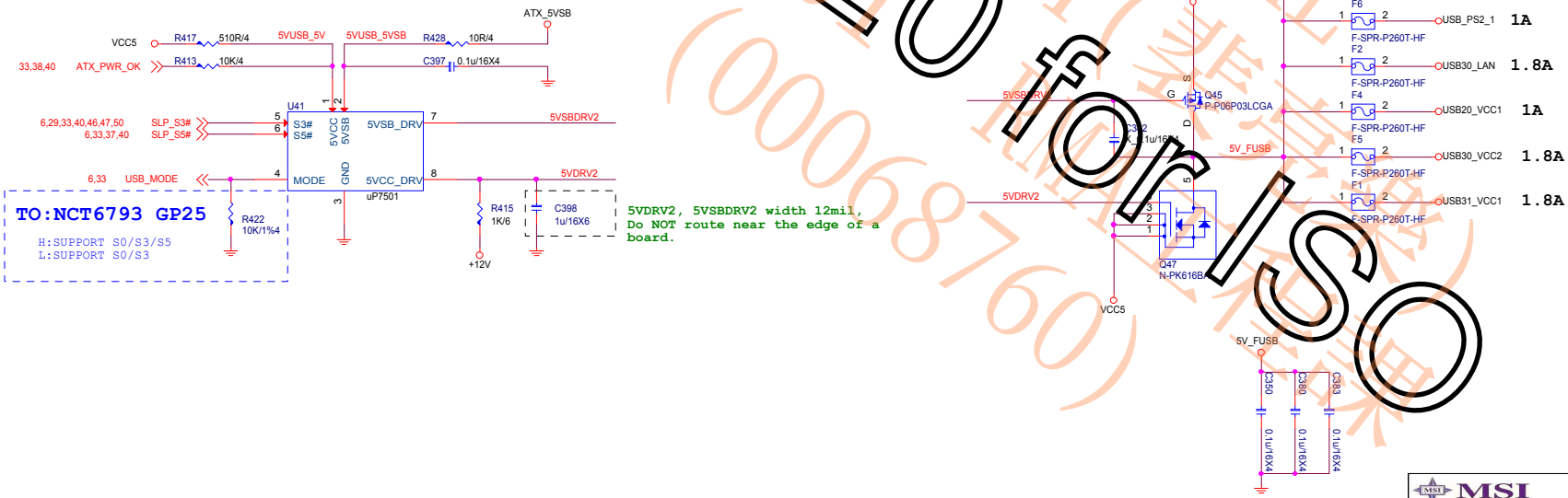
PS2+USB



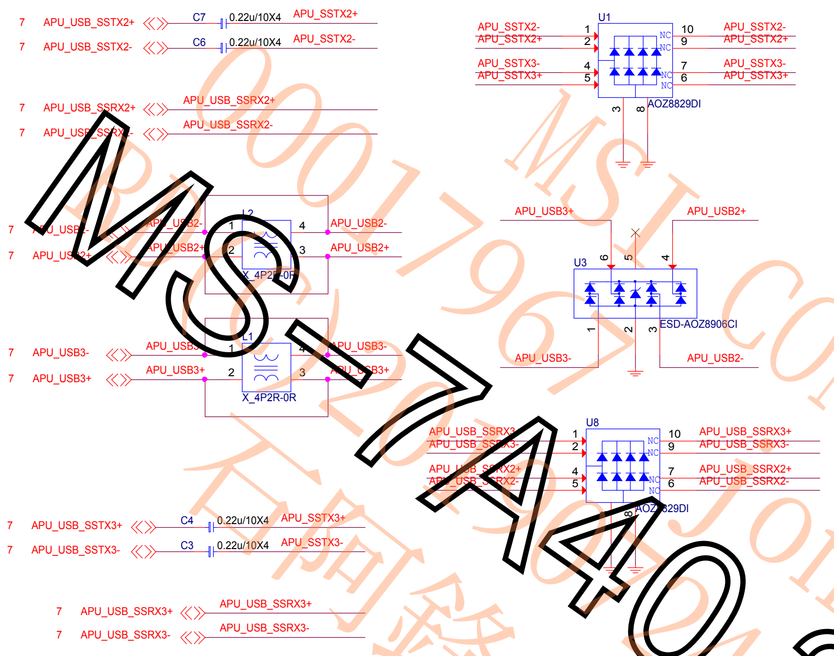
USB Power



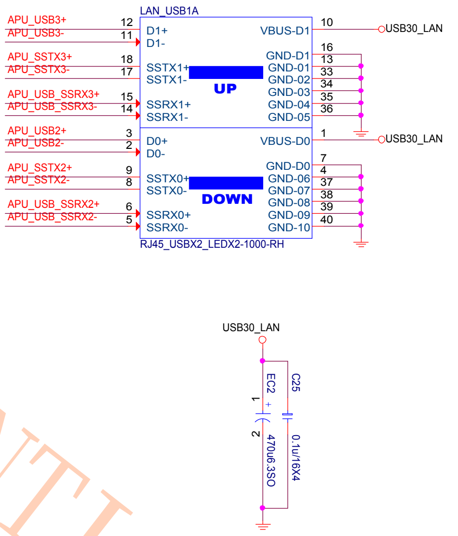
MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

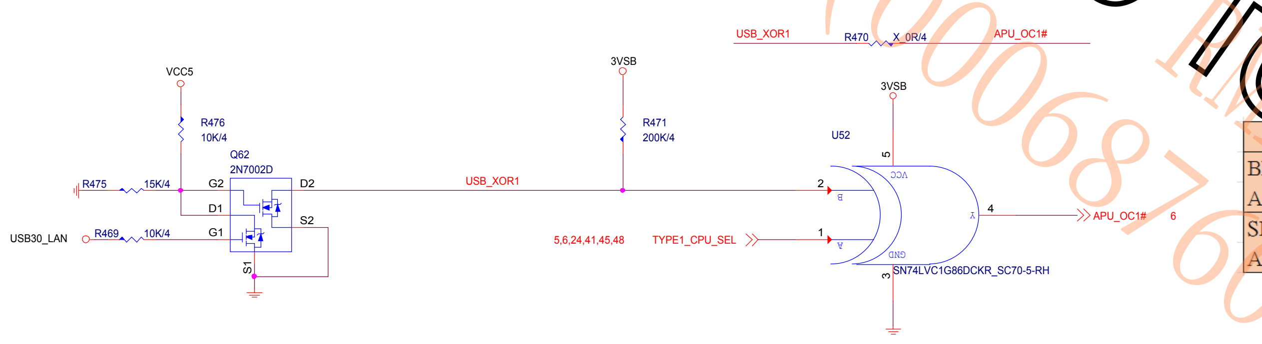
Title	USB Rear PS2+USB2.0	
Size: Custom	Document Number: MS-7A40	Rev: 20
Date: Thursday, May 17, 2018	Sheet 22 of 55	

USB3.1 GEN1



LAN+USB





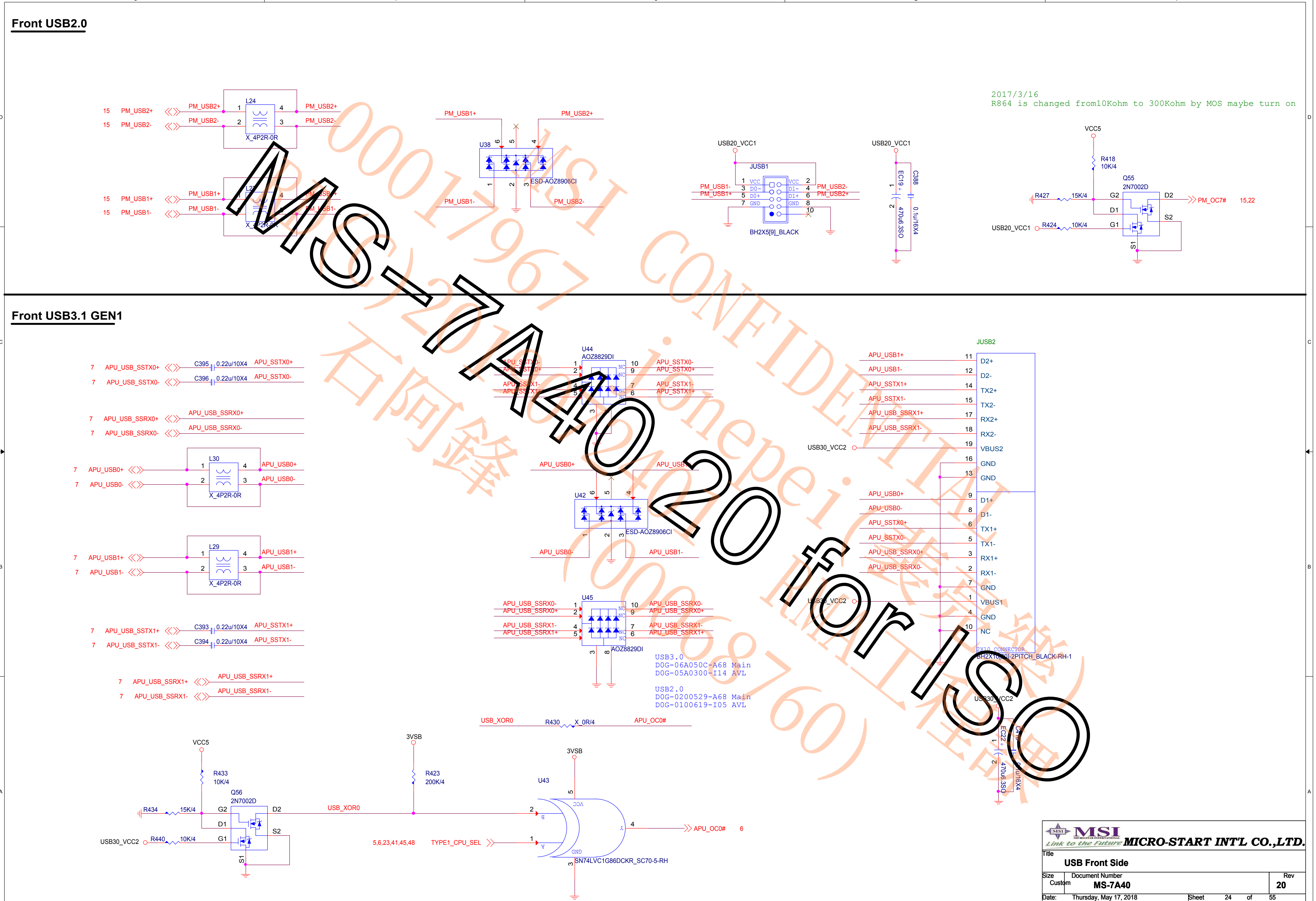
	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MICRO-START INT'L CO.,LTD.

Title: USB Rear LAN+USB3.1 GEN1

Size	Document Number	Rev
Custom	MS-7A40	20

Date: Thursday, May 17, 2018 Sheet 23 of 55

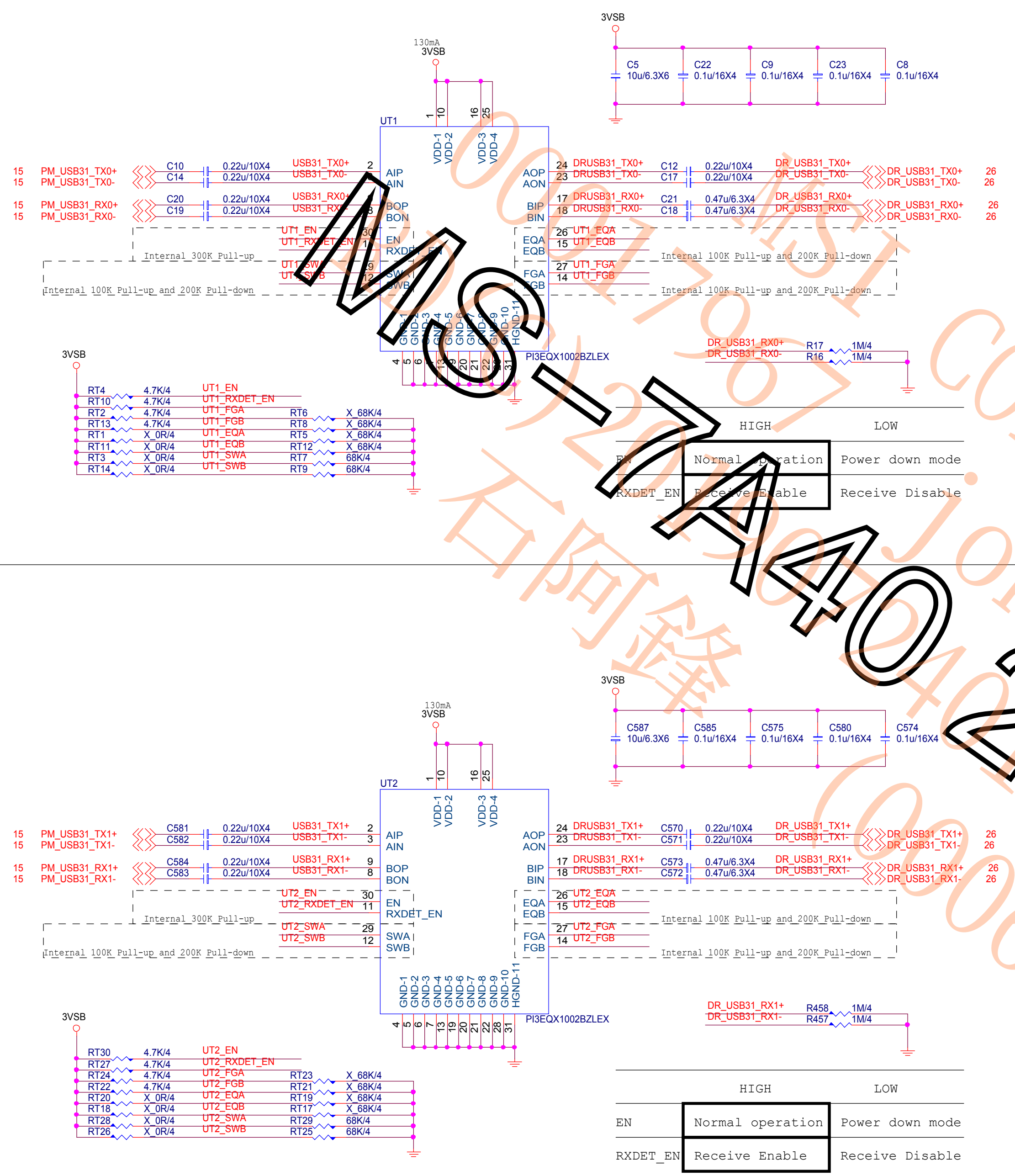


MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: **USB Front Side**

Size: Custom | Document Number: **MS-7A40** | Rev: **20**

Date: Thursday, May 17, 2018 | Sheet 24 of 55



EQA/B are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B	*@2.5GHz*	*@5GHz*
0	5.1	10.9
R	1.9	6.7
F	3.5	8.9 (Default)
1	6.8	13.1

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

	Flat Gain Settings
FGA/B	*dB*
0	-3
R	-1.5
F	0 (Default)
1	+2

-1dB compression point linear Swing Setting:

SWA/B are the selection bits for the output linear swing setting

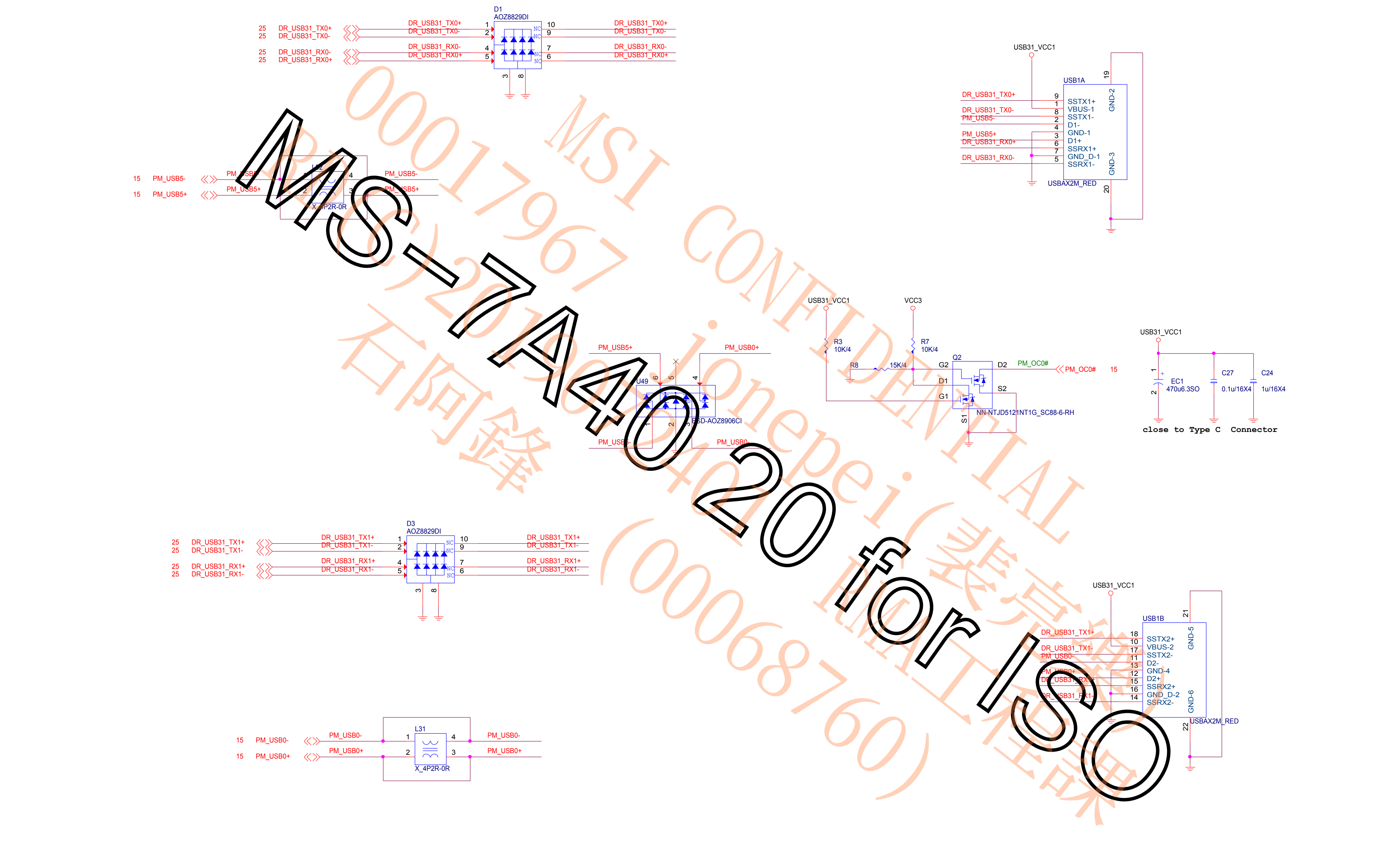
	Output Linear Swing Settings
SWA/B	*mVppd*
0	800
R	1200
F	1000 (Default)
1	1100

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: USB 3.1 Gen2 redriver

Size: Custom | Document Number: MS-7A40 | Rev: 20

Date: Thursday, May 17, 2018 | Sheet 25 of 55

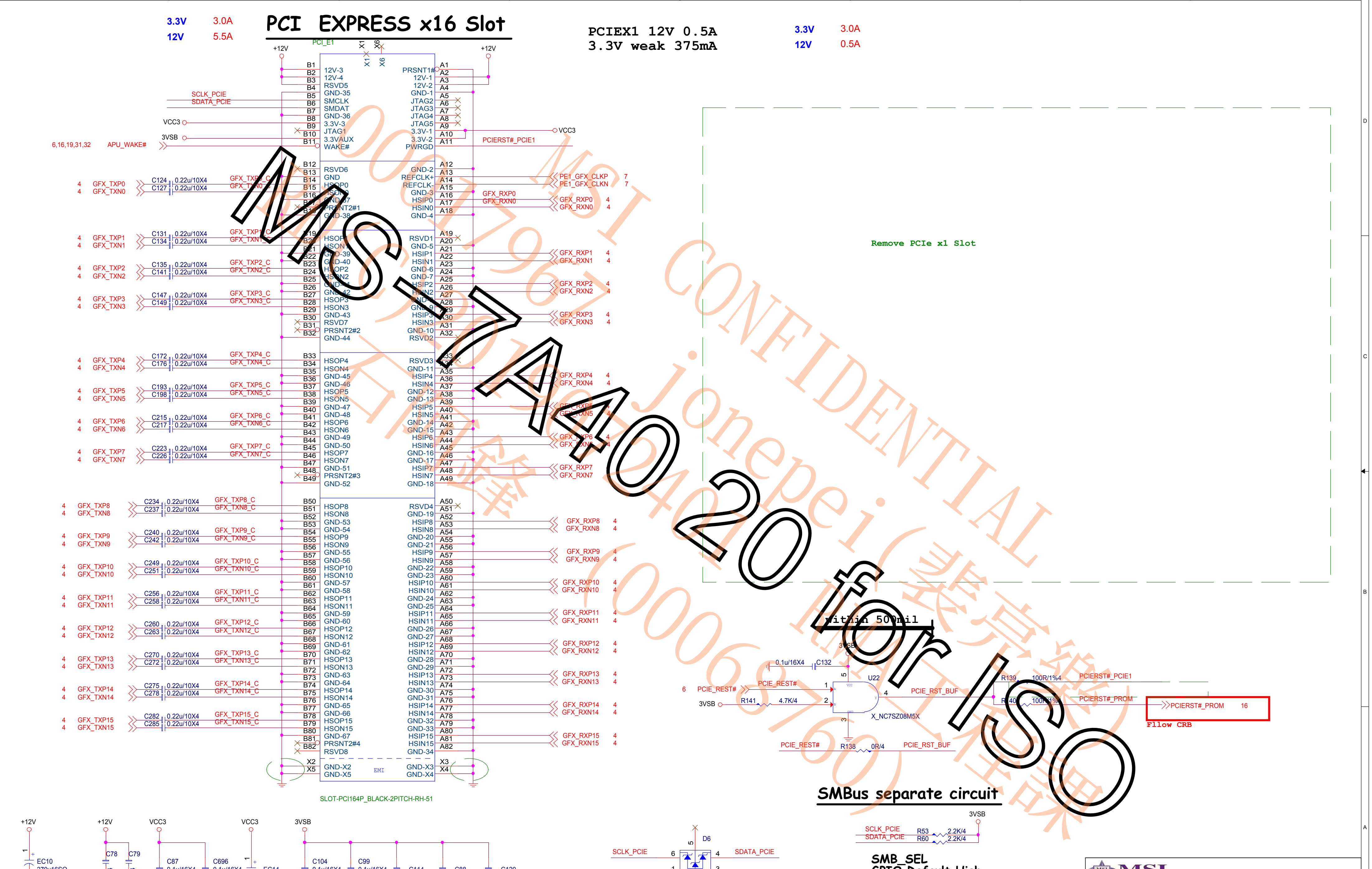


MICRO-START INT'L CO.,LTD.

Title: USB 3.1 GEN2 TYPE A*2

Size	Document Number	Rev
Custom	MS-7A40	20

Date: Thursday, May 17, 2018 — Sheet 26 of 55

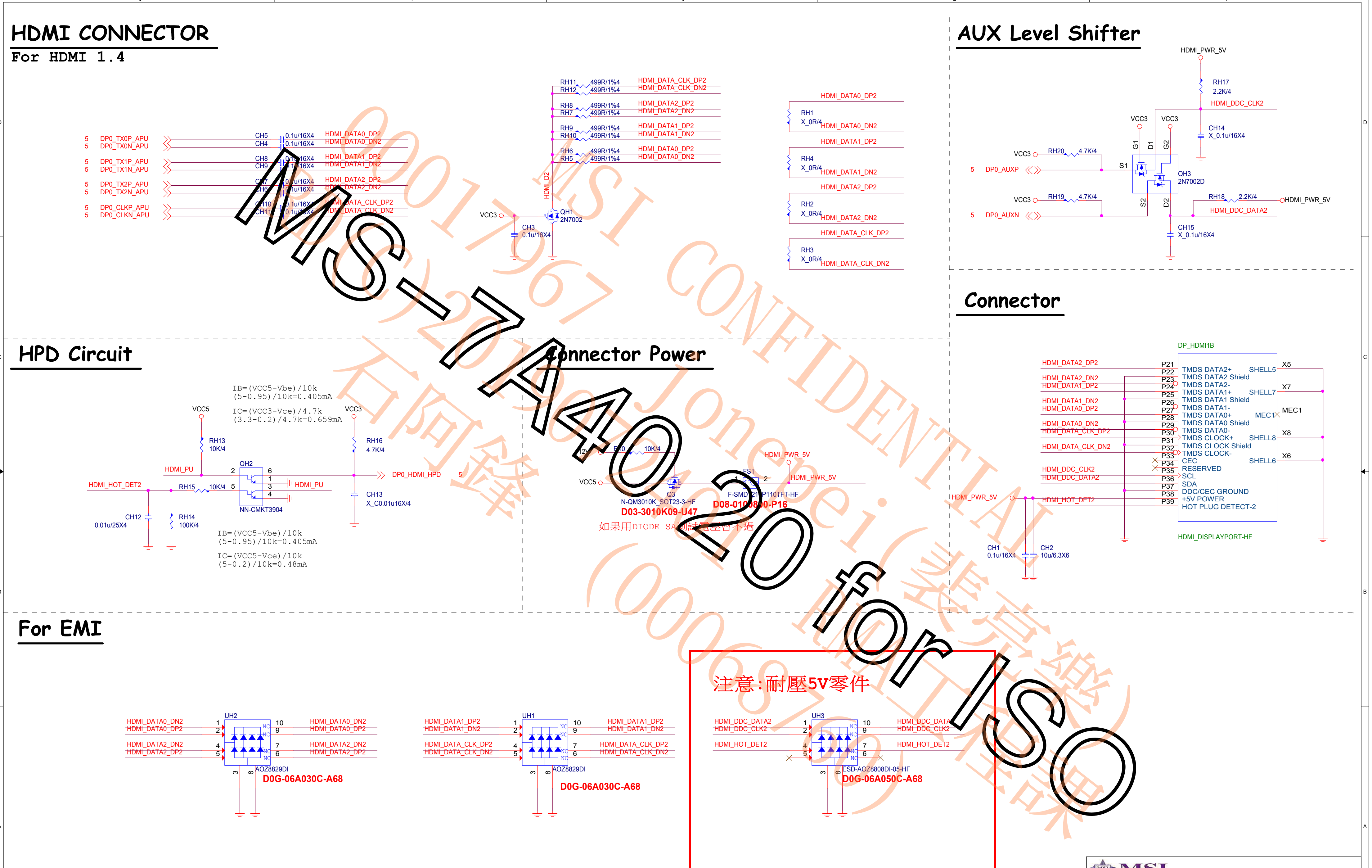


MICRO-START INT'L CO.,LTD.

Title: PCIE X16 SLOT

Size	Document Number	Rev
Custom	MS-7A40	20

Date: Thursday, May 17, 2018 Sheet 27 of 55



MICRO-START INT'L CO.,LTD.

Title: HDMI Connector

Size	Document Number	Rev
Custom	MS-7A40	20

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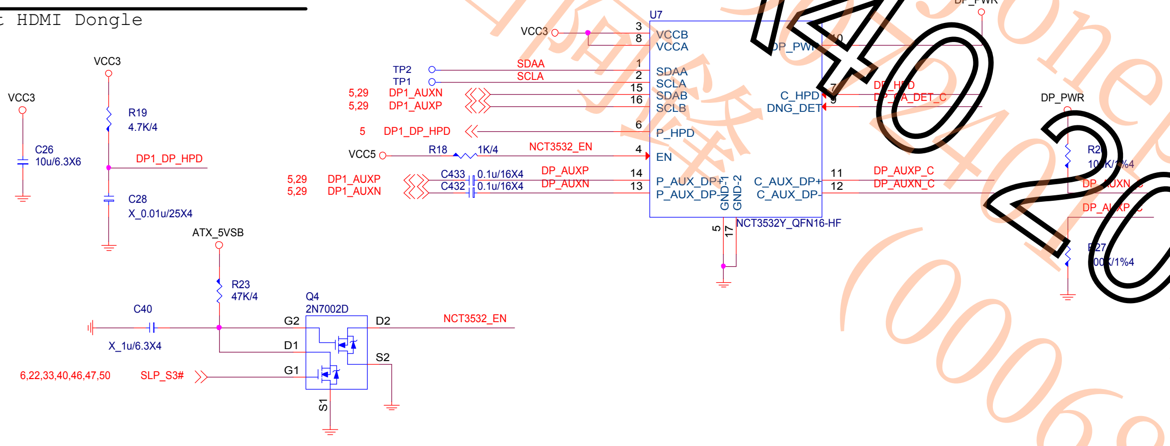
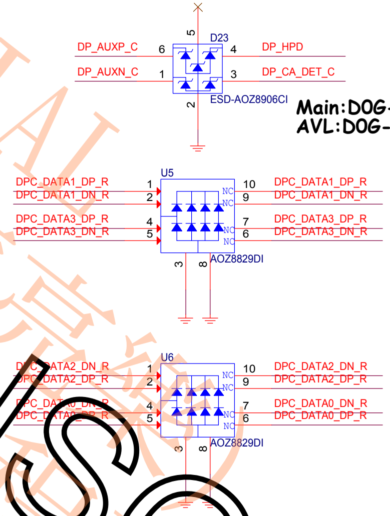
DP CONNECTOR

DP AUX & HPD Circuit

Support HDMI Dongle



ESD



Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

MSI MICRO-START INT'L CO.,LTD.

Title	DP Connector	
Size: Custom	Document Number: MS-7A40	Rev: 20
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SATA Connector

MICRO-START INT'L CO.,LTD.

Title	SATA Connector	
Size: Custom	Document Number: MS-7A40	Rev: 20
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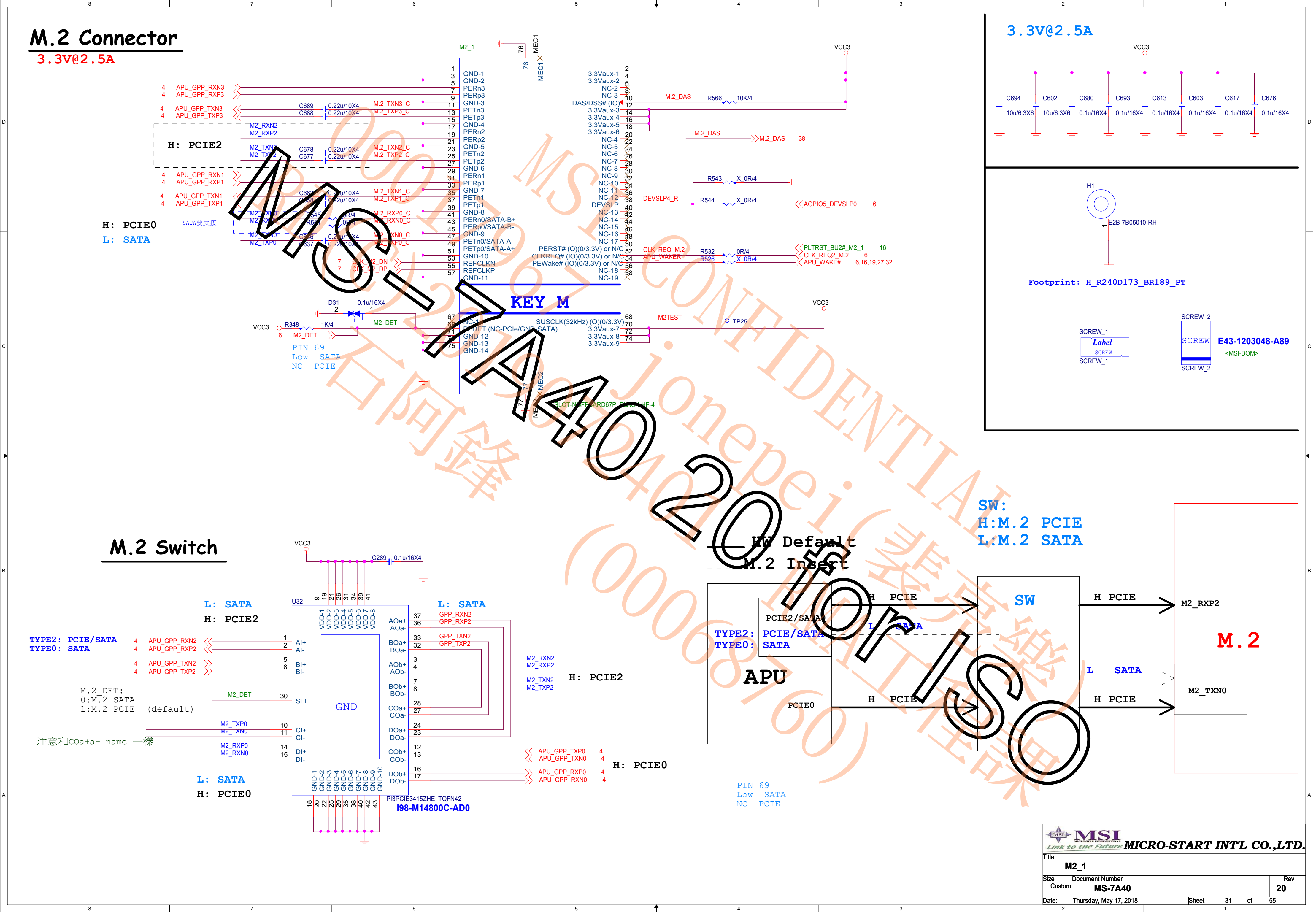

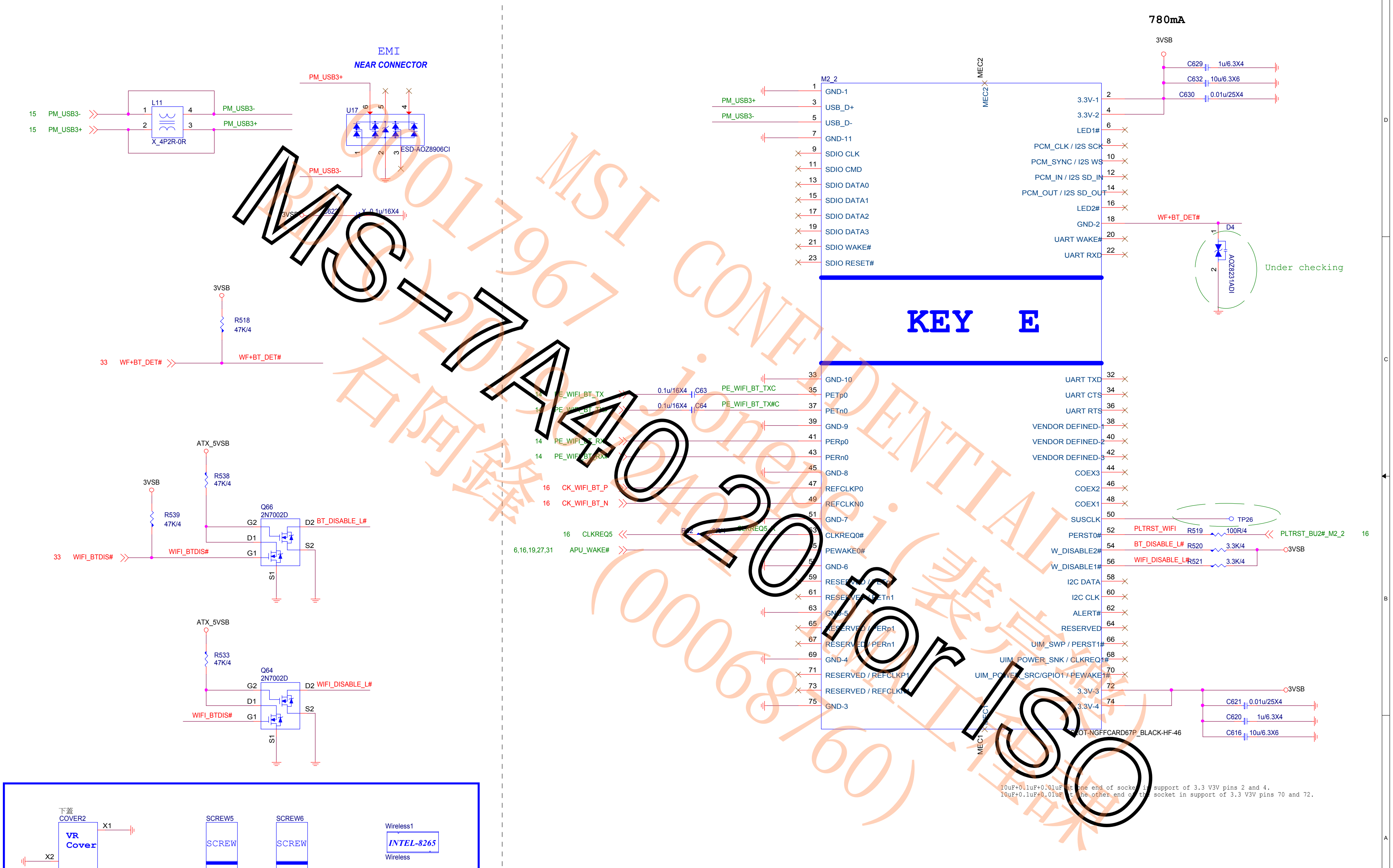

MSI MICRO-START INT'L CO.,LTD.

Title: M2_2(WIFI & BT)

Size	Document Number	Rev
Custom	MS-7A40	20

Date: Thursday, May 17, 2018 — Sheet 32 of 55

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Co-Lay NCT6795

(PIN9)(RTSB#)80_ENA	0=Disable	1=Enable
(PIN10)(DTRB#)80_ENB	0=Disable	1=Enable
(PIN32)(DTRA#)FANOUT	0=50%	1=100%
(PIN12)TEST_MODE_EN1	0=Disable	1=Enable
(PIN103)TEST_MODE_EN0	0=Disable	1=Enable
(PIN27)ESPI_EN0	0=LPC	1=ESPI
(PIN15)DDR4_EN	0=Disable	1=Enable

U16 NCT6795D-M

LPC Interface · DSW Interface · Printer mode · Port80 LED Control · GPIO · Debug · Harddware Monitor · JAR SIR · KBC Function · FAN Control · ACPI Function · Power Pin

3V Analog Power Closed PIN108

Thermal Monitor

For System Close to SIO

For CPU Under Socket

Close to CPU MOS

For CPU 2016/05/24 Add

For PROM 2016/11/03 Add

Place to under Promontory

Closed PIN99 · Closed PIN24,108 · Closed PIN46,85

2015.05.19 Stuff

Power Fault detect through VIN0,VIN1

MS-17A40 for ISO

Title	SIO NCT6795
Size	Custom
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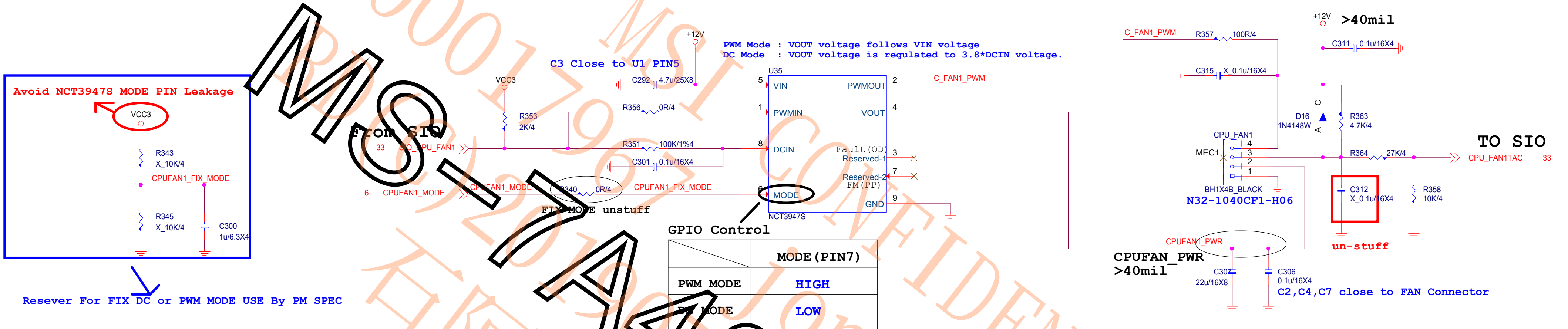
MICRO-START INT'L CO.,LTD.

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

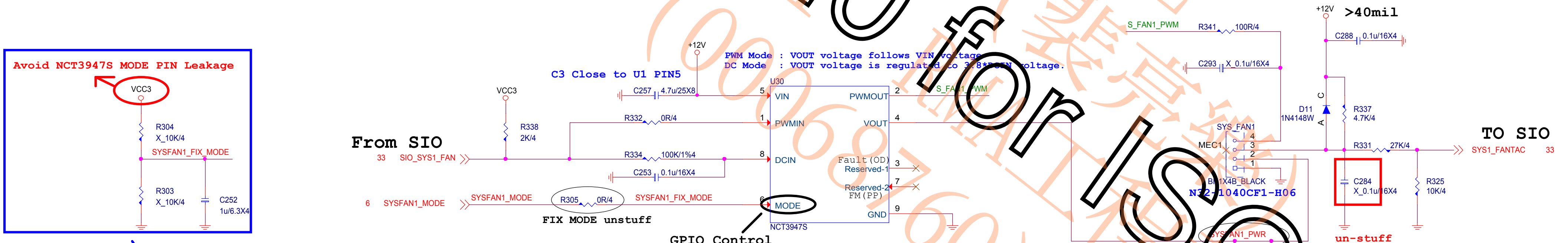
2.GPIO可以由BIOS切換 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V

MSI MICRO-START INT'L CO.,LTD.

Title	CPU/SYS FAN Control TYPE K	
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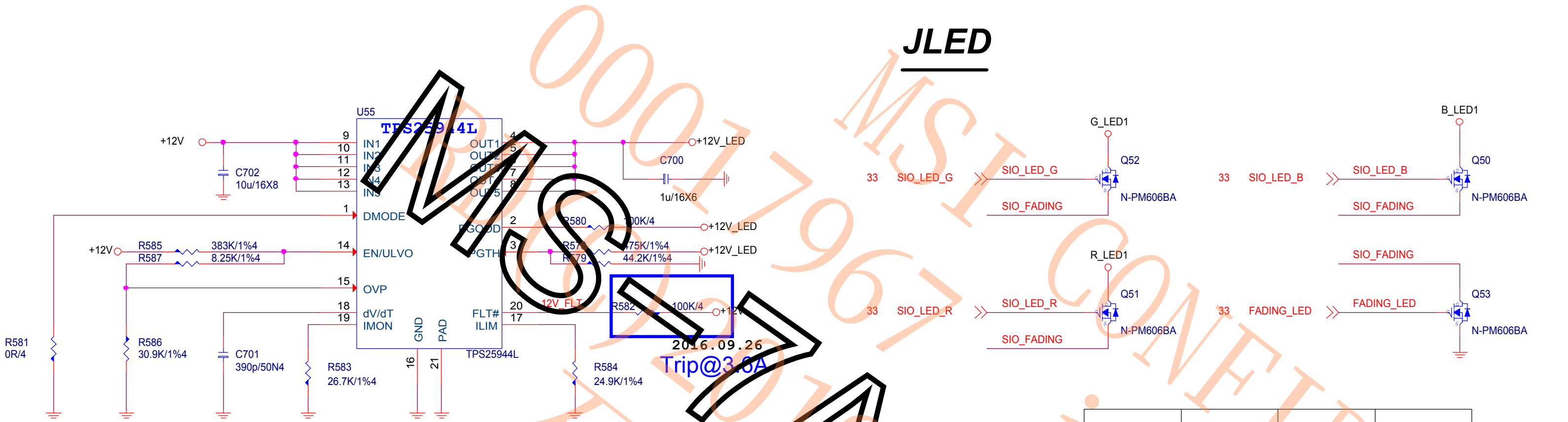
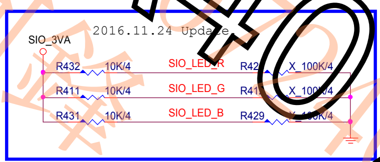
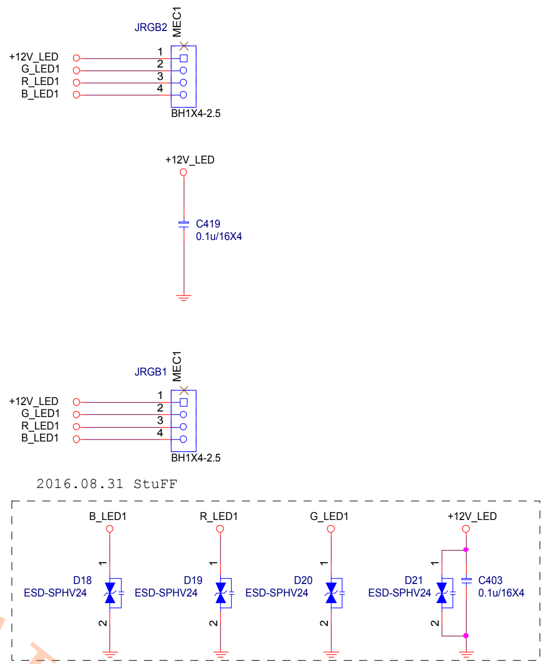
定義:外接LED 燈條
---- 彩色 : SIO 6795D-M(128pin) : OB2-7A58001
---- 單色 : SIO 5565(64pin) : B02-5565D04-N62
---- PCB 文字面 (JLED)
---- 手冊 註明接頭支援標準 5050 RGB or 單色 LED 共陽燈條 (12V+/G/R/B) or (12V+/-/S/-) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JLED

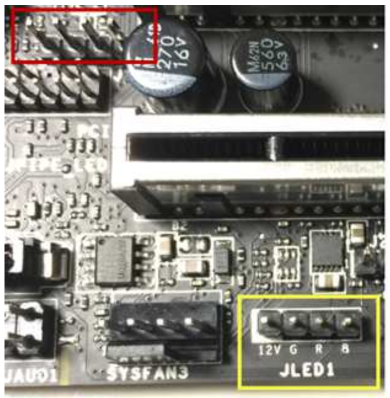




Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

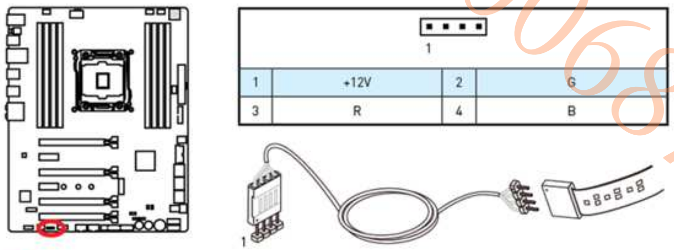


close to JLED2



JLED1: RGB LED connector

This connector allows you to connect the RGB LED strip.

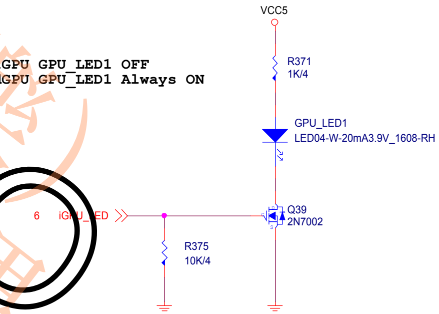


Important

- This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.
- Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.
- Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.

AM4 APU Detect LED Circuit

iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON



MSI MICRO-START INT'L CO.,LTD.
Title: 6795 RGB LED
Size: Custom | Document Number: MS-7A40 | Rev: 20
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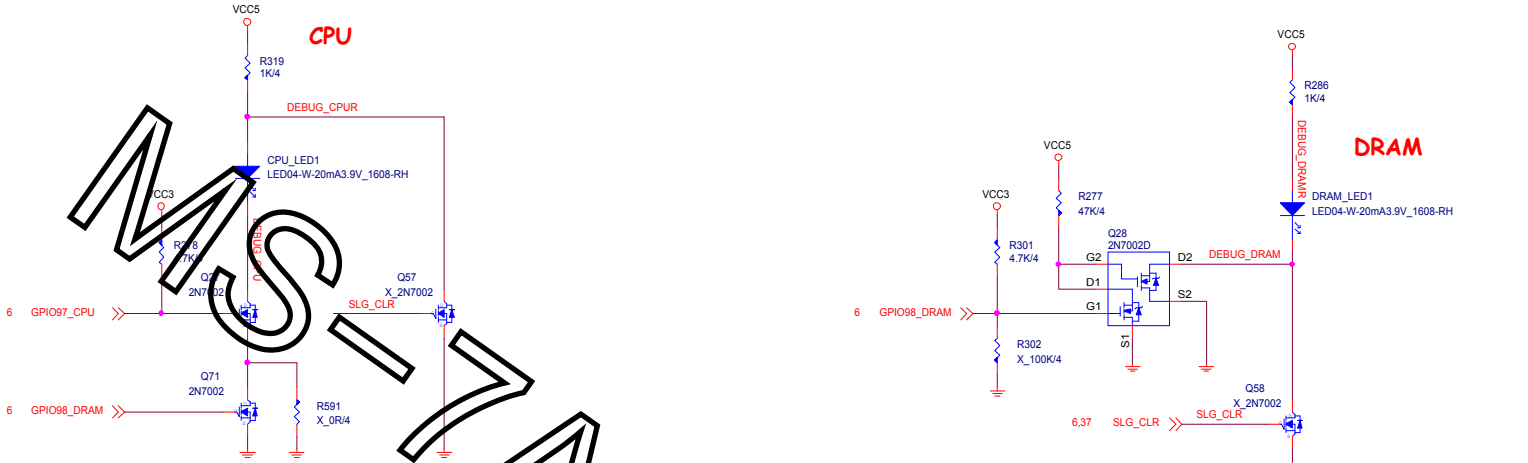
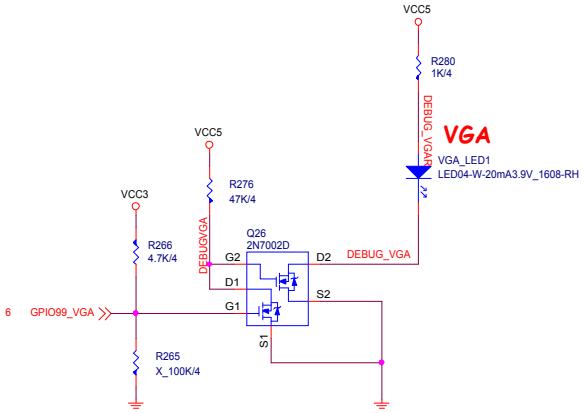
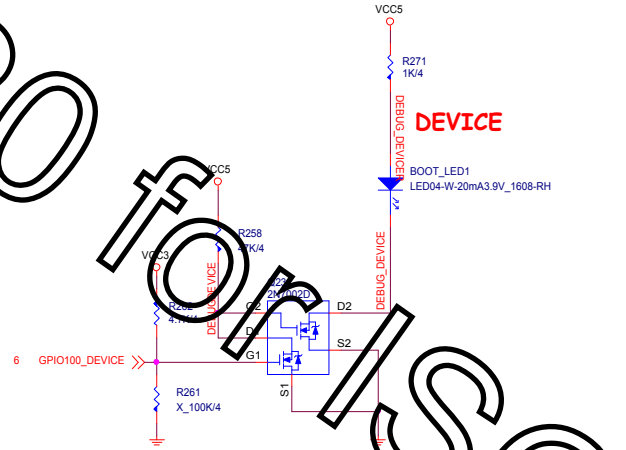
EZ Debug LED







LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: EZ Debug LED		
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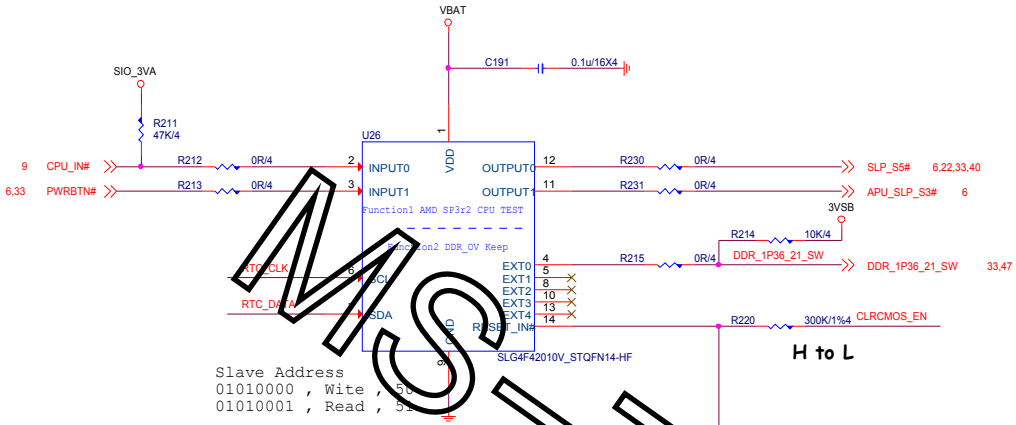
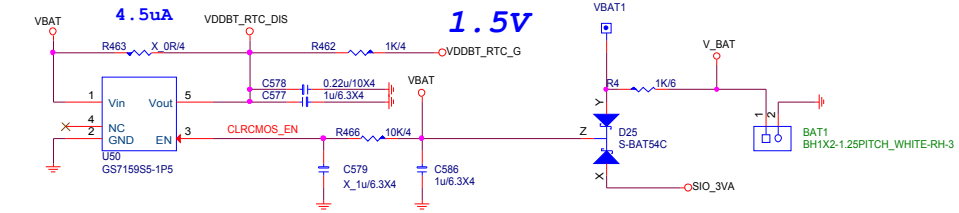
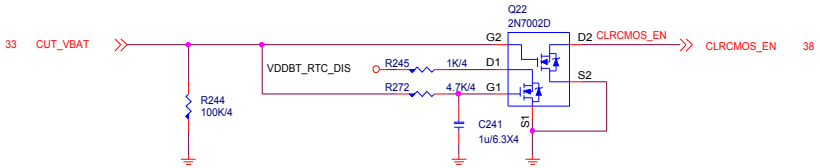
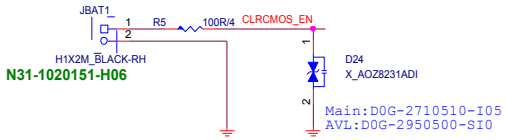


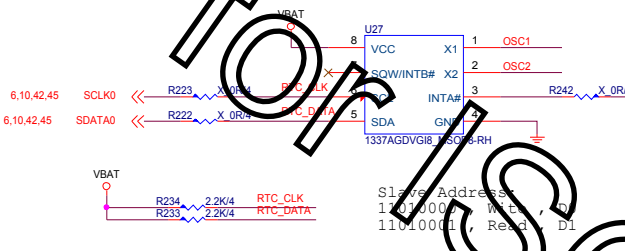
RTC & Clear CMOS Circuit

Placement Bottom Side

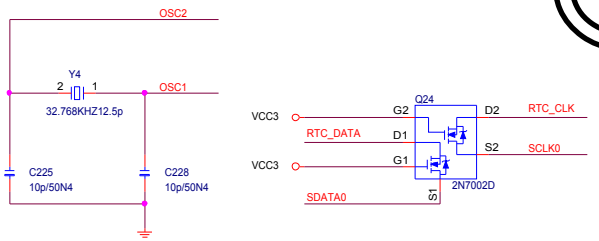








Slave Address
11010000 , Wite , D0
11010001 , Read , D1



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Link to the Future

Title	RTC Circuit / Moat Cap	
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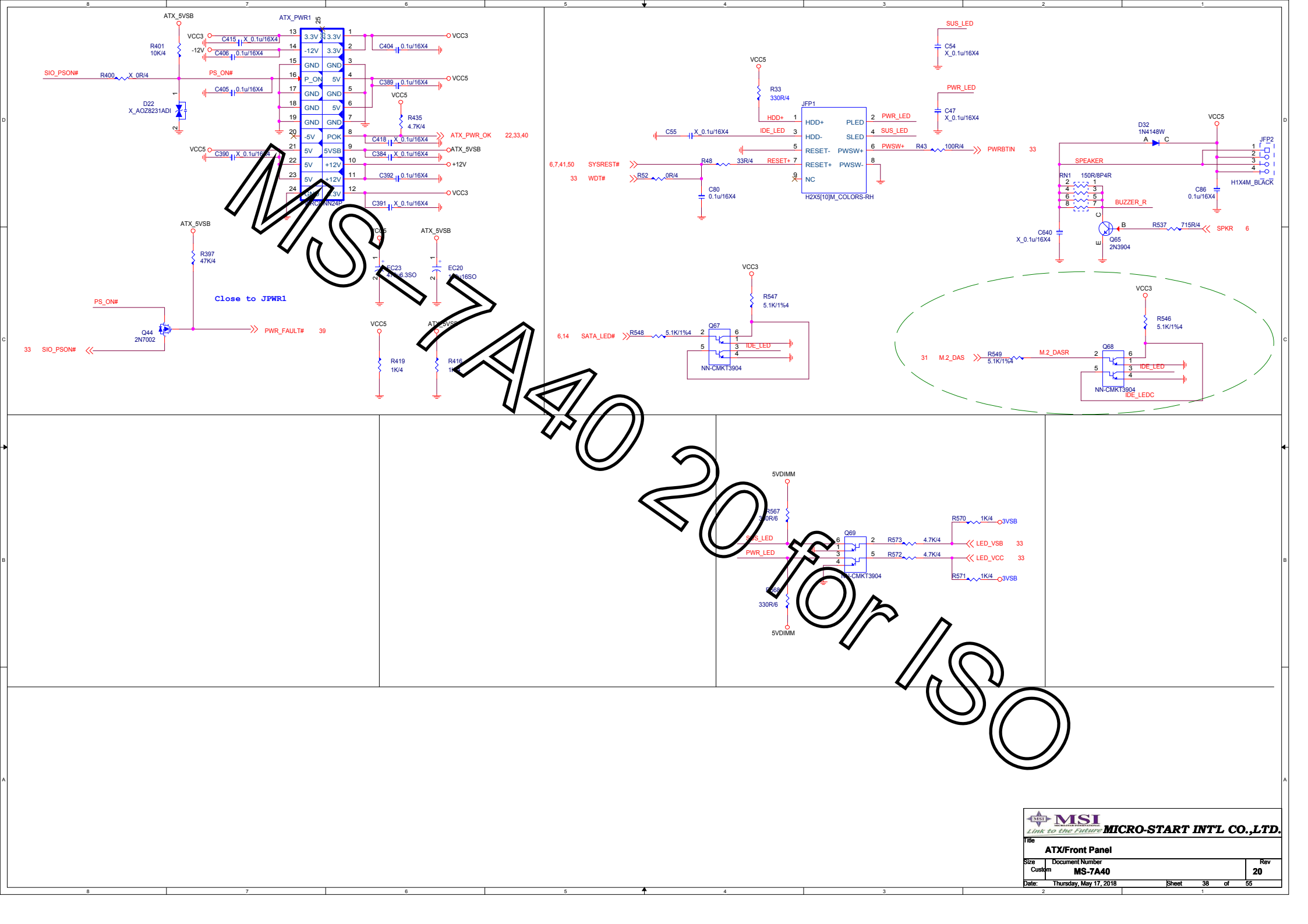

MICRO-STAR INT'L CO.,LTD.

Title: ATX/Front Panel

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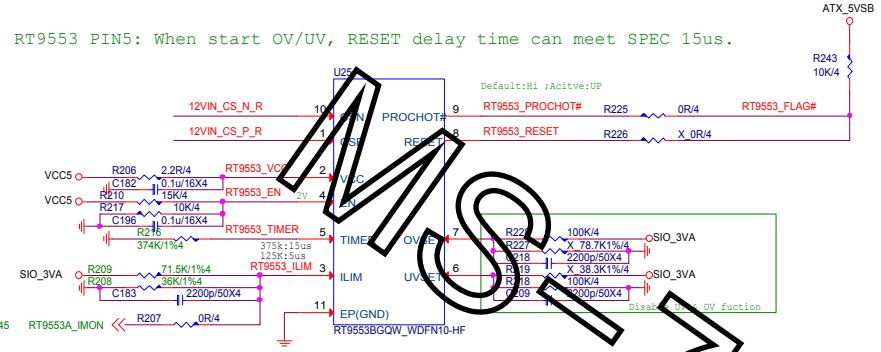
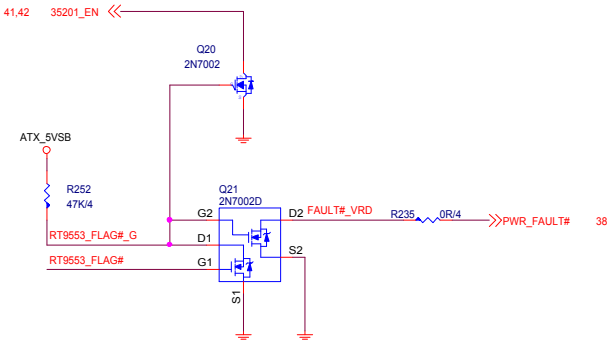
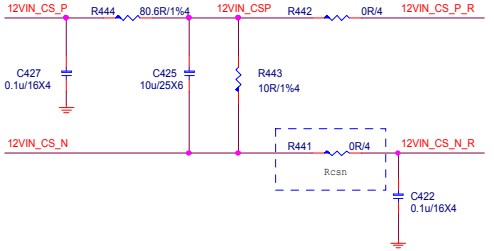
RT9553B CURRENT SENSE

VCORE EDC MAC 125A

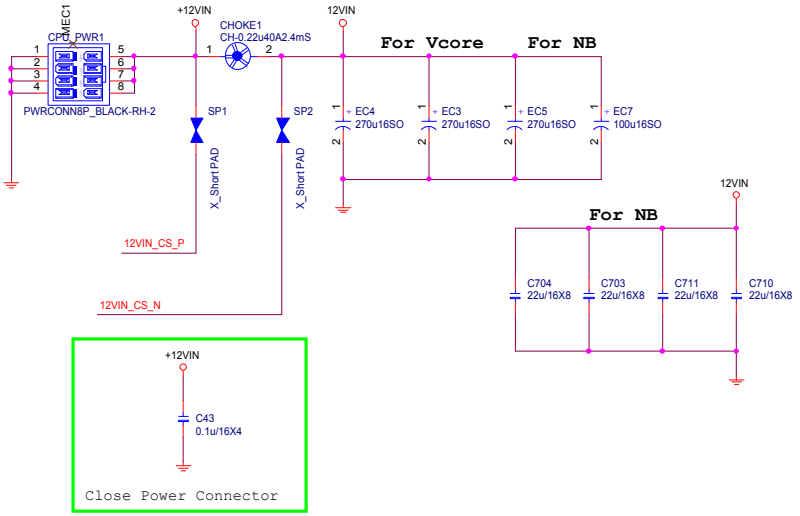
NB EDC MAX75A







CPU POWER CONNECTOR



D=Vout/Vin		
Vin	=	12
Vout	=	1.5
D	=	0.125

I o = Icore(max)*0.6		
I core(max)	=	125 > Vcore current
I avg.	=	100 A

I ripple={ Io*√D*√(1-D)} / Phase		
Phase	=	4 6 phase
I ripple	=	A

5.511982

How many pcs. Of Cap.		
I ripple(cap)	=	5000 m A
COE TEMP	=	1
Input Cap.	=	2 pcs.

CORE:
D = Vout/Vin
= 1.5/12
= 0.125
N = 6
Irms = Iout * [D/N - (D)^2]^(1/2)
= 125 * (0.02083 - 0.015625)^(1/2)
= 9.0182A

D=Vout/Vin		
Vin	=	12 > input voltage
Vout	=	1.2 > output Vcore
D	=	0.1

I o = Icore(max)*0.8		
I core(max)	=	75 > Vcore current
I avg.	=	60 A

I ripple={ Io*√D*√(1-D)} / Phase		
Phase	=	2 phase
I ripple	=	9 A

How many pcs. Of Cap.		
I ripple(cap)	=	5000 m A
COE TEMP	=	1
Input Cap.	=	2 pcs.

NB:
D = Vout/Vin
= 1.2/12
= 0.1
N = 2
Irms = Iout * [D/N - (D)^2]^(1/2)
= 75 * (0.05 - 0.01)^(1/2)
= 15A

MICRO-START INT'L CO.,LTD.

Title		
RT9553 CURRENT SENSE		
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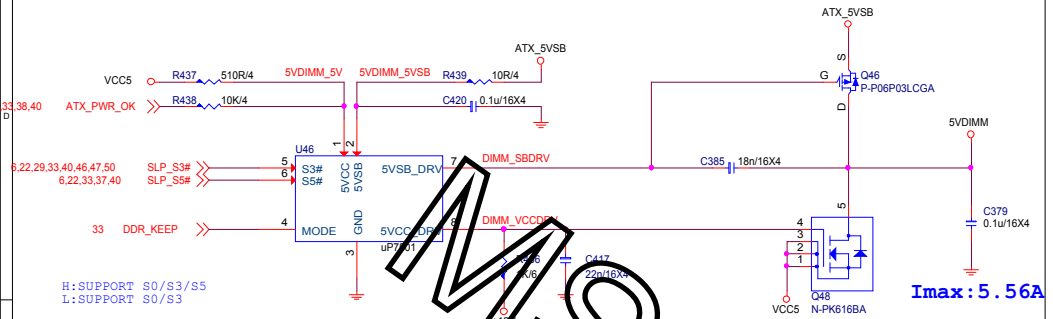
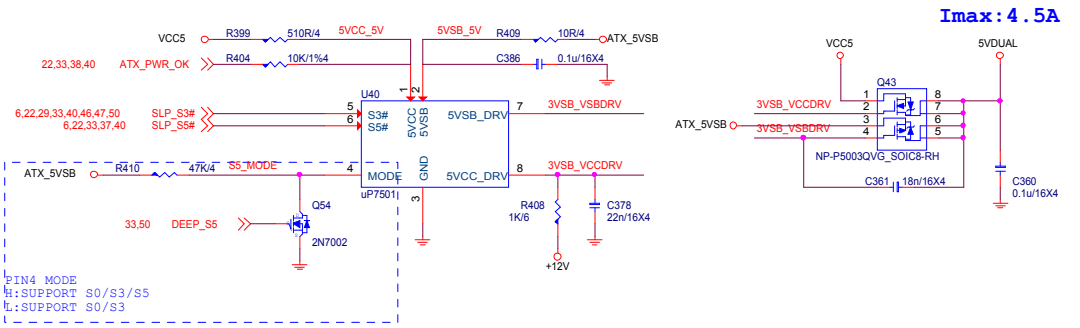
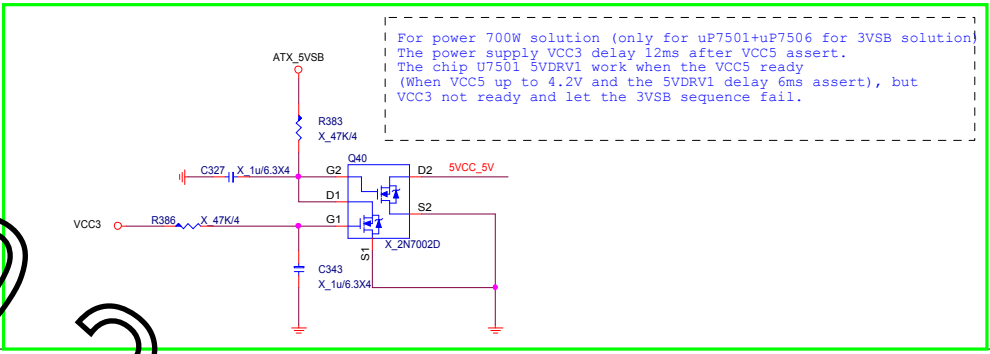
5VDIMM FOR DDR

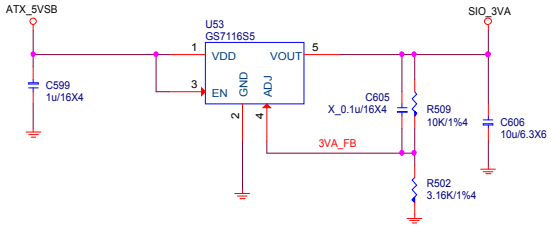


5VDUAL For 3VSB、CPU 1.8V 、 VDDP

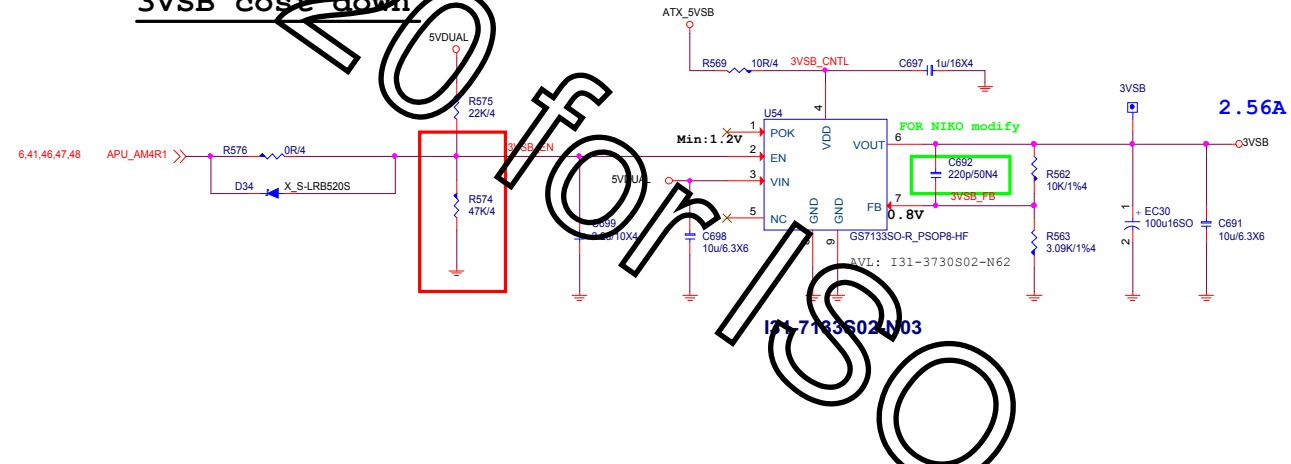




SIO_3VA



3VSB cost down



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Link to the Future

Title	ACPI uPI-5VDIMM&3VSB	
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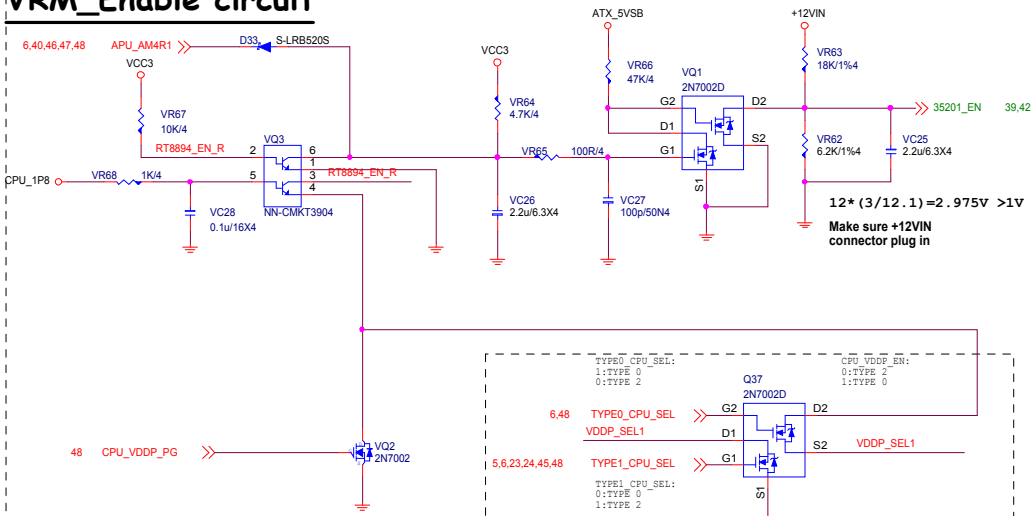
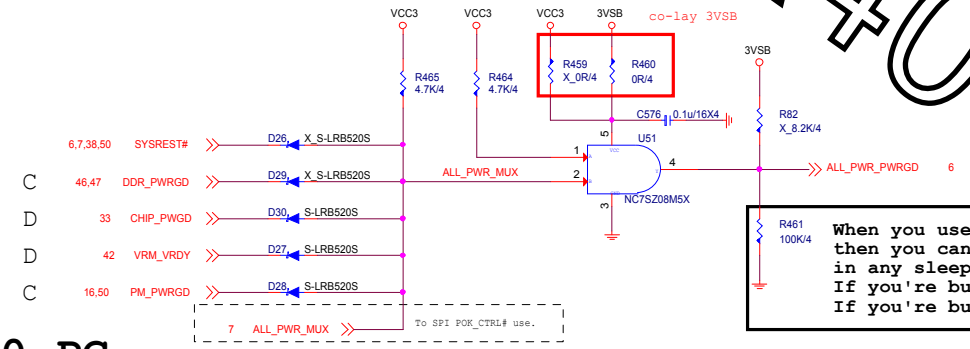
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

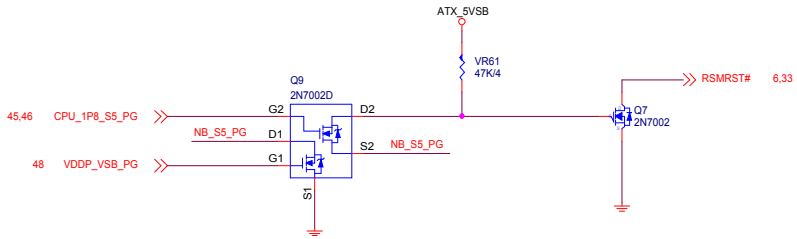


R461 100K/4

When you use external buffer,
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MS-7A40 2.0 for ISO

MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title	PWR Sequence	
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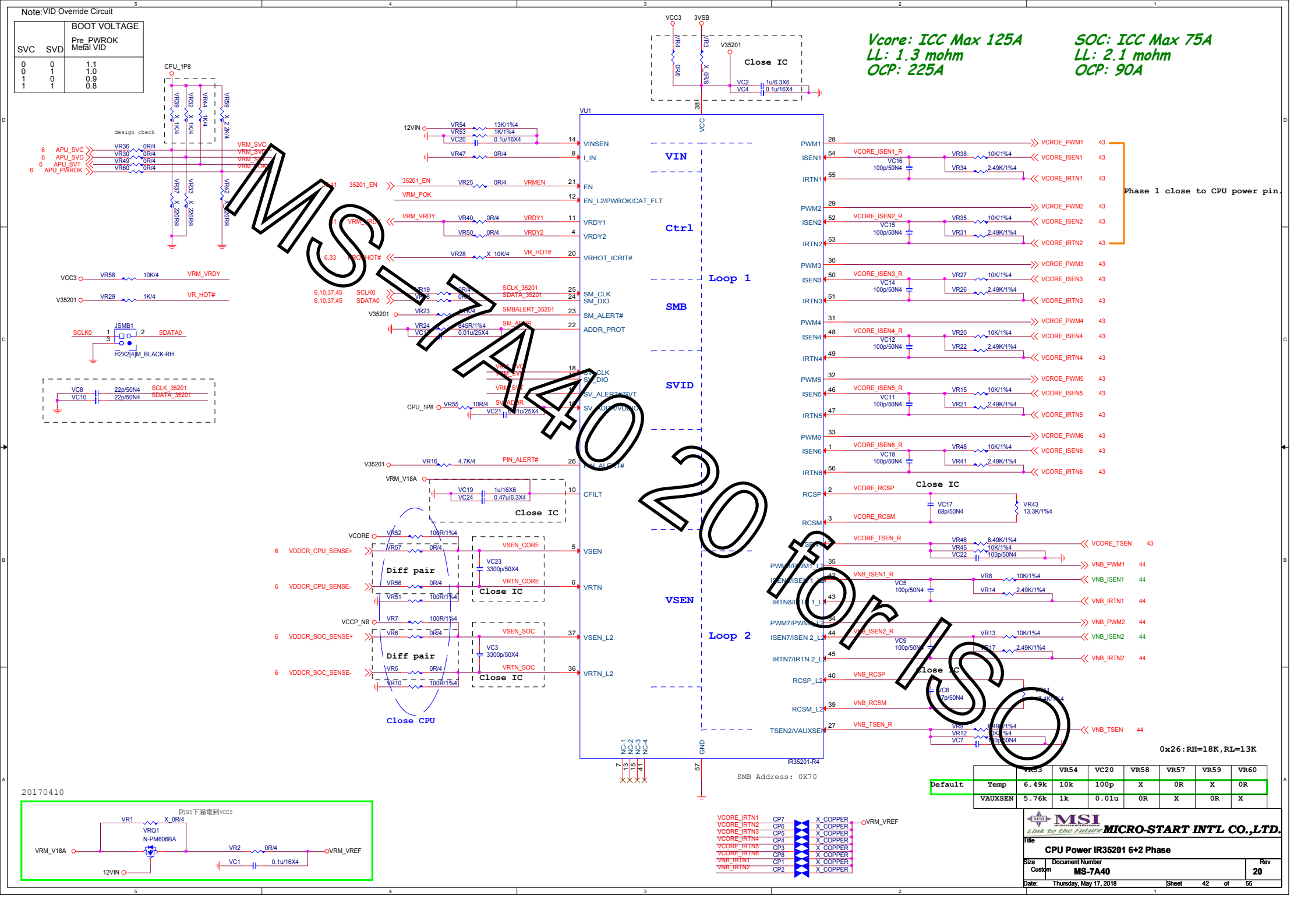
Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vcore: ICC Max 125A
LL: 1.3 mohm
OCP: 225A

SOC: ICC Max 75A
LL: 2.1 mohm
OCP: 90A



	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	CPU Power IR35201 6+2 Phase		
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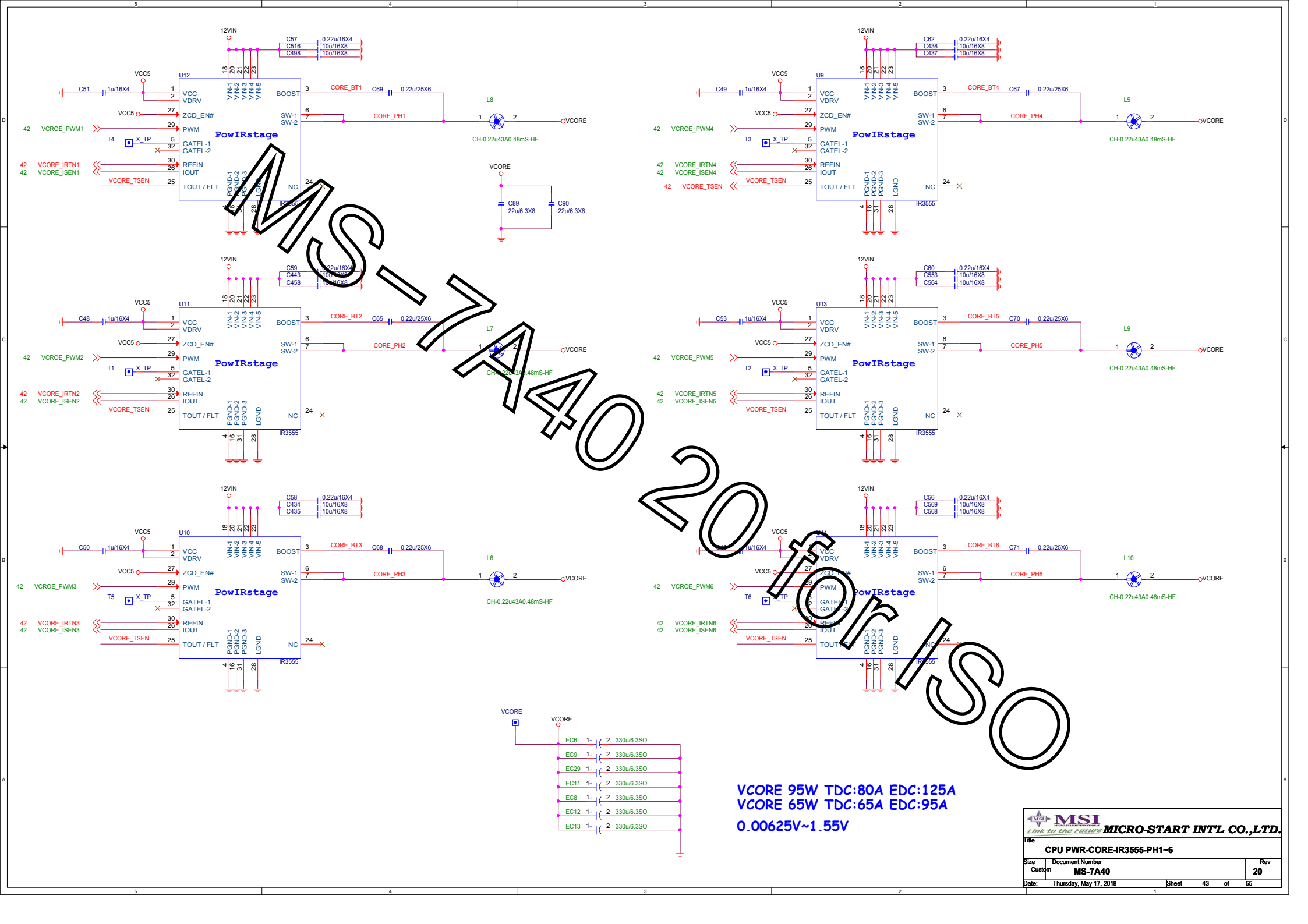

MS-7A40 20 for ISO

VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

0.00625V~1.55V

MICRO-STAR INT'L CO.,LTD.

Title	CPU PWR-CORE-IR3555-PH1~6	
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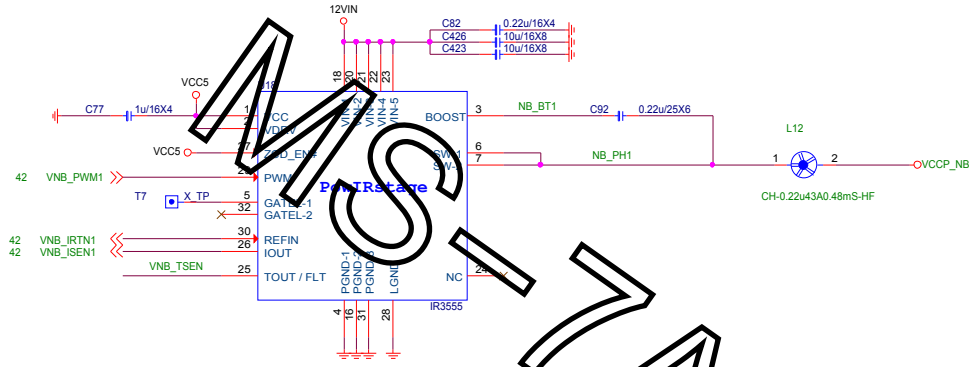
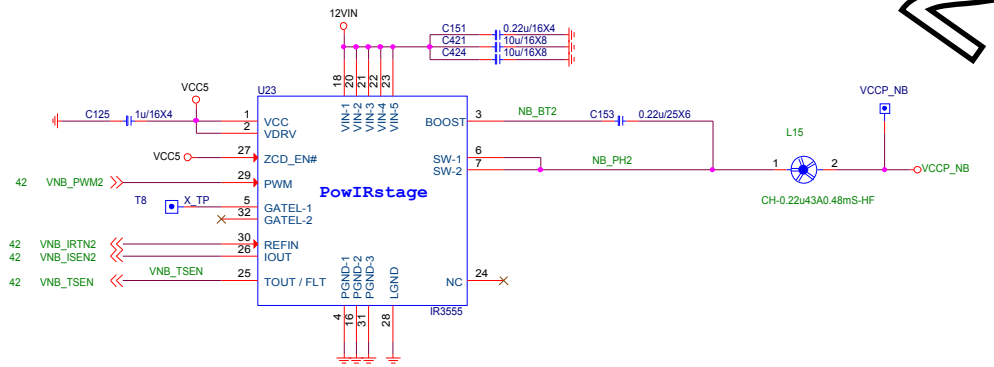
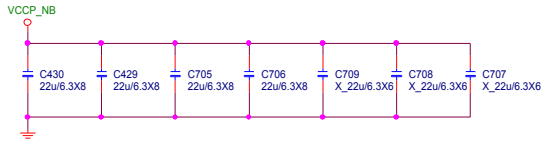
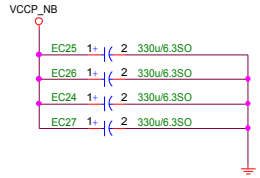
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

VCCP_NB OCP:100A









0.00625V~1.55V

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Title	CPU Power NB Phase 1-2	
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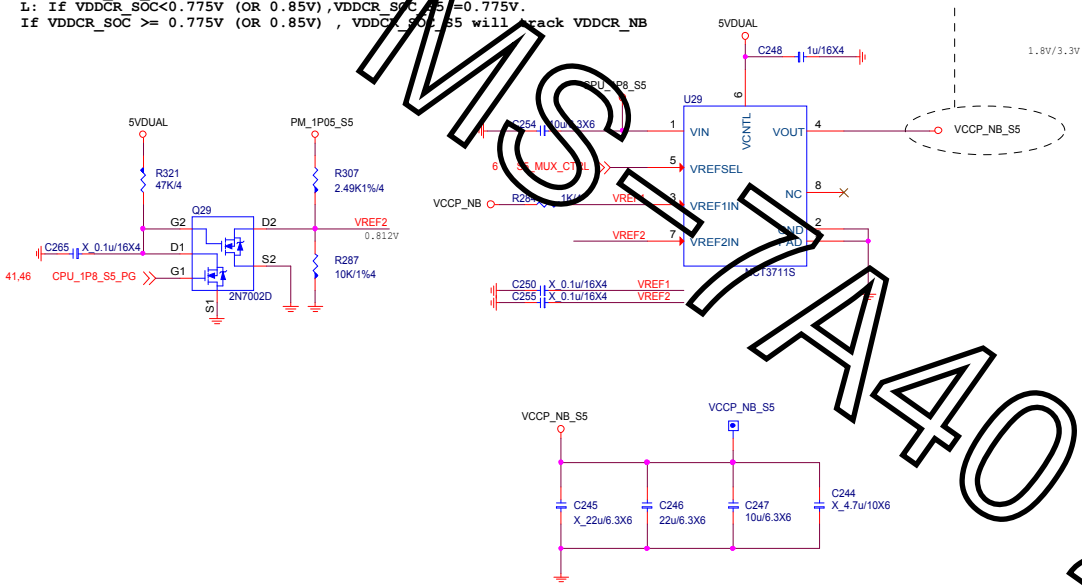
FOR
VCCP_SOC_s5
0.9A

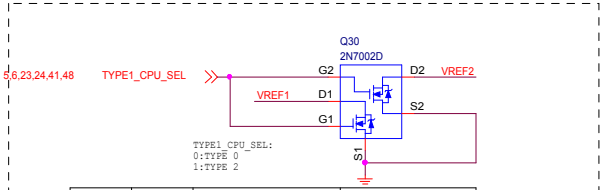
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0



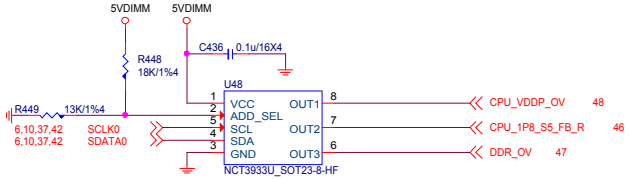


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

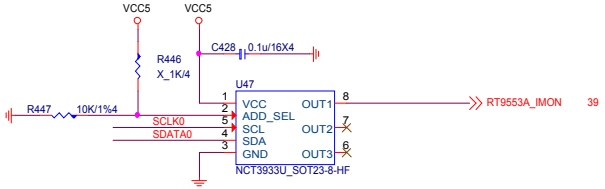
CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

0x26:RH=18K,RL=13K



0x2A:RH=OPEN,RL=10K



VR2 VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Title	CPU Power NB Switch/NCT3933	
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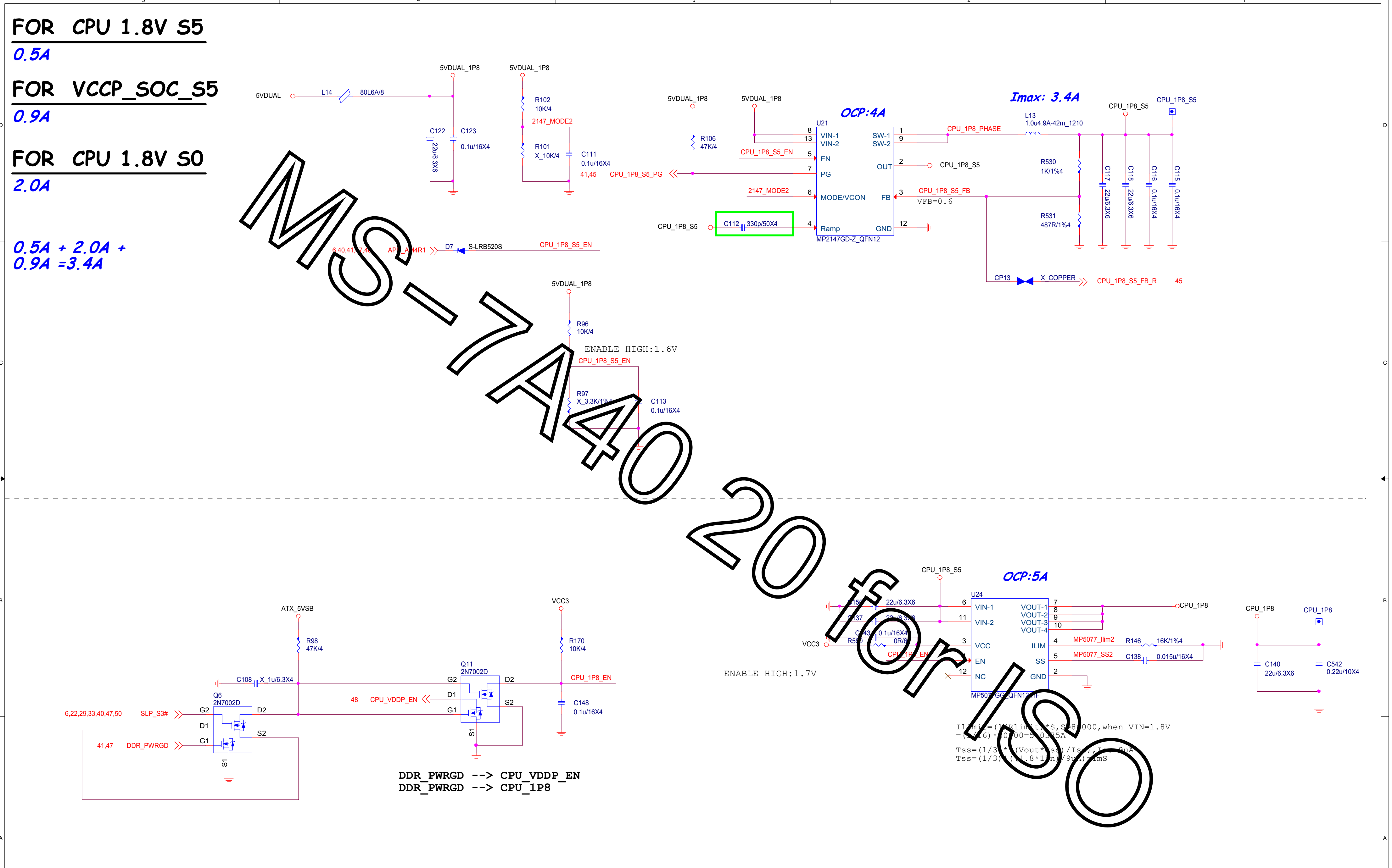

Title: CPU Power 1P8V-MP2147

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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM
0.6A FOR DDR VTT

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675 for 1.232V
L	0.75 for 1.369V

Imax: 20.85A

OCP:24A

f:400KHz

By layout modify

27.5A

FB:0.75V

R178=90.9K for OCP(dc)=24A (typ)
and OCP(dc)=23.8A(min)

Close to PIN19

1.1uH change to 0.47uH

1.2V

default=1.36V

R195=1K, R181=1.21K,
Vo=0.75V*(1+R195/R181=1.369V

I32-8231A0C-R11

MS-7A40 20 for ISO

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Title: DDR Power-RT8231AGQW			
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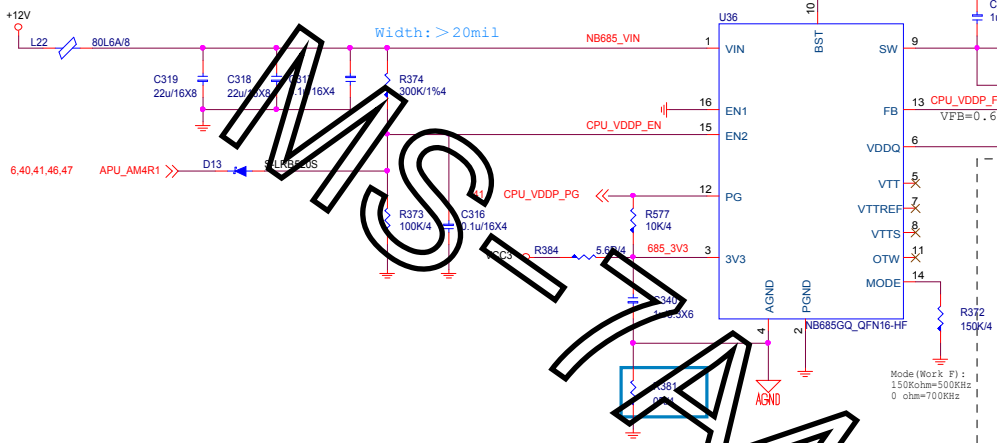
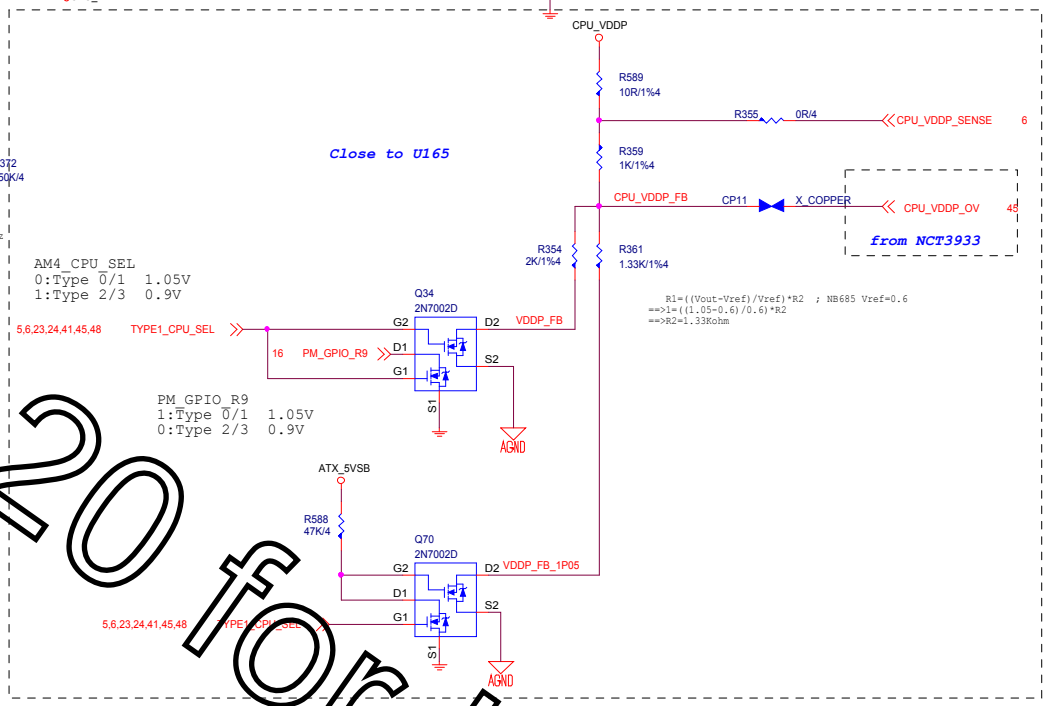
CPU_VDDP_S0

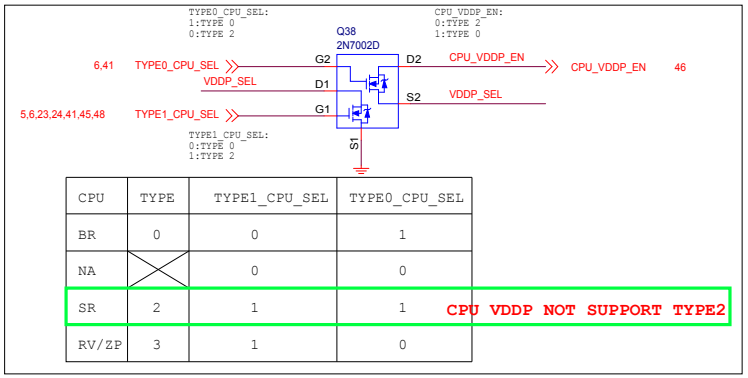
1.05V/0.9
S0:8.5A

OCP=15.45A

I9C-685GQ0C-M03





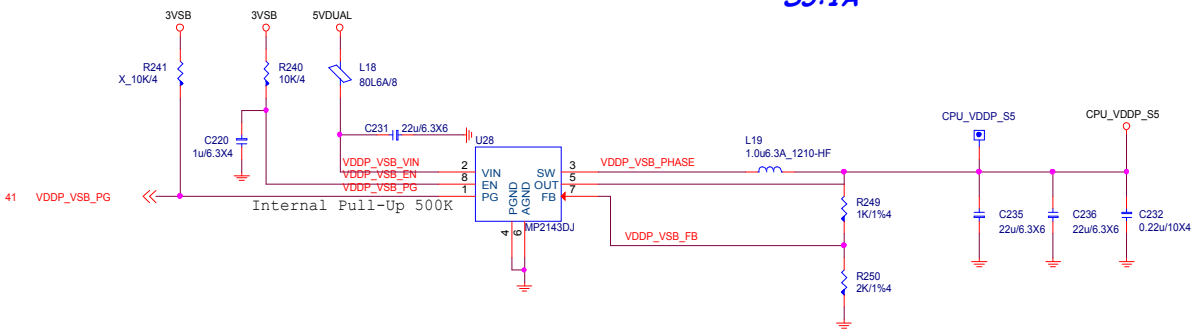


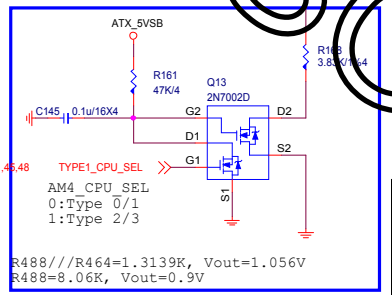
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

CPU_VDDP_S5

VDDP_S5
1.05V/0.9
S5:1A





MS-7A40 20 for ISO

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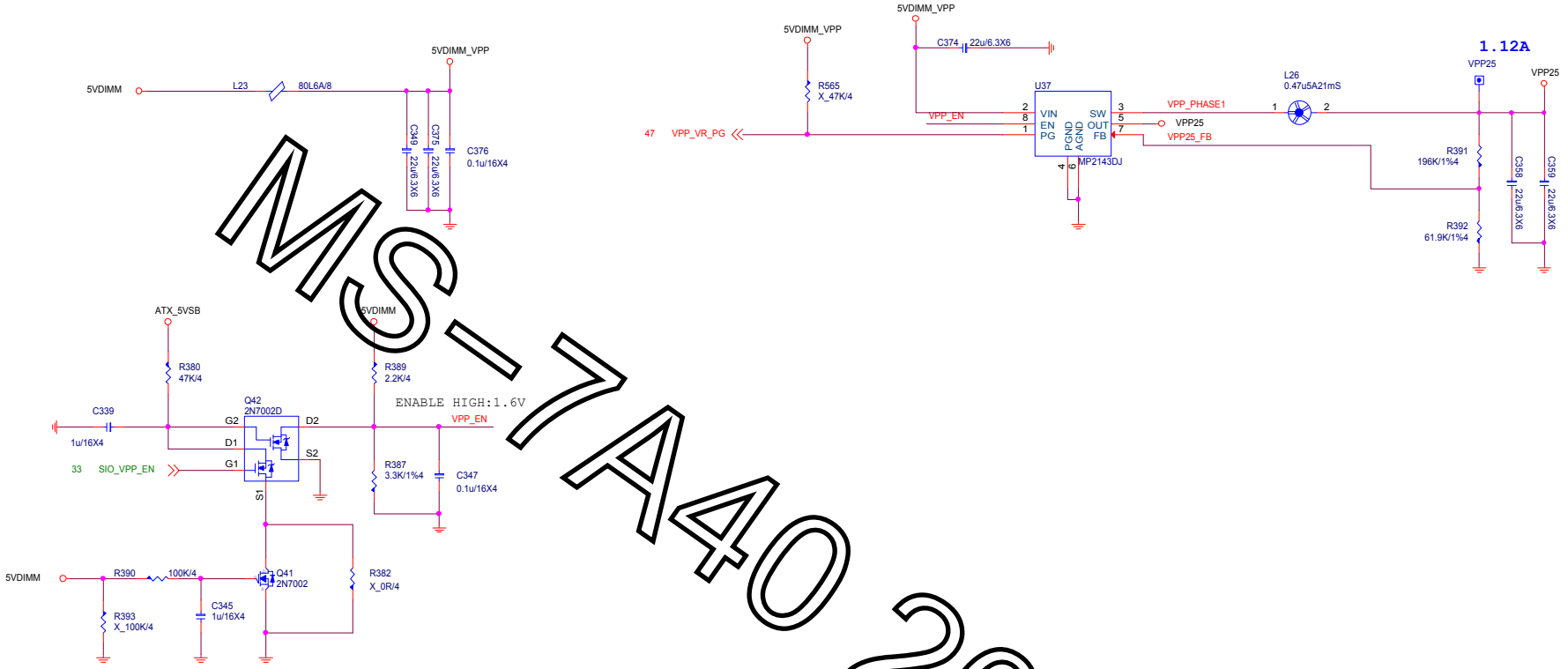
2DIMM :1.12A FOR DDR VPP2.5V



MSI MICRO-STAR INT'L CO.,LTD.
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Title: DDR PWR VPP25/VTT-MP2143		
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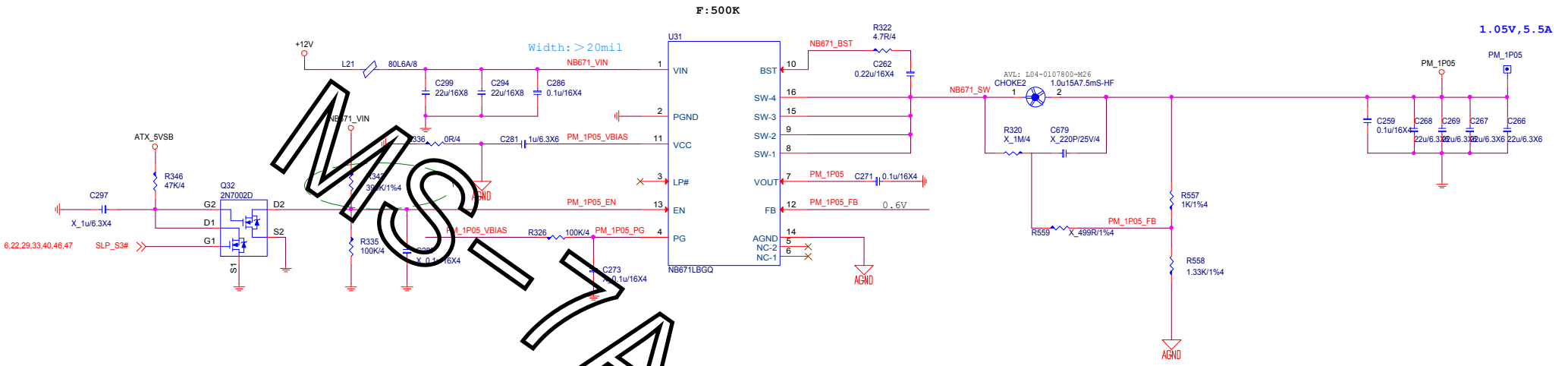
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

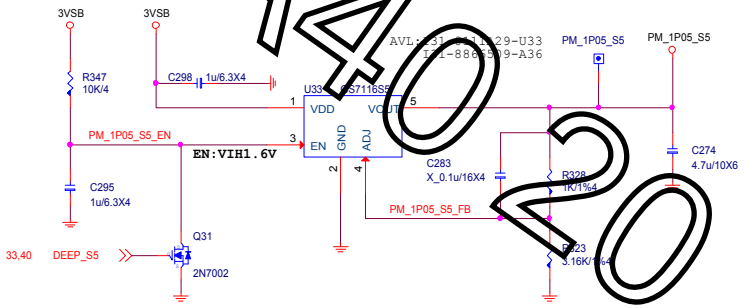
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH



FOR Promontory 1.05V_S5

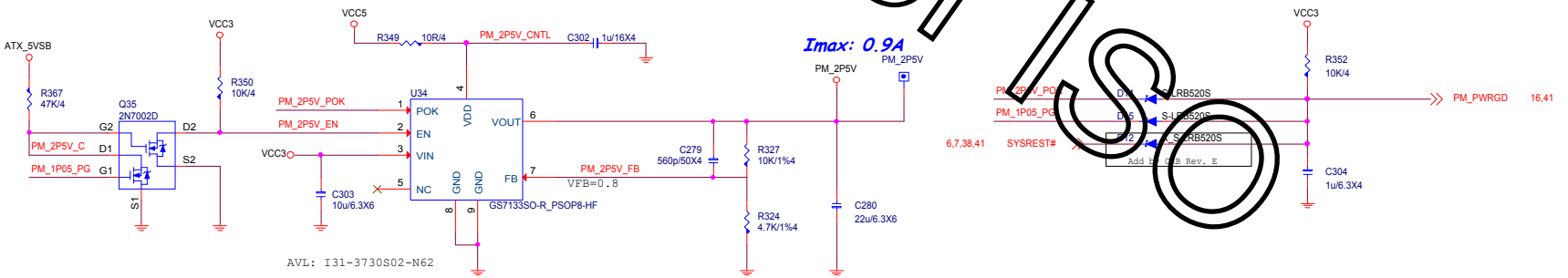
0.05A



Promontory-2.5V

2.5V; 900mA

Imax: 0.9A



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	PM-NB671-1.05V/GS7133-2.5V	
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HEAT SINK

PM_HS1
MEC2
MEC1
OE3-7A40001-K08

MOS HS(VCORE)

HS_MOS1
MEC2
MEC1
OE3-7A40002-K08

CPU Socket

CPU2
E95-0000021-C22

RETENTION MODULE

Simulation

X_JS1
SIM1
X_PIN1*2

X_JS2
SIM2
X_PIN1*2

MANUAL PART

UEFI1
G51-MTSPXXA-A09

BAT1_X1
BAT-BCR2032P-RH

PCB1
7A40-20
PD0-07A4020-G37,精成-深圳,1,台北微星廠(MSI)

HDMI_LA1
Label
HDMI
HDMI LABEL

MKT1
Label
MKT_B350I_PRO
X_B350I_PRO

FCH2
Label
FCH_A320.
X_A320

MKT2
Label
MKT_B350I_S01
X_B350I_S01

MKT3
Label
MKT_A320_PRO
X_A320I_PRO

MKT4
Label
MKT_A320_S01
X_A320I_PRO

CAP1
Label
B350I_S01_470u
X_B350I_S01_470

PCIE1
Label
PCIE
X_PCIE_S01

CAP2
Label
B350I_S01_270u
X_B350I_S01_270

MOS HS(NB)

HS_MOS2
MEC2
MEC1
HS-0505410-RH

Optics Orientation Holes

MH3
X_MH001

MH1
X_MH001

MH2
X_MH001

5010
FM1 FM4 FM7
X_FM120 X_FM120 X_FM120

5020
FM3 FM2 FM5
X_FM120 X_FM120 X_FM120

FM8 FM6
X_FM120 X_FM120

MS-7A40 20 for ISO

MSI MICRO-STAR INTERNATIONAL
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MICRO-START INT'L CO.,LTD.

Title: BOM Option		
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