MS-7A39 Ver:2.0

CPU:
AMD AM4

System Chipset:
Promontory A320
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

VRM
RT8894 3+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H

Azalia CODEC - Realtek ALC887

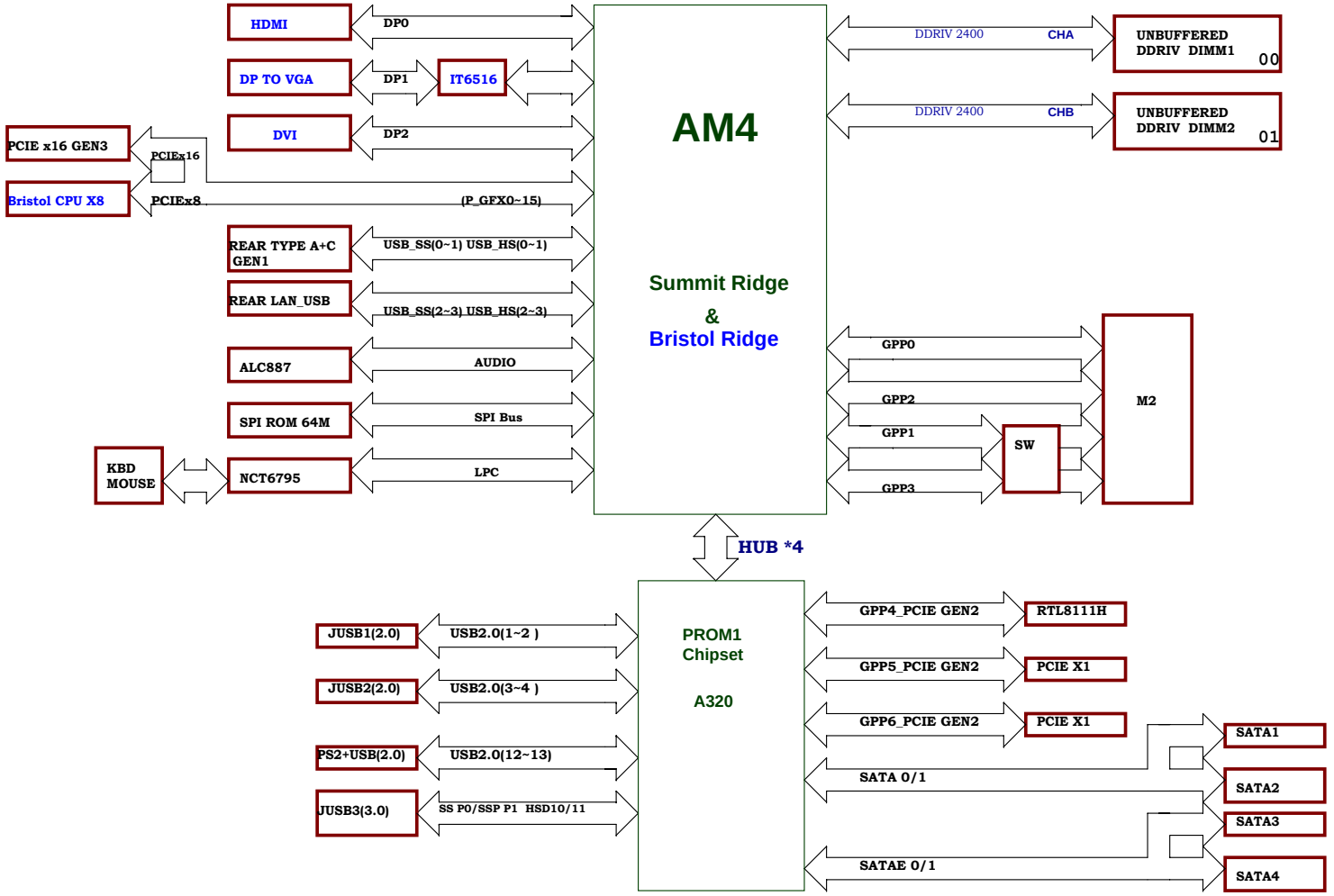
Expansion Slots:

From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

OCP IC:

UP6273

FUSION BLOCK DIAGRAM



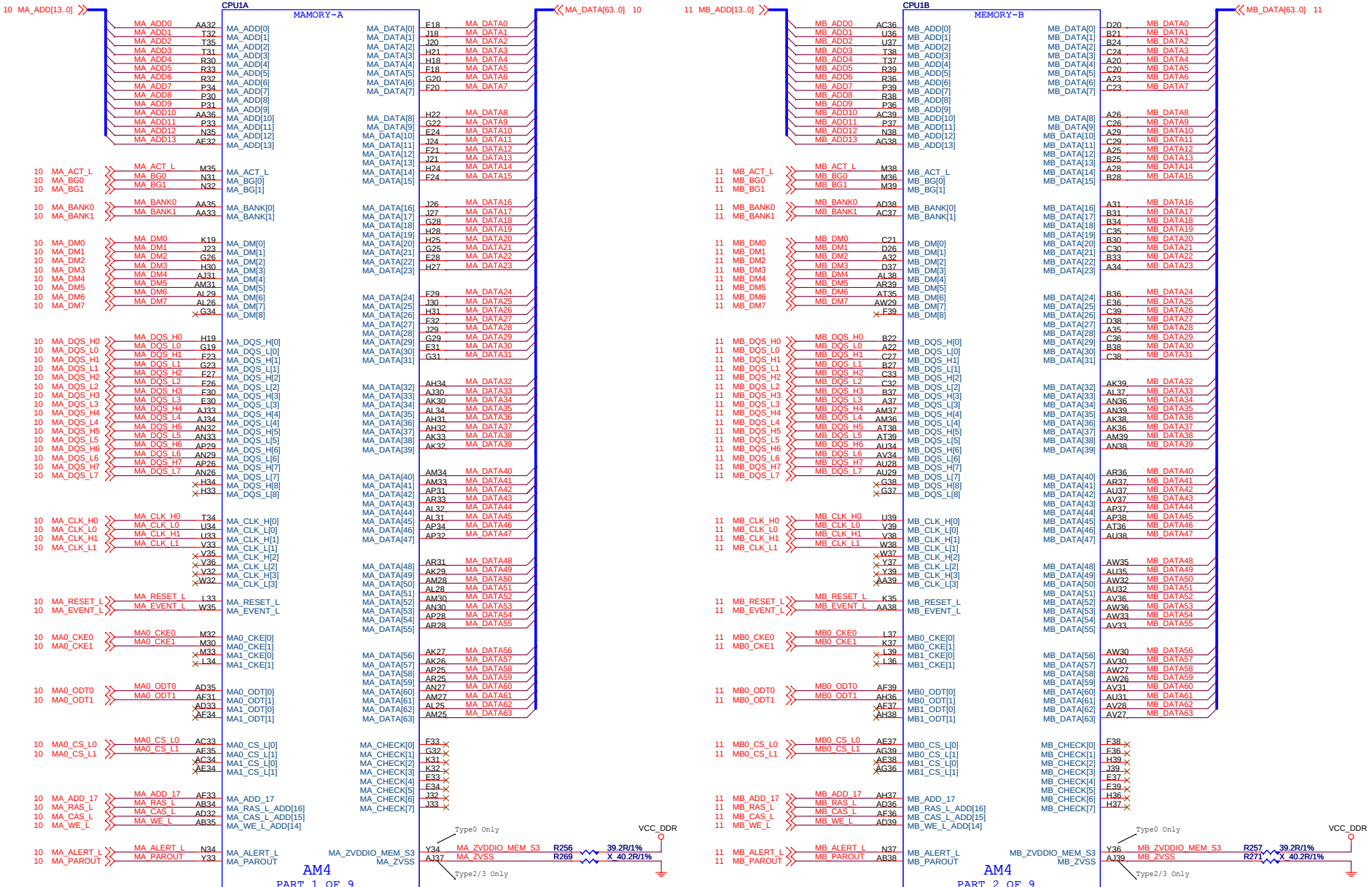
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: AM4 DDR4 I/F		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 1 of 55	

AMD AM4

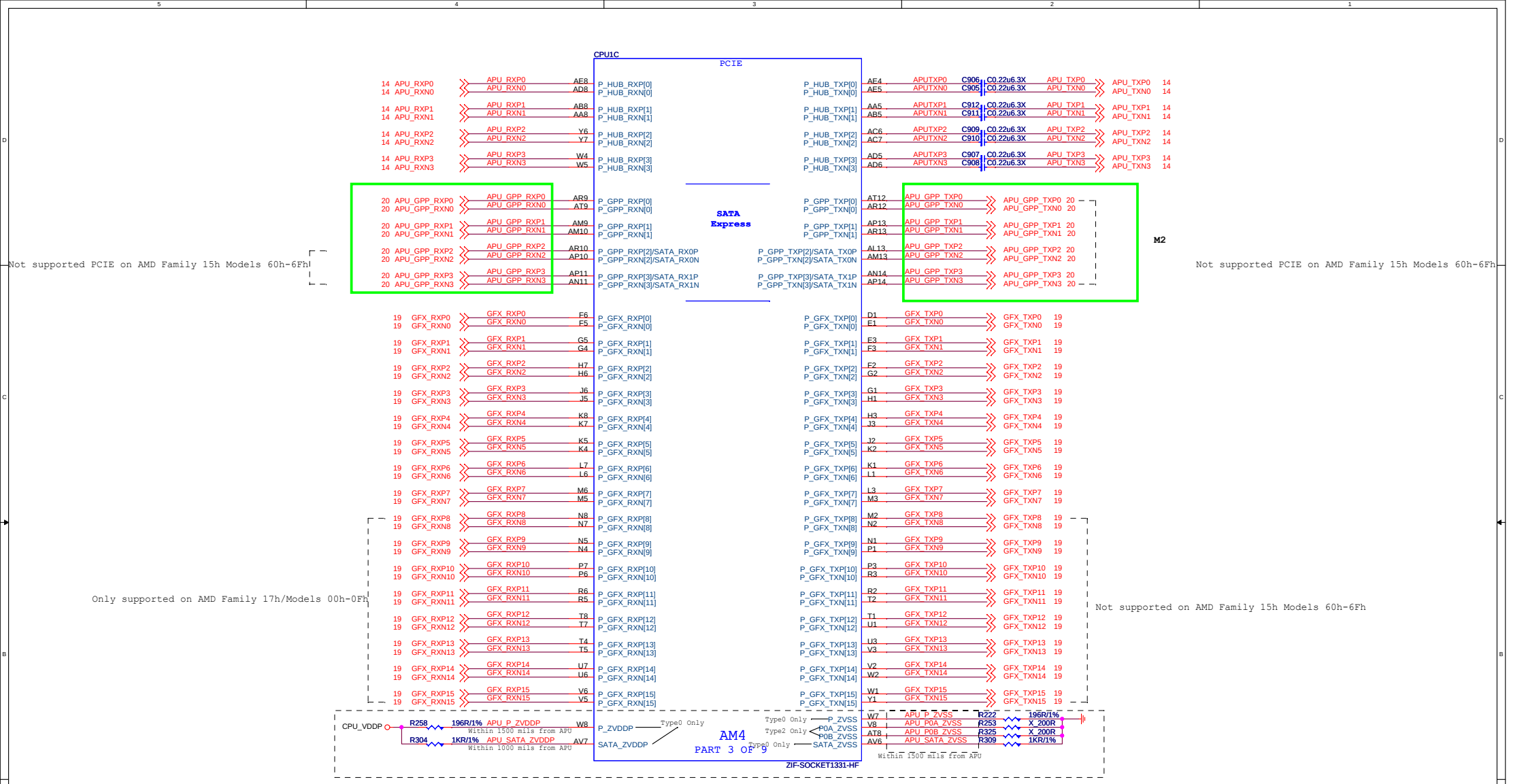
MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: AM4 DDR4 I/F		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 2 of 55	

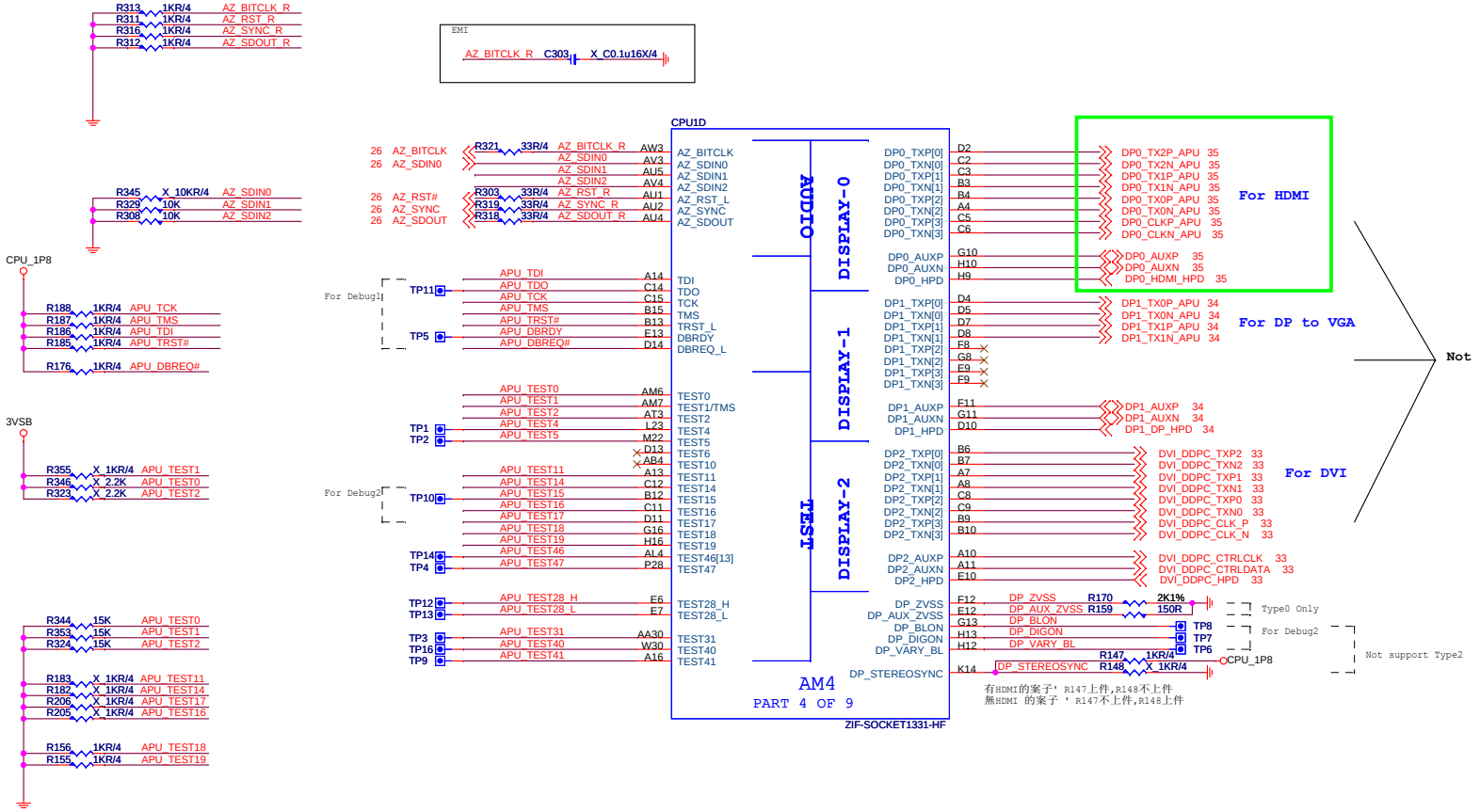


MICRO-START INT'L CO.,LTD.

Title	AM4 DDR4 I/F	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 3 of 55	



MSI MICRO-START INT'L CO.,LTD.		
Title: AM4 PCIE/SATAE		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 4 of 55	

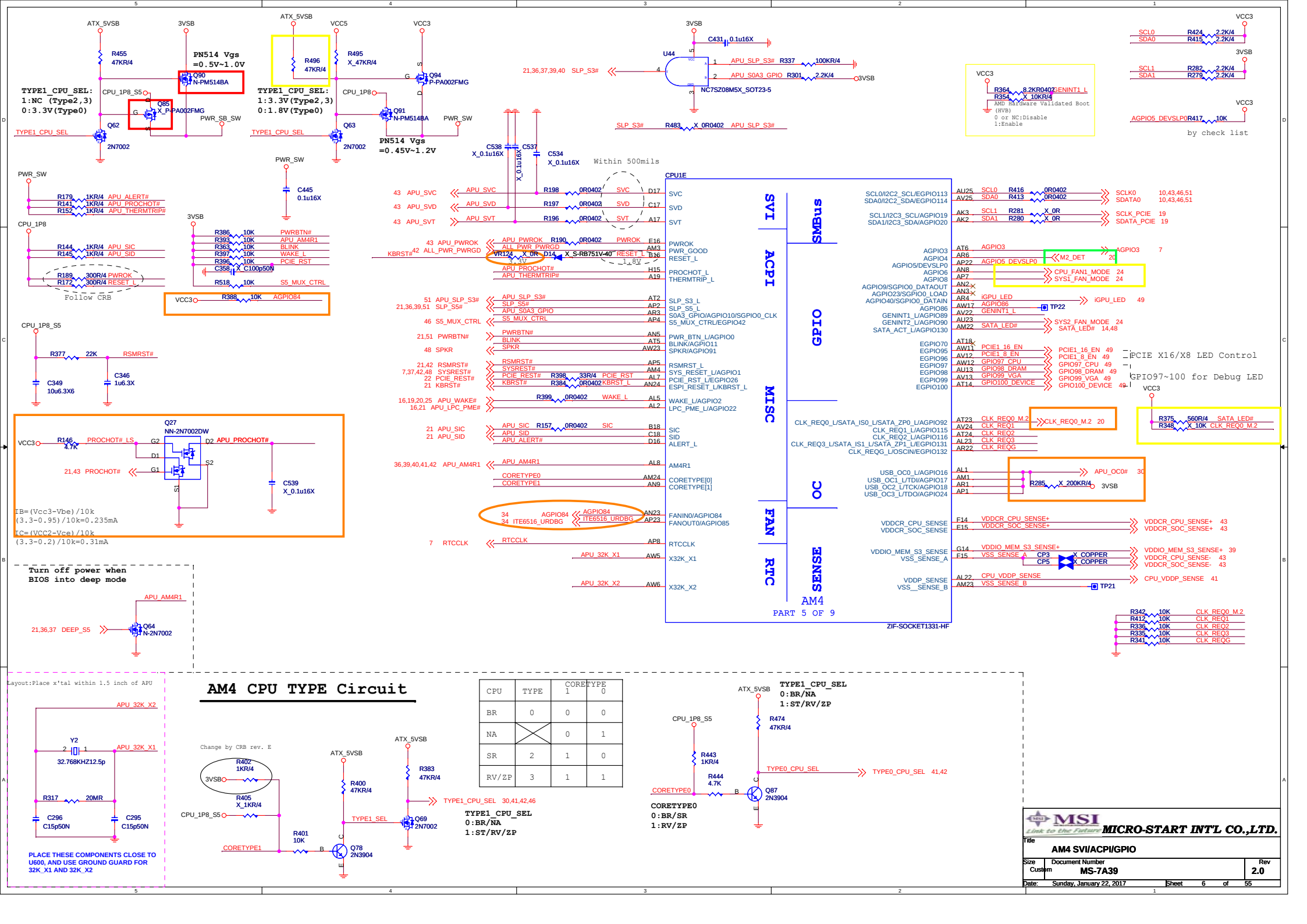


MICRO-START INT'L CO.,LTD.

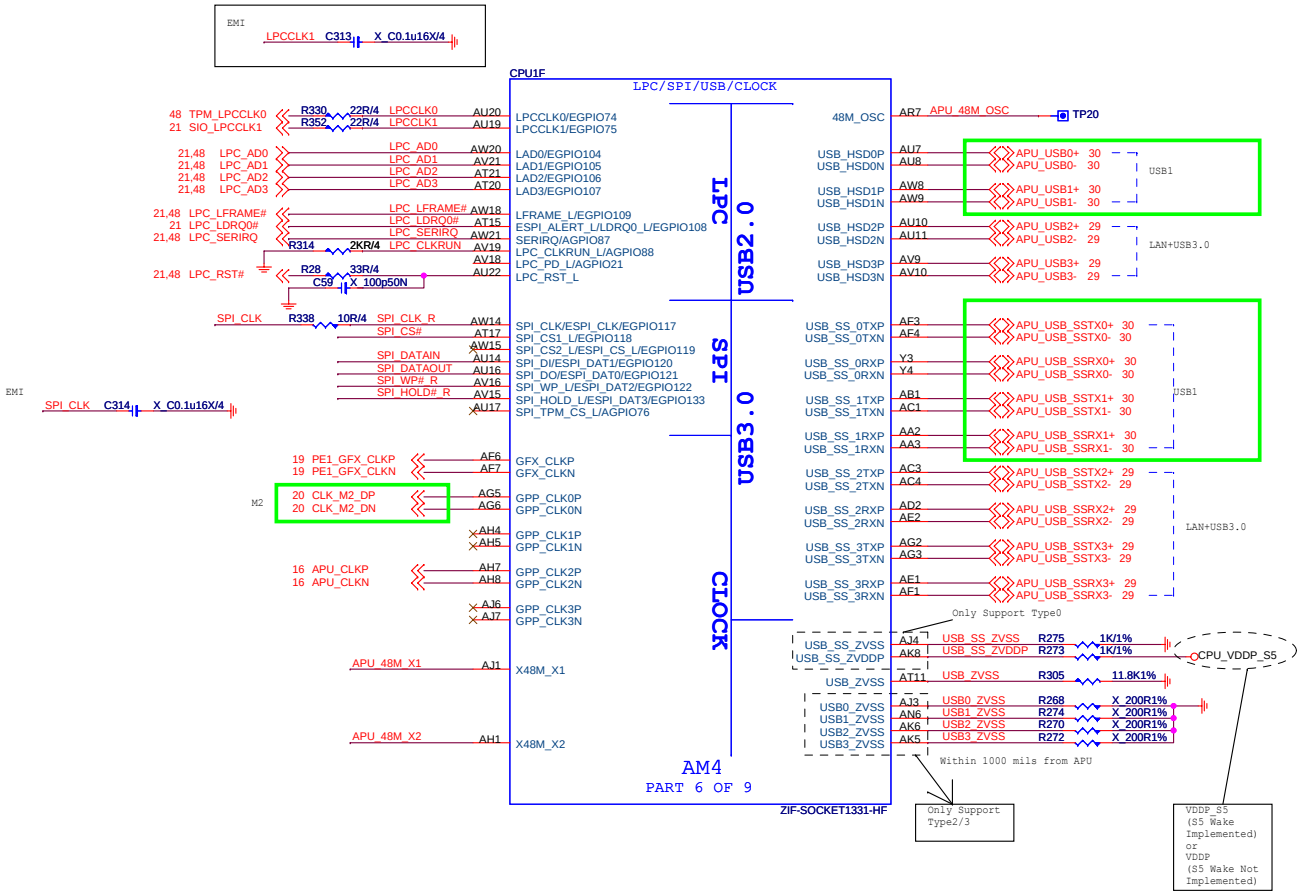
Title: AM4 DISPLAY/AUDIO

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

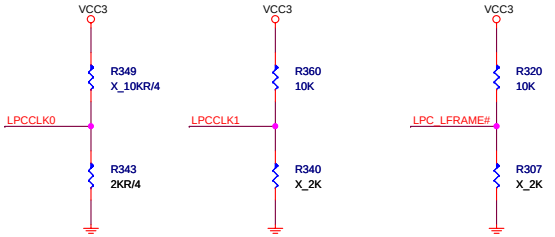
Date: Sunday, January 22, 2017 | Sheet 5 of 55



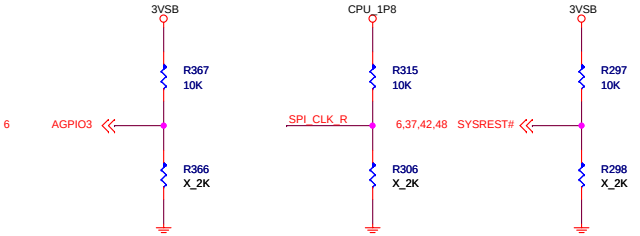
CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1



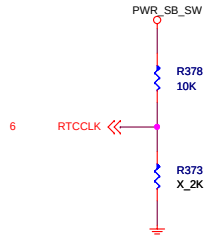
Strapping Options



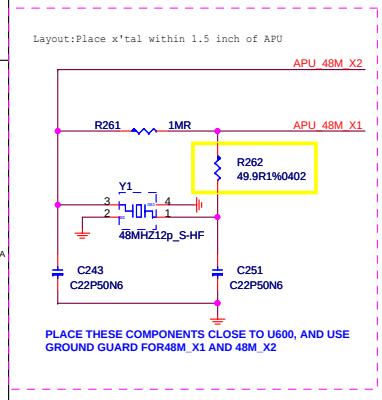
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



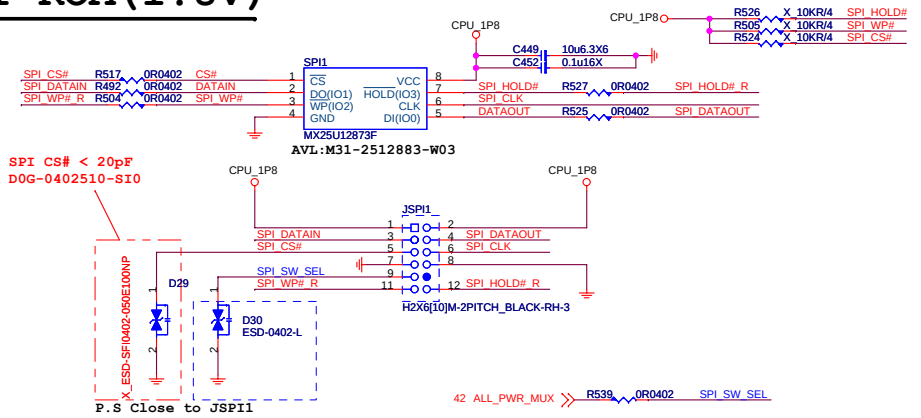
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board



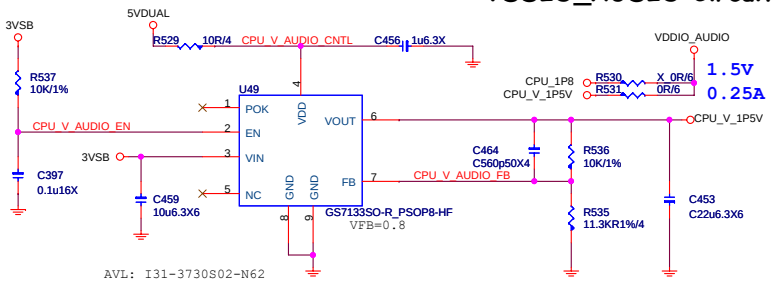
SPI ROM(1.8V)



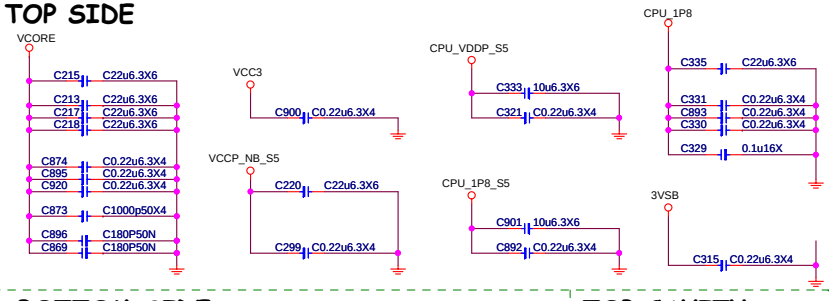
MSI Link to the Future MICRO-START INTL CO.,LTD.

Title	AM4 LPC/SPI/USB/CLK/STRAP	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 7 of 55	

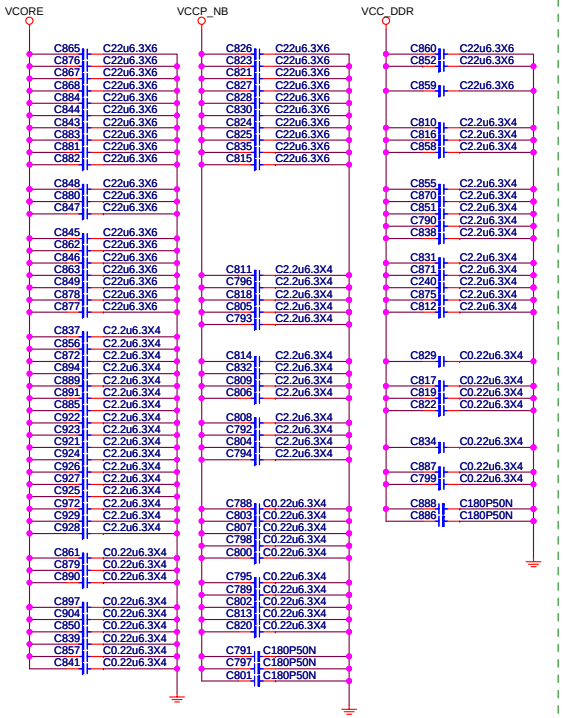
VDDIO_AUDIO Circuit



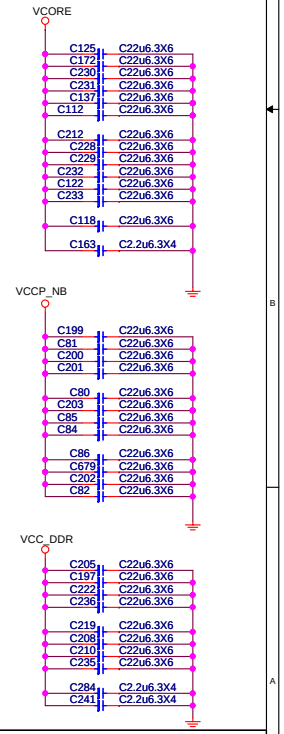
TOP SIDE

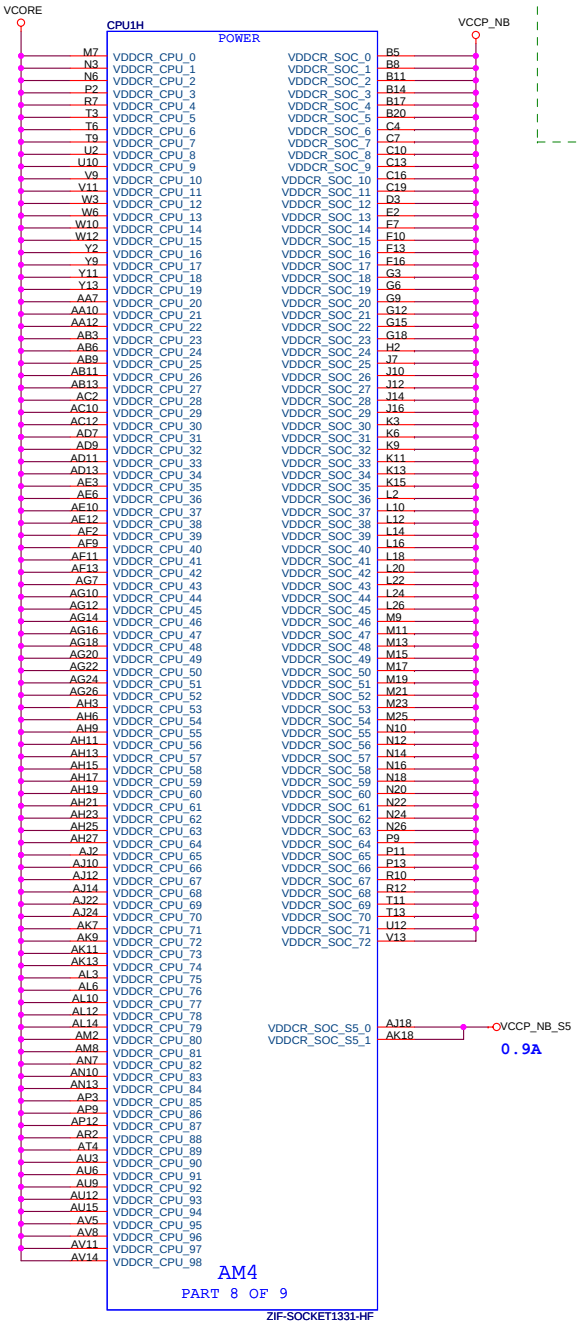


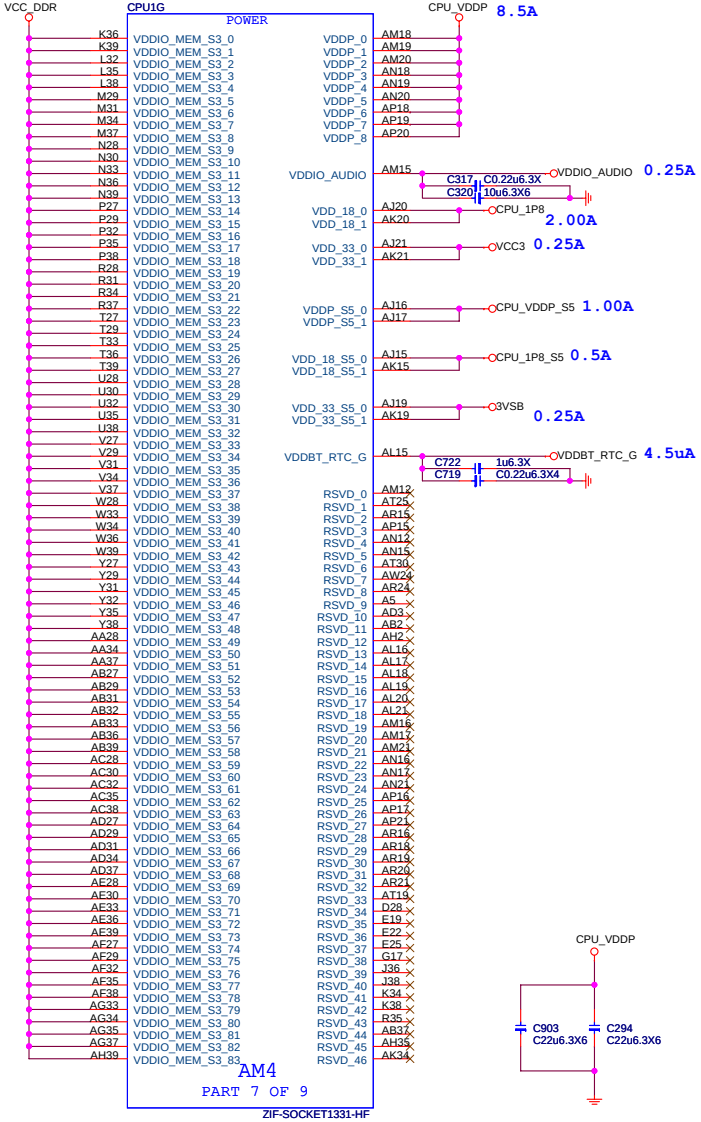
BOTTOM SIDE



TOP CAVITY

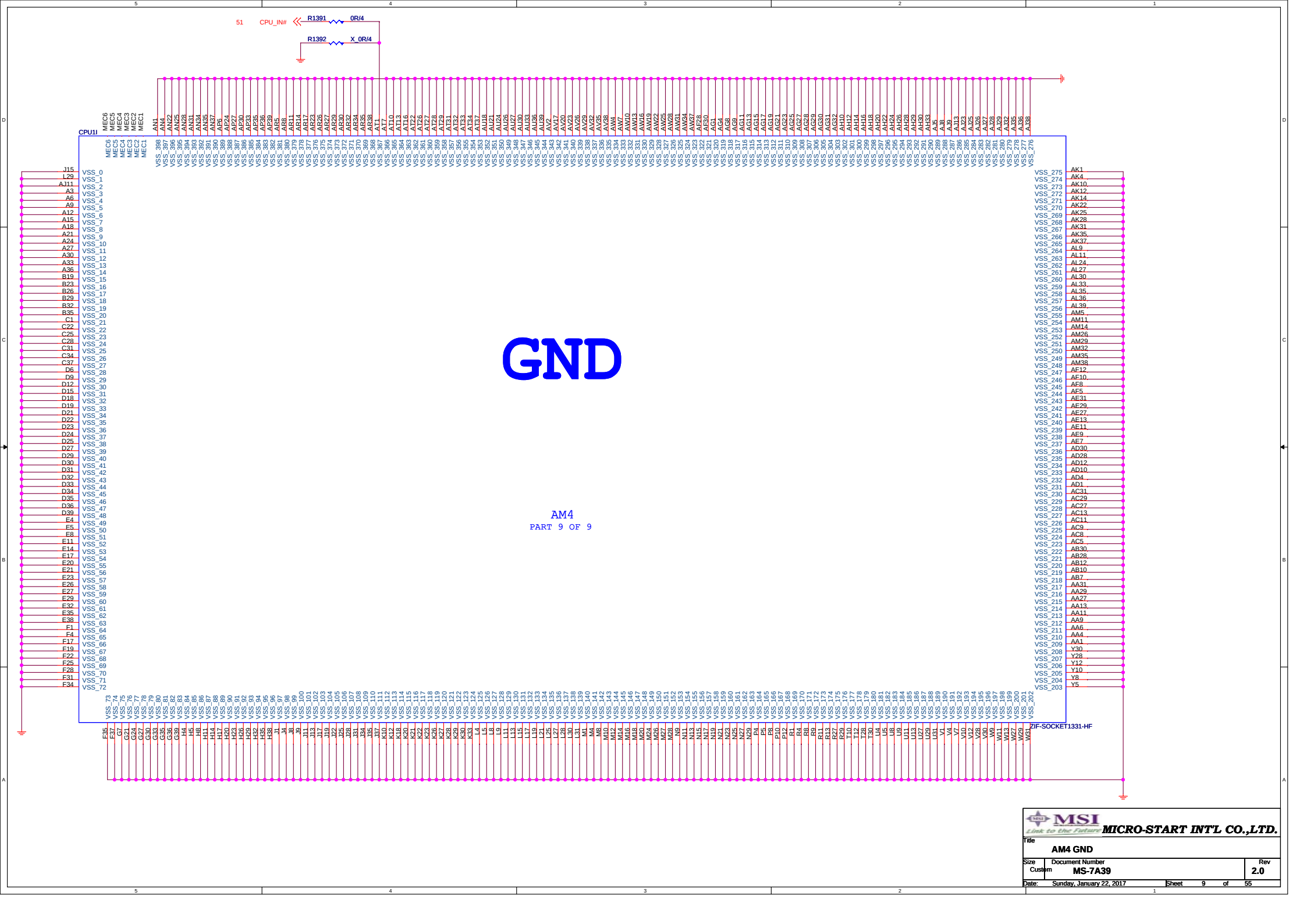




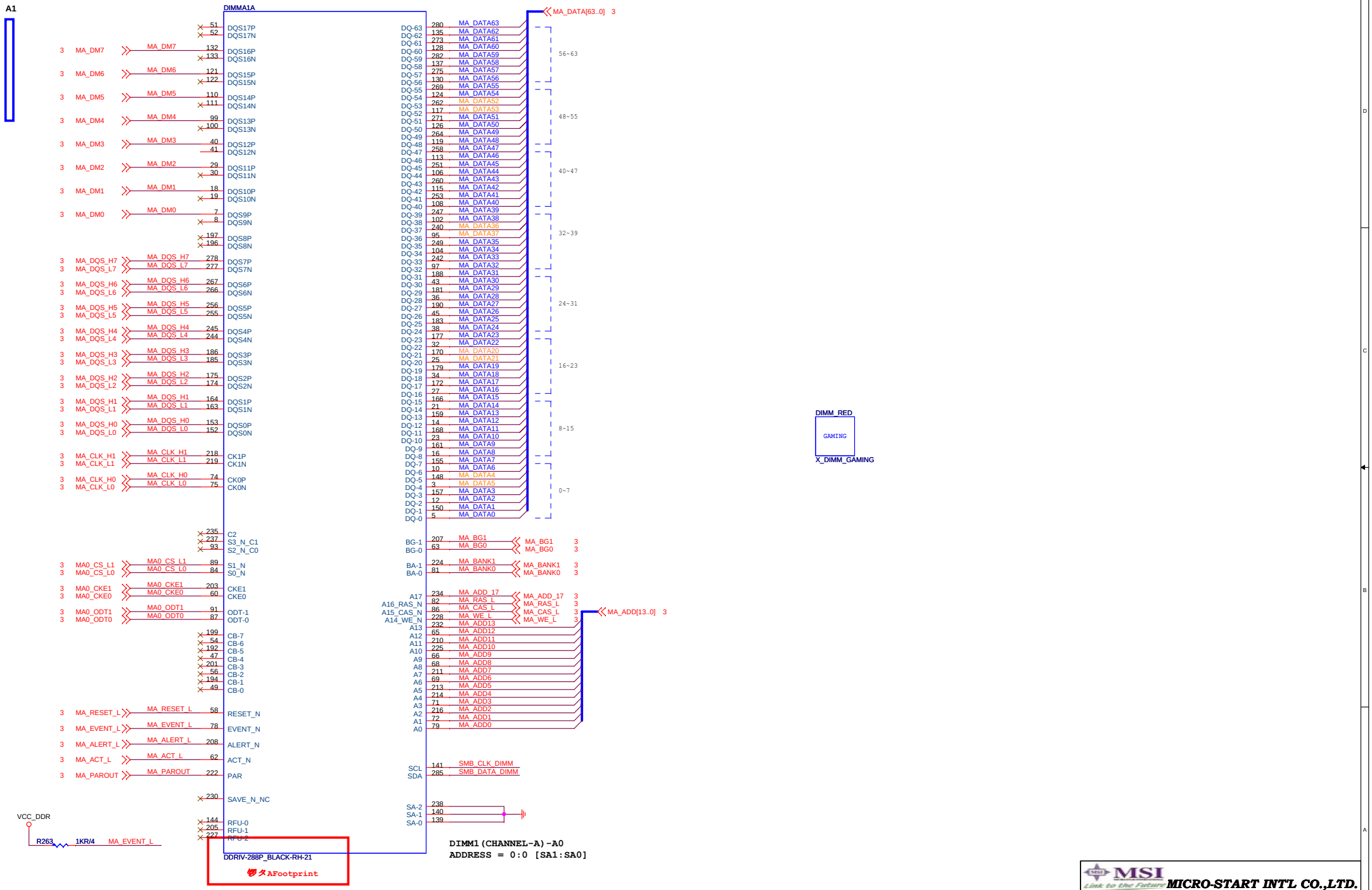


MSI MICRO-START INT'L CO.,LTD.

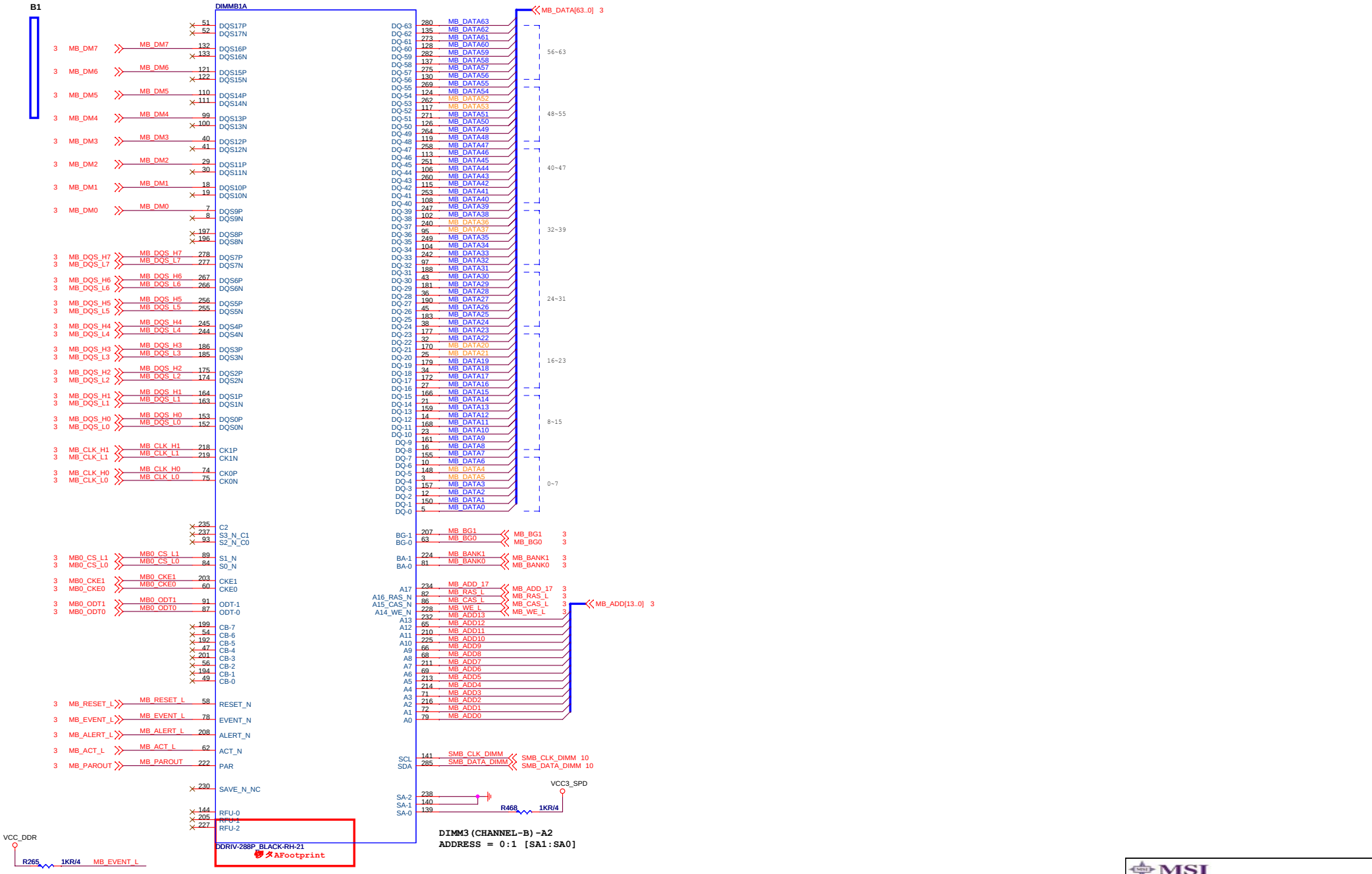
Title: AM4 Power/RTC Power		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 8 of 55	



MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title: AM4 GND		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 9 of 55	

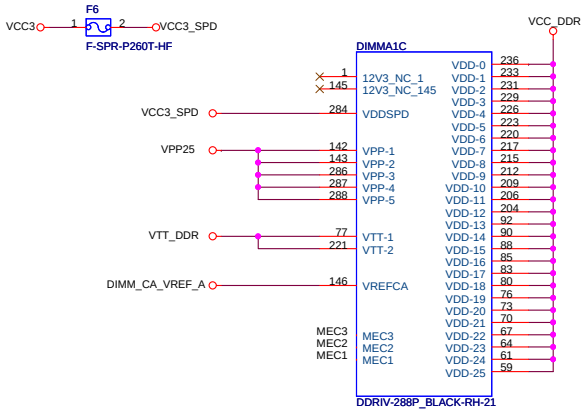


Company	MICRO-START INT'L CO.,LTD.
Title	DDR4 DIMM CH-A
Size	Custom
Document Number	MS-7A39
Rev	2.0
Date:	Sunday, January 22, 2017
Sheet	10 of 55



MSI MICRO-START INT'L CO.,LTD.
Link to the Future

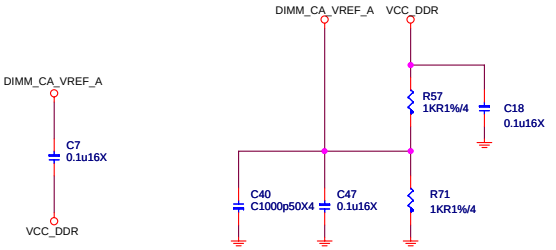
Title	DDR4 DIMM CH-B		
Size: Custom	Document Number: MS-7A39		Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 11 of 55		

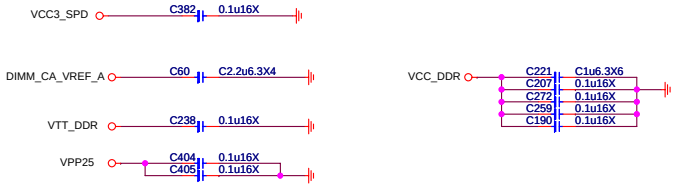


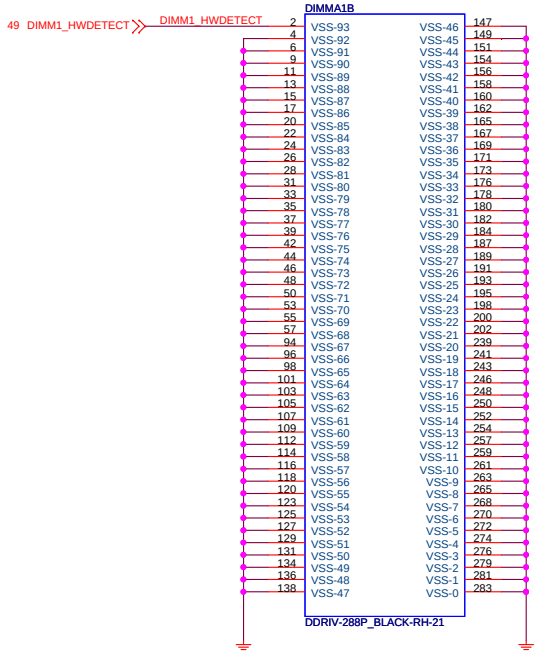
DIMM SLOT PN BY SPEC

DDR VREF

(place resistors close to DIMMs)





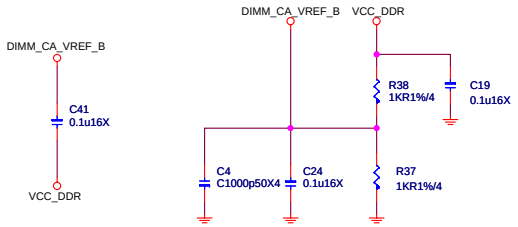


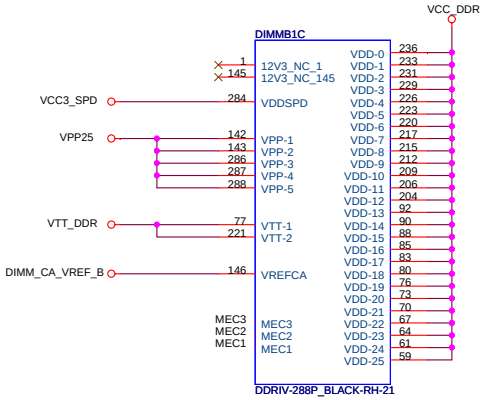
MSI — Link to the Future — **MICRO-START INT'L CO.,LTD.**

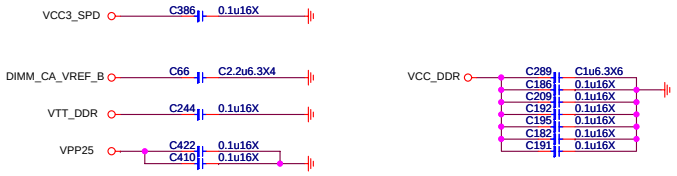
Title	DDR4-POWER/GND-1	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 12 of 55	

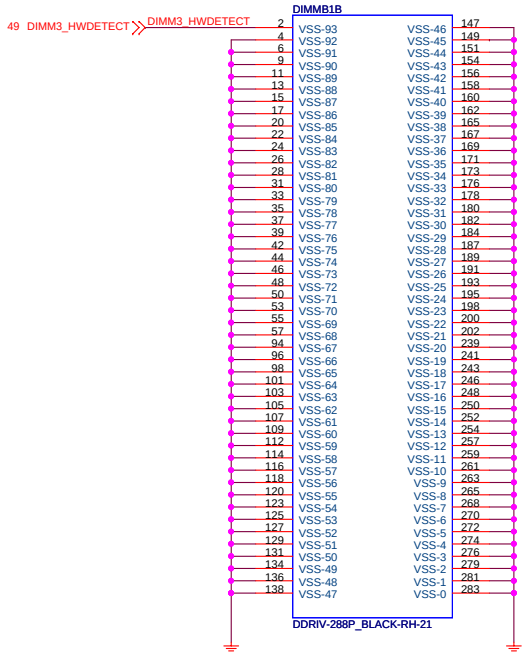
DDR VREF

(place resistors close to DIMMs)

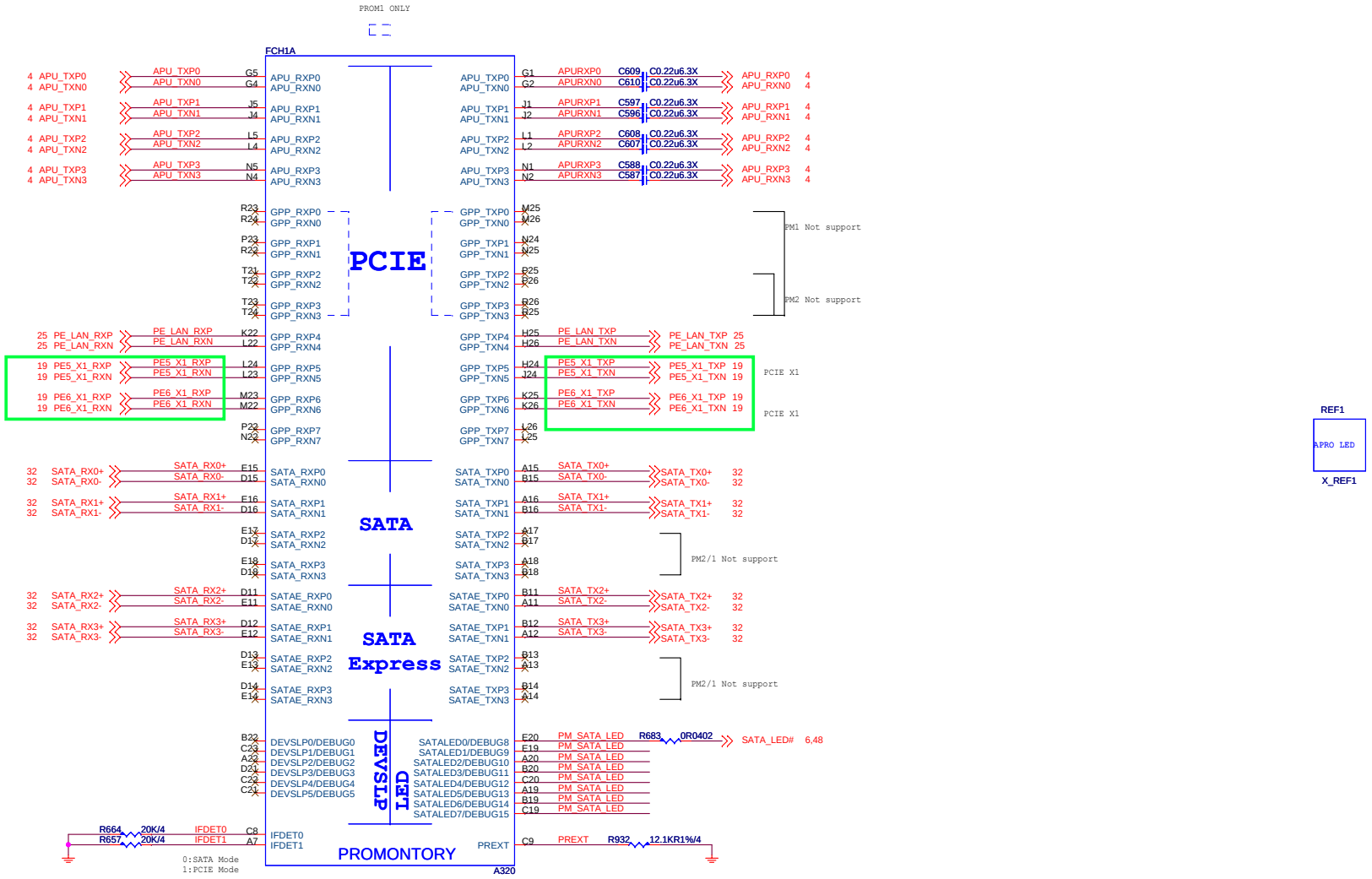




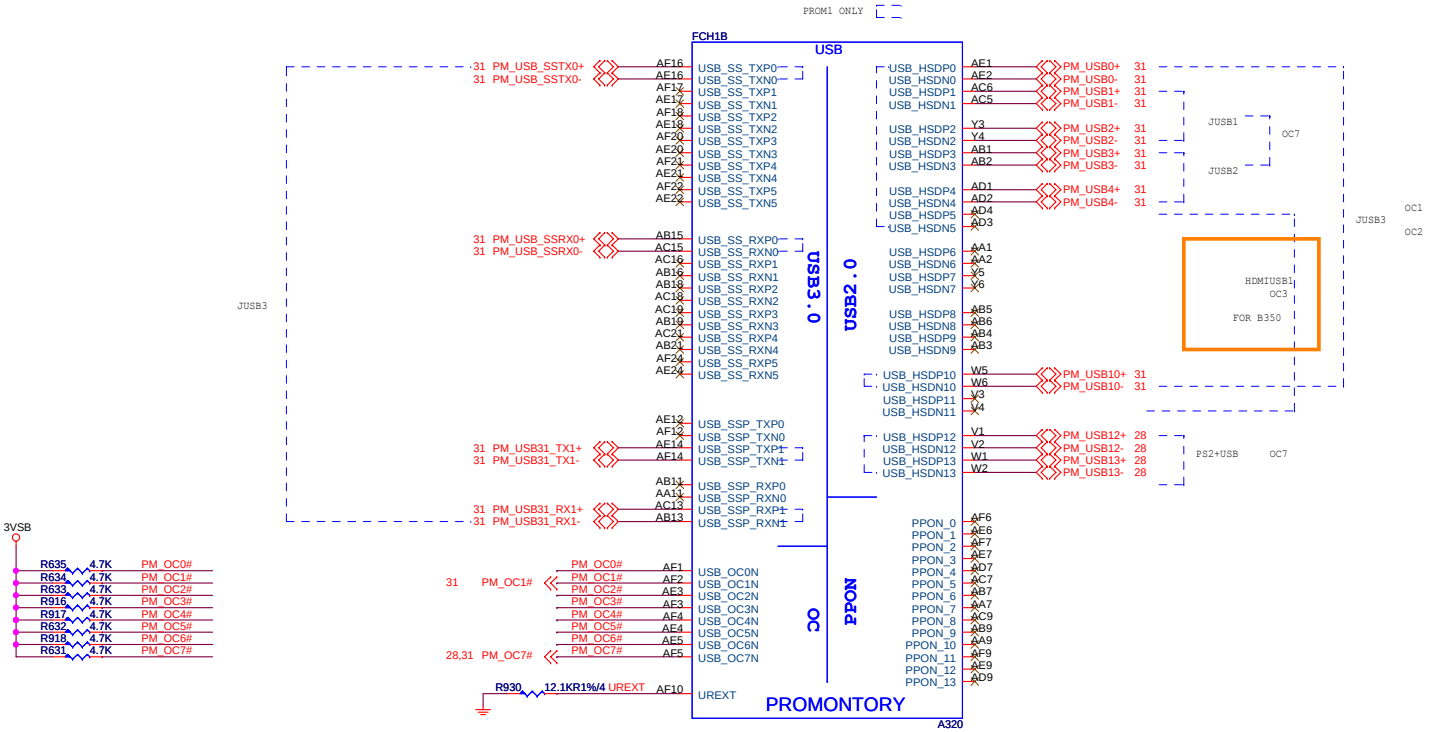




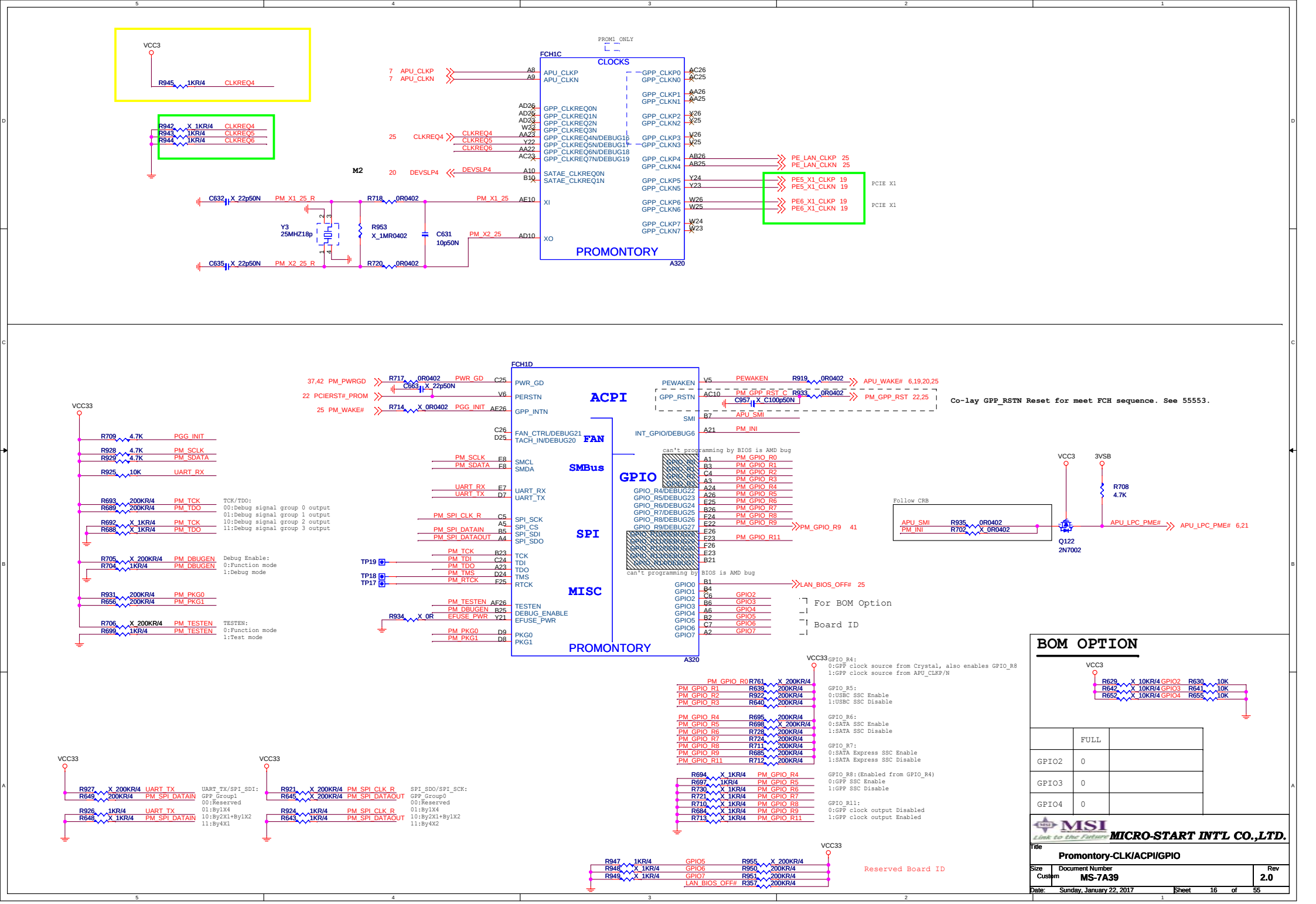
MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	DDR4-POWER/GND-2		
Size: Custom	Document Number: MS-7A39		Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 13 of 55		

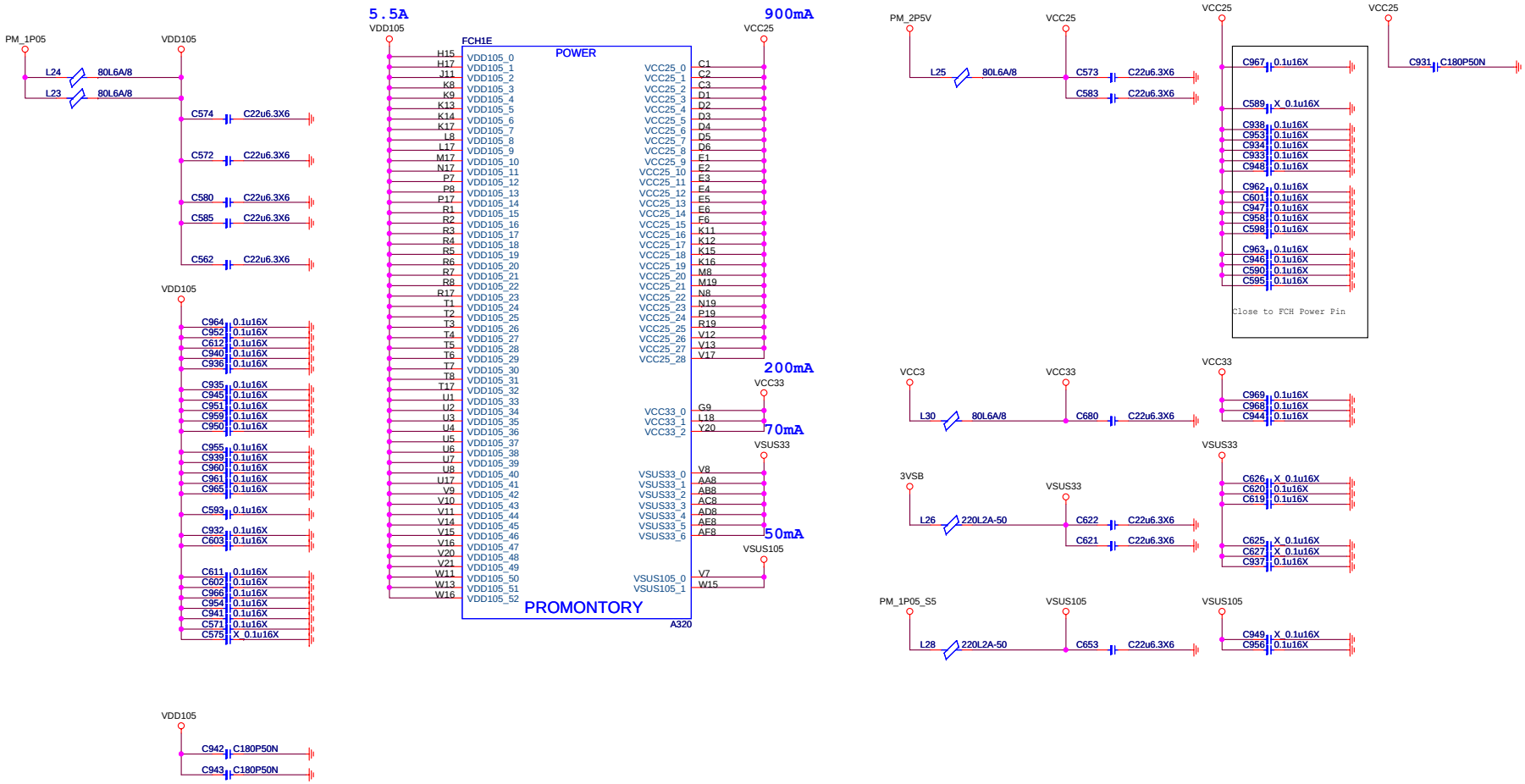


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	Promontory-PCIE/SATA/SATAE		
Size: Custom	Document Number: MS-7A39		Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 14 of 55		



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	Promontory-USB/OC		
Size: Custom	Document Number: MS-7A39	Rev: 2.0	
Date: Sunday, January 22, 2017	Sheet 15 of 55		


VCC3
R945 1KR/4 CLKREQ4
R942 X_1KR/4 CLKREQ4
R943 1KR/4 CLKREQ5
R944 1KR/4 CLKREQ6
M2
PROM1_ONLY
FCH1C
CLOCKS
7 APU_CLKP
7 APU_CLKN
APU_CLKP
APU_CLKN
GPP_CLKP0 AC26
GPP_CLKN0 AC25
GPP_CLKP1 AA26
GPP_CLKN1 AA25
GPP_CLKP2 Y26
GPP_CLKN2 Y25
GPP_CLKP3 V26
GPP_CLKN3 V25
GPP_CLKP4 AB26
GPP_CLKN4 AB25
GPP_CLKP5 Y24
GPP_CLKN5 Y23
GPP_CLKP6 W26
GPP_CLKN6 W25
GPP_CLKP7 W24
GPP_CLKN7 W23
GPP_CLKREQ0N AD26
GPP_CLKREQ1N AD25
GPP_CLKREQ2N AD23
GPP_CLKREQ3N W22
GPP_CLKREQ4N/DEBUG16 AA23
GPP_CLKREQ5N/DEBUG17 Y22
GPP_CLKREQ6N/DEBUG18 AA22
GPP_CLKREQ7N/DEBUG19 AC22
25 CLKREQ4
CLKREQ4
CLKREQ5
CLKREQ6
20 DEVSLP4
DEVSLP4 A10
B10
SATAE_CLKREQ0N
SATAE_CLKREQ1N
PE_LAN_CLKP 25
PE_LAN_CLKN 25
PE5_X1_CLKP 19
PE5_X1_CLKN 19
PCIE X1
PE6_X1_CLKP 19
PE6_X1_CLKN 19
PCIE X1
C632 X_22p50N PM_X1_25_R
R718 0R0402 PM_X1_25 AE10 XI
Y3 25MHZ18p
R953 X_1MR0402
C631 10p50N PM_X2_25 AD10 XO
C635 X_22p50N PM_X2_25_R
R720 0R0402
PROMONTORY
A320
FCH1D
ACPI
FAN
SMBus
GPIO
SPI
MISC
37,42 PM_PWRGD
R717 0R0402 PWR_GD C25 PWR_GD
C663 X_22p50N
22 PCIERST#_PROM V6 PERSTN
25 PM_WAKE#
R714 X_0R0402 PGG_INIT AE26 GPP_INTN
C26 FAN_CTRL/DEBUG21
D25 TACH_IN/DEBUG20
PM_SCLK F8 SMCL
PM_SDATA F8 SMDA
UART_RX E7
UART_TX D7
PM_SPI_CLK_R C5 SPI_SCK
A5 SPI_CS
PM_SPI_DATAIN B5 SPI_SDI
PM_SPI_DATAOUT A4 SPI_SDO
PM_TCK B23 TCK
PM_TDI C24 TDI
PM_TDO A23 TDO
PM_TMS D24 TMS
PM_RTCK F25 RTCK
PM_TESTEN AE26 TESTEN
PM_DBUGEN B25 DEBUG_ENABLE
R934 X_0R EFUSE_PWR Y21 EFUSE_PWR
PM_PKG0 D9 PKG0
PM_PKG1 D8 PKG1
TP19
TP18
TP17
PEWAKEN V5
GPP_RSTN AC10
SMI B7
INT_GPIO/DEBUG6 A21
PEWAKEN R919 0R0402 APU_WAKE# 6,19,20,25
PM_GPP_RST_C R933 0R0402 PM_GPP_RST 22,25
C957 X_C100p50N
APU_SMI
PM_INI
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
can't programming by BIOS is AMD bug
GPIO_R4/DEBUG22 A1 PM_GPIO_R0
GPIO_R5/DEBUG23 B3 PM_GPIO_R1
GPIO_R6/DEBUG24 C4 PM_GPIO_R2
GPIO_R7/DEBUG25 A3 PM_GPIO_R3
GPIO_R8/DEBUG26 A24 PM_GPIO_R4
GPIO_R9/DEBUG27 A26 PM_GPIO_R5
E25 PM_GPIO_R6
B26 PM_GPIO_R7
E24 PM_GPIO_R8
E22 PM_GPIO_R9
PM_GPIO_R9 41
E26
E23 PM_GPIO_R11
F26
E23
B21
can't programming by BIOS is AMD bug
GPIO0 B1
GPIO1 B4
GPIO2 C6 GPIO2
GPIO3 B6 GPIO3
GPIO4 A6 GPIO4
GPIO5 B2 GPIO5
GPIO6 C7 GPIO6
GPIO7 A2 GPIO7
LAN_BIOS_OFF# 25
For BOM Option
Board ID
VCC33
R709 4.7K PGG_INIT
R928 4.7K PM_SCLK
R929 4.7K PM_SDATA
R925 10K UART_RX
R693 200KR/4 PM_TCK
R689 200KR/4 PM_TDO
R692 X_1KR/4 PM_TCK
R688 X_1KR/4 PM_TDO
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
R705 X_200KR/4 PM_DBUGEN
R704 1KR/4 PM_DBUGEN
Debug Enable:
0:Function mode
1:Debug mode
R931 200KR/4 PM_PKG0
R656 200KR/4 PM_PKG1
R706 X_200KR/4 PM_TESTEN
R699 1KR/4 PM_TESTEN
TESTEN:
0:Function mode
1:Test mode
VCC3
3VSB
R708 4.7K
Follow CRB
APU_SMI R935 0R0402
PM_INI R702 X_0R0402
Q122 2N7002
APU_LPC_PME# APU_LPC_PME# 6,21
VCC33
R927 X_200KR/4 UART_TX
R649 200KR/4 PM_SPI_DATAIN
R926 1KR/4 UART_TX
R648 X_1KR/4 PM_SPI_DATAIN
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X1
R921 X_200KR/4 PM_SPI_CLK_R
R645 X_200KR/4 PM_SPI_DATAOUT
R924 1KR/4 PM_SPI_CLK_R
R643 1KR/4 PM_SPI_DATAOUT
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
VCC33
PM_GPIO_R0 R761 X_200KR/4
PM_GPIO_R1 R639 200KR/4
PM_GPIO_R2 R922 200KR/4
PM_GPIO_R3 R640 200KR/4
PM_GPIO_R4 R695 200KR/4
PM_GPIO_R5 R698 X_200KR/4
PM_GPIO_R6 R728 200KR/4
PM_GPIO_R7 R724 200KR/4
PM_GPIO_R8 R711 200KR/4
PM_GPIO_R9 R685 200KR/4
PM_GPIO_R11 R712 200KR/4
GPIO_R4:
0:GPP clock source from Crystal, also enables GPIO_R8
1:GPP clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
R694 X_1KR/4 PM_GPIO_R4
R697 1KR/4 PM_GPIO_R5
R730 X_1KR/4 PM_GPIO_R6
R721 X_1KR/4 PM_GPIO_R7
R710 X_1KR/4 PM_GPIO_R8
R684 X_1KR/4 PM_GPIO_R9
R713 X_1KR/4 PM_GPIO_R11
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
VCC33
R947 1KR/4 GPIO5
R948 X_1KR/4 GPIO6
R949 X_1KR/4 GPIO7
R955 X_200KR/4
R950 200KR/4
R951 200KR/4
LAN_BIOS_OFF# R357 200KR/4
Reserved Board ID
BOM OPTION
VCC3
R629 X_10KR/4 GPIO2
R642 X_10KR/4 GPIO3
R652 X_10KR/4 GPIO4
R630 10K
R641 10K
R655 10K
FULL
GPIO2 0
GPIO3 0
GPIO4 0
MSI
MICRO-START INTL CO.,LTD.
Title
Promontory-CLK/ACPI/GPIO
Size Custom
Document Number MS-7A39
Rev 2.0
Date: Sunday, January 22, 2017
Sheet 16 of 55

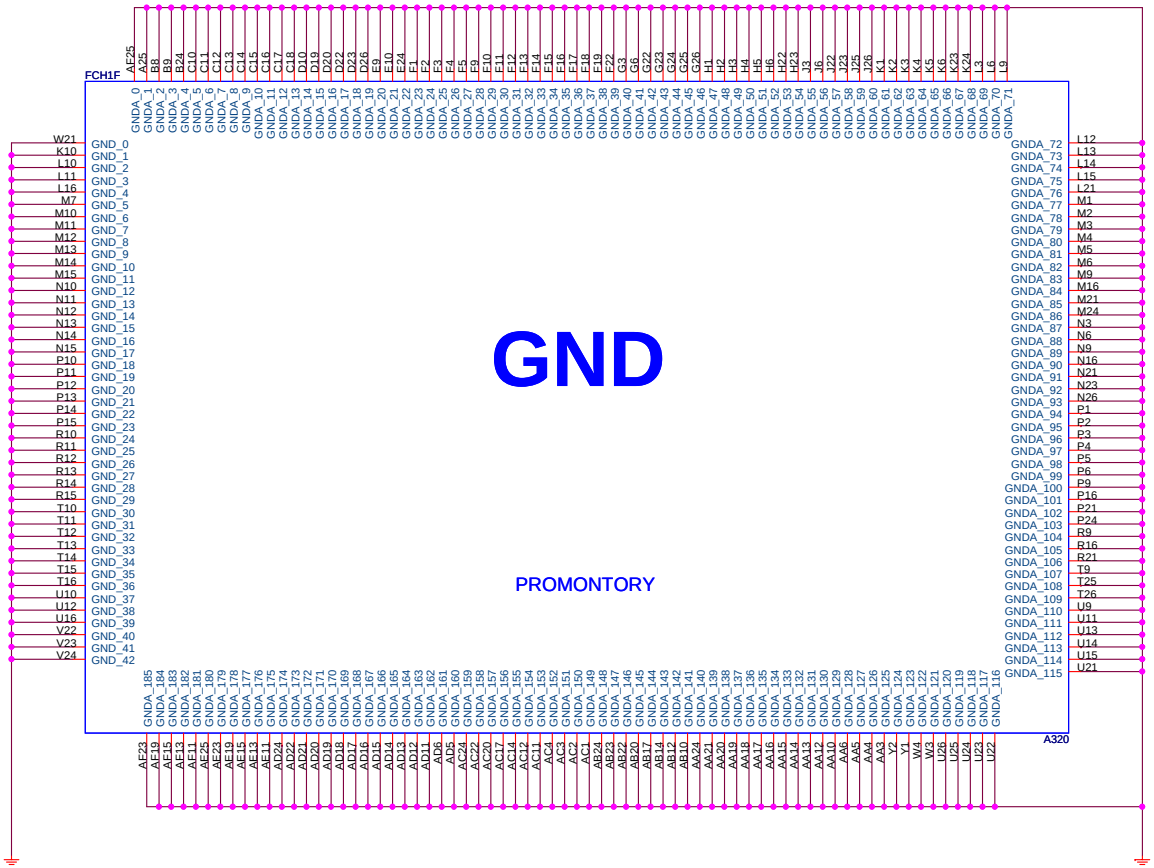


MSI MICRO-START INT'L CO.,LTD.

Title: Promontory-Power

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

Date: Sunday, January 22, 2017 | Sheet 17 of 55



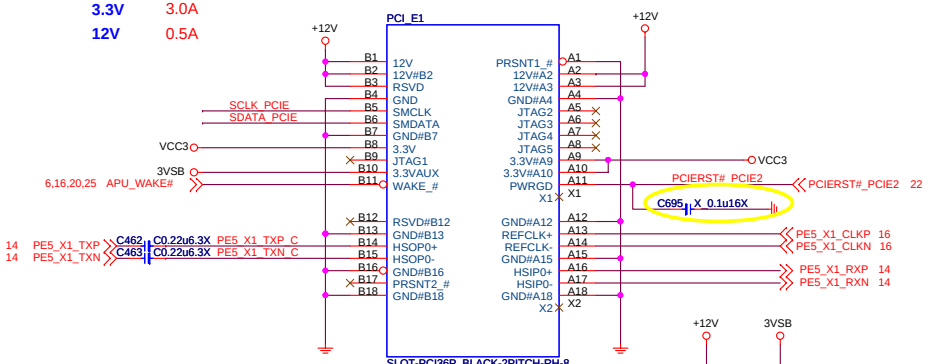
MSI	MICRO-START INT'L CO.,LTD.
Title	Promontory-GND
Size	Custom
Document Number	MS-7A39
Rev	2.0
Date:	Sunday, January 22, 2017
Sheet	18 of 55

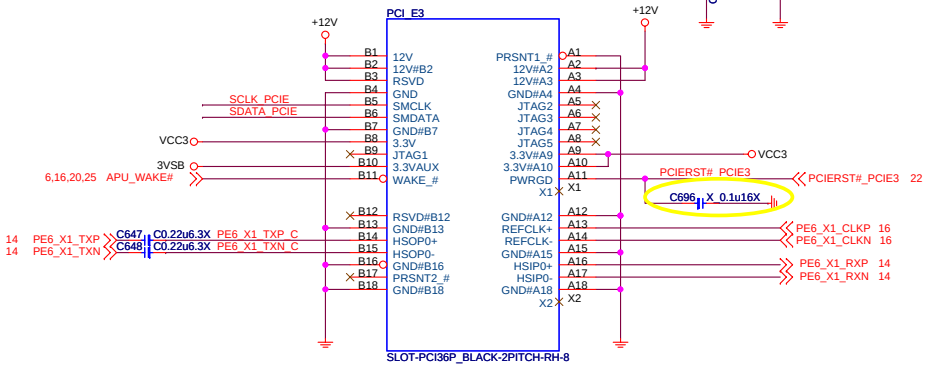
PCI EXPRESS x16 Slot

3.3V 3.0A
12V 5.5A

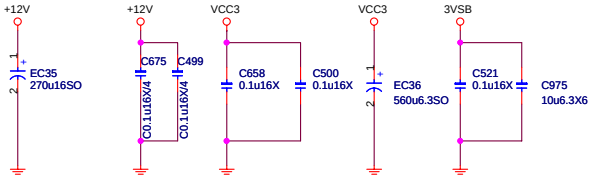
PCIEX1 12V 0.5A
3.3V weak 375mA

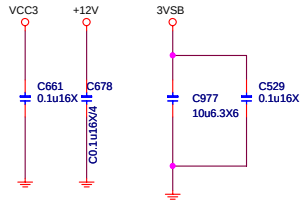
3.3V 3.0A
12V 0.5A



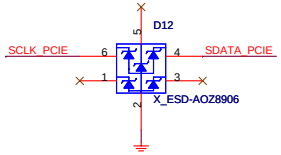


PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

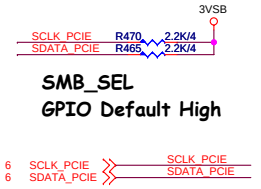




PCIE2_16
GAMING
X_PCIE X16



SMBus separate circuit

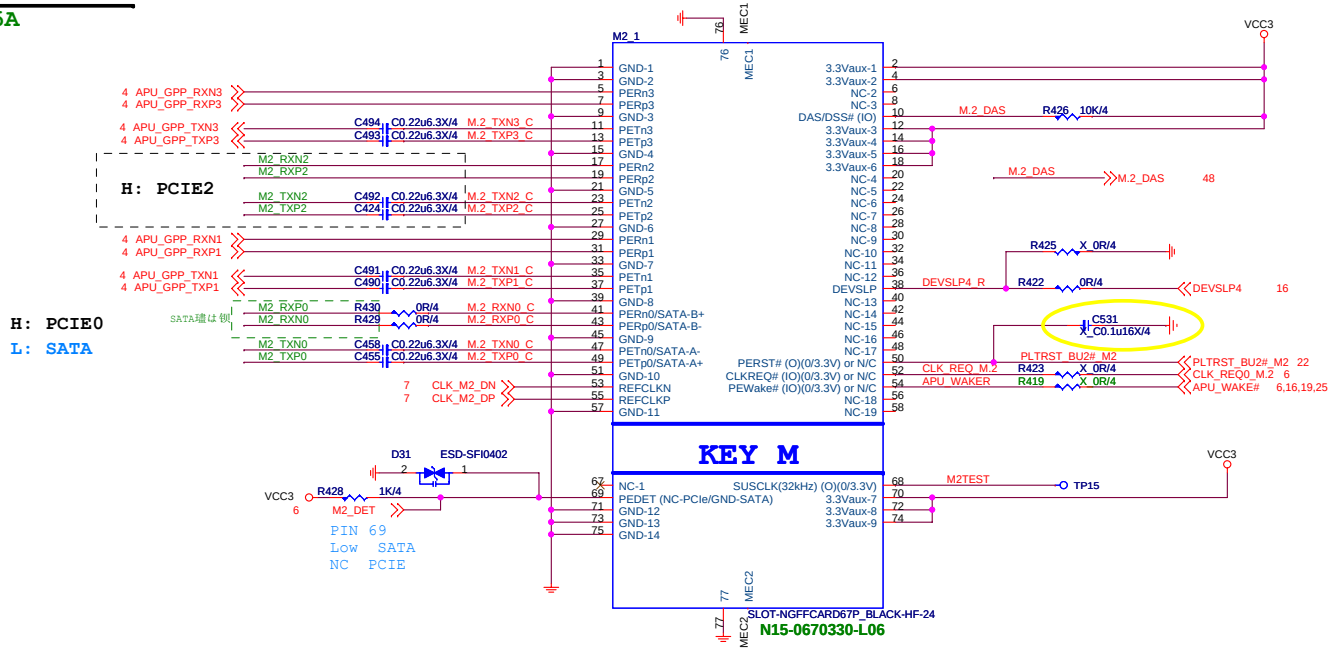


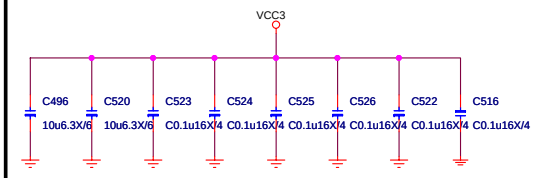
Title	PCIE X16(X1*2) SLOT
Size: Custom	Document Number: MS-7A39
Rev	2.0
Date: Sunday, January 22, 2017	Sheet 19 of 55

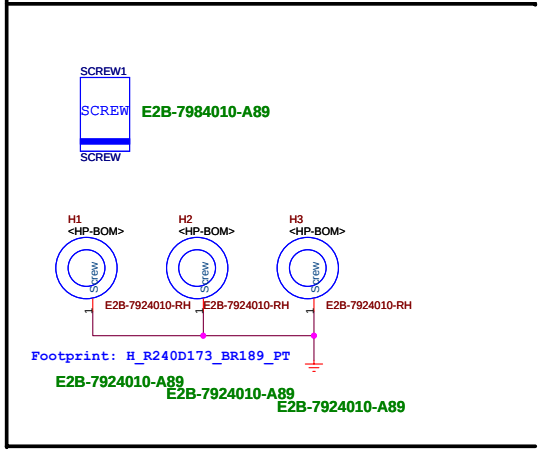
MSI Link to the Future MICRO-START INT'L CO.,LTD.

M.2 Connector

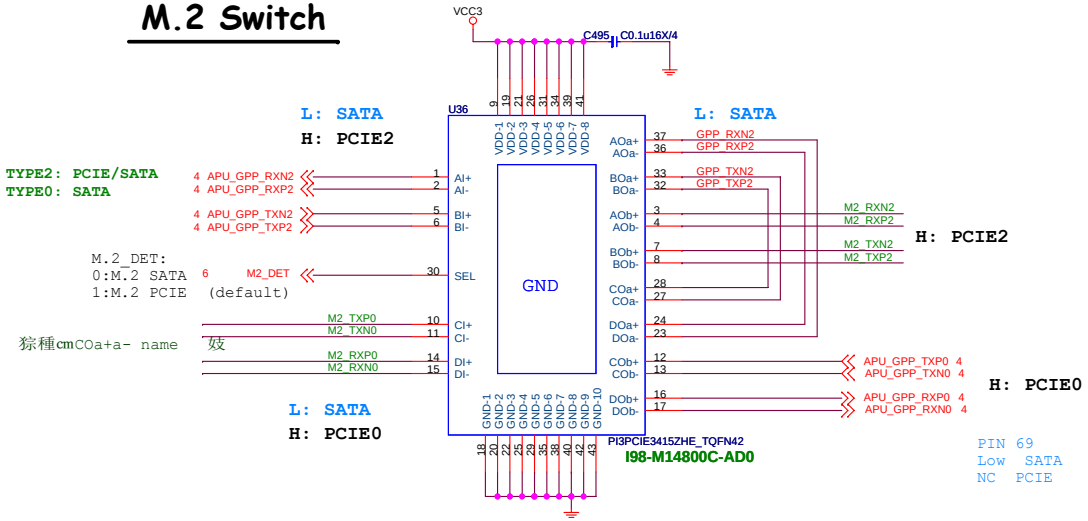
3.3V@2.5A



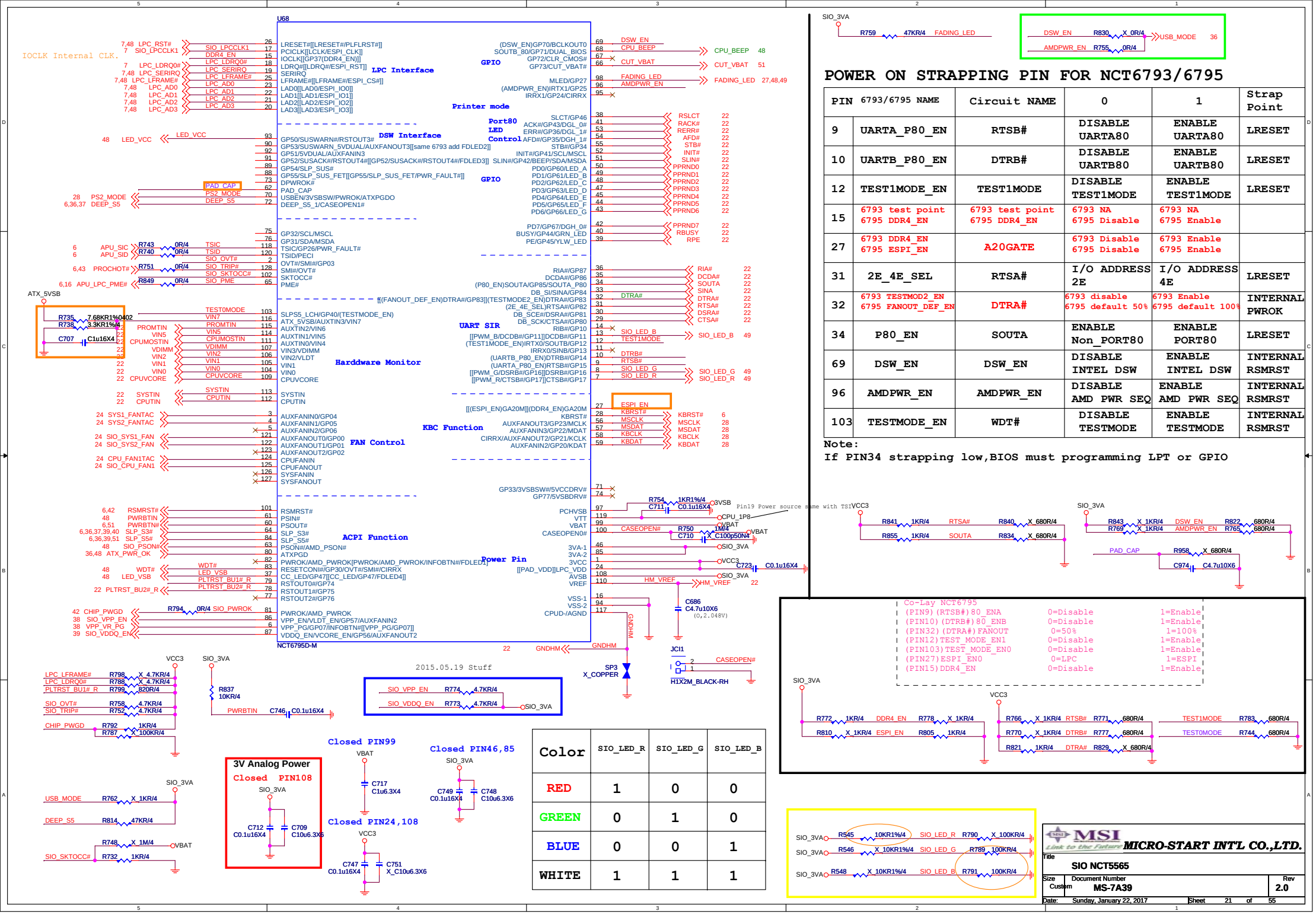




M.2 Switch



MSI MICRO-START INT'L CO.,LTD.			
Title: M2			
Size: Custom	Document Number: MS-7A39		Rev: 2.0
Date: Wednesday, January 25, 2017	Sheet 20 of 55		



POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

MSI MICRO-START INT'L CO.,LTD.
Title: SIO NCT5565
Size: Custom | Document Number: MS-7A39 | Rev: 2.0
Date: Sunday, January 22, 2017 | Sheet 21 of 55

HW Monitor - Voltage

+12V R390 220K1%/4 VIN0 → VIN0
R385 20K1%/4
C345 0.1u16X

VCC5 R440 12K1%/4 VIN1 → VIN1 21
R436 3K1%/4
C355 0.1u16X

Inform BIOS disable VIN2 with Power Fault

VCCP_NB R532 10KR1%/4 VIN2 → VIN2
R542 X_10KR1%/4
C547 10u6.3X/6

CPU_VDDP R541 10KR1%/4 VIN5 → VIN5
C555 10u6.3X/6

SIO HM Voltage over 2.048V will not detect

VCORE R356 10K/1% CPUVCORE 21
R374 X_10K1%/4
C359 10u6.3X6

VCC_DDR 10KR1%/4 R533
R534 10KR1%/4
C558 10u6.3X/6

VCCP_NB → VCCP_NB
CPU_VDDP → CPU_VDDP1
VCORE → VCORE
VCC_DDR → VCC_DDR

COM PORT

VCC3
C754 X_0.1u16X
VCC5

R842 X_2.7K/4 SINA
R820 X_2.7K/4 CTSA#
R839 X_2.7K/4 RIA#
R838 X_2.7K/4 DCDA#
R828 X_2.7K/4 DSRA#

NO USE UART PORT1

U71 GD75232DBR_SSOP20-RH
NRIA 20 VCC
NCTSA# 2 RA1
NDSRA# 3 RA2
NSINA 4 RA3
NDCDA# 7 RA4
9 RA5
VDD 16
RY1 19
RY2 18
RY3 17
RY4 14
RY5 12
DA1 1
DA2 19
DA3 18
GND 17
VSS 14
DY1 12
DY2 5
DY3 6
8
10

+12V_COM
RIA# 21
CTSA# 21
DSRA# 21
SINA 21
DCDA# 21
-12V_COM

RTSA# 21
DTRA# 21
SOUTA 21

C753 C0.1u16X/4
D49 1N4148W → +12V
C752 C0.1u16X/4
D48 1N4148W → -12V

JCOM1 H2X5[10]M_BLACK-RH
NDCDA# NSINA
NSOUTA NDTRA
NRTSA NDSRA#
NRIA NCTSA#

CN3 X_8P4C-470p50X4
NRTSA NDSRA# NCTSA# NRIA

CN4 X_8P4C-470p50X4
NDCDA# NSOUTA NSINA NDTRA

Thermal Monitor

For CPU Under Socket

HM_VREF → HM_VREF 21
R722 10K/1%
CPUTIN → CPUTIN 21
RT6 10KRT1%0402
C685 C2200p50X
GNDHM → GNDHM 21

R543 10KR1%/4
HM_VREF 21
CPUMOSTIN 21
RT1 10KRT1%0402
C528 C2200p50X/4
GNDHM 21

Close to CPU MOS

For System Close to SIO

SYSTIN → SYSTIN 21
Q53 P-3906
C488 2.2n50X/4
GNDHM

R551 10KR1%/4
HM_VREF 21
PROMTIN 21
RT2 10KRT1%0402
C533 C2200p50X/4
GNDHM 21

Close to CPU MOS

CPU RST

3VSB
0.1u16X C527
U81 X_NC7SZ08M5X_SOT23-5
6 PCIE_REST#
3VSB R600 4.7K
PCIE_REST# PCIE_RST_BUF

R804 100R1%/4 PCIERST#_PCIE1 → PCIERST#_PCIE1 19
R800 100R1%/4
R801 100R1%/4 PCIERST#_PROM → PLTRST_BU2#_M2 20, PCIERST#_PROM 16

PCIE_REST# R601 0R/4 PCIE_RST_BUF

PROM RESET

SIO 21 PLTRST_BU2#_R → R620 X_22R1%/4 → PLTRST_BU2#
R623 100R1%/4 → PCIERST#_PCIE2 19
R627 100R1%/4 → PCIERST#_PCIE3 19

PROM 16,25 PM_GPP_RST → R626 0R/4 → PLTRST_BU2#

Co-lay FCH Reset for meet FCH sequence. See 55553.

PARALLAL PORT

D45 1N4148W
VCC5 → A C LPT_VC
C656 C0.1u16X/4

21	PPRND3	R707 33R/4	PRND3	R716 2.7K/4		PRND0	C637	X_470p50/4
21	PPRND2	R736 33R/4	PRND2	R727 2.7K/4		PRND1	C641	X_470p50/4
21	PPRND1	R760 33R/4	PRND1	R741 2.7K/4		PRND2	C652	X_470p50/4
21	PPRND0	R700 33R/4	PRND0	R763 2.7K/4		PRND3	C639	X_470p50/4
21	PPRND4	R701 33R/4	PRND4	R719 2.7K/4		PRND7	C643	X_470p50/4
21	PPRND5	R733 33R/4	PRND5	R739 2.7K/4		PRND6	C644	X_470p50/4
21	PPRND6	R746 33R/4	PRND6	R749 2.7K/4		PRND5	C654	X_470p50/4
21	PPRND7	R780 33R/4	PRND7	R781 2.7K/4		PRND4	C640	X_470p50/4
21	STB#	R725 33R/4	RSTB#	R726 2.7K/4		RSTB#	C642	X_470p50/4
21	SLIN#	R745 33R/4	RSLIN#	R747 2.7K/4		RSLIN#	C651	X_470p50/4
21	INIT#	R757 33R/4	RINIT#	R767 2.7K/4		RINIT#	C657	X_470p50/4
21	AFD#	R782 33R/4	RAFD#	R784 2.7K/4		RAFD#	C638	X_470p50/4
21	RACK#			R729 2.7K/4		RACK#	C650	X_470p50/4
21	RBUSY			R756 2.7K/4		RBUSY	C655	X_470p50/4
21	RPE			R775 2.7K/4		RPE	C659	X_470p50/4
21	RSLCT			R723 2.7K/4		RSLCT	C649	X_470p50/4
21	RERR#			R715 2.7K/4		RERR#	C660	X_470p50/4

JLPT1 H2X13[26]M_BLACK-RH
RSTB# RAFD#
PRND0 RERR#
PRND1 RINIT#
PRND2 RSLIN#
PRND3
PRND4
PRND5
PRND6
PRND7
RACK#
RBUSY
RPE
RSLCT

N31-2131131-H06

MICRO-START INT'L CO.,LTD.

Title: SIO NCT6793D
Size: Custom | Document Number: MS-7A39 | Rev: 2.0
Date: Sunday, January 22, 2017 | Sheet 22 of 55

MICRO-START INT'L CO.,LTD.

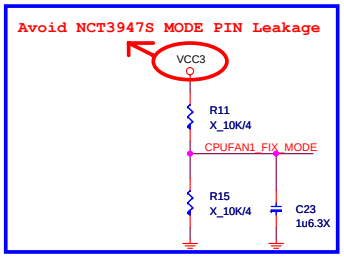
Title: Manual parts

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

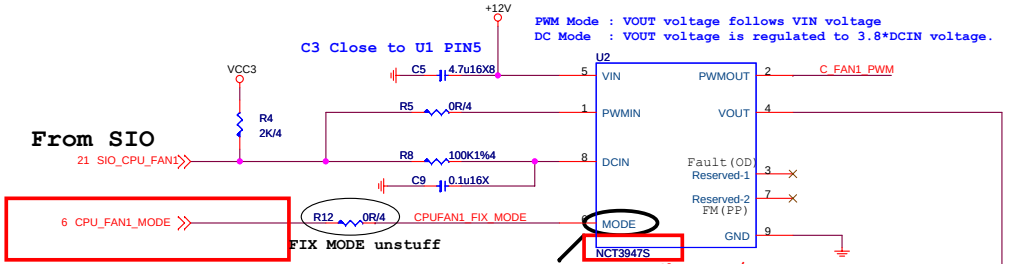
Date: Sunday, January 22, 2017 | Sheet 23 of 55

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　　パBIOSち传 PWM/DC MODE



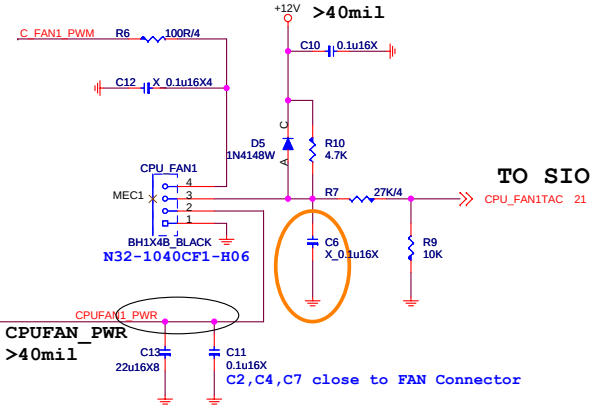
Resever For FIX DC or PWM MODE USE By PM SPEC

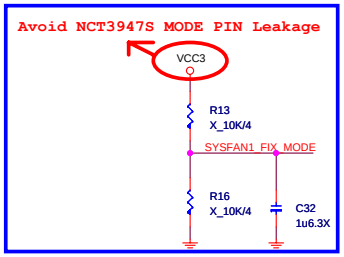


GPIO Control

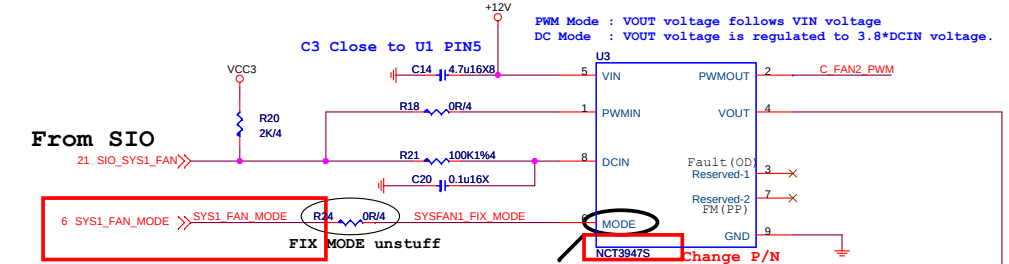
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V





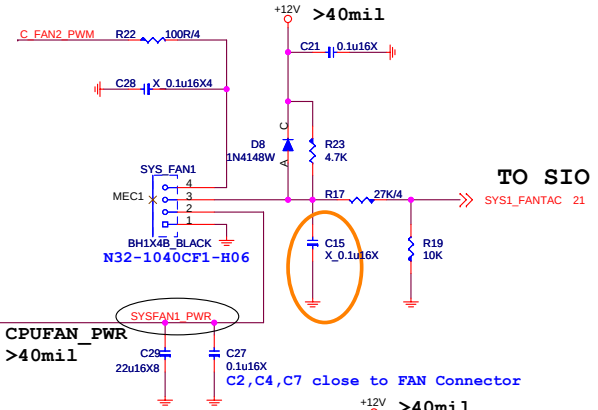
Resever For FIX DC or PWM MODE USE By PM SPEC

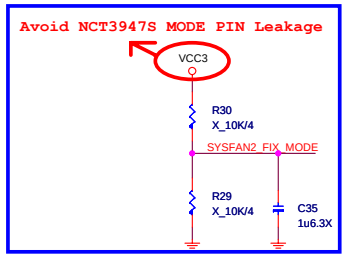


GPIO Control

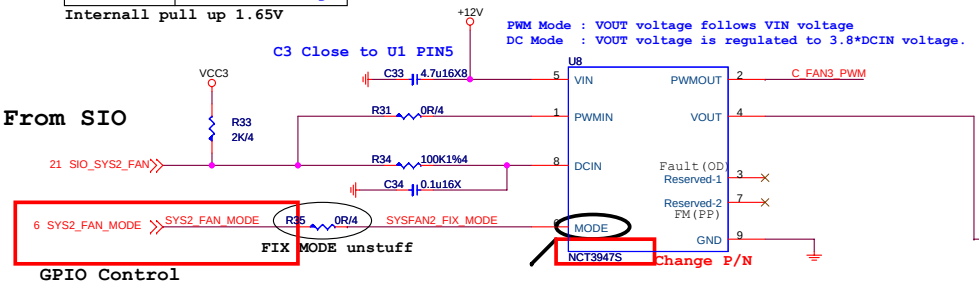
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V





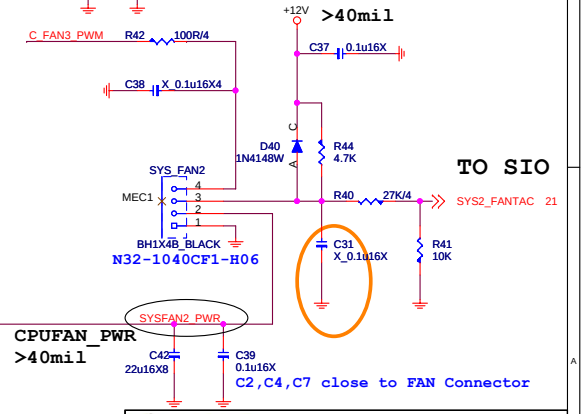
Resever For FIX DC or PWM MODE USE By PM SPEC



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



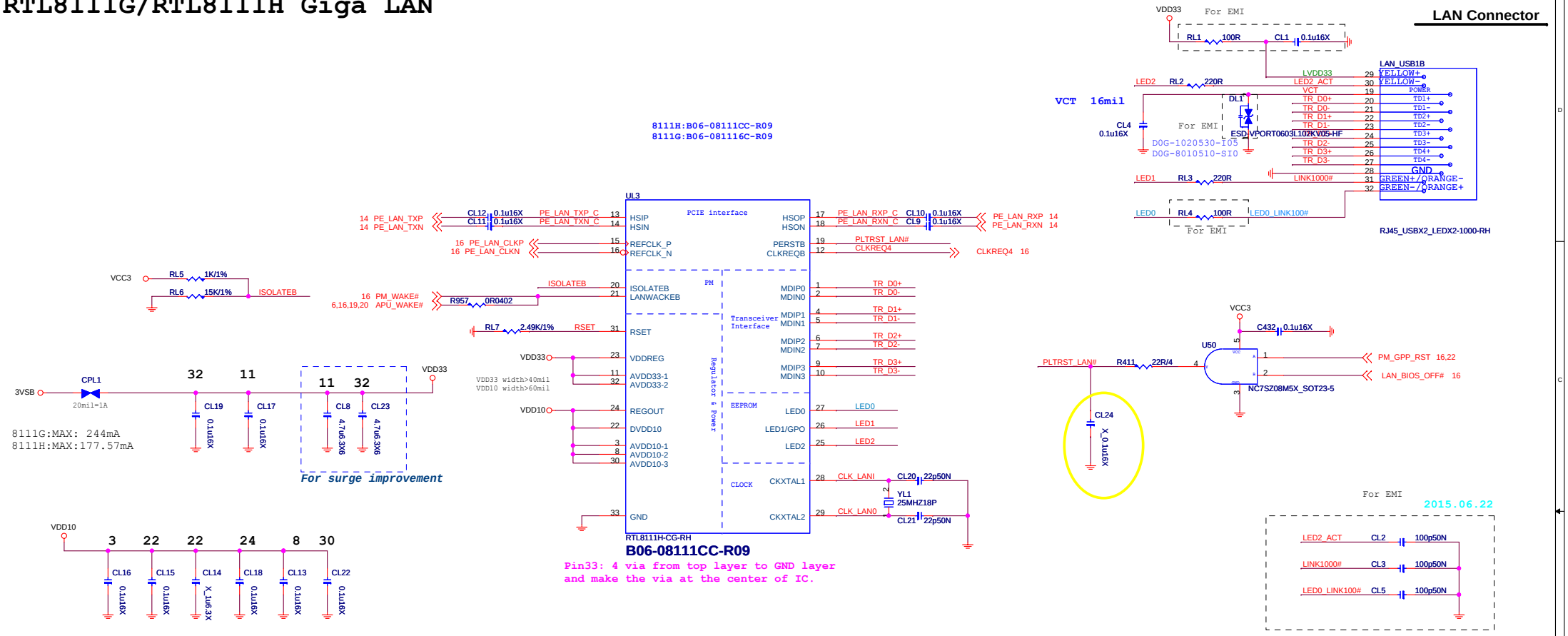
MSI MICRO-START INTL CO.,LTD.

Title: CPU FAN Control

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

Date: Sunday, January 22, 2017 | Sheet 24 of 55

RTL8111G/RTL8111H Giga LAN



LAN Connector

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

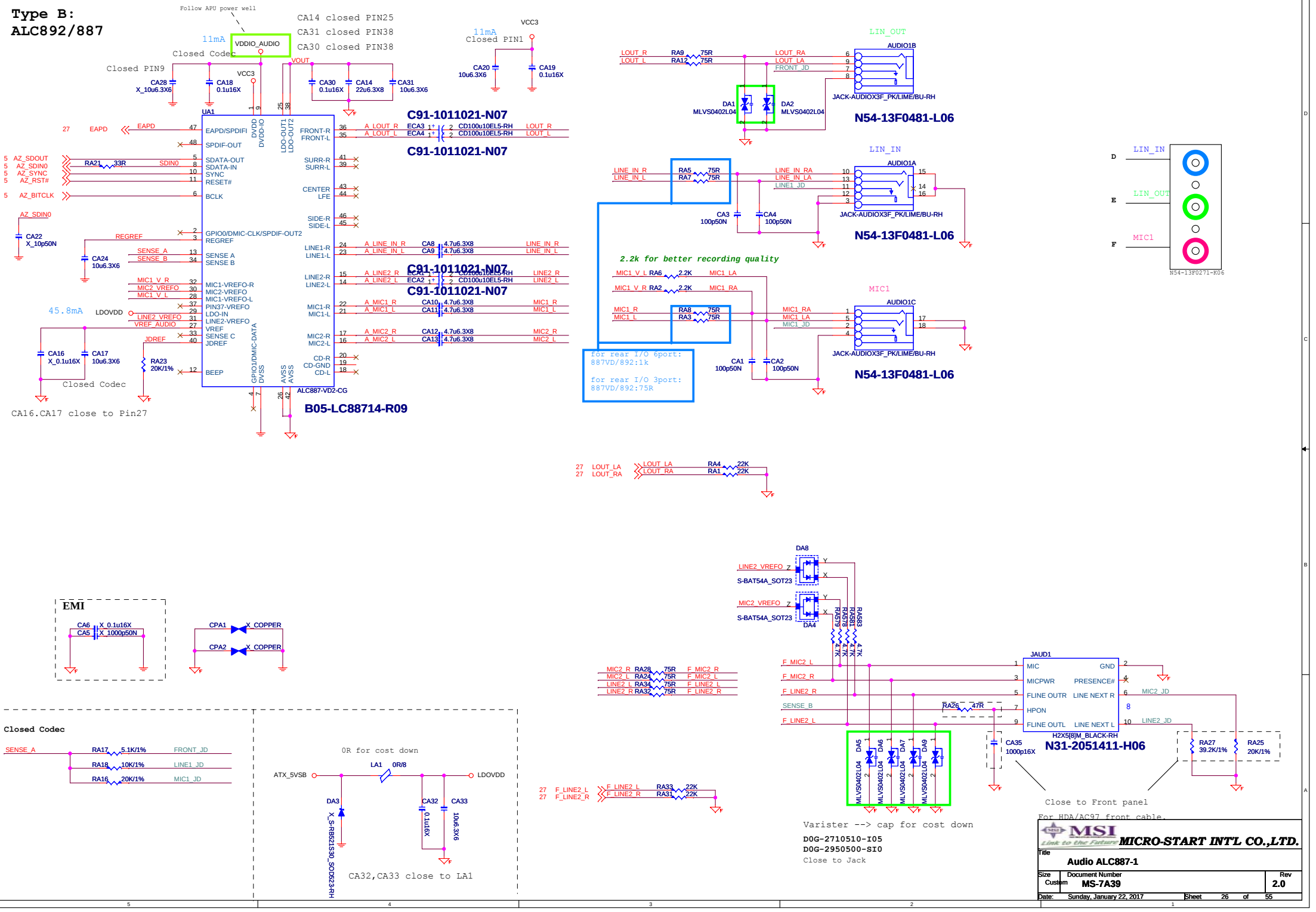
8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-START INT'L CO.,LTD.

Title: LAN-RTL8111H		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 25 of 55	

Type B:
ALC892/887



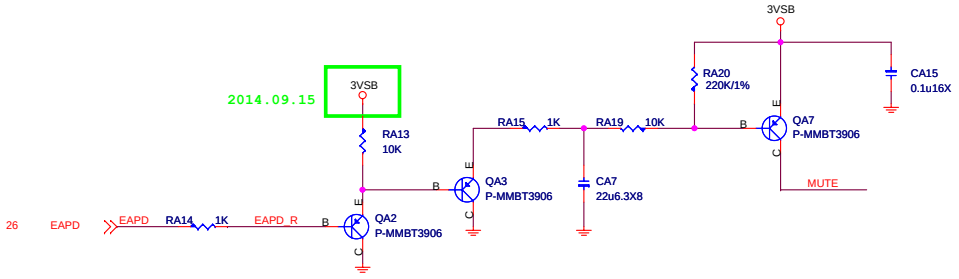
Varister --> cap for cost down
D0G-2710510-I05
D0G-2950500-SI0
Close to Jack

MSI Link to the Future
MICRO-START INT'L CO.,LTD.

Title	Audio ALC887-1	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 26 of 55	

Rear Line OUT De-POP circuit

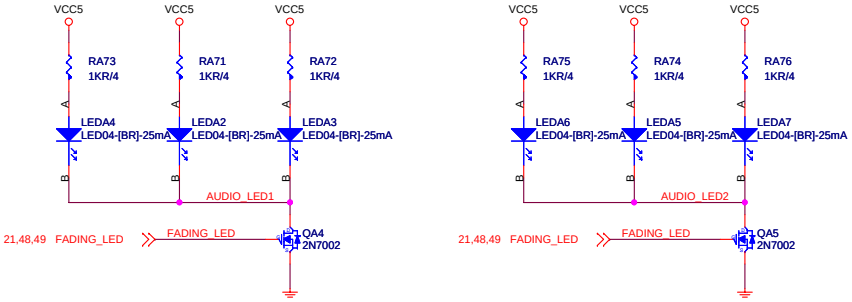
De-pop circuit for Rear Line out & Front Headphone out)

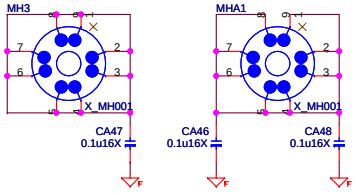


Digital

Analog

厂ノ代 LED

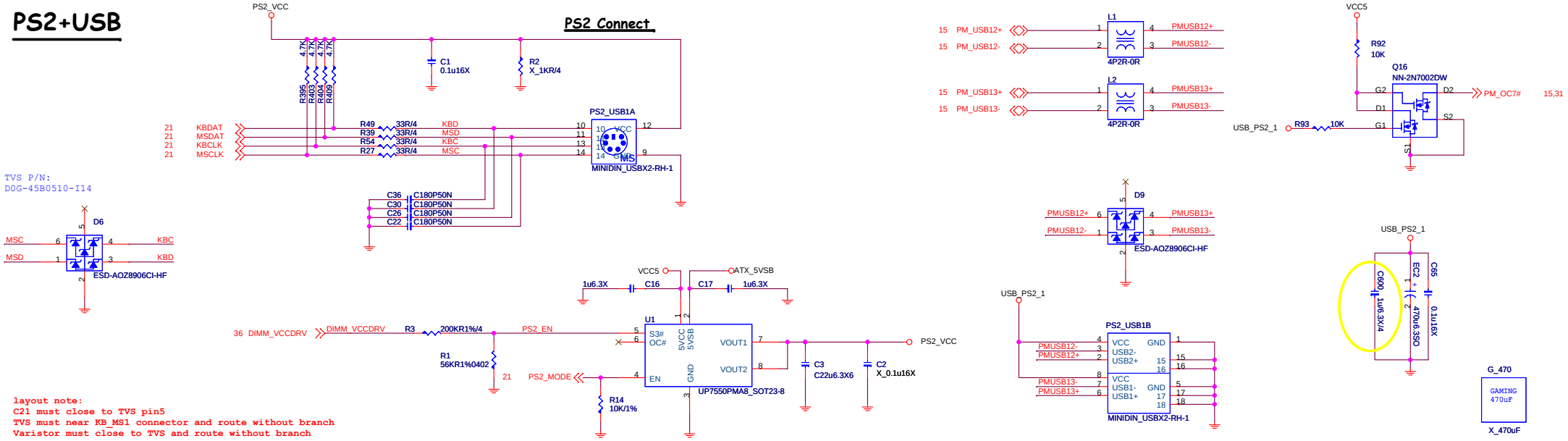




MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: Audio ALC887-2		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 27 of 55	

PS2+USB



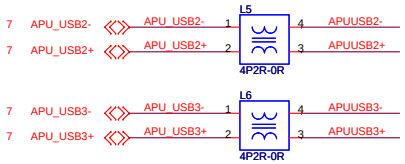
USB Power

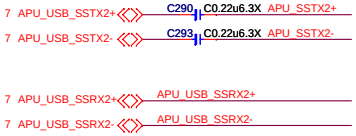
MICRO-START INT'L CO.,LTD.

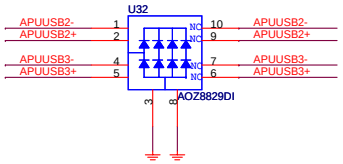
Title: USB Rear PS2+USB2.0		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 28 of 55	

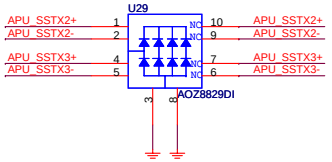
USB3.1 GEN1

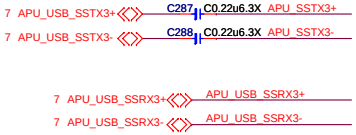
VR Sloution U2 redriver

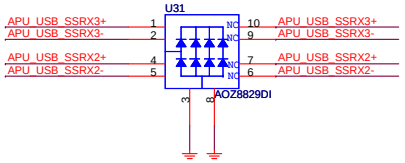




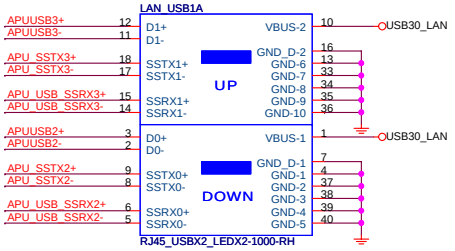


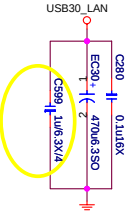






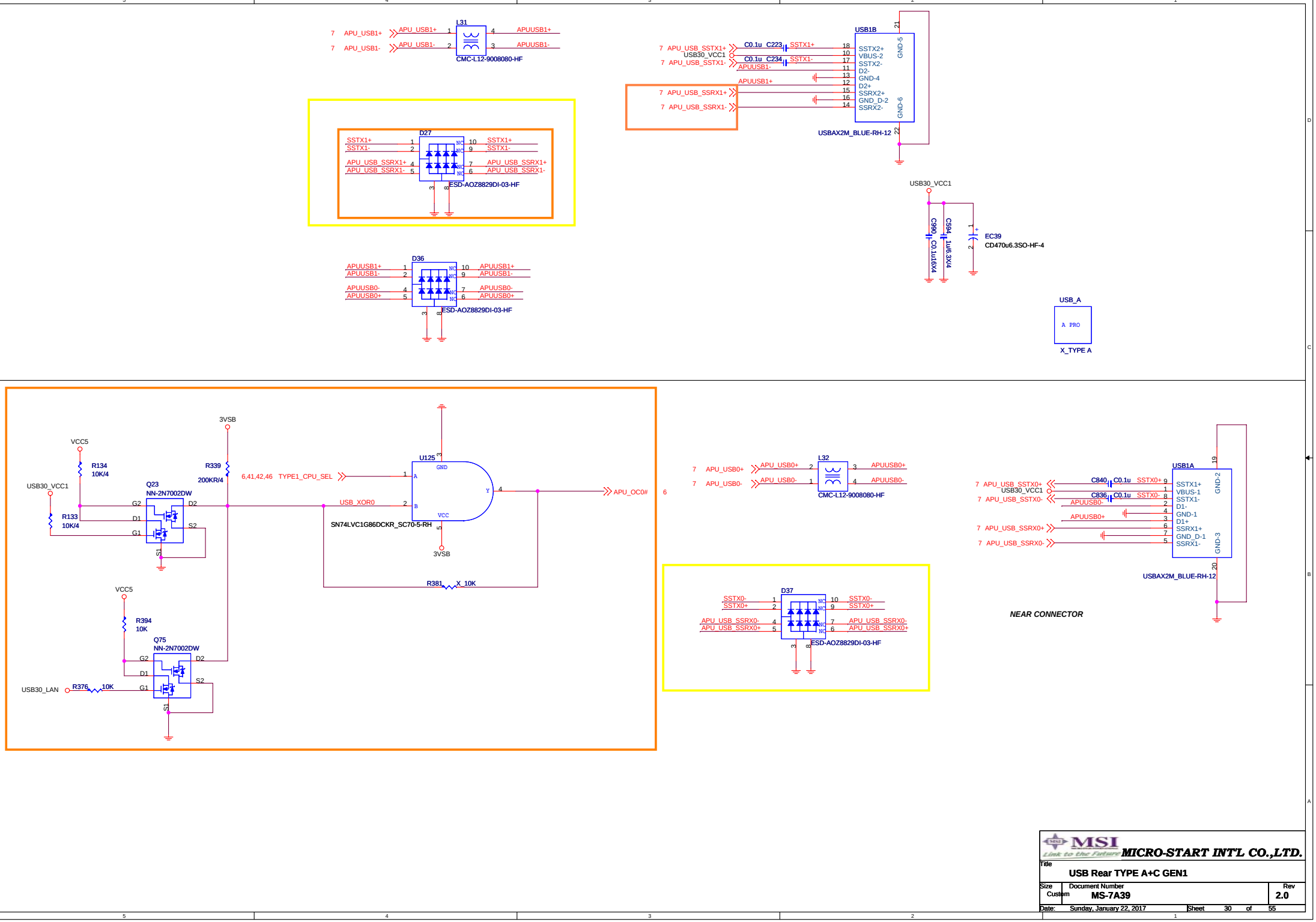
LAN+USB





MSI Link to the Future MICRO-START INT'L CO.,LTD.

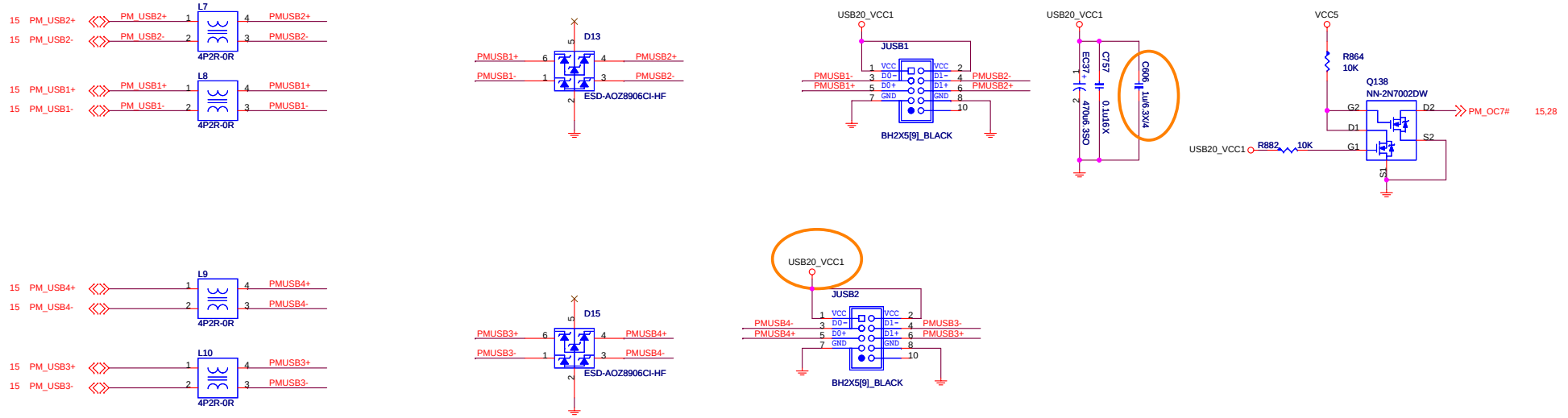
Title: USB Rear LAN+USB3.1 GEN1		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 29 of 55	



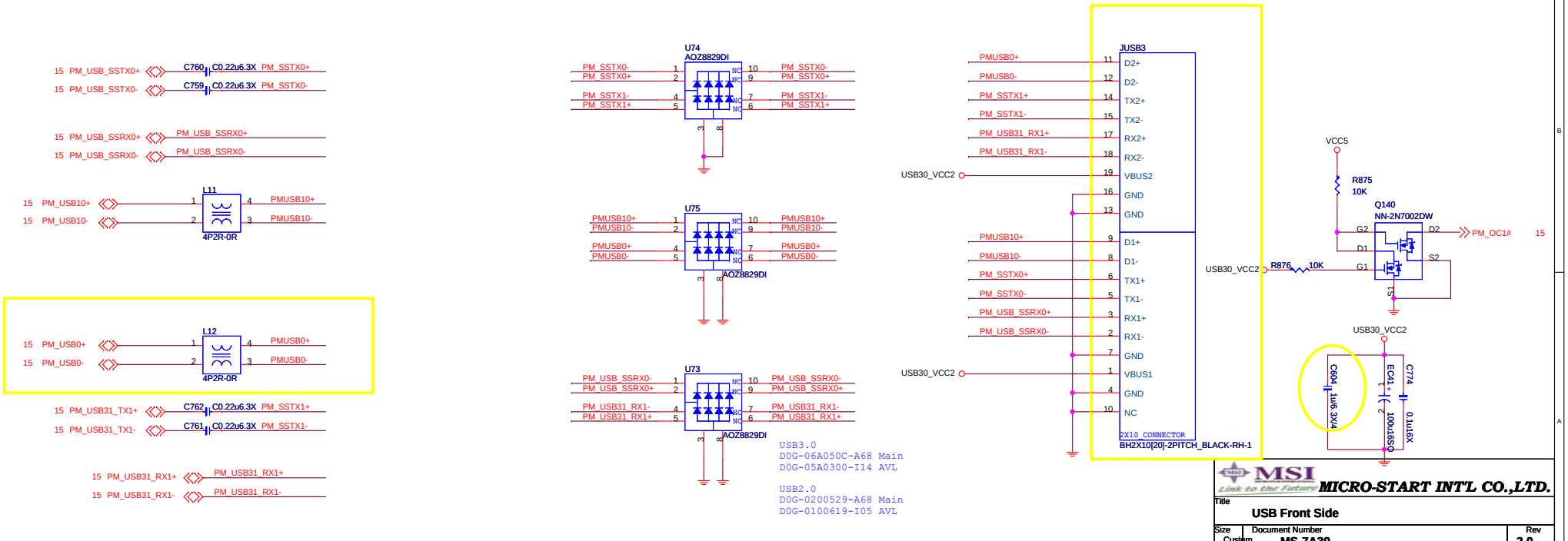
Title	USB Rear TYPE A+C GEN1
Size	Custom
Document Number	MS-7A39
Rev	2.0
Date:	Sunday, January 22, 2017
Sheet	30 of 55

MICRO-STAR INT'L CO.,LTD.

Front USB2.0

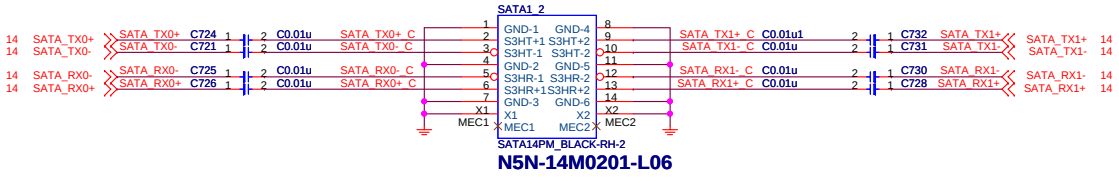


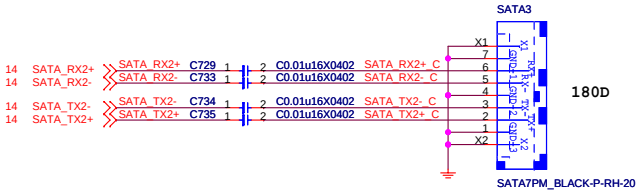
Front USB3.1 GEN1

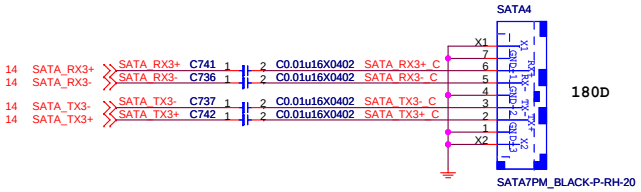


MSI Link to the Future	MICRO-START INTL CO.,LTD.		
Title: USB Front Side			
Size: Custom	Document Number: MS-7A39		Rev: 2.0
Date: Sunday, January 22, 2017		Sheet 31 of 55	

SATA Connector







MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: SATA Connector		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 32 of 55	

DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

5 DVI_DDPC_CLK_N — C154 0.1u16X — DVI_TXC- — R165 499R/1%
5 DVI_DDPC_CLK_P — C159 0.1u16X — DVI_TXC+ — R201 499R/1%
5 DVI_DDPC_TXN2 — C149 0.1u16X — DVI_TXD2- — R194 499R/1%
5 DVI_DDPC_TXP2 — C171 0.1u16X — DVI_TXD2+ — R164 499R/1%
5 DVI_DDPC_TXN1 — C169 0.1u16X — DVI_TXD1- — R207 499R/1%
5 DVI_DDPC_TXP1 — C143 0.1u16X — DVI_TXD1+ — R160 499R/1%
5 DVI_DDPC_TXN0 — C144 0.1u16X — DVI_TXD0- — R150 499R/1%
5 DVI_DDPC_TXP0 — C141 0.1u16X — DVI_TXD0+ — R192 499R/1%

DVI_DATA

VCC3 — Q71 2N7002 — R617 0R/6

2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

DVI_VGA_5V — R169 2.2K
DVI_VGA_5V — R193 2.2K

Q84 2N7002D
VCC3 — G2
DVI_DDC_CLK_R — D1
VCC3 — G1
S1
D2 — DVI_DDC_DATA_R
S2 — DVI_DDPC_CTRLDATA 5
5 DVI_DDPC_CTRLCLK

VCC3 — C489 X_0.1u16X

VCC3 — RH21 4.7K/4 — DVI_DDPC_CTRLCLK
VCC3 — RH22 4.7K/4 — DVI_DDPC_CTRLDATA

U6 AOZ8829DI
DVI_TXD2+ 1 — DVI_TXD2+ 10
DVI_TXD2- 2 — DVI_TXD2- 9
DVI_TXD1+ 4 — DVI_TXD1+ 7
DVI_TXD1- 5 — DVI_TXD1- 6
NC 8 NC 3

U5 AOZ8829DI
DVI_TXD0+ 1 — DVI_TXD0+ 10
DVI_TXD0- 2 — DVI_TXD0- 9
DVI_TXC+ 4 — DVI_TXC+ 7
DVI_TXC- 5 — DVI_TXC- 6
NC 8 NC 3

VGA_DVI1B
DVI_VGA_5V
X1 Shell-1
DVI_TXD2- D1
DVI_TXD2+ D2 DATA2
D3 DATA2 SHIELD-1
D4 DATA4
D5 DATA4
DVI_DDC_CLK_R D6 DDCCLK
DVI_DDC_DATA_R D7 DDCDATA
D8 NC
DVI_TXD1- D9 DATA1
DVI_TXD1+ D10 DATA1
D11 SHIELD-2
D12 DATA3
D13 DATA3
D14 VCC5
D15 GND5
DVI_HOT_DET D16 HPDET
DVI_TXD0- D17 DATA0
DVI_TXD0+ D18 DATA0
D19 SHIELD-3
D20 DATA5
D21 DATA5
DVI_TXC+ D22 SHIELD-4
DVI_TXC- D23 CLK
D24 CLK
X2 Shell-2
VGA_DVI-RH-22

DVI_VGA_5V — C155 0.1u16X

U4 ESD-AOZ8906CI-HF
DVI_DDC_CLK_R 6 — 4 DVI_DDC_DATA_R
DVI_HOT_DET 1 — 3
5
2

HPD

VCC3 — R191 10K
DVI_VGA_5V — R203 10K
5 DVI_DDPC_HPD
C173 X_0.01u16X
Q28 NN-CMKT3904
DVI_HOT_DET_R — R171 10K — DVI_HOT_DET
R168 100K
C148 0.01u16X

For EMI

DVI_TXD0- — R151 X_243R/1% — DVI_TXD0+
DVI_TXD1- — R158 X_243R/1% — DVI_TXD1+
DVI_TXC- — R200 X_243R/1% — DVI_TXC+
DVI_TXD2- — R162 X_243R/1% — DVI_TXD2+

DVI_HOT_DET
DVI_DDC_CLK_R
DVI_DDC_DATA_R
C147 X_10p50N
C146 X_10p50N
C151 X_10p50N

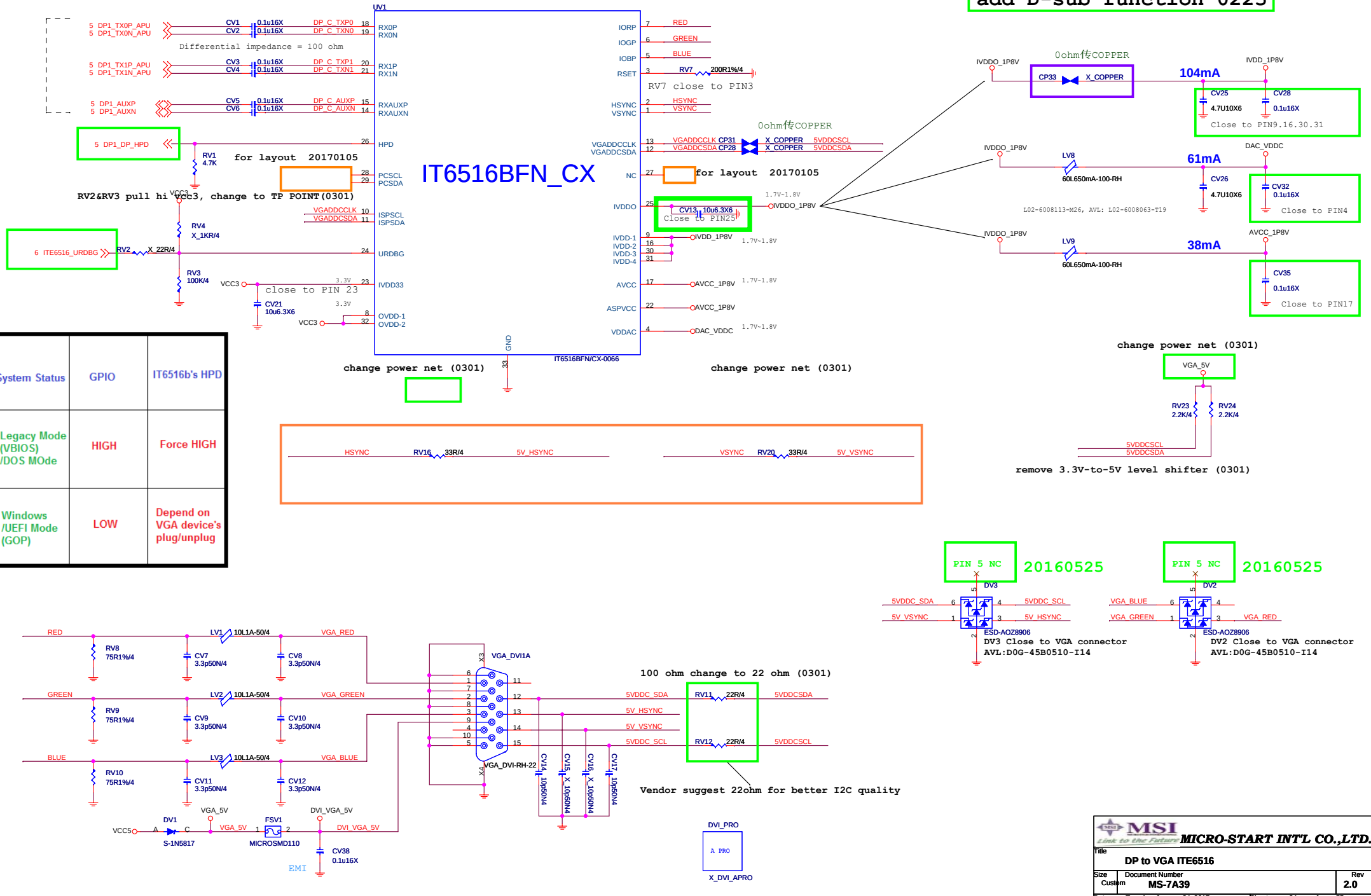
MICRO-START INT'L CO.,LTD.

Title	DVI Connector	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 33 of 55	

Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

add D-sub function 0225



System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

change power net (0301)

remove 3.3V-to-5V level shifter (0301)

PIN 5 NC 20160525

DV3 Close to VGA connector
AVL:D0G-45B0510-I14

PIN 5 NC 20160525

DV2 Close to VGA connector
AVL:D0G-45B0510-I14

MICRO-START INTL CO.,LTD.

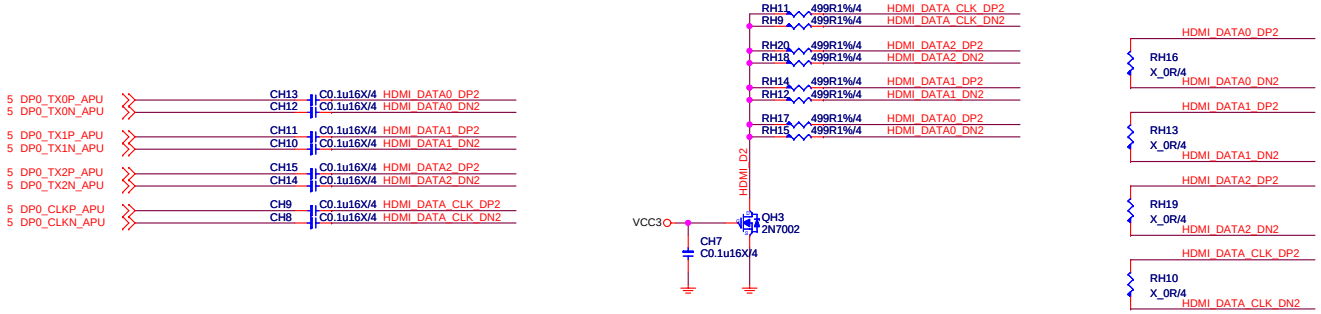
Title: DP to VGA ITE6516

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

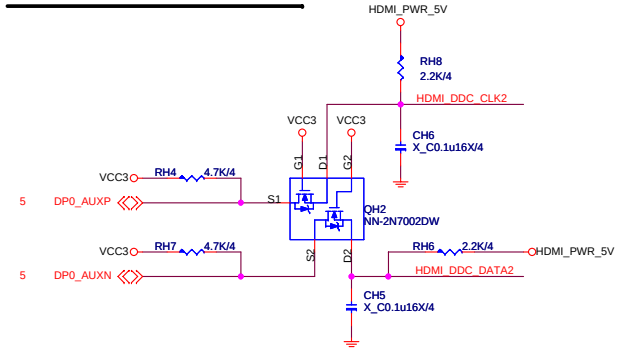
Date: Tuesday, January 24, 2017 | Sheet 34 of 55

HDMI CONNECTOR

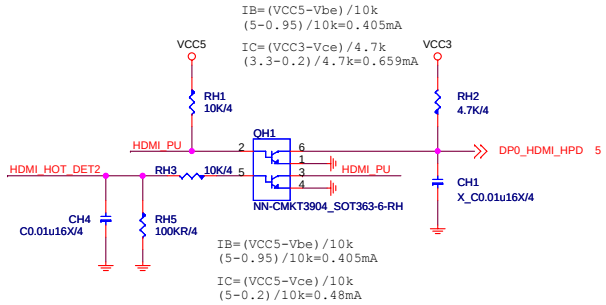
For HDMI 1.4



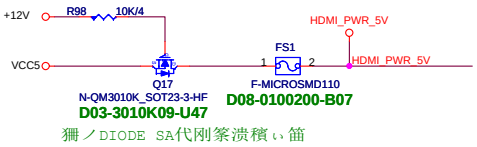
AUX Level Shifter



HPD Circuit

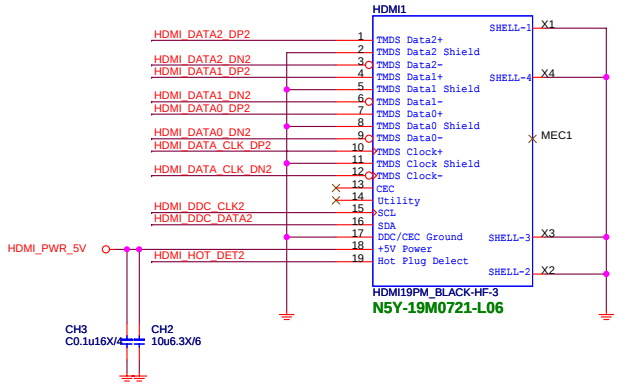


Connector Power

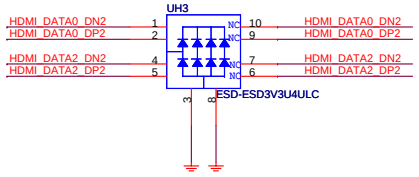


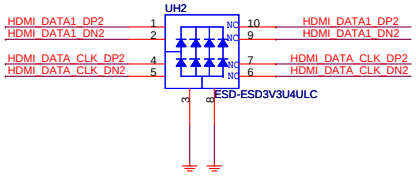
猫ノDIODE SA代刚篆溃稹い笛

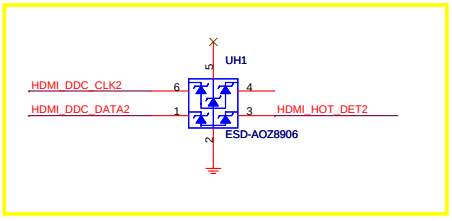
Connector



For EMI



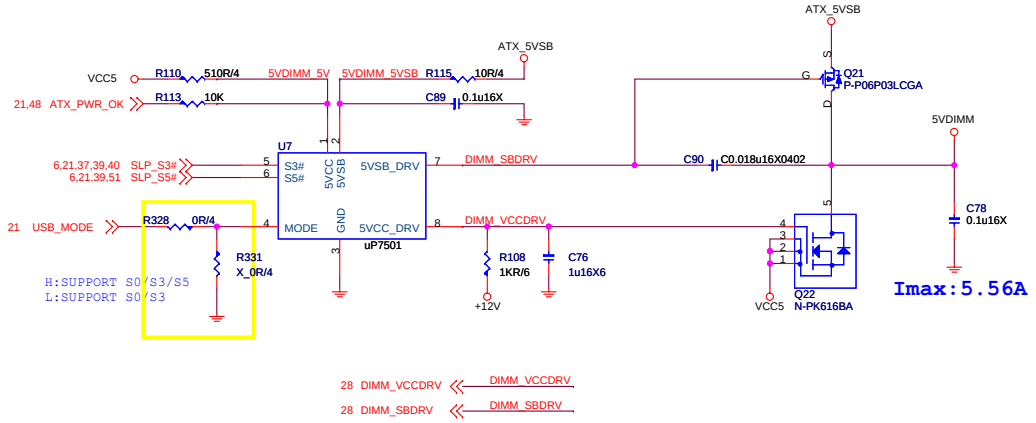




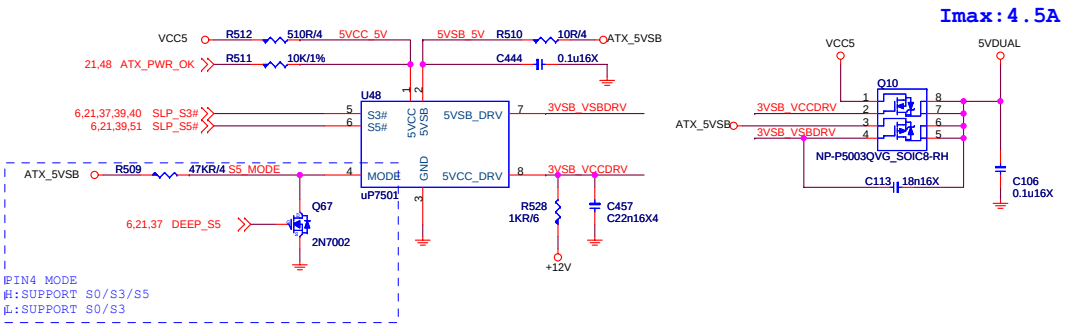
MSI MICRO-START INT'L CO.,LTD.

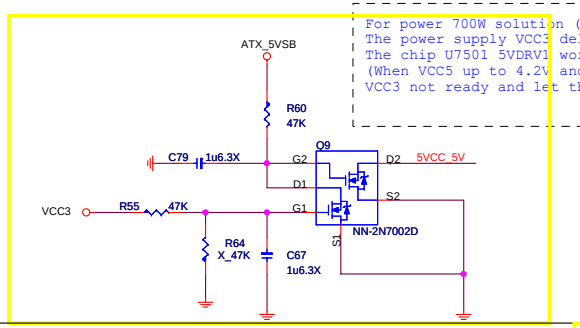
Title: HDMI 1.4		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 35 of 55	

5VDIMM FOR DDR

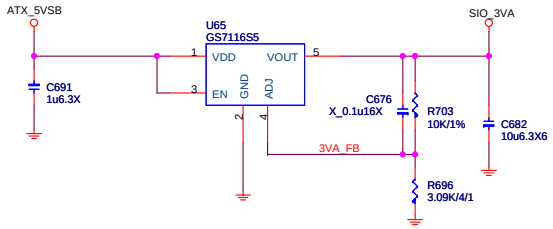


5VDUAL For 3VSB CPU 1.8V VDDP

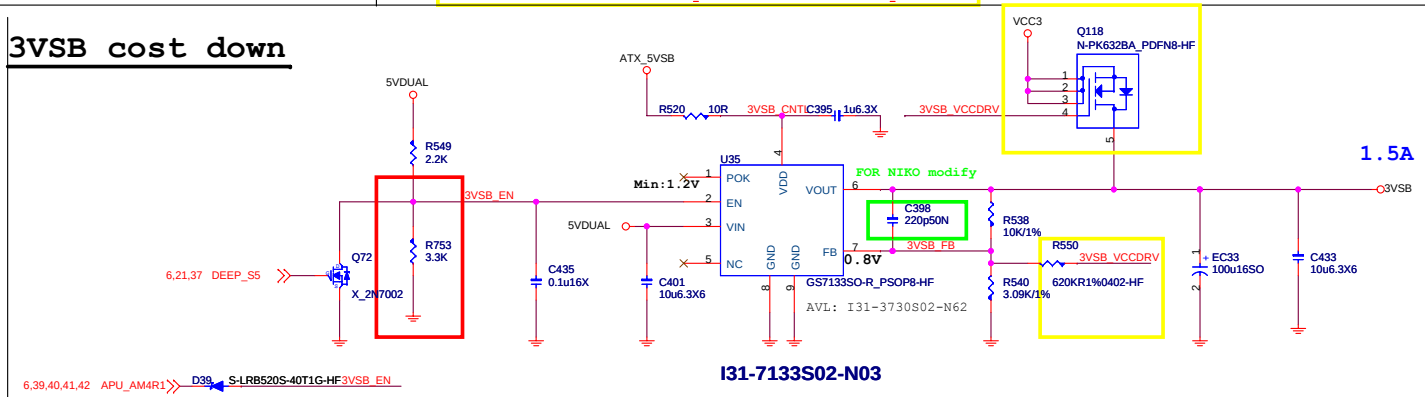




SIO_3VA



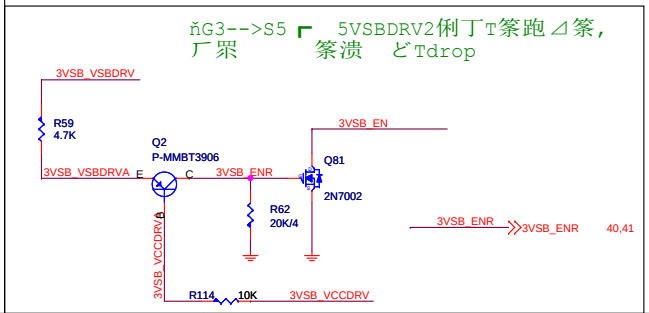
3VSB cost down



3VSB cost down

3.3V@1.4959A

1.05V@0.05A
VDDBT_RTC_G@4.5uA
FCH@0.07A
CPU@0.25A
*PCIE*3 @1.125A*
USB TYPE-C @0.9mA



MSI MICRO-START INTL CO.,LTD.

Title: ACPI uPI-5VDIMM&3VSB		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 36 of 55	

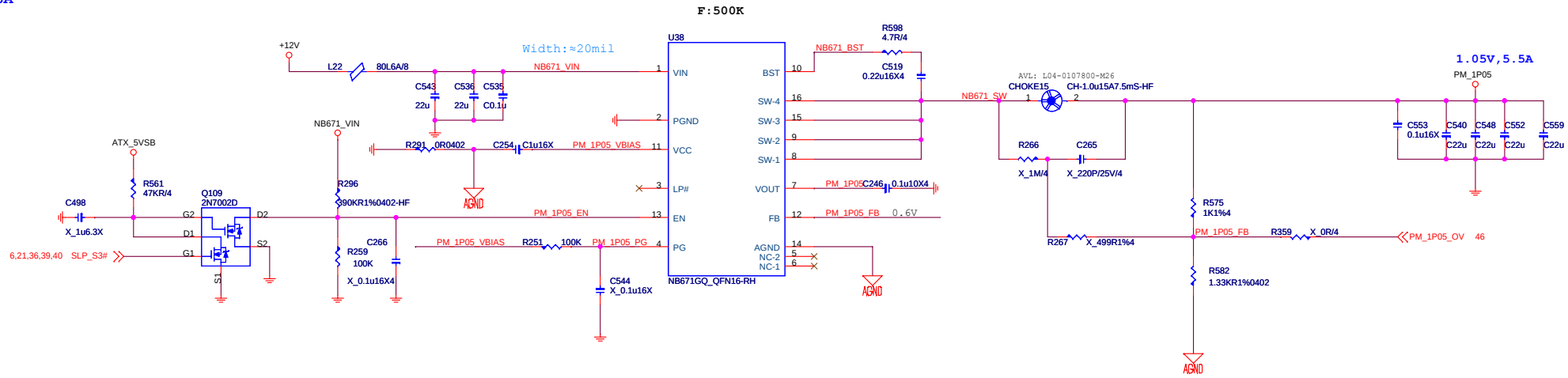
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

support OV=>NB685
not support OV=> NB681

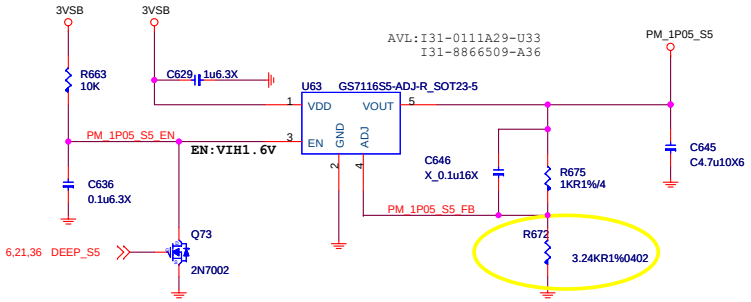
IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*

0.7776uH≤L≤1.1664uH



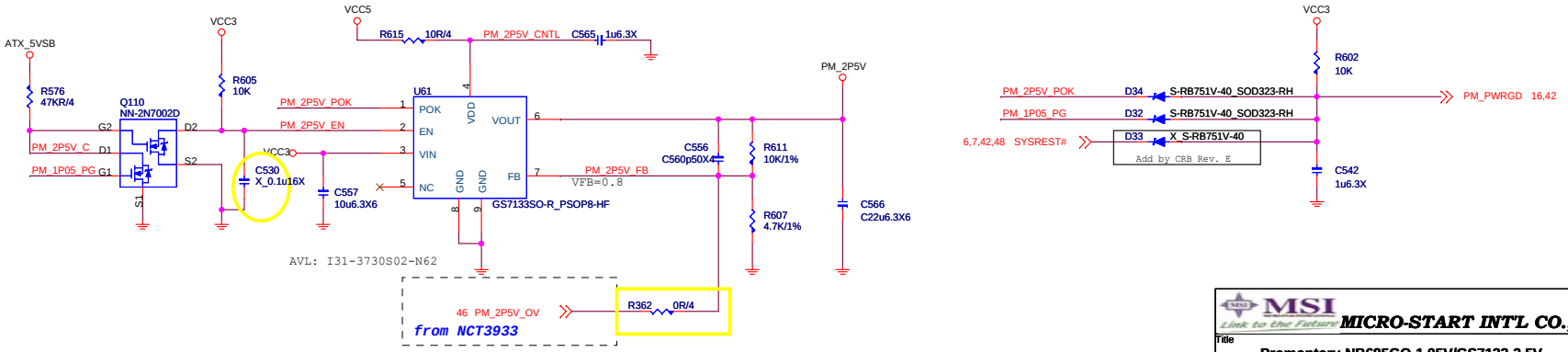
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

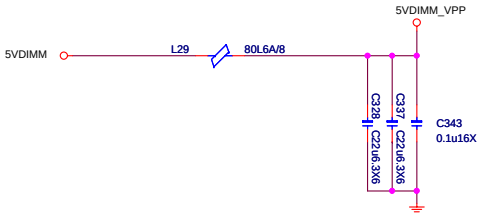
2.5V; 900mA

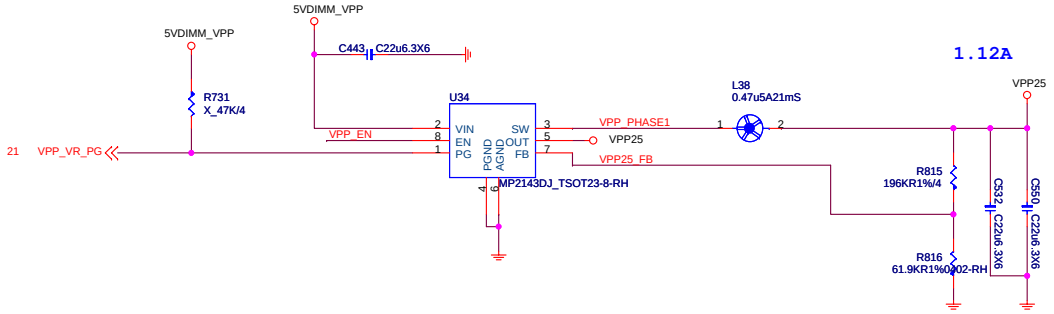


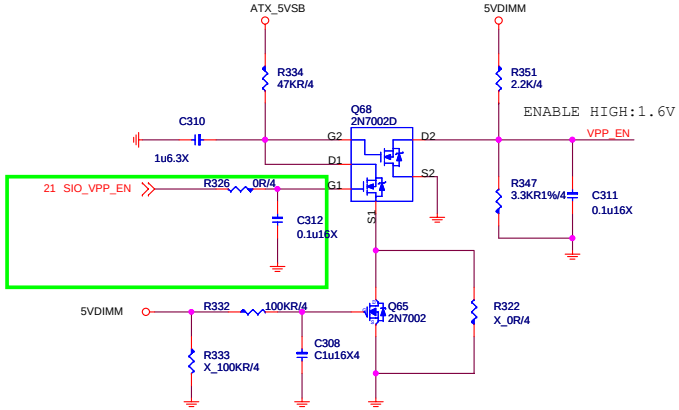
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	Promontory-NB685GQ-1.05V/GS7133-2.5V	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 37 of 55	

2DIMM :1.12A FOR DDR VPP2.5V







MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title: DDR PWR VPP25/VTT-MP2143		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 38 of 55	

DDR4_1.2V 15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM

0.3*2=0.6A FOR DDR VTT

OCP =7.925A*1.5=11.8875A

Current limit= 110K(R178)*5uA/10/4mohm)=33A

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675
L	0.75

OCP:27.5A

Imax: 20.85A

By layout modify

f:400KHz

27.5A

FB:0.75V

I32-8231A0C-R11

MAX:20.85A

1.2V

0.1uFx1 per dimm

Close to PIN19

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K

MICRO-START INT'L CO.,LTD.

Title: DDR Power-RT8231AGQW

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

Date: Sunday, January 22, 2017 | Sheet 39 of 55

FOR CPU 1.8V S5

0.5A

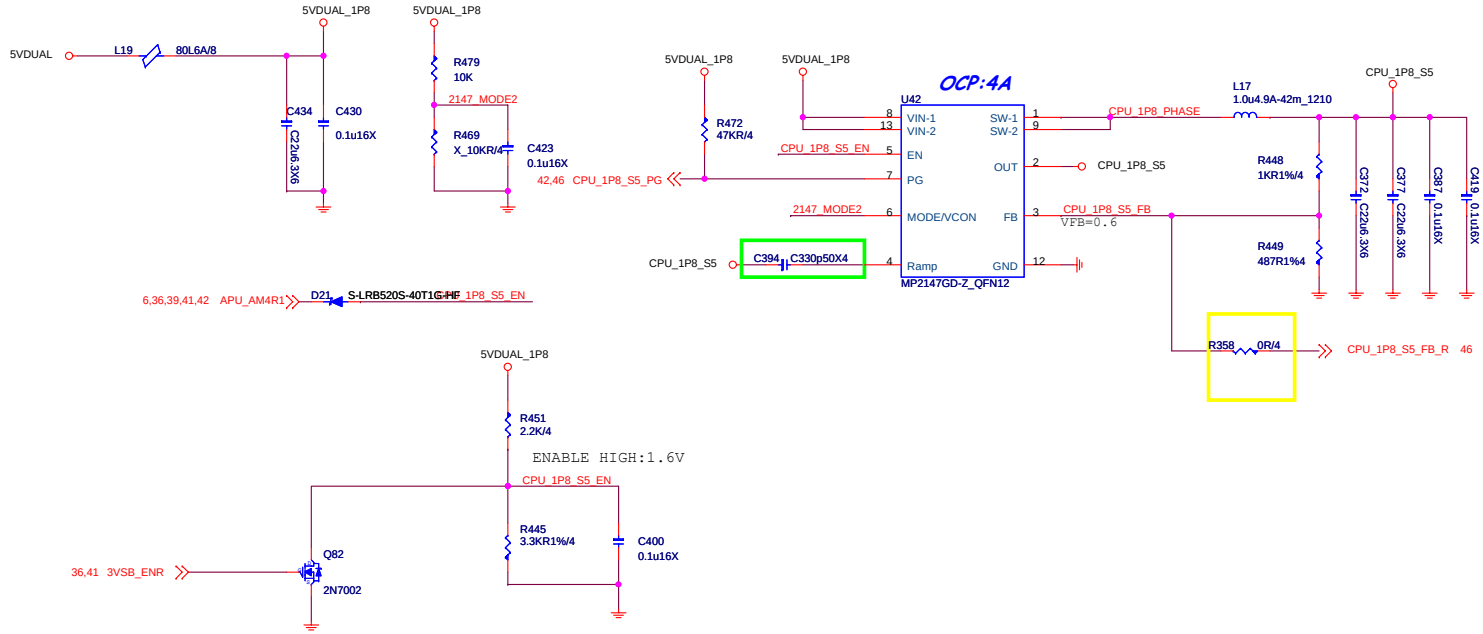
FOR VCCP_SOC_S5

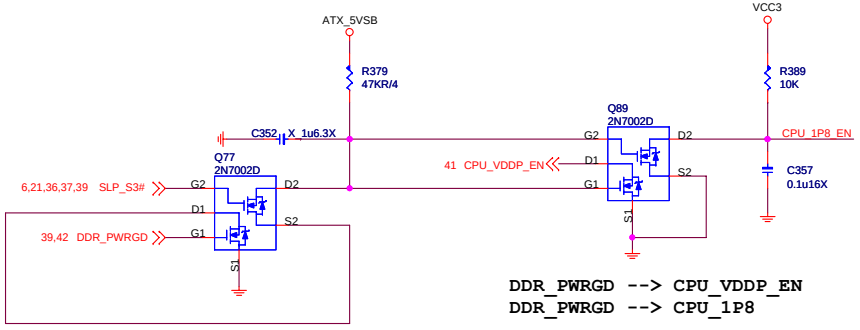
0.9A

FOR CPU 1.8V S0

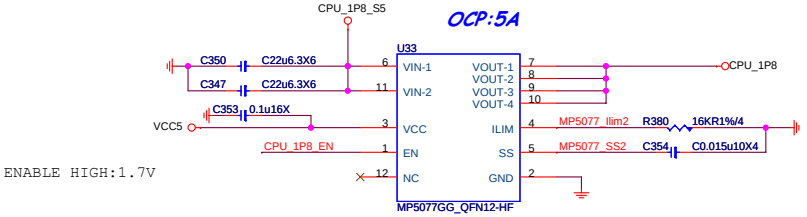
2.0A

0.5A + 2.0A + 0.9A =3.4A





DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



Ilimit=(1/Rlimit)*S,S=80000,when VIN=1.8V
=(1/16)*80000=5.0375A

Tss=(1/3)*((Vout*Css)/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n)/9uA)=1mS

MICRO-START INT'L CO.,LTD.

Title: CPU Power 1P8V-MP2147		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 40 of 55	

CPU_VDDP_S0

1.05V/0.9
S0:8.5A
OCP=12A

by layout

+12V
R406 100K1%4
EN:VIH1.6V
CPU_VDDP_EN
R418 33K/1%
C389 0.1u16X

VCC5
R437 10K
42 CPU_VDDP_PG

EN:VIH1.6V
EN pin Maximum:6.5V

by layout
+12V
R494 10R/8
U6_VCC
C429 C1u16X6

6,36,39,40,42 APU_AM4R1
D20 S-LRB520S-40T1G-HF
CPU_VDDP_EN

U41
EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT
PHASE
UGATE
LGATE/OCSET
FB
RT8125EGQW_WDFN10-HF

CPU_VDDP_BOOT1
R484 0R/6
C440 0.1u16X25
CPU_VDDP_PH1
CPU_VDDP_UG1
CPU_VDDP_LG1
CPU_VDDP_FB
FB:0.8V

CPU_VDDP_REFOUT
C426 C1000p50X4
R453 768R1%4
CPU_VDDP_REFIN
0.8V
0.684V
C374 C1000p50X4
R463 4.53KR1%4

CPU_VDDP
R420 10R1%4
R438 1KR1%/4
CPU_VDDP_SENSE_R
R421 0R/4
CPU_VDDP_SENSE 6
C399 X_0.1u16X
R450 3.16K/1%

AM4_CPU_SEL
0:Type 0/1 1.05V
1:Type 2/3 0.9V

6,30,42,46 TYPE1_CPU_SEL
Q86 NN-2N7002DW
G2 D2
16 PM_GPIO_R9 D1
G1 S2
S1

46 CPU_VDDP_OV
CP25 X_COPPER

PM_GPIO_R9
1:Type 0/1 1.05V
0:Type 2/3 0.9V

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.8 * 0.282566
= 3.46A

TYPE0_CPU_SEL:
1:TYPE 0
0:TYPE 2

CPU_VDDP_EN:
0:TYPE 2
1:TYPE 0

Q92 NN-2N7002DW
6,42 TYPE0_CPU_SEL
VDDP_SEL
6,30,42,46 TYPE1_CPU_SEL
G2 D2 CPU_VDDP_EN
D1 S2 VDDP_SEL
G1
S1
CPU_VDDP_EN 40

TYPE1_CPU_SEL:
0:TYPE 0
1:TYPE 2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

12VCC_IN
CHOKE14 CH-0.47u5A21mS-HF
+12V
C461 C1u16X6
C460 22u16X8
EC11 270u16SO
C446 0.1u16X

CPU_VDDP_UG1
R508 0R/6
CPU_VDDP_UG1_R
R500 X_10KR/4
N-PK616BA_PDFN8-HF
Q97

CPU_VDDP_PH1
CHOKE13 1.0u15A7.5mS-HF
CPU_VDDP
OCP=12A
1.05V,8.5A

CPU_VDDP_LG1
R482 X_2.2R/8
snubber
C437 X_C3300p50X4
C334 1u6.3X
C425 C22u6.3X6
EC31 560u6.3SO
EC32 560u6.3SO

OCPSET:min 5Kohm
OCP
=(R475*10uA)/DCR
=(5.1k*10uA)/3.3m
=15.45A
R475 5.1K/1%/4
N-PK632BA_PDFN8-HF
Q96

CPU_VDDP_S5

VDDP_S5 1.05V/0.9
S5:1A

3VSB
3VSB
5VDUAL
L20 80L6A/8
R501 X_10KR/4
R502 10K
C439 C22u6.3X6
U45
VDDP_VSB_VIN
VDDP_VSB_EN
VDDP_VSB_PG
VIN
EN
PG
PGND
AGND
SW
OUT
FB
MP2143DJ
VDDP_VSB_PHASE
VDDP_VSB_FB
42 VDDP_VSB_PG
Internal Pull-Up 500K

L18 1.0u6.3A_1210-HF
CPU_VDDP_S5
R489 1KR1%/4
R488 2KR1%/4
C412 C22u6.3X6
C421 C22u6.3X6
C427 C0.22u6.3X4

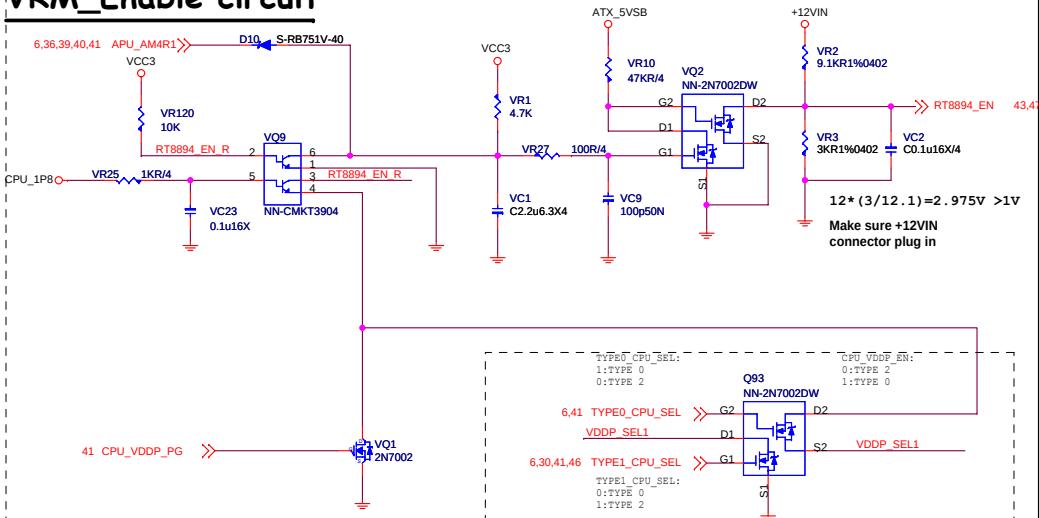
6,36,39,40,42 APU_AM4R1
D28 S-LRB520S-40T1G-HF
VDDP_VSB_EN
C390 X_0.1u16X
36,40 3VSB_ENR
Q98 2N7002

VDDP_VSB_FB
ATX_5VSB
R464 3.83KR1%4
R490 47KR/4
Q95 NN-2N7002DW
C436 0.1u16X
6,30,42,46 TYPE1_CPU_SEL
AM4_CPU_SEL
0:Type 0/1
1:Type 2/3
R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

MSI MICRO-START INTL CO.,LTD.

Title			
CPU Power VDDP-RT8125E			
Size: Custom	Document Number: MS-7A39		Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 41 of 55		

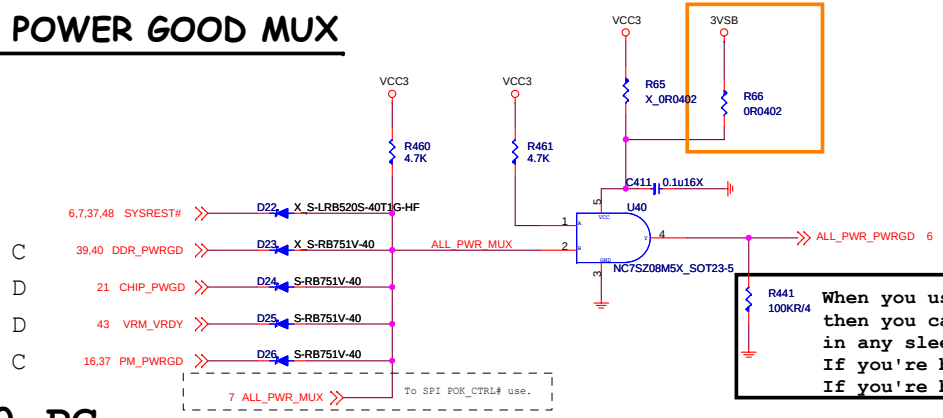
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

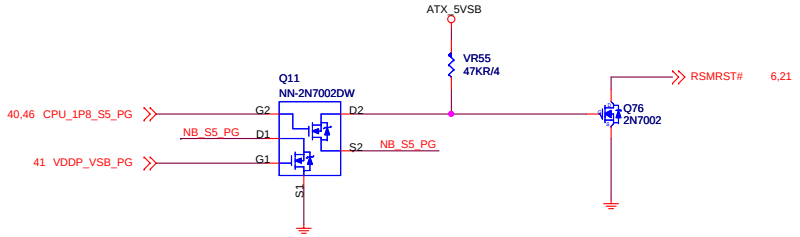


R441 100KR/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG

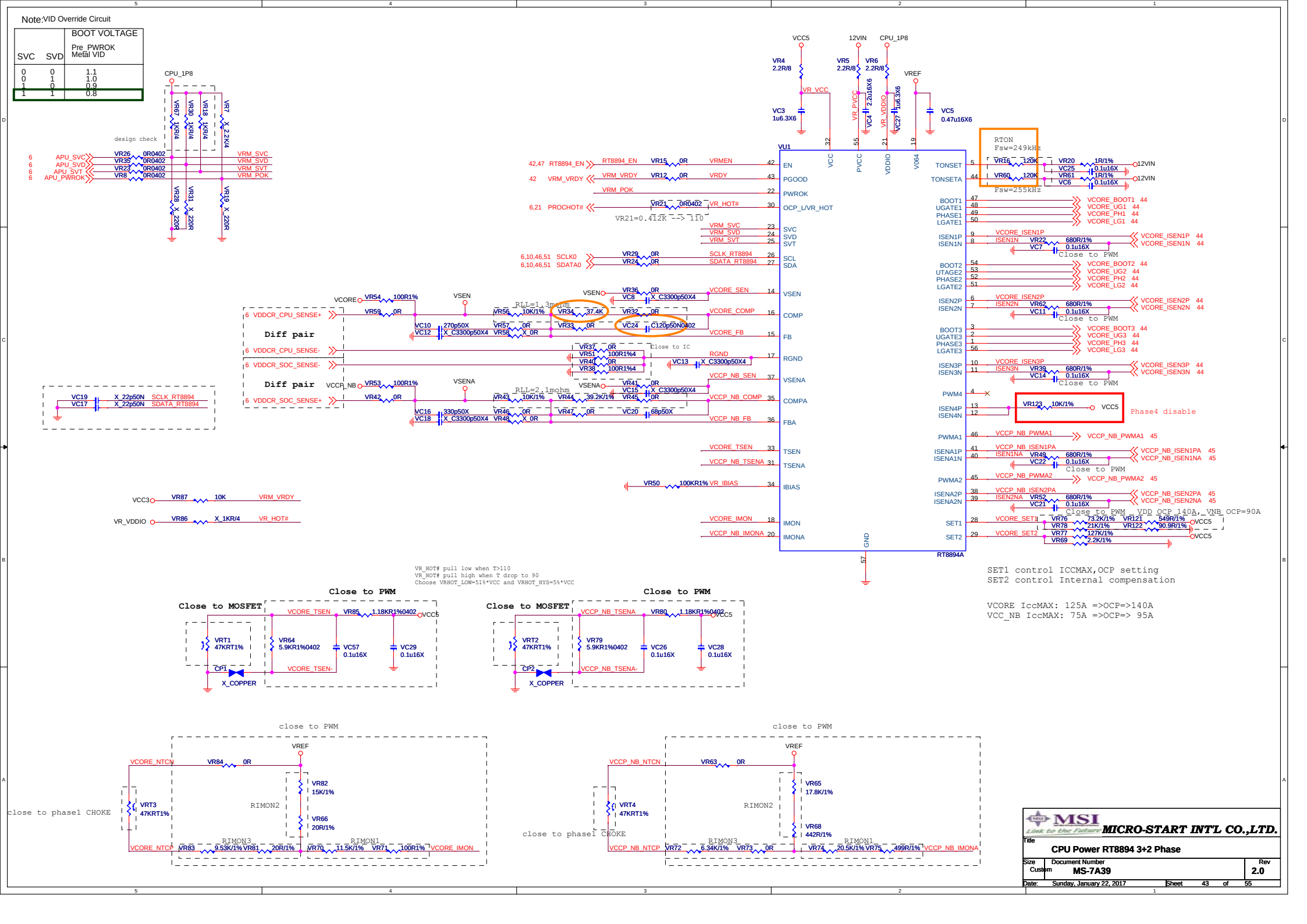


MSI MICRO-START INT'L CO.,LTD.

Title	CPU PWR-IR3599	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 42 of 55	

Note:VID Override Circuit

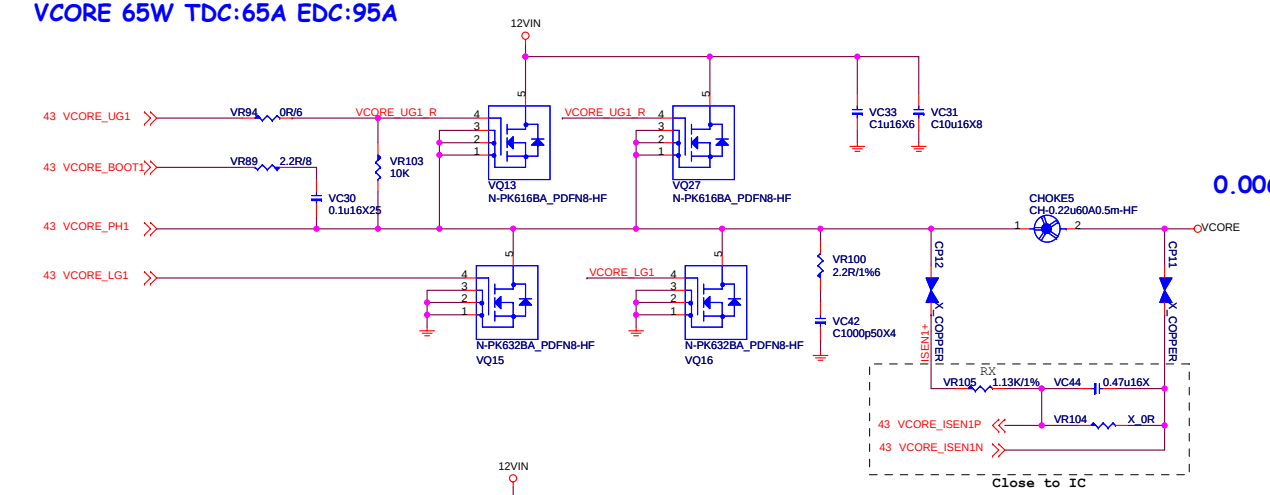
SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



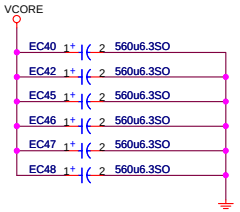
MICRO-START INT'L CO.,LTD.

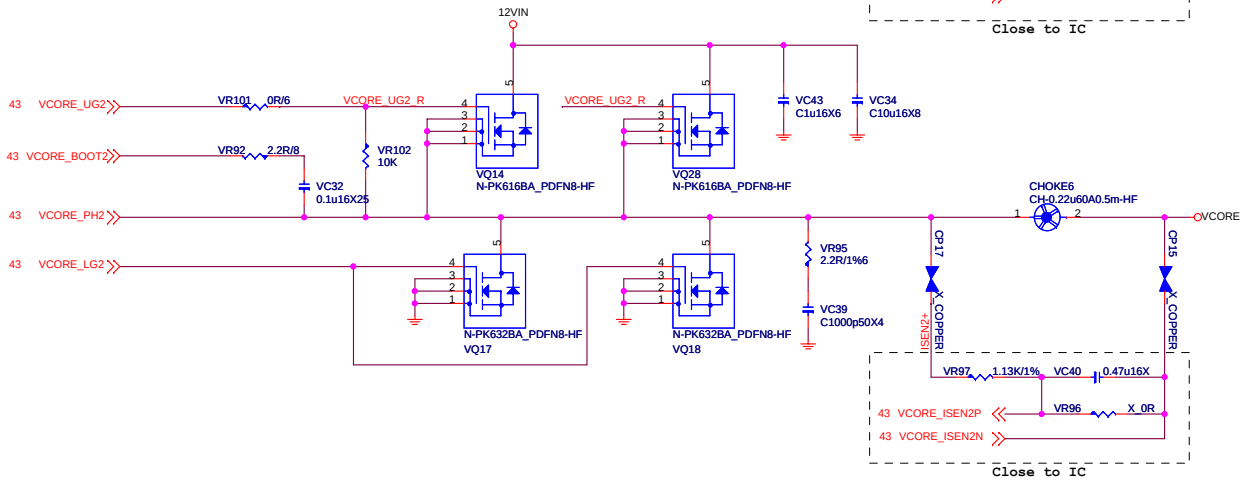
Title: CPU Power RT8894 3+2 Phase		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 43 of 55	

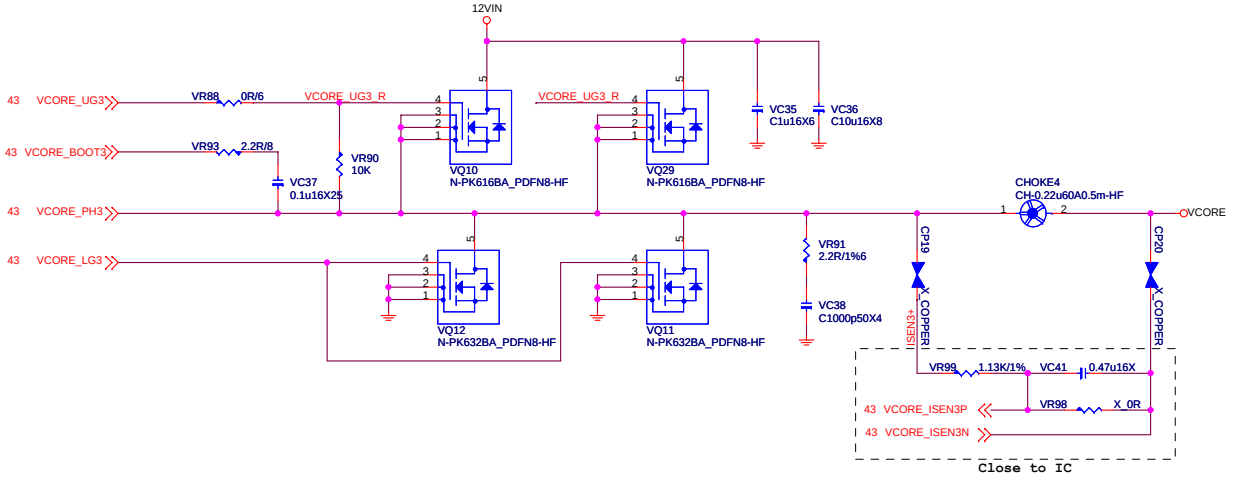
VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A



0.00625V~1.55V



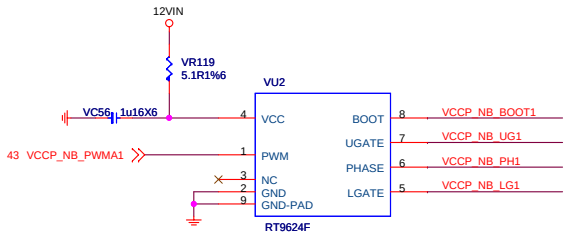


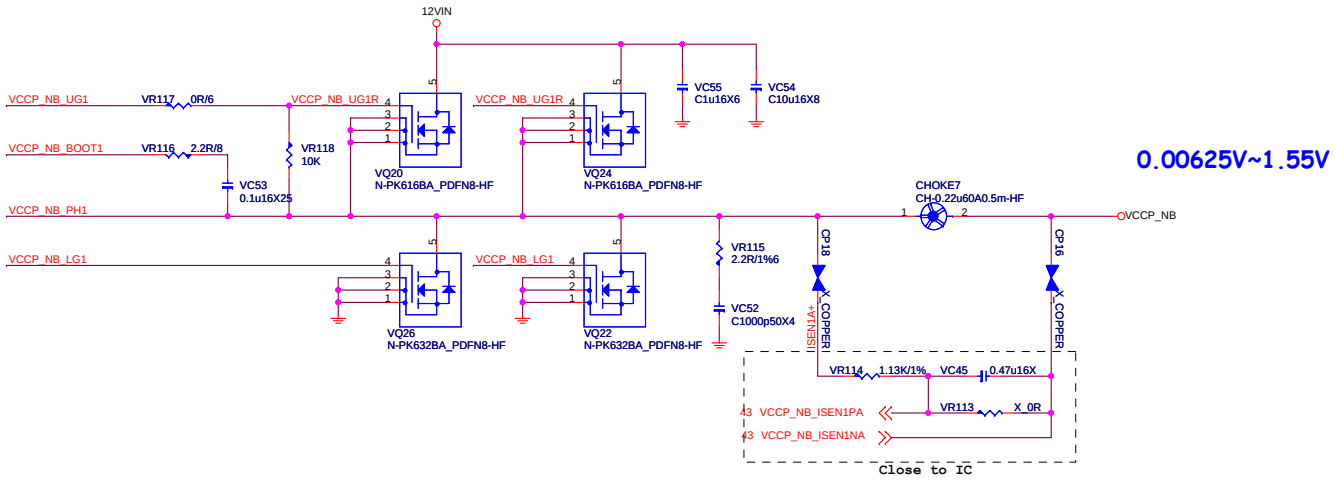


MICRO-START INT'L CO.,LTD.

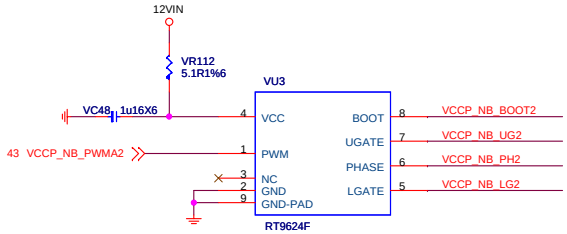
Title	CPU Power Phase 1-3	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Tuesday, January 24, 2017	Sheet 44 of 55	

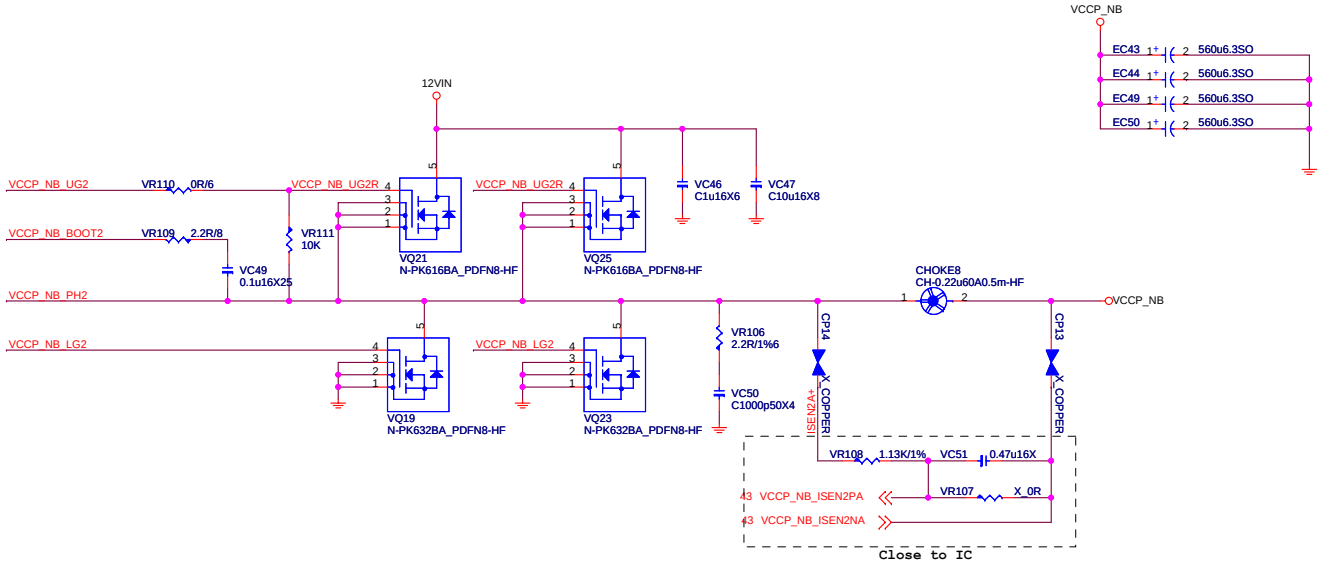
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A





0.00625V~1.55V





MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Phase 1-2		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 45 of 55	

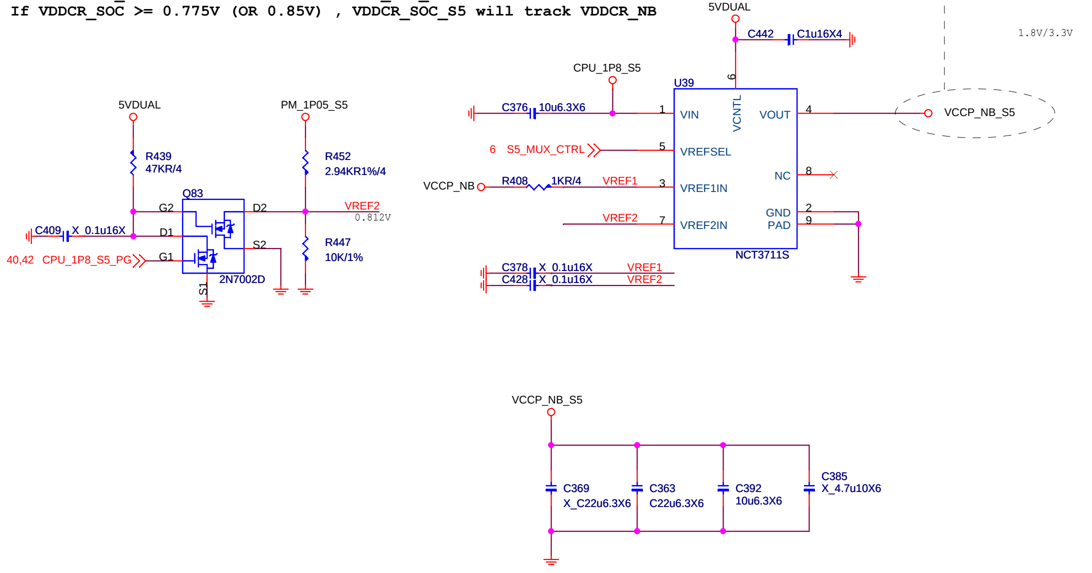
FOR VCCP_SOC_s5
0.9A

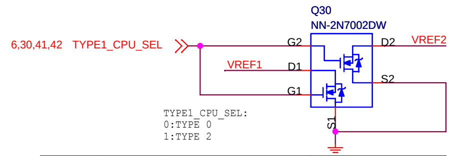
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0





CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

UPI VOLTAGE CONSOLE

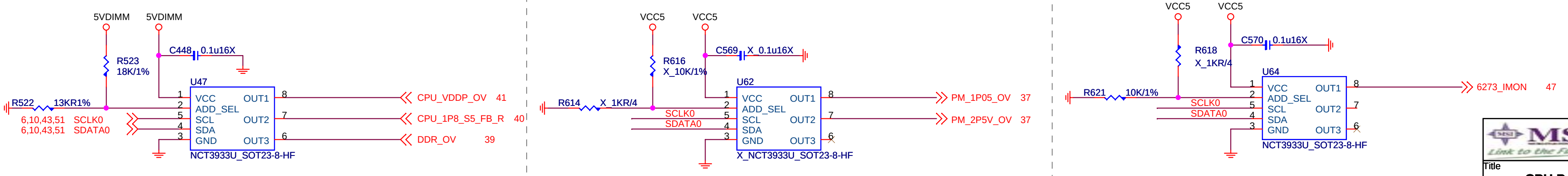
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

埃獲禬渋癸 ｒヴ：腊 ， 玥ぃ NCT3933籔柞禬渋匡兜

0x26:RH=18K,RL=13K

0x20:RH=10K,RL=OPEN

0x2A:RH=OPEN,RL=10K



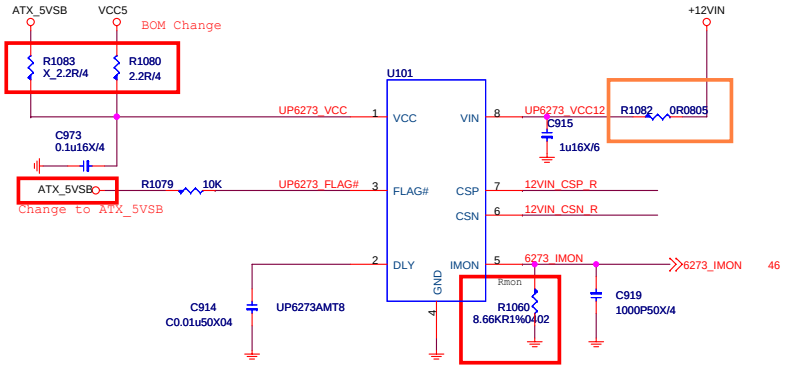
MSI Link to the Future
MICRO-START INT'L CO.,LTD.

Title	CPU Power NB Switch / NCT3933 OV	
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 46 of 55	

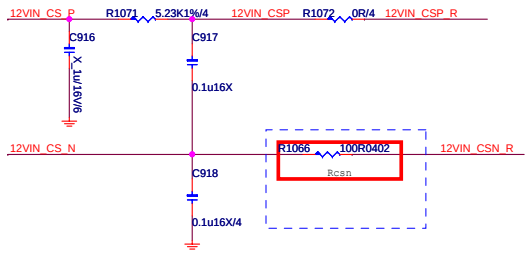
uP6273 CURRENT SENSE

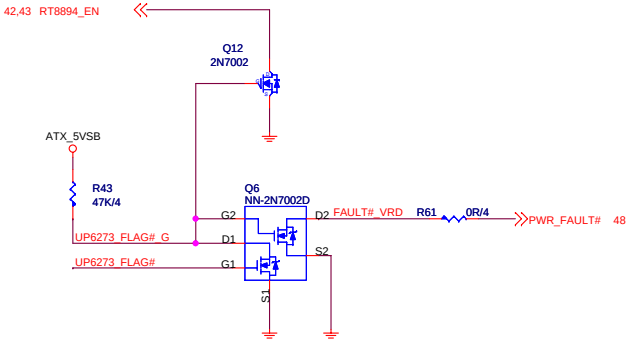
VCORE EDC MAC 125A

NB EDC MAX75A

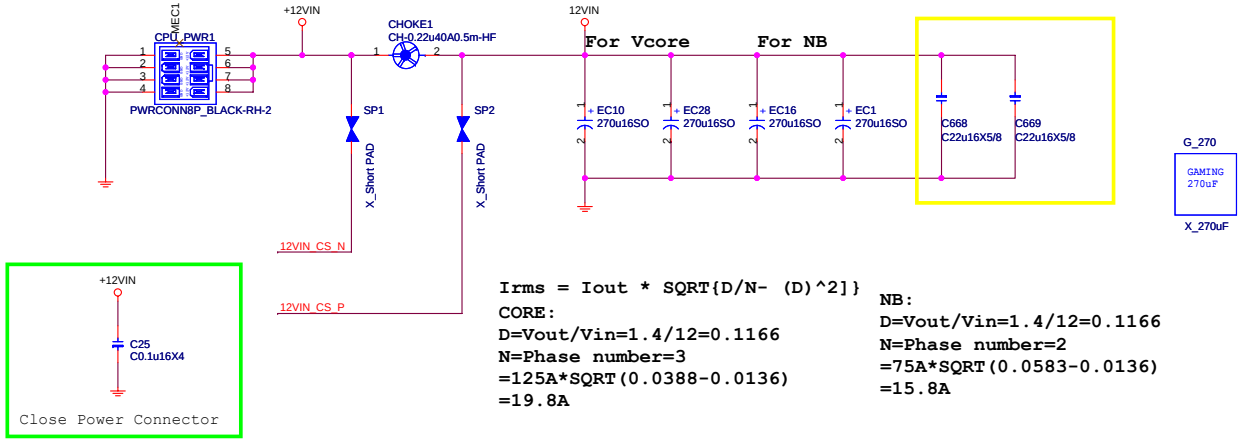


OCP = 26A(default)





CPU POWER CONNECTOR



Irms = Iout * SQRT{D/N- (D)^2]}

CORE:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=3
=125A*SQRT(0.0388-0.0136)
=19.8A

NB:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=2
=75A*SQRT(0.0583-0.0136)
=15.8A

uP6273 CURRENT SENSE

VCORE EDC MAC 125A

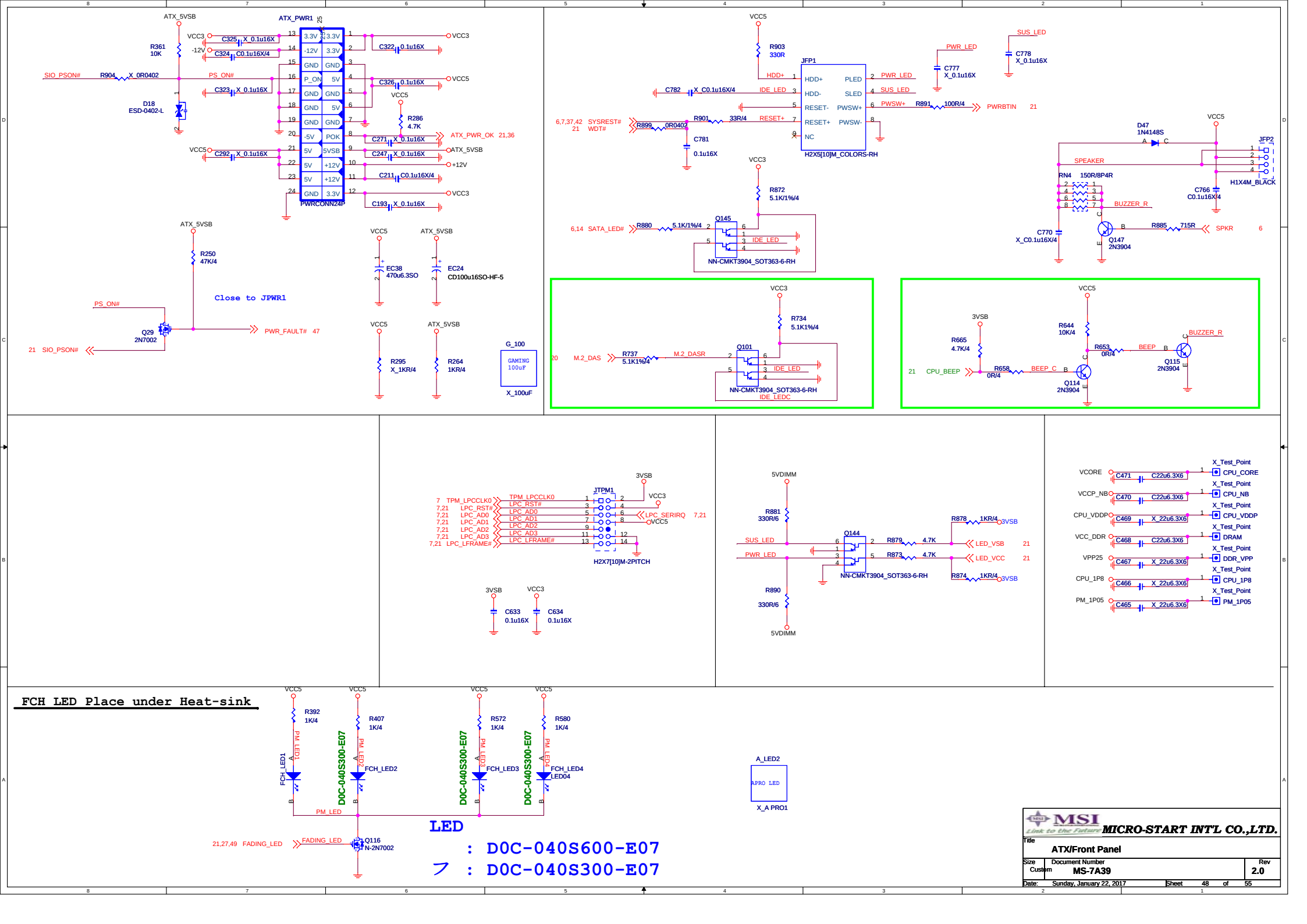
NB EDC MAX75A

MICRO-START INT'L CO.,LTD.

Title: uP6273 CURRENT SENSE

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

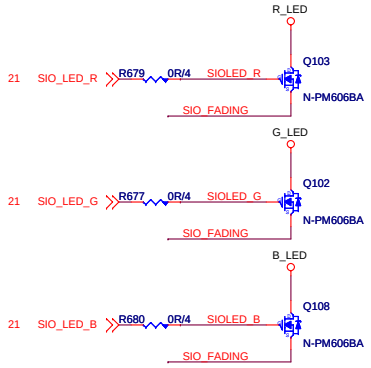
Date: Sunday, January 22, 2017 | Sheet 47 of 55



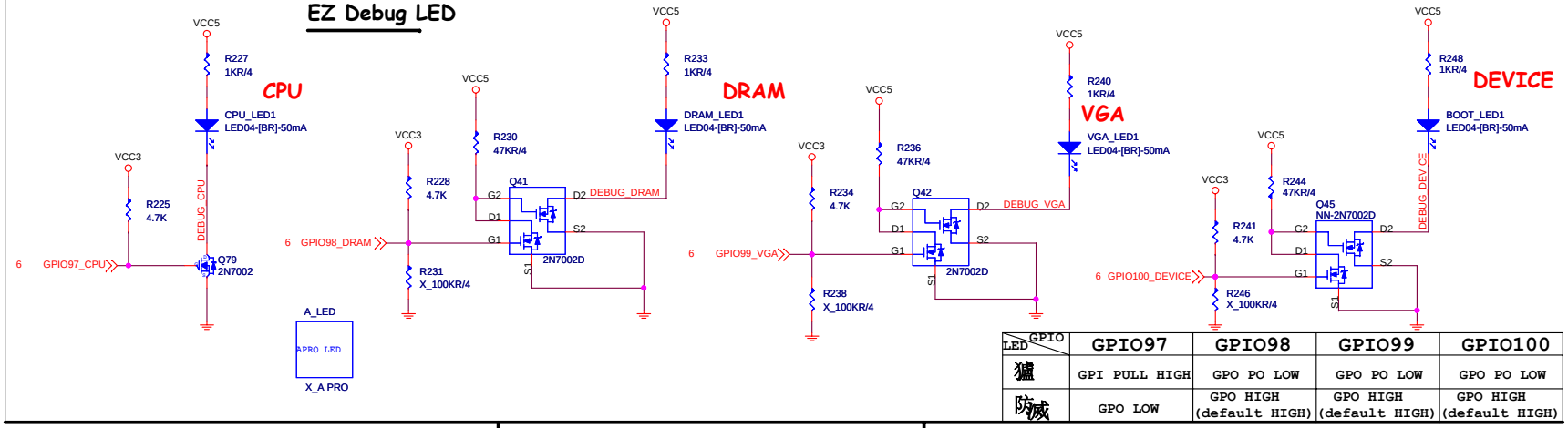
MICRO-START INT'L CO.,LTD.

Title: ATX/Front Panel		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 48 of 55	

LED Control by SIO

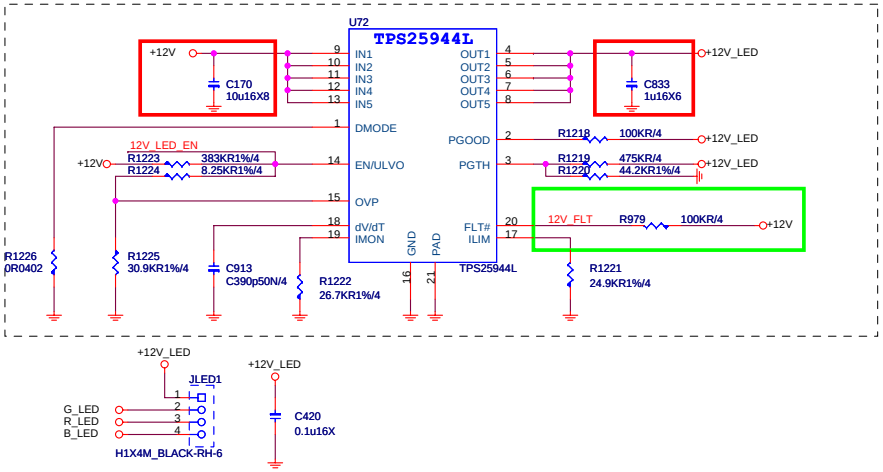


EZ Debug LED

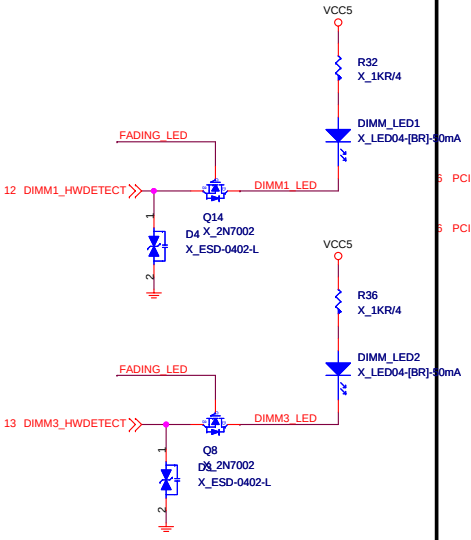


LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獨	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

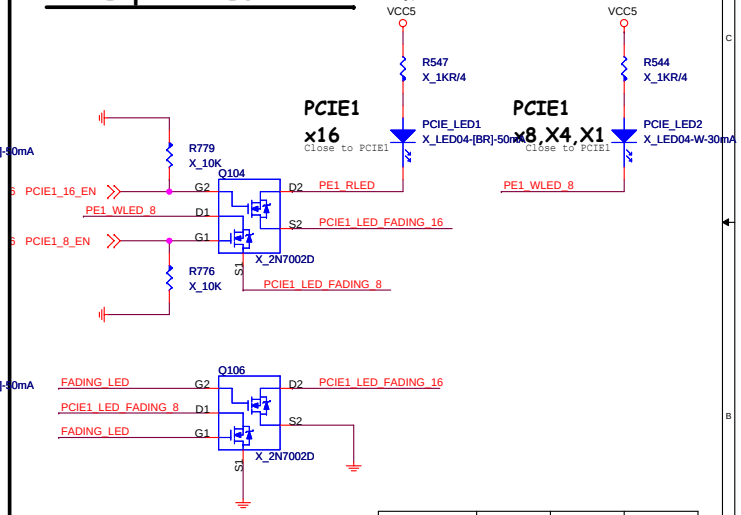
2016.07.06 Use TPS25944L



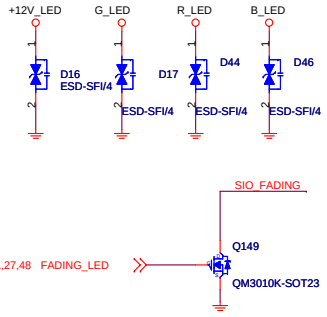
DDR LED REMOVE



PCI Express LED Control remove

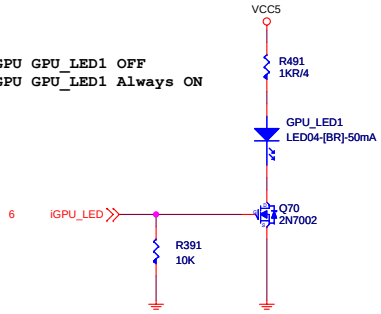


LED	x16	x8	x4
PCIE2	Red	White	White

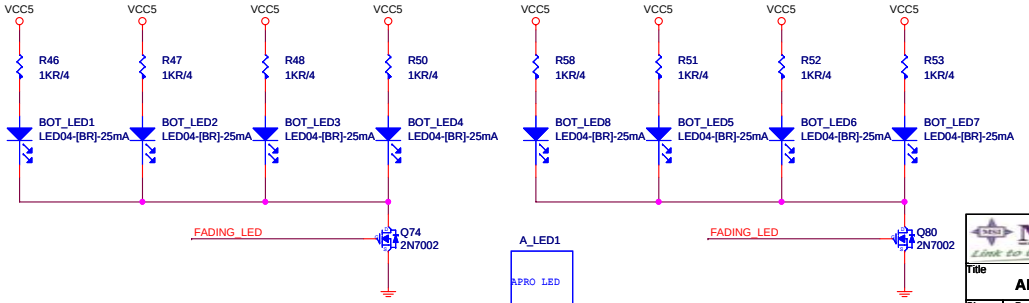


AM4 APU Detect LED Circuit

iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON



Bottom LED



LED \ GPIO	EGPIO95	EGPIO96
獨	GPO PO HIGH	GPO PO HIGH
防	GPI (default LOW)	GPI (default LOW)

MSI Link to the Future **MICRO-START INTL CO.,LTD.**

Title: ALL LED Control

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

Date: Sunday, January 22, 2017 | Sheet 49 of 55

HEAT SINK

PM_HS1
MEC2
MEC1
HS-0408790-RH

MOS_HS1
MEC2
MEC1
MOS_HS1
E31-0504740-K08

CPU Socket

CPU2
E95-0000021-C22
RETENTION MODULE

Simulation

X_JS3
SIM1
X_PIN1*2

X_JS4
SIM2
X_PIN1*2

MANUAL PART

HDMI_LA1
Y01-RHDMI03-000

SSE_LA1
X_Y02-MA00101-SSE

XSP_LA1
Y02-MA00401-XSP

CFOS_LA1
Y02-MU00170-CFO

MKT2
G51-M1SPK31-Q13

MKT1
G51-M1SPK31-Q13

BIOS_LABEL
G51-M1SPXXA-A09

REF2
APRO LED
X_REF2

PCB1
7A36-0A
PK0-07A360A-E48,腦地,腳　　吹邻紅(MSIS)
PK0-07A360A-G37,弘e-襄　,腳　　吹邻紅(MSIS)

BAT1_X1
BAT-CR2032-RH

Optics Orientation Holes

MH4
X_MH001

MH6
X_MH001

MH1
X_MH001

MH2
X_MH001

5010
FM1
FM2
X_FM120
X_FM120

5020
FM3
FM4
X_FM120
X_FM120

FM5
FM6
X_FM120
X_FM120

FM7
FM8
X_FM120
X_FM120

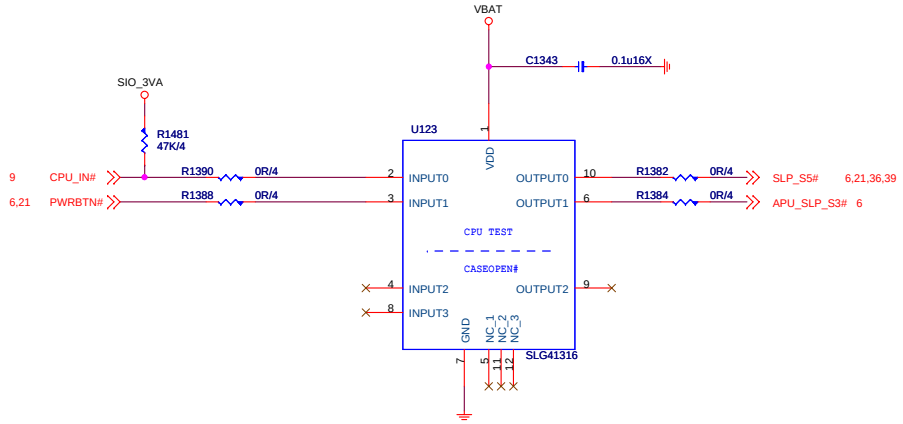
OPT	Configure	BOM	Function
		601-7A36-A01	XXXX

MSI Link to the Future MICRO-START INT'L CO.,LTD.

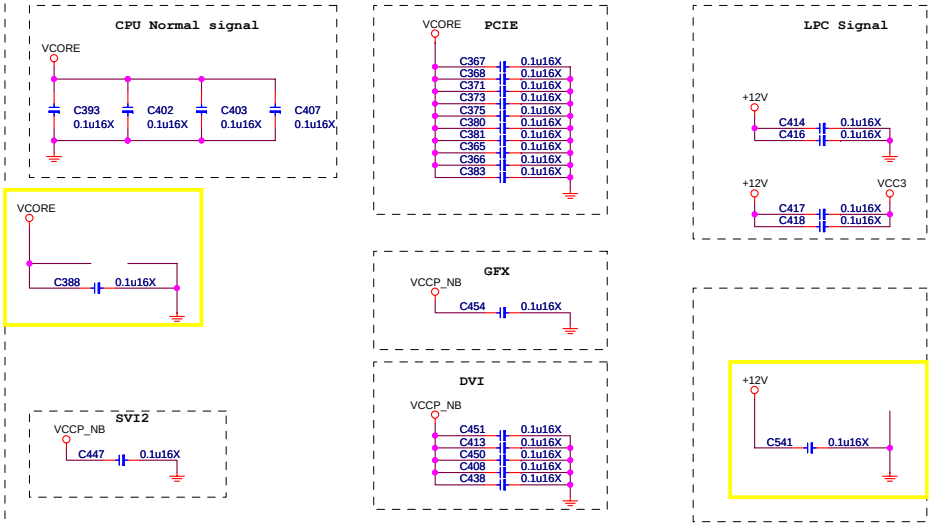
Title: BOM OPTION

Size: Custom | Document Number: MS-7A39 | Rev: 2.0

Date: Tuesday, January 24, 2017 | Sheet 50 of 55

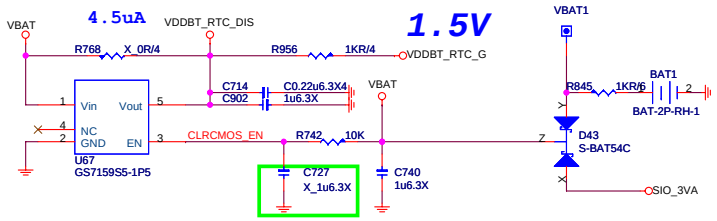


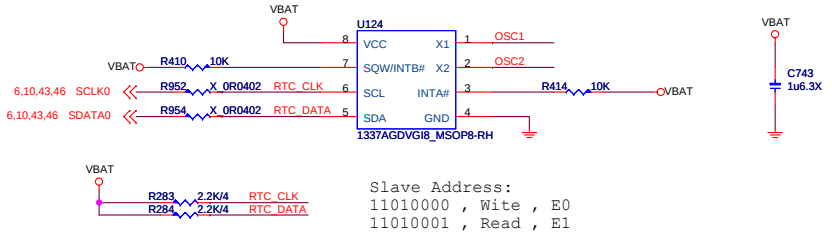
Moat Cap



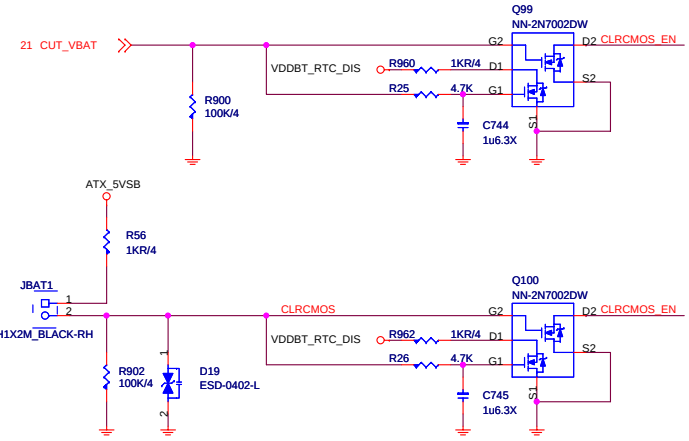
RTC & Clear CMOS Circuit

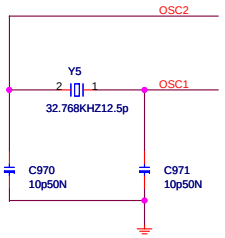
Placement Bottom Side

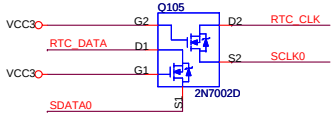




Slave Address:
11010000 , Wite , E0
11010001 , Read , E1







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Title: RTC Circuit		
Size: Custom	Document Number: MS-7A39	Rev: 2.0
Date: Sunday, January 22, 2017	Sheet 51 of 55	