MS-7A38 Ver:6.0

CPU:
AMD AM4

System Chipset:
Promontory B350/A320
(Value DIY or System Builder)

Main Memory:
DDR IV * 4   MAX:64 GB

VRM
RT8894 4+2

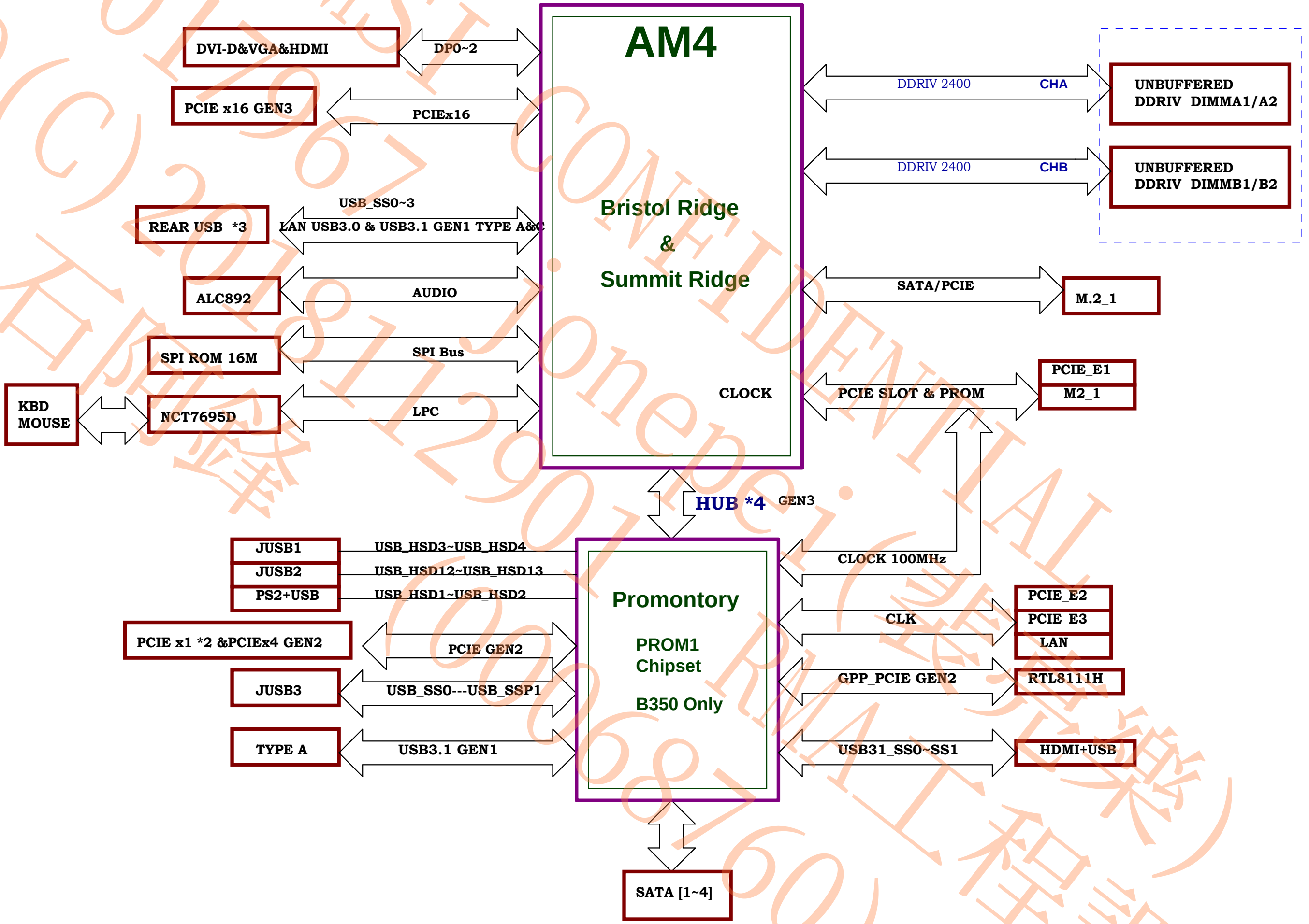
On Board Chipset:
LPC Super I/O --NCT6795D
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

OCP IC:

UP6273

FUSION BLOCK DIAGRAM



MSI MICRO-START INT'L CO.,LTD.		
Title: Block Diagram		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
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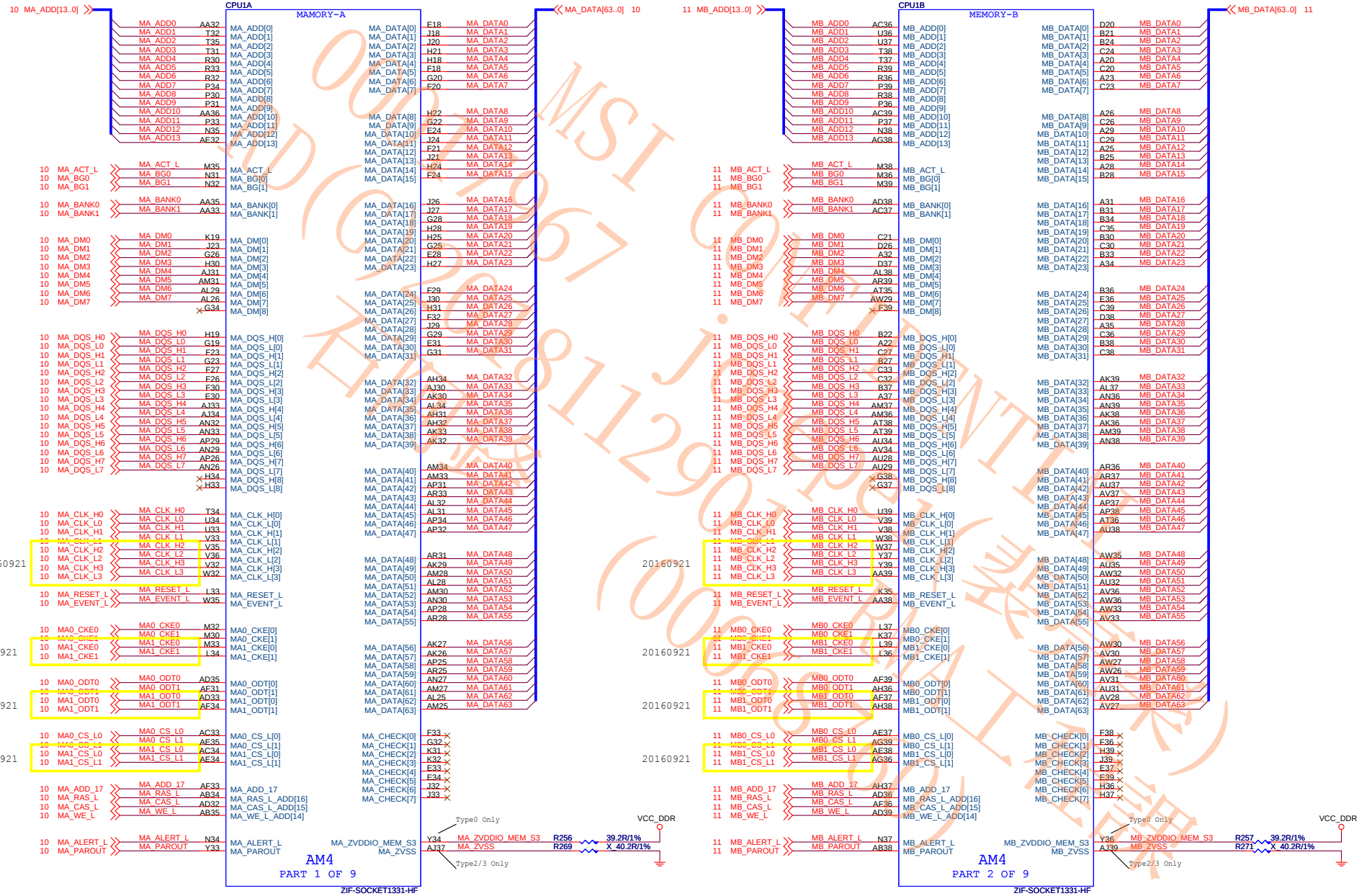
AMD AM4

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: COVER SHEET		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 2 of 60	



N12-331A030-L06

N12-331A030-L06

MICRO-START INTL CO.,LTD.		
Title: AM4 DDR4 I/F		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
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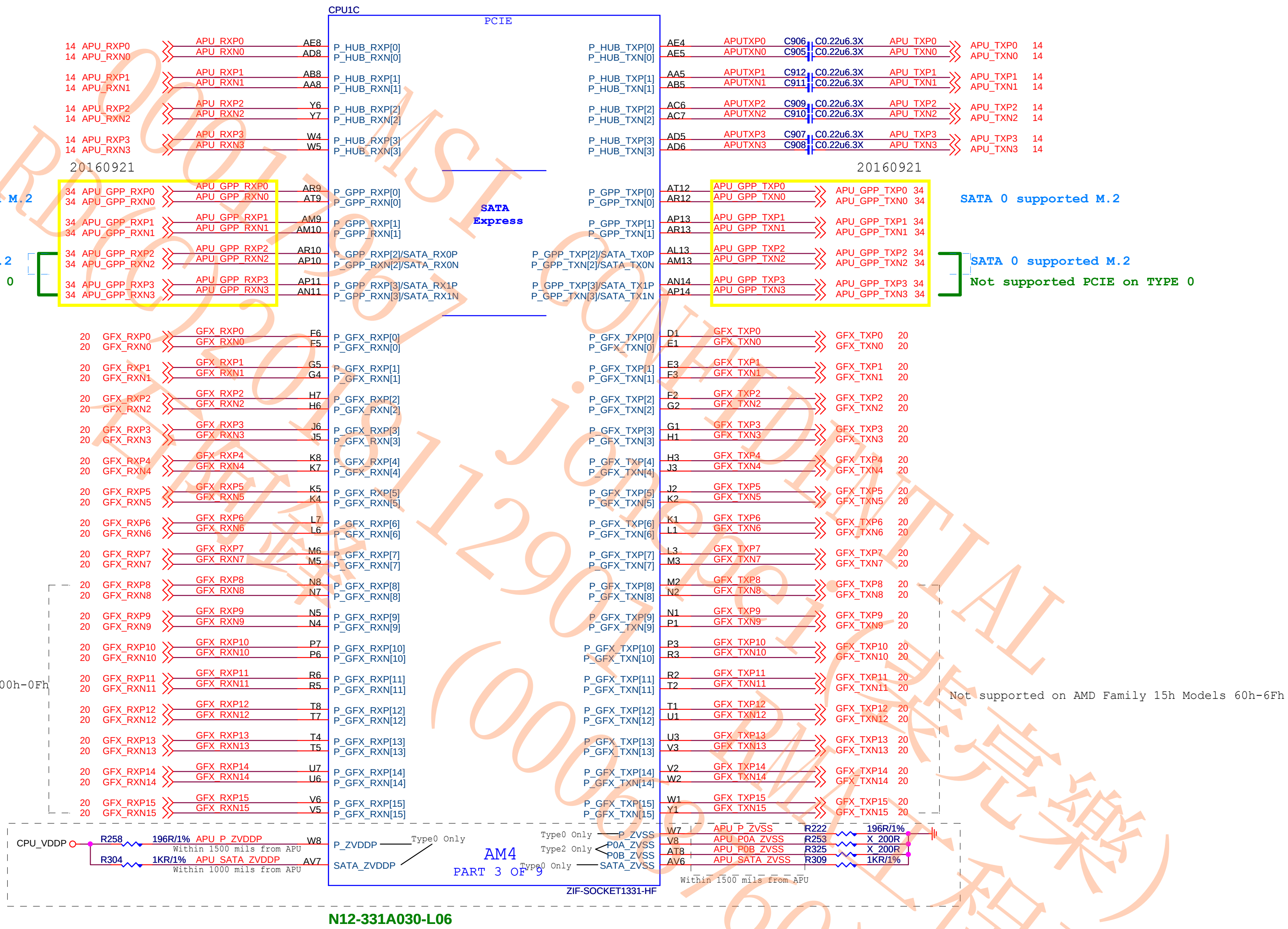
SATA 0 supported M.2

SATA 0 supported M.2
Not supported PCIE on TYPE 0

	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

Only supported on AMD Family 17h/Models 00h-0Fh



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	AM4 PCIE/SATAE
Size	Custom
Document Number	MS-7A38
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Date:	Wednesday, September 26, 2018
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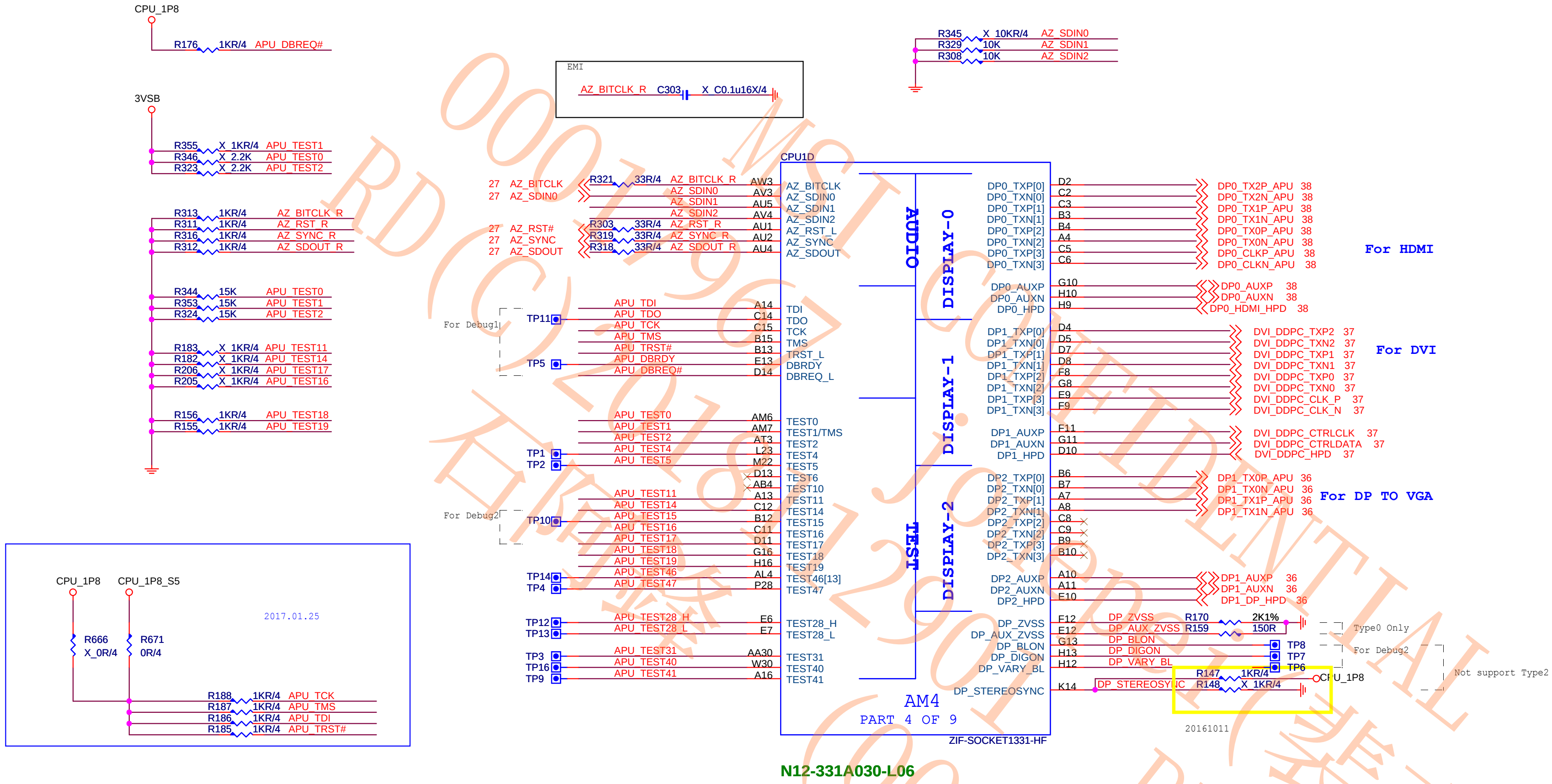
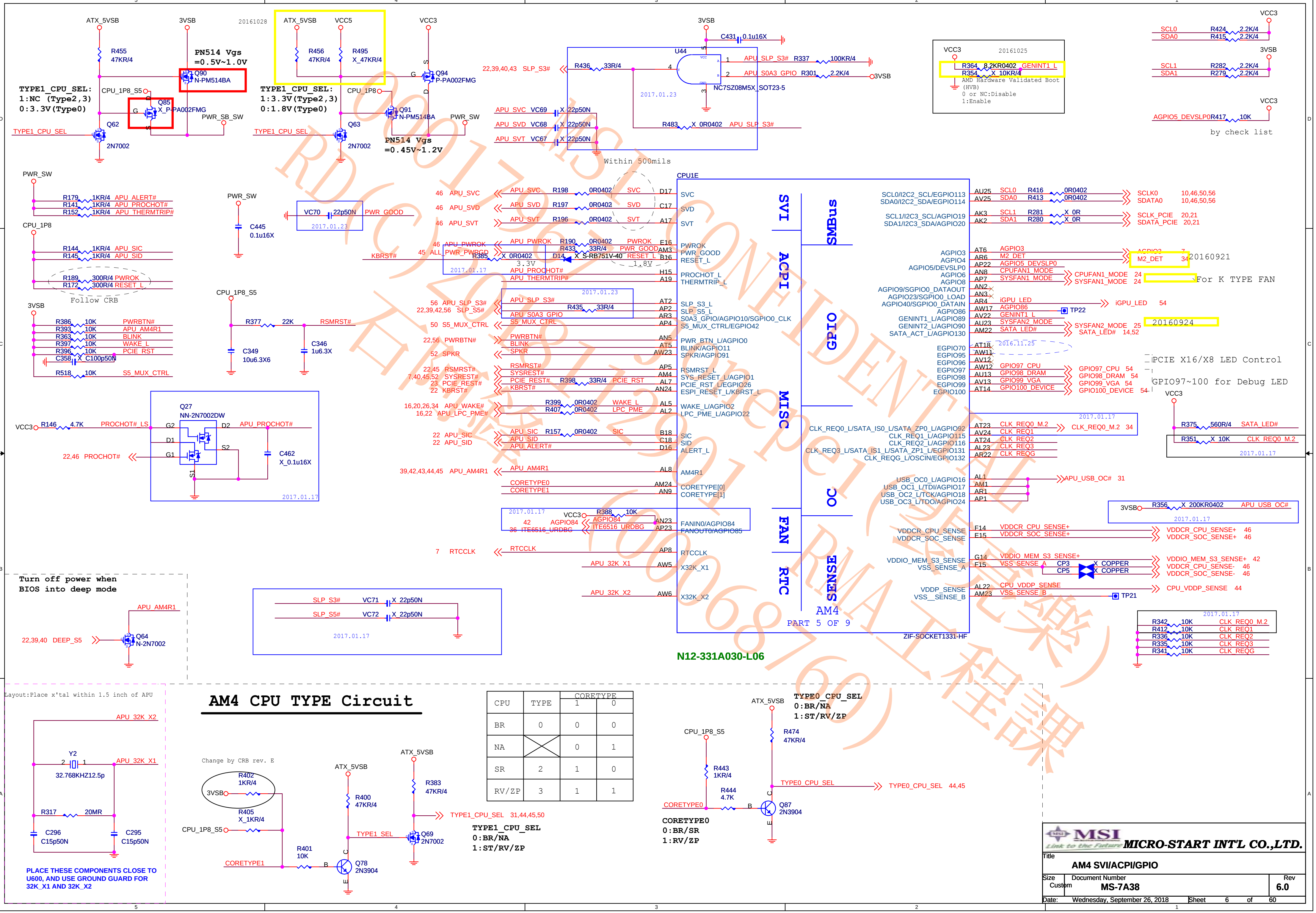


MSI MICRO-START INT'L CO.,LTD.		
Title	AM4 DISPLAY/AUDIO	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 5 of 60	



AM4 CPU TYPE Circuit

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: AM4 SVI/ACPI/GPIO

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

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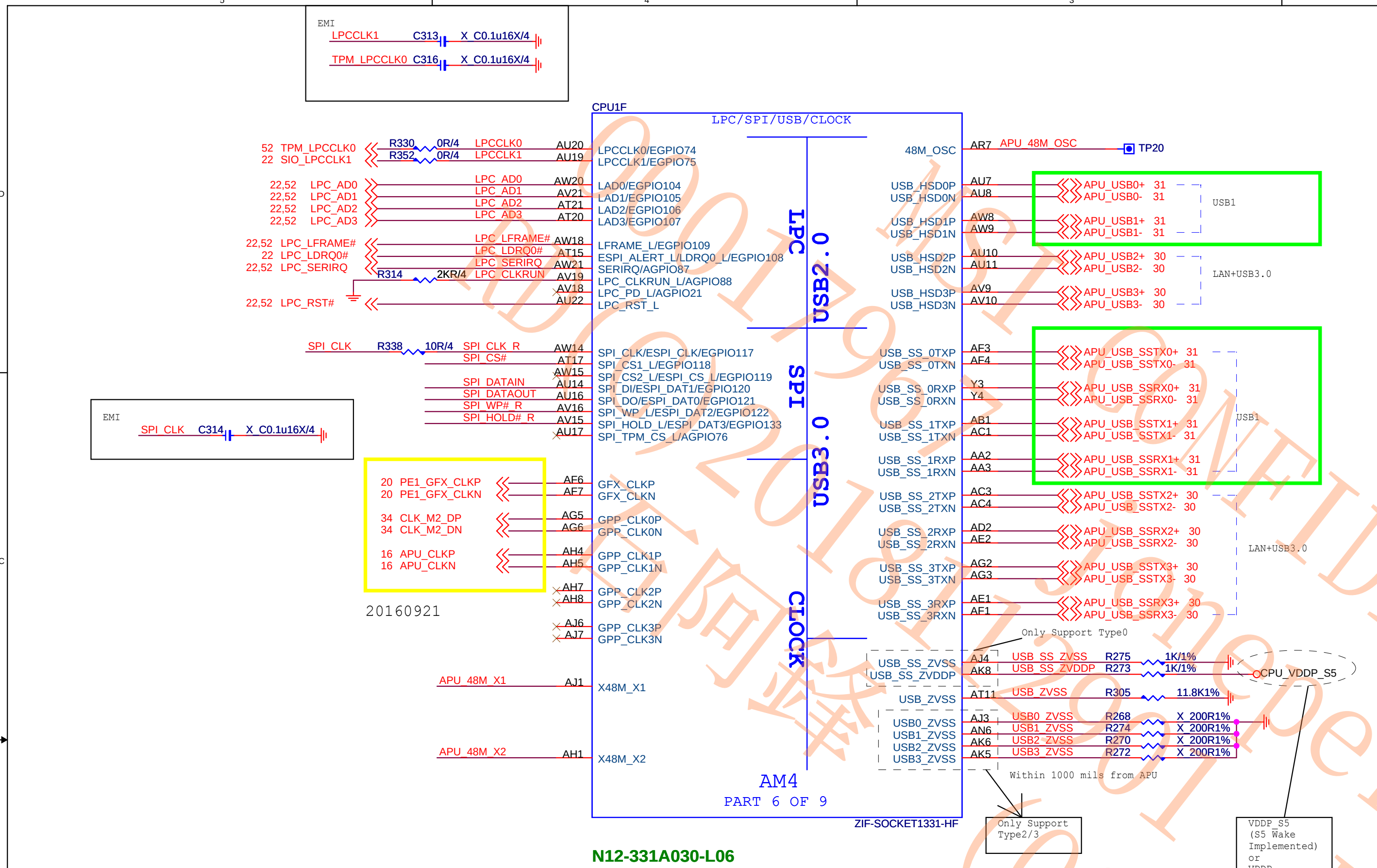
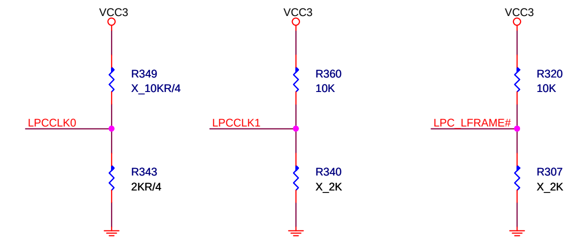
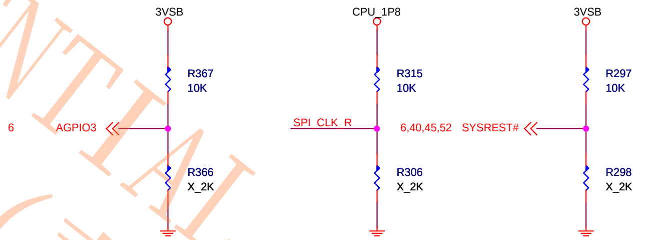
Strapping Options



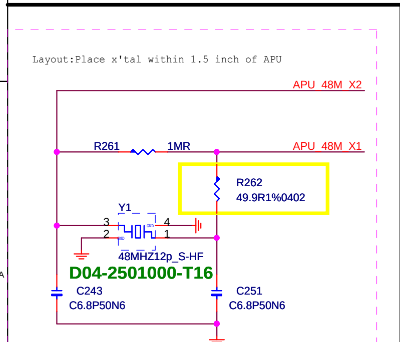
N12-331A030-L06



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ?????	LPC ROM

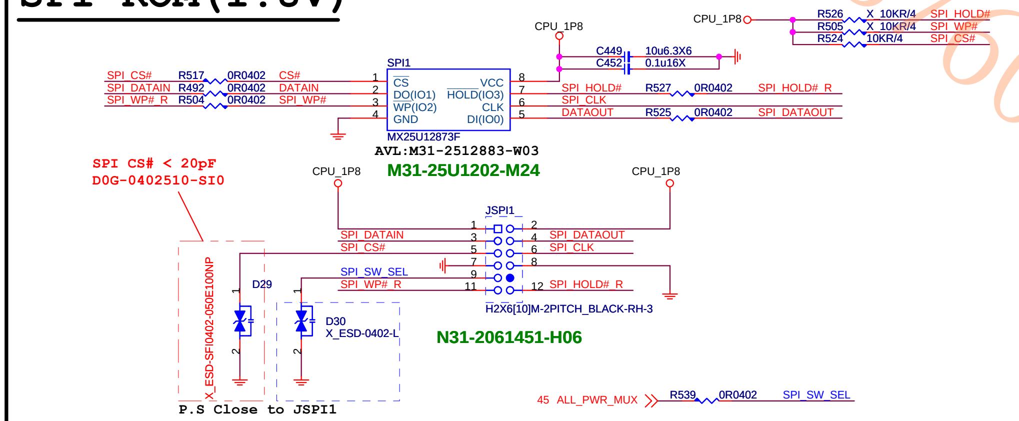


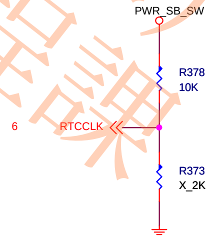
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

SPI ROM(1.8V)





	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

MICRO-START INT'L CO.,LTD.

Title	AM4 LPC/SPI/USB/CLK/STRAP
Size	Custom
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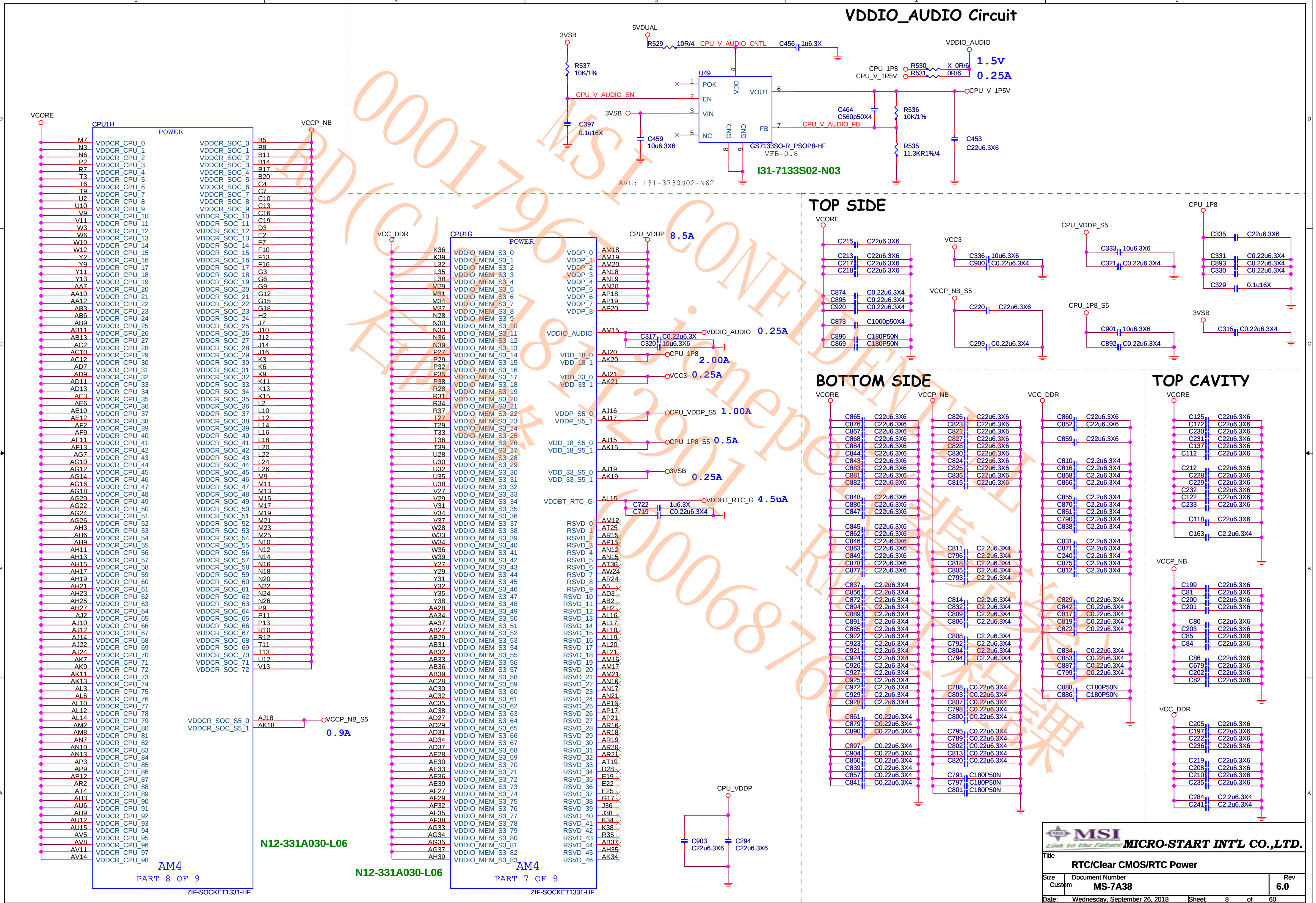
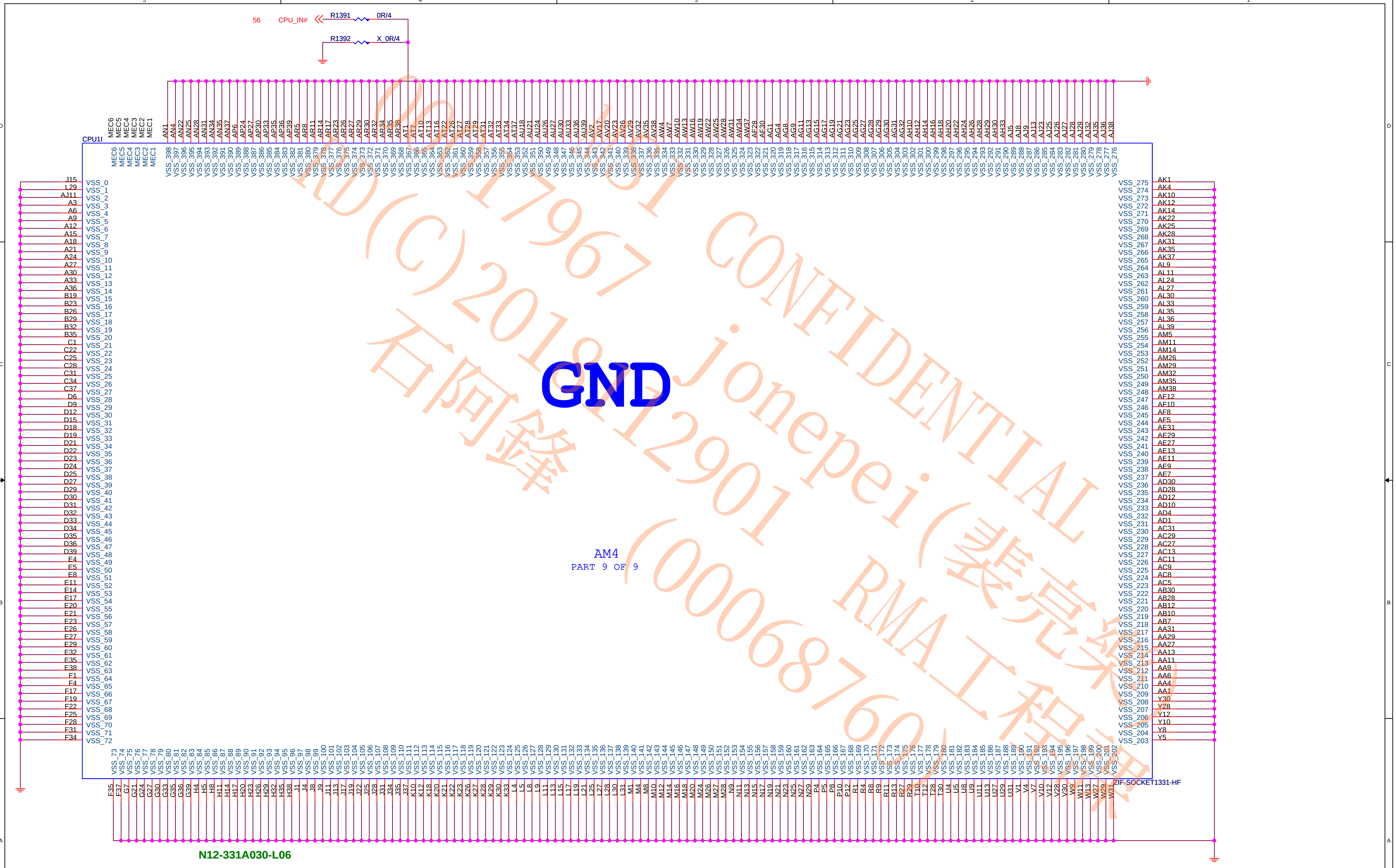


MSI *Link to the Future*

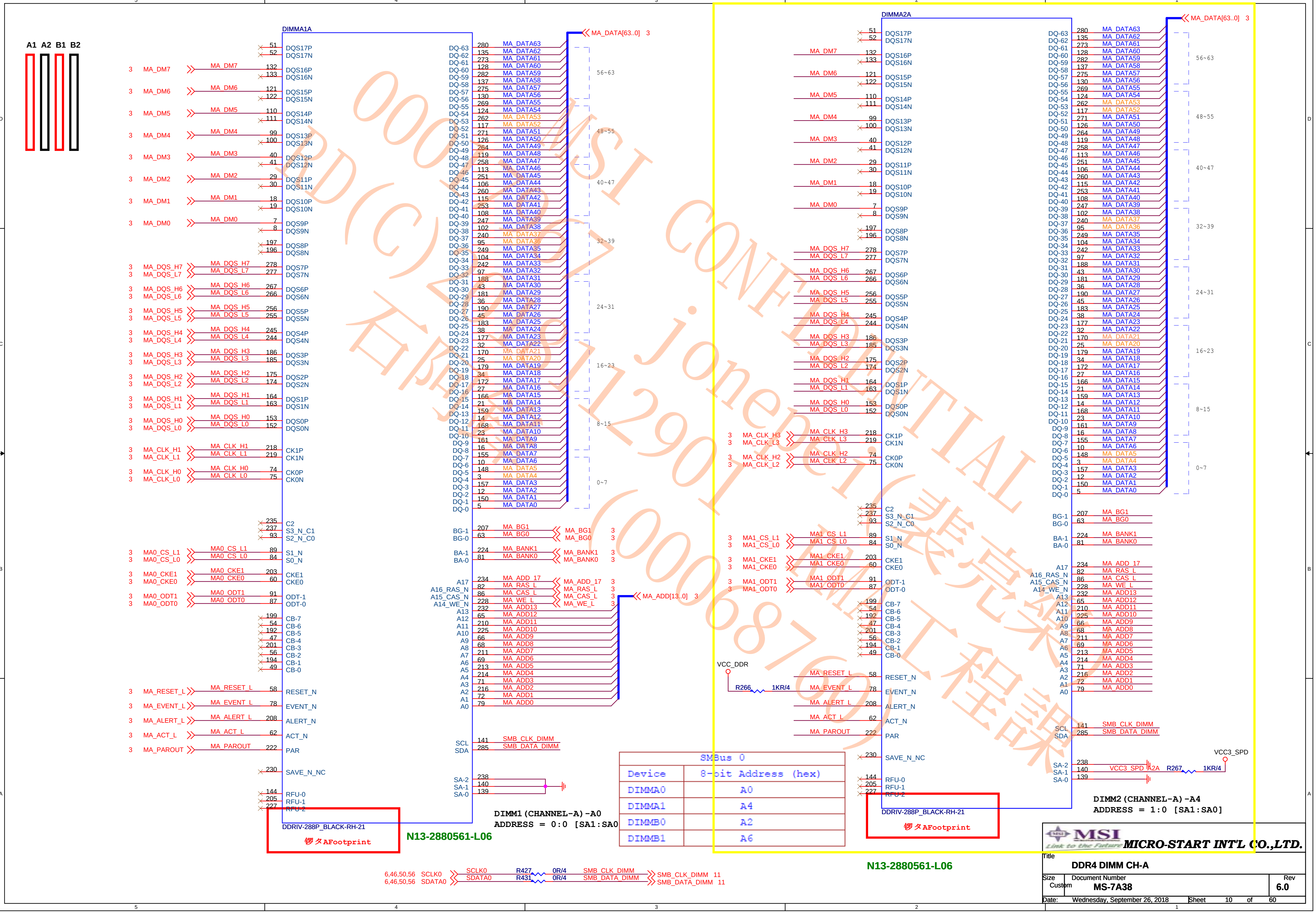
MICRO-START INT'L CO.,LTD.

Title	RTC/Clear CMOS/RTC Power	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 8 of 60	



MSI
MICRO-START INT'L CO.,LTD.

Title: AM4 GND		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 9 of 60	



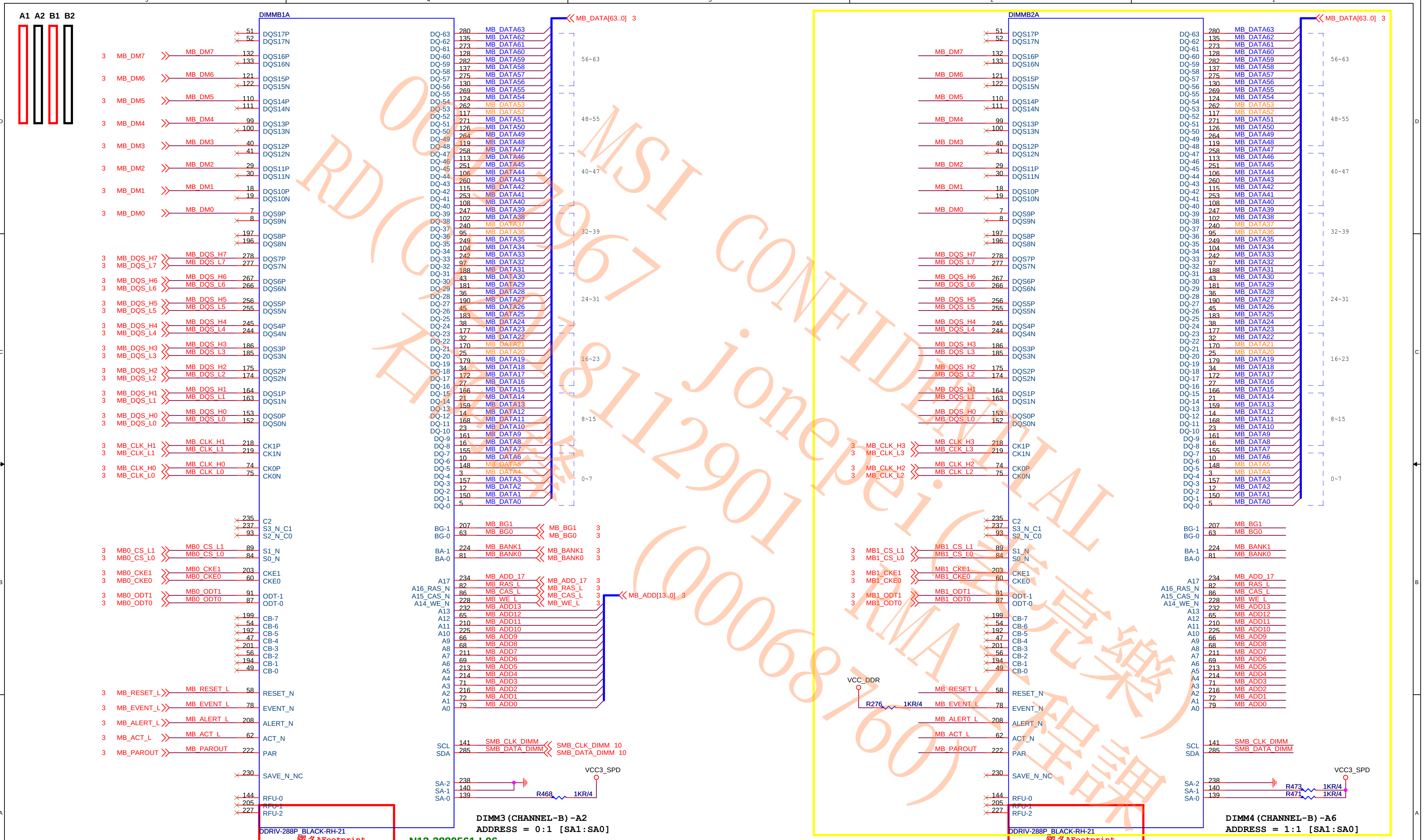
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

MSI MICRO-START INT'L CO.,LTD.

Title: DDR4 DIMM CH-A

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

Date: Wednesday, September 26, 2018 | Sheet 10 of 60



MSI
MICRO-START INT'L CO.,LTD.

Title: DDR4 DIMM CH-B

Size	Document Number	Rev
Custom	MS-7A38	6.0

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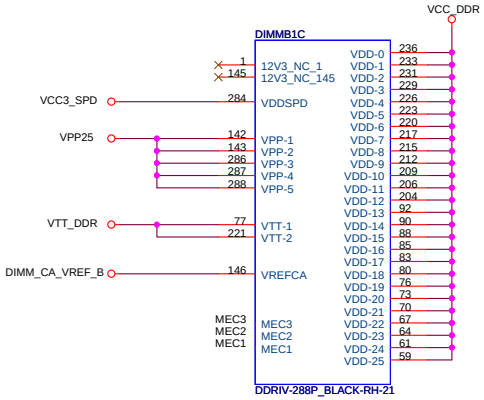
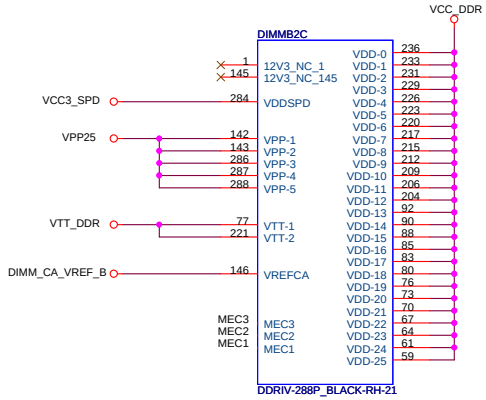
MSI MICRO-START INTL CO.,LTD.			
Title: DDR4-POWER/GND-1			
Size: Custom	Document Number: MS-7A38		Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 12 of 60		



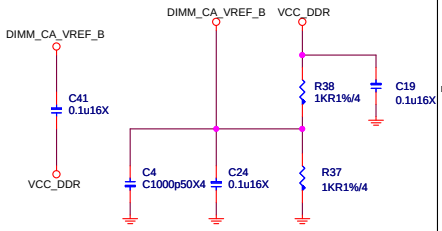
N13-2880561-L06

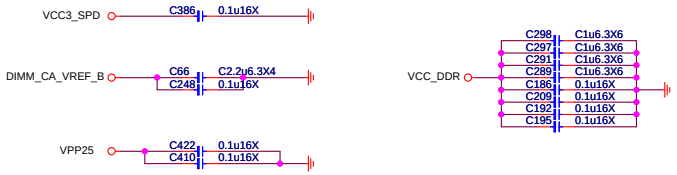


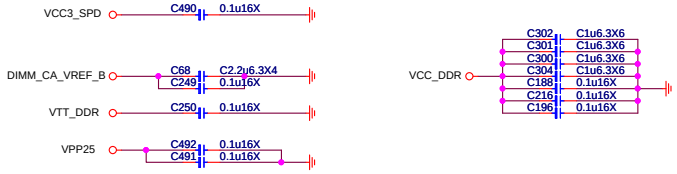
N13-2880561-L06

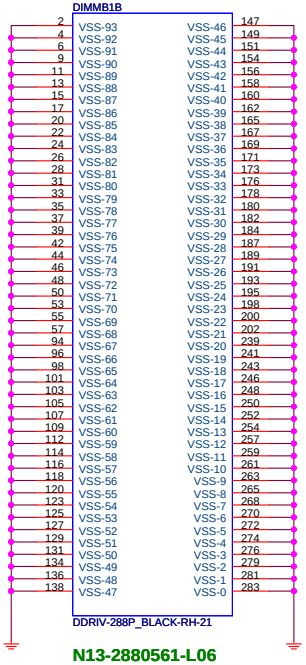
DDR VREF

(place resistors close to DIMMs)

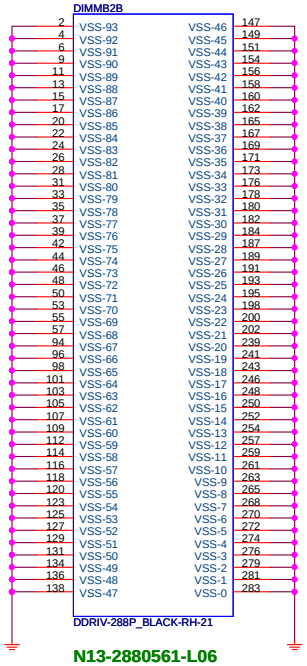








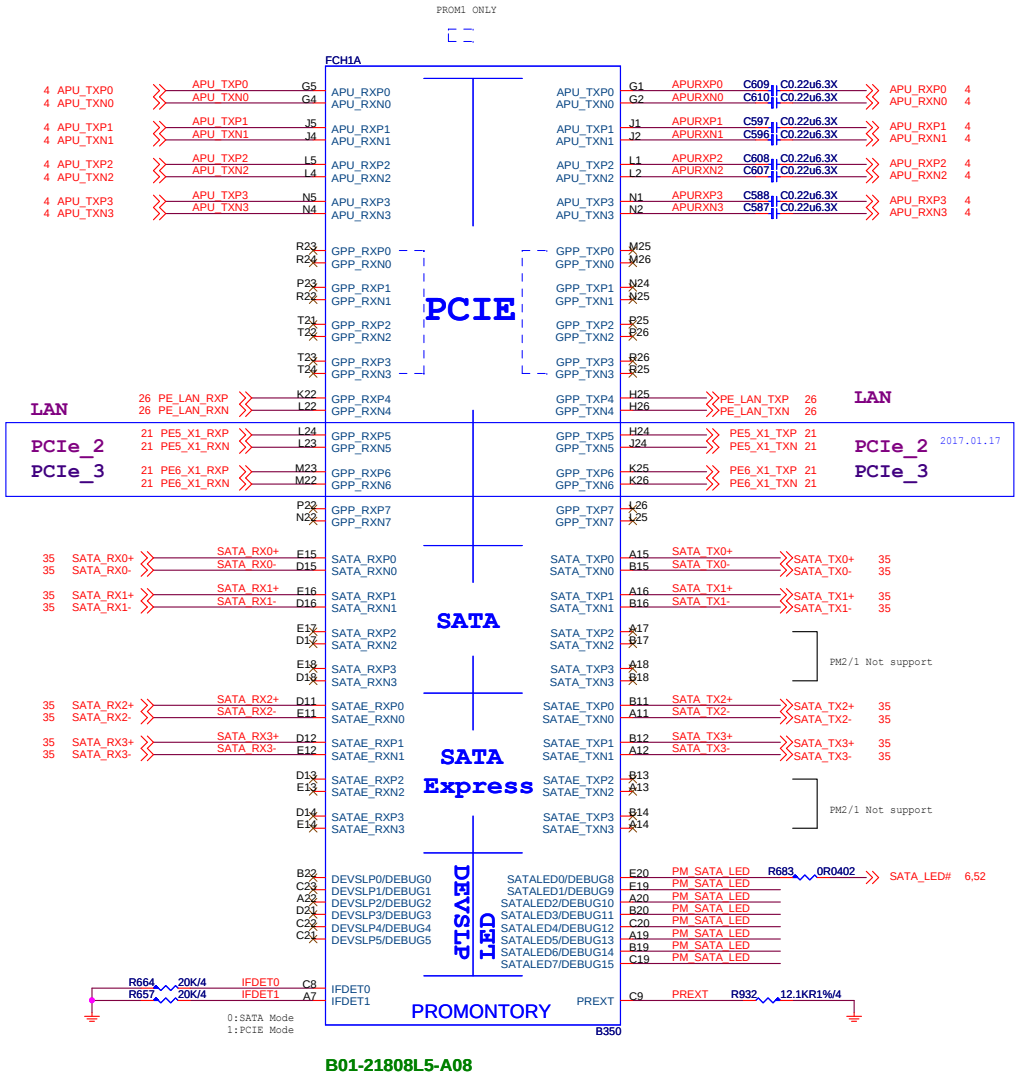
N13-2880561-L06



N13-2880561-L06

MSI MICRO-START INT'L CO.,LTD.

Title: DDR4-POWER/GND-2		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 13 of 60	



B01-21808L5-A08

MICRO-START INT'L CO.,LTD.	
Title	Promontory-PCIE/SATA/SATAE
Size: Custom	Document Number: MS-7A38
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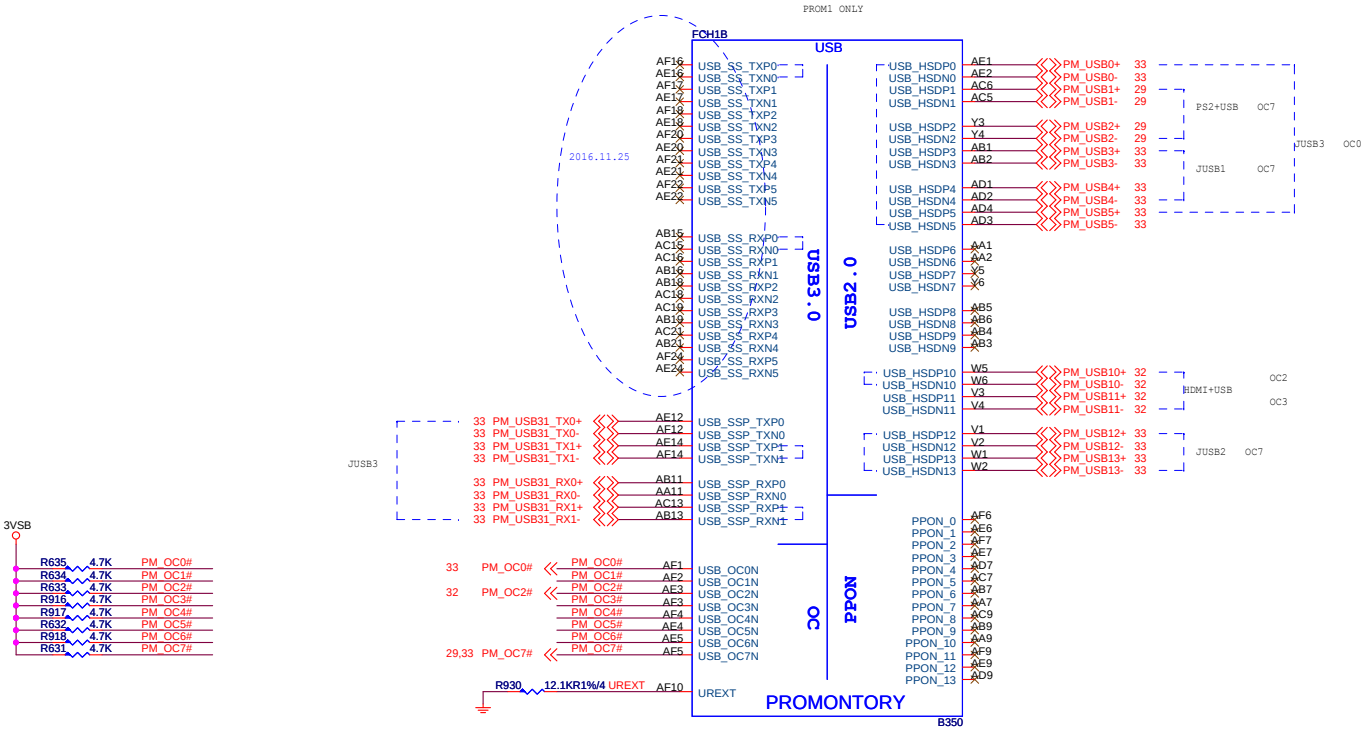
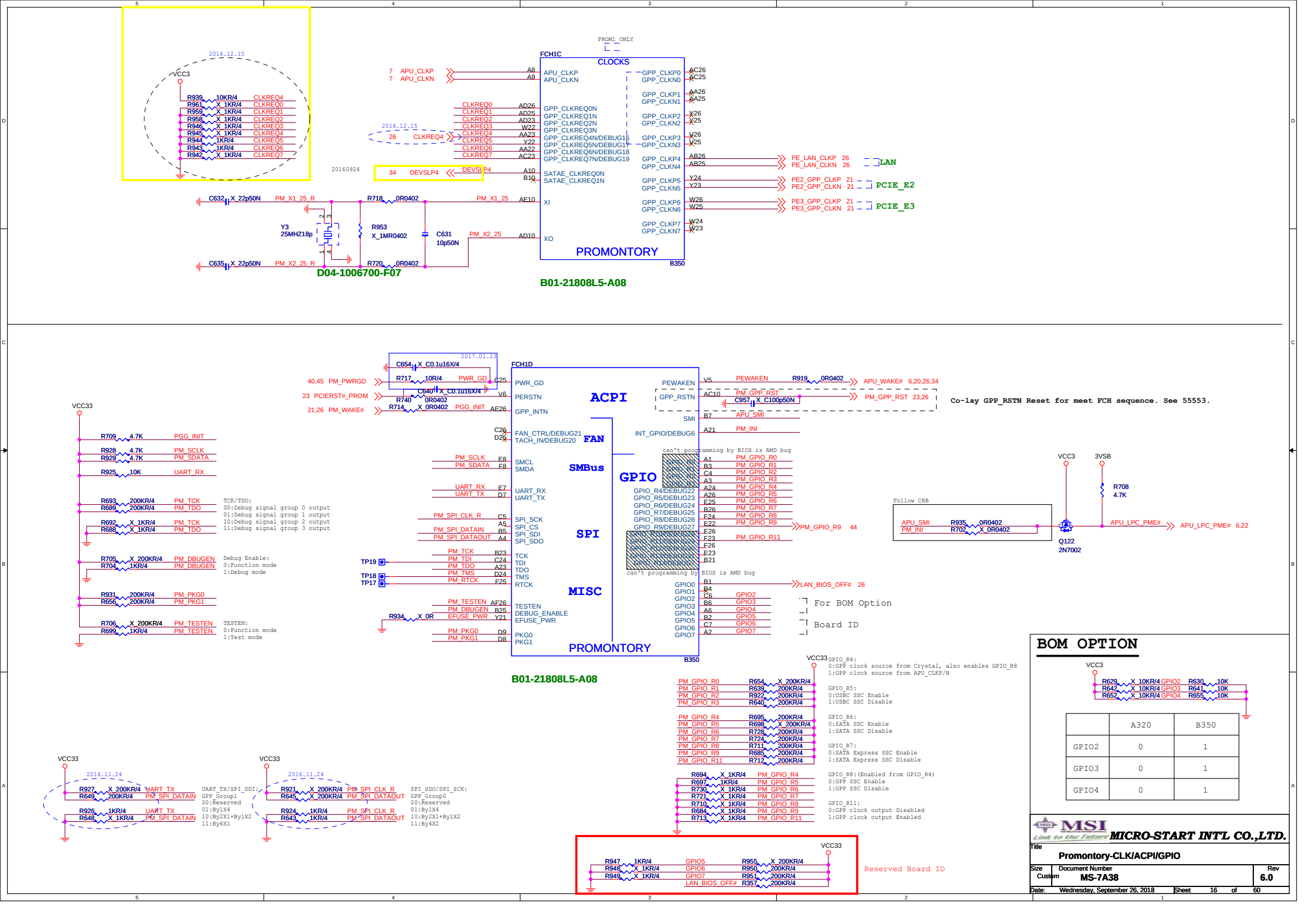
Date: Wednesday, September 26, 2018	Sheet 14 of 60



B01-21808L5-A08

MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title: Promontory-USB/OC		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 15 of 60	


2016.12.15
VCC3
R939 10KR/4 CLKREQ4
R961 X_1KR/4 CLKREQ0
R959 X_1KR/4 CLKREQ1
R958 X_1KR/4 CLKREQ2
R946 X_1KR/4 CLKREQ3
R945 X_1KR/4 CLKREQ4
R944 1KR/4 CLKREQ5
R943 1KR/4 CLKREQ6
R942 X_1KR/4 CLKREQ7
PROM1_ONLY
FCH1C
CLOCKS
7 APU_CLKP
7 APU_CLKN
APU_CLKP
APU_CLKN
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
CLKREQ0
CLKREQ1
CLKREQ2
CLKREQ3
CLKREQ4
CLKREQ5
CLKREQ6
CLKREQ7
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEBUG16
GPP_CLKREQ5N/DEBUG17
GPP_CLKREQ6N/DEBUG18
GPP_CLKREQ7N/DEBUG19
2016.12.15
26 CLKREQ4
20160924
34 DEVSLP4
DEVSLP4
SATAE_CLKREQ0N
SATAE_CLKREQ1N
PE_LAN_CLKP 26
PE_LAN_CLKN 26
LAN
PE2_GPP_CLKP 21
PE2_GPP_CLKN 21
PCIE_E2
PE3_GPP_CLKP 21
PE3_GPP_CLKN 21
PCIE_E3
C632 X_22p50N PM_X1_25_R
R718 0R0402 PM_X1_25
XI
Y3
25MHZ18p
R953
X_1MR0402
C631
10p50N
PM_X2_25
XO
C635 X_22p50N PM_X2_25_R
R720 0R0402
PROMONTORY
B350
D04-1006700-F07
B01-21808L5-A08
2017.01.23
C654 X_C0.1u16X/4
R717 10R/4 PWR_GD
C640 X_C0.1016X/4
R740 0R0402
R714 X_0R0402 PGG_INIT
40,45 PM_PWRGD
23 PCIERST#_PROM
21,26 PM_WAKE#
FCH1D
ACPI
PWR_GD
PERSTN
GPP_INTN
PEWAKEN
GPP_RSTN
SMI
INT_GPIO/DEBUG6
FAN
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMBus
SMCL
SMDA
GPIO
SPI
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
MISC
TCK
TDI
TDO
TMS
RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PKG0
PKG1
PROMONTORY
B350
V5 PEWAKEN
R919 0R0402
APU_WAKE# 6,20,26,34
AC10 PM_GPP_RST
C957 X_C100p50N
PM_GPP_RST 23,26
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
B7 APU_SMI
A21 PM_INI
can't programming by BIOS is AMD bug
GPIO_R4/DEBUG22
GPIO_R5/DEBUG23
GPIO_R6/DEBUG24
GPIO_R7/DEBUG25
GPIO_R8/DEBUG26
GPIO_R9/DEBUG27
PM_GPIO_R9 44
PM_GPIO_R11
can't programming by BIOS is AMD bug
LAN_BIOS_OFF# 26
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
For BOM Option
Board ID
PM_SCLK
PM_SDATA
UART_RX
UART_TX
PM_SPI_CLK_R
PM_SPI_DATAIN
PM_SPI_DATAOUT
PM_TCK
PM_TDI
PM_TDO
PM_TMS
PM_RTCK
PM_TESTEN
PM_DBUGEN
EFUSE_PWR
PM_PKG0
PM_PKG1
TP19
TP18
TP17
R934 X_0R
VCC33
R709 4.7K PGG_INIT
R928 4.7K PM_SCLK
R929 4.7K PM_SDATA
R925 10K UART_RX
R693 200KR/4 PM_TCK
R689 200KR/4 PM_TDO
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
R692 X_1KR/4 PM_TCK
R688 X_1KR/4 PM_TDO
R705 X_200KR/4 PM_DBUGEN
R704 1KR/4 PM_DBUGEN
Debug Enable:
0:Function mode
1:Debug mode
R931 200KR/4 PM_PKG0
R656 200KR/4 PM_PKG1
R706 X_200KR/4 PM_TESTEN
R699 1KR/4 PM_TESTEN
TESTEN:
0:Function mode
1:Test mode
Follow CRB
APU_SMI
PM_INI
R935 0R0402
R702 X_0R0402
Q122
2N7002
VCC3
3VSB
R708
4.7K
APU_LPC_PME#
APU_LPC_PME# 6,22
PM_GPIO_R0
PM_GPIO_R1
PM_GPIO_R2
PM_GPIO_R3
PM_GPIO_R4
PM_GPIO_R5
PM_GPIO_R6
PM_GPIO_R7
PM_GPIO_R8
PM_GPIO_R9
PM_GPIO_R11
R654 X_200KR/4
R639 200KR/4
R922 200KR/4
R640 200KR/4
R695 200KR/4
R698 X_200KR/4
R728 200KR/4
R724 200KR/4
R711 200KR/4
R685 200KR/4
R712 200KR/4
GPIO_R4:
0:GPP clock source from Crystal, also enables GPIO_R8
1:GPP clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
R694 X_1KR/4
R697 1KR/4
R730 X_1KR/4
R721 X_1KR/4
R710 X_1KR/4
R684 X_1KR/4
R713 X_1KR/4
R947 1KR/4 GPIO5
R948 X_1KR/4 GPIO6
R949 X_1KR/4 GPIO7
R955 X_200KR/4
R950 200KR/4
R951 200KR/4
R357 200KR/4
LAN_BIOS_OFF#
Reserved Board ID
BOM OPTION
R629 X_10KR/4 GPIO2
R642 X_10KR/4 GPIO3
R652 X_10KR/4 GPIO4
R630 10K
R641 10K
R655 10K
A320
B350
GPIO2 0 1
GPIO3 0 1
GPIO4 0 1
2016.11.24
R927 X_200KR/4 UART_TX
R649 200KR/4 PM_SPI_DATAIN
R926 1KR/4 UART_TX
R648 X_1KR/4 PM_SPI_DATAIN
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X1
R921 X_200KR/4 PM_SPI_CLK_R
R645 X_200KR/4 PM_SPI_DATAOUT
R924 1KR/4 PM_SPI_CLK_R
R643 1KR/4 PM_SPI_DATAOUT
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
MSI
MICRO-START INTL CO.,LTD.
Title
Promontory-CLK/ACPI/GPIO
Size Custom
Document Number MS-7A38
Rev 6.0
Date: Wednesday, September 26, 2018
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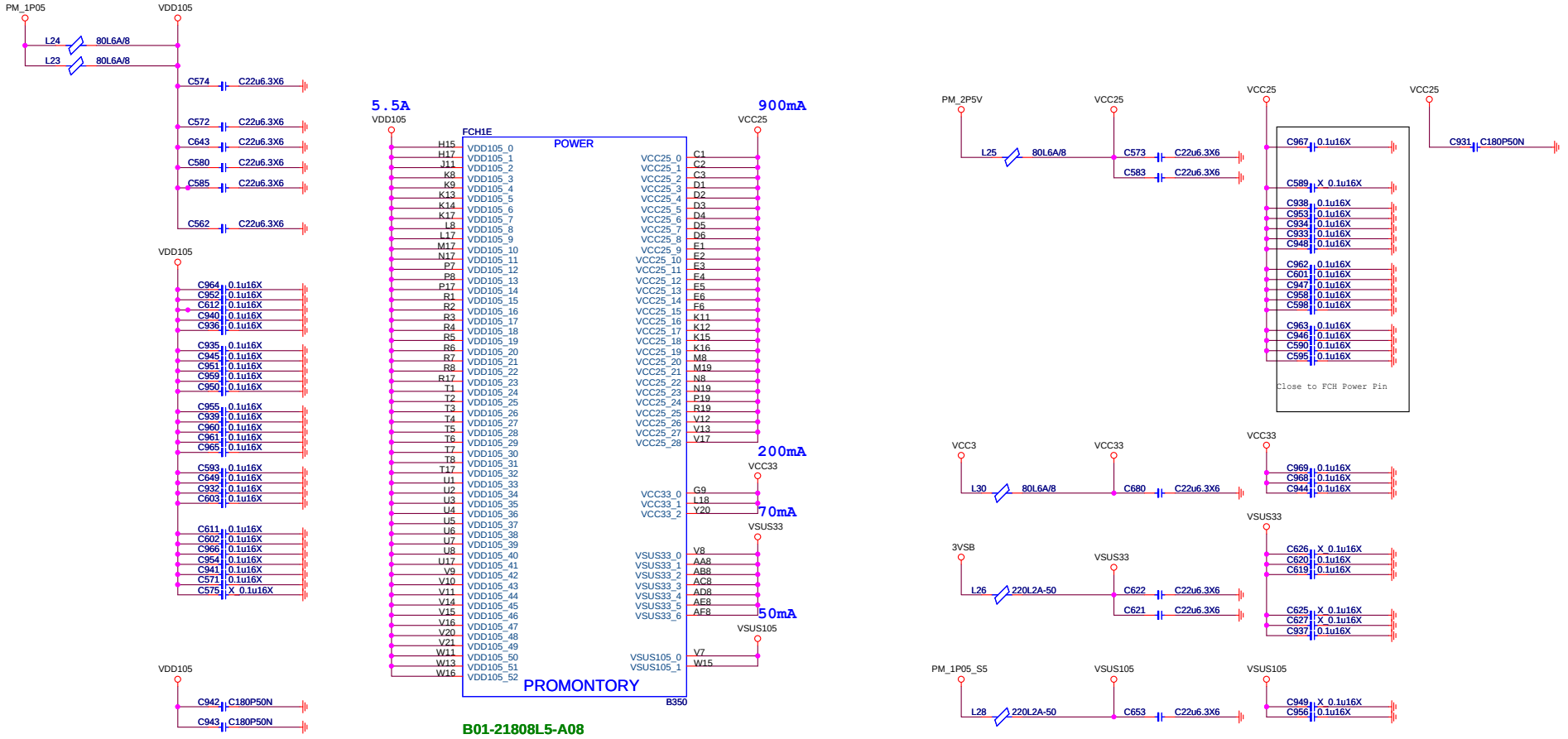
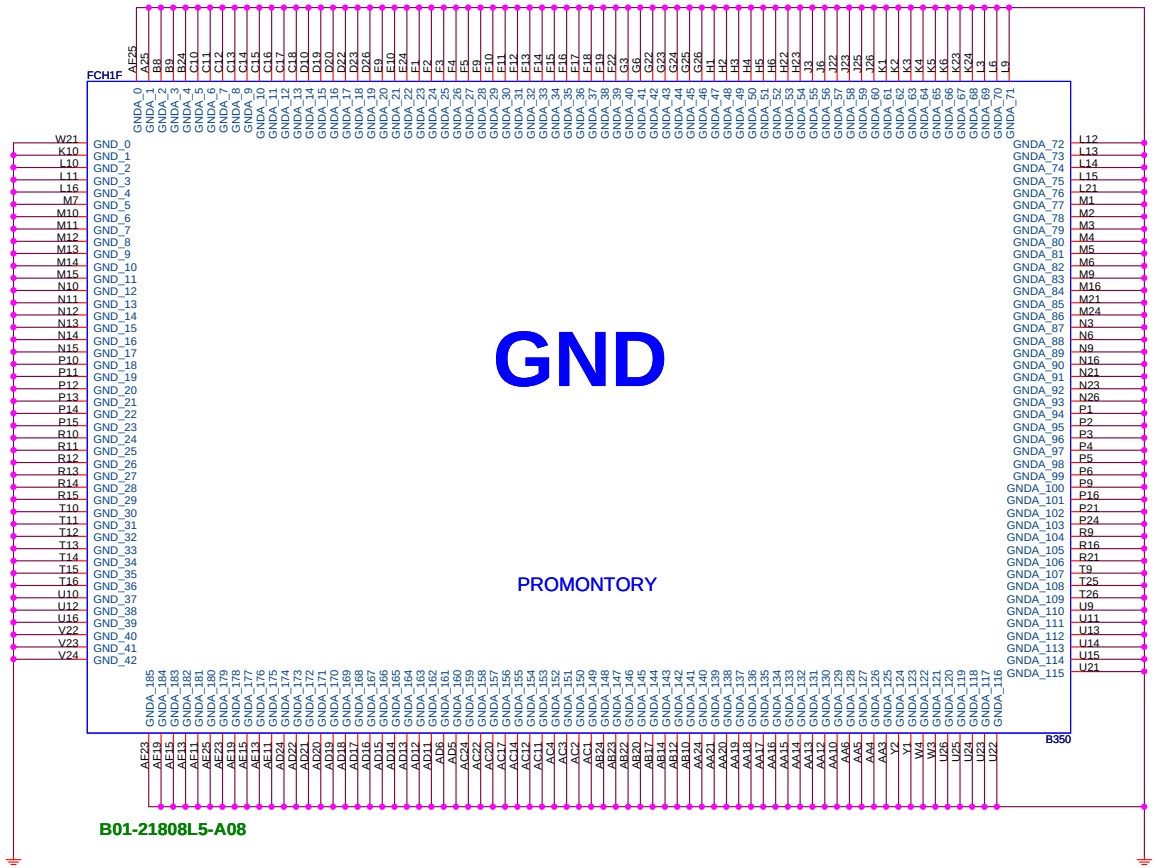


MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title: Promontory-Power		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 17 of 60	



MSI	MICRO-START INT'L CO.,LTD.
Title	Promontory-GND
Size	Custom
Document Number	MS-7A38
Rev	6.0
Date:	Wednesday, September 26, 2018
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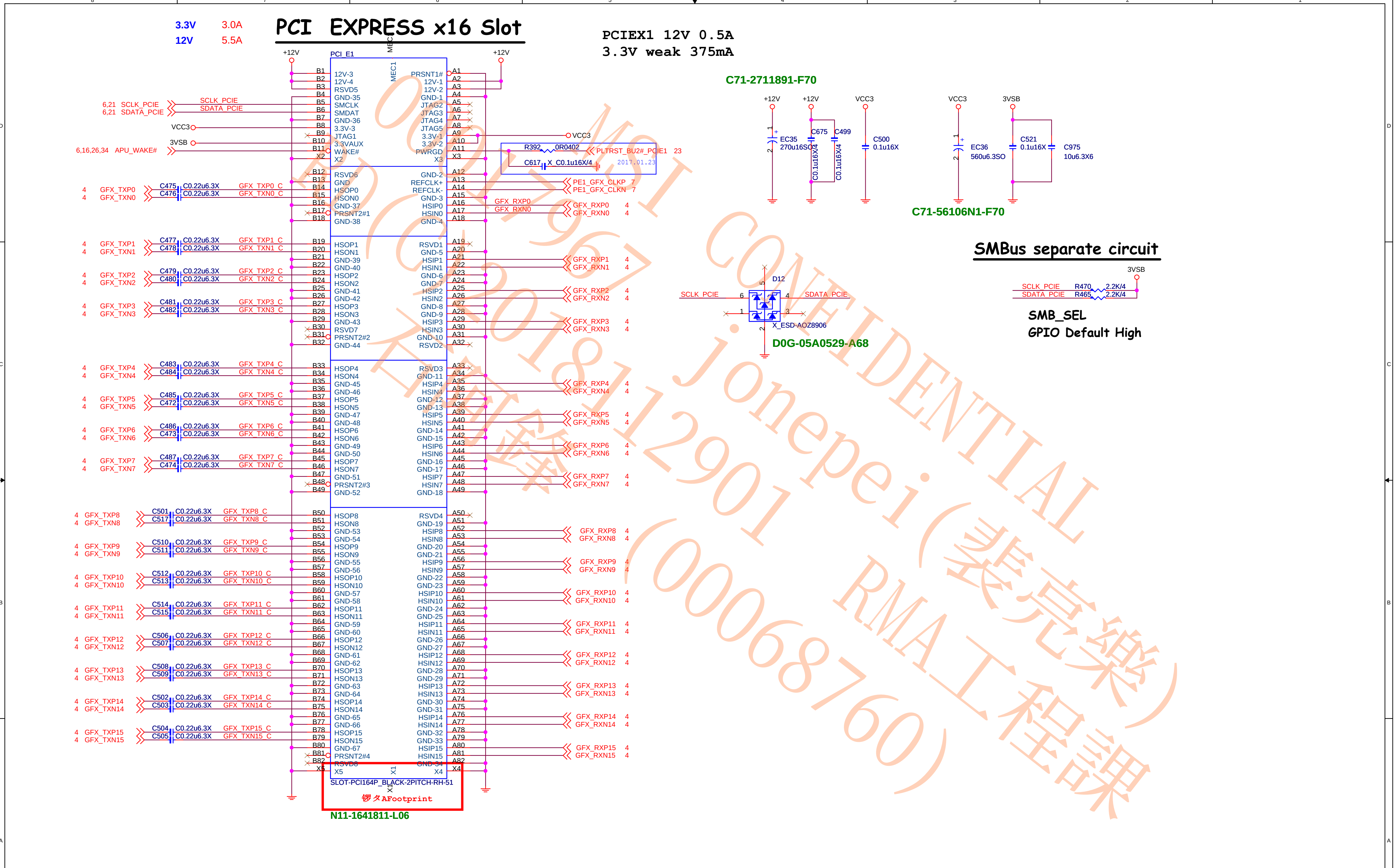
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: PCIE CLK		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 19 of 60	



PCI EXPRESS x16 Slot
3.3V 3.0A
12V 5.5A
PCIEX1 12V 0.5A
3.3V weak 375mA
C71-2711891-F70
C71-56106N1-F70
SMBus separate circuit
SMB_SEL
GPIO Default High
D0G-05A0529-A68
N11-1641811-L06
SLOT-PCI164P_BLACK-2PITCH-RH-51
PCI_E1
+12V
VCC3
3VSB
6,21 SCLK_PCIE
6,21 SDATA_PCIE
6,16,26,34 APU_WAKE#
PLTRST_BU2#_PCIE1 23
PE1_GFX_CLKP 7
PE1_GFX_CLKN 7
R392 0R0402
C617 X_C0.1u16X/4
2017.01.23
EC35 270u16SO
C675 C0.1u16X/4
C499 C0.1u16X/4
C500 0.1u16X
EC36 560u6.3SO
C521 0.1u16X
C975 10u6.3X6
R470 2.2K/4
R465 2.2K/4
D12
X_ESD-AOZ8906
GFX_TXP0 – GFX_TXP15, GFX_TXN0 – GFX_TXN15
GFX_RXP0 – GFX_RXP15, GFX_RXN0 – GFX_RXN15
C0.22u6.3X

MICRO-START INT'L CO.,LTD.

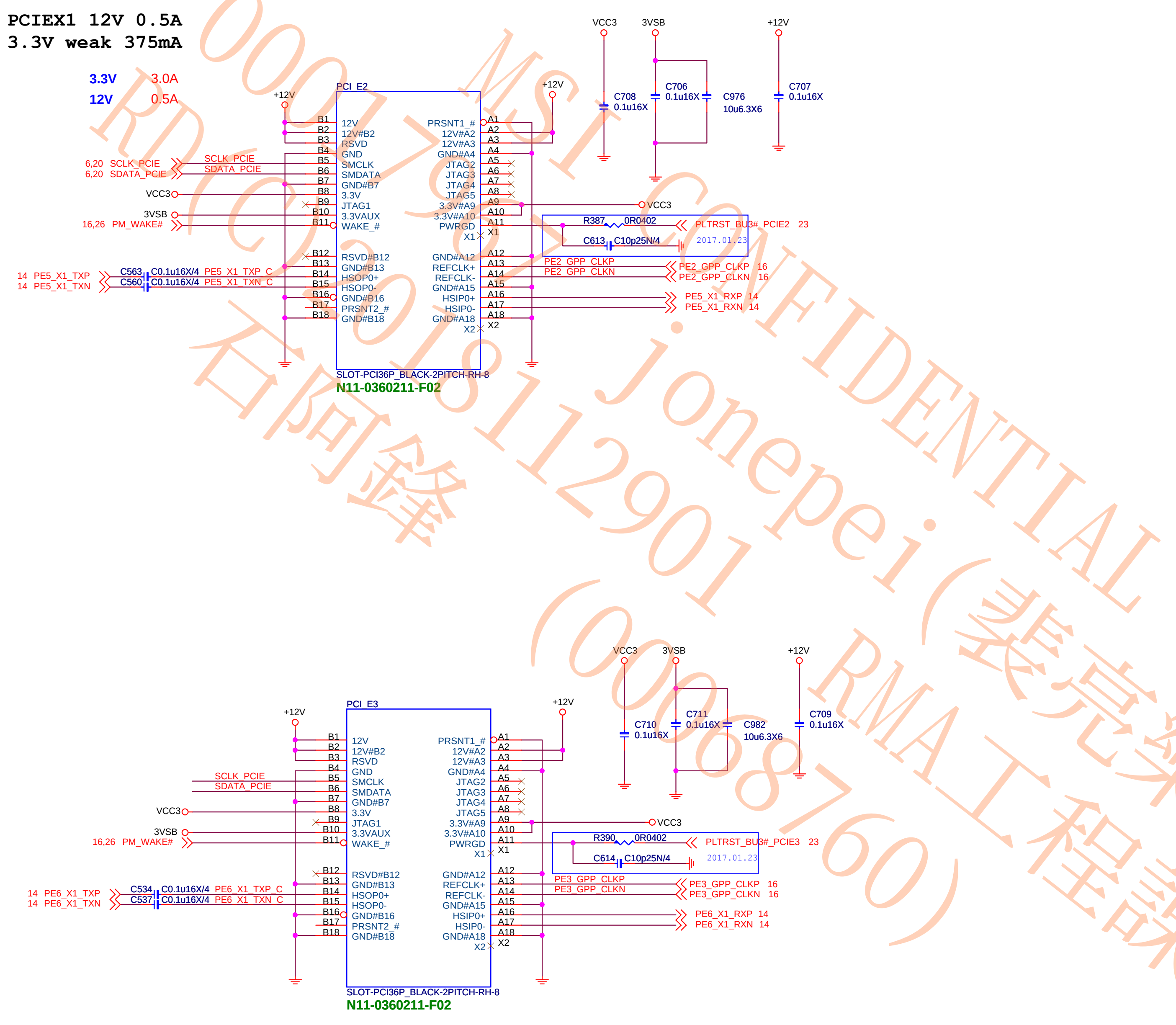
Title: PCIE X16 SLOT

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

Date: Wednesday, September 26, 2018 | Sheet 20 of 60

PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V	3.0A
12V	0.5A

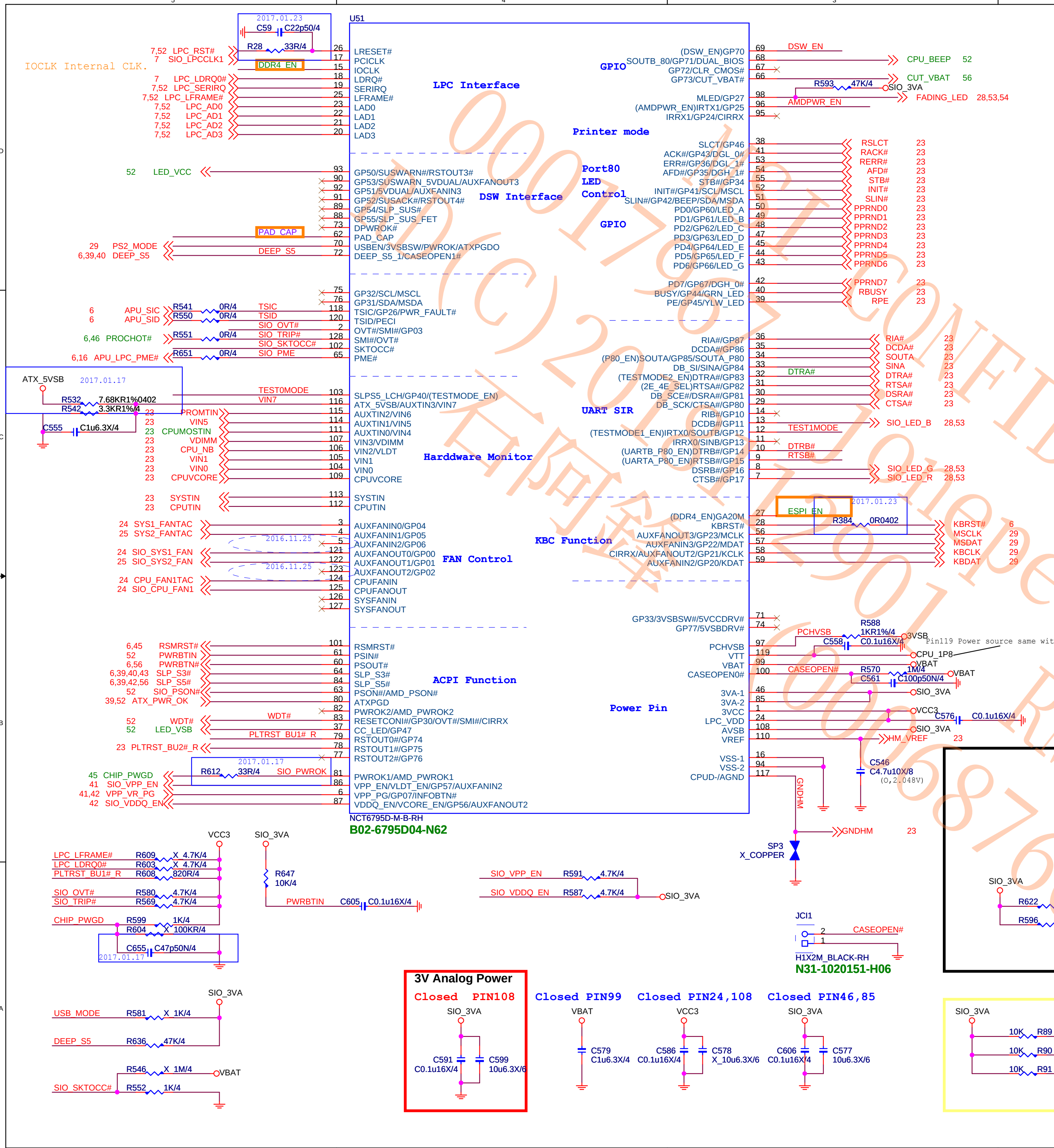


PCI Express x1 Slot *2

+12V		- 1 A
+VCC3		- 6A
+3V3_S5	(wake)	- 750mA
+3V3_S5	(no wake)	- 40mA

MSI Link to the Future MICRO-START INT'L CO.,LTD.

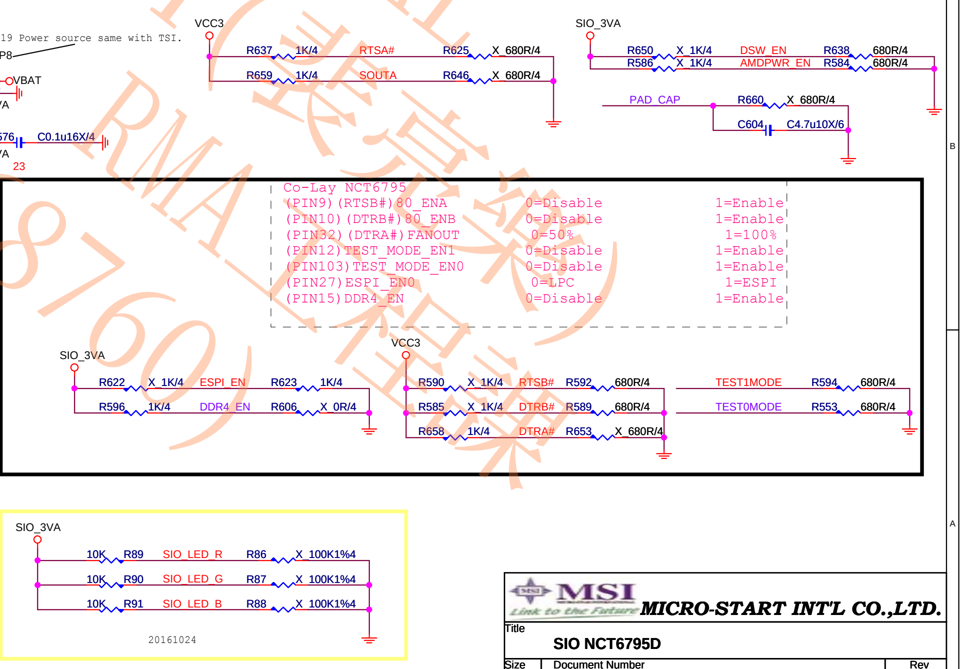
Title	PCIE X4(X1*2) SLOT	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 21 of 60	



POWER ON STRAPPING PIN FOR NCT6793/6795

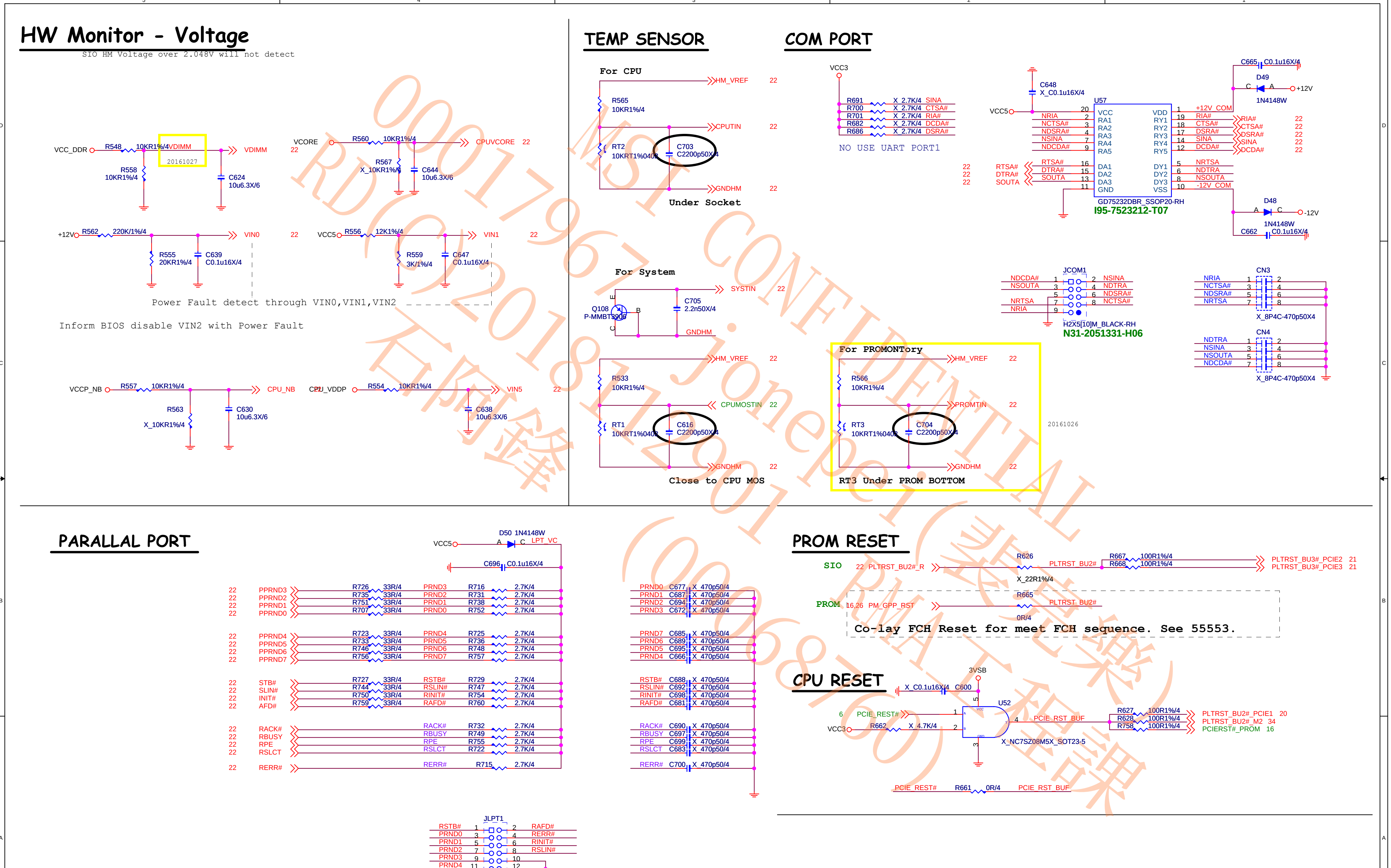
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO



MICRO-START INT'L CO.,LTD.

Title	SIO NCT6795D
Size Custom	Document Number MS-7A38
Rev	6.0
Date:	Wednesday, September 26, 2018
Sheet	22 of 60

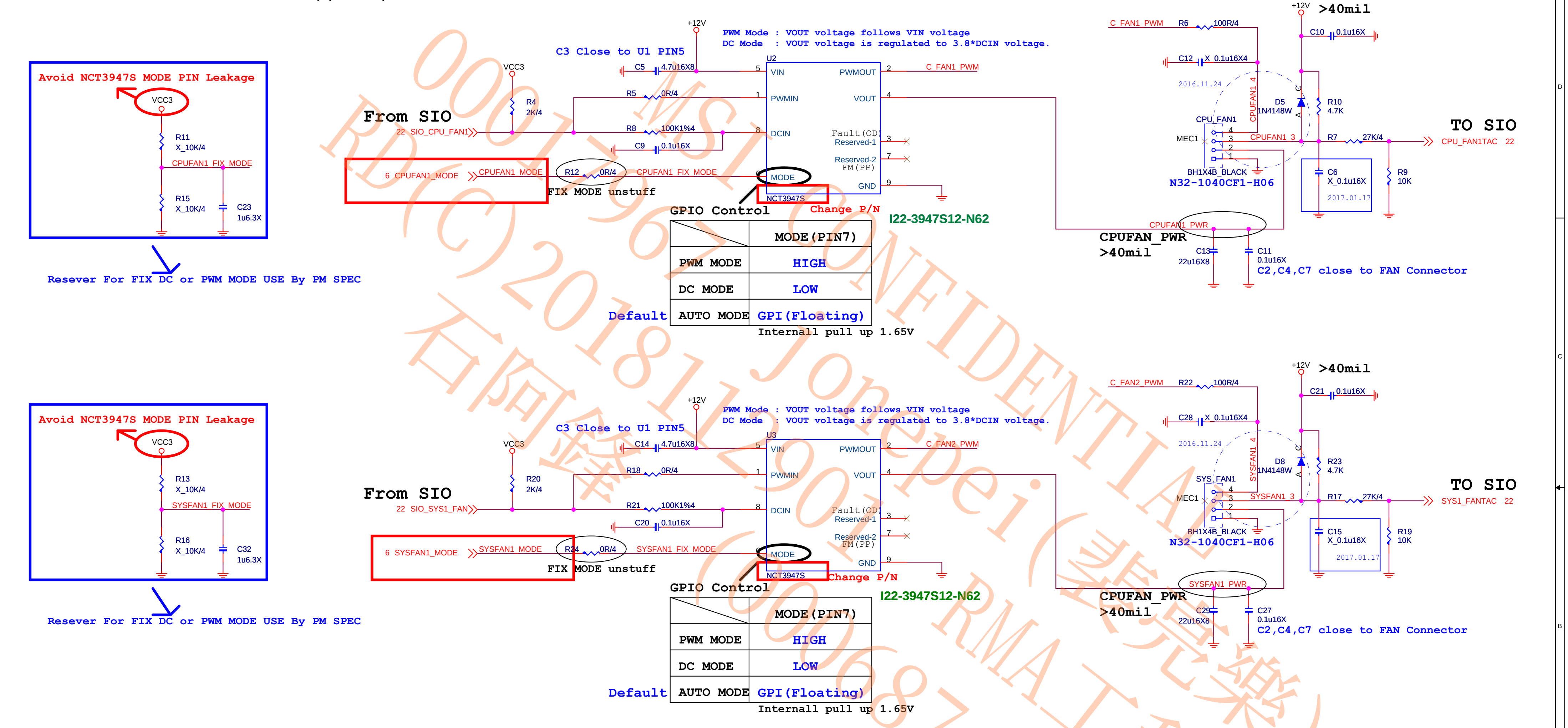


MSI MICRO-START INT'L CO.,LTD.

Title	HWM/COM/Debug LED	
Size Custom	Document Number MS-7A38	Rev 6.0
Date: Wednesday, September 26, 2018	Sheet 23 of 60	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パBIOSち传 PWM/DC MODE



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

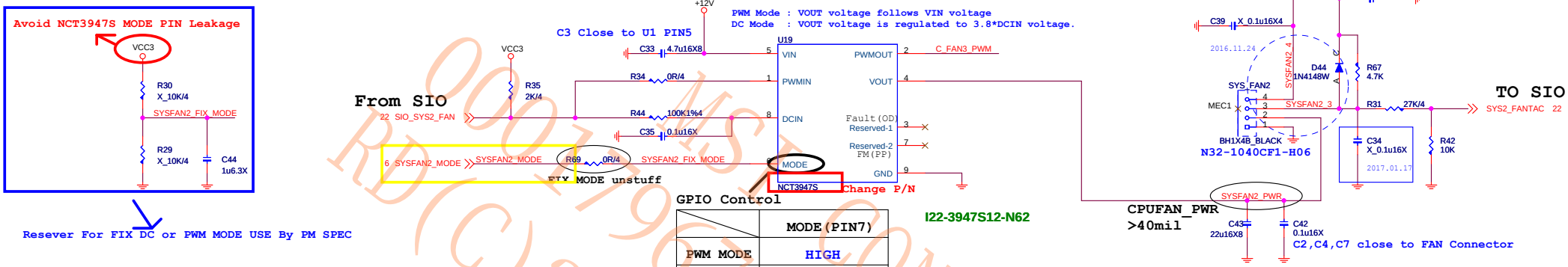
Internall pull up 1.65V

MSI MICRO-START INT'L CO.,LTD.

Title: CPU/SYS FAN Control TYPE K

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

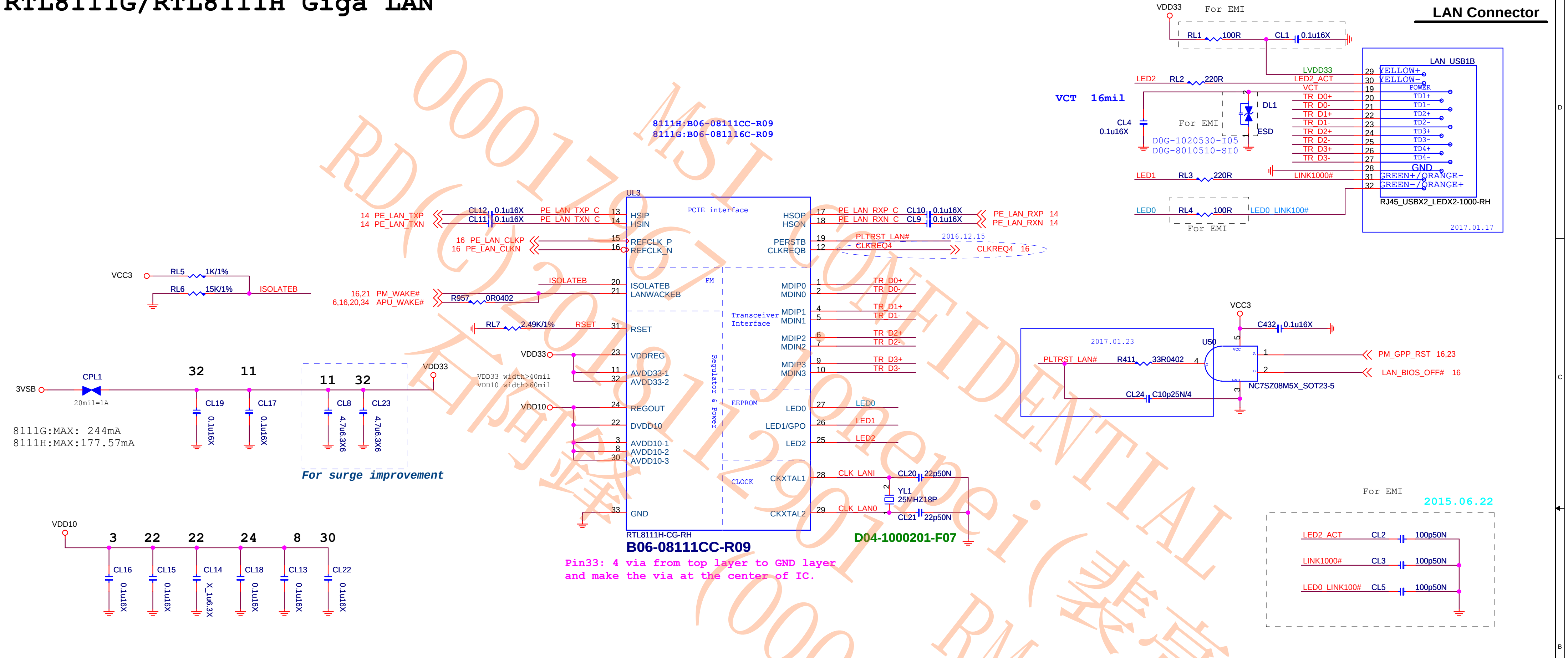
Date: Wednesday, September 26, 2018 | Sheet 24 of 60

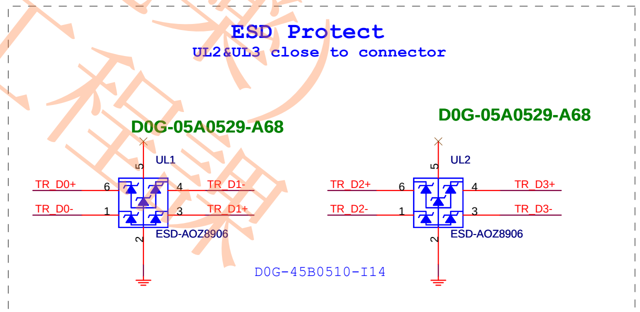


Title	CPU/SYS FAN 2	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 25 of 60	

MICRO-START INT'L CO.,LTD.

RTL8111G/RTL8111H Giga LAN





8111G POWER Consumption

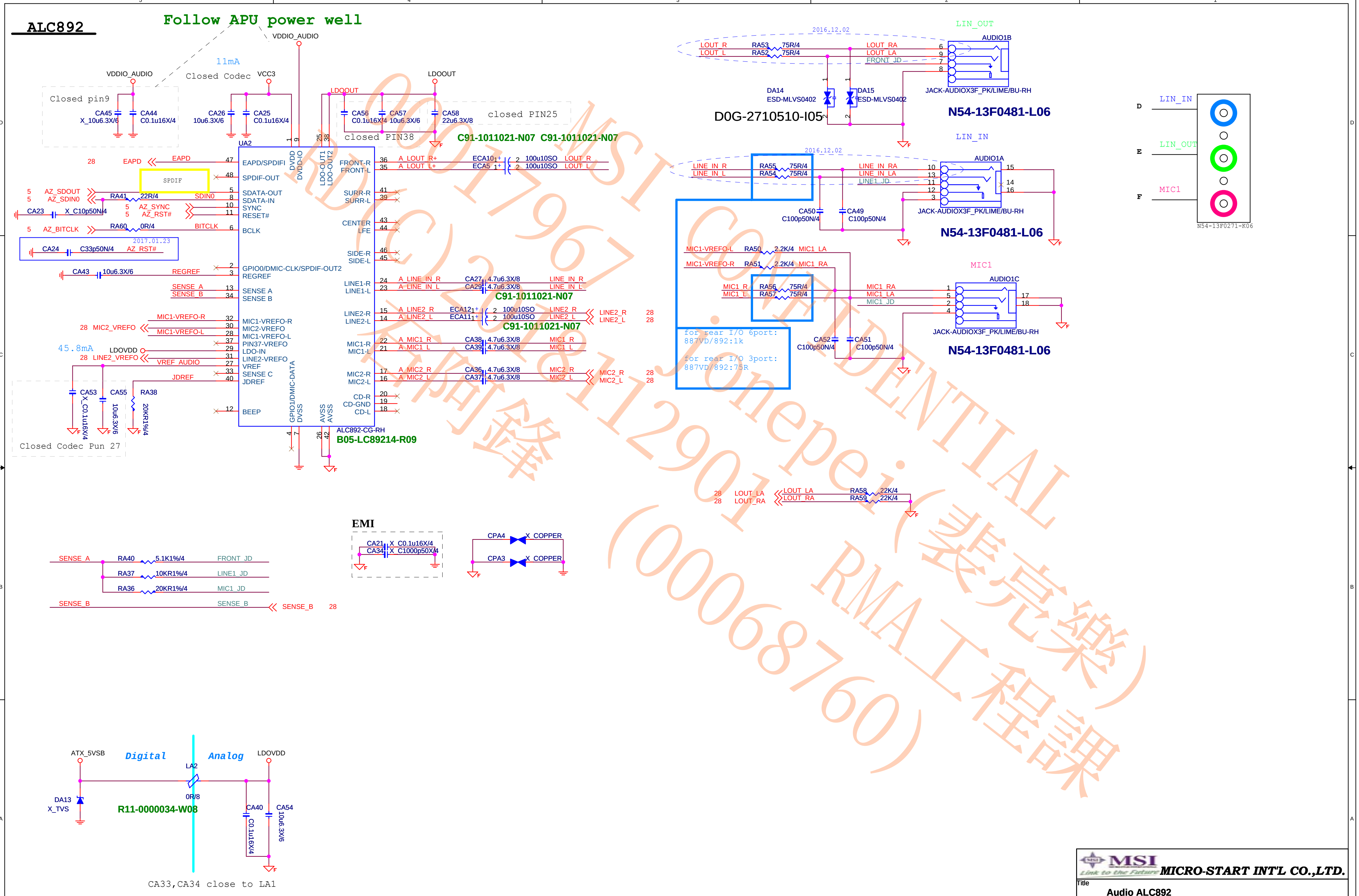
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

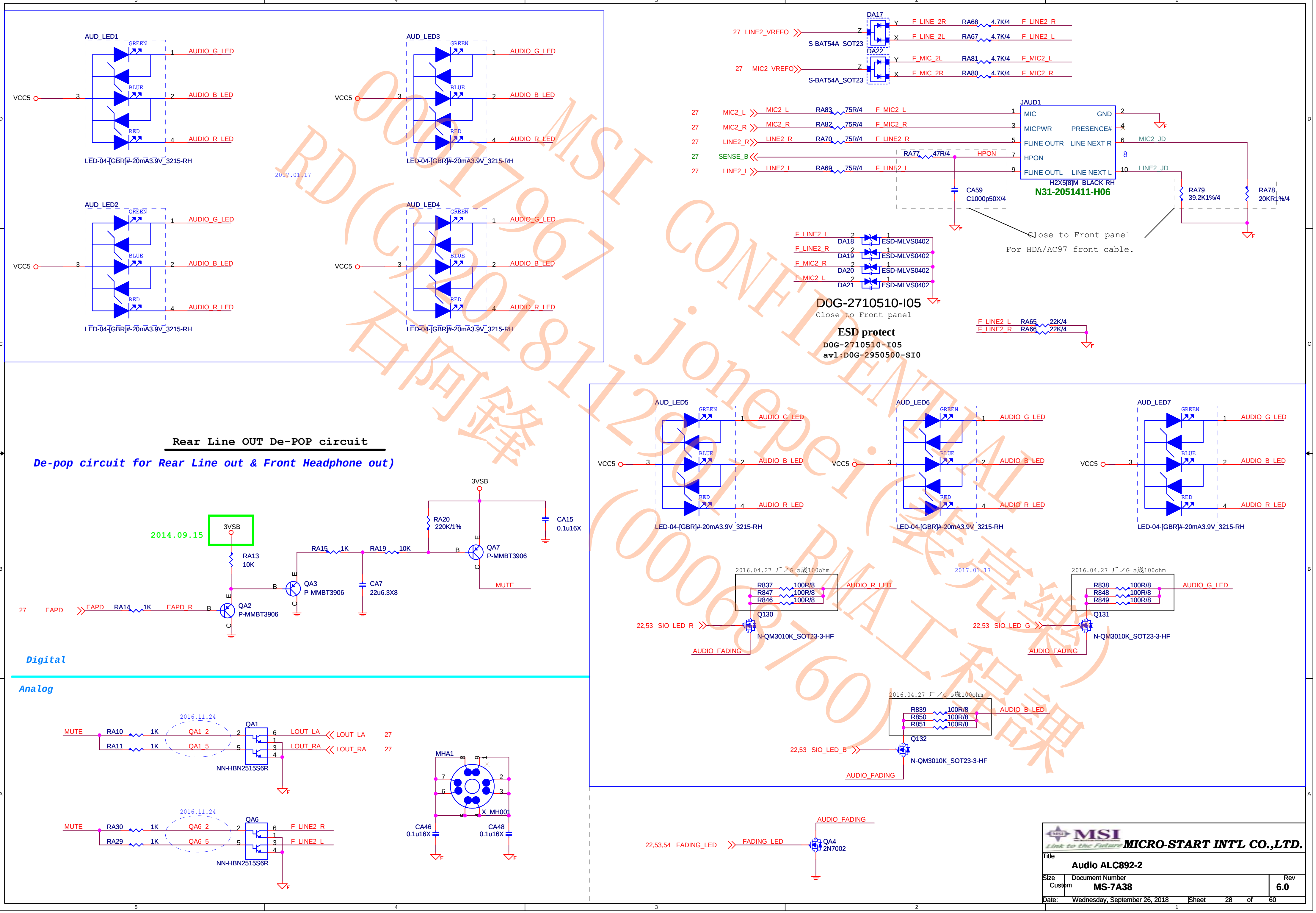
MSI Link to the Future MICRO-STAR INT'L CO.,LTD.

Title	LAN-RTL8111H	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 26 of 60	



MICRO-START INT'L CO.,LTD.

Title	Audio ALC892	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 27 of 60	



AUD_LED1
AUD_LED2
AUD_LED3
AUD_LED4
AUD_LED5
AUD_LED6
AUD_LED7
GREEN
BLUE
RED
VCC5
AUDIO_G_LED
AUDIO_B_LED
AUDIO_R_LED
LED-04-[GBR]#-20mA3.9V_3215-RH
2017.01.17
27 LINE2_VREFO
27 MIC2_VREFO
DA17
DA22
S-BAT54A_SOT23
F_LINE_2R RA68 4.7K/4 F_LINE2_R
F_LINE_2L RA67 4.7K/4 F_LINE2_L
F_MIC_2L RA81 4.7K/4 F_MIC2_L
F_MIC_2R RA80 4.7K/4 F_MIC2_R
JAUD1
27 MIC2_L MIC2_L RA83 75R/4 F_MIC2_L
27 MIC2_R MIC2_R RA82 75R/4 F_MIC2_R
27 LINE2_R LINE2_R RA70 75R/4 F_LINE2_R
27 SENSE_B RA77 47R/4 HPON
27 LINE2_L LINE2_L RA69 75R/4 F_LINE2_L
MIC GND
MICPWR PRESENCE#
FLINE OUTR LINE NEXT R
HPON
FLINE OUTL LINE NEXT L
MIC2_JD
LINE2_JD
H2X5[8]M_BLACK-RH
N31-2051411-H06
CA59 C1000p50X/4
RA79 39.2K1%/4
RA78 20KR1%/4
Close to Front panel
For HDA/AC97 front cable.
F_LINE2_L DA18 ESD-MLVS0402
F_LINE2_R DA19 ESD-MLVS0402
F_MIC2_R DA20 ESD-MLVS0402
F_MIC2_L DA21 ESD-MLVS0402
D0G-2710510-I05
Close to Front panel
ESD protect
D0G-2710510-I05
avl:D0G-2950500-SI0
F_LINE2_L RA65 22K/4
F_LINE2_R RA66 22K/4
Rear Line OUT De-POP circuit
De-pop circuit for Rear Line out & Front Headphone out)
3VSB
2014.09.15
RA13 10K
RA20 220K/1%
CA15 0.1u16X
RA15 1K
RA19 10K
QA7 P-MMBT3906
QA3 P-MMBT3906
CA7 22u6.3X8
MUTE
27 EAPD EAPD RA14 1K EAPD_R
QA2 P-MMBT3906
Digital
Analog
2016.11.24
MUTE RA10 1K QA1_2
RA11 1K QA1_5
QA1
LOUT_LA LOUT_LA 27
LOUT_RA LOUT_RA 27
NN-HBN2515S6R
MUTE RA30 1K QA6_2
RA29 1K QA6_5
QA6
F_LINE2_R
F_LINE2_L
MHA1
X_MH001
CA46 0.1u16X
CA48 0.1u16X
R837 100R/8
R847 100R/8
R846 100R/8
Q130
22,53 SIO_LED_R
N-QM3010K_SOT23-3-HF
AUDIO_FADING
R838 100R/8
R848 100R/8
R849 100R/8
Q131
22,53 SIO_LED_G
R839 100R/8
R850 100R/8
R851 100R/8
Q132
22,53 SIO_LED_B
22,53,54 FADING_LED FADING_LED
QA4 2N7002
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.
Title
Audio ALC892-2
Size Custom
Document Number MS-7A38
Rev 6.0
Date: Wednesday, September 26, 2018
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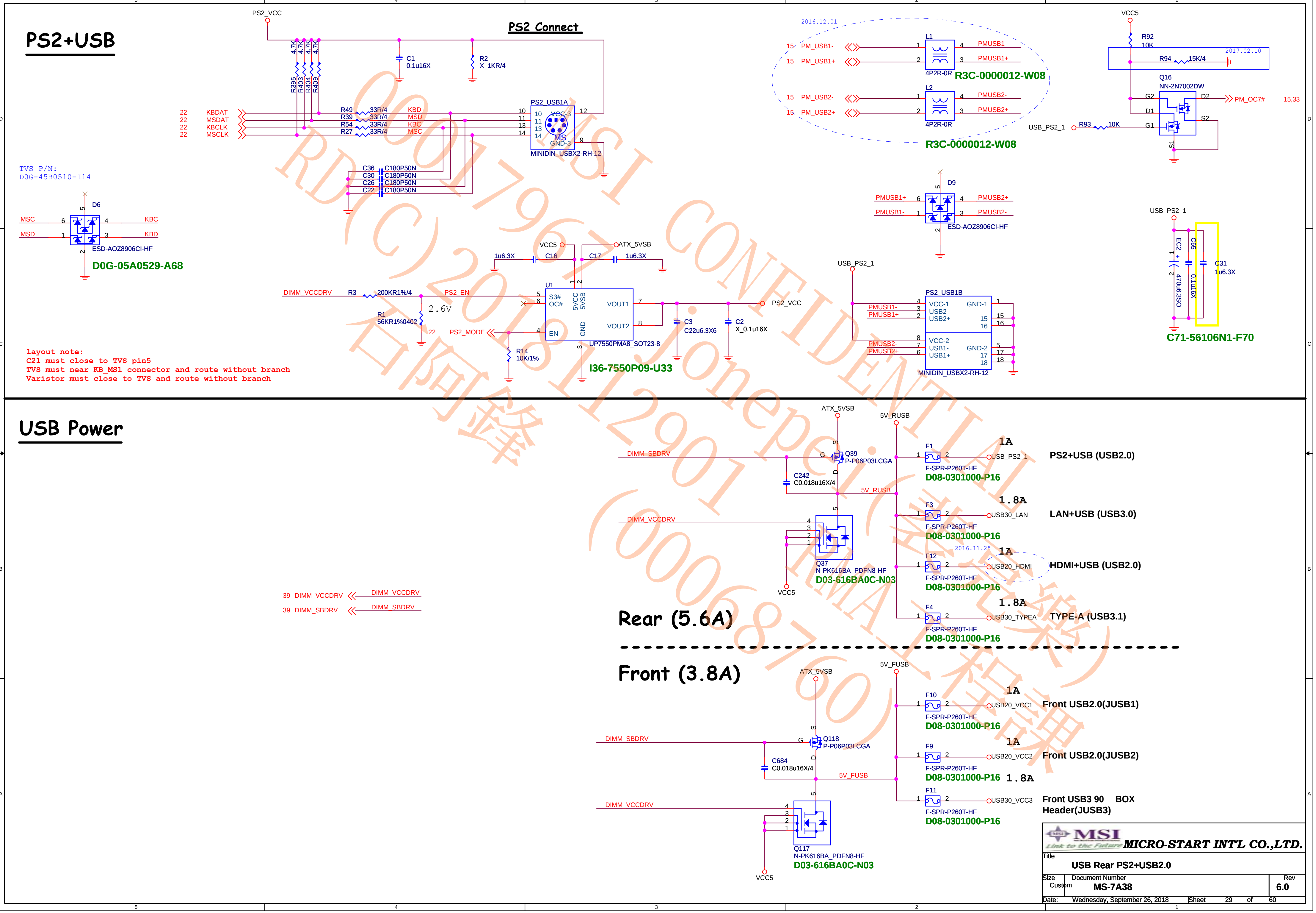
PS2+USB
PS2 Connect
USB Power
TVS P/N:
D0G-45B0510-I14
D0G-05A0529-A68
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch
R3C-0000012-W08
I36-7550P09-U33
UP7550PMA8_SOT23-8
C71-56106N1-F70
MINIDIN_USBX2-RH-12
ESD-AOZ8906CI-HF
Rear (5.6A)
Front (3.8A)
PS2+USB (USB2.0)
LAN+USB (USB3.0)
HDMI+USB (USB2.0)
TYPE-A (USB3.1)
Front USB2.0(JUSB1)
Front USB2.0(JUSB2)
Front USB3 90 BOX Header(JUSB3)
F-SPR-P260T-HF
D08-0301000-P16
N-PK616BA_PDFN8-HF
D03-616BA0C-N03
P-P06P03LCGA
MICRO-START INT'L CO.,LTD.
Title
USB Rear PS2+USB2.0
Size Custom
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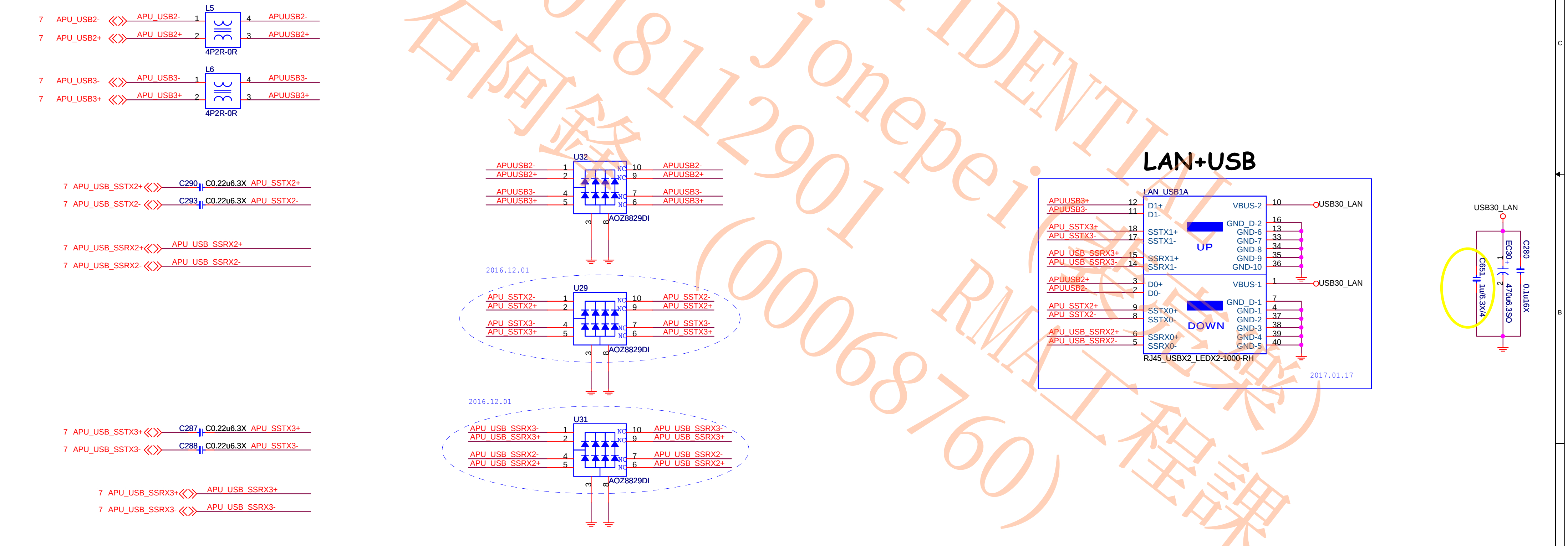
USB3.1 GEN1

VR Sloution U2 redriver



MICRO-START INT'L CO.,LTD.

Title: USB Rear LAN+TYPE A

Size	Document Number	Rev
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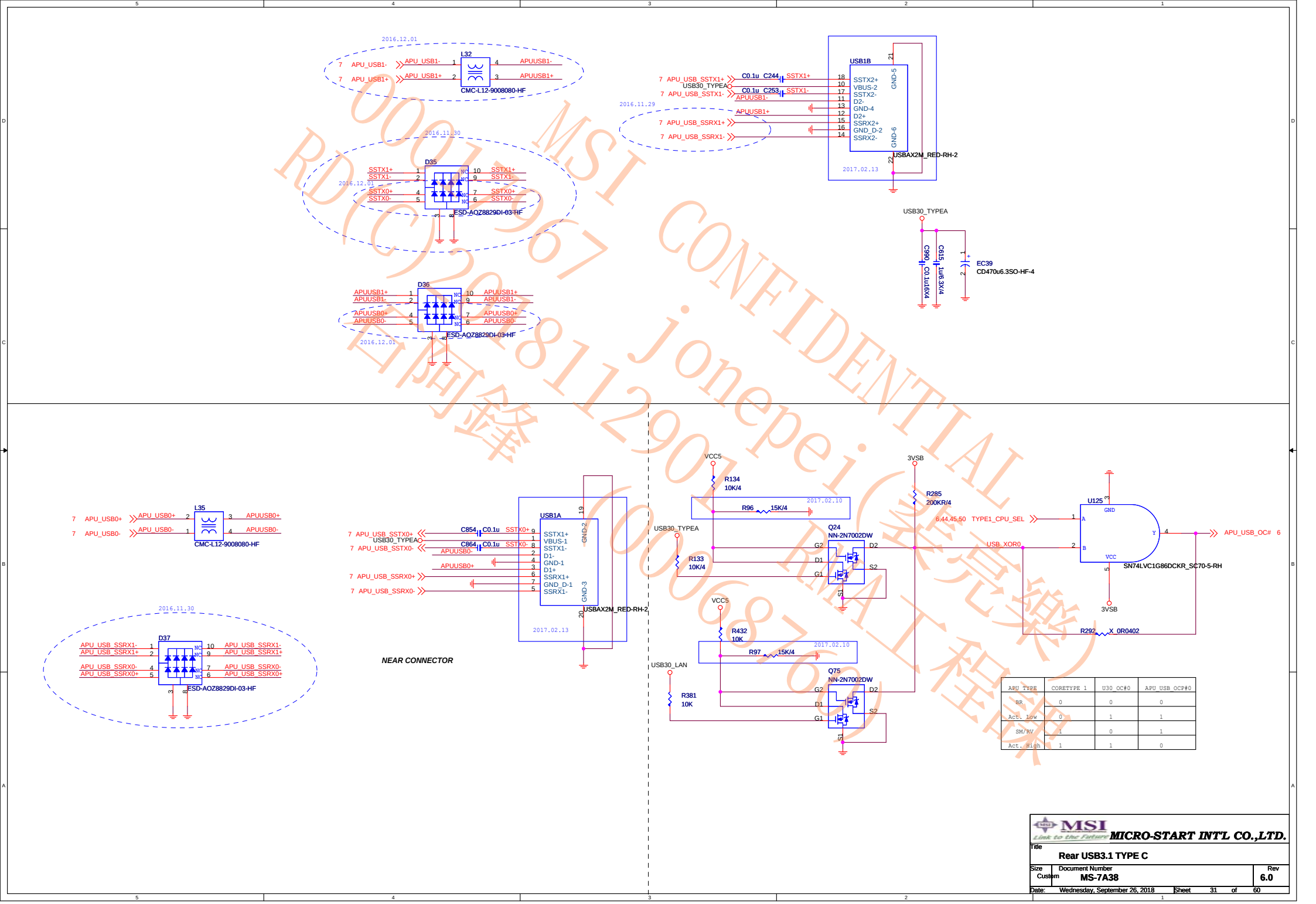
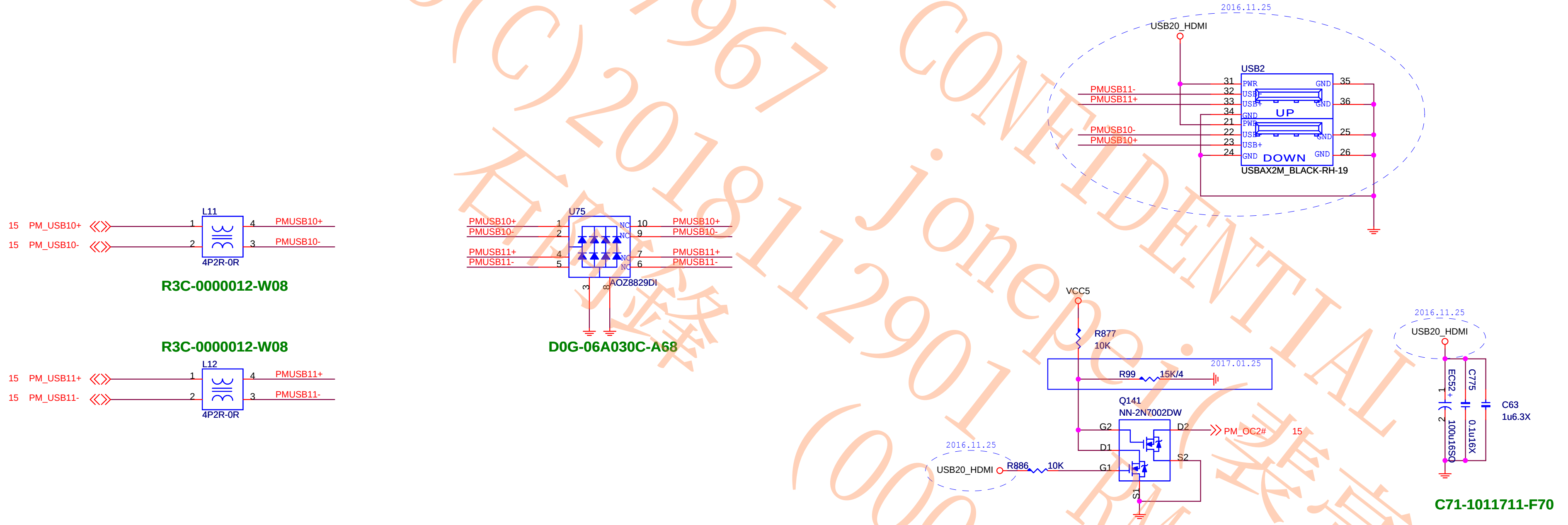

L32
CMC-L12-9008080-HF
USB1B
USBAX2M_RED-RH-2
D35
ESD-AOZ8829DI-03-HF
D36
ESD-AOZ8829DI-03-HF
EC39
CD470u6.3SO-HF-4
L35
CMC-L12-9008080-HF
USB1A
USBAX2M_RED-RH-2
D37
ESD-AOZ8829DI-03-HF
NEAR CONNECTOR
Q24
NN-2N7002DW
Q75
NN-2N7002DW
U125
SN74LVC1G86DCKR_SC70-5-RH
R134
10K/4
R96
15K/4
R133
10K/4
R285
200KR/4
R432
10K
R97
15K/4
R381
10K
R292
X_0R0402
APU_TYPE
CORETYPE_1
U30_OC#0
APU_USB_OCP#0
BR
Act. Low
SM/RV
Act. High
MICRO-START INT'L CO.,LTD.
Rear USB3.1 TYPE C
MS-7A38
Wednesday, September 26, 2018

Front USB2.0

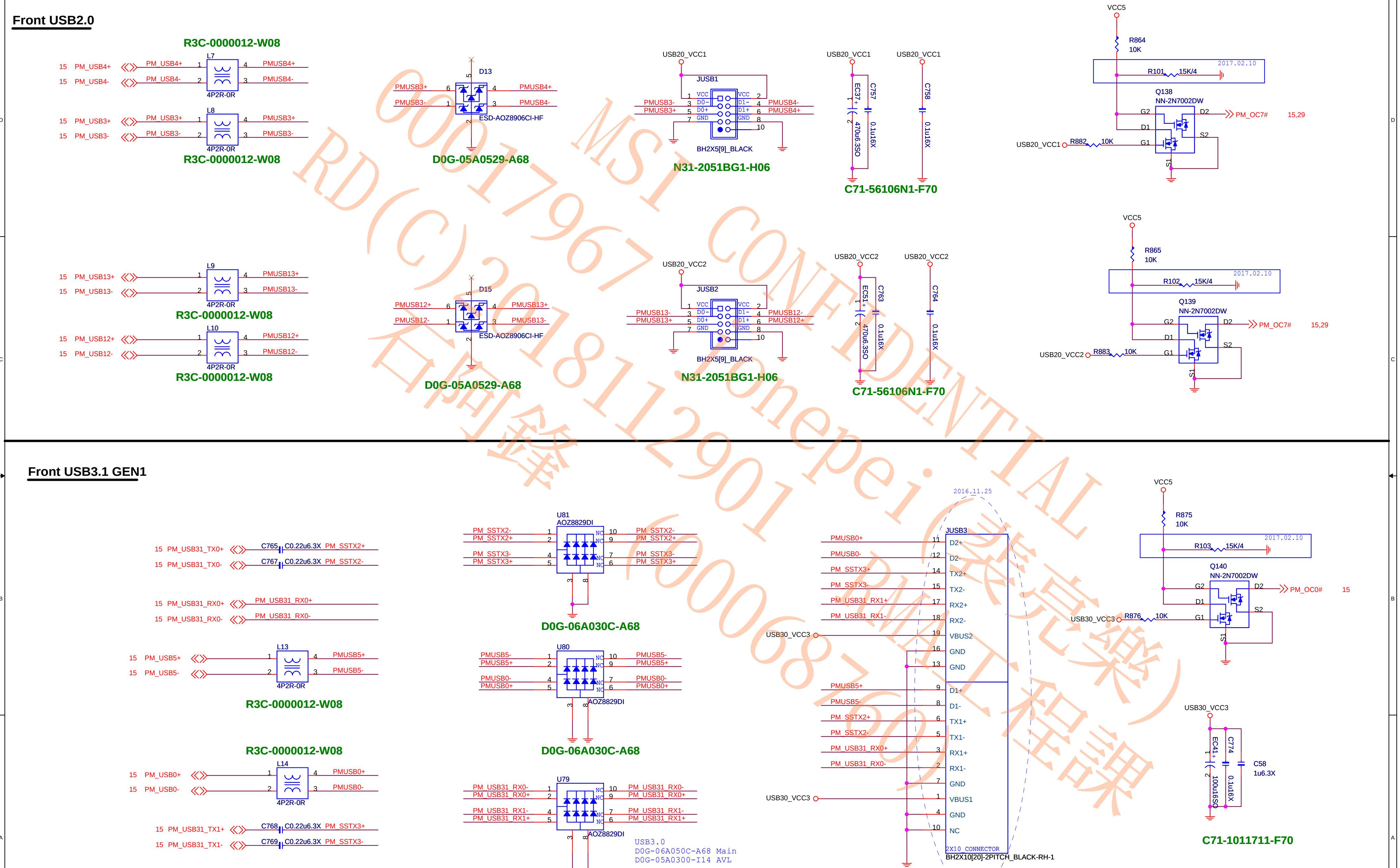


MICRO-START INT'L CO.,LTD.

Title: USB Rear HDMI+USB2.0

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

Date: Wednesday, September 26, 2018 | Sheet 32 of 60


Front USB2.0
R3C-0000012-W08
PM_USB4+
PM_USB4-
PMUSB4+
PMUSB4-
L7
4P2R-0R
L8
PM_USB3+
PM_USB3-
PMUSB3+
PMUSB3-
D13
ESD-AOZ8906CI-HF
D0G-05A0529-A68
USB20_VCC1
JUSB1
BH2X5[9]_BLACK
N31-2051BG1-H06
EC37
470u6.3SO
C757
0.1u16X
C758
C71-56106N1-F70
VCC5
R864
10K
R101
15K/4
2017.02.10
Q138
NN-2N7002DW
PM_OC7#
15,29
R882
L9
PM_USB13+
PM_USB13-
PMUSB13+
PMUSB13-
L10
PM_USB12+
PM_USB12-
PMUSB12+
PMUSB12-
D15
USB20_VCC2
JUSB2
EC51
C763
C764
R865
R102
Q139
R883
Front USB3.1 GEN1
PM_USB31_TX0+
PM_USB31_TX0-
C765
C767
C0.22u6.3X
PM_SSTX2+
PM_SSTX2-
PM_USB31_RX0+
PM_USB31_RX0-
L13
PM_USB5+
PM_USB5-
PMUSB5+
PMUSB5-
L14
PM_USB0+
PM_USB0-
PMUSB0+
PMUSB0-
PM_USB31_TX1+
PM_USB31_TX1-
C768
C769
PM_SSTX3+
PM_SSTX3-
PM_USB31_RX1+
PM_USB31_RX1-
U81
AOZ8829DI
D0G-06A030C-A68
U80
U79
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL
2016.11.25
JUSB3
USB30_VCC3
VBUS2
VBUS1
GND
NC
2X10_CONNECTOR
BH2X10[20]-2PITCH_BLACK-RH-1
R875
R103
Q140
PM_OC0#
R876
EC41
100u16SO
C774
C58
1u6.3X
C71-1011711-F70

MSI MICRO-START INT'L CO.,LTD.

Title: USB Front Side

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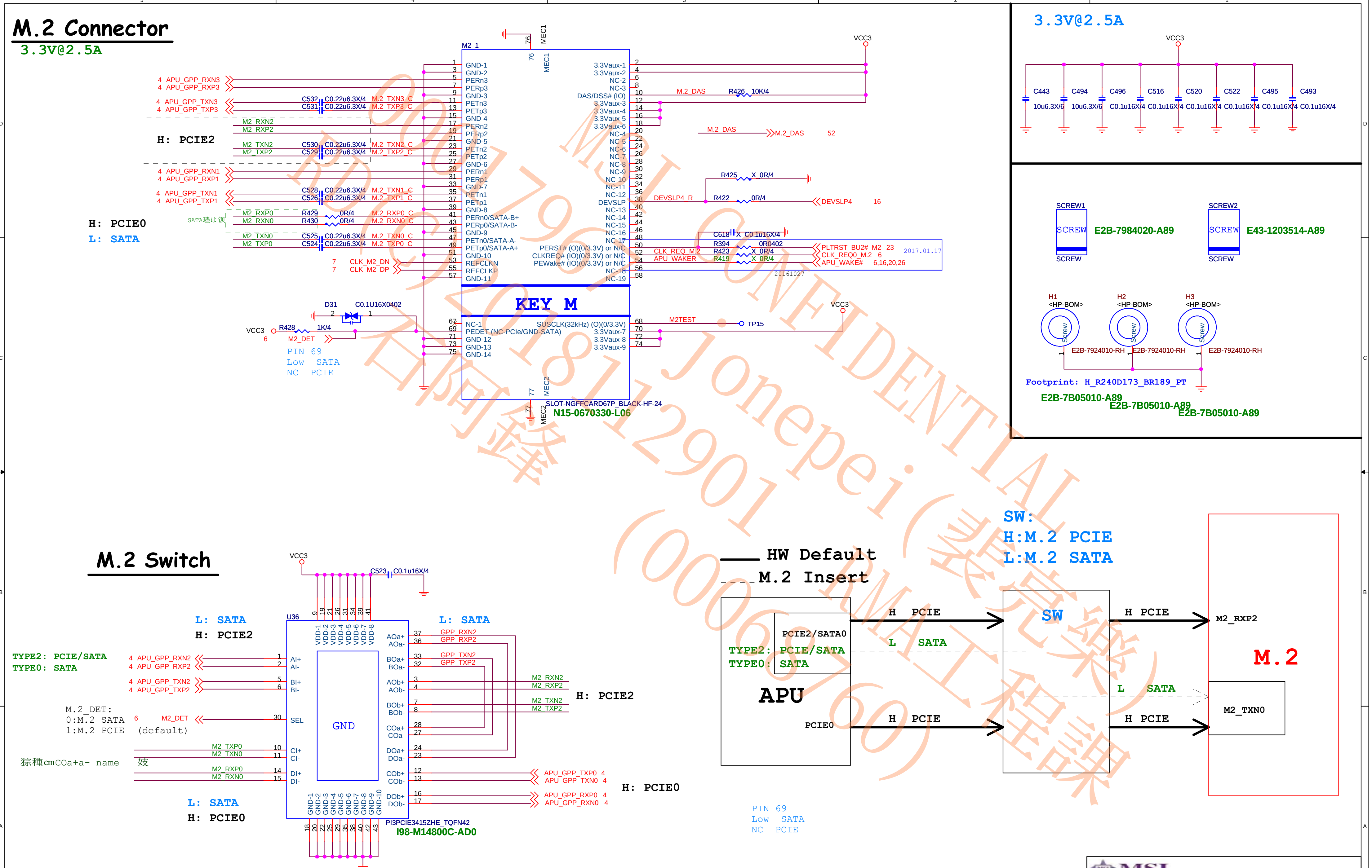


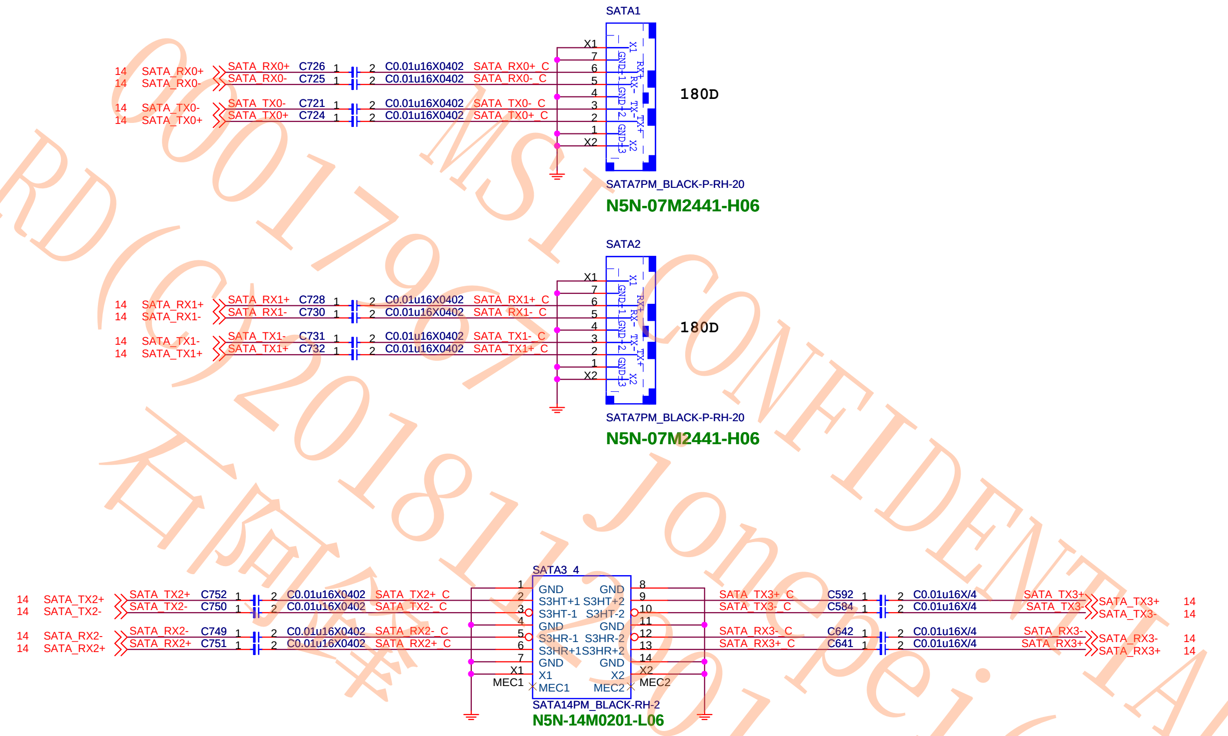
MSI MICRO-START INT'L CO.,LTD.

Title: M.2

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

Date: Wednesday, September 26, 2018 | Sheet 34 of 60

SATA Connector



MSI MICRO-START INT'L CO.,LTD.

Title	SATA Connector	
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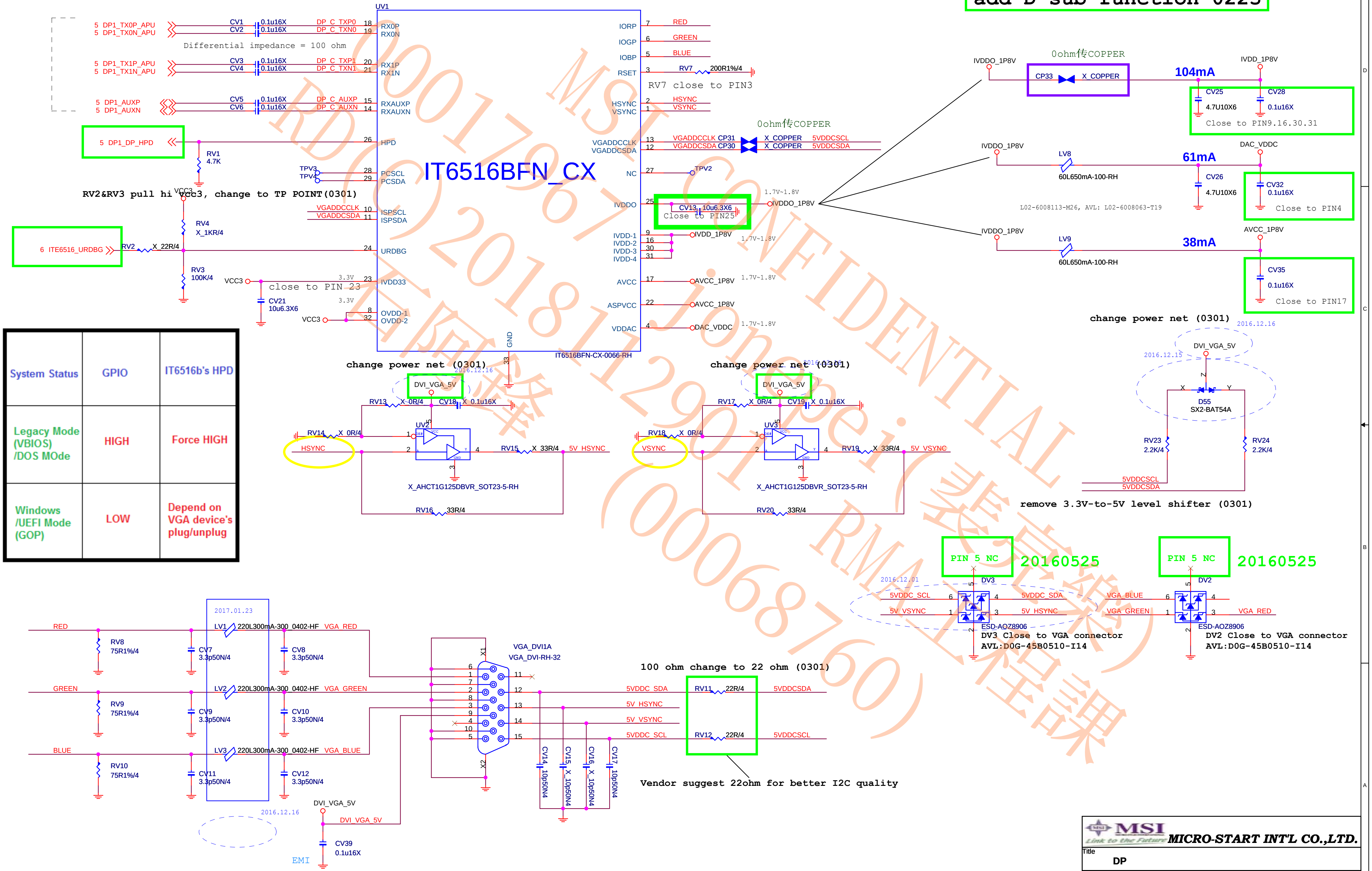
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

add D-sub function 0225



System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

Title	DP	
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DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

5 DVI_DDPC_CLK_N
5 DVI_DDPC_CLK_P
5 DVI_DDPC_TXN2
5 DVI_DDPC_TXP2
5 DVI_DDPC_TXN1
5 DVI_DDPC_TXP1
5 DVI_DDPC_TXN0
5 DVI_DDPC_TXP0

C154 0.1u16X DVI_TXC- R165 499R/1%
C159 0.1u16X DVI_TXC+ R201 499R/1%
C149 0.1u16X DVI_TXD2- R194 499R/1%
C171 0.1u16X DVI_TXD2+ R164 499R/1%
C169 0.1u16X DVI_TXD1- R207 499R/1%
C143 0.1u16X DVI_TXD1+ R160 499R/1%
C144 0.1u16X DVI_TXD0- R150 499R/1%
C141 0.1u16X DVI_TXD0+ R192 499R/1%

DVI_DATA

VCC3 Q71 2N7002

2016.11.24

R617 0R/6

DVI_VGA_5V

2016.12.15

D57 SX2-BAT54A

R169 2.2K
R193 2.2K

Q84 2N7002D

VCC3 G2 D2 DVI_DDC_DATA_R
DVI_DDC_CLK_R D1
VCC3 G1 S2 DVI_DDPC_CTRLDATA 5
S1
5 DVI_DDPC_CTRLCLK

VCC3 C489 X_0.1u16X

VCC3 R619 4.7KR/4 DVI_DDPC_CTRLCLK
VCC3 R620 4.7KR/4 DVI_DDPC_CTRLDATA

20161027

2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

U6

DVI_TXD2- DVI_TXD2+ DVI_TXC+ DVI_TXC-
AOZ8829DI
DVI_TXD2- DVI_TXD2+ DVI_TXC+ DVI_TXC-

D0G-06A030C-A68

U5

DVI_TXD0- DVI_TXD0+ DVI_TXD1- DVI_TXD1+
AOZ8829DI
DVI_TXD0- DVI_TXD0+ DVI_TXD1- DVI_TXD1+

D0G-06A030C-A68

VGA_DVI1B

DVI_TXD2- DVI_TXD2+ DVI_DDC_CLK_R DVI_DDC_DATA_R DVI_TXD1- DVI_TXD1+ DVI_HOT_DET DVI_TXD0- DVI_TXD0+ DVI_TXC+ DVI_TXC-

Shell-3 Shell-5 Shell-6 Shell-7 Shell-8 Shell-4
DATA2 SHIELD-1 DATA4 DDCCLK DDCDATA NC DATA1 SHIELD-2 DATA3 VCC5 GND5 HPDET DATA0 SHIELD-3 DATA5 SHIELD-4 CLK
G1 G2 G3 G4

VGA_DVI-RH-32

DVI_VGA_5V

C155 0.1u16X

HPD

VCC3 DVI_VGA_5V R203 10K
R191 10K
5 DVI_DDPC_HPD
Q28
C173 X_0.01u16X
NN-CMKT3904
DVI_HOT_DET_R R171 10K DVI_HOT_DET
R168 100K C148 0.01u16X

DVI1

DVI_VGA_5V
DVI_TXD2- DVI_TXD2+ DVI_DDC_CLK_R DVI_DDC_DATA_R DVI_TXD1- DVI_TXD1+ DVI_HOT_DET DVI_TXD0- DVI_TXD0+ DVI_TXC+ DVI_TXC-

Shell-1 DATA2 SHIELD24 DATA4 DDCCLK DDCDATA NC DATA1 SHIELD13 DATA3 VCC5 GND5 HPDET DATA0 SHIELD05 DATA5 SHIELDCLK CLK Shell-2 Shell-3 Shell-4 Shell-5 Shell-6

DI24FD680B2

2016.12.01

U4

DVI_DDC_CLK_R DVI_DDC_DATA_R DVI_HOT_DET
ESD-AOZ8906CI-HF

D0G-05A0529-A68

For EMI

DVI_TXD0- DVI_TXD0+ R151 X_243R/1%
DVI_TXD1- DVI_TXD1+ R158 X_243R/1%
DVI_TXC- DVI_TXC+ R200 X_243R/1%
DVI_TXD2- DVI_TXD2+ R162 X_243R/1%

DVI_HOT_DET
DVI_DDC_CLK_R
DVI_DDC_DATA_R
C147 X_10p50N
C146 X_10p50N
C151 X_10p50N

D08-0100800-P16

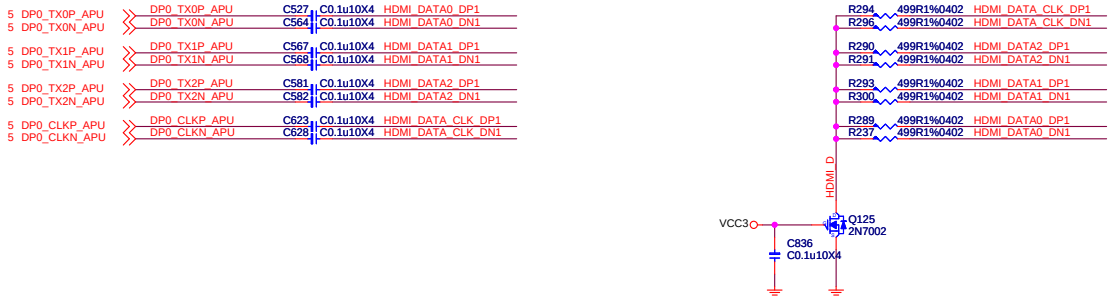
VCC5 DV1 S-1N5817 FSV1 MICROSMD110 DVI_VGA_5V
CV38 0.1u16X
EMI

MSI Link to the Future MICRO-START INT'L CO.,LTD.

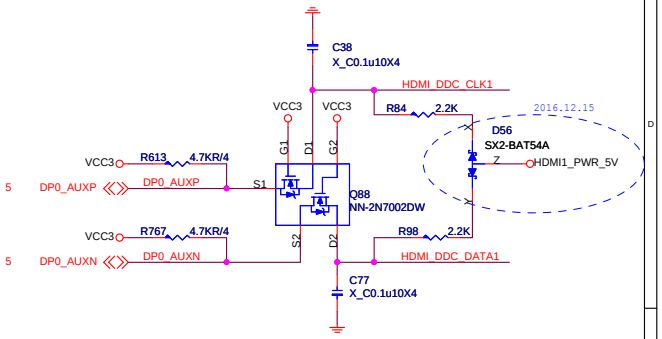
Title: DVI Connector		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 37 of 60	

HDMI CONNECTOR

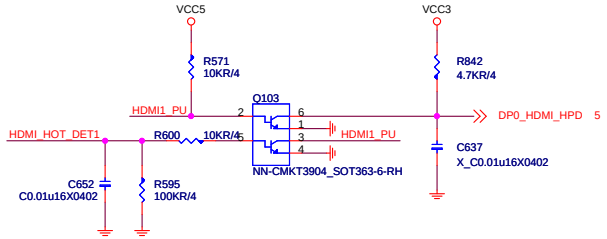
For HDMI 1.4



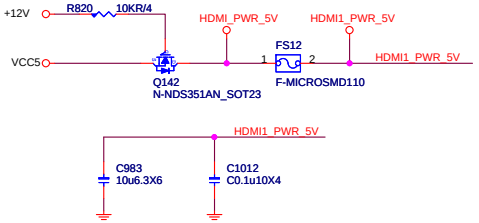
AUX Level Shifter



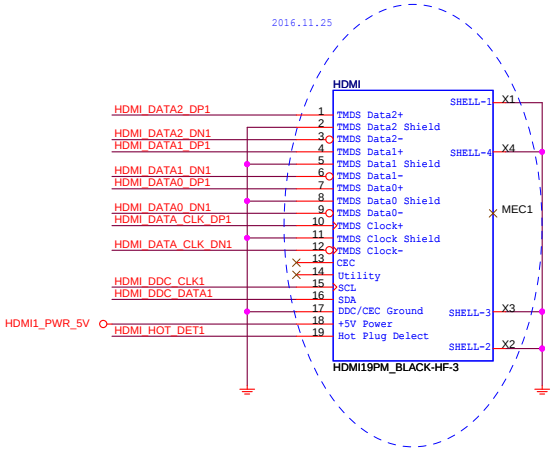
HPD Circuit



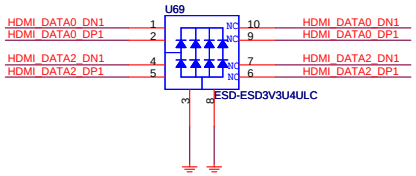
Connector Power



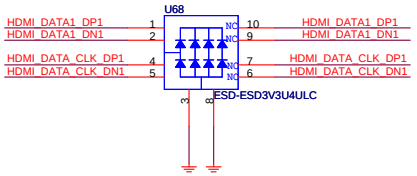
Connector



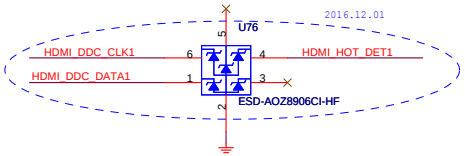
For EMI



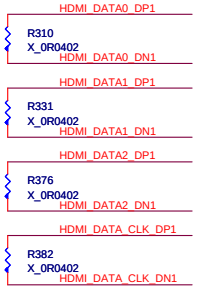
D0G-05A0300-I14



D0G-05A0300-I14



D0G-05A0529-A68



MICRO-START INT'L CO.,LTD.

Title: HDMI		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
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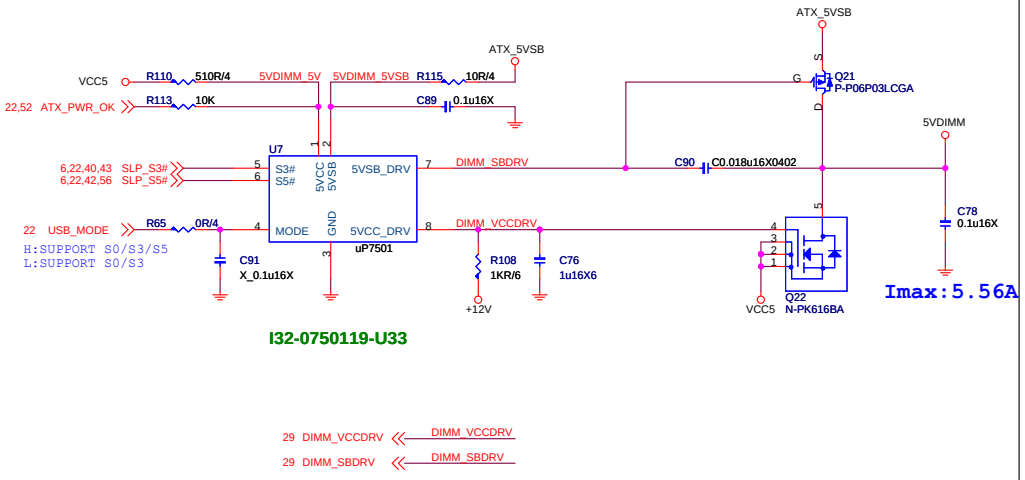
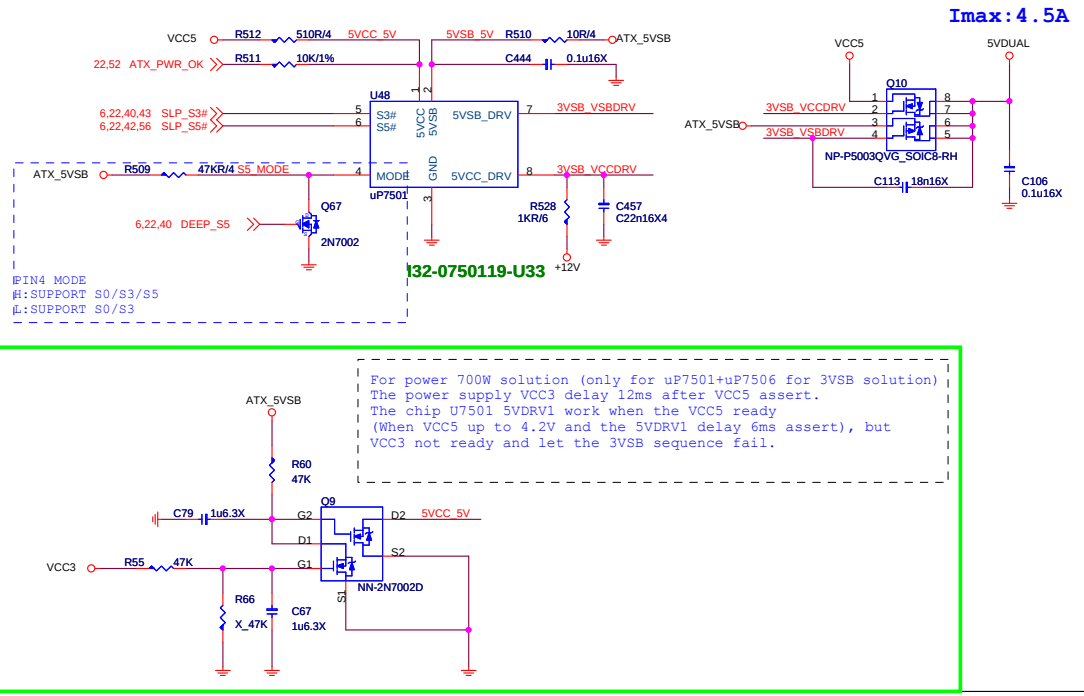
5VDIMM FOR DDR

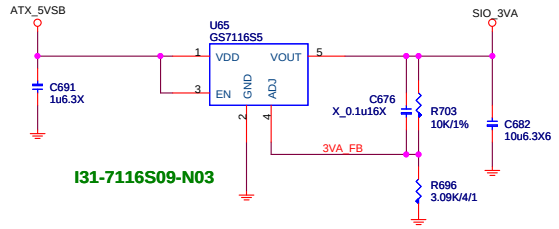


5VDUAL For 3VSB CPU 1.8V VDDP



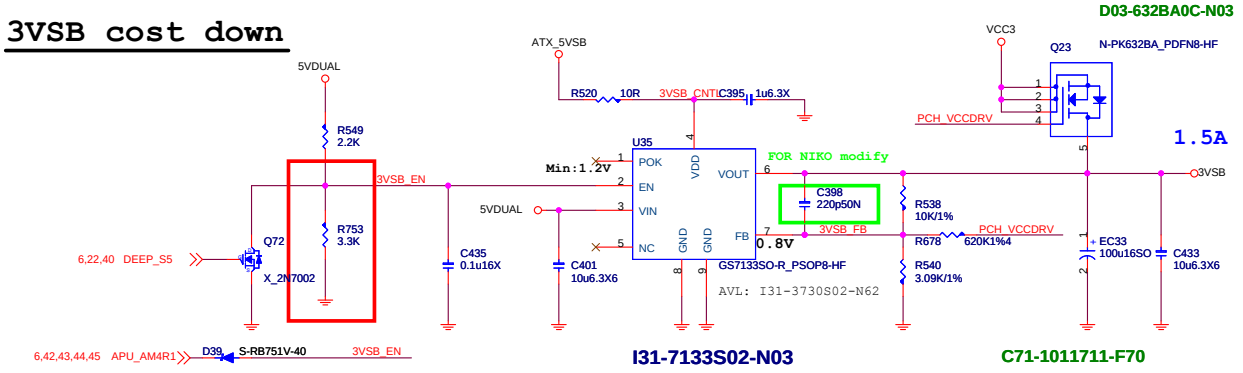
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

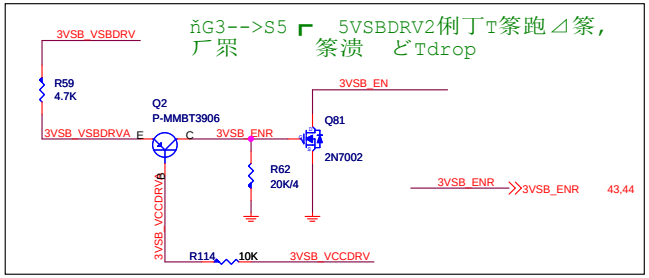
SIO_3VA



3VSB cost down

D03-632BA0C-N03





MSI Link to the Future MICRO-START INTL CO.,LTD.

Title	ACPI uPI-5VDIMM&3VSB	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
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FOR Promontory 1.05V_S0

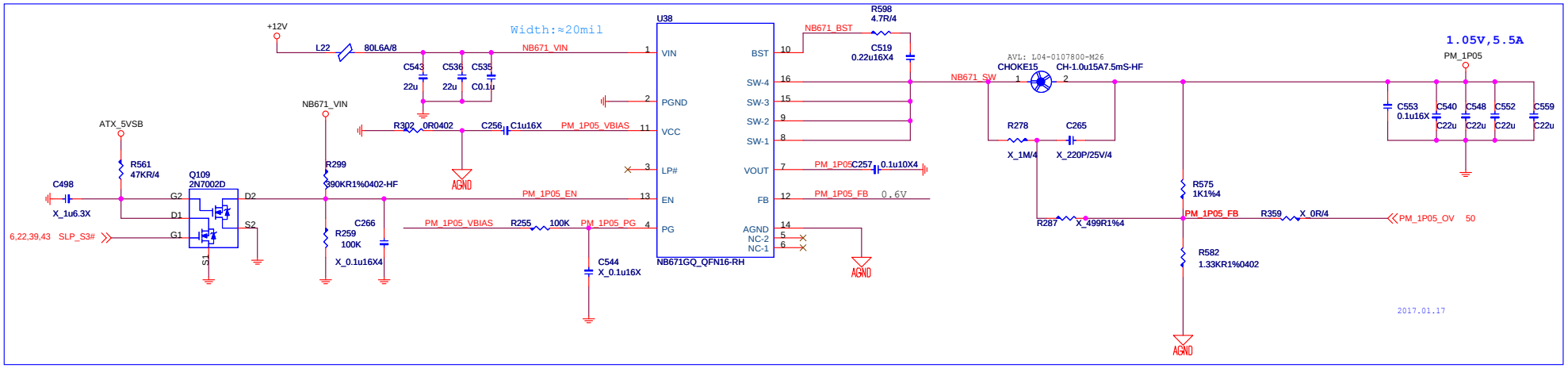
support 0V=>NB685
not support 0V=> NB681

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH≦L≦1.1664uH

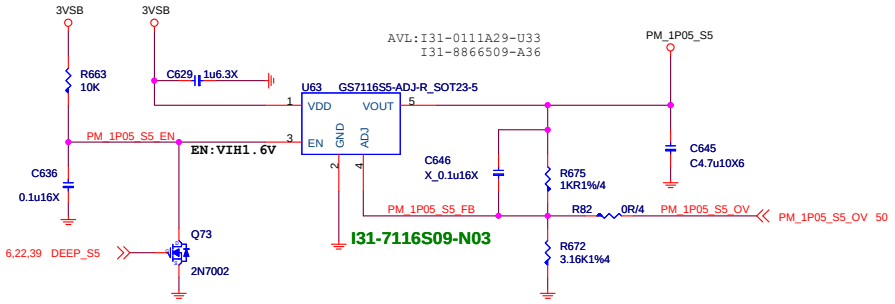
1.05V
S0:5.5A
S5:0.05A

F:500K



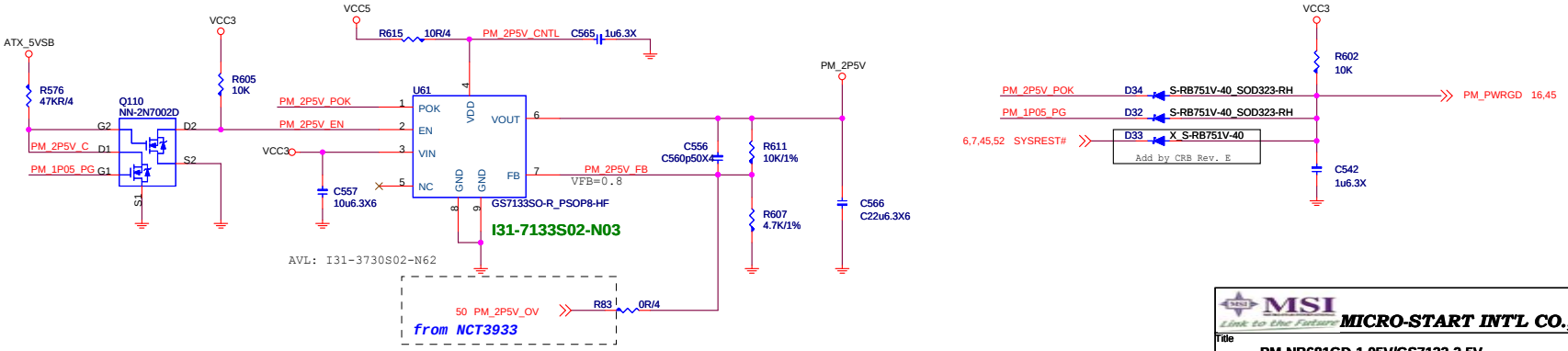
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

2.5V; 900mA



MICRO-START INTL CO.,LTD.

Title: PM-NB681GD-1.05V/GS7133-2.5V

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

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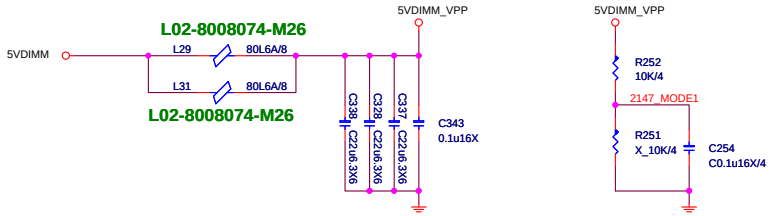
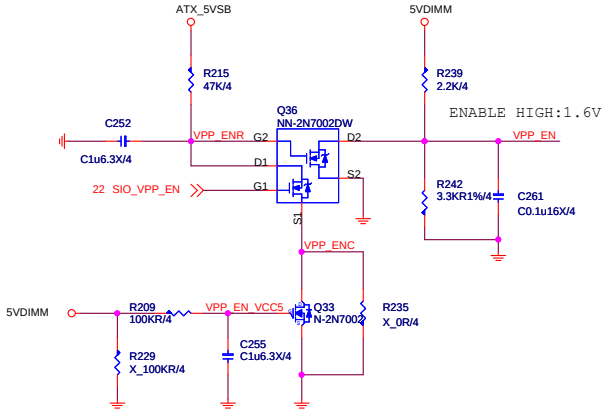
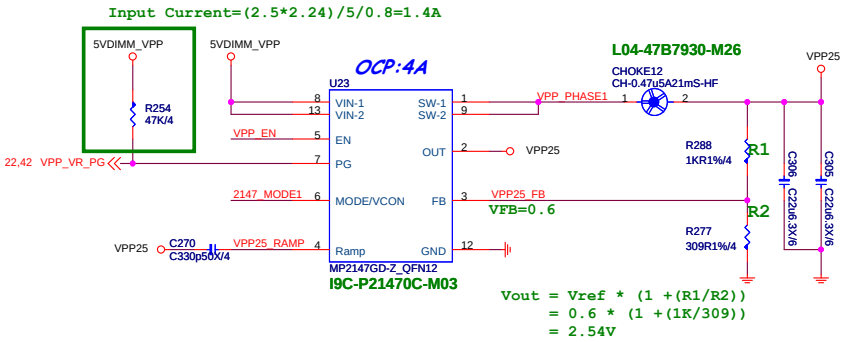
4DIMM : VPP25

2.5V@2.24A

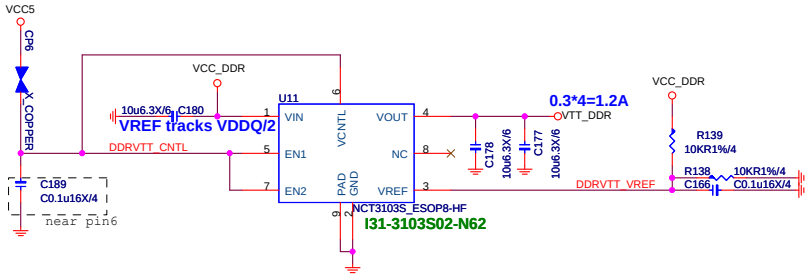


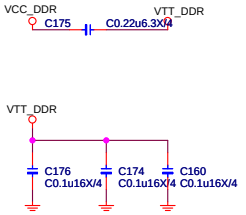




DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





MSI MICRO-START INT'L CO.,LTD.

Title: DDR PWR VPP25/VTT_DDR

Size	Document Number	Rev
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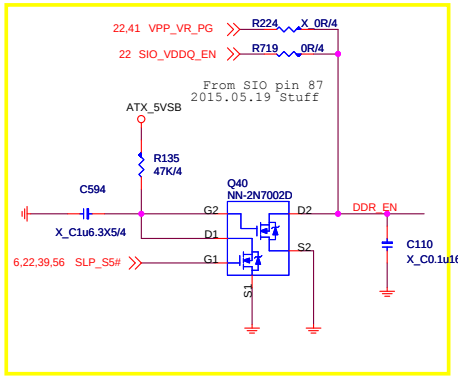
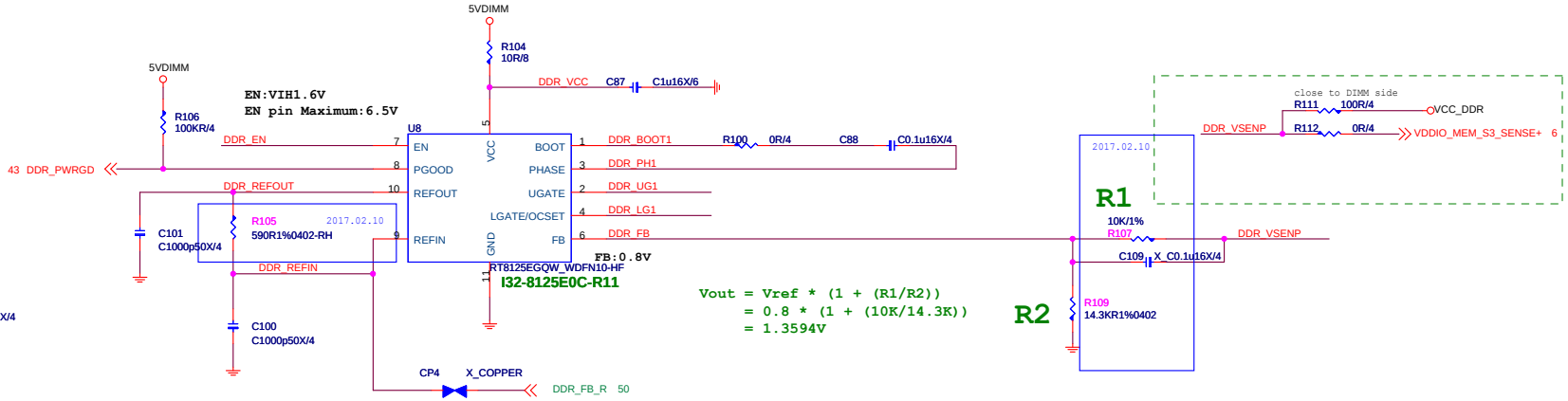
DDR4_1.2V@26.2A

15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT





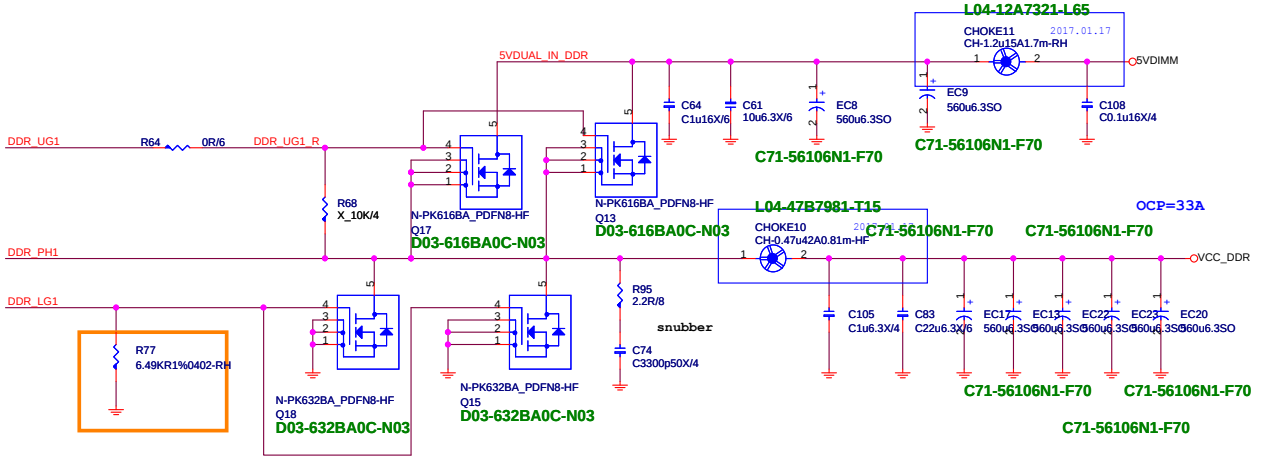
6,39,43,44,45 APU_AM4R1 D27 S-RB751V-40 DDR_EN

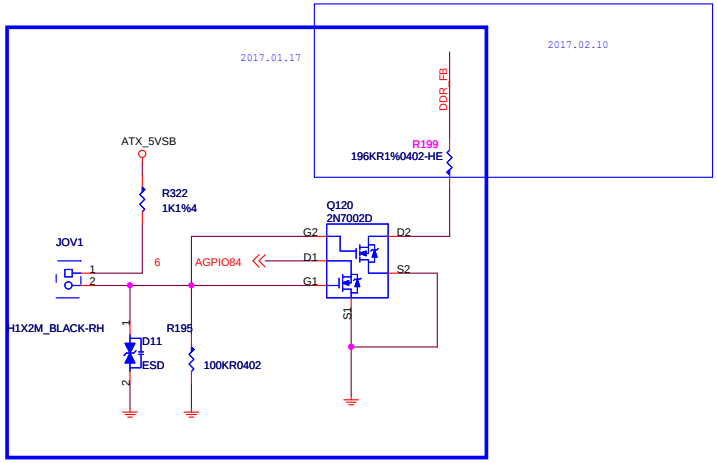
EN:VIH2V
EN pin Maximum:5.5V,RECOMMENDED:3.6V

EDC: Irms = Iout /N*SQRT{ND(1-ND)}
CORE:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=26.2/1*SQRT{0.24*[1-0.24]}
=11.189A

OCP =26.2A*1.5=39.3A
Rocs(R95)=OCP*Rdson[Low side]/10uA
=35A*1.65mohm/10uA
=5.77K

Input Current=(26.2*1.2)/5/0.8=7.86A





MSI Link to the Future	MICRO-START INTL CO.,LTD.		
Title: DDR4 8125E Power			
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FOR CPU 1.8V S5

0.5A

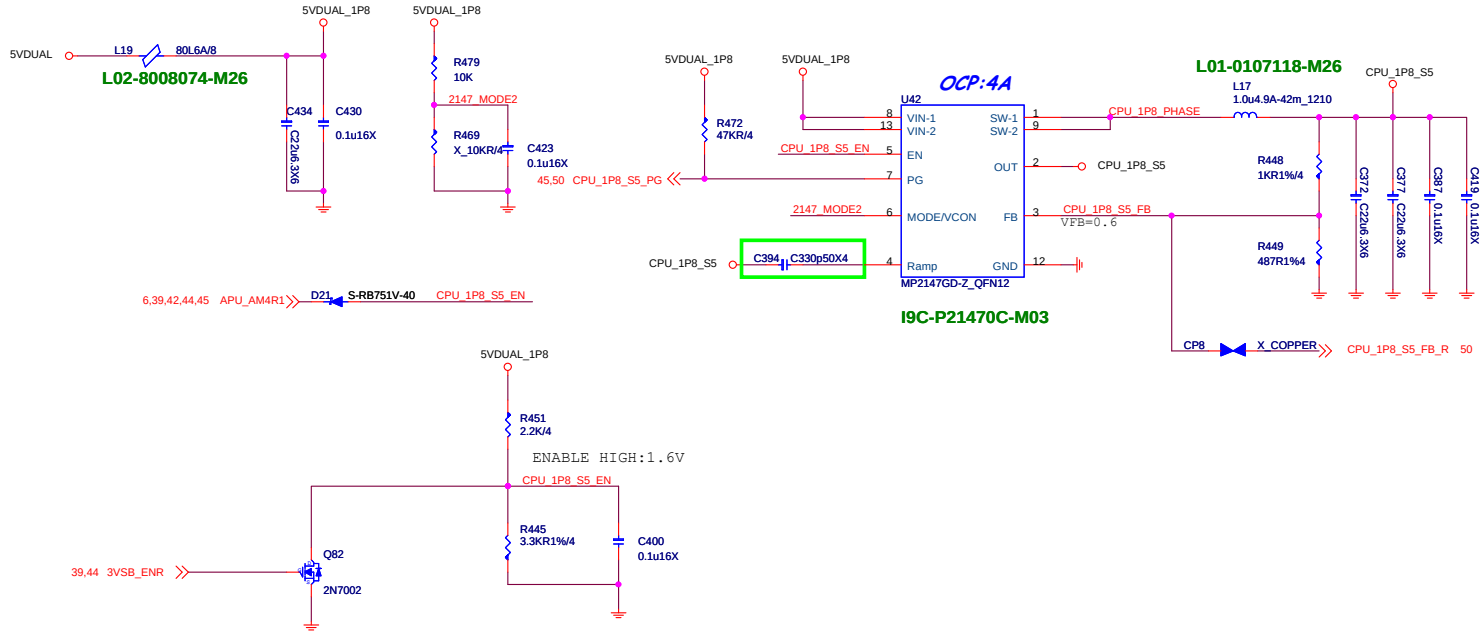
FOR VCCP_SOC_S5

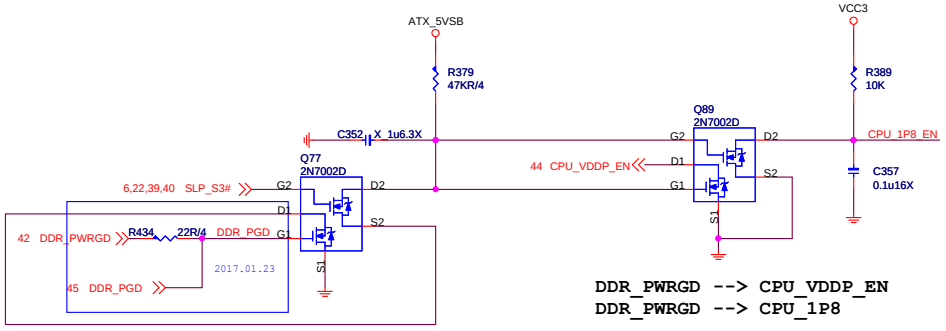
0.9A

FOR CPU 1.8V S0

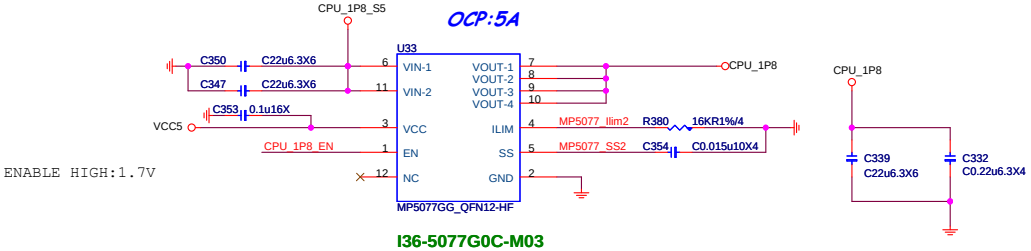
2.0A

0.5A + 2.0A + 0.9A =3.4A





DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



ENABLE HIGH:1.7V

I36-5077G0C-M03

Ilimit=(1/Rlimit)*S,S=80000,when VIN=1.8V
=(1/16)*80000=5.0375A

Tss=(1/3)*((Vout*Css)/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n)/9uA)=1ms

MICRO-START INT'L CO.,LTD.

Title: CPU Power 1P8V-MP2147		
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CPU_VDDP_S0

1.05V/0.9
S0:8.5A
OCP=12A

by layout

+12V
R406 100K1%4
EN:VIH1.6V
CPU_VDDP_EN
R418 33K/1%
C389 0.1u16X

VCC5
R437 10K
45 CPU_VDDP_PG

EN:VIH1.6V
EN pin Maximum:6.5V

6,39,42,43,45 APU_AM4R1
D20 S-RB751V-40
CPU_VDDP_EN

U41
EN
PGOOD
REFOUT
REFIN
BOOT
PHASE
UGATE
LGATE/OCSET
FB
VCC
GND
RT8125EGQW_WDFN10-HF

by layout
+12V
R494 10R/8
U6_VCC
C429 C1u16X6

CPU_VDDP_BOOT1
R484 0R/6
C440 0.1u16X25
CPU_VDDP_PH1
CPU_VDDP_UG1
CPU_VDDP_LG1
CPU_VDDP_FB
FB:0.8V

CPU_VDDP_REFOUT
C426 C1000p50X4
R453 768R1%4
CPU_VDDP_REFIN
C374 C1000p50X4
R463 4.53KR1%4
0.8V
0.684V

I32-8125E0C-R11

CPU_VDDP
R420 10R1%4
R438 1KR1%/4
CPU_VDDP_SENSE_R
R421 0R/4
CPU_VDDP_SENSE 6
C399 X_0.1u16X
R450 3.16K/1%

AM4_CPU_SEL
0:Type 0/1 1.05V
1:Type 2/3 0.9V

6,31,45,50 TYPE1_CPU_SEL
Q86 NN-2N7002DW
G2 D2
16 PM_GPIO_R9 D1
G1 S2
S1

50 CPU_VDDP_OV
CP25 X_COPPER

PM_GPIO_R9
1:Type 0/1 1.05V
0:Type 2/3 0.9V

EDC: Irms = Iout /N*SQRT{ND(1-ND)}
CORE:
D=Vout/Vin=1.05/12=0.0875
N=Phase number=1
=8.5/1*SQRT{1*0.0875*[1-1*0.0875]}
=2.4A

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.8 * 0.282566
= 3.46A

L04-47B7930-M26

CHOKE14
CH-0.47u5A21mS-HF
12VCC_IN
+12V
C461 C1u16X6
C460 22u16X8
EC11 270u16SO
C446 0.1u16X

C71-2711891-F70

CPU_VDDP_UG1
R508 0R/6
CPU_VDDP_UG1_R
R500 X_10KR/4
N-PK616BA_PDFN8-HF
Q97

CPU_VDDP_PH1

CPU_VDDP_LG1
R475 5.1K/1%/4
N-PK632BA_PDFN8-HF
Q96

OCPSET:min 5Kohm
OCP
=(R475*10uA)/DCR
=(5.1k*10uA)/3.3m
=15.45A

CHOKE13
1.0u15A7.5mS-HF
CPU_VDDP
R482 X_2.2R/8
snubber
C437 X_C3300p50X4

L04-01072H0-T15

C334 1u6.3X
C425 C22u6.3X6
EC31 560u6.3SO
EC32 560u6.3SO

OCP=12A
1.05V,8.5A

C71-56106N1-F70

TYPE0_CPU_SEL:
1:TYPE 0
0:TYPE 2

CPU_VDDP_EN:
0:TYPE 2
1:TYPE 0

6,45 TYPE0_CPU_SEL
Q92 NN-2N7002DW
VDDP_SEL
CPU_VDDP_EN
CPU_VDDP_EN 43
6,31,45,50 TYPE1_CPU_SEL

TYPE1_CPU_SEL:
0:TYPE 0
1:TYPE 2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

CPU_VDDP_S5

VDDP_S5 1.05V/0.9
S5:1A

5VDUAL
3VSB
3VSB
L20 80L6A/8
R501 X_10KR/4
R502 10K
C439 C22u6.3X6
U45
VDDP_VSB_VIN
VDDP_VSB_EN
VDDP_VSB_PG
45 VDDP_VSB_PG
Internal Pull-Up 500K
VIN
EN
PG
PGND
AGND
SW
OUT
FB
MP2143DJ
VDDP_VSB_PHASE
VDDP_VSB_FB

L18 1.0u6.3A_1210-HF
CPU_VDDP_S5
R489 1KR1%/4
R488 2KR1%/4
C412 C22u6.3X6
C421 C22u6.3X6
C427 C0.22u6.3X4

I9C-2143D09-M03

6,39,42,43,45 APU_AM4R1
D28 S-RB751V-40
VDDP_VSB_EN
C390 X_0.1u16X
39,43 3VSB_ENR
Q98 2N7002

ATX_5VSB
R490 47KR/4
Q95 NN-2N7002DW
C436 0.1u16X
6,31,45,50 TYPE1_CPU_SEL
AM4_CPU_SEL
0:Type 0/1
1:Type 2/3
VDDP_VSB_FB
R464 3.83KR1%4

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

MSI Link to the Future MICRO-START INTL CO.,LTD.

Title	CPU Power VDDP-RT8125E	
Size: Custom	Document Number: MS-7A38	Rev: 6.0
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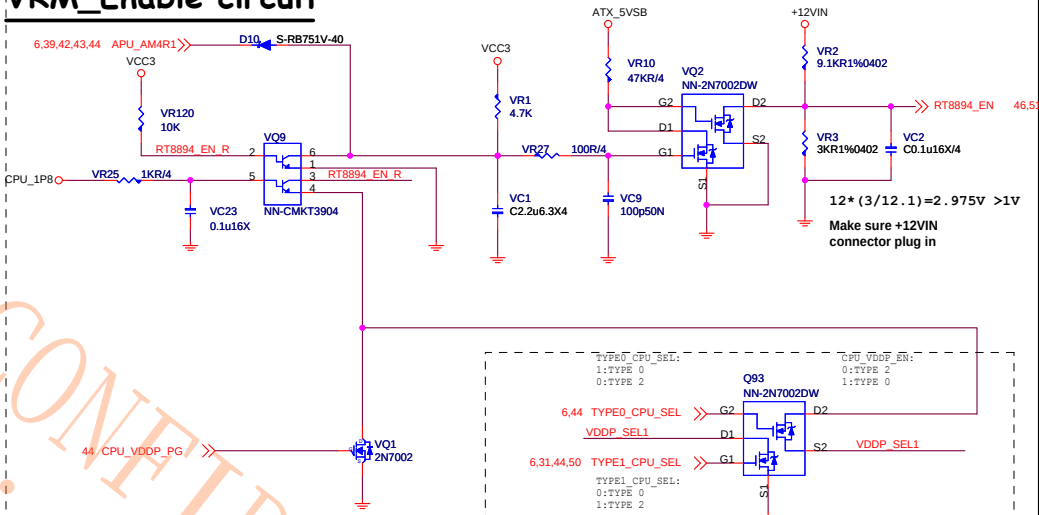
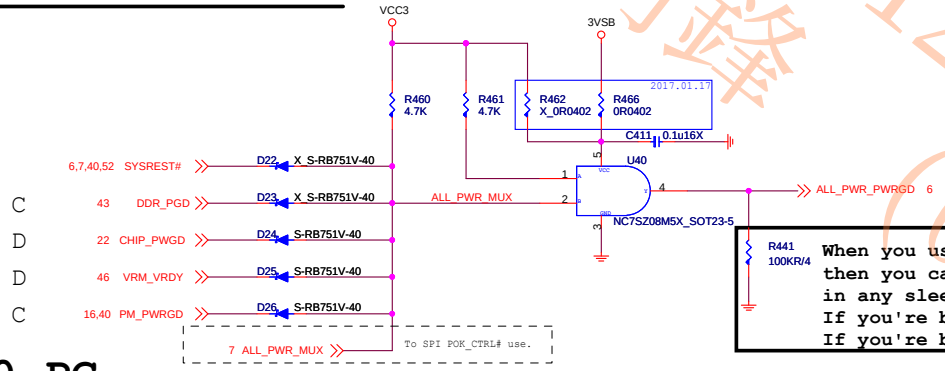
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

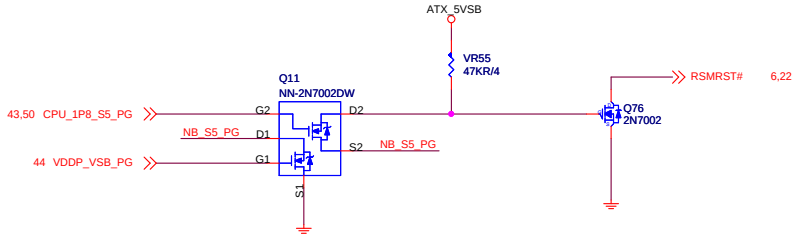


R441 100KR/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MSI MICRO-START INT'L CO.,LTD.

Title: CPU Power Connector/PWRGD

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

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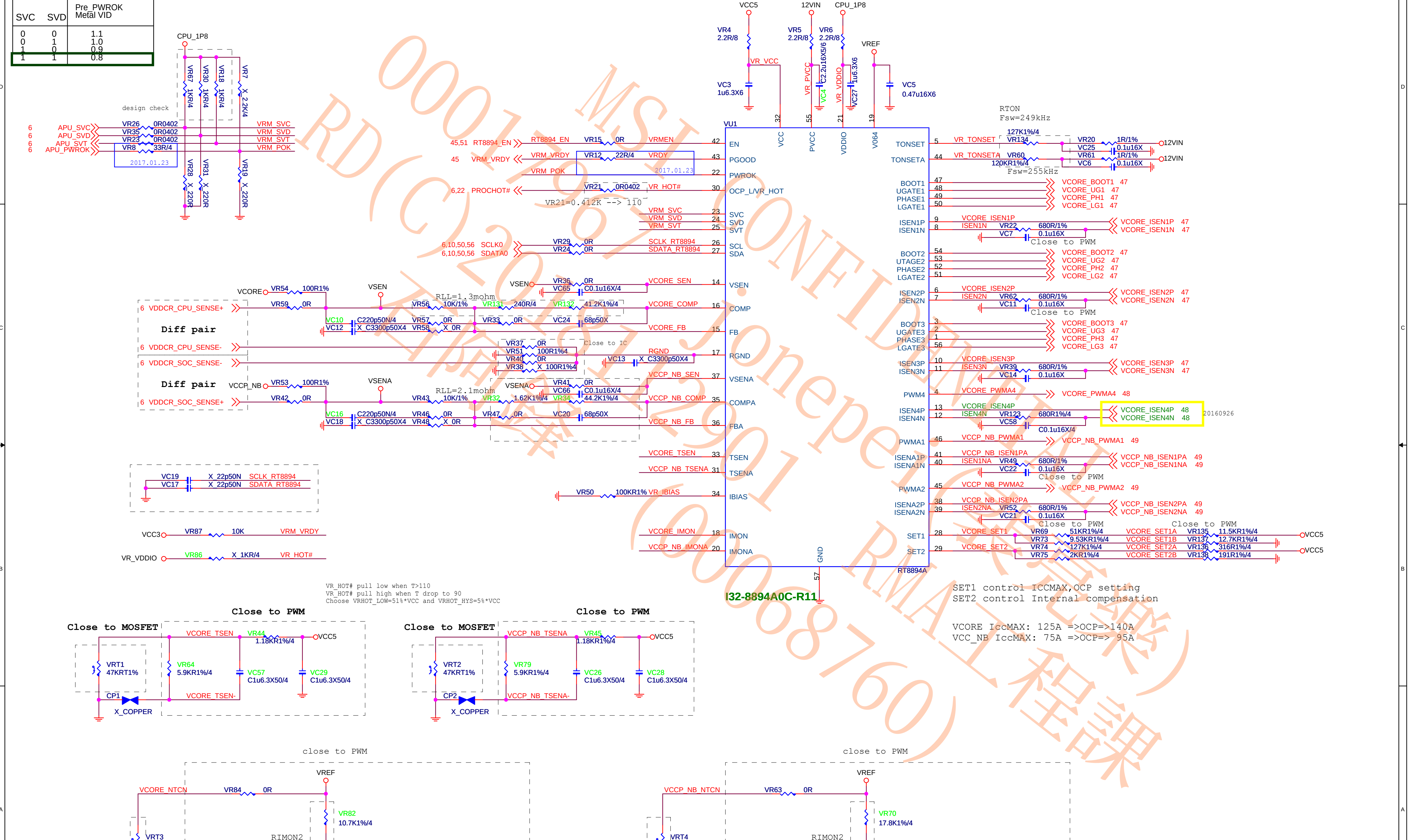
Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



MICRO-START INT'L CO.,LTD.

Title: CPU Power RT8894 4+2 Phase

Size: Custom | Document Number: MS-7A38 | Rev: 6.0

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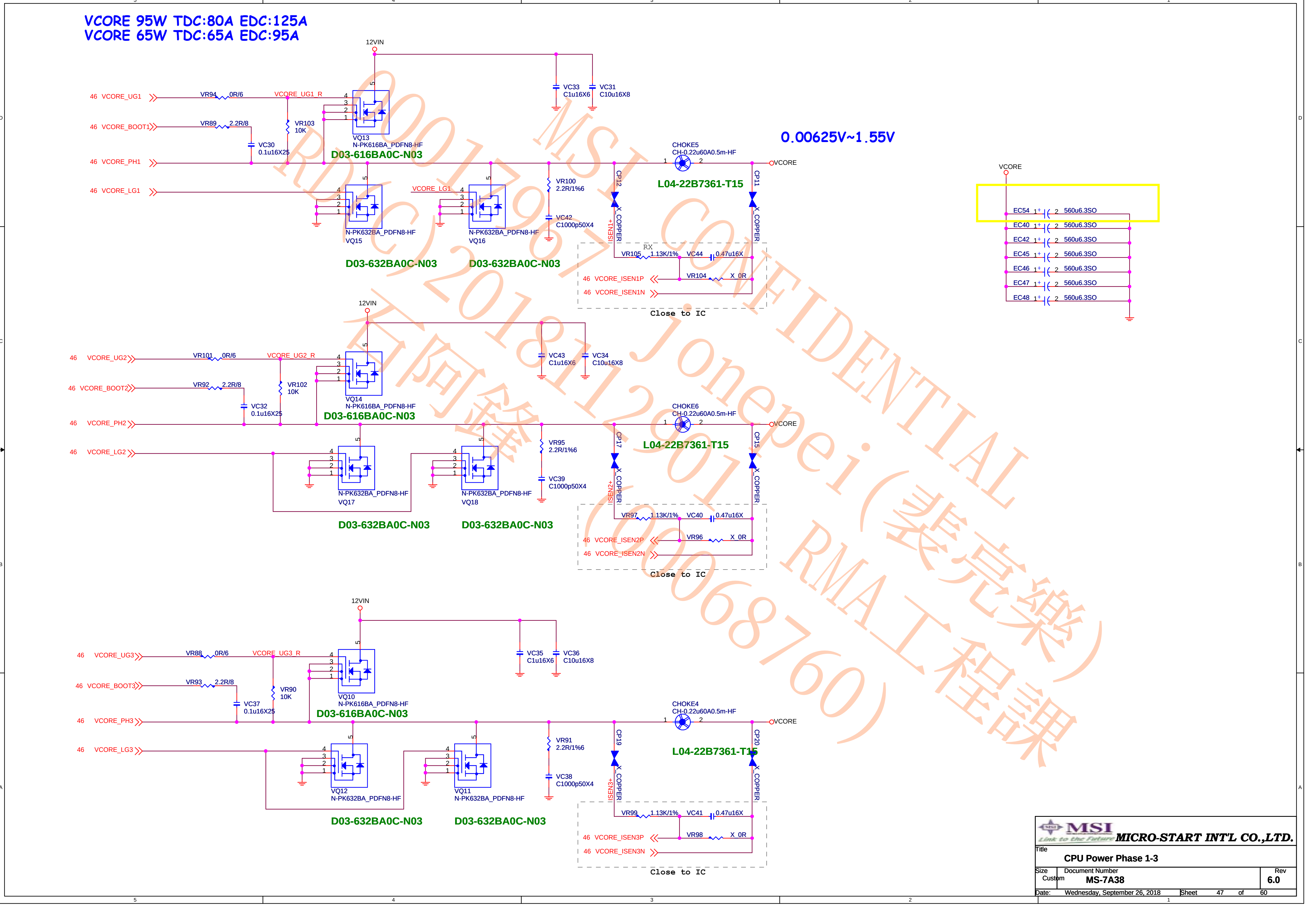
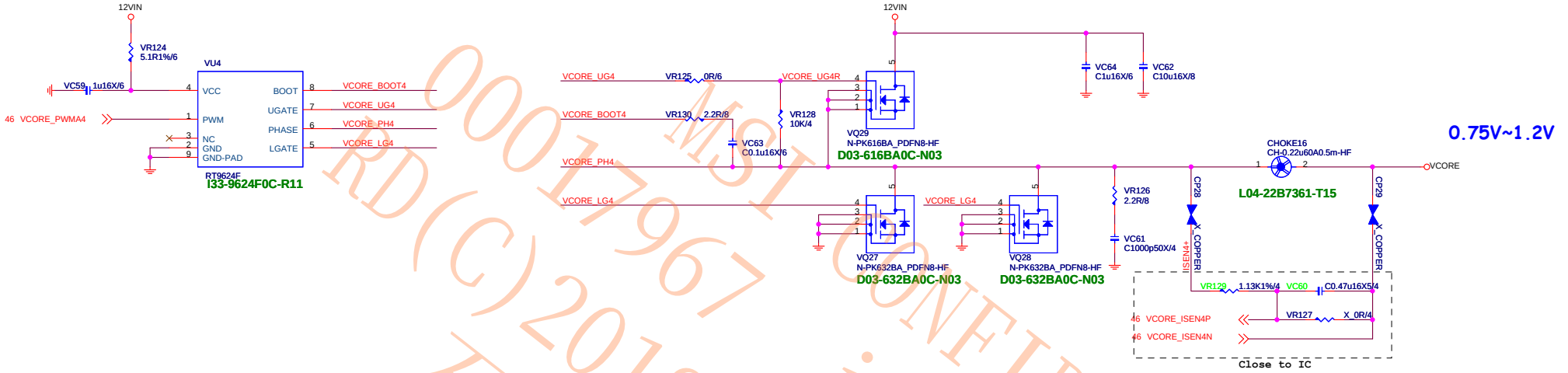
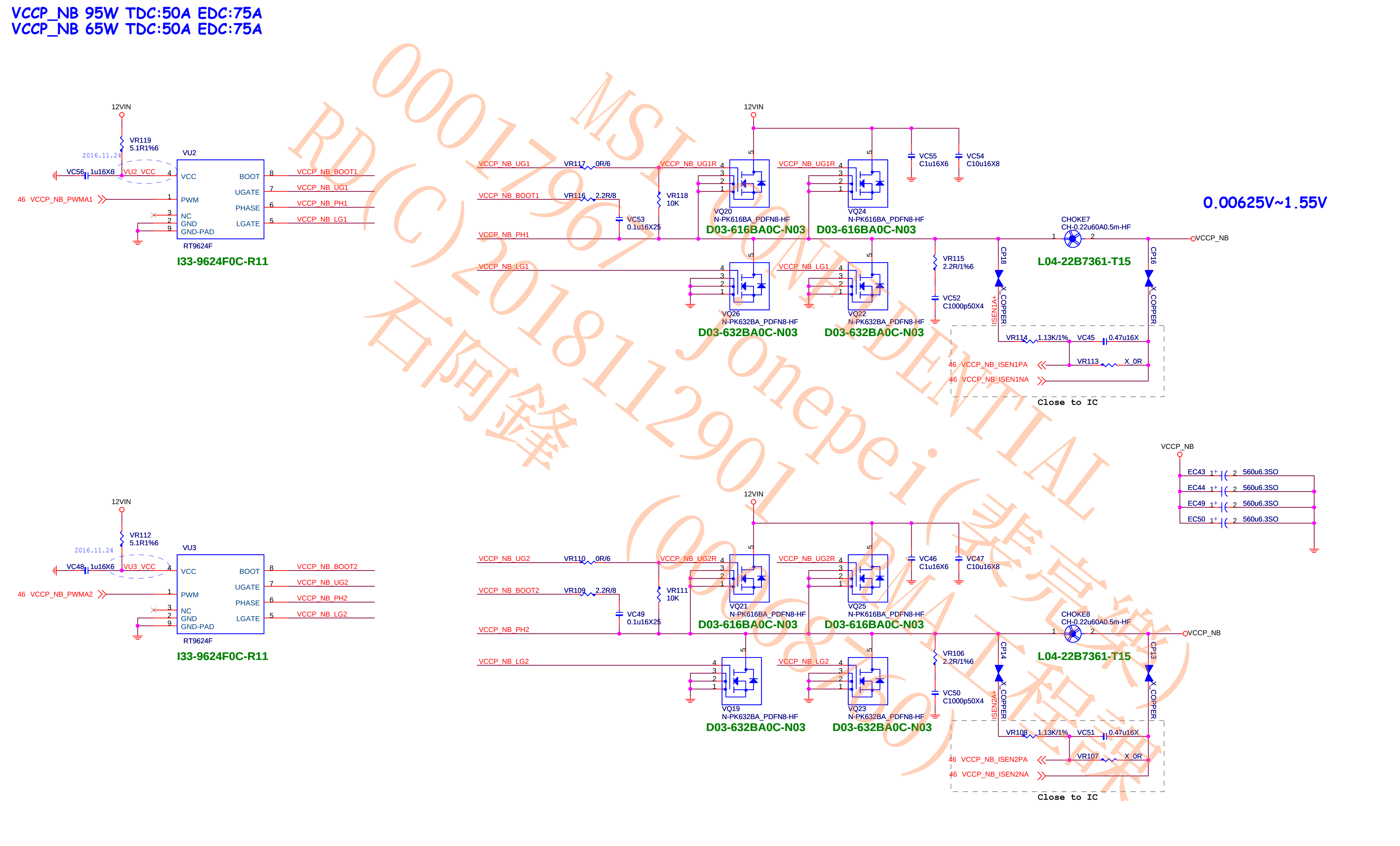

VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A
0.00625V~1.55V
12VIN
46 VCORE_UG1
46 VCORE_BOOT1
46 VCORE_PH1
46 VCORE_LG1
VR94 0R/6
VCORE_UG1_R
VR89 2.2R/8
VR103 10K
VC30 0.1u16X25
VQ13 N-PK616BA_PDFN8-HF
D03-616BA0C-N03
VC33 C1u16X6
VC31 C10u16X8
CHOKE5 CH-0.22u60A0.5m-HF
L04-22B7361-T15
VCORE
VCORE_LG1
VR100 2.2R/1%6
VC42 C1000p50X4
N-PK632BA_PDFN8-HF
VQ15
VQ16
D03-632BA0C-N03
CP12
CP11
X_COPPER
ISEN1+
RX
VR105 1.13K/1%
VC44 0.47u16X
VR104 X_0R
46 VCORE_ISEN1P
46 VCORE_ISEN1N
Close to IC
VCORE
EC54 560u6.3SO
EC40 560u6.3SO
EC42 560u6.3SO
EC45 560u6.3SO
EC46 560u6.3SO
EC47 560u6.3SO
EC48 560u6.3SO
46 VCORE_UG2
46 VCORE_BOOT2
46 VCORE_PH2
46 VCORE_LG2
VR101 0R/6
VCORE_UG2_R
VR92 2.2R/8
VR102 10K
VC32 0.1u16X25
VQ14 N-PK616BA_PDFN8-HF
VC43 C1u16X6
VC34 C10u16X8
CHOKE6 CH-0.22u60A0.5m-HF
VR95 2.2R/1%6
VC39 C1000p50X4
VQ17
VQ18
CP17
CP15
ISEN2+
VR97 1.13K/1%
VC40 0.47u16X
VR96 X_0R
46 VCORE_ISEN2P
46 VCORE_ISEN2N
46 VCORE_UG3
46 VCORE_BOOT3
46 VCORE_PH3
46 VCORE_LG3
VR88 0R/6
VCORE_UG3_R
VR93 2.2R/8
VR90 10K
VC37 0.1u16X25
VQ10 N-PK616BA_PDFN8-HF
VC35 C1u16X6
VC36 C10u16X8
CHOKE4 CH-0.22u60A0.5m-HF
VR91 2.2R/1%6
VC38 C1000p50X4
VQ12 N-PK632BA_PDFN8-HF
VQ11 N-PK632BA_PDFN8-HF
CP19
CP20
ISEN3+
VR99 1.13K/1%
VC41 0.47u16X
VR98 X_0R
46 VCORE_ISEN3P
46 VCORE_ISEN3N
MSI Link to the Future
MICRO-START INT'L CO.,LTD.
Title
CPU Power Phase 1-3
Size Custom
Document Number MS-7A38
Rev 6.0
Date: Wednesday, September 26, 2018
Sheet 47 of 60



MSI MICRO-START INT'L CO.,LTD.

Title: CPU Power Phase 4		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
Date: Wednesday, September 26, 2018	Sheet 48 of 60	



MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Phase 1-2

Size	Document Number	Rev
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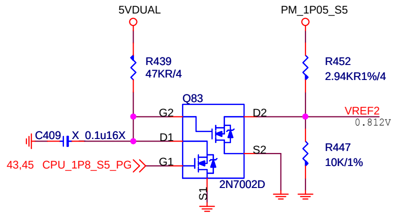
FOR VCCP_SOC_s5
0.9A

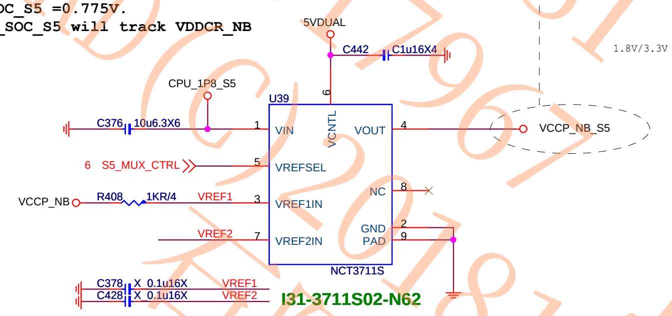
TYPE0 Only

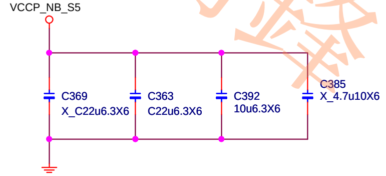
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

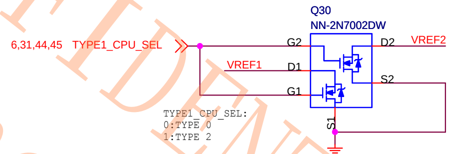
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0









CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

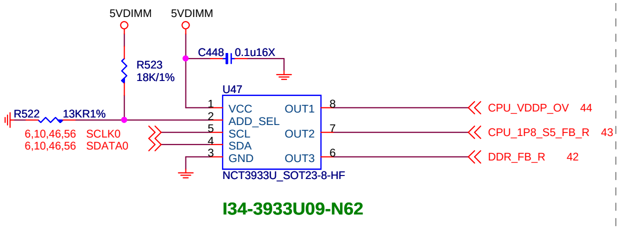
Over Voltage Control IC

UPI VOLTAGE CONSOLE

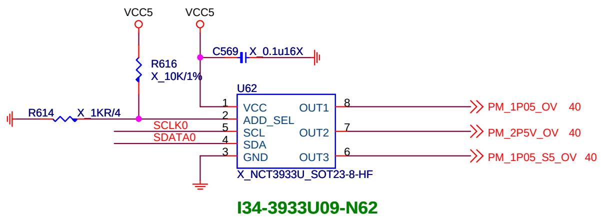
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

埃獲襘溃癸 Tヴ：腊 ， 玥ぃ NCT3933鈹柞襘溃匡兜

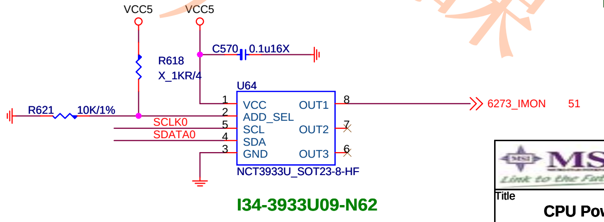
0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



0x2A:RH=OPEN,RL=10K



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	CPU Power NB Switch/NCT3933
Size	Custom
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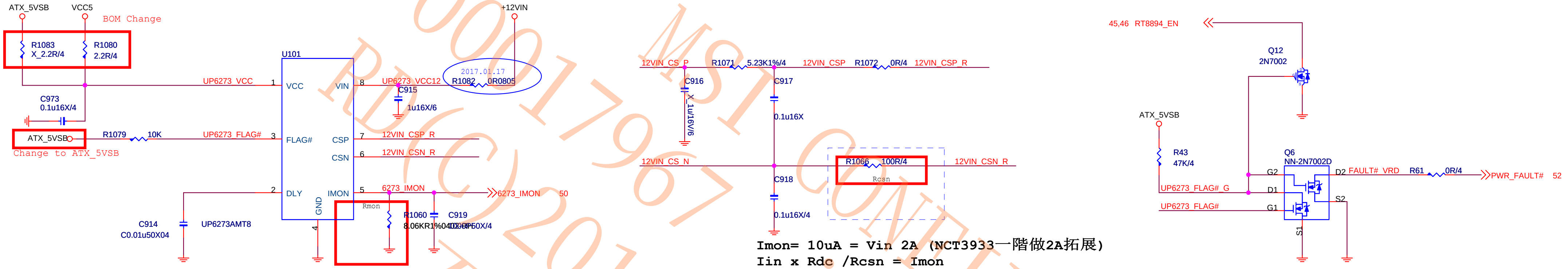
uP6273 CURRENT SENSE

VCORE EDC MAC 125A

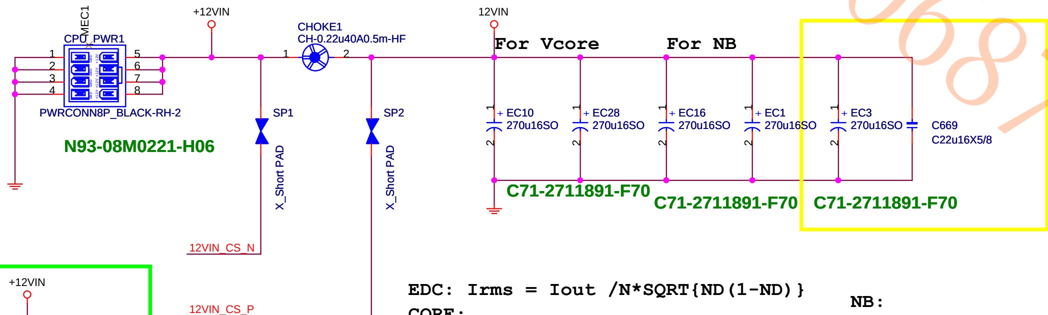
NB EDC MAX75A



Imon= 10uA = Vin 2A (NCT3933一階做2A拓展)
Iin x Rdc /Rcsn = Imon
2A x 0.5m / Rcsn = 10uA
Rcsn=100 ohm

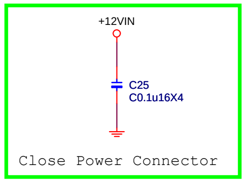
Vmon = 1.2V觸發ocp
Vmon=(Iin x Rdc / Rcsn) x Rmon
1.2V=30 x 0.5m /100 x Rmon
Rmon=8K

CPU POWER CONNECTOR



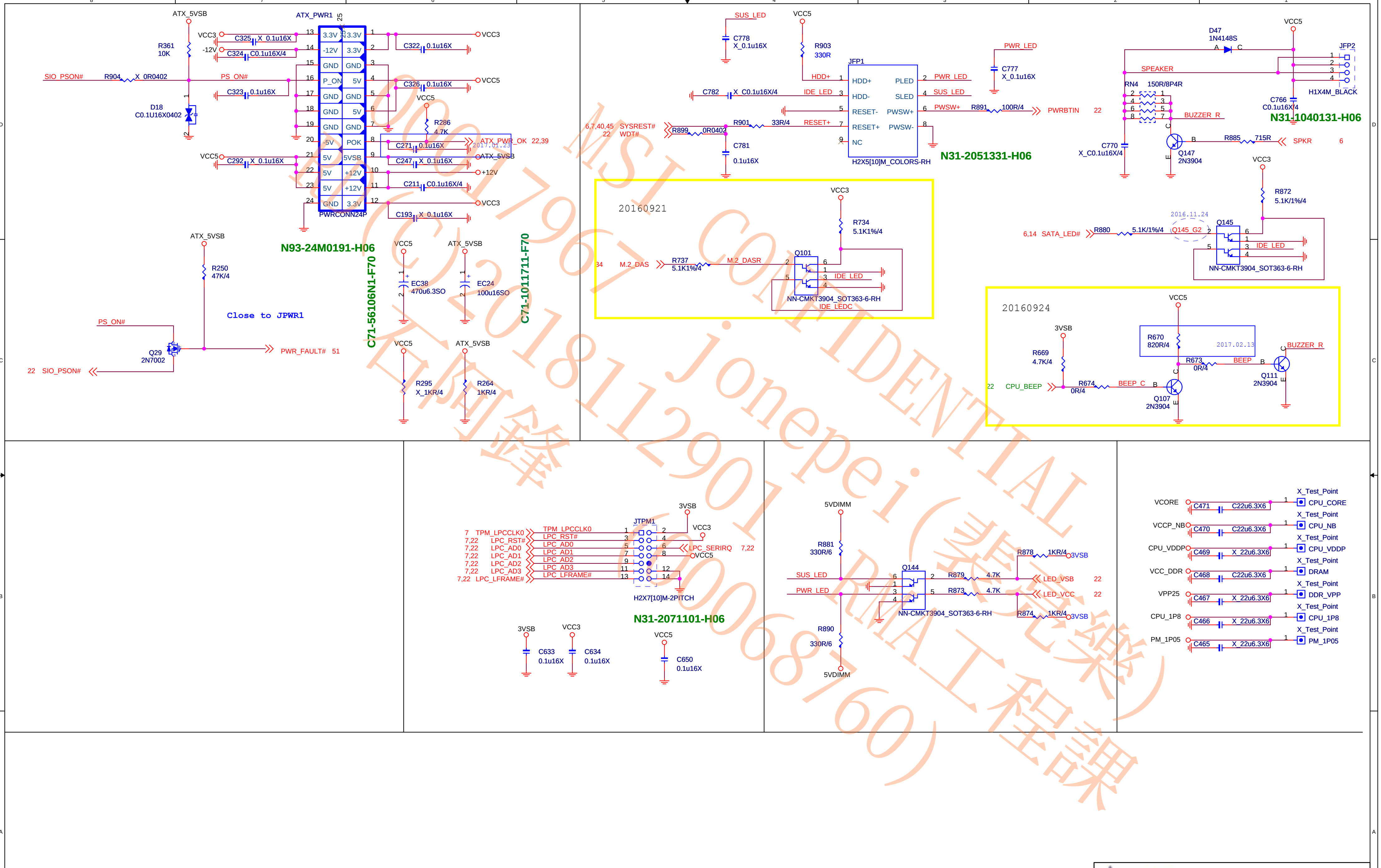
TDC: Irms = Iout /N*SQRT{ND(1-ND)}
CORE:
D=Vout/Vin=1.5/12=0.125
N=Phase number=4
=80/4*SQRT{4*0.125*[1-4*0.125]}
=10A

NB:
D=Vout/Vin=1.2/12=0.1
N=Phase number=2
=65A/2*SQRT(2*0.1*(1-2*0.1))
=13A



EDC: Irms = Iout /N*SQRT{ND(1-ND)}
CORE:
D=Vout/Vin=1.5/12=0.125
N=Phase number=4
=125/4*SQRT{4*0.125*[1-4*0.125]}
=15.625A

NB:
D=Vout/Vin=1.2/12=0.1
N=Phase number=2
=75A/2*SQRT(2*0.1*(1-2*0.1))
=15A



MSI MICRO-START INT'L CO.,LTD.

Title: ATX/Front Panel

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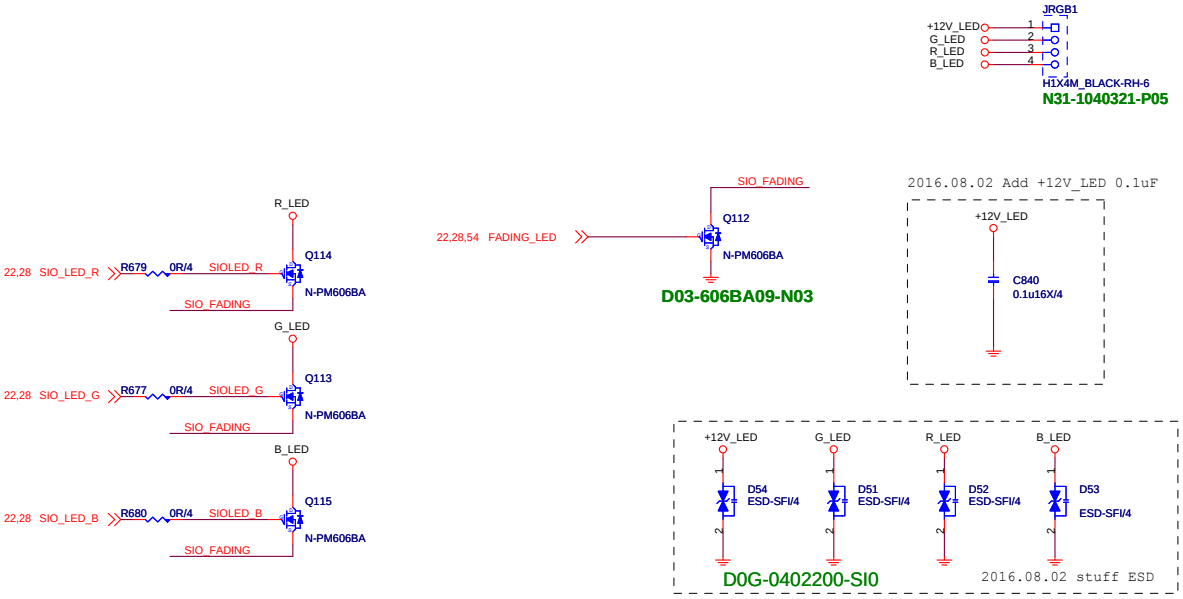
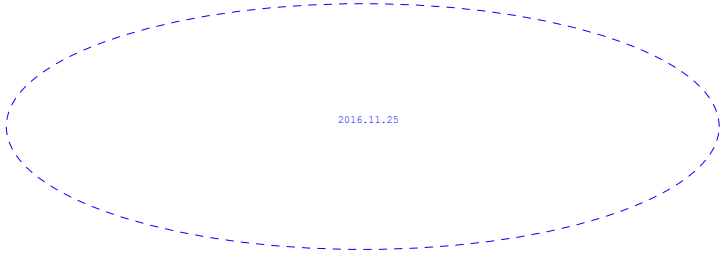


FCH LED Place under Heat-sink



LED
翔 : D0C-040S600-E07
フ : D0C-040S300-E07

MSI MICRO-START INT'L CO.,LTD.

Title: ALL LED		
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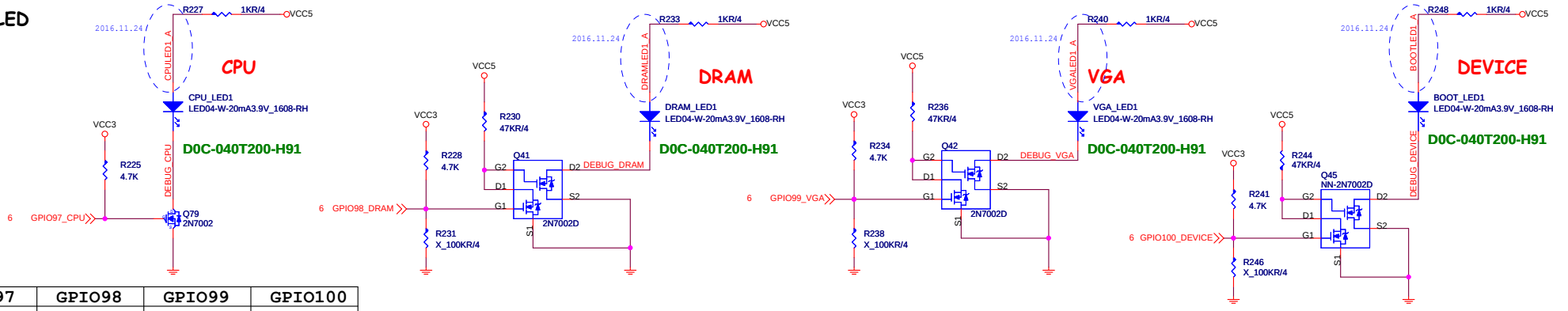
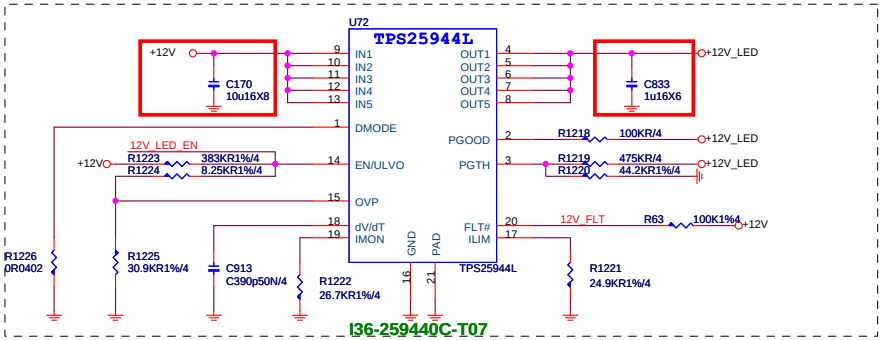
EZ Debug LED



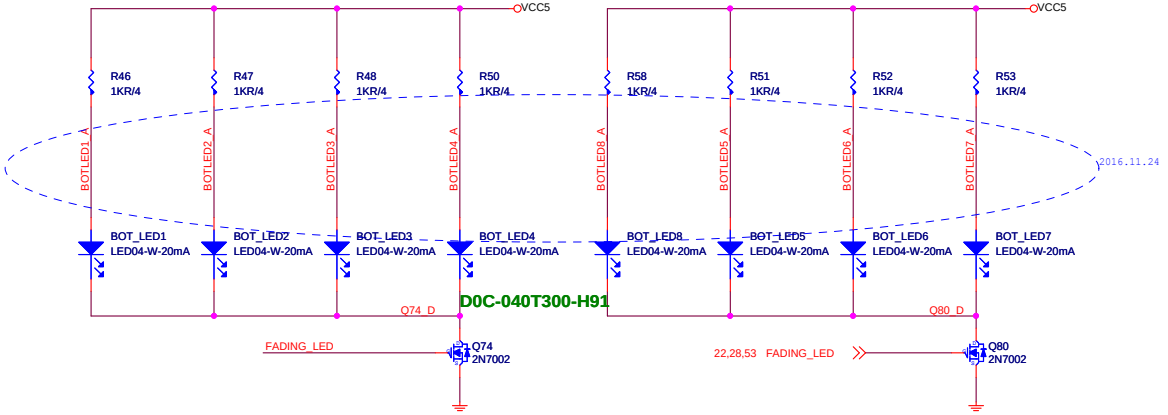
LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獵	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED Control by SIO

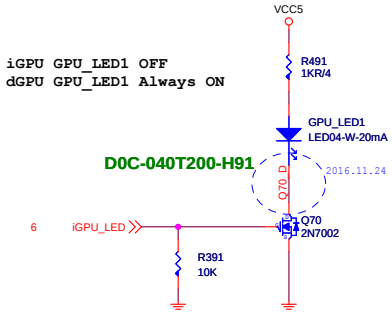
2016.07.06 Use TPS25944L



Bottom LED



AM4 APU Detect LED Circuit



MSI MICRO-START INTL CO.,LTD.

Title: ALL LED Control

Size	Document Number	Rev
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HEAT SINK

2017.01.17

PM_HS1

MEC1

MEC2

HS-0436-2408F

E31-0408930-K08

Long

MOS_HS1

MEC2

MEC1

HS-0504270-RH

E31-0504810-K08

CPU Socket

CPU2

E95-0000021-C22

RETENTION MODULE

E95-0000022-C22

Simulation

2016.12.02

X_JS3

SIM1

X_PIN1*2

VCC5

X_JS4

SIM2

X_PIN1*2

VCC_DDR

VCC_DDR

MANUAL PART

UEFI1

G51-M1SPXXA-A09

G51-M1SPXXA-A09

搞不懂

BAT1_X1

BAT-CR2032-RH

D06-0100101-P01

MKT1

G51-M1SPK31-Q13

G51-M1SPN80-Q13

cFosSoftware

X_Y02-MU00170-CFO

Y02-MU00170-CFO

HDMI_LA1

Label

HDMI

HDMI LABEL

Y01-RHDMI03-000

NAHIMIC_LA1

Label

HDMI

NAHIMIC LABEL

Y02-MU00100-NAH

XSPLIT_LA1

Label

HDMI

XSPLIT LABEL

Y02-MA00401-XSP

SSE_LA1

Label

HDMI

X_SSE LABEL

Y02-MA00101-SSE

PCB1

7A38-4.0

PDO-07A380A-E48,腦地,腳 塑吹邻紅(MSIS)

PDO-07A380A-G37,弘e-襄 ,腳 塑吹邻紅(MSIS)

REF1

OPT

X_FCH

REF2

OPT

X_MKT

Optics Orientation Holes

MH4

MH6

MH5

MH7

MH1

MH2

MH3

X_MH001

2017.01.17

5010

5020

FM1

FM2

FM3

FM4

X_FM120

FM5

FM6

FM8

FM7

OPT	Configure	BOM	Function
		601-7A38-A01	XXXX

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: BOM Option

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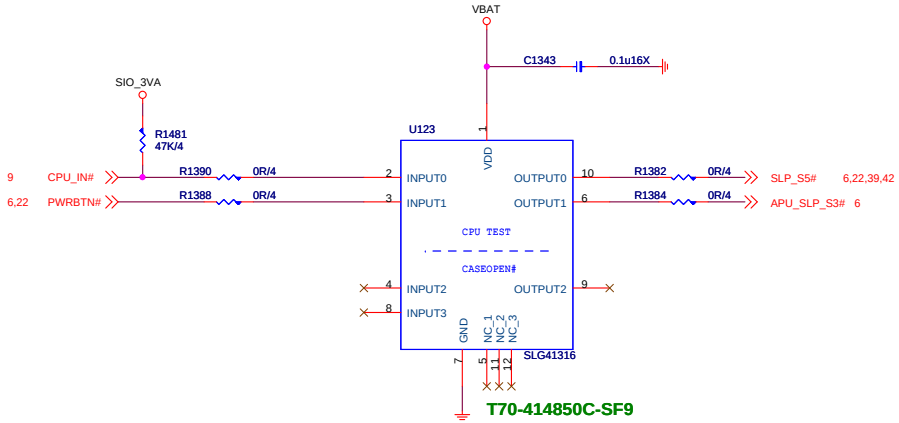
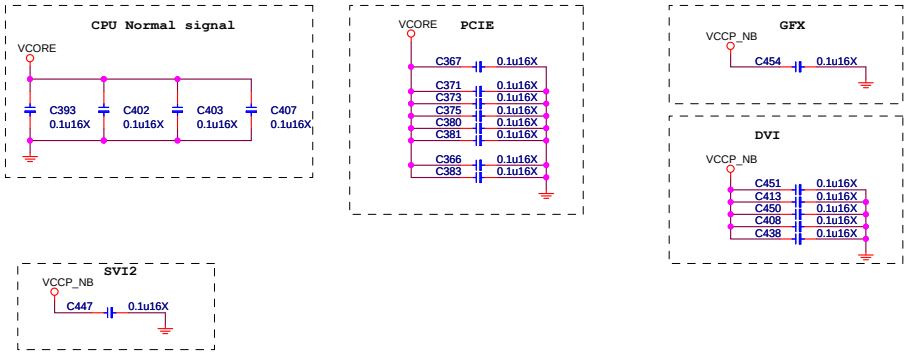
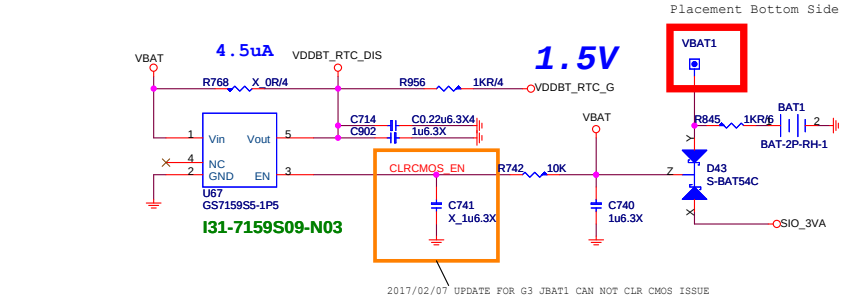
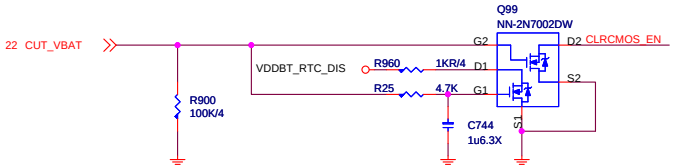


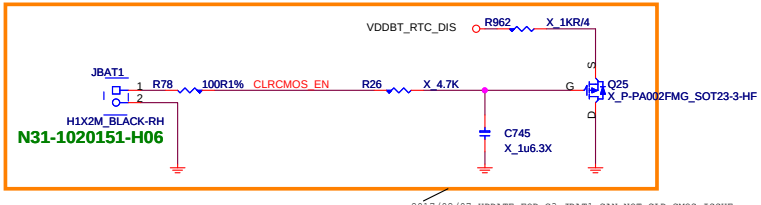
Moat Cap

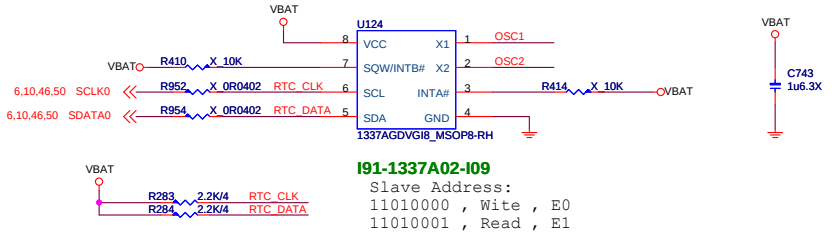


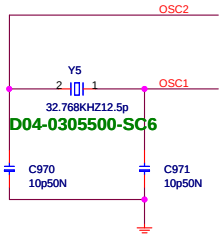
RTC & Clear CMOS Circuit

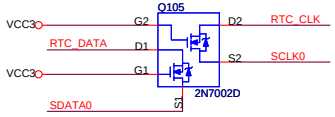












MICRO-START INT'L CO.,LTD.

Title: RTC Circuit / Moat Cap		
Size: Custom	Document Number: MS-7A38	Rev: 6.0
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