MS-7A40 Ver:21.

CPU:
AMD AM4

System Chipset:
Promontory B450
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

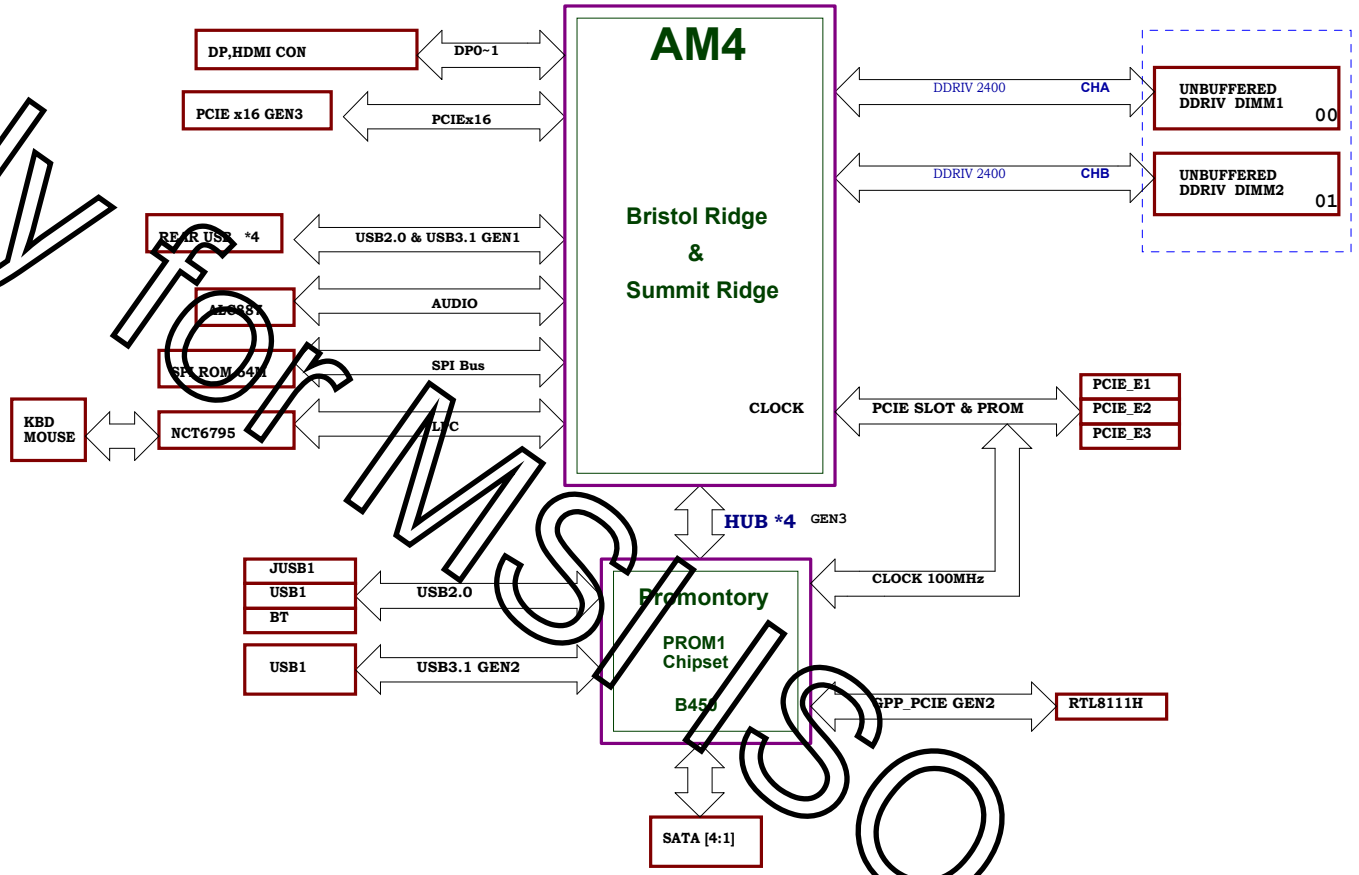
VRM
IR35201 6+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1

OCP IC:
RT9553

FUSION BLOCK DIAGRAM



MICRO-START INT'L CO.,LTD.

Title: Block Diagram		
Size: Custom	Document Number: MS-7A40	Rev: 21
Date: Monday, July 13, 2020	Sheet 1 of 55	

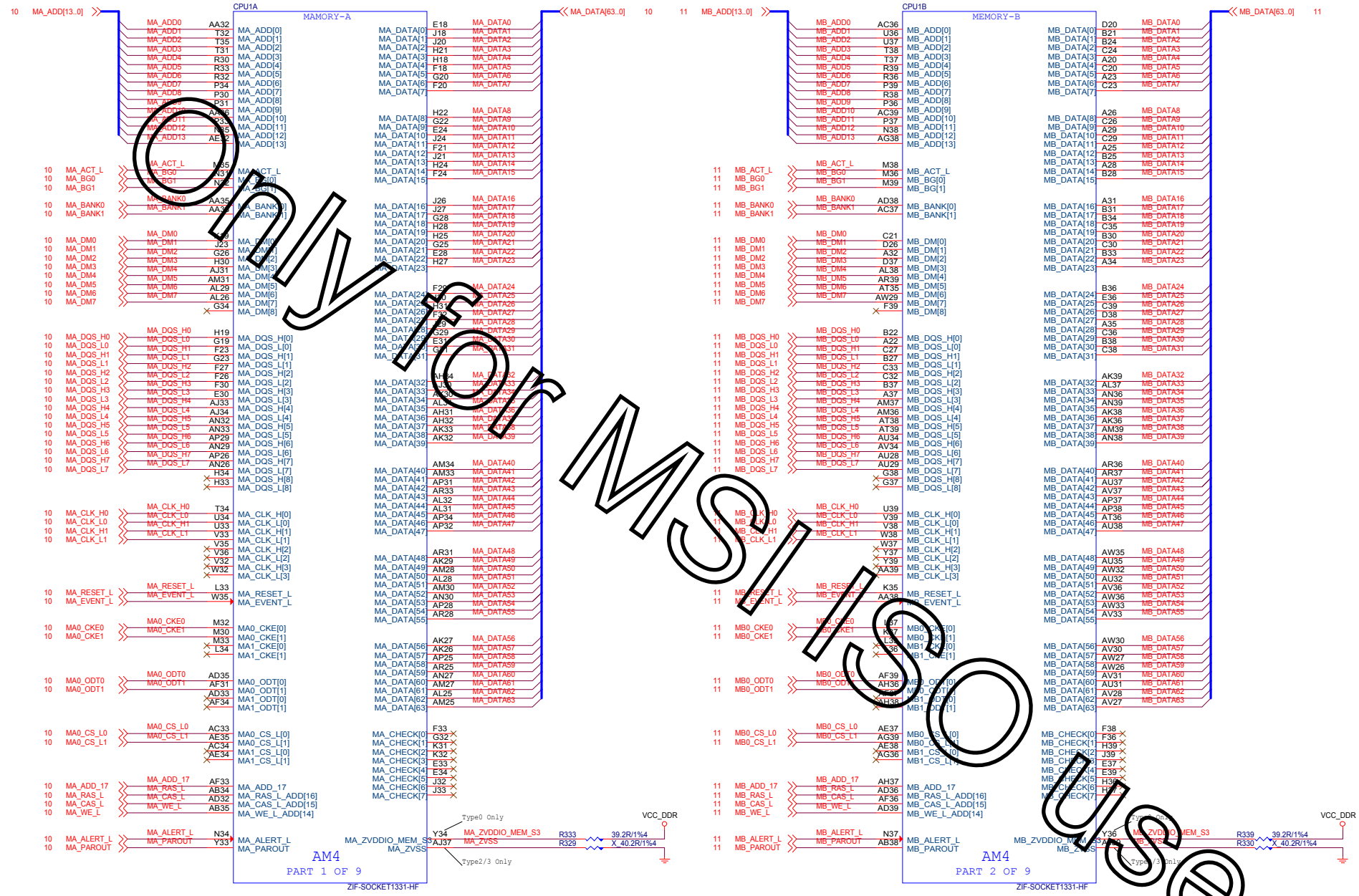
AMD AM4

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: COVER SHEET

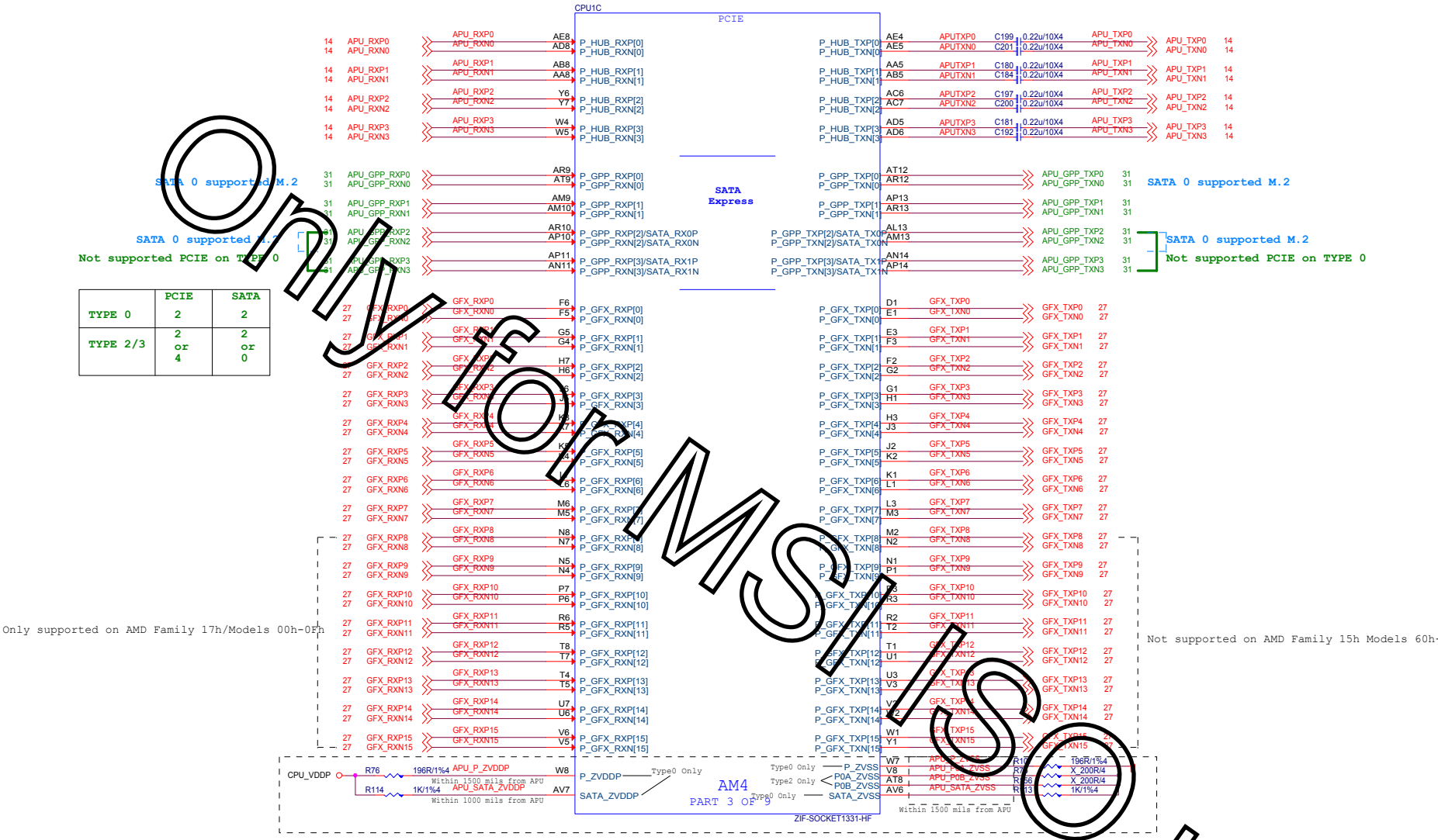
Size: Custom | Document Number: MS-7A40 | Rev: 21

Date: Monday, July 13, 2020 | Sheet 2 of 55



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

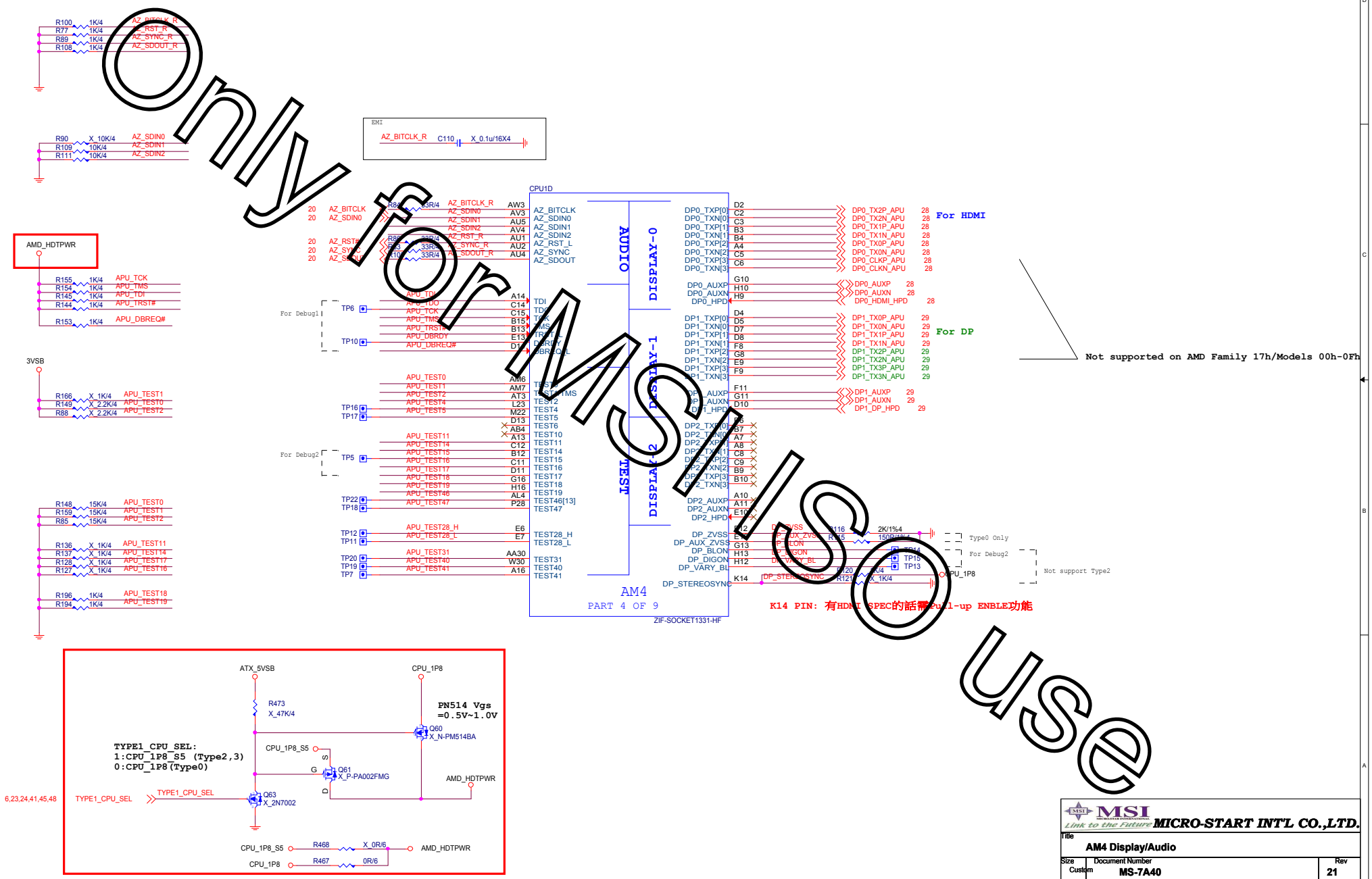
Title	AM4 DDR4 I/F	
Size: Custom	Document Number: MS-7A40	Rev: 21
Date: Monday, July 13, 2020	Sheet 3 of 55	



	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	AM4 PCIE/SATAE	
Size: Custom	Document Number: MS-7A40	Rev: 21
Date: Monday, July 13, 2020	Sheet 4 of 55	



MICRO-START INT'L CO.,LTD.

Title: AM4 Display/Audio

Size: Custom | Document Number: MS-7A40 | Rev: 21

Date: Monday, July 13, 2020 | Sheet 5 of 55

AM4 CPU TYPE Circuit

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP

CORETYPE0
0:BR/SR
1:RV/ZP

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

Layout:Place x'tal within 1.5 inch of APU

Change by CRB rev. E

Follow CRB

Within 500mils

For K TYPE FAN

GPIO97~100 for Debug LED

Modify USB_OC# circuit

IB=(Vcc3-Vbe)/10k
(3.3-0.95)/10k=0.235mA

IC=(VCC2-Vce)/10k
(3.3-0.2)/10k=0.31mA

PN514 Vgs
=0.5V~1.0V

PN514 Vgs
=0.45V~1.2V

AMD Hardware Validated Boot (HVB)
0:Enable
1 or NC:Disable

by check list

MICRO-START INT'L CO.,LTD.

Title	AM4 SVI/ACPI/GPIO
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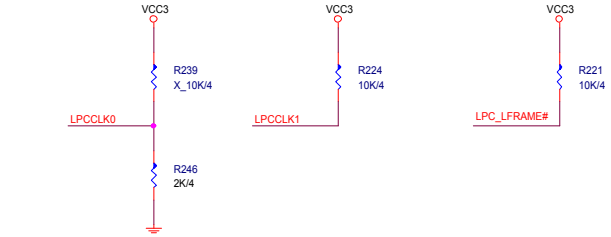
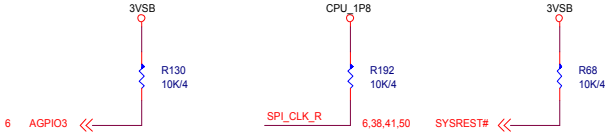
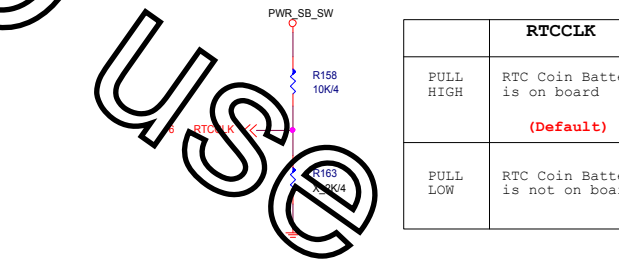
Strapping Options



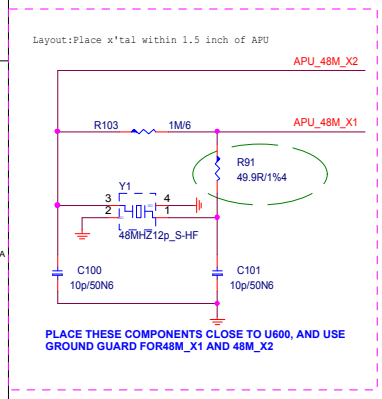
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



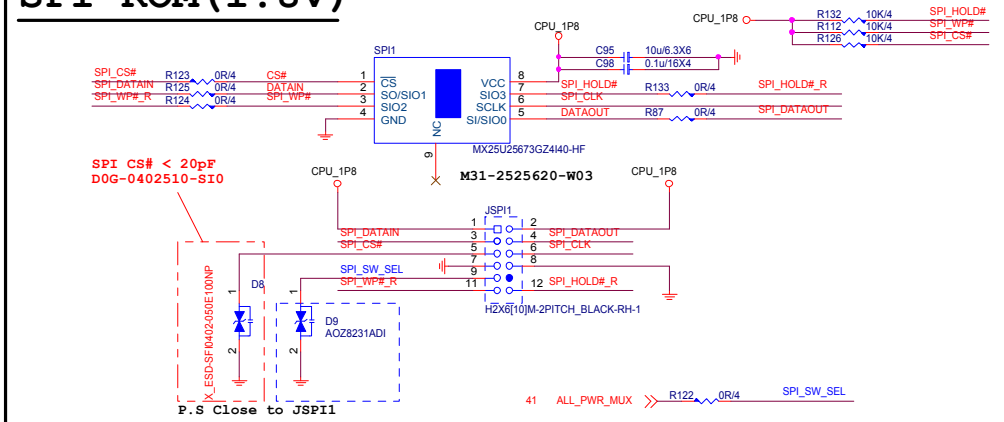
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board



SPI ROM(1.8V)

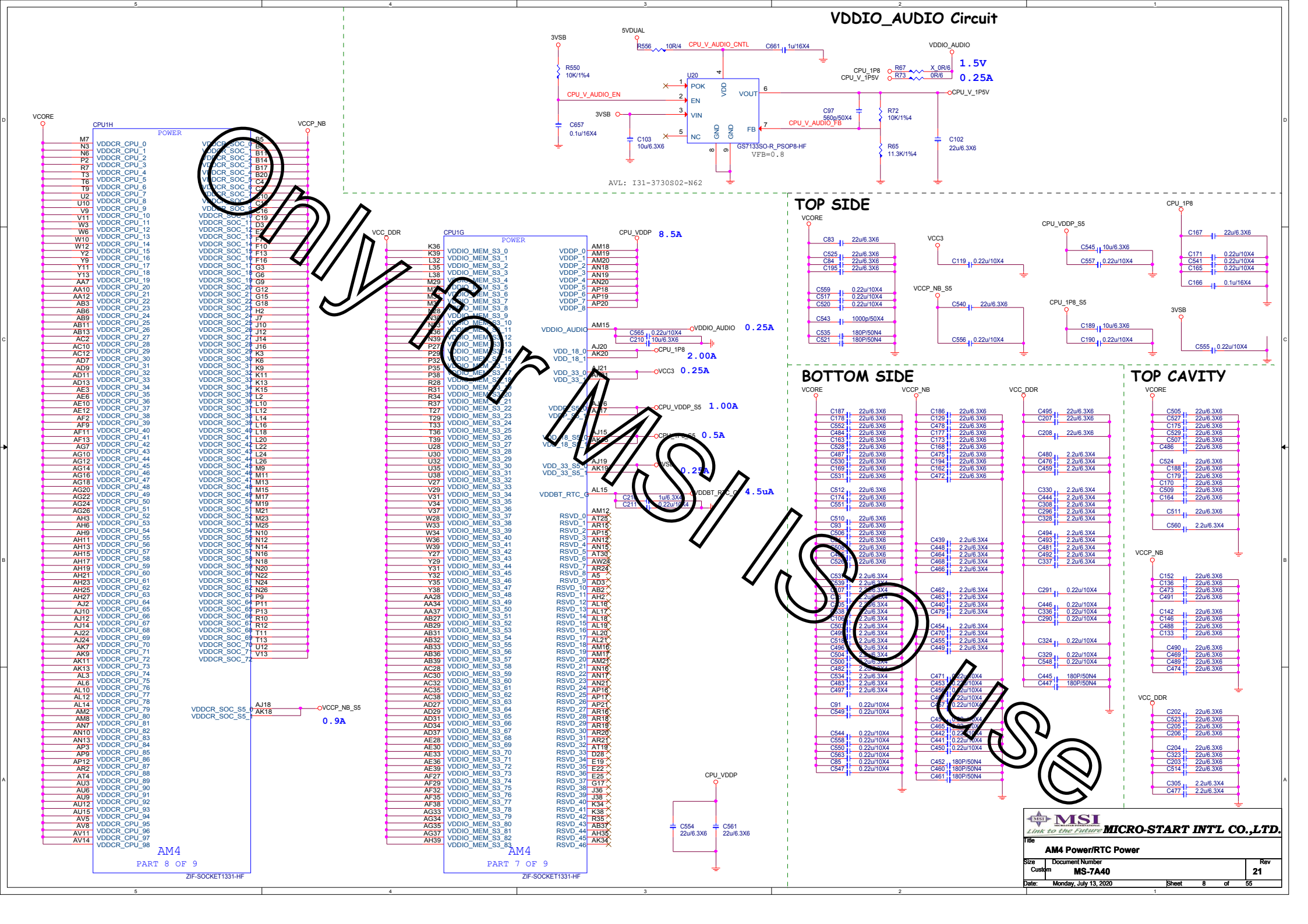


MICRO-START INT'L CO.,LTD.

Title: AM4 LPC/SPI/USB/CLK/STRAP

Size: Custom | Document Number: MS-7A40 | Rev: 21

Date: Monday, July 13, 2020 | Sheet 7 of 55


VDDIO_AUDIO Circuit
3VSB
5VDUAL
R556 10R/4
CPU_V_AUDIO_CNTL
C661 1u/16X4
VDDIO_AUDIO
1.5V
0.25A
R550 10K/1%4
U20
POK
EN
VIN
NC
VDD
VOUT
GND
FB
CPU_V_AUDIO_EN
CPU_V_AUDIO_FB
CPU_1P8
CPU_V_1P5V
R67 X_0R/6
R73 0R/6
CPU_V_1P5V
C97 560p/50X4
R72 10K/1%4
C657 0.1u/16X4
C103 10u/6.3X6
R65 11.3K/1%4
C102 22u/6.3X6
GS7133SO-R_PSOP8-HF
VFB=0.8
AVL: I31-3730S02-N62
TOP SIDE
BOTTOM SIDE
TOP CAVITY
CPU1H
POWER
VCORE
VCCP_NB
VCC_DDR
CPU1G
CPU_VDDP 8.5A
VDDIO_AUDIO 0.25A
CPU_1P8 2.00A
VCC3 0.25A
CPU_VDDP_S5 1.00A
VSB 0.25A
VDDBT_RTC_G 4.5uA
VCCP_NB_S5 0.9A
CPU_VDDP
AM4
PART 8 OF 9
PART 7 OF 9
ZIF-SOCKET1331-HF
Only for MSI ISO use
MICRO-START INT'L CO.,LTD.
Link to the Future
Title
AM4 Power/RTC Power
Size
Custom
Document Number
MS-7A40
Rev
21
Date: Monday, July 13, 2020
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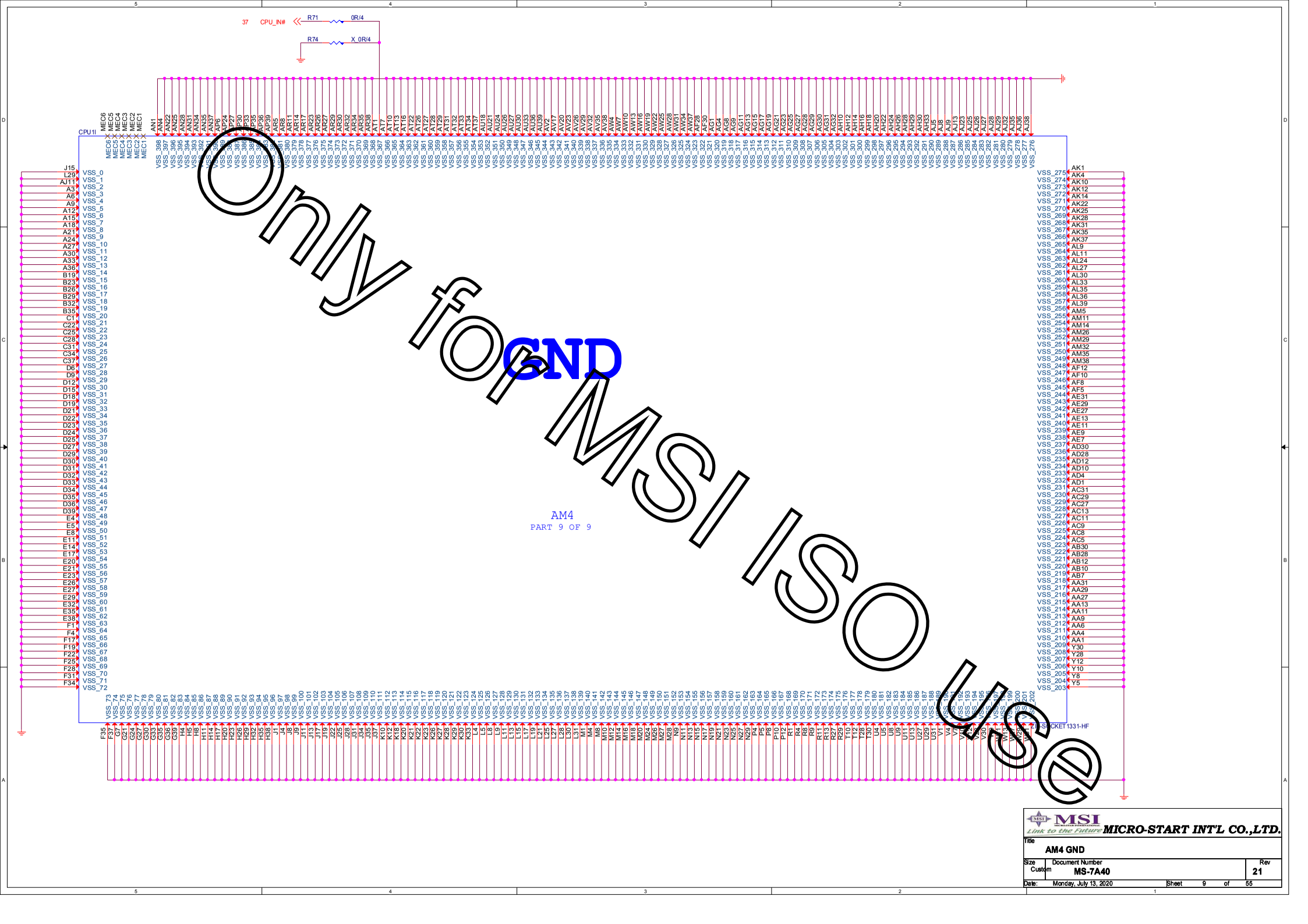

MICRO-STAR INT'L CO.,LTD.

Link to the Future

Title	AM4 GND	
Size: Custom	Document Number: MS-7A40	Rev: 21
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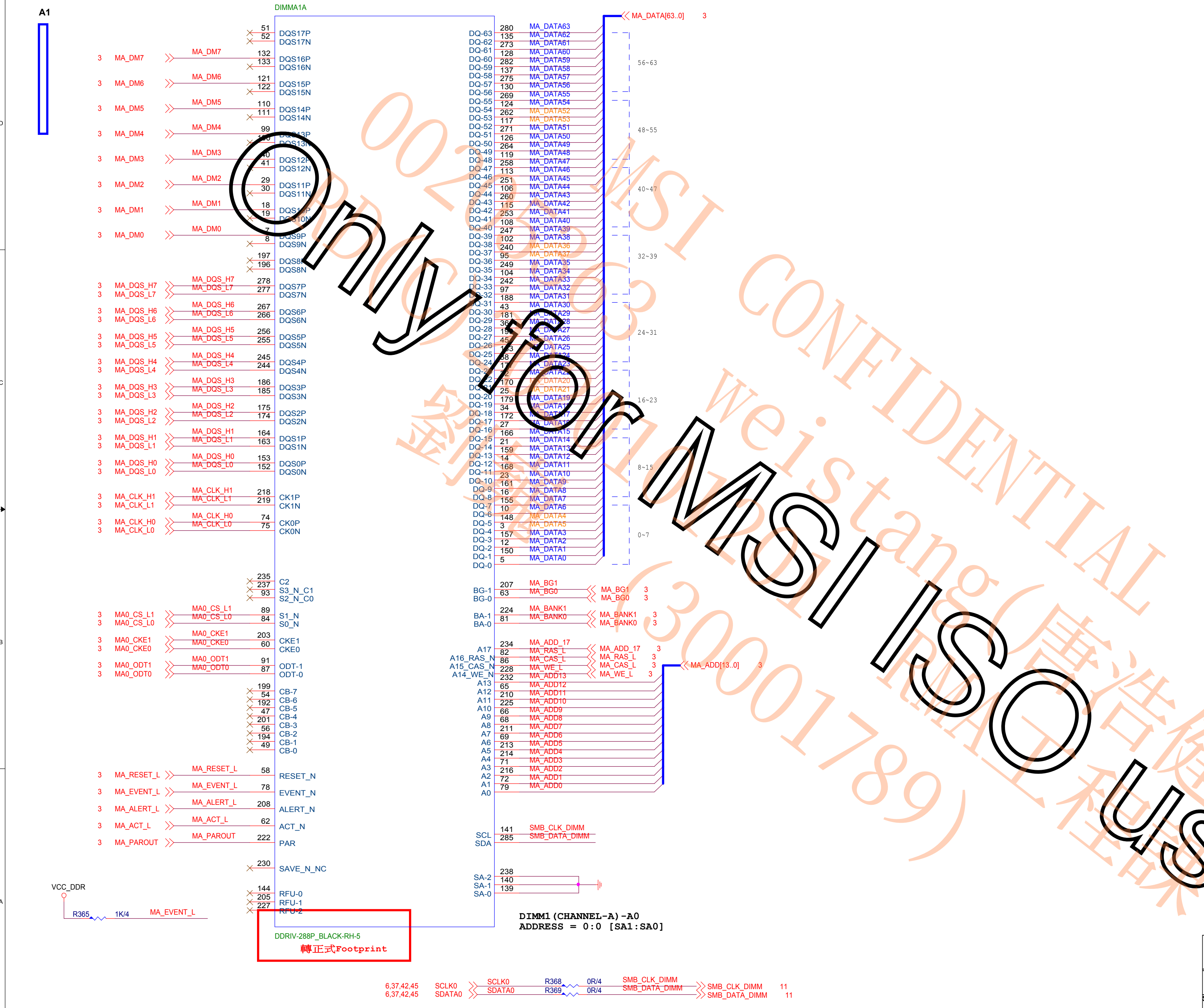
A1


DIMMA1A
MA_DATA[63..0] 3
51 52 DQS17P DQS17N
3 MA_DM7 MA_DM7 132 133 DQS16P DQS16N
3 MA_DM6 MA_DM6 121 122 DQS15P DQS15N
3 MA_DM5 MA_DM5 110 111 DQS14P DQS14N
3 MA_DM4 MA_DM4 99 100 DQS13P DQS13N
3 MA_DM3 MA_DM3 40 41 DQS12P DQS12N
3 MA_DM2 MA_DM2 29 30 DQS11P DQS11N
3 MA_DM1 MA_DM1 18 19 DQS10P DQS10N
3 MA_DM0 MA_DM0 7 8 DQS9P DQS9N
197 196 DQS8P DQS8N
3 MA_DQS_H7 3 MA_DQS_L7 278 277 DQS7P DQS7N
3 MA_DQS_H6 3 MA_DQS_L6 267 266 DQS6P DQS6N
3 MA_DQS_H5 3 MA_DQS_L5 256 255 DQS5P DQS5N
3 MA_DQS_H4 3 MA_DQS_L4 245 244 DQS4P DQS4N
3 MA_DQS_H3 3 MA_DQS_L3 186 185 DQS3P DQS3N
3 MA_DQS_H2 3 MA_DQS_L2 175 174 DQS2P DQS2N
3 MA_DQS_H1 3 MA_DQS_L1 164 163 DQS1P DQS1N
3 MA_DQS_H0 3 MA_DQS_L0 153 152 DQS0P DQS0N
3 MA_CLK_H1 3 MA_CLK_L1 218 219 CK1P CK1N
3 MA_CLK_H0 3 MA_CLK_L0 74 75 CK0P CK0N
235 237 93 C2 S3_N_C1 S2_N_C0
3 MA0_CS_L1 3 MA0_CS_L0 89 84 S1_N S0_N
3 MA0_CKE1 3 MA0_CKE0 203 60 CKE1 CKE0
3 MA0_ODT1 3 MA0_ODT0 91 87 ODT-1 ODT-0
199 54 192 47 201 56 194 49 CB-7 CB-6 CB-5 CB-4 CB-3 CB-2 CB-1 CB-0
3 MA_RESET_L 58 RESET_N
3 MA_EVENT_L 78 EVENT_N
3 MA_ALERT_L 208 ALERT_N
3 MA_ACT_L 62 ACT_N
3 MA_PAROUT 222 PAR
230 SAVE_N_NC
144 205 227 RFU-0 RFU-1 RFU-2
VCC_DDR
R365 1K/4 MA_EVENT_L
DQ-63 280 MA_DATA63
DQ-62 135 MA_DATA62
DQ-61 273 MA_DATA61
DQ-60 128 MA_DATA60
DQ-59 282 MA_DATA59
DQ-58 137 MA_DATA58
DQ-57 275 MA_DATA57
DQ-56 130 MA_DATA56
DQ-55 269 MA_DATA55
DQ-54 124 MA_DATA54
DQ-53 262 MA_DATA52
DQ-52 117 MA_DATA53
DQ-51 271 MA_DATA51
DQ-50 126 MA_DATA50
DQ-49 264 MA_DATA49
DQ-48 119 MA_DATA48
DQ-47 258 MA_DATA47
DQ-46 113 MA_DATA46
DQ-45 251 MA_DATA45
DQ-44 106 MA_DATA44
DQ-43 260 MA_DATA43
DQ-42 115 MA_DATA42
DQ-41 253 MA_DATA41
DQ-40 108 MA_DATA40
DQ-39 247 MA_DATA39
DQ-38 102 MA_DATA38
DQ-37 240 MA_DATA36
DQ-36 95 MA_DATA37
DQ-35 249 MA_DATA35
DQ-34 104 MA_DATA34
DQ-33 242 MA_DATA33
DQ-32 97 MA_DATA32
DQ-31 188 MA_DATA31
DQ-30 43 MA_DATA30
DQ-29 181 MA_DATA29
DQ-28 36 MA_DATA28
DQ-27 MA_DATA27
DQ-26 MA_DATA26
DQ-25 MA_DATA25
DQ-24 MA_DATA24
DQ-23 MA_DATA23
DQ-22 MA_DATA22
DQ-21 170 MA_DATA20
DQ-20 25 MA_DATA21
DQ-19 179 MA_DATA19
DQ-18 34 MA_DATA18
DQ-17 172 MA_DATA17
DQ-16 27 MA_DATA16
DQ-15 166 MA_DATA15
DQ-14 21 MA_DATA14
DQ-13 159 MA_DATA13
DQ-12 14 MA_DATA12
DQ-11 168 MA_DATA11
DQ-10 23 MA_DATA10
DQ-9 161 MA_DATA9
DQ-8 16 MA_DATA8
DQ-7 155 MA_DATA7
DQ-6 10 MA_DATA6
DQ-5 148 MA_DATA4
DQ-4 3 MA_DATA5
DQ-3 157 MA_DATA3
DQ-2 12 MA_DATA2
DQ-1 150 MA_DATA1
DQ-0 5 MA_DATA0
56~63
48~55
40~47
32~39
24~31
16~23
8~15
0~7
BG-1 207 MA_BG1 MA_BG1 3
BG-0 63 MA_BG0 MA_BG0 3
BA-1 224 MA_BANK1 MA_BANK1 3
BA-0 81 MA_BANK0 MA_BANK0 3
A17 234 MA_ADD_17 MA_ADD_17 3
A16_RAS_N 82 MA_RAS_L MA_RAS_L 3
A15_CAS_N 86 MA_CAS_L MA_CAS_L 3
A14_WE_N 228 MA_WE_L MA_WE_L 3
MA_ADD[13..0] 3
A13 232 MA_ADD13
A12 65 MA_ADD12
A11 210 MA_ADD11
A10 225 MA_ADD10
A9 66 MA_ADD9
A8 68 MA_ADD8
A7 211 MA_ADD7
A6 69 MA_ADD6
A5 213 MA_ADD5
A4 214 MA_ADD4
A3 71 MA_ADD3
A2 216 MA_ADD2
A1 72 MA_ADD1
A0 79 MA_ADD0
SCL 141 SMB_CLK_DIMM
SDA 285 SMB_DATA_DIMM
SA-2 238
SA-1 140
SA-0 139
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
DDRIV-288P_BLACK-RH-5
轉正式Footprint
6,37,42,45 SCLK0 SCLK0 R368 0R/4 SMB_CLK_DIMM SMB_CLK_DIMM 11
6,37,42,45 SDATA0 SDATA0 R369 0R/4 SMB_DATA_DIMM SMB_DATA_DIMM 11

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: DDR4-DIMM CH-A

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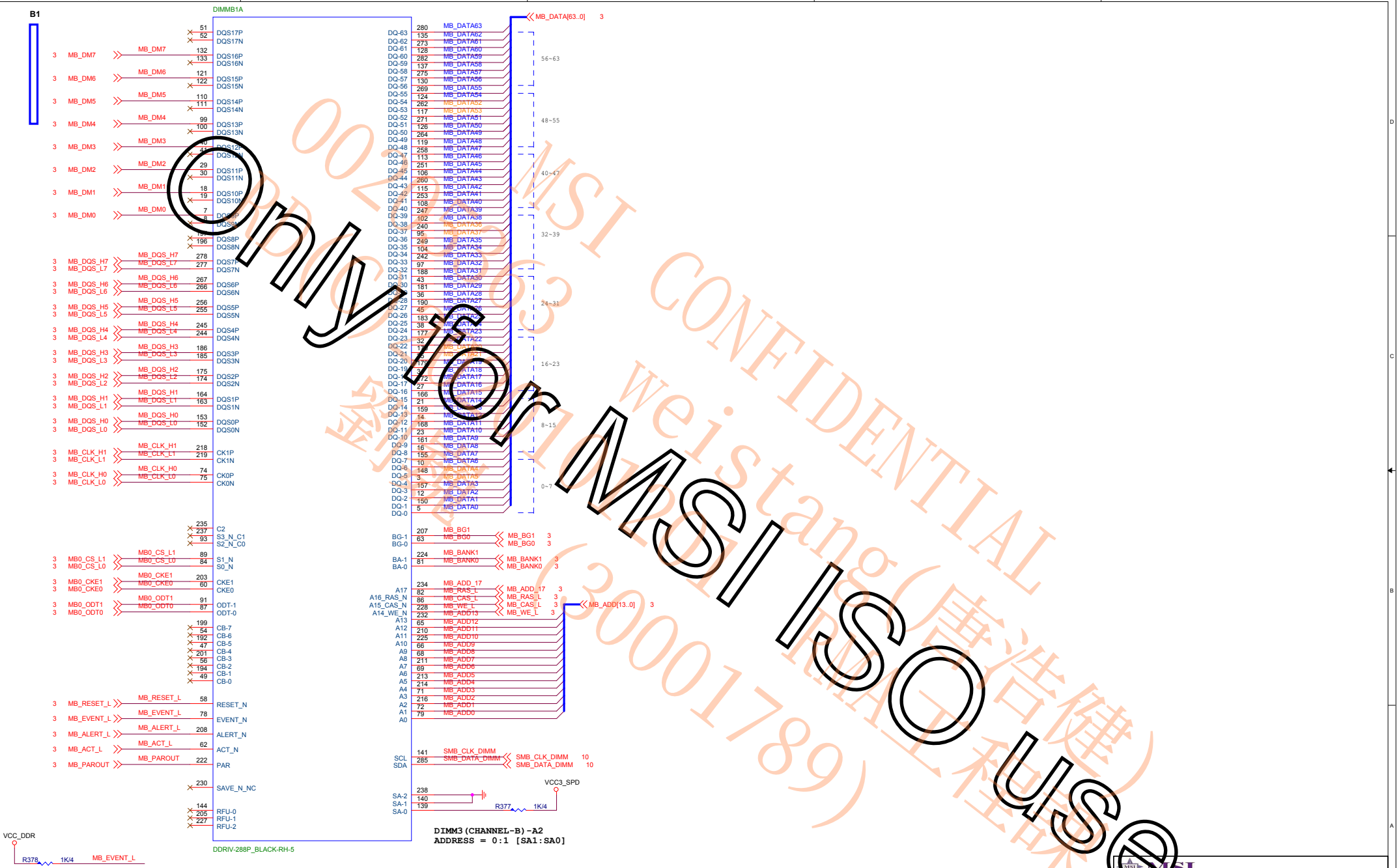

Title	DDR4-DIMM CH-B
Size	Custom
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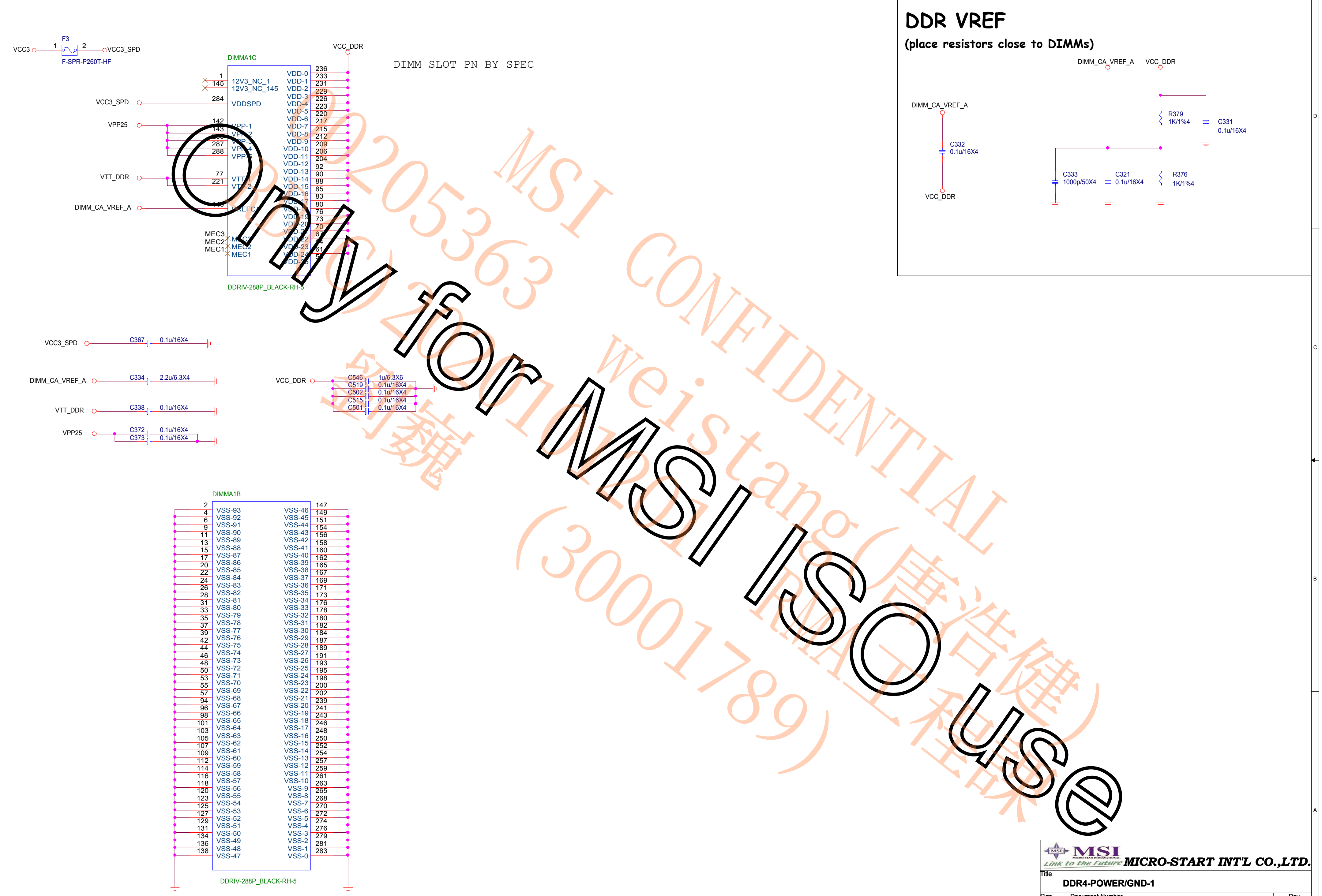
MICRO-START INT'L CO.,LTD.



DDR VREF
(place resistors close to DIMMs)
DIMM SLOT PN BY SPEC
VCC3
F3
F-SPR-P260T-HF
VCC3_SPD
VCC_DDR
DIMMA1C
12V3_NC_1
12V3_NC_145
VDDSPD
VPP25
VPP-1
VPP-2
VPP-3
VPP-4
VPP-5
VTT_DDR
VTT-1
VTT-2
DIMM_CA_VREF_A
VREFCA
MEC3
MEC2
MEC1
VDD-0 … VDD-25
DDRIV-288P_BLACK-RH-5
C332 0.1u/16X4
R379 1K/1%4
C331 0.1u/16X4
C333 1000p/50X4
C321 0.1u/16X4
R376 1K/1%4
C367 0.1u/16X4
C334 2.2u/6.3X4
C338 0.1u/16X4
C372 0.1u/16X4
C373 0.1u/16X4
C546 1u/6.3X6
C519 0.1u/16X4
C502 0.1u/16X4
C515 0.1u/16X4
C501 0.1u/16X4
DIMMA1B
VSS-0 … VSS-93
DDRIV-288P_BLACK-RH-5

MICRO-START INT'L CO.,LTD.

Title: DDR4-POWER/GND-1

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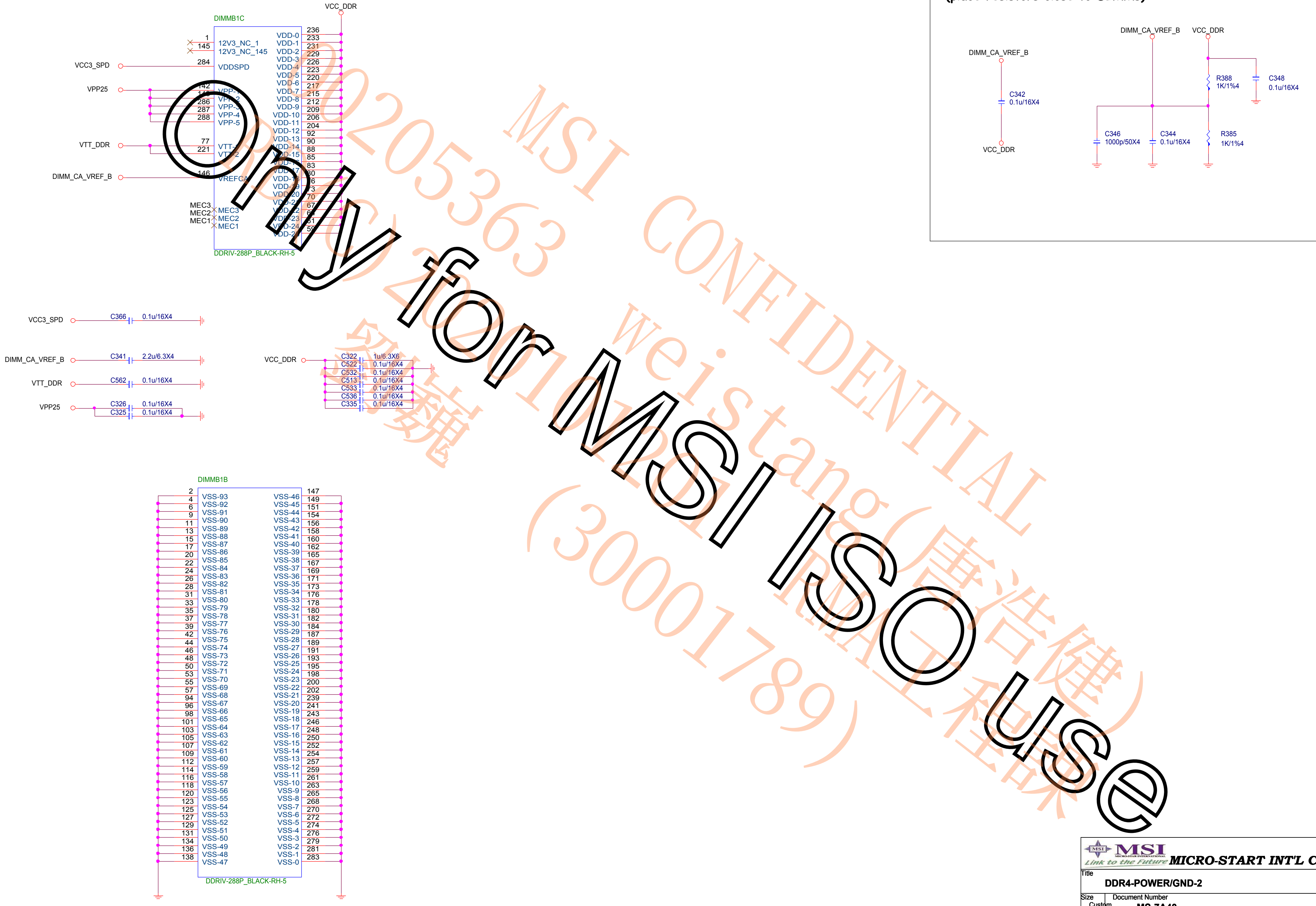
DDR VREF

(place resistors close to DIMMs)



DIMMB1C
VCC_DDR
12V3_NC_1
12V3_NC_145
VDDSPD
VPP-1
VPP-2
VPP-3
VPP-4
VPP-5
VTT-1
VTT-2
VREFCA
MEC3
MEC2
MEC1
VCC3_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
DDRIV-288P_BLACK-RH-5
DIMM_CA_VREF_B
C342
0.1u/16X4
VCC_DDR
DIMM_CA_VREF_B
VCC_DDR
R388
1K/1%4
C348
0.1u/16X4
C346
1000p/50X4
C344
0.1u/16X4
R385
1K/1%4
VCC3_SPD
C366
0.1u/16X4
DIMM_CA_VREF_B
C341
2.2u/6.3X4
VTT_DDR
C562
0.1u/16X4
VPP25
C326
0.1u/16X4
C325
0.1u/16X4
VCC_DDR
C322
1u/6.3X6
C522
0.1u/16X4
C532
0.1u/16X4
C513
0.1u/16X4
C533
0.1u/16X4
C536
0.1u/16X4
C335
0.1u/16X4
DIMMB1B
DDRIV-288P_BLACK-RH-5

MICRO-START INT'L CO.,LTD.
Title: DDR4-POWER/GND-2
Size: Custom
Document Number: MS-7A40
Rev: 21
Date: Monday, July 13, 2020
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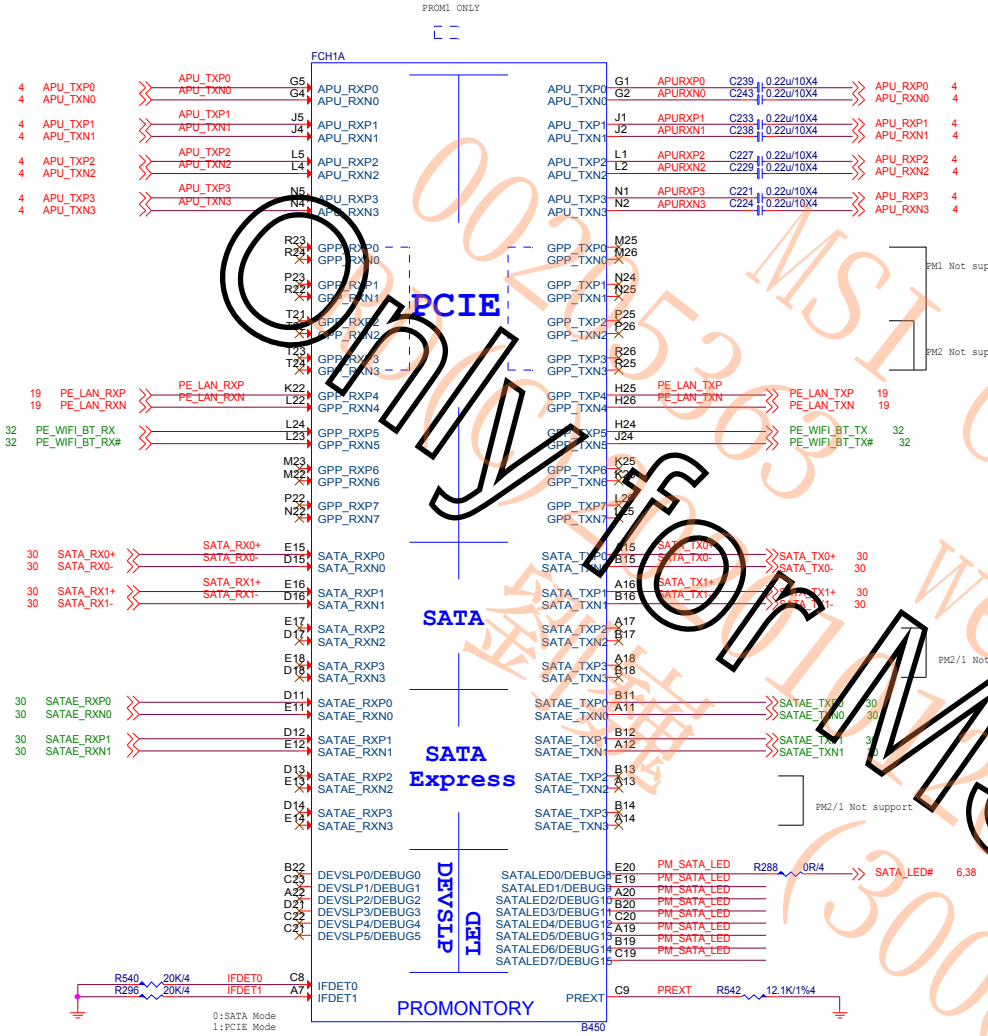

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	Promontory-PCIE/SATA/SATAE	
Size: Custom	Document Number: MS-7A40	Rev: 21
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USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

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AMD 300-Series Chipsets, "Promontory" Sub-Family Data Sheet 55553 Rev. 1.08 September 2016

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

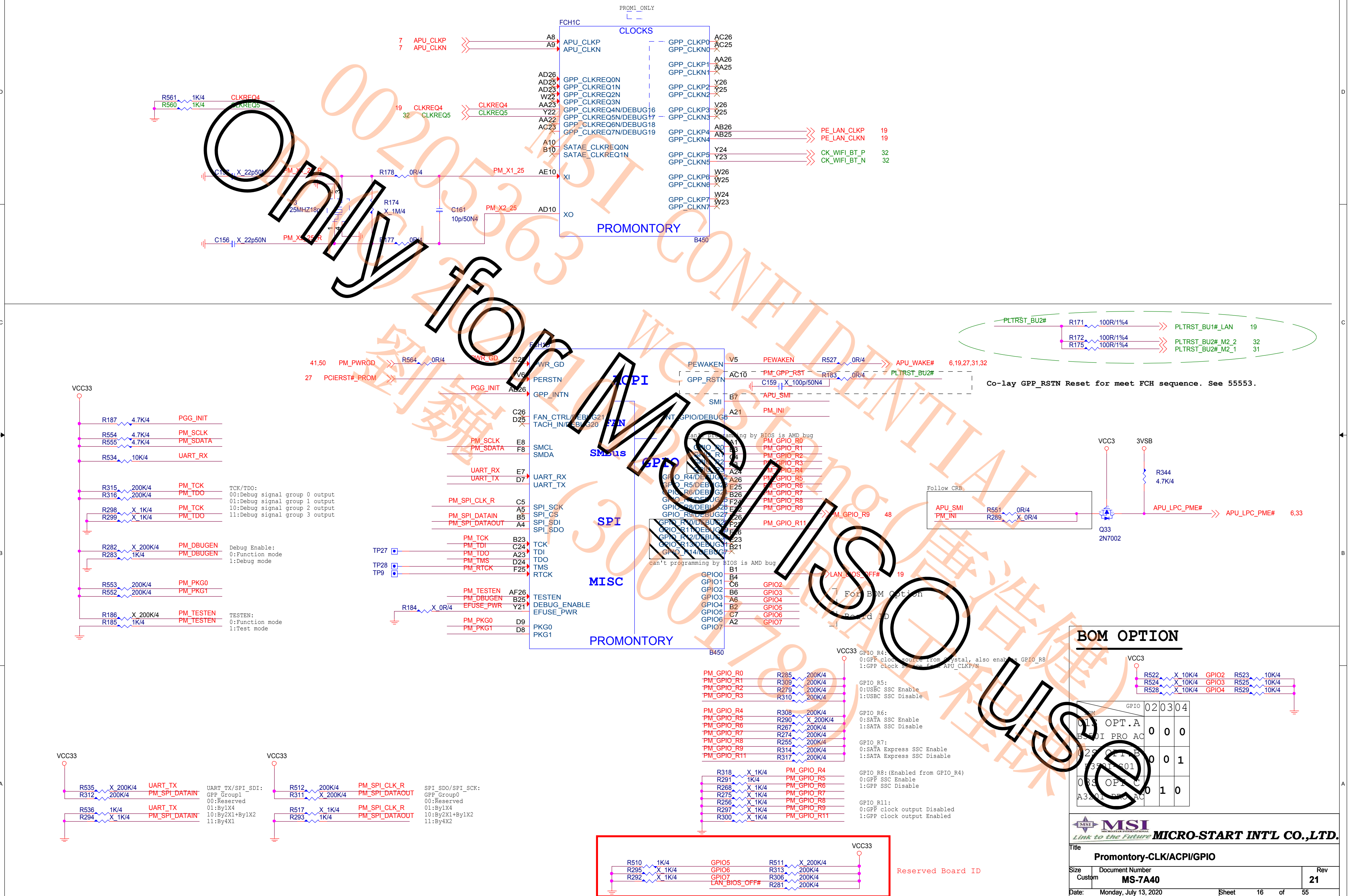
BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: **Promontory-USB/OC**

Size: Custom | Document Number: **MS-7A40** | Rev: **21**

Date: Monday, July 13, 2020 | Sheet 15 of 55



PROM1_ONLY
FCH1C
CLOCKS
APU_CLKP
APU_CLKN
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEBUG16
GPP_CLKREQ5N/DEBUG17
GPP_CLKREQ6N/DEBUG18
GPP_CLKREQ7N/DEBUG19
SATAE_CLKREQ0N
SATAE_CLKREQ1N
XI
XO
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
PROMONTORY
B450
PE_LAN_CLKP 19
PE_LAN_CLKN 19
CK_WIFI_BT_P 32
CK_WIFI_BT_N 32
CLKREQ4
CLKREQ5
R561 1K/4
R560 1K/4
C157 X_22p50N
C156 X_22p50N
25MHZ18p
R178 0R/4
R174 X_1M/4
R177 0R/4
C161 10p/50N4
PM_X1_25
PM_X2_25
PLTRST_BU2#
R171 100R/1%4 PLTRST_BU1#_LAN 19
R172 100R/1%4 PLTRST_BU2#_M2_2 32
R175 100R/1%4 PLTRST_BU2#_M2_1 31
41,50 PM_PWRGD
27 PCIERST#_PROM
R564 0R/4
PWR_GD
PERSTN
GPP_INTN
ACPI
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
FAN
SMCL
SMDA
SMBus
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
SPI
TCK
TDI
TDO
TMS
RTCK
MISC
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PKG0
PKG1
PEWAKEN
GPP_RSTN
SMI
INT_GPIO/DEBUG6
GPIO
PEWAKEN R527 0R/4 APU_WAKE# 6,19,27,31,32
PM_GPP_RST R183 0R/4 PLTRST_BU2#
C159 X_100p/50N4
APU_SMI
PM_INI
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
can't programming by BIOS is AMD bug
PM_GPIO_R9 48
PM_GPIO_R11
LAN_BIOS_OFF# 19
For BOM Option
Board ID
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
VCC33
R187 4.7K/4 PGG_INIT
R554 4.7K/4 PM_SCLK
R555 4.7K/4 PM_SDATA
R534 10K/4 UART_RX
R315 200K/4 PM_TCK
R316 200K/4 PM_TDO
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
R298 X_1K/4 PM_TCK
R299 X_1K/4 PM_TDO
R282 X_200K/4 PM_DBUGEN
R283 1K/4 PM_DBUGEN
Debug Enable:
0:Function mode
1:Debug mode
R553 200K/4 PM_PKG0
R552 200K/4 PM_PKG1
R186 X_200K/4 PM_TESTEN
R185 1K/4 PM_TESTEN
TESTEN:
0:Function mode
1:Test mode
TP27
TP28
TP9
R184 X_0R/4
Follow CRB
APU_SMI R551 0R/4
PM_INI R289 X_0R/4
Q33 2N7002
VCC3
3VSB
R344 4.7K/4
APU_LPC_PME#
APU_LPC_PME# 6,33
GPIO_R4:
0:GPP clock source from crystal, also enable GPIO_R8
1:GPP clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
R535 X_200K/4 UART_TX
R312 200K/4 PM_SPI_DATAIN
R536 1K/4 UART_TX
R294 X_1K/4 PM_SPI_DATAIN
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X1
R512 200K/4 PM_SPI_CLK_R
R311 X_200K/4 PM_SPI_DATAOUT
R517 X_1K/4 PM_SPI_CLK_R
R293 1K/4 PM_SPI_DATAOUT
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
R510 1K/4 GPIO5 R511 X_200K/4
R295 X_1K/4 GPIO6 R313 200K/4
R292 X_1K/4 GPIO7 R306 200K/4
LAN_BIOS_OFF# R281 200K/4
Reserved Board ID
BOM OPTION
R522 X_10K/4 GPIO2 R523 10K/4
R524 X_10K/4 GPIO3 R525 10K/4
R528 X_10K/4 GPIO4 R529 10K/4

BOM OPTION

GPIO	02	03	04
01S OPT.A B350I PRO AC	0	0	0
02S OPT.B B350I-S01	0	0	1
03S OPT.C A320I PRO AC	0	1	0

MICRO-STAR INT'L CO.,LTD.

Title: Promontory-CLK/ACPI/GPIO

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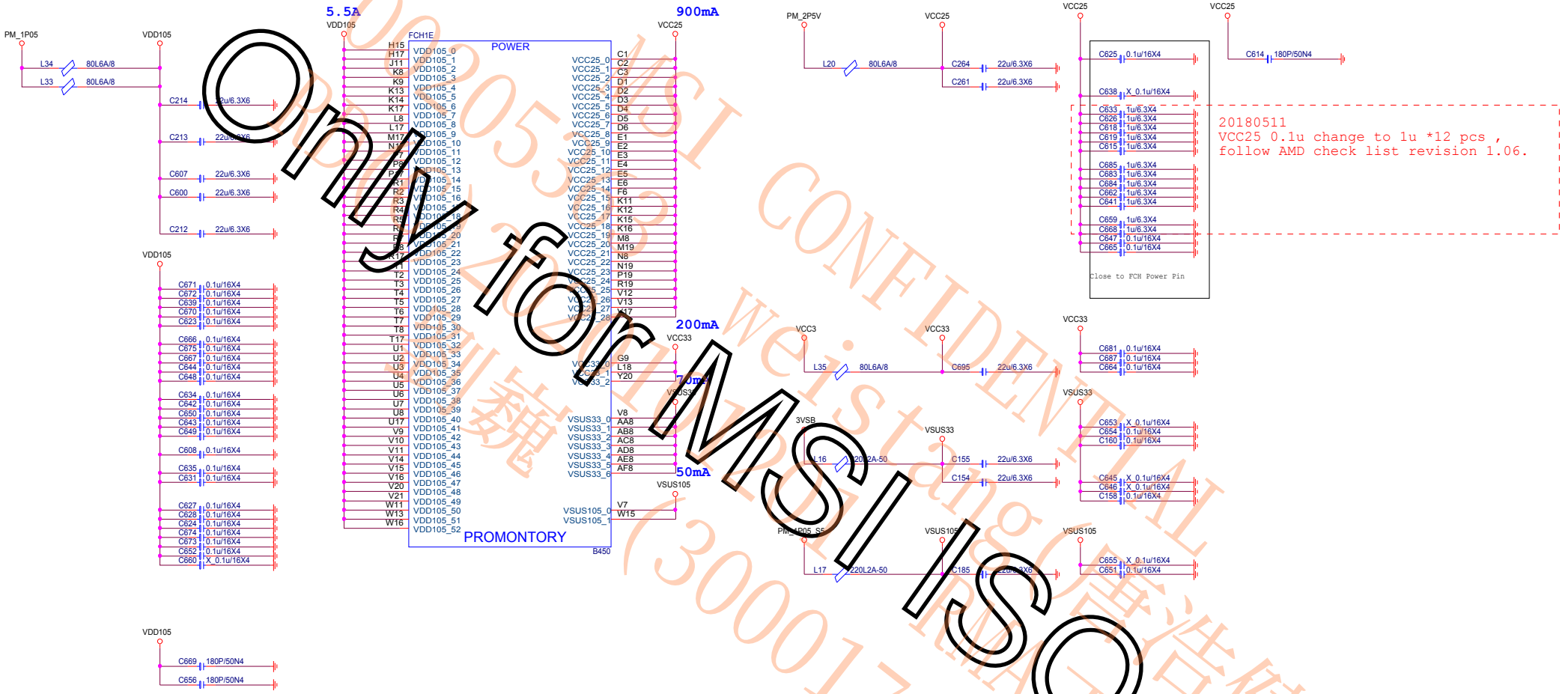
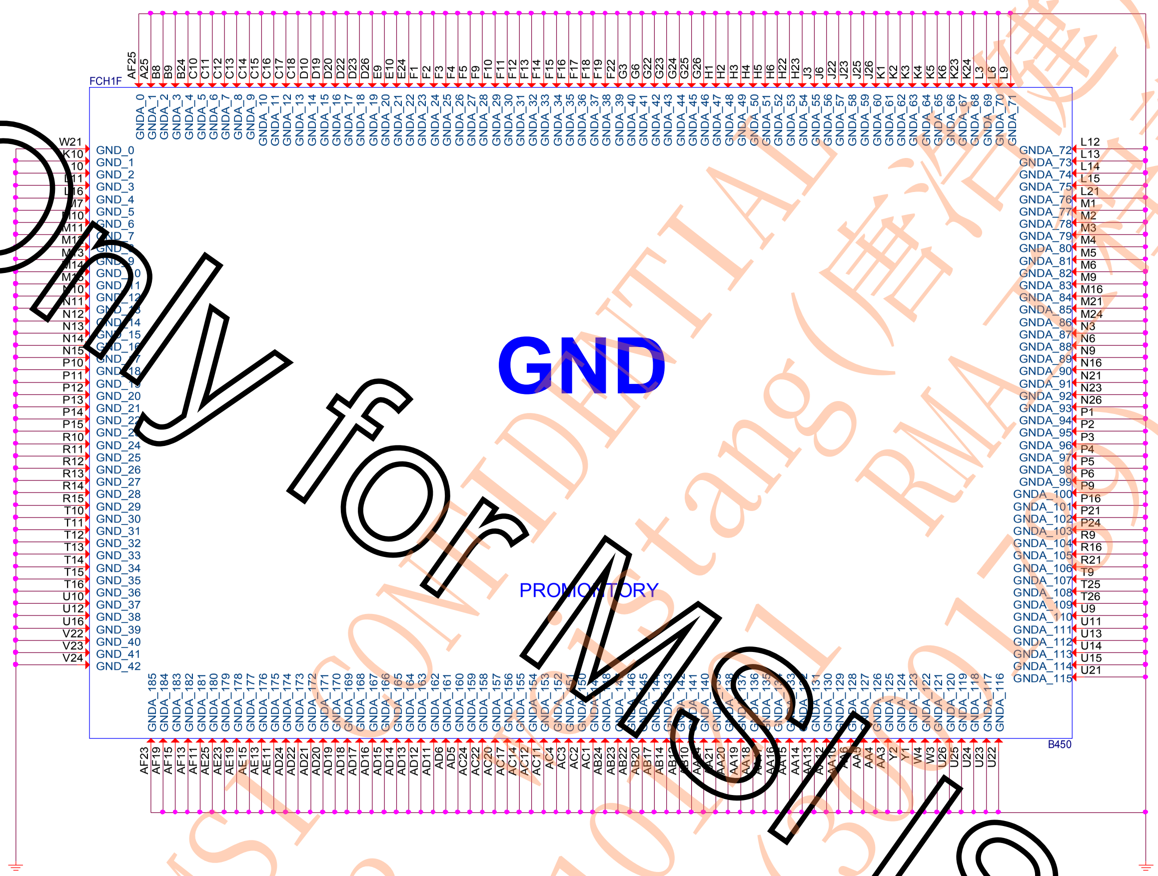


MICRO-START INT'L CO.,LTD.

Title: Promontory-Power		
Size: Custom	Document Number: MS-7A40	Rev: 21
Date: Monday, July 13, 2020	Sheet 17 of 55	



MICRO-START INT'L CO.,LTD.

Title: Promontory-GND		
Size: Custom	Document Number: MS-7A40	Rev: 21
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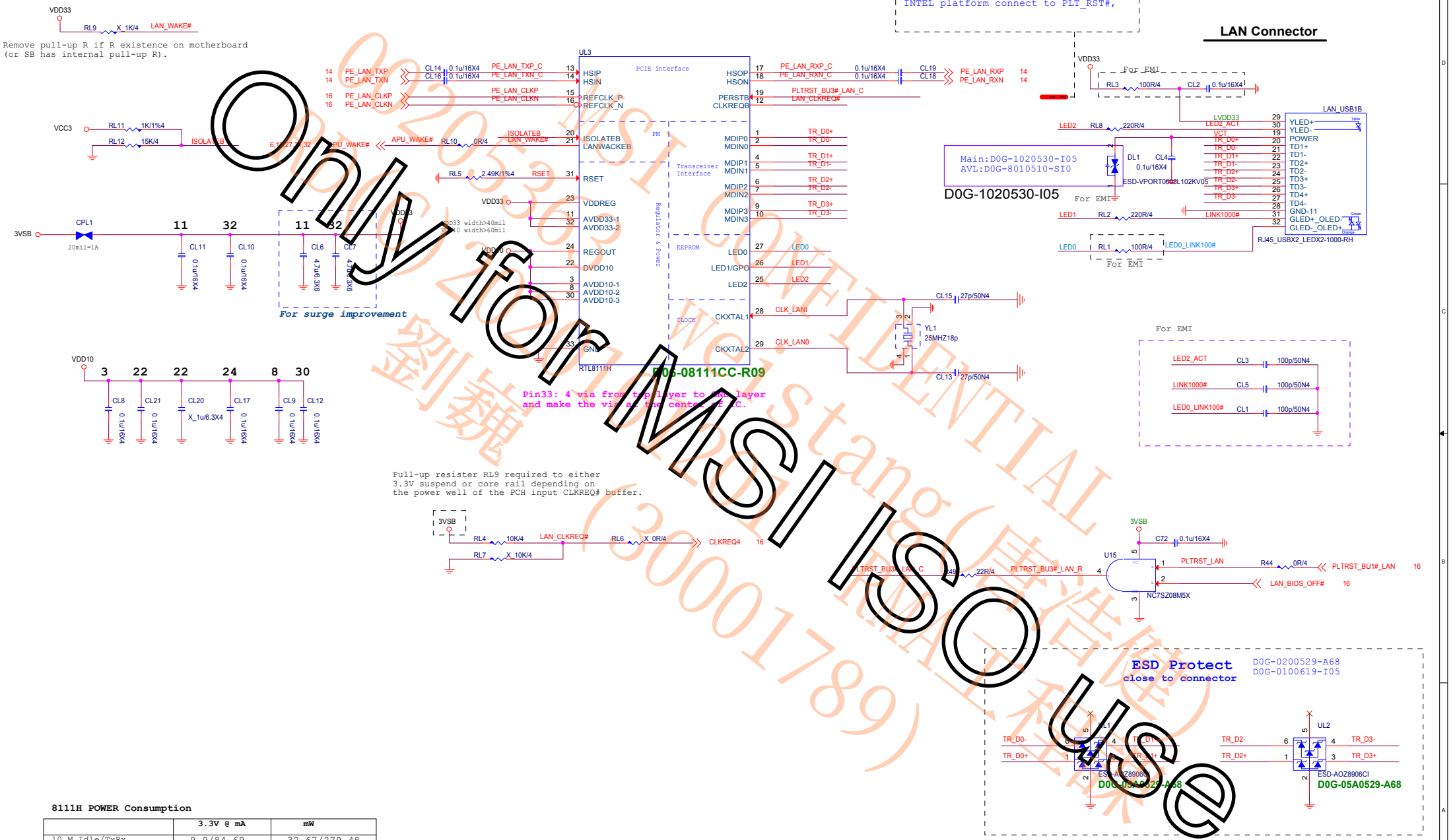
RTL8111H Giga LAN

3.3V@177.57mA



8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-START INT'L CO.,LTD.

Title: LAN-RLT 8111H

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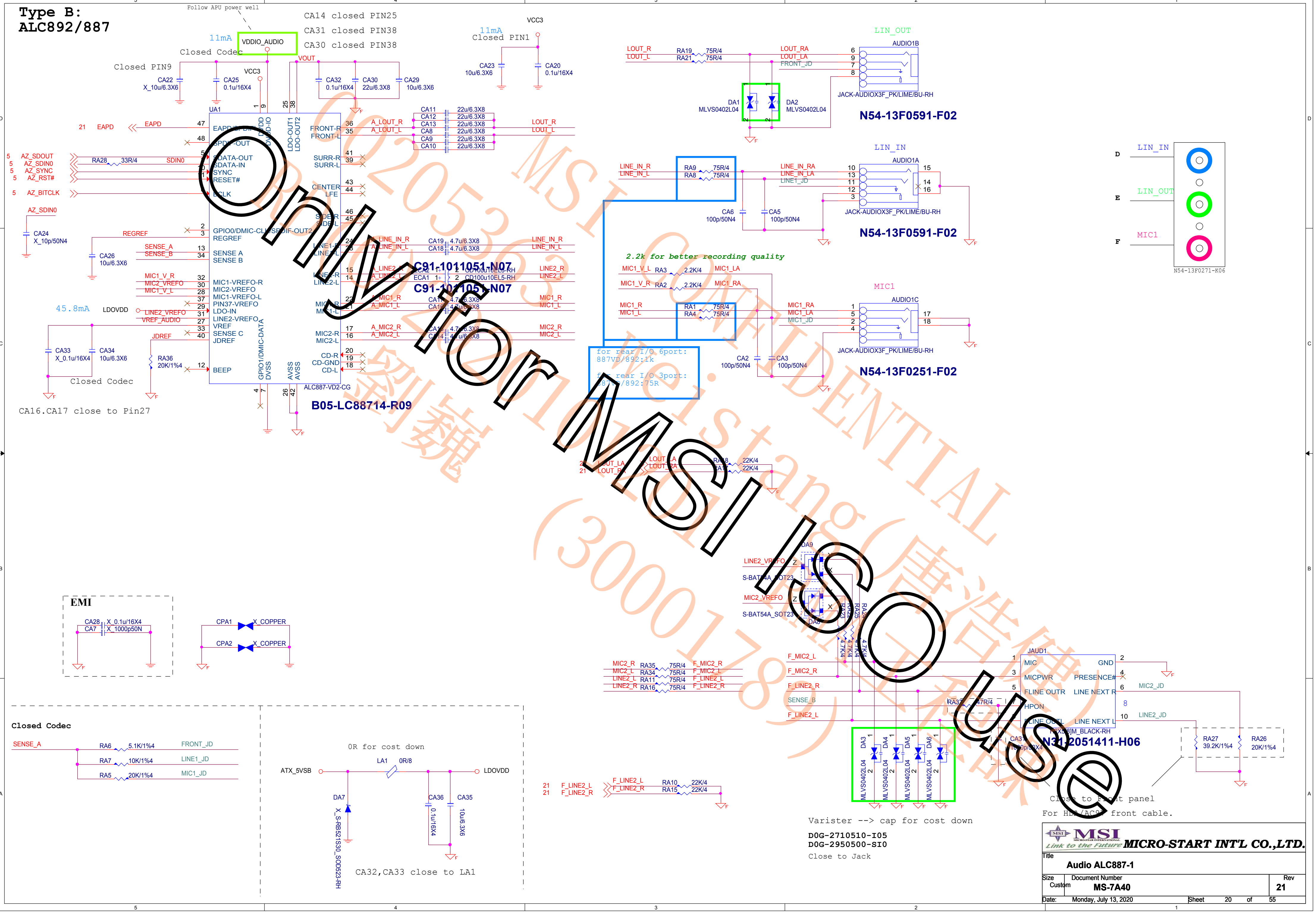

Type B:
ALC892/887
Follow APU power well
11mA
VDDIO_AUDIO
Closed Codec
CA14 closed PIN25
CA31 closed PIN38
CA30 closed PIN38
11mA
Closed PIN1
VCC3
Closed PIN9
UA1
EAPD
AZ_SDOUT
AZ_SDIN0
AZ_SYNC
AZ_RST#
AZ_BITCLK
AZ_SDIN0
REGREF
SENSE_A
SENSE_B
MIC1_V_R
MIC2_VREFO
MIC1_V_L
45.8mA
LDOVDD
LINE2_VREFO
VREF_AUDIO
JDREF
Closed Codec
CA16.CA17 close to Pin27
ALC887-VD2-CG
B05-LC88714-R09
C91-1011051-N07
C91-1011051-N07
LIN_OUT
AUDIO1B
JACK-AUDIOX3F_PK/LIME/BU-RH
N54-13F0591-F02
LIN_IN
AUDIO1A
JACK-AUDIOX3F_PK/LIME/BU-RH
N54-13F0591-F02
2.2k for better recording quality
MIC1
AUDIO1C
JACK-AUDIOX3F_PK/LIME/BU-RH
N54-13F0251-F02
for rear I/O 6port: 887VD/892:1k
for rear I/O 3port: 887VD/892:75R
LIN_IN
LIN_OUT
MIC1
N54-13F0271-K06
EMI
S-BAT54A_SOT23
S-BAT54A_SOT23
JAUD1
MIC
MICPWR
FLINE OUTR
HPON
FLINE OUTL
GND
PRESENCE#
LINE NEXT R
LINE NEXT L
N31-2051411-H06
Close to Front panel
For HDA/AC97 front cable.
Varister --> cap for cost down
D0G-2710510-I05
D0G-2950500-SI0
Close to Jack
Closed Codec
SENSE_A
FRONT_JD
LINE1_JD
MIC1_JD
0R for cost down
ATX_5VSB
LA1
LDOVDD
CA32,CA33 close to LA1
MICRO-START INT'L CO.,LTD.
Title
Audio ALC887-1
Size Custom
Document Number MS-7A40
Rev 21
Date: Monday, July 13, 2020
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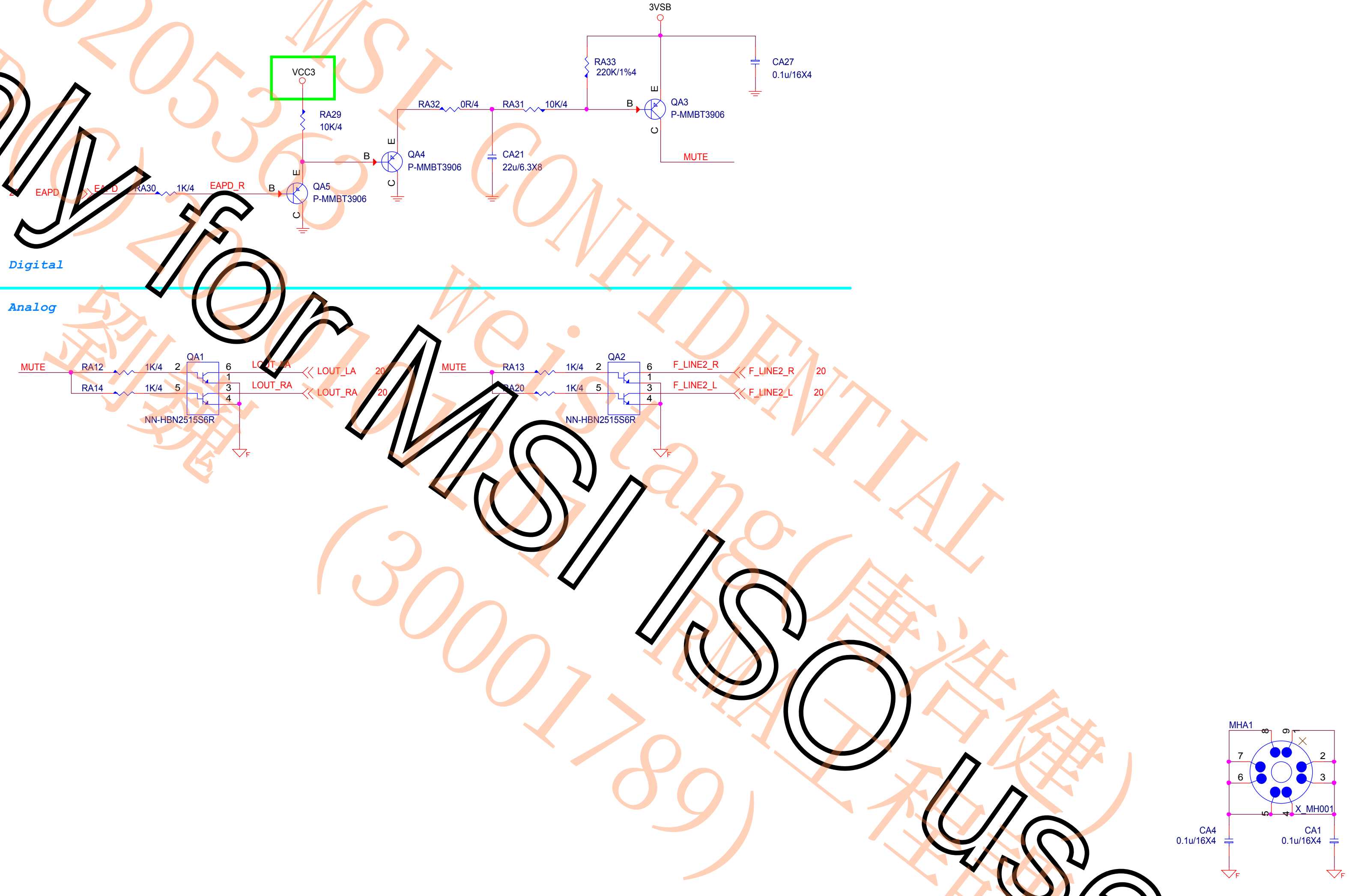
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



MSI MICRO-START INT'L CO.,LTD.			
Title	Audio ALC887-2		
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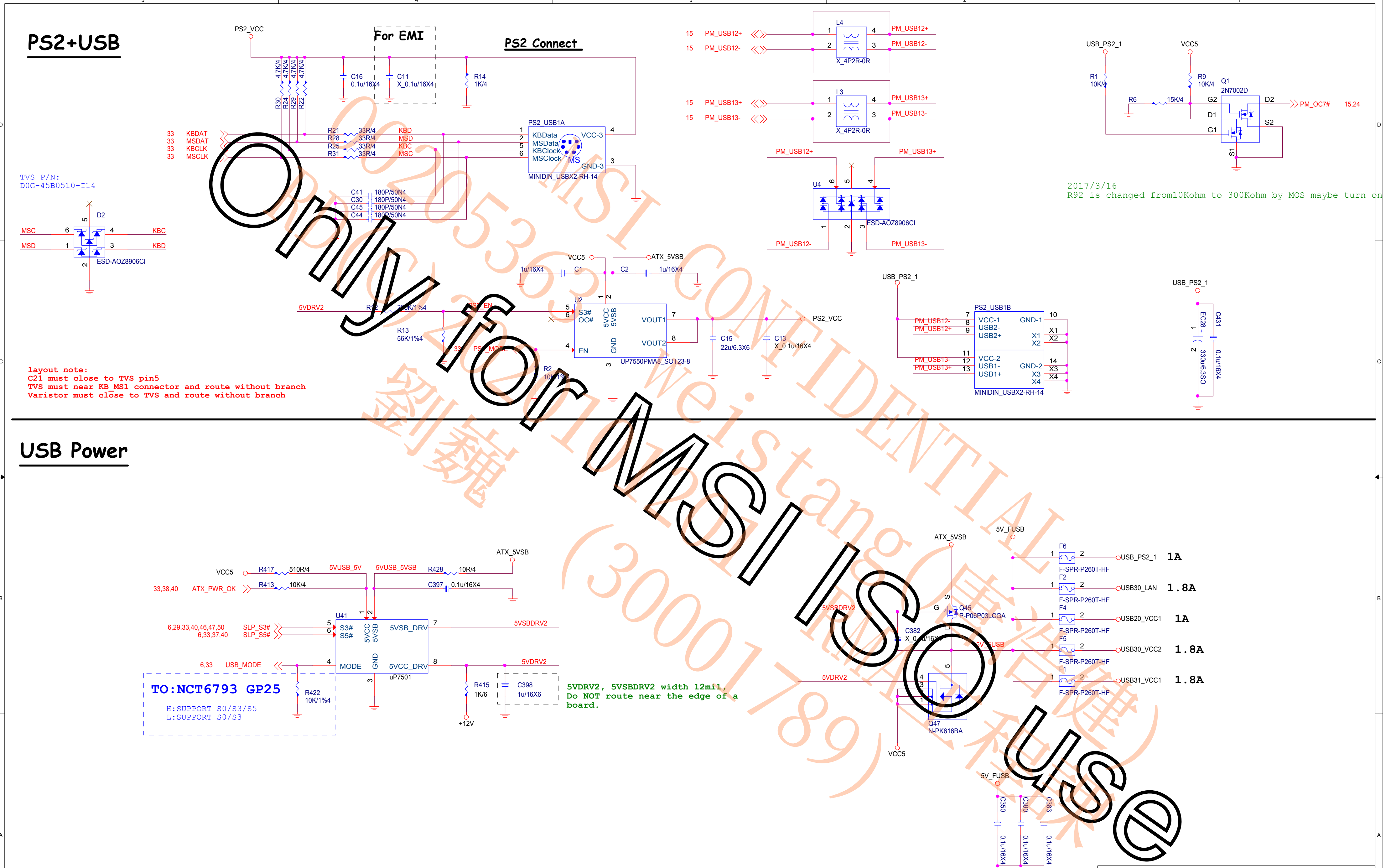

PS2+USB
For EMI
PS2 Connect
PS2_VCC
R30 R24 R29 R22 4.7K/4
C16 0.1u/16X4
C11 X_0.1u/16X4
R14 1K/4
33 KBDAT
33 MSDAT
33 KBCLK
33 MSCLK
R21 33R/4 KBD
R28 33R/4 MSD
R25 33R/4 KBC
R31 33R/4 MSC
PS2_USB1A
KBData
MSData
KBClock
MSClock
VCC-3
GND-3
MINIDIN_USBX2-RH-14
C41 180P/50N4
C30 180P/50N4
C45 180P/50N4
C44 180P/50N4
TVS P/N:
D0G-45B0510-I14
D2
MSC
MSD
KBC
KBD
ESD-AOZ8906CI
15 PM_USB12+
15 PM_USB12-
15 PM_USB13+
15 PM_USB13-
L4
L3
X_4P2R-0R
U4
ESD-AOZ8906CI
USB_PS2_1
VCC5
R1 10K/4
R9 10K/4
R6 15K/4
Q1 2N7002D
PM_OC7# 15,24
2017/3/16
R92 is changed from10Kohm to 300Kohm by MOS maybe turn on
VCC5
ATX_5VSB
C1 1u/16X4
C2 1u/16X4
U2
5VDRV2
R12 200K/1%4
R13 56K/1%4
R2 10K/1%4
33 PS2_MODE
S3#
OC#
EN
5VCC
5VSB
GND
VOUT1
VOUT2
UP7550PMA8_SOT23-8
PS2_VCC
C15 22u/6.3X6
C13 X_0.1u/16X4
PS2_USB1B
VCC-1
USB2-
USB2+
VCC-2
USB1-
USB1+
GND-1
GND-2
MINIDIN_USBX2-RH-14
EC28 330u/6.3SO
C431 0.1u/16X4
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch
USB Power
VCC5
R417 510R/4
5VUSB_5V
5VUSB_5VSB
R428 10R/4
ATX_5VSB
33,38,40 ATX_PWR_OK
R413 10K/4
C397 0.1u/16X4
U41
6,29,33,40,46,47,50 SLP_S3#
6,33,37,40 SLP_S5#
6,33 USB_MODE
MODE
5VSB_DRV
5VCC_DRV
uP7501
5VSBDRV2
5VDRV2
R422 10K/1%4
R415 1K/6
+12V
C398 1u/16X6
TO:NCT6793 GP25
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3
5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.
ATX_5VSB
Q45 P-P06P03LCGA
C382 X_0.1u/16X4
5V_FUSB
Q47 N-PK616BA
VCC5
F6 F-SPR-P260T-HF USB_PS2_1 1A
F2 F-SPR-P260T-HF USB30_LAN 1.8A
F4 F-SPR-P260T-HF USB20_VCC1 1A
F5 F-SPR-P260T-HF USB30_VCC2 1.8A
F1 F-SPR-P260T-HF USB31_VCC1 1.8A
5V_FUSB
C350 C380 C383 0.1u/16X4

MICRO-START INT'L CO.,LTD.

Title: USB Rear PS2+USB2.0

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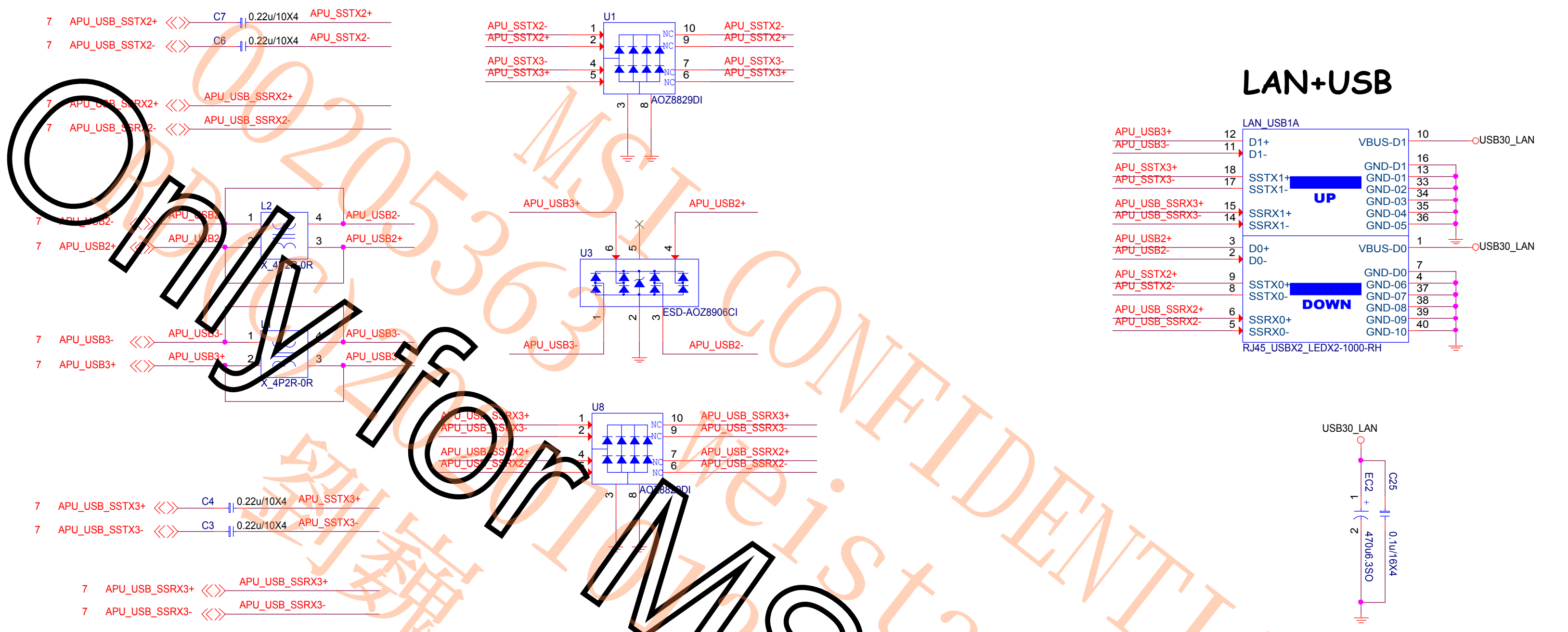
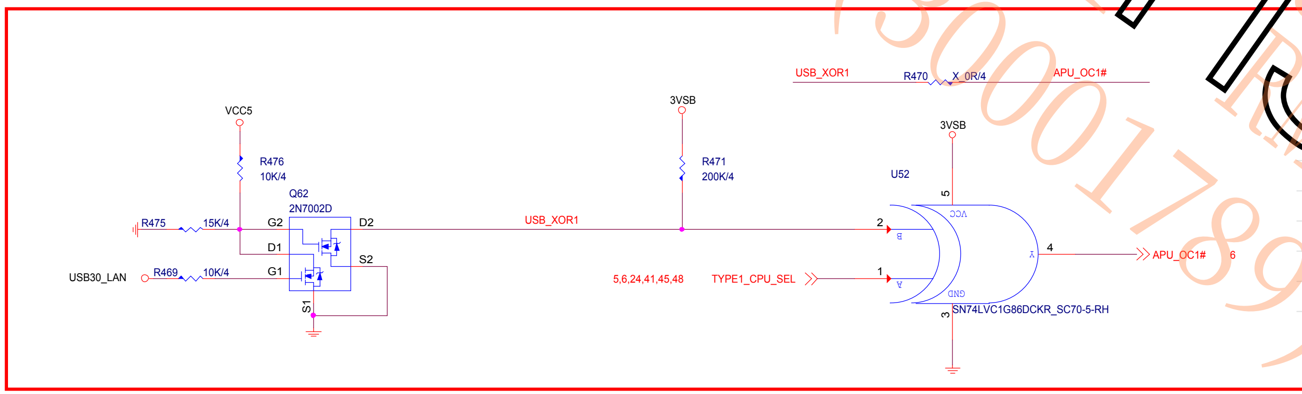
USB3.1 GEN1





	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MICRO-START INT'L CO.,LTD.

Title: USB Rear LAN+USB3.1 GEN1

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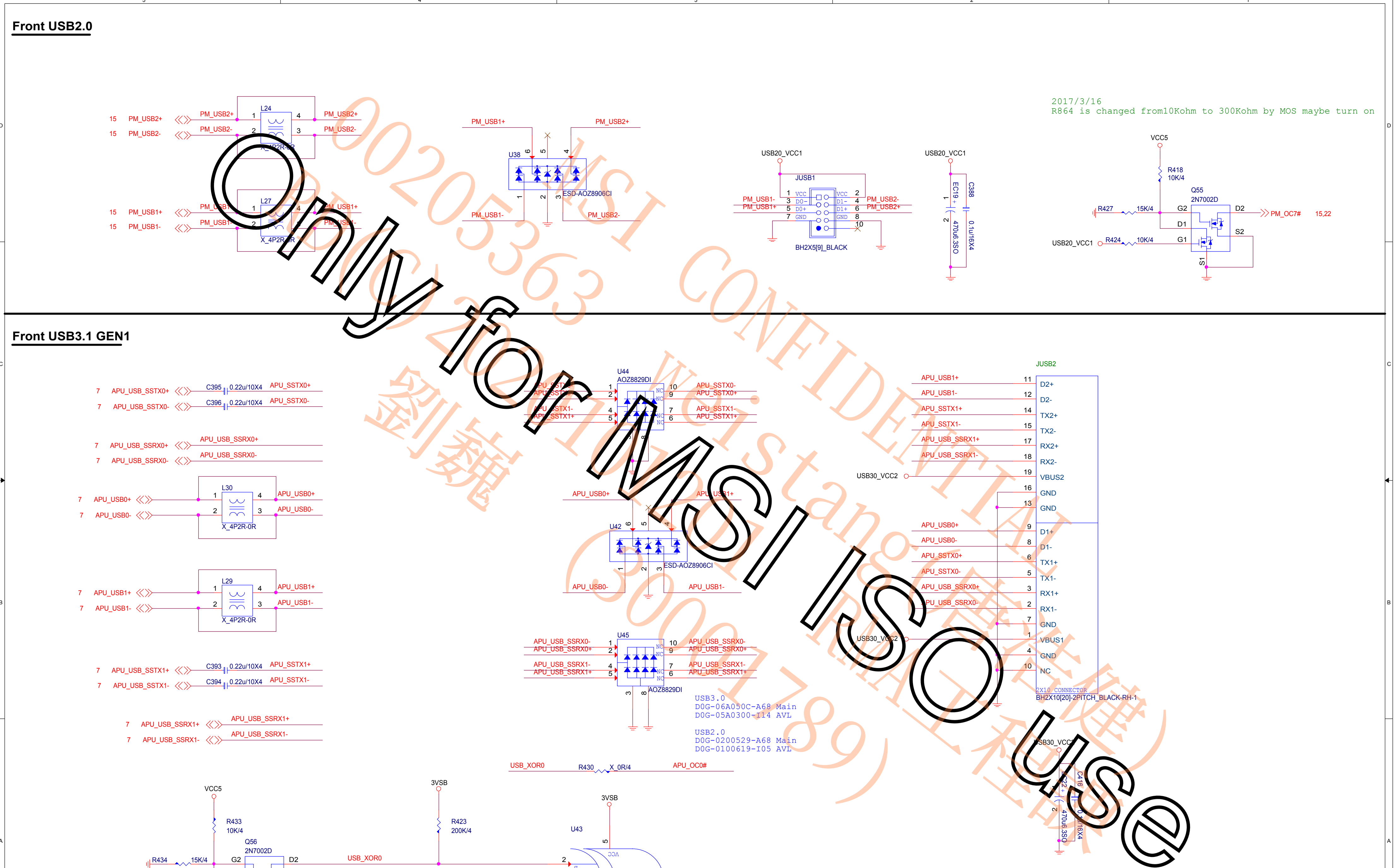

Front USB2.0
Front USB3.1 GEN1
2017/3/16
R864 is changed from10Kohm to 300Kohm by MOS maybe turn on
L24 X_4P2R-0R
L27 X_4P2R-0R
U38 ESD-AOZ8906CI
JUSB1 BH2X5[9]_BLACK
USB20_VCC1
EC19 470u6.3SO
C388 0.1u/16X4
VCC5
R418 10K/4
Q55 2N7002D
R427 15K/4
R424 10K/4
PM_OC7#
PM_USB1+
PM_USB1-
PM_USB2+
PM_USB2-
C395 0.22u/10X4
C396 0.22u/10X4
C393 0.22u/10X4
C394 0.22u/10X4
L30 X_4P2R-0R
L29 X_4P2R-0R
U44 AOZ8829DI
U42 ESD-AOZ8906CI
U45 AOZ8829DI
JUSB2 BH2X10[20]-2PITCH_BLACK-RH-1
USB30_VCC2
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL
R430 X_0R/4
USB_XOR0
APU_OC0#
R433 10K/4
Q56 2N7002D
R434 15K/4
R440 10K/4
R423 200K/4
3VSB
U43 SN74LVC1G86DCKR_SC70-5-RH
TYPE1_CPU_SEL
EC22 470u6.3SO
C416 0.1u/16X4

MICRO-START INT'L CO.,LTD.

Title: USB Front Side

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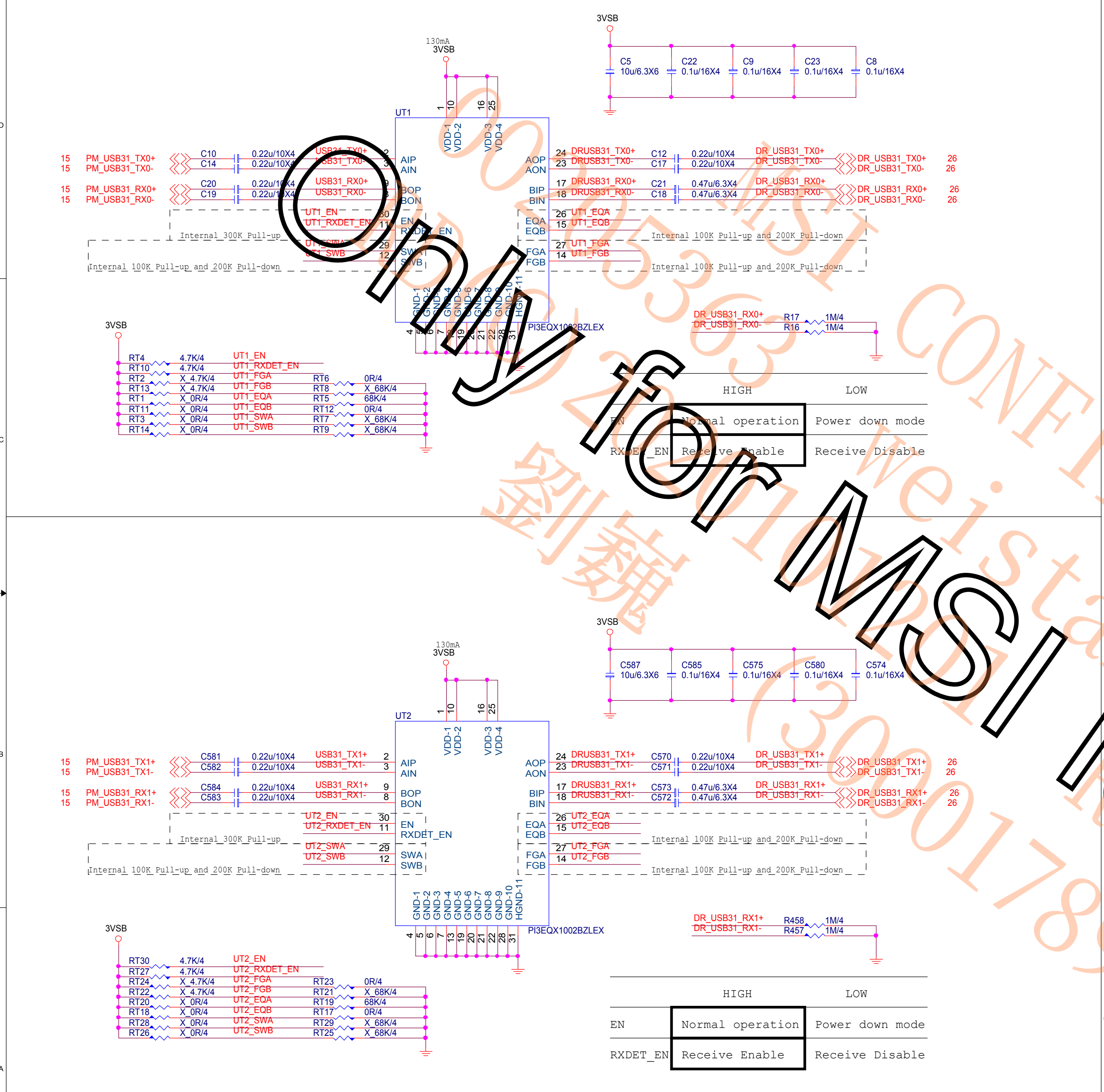

EQA/B are the selection pins for the equalization selection

EQA/B	Equalizer setting (dB) @2.5GHz	@5GHz
0	5.1	10.9
R	1.9	6.7
F	3.5	8.9 (Default)
1	6.8	13.1

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

FGA/B	Flat Gain Settings dB
0	-3
R	-1.5
F	0 (Default)
1	+2

-1dB compression point linear Swing Setting:

SWA/B are the selection bits for the output linear swing setting

SWA/B	Output Linear Swing Settings mVppd
0	800
R	1200
F	1000 (Default)
1	1100

MICRO-START INT'L CO.,LTD.

Title: USB 3.1 Gen2 redriver

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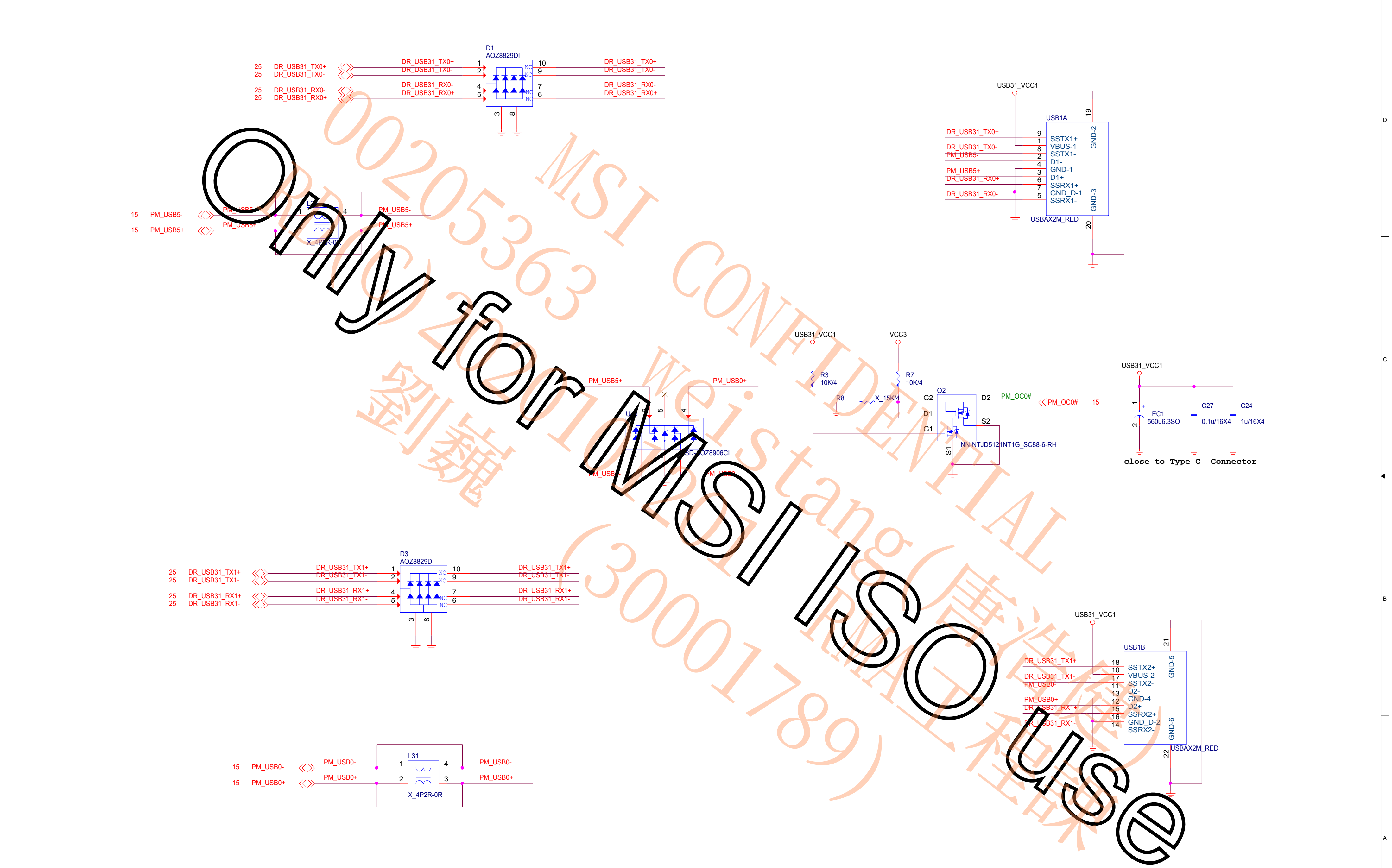
D1
AOZ8829DI
DR_USB31_TX0+
DR_USB31_TX0-
DR_USB31_RX0-
DR_USB31_RX0+
L2
X_4P2R-0R
PM_USB5-
PM_USB5+
USB31_VCC1
USB1A
SSTX1+
VBUS-1
SSTX1-
D1-
GND-1
D1+
SSRX1+
GND_D-1
SSRX1-
GND-2
GND-3
USBAX2M_RED
VCC3
R3
10K/4
R7
10K/4
R8
X_15K/4
Q2
G2
D2
D1
S2
G1
S1
PM_OC0#
NN-NTJD5121NT1G_SC88-6-RH
PM_USB0+
PM_USB0-
U4
ESD-AOZ8906CI
EC1
560u6.3SO
C27
0.1u/16X4
C24
1u/16X4
close to Type C Connector
D3
AOZ8829DI
DR_USB31_TX1+
DR_USB31_TX1-
DR_USB31_RX1+
DR_USB31_RX1-
USB1B
SSTX2+
VBUS-2
SSTX2-
D2-
GND-4
D2+
SSRX2+
GND_D-2
SSRX2-
GND-5
GND-6
L31

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	USB 3.1 GEN2 TYPE A*2	
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PCI EXPRESS x16 Slot

3.3V 3.0A
12V 5.5A

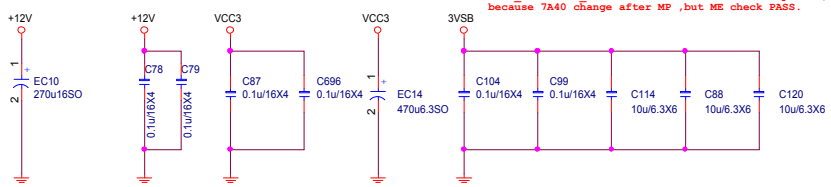
PCIEX1 12V 0.5A
3.3V weak 375mA

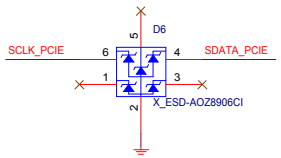
3.3V 3.0A
12V 0.5A

PCI_E1

SLOT-PCI164P_BLACK-2PITCH-RH-51

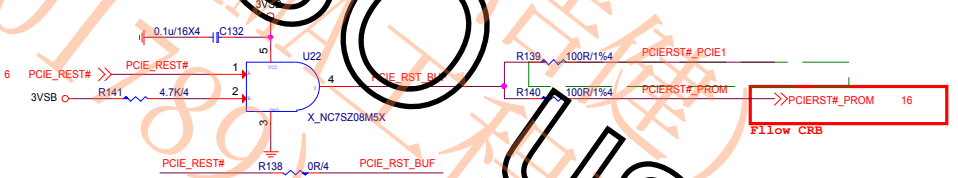
SLOT_PCIEXP164_13 is not N11-1641811-L06 footprint , because 7A40 change after MP ,but ME check PASS.



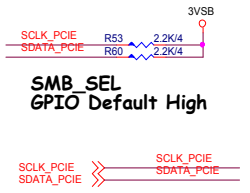


Remove PCIe x1 Slot

within 500mil



SMBus separate circuit



MICRO-START INT'L CO.,LTD.

Title	PCIE X16 SLOT	
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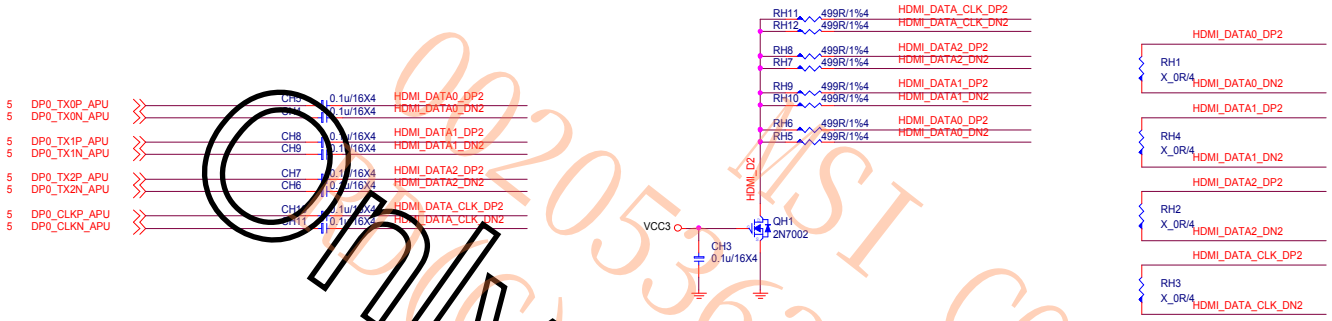
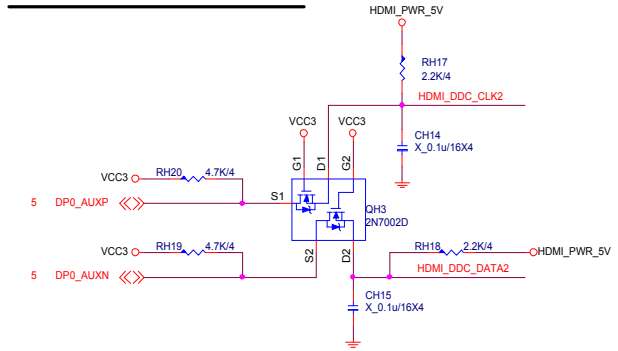
HDMI CONNECTOR

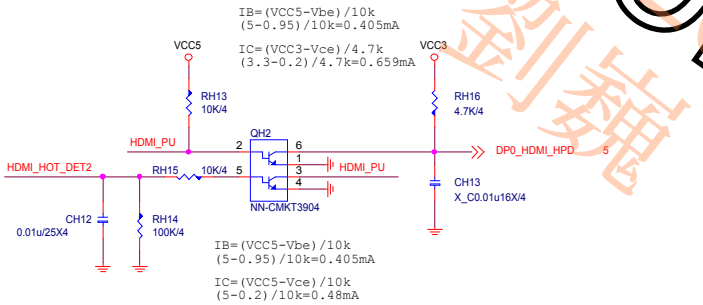
For HDMI 1.4



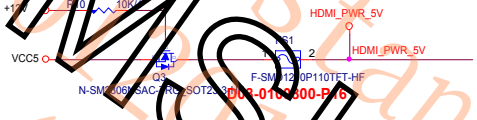
AUX Level Shifter



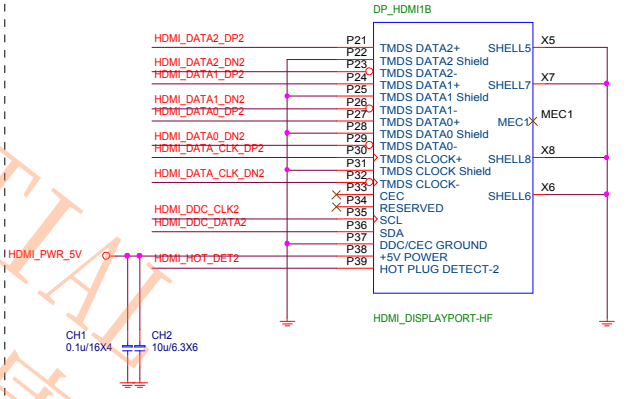
HPD Circuit



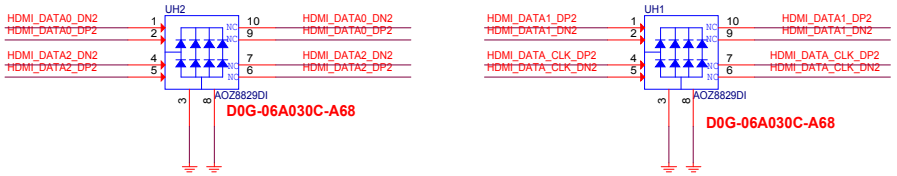
Connector Power



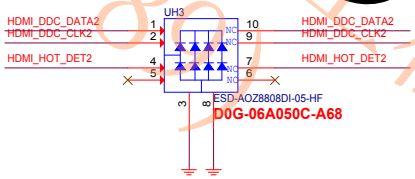
Connector



For EMI



注意:耐壓5V零件



MSI MICRO-START INT'L CO.,LTD.
Link to the Future

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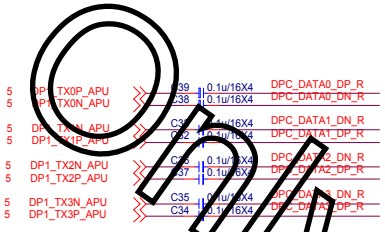
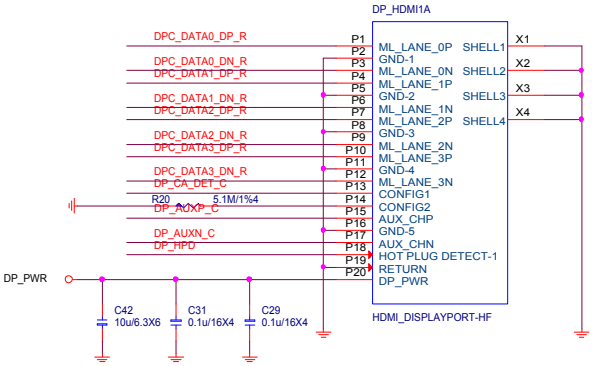
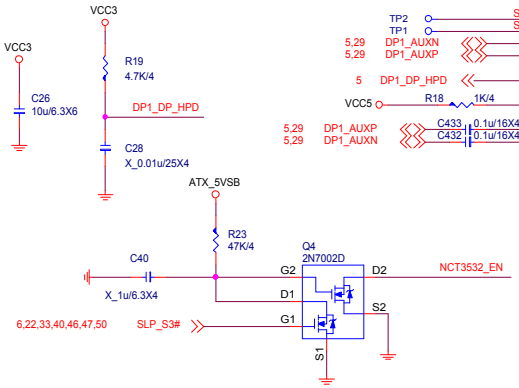
DP CONNECTOR

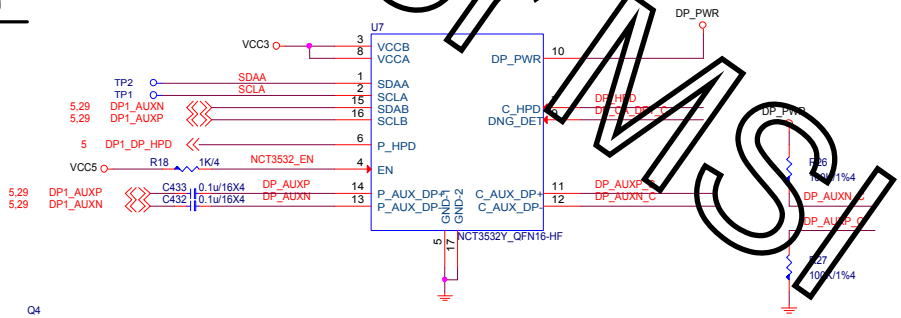




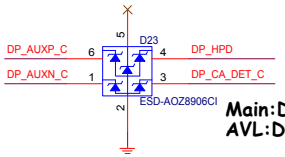
DP AUX & HPD Circuit

Support HDMI Dongle





ESD



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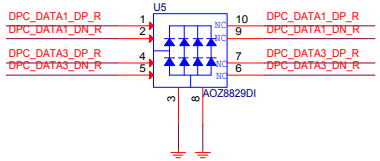
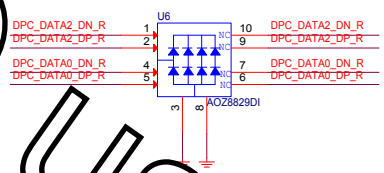
AVL:D0G-45B0510-I14





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Link to the Future

Title: DP Connector		
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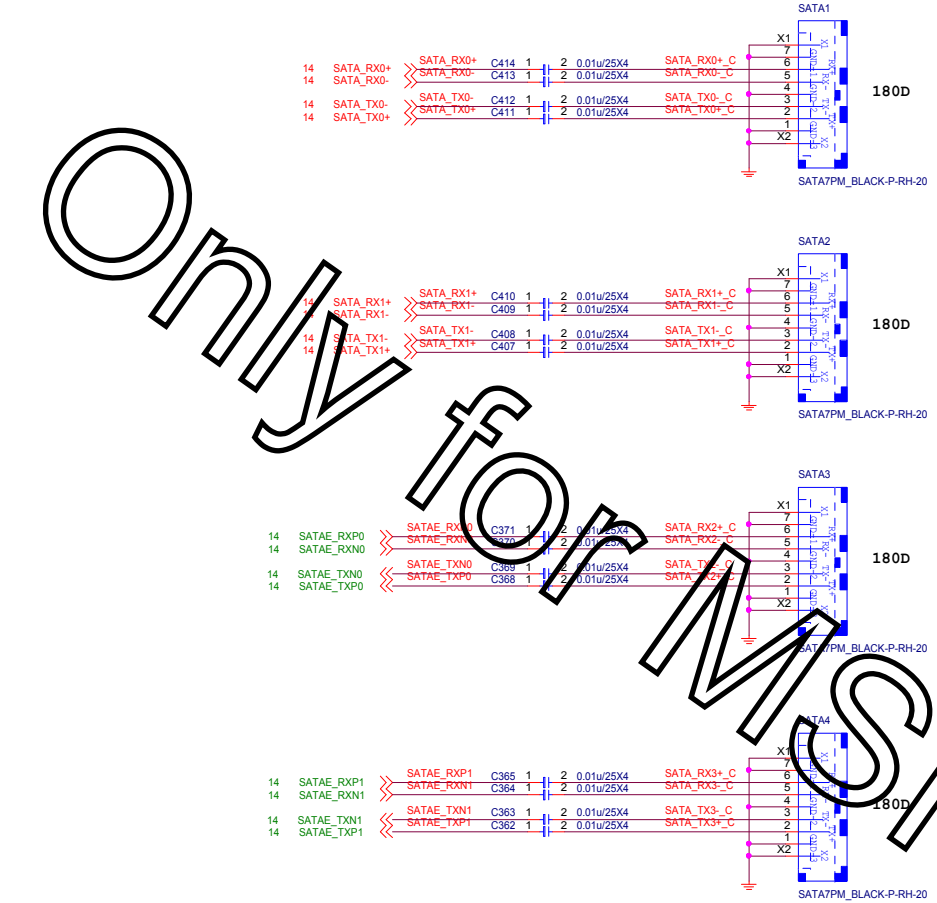
SATA Connector



MICRO-START INT'L CO.,LTD.

Title: SATA Connector		
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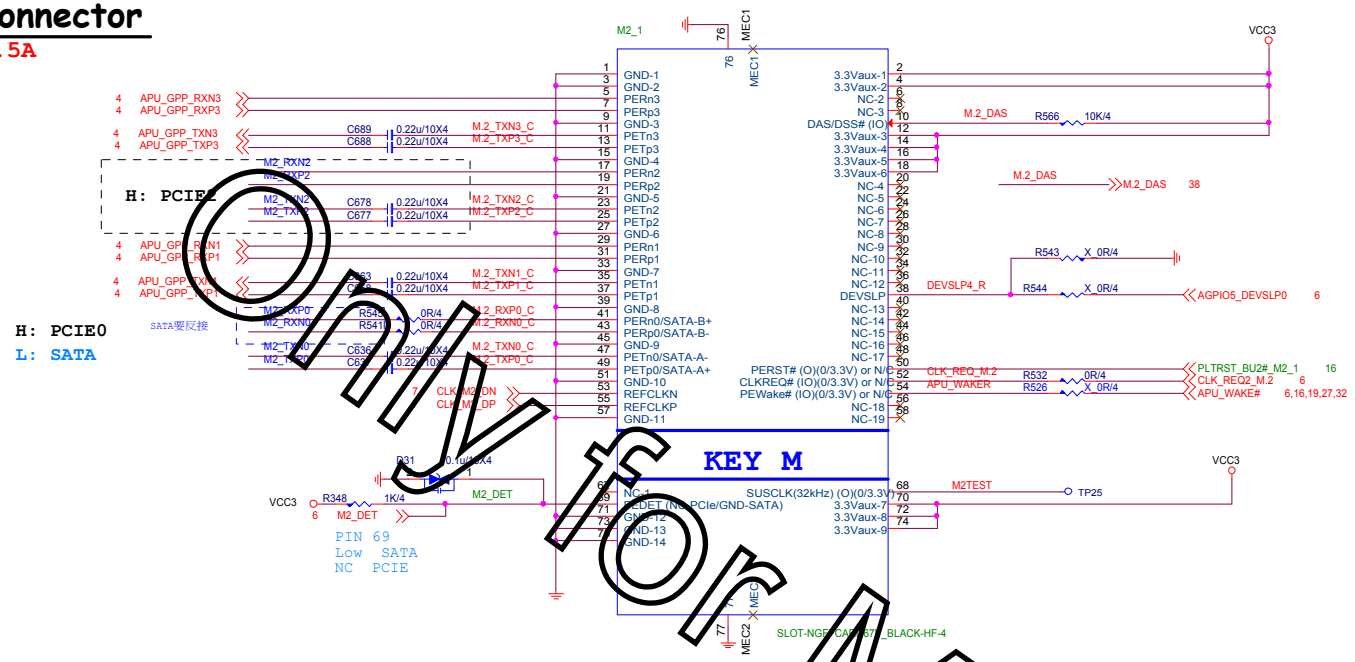
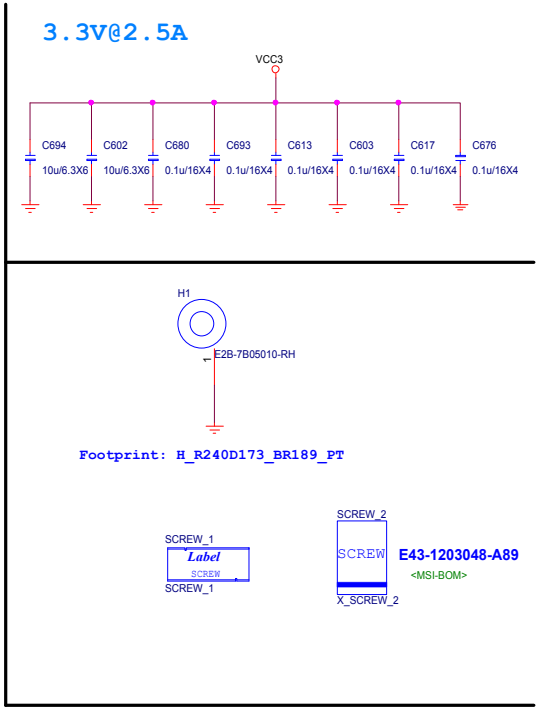
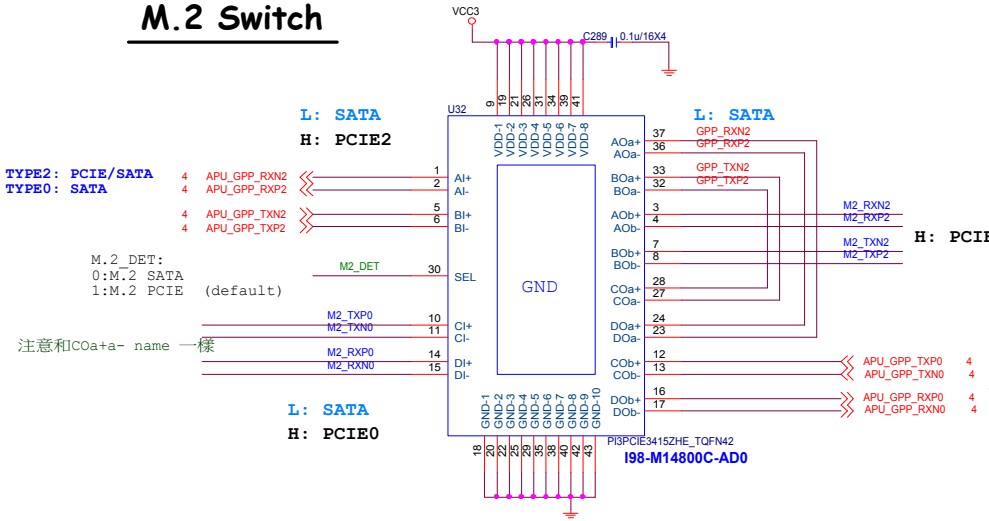
M.2 Connector

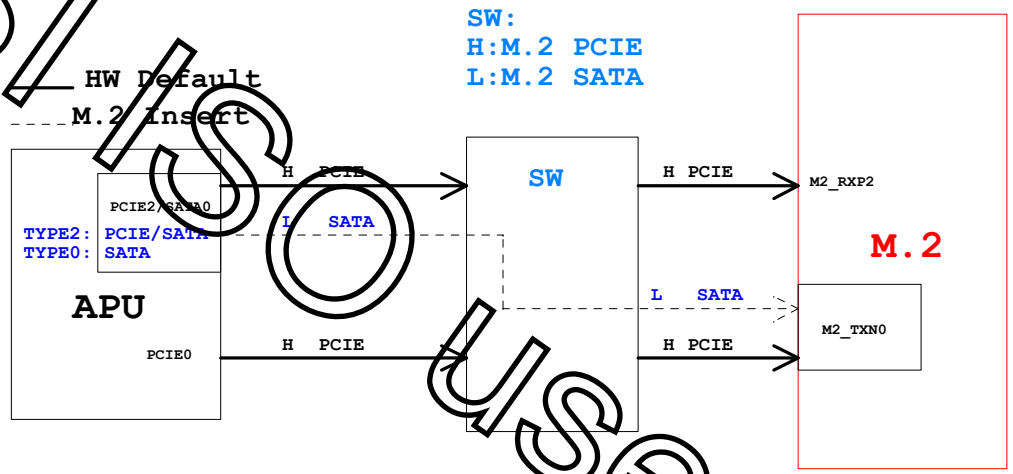
3.3V@2.5A





M.2 Switch





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Title: M2_1		
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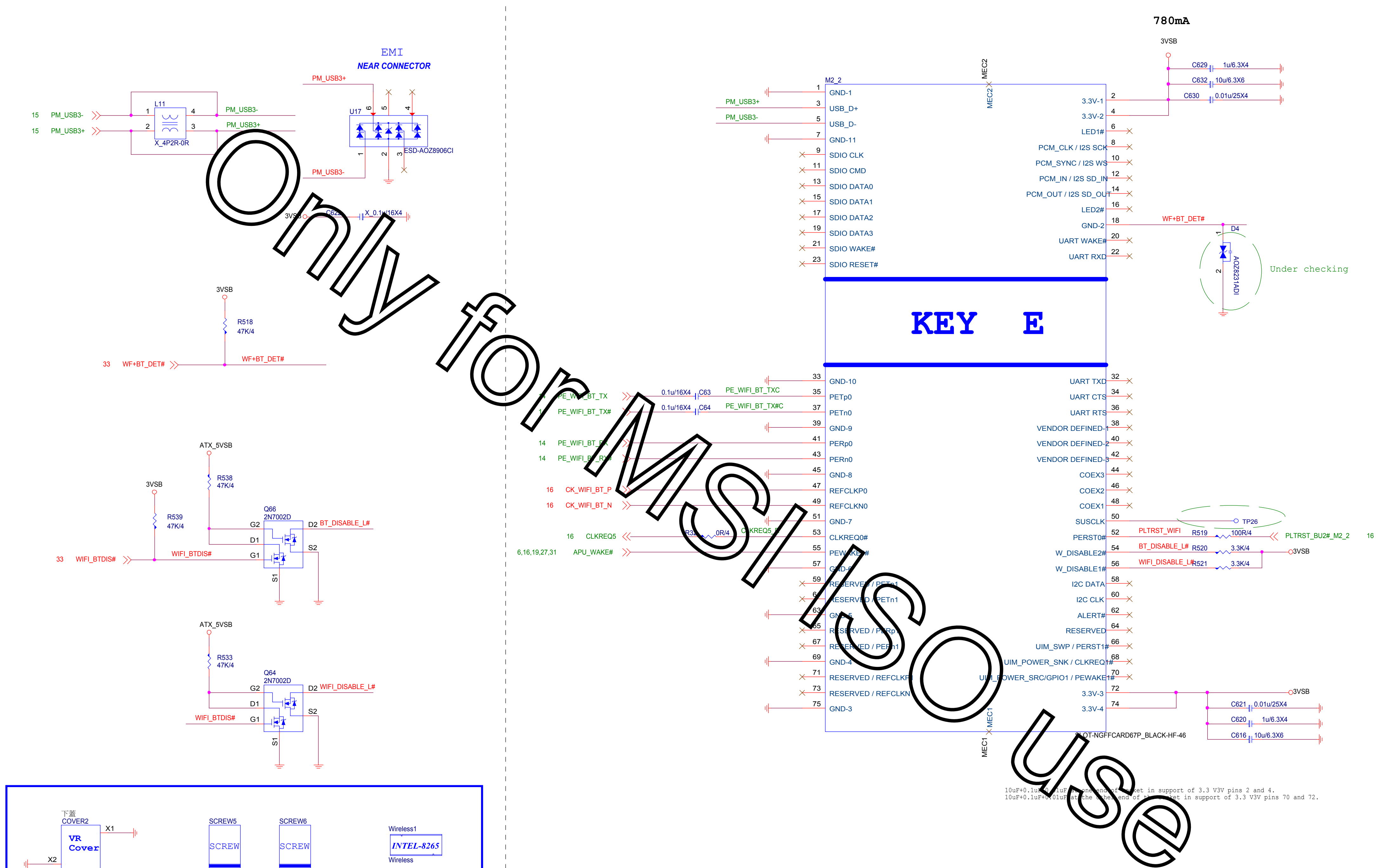

780mA
3VSB
C629 1u/6.3X4
C632 10u/6.3X6
C630 0.01u/25X4
EMI
NEAR CONNECTOR
PM_USB3+
PM_USB3-
U17
ESD-AOZ8906CI
L11
X_4P2R-0R
15 PM_USB3-
15 PM_USB3+
C628 X_0.1u/16X4
3VSB
R518 47K/4
33 WF+BT_DET#
WF+BT_DET#
M2_2
MEC2
GND-1
USB_D+
USB_D-
GND-11
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
SDIO DATA2
SDIO DATA3
SDIO WAKE#
SDIO RESET#
3.3V-1
3.3V-2
LED1#
PCM_CLK / I2S SCK
PCM_SYNC / I2S WS
PCM_IN / I2S SD_IN
PCM_OUT / I2S SD_OUT
LED2#
GND-2
UART WAKE#
UART RXD
WF+BT_DET#
D4
AOZ8231ADI
Under checking
KEY E
GND-10
PETp0
PETn0
GND-9
PERp0
PERn0
GND-8
REFCLKP0
REFCLKN0
GND-7
CLKREQ0#
PEWAKE0#
GND-6
RESERVED / PETp1
RESERVED / PETn1
GND-5
RESERVED / PERp1
RESERVED / PERn1
GND-4
RESERVED / REFCLKP1
RESERVED / REFCLKN1
GND-3
UART TXD
UART CTS
UART RTS
VENDOR DEFINED-1
VENDOR DEFINED-2
VENDOR DEFINED-3
COEX3
COEX2
COEX1
SUSCLK
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C DATA
I2C CLK
ALERT#
RESERVED
UIM_SWP / PERST1#
UIM_POWER_SNK / CLKREQ1#
UIM_POWER_SRC/GPIO1 / PEWAKE1#
3.3V-3
3.3V-4
MEC1
SLOT-NGFFCARD67P_BLACK-HF-46
0.1u/16X4 C63 PE_WIFI_BT_TXC
0.1u/16X4 C64 PE_WIFI_BT_TX#C
14 PE_WIFI_BT_TX
14 PE_WIFI_BT_TX#
14 PE_WIFI_BT_RX
14 PE_WIFI_BT_RX#
16 CK_WIFI_BT_P
16 CK_WIFI_BT_N
16 CLKREQ5
R32 0R/4 CLKREQ5_R
6,16,19,27,31 APU_WAKE#
TP26
PLTRST_WIFI R519 100R/4 PLTRST_BU2#_M2_2 16
BT_DISABLE_L# R520 3.3K/4 3VSB
WIFI_DISABLE_L# R521 3.3K/4
3VSB
C621 0.01u/25X4
C620 1u/6.3X4
C616 10u/6.3X6
10uF+0.1uF+0.1uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.
ATX_5VSB
R538 47K/4
3VSB
R539 47K/4
Q66 2N7002D
D2 BT_DISABLE_L#
33 WIFI_BTDIS#
WIFI_BTDIS#
ATX_5VSB
R533 47K/4
Q64 2N7002D
D2 WIFI_DISABLE_L#
WIFI_BTDIS#
下蓋
COVER2
VR Cover
X1
X2
X_E21-4437010-RH
E21-4437010-A91
SCREW5
SCREW
鎖WiFi Module螺絲
E43-1204046-P65
SCREW6
SCREW
鎖WiFi Module螺絲
E43-1204046-P65
Wireless1
INTEL-8265
Wireless

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: M2_2(WIFI & BT)

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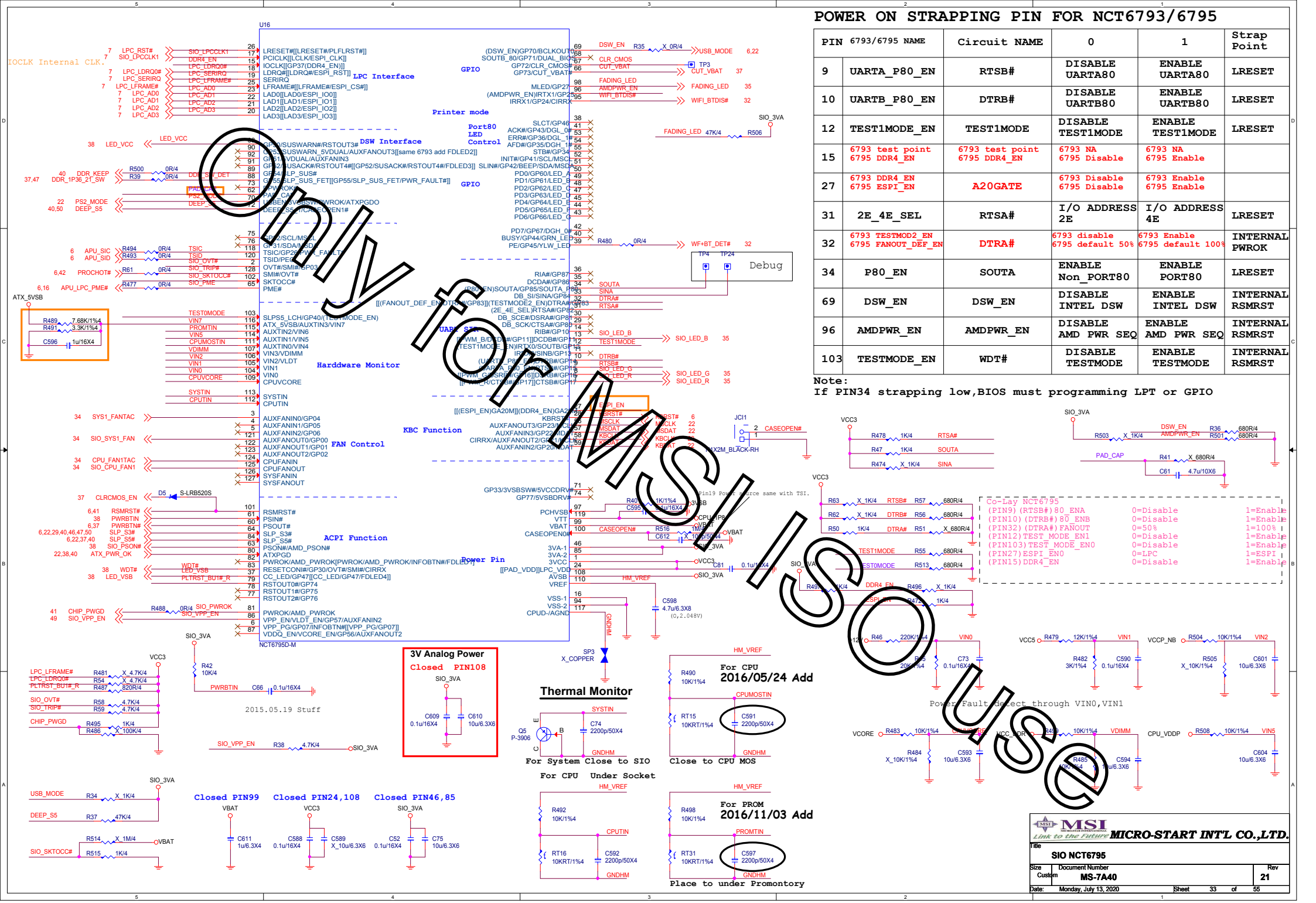

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

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Title	SIO NCT6795	
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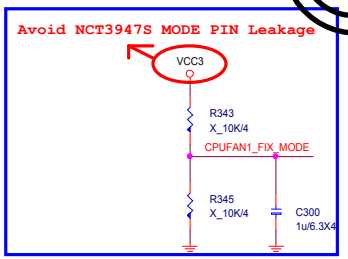
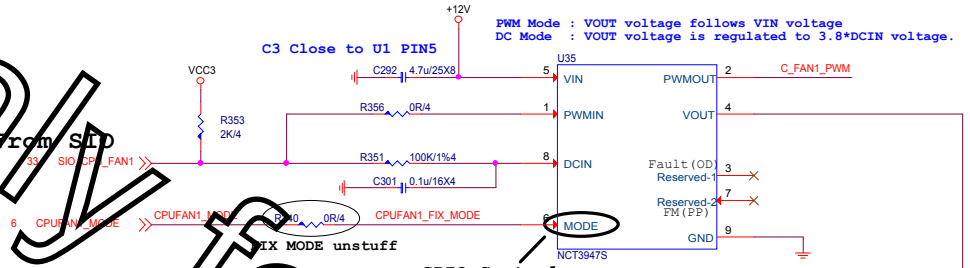
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切換 PWM/DC MODE



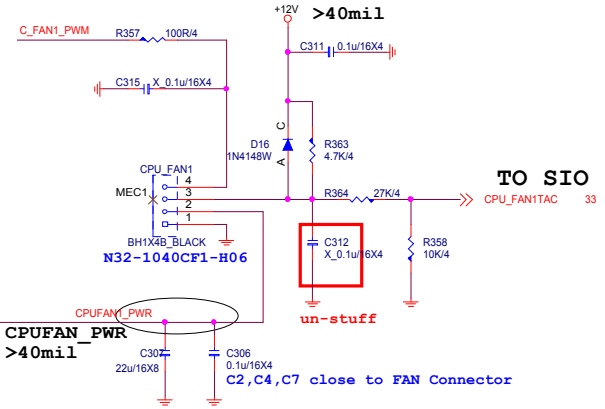
Resever For FIX DC or PWM MODE USE By PM SPEC

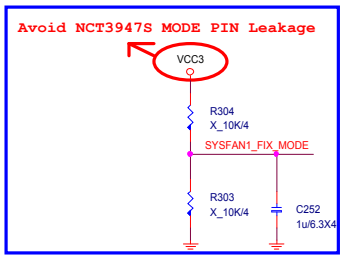


GPIO Control

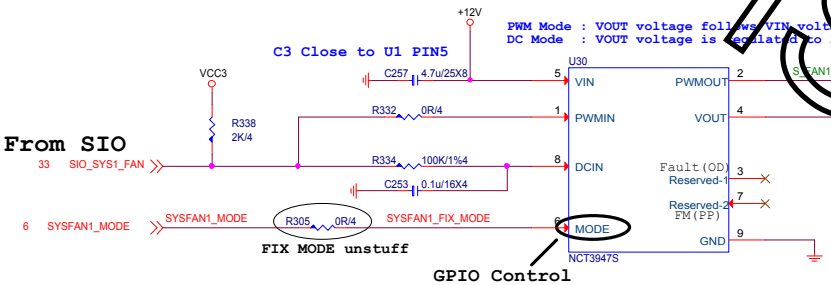
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V





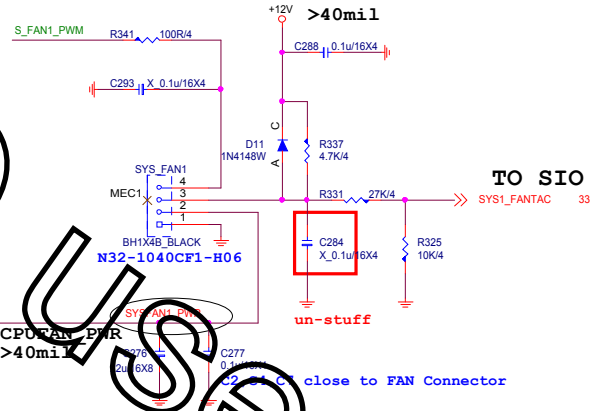
Resever For FIX DC or PWM MODE USE By PM SPEC



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future
Title: CPU/SYS FAN Control TYPE K
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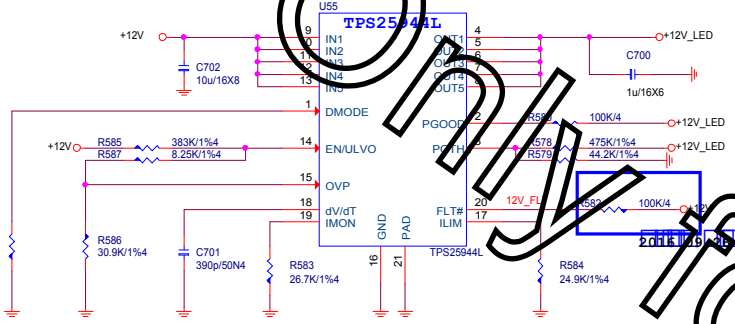
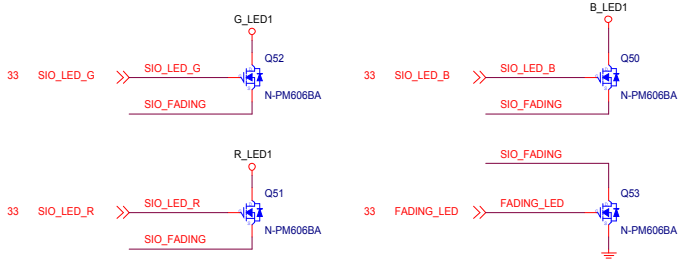
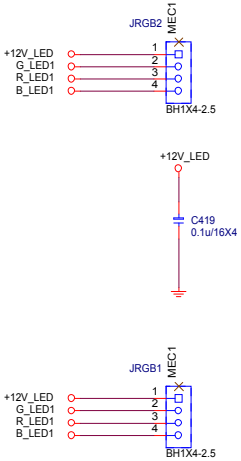
定義:外接LED 燈條
---- 彩色 : SIO 6795D-M(128pin) : OB2-7A58001
---- 單色 : SIO 5565(64pin) : B02-5565D04-N62
---- PCB 文字面 (JLED)
---- 手冊 註明接頭支援標準 5050 RGB or 單色 LED 共陽燈條 (12V+/G/R/B) or (12V+/-/S/-) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

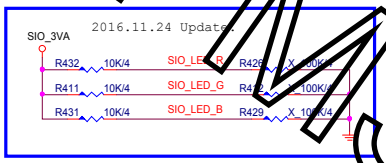
JLED



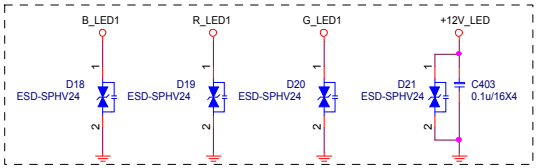




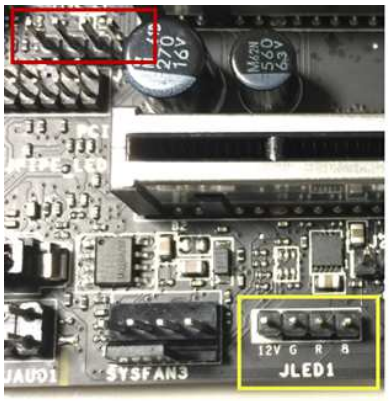
Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1



2016.08.31 StuFF

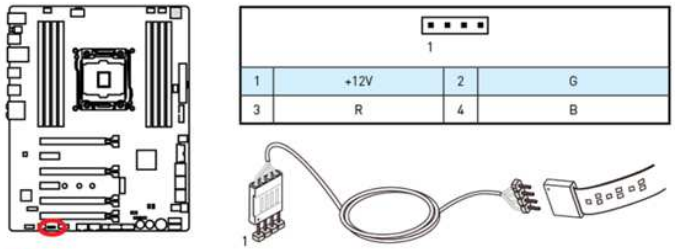


close to JLED2



JLED1: RGB LED connector

This connector allows you to connect the RGB LED strip.

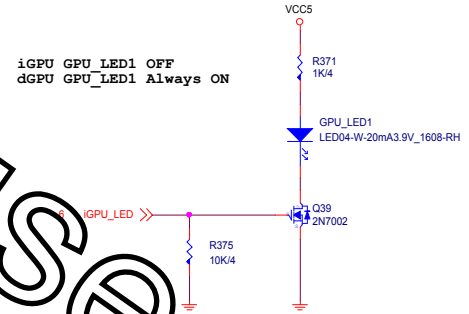


Important

- *This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.*
- *Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.*
- *Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.*

AM4 APU Detect LED Circuit

iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON



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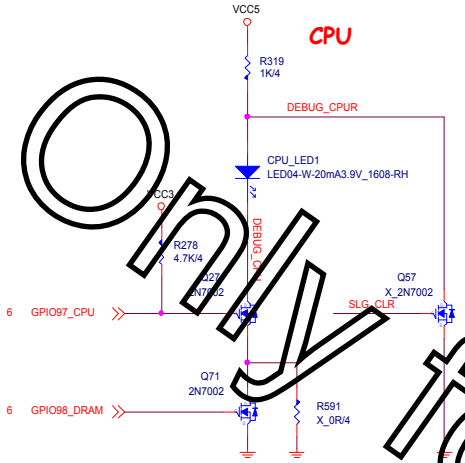
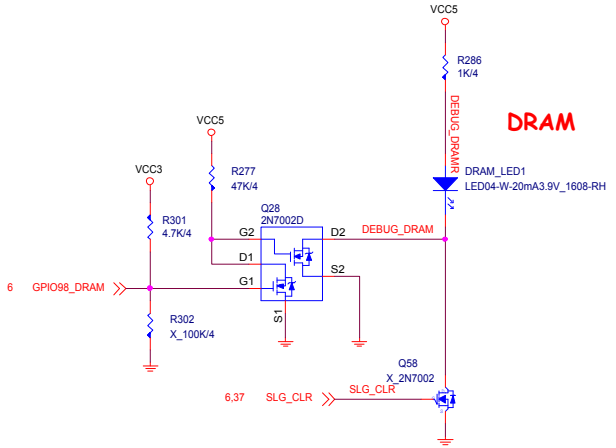
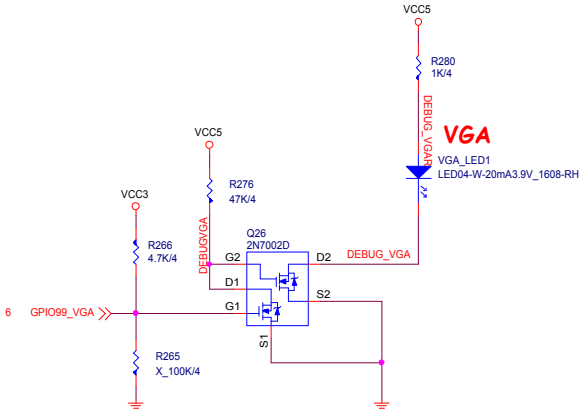
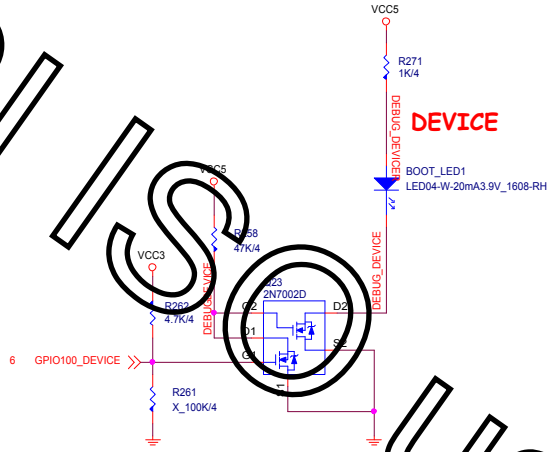
EZ Debug LED









LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

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MICRO-START INT'L CO.,LTD.

Title	EZ Debug LED		
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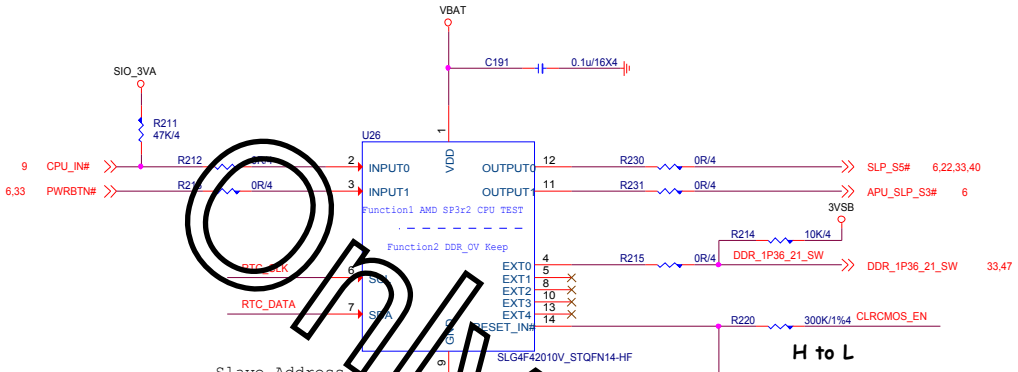
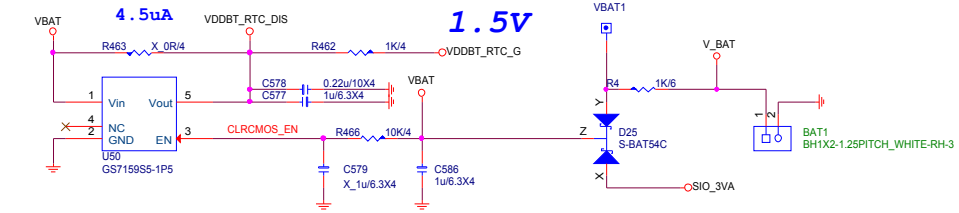
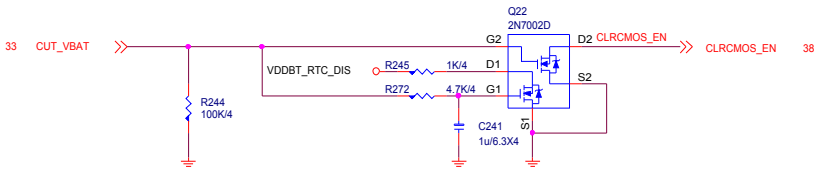
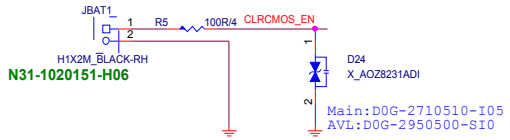


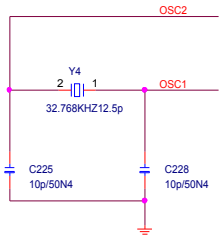
RTC & Clear CMOS Circuit

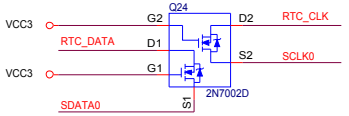
Placement Bottom Side

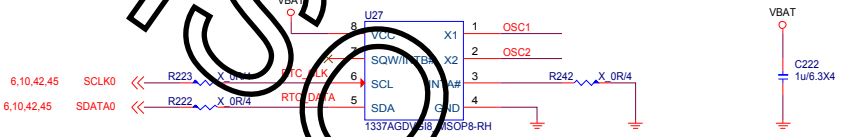












MICRO-START INT'L CO.,LTD.

Title: RTC Circuit / Moat Cap

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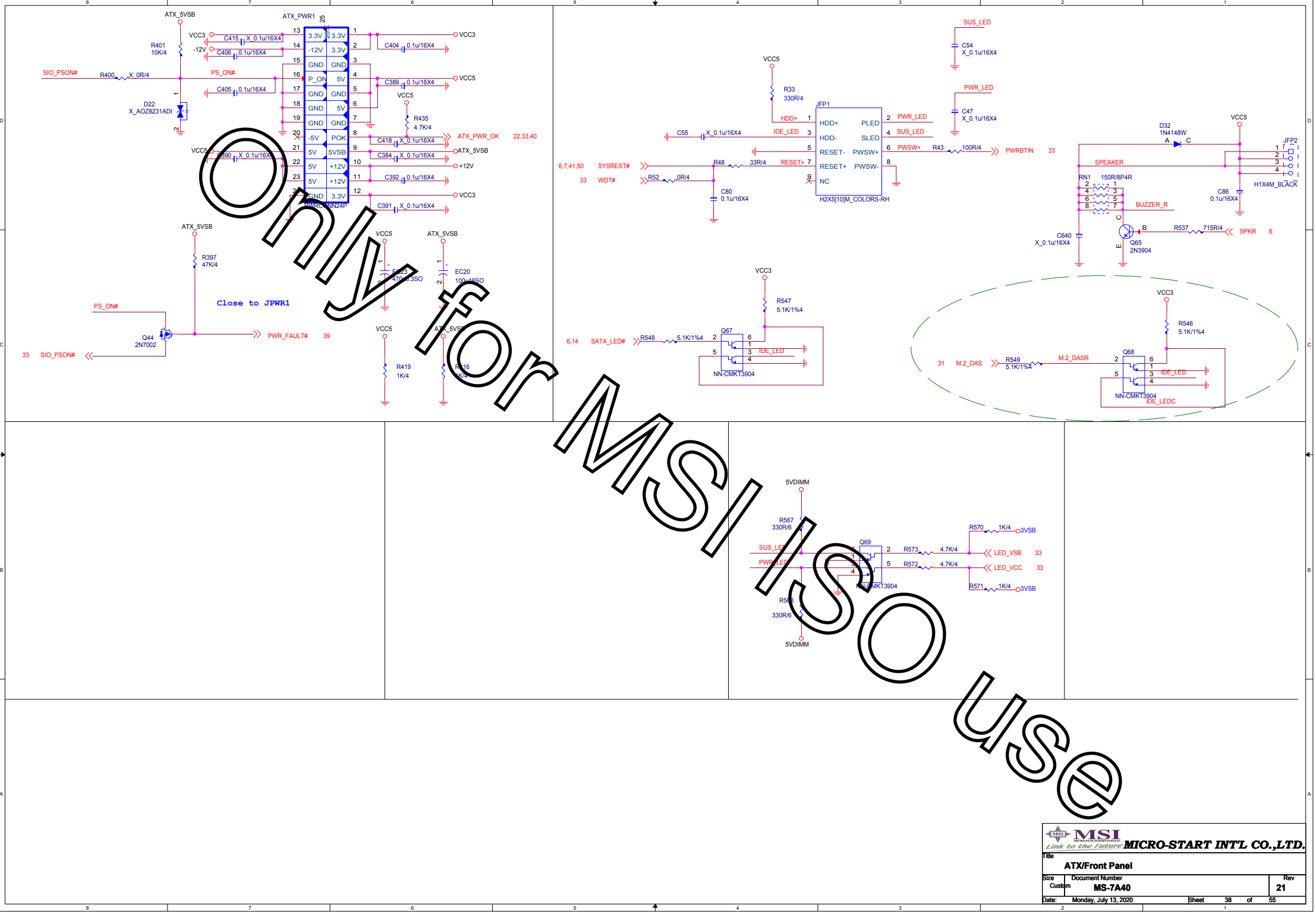

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	ATX/Front Panel	
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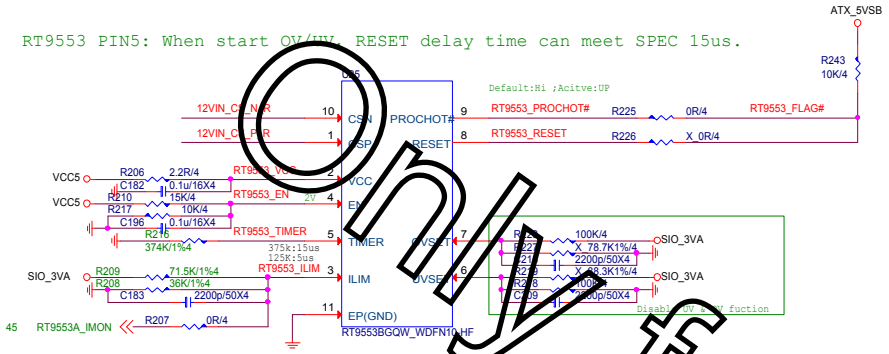
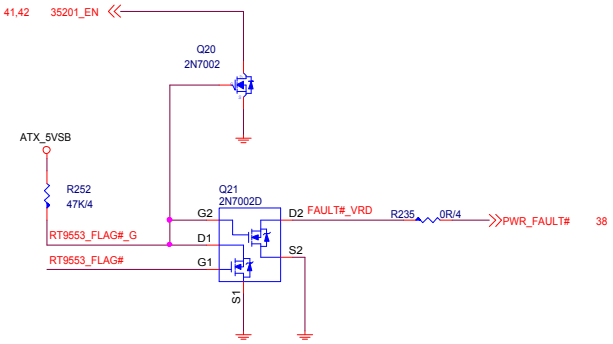
RT9553B CURRENT SENSE

VCORE EDC MAC 125A

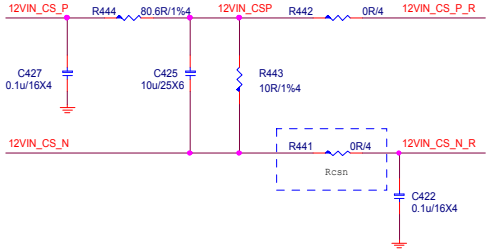
NB EDC MAX75A



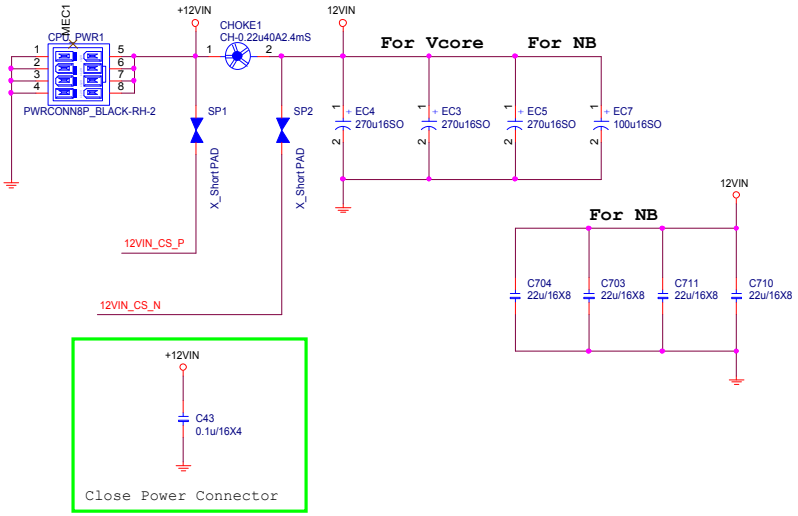
OCP = 37A(default)



(set OCP=37A)



CPU POWER CONNECTOR



D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.5	> output Vcore
D	=	0.125	

I o = Icore(max)*0.8			
I core(max)	=	125	> Vcore current
I avg.	=	100	A

I ripple={ Io*√ D*√ (1-D)} / Phase			
Phase	=	6	phase
I ripple	=	[illegible]	A

5.511982

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

CORE:
D = Vout/Vin
= 1.5/12
= 0.125
N = 6
Irms = Iout * [D/N - (D)^2]^(1/2)
= 125 * (0.02083 - 0.015625)^(1/2)
= 9.0182A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.2	> output Vcore
D	=	0.1	

I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A

I ripple={ Io*√ D*√ (1-D)} / Phase			
Phase	=	2	phase
I ripple	=	9	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

NB:
D = Vout/Vin
= 1.2/12
= 0.1
N = 2
Irms = Iout * [D/N - (D)^2]^(1/2)
= 75 * (0.05 - 0.01)^(1/2)
= 15A

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Link to the Future

Title	RT9553 CURRENT SENSE		
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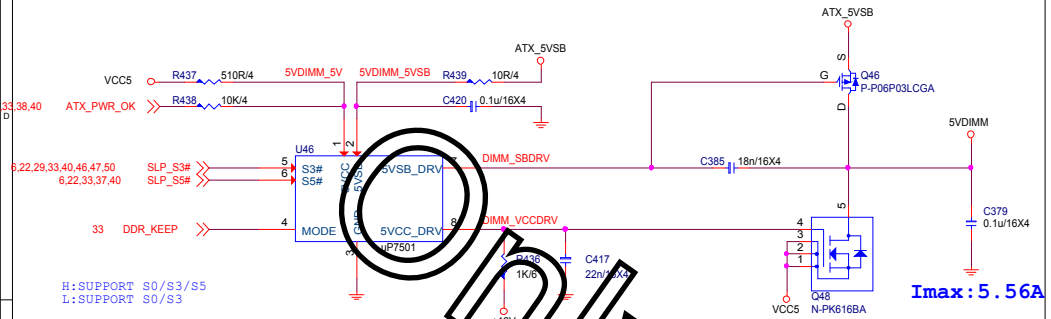
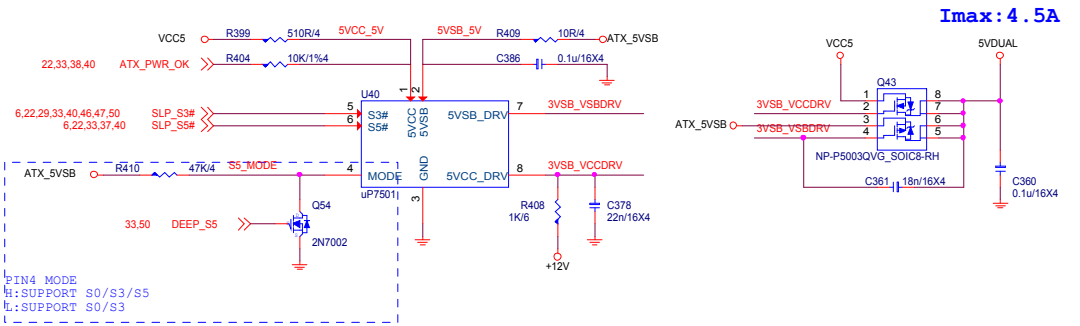
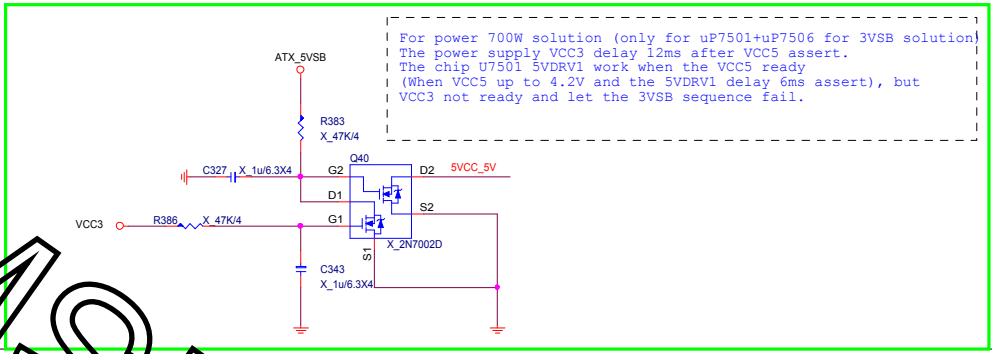
5VDIMM FOR DDR

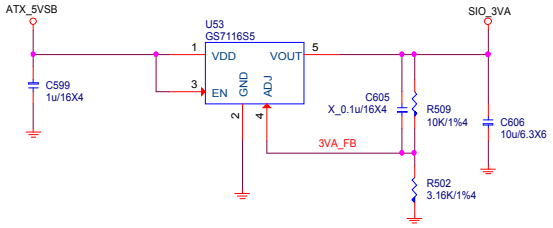


5VDUAL For 3VSB、CPU 1.8V 、 VDDP

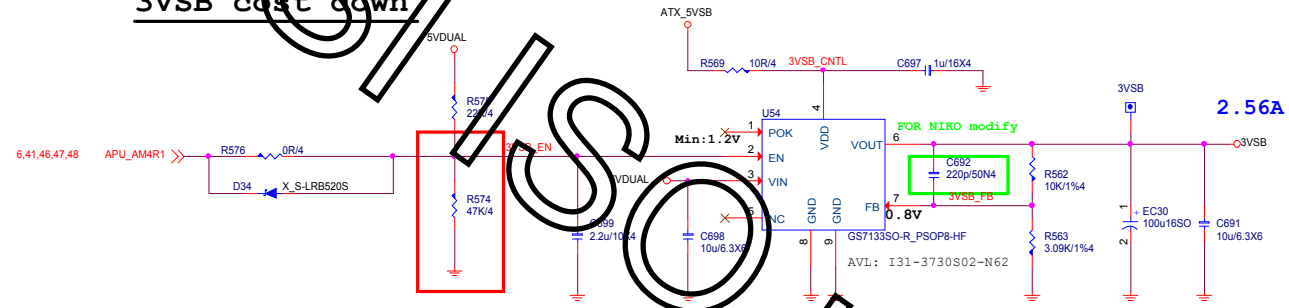




SIO_3VA



3VSB cost down



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Link to the Future

Title	ACPI uPI-5VDIMM&3VSB	
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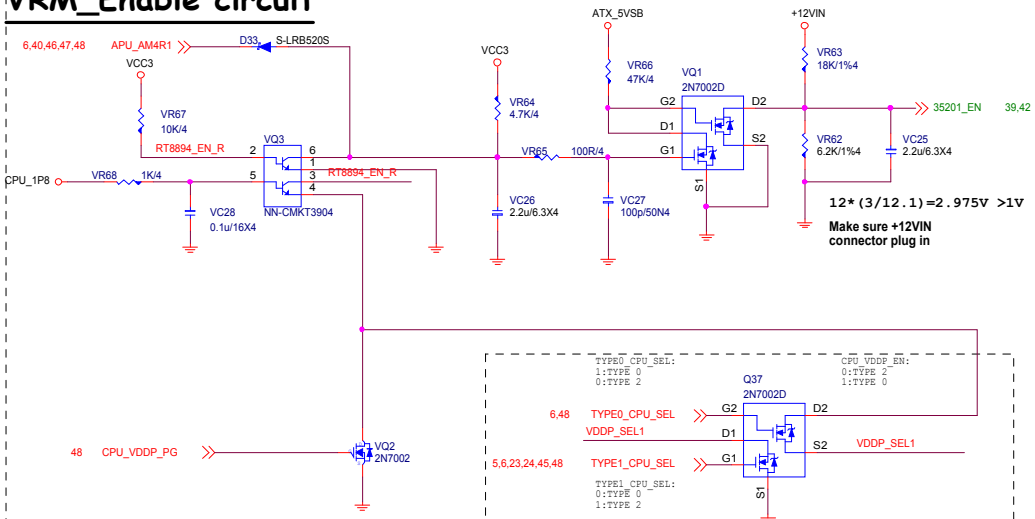
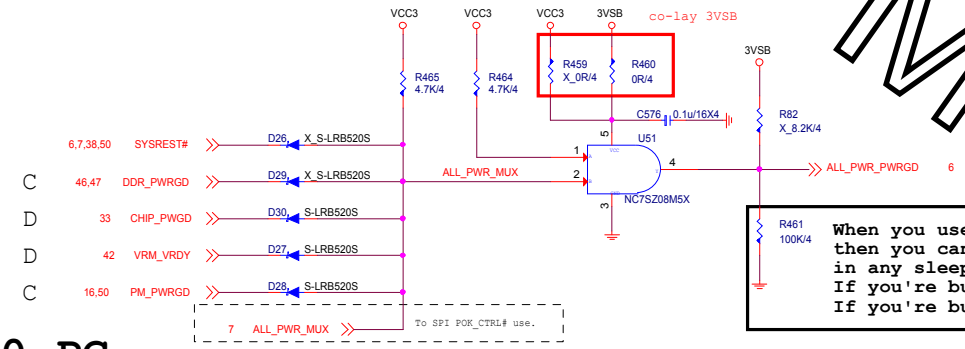
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

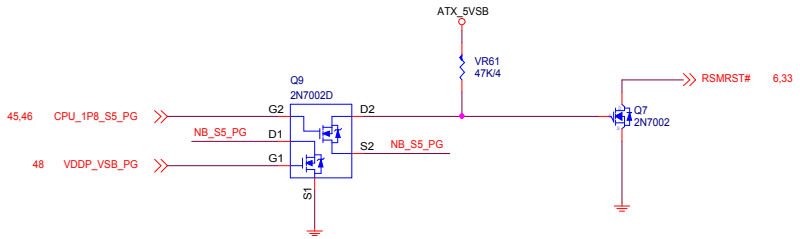


R461 100K/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



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Title	PWR Sequence	
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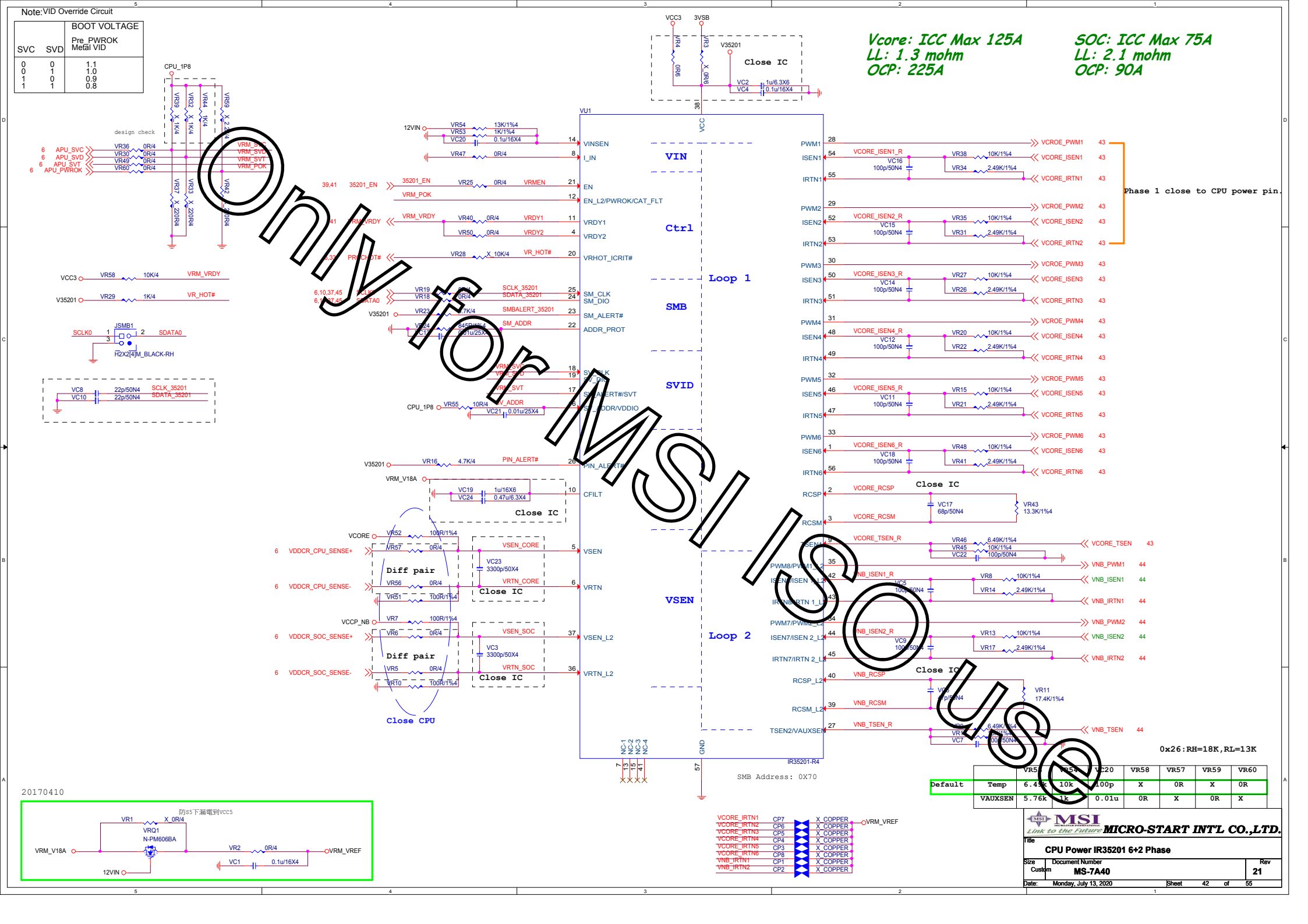
Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vcore: ICC Max 125A
LL: 1.3 mohm
OCP: 225A

SOC: ICC Max 75A
LL: 2.1 mohm
OCP: 90A



MICRO-START INT'L CO.,LTD.
Link to the Future

Title: CPU Power IR35201 6+2 Phase
Size: Custom
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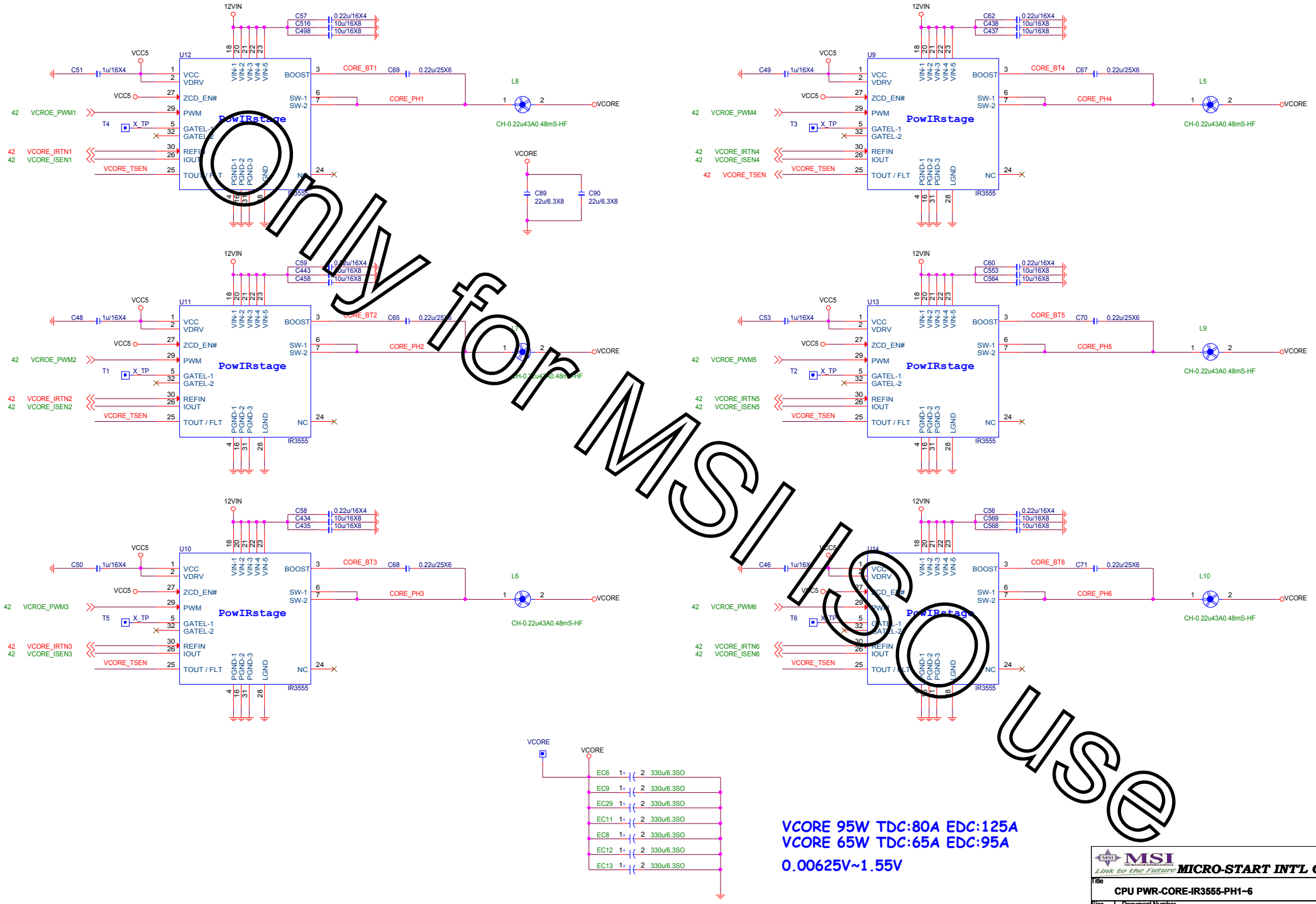

MICRO-START INT'L CO.,LTD.

Title	CPU PWR-CORE-IR3555-PH1~6		
Size: Custom	Document Number: MS-7A40		Rev: 21
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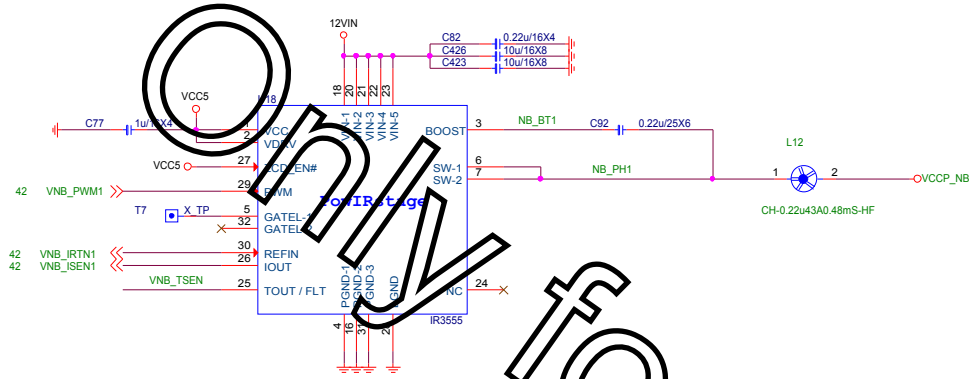
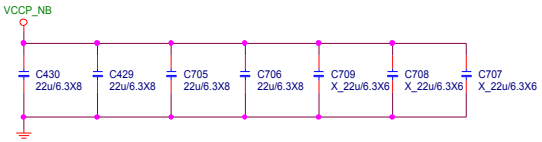
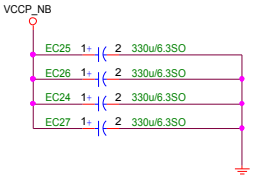
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

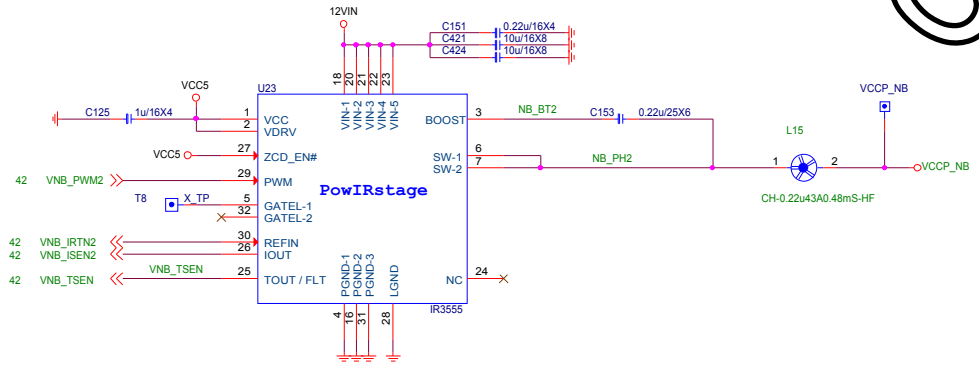
VCCP_NB OCP:100A



0.00625V~1.55V







MSI MICRO-STAR INTERNATIONAL Link to the Future MICRO-START INT'L CO.,LTD.

Title	CPU Power NB Phase 1-2	
Size: Custom	Document Number: MS-7A40	Rev: 21
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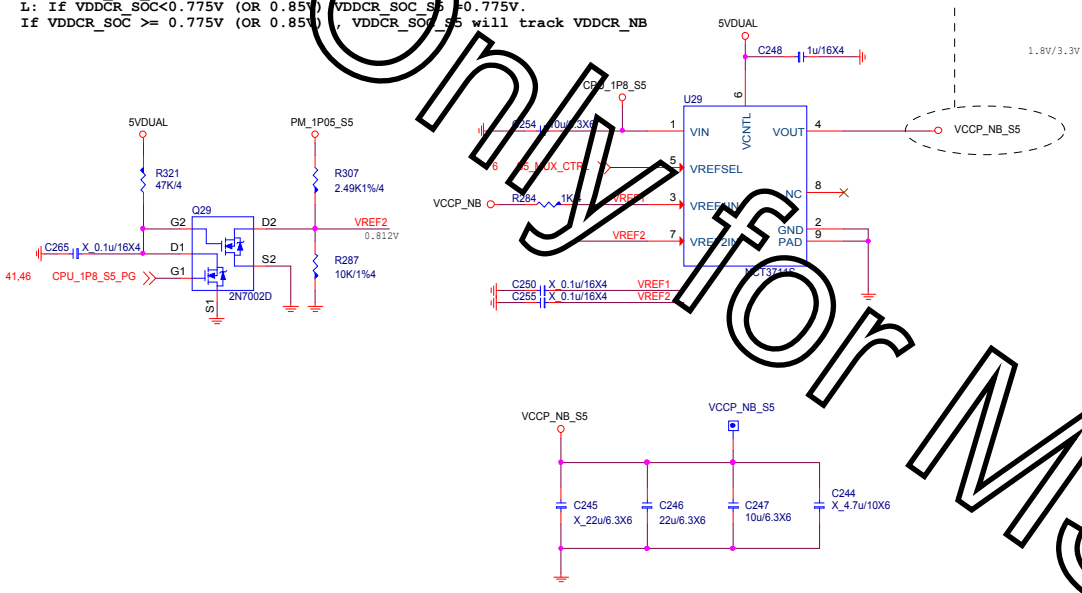
FOR
VCCP_SOC_s5
0.9A

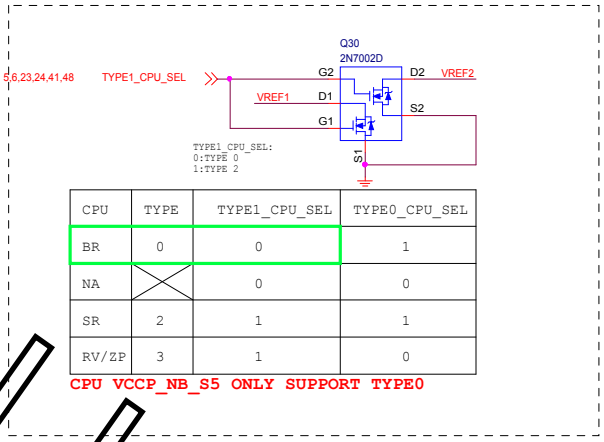
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0



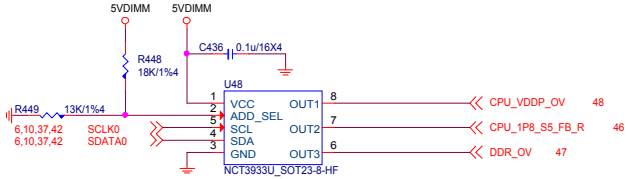


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

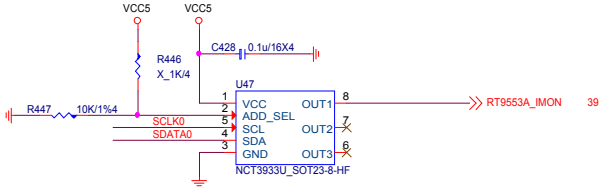
CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

0x26:RH=18K,RL=13K



0x2A:RH=OPEN,RL=10K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Title	CPU Power NB Switch/NCT3933	
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FOR CPU 1.8V S5

0.5A

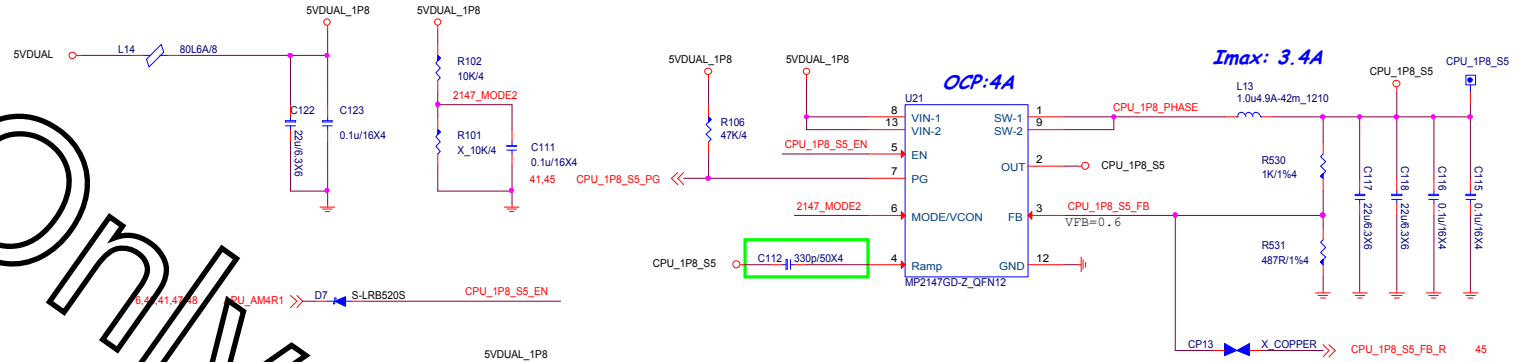
FOR VCCP_SOC_S5

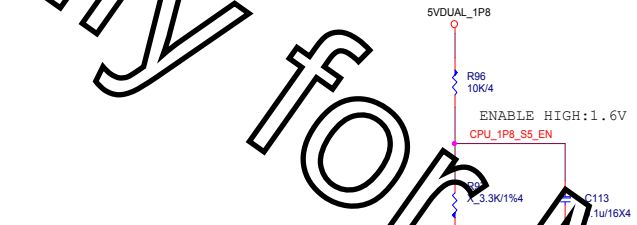
0.9A

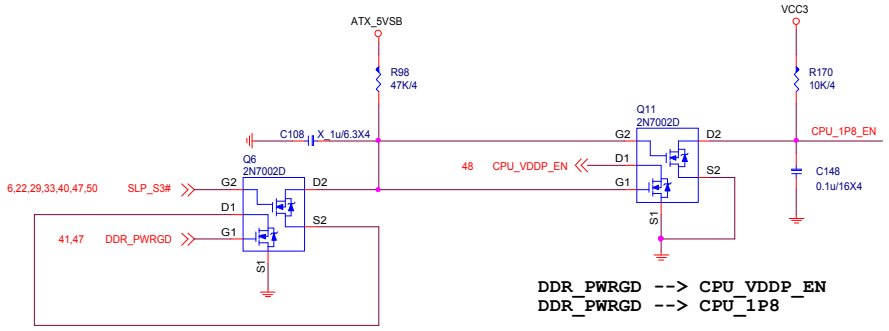
FOR CPU 1.8V S0

2.0A

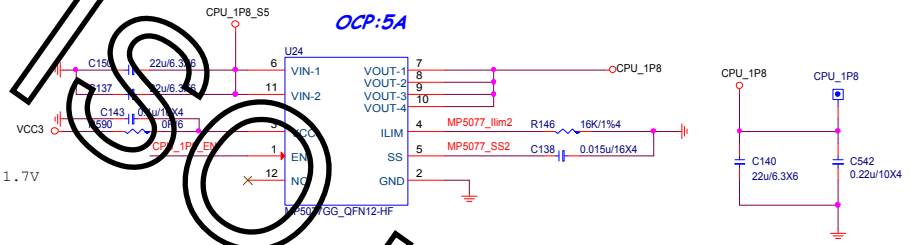
0.5A + 2.0A + 0.9A =3.4A







DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



ENABLE HIGH:1.7V

Ilimit=(1/Rlim)*S,S=80000,when VIN=1.8V
=(1/16)*80000*0.0375A

Tss=(1/3)*(Vout*Css/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n/9uA)=3ms

MICRO-START INT'L CO.,LTD.

Title: CPU Power 1P8V-MP2147

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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM
0.6A FOR DDR VTT

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675 for 1.232V
L	0.75 for 1.369V

2V

Imax: 20.85A

OCP:24A

By layout modify

f:400KHz

R178=90.9K for OCP(dc)=24A (typ) and OCP(dc)=23.8A(min)

27.5A

FB:0.75V

default=1.36V

R195=1K, R181=1.21K,
Vo=0.75V*(1+R195/R181=1.369V

Close to PIN19

1.1uH change to 0.47uH

1.2V

4.7uF*4 per dimm

MICRO-START INT'L CO.,LTD.

Title: DDR Power-RT8231AGQW
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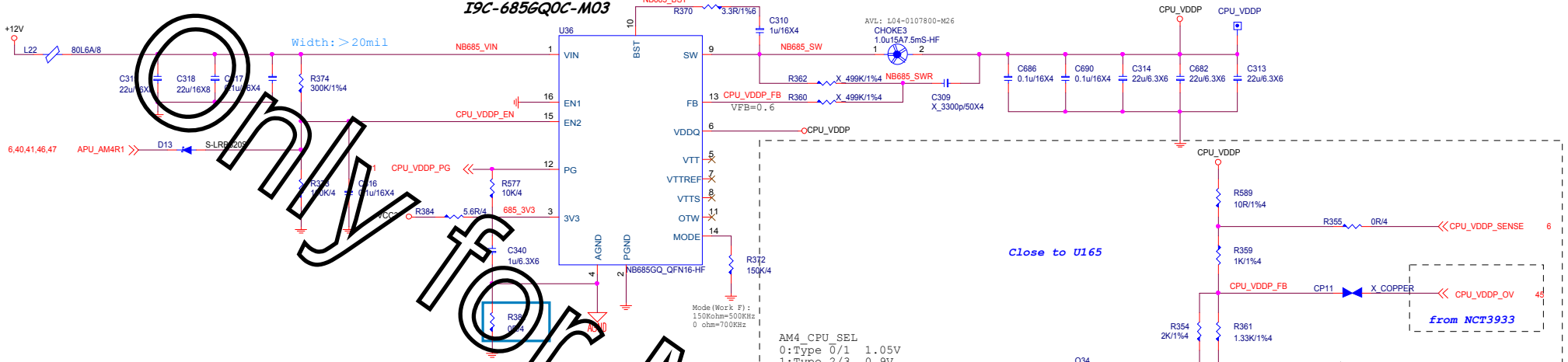
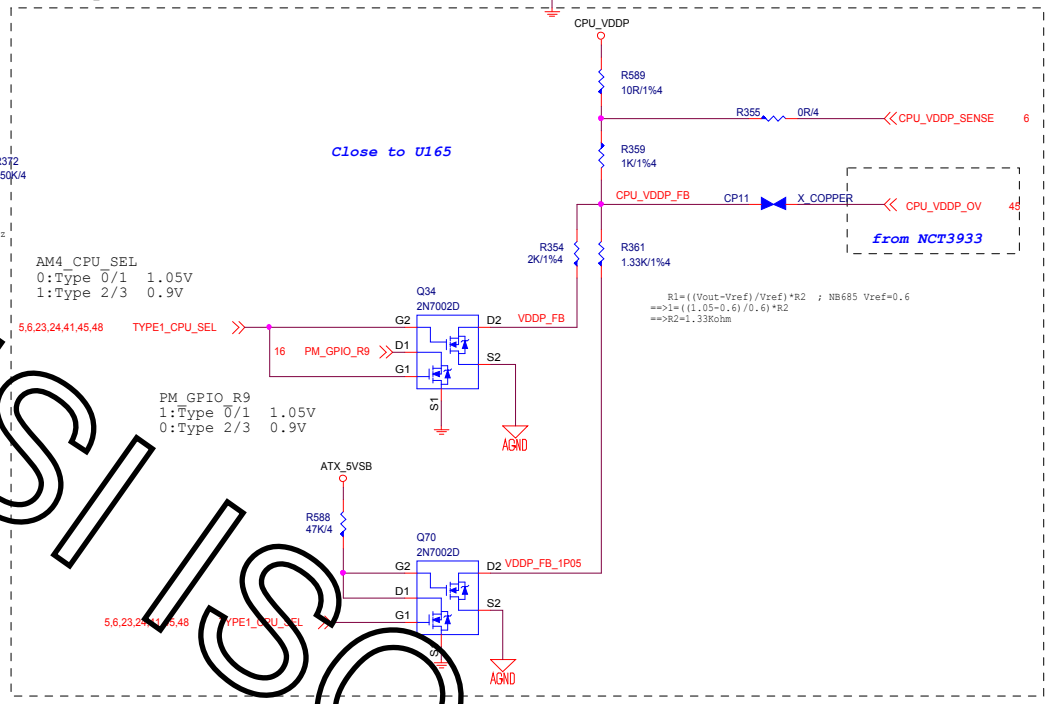
CPU_VDDP_S0

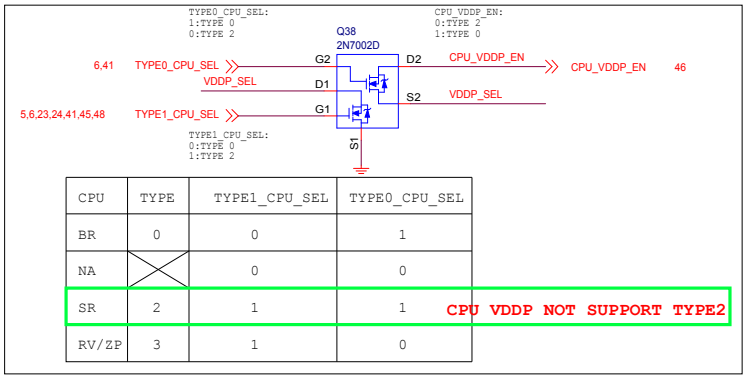
1.05V/0.9
S0:8.5A

OCP=15.45A

I9C-685GQ0C-M03





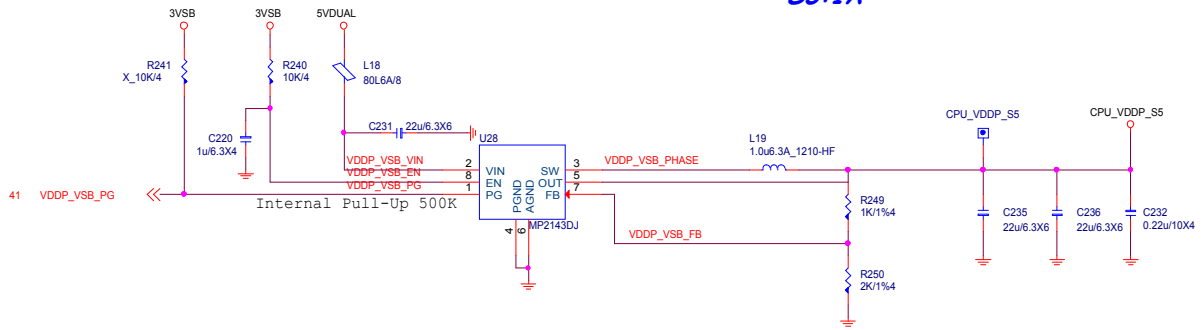


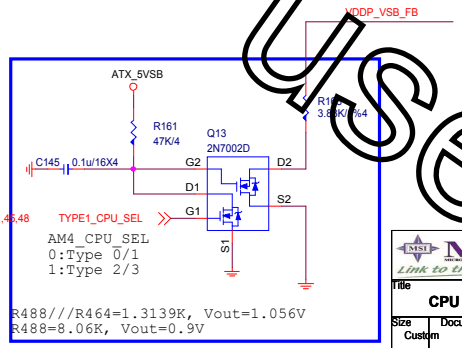
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

CPU_VDDP_S5

VDDP_S5
1.05V/0.9
S5:1A





MICRO-START INT'L CO.,LTD.

Title: CPU Power VDDP-NB685

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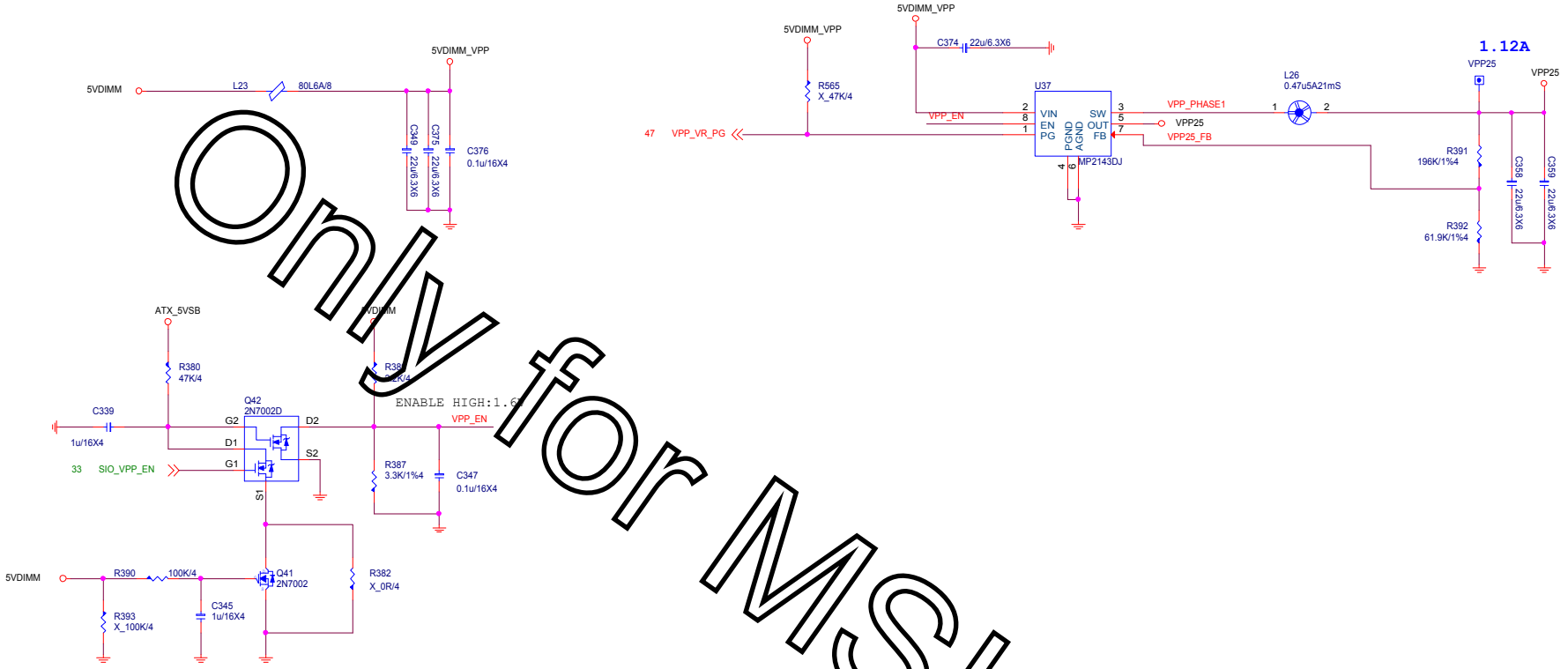
2DIMM :1.12A FOR DDR VPP2.5V



MICRO-START INT'L CO.,LTD.

Link to the Future

Title: DDR PWR VPP25/VTT-MP2143		
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FOR Promontory 1.05V_S0

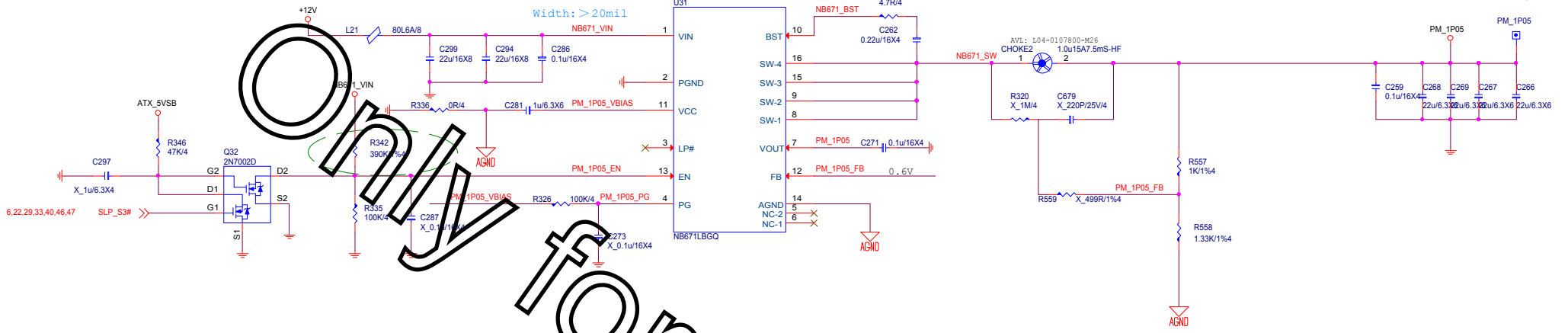
1.05V
S0:5.5A
S5:0.05A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH

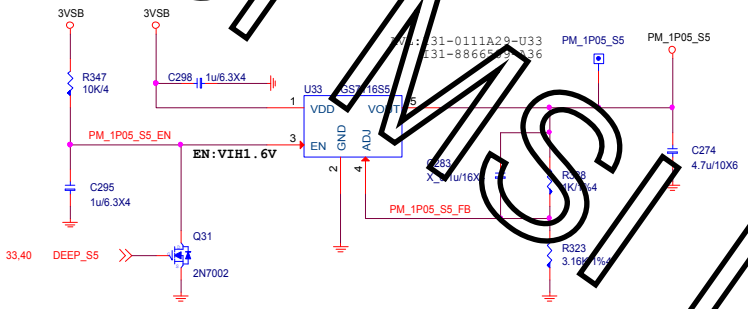
F:500K

1.05V,5.5A



FOR Promontory 1.05V_S5

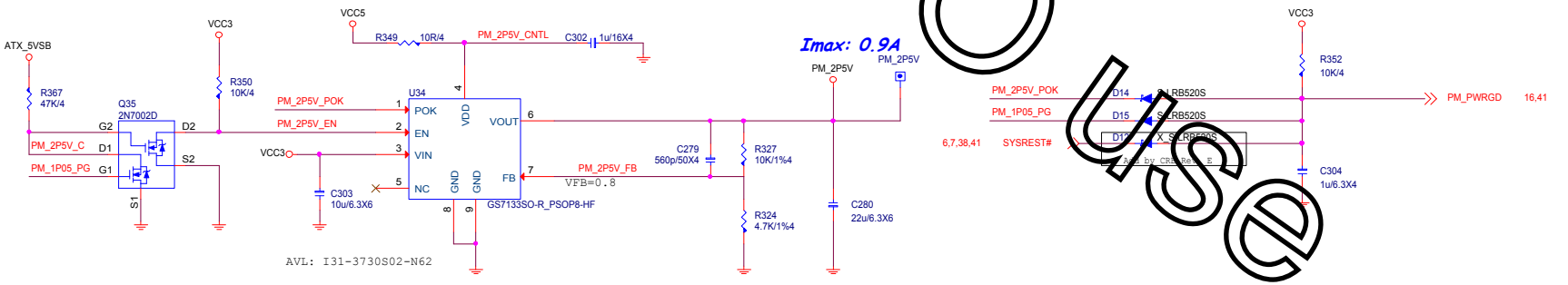
0.05A



Promontory-2.5V

2.5V; 900mA

Imax: 0.9A



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HEAT SINK

PM_HS1

MEC2

MEC1

OE3-7A40001-K08

MOS HS(VCORE)

HS_MOS1

MEC2

MEC1

E31-0007150-K08

CPU Socket

CPU2

E95-0000021-C22

RETENTION MODULE

Simulation

X_JS1

SIM1

X_PIN1*2

X_JS2

SIM2

X_PIN1*2

MANUAL PART

UEFI1

G51-MTSPXXA-A09

BAT1_X1

BAT-BCR2032P-RH

HDMI_LA1

Label

HDMI

HDMI LABEL

MKT1

Label

B450I_GP_AC

B450I_GP_AC

FCH2

Label

FCH_A320_

X_A320

MKT2

Label

MKT_B350I_S01

X_B350I_S01

MKT3

Label

MKT_A320_PRO

X_A320I_PRO

PCB1

7A40-21

PD0-07A4021-G37,精成-深圳,32,微星_寶安恩斯邁廠(MSIS)

MKT4

Label

MKT_A320_SQ1

X_A320I_PRO

CAP1

Label

B350I_S01_470u

X_B350I_S01_470

PCIE1

Label

PCIE_

X_PCIE_S01

CAP2

Label

B350I_S01_270u_

X_B350I_S01_270

MOS HS(NB)

HS_MOS2

MEC2

MEC1

X_HS-0505410-RH

Optics Orientation Holes

MH3

X_MH001

MH1

X_MH001

MH2

X_MH001

5010

FM1 FM4 FM7

X_FM120 X_FM120 X_FM120

5020

FM3 FM2 FM5

X_FM120 X_FM120 X_FM120

FM8 FM6

X_FM120 X_FM120

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