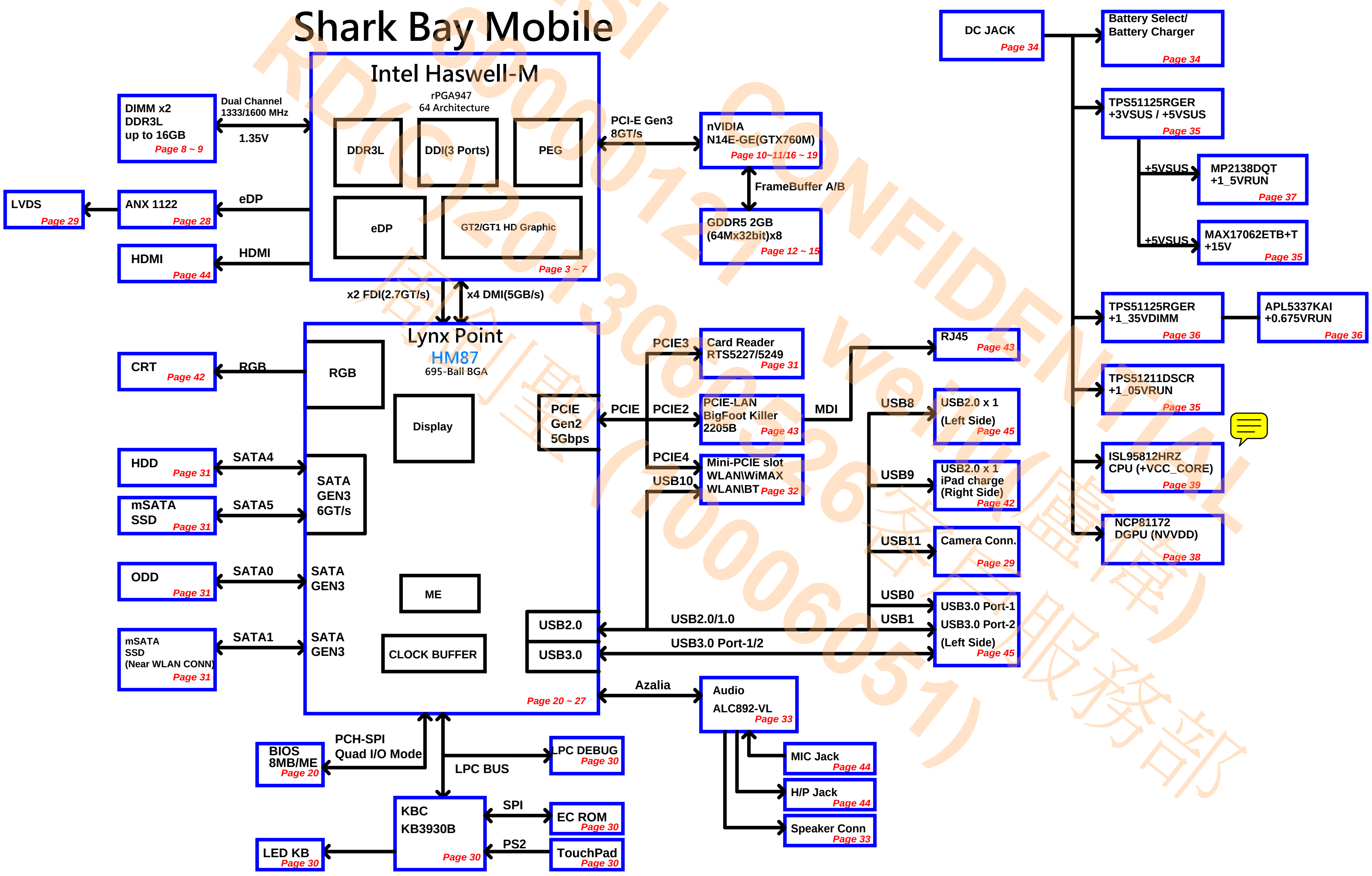
MS-16GC ver:0B



Title	Block Diagram
Size: Custom	Document Number: MS-16GC
Rev	0B
Date: Thursday, December 27, 2012	Sheet 1 of 50

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

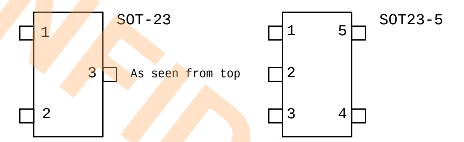
Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S4#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	PM_SLP_S3#
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	PM_SLP_S3#
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.2V Core Voltage for Processor	VR_ON
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVVDD	0.6~1.2V(VBoot:0.9V)Core Voltage for nVIDIA N14E-GE DGPU	GPIO11_GPUVID
+3V3_NV	3.3V GPU I/O power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	GPU_PWRGD
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	GPU_PWRGD

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

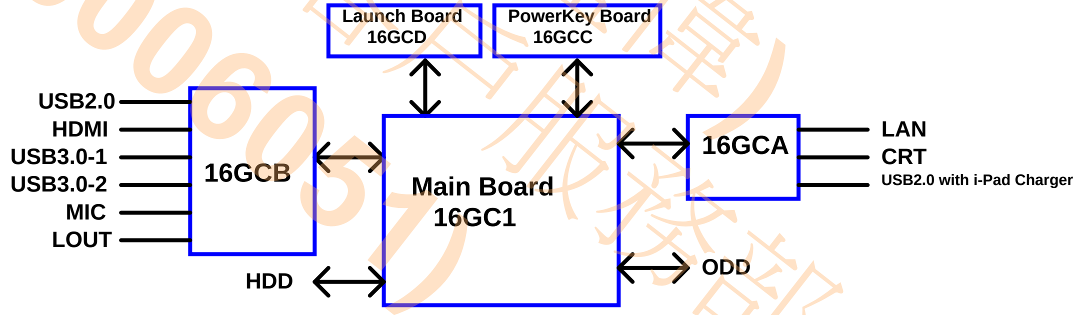
PCB Footprints



POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high



Title	Platform
Size	Custom
Document Number	MS-16GC
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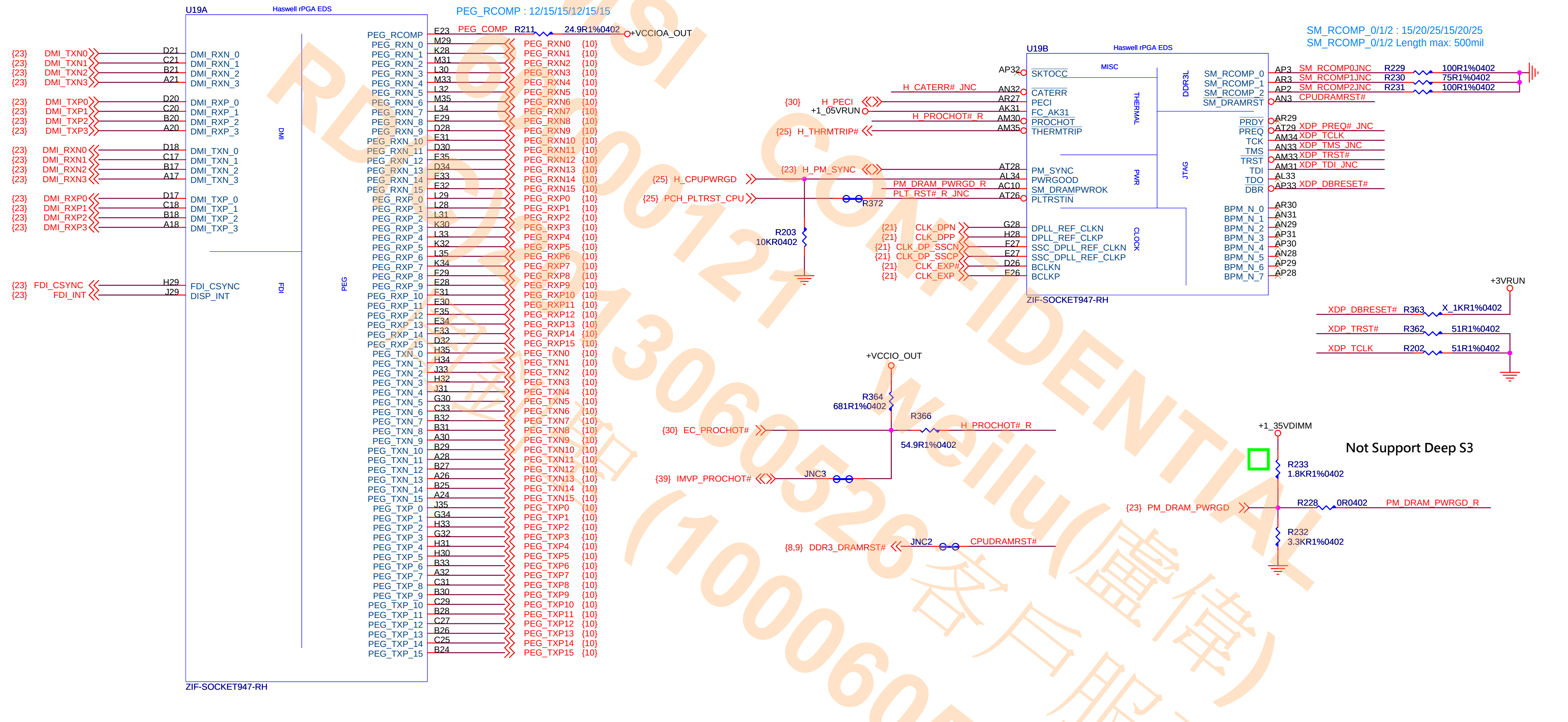
Date:	Thursday, December 27, 2012
Sheet	2 of 50

Haswell (DMI,PEG,FDI)

Haswell (CLK,MISC,JTAG)

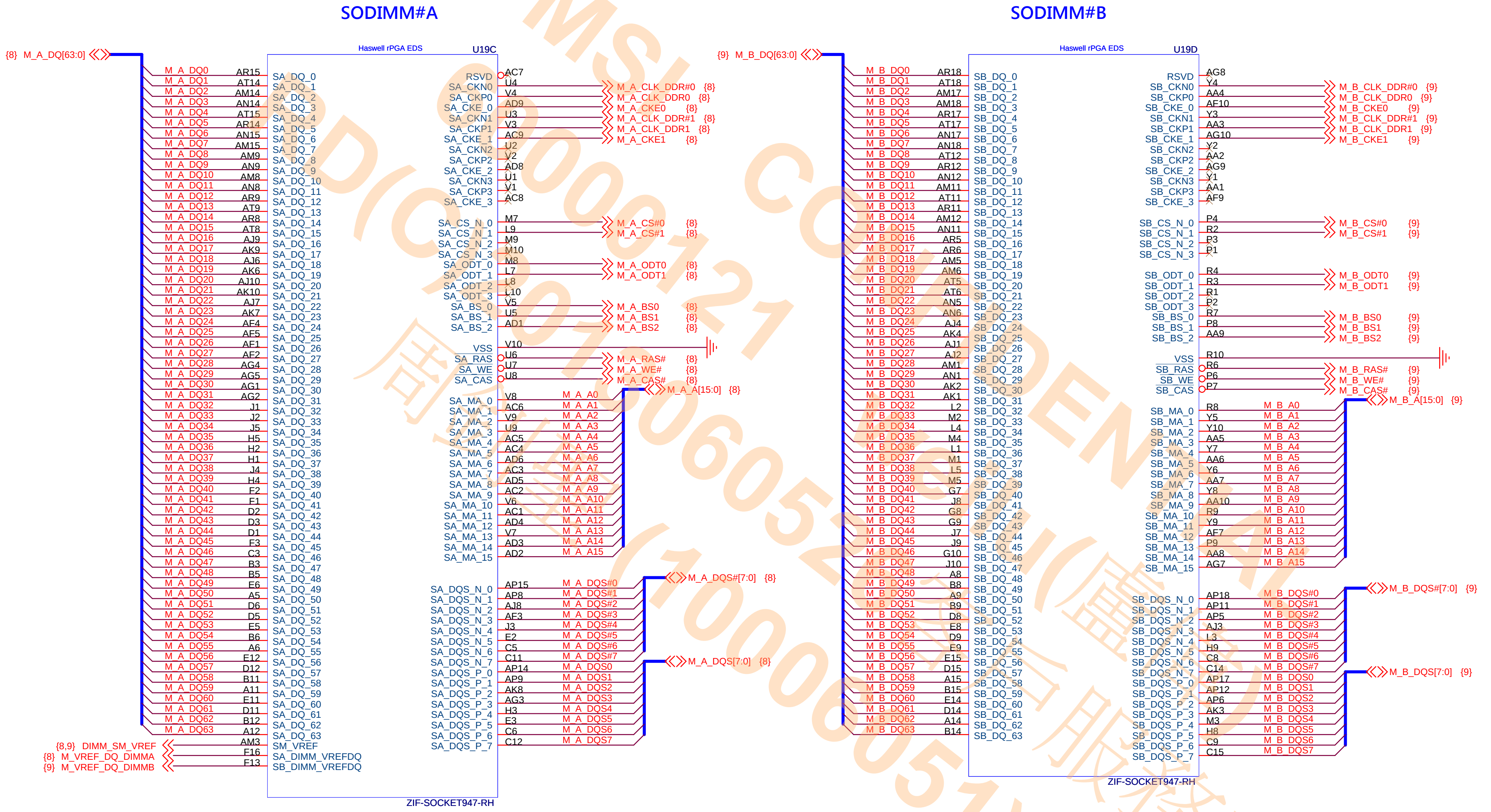


Title: CPU-1 (Host Bus)

Size: Custom | Document Number: MS-16GC | Rev: 0B

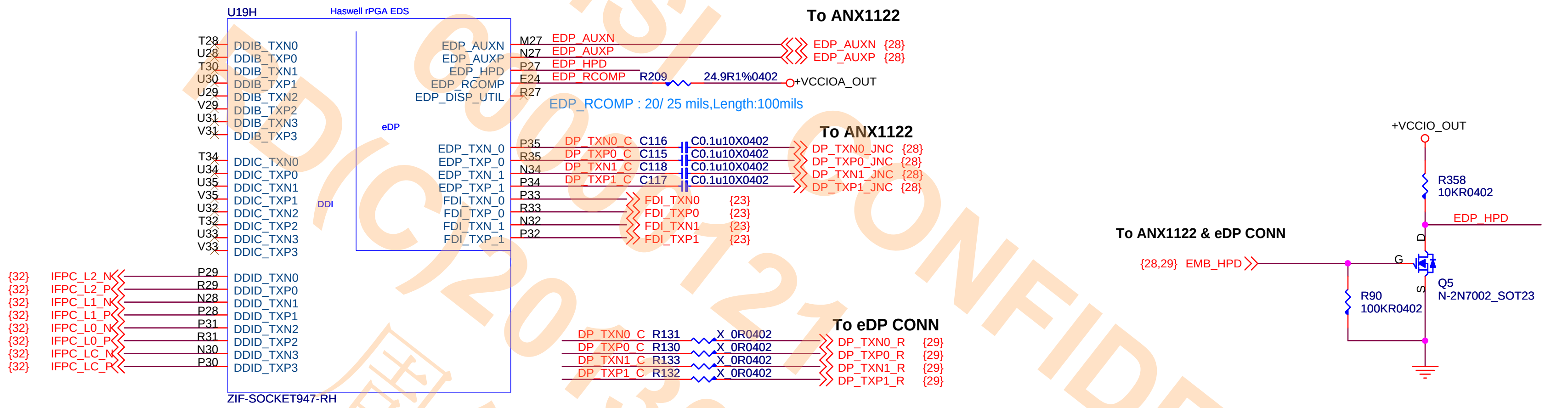
Date: Friday, December 28, 2012 | Sheet 3 of 50

Haswell (DDR3L)

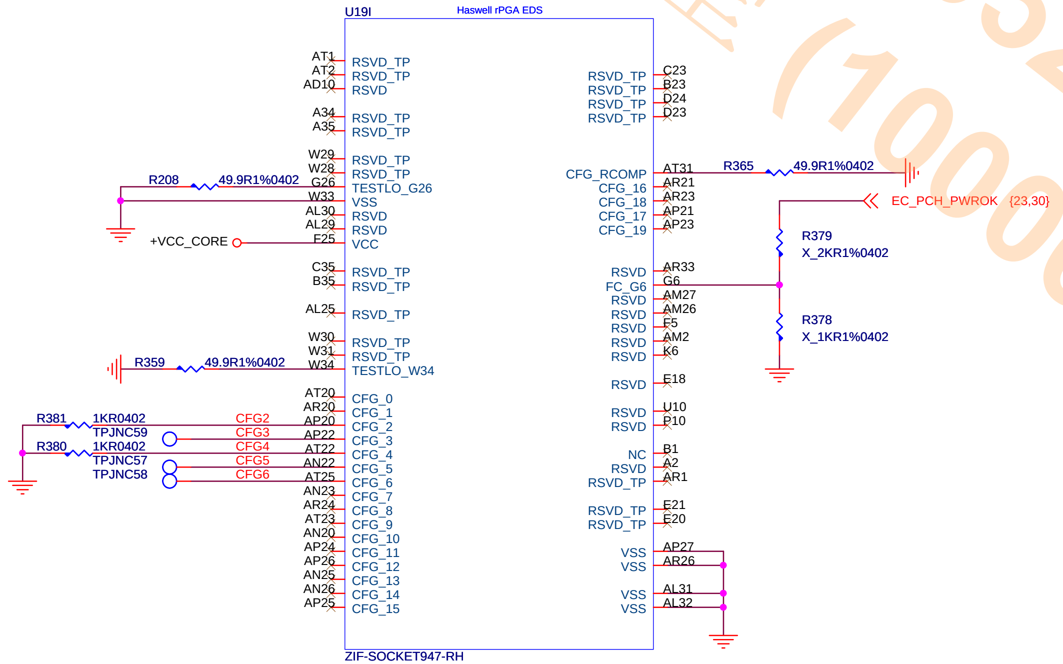


Title	CPU-2 (DDR3L)	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Thursday, December 27, 2012	Sheet 4 of 50	

Haswell (Display)



Haswell (Reserved)



PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

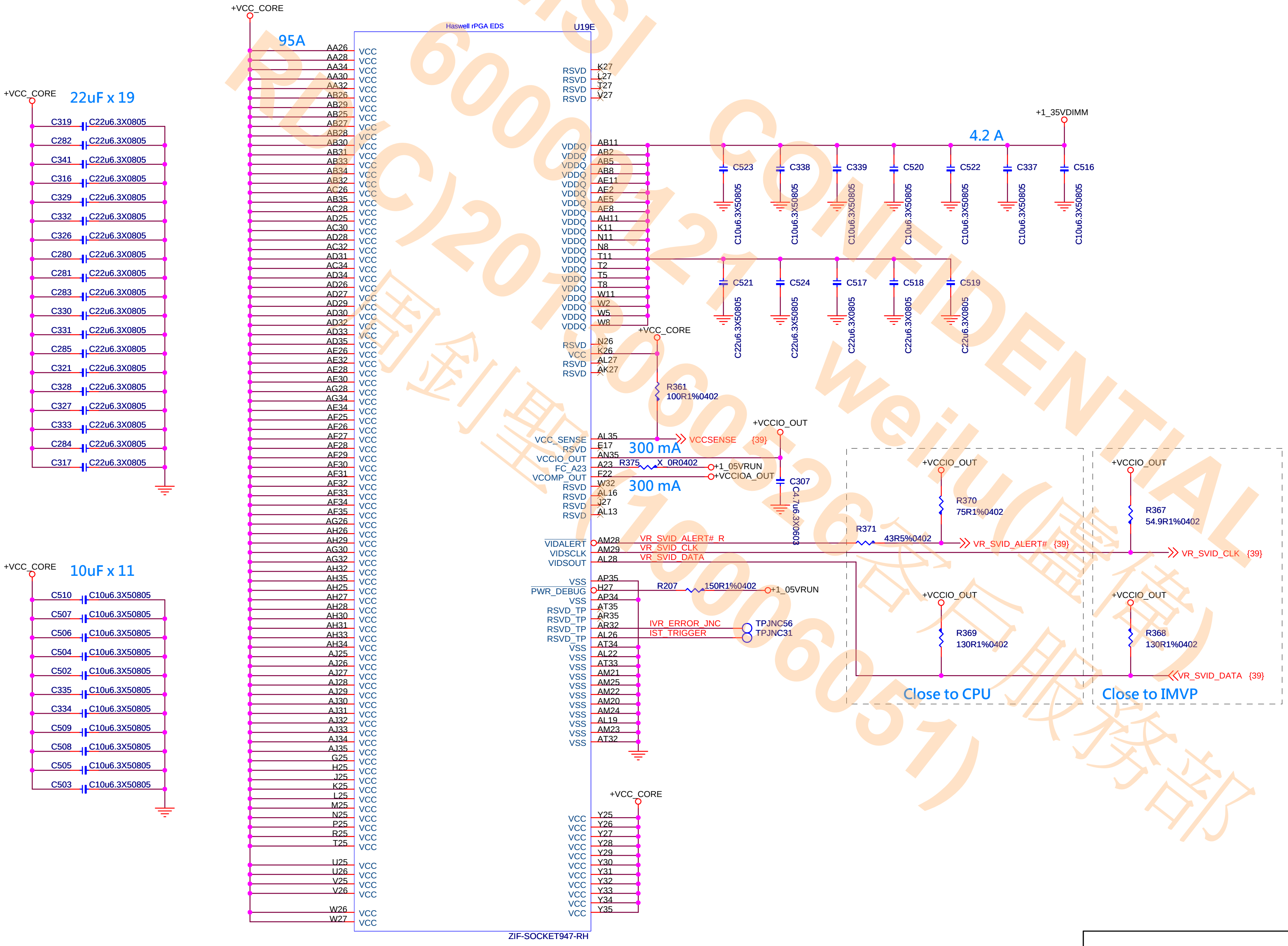
eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Title	CPU-3 (Display/Reserved)
Size: Custom	Document Number: MS-16GC
Rev	0B
Date:	Friday, December 28, 2012
Sheet	5 of 50

Haswell (POWER)

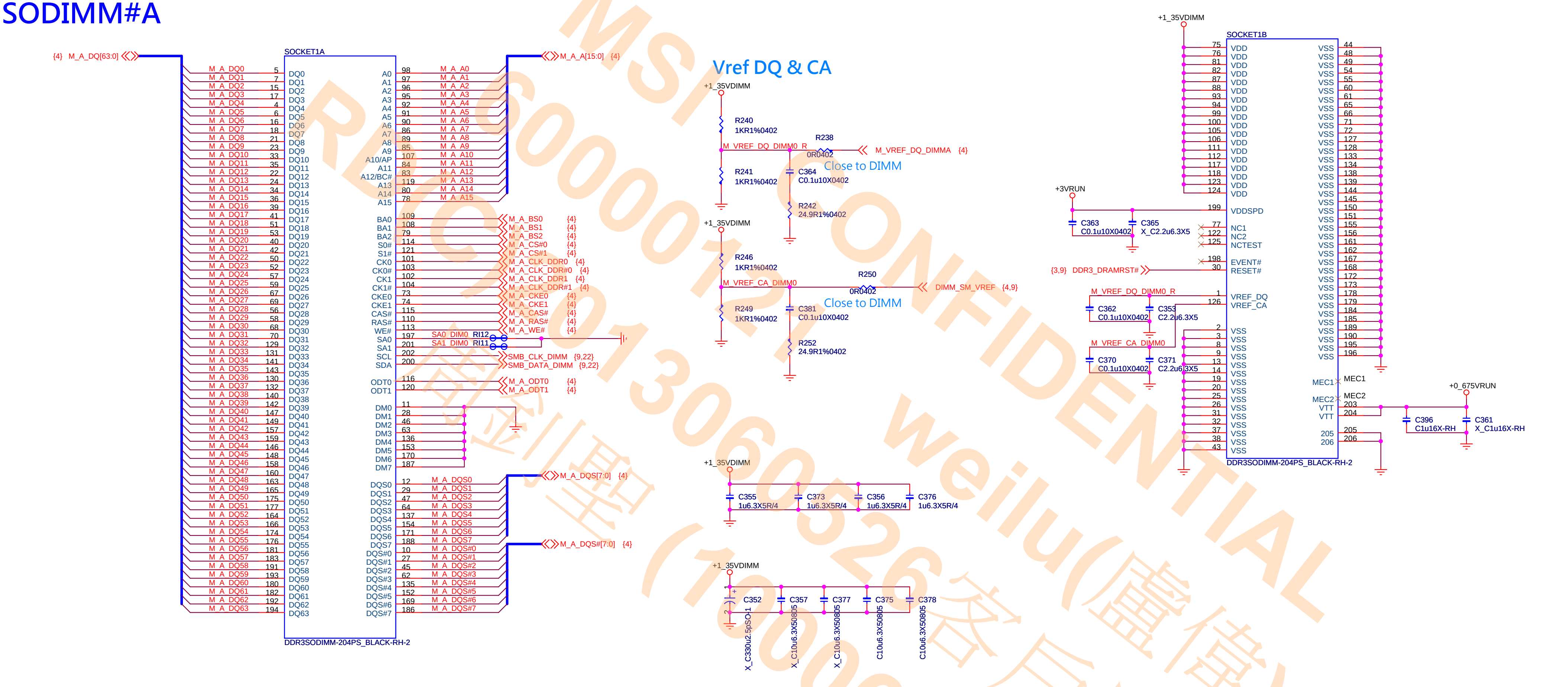


Title	CPU-4 (Power)	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Friday, December 28, 2012	Sheet 6 of 50	

Haswell (GND)

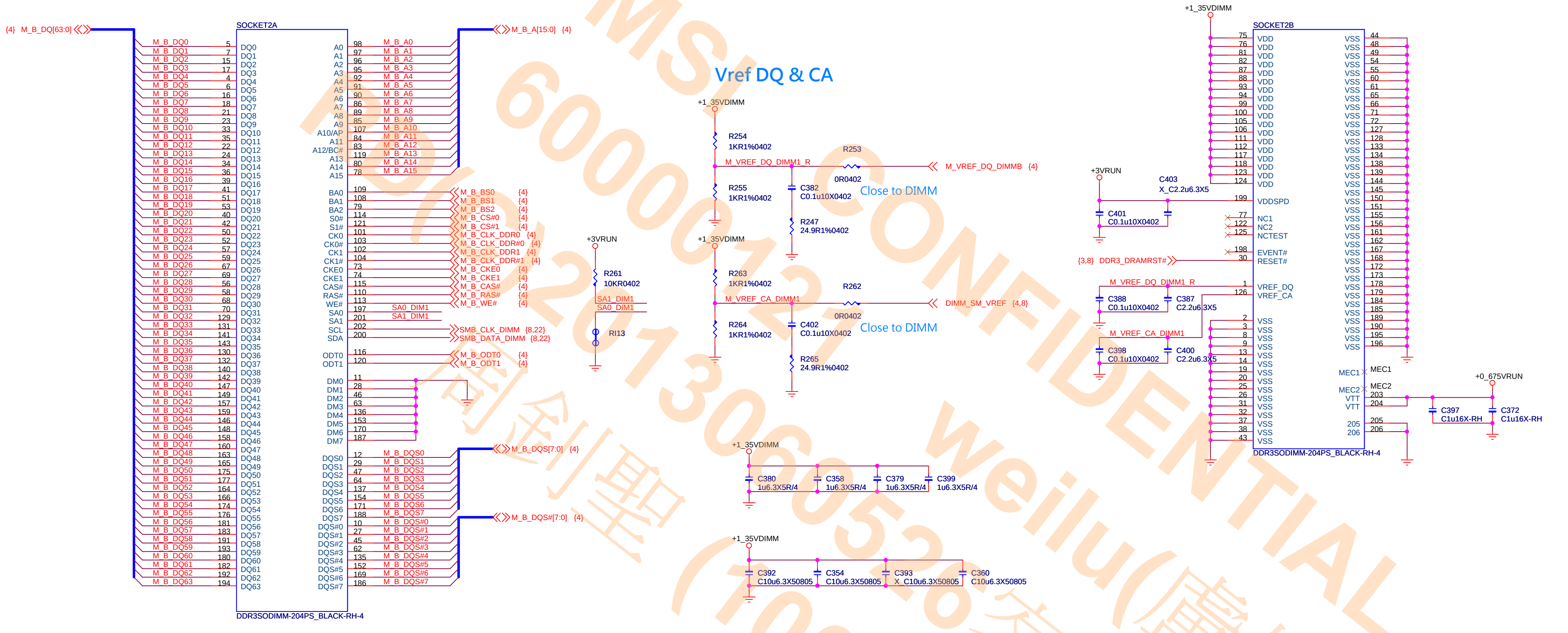
Title
CPU-5 (GND)
Size Custom | Document Number MS-16GC | Rev 0B
Date: Thursday, December 27, 2012 | Sheet 7 of 50

SODIMM#A



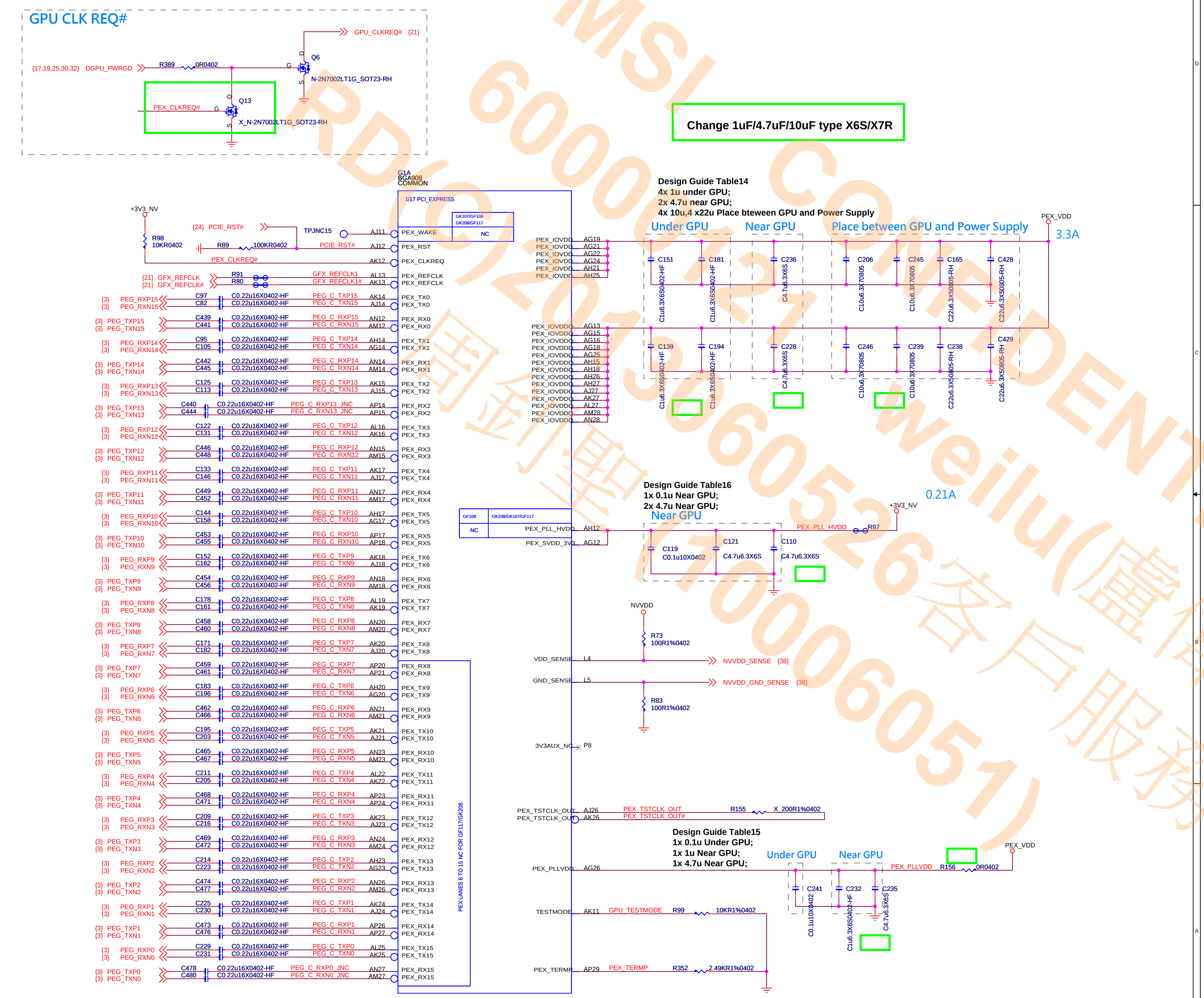
Title	DDR3L SODIMM 0	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Thursday, December 27, 2012	Sheet 8 of 50	

SODIMM#B



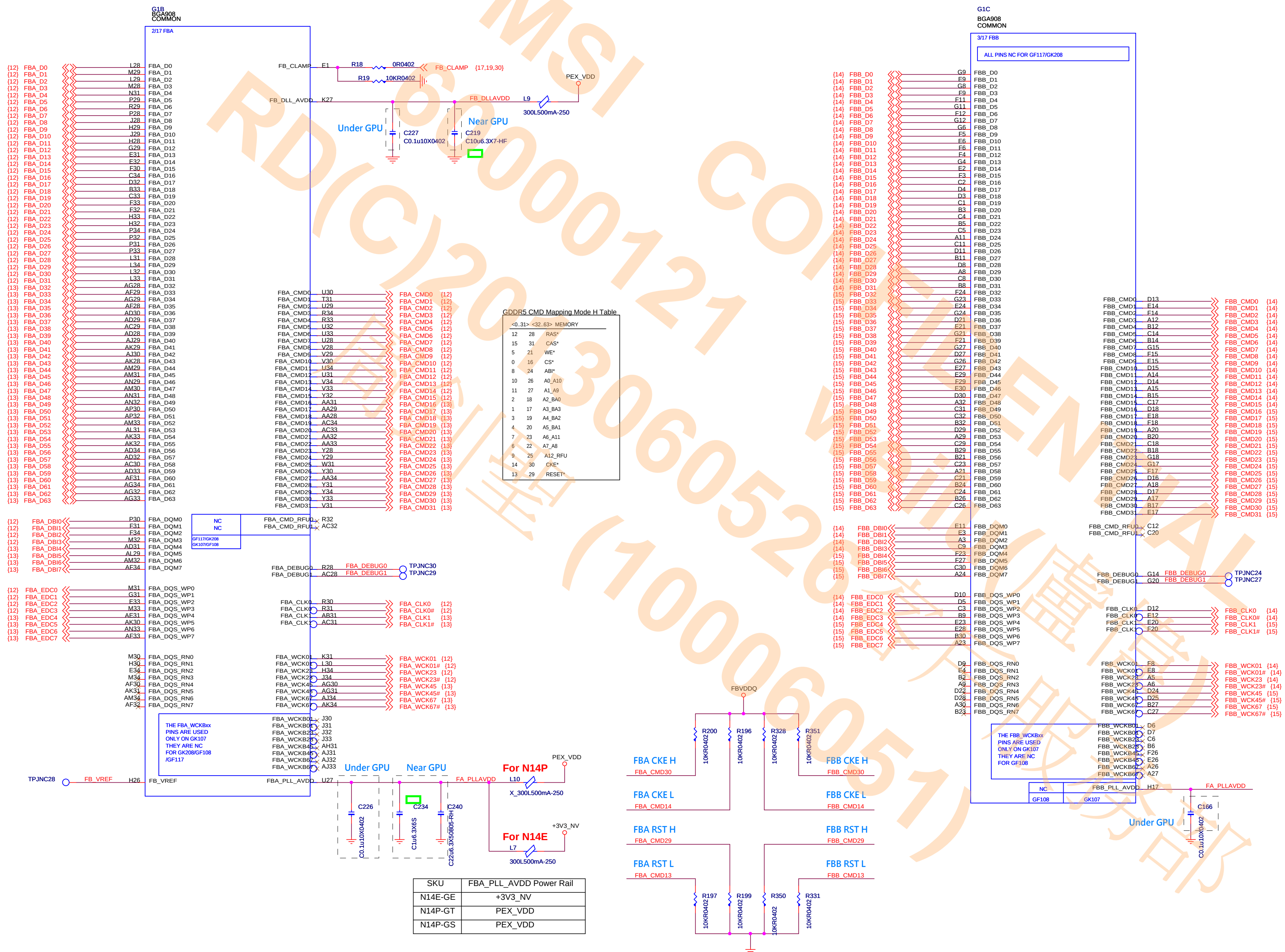
Title	DDR3L SODIMM 1		
Size: Custom	Document Number: MS-16GC		Rev: 0B
Date: Thursday, December 27, 2012	Sheet 9 of 50		

N14E-GE(PCI-Express Gen3 x16 Interface)



Title	N14E-GE_PCI-E Host	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Friday, December 28, 2012	Sheet 10 of 50	

N14E-GE(Frame Buffer Interface)



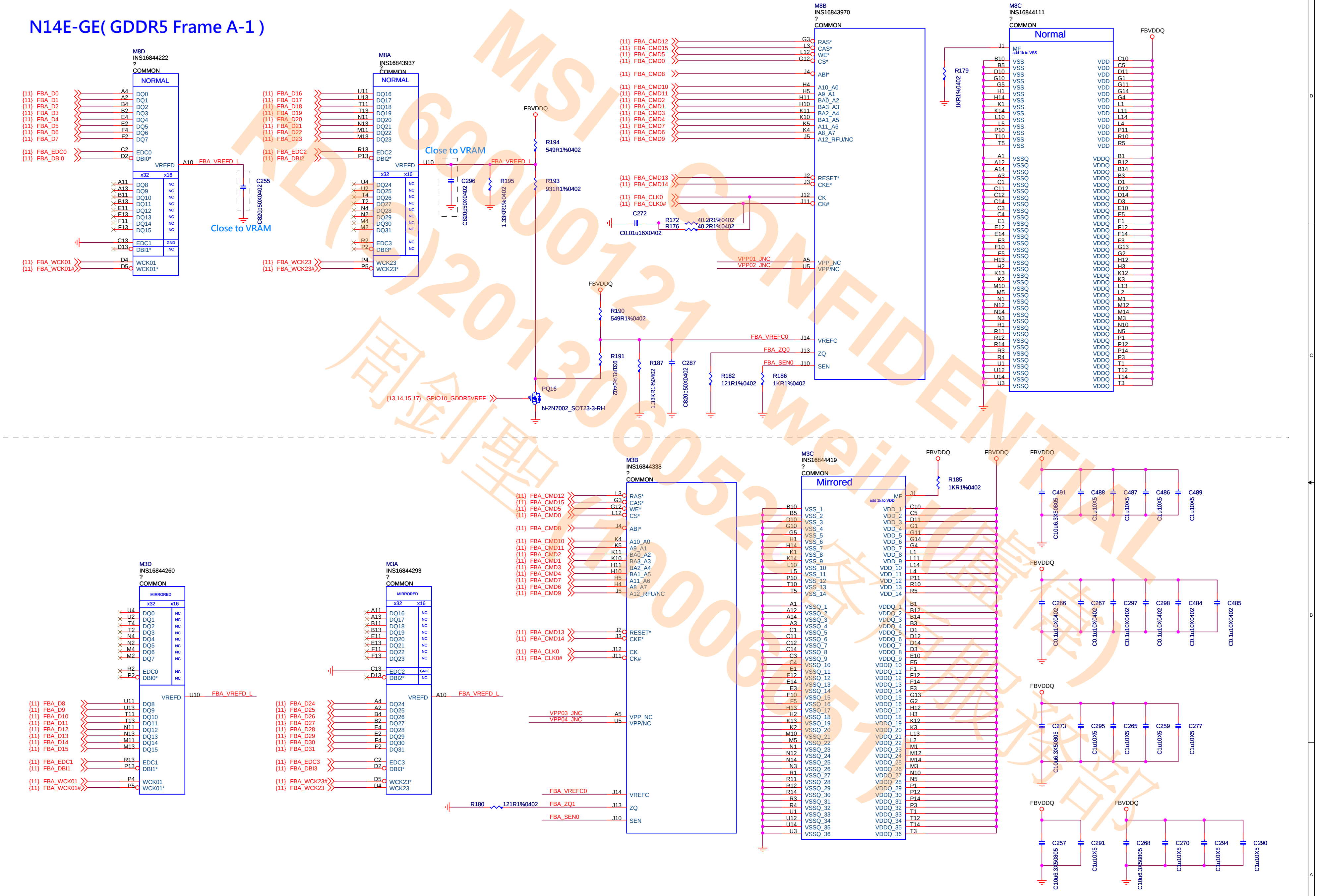
GDDR5 CMD Mapping Mode H Table

<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE*
13	29	RESET*

SKU	FBA_PLL_AVDD Power Rail
N14E-GE	+3V3_NV
N14P-GT	PEX_VDD
N14P-GS	PEX_VDD

Title	N14E-GE_MEM IF A/B	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Thursday, December 27, 2012	Sheet 11 of 50	

N14E-GE(GDDR5 Frame A-1)

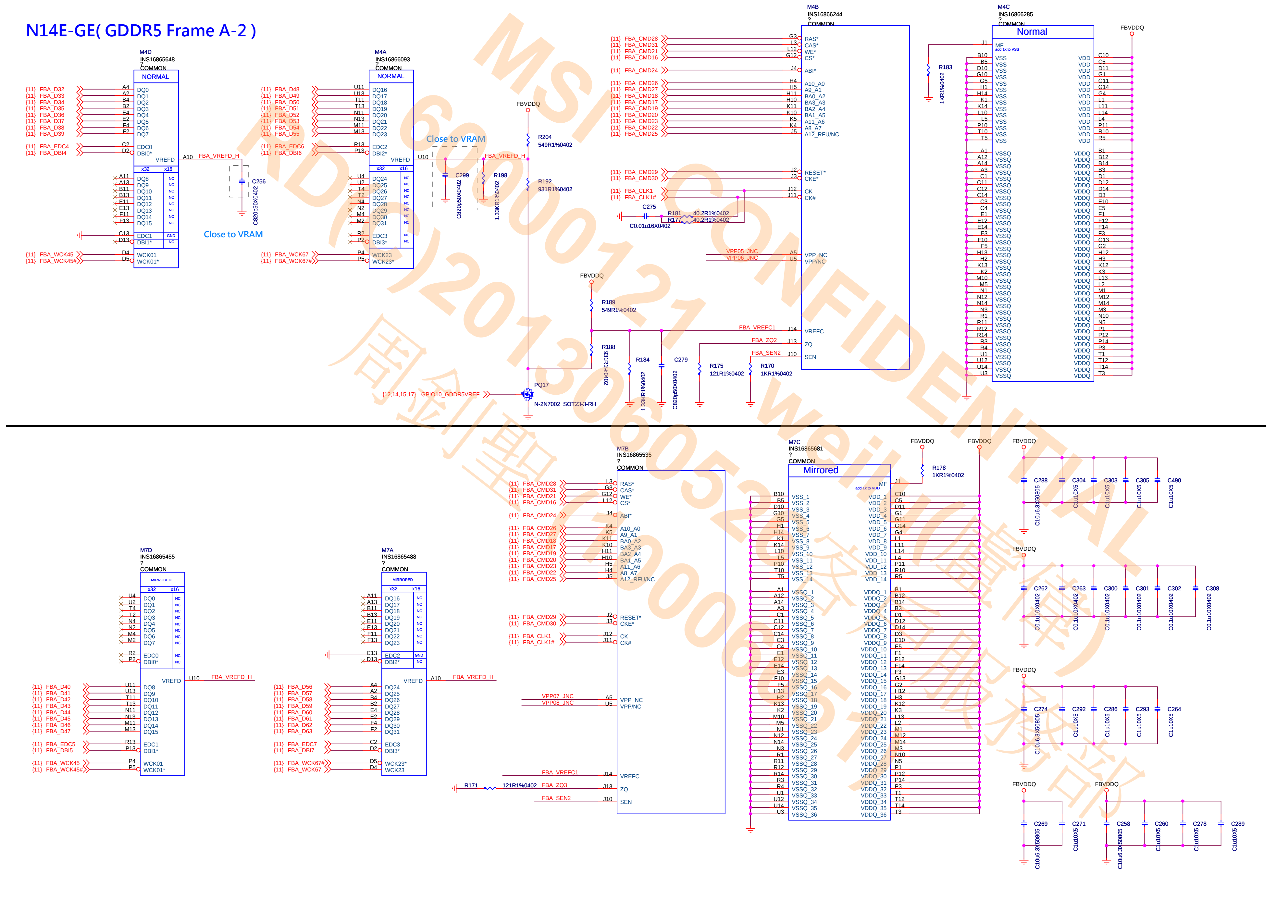


Title: N14E-GE_GDDR5 Frame A-1

Size: Custom | Document Number: MS-16GC | Rev: 0B

Date: Friday, December 28, 2012 | Sheet 12 of 50

N14E-GE(GDDR5 Frame A-2)



Title	N14E-GE_GDDR5 Frame A-2
Size: Custom	Document Number: MS-16GC
Rev	0B
Date:	Friday, December 28, 2012
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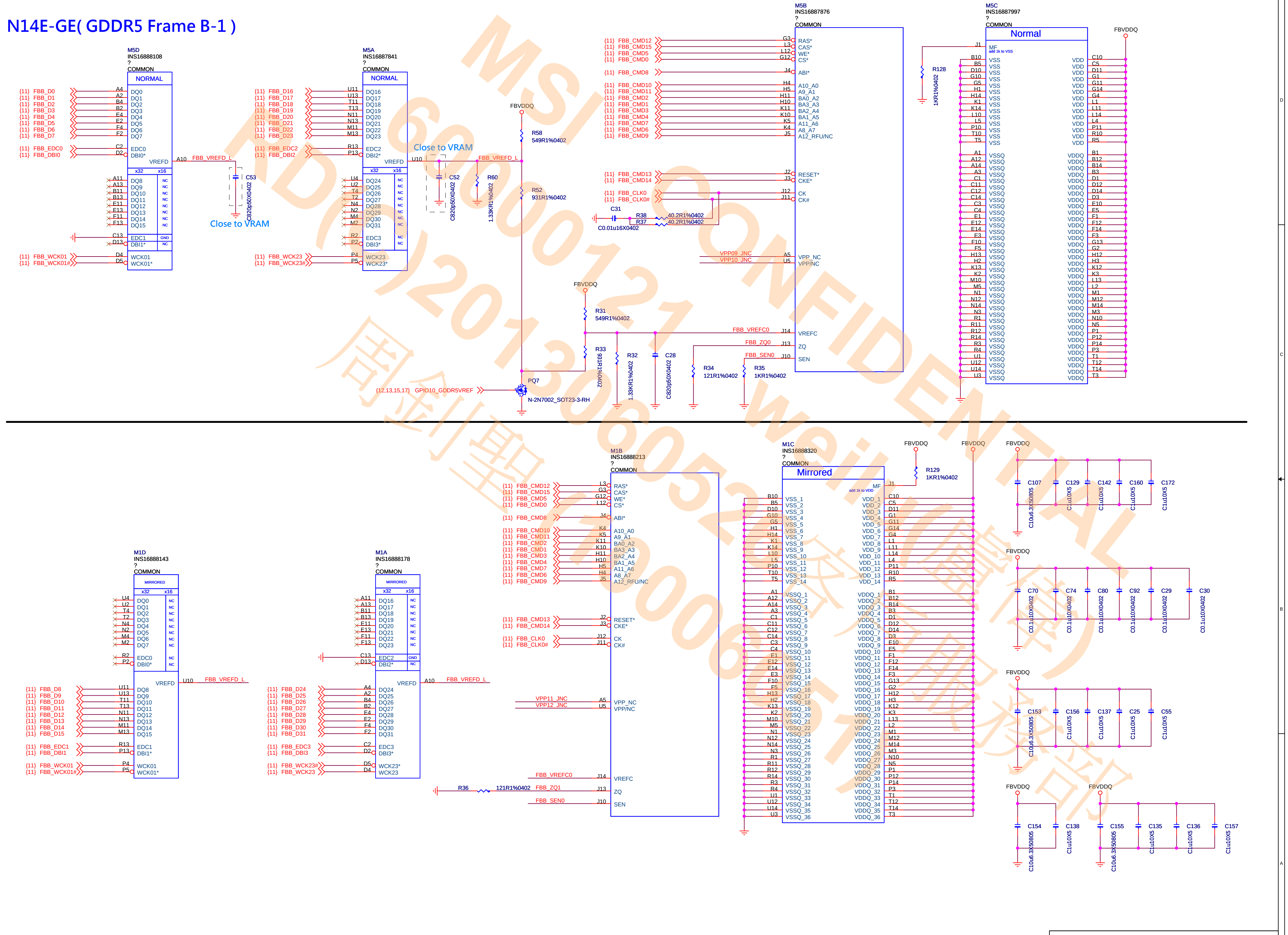
N14E-GE(GDDR5 Frame B-1)

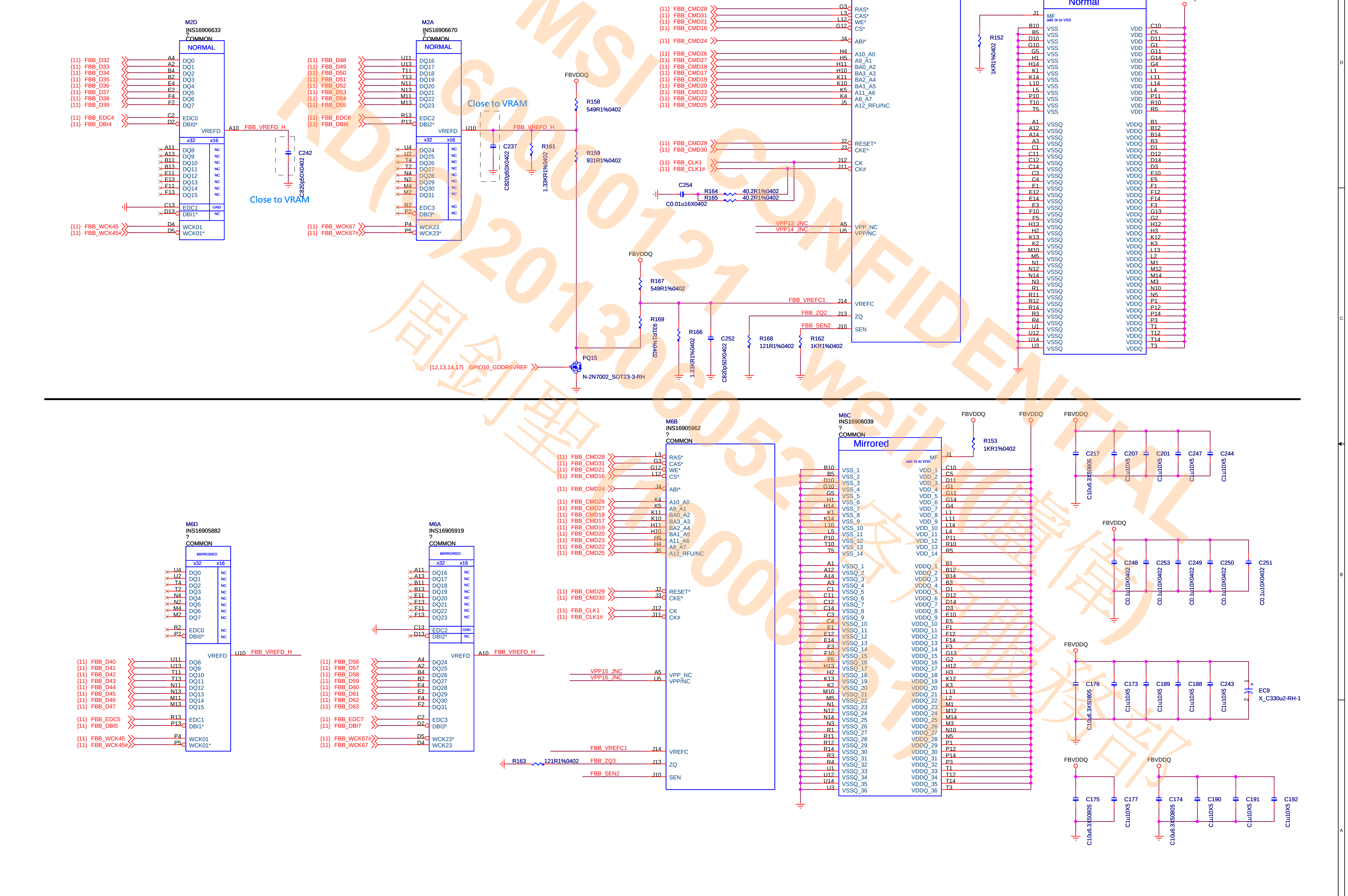


Title: N14E-GE_GDDR5 Frame B-1

Size: Custom | Document Number: MS-16GC | Rev: 0B

Date: Friday, December 28, 2012 | Sheet 14 of 50

N14E-GE(GDDR5 Frame B-2)

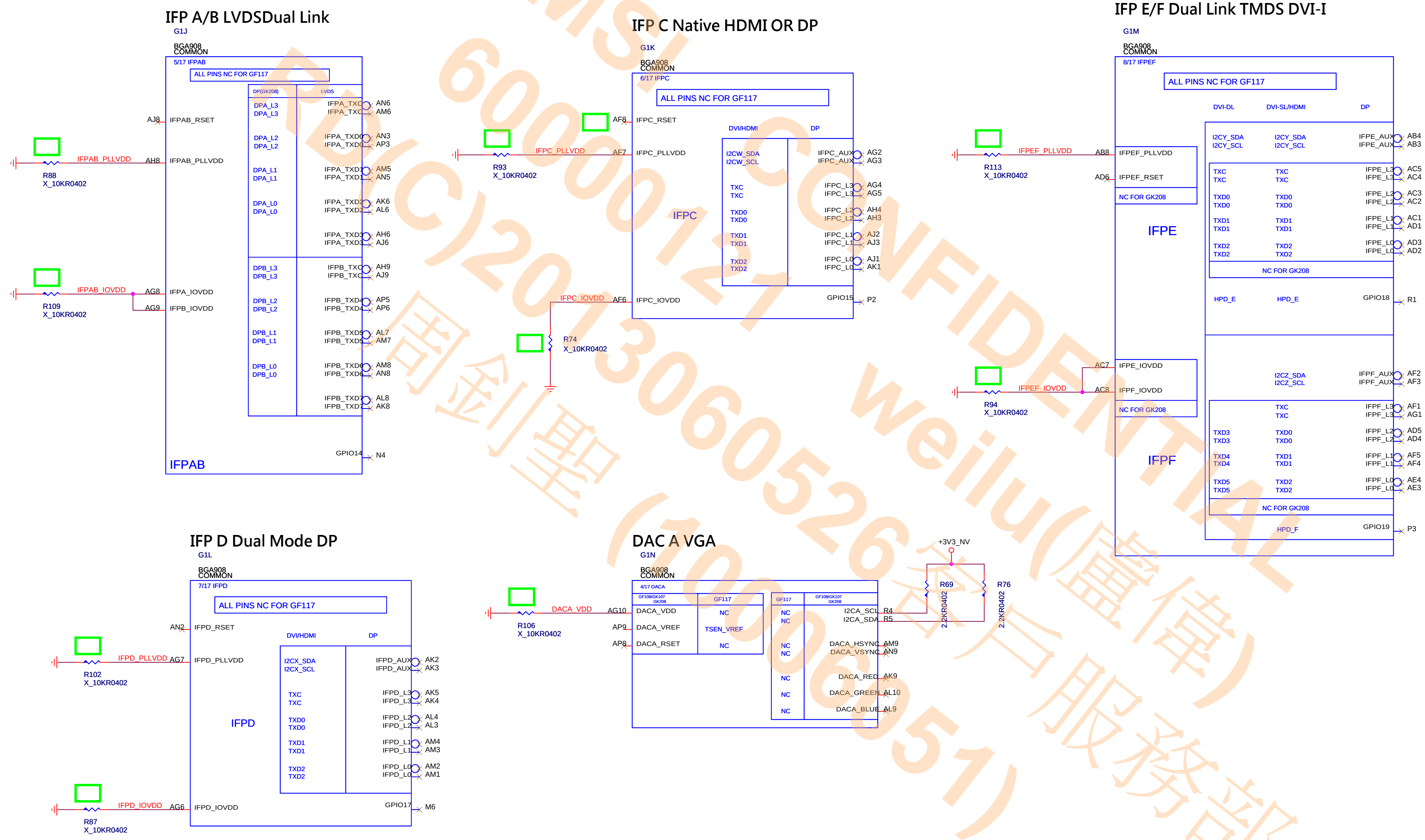


Title: N14E-GE_GDDR5 Frame B-2

Size: Custom | Document Number: MS-16GC | Rev: 0B

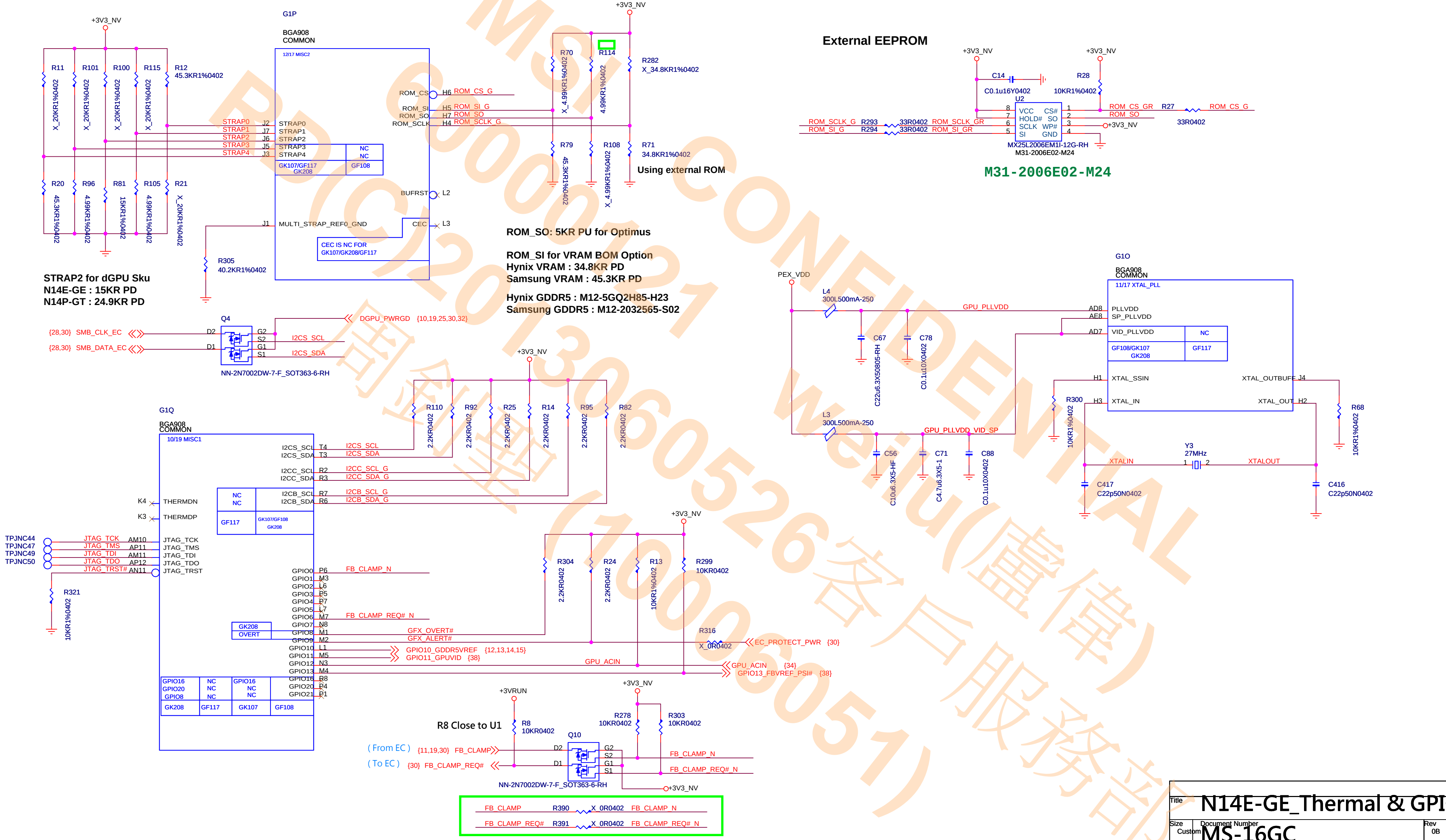
Date: Friday, December 28, 2012 | Sheet 15 of 50

N14E-GE(Display IF)



Title	N14E-GE_Display IF		
Size Custom	Document Number MS-16GC		Rev 0B
Date: Friday, December 28, 2012	Sheet 16	of 50	

N14E-GE(Thermal & GPIO)



Title	N14E-GE_Thermal & GPIO
Size: Custom	Document Number: MS-16GC
Rev	0B
Date:	Friday, December 28, 2012
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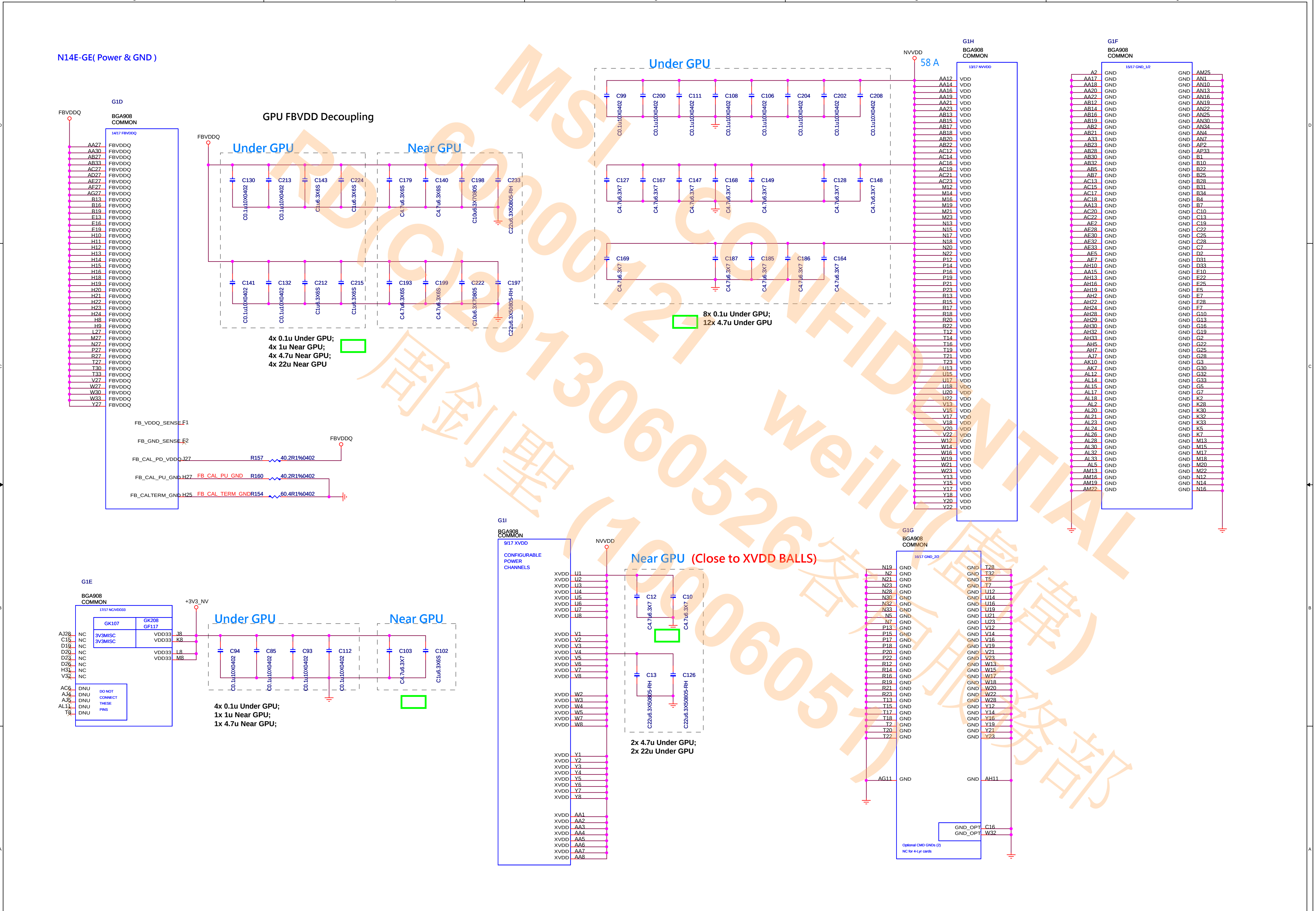
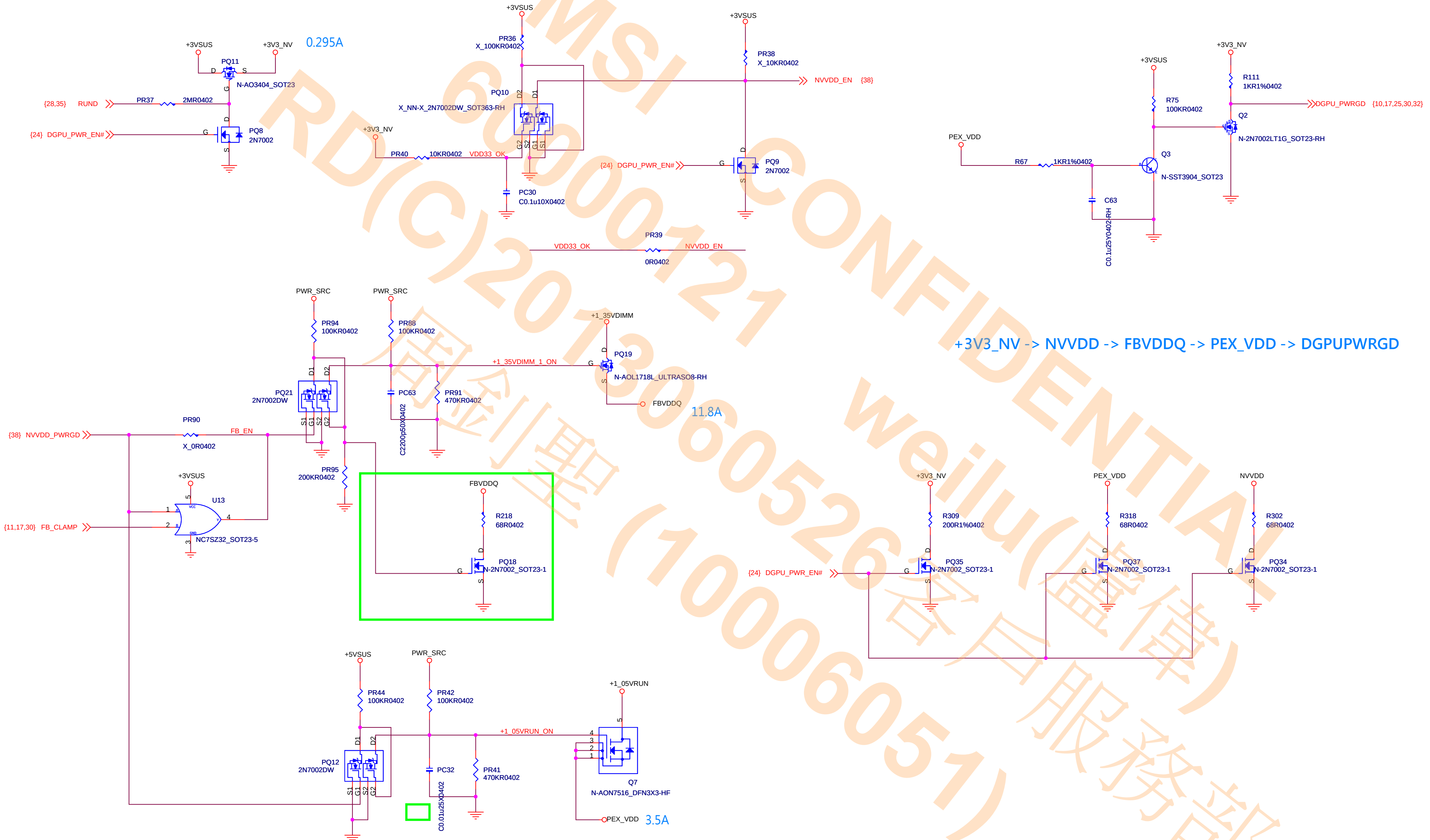


Title	N14E-GE_Power & GND
Size	Custom
Document Number	MS-16GC
Rev	0B
Date:	Friday, December 28, 2012
Sheet	18 of 50

N14E-GE(Power Control)

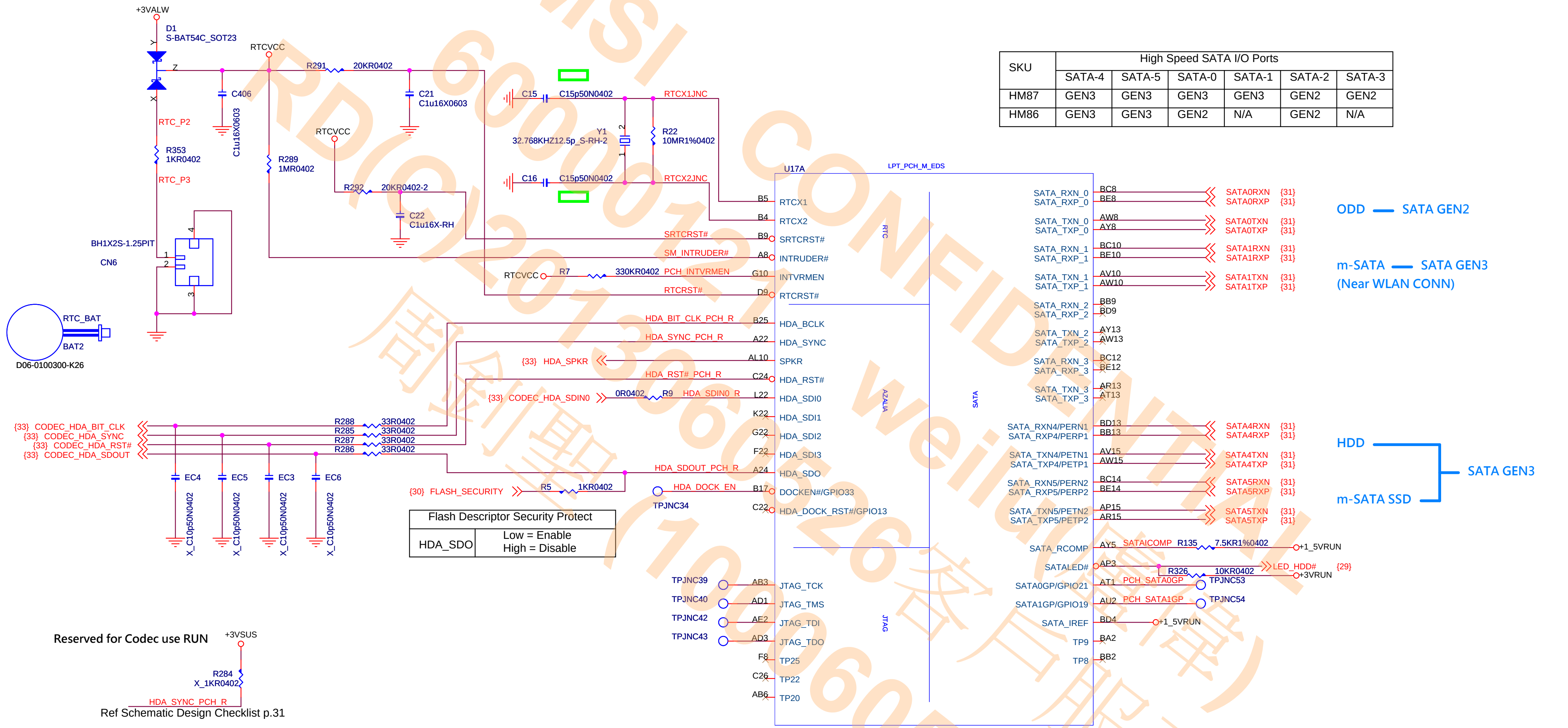


Title: N14E-GE_Power Control

Size: Custom | Document Number: MS-16GC | Rev: 0B

Date: Friday, December 28, 2012 | Sheet 19 of 50

Lynx Point (HDA,JTAG,SATA)



SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

Reserved for Codec use RUN

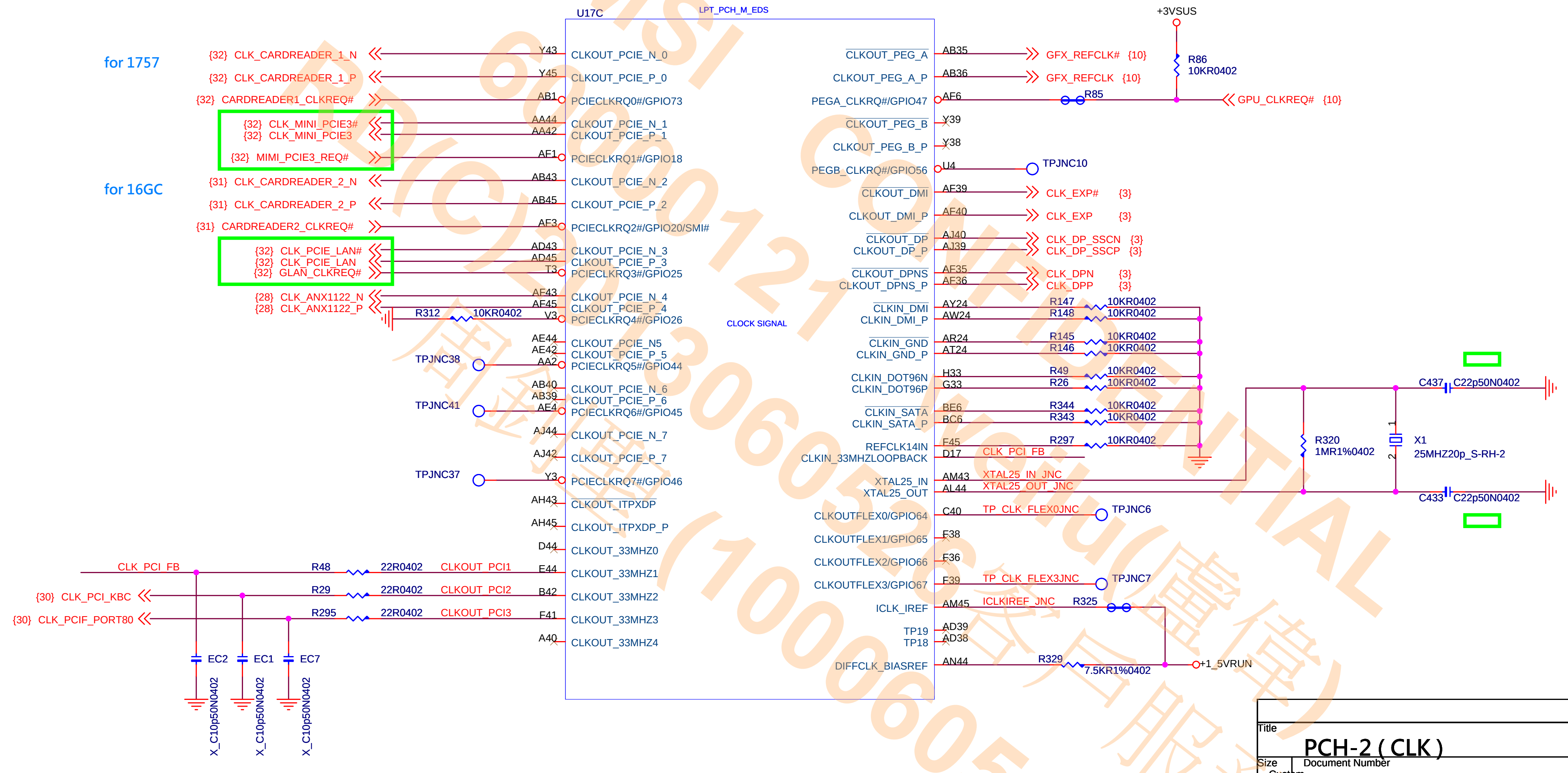
Ref Schematic Design Checklist p.31

Title: PCH-1 (HDA/JTAG/SATA)

Size: Custom | Document Number: MS-16GC | Rev: 0B

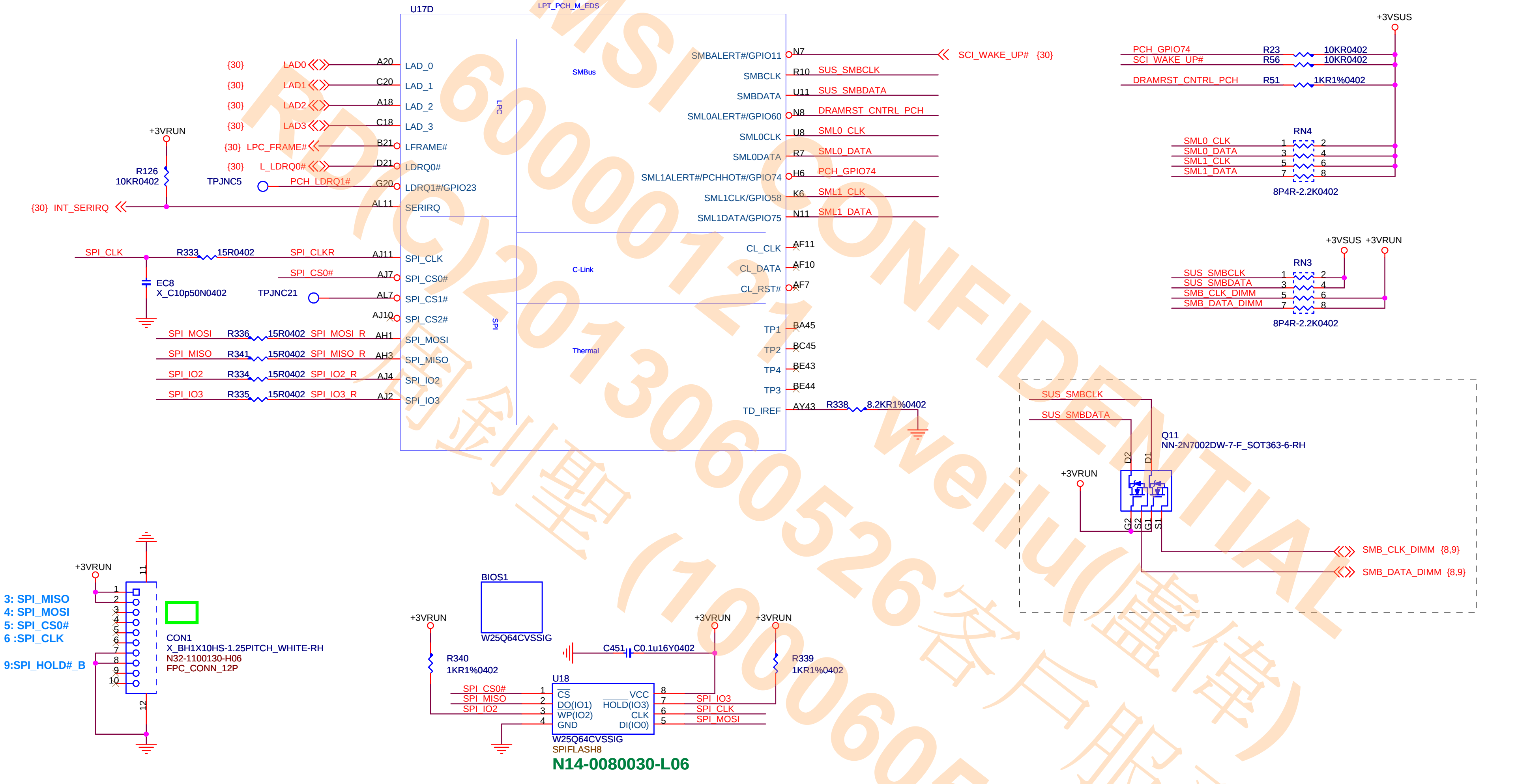
Date: Thursday, December 27, 2012 | Sheet 20 of 50

Lynx Point (Clock)



Title	PCH-2 (CLK)	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Thursday, December 27, 2012	Sheet 21 of 50	

Lynx Point (LPC,SMBUS)

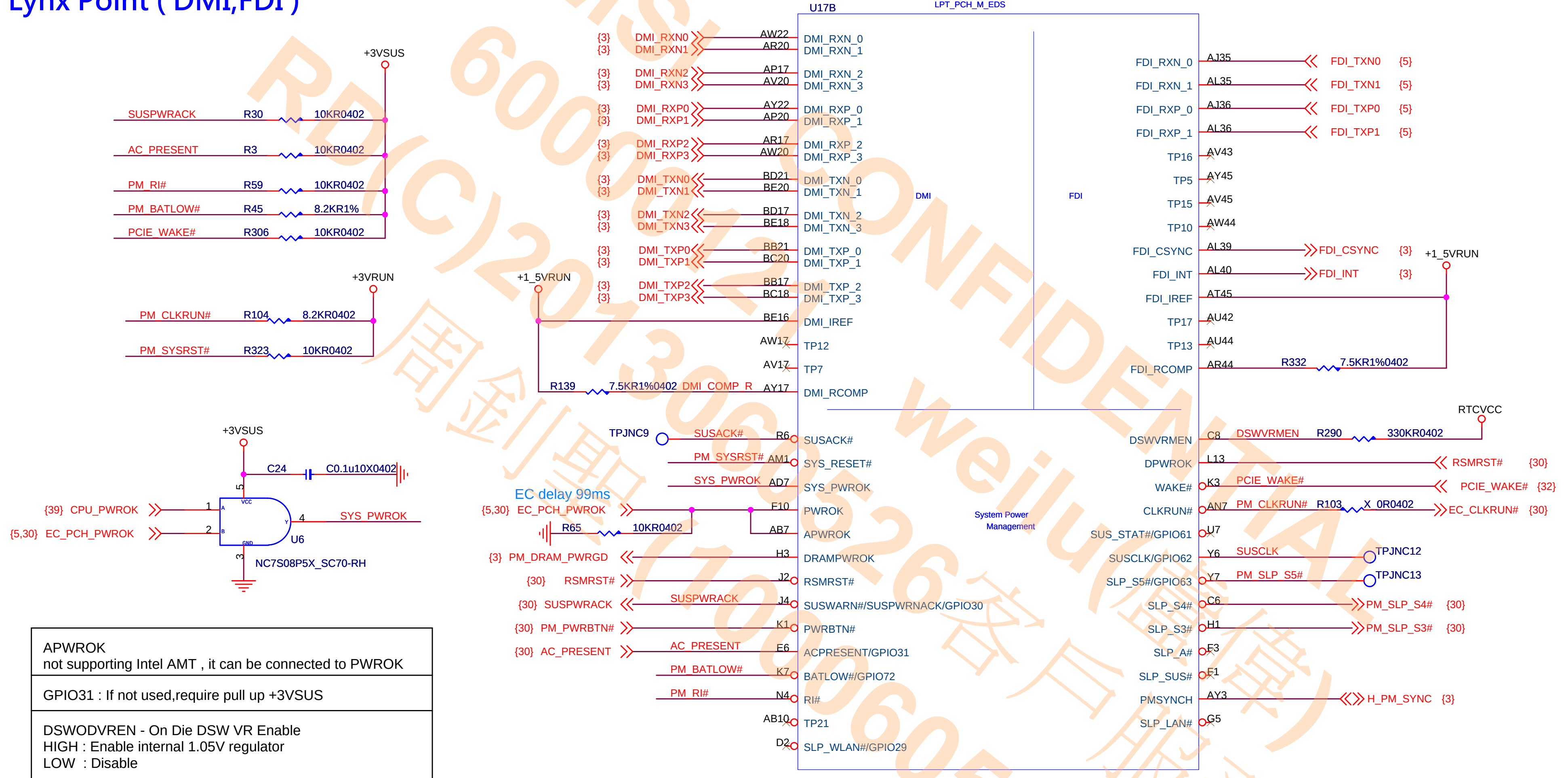


Title: PCH-3 (LPC,SMBUS)

Size: Custom | Document Number: MS-16GC | Rev: 0B

Date: Thursday, December 27, 2012 | Sheet 22 of 50

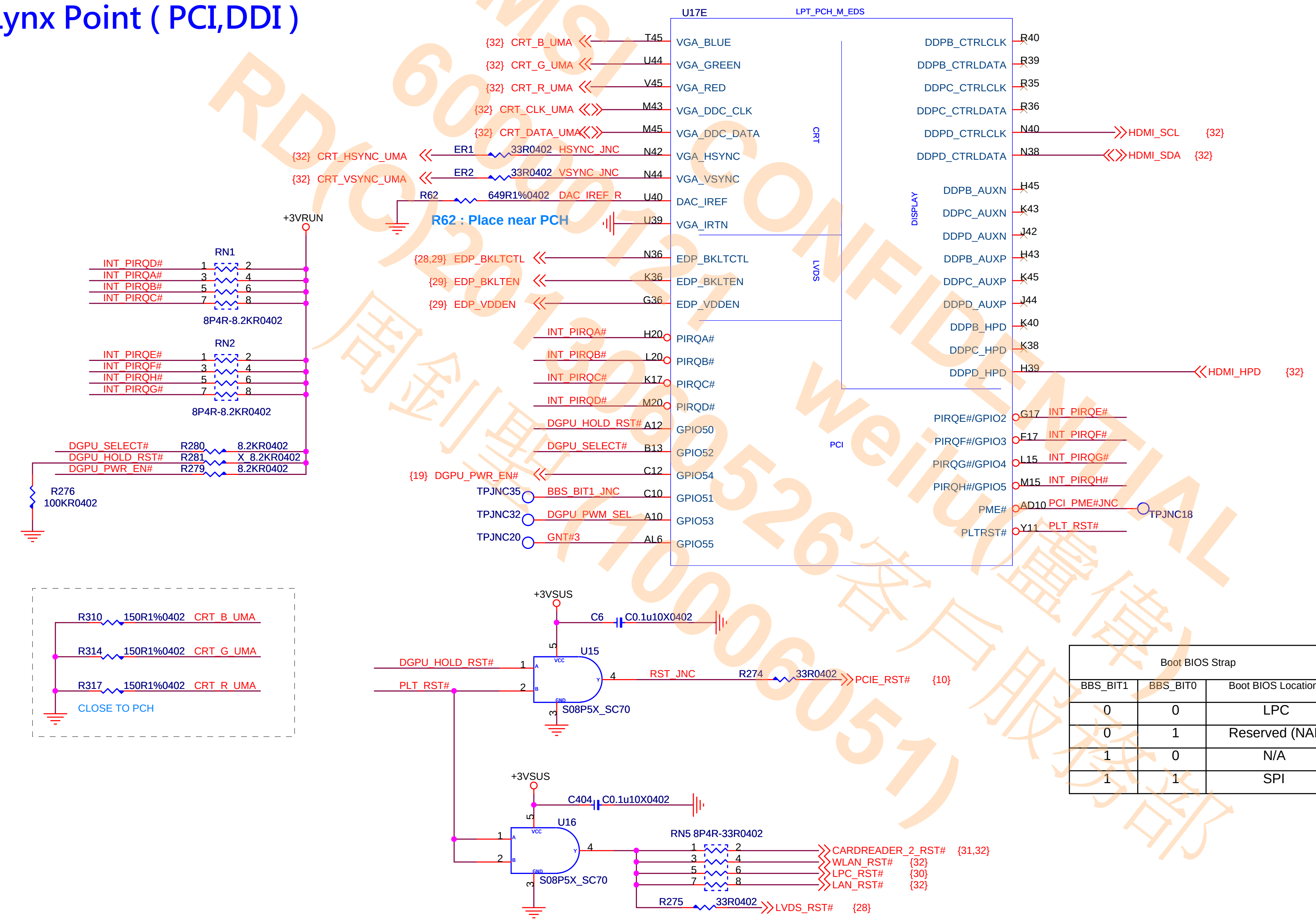
Lynx Point (DMI,FDI)



APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWODVREN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

Title	PCH-4 (DMI,FDI)		
Size Custom	Document Number MS-16GC		Rev 0B
Date: Thursday, December 27, 2012	Sheet 23 of 50		

Lynx Point (PCI,DDI)



Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

Title: PCH-5 (PCI,DDI)

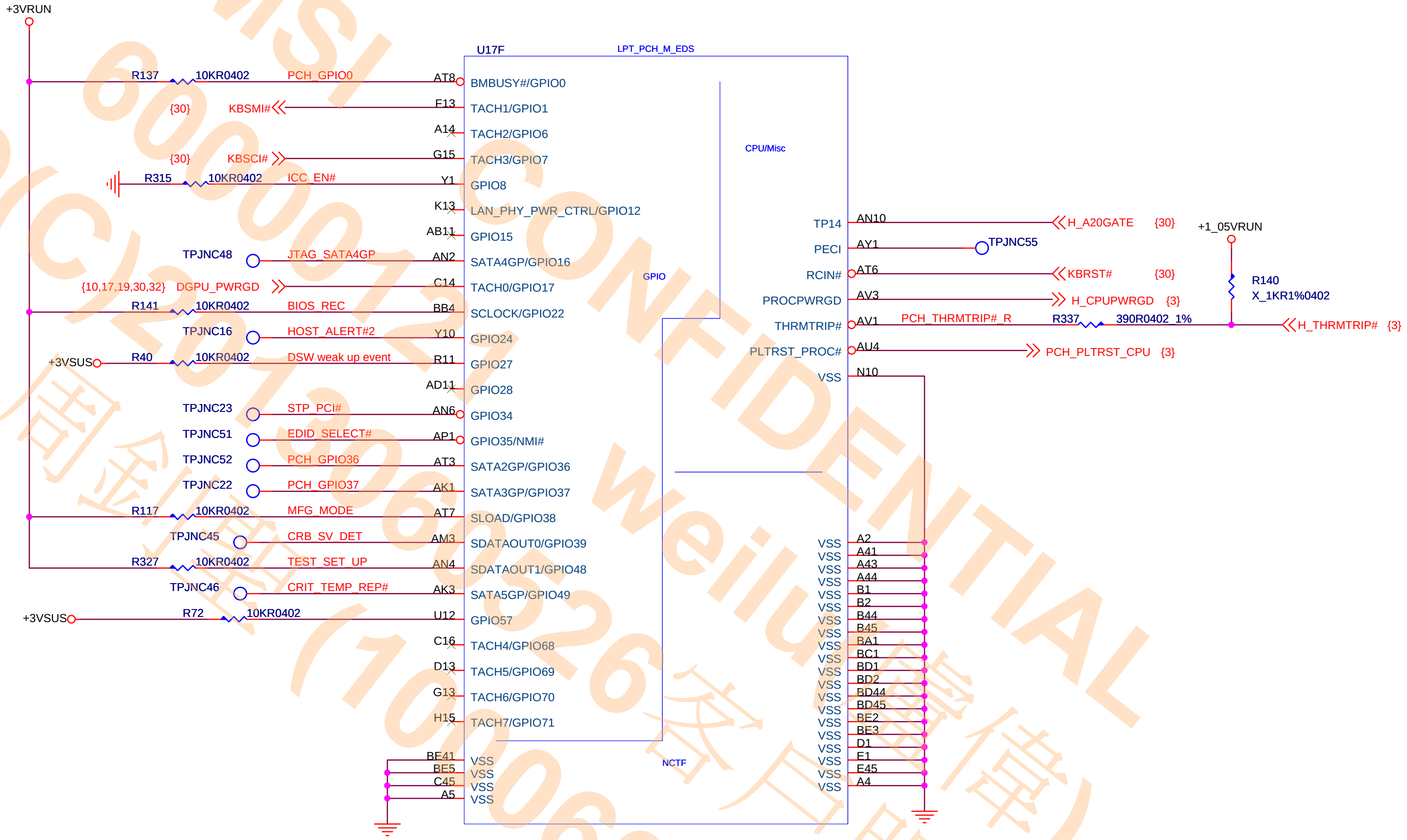
Size: Custom | Document Number: MS-16GC | Rev: 0B

Date: Thursday, December 27, 2012 | Sheet 24 of 50

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



Title	PCH-6 (GPIO,MISC)	
Size: Custom	Document Number: MS-16GC	Rev: 0B
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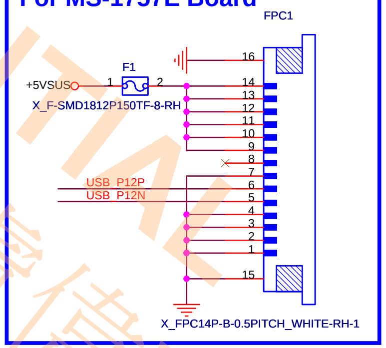
Lynx Point (PCIE,USB)

USB			
USB 2.0	**USB 3.0**	**Device**	**Note**
0	1	USB 3.0 Port 1	(16GCB/1757B)
1	2	USB 3.0 Port 2	(16GCB/1757B)
2			NC
3			NC
4			NC
5			NC
6			NC
7			NC
8		USB 2.0 Port	(16GCB)
9		USB 2.0 Port	(16GCA/1757A)
10		WLAN	
11		WebCam	
12		USB 2.0 Port	(1757E)
13			NC
	3		NC
	4		NC
	5		NC
	6		NC

For MS-1757E Board



Title: PCH-7 (PCIE,USB)
Size: Custom
Document Number: MS-16GC
Rev: 0B
Date: Thursday, December 27, 2012
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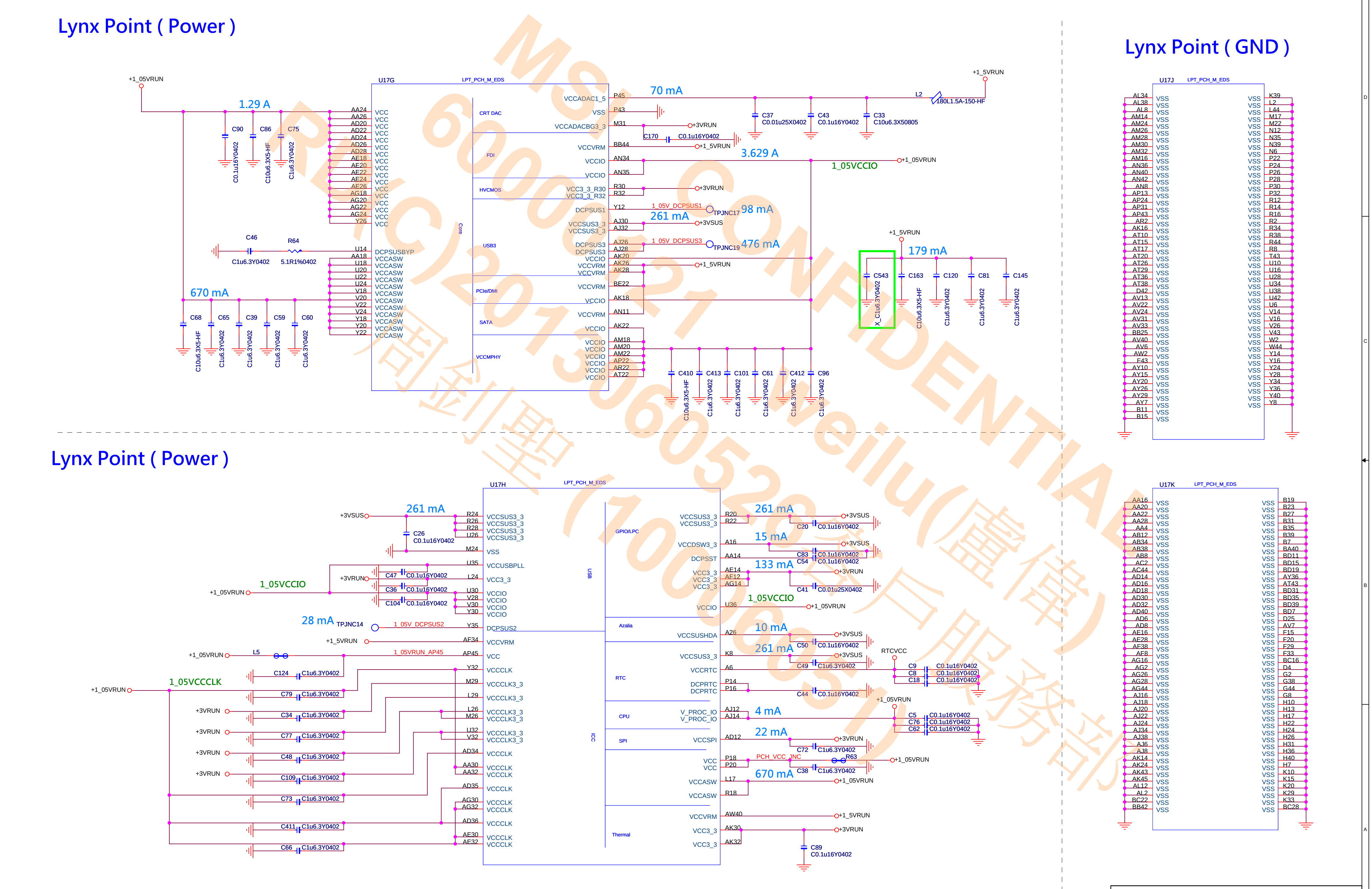

Title: PCH-8 (Power,GND)

Size	Document Number	Rev
Custom	MS-16GC	0B

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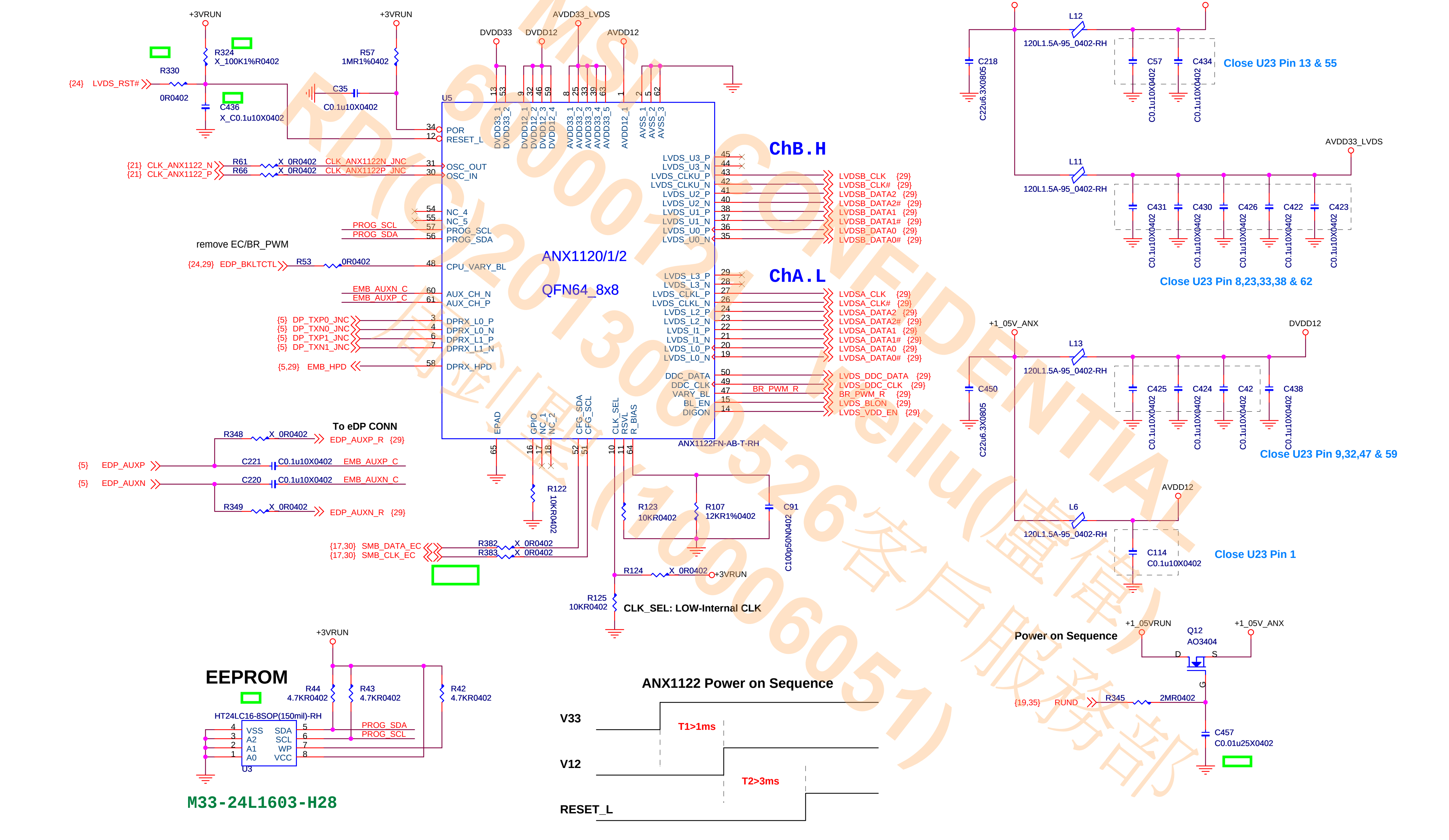
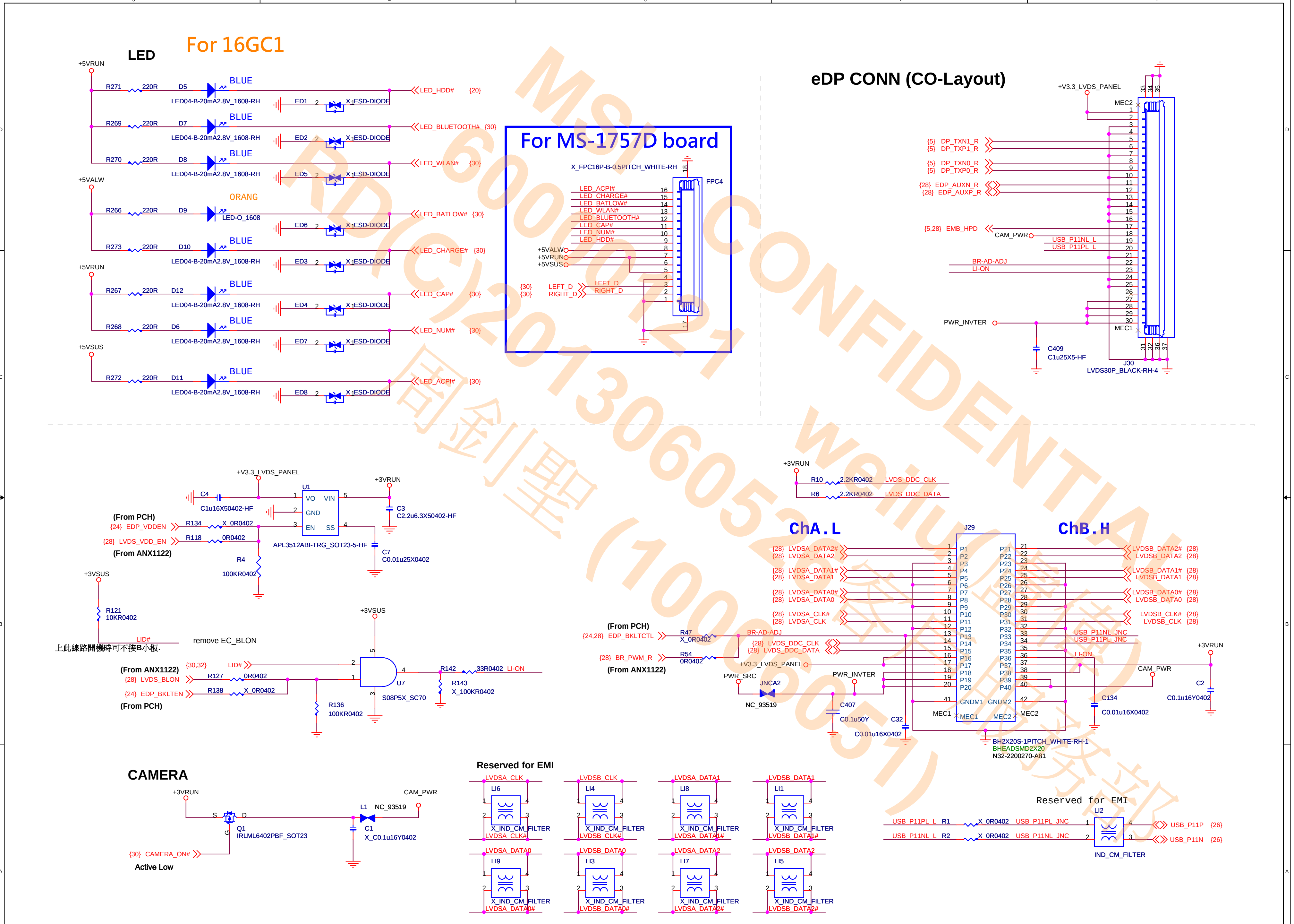
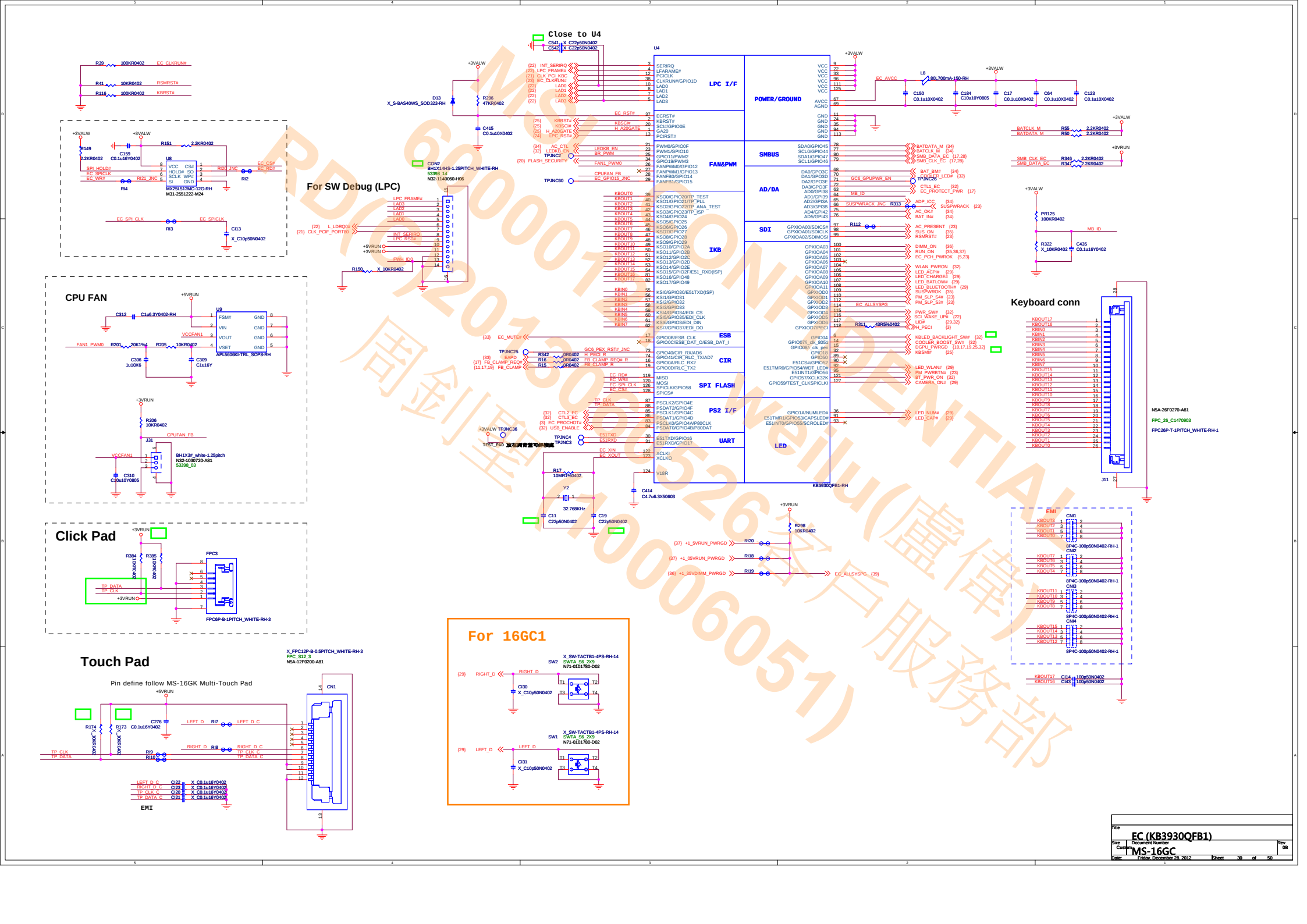
eDP to LVDS

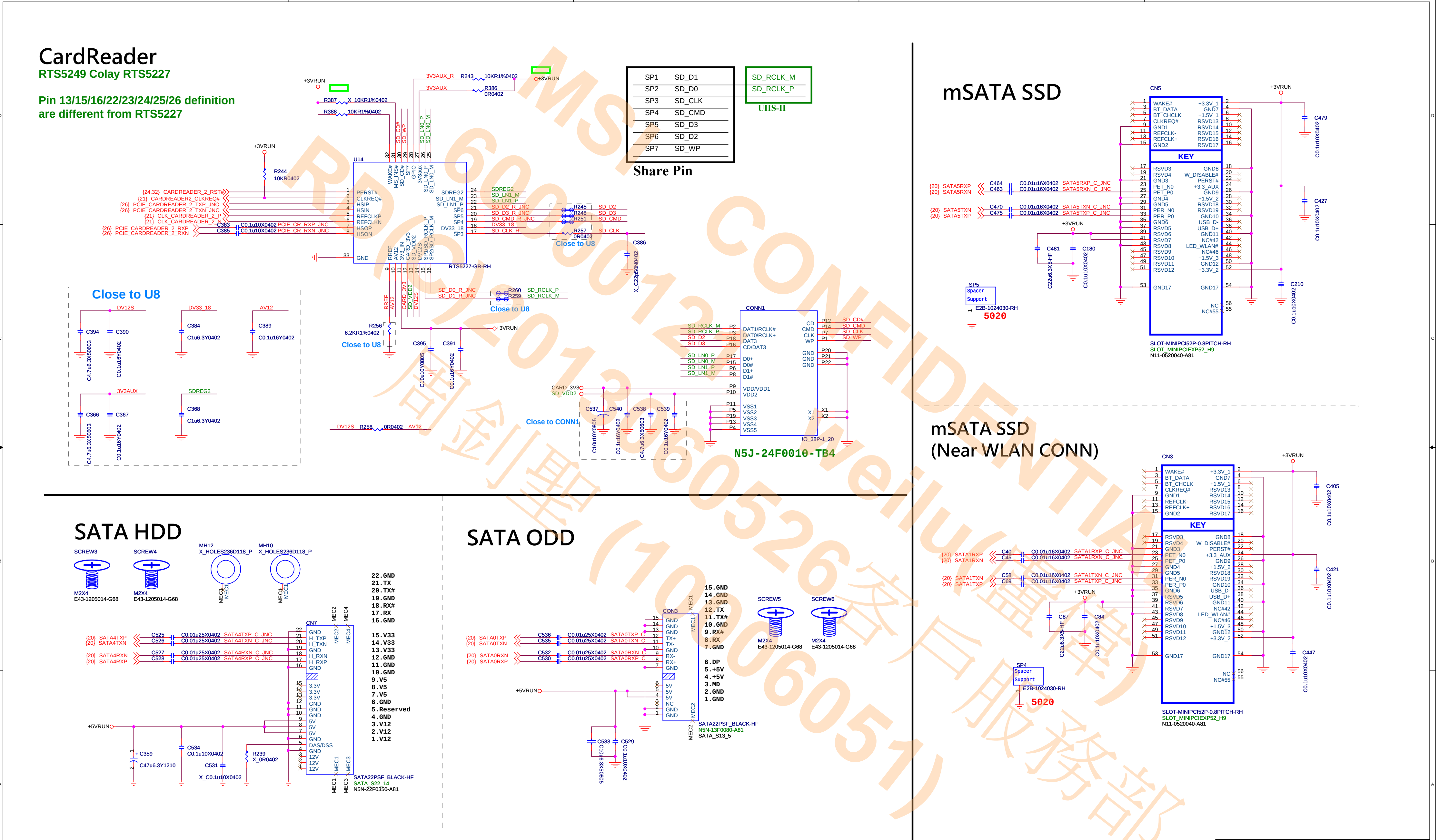


Title	eDP to LVDS (ANX1122)	
Size Custom	Document Number MS-16GC	Rev 0B
Date: Friday, December 28, 2012	Sheet 28 of 50	



Title	FAN/LED/LVDS	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Thursday, December 27, 2012	Sheet 29 of 50	


Close to U4
For SW Debug (LPC)
CPU FAN
Click Pad
Touch Pad
For 16GC1
Keyboard conn
U4
KB3930QFB1-RH
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
U8
M25L512MC-12G-RH
M31-2551222-M24
U9
APL5606KI-TRL_SOP8-RH
CON2
BH1X14HS-1.25PITCH_WHITE-RH
53398_14
N32-1140060-H06
J31
BH1X3#_white-1.25pitch
N32-1030720-A81
53398_03
FPC3
FPC6P-B-1PITCH_WHITE-RH-3
X_FPC12P-B-0.5PITCH_WHITE-RH-3
FPC_S12_3
N5A-12F0200-A81
CN1
EMI
N5A-26F0270-A81
FPC_26_C1470903
FPC26P-T-1PITCH_WHITE-RH-1
Title
EC (KB3930QFB1)
Size
Custom
Document Number
MS-16GC
Rev
0B
Date:
Friday, December 28, 2012
Sheet
30
of
50



Title	Card Reader/HDD/SSD/ODD
Size: Custom	Document Number: MS-16GC
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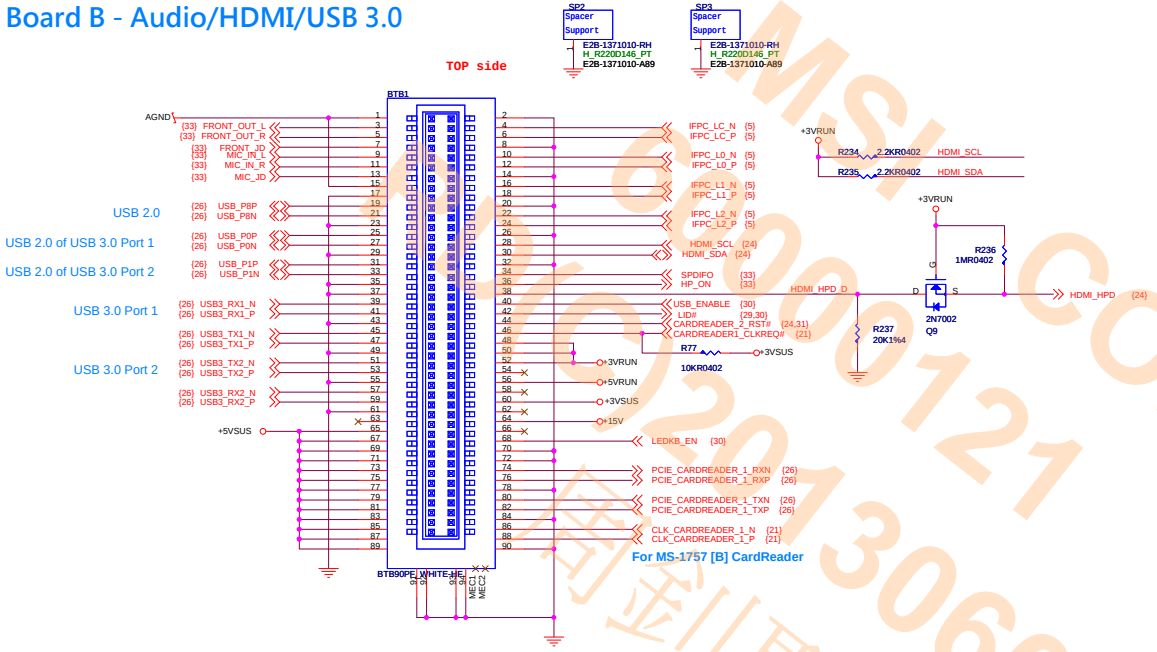
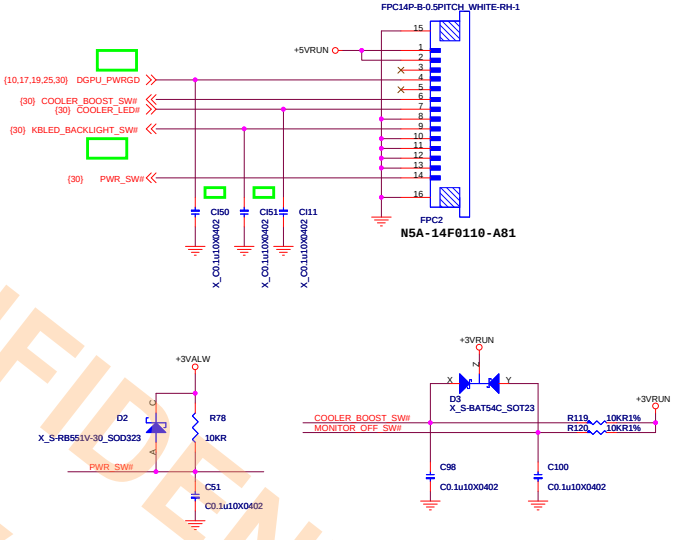
TOP side

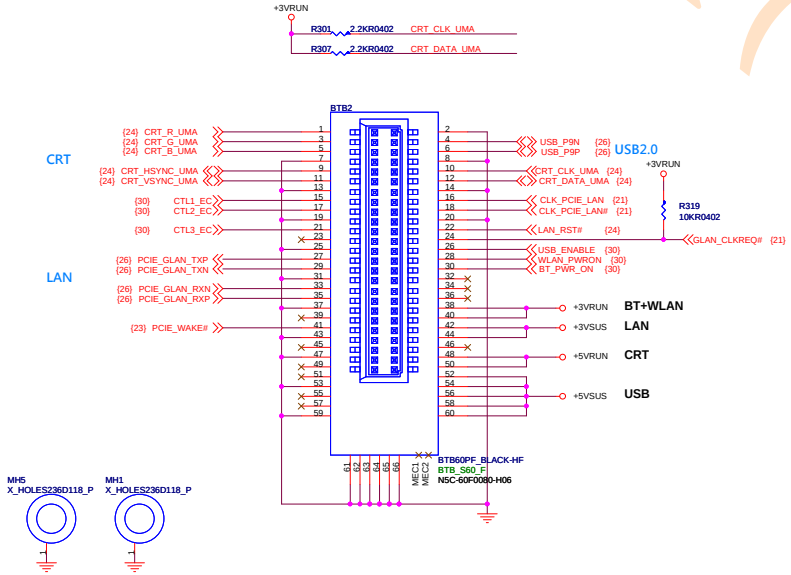
Board B - Audio/HDMI/USB 3.0



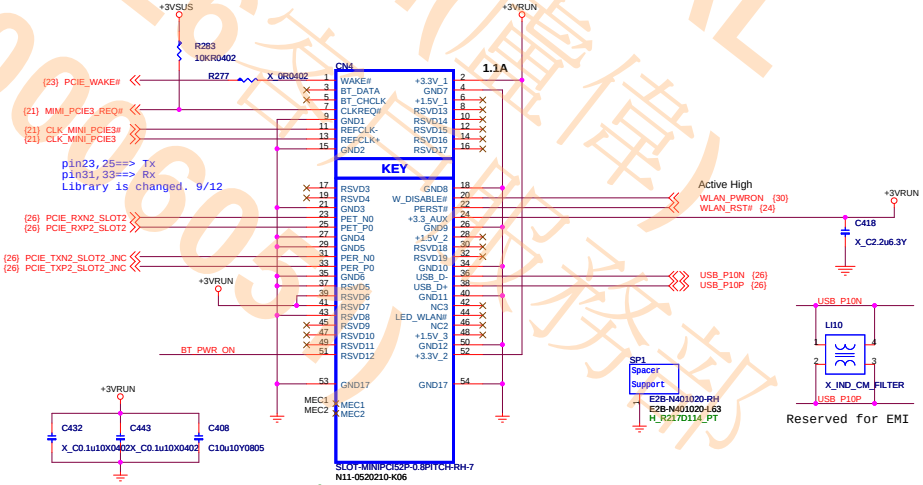
To 16GCC(Power Key Board) / FPCC1



Board A - CRT/USB/WLAN/BT/LAN



WLAN CARD



Title	BTB Connector
Size / Custom	Document Number: MS-16GC / Rev: 0B
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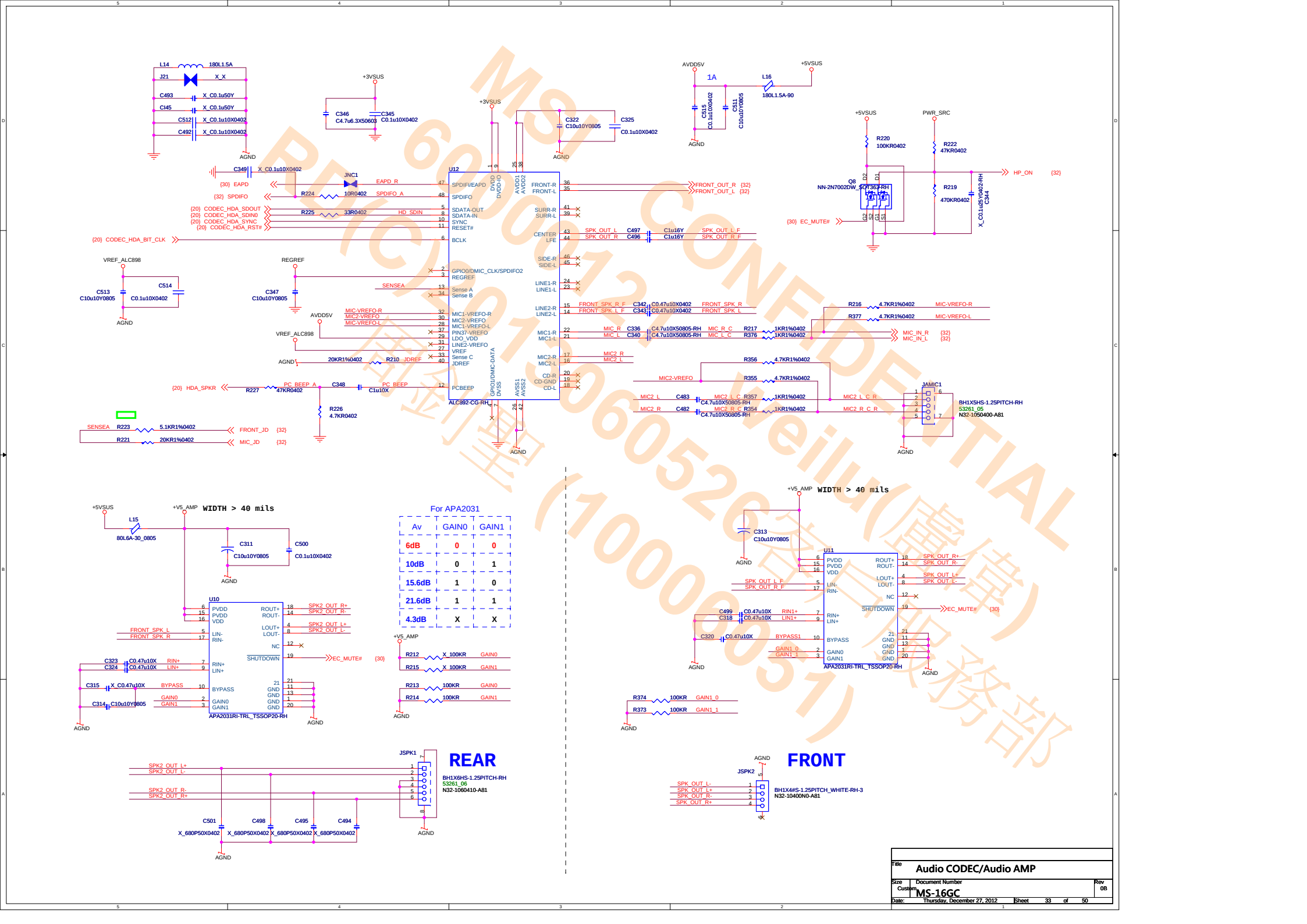
ALC892-CG-RH
APA2031RI-TRL_TSSOP20-RH
BH1X5HS-1.25PITCH-RH
BH1X6HS-1.25PITCH-RH
BH1X4#S-1.25PITCH_WHITE-RH-3
NN-2N7002DW_SOT363-RH
REAR
FRONT
For APA2031
Av GAIN0 GAIN1
6dB 0 0
10dB 0 1
15.6dB 1 0
21.6dB 1 1
4.3dB X X
WIDTH > 40 mils
Audio CODEC/Audio AMP
MS-16GC
Thursday, December 27, 2012
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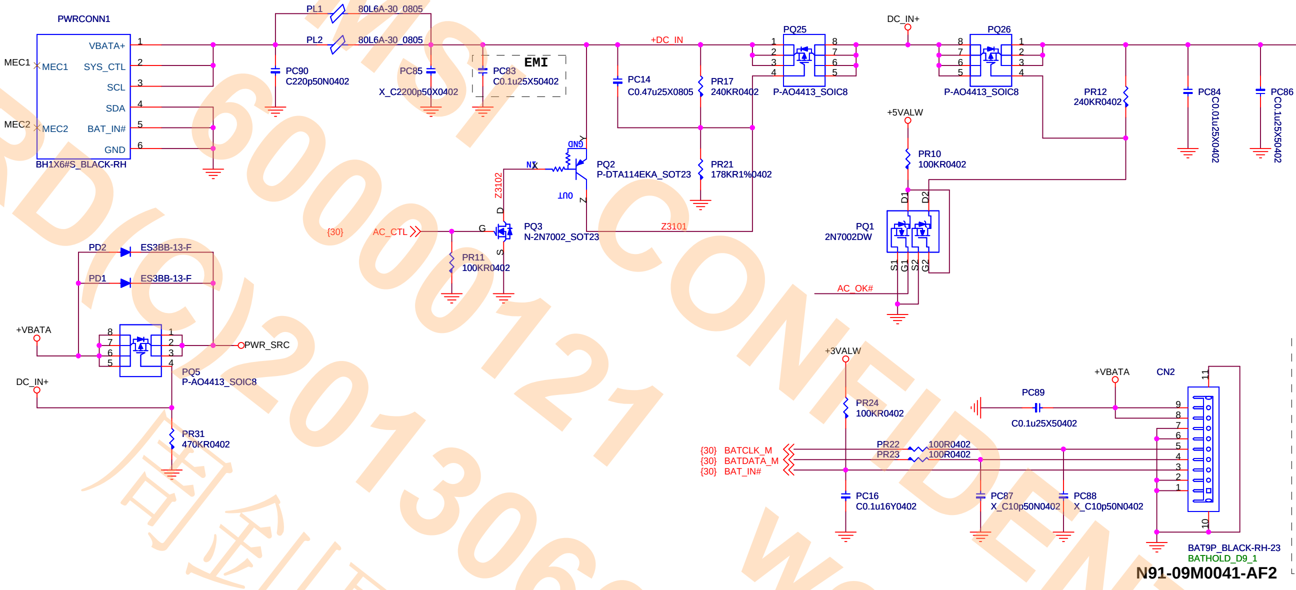
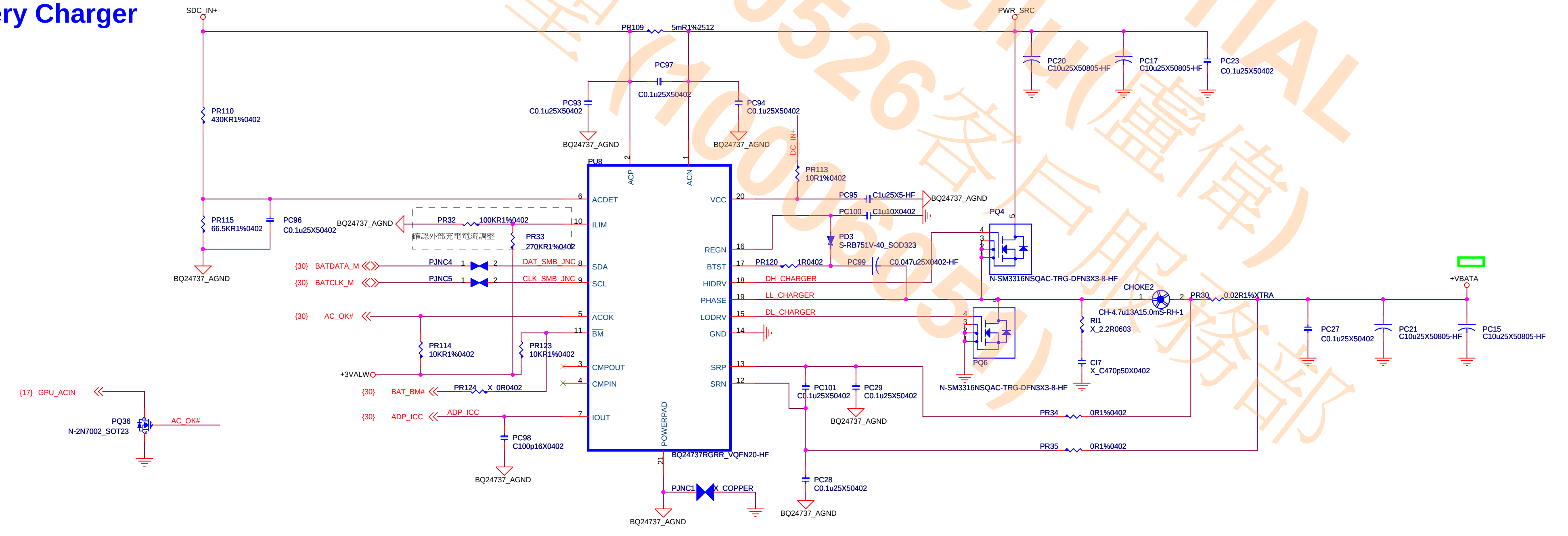
Battery Select



JBAT1 Pin Definition

1: GND
2: GND
3: BAT_IN#
4: SMBDATA
5: SMBCLK
6: NC
7: NC
8: VBATA+
9: VBATA+

Battery Charger



Title: Battery Select/Charger
Size: Custom | Document Number: MS-16GC | Rev: 0B
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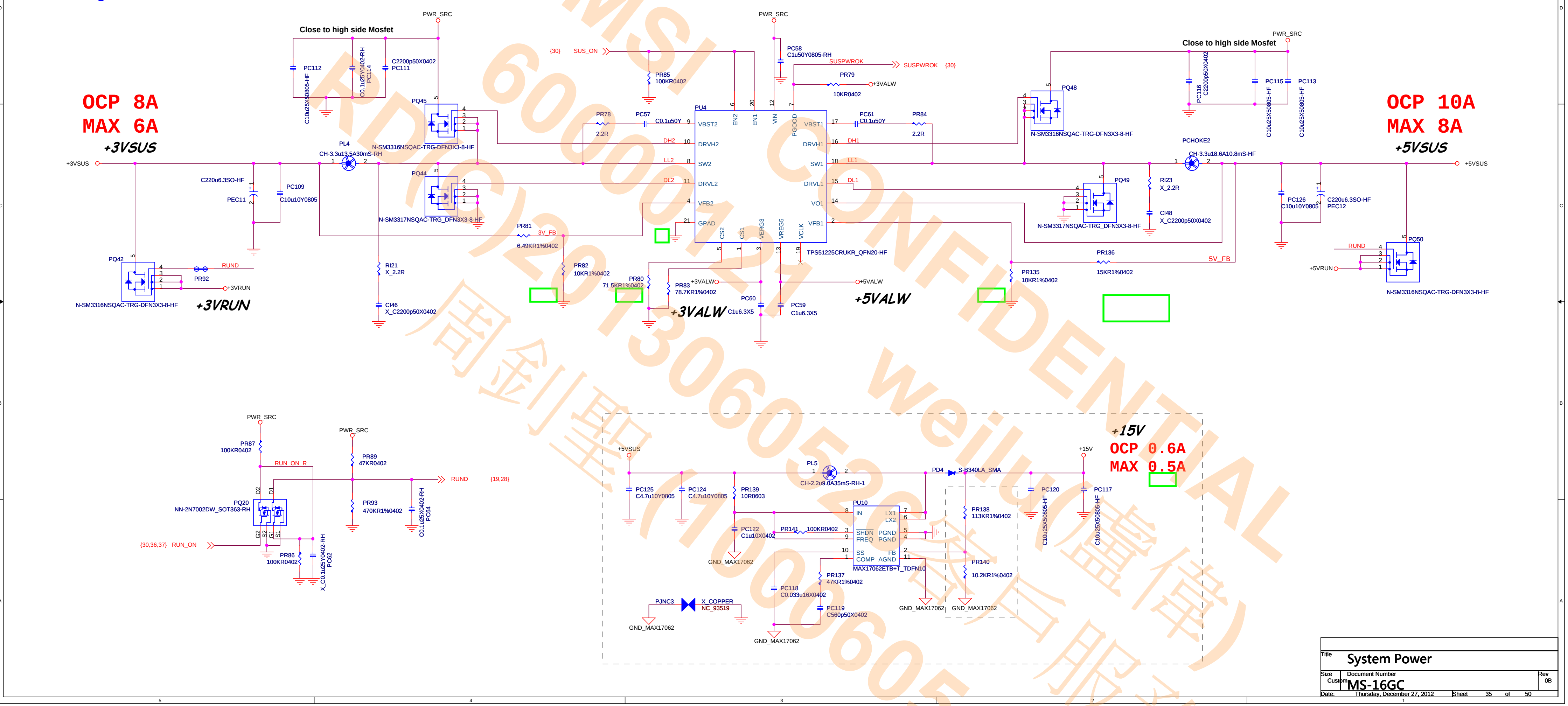
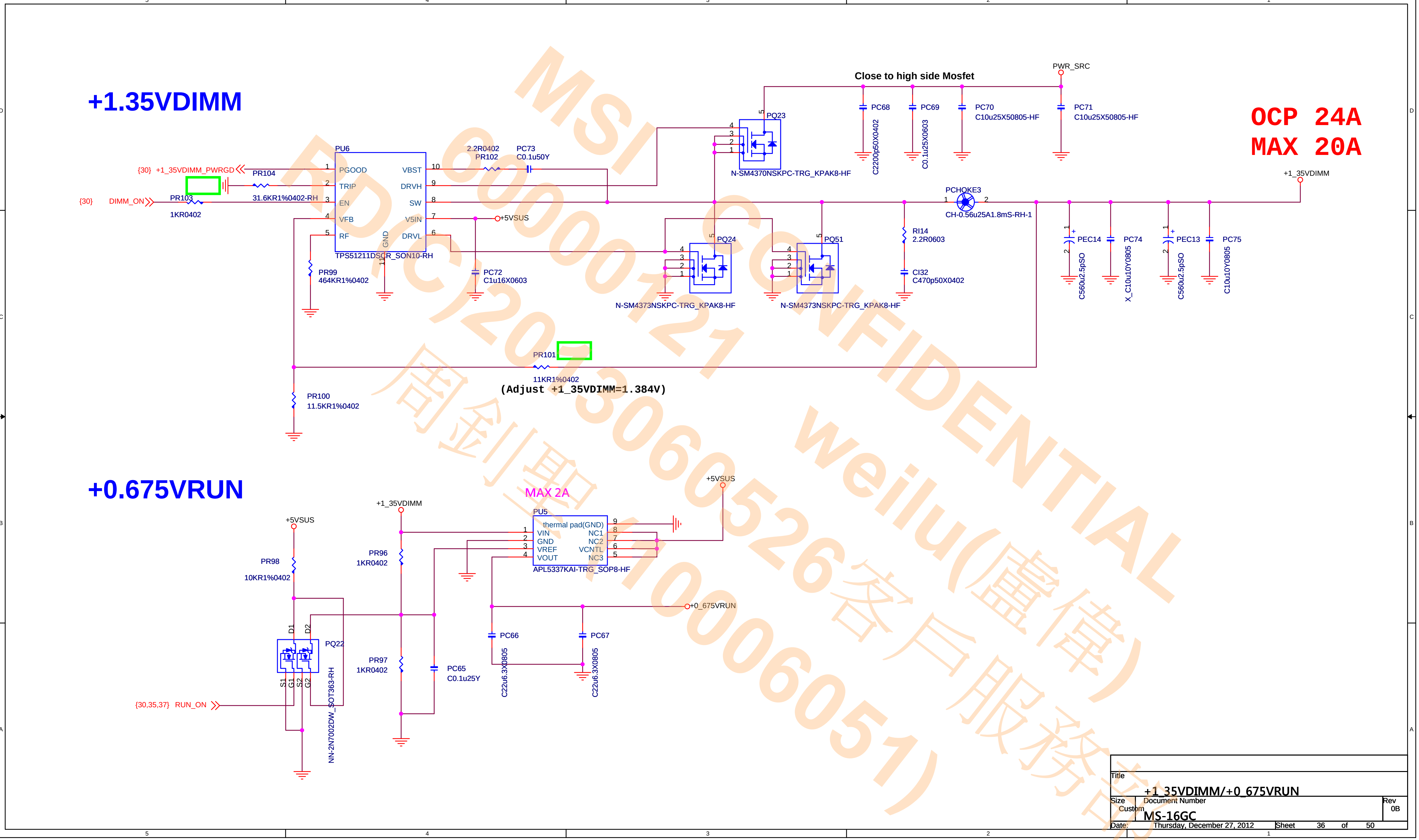
System Power




+1.35VDIMM
OCP 24A
MAX 20A
Close to high side Mosfet
PWR_SRC
PU6
TPS51211DSCR_SON10-RH
PGOOD
TRIP
EN
VFB
RF
GND
VBST
DRVH
SW
V5IN
DRVL
{30} +1_35VDIMM_PWRGD
{30} DIMM_ON
PR103
1KR0402
PR104
31.6KR1%0402-RH
2.2R0402
PR102
PC73
C0.1u50Y
+5VSUS
PR99
464KR1%0402
PC72
C1u16X0603
PQ23
N-SM4370NSKPC-TRG_KPAK8-HF
PQ24
N-SM4373NSKPC-TRG_KPAK8-HF
PQ51
N-SM4373NSKPC-TRG_KPAK8-HF
PC68
C2200p50X0402
PC69
C0.1u25X0603
PC70
C10u25X50805-HF
PC71
C10u25X50805-HF
PCHOKE3
CH-0.56u25A1.8mS-RH-1
RI14
2.2R0603
CI32
C470p50X0402
+1_35VDIMM
PEC14
C560u2.5pSO
PC74
X_C10u10Y0805
PEC13
C560u2.5pSO
PC75
C10u10Y0805
PR101
11KR1%0402
(Adjust +1_35VDIMM=1.384V)
PR100
11.5KR1%0402
+0.675VRUN
MAX 2A
+1_35VDIMM
+5VSUS
PU5
APL5337KAI-TRG_SOP8-HF
thermal pad(GND)
VIN
GND
VREF
VOUT
NC1
NC2
VCNTL
NC3
PR98
10KR1%0402
PR96
1KR0402
PR97
1KR0402
PC65
C0.1u25Y
PC66
C22u6.3X0805
PC67
C22u6.3X0805
+0_675VRUN
PQ22
NN-2N7002DW_SOT363-RH
{30,35,37} RUN_ON
Title
+1_35VDIMM/+0_675VRUN
Size
Custom
Document Number
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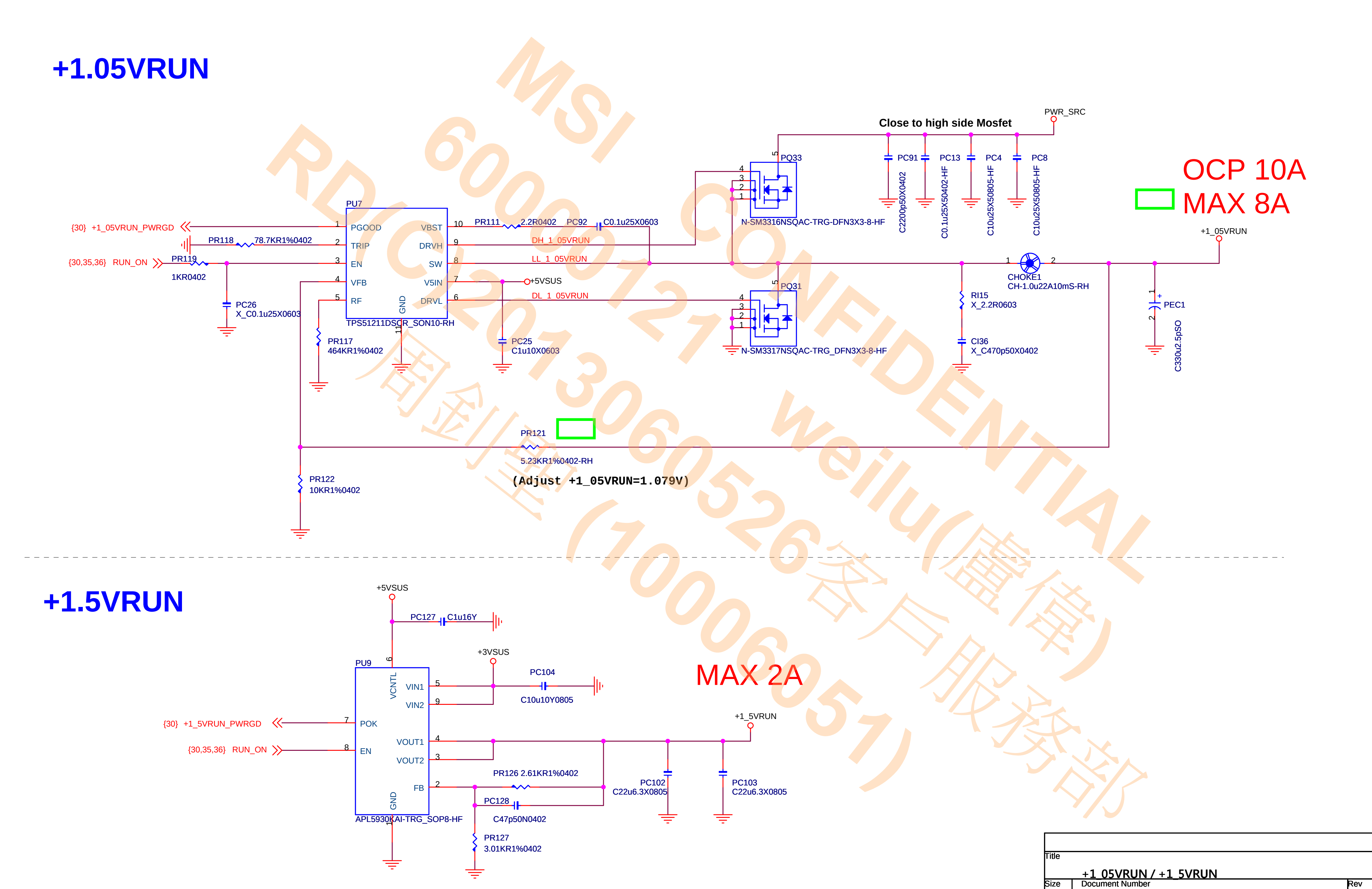

Title	+1_05VRUN / +1_5VRUN	
Size: Custom	Document Number: MS-16GC	Rev: 0B
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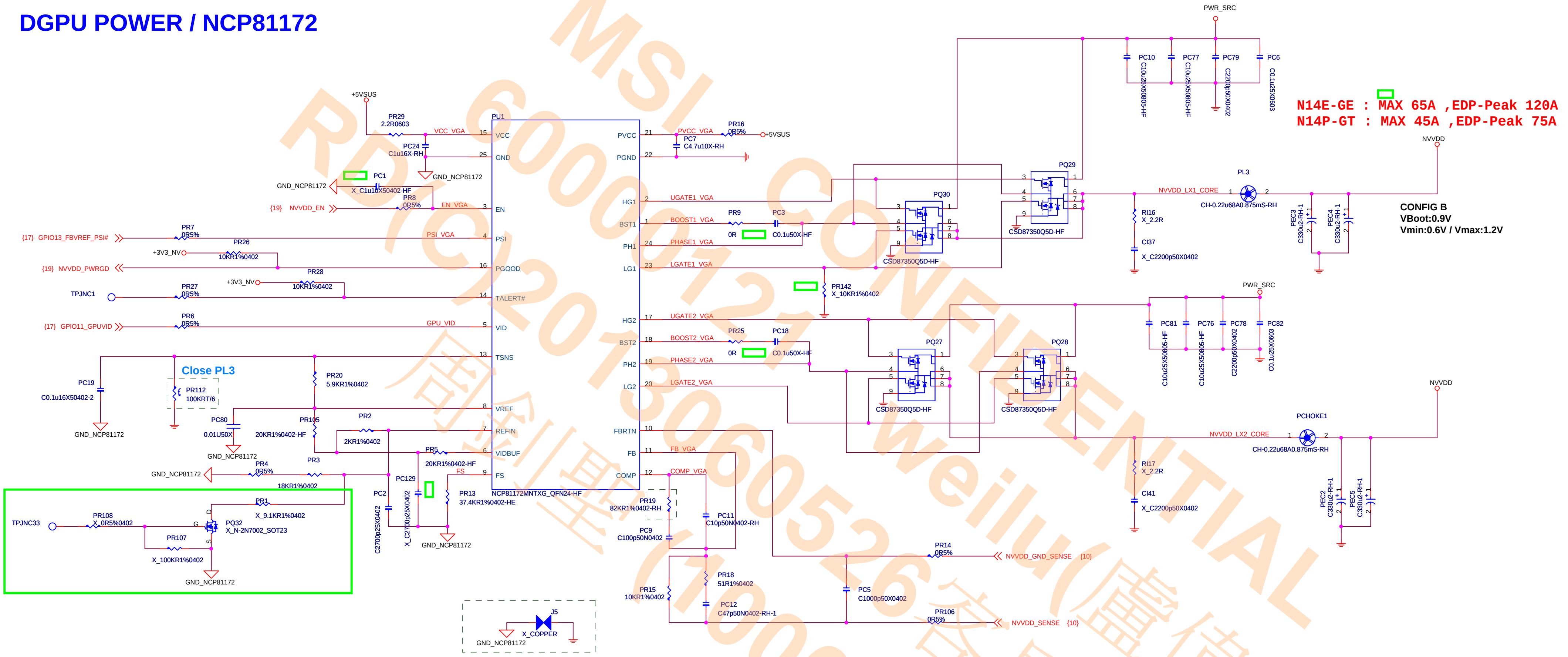
DGPU POWER / NCP81172



Title	DGPU Power	
Size Custom	Document Number MS-16GC	Rev 0B
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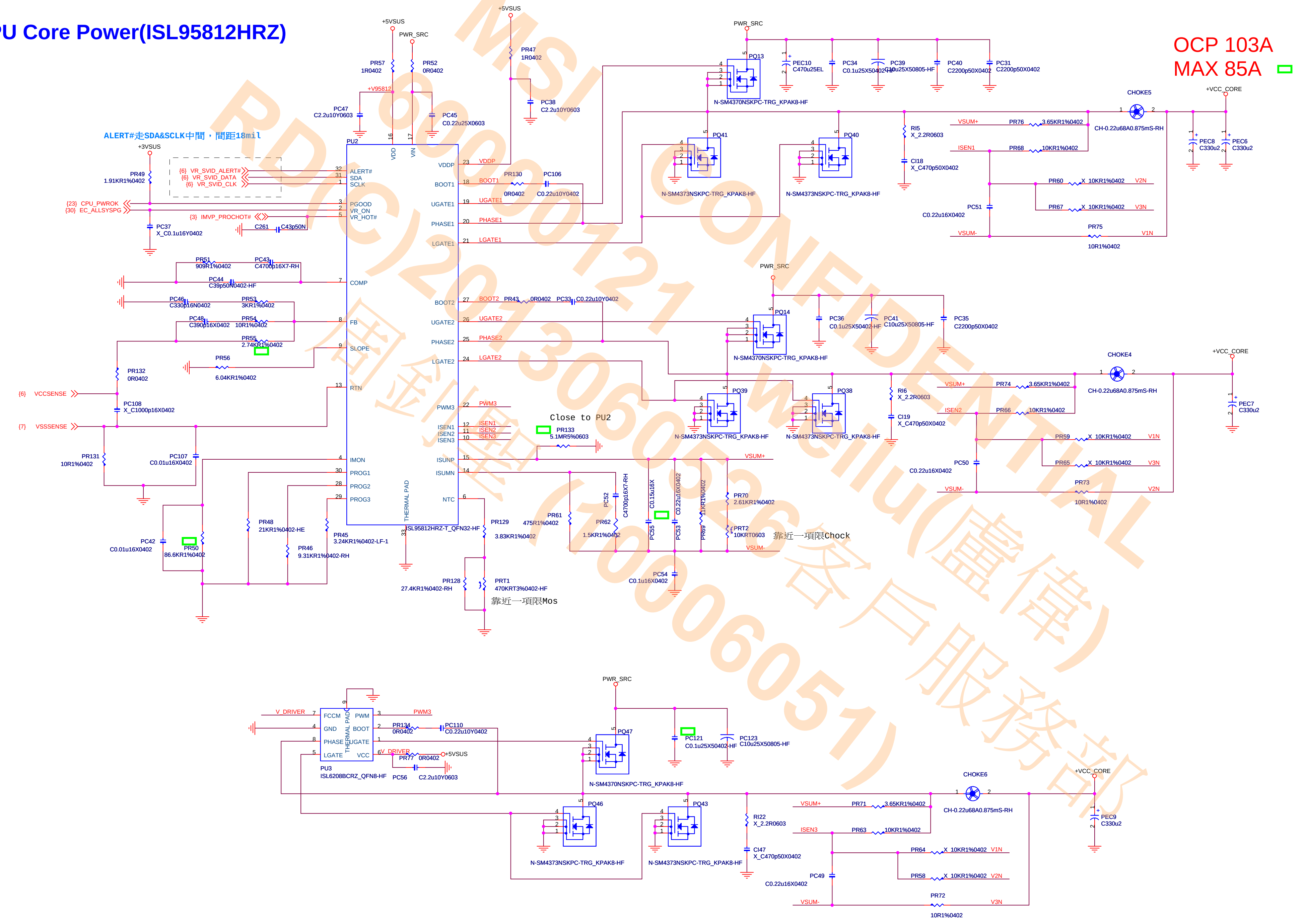
CPU Core Power(ISL95812HRZ)



Title	CPU Power		
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HOLES_NR91D91
H4

NPTH118
H5

HOLE118
H7

HOLE118
H1

HOLE118
H2

HOLE118
H6

HOLES_8X8_D3MM_VIA8
MH13 X_8x8

H_R315D118_PT_V3
MH2 X_8x8

HOLES_8X8_D3MM_VIA3
MH9 X_8x8

H_R295D118_V3
MH4 X_8x8

HOLES_8X8_D3MM_VIA8
MH8 X_8x8

H_R315D118_PT_V3
MH3 X_8x8

MH11
X_8.5x8.5

HOLES_8X8_D3MM_VIA3
MH7 X_8x8

HOLES_8X8_D3MM_VIA8
MH6 X_8x8

HOLES_8X8_D3MM_VIA8
MH14 X_8x8

FM10 FM15 FM18 FM13 FM4 FM19 FM3 FM8 FM9 FM6 FM5 FM17 FM1 FM14 FM7 FM16 FM11 FM12 FM2

TOP SPRING

PAD7 X_HS-MS1011-RH E23-1011040-CA7
PAD9 X_HS-MS1011-RH E23-1011040-CA7
PAD5 X_HS-MS1011-RH E23-1011040-CA7
PAD2 X_HS-MS1011-RH E23-1011040-CA7
PAD8 X_HS-MS1011-RH E23-1011040-CA7
PAD13 X_HS-MS1011-RH E23-1011040-CA7

BOT SPRING

PAD4 X_HS-MS1011-RH E23-1029060-CA7
PAD16 X_HS-MS1011-RH E23-1011040-CA7
PAD17 X_HS-MS1011-RH E23-1011040-CA7

CPU

CPU_H2 X_CPU SCREW HOLE HOLES_R276D185P_PT
CPU_H1 X_CPU SCREW HOLE HOLES_R276D185P_PT
CPU_H4 X_CPU SCREW HOLE HOLES_R276D185P_PT
CPU_H3 X_CPU SCREW HOLE HOLES_R276D185P_PT

Bracket1 CPU Bracket 307-6G10212-A89
UME4 ME E2Y-Z001711-Y42
UME5 ME E2Y-Z001711-Y42
UME6 ODD CONN mylar E2P-6G14611-Y42
Bracket2 GPU Bracket 307-6G10311-A20
UME7 ME E2M-6G11612-Y42
UME8 ME E2Y-6G10912-Y42

GPU

GPU_H2 X_CPU SCREW HOLE HOLES_R276D185P_PT
GPU_H1 X_CPU SCREW HOLE HOLES_R276D185P_PT
H_NR177D177_1
H3
GPU_H4 X_CPU SCREW HOLE HOLES_R276D185P_PT
GPU_H3 X_CPU SCREW HOLE HOLES_R276D185P_PT

SCREW1 X_M2X3 E43-1203003-G68
SCREW2 X_M2X3 E43-1203003-G68

04/20
ADD SB Heatsink and Screw x2

RACK1 X_RACK1 E2P-6310611-K23
RACK2 X_RACK1 E2P-6310611-K23

UME1 PCB HDMI ROYALTY Y01-RHDMI03-000

PCB1 PCB

UME16 BIOS LABEL X_BIOS_LABEL

For MP: BIOS Label

Title	Screw/ME		
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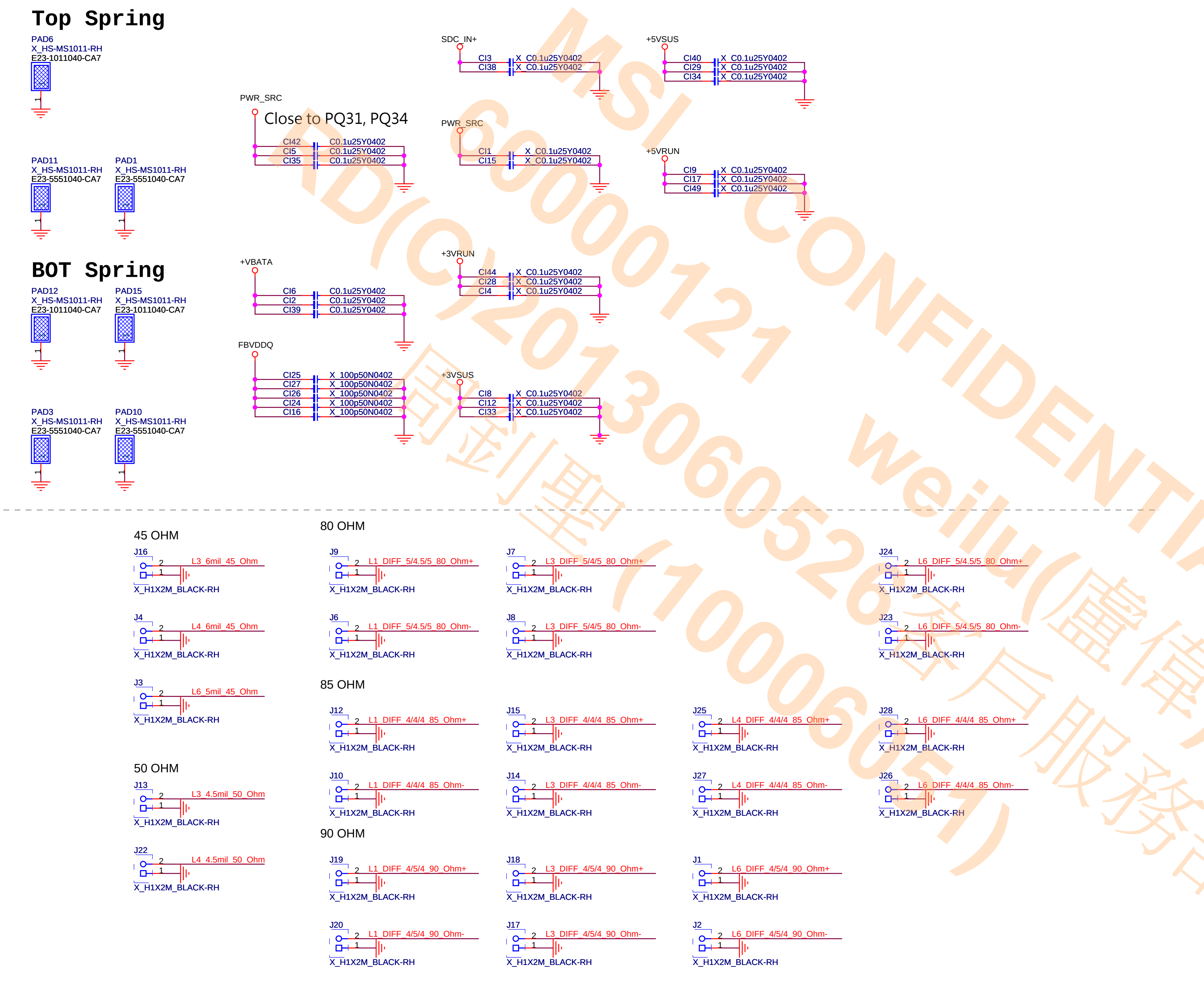

Title
EMI

Size	Document Number	Rev
Custom	MS-16GC	0B

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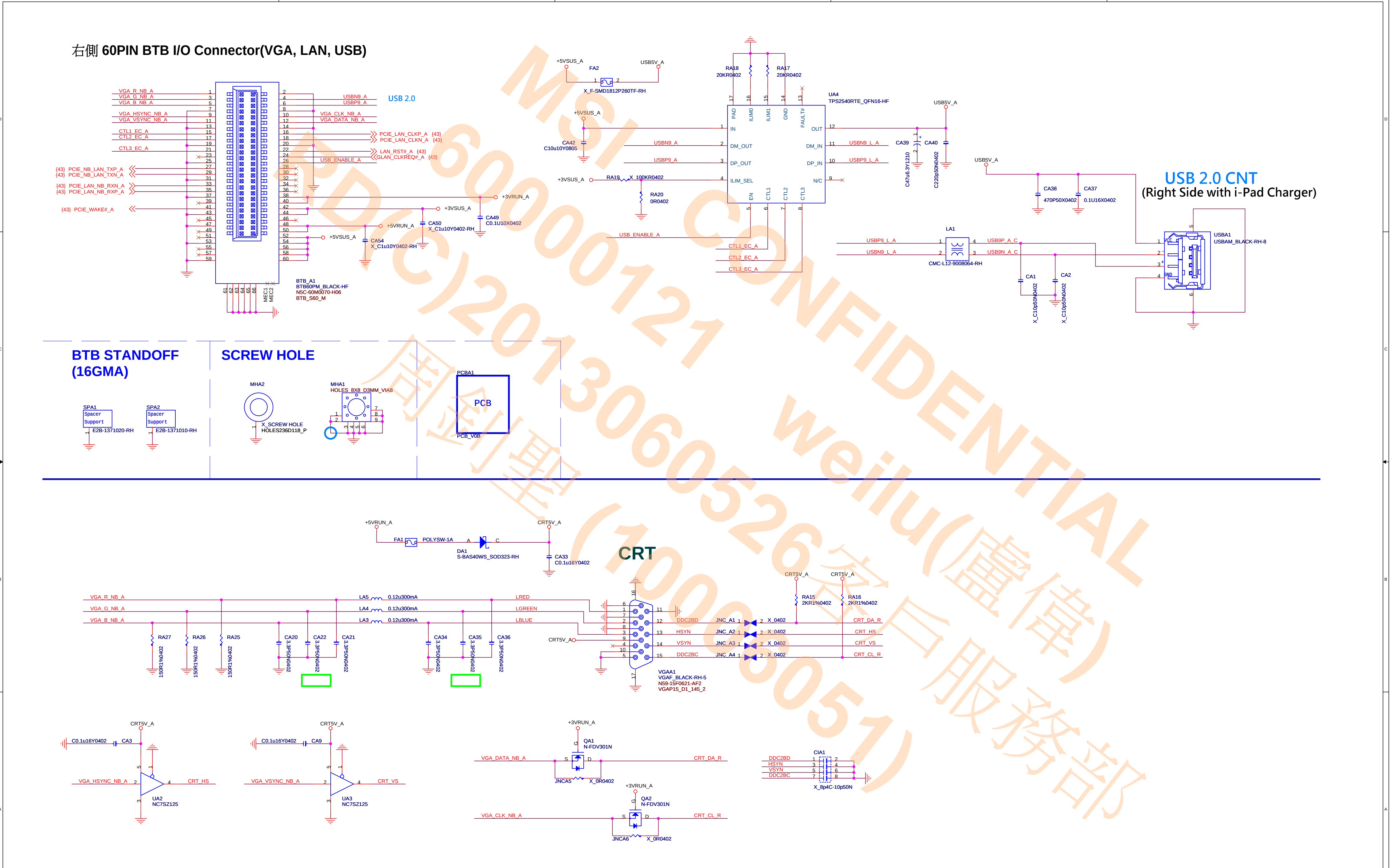

Title	[A] BTB CNT/CRT/USB/WLAN/BT		
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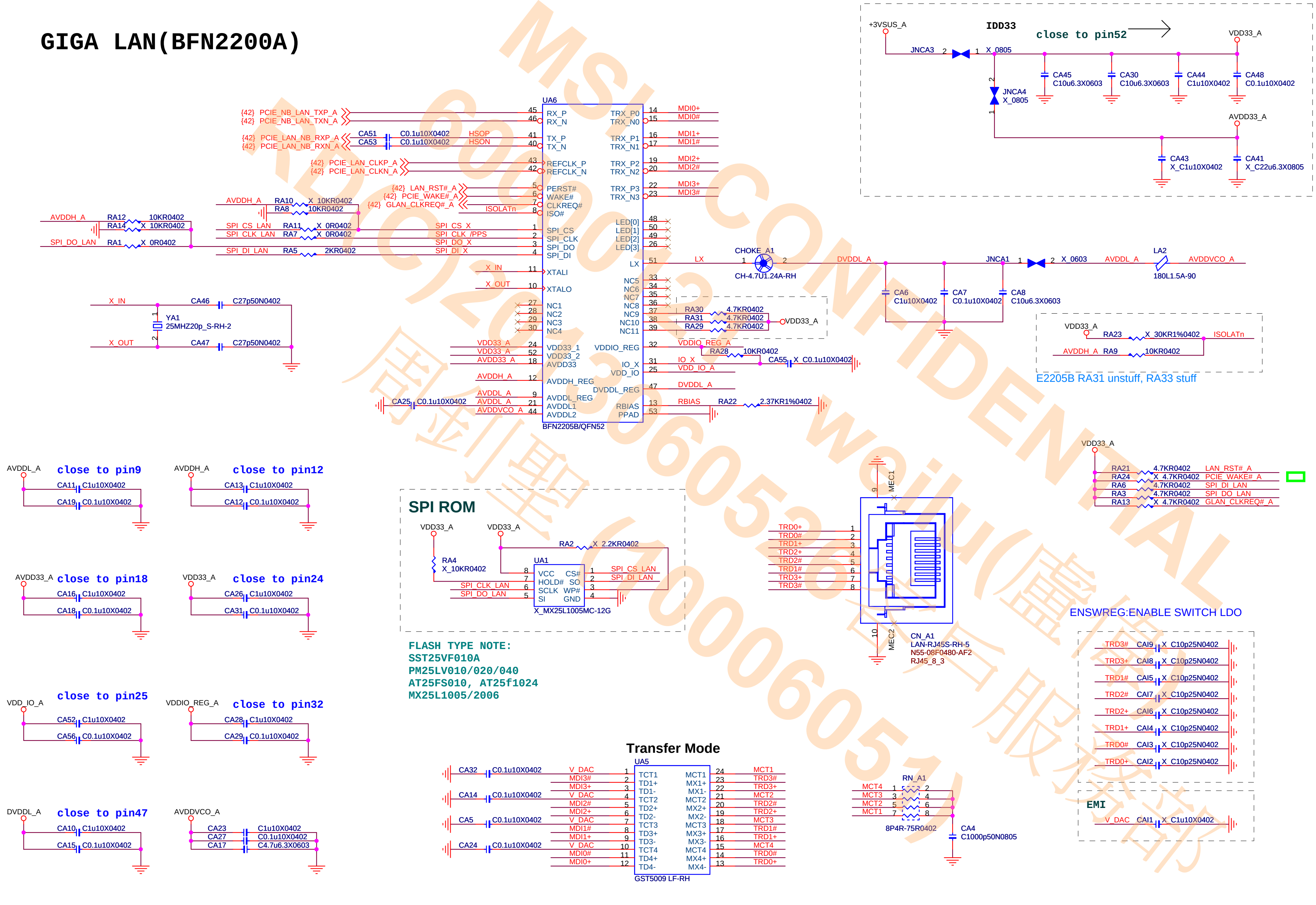
GIGA LAN(BFN2200A)



Title: [A] GIGA LAN(BFN2205B)

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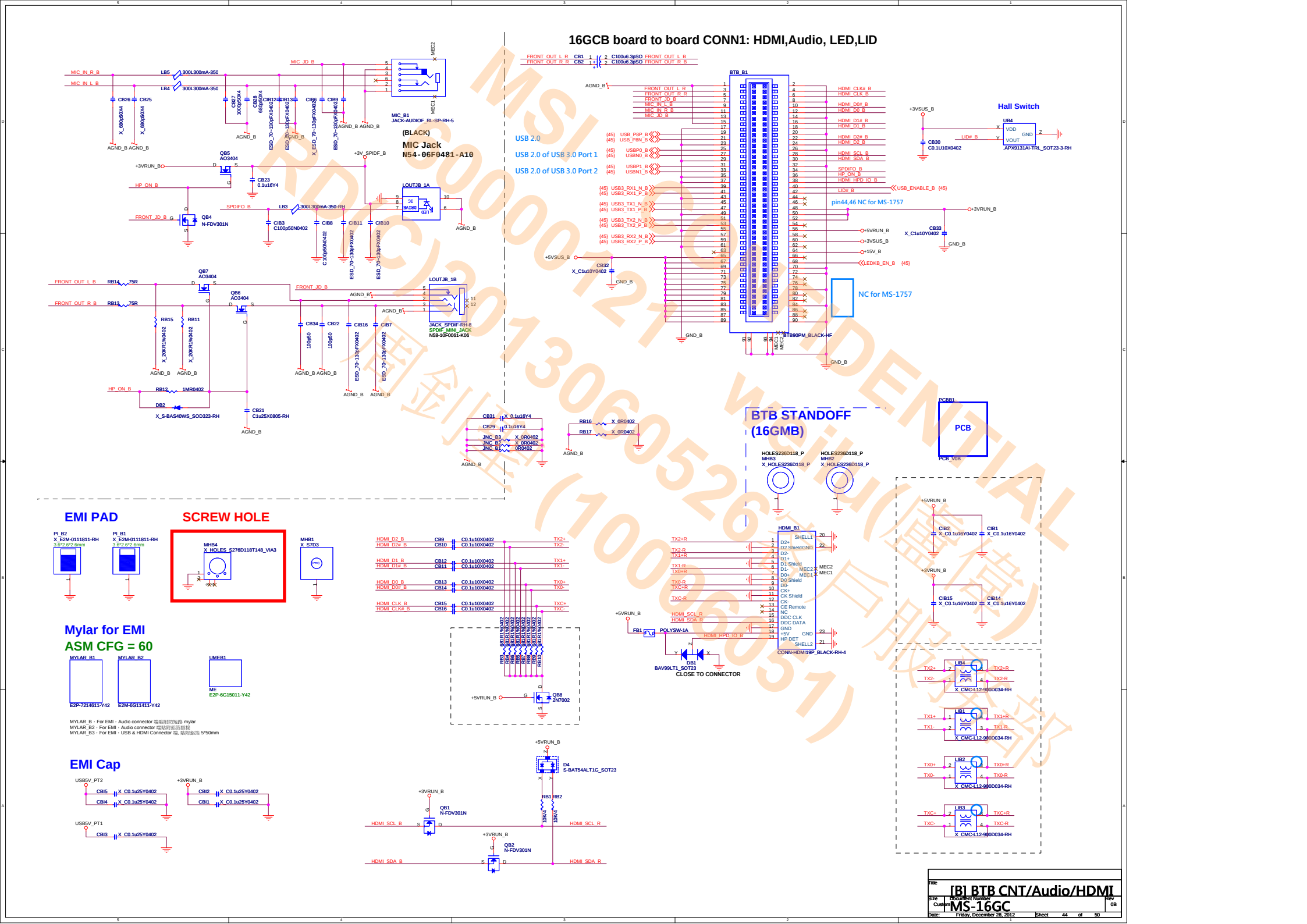
16GCB board to board CONN1: HDMI,Audio, LED,LID
MIC Jack
N54-06F0481-A10
(BLACK)
MIC_B1
JACK-AUDIOF_BL-SP-RH-5
USB 2.0
USB 2.0 of USB 3.0 Port 1
USB 2.0 of USB 3.0 Port 2
Hall Switch
APX9131AI-TRL_SOT23-3-RH
pin44,46 NC for MS-1757
NC for MS-1757
BTB STANDOFF
(16GMB)
PCB
PCB_V0B
EMI PAD
SCREW HOLE
Mylar for EMI
ASM CFG = 60
MYLAR_B1
MYLAR_B2
E2P-7214611-Y42
E2M-6C11411-Y42
ME
E2P-6G15011-Y42
MYLAR_B：For EMI，Audio connector 端貼附防短路 mylar
MYLAR_B2：For EMI，Audio connector 端貼附鋁箔搭接
MYLAR_B3：For EMI，USB & HDMI Connector 端, 貼附鋁箔 5*50mm
EMI Cap
CLOSE TO CONNECTOR
BAV99LT1_SOT23
CONN-HDMI19P_BLACK-RH-4
BT890PM_BLACK-HF
JACK_SPDIF-RH-8
SPDIF_MINI_JACK
N58-10F0061-K06
Title
[B] BTB CNT/Audio/HDMI
Size
Custom
Document Number
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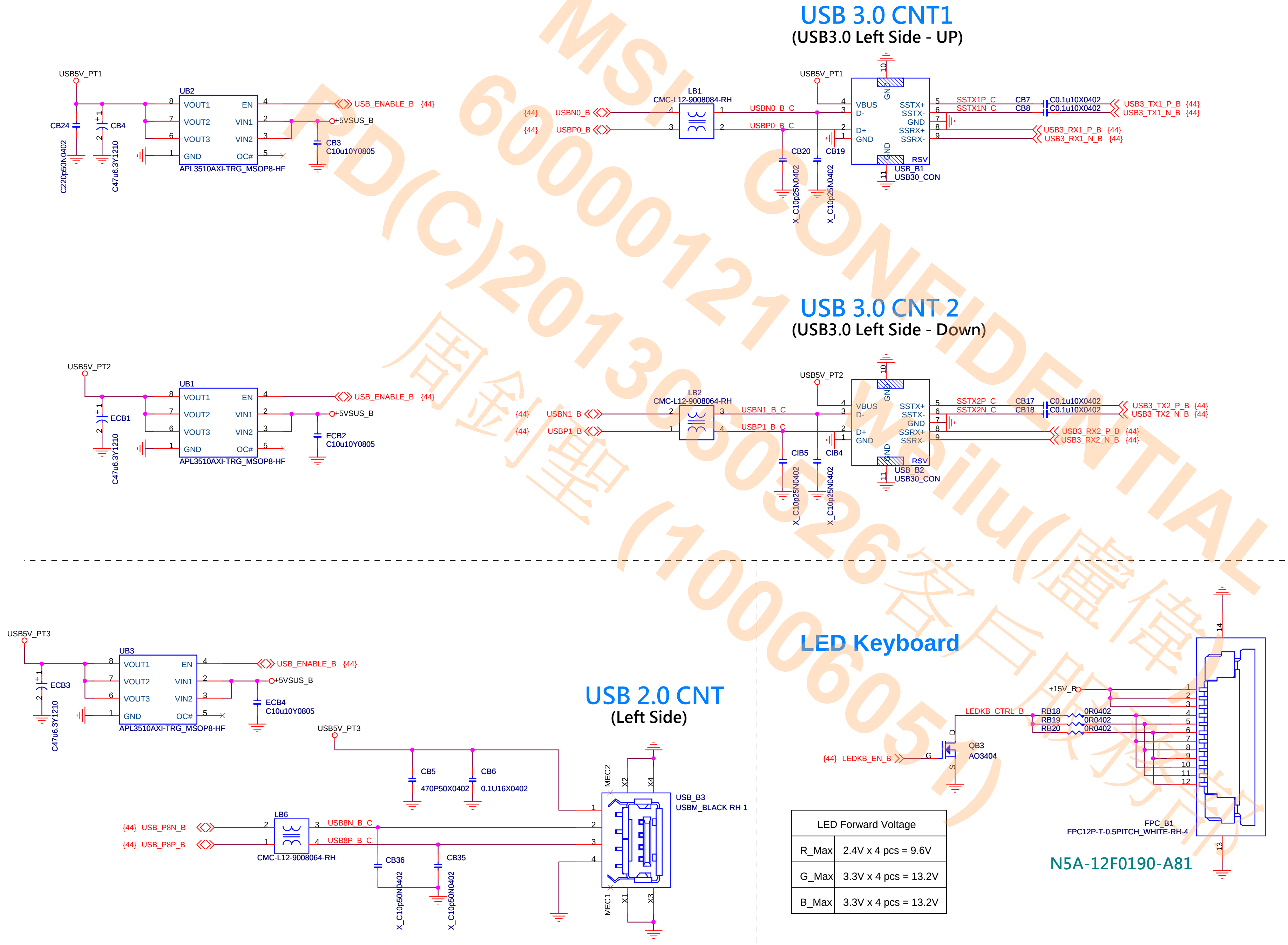

LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

LED Forward Voltage	
R_Max	2.4V x 4 pcs = 9.6V
G_Max	3.3V x 4 pcs = 13.2V
B_Max	3.3V x 4 pcs = 13.2V

Title: [B] USB3.0x2/USB2.0x1/LED KB

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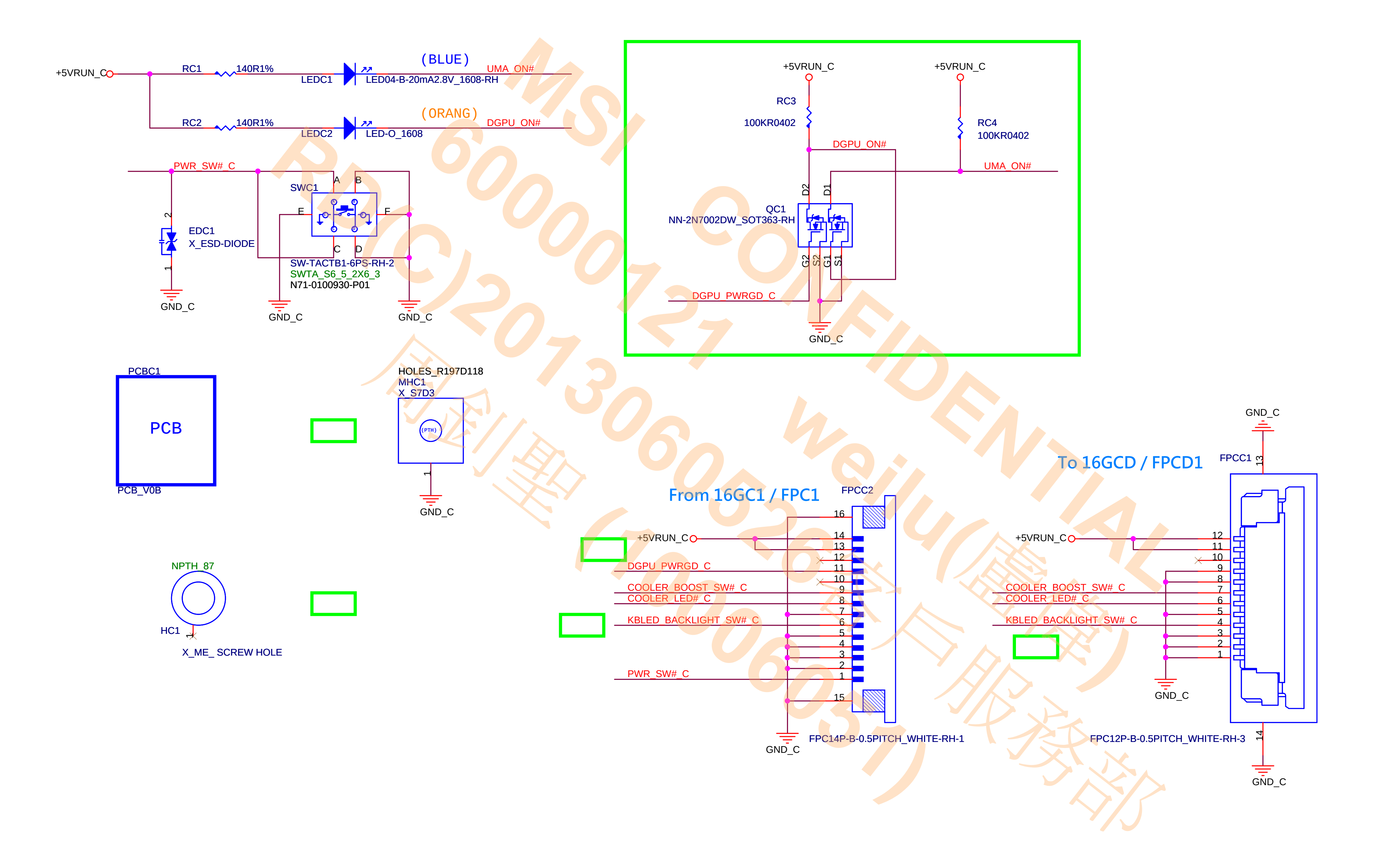

Title	[C] Power SW Board
Size: Custom	Document Number: MS-16GC
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Date:	Friday, December 28, 2012
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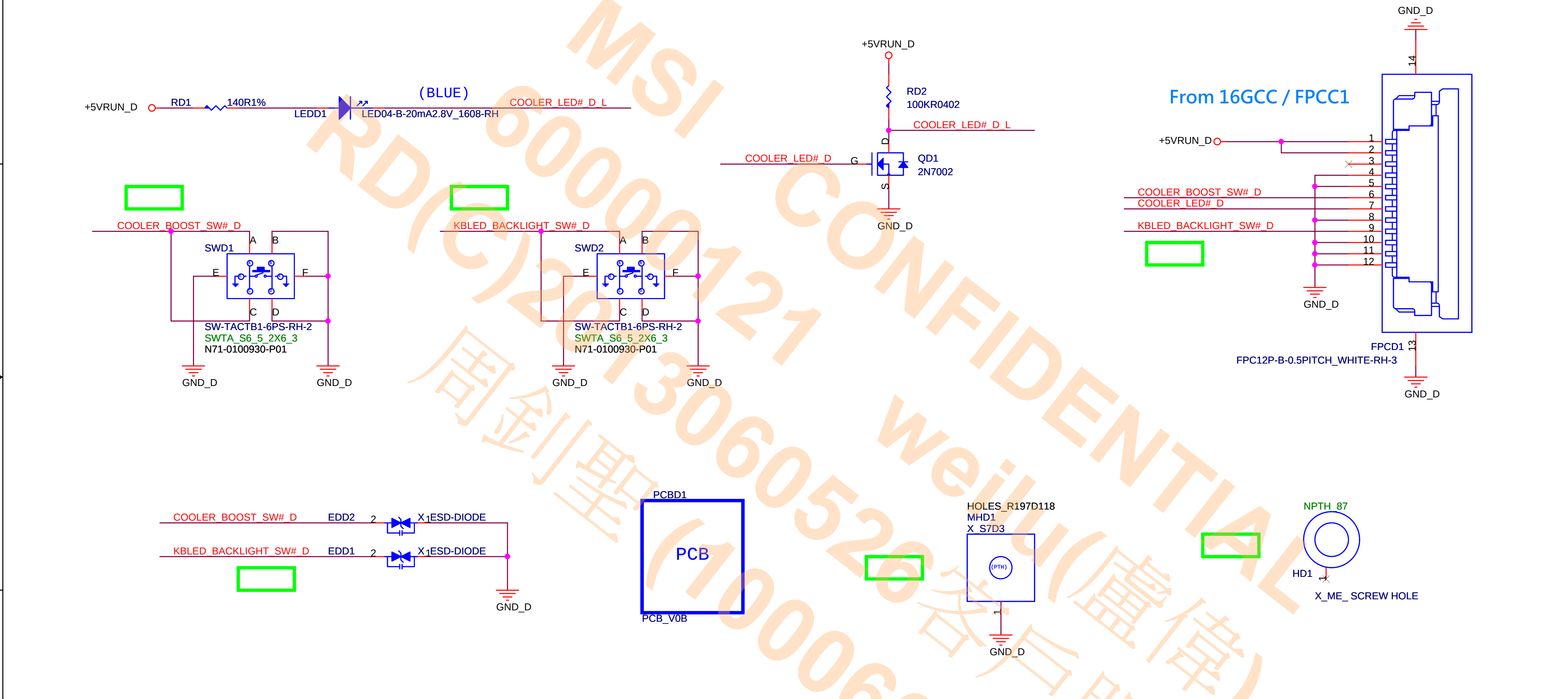

Title	[D] Launch Board	
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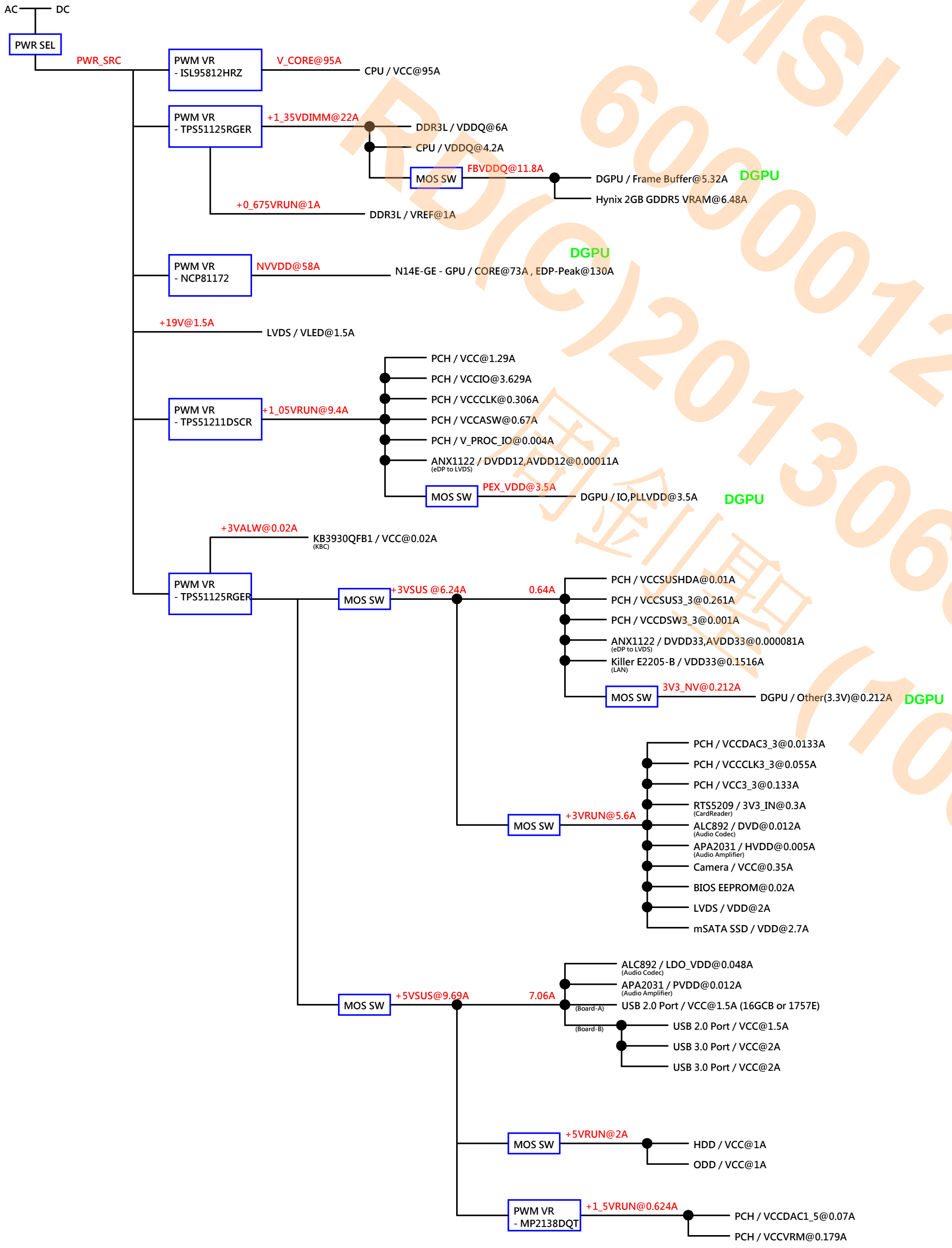
16GC Power Delivery Chart



Power Delivery Chart
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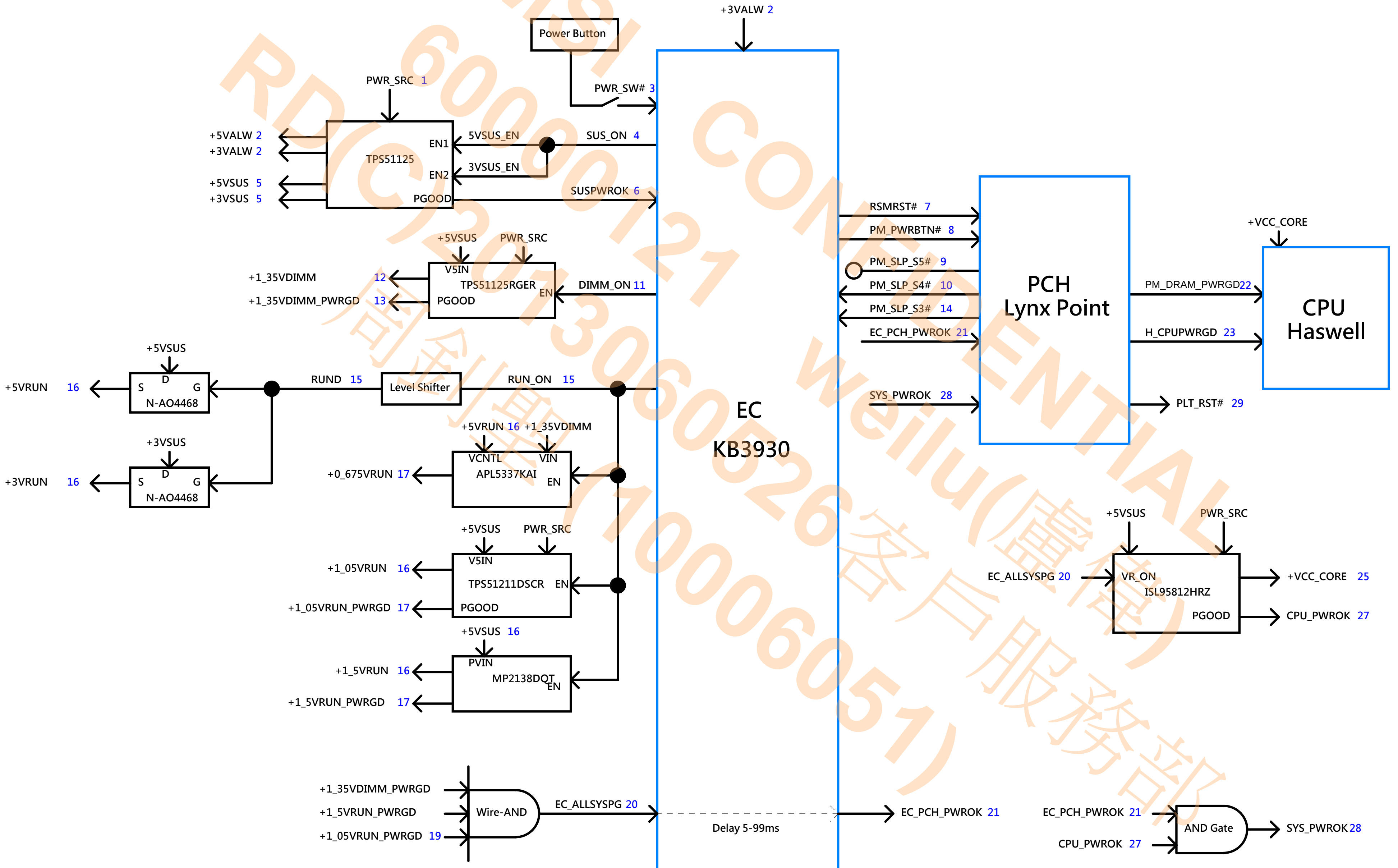
16GC Power on Block Diagram



Title: Power on Block Diagram		
Size: Custom	Document Number: MS-16GC	Rev: 0B
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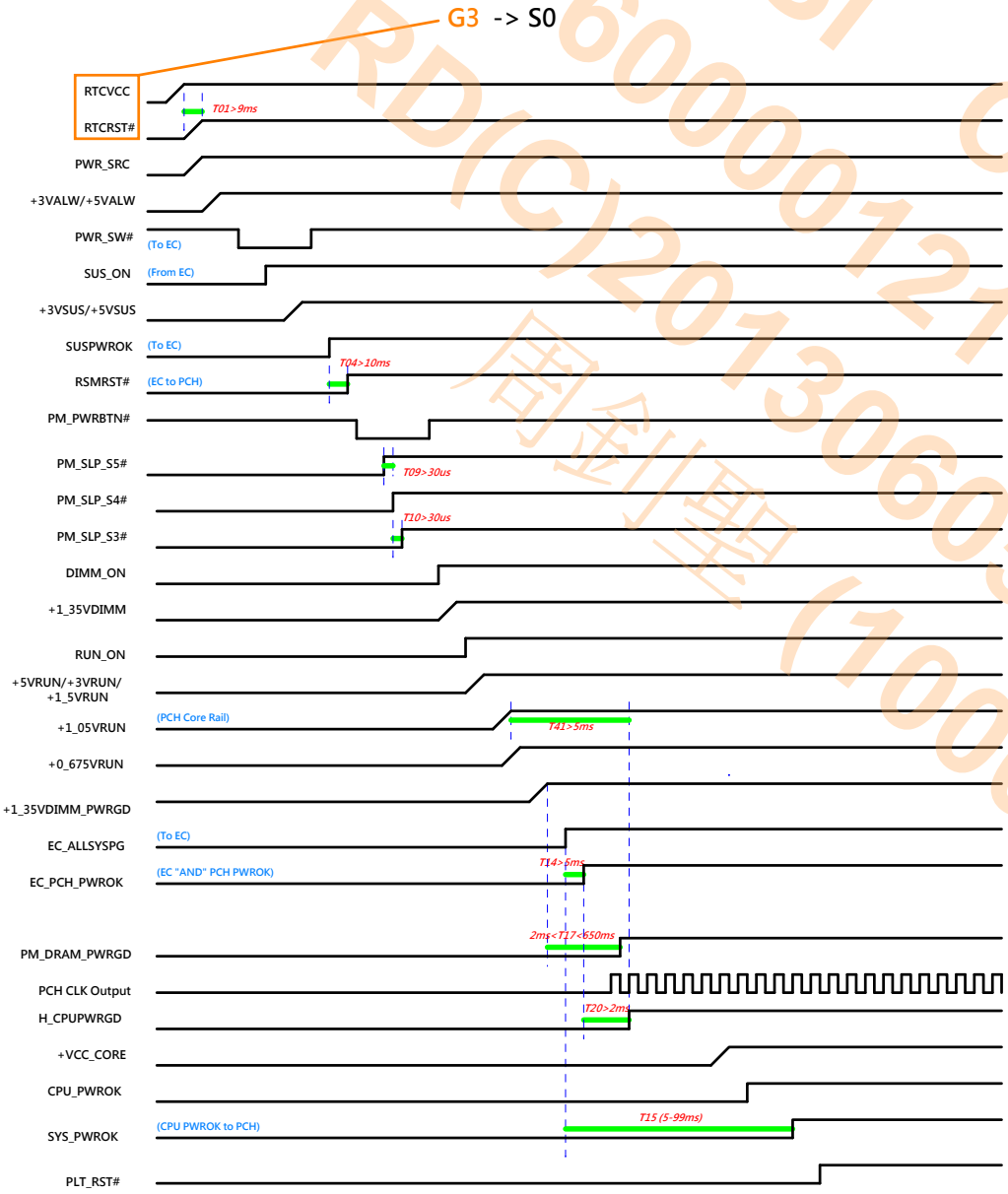
Power on Sequence



Title	Power on Sequence	
Size: Custom	Document Number: MS-16GC	Rev: 0B
Date: Thursday, December 27, 2012	Sheet 50 of 50	