MS-1755 Ver : 10 (nVIDIA N13P-GS/GL)

Chief River Platform

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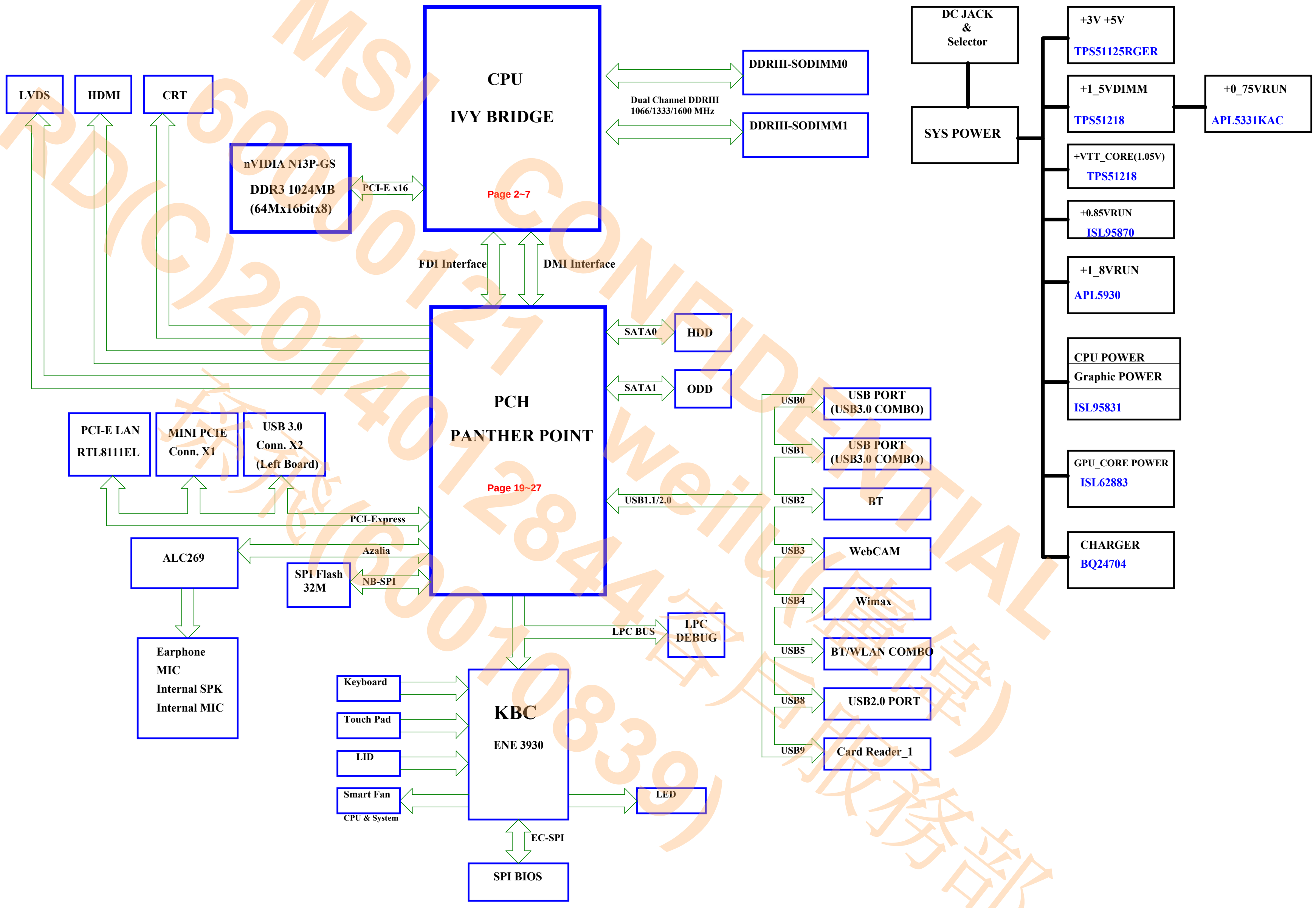
Page Description



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Title	BLOCK DIAGRAM	
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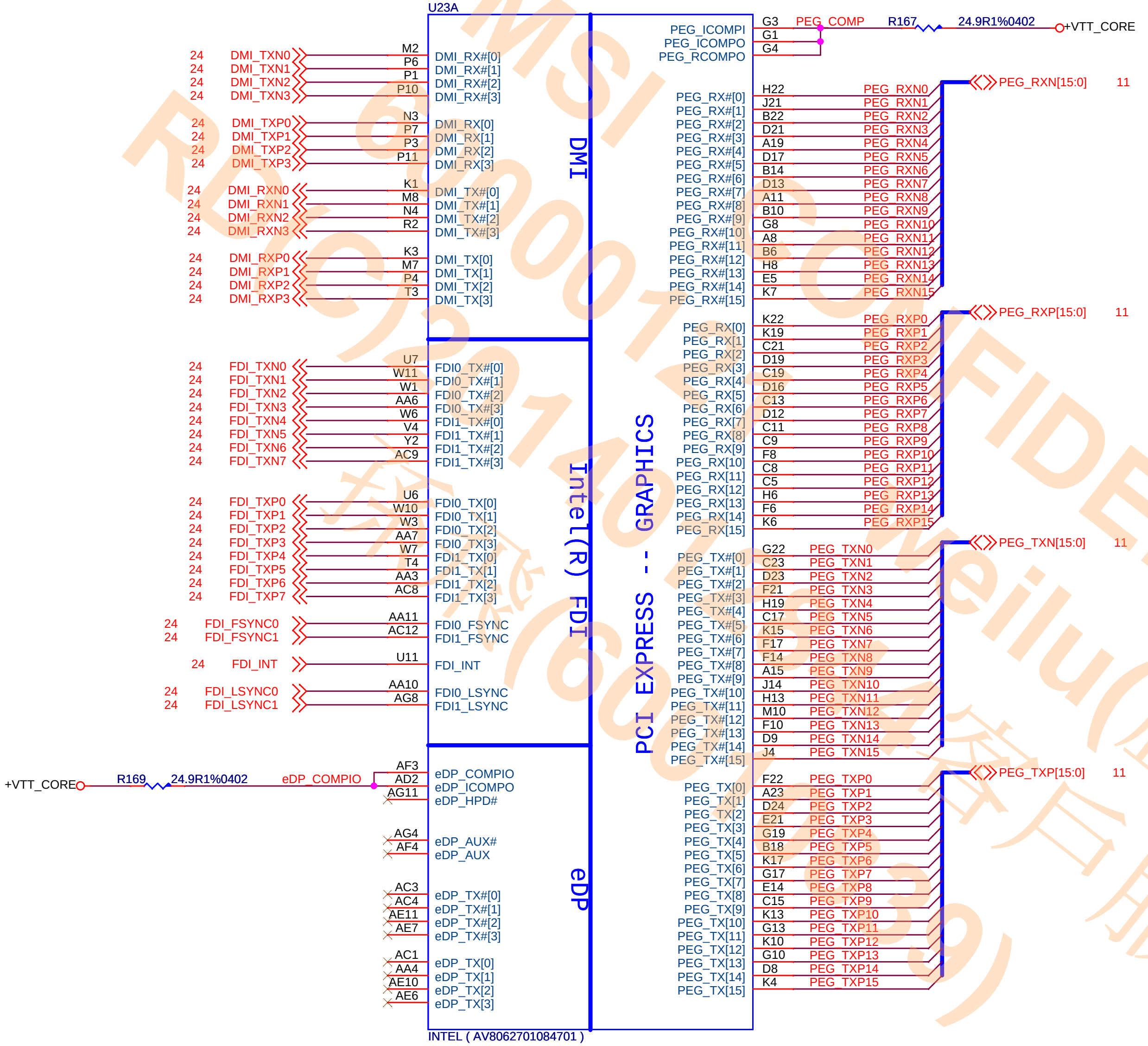
IVY BRIDGE PROCESSOR (HOST)



Title		
PROCESSOR-1 (HOST BUS)		
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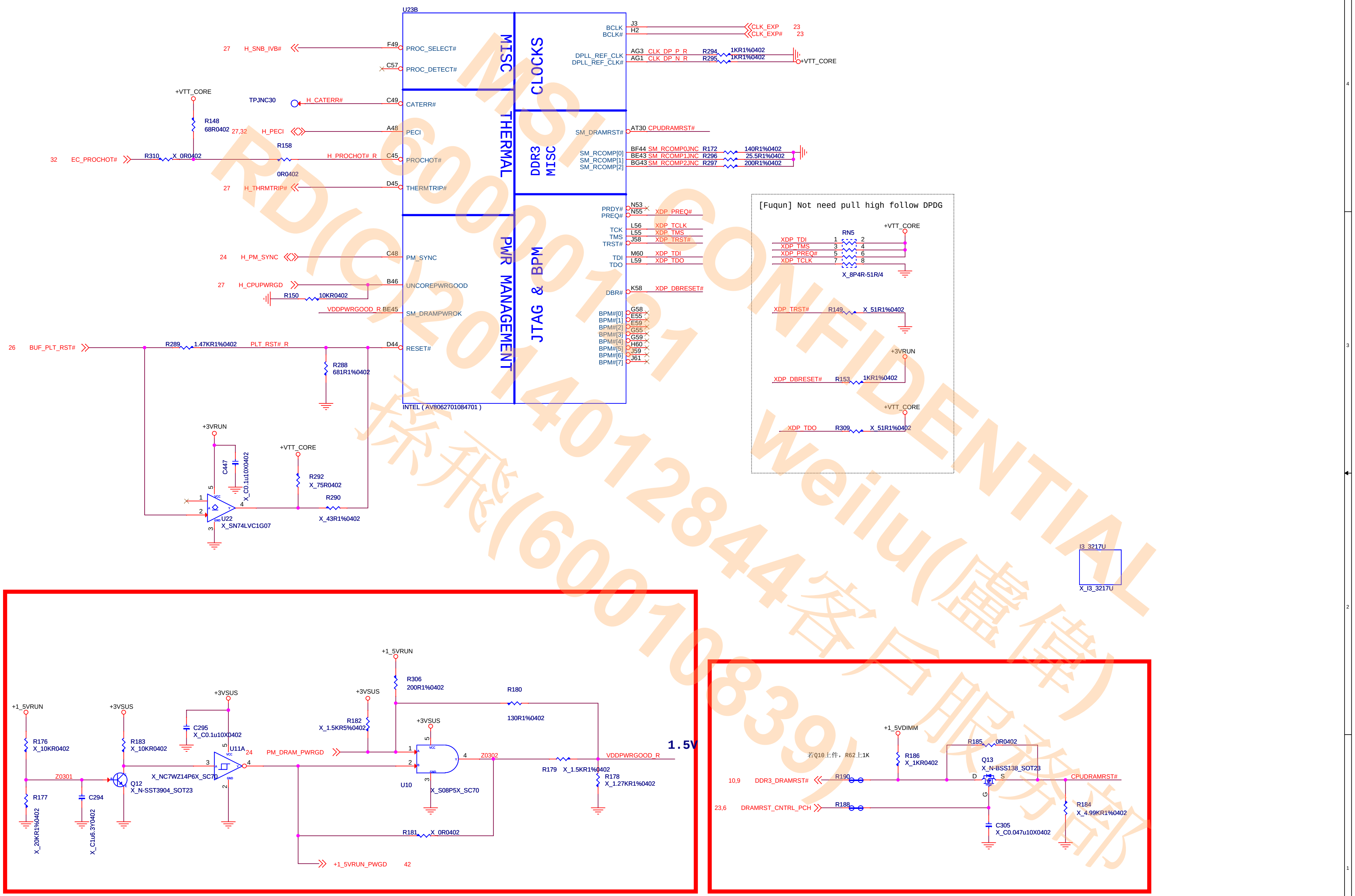
IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



Title: PROCESSOR-2 (MISC)

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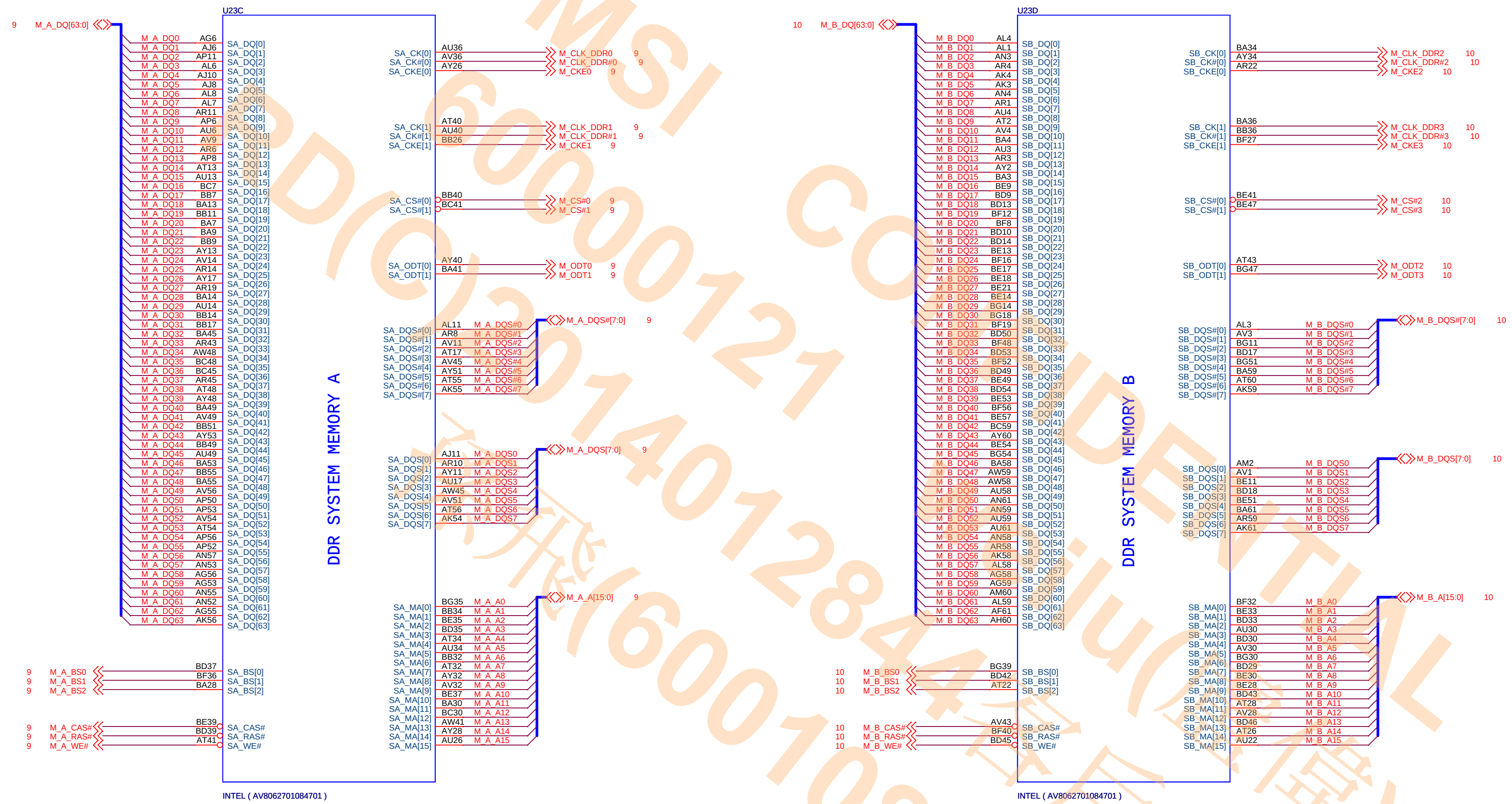
IVY BRIDGE PROCESSOR (DDR3)



Title	PROCESSOR-3 (DDR3)	
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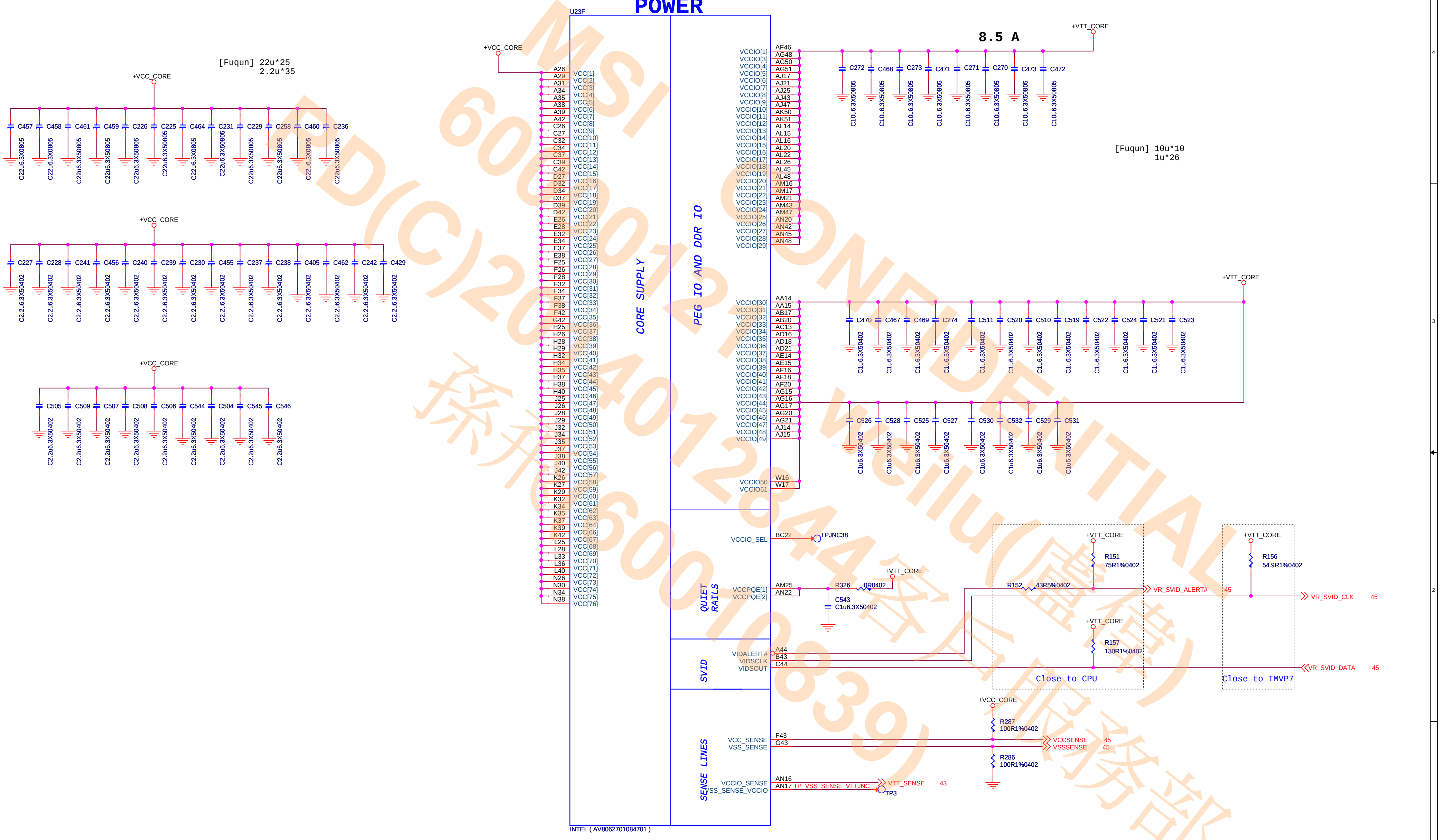
IVY BRIDGE PROCESSOR (POWER)

For SV CPU



Title: PROCESSOR-4 (POWER)

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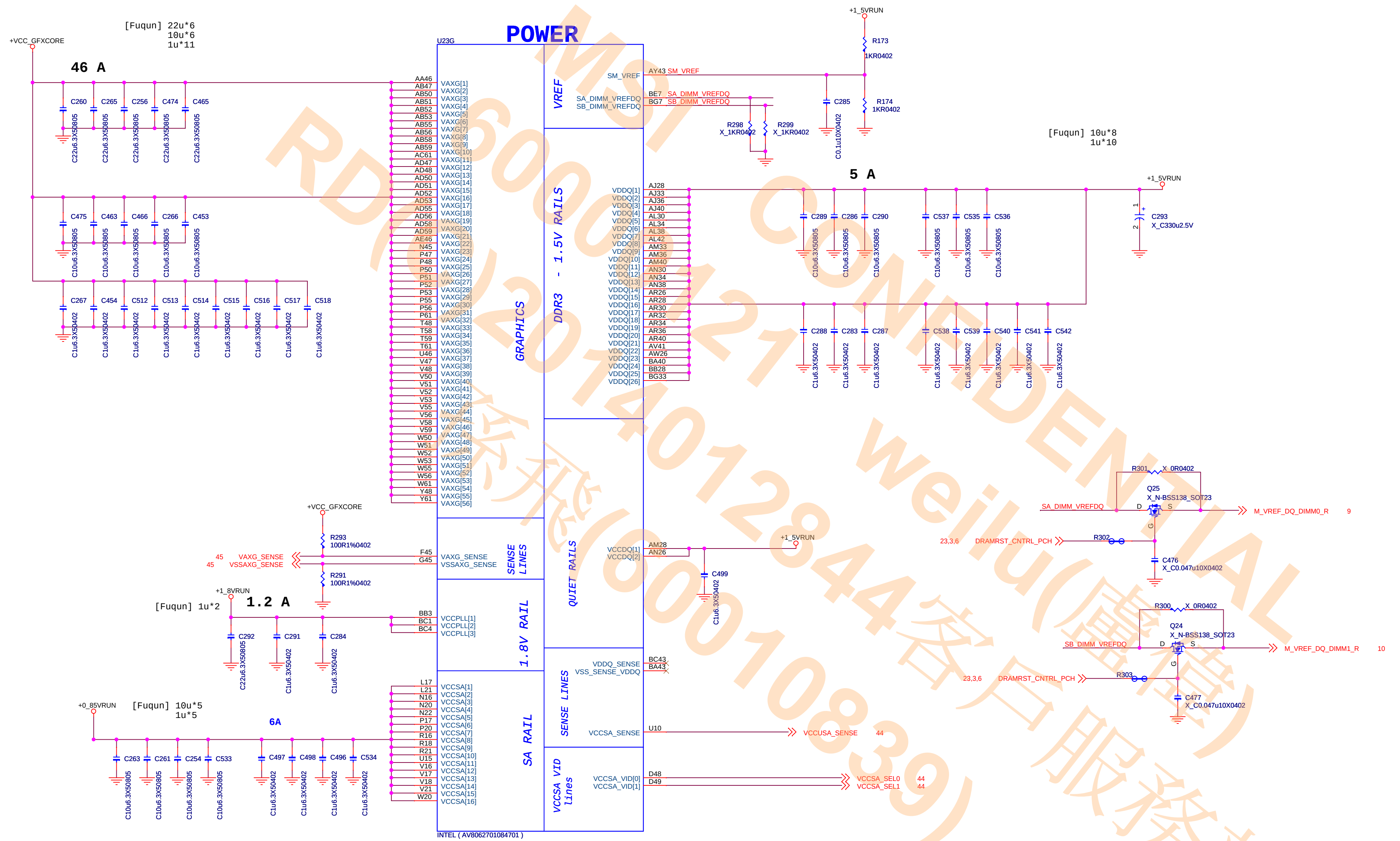
IVY BRIDGE PROCESSOR (GRAPHICS POWER)



Title
PROCESSOR-5 (GRAPHICS POWER)

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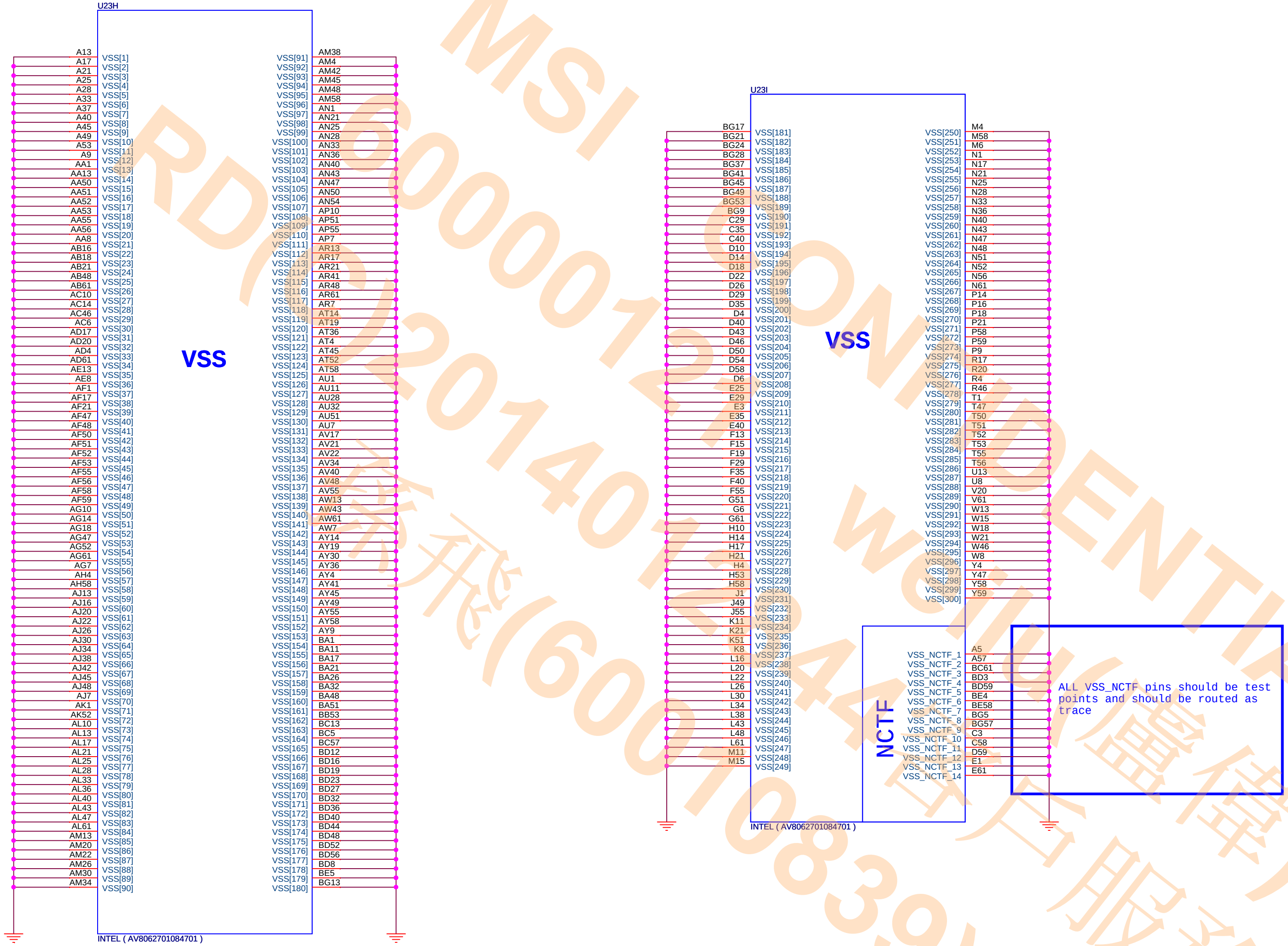
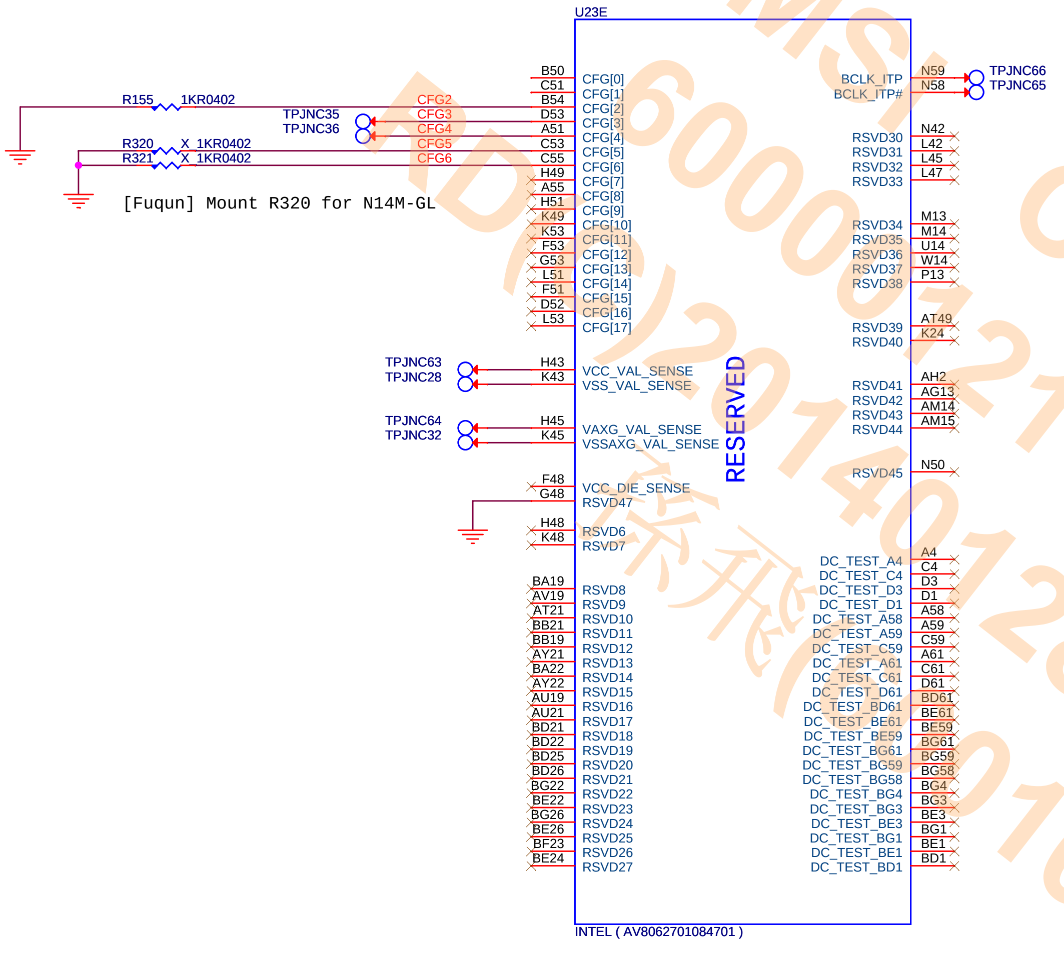
IVY BRIDGE PROCESSOR (GND)



IVY BRIDGE PROCESSOR (RESERVED)



CFG2 - PCI-Express Static Lane Reversal

CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (NC in DG) 0:Enabled; An external Display Port device is connected to the Embedded Display Port (Pull down to GND through a 1K Ω 5% resistor)

PCI-Express Configuration Select

CFG[5:6]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express (Default)

Title	PROCESSOR-7 (RESERVE)	
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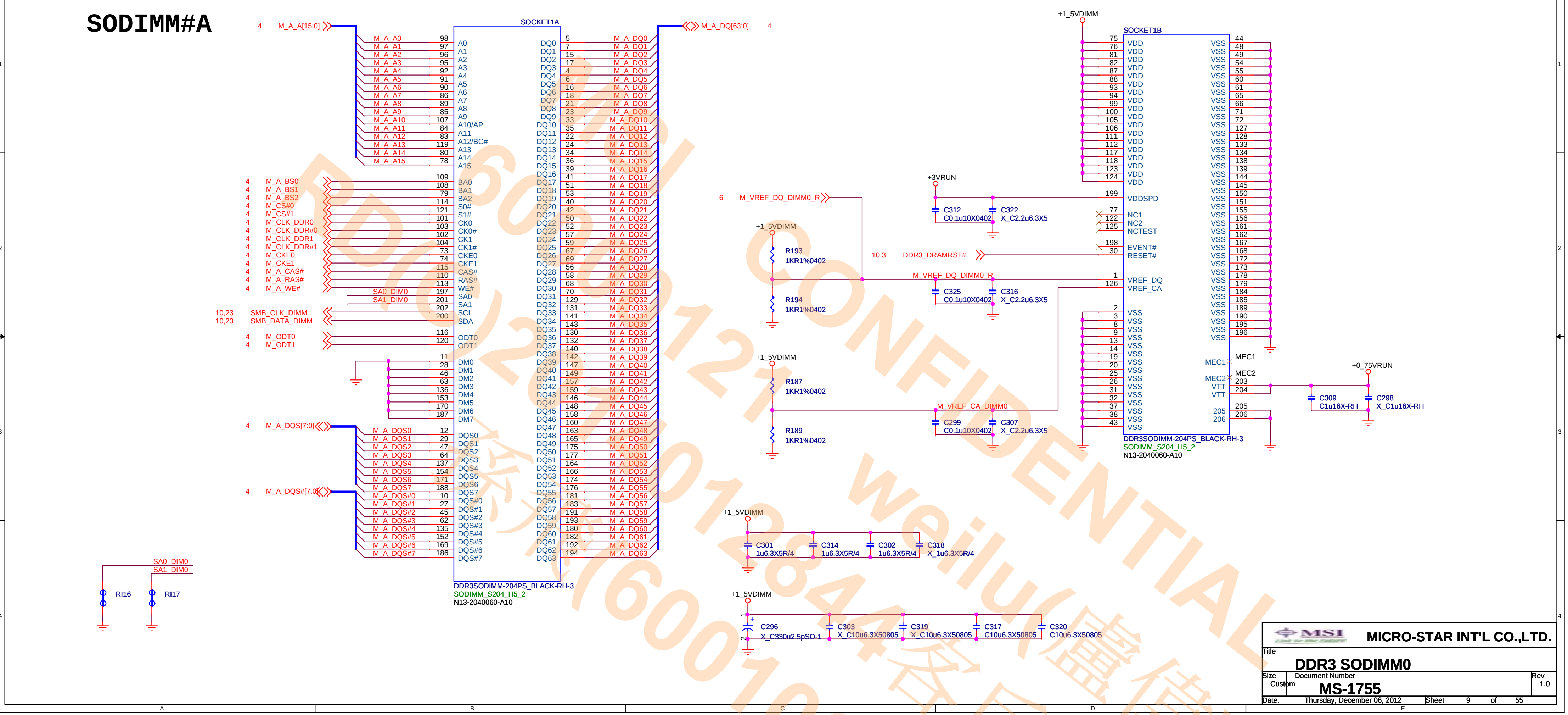
SODIMM#A



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Title	DDR3 SODIMM0	
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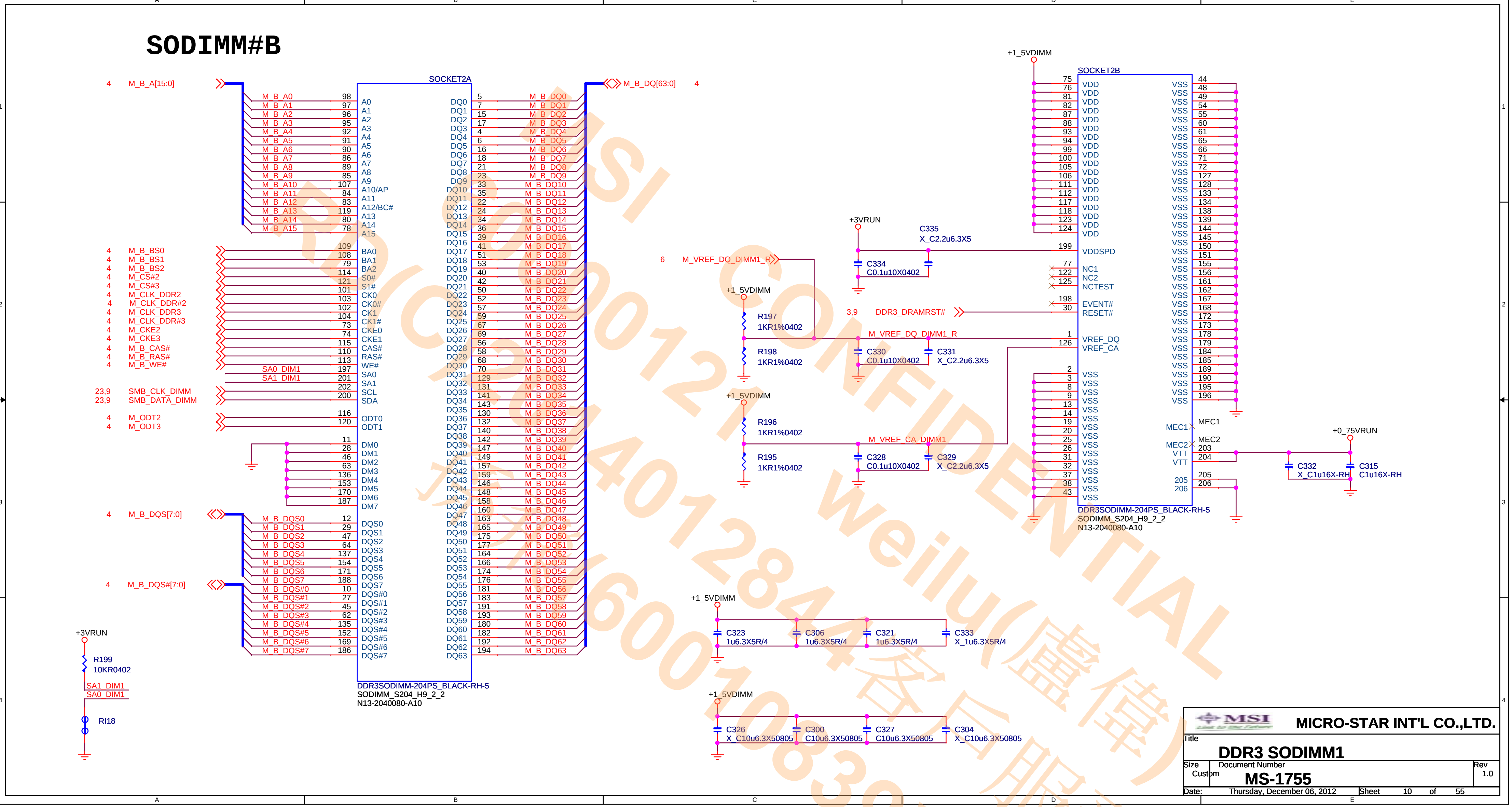
SODIMM#B



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Title	DDR3 SODIMM1	
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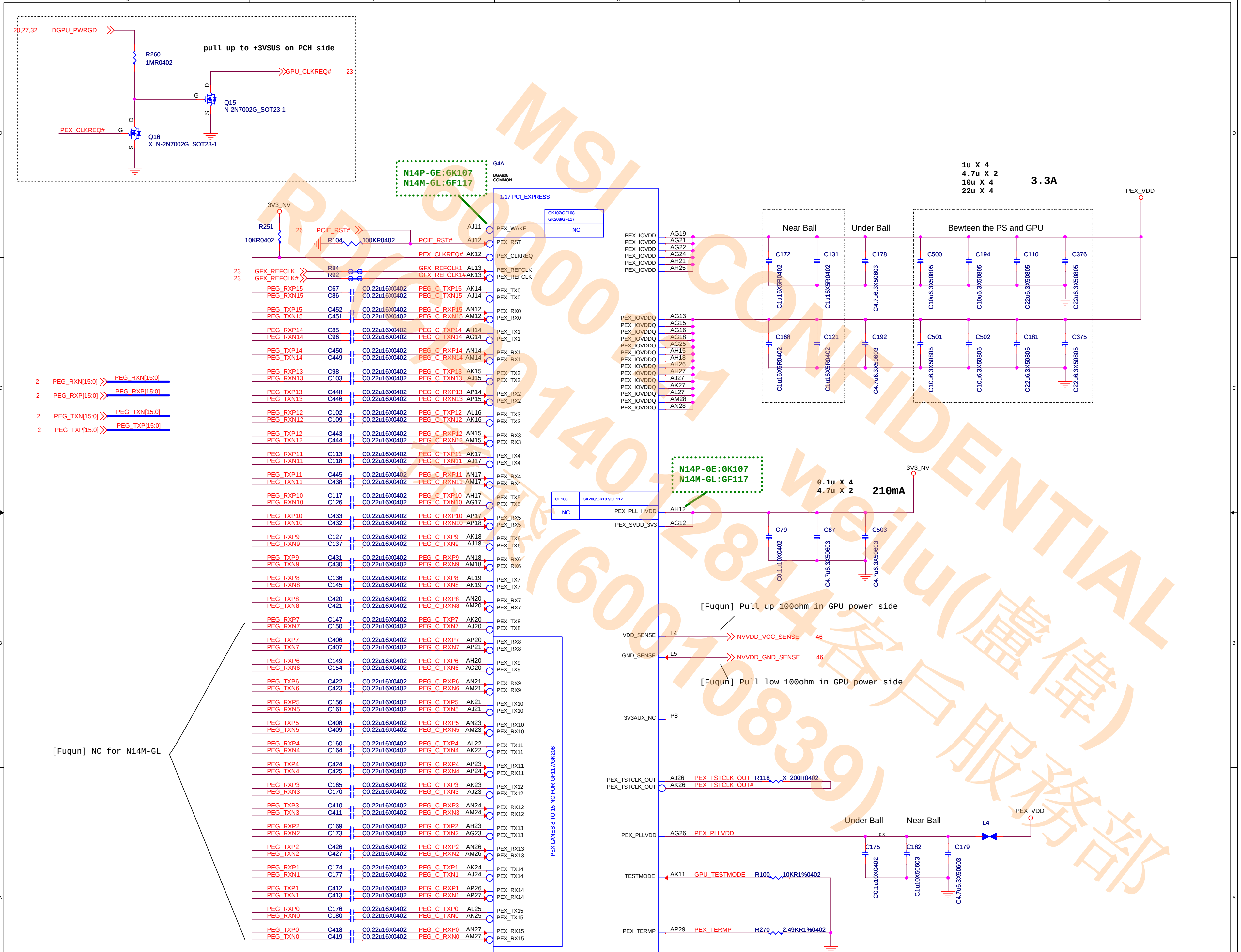

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Title	N13P-GS/GL_PCIE Host		
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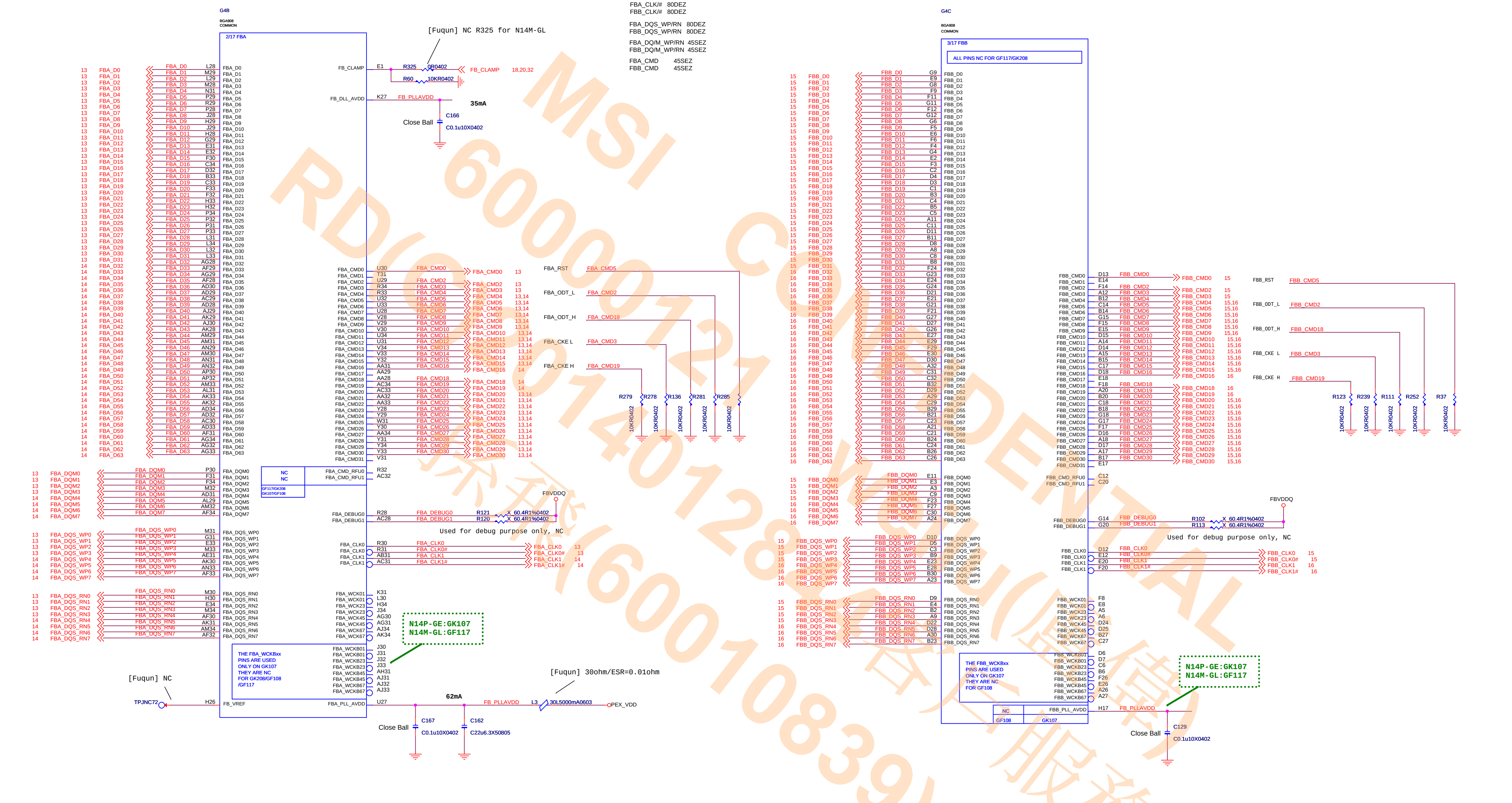
Frame Buffer Partitions A/B



MICRO-STAR INT'L CO.,LTD.			
Title	N13P-GS/GL_MEM Interface A/B		
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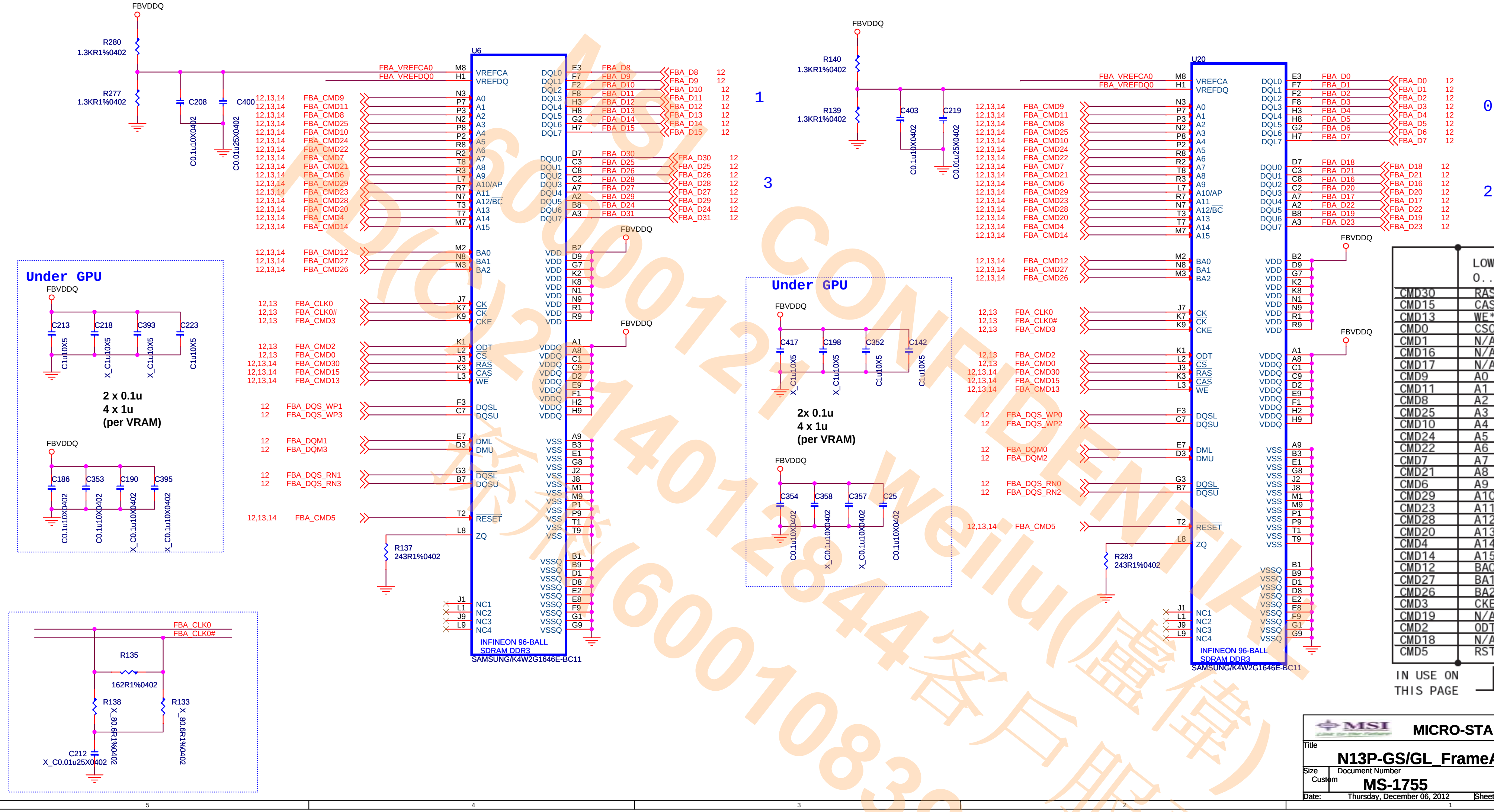
Memory Lower Partition A



	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

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Title: N13P-GS/GL_FrameA DDR3 I

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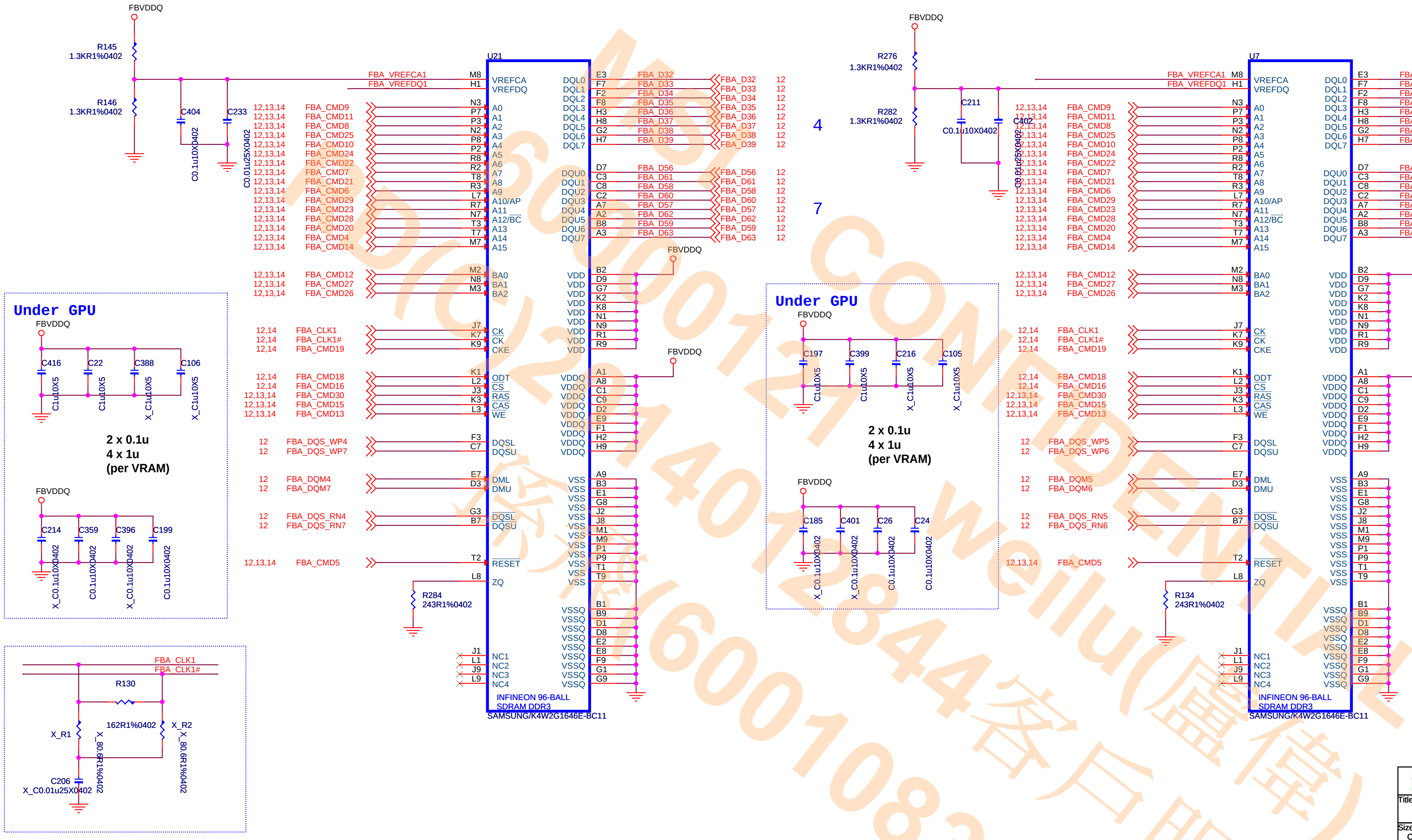
Memory Upper Partition A



	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

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MICRO-STAR INT'L CO.,LTD.

Title: N13P-GS/GL_FrameA DDR3 II

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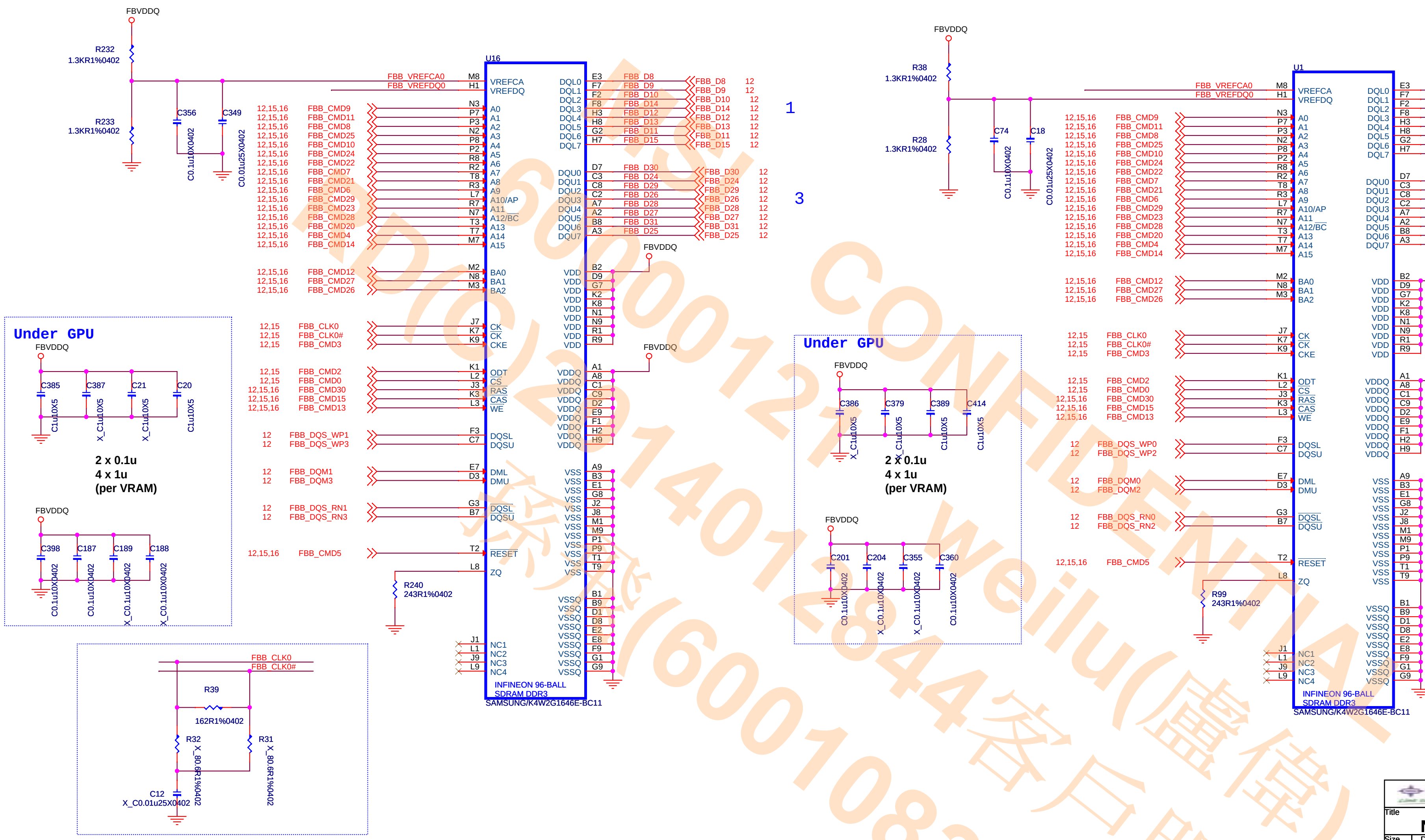
Memory Lower Partition B



	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

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MICRO-STAR INT'L CO.,LTD.

Title: N13P-GS/GL_FrameB DDR3 I

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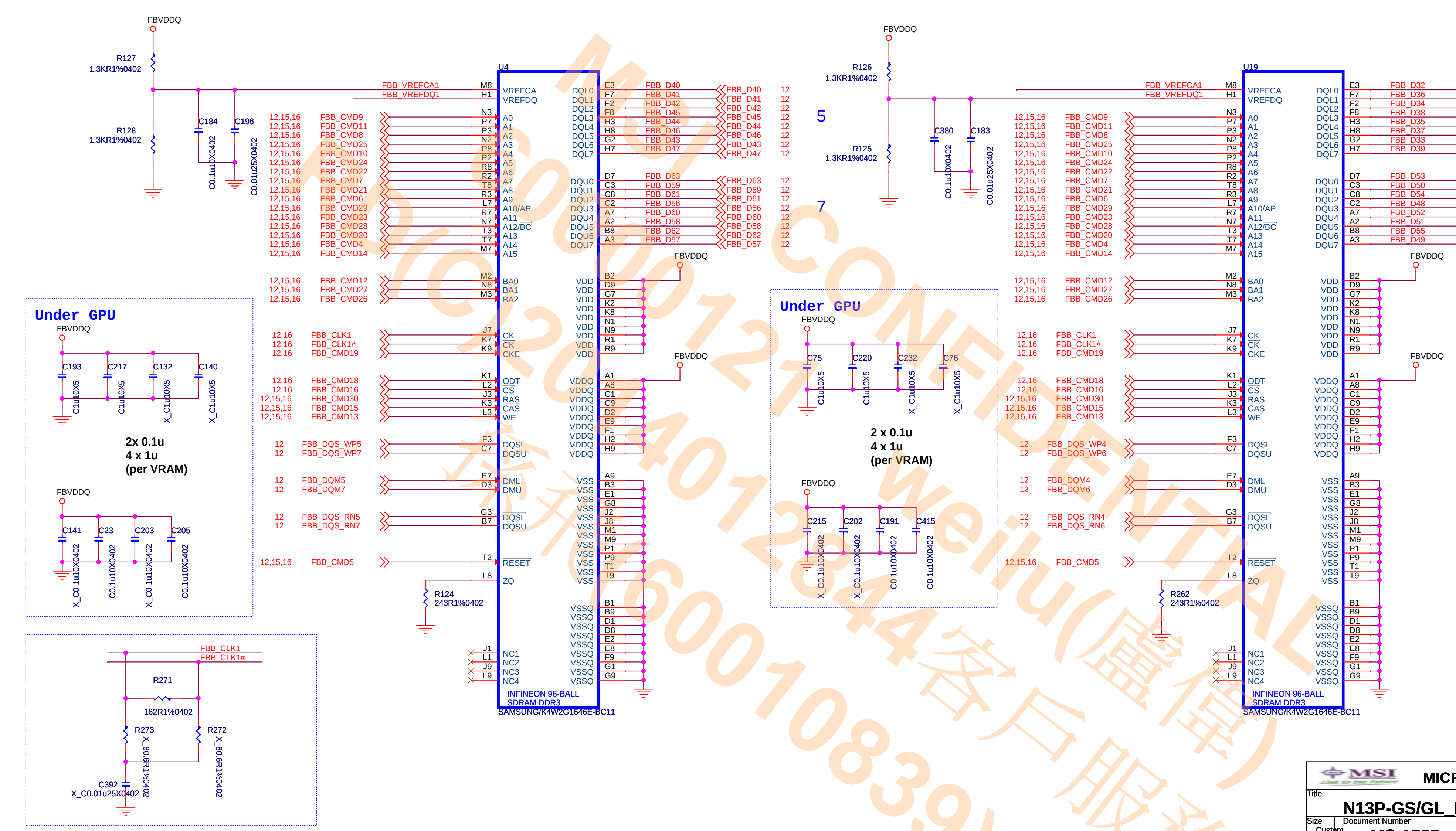
Memory Upper Partition B



	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

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Title: N13P-GS/GL_FrameB DDR3 II

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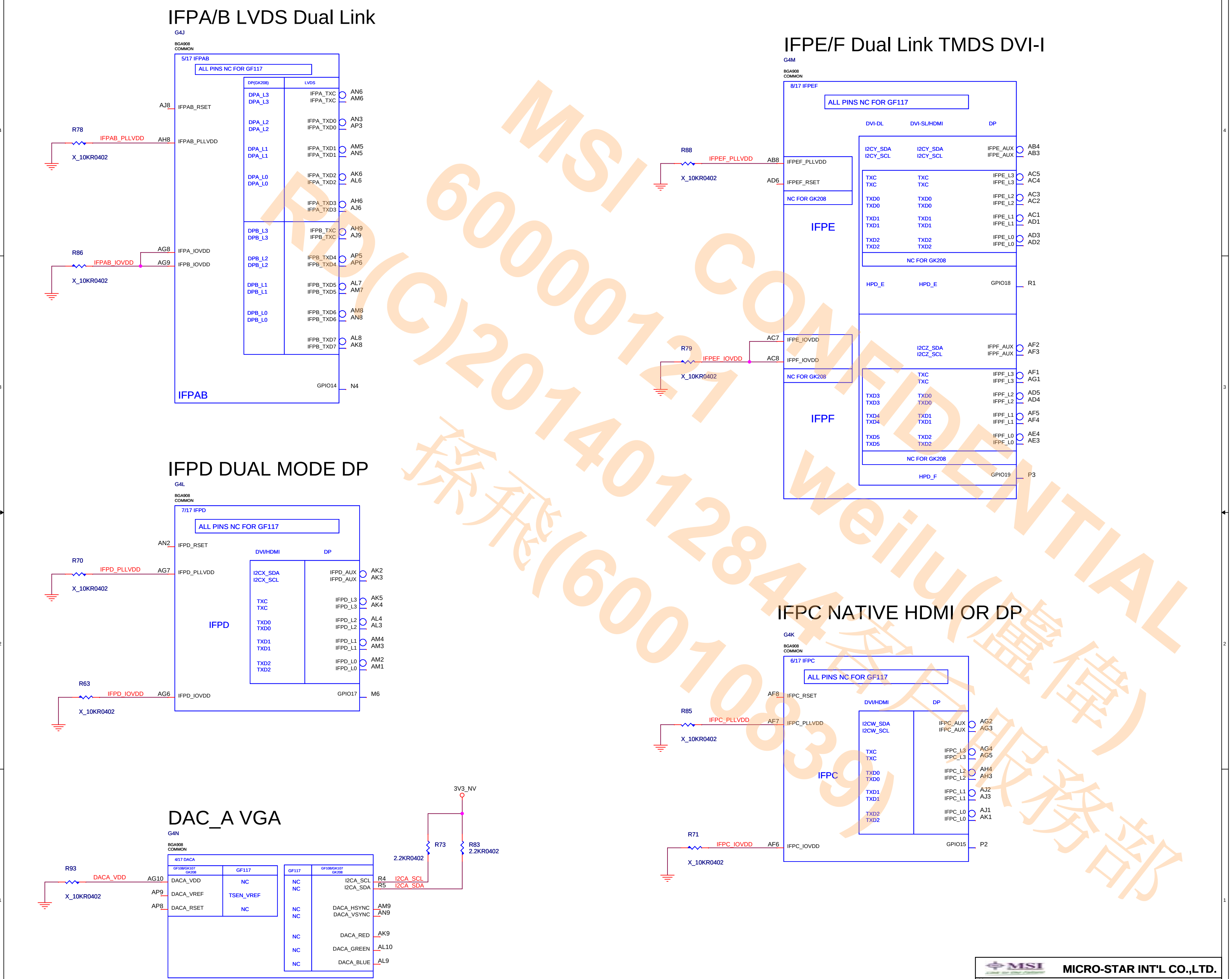

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Title: N13P-GS/GL_Display Interface

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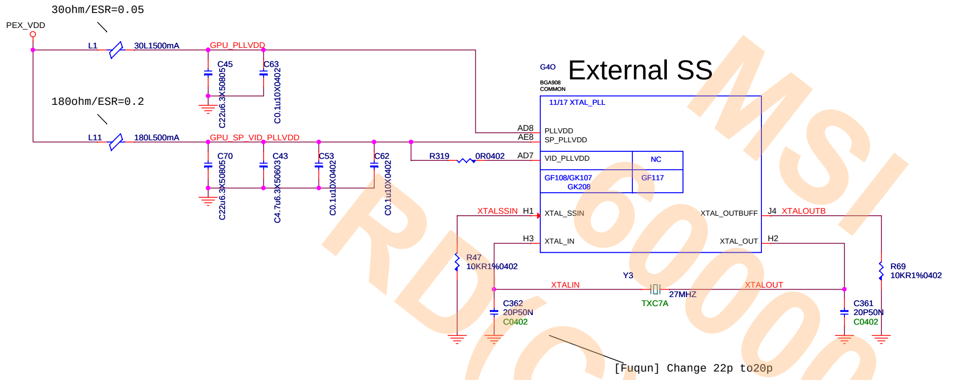
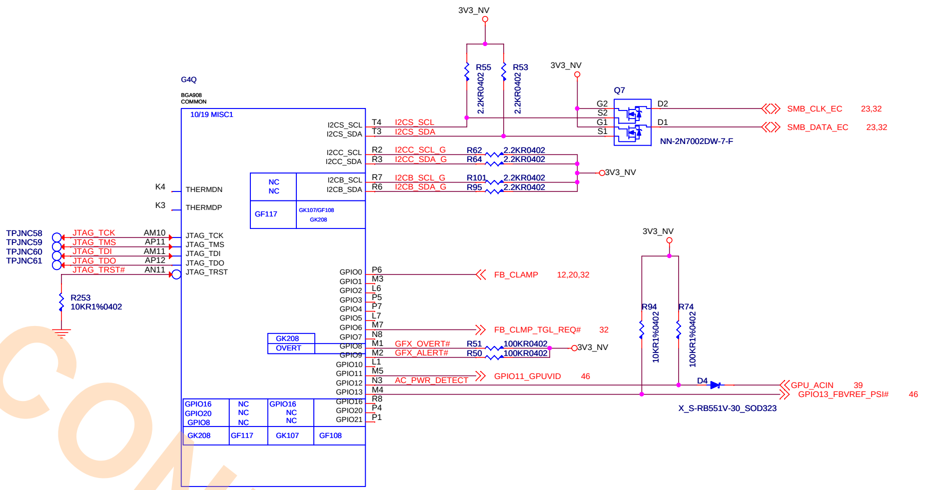
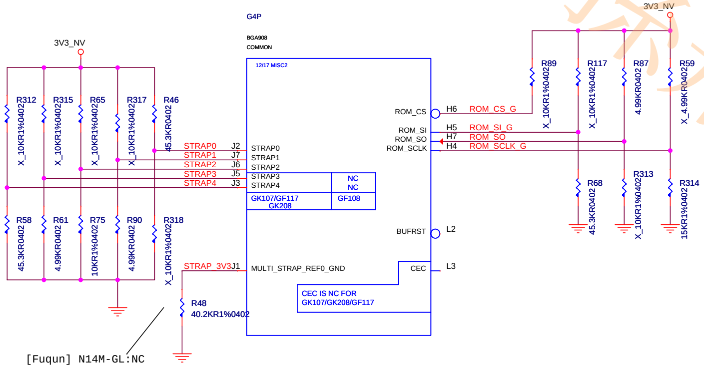




N14P-GE

Strap Pin	straping bit3	straping bit2	straping bit1	straping bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	0	0(Share SBIOS)	1	0(Default)
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
0111(0x7-Samsung)	0	1	1	1
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	1(Default)	0(Default)	0(Default)	0(Primary Display)
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
1111(EDID is used)	1	1	1	1
STRAP1	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
0000(Gen3)	0	0(Gen3)	0(Gen3)	0
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
0x0001(Device ID)	0	0	0	1
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	0	0	0	0
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	0	1(Enable Gen3)	1(Gen2/Gen3)	1(Default)

N14P-GE:GK107
N14M-GL:GF117

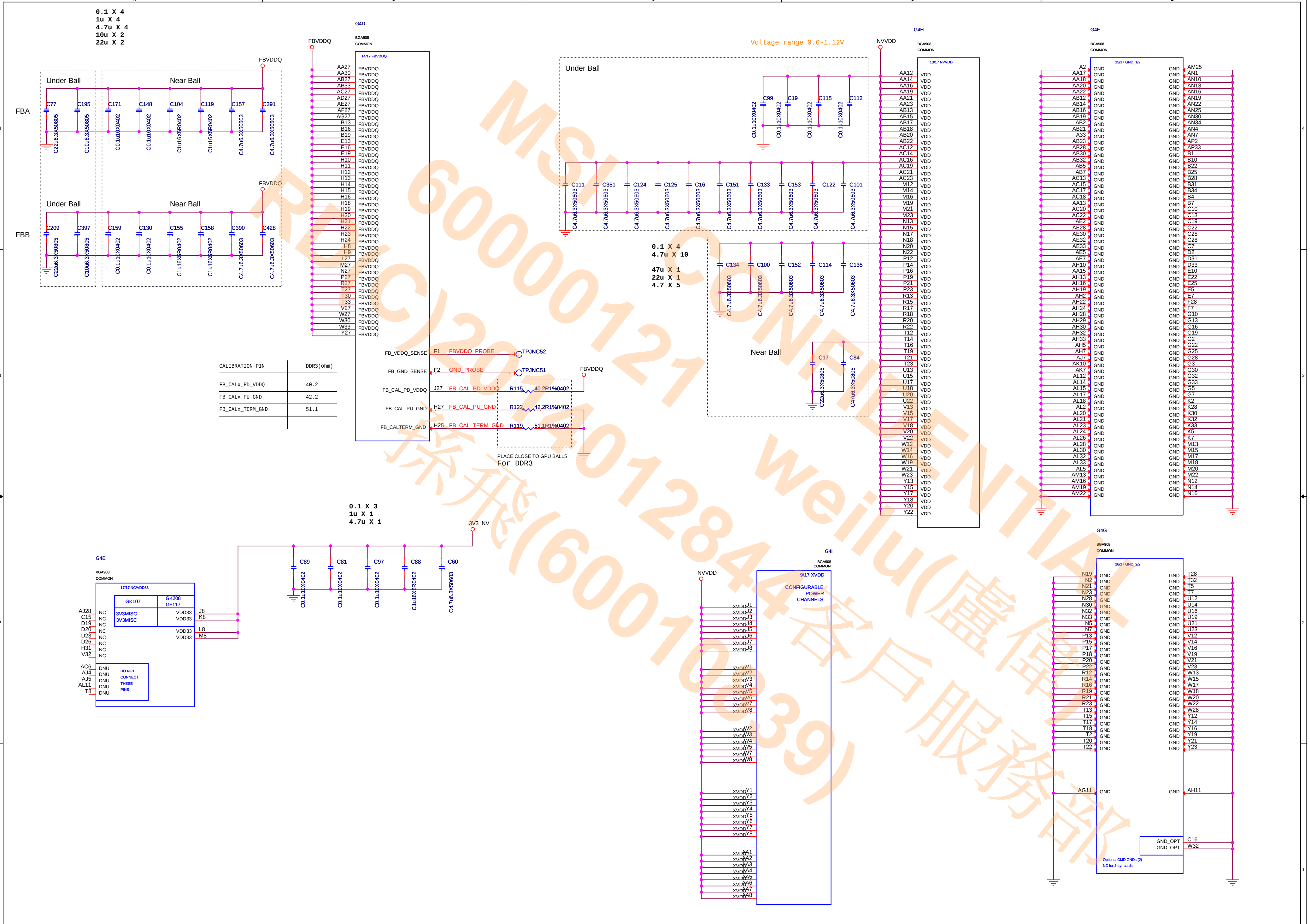


Rvalue	Pull up	Pull down
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

N14M-GL

ROM_SCLK	SMB_ALT_ADDR 0
ROM_SI	SUB_VENDER 0
ROM_SO	VGA-DEVICE 0
STRAP0	RAM_CFG[0] 1
STRAP1	RAM_CFG1] 0
STRAP2	RAM_CFG[2] 1
STRAP3	RAM_CFG[3] 0
STRAP4	PCIE_MAX_SPEED 0

Item	N14M-GL-B	N14P-GE-A2
Strap Mode	MULTISTRAP_REF_GND: NC	MULTISTRAP_REF_GND, 40.2k PD to GND
Device ID	0x1140	0x0FE1
Package	GB4-128	GB4-128
Memory type	sDDR3	SDDR3
ROM_SI	10kohm Pull Down	0x6, Hynix 2G, 35kohm PD
		0x7, Samsung 2G, 45kohm PD
ROM_SO	10kohm Pull Down	0x8, 5kohm pull high
ROM_SCLK	10kohm pull down	0x0010, 15Kohm pull down
Strap0	Strap3,2,1,0: RAM_CFG[3:0]	45kohm pull up
Strap1	[0101], Samsung2G	5kohm pull down
Strap2	[0110], Hynix2G	Device_ID, 0x1_0x0001_PD 10kohm
Strap3	("0", 10k PD; "1", 10k PU to 3V3)	0x0 for Optimus, 5kohm pull down
Strap4	10kohm pull down	0x0111, 45kohm pull down
OpenVR	Config C	Config B
NVVDD Boot Voltage	0.9V	0.9V



CALIBRATION PIN	DDR3(ohm)
FB_CALx_PD_VDDQ	40.2
FB_CALx_PU_GND	42.2
FB_CALx_TERM_GND	51.1

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Title	N13P-GS/GL Power & GND
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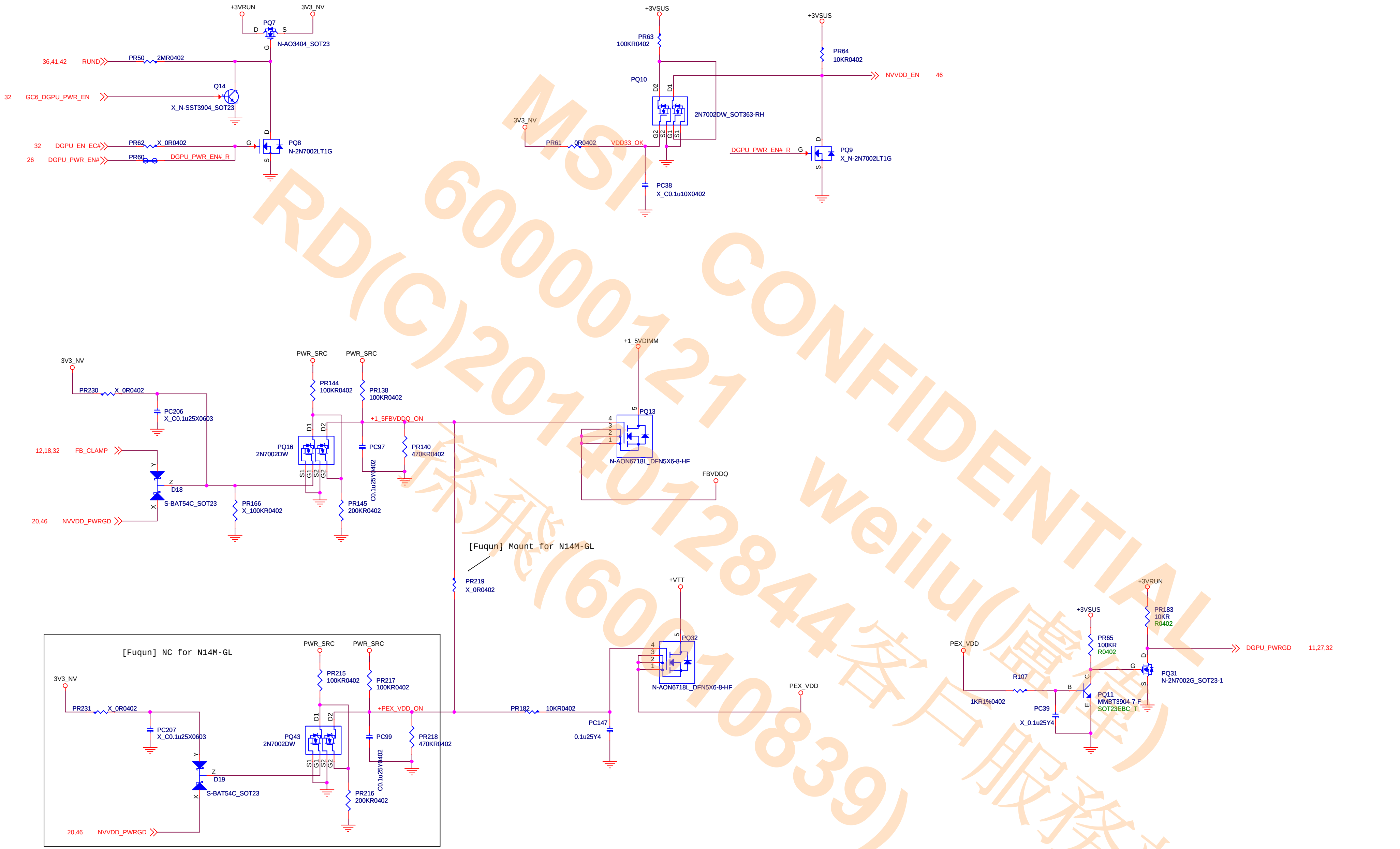

MICRO-STAR INT'L CO.,LTD.

Title: N13P-GS/GL Power & GND

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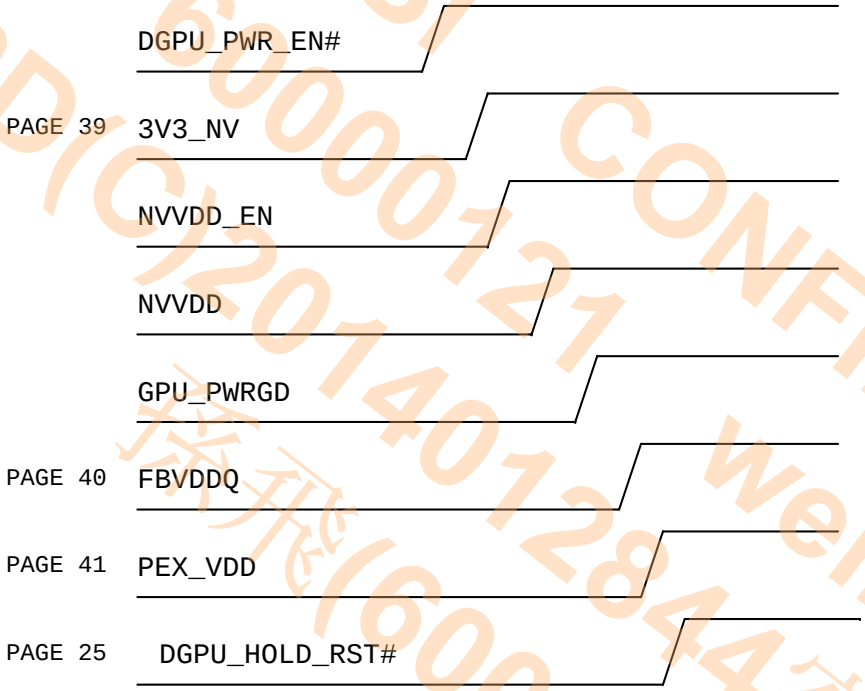

GPU Power Sequence

[Fuuqn] The total time of all power on should be within 6ms

[Fuuqn] The total time of all power off should be within 10ms

MSI MICRO-STAR INTERNATIONAL Link to the Future	MICRO-STAR INT'L CO.,LTD.	
Title: N13P-GS_Power Sequence		
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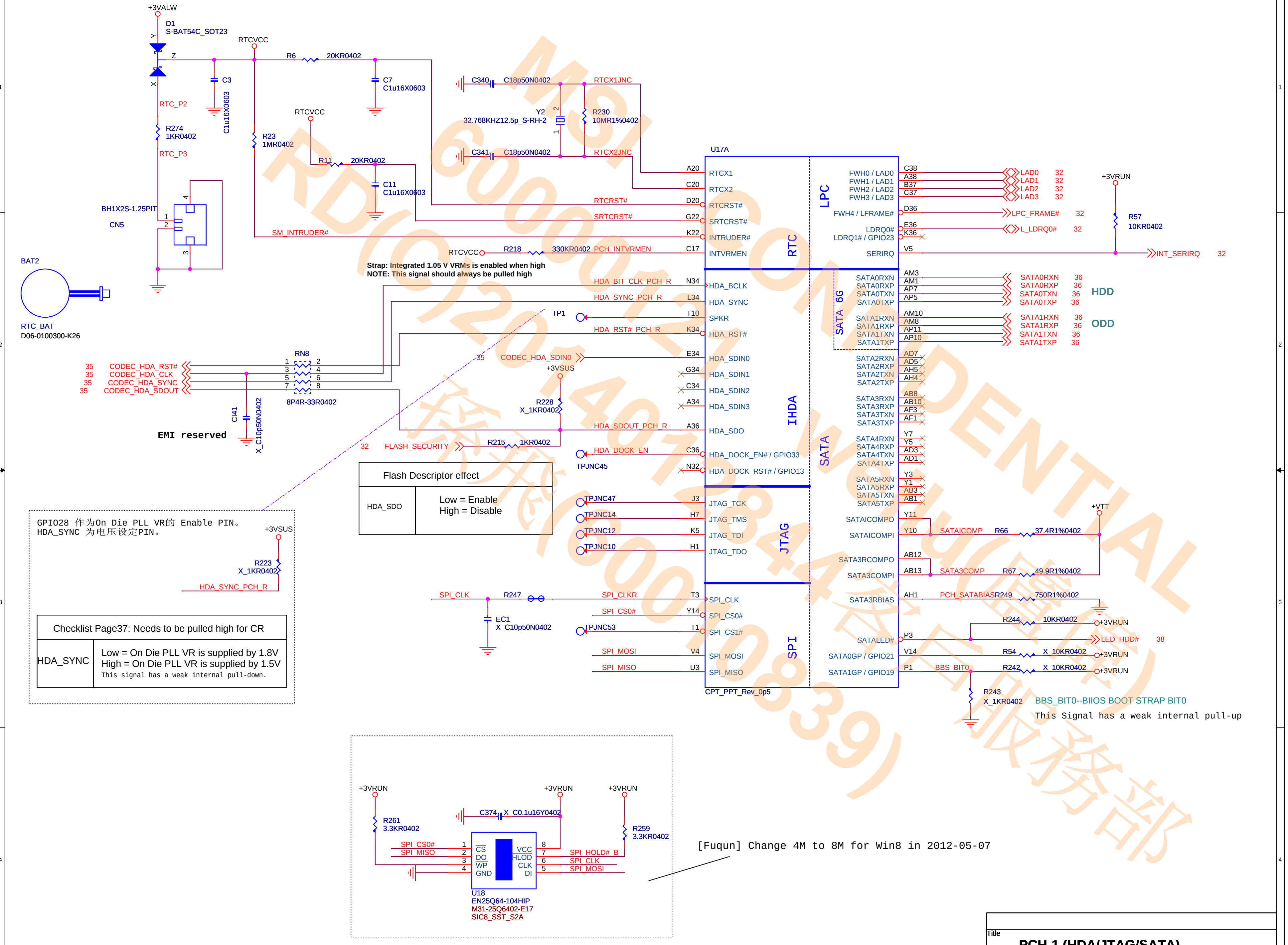
PANTHER POINT (HDA,JTAG,SATA)



Flash Descriptor effect	
HDA_SDO	Low = Enable High = Disable

Checklist Page37: Needs to be pulled high for CR	
HDA_SYNC	Low = On Die PLL VR is supplied by 1.8V High = On Die PLL VR is supplied by 1.5V This signal has a weak internal pull-down.

Title	PCH-1 (HDA/JTAG/SATA)	
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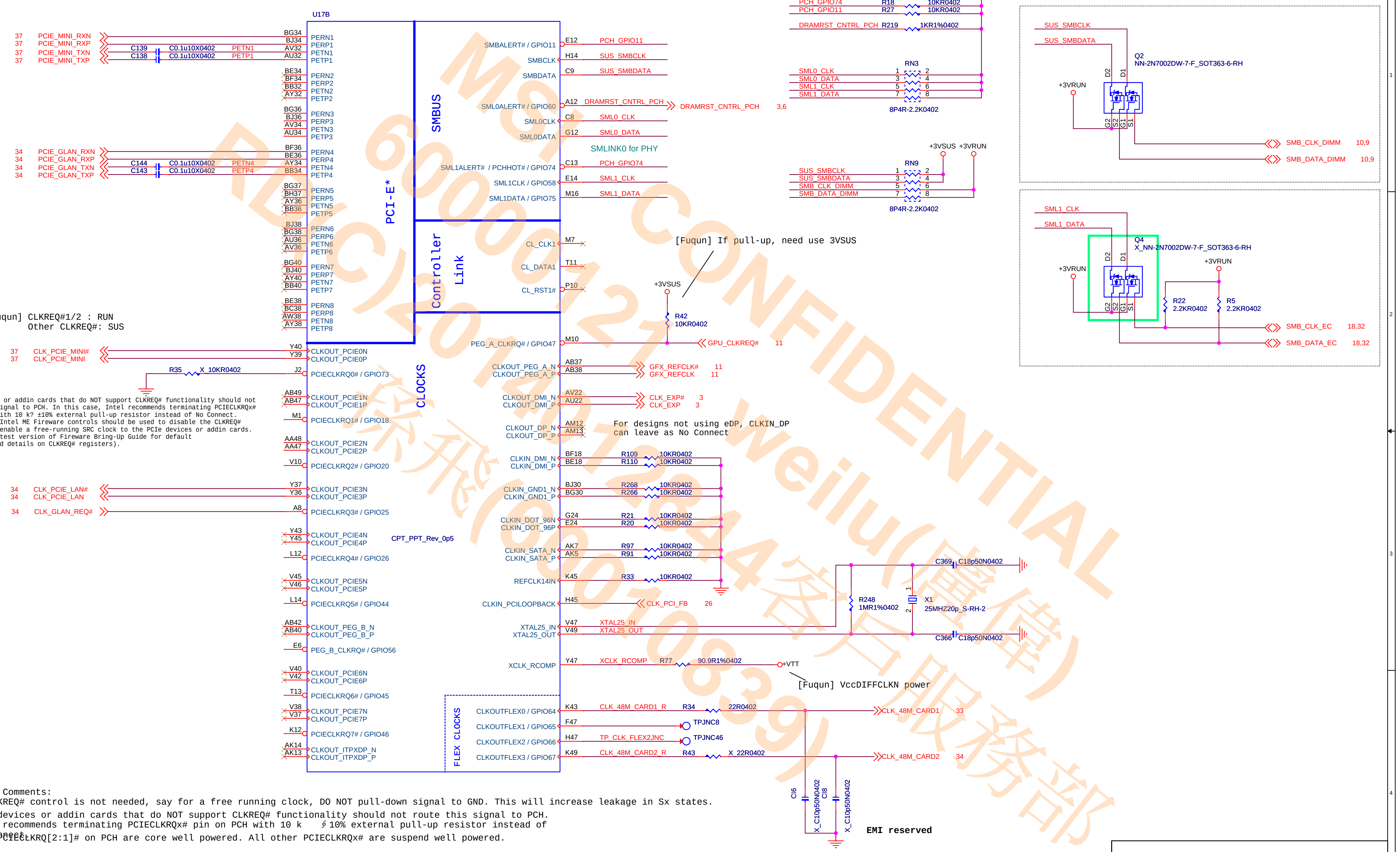
PANTHER POINT (PCI-E,SMBUS,CLK)



PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH. In this case, Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k? ±10% external pull-up resistor instead of No Connect. Appropriate Intel ME Fireware controls should be used to disable the CLKREQ# feature and enable a free-running SRC clock to the PCIe devices or addin cards. (Refer to latest version of Fireware Bring-Up Guide for default settings and details on CLKREQ# registers).

Intel Comments:
If CLKREQ# control is not needed, say for a free running clock, DO NOT pull-down signal to GND. This will increase leakage in Sx states.
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k ∲10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

Title	PCH-2 (PCI-E/SMBUS/CLK)	
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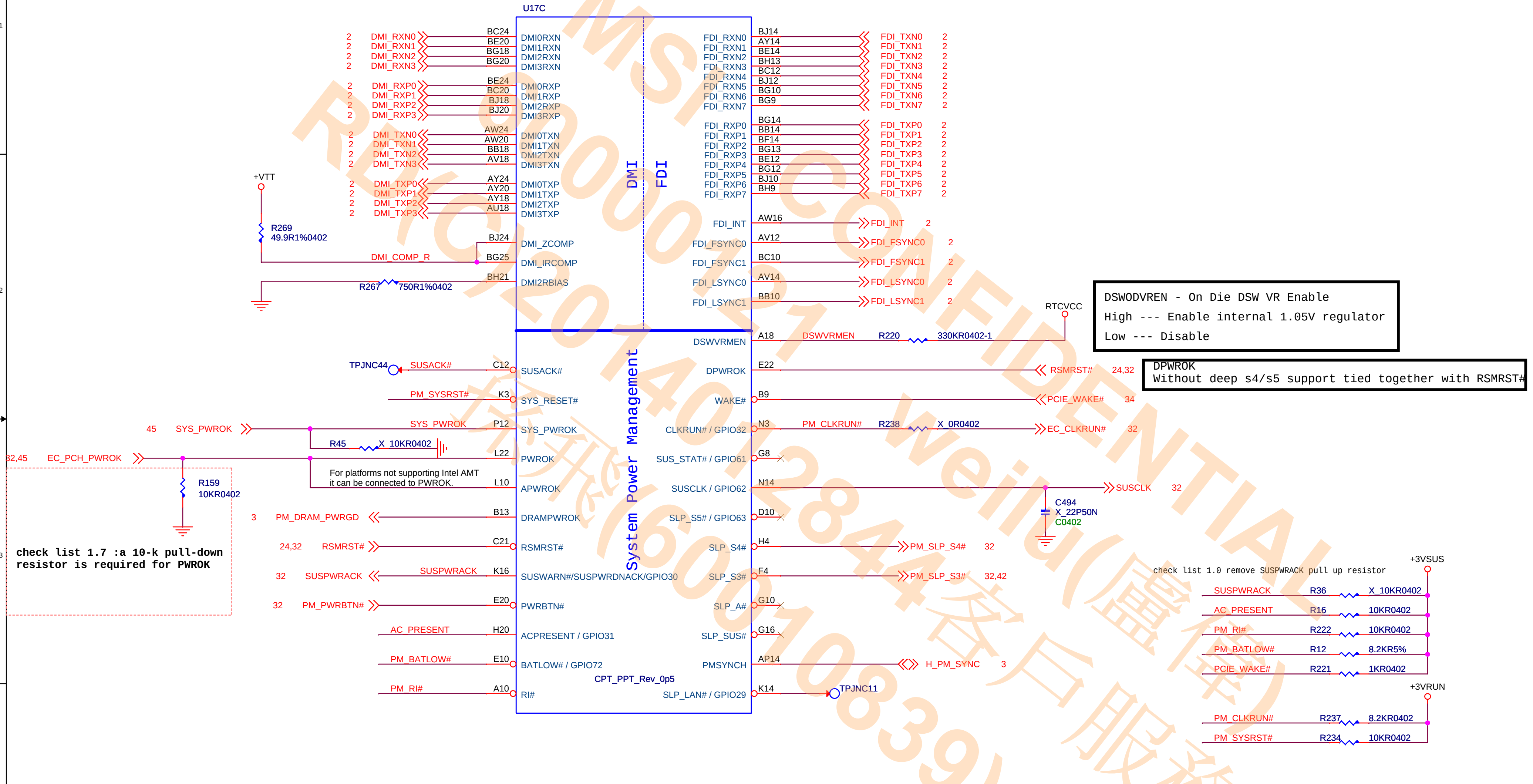
PANTHER POINT (DMI,FDI,GPIO)



Title	PCH-3 (DMI/FDI/GPIO)
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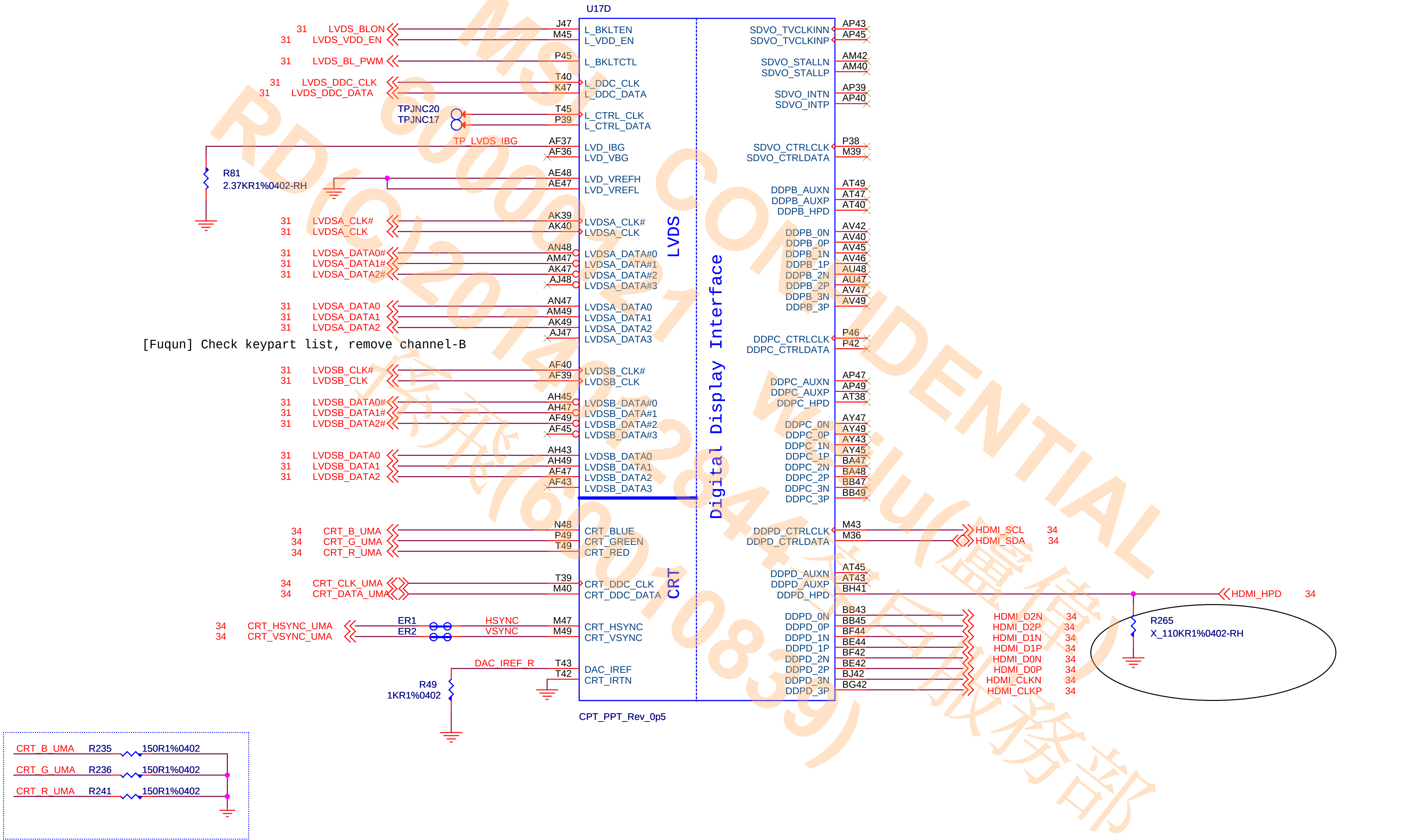
PANTHER POINT (LVDS,DDI)



Title	PCH-4 (LVDS/DDI)
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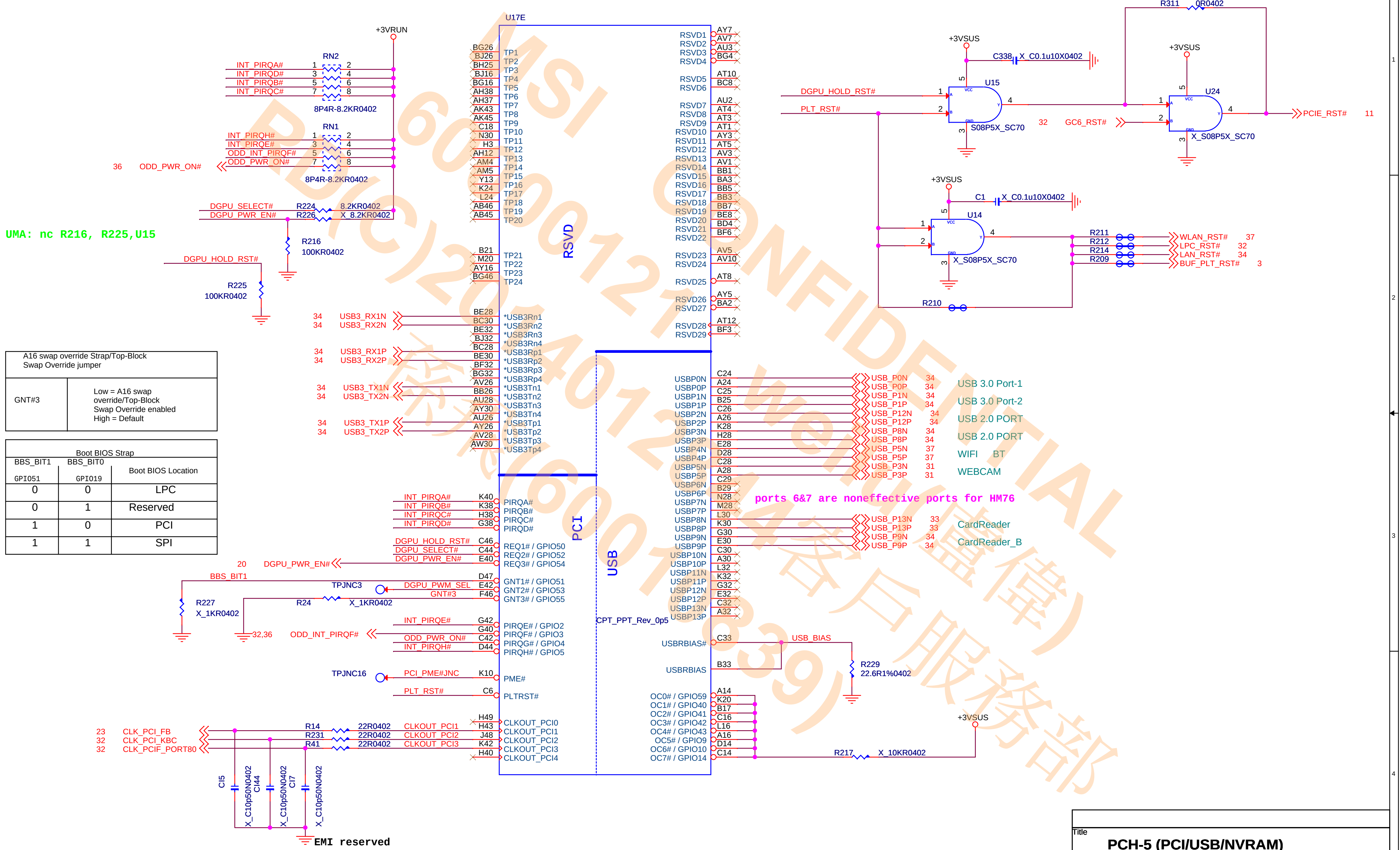
PANTHER POINT (PCI,USB,NVRAM)



A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap

BBS_BIT1 GPIO51	BBS_BIT0 GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

Title	PCH-5 (PCI/USB/NVRAM)
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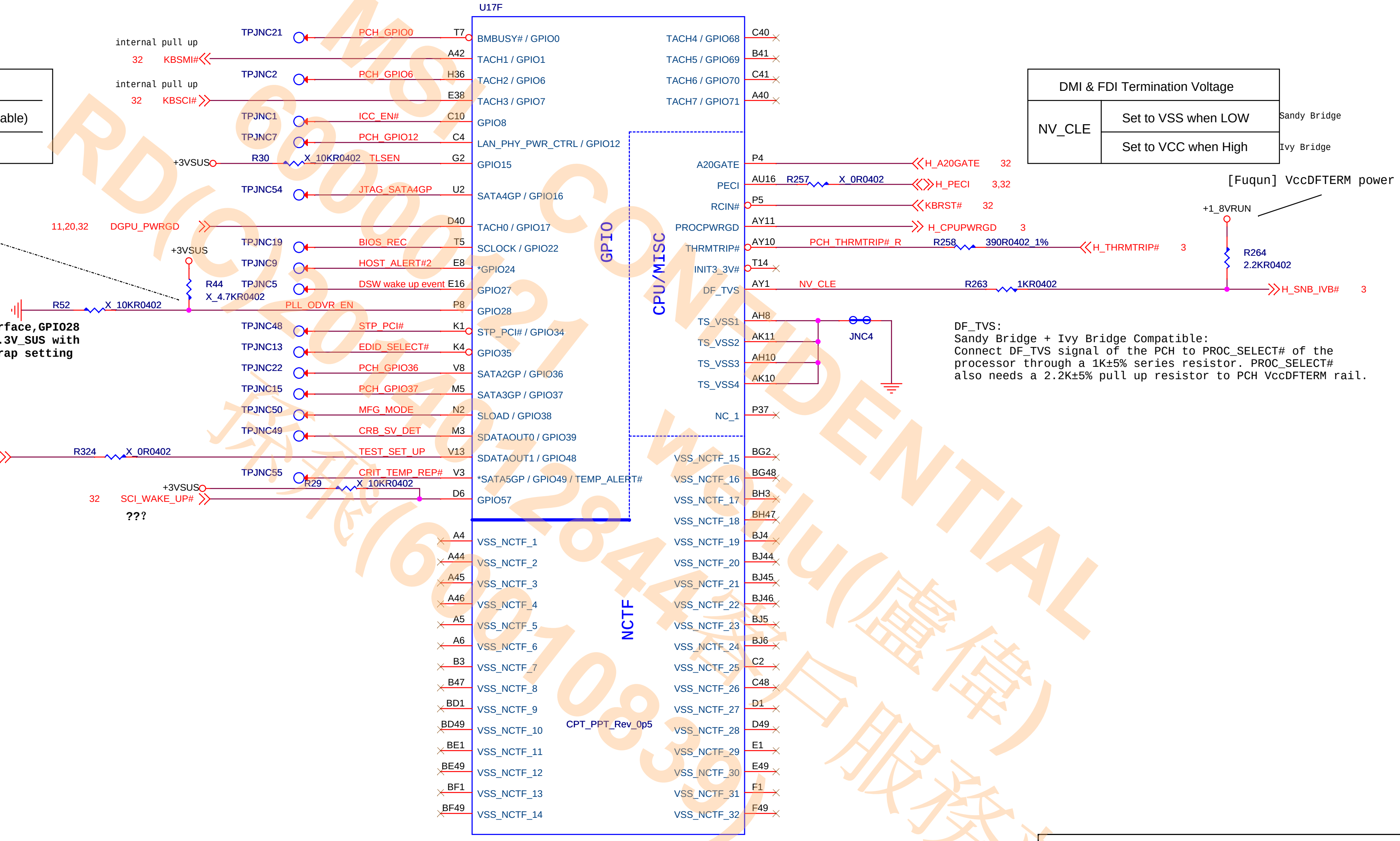
PANTHER POINT (GPIO,VSS_NCTF,RSVD)



PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

when use as the chipset test interface,GPIO28 signal needs to be pulled up to 3.3V_SUS with 4.7K resistor to ensure proper strap setting

DMI & FDI Termination Voltage		
NV_CLE	Set to VSS when LOW	Sandy Bridge
	Set to VCC when High	Ivy Bridge

[Fuqun] VccDFTERM power

DF_TVS:
Sandy Bridge + Ivy Bridge Compatible:
Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTERM rail.

Title	PCH-6 (GPIO/NCTF/RSVD)	
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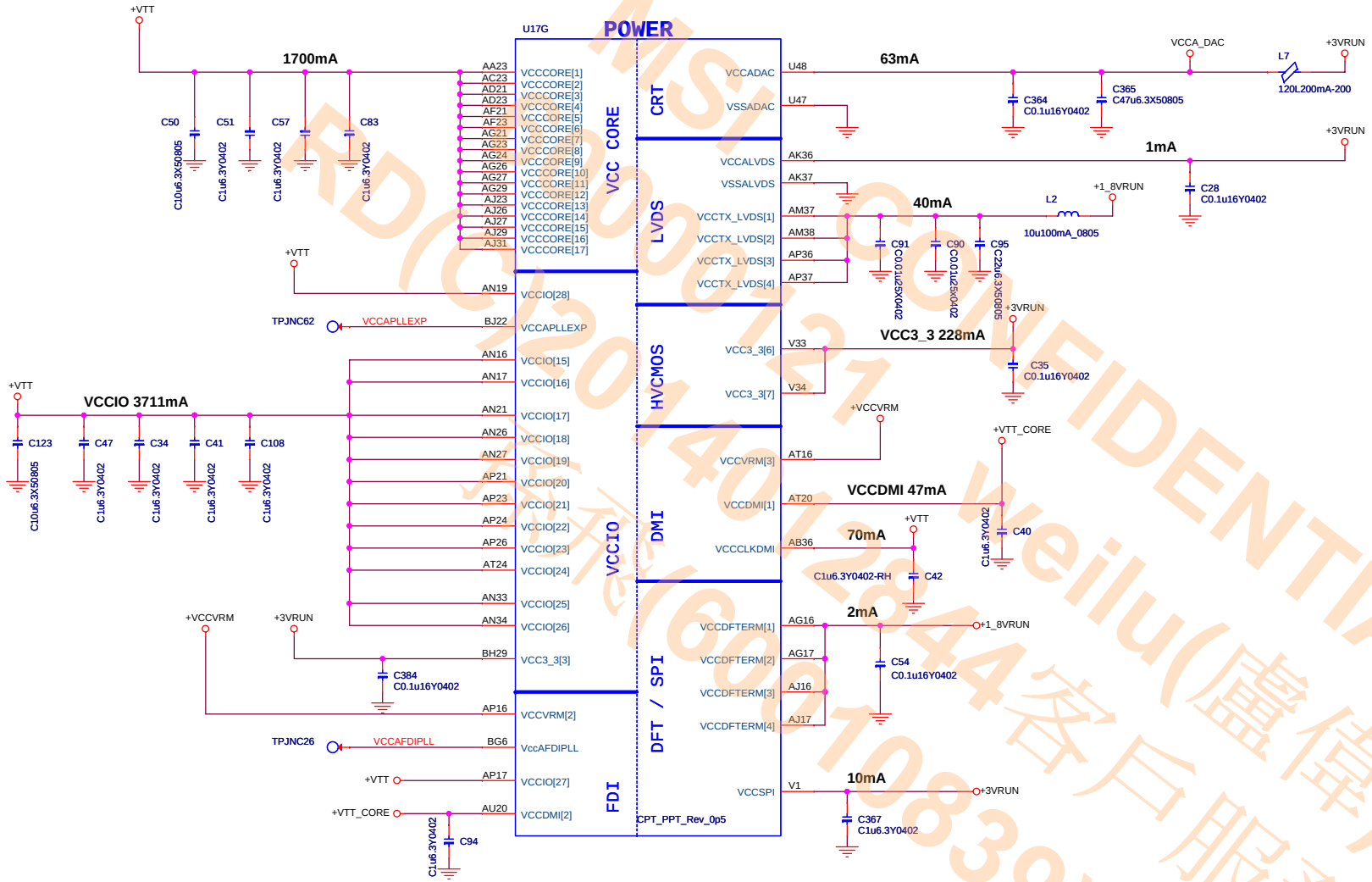
PANTHER POINT (POWER)



GPIO28 作为On Die PLL VR的 Enable PIN。
HDA_SYNC 为电压设定PIN。

Checklist Page37: Needs to be pulled high for CR	
HDA_SYNC	Low = On Die PLL VR is supplied by 1.8V High = On Die PLL VR is supplied by 1.5V This signal has a weak internal pull-down.

The VCCVRM rail (1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VccAPLLEXP, VccaPLLDMI2, and VccAPLLSATA). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO28,

Title	PCH-7 (POWER)		
Size: Custom	Document Number: MS-1755		Rev: 1.0
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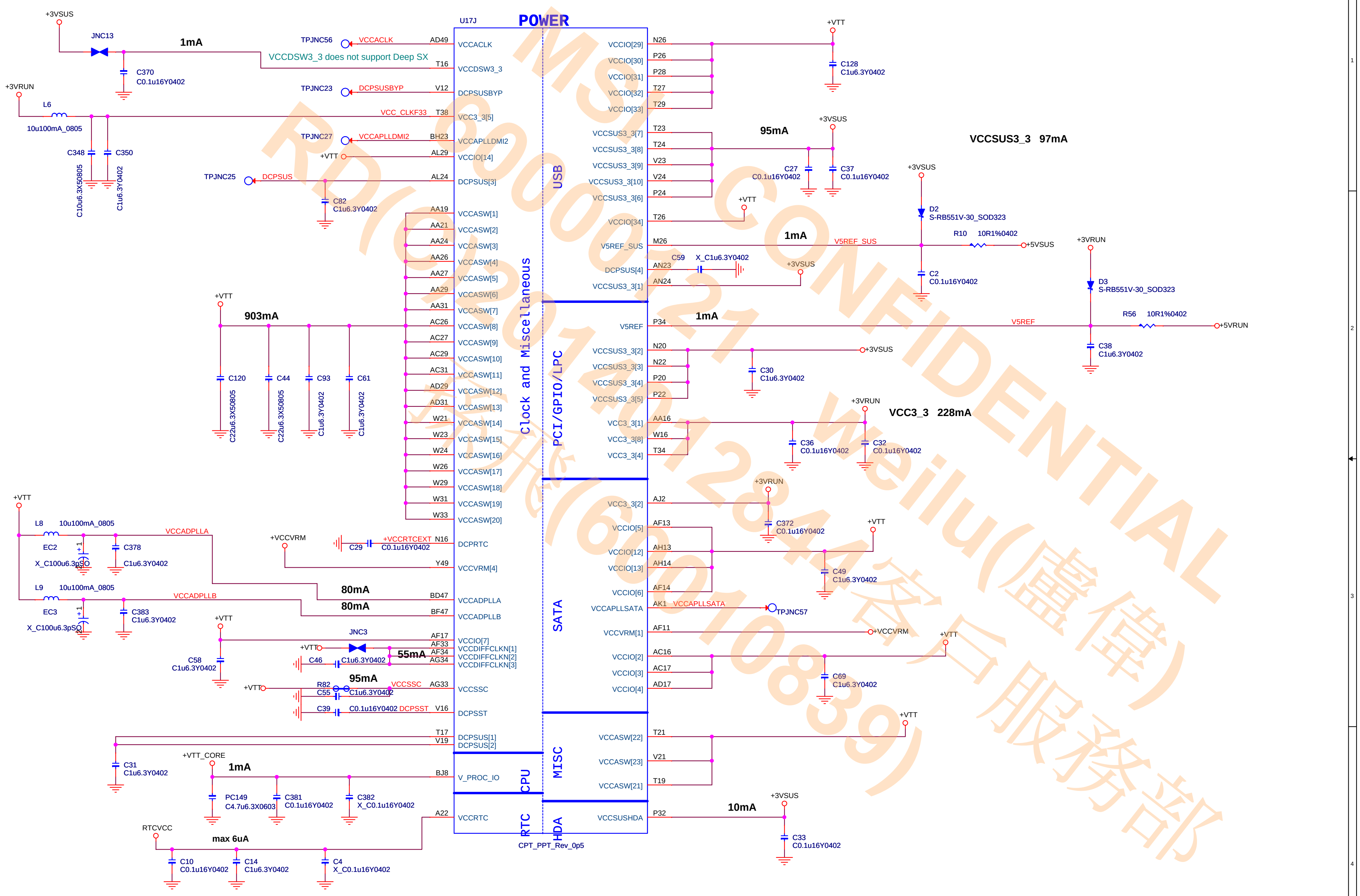
PANTHER POINT (POWER)



Title	PCH-8 (POWER)
Size	Custom
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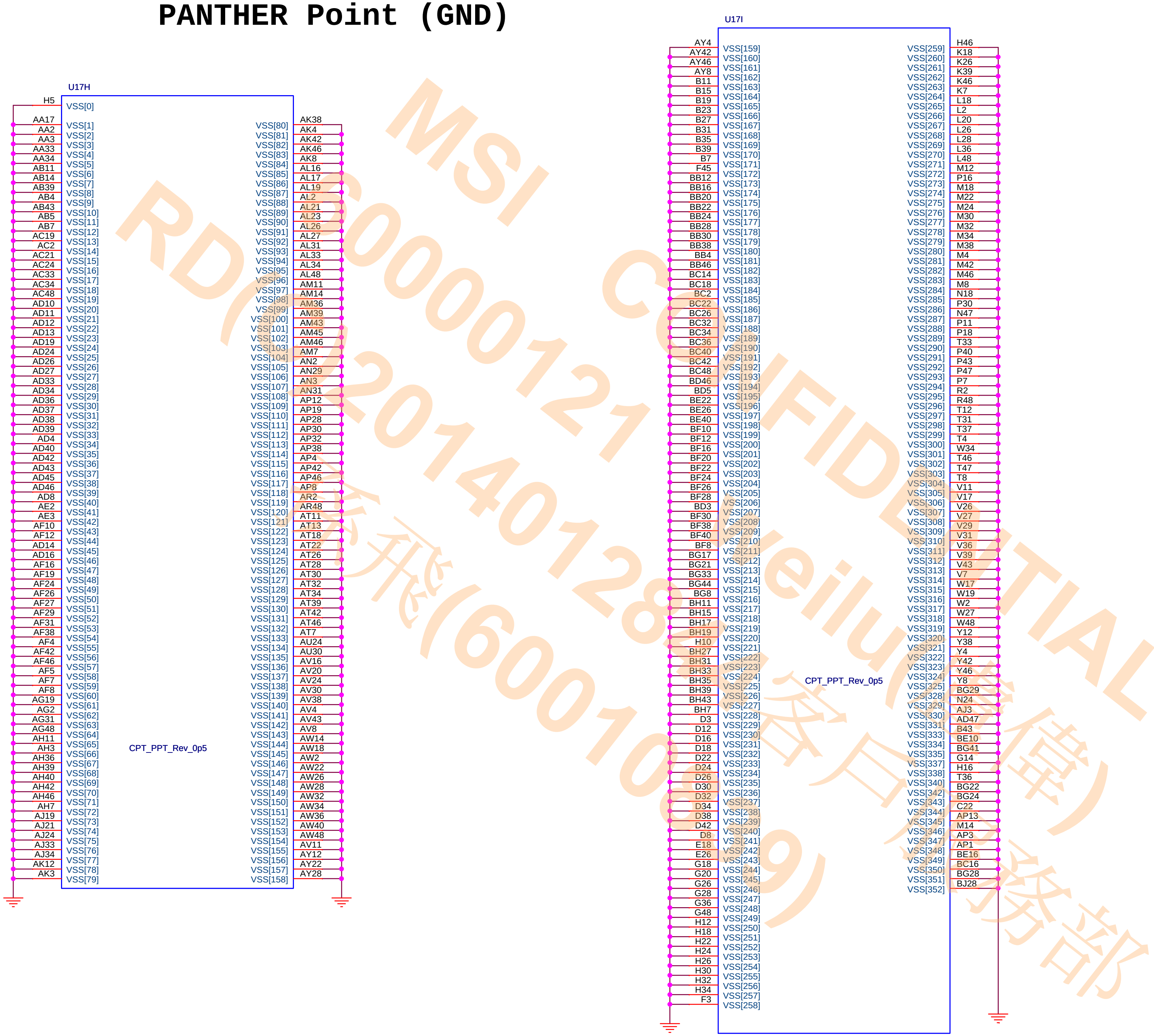
PANTHER Point (GND)



Title	PCH-9 (GND)
Size	Custom
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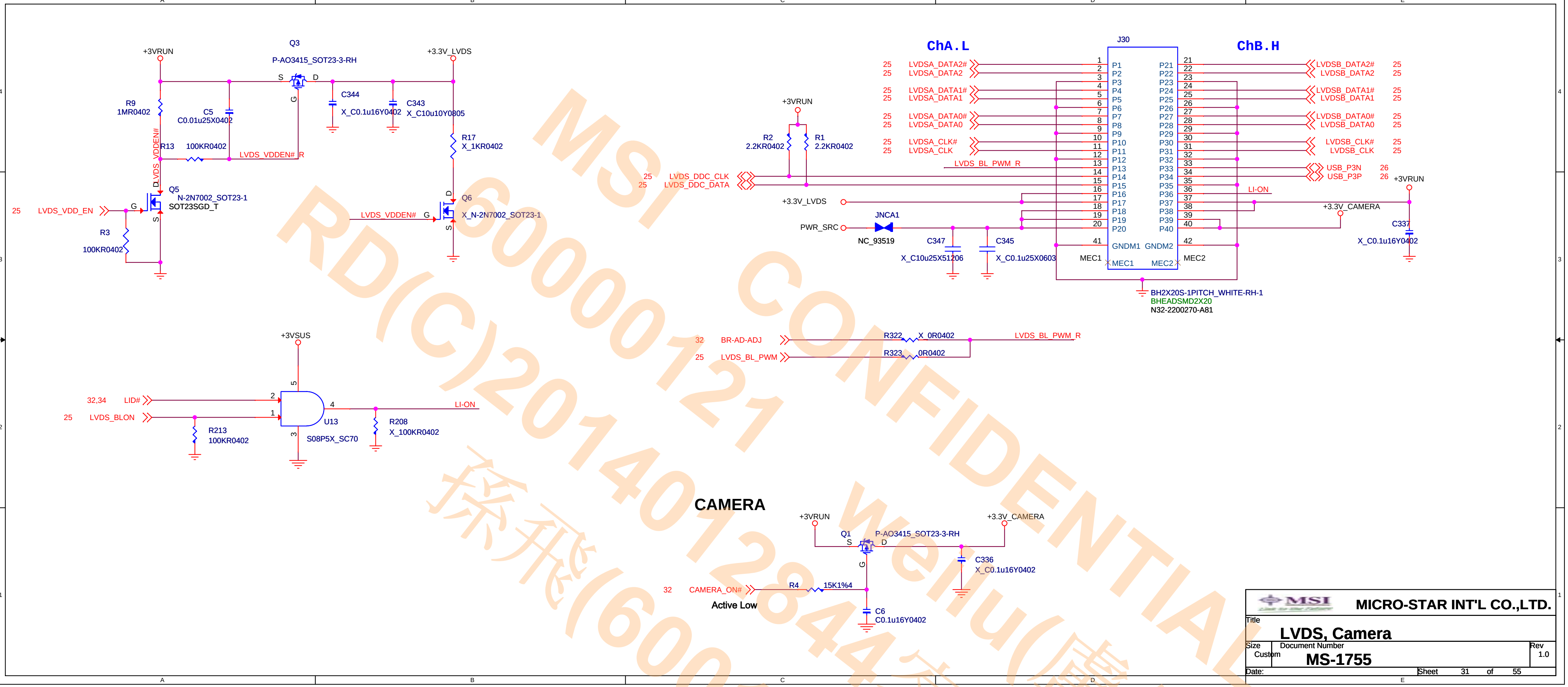
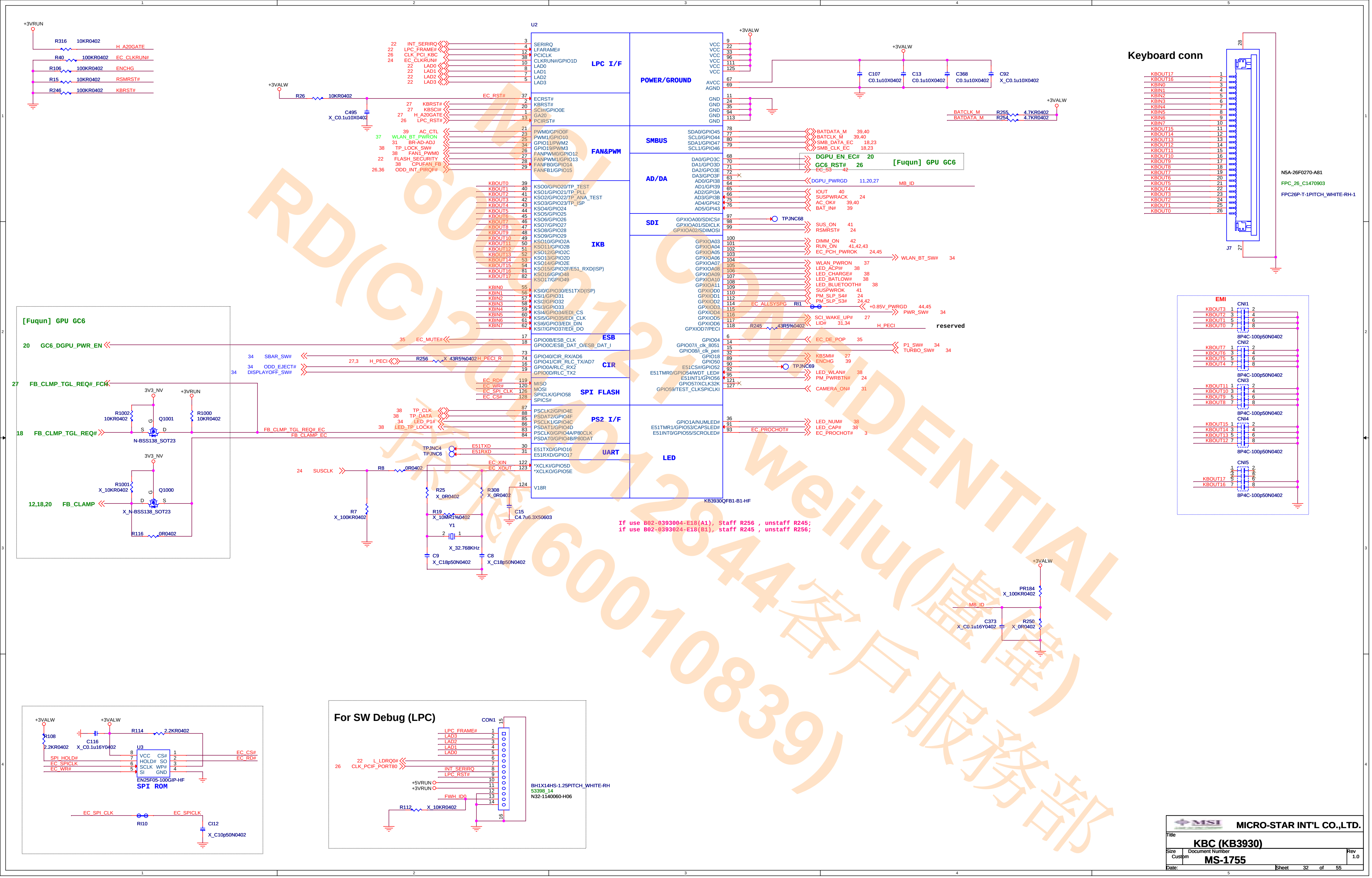
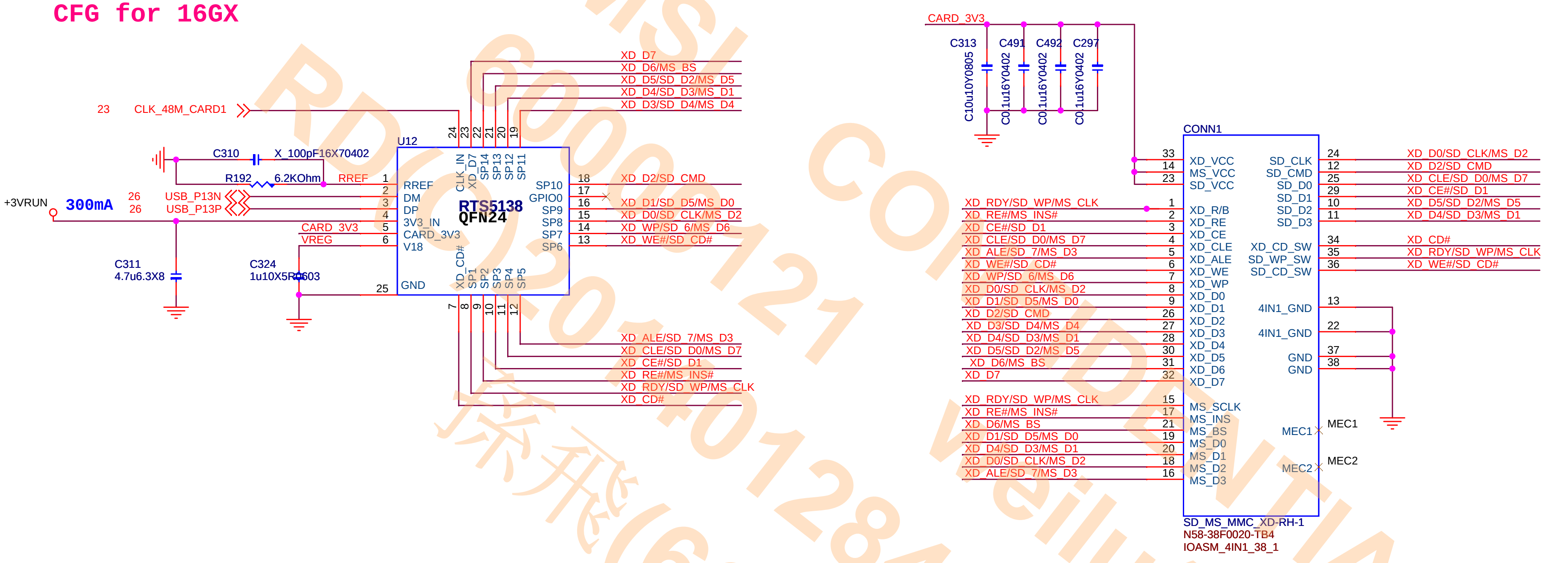




Card Reader controller RTS5138

CFG for 16GX

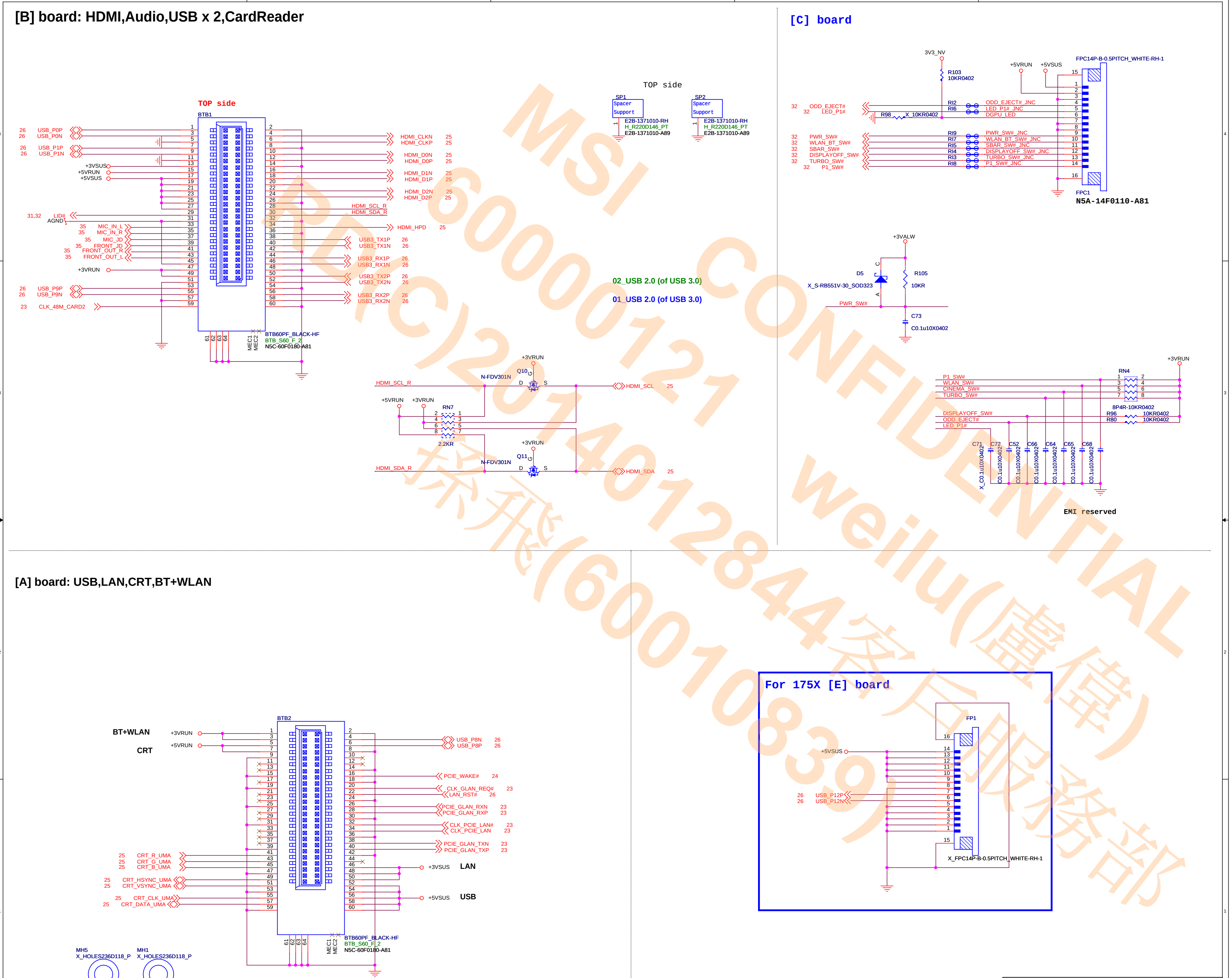


MICRO-STAR INT'L CO.,LTD.

Title: CardReader

Size: B | Document Number: MS-1755 | Rev: 1.0

Date: | Sheet 33 of 55



MICRO-STAR INT'L CO.,LTD.

Title: BTB PCIE Connectors

Size	Document Number	Rev
Custom	MS-1755	1.0

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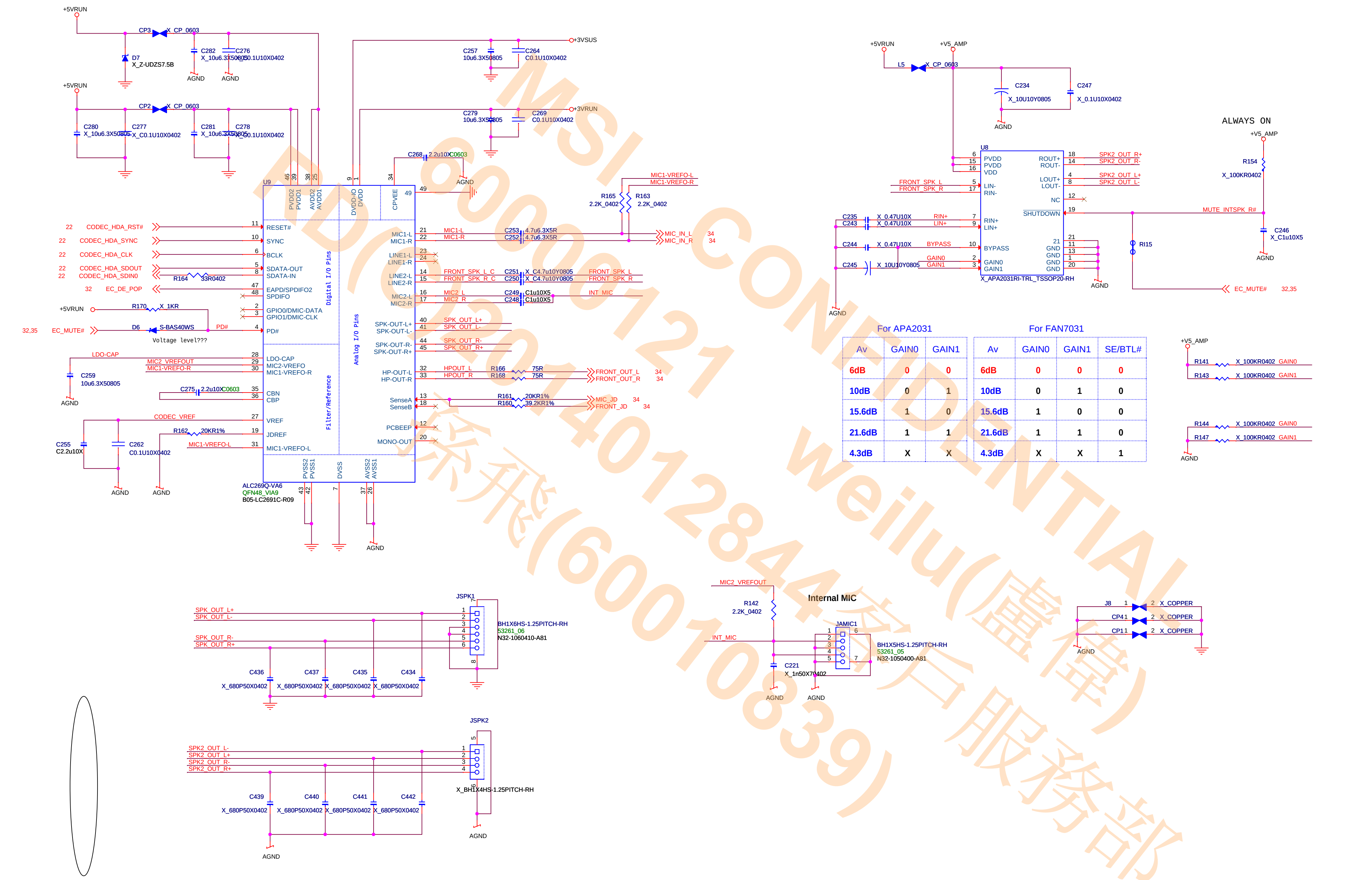

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

For FAN7031

Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

MICRO-STAR INT'L CO.,LTD.

Title: Audio ALC269/ AMP(APA2031)

Size: C | Document Number: MS-1755 | Rev: 1.0

SATA HDD

SCREW3
M2X4
E43-1205014-G68

SCREW4
M2X4
E43-1205014-G68

CN6
SATA22PSF_BLACK-HF
SATA_S22_14
N5N-22F0350-A81

C478 C0.01u25X0402 SATA0TXP_C
C479 C0.01u25X0402 SATA0TXN_C
C480 C0.01u25X0402 SATA0RXN_C
C481 C0.01u25X0402 SATA0RXP_C

22.GND
21.TX
20.TX#
19.GND
18.RX#
17.RX
16.GND
15.V33
14.V33
13.V33
12.GND
11.GND
10.GND
9.V5
8.V5
7.V5
6.GND
5.Reserved
4.GND
3.V12
2.V12
1.V12

+5VRUN
C308 C22u6.3X50805-HF
C489 C0.1u10X0402
C487 X_C0.1u10X0402
R191 X_0R0402

SATA ODD

SCREW5
M2X4
E43-1205014-G68

SCREW6
M2X4
E43-1205014-G68

CON2
SATA22PSF_BLACK-HF
N5N-13F0080-A81
SATA_S13_5

C493 C0.01u25X0402 SATA1TXP_C
C490 C0.01u25X0402 SATA1TXN_C
C488 C0.01u25X0402 SATA1RXN_C
C485 C0.01u25X0402 SATA1RXP_C

15.GND
14.GND
13.GND
12.TX
11.TX#
10.GND
9.RX#
8.RX
7.GND
6.DP
5.+5V
4.+5V
3.MD
2.GND
1.GND

+5VRUN
R305 X_10KR0402 DP
+5VRUN_ODD
26,32 ODD_INT_PIRQF#

L10 X_80ohm3A
Q27 N-AO3404_SOT23
R304 2MR0402
Q26 N-2N7002G_SOT23-1
C482 X_C0.1u10X0402
C484 X_C100u6.3X51210
C483 X_C10u6.3X50805
C486 C0.1u10X0402
20,41,42 RUND
26 ODD_PWR_ON#

[Fuqun] EC control change to PCH control

MICRO-STAR INT'L CO.,LTD.

Title: HDD, ODD		
Size: B	Document Number: MS-1755	Rev: 1.0
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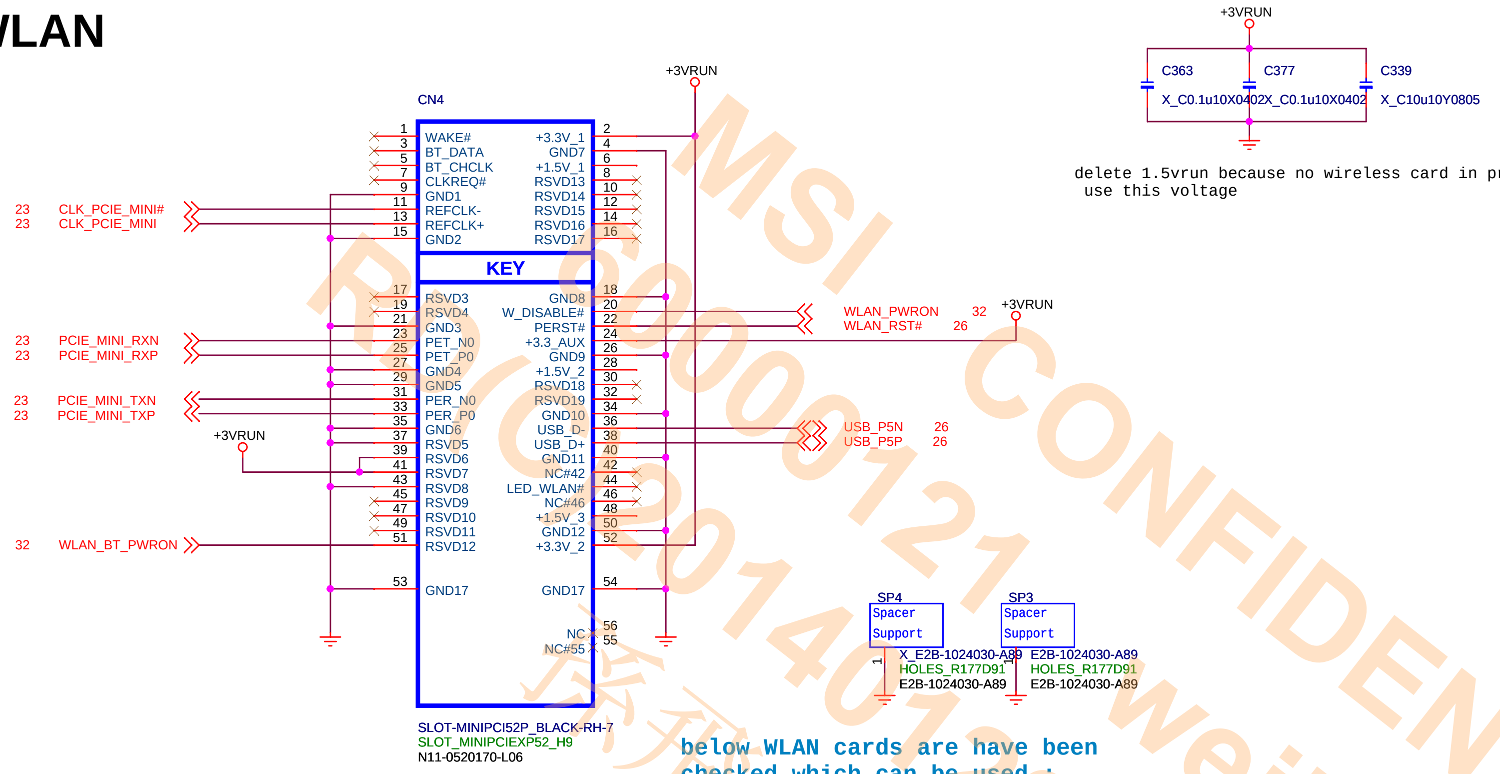
WLAN



delete 1.5vrun because no wireless card in product AVL
use this voltage

PIN51 for intel N130 BT control &AW-NB087H BT control;
PIN5 for AW-NB041H BT control;

AW-NB087H BT do not use USB interface,it only share PCIE interface.

below WLAN cards are have been checked which can be used :
Intel N130/N135;
AW-NB100H/NE785H/NE139H;

MICRO-STAR INT'L CO.,LTD.

Title	WLAN, BT
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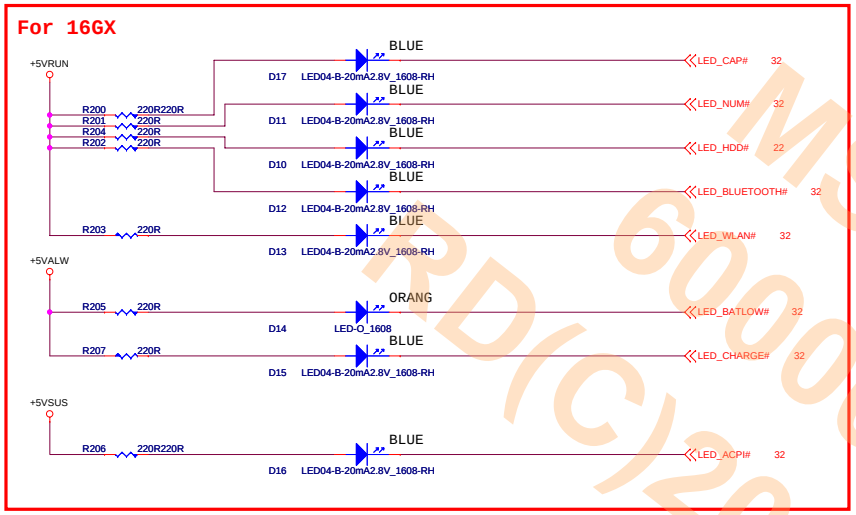
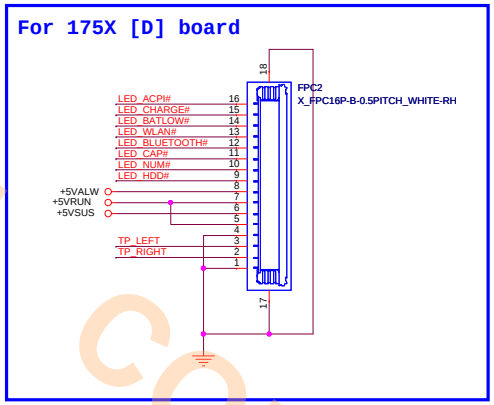
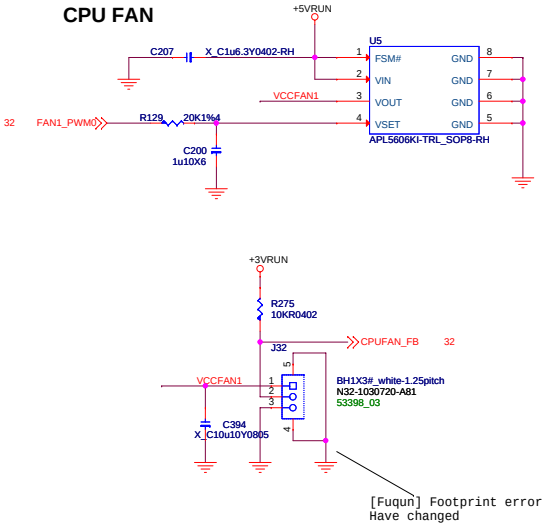
LED

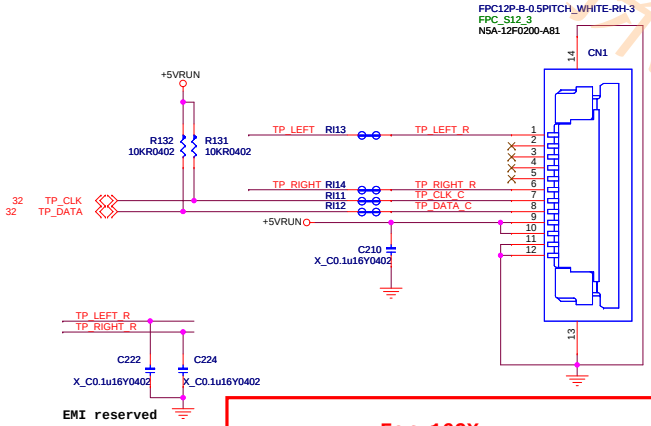


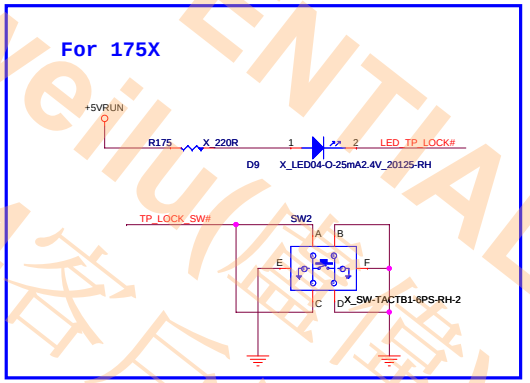


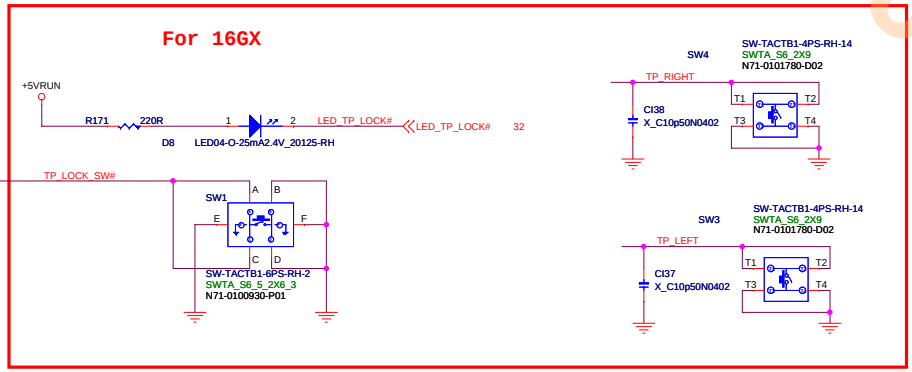
CPU FAN



Touch Pad







MSI	MICRO-STAR INT'L CO.,LTD.	
Title	TP, LED, FAN	
Size: Custom	Document Number: MS-1755	Rev: 1.0
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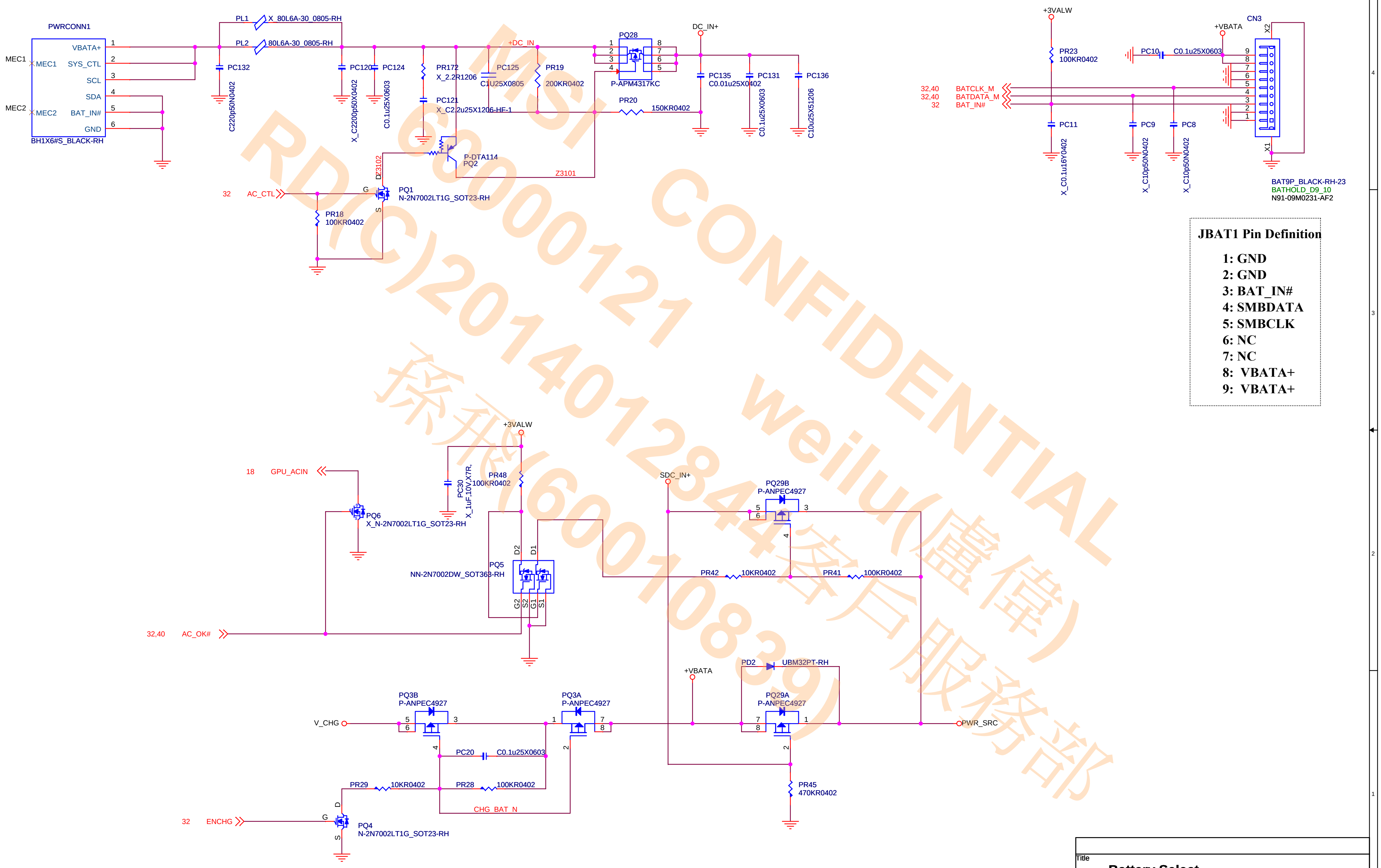

Title: Battery Select		
Size: Custom	Document Number: MS-1755	Rev: 1.0
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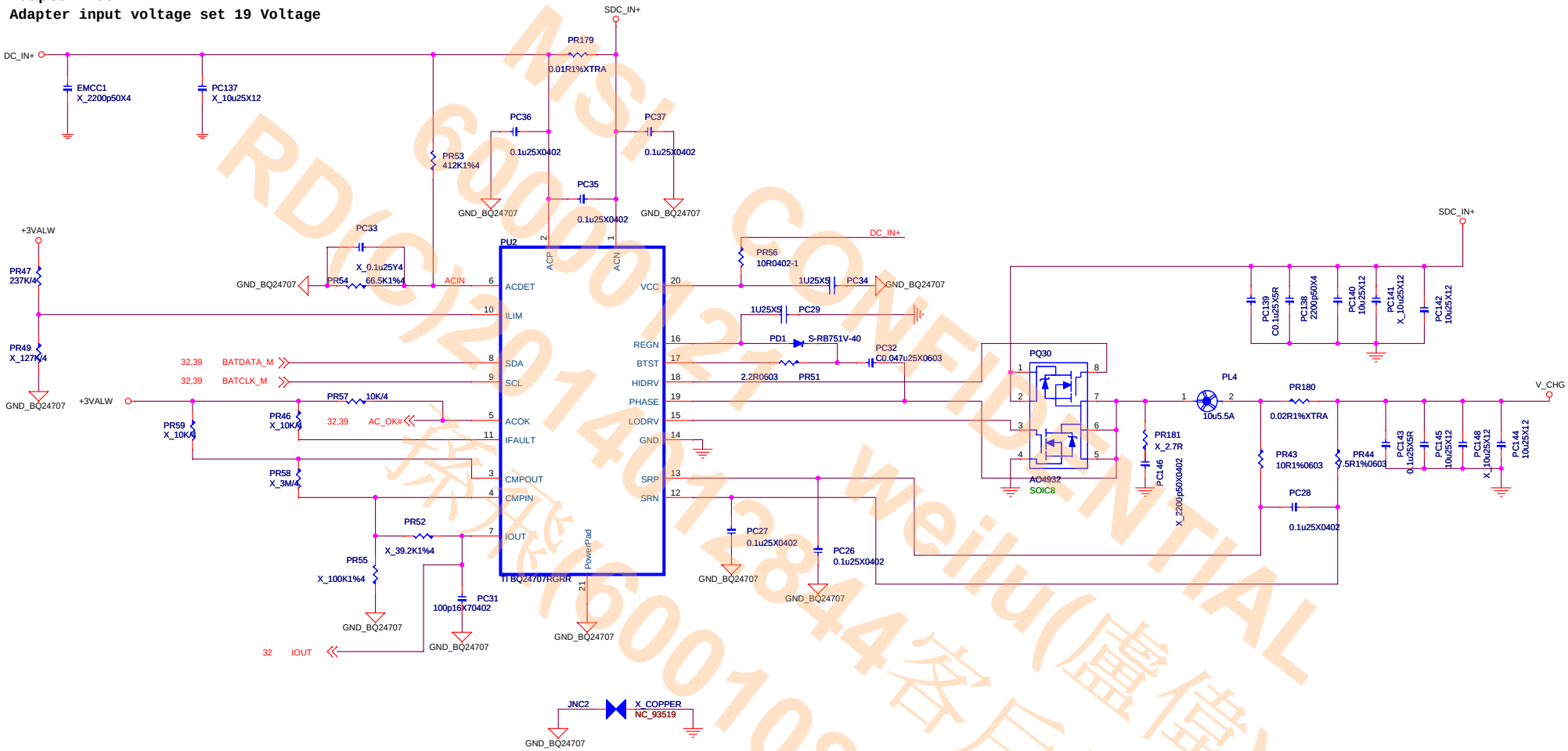
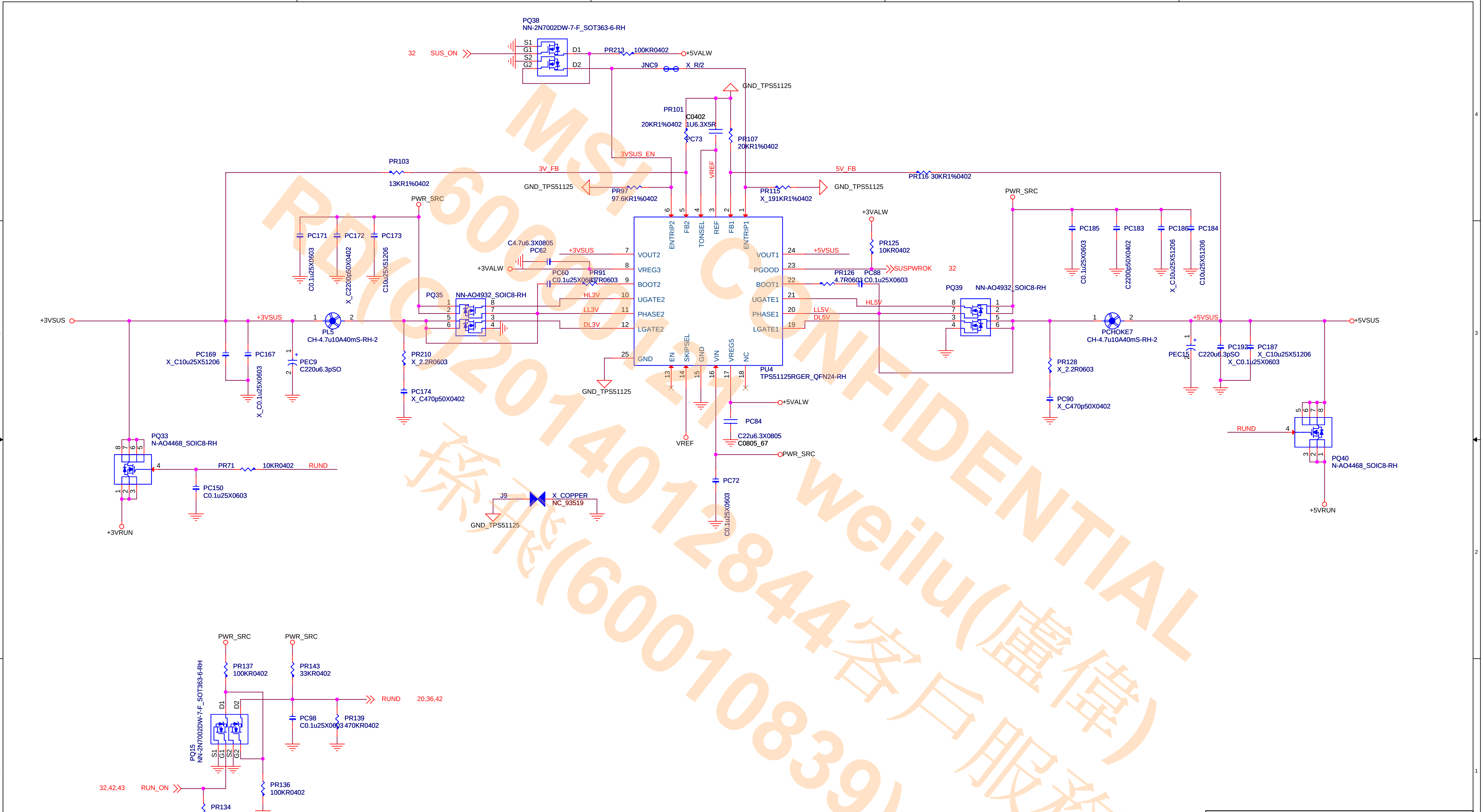
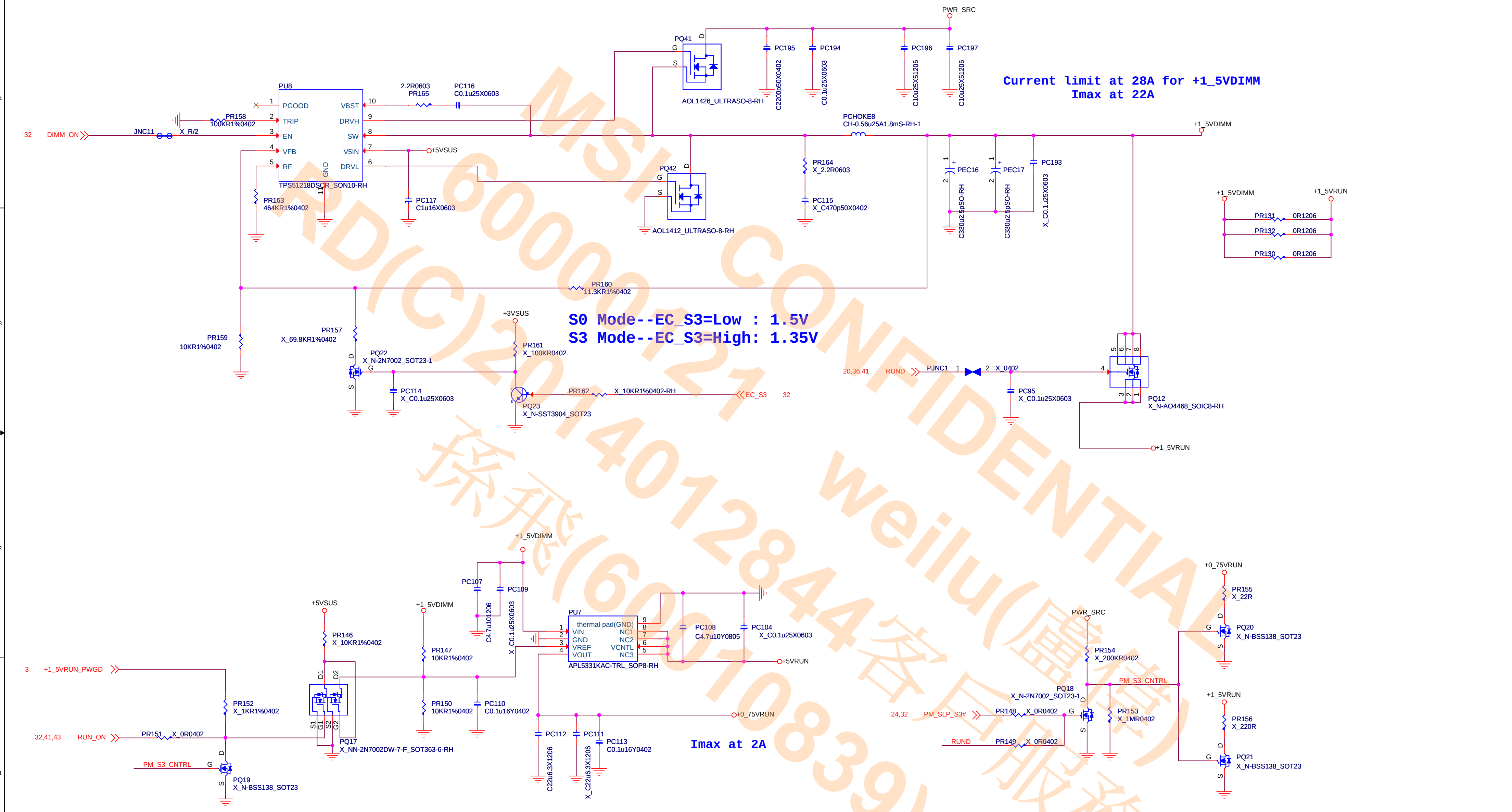
Adapter= 90W
Adapter input voltage set 19 Voltage



MSI	MICRO-STAR INT'L CO.,LTD.	
Title: Charger		
Size: Custom	Document Number: MS-1755	Rev: 1.0
Date: Thursday, December 06, 2012	Sheet 40 of 55	



Title	System Power	
Size Custom	Document Number MS-1755	Rev 1.0
Date: Thursday, December 06, 2012	Sheet 41 of 55	



Title	DIMM_1.5VRUN
Size	Custom
Document Number	MS-1755
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Date:	Thursday, December 06, 2012
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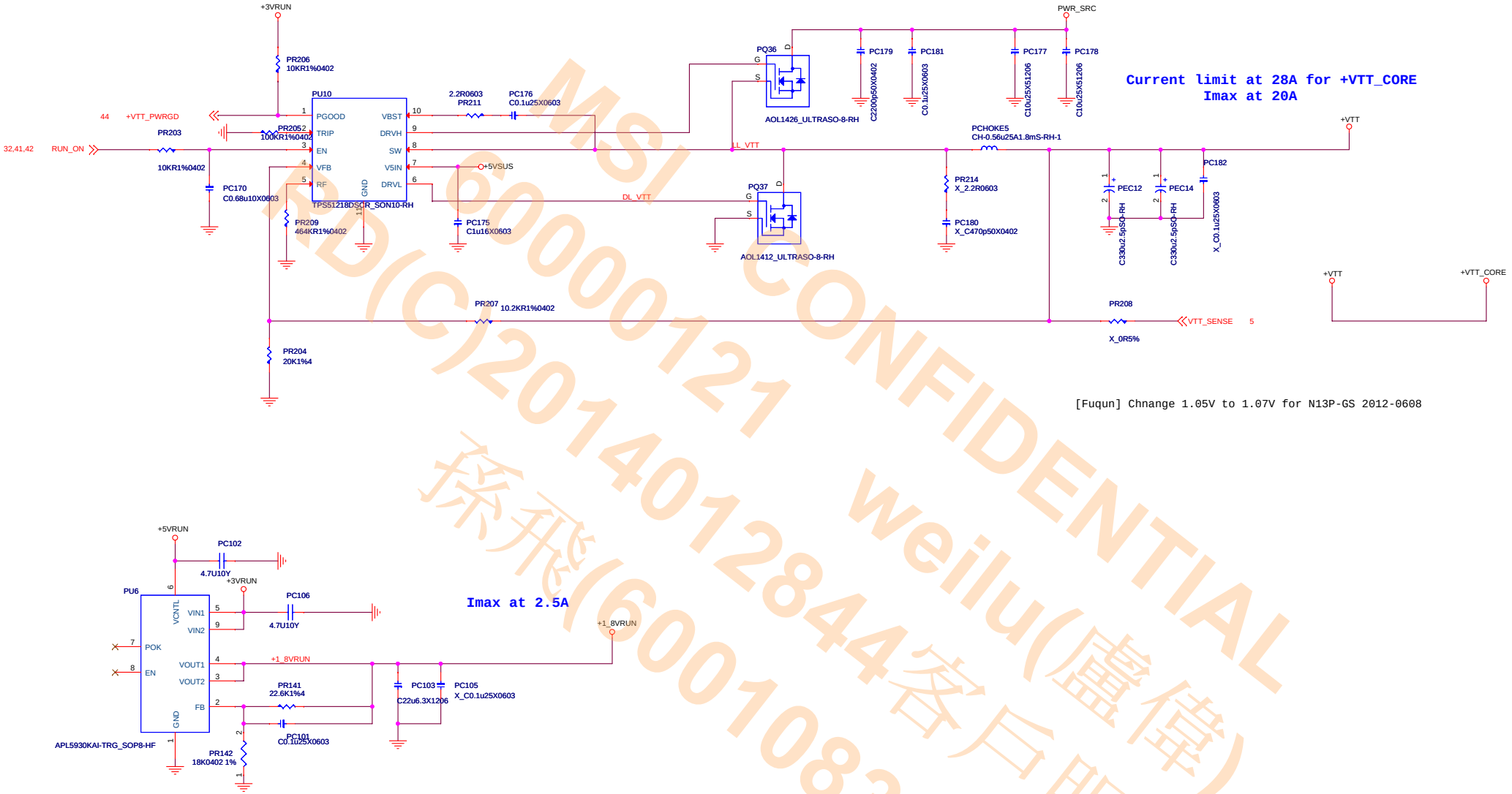
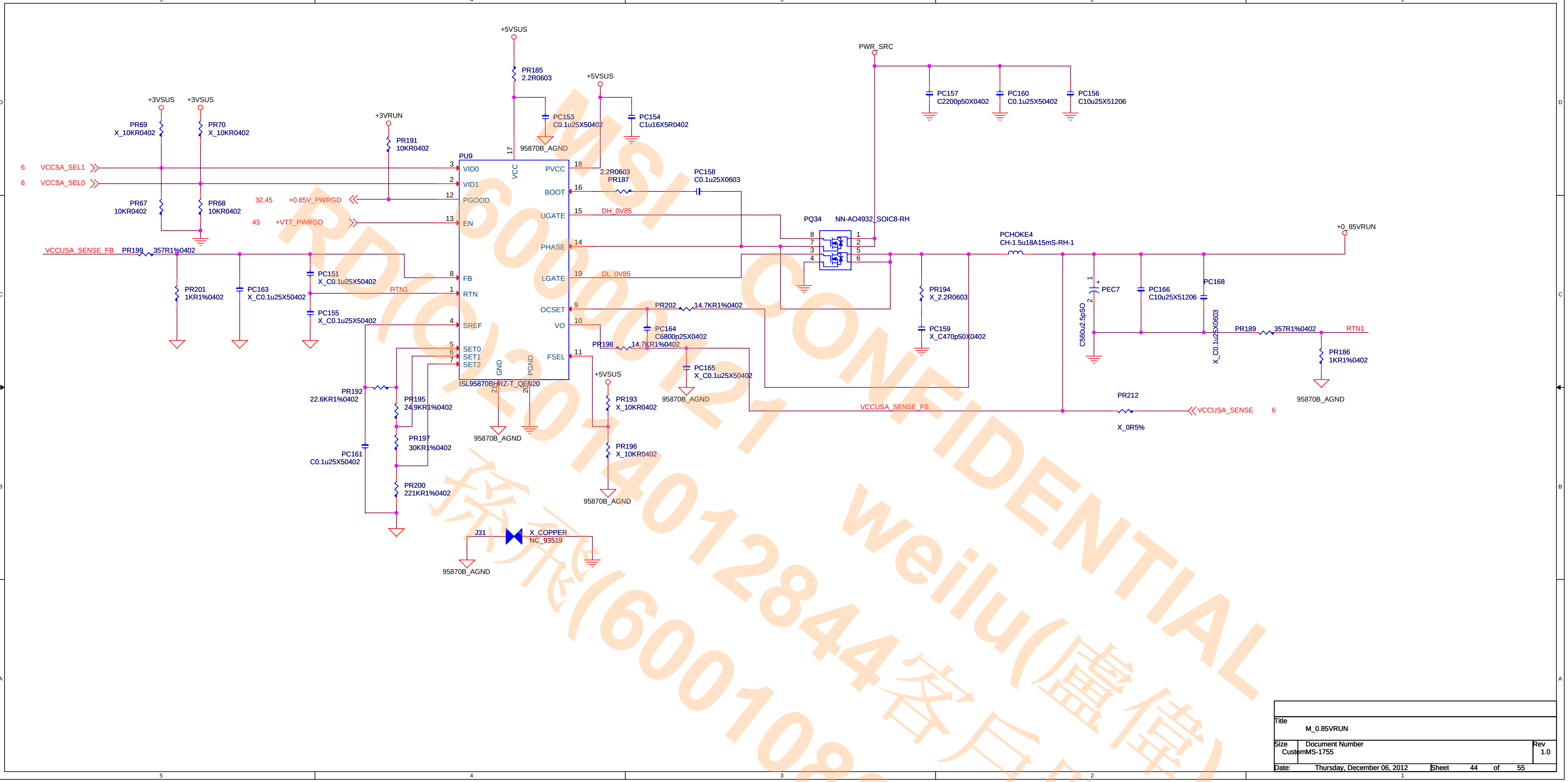


Title	VTT_1.8VRUN	
Size: Custom	Document Number: MS-1755	Rev: 1.0
Date: Thursday, December 06, 2012	Sheet 43 of 55	



Title: M_0.85VRUN

Size	Document Number	Rev
Custom	MS-1755	1.0

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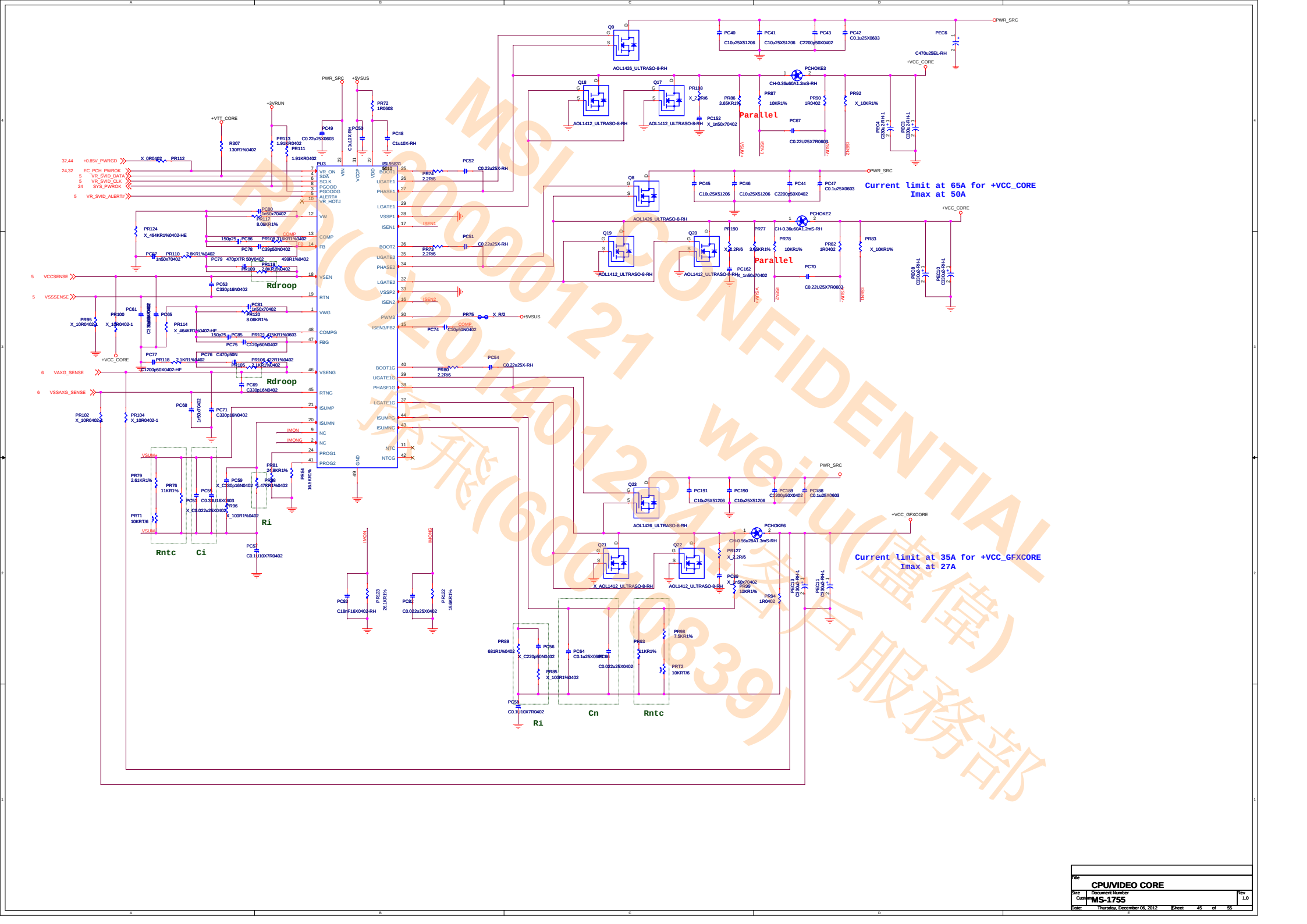
Parallel
Parallel
Current limit at 65A for +VCC_CORE
Imax at 50A
Current limit at 35A for +VCC_GFXCORE
Imax at 27A
Rdroop
Rdroop
Rntc
Ci
Ri
Cn
Rntc
Ri
VSUM+
VSUM-
IMON
IMONG
PWR_SRC
+5VSUS
+3VRUN
+VTT_CORE
+VCC_CORE
+VCC_GFXCORE
VCCSENSE
VSSSENSE
VAXG_SENSE
VSSAXG_SENSE
Title
CPU/VIDEO CORE
Size
Custom
Document Number
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1.0
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45
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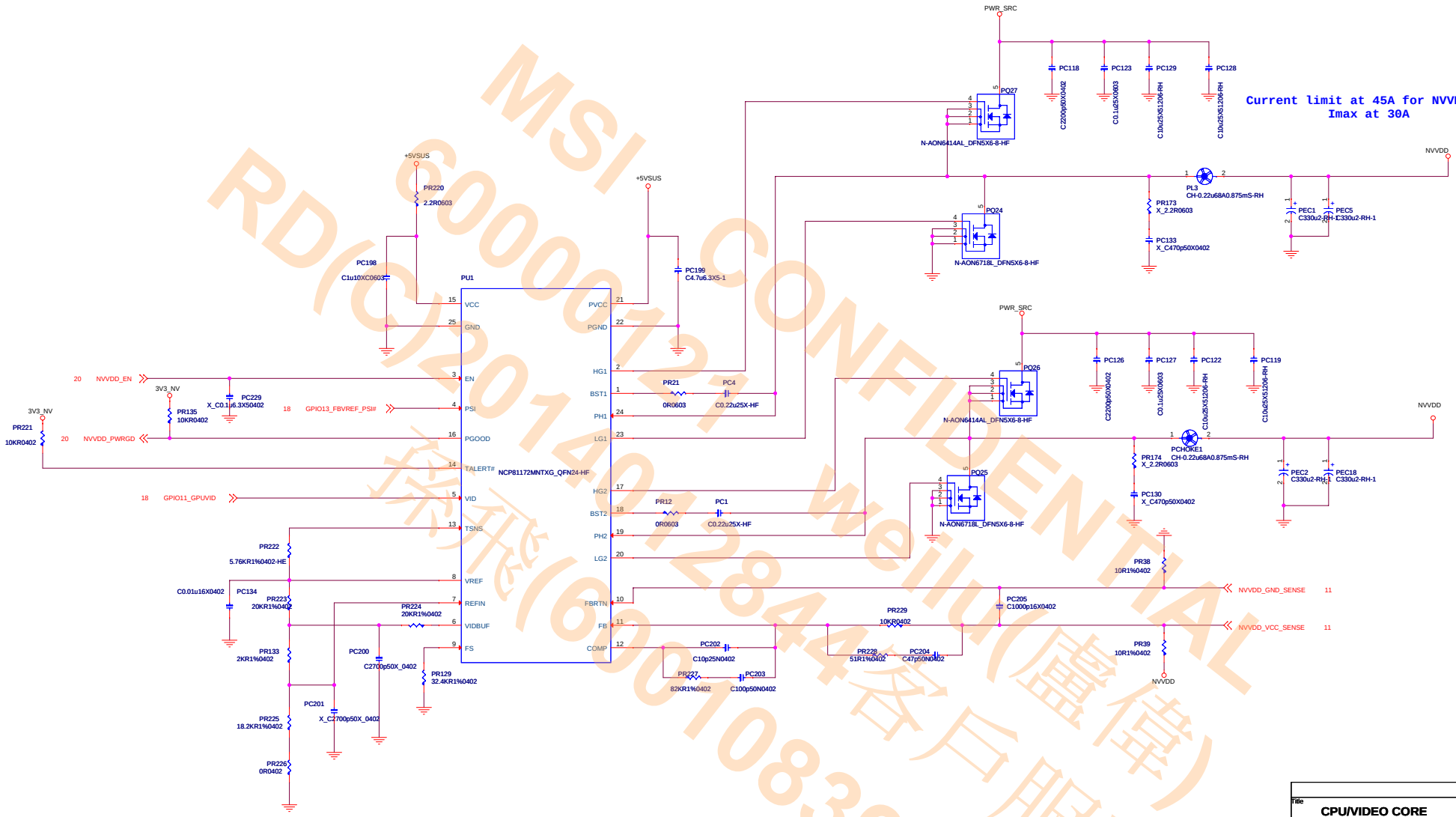

Title	CPU/VIDEO CORE		
Size	Document Number		Rev
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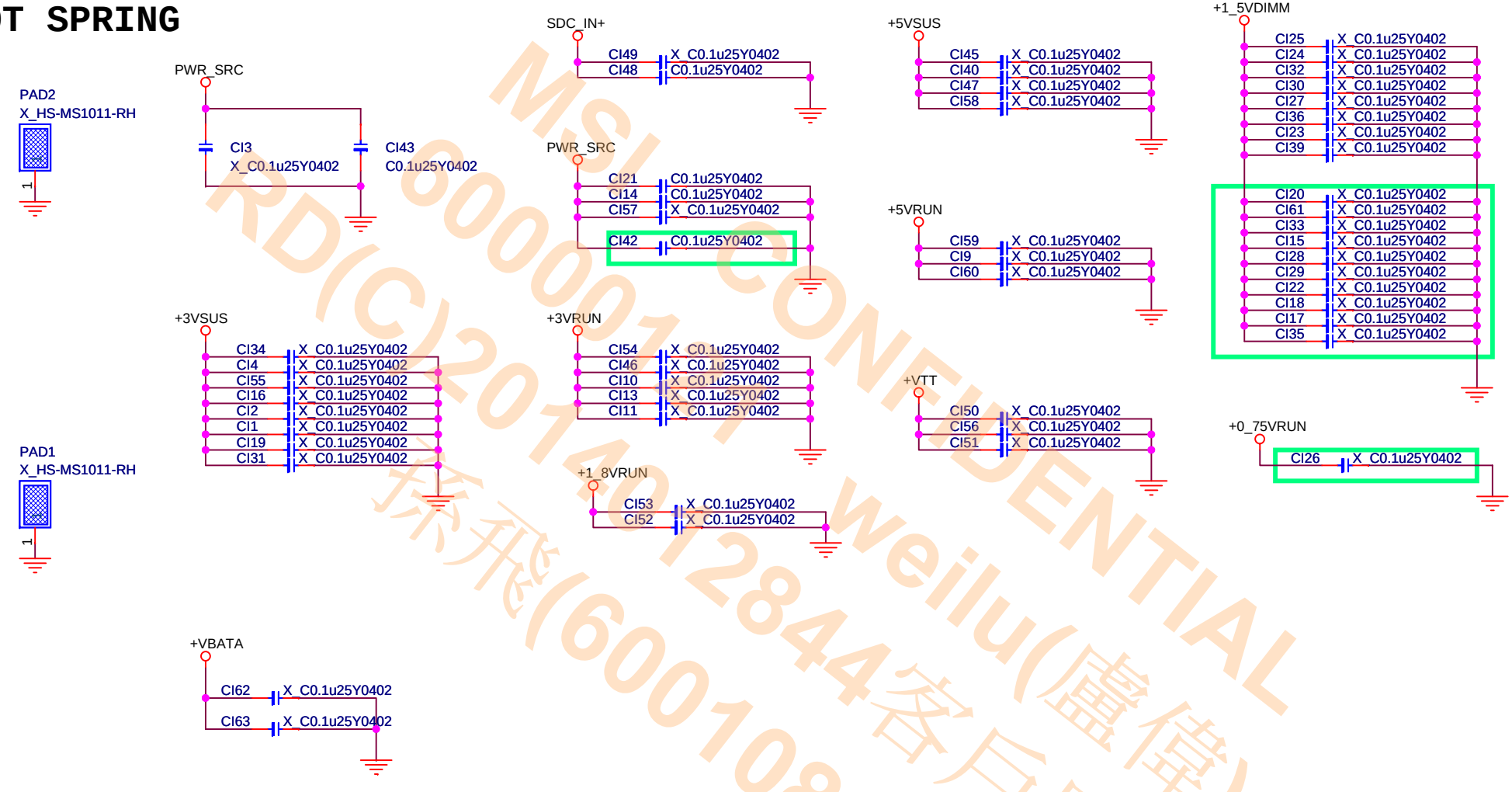
BOT SPRING



MICRO-STAR INT'L CO.,LTD.		
Title: EMI		
Size: Custom	Document Number: MS-1755	Rev: 1.0
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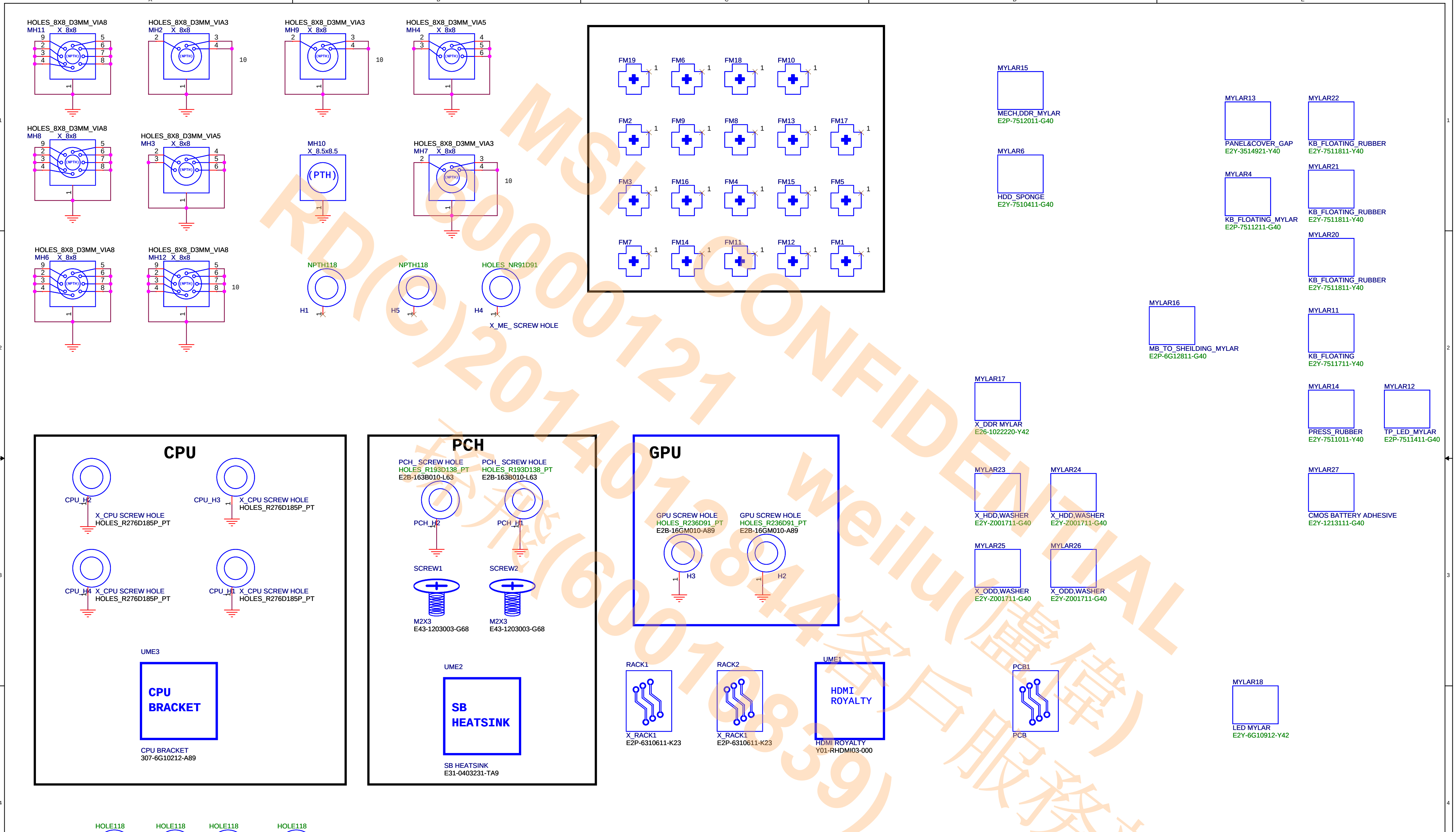

MICRO-STAR INT'L CO.,LTD.

Title: Screw / ME

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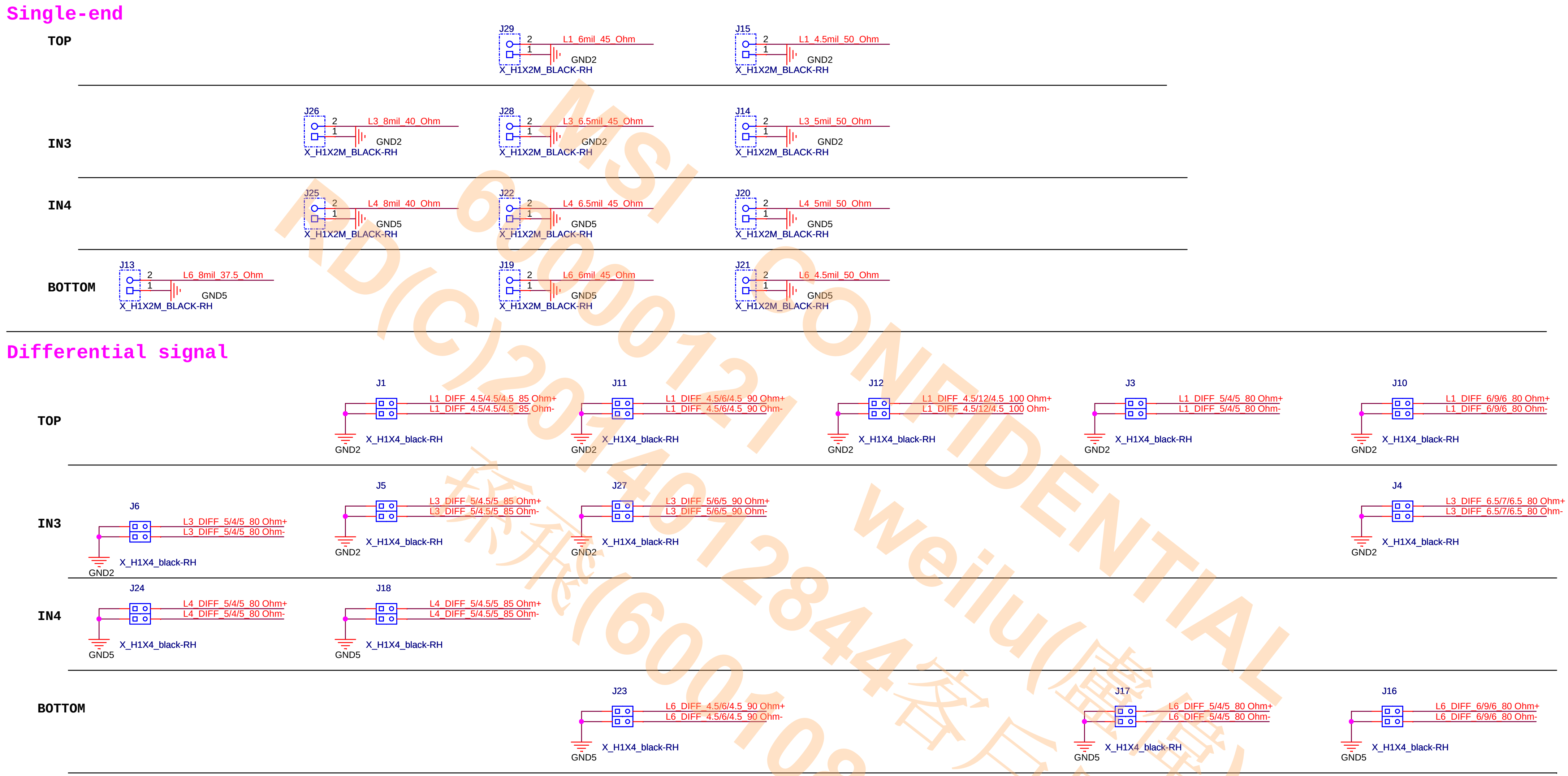
Custom	MS-1755	1.0

Date: Thursday, December 06, 2012 Sheet 48 of 55


Single-end
TOP
J29
L1_6mil_45_Ohm
GND2
X_H1X2M_BLACK-RH
J15
L1_4.5mil_50_Ohm
GND2
X_H1X2M_BLACK-RH
IN3
J26
L3_8mil_40_Ohm
GND2
X_H1X2M_BLACK-RH
J28
L3_6.5mil_45_Ohm
GND2
X_H1X2M_BLACK-RH
J14
L3_5mil_50_Ohm
GND2
X_H1X2M_BLACK-RH
IN4
J25
L4_8mil_40_Ohm
GND5
X_H1X2M_BLACK-RH
J22
L4_6.5mil_45_Ohm
GND5
X_H1X2M_BLACK-RH
J20
L4_5mil_50_Ohm
GND5
X_H1X2M_BLACK-RH
BOTTOM
J13
L6_8mil_37.5_Ohm
GND5
X_H1X2M_BLACK-RH
J19
L6_6mil_45_Ohm
GND5
X_H1X2M_BLACK-RH
J21
L6_4.5mil_50_Ohm
GND5
X_H1X2M_BLACK-RH
Differential signal
TOP
J1
L1_DIFF_4.5/4.5/4.5_85 Ohm+
L1_DIFF_4.5/4.5/4.5_85 Ohm-
GND2
X_H1X4_black-RH
J11
L1_DIFF_4.5/6/4.5_90 Ohm+
L1_DIFF_4.5/6/4.5_90 Ohm-
GND2
X_H1X4_black-RH
J12
L1_DIFF_4.5/12/4.5_100 Ohm+
L1_DIFF_4.5/12/4.5_100 Ohm-
GND2
X_H1X4_black-RH
J3
L1_DIFF_5/4/5_80 Ohm+
L1_DIFF_5/4/5_80 Ohm-
GND2
X_H1X4_black-RH
J10
L1_DIFF_6/9/6_80 Ohm+
L1_DIFF_6/9/6_80 Ohm-
GND2
X_H1X4_black-RH
IN3
J6
L3_DIFF_5/4/5_80 Ohm+
L3_DIFF_5/4/5_80 Ohm-
GND2
X_H1X4_black-RH
J5
L3_DIFF_5/4.5/5_85 Ohm+
L3_DIFF_5/4.5/5_85 Ohm-
GND2
X_H1X4_black-RH
J27
L3_DIFF_5/6/5_90 Ohm+
L3_DIFF_5/6/5_90 Ohm-
GND2
X_H1X4_black-RH
J4
L3_DIFF_6.5/7/6.5_80 Ohm+
L3_DIFF_6.5/7/6.5_80 Ohm-
GND2
X_H1X4_black-RH
IN4
J24
L4_DIFF_5/4/5_80 Ohm+
L4_DIFF_5/4/5_80 Ohm-
GND5
X_H1X4_black-RH
J18
L4_DIFF_5/4.5/5_85 Ohm+
L4_DIFF_5/4.5/5_85 Ohm-
GND5
X_H1X4_black-RH
BOTTOM
J23
L6_DIFF_4.5/6/4.5_90 Ohm+
L6_DIFF_4.5/6/4.5_90 Ohm-
GND5
X_H1X4_black-RH
J17
L6_DIFF_5/4/5_80 Ohm+
L6_DIFF_5/4/5_80 Ohm-
GND5
X_H1X4_black-RH
J16
L6_DIFF_6/9/6_80 Ohm+
L6_DIFF_6/9/6_80 Ohm-
GND5
X_H1X4_black-RH

Title	Impedance	
Size: Custom	Document Number: MS-1755	Rev: 1.0
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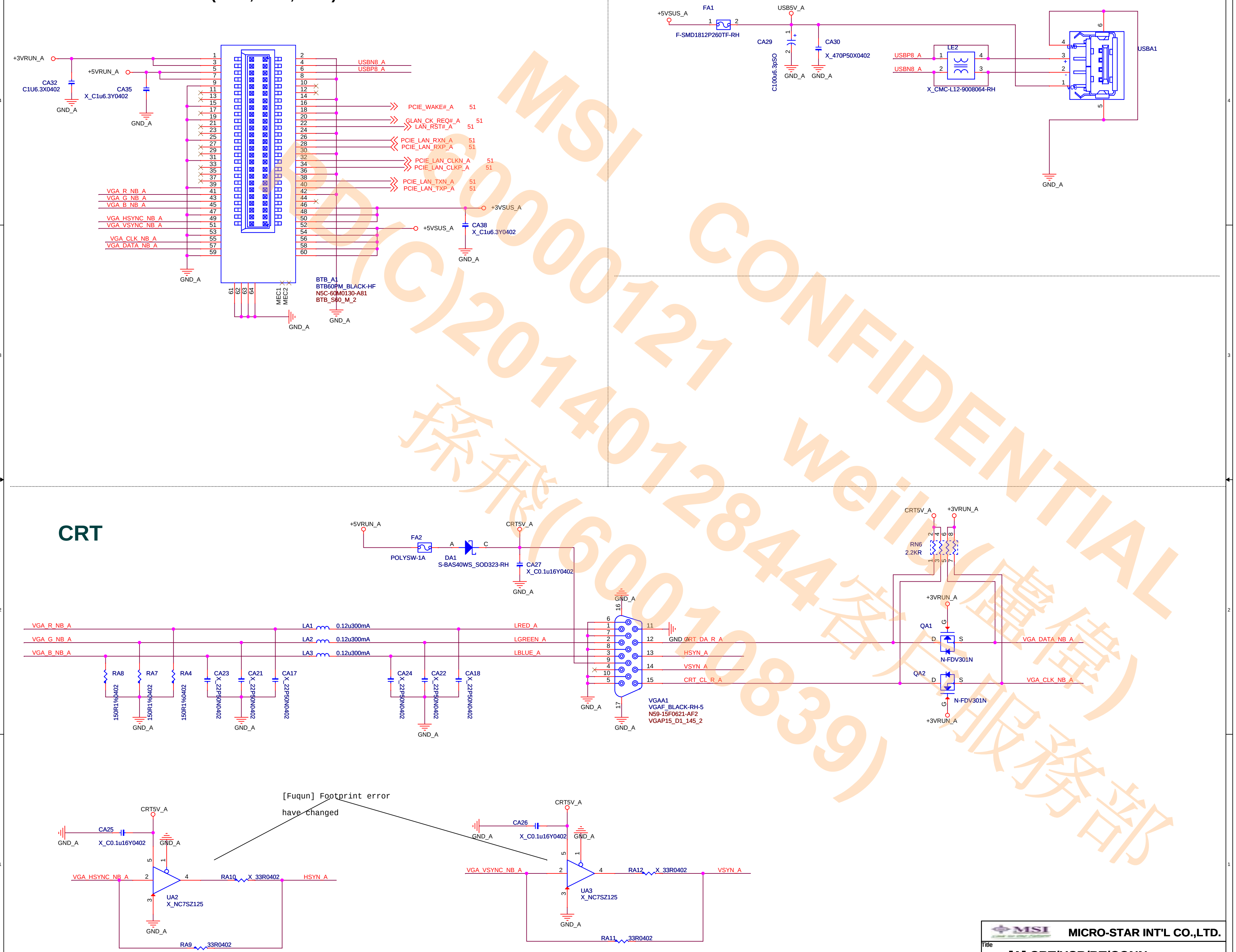
60PIN BTB I/O Connector(VGA, LAN, USB)

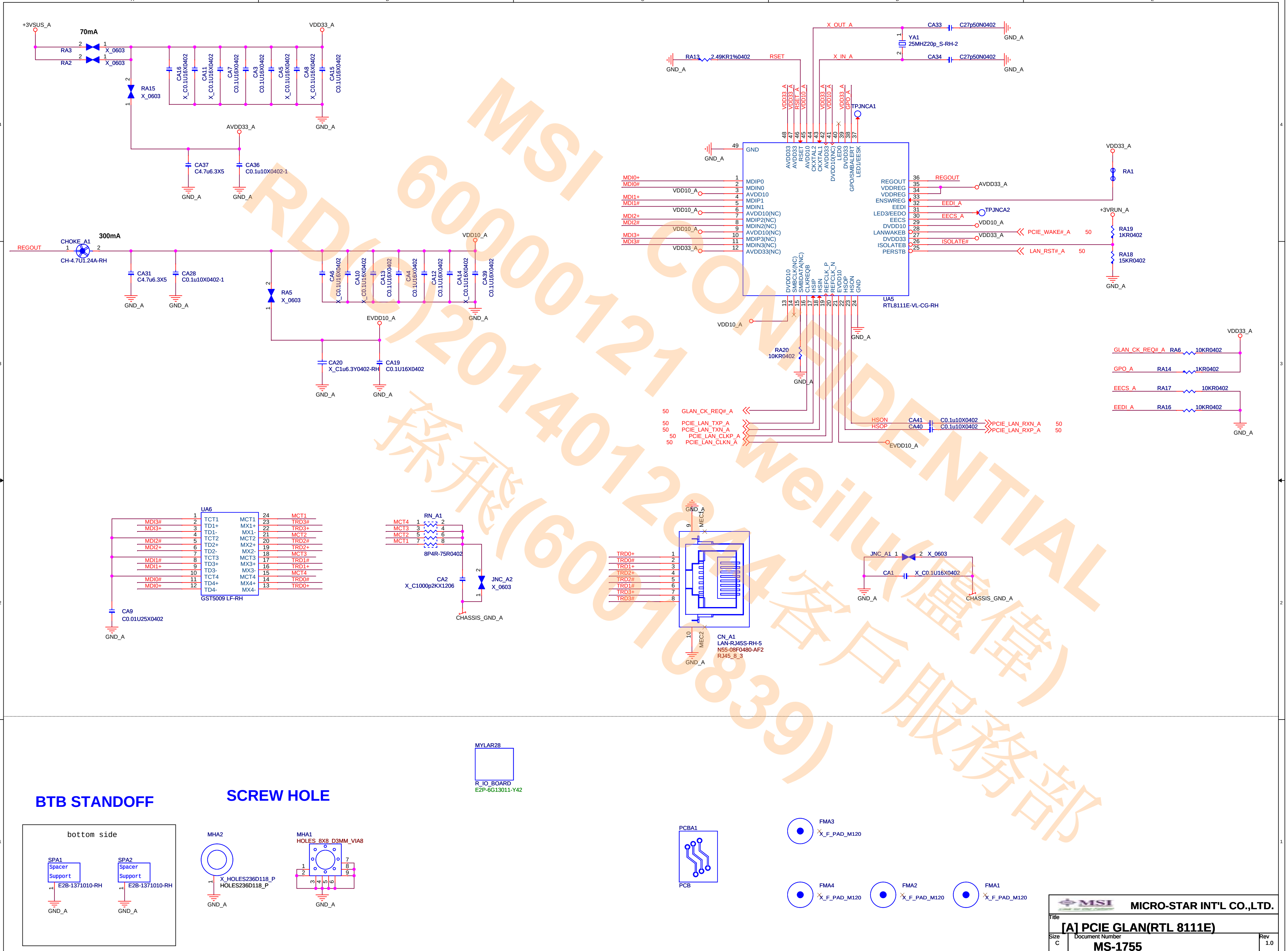


MICRO-STAR INT'L CO.,LTD.

Title: [A] CRT/USB/BT/CONN

Size: Custom | Document Number: MS-1755 | Rev: 1.0

Date: Thursday, December 06, 2012 | Sheet 50 of 55



MICRO-STAR INT'L CO.,LTD.

Title: [A] PCIE GLAN(RTL 8111E)

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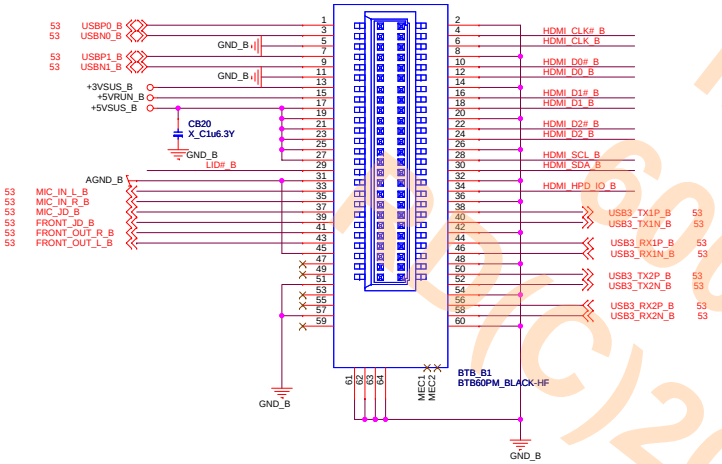
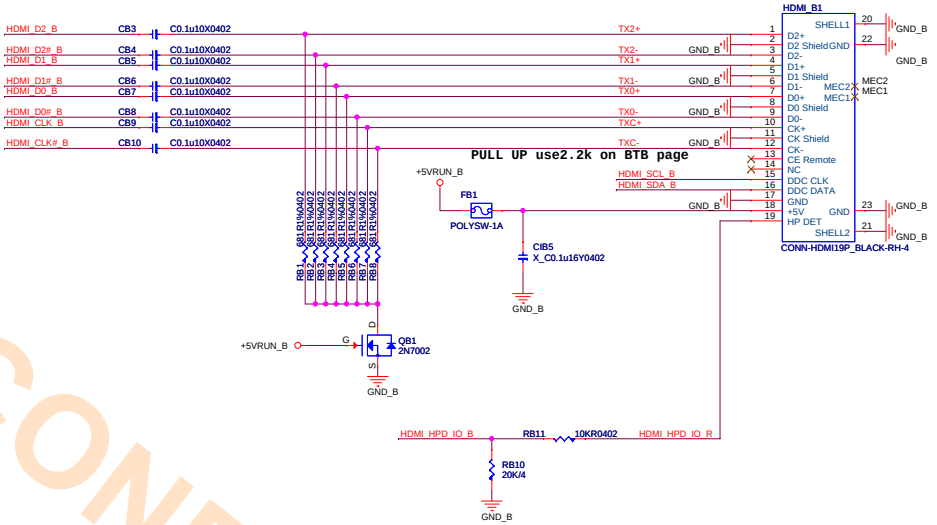
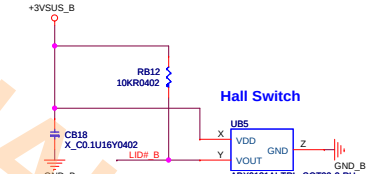
(オ凹 board to board CONN1: HDMI,Audio, LED,LID)



HDMI



LID



MICRO-STAR INT'L CO.,LTD.		
Title: [B] HDMI/Cardreader/CONN		
Size: C	Document Number: MS-1755	Rev: 1.0
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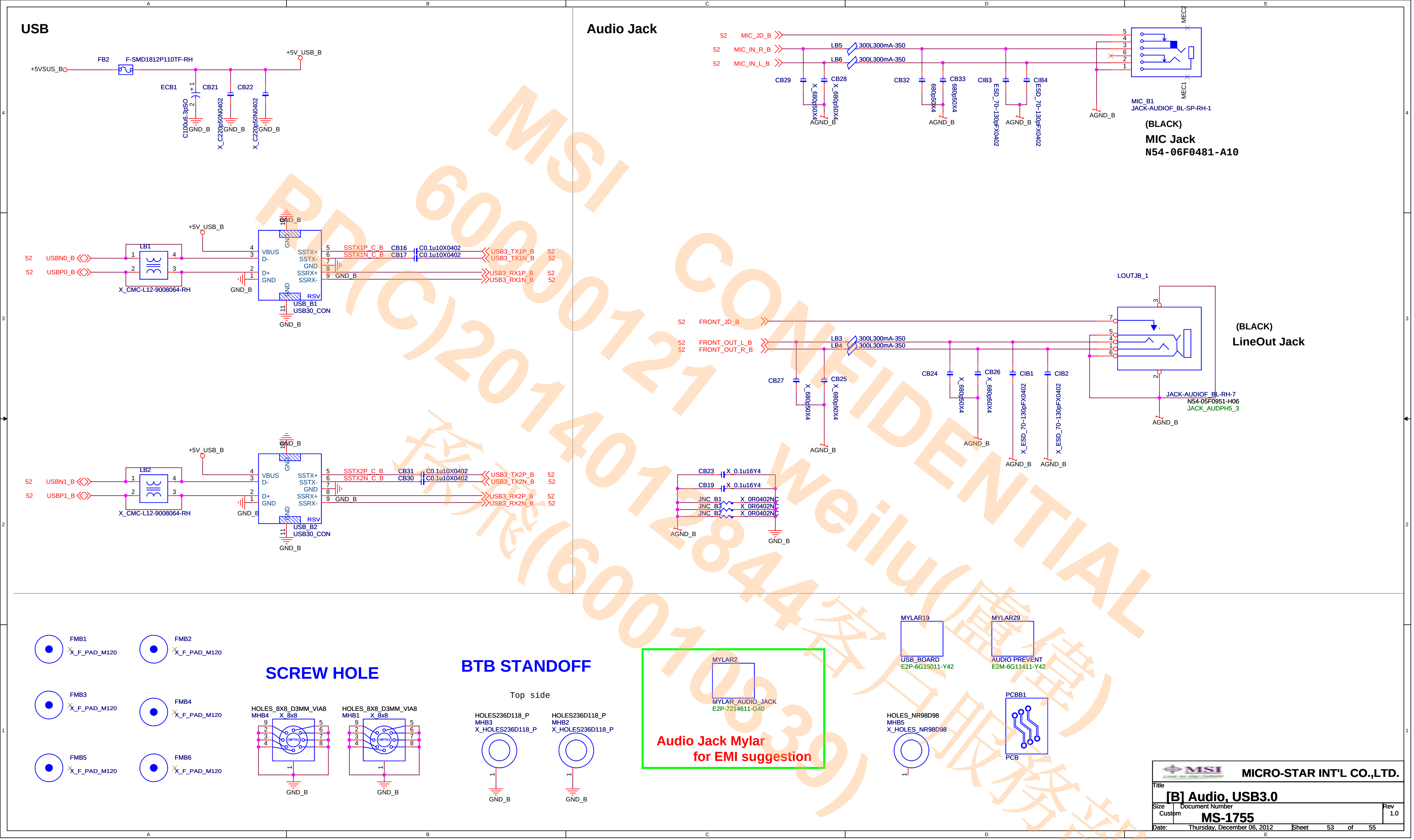
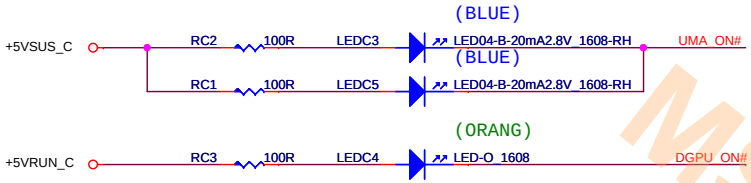
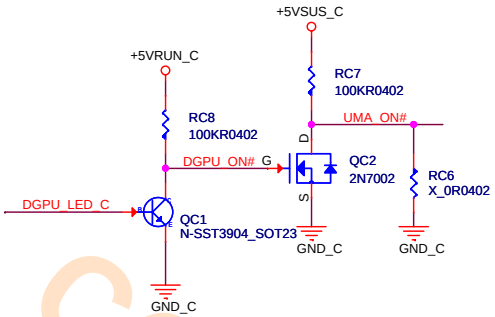
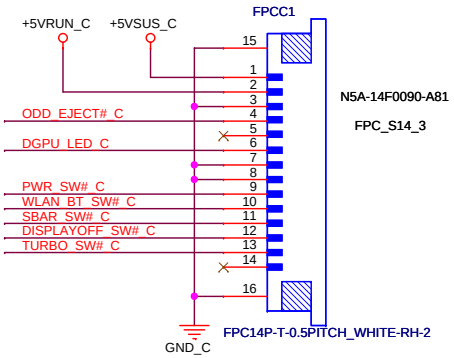
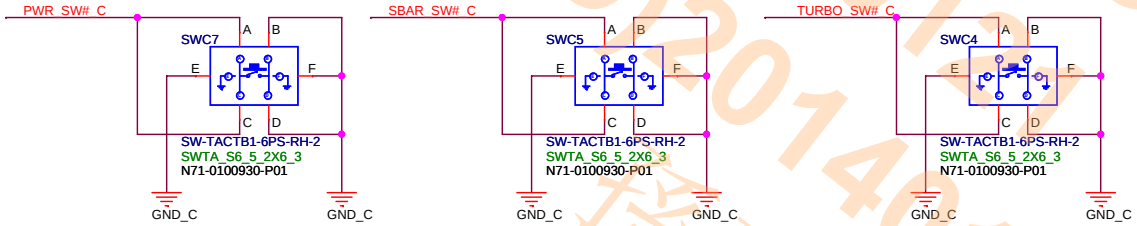


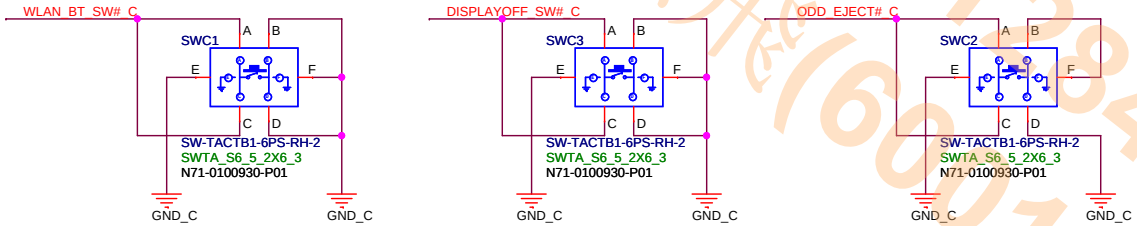
RC7 connection change from
+5VRUN_C to +5VSUS_C in 0B Ver .

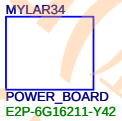


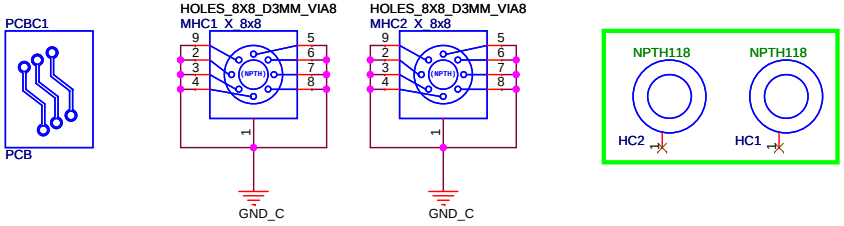


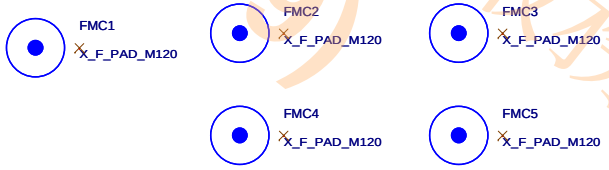












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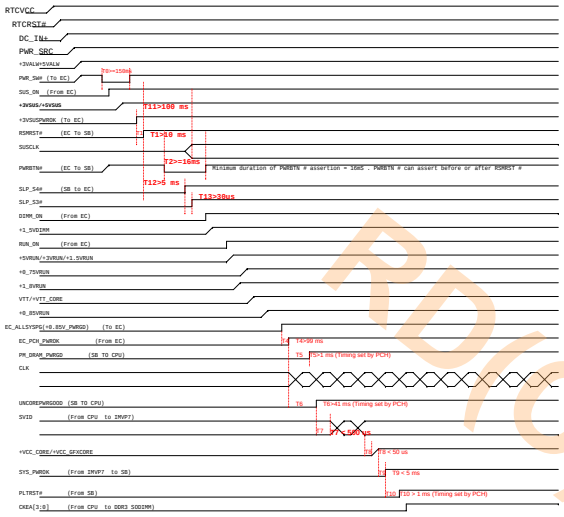
S5-S0

EC programming timing

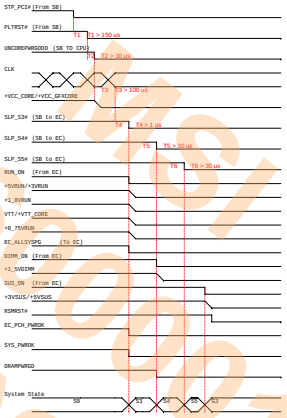
Intel Chief River timing SPEC



S0-S5

EC programming timing

Intel chief River timing SPEC



0705:

1 LOUTJB_3000

2 CHOKE_A3000

3 PWRCONN3000

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