Project Name :GK5CP5Z

Platform : CFL-HR+N18P-GX

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

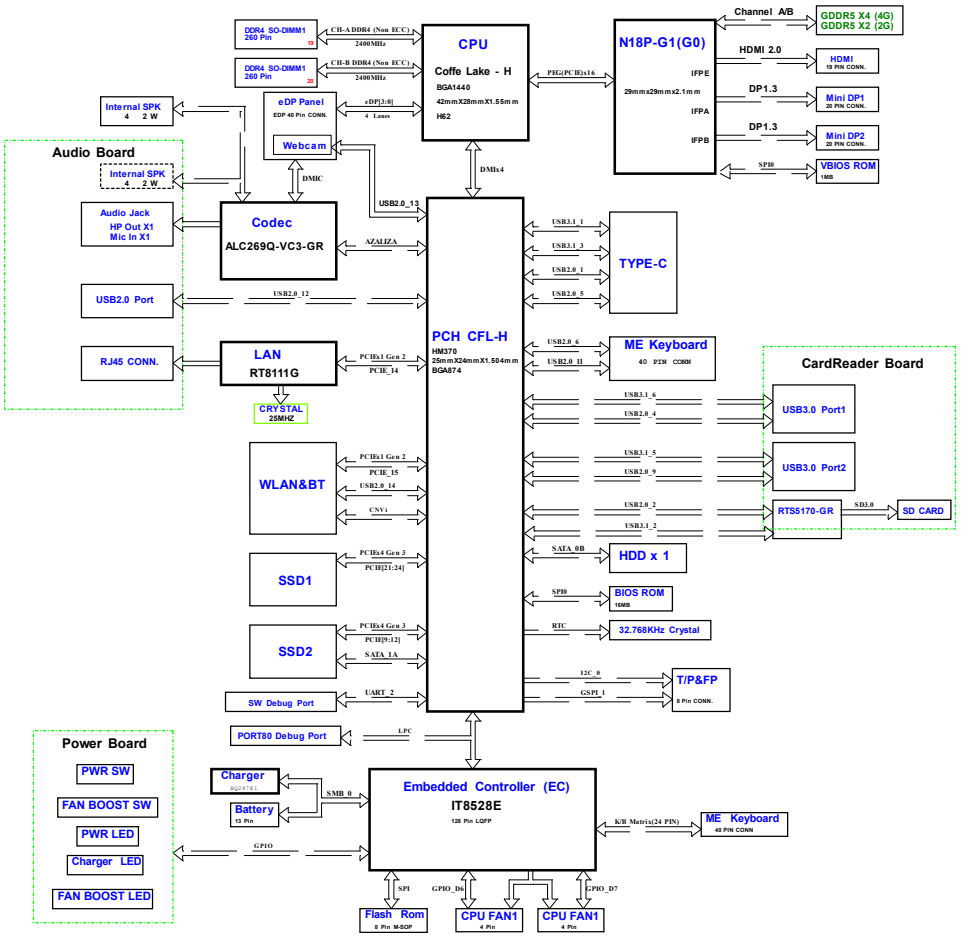
同方国际信息技术有限公司

Title: INDEX

Size: Custom | Document Number: GK5CP5Z | Rev: A

Date: Friday, November 02, 2018 | Sheet 1 of 61

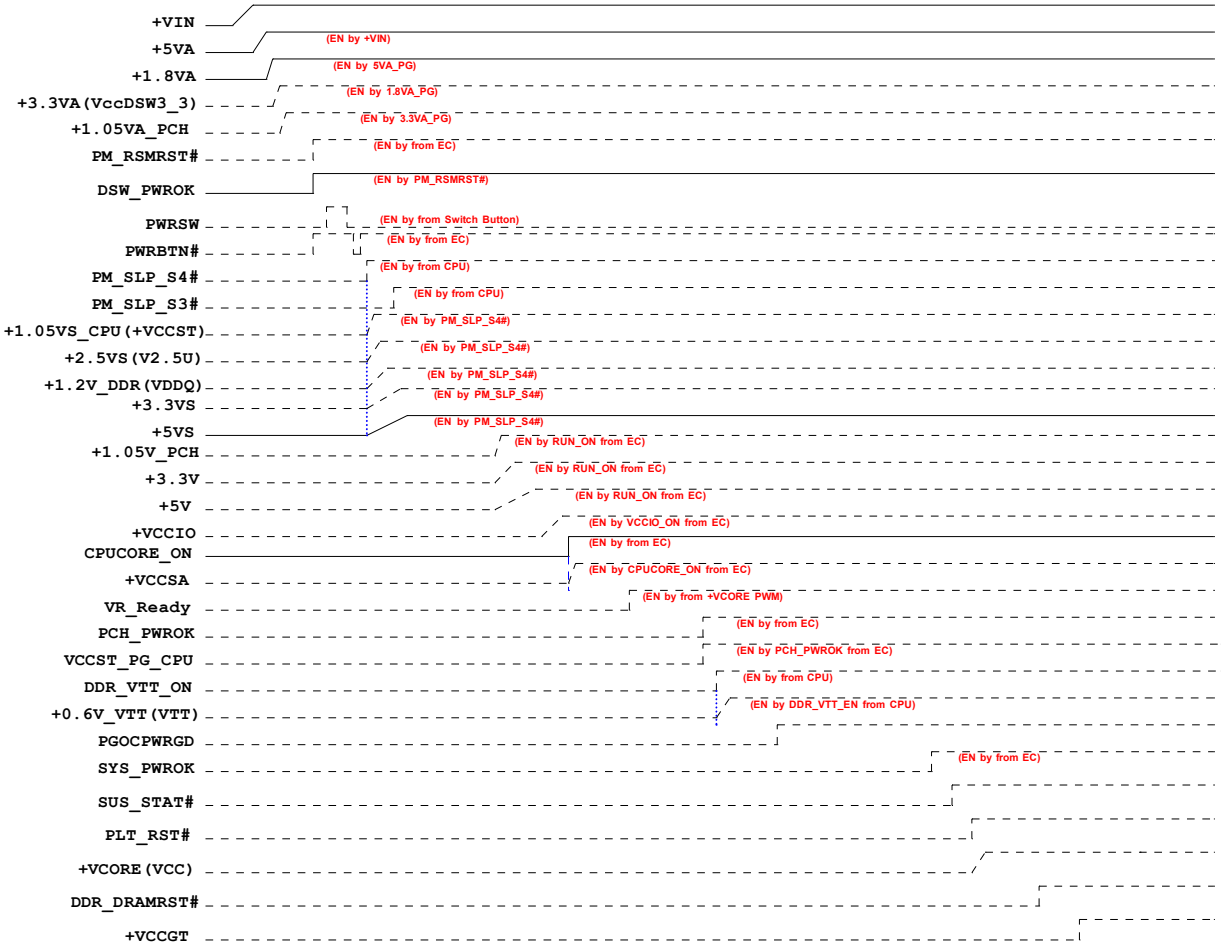
SYSTEM BLOCK DIAGRAM



SYSTEM BLOCK

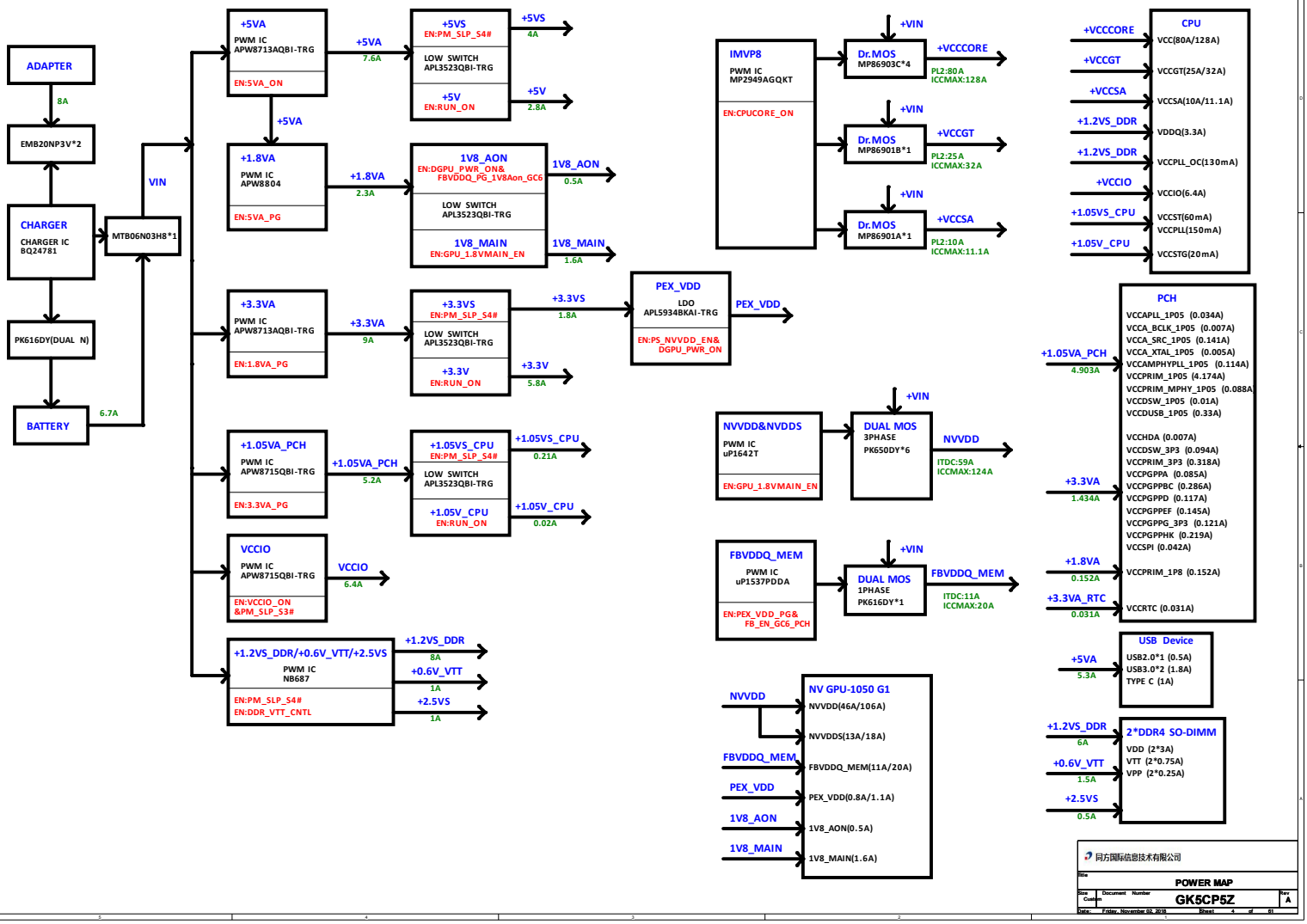
GK5CP5Z

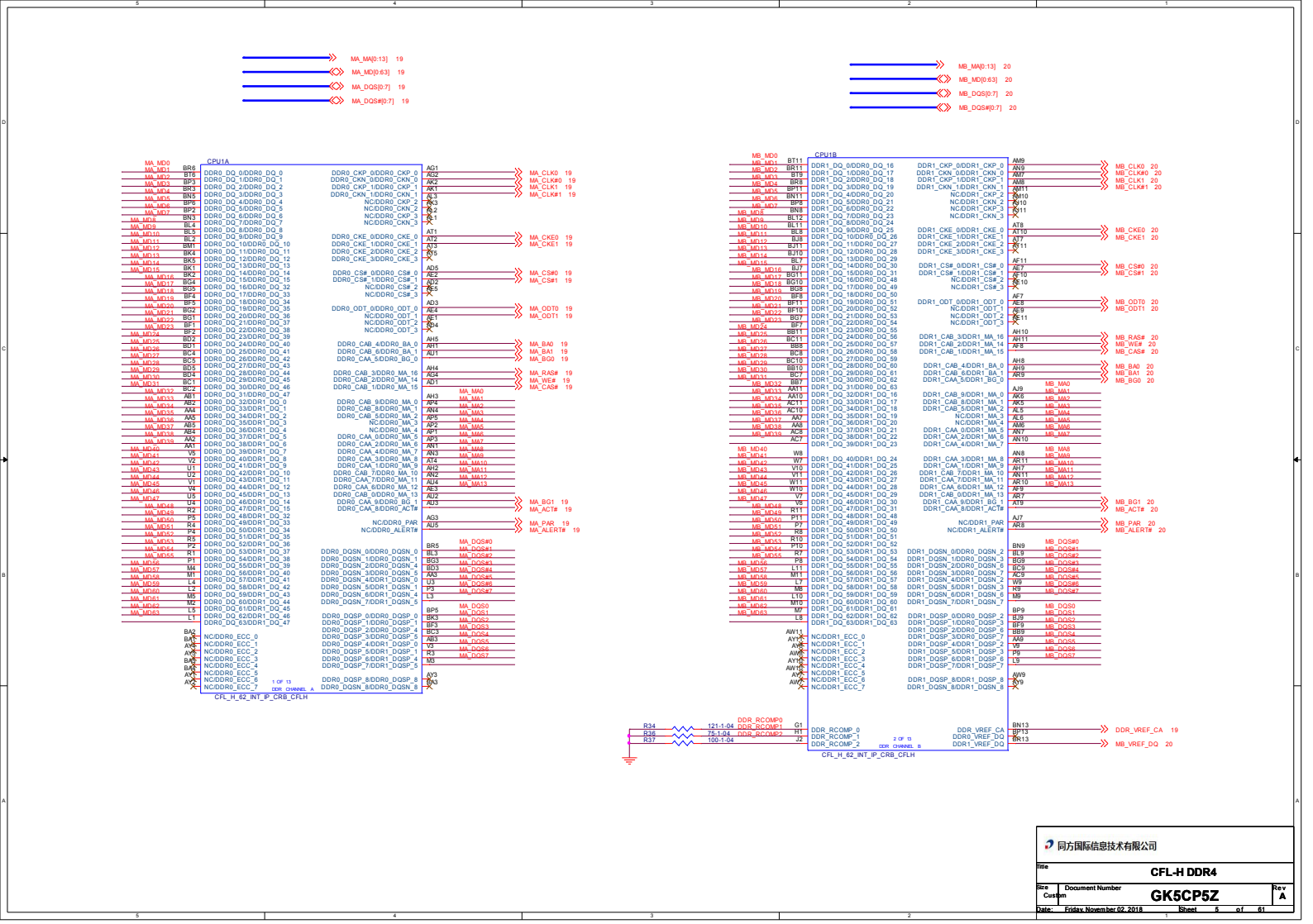
POWER ON SEQUENCE



同方国际信息技术有限公司

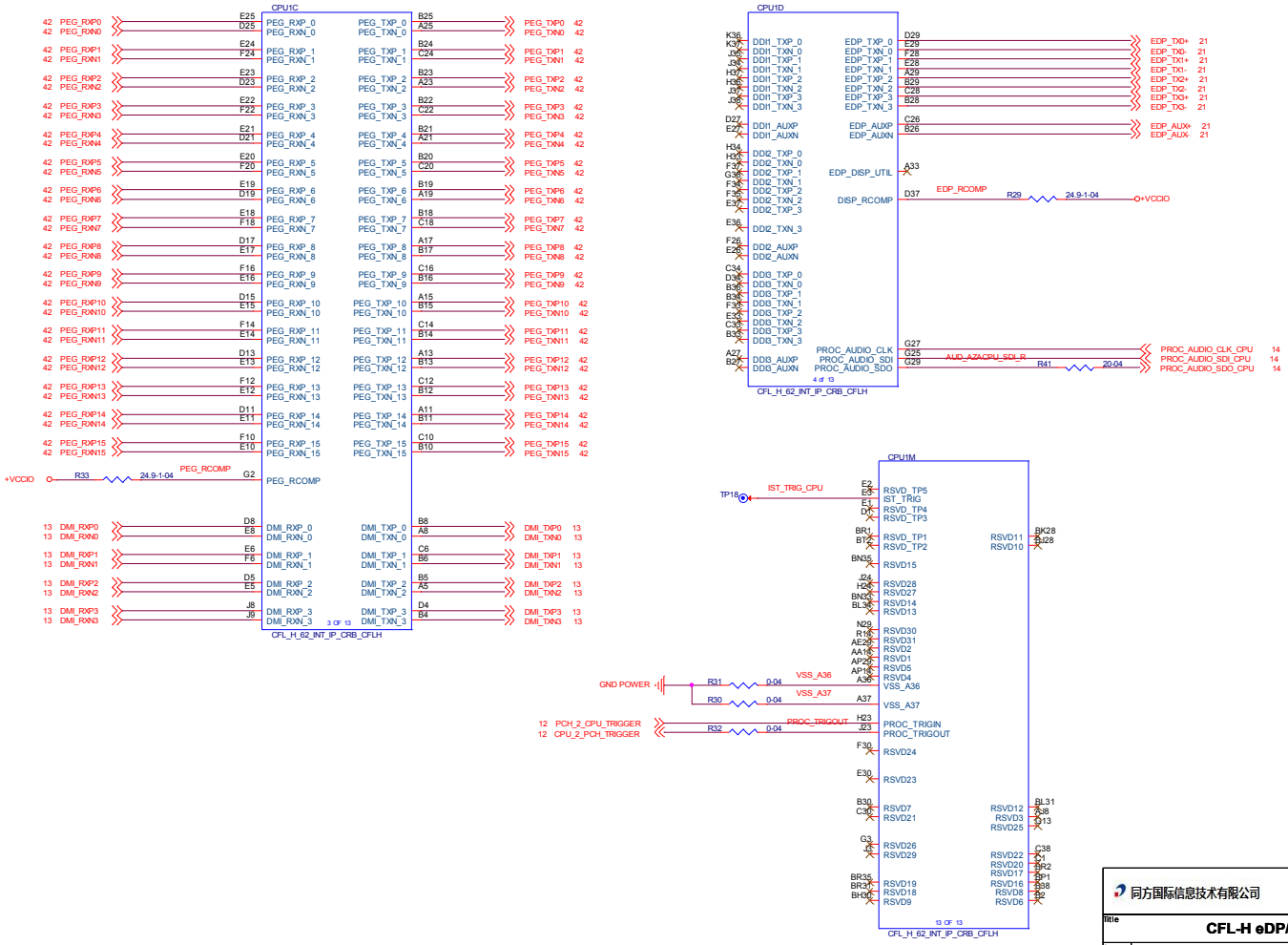
Title	POWER SEQUENCE	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 3 of 61	


ADAPTER
8A
EMB20NP3V*2
CHARGER
CHARGER IC
BQ24781
PK616DY(DUAL N)
BATTERY
6.7A
MTB06N03H8*1
VIN
+5VA
PWM IC
APW8713AQBI-TRG
EN:5VA_ON
7.6A
+5VS
EN:PM_SLP_S4#
LOW SWITCH
APL3523QBI-TRG
+5V
EN:RUN_ON
4A
2.8A
+1.8VA
PWM IC
APW8804
EN:5VA_PG
2.3A
1V8_AON
EN:DGPU_PWR_ON&
FBVDDQ_PG_1V8Aon_GC6
1V8_MAIN
EN:GPU_1.8VMAIN_EN
0.5A
1.6A
+3.3VA
PWM IC
APW8713AQBI-TRG
EN:1.8VA_PG
9A
+3.3VS
EN:PM_SLP_S4#
+3.3V
EN:RUN_ON
1.8A
5.8A
PEX_VDD
LDO
APL5934BKAI-TRG
EN:PS_NVVDD_EN&
DGPU_PWR_ON
+1.05VA_PCH
PWM IC
APW8715QBI-TRG
EN:3.3VA_PG
5.2A
+1.05VS_CPU
EN:PM_SLP_S4#
+1.05V_CPU
EN:RUN_ON
0.21A
0.02A
VCCIO
PWM IC
APW8715QBI-TRG
EN:VCCIO_ON
&PM_SLP_S3#
6.4A
+1.2VS_DDR/+0.6V_VTT/+2.5VS
PWM IC
NB687
EN:PM_SLP_S4#
EN:DDR_VTT_CNTL
8A
1A
1A
IMVP8
PWM IC
MP2949AGQKT
EN:CPUCORE_ON
Dr.MOS
MP86903C*4
Dr.MOS
MP86901B*1
Dr.MOS
MP86901A*1
+VIN
+VCCCORE
PL2:80A
ICCMAX:128A
+VCCGT
PL2:25A
ICCMAX:32A
+VCCSA
PL2:10A
ICCMAX:11.1A
NVVDD&NVDDS
PWM IC
uP1642T
EN:GPU_1.8VMAIN_EN
DUAL MOS
3PHASE
PK650DY*6
NVVDD
ITDC:59A
ICCMAX:124A
FBVDDQ_MEM
PWM IC
uP1537PDDA
EN:PEX_VDD_PG&
FB_EN_GC6_PCH
DUAL MOS
1PHASE
PK616DY*1
FBVDDQ_MEM
ITDC:11A
ICCMAX:20A
NV GPU-1050 G1
NVVDD
NVVDD(46A/106A)
NVVDDS(13A/18A)
FBVDDQ_MEM
FBVDDQ_MEM(11A/20A)
PEX_VDD
PEX_VDD(0.8A/1.1A)
1V8_AON
1V8_AON(0.5A)
1V8_MAIN
1V8_MAIN(1.6A)
CPU
+VCCCORE
VCC(80A/128A)
+VCCGT
VCCGT(25A/32A)
+VCCSA
VCCSA(10A/11.1A)
+1.2VS_DDR
VDDQ(3.3A)
+1.2VS_DDR
VCCPLL_OC(130mA)
+VCCIO
VCCIO(6.4A)
+1.05VS_CPU
VCCST(60mA)
VCCPLL(150mA)
+1.05V_CPU
VCCSTG(20mA)
PCH
+1.05VA_PCH
4.903A
VCCAPLL_1P05 (0.034A)
VCCA_BCLK_1P05 (0.007A)
VCCA_SRC_1P05 (0.141A)
VCCA_XTAL_1P05 (0.005A)
VCCAMPHYPLL_1P05 (0.114A)
VCCPRIM_1P05 (4.174A)
VCCPRIM_MPHY_1P05 (0.088A)
VCCDSW_1P05 (0.01A)
VCCDUSB_1P05 (0.33A)
VCCHDA (0.007A)
+3.3VA
1.434A
VCCDSW_3P3 (0.094A)
VCCPRIM_3P3 (0.318A)
VCCPGPPA (0.085A)
VCCPGPPBC (0.286A)
VCCPGPPD (0.117A)
VCCPGPPEF (0.145A)
VCCPGPPG_3P3 (0.121A)
VCCPGPPHK (0.219A)
VCCSPI (0.042A)
+1.8VA
0.152A
VCCPRIM_1P8 (0.152A)
+3.3VA_RTC
0.031A
VCCRTC (0.031A)
USB Device
+5VA
5.3A
USB2.0*1 (0.5A)
USB3.0*2 (1.8A)
TYPE C (1A)
2*DDR4 SO-DIMM
+1.2VS_DDR
6A
VDD (2*3A)
+0.6V_VTT
1.5A
VTT (2*0.75A)
+2.5VS
0.5A
VPP (2*0.25A)
同方国际信息技术有限公司
POWER MAP
GK5CP5Z
A
Friday, November 02, 2018
4
of
61



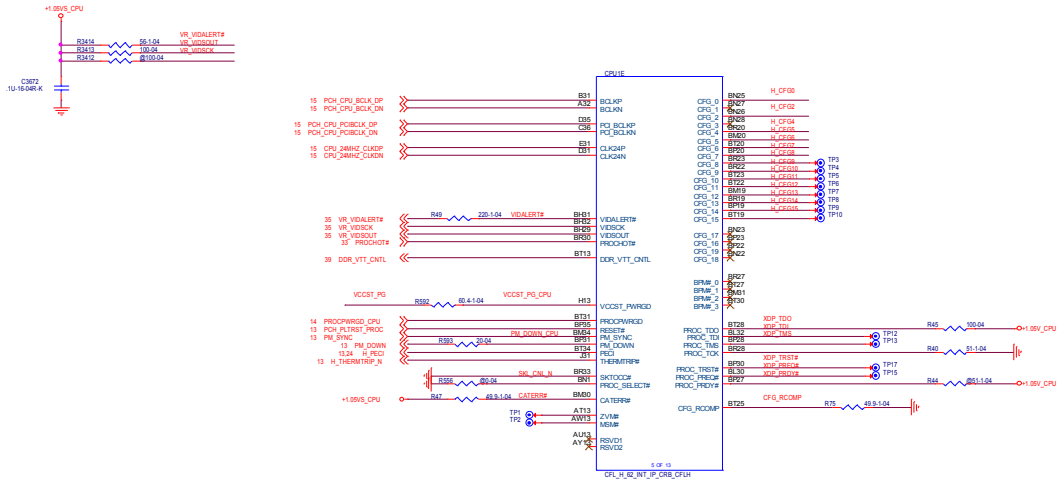
同方国际信息技术有限公司

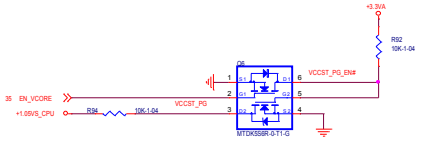
Title	CFL-H DDR4		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Friday, November 02, 2018	Sheet 5 of 61		

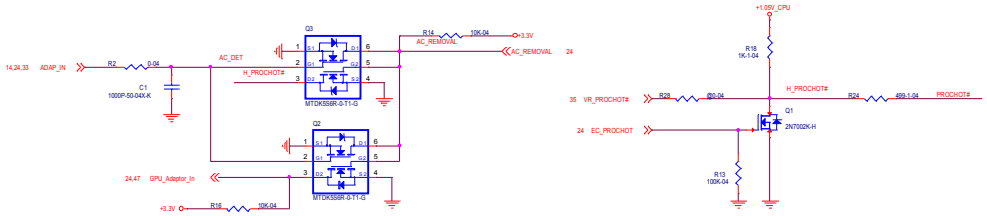


同方国际信息技术有限公司

Title	CFL-H eDP/PEX/DMI/RSVD		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Friday, November 02, 2018	Sheet 6 of 61		







H_CFG0 (IPU)	Stall reset sequence after PCU PLL lock until de-asserted
0	Stall
1	Normal Operation No stall. (Default)

H_CFG0 R180 @1K-1-04

H_CFG2 (IPU)	PCI Express* Static x16 Lane Numbering Reversal
0	Lane numbers reversed
1	Normal operation

H_CFG2 R181 1K-1-04

H_CFG4 (IPU)	eDP Presence strap
0	Enabled
1	Disabled

H_CFG4 R172 1K-1-04

H_CFG6 (IPU)	H_CFG5 (IPU)	PCI Express* Bifurcation
0	0	1 x8, 2 x4 PCI Express
0	1	reserved
1	0	2 x8 PCI Express
1	1	1 x16 PCI Express

H_CFG5 R174 @1K-1-04
H_CFG6 R173 @1K-1-04

H_CFG7 (IPU)	PEG Training
0	PEG Wait for BIOS for training
1	PEG Train immediately following RESET# de assertion (Default)

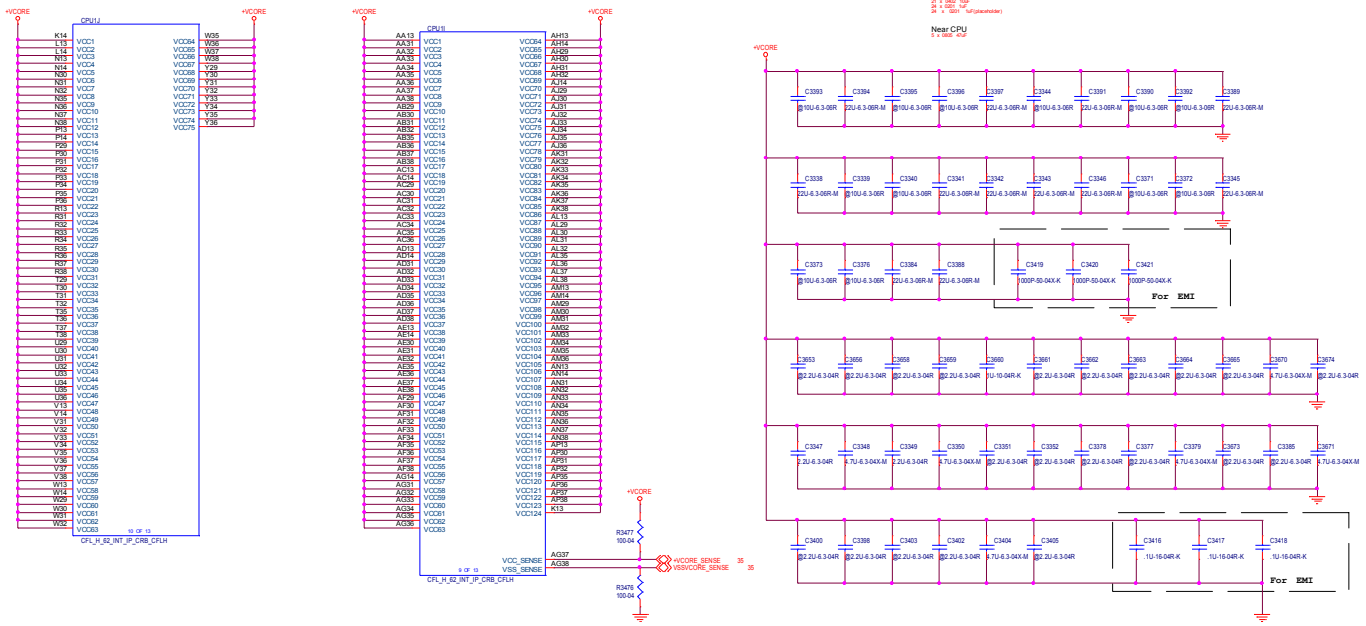
H_CFG7 R175 @1K-1-04

同方国际信息技术有限公司

Title: CFL-H MISC/CLK/JTAG/CFG

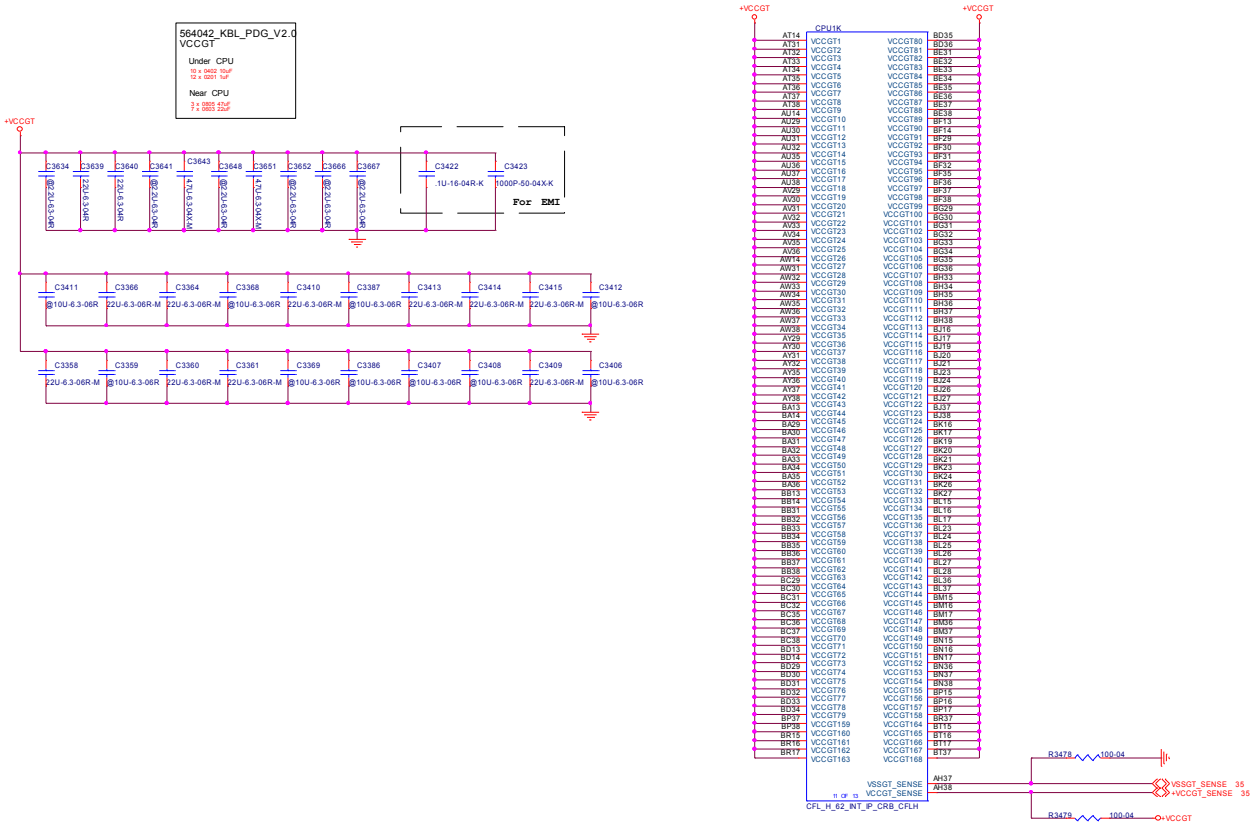
Size: Custom | Document Number: GK5CP5Z | Rev: A

Date: Friday, November 02, 2018 | Sheet 7 of 61



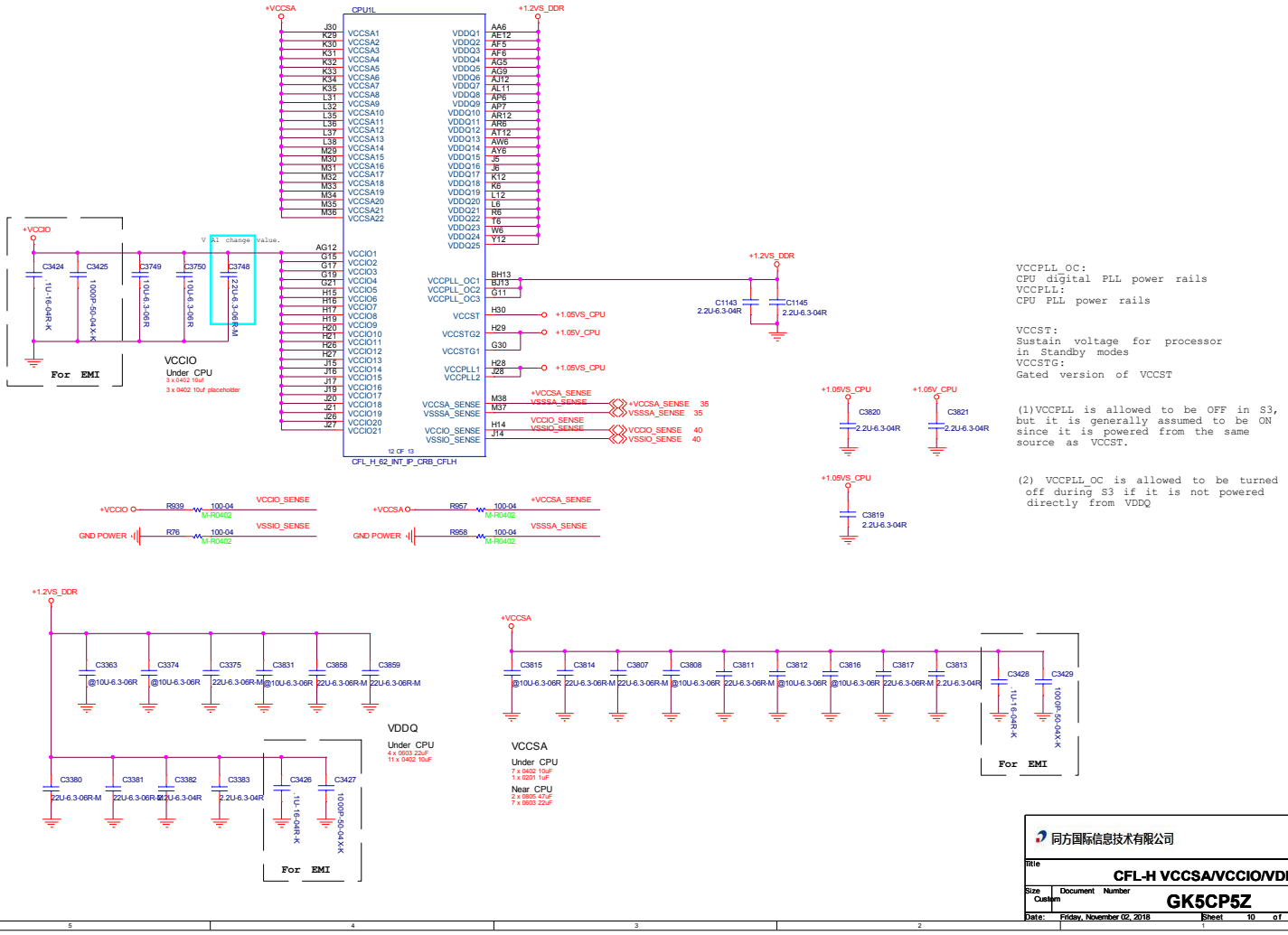
同方国际信息技术有限公司

Title	CFL-H VCORE	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 8 of 61	



同方国际信息技术有限公司

Title	CFL-H VCCGT		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Friday, November 02, 2018	Sheet 9 of 61		



VCCPLL_OC:
CPU digital PLL power rails
VCCPLL:
CPU PLL power rails

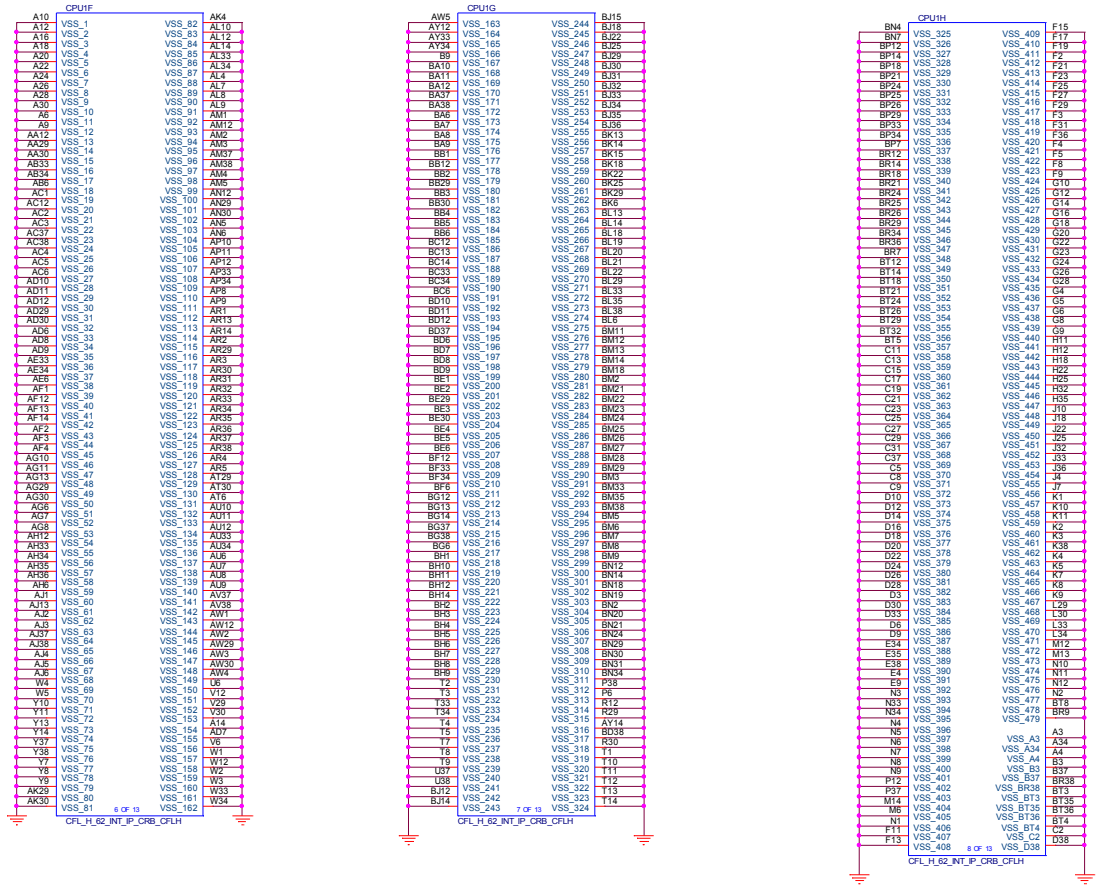
VCCST:
Sustain voltage for processor in Standby modes
VCCSTG:
Gated version of VCCST

(1)VCCPLL is allowed to be OFF in S3, but it is generally assumed to be ON since it is powered from the same source as VCCST.

(2) VCCPLL_OC is allowed to be turned off during S3 if it is not powered directly from VDDQ

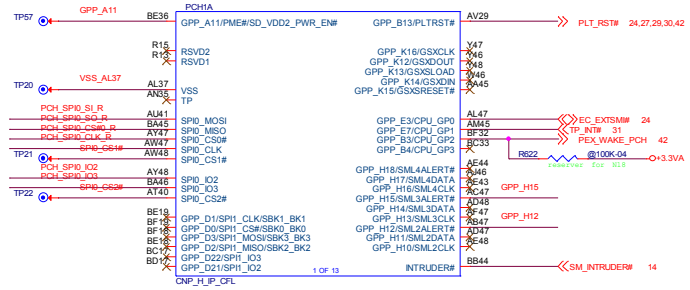
同方国际信息技术有限公司

Title	CFL-H VCCSA/VCCIO/VDDQ	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 10 of 61	



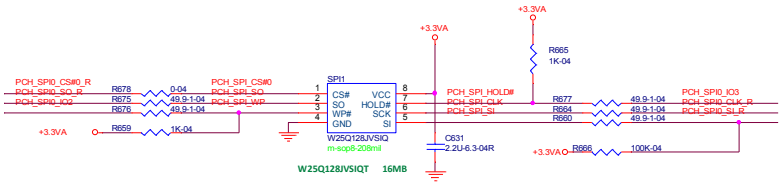
同方国际信息技术有限公司

Title	CFL-H GND	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 11 of 61	

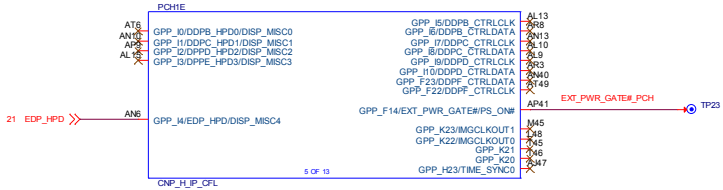


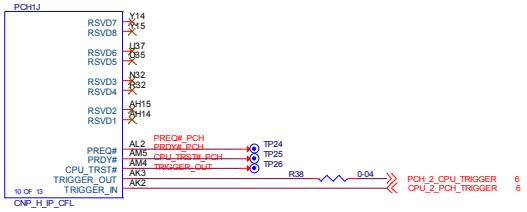
GPP_H15
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

GPP_H12	eSPI Flash Sharing Mode
0	Master Attached Flash Sharing (MAFS) enabled (Default)
1	Slave Attached Flash Sharing (SAFS) enabled



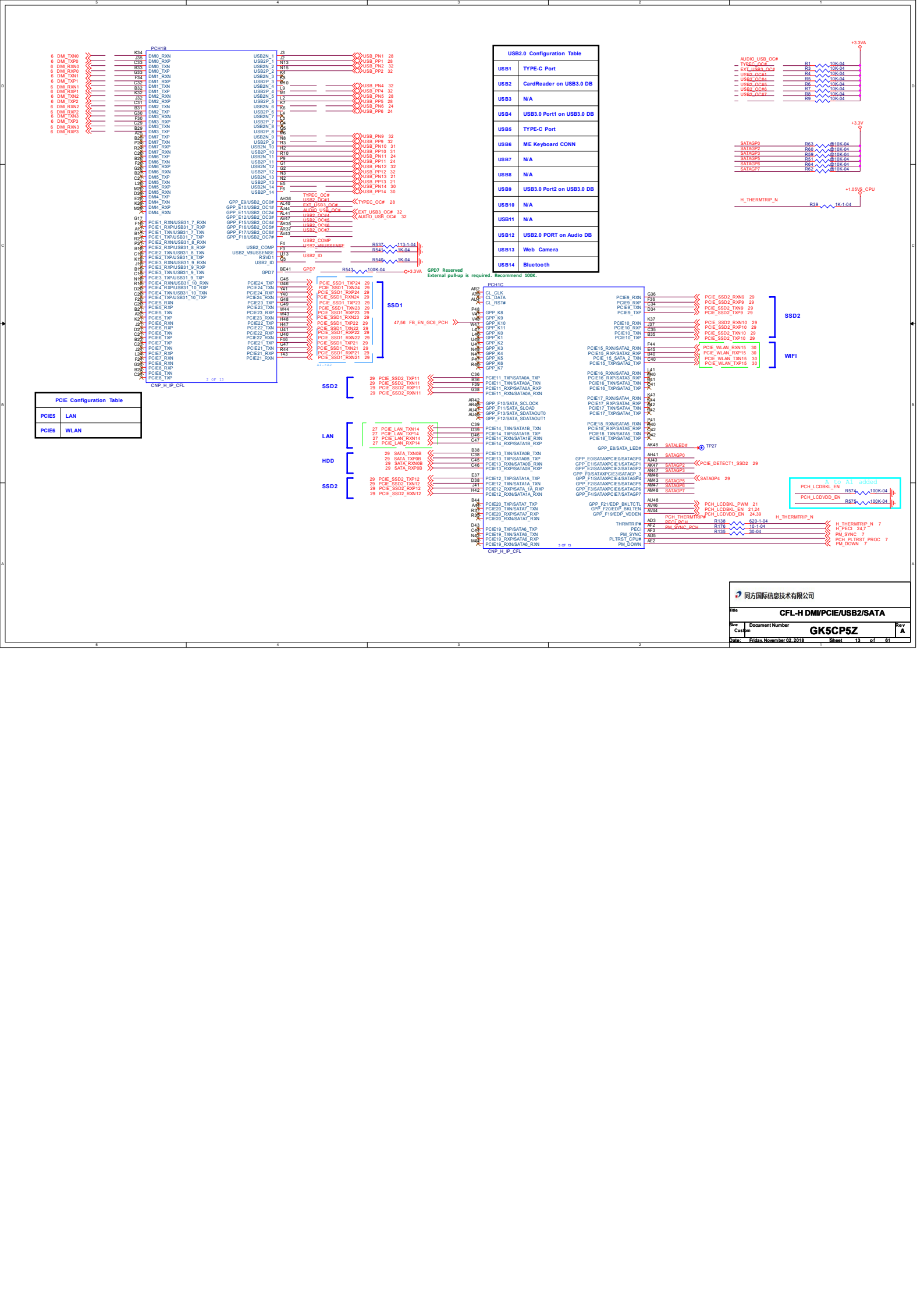
SPI0_MOSI
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

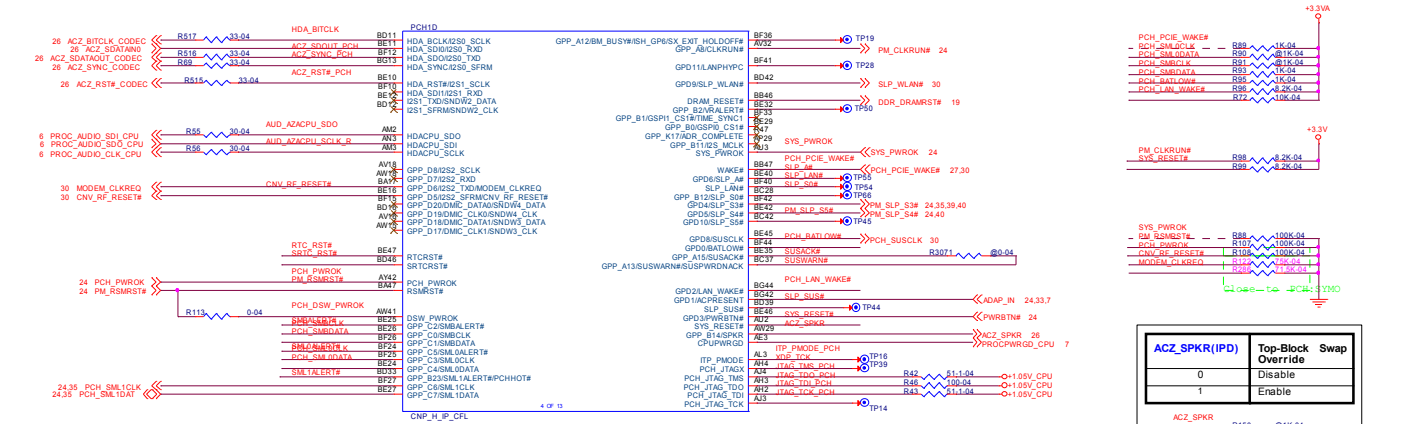




同方国际信息技术有限公司

Title	CFL-H SPI/DDI CTRL/RSVD	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 12 of 61	


PCH1B
PCH1C
CNP_H_IP_CFL
USB2.0 Configuration Table
USB1 TYPE-C Port
USB2 CardReader on USB3.0 DB
USB3 N/A
USB4 USB3.0 Port1 on USB3.0 DB
USB5 TYPE-C Port
USB6 ME Keyboard CONN
USB7 N/A
USB8 N/A
USB9 USB3.0 Port2 on USB3.0 DB
USB10 N/A
USB11 N/A
USB12 USB2.0 PORT on Audio DB
USB13 Web Camera
USB14 Bluetooth
PCIE Configuration Table
PCIE5 LAN
PCIE6 WLAN
SSD1
SSD2
LAN
HDD
WIFI
GPD7 Reserved
External pull-up is required. Recommend 100K.
A_to_A1 added
同方国际信息技术有限公司
CFL-H DMI/PCIE/USB2/SATA
GK5CP5Z
Rev A
Friday, November 02, 2018
Sheet 13 of 61



ACZ_SPKR(IPD)	Top-Block Swap Override
0	Disable
1	Enable

ACZ_SPKR R150 @1K-04 +3.3V

HDA_SDO (IPD)	Flash Descriptor Security Override
0	ME Enable security (Default)
1	ME Disabled security

+3.3VA R154 @1K-1-04 ACZ_SDOUT_PCH
24 MELOCK# R106 1K-1-04

SMBALERT#(IPD)	Intel ME Crypto Transport Layer Security Confidentiality (TLS)
0	Disable (Default)
1	Enable

+3.3VA R67 @4.7K-04 SMBALERT#

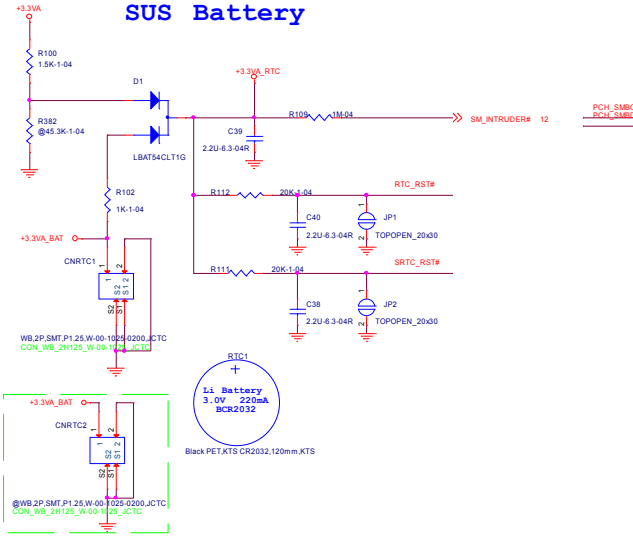
SML0ALERT#(IPD)	eSPI&LPC Select
0	LPC (Default)
1	eSPI

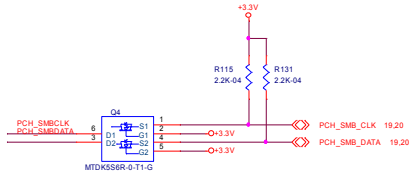
+3.3VA R77 @4.7K-04 SML0ALERT#

SML1ALERT#(IPD)	IntelR DCI-OOB
0	Disable (Default)
1	Enable

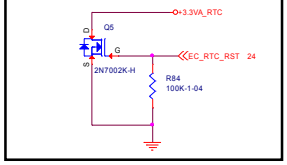
+3.3VA R78 @4.7K-04 SML1ALERT#

SUS Battery



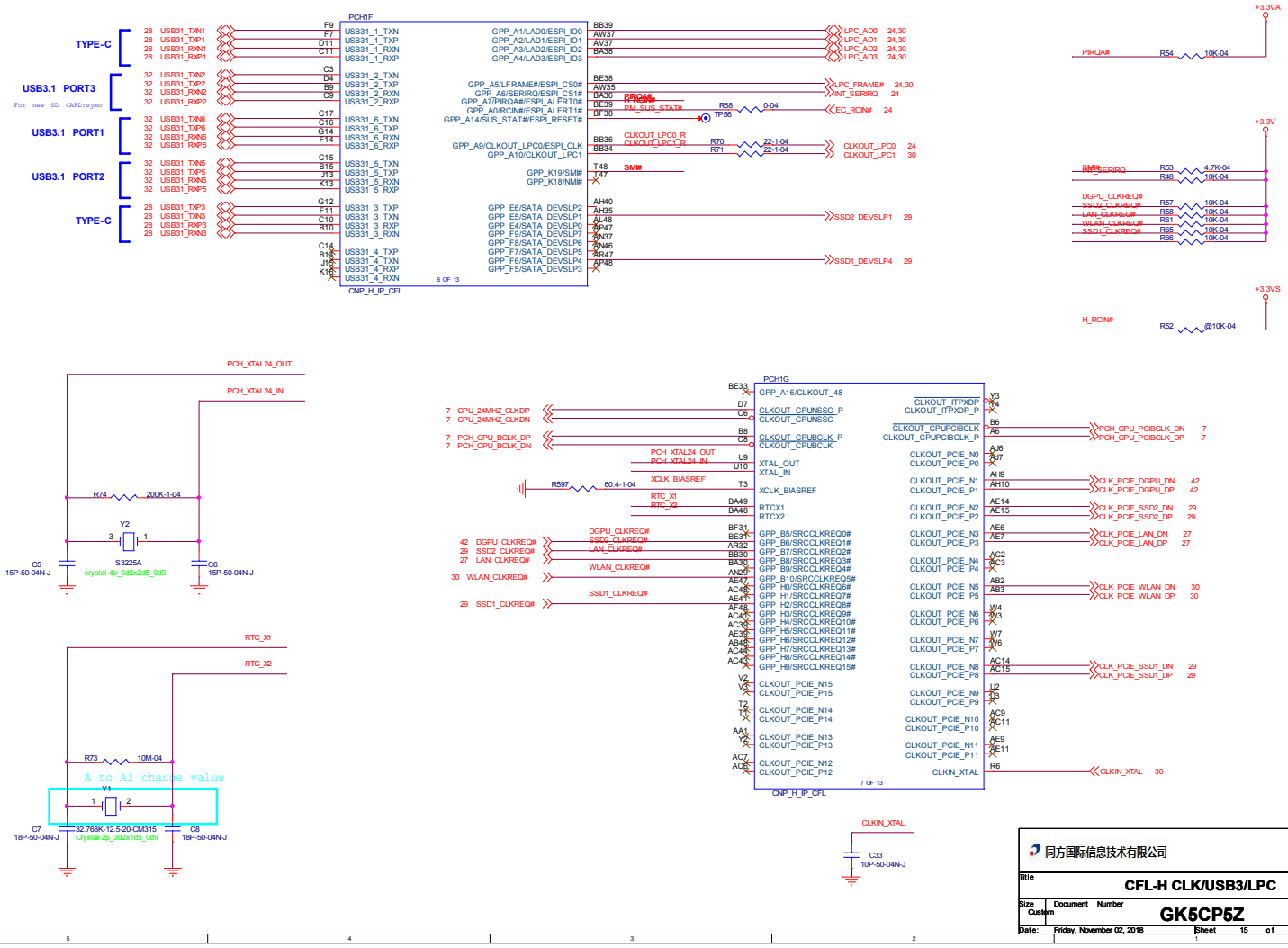


CLEAR CMOS



同方国际信息技术有限公司

Title	CFL-H PM/HDA/SMBUS/RTC		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Friday, November 02, 2018	Sheet 14 of 61		


PCH1F
TYPE-C
USB3.1 PORT3
USB3.1 PORT1
USB3.1 PORT2
TYPE-C
CNP_H_IP_CFL
6 OF 13
PCH1G
CNP_H_IP_CFL
7 OF 13
+3.3VA
+3.3V
+3.3VS
PCH_XTAL24_OUT
PCH_XTAL24_IN
RTC_X1
RTC_X2
A to A1 change value
CLKIN_XTAL
同方国际信息技术有限公司
CFL-H CLK/USB3/LPC
GK5CP5Z
Friday, November 02, 2018

GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Destination
0	SPI (Default)
1	LPC

+3.3VO R545 @150K-04 PCH_GSPI1_SI_R

GPP_B18/GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable

+3.3VO R546 @4.7K-04 GPP_B18

CNV_BRI_DT (IPD)	XTAL Frequency Select
0	38.4MHz XTAL frequency
1	24MHz XTAL frequency (Default)

+VCCPRIM_1P8 R610 10K-04 CNV_BRI_DT_PCH

CNV_RGI_DT	M.2 CNV Mode Select
0	Integrated CNVi enable
1	Integrated CNVi disable

CNV_RGI_DT_PCH

R617 @100K-04

+VCCPRIM_1P8 R615 20K-04 CNV_BRI_RSP

R656 20K-04 CNV_RGI_RSP

Close to PCH:SYMO

A to A1 added

39 MEM_OVERCLK_EN R572 0-04 PCH_GSPI1_SI_R

58 OVRM_TGP_SEL R573 @0-04 GPP_B18

PCH1K

BA26 GPP_B22/GSPI1_MOSI
BD30 GPP_B21/GSPI1_MISO
AU26 GPP_B20/GSPI1_CLK
AW26 GPP_B19/GSPI1_CS0#
BE30 GPP_B18/GSPI0_MOSI
BD29 GPP_B17/GSPI0_MISO
BF25 GPP_B16/GSPI0_CLK
BB26 GPP_B15/GSPI0_CS0#

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# BA20
GPP_D10/ISH_SPI_CLK/GSPI2_CLK BB20
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO BB16
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI AN18
GPP_D16/ISH_UART0_CTS#/CNV_WCEN BF14
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN AR18
GPP_D14/ISH_UART0_TXD/I2C2_SCL BF17
GPP_D13/ISH_UART0_RXD/I2C2_SDA BE17

24 SMC_WAKE_SCI# BB24 GPP_C9/UART0_TXD
55,56 FBVDDQ_PG_1VBAon_GC6 BE23 GPP_C8/UART0_RXD
AP23 GPP_C11/UART0_CTS#
BA24 GPP_C10/UART0_RTS#

24,53,55 Dgpu_PWR_ON BD21 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AW24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AP21 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU24 GPP_C12/UART1_RXD/ISH_UART1_RXD

GPP_H20/ISH_I2C0_SCL AG45
GPP_H19/ISH_I2C0_SDA AG46
GPP_H22/ISH_I2C1_SCL AH47
GPP_H21/ISH_I2C1_SDA AN48

30 UART2_DEBUG_TXD AV21 GPP_C23/UART2_CTS#
30 UART2_DEBUG_RXD AW25 GPP_C22/UART2_RTS#
BE20 GPP_C21/UART2_TXD
BD20 GPP_C20/UART2_RXD

47 GPU_EVENT#_GC6 BE21 GPP_C19/I2C1_SCL
42 DGPU_RST# BF21 GPP_C18/I2C1_SDA
31 TP_I2C0_SCL BC22 GPP_C17/I2C0_SCL
31 TP_I2C0_SDA BF23 GPP_C16/I2C0_SDA

GPP_A23/ISH_GP5 AV34
GPP_A22/ISH_GP4 AW32
GPP_A21/ISH_GP3 BA33
GPP_A20/ISH_GP2 BB34
GPP_A19/ISH_GP1 BB35
GPP_A18/ISH_GP0 BB38
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7

BE15 GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
BE13 GPP_D23/ISH_I2C2_SCL/I2C3_SCL

11 OF 13

CNP_H_IP_CFL

PCH1M

AW13 GPP_G0/SD_CMD
BE5 GPP_G1/SD_D0
BH5 GPP_G2/SD_D1
BF5 GPP_G3/SD_D2
BC5 GPP_G4/SD_D3
BE5 GPP_G5/SD_CD#
BD5 GPP_G6/SD_CLK
AV5 GPP_G7/SD_WP

AP3 GPP_I11/M2_SKT2_CFG0
AK3 GPP_I12/M2_SKT2_CFG1
AN3 GPP_I13/M2_SKT2_CFG2
AM3 GPP_I14/M2_SKT2_CFG3

TP11 VCCIO_PWR_GATE#
AV8 GPP_J0/CNV_PA_BLANKING
AR11 GPP_J1/CPU_VCCIO_PWR_GATE#
AV3 GPP_J11/AWP_PRESENT
AW3 GPP_J10
AT10 GPP_J_2
AV6 GPP_J_3

30 CNV_BRI_DT R612 33-04 CNV_BRI_DT_PCH
30 CNV_BRI_RSP
30 CNV_RGI_DT R614 33-04 CNV_RGI_DT_PCH
30 CNV_RGI_RSP

AV2 GPP_J_4_CNV_BRI_DT_UART0_RTSB
BA4 GPP_J5/CNV_BRI_RSP/UART0_RXD
AV3 GPP_J6/CNV_RGI_DT/UART0_TXD
AW2 GPP_J7/CNV_RGI_RSP/UART0_CTS#
AU9 GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD

GPP_J9

CNV_WR_CLKN BD4
CNV_WR_CLKP BE3
CNV_WR_D0N BB3
CNV_WR_D0P BB4
CNV_WR_D1N BA3
CNV_WR_D1P BA2
CNV_WT_CLKN BC5
CNV_WT_CLKP BB6
CNV_WT_D0N BE6
CNV_WT_D0P BD7
CNV_WT_D1N BC6
CNV_WT_D1P BF6
CNV_WT_RCOMP BA1

CNV_WR_CLKN 30
CNV_WR_CLKP 30
CNV_WR_D0N 30
CNV_WR_D0P 30
CNV_WR_D1N 30
CNV_WR_D1P 30
CNV_WT_CLKN 30
CNV_WT_CLKP 30
CNV_WT_D0N 30
CNV_WT_D0P 30
CNV_WT_D1N 30
CNV_WT_D1P 30

CNV_WT_RCOMP R598 150-1-04 PCIE_RCOMPN

PCIE_RCOMPN B12
PCIE_RCOMPP A13
SD_RCOMP_1P8 BE5
SD_RCOMP_1P8 BE4
SD_RCOMP_3P3 BD1
GPPJ_RCOMP_1P81 BE1
GPPJ_RCOMP_1P82 BE2
GPPJ_RCOMP_1P83

PCIE_RCOMPP R596 100-1-04
SD_RCOMP_1P8 R599 200-1-04
SD_RCOMP_3P3 R600 200-1-04
GPPJ_RCOMP_1P8 R606 200-1-04

RSVD2 V35
RSVD3 V36
RSVD1 BC1
TP AL35 TP58

15 OF 13

CNP_H_IP_CFL

GPP_J9	VCCPSPI Rail select
0	VCCSPI is connected to 3.3V
1	VCCSPI is connected to 1.8V

+VCCPRIM_1P8 R611 @4.7K-04 GPP_J9

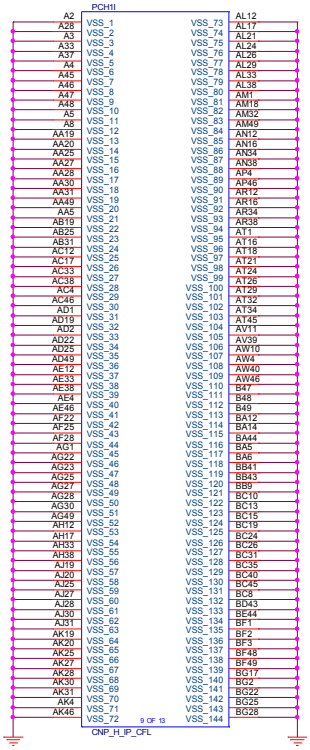
同方国际信息技术有限公司

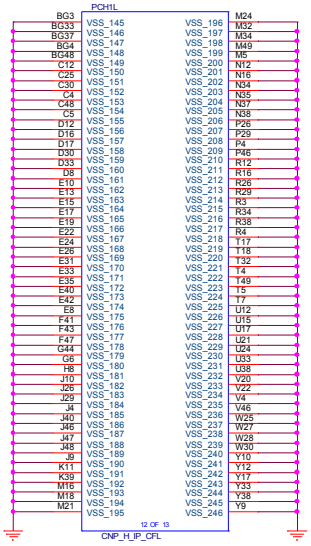
Title: CFL-H CNV/UART/I2C

Size: Custom | Document Number: GK5CP5Z | Rev: A

Date: Sunday, November 25, 2018 | Sheet 16 of 61

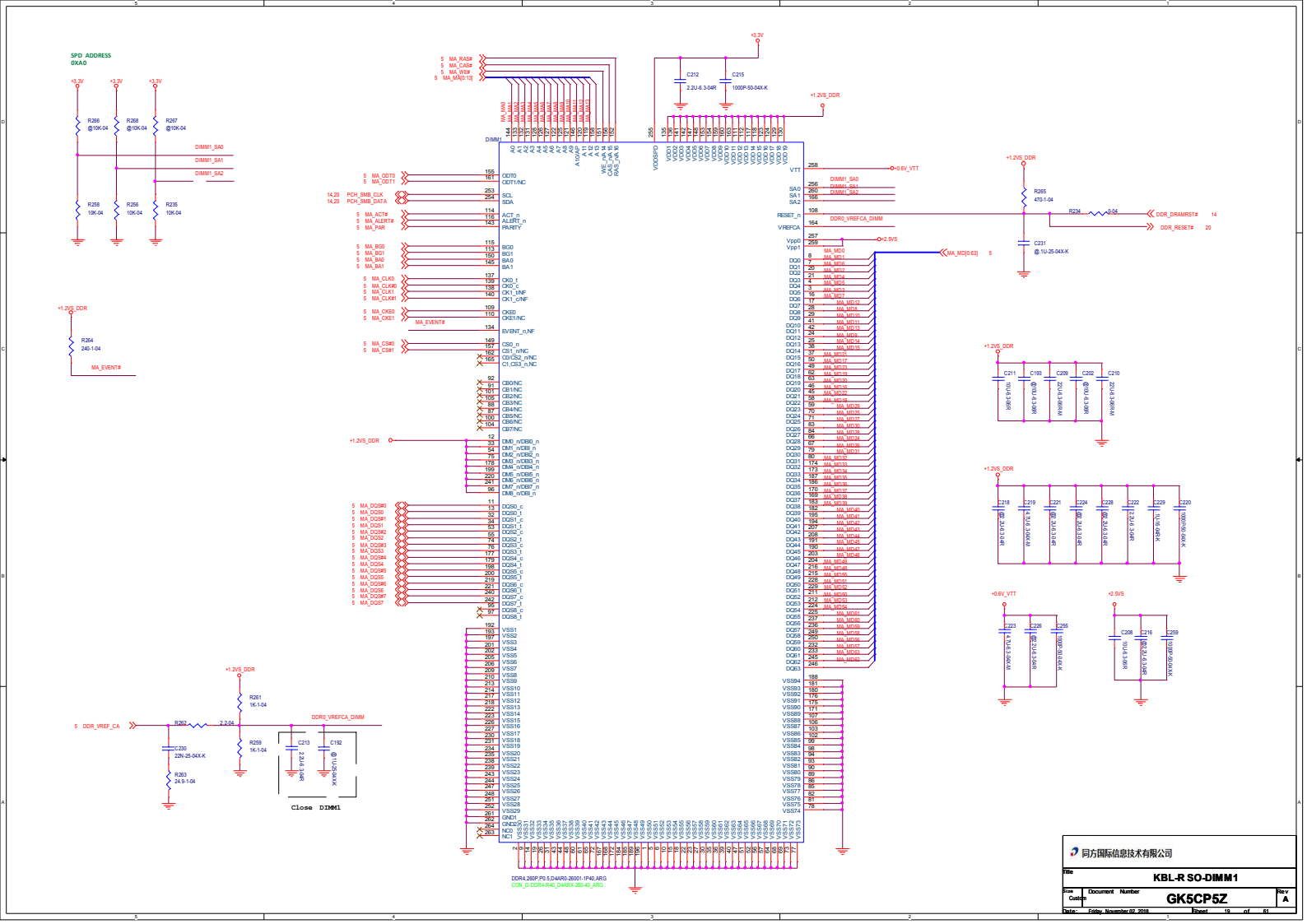

PCH1H
CNP_H_IP_CFL
8 OF 13
For EMI
VCCPRIM_3P3
For EMI
VCCPGPPEF
VCCPGPPD
VCCPGPPBC
VCCSPI
VCCDUSB_1P05
VCCPRIM_MPHY_1P05
VCCA_XTAL_1P05
VCCA_SRC_1P05
VCCPGPPA
VCCDSW_3P3
+VCCPRIM_1P8
VCCPHVLDO_1P8
VCCDPHY_1P24
VPHY_1P24
同方国际信息技术有限公司
CFL-H POWER
GK5CP5Z
Friday, November 02, 2018
17 of 61

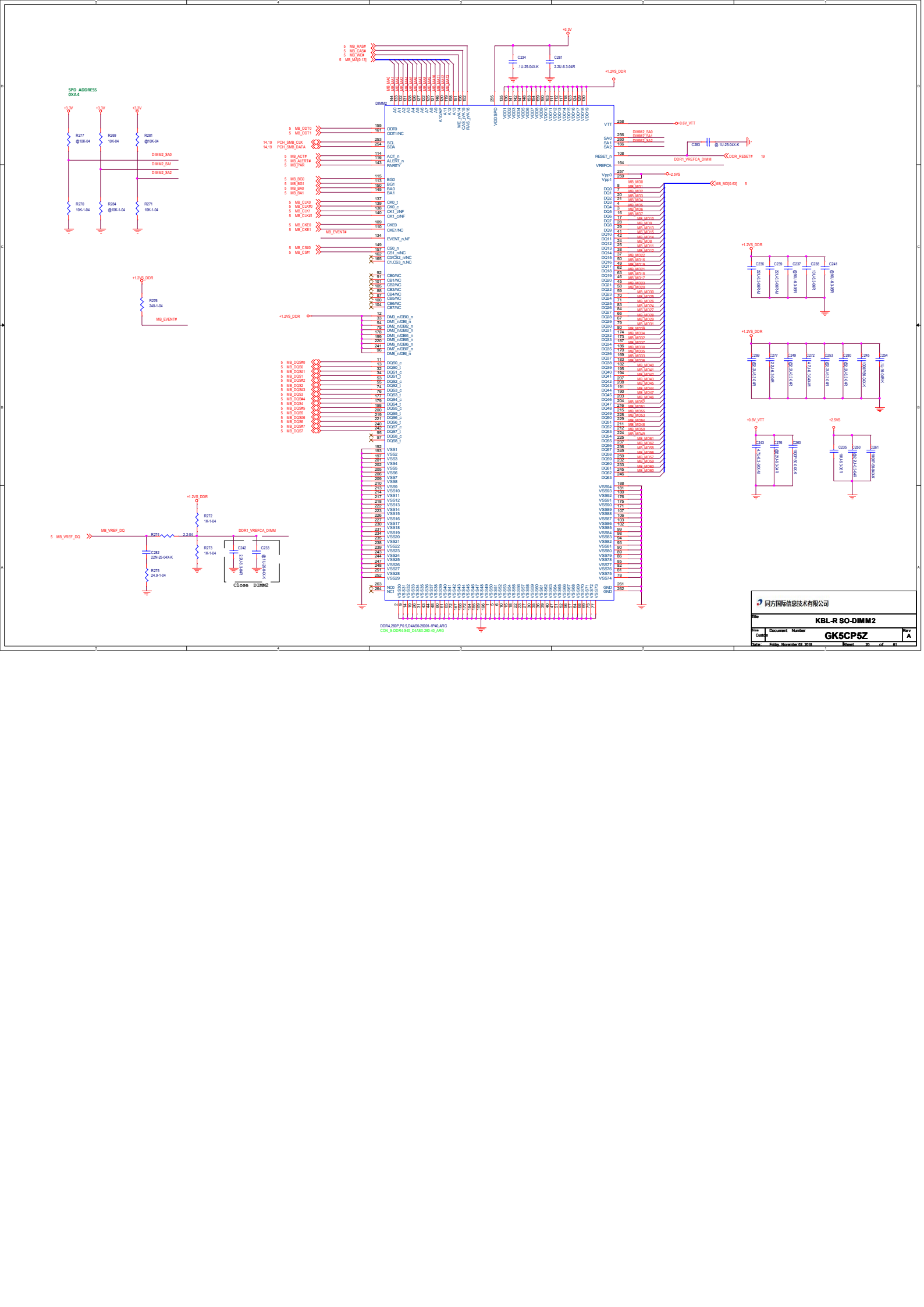


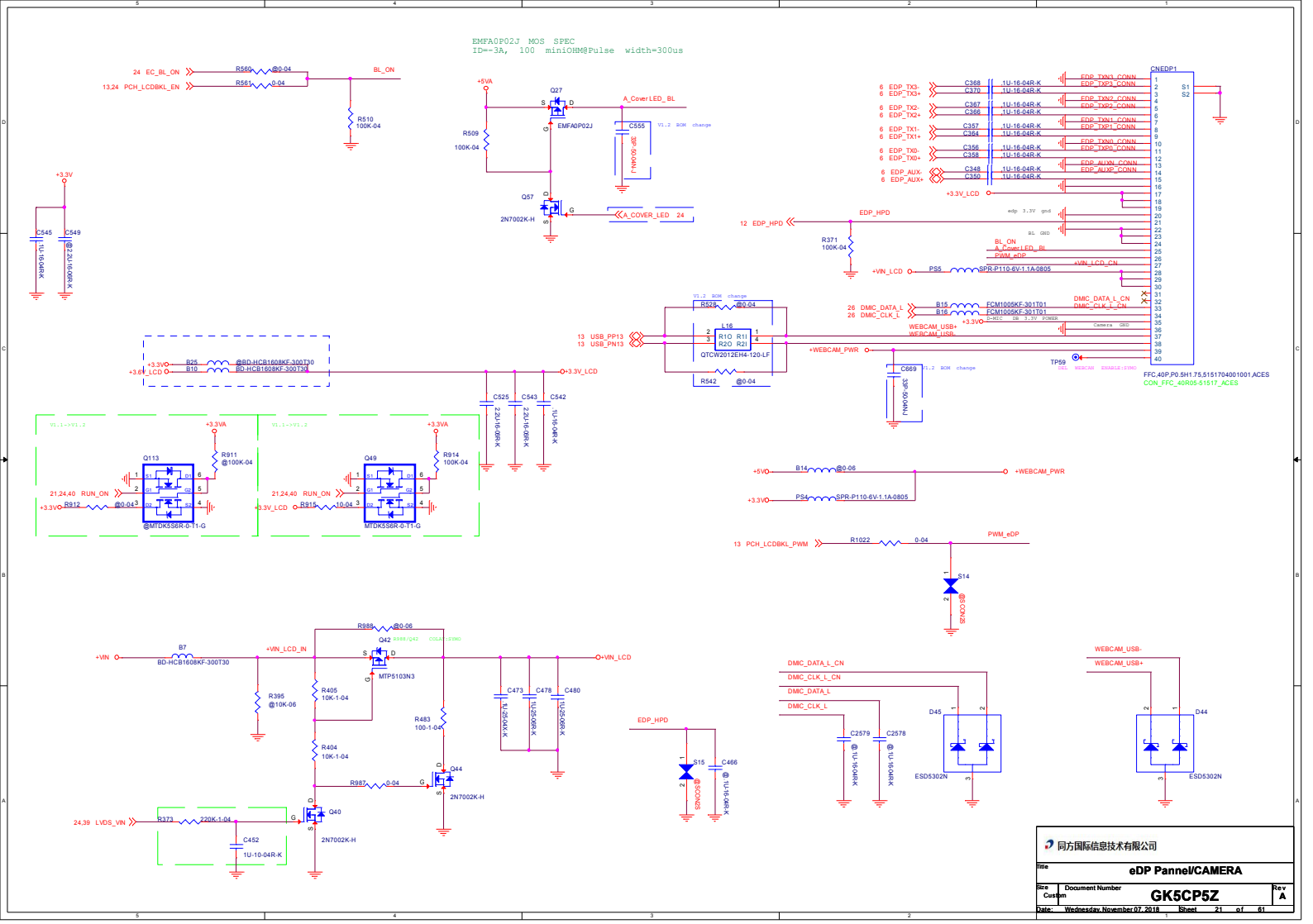


同方国际信息技术有限公司

title	CFL-H GND	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 18 of 61	


SPD ADDRESS
0XA0
DIMM1
Close DIMM1
DDR4_260P.P0.5.D4ARS-26001-1P40_ARG
CON_D-DDR4-R40_D4ARX-260-40_ARG
同方国际信息技术有限公司
KBL-R SO-DIMM1
GK5CP5Z
Custom
Document Number
Rev
A
Date: Friday, November 02, 2018
Sheet 19 of 61


SPD ADDRESS
0XA4
DIMM2_SA0
DIMM2_SA1
DIMM2_SA2
Close DIMM2
DDR4_260P_P0.5_D4AS0-26001-1P40_ARG
CON_S-DDR4-S40_D4ASX-260-40_ARG
同方国际信息技术有限公司
KBL-R SO-DIMM2
GK5CP5Z
Rev A
Friday, November 02, 2018
Sheet 20 of 61

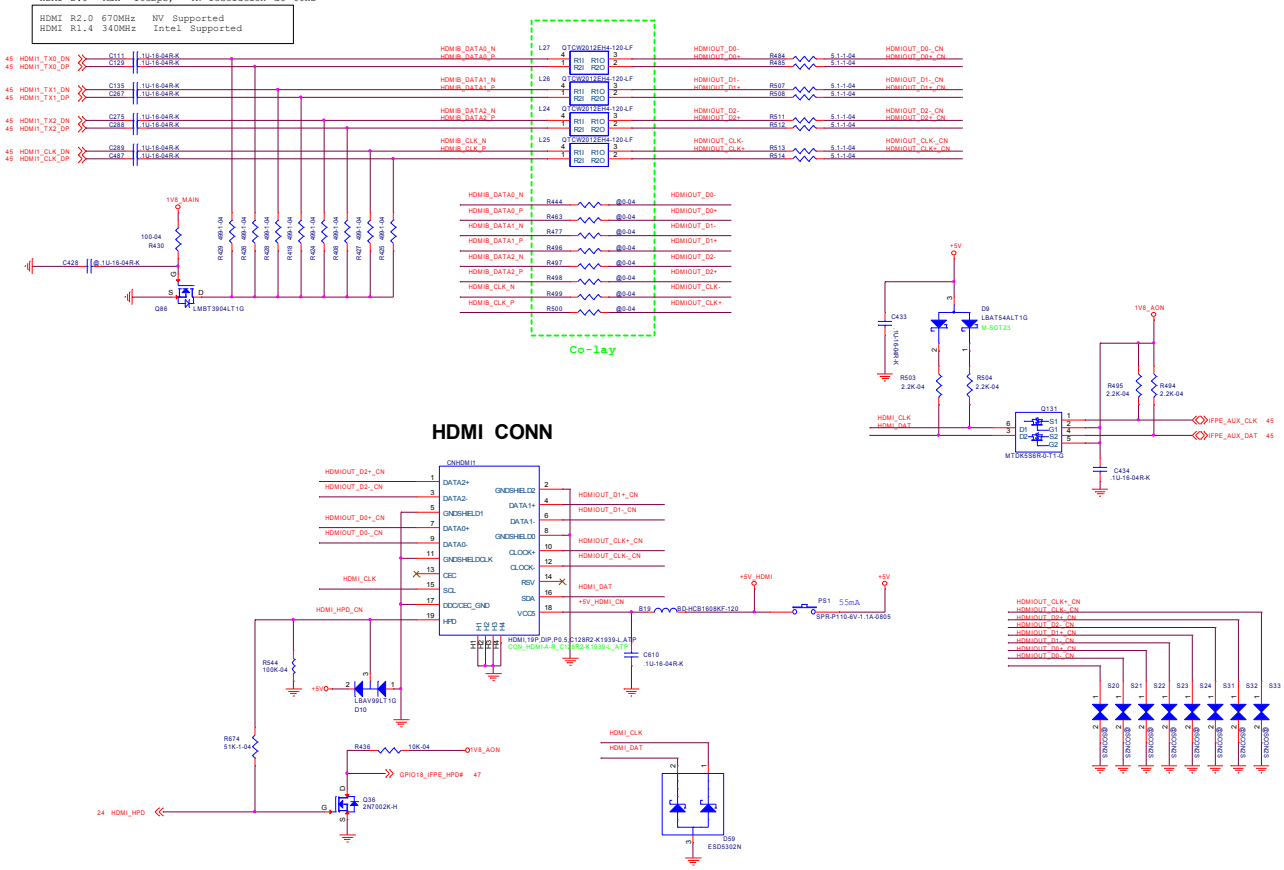


同方国际信息技术有限公司

Title	eDP Pannel/CAMERA	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Wednesday November 07, 2018	Sheet 21 of 61	

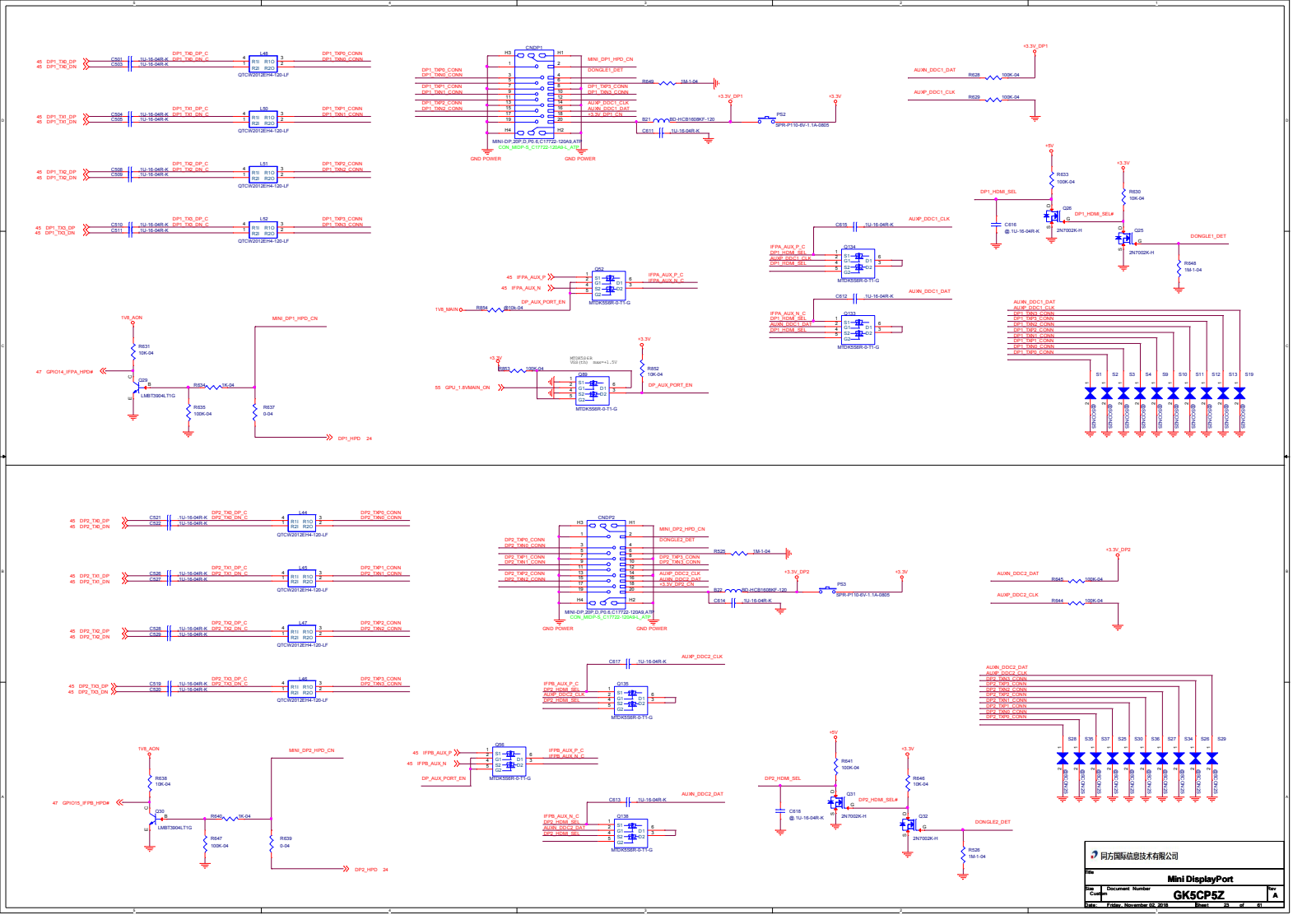
HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported



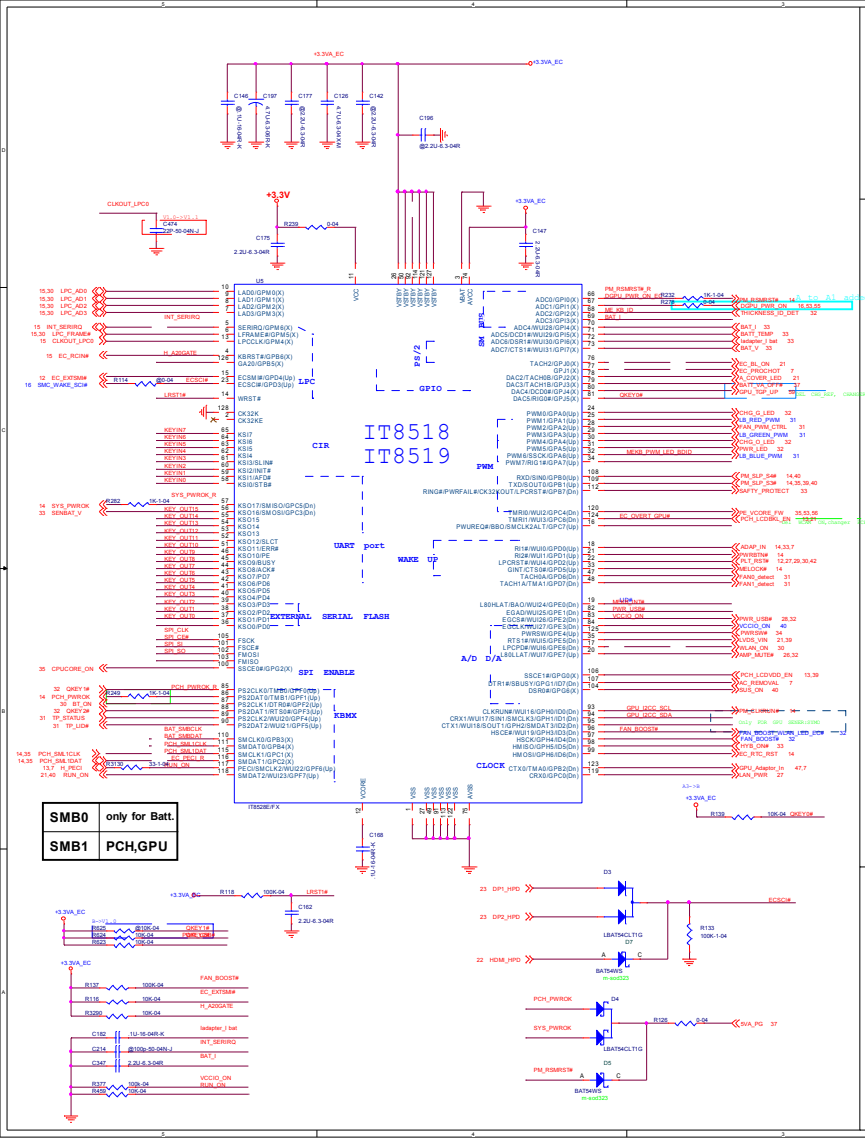
HDMI CONN

同方国际信息技术有限公司			
Title	HDMI		
Size C	Document Number GK5CP5Z		Rev A
Date: Friday, November 02, 2018	Sheet 22 of 61		

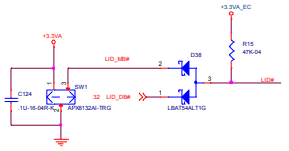


同方国际信息技术有限公司

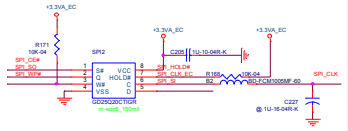
Title	Mini DisplayPort		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Friday, November 02, 2018	Sheet 23 of 61		



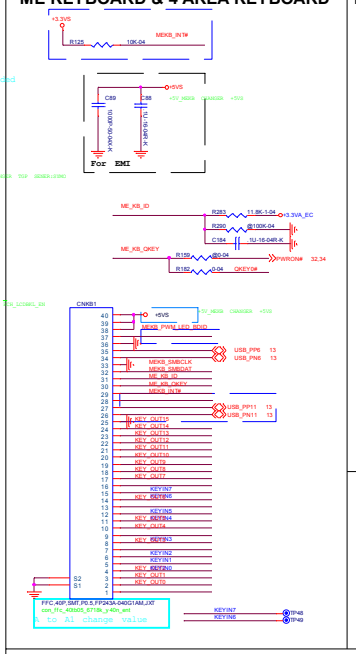
LID SW



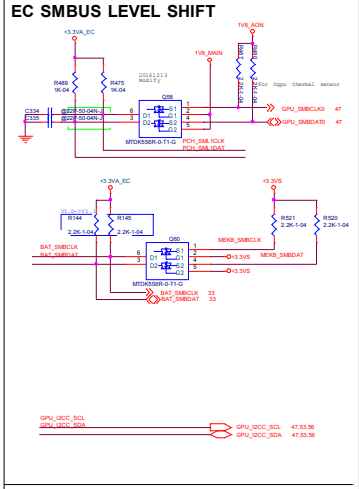
EC FLASH ROM(SPI)



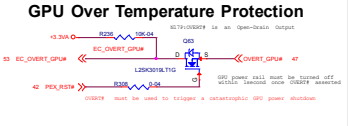
ME KEYBOARD & 4 AREA KEYBOARD



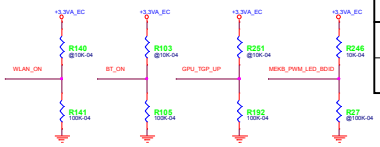
EC SMBUS LEVEL SHIFT



GPU Over Temperature Protection



Platform ID



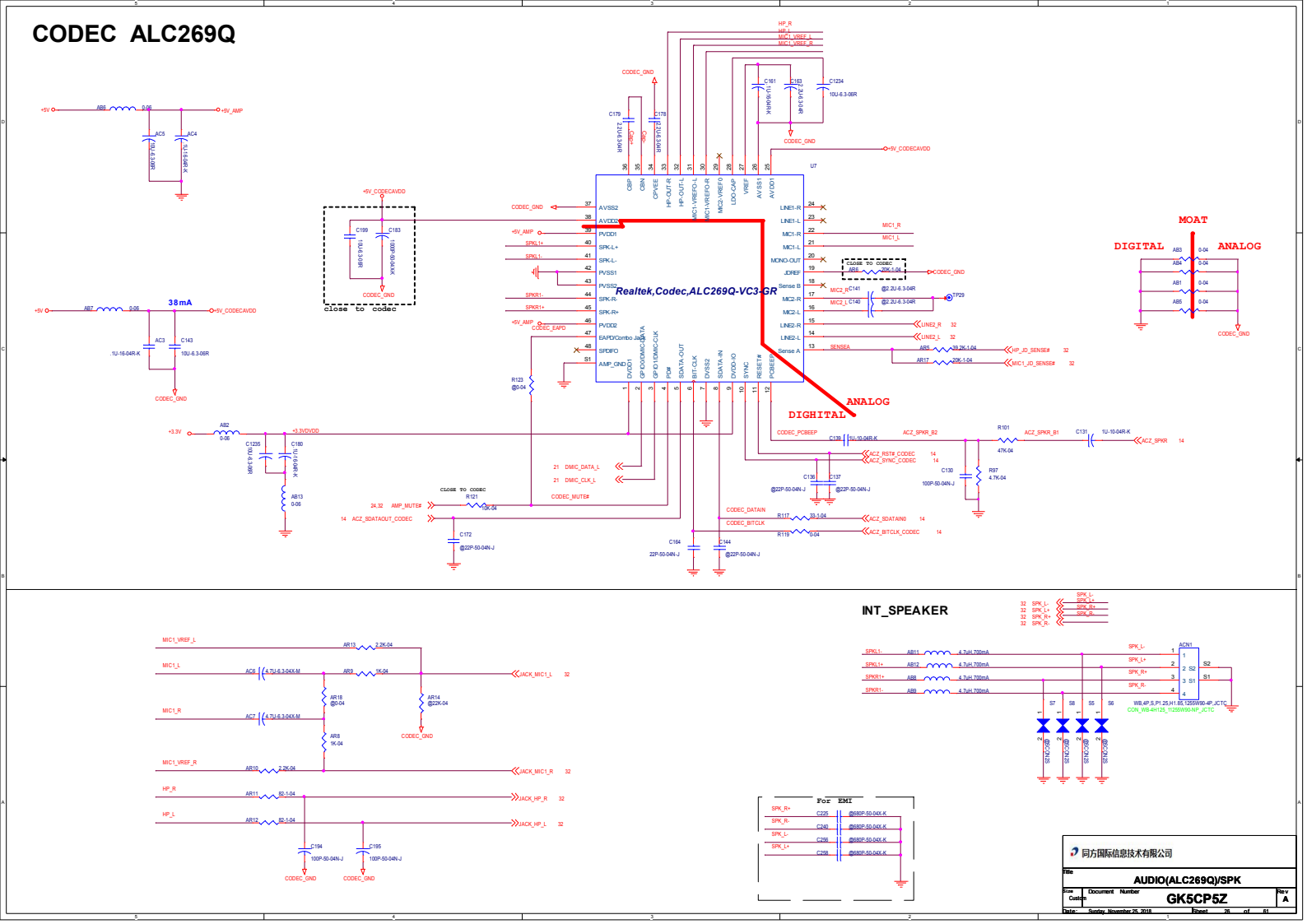
NET / Level	WLAN_ON	BT_ON	GPU_TGP_UP	Board ID
HIGH			GK5CN6Z	
LOW	15"	CFL-H	GK5CN5Z	

同方国际信息技术有限公司

Title	EC(IT8528E)/BIOS/KB CONN		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Wednesday, November 14, 2018	Sheet 24 of 51		

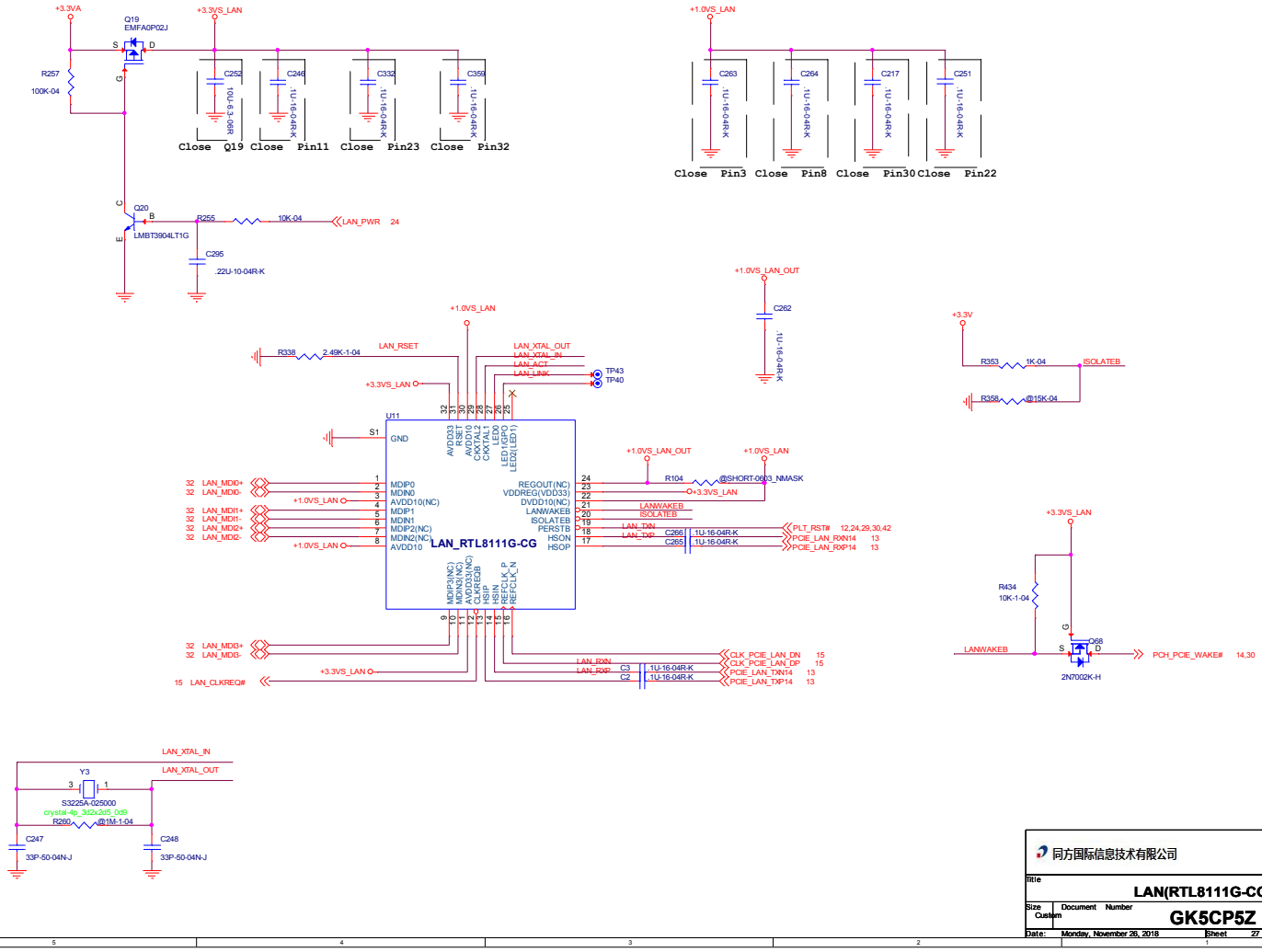
Title	GK5CNXX-10L
Size: C	Document Number: GK5CP5Z
Rev: A	
Date: Friday, November 02, 2018	Sheet 25 of 61

CODEC ALC269Q



同方国际信息技术有限公司

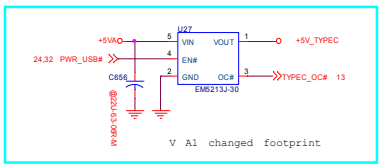
Title	AUDIO(ALC269Q)/SPK		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Sunday, November 25, 2018	Sheet 26 of 61		

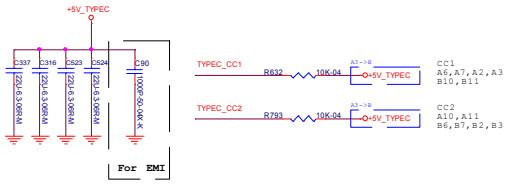


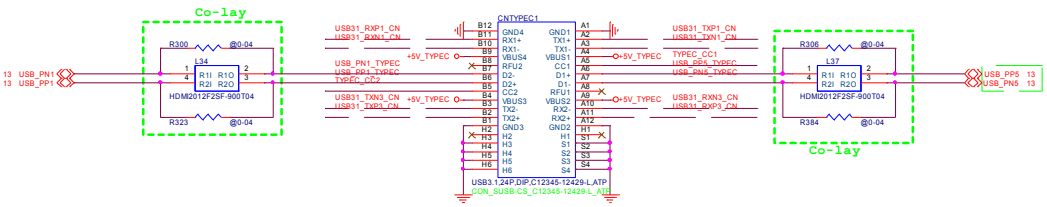
同方国际信息技术有限公司

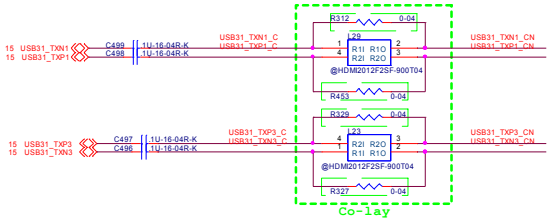
Title	LAN(RTL8111G-CG)	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Monday, November 26, 2018	Sheet 27 of 61	

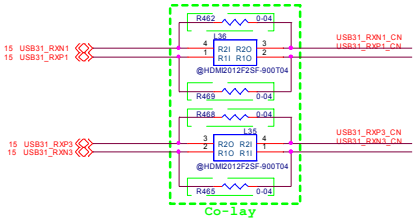
USB3.0 TYPE-C

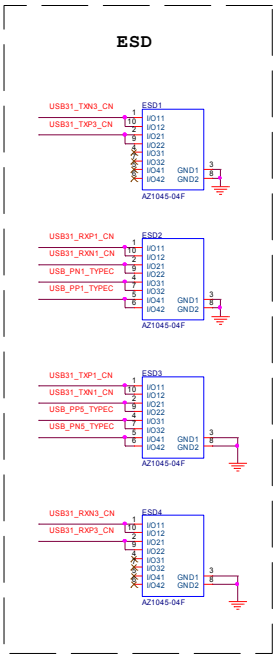








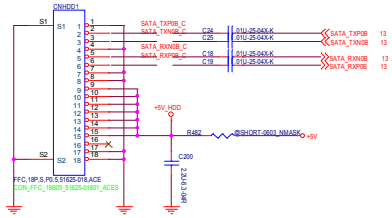




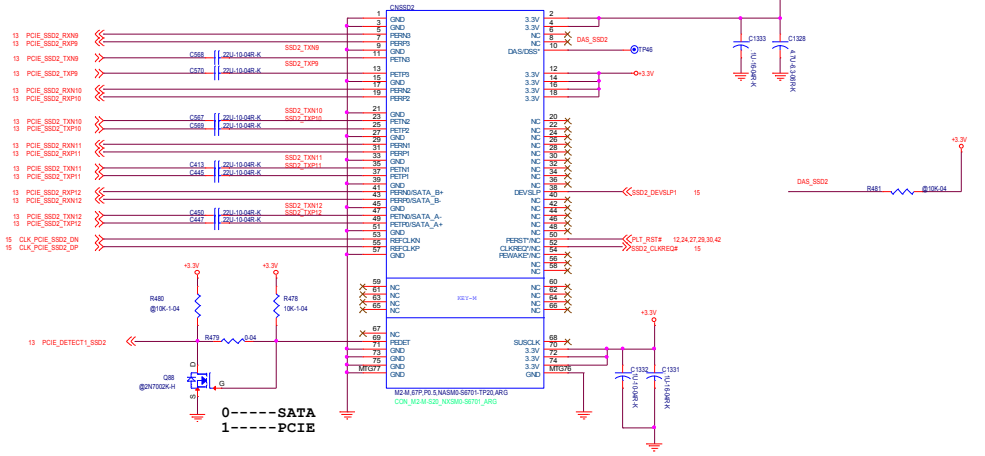
同方国际信息技术有限公司

Title	USB3.1 TYPE-C		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Friday, November 02, 2018	Sheet 28 of 61		

SATA-HDD

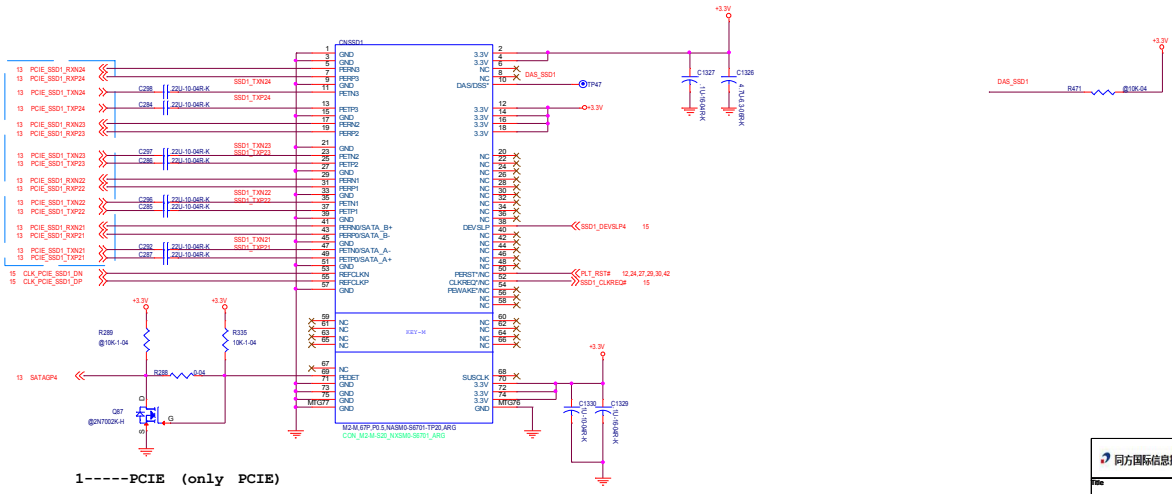


SSD2



0-----SATA
1-----PCIE

SSD1

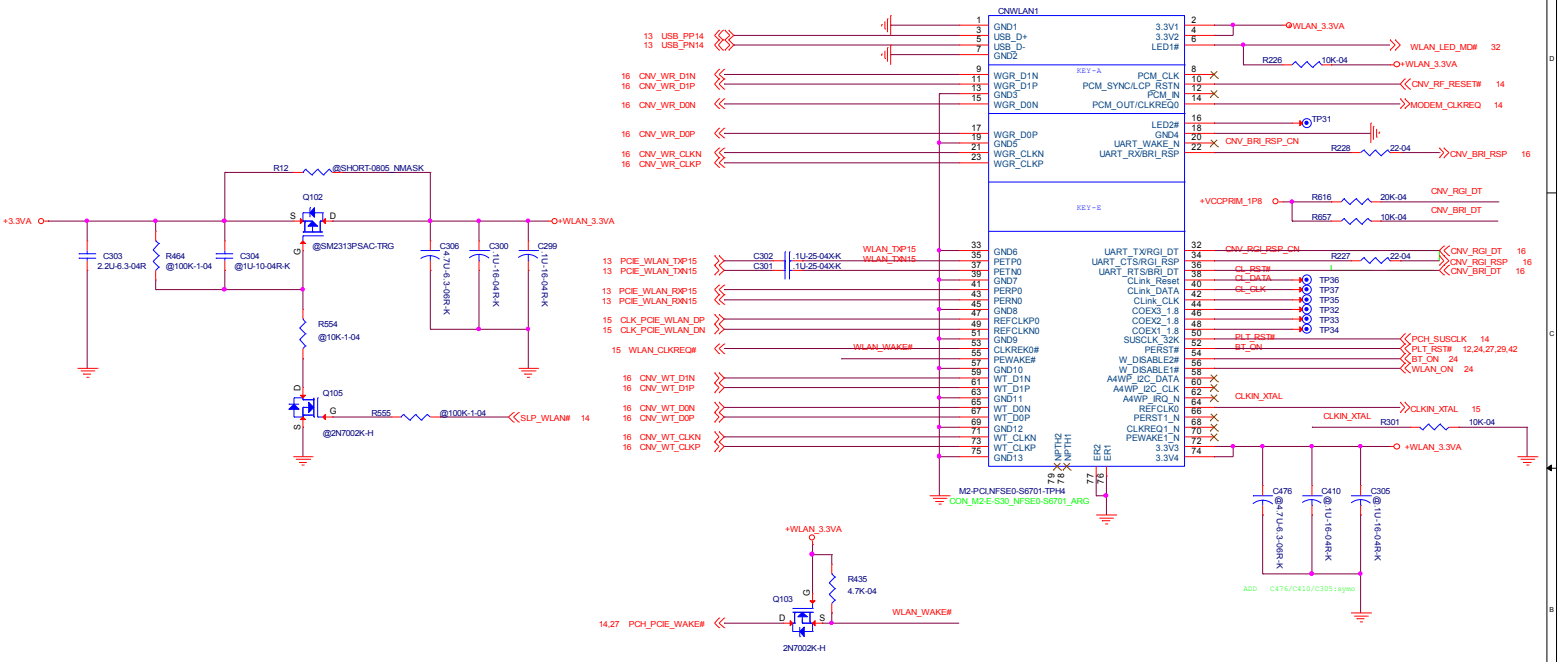


1-----PCIE (only PCIE)

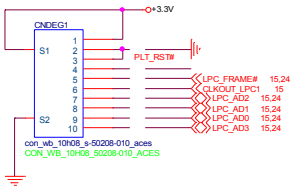
同方国际信息技术有限公司

Title	HDD/SSD		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Sunday, November 25, 2018	Sheet 29 of 61		

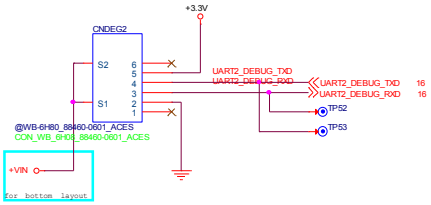
WLAN CONN



LPC debug port



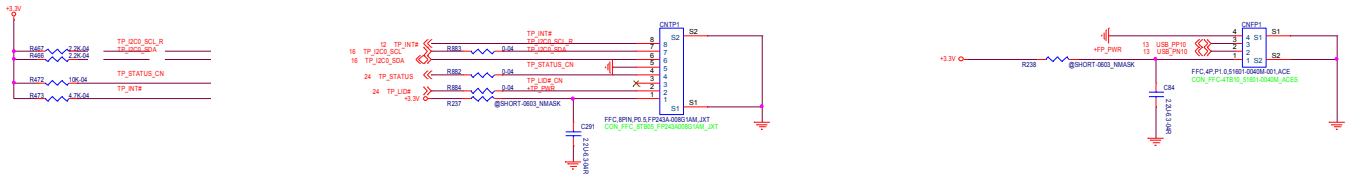
UART debug port



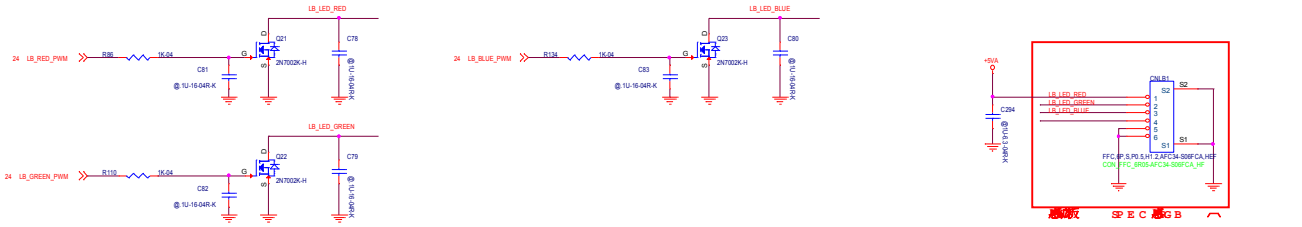
同方国际信息技术有限公司

Title	WLAN/UART DEBUG/LPC DEBUG	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Sunday, November 25, 2018	Sheet 30 of 61	

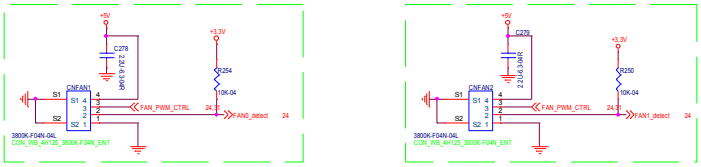
Touch Pad&Finger Print



Light bar Control



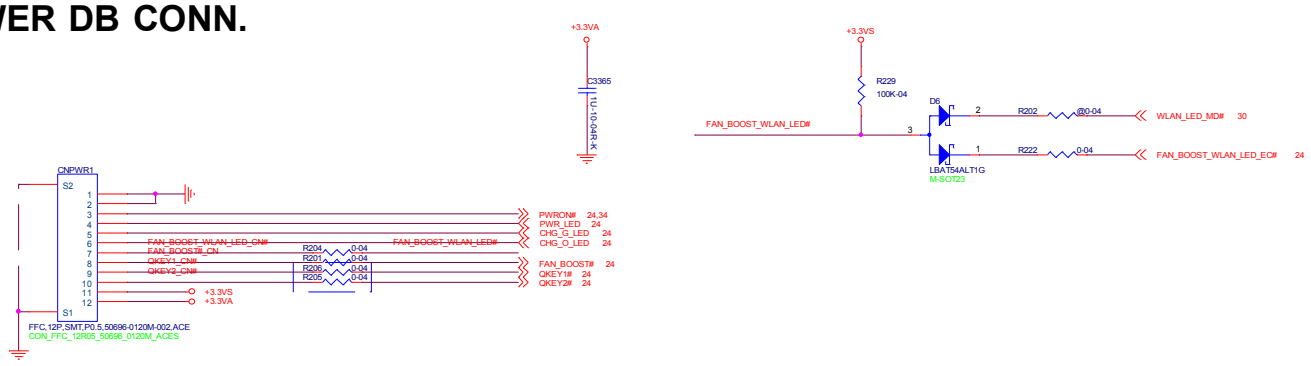
FAN CONTROLLER



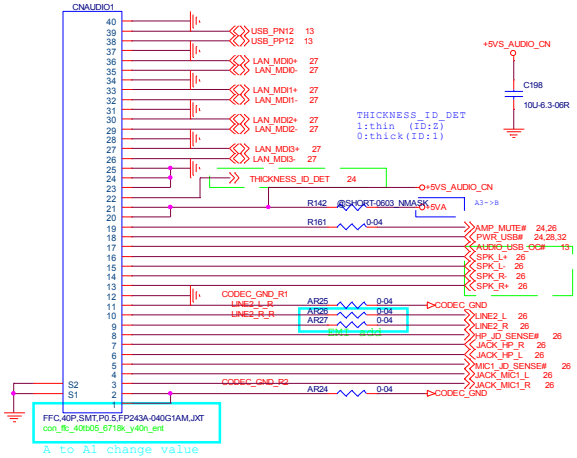
同方国际信息技术有限公司

Title	TP/CP/FAN/LB	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Sunday, November 25, 2018	Sheet 31 of 61	

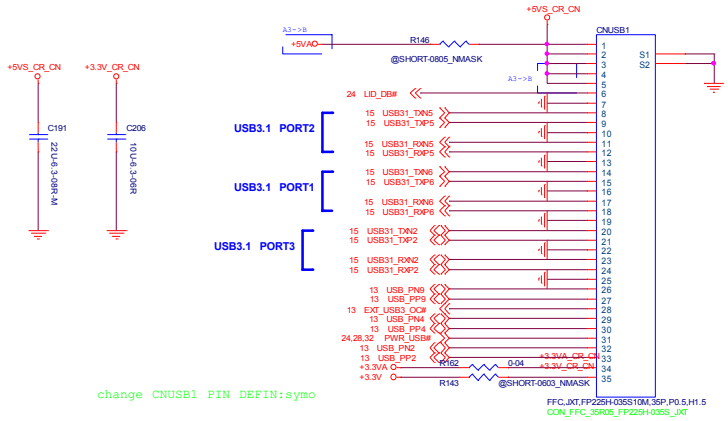
POWER DB CONN.



Audio&LAN DB CONN.

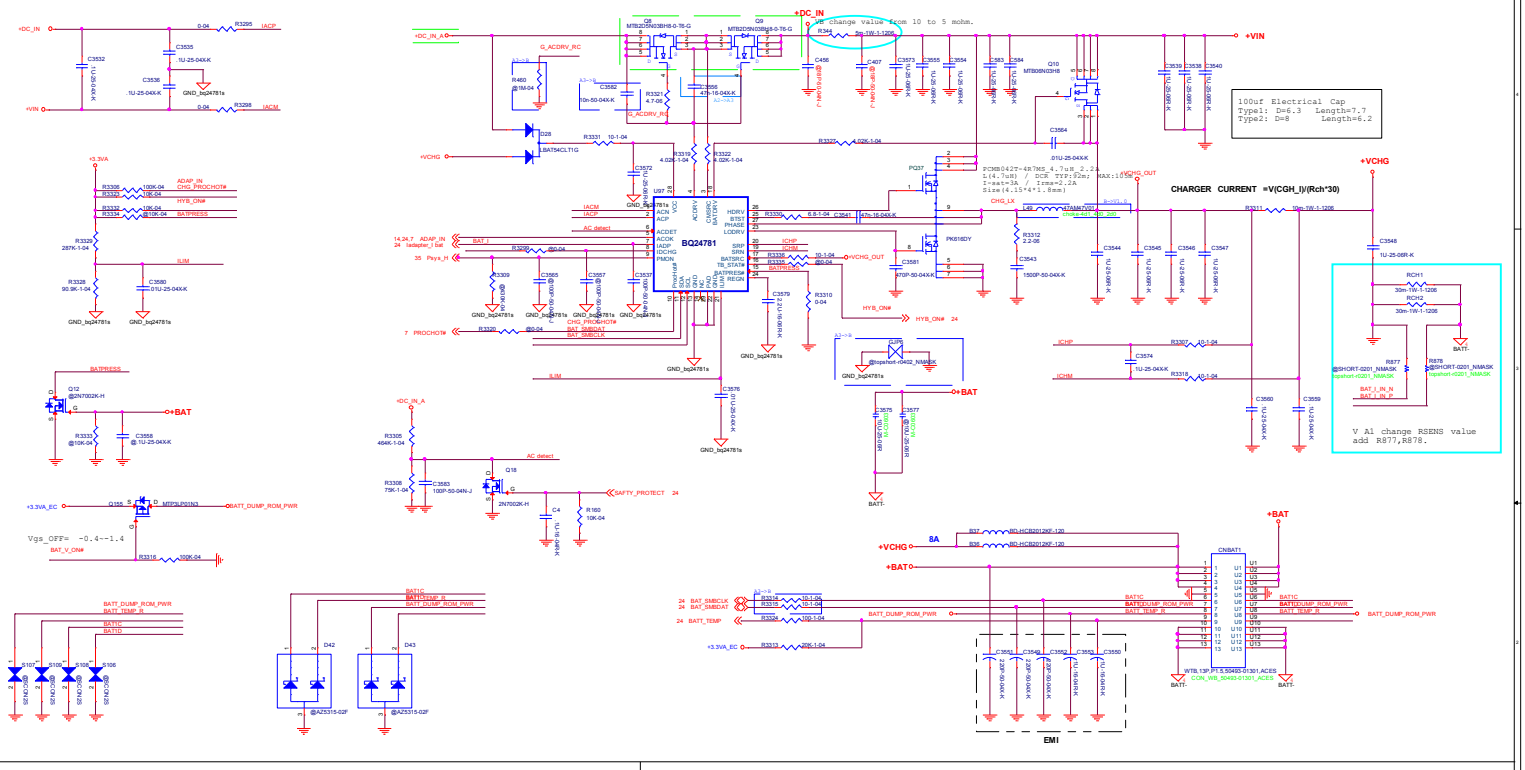


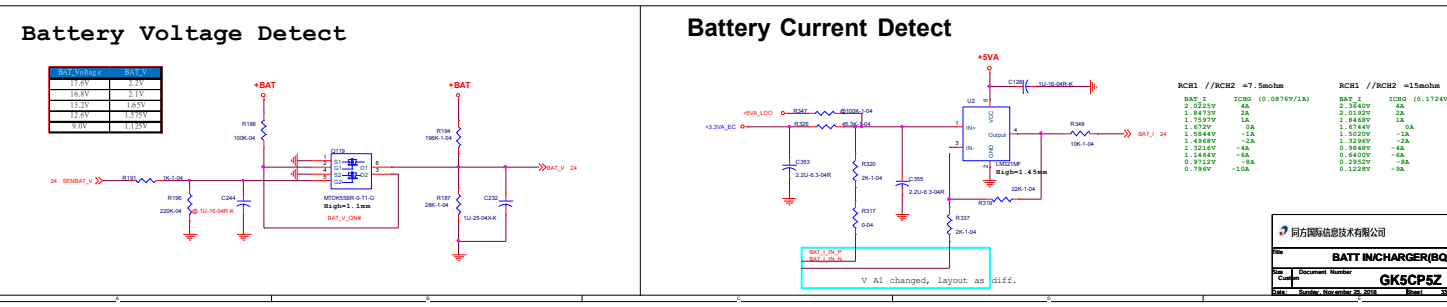
USB3.0 DB CONN.



同方国际信息技术有限公司

Title	PWR_DB/USB3.0 DB/Audio DB	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Monday, November 26, 2018	Sheet 32 of 61	





Battery Voltage Detect

BAT_Voltage	BAT_V
17.6V	2.2V
16.8V	2.1V
13.2V	1.65V
12.4V	1.575V
9.0V	1.125V

Battery Current Detect

RCH1 //RCH2 =7.5mohm

BAT_I	ICHG (0.0876V/1A)
2.0225V	4A
1.8473V	2A
1.7597V	1A
1.672V	0A
1.5844V	-1A
1.4968V	-2A
1.3216V	-4A
1.1464V	-6A
0.9712V	-8A
0.796V	-10A

RCH1 //RCH2 =15mohm

BAT_I	ICHG (0.1724V/1A)
2.3640V	4A
2.0192V	2A
1.8468V	1A
1.6744V	0A
1.5020V	-1A
1.3296V	-2A
0.9848V	-4A
0.6400V	-6A
0.2952V	-8A
0.1228V	-9A

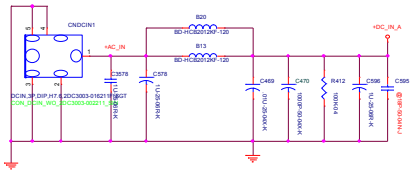
同方国际信息技术有限公司

Title: BATT IN/CHARGER(BQ24781)

Size: Custom | Document Number: GK5CP5Z | Rev: A

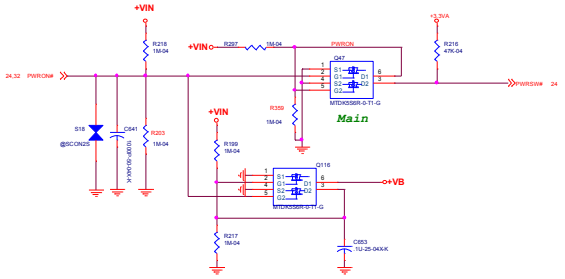
Date: Sunday, November 25, 2018 | Sheet 33 of 61

+DC_IN

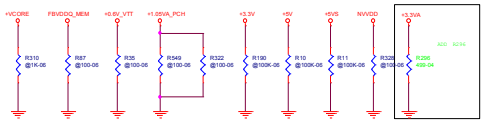


EMB20NP3V
ID=-13A TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms

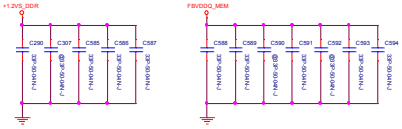
POWER SW



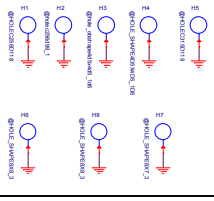
Discharge Resistor



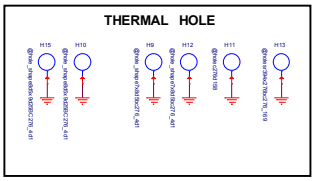
For RF



PCB HOLE

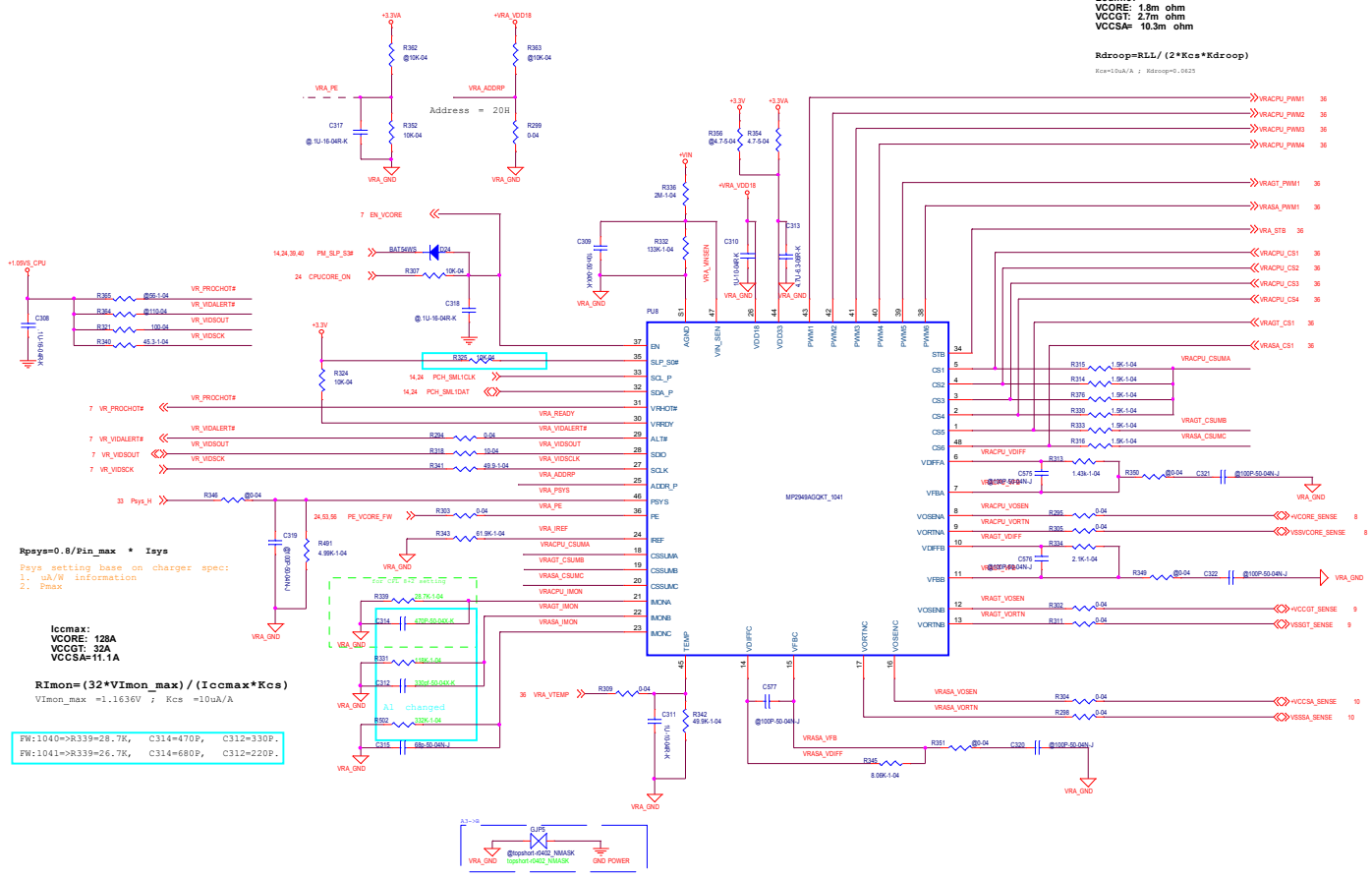


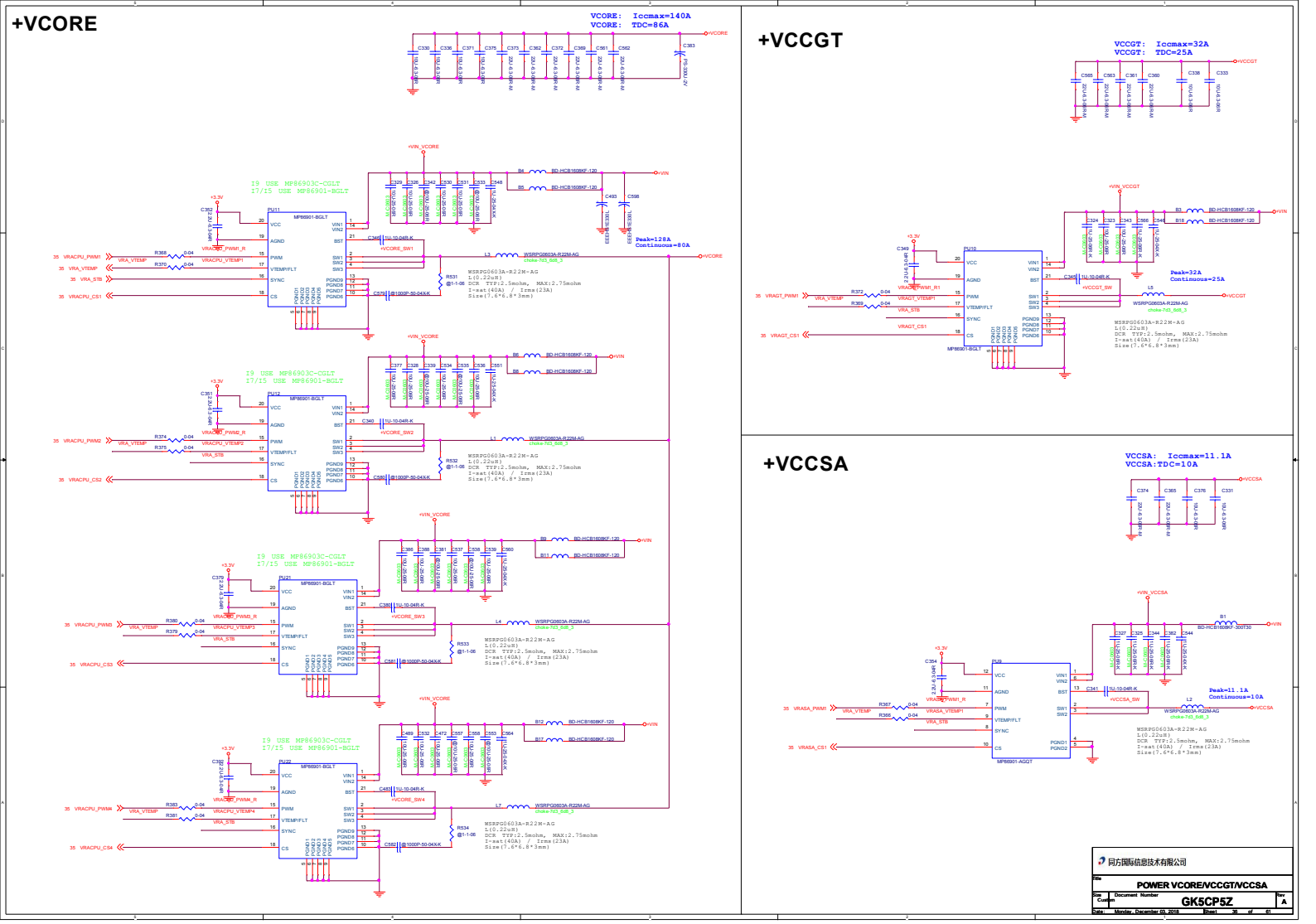
THERMAL HOLE



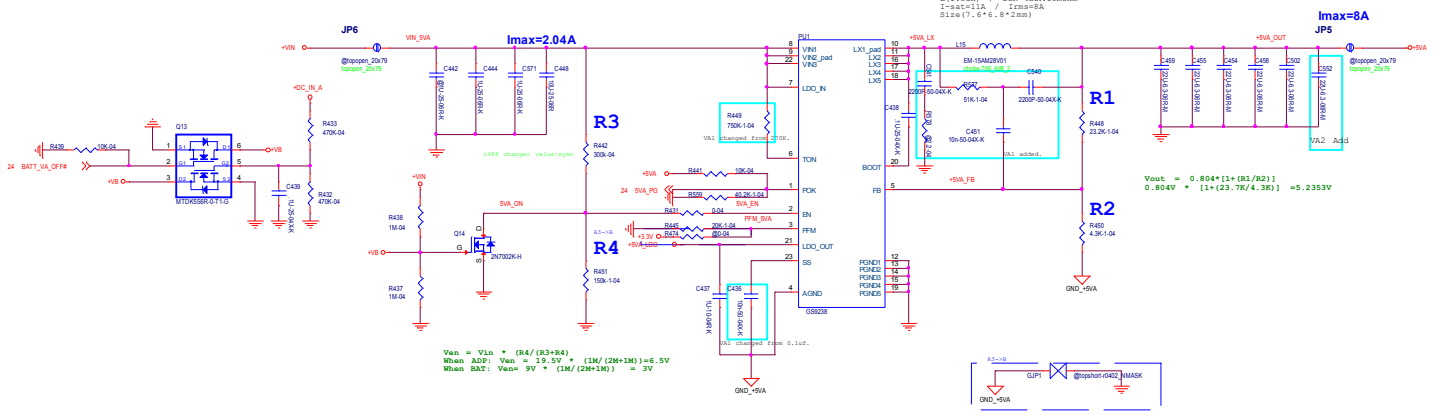
同方国际信息技术有限公司

Title	DC IN/PWR_SW/H-S CAP/SCREW		
Size	Document Number		Rev
Custom	GK5CP5Z		A
Date: Friday, November 02, 2018	Sheet 34 of 61		

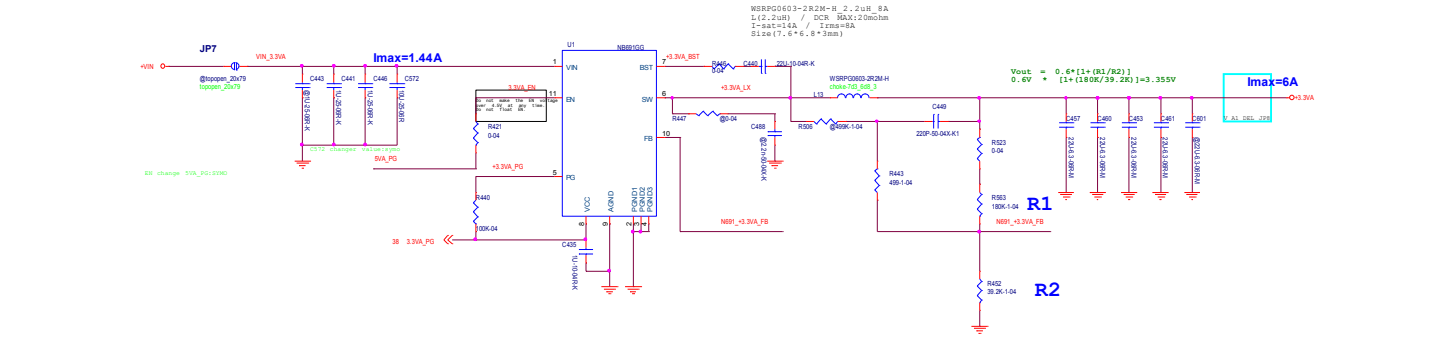

Loaline:
VCORE: 1.8m ohm
VCCGT: 2.7m ohm
VCCSA= 10.3m ohm
Rdroop=RLL/(2*Kcs*Kdroop)
Kcs=10uA/A ; Rdroop=0.0625
Address = 20H
MP2949AGQKT_1041
Rpsys=0.8/Pin_max * Isys
Psys setting base on charger spec:
1. uA/W information
2. Pmax
Iccmax:
VCORE: 128A
VCCGT: 32A
VCCSA=11.1A
RImon=(32*VImon_max)/(Iccmax*Kcs)
VImon_max =1.1636V ; Kcs =10uA/A
FW:1040=>R339=28.7K, C314=470P, C312=330P.
FW:1041=>R339=26.7K, C314=680P, C312=220P.
A1 changed
同方国际信息技术有限公司
POWER VR CONTROLLER
GK5CP5Z


+VCORE
VCORE: Iccmax=140A
VCORE: TDC=86A
I9 USE MP86903C-CGLT
I7/I5 USE MP86901-BGLT
MP86901-BGLT
Peak=128A
Continuous=80A
+VCCGT
VCCGT: Iccmax=32A
VCCGT: TDC=25A
Peak=32A
Continuous=25A
+VCCSA
VCCSA: Iccmax=11.1A
VCCSA:TDC=10A
Peak=11.1A
Continuous=10A
MP86901-AGQT
同方国际信息技术有限公司
POWER VCORE/VCCGT/VCCSA
GK5CP5Z
Monday, December 03, 2018
35 of 61

+5VA



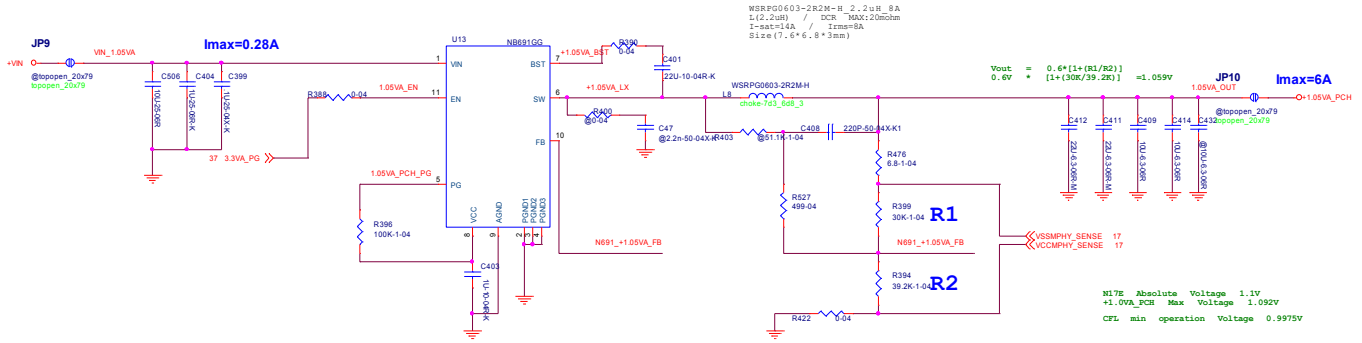
+3.3VA



同方国际信息技术有限公司

Title	POWER +5VA/+3.3VA		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Sunday, November 25, 2018	Sheet 37 of 61		

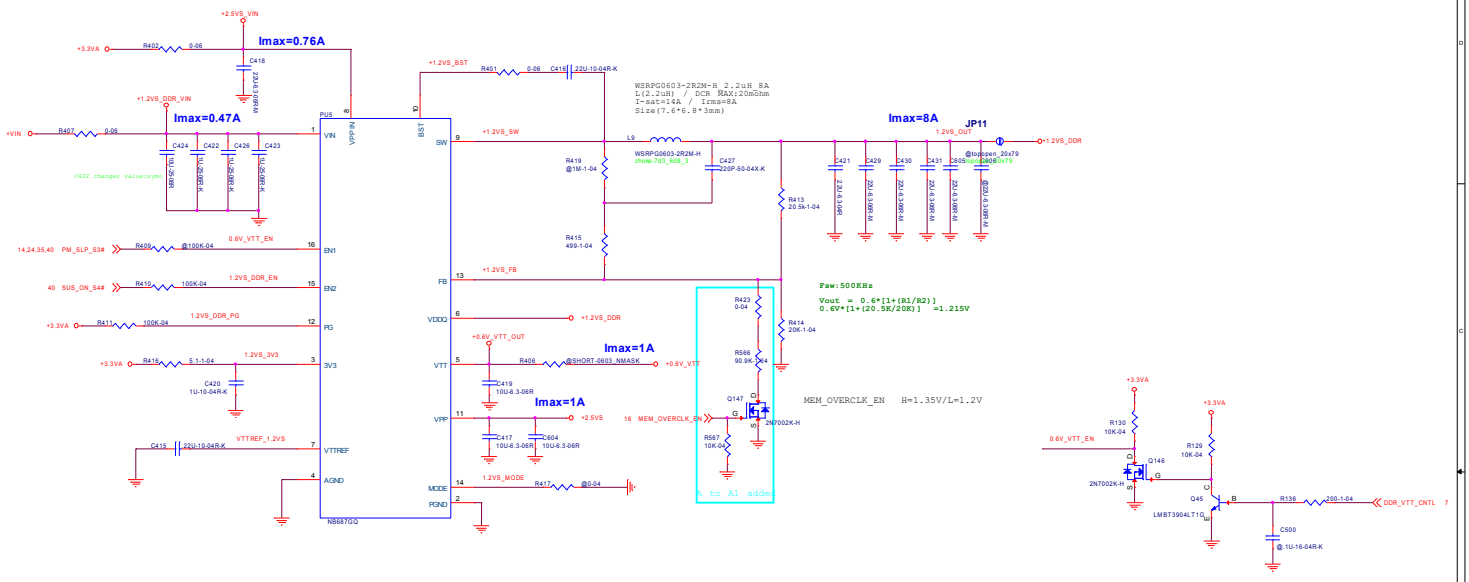
+1.05VA_PCH



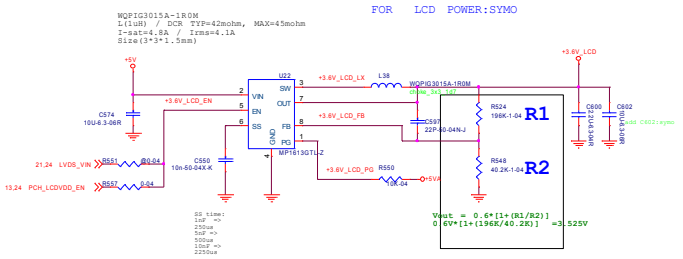
同方国际信息技术有限公司

Title	POWER +1.8VA/+1.05VA_PCH	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 38 of 61	

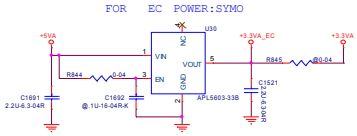
+1.2VS_DDR/+2.5VS/+0.6V_VTT



+3.6V_LCD



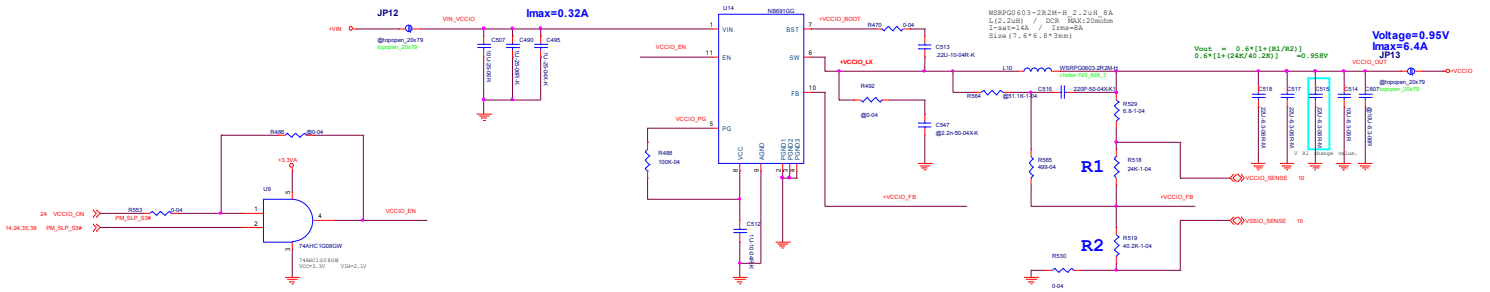
+3.3VA_EC



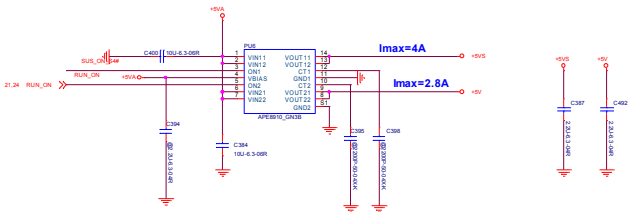
同方国际信息技术有限公司

Title	POWER +1.2VS_DDR/2.5VS/VTT		
Size C	Document Number GK5CP5Z		Rev A
Date: Sunday, November 25, 2018	Sheet 39 of 61		

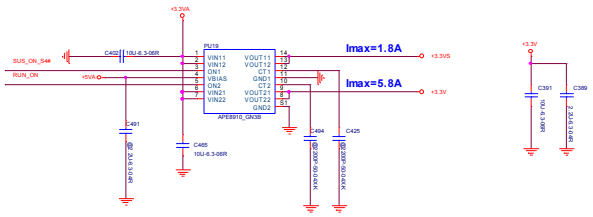
+VCCIO



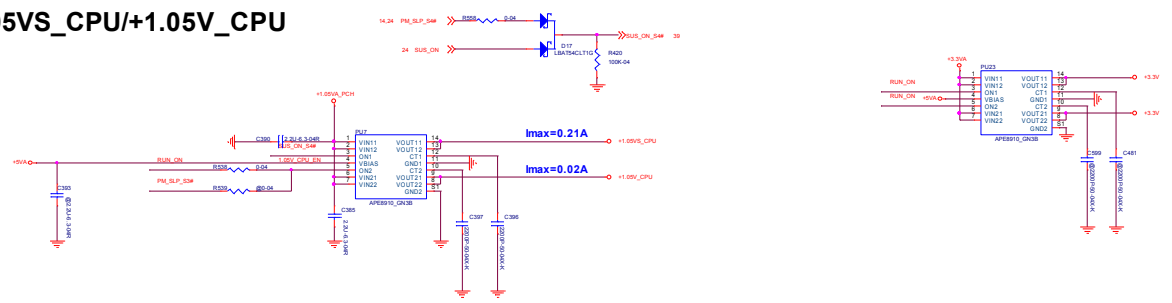
+5VS/+5V



+3.3VS/+3.3V



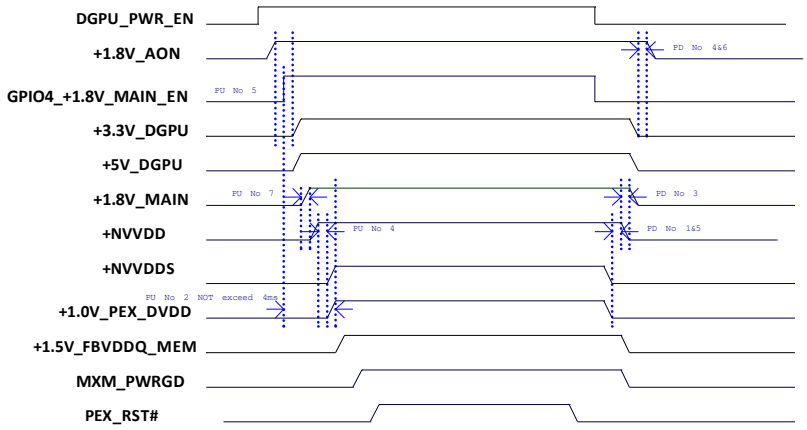
+1.05VS_CPU/+1.05V_CPU



同方国际信息技术有限公司

Title	POWER +VCCIO/+VS PWR/+V PWR		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Friday, November 02, 2018	Sheet 40 of 61		

DGPU POWER SEQUENCE

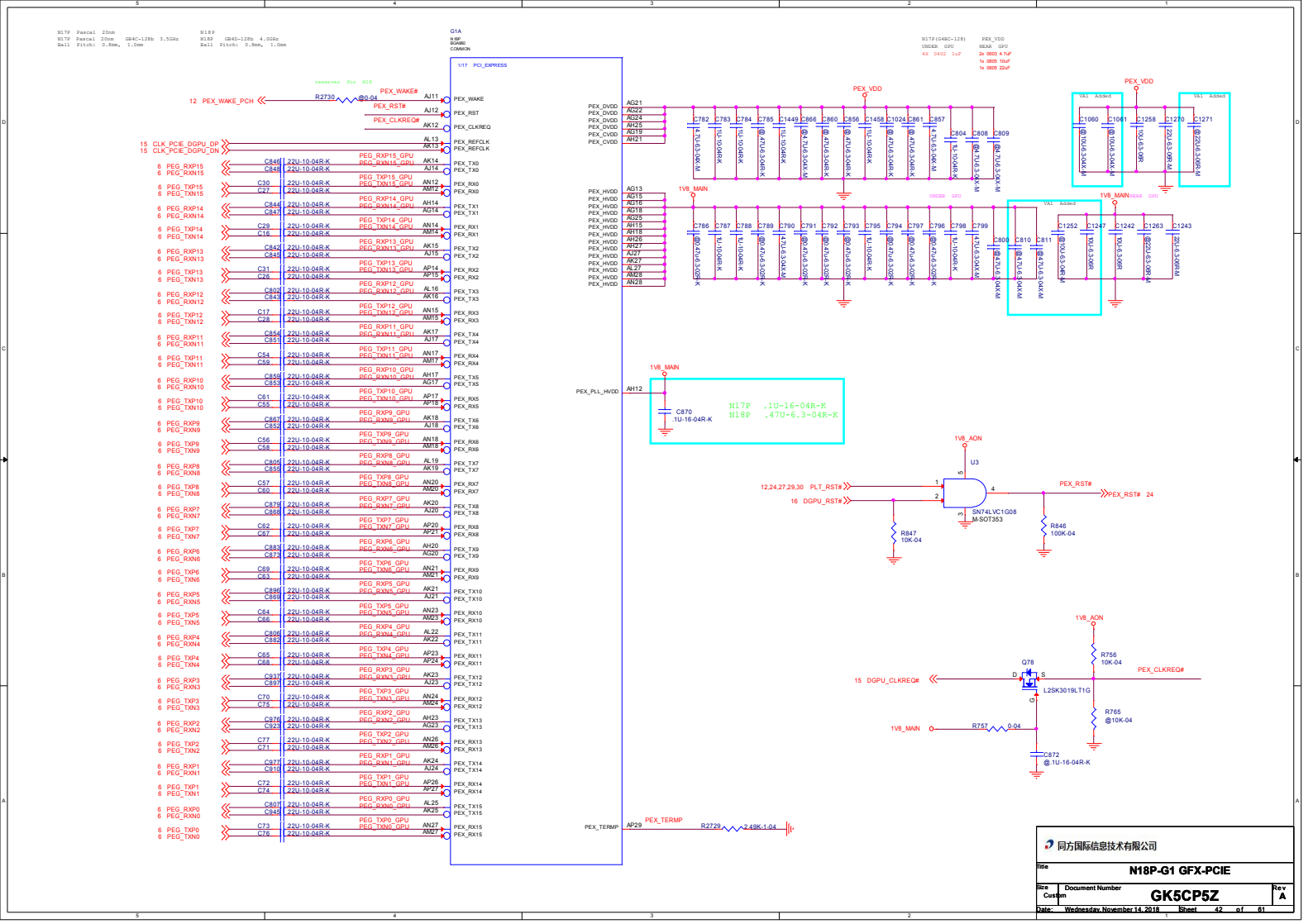


POWER UP sequence is required:+1.8V_AON->+1.8V_MAIN->+NVVDD->+NVVDDS/+1.0V_PEX_DVDD->+1.5V_FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.t1 From +1.8V_MAIN_EN to +1.0V_PEX_DVDD/+NVVDD_PGOOD) must NOT exceed 4ms.
3.The ramp-up overshoot should not exceed the silicon reliability limit voltage
4.Power up +NVVDD must be 90% before +1.0V+PEX_DVDD and NVVDDS can start ramp up.
5.Power up +1.8V_AON must be 90% before 3.3V ramp up.
6.All 3.3V devices that connect to the GPU must be powered after +1.8V_AON ; GPU can't have any 3.3V leakage path before +1.8V_AON present.
7.The propagation delay between +1.8V_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.

POWER DOWN sequence is required
1.+NVVDDS/+1.0V_PEX_DVDD must ramp down before NVVDD.
2.All other power rails can ramp down together with NVVDD.
3.+1.8V_MAIN must power down after NVVDD power down
3.The progapation delay between +1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
5.Power down NVVDDS and +1.0V_PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down 3.3V must be less than 10% before +1.8V_AON can start ramp down.

同方国际信息技术有限公司

Title	N18P-G1 POWER SEQUENCE	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Friday, November 02, 2018	Sheet 41 of 61	


N17P Pascal 20nm GB4C-128b 3.5GHz Ball Pitch: 0.8mm, 1.0mm
N18P GB4D-128b 4.0GHz Ball Pitch: 0.8mm, 1.0mm
G1A
N18P SIGNED COMMON
1/17 PCI_EXPRESS
reserver for N18
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK
PEX_TX0
PEX_TX0
PEX_RX0
PEX_RX0
PEX_TX1
PEX_TX1
PEX_RX1
PEX_RX1
PEX_TX2
PEX_TX2
PEX_RX2
PEX_RX2
PEX_TX3
PEX_TX3
PEX_RX3
PEX_RX3
PEX_TX4
PEX_TX4
PEX_RX4
PEX_RX4
PEX_TX5
PEX_TX5
PEX_RX5
PEX_RX5
PEX_TX6
PEX_TX6
PEX_RX6
PEX_RX6
PEX_TX7
PEX_TX7
PEX_RX7
PEX_RX7
PEX_TX8
PEX_TX8
PEX_RX8
PEX_RX8
PEX_TX9
PEX_TX9
PEX_RX9
PEX_RX9
PEX_TX10
PEX_TX10
PEX_RX10
PEX_RX10
PEX_TX11
PEX_TX11
PEX_RX11
PEX_RX11
PEX_TX12
PEX_TX12
PEX_RX12
PEX_RX12
PEX_TX13
PEX_TX13
PEX_RX13
PEX_RX13
PEX_TX14
PEX_TX14
PEX_RX14
PEX_RX14
PEX_TX15
PEX_TX15
PEX_RX15
PEX_RX15
PEX_VDD
1V8_MAIN
1V8_AON
PEX_PLL_HVDD
PEX_TERMP
PEX_TERMP
2.49K-1-04
U3
SN74LVC1G08 M-SOT353
PLT_RST#
DGPU_RST#
PEX_RST#
PEX_CLKREQ#
DGPU_CLKREQ#
Q78
L2SK3019LT1G
R847 10K-04
R846 100K-04
R756 10K-04
R765 @10K-04
R757 0-04
C872 @.1U-16-04R-K
C870 .1U-16-04R-K
N17P .1U-16-04R-K
N18P .47U-6.3-04R-K
同方国际信息技术有限公司
N18P-G1 GFX-PCIE
GK5CP5Z
Rev A
Wednesday November 14, 2018
Sheet 42 of 61

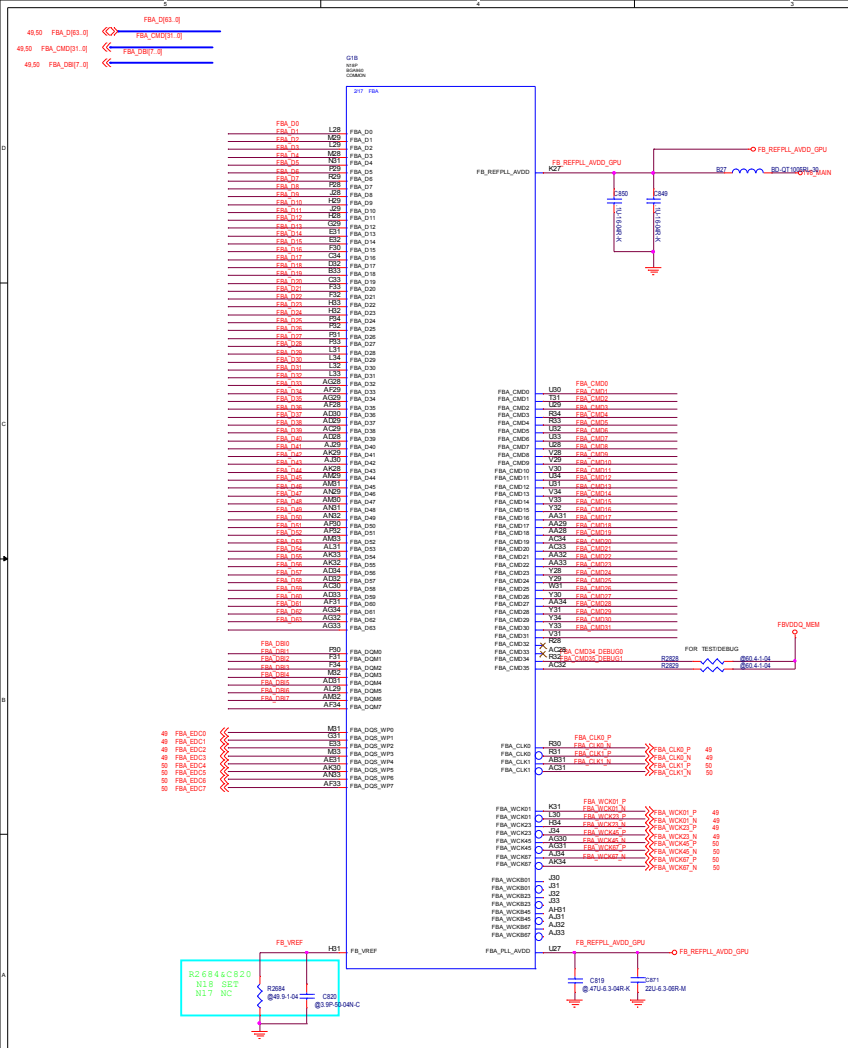
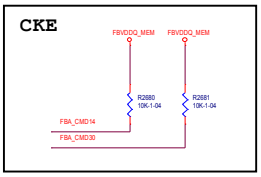
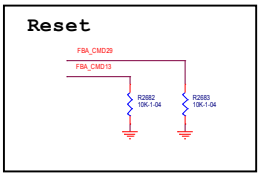


Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

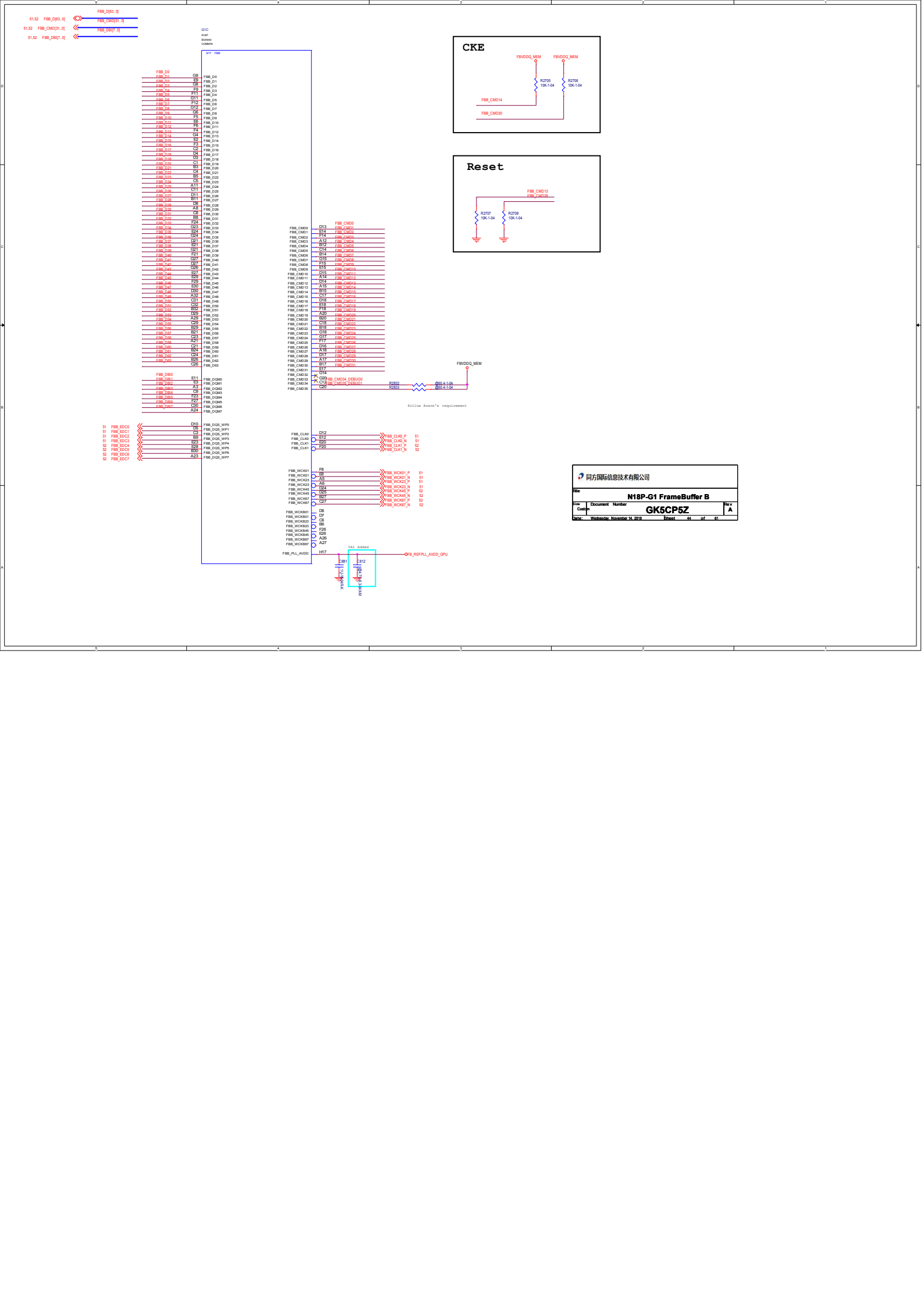
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*





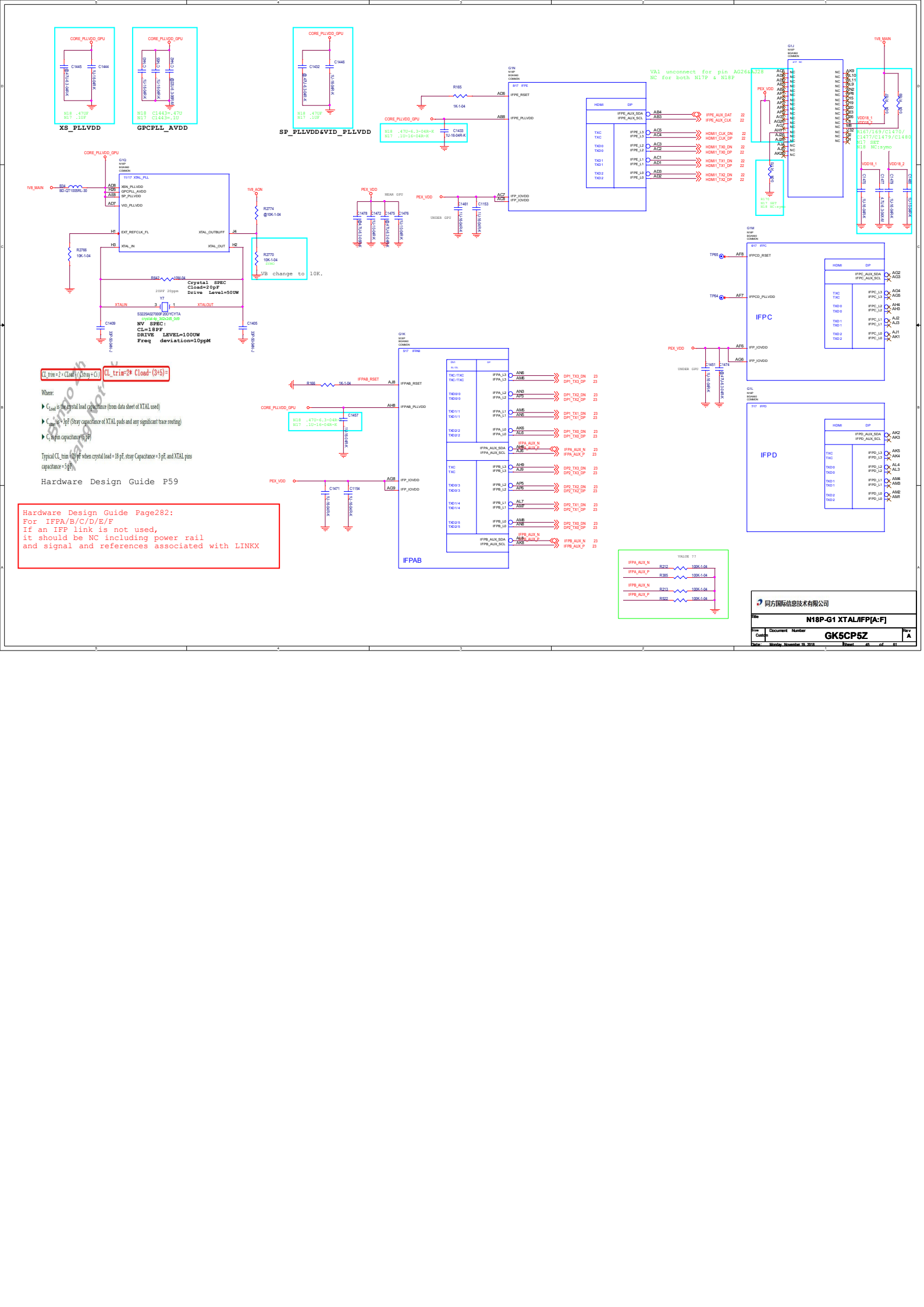
同方国际信息技术有限公司

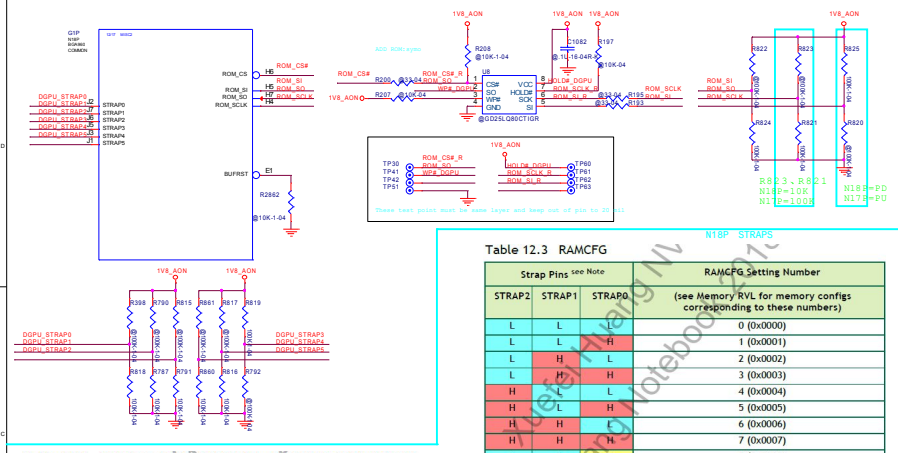
Title	N18P-G1 FrameBuffer A		
Size Custom	Document Number GK5CP5Z		Rev A
Date: Wednesday, November 14, 2018	Sheet 43 of 61		



同方国际信息技术有限公司

File	N18P-G1 FrameBuffer B		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Wednesday, November 14, 2018	Sheet 44 of 61		


XS_PLLVDD
GPCPLL_AVDD
SP_PLLVDD&VID_PLLVDD
VA1 unconnect for pin AG26&AN28
NC for both N17P & N18P
VB change to 10K.
Crystal SPEC
Cload=20pF
Drive Level=50UW
NV SPEC:
CL=18PF
DRIVE LEVEL=100UW
Freq deviation=10ppM
CL_trim=2×CLoad-(Cstray+Ci)
CL_trim=2* Cload-(3+5)=
Where:
CLoad is the crystal load capacitance (from data sheet of XTAL used)
Cstray = 5pF (Stray capacitance of XTAL pads and any significant trace routing)
Ci is pin capacitance =3 pF
Typical CL_trim =20 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF.
Hardware Design Guide P59
Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used,
it should be NC including power rail
and signal and references associated with LINKX
IFPC
IFPD
IFPAB
同方国际信息技术有限公司
N18P-G1 XTAL/IFP[A:F]
GK5CP5Z
Rev A
Monday, November 19, 2018
Sheet 45 of 61



GDDR5 CFG Setting						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
4GB	Samsung	K4G80325FB-HC28 B-die	0X0	L	L	L
4GB	Micron	MT51J256M32HF-70:A A-die	0X1	L	L	H
4GB	Hynix	H5GC8H24MJR-ROC M-die	0X2	L	H	L
2GB	Samsung	K4G41325FE-HC28 E-die	0X7	H	H	H
2GB	Micron	H5GC4H24AJR-ROC A-die	0X6	H	H	L
2GB	Hynix	EDW4032BABG-70-F A-die	0X8	L	L	M

N18P STRAPS

Table 12.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Note: The ternary strap pins listed in the STRAP columns must be pulled to one of three voltage levels. "L" means Low level (GND). "M" means Middle level (0.9V). "H" means High level (1.8V).

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin	voltage<1.5V	
	0.3V<pin	voltage<0.5V	

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V²	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V²	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

N17P STRAPS

SOR_EXPOSED Audio Configuration Straps

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0
No other configurations are supported.			

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

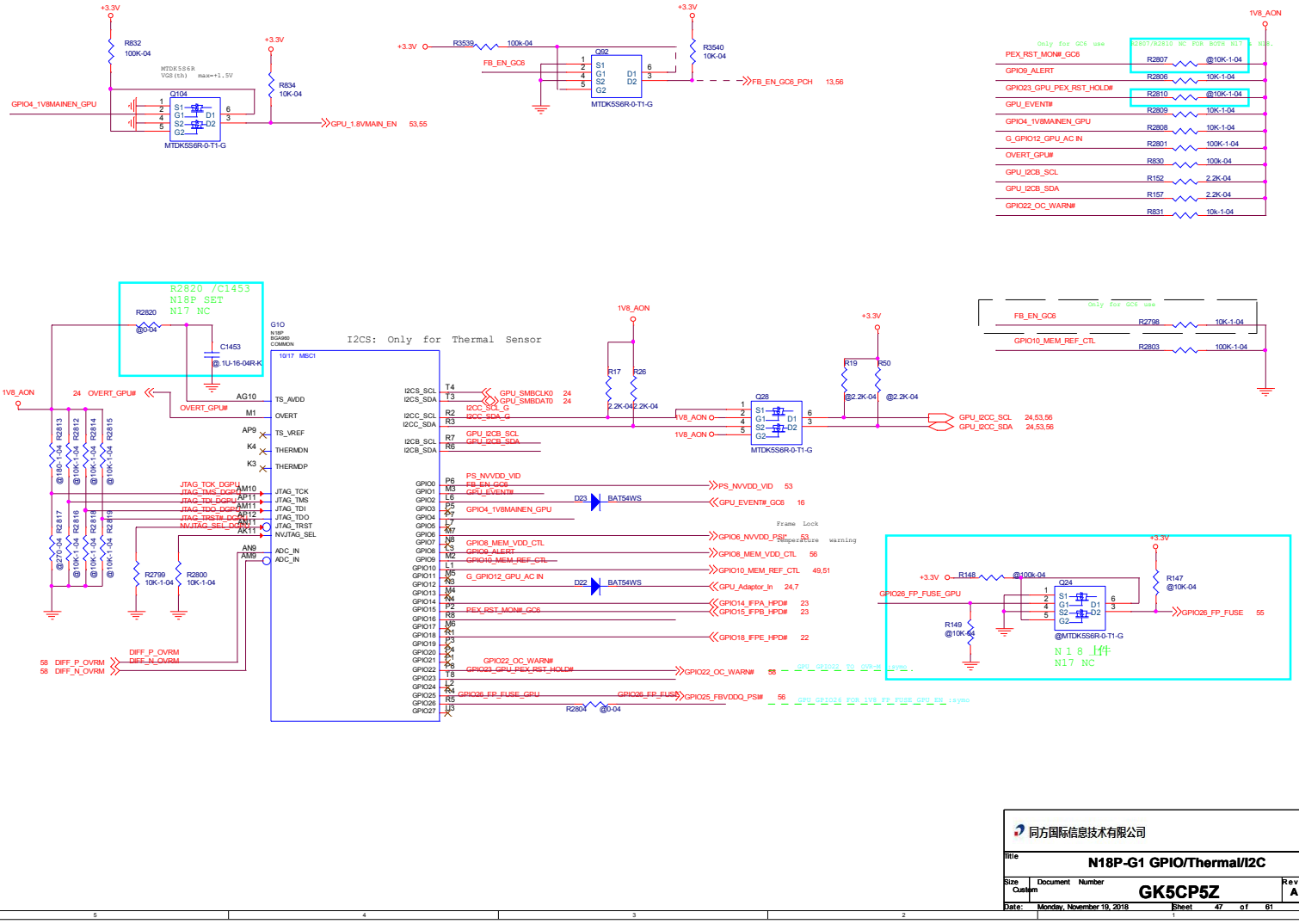
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
All other Strap Configurations				(Reserved)			

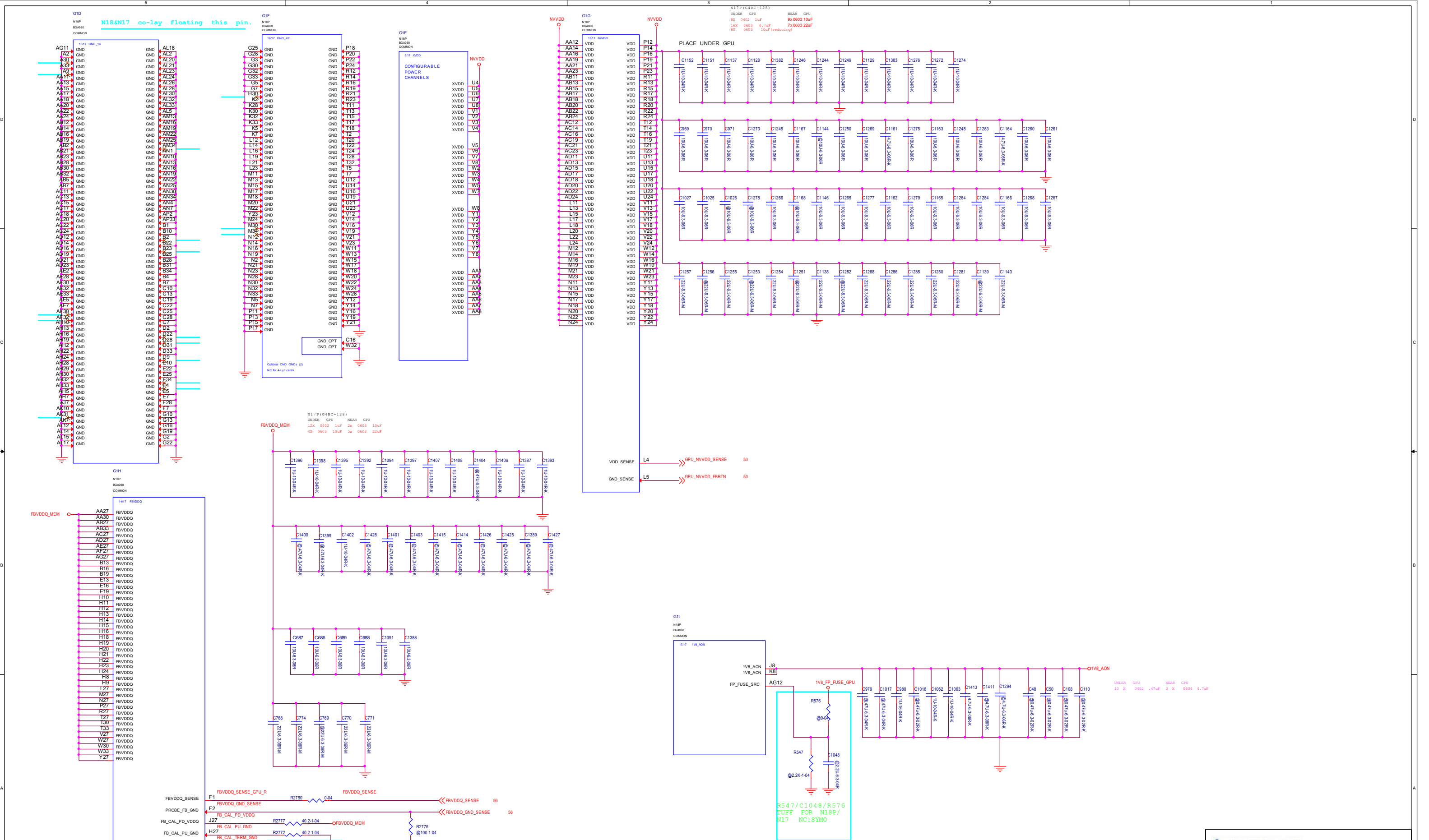
Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

同方国际信息技术有限公司

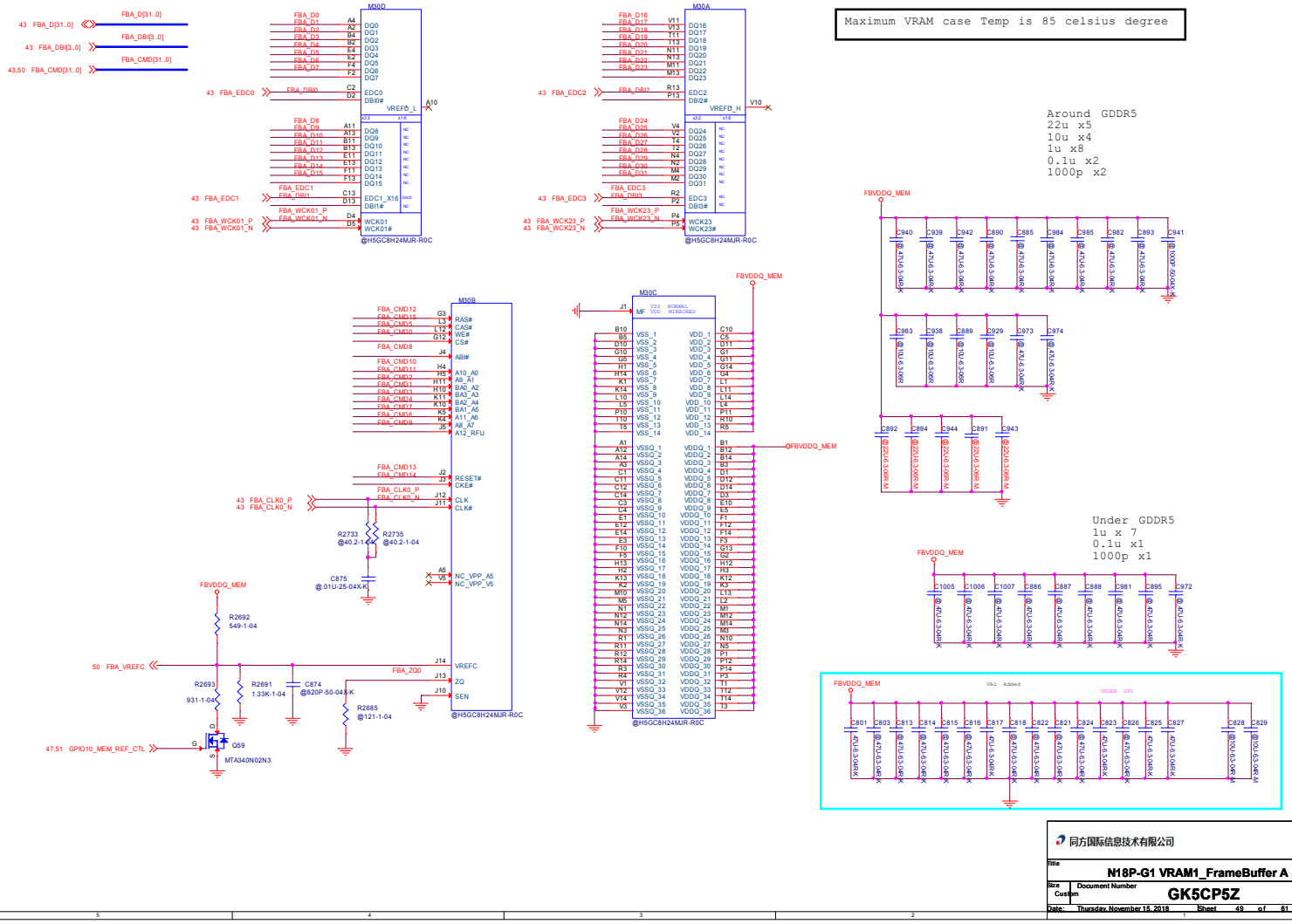
Title	N18P-G1 STRAP/Serial ROM	
Size C	Document Number GK5CP5Z	Rev A
Date: Wednesday, November 14, 2018	Sheet 46 of 61	


R2820 /C1453
N18P SET
N17 NC
I2CS: Only for Thermal Sensor
Only for GC6 use
R2807/R2810 NC FOR BOTH N17 & N18.
N18 件
N17 NC
同方国际信息技术有限公司
N18P-G1 GPIO/Thermal/I2C
GK5CP5Z
Monday, November 19, 2018
47 of 61

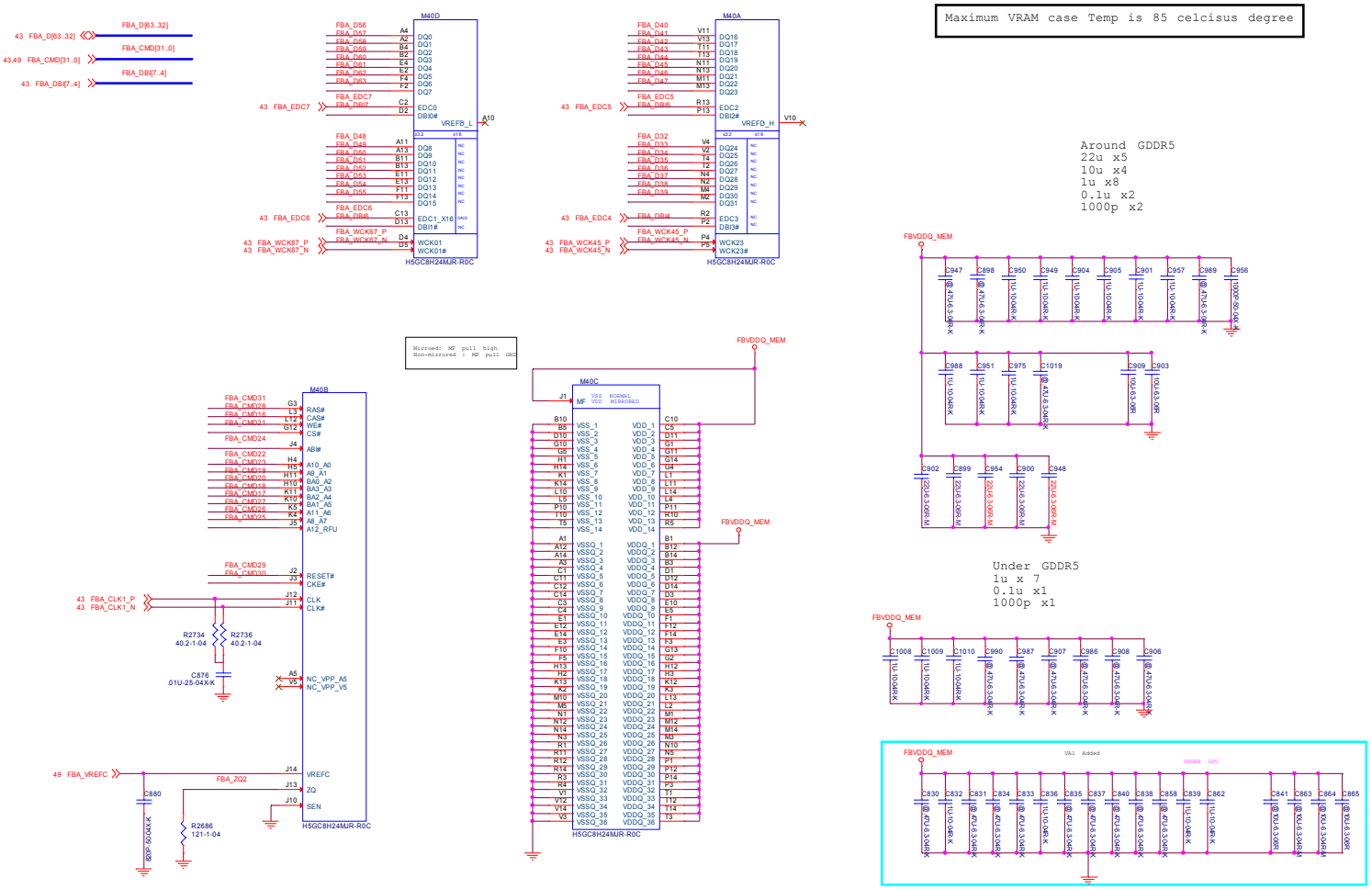


同方国际信息技术有限公司

Title	N18P-G1 POWER	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Thursday, November 15, 2018	Sheet 48 of 61	


Maximum VRAM case Temp is 85 celsius degree
Around GDDR5
22u x5
10u x4
1u x8
0.1u x2
1000p x2
Under GDDR5
1u x 7
0.1u x1
1000p x1
M30D
M30A
M30B
M30C
@H5GC8H24MJR-R0C
FBVDDQ_MEM
FBA_D[31..0]
FBA_DBI[3..0]
FBA_CMD[31..0]
FBA_EDC0
FBA_EDC1
FBA_EDC2
FBA_EDC3
FBA_WCK01_P
FBA_WCK01_N
FBA_WCK23_P
FBA_WCK23_N
FBA_CLK0_P
FBA_CLK0_N
FBA_VREFC
FBA_ZQ0
47,51 GPIO10_MEM_REF_CTL
MTA340N02N3
同方国际信息技术有限公司
N18P-G1 VRAM1_FrameBuffer A
GK5CP5Z
Thursday, November 15, 2018
49
61

Maximum VRAM case Temp is 85 celcisus degree

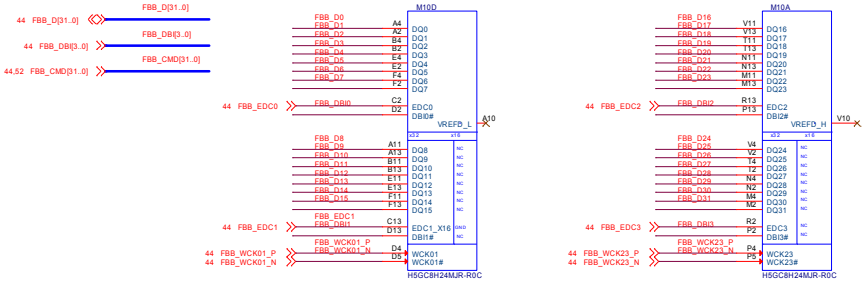


同方国际信息技术有限公司

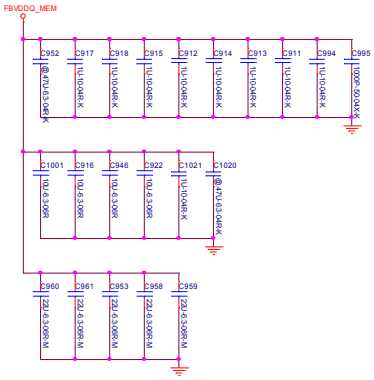
Title	N18P-G1 VRAM2_FrameBuffer A	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Thursday, November 15, 2018	Sheet 50 of 61	

Maximum VRAM case Temp is 85 celcisus degree

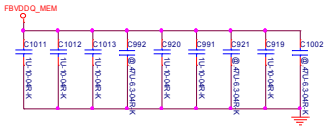
Mirrored: Pull high to VDDQ
Normal: GND

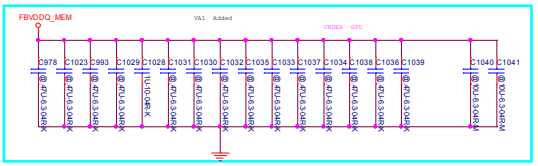


Around GDDR5
22u x5
10u x4
1u x8
0.1u x2
1000p x2



Under GDDR5
1u x 7
0.1u x1
1000p x1





同方国际信息技术有限公司

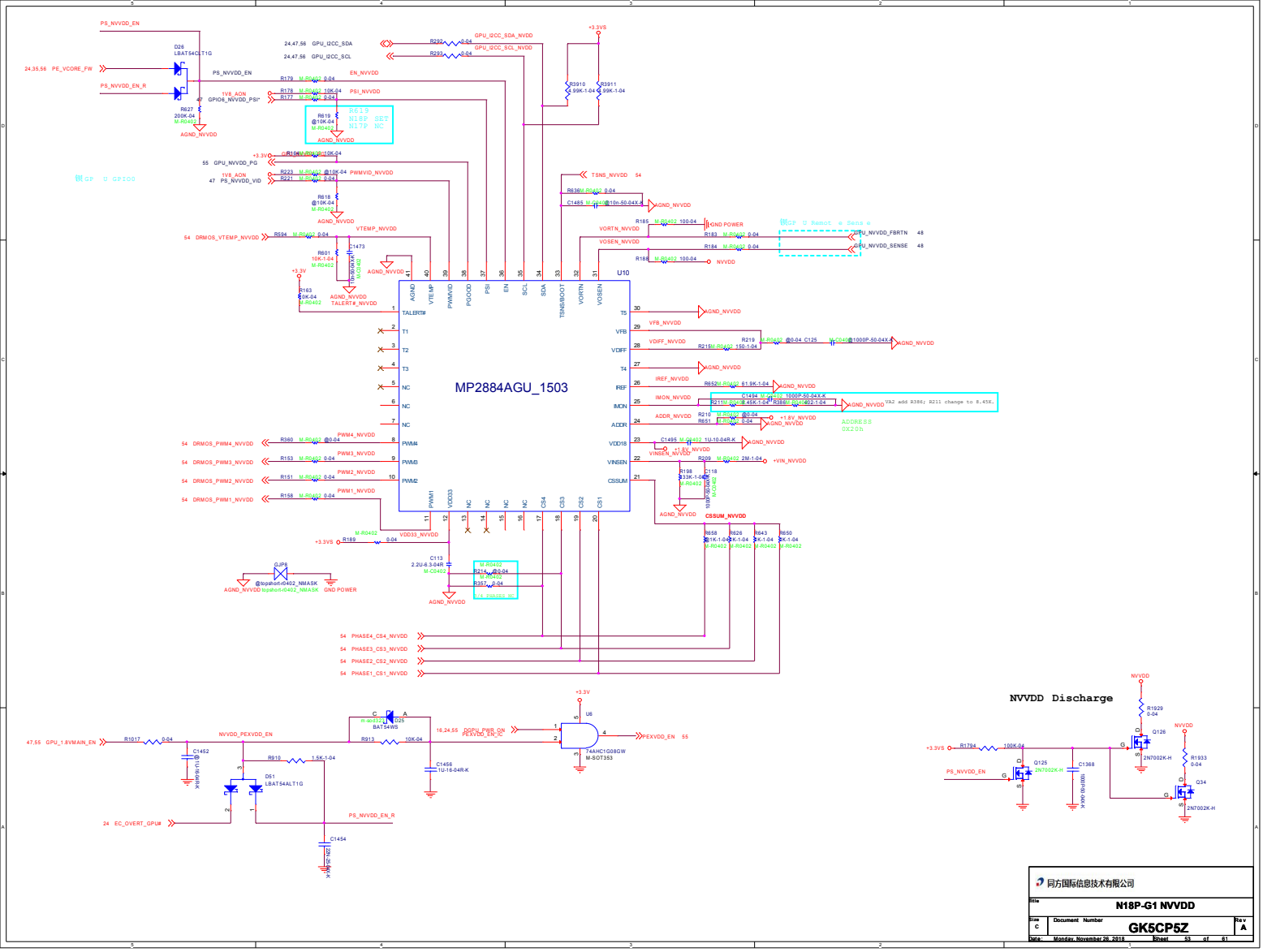
Title	N18P-G1 VRAM3_FrameBuffer B	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Thursday, November 15, 2018	Sheet 51 of 61	

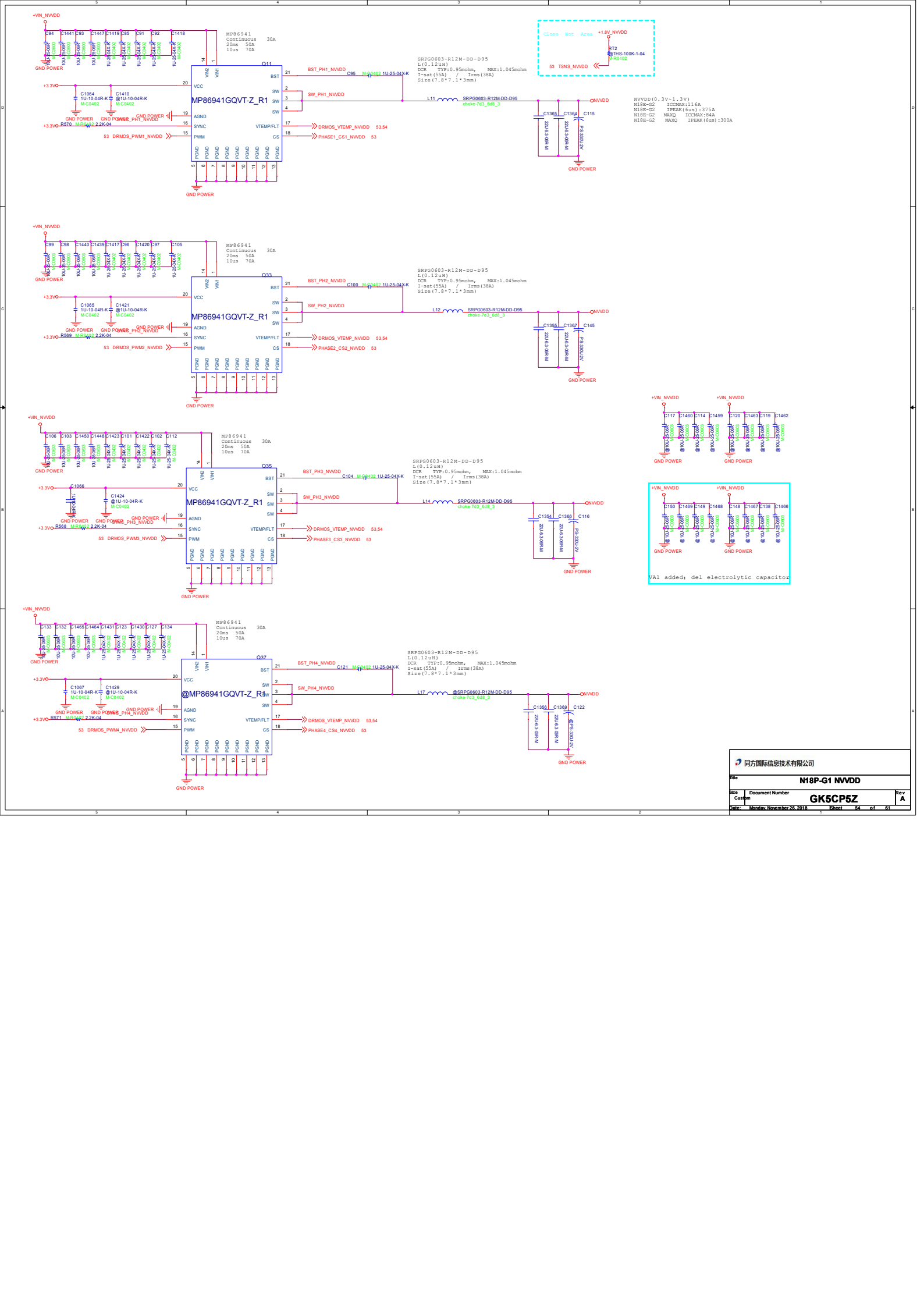
Maximum VRAM case Temp is 85 celcisus degree

Around GDDR5
22u x5
10u x4
1u x8
0.1u x2
1000p x2

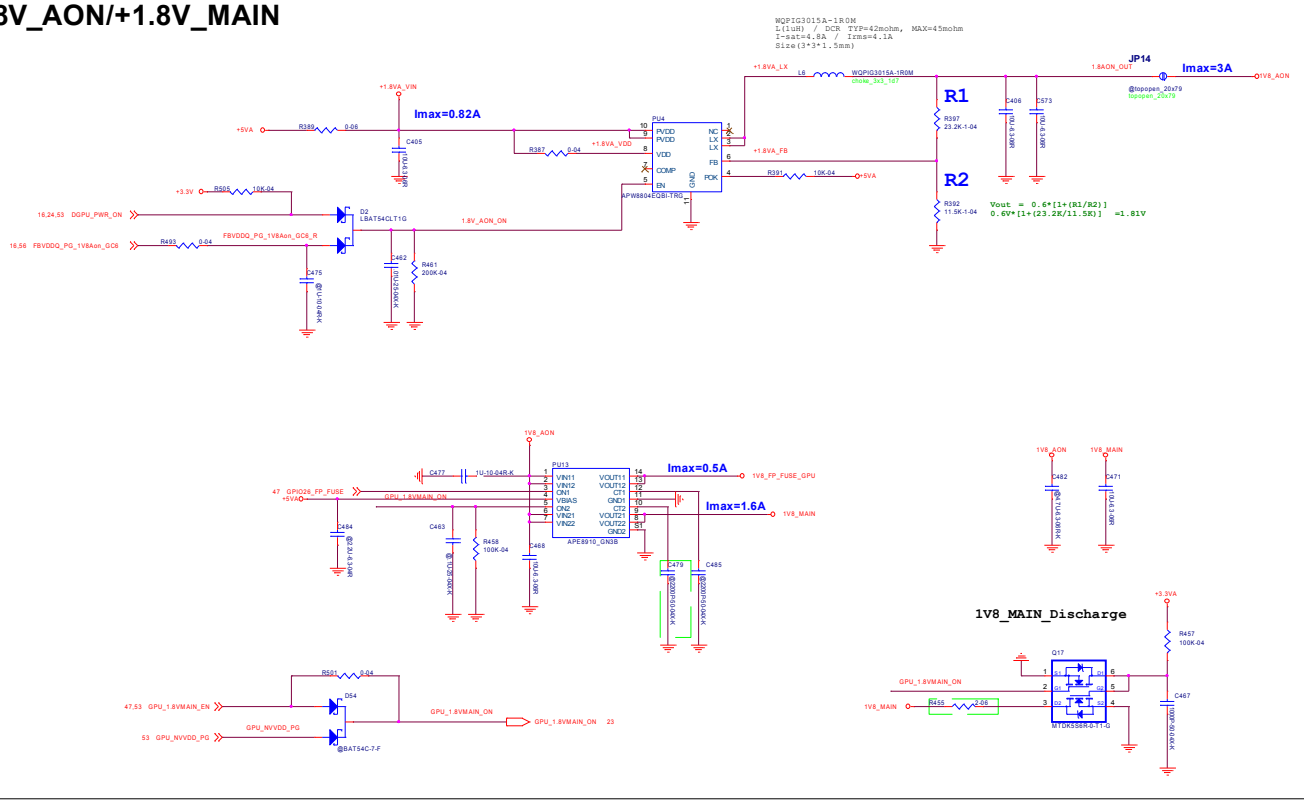
Under GDDR5
1u x 7
0.1u x1
1000p x1

同方国际信息技术有限公司	
Title	N18P-G1 VRAM4_FrameBuffer B
Size: Custom	Document Number: GK5CP5Z
Rev: A	
Date: Thursday, November 15, 2018	Sheet 52 of 61

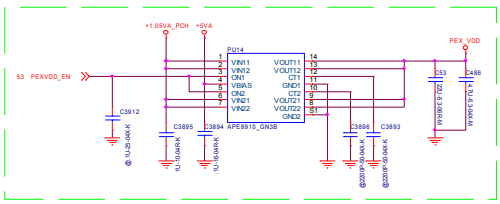

MP2884AGU_1503
U10
NVVDD Discharge
同方国际信息技术有限公司
N18P-G1 NVVDD
GK5CP5Z
Monday, November 26, 2018
Sheet 53 of 61

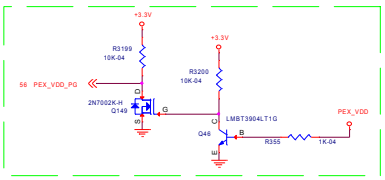

+VIN_NVVDD
MP86941
Continuous 30A
20ms 50A
10us 70A
Q11
MP86941GQVT-Z_R1
BST_PH1_NVVDD
SW_PH1_NVVDD
SRPG0603-R12M-DD-D95
L(0.12uH)
DCR TYP:0.95mohm, MAX:1.045mohm
I-sat(55A) / Irms(38A)
Size(7.8*7.1*3mm)
L11
NVVDD
Close Hot Area
+1.8V_NVVDD
RT2
THS-100K-1-04
53 TSNS_NVVDD
NVVDD(0.3V~1.3V)
N18E-G2 ICCMAX:116A
N18E-G2 IPEAK(6us):375A
N18E-G2 MAXQ ICCMAX:84A
N18E-G2 MAXQ IPEAK(6us):300A
DRMOS_VTEMP_NVVDD 53,54
PHASE1_CS1_NVVDD 53
DRMOS_PWM1_NVVDD
Q33
BST_PH2_NVVDD
SW_PH2_NVVDD
L12
DRMOS_VTEMP_NVVDD 53,54
PHASE2_CS2_NVVDD 53
DRMOS_PWM2_NVVDD
Q35
BST_PH3_NVVDD
SW_PH3_NVVDD
L14
DRMOS_VTEMP_NVVDD 53,54
PHASE3_CS3_NVVDD 53
DRMOS_PWM3_NVVDD
Q37
@MP86941GQVT-Z_R1
BST_PH4_NVVDD
SW_PH4_NVVDD
L17
DRMOS_VTEMP_NVVDD 53,54
PHASE4_CS4_NVVDD 53
DRMOS_PWM4_NVVDD
VA1 added: del electrolytic capacitor
同方国际信息技术有限公司
Title N18P-G1 NVVDD
Size Custom
Document Number GK5CP5Z
Rev A
Date: Monday, November 26, 2018
Sheet 54 of 61

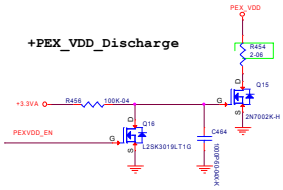
+1.8V_AON/+1.8V_MAIN



PEX_VDD





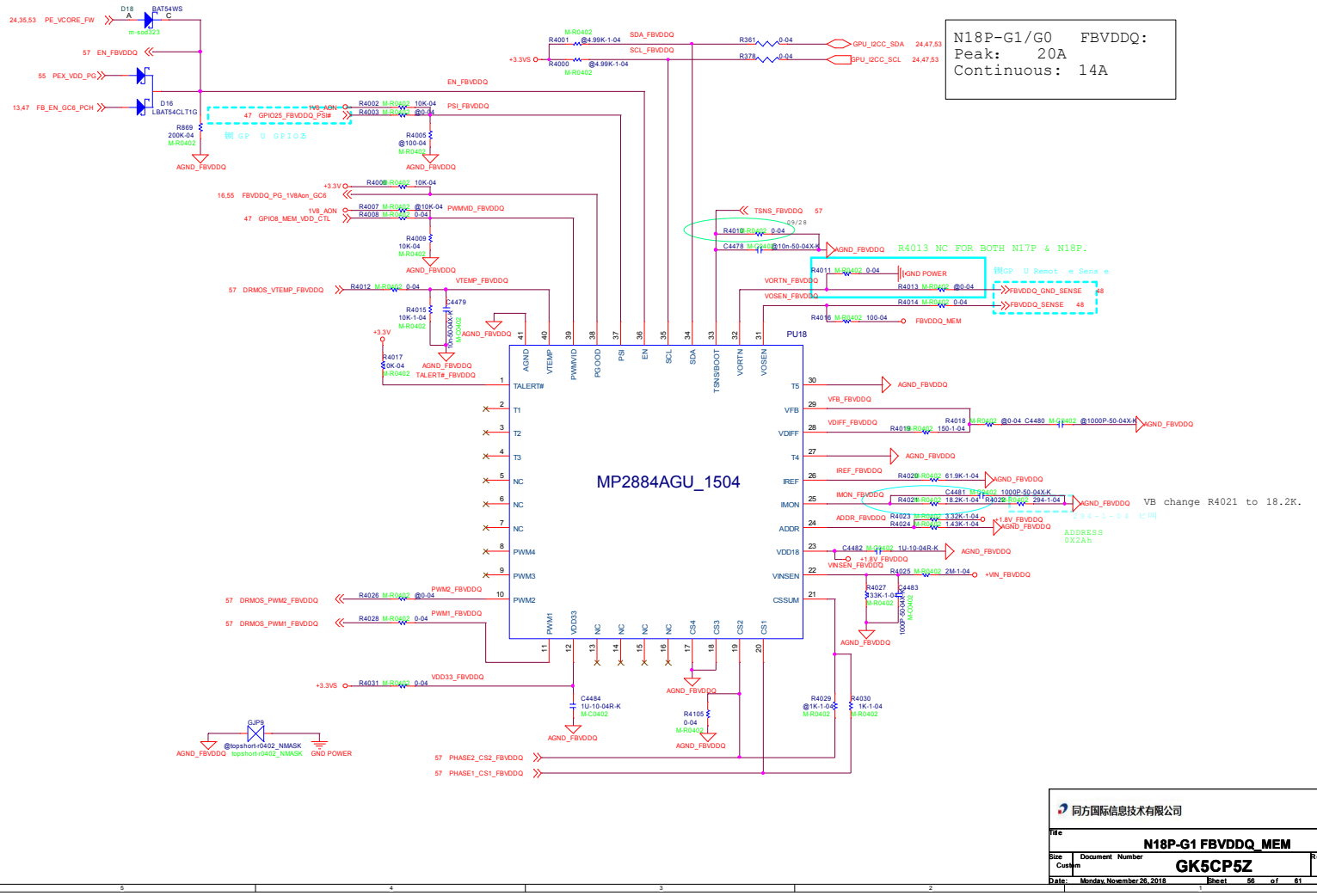


同方国际信息技术有限公司

Title	N18P-G1 1V8_AON/1V8_MAIN/PEX		
Size C	Document Number GK5CP5Z		Rev A
Date: Friday, November 02, 2018	Sheet 55 of 61		

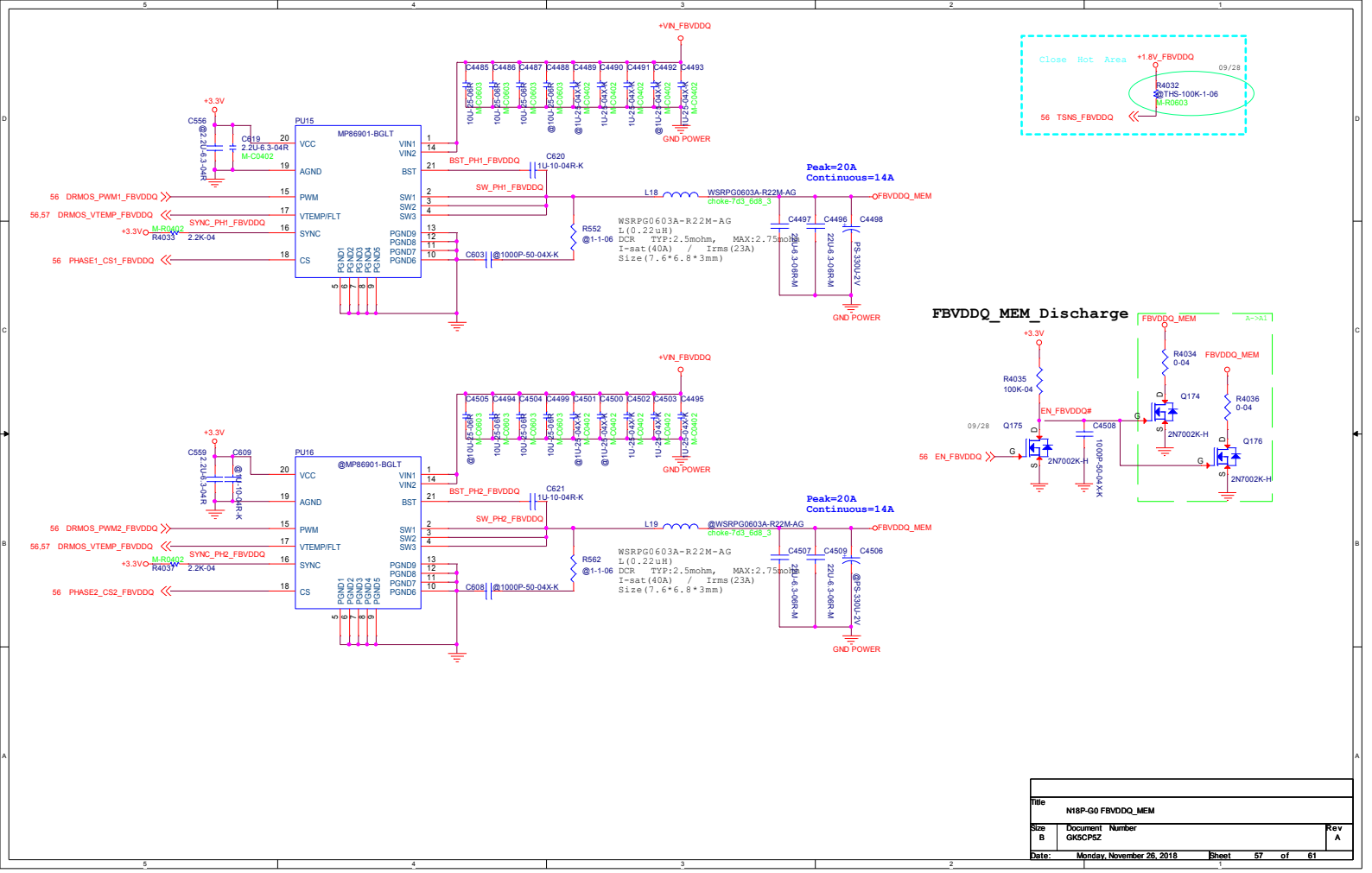
GP

FBVDDQ_MEM



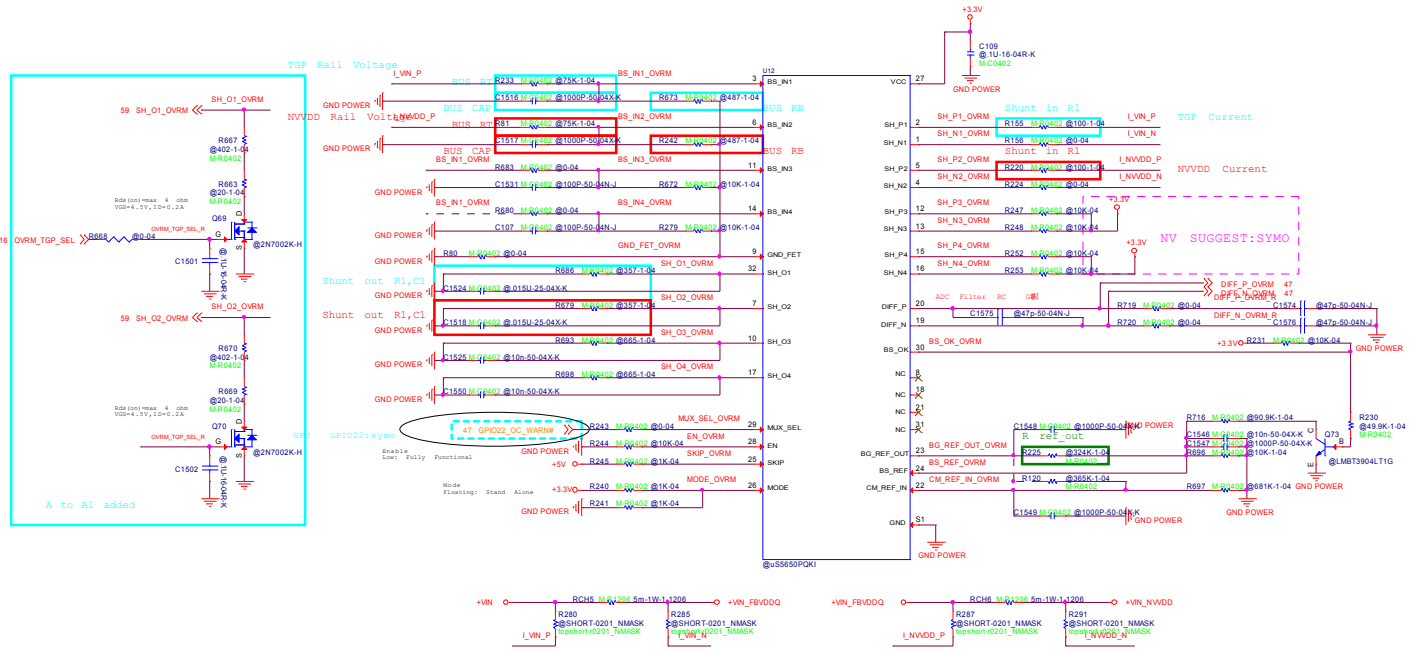
同方国际信息技术有限公司

Title	N18P-G1 FBVDDQ_MEM		
Size: Custom	Document Number: GK5CP5Z		Rev: A
Date: Monday, November 26, 2018	Sheet 56 of 61		



Title	N18P-G0 FBVDDQ_MEM	
Size B	Document Number GK5CP5Z	Rev A
Date: Monday, November 26, 2018	Sheet 57 of 61	

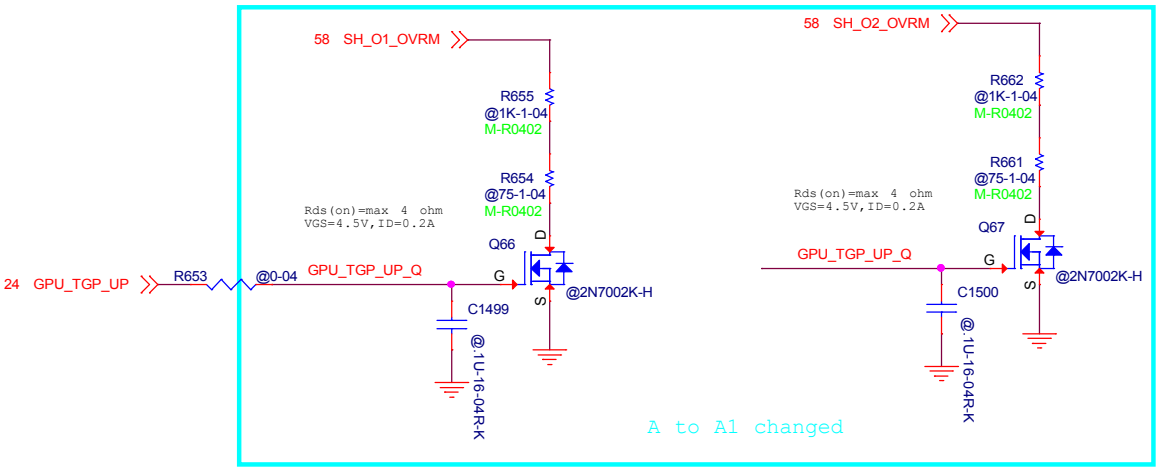
NC ALL FOR N17P



GPU	Component Values				
	R673,R242	R686,R679	R225	R233,R81	C1516,C1517
N18P-G0	487Ω	357Ω	324KΩ	75KΩ	1.0nf
N18P-G0 MAX-Q					
150W+	487Ω	127Ω	324KΩ	75KΩ	1.0nf
115W to 130W	487Ω	143Ω	324KΩ	75KΩ	1.0nf
100W to 110W	487Ω	165Ω	324KΩ	75KΩ	1.0nf
75W to 90W	487Ω	215Ω	324KΩ	75KΩ	1.0nf
70W or lower	487Ω	357Ω	324KΩ	75KΩ	1.0nf

同方国际信息技术有限公司

Title	N18P-G0 OVRM	
Size: Custom	Document Number: GK5CP5Z	Rev: A
Date: Thursday, November 15, 2018	Sheet 58 of 61	



TGP Control / TGP Watt	GPU_TGP_UP	OVRM_TGP_SEL
OVER 130W	HIGH	HIGH
100W TO 110W	HIGH	LOW
115W TO 130W (7S)	LOW	HIGH
75W TO 90W (7Z)	LOW	LOW

同方国际信息技术有限公司

Title	N18P-G0 TGP	
Size A	Document Number GK5CP5Z	Rev A
Date: Thursday, November 15, 2018	Sheet 59 of 61	

GK5CN5Z A->A1 change list:
1.Erplot6 power off over 0.5W issue(close VCORE program mode)
POP R352 10K-04
R303 10K-04->0-04
EC GPC4(PIN120) connect to R303
2.Correcting PCH_PWROK,SYS_PWROK & PM_RSMRST# series resistors
R249,R282 and R232 connect to EC
POP R108 100K-04
R126 1.05VA_PCH_PG->5VA_PG
3.CNEDP1 PIN19 change to +3.3V_LCD for 4K PANEL
CNEDP1.19 from GND change to +3.3V_LCD
4.MP2949AGQKT VIN_SEN 1/16 divider network
R336 2M-1-04,R332 133K-1-04
5.PEX_VDD LDO -> Low switch for NV sequencing
PU14 APL5934BKAI-TRG(LDO)->APL3523QBI-TRG(low switch)
R454 10-06 ->2-06
6.FBVDDQ_MEM discharge circuit modify to dual path
Add Q139 2N7002K-H
7.PCH PCIE change
PCIE6(NA) -> PCIE15 WLAN
PCIE5(GbE)-> PCIE14 LAN
8.typec usb2.0 (usb 5) reverse modify
USB_PP5,USB_PN5 swap
9.ME KB ID PIN pull high resitor 1%
R283 10K-04->10K-1-04
Add C184
10.+VPHY_1P24
POP C4T 10U-6.3-06R
11.+VCCPHVLDO_1P8
R25 +1.8VA->+VCCPRIM_1P8
12.GPU SMBUS to EC SMBUS reverse modify
PCH_SML1CLK & PCH_SML1DAT SWAP
13.FAN CONN change 3PIN to 4PIN
Remove U14 & U16 APL5607AKI-TRG
CNFAN1 & CNFAN2 WB,3P,SMT,P1.25,3800K-F03N-03LENT->CON_WB_4H125_3800K-F04N_ENT
14.NVDD discharge circuit modify
MTDK5S6R-0-T1-G change to 2N7002K-H
15.EDP power sequencing
Q101 remove
add Q49 2N7002K-H,Q113 MTDK5S6R-0-T1-G change to 2N7002K-H
R373 82K-1-04->220K-1-04
C452 .47U-25-04R-K->1U-10-04R-K
16.Detect ID thickness
CNAUDIO1,22 add net THICKNESS_ID_DET
EC U5.82(GPE1) add net THICKNESS_ID_DET
17.EC detect ME KB US or UK sequecing
EC U5.104(GPG6) add net SUS_ON
ADD D17
PU5.15, PU6.3, PU7.3 and PU19.3 PM_SLP_S4#->SUS_ON_S4#
18.DCIN SAFTY_PROTECT combine to TI charger ic
Delete Q41, Q43, Q120 and other component
19.HDMI & DP hot plug add pull low resistor
change R133 100K-04 to pull low
20.+VCORE off sequencing modify
Add D24 BAT54WS
21.PEX_CLKREQ# level shift mos change
Q78 2N7002K-H->L2SK3019LT1G
22.1V8_MAIN sequencing
UNPOP C479
R455 10-06 -> 2-06
23.+5VA choke 3mm->2mm for ME
L15 WSRPG0603-2R2M-H->EM-15AM28V01
24.VCCST_PG sequencing tuning
remove U1
Q6.2 net name change to EN_VCORE
25.CNVI follow check list
R227 R228 22-1-04 -> 0-04
R612 R614 33-1-04 -> 0-04
Reserve C33
26.Mini DP & HDMI Hot plug
Remove Q28, Q33, Q35
R674 51K-1-04, R637 0-04, R639 0-04
27.Crystal tuning
C5, C6 22P-50-04N-J -> 15P-50-04N-J
C1405, C1409 18P-50-04N-J -> 33P-50-04N-J
28.PJP change to Short plane
Remove PJP2, PJP5, PJP7, PJP8, PJP10, PJP11
29.ME KB ADD ESD
Remove R139, R153,R120
Add D60~D73
30.HDMI SI tuning
Q86 L2SK3019LT1G->LMBT3904LT1G
R430 4.7K-04->100-04
31.AC VIN input add H:4mm CAP
Add C574, C597, C598 EEEHS1E330L
32.ME request two RTC BAT CONN
Add CNRTC2
33.SPK PIN SWAP for ME
ACN1 SWAP

GK5CN5Z A->A1 change list:
34.DCIN JACK change
CNDCIN1 DCIN_WO_2DC3003-002211_SIN->CON_DCIN_WO_2DC3003-016211F_SIN
35.+5VA voltage target change to 5.142V for loss
R448 23.2K-1-04, R450 4.3K-1-04
36.SPK beat placement change for EMI request
Del R125, R252, R285, R287
37.Battery only leakage current improving
R442 220K-1-04 -> 2M-04, R451 100K-1-04 -> 1M-04
R438,R437,R218,R203,R199,R217,R297, R359 470K-04->1M-04
R194 93.1K-0.1-04->196K-1-04
R187 13.3K-0.1-0402->28K-1-04
38.RTC battery tuning
UNPOP R382
39.EMI request
UNPOP L23 , L29 , L35 , L36
POP R312, R453, R329, R327, R462, R469, R468, R465
AB11, AB12, AB8, AB9 BD-FCM1608KF-600T07->FCM1608KF-121T06
POP C1005, C1006, C988, C951, C921, C924, C1000 33P-50-04N-J

GK5CN5Z A1->A2 change list:
1.+5V_AMP modify
Remove AB10
2.AB8, AB9, AB11, AB12 FCM1608KF-121T06 -> BD-HCB1608KF-120
3.CNSSD1 support NVMe
PCIE 17-20 -> PCIE 21-24

GK5CN5Z A2->A3 change list:
1.CNKB1 +5VS modify
Add PU17 to seperate KB power control by EC
2.Q8 soft start modify
C3556 1U-25-04X-K ->47n-16-04X-K
UNPOP C3582
3.+VCORE & NVDD +VIN INPUT CAP modify for fast transient
C329,C326,... 1U-25-06R-K->10U-25-06R
C1372,C1370,... 1U-25-06R-K->10U-25-06R

GK5CN5Z A3->B change list:
1.Q8 soft start modify
Reserving R460 for discharge
C3582 10n-50-04X-K
2.Jumper modify
GJP1,GJP2,GJP3,GJP4,GJP6,GJP7 -> TOPSHORT_20X30 ->topshort-r0402_NMASK
GJP5 topshort-r0402->topshort-r0402_NMASK
Remove PJP1,PJP6,PJP9,PJP12
3.Remove All MEKB ESD
Remove D60 - D73
4.Short +5VS to +5V_MEKB
Add R120
UNPOP PU17...
5.MEKB new PIN definition
GPA7 net name change to MEKB_PWM LED_BDID
GPJ2 net name change to A_COVER_LED
GPI2 net name change to MEKB_INT#
6.+5VA noise reduce
R449 360K-1-04->270K-1-04
Add R474
7.NVDD MLCC TOP & BOT reducing noise
Remove C2821
8.+5VA increase voltage for USB Droop
R448 23.2K-1-04->23.7K-1-04
9.TYPEC CC PIN power change
R632, R793 +5V->+5V_TYPEC
10.All USB port power from +5VS to +5VA
CNUSB1,5 +5VS_CR_CN
R146,U27.2,U27.3,R142 +5VS->+5VA
11.DFM check list request
POP C669 1U-10-04R-K
12.reserve internal 1.8V VRM solution
Delete R26
R610,R616,R611 +1.8VA->+VCCPRIM_1P8
13.BAT_SMB driving improving
R144,R145 4.7K-04->1K-04
14.MP2949AGQKT reserve 3.3V option
Add R356
15.R3314,R3315 100-1-04-> 10-1-04
16.CNVI CLKIN_XTAL CAP filter
C33 10P-50-04N-J

GK5CN5Z B->V1.0 change list:
1.QKEY reserve
POP R205,R206 0-04
Add R624,R625

GK5CN5Z V1.0->V1.1 change list:
1.CLKOUT_LPC0 noise reducing
Add C474 22P-50-04N-J
2.BAT SMBUS compatible tuning
R144 & R145 1K-04 -> 2.2K-1-04
3.+1.05VA_PCH inrease voltage
R399 3.01K-1-04
R394 9.76K-1-04
4.Support Subwoofer
POP R161 0-04

GK5CN5Z V1.1->V1.2 change list:
1.+3.3V add twice Low switch
Add PU23, C599, C481
2.CHG_REF CAP value change
C353,C355 1U-10-04R-K->2.2U-6.3-04R
3.BAT_I ZERO-I accuracy modify
Add R347 100K-1-04
UNPOP R326
4.Support 3.6V 144HZ PANEL
Add U18 LDO IC & related component
discharge circuit Q49 & Q113 modify
5.Remove SPI FP, Add USB FP
Remove PCH_GSPI1_CLK...
Add USB_PP10 & USB_PN10

GK5CN5Z V1.1->V1.2 BOM change list:
1.DCIN MOS
Q8,Q9 MTB06N03H8 -> MTB2D5N03BH8-0-T6-G
2.+3.3V Dual LOW SWITCH
POP PU23 APE8910_GN3B
3.+3.3VA Voltage increase to 3.4586V
R443 56.2K-1-04 ->44.2K-1-04
R452 18K-1-04 -> 13.3K-1-04
4.ME_KB_ID pull high modify
R283 10K-1-04 ->11.8K-1-04
5.WEBCAM USB 0 ohm -> common choke
UNPOP R528,R542 0-04
POP L16 QTCW2012EH4-120-LF
C669 1U-10-04R-K->33P-50-04N-J
6.IR CAMERA POWER CAP
C555 POP 33P-50-04N-J

Title	HISTORY	
Size C	Document Number GK5CP5Z	Rev A
Date: Friday, November 02, 2018	Sheet 60 of 61	

1. Add a I2C circuit of NVVDD, FBVDDQ power IC for EC control, as below
   a. Remove 'EC_WEBCA_ON' and 'CHG_REF' of EC function
   b. Let PCH_LCDBKL_EN to connect GPC6 of EC
   c. Let QKEY0# to connect GPJ5 of EC
   d. Let CNEDP1 pin 40 connect to TP59.
   e. Let GPU_TGP_UP to used for Project ID strap pin
   f. Let GPU_PWR_SMDAT3, GPU_PWR_SMCLK3 to connect NVVDD PWR CTRL IC that is through R292, R293.
   g. Let GPU_PWR_SMDAT3, GPU_PWR_SMCLK3 to connect FBVDDQ PWR CTRL IC, that is through R361, R378
   h, Modify enable circuit of NVVDD, FBVDDQ power rail. Let PE_VCORE_FW to connect enable pin that is through OR gate. (Add D18, D26, R627)
2. Change CNWLAN1 of footprint from CON_M2-E-S30_NFSE0-S6701_ARG to CON_M2-E-S48_NXSE0-S6701_ARG
3. Add a 3.3V level shift circuit (Q89) between DP_AUX_PORT_EN and GPU_1.8VMAIN_ON to prevent if MOSFET cannot turn on.
4. Change CNFP1 fo Pin count from 8pin to 4pin. Re-arrange pin assignment.
5. Change CNKB1, CNAUDIO1 of value from FFC,40P,P0.5,6718K-Y40N-00L,ENT to FFC,40P,SMT,P0.5,FP243A-040G1AM,JXT. Follow connector list.
6. Modify +1.2VS_DDR power circuit for system memory to do overclock function, as below
   a. Add R572,R423,R566,R567,Q147 and let MEM_OVERCLK_EN to control PU4 of feedback voltage for adjust +1.2VS_DDR voltage from 1.2V to 1.35V.

VA1 CHANGE LIST

7. Remove PCB thermal monitor function. Delete R278, RT10.
8. Let DGPU_PWR_ON to connect EC GPI1 and set to input. It's for smart APC
9. Modify TGP offset circuit,Add R653,R654, R655, R661, R662,Q66,Q67 to adjust TGP offset setting when GPU_TGP_UP is high.
10. Add R574,R575(100K) PD resistor to prevent leakage voltage.
11. Add C602 10uF for decrease overshoot voltage
12. 10/15 DEL AGND FOR U13,U14,U1,PU5. DEL JP8 for +3.3VA.
13. Change U27 of footprint from MSOP8 to SOT23-5, The P/N is EM5213J-30
14. Modify BAT_I circuit for improve output accuracy
    a. Change RCH1, RCH2 of value from 15mohm to 30mohm
    b. Add R878 and let it connect between GND_PWR and BAT_I input +
    C. Add R877 and let it connect between GND_PWR and BAT_I input -
15. 10/22 change R442 to 300K, R451 to 150K, change R449 to 750k, change C436 to 10nf,
    add RC R577&C540, add snubber C541&R578.
16. 10/26 NC R825, SET R820 for N18P.
17. 10/27 NC R4013, R4011=0ohm for N18P/ SET R4013, R4011=100ohm for N17P
18. 11/2 NC C494,C425,C599,C481 to fix DGPU Dr.MOS sequence.
19. 11/2 change C3575,C3577 from 0805 to 0603.
20. 11/2 NC R52 as EC internal PU.
21. 11/2 change PU8 value from MP2949AGQKT to MP2949AGQKT_1041.
22. 11/2 change CNFP1 value for BOM.
23. 11/2 change Q11,Q33,Q35,Q37 value to MP86941GQVT-Z_R1.
24. 11/2 change R209,R4025 to 2M; R198,R4027 to 133K.
25. 11/2 SET R3310 to follow TI suggestion.

VA2 CHANGE LIST

26. 11/16 change R344 from 10mohm to 5mohm.
27. 11/16 NC R625 for IDR/S add LED.
28. 11/19 change R2770 from 100K to 10K according to NV.
29. 11/21 change U10 PIN8 net name to 'PWM4_NVVDD'.
30. 11/21 reserve C1064, C1065, C1066, C1067, C609, C619 close to Dr.MOS for MPS requirement.
31. 11/22 change PU18 value to 'MP2884AGU_1504', change R4021 from 30.1k to 18.2K.
32. 11/22 change C540 to 2.2nf, C451 to 10nf, R448 to 23.2K for 5VA voltage.
33. 11/25 Change R435 from 10K to 4.7K follow 7s.
34. 11/25 Change R610 from 4.7K to 10K follow 7S.
35. 11/25 Change AB11,AB12,AB8,AB9 to QTLC201210CB-4R7M-LF(0805) for reduce SPK noise follow 7S.
36. 11/25 add C552 for +5VA.
37. 11/25 change R146,R12 to 0805 short pad.
38. 11/25 change R104,R142,R143,R238,R406,R482,R237 to 0603 short pad.
39. 11/25 add R386; R211 change to 8.45K for NVVDD IMON.
40. 11/25 change PU18,U10 PIN T4&T5 connect to GND for MPS request.

Title	<Title>	
Size: C	Document Number: <Doc>	Rev: A
Date: Monday, November 26, 2018	Sheet 61 of 61	