South Peak 15" MLK Schematics

Alder Lake-P

2021-05-19

REV:SB

DY : None Installed
UMA: UMA only installed
OPS: DISCRETE OPTIMUS installed

<Core Design>

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Size A4	Document Number SouthPeak15 MLK	Rev SB
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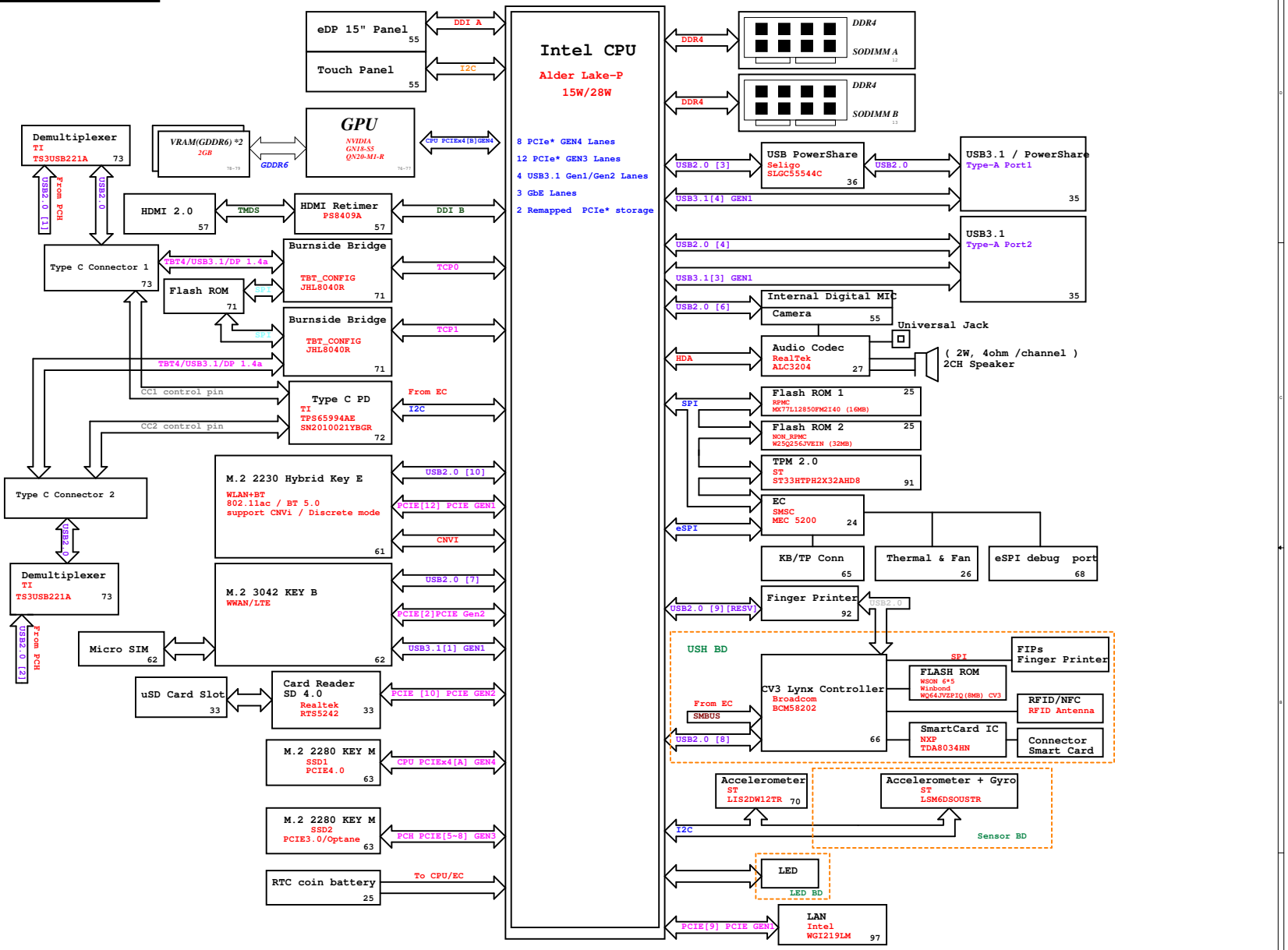
Project code :
RFQ - > QRQY00013546
SouthPeak 15 - > 4PD0PH010001
SouthPeak 15P - > 4PD0PG010001
PCB P/N : 203102
Revision : SB

South Peak 15" MLK Block Diagram



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Title: Block Diagram

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Main Func = CPU

[24,39] THERMTRIP_CPU_N
[22,44,72] PROCHOT_PD_R_N
[22,24,46] PROCHOT_CPU_N

[24] PECI_CPU
[15,99] DBG_PMODE

[99] CPU_EAR

[99] CPU_JTAG_TRST_N
[99] CPU_JTAG_TMS
[99] CPU_JTAG_TDO
[99] CPU_JTAG_TDI
[99] CPU_JTAG_TCK
[99] CPU_JTAG_PREQ_N
[99] CPU_JTAG_PRDY_N

[99] PCH_JTAG_TCK

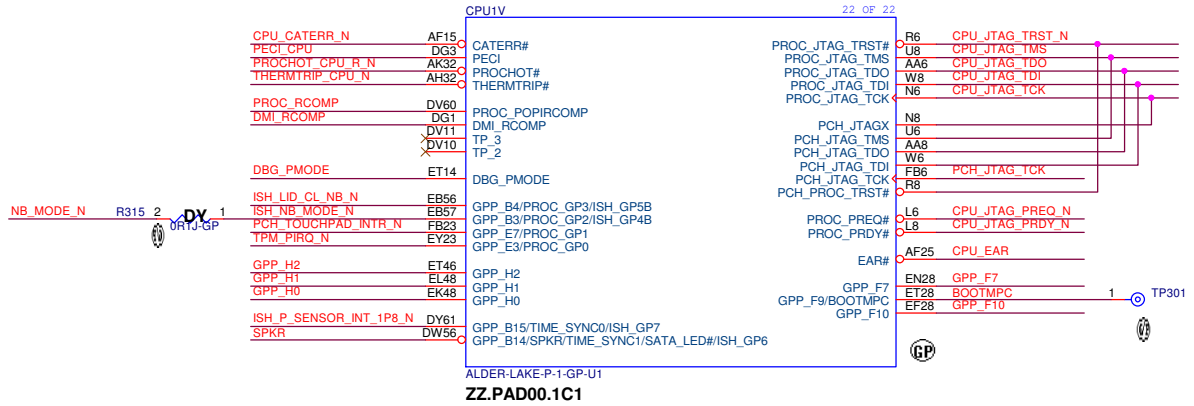
[91] TPM_PIRQ_N
[56] ISH_P_SENSOR_INT_1P8_N

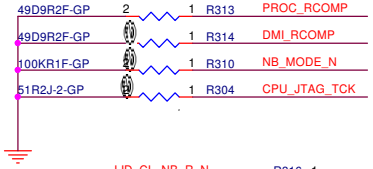
[24,65] PCH_TOUCHPAD_INTR_N
[24,27] SPKR

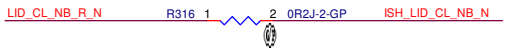
[24] NB_MODE_N
[24] LID_CL_NB_R_N

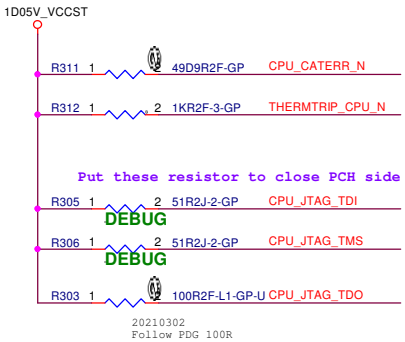
[15] GPP_F7
[15] GPP_F10

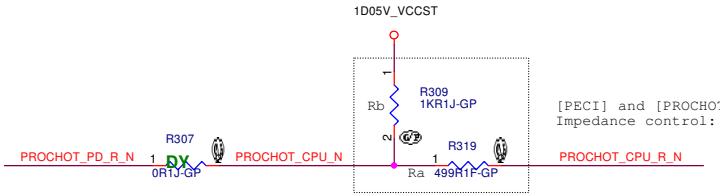
[15] GPP_H0
[15] GPP_H1
[15] GPP_H2











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Title: CPU (THML/JTAG)

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Main Func = CPU

eDP

[55] eDP_TX_CPU_N3
[55] eDP_TX_CPU_P3
[55] eDP_TX_CPU_N2
[55] eDP_TX_CPU_P2
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1
[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P

[55] EDP_HPD
[55] eDP_VDDEN_CPU
[55] eDP_BLEN_CPU
[55] eDP_BLCTRL_CPU

DP to MUX

[57] DP_DDI_TX_P3
[57] DP_DDI_TX_N3
[57] DP_DDI_TX_P2
[57] DP_DDI_TX_N2
[57] DP_DDI_TX_P1
[57] DP_DDI_TX_N1
[57] DP_DDI_TX_P0
[57] DP_DDI_TX_N0

[57] DP_HPD_CPU

[57] CPU_DPB_CTRL_CLK

[57] CPU_DPB_CTRL_DATA

USB-C Port1

[71] USB1_TCSS_TX_N0
[71] USB1_TCSS_TX_P0
[71] USB1_TCSS_TX_N1
[71] USB1_TCSS_TX_P1
[71] USB1_TCSS_RX_N0
[71] USB1_TCSS_RX_P0
[71] USB1_TCSS_RX_N1
[71] USB1_TCSS_RX_P1
[71] USB1_TCSS_AUX_N
[71] USB1_TCSS_AUX_P

USB-C Port2

[71] USB2_TCSS_TX_N0
[71] USB2_TCSS_TX_P0
[71] USB2_TCSS_TX_N1
[71] USB2_TCSS_TX_P1
[71] USB2_TCSS_RX_N0
[71] USB2_TCSS_RX_P0
[71] USB2_TCSS_RX_N1
[71] USB2_TCSS_RX_P1
[71] USB2_TCSS_AUX_N
[71] USB2_TCSS_AUX_P

[71] TBT_0_LSX_TX
[15,71] TBT_0_LSX_RX

[71] TBT_1_LSX_TX
[15,71] TBT_1_LSX_RX

others

[65] KB_DET_N
[40] 3.3V_CAM_EN_N
[35] USB_OC1_N
[33] HOST_SD_WP_N

[62] WWAN_FULL_PWR_EN_R
[20,24] ISH_TABLE_MODE_N

HDMI 2.0

TBT

CPU1A — 1 OF 22

eDP_TX_CPU_P3	W3	DDIA_TXP_3	
eDP_TX_CPU_N3	AA3	DDIA_TXN_3	
eDP_TX_CPU_P2	AA1	DDIA_TXP_2	
eDP_TX_CPU_N2	AB1	DDIA_TXN_2	
eDP_TX_CPU_P1	AB3	DDIA_TXP_1	
eDP_TX_CPU_N1	AD3	DDIA_TXN_1	
eDP_TX_CPU_P0	AF1	DDIA_TXP_0	
eDP_TX_CPU_N0	AD1	DDIA_TXN_0	
eDP_AUX_CPU_P	AF3	DDIA_AUXP	
eDP_AUX_CPU_N	AG3	DDIA_AUXN	
	ER23	GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD	
	ET23	GPP_E23/DDPA_CTRLDATA	
EDP_HPD	EV25	GPP_E14/DDSP_HPDA/DISP_MISC_A	
DP_DDI_TX_P3	AP6	DDIB_TXP_3	
DP_DDI_TX_N3	AP8	DDIB_TXN_3	
DP_DDI_TX_P0	AM6	DDIB_TXP_2	
DP_DDI_TX_N0	AM8	DDIB_TXN_2	
DP_DDI_TX_P1	AK6	DDIB_TXP_1	
DP_DDI_TX_N1	AK8	DDIB_TXN_1	
DP_DDI_TX_P2	AH6	DDIB_TXP_0	
DP_DDI_TX_N2	AH8	DDIB_TXN_0	
DDIB_AUXP	AE6	DDIB_AUXP	
DDIB_AUXN	AE8	DDIB_AUXN	
CPU_DPB_CTRL_CLK	EK46	GPP_H15/DDPB_CTRLCLK/PCIE_LINK_DOWN	
CPU_DPB_CTRL_DATA	EL46	GPP_H17/DDPB_CTRLDATA	
DP_HPD_CPU	EB47	GPP_A18/DDSP_HPDB/DISP_MISCB	
3.3V_CAM_EN_N	DV54	GPP_A21/DDPC_CTRLCLK	
KB_DET_N	DV52	GPP_A22/DDPC_CTRLDATA	
TBT_0_LSX_TX	ER26	GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD/BSSB_LS0_RX	
TBT_0_LSX_RX	ET26	GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD/BSSB_LS0_TX	
TBT_1_LSX_TX	EL26	GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD/BSSB_LS1_RX	
TBT_1_LSX_RX	EN26	GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD/BSSB_LS1_TX	
	FC37	GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/BSSB_LS2_RX/GSPI2_CS0#	
	EV37	GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/BSSB_LS2_TX/GSPI2_CLK	
	EY37	GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/BSSB_LS3_RX/GSPI2_MISO	
	FA37	GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/BSSB_LS3_TX/GSPI2_MOSI	
HOST_SD_WP_N	DY54	GPP_A17/DISP_MISCC	
WWAN_FULL_PWR_EN	EB49	GPP_A19/DDSP_HPD1/DISP_MISC1	
ISH_TABLE_MODE_PCH_N	EB51	GPP_A20/DDSP_HPD2/DISP_MISC2	
USB_OC1_N	DY47	GPP_A14/USB_OC1#/DDSP_HPD3/DISP_MISC3	
USB_OC2_N	DY49	GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4	
eDP_VDDEN_CPU	ET21	VDDEN	
eDP_BLEN_CPU	EN21	EDP_BKLTEN	
eDP_BLCTRL_CPU	EL21	EDP_BKLTCTL	

ALDER-LAKE-P-1-GP-U1

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TCP0_TXRX_P1	BE8	USB1_TCSS_RX_P1	TBT
TCP0_TXRX_N1	BE6	USB1_TCSS_RX_N1	
TCP0_TXRX_P0	BG8	USB1_TCSS_RX_P0	
TCP0_TXRX_N0	BG6	USB1_TCSS_RX_N0	
TCP0_TX_P1	AY3	USB1_TCSS_TX_P1	
TCP0_TX_N1	BB3	USB1_TCSS_TX_N1	
TCP0_TX_P0	BD3	USB1_TCSS_TX_P0	
TCP0_TX_N0	BE3	USB1_TCSS_TX_N0	
TCP0_AUX_P	BB1	USB1_TCSS_AUX_P	
TCP0_AUX_N	BD1	USB1_TCSS_AUX_N	
TCP1_TXRX_P1	AV8	USB2_TCSS_RX_P1	TBT2
TCP1_TXRX_N1	AV6	USB2_TCSS_RX_N1	
TCP1_TXRX_P0	AY8	USB2_TCSS_RX_P0	
TCP1_TXRX_N0	AY6	USB2_TCSS_RX_N0	
TCP1_TX_P1	AP3	USB2_TCSS_TX_P1	
TCP1_TX_N1	AR3	USB2_TCSS_TX_N1	
TCP1_TX_P0	AU3	USB2_TCSS_TX_P0	
TCP1_TX_N0	AW3	USB2_TCSS_TX_N0	
TCP1_AUX_P	AR1	USB2_TCSS_AUX_P	
TCP1_AUX_N	AU1	USB2_TCSS_AUX_N	
TCP2_TXRX_P1	BN8		
TCP2_TXRX_N1	BN6		
TCP2_TXRX_P0	BL8		
TCP2_TXRX_N0	BL6		
TCP2_TX_P1	BK3		
TCP2_TX_N1	BM3		
TCP2_TX_P0	BG3		
TCP2_TX_N0	BH3		
TCP2_AUX_P	BH1		
TCP2_AUX_N	BK1		
TCP3_TXRX_P1	BW8		
TCP3_TXRX_N1	BW6		
TCP3_TXRX_P0	BU8		
TCP3_TXRX_N0	BU6		
TCP3_TX_P1	BU3		
TCP3_TX_N1	BV3		
TCP3_TX_P0	BN3		
TCP3_TX_N0	BR3		
TCP3_AUX_P	BR1		
TCP3_AUX_N	BU1		
VSS_589	AL3		
TCP_RCOMP	AM1	TCSS_RCOMP R404 2K2R2F-GP	
DISP_UTILS_2	AF32		
DDIA_RCOMP	AJ1	eDP_RCOMP R401 150R2F-1-GP	
DDIB_RCOMP	AL1	DP2_RCOMP R402 150R2F-1-GP	
DISP_UTILS_1	DJ1		

TP401 TP402

ISH_TABLE_MODE_N R409 0R1J-GP DY

3D3V_S5_PCH

R407 10KR1J-GP USB_OC1_N
R408 10KR1J-GP USB_OC2_N
RN401 SRN100KJ-6-GP 3.3V_CAM_EN_N KB_DET_N

WWAN_FULL_PWR_EN_R R403 0R2J-2-GP WWAN_FULL_PWR_EN

3D3V_S0

R406 10KR2J-3-GP HOST_SD_WP_N

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Title: CPU (DDI/EDP)

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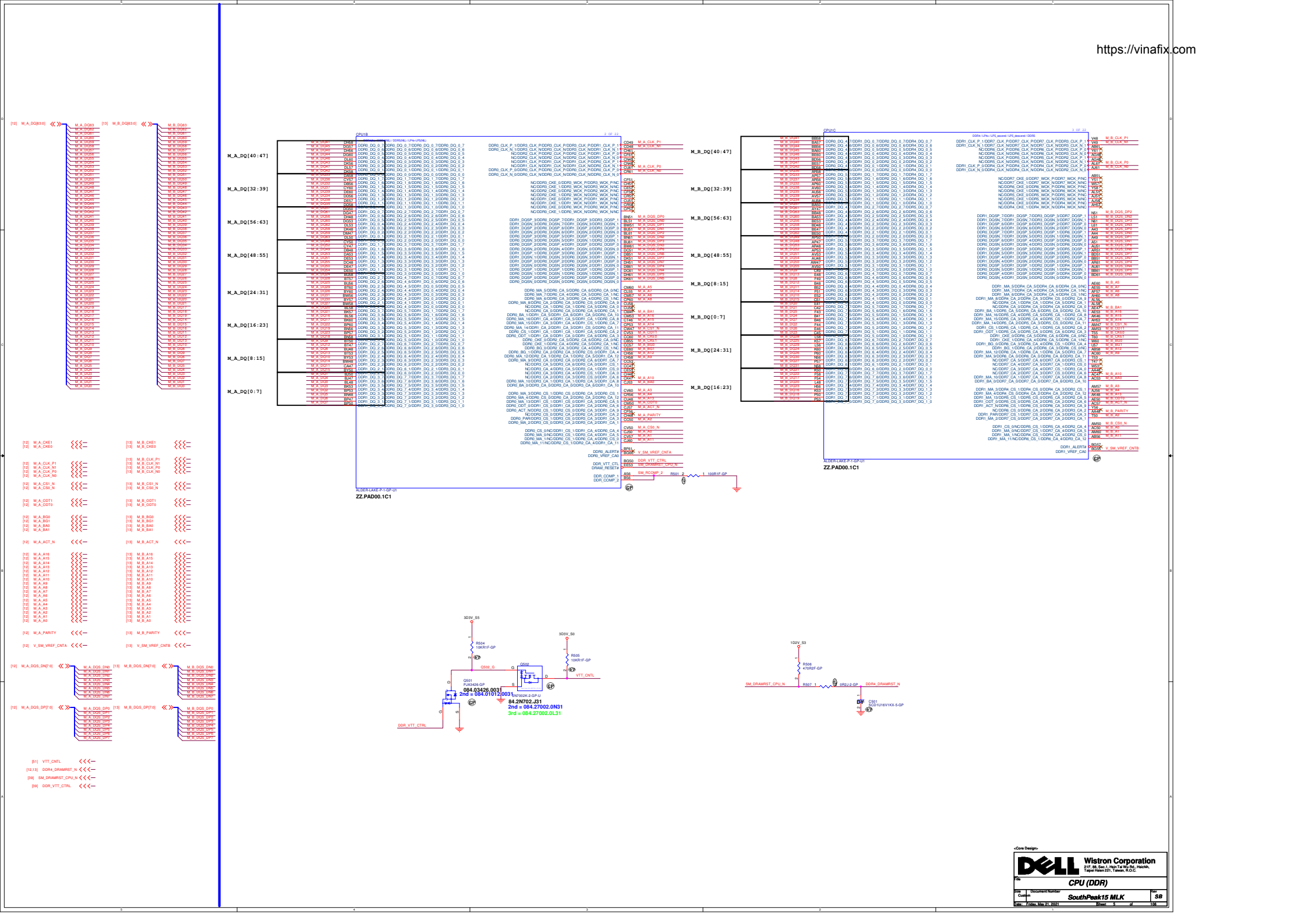

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Title	CPU (DDR)		
Size	Document Number		Rev
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Main Func = CPU

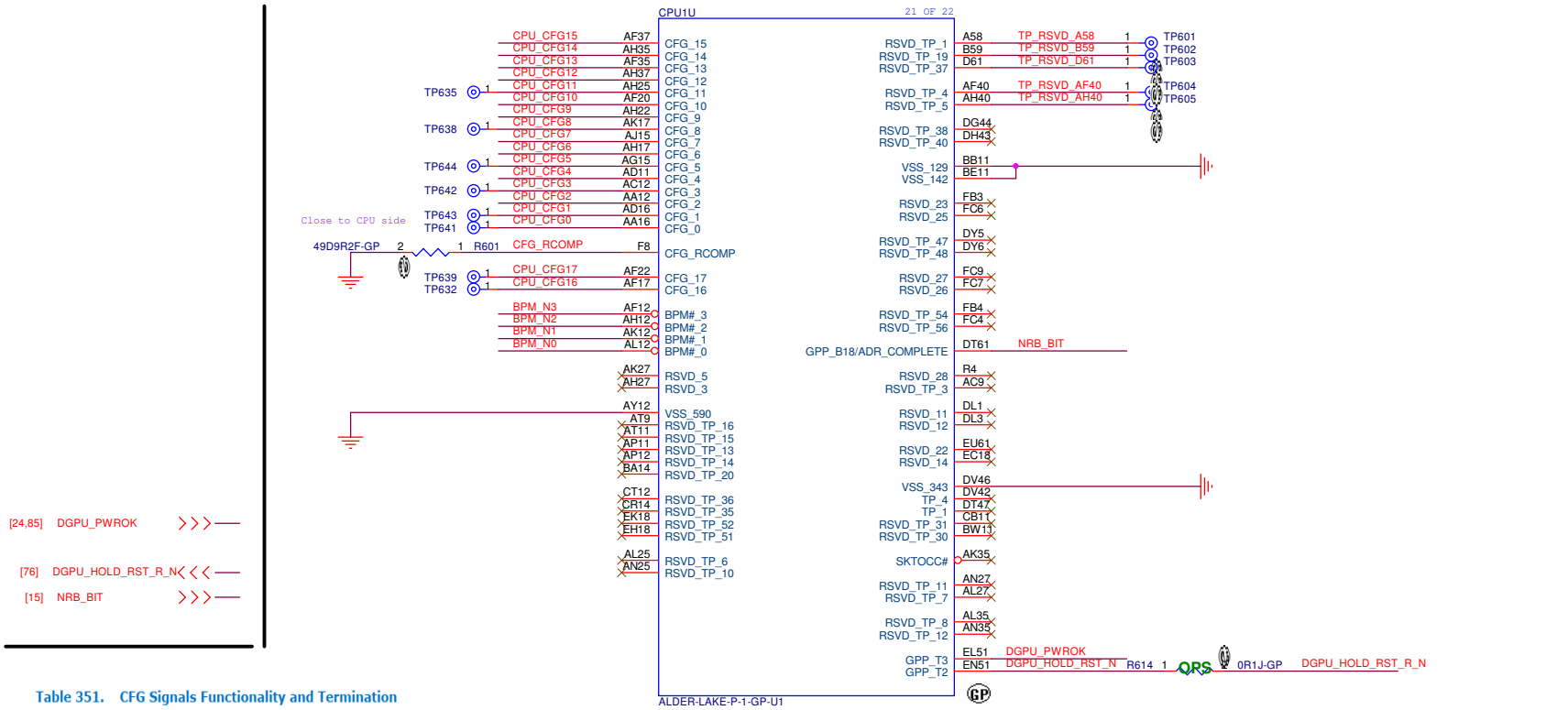

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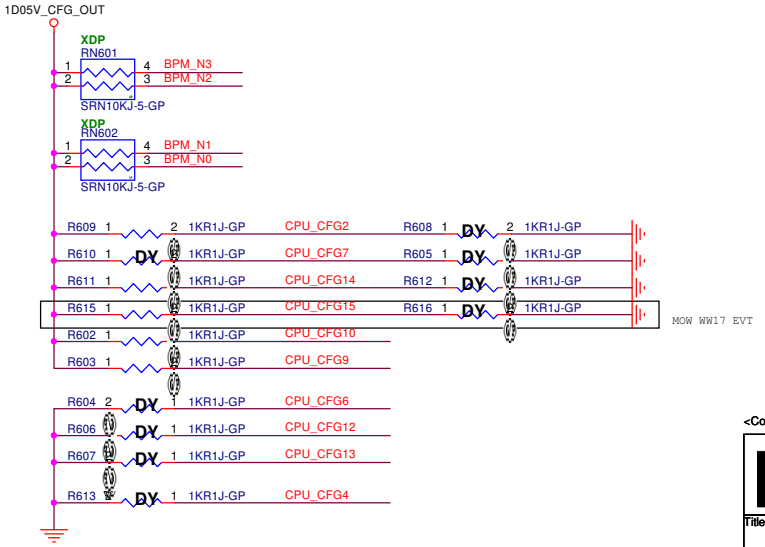
Table 351. CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull -Up to VCC1P05_PROC	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	None	
CFG[2]	PCI Express* Static X8 (PEG 10/11) Lane Numbering Reversal • 1:Normal Operation • 0: Lane Numbers reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[3]	RSVD	None	
CFG[4]	RSVD	None	
CFG[5]	RSVD	None	
CFG[6]	RSVD	NONE	
CFG[8:7]	RSVD	None	
CFG[10:9]	RSVD	Pull -Up to VCC_CFG_PU_OUT[1]	1K Ohms
CFG[13:11]	RSVD	None	
CFG[14]	PEG60 /PEG 62 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	
Note: 1.To ensure reliable boot across HVM.			



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Title: CPU (CFG/IST)

Size: A3 | Document Number: SouthPeak15 MLK | Rev: SB

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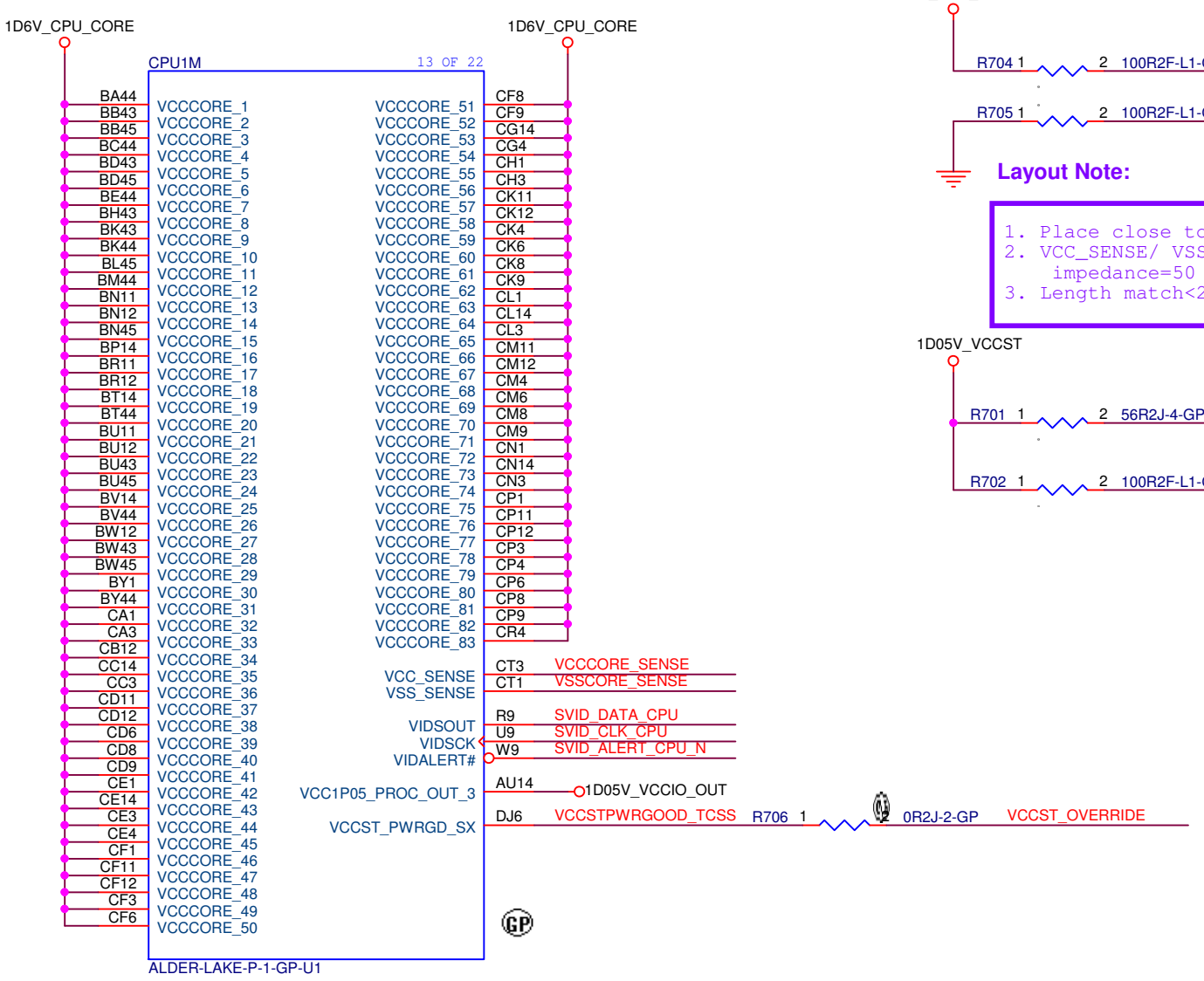
Main Func = CPU

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[17,40] VCCST_OVERRIDE
[46] SVID_ALERT_CPU_N
[39,46] SVID_CLK_CPU
[46] SVID_DATA_CPU



1D6V_CPU_CORE
R704 1 2 100R2F-L1-GP-U VCCCORE_SENSE
R705 1 2 100R2F-L1-GP-U VSSCORE_SENSE

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

1D05V_VCCST
R701 1 2 56R2J-4-GP SVID_ALERT_CPU_N
R702 1 2 100R2F-L1-GP-U SVID_DATA_CPU

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Title: CPU (VCORE/VID)

Size	Document Number	Rev
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Main Func = CPU

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[46] VCCGT_SENSE <<<—

[46] VSSGT_SENSE <<<—

CPU1O — 15 OF 22

(4.3A) 1D2V_S3

AD61	VDD2_1	VCCGT_1	CP44
AG61	VDD2_2	VCCGT_2	CR45
AN61	VDD2_3	VCCGT_3	CT44
AP41	VDD2_4	VCCGT_4	CU43
AP44	VDD2_5	VCCGT_5	CU45
AR43	VDD2_6	VCCGT_6	CV4
AR45	VDD2_7	VCCGT_7	CV44
AT44	VDD2_8	VCCGT_8	CW1
AU43	VDD2_9	VCCGT_9	CW11
AU45	VDD2_10	VCCGT_10	CW12
AV44	VDD2_11	VCCGT_11	CW3
AY61	VDD2_12	VCCGT_12	CW6
BH61	VDD2_13	VCCGT_13	CW8
BR61	VDD2_14	VCCGT_14	CW9
CA61	VDD2_15	VCCGT_15	CY14
CC44	VDD2_16	VCCGT_16	CY4
CD43	VDD2_17	VCCGT_17	CY44
CD61	VDD2_18	VCCGT_18	DA1
CE44	VDD2_19	VCCGT_19	DA3
CF43	VDD2_20	VCCGT_20	DA43
CF45	VDD2_21	VCCGT_21	DB45
CG44	VDD2_22	VCCGT_22	DC1
CH45	VDD2_23	VCCGT_23	DC11
CK61	VDD2_24	VCCGT_24	DC12
CN61	VDD2_25	VCCGT_25	DC3
CW61	VDD2_26	VCCGT_26	DC4
DF61	VDD2_27	VCCGT_27	DC44
J61	VDD2_28	VCCGT_28	DC6
R61	VDD2_29	VCCGT_29	DC8
V61	VDD2_30	VCCGT_30	DC9
		VCCGT_31	DD1
AR14	VCC1P05_PROC_OUT_1	VCCGT_32	DD14
AT12	VCC1P05_PROC_OUT_2	VCCGT_33	DD3
		VCCGT_34	DD43
CM44		VCCGT_35	DD45
EA14	RSVD_TP_33	VCCGT_36	DE11
	RSVD_TP_49	VCCGT_37	DE12
E61	VCC1P8_PROC_8	VCCGT_38	DE4
G61	VCC1P8_PROC_9	VCCGT_39	DE6
H59	VCC1P8_PROC_10	VCCGT_40	DE8
AH44	VCC1P8_PROC_1	VCCGT_41	DE9
AJ45	VCC1P8_PROC_2	VCCGT_42	DF1
AK44	VCC1P8_PROC_3	VCCGT_43	DF14
AL45	VCC1P8_PROC_4	VCCGT_44	DF3
AM41	VCC1P8_PROC_5	VCCGT_45	DG4
AM44	VCC1P8_PROC_6		
AN43	VCC1P8_PROC_7		
CV1	VCCGT_SENSE		
CV3	VSSGT_SENSE		

1D5V_VCCGT

1D05V_VCCIO_OUT

R803 1 — VCC1P8_PROC_1 — 0R2J-2-GP

R804 1 — VCC1P8_PROC_2 — 0R2J-2-GP

ALDER-LAKE-P-1-GP-U1

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1D05V_VCCIO_OUT

C834 SC1U10V2KX-1DLGP DY GP

1D5V_VCCGT

R801 1 — 2 — 100R2F-L1-GP-U — VCCGT_SENSE

R802 1 — 2 — 100R2F-L1-GP-U — VSSGT_SENSE

VDDQ

1D2V_S3

1u 0402 x 6

C840 SC1U10V2KX-1DLGP GP

C841 SC1U10V2KX-1DLGP GP

C842 SC1U10V2KX-1DLGP GP

C843 SC1U10V2KX-1DLGP GP

C844 SC1U10V2KX-1DLGP GP

C845 SC1U10V2KX-1DLGP GP

10u 0402 x 3

C820 SC10U6D3V2MX-2-GP GP

C821 SC10U6D3V2MX-2-GP GP

C822 SC10U6D3V2MX-2-GP GP

C830 SC10U6D3V2MX-2-GP DY GP

C831 SC10U6D3V2MX-2-GP DY GP

C832 SC10U6D3V2MX-2-GP DY GP

C833 SC10U6D3V2MX-2-GP DY GP

C836 SC10U6D3V2MX-2-GP DY GP

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

<Core Design>

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Title: CPU (VCCGT/VCCIO/VDDQ/VCCSA)

Size: A4 | Document Number: SouthPeak15 MLK | Rev: SB

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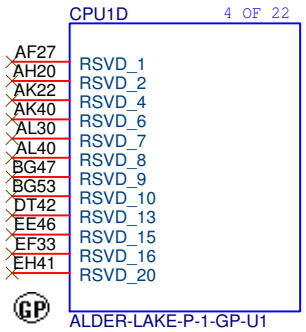

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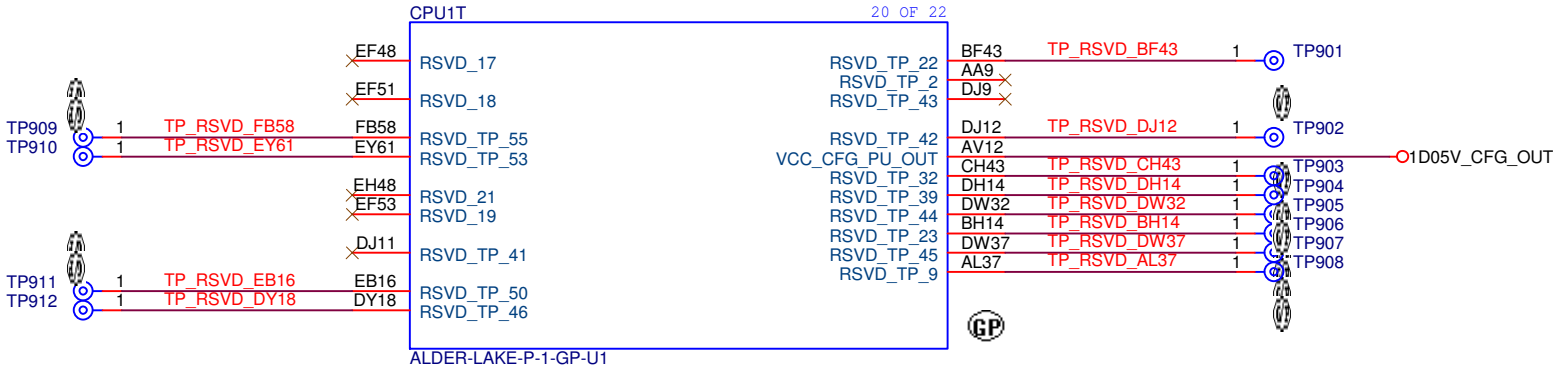

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (RSVD)***

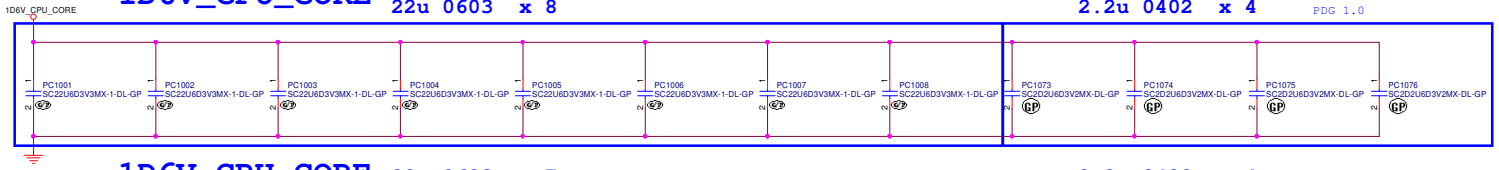
Size	Document Number	Rev
A4	***SouthPeak15 MLK***	***SB***

Date: Friday, May 21, 2021 Sheet 9 of 106

Main Func = CPU

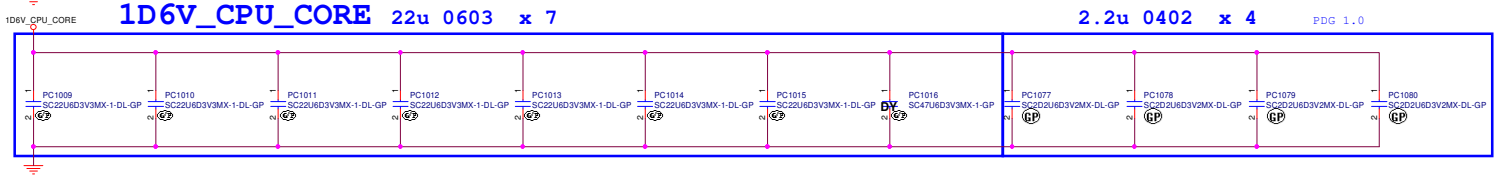
1D6V_CPU_CORE 22u 0603 x 8 2.2u 0402 x 4

PDG 1.0

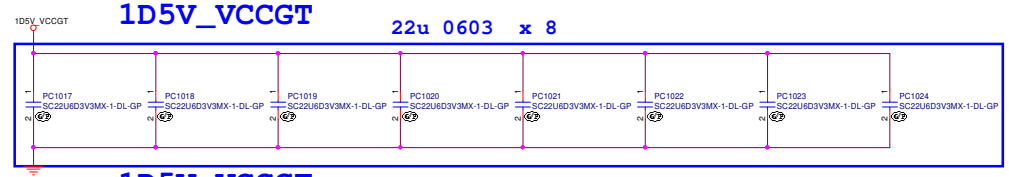


1D6V_CPU_CORE 22u 0603 x 7 2.2u 0402 x 4

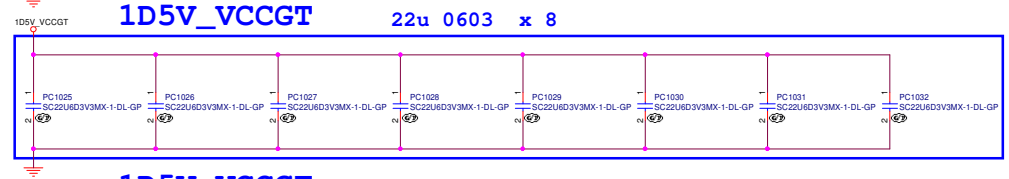
PDG 1.0



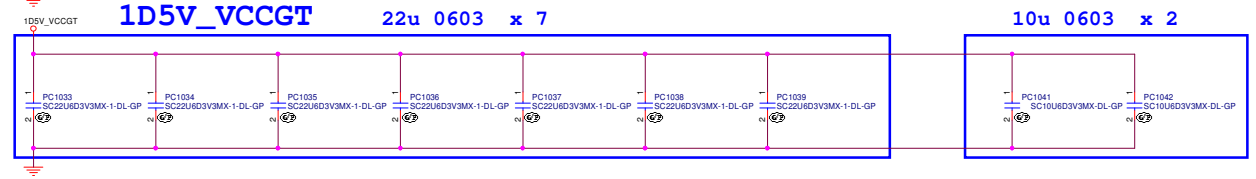
1D5V_VCCGT 22u 0603 x 8



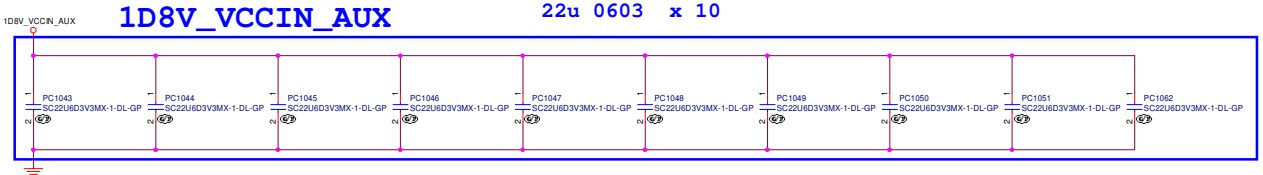
1D5V_VCCGT 22u 0603 x 8



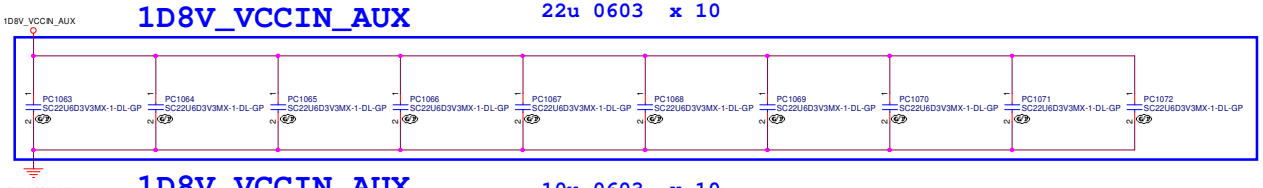
1D5V_VCCGT 22u 0603 x 7 10u 0603 x 2



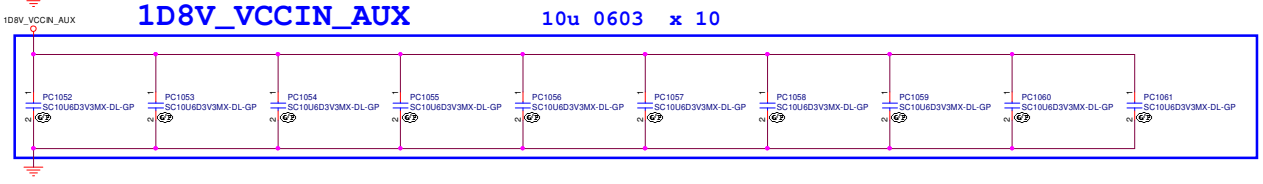
1D8V_VCCIN_AUX 22u 0603 x 10



1D8V_VCCIN_AUX 22u 0603 x 10



1D8V_VCCIN_AUX 10u 0603 x 10



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB

Date: Friday, May 21, 2021 | Sheet 10 of 106

Main Func = CPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (Power Cap2)***

Size	Document Number	Rev
A4	***SouthPeak15 MLK***	***SB***

Date: Friday, May 21, 2021 Sheet 11 of 106

Main Func = MEMORY

M_A_DQS_DN0 M_A_DQS_DN1 M_A_DQS_DN2 M_A_DQS_DN3 M_A_DQS_DN4 M_A_DQS_DN5 M_A_DQS_DN6 M_A_DQS_DN7 — M_A_DQS_DN[7:0] [5]

M_A_DQS_DP0 M_A_DQS_DP1 M_A_DQS_DP2 M_A_DQS_DP3 M_A_DQS_DP4 M_A_DQS_DP5 M_A_DQS_DP6 M_A_DQS_DP7 — M_A_DQS_DP[7:0] [5]

M_A_A0 [5]
M_A_A1 [5]
M_A_A2 [5]
M_A_A3 [5]
M_A_A4 [5]
M_A_A5 [5]
M_A_A6 [5]
M_A_A7 [5]
M_A_A8 [5]
M_A_A9 [5]
M_A_A10 [5]
M_A_A11 [5]
M_A_A12 [5]
M_A_A13 [5]
M_A_A14 [5]
M_A_A15 [5]
M_A_A16 [5]

M_A_DQ63 M_A_DQ62 M_A_DQ61 M_A_DQ60 M_A_DQ59 M_A_DQ58 M_A_DQ57 M_A_DQ56 M_A_DQ55 M_A_DQ54 M_A_DQ53 M_A_DQ52 M_A_DQ51 M_A_DQ50 M_A_DQ49 M_A_DQ48 M_A_DQ47 M_A_DQ46 M_A_DQ45 M_A_DQ44 M_A_DQ43 M_A_DQ42 M_A_DQ41 M_A_DQ40 M_A_DQ39 M_A_DQ38 M_A_DQ37 M_A_DQ36 M_A_DQ35 M_A_DQ34 M_A_DQ33 M_A_DQ32 M_A_DQ31 M_A_DQ30 M_A_DQ29 M_A_DQ28 M_A_DQ27 M_A_DQ26 M_A_DQ25 M_A_DQ24 M_A_DQ23 M_A_DQ22 M_A_DQ21 M_A_DQ20 M_A_DQ19 M_A_DQ18 M_A_DQ17 M_A_DQ16 M_A_DQ15 M_A_DQ14 M_A_DQ13 M_A_DQ12 M_A_DQ11 M_A_DQ10 M_A_DQ9 M_A_DQ8 M_A_DQ7 M_A_DQ6 M_A_DQ5 M_A_DQ4 M_A_DQ3 M_A_DQ2 M_A_DQ1 M_A_DQ0 — M_A_DQ[63:0] [5]

M_A_CLK_P0 [5]
M_A_CLK_N0 [5]
M_A_CLK_P1 [5]
M_A_CLK_N1 [5]

M_A_CKE0 [5]
M_A_CKE1 [5]

M_A_CS0_N [5]
M_A_CS1_N [5]

M_A_ODT0 [5]
M_A_ODT1 [5]

CPU_SMB_SDA_DDR [13,18,98]
CPU_SMB_SCL_DDR [13,18,98]

DDR4_DRAMRST_N [5,13]
M_A_ACT_N [5]

M_A_PARITY [5]

M_A_BA0 [5]
M_A_BA1 [5]
M_A_BG0 [5]
M_A_BG1 [5]

V_SM_VREF_CNTA [5]

DIMM1A 1 OF 4 — DDR4-260P-130-GP — 062.10011.M030

M_A_DQ[16:23]
M_A_DQ[24:31]
M_A_DQ[0:7]
M_A_DQ[8:15]
M_A_DQ[32:39]
M_A_DQ[40:47]
M_A_DQ[48:55]
M_A_DQ[56:63]

DIMM1B 2 OF 4 — DDR4-260P-130-GP — 062.10011.M030

DIMM1C 3 OF 4 — DDR4-260P-130-GP — 062.10011.M030

DIMM1D 4 OF 4 — DDR4-260P-130-GP — 062.10011.M030

1D2V_S3 R1215.1 DY 2 0240R2F-1-GP C1229 SCD1U16V2KX-1DL-GP

DDR4_DRAMRST_N ED1217 AZ5725-01FDR7G-GP 83.05725.0A0 2nd = 083.00511.00AF

3D3V_S0 R1204.1 DY 2 10KR2J-3-GP SA0_CHA_DIM0 R1205.2 1 0R2J-2-GP
3D3V_S0 R1208.1 DY 2 10KR2J-3-GP SA1_CHA_DIM0 R1210.2 1 0R2J-2-GP
3D3V_S0 R1211.1 DY 2 10KR2J-3-GP SA2_CHA_DIM0 R1212.2 1 0R2J-2-GP

1D2V_S3 RN1201 SRN1KJ-7-GP M_VREF_CA_DIMMA R1206 2R2F-GP V_SM_VREF_CNTA
C1222 SCD022U16V2KX-3DLGP +V_VREF_PATH1 R1209 24D9R2F-L-GP
C1230 C1240 C1241 SCD1U16V2KX-3DLGP DY

1D2V_S3 C1202 C1203 C1204 C1205 C1206 C1208 C1209 C1210 SC1U06D3X6MX-2DLGP
C1214 C1215 C1216 C1217 C1218 C1219 C1220 C1221 EC1202 EC1203 SCD1U16V2KX-1DLGP
C1232 C1233 C1234 C1235 C1236 C1237 C1238 C1239 SC22U06D3V6MX-1DLGP DY

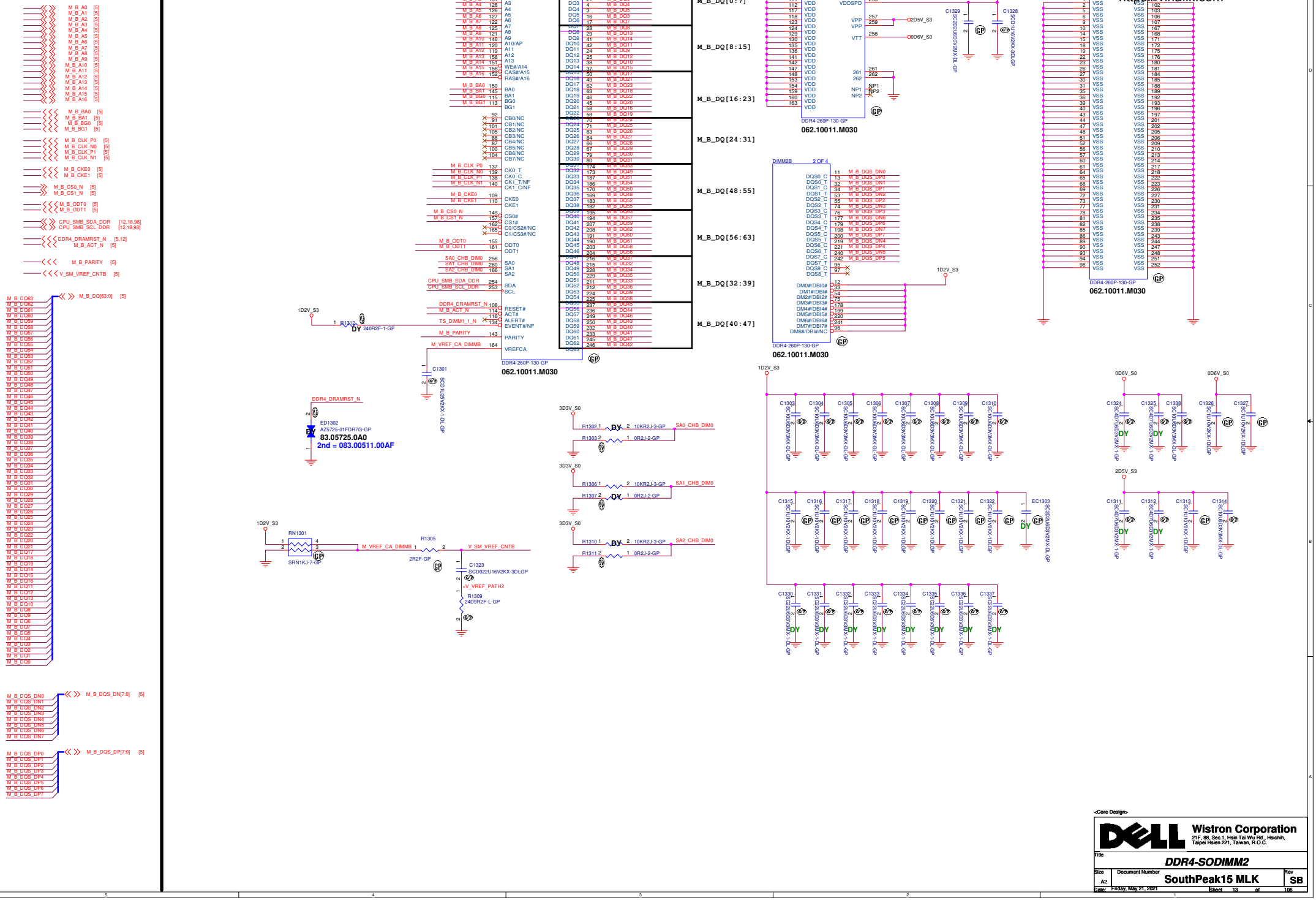
0D6V_S0 C1225 C1226 SC1U10V6KX-1DLGP
0D6V_S0 C1223 C1227 C1224 SC4D7U06D3X6MX-1GP DY
2D5V_S3 C1231 C1212 C1207 C1211 SC4D7U06D3V6MX-1GP DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4-SODIMM1
Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB
Date: Friday, May 21, 2021 | Sheet 12 of 106

Main Func = MEMORY



(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (RSVD) (DDR4-CHA1)

Size: A4 | Document Number: SouthPeak15 MLK | Rev: SB

Date: Friday, May 21, 2021 | Sheet 14 of 106

[18,24,25,68,91] SPI_SI_CPU
[21,61] CNV_RGI_DT
[19] HDA_SDO
[22] 3D3V_GPPR_S5
[3,99] DBG_PMODE
[21,61] CNV_BRI_DT
[6] NRB_BIT
[18] GPP_E6
[18] GPP_B23
[18] GPP_C5
[18] GPP_C2
[3] GPP_F7
[3] GPP_F10
[17] SPI_VCC_SEL
[3] GPP_H0
[3] GPP_H1
[3] GPP_H2
[4,71] TBT_0_LSX_RX
[4,71] TBT_1_LSX_RX
[17] GPD7
[18,24,25,68] SPI_HOLD_CPU
[18,24,25,68,99] SPI_WP_CPU

GPIO	GPP_B14/SPKR TOP SWAP OVERRIDE	SPI0_MOSI	GPP_E6 JTAG ODT Disable	GPP_F0 XTAL Freq Selection	SPI_IO_2 SPI_WP_CPU	GPP_R2 / HDA_SDO Flash Security Override	GPP_F2 / CNV_RGI_DT M.2 CNVi Mode Select
Schematic	=default= =20K PD=	=External PH required.= Close to BIOS1/SPI1	=default= =20K PD=	=default= =20K PD=	=External PH required.= PH at ROM side Close to BIOS1/SKT1	* PH as VCCPGPPR =default= =20K PD=	=NO INTERNAL=
High	Enable	Reserved	JTAG ODT is enabled	24 MHz	Reserved	Enable Override	INTEGRATED CNVI DISABLE
Low	Disable	Reserved	JTAG ODT is disabled	38.4 MHz	Reserved	Disable Override	INTEGRATED CNVI ENABLE

GPIO	GPP_E19 TBT_LSX0_VCC config	GPP_E21 TBT_LSX1_VCC config	GPP_D10 DDP3 I2C / TBT_LSX2 BBSB_LS2 pins VCC configuration	GPP_D12 DDP4 I2C / TBT_LSX3 BSSB_LS3 pins VCC configuration	SPI_IO_3 SPI_HOLD_CPU	DBG_PMODE	GPP_B18 No Reboot
Schematic	=20K PD=	=20K PD=	=20K PD=	=20K PD=	=External PH required.= PH at ROM side Close to BIOS1/SKT1	=20K PU=	=default= =20K PD=
High	3.3V	3.3V	3.3V	3.3V	Reserved	Reserved	Enable "No Reboot" mode
Low	1.8V	1.8V	1.8V	1.8V	Reserved	Reserved	Disable

GPIO	GPD_7	GPP_C2/SMBALERT# TLS Confidentiality	GPP_B23/PCHHOT# CPUNSSC CLOCK FREQ	SPIVCCIOSEL	GPP_F7	GPP_F10
Schematic	=20K PD=	=default= =20K PD=	=default= =20K PD=	SPI Operation Voltage Select	=default= =20K PD=	=default= =20K PD=
High	Reserved	Enable	19.2MHz	1.8V	Reserved	Reserved
Low	Reserved	Disable	38.4MHz	3.3V	Reserved	Reserved

GPIO	GPP_C5 Boot Strap 0	GPP_H0/GPP_H0_BOOT_STRAP1 Boot Strap 1	GPP_H1/GPP_H1_BOOT_STRAP2 Boot Strap 2	GPP_H2/GPP_H2_BOOT_STRAP3 Boot Strap 3
Schematic	=20K PD=	=20K PD=	=20K PD=	=20K PD=
High	eSPI is disabled	eSPI is disabled	eSPI is disabled	eSPI is disabled
Low	eSPI is enabled	eSPI is enabled	eSPI is enabled	eSPI is enabled

This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).

4-bit boot strap configuration encodings:

0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is enabled

0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled

0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI

1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).

1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.

Others: Reserved

Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB

Date: Friday, May 21, 2021 | Sheet 15 of 106

Main Func = PCH

SSD1

[63] SSD1_PCIE_RX_P3 — [63] SSD1_PCIE_TX_P3
[63] SSD1_PCIE_RX_N3 — [63] SSD1_PCIE_TX_N3
[63] SSD1_PCIE_RX_P2 — [63] SSD1_PCIE_TX_P2
[63] SSD1_PCIE_RX_N2 — [63] SSD1_PCIE_TX_N2
[63] SSD1_PCIE_RX_P1 — [63] SSD1_PCIE_TX_P1
[63] SSD1_PCIE_RX_N1 — [63] SSD1_PCIE_TX_N1
[63] SSD1_PCIE_RX_P0 — [63] SSD1_PCIE_TX_P0
[63] SSD1_PCIE_RX_N0 — [63] SSD1_PCIE_TX_N0

GPU_PCIE

[76] GFX_PCIE_RX_P3 — [76] GFX_PCIE_TX_P3
[76] GFX_PCIE_RX_N3 — [76] GFX_PCIE_TX_N3
[76] GFX_PCIE_RX_P2 — [76] GFX_PCIE_TX_P2
[76] GFX_PCIE_RX_N2 — [76] GFX_PCIE_TX_N2
[76] GFX_PCIE_RX_P1 — [76] GFX_PCIE_TX_P1
[76] GFX_PCIE_RX_N1 — [76] GFX_PCIE_TX_N1
[76] GFX_PCIE_RX_P0 — [76] GFX_PCIE_TX_P0
[76] GFX_PCIE_RX_N0 — [76] GFX_PCIE_TX_N0

SSD2

[63] SSD2_PCIE_RX_P4 — [63] SSD2_PCIE_TX_P4
[63] SSD2_PCIE_RX_N4 — [63] SSD2_PCIE_TX_N4
[63] SSD2_PCIE_RX_P3 — [63] SSD2_PCIE_TX_P3
[63] SSD2_PCIE_RX_N3 — [63] SSD2_PCIE_TX_N3
[63] SSD2_PCIE_RX_P2 — [63] SSD2_PCIE_TX_P2
[63] SSD2_PCIE_RX_N2 — [63] SSD2_PCIE_TX_N2
[63] SSD2_PCIE_RX_P1 — [63] SSD2_PCIE_TX_P1
[63] SSD2_PCIE_RX_N1 — [63] SSD2_PCIE_TX_N1

LAN

[97] LAN_PCIE_RX_P — [97] LAN_PCIE_TX_P
[97] LAN_PCIE_RX_N — [97] LAN_PCIE_TX_N

CARD

[33] CARD_PCIE_RX_P — [33] CARD_PCIE_TX_P
[33] CARD_PCIE_RX_N — [33] CARD_PCIE_TX_N

WLAN

[61] WLAN_PCIE_RX_P — [61] WLAN_PCIE_TX_P
[61] WLAN_PCIE_RX_N — [61] WLAN_PCIE_TX_N

WWAN

[62] WWAN_PCIE_RX_P — [62] WWAN_PCIE_TX_P
[62] WWAN_PCIE_RX_N — [62] WWAN_PCIE_TX_N

[62] WWAN_USB31_RX_P — [62] WWAN_USB31_TX_P
[62] WWAN_USB31_RX_N — [62] WWAN_USB31_TX_N

USB3 USB4

[35] USB2_USB31_RX_P — [35] USB2_USB31_TX_P
[35] USB2_USB31_RX_N — [35] USB2_USB31_TX_N

[35] USB1_USB31_RX_P — [35] USB1_USB31_TX_P
[35] USB1_USB31_RX_N — [35] USB1_USB31_TX_N

BT

[61] BT_USB20_P
[61] BT_USB20_N

FP

[92] FP_USB20_P
[92] FP_USB20_N

USH

[66] USH_USB20_P
[66] USH_USB20_N

WWAN

[62] WWAN_USB20_P
[62] WWAN_USB20_N

CAMERA

[56] CCD_USB20_P
[56] CCD_USB20_N

USB4

[35] USB4_USB20_P
[35] USB4_USB20_N

USB3 Charger

[36] Charger_USB20_P
[36] Charger_USB20_N

USB2

[73] USB2_USB20_P
[73] USB2_USB20_N

USB1

[73] USB1_USB20_P
[73] USB1_USB20_N

[36] USB_OC0_N

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

https://vinafix.com

M.2 SSD1

CPU1H — 8 OF 22

SSD1_PCIE_TX_P3 A20 — PCIEX4_A_TX_P_3
SSD1_PCIE_TX_N3 C20 — PCIEX4_A_TX_N_3
SSD1_PCIE_RX_P3 M22 — PCIEX4_A_RX_P_3
SSD1_PCIE_RX_N3 M24 — PCIEX4_A_RX_N_3
SSD1_PCIE_TX_P2 G20 — PCIEX4_A_TX_P_2
SSD1_PCIE_TX_N2 F20 — PCIEX4_A_TX_N_2
SSD1_PCIE_RX_P2 V22 — PCIEX4_A_RX_P_2
SSD1_PCIE_RX_N2 U22 — PCIEX4_A_RX_N_2
SSD1_PCIE_TX_P1 A17 — PCIEX4_A_TX_P_1
SSD1_PCIE_TX_N1 C17 — PCIEX4_A_TX_N_1
SSD1_PCIE_RX_P1 AC22 — PCIEX4_A_RX_P_1
SSD1_PCIE_RX_N1 AA22 — PCIEX4_A_RX_N_1
SSD1_PCIE_TX_P0 G17 — PCIEX4_A_TX_P_0
SSD1_PCIE_TX_N0 F17 — PCIEX4_A_TX_N_0
SSD1_PCIE_RX_P0 M18 — PCIEX4_A_RX_P_0
SSD1_PCIE_RX_N0 M19 — PCIEX4_A_RX_N_0

PCIE4_RCOMP_N F6 — PCIEX4_RCOMP_N
PCIE4_A_RCOMP_P A6 — PCIEX4_A_RCOMP_P_1
C6 — PCIEX4_A_RCOMP_P_2
PCIE4_B_RCOMP_P A5 — PCIEX4_B_RCOMP_P_1
D6 — PCIEX4_B_RCOMP_P_2

R1601 1 — 2K2R2B-1-GP — PCIE4_A_RCOMP_P
R1608 1 — 2K2R2B-1-GP — PCIE4_B_RCOMP_P

Put Caps to close GPU1

GPU1

GFX_PCIE_TX_P3 C1602 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_P3 A14 — PCIEX4_B_TXP_3
GFX_PCIE_TX_N3 C1603 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_N3 C14 — PCIEX4_B_TXN_3
GFX_PCIE_RX_P3 C1612 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_P3 V17 — PCIEX4_B_RXP_3
GFX_PCIE_RX_N3 C1613 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_N3 U17 — PCIEX4_B_RXN_3
GFX_PCIE_TX_P2 C1607 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_P2 G14 — PCIEX4_B_TXP_2
GFX_PCIE_TX_N2 C1606 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_N2 F14 — PCIEX4_B_TXN_2
GFX_PCIE_RX_P2 C1616 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_P2 AC17 — PCIEX4_B_RXP_2
GFX_PCIE_RX_N2 C1617 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_N2 AA17 — PCIEX4_B_RXN_2
GFX_PCIE_TX_P1 C1611 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_P1 A11 — PCIEX4_B_TXP_1
GFX_PCIE_TX_N1 C1610 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_N1 C11 — PCIEX4_B_TXN_1
GFX_PCIE_RX_P1 C1619 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_P1 M13 — PCIEX4_B_RXP_1
GFX_PCIE_RX_N1 C1618 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_N1 M14 — PCIEX4_B_RXN_1
GFX_PCIE_TX_P0 C1615 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_P0 G11 — PCIEX4_B_TXP_0
GFX_PCIE_TX_N0 C1614 — SCD22U10V1KX-1-GP — GFX_PCIE_TX_C_N0 F11 — PCIEX4_B_TXN_0
GFX_PCIE_RX_P0 C1621 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_P0 V12 — PCIEX4_B_RXP_0
GFX_PCIE_RX_N0 C1620 — SCD22U10V1KX-1-GP — GFX_PCIE_RX_C_N0 U12 — PCIEX4_B_RXN_0

PCIEX8_TX_P_7 C33
PCIEX8_TX_N_7 D33
PCIEX8_TX_P_6 J33
PCIEX8_TX_N_6 G33
PCIEX8_TX_P_5 C30
PCIEX8_TX_N_5 D30
PCIEX8_TX_P_4 J30
PCIEX8_TX_N_4 G30
PCIEX8_TX_P_3 C26
PCIEX8_TX_N_3 D26
PCIEX8_TX_P_2 J26
PCIEX8_TX_N_2 G26
PCIEX8_TX_P_1 C23
PCIEX8_TX_N_1 D23
PCIEX8_TX_P_0 J23
PCIEX8_TX_N_0 G23
PCIEX8_RX_P_7 M39
PCIEX8_RX_N_7 M37
PCIEX8_RX_P_6 U37
PCIEX8_RX_N_6 V37
PCIEX8_RX_P_5 AA37
PCIEX8_RX_N_5 AC37
PCIEX8_RX_P_4 U32
PCIEX8_RX_N_4 V32
PCIEX8_RX_P_3 AA32
PCIEX8_RX_N_3 AC32
PCIEX8_RX_P_2 M29
PCIEX8_RX_N_2 M27
PCIEX8_RX_P_1 U27
PCIEX8_RX_N_1 V27
PCIEX8_RX_P_0 AA27
PCIEX8_RX_N_0 AC27

PCIEX8_RCOMP_P_1 A8
PCIEX8_RCOMP_P_2 C8 — PCIE8_RCOMP_P — R1606 2 — 150R2F-1-GP — 1 — PCIE8_RCOMP_N — D8
PCIEX8_RCOMP_N

ALDER-LAKE-P-1-GP-U1
ZZ.PAD00.1C1

WLAN
CARD
LAN
M.2 SSD2
USB3 Type A port1
USB4 Type A port2
WINDOS WWAN
UBUNTU WWAN

CPU1I — 9 OF 22

WLAN_PCIE_TX_P DY10 — PCIE12_TXP/SATA1_TXP
WLAN_PCIE_TX_N DY11 — PCIE12_TXN/SATA1_TXN
WLAN_PCIE_RX_P EA4 — PCIE12_RXP/SATA1_RXP
WLAN_PCIE_RX_N EA6 — PCIE12_RXN/SATA1_RXN
EB10 — PCIE11_TXP/SATA0_TXP
EB11 — PCIE11_TXN/SATA0_TXN
EC5 — PCIE11_RXP/SATA0_RXP
EC6 — PCIE11_RXN/SATA0_RXN
CARD_PCIE_TX_P ED10 — PCIE10_TXP/UFS11_TXP
CARD_PCIE_TX_N ED11 — PCIE10_TXN/UFS11_TXN
CARD_PCIE_RX_P EC1 — PCIE10_RXP/UFS11_RXP
CARD_PCIE_RX_N EC3 — PCIE10_RXN/UFS11_RXN
LAN_PCIE_TX_P EF10 — PCIE9_TXP/UFS10_TXP
LAN_PCIE_TX_N EF11 — PCIE9_TXN/UFS10_TXN
LAN_PCIE_RX_P EF5 — PCIE9_RXP/UFS10_RXP
LAN_PCIE_RX_N EF6 — PCIE9_RXN/UFS10_RXN
SSD2_PCIE_TX_P4 EH10 — PCIE8_TXP
SSD2_PCIE_TX_N4 EH11 — PCIE8_TXN
SSD2_PCIE_RX_P4 EF1 — PCIE8_RXP
SSD2_PCIE_RX_N4 EF3 — PCIE8_RXN
SSD2_PCIE_TX_P3 EL10 — PCIE7_TXP
SSD2_PCIE_TX_N3 EL11 — PCIE7_TXN
SSD2_PCIE_RX_P3 EG4 — PCIE7_RXP
SSD2_PCIE_RX_N3 EG6 — PCIE7_RXN
SSD2_PCIE_TX_P2 EN10 — PCIE6_TXP
SSD2_PCIE_TX_N2 EN11 — PCIE6_TXN
SSD2_PCIE_RX_P2 EJ5 — PCIE6_RXP
SSD2_PCIE_RX_N2 EJ6 — PCIE6_RXN
SSD2_PCIE_TX_P1 ER10 — PCIE5_TXP
SSD2_PCIE_TX_N1 ER11 — PCIE5_TXN
SSD2_PCIE_RX_P1 EJ1 — PCIE5_RXP
SSD2_PCIE_RX_N1 EJ3 — PCIE5_RXN
USB1_USB31_TX_P FB10 — PCIE4_TXP/USB32_4_TXP
USB1_USB31_TX_N FA9 — PCIE4_TXN/USB32_4_TXN
USB1_USB31_RX_P EV16 — PCIE4_RXP/USB32_4_RXP
USB1_USB31_RX_N EV16 — PCIE4_RXN/USB32_4_RXN
USB2_USB31_TX_P EW11 — PCIE3_TXP/USB32_3_TXP
USB2_USB31_TX_N EY11 — PCIE3_TXN/USB32_3_TXN
USB2_USB31_RX_P EW17 — PCIE3_RXP/USB32_3_RXP
USB2_USB31_RX_N EY17 — PCIE3_RXN/USB32_3_RXN
WWAN_PCIE_TX_P FA12 — PCIE2_TXP/USB32_2_TXP
WWAN_PCIE_TX_N FC12 — PCIE2_TXN/USB32_2_TXN
WWAN_PCIE_RX_P FA18 — PCIE2_RXP/USB32_2_RXP
WWAN_PCIE_RX_N FC18 — PCIE2_RXN/USB32_2_RXN
WWAN_USB31_TX_P EV12 — PCIE1_TXP/USB32_1_TXP
WWAN_USB31_TX_N EY12 — PCIE1_TXN/USB32_1_TXN
WWAN_USB31_RX_P EV19 — PCIE1_RXP/USB32_1_RXP
WWAN_USB31_RX_N EY19 — PCIE1_RXN/USB32_1_RXN

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USB2P_10 EM5 — BT_USB20_P — BT
USB2N_10 EM6 — BT_USB20_N
USB2P_9 EL18 — FP_USB20_P — FP
USB2N_9 EN18 — FP_USB20_N
USB2P_8 EN1 — USH_USB20_P — USH
USB2N_8 EN3 — USH_USB20_N
USB2P_7 ER16 — WWAN_USB20_P — WWAN
USB2N_7 ET16 — WWAN_USB20_N
USB2P_6 EP4 — CCD_USB20_P — CAMERA
USB2N_6 EP6 — CCD_USB20_N
USB2P_5 FA15
USB2N_5 FC15
USB2P_4 ER5 — USB4_USB20_P — USB4 Type A port 2
USB2N_4 ER6 — USB4_USB20_N
USB2P_3 ER18 — Charger_USB20_P — USB3 Type A port 1
USB2N_3 ET18 — Charger_USB20_N
USB2P_2 EH16 — USB2_USB20_P — USB2 Type C port 2
USB2N_2 EK16 — USB2_USB20_N
USB2P_1 EL16 — USB1_USB20_P — USB1 Type C port 1
USB2N_1 EN16 — USB1_USB20_N

GPP_E9/USB_OC0#/ISH_GP4 FC25 — USB_OC0_N
GPP_A16/USB_OC3#/ISH_GP5 DY51 — USB_OC3_N
GPP_E5/DEVSLP1 FA25 — SD_SUPPORT
GPP_E4/DEVSLP0 FC22 — P_SENSOR_PWR_SAVE_RF_1P8_N

MPHY_RCOMPP DY1 — MPHY_RCOMP_P — R1605 1 — 2 — 100R2F-L1-GP-U
MPHY_RCOMPN DY3 — MPHY_RCOMP_N

USB_VBUSSENSE EF18 — USB2_VBUSSENSE — R1602 1 — 2 — 10KR2F-2-GP
USB_ID EF16 — USB2_ID — R1603 1 — 2 — 10KR2F-2-GP
USB2_COMP FB20 — USB2_COMP — R1604 1 — 2 — 113R2F-GP

UFS_RESET# DL8

3D3V_S5_PCH
USB_OC0_N — 1 — RN1601 — 4 — 2 — 3 — SRN10KJ-5-GP

1D8V_S5
P_SENSOR_PWR_SAVE_RF_1P8_N — 10KR2F-2-GP — 1R1609
EM3A doesn't support PWR save function
Just reserve this pin

3D3V_S5_PCH
R1611 100KR1F-GP — DY
SD_SUPPORT
R1612 100KR1F-GP — DY

SD_SUPPORT	
HIGH	SD support
LOW	SD no support

Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)
Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB
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[24,39,40] PM_SLP_SUS_N
[39,68] SIO_SLP_S5_N
[39,51,68] SIO_SLP_S4_N
[22,24,39,40,68] SIO_SLP_S3_N
[68] SIO_SLP_A_N
[68,91] SIO_SLP_S0_N
[40] PM_SLP_LAN_N
[24,39,64,99] RSMRST_KBC_N
[68] SYS_RESET_N
62,63,76,91,97,99] PCH_PLTRST_RIGHT_N

[24,39] PCH_DPWROK
[24,39] SYS_PWROK_R
[40,46] PCH_PWROK
[89] RTC_INTRUDER_N
[24,39] SIO_PWRBTN_N
[24,39] AC_PRESENT
[72] TBT_I2C_INT_N
[39,91] CPU_C10_GATE_N
[66] SC_CAGE_DET_N
[24] PCH_PCIE_WAKE_N
[97] LAN_WAKE_N
[97] PM_LANPHY_EN

[24,39,40] ALL_SYS_PWRGD

[7,40] VCCST_OVERRIDE
[15] SPI_VCC_SEL
[89] RTC_INTRUDER_R_N
[44] AC_DIS_ACP
[15] GPD7
[39] CPU_PWRGD
[39] DSW_PWROK_R
[39] VCCST_PWRGD
[39] PCH_PLTRST_N
[39] PCH_PWROK_R

CPU1L
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ALDER-LAKE-P-1-GP-U1
ZZ.PAD00.1C1

PM_SLP_SUS_N EN53 SLP_SUS#
SIO_SLP_S5_N EG60 GPD10/SLP_S5#
SIO_SLP_S4_N EP56 GPD5/SLP_S4#
SIO_SLP_S3_N EM59 GPD4/SLP_S3#
SIO_SLP_A_N EM57 GPD6/SLP_A#
SIO_SLP_WLAN_N EJ57 GPD9/SLP_WLAN#
SIO_SLP_S0_N DW59 GPP_B12/SLP_S0#
PM_SLP_LAN_N EK53 SLP_LAN#
RSMRST_KBC_N 1 R1720 0R1J-GP PM_RSMRST_N EH53 RSMRST#
SYS_RESET_N EK26 SYS_RESET#
PCH_PLTRST_N DW57 GPP_B13/PLTRST#
PCH_DPWROK 1 R1725 0R2J-2-GP 2 DSW_PWROK_R EE48 DSW_PWROK
SYS_PWROK_R EK23 SYS_PWROK
PCH_PWROK 1 R1726 0R2J-2-GP 2 PCH_PWROK_R EH51 PCH_PWROK
RTC_INTRUDER_N DY44 INTRUDER#
SPI_VCC_SEL EL53 SPIVCCIOSEL
CPU_PWRGD BG11 PROCPWRGD

EM61 SIO_PWRBTN_N GPD3/PWRBTN#
EM56 PCH_BATLOW_N GPD0/BATLOW#
EJ59 AC_PRESENT GPD1/ACPRESENT
EA56 TBT_I2C_INT_N GPP_B11/PMCALERT#
ER46 CPU_C10_GATE_N GPP_H18/PROC_C10_GATE#
ET48 SC_CAGE_DET_N GPP_H3/SX_EXIT_HOLDOFF#
ET51 PCH_PCIE_WAKE_N WAKE#
EP58 LAN_WAKE_N GPD2/LAN_WAKE#
EJ56 PM_LANPHY_EN GPD11/LANPHYPC
EK60 GPD7
FA22 SLP_DRAM_TP_N GPP_E8/SLP_DRAM# 1 TP1702
DJ8 VCCST_PWRGD VCCST_OVERRIDE
DK4 VCCST_OVERRIDE
EH28 EXT_PWR_GATE_1P8_N GPP_F20/EXT_PWR_GATE# 1 TP1703
EH31 EXT_PWR_GATE2_1P8 GPP_F21/EXT_PWR_GATE2# 1 TP1704

3D3V_S5_PCH
Close CPU side
R1705 1 10KR1F-GP LAN_WAKE_N
R1706 1 2 100KR2J-1-GP AC_PRESENT
R1707 1 100KR2F-L1-GP PCH_BATLOW_N
R1712 1 10KR1F-GP PCH_PCIE_WAKE_N
R1714 1 10KR1F-GP SIO_PWRBTN_N
R1716 1 DY 10KR1F-GP SIO_SLP_S0_N
R1737 1 2 10KR2F-2-GP SYS_RESET_N
MOW WW16 EVT

3D3V_RTC_PCH
R1704 100KR1F-GP
RTC_INTRUDER_R_N

From EC Control
DSW_PWROK_R
R1736 1MR2F-GP
C1704 DY SCD01U25V2KX-L1-GP
Delay 3D3V_S5 over 10ms.

CPU_C10_GATE_N 100KR2J-1-GP R1718
SYS_PWROK_R 100KR2J-1-GP R1717
SIO_SLP_S4_N 100KR2J-1-GP R1731
SIO_SLP_S3_N 100KR2J-1-GP R1732
SIO_SLP_A_N 100KR2J-1-GP R1733
SIO_SLP_WLAN_N 100KR2J-1-GP R1734
PM_SLP_LAN_N 100KR2J-1-GP R1735
SIO_SLP_S0_N 100KR2J-1-GP R1738
SIO_SLP_S5_N 100KR2J-1-GP R1739

RTC_INTRUDER_N
C1702 SCD1U16V1KX-5-GP
R1713 10MR1J-GP

3D3V_S5_PCH
PCH_PLTRST_N
R1723 100KR2F-L1-GP
U1701 TC7SZ08FU-LJ-CT-GP
C1703 SCD1U16V2KX-3DLGP
PCH_PLTRST_Q_N
R1721 0R1J-GP
PCH_PLTRST_RIGHT_N
R1724 DY 100KR1F-GP
073.7SZ08.000G
2nd = 73.01G08.L04
3rd = 73.01G08.IHG

3D3V_AUX_S5
R1708 10KR2F-2-GP
PM_RSMRST
Q1701 2N7002KDW-1-GP
D1702 RB520S30-GP
AC_DIS_ACP
AC_PRESENT
RSMRST_KBC_N
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F
75.27002.F7C

3D3V_S5_PCH
1D05V_VCCST
U1702 74LVC1G07GW-GP
ALL_SYS_PWRGD
C1701 SCD1U16V2KX-3DLGP
R1702 1KR2F-3-GP
VCCST_PWRGD_R
R1701 62R2F-GP
VCCST_PWRGD
73.01G07.0HG
2nd = 073.7SZ07.000G
3rd = 073.01G07.0C0G

RSMRST_KBC_N
PM_RSMRST_N
PCH_PWROK
SYS_RESET_N
PCH_PLTRST_N
EC1701 DY SCD1KP50V2KX-1DLGP
R1715 100KR2F-L1-GP
R1727 DY 100KR1F-GP
EC1702 DY SCD1KP25V1KX-GP
EC1703 DY SCD1KP50V2KX-1DLGP
ED1702 AZ5725-01FDR7G-GP
83.05725.0A0
2nd = 083.00511.00AF
DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: A3
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SSD
[63] SSD2_CLK_CPU_P
[63] SSD2_CLK_CPU_N
[63] SSD1_CLK_CPU_P
[63] SSD1_CLK_CPU_N

WLAN
[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] CL_CLK
[61] CL_RST_N
[61] CL_DATA

GFX
[76] GFX_CLK_CPU_P
[76] GFX_CLK_CPU_N

CARD
[33,39] CARD_CLK_CPU_P
[33] CARD_CLK_CPU_N

WWAN
[62] WWAN_CLK_CPU_P
[62] WWAN_CLK_CPU_N
[62] WWAN_BB_RST_1P8_N
[62] WWAN_GPIO_WAKE_N
[62] WWAN_GPIO_PERST_N

LAN
[97] LAN_CLK_CPU_P
[97] LAN_CLK_CPU_N

[63] CLKREQ_PCIE0_N
[61] CLKREQ_PCIE1_N
[62] CLKREQ_PCIE2_N
[76] CLKREQ_PCIE3_N
[63] CLKREQ_PCIE4_N
[33] CLKREQ_PCIE5_N
[97] CLKREQ_PCIE6_N
[39,61] SUSCLK

SPI
[15,24,25,68,91] SPI_SI_CPU
[24,25,68] SPI_CS_CPU_N0
[15,24,25,68] SPI_HOLD_CPU
[15,24,25,68,99] SPI_WP_CPU
[24,25,68,91] SPI_SO_CPU
[24,25,68,91] SPI_CLK_CPU
[24,25,68] SPI_CS_CPU_N1
[91] SPI_CS_CPU_N2

ESPI
[24,68,98] ESPI_IO0
[24,68,98] ESPI_IO1
[24,68,98] ESPI_IO2
[24,68,98] ESPI_IO3
[24,68,98] ESPI_CS_N
[24,39,68] ESPI_RESET_N
[24,68,98] ESPI_CLK

[12,13,98] CPU_SMB_SCL_DDR
[12,13,98] CPU_SMB_SDA_DDR
[15] GPP_C2

[33] MEDIACARD_IRQ_N
[55] TOUCH_SCREEN_INT_N
[25] RTC_DET_N
[15] GPP_E6
[15] GPP_C5
[56] P_SENSOR_DET_1P8_N

[15] GPP_B23
[39,68] RTC_RST_N
[24] RTCRST_ON
[39] SRTC_RST_N
[61] CNVI_EN_N
[56] SECURE_BIO
[98] ESPI_CLK_1P8
[98] ESPI_IO0_1P8
[98] ESPI_IO1_1P8
[98] ESPI_IO2_1P8
[98] ESPI_IO3_1P8
[98] MEM_SMBCLK
[98] MEM_SMBDATA
[71,97,98] SML0_SMBCLK
[71,97,98] SML0_SMBDATA
[72,98] SML1_SMBCLK
[72,98] SML1_SMBDATA

[55] TOUCH_SCREEN_DET_N
[55] LCD_CBL_DET_N
[57] HDMI_PD_R_N
[56] IR_CAM_DET_N
[55] TOUCH_SCREEN_RST_N
[40] PCH_TOUCH_SCREEN_EN
[55] TOUCH_SCREEN_PD_N
[98] ESPI_CS_1P8_N
[56] CAM_MIC_CBL_DET_N

CPU1E — 5 OF 22 — ALDER-LAKE-P-1-GP-U1
ZZ.PAD00.1C1

CPU1K — 11 OF 22 — ALDER-LAKE-P-1-GP-U1
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TBT_DET# Dectect	
HIGH	NON TBT
LOW	TBT

CARD_IDENTIFY	
HIGH	GENESYS
LOW	REALTEK

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/ESPI/SMBS/XTAL/CLK)
Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB
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[98] HDA_BCLK
[15] HDA_SDO
[27,98] HDA_SDI0
[27] HDA_SDOUT_CODEC
[27,98] HDA_SYNC_CODEC
[27] HDA_BITCLK_CODEC
[98] HDA_SYNC
[27] HDA_RST_N

[55] DISP_ON

[68] ME_FWP_PCH
[61] PCH_BT_RADIO_DIS_N
[79,86] GPU_GC6_FB_EN
[86] DGPU_PWR_EN

CPU1G 7 OF 22

DISP_ON EY34 GPP_D19/I2S_MCLK1_OUT

EV53 GPP_S0/SNDW0_CLK/I2S1_SCLK
EY53 GPP_S1/SNDW0_DATA/I2S1_SFRM

FA50 GPP_S2/SNDW1_CLK/DMIC_CKL_A0/I2S1_TXD
FC50 GPP_S3/SNDW1_DATA/DMIC_DATA0/I2S1_RXD

PROJECT_ID2 EV50 GPP_S4/SNDW2_CLK/DMIC_CLK_B0
EY50 GPP_S5/SNDW2_DATA/DMIC_CLK_B1

EW48 GPP_S6/SNDW3_CLK/DMIC_CLK_A1
EY48 GPP_S7/SNDW3_DATA/DMIC_DATA1

ALDER-LAKE-P-1-GP-U1

ZZ.PAD00.1C1

GPP_R0/HDA_BCLK/I2S0_SCLK/DMIC_CLK_B0/HDAPROC_BCLK
GPP_R1/HDA_SYNC/I2S0_SFRM/DMIC_CLK_B1
GPP_R2/HDA_SDO/I2S0_TXD/HDAPROC_SDO
GPP_R3/HDA_SDI0/I2S0_RXD/HDAPROC_SDI

GPP_R4/HDA_RST#/I2S2_SCLK/DMIC_CLK_A0
GPP_R5/HDA_SDI1/I2S2_SFRM/DMIC_DATA0
GPP_R6/I2S2_TXD/DMIC_CLK_A1
GPP_R7/I2S2_RXD/DMIC_DATA1

GPP_A11/PMC_I2C_SDA
GPP_A13/PMC_I2C_SCL

SNDW_RCOMP_1
SNDW_RCOMP_2

ER56 HDA_BCLK
EP60 HDA_SYNC
ER57 HDA_SDO
ER59 HDA_SDI0

ER53 HDA_RST_N
ET53 PROJECT_ID1
EB44 GPU_GC6_FB_EN
EB46 DGPU_PWR_EN

DV51 AUD_PWR_EN
DV47 PCH_BT_RADIO_DIS_N

FA53 SNDW_RCOMP
FC53

ME_FWP_PCH 1 R1907 2 2K2R2J-2-GP HDA_SDO

R1914 1 HDA_BITCLK_CODEC 33R2F-3-GP
R1915 1 HDA_SYNC_CODEC 33R2F-3-GP
R1916 1 HDA_SDOUT_CODEC 33R2F-3-GP

R1901 2 1 200R2F-L-GP

HDA_BITCLK_CODEC
HDA_RST_N
EC1902 SC1K50V2KX-1DLGP DY
R1909 100KR2F-L-GP DY

3D3V_S0
R1908 1 DY 2 100KR2F-L-GP AUD_PWR_EN

HDA_BCLK
EC1901 SC10P50V2JN-4DLGP DY
Follow BM15 MLK change to 10P

1D8V_S5
R1934 100KR1F-GP 18P
PROJECT_ID2
R1935 100KR2J-1-GP 18

3D3V_S0
R1936 100KR1F-GP UMA
PROJECT_ID1
R1937 100KR1F-GP QPS

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HDA/I2S/SD/DMIC)
Size: A3 | Document Number: SouthPeak15 MLK | Rev: SB
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[68] SBIOS_TX
[68] SBIOS_RX
[66] CONTACTLESS_DET_N
[56] ISH_ALS_INT_RF_1P8_N
[4,24] ISH_TABLE_MODE_N

[61,62] CNV_COEX2_1P8
[61,62] CNV_COEX1_1P8
[69,70,98] CPU_I2C_SDA_SENSOR
[69,70,98] CPU_I2C_SCL_SENSOR
[56,98] WA_SCL
[56,98] WA_SDA

[24,98] SML0B_SMBDATA
[24,98] SML0B_SMBCLK

[70] LNG2DMTR_INT1
[69] GSEN_INT1

[62,98] CPU_I2C_SDA_GNSS
[62,98] CPU_I2C_SCL_GNSS
[55,98] CPU_I2C_SDA_TS
[55,98] CPU_I2C_SCL_TS
[65] CPU_I2C_SDA_TP
[65] CPU_I2C_SCL_TP

[98] I2C0_SCL_TS
[98] I2C0_SDA_TS
[98] I2C1_SCL_TP
[98] I2C1_SDA_TP
[98] ISH_I2C0_SCL
[98] ISH_I2C0_SDA
[98] ISH_I2C1_SCL_RF_1P8
[98] ISH_I2C1_SDA_RF_1P8
[98] ISH_I2C2_SCL
[98] ISH_I2C2_SDA

CPU1F — 6 OF 22

TP2001

TS: SBIOS_TX EN48, SBIOS_RX EN46
ISH_LID_CL_TAB_N EL41 / EK41
TP: CONTACTLESS_DET_N EW30, ONE_DIMM_N EV34
SENSOR: I2C0_SCL_TS EH46, I2C0_SDA_TS EF46
ALS: I2C1_SCL_TP EH43, I2C1_SDA_TP EF43
ISH_I2C0_SCL DT57, ISH_I2C0_SDA DT56
ISH_I2C1_SCL_RF_1P8 DR56, ISH_I2C1_SDA_RF_1P8 DR58
CNV_COEX2_1P8 EN43, CNV_COEX1_1P8 EL43
WWAN: ISH_I2C2_SCL DN60, ISH_I2C2_SDA DN57

GPP_H11/UART0_TXD/M2_SKT2_CFG1
GPP_H10/UART0_RXD/M2_SKT2_CFG0
GPP_H13/I2C7_SCL/UART0_CTS#/M2_SKT2_CFG3/ISH_GP7B/DEVSLP1B
GPP_H12/I2C7_SDA/UART0_RTS#/M2_SKT2_CFG2/ISH_GP6B/DEVSLP0B
GPP_D18/UART1_TXD/ISH_UART1_TXD
GPP_D17/UART1_RXD/ISH_UART1_RXD
GPP_H5/I2C0_SCL
GPP_H4/I2C0_SDA
GPP_H7/I2C1_SCL
GPP_H6/I2C1_SDA
GPP_B6/ISH_I2C0_SCL/I2C2_SCL
GPP_B5/ISH_I2C0_SDA/I2C2_SDA
GPP_B8/ISH_I2C1_SCL/I2C3_SCL
GPP_B7/ISH_I2C1_SDA/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD
GPP_B17/I2C5_SCL/ISH_I2C2_SCL
GPP_B16/I2C5_SDA/ISH_I2C2_SDA

GPP_D14/ISH_UART0_TXD/I2C4B_SCL
GPP_D13/ISH_UART0_RXD/I2C4B_SDA
GPP_D16/ISH_UART0_CTS#/I2C7B_SCL
GPP_D15/ISH_UART0_RTS#/I2C7B_SDA
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPPC_RCOMP

EY28 SML0B_SMBCLK
EY28 SML0B_SMBDATA
EY36 MEM_INTERLEAVED
EW36
FA34 ISH_ALS_INT_RF_1P8_N
EY30 ISH_TABLE_MODE_D2_N — R2021 1 — 2 0R1J-GP — ISH_TABLE_MODE_N
EY31 ISH_ACC2_INT
EY31 ISH_ACC1_INT
DR61 GPPC_RCOMP — R2001 1 — 2 200R2F-L-GP

ALDER-LAKE-P-1-GP-U1

ZZ.PAD00.1C1

3D3V_S0
R2005 1 — 2 100KR2J-1-GP — CONTACTLESS_DET_N
RN2004 1 4 LNG2DMTR_INT1, 2 3 GSEN_INT1
SRN100KJ-6-GP

3D3V_S0
RN2006 SRN1KJ-7-GP
ISH_I2C2_SDA — R2022 0R1J-GP — CPU_I2C_SDA_GNSS
ISH_I2C2_SCL — R2023 0R1J-GP — CPU_I2C_SCL_GNSS

3D3V_S5_PCH
R2002 100KR2J-1-GP
MEM_INTERLEAVED
R2003 100KR2J-1-GP

DIMM_TYPE	
LOW	HIGH
NON_INTERLEAVED	INTERLEAVED

3D3V_S5_PCH
R2012 1 — 2 1KR2J-1-GP — SML0B_SMBCLK
R2014 1 — 2 1KR2J-1-GP — SML0B_SMBDATA
Follow CSLP 10k PU
R2004 1 — 10KR2F-2-GP — SBIOS_RX
R2007 1 — 10KR2F-2-GP — SBIOS_TX

DEBUG

1D8V_S0
RN2003 2 WA_SCL, 1 4 WA_SDA
SRN2K2J-1-GP
R2009 1 — 10KR2F-2-GP — ISH_ALS_INT_RF_1P8_N

WA_SCL — R2033 1 — 0R2J-2-GP — ISH_I2C1_SCL_RF_1P8
WA_SDA — R2034 1 — 0R2J-2-GP — ISH_I2C1_SDA_RF_1P8
CPU_I2C_SDA_SENSOR — R2032 1 — 0R2J-2-GP — ISH_I2C0_SDA
CPU_I2C_SCL_SENSOR — R2031 1 — 0R2J-2-GP — ISH_I2C0_SCL
LNG2DMTR_INT1 — R2042 1 — 0R2J-2-GP — ISH_ACC2_INT
GSEN_INT1 — R2048 1 — 0R2J-2-GP — ISH_ACC1_INT

3D3V_S0
RN2005 SRN2K2J-1-GP
I2C0_SDA_TS — R2015 0R2J-2-GP — CPU_I2C_SDA_TS
I2C0_SCL_TS — R2016 0R2J-2-GP — CPU_I2C_SCL_TS
I2C1_SDA_TP — R2019 0R2J-2-GP — CPU_I2C_SDA_TP
I2C1_SCL_TP — R2018 0R2J-2-GP — CPU_I2C_SCL_TP

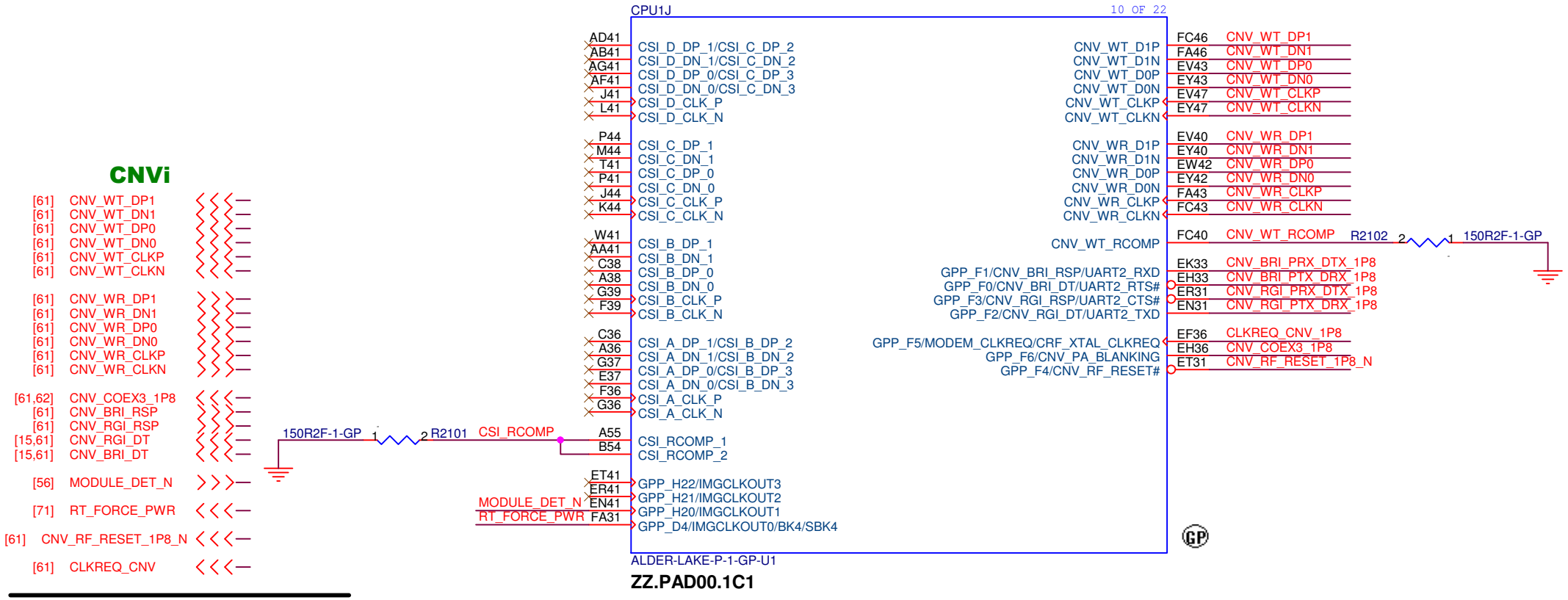
3D3V_S5_PCH
R2035 100KR2J-1-GP
DDR5
ONE_DIMM_N
R2011 100KR2J-1-GP
DDR4

DIMM Dectect	
HIGH	DDR5
LOW	DDR4

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A3 | Document Number: SouthPeak15 MLK | Rev: SB
Date: Friday, May 21, 2021 | Sheet 20 of 106



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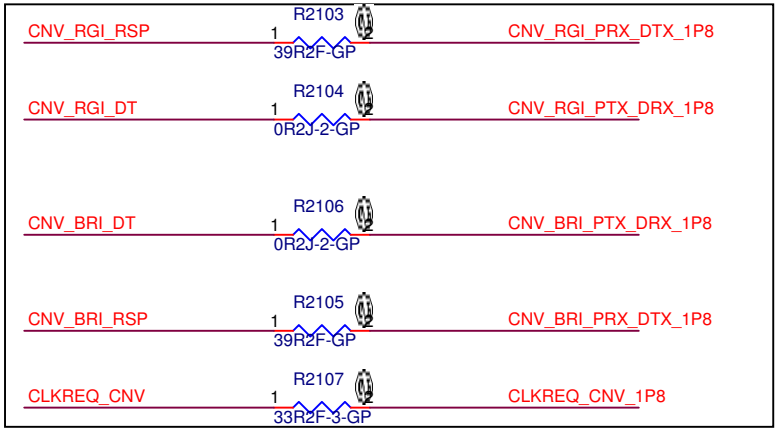
20210225
Follow PDG 1.0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (EMMC/CNVi)**

Size	Document Number	Rev
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[50] VSSINAUX_SENSE
[50] VCCINAUX_SENSE
[40,50] CORE_VID0_1P8
[40,50] CORE_VID1_1P8
[15] 3D3V_GPPR_S5
[17,24,39,40,68] SIO_SLP_S3_N
[3,24,46] PROCHOT_CPU_N
[3,44,72] PROCHOT_PD_R_N
[54] PWR_VNN1D05V_VID1
[54] PWR_VNN1D05V_VID2

CPU1N — ALDER-LAKE-P-1-GP-U1 — 14 OF 22

(Max 6A) 1D8V_VCCIN_AUX
1D8V_VCCIN_AUX
PWR_VNN1D05V_VID2 — R2216 — 0R2J-2-GP — V1P05_CTRL
PWR_VNN1D05V_VID1 — R2215 — 0R2J-2-GP — SIO_SLP_S3_N
R2207 — DY — 0R2J-2-GP — VNN_CTRL
1D8V_VCCIN_AUX_FLTR
PH/PL 100R at VR side
VSSINAUX_SENSE
VCCINAUX_SENSE
(200mA) 1D05V_VNN_BYPASS
(200mA) 1D05V_S5_BYPASS
3D3V_S5_PCH — R2212 — 10KR2J-3-GP — VRALERT_N — VNN_CTRL — V1P05_CTRL
CORE_VID0_1P8
CORE_VID1_1P8

VCCIN_AUX_1 … VCCIN_AUX_44
VCCIN_AUX_15 … VCCIN_AUX_42 (DH45, DJ41, DJ44, DK40, DK43, DK45, DL44, DM1, DM14, DM43, DP41, DP42, DR14, DR40, DT41, DU14, DU40, DV2, ED2, EL2, P1)
VCCIN_AUX_FLTR
VSSINAUX_SENSE (AH30)
VCCINAUX_SENSE (AF30)
VCC_VNNEXT_1P05_1 (EF21)
VCC_VNNEXT_1P05_2 (EH21)
VCC_V1P05EXT_1P05_1 (EE18)
VCC_V1P05EXT_1P05_2 (EE21)
GPP_B2/VRALERT# (DT59)
GPP_F22/VNN_CTRL (EK31)
GPP_F23/V1P05_CTRL (EL28)
GPP_B0/CORE_VID0 (EA60)
GPP_B1/CORE_VID1 (EA58)

1D8V_S5_VCCPRIM — R2202 — D01HSF-GP — 1D8V_S5 (Max 1.53A)
VCCPRIM_1P8_1 … VCCPRIM_1P8_23 (DW20, DW22, DW27, DW30, DY21, DY23, DY26, DY28, DY31, EB18, EB21, EB23, EB28, EC14, EC16, EC23, EC26, EE14, EE28, EG14, FB33)
VCCPRIM_3P3_1 … VCCPRIM_3P3_7 (DV41, DW40, EB33, EC31, EC33, EE31) — 3D3V_S5_PCH (Max 287mA)
RSVD_24 (FB45)
VCCLDOSTD_0P85 (FB52) — 0D85V_S5_VCCLDOSTD_OUT — Out — Trace width need to 12mil
VCCA_CLKLDO_1P8_1 / VCCA_CLKLDO_1P8_2 (EJ14, EM14) — 1D8V_S5_CLKLDO (Max 135mA) In — Trace width need to 20mil
VCCDPHY_1P24 (FB39) — 1D24V_S5_VCCDPHY_OUT (Max 22mA) Out — Trace width need to 12mil
RSVD_TP_28 … RSVD_TP_24 (BN43, AY11, BP44, BL12, BJ11, CN43, BJ11)
VCCPRIM1P05_OUT_PCH_1 / VCCPRIM1P05_OUT_PCH_3 (EB36, EC36, EE41) — 1D05V_S5_VCCPRIM_OUT — Out
VCCDSW_1P05 / VCC_MIPILP — TP_VCC_MIPILP — TP2210 — 1D05V_DSW (Max 6mA) Out
VCCPRIM1P05_OUT_PCH_2 / VCCPRIM1P05_OUT_PCH_4 (EB38, EE36) — 1D05V_S5_VCCPRIM_OUT — Out
1D24V_MIPI_DSI
If no used MIPI-DSI, VCC_MIPILP can be NC
VCCRTC (EC38) — 3D3V_RTC_PCH — R2214 — R2204 — 0R2J-2-GP — 3D3V_S5_PCH
VCCPDSW_3P3 (EB42) — 3D3V_VCCDSW — 3D3V_S5_PCH (Max 8mA) DSW
VCCPGPPR (EE33) — 3D3V_GPPR_S5 — (Max 22mA)
VCCPRIM_3P3_4 (EB41) — 3D3V_S5_PCH
VCCPRIM_1P8_10 (DY41) — 1D8V_S5_VCCPRIM
VCCPRIM_1P8_11 (DY42)
VCC1P05_PROC_1 / VCC1P05_PROC_2 (EU1, EU4) — 1D05V_VCCST
VCC1P05_OUT_FET_1 / VCC1P05_OUT_FET_2 / VCC1P05_OUT_FET_3 (EV3, EW1, EY1) — 1D05V_S5_OUT (1.5A) — Out for 1D05V_CPU, XDP
VCC_DISPIO (AM15) — 1D05V_DISPIO — R2208 — 0R2J-2-GP — 1D05V_VCCIO_OUT
If no used MIPI-DSI, VCC_DISPIO need link to 1D05V_VCCIO_OUT
RSVD_TP_25 … RSVD_TP_21 (BJ12, BK14, BF14)

ZZ.PAD00.1C1

Place cap within 3mm from SOC edge.
1D24V_S5_VCCDPHY_OUT — For CNVi — C2204 — C2225 — DY — SCD1U16V1KX-5-GP
Place cap within 3mm from SOC edge.
0D85V_S5_VCCLDOSTD_OUT — C2210 — C2223 — DY — SCD1U16V1KX-5-GP
Must take care this power layout and add shield GND.
1D8V_S5 — R2203 — 0R2J-2-GP — 1D8V_S5_CLKLDO (165mA)
C2227 — C2213 — C2212 — DY — SCD1U16V1KX-5-GP / SC220U6D3VM3X-1DLGP

(1.3A) 1D8V_S5_VCCPRIM — C2208 — C2207 — DY — SCD1U16V1KX-5-GP / SC1U10V2KX-1DLGP
Place cap closest possible to the BGA
3D3V_RTC_PCH — C2205 — C2206 — SC1U10V2KX-1DLGP / SCD1U16V2KX-3DLGP
Place cap closest possible to the BGA
1D05V_VCCST — C2217 — C2218 — C2221 — DY — SC1U10V2KX-1DLGP / SCD1U16V1KX-5-GP
PCH power rail should reserved 0.1u cap of factory requests
1D8V_VCCIN_AUX_FLTR — C2215 — C2216 — C2234 — DY — SC47U6D3V6MX-2-GP / SC10U6D3V2MX-2-GP / SCD1U16V1KX-5-GP
Put cap to close pin-EB33, EE31
3D3V_S5_PCH — RVT is reserve 1u and 0.1u cap — C2221 — C2222 — C2220 — DY — SC1U10V2KX-1DLGP / SCD1U16V1KX-5-GP

1D05V_VNN_BYPASS — DY — R2205 — 100KR2J-1-GP
1D05V_S5_BYPASS — DY — R2206 — 100KR2J-1-GP

PH Same as SPI Programming Guide for details
1D8V_S5 — RN2201 — CORE_VID0_1P8 / CORE_VDT_1P8 — SRN100KJ-6-GP
3D3V_S5_PCH — RN2202 — CORE_VID0_1P8 / CORE_VDT_1P8 — SRN100KJ-6-GP

Put cap to close pin-EB42
3D3V_VCCDSW — Factory requests PCH power rail should reserved 0.1u cap — C2211 — C2209 — DY — SCD1U16V1KX-5-GP / SC1U10V2KX-1DLGP
3D3V_GPPR_S5 — C2230 — DY — SCD1U16V1KX-5-GP
Place cap closest possible to the BGA
1D05V_DSW — W=15mil — C2214 — C2227 — DY — SCD1U16V1KX-5-GP / SC1U10V2KX-1DLGP
1D05V_S5_VCCPRIM_OUT — RVT doesn't reserve cap — C2203 — SC1U10V2KX-1DLGP
(200mA) 1D05V_S5_BYPASS — C2202 — C2235 — DY — SCD1U16V1KX-5-GP / SC1U10V2KX-1DLGP
(200mA) 1D05V_VNN_BYPASS — C2201 — C2236 — DY — SCD1U16V1KX-5-GP / SC1U10V2KX-1DLGP

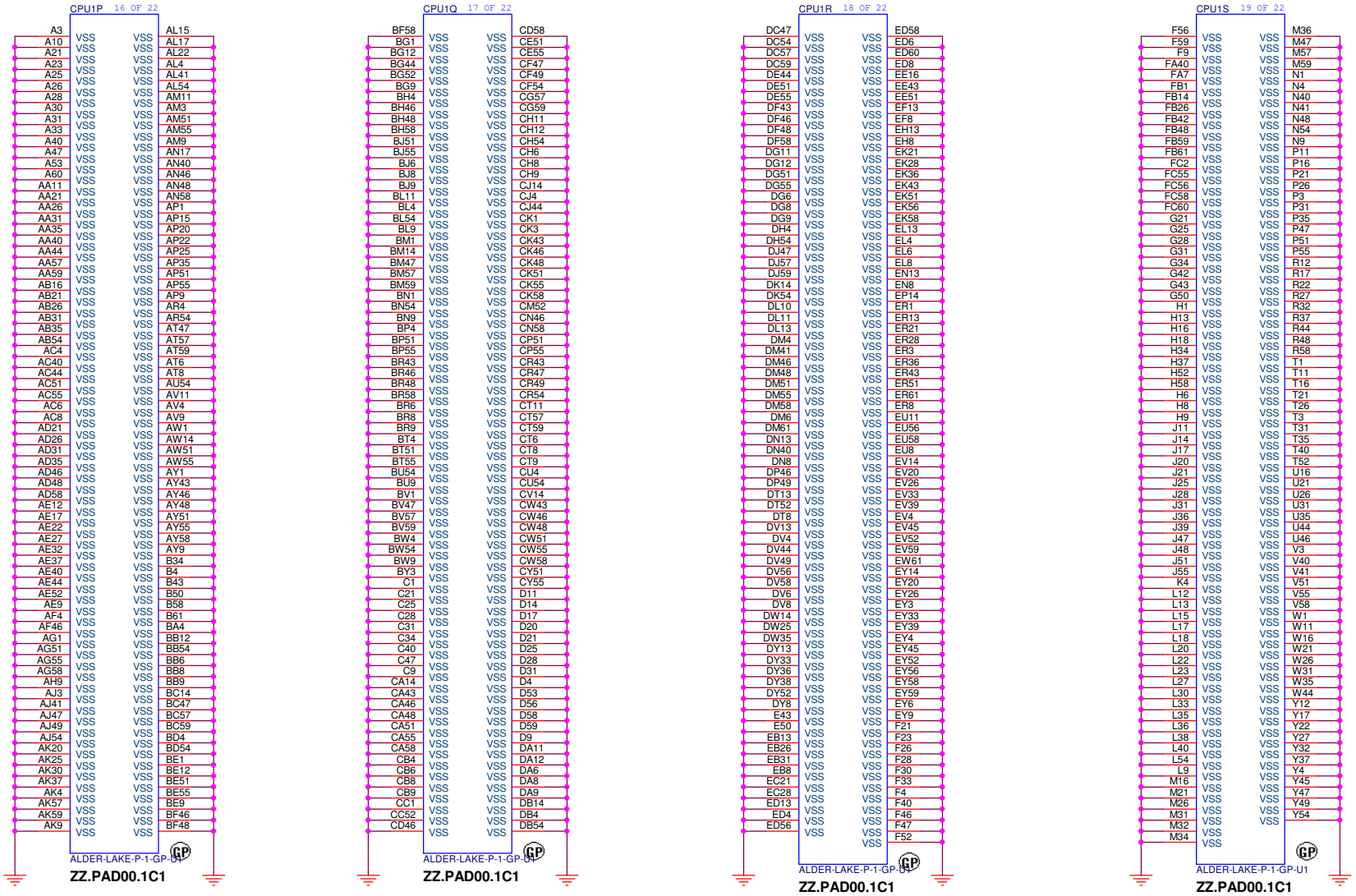
1D05V_S5_OUT — C2232 — DY — SCD1U16V1KX-5-GP
1D05V_DISPIO — Factory request PCH power rail should reserved 0.1u cap — C2233 — DY — SCD1U16V1KX-5-GP

PROCHOT_CPU_N
3D3V_S5_PCH — R2209 — 100KR1J-GP — Q2201_G
LMBT3904LT1G-GP — Q2201 — 84.T3904.H11 — 2nd = 84.03904.T11 — 3rd = 084.03904.0H11
R2211 — 0R1J-GP — PROCHOT_PD_R_N — VRALERT_N

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)
Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB
Date: Friday, May 21, 2021 | Sheet 22 of 106



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: SouthPeak15 MLK | Rev: SB

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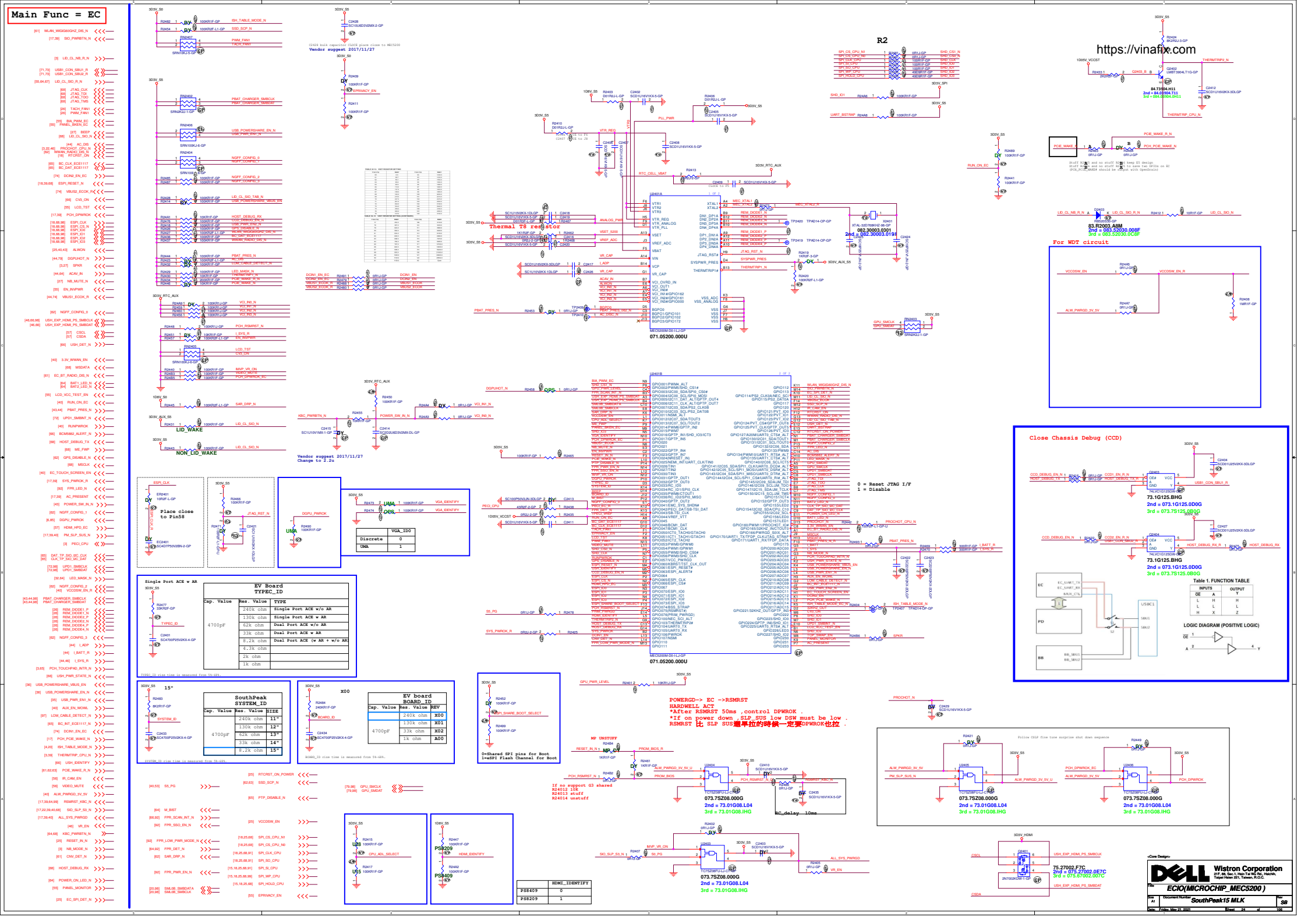
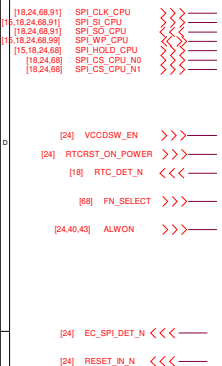
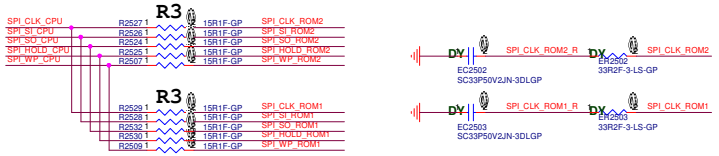
Main Func = EC


https://vinafix.com
Vendor suggest 2017/11/27
Thermal TS resistor
LID_WAKE
NON_LID_WAKE
Vendor suggest 2017/11/27
Change to 2.2u
Place close to Pin58
Close Chassis Debug (CCD)
0 = Reset JTAG I/F
1 = Disable
Single Port ACE w AR
EV Board TYPEC_ID
SouthPeak SYSTEM_ID
EV board BOARD_ID
0=Shared SPI pins for Boot
1=eSPI Flash Channel for Boot
POWERGD-> EC ->RSMRST
HARDWELL ACT
*After RSMRST 50ms ,control DPWROK .
*If on power down ,SLP_SUS low DSW must be low .
RSMRST 比 SLP SUS還早拉的時候一定要DPWROK也拉 .
If no support G3 shared
R24012 10K
R24013 stuff
R24014 unstuff
For WDT circuit
Table 1. FUNCTION TABLE
LOGIC DIAGRAM (POSITIVE LOGIC)
R2
Wistron Corporation
ECIO(MICROCHIP_MEC5200)
SouthPeak15 MLK
Friday, May 21, 2021

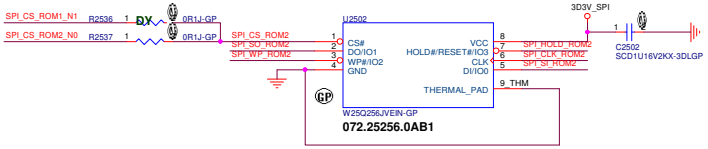
Main Func = BIOS ROM/RTC



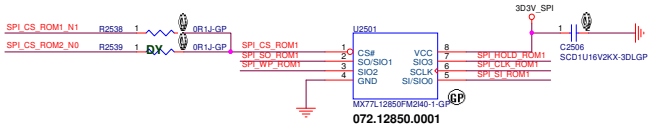
SYSTEM SPI ROM



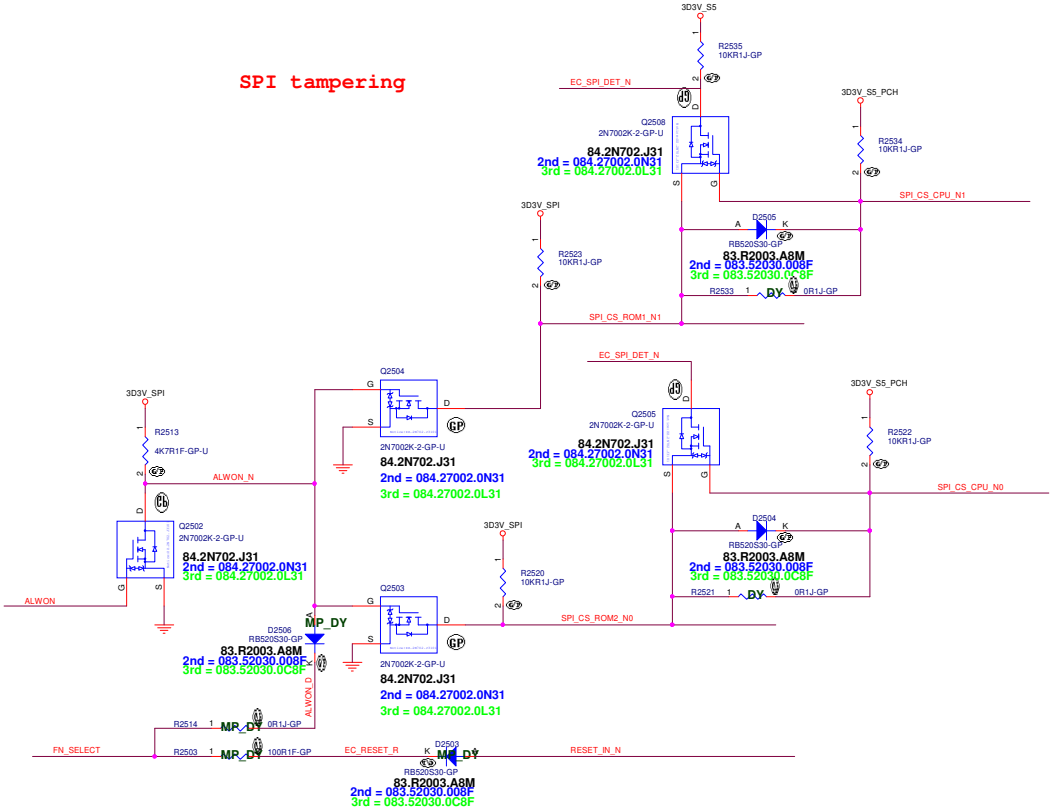
32M ROM : 072.25256.0AB1



16M RPMC ROM : 072.12850.0001

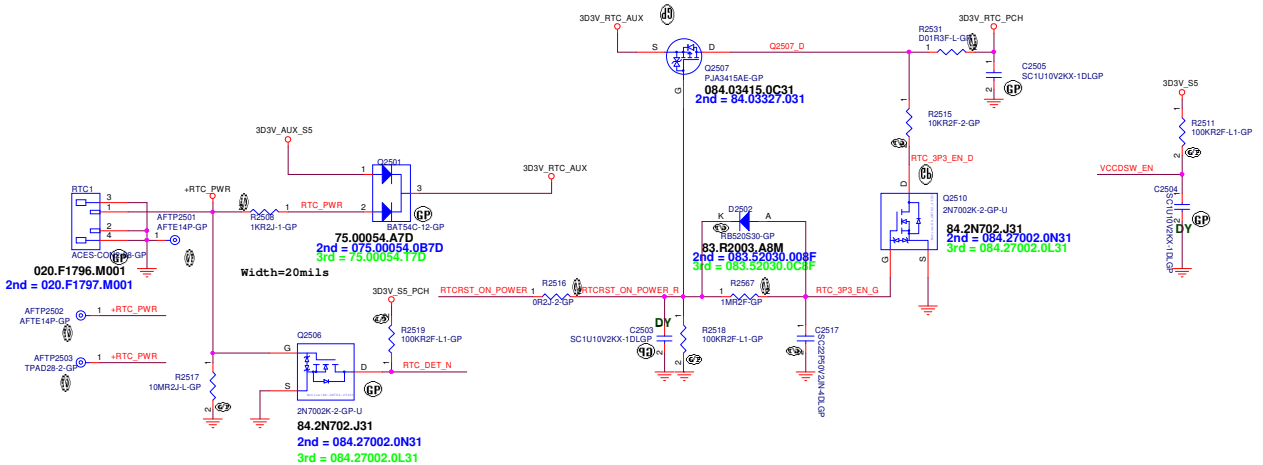


SPI tampering



https://vinafix.com

X09 design DS3_Non-DS3 with RTC power gating



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB

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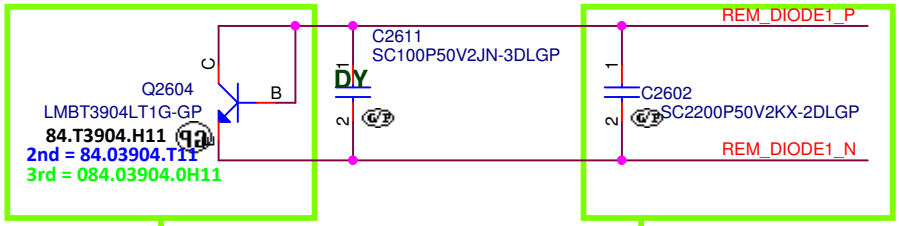
Main Func = Thermal / FAN

Description	Functionality
Q2601(TOP)	GPU
Q2602(BOT)	CPU
Q2603(BOT)	SSD2
Q2604(TOP)	CPU PWR
Q2605(BOT)	Amb.

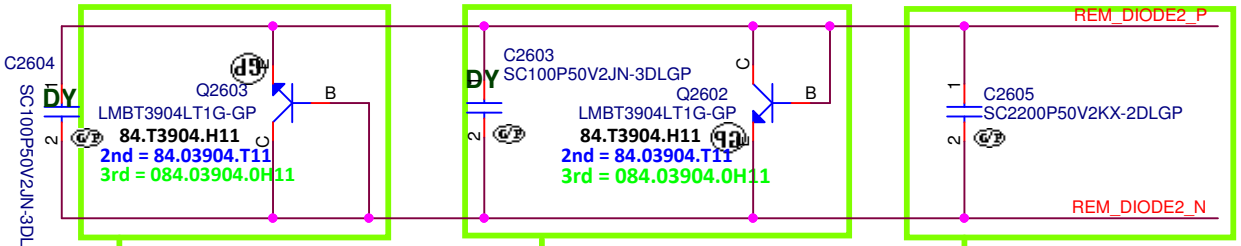
[24] REM_DIODE1_P
[24] REM_DIODE1_N
[24] REM_DIODE2_P
[24] REM_DIODE2_N

[24] REM_DIODE4_P
[24] REM_DIODE4_N
[24] PWM_FAN1
[24] TACH_FAN1



Layout Note: Place to CPU PWR
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

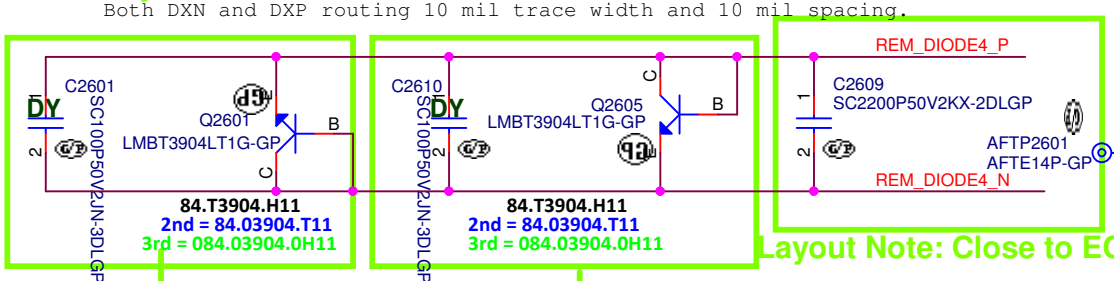
Layout Note: Close to EC



Layout Note:Place to SSD2
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to CPU

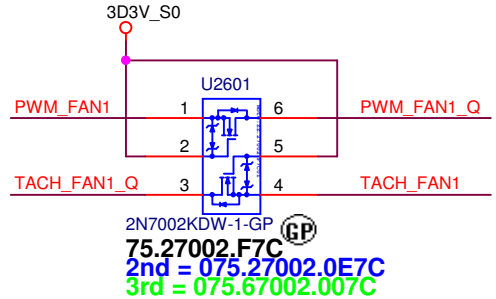
Layout Note: Close to EC

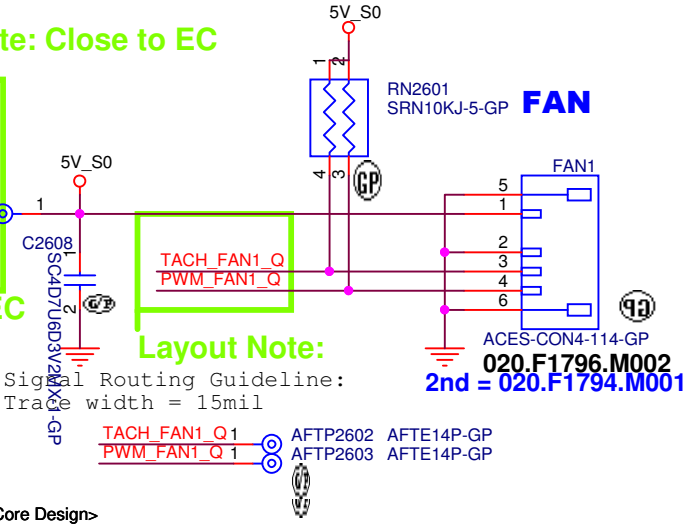


Layout Note:Place to GPU
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note:Place to DM

Layout Note: Close to EC





Layout Note:
Signal Routing Guideline:
Trace width = 15mil

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

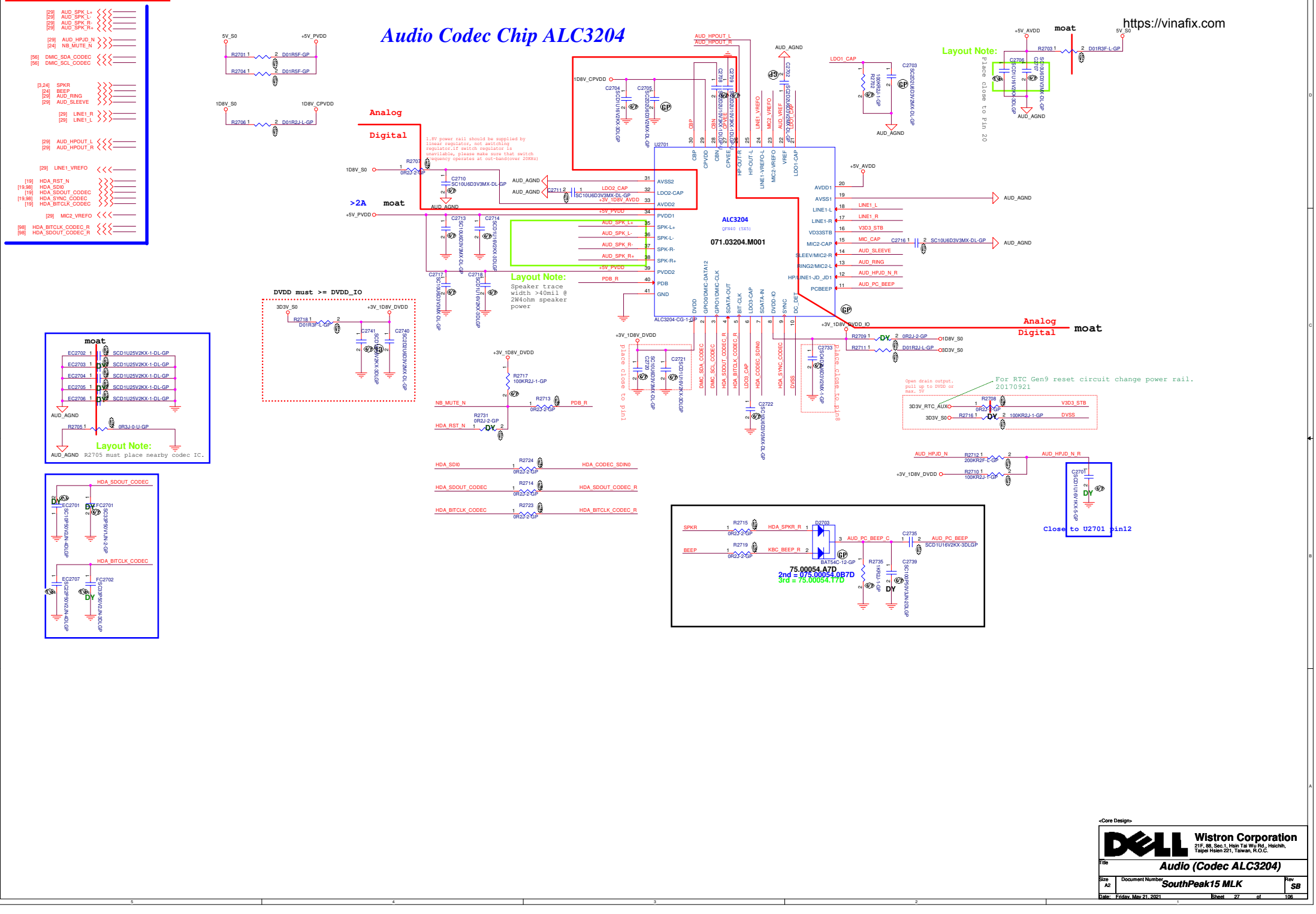
Title: INT IO (Thermal/Fan)

Size: A4 | Document Number: SouthPeak15 MLK | Rev: SB

Date: Friday, May 21, 2021 | Sheet 26 of 106

Main Func = Audio

Audio Codec Chip ALC3204



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (Codec ALC3204)

Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio (RSVD) (Audio AMP)***

Size	Document Number	Rev
A4	***SouthPeak15 MLK***	***SB***

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Main Func = Audio

[27] AUD_SPK_L+
[27] AUD_SPK_L-
[27] AUD_SPK_R-
[27] AUD_SPK_R+
[27] MIC2_VREFO
[27] AUD_RING
[27] AUD_HPOUT_L
[27] LINE1_L
[27] AUD_HPOUT_R
[27] LINE1_R
[27] AUD_SLEEVE
[27] AUD_HPJD_N
[27] LINE1_VREFO

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

AUD_SPK_L+ — EL2901 — HCB1005KF-121T20-GP — AUD_SPK_L+_C
AUD_SPK_L- — EL2902 — HCB1005KF-121T20-GP — AUD_SPK_L-_C
AUD_SPK_R- — EL2903 — HCB1005KF-121T20-GP — AUD_SPK_R-_C
AUD_SPK_R+ — EL2904 — HCB1005KF-121T20-GP — AUD_SPK_R+_C

main: 68.00358.031
2nd: 068.00006.0041

EC2904 SC100P50V2JN-3DLGP
EC2903 SC100P50V2JN-3DLGP
EC2901 SC100P50V2JN-3DLGP
EC2902 SC100P50V2JN-3DLGP

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

HI	YG
LOW	FG

EC2908 SC1KP50V2KX-1DLGP
EC2907 SC1KP50V2KX-1DLGP
EC2906 SC1KP50V2KX-1DLGP
EC2905 SC1KP50V2KX-1DLGP

SPK1
ACES-CON6-91-GP
020.F1803.M001
2nd = 020.F1804.M001

AUD_SPK_L+_C
AUD_SPK_L-_C
AUD_SPK_R-_C
AUD_SPK_R+_C

ED2904 AZ5725-01FDR7G-GP — 2nd = 083.00511.00AF (83.05725.0A0)
ED2905 AZ5725-01FDR7G-GP — 2nd = 083.00511.00AF (83.05725.0A0)
ED2906 AZ5725-01FDR7G-GP — 2nd = 083.00511.00AF (83.05725.0A0)
ED2907 AZ5725-01FDR7G-GP — 2nd = 083.00511.00AF (83.05725.0A0)

MIC2_VREFO — RN2901 SRN2K2-J-1-GP
AUD_RING — R2901 0R3J-0-U-GP — AUD_HP1_JACK_L1
AUD_HPOUT_L
LINE1_L — C2901 SC10U6D3V3MX-DL-GP — LINE1-L_C — R2904 0R2J-2-GP
AUD_HPOUT_R — R2906 0R3J-0-U-GP — AUD_HP1_JACK_R1
LINE1_R — C2902 SC10U6D3V3MX-DL-GP — LINE1-R_C — R2908 0R2J-2-GP
AUD_SLEEVE

D2901 BAT54A-11-GP
LINE1_VREFO — LINE1_VREFO_D1 — R2910 4K7R2J-2-GP
LINE1_VREFO — LINE1_VREFO_D2 — R2916 4K7R2J-2-GP
75.BAT54.07D
2nd = 075.00054.0A7D
3rd = 75.00054.I7D

Layout Note:
R2901 must place nearby AUD1.

R2905 0R5J-5-GP — AUD_AGND

R2902 0R3J-0-U-GP — R2903 16D2R3F-2-GP — RING2_R — AUD_PORTA_L_R_B
R2907 16D2R3F-2-GP — R2909 0R3J-0-U-GP — AUD_PORTA_R_R_B — SLEEVE_R

EC2909 SC680P50V2KX-2DLGP
EC2910 SC680P50V2KX-2DLGP
EC2911 SC680P50V2KX-2DLGP
EC2912 SC680P50V2KX-2DLGP
AUD_AGND

Universal Jack

AUD1
RING2_R
AUD_PORTA_L_R_B
JACK_PLUG
JACK_PLUG_DET
AUD_PORTA_R_R_B
SLEEVE_R
MS
AUDIO-JK727-GP
022.10002.M009
2nd = 022.10002.M010

RING2_R
AUD_PORTA_L_R_B
JACK_PLUG
JACK_PLUG_DET
AUD_PORTA_R_R_B
SLEEVE_R

ED2901 AZ5125-02S-R7G-GP — 75.05125.07D — 2nd = 075.52215.007D
ED2902 AZ5125-02S-R7G-GP — 75.05125.07D — 2nd = 075.52215.007D
ED2903 AZ5125-02S-R7G-GP — 75.05125.07D — 2nd = 075.52215.007D

AUD_HPJD_N — R2913 0R0603-PAD-1-GP-U — JACK_PLUG

Delay circuit

JACK_PLUG_DET — R2914 0R0402-PAD-1-GP — AUD_AGND

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (HP/SPK/MIC Jack)
Size: A3
Document Number: SouthPeak15 MLK
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Date: Friday, May 21, 2021
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio (HP/SPK/MIC Jack)***

Size	Document Number	Rev
A4	***SouthPeak15 MLK***	***SB***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***LAN (RSVD)***

Size	Document Number	Rev
A4	***SouthPeak15 MLK***	***SB***

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Main Func = LAN

[24,64] LED_MASK_N
[97] LAN_0_GREEN_LINK_N
[97] LAN_1_AMBER_ACT_N

[97] LAN_MDI0_P
[97] LAN_MDI0_N

[97] LAN_MDI1_P
[97] LAN_MDI1_N

[97] LAN_MDI2_P
[97] LAN_MDI2_N

[97] LAN_MDI3_P
[97] LAN_MDI3_N

XF3201

LAN_MDI3_N 2 — 1CT:1CT — 23 MDO3-
1 — 24 MCT0
LAN_MDI3_P 3 — 22 MDO3+
LAN_MDI2_N 5 — 1CT:1CT — 20 MDO2-
4 — 21 MCT1
LAN_MDI2_P 6 — 19 MDO2+
LAN_MDI1_N 8 — 1CT:1CT — 17 MDO1-
7 — 18 MCT2
LAN_MDI1_P 9 — 16 MDO1+
LAN_MDI0_N 11 — 1CT:1CT — 14 MDO0-
10 — 15 MCT3
LAN_MDI0_P 12 — 13 MDO0+

XFORM-24P-19-GP
68.IH601.301
2nd = 68.05009.30A
3rd = 068.24002.3001

LOM_TCT
C3202 SCD01U25V2KX-3DLGP

Layout note:
30 mil spacing between MDI differential pairs.
Follow Reference Schematic 0.01uF~0.4uF

3D3V_LAN

LOM_AMB_N 1 — R3202 510R2J-1-GP — 2 LOM_AMB_N_R

https://vinafix.com

RJ45
MDO3- 13
MDO3+ 9
MDO1- 8
MDO2- 7
MDO2+ 6
MDO1+ 5
MDO0- 4
MDO0+ 3
2
1
11
14
Amber 15 10
Green 12 16

Check again Lan Led behavior as ARD want

LOM_GRN_N 1 — R3201 510R2J-1-GP — 2 LOM_GRN_N_R

RJ45-LED-12P-49-GP-U
022.10008.0881
2nd = 022.10001.08Y1

1
AFTP3214 AFTE14P-GP

ED3201

LAN_MDI3_N 1 — 10 LAN_MDI3_N
LAN_MDI3_P 2 — 9 LAN_MDI3_P
LAN_MDI2_N 4 — 7 LAN_MDI2_N
LAN_MDI2_P 5 — 6 LAN_MDI2_P
8
3

075.01043.0073
2nd = 075.73044.0003
3rd = 075.08810.0A73
AZ1043-04F-R7G-GP

ED3202

LAN_MDI1_N 1 — 10 LAN_MDI1_N
LAN_MDI1_P 2 — 9 LAN_MDI1_P
LAN_MDI0_N 4 — 7 LAN_MDI0_N
LAN_MDI0_P 5 — 6 LAN_MDI0_P
8
3

075.01043.0073
2nd = 075.73044.0003
3rd = 075.08810.0A73
AZ1043-04F-R7G-GP

MCT0
MCT1
MCT2
MCT3

RN3201
SRN75J-1-GP

MCT

C3201
SC56P3KV8JN-1-GP
078.5603N.014D
Follow KS13 cap

LOM_GRN_N_R
EC3202 SC1KP50V2KX-1DLGP

LOM_AMB_N_R
EC3203 SC1KP50V2KX-1DLGP

LAN_1_AMBER_ACT_N 4 — Q3202 — 3 LOM_AMB_N
LED_MASK_N 5 — 2 LED_MASK_N
LOM_GRN_N 6 — 1 LAN_0_GREEN_LINK_N

2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C

- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD) (RJ45+Transformer)

Size	Document Number	Rev
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Main Func = Card Reader

[16] CARD_PCIE_RX_N
[16] CARD_PCIE_RX_P
[16] CARD_PCIE_TX_N
[16] CARD_PCIE_TX_P

[18,39] CARD_CLK_CPU_P
[18] CARD_CLK_CPU_N
[18] CLKREQ_PCIE5_N
[18] MEDIACARD_IRQ_N

[17,61,62,63,76,91,97,99] PCH_PLTRST_RIGHT_N
[4] HOST_SD_WP_N

Layout Note:

3D3V_S0_CARD — Close to pin11
3D3V_AUX_CARD — Close to pin27
Close to pin14
Close to pin10

C3301 SCD1U16V2KX-3DLGP
C3302 SCD1U16V2KX-3DLGP
C3303 SC4D7U6D3V2MX-1-GP
C3304 SCD1U16V2KX-3DLGP

1D2V_LDO
C3306 SC4D7U6D3V2MX-1-GP
C3307 SCD1U16V2KX-3DLGP
C3308 SCD1U16V2KX-3DLGP

SD_VDD1
C3314 SCD1U16V2KX-3DLGP
C3315 SC4D7U6D3V2MX-1-GP

Layout Note:Close to Card Reader CONN

SD_VDD2
C3316 SCD1U16V2KX-3DLGP
C3317 SC4D7U6D3V2MX-1-GP

3D3V_S0_CARD

850mA

3D3V_S0 — R3301 D01R5F-GP — 3D3V_S0_CARD
3D3V_S0_CARD — R3303 0R3J-0-U-GP — 3D3V_AUX_CARD
3D3V_AUX_CARD — R3302 10KR2F-2-GP — MEDIACARD_IRQ_N

https://vinafix.com

U3301

1D2V_LDO	10	AV12	
3D3V_S0_CARD	11	3V3_IN	
	12	CARD_3V3	
	13	SD_VDD2	
1D2V_LDO	14	DV12S	
DV33_18	18	DV33_18	
3D3V_AUX_CARD	27	3V3AUX	
CARD_PCIE_TX_P	3	HSIP	
CARD_PCIE_TX_N	4	HSIN	
CARD_PCIE_RX_P	7	HSOP	
CARD_PCIE_RX_N	8	HSON	
CARD_CLK_CPU_P	5	REFCLKP	
CARD_CLK_CPU_N	6	REFCLKN	
SD_D0P	26	SD_LN0_P	
SD_D0N	25	SD_LN0_M	
SD_D1P	22	SD_LN1_P	
SD_D1N	23	SD_LN1_M	
	15	SP1	SD_DATA1
	16	SP2	SD_DATA0
	17	SP3	SD_CLK
	19	SP4	SD_CMD
	20	SP5	SD_DATA3
	21	SP6	SD_DATA2
	29	SP7	SD_WP
	30	SD_CD#	SD_CD_N
	31	MS_INS#	MS_INS_N
	1	PERST#	PCIE_CARD_PLT_RST_N
	2	CLK_REQ#	CLKREQ_PCIE5_N
	32	WAKE#	DEV_WAKE_N
	9	RREF	CARD_RREF
	24	SDREG2	CARD_SDREG2
	28	GPIO	CARD_GPIO
	33	GND	

R3305 0R2J-2-GP — SD_DATA1_CON
R3306 0R2J-2-GP — SD_DATA0_CON
ER3304 10R2F-L-GP — SD_CLK_CON
R3307 0R2J-2-GP — SD_CMD_CON
R3308 0R2J-2-GP — SD_DATA3_CON
R3309 0R2J-2-GP — SD_DATA2_CON

TP3301
R3310 0R2J-2-GP — PCH_PLTRST_RIGHT_N
R3311 0R2J-2-GP — MEDIACARD_IRQ_N
R3312 10KR2F-2-GP — 3D3V_AUX_CARD
C3313 SC1U10V2KX-1DLGP
R3313 6K2R2F-GP

RTS5242-GR-GP-U
071.05242.0003

For UHS-II

C3305 SC1U10V2KX-1DLGP
C3309 SCD1U16V2KX-3DLGP
C3310 SCD1U16V2KX-3DLGP
C33111 SCD1U16V2KX-3DLGP
C33121 SCD1U16V2KX-3DLGP

Vendor:
EC3301 Closed to chip

EC3301 SC5P50V2CN-2DL-GP
R3304 0R2J-2-GP
Q3301 2N7002K-2-GP-U
HOST_SD_WP_N — G
D — SD_WP
S

84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

SD_CD_N
EC3306 SC1KP50V2KX-1DLGP

ED3302 UCLAMP0502T-TCT-GP
SD_CLK_CON — K1
SD_CMD_CON — K2
A
83.00502.0A0
2nd = 083.08822.00A3

ED3303 UCLAMP0502T-TCT-GP
SD_DATA0_CON — K1
SD_DATA1_CON — K2
A
83.00502.0A0
2nd = 083.08822.00A3

ED3304 UCLAMP0502T-TCT-GP
SD_DATA2_CON — K1
SD_DATA3_CON — K2
A
83.00502.0A0
2nd = 083.08822.00A3

ED3305 UCLAMP0502T-TCT-GP
SD_D0P — K1
SD_D0N — K2
A
83.00502.0A0
2nd = 083.08822.00A3

ED3306 UCLAMP0502T-TCT-GP
SD_D1P — K1
SD_D1N — K2
A
83.00502.0A0
2nd = 083.08822.00A3

SD_VDD2 SD_VDD1

CARD1

	4	VDD1	D0+ 13 SD_D0P
	10	VDD2	D0- 14 SD_D0N
			D1+ 17 SD_D1P
			D1- 16 SD_D1N
SD_DATA0_CON	7	DAT0/RCLK+	
SD_DATA1_CON	8	DAT1/RCLK-	
SD_DATA2_CON	1	DAT2	VSS 6
SD_DATA3_CON	2	CD/DAT3	VSS 12
			VSS 15
			VSS 18
SD_CMD_CON	3	CMD	
SD_CLK_CON	5	CLK	GND 19
SD_CD_N	9	CD	GND 20
	11	SWIO	GND 21
			GND 22

CARDBUS18P-1-GP-U
062.10045.0021

SD_DATA3_CON
SD_DATA2_CON
SD_DATA1_CON
SD_DATA0_CON

EC3303 SCD6D8P50V2CN-DL-GP
EC3304 SCD6D8P50V2CN-DL-GP
EC3305 SCD6D8P50V2CN-DL-GP
EC3302 SCD6D8P50V2CN-DL-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARDREADER (SDIO/SD Conn)**

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

USB (RSVD) (USB2.0 CONN)

Size	Document Number	Rev
A4	***SouthPeak15 MLK***	***SB***

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Main Func = USB 3.0

USB3/USB31-4/USB20-3/PowerShare

USB3.1 PORT1

[16] USB1_USB31_RX_N
[16] USB1_USB31_RX_P
[16] USB1_USB31_TX_N
[16] USB1_USB31_TX_P

USB2.0 port3

[36] USB3_USB20_N
[36] USB3_USB20_P

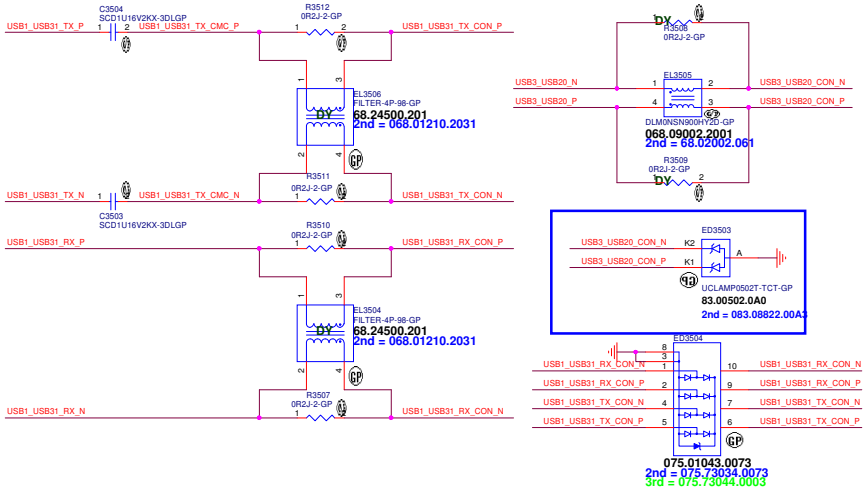
USB3.1 PORT2

[16] USB2_USB31_RX_N
[16] USB2_USB31_RX_P
[16] USB2_USB31_TX_N
[16] USB2_USB31_TX_P

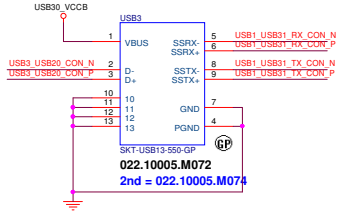
USB2.0 port4

[16] USB4_USB20_N
[16] USB4_USB20_P

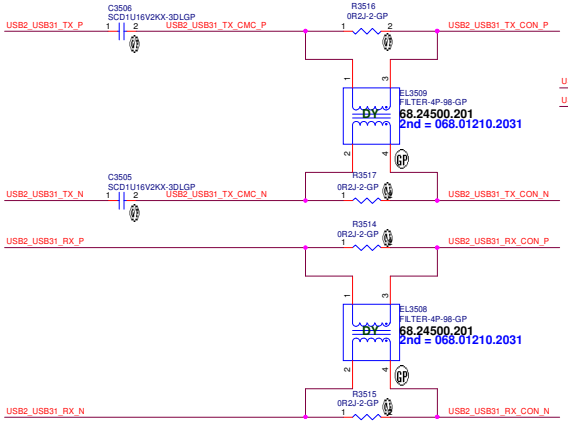
[24] USB_PWR_EN1_N
[4] USB_OC1_N

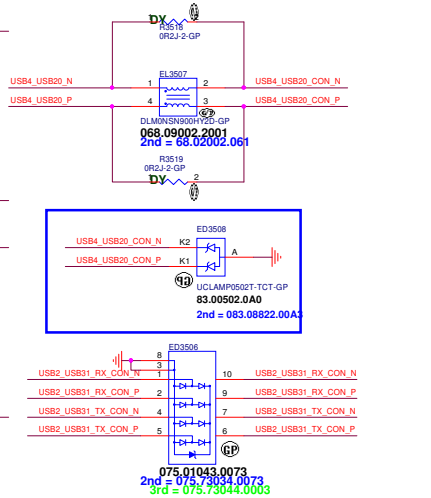


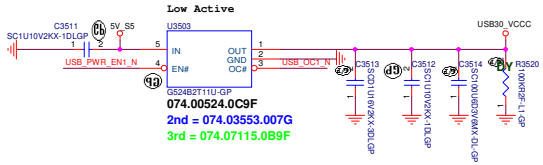
EXT Port1 Right Side, Support Power Share



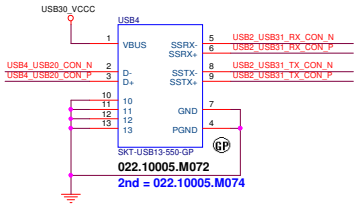
USB4/USB31-3/USB20-4







EXT Port1 Right Side, Support Power Share



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB (USB3.0 CONN)**

Size	Document Number	Rev
A2	SouthPeak15 MLK	SB

Date: Friday, May 21, 2021 Sheet 35 of 106

Main Func = USB Charger

support power share on the USB3.0 port on the right side of platform

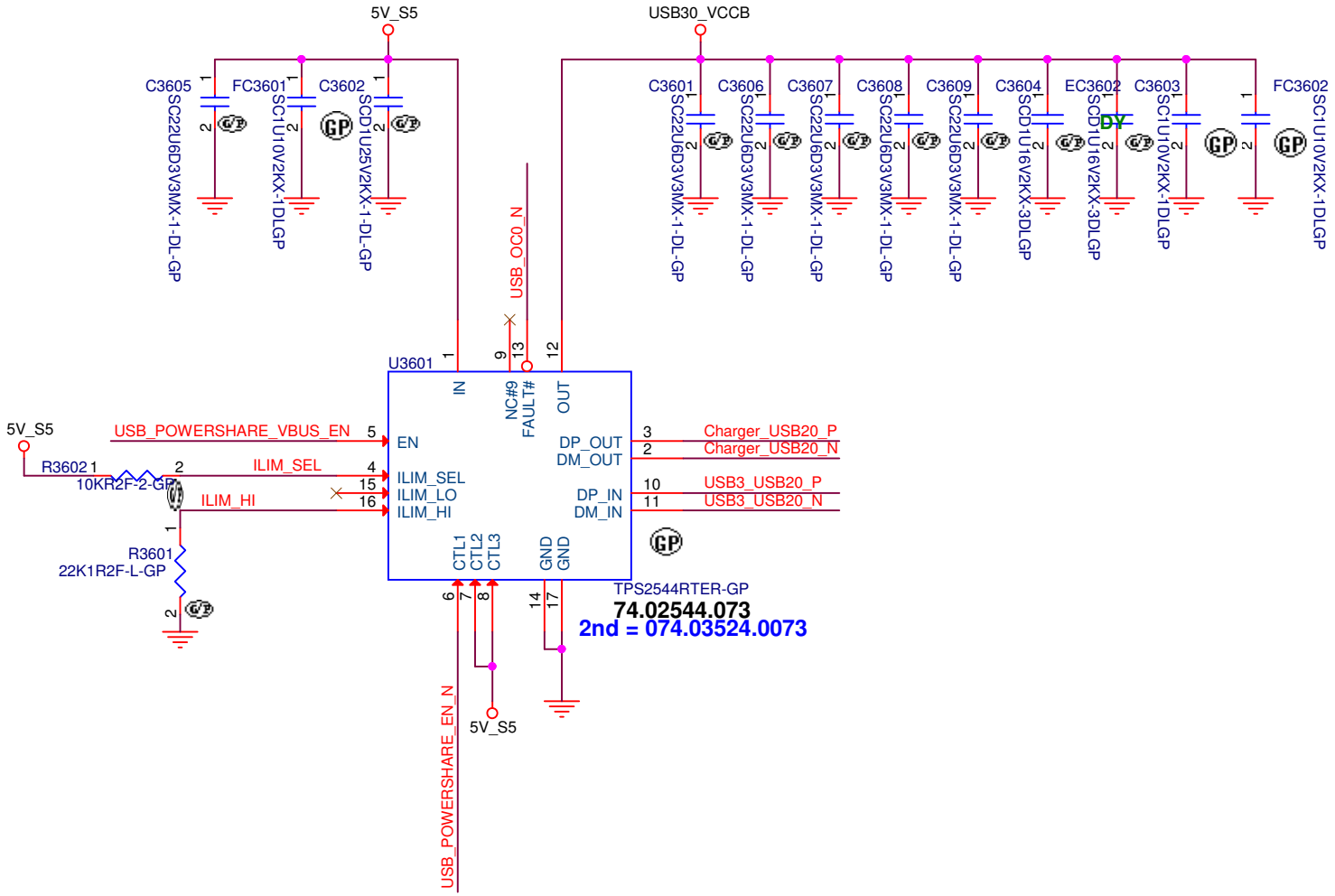
USB2.0 port3

[35] USB3_USB20_N
[35] USB3_USB20_P
[16] USB_OC0_N
[24] USB_POWERSHARE_VBUS_EN
[24] USB_POWERSHARE_EN_N

USB charger

[16] Charger_USB20_N
[16] Charger_USB20_P

USB3.0 Port2



Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB Charger)

Size: A4 | Document Number: SouthPeak15 MLK | Rev: SB

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (PCIE to USB3.0)

Size	Document Number	Rev
A4	***SouthPeak15 MLK***	***SB***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB Redriver/Hub)

Size	Document Number	Rev
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PSTP3901	1 PSTP14-OP-1-GP	SIO_PWRBTN_N [17,24]
PSTP3902	1 PSTP14-OP-1-GP	RTC_RST_N [18,68]
PSTP3903	1 PSTP14-OP-1-GP	SIO_SLP_S4_N [17,51,68]
PSTP3904	1 PSTP14-OP-1-GP	DDR_VTT_CTRL [5]
PSTP3905	1 PSTP14-OP-1-GP	SRTC_RST_N [18]
PSTP3906	1 PSTP14-OP-1-GP	SVID_CLK_CPU [7,46]
PSTP3908	1 PSTP14-OP-1-GP	ESPI_RESET_N [18,24,68]
PSTP3909	1 PSTP14-OP-1-GP	CPU_PWRGD [17]
PSTP3910	1 PSTP14-OP-1-GP	CPU_C10_GATE_N [17,91]
PSTP3911	1 PSTP14-OP-1-GP	SM_DRAMRST_CPU_N [5]
PSTP3912	1 PSTP14-OP-1-GP	SUSCLK [18,61]
PSTP3913	1 PSTP14-OP-1-GP	CARD_CLK_CPU_P [18,33]
PSTP3914	1 PSTP14-OP-1-GP	AC_PRESENT [17,24]
PSTP3915	1 PSTP14-OP-1-GP	SIO_SLP_S5_N [17,68]
PSTP3916	1 PSTP14-OP-1-GP	THERMTRIP_CPU_N [3,24]
PSTP3917	1 PSTP14-OP-1-GP	DSW_PWROK_R [17]
PSTP3918	1 PSTP14-OP-1-GP	PCH_DPWROK [17,24]
PSTP3919	1 PSTP14-OP-1-GP	VCCST_PWRGD [17,39]
PSTP3920	1 PSTP14-OP-1-GP	VCCST_PWRGD [17,39]
PSTP3921	1 PSTP14-OP-1-GP	SIO_SLP_S3_N [17,22,24,39,40,68]
PSTP3922	1 PSTP14-OP-1-GP	SIO_SLP_S3_N [17,22,24,39,40,68]
PSTP3923	1 PSTP14-OP-1-GP	PM_SLP_SUS_N [17,24,39,40]
PSTP3924	1 PSTP14-OP-1-GP	PM_SLP_SUS_N [17,24,39,40]
PSTP3925	1 PSTP14-OP-1-GP	SYS_PWROK_R [17,24,39]
PSTP3926	1 PSTP14-OP-1-GP	SYS_PWROK_R [17,24,39]
PSTP3927	1 PSTP14-OP-1-GP	ALL_SYS_PWRGD [17,24,39,40]
PSTP3928	1 PSTP14-OP-1-GP	ALL_SYS_PWRGD [17,24,39,40]

PSTP3931	1 PSTP14-OP-1-GP	PCH_PLTRST_N [17,39]
PSTP3932	1 PSTP14-OP-1-GP	PCH_PLTRST_N [17,39]
PSTP3933	1 PSTP14-OP-1-GP	PCH_PWROK_R [17,39]
PSTP3934	1 PSTP14-OP-1-GP	PCH_PWROK_R [17,39]
PSTP3935	1 PSTP14-OP-1-GP	RSMRST_KBC_N [17,24,39,64,99]
PSTP3936	1 PSTP14-OP-1-GP	RSMRST_KBC_N [17,24,39,64,99]

PSTP3937	1 PSTP14-OP-1-GP	1D2V_S3
PSTP3938	1 PSTP14-OP-1-GP	3D3V_S5
PSTP3939	1 PSTP14-OP-1-GP	3D3V_RTC_AUX
PSTP3940	1 PSTP14-OP-1-GP	1D8V_S5
PSTP3941	1 PSTP14-OP-1-GP	PWR_VDDQVTT
PSTP3942	1 PSTP14-OP-1-GP	1D8V_S0
PSTP3943	1 PSTP14-OP-1-GP	1D8V_VCCIN_AUX
PSTP3944	1 PSTP14-OP-1-GP	1D05V_VCCST
PSTP3945	1 PSTP14-OP-1-GP	1D05V_VCCST
PSTP3948	1 PSTP14-OP-1-GP	3D3V_S5_PCH

<Core Design>

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Title: ***Sequence (RSVD)***

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Main Func = Power Plane EN Sequence

[24,25,43] ALWON
[45] 3V5V_EN
[45] 3D3V_PG
[45] 5V_PG
[24] ALW_PWRGD_3V_5V
[17] PM_SLP_LAN_N
[24] AUX_EN_WOWL
[24] 3.3V_WWAN_EN
[99] XDP_OVERRIDE_N
[57] RUN_ON_R
[24] VCCDSW_EN_R
[17,22,24,39,68] SIO_SLP_S3_N
[24] RUN_ON_EC
[24] RUNPWROK
[24] EC_TOUCH_SCREEN_EN
[18] PCH_TOUCH_SCREEN_EN
[4] 3.3V_CAM_EN_N
[51] 1D2V_S3_PG
[17,46] PCH_PWROK
[17,24,39] ALL_SYS_PWRGD
[54] PWR_VNN_EN
[54] PWR_1D05V_EN
[7,17] VCCST_OVERRIDE
[24,53] S5_PG
[50] VCCIN_AUX_PWRGD
[54] PWR_VNN1D05V_PG
[22,53] CORE_VID0_1P8
[22,53] CORE_VID1_1P8
[53] PWR_1D8V_EN
[17,24,39] PM_SLP_SUS_N

3D3V_S5_PCH/3D3V_LAN

823mA
520us
164mA
074.02898.0093
2nd = 074.05209.0093
3rd = 074.07110.0093
4th = 074.07107.0003

5V_S0/3D3V_S0

2200mA
3742 mA
074.02898.0093
2nd = 074.05209.0093
3rd = 074.07110.0093
4th = 074.07107.0003

RUN_ON_R

073.7SZ08.000G
2nd = 73.01G08.L04
3rd = 73.01G08.IHG

RUNPWROK

75.27002.F7G
2nd = 075.27002.0E7C
3rd = 075.67002.007C

1D8V_S0

190mA
074.05027.0B93
2nd = 074.05201.0A93

5V_TSP_S0/3D3V_CAMERA_S0

125mA
242mA
069.41501.0061
2nd = 69.41001.131
074.02898.0093
2nd = 074.05209.0093
3rd = 074.07110.0093
4th = 074.07107.0003

VCC1P05_PROC

970mA
084.03426.0031
2nd = 084.01012.0031
75.00054.A7D
2nd = 75.00054.0B7D
3rd = 75.00054.17D
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31
074.05027.0B93
2nd = 074.05201.0A93
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

1D05V_VCCST_EN

(1.05V)
VCCST_OVERRIDE
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F
073.74132.0A0G
2nd = 073.7SZ32.0A0G
3rd = 73.7SZ32.CAH

1D8V_EN

3D3V_WLAN/3D3V_S5_WWAN

800mA
close PIN 72,74
close PIN 2,4
1200mA
074.02898.0093
2nd = 074.05209.0093
3rd = 074.07110.0093
4th = 074.07107.0003
Place near WWAN CONN

RF_CAP

NON_BYPASS
BYPASS

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Title: Sequence (Power Plane Enable)
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Title: ***Sequence (RSVD) (DS3/S0ix)***

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Title

INT IO (RSVD)

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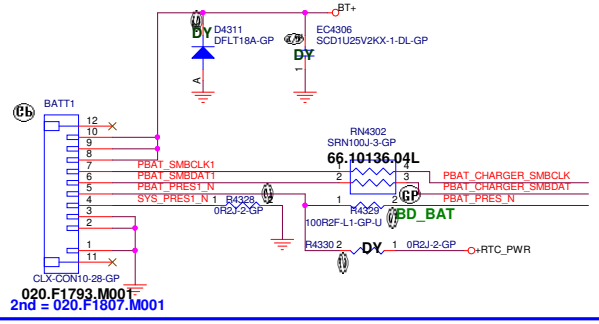
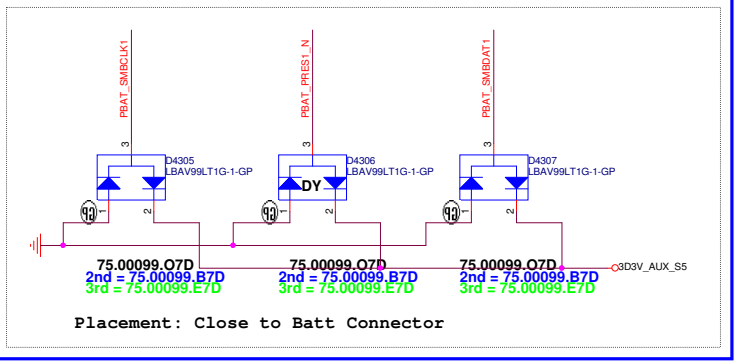
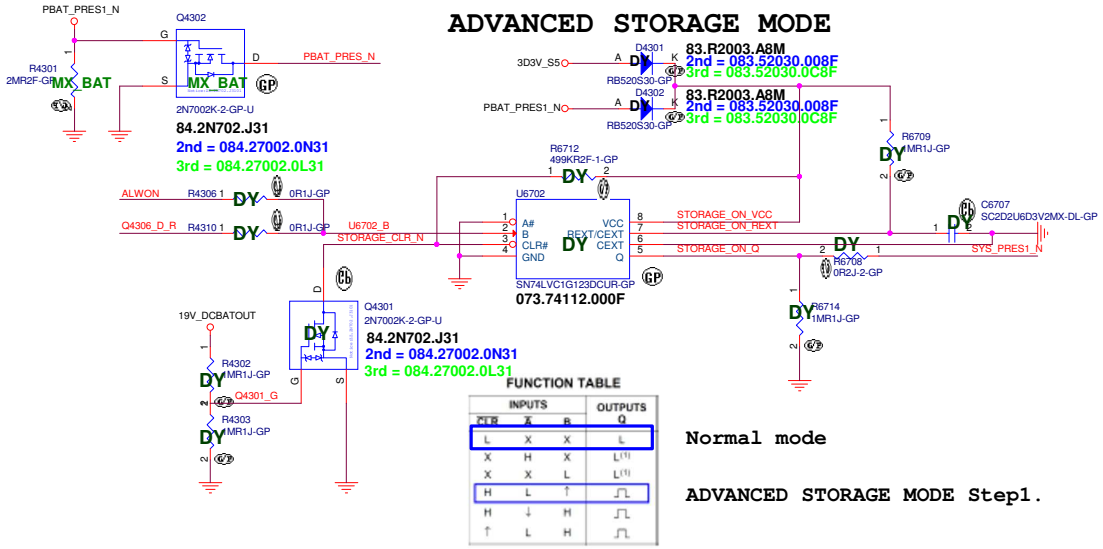
Main Func = BATT Com

Batt Connecter



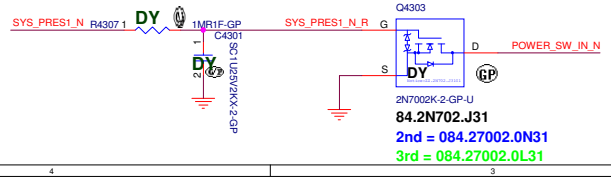


ADVANCED STORAGE MODE

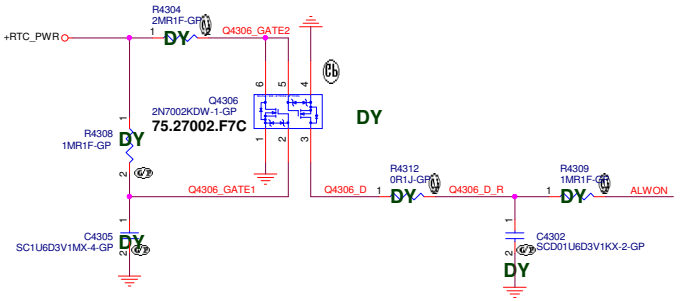


Normal mode

ADVANCED STORAGE MODE Step1.



Press power button duration time improvement



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Main Func = Power_Charger

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[24,43,98] PBAT_CHARGER_SMBDAT — PC4411 0R2J-2-GP — PWR_CHG_DATA
[24,43,98] PBAT_CHARGER_SMBCLK — PC4412 0R2J-2-GP — PWR_CHG_CLK
[24] I_ADP — PR4440 0R1J-GP — PWR_CHG_AMON
[24] I_BATT_R — PR4419 0R1J-GP
[24,46] I_SYS_R — PR4418 0R1J-GP — PWR_CHG_PMON
[3,22,72] PROCHOT_PD_R_N — PR4446 0R1J-GP — PWR_CHG_PROCHOT_RR_N
[24,43] PBAT_PRES_N — PR4447 0R1J-GP — PWR_PBAT_PRES_N
BD_BAT
[24,64] ACAV_IN — PR4448 0R1J-GP — PWR_ACAV_IN
[17] AC_DIS_ACP
[24,74] VBUS1_ECOK_R

[79,85] PWR_VGA_NVDDS_EN
[76,85,86] PWR_VGA_NVDDS_PG

Vcore_OVP

LOW NOISE CAP

Acoustic
PC4402 T598J225M-GP — 077.C6861.0011
2nd = 077.C6861.0021

Charger

	PR4461	PC4430	PR4447	EC token "SUPPORT_3VLDO_AS_BATTPRES"
Coin cell battery	DY	Stuff	Stuff	Disable
Battery internal LDO	Stuff	DY	DY	Enable

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

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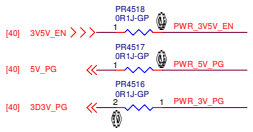
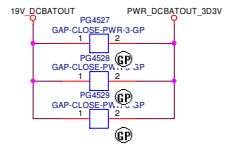
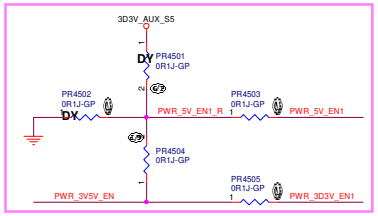
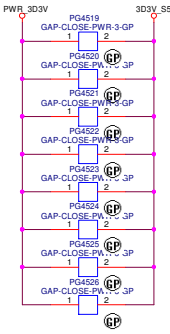


Main Func = Power_System 5V/3D3V







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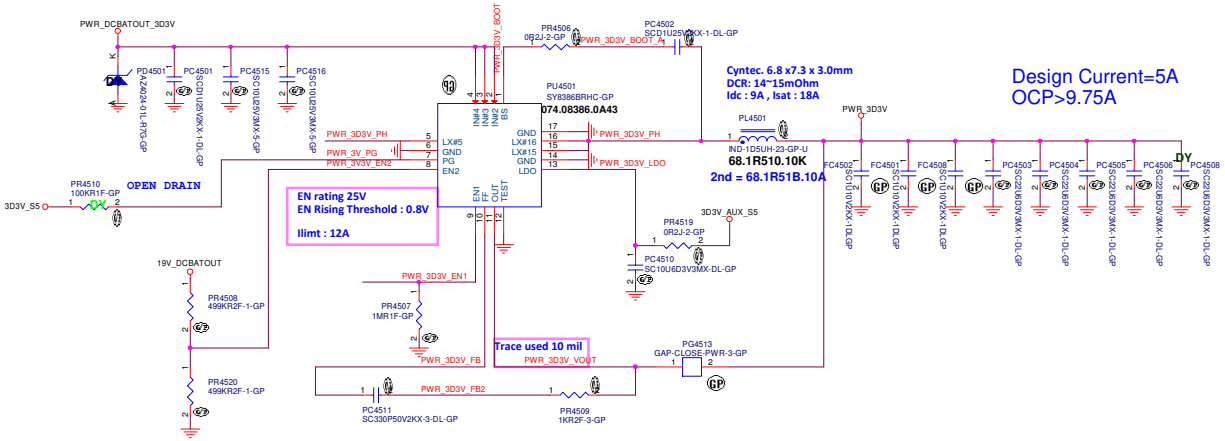

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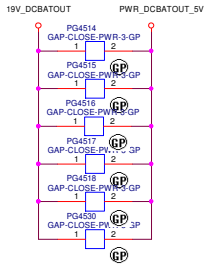
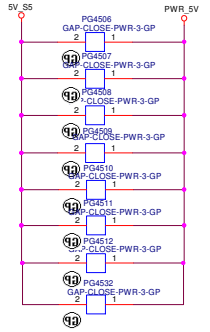
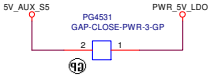
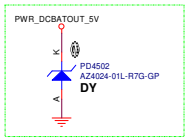
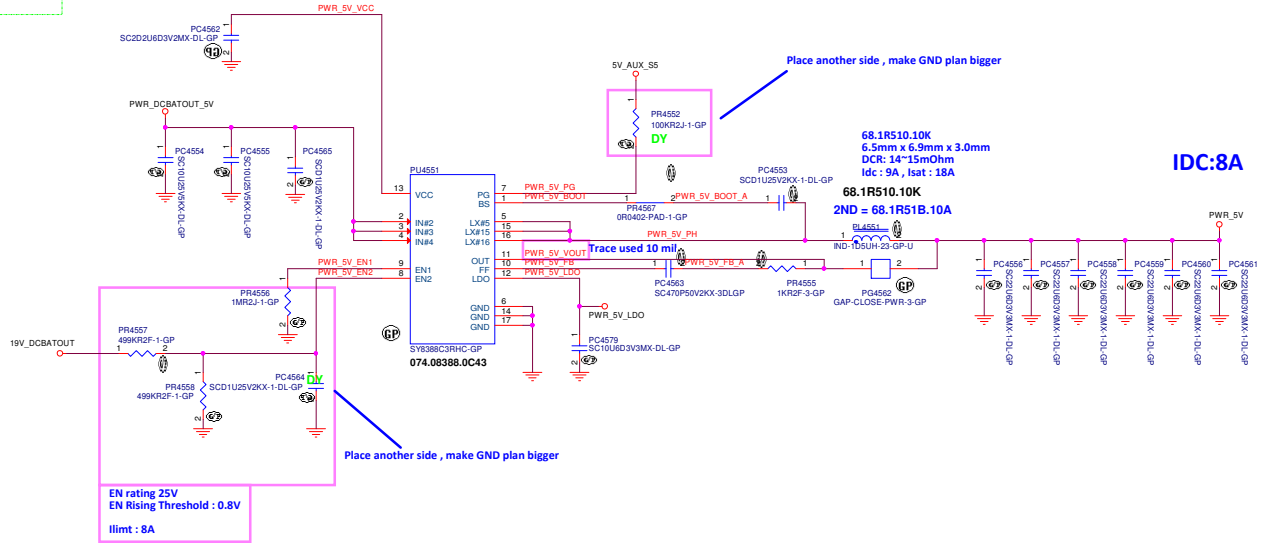








SY8388C For 5V



<Core Design>

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Title: 5V/3D3V

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Main Func = CPU.CorePower

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[24] VR_EN — PR4619 1 0R1J-GP — PWR_VCORE_VR_EN
[17,40] PCH_PWROK — PR4617 1 0R1J-GP — PWR_VCORE_VR_READY
[3,22,24] PROCHOT_CPU_N — PR4614 1 0R1J-GP — PWR_VCCIN_VRHOT_N
[24,44] I_SYS_R — PR4652 1 0R1J-GP — PWR_VCCIN_PSYS

PWM
[47] PWR_VCCCORE_PWM1
[47] PWR_VCCCORE_PWM2
[48] PWR_VCCGT_PWM6

CS
[47] PWR_VCCCORE_CS1
[47] PWR_VCCCORE_CS2
[48] PWR_VCCGT_CS6

[47,48] PWR_VCCIN_VTEMP
[47] PWR_VCCCORE_SYNC
[48] PWR_VCCGT_SYNC
[50] PWR_VCCIN_AUX_IMON

VCCCORE SENSE
[7] VCCCORE_SENSE
[7] VSSCORE_SENSE

VCCGT SENSE
[8] VCCGT_SENSE
[8] VSSGT_SENSE

SMBUS
[24,66,98] USH_EXP_HDMI_PS_SMBCLK — PR4616 0R1J-GP — PWR_VCCIN_SCL_P
[24,66] USH_EXP_HDMI_PS_SMBDAT — PR4633 0R1J-GP — PWR_VCCIN_SDA_P

SVID
1D05V_VCCST — PR4618 — PR4630 — PR4695 — PC4606 SCD01U10V1KX-3-GP
PR4618 100R1F-GP; PR4630 100R1F-GP; PR4695 453R1F-GP
[7,39] SVID_CLK_CPU — 0R2J-2-GP PR4630 — PWR_VCCIN_SCLK
[7] SVID_ALERT_CPU_N — 0R2J-2-GP PR4631 — PWR_VCCIN_ALT_N
[7] SVID_DATA_CPU — 0R2J-2-GP PR4632 — PWR_VCCIN_SDIO

VCCCORE SENSE 1D6V_CPU_CORE
PH/PL at EE Side.
PR4638 100R1F-GP
VCCCORE_SENSE — PR4636 0R1J-GP — PWR_VCCIN_VOSENA
VSSCORE_SENSE — PR4637 0R1J-GP — PWR_VCCIN_VORTNA
PR4639 100R1F-GP

VCCGT SENSE 1D5V_VCCGT
PH/PL at EE Side.
PR4642 100R1F-GP
VCCGT_SENSE — PR4640 0R1J-GP — PWR_VCCIN_VOSENB
VSSGT_SENSE — PR4641 0R1J-GP — PWR_VCCIN_VORTNB
PR4643 100R1F-GP

CHECK EE
PULL HIGH AT EE SIDE
3D3V_S0 — PR4645 1 10KR1J-GP — PWR_VCORE_VR_READY
3D3V_S5 — PR4632 1 DY 10KR1J-GP — PWR_VCCIN_SCL_P
PR4644 1 DY 10KR1J-GP — PWR_VCCIN_SDA_P
PR4646 1 DY 10KR1J-GP — PWR_VCORE_VR_EN
1D05V_VCCST — PR4647 1 DY 10KR1J-GP — PWR_VCCIN_VRHOT_N

	U15	U28
PR4607	1.13k (64.11315.6DL)	909R (64.90905.6DL)
PU4601	074.02964.M009	074.02964.M010

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PWR_VCCIN_VFBA_C — PC4616 2 DY 1 SC1U25V2KX-4-GP — PR4650 DY 10KR2F-2-GP
PR4607 1K13R2F-1-GP — U15
PWR_VCCIN_VFBB_C — PC4617 2 DY 1 SC1U25V2KX-4-GP — PR4651 DY 10KR2F-2-GP
PR4613 1K27R2F-L-GP — PWR_VCCIN_VDIFFB
PWR_VCCIN_VDD18 — PR4634 2 DY 1 0R1J-GP — PWR_VCCIN_CSSUMA
1KR2F-3-GP 1 PR4625 — PWR_VCCIN_CSSUMB
PWR_VCCIN_VDD18 — PR4612 DY 0R1J-GP — PWR_VCCIN_CSSUMB
19V_DCBATOUT — PR4601 2MR1F-GP; PR4624 133KR1F-GP; PC4607 SCD01U10V1KX-4-GP

PU4601 (074.02964.M009, MP2964GQKT-1501-Z-GP, U15)
VDIFFB, VORTNA, VOSENA, VFBA, VDIFFA, CS1, CS2, CS3, CS4, NC#3, NC#2, NC#1
VFBB, VOSENB, VORTNB, CSSUMA, CSSUMB, IMONA, IMONB, AUX_IMON, VDD18, SCLK, SDIO, ALT#, THERMAL_PAD
CS5, CS6, VIN_SEN, PSYS, TEMP, VDD33, PWM1, PWM2, PWM3, PWM4, ADDR, NC#37
VRRDY, VRHOT#, SDA_P, SCL_P, VID_STRAP, STBB, STBA, PE, EN, PWM6, PWM5, NC#36

PWR_VCCIN_VFBB — PR4651 DY 10KR2F-2-GP
PWR_VCCIN_AUX_IMON_R — PR4615 7K15R2B-GP — PC4615 GP SC680P50V2KX-2DLGP — PR4653 124R2F-U-GP
PC4603 SC1U25V2KX-4-GP — PWR_VCCIN_VDD18
PWR_VCCIN_SCLK
PWR_VCCIN_SDIO
PWR_VCCIN_ALT_N
PWR_VCCGT_CS6 — 1KR2F-3-GP PR4610
PWR_VCCIN_VINSEN
PC4604 SC2200P50V2KK-2DLGP — PWR_VCCIN_PSYS
PWR_VCCIN_VTEMP
PR4609 4D7R3F-L-GP — 3D3V_S5 — PWR_VCCIN_VDD33
PC4601 SC4D7U6D3V2MX-1-GP — PWR_VCCCORE_PWM1
PWR_VCCCORE_PWM2
PR4654 0R1J-GP — PWR_VCCIN_VDD18 — PWR_VCCIN_ADDR
PR4655 0R1J-GP
PWR_VCORE_VR_READY
PWR_VCCIN_VRHOT_N
TP4601 — PWR_VCCIN_SDA_P
TP4602 — PWR_VCCIN_SCL_P
PWR_VCCIN_VIDSTRAP
PWR_VCCGT_PWM6
PWR_VCORE_VR_EN
PWR_VCCIN_PE
PR4635 DY 0R2J-2-GP

TEMP
PWR_VCCIN_VTEMP — PC4608 SC1U25V2KX-4-GP — PR4631 49K9R1F-GP

PE
3D3V_S5 — PR4622 DY 10KR2F-2-GP — PWR_VCCIN_PE — PC4612 DY SCD01U25V1KX-3-GP — PR4649 0R2J-2-GP

STRAP
3D3V_S5 — PR4626 10KR2F-2-GP — PWR_VCCIN_VIDSTRAP — PC4602 DY SCD01U25V1KX-3-GP — PR4648 DY 10KR2F-2-GP

IMONA
PR4611 36KR2J-GP — PWR_VCCIN_IMONA — PR4627 2K74R2F-GP — PWR_VCCIN_IMONA_C
PC4609 SC560P50V2KX-2DLGP

IMONB
PR4608 56K2R2F-2-GP — PWR_VCCIN_IMONB — PR4621 10K5R2F-GP — PWR_VCCIN_IMONB_C
PC4610 SC330P50V2KX-3-DL-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPUCORE(1/3))
Size: A2 | Document Number | Rev: SB
Date: Friday, May 21, 2021 | Sheet 46 of 106

Main Func = CPU.CorePower

OFFPAGE

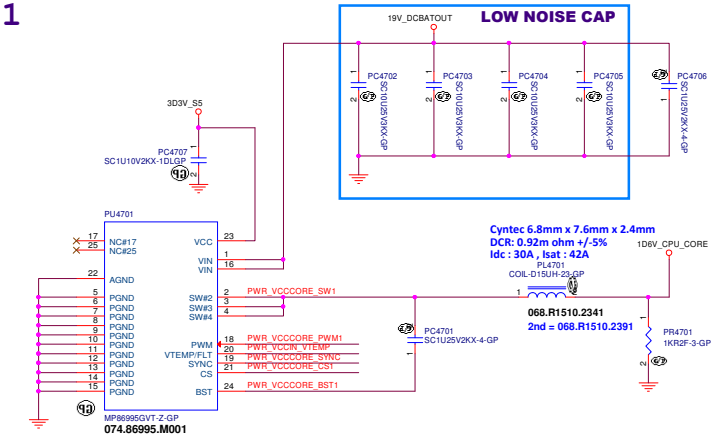
[46] PWR_VCCCORE_PWM1
[46] PWR_VCCCORE_PWM2

[46] PWR_VCCCORE_CS1
[46] PWR_VCCCORE_CS2

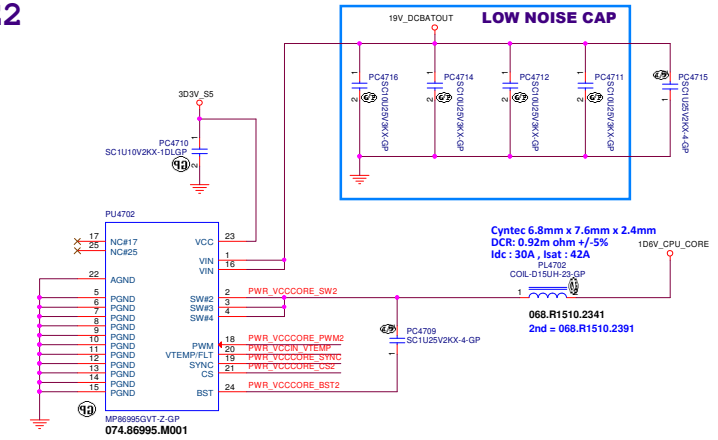
[46] PWR_VCCCORE_SYNC
[46,48] PWR_VCCIN_VTEMP

MP86995 For VCCCORE (Placement Only)

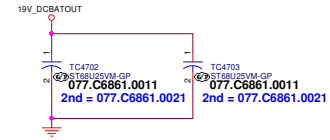
PHASE1



PHASE2



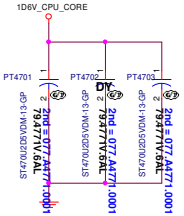
Acoustic



TDC = 47A
Iccmax = 80A

OUTPUT

ESR : 4.5 mohms
Rated Voltage(V.DC) : 2.5V



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CPUCORE(2/3)	
Size A2	Document Number SouthPeak15 MLK	Rev SB
Date: Friday, May 21, 2021	Sheet 47 of 106	

Main Func = CPU.CorePower

OFFPAGE

[46] PWR_VCCGT_PWM6

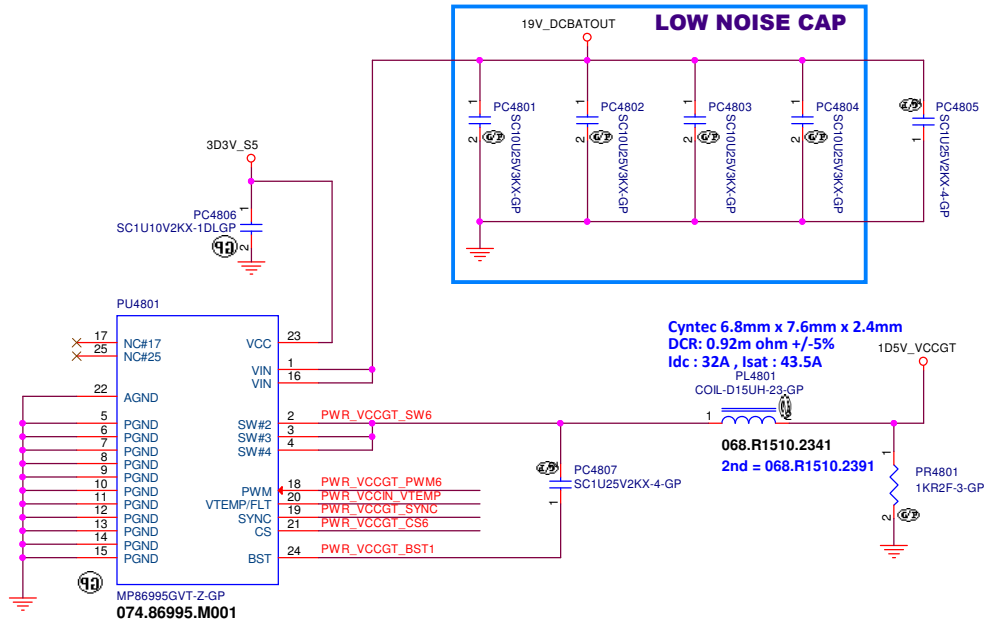
[46] PWR_VCCGT_CS6

[46] PWR_VCCGT_SYNC

[46,47] PWR_VCCIN_VTEMP

MP86995 For VCCCORE (Placement Only)

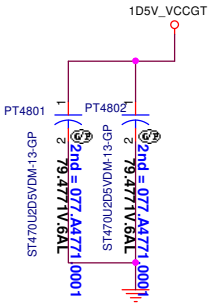
PHASE1



TDC = 23A
Iccmax = 40A

OUTPUT

ESR : 4.5 mohms
Rated Voltage(V.DC) : 2.5V



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER	
Size A3	Document Number SouthPeak13 ADL-P	Rev SB
Date: Friday, May 21, 2021	Sheet 48 of 106	

<Core Design>

Wistron Corporation
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Title

NCP81210MN_CPU_VCCGTUS

Size	Document Number	Rev
A4		SB

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VID

[22,40] CORE_VID0_1P8 — PR5002 0R2F-1-GP — PWR_VCCIN_AUX_VID0

[22,40] CORE_VID1_1P8 — PR5003 0R2F-1-GP — PWR_VCCIN_AUX_VID1

[53] PWR_1D8V_PG — PR5004 0R2F-1-GP — PWR_VCCIN_AUX_EN_R

[40] VCCIN_AUX_PWRGD — PR5006 0R2F-1-GP — PWR_VCCIN_AUX_PG

VCCIN_AUX SENSE

[22] VCCINAUX_SENSE

[22] VSSINAUX_SENSE

PWR_1229

[46] PWR_VCCIN_AUX_IMON

MP2961
Fsw=1200kHz

PWR_VCCIN_AUX_3V3 — PR5001 100KR2F-L1-GP — PWR_VCCIN_AUX_PG

19V_DCBATOUT — Acoustic — TC5004 ST68U25VM-GP — 077.C6861.0011 — 2nd = 077.C6861.0021

19V_DCBATOUT, PWR_VCCIN_AUX_IN — PG5001 GAP-CLOSE-PWR-3-GP, PG5002 GAP-CLOSE-PWR-3-GP, PG5003 GAP-CLOSE-PWR-3-GP — PWR_1119

PWR_VCCIN_AUX_IN — LOW NOISE CAP — PC5009, PC5002, PC5003, PC5006 SCD10U25V3KX-GP

PC5005 SC1U10V2KX-1DLGP — PR5005 5D1R2F-GP — 3D3V_S5

PU5001 MP2961GL-Z-GP — 074.02961.M001

PWR_VCCIN_AUX_3V3, PWR_VCCIN_AUX_VID1, PWR_VCCIN_AUX_VIDA0, PWR_VCCIN_AUX_IMON, PWR_VCCIN_AUX_LL, PWR_VCCIN_AUX_EN_R, PWR_VCCIN_AUX_PG, PWR_VCCIN_AUX_MODE1, PWR_VCCIN_AUX_MODE2

PR5008 0R2F-1-GP, PR5009 0R2F-1-GP, PR5010 90K9R2F-GP

PWR_VCCIN_AUX_BST1, PWR_VCCIN_AUX_BST2, PWR_VCCIN_AUX_PHASE, PWR_VCCIN_AUX_VOUT, PWR_VCCIN_AUX_RGND

PC5001, PC5004 SCD22U25V3KX-DL-GP — PR6016 0R2J-2-GP — PR5015 0R2J-2-GP — PWR_1216

PL5001 COIL-D15UH-23-GP — 068.R1510.2341 — 2nd = 068.R1510.2391

Cyntec 6.8mm x 7.6mm x 2.4mm
DCR: 0.92m ohm +/-5%
Idc : 30A , Isat : 42A

1D8V_VCCIN_AUX

PT5001 — 2R5TPE470MAM1-GP — 2R5TPE470MAM1LD001

ESR : 4.5 mohms
Rated Voltage(V.DC) : 2.5V

VCCIN_AUX:
ICCMAX:32A
TDC:14A

PR5011 100R2F-L1-GP-U — 1D8V_VCCIN_AUX

PWR_VCCIN_AUX_VOUT — PR5012 0R2F-1-GP — VCCINAUX_SENSE

PC5010 SCD1U16V2JX-1-DL-GP — PWR_VCCIN_AUX_RGND — PR5013 0R2F-1-GP — VSSINAUX_SENSE

PR5014 100R2F-L1-GP-U

VID0	VID1	VCCIN_AUX
0	0	0.00V
0	1	1.10V
1	0	1.65V
1	1	1.80V

Interleaving	VID Down	PR4909
N	Slew down	0 ohm
Y	Slew down	90k ohm
Y	Decay	150k ohm
N	Decay	>230k ohm or float

Loadline	PR4911
1m ohm	0 ohm
1.5m ohm	90k ohm
2m ohm	150k ohm
2.5m ohm	>230k ohm or float

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power_VCCIN_AUX

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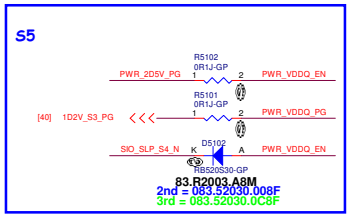
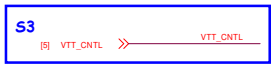
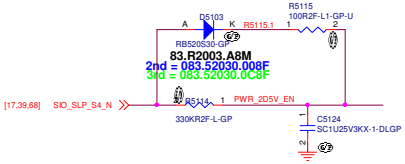
OFFPAGE







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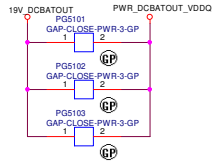
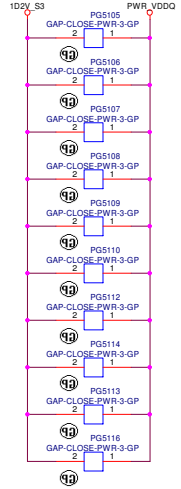
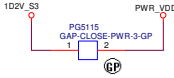
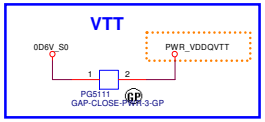
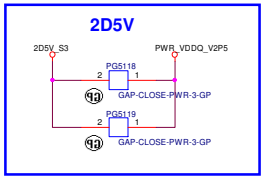
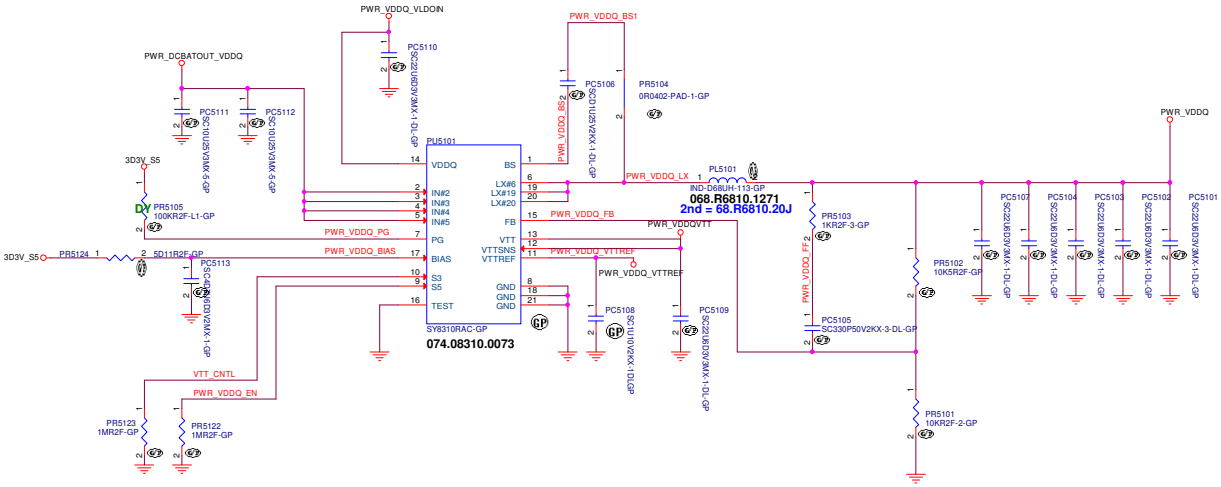








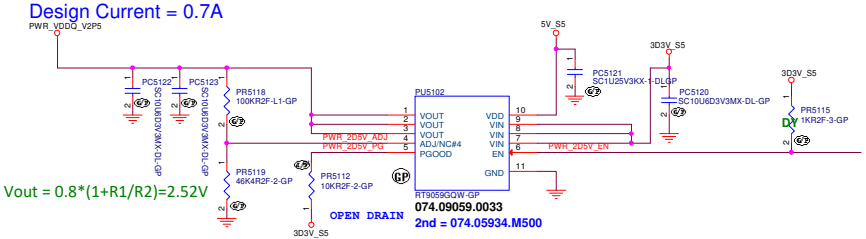




MAX:300
TPE:210

Design Current = 0.7A

RT9059GQW for 2D5V



Vout = 0.8*(1+R1/R2)=2.52V

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *SY8310_VDDQ/VTT*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

(Reserved)

Size	Document Number	Rev
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OFFPAGE-Signal

[24,40] S5_PG

[50] PWR_1D8V_PG

[40] PWR_1D8V_EN

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_1D8V
PG5302 GAP-CLOSE-PWR-3-GP
PG5303 GAP-CLOSE-PWR-3-GP

1D8V_S5 — PWR_1D8V
PG5311 GAP-CLOSE-PWR-3-GP
PG5310 GAP-CLOSE-PWR-3-GP
PG5307 GAP-CLOSE-PWR-3-GP
PG5308 GAP-CLOSE-PWR-3-GP
PG5309 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_1D8VCPU_VIN
PG5305 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_1D8V
PD5301 AZ4024-01L-R7G-GP
PC5301 SC1U25V3MX-5-GP
PC5302 SC1U25V3MX-5-GP
PC5313 SCD1U25V2KX-1DLGP
PU5301
PGOOD → PWR_1D8V_PG
BST → PWR_1D8V_BOOT → PR5303 0R0603-PAD-1-GP-U → PWR_1D8V_BOOT_A → PC5303 SCD1U25V2KX-1-DL-GP
SW#6 / SW#19 / SW#20 → PWR_1D8V_PH
PL5301 COIL-1UH-34-GP-U1
68.1R01A.20B
2nd = 68.1R01E.10C
Cyntec 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A
IDC:5A
PWR_1D8V
PC5304 PC5305 PC5306 PC5307 PC5308 SC22U6D3V3MX-1-DL-GP
PG5306 GAP-CLOSE-PWR-3-GP
PR5313 0R2J-2-GP
PWR_1D8V_FB_B
R1 PR5306 20KR1F-GP
DY PC5310 SC10P50V2JN-4DLGP
R2 PR5307 10KR1F-GP
Trace used 10 mil
FB ← PWR_1D8V_FB
AGND
MODE ← PWR_1D8V_MODE
PR5304 332KR1F-GP ← PWR_1D8V_VCC
PR5301 5K11R1F-GP
VIN ×4
NC#10
NC#16
VCC ← PWR_1D8V_VCC
PC5309 SC2D2U10V3KX-1DLGP-U
EN ← PWR_1D8V_EN
SS ← PWR_1D8V_SS
PR5305 1MR1F-GP
PC5311 SCD022U16V2KX-3DLGP
GND ×4
TPS51396RJER-GP
074.51396.0043
2nd = 074.51397.0A43
Vout = 0.6V x (1+ R1/R2)
= 0.6 x (1 + 20K/10K)
= 0.6 x 3 = 1.8 V
3D3V_S5
PR5302 100KR1F-GP
PR5311 0R2J-2-GP
S5_PG
PWR_1D8V_PG
Place another side , make GND plan bigger
PWR_1D8V_PH
PR5312 2D2R6J-3-GP
PWR_1D8V_SNB
PC5314 SC1500P50V2KX-2-DL-GP

Imax= 0.3A
PWR_1D8VCPU_VIN
PC5324 SC1U10V2KX-1DLGP
5V_S5
PC5325 SCD1U16V2KX-3DLGP
PU5302
VIN / GND / BIAS / GND
VOUT / ADJ/C / EN
PWR_1D8VCPU_ADJ
1D8V_CPU_EN_R
RT9081DGQZA-GP
074.09081.0033
DY
PC5322 SCD1U16V2KX-3DLGP
PR5310 12K7R2F-GP
PR5315 10KR2F-GP
PC5315 SC22P50V2JN-4GP
PR5314 100R2F-L1-GP-U
PC5323 SC2D2U6D3V2MX-DL-GP
PWR_1D8V_CPU
20200925 Power

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51396_1D8V		
Size: Custom	Document Number: SouthPeak15 MLK		Rev: SB
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PH on EE Side

VCCIN_AUX_PWRGD
[40] PWR_VNN_EN >> PWR_VNN_EN

[40] PWR_1D05V_EN >> PWR_1D05V_EN

PH on EE Side

1D05V_BYPASS_CTRL
[22] PWR_VNN1D05V_VID2 >>

PM_SLP_S3#
[22] PWR_VNN1D05V_VID1 >>

[40] PWR_VNN1D05V_PG <<<

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

OFFPAGE-GAP

1D05V_VNN_BYPASS — R5499 1 2 D01R2J-L-GP BYPASS — PWR_VNN

1D05V_S5_BYPASS — R5498 1 2 D01R2J-L-GP BYPASS — PWR_1D05V

3D3V_S5 — 100KR1J-GP PR5420 BYPASS — PWR_VNN1D05V_PG

PU5401 APW8743CQBI-TRG-GP
074.08743.0A73

Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A
PL5401 IND-1UH-382-GP
068.1R010.1131
2nd = 068.1R010.1281
3rd = 068.1R010.1D41

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A
PL5402 IND-10UH-330-GP
68.1001S.10K
2nd = 068.10010.1A41

PR5426 10KR1F-GP PWR_VNN1D05V_VID1
PR5427 10KR1F-GP PWR_VNN1D05V_VID2
PR5433 10KR1F-GP
PR5428 10KR1F-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APW8738_ByPASS
Size: A3 | Document Number: SouthPeak15 MLK | Rev: SB
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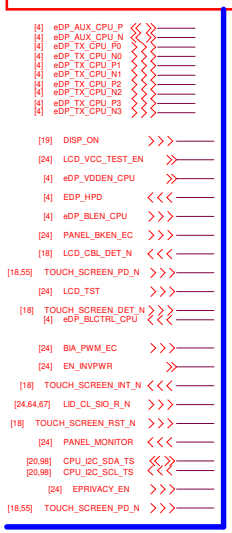
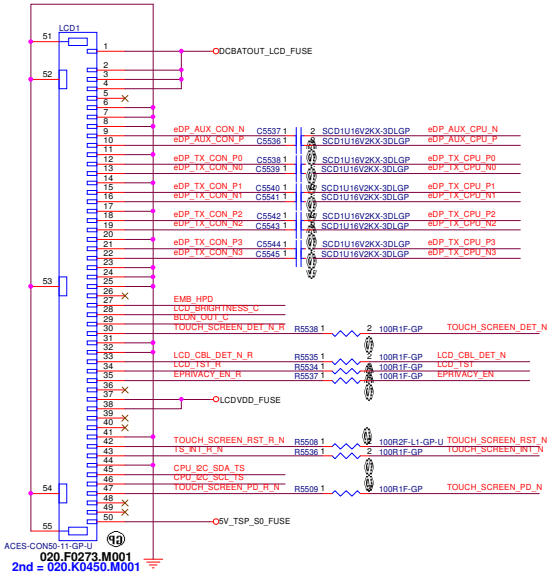
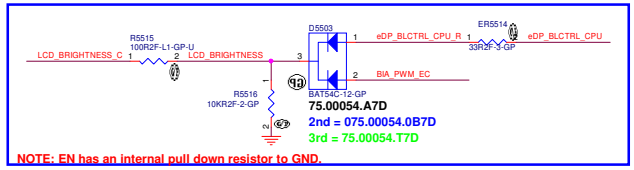
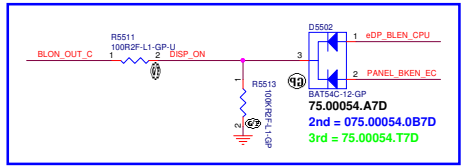
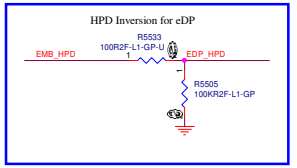
Main Func = LCD/Touch





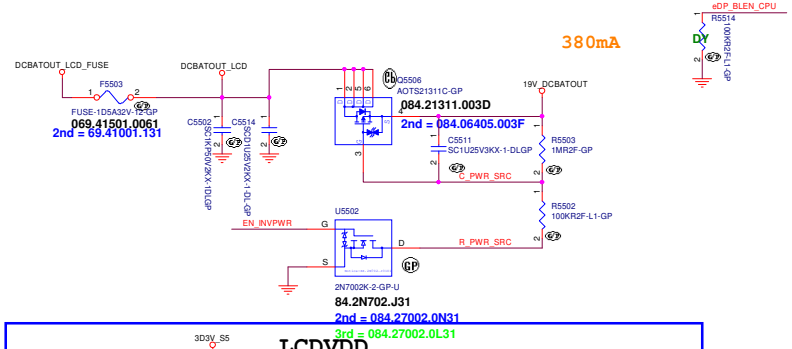


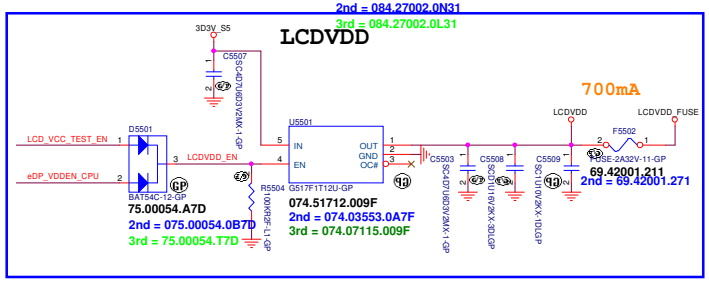


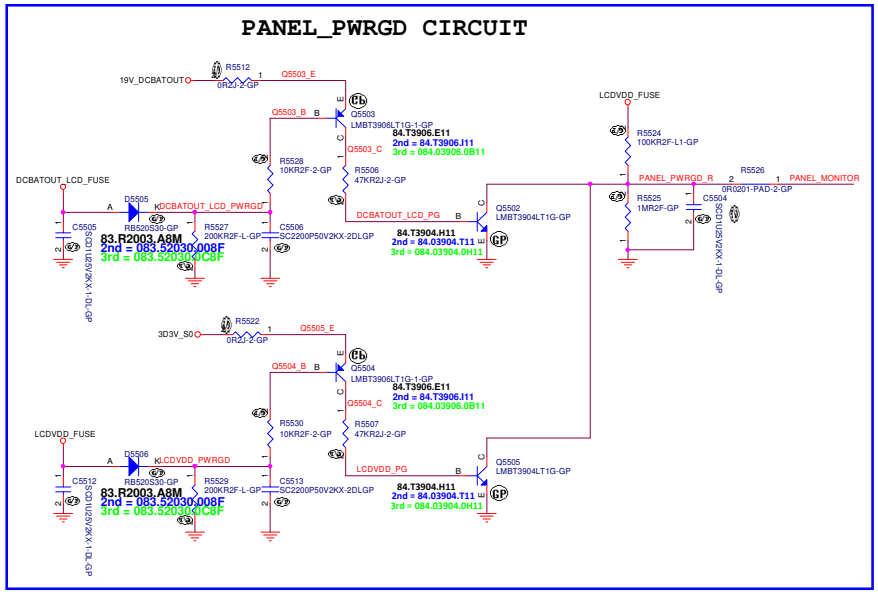


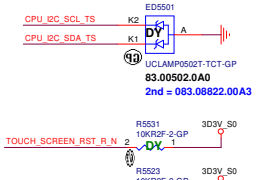
https://vinafix.com

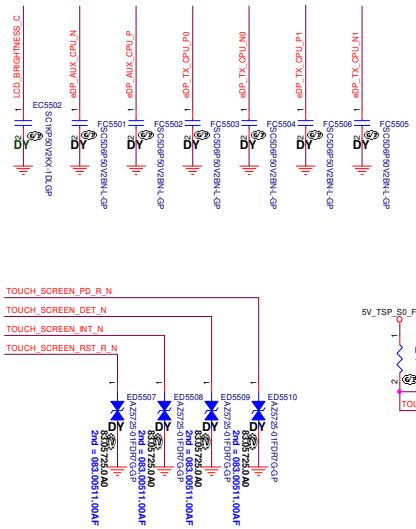
INVERTER POWER

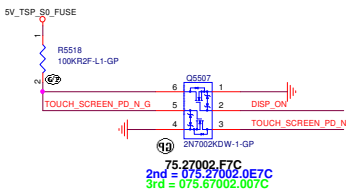












<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display (LCD/Inverter)**

Size	Document Number	Rev
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Main Func = IR CAM

CAM_MIC_CBL_DET_N (GPP_F14)	IR_CAM_DET_N (GPP_E15)	P_DET_N (GPP_D2)	MODULE_DET_N (GPP_H20)	USB camera detected during	Module Detection
0	1	0	0	Y	101 IR+FHD (IR_CAM_DET_N(GPP_E15)=1)
0	0	0	0	Y	EMZA IR+FHD (P_DET_N(GPP_D2)=0)
0	0	1	0	Y	IR+FHD (IR_CAM_DET_N(GPP_E15)=0)
0	1	1	0	Y	RGB (IR_CAM_DET_N=1,MIC_DET=1,USB camera detected)
0	1	1	0	N	Mic (IR_CAM_DET_N=1,MIC_DET=1,USB camera not detected)
0	1	1	1	N	Cable (CAM_MIC_CBL_DET_N=0)
1	1	1	1	N	No cable (CAM_MIC_CBL_DET_N=1)

[16] CCD_USB20_N
[16] CCD_USB20_P
[27] DMIC_SDA_CODEC
[27] DMIC_SCL_CODEC
[18] IR_CAM_DET_N
[18] CAM_MIC_CBL_DET_N
[20,98] WA_SCL
[20,98] WA_SDA
[18] P_SENSOR_DET_1P8_N
[20] ISH_ALS_INT_RF_1P8_N
[18] SECURE_BIO
[3] ISH_P_SENSOR_INT_1P8_N
[24] IR_CAM_EN
[21] MODULE_DET_N
[24] VIDEO_MUTE

187mA
DCBATOUT_IRCAM
CIR1
STM-CON30-6-GP
020.F1027.0030
2nd = 020.F1428.0030
242mA

IR_CAM_DET_R_N — R5606 100R1F-GP — IR_CAM_DET_N
MODULE_DET_R_N — R5619 100R1F-GP — MODULE_DET_N
CAM_MIC_CBL_DET_N_R — R5610 100R1F-GP — CAM_MIC_CBL_DET_N
P_DET_R_N — R5609 100R1F-GP — P_SENSOR_DET_1P8_N
SECURE_BIO_R — R5601 100R1F-GP — SECURE_BIO
WA_INT — WE1_PWR — R5611 100R1F-GP — ISH_P_SENSOR_INT_1P8_N
WA_SCL
WA_SDA
ALS_INT — ALS_PWR — R5604 100R1F-GP — ISH_ALS_INT_RF_1P8_N
VIDEO_MUTE
DMIC_SCL_CODEC_CON
DMIC_SDA_CODEC_CON
DMIC_PWR
3D3V_CAMERA_S0_FUSE

1D8V_S0 — R5612 100KR2J-1-GP — P_SENSOR_DET_1P8_N
3D3V_S0 — R5618 100KR2J-1-GP — MODULE_DET_N

DMIC_SDA_CODEC_CON — R5607 BLM15AG121SN-1GP — DMIC_SDA_CODEC
68.00084.921
2nd = 68.00217.401
DMIC_SCL_CODEC_CON — R5608 BLM15AG121SN-1GP — DMIC_SCL_CODEC
68.00084.921
2nd = 68.00217.401
C5604 DY SC2P50V1JN-1-GP
C5605 DY SC2P50V1JN-1-GP

DMIC_PWR — R5603 DY 0R2J-2-GP — 3D3V_CAMERA_S0_FUSE
3D3V_S0 — F5602 FUSE-1D5A32V-T2-GP
069.41501.0061
2nd = 69.41001.131

ALS_PWR — F5603 FUSE-1D5A32V-T2-GP
069.41501.0061
2nd = 69.41001.131

WE1_PWR — F5604 FUSE-1D5A32V-T2-GP — 3D3V_S0
069.41501.0061
2nd = 69.41001.131

ED5601 AZC099-04S-2-GP
IR_CAM_DET_R_N — I/O1
CAM_MIC_CBL_DET_N — I/O2
GND
DY VDD
I/O3 — CCD_USB20_CON_N
I/O4 — CCD_USB20_CON_P
ED5601_VDD — TP5601 TPAD14-OP-GP
075.09904.0A7C
2nd = 075.53456.000C

CCD_USB20_P — EL5601 DLM0NSN900HY2D-GP — CCD_USB20_CON_P
CCD_USB20_N — CCD_USB20_CON_N
068.09002.2001
2nd = 68.02002.061

DMIC_PWR — DY ED5603 AZ5123-01F-R7G-GP-U
83.05123.AA0
DCBATOUT_IRCAM — DY ED5602 AZ4024-01H-R7G-GP
083.04024.00A1

DCBATOUT_IRCAM — F5601 FUSE-2A32V-11-GP
69.42001.211
2nd = 69.42001.271
DCBATOUT_IRCAM_FUSE — C5602 DY SC1P50V2KX-1DLGP — C5601 SCD1U25V2KX-1-DL-GP
R5617 1KR2F-3-GP
IR_CAM_PER_BLEED
Q5603 2N7002K-2-GP-U
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31
IR_CAM_EN_N

Q5601 AOTS21311C-GP
084.21311.003D
2nd = 084.06405.003F
19V_DCBATOUT
C5603 SC1U25V3KX-1-DLGP
IR_CAM_PWR_FET_GATE
R5613 1MR2F-GP
R5614 100KR2F-L1-GP

IR_CAM_EN — R5616 0R2J-2-GP — IR_CAM_EN_R
R5615 100KR2F-L1-GP
Q5602 2N7002K-2-GP-U
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31
IR_CAM_EN_N

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Inverter)
Size: A3
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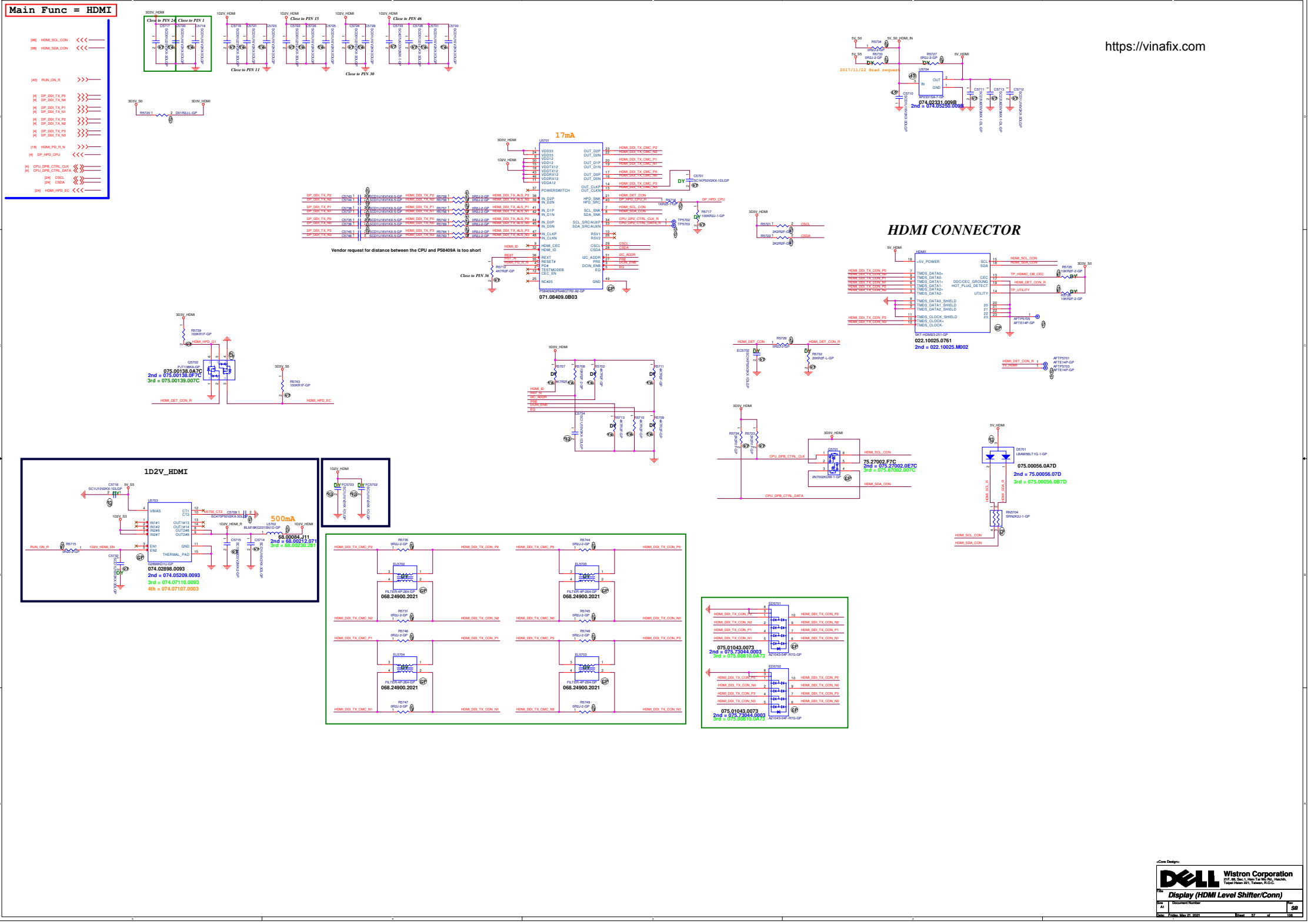
Main Func = HDMI



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display (RSVD) DP***

Size	Document Number	Rev
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Date: Friday, May 21, 2021 Sheet 58 of 106

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Display (RSVD) DVI

Size	Document Number	Rev
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Date: Friday, May 21, 2021 Sheet 59 of 106

<Core Design>

Wistron Corporation
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Title

INT IO (RSVD)(HDD)

Size	Document Number	Rev
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Main Func = WLAN

WLAN

[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P
[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P

BT

[16] BT_USB20_N
[16] BT_USB20_P

CNVi

[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP
[21] CNV_BRI_RSP
[15,21] CNV_RGI_DT
[15,21] CNV_BRI_DT
[21] CNV_RGI_RSP
[21] CNV_RF_RESET_1P8_N
[24] CNV_DET_N

WLAN

[18] WLAN_CLK_CPU_P
[18] WLAN_CLK_CPU_N
[18] CLKREQ_PCIE1_N
[24,62,63] PCIE_WAKE_R_N
[21,62] CNV_COEX3_1P8
[20,62] CNV_COEX2_1P8
[20,62] CNV_COEX1_1P8
[18] CL_CLK
[18] CL_DATA
[18] CL_RST_N
[21] CLKREQ_CNV
[24] WLAN_WIGIG60GHZ_DIS_N
[24] EC_BT_RADIO_DIS_N
[18,39] SUSCLK
7,33,62,63,76,91,97,99] PCH_PLTRST_RIGHT_N
[18] CNVI_EN_N
[19] PCH_BT_RADIO_DIS_N

R6111 0R2J-2-GP
EL6101
DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
R6113 0R2J-2-GP
BT_USB20_P
BT_USB20_N
BT_USB20_CON_P
BT_USB20_CON_N

1D8V_S5
R6143 20KR2F-L-GP
CNV_RGI_RSP
R6144 20KR2F-L-GP
CNV_BRI_RSP
R6145 20KR2F-L-GP
CNV_BRI_DT

D6102 RB520S30-GP
WLAN_WIGIG60GHZ_DIS_N
WLAN_WIGIG60GHZ_DIS_N_R
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

D6105 RB520S30-GP
PCH_BT_RADIO_DIS_N
BT_RADIO_DIS_N
R6114 0R1J-GP
BT_RADIO_DIS_N_R
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

D6104 RB520S30-GP
EC_BT_RADIO_DIS_N
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

CLKREQ_CNV
R6103 75KR2F-GP

3D3V_S5_PCH
R6120 100KR2F-L1-GP
CNVI_EN_N
R6125 0R1J-GP
CNV_RF_RESET_WLAN_N_R
R6119 0R2J-2-GP
CNV_DET_N
R6128 75KR2F-GP
U6102 PJA138KA-GP
084.00138.0A31
2nd = 084.00139.0A31
CNV_RF_RESET_WLAN_N
R6118 0R2J-2-GP
CNV_RF_RESET_1P8_N
R6102 75KR2F-GP
1090mA

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3D3V_S5_WLAN
R6126 10KR2F-2-GP
R6127 10KR2F-2-GP
RN6101 SRN100KJ-6-GP
WLAN_WIGIG60GHZ_DIS_N_R
BT_RADIO_DIS_N_R
EC_BT_RADIO_DIS_N
PCH_BT_RADIO_DIS_N

WLAN1
NGFF_KEY_E_75P
SKT-MINI75P-6-GP
062.10007.0051
2nd = 062.10007.0061
3rd = 062.10007.0401

WLAN_PCIE_TX_P
WLAN_PCIE_TX_N
C6115 SCD1U16V2KX-3DLGP
C6102 SCD1U16V2KX-3DLGP
WLAN_PCIE_TX_CON_P
WLAN_PCIE_TX_CON_N
WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
CLKREQ_PCIE1_N
WLAN_WAKE_N
PCIE_WAKE_R_N
R6110 0R2J-2-GP
CNV_WT_DN1
CNV_WT_DP1
CNV_WT_DN0
CNV_WT_DP0
CNV_WT_CLKN
CNV_WT_CLKP

BT_USB20_CON_P
BT_USB20_CON_N
CNV_WR_DN1
CNV_WR_DP1
CNV_WR_DN0
CNV_WR_DP0
CNV_WR_CLKN
CNV_WR_CLKP

3D3V_S5_WLAN
CNV_RF_RESET_WLAN_N
CLKREQ_CNV
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
CNV_BRI_DT
CL_RST_N
CL_DATA
CL_CLK
R6132 0R2J-2-GP CNV_COEX3_1P8
R6133 0R2J-2-GP CNV_COEX2_1P8
R6134 0R2J-2-GP CNV_COEX1_1P8
R6135 33R2F-3-GP SUSCLK
R6136 0R2J-2-GP PCH_PLTRST_RIGHT_N
BT_RADIO_DIS_N_R
WLAN_WIGIG60GHZ_DIS_N_R
PULSAR_38P4M_REFCLK_WLAN
R6121 10KR2F-2-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2)
Size: A3
Document Number:
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Main Func = WWAN

NGFF(WWAN/SSD)

To use GPIO as PEWAKE without SPDT ,unstuff R6241 ,R6243 and stuff R6242 or simply un stuff the SPDT.

2500mA

SKT-NGFF75P-167-GP
062.10003.0B71
2nd = 062.10003.0661
3rd = 062.10003.0671

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN--USB3.1, PCIe Gen1	0

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN--USB3.1, PCIe Gen1	0

Figure 3-5 Timing Control for Start-up

Index	Minimum	Typical	Notes
t_{pr}	-	-	+3.3V power supply rises time. If power supply always ready, there is no t_{pr}
t_{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t_{on2}	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#

Figure 3-6 Software control power off timing

Index	Minimum	Typical	Maxim	Notes
t_{pd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t_{pd}
t_{off1}	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_OFF#
t_{off2}	0ms	30ms	t_{off1}	PERST# should asserted after RESET#

SKT-SIM6-33-GP-U
062.10008.0281

Reverse type

84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

Layout Close to SIM1 Connector

<Core Design>

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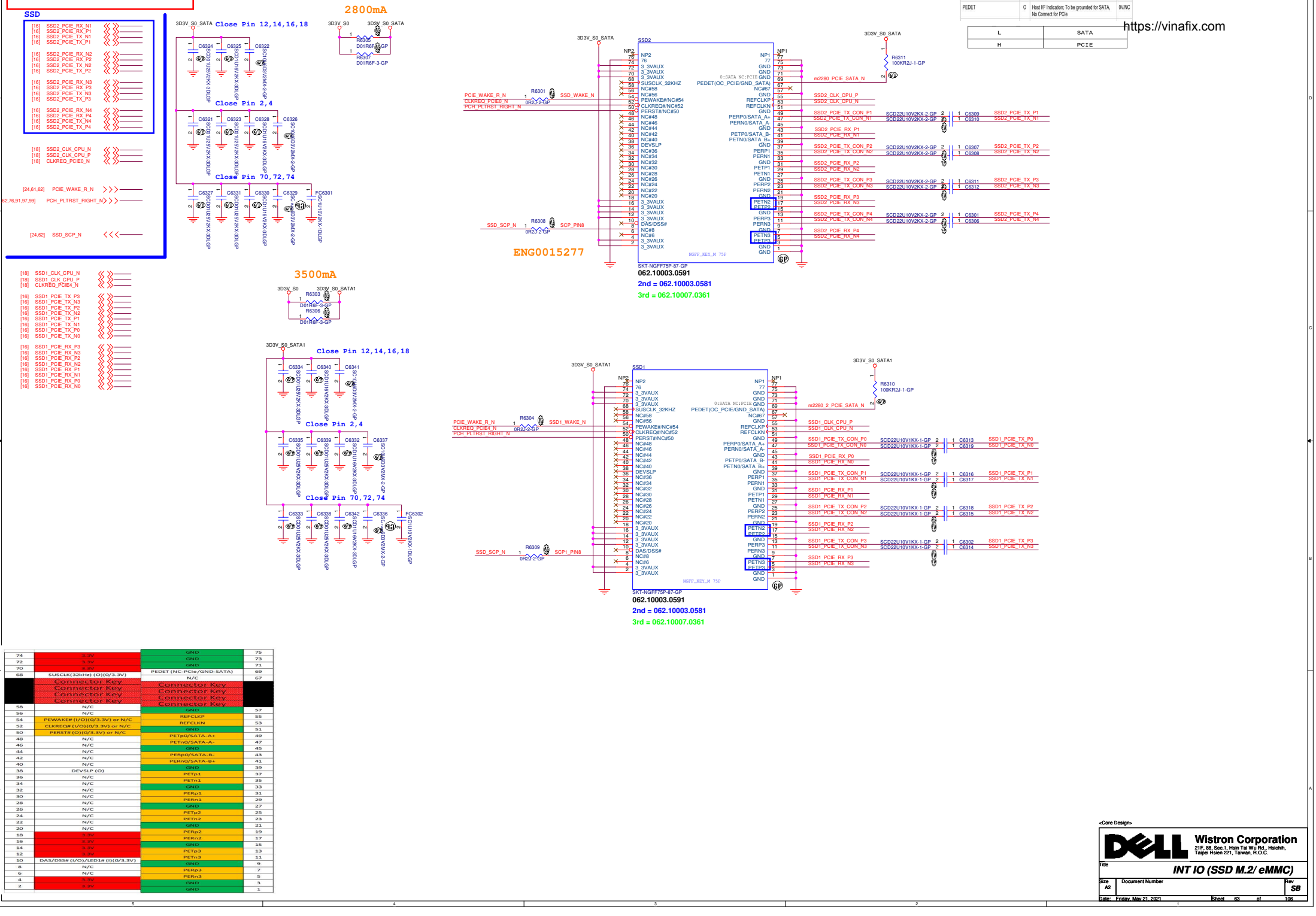
Title: INT IO WWAN

Size: A2 | Document Number | Rev: SB

Date: Friday, May 21, 2021 | Sheet 62 of 106

Main Func = m.2 SSD



74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	N/C	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C		
56	N/C	GND	57
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKP	55
52	CLKREQ# (I/O)(0/3.3V) or N/C	REFCLKN	53
50	PERST# (O)(0/3.3V) or N/C	GND	51
48	N/C	PETp0/SATA-A+	49
46	N/C	PETn0/SATA-A-	47
44	N/C	GND	45
42	N/C	PERp0/SATA-B-	43
40	N/C	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	N/C	PETp1	37
34	N/C	PETn1	35
32	N/C	GND	33
30	N/C	PERp1	31
28	N/C	PERn1	29
26	N/C	GND	27
24	N/C	PETp2	25
22	N/C	PETn2	23
20	N/C	GND	21
18	3.3V	PERp2	19
16	3.3V	PERn2	17
14	3.3V	GND	15
12	3.3V	PETp3	13
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	PETn3	11
8	N/C	GND	9
6	N/C	PERp3	7
4	3.3V	PERn3	5
2	3.3V	GND	1

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2/ eMMC)

Size	Document Number	Rev
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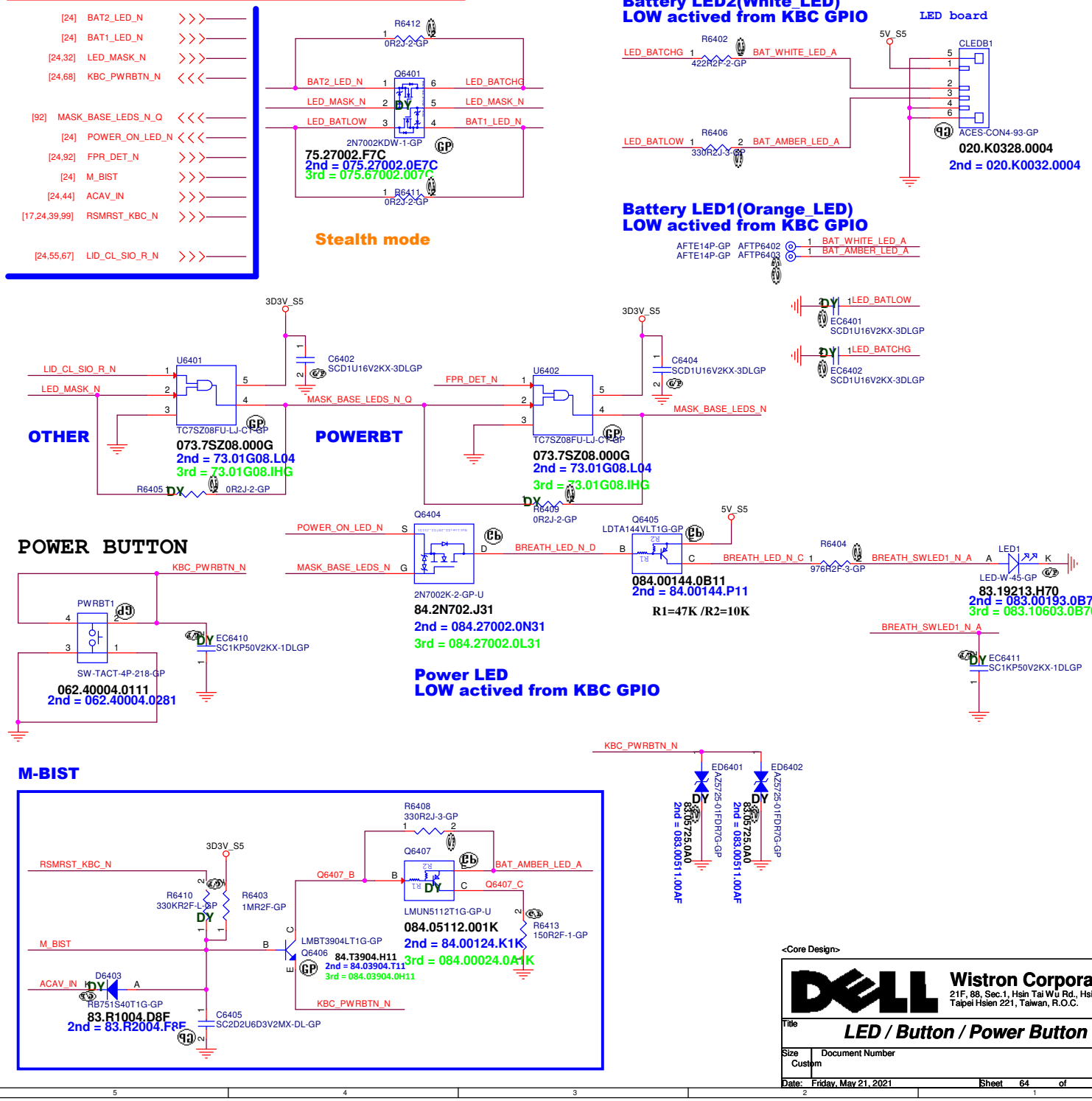
Main Func = LED/HALL/Button



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button

Size	Document Number	Rev
Custom		SB

Date: Friday, May 21, 2021 Sheet 64 of 106

Main Func = Key Board/Touch Pad

10mA

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[4] KB_DET_N

[24] BC_INT_ECE1117_N
[24] BC_DAT_ECE1117
[24] BC_CLK_ECE1117
[3,24] PCH_TOUCHPAD_INTR_N

[24] CLK_TP_SIO_I2C_DAT
[24] DAT_TP_SIO_I2C_CLK

[20] CPU_I2C_SDA_TP
[20] CPU_I2C_SCL_TP

[24] PTP_DISABLE_N

[98] I2C1_SCK_TP_R
[98] I2C1_SDA_TP_R

3D3V_TP
R6518
100KR2F-L1-GP
PTP_DISABLE_N

3D3V_S0
3D3V_TP
R6511 1 2 D01R2J-L-GP

TPAD1
21
1 KO_2
2 KI_3
3
4 EC_KO2
5
6 BC_INT_ECE1117_N
7
8 BC_CLK_ECE1117
9 BC_DAT_ECE1117
10
11 EC_KI3
12
13 PCH_TOUCHPAD_INTR_N
14 I2C1_SDA_TP_R
15
16 I2C1_SCK_TP_R
17 PTP_DISABLE_N
18 KB_DET_N
19
20
22
ACES-CON20-48-GP

R6502 1 2 0R0201-PAD-GP
3D3V_S5
R6501 1 2 0R0201-PAD-GP
5V_S0
3D3V_TP

020.K0440.M001
2nd = 020.K0442.M001

3D3V_TP
AFTP6501
AFTE14P-GP

3D3V_S0
R6520
100KR2F-L1-GP
PCH_TOUCHPAD_INTR_N

3D3V_TP
3D3V_S5
5V_S0
C6503 SCD1U25V2KX-1-DL-GP
C6504 SCD1U25V2KX-1-DL-GP
C6505 SCD1U25V2KX-1-DL-GP
EC6502 SC1KP50V2KX-1DLGP
KB_DET_N

DAT_TP_SIO_I2C_CLK
CLK_TP_SIO_I2C_DAT
C6506 SC10P50V2JN-4DLGP
C6507 SC10P50V2JN-4DLGP

PCH_TOUCHPAD_INTR_N
I2C1_SDA_TP_R
I2C1_SCK_TP_R
EC6503 SC1KP50V2KX-1DLGP
EC6504 SC1KP50V2KX-1DLGP
EC6505 SC1KP50V2KX-1DLGP

3D3V_TP
R6505 2K2R2F-GP
R6506 2K2R2F-GP
R6513 0R2J-2-GP CLK_TP_SIO_I2C_DAT
R6512 0R2J-2-GP DAT_TP_SIO_I2C_CLK
R6503 0R2J-2-GP I2C1_SDA_TP_R CPU_I2C_SDA_TP
R6504 0R2J-2-GP I2C1_SCK_TP_R CPU_I2C_SCL_TP

<Core Design>

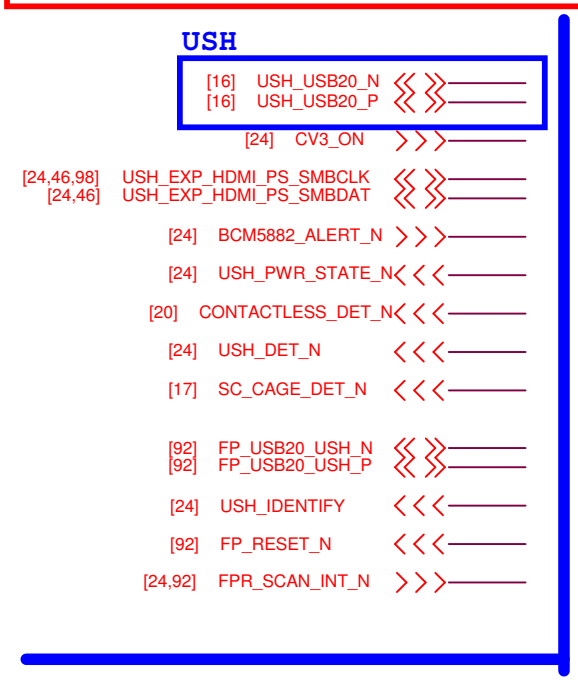
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)

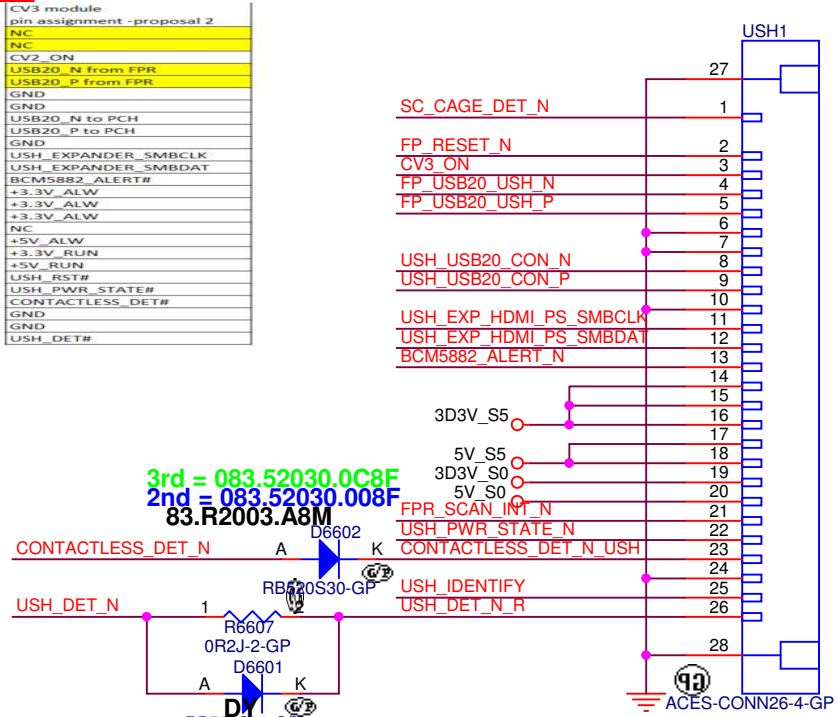
Size	Document Number	Rev
A4		SB

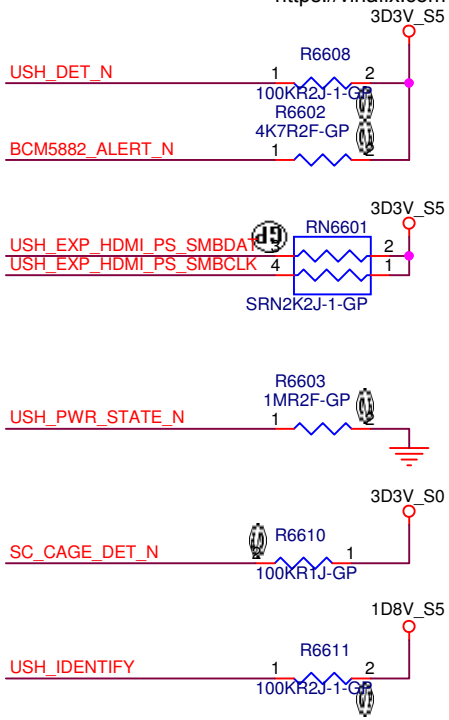
Date: Friday, May 21, 2021 Sheet 65 of 106

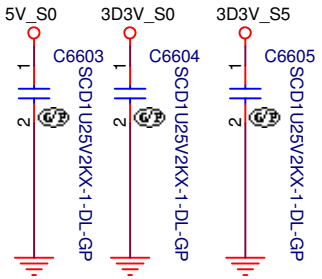
Main Func = USH BD

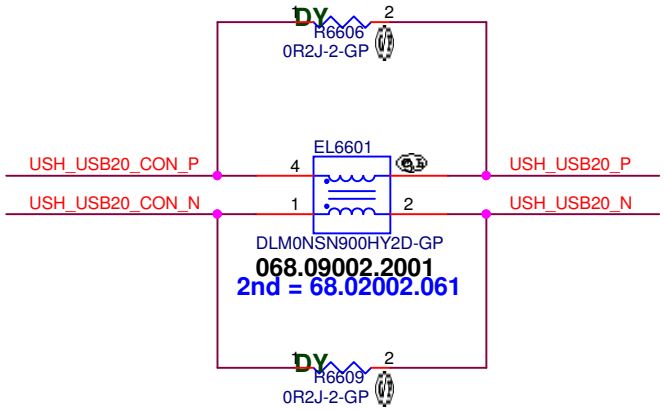


CV3 module
pin assignment -proposal 2
NC
NC
CV2_ON
USB20_N from FPR
USB20_P from FPR
GND
GND
USB20_N to PCH
USB20_P to PCH
GND
USH_EXPANDER_SMBCLK
USH_EXPANDER_SMBDAT
BCM5882_ALERT#
+3.3V_ALW
+3.3V_ALW
+3.3V_ALW
NC
+5V_ALW
+3.3V_RUN
+5V_RUN
USH_RST#
USH_PWR_STATE#
CONTACTLESS_DET#
GND
GND
USH_DET#









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

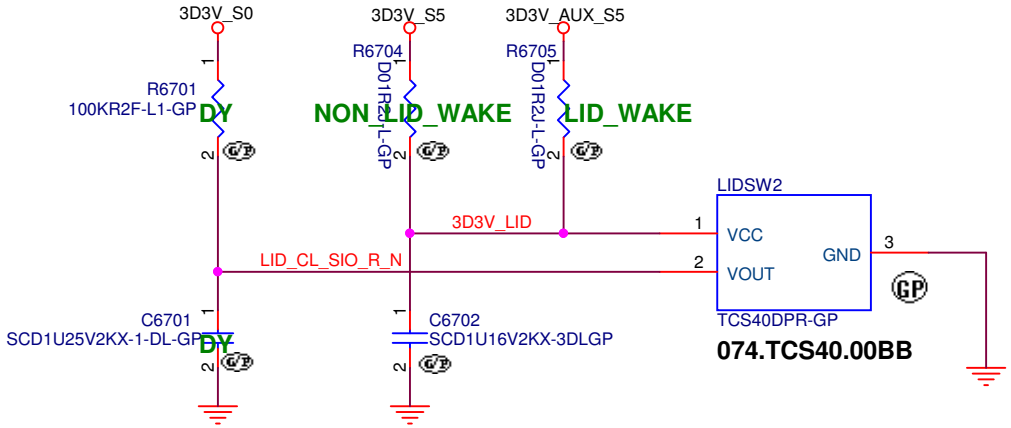
Title: *IO Board Conn (USH)*

Size	Document Number	Rev
A4		SB

Date: Friday, May 21, 2021 Sheet 66 of 106

Main Func = Sensor (Hall-Sensor)

[24,55,64] LID_CL_SIO_R_N



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (Hall-Sensor)***

Size	Document Number	Rev
A4		SB

Date: Friday, May 21, 2021 Sheet 67 of 106

Main Func = Debug

Firmware SW

R6819 0R2J-2-GP DY — ME_FWP_PCH — ME_FWP

Install after MP

R6820 1KR2F-3-GP MP_DY — 3D3V_S5_PCH

MESW1 SW-SLIDE3P-36-GP 062.40006.0151

ME_FWP_PCH	A	B
	Low	High
	Normal Operation (Default)	Override

ESPI DEBUG (Wistron)

ESPI2 ACES-CON14-11-GP 20.F1637.014

ESPI_CLK, ESPI_RESET_N, ESPI_CS_N, ESPI_IO3, ESPI_IO2, ESPI_IO1, ESPI_IO0, ESPI_DEBUG_PWR, DEBUG_TX, SBIOS_TX, SBIOS_RX

R6818 0R2J-2-GP DEBUG — 3D3V_S0 — HOST_DEBUG_TX

R6817 0R2J-2-GP DEBUG

ESPI DEBUG (DELL)

ESPI1 ACES-CON10-60-GP-U 020.K0156.0010

3D3V_S0

ESPI_IO0, ESPI_IO1, ESPI_IO2, ESPI_IO3, ESPI_CS_N, ESPI_RESET_R_N, ESPI_CLK

R6823 0R1J-GP DEBUG — ESPI_RESET_N

APS DEBUG

APS1 HDR-ETY-CON18-2-GP 20.K0493.018

3D3V_S5_PCH, SIO_SLP_S3_N, SIO_SLP_S5_N, SIO_SLP_S4_N, SIO_SLP_A_N, RTC_RST_N, SYS_RESET_N, SIO_SLP_S0_N

KBC_PWRBTN_N — R6824 0R1J-GP DEBUG — KBC_PWRBTN_R_N

DEBUG

SPI DEBUG

R1

52mA

3D3V_S5_PCH — D6801 — 3D3V_SPI

MP_DY SDM1L20CSP-7 083.01307.0080

58mA

MP change to short pad

JTAG

3D3V_S5

R6821 49D9R2F-GP — RN6801 SRN10KJ-5-GP — RN6802 SRN10KJ-5-GP — R6803 100KR2J-1-GP — R6807 10KR2F-GP

JTAG1 ACES-CON10-28-GP-U 20.K0460.010

JTAG_PU, JTAG_TDI, JTAG_TMS, JTAG_CLK, JTAG_TDO, MSCLK, MSDATA, HOST_DEBUG_TX_C, UART0_TXD_R

R6802 0R2J-2-GP DEBUG — HOST_DEBUG_TX

R6816 0R2J-2-GP DEBUG

MSCLK — R6822 10KR2F-2-GP

145mA

3D3V_SPI — D6803 — 3D3V_DUDC — MP_DY — SBA0520Q-R1-00001-GP-U 083.00520.0F8F

C6803 SCD1U16V2KX-DLGP — C6802 SCD1U16V2KX-DLGP

3D3V_DUDC_MUX — D6805 — MP_DY — SBA0520Q-R1-00001-GP-U 083.00520.0F8F

3D3V_AUX_S5 — D6804 — MP_DY — SBA0520Q-R1-00001-GP-U 083.00520.0F8F

DUDC1 ACES-CON10-60-GP-U 020.K0156.0010

FN_SELECT, PWR_BTN_L_SPI_D3, EC_DEBUG_VCC_SPI_D2, JTAG_TMS_EC_TX_SPI_CS0_N, JTAG_TDO_EC_RX_SPI_CLK, JTAG_TDI_BIOS_RX_SPI_D1, JTAG_TCK_BIOS_TX_SPI_D0, LID_CTL_SPI_CS1_N

3D3V_DUDC_MUX — C6804 SCD1U16V2KX-3DLGP — MP_DY

U6802 TS5A23157DGSR-GP 74.23157.A99

FN_SELECT, LID_CTL_SPI_CS1_N

SPI_CS_DEBUG_N1_R — R6847 22D6R1F-GP — SPI_CS_CPU_N1

LID_CL_SIO — R6846 22D6R1F-GP — LID_CL_SIO_N

FUNCTION TABLE

INPUT IN	NC TO COM COM TO NC	NO TO COM COM TO NO
L	ON	OFF
H	OFF	ON

3D3V_DUDC_MUX — C6801 SCD1U16V2KX-3DLGP — MP_DY

U6801 TS3A27518ERTWR-GP 073.32751.0A03

DUDC_EN_N, FN_SELECT

JTAG_TMS_EC_TX_SPI_CS0_N — R6831 22D6R1F-GP — SPI_CS_CPU_N0

JTAG_TMS_DUDC — R6832 22D6R1F-GP — JTAG_TMS

JTAG_TCK_BIOS_TX_SPI_D0 — SPI_SI_DEBUG_DUDC — R6833 22D6R1F-GP — SPI_SI_CPU

JTAG_CLK_DUDC — R6834 22D6R1F-GP — JTAG_CLK

EC_DEBUG_VCC_SPI_D2 — SPI_WP_DEBUG_DUDC — R6835 22D6R1F-GP — SPI_WP_CPU

EC_DEBUG_VCC

JTAG_TDO_EC_RX_SPI_CLK — SPI_CLK_DEBUG_DUDC — R6836 22D6R1F-GP — SPI_CLK_CPU

JTAG_TDO_DUDC — R6837 22D6R1F-GP — JTAG_TDO

JTAG_TDI_BIOS_RX_SPI_D1 — SPI_SO_DEBUG_DUDC — R6838 22D6R1F-GP — SPI_SO_CPU

JTAG_TDI_DUDC — R6839 22D6R1F-GP — JTAG_TDI

PWR_BTN_L_SPI_D3 — SPI_HOLD_DEBUG_DUDC — R6840 22D6R1F-GP — SPI_HOLD_CPU

KBC_PWRBTN_N_DUDC — R6841 22D6R1F-GP — KBC_PWRBTN_N

3D3V_DUDC_MUX — R6850 0R1J-GP

R6842 22D6R1F-GP — HOST_DEBUG_TX

R6843 22D6R1F-GP — HOST_DEBUG_RX

R6844 22D6R1F-GP — SBIOS_RX

R6845 22D6R1F-GP — SBIOS_TX

JTAG_CLK — R6849 100R1F-GP DY

DUDC_EN_N — R6830 10KR1F-GP MP_DY

3D3V_DUDC_MUX — R6848 10KR1F-GP MP_DY — FN_SELECT

ARD R6819 is depopulated in Development and populated in shipping systems

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (LPC debug)

Size: Custom | Document Number | Rev: SB

Date: Friday, May 21, 2021 | Sheet 68 of 106

[19] ME_FWP_PCH
[24] ME_FWP

[17,22,24,39,40] SIO_SLP_S3_N
[17,39] SIO_SLP_S5_N
[17,39,51] SIO_SLP_S4_N
[17] SIO_SLP_A_N
[18,39] RTC_RST_N
[24,64] KBC_PWRBTN_N
[17] SYS_RESET_N
[17,91] SIO_SLP_S0_N

[18,24,98] ESPI_IO0
[18,24,98] ESPI_IO1
[18,24,98] ESPI_IO2
[18,24,98] ESPI_IO3
[18,24,98] ESPI_CS_N
[18,24,39] ESPI_RESET_N
[18,24,98] ESPI_CLK

[24] JTAG_TDI
[24] JTAG_TMS
[24] JTAG_CLK
[24] JTAG_TDO
[24] MSCLK
[24] MSDATA
[24] HOST_DEBUG_TX

[18,24,25,91] SPI_CLK_CPU
[15,18,24,25,91] SPI_SI_CPU
[18,24,25,91] SPI_SO_CPU
[15,18,24,25,99] SPI_WP_CPU
[15,18,24,25] SPI_HOLD_CPU
[18,24,25] SPI_CS_CPU_N0
[18,24,25] SPI_CS_CPU_N1

[25] FN_SELECT

[24] LID_CL_SIO_N

[20] SBIOS_TX
[20] SBIOS_RX

[24] HOST_DEBUG_RX

Main Func = Sensor (E-compass/A+Gyro/SAR)

[20] GSEN_INT1

[20,70,98] CPU_I2C_SCL_SENSOR
[20,70,98] CPU_I2C_SDA_SENSOR

3D3V_SEN_S0 — F6901 (1, 2) — 3D3V_S0

FUSE-D5A63V-1-GP
069.4R500.0091
2nd = 69.4R500.221

3D3V_SEN_S0

RN6901
CPU_I2C_SDA_SENSOR — 4
CPU_I2C_SCL_SENSOR — 3
1 — 3D3V_SEN_S0
2

SRN2K2J-1-GP

SENBD1
11 — 3D3V_SEN_S0
1
2
3
4
5
6 — CPU_I2C_SDA_SENSOR
7 — CPU_I2C_SCL_SENSOR
8 — GSEN_INT1
9
10
12

ACES-CON10[illegible]-GP
020.F1799.M001

ED6901
CPU_I2C_SDA_SENSOR — K2
CPU_I2C_SCL_SENSOR — K1
DY
A

UCLAMP0502T-TCT-GP
83.00502.0A0
2nd = 083.08822.00A3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Sensor (GYROSCOPE/PRESSUE/ALS)

Size	Document Number	Rev
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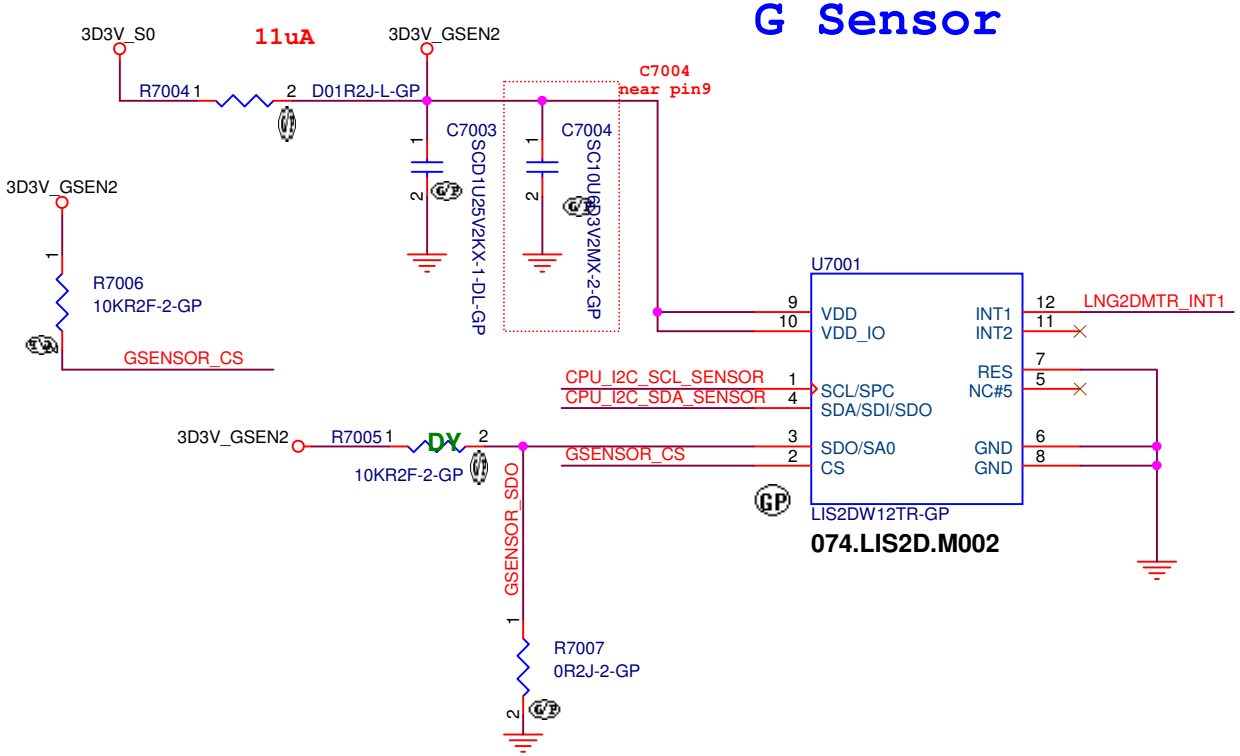
Main Func = G-sensor

[20,69,98] CPU_I2C_SDA_SENSOR
[20,69,98] CPU_I2C_SCL_SENSOR
[20] LNG2DMTR_INT1

G Sensor



<Core Design>

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Title: ***Sensor (G-sensor)***

Size	Document Number	Rev
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Main Func = TBT

USB1

TBT PORTS

MISC & DEBUG

POWER

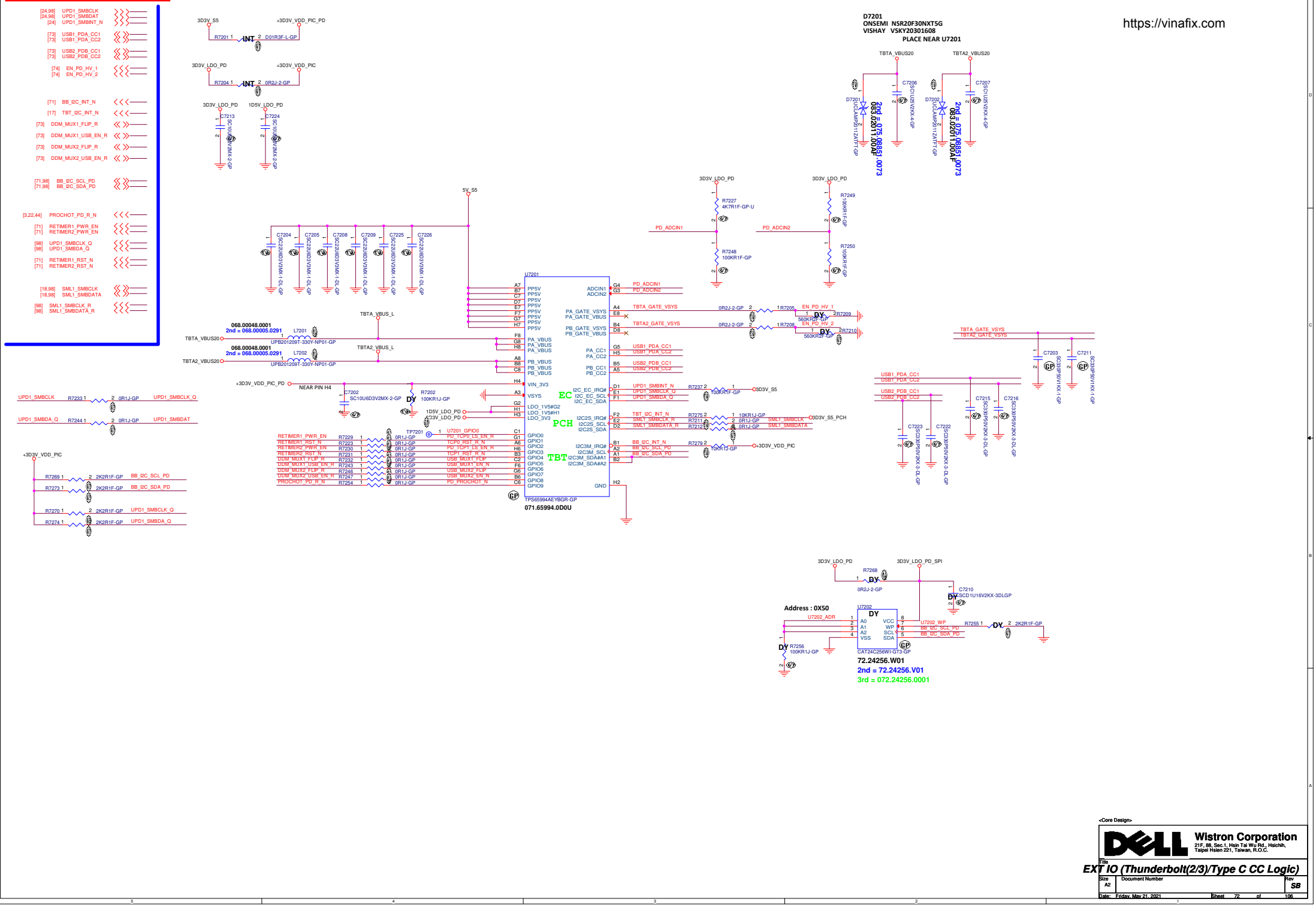
GND

Wistron Corporation

EXT IO (Thunderbolt(1/3)/Type C Re-driver)

SouthPeak15 MLK

Main Func = TypeC



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Title
EXT IO (Thunderbolt(2/3)/Type C CC Logic)

Size	Document Number	Rev
A2		SB

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Main Func = TypeC

USB1

[71] USB1_SSTX_CON_P0
[71] USB1_SSTX_CON_N0
[71] USB1_SSTX_CON_P1
[71] USB1_SSTX_CON_N1
[71] USB1_SSRX_CON_P0
[71] USB1_SSRX_CON_N0
[71] USB1_SSRX_CON_P1
[71] USB1_SSRX_CON_N1
[16] USB1_USB20_P
[16] USB1_USB20_N
[72] DDM_MUX1_FLIP_R
[72] USB1_PDA_CC1
[72] USB1_PDA_CC2
[24,71] USB1_CON_SBU1_R
[24,71] USB1_CON_SBU2_R
[72] DDM_MUX1_USB_EN_R

USB2

[71] USB2_SSTX_CON_P0
[71] USB2_SSTX_CON_N0
[71] USB2_SSTX_CON_P1
[71] USB2_SSTX_CON_N1
[71] USB2_SSRX_CON_P0
[71] USB2_SSRX_CON_N0
[71] USB2_SSRX_CON_P1
[71] USB2_SSRX_CON_N1
[16] USB2_USB20_P
[16] USB2_USB20_N
[72] DDM_MUX2_FLIP_R
[72] USB2_PDB_CC1
[72] USB2_PDB_CC2
[72] DDM_MUX2_USB_EN_R
[71] USB2_CON_SBU1_R
[71] USB2_CON_SBU2_R

3D3V_S5
3D3V_MUX1
3D3V_MUX2
3D3V_LDO_PD
TBTA_VBUS20
TBTA2_VBUS20

R7324 1 2 0_01R2J-L-GP
C7313 0.22U10V6K-2GP
DDM_MUX1_FLIP_R
DDM_MUX1_USB_EN_R
10KR1J-GP
100KR1J-GP
R7325 1 2 100KR1J-GP
3V

U7302 TS3USB221ARSER-GP-U
73.03221.E03
2nd = 073.03221.0A03
3rd = 073.03221.0003

U7304_VBIAS
U7304_FLT_N
R7341 2 DY 1 100KR1J-GP
U7304 TPD4S311YBFR-GP
DY

USB1_SSTX_CON_C_P0
USB1_SSTX_CON_C_N0
USB1_CON_CC1
USB1_USB20_CONT_P
USB1_USB20_CONT_N
USB1_CON_SBU1
USB1_SSRX_AR_C_N1
USB1_SSRX_AR_C_P1
USB1_SSTX_CON_C_P1
USB1_SSTX_CON_C_N1
USB1_CON_CC2
USB1_SSRX_AR_C_N0
USB1_SSRX_AR_C_P0
SKT-USB32-72-GP-U
062.10009.M064

Co-lay with U7304

USB1_CON_SBU1 R7305 1 2 0R1J-GP USB1_CON_SBU1_R
USB1_CON_SBU2 R7306 1 2 0R1J-GP USB1_CON_SBU2_R
USB1_CON_CC1 R7323 1 2 0R2J-2-GP USB1_PDA_CC1
USB1_CON_CC2 R7325 1 2 0R2J-2-GP USB1_PDA_CC2

R7302 0R2J-2-GP
R7301 0R2J-2-GP
EL7302 EL7301
DLW32SN900SQ2-GP
068.09002.2001
2nd = 68.02002.061
R7303 0R2J-2-GP
R7304 0R2J-2-GP

C7301 C7302 C7303 C7304
0.1U10V1MK-1-GP

USB1_SSTX_CON_P0 R7307 1 2 0R2R1J-GP USB1_SSTX_CON_R_P0 C7305 1 SCD22U25V1KK-1-GP USB1_SSTX_CON_C_P0
USB1_SSTX_CON_N0 R7316 1 2 0R2R1J-GP USB1_SSTX_CON_R_N0 C7306 1 SCD33U25V1KX-3-GP USB1_SSTX_CON_C_N0
USB1_SSRX_CON_P0 R7317 1 2 0R2R1J-GP USB1_SSRX_AR_R_P0 C7307 1 SCD33U25V1KX-3-GP USB1_SSRX_AR_C_P0
USB1_SSRX_CON_N0 R7318 1 2 0R2R1J-GP USB1_SSRX_AR_R_N0 C7308 1 SCD33U25V1KX-3-GP USB1_SSRX_AR_C_N0
USB1_SSTX_CON_P1 R7319 1 2 0R2R1J-GP USB1_SSTX_CON_R_P1 C7309 1 SCD22U25V1KK-1-GP USB1_SSTX_CON_C_P1
USB1_SSTX_CON_N1 R7320 1 2 0R2R1J-GP USB1_SSTX_CON_R_N1 C7310 1 SCD22U25V1KK-1-GP USB1_SSTX_CON_C_N1
USB1_SSRX_CON_P1 R7321 1 2 0R2R1J-GP USB1_SSRX_AR_R_P1 C7311 1 SCD33U25V1KX-3-GP USB1_SSRX_AR_C_P1
USB1_SSRX_CON_N1 R7321 1 2 0R2R1J-GP USB1_SSRX_AR_R_N1 C7312 1 SCD33U25V1KX-3-GP USB1_SSRX_AR_C_N1

ED7301 ED7302 ED7303 ED7304 ED7305 ED7306 ED7307 ED7308
ED7309 ED7310 ED7311 ED7312 ED7313 ED7314 ED7315 ED7316
083.5V0H1.00AF
2nd = 083.58017.00AF
3rd = 075.08315.0073

R7308 R7309 R7310 R7311 R7312 R7313 R7314 R7315
0R2J-2-GP

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R7346 1 2 0_01R2J-L-GP
C7325 0.22U10V6K-2GP
DDM_MUX2_FLIP_R
DDM_MUX2_USB_EN_R
10KR1J-GP
100KR1J-GP
R7328 2 DY 1 100KR1J-GP

U7303 TS3USB221ARSER-GP-U
73.03221.E03
2nd = 073.03221.0A03
3rd = 073.03221.0003

C7330 0.1U10V1MK-1-GP
C7329 0.1U10V1MK-1-GP
A 50-V, X7R capacitor is recommended
U7305_VBIAS
U7305_FLT_N
R7342 2 DY 1 100KR1J-GP
U7305 TPD4S311YBFR-GP
DY

USB2_SSTX_CON_C_P0
USB2_SSTX_CON_C_N0
USB2_CON_CC1
USB2_USB20_CONT_P
USB2_USB20_CONT_N
USB2_CON_SBU1
USB2_SSRX_AR_C_N1
USB2_SSRX_AR_C_P1
USB2_SSTX_CON_C_P1
USB2_SSTX_CON_C_N1
USB2_CON_CC2
USB2_SSRX_AR_C_N0
USB2_SSRX_AR_C_P0
SKT-USB32-72-GP-U
062.10009.M064

Co-lay with U7305

USB2_CON_SBU1 R7345 1 2 0R1J-GP USB2_CON_SBU1_R
USB2_CON_SBU2 R7352 1 2 0R1J-GP USB2_CON_SBU2_R
USB2_CON_CC1 R7326 1 2 0R2J-2-GP USB2_PDB_CC1
USB2_CON_CC2 R7350 1 2 0R2J-2-GP USB2_PDB_CC2

C7322 C7326 C7323 C7320
0.1U10V1MK-1-GP

R7378 R7384
0R2J-2-GP
EL7303 EL7304
DLW32SN900SQ2-GP
068.09002.2001
2nd = 68.02002.061
R7383 0R2J-2-GP
R7381 0R2J-2-GP

USB2_SSTX_CON_P0 R7377 1 2 0R2R1J-GP USB2_SSTX_CON_R_P0 C7315 1 SCD22U25V1KK-1-GP USB2_SSTX_CON_C_P0
USB2_SSTX_CON_N0 R7374 1 2 0R2R1J-GP USB2_SSTX_CON_R_N0 C7324 1 SCD33U25V1KX-3-GP USB2_SSTX_CON_C_N0
USB2_SSRX_CON_P0 R7372 1 2 0R2R1J-GP USB2_SSRX_AR_R_P0 C7321 1 SCD33U25V1KX-3-GP USB2_SSRX_AR_C_P0
USB2_SSRX_CON_N0 R7356 1 2 0R2R1J-GP USB2_SSRX_AR_R_N0 C7316 1 SCD33U25V1KX-3-GP USB2_SSRX_AR_C_N0
USB2_SSTX_CON_P1 R7351 1 2 0R2R1J-GP USB2_SSTX_CON_R_P1 C7314 1 SCD22U25V1KK-1-GP USB2_SSTX_CON_C_P1
USB2_SSTX_CON_N1 R7354 1 2 0R2R1J-GP USB2_SSTX_CON_R_N1 C7318 1 SCD22U25V1KK-1-GP USB2_SSTX_CON_C_N1
USB2_SSRX_CON_P1 R7375 1 2 0R2R1J-GP USB2_SSRX_AR_R_P1 C7317 1 SCD33U25V1KX-3-GP USB2_SSRX_AR_C_P1
USB2_SSRX_CON_N1 R7388 1 2 0R2R1J-GP USB2_SSRX_AR_R_N1 C7319 1 SCD33U25V1KX-3-GP USB2_SSRX_AR_C_N1

ED7324 ED7328 ED7330 ED7331 ED7318 ED7319 ED7323 ED7329
ED7326 ED7317 ED7322 ED7332 ED7321 ED7327 ED7325 ED7320
083.5V0H1.00AF
2nd = 083.58017.00AF
3rd = 075.08315.0073

R7385 R7348 R7376 R7350 R7388 R7347 R7342 R7387
0R2J-2-GP

<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: EXT IO (Thunderbolt(3/3)/Type C Conn)
Size: A1 | Document Number | Rev: SB
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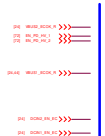
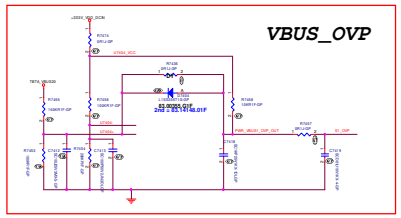
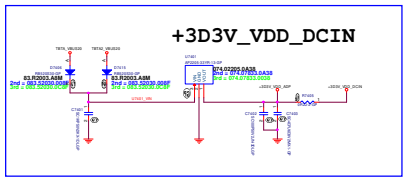
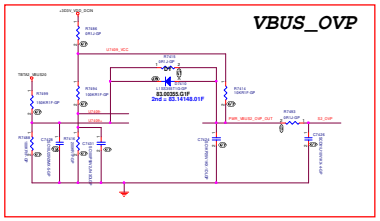
Main Func = TypeC









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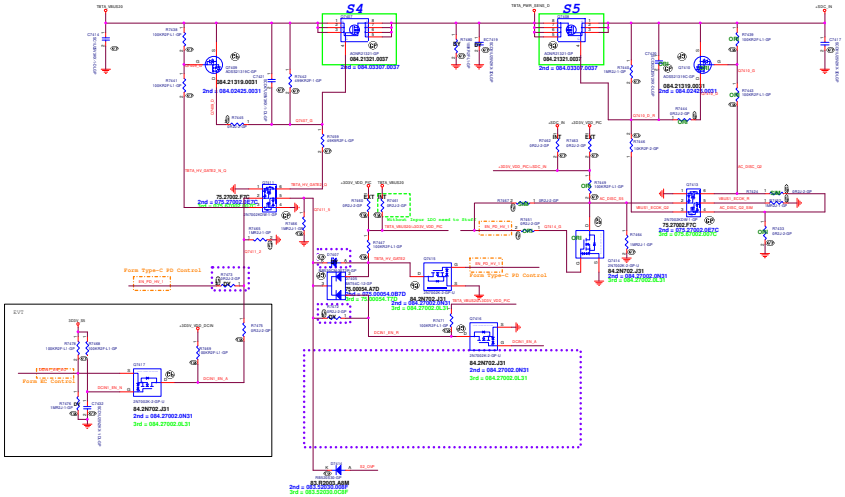

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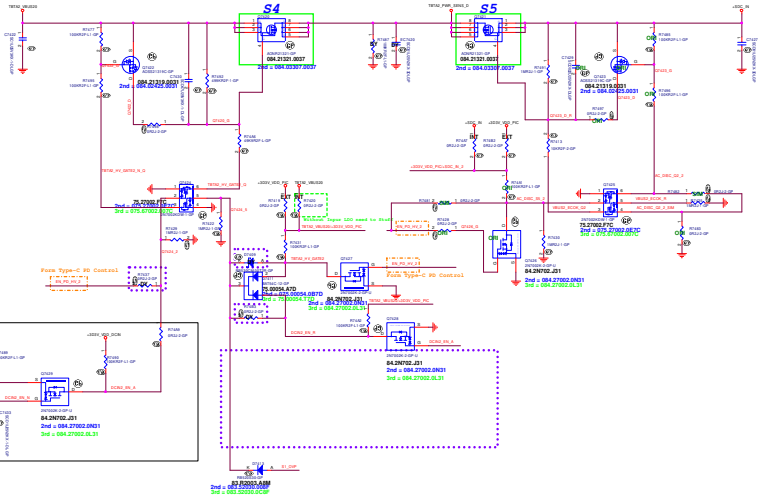

EXT IO (TYPEC PD)

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Title

EXT IO (RSVD)

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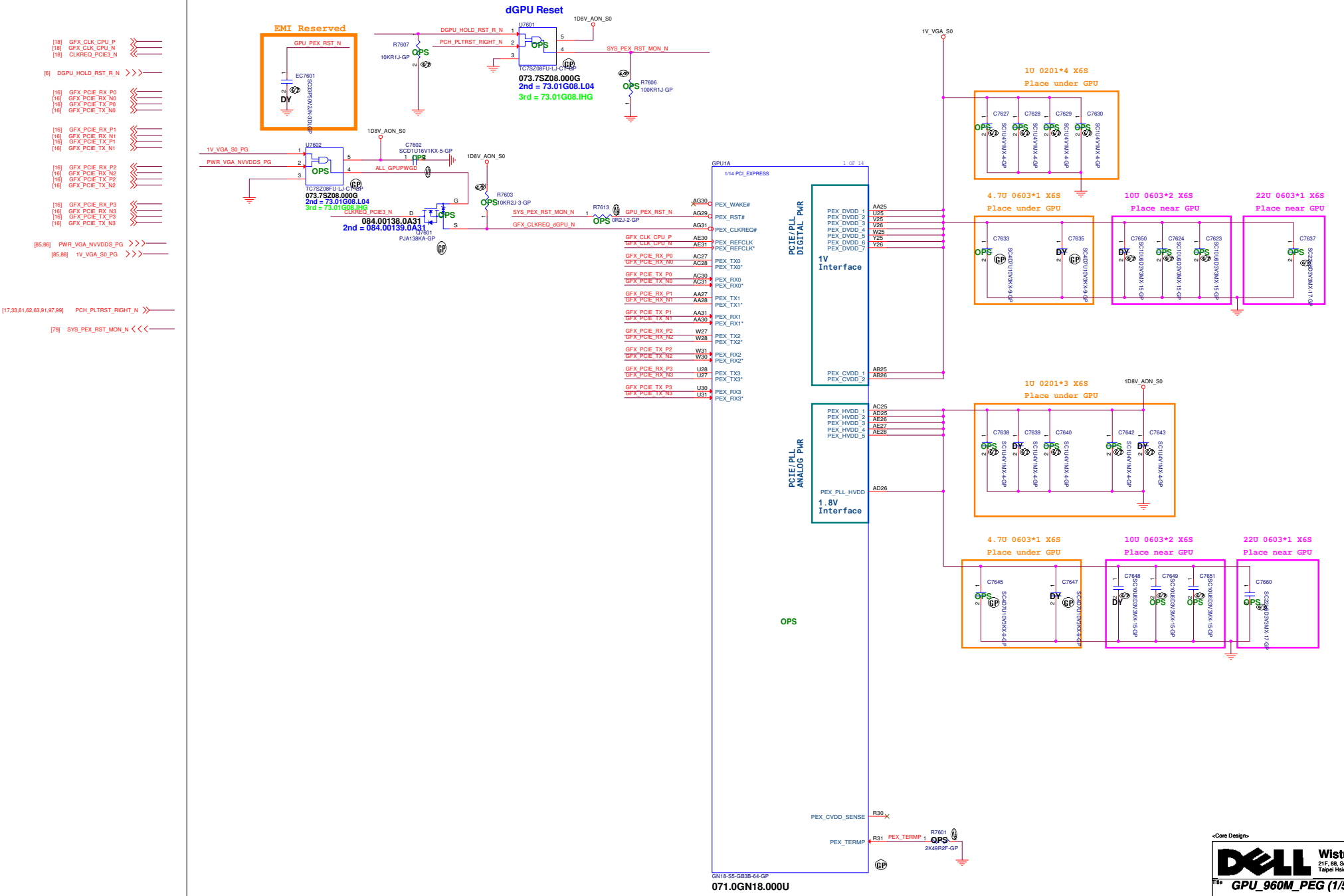
▶ PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.



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Title: GPU_960M_PEG (1/5)

Size: A2 | Document Number: SouthPeak15 MLK | Rev: SB

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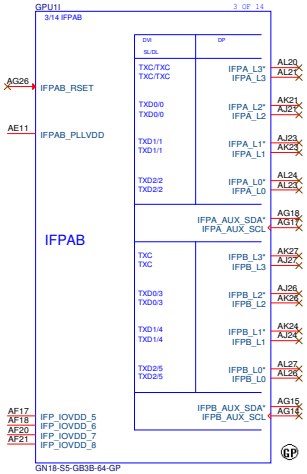
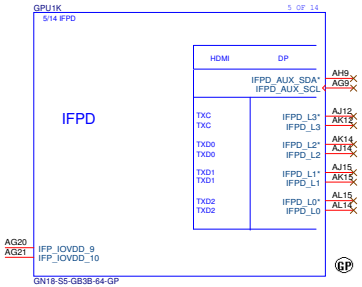
Main Func = dGPU



OPS

071.0GN18.000U



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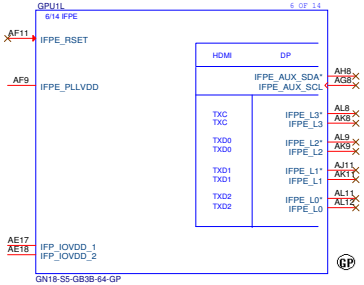

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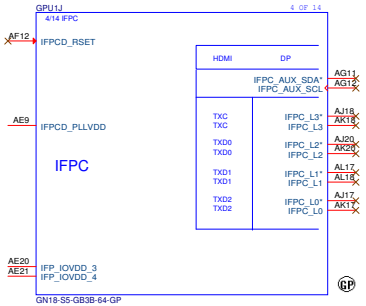

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Title: *GPU_DIGITALOUT (2/5)*

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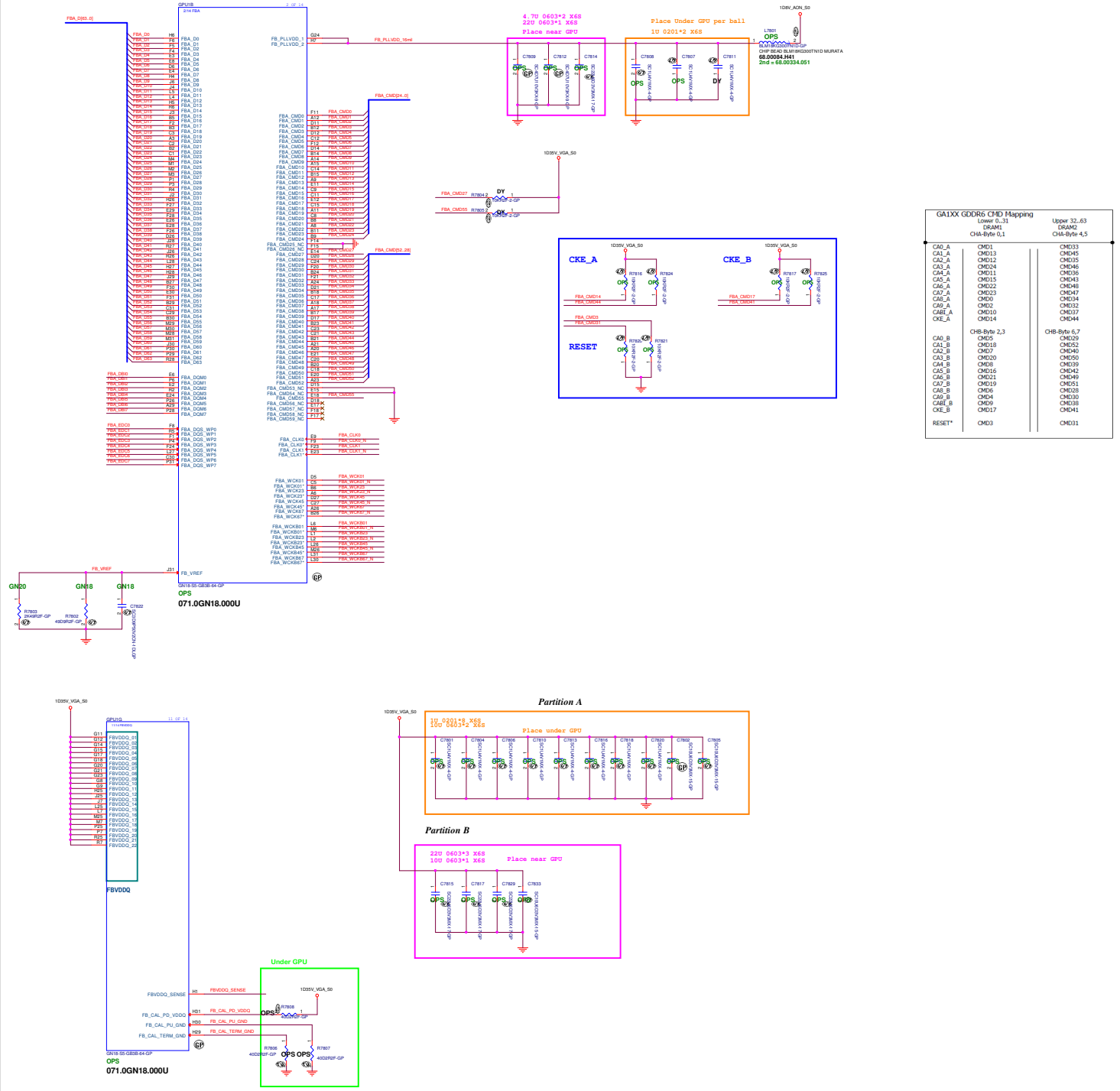
Group A

Group B



GA1XX GDDR6 CMD Mapping

	Lower 0..31 DRAM1 CHA-Byte 0,1	Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD1	CMD33
CA1_A	CMD13	CMD45
CA2_A	CMD12	CMD35
CA3_A	CMD24	CMD46
CA4_A	CMD11	CMD36
CA5_A	CMD15	CMD43
CA6_A	CMD22	CMD48
CA7_A	CMD23	CMD47
CA8_A	CMD0	CMD34
CA9_A	CMD2	CMD32
CABI_A	CMD10	CMD37
CKE_A	CMD14	CMD44
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD5	CMD29
CA1_B	CMD18	CMD52
CA2_B	CMD7	CMD40
CA3_B	CMD20	CMD50
CA4_B	CMD8	CMD39
CA5_B	CMD16	CMD42
CA6_B	CMD21	CMD49
CA7_B	CMD19	CMD51
CA8_B	CMD6	CMD28
CA9_B	CMD4	CMD30
CABI_B	CMD9	CMD38
CKE_B	CMD17	CMD41
RESET*	CMD3	CMD31

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Title: GPU_VRAM I/F (3/5)

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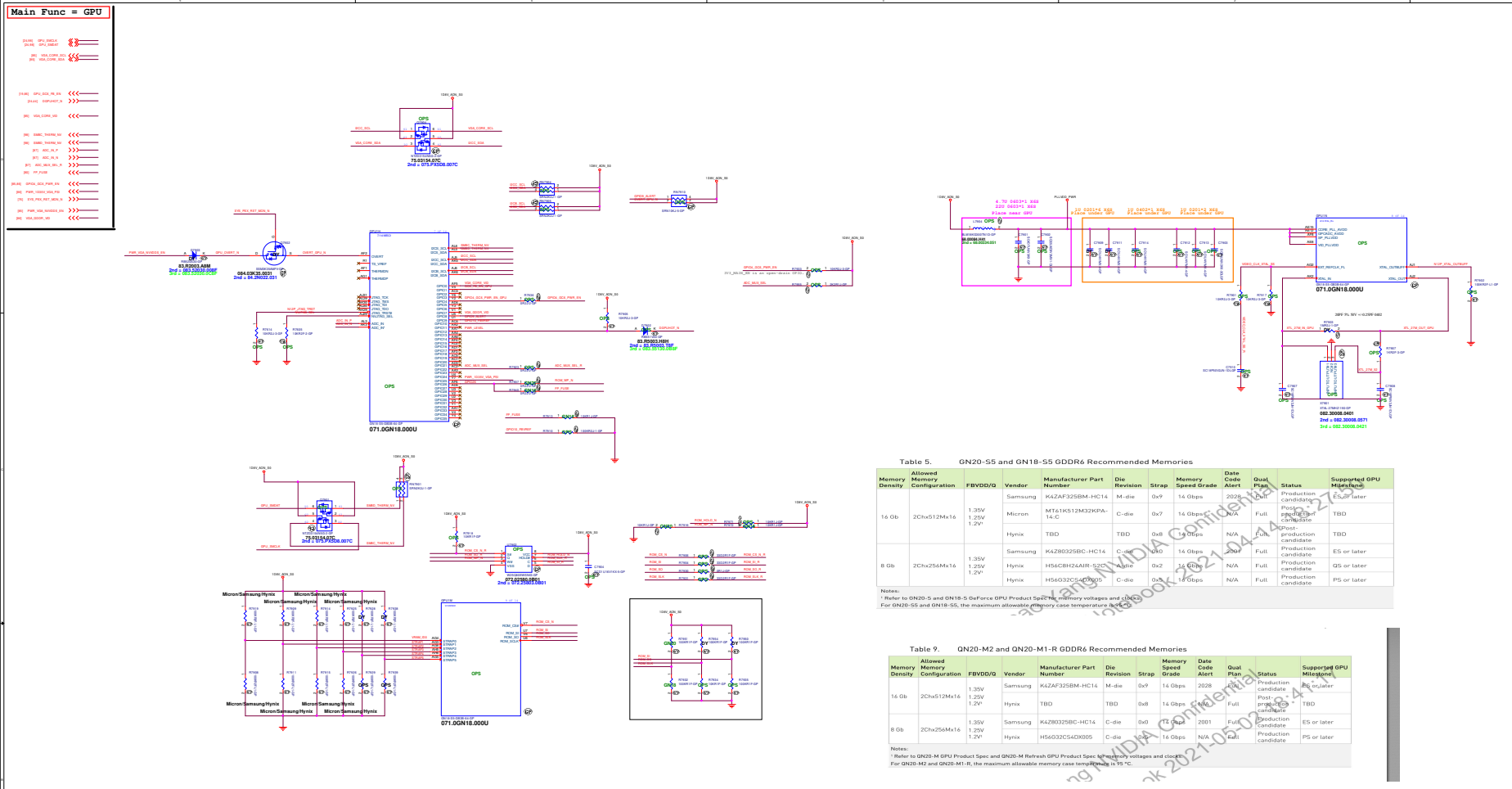


Table 5. GN20-S5 and GN18-S5 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	2028	Full	Production candidate	ES or later
			Micron	MT61K512M32KPA-14:C	C-die	0x7	14 Gbps	N/A	Full	Post-production candidate	TBD
			Hynix	TBD	TBD	0x8	14 Gbps	N/A	Full	Post-production candidate	TBD
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001	Full	Production candidate	ES or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate	QS or later
			Hynix	H56G32CS4DX005	C-die	0x5	16 Gbps	N/A	Full	Production candidate	PS or later

Notes:
[1] Refer to GN20-S and GN18-S GeForce GPU Product Spec for memory voltages and clocks.
For GN20-S5 and GN18-S5, the maximum allowable memory case temperature is 95 °C.

Table 9. QN20-M2 and QN20-M1-R GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	2028	Full	Production candidate	ES or later
			Hynix	TBD	TBD	0x8	14 Gbps	N/A	Full	Post-production candidate	TBD
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001	Full	Production candidate	ES or later
			Hynix	H56G32CS4DX005	C-die	0x5	16 Gbps	N/A	Full	Production candidate	PS or later

Notes:
[1] Refer to QN20-M GPU Product Spec and QN20-M Refresh GPU Product Spec for memory voltages and clocks.
For QN20-M2 and QN20-M1-R, the maximum allowable memory case temperature is 95 °C.

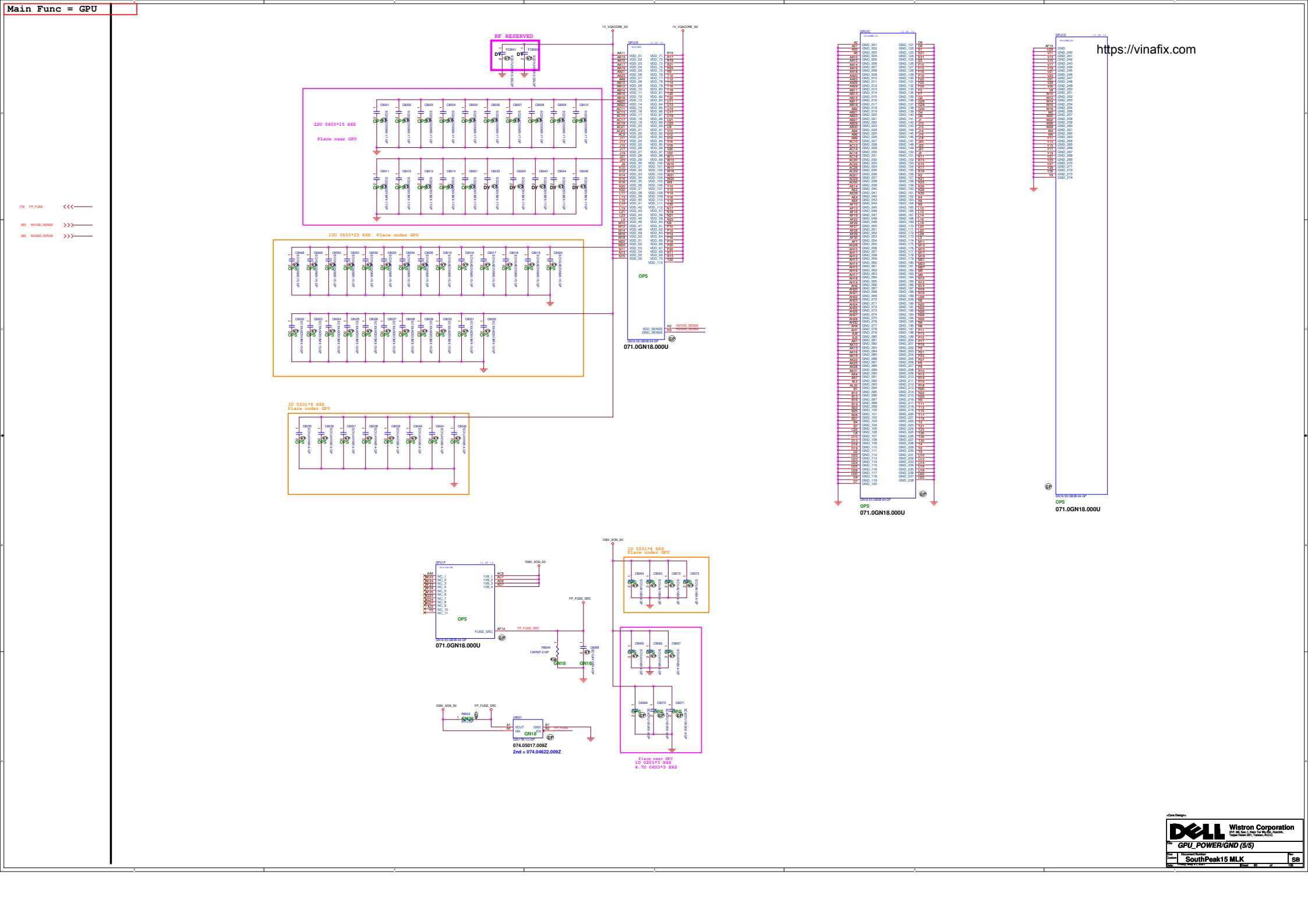
Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 3. GB3-64 and GB3B-64 Ternary Straps

Strap Pin	GB3-64	GB3B-64
ROM_SI ROM_SO ROM_CLK	Set (ROM_SO, ROM_SI, ROM_CLK) to (L, M, L) to enable FS_OVERT* • ROM_SI and ROM_CLK: 100 kΩ • ROM_SO: 10 kΩ	Set (ROM_SO, ROM_SI, ROM_CLK) to (L, L, L) to enable FS_OVERT • ROM_SI and ROM_CLK: 100 kΩ • ROM_SO: 10 kΩ

Main Func = GPU



Title	GPU_POWER/GND (5/5)
Size / Custom	Document Number: SouthPeak15 MLK
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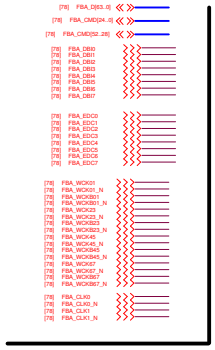
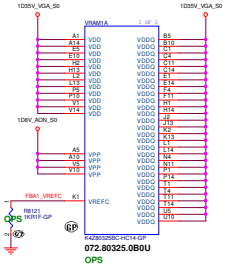
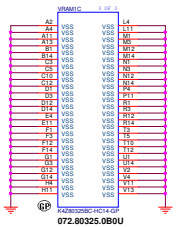
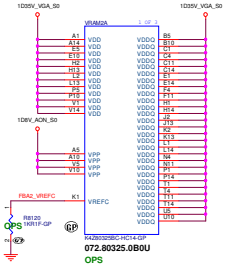
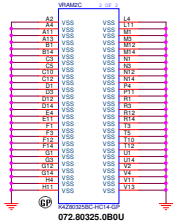










8.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for CMD and ADDR). Figure 8.8 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values.

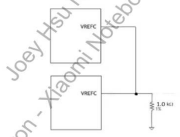
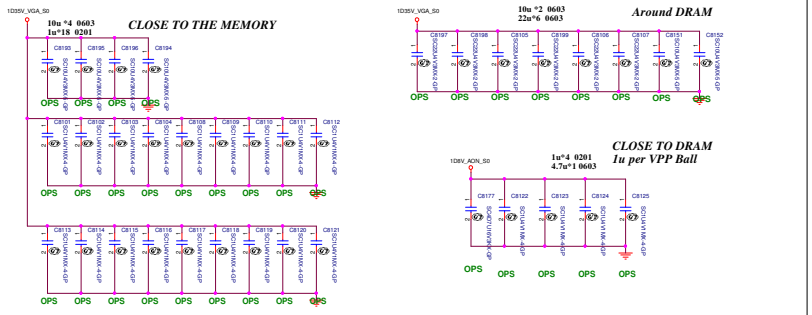


Figure 8.8 Use of Integrated VREFC for ×16 Mode

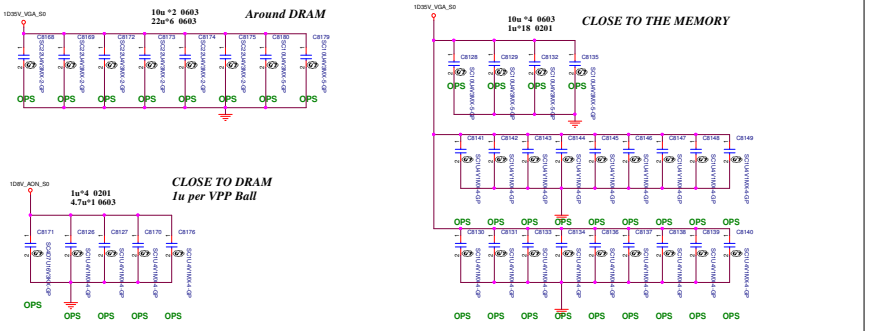
FOR VRAM1

PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE



FOR VRAM2

PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE



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File: VRAM 1,2 (1/4)

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Title ***VGA Power A***

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Title ***VGA Power B***

Size	Document Number	Rev
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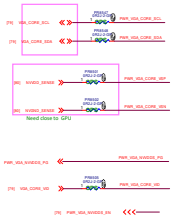

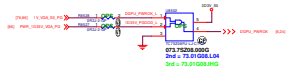

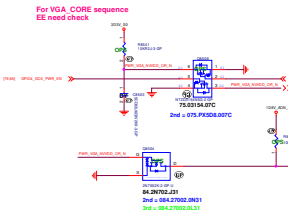

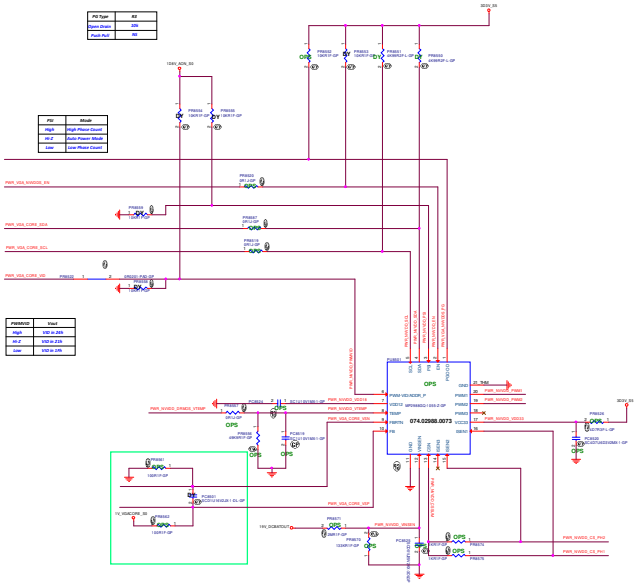

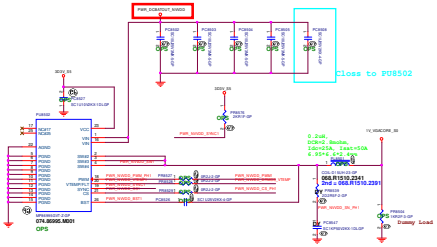

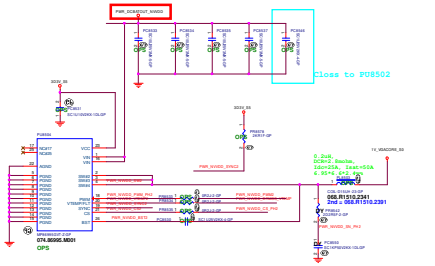

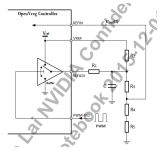

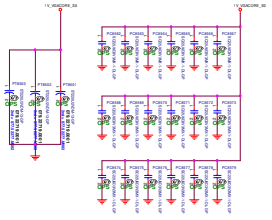

Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	~100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.499
C	nF	1.5

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	~100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.499
C	nF	1.5

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GPU VCORE POWER

SouthPeak15 MLK

OFFPAGE

Main Func = dGPU

[DG-07158-001 Rev03]Power up sequence:
3.3V ==> MVVDD (VGA_CORE) ==> PEX_VDD (1.05V) ==> FBVDD/Q (1.20V)

1D8V_S5_S0 to 1D8V_AON_S0

dGPU Power Discharge Circuit

1V_VGA_S0

VGA_CORE

1D35V_VGA_S0

1D8V_AON_S0

https://vinafix.com

1D8V_AON_S0 to 1D8V_VGA_S0

For tuning VGA_CORE sequence.

RT5797 for 1V_VGA_S0

1V_VGA_S0

Vout	PR8620
0.95V	59K (64.59025_6DL)
1V	51K (64.51025_6DL)

Iccmax : 38A
OCP : 60A

Power 1228

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

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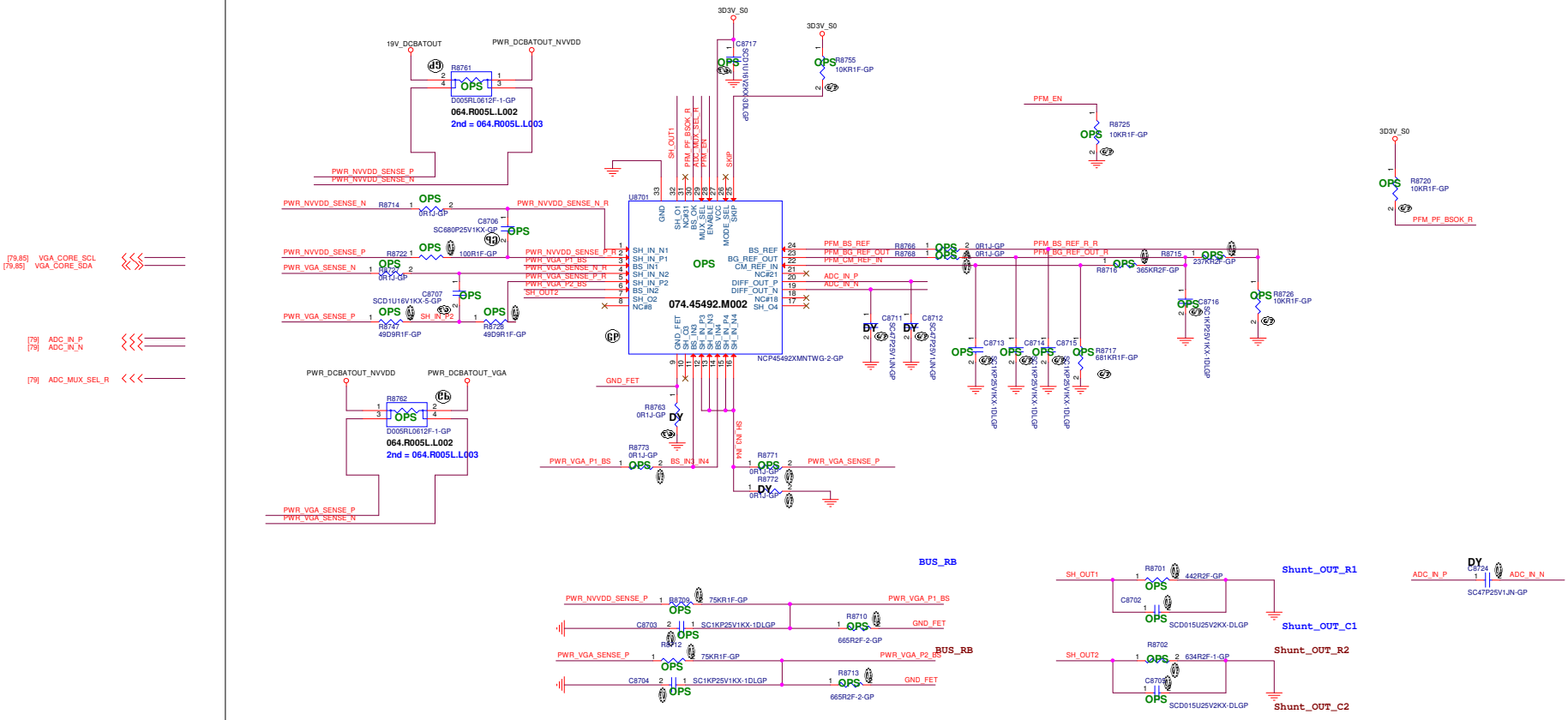
GPU GDDR 1D35V

SoundPack1S MLK

OVR-M Gen1



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Title: Discharge		
Size: A2	Document Number: SouthPeak15 MLK	Rev: SB
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<Core Design>

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Title

UNUSED PARTS (RSVD)

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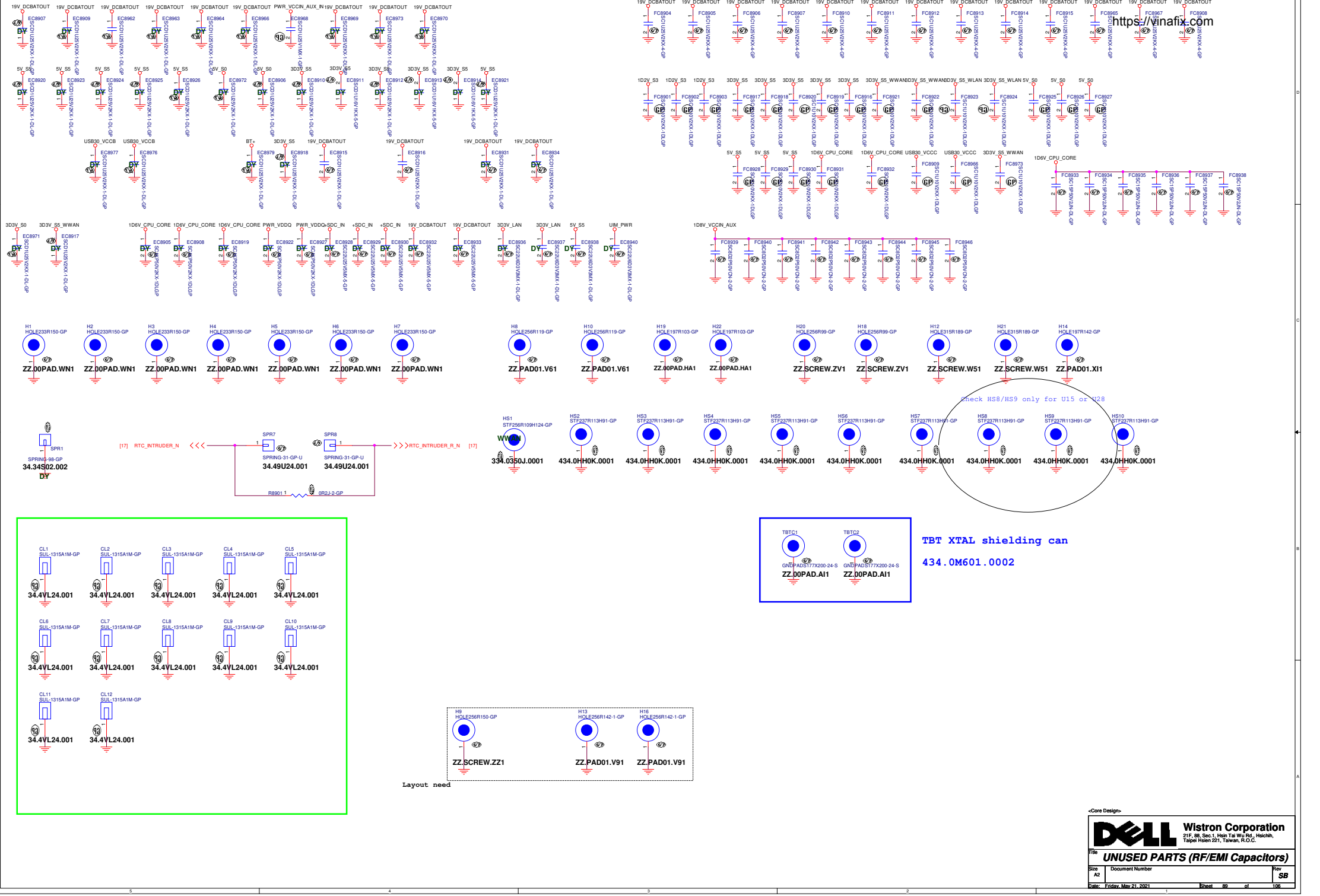
Main Func = EMC/ RF



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Title: UNUSED PARTS (RF/EMI Capacitors)

Size: A2 | Document Number | Rev: SB

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<Core Design>

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Title

INT IO (RSVD) (NFC)

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Main Func = TPM

[3] TPM_PIRQ_N
[17,68] SIO_SLP_S0_N
[17,33,61,62,63,76,97,99] PCH_PLTRST_RIGHT_N

[18,24,25,68] SPI_CLK_CPU
[15,18,24,25,68] SPI_SI_CPU
[18,24,25,68] SPI_SO_CPU
[18] SPI_CS_CPU_N2
[17,39] CPU_C10_GATE_N

R9102 3D3V_TPM 10KR1F-GP DY

SPI_CS_CPU_N2 R9103 0R1J-GP SPI_CS_TPM_N2
SPI_SO_CPU R9104 15R1F-GP SPI_SO_TPM
SPI_SI_CPU R9105 15R1F-GP SPI_SI_TPM
SPI_CLK_CPU R9106 15R1F-GP SPI_CLK_TPM

R5

3D3V_TPM
R9108 10KR1F-GP DY
Q9101
SPI_CS_CPU_N2 G
S D
2N7002K-2-GP-U
TPM_GPIO2

84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

3D3V_S0 R9101 0R2J-GP NUVOTON
3D3V_S5 R9107 0R2J-GP DY +UZ12_TPM

Do NOT change to short pad

3D3V_S5_PCH R9151 D01R2J-L-GP ST
3D3V_S0 R9150 0R2J-GP NUVOTON
3D3V_TPM1

Q9102 SM2421PSANC-TRG-GP
TPM_GPIO2 D G
3D3V_TPM
R9109 10KR1F-GP DY
084.02421.0031
2nd = 084.03401.0A31
R9110 100R1F-GP DY
Q9102.G1 SPI_CS_CPU_N2

+UZ12_TPM
3D3V_TPM1
C9104 SCD1U16V1KX-5-GP
C9102 SC10U6D3V3MX-DL-GP ST
C9107 SCD1U16V1KX-5-GP
C9105 SCD1U16V1KX-5-GP
C9106 SC4D7U6D3V2MX-GP
NUVOTON
Pin8 Pin22

C9114 C9115 SC2200P50V2KX-2DLGP DY

TPM_PIRQ_N_R R9152 0R1J-GP TPM_GPIO2
NUVOTON

3D3V_TPM
R9113 100KR1J-GP
TPM_PIRQ_N R9112 0R1J-GP TPM_PIRQ_N_R

3D3V_TPM1
45mA

3D3V_S5 R9119 0R2J-GP
3D3V_TPM R9117 0R2J-GP NUVOTON
C9101 SC4D7U6D3V2MX-1-GP NUVOTON
C9103 SCD1U16V1KX-5-GP NUVOTON
TP9102 NUVOTON_PP
TPM_VSB
+UZ12_TPM

SPI_CS_CPU_N2 R9118 2K2R1F-GP DY TPM_GPIO4
0R2J-GP R9122 U9101_16_GND
0R2J-GP R9123 U9101_23_GND
NUVOTON

U9101
VPS 22
NIC#1 1
NIC#3 3
NIC#4 4
NIC#5 5
NIC#8 8
NIC#9 9
NIC#10 10
NIC#11 11
NIC#12 12
NIC#13 13
NIC#14 14
NIC#15 15
NIC#16 16
NIC#23 23
NIC#25 25
NIC#26 26
NIC#27 27
NIC#28 28

NIC#29 29 TPM_GPIO0
NIC#30 30 TPM_GPIO1
NIC#31 31
NIC#32 32
GPIO_LP 6 TPM_GPIO0
GPIO_PP 7 ST_PP
MOSI 21 SPI_SI_TPM
MISO 24 SPI_SO_TPM
SPI_RST# 17 PCH_PLTRST_TPM_N
SPI_PIRQ# 18 TPM_PIRQ_N_R
SPI_CS# 20 SPI_CS_TPM_N2
SPI_CLK 19 SPI_CLK_TPM
GND 2
THERMAL_PAD 33_THM

ST33HTPH2X32AHD8-GP
071.33232.0L03
Colay
NPCT750JADYX-1-GP
071.00760.0003

R9114 0R1J-GP DY CPU_C10_GATE_N
R9111 0R1J-GP DY SIO_SLP_S0_N
TP9104
TP9101
R9120 0R1J-GP PCH_PLTRST_RIGHT_N

U9101_2_GND
R9124 0R2J-GP ST

Do NOT change to short pad

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (TPM)
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Main Func = Finger Printer

[16] FP_USB20_P
[16] FP_USB20_N
[24,64] FPR_DET_N
[66] FP_USB20_USH_N
[66] FP_USB20_USH_P
[24] FPR_PWR_EN_N
[24,66] FPR_SCAN_INT_N
[24] FPR_SSO_EN_N
[24] FPR_LOW_PWR_MODE_N
[66] FP_RESET_N
[24] FPR_LED_N
[64] MASK_BASE_LEDS_N_Q

3D3V_S5 — R9204 100KR2F-L1-GP — EC9202 SC1KP50V2KX-1DLGP (DY)

FP2 FOX-CONN16D-1-GP (GP)
20.F2321.016
2nd = 20.F2448.016

FPR_DET_N
FPR_LED_4
FPR_LED_3
FPR_LED_2
FPR_LED_1
FPR_LOW_PWR_MODE_N
FPR_UEFI_MGMT_N_R
FPR_SCAN_INT_N_R
FP_USB20_CON_P
FP_USB20_CON_N
FP_RESET_N_R
FPR_SSO_EN_N

3D3V_S0_FP — R9215 100KR2J-1-GP — EC9203 SC1KP50V2KX-1DLGP (DY)

3D3V_S0_FP — R9216 0R2J-2-GP — FP_PH

R9212 10KR2F-2-GP FPR_UEFI_MGMT_N_R
R9213 100KR2F-L1-GP FPR_SSO_EN_N
R9214 100KR2F-L1-GP FPR_LOW_PWR_MODE_N

3D3V_S5 — R9220 100KR2F-L1-GP FPR_PWR_EN_N

100mA

3D3V_S5 — R9205 D01R2J-L-GP — 3D3V_FP_PWR — Q9202 PJA3415AE-GP
084.03415.0C31
2nd = 84.03327.031

3D3V_S0_FP_R — R9217 D01R2J-L-GP — C9203 SCD1U16V1KX-5-GP (DY)

FPR_PWR_EN_N — R9224 0R1J-GP — FPR_PWR_EN_N_R
C9208 SCD1U16V1KX-5-GP (DY)

Try to co-lay

Do NOT change to short pad

PCH	USH
FP_USB20_N — R9208 0R2J-2-GP (DY) — FP_USB20_R_N	FP_USB20_R_N — R9206 0R2J-2-GP — FP_USB20_USH_N
FP_USB20_P — R9209 0R2J-2-GP (DY) — FP_USB20_R_P	FP_USB20_R_P — R9207 0R2J-2-GP — FP_USB20_USH_P

FP_USB20_CON_N — EU9202 K2
FP_USB20_CON_P — EU9202 K1
EU9202 A
EU9202 UCLAMP0502T-TCT-GP
83.00502.0A0
2nd = 083.08822.00A3

5V_S5 — R9230 100KR2F-L1-GP — Q9204 PJA3415AE-GP
084.03415.0C31
2nd = 84.03327.031

FP_LED_D — R9225 1K2R2F-1-GP — FPR_LED_1
R9226 1K2R2F-1-GP — FPR_LED_2
R9227 1K2R2F-1-GP — FPR_LED_3
R9228 1K2R2F-1-GP — FPR_LED_4

FPR_LED_N — Q9207
MASK_BASE_LEDS_N_Q — Q9207
Q9207 2N7002K-2-GP-U
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

FP_LED_EN_N — R9231 0R1J-GP — FP_LED_EN_N_R
C9207 SCD1U16V1KX-5-GP (DY)

R9202 0R2J-2-GP
FP_USB20_CON_P — EL9201 — FP_USB20_R_P
FP_USB20_CON_N — EL9201 — FP_USB20_R_N
EL9201 FILTER-4P-156-GP-U
068.24900.2001
R9201 0R2J-2-GP

3D3V_S0_FP — R9211 100KR2F-L1-GP — FPR_SCAN_INT_N_R
3D3V_S0_FP — Q9203
Q9203 2N7002K-2-GP-U
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

3D3V_S5 — R9222 100KR2F-L1-GP — FPR_SCAN_INT_N
R9223 0R2J-2-GP (DY)

FP_RESET_N_R — R9221 0R2J-2-GP (DY) — D9202 RB520S30-GP — FP_RESET_N
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Finger Printer)
Size: A3 | Document Number | Rev: SB
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
EXT IO (RSVD) (Express Card/PCIE slot)

Size	Document Number	Rev
A4		*SB*

Date:	Friday, May 21, 2021	Sheet	93	of	106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
EXT IO (RSVD) (Smart Card/COM/PS2)

Size	Document Number	Rev
A4		*SB*

Date: Friday, May 21, 2021 Sheet 94 of 106

<Core Design>

Wistron Corporation
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Title

EXT IO (RSVD) (Docking/LPT)

Size	Document Number	Rev
A4		*SB*

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Main Func = LAN

LAN

[16] LAN_PCIE_RX_N
[16] LAN_PCIE_RX_P
[16] LAN_PCIE_TX_N
[16] LAN_PCIE_TX_P

[3,61,62,63,76,91,99] PCH_PLTRST_RIGHT_N
[17] LAN_WAKE_N
[17] PM_LANPHY_EN
[18,71,98] SML0_SMBCLK
[18,71,98] SML0_SMBDATA
[32] LAN_0_GREEN_LINK_N
[32] LAN_1_AMBER_ACT_N
[24] LOM_CABLE_DETECT_N
[32] LAN_MDI0_P
[32] LAN_MDI0_N
[32] LAN_MDI1_P
[32] LAN_MDI1_N
[32] LAN_MDI2_P
[32] LAN_MDI2_N
[32] LAN_MDI3_P
[32] LAN_MDI3_N
[18] LAN_CLK_CPU_N
[18] LAN_CLK_CPU_P
[18] CLKREQ_PCIE6_N
[98] CPU_SMB_SCL_LAN
[98] CPU_SMB_SDA_LAN

3D3V_LAN
DY R9701 10KR2F-2-GP
PM_LANPHY_EN
DY R9702 10KR2F-2-GP

DESIGN NOTE: LAN_DISABLE_N must be connected to PCH's GPIO/LANPHYPC output. This GPIO pin must be set as "LANPHYPC" function through FITC tool. The signal does not require pull-up. R15 resistor is no-stuff default (for testing purpose).

https://vinafix.com

U9701

CLKREQ_PCIE6_N 48 CLK_REQ#
PCH_PLTRST_RIGHT_N 36 PE_RST#
LAN_CLK_CPU_P 44 PE_CLKP
LAN_CLK_CPU_N 45 PE_CLKN
PCIE

LAN_PCIE_RX_P C9701 SCD1U16V2KX-3DLGP LAN_PCIE_RX_C_P 38 PETP
LAN_PCIE_RX_N C9702 SCD1U16V2KX-3DLGP LAN_PCIE_RX_C_N 39 PETN
LAN_PCIE_TX_P C9703 SCD1U16V2KX-3DLGP LAN_PCIE_TX_C_P 41 PERP
LAN_PCIE_TX_N C9704 SCD1U16V2KX-3DLGP LAN_PCIE_TX_C_N 42 PERN

MDI_PLUS0 13 LAN_MDI0_P
MDI_MINUS0 14 LAN_MDI0_N
MDI_PLUS1 17 LAN_MDI1_P
MDI_MINUS1 18 LAN_MDI1_N
MDI_PLUS2 20 LAN_MDI2_P
MDI_MINUS2 21 LAN_MDI2_N
MDI_PLUS3 23 LAN_MDI3_P
MDI_MINUS3 24 LAN_MDI3_N
MDI

SML0_SMBCLK R9704 0R2J-2-GP CPU_SMB_SCL_LAN 28 SMB_CLK
SML0_SMBDATA R9706 0R2J-2-GP CPU_SMB_SDA_LAN 31 SMB_DATA
SMBUS

LAN_WAKE_N R9708 0R2J-2-GP LAN_WAKE_R_N 2 LANWAKE#
PM_LANPHY_EN R9710 0R2J-2-GP LAN_DISABLE_R_N 3 LAN_DISABLE#

NOTE:DESIGN NOTE: LANWAKE_N must be connected to PCH's LANWAKE input.

TP9703 TPAD14-OP-GP
LAN_0_GREEN_LINK_N 26 LED0
LAN_1_AMBER_ACT_N 27 LED1
LAN_LED2 25 LED2
LED

TP9701 TPAD14-OP-GP
TP9702 TPAD14-OP-GP
LAN_JTAG_TDI 32 JTAG_TDI
LAN_JTAG_TDO 34 JTAG_TDO
LAN_JTAG_TMS 33 JTAG_TMS
LAN_JTAG_TCK 35 JTAG_TCK
JTAG

LAN_0_GREEN_LINK_N
LAN_1_AMBER_ACT_N
LAN_LED2
EC9702 SC1KP50V2KX-1DLGP
EC9703 SC1KP50V2KX-1DLGP
EC9704 SC1KP50V2KX-1DLGP

XTL_25M_X2_LAN 9 XTAL_OUT
XTL_25M_X1_LAN 10 XTAL_IN
R9713 1KR2F-3-GP
TEST_EN 30 TEST_EN
RBIAS 12 RBIAS
R9714 3K01R2F-3-GP

SVR_EN# 6 SVR_EN_N
RSVD1_VSS3P3 1 RSVD1_VCC3P3
R9703 0R0402-PAD-1-GP
DY R9705 4K7R2F-GP
DY R9707 4K7R2F-GP
3D3V_LAN

VDD3P3_IN 5
VDD3P3 4 15 19 29
3D3V_LANOUT
C9705 SC22U6D3V3MX-1-DL-GP
C9714 SCD1U16V2KX-3DLGP
DY C9707 SC22U6D3V3MX-1-DL-GP
R9709 0R3J-0-U-GP
3D3V_LAN

VDD0P9 8 11 16 22 37
VDD0P9_11
VDD0P9_LAN
L9701 IND-4D7UH-268-GP
CTRL0P9 7 CTRL_0P9
GND 49
68.4R71F.10H
2nd = 068.4R710.1761
3rd = 068.4R710.1771
C9708 SC22U6D3V3MX-1-DL-GP
C9709 SCD1U16V2KX-3DLGP
DY C9710 SC10U10V2MX-DL-GP-U

WGI219LM-GP
071.219LM.0003

3D3V_LAN R9711 1MR2F-GP LAN_0_GREEN_LINK_N
Refer RoundRock

C9711 SC15P50V2JN-DL-GP XTL_25M_X2_LAN_R R9717 0R0402-PAD-1-GP XTL_25M_X2_LAN
X9701
INPUT/OUTPUT#1
NO_CONNECT
INPUT/OUTPUT#3
XTAL-25MHZ-334-GP
082.30005.0911
2nd = 082.30005.0B21
3rd = 082.30005.0931
R9720 DY 1MR2F-GP
C9713 SC15P50V2JN-DL-GP XTL_25M_X1_LAN

3D3V_LAN
DY R9715 10KR2F-2-GP LAN_JTAG_TMS
DY R9716 10KR2F-2-GP LAN_JTAG_TCK
DY R9718 4K7R2F-GP CLKREQ_PCIE6_N
DY R9719 10KR2F-2-GP LAN_WAKE_R_N

LAN_0_GREEN_LINK_N R9712 0R2J-2-GP LOM_CABLE_DETECT_N

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Commercial (Intel LAN)

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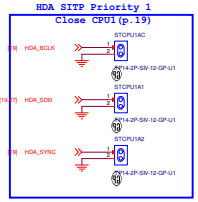
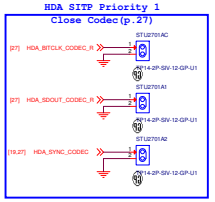
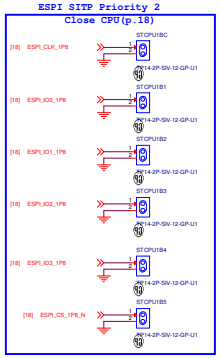
HDA SITP Priority 1
Close CPU1(p.19)



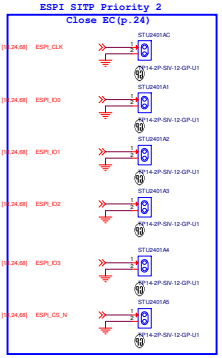
HDA SITP Priority 1
Close Codec(p.27)



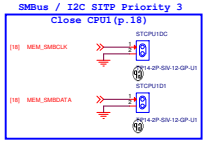
ESPI SITP Priority 2
Close CPU(p.18)



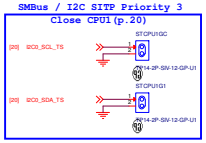
ESPI SITP Priority 2
Close EC(p.24)



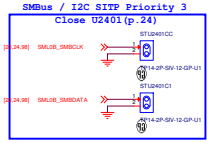
SMBus / I2C SITP Priority 3
Close CPU1(p.18)



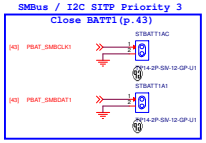
SMBus / I2C SITP Priority 3
Close CPU1(p.20)



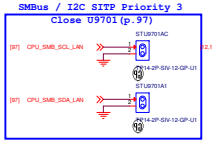
SMBus / I2C SITP Priority 3
Close U2401(p.24)



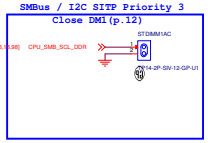
SMBus / I2C SITP Priority 3
Close BATT1(p.43)



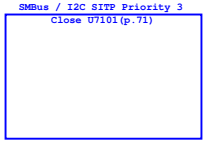
SMBus / I2C SITP Priority 3
Close U9701(p.97)



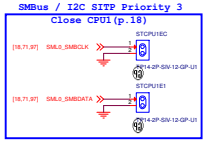
SMBus / I2C SITP Priority 3
Close DM1(p.12)



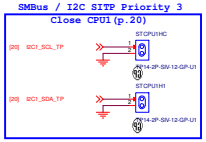
SMBus / I2C SITP Priority 3
Close U7101(p.71)



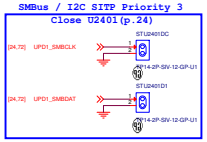
SMBus / I2C SITP Priority 3
Close CPU1(p.18)



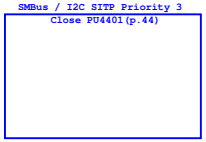
SMBus / I2C SITP Priority 3
Close CPU1(p.20)



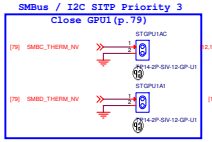
SMBus / I2C SITP Priority 3
Close U2401(p.24)



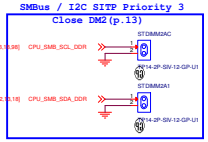
SMBus / I2C SITP Priority 3
Close PU4401(p.44)



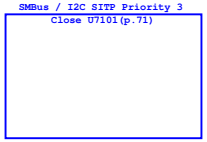
SMBus / I2C SITP Priority 3
Close GPU1(p.79)



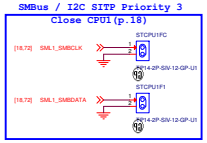
SMBus / I2C SITP Priority 3
Close DM2(p.13)



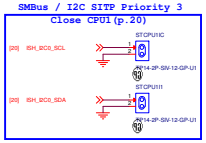
SMBus / I2C SITP Priority 3
Close U7101(p.71)



SMBus / I2C SITP Priority 3
Close CPU1(p.18)



SMBus / I2C SITP Priority 3
Close CPU1(p.20)



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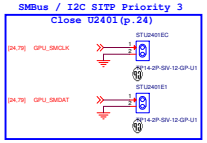

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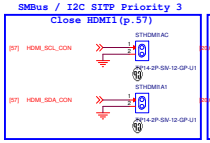
Close HDMI1(p.57)



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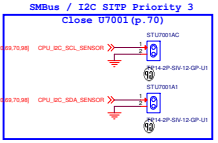
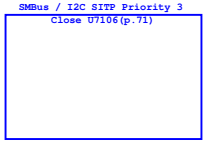
Close U7001(p.70)



SMBus / I2C SITP Priority 3
Close U7106(p.71)



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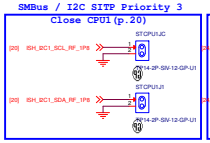
Close CPU1(p.20)



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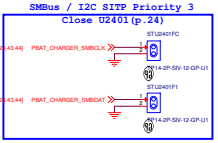
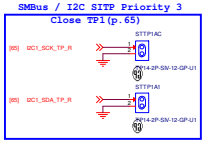
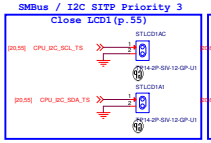


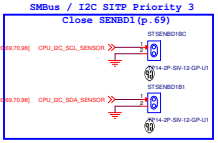
SMBus / I2C SITP Priority 3
Close TP1(p.65)



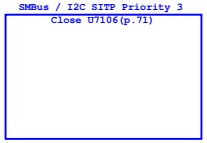
SMBus / I2C SITP Priority 3
Close LCD1(p.55)



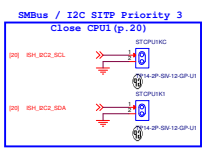
SMBus / I2C SITP Priority 3
Close SENBD1(p.69)



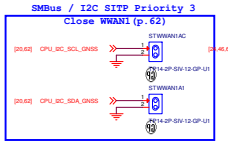
SMBus / I2C SITP Priority 3
Close U7106(p.71)



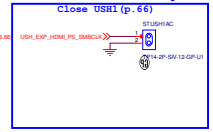
SMBus / I2C SITP Priority 3
Close CPU1(p.20)



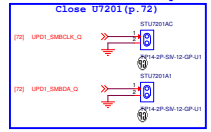
SMBus / I2C SITP Priority 3
Close WWAN1(p.62)



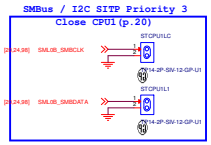
SMBus / I2C SITP Priority 3
Close USH1(p.66)



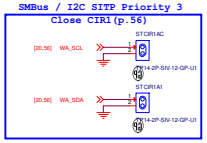
SMBus / I2C SITP Priority 3
Close U7201(p.72)



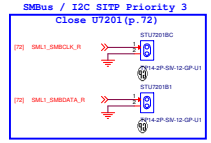
SMBus / I2C SITP Priority 3
Close CPU1(p.20)



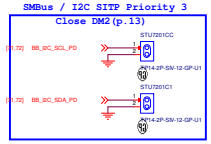
SMBus / I2C SITP Priority 3
Close CIR1(p.56)



SMBus / I2C SITP Priority 3
Close U7201(p.72)



SMBus / I2C SITP Priority 3
Close DM2(p.13)



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Commercial (LAN Switch)
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Main Func = Debug (MIPI)

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[3,15] DBG_PMODE
[3] PCH_JTAG_TCK
[3] CPU_JTAG_PRDY_N
[3] CPU_JTAG_PREQ_N
[3] CPU_JTAG_TRST_N
[3] CPU_JTAG_TCK
[3] CPU_JTAG_TDI
[3] CPU_JTAG_TDO
[3] CPU_JTAG_TMS

[15,18,24,25,68] SPI_WP_CPU
[17,24,39,64] RSMRST_KBC_N
[40] XDP_OVERRIDE_N
[3] CPU_EAR

CPU_EAR — R9927 0R1J-GP — XDP_CFG0_N_R
SPI_WP_CPU — R9923 1KR1J-GP — XDP_PRSNT_PIN1
RSMRST_KBC_N — R9920 1KR1J-GP — XDP_RSMRST_N
CPU_JTAG_TRST_N — R9904 0R1J-GP — XDP_JTAG_TRST_N
CPU_JTAG_TDI — R9906 0R1J-GP — XDP_JTAG_TDI
CPU_JTAG_TDO — R9908 0R1J-GP — XDP_JTAG_TDO
CPU_JTAG_TMS — R9910 0R1J-GP — XDP_JTAG_TMS
CPU_JTAG_TCK — R9912 0R1J-GP — XDP_JTAG_TCK
PCH_JTAG_TCK — R9916 0R1J-GP — XDP_JTAG_TCK1

[17,33,61,62,63,76,91,97] PCH_PLTRST_RIGHT_N

1D05V_S5_OUT — R9907 0R3J-0-U-GP — 1D05V_S5_XDP

1D05V_S5_XDP — R9905 0R3J-0-U-GP — 1D05V_CPU_XDP_CD
C9904 SCD1U16V2KX-3DLGP

XDP1 (XDP):
19 17 1
2 XDP_JTAG_TCK
3 XDP_JTAG_TDI
4 XDP_JTAG_TMS
5 XDP_JTAG_TDO
6 XDP_JTAG_TRST_N
7 XDP_ITP_PMODE
8 CPU_JTAG_PRDY_N
9 XDP_JTAG_TCK1
10 XDP_RSMRST_N
11 XDP_PRSNT_PIN1
12 XDP_OVERRIDE_N
13 CPU_JTAG_PREQ_N
14 XDP_CFG0_N_R
15 PCH_PLTRST_RIGHT_N
16 18 20
CLX-CCAP18-3-GP-U

3D3V_AUX_S5 — R9901 100KR1J-GP — XDP

020.K0451.M001

DBG_PMODE — R9917 0R1J-GP — XDP_ITP_PMODE

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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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Change notes –

	VERSON	DATE	Page	Modify List	OWNER
	X00		6	Add R615 and R616 1K ohm resistor.	EE
	X00		17	Change R1737.1 from 3D3V_0 to 3D3V_S5_PCH	EE
	X00		27	Change U2701 to 071.03204.M001	EE
	X00		25	Reserve 0 ohm resistor for CS0 and CS1. Add R2535 R2537 R2538 R2539	EE
	X00		33	Reserve 0 ohm resistor for SD_WP. Add R3304	EE
	X00		55.56	Modify CIR1 and LCD1 pin define to reduce cable jump wire.	EE
	X00		64	Change CLEDB1 to 020.K0328.0004	EE
	X00		66	Assign one pin for USH_IDENTIFY. Add R6611	EE
	X00		68	Add resistor on debug connector for security. Add R6823 and R6824	EE
	X00		72	Change to X13 PD GPIO table.	EE
	X00		72	Change U7201 from 071.19080.000U to 071.65994.0D0U	EE
	X00		74	Change DCIN1_EN circuit to solve +SDC_IN leakage on power swap. Change Q7417 to single MOS and modify circuit	EE
	X00		76~87	Change N18S-G5 to GN18-S5.	EE
	X00		68	Delete SPI1 R6808 R6809 R6810 R6811 R6812 R6813 R6814 D6802 R6815 G6801	EE
	X00		61	Follow RVP and CSLP CLKREQ_CNV PD resistor value. Change R6103 to 75K	EE
	X00		22	Reserve RN2002 PU to 3D3V_S5_PCH. Reserve R4063 0 ohm resistor.	EE
	X00		16	Reserve R1611, R1612 PU/PD resistor for SD_Support pin.	EE
	X00		24	Add R24A4 for VCI_IN1_N and tie to POWER_SW_IN_N	EE
	X00		44	PR4410 is modified from 105k to 316k (64.31635.6DL)	PWR
	X00		44	PR4413 is modified from 9.09k to 12.1k (64.12125.6DL)	PWR
	X00		45	PU4501 is changed from TPS51393 to SY8386B	PWR
	X00		45	PU4551 is changed from SY8288 to SY8388	PWR
	X00		46	PU4601 is changed from RAA225000 to MP2964 (074.02964.M009)	PWR
	X00		47	PU4701&PU4702 are changed from SIC648AED to MP86995GVT (074.86995.M001)	PWR
	X00		48	PU4801 is changed from SIC648AED to MP86995GVT (074.86995.M001)	PWR
	X00		50	PU5001 is changed from AOZ23645 to MP2961GL (074.02961.M001)	PWR
	X00		54	PU5401&PU5402 are changed from 2x SYV659 to 1x APW8743	PWR
	X00		85	PU8502&PU8504 are changed from MP86941 to MP86995GVT (074.86995.M001)	PWR
	X00		85	Add 1k dummy load @ 1V_VGACORE_S0	PWR
	X00		85	PL8501 & PL8503 are changed to 0.15uH (068.R1510.2341)	PWR
	X00		85	PR8571 is changed to 2 ??Ω and PR8570 is changed to 133 KΩ	PWR

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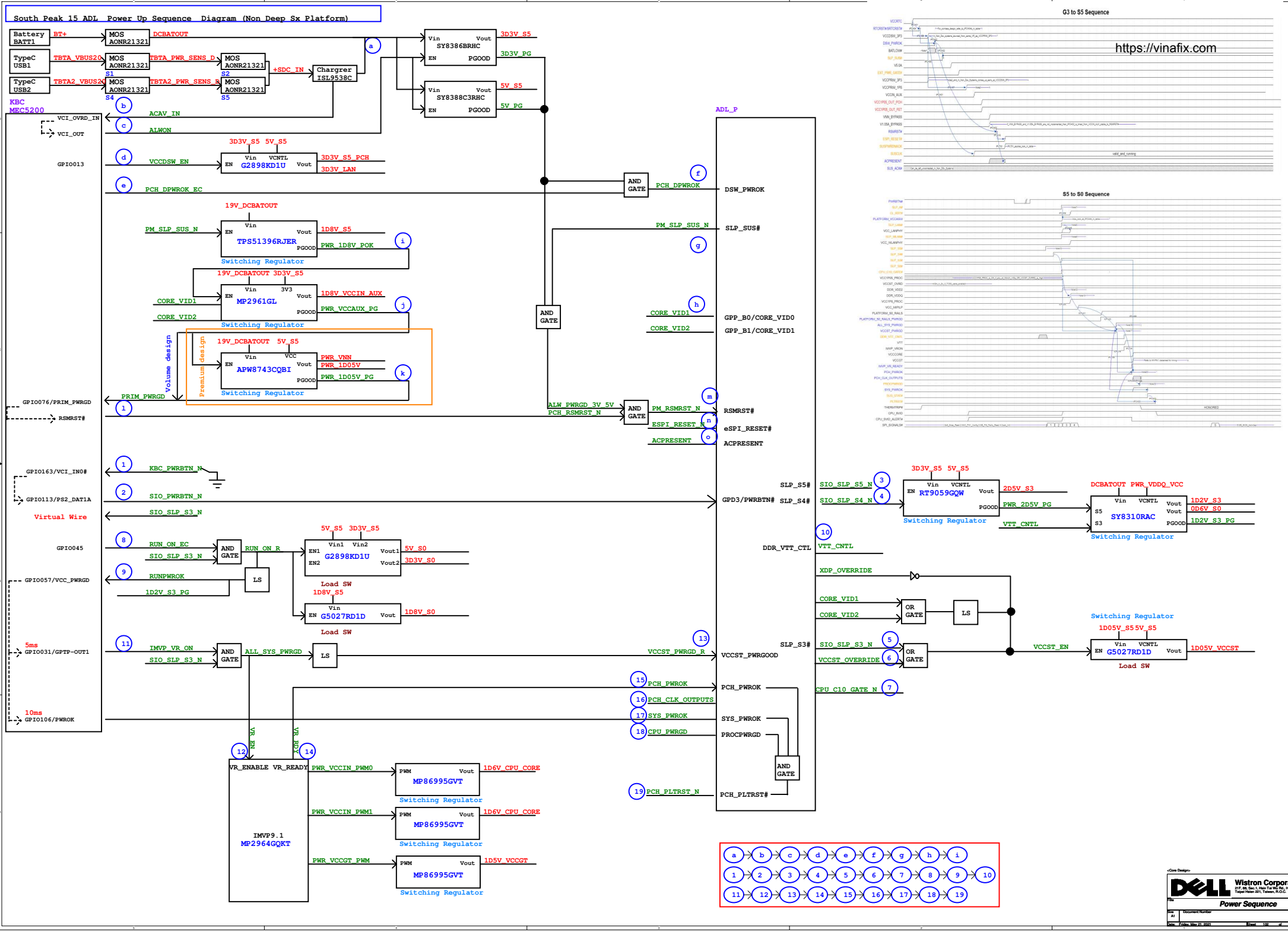
South Peak 15 ADL Power Up Sequence Diagram (Non Deep Sx Platform)



a	b	c	d	e	f	g	h	i	
1	2	3	4	5	6	7	8	9	10
11	12	13	14	15	16	17	18	19	

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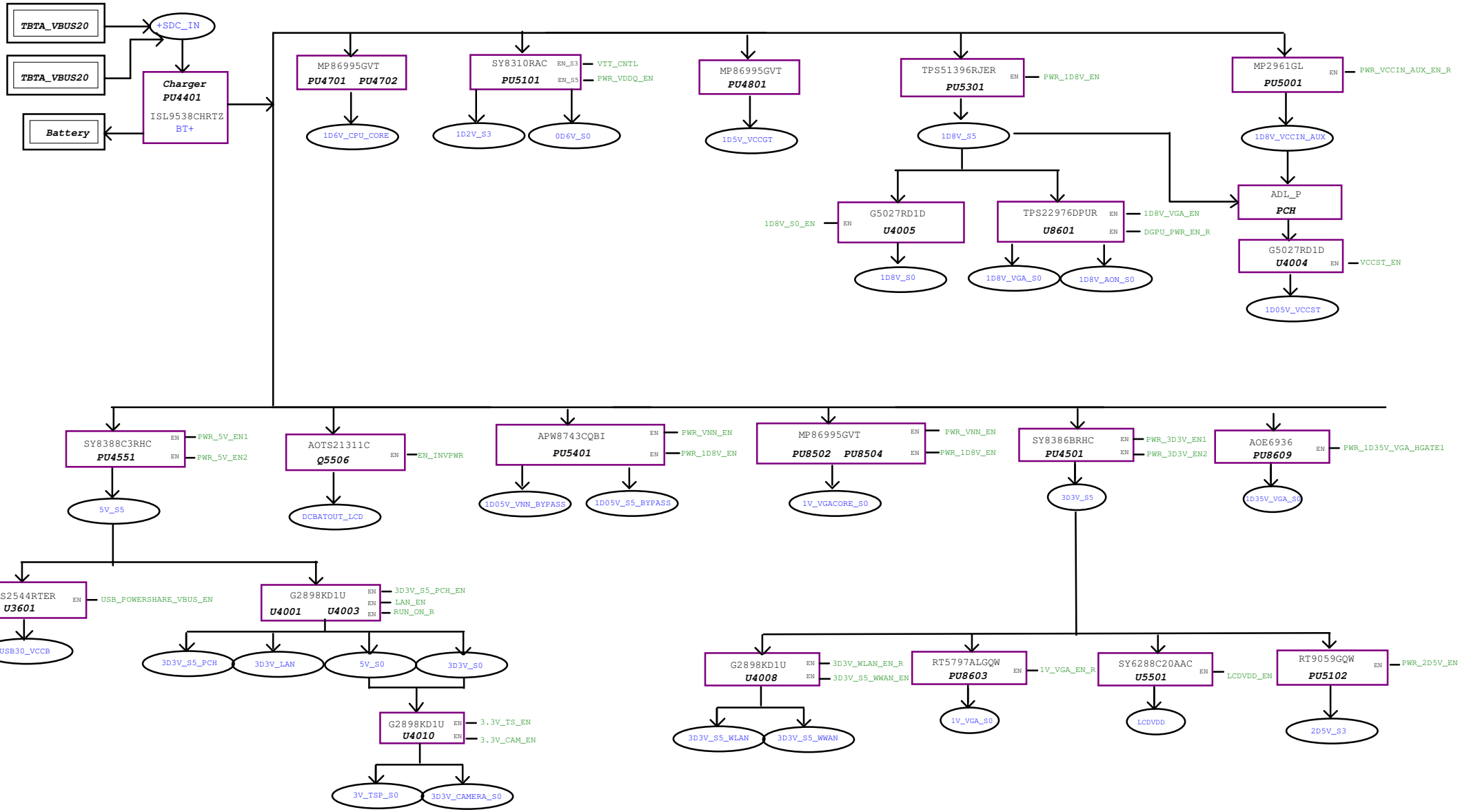

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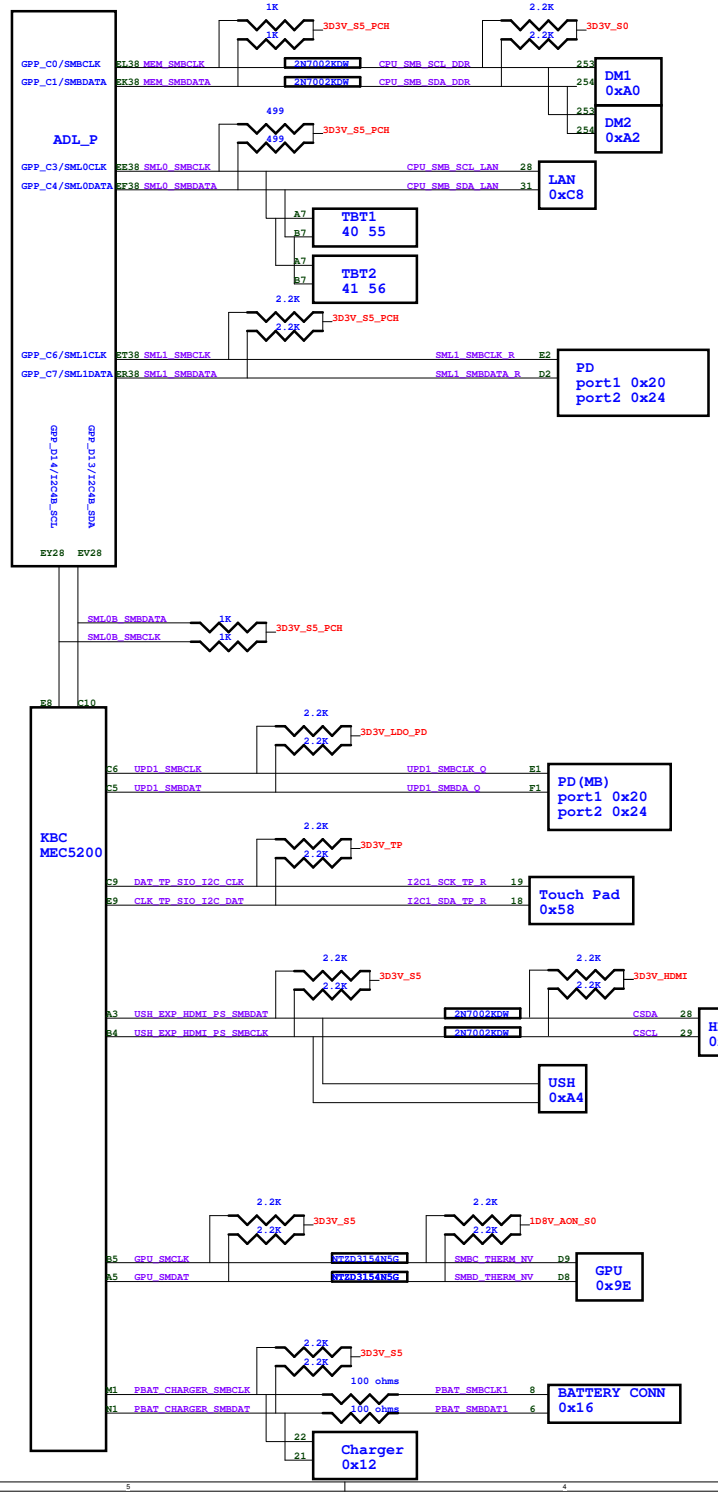
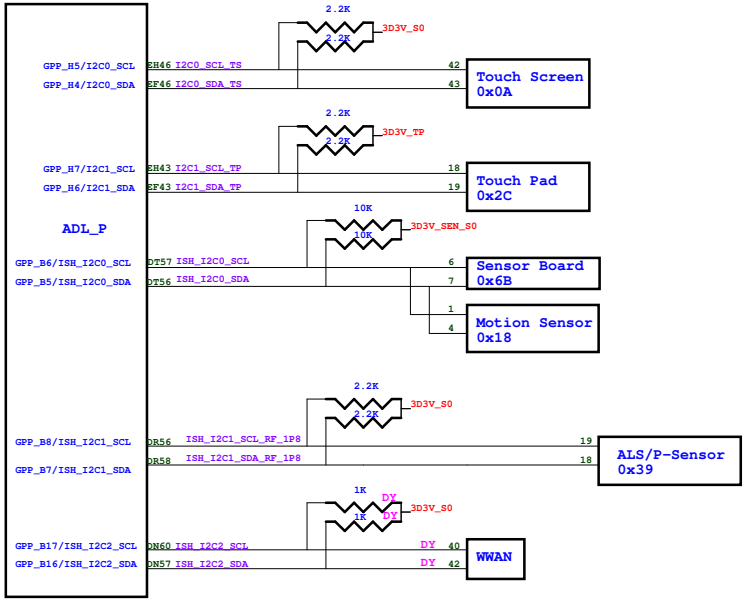
SMbus Block Diagram



I2C Block Diagram



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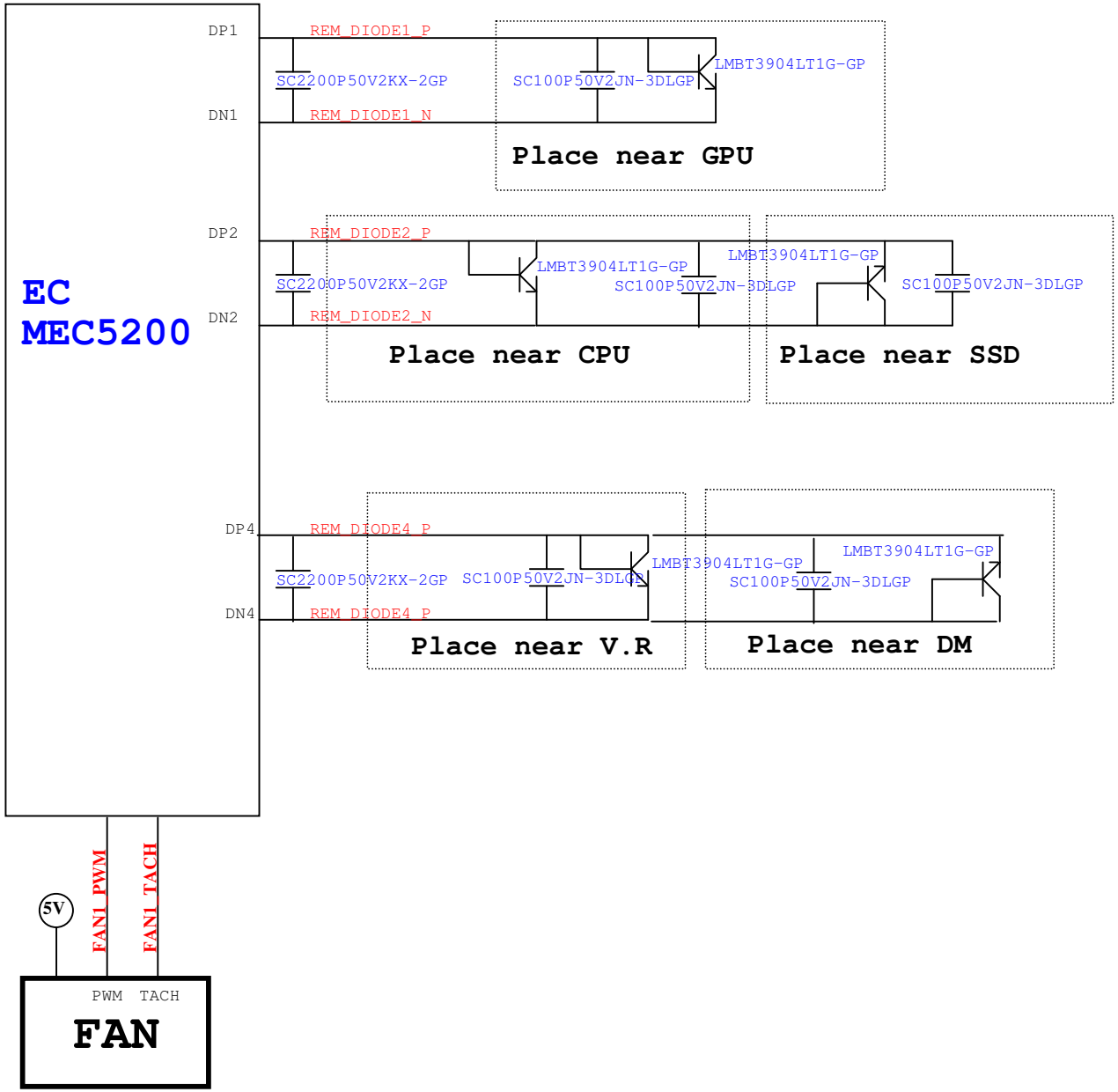
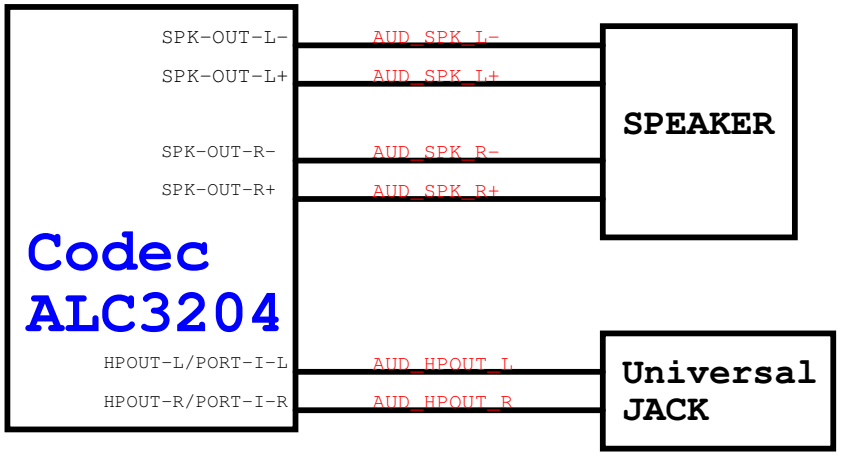
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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Title

CLK Block

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