HSF Property:ROHS

ACER

BAP41/BAP51/BAP52/BXP41/SJM52
UMA+Discrete(SW Gfx)
MAIN BOARD

2009.06.30

Tuesday, June 30, 2009		A02
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)

SIZE	CODE	DOC.NUMBER	REV
C	A02	D-CS-1310A2292001-ALG	A02

SHEET 1 of 49

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title
2. Schematic Page DESCR
3. Block Diagram
4. Annotations
5. Schematic Modify
6. Timing Diagram
7. Power Block Diagram
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9. 5VLA/5VA/3VA
10. 3VS/5VS/1.5V (DDR3)
11. 1.05VS/1.5S/1.8V/1.5VA
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13. CPU Core Power
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26. DDR3 SDRAM SO-DIMM1
27. ICH9M CPU/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD/CRT
32. KBC ITE8502E-L
33. IO CN
34. IO CN
35. IO CN
36. Audio Codec
37. EASY PORT CN/ LEVEL SHIFTER
38. M92-S2(1/5)
39. M92-S2(2/5)
40. M92-S2(3/5)
41. M92-S2(4/5)
42. M92-S2(5/5)
43. DDR3 VRAM
44. HyBrid Switch
45. dGPU Power
46. dGPU Power
47. dGPU Power
48. HDD Board
49. TPM Board

CHANGE by	Shiun-Chin Chang	DATE	Tuesday, June 30, 2009

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Schematic Page

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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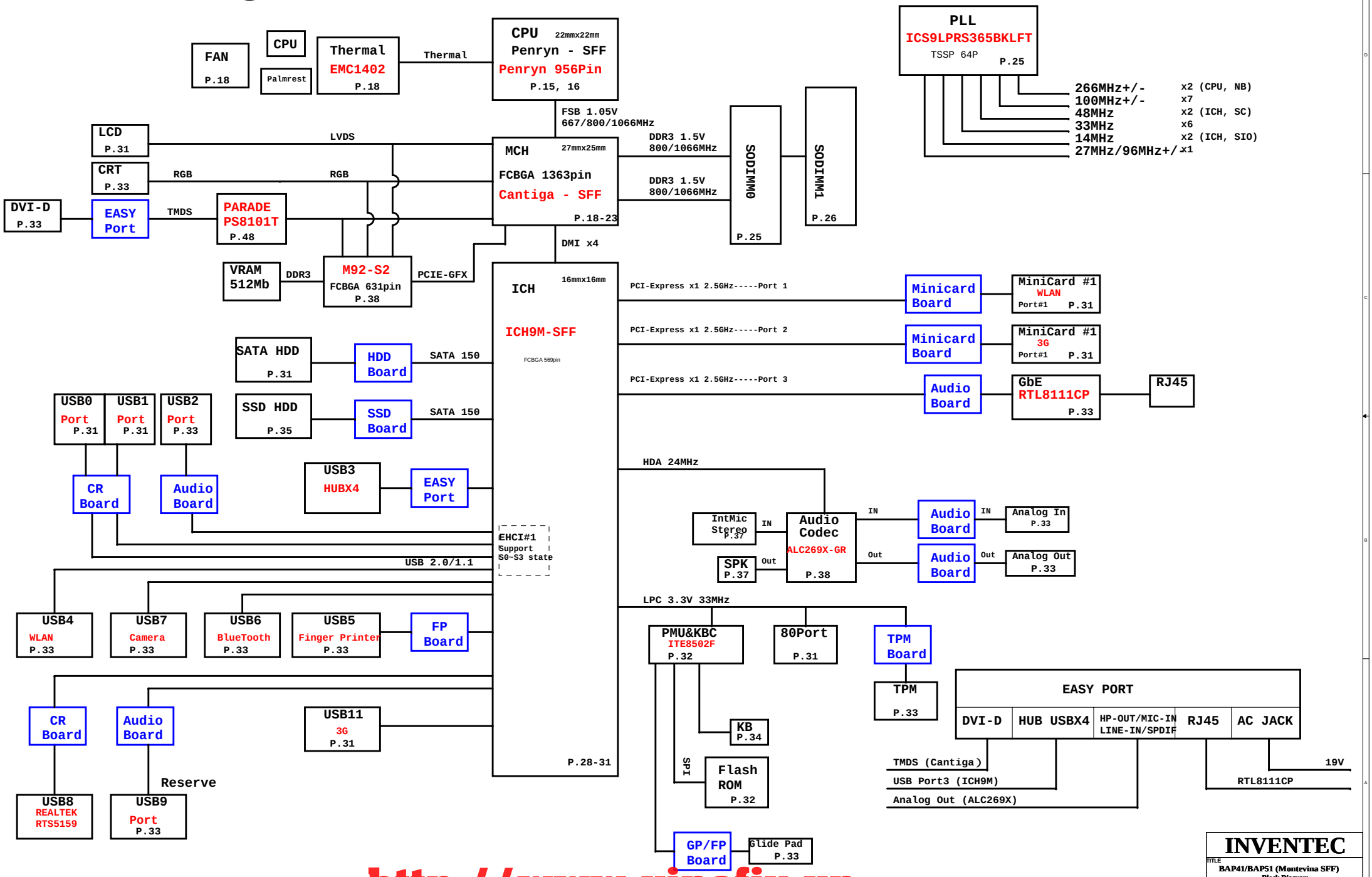
3. Block Diagram :



INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Monday, June 29, 2009 SHEET 3 of 49

4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:		
	Super I/O: IT8305E	3.0V~3.3V~3.6V	
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

CHANGE by	Shiun-Chin Chang	DATE	Monday, June 29, 2009		

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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6.Schematic modify Item and History :

CHANGE by	Shiun-Chin Chang	DATE	Monday, June 29, 2009

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)

Schematic Modify

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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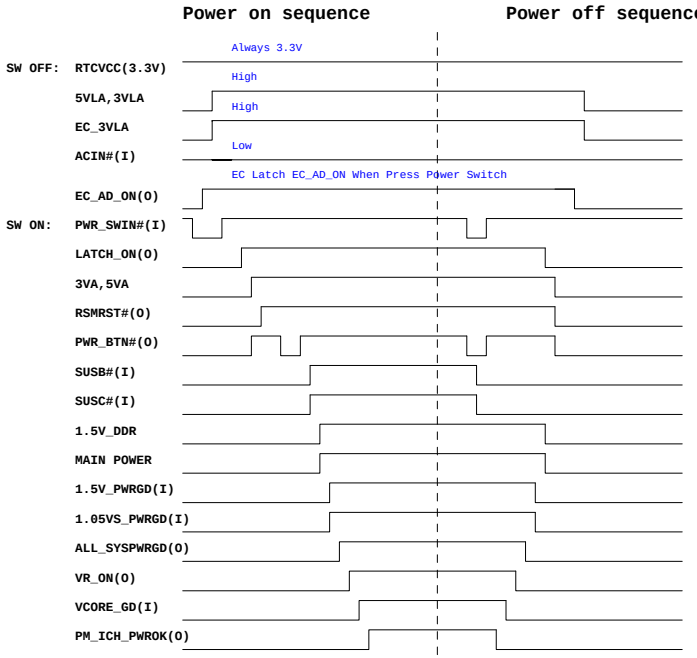
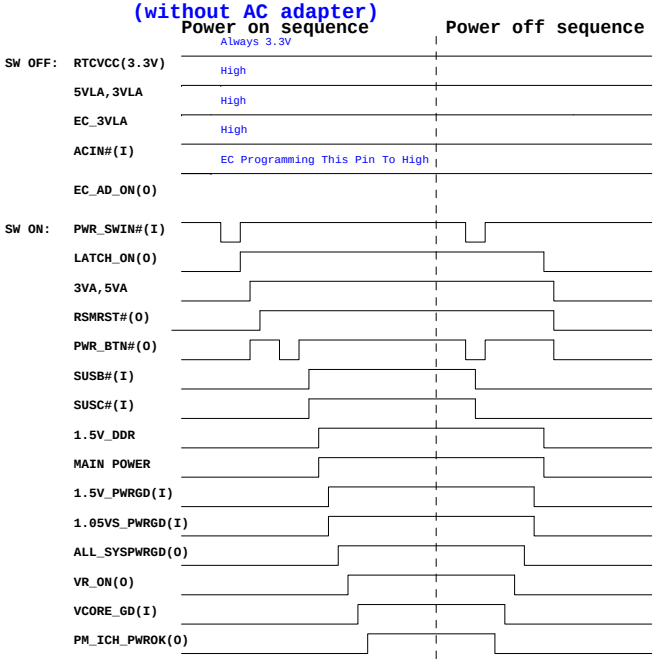
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

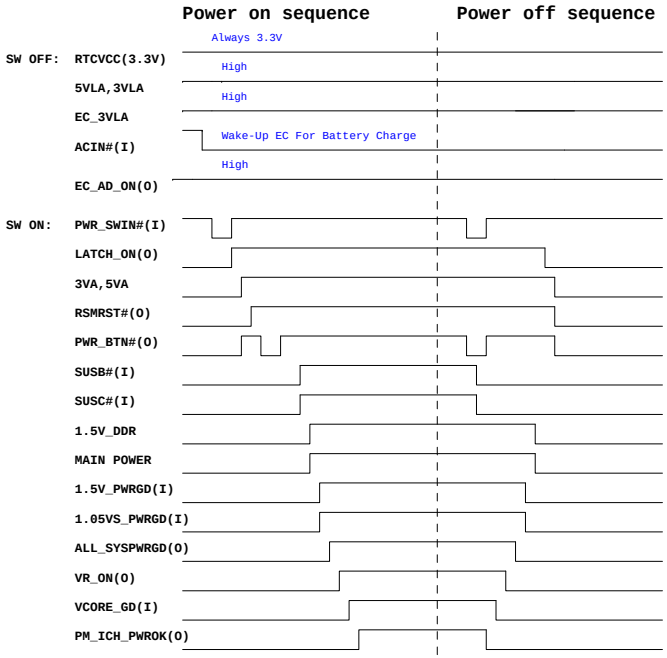
Power on/off sequence AC insert (without Battery Pack)



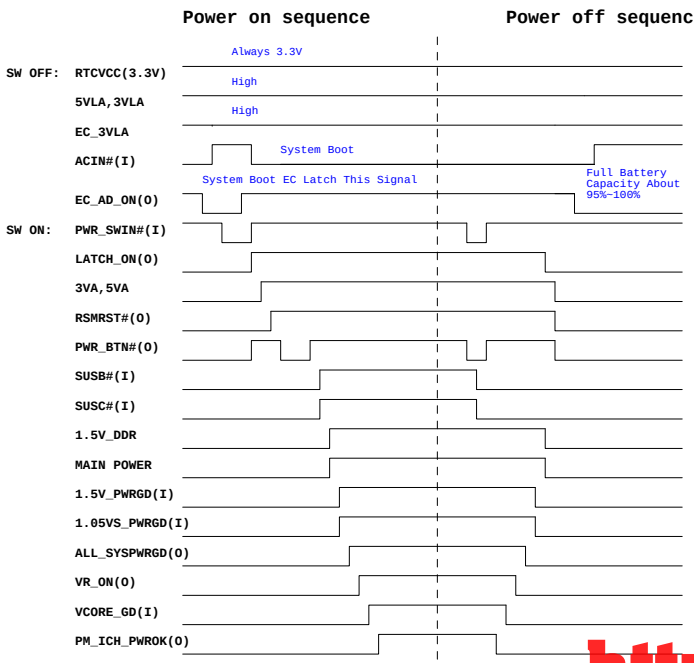
Power on/off sequence Battery insert (without AC adapter)



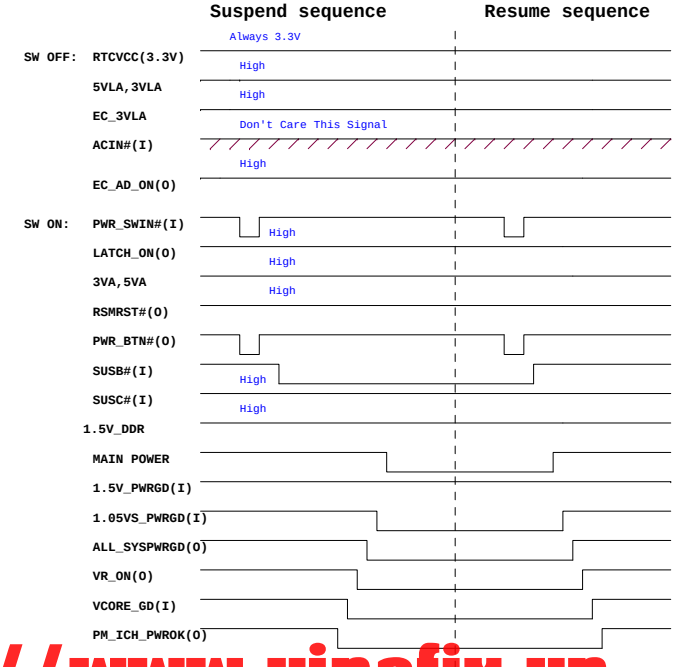
Power on/off sequence AC insert(with charge over 95%)



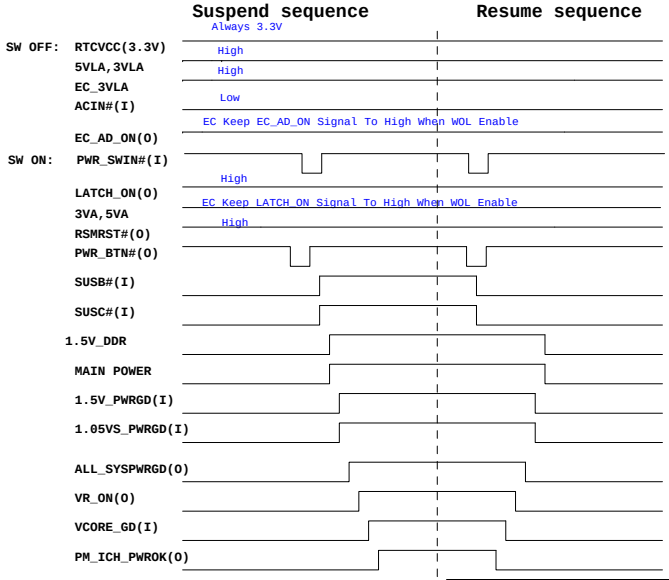
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC

TITLE
BAP41/BAP51 (Montevina SFF)
Time Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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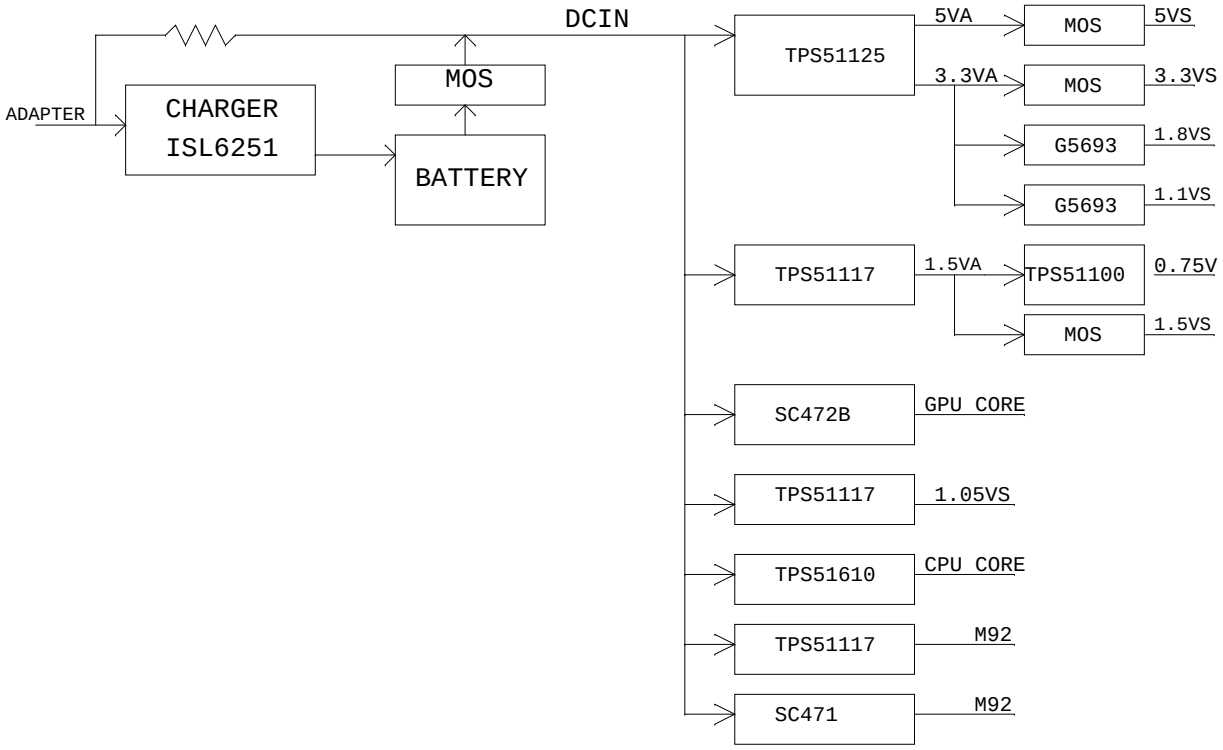
CHANGE by Shiun-Chin Chang DATE Monday, June 29, 2009

Power Block Diagram :



INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Power Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	A02	D-CS-1310A2292001-ALG	A02

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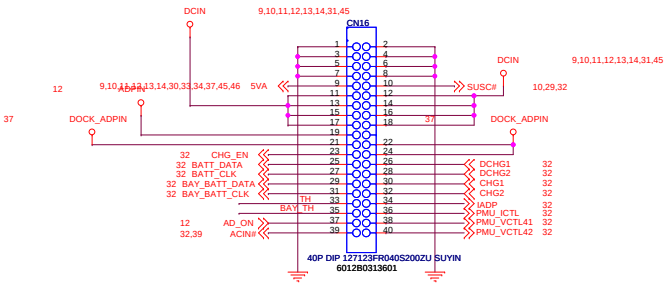
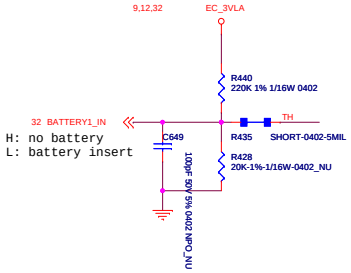
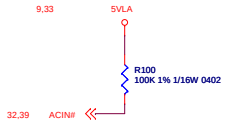
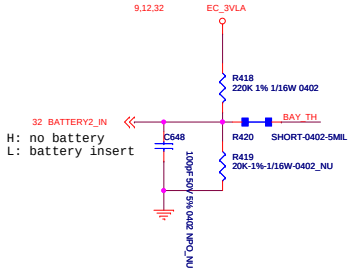
CHANGE by Shiun-Chin Chang DATE Monday, June 29, 2009

Charger CN TO USIM/B









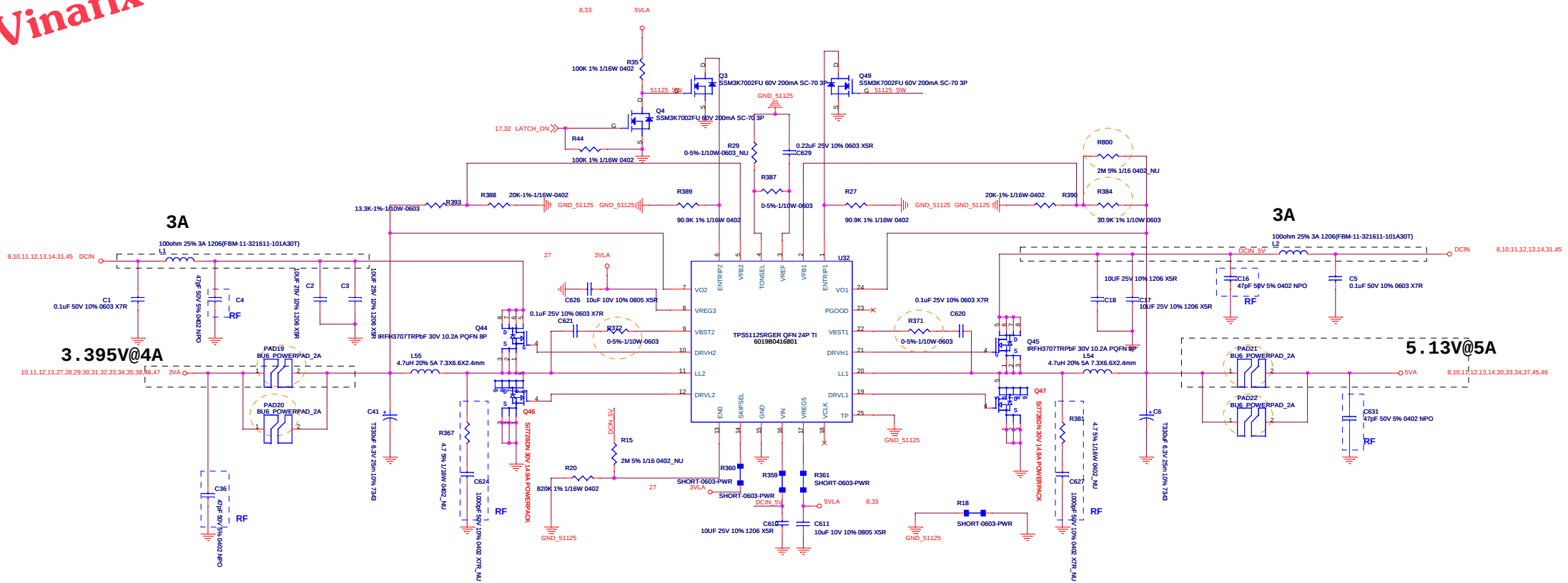
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)

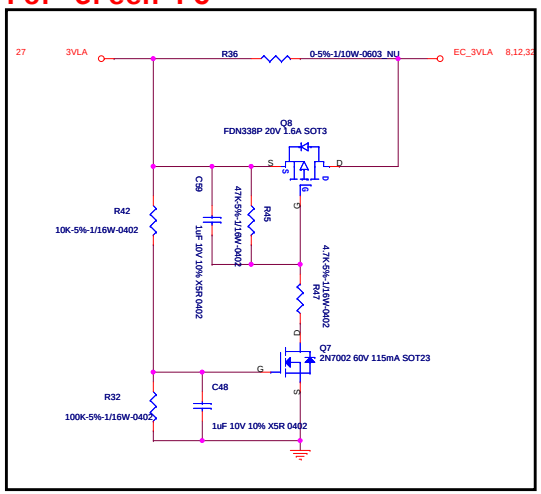
Adaptor in / Charge

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

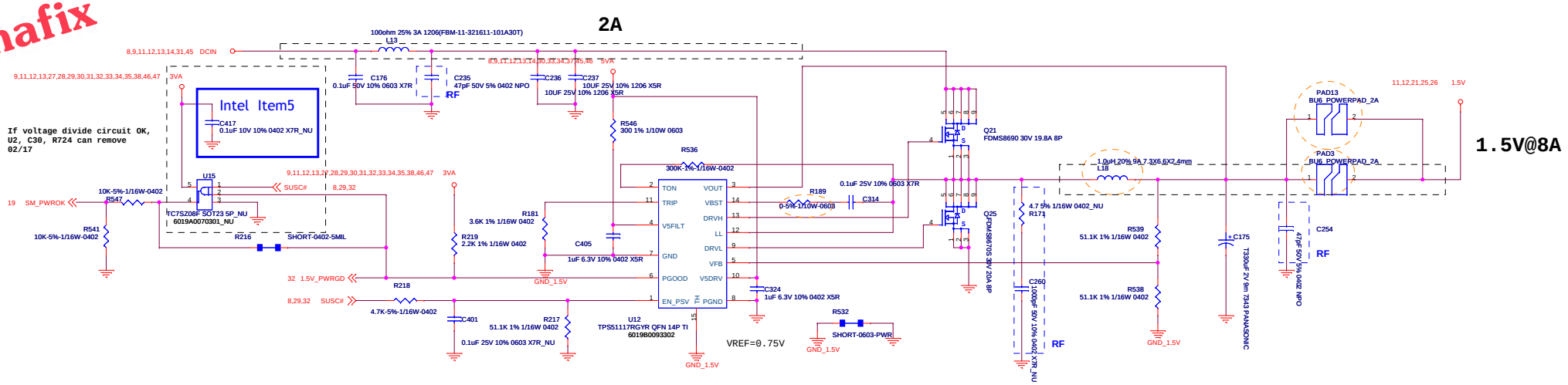
CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 8 of 49

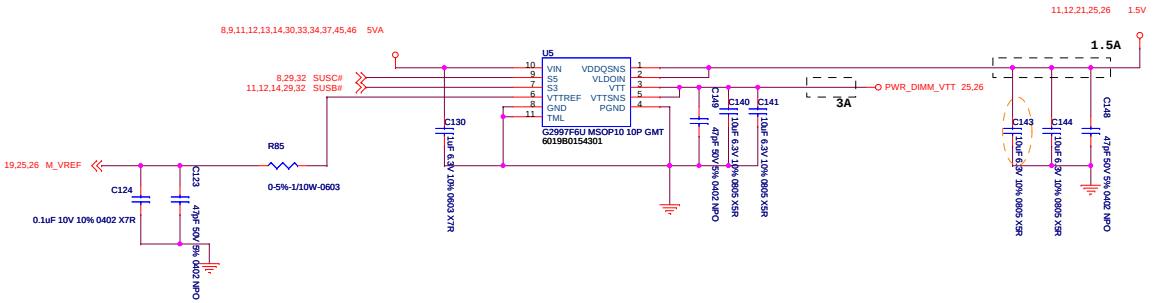


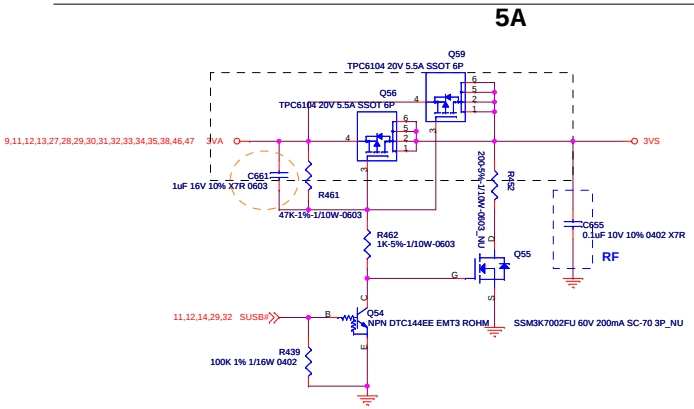
For Green PC

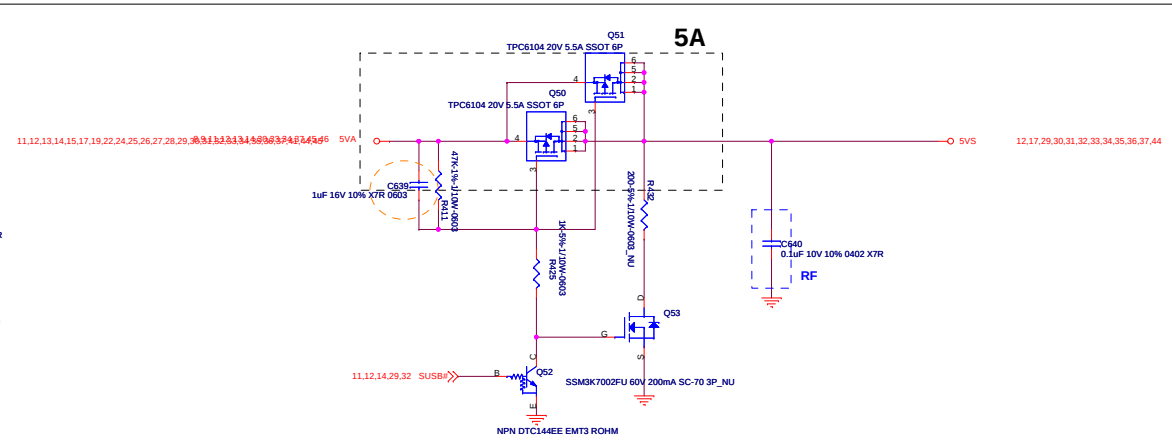


TITLE	INVENTEC
	BAP41/BAP51 (Montevina SFF)
	5VLA/5VA/3VLA/3VA
SIZE	Custom
CODE	A02
DOC.NUMBER	D-CS-1310A2292001-ALG
REV	A02
CHANGE by	Shiun-Chin Chang
DATE	Thursday, July 02, 2009
SHEET	9 of 49

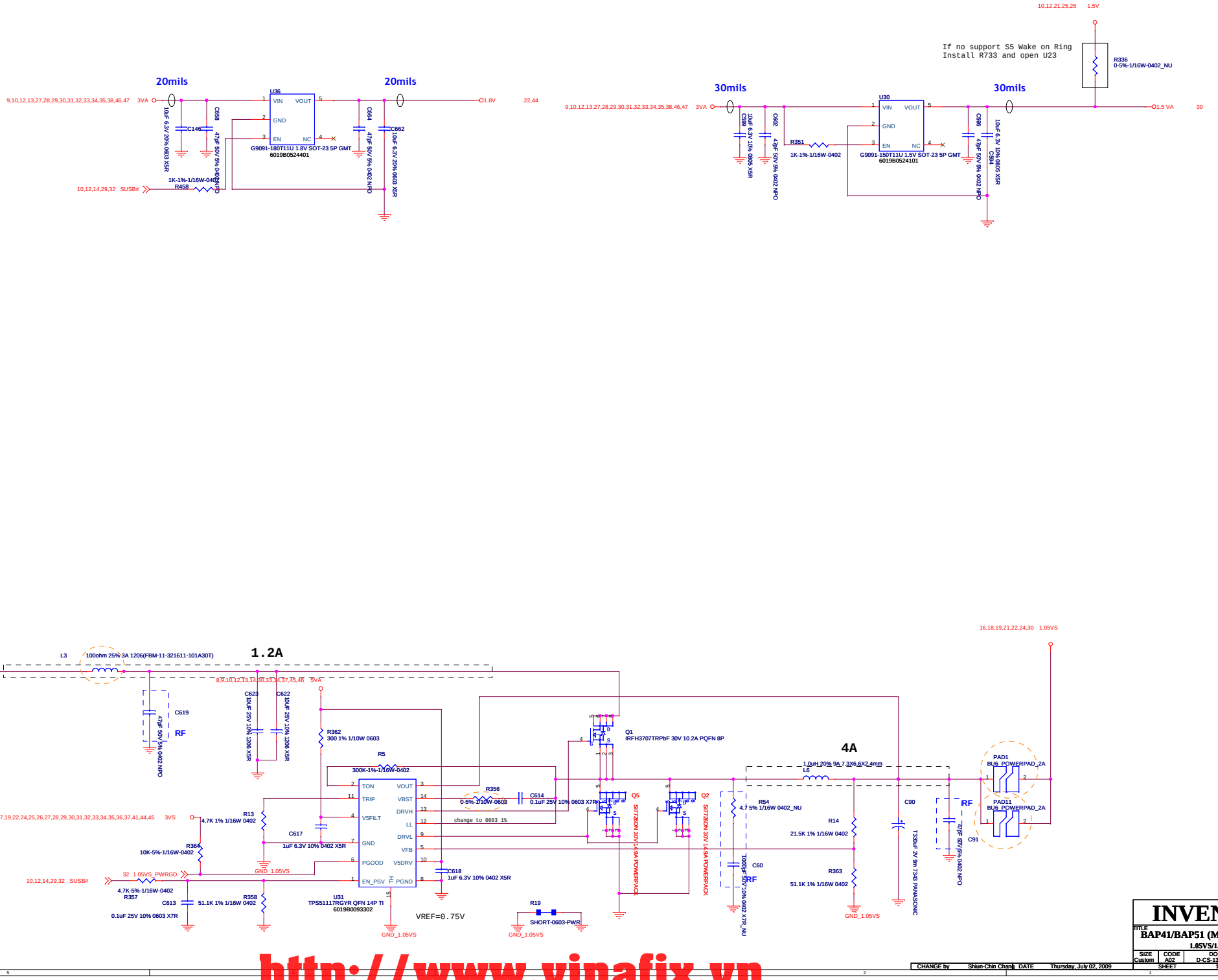








INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) 3VS/5VS/1.5V (DDR3)			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 10 of 49	



CHANGE by	Shiun-Chin Chang	DATE	Thursday, July 02, 2009

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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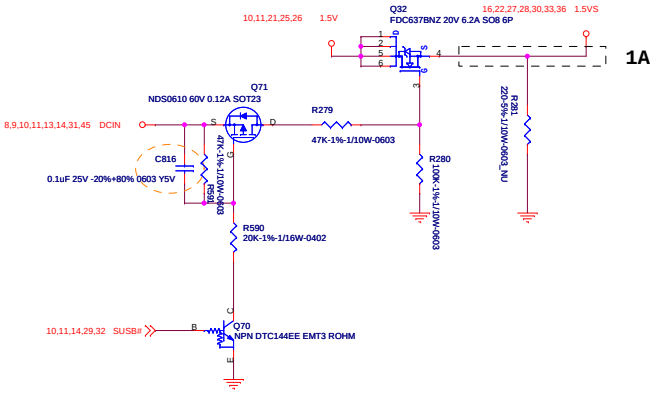
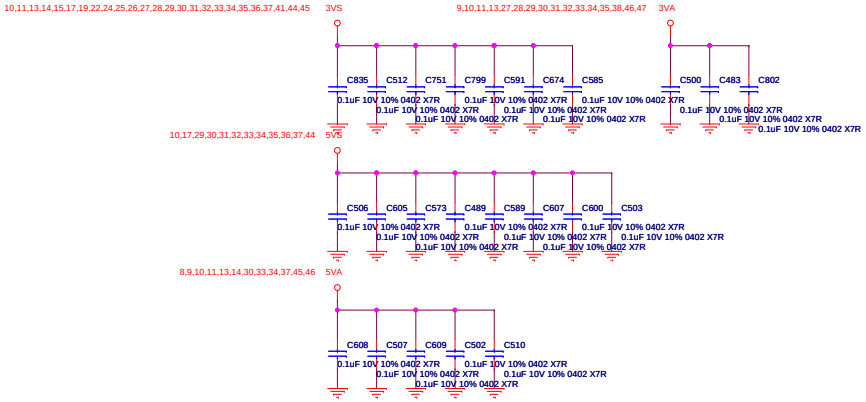
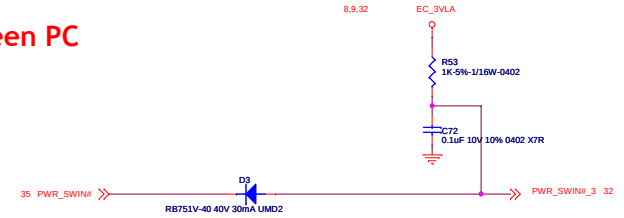
1.5VS



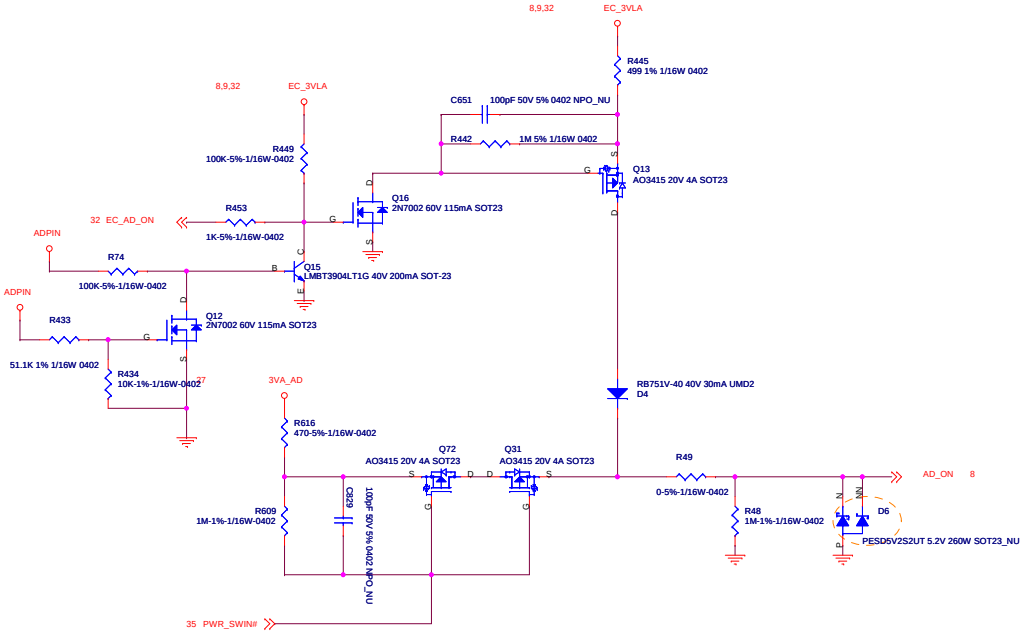
EMI Cap

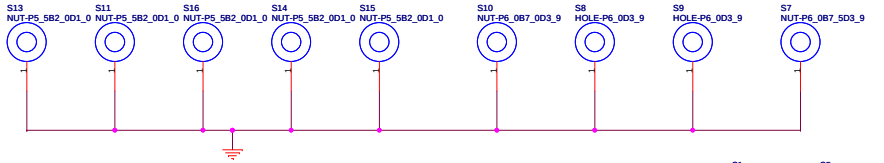


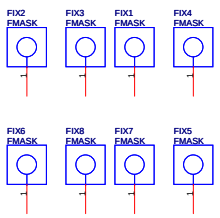
For Green PC

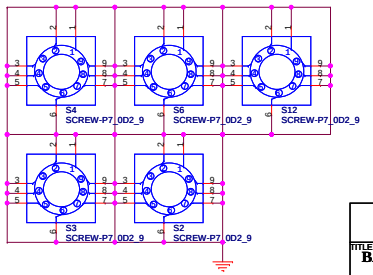


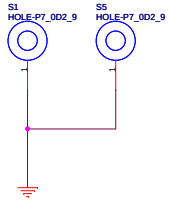
None Green PC ---- NU









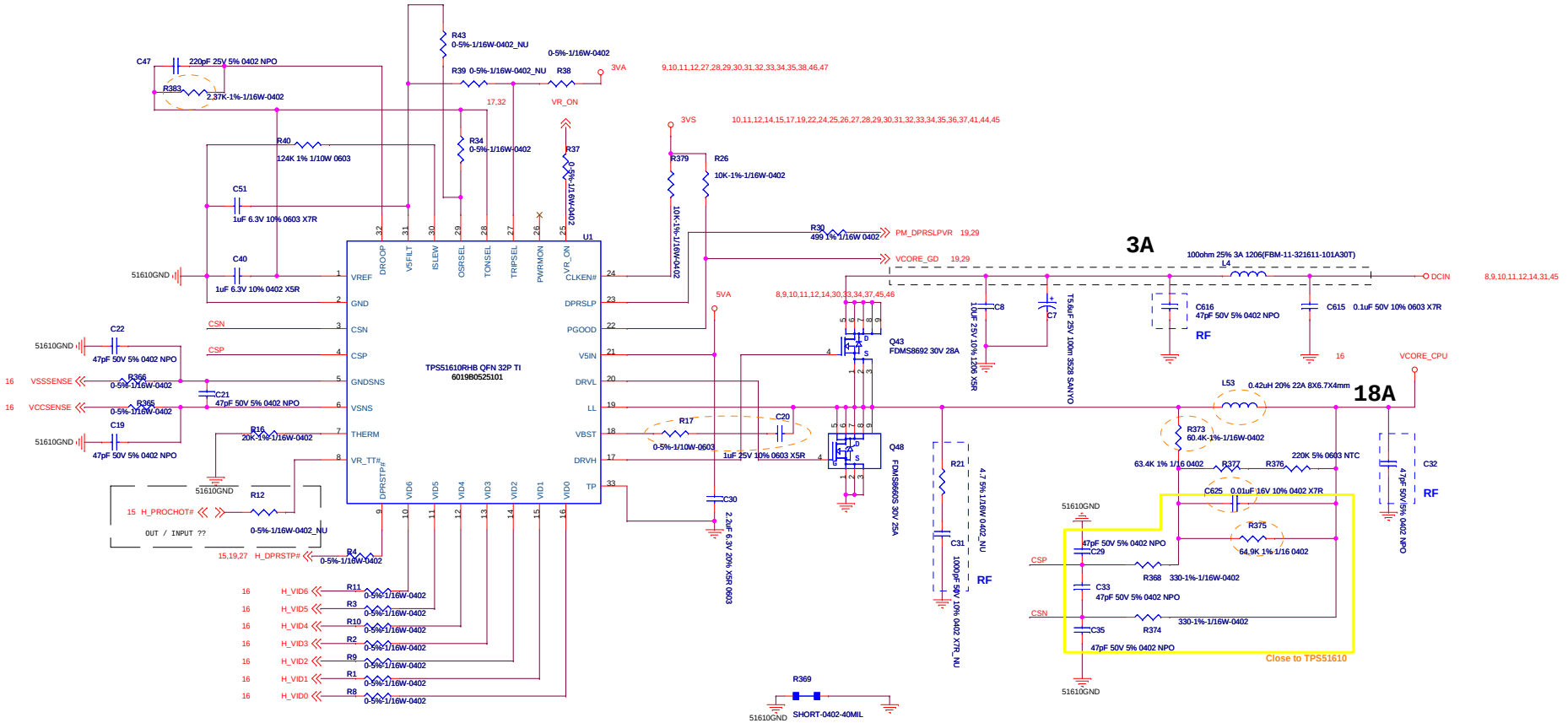


INVENTEC

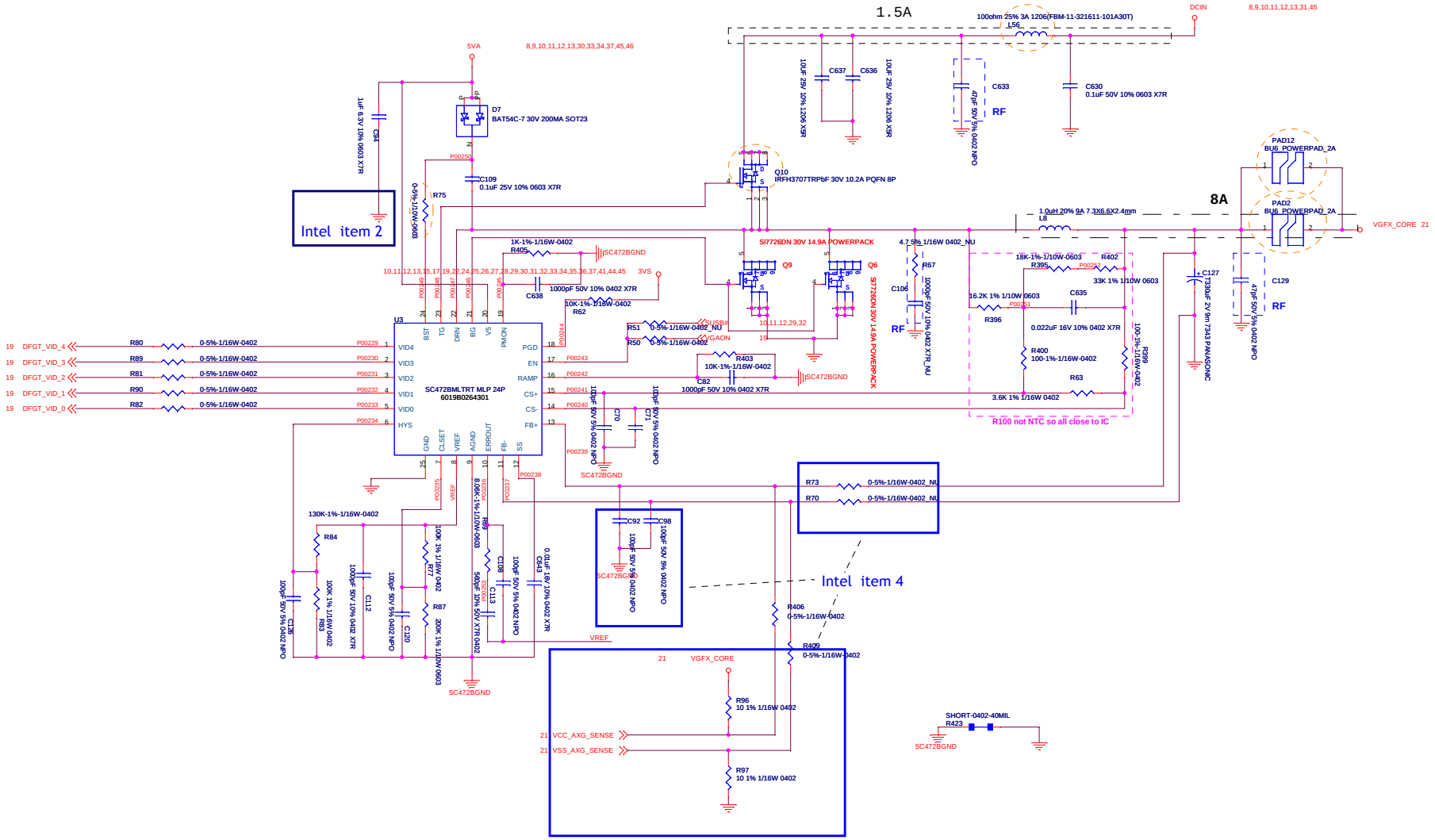
TITLE: BAP41/BAP51 (Montevina SFF)
Power on latch

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

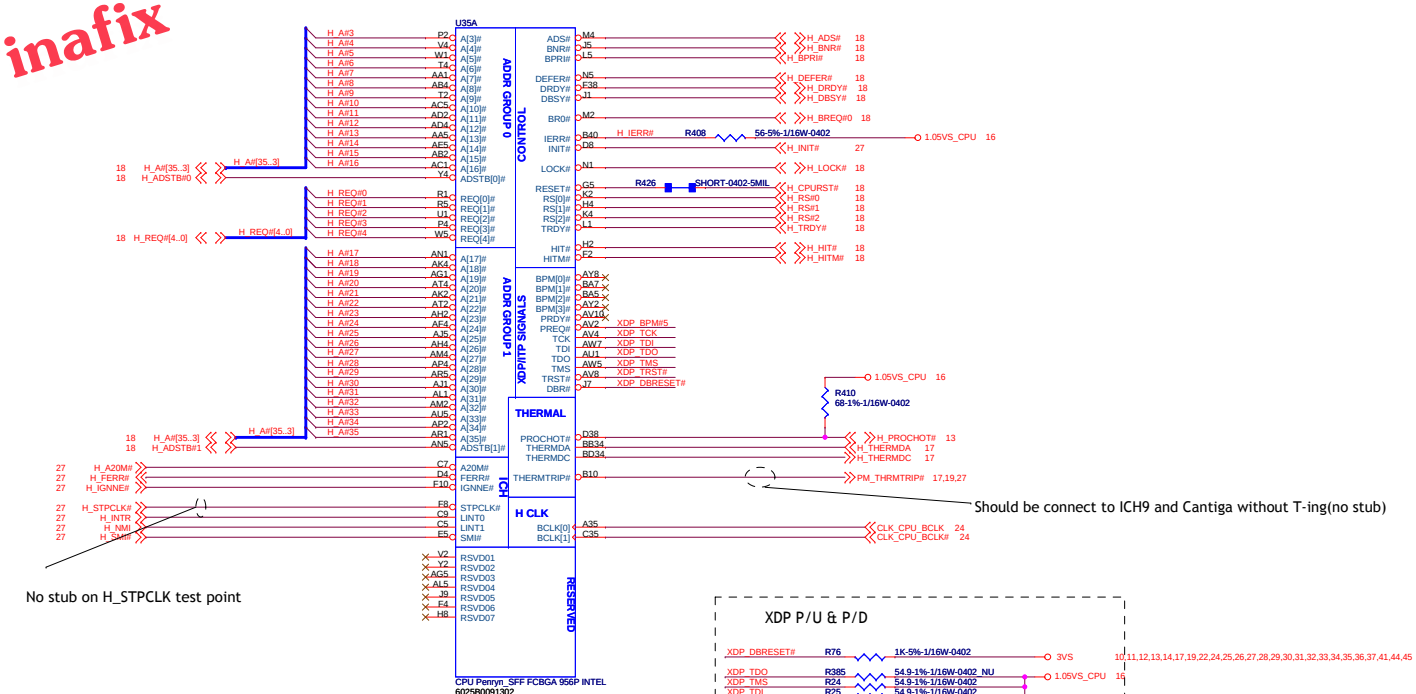
CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 12 of 49



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) CPU Core Power			
SIZE: C	CODE: A02	DOC NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 13 of 49	



TITLE	INVENTEC
	BAP41/BAP51 (Montevina SFF)
	GPU CORE
SIZE	Custom
CODE	A02
DOC.NUMBER	D-CS-1310A2292001-ALG
REV	A02
CHANGE by	Shiun-Chin Chang
DATE	Thursday, July 02, 2009
SHEET	14 of 49

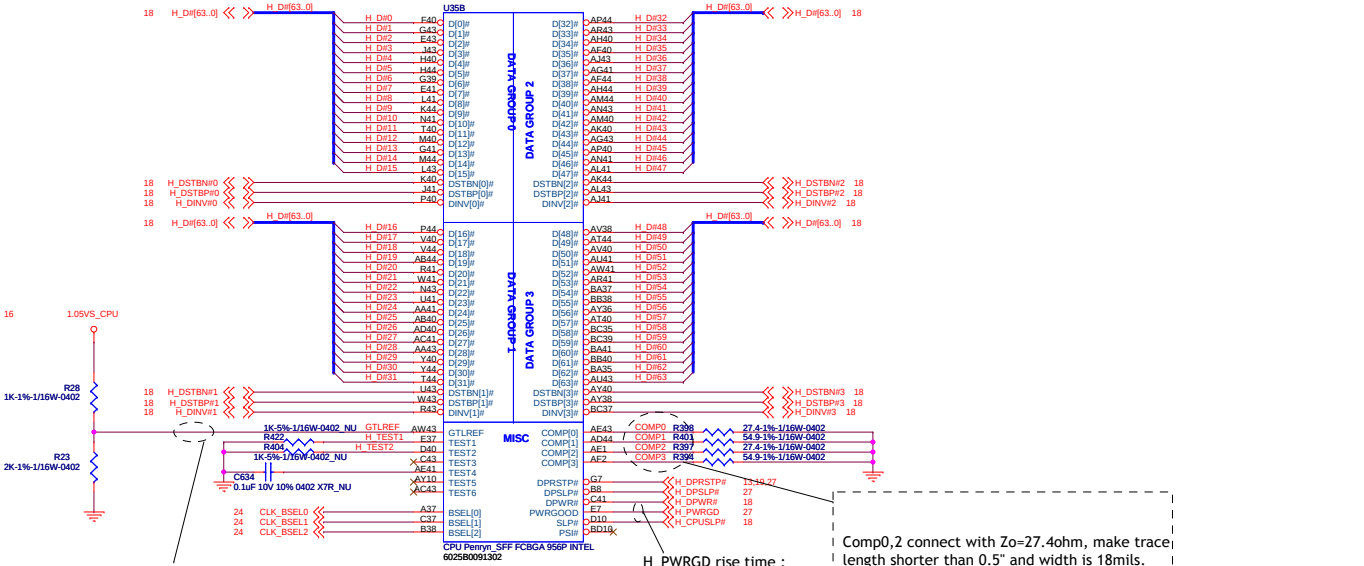


No stub on H_STPCLK test point

Should be connect to ICH9 and Cantiga without T-ing(no stub)

Rout to TP via and place gnd via w/in 100mils

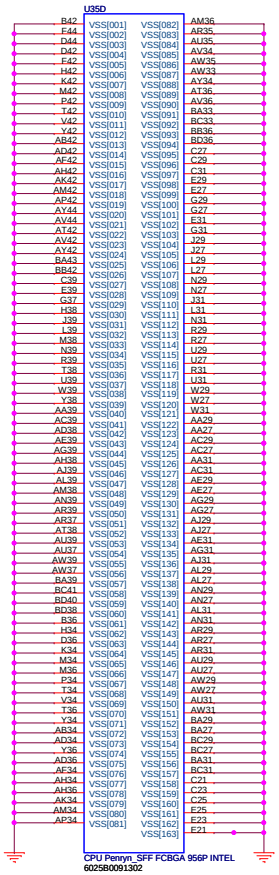
A#[32-39], APM#[0-1]:Leave escape routing on for future functionality

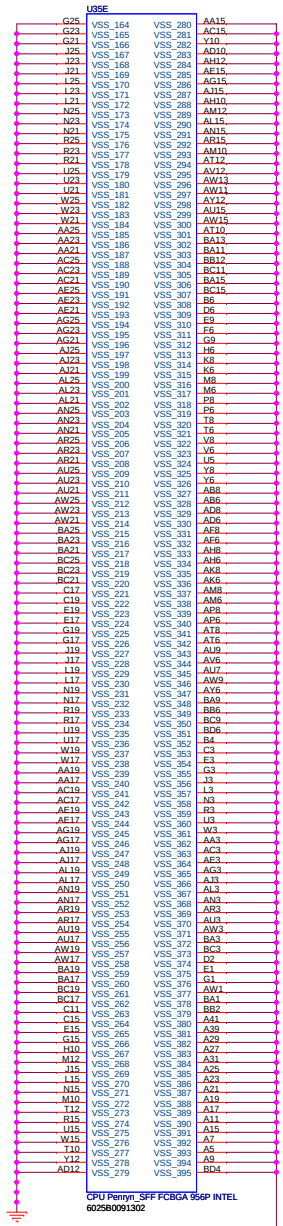


Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.
Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals.

H_PWRGD rise time :
Max : 15ns

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils



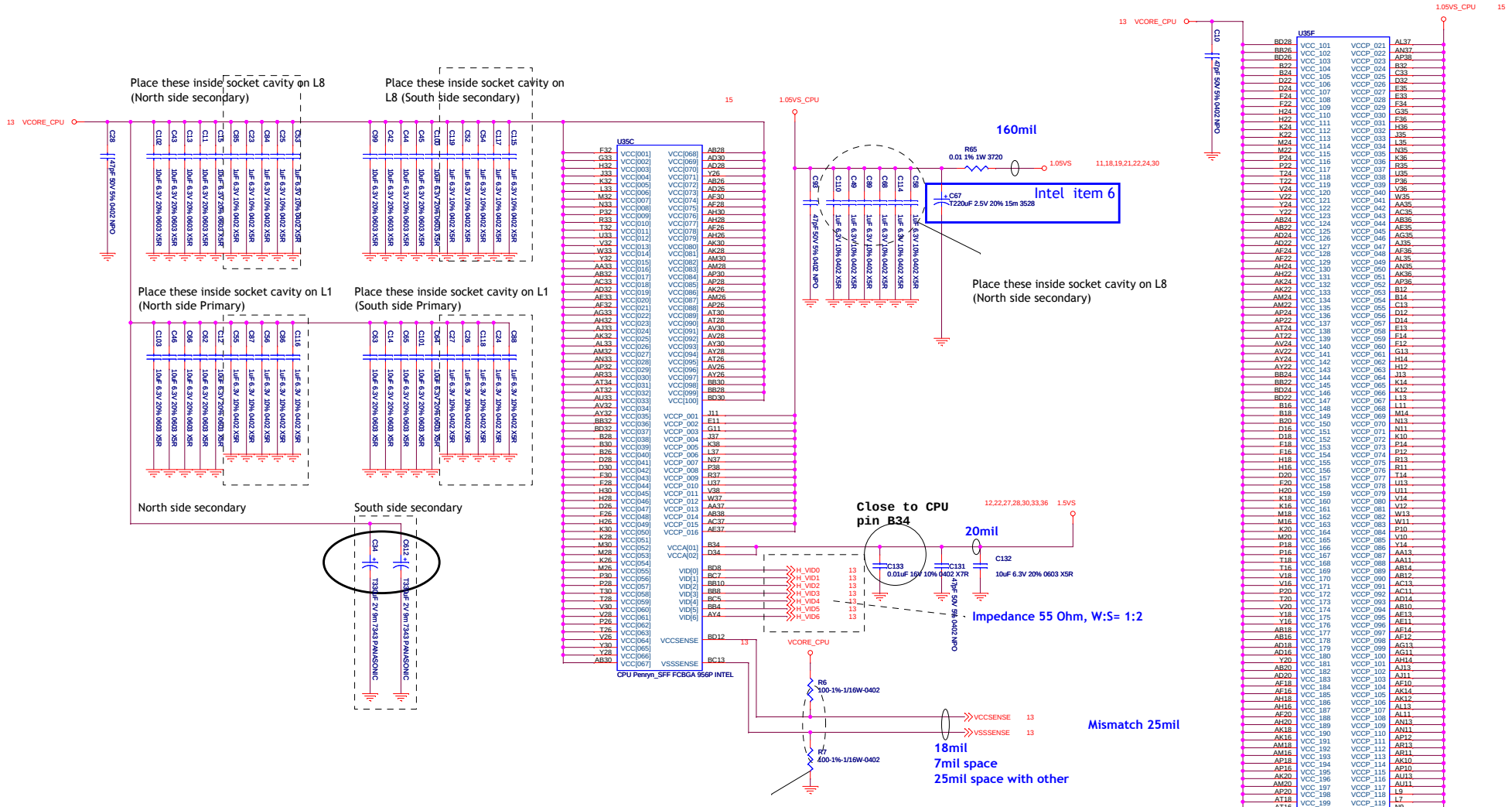


INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Penryn Processor(1/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 15 of 49



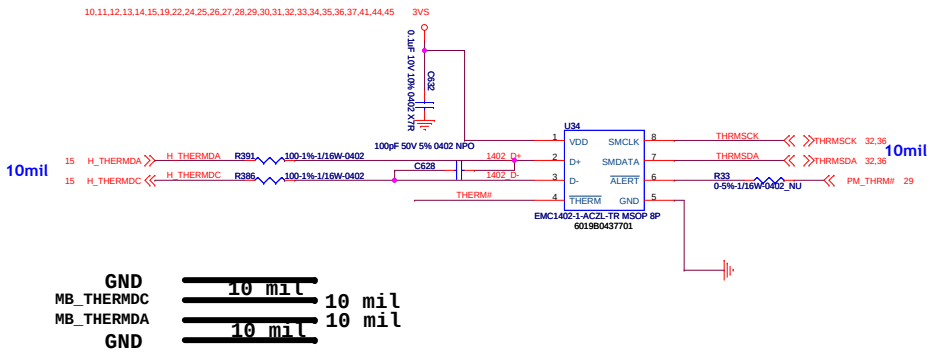
INVENTEC

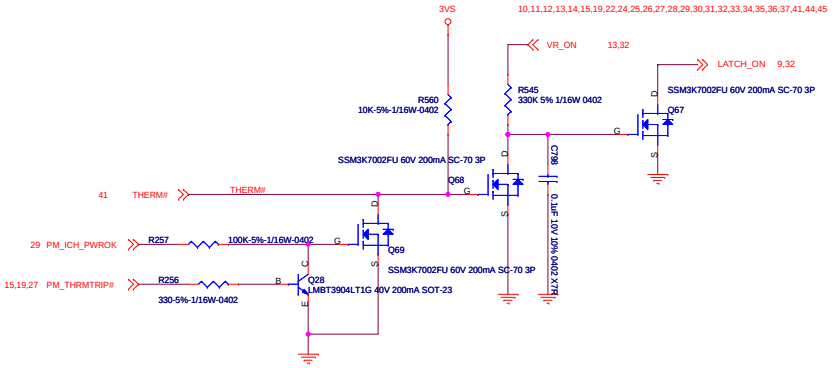
TITLE: BAP41/BAP51 (Montevina SFF)
Penryn Processor(2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

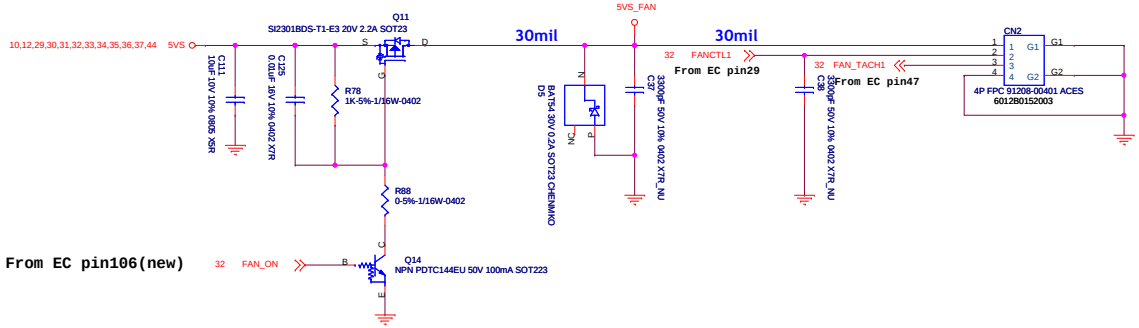
CHANGE by: Shiun-Chin Chang | DATE: Thursday, July 02, 2009 | SHEET 16 of 49

THERMAL SENSOR

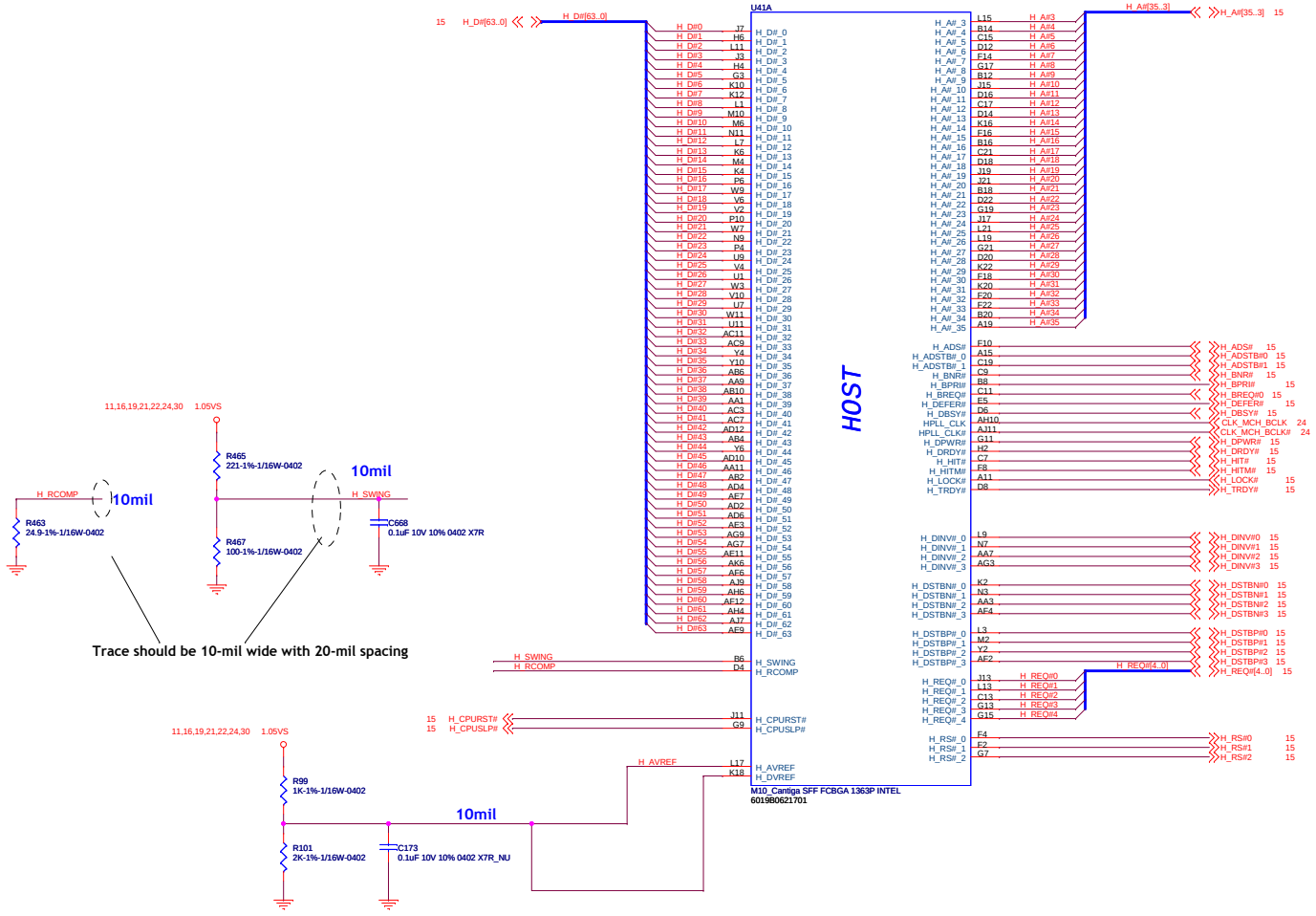




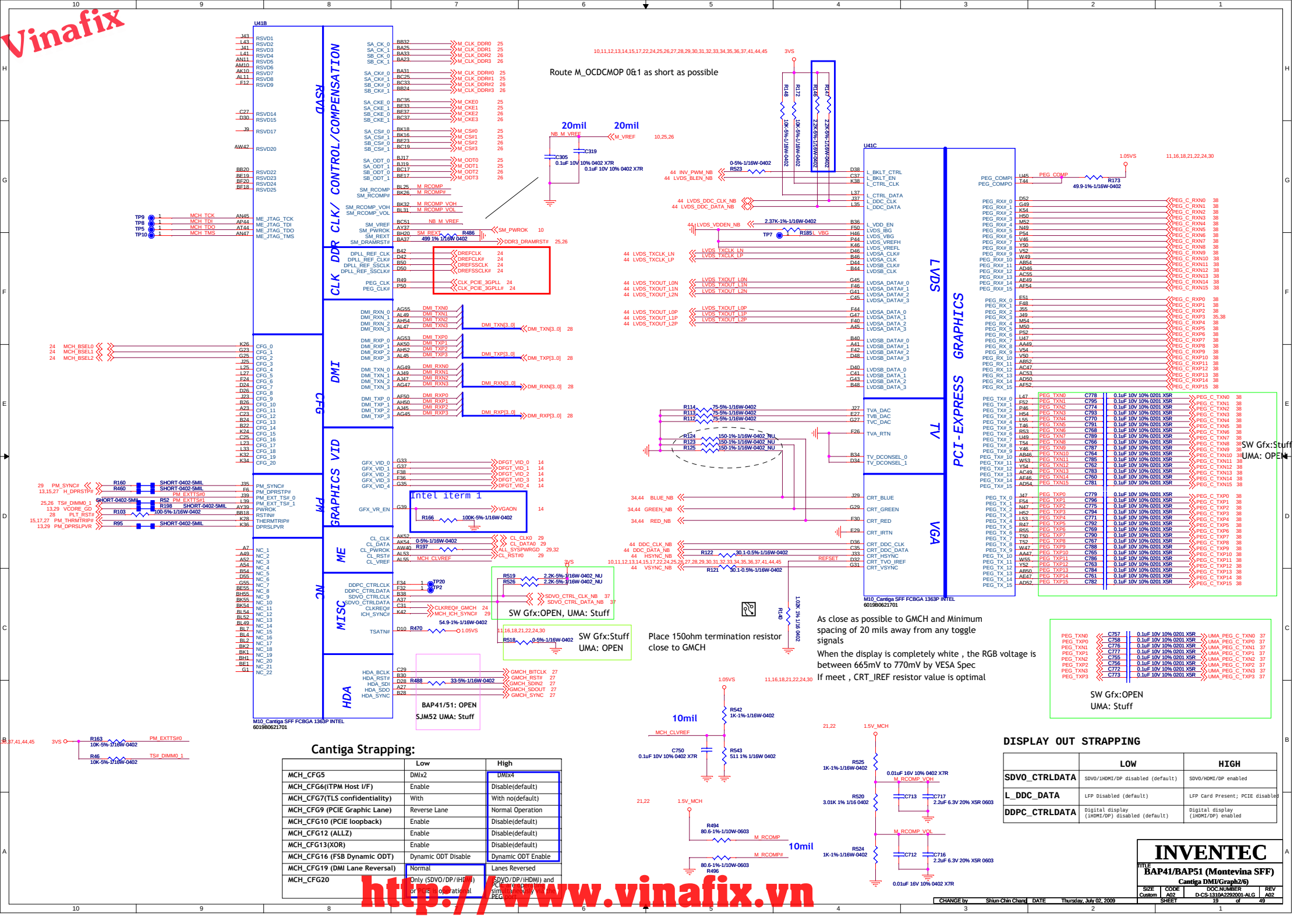
Fan control



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) CPU Thermal			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 17 of 49	



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF)			
Cantiga Host(1/6)			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 18 of 49	



Cantiga Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only (SDVO/DP/iHDMI) or PCIE for operational	(SDVO/DP/iHDMI) and PCIE can be simultaneously operational

DISPLAY OUT STRAPPING

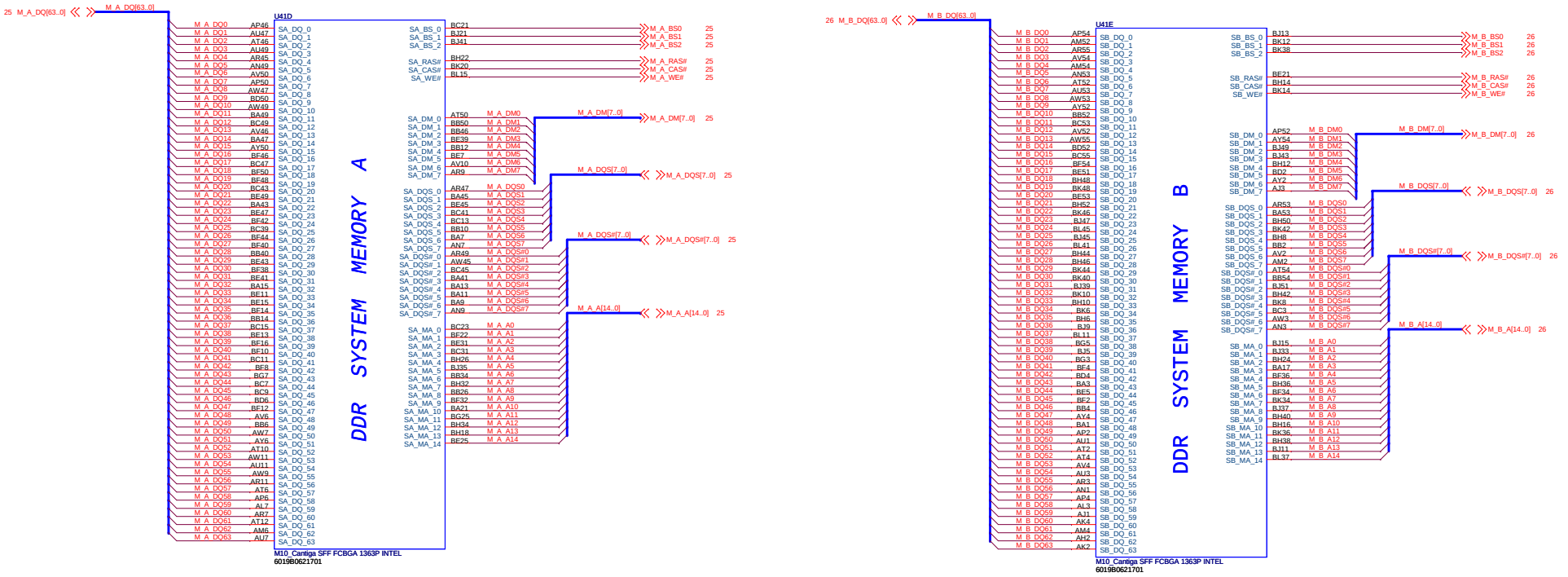
	LOW	HIGH
SDVO_CTRLDATA	SDVO/iHDMI/DP disabled (default)	SDVO/HDMI/DP enabled
L_DDC_DATA	LFP Disabled (default)	LFP Card Present; PCIE disabled
DDPC_CTRLDATA	Digital display (iHDMI/DP) disabled (default)	Digital display (iHDMI/DP) enabled

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Cantiga DMI/Graph2/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2290001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 19 of 49

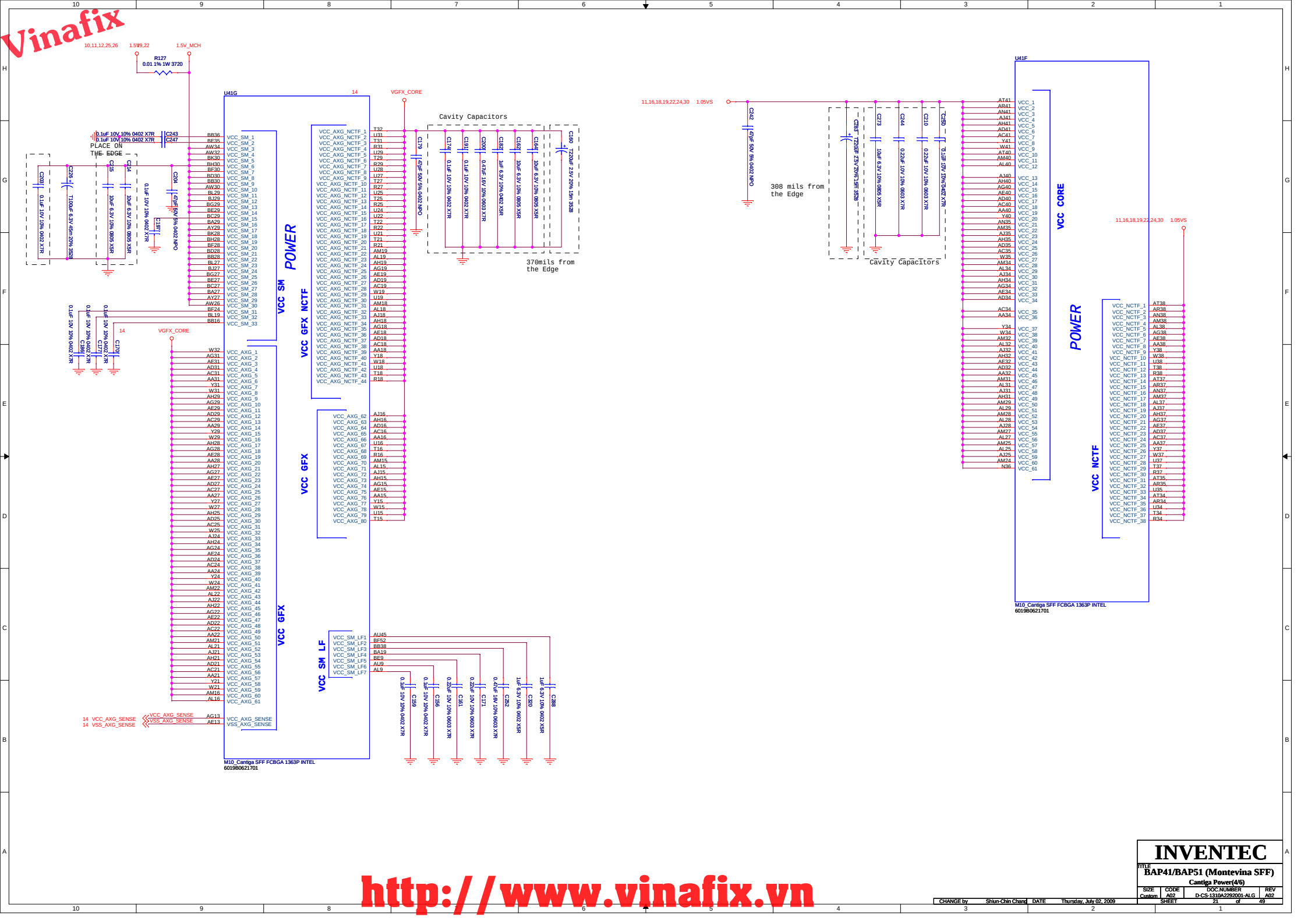


INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Cantiga DDR3(3/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 20 of 49



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF)			
Cantiga Power(4/6)			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 21 of 49	

0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils

11,16,18,19,21,24,30 1.05VS

30mil

L27 100ohm 25% 2A 0.1ohm 0603 — (64.8mA) 10mil — 1.05VS_DPLLA
C290 10uF 6.3V 10% 0805 X5R — C284 0.1uF 10V 10% 0402 X7R

L29 100ohm 25% 2A 0.1ohm 0603 — (64.8mA) 10mil — 1.05VS_DPLLB
C245 10uF 6.3V 10% 0805 X5R — C304 0.1uF 10V 10% 0402 X7R

L12 100ohm 25% 2A 0.1ohm 0603 — (24mA) 10mil — 1.05VS_HPLL
C157 4.7uF 6.3V 10% 0603 X5R — C158 0.1uF 10V 10% 0402 X7R

L57 100ohm 25% 2A 0.1ohm 0603 — (139.2mA) 10mil — 1.05VS_MPLL
C652 10uF 6.3V 10% 0805 X5R — C656 0.1uF 10V 10% 0402 X7R

L26 100ohm 25% 2A 0.1ohm 0603 — 10mil — 1.05VS_PEGPLL
C292 10uF 6.3V 10% 0805 X5R — C263 0.1uF 10V 10% 0402 X7R

12,16,27,28,30,33,36 1.5VS

R118 0-5%-1/10W-0603 — (35mA) 10mil — 1.5VS_TVDAC
C199 0.1uF 10V 10% 0402 X7R — C213 0.01uF 16V 10% 0402 X7R

L15 180ohm 25% 1.5A 0603(FBM-11-160808-181A15T) — (0.5mA) 10mil — 1.5VS_QDAC
C217 0.1uF 10V 10% 0402 X7R — C234 0.01uF 16V 10% 0402 X7R

Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36,37,41,44,45

R156 0-5%-1/10W-0603 — (120mA) 10mil — VCCS_TVDACA
C239 0.1uF 10V 10% 0402 X7R — C230 0.01uF 16V 10% 0402 X7R

3VDDM_TVDAC should be within 250mils of edge

Vout
R1 Vout=Vref(1+R2/R1)+Iadj*R2
R2=R1(Vout/Vref-1)
FB 1117 Vref=1.250V,Iadj=55uA
R2
GND

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36,37,41,44,45

L19 180ohm 25% 1.5A 0603(FBM-11-160808-181A15T)

(73mA) 20mil — C205 0.01uF 16V 10% 0402 X7R — C206 0.1uF 10V 10% 0402 X7R — J31 VCCA_CRT_DAC
(5mA) 20mil — C229 0.01uF 16V 10% 0402 X7R — C228 0.1uF 10V 10% 0402 X7R — L31 M33 VCCA_DAC_BG VSSA_DAC_BG

CRT

1.05VS_DPLLA J45 VCCA_DPLLA
1.05VS_DPLLB L49 VCCA_DPLLB
1.05VS_HPLL AF10 VCCA_HPLL
1.05VS_MPLL AE1 VCCA_MPLL

PLL

1.8V_TXLVDS — C258 1000pF 50V 10% 0402 X7R — (10mA) — U43 U41 VCCA_LVDS1 VCCA_LVDS2 V44 VSSA_LVDS

LVDS

12,16,27,28,30,33,36 1.5VS — C264 0.1uF 10V 10% 0402 X7R — (0.414mA) — AJ43 VCCA_PEG_BG
1.05VS_PEGPLL — (50mA) — AG43 VCCA_PEG_PLL

PEG A

11,16,18,19,21,24,30 1.05VS — (747.5mA)
C183 10uF 6.3V 10% 0805 X5R — C172 4.7uF 6.3V 10% 0603 X5R — C157 10uF 6.3V 10% 0805 X5R — C185 1uF 6.3V 10% 0402 X5R

AW24 AU24 AW22 AU22 AU21 AW20 AU19 AW18 AU18 AW16 AU16 AT16 AR16 AU15 AT15 AR15 AW14 VCCA_SM_1 … VCCA_SM_17

A SM

AT24 AR24 AT22 AR22 AT21 AR21 AT19 AR19 AT18 AR18 VCCA_SM_NCTF_1 … VCCA_SM_NCTF_10

POWER

11,16,18,19,21,24,30 1.05VS — (37.95mA)
C183 10uF 6.3V 10% 0805 X5R — C235 4.7uF 6.3V 10% 0603 X5R — C189 0.1uF 10V 10% 0402 X7R

AU27 AU28 AU29 AU31 AT31 AR31 AT29 AR29 AT28 AR28 AT27 AR27 VCCA_SM_CK_4 … VCCA_SM_CK_1
VCCA_SM_CK_NCTF_1 … VCCA_SM_CK_NCTF_8

11,16,18,19,21,24,30 1.05VS — (157.2mA)
C165 0.1uF 10V 10% 0402 X7R — AH12 VCCD_HPLL — AE43 VCCD_PEG_PLL
1.05VS_PEGPLL — C278 0.1uF 10V 10% 0402 X7R — (50mA) — M46 L45 VCCD_LVDS_1 VCCD_LVDS_2

11,44 1.8V — (30mA) — C289 1uF 6.3V 10% 0402 X5R

M10_Cantiga SFF FCBGA 1363P INTEL
6019B0621701

(852mA) — 11,16,18,19,21,24,30 1.05VS
C363 4.7uF 6.3V 10% 0603 X5R — C367 4.7uF 6.3V 10% 0603 X5R — C153 2.2uF 6.3V 10% 0603 X7R — C154 0.47uF 10V 10% 0603 X5R — PLACE ON THE EDGE
C142 T100uF 6.3V 45m 20% 3528_NU — GM OPEN

VTT_1 T12 VTT_2 R11 VTT_3 T10 VTT_4 R9 VTT_5 T8 VTT_6 R7 VTT_7 T6 VTT_8 R5 VTT_9 T4 VTT_10 R3 VTT_11 T2 VTT_12 VTT_13 R1

VTT

(79mA) 10mil — K30 VCCS_TVDACA

TV

(50mA) — A31 VCC_HDA — R508 0-5%-1/16W-0402_NU — 1.5VS — 12,16,27,28,30,33,36
R507 0-5%-1/16W-0402 — C706 0.1uF 10V 10% 0402 X7R_NU

HDA

w/ iHDMI: 1.5VS (SJM52)
w/o iHDMI: GND (BAP41/BAP51)

TV/CRT

N34 1.5VS_QDAC
N32 1.5VS_TVDAC

30mil (440mA) — 1uF 6.3V 10% 0402 X5R — 1.05VS — 11,16,18,19,21,24,30
C184 — C192 10uF 6.3V 10% 0805 X5R_NU

30mil (149.5mA) — 0.1uF 10V 10% 0402 X7R — L14 100ohm 25% 2A 0.1ohm 0603 — 1.5V_MCH — 19,21
C187 — C188 10uF 6.3V 10% 0805 X5R

AXF

M25 VCC_AXF_1
N24 VCC_AXF_2
M23 VCC_AXF_3

BK24 VCC_SM_CK_1
BL23 VCC_SM_CK_2
BJ23 VCC_SM_CK_3
BK22 VCC_SM_CK_4

SM CK

(80mA) — 1.8V_TXLVDS — L25
10mil — 1000pF 50V 10% 0402 X7R — C257 — C256 120ohm 25% 200mA 0603(BLM11A121S) — 1.8V — 11,44
22uF 6.3V 20% 0805 X5R_NU — GM OPEN

VCC_TX_LVDS T41
VCC_HV_1 C33
VCC_HV_2 A33 — 3VS_HV

HV

(1782mA) — 1.05VS — 11,16,18,19,21,24,30
AB44 VCC_PEG_1
Y44 VCC_PEG_2
AC43 VCC_PEG_3
AA43 VCC_PEG_4 — 10uF 6.3V 10% 0805 X5R — C279 — C249 T100uF 6.3V 45m 20% 3528

PEG

(456mA) 20mil — GM OPEN

AM44 VCC_DMI_1
AN43 VCC_DMI_2
AL43 VCC_DMI_3

DMI

C272 — C255 0.1uF 10V 10% 0402 X7R — 10uF 6.3V 10% 0805 X5R

K14 VTTLF1
Y12 VTTLF2
F2 VTTLF3 — VTTLF_CAP1 VTTLF_CAP2 VTTLF_CAP3

VTTLF

C267 0.47uF 16V 10% 0603 X7R — C268 0.47uF 16V 10% 0603 X7R — C158 0.47uF 16V 10% 0603 X7R

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36,37,41,44,45

R175 10-5%-1/10W-0603 — D12 1SS355PT 90V 0.5A — 1.05VS — 11,16,18,19,21,24,30

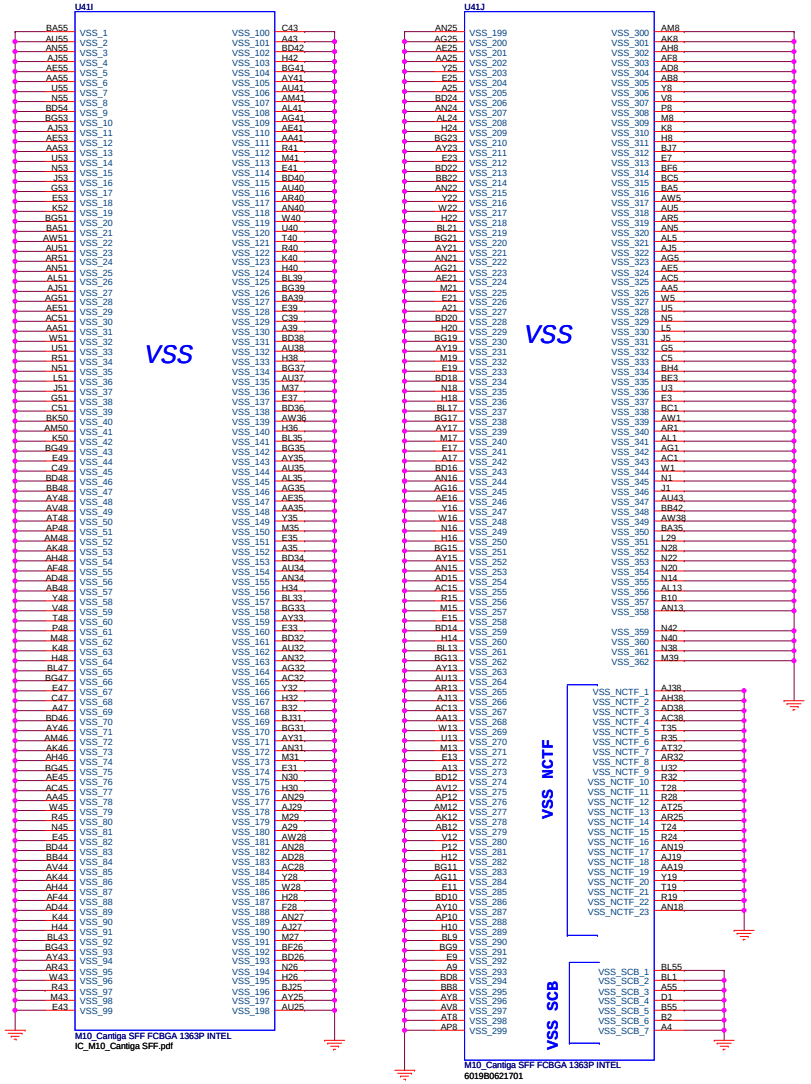
20mil (105.3mA) — R515 SHORT-0402-15MIL — 3VS_HV — C714 0.1uF 10V 10% 0402 X7R

INVENTEC

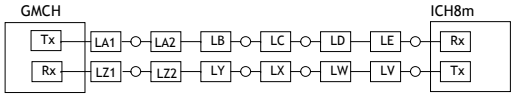
TITLE BAP41/BAP51 (Montevina SFF)
Cantiga Power(5/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by Shiun-Chin Chang DATE Thursday, July 02, 2009 SHEET 22 of 49



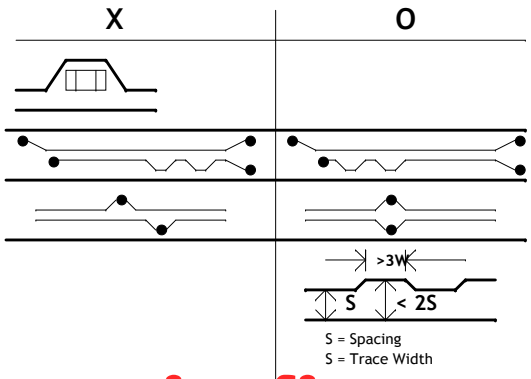
DMI Routing Guideline



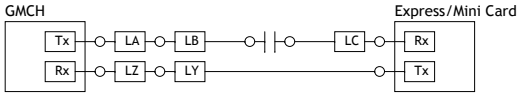
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Dideferential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



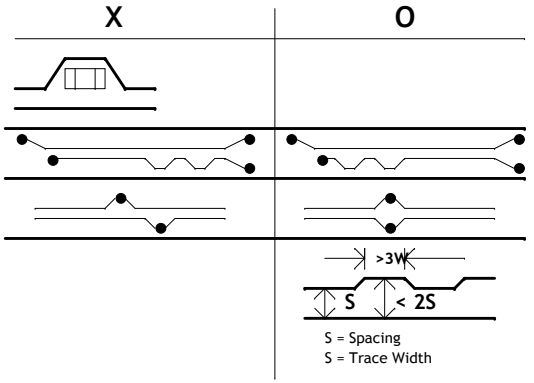
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



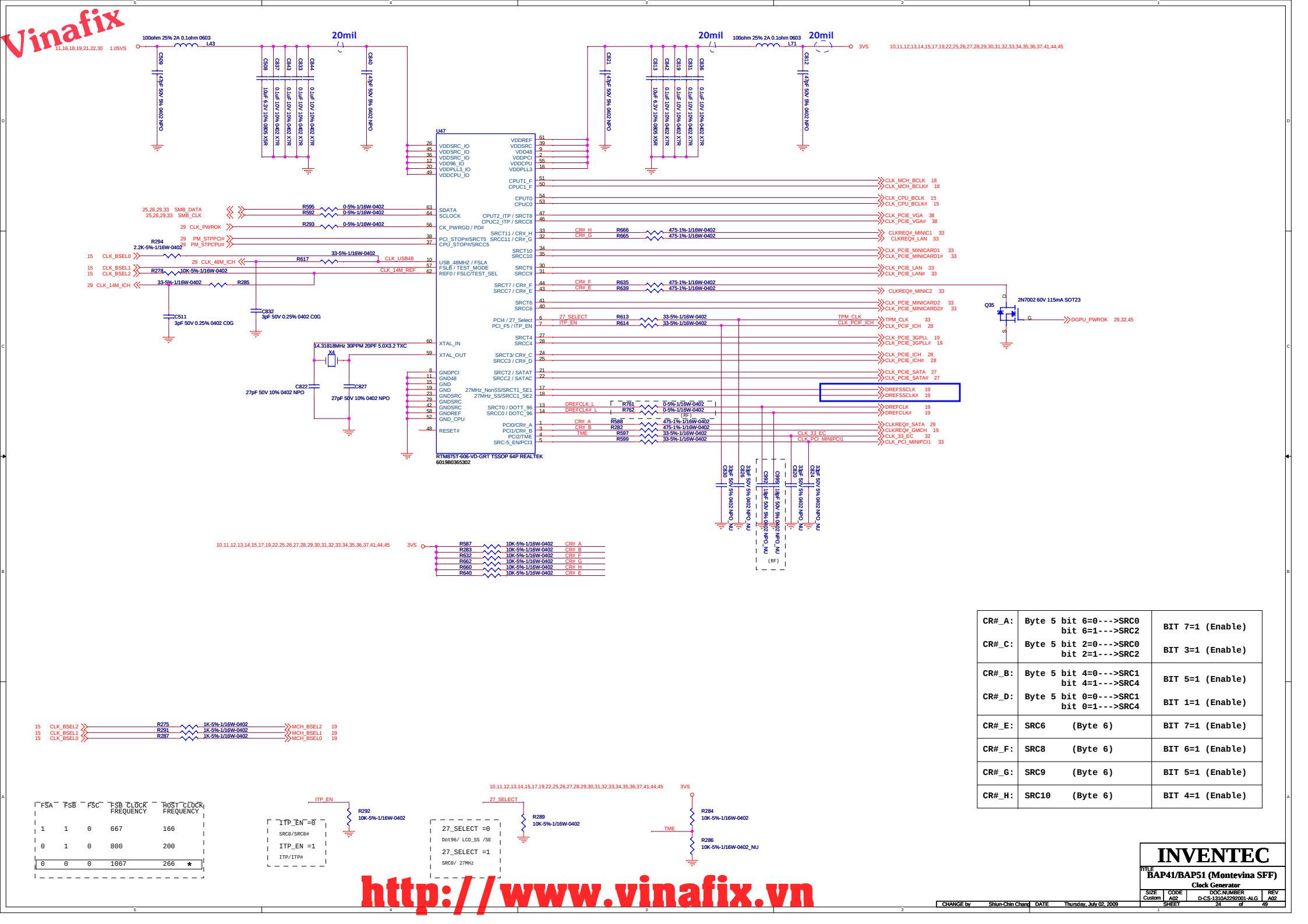
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Cantiga Ground(6/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

SHEET 23 of 49

CHANGE by Shiun-Chin Chang DATE Monday, June 29, 2009



CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY	
1	1	0	667	166	
0	1	0	800	200	
0	0	0	1067	266	*

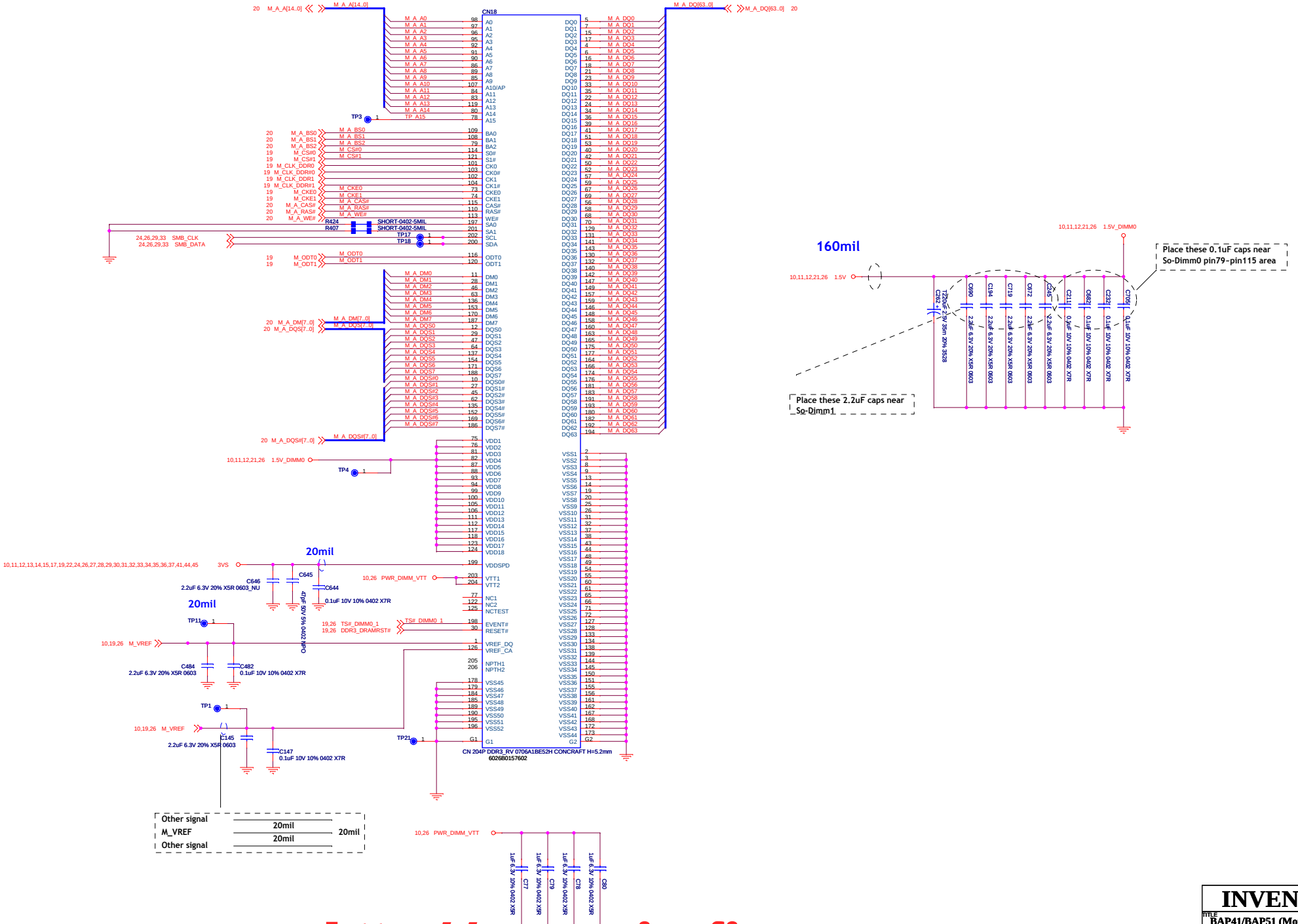
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

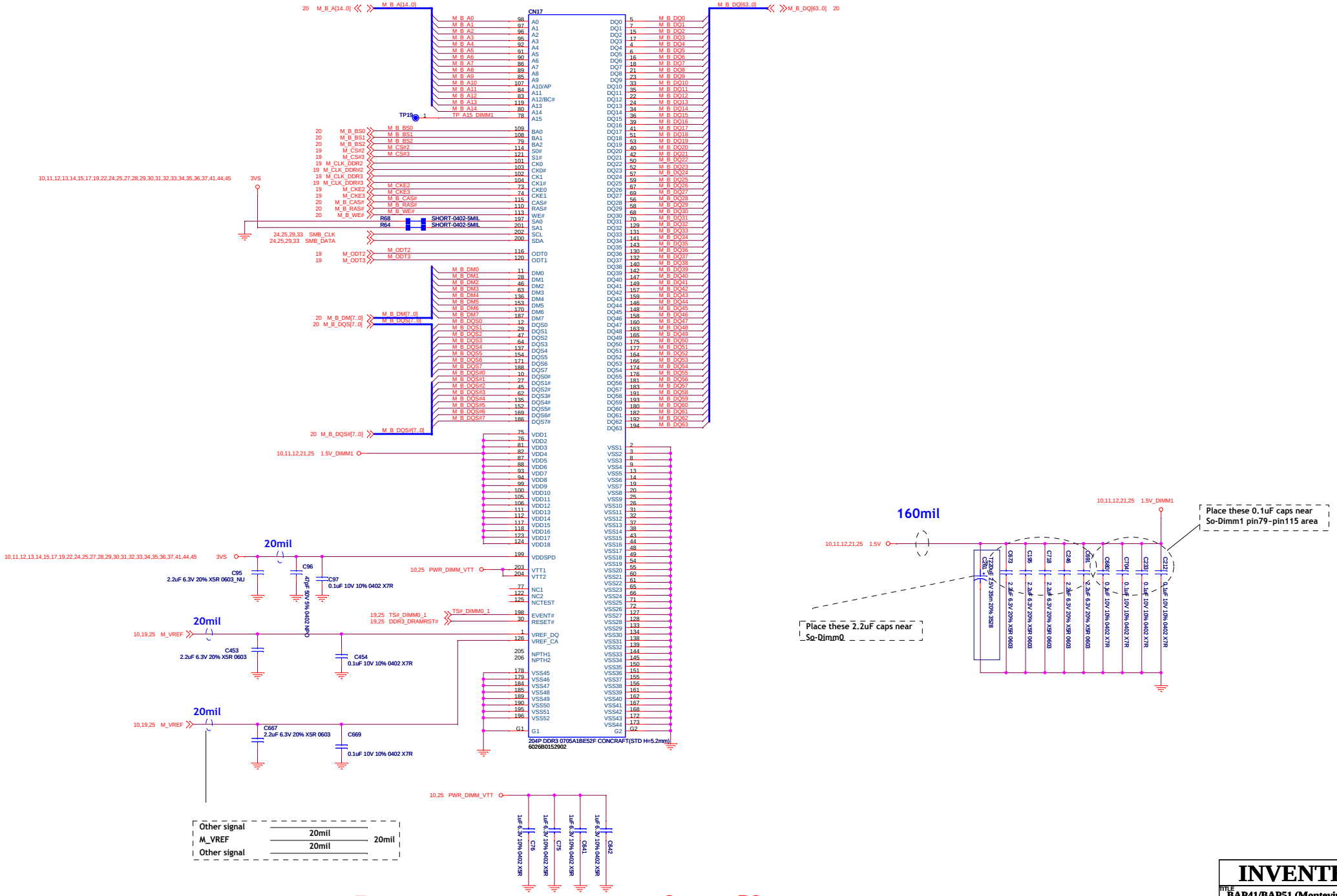
CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 24 of 49

SO-DIMM0



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF)			
DDR3 SDRAM SO-DIMM0			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 25 of 49	

SO-DIMM1

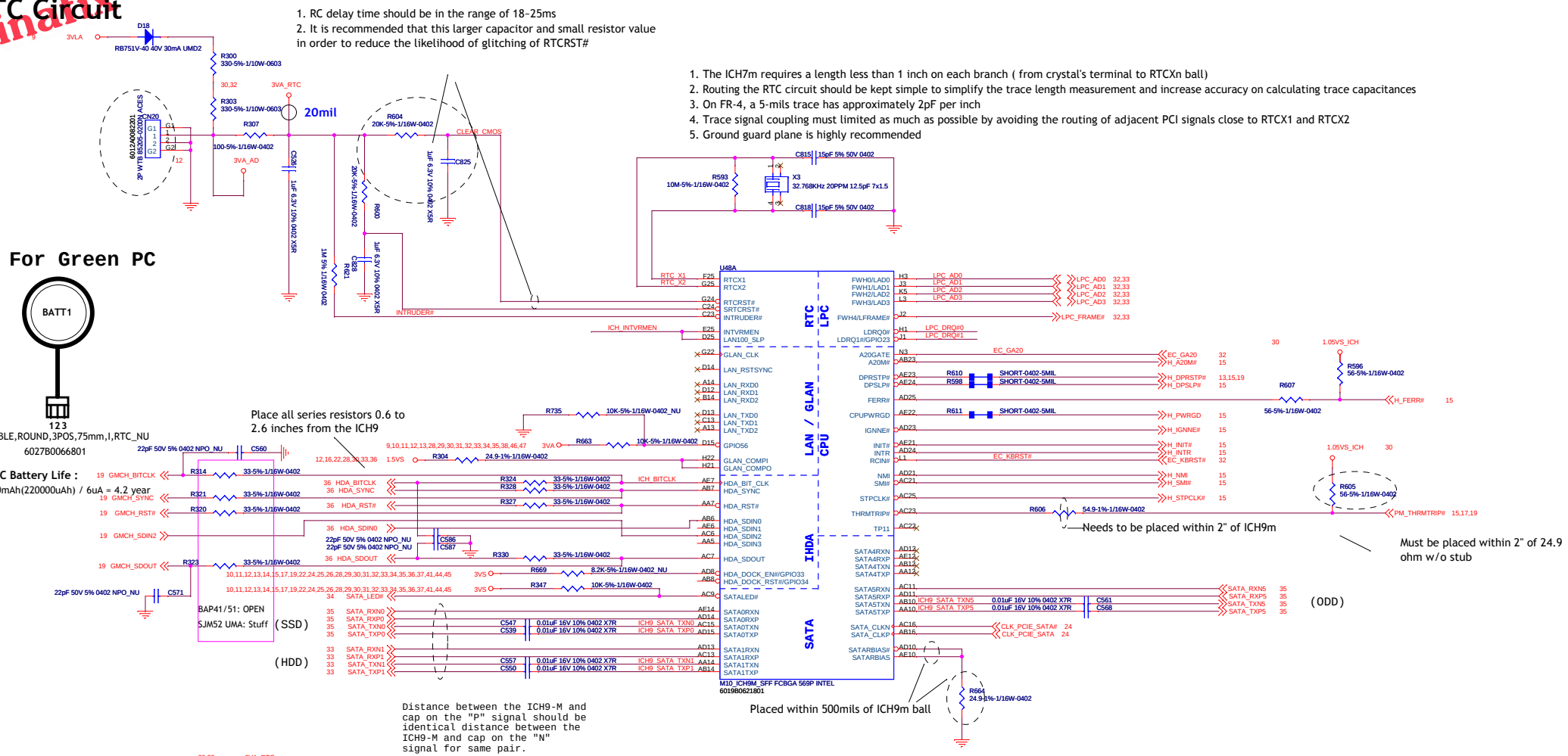


TITLE	BAP41/BAP51 (Montevina SFF)
	DDR3 SDRAM SO-DIMM1
SIZE	Custom
CODE	A02
DOC.NUMBER	D-CS-1310A2292001-ALG
REV	A02
CHANGE by	Shiun-Chin Chang
DATE	Thursday, July 02, 2009
SHEET	26 of 49

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

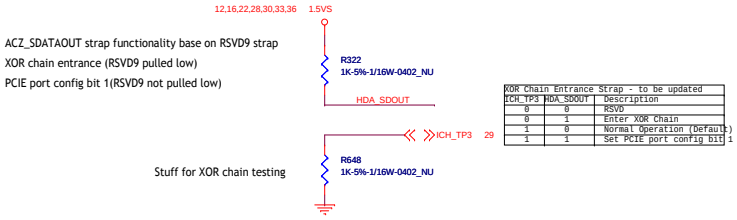


ICH8m internal VR enable strap

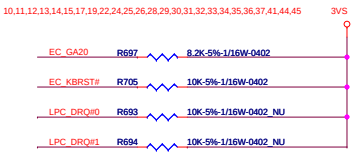
	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

Short pins AG1 and AG2 at the package



XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF)			
ICH9M CPU/SATA(1/4)			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 27 of 49	

PCIE AC coupling caps need to be within 250mils of the driver

WLAN
3G
LAN

U48D

PCI-Express Direct Media Interface

SPI

USB

M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

10mil

Place within 500mils of ICH

Place within 500mils of ICH
5/5 mils spacing on microstrip

U48B

PCI

Interrupt I/F

M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

PCI Pull up

Buffer to reduce loading on PLT_RST#

PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

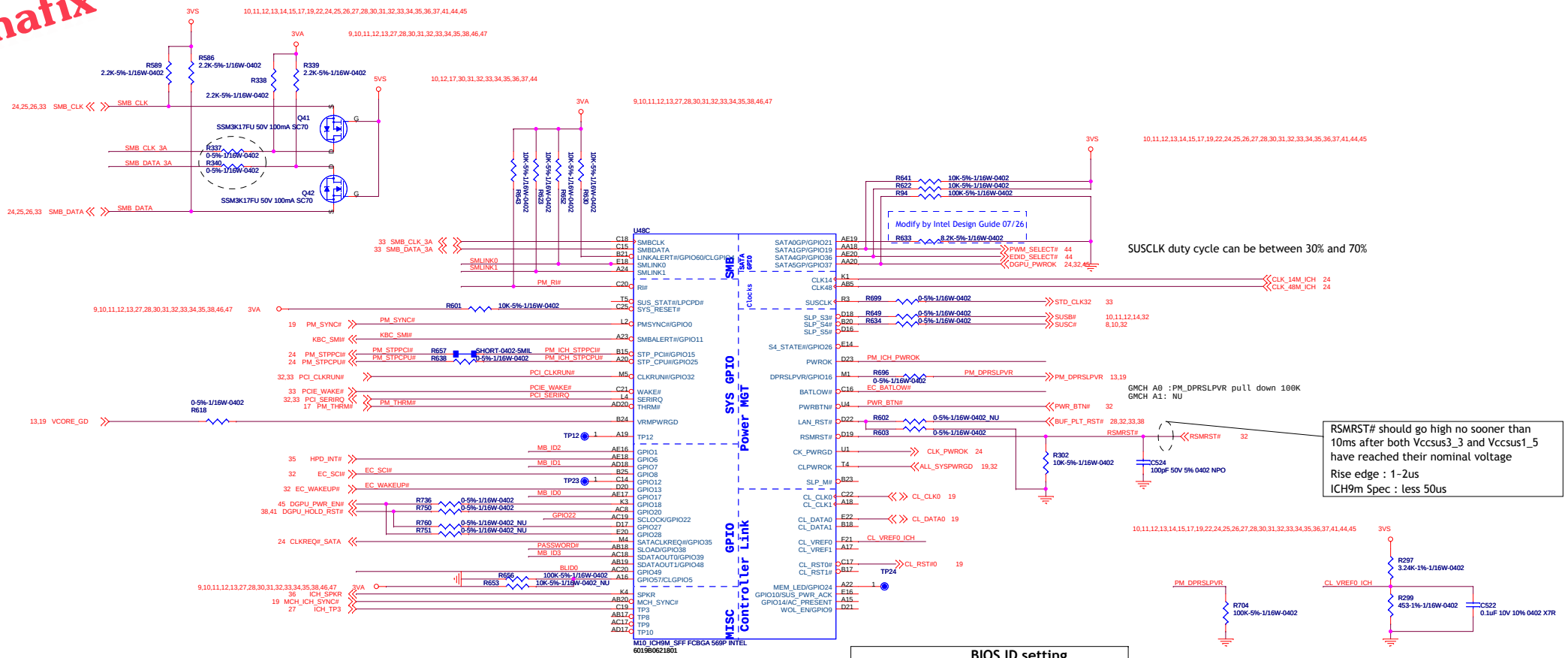
Check BIOS type

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
ICH9M PCI/PCIE/DMI/USB(2/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

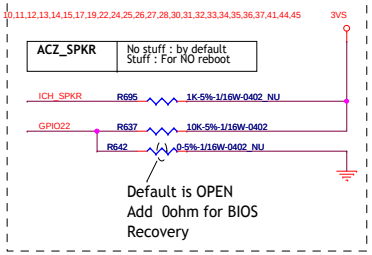
CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 28 of 49



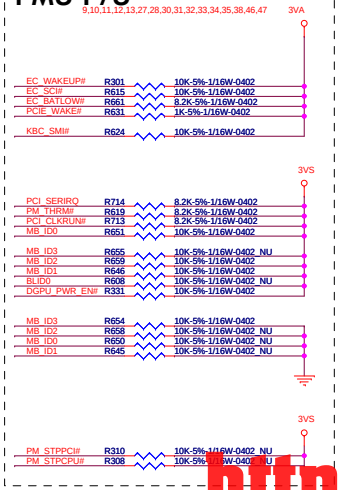
BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
BAP41 (UMA)	1	1	0	0
BAP51 (UMA)	1	0	1	1
JM31 (dGPU)	1	0	1	0
SJM31 (dGPU)	1	0	0	1
BAP31 (dGPU)	1	0	0	0
BAP41 (dGPU)	0	1	1	1
BAP51 (dGPU)	0	1	1	0
SJM52 (UMA)	0	1	0	1
SJM52 (dGPU)	0	1	0	0
BAP52 (UMA)	0	0	1	1
BAP52 (dGPU)	0	0	1	0
BXP41(UMA)	0	0	0	1
BXP41(dGPU)	0	0	0	0

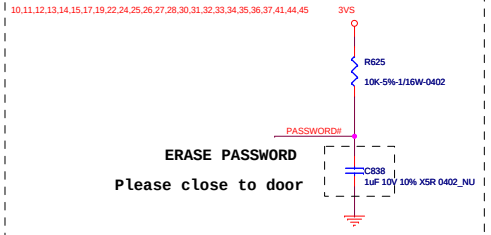
ICH9m strap

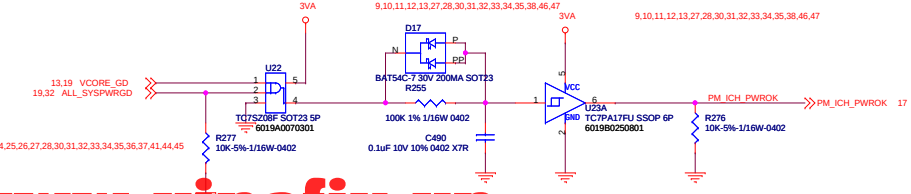


PMU P/U



PASSWORD CLEAR





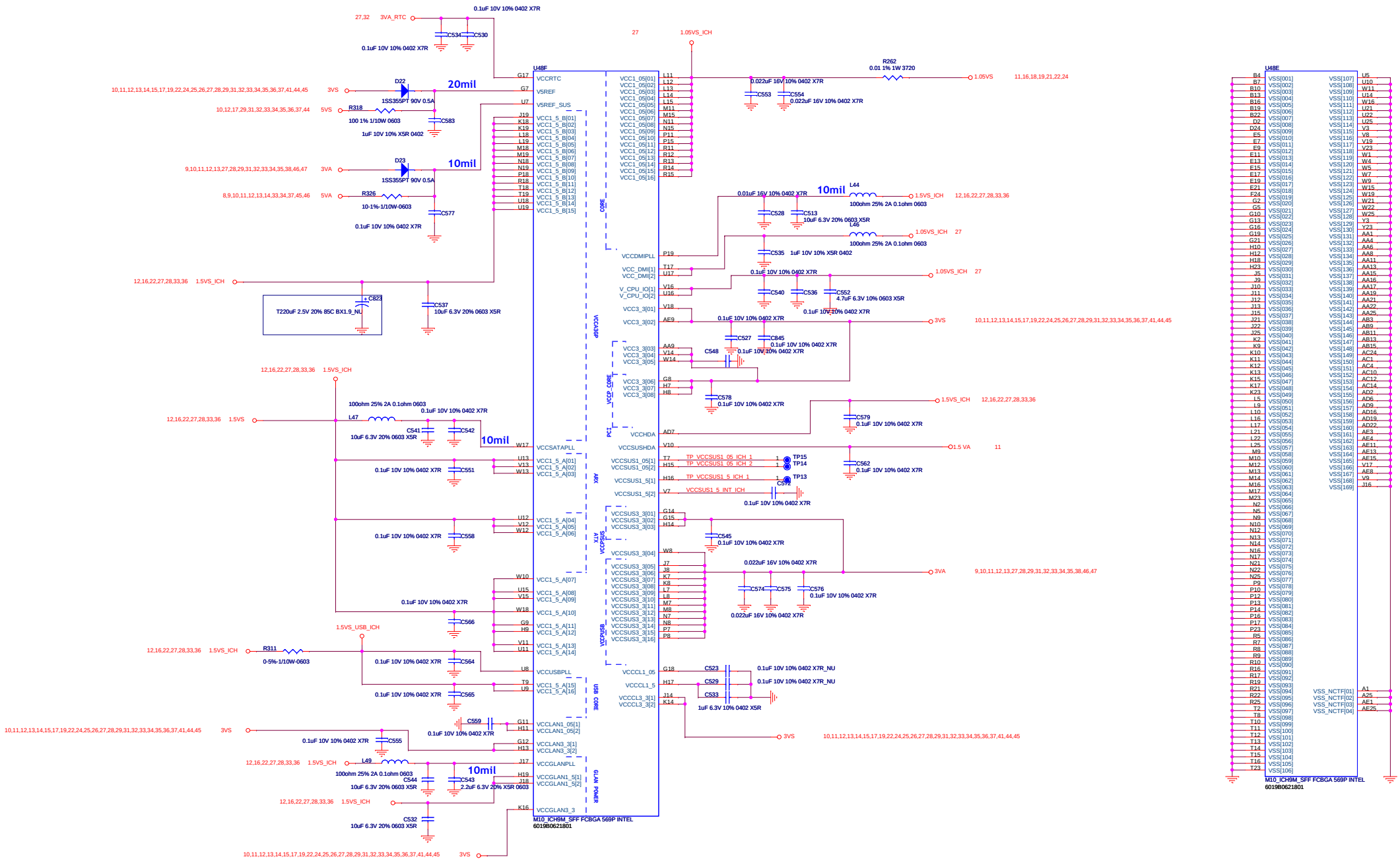
CHANGE by	Shiun-Chin Chang	DATE	Thursday, July 02, 2009	

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
ICH9M GPIO(3/4)

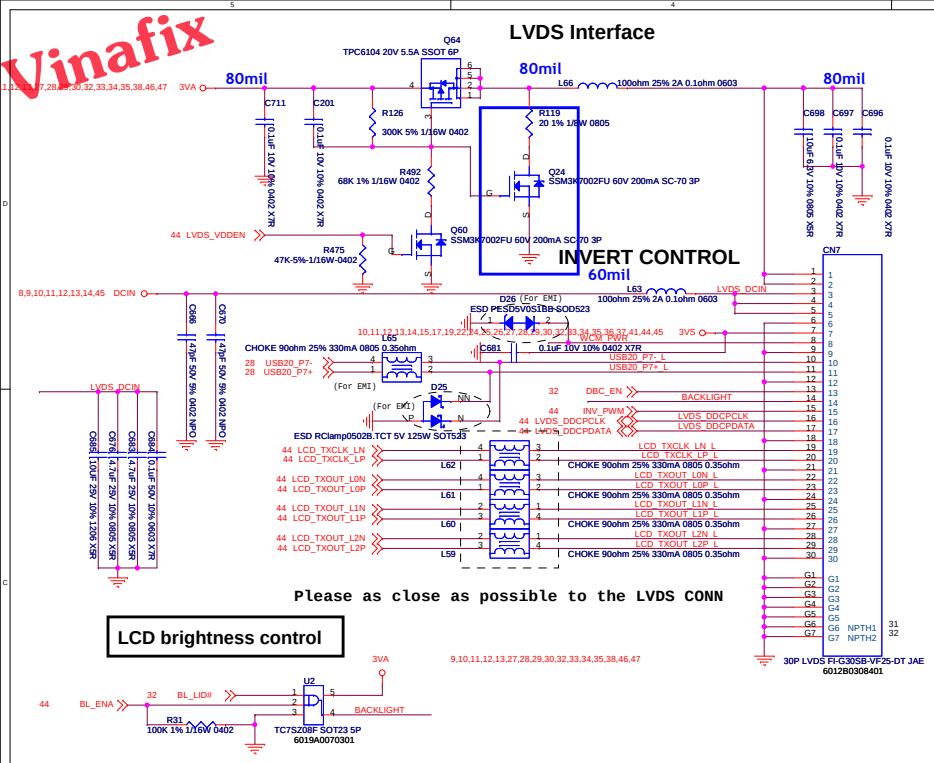
SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

SHEET 29 of 49

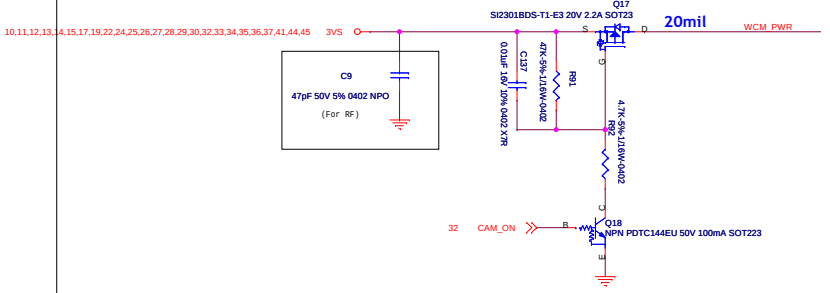


INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF)			
ICH9M Power/GND(4/4)			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 30 of 49	

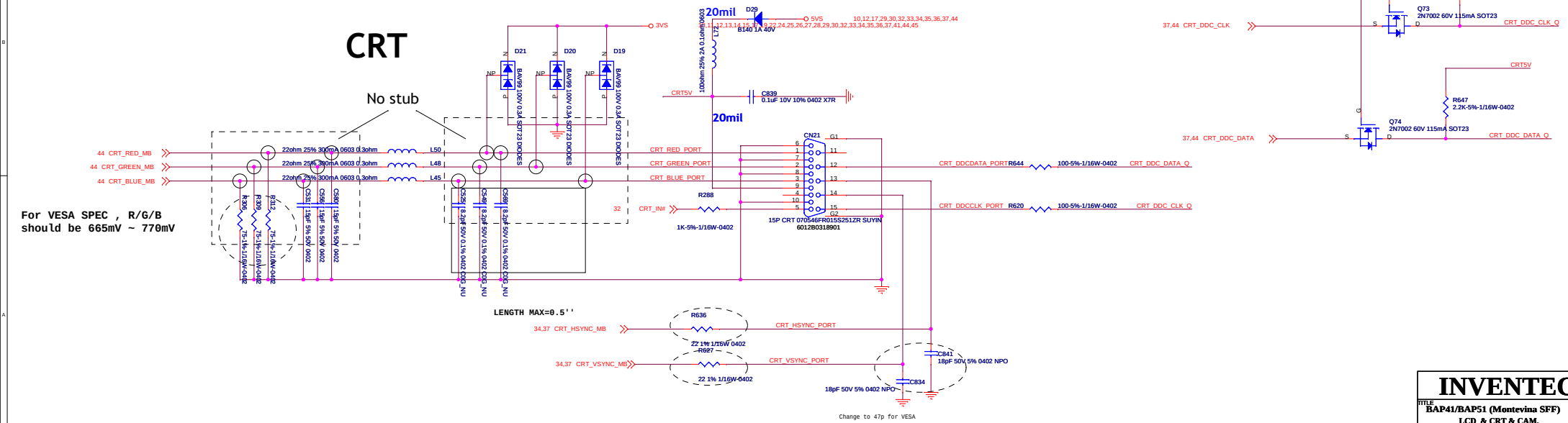
LVDS Interface



WEB Cam.



CRT



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) LCD & CRT & CAM.			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 31 of 49	

For Green PC

IT8502E-L

SPI FLASH

Don't place any pull-up resistor on GPG0 and GPG6

Pull down is for SPI flash

GPIO groud I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode

BAP41/51/52/BXP41 SW Gfx : Stuff R473,R477,R480,R476,R481,Q62,Q63,R767,R768,R769
OPEN R472,R474,R479

BAP41/51/52/BXP41 UMA : Stuff R473,R477,R480,R476,R481
OPEN R472,R474,R479,Q62,Q63,R767,R768,R769

SJM52 SW Gfx : Stuff R472,R477,R480,R474,R479,Q62,Q63,R767,R768,R769
OPEN R473,R476,R481

SJM52 UMA : Stuff R472,R477,R480,R474,R479
OPEN R473,R476,R481,Q62,Q63,R767,R768,R769

	R86	C128
For IT8502IX	0 Ohm	NU
For IT8502JX	NU	0.1uF

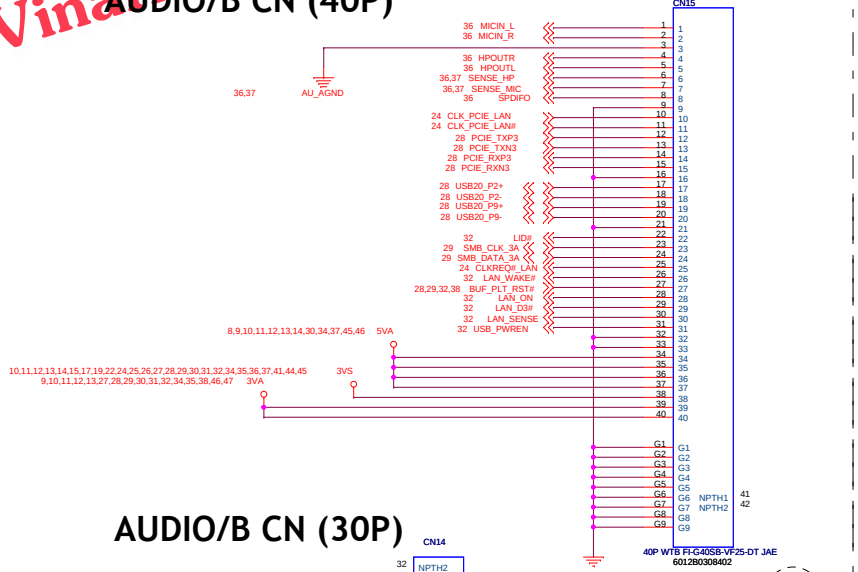
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
KBC ITE8502E-L

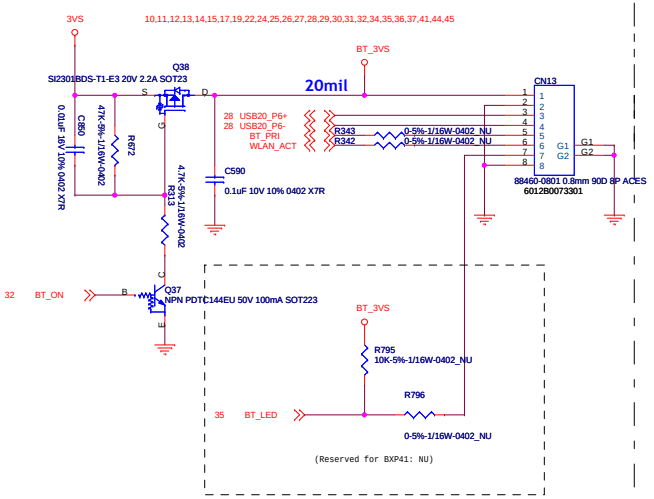
SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 32 of 49

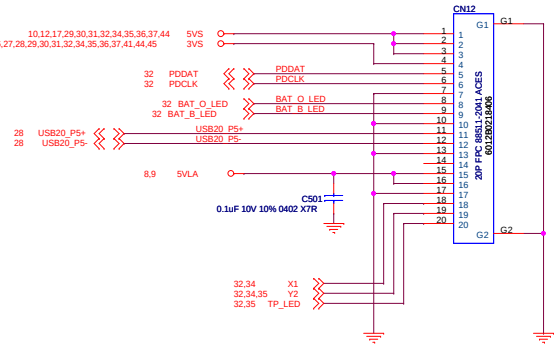
AUDIO/B CN (40P)



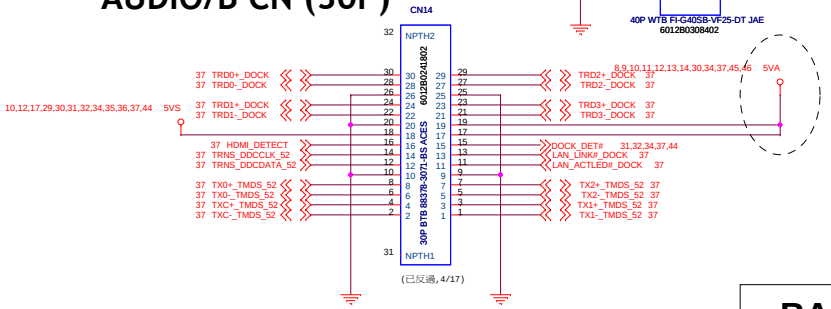
Bluetooth CN



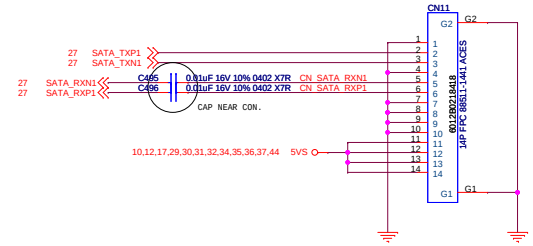
GLIDE PAD Board



AUDIO/B CN (30P)

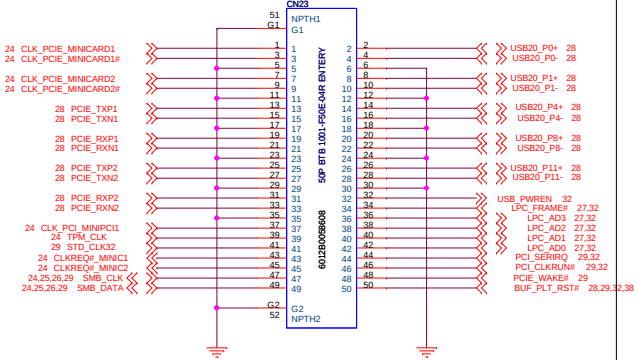


HDD BOARD CN



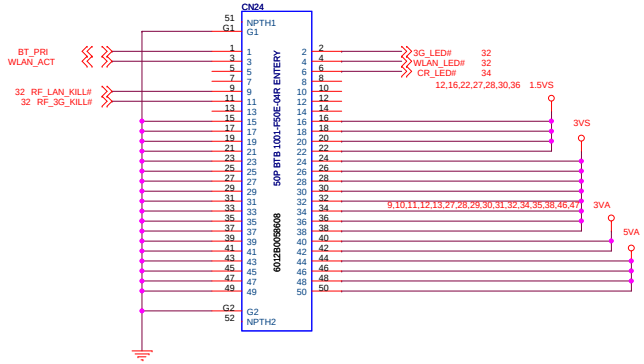
BAP41/BXP41:
Transfer/B CN:6012B0058608

BAP51/52/SJM52:
Mini-Card/B CN:6012B0058609



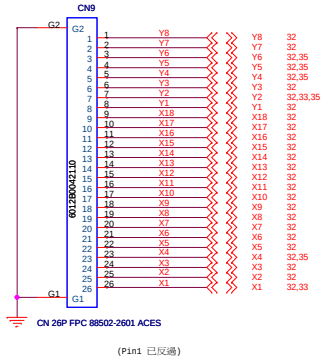
BAP41/BXP41:
Transfer/B CN:6012B0058608

BAP51/52/SJM52:
Mini-Card/B CN:6012B0058609

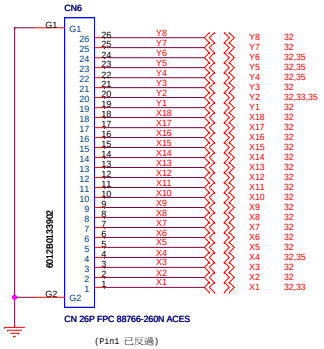


INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) Daughter Connector			
SIZE: Custom	CODE: A02	DOC NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 33 of 49	

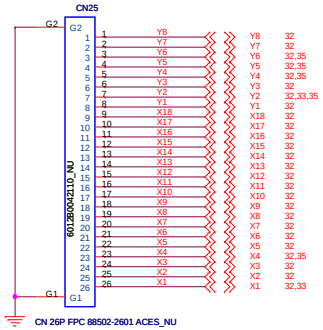
To K/B(For BAP41)



To K/B (For BAP51/BAP52/SJM52)

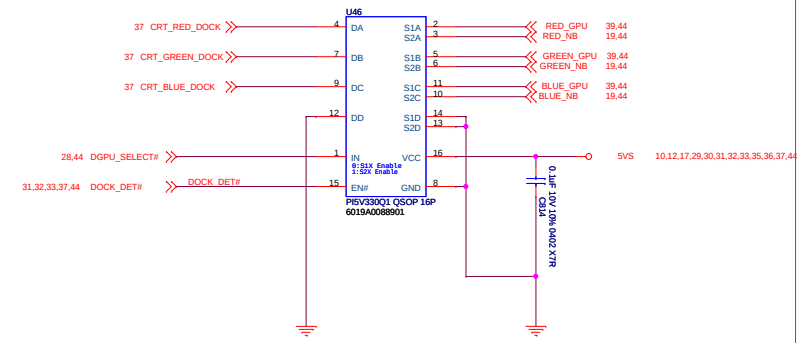


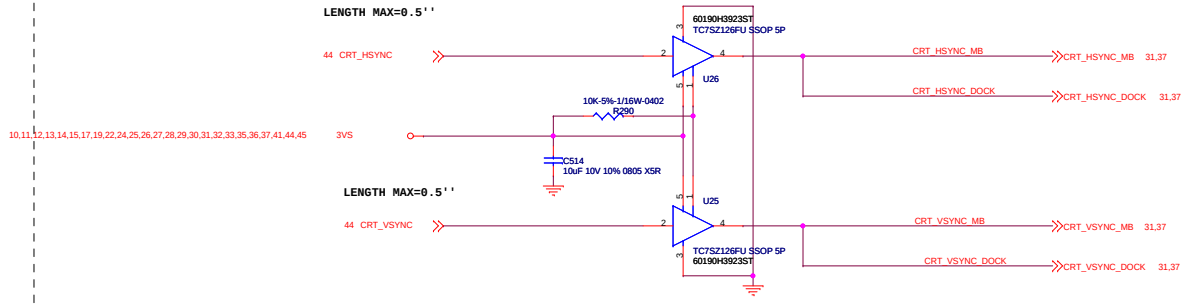
To K/B(For BXP41)

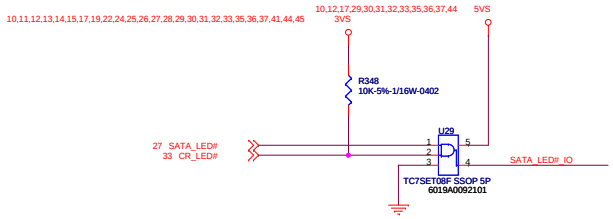


BAP41/51/52/BXP41: Stuff U46,C814

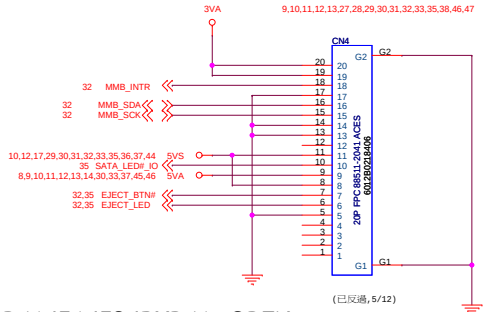
SJM52 : OPEN U46,C814







SW Sensor BOARD(For SJM52)

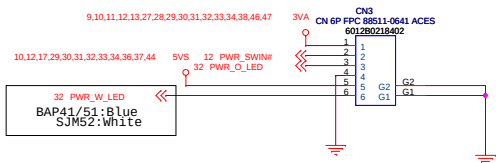


BAP41/51/52/BXP41: OPEN
SJM52: Stuff

INVENTEC

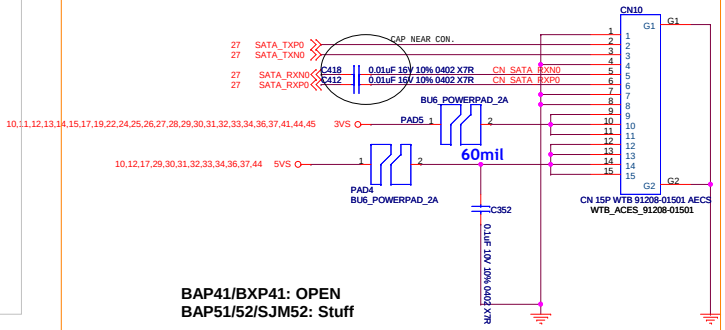
TITLE	BAP41/BAP51 (Montevina SFF) BDP		
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02
CHANGE by	Shiun-Chin Chang	DATE Thursday, July 02, 2009	SHEET 34 of 49

MB(PWR_SWIN#) TO DC-JACK/B



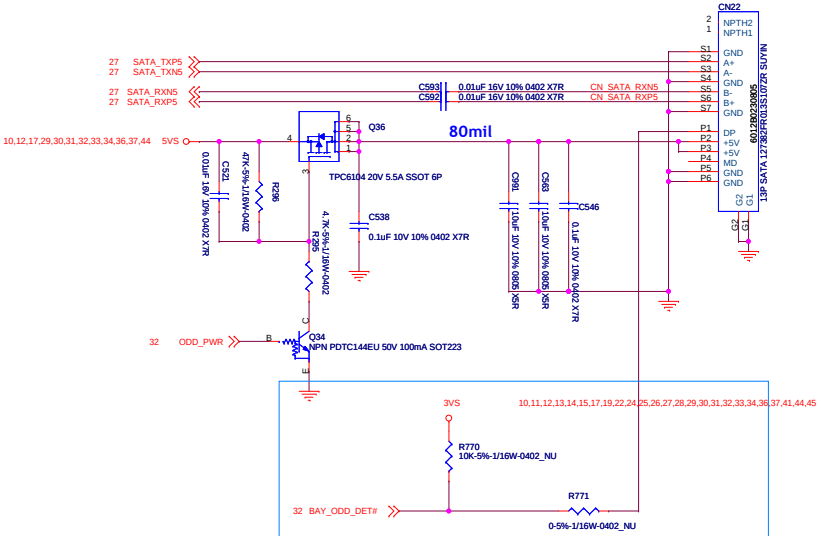
BXP41: OPEN

SSD I/F



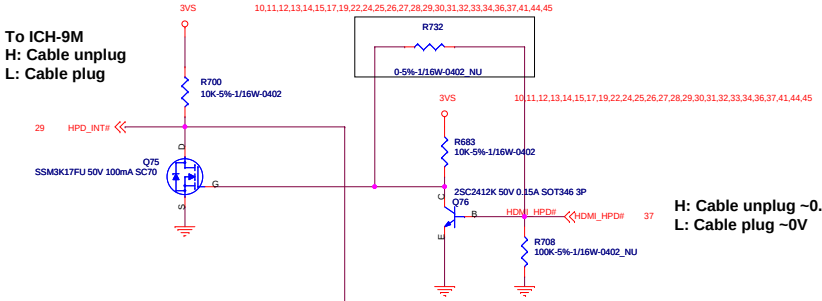
BAP41/BXP41: OPEN
BAP51/52/SJM52: Stuff

ODD I/F



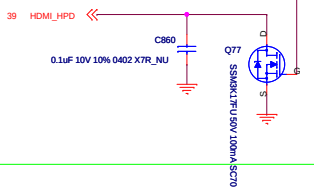
For BAP52 : Stuff

To ICH-9M
H: Cable unplug
L: Cable plug



H: Cable unplug ~0.9V
L: Cable plug ~0V

To M92-S2
H: Cable plug
L: Cable unplug



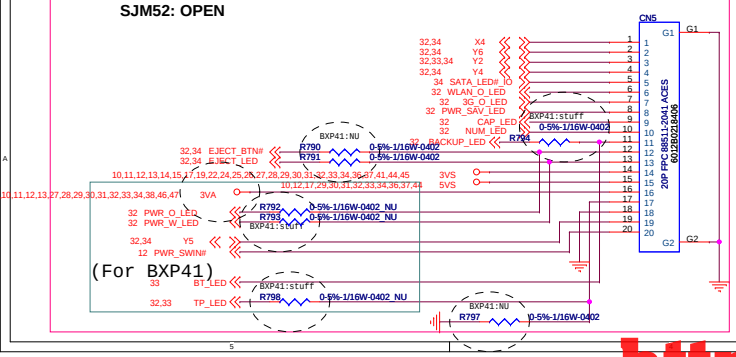
SW Gfx : Stuff
UMA : OPEN

SW Gfx : OPEN
UMA : Stuff

Size:0201

SW/B CN

BAP41/51/52/BXP41: Stuff
SJM52: OPEN

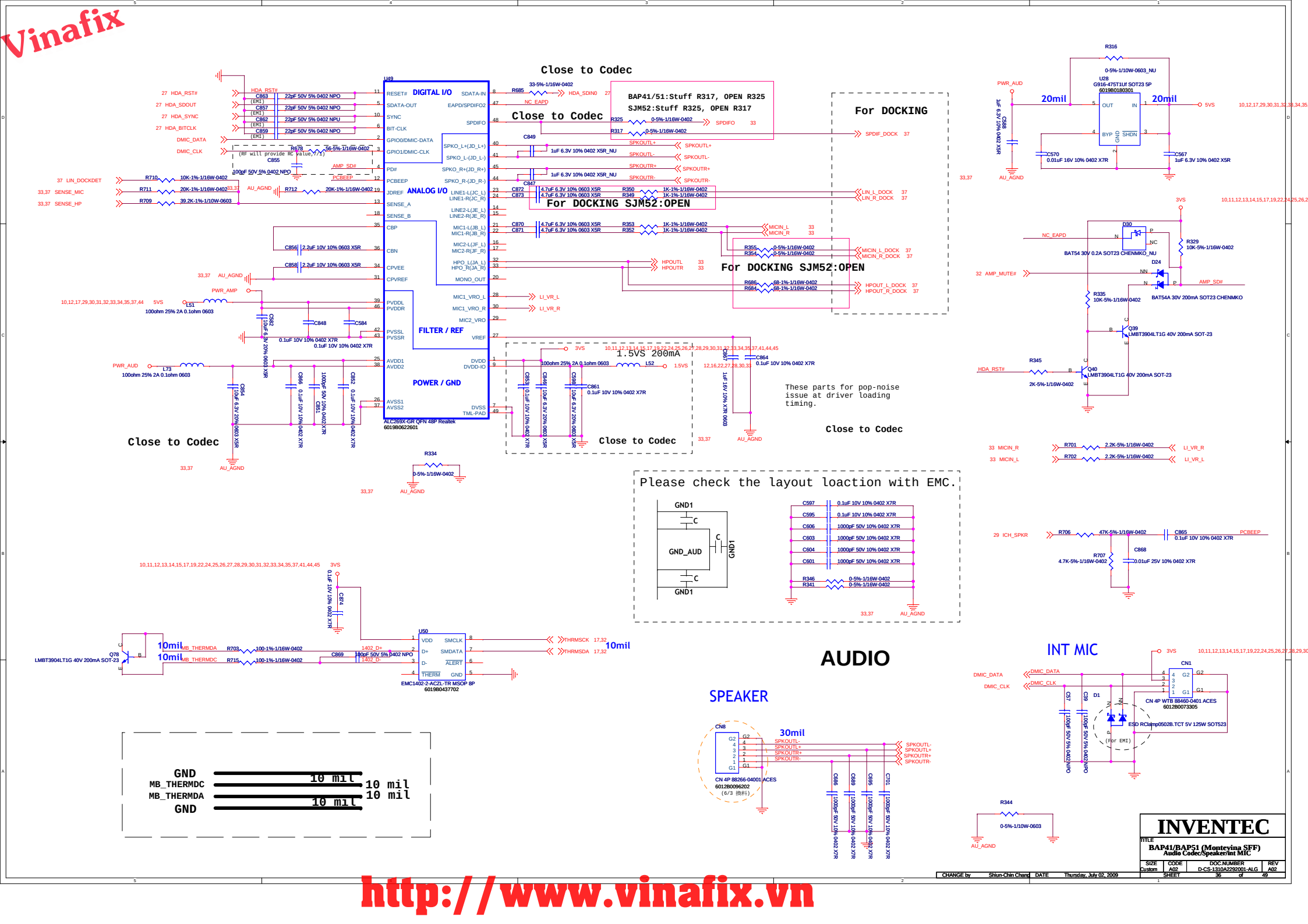


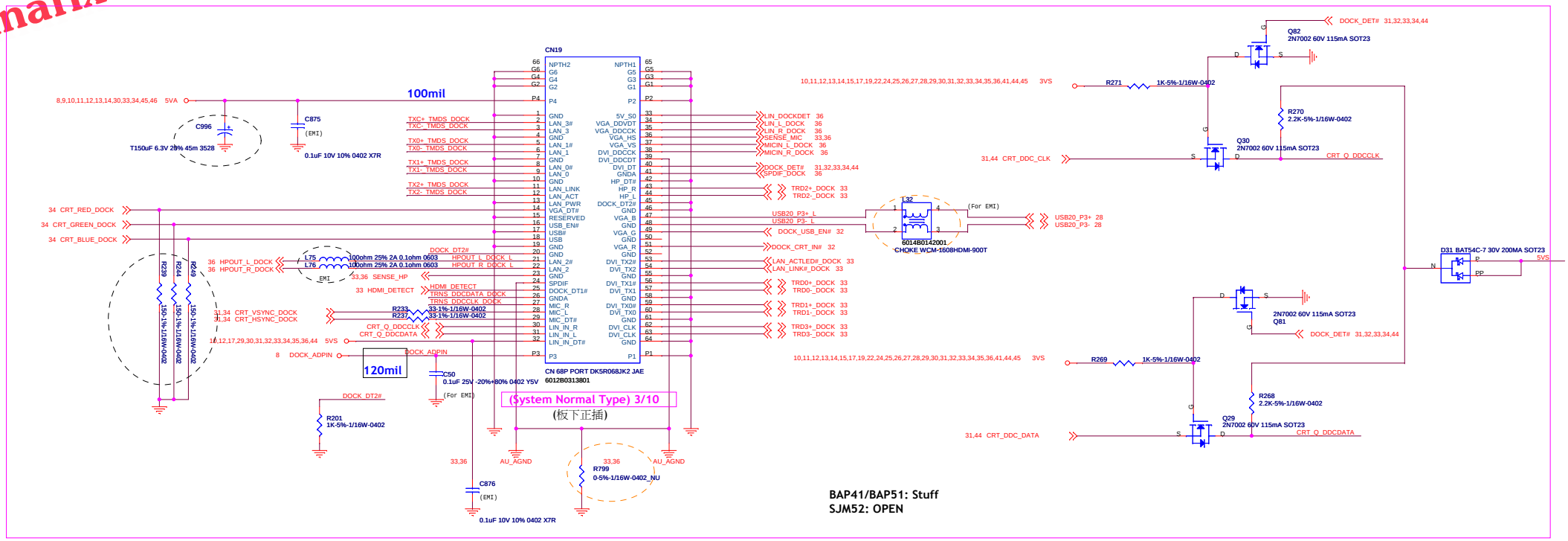
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF) BDP

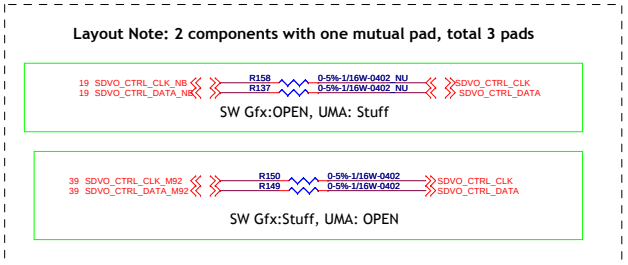
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

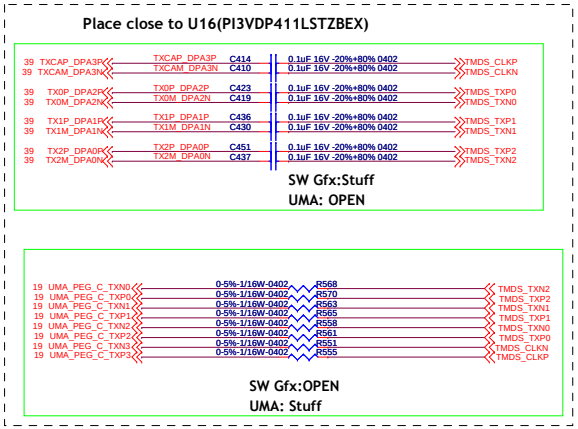
CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 35 of 49

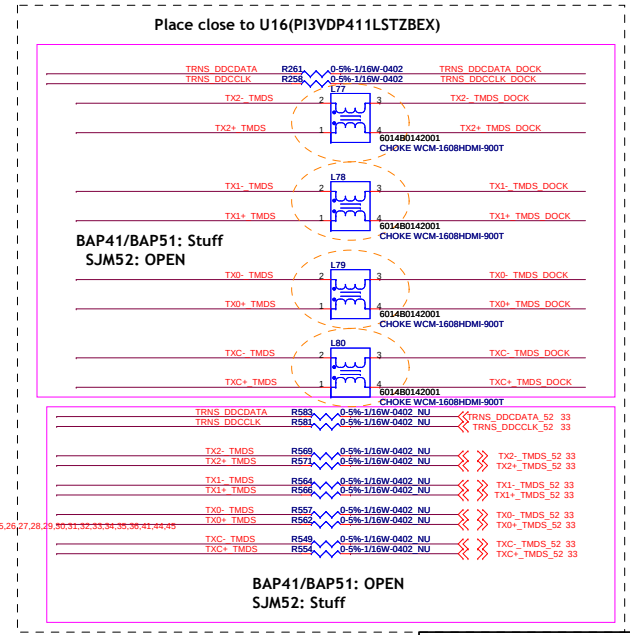


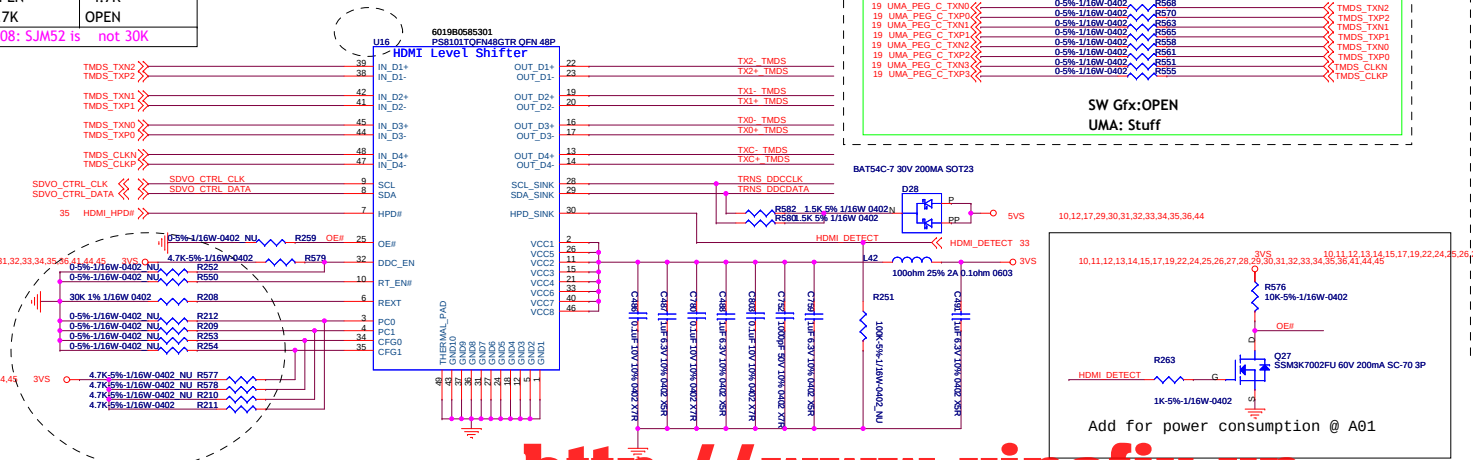


Parade	Pericom
U16 : 6019B0585301	6019B0443802
R550 : OPEN	0 ohm
R208 : 30K	OPEN
R212 : OPEN	0 ohm
R209 : OPEN	0 ohm
R253 : OPEN	0 ohm
R577 : OPEN	4.7K
R211 : 4.7K	OPEN
Note: R208: SJM52 is not 30K	







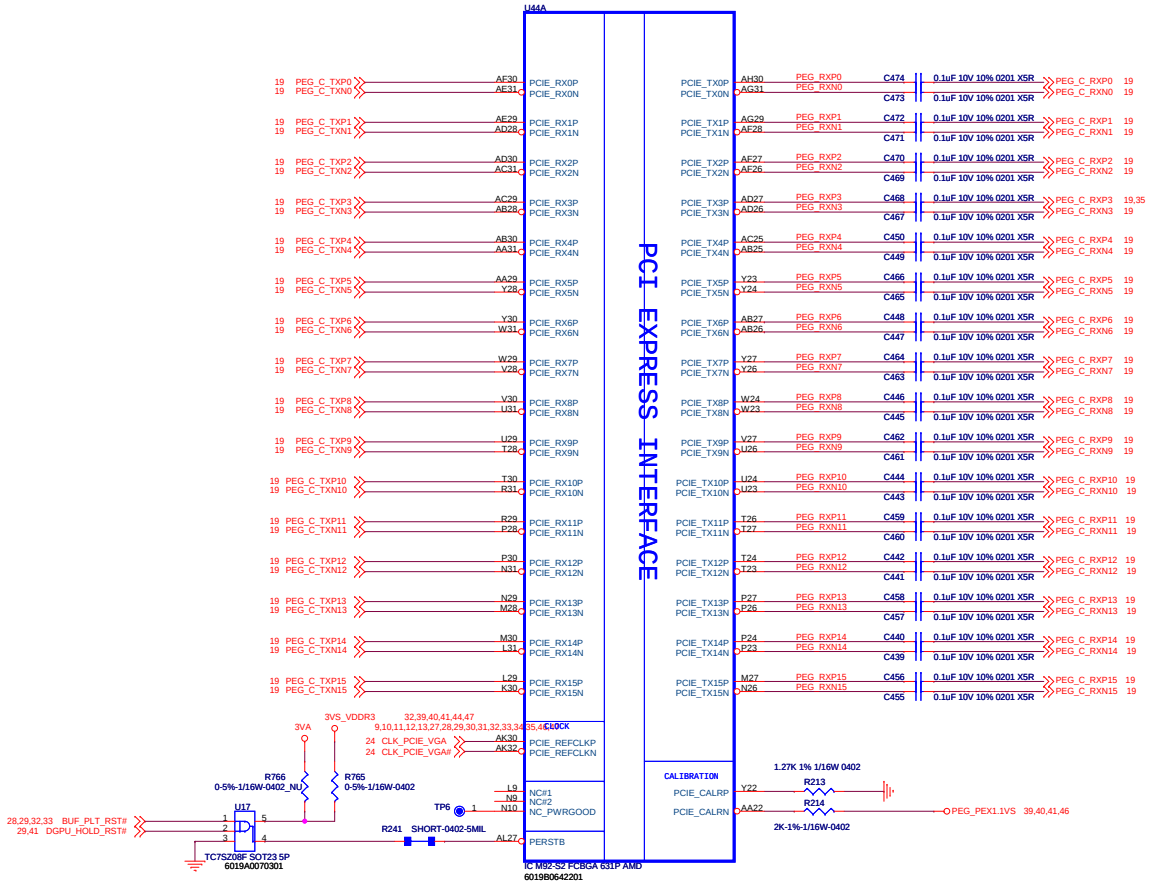


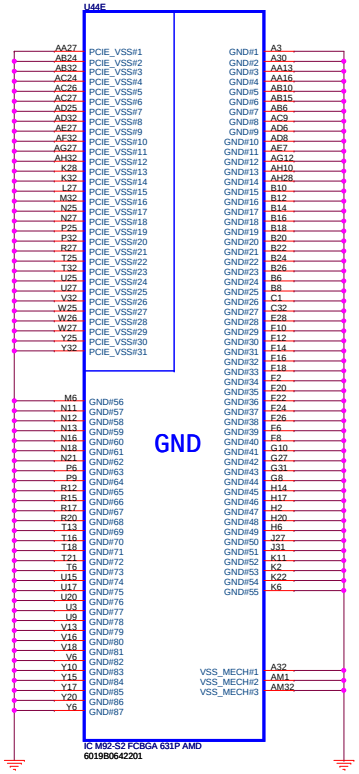
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF) EASY PORT CN/Level Shifter

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 37 of 49





Page 38:
SW Gfx: Stuff
UMA: OPEN

INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) M92			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 38 of 49	

GPIO_13	GPIO_12	GPIO_11	For DDR3
0	0	0	128M
0	0	1	256M(Default)
1	1	0	Reserved

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16

PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

H: Cable plug
L: Cable unplug

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

(1.8V@120mA DPLL_PVDD)

(1.1V@300mA DPLL_VDDC)

(1.8V@20mA TSVDD)

(1.8V@70mA AVDD)

(1.8V@45mA VDD1DI)

(1.8V@2mA AVDDQ)

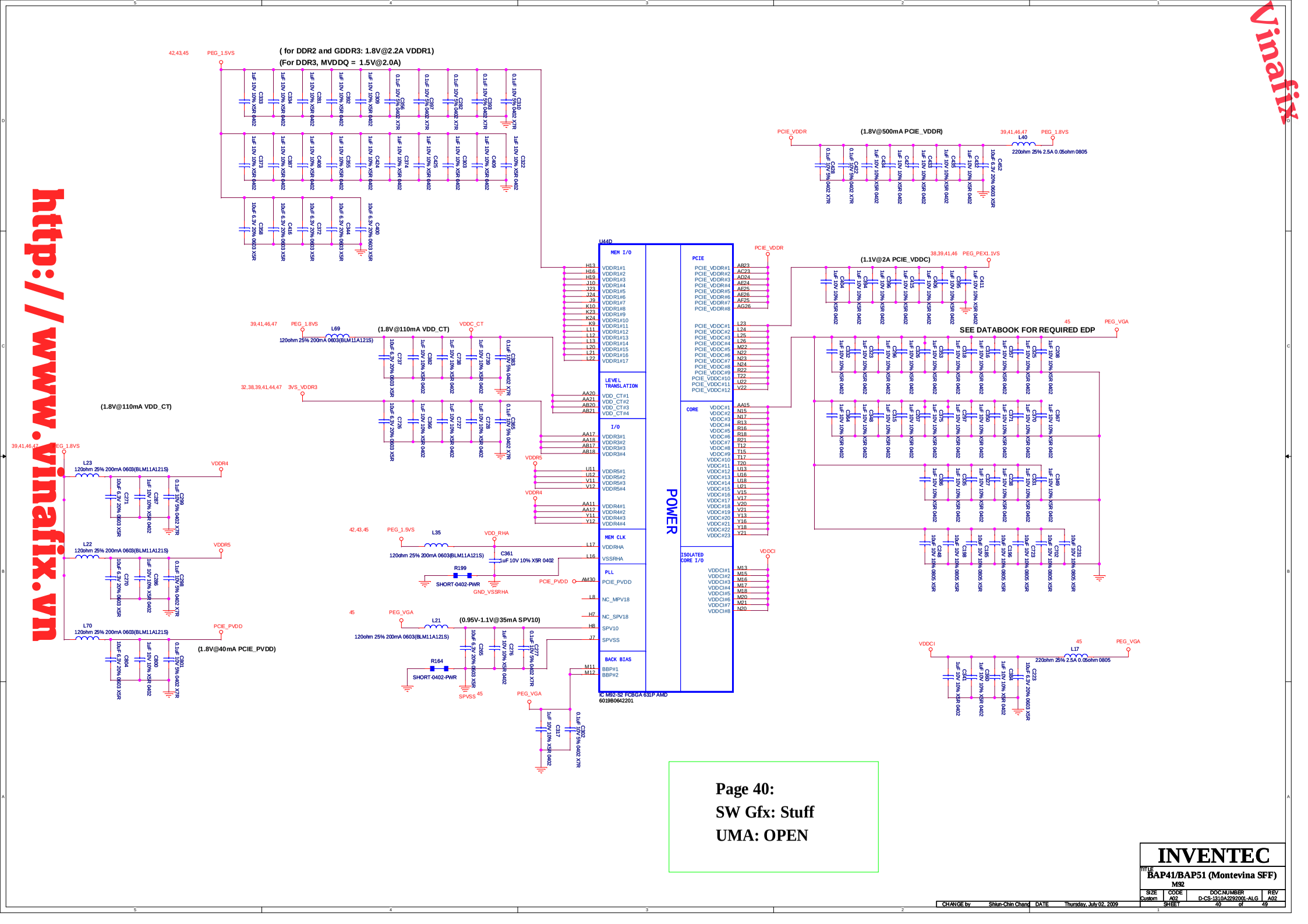
(1.8V@40mA VDD2DI)

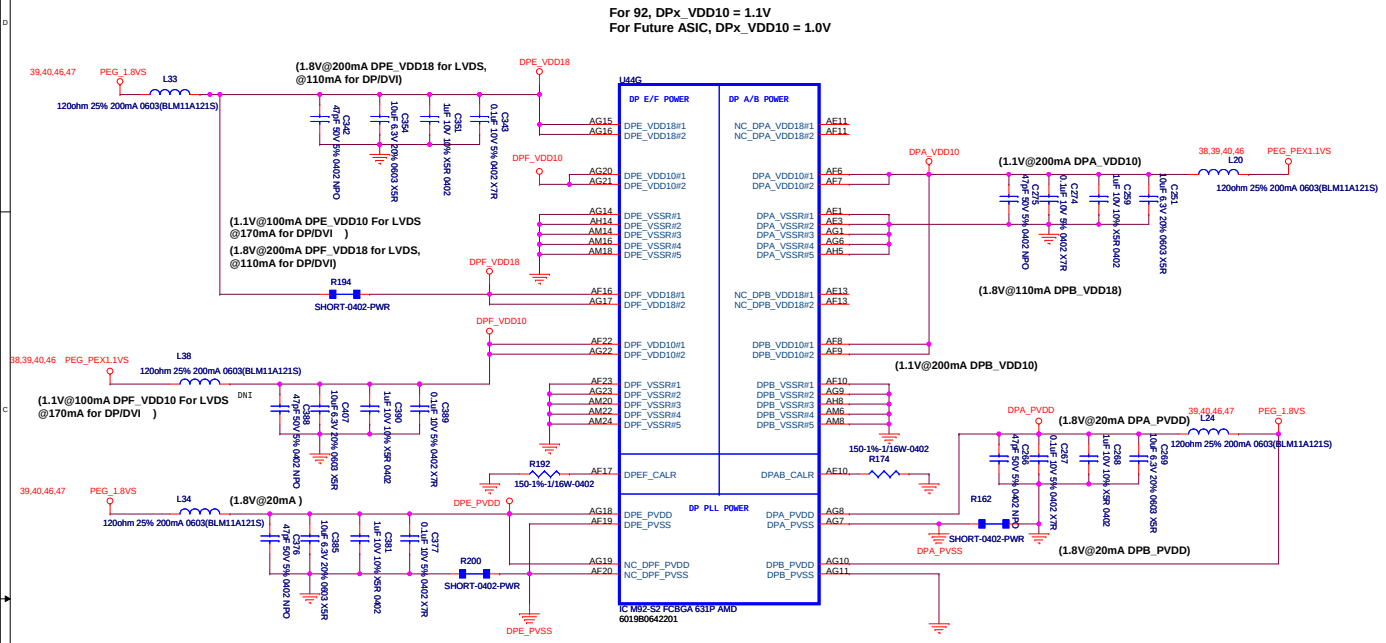
(3.3V@65mA A2VDD)

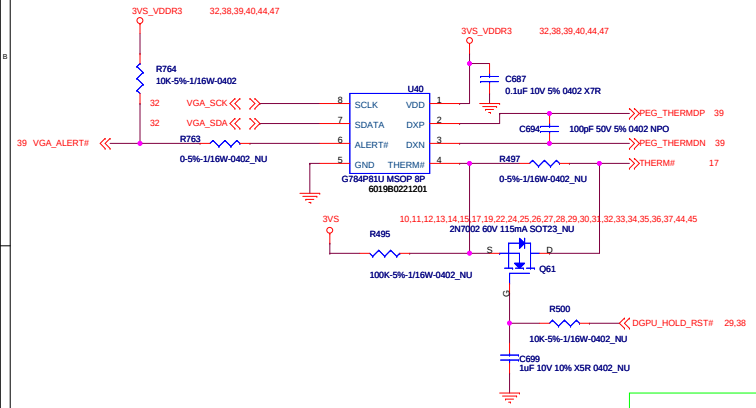
SW Gfx:Stuff, UMA: OPEN

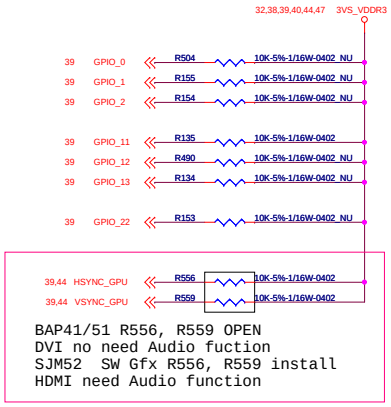
Page 39:
SW Gfx: Stuff
UMA: OPEN

INVENTEC
TITLE: BAP41/BAP51 (Montevina SFF)
M92
SIZE: Custom | CODE: A02 | DOC.NUMBER: D-CS-1310A2292001-ALG | REV: A02
CHANGE by: Shiun-Chin Chang | DATE: Thursday, July 02, 2009 | SHEET: 39 of 49


(for DDR2 and GDDR3: 1.8V@2.2A VDDR1)
(For DDR3, MVDDQ = 1.5V@2.0A)
PEG_1.5VS
(1.8V@500mA PCIE_VDDR)
PCIE_VDDR
L40
220ohm 25% 2.5A 0.05ohm 0805
PEG_1.8VS
(1.8V@110mA VDD_CT)
VDDC_CT
L69
120ohm 25% 200mA 0603(BLM11A121S)
3VS_VDDR3
(1.1V@2A PCIE_VDDC)
PEG_PEX1_1VS
SEE DATABOOK FOR REQUIRED EDP
PEG_VGA
U44D
MEM I/O
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
POWER
PCIE
CORE
ISOLATED CORE I/O
IC M92-S2 FCBGA 631P AMD
6019B0642201
VDDR4
VDDR5
L23
L22
L70
(1.8V@40mA PCIE_PVDD)
PCIE_PVDD
L35
VDD_RHA
C361
1uF 10V 10% X5R 0402
R199
SHORT-0402-PWR
GND_VSSRHA
L21
(0.95V-1.1V@35mA SPV10)
R164
SPVSS
VDDCI
L17
220ohm 25% 2.5A 0.05ohm 0805
Page 40:
SW Gfx: Stuff
UMA: OPEN
INVENTEC
BAP41/BAP51 (Montevina SFF)
M92
Custom
A02
D-CS-1310A2292001-ALG
A02
CHANGE by
Shiun-Chin Chang
DATE
Thursday, July 02, 2009
SHEET
40
of
49
Vinafix
http://www.vinafix.vn







PIN STRAPS

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function	X X
		0 1 Audio for DisplayPort and HDMI if dongle is detected	
		1 0 Audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Page 41:
SW Gfx: Stuff
UMA: OPEN

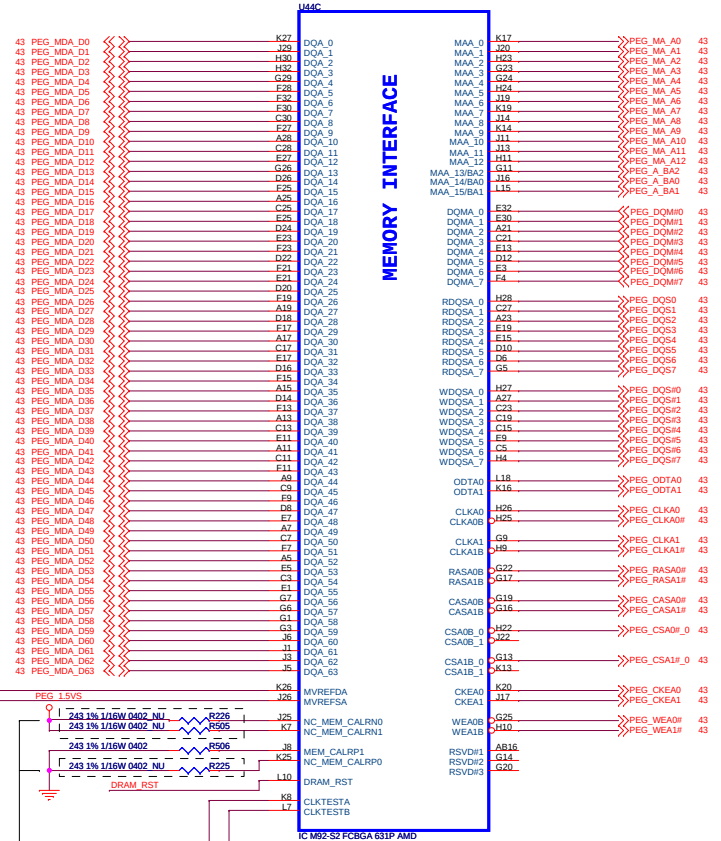
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
M92

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang | DATE: Thursday, July 02, 2009 | SHEET 41 of 49

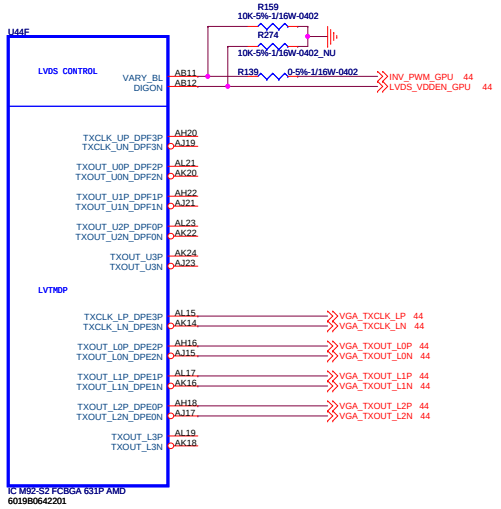
DDR3 Memory Interface



DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

MVDDQ = 1.5V FOR DDR3 Memory

LVDS Interface



Page 42:
SW Gfx: Stuff
UMA: OPEN

CHANGE by	Shiun-Chin Chang	DATE	Thursday, July 02, 2009

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF) M92

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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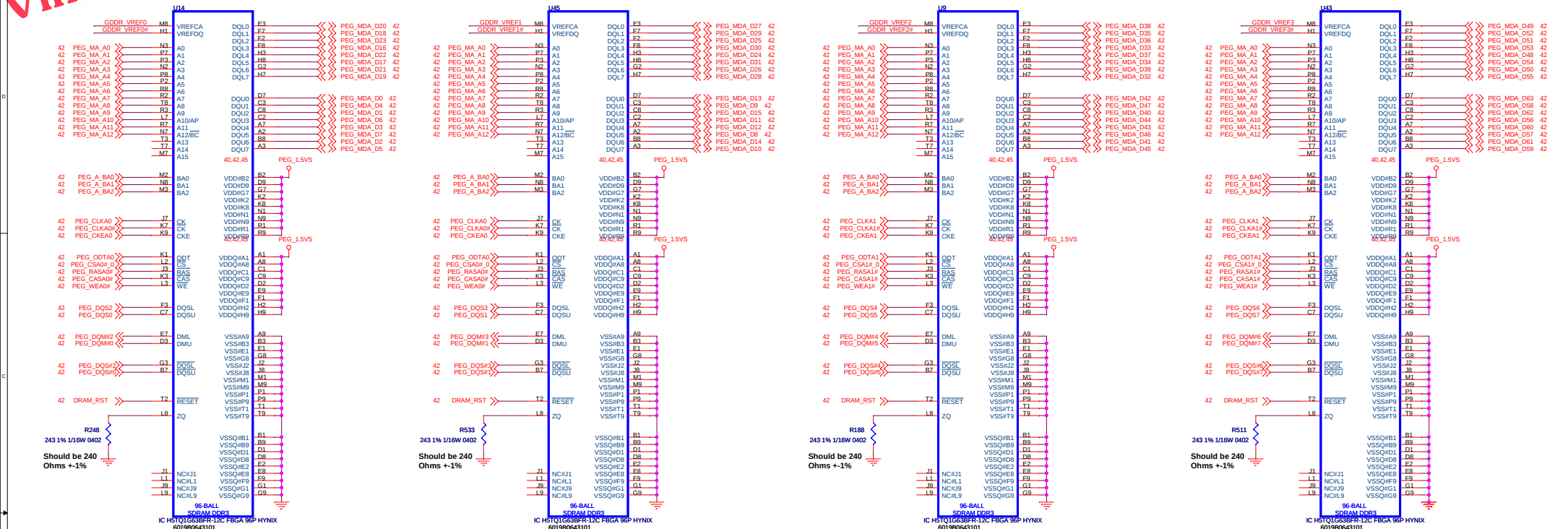
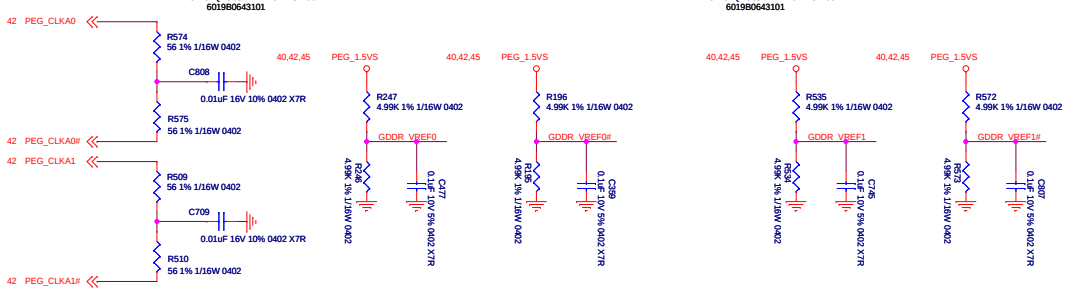
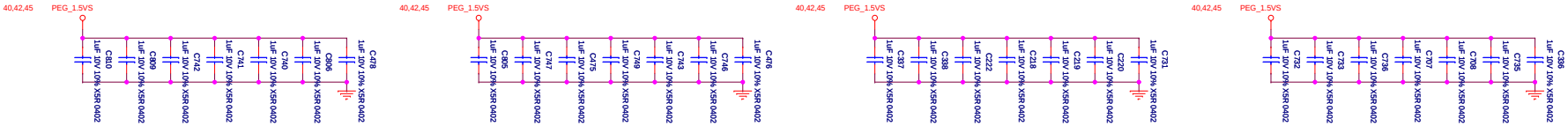
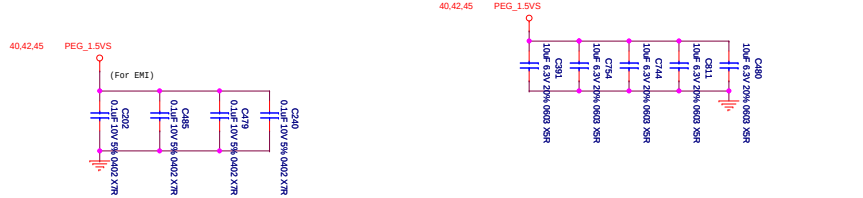








Page 43:
SW Gfx: Stuff
UMA: OPEN

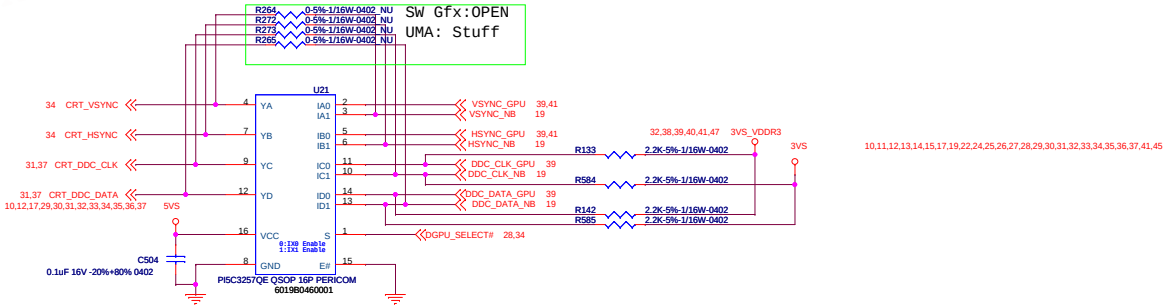
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
VRAM

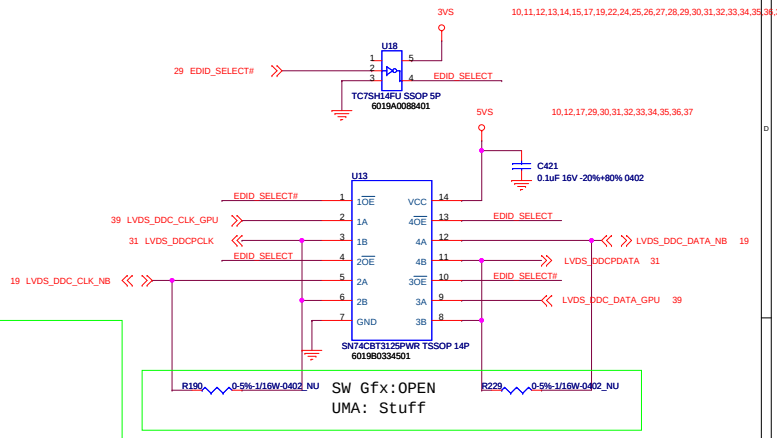
SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang | DATE: Thursday, July 02, 2009 | SHEET 43 of 49

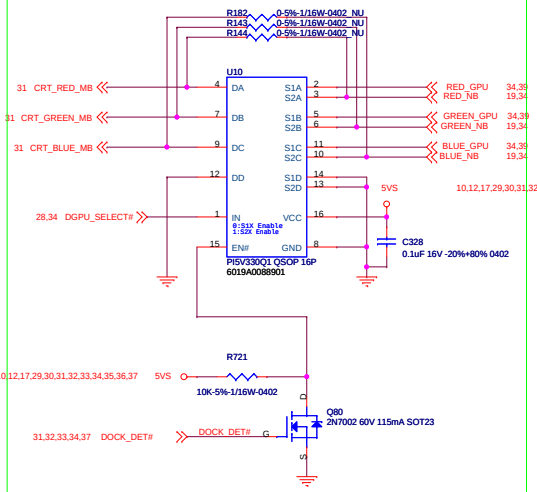
CRT HSYNC/VSYNC/DDC SW



LCD DDC SW



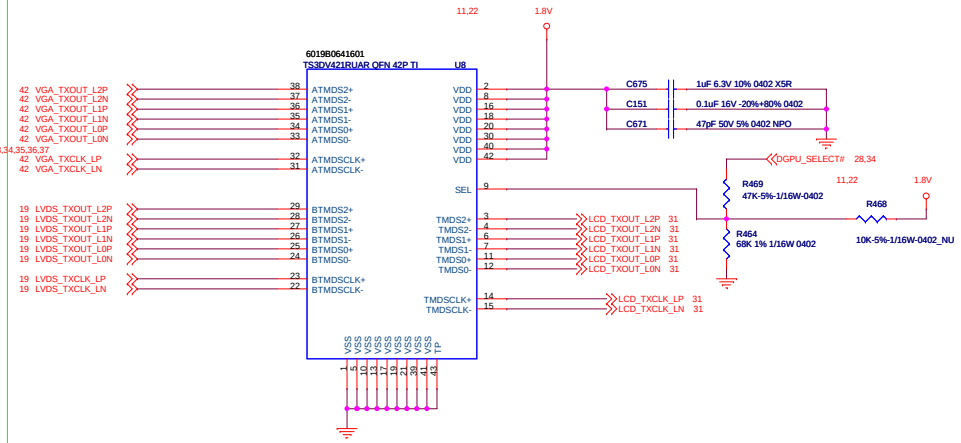
CRT R/G/B SW



Stuff CRT/RGB SW for both SW Gfx and UMA

SW Gfx : Stuff U10,C328,R721,Q80
UMA : Stuff U10,C328,R721,Q80

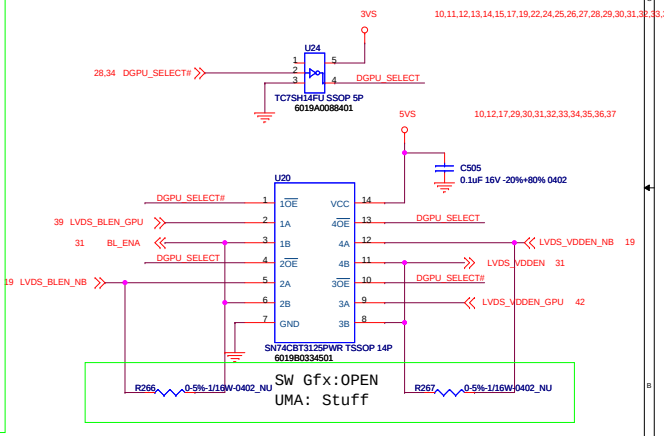
LVDS SW



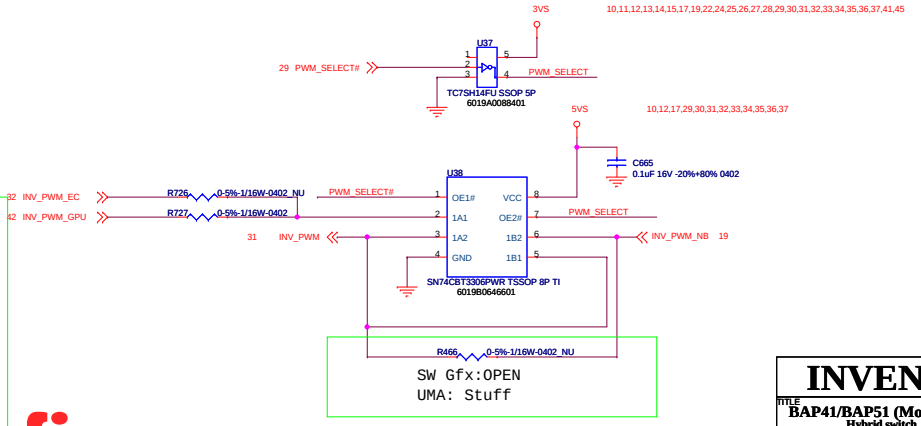
Thermal Pad limitation : Stuff LVDS SW for both SW Gfx and UMA

SW Gfx : Stuff U8,C675,C151,C671,R469,R464, OPEN R468
UMA : Stuff U8,C675,C151,C671,R468, OPEN R469,R464

LVDS BKL and Vcc Enable SW



LCD PWM SW



Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
EDID_SELECT#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

Page 44:
SW Gfx: Stuff
UMA: OPEN

INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
Hybrid switch

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

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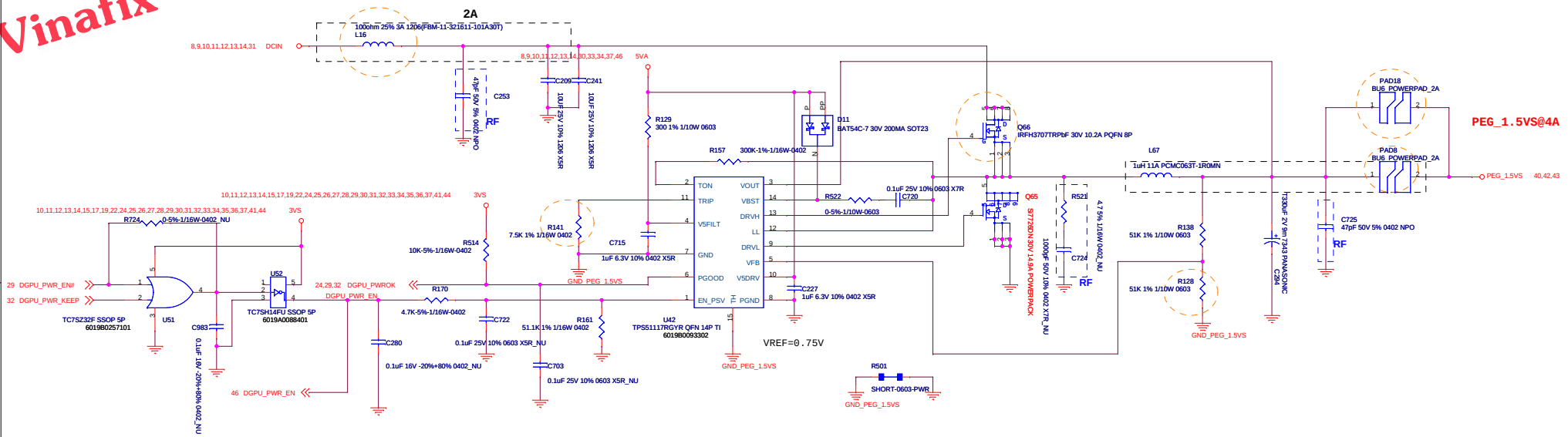
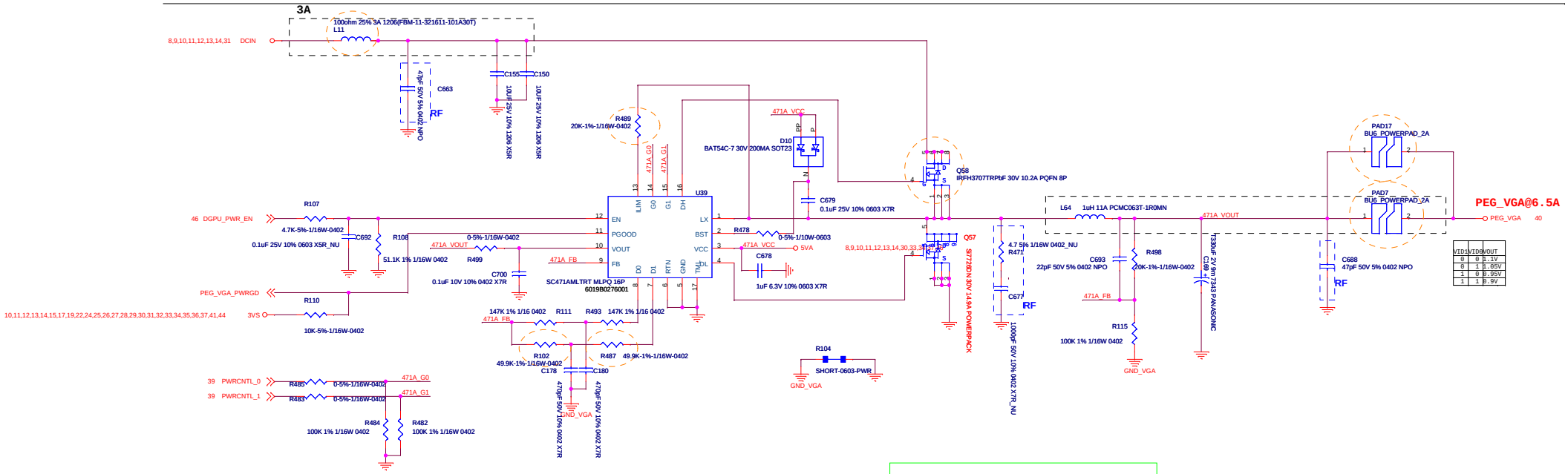
CHANGE by Shiun-Chin Chang DATE Thursday, July 02, 2009





VID1	VID0	VOUT
0	0	1.1V
0	1	1.05V
1	0	0.95V
1	1	0.9V

PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

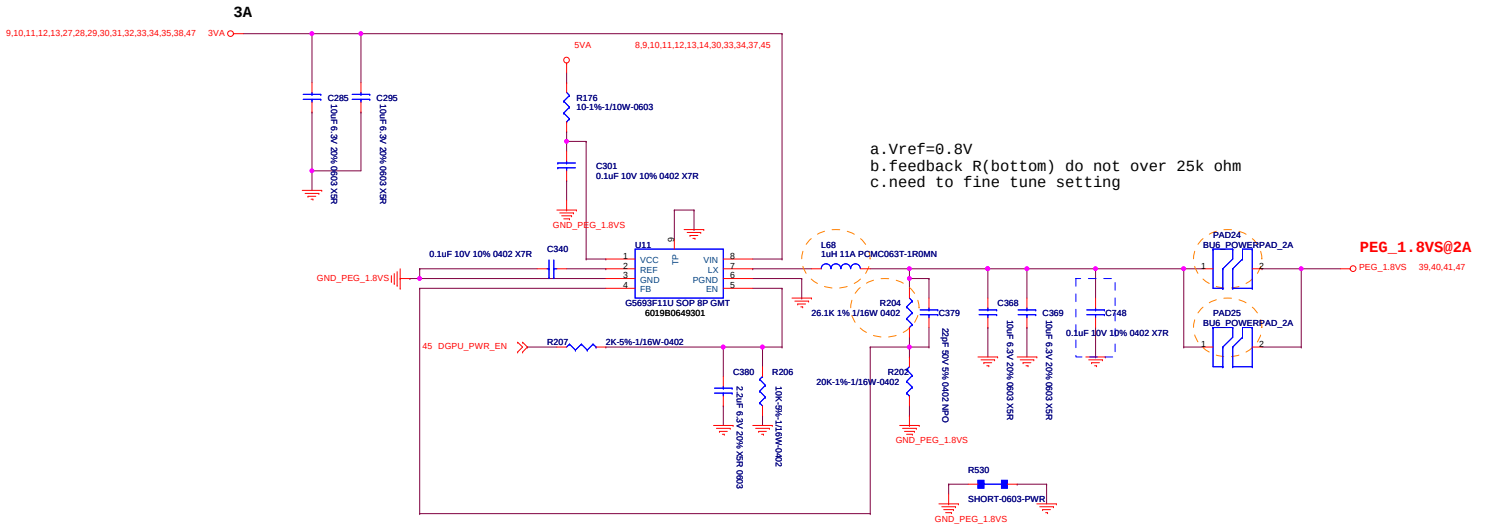
Page 45:
SW Gfx: Stuff
UMA: OPEN

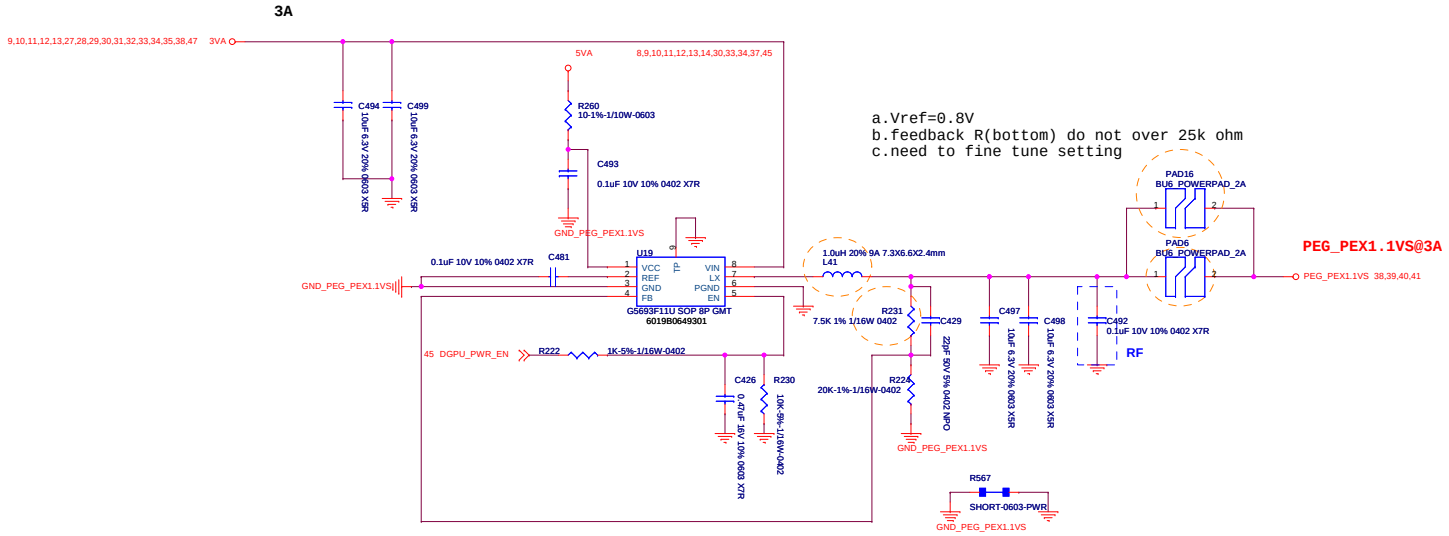
INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF)
VGA Power

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

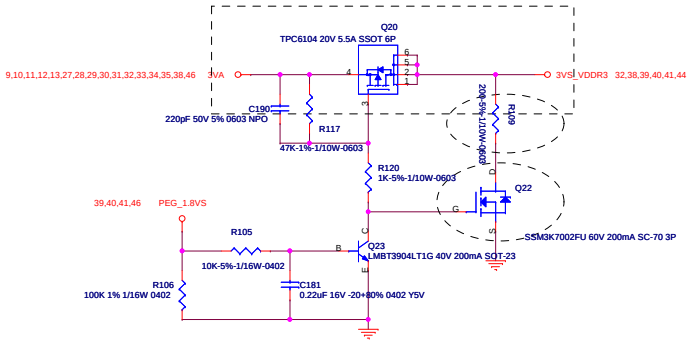
CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009 SHEET 45 of 49





Page 46:
SW Gfx: Stuff
UMA: OPEN

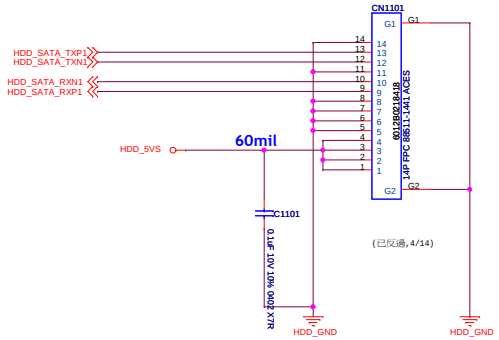
INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) VGA Power			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang DATE: Thursday, July 02, 2009		SHEET: 46 of 49	



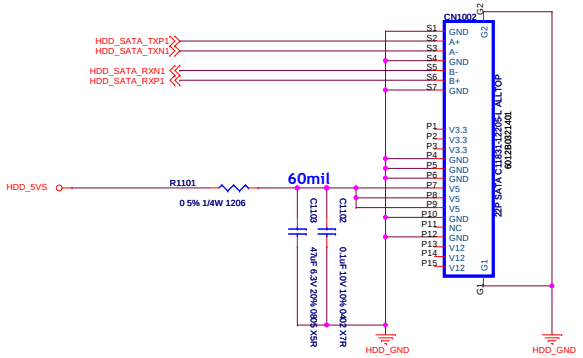
Page 47:
SW Gfx: Stuff
UMA: OPEN

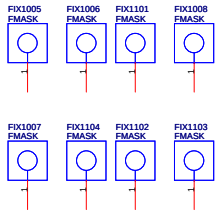
INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF) VGA Power			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Thursday, July 02, 2009	SHEET: 47 of 49	

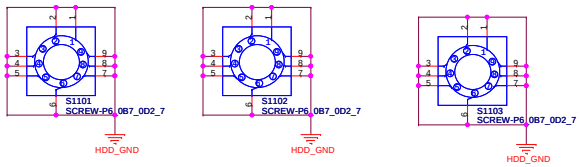
HDD Board CN TO MB



HDD I/F

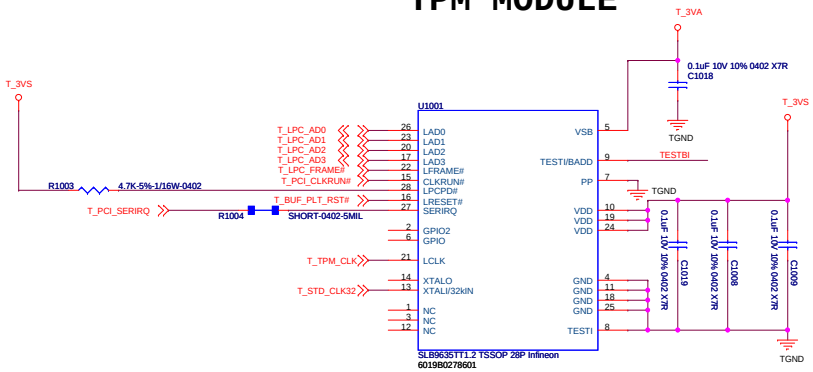




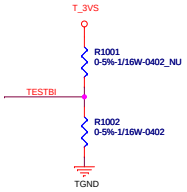


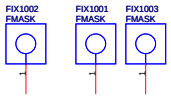
INVENTEC			
TITLE: **BAP41/BAP51 (Montevina SFF) HDD Board**			
SIZE: Custom	CODE: A02	DOC.NUMBER: D-CS-1310A2292001-ALG	REV: A02
CHANGE by: Shiun-Chin Chang	DATE: Monday, June 29, 2009	SHEET: 48 of 49	

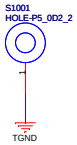
TPM MODULE



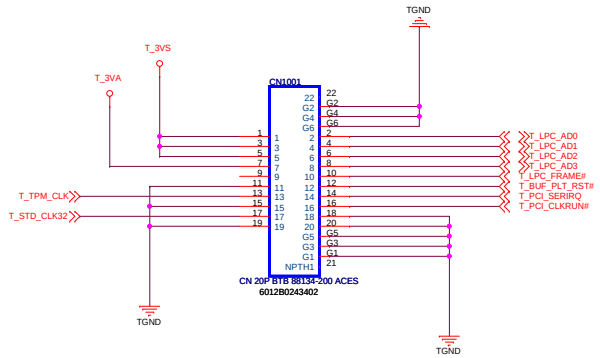
TESTBI	I/O ADDRESS
	CONFIG REGISTER
HIGH	4EH
LOW	2EH







TO MINI-CARD/B



INVENTEC

TITLE: BAP41/BAP51 (Montevina SFF) TPM Board

SIZE	CODE	DOC.NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

CHANGE by: Shiun-Chin Chang | DATE: Monday, June 29, 2009 | SHEET 49 of 49