Compal Confidential

LA-E822P Schematics Document

INTEL Kabylake-U CPU with DDR4 + AMD GPU(R17M)

AIO M/B

02/21 , 2017

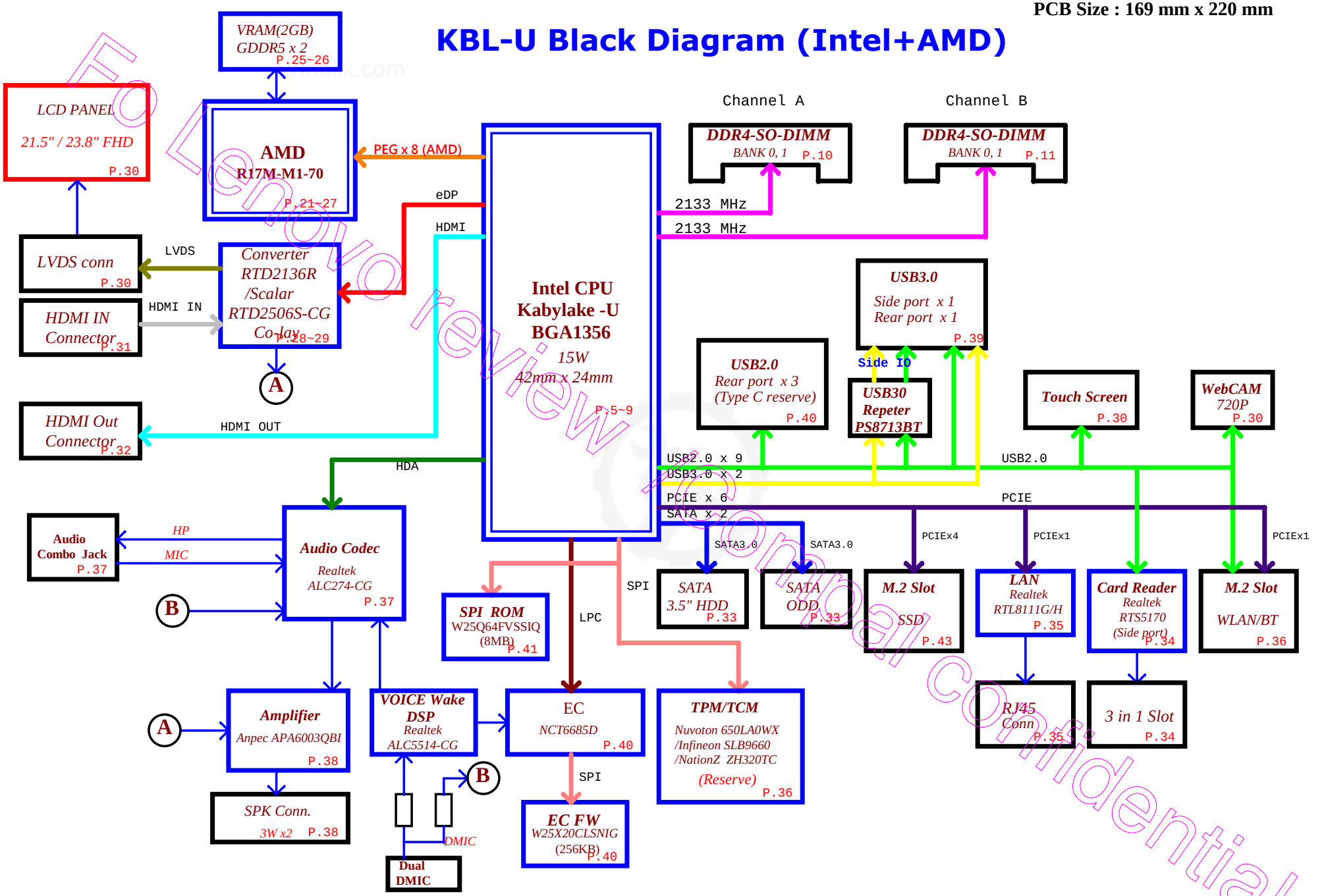
REV : 0.2

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.			
Title: *Cover Page*			
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 1 of 60		

PCB Size : 169 mm x 220 mm

KBL-U Black Diagram (Intel+AMD)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date 2016/09/24	Title: Black Diagram
			Size: D26 Custom; Document Number: LA-E822P M/B; Rev: 0.1
			Date: Friday, March 31, 2017; Sheet 2 of 60

PCIE Port Table

No.	Port	Device
1	5	DGPU
2	6	DGPU
3	7	DGPU
4	8	DGPU
5	9	LAN
6	10	WLAN/BT
7	11	NA
8	12	NA
9	13	SSD
10	14	SSD
11	15	SSD
12	16	SSD

SATA Port Table

No.	Port	Device
0	11	ODD
1A	12	HDD
1B	15	NA
2	16	NA

USB2.0 Port Table

Port	Device
1	Cardreader Side IO
2	USB 3.0/2.0 Side IO
3	USB 2.0 Rear IO
4	Web Camera
5	USB 3.0/2.0 Rear IO
6	Mini Card(WiFi/BT)
7	USB 2.0 Rear IO(TYPE-C)
8	USB 2.0 Rear IO
9	NC
10	TOUCH

USB3.0 Port Table

No.	Port	Device
1	1	USB30 rear IO
2	2	USB30 rear IO (TYPE-C)
3	3	USB30 rear IO (TYPE-C)
4	4	USB30 side IO (Debug)

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	

SKU ID(Project) Table

SKU (UMA&DIS)	DCA30(C5) EVT BOM Configure Table
431A7A38L01 Scalar SAMSUNG (DIS)	7500U@ PCB@ DIS@ C4@ IRCAM@ RF@ U22@ DEBUG@ Dischg@ NFAN_SW@ GPU@ SC@ HDMIIN@ TYPE_C@ SW_TPM@ SMART@ WOV@
X4EA7A38L01	EMI@ ESD@ DIS_EMI@ HDMIIN_EMI@ HDMIIN_ESD@ U22_EMI@ TYPE_C_EMI@ TYPE_C_ESD@
431A7A38L02 Scalar SAMSUNG (DIS)	7200U@ PCB@ DIS@ C4@ IRCAM@ RF@ U22@ DEBUG@ Dischg@ NFAN_SW@ GPU@ SC@ HDMIIN@ N_TYPE_C@ SW_TPM@ SMART@ WOV@
X4EA7A38L02	EMI@ ESD@ DIS_EMI@ HDMIIN_EMI@ HDMIIN_ESD@ U22_EMI@
431A7A38L03 Scalar Micron (DIS)	7100U@ PCB@ DIS@ C5@ IRCAM@ RF@ U22@ DEBUG@ Dischg@ NFAN_SW@ GPU@ SC@ HDMIIN@ N_TYPE_C@ SW_TPM@ SMART@ WOV@
X4EA7A38L03	EMI@ ESD@ DIS_EMI@ HDMIIN_EMI@ HDMIIN_ESD@ U22_EMI@
431A7A38L04 Scalar Hynix (DIS)	6006U@ PCB@ DIS@ C4@ IRCAM@ RF@ U22@ DEBUG@ Dischg@ NFAN_SW@ GPU@ SC@ HDMIIN@ N_TYPE_C@ SW_TPM@ SMART@ WOV@
X4EA7A38L04	EMI@ ESD@ DIS_EMI@ HDMIIN_EMI@ HDMIIN_ESD@ U22_EMI@
431A7A38L05 Converter (UMA)	4415U@ PCB@ UMA@ C5@ IRCAM@ RF@ U22@ DEBUG@ Dischg@ NFAN_SW@ CVT@ N_TYPE_C@ Nuvton@ TPM@ NSMART@ NWOV@
X4EA7A38L03	EMI@ ESD@ U22_EMI@
451A7A38L06 Converter (UMA)	4415U@ PCB@ UMA@ C4@ IRCAM@ RF@ U22@ DEBUG@ Dischg@ NFAN_SW@ CVT@ N_TYPE_C@ ST@ TPM@ NSMART@ NWOV@
X4EA7A38L03	EMI@ ESD@ U22_EMI@
451A7A38L07 Scalar Micron (DIS)	7200U@ PCB@ DIS@ C4@ IRCAM@ RF@ U22@ DEBUG@ Dischg@ NFAN_SW@ GPU@ SC@ HDMIIN@ N_TYPE_C@ SW_TPM@ NSMART@ NWOV@
X4EA7A38L05	EMI@ ESD@ DIS_EMI@ HDMIIN_EMI@ HDMIIN_ESD@ U22_EMI@

BOM Structure Table

BOM Structure	BTO Item
PCB@	LA-D951P 6 Layer PCB
@ and @xxxxx@	Unpop
TP@	Test point
CONN@	Connector part control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
CVT@	eDP to LVDS Converter IC
SC@	Scaler
SW_TPM@	NO HW TPM
DIS@	GPU SKU
DIS_EMI@	GPU EMI pop component
X76@	X76 for VRAM config
UMA@	UMA SKU
C @	C4 Only
C5@	C5 Only
TPM@	HW TPM
HDMIIN@	HDMI-IN
HDMIIN_EMI@	HDMI-IN EMI pop component
HDMIIN_ESD@	HDMI-IN ESD pop component
TYPE_C@	USB TYPE-C
TYPE_C_EMI@	USB TYPE-C EMI pop component
TYPE_C_ESD@	USB TYPE-C ESD pop component
N_TYPE_C@	TYPE-C co-lay USB20 pop component
IRCAM@	IR Cemara
SMART@	SMART power on
WOV@	Wake On Voice
NWOV@	Wake On Voice unpop component
RF@	RF pop component
U22@	For U22 CPU crystal pop component
U22_EMI@	For U22 CPU crystal EMI pop component
U42@	For U42 CPU crystal pop component
U42_EMI@	For U42 CPU crystal EMI pop component

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DSW	3.3V DSW on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VALW_S5	12V always on power rail	ON	ON	ON
+1.8VALW_S5	1.8V always on power rail	ON	ON	ON
+1.0VALW_S5	1.0V always on power rail	ON	ON	ON
+1.0V_VCCST_S3	1.0V power rail for CPU VCCST	ON	ON	OFF
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+CPU_VCCIO_S0	0.95V power rail for CPU VCCIO	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+1.05VS_S0	+1.5VS on power rail for CPU VCCSA	ON	OFF	OFF
+CPU_CORE	VCC Core voltage for CPU	ON	OFF	OFF
+VCC_GT_S0	Core voltage for CPU graphic	ON	OFF	OFF
+3VS_DGPU_S0	3.3V power rail for DIS graphic	ON	OFF	OFF
+VGA_CORE_S0	VCC Core voltage for GPU	ON	OFF	OFF
+1.05VS_DGPU_S0	1.05V power rail for DIS graphic	ON	OFF	OFF
+1.35VS_VGA_S0	1.35V power rail for VRAM	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 Address

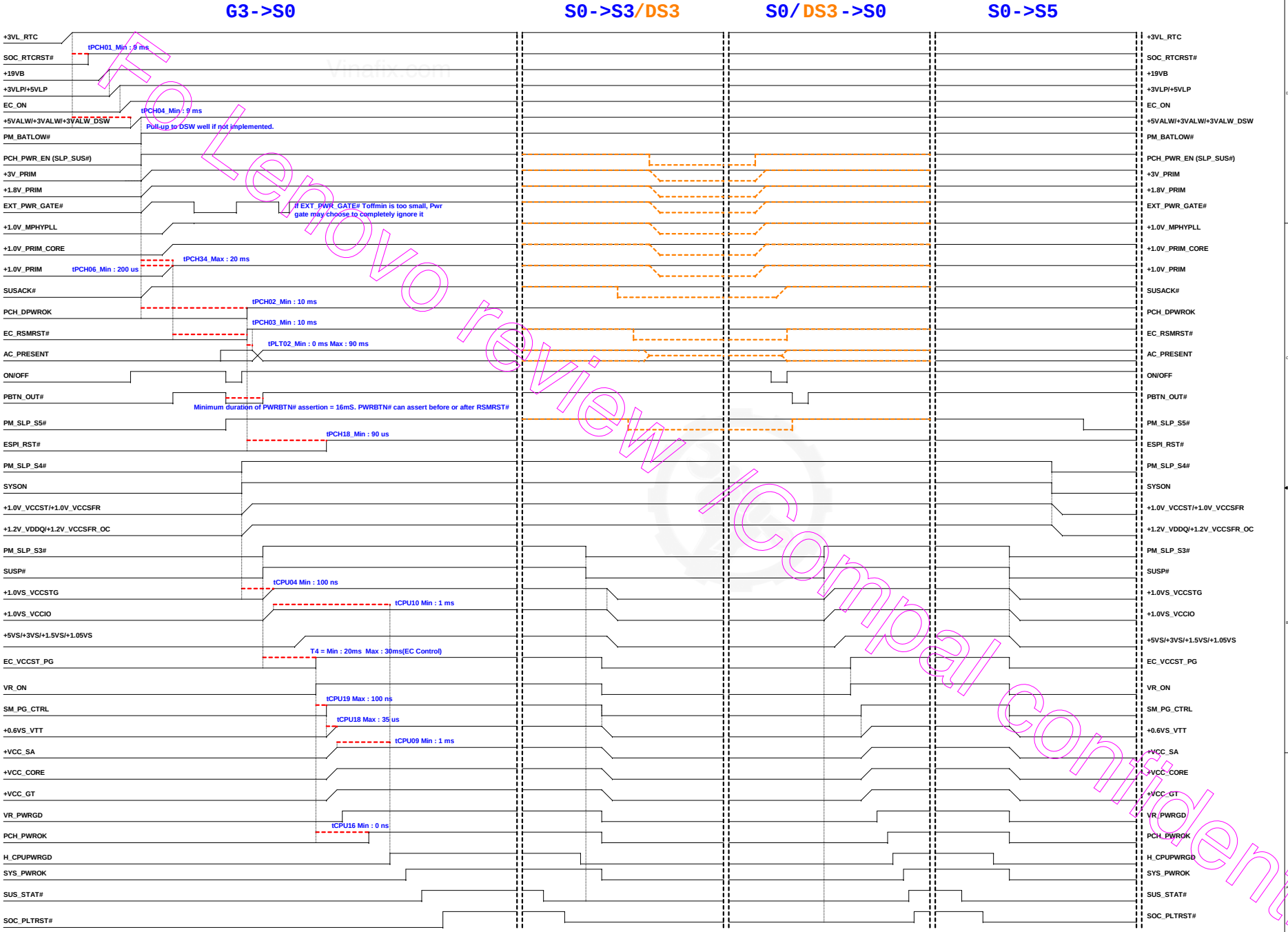
Device	Address	HEX
RTD-2136N	1001-0100xb	94
Converter	0110-0010xb	62

PCH SM Bus Address

Device	Address	HEX
GPU	0100-1100xb	4CH
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

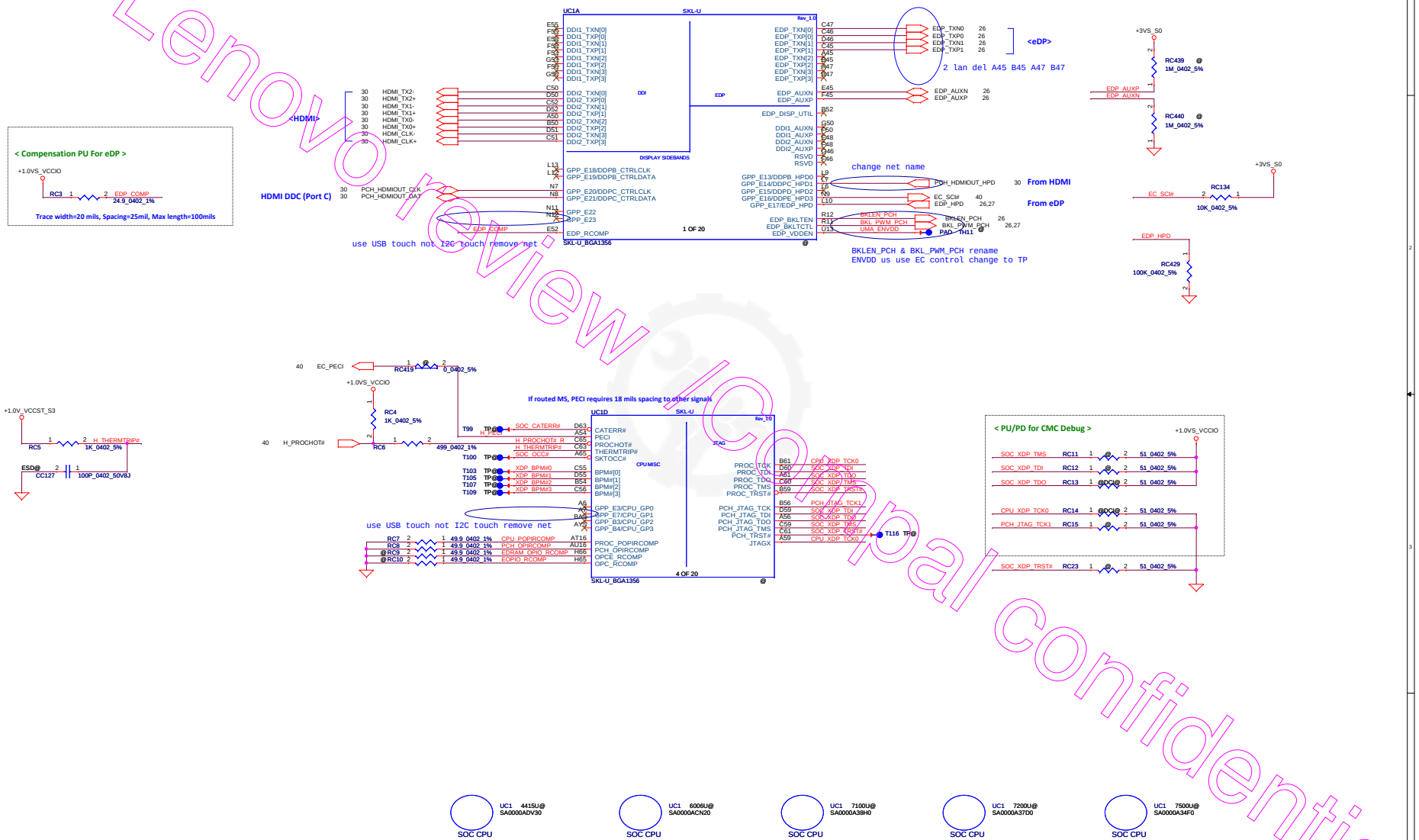
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date	2013/09/01
Title	Notes List		
Size C	Document Number LA-E822P M/B		Rev 0.1
Date: Friday, March 31, 2017	Sheet 3 of 60		

[DCA30-PWR Sequence_KBLR- U42_DDR4_Volume_S0iX]



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date	2013/09/01

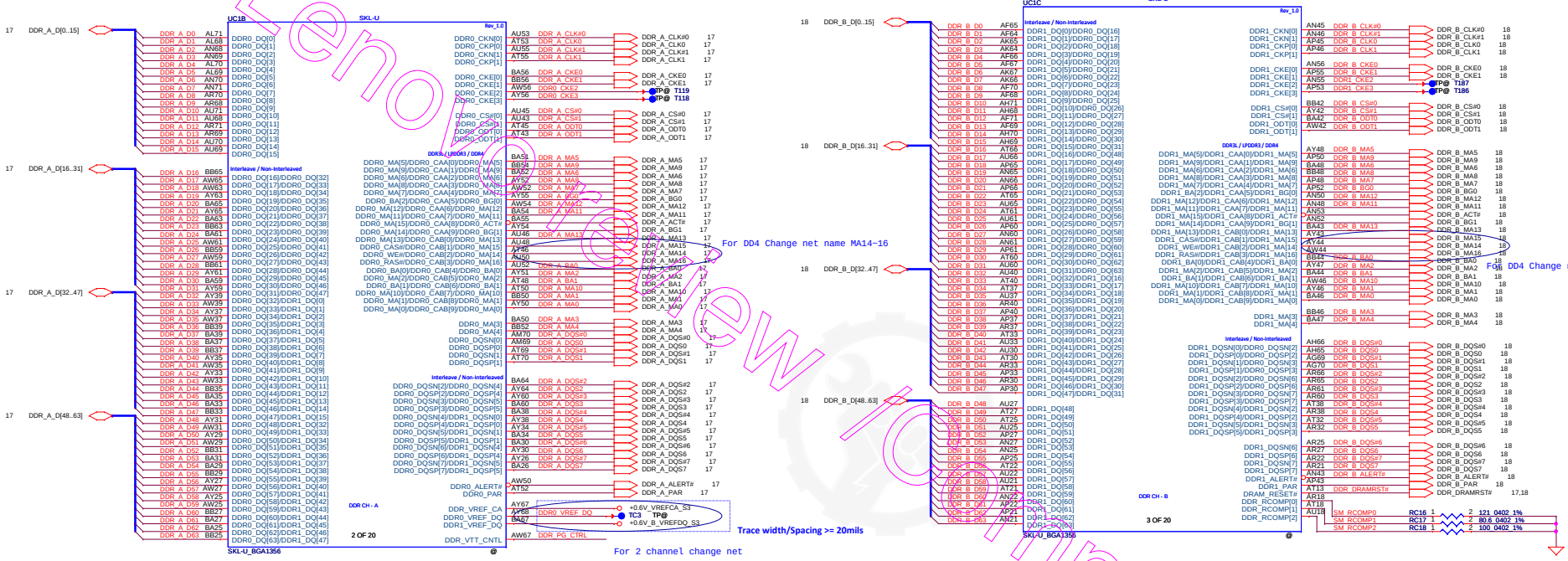
Title	PWR Sequence		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 4 of 60		

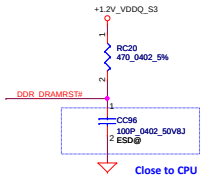


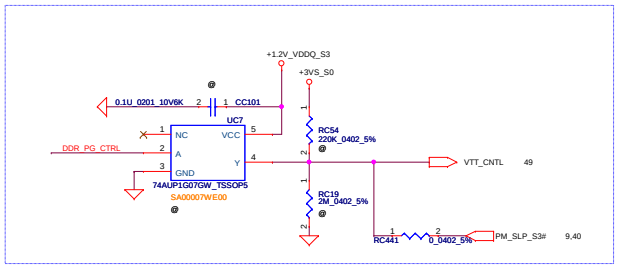
Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

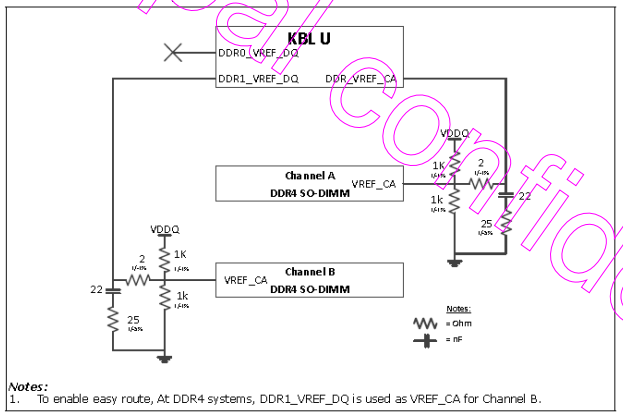
Compal Electronics, Inc.			
Title	SKL-U(1/12)DDI,EDP,MISC,CMC		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 5 of 60		

Interleaved Memory







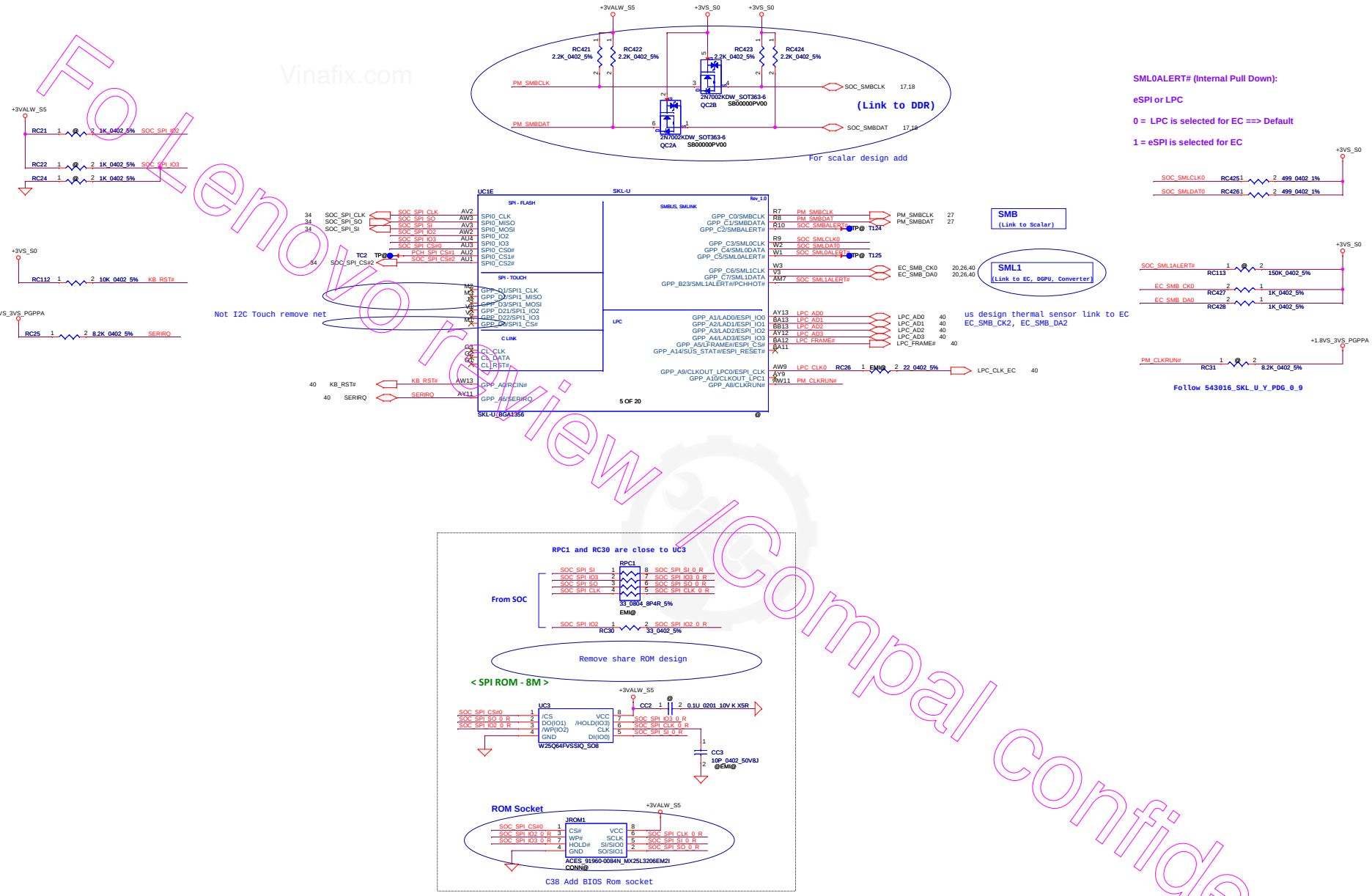


Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title	SKL-U(2/12)DDR3L		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 6 of 60		



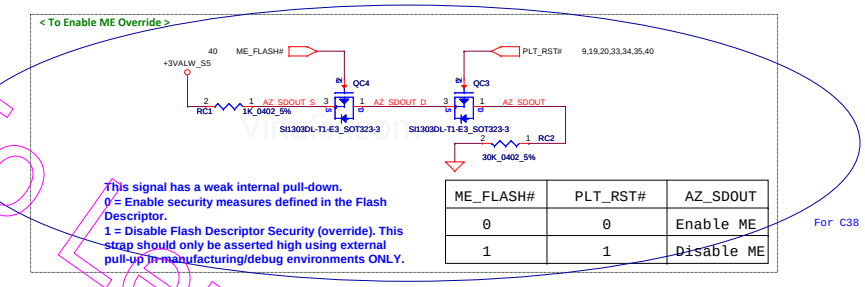
Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,SMB,LPC,ESPI

Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

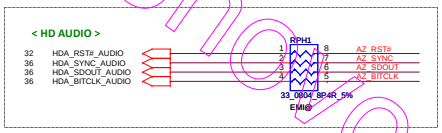
Date: Friday, March 31, 2017 | Sheet 7 of 60

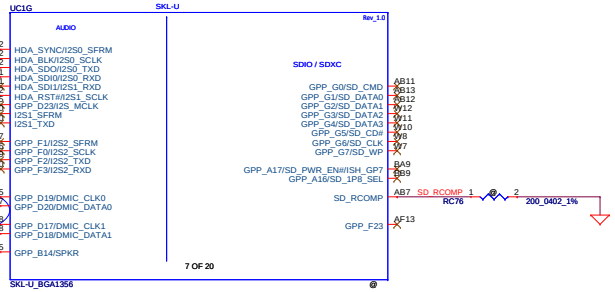


This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

ME_FLASH#	PLT_RST#	AZ_SDOUT
0	0	Enable ME
1	1	Disable ME

For C38 design add



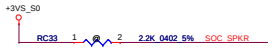


36 HDA_SDIN0
AZ_SYNC
AZ_BITCLK
AZ_SDOUT
AZ_RST#

T188 TP@ OSC_DMIC_CLK0
T189 TP@ OSC_DMIC_DAT0
T190 TP@ OSC_DMIC_CLK1
T191 TP@ OSC_DMIC_DAT1

12/02 Reserve test point

36 SOC_SPKR



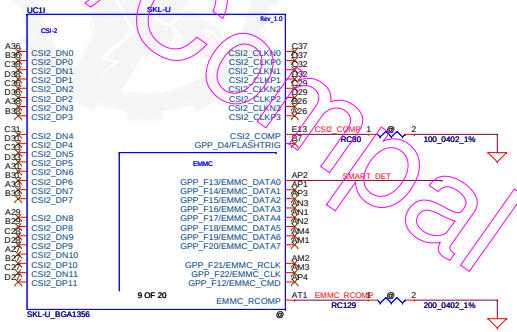
SPKR (Internal Pull Down):

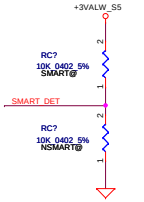
TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

SMART_PWON	Smart power on select
H	Support Smart Power On
L	No Support Smart Power On





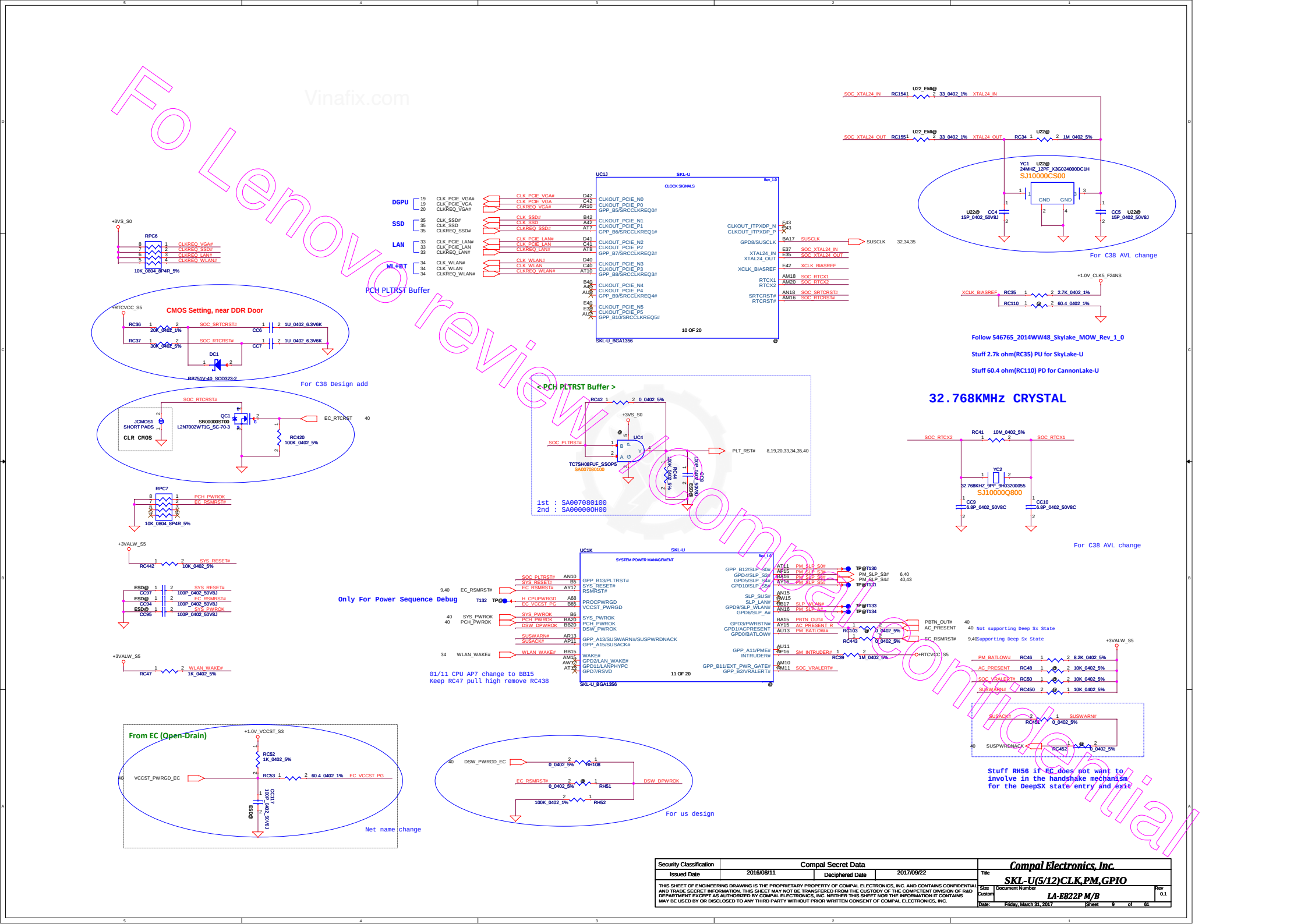
Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 8 of 60



Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.	
Title	SKL-U(5/12)CLK,PM,GPIO
Size: Custom	Document Number: LA-E822P M/B
Rev: 0.1	
Date: Friday, March 31, 2017	Sheet 9 of 61

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

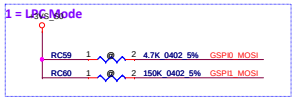
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

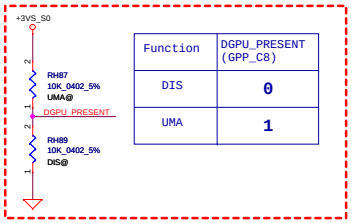
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

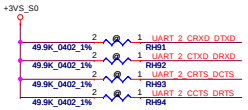
0 = SPI Mode ==> Default

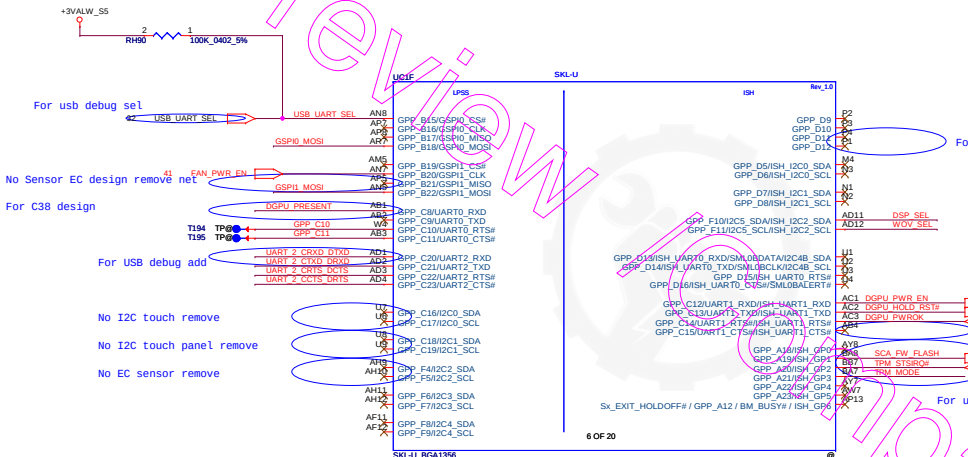
1 = LPC Mode

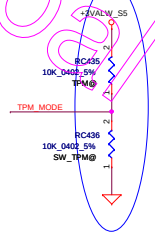


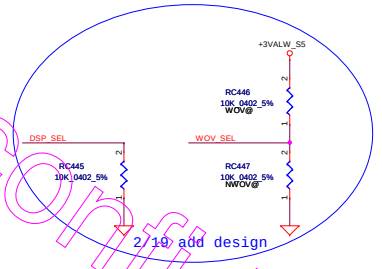


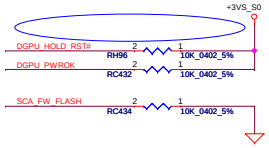
Function	DGPU_PRESENT (GPP_C8)
DIS	0
UMA	1











GPU_EVENT# & GC6_FB_EN for NV GPU design

WOV_SEL (GPP_F11)	DSP_SEL (GPP_F10) L	DSP_SEL (GPP_F10) H
L	AMP Only (DCA10/30/70)	DSP + AMP (DCA70 Only)
H	5514 + AMP (DCA10/30/70)	DSP+5514+AMP (DCA70 Only)

Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 10 of 60

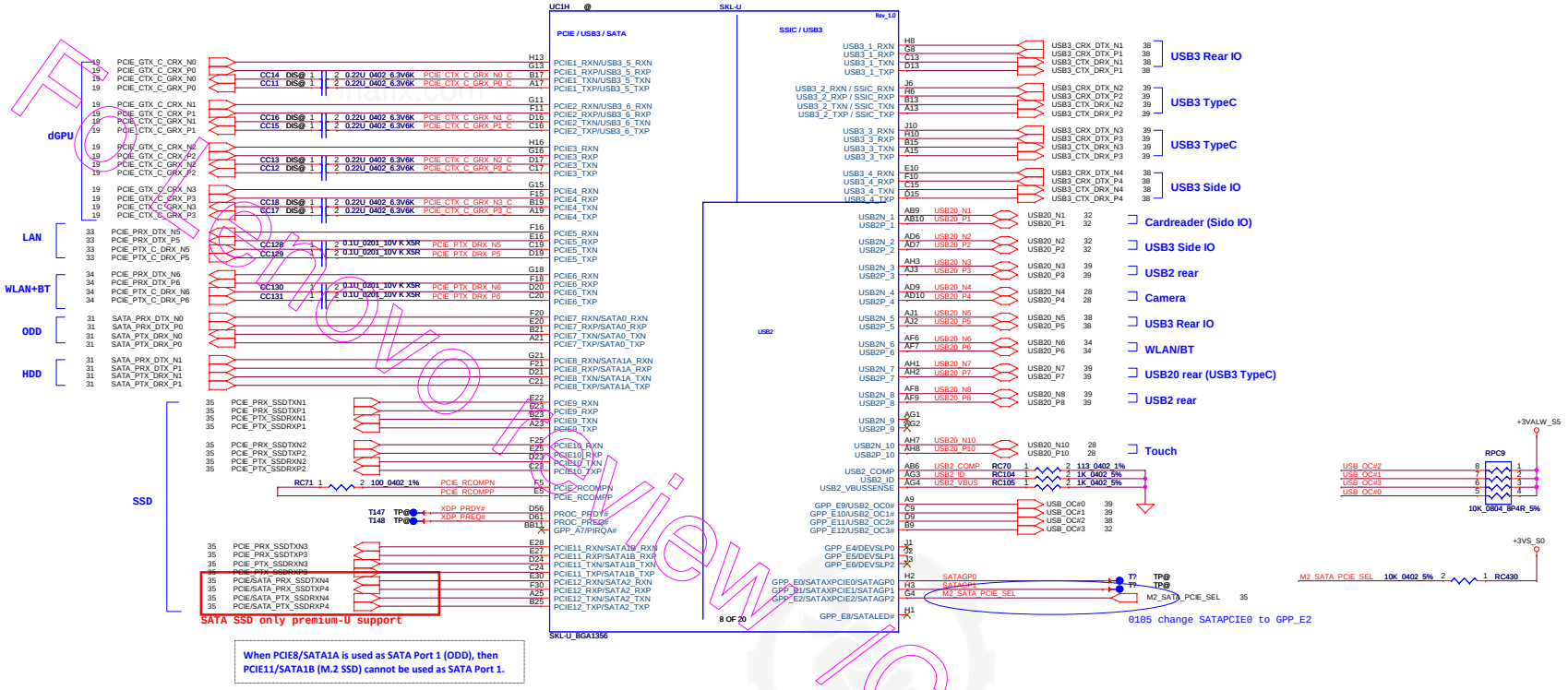


Figure 3-1. HSIO Multiplexing on PCH-U

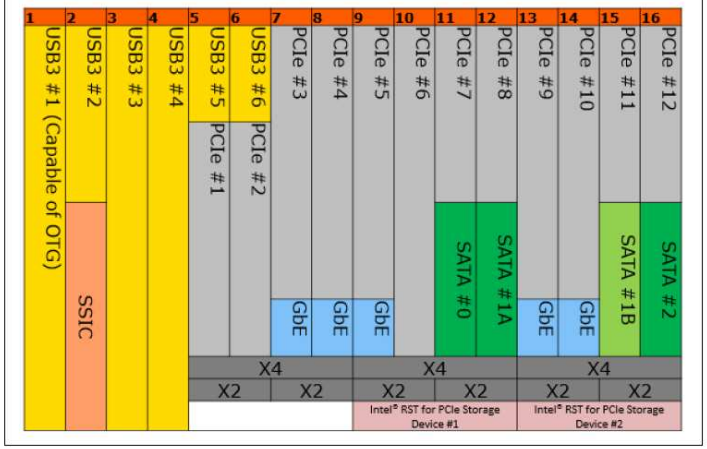


Table 1-2. PCH SKUs

Features	Base-U	Premium-U	Premium-Y
Intel® Rapid Storage Technology (Intel® RST)	AHCI Mode	AHCI and RAID Mode	AHCI and RAID Mode
Total USB 3.0 Ports	4	6	6
Total USB 2.0 Ports	8[1]	10[2]	6[3]
Total SATA 3.0 Ports (Max. 6Gb/s)	2	3	2
Total PCI Express* Lanes (Gen)	10 (2.0)	12 (3.0)	10 (3.0)
Total Intel® RST for PCIe* Storage and SATA Express[4] Storage Devices	0	2[5]	2[5]
Total CSI2 lanes	8 lanes	12 lanes	12 lanes

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)
5. Intel® RST PCIe supports RAID configuration 0/1

Table 1-3. PCH HSIO Detail

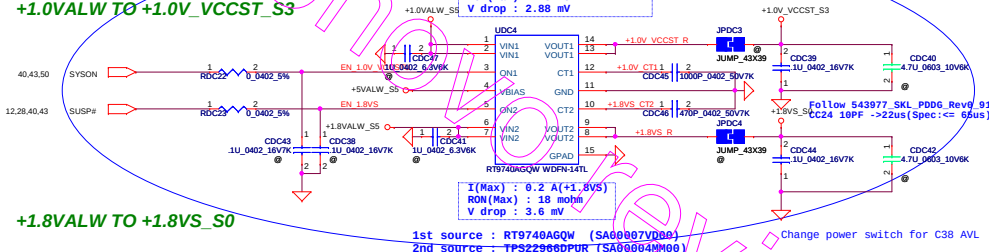
SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/08/11	Deciphered Date 2017/09/22	Title: SKL-U(7/12)PCIE,USB,SATA
			Size: Custom; Document Number: LA-E822P M/B; Rev: 0.1
			Date: Friday, March 31, 2017; Sheet 11 of 60

+1.0VALW TO +1.0V_VCCST_S3

VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

I(Max) : 0.16 A(+1.0V_VCCST)
RON(Max) : 18 mohm
V drop : 2.88 mV



I(Max) : 0.2 A(+1.8VS)
RON(Max) : 18 mohm
V drop : 3.6 mV

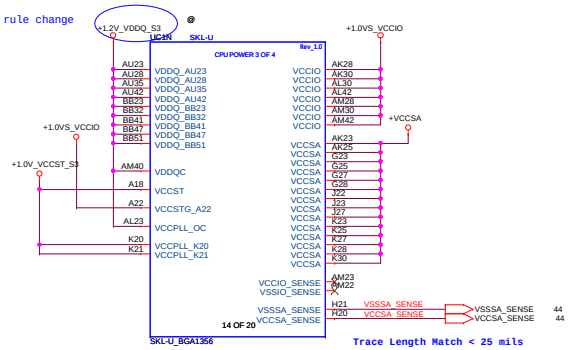
+1.8VALW TO +1.8VS_S0

1st source : RT9740AGQW (SA00007VD00)
2nd source : TPS22966DPUR (SA00004MM00)

Follow 543977_SKL_PDDG_Rev0_91
CC24 10PF ->22us(Spec:<= 65us)

Change power switch for C38 AVL

Follow net name rule change

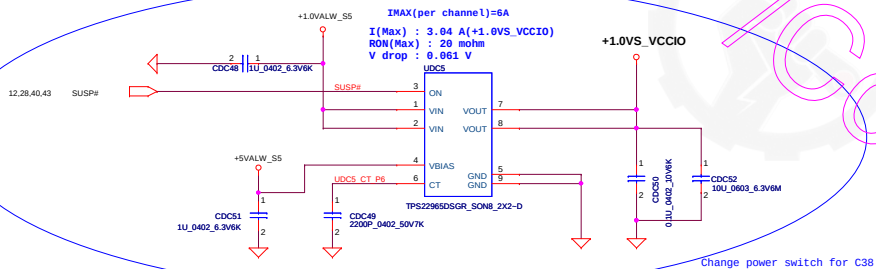


Trace Length Match < 25 mils

+1.0VALW TO +1.0VS_VCCIO

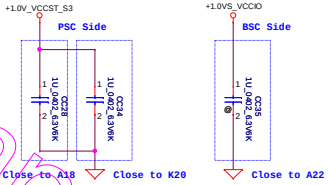
IMAX(per channel)=6A

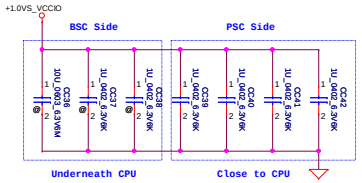
I(Max) : 3.04 A(+1.0VS_VCCIO)
RON(Max) : 20 mohm
V drop : 0.061 V

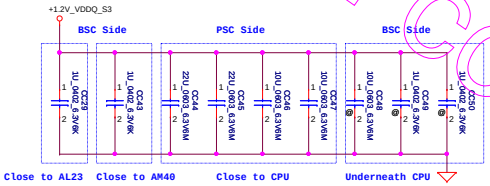


Change power switch for C38 AVL

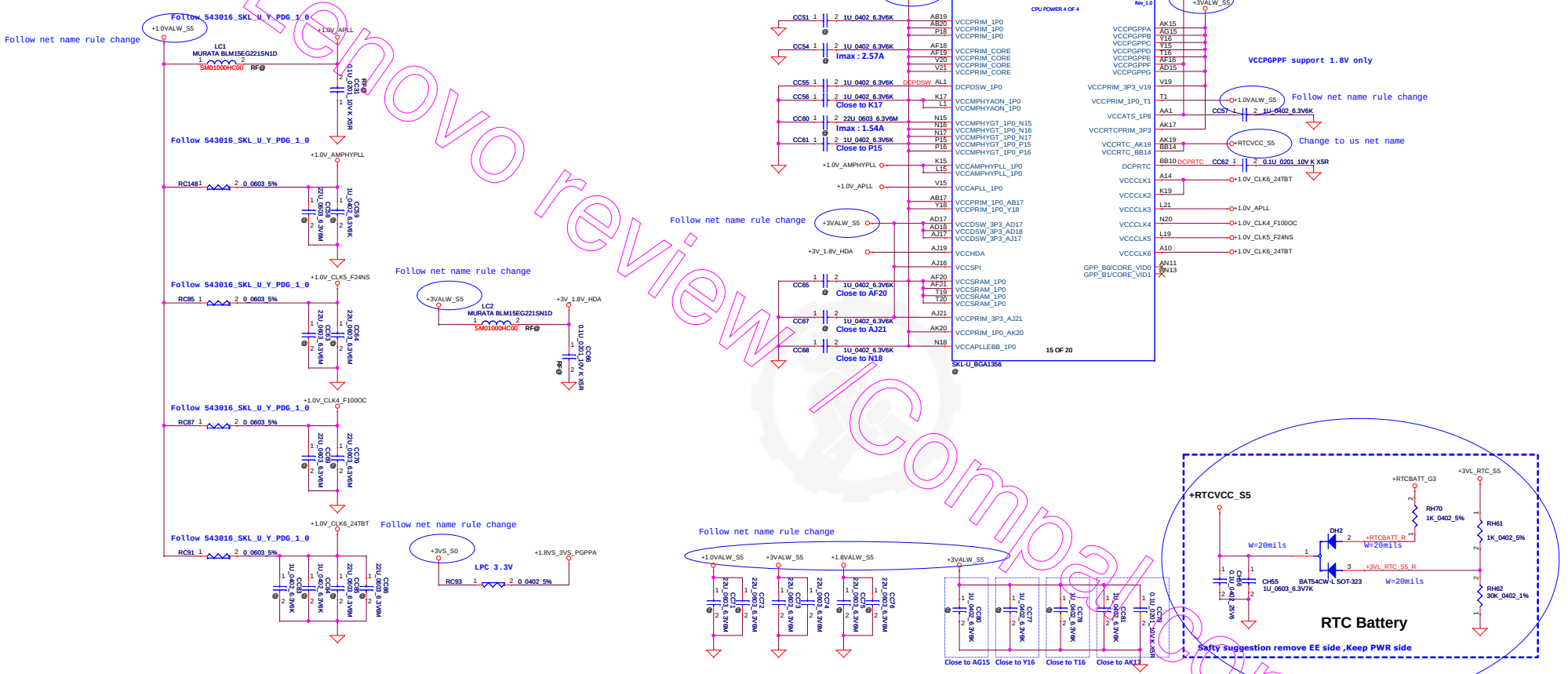
1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)







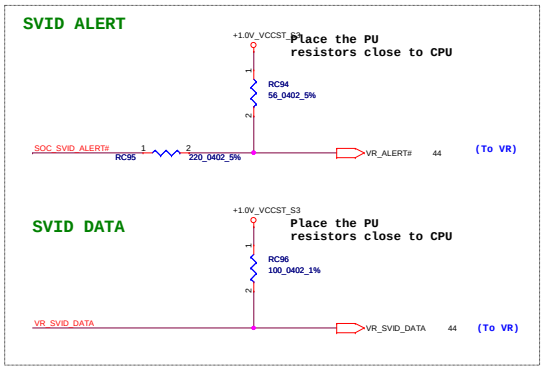
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/08/11	Deciphered Date 2017/09/22	Title SKL-U(8/12)Power
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Custom / Document Number LA-E822P M/B / Rev 0.1
			Date: Friday, March 31, 2017 Sheet 12 of 60



Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

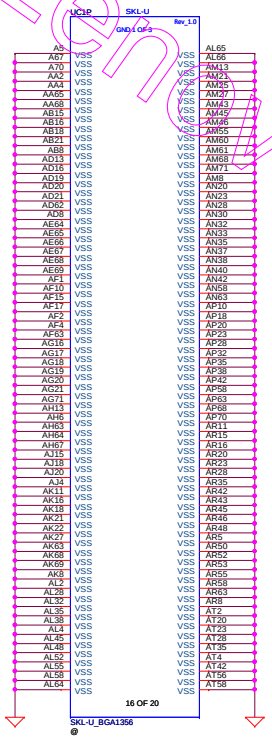
Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet: 13	of: 61	

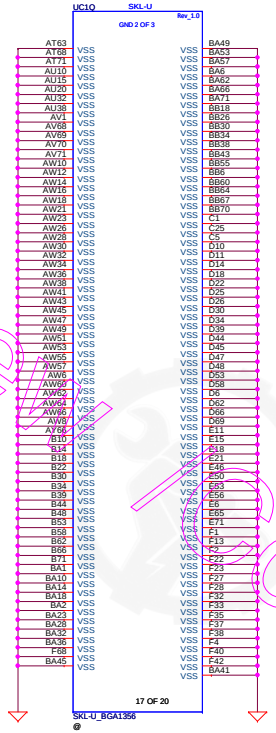
Ball #	Ball Names R-U42	Ball Names U22
C7	XTAL24_OUT	NC
E3	XTAL24_IN	NC
E35	NC	XTAL24_OUT
E37	NC	XTAL24_IN
AK42	VCCCORE	VccGTx
AK43		
AK45		
AK46		
AK48		
AK50		
AL43		
AL46		
AL50		
AM48		
AM50		
AM52		
J43		VCCGT
J45		
J46		
J48		
J50		
J52		
K48		
K50		
A48		
A53		
AK52	RSVD	VccGTx
K52	RSVD	VCCGT

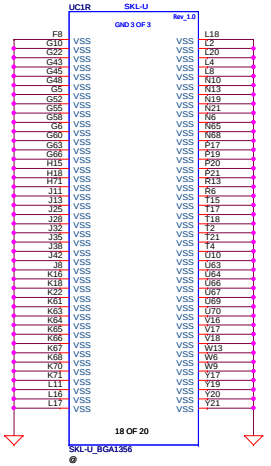


Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

Compal Electronics, Inc.			
Title	SKL-U(10/12)Power,SVID		
Size	Document Number		Rev
Custom	LA-E822P M/B		0.1
Date:	Friday, March 31, 2017	Sheet 14 of 60	



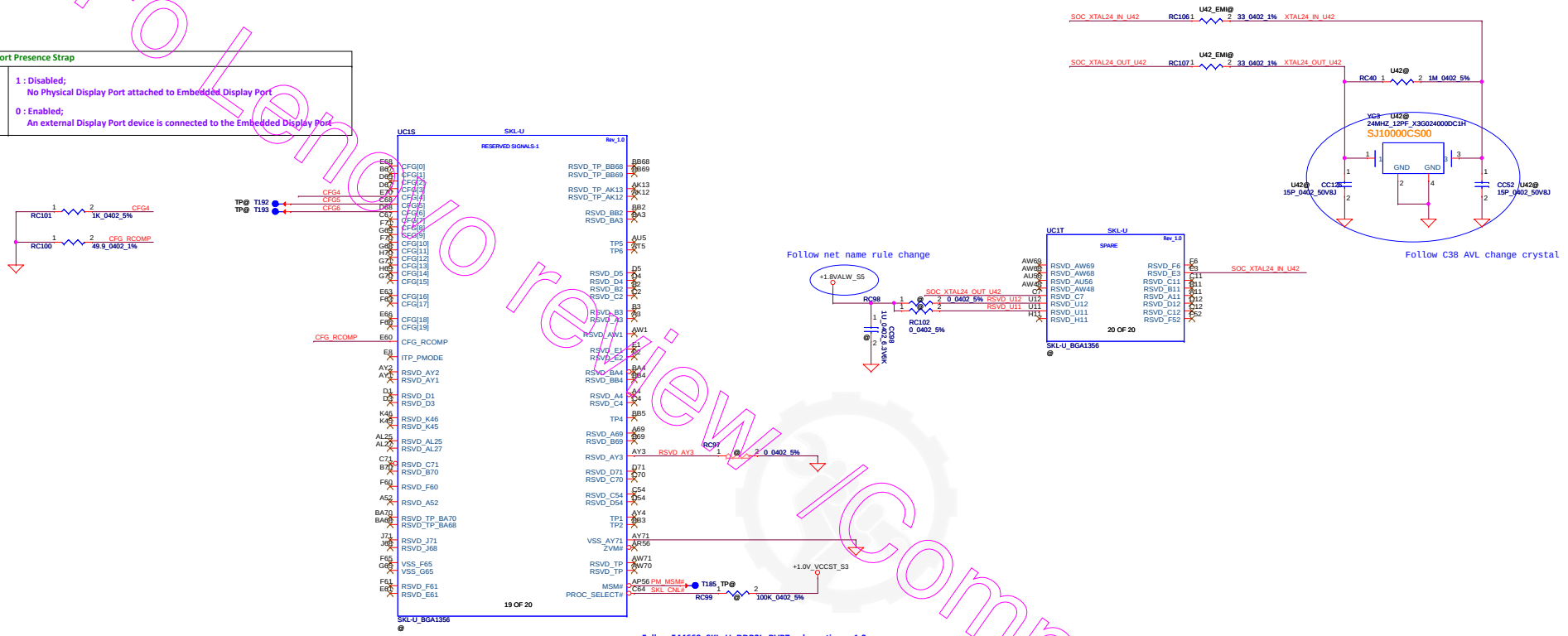




Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

Compal Electronics, Inc.			
Title	SKL-U(11/12)GND		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 15 of 60		

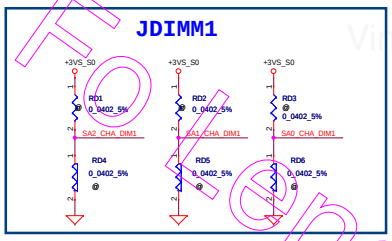
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



Security Classification	Compal Secret Data		
Issued Date	2016/08/11	Deciphered Date	2017/09/22

Compal Electronics, Inc.			
Title	SKL-U(12/12)CFG,RSVD		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 16 of 60		

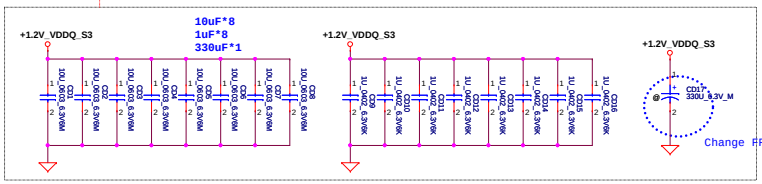
CHANNEL-A



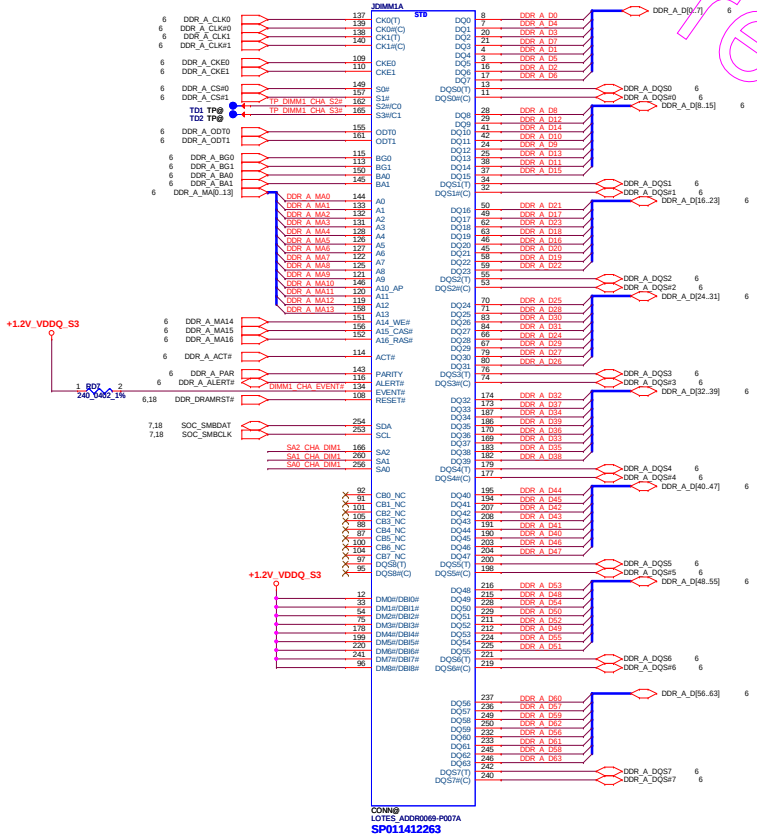
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

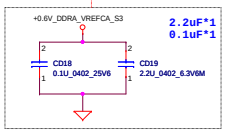
Layout Note:
Place near JDIMM1

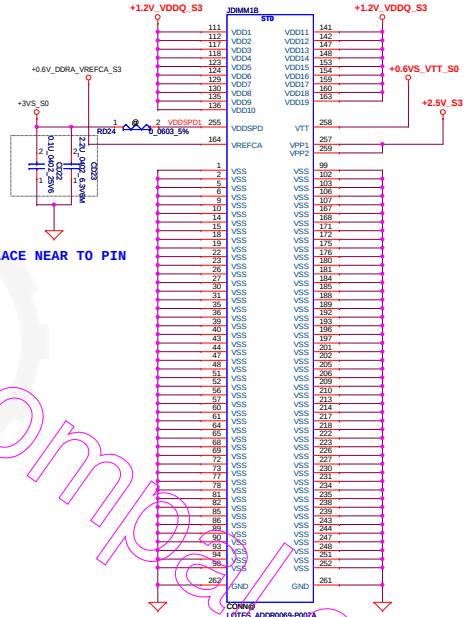


(8.0 mm)

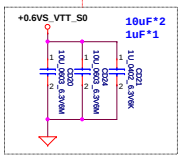


Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1

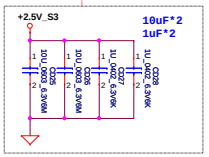


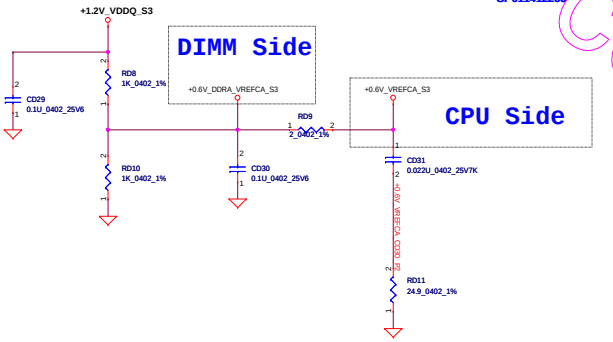


Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1

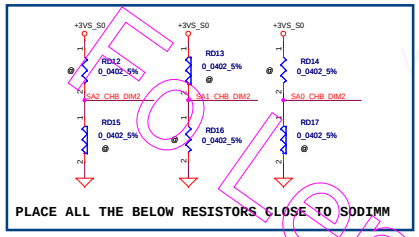




Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/12/31

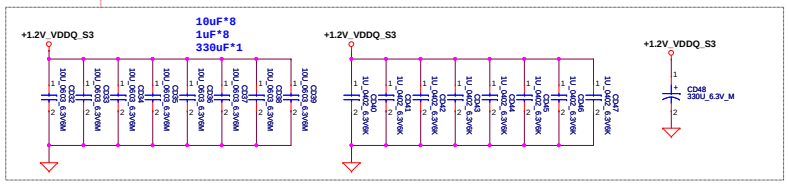
Compal Electronics, Inc.			
Title	DDR4_DIMMA		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 17 of 60		

CHANNEL-B

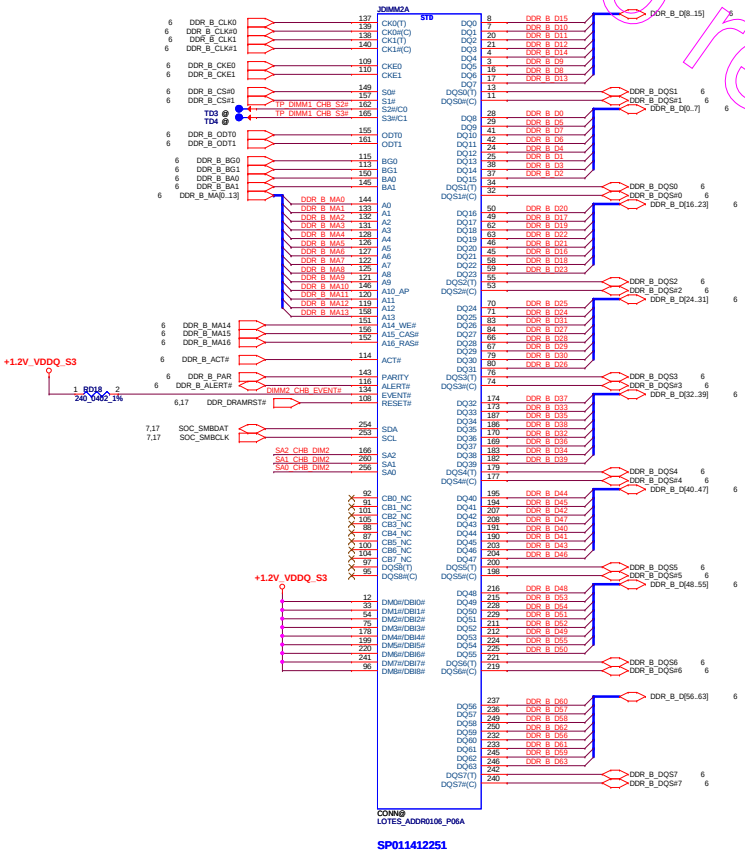


SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:0xA4
READ ADDRESS: 0xA5
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

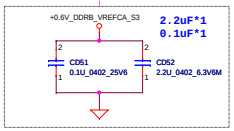
Layout Note:
Place near JDIMM2

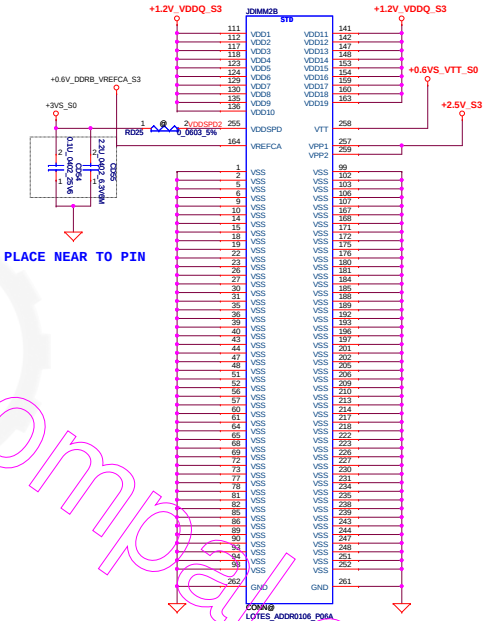


(4.0 mm) STD

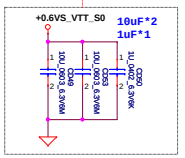


Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

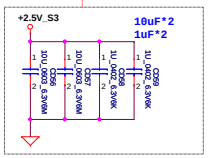


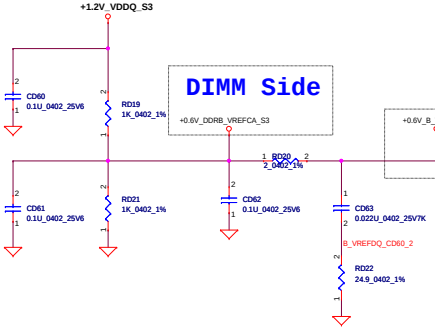


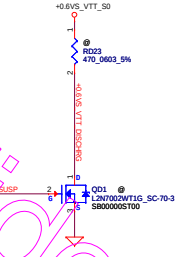
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2







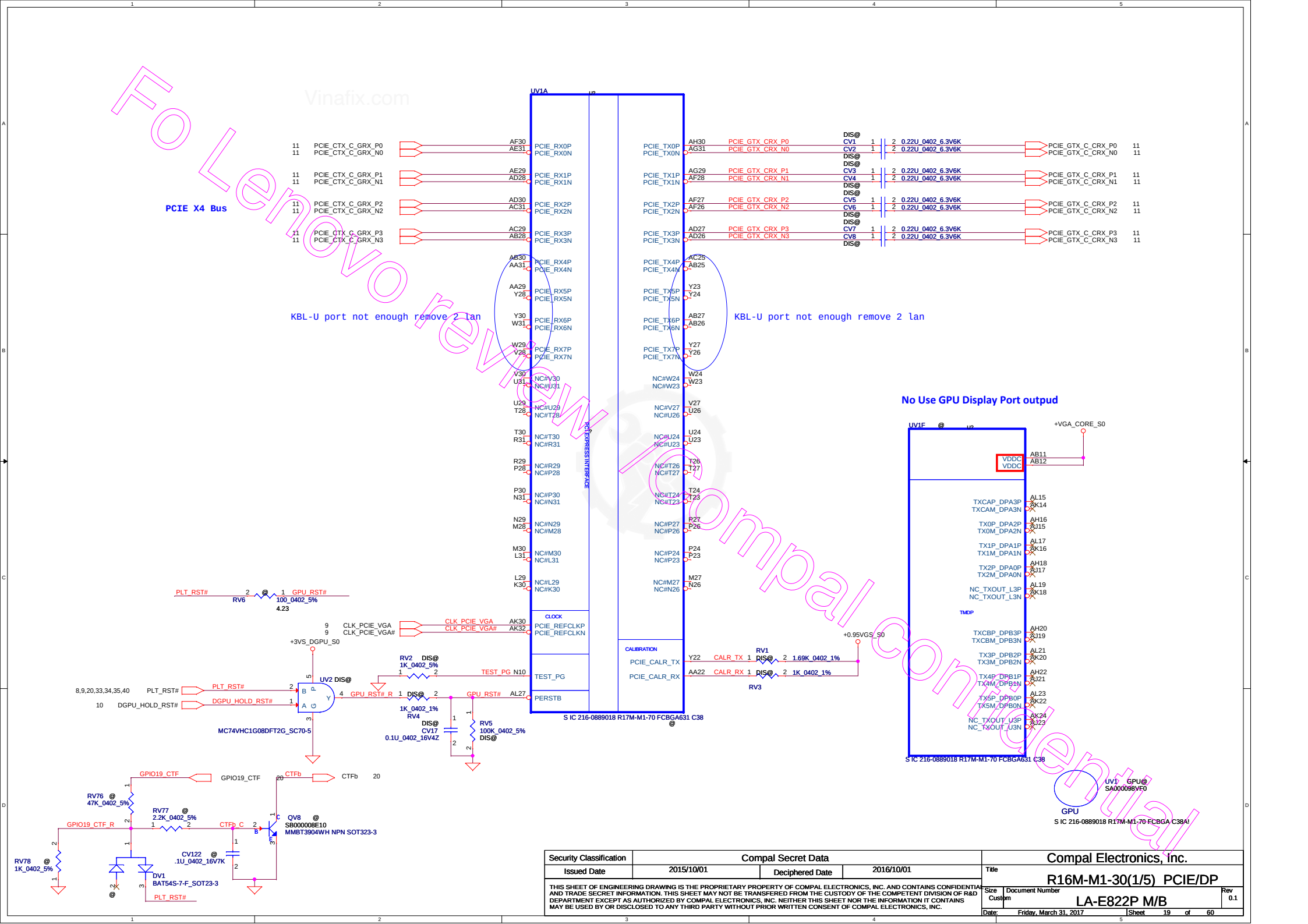
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: DDR4_DIMMB

Size	Document Number	Rev
Custom	LA-E822P M/B	0.1

Date: Friday, March 31, 2017 Sheet 18 of 60



Meso/M16M-R16M-M2-50

GPIO_11, 12, and 13 are added back.

The following balls cease to work as GPIOs or designated functional pins, and become **VDDC:**

- GPIO_1
- GPIO_2
- GPIO_14_HPD2
- GPIO_18_HPD3

The following ball ceases to work as a GPIO or designated functional pin, and becomes **NC:**

- GPIO_7_BLON

"Topaz" allocates 11 more VDDC balls so that the total number of VDDC balls becomes 36.

The following functional balls on earlier generations of ASICs are reassigned as the additional VDDC balls:

- VARY_BL (AB11)
- DIGON (AB12)
- GENERICA (AB13)
- GENERICC (W9)
- DDC2CLK (AC11)
- DDC2DATA (AC13)
- HPD1 (AC14)
- GPIO_1 (U10)
- GPIO_2 (T10)
- GPIO_18 (W10)
- GPIO_14_HPD2 (Y9)

Exo/R16M-M1-30

The following balls cease to work as GPIOs or designated functional pins, and become **NC:**

- GPIO_1
- GPIO_2
- GPIO_7_BLON
- GPIO_11
- GPIO_12
- GPIO_13
- GPIO_14_HPD2
- GPIO_18_HPD3

"Jet"/"Sun" has a total of 25 VDDC balls.

The 11 balls listed in the "Topaz" column are NC on "Jet"/"Sun".

10/26 Modify

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

When PS_2 bit 3=0, PS_0 bits [3:1] define the size of the Primary Memory Aperture as per table opposite

Setting Memory Aperture Size

PS_0[3] romidcfg_2	PS_0[2] romidcfg_1	PS_0[1] romidcfg_0	Memory Aperture Size
0	0	0	128 MB
0	0	1	256 MB
0	1	0	64 MB
0	1	1	Reserved
1	0	0	512 MB-Not Supported
1	0	1	1 GB-Not Supported
1	1	0	2 GB-Not Supported
1	1	1	4 GB-Not Supported

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11
AMD recommend 09/25

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Memeory ID Setting

Board Config[2:0]		Memory Type	Configuration	Channel Size	Vendor P/N	Compal P/N
ID	[2:0]					
0	000	Samsung	128Mx32 2PCS	1GB	K4G41325FE-HC28	SA00009TT40
1	001	Hynix	128Mx32 2PCS	1GB	H5GC4H24AJR-R0C	SA00008HQ00
2	010	Micron	256Mx32 2PCS	2GB	MT51J256M32HF-60	SA000096K40
3	011	Samsung	256Mx32 2PCS	2GB	K4G80325FB-HC28	SA000092D20
4	100	Hynix	256Mx32 2PCS	2GB	H5GC8H24MJR-R0C	SA00009U20

X7673738L01 : RV20 = 4.53K , RV22 = 2K
X7673738L02 : RV20 = 6.98K , RV22 = 4.99K
X7673738L03 : RV20 = 4.53K , RV22 = 4.99K

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

ZZZ6 Micron 2G M2G@ Part Number = X7673738L01
ZZZ7 Samsung 2G S2G@ Part Number = X7673738L02
ZZZ5 HYNIX 2G H2G@ Part Number = X7673738L03

Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: R16M-M1-30(2/5)_MSIC

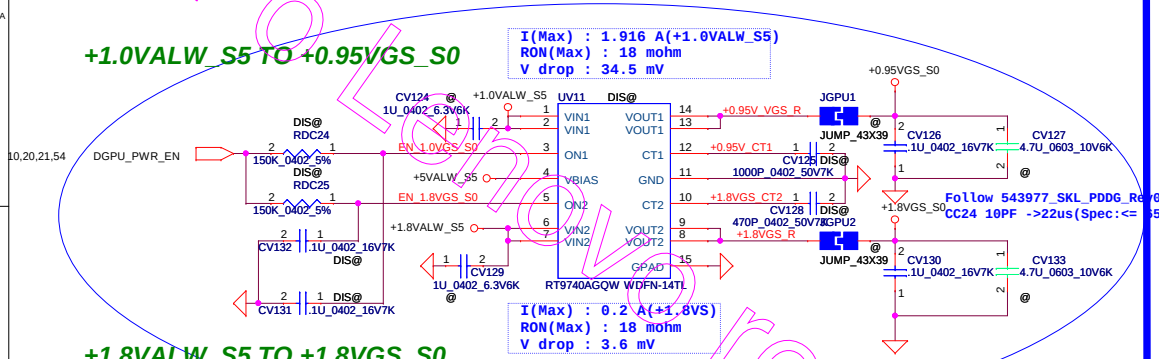
Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 20 of 60

+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch

+1.0VALW_S5 TO +0.95VGS_S0

I(Max) : 1.916 A(+1.0VALW_S5)
RON(Max) : 18 mohm
V drop : 34.5 mV



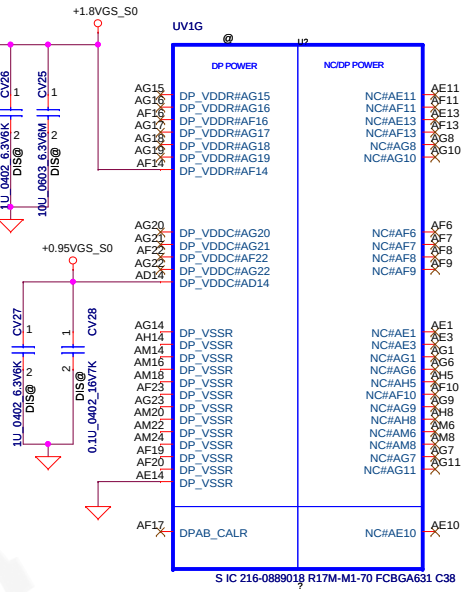
Follow 543977_SKL_PDDG_Re 0_91
CC24 10PF ->22us(Spec:<= 55us)

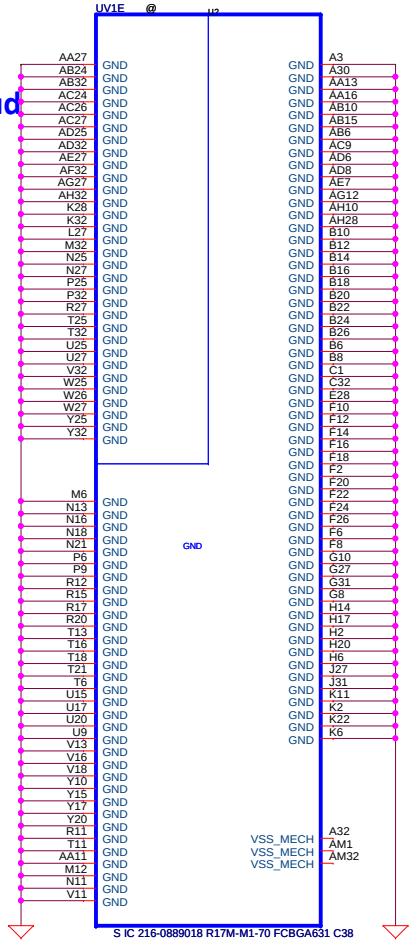
I(Max) : 0.2 A(+1.8VS)
RON(Max) : 18 mohm
V drop : 3.6 mV

+1.8VALW_S5 TO +1.8VGS_S0

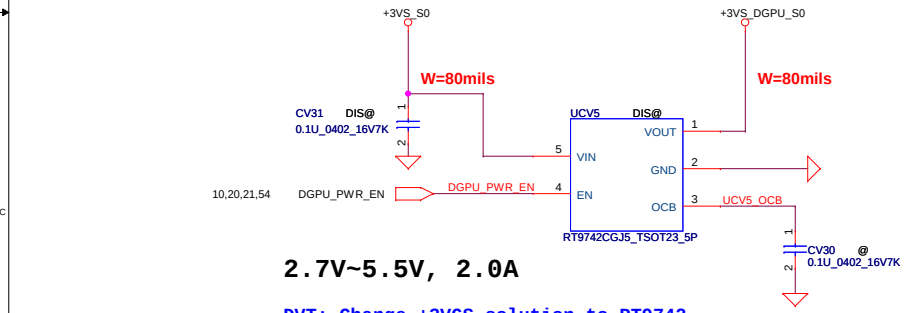
1st source : RT9740AGQW (SA00007VD00)
2nd source : TPS22966DPUR (SA00004MM00)

No Use GPU Display Port outpud



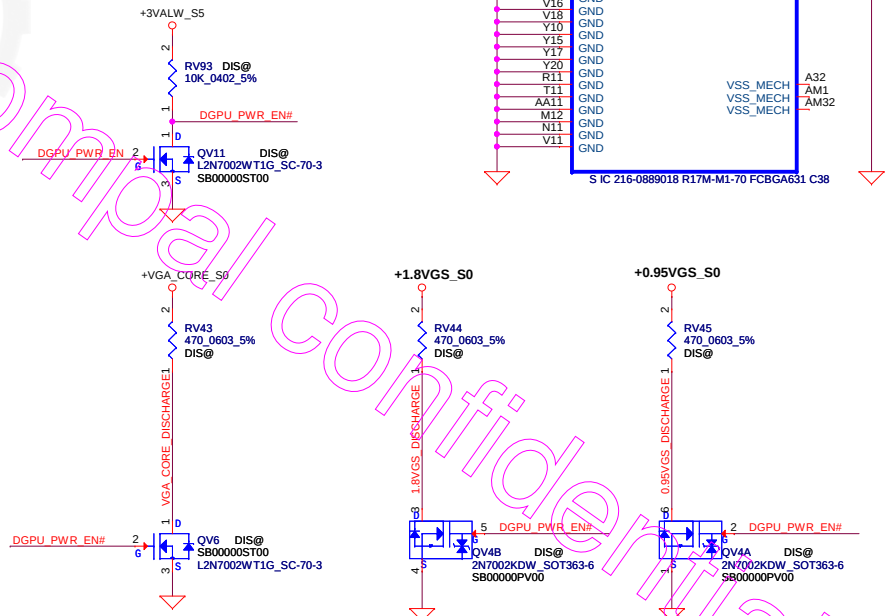


+3VALW to +3VGS

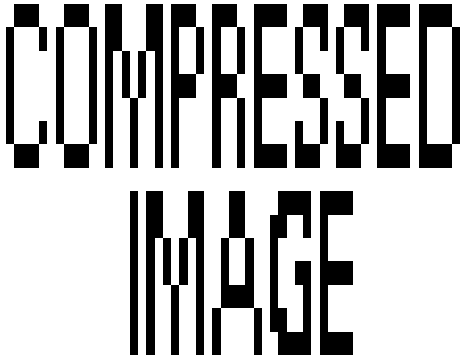


2.7V~5.5V, 2.0A

DVT: Change +3VGS solution to RT9742



DGPU Power Sequence



1. ODM uses different design for (0.95V/3.3V);
Please ensure that the design can be provided enough power and complies with AMD requirements posted on ORC.

Please ensure that all GPU power sequence are meet with AMD requirement :"R17M-M1-70/R17M-M2-50" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs

It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µs before VDDC, VDDCI, and VMEMIO start to ramp up.

Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.			
Title	R16M-M1-30 (3/5) PWR/GND		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 21 of 60		

+1.35VS_VGA_S0

12/20 UPDATE

10U_0603_6.3V6M DIS@ CV37
10U_0603_6.3V6M DIS@ CV33
10U_0603_6.3V6M DIS@ CV39
2.2U_0402_16V6K DIS@ CV41
2.2U_0402_16V6K DIS@ CV42
2.2U_0402_16V6K DIS@ CV43
2.2U_0402_16V6K DIS@ CV44
2.2U_0402_16V6K DIS@ CV45

UV1D @ U2

MEM I/O
H13 VMEMIO
H16 VMEMIO
H19 VMEMIO
J10 VMEMIO
J23 VMEMIO
J24 VMEMIO
J9 VMEMIO
K10 VMEMIO
K23 VMEMIO
K24 VMEMIO
K9 VMEMIO
L11 VMEMIO
L12 VMEMIO
L13 VMEMIO
L20 VMEMIO
L21 VMEMIO
L22 VMEMIO

LEVEL TRANSLATION
AA20 VDD_GPIO18
AA21 VDD_GPIO18
AB20 VDD_GPIO18
AB21 VDD_GPIO18

I/O
AA17 VDDR_GPIO3
AA18 VDDR_GPIO3
AB17 VDDR_GPIO3
AB18 VDDR_GPIO3

V12 VDDR4
Y12 VDDR4
U12 VDDR4

PLL
L8 MPLL_PVDD
H7 SPLL_PVDD
H8 SPLL_VDDC
J7 SPLL_PVSS

PCIE
AM30 PCIE_PVDD
AB23 NC#AB23
AC23 NC#AC23
AD24 NC#AD24
AE24 NC#AE24
AE25 NC#AE25
AE26 NC#AE26
AF25 NC#AF25
AG26 NC#AG26

L23 PCIE_VDDC
L24 PCIE_VDDC
L25 PCIE_VDDC
L26 PCIE_VDDC
M22 PCIE_VDDC
N22 PCIE_VDDC
N23 PCIE_VDDC
N24 PCIE_VDDC
R22 PCIE_VDDC
T22 PCIE_VDDC
U22 PCIE_VDDC
V22 PCIE_VDDC

CORE
AA15 VDDC
N15 VDDC
N17 VDDC
R13 VDDC
R16 VDDC
R18 VDDC
Y21 VDDC
T12 VDDC
T15 VDDC
T17 VDDC
T20 VDDC
U13 VDDC
U16 VDDC
U18 VDDC
V21 VDDC
V15 VDDC
V17 VDDC
V20 VDDC
Y13 VDDC
Y16 VDDC
Y18 VDDC
AA12 VDDC
M11 VDDC
N12 VDDC
U11 VDDC

POWER

R21 BIF_VDDC
U21 BIF_VDDC

ISOLATED CORE I/O
M13 VDDCI
M15 VDDCI
M16 VDDCI
M17 VDDCI
M18 VDDCI
M20 VDDCI
M21 VDDCI
N20 VDDCI

S IC 216-0889018 R17M-M1-70 FCBGA631 C38

+1.8VGS_S0
10U_0603_6.3V6M DIS@ CV36
1U_0402_6.3V6K DIS@ CV32

+0.95VGS_S0
10U_0603_6.3V6M DIS@ CV50
1U_0402_6.3V6K DIS@ CV51
1U_0402_6.3V6K DIS@ CV52
1U_0402_6.3V6K DIS@ CV53
1U_0402_6.3V6K DIS@ CV54
1U_0402_6.3V6K @ CV55

+VGA_CORE_S0

VGA_CORE Caps in power side sheet

+1.8VGS_S0
1U_0402_6.3V6K DIS@ CV56
+3VS_DGPU_S0
1U_0402_6.3V6K DIS@ CV57
1U_0402_6.3V6K DIS@ CV61

+1.8VGS_S0
LV2 0_0603_5%
10U_0603_6.3V6M DIS@ CV58
1U_0402_6.3V6K DIS@ CV59
0.1U_0402_16V4Z DIS@ CV117
+MPLL_PVDD

+1.8VGS_S0
LV3 0_0402_5%
10U_0603_6.3V6M DIS@ CV62
1U_0402_6.3V6K DIS@ CV63
0.1U_0402_16V4Z DIS@ CV116
+SPLL_PVDD

+0.95VGS_S0
LV4 0_0402_5%
10U_0603_6.3V6M DIS@ CV115
1U_0402_6.3V6K DIS@ CV64
0.1U_0402_16V4Z DIS@ CV65
+SPLL_VDDC

+VGA_CORE_S0

VGA_CORE Caps in power side sheet

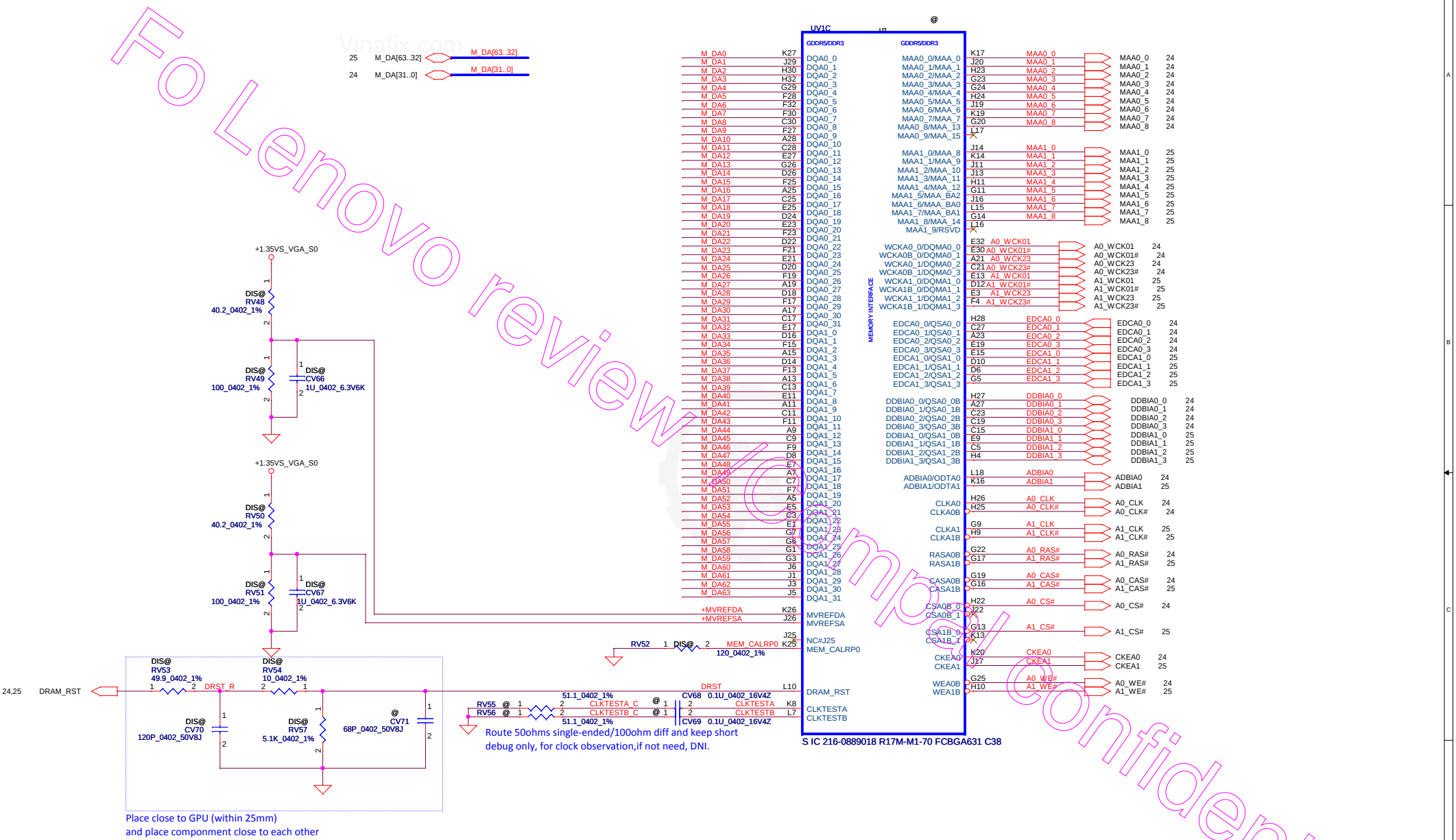
Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

Title: R16M-M1-30(4/5) PWR

Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 22 of 60

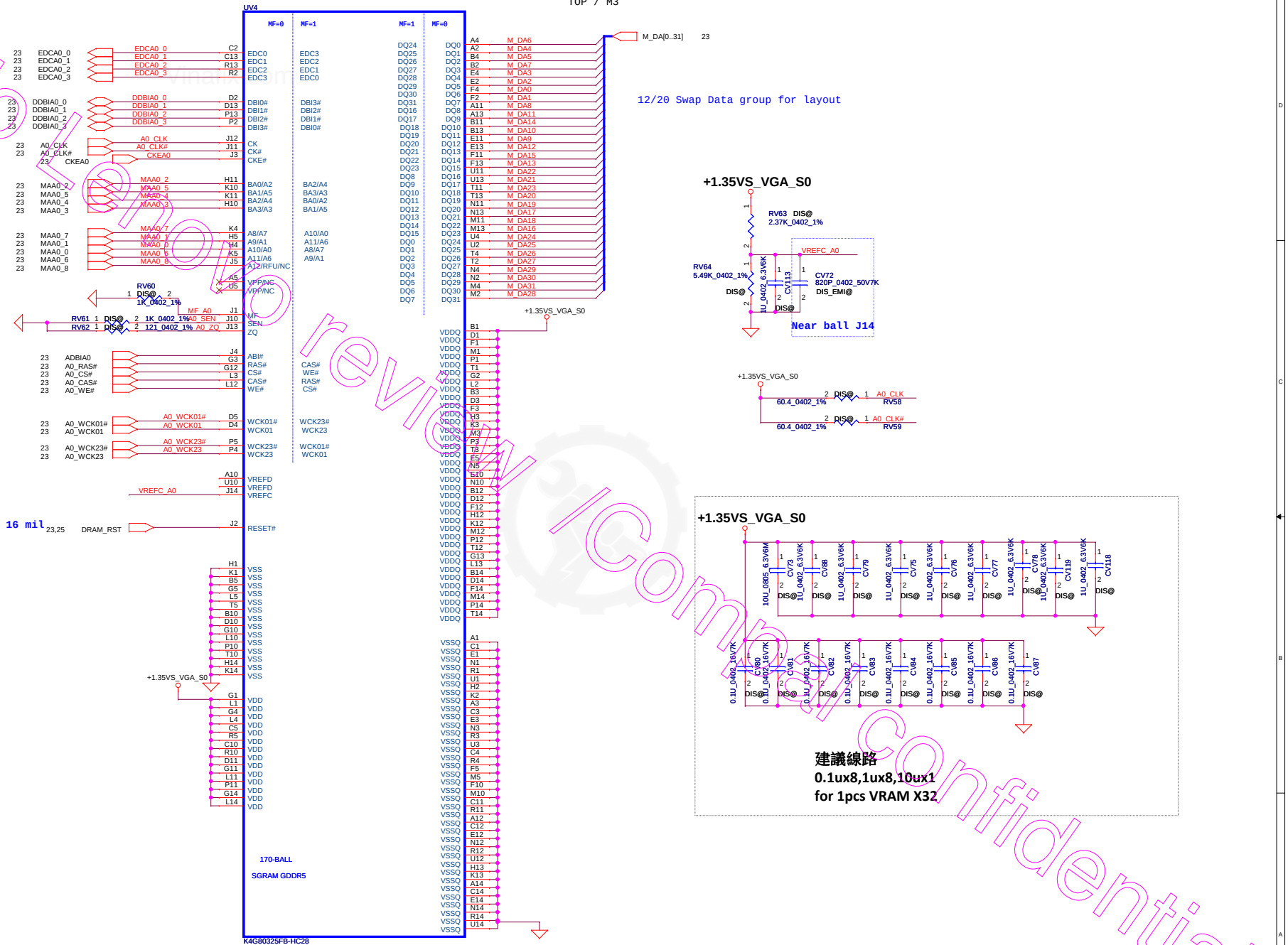


Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.			
Title	R16M-M1-30(5/5) MEM		
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 23 of 60		

Memory Partition A Lower -32 bits

TOP / M3



Security Classification	Compal Secret Data		
Issued Date	2013/03/01	Deciphered Date	2014/03/01

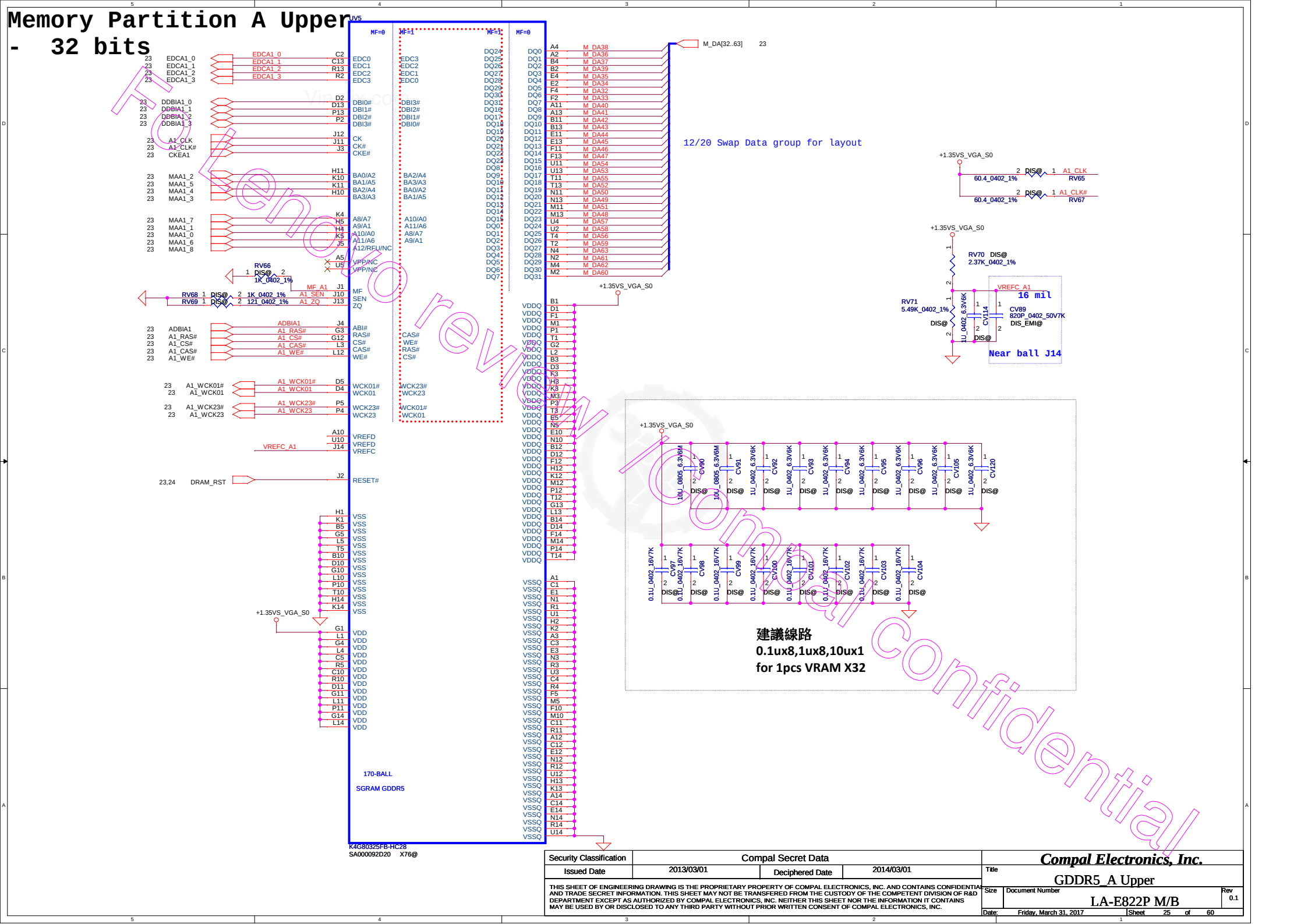
Compal Electronics, Inc.

Title: GDDR5 VRAM A Lower

Size	Document Number	Rev
	LA-E822P M/B	0.1

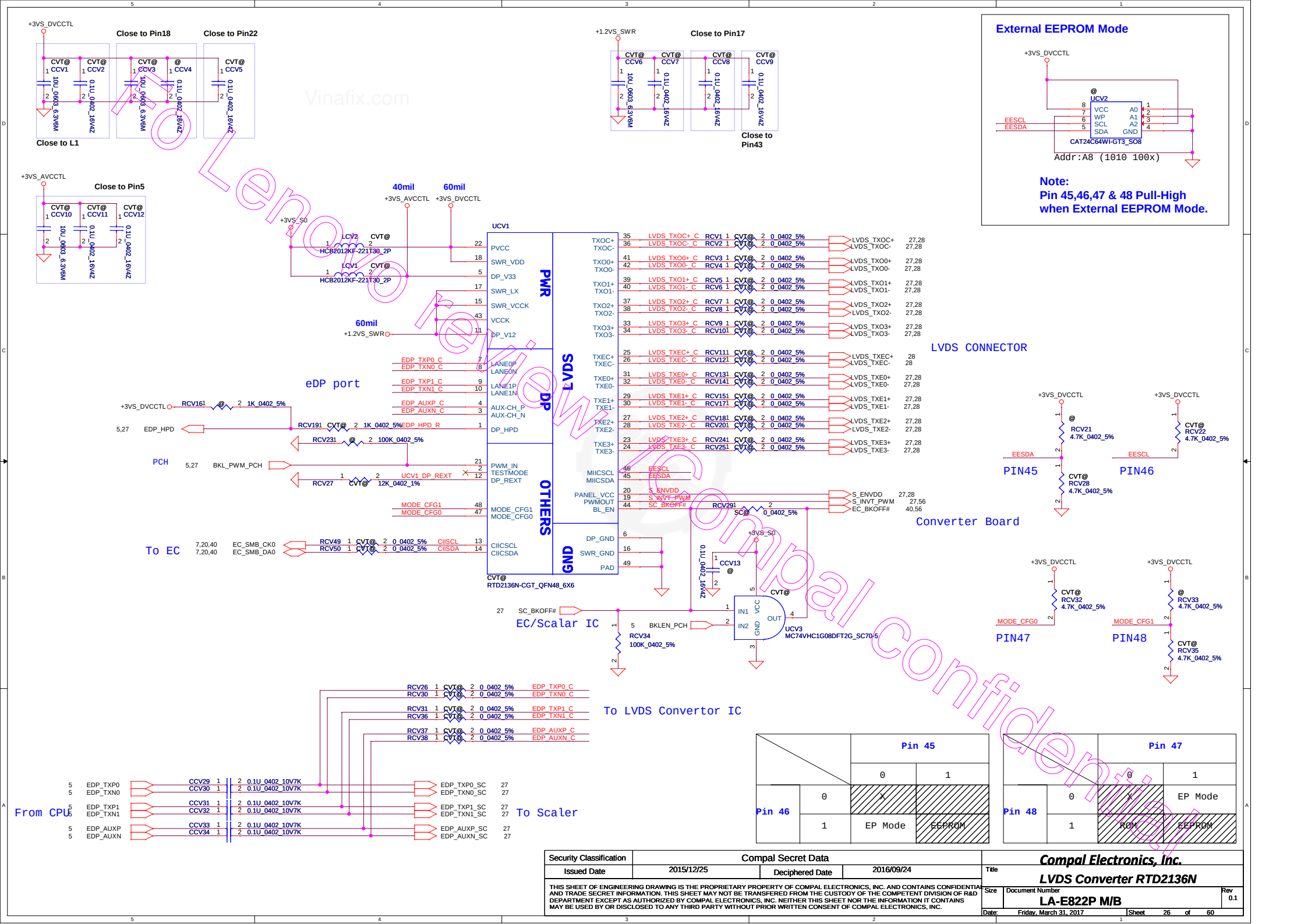
Date: Friday, March 31, 2017 Sheet 24 of 60

Memory Partition A Upper - 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/03/01	Deciphered Date	2014/03/01

Compal Electronics, Inc.			
Title	GDDR5_A Upper		
Size	Document Number		Rev
	LA-E822P M/B		0.1
Date: Friday, March 31, 2017	Sheet 25 of 60		



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title	Compal Electronics, Inc. LVDS Converter RTD2136N
Size	Document Number: LA-E822P M/B
Rev	0.1
Date:	Friday, March 31, 2017
Sheet	26 of 60

+3VALW TO +1.1VALW

340mA

2nd source
*0.340+3.3*57/1000000=0.748+0.0001881=0.74819
θ JA= 50 °C/W
PD*θ JA =0.74819*50= 37.4 °C

main source : RT9059GSP
second srouce: APL5933CKAI

Vout =0.8*[1+(39.2/100)]= 1.11V

IQ(typ)=47uA,IQ(max)=57uA
PD = (Vin-Vout)*Iout + Vin*IQ
=(3.3-1.1)*0.340+3.3*57/1000000
=0.748+0.0001881=0.74819
θ JA= 33.7 °C/W
PD*θ JA =0.74819*33.7= 25.2 °C

+3VSCA_DSW

W=80mils

W=80mils

VIN: 2.7V~5.5V / 2.0A

DVT: change +3V_SCA_DSW solution to RT9742

Remove RSC4 have check vendor no need 12/19

SPI 4M

Change FF to 45.1

FOR Scalar Firmware Code

158mA

0.67mA

eDP

HDMI IN

HDMI-Port0

HDMI-Port1

LVDS

USC4 EEPROM 16M circuit remove have check vendor 12/19

close to USC1 (Scaler)

intel	PROJECT_ID1 AMD: H Intel : L	PROJECT_ID2	PROJECT_ID3
C4	L	L	H
C5	L	H	H

DVT: Remove RSC48 and Change CSC23 to 0.1u

Pull high remove have check vendor 12/19

	SC_MODE1	SC_MODE2
PC mode	L	L
Monitor mode	L	H
AMP Mute	H	L
S5 Mode	H	H

SMBus

RTD2506S-CG-LQFP128_14X14

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: **Scalar RTD2506S**

Size: Custom | Document Number: **LA-E822P M/B** | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 27 of 60

Willy 2016.11.10 Change FCA1 for 0.75A

0.75A PTC

+3VS_S0

80 mils

+3VS_CAM_S0

FCA1

0.75A_6V_0805L075ULYR

CCA1
10U_0603_6.3V6M

LCA1 EMI@

11 USB20_N4

11 USB20_P4

USB20_N4_R

USB20_P4_R

MCM1012B900F06BP_4P
SM070003Z00

Place close to JCAM1

DCA1

PESD5V0U2BT_SOT23-3
SCA00000T00

ESD@

Willy 2016.11.10 Add IR CAM for 5V

+5VS_CAM_S0

FCA2
2A_8V_1812L200THPR

100 mils

40 mils

+5VS_CAM_S0_C

USB20_N4_R

USB20_P4_R

JCAM1

ACES_87213-0800G
SP02000CZ00
CONN@

CAMERA

+5VALW_S5

IRCAM@
CCA2
1U_0402_6.3V6K

12,40,43 SUSP#

UCA1 IRCAM@

TPS22965DSGR_SON8_2X2~D

IRCAM@
CCA3
1U_0402_6.3V6K

UCAM_CT

IRCAM@
CCA4
2200P_0402_50V7K

IRCAM@
CCA5
0.1U_0402_10V6K

IRCAM@
CCA6
10U_0603_6.3V6M

+5VS_CAM_S0

RSC62/RSC63 near JLVDS1 pin19 and 21

LVDS_TXOC- SC@ RSC62 LVDS_TXEC-
LVDS_TXOC+ SC@ RSC63 LVDS_TXEC+
0_0402_5%

+LCD5V_S5

JLVDS1

CCV20
680P_0402_50V7K

+5VS_TOUCH_S0

CTO1
0.1U_0402_16V7K

USB20_N10_R

USB20_P10_R

+3VS_MIC_S0

INT_DMIC_DSP_DA2

INT_DMIC_DSP_CK2

INT_DMIC_DSP_DA1

INT_DMIC_DSP_CK1

SP02000TL00
CONN@

ACES_50238-05071-001

11/28 LVDS conn rotate 90 change pin define

Touch

RTO1 RTO2 0_0402_5%

EMI@

@EMI@ LTO1

MCM1012B900F06BP_4P
SM070003Z00

USB20_N10

USB20_P10

Place close to JLVDS1

+5VS_S0

0.75A PTC

FTO1

0.75A_6V_0805L075ULYR

CTO2
0.1U_0402_16V4Z

DTO1

PESD5V0U2BT_SOT23-3
SCA00000T00

@ESD@

+LCDVDD Current Rating: Max=1500mA

+5VALW_S5

+LCD5V_F_S5

+LCD5V_S5

1.5A_PTC

80mil

UCV4

RT9742CGJ5_TSOT23_5P
SA00009SV00
2A_Active High

FCV1
1.5A_8V_1206L150THWR

CCV23
1U_0402_6.3V6K

CCV24
4.7U_0603_10V6K

CCV25
0.1U_0402_16V4Z

CCV26
0.1U_0402_16V7K

UCV1_FLG

Main: SA00009SV00 RT9742CGJ5 TSOT23 5P
Second: SA00009RN00 UP7549UMA5-20 SOT23 5P

S_ENVDD 26,27

RCV48
100K_0402_5%

CCV28
0.1U_0402_16V4Z

Follow name rule change net name

MIC

0.75A PTC

+3VS_S0

FMIC1

0.75A_6V_0805L075ULYR

40 mils

+3VS_MIC_S0

CMIC2
10U_0603_6.3V6M

DMIC1 ESD@
PESD5V0U2BT_SOT23-3
SCA00000T00

INT_DMIC_DSP_CK1

INT_DMIC_DSP_DA1

RMIC1
10_0402_5%

INT_DMIC_DSP_CK1_EMI

EMI@ CMIC3
10P_0402_50V8J

EMI@ CMIC1
10P_0402_50V8J

Place close to JLVDS1

DMIC2 ESD@
PESD5V0U2BT_SOT23-3
SCA00000T00

INT_DMIC_DSP_CK2

INT_DMIC_DSP_DA2

RMIC2
10_0402_5%

INT_DMIC_DSP_CK2_EMI

EMI@ CMIC5
10P_0402_50V8J

EMI@ CMIC6
10P_0402_50V8J

Follow Dual MIC add

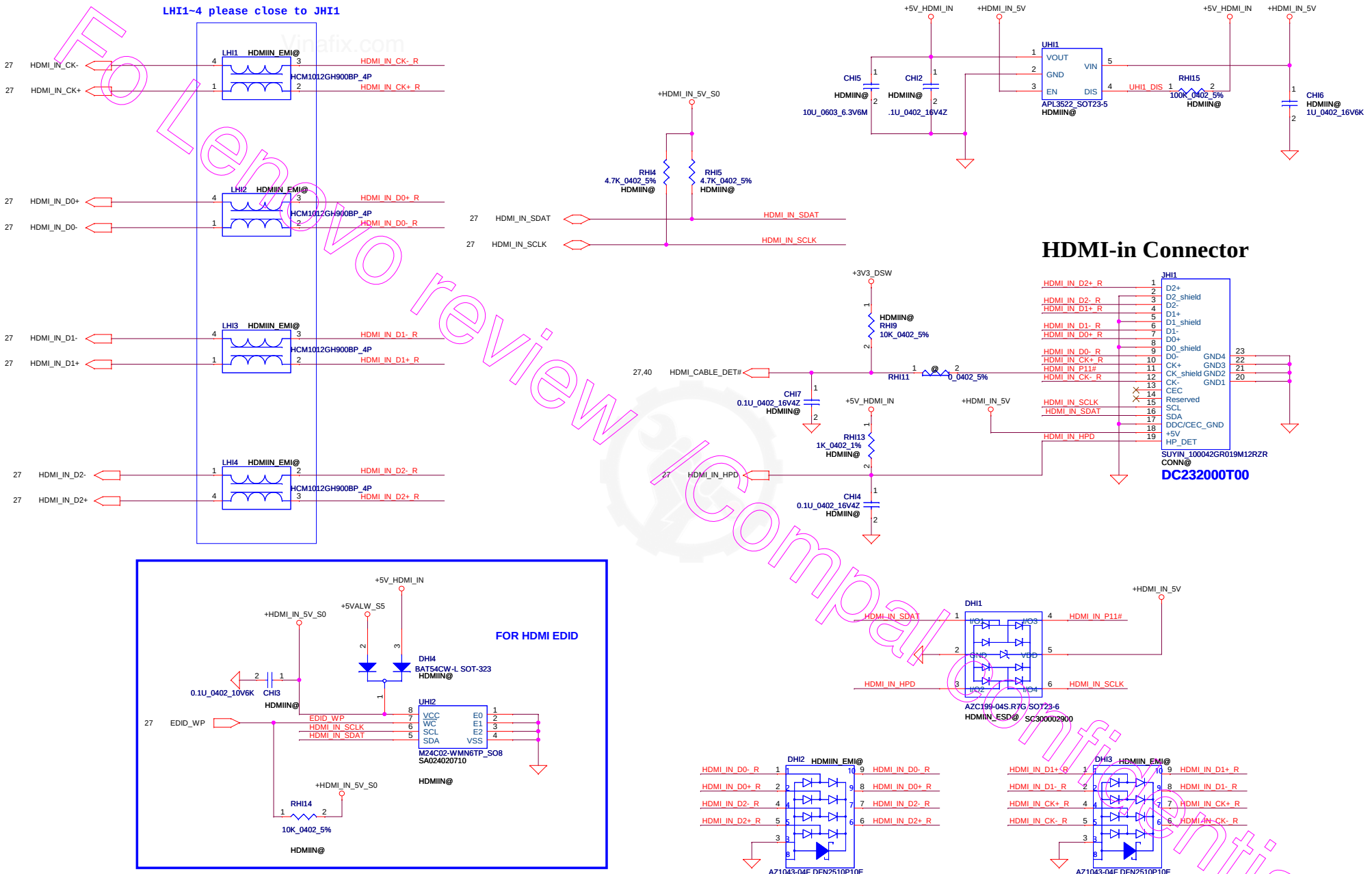
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: LVDS/Convertor/CAM/Touch

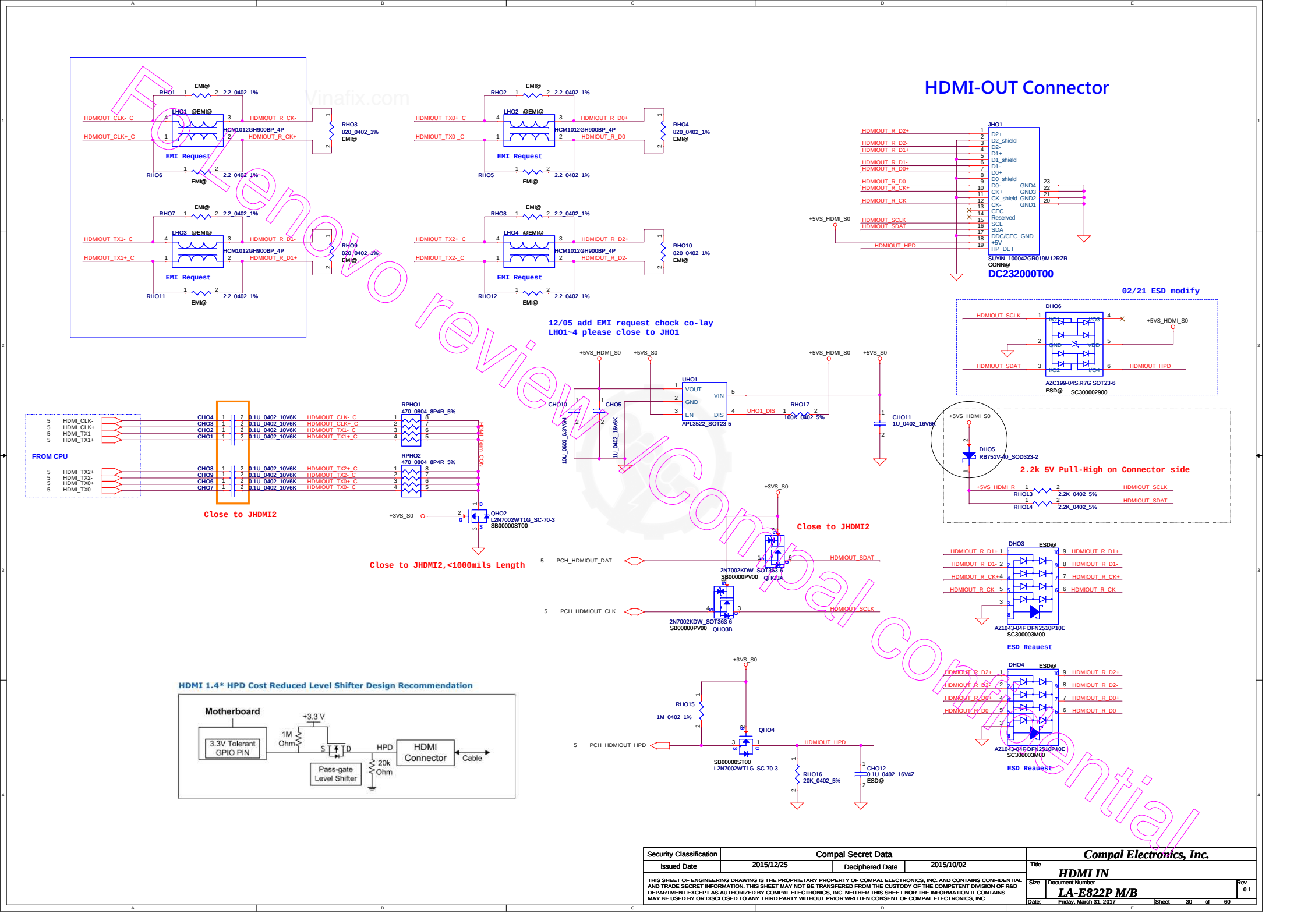
Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 28 of 60



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title: HDMI-IN conn			
Size: Custom	Document Number: LA-E822P M/B		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 29 of 60		



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/10/02

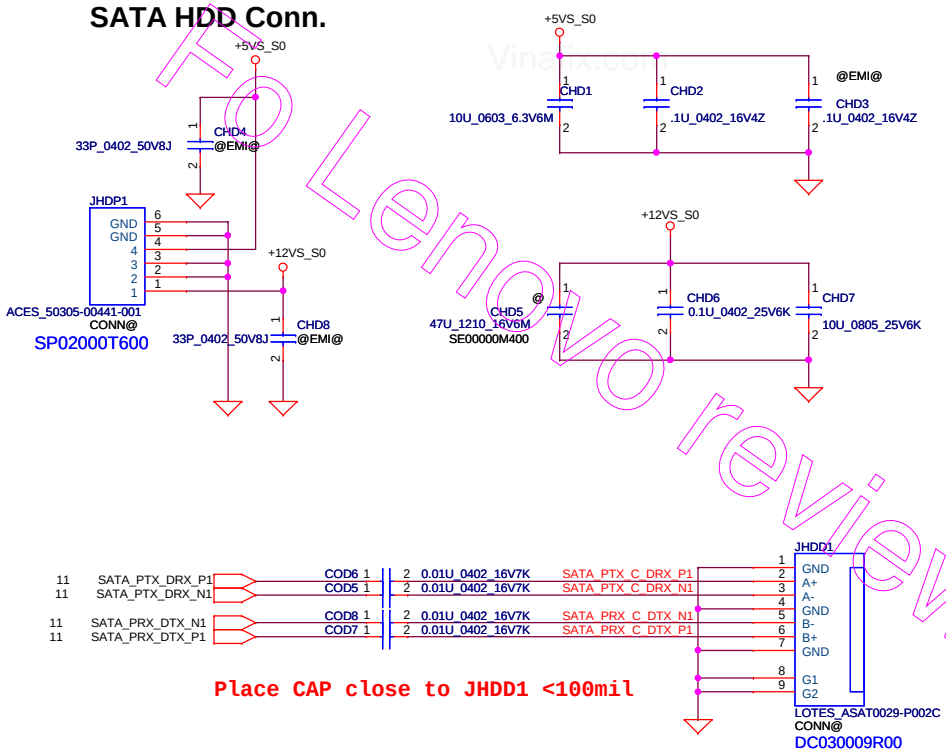
Compal Electronics, Inc.

Title: **HDMI IN**

Size | Document Number: **LA-E822P M/B** | Rev: 0.1

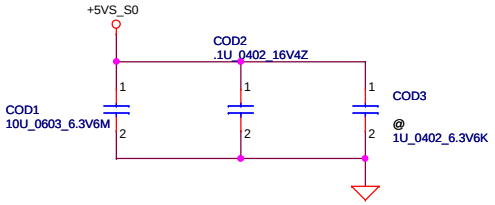
Date: Friday, March 31, 2017 | Sheet 30 of 60

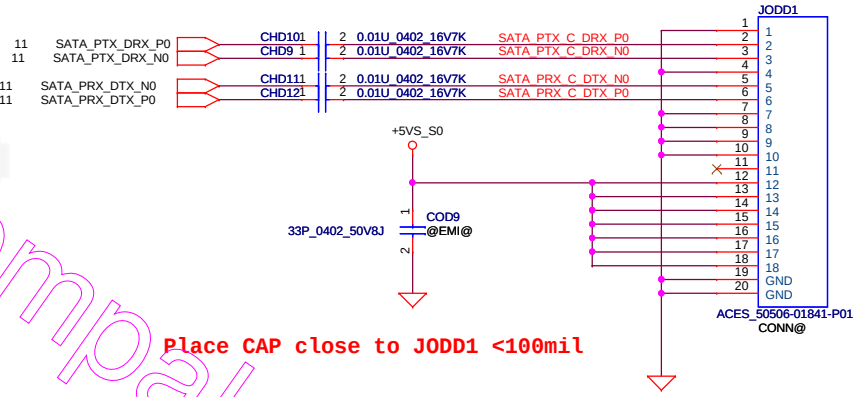
SATA HDD Conn.



Place CAP close to JHDD1 <100mil

SATA ODD Conn





Place CAP close to JODD1 <100mil

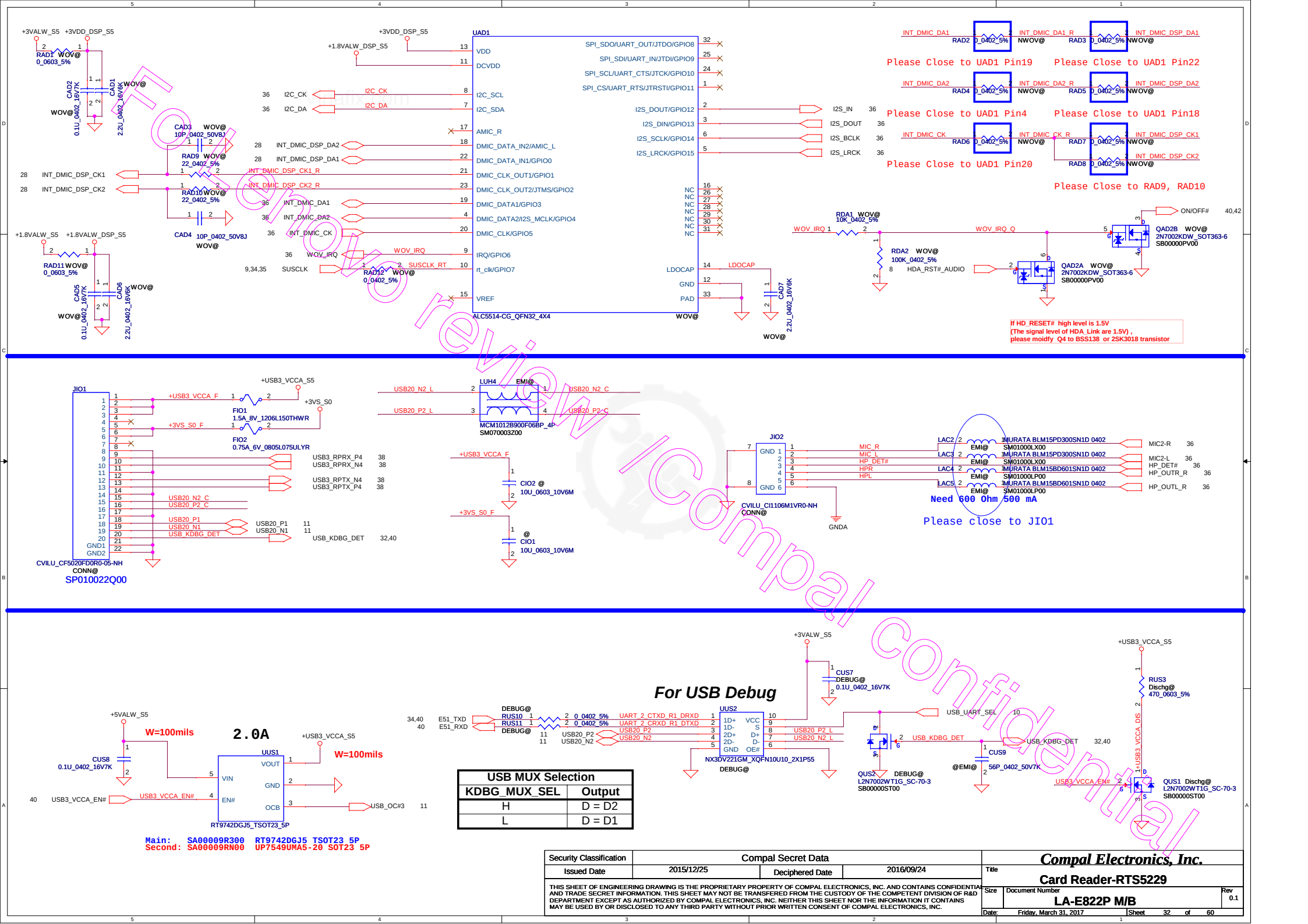
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***HDD/ODD***

Size	Document Number	Rev
Custom	LA-E822P M/B	0.1

Date: Friday, March 31, 2017 | Sheet 31 of 60



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

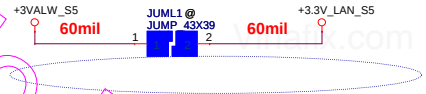
Compal Electronics, Inc.

Title: **Card Reader-RTS5229**

Size	Document Number	Rev
	LA-E822P M/B	0.1

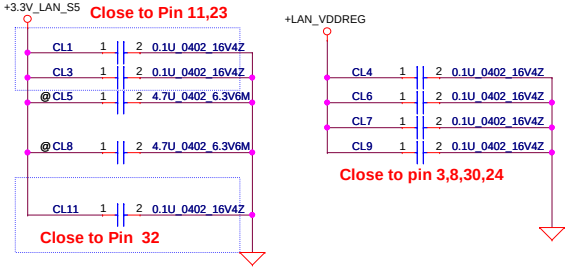
Date: Friday, March 31, 2017 | Sheet 32 of 60

WOL circuit (Connect +3V_LAN to +3VALW)



+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

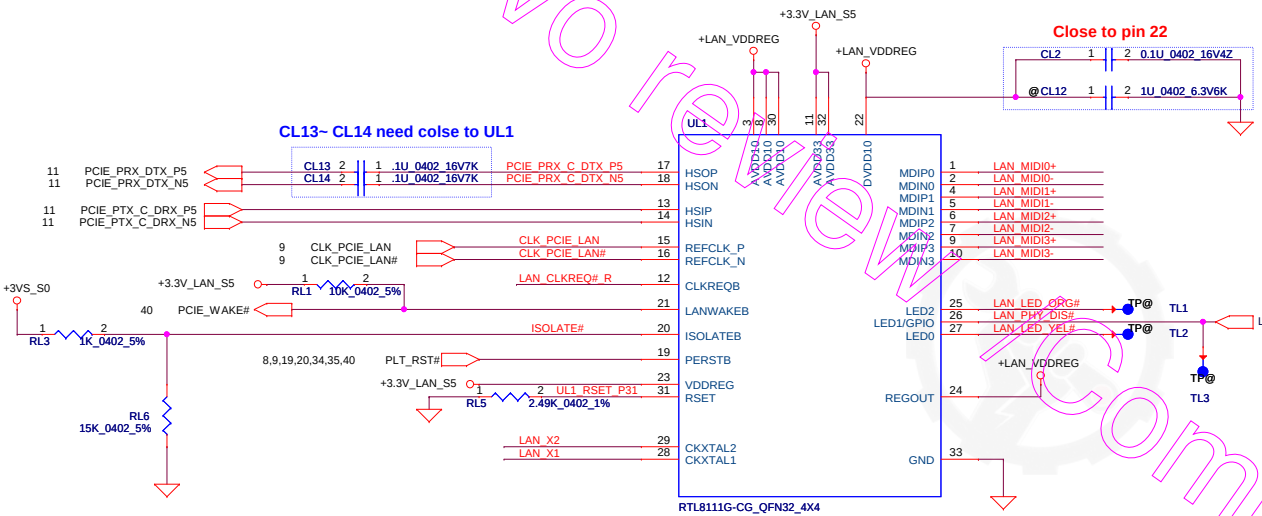


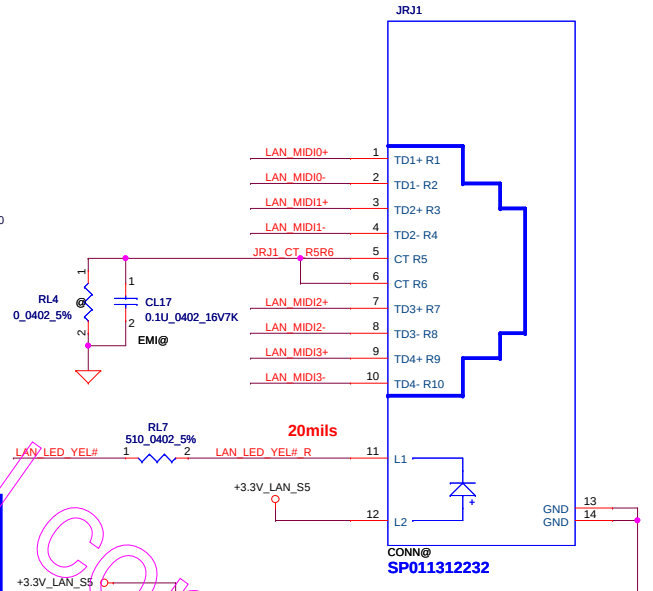
LED Status

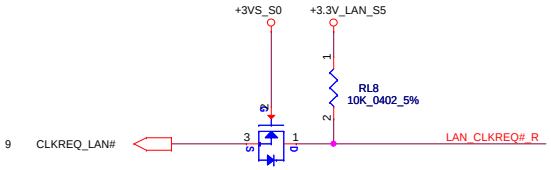
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

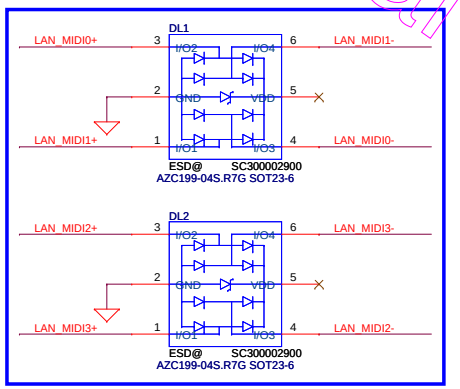
always on

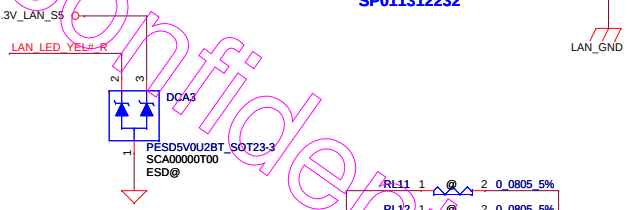
blinking

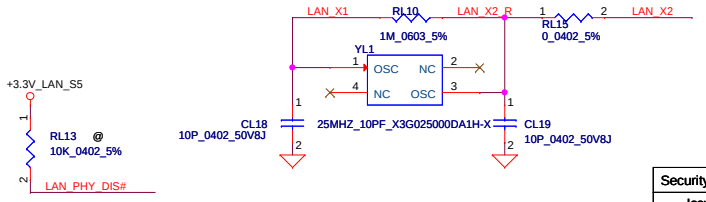












Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/12/15

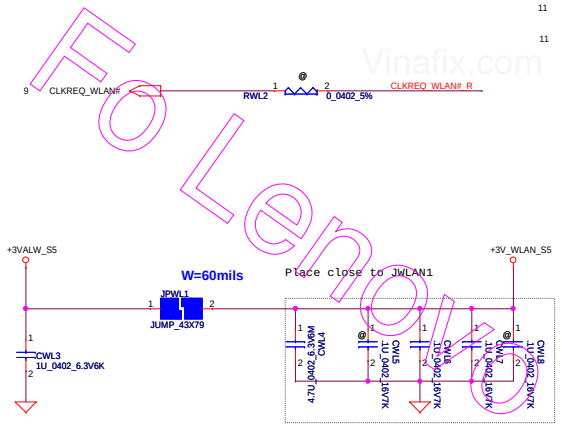
Compal Electronics, Inc.

Title: **LAN RTL8111G/H**

Size: Custom | Document Number: **LA-E822P M/B** | Rev: 0.1

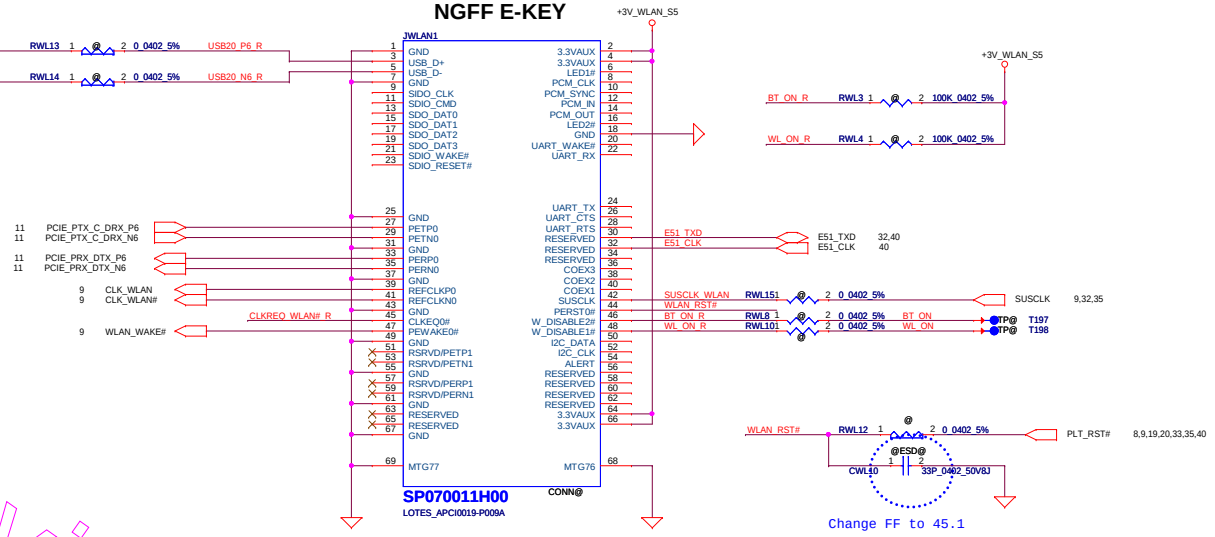
Date: Friday, March 31, 2017 | Sheet 33 of 60

WLAN (WIFI/BT Combo)



WLAN Conn.

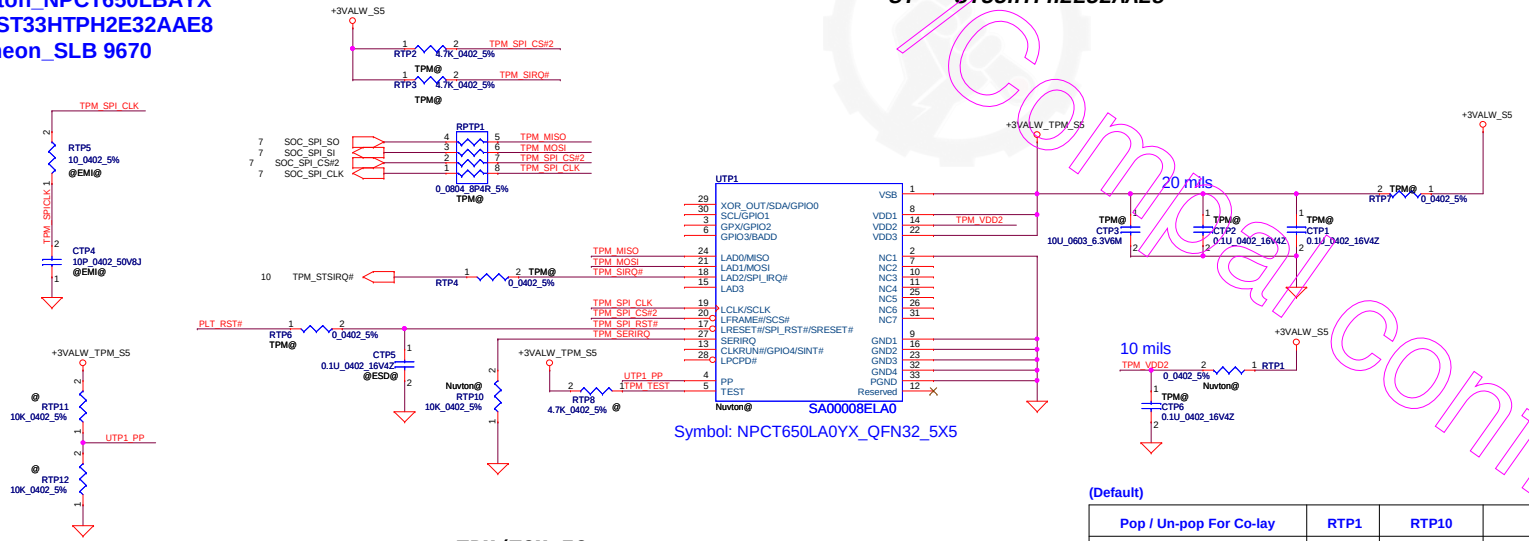
NGFF E-KEY



TPM 2.0 Co-lay

1.Nuvton_NPCT650LBAYX
2.ST_ST33HTPH2E32AAE8
3.Infineon_SLB 9670

NEW PART: Nuvoton NPCT650LBAYX (Default)
Infineon SLB 9670
ST ST33HTPH2E32AAE8



TPM/TCM IC

UTP1 ST@ — ST_ST33HTPH2E32AAE8(SPI) — SA00009SO10

UTP1 Infineon@ — Infineon_SLB 9670(SPI) — SA00009N230

(Default)

Pop / Un-pop For Co-lay	RTP1	RTP10	BOM Config
Nuvton_NPCT650LBAYX (SPI)	V	V	Nuvton@+TPM@
ST_ST33HTPH2E32AAE8(SPI)	X	X	ST@+TPM@
Infineon_SLB 9670(SPI)	X	X	Infineon@+TPM@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date	2015/10/02

Title	WLAN (NGFF) / TPM		
Size	Document Number		Rev
	LA-E822P M/B		0.1
Date:	Friday, March 31, 2017	Sheet	34 of 60

+3VS_S0 — W=60mils — JPSSD1 (JUMP_43X79) — +3V_SSD_S0

Place close to JSSD1

CSSD1 10U_0603_6.3V6M

CSSD2@ .1U_0402_16V7K

CSSD3 .1U_0402_16V7K

NGFF KEY M (SSD)

JSSD1 — SP07001CT00 — FOX_AS0BC21-S85BM-WH — CONN@

1	GND		2	3P3VAUX	
3	GND		4	3P3VAUX	
5	PERn3		6	NC	
7	PERp3		8	NC	
9	GND		10	DAS/DSS#	
11	PETn3		12	3P3VAUX	
13	PETp3		14	3P3VAUX	
15	GND		16	3P3VAUX	
17	PERn2		18	3P3VAUX	
19	PERp2		20	NC	
21	GND		22	NC	
23	PETn2		24	NC	
25	PETp2		26	NC	
27	GND		28	NC	
29	PERn1		30	NC	
31	PERp1		32	NC	
33	GND		34	NC	
35	PETn1		36	NC	
37	PETp1		38	DEVSLP	DEVSLP 1 RSSD1 2 10K_0402_5%
39	GND		40		
41	PERn0/SATA-B+		42	NC	
43	PERp0/SATA-B-		44	NC	
45	GND		46	NC	
47	PETn0/SATA-A-		48	NC	
49	PETp0/SATA-A+		50	PERST#	PLT_RST# 8,9,19,20,33,34,40
51	GND		52	CLKREQ#	CLKREQ_SSD# 9
53	REFCLKN		54	PEWake#	M2_WAKE# 2 @ 1 M2_WAKE#_R RSSD5 0_0402_5% TP@ T196
55	REFCLKP		56	NC	
57	GND		58	NC	
67	NC		68	SUSCLK(32kHz)	SUSCLK_R 2 @ 1 SUSCLK 9,32,34 RSSD6 0_0402_5%
69	PEDET(NC-PCIE/GND-SATA)		70	3P3VAUX	
71	GND		72	3P3VAUX	
73	GND		74	3P3VAUX	
75	GND		76	GND1	
			77	GND2	

+3VS_S0

PLT_RST#

CSSD14 0.1U_0402_16V4Z @ESD@

Please close to JSSD1

11	PCIE_PRX_SSDTXN1		
11	PCIE_PRX_SSDTXP1		
11	PCIE_PTX_SSDRXN1	CSSD12 2	1 0.22U_0402_16V7K PCIE_PTX_C_SSDRXN1
11	PCIE_PTX_SSDRXP1	CSSD13 2	1 0.22U_0402_16V7K PCIE_PTX_C_SSDRXP1
11	PCIE_PRX_SSDTXN2		
11	PCIE_PRX_SSDTXP2		
11	PCIE_PTX_SSDRXN2	CSSD10 2	1 0.22U_0402_16V7K PCIE_PTX_C_SSDRXN2
11	PCIE_PTX_SSDRXP2	CSSD11 2	1 0.22U_0402_16V7K PCIE_PTX_C_SSDRXP2
11	PCIE_PRX_SSDTXN3		
11	PCIE_PRX_SSDTXP3		
11	PCIE_PTX_SSDRXN3	CSSD8 2	1 0.22U_0402_16V7K PCIE_PTX_C_SSDRXN3
11	PCIE_PTX_SSDRXP3	CSSD9 2	1 0.22U_0402_16V7K PCIE_PTX_C_SSDRXP3
11	PCIE/SATA_PRX_SSDTXP4		
11	PCIE/SATA_PRX_SSDTXN4		
11	PCIE/SATA_PTX_SSDRXN4	CSSD6 2	1 0.22U_0402_16V7K PCIE/SATA_PTX_C_SSDRXN4
11	PCIE/SATA_PTX_SSDRXP4	CSSD7 2	1 0.22U_0402_16V7K PCIE/SATA_PTX_C_SSDRXP4
9	CLK_SSD#		
9	CLK_SSD		

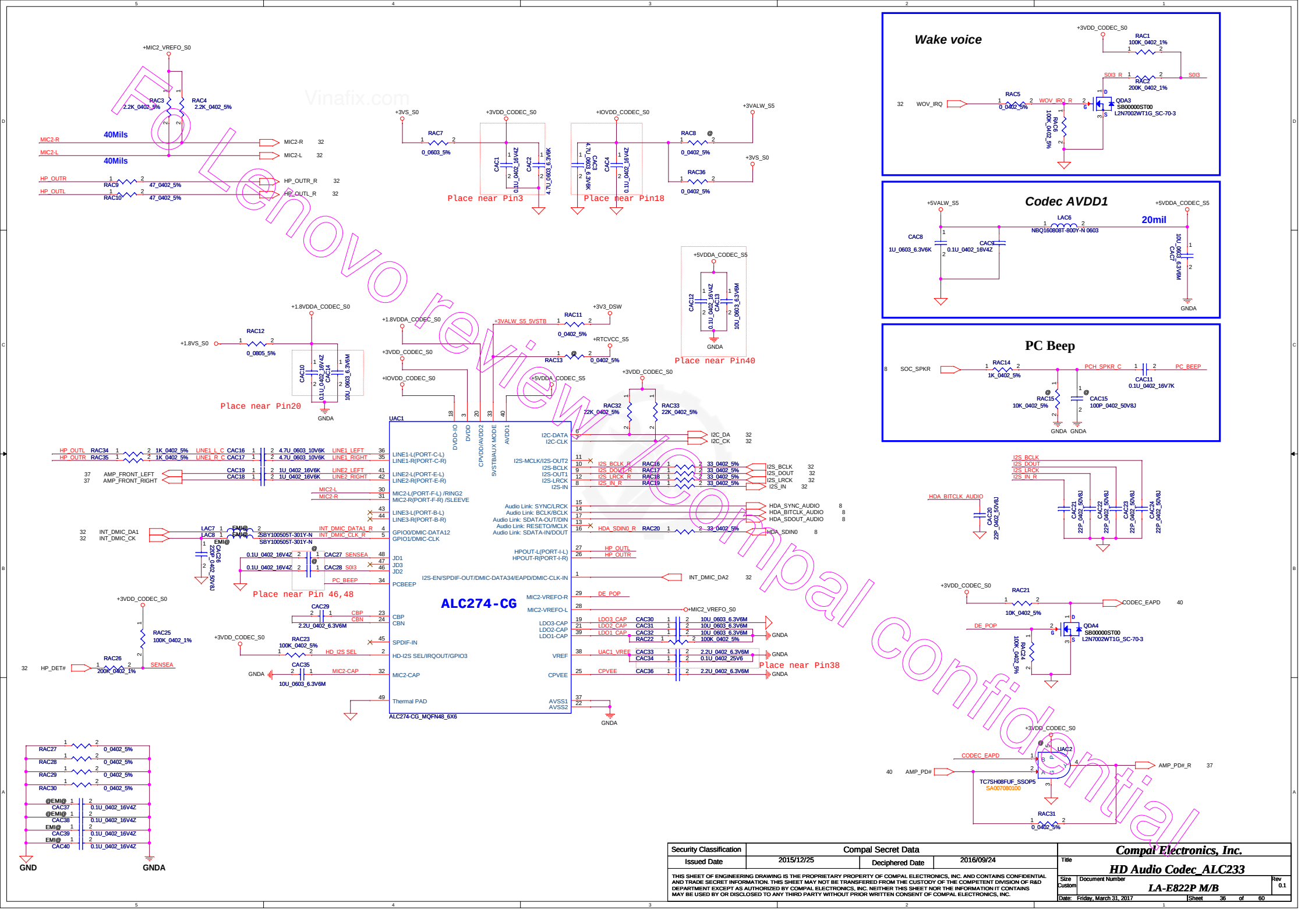
11 M2_SATA_PCIE_SEL

GPIO Control BIOS SEL PCIE/SATA

Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.			
Title	SSD (M2)		
Size B	Document Number LA-E822P M/B		Rev 0.1
Date: Friday, March 31, 2017	Sheet 35 of 60		



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

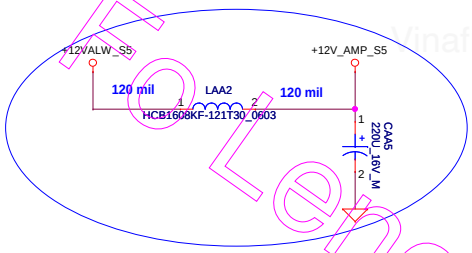
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: HD Audio Codec_ALC233

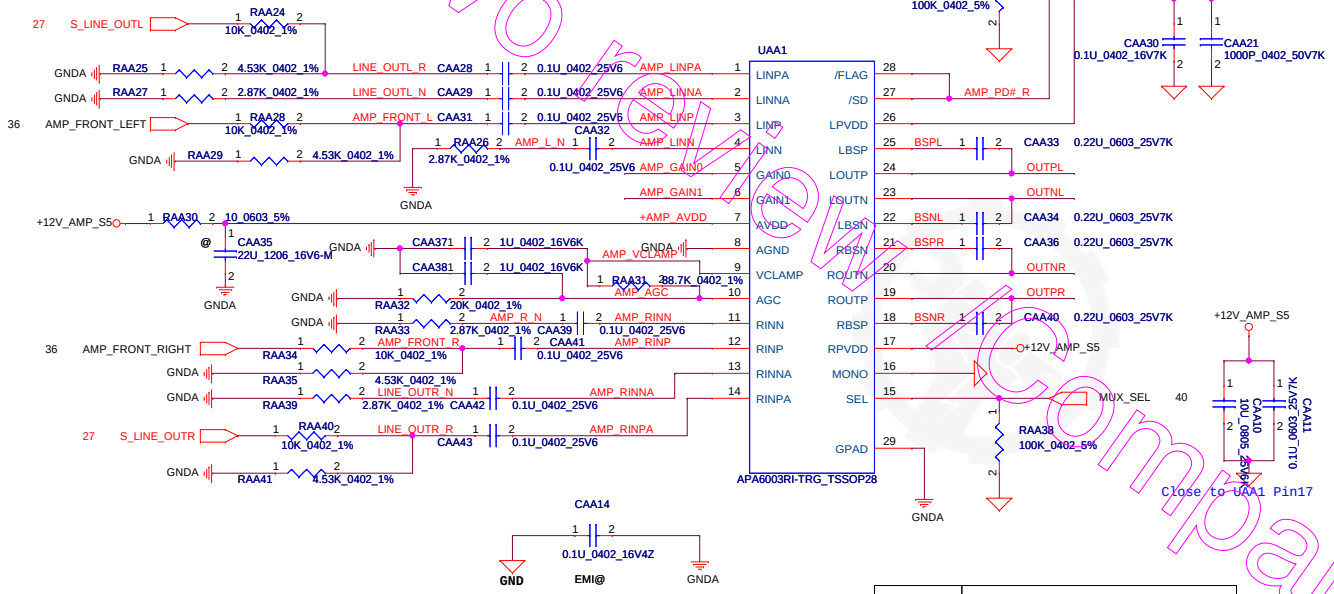
Size	Document Number	Rev
Custom	LA-E822P M/B	0.1

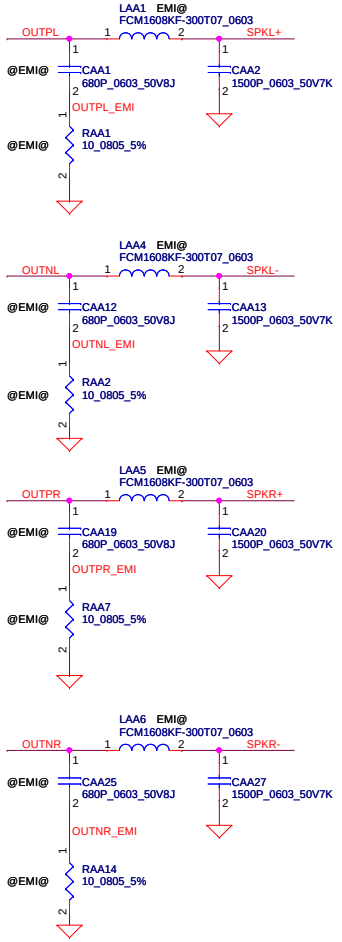
Date: Friday, March 31, 2017 Sheet 36 of 60



Remove 0.1u*2, 4.7u*1, 10u*1

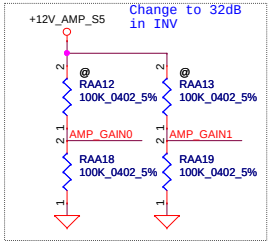
Remove RAC37, 1u*1 4.7u*1 (reserve cap)





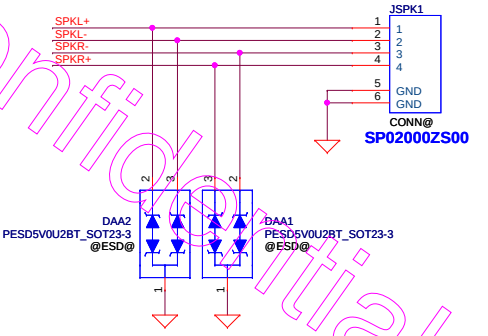
MUX_SEL	L=Audio Codec Input source H=Scalar Input source

APA6003 for Speaker (CRB)



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

Speaker Conn.
3Wx2 4ohm Speaker



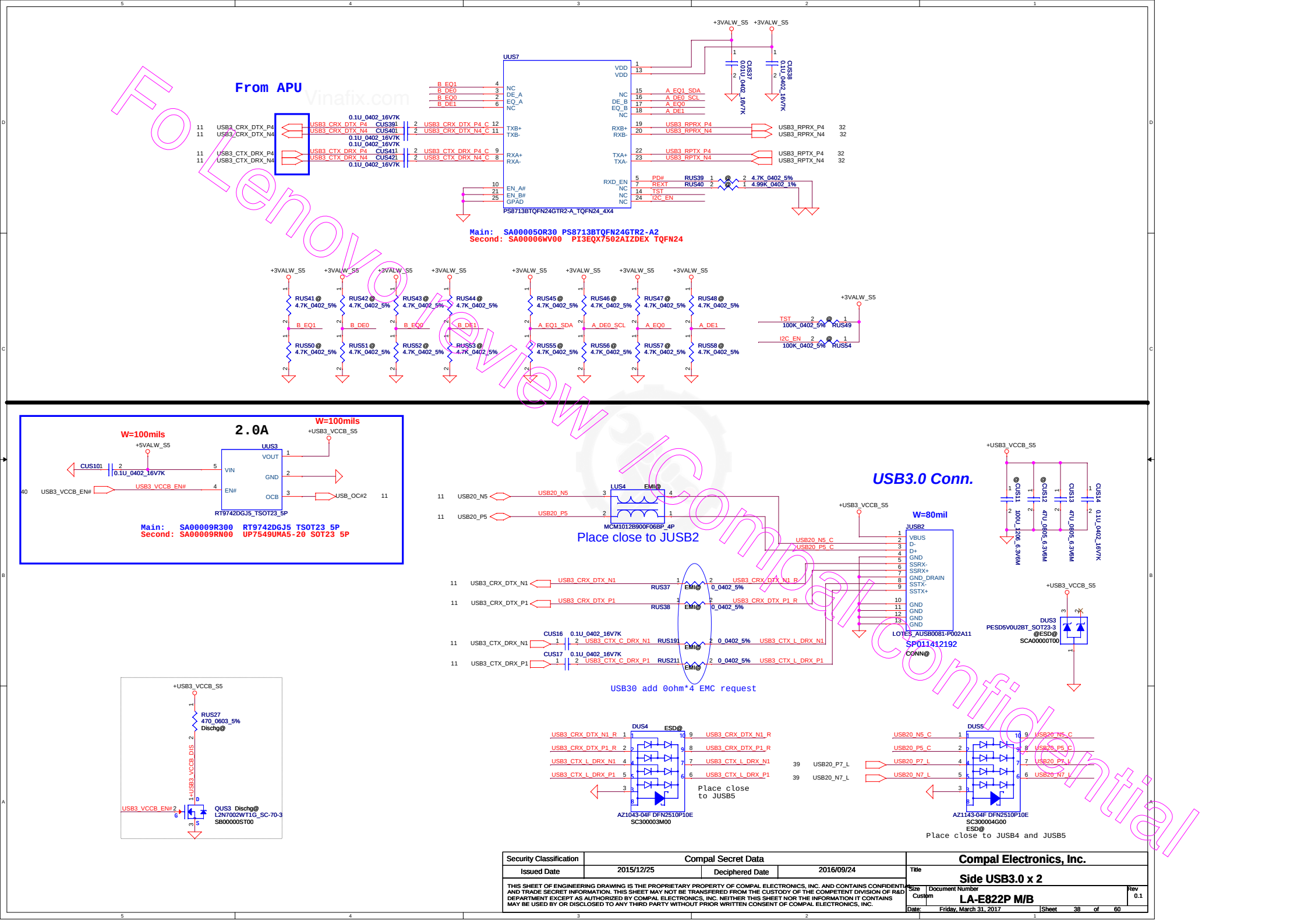
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/12/15

Compal Electronics, Inc.

Title: Amp ANPEC APA6003

Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 37 of 60



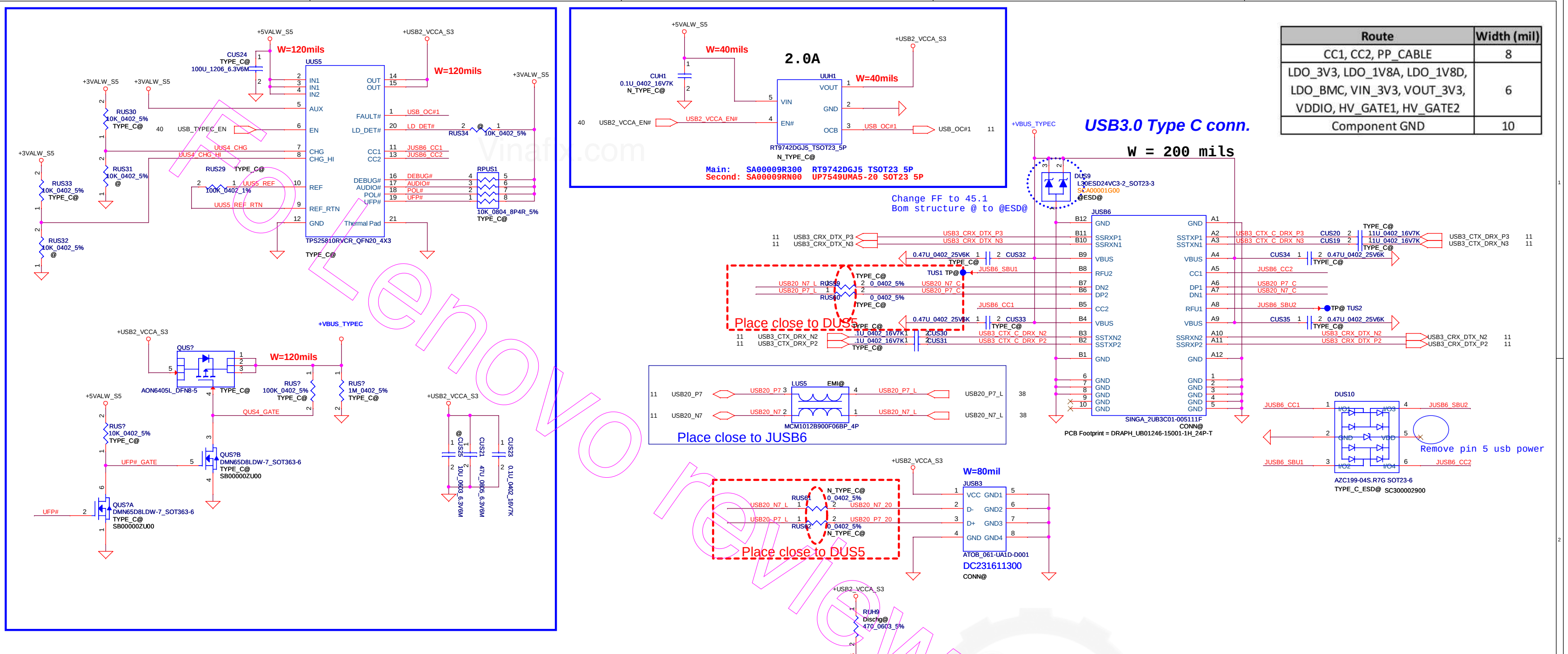
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: **Side USB3.0 x 2**

Size	Document Number	Rev
Custom	LA-E822P M/B	0.1

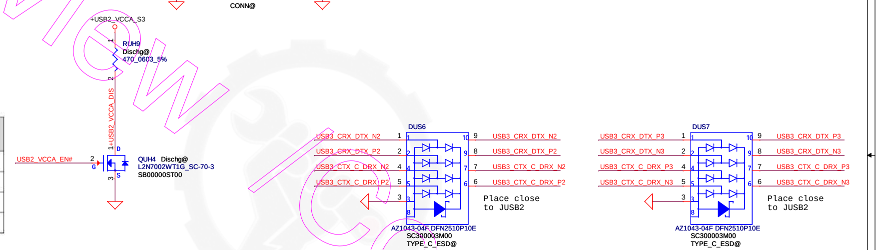
Date: Friday, March 31, 2017 Sheet 38 of 60

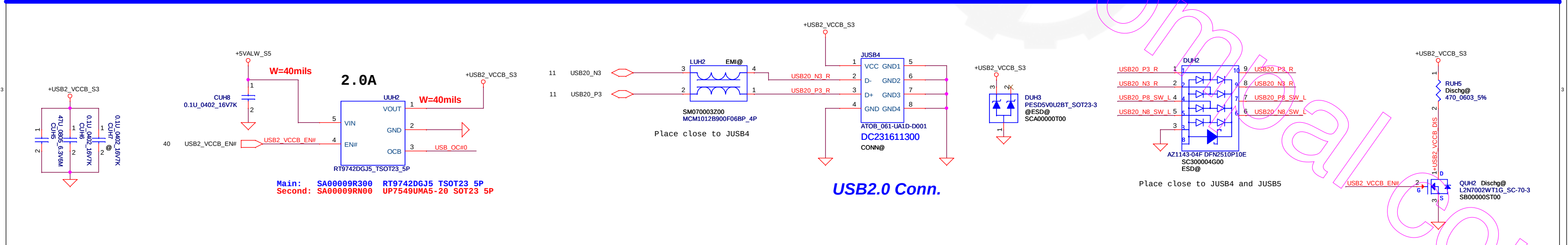


Route	Width (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

Table 3. USB Type-C Current Advertisement

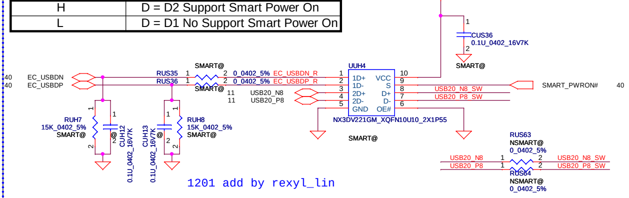
CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

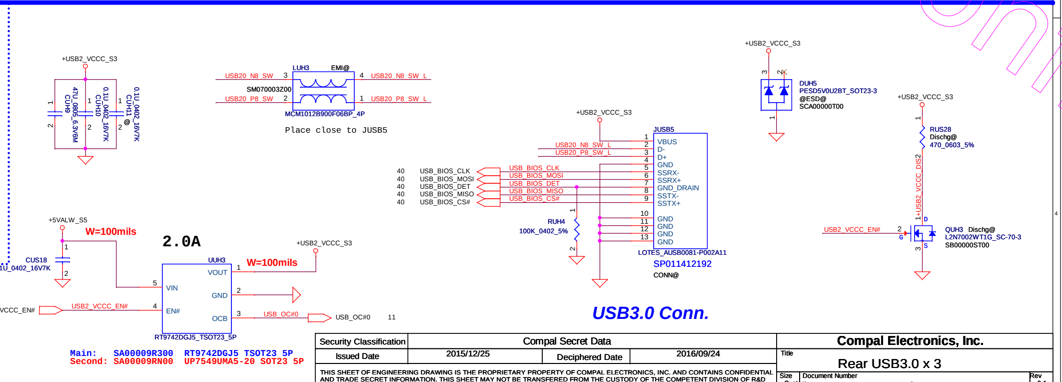




For SMART Power on

SMART_PWON	Smart power on select
H	D = D2 Support Smart Power On
L	D = D1 No Support Smart Power On





Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: Rear USB3.0 x 3

Size: Custom — Document Number: LA-E822P M/B — Rev: 0.1

Date: Friday, March 31, 2017 — Sheet 39 of 60

Place closely UEC1

V1.0 update

2Mb SPI ROM

W25X20CLSNIG_SO8
SA00003GM30

LPC Address Select:
0: 2Eh/2Fh
1: 4Eh/4Fh

EC DEBUG port
Reserve REC34 for EC debug.

AD Voltage Range:
0 to 2.048 V

Ra (100K)
Rb (Max:150k)

EVT : 30K Ohm : 0.76V
DVT : 56K Ohm : 1.18V
PVT : 100K Ohm : 1.67V
MP : 150K Ohm : 1.98V

BIOS recovery

V1.0 update

AC in-->One touch -->Power button--> Clear CMOS
Always short-->AC in-->Power button--> Crisis

NCT6685D_LQFP128_14X14

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2014/04/01

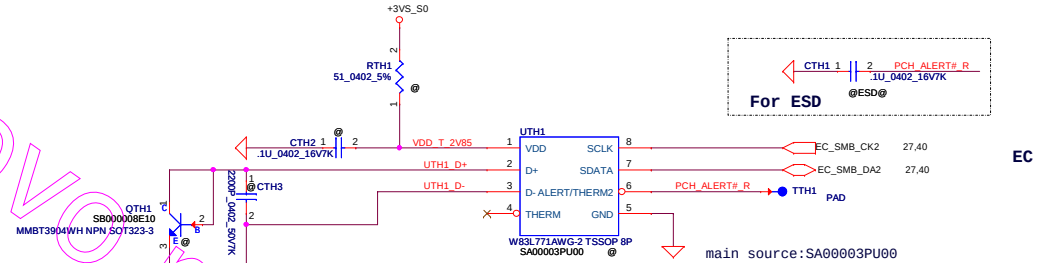
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

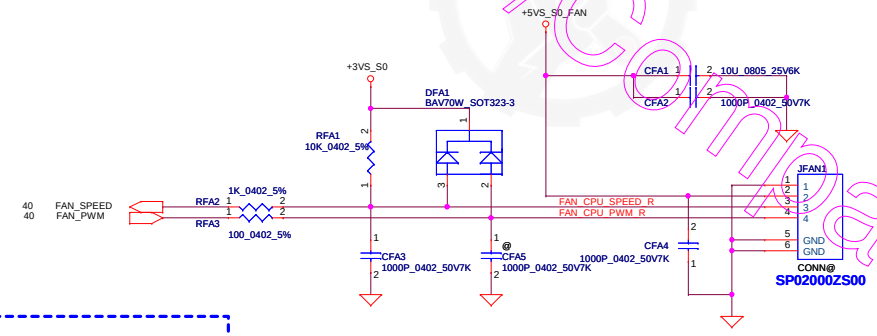
Title: EC NCT6685

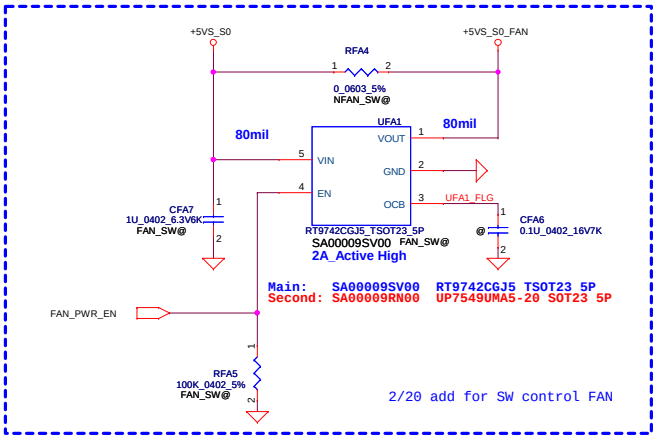
Size: Custom | Document Number: LA-E822P M/B | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 40 of 60



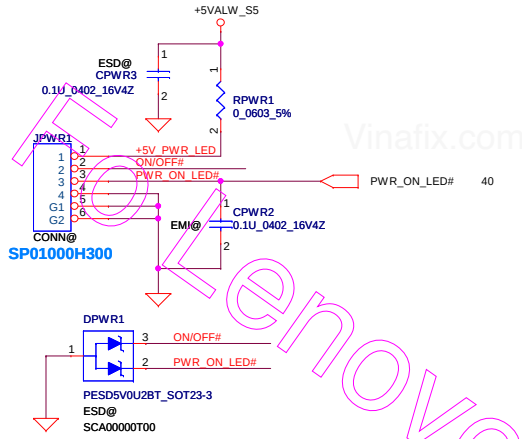
EC



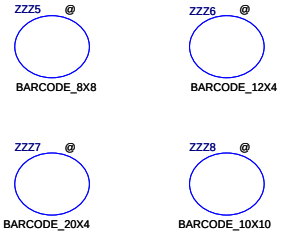


Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/10/02

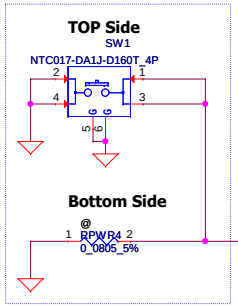
Compal Electronics, Inc.			
Title	FAN/Thermal Sensor		
Size	Document Number	LA-E822P M/B	Rev 0.1
Date: Friday, March 31, 2017	Sheet 41 of 60		



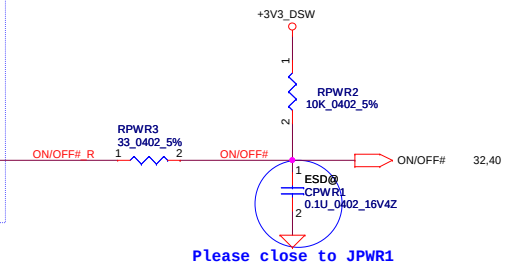
BARCODE



ON/OFF switch

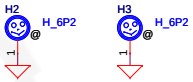


Power Button



WIFI Hole

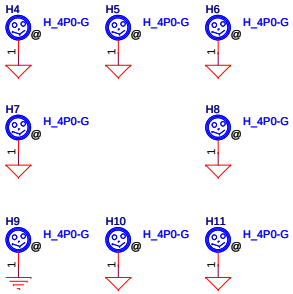
SSD Hole



Other Hole

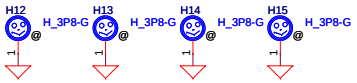
Screw Hole

4.0 mm x 8



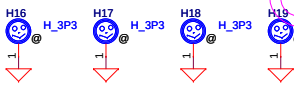
CPU Hole

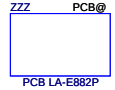
3.8 mm x 4



GPU Hole

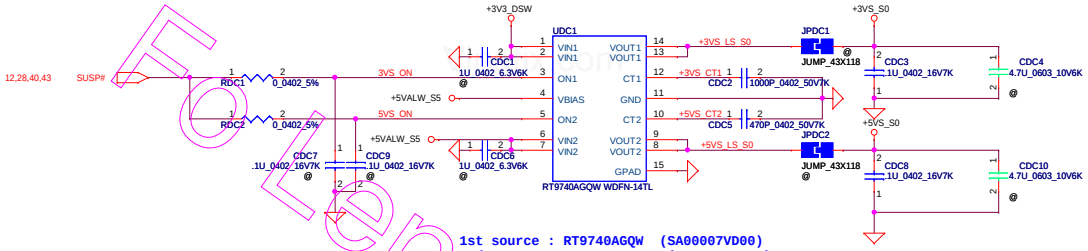
3.3 mm x 4





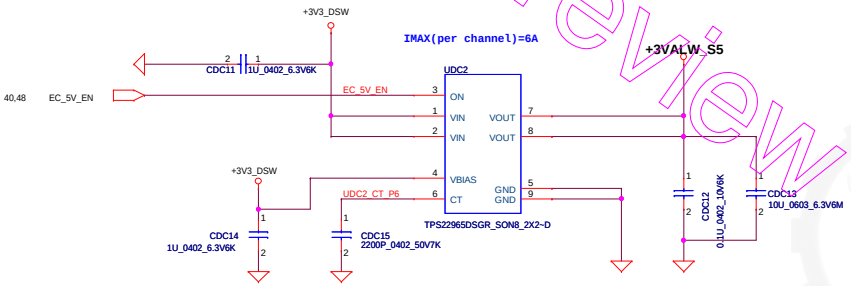
Compal Electronics, Inc.	
Title	PWR SW/LED/SCREW
Size: Custom	Document Number: LA-E822P M/B
Rev	0.1
Date: Friday, March 31, 2017	Sheet 42 of 60

VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

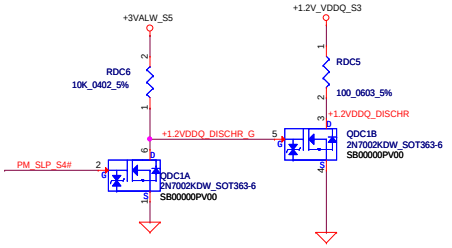


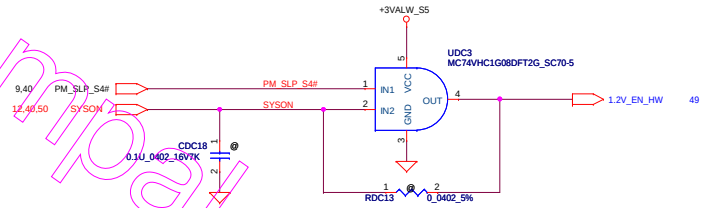
1st source : RT9740AGQW (SA00007VD00)
2nd source : TPS22966DPUR (SA00004MM00)

+3VDSW_S5 to +3VALW_S5 Transfer

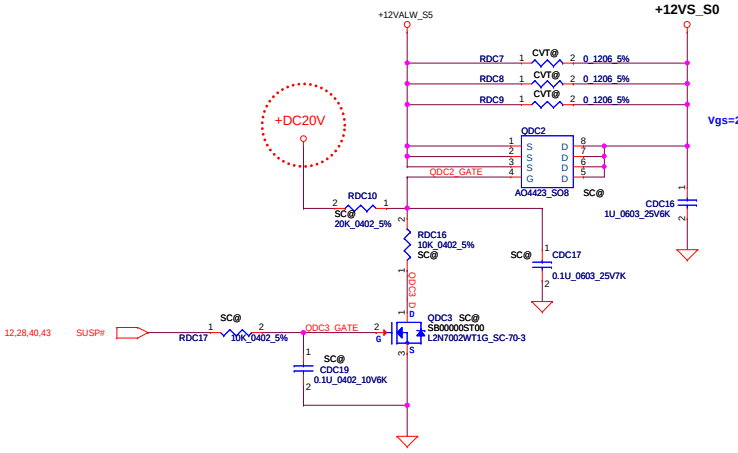


1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)





+12VALW_S5 TO +12VS_S0 (PMOS)



Vgs=20V,Id=15A,Rds=7mohm

	+12VALW_S5	+12VS_S0	BOM
Converter SKU	+12VALW_S5 = +12VS_S0 , Enable: HW_12V_EN# (Follow SPL_S3#)		RDC7,RDC8,RDC9
Scalar SKU	HW_12V_EN#(Follow SCALER_ON#)	SUSP# (Follow SPL_S3#)	QDC2,RDC10,RDC16,RDC17,CDC19,CDC16

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date 2016/03/27	Title: DC INTERFACE
			Size: C; Document Number: LA-E822P M/B; Rev: 0.1
			Date: Friday, March 31, 2017; Sheet 43 of 60

CPU CORE

Module model information

NCP81218_U22U42_COLAY_KBL_V1A.mdd for IC portion

NCP81218_U22U42_COLAY_KBL_V1B.mdd for SW portion

Copy the schematic to new page,
the co-lay location maybe changed.

PRI2, PRI8 place near CPU side.
If the resisters are at HW side and POP. PRI2, PRI8 can be canceled.

PRI11, PRI16 place near CPU side.
If the resisters are at HW side and POP. PRI11, PRI16 can be canceled.

PSYS
Please confirm charger pull low resistance.
Charger side should be unpop.

OCP for VCCSA

RDRPSP

IccMAX@SA= 5A
RIccMAX@SA= 15.8K ---->PRI65

RIccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K ---->PRI14

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=24K ---->PRI5

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.78K ---->PRI4

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

Close to SA choke

IMVP8_EN
Upper Threshold > 0.8V
Lower Threshold < 0.3V

+1.0V_VCCST_S3
confirm with power sequence,
it need behind +5VS.

**PRI26 and PRI33 pull high resistor are pop at the end of VR SVID.
Other VR is unpop.**

RIOUT@VCORE:
U22 = 32.4K PRI23
U42 = 32.4K PRI23

IoutGT:
For U22: PRI42=82.5K
For U42: PRI42=82.5K

RPH@VCORE:
U22 =71.5K PRI30,PRI38(De-pop)
U23e =71.56K PRI30,PRI38

Close to VCORE1 choke

VCORE OCP U42@
U22 12.7K PRI39
U42 24.9K

Close to VCORE1 MOS

For U22:
PRI43=De-pop
For U42:
PRI43,PRI38=Pop

For U22:
PRI47=2K, PRI54=De-pop
For U42:
PRI47,PRI54=2K

For U22:
PCI23=De-pop
For U42:
PCI23=0.047u

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

NCP81218 Operating Frequency
I/A and GT are 450KHz and SA is 600KHz

Fsw for CORE & GT

RiccMAX2ph:
For U22:
PRI63=51.1K
For U42:
PRI63=102K
PRI63 U42@
102K_0402_1%

RiccMAX1a:
For U22:
PRI64=97.6K
For U42:
PRI64=97.6K

VBOOT:
51.1K for debuge setting.

Close to VGT choke

Close to VGT MOS

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

PRI51, PRI58 place near CPU side.
If the resisters are at HW side and POP. PRI51, PRI58 can be canceled.

OCP for VGT

U22 OCP@VCORE= 40A
RLIM@VCORE=9.76K ---->PRI39
U42 OCP@VCORE= 70A
RLIM@VCORE=16.9K ---->PRI39

RLIM= IoutLIMIT * Load line/10

U22 IccMAX@VCORE= 32A
RIccMAX2ph= 51.1K ---->PRI63
U42 IccMAX@VCORE= 64A
RIccMAX2ph= 100k ---->PRI63

RIccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127

U22 Iout@VCORE= 32A
RIOUT@VCORE=26.1K ---->PRI23
U42 Iout@VCORE= 64A
RIOUT@VCORE=23.2K ---->PRI23

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

U22 Load line@VCORE= 2.4m
RPH@VCORE=113K ---->PRI30
U42 Load line@VCORE= 2.4m
RPH@VCORE=113K ---->PRI30,PRI38

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH

U22/U42 Load line@GT= 3.1m
RDRPSP@VCORE=2.74K ---->PRI56

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

U22 IccMAX@GT= 31A
RIccMAX@GT= 97.6K ---->PRI64
U42 IccMAX@GT= 28A
RIccMAX@GT= 88.7K ---->PRI64
RIccMAX@GT= IccMAX*2V/10uA/64A

U22 IOUTSP@GT= 31A
RIOUTSP@GT=57.6K ---->PRI42
U42 IOUTSP@GT= 28A
RIOUTSP@GT=63.4K ---->PRI42
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@GT= 39A
RLIMSP@VCORE=29.4K ---->PRI53

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

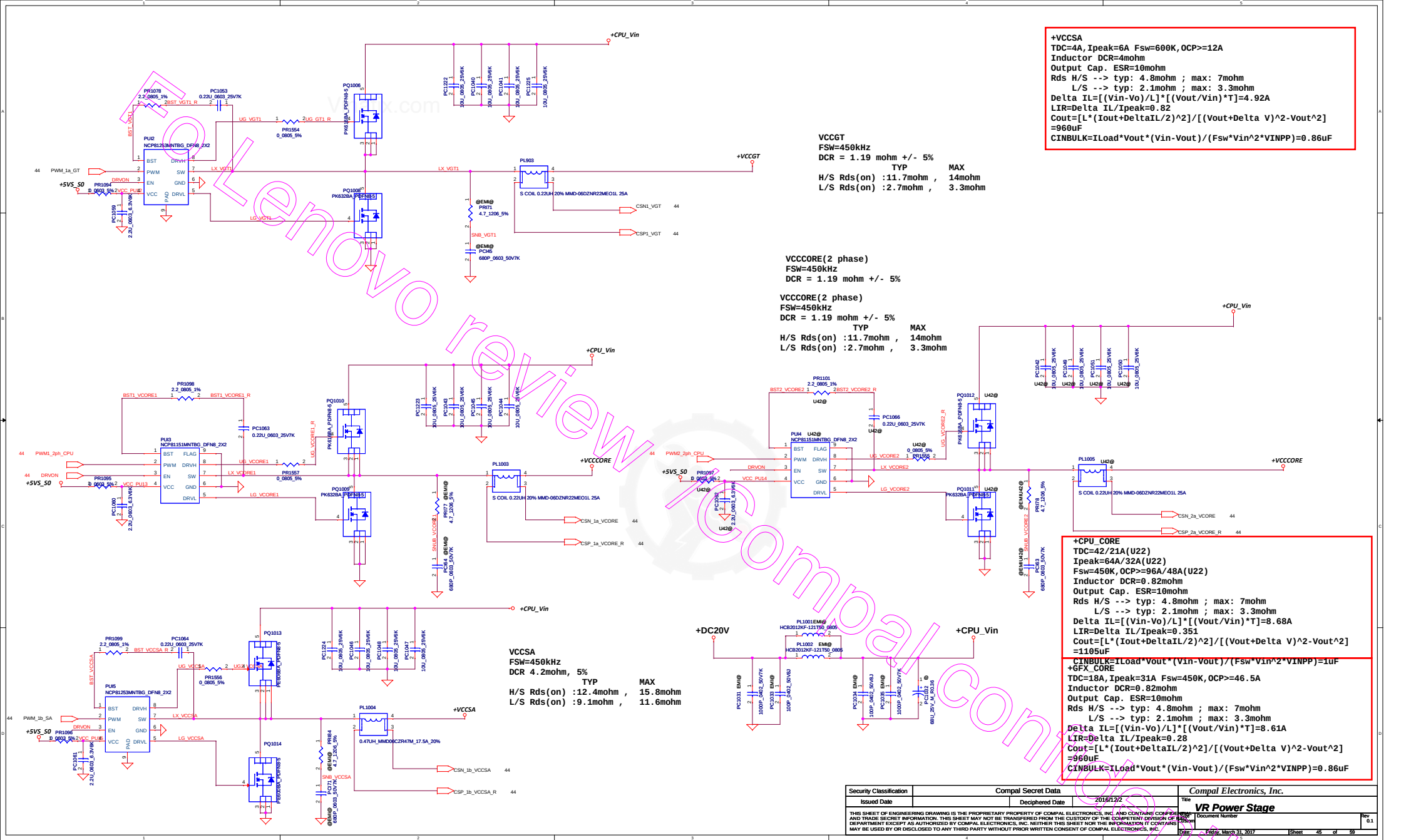
Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2016/12/2

Compal Electronics, Inc.

Title: **VR Controller**

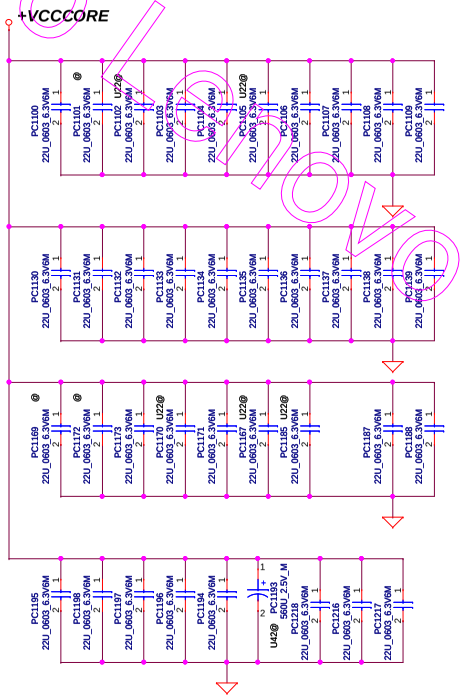
Size	Document Number	Rev
C		0.1

Date: Friday, March 31, 2017 Sheet 44 of 59



+IA_CORE_S0

+VCCCORE

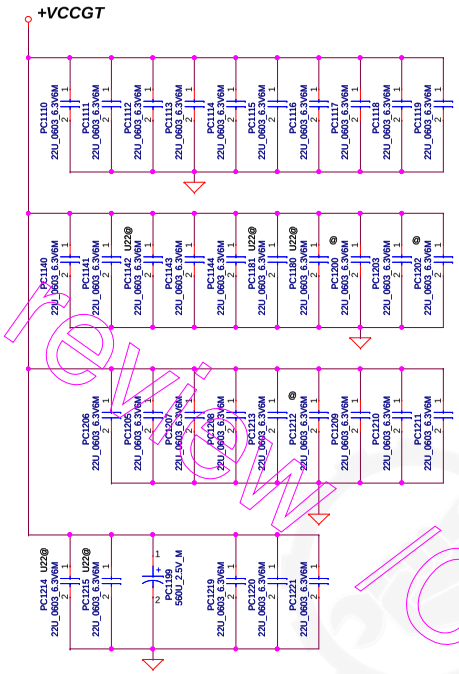


IA_CORE(U22)
22uF_0603*35

IA_CORE(U42)
22uF_0603*30
560uF_10m*1

+GT_CORE_NB_S0

+VCCGT

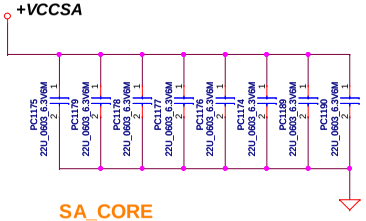


GT_CORE(U22)
IccMax=31A
22uF_0603*32
560uF_10m*1

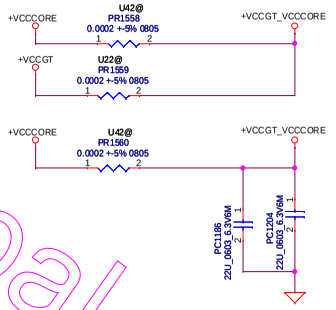
GT_CORE(U42)
IccMax=31A
22uF_0603*27
560uF_10m*1

+VCCSA_S0

+VCCSA



SA_CORE
U22 22uF_0603*8
U42 22uF_0603*8



VCC_CORE :	VCC_GT :	VCC_SA :
U22	U22 & U42	U22 & U42
22uF*28	330uF*1	22uF*9
1uF*35	22uF*33	1uF*7
	0.47uF*4	
U42	1uF*9	
330uF*1		
22uF*32		
1uF*35		

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2016/12/2

Title	VR Output Cap		
Size C	Document Number		Rev 0.1
Date:		Sheet 46 of 59	

Main source:AON6405
PD =I^2*Rds(on)=6^2*11m ohm=0.396W
θ JA= 40°C/W*0.396W=15.84°C

Second source:
PD =I^2*Rds(on)=6^2*12m ohm=0.432W
θ JA= 50°C/W*0.468W=21.6°C

BOM Control

DC_IN_S1

DC_IN_S2

VIN_B2B

CONN@ PJP1
GND
GND
GROUND
POWER
DETECT
POWER
GROUND
LOTES_AJAK0031-P002A

PL1 EMI@ HCB2012KF-121T50_0805
PL2 EMI@ HCB2012KF-121T50_0805

PC5 EMI@ 1000P_0402_50V7K
PC6 EMI@ 100P_0402_50V8J
PC7 EMI@ 100P_0402_50V8J
PC8 EMI@ 1000P_0402_50V7K

PR2 2.2_1206_5%
PC9 2.2U_1206_50V7K
DC_IN_S2

PC1 0.22U_0603_25V7K
PR3 200K_0402_1%

PQ1205 PZ0703EK_P_DFN56-8-5

PC2 0.022U_0603_25V7K
PC3 @EMI@ 0.1U_0603_25V7K
PC4 @ 100U_25V_M

PL1012 @ HCB2012KF-121T50_0805
PL1013 @ HCB2012KF-121T50_0805
PR1 0.01_1206_1%

+DC20V

P=I^2* R(max)=0.3636W

main source : LOTES AJAK0031-P002A
second srouce:Drapho PJSS0056-C011H

RTC BATT CONNECTER

PJP2 CONN@
LOTES_AAA-BAT-054-K01

+RTCBATT_G3

Current Limit Function

+3VS_S0

PU1 INA300AIDSQR_SON10_2X2
ENABLE
IN+
IN-
LATCH
ALERT#
LIMIT
DELAY
HYS
TP
GND
VS

PR14 0_0402_5%
PR15 0_0402_5%
PC11 100P_0402_50V8J
PR12 100K_0402_1%
PR13 10K_0402_1%
PR16 2.61K_0402_1%
PC12 .1U_0402_16V7K

INA300_IN+
INA300_IN-
INA300_EN
INA300_LIMIT
INA300_LATCH 40
INA300_ALERT# 40

+5VS_S0

+3VL_S5

+3VL_RTC_S5

PR17 0_0402_5%

90W:
Full Load(100%) --> 4.5A
Vtrip=4.5*10m=45mV
VLimit=Vtrip; Rlimit=(45mV+0.5mV)/20uA= 2.275K

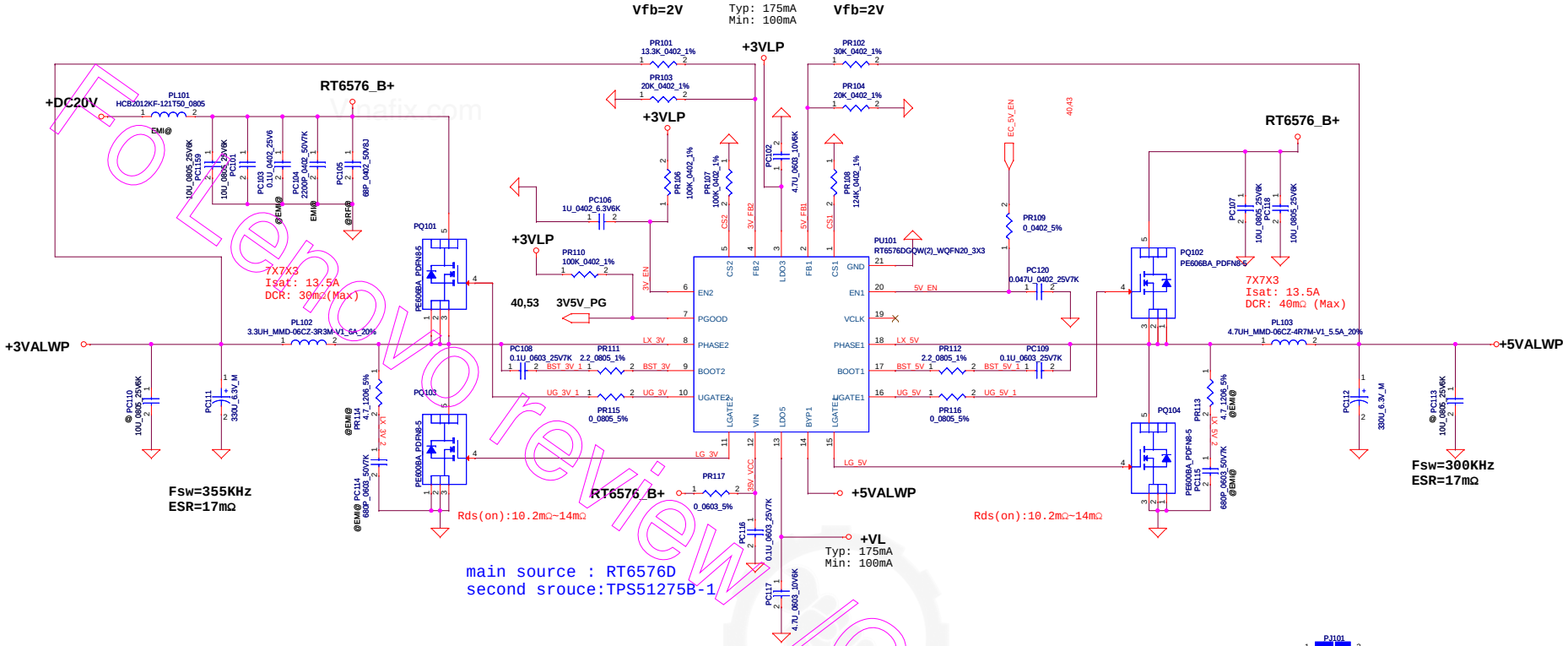
Trigger(116.7%) -->5.25A (@105W)
Vtrip=5.25*10m=52.5mV
Rlimit=(52.5mV+0.5mV)/20uA=2.65K
Select Rlimit=2.61K
I_Trigger-->5.22A

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2016/12/2

Compal Electronics, Inc.

Title: DCIN / CONN

Size: Custom	Document Number	Rev 0.1
Date: Friday, March 31, 2017	Sheet 47 of 59	



+3VALWP
Vin = 20V
Iin =3.3*6/0.85/20
= 1.16A

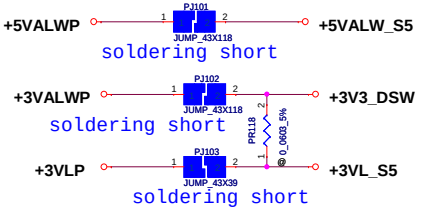
Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(13.3K/20K)]
= 3.3V

+3VALWP
Imax=4.2 ; Ipeak=6 ;Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10A~12.7A
Iin_ripple=1.56A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.352A
LIR=Delta IL/Ipeak=0.392
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=177.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.63uF

+5VALWP
Vin = 20V
Iin =5*7.68/0.85/20
= 2.25A

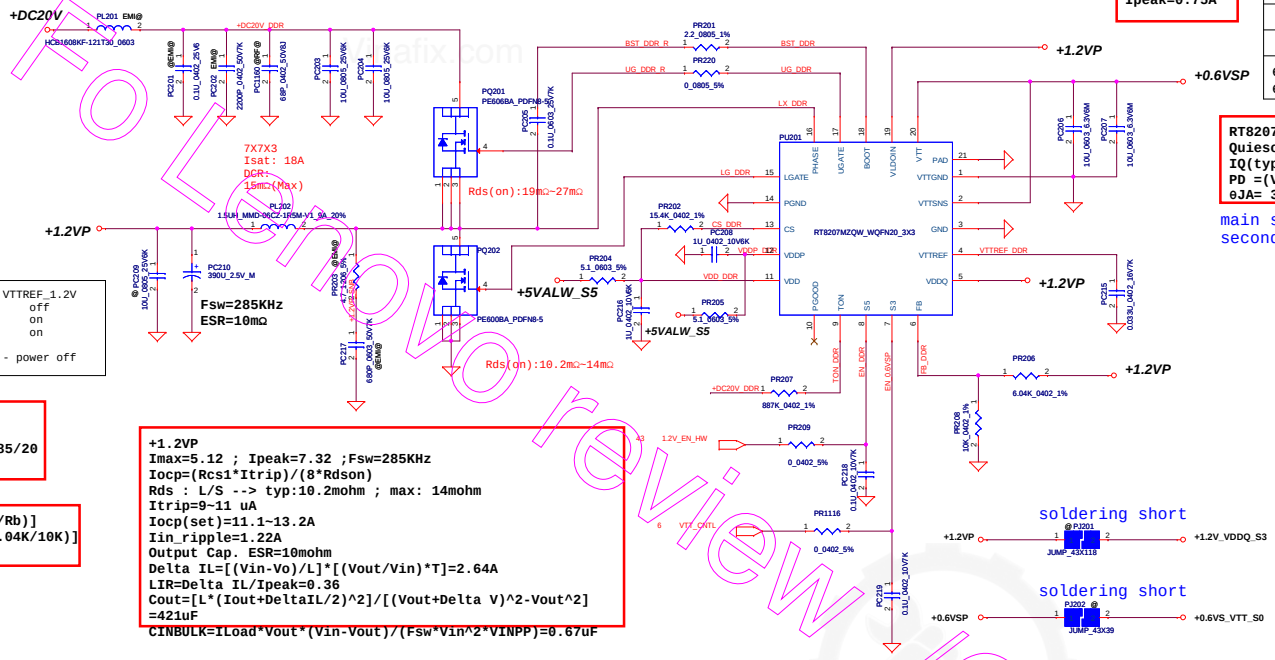
Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(30K/20K)]
=5V

+5VALWP
Imax=5.37A,Ipeak=7.68A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2ohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=12A~14A
Iin_ripple=2.33A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.660A
LIR=Delta IL/Ipeak=0.391
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=250uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.88uF



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date 2016/12/2	Title +3VALWP / +5VALWP

Size C	Document Number		Rev 0.1
Date: Friday, March 31, 2017	Sheet 48 of 59		



Rds(on):19mΩ~27mΩ

Rds(on):10.2mΩ~14mΩ

7X7X3
Isat: 18A
DCR:
15mΩ(Max)

Fsw=285KHz
ESR=10mΩ

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.2VP
Vin = 20V
Iin =7.32*1.2/0.85/20
= 0.51A

Vout = Vfb*[1+(Rt/Rb)]
= 0.75*[1+(6.04K/10K)]
= 1.203V

+1.2VP
Imax=5.12 ; Ipeak=7.32 ;Fsw=285KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.1~13.2A
Iin_ripple=1.22A
Output Cap. ESR=10mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.64A
LIR=Delta IL/Ipeak=0.36
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=421uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.67uF

+0.6VSP
TDC=0.53A
Ipeak=0.75A

Vo	0.6	
Vin	1.2	
Io	0.75	
PD	0.455	
θJA(main) θJA(2nd)	52 68	°C/W

RT8207M:
Quiescent Current (GND Current)
IQ(typ)=0.47mA,IQ(max)=1mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.455W
θJA= 33.7°C/W*0.903=23.66°C

main source : RT8207MZQW
second srouce:UP1566PQKF

Security Classification	Compal Secret Data	
Issued Date	Deciphered Date	2016/12/2

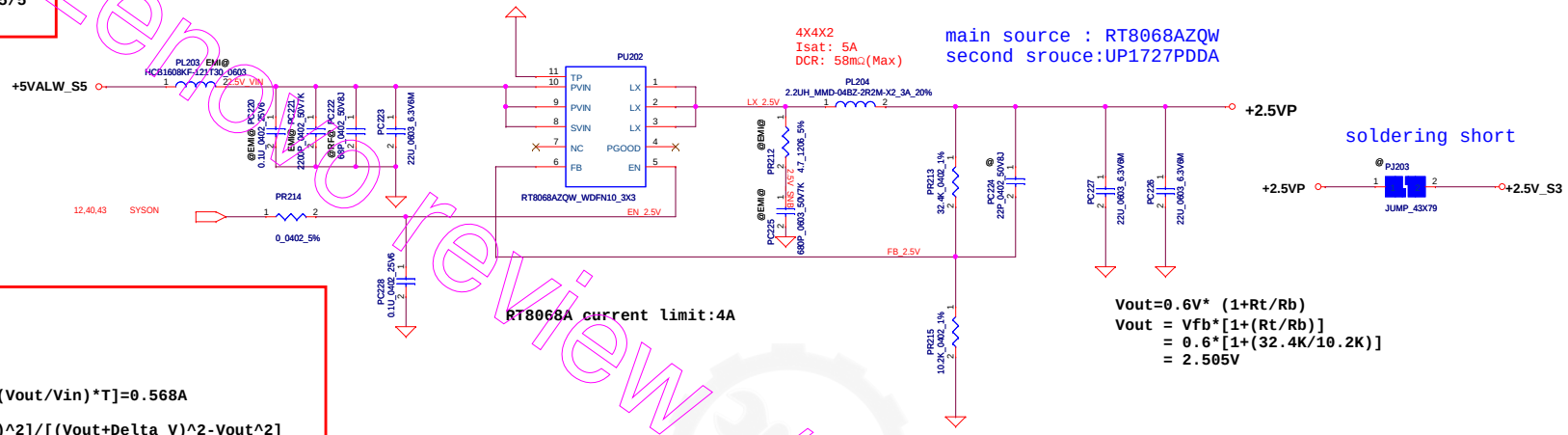
Compal Electronics, Inc.

Title: +1.2VP/+0.6VSP

Size: Custom | Document Number | Rev: 0.1

Date: Friday, March 31, 2017 | Sheet 49 of 59

+2.5VP
Vin =5V
Iin = 2.5*2.24/0.85/5
=1.32A

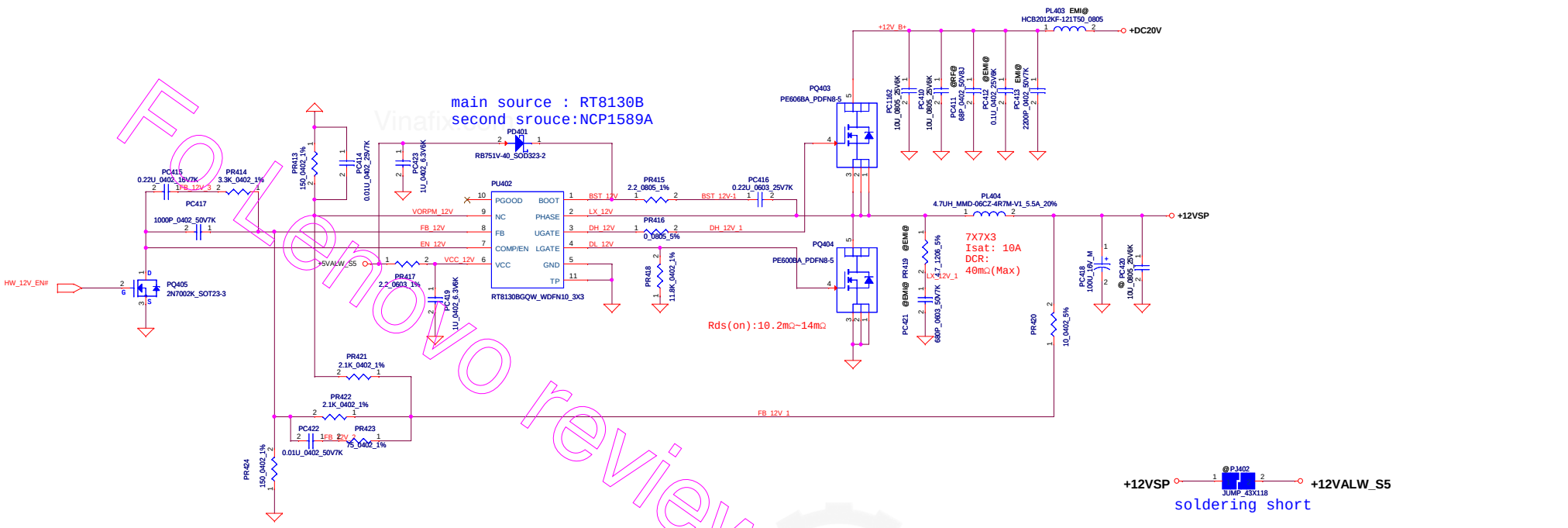


RT8068A current limit:4A

Vout=0.6V* (1+Rt/Rb)
Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(32.4K/10.2K)]
= 2.505V

+2.5VP
Ipeak=2.24A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.75A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta IL/Ipeak=0.25
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.78uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date 2016/12/2	Title +2.5VP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size C / Document Number / Rev 0.1
			Date: / Sheet 50 of 59



+12VSP
Imax=2.4A,Ipeak=3.43A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10.11~11.98A
Iin_ripple=0.546A
Output Cap. ESR=24mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.404A
LIR=Delta IL/Ipeak=0.992
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=9.02uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.96uF

Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(2.21K/158)]
= 11.99V

+12VSP
Vin = 20V
Iin = 12*2.4/0.85/20
= 2.42A

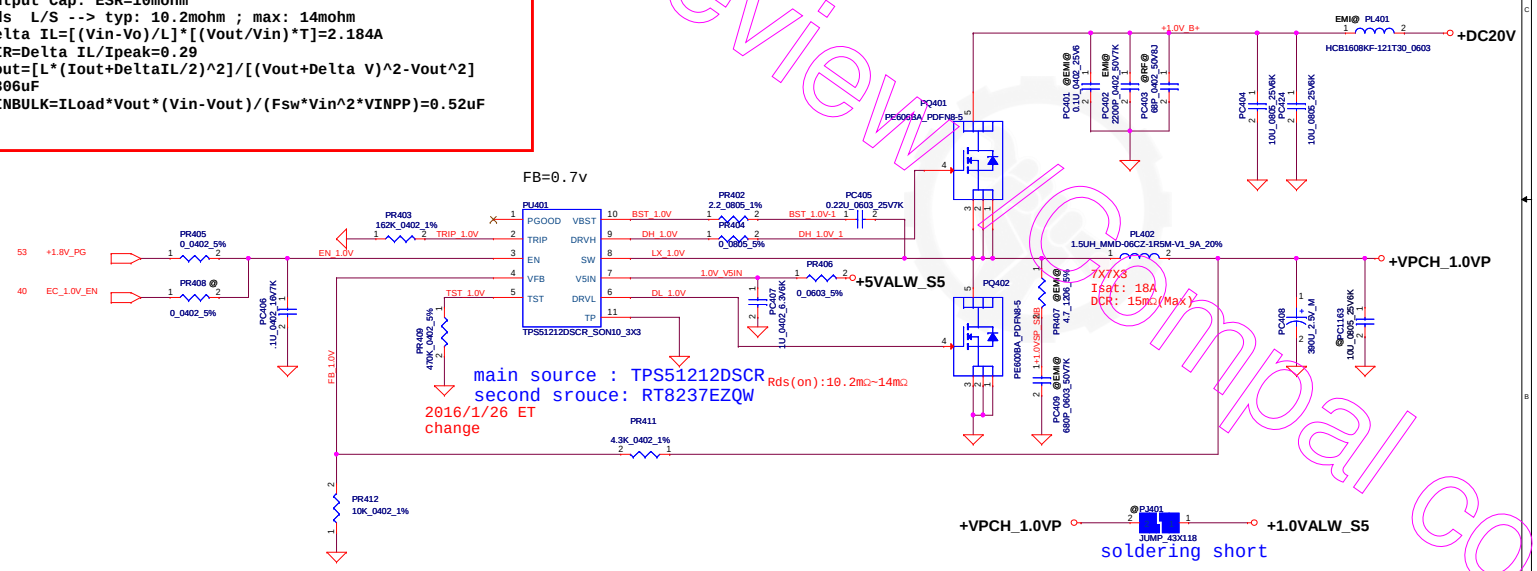
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date 2016/12/02	Title +12VSP
			Size C / Document Number / Rev 0.1
			Date: / Sheet 51 of 59

+VPCH_1.0VP
Ipeak=9.04A,Imax=6.33 ; Iocp=14.44A~15.67A

Fsw=290K
Iin_ripple= 1.38A
Output Cap. ESR=10mohm
Rds L/S --> typ: 10.2mohm ; max: 14mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.184A
LIR=Delta IL/Ipeak=0.29
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=806uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.52uF

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(4.42K/10.2K)]
= 1.003V

+1VP
Vin = 20V
Iin =9.04*1/0.85/20
= 0.53A



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2013/08/29

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

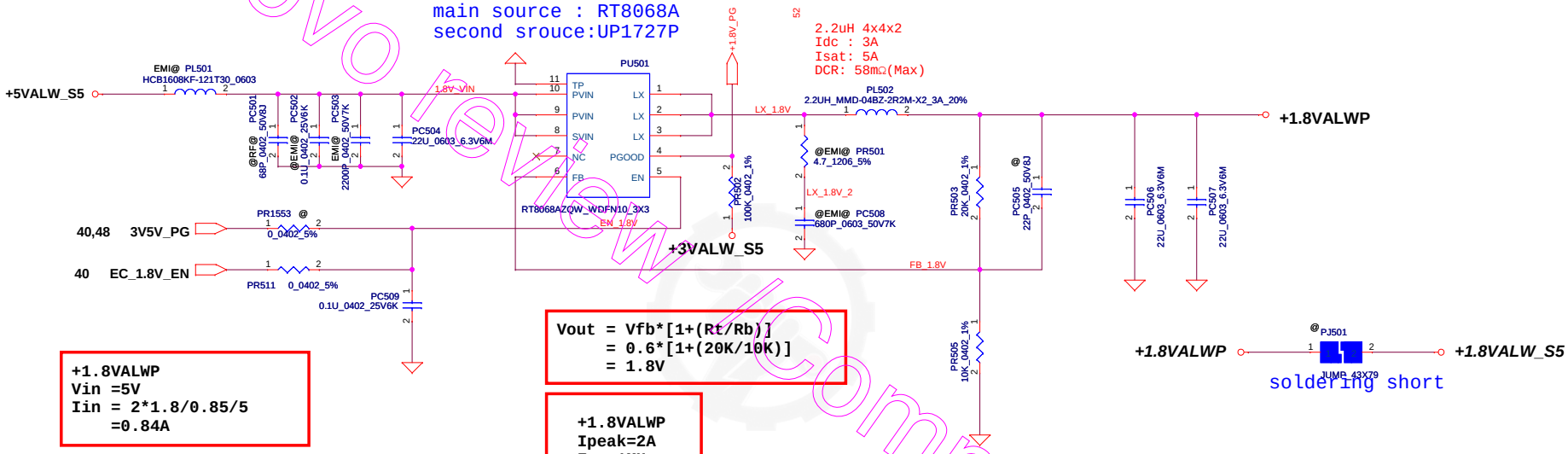
Compal Electronics, Inc.

Title: +VPCH_1.0VP/+12VSP

Size: Custom | Document Number | Rev: 0.1

Date: | Sheet 52 of 60

main source : RT8068A
second srouce:UP1727P



2.2uH 4x4x2
Idc : 3A
Isat: 5A
DCR: 58mΩ(Max)

soldering short

Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(20K/10K)]
= 1.8V

+1.8VALWP
Vin =5V
Iin = 2*1.8/0.85/5
=0.84A

+1.8VALWP
Ipeak=2A
Fsw=1MHz

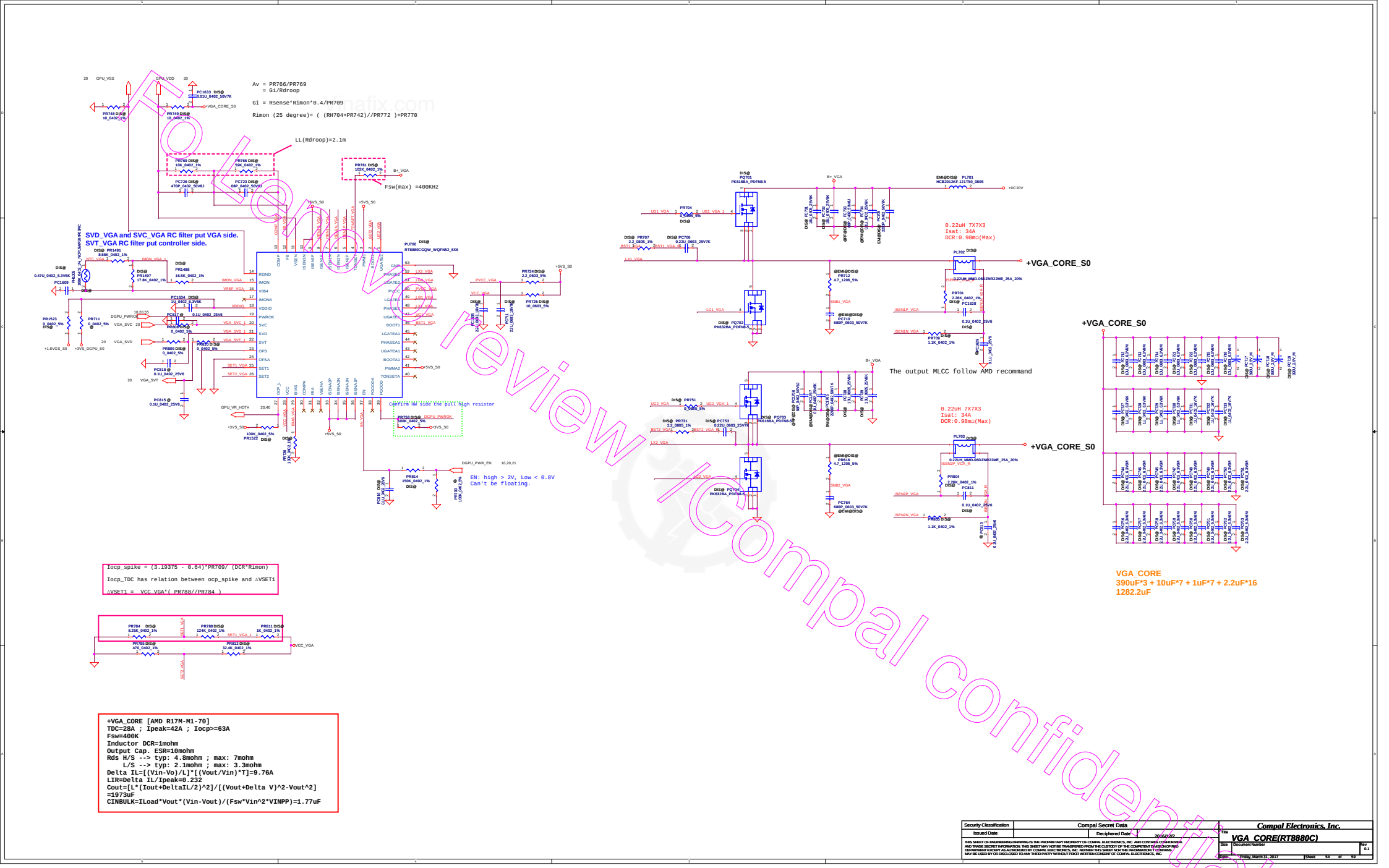
+1.8VALWP
Ipeak=1.5A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.17A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.524A
LIR=Delta IL/Ipeak=0.26
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=2.48uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.16uF

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2016/12/2

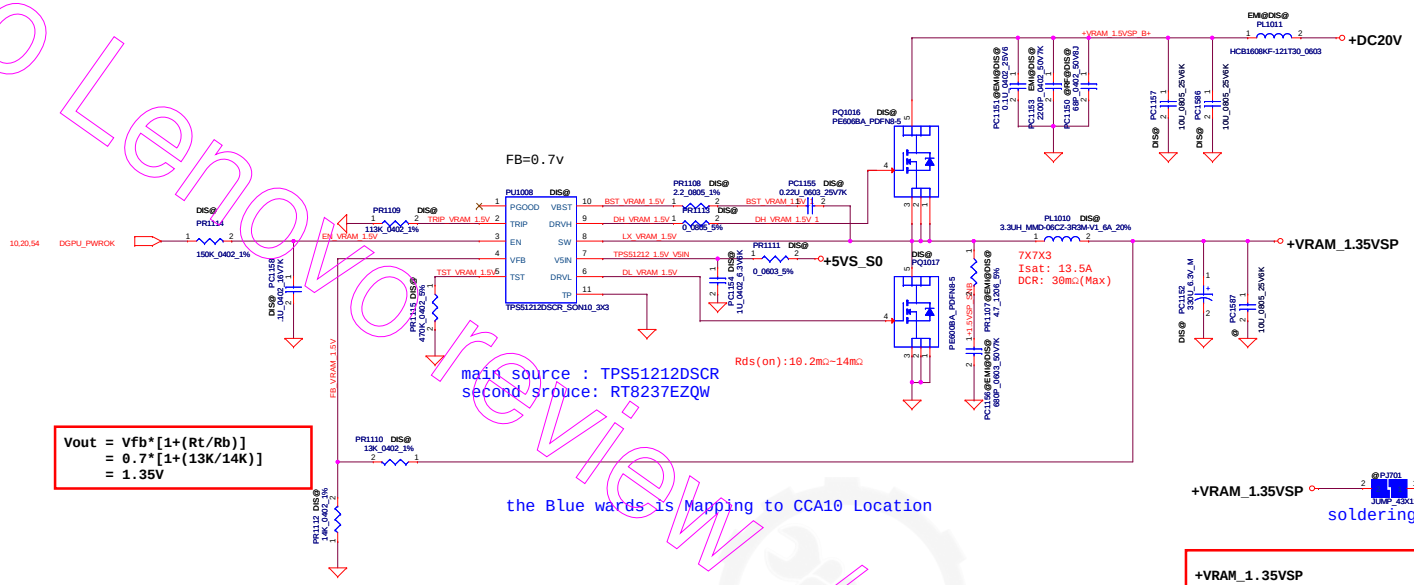
Compal Electronics, Inc.

Title: +1.8VSP

Size	Document Number	Rev 0.1
Date: Friday, March 31, 2017	Sheet 53 of 59	


Av = PR766/PR769
= Gi/Rdroop
Gi = Rsense*Rimon*0.4/PR709
Rimon (25 degree)= ((RH704+PR742)//PR772)+PR770
LL(Rdroop)=2.1m
Fsw(max) =400KHz
SVD_VGA and SVC_VGA RC filter put VGA side.
SVT_VGA RC filter put controller side.
The output MLCC follow AMD recommand
0.22uH 7X7X3
Isat: 34A
DCR:0.98mΩ(Max)
+VGA_CORE_S0
VGA_CORE
390uF*3 + 10uF*7 + 1uF*7 + 2.2uF*16
1282.2uF
Iocp_spike = (3.19375 - 0.64)*PR709/ (DCR*Rimon)
Iocp_TDC has relation between ocp_spike and ΔVSET1
ΔVSET1 = VCC_VGA*(PR788//PR784)
+VGA_CORE [AMD R17M-M1-70]
TDC=28A ; Ipeak=42A ; Iocp>=63A
Fsw=400K
Inductor DCR=1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=9.76A
LIR=Delta IL/Ipeak=0.232
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1973uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.77uF
EN: high > 2V, Low < 0.8V
Can't be floating.
Security Classification
Compal Secret Data
Issued Date
Deciphered Date
2016/0/22
Compal Electronics, Inc.
VGA_CORE(RT8880C)
Size
Document Number
Rev
0.1
Date: Friday, March 31, 2017
Sheet 54 of 59

+VRAM_1.35VSP
Vin = 20V
Iin = 1.35*5.38/0.85/20
= 0.3A



main source : TPS51212DSCR
second srouce: RT8237EZQW

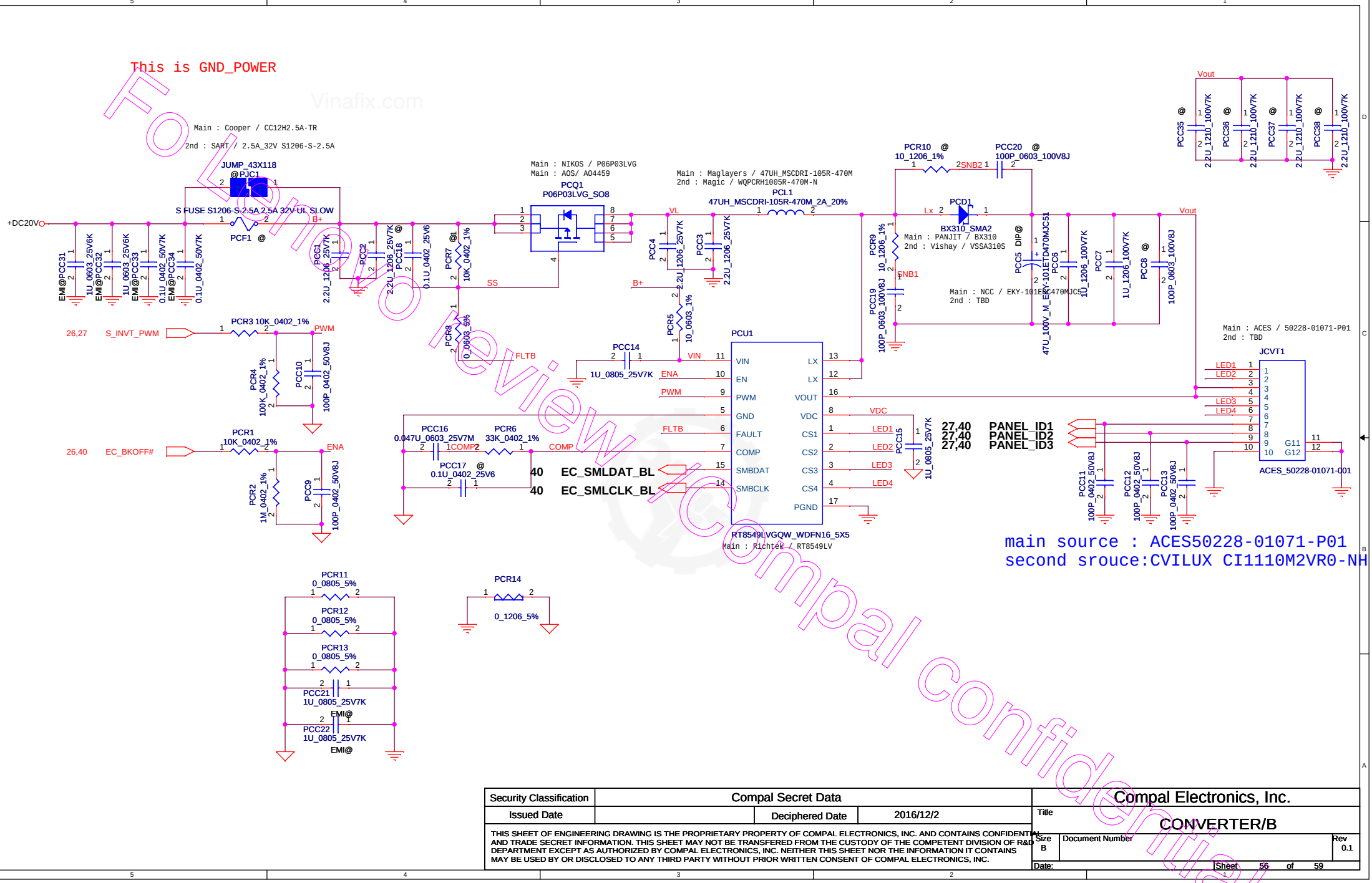
Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(13K/14K)]
= 1.35V

the Blue wards is Mapping to CCA10 Location

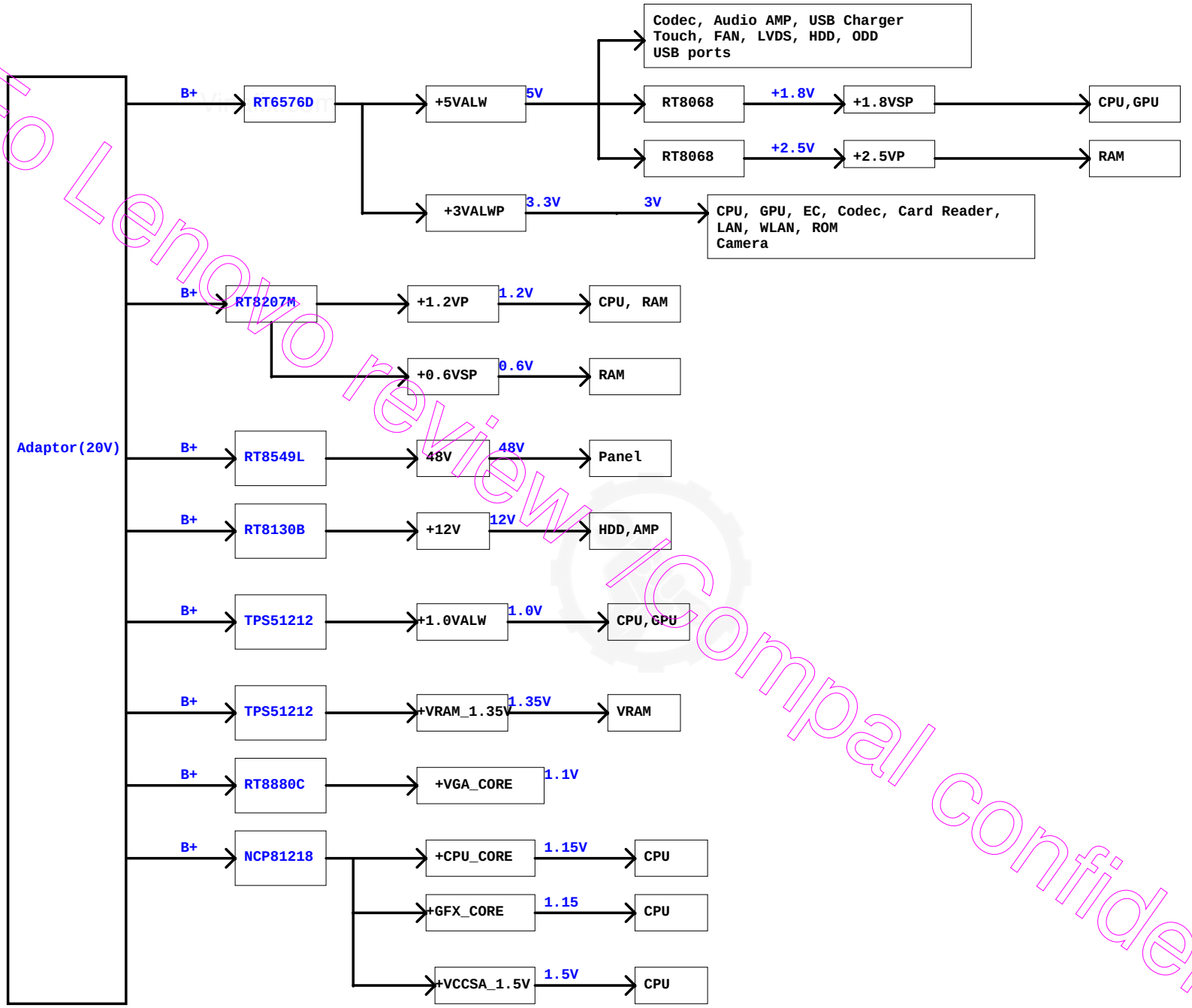
soldering short

+VRAM_1.35VSP
Imax=2.69A,Ipeak=3.8A ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ: 10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.61~13.56A
Iin_ripple=0.67A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.315A
LIR=Delta IL/Ipeak=0.346
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=327uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.29uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date 2016/12/2	Title: VRAM 1.35V
Size: Custom	Document Number		Rev: 0.1
Date:		Sheet 55 of 59	



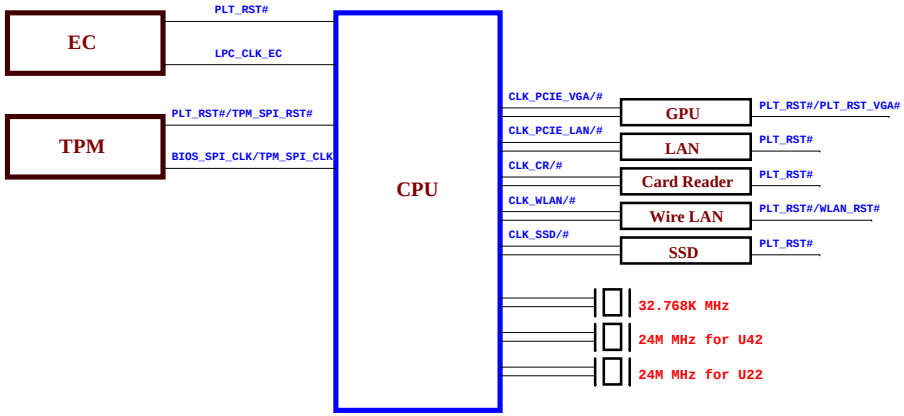
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date 2016/12/2	Title CONVERTER/B
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size B / Document Number / Rev 0.1
			Date: / Sheet 56 of 59



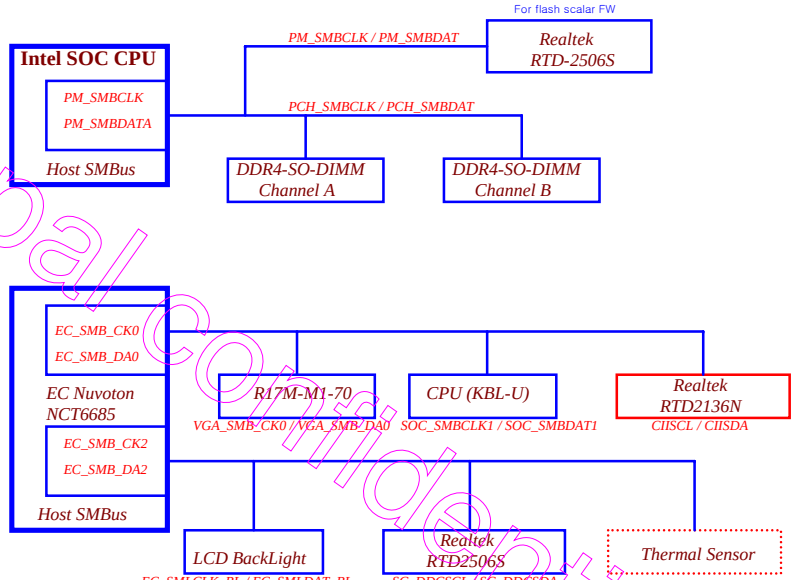
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/12/18	Deciphered Date 2013/12/18	Title: Power Rail

Size: Custom	Document Number		Rev: 0.1
Date: Friday, March 31, 2017	Sheet 57 of 59		

System clock and Reset map



SMBUS Block Diagram



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date 2015/10/02	Title: GPIO Table & SMBUS BD
			Size: Document Number: LA-E822P M/B Rev: 0.1
Date: Friday, March 31, 2017		Sheet 59 of 60	