LV550 AMD Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

Properties

DY	***DUMMY, NOT ASM, not assemble***
MEM_IDx_x	***Memory ID for SW Team (BOM Control)***
PCB_ID	***PCB ID for SW Team (PCB version)***
SKU_ID	***SKU ID for SW Team (Model ID)***
HDT	***Debug Connector***
PSL	***KBC Power Switched Logic***
MS/ NON_MS	***Modern stand by / NON Modern stand by***
TPM	***TPM***

LV550 AMD

緯創資通 **Wistron Corporation**
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Title: ***Cover Page***

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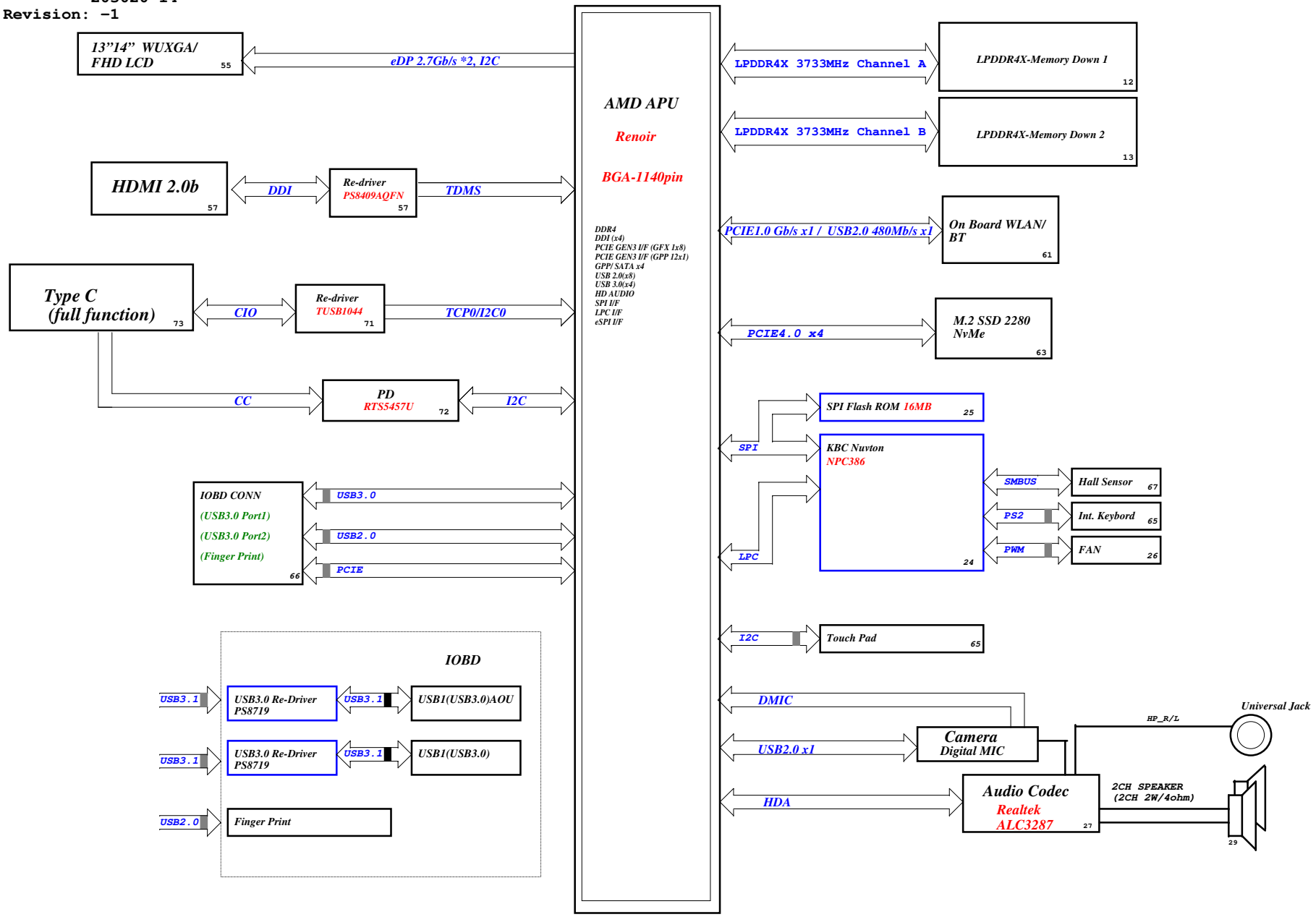
Project code: 4PD0LX010001
(13") LV550-13AR: 4PD0M5010001
(14") LV550-14AR: 4PD0M4010001
PCB P/N: 203004 13"
203020 14"
Revision: -1

LV550 AMD Block Diagram

AMD Cezanne new project code:
LV550-13AC: 4PD0NK010001
LV550-14AC: 4PD0NK01A001



PCB Layer Stackup

L1 : Signal
L2: GND\POWER
L3: Signal
L4: Signal
L5: GND\POWER
L6: Signal
L7: GND\POWER
L8: Signal

Battery Charger/Selector BQ25700ARSNR		44
PWR_ADP_TOSYS	19V_DCBATOUT BT+	
System DC/DC TPS51395PRJER		45
19V_DCBATOUT	5V_S5 5V_AUX_S5	
System DC/DC TPS51393PRJER		45
19V_DCBATOUT	3D3V_S5 3D3V_AUX_S5	
CPU_VCORE RT3663BMGQW		46
DC/DC VCCCPUCORE AOZ5516QI		47
19V_DCBATOUT	1V_CPU_CORE	
DC/DC VCCCPUCORE RT9610BZQW		48
19V_DCBATOUT	1V_VDDCR_SOC	
DC/DC 1D2V_S3 RT8231CGQW		51
19V_DCBATOUT	1D1V_S3	
DC/DC 0D6V_VREF_S0 RT8231AGQW		51
1D1V_S3	0D6V_S3	
DC/DC 0D75V_S5 RT5797ALGQW		52
3D3V_S5	0D75V_S5	
DC/DC 0D75V_S0 RT5797ALGQW		52
3D3V_S5	0D75V_S0	
1D8V_S5 SY8386RHC		53
19V_DCBATOUT	1D8V_S5	

LV550 AMD

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Title: Block Diagram
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SSID = PCH

SSD1 M.2 (PCIE)

63	SSD_PCIE_RX_P0
63	SSD_PCIE_RX_N0
63	SSD_PCIE_RX_P1
63	SSD_PCIE_RX_N1
63	SSD_PCIE_RX_P2
63	SSD_PCIE_RX_N2
63	SSD_PCIE_RX_P3
63	SSD_PCIE_RX_N3
63	SSD_PCIE_TX_CON_P0
63	SSD_PCIE_TX_CON_N0
63	SSD_PCIE_TX_CON_P1
63	SSD_PCIE_TX_CON_N1
63	SSD_PCIE_TX_CON_P2
63	SSD_PCIE_TX_CON_N2
63	SSD_PCIE_TX_CON_P3
63	SSD_PCIE_TX_CON_N3

WLAN

61	WLAN_PCIE_RX_N
61	WLAN_PCIE_RX_P
61	WLAN_PCIE_TX_CON_N
61	WLAN_PCIE_TX_CON_P

GFX & GPP, 85Ω

CPU1B

PCIE

G13	P_GFX_RXP0	F4	P_GFX_TXP0
F13	P_GFX_RXN0	F2	P_GFX_TXN0
J14	P_GFX_RXP1	F3	P_GFX_TXP1
H14	P_GFX_RXN1	E4	P_GFX_TXN1
G15	P_GFX_RXP2	E1	P_GFX_TXP2
F15	P_GFX_RXN2	C1	P_GFX_TXN2
J15	P_GFX_RXP3	D5	P_GFX_TXP3
K15	P_GFX_RXN3	E6	P_GFX_TXN3
H16	P_GFX_RXP4	C6	P_GFX_TXP4
J16	P_GFX_RXN4	D6	P_GFX_TXN4
F18	P_GFX_RXP5	B6	P_GFX_TXP5
G18	P_GFX_RXN5	C7	P_GFX_TXN5
J18	P_GFX_RXP6	D8	P_GFX_TXP6
K18	P_GFX_RXN6	B8	P_GFX_TXN6
H19	P_GFX_RXP7	C8	P_GFX_TXP7
G19	P_GFX_RXN7	A8	P_GFX_TXN7

M.2 SSD1 (PCIE)

SSD_PCIE_RX_P0	G11	P_GPP_RXP0	L3	P_GPP_TXP0	SSD_PCIE_TX_P0	C305 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_P0
SSD_PCIE_RX_N0	F11	P_GPP_RXN0	L1	P_GPP_TXN0	SSD_PCIE_TX_N0	C306 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_N0
SSD_PCIE_RX_P1	J10	P_GPP_RXP1	L4	P_GPP_TXP1	SSD_PCIE_TX_P1	C307 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_P1
SSD_PCIE_RX_N1	H10	P_GPP_RXN1	L2	P_GPP_TXN1	SSD_PCIE_TX_N1	C308 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_N1
SSD_PCIE_RX_P2	G8	P_GPP_RXP2/SATA0_RXP	M4	P_GPP_TXP2/SATA0_TXP	SSD_PCIE_TX_P2	C309 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_P2
SSD_PCIE_RX_N2	F8	P_GPP_RXN2/SATA0_RXN	M2	P_GPP_TXN2/SATA0_TXN	SSD_PCIE_TX_N2	C310 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_N2
SSD_PCIE_RX_P3	G6	P_GPP_RXP3/SATA1_RXP	N3	P_GPP_TXP3/SATA1_TXP	SSD_PCIE_TX_P3	C311 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_P3
SSD_PCIE_RX_N3	F7	P_GPP_RXN3/SATA1_RXN	N1	P_GPP_TXN3/SATA1_TXN	SSD_PCIE_TX_N3	C312 1	SCD22U6D3V1MX-1-GP	SSD_PCIE_TX_CON_N3

M.2 SSD1 (PCIE)

M9	P_GPP_RXP4	T2	P_GPP_TXP4	
M8	P_GPP_RXN4	T4	P_GPP_TXN4	
L7	P_GPP_RXP5	R1	P_GPP_TXP5	
L6	P_GPP_RXN5	R3	P_GPP_TXN5	
K7	P_GPP_RXP6	P2	P_GPP_TXP6	
K8	P_GPP_RXN6	P4	P_GPP_TXN6	
H6	P_GPP_RXP7	N2	P_GPP_TXP7	
H7	P_GPP_RXN7	N4	P_GPP_TXN7	

layout impact 0402-> 0201

WLAN

WLAN_PCIE_RX_P	WLAN_PCIE_TX_P	C303 1	SCD1U6D3V1KX-GP	WLAN_PCIE_TX_CON_P
WLAN_PCIE_RX_N	WLAN_PCIE_TX_N	C304 1	SCD1U6D3V1KX-GP	WLAN_PCIE_TX_CON_N

WLAN

L9	P_GPP_RXP8/SATA2_RXP	K2	P_GPP_TXP8/SATA2_TXP
L10	P_GPP_RXN8/SATA2_RXN	K4	P_GPP_TXN8/SATA2_TXN
K11	P_GPP_RXP9/SATA3_RXP	J4	P_GPP_TXP9/SATA3_TXP
J11	P_GPP_RXN9/SATA3_RXN	J2	P_GPP_TXN9/SATA3_TXN
J12	P_GPP_RXP10	H3	P_GPP_TXP10
H12	P_GPP_RXN10	H1	P_GPP_TXN10
J13	P_GPP_RXP11	H4	P_GPP_TXP11
K13	P_GPP_RXN11	H2	P_GPP_TXN11

FP6 REV 0.92
PART 2 OF 13

RENOIR-FP6-GP

ZZ.00CPU.421

LV550 AMD

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (PCIE/SATA)*

Size	Document Number	Rev
A3	LV550 AMD	-1

Date: Monday, August 17, 2020 Sheet 3 of 106

5 4 3 2 1

D

C

(Blanking)

B

A

LV550 AMD

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Title		
	CPU (RSVD)	
Size A4	Document Number **LV550_AMD**	Rev **-1**
Date: Monday, August 17, 2020	Sheet 4 of 106	

SSID = CPU

APU Type 2 does not support Channel A

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer

CPU1A

MEMORY A

Signal	Pin
M_A_DQ[31:0]	M_A_DQ0, M_A_DQ1, M_A_DQ2, M_A_DQ3, M_A_DQ4, M_A_DQ5, M_A_DQ6, M_A_DQ7, M_A_DQ8, M_A_DQ9, M_A_DQ10, M_A_DQ11, M_A_DQ12, M_A_DQ13, M_A_DQ14, M_A_DQ15, M_A_DQ16, M_A_DQ17, M_A_DQ18, M_A_DQ19, M_A_DQ20, M_A_DQ21, M_A_DQ22, M_A_DQ23, M_A_DQ24, M_A_DQ25, M_A_DQ26, M_A_DQ27, M_A_DQ28, M_A_DQ29, M_A_DQ30, M_A_DQ31
M_B_DQ[31:0]	M_B_DQ0, M_B_DQ1, M_B_DQ2, M_B_DQ3, M_B_DQ4, M_B_DQ5, M_B_DQ6, M_B_DQ7, M_B_DQ8, M_B_DQ9, M_B_DQ10, M_B_DQ11, M_B_DQ12, M_B_DQ13, M_B_DQ14, M_B_DQ15, M_B_DQ16, M_B_DQ17, M_B_DQ18, M_B_DQ19, M_B_DQ20, M_B_DQ21, M_B_DQ22, M_B_DQ23, M_B_DQ24, M_B_DQ25, M_B_DQ26, M_B_DQ27, M_B_DQ28, M_B_DQ29, M_B_DQ30, M_B_DQ31
M_A_DQS_DN[3:0]	M_A_DQS_DN0, M_A_DQS_DN1, M_A_DQS_DN2, M_A_DQS_DN3
M_B_DQS_DN[3:0]	M_B_DQS_DN0, M_B_DQS_DN1, M_B_DQS_DN2, M_B_DQS_DN3
M_A_DQS_DP[3:0]	M_A_DQS_DP0, M_A_DQS_DP1, M_A_DQS_DP2, M_A_DQS_DP3
M_B_DQS_DP[3:0]	M_B_DQS_DP0, M_B_DQS_DP1, M_B_DQS_DP2, M_B_DQS_DP3
M_A_CKE0, M_A_CKE1	
M_B_CKE0, M_B_CKE1	
M_A_CS0_N, M_A_CS1_N	
M_B_CS0_N, M_B_CS1_N	
M_A_A0, M_A_A1, M_A_A2, M_A_A3, M_A_A4, M_A_A5	
M_B_A0, M_B_A1, M_B_A2, M_B_A3, M_B_A4, M_B_A5	
M_A_CLK_P, M_A_CLK_N	
M_B_CLK_P, M_B_CLK_N	
M_A_DM1, M_A_DM0, M_A_DM2, M_A_DM3	
M_B_DM2, M_B_DM3, M_B_DM1, M_B_DM0	
M_A_RESET_N	

Pin	Signal
AK26	MA_ADD0/RSVD
AG24	MA_ADD1/RSVD
AG23	MA_ADD2/MAB_CA0
AG26	MA_ADD3/MAA_CA4
AG27	MA_ADD4/MAA_CA5
AF21	MA_ADD5/MAA_CA3
AF22	MA_ADD6/MAA_CA2
AF25	MA_ADD7/RSVD
AF24	MA_ADD8/RSVD
AE21	MA_ADD9/RSVD
AL21	MA_ADD10/MAB_CS_L1
AF27	MA_ADD11/MAA_CKE1
AE23	MA_ADD12/MAA_CKE0
AM23	MA_ADD13_BANK2/RSVD
AM21	MA_WE_L_ADD14/MAB_CKE1
AL27	MA_CAS_L_ADD15/RSVD
AL24	MA_RAS_L_ADD16/MAB_CKE0
AL22	MA_BANK0/MAB_CS_L0
AK27	MA_BANK1/MAB_CA1
AE27	MA_BG0/MAA_CS_L1
AE26	MA_BG1/MAA_CS_L0
AD22	MA_ACT_L/RSVD
L27	MA_DM0/MAA_DM1
N23	MA_DM1/MAA_DM0
R27	MA_DM2/MAA_DM2
Y24	MA_DM3/MAA_DM3
AP27	MA_DM4/MAB_DM2
AW23	MA_DM5/MAB_DM3
AT21	MA_DM6/MAB_DM1
AV18	MA_DM7/MAB_DM0
W24	RSVD_52
M25	MA_DQS_H0/MAA_DQS_H1
M24	MA_DQS_L0/MAA_DQS_L1
P22	MA_DQS_H1/MAA_DQS_H0
P21	MA_DQS_L1/MAA_DQS_L0
T24	MA_DQS_H2/MAA_DQS_H2
R24	MA_DQS_L2/MAA_DQS_L2
AA21	MA_DQS_H3/MAA_DQS_H3
Y21	MA_DQS_L3/MAA_DQS_L3
AP23	MA_DQS_H4/MAB_DQS_H2
AP24	MA_DQS_L4/MAB_DQS_L2
AW22	MA_DQS_H5/MAB_DQS_H3
AV22	MA_DQS_L5/MAB_DQS_L3
AT20	MA_DQS_H6/MAB_DQS_H1
AR20	MA_DQS_L6/MAB_DQS_L1
AR18	MA_DQS_H7/MAB_DQS_H0
AT18	MA_DQS_L7/MAB_DQS_L0
Y26	RSVD_58
Y27	RSVD_59
AJ25	MA_CLK_H0/MAA_CKT
AJ24	MA_CLK_L0/MAA_CKC
AJ22	MA_CLK_H1/MAB_CKT
AJ21	MA_CLK_L1/MAB_CKC
AL25	MA_CS_L0/MAB_CA2
AM26	MA_CS_L1/MAB_CA5
AD24	MA_CKE0/MAA_CA1
AD25	MA_CKE1/MAA_CA0
AM24	MA_ODT0/MAB_CA3
AM27	MA_ODT1/MAB_CA4
AE24	MA_ALERT_L/TEST31A
AK23	MA_EVENT_L
AD27	MA_RESET_L

Pin	Signal
K27	MA_DATA0/MAA_DATA8
L26	MA_DATA1/MAA_DATA9
N26	MA_DATA2/MAA_DATA13
N27	MA_DATA3/MAA_DATA12
G27	MA_DATA4/MAA_DATA11
H27	MA_DATA5/MAA_DATA10
M27	MA_DATA6/MAA_DATA15
N24	MA_DATA7/MAA_DATA14
L23	MA_DATA8/MAA_DATA0
N21	MA_DATA9/MAA_DATA1
T21	MA_DATA10/MAA_DATA5
T22	MA_DATA11/MAA_DATA4
M22	MA_DATA12/MAA_DATA7
L24	MA_DATA13/MAA_DATA6
R21	MA_DATA14/MAA_DATA2
R23	MA_DATA15/MAA_DATA3
P24	MA_DATA16/MAA_DATA17
R26	MA_DATA17/MAA_DATA16
T27	MA_DATA18/MAA_DATA21
V27	MA_DATA19/MAA_DATA20
P25	MA_DATA20/MAA_DATA19
P27	MA_DATA21/MAA_DATA18
V23	MA_DATA22/MAA_DATA23
T25	MA_DATA23/MAA_DATA22
W22	MA_DATA24/MAA_DATA30
Y23	MA_DATA25/MAA_DATA31
AC24	MA_DATA26/MAA_DATA26
AC23	MA_DATA27/MAA_DATA27
V21	MA_DATA28/MAA_DATA28
W21	MA_DATA29/MAA_DATA29
AA24	MA_DATA30/MAA_DATA24
AA22	MA_DATA31/MAA_DATA25
AP26	MA_DATA32/MAB_DATA17
AN24	MA_DATA33/MAB_DATA16
AR25	MA_DATA34/MAB_DATA21
AU26	MA_DATA35/MAB_DATA20
AN25	MA_DATA36/MAB_DATA19
AN27	MA_DATA37/MAB_DATA18
AR27	MA_DATA38/MAB_DATA23
AU27	MA_DATA39/MAB_DATA22
AV25	MA_DATA40/MAB_DATA30
AW25	MA_DATA41/MAB_DATA31
AV20	MA_DATA42/MAB_DATA26
AW20	MA_DATA43/MAB_DATA27
AV27	MA_DATA44/MAB_DATA28
AW26	MA_DATA45/MAB_DATA29
AU21	MA_DATA46/MAB_DATA24
AW21	MA_DATA47/MAB_DATA25
AT22	MA_DATA48/MAB_DATA11
AP21	MA_DATA49/MAB_DATA10
AN19	MA_DATA50/MAB_DATA14
AN18	MA_DATA51/MAB_DATA15
AU23	MA_DATA52/MAB_DATA12
AR22	MA_DATA53/MAB_DATA13
AN20	MA_DATA54/MAB_DATA9
AP19	MA_DATA55/MAB_DATA8
AT19	MA_DATA56/MAB_DATA6
AW18	MA_DATA57/MAB_DATA7
AU16	MA_DATA58/MAB_DATA2
AW16	MA_DATA59/MAB_DATA3
AW19	MA_DATA60/MAB_DATA4
AU19	MA_DATA61/MAB_DATA5
AP16	MA_DATA62/MAB_DATA1
AT16	MA_DATA63/MAB_DATA0
W27	RSVD_54
W25	RSVD_53
AC26	RSVD_68
AC27	RSVD_69
V26	RSVD_49
V24	RSVD_48
AA27	RSVD_63
AA25	RSVD_62
AK24	MA_PAROUT/RSVD
AN21	M_DDR4
AN22	M_LPDDR4

TP501 1 MA_TEST

M_A_EVENT_N AK23
M_A_RESET_N AD27

FP6 REV 0.92
PART 1 OF 13

RENOIR-FP6-GP

ZZ.00CPU.421

1D1V_S3

Follow CRB 20200313

1D1V_S3

R501 1 1KR2J-1-GP M_A_EVENT_N

LV550 AMD

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR4_CHA)

Size: A3 | Document Number: LV550 AMD | Rev: -1

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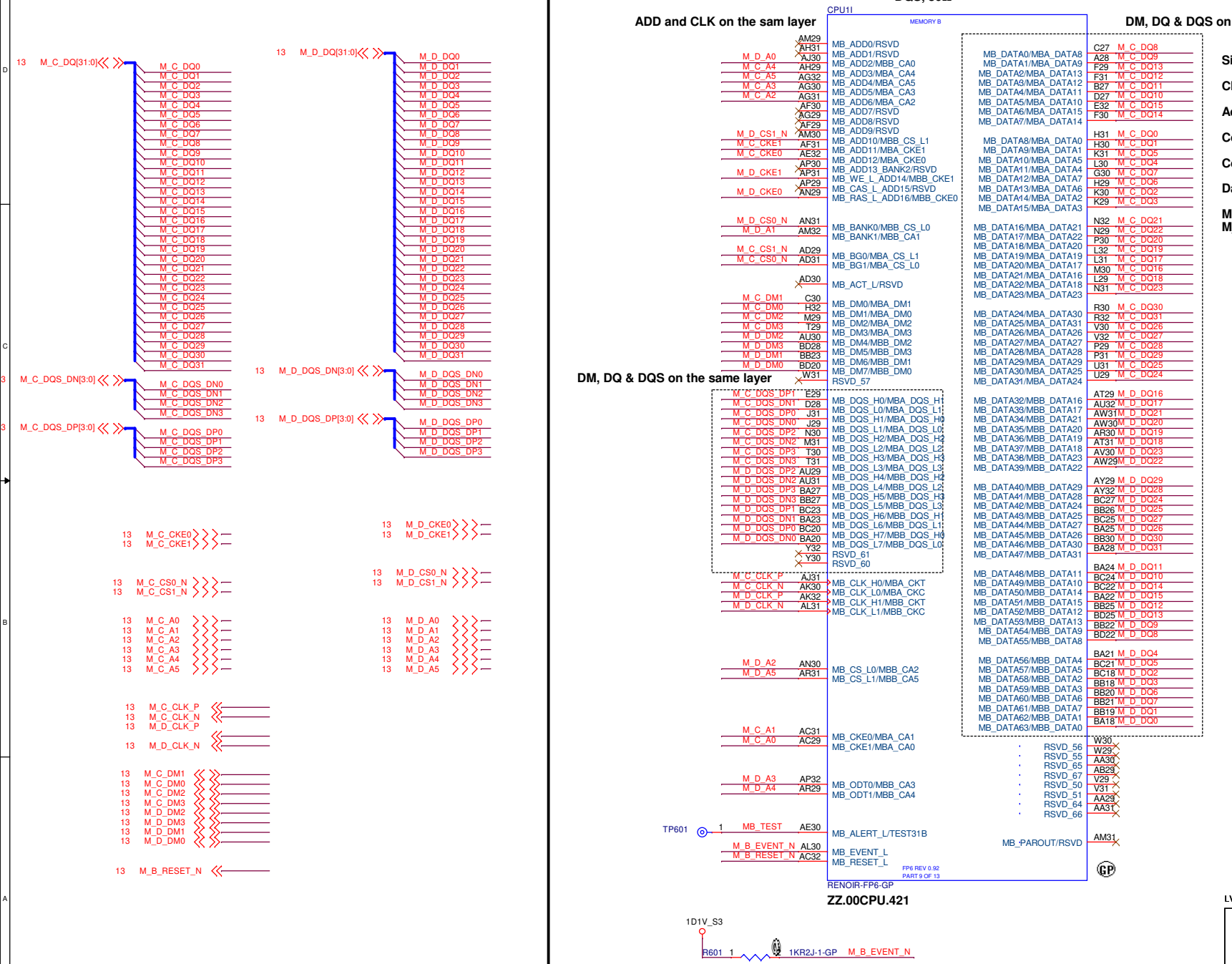
SSID = CPU

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer



ZZ.00CPU.421

Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc. M_PAROUT	M_RESET_L	M_EVENT_L	M_ALERT	

LV550 AMD

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR4_CHB)

Size: A3 | Document Number: LV550 AMD | Rev: -1

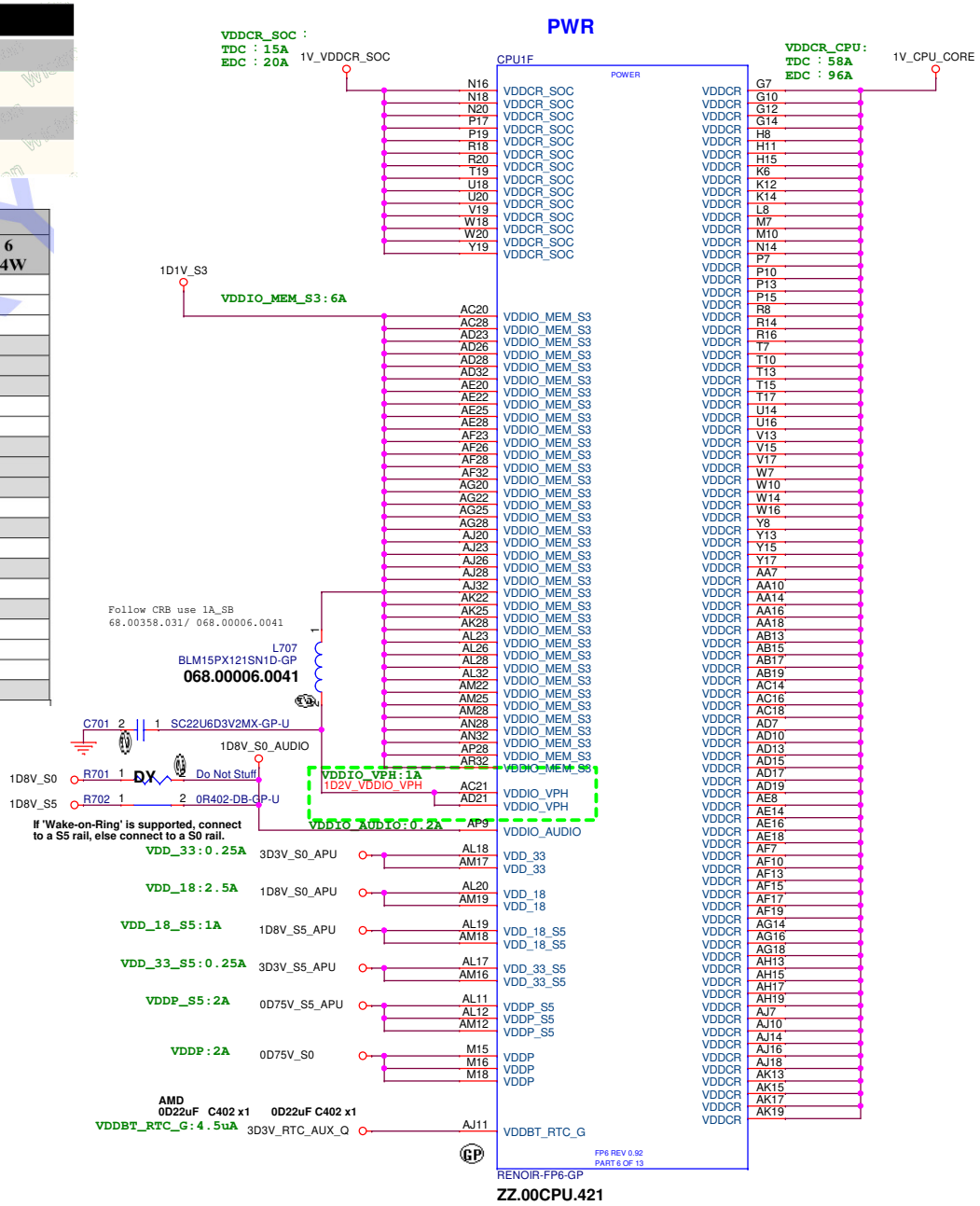
Date: Monday, August 17, 2020 | Sheet 6 of 106

SVI	FP4 – Bristol Ridge	FP5 – Raven Ridge
Supply 1	VDDCR_CPU – x86 Cores	VDDCR_VDD – x86 Cores, GPU
Supply 2	VDDCR_NB – Rest Of Chip	VDDCR_SOC – Rest Of Chip
Supply 3	VDDCR_GFX – GPU	N/A
Sum@15W	TDC: 56A, EDC: 87A	TDC: 45A, EDC: 58A

Table 5. FP6 Processor Voltage Supply Currents

Supply [1]	Nominal Voltage at Pkg Ball (V) [2]	Condition	SYSTEM_CONFIGURATION 1 10W	2 15W	3 25W	4 35W	5 45W	6 54W
VDDCR_VDD	Variable (0.65–TBD)[5]	TDC [3]	20	33	44	51	58	
		EDC	34	50	70	90	96	
		Max Loadstep [4]	29	43	65	76	84	
VDDCR_SOC	Variable (0.7–TBD)[5]	TDC [3]	10	13		15		
		EDC	13	17		20		
		Max Loadstep [4]						
VDDIO_MEM_S3[6]	1.10	TDC	6.00					
	1.20	TDC	6.00					
VDDIO_VPH[7]	1.10	TDC	1.00					
	1.20	TDC	1.00					
	1.80	TDC	1.00					
VDDP	0.75	TDC	2.00					
VDDP_S5	0.75	TDC	2.00					
VDD_18	1.80	TDC	2.50					
VDD_18_S5	1.80	TDC	1.00					
VDD_33	3.30	TDC	0.25					
VDD_33_S5	3.30	TDC	0.25					
VDDIO_AUDIO	1.20	TDC	0.20					
	1.50	TDC	0.20					
	1.80	TDC	0.20					
VDDBT_RTC_G	3.00	TDC	4.5µA					

WINARY



15.3.5 VDDIO _ VPH Power Delivery and Decoupling
VDDIO _ VPH is the dedicated supply voltage for DisplayPort 0 and PCIe phys . When DisplayPort 0 is used for eDP , the source of VDDIO _ VPH can be the same source as VDDIO _ MEM _ S 3. This allows lower power and better battery life . When DisplayPort 0 is used for DP or TMDS , the source of VDDIO _ VPH can be the same source as VDD _18.

LV550 AMD

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SSID = PCH

DISPLAY/SVI/JTAG/TEST

APU Type I(CZ): 1D8V
APU Type II(CZ-L): 3D3V

APU Type I 1D8V
APU Type II 3D3V

PINOUT	Description
DP_BLON	BL_ENABLE
DP_DIGON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM

DisplayPort	Device
0	eDP
1	HDMI
2	TYPE-C
3	

eDP

55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N3
24 PANEL_BLEN
55 EDP_VDD_EN
55 PANEL_BKLTCTL
55 EDP_AUX_CPU_P
55 EDP_AUX_CPU_N
55 EDP_HPD_CPU

HDMI

57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_HPD_CPU

71 USB3_TCSS_AUX_P
71 USB3_TCSS_AUX_N
71,72 TYPEC_HPD_CPU

HDT

68 APU_TDI
68 APU_TDO
68 APU_TCK
68 APU_TMS
68 APU_TRST_N
68 APU_DBREQ_N

68,72 RST_N_CPU
46,68 PWR_SVID_PWRGD

24,44,46 PROCHOT_N_CPU

SVID

46 SVID_CLK_CPU
46 SVID_DATA_CPU
46 SVID_ALERT_CPU_N

46 VDDNB_SENSE
46 VCCCORE_SENSE

46 VSSCORE_SENSE

52 VDDP_S5_SENSE
52 VDDP_S0_SENSE

51 VDDIO_MEM_S3_SENSE

24 CPU_SMB_SDA_EC
24 CPU_SMB_SCL_EC

1D8V_S5 RN803 SRN4K7J-8-GP
RST_N_CPU
PWR_SVID_PWRGD

HDT EVT stage要上

1D8V_S5 HDT PIN Pull High Resistor
ASM if HDT CONN is needs of use
RN804 SRN1KJ-4-GP HDT
APU_TDI
APU_TCK
APU_TRST_N
APU_DBREQ_N
R805 1KR2J-1-GP HDT
APU_TMS

3D3V_S0
RN801 SRN1KJ-7-GP
PROCHOT_N_CPU
ALERT_N_CPU
RN802 SRN1KJ-7-GP
SIC_CPU
SID_CPU
R803 1KR2J-1-GP
THERMTRIP_N_CPU

C821 DY Do Not Stuff RST_N_CPU
C822 DY Do Not Stuff PWR_SVID_PWRGD

1D8V_S0
RN805 DY
SIC_CPU
SID_CPU
Do Not Stuff

RN801 change to 4 pin from 8 pin & add RN802
Add RN803 RSVD SIC/ SID 1D8V_S0 signal
Reserve 1.8v pull up at SIC & SID of CPU (Right now pull up 3.3v)_-1

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

CPU1C
DISPLAY/SVI2/JTAG/TEST

eDP_TX_CPU_P0 D11 DP0_TXP0
eDP_TX_CPU_N0 B11 DP0_TXN0
eDP_TX_CPU_P1 C11 DP0_TXP1
eDP_TX_CPU_N1 A11 DP0_TXN1
eDP_TX_CPU_P2 D10 DP0_TXP2
eDP_TX_CPU_N2 B10 DP0_TXN2
eDP_TX_CPU_P3 D9 DP0_TXP3
eDP_TX_CPU_N3 B9 DP0_TXN3
HDMI_DDI_TX_P0 G23 DP1_TXP0
HDMI_DDI_TX_N0 H23 DP1_TXN0
HDMI_DDI_TX_P1 F22 DP1_TXP1
HDMI_DDI_TX_N1 G22 DP1_TXN1
HDMI_DDI_TX_P2 G21 DP1_TXP2
HDMI_DDI_TX_N2 H21 DP1_TXN2
HDMI_DDI_TX_P3 F20 DP1_TXP3
HDMI_DDI_TX_N3 G20 DP1_TXN3

DP_BLON A22 PANEL_BLEN
DP_DIGON D23 EDP_VDD_EN
DP_VARY_BL C23 PANEL_BKLTCTL
DP0_AUXP D12 EDP_AUX_CPU_P
DP0_AUXN B12 EDP_AUX_CPU_N
DP0_HPD C12 EDP_HPD_CPU
DP1_AUXP J20 HDMI_SCL_CPU
DP1_AUXN K20 HDMI_SDA_CPU
DP1_HPD L21 HDMI_HPD_CPU
DP2_AUXP L19 USB3_TCSS_AUX_P
DP2_AUXN M19 USB3_TCSS_AUX_N
DP2_HPD M20 TYPEC_HPD_CPU
DP3_AUXP M14
DP3_AUXN L14
DP3_HPD L16
DP_STEREOSYNC B23 DP_STEREOSYNC_APU

eDP R840 10KR2F-2-GP R841 10KR2F-2-GP
HDMI
TYPEC USB3

TEST4 BB6 TEST4 TP808
TEST5 BD5 TEST5 TP807
TEST6 AG12
TEST14 G25 TEST14_APU TP810
TEST15 K25 TEST15_APU TP811
TEST16 F25 TEST16_APU TP812
TEST17 F26 TEST17_APU TP813
TEST31 H26 TEST31_APU TP802
TEST41 AK9 TEST41 TP809
ANALOGIO_0 AK21
ANALOGIO_1 AG21

HDT
APU_TDI AP3 TDI
APU_TDO AU1 TDO
APU_TCK AR2 TCK
APU_TMS AU3 TMS
APU_TRST_N AR4 TRST_L
APU_DBREQ_N AT2 DBREQ_L
HDT CONN PIN#12 RST_N_CPU AW3 RESET#
HDT CONN PIN#10 PWR_SVID_PWRGD AW4 PWROK
SIC_CPU B22 SIC
SID_CPU D22 SID
ALERT_N_CPU C22 ALERT_L
THERMTRIP_N_CPU AN9 THERMTRIP_L
PROCHOT_N_CPU B25 PROCHOT_L
an output signal as overtemperature condition

3D3V

SVID
SVID_CLK_CPU D25 SVC0
SVID_DATA_CPU C25 SVD0
SVID_ALERT_CPU_N A25 SVT0

FP6 REV 0.92
PART 3 OF 13
RENOIR-FP6-GP
ZZ.00CPU.421

0D75V_S0
SMU_ZVDD P3 SMU_ZVDD R812 196R2F-GP
VDDP_S5_SENSE AK7 VDDP_S5_SENSE_APU R815 0R2-PT5-LILY-GP VDDP_S5_SENSE
VDDP_SENSE AK12 VDDP_S0_SENSE_APU R816 0R2-PT5-LILY-GP VDDP_S0_SENSE
VDDCR_SOC_SENSE J23 VDDNB_SENSE_APU R806 0R2-PT5-LILY-GP VDDNB_SENSE
VDDCR_SENSE K22 VCCCORE_SENSE_APU R807 0R2-PT5-LILY-GP VCCCORE_SENSE
VDDIO_MEM_S3_SENSE J21 VDDIO_MEM_S3_SENSE TP814
VSS_SENSE_A J22 VSS_SENSE_APU R809 0R2-PT5-LILY-GP VSSCORE_SENSE
VSS_SENSE_B AJ12 VSS_SENSEB TP801

DY C879 Do Not Stuff
DY C889 Do Not Stuff
C890 SC2750V2JN-2-GP
if SI is not ok, suggest that install capacitor.
C890 ASM
for SVID Signal Quality test
Alert noise over spec 200mv_SC

VDDNB_SENSE R801 DY Do Not Stuff 1V_VDDCR_SOC
VCCCORE_SENSE R802 DY Do Not Stuff 1V_CPU_CORE
VSSCORE_SENSE R804 DY Do Not Stuff
VSS_SENSEB R817 DY Do Not Stuff

Check list: PD/CRB:PH

1D8V_S0 R837 1KR2F-L1-GP
DP_STEREOSYNC_APU
R808 DY Do Not Stuff

1D8V_S0 R810 DY Do Not Stuff
3D3V_S0 R811 0R2J-2-GP
3D3V_S0_SIC_SID
Q808 2N7002KDW-1-GP
SID_CPU CPU_SMB_SDA_EC
SIC_CPU CPU_SMB_SCL_EC

75.27002.F7C

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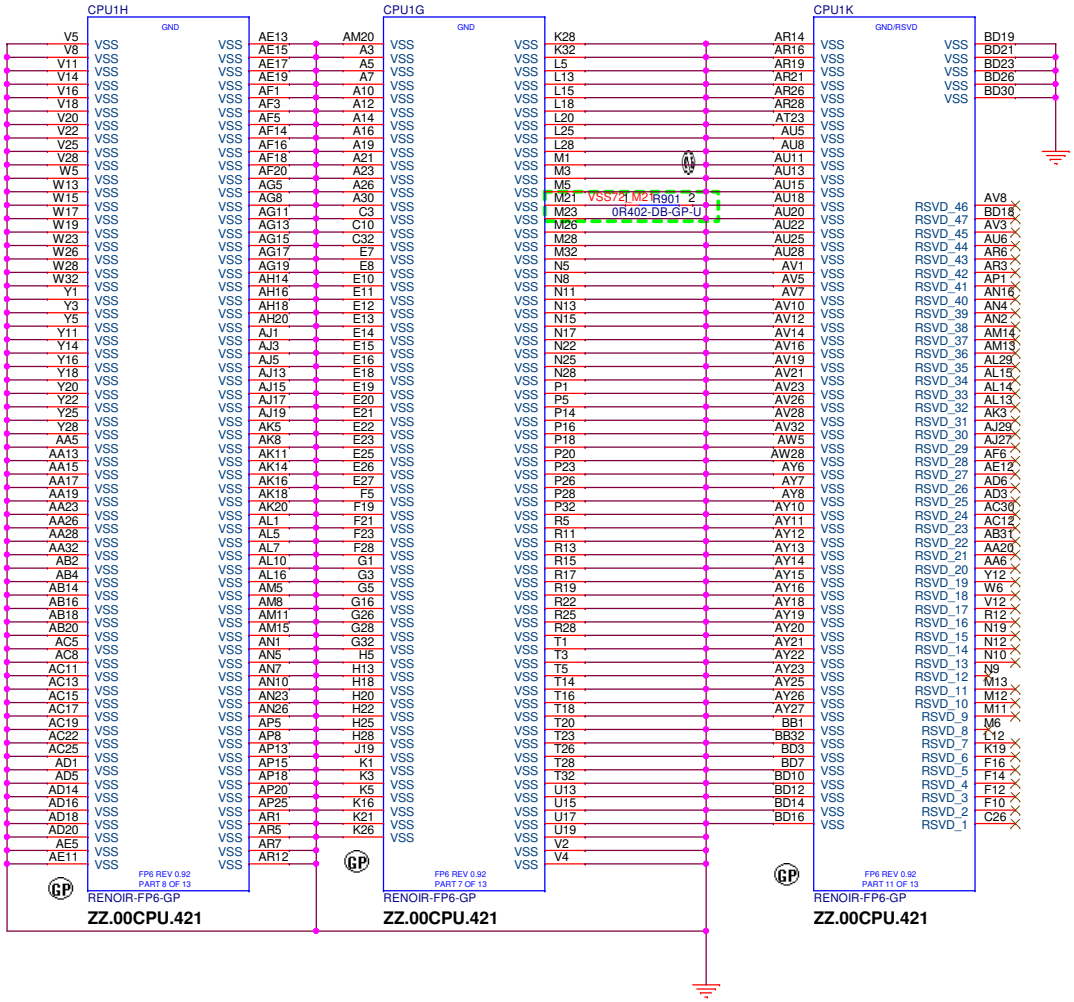
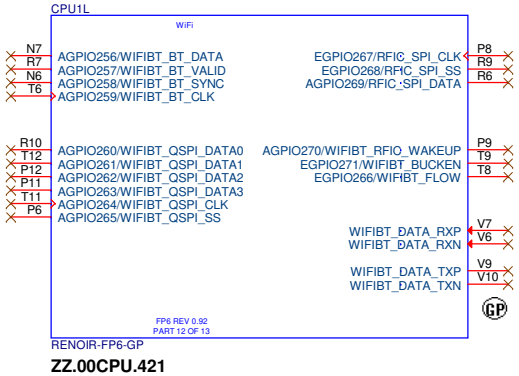
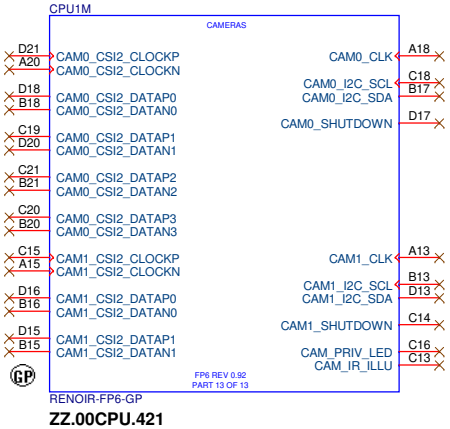
VSS







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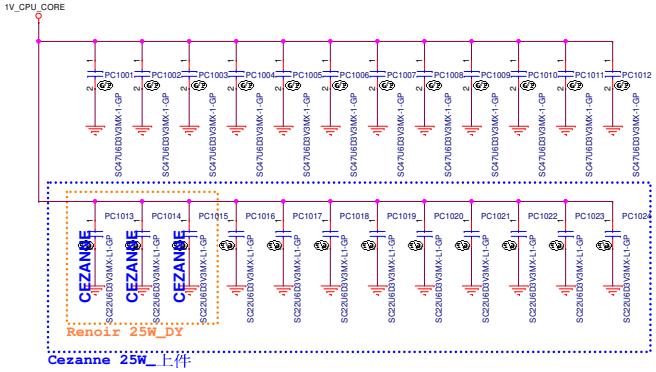
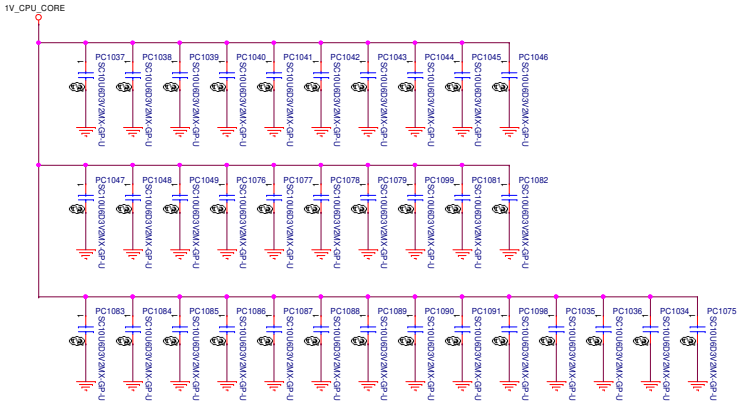
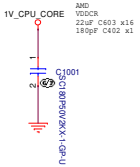
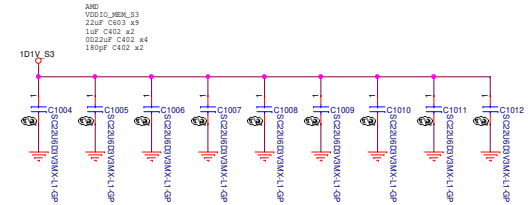
Main Func = CPU

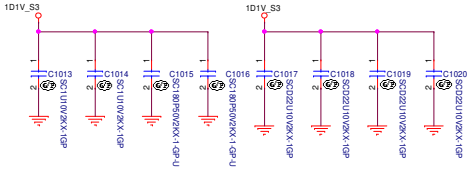
1V_VDDCORE AMD_FP6_25W



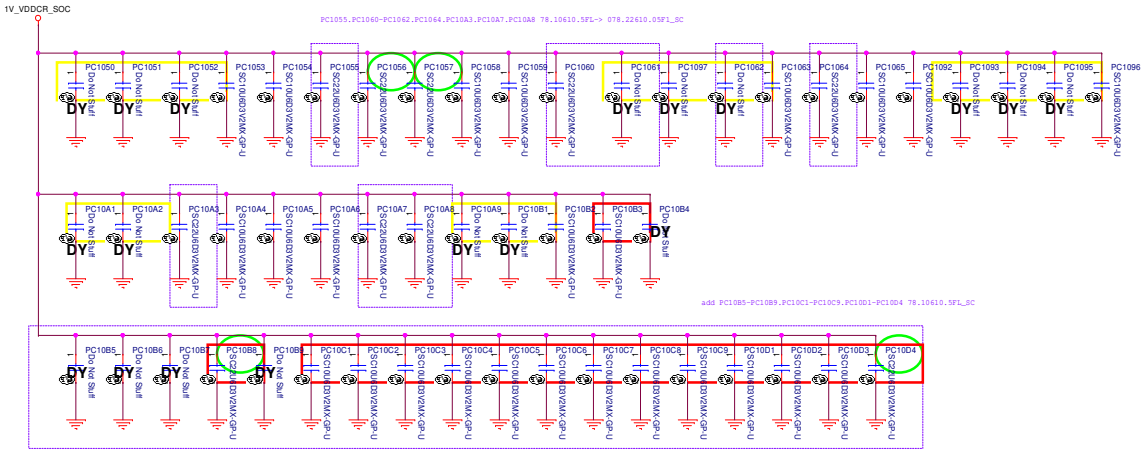


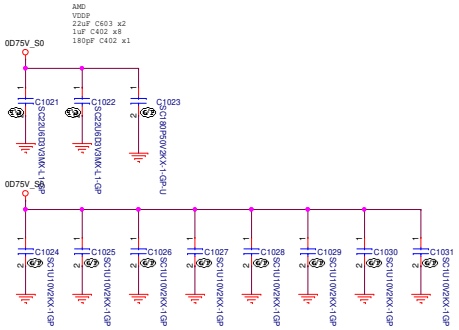


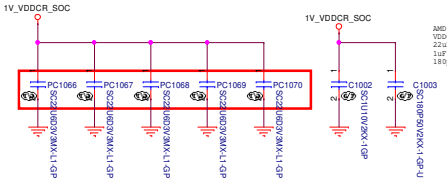


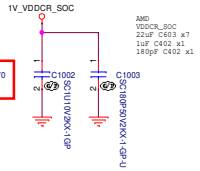


1V_VDDCR_SOC









RED:ASM
YELLOW:DY
GREEN:PC1088 · PC10D4 · PC1056 · PC1057換成 078.22610.05F1 (22uF/0402)
20200629_SC

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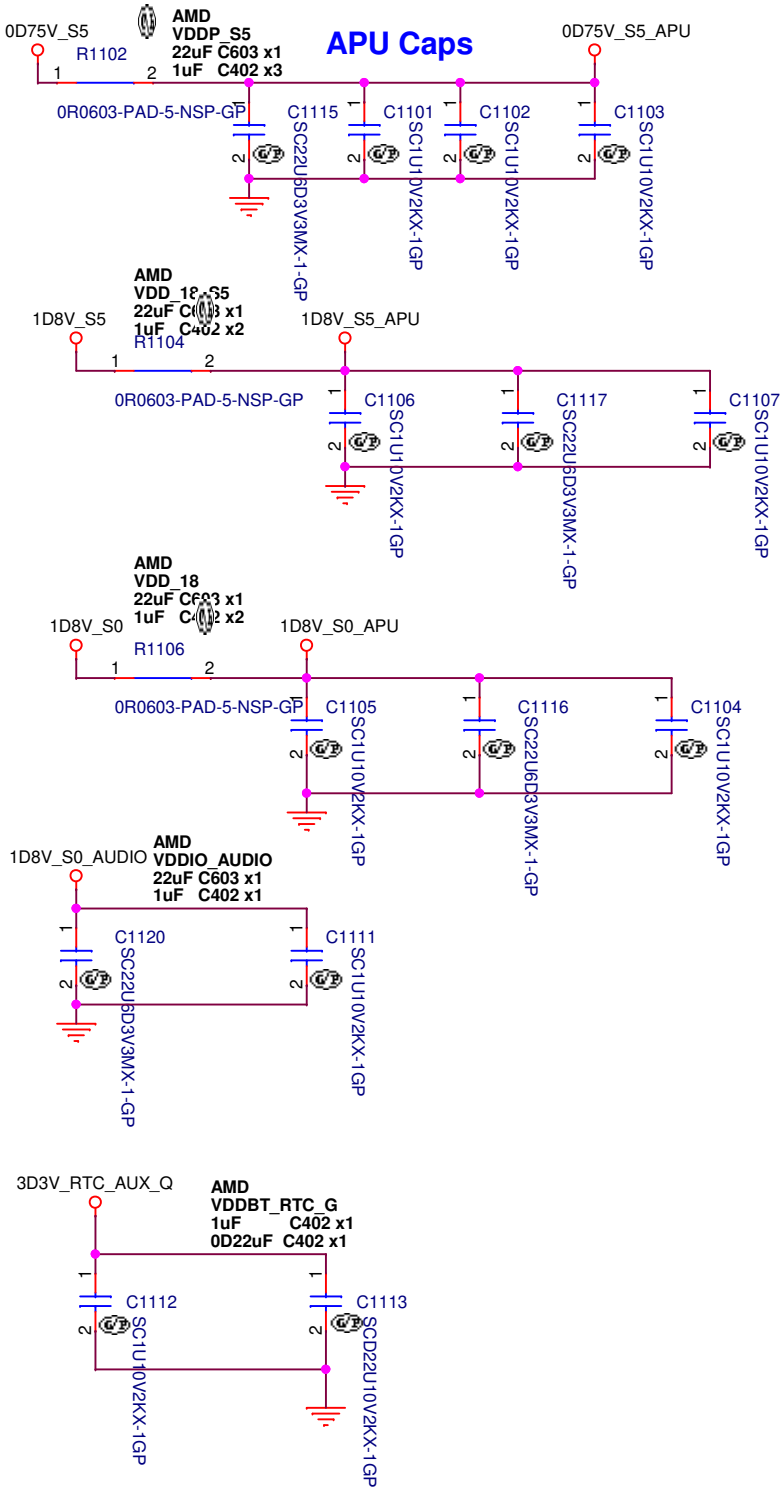

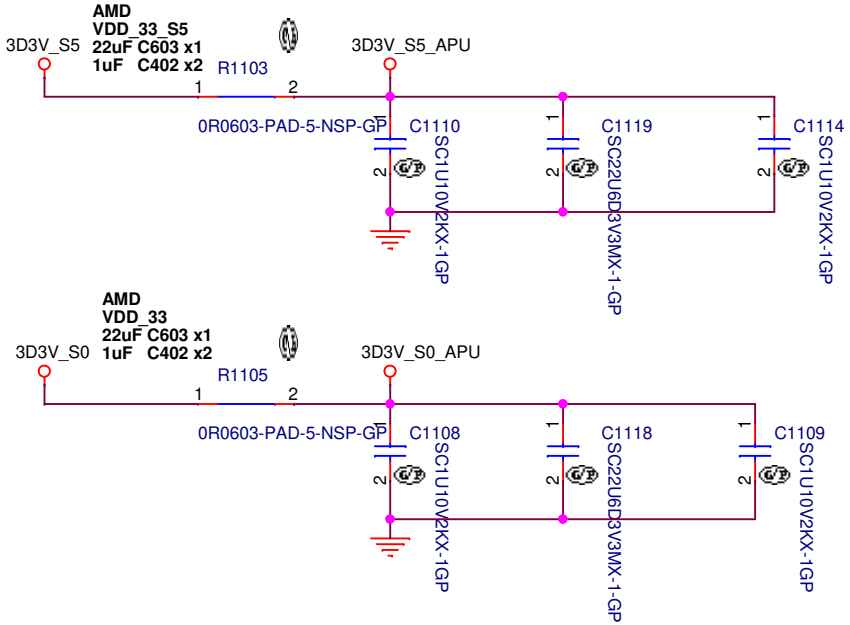

Table 110. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S3[1, 2]	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 µF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 µF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 µF	0402 X5R	-	-	4(split)	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2(split)	1BU	-	-	-	-	-	-	-

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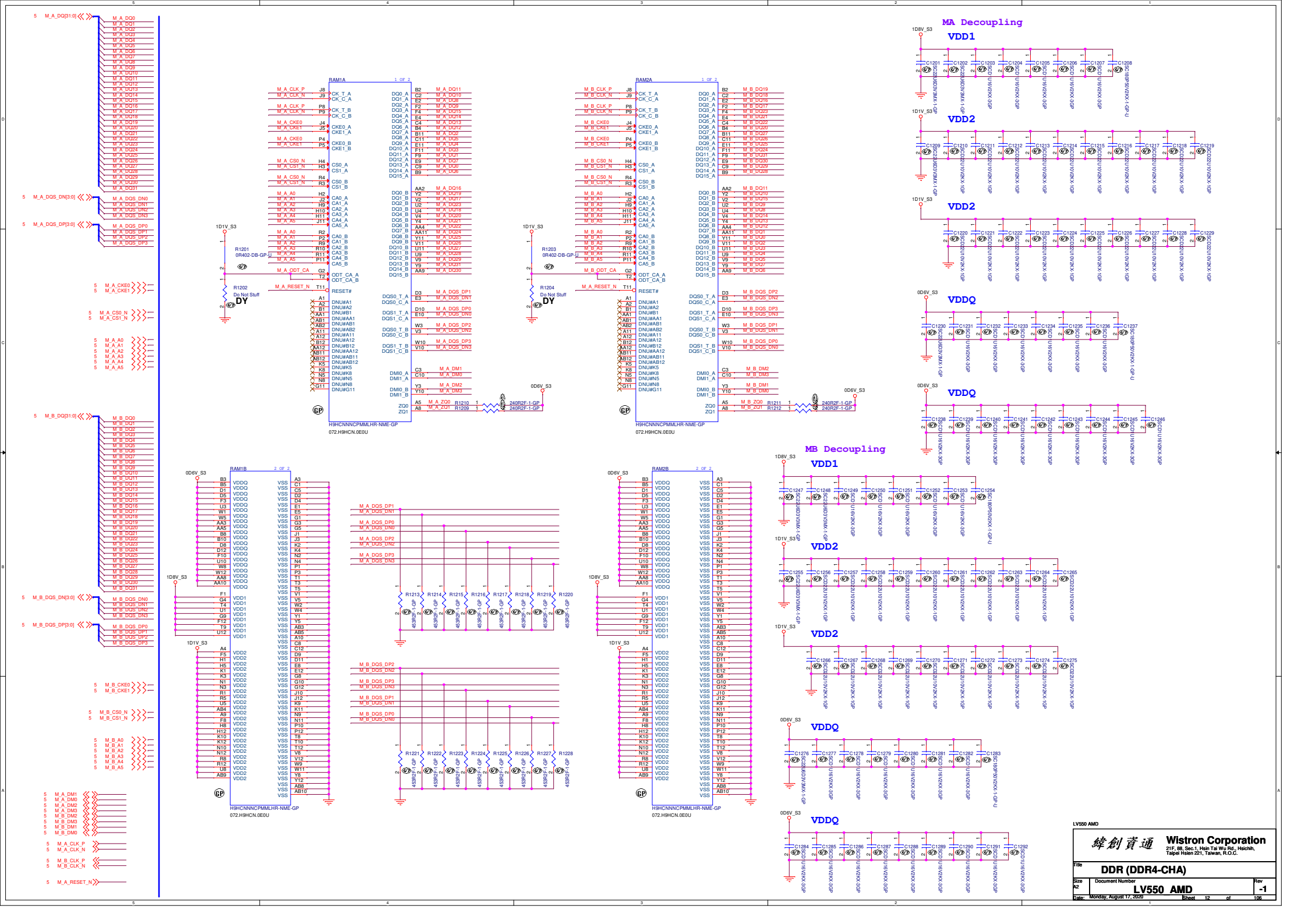
MA Decoupling
VDD1
VDD2
VDDQ
MB Decoupling
RAM1A
RAM1B
RAM2A
RAM2B
H9HCNNNCPMMLHR-NME-GP
072.H9HCN.0E0U
DY
Do Not Stuff
LV550 AMD
Wistron Corporation
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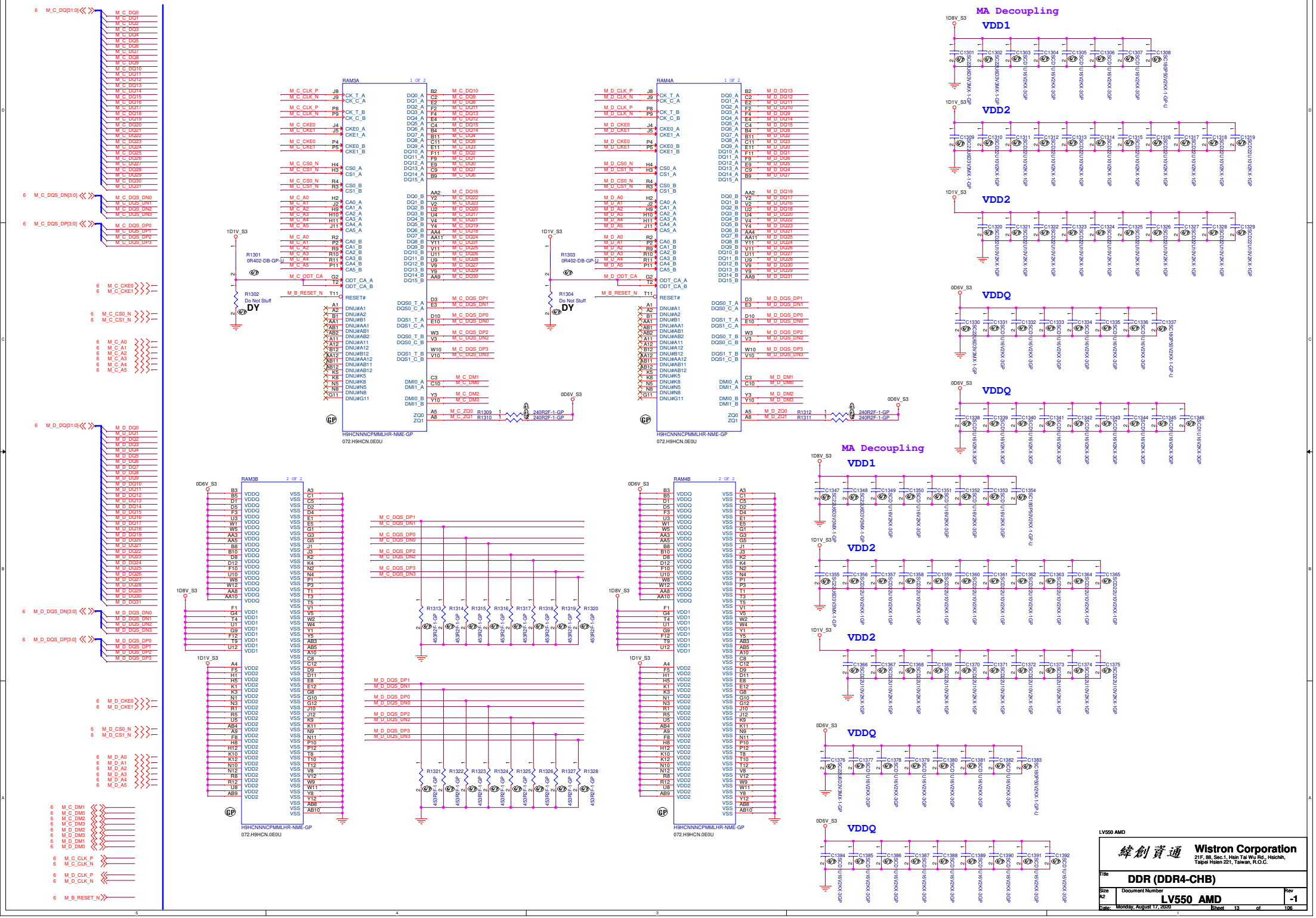
RAM3A
RAM4A
RAM3B
RAM4B
H9HCNNNCPMMLHR-NME-GP
072.H9HCN.0E0U
MA Decoupling
VDD1
VDD2
VDDQ
R1301 0R402-DB-GP-U
R1302 Do Not Stuff
R1303 0R402-DB-GP-U
R1304 Do Not Stuff
DY
240R2F-1-GP
453R2F-1-GP
1D8V_S3
1D1V_S3
0D6V_S3
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Title: DDR (RSVD)

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SSD

63	SSD_CLK_CPU_P	
63	SSD_CLK_CPU_N	
63	SSD_CLKREQ_CPU_N	

WLAN

61	WLAN_CLK_CPU_P	
61	WLAN_CLK_CPU_N	
61	WLAN_CLKREQ_CPU_N	

SPI

20,25	SPI_CLK_ROM	
25	SPI_SO_ROM	
25	SPI_SI_ROM	
25	SPI_WP_ROM	
25	SPI_HOLD_ROM	
25	SPI_CS_ROM_N0	

LPC

24	ECSMI_N_KBC	
24,68	LPC_AD_CPU_P0	
24,68	LPC_AD_CPU_P1	
24,68	LPC_AD_CPU_P2	
24,68	LPC_AD_CPU_P3	
24	LPC_CLK_KBC	
68	LPC_CLK_DBG	
24,68	LPC_SERIRQ_CPU	
24,68	LPC_FRAME_N_CPU	
24,68,91	LPC_RST_N	

24	CLK_RUN_N	
91	PIRQA_N	
24	ECSCI_N_KBC	
24	KBRST_N	
61	SUS_CLK_CPU	
91	SPI_CS_CPU_N2	
91	SPI_CLK_CPU	
91	SPI_SI_CPU	
91	SPI_SO_CPU	
68	EC_SMI_APU	
68	EGPIO141	
68	EGPIO143	

CLK/SATA/USB/SPI/LPC

P_GPP CLK port	AMD	Device
0	GFX	NC
1	LAN	NC
2	WWAN	NC
3	PCIETBT	NC
4	PCIEDT	CARD
5	SSD	SSD
6	WLAN	WLAN

LPCCLK1/EGPIO75
CLK_REQ5_L
If unused,
enable internal pull up or pull down by software.

GFX & GPP CLK, 85Ω
SATA & USB, 90Ω

CPU1E

CLK/LPC/EMMC/SD/SPI/eSPI/UART

AR13	CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92	
AP10	CLK_REQ1_L/AGPIO115	
AH15	CLK_REQ2_L/AGPIO116	
AT14	CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131	
AN11	CLK_REQ4_L/OSCIN/EGPIO132	SSD_CLKREQ_CPU_N
AN13	CLK_REQ5_L/EGPIO120	WLAN_CLKREQ_CPU_N
AN15	CLK_REQ6_L/EGPIO121	
AF11	GPP_CLK0P	
AF12	GPP_CLK0N	
AG4	GPP_CLK1P	
AG2	GPP_CLK1N	
AG3	GPP_CLK2P	
AG1	GPP_CLK2N	
AF2	GPP_CLK3P	
AF4	GPP_CLK3N	
AH2	GPP_CLK4P	
AH4	GPP_CLK4N	
AJ2	GPP_CLK5P	SSD_CLK_CPU_P
AJ4	GPP_CLK5N	SSD_CLK_CPU_N
AF8	GPP_CLK6P/WIFIBT_CLKP	WLAN_CLK_CPU_P
AF9	GPP_CLK6N/WIFIBT_CLKN	WLAN_CLK_CPU_N
AK1	X48M_OSC	
BB3	X48M_X1	XTL_48M_X1_CPU
BA5	X48M_X2	XTL_48M_X2_CPU
AG10	RSVD_71	RSVD_71
AG9	RSVD_70	RSVD_70
AW10	RTCCLK	SUS_CLK_CPU
AY1	X32K_X1	XTL_32K_X1_CPU
AY4	X32K_X2	XTL_32K_X2_CPU

FP6 REV 0.92
PART 5 OF 13

RENOIR-FP6-GP

AW14	EGPIO70	
BB13	LPC_PD_L/AGPIO21	EC_SMI_APU
BA16	LAD0/ESPI1_DATA0/EGPIO104	LPC_AD_CPU_P0_R
BA15	LAD1/ESPI1_DATA1/EGPIO105	LPC_AD_CPU_P1_R
BC13	LAD2/ESPI1_DATA2/EGPIO106	LPC_AD_CPU_P2_R
BB14	LAD3/ESPI1_DATA3/EGPIO107	LPC_AD_CPU_P3_R
BB15	LPCCLK0/EGPIO74	LPC_CLK_CPU_P0
BD13	LPC_CLKRUN_L/AGPIO88	LPC_CLKRUN_N
BA12	LPCCLK1/EGPIO75	LPC_CLK_CPU_P1
BC15	SERIRQ/AGPIO87	
BA13	LFRAME_L/EGPIO109	
BC12	LPC_RST_L/AGPIO32	RST_N_APU
AU12	AGPIO68	
AP4	LPC_PME_L/AGPIO22	ECSCI_N_KBC
BA11	SPI_ROM_REQ/EGPIO67	EGPIO67
BB11	SPI_ROM_GNT/EGPIO76	EGPIO76
AT15	ESPI_RESET_L/KBRST_L/AGPIO129	KBRST_N
BC11	ESPI_ALERT_L/LDRQ0_L/EGPIO108	LDRQ0_N
BC10	SPI_CLK/ESPI_CLK	SPI_CLK_CPU
BA10	SPI_DI/ESPI_DATA	SPI_SO_CPU
BB8	SPI_DO	SPI_SI_CPU
BA9	SPI_WP_L/ESPI_DAT2	SPI_WP_CPU
BC8	SPI_HOLD_L/ESPI_DAT3	SPI_HOLD_CPU
BD11	SPI_CS1_L	SPI_CS_CPU_N0
BC9	SPI_CS2_L/ESPI_CS_L/AGPIO30	
BB10	SPI_CS3_L/AGPIO31	
BD8	SPI_TPM_CS_L/AGPIO29	SPI_CS_CPU_N2
BA17	EGPIO141/UART0_RXD	EGPIO141
BC16	EGPIO143/UART0_TXD	EGPIO143
BD15	EGPIO142/UART0_RTS_L/UART1_RXD	EGPIO142
BC17	EGPIO140/UART0_CTS_L/UART1_TXD	EGPIO140
BB16	AGPIO144/SHUTDOWN_L/UART0_INTR	

3D3V_S0

ECSMI_N_KBC	R1606	1	DY	2	Do Not Stuff
LPC_CLKRUN_N	R1651	1	DY	2	Do Not Stuff
	R1652	1		2	0R0201-PAD-2-GP
EC_SMI_APU	R1602	1		2	0R0201-PAD-2-GP
LPC_AD_CPU_P0_R	R1626	1		2	10R1J-GP
LPC_AD_CPU_P1_R	R1627	1		2	10R1J-GP
LPC_AD_CPU_P2_R	R1628	1		2	10R1J-GP
LPC_AD_CPU_P3_R	R1629	1		2	10R1J-GP
LPC_CLK_CPU_P0	R1608	1		2	22R1J-GP
LPC_CLK_CPU_P1	R1609	1		2	22R1J-GP
RST_N_APU	R1612	1		2	33R1J-GP
ECSCI_N_KBC	WIFI_RF_EN	24,61			
EGPIO67	TPAD14-OP-GP	TP1605			
EGPIO76	TPAD14-OP-GP	TP1606			
SPI_CLK_CPU	R1611	1		2	33R1J-GP
SPI_SO_CPU	R1613	1		2	33R1J-GP
SPI_SI_CPU	R1614	1		2	0R0201-PAD-2-GP
SPI_WP_CPU	R1621	1		2	0R0201-PAD-2-GP
SPI_HOLD_CPU	R1622	1		2	0R0201-PAD-2-GP
SPI_CS_CPU_N0	R1607	1		2	0R0201-PAD-2-GP
EGPIO141	TPAD14-OP-GP	TP1601			
EGPIO143	TPAD14-OP-GP	TP1602			
EGPIO142	TPAD14-OP-GP	TP1603			
EGPIO140	TPAD14-OP-GP	TP1604			

to KBC

DB_170410
Follow BIOS request for AMD
LPC interface debug

change TPM CS# pin from SPI_CS2_L/ESPI_CS_L/AGPIO30 to SPI_TPM_CS_L/AGPIO29
follow CRB_SC

3D3V_S0

RN1601	1	4	SRN10KJ-5-GP	SSD_CLKREQ_CPU_N	
	2	3		WLAN_CLKREQ_CPU_N	
R1620	1		10KR2J-3-GP	LDRQ0_N	

1D8V_S5

R1605	1	DY	2	Do Not Stuff	SUS_CLK_CPU
R1632	1	DY	2	Do Not Stuff	SPI_SI_ROM

Follow FP6 CL 20190424

R1635	1		2	0R2-PT5-LILY-GP	RSVD_71
R1636	1		2	0R2-PT5-LILY-GP	RSVD_70
C1603	1		2	SC150P50V2JN-3GP	LPC_RST_N
EC1614	1	DY	2	Do Not Stuff	LPC_CLK_KBC
EC1615	1	DY	2	Do Not Stuff	LPC_CLK_DBG
C1616	1	DY	2	Do Not Stuff	LPC_SERIRQ_CPU

R1648	1	DY	2	Do Not Stuff	
SPI_CLK_ROM_R	S				
5V_S0	G		D	SPI_CLK_ROM	

Q1601
2N7002K-2-GP-U
84.2N702.J31

XTL_32K_X1_CPU	R1649	1	2	XTL_32K_X1	33R2J-L1-GP
XTL_32K_X2_CPU	R1650	1	2	XTL_32K_X2	33R2J-L1-GP
R1615	1		2	20MR2J-GP	

X1602
XTAL-32D768KHZ-98-GP
082.30003.0301

C1601 SC15P50V2JN-2-GP
C1602 SC15P50V2JN-2-GP

78.15034.1FLLL is common part, but not in stock

Note:
Connected to 48-MHz Fundamental XTAL (±10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X2.
Connected to 48-MHz Fundamental XTAL (±10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X1.

XTL_48M_X1_CPU	R1623	1	2	XTL_48M_X1	33R2J-L1-GP
R1618	1MR2F-GP				
XTL_48M_X2_CPU	R1624	1	2	XTL_48M_X2	33R2J-L1-GP

X1601
XTAL-48MHZ-101-GP
082.30028.0491

C1612	1		2	SC10P50V2JN-4GP	
C1613	1		2	SC10P50V2JN-4GP	

082.30028.0511

		C1601	C1602	
V	SEIKO 082.30003.0301	15pF	15pF	4ZA.0M501.0001
	EPSON 082.30003.0191	15pF	15pF	4ZA.0M501.0002
V 無交期	NDK 082.30003.0221	15pF	15pF	4ZA.0M501.0003
無交期	TXC 082.30003.0231	15pF	15pF	4ZA.0M501.0004
	TAITIEN 082.30003.0A11	12pF	12pF	4ZA.0M501.0005

HARMONY
82.30026.371->
HOSONIC
082.30028.0491
Need 10ppm

	C1612	C1613
HOSONIC 082.30028.0491 E3FB48E00000VE	10pF	10pF
HOSONIC 082.30028.0511 E3SB48E00000GE		

LV550 AMD

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **FCH (CLK/LPC/SPI/EMMC/SD/UA)**

Size: A3 | Document Number: **LV550 AMD** | Rev: -1

Date: Monday, August 17, 2020 | Sheet 16 of 106

SSID = PCH

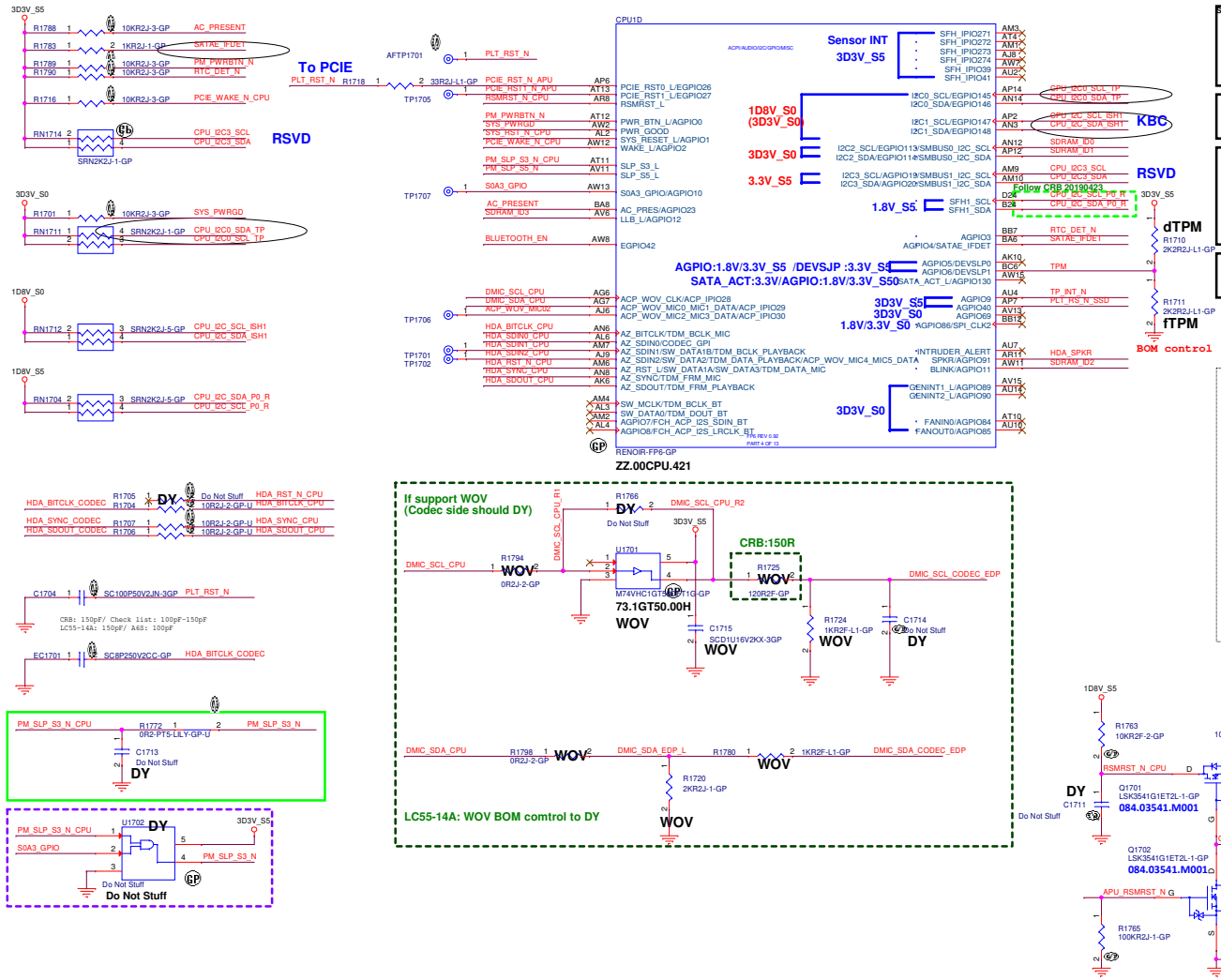
CLK/SATA/USB/SPI/LPC

Touch Pad

65	CPU_I2C0_SCL_TP_R
65	CPU_I2C0_SDA_TP_R

HDA

27	HDA_SDIN0_CPU
27	HDA_BITCLK_CODEC
27	HDA_SYNC_CODEC
27	HDA_SDOUT_CODEC
40	3V_5V_PWRGD
61	PCIE_WAKE_N_CPU
24,40,51,71	PM_SLP_S5_N
24,40,51,52,57	PM_SLP_S3_N
61,63,68,91	PLT_RST_N
24	PM_PWRBTN_N
24,40	SYS_PWRGD
20	SYS_RST_N_CPU
24	AC_PRESENT
24,65	TP_INT_N
25	RTC_DET_N
27	HDA_SPKR
24,61	BLUETOOTH_EN
63	PLT_RS_N_SSD
66	DMIC_SDA_CODEC_EDP
66	DMIC_SCL_CODEC_EDP



INTERNAL DEBUG PURPOSE ONLY

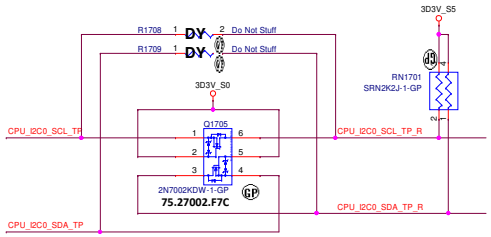
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

EVT/FVT/SIT/SVT:

Memory Configuration	Memory Supplier
00: (Reserve) 01: 8GB 10: 16GB 11: (Reserve)	00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)

AGPIO12	AGPIO11	EGPIO114	EGPIO113		072.H9HCN.0E0U						
SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Memory ID	Supplier	Density	PN	EVT	FVT 13'	FVT 14'	
X	X	0	0	0	SAMSUNG	4GB	SM30N76677	SKU1	SKU2.3.4	SKU1.3	3200
0	1	0	0	1	SAMSUNG	8GB	SM30N76677				10*15 mm
1	0	0	0	2	SAMSUNG	16GB	SM30N76678				10*15 mm
1	1	0	0	3	SAMSUNG						
X	X	0	1	4	MICRON	4GB	SM30N76681	SKU1	SKU2.3.4	SKU1.3	3200
0	1	0	1	5	MICRON	8GB	SM30E51328				10*14.5 mm
1	0	0	1	6	MICRON	16GB	SM30N76681		SKU2.3.4	SKU1.3	10*14.5 mm
1	1	0	1	7	MICRON						
X	X	1	0	8	SK HYNIX	4GB	SM30N76602	SKU1	SKU2.3.4	SKU1.3	3200
0	1	1	0	9	SK HYNIX	8GB	SM30N76602	SKU1			10*15 mm
1	0	1	0	10	SK HYNIX	16GB	SM30N76603	SKU3.4	SKU1	SKU2	10*15 mm
1	1	1	0	11	SK HYNIX						

0=L, 1=H



LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (AZ/I2C/GPIO/RTC/SMBS/M)

Size: A2 | Document Number: LV550 AMD | Rev: -1

Date: Monday, August 17, 2020 | Sheet 17 of 106

Main Func = USB

USB3.0 Port1

66 USB1_USB30_RX_N
66 USB1_USB30_RX_P
66 USB1_USB30_TX_N
66 USB1_USB30_TX_P

36 USB1_USB20_N
36 USB1_USB20_P

USB3.0 Port2

66 USB2_USB30_RX_N
66 USB2_USB30_RX_P
66 USB2_USB30_TX_N
66 USB2_USB30_TX_P

66 USB2_USB20_N
66 USB2_USB20_P

Finger Printer

66 FP_USB20_N
66 FP_USB20_P

IR Camera

56 CCD_USB20_N
56 CCD_USB20_P

Type C USB20

73 TYPEC_USB20_N
73 TYPEC_USB20_P

Type-C

71 USB3_TCSS_TX_P0
71 USB3_TCSS_TX_N0
71 USB3_TCSS_RX_P0
71 USB3_TCSS_RX_N0

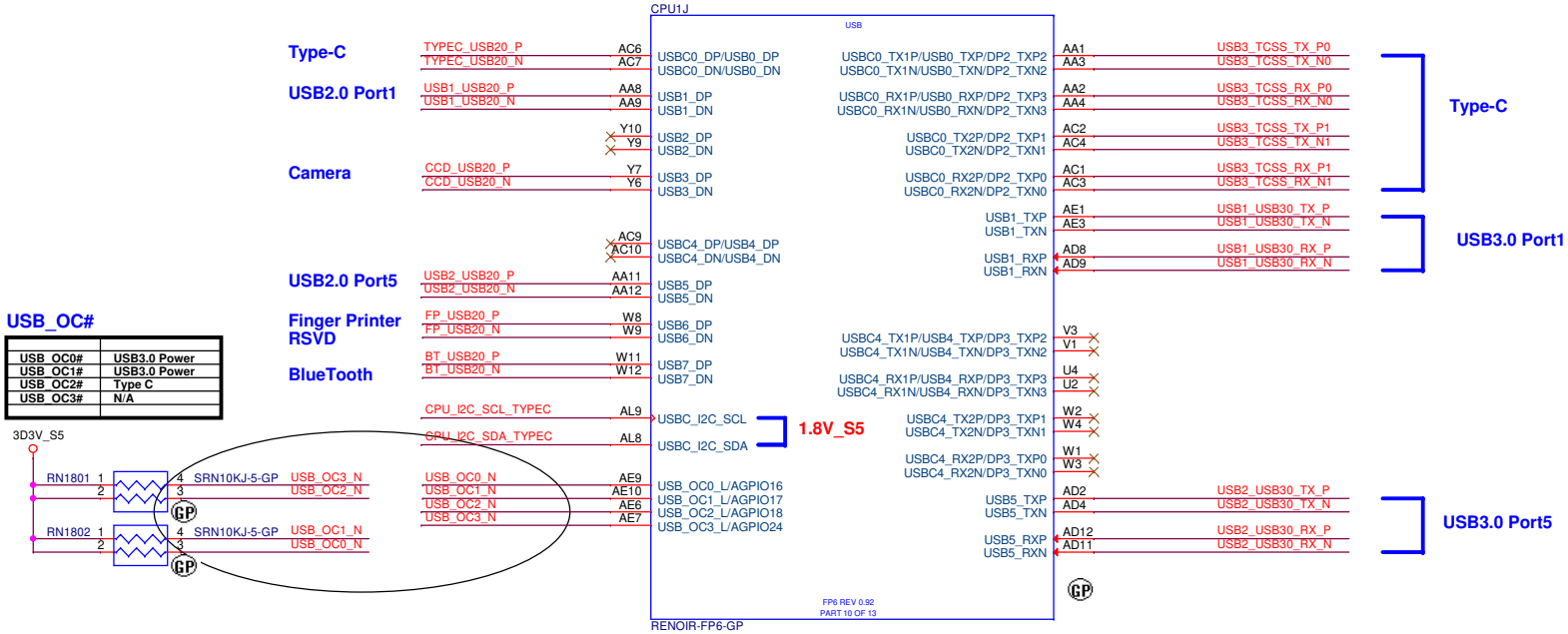
71 USB3_TCSS_TX_P1
71 USB3_TCSS_TX_N1
71 USB3_TCSS_RX_P1
71 USB3_TCSS_RX_N1

36 USB_OC0_N
66 USB_OC3_N

71,72 PD_I2C_SCL_CPU
71,72 PD_I2C_SDA_CPU

BT

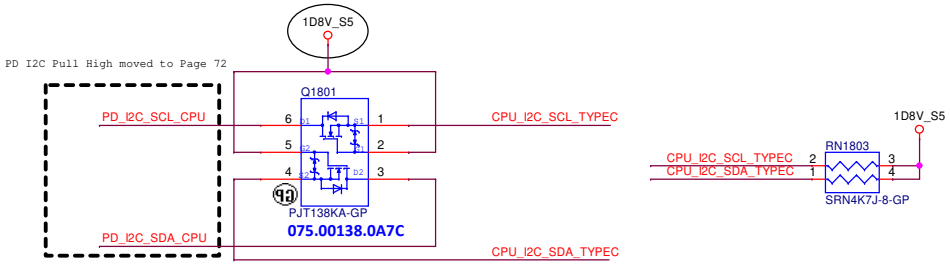
61 BT_USB20_P
61 BT_USB20_N



USB_OC#

USB_OC0#	USB3.0 Power
USB_OC1#	USB3.0 Power
USB_OC2#	Type C
USB_OC3#	N/A

AGPIO13/USB_OC5_L
If unused,
enable internal pull up or pull down by software.



LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **FCH (USB/Camera/RSVD)**

Size	Document Number	Rev
A3	LV550 AMD	-1

Date: Monday, August 17, 2020 Sheet 18 of 106

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LV550 AMD

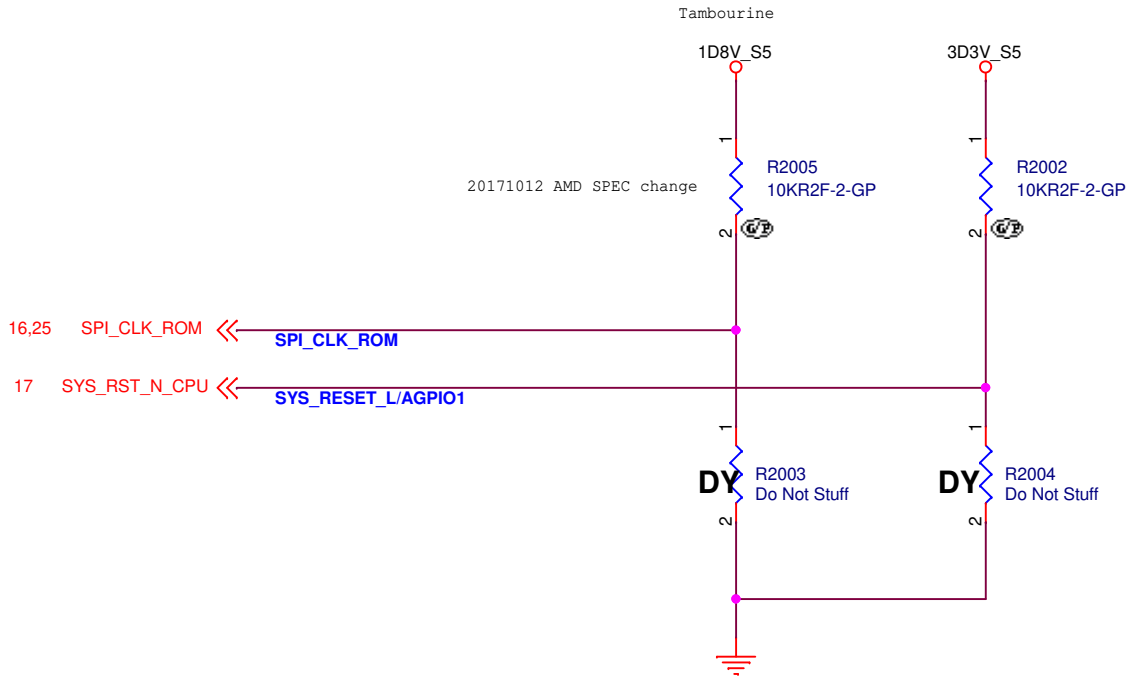
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 19 of 106

STRAP PINS



	PIN SPI_CLK NET SPI_CLK_ROM	PIN SYS_RESET_L//AGPIO1 NET SYS_RST#_CPU
PULL HIGH	Configured for internal clock-generator 10kΩ(± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10KΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL LOW	Reserved	Reserved

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *FCH (Strap)*

Size: A4 | Document Number: LV550_AMD | Rev: -1

Date: Monday, August 17, 2020 | Sheet 20 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 21 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 22 of 106

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LV550 AMD

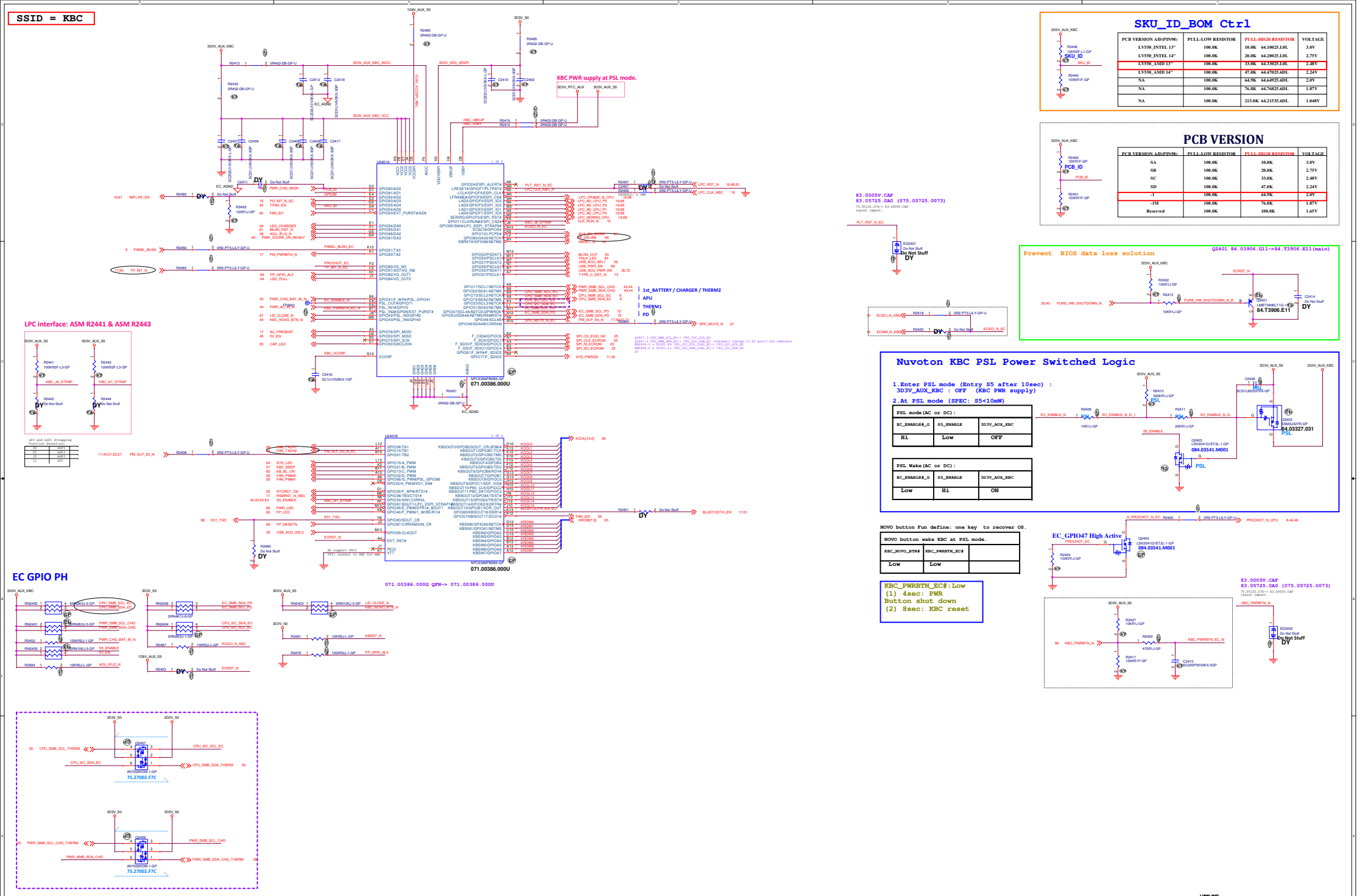
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 23 of 106

SSID = KBC



SKU_ID_BOM Ctrl

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LV550_INTEL 13"	100.0K	10.0K 64.10025.L0L	3.0V
LV550_INTEL 14"	100.0K	20.0K 64.20025.L0L	2.75V
LV550_AMD 13"	100.0K	33.0K 64.33025.L0L	2.48V
LV550_AMD 14"	100.0K	47.0K 64.47025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-1M	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

SSID = Flash.ROM

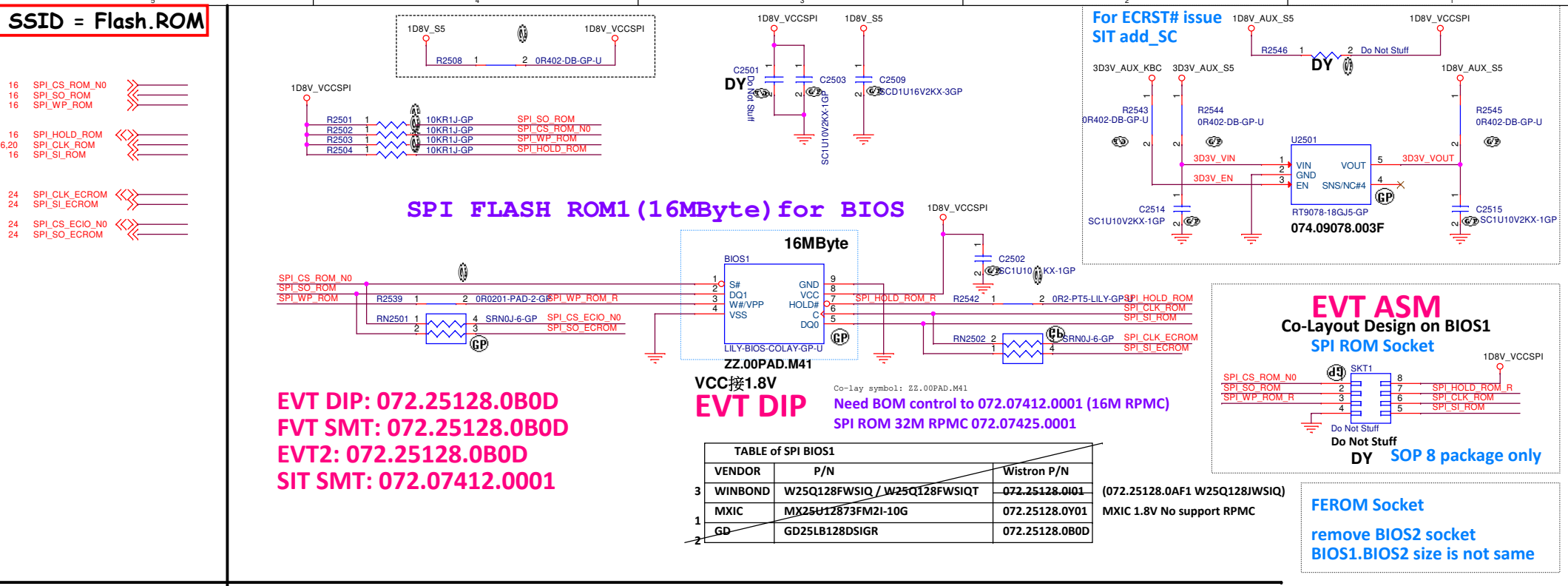
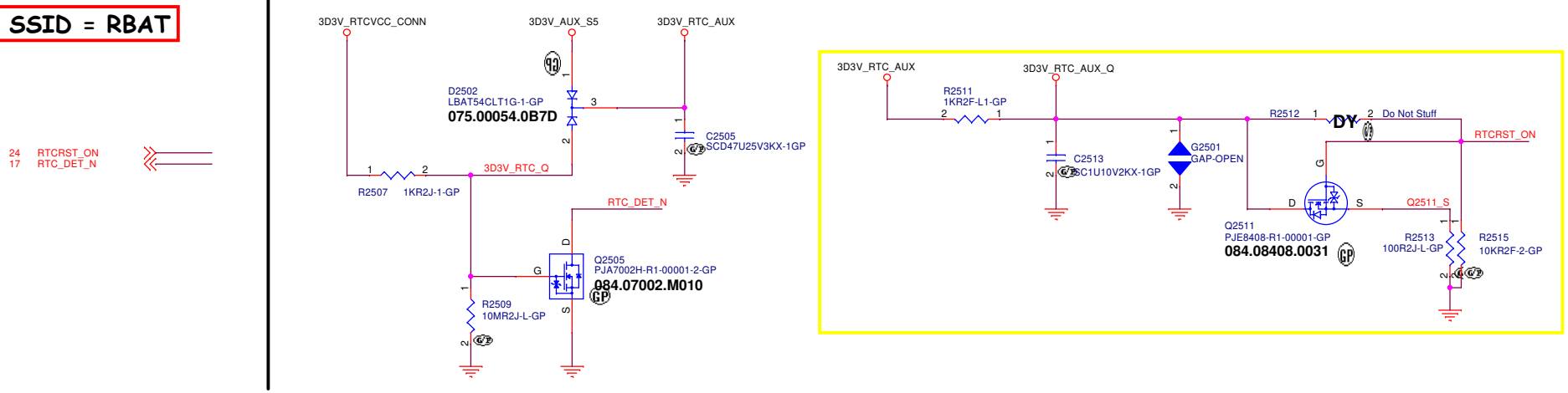


	TABLE of SPI BIOS1			
	VENDOR	P/N	Wistron P/N	
3	WINBOND	W25Q128FWSIQ / W25Q128FWSIQT	~~072.25128.0I01~~	(072.25128.0AF1 W25Q128JWSIQ)
1	MXIC	MX25U12873FM2I-10G	072.25128.0Y01	MXIC 1.8V No support RPMC
2	GD	GD25LB128DSIGR	072.25128.0B0D	

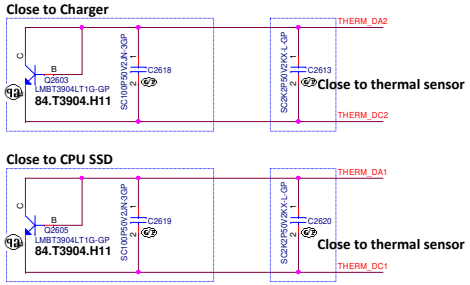
SSID = RBAT

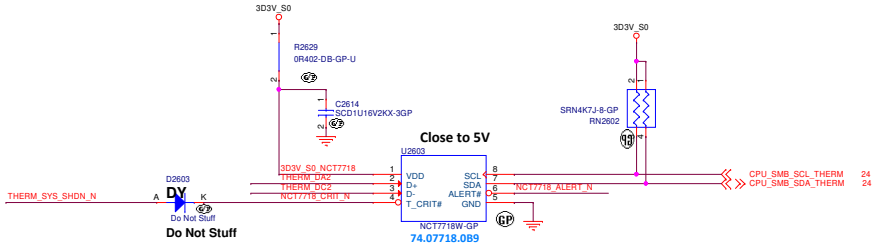


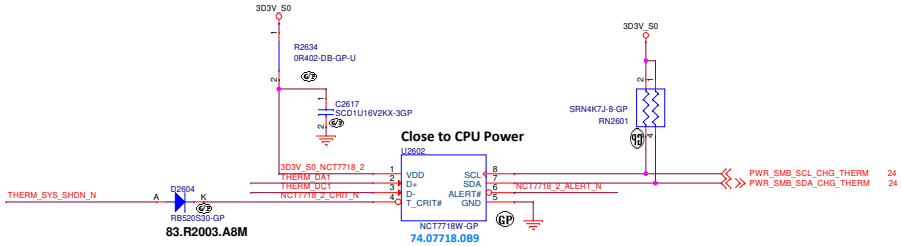
LV550 AMD

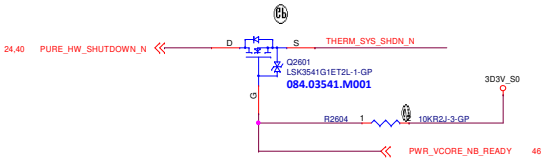
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Flash/RTC	
Size A3	Document Number LV550_AMD	Rev -1
Date: Monday, August 17, 2020	Sheet 25 of 106	

Main Func = Thermal Sensor

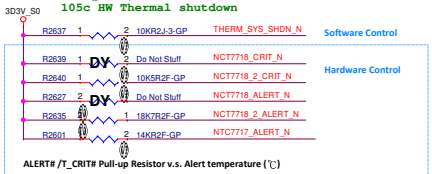








Set Q2605, U2602
105c HW Thermal shutdown



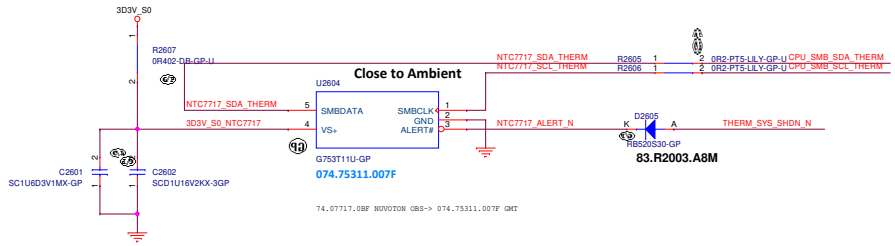
ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

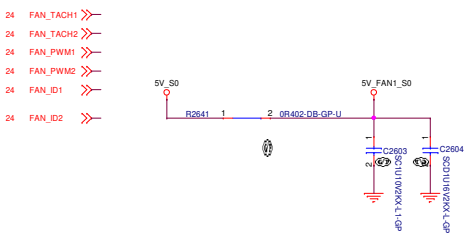
NCT7718W Table:

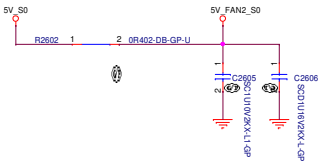
R2627 \ R2639 R2635 \ R2640	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

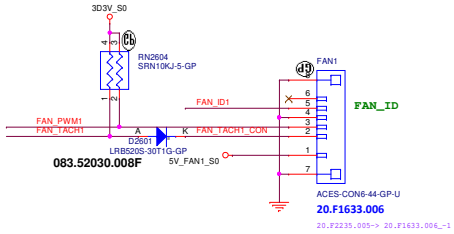
NCT77117U Table:

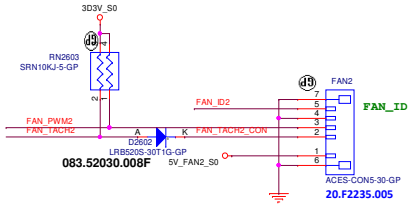
R2601	℃
2.0K	75
7.5K	90
10.5K	100
14.0K	105
18.7K	110



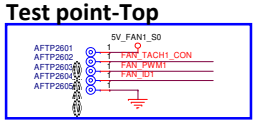








Test point-Top



Add AFTP2601- AFTP2610_SC

Test point-Top

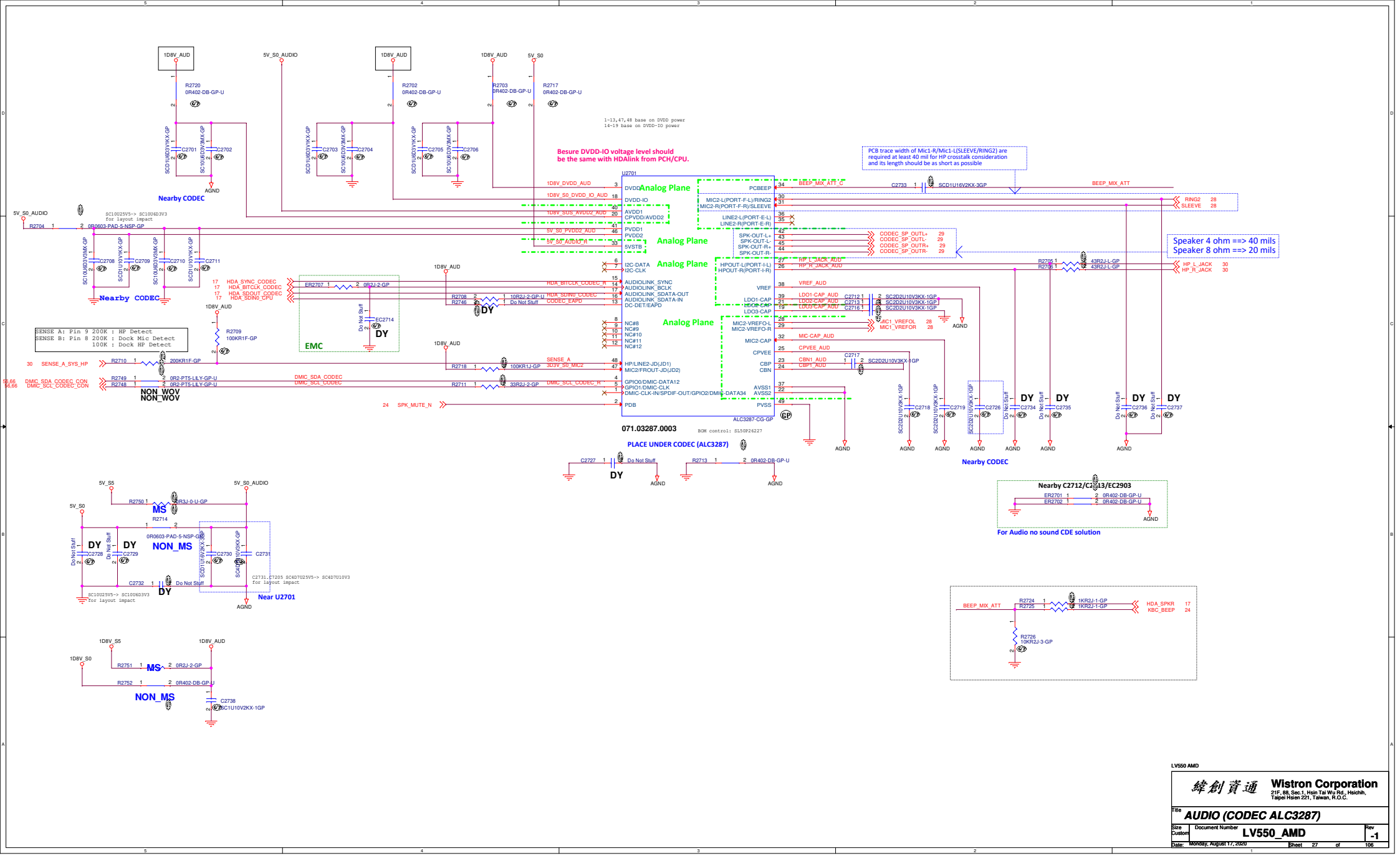
LV550 AMD

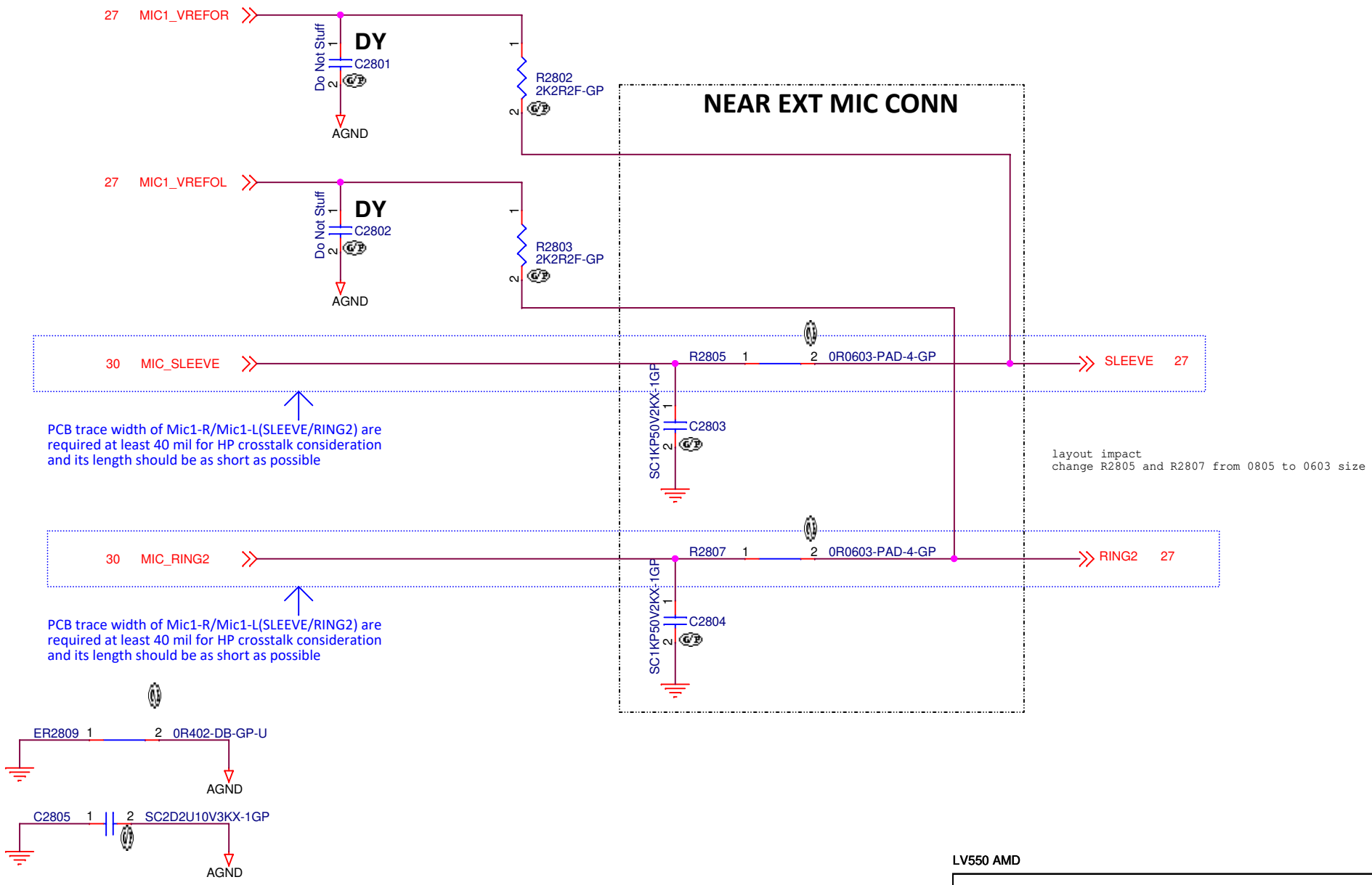
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (THERMAL/FAN)

Size	Document Number	Rev
A2	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 26 of 106


1D8V_AUD
5V_S0_AUDIO
5V_S0
R2720 0R402-DB-GP-U
R2702 0R402-DB-GP-U
R2703 0R402-DB-GP-U
R2717 0R402-DB-GP-U
1-13,47,48 base on DVDD power
14-19 base on DVDD-IO power
Besure DVDD-IO voltage level should be the same with HDAlink from PCH/CPU.
PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration and its length should be as short as possible
Nearby CODEC
U2701
Analog Plane
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
SENSE A: Pin 9 200K : HP Detect
SENSE B: Pin 8 200K : Dock Mic Detect
100K : Dock HP Detect
EMC
NON_WOV
071.03287.0003
ALC3287-CG-GP
BOM control: SL50P26227
PLACE UNDER CODEC (ALC3287)
Nearby C2712/C2713/EC2903
For Audio no sound CDE solution
MS
NON_MS
Near U2701
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
LV550 AMD
AUDIO (CODEC ALC3287)
Document Number LV550_AMD
Rev -1
Date: Monday, August 17, 2020
Sheet 27 of 106



LV550 AMD

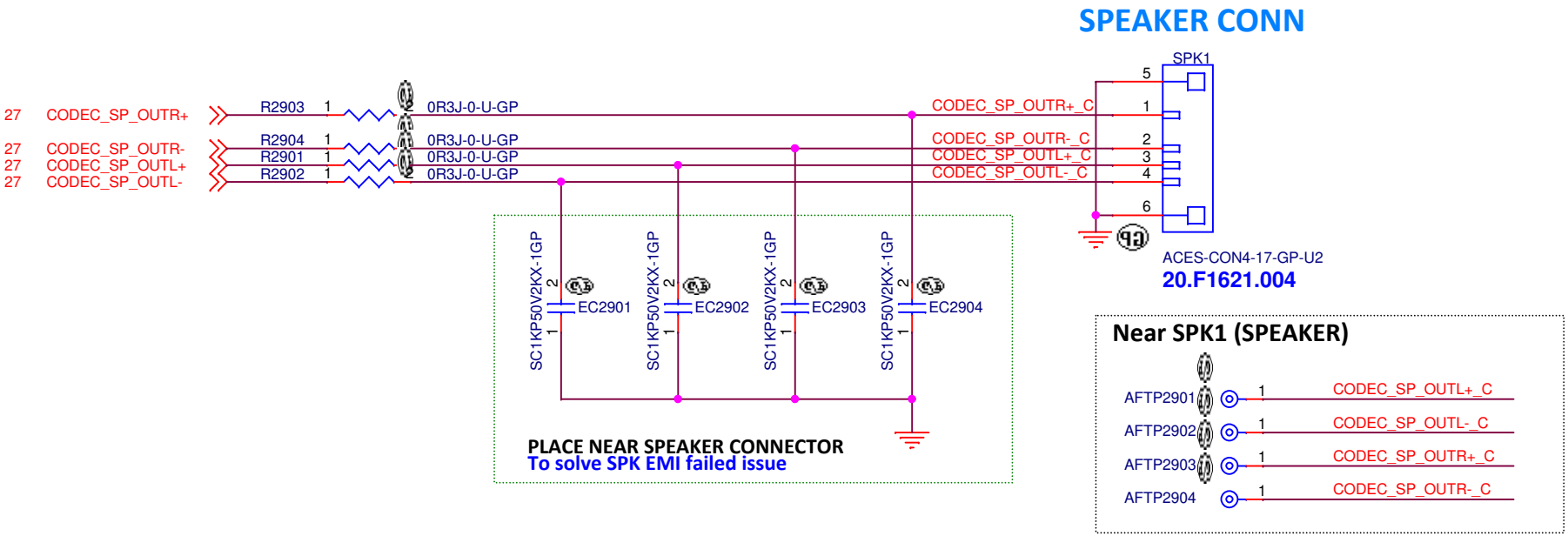
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***AUDIO (MIC I/F)***

Size	Document Number	Rev
A4	**LV550_AMD**	**-1**

Date: Monday, August 17, 2020 Sheet 28 of 106

Main Func = AUDIO



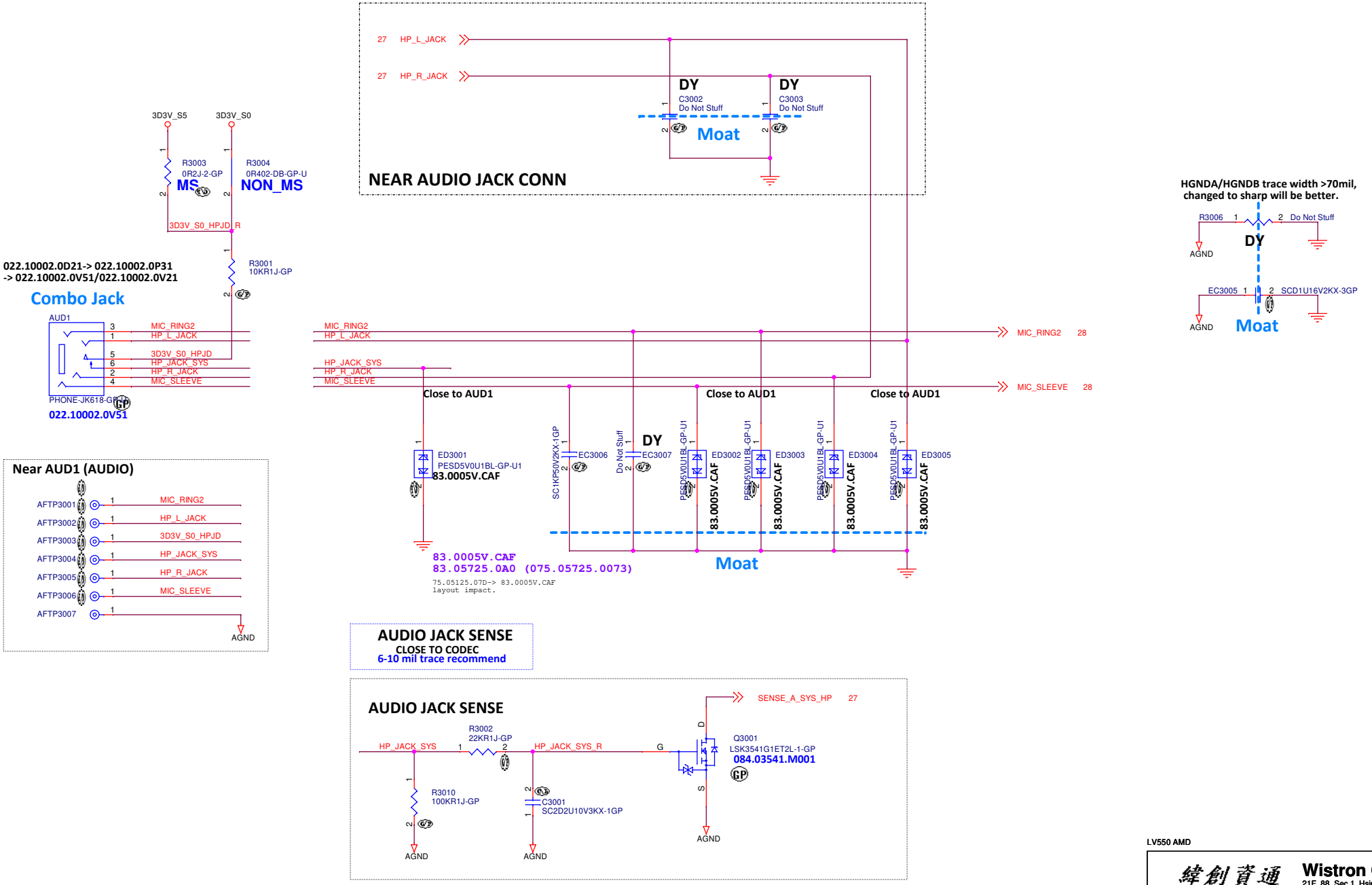
LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO (SPEAKER)*

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 29 of 106



LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (AUDIO JACK)***

Size	Document Number	Rev
A3	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 30 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 31 of 106

(Blanking)

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD) (RJ45+Transfor)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 32 of 106

(Blanking)

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER (RSVD)(SDIO/CONN)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 33 of 106

(Blanking)

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD) (USB2.0 CONN)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 34 of 106

(Blanking)

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

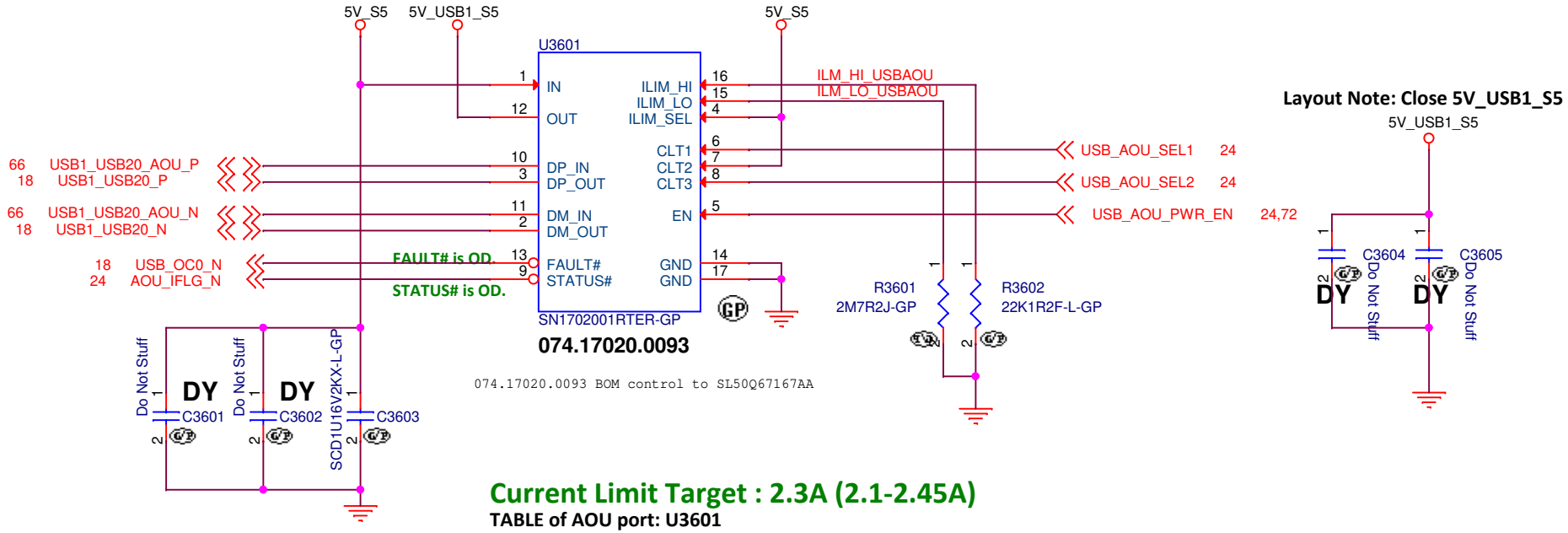
Title: USB (RSVD)(USB3.0 Conn)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 35 of 106

Main Func = USB Charger

For USB3.0 System Port1 (For AOU)



Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3601

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER	SL50Q67167AA
2nd	DIODES	PI5USB2546HZHEX	SL50Q67168AA

SN1702001RTER is not equivalent device of TPS2546RTER

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB(USB Charger)

Size: A4 | Document Number: LV550_AMD | Rev: -1

Date: Monday, August 17, 2020 | Sheet 36 of 106

(Blanking)

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD)(PCIE to USB3.0)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 37 of 106

(Blanking)

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD)(USB Redriver/Hub)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 38 of 106

(Blanking)

LV550 AMD

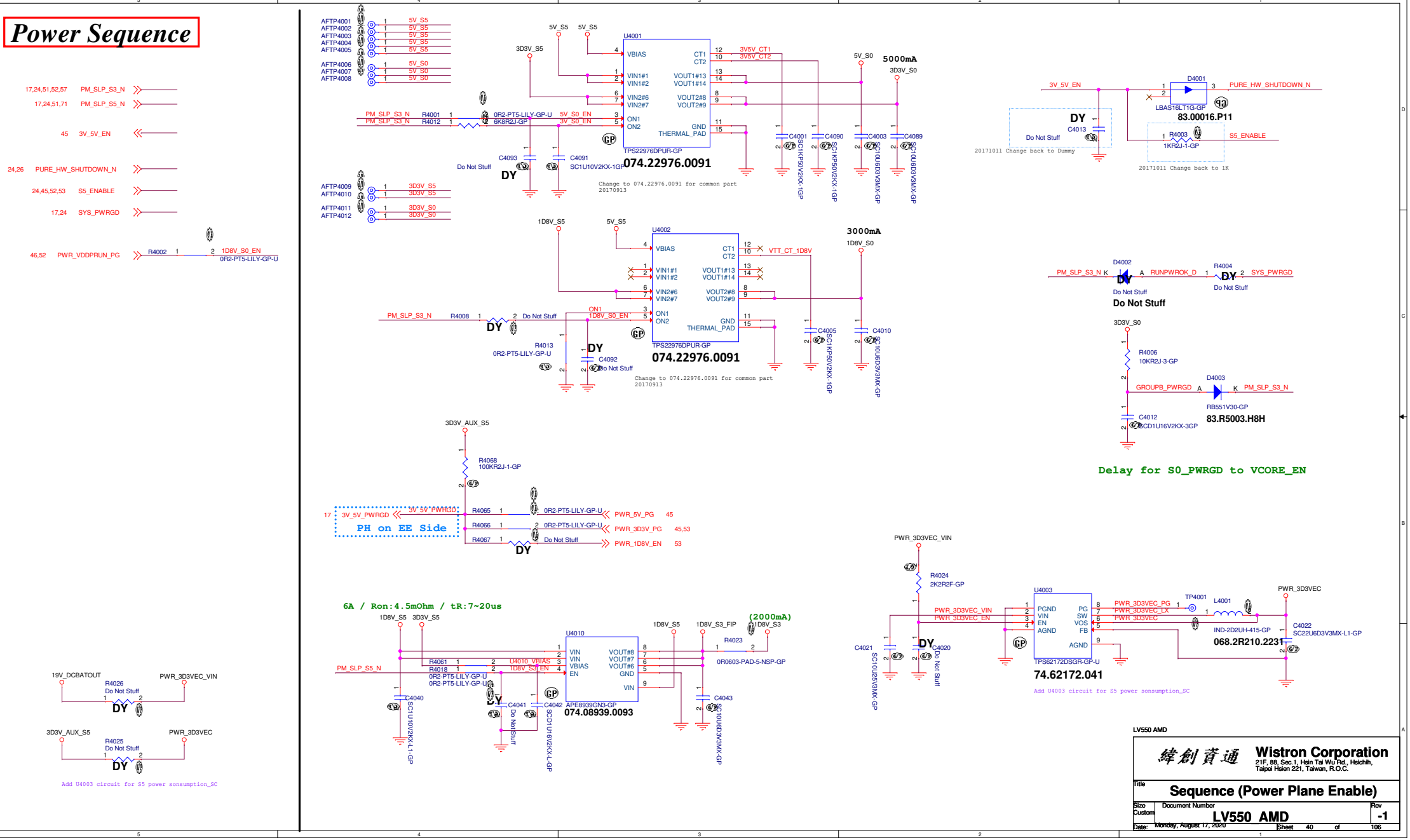
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 39 of 106

Power Sequence



LV550 AMD

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Sequence (Power Plane Enable)
Size: Custom	Document Number: LV550_AMD
Rev	-1
Date: Monday, August 17, 2020	Sheet 40 of 106

(Blanking)

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (RSVD) (DS3/S0ix)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 41 of 106

(Blanking)

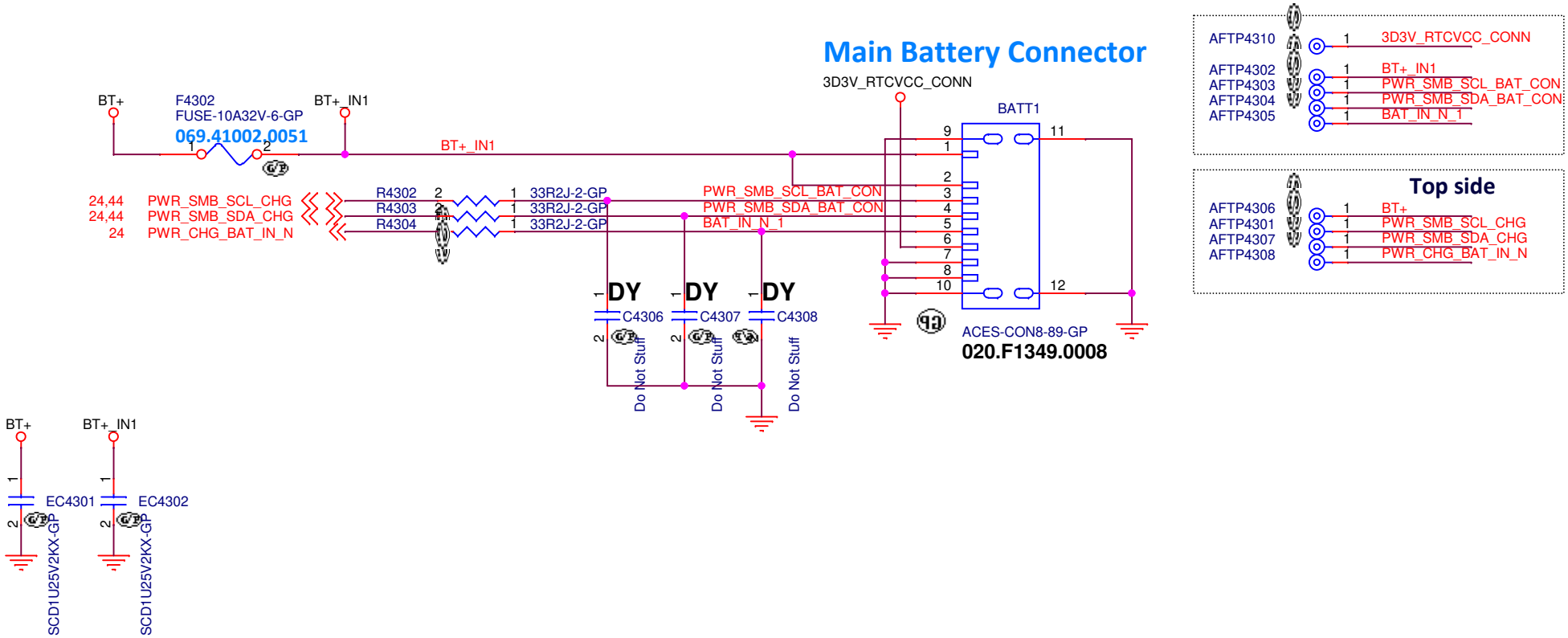
LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)(TYPEC DC-DC)*

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 42 of 106



LV550 AMD

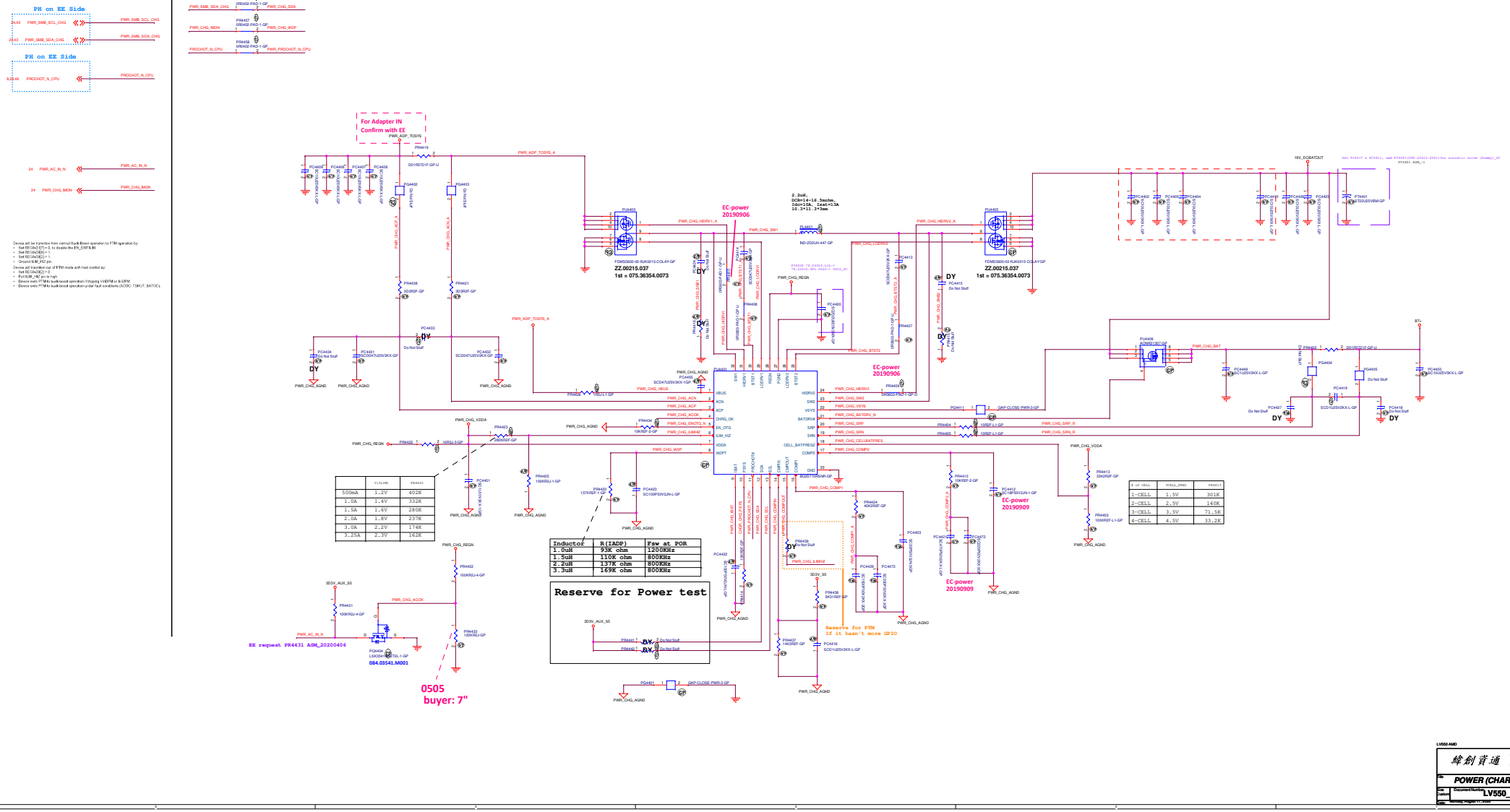
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***INT IO (DCIN/BATT CONN)***

Size	Document Number	Rev
A4	**LV550_AMD**	**-1**

Date: Monday, August 17, 2020 Sheet 43 of 106

OFFPAGE - PIC - EE



LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (CHARGER_BQ25710R)
Size / Custom	Document Number: LV550_AMD
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OFFPAGE-Signal

AMD power sequence_SC

24,40,52,53 S5_ENABLE — R4501 4K3R2J-GP — PWR_3D3V_EN

40,45 3V_5V_EN — R4502 Do Not Stuff — DY — C4501 SC22U6D3V3MX-L-GP

48,53 PWR_3D3V_PG — PWR_3D3V_PG

24 5V_EN — R4503 0R2-PT5-LLY-GP-U — PWR_5V_EN

40,45 3V_5V_EN — R4504 Do Not Stuff — DY

PH on EE Side

40 PWR_5V_PG — PWR_5V_PG

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_3D3V
PG4515 GAP-CLOSE-PWR-3-GP
PG4516 GAP-CLOSE-PWR-3-GP
PG4517 GAP-CLOSE-PWR-3-GP
PG4518 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_3D3V
PG4519 GAP-CLOSE-PWR-3-GP
PG4520 GAP-CLOSE-PWR-3-GP
PG4521 GAP-CLOSE-PWR-3-GP
PG4522 GAP-CLOSE-PWR-3-GP
PG4523 GAP-CLOSE-PWR-3-GP
PG4524 GAP-CLOSE-PWR-3-GP

3D3V_AUX_S5 — PR4532 0R2J-2-GP — PWR_3D3V_LDO

PG4532 GAP-> 0 ohm_SC
PG4532-> PR4532_-1

19V_DCBATOUT — PWR_DCBATOUT_5V
PG4552 GAP-CLOSE-PWR-3-GP
PG4553 GAP-CLOSE-PWR-3-GP
PG4555 GAP-CLOSE-PWR-3-GP
PG4557 GAP-CLOSE-PWR-3-GP
PG4559 GAP-CLOSE-PWR-3-GP
PG4561 GAP-CLOSE-PWR-3-GP

5V_S5 — PWR_5V
PG4551 GAP-CLOSE-PWR-3-GP
PG4554 GAP-CLOSE-PWR-3-GP
PG4556 GAP-CLOSE-PWR-3-GP
PG4558 GAP-CLOSE-PWR-3-GP
PG4560 GAP-CLOSE-PWR-3-GP
PG4563 GAP-CLOSE-PWR-3-GP
PG4564 GAP-CLOSE-PWR-3-GP
PG4566 GAP-CLOSE-PWR-3-GP

5V_AUX_S5 — PG4565 GAP-CLOSE-PWR-3-GP — PWR_5V_LDO

IDC : 6A
OCP : 8A

Vin Operating range : 4~24V
Vin_Max : 26V

Ilimt : 8A

Hybrid/NVDC4串BT Need Change Solution

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PU4501 TPS51393PRJER-GP

Close to PU4501

Place another side , make GND plan bigger

EN rating :5 .5V
ENLDO Rising Threshold :1.5V
ENLDO Falling Threshold : 0.8V
EN Rising Threshold :1.3V
EN Falling Threshold : 1.12V

Trace used 10 mil

Close to PC4511

IDC:8A

Vin Operating range : 4~24V
Vin_Max : 26V

Ilimt : 8A

Hybrid/NVDC4串BT Need Change Solution

Place another side , make GND plan bigger

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PU4551 TPS51395PRJER-GP

Close to PU4551

Trace used 10 mil

EN rating :5 .5V
ENLDO Rising Threshold :1.5V
ENLDO Falling Threshold : 0.8V
EN Rising Threshold :1.3V
EN Falling Threshold : 1.12V

LV550 AMD

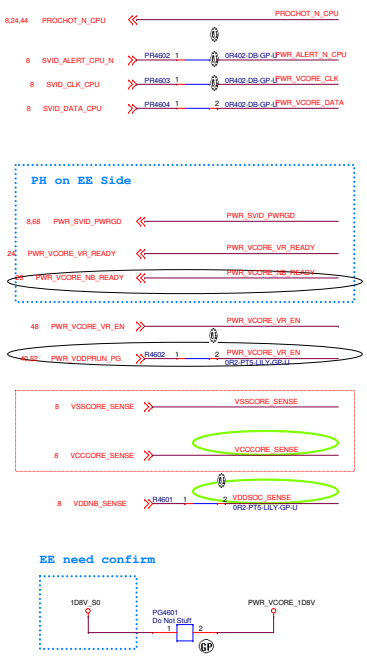
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51393/TPS51395R_5V/3D3V

Size: A2 | Document Number: LV550_AMD | Rev: -1

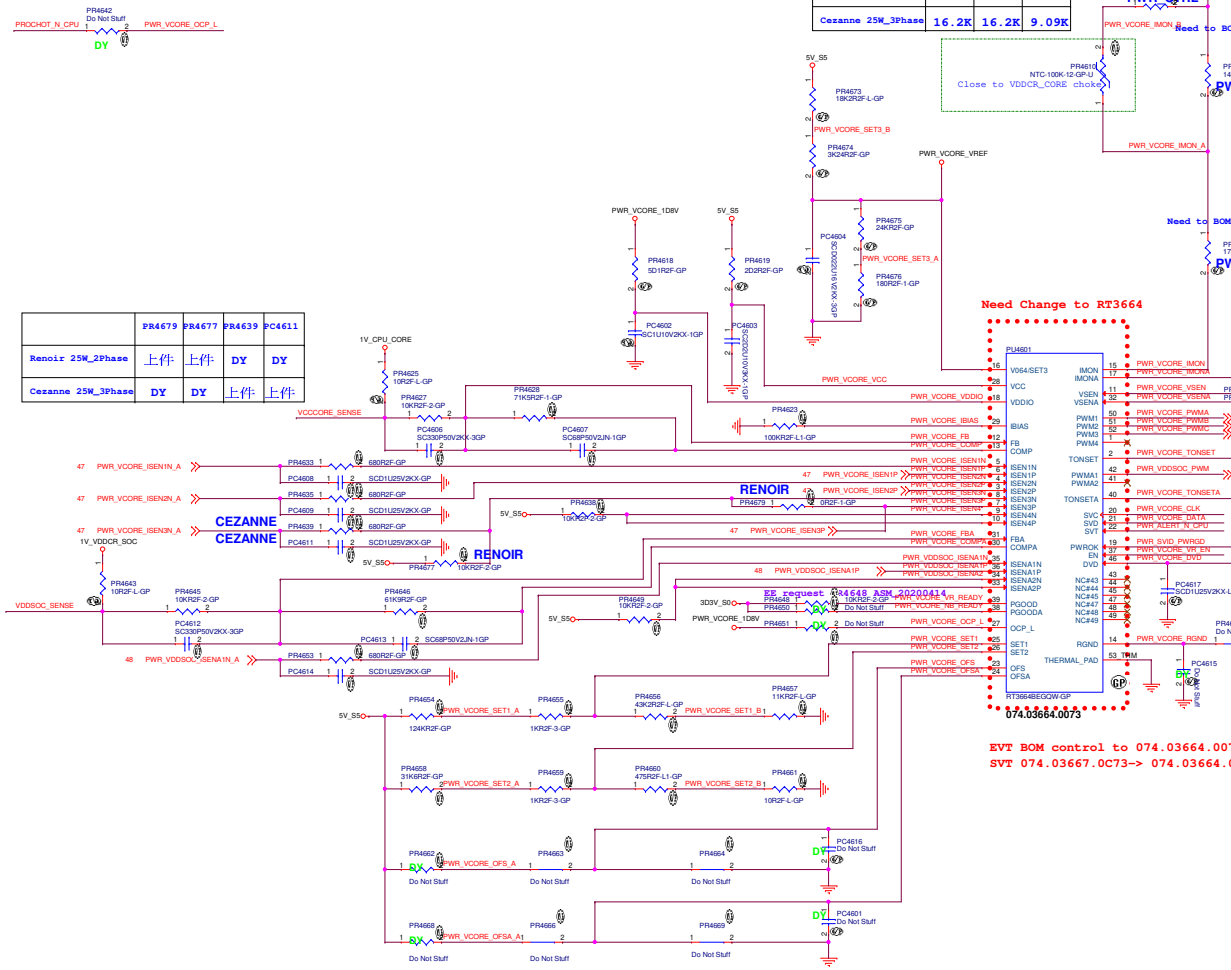
Date: Monday, August 17, 2020 | Sheet 45 of 106

OFFPAGE



Need to BOM control	PR4606	PR4608	PR4614
Renoir 25W_2Phase	4.12K	14.3K	17.4K
Cezanne 25W_3Phase	16.2K	16.2K	9.09K

	PR4679	PR4677	PR4639	PC4611
Renoir 25W_2Phase	上件	上件	DY	DY
Cezanne 25W_3Phase	DY	DY	上件	上件



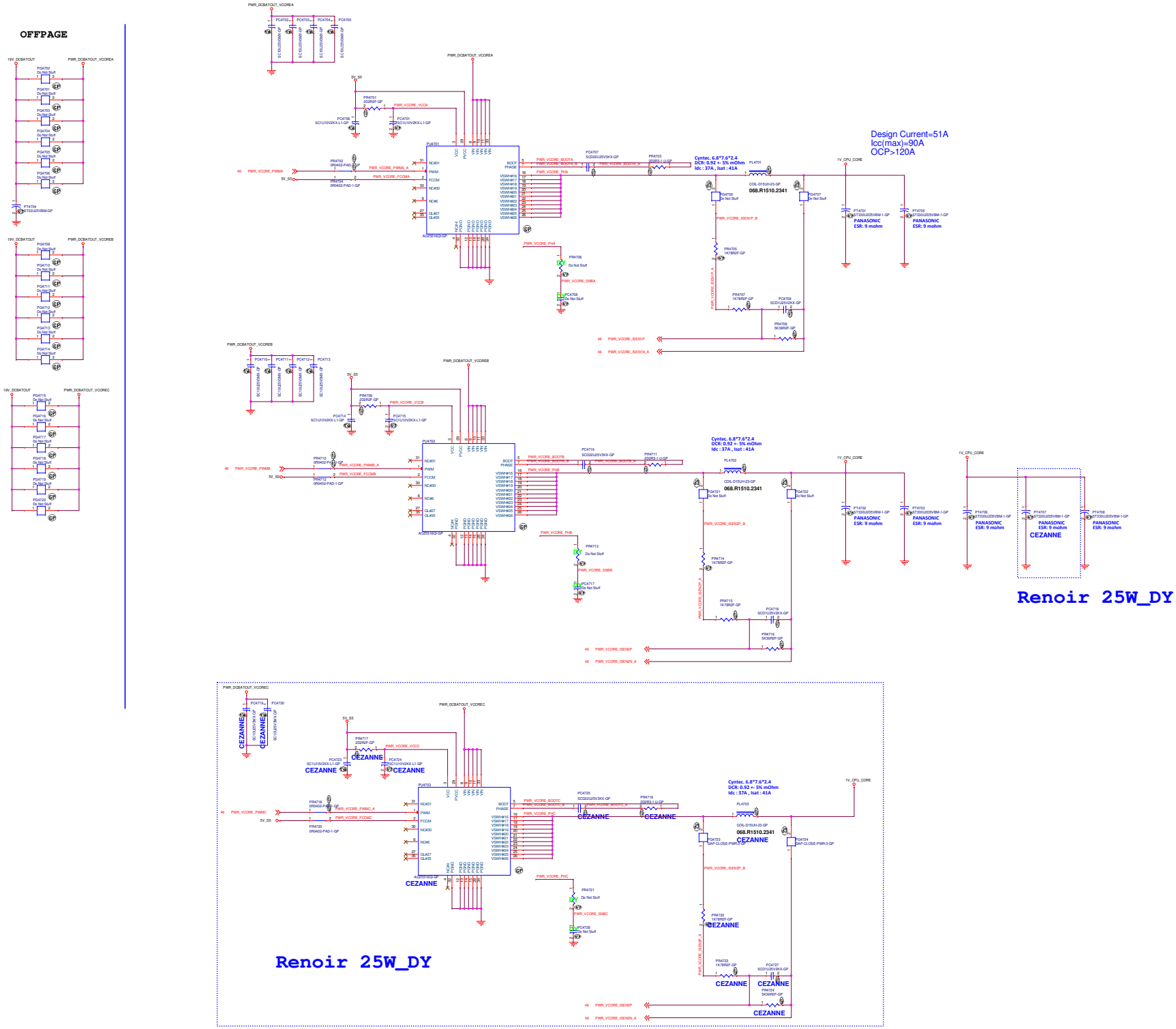
LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT3667BE_VCORE(1/3)

Size: Custom | Document Number: LV550_AMD | Rev: -1

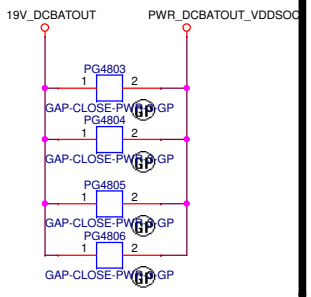
Date: Monday, August 17, 2020 | Sheet 46 of 105



LV550 AMD

蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title:	AOZ5516_VCORE(2/3)
Size:	
Document Number:	LV550_AMD
Rev:	-1
Date: Wednesday, August 17, 2005	Sheet 42 of 50

OFFPAGE



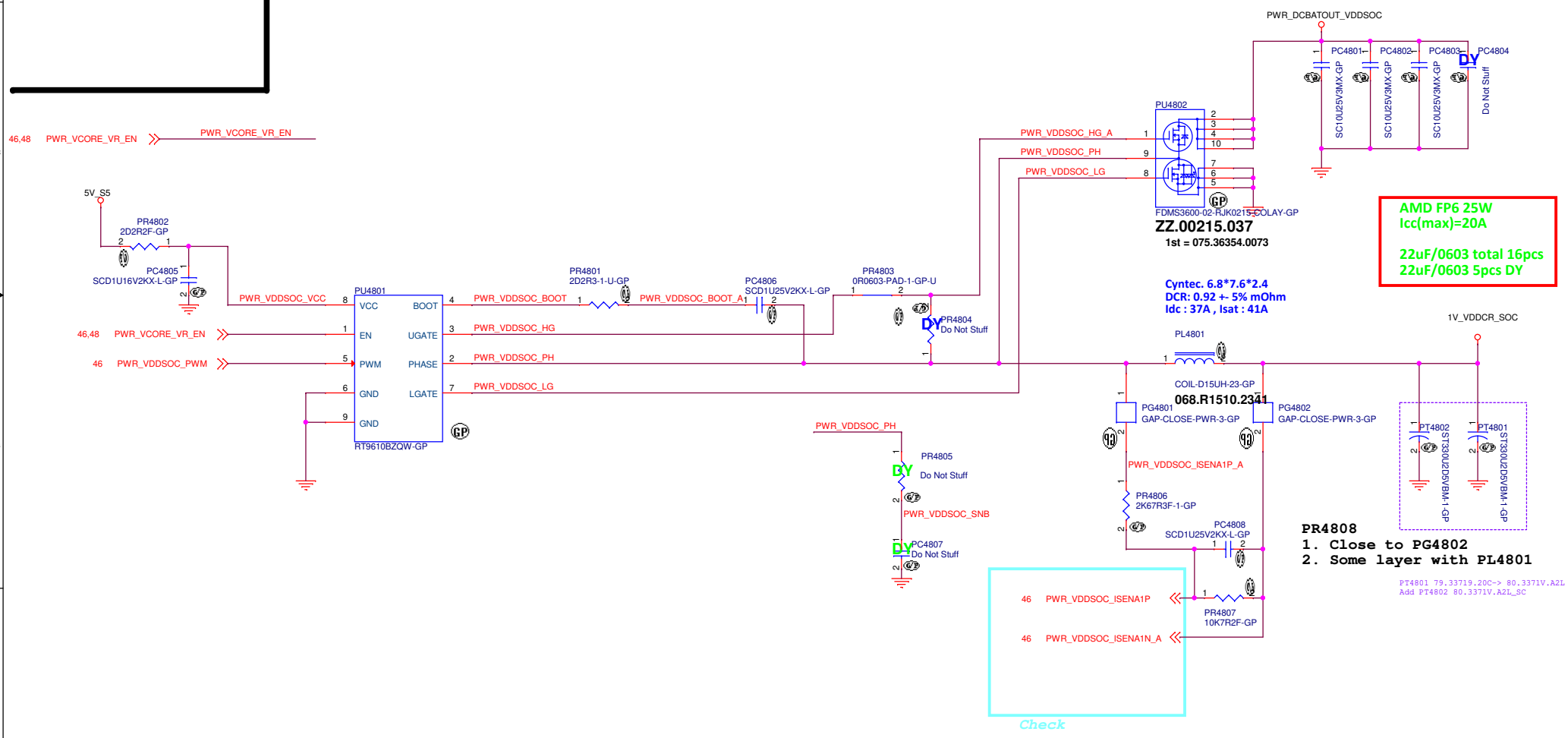
Main Func = CPU_CORE

AMD FP6 35W
Icc(max)=20A

22uF/0603 total 25pcs

AMD FP6 25W
Icc(max)=20A

22uF/0603 total 16pcs
22uF/0603 5pcs DY



LV550 AMD

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RT9610_VDDSOC(3/3)***
Size: Custom	Document Number: **LV550_AMD** — Rev: **-1**
Date: Monday, August 17, 2020	Sheet 48 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power (RSVD)**

Size	Document Number	Rev
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Date: Monday, August 17, 2020 Sheet 49 of 106

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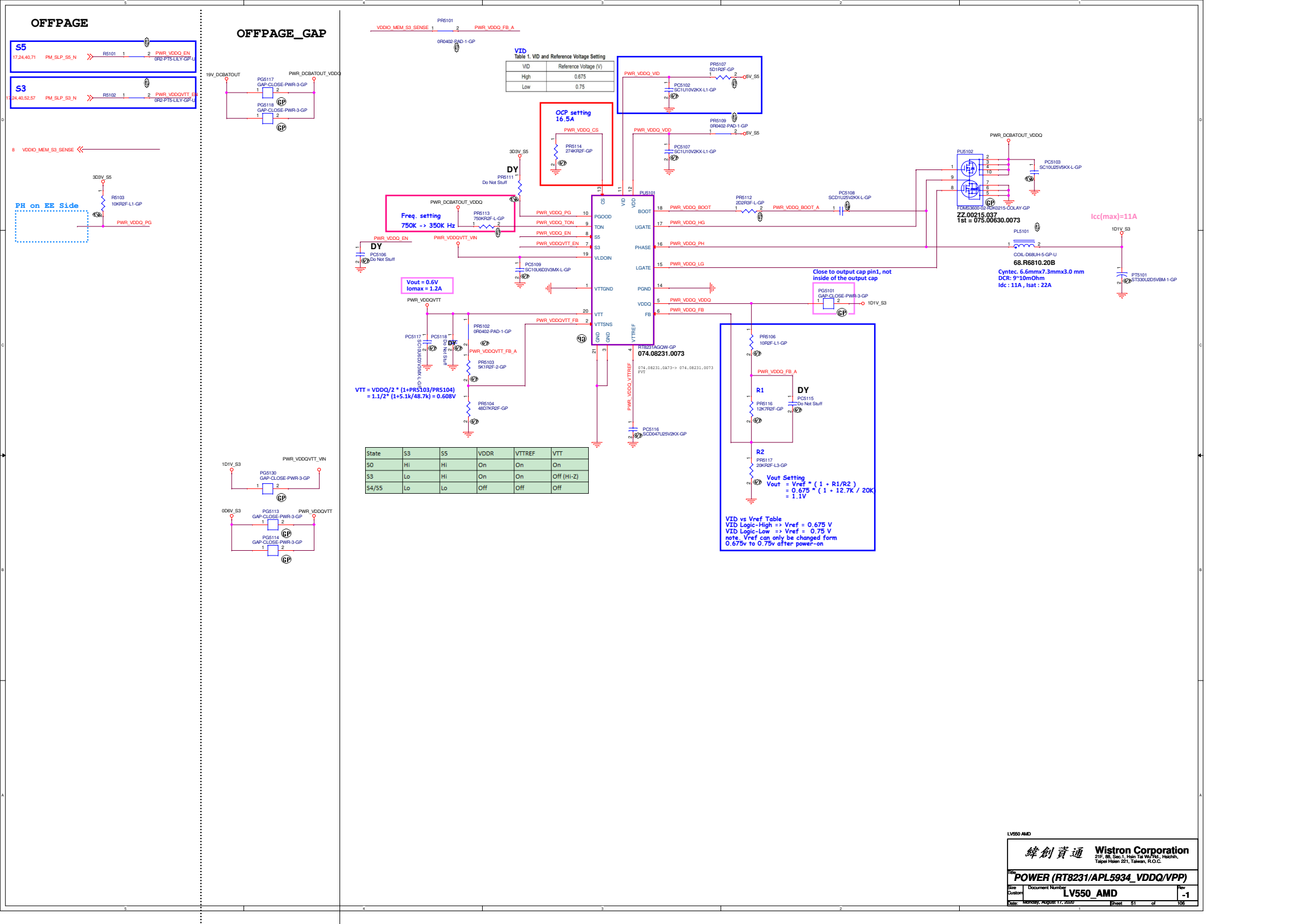
LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

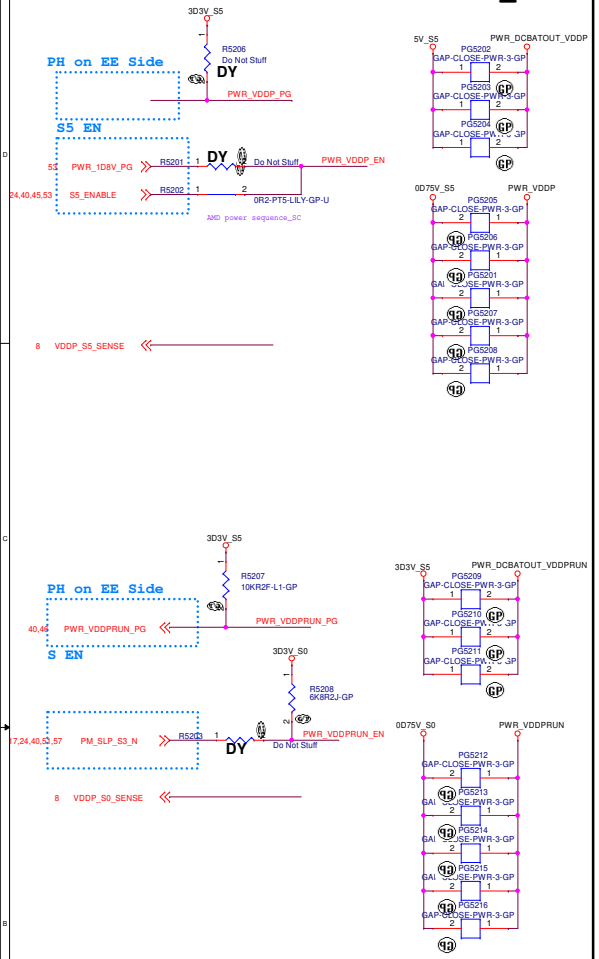
Title: **Power (RSVD)**

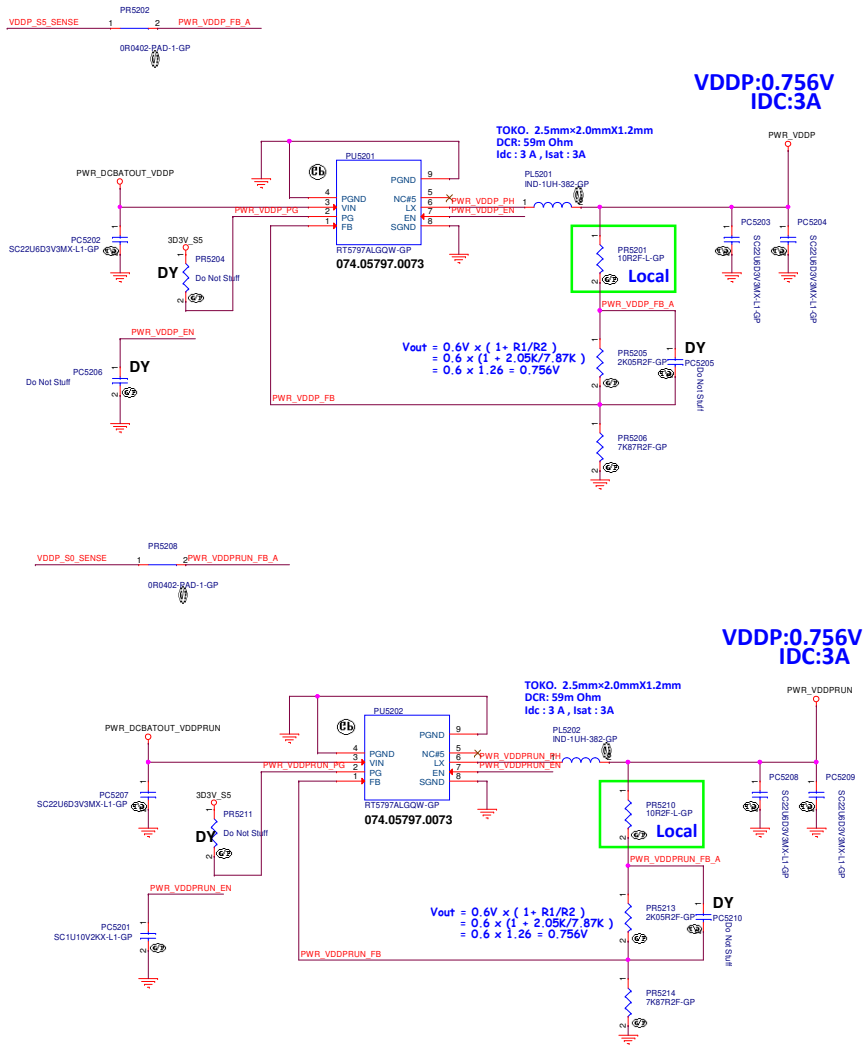
Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 50 of 106



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off





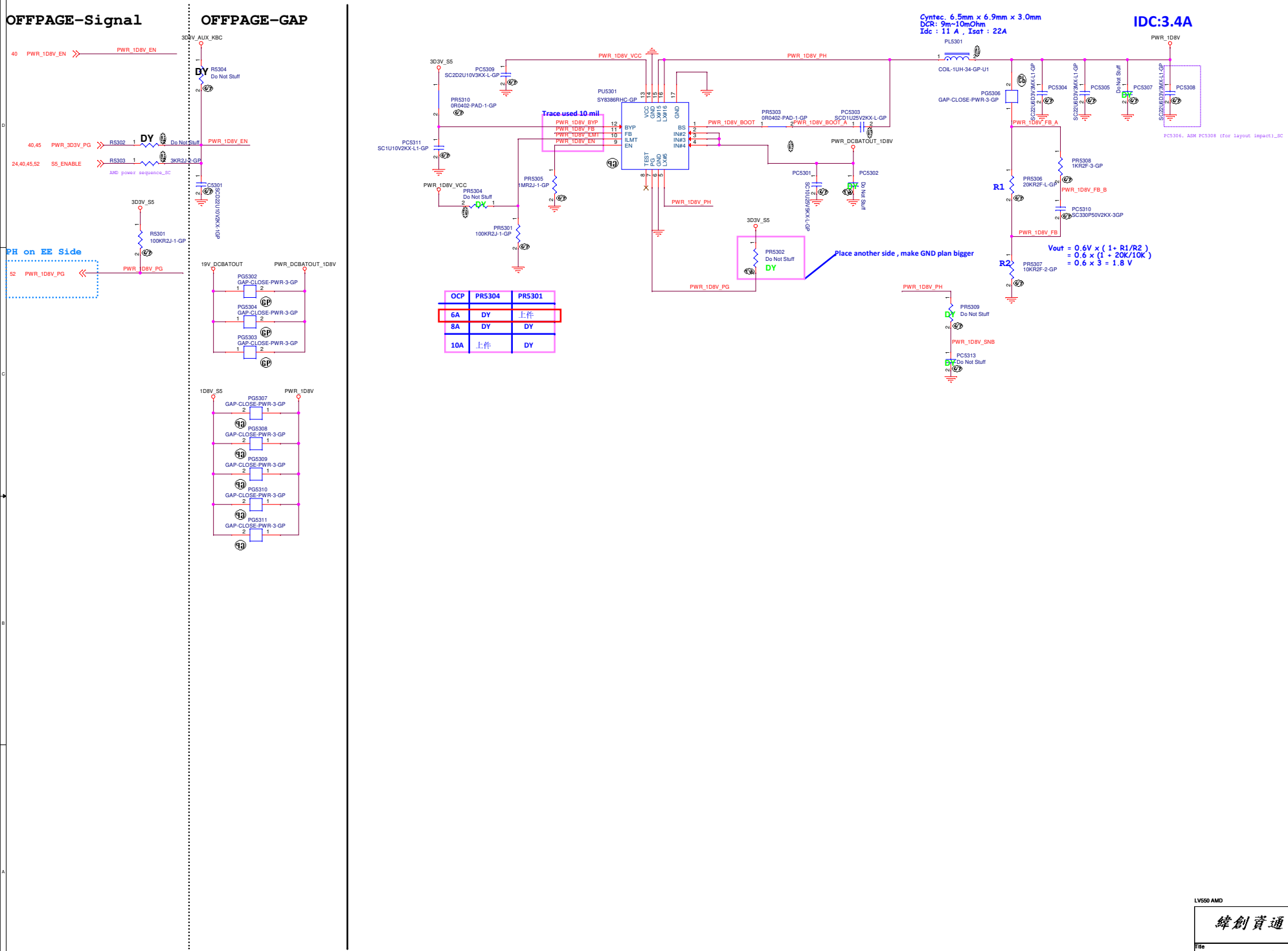
LV550 AMD

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER (RT5797_VDDP)***

Size	Document Number	Rev
A2	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 52 of 106



OCP	PR5304	PR5301
6A	DY	上件
8A	DY	DY
10A	上件	DY

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8386R_1D8V

Size	Document Number	Rev
A2	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 53 of 106

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LV550 AMD

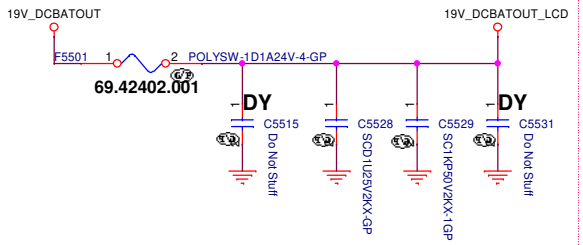
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER(RSVD)	
Size A4	Document Number LV550_AMD	Rev
Date: Monday, August 17, 2020	Sheet 54 of 106	

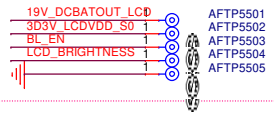
Main Func = LCD

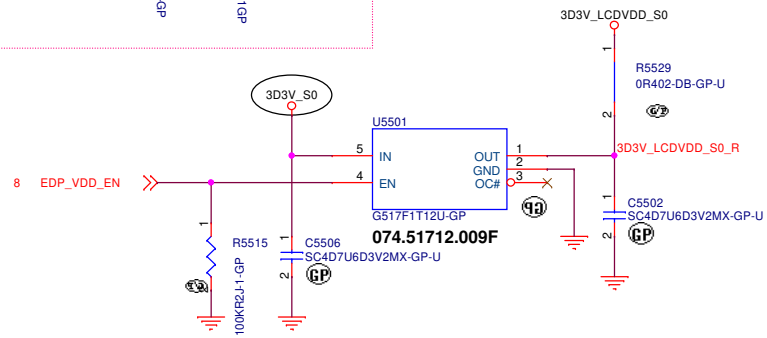
INVERTER POWER

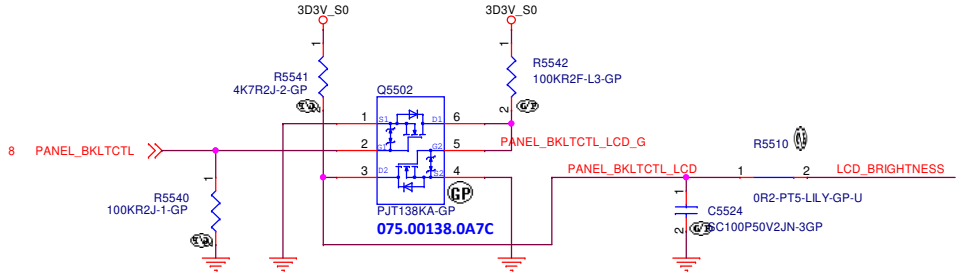
F5501 69.50007.A31->69.42402.001 (main)_20180718



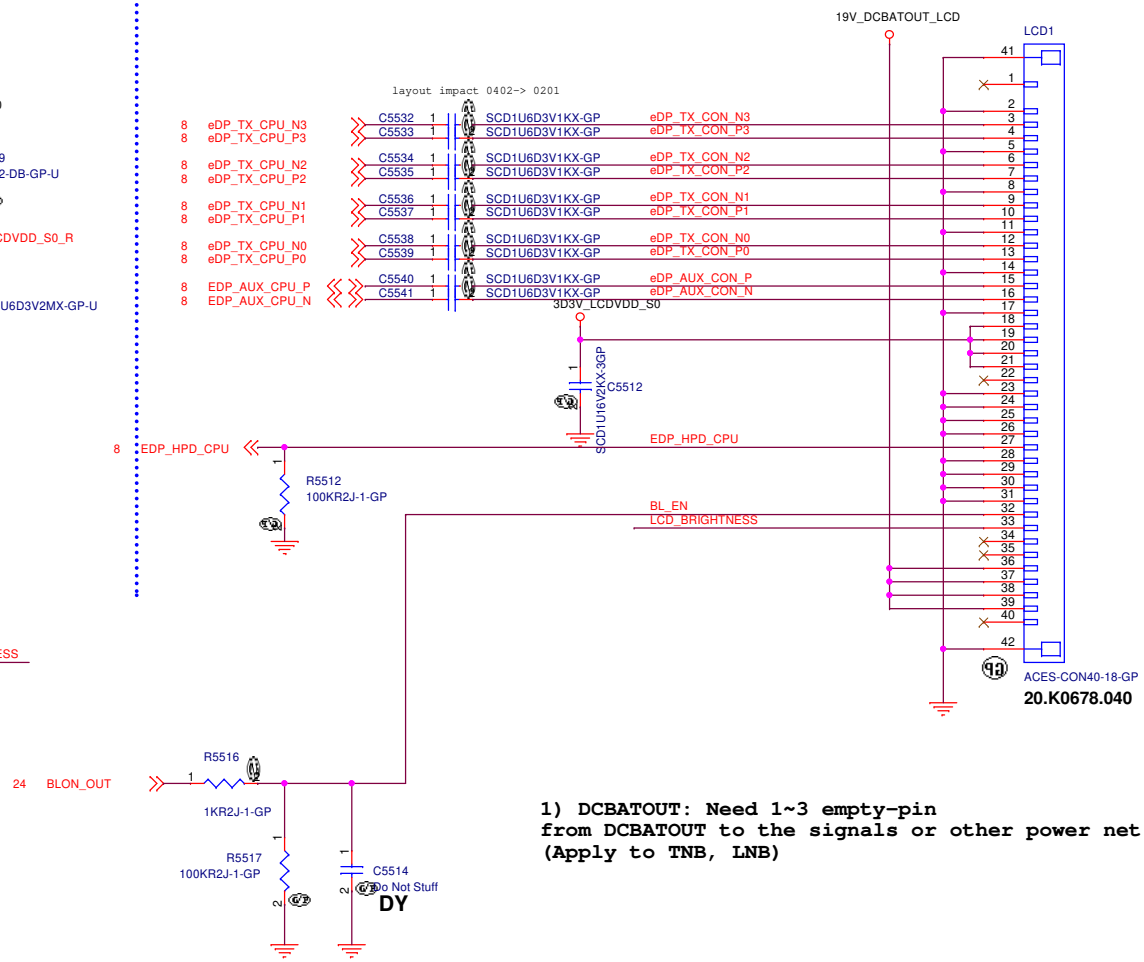
Test point







LCD Connector



1) DCBATOUT: Need 1~3 empty-pin
from DCBATOUT to the signals or other power net.
(Apply to TNB, LNB)

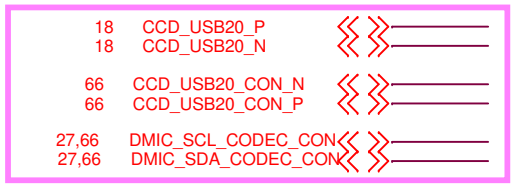
LV550 AMD

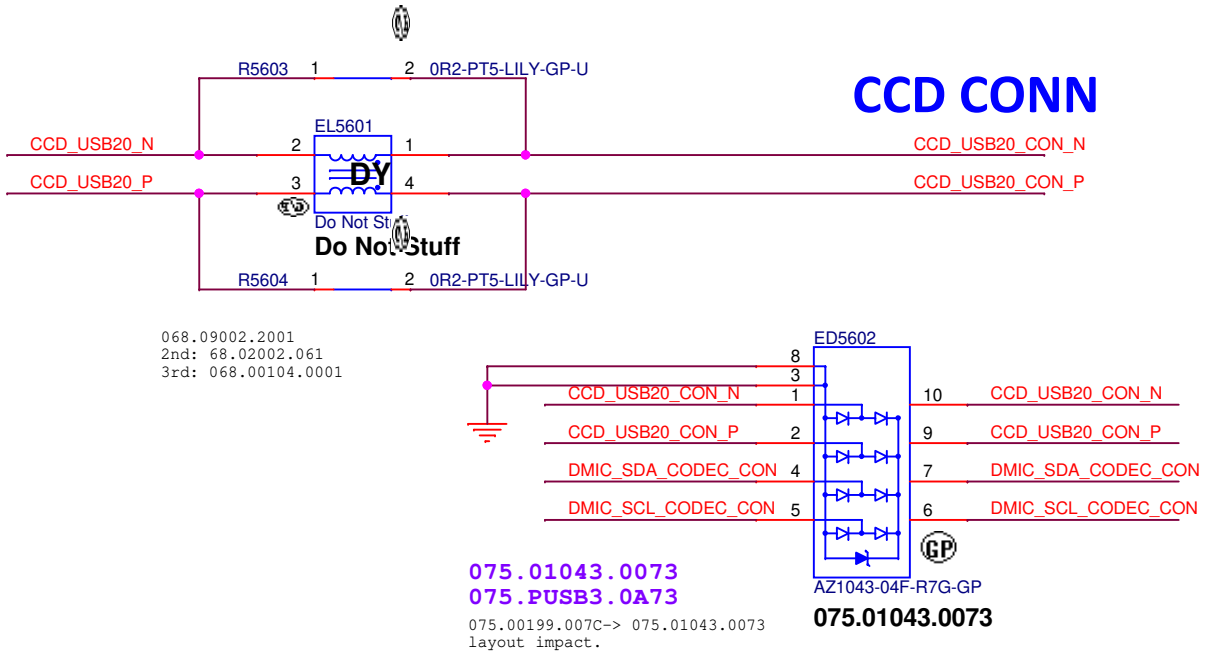
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISPLAY (LCD/TOUCH)

Size	Document Number	Rev
A3	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 55 of 106





LV550 AMD

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

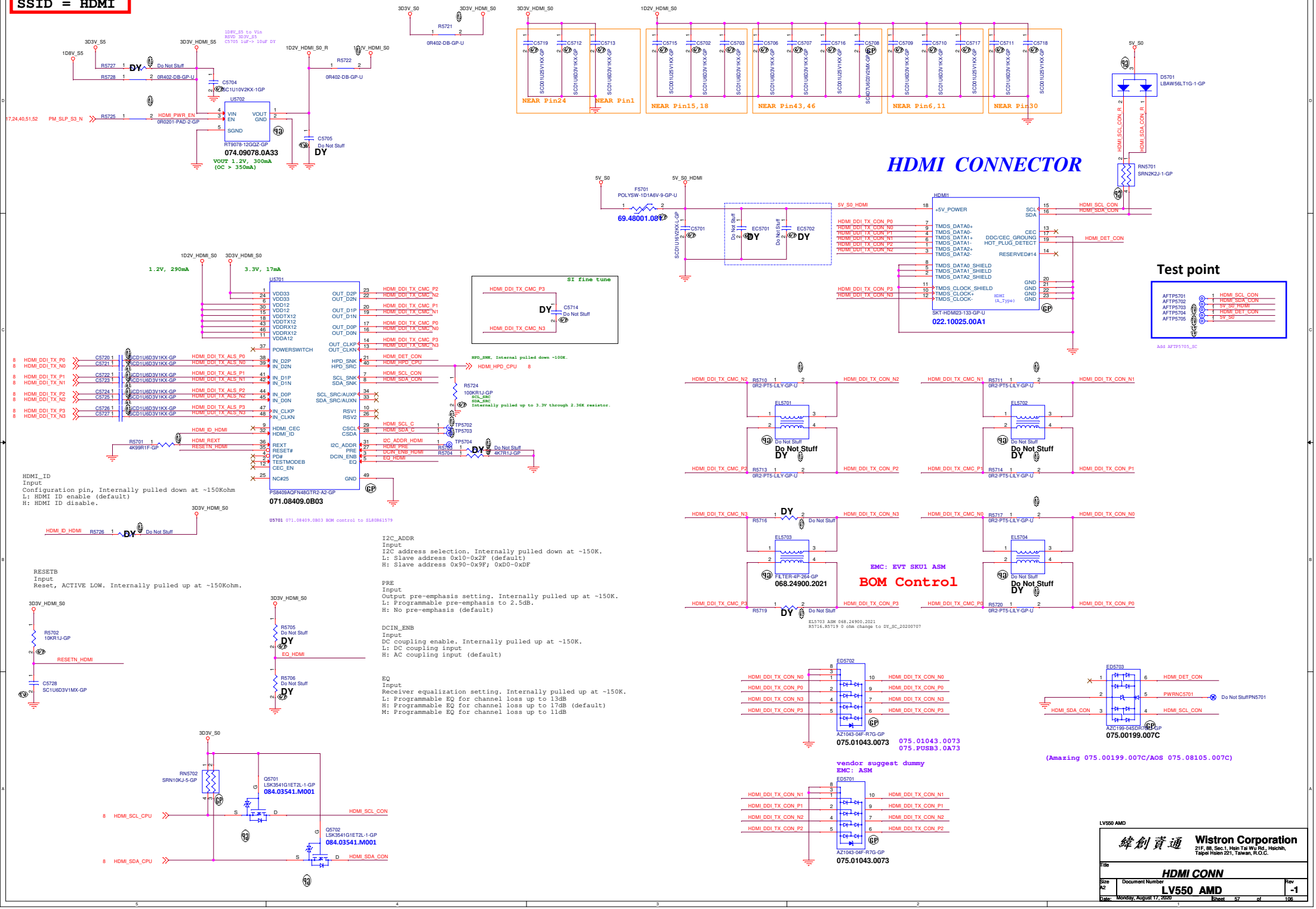
Title: ***Display (CRT/IR Camera)***

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 56 of 106

SSID = HDMI

HDMI CONNECTOR



LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI CONN**

Size	Document Number	Rev
A2	LV550 AMD	-1

Date: Monday, August 17, 2020 Sheet 57 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display (RSVD) DP / DVI**

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 58 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 59 of 106

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LV550 AMD

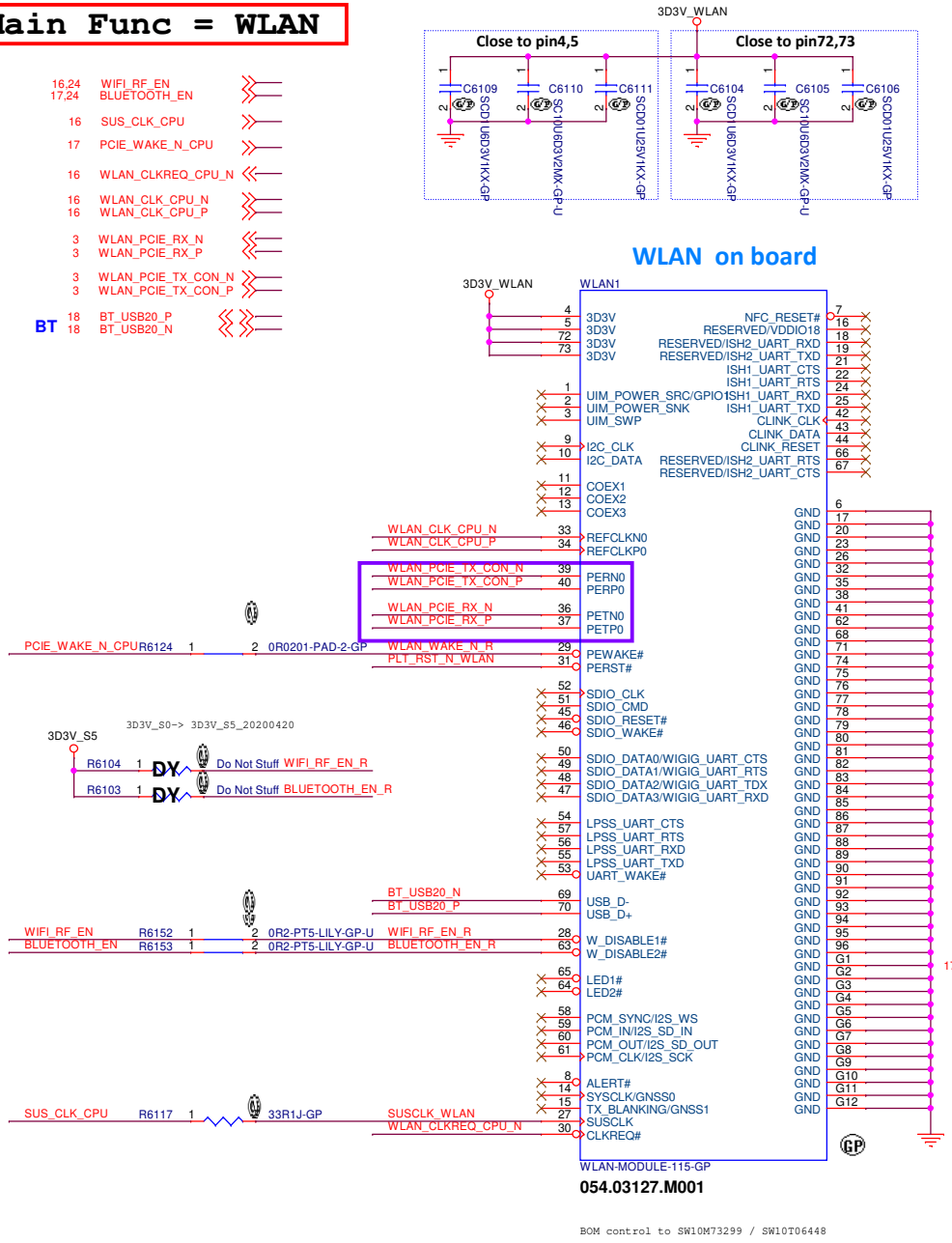
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (RSVD)(HDD/ODD)

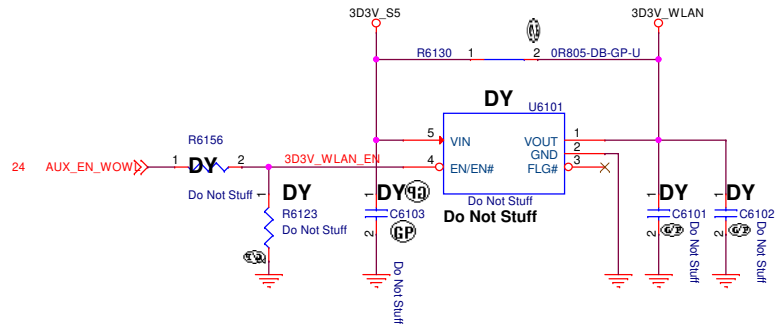
Size	Document Number	Rev
A4	LV550_AMD	-1

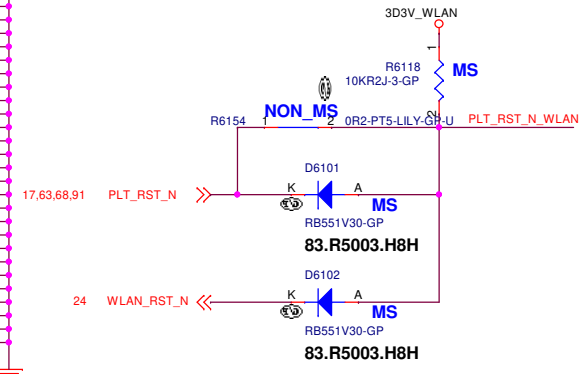
Date: Monday, August 17, 2020 Sheet 60 of 106

Main Func = WLAN



AOAC function circuit





Pin #	Pin Name platform pinout	Pin Name module pinout	Voltage on Card Side	WLAN, BT, or	Connection on Platform/Usage
30	CLKREQ#	CLKREQ#	3.3 V	WLAN	Also support 1.8 V electrical levels on this signal
31	PERST#	PERST#	3.3 V	WLAN	Also support 1.8 V electrical levels on this signal
32	GND	GND			
33	REFCLKN0	REFCLKN0	PCIe phy	WLAN	PCIe phy signals, use phy levels and not digital pins
34	REFCLKP0	REFCLKP0	PCIe phy	WLAN	PCIe phy signals, use phy levels and not digital pins
35	GND	GND			
36	PERn0	PETn0	PCIe phy	WLAN	PCIe phy signals, use phy levels and not digital pins
37	PERp0	PETp0	PCIe phy	WLAN	PCIe phy signals, use phy levels and not digital pins
38	GND	GND			
39	PETn0	PERn0	PCIe phy	WLAN	PCIe phy signals, use phy levels and not digital pins
40	PETp0	PERp0	PCIe phy	WLAN	PCIe phy signals, use phy levels and not digital pins
41	GND	GND			
42	CLINK_CLK	CLINK_CLK	CLINK phy (1 V)	WLAN	CLINK phy
43	CLINK_DATA	CLINK_DATA	CLINK phy (1 V)	WLAN	CLINK phy
44	CLINK_RESET	CLINK_RESET	3.3 V	WLAN	CcP also supports 1.8 V electrical levels on this signal
45	SDIO_RESET# (O)	SDIO_RESET# (I)	NA		Signal not used, leave NC in platform side
46	SDIO_WAKE# (I)	SDIO_WAKE# (O)	NA		Signal not used, leave NC in platform side
47	SDIO_DATA3 (IO)/WIGIG_UART_TXD (O)	SDIO_DATA3 (IO)/WIGIG_UART_RXD (I)	NA		Signal not used, leave NC in platform side
48	SDIO_DATA2 (IO)/WIGIG_UART_RXD (I)	SDIO_DATA2 (IO)/WIGIG_UART_TDX (O)	NA		Signal not used, leave NC in platform side

LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2)

Size: A3 | Document Number: LV550 AMD | Rev: -1

Date: Monday, August 17, 2020 | Sheet 61 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (RSVD)(WWAN)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 62 of 106

Main M.2 SSD

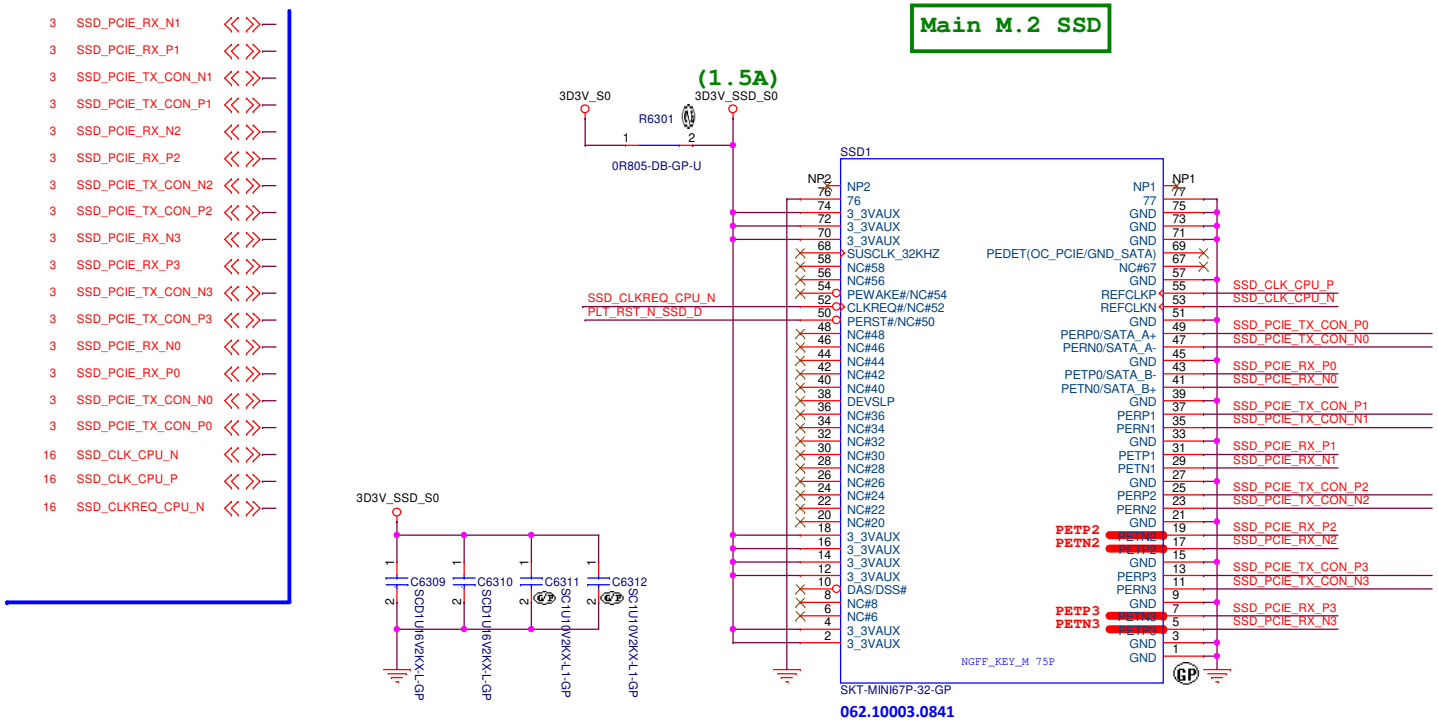
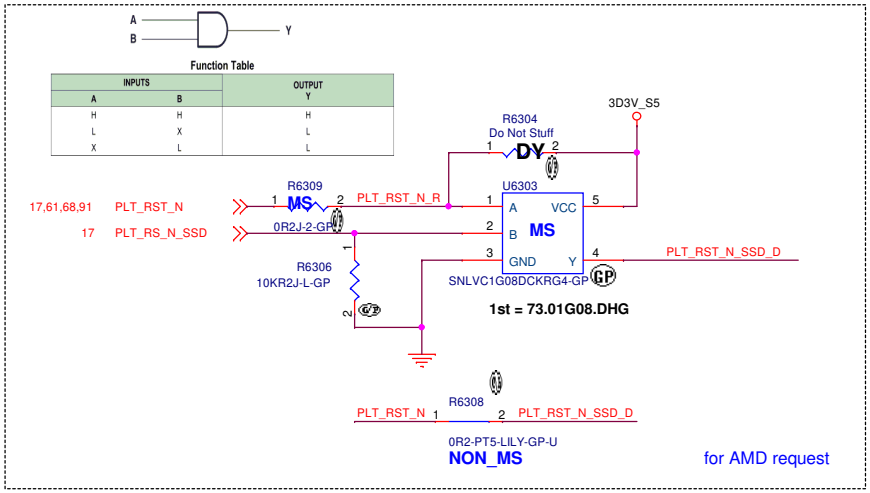
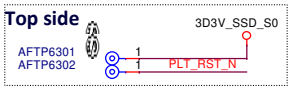


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
		N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1





LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2/ eMMC)

Size: A3 | Document Number: LV550 AMD | Rev: -1

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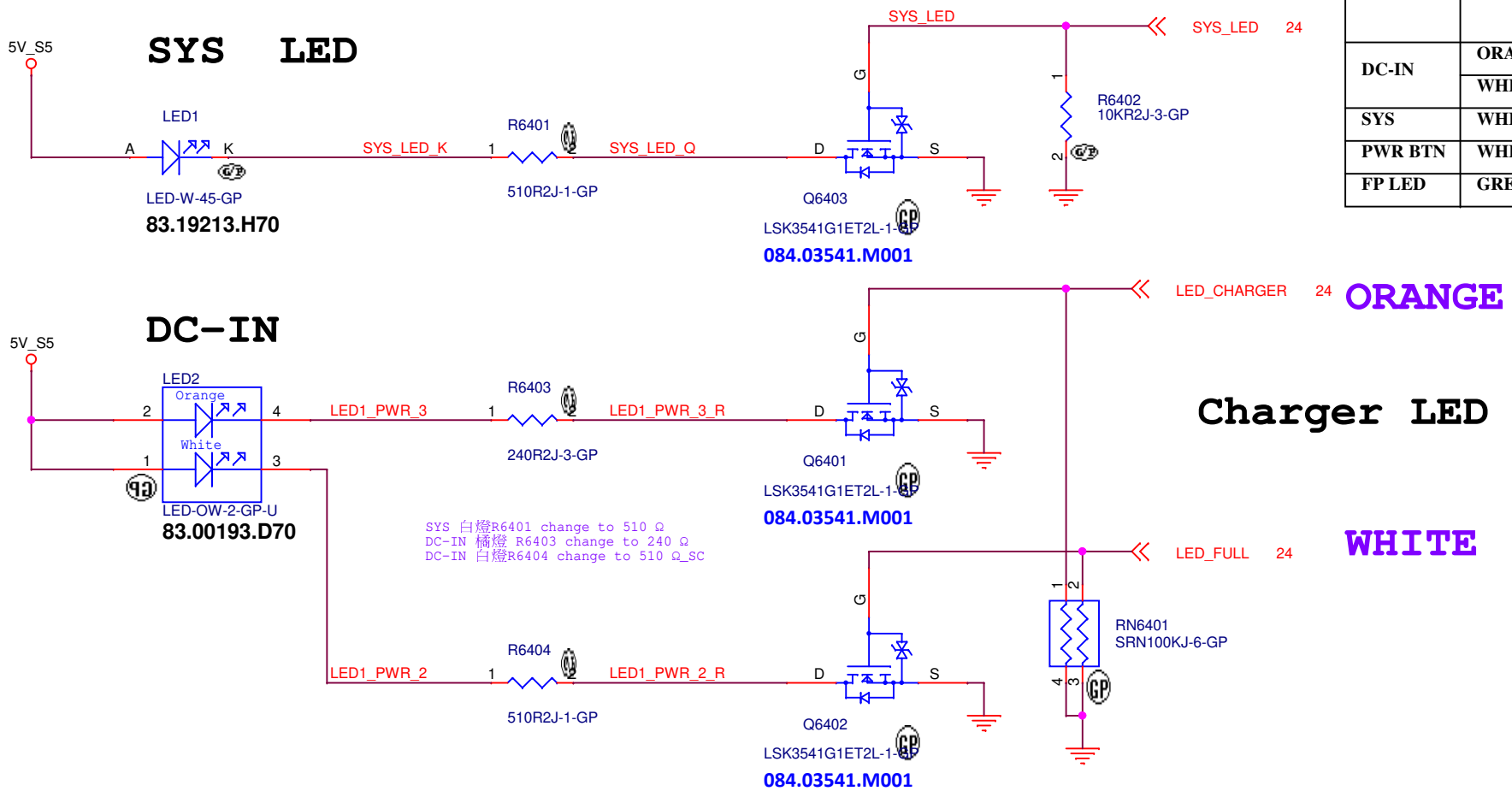
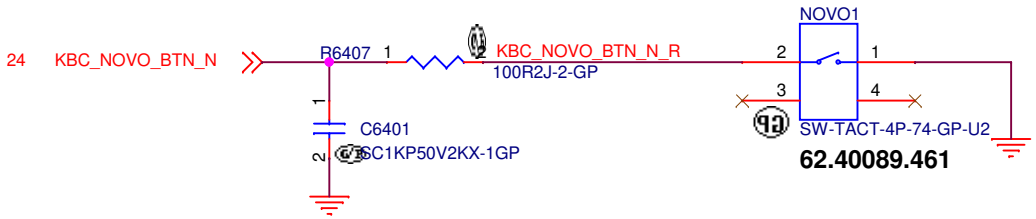
LED

LED resistor

		13'	14'
DC-IN	ORANGE	150 OHM	250 OHM
	WHITE	300 OHM	250 OHM
SYS	WHITE	1.5K OHM	800 OHM
PWR BTN	WHITE	1K OHM	500 OHM
FP LED	GREEN	500 OHM	250 OHM



NOVO BUTTON



LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LED / Button / Power Button*

Size	Document Number	Rev
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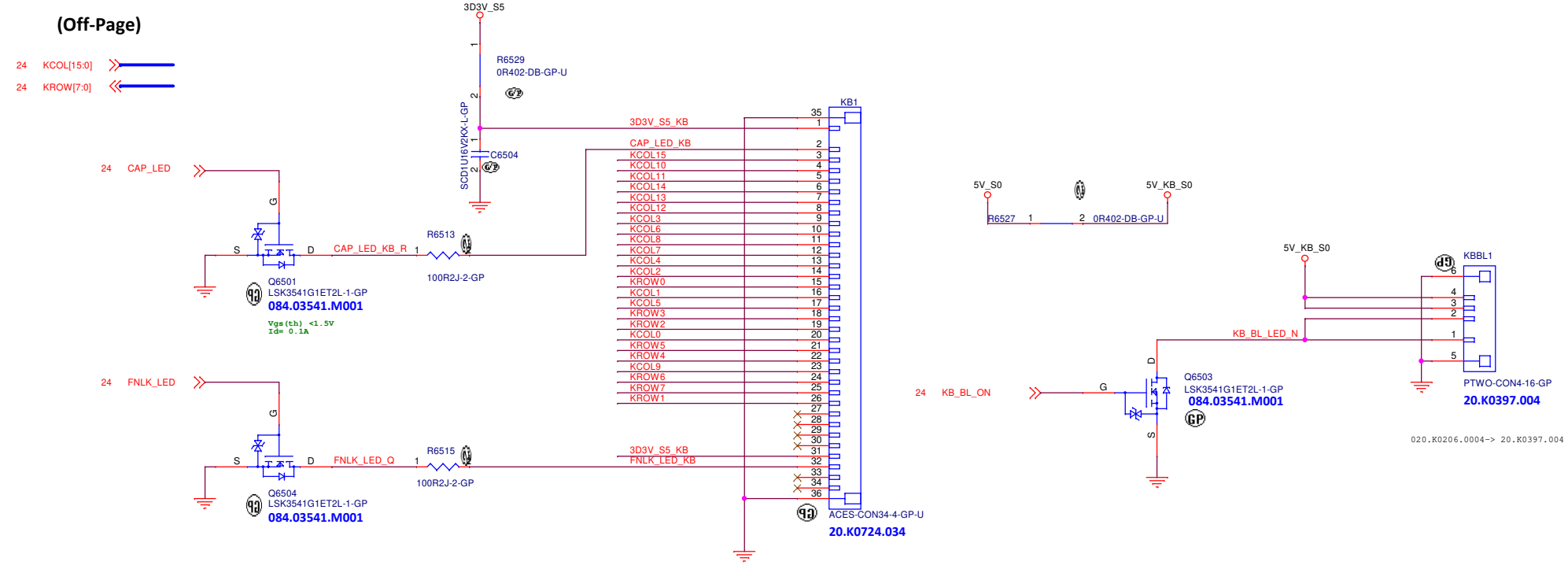

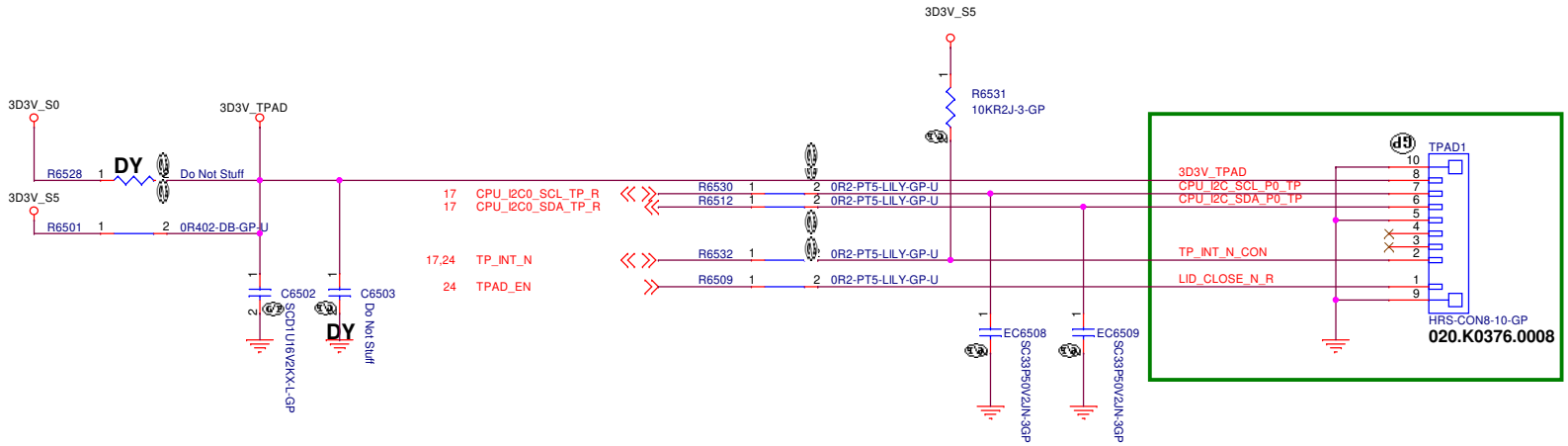

LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (KB/TP)**

Size	Document Number	Rev
A3	LV550 AMD	-1

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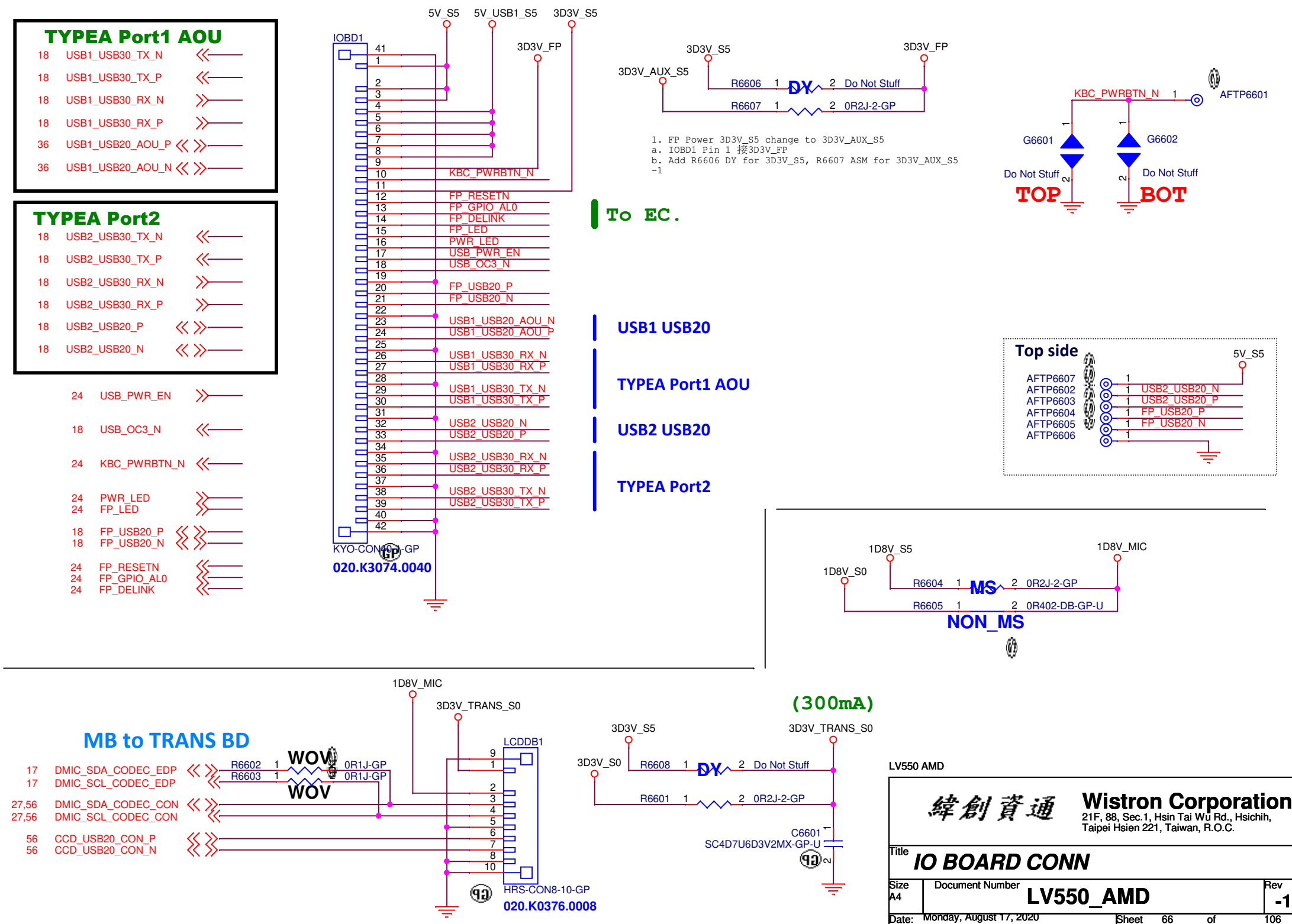
TYPEA Port1 AOU
18 USB1_USB30_TX_N
18 USB1_USB30_TX_P
18 USB1_USB30_RX_N
18 USB1_USB30_RX_P
36 USB1_USB20_AOU_P
36 USB1_USB20_AOU_N
TYPEA Port2
18 USB2_USB30_TX_N
18 USB2_USB30_TX_P
18 USB2_USB30_RX_N
18 USB2_USB30_RX_P
18 USB2_USB20_P
18 USB2_USB20_N
24 USB_PWR_EN
18 USB_OC3_N
24 KBC_PWRBTN_N
24 PWR_LED
24 FP_LED
18 FP_USB20_P
18 FP_USB20_N
24 FP_RESETN
24 FP_GPIO_AL0
24 FP_DELINK
5V_S5
5V_USB1_S5
3D3V_S5
3D3V_FP
IOBD1
KBC_PWRBTN_N
FP_RESETN
FP_GPIO_AL0
FP_DELINK
FP_LED
PWR_LED
USB_PWR_EN
USB_OC3_N
FP_USB20_P
FP_USB20_N
USB1_USB20_AOU_N
USB1_USB20_AOU_P
USB1_USB30_RX_N
USB1_USB30_RX_P
USB1_USB30_TX_N
USB1_USB30_TX_P
USB2_USB20_N
USB2_USB20_P
USB2_USB30_RX_N
USB2_USB30_RX_P
USB2_USB30_TX_N
USB2_USB30_TX_P
KYO-CON42-GP
020.K3074.0040
To EC.
USB1 USB20
TYPEA Port1 AOU
USB2 USB20
TYPEA Port2
3D3V_AUX_S5
R6606 1 DY 2 Do Not Stuff
R6607 1 2 0R2J-2-GP
1. FP Power 3D3V_S5 change to 3D3V_AUX_S5
a. IOBD1 Pin 1 接3D3V_FP
b. Add R6606 DY for 3D3V_S5, R6607 ASM for 3D3V_AUX_S5
-1
KBC_PWRBTN_N
AFTP6601
G6601
G6602
Do Not Stuff
TOP
BOT
Top side
AFTP6607
AFTP6602
AFTP6603
AFTP6604
AFTP6605
AFTP6606
USB2_USB20_N
USB2_USB20_P
FP_USB20_P
FP_USB20_N
1D8V_S5
1D8V_S0
1D8V_MIC
R6604 1 MS 2 0R2J-2-GP
R6605 1 2 0R402-DB-GP-U
NON_MS
MB to TRANS BD
17 DMIC_SDA_CODEC_EDP
17 DMIC_SCL_CODEC_EDP
27,56 DMIC_SDA_CODEC_CON
27,56 DMIC_SCL_CODEC_CON
56 CCD_USB20_CON_P
56 CCD_USB20_CON_N
R6602 1 WOV 2 0R1J-GP
R6603 1 WOV 2 0R1J-GP
1D8V_MIC
3D3V_TRANS_S0
LCDDB1
HRS-CON8-10-GP
020.K0376.0008
(300mA)
3D3V_S5
3D3V_S0
3D3V_TRANS_S0
R6608 1 DY 2 Do Not Stuff
R6601 1 2 0R2J-2-GP
C6601
SC4D7U6D3V2MX-GP-U
LV550 AMD
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
IO BOARD CONN
Size
A4
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LV550_AMD
Rev
-1
Date: Monday, August 17, 2020
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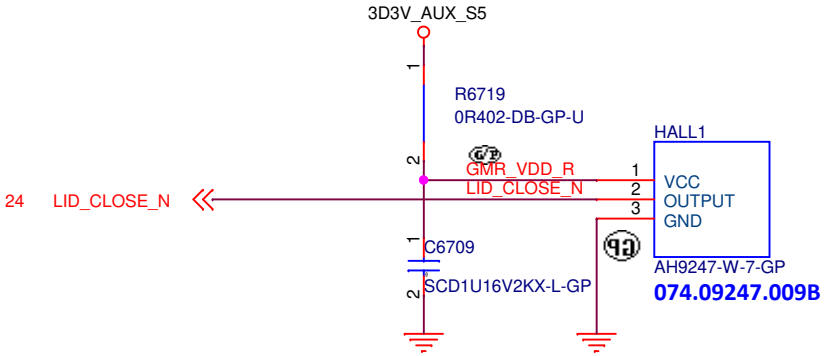

LV550 AMD

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***SENSOR (HALL-SENSOR)***

Size	Document Number	Rev
A4	LV550_AMD	-1

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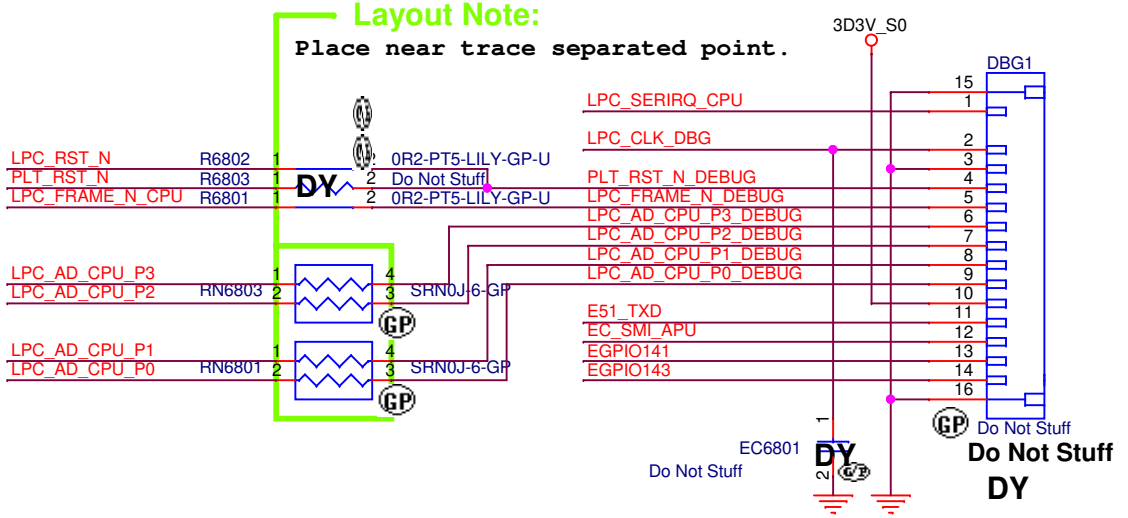
SSID = DEBUG PORT

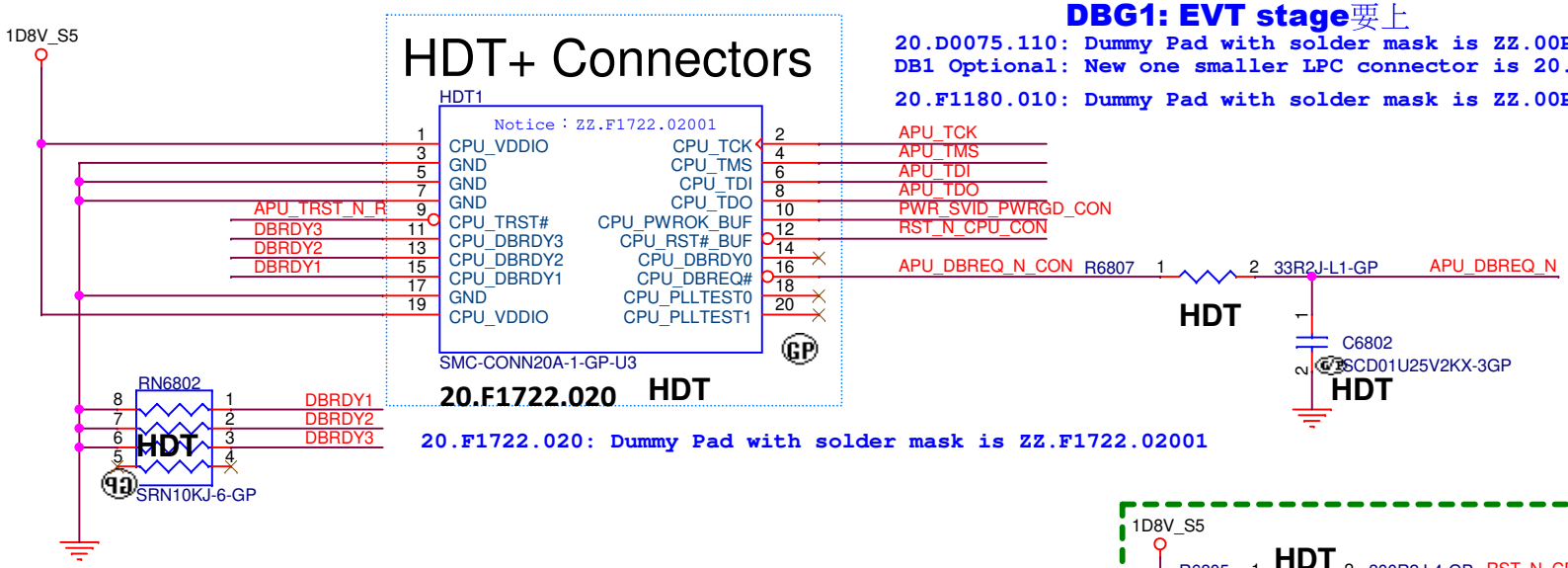
16,24 LPC_AD_CPU_P0
16,24 LPC_AD_CPU_P1
16,24 LPC_AD_CPU_P2
16,24 LPC_AD_CPU_P3
16,24 LPC_FRAME_N_CPU
16,24,91 LPC_RST_N
17,61,63,91 PLT_RST_N
16 LPC_CLK_DBG
8 APU_TCK
8 APU_TMS
8 APU_TDI
8 APU_TDO
8,46 PWR_SVID_PWRGD
8,72 RST_N_CPU
8 APU_DBREQ_N
8 APU_TRST_N
24 E51_TXD
16 EGPIO141
16 EGPIO143
16,24 LPC_SERIRQ_CPU
16 EC_SMI_APU

Debug Connector

Layout Note:
Place near trace separated point.



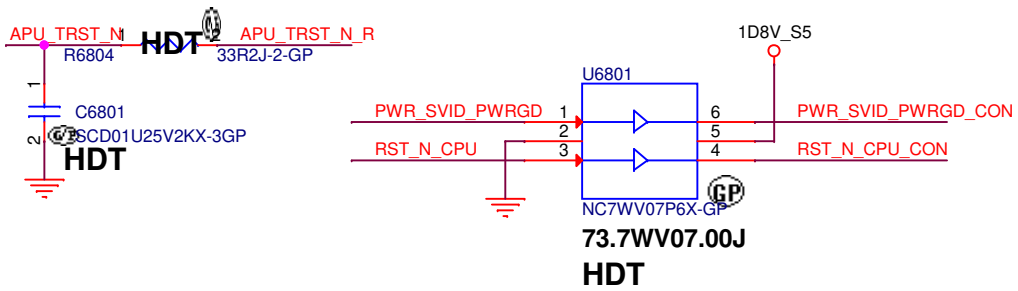
HDT+ Connectors

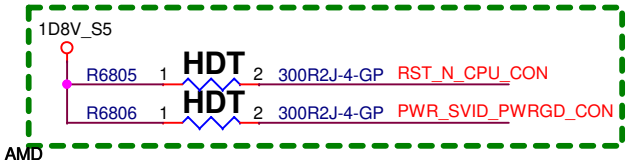


DBG1: EVT stage要上

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.
20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

20.F1722.020: Dummy Pad with solder mask is ZZ.F1722.02001





LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (LPC/HDT)

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A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor (RSVD) (GYROSCOPE/PRESSUE

Size	Document Number	Rev
A4	LV550_AMD	-1

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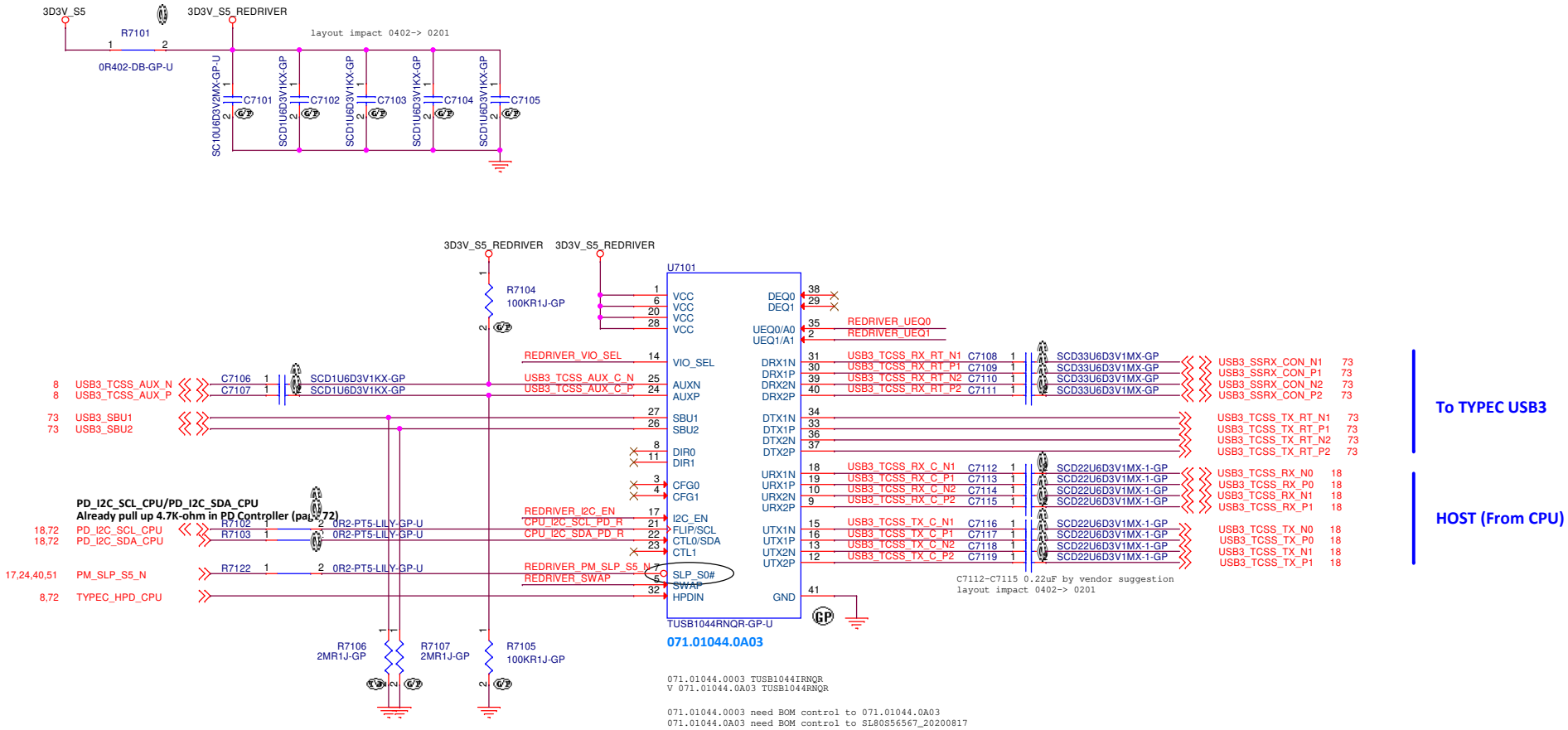
LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

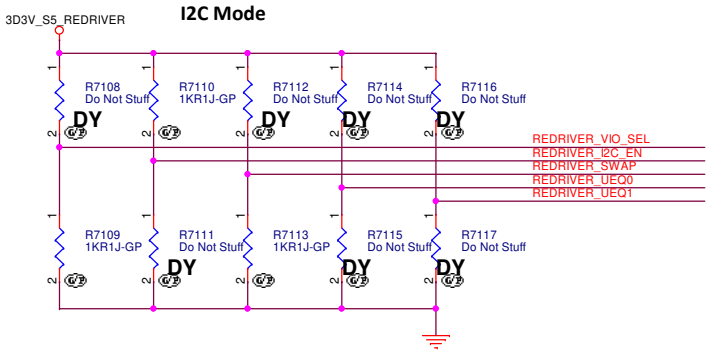
Title: *Sensor (G-sensor)(RSVD)*

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 70 of 106



I2C Mode



I2C_EN: 1=I2C enabled
VIO_SEL: 0 = 3.3-V configuration I/O voltage, 3.3-V I 2C interface (Default)
SWAP: 0 - Do not swap channel directions and EQ settings (Default)

UEQ0/A0 and UEQ1/A1:FF

LV550 AMD

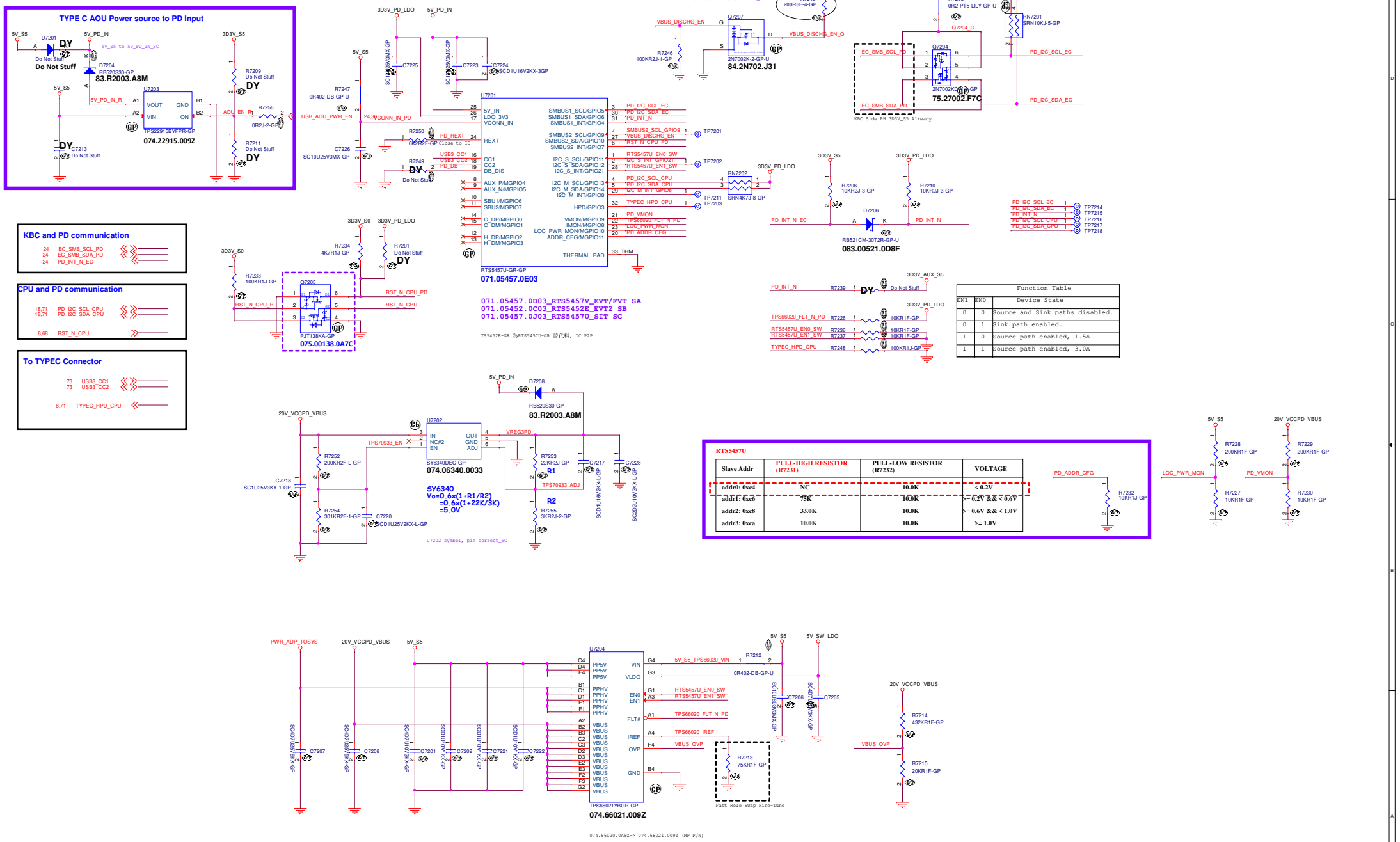
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RYPE-C RE TIMER(1/2)**

Size	Document Number	Rev
A3	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 71 of 106

USB Port3, Type C_USB3.0, PD



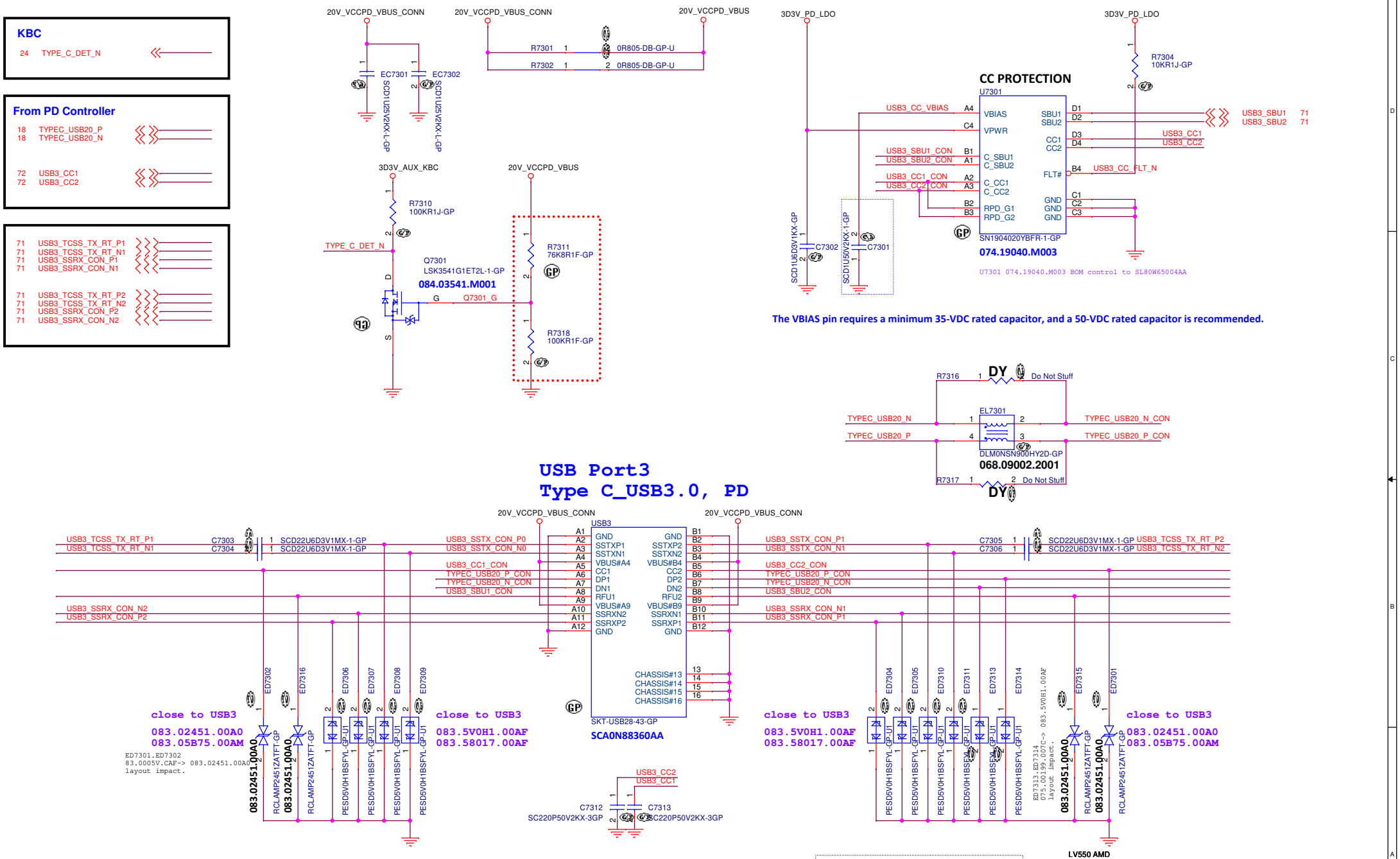
LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TypeC Controller-1)

Size: A2 | Document Number: LV550 AMD | Rev: -1

Date: Monday, August 17, 2020 | Sheet 72 of 106



LV550 AMD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (TypeC Conn/Protect)***

Size	Document Number	Rev
A3	LV550 AMD	-1

Date: Monday, August 17, 2020 Sheet 73 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TBT Re-Timer-2 RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 74 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **EXT IO (TypeC Controller-2 RSVD)**

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (PEG 1/5)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 76 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (DIGITAL 2/5)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 77 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (VRAM 3/5)

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (GPIO 4/5)

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (PWR/GND 5/5)

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 82 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: GPU (RSVD) (Power_VGA_CORE)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 85 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD) (Power_others)*

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 86 of 106

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (EE_Power)

Size	Document Number	Rev
A4	LV550_AMD	-1

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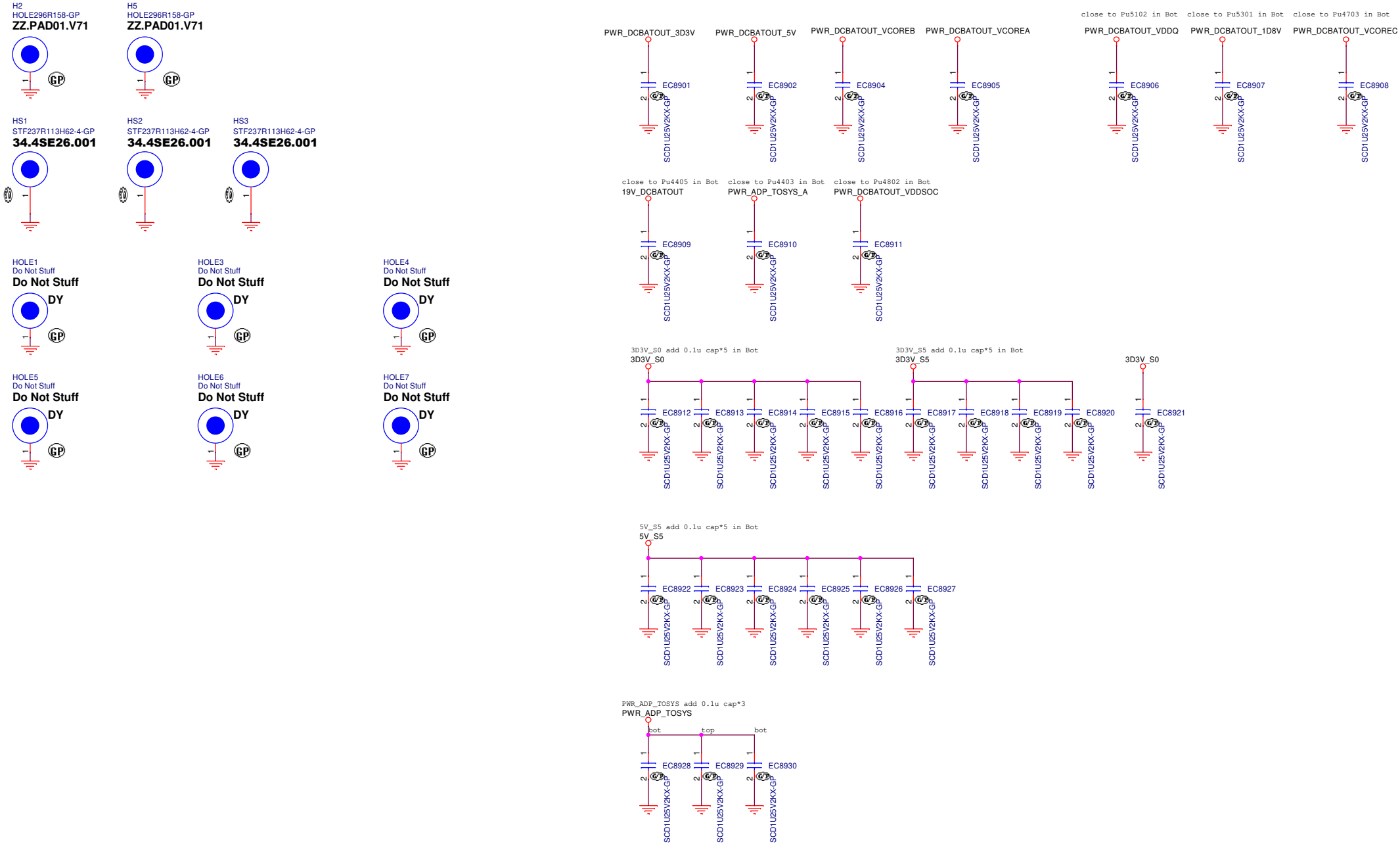
LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (Discharge/Sequence)

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 88 of 106



LV550 AMD

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **UNUSED PARTS (RF/EMI Capacitors)**

Size	Document Number	Rev
A3	LV550 AMD	-1

Date: Monday, August 17, 2020 Sheet 89 of 106

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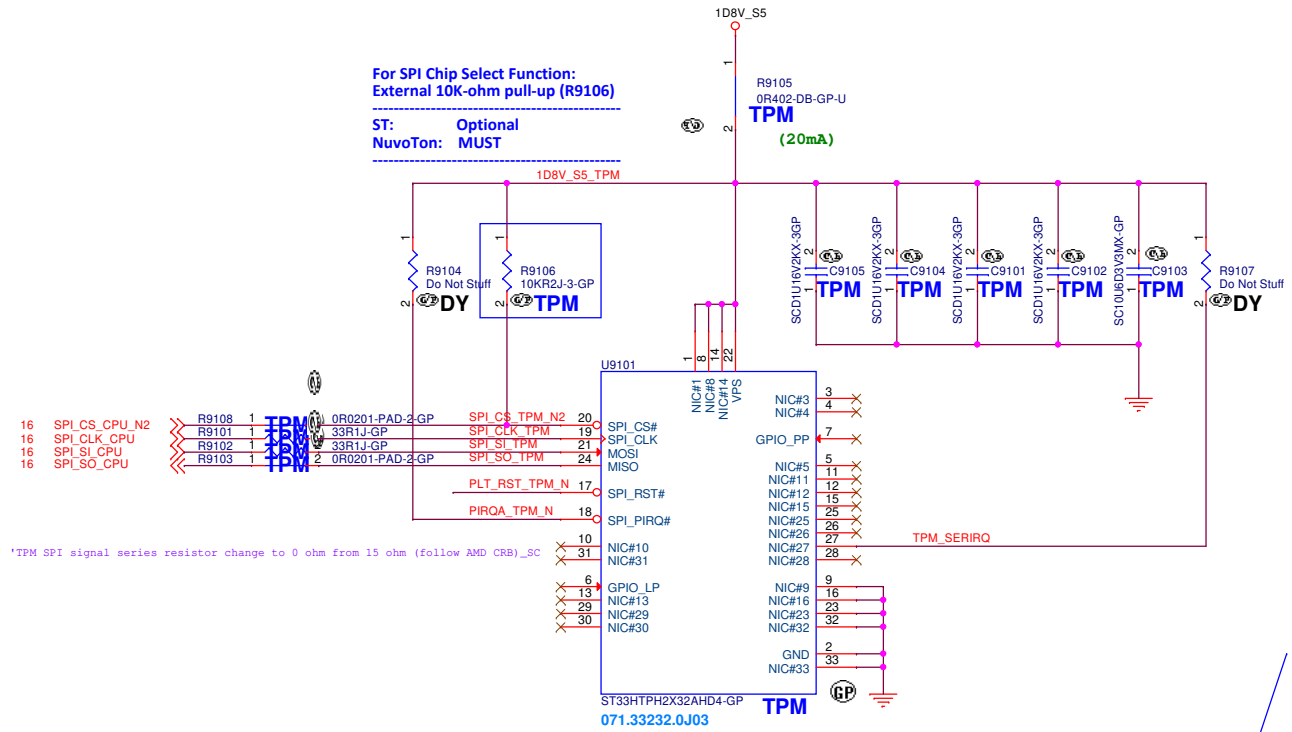
LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(RESERVED)*

Size	Document Number	Rev
A4	LV550_AMD	-1

Date: Monday, August 17, 2020 Sheet 90 of 106



For SPI Chip Select Function:
External 10K-ohm pull-up (R9106)

ST: Optional
NuvoTon: MUST

SPI Chip Select Pin:
ST (SPI_CS#) Internal pull-up
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

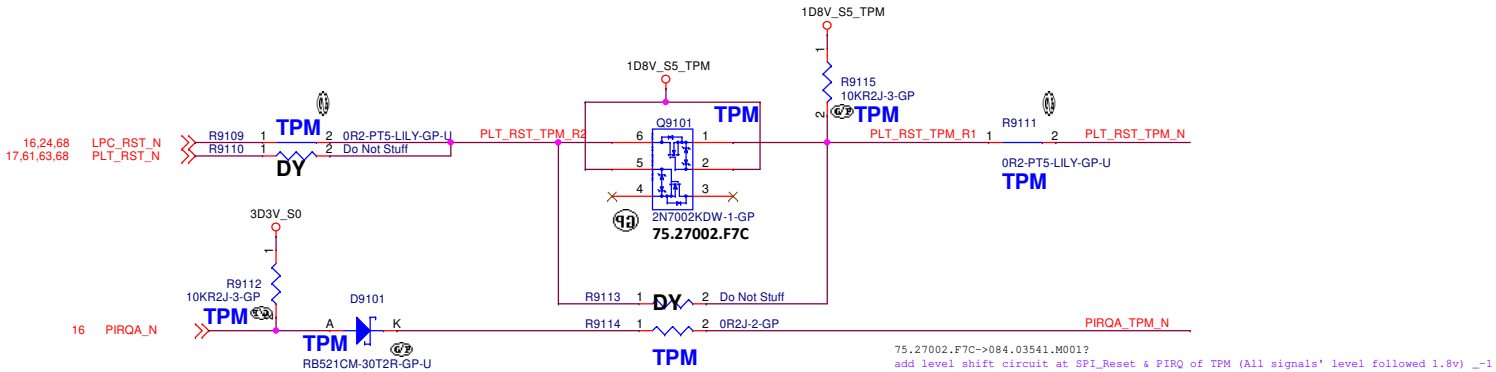
TPM TABLE

1st	ST33HTPH2X32AHD4	071.33232.0J03	SL80X01013AA
2nd	NPCT750LADYX	071.00750.0H03	

Nuvoton TPM FW: 7.2.1.0 part will be dropped, and instead by new one_20200603
NuvoTon PNLenovo PNTPM FW
NPCT750LADYXSL80W591227.2.2.0
NPCT750LABYXSL80R401587.2.1.0

TABLE

Pin No	TCG PTP Spec(V38)	ST ST33HTPH2X32AHD4 071.33232.0J03	NuvoTon NPCT750LADYX 071.00750.0H03	~~071.09670.0I03~~ Infineon SLB9670VQ2.0 FW7.63
1	VDD	NC	VSB	VDD
2	GND	GND	NC	GND
3	NC	NC	NC	NC
4	GPIO	NC	GPIO/PP	NC
5	NC	NC	NC	NC
6	GPIO	GPIO_LP	GPIO3	GPIO
7	GPIO	GPIO_PP	NC	PP
8	VDD	NC	VHIO	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	NC	GPIO4	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	NC
17	SPI_RST#	SPI_RST#	RST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	NC	SDA/GPIO0	NC
30	SDA/GPIO0	NC	SCL/GPIO1	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND



LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (TPM)**

Size: A3 | Document Number: **LV550 AMD** | Rev: -1

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LV550 AMD

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	***INT IO (FP) (RSVD)***	
Size A4	Document Number **LV550_AMD**	Rev **-1**
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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TYPEC_DP_RTS5455

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TYPEC_PD_Controller

Size	Document Number	Rev
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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size	Document Number	Rev
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LV550 AMD

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size	Document Number	Rev
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LV550 AMD

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size	Document Number	Rev
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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Debug (RSVD)(XDP debug)*

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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size	Document Number	Rev
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LV550 AMD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
A4	LV550_AMD	-1

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LV550 AMD

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Power Sequence

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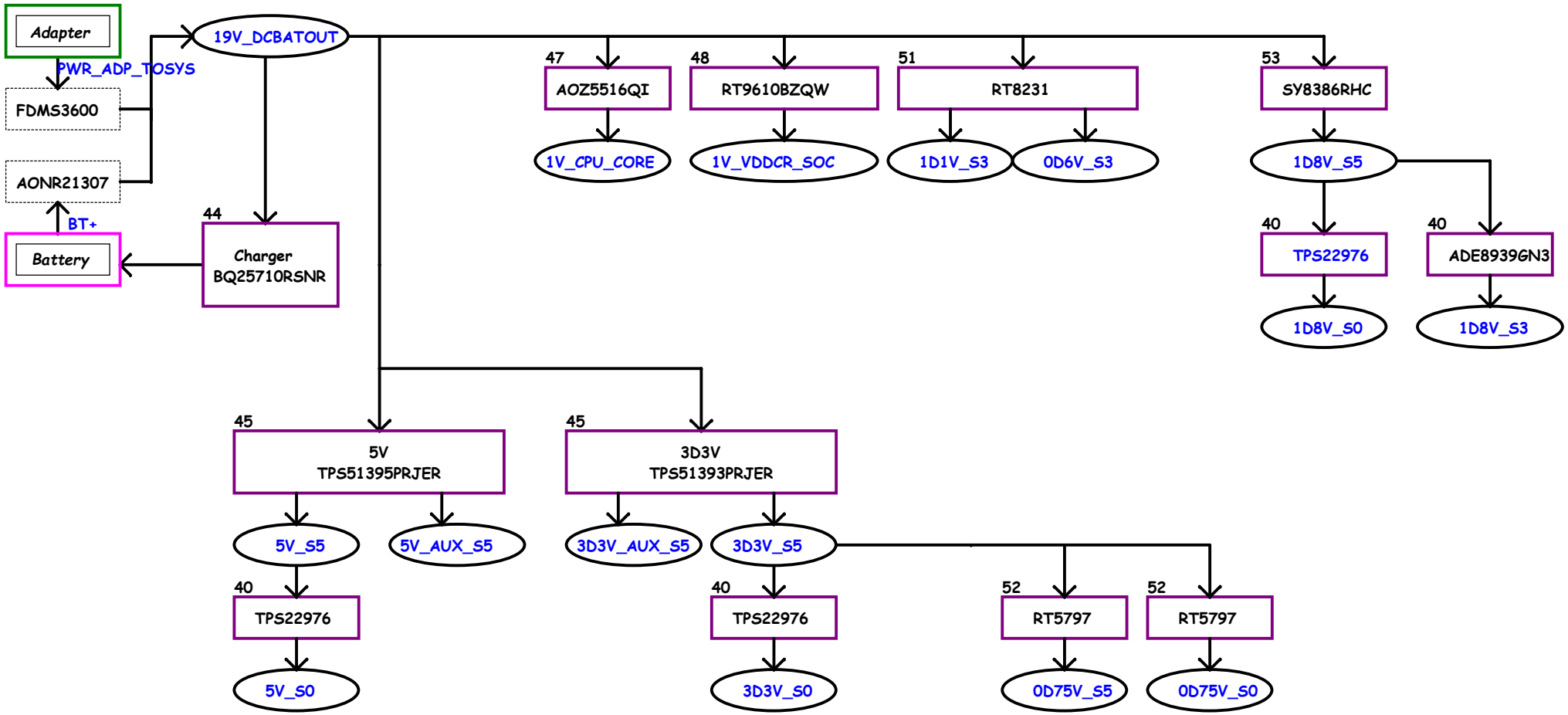

LV550 AMD

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	LV550 AMD	-1

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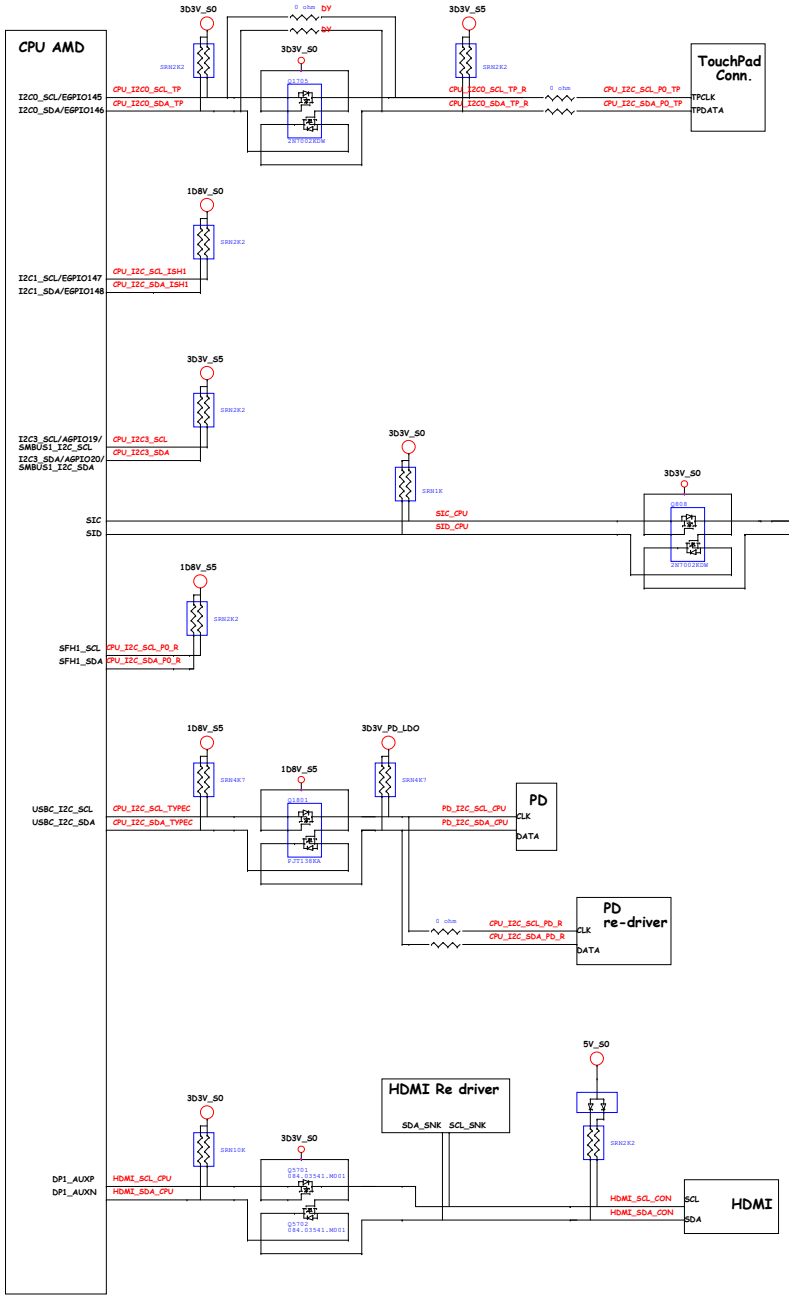
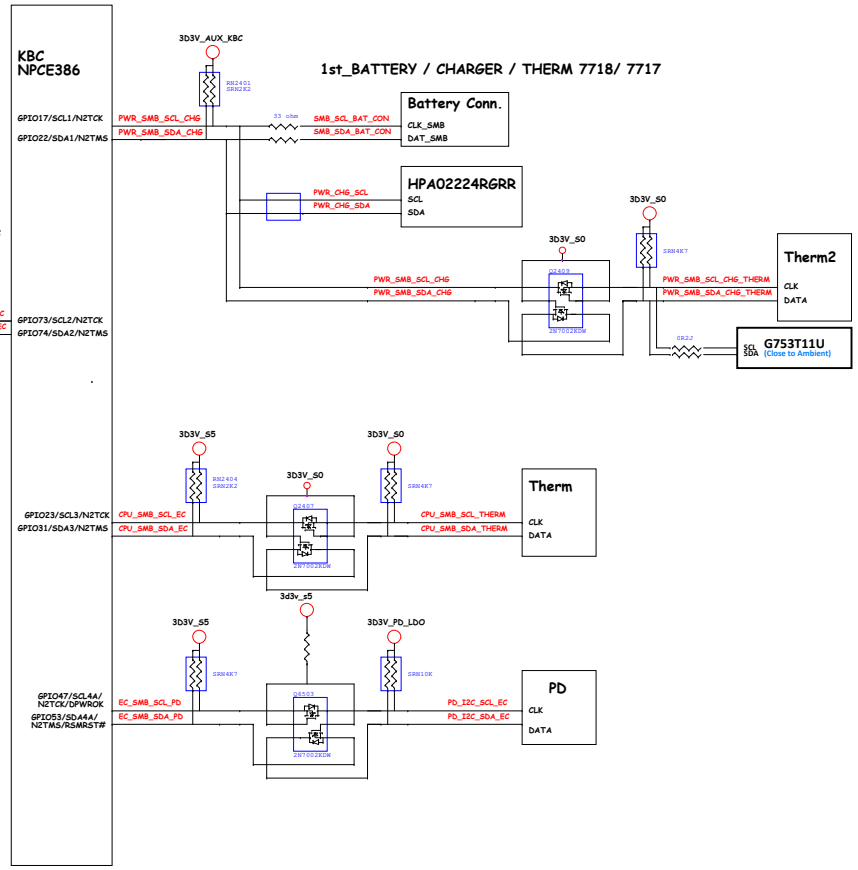
PCH SMBus Block Diagram



KBC SMBus Block Diagram



LV550 AMD

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS/I2C BLOCK DIAGRAM

Size	Document Number	Rev
A1	LV550 AMD	-1

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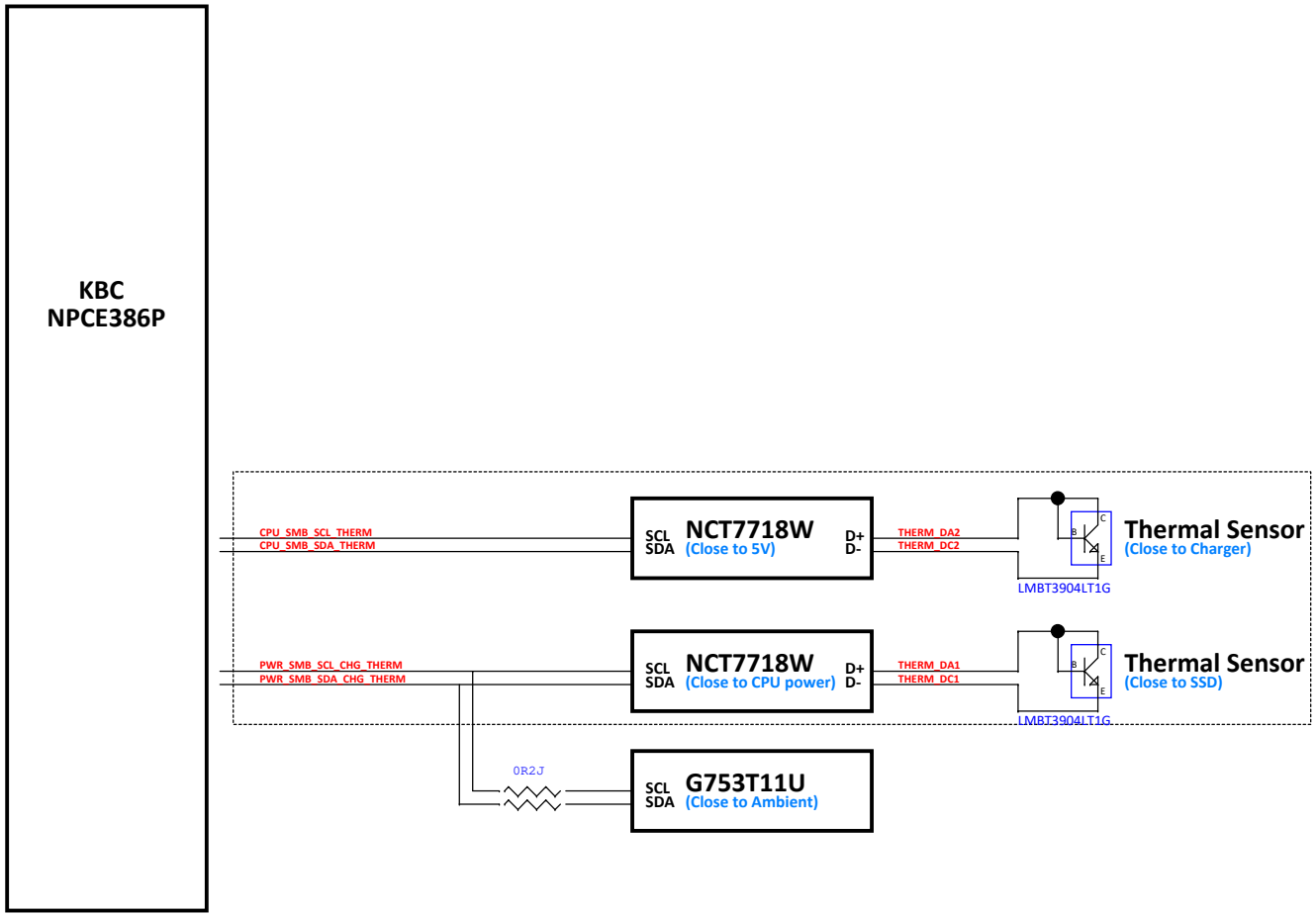
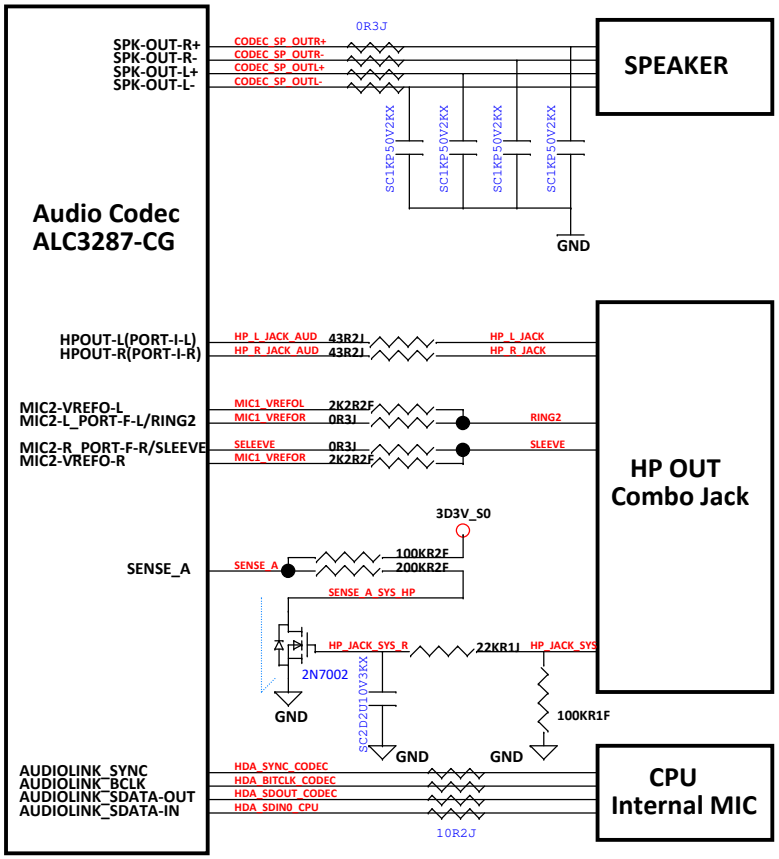
Thermal Block Diagram



Audio Block Diagram



LV550 AMD

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/AUDIO BLOCK DIAGRAM

Size	Document Number	Rev
A3	LV550 AMD	-1

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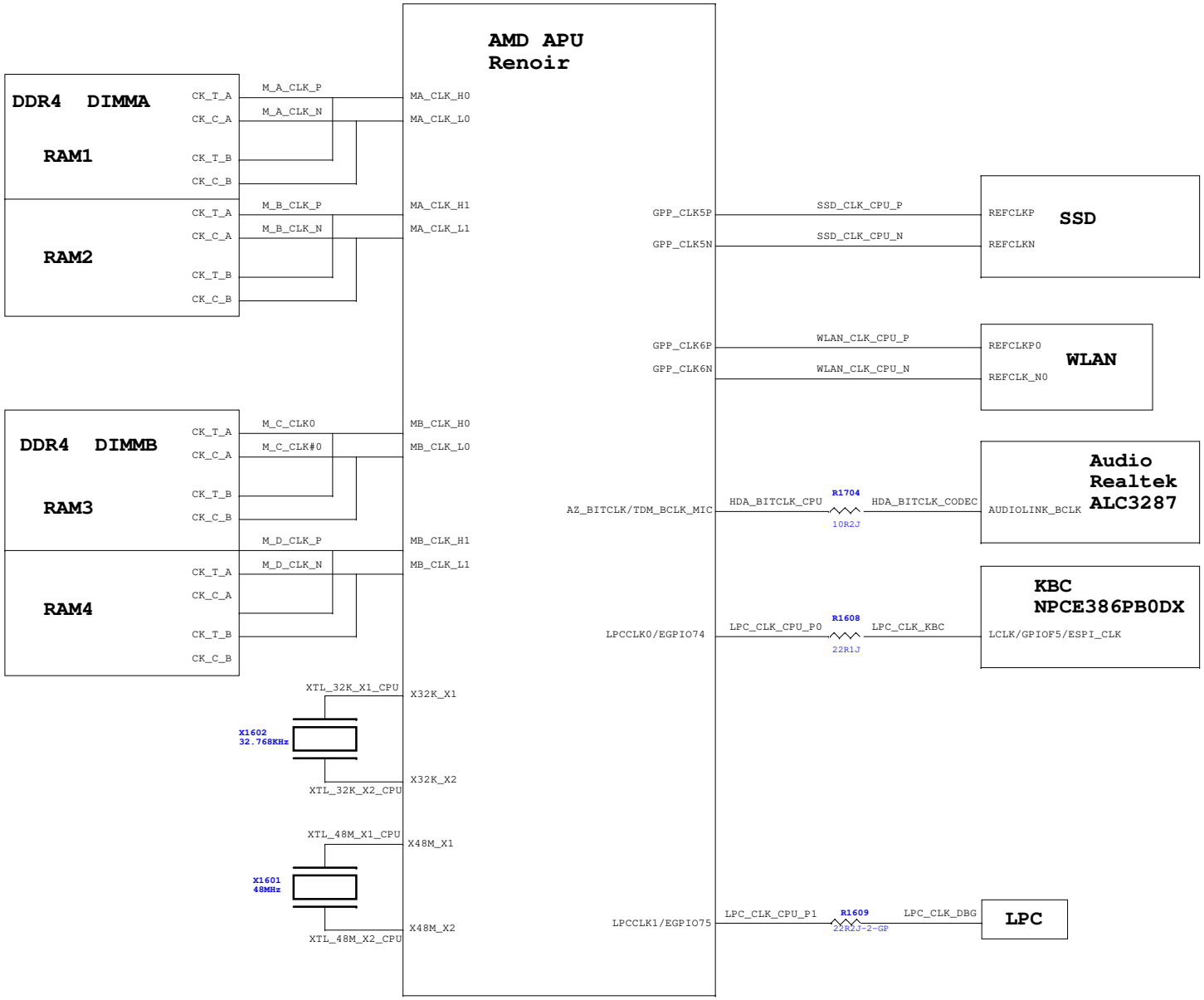
CLK Block Diagram



LV550 AMD

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CLK Block	
Size A2	Document Number LV550 AMD	Rev -1
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