UX562FD SCHEMATIC Revision 2.0

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50	FRAME BUFFER-A(3)++
51	FRAME BUFFER-B(4)++
52	VGA_CRT/LVDS(5)++
53	VGA_GPIO/DVI/DP(6)++
54	VGA_STRAP&PINS(7)++
55	VGA_PWG/GND(8)++
56	VRAM CH
80	PW_KABY LAKE-U(1)
81	PW_KABY LAKE-U(2)
83	PW_+1.05VSUS / +1.8VSUS
84	PW_+1.5VS
86	PW_+1.2V/+VTT/+2.5V
87	PW_+3VADSW/+5VSUS
88	LOAD SWITCH
89	PW_CHARGER
90	PW_PROTECTION
91	PW_+NVVDD (RT8819 2Phase)
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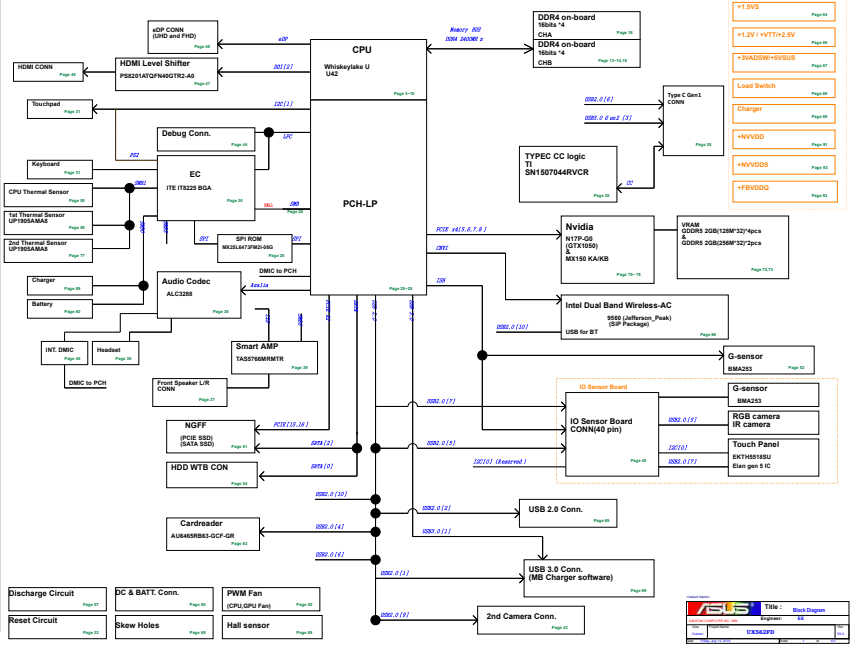
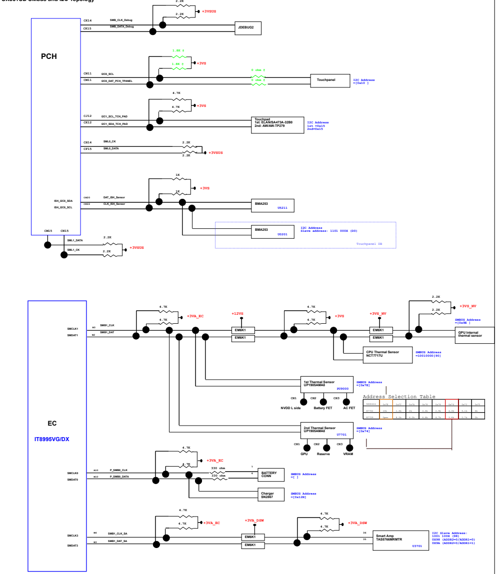
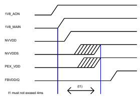
BLOCK DIAGRAM



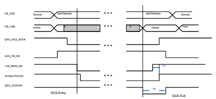
UX561UD SMbus and I2C Topology



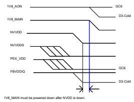
GPU Power Up Power Rail Sequence

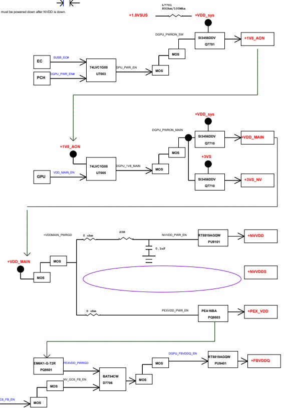


GC6 2.1 Entry/Exit Timing



GPU Power Down Sequence





<Variant Name>

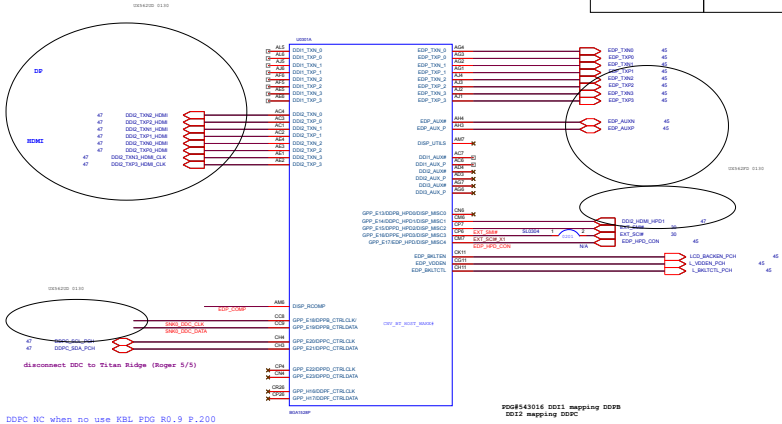
ASUS	Title :	SKU TABLE
	Engineer:	EE
Size: Custom	Project Name: UX562FD	Rev: R2.0
Date: Friday, July 13, 2018	Sheet 103	of 103

Main Board

Display Port

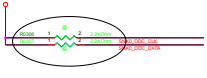
A	EDP
B	Type C(DP)
C	HDMI

Intel Version	ASUS P/N
ES-0	01001-01540000



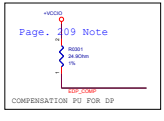
DDPC NC when no use KBL PDG R0.9 P.200

DDI Enable pull up. Disable NC.



	HDMI
DDI_0	Lane2
DDI_1	Lane1
DDI_2	Lane0
DDI_3	CLK

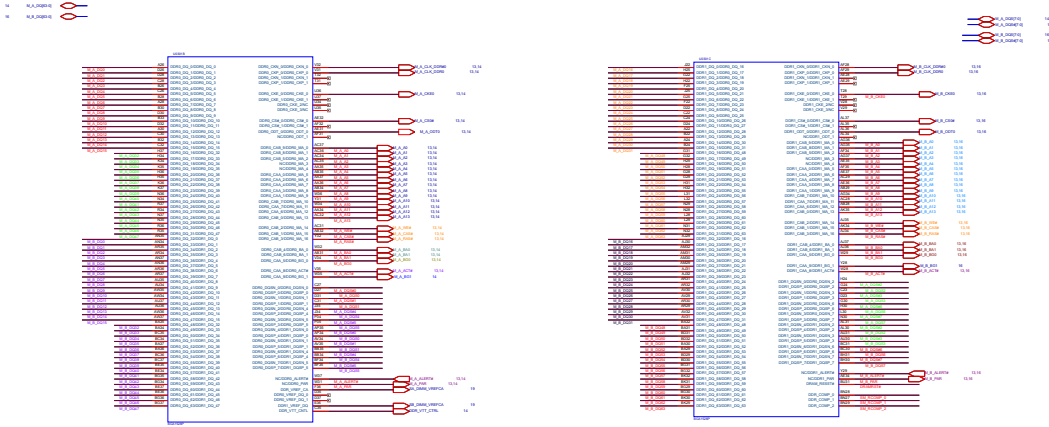
PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPC

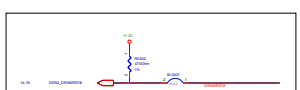


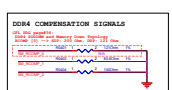
<Variant Name>

ASUS	Project Name: UX5623FD		Rev: 0.2.0
Title : CPU_DISPLAY			
Size: Custom	Dept.: MB1-RD3E01	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet 3 of 102		

Non-Interleaved

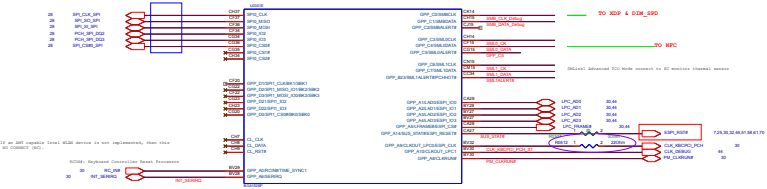


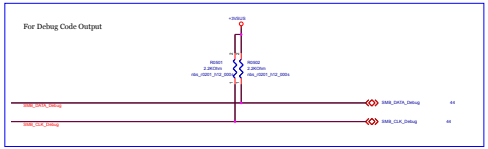


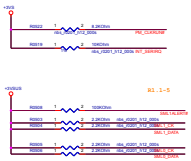


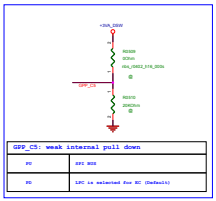
Variant Name:			
Title :	CPU DDR4		
Engineer:	Ryan_Chang		
Size	Project Name		Rev
A1	UX562FD		REV.0
Date: Friday, July 19, 2019		Sheet 2 of 32	

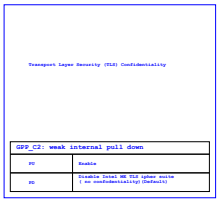
Main Board

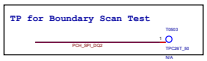






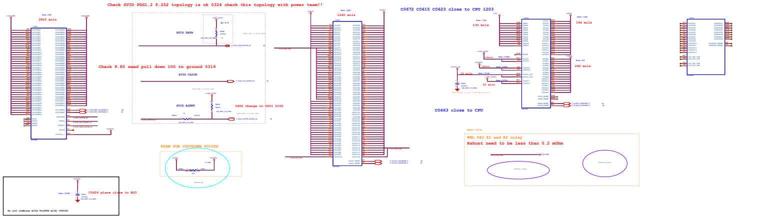






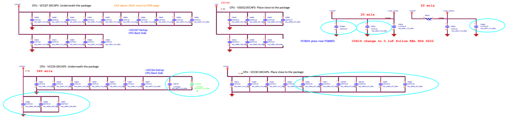
<Variant Name>

ASUS	Project Name: UX562FD		Rev: R2.0
Title :	CPU_LPC,SPI,SMB,CLINK		
Size: Custom	Dept.: MH-RD3&51	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet 9 of 102		

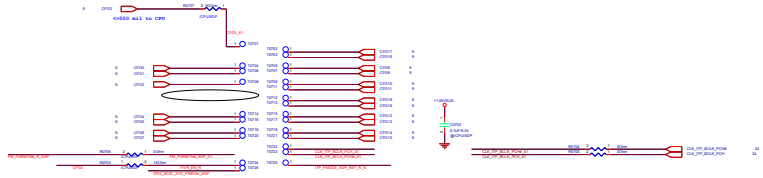


Power Plane:

+VCCCORE		
+VCCSA	System Agent power rail	
+VCCGT	Sliced graphics power rail	
+1.0V_VCCPLL=+VCCST	CPU PLL power rails	
+VCCIO_CPU=+VCCIO=+VCCSTG	IO power rail	Gated version of VCCST
+VCCPLL_OC=+1.2V	CPU digital PLL power rails	
+VDDQ_CPU=+1.2V	CPU Memory power rail, voltage dependent on memory technology	
+VCCST	Sustain voltage for processor in Standby modes	
+VCC_EDRAM_EOPIO		
+VCC_EDRAM_1P8		

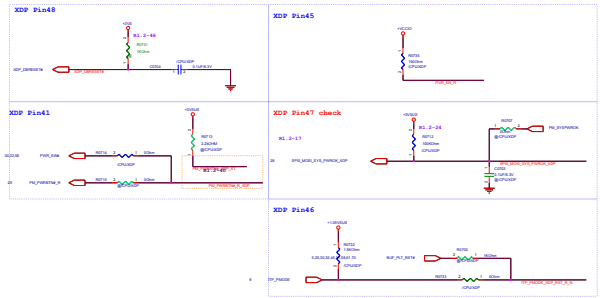


CPU XDP connector

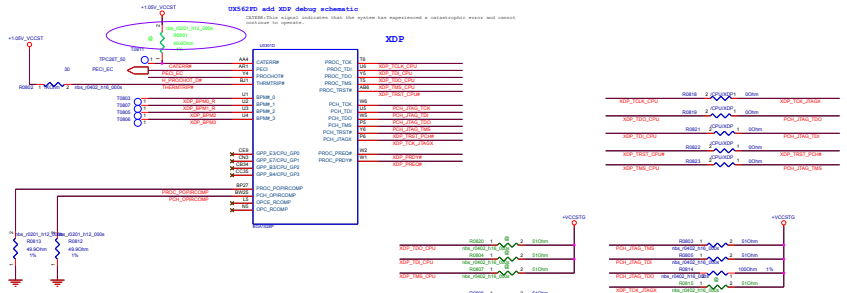


If need to provide system with XDP function to Intel, please unmount R0706/R0707

<<SIO will to CPU>>

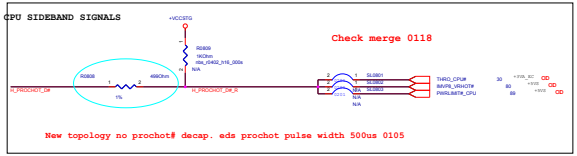


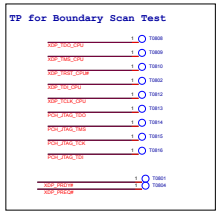
Main Board



On Package Cache resistance Compensation
from processor: Refer to the appropriate platform
design guide for implementation details and values.
Unconnected for Processors without OPC.

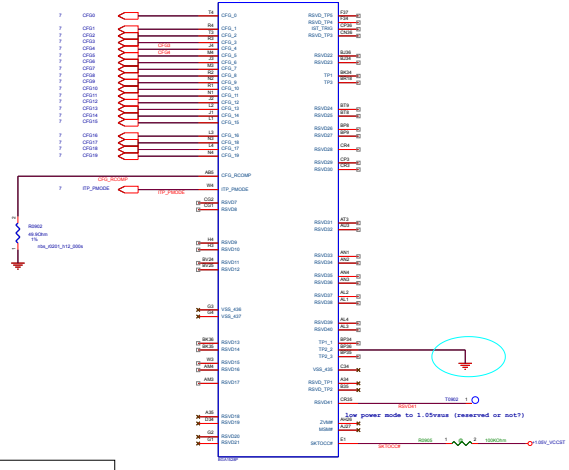
No OPC Check remove 且R0811 R0810量測兩端為0V 0126





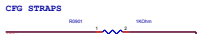
Project Name: UX562FD			Rev: 0.2.0
Title: CPU_MISC,JTAG,CLK			
Size: B	Dept.: MBH RD3&E1	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet: 8	of: 102	

Main Board



TP for Boundary Scan Test

CFG STRAPS



	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

<Variant Name>

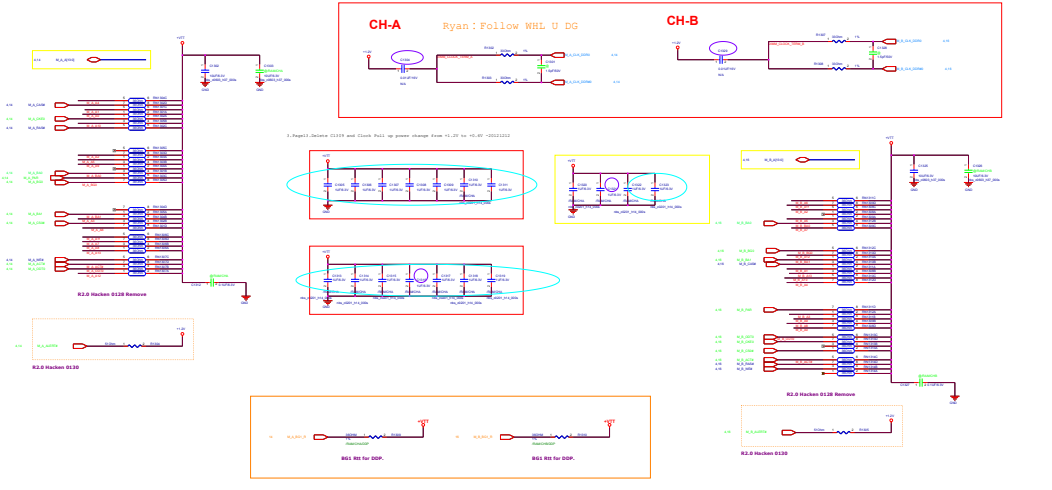
ASUS Project Name: UX562FD Rev: RSVD

Title : CPU_CFG,RSVD

Size: Custom Dept.: MH-RD3E01 Engineer: Ryan_Chang

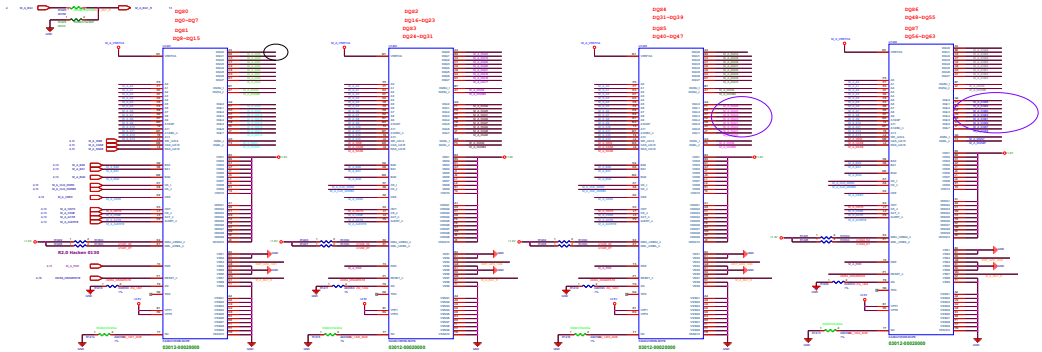
Date: Friday, July 13, 2018 Sheet 9 of 102

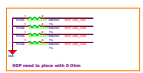
Project Name: UX562FD			Rev: 92.0
Title : CPU_POWER_CAP			
Size: B	Dept.: NB1-RCSE1	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet 92 of 102		

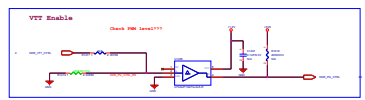


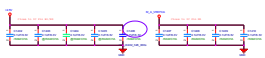
待確認...

Title :	DDR3 TERMINATION
Engineer:	Ryan_Chang
Size:	Custom
Project Name:	1255GDFD
Rev:	0x01
Date:	2012-01-13 2012
Sheet	13 of 37

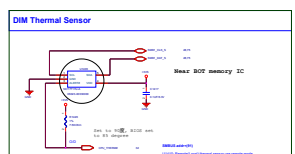

dq0
dq0~dq7
dqs1
dq8~dq15
dq2
dq16~dq23
dqs3
dq24~dq31
dq6
dq32~dq39
dqs5
dq40~dq47
dq8
dq48~dq55
dqs7
dq56~dq63
R2.0 Hades 0128
820-00020000
820-00020000
820-00020000
820-00020000

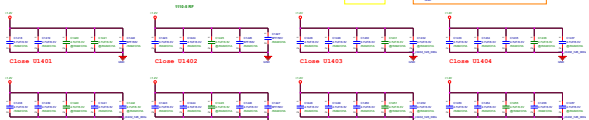

RDP need to place with 0 Ohm


VTT Enable
Check PMU level???




EMI & RF


DIM Thermal Sensor
Near BOT memory IC


Close U1401
Close U1402
Close U1403
Close U1404
Close U1401
Close U1402
Close U1403
Close U1404


Title :
Ryan_Chang

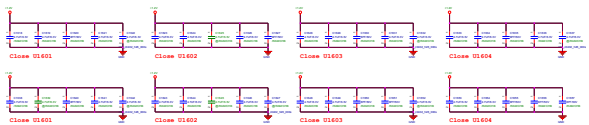

dq0
dq0~dq7
dq1
dq8~dq15
R2.0 Radeon E130
E3012-00020000
dq2
dq16~dq23
dq24
dq32~dq39
dq3
dq24~dq31
dq5
dq40~dq47
dq6
dq48~dq55
dq7
dq56~dq63


R2.0 Radeon E128

待確認...

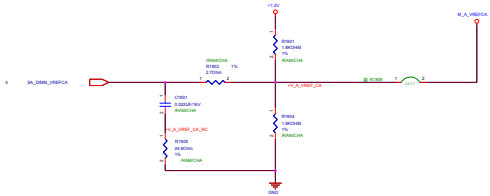

SDP need to place with S-Chm

EMI & RF


1110.0 RF
Close U1601
Close U1602
Close U1603
Close U1604
Close U1601
Close U1602
Close U1603
Close U1604


Title :
DDR4_ON-BOARD_81
Engineer
Ryan_Chang
E3E4A1BY0

待確認...



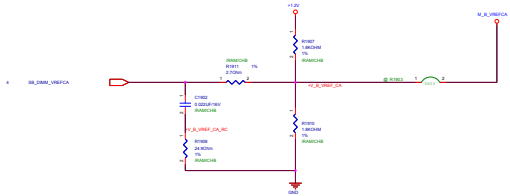
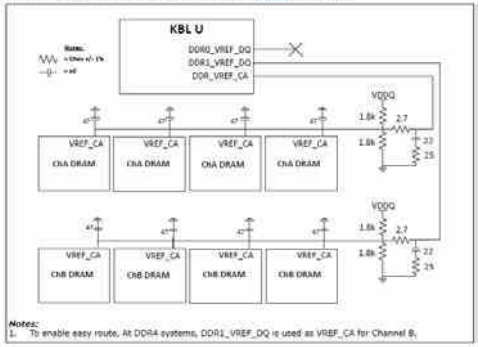
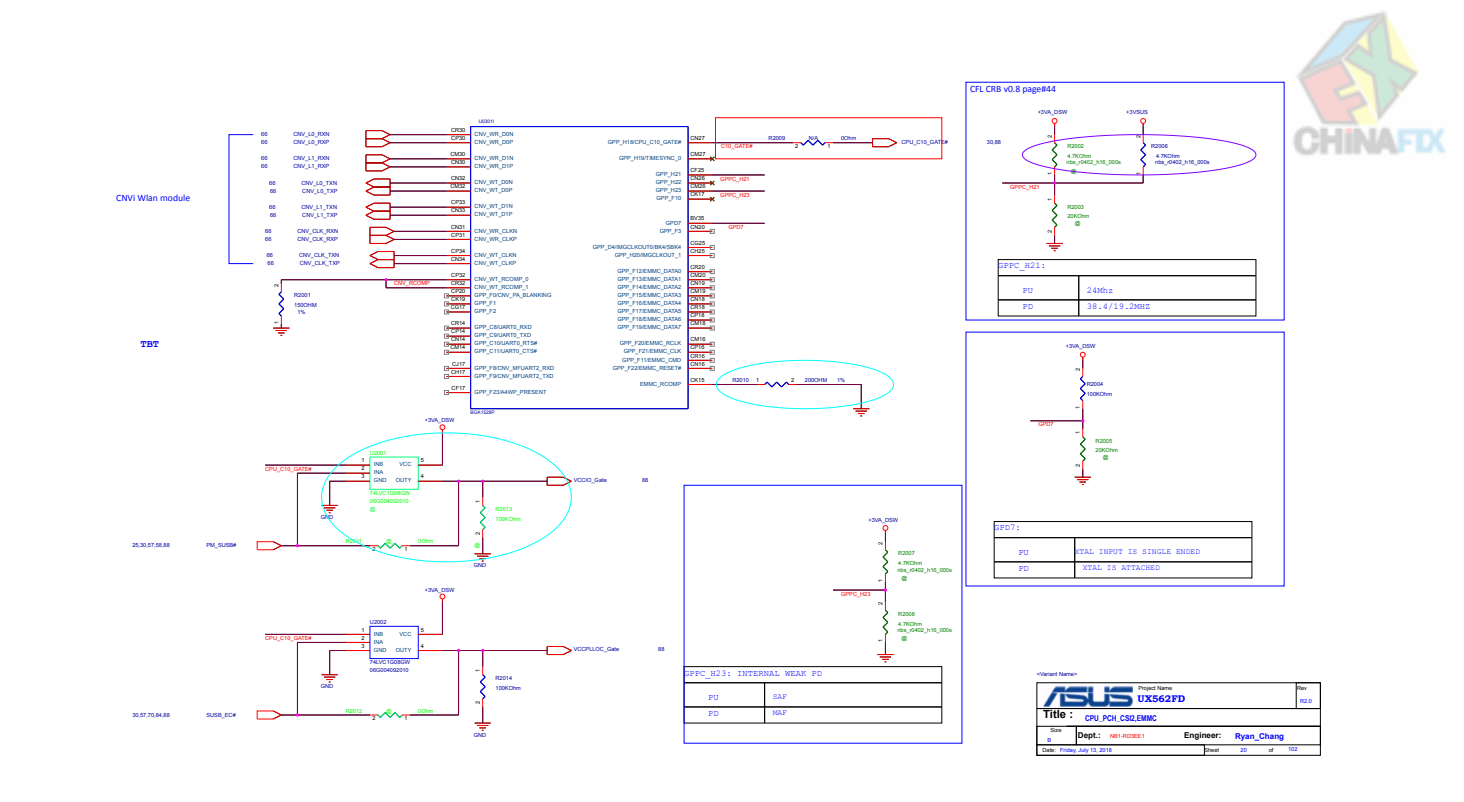
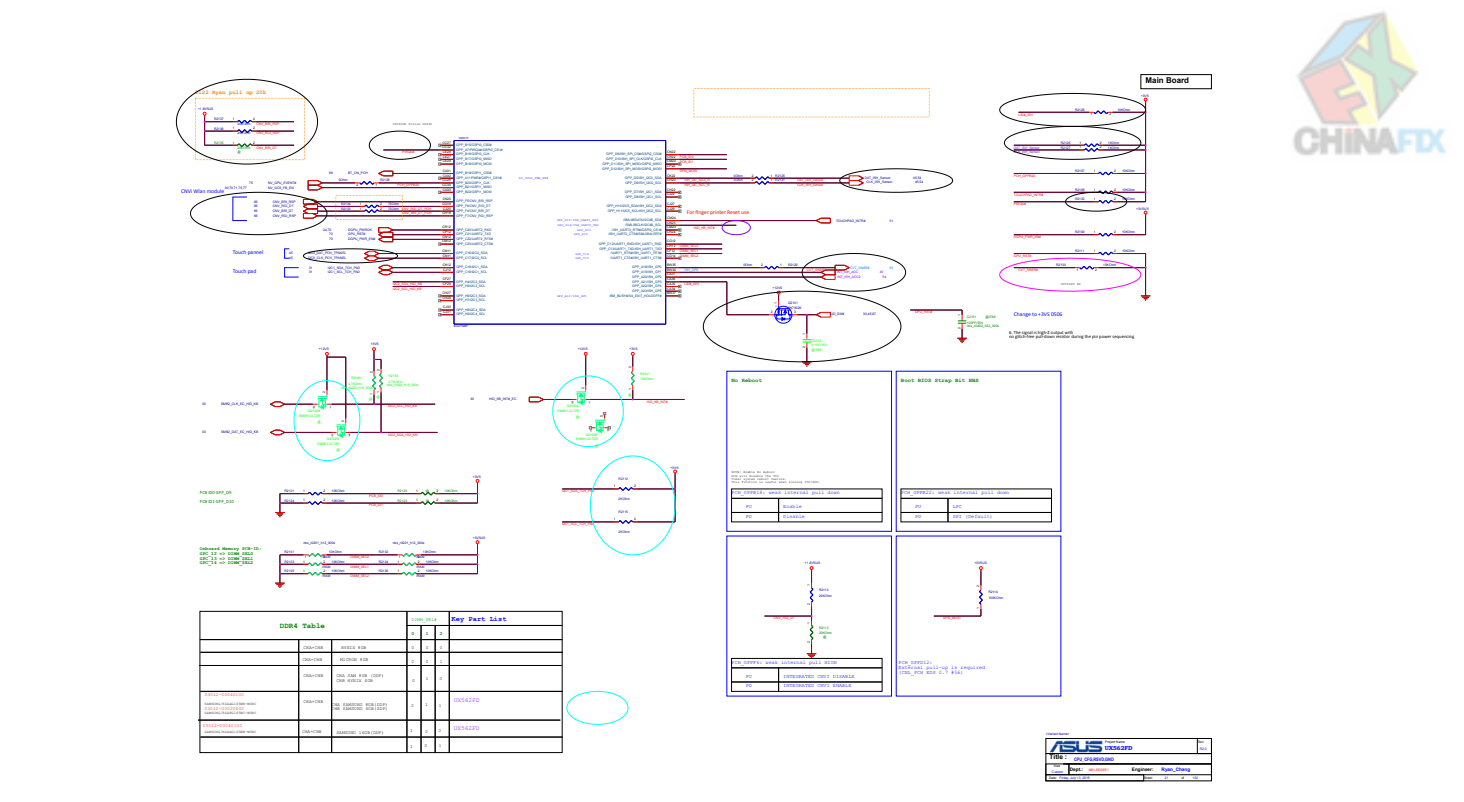


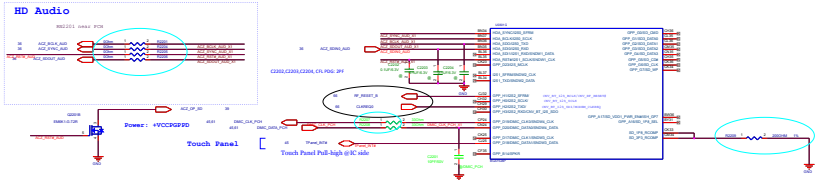
Figure 4-50. KBL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

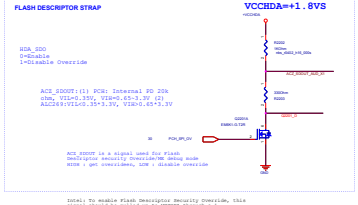



CNVi Wlan module
TBT
CFL CRB v0.8 page#44
GPFC_H21:
PU
24Mhz
PD
38.4/19.2MHz
GPD7:
PU
XTAL INPUT IS SINGLE ENDED
PD
XTAL IS ATTACHED
GPFC_H23: INTERNAL WEAK PD
PU
SAF
PD
MAF
Project Name
UX562FD
Title :
CPU_PCH_CSI2,EMMC
Dept.:
Engineer:
Ryan_Chang
Date:
Sheet
of

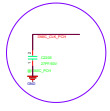

Main Board
Add 4pin pull up 20k
+1.8VALW
ONW Wlan module
Touch pannel
Touch pad
For finger printer Reset use
Change to +3VS 0536
No Reboot
Boot ROM Strap Bit BB8
PCH_SPKR22: weak internal pull down
PCH_SPKR10: weak internal pull down
PCH_SPKR11: weak internal pull down
PCH_SPKR12: External pull-up is required (CNL PCH EDS 0.7 #94)
Onboard Memory PCB ID:
SPC_1.4 =1 DDR4_SKU1
SPC_1.4 =2 DDR4_SKU2
SPC_1.4 =3 DDR4_SKU3
DDR4 Table
Key Part List
UX562FD
Project Name
Rev
Title :
CPU_CFG,MISC,GND
Engineer: Ryan_Chang
Date:
Sheet
of

Refer to PDG 0.8: Resistor values should be 33 ohms for both 3.3V and 1.8V bus voltage

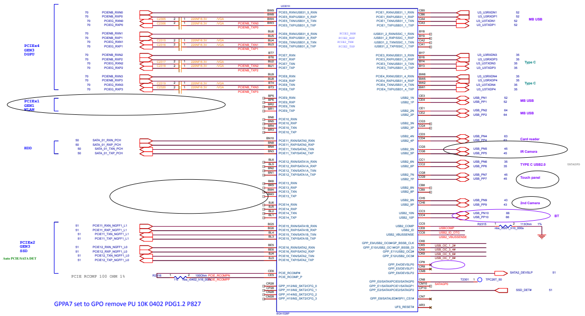




Intel: To enable Flash Descriptor Security Override, this signal should be pulled up to VCCHDA through a 1 MΩ to 2.2 MΩ ±5% resistor.



Variant Name:		Document Number:		Rev:
ASUS		UX562FD		0.1
Title :	SKL_PCH_AUDIO (ENG.SPEC)			
Size:	Project:		Engineer:	Ryan_Chang
A3	Dept.:	MB-INVBU1		
Date:	Friday, July 13, 2018	Sheet	22 of	102



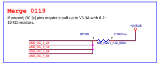
GPPA7 set to GPO remove PU 10K 0402 PDG1.2 P827

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 1			
PCIE 2			
PCIE 3			
PCIE 4			
PCIE 5	DGPU		Port 5
PCIE 6	DGPU		
PCIE 7	DGPU		
PCIE 8	DGPU		
PCIE 9			
PCIE 10	N/A		
PCIE 11/SATA_0	HDD		
PCIE 12/SATA_1A	N/A		
PCIE 13	N/A		
PCIE 14	N/A		
PCIE 15/SATA_1B	SSD(PCIE)	SSD(PCIE)	Port1
PCIE 16/SATA_2	SSD(SATA)		

SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	N/A
PORT 2	SSD

	USB 2.0
1	MB Right side
2	MB left side
3	
4	Card Reader
5	IR Camera
6	TYPEC
7	Touch panel
8	
9	2nd camera
10	BT

	USB 3.0
USB3_1	USB 3.1 Port(Type A)
USB3_2	
USB3_3	Type-C USB 3.1 gen1
USB3_4	Type-C USB 3.1 gen1

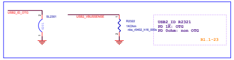


WhenusedasDEVSLP,noexternalpull-uporpull-downtermina onrequiredfromSATA

HostDEVSLP. **R2.0 SATA_DEVSLP change to DEVSLP2**

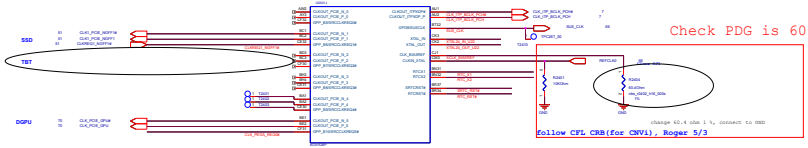
SATA PORT2 0323

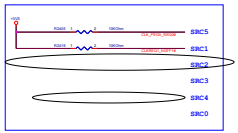
PDG1.2 P.848 Unused SATAGP[2:0] pins can be left as no connect and need to be default to GPIO funconality , refer to an unused GPIO for terminaon guidance.

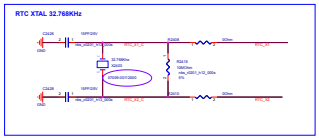


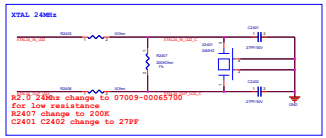
<Variant Name>

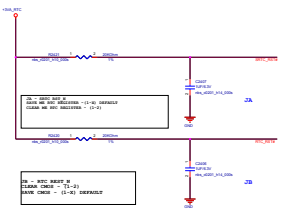
Project Name	UX562FD	Rev R2.0
Title :	CPU_PCH_PCIE,USB,SATA	
Size Custom	Dept.: NB1-RD3EE1	Engineer: Ryan_Chang
Date: Friday, July 13, 2018	Sheet 23 of 102	

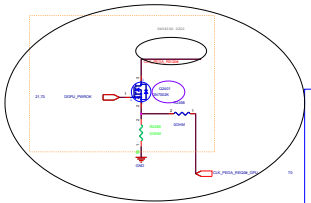

SSD
TBT
DGPU
Check PDG is 60 ohm 1%
follow CFL CRB(for CNVi), Roger 5/3

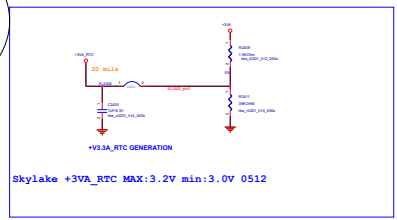

SRC5
SRC1
SRC2
SRC3
SRC4
SRC0


RTC XTAL 32.768KHz


XTAL 24MHz
R2.0 24Mhz change to 07009-00065700
for low resistance
R2407 change to 200K
C2401 C2402 change to 27PF

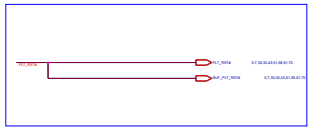

JA
JB

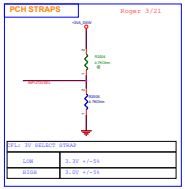



20 mils
+V3.3A_RTC GENERATION
Skylake +3VA_RTC MAX:3.2V min:3.0V 0512


ASUS
UX562FD
Title :
Dept.:
Engineer:
Ryan_Chang

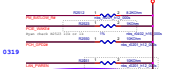
Main Board

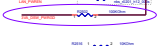




LAN_WAKE#=PCH_GPD2 PDG1.2 P.849Connect this signal on PCH to EC. 0319

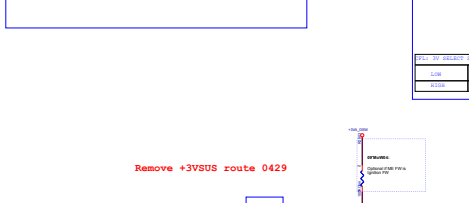
R2559 change to 1M to reduce power consumption/0330





ADD 0302 prevent PCH floating

Remove +3VSUS route 0429



D2607 Prevent EC drive high SUS_PWRGD sink low in S5->S3

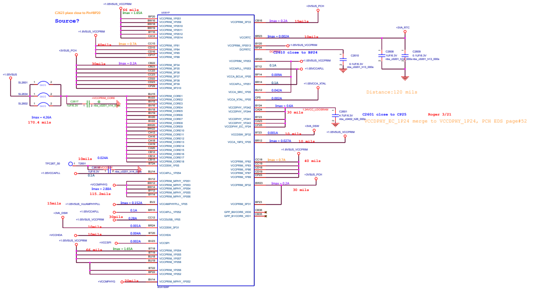
2014/04/09-1

Power failure solution (S0->G3,S5->G3):

ADD 0302 prevent PCH floating

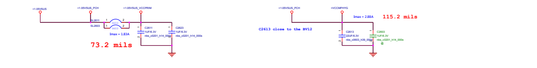
TP for Boundary Scan Test

Remove +3VSUS route 0429

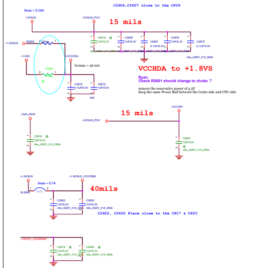


+1.05VSUS

Combine +1.0VSUS_PCH to +1.0VSUS 0423



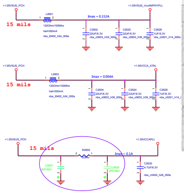
+3VSUS / +1.8VSUS



Filter requirement for +1.05VSUS

LC size 0603->0402 DCR MAX 0.3 ohm 0126

Distance:400 mils



CFL PDG V0.7 page#457

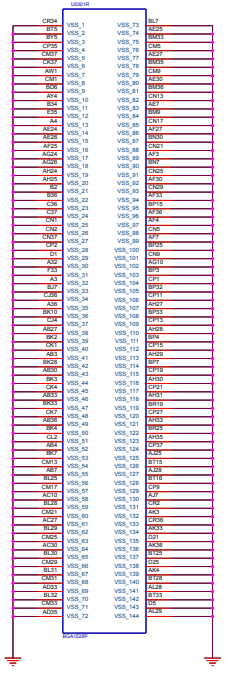
Filter Requirements for CFL U PCH

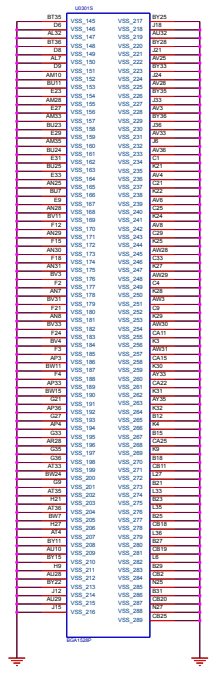
Supply	Value	Quantity	Type	Notes
VCCA_XTAL_1P05 (Pin F1) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR < 0.3 ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended
VCCAMPHYPLL_1P05 (Pin R22) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR < 0.3 ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended

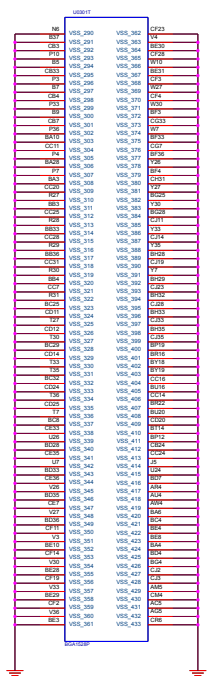
Notes:
1. Placeholder is only. Does not need to be stuffed.
2. All capacitors are bulk capacitors unless labeled otherwise.
3. 2x 22uF 0603 caps can optionally be used instead of 1x 47 uF of 0603 caps. Caps should be with X5R temperature characteristics.

<Variant Name>

ASUS	Project Name: UX562FD	Rev: R2.0
Title : CPU_PCH_POEWR,GND		
Size: D	Dept.: NB1-RD3EE1	Engineer: Ryan_Chang
Date: Friday, July 13, 2018	Sheet 26 of 102	



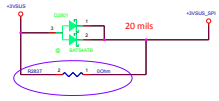


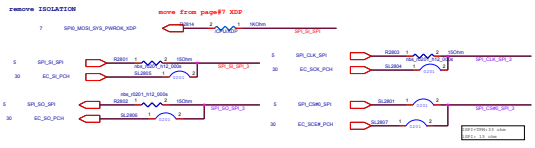


<Variant Name>

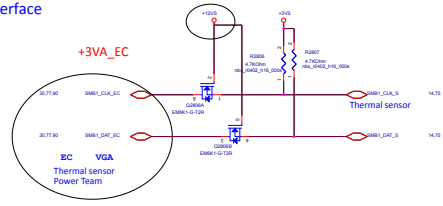
ASUS	Project Name: UX562FD	Rev: R2.0
Title : CPU_PCH_POEWR,GND		
Size: B	Dept.: NB1-RD3EE1	Engineer: Ryan_Chang
Date: Friday, July 13, 2018	Sheet 27 of 102	

SPI PCH Power

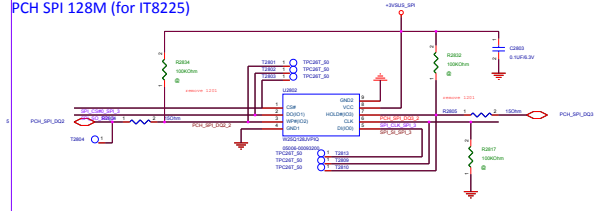




System Management Interface



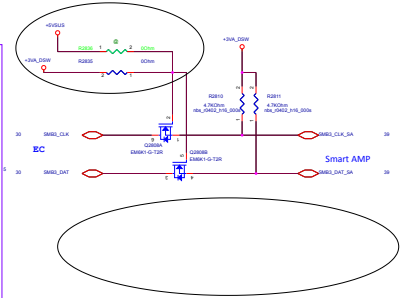
PCH SPI 128M (for IT8225)



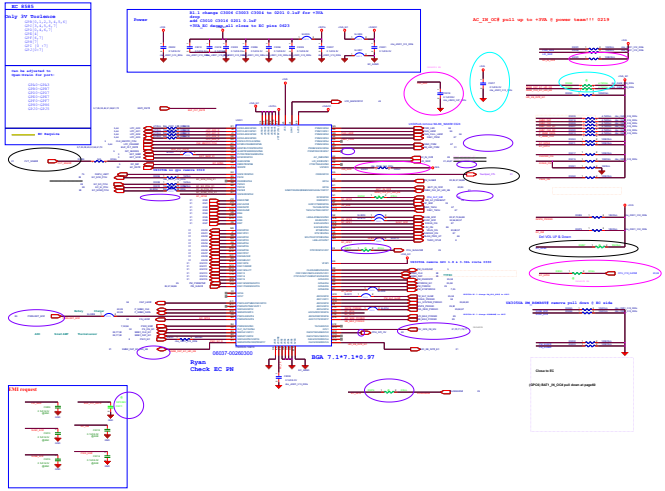
main: 05006-00093700

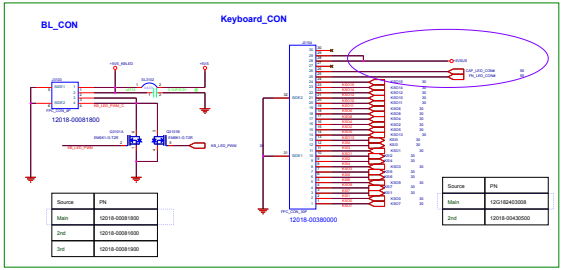
2nd : 05006-00093200

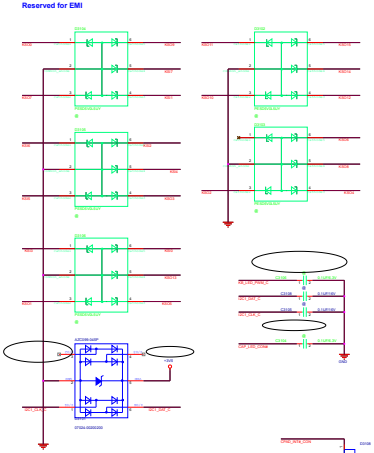
Ryan Check for SPI ROM capacity

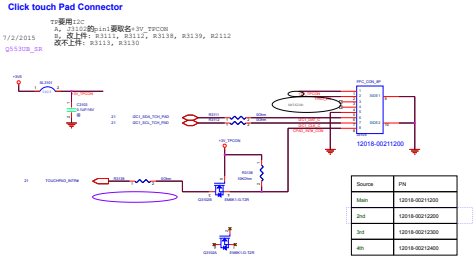


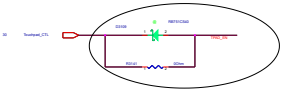
ASUS	Project Name: UX562FD		Rev: R0.0
Title : PCH-SPI ROM,OTH			
Size: B	Dept.: NB1-RD3ED1	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet 28 of 102		


EC 8181
Only 3V Variable
Can be adjusted to Open-Drain for port:
3V Requires
Power
R1.1 change C3004 C3003 C3014 to 0201 0.1uF for +5VA
add C3040 C3014 0201 0.1uF
+5VA_EC change all views to EC pins 0423
AC_IN_OCB pull up to +3VA I power team!!! 0219
Change to 32K Cmos 1V8
Ryan
Check EC PN
BGA 7.1*7.1*0.97
06037-00280300
CMOS request

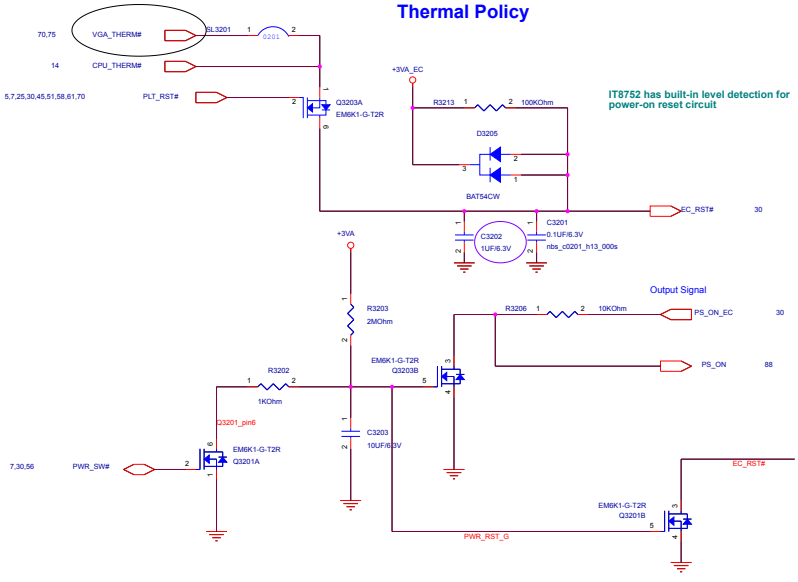

BL_CON
Keyboard_CON
12018-00081800
12018-00380000
Source
PN
Main
12018-00081800
2nd
12018-00081600
3rd
12018-00081900
Source
PN
Main
12018240300B
2nd
12018-00430500


Reserved for EMI


Click touch Pad Connector
TP要用I2C
A, 为此pin要取名+3V_TPCON
B, 改上拉: R3111, R3112, R3138, R3139, R2112
改不上拉: R3113, R3130
7/2/2015
Q5530B_ER
12018-00211200
Source
PN
Main
12018-00211200
2nd
12018-00212000
3rd
12018-00212300
4th
12018-00212400



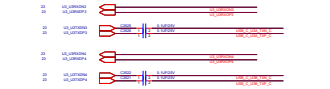

Title :
EC_KB_TP_TPM
Engineer:
KB
UX562FD

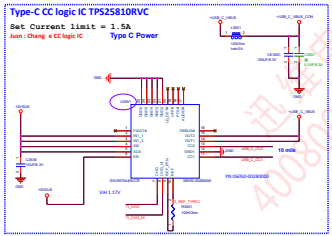


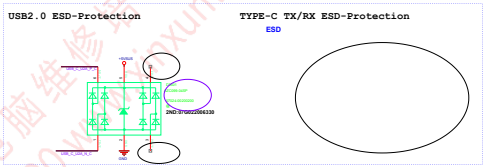
battery embedded (press pwr_sw 10sec, then reset ec)

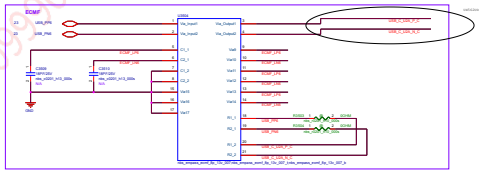
<Variant Name>

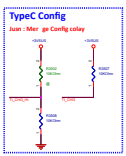
ASUS	Project Name: UX562FD	Rev: R2.0
Title : RST_Reset Circuit		
Size: A	Dept.: NB1-RD3EE1	Engineer: Ryan_Chang
Date: Friday, July 13, 2018	Sheet 32 of 102	



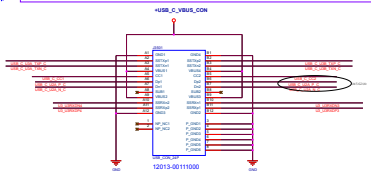


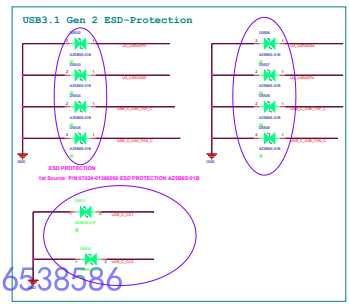


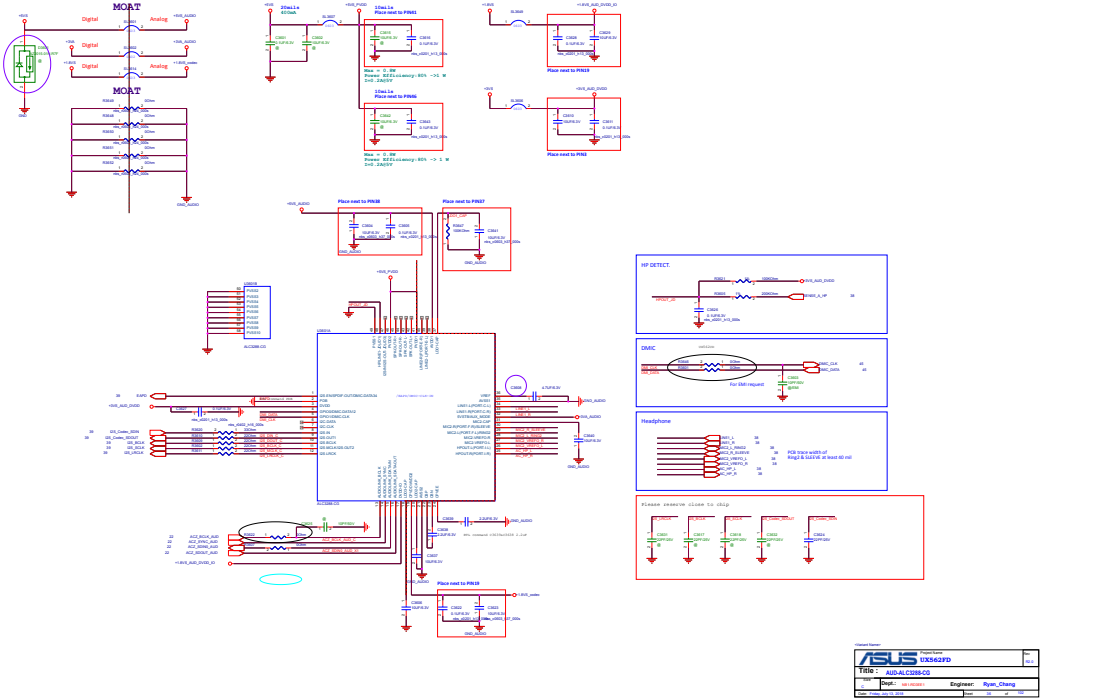


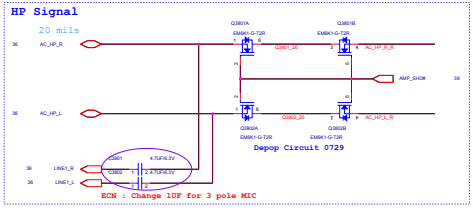


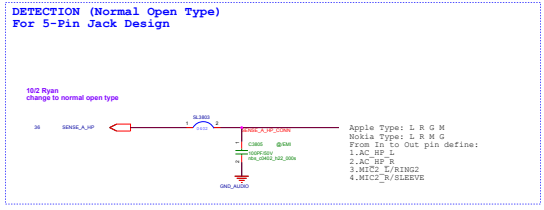
CHG_HI	CHG	TI CONFIG
0	0	Default USB power
0	1	1.5A @5V
1	0	Default USB power
1	1	3A @5V

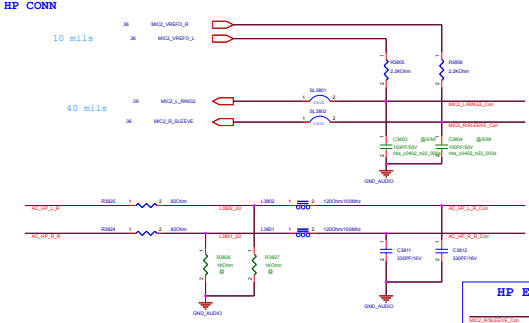


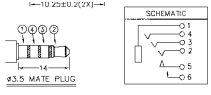


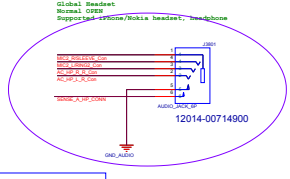

MOAT
Digital
Analog
MOAT
Place next to PIN61
Place next to PIN62
Place next to PIN19
Place next to PIN3
Place next to PIN38
Place next to PIN37
Place next to PIN10
HP DETECT.
DMIC
Headphone
Please reserve close to chip
ALC3288-CG
UX5602FD
AUD-ALC3288-CG
Ryan_Chang

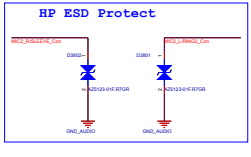




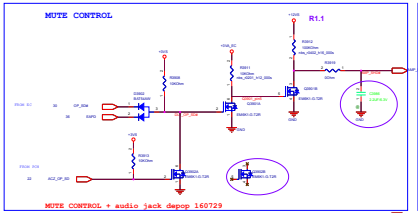


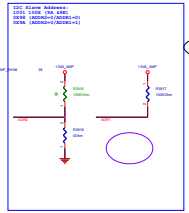


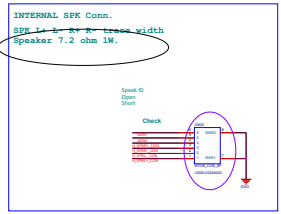


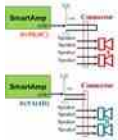


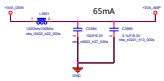
ASUS	Project Name: UX562FD		Rev: R2.0
Title : AUD_Headphone			
Size: B	Dept.: MB-RD2/EE1	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet 38 of 102		

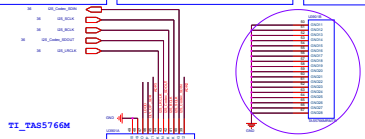

MUTE CONTROL
R1.1
MUTE CONTROL + audio jack depop 160729


I2C Slave Address:
1011 110R (7A 69R)
0697H (ADDR2=0/ADDR1=0)
0693A (ADDR2=0/ADDR1=1)


INTERNAL SPK Conn.
SPK_L+_R+_R-_L- trace width
Speaker 7.2 ohm 1W.
Speak ID
Open
Short
Check

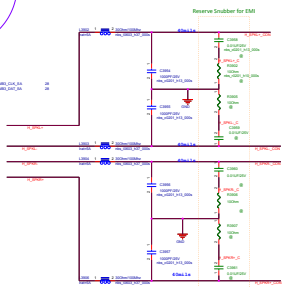

SmartAmp
SmartAmp

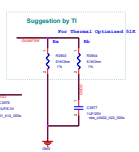

65mA


TI_TAS5766M

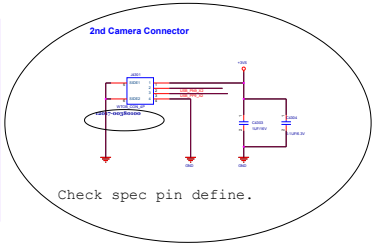

Max = 4W / Channel = 8W
Power Efficiency:85% -> 9.5 W
I=1.05A@9V 0.8 A@12V 0.5A@19V


Close PIN13/14


Reserve Snubber for EMI


Suggestion by TI
For Thermal Optimized SIZ

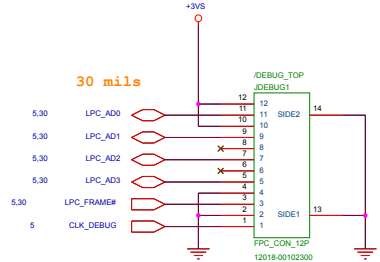

ASUS
UX562FD
Title : AUD_SMA_TAS5760M
Dept. :
Engineer: Ryan_Chang



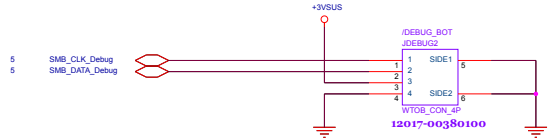
ASUS	Project Name: UX562FD		Rev: 0.2
Title : CS			
Size:	Dept.:	Engineer: Ryan_Chang	
Date: Friday, July 27, 2018		Sheet 25 of 100	

Main Board

LPC Debug Port

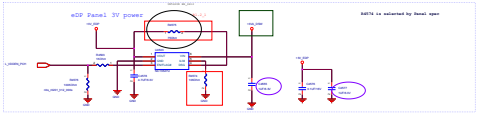


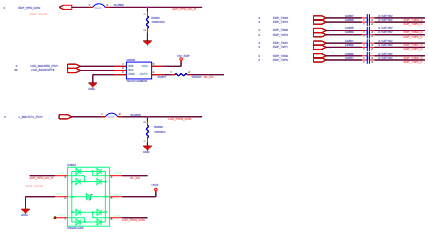
DIMM Debug Port

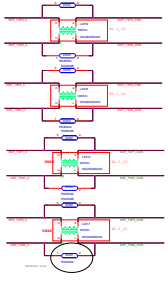


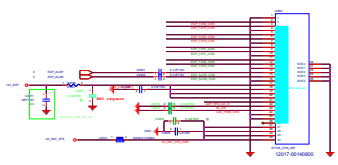
<Variant Name>

ASUS	Project Name: UX562FD	Rev: R2.0
Title : BUG_Debug		
Size: A	Dept.: NB1-RD3EE1	Engineer: Ryan_Chang
Date: Friday, July 13, 2018	Sheet 44 of 102	

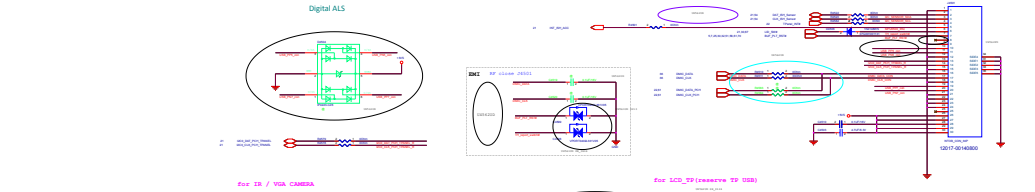


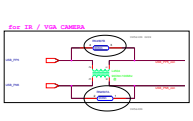






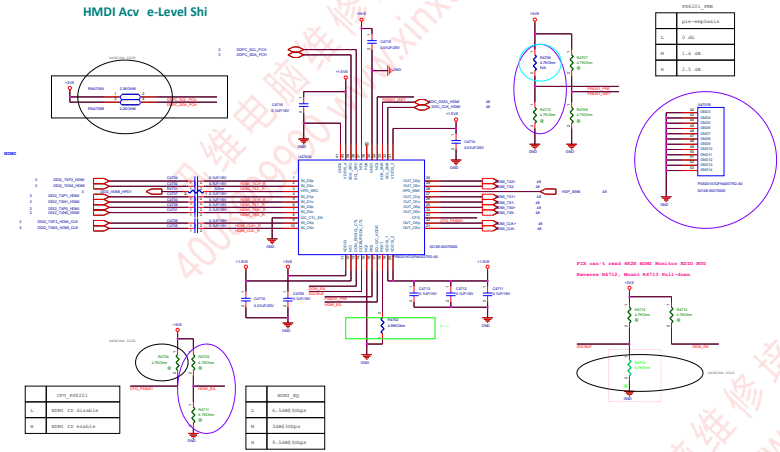
Source	PN
Main	12017-00140800
2nd	12017-00140800
3rd	12017-00140800





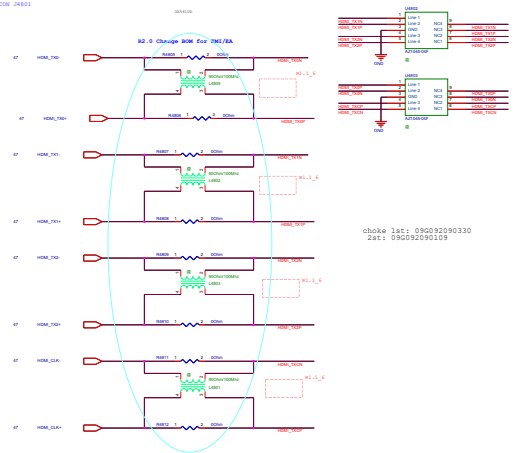
Source	PN
Main	12017-00140800
2nd	12017-00141000
3rd	12017-00140800

Main Board

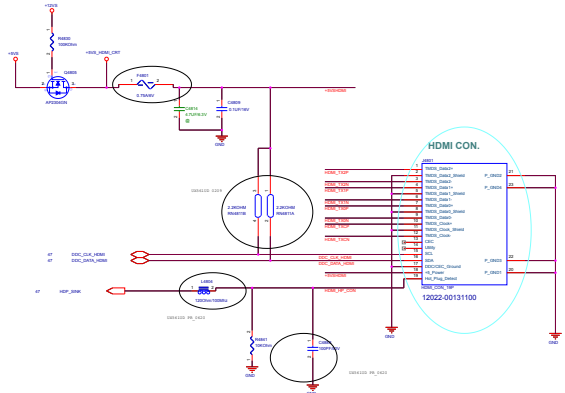


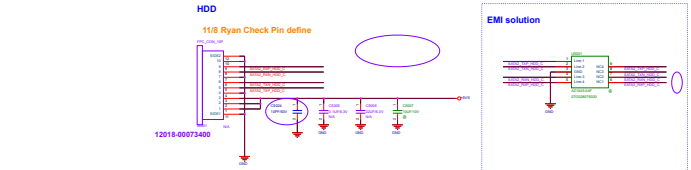
Close to CONNECTOR

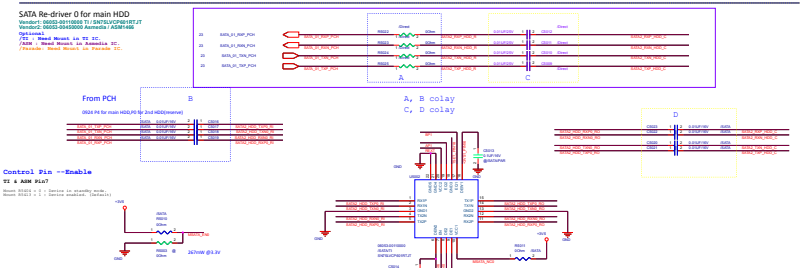
Near CON 24801



choke 1st: 09G092090330
2st: 09G092090109







TI / SN75LVCP601

Function	Pin No.	Mount
PWR	18, 20	
GND	19, 3, 13	
Enable	7	

TI_DE & EQ Settings

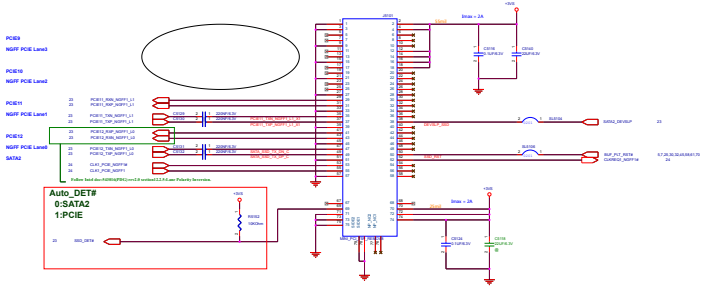
DE1 / DE2	EQ1 / EQ2	DE	EQ
Pin 8 / Pin 9	Pin 17 / Pin 19		
NC	NC	-4 dB	0 dB
0	0	0 dB	7 dB
1	1	-2 dB	14 dB

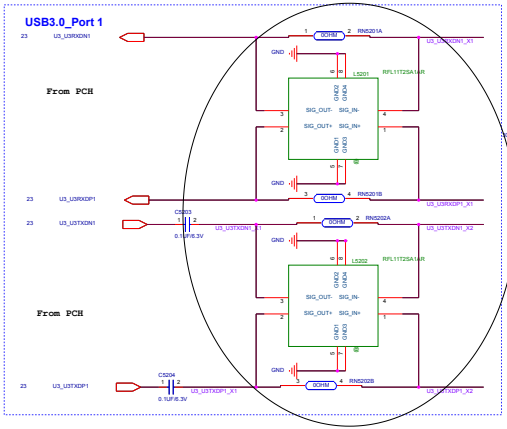
TI_ Device Function

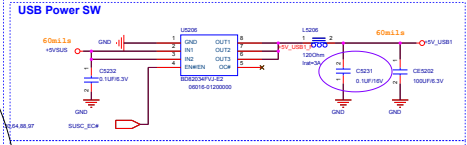
DEW_1	DEW_2	DE Width
Pin 16	Pin 6	
0	0	SATA 3/2/1
1	1	SATA 2/1

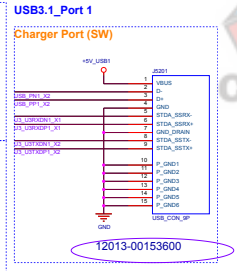
ASUS	Project Name: UX562FD	Rev: 0.1
Title :	HDD & ODD CON	
Size: A3	Dept.: Gen Modern	Engineer: Ryan_Chang
Date: Friday, July 19, 2019	Sheet 62 of 132	

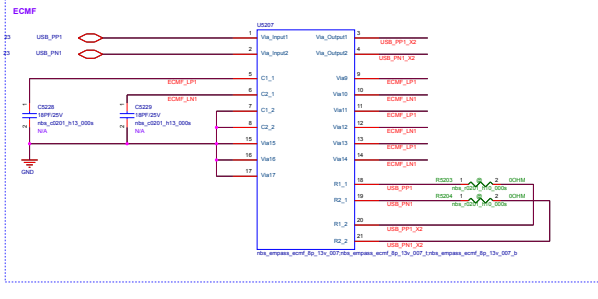
1st SSD

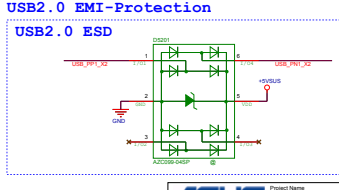












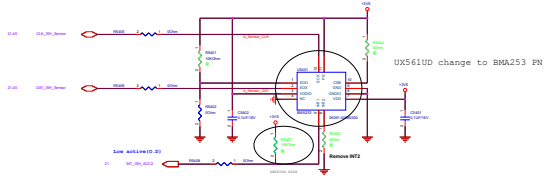
ASUS	Project Name: UX562FD		Rev: R2.0
Title : USB Charger			
Size: B	Dept.: NB1-RD3EE1	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet 52 of 102		

Main Board

08091-00040000

	mount	
KXTJ2	RS213, RS214	02151-00040000
BMA255	unmount	08091-00040000

G Sensor(C,D part)

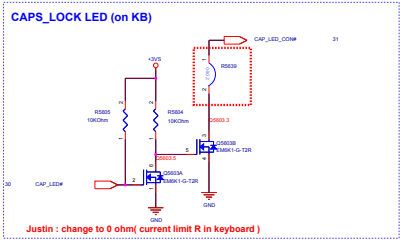


UX561UD change to BMA253 PN

I2C address

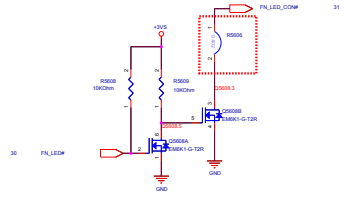
	mount	KXTJ2	BMA255
Pull High	RS211	0001111x (DPh)	0011001x (19h)
Pull Low	RS212	0001110x (DEh) (Default)	0011000x (18h) (Default)

CAPS_LOCK LED (on KB)



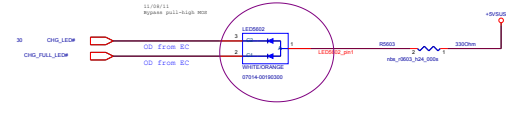
Justin : change to 0 ohm(current limit R in keyboard)

FN LED

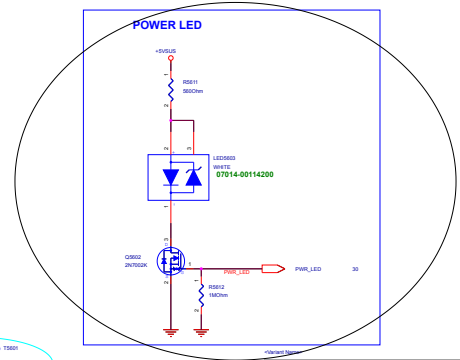


Justin : change to 0 ohm(current limit R in keyboard)

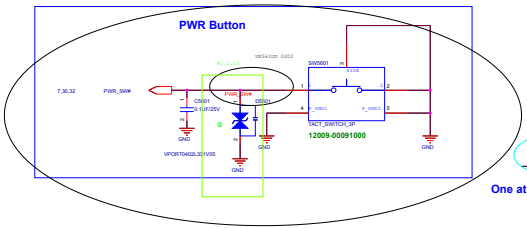
Charger LED (on MB)

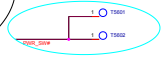


POWER LED



PWR Button



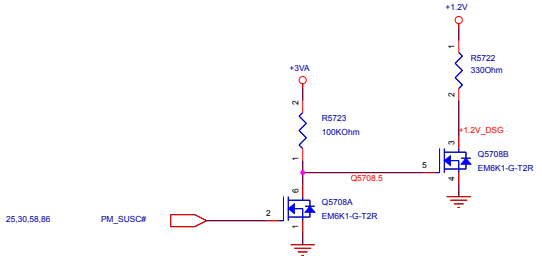


One at TOP, the other at BOT

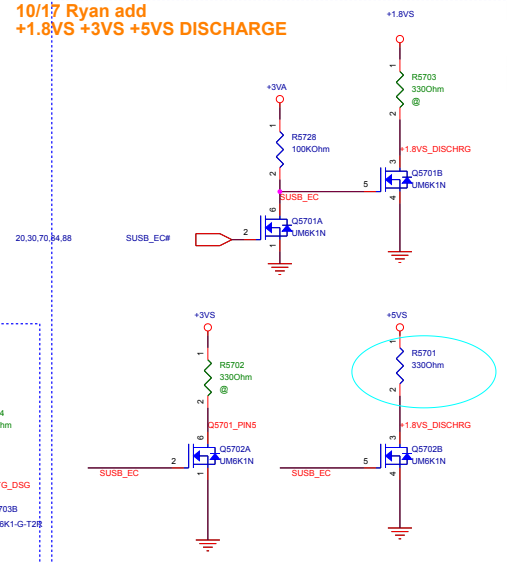
ASUS	Project Name: UX562FD		Rev: R2.0
Title : LED_Indicator			
Size: B	Dept.: NB1-RDSE1	Engineer: Ryan_Chang	
Date: Friday, July 13, 2018	Sheet 56 of 102		

Justin : Removed no used Discharge circuit
1.8V ,VCCIO,+5VS load switch already build in 180~260 ohm discharge function

+1.2V DISCHARGE

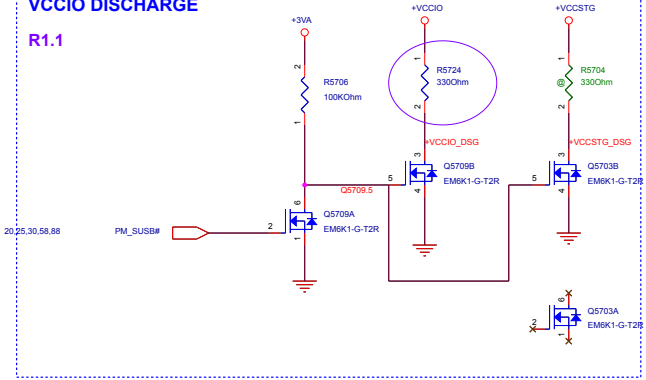


10/17 Ryan add
+1.8VS +3VS +5VS DISCHARGE



VCCIO DISCHARGE

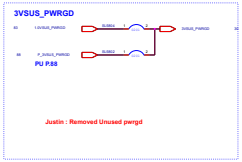
R1.1

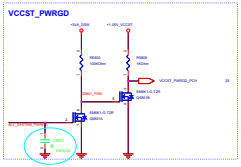


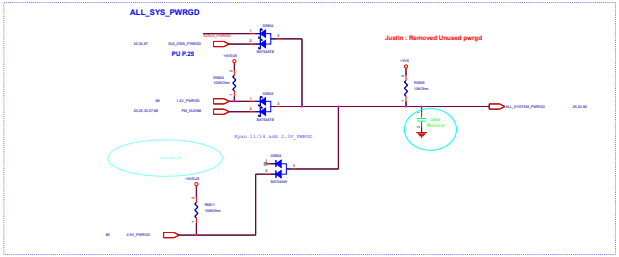
<Variant Name>

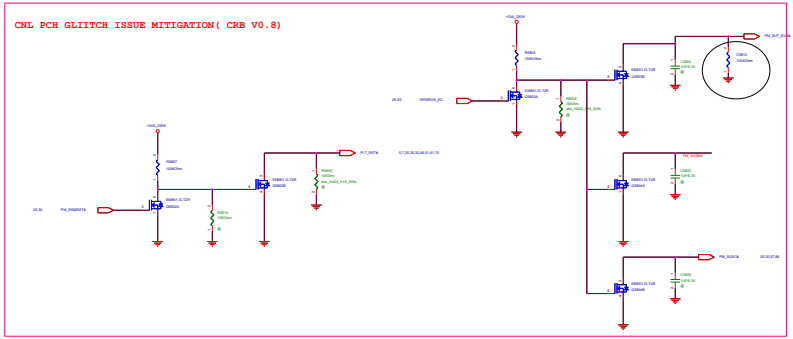
ASUS	Project Name: UX562FD	Rev: R2.0
Title : DSG_Discharge		
Size: A	Dept.: NB1-RD3EE1	Engineer: Ryan_Chang
Date: Friday, July 13, 2018	Sheet 57 of 102	

Main Board

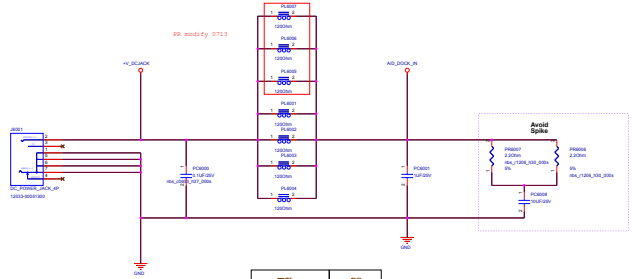






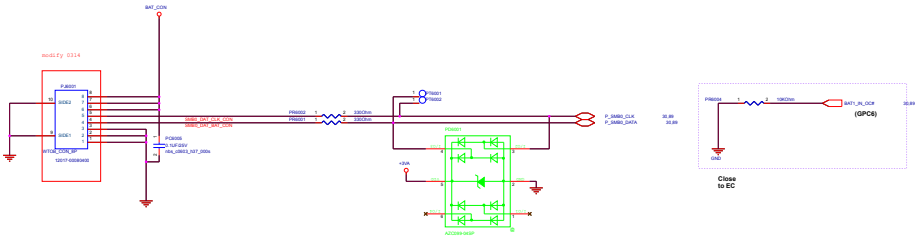


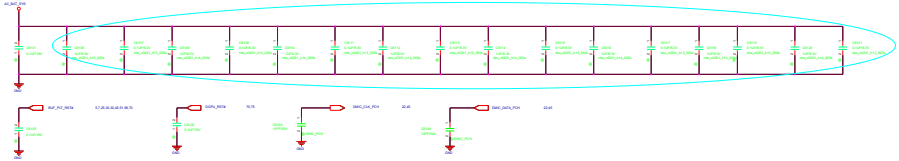
ASUS	Project Name: UX562FD		Rev: 0.2
Title : PEC_Protect			
Size: A3	Docl:	Engineer: Ryan_Chang	
Date: Friday, July 19, 2019		Sheet 55 of 102	



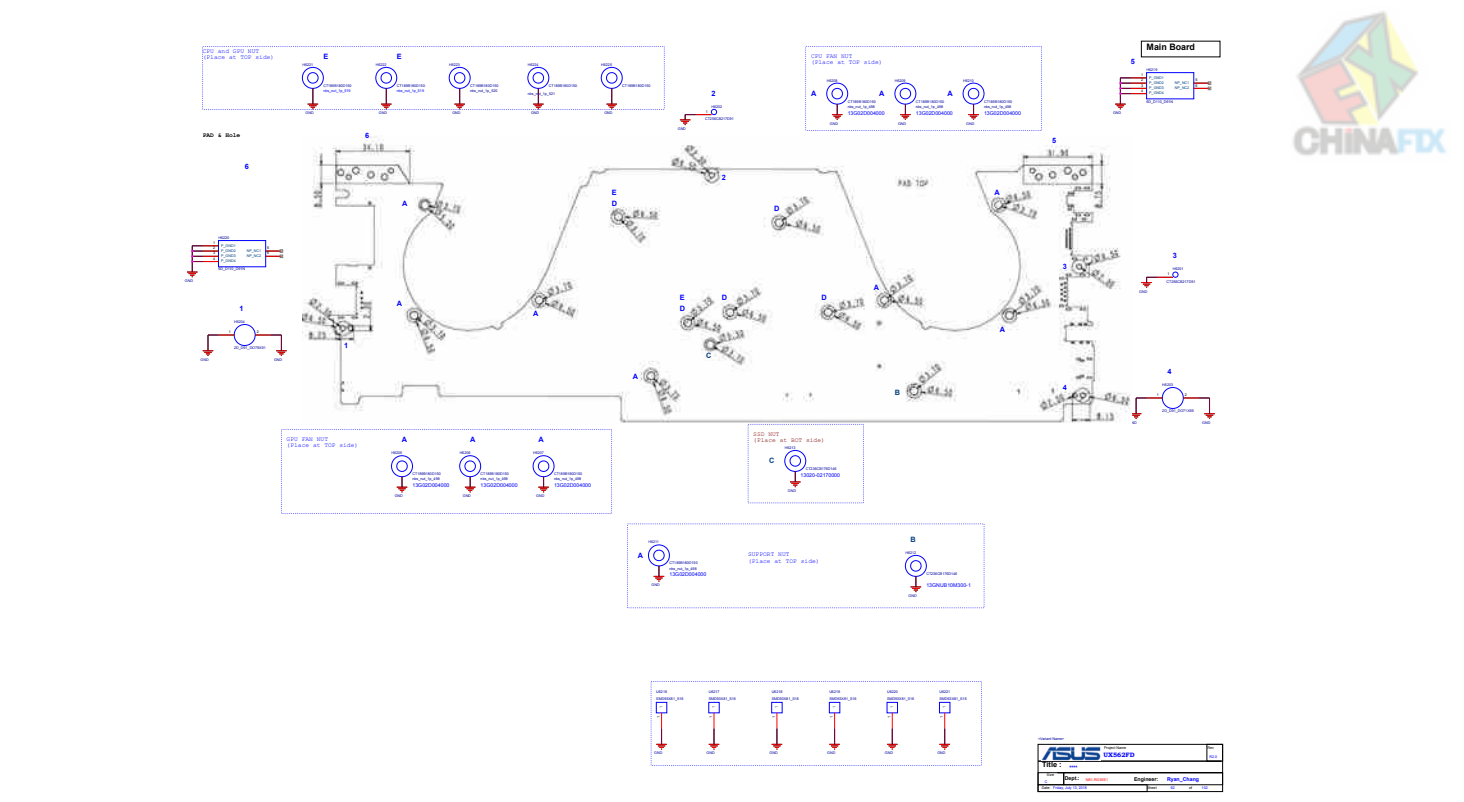
瓦數	Boot 數量
45W & 65W	3
90W	4

Battery Connector





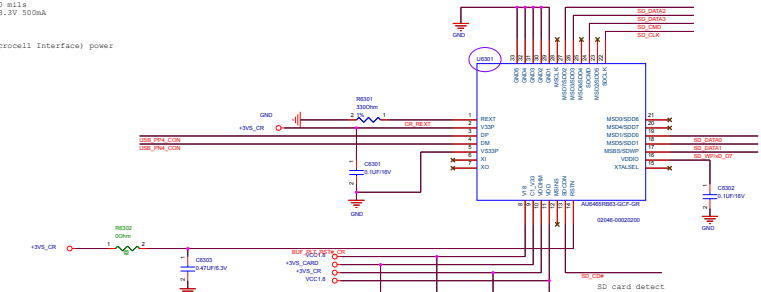

ASUS
Project Name
UX562FD
Title :
Size
Document Number
Rev
0.1
Engineer:
Ryan_Chang
Date: Friday, May 03, 2019
Sheet
of


Main Board
CPU and GPU NUT
(Place at TOP side)
CPU FAN NUT
(Place at TOP side)
PAD & Hole
PAD TOP
GPU FAN NUT
(Place at TOP side)
SSD NUT
(Place at BOT side)
SUPPORT NUT
(Place at TOP side)
ASUS
TX562FD

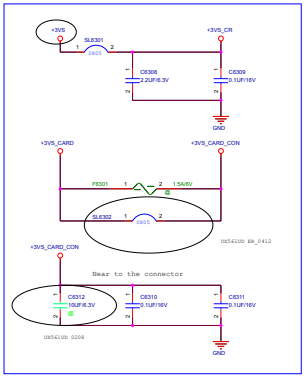
Card Reader (AU6465RB63-GCF-GR)

Power Trace:
+3VS 40 mils source
+3V_CR 40 mils
+3V_CARD 40 mils
+3V_CARD_CON 40 mils
SD Card power 3.3V 500mA

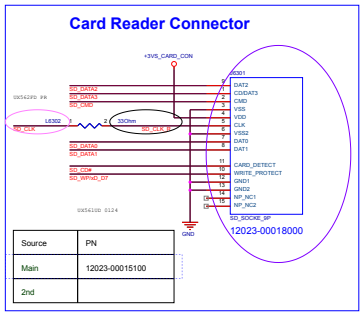
UTMI(USB2.0
Transceiver Macrocell Interface) power



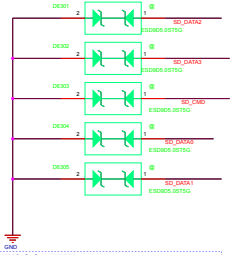
R1.1_1/8-1



Card Reader Connector

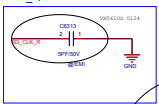


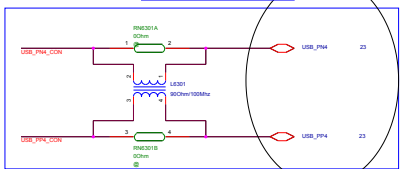
Source	PN
Main	12023-00015100
2nd	



Remove VCC1.8 from VDDIO.
VDDIO is IN/OUT PUT pin would output 3.3V
which would affect VCC1.8 when connecting.

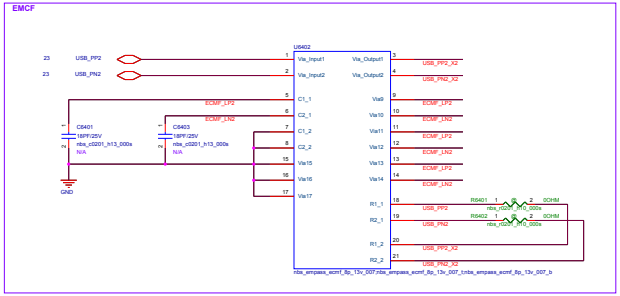
R1.1_1/8-2

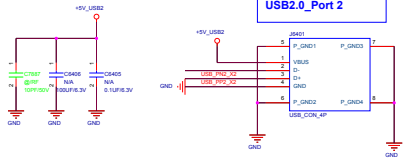


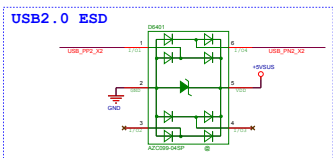


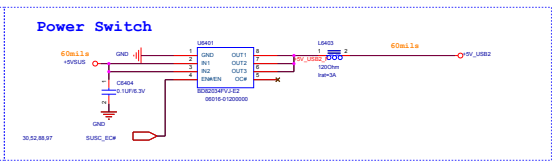
<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title : IO_Board(1)_CardReader		
	Engineer: Mario_Jhu		
Size: B	Project Name: UX562FD		Rev: R2.0
Date: Friday, July 13, 2018	Sheet 63 of 101		



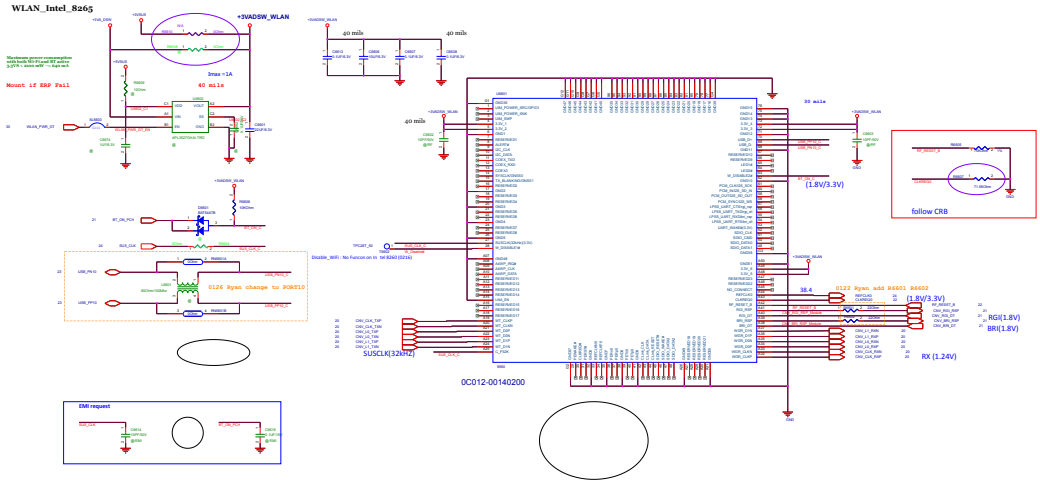




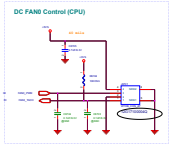


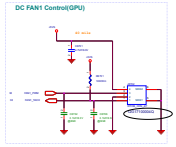
BOM

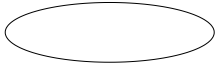
ASUS	Project Name: UX562FD	Rev: R2.0
Title :		
Size: B	Dept.: N81-RD3EE1	Engineer: Ryan_Chang
Date: Friday, July 13, 2018	Sheet 64 of 102	

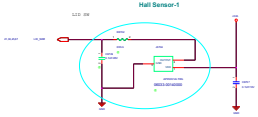


Project Name	UX562FD	Rev	0.1
Title :	NGFF WLAN&BT		
Size	Document Number		
Date: Friday, July 13, 2018	Sheet 66 of 102		
Dept.: MB-RD&SI1	Engineer: Ryan_Chang		

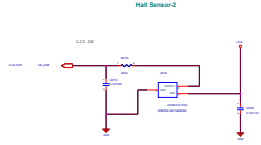




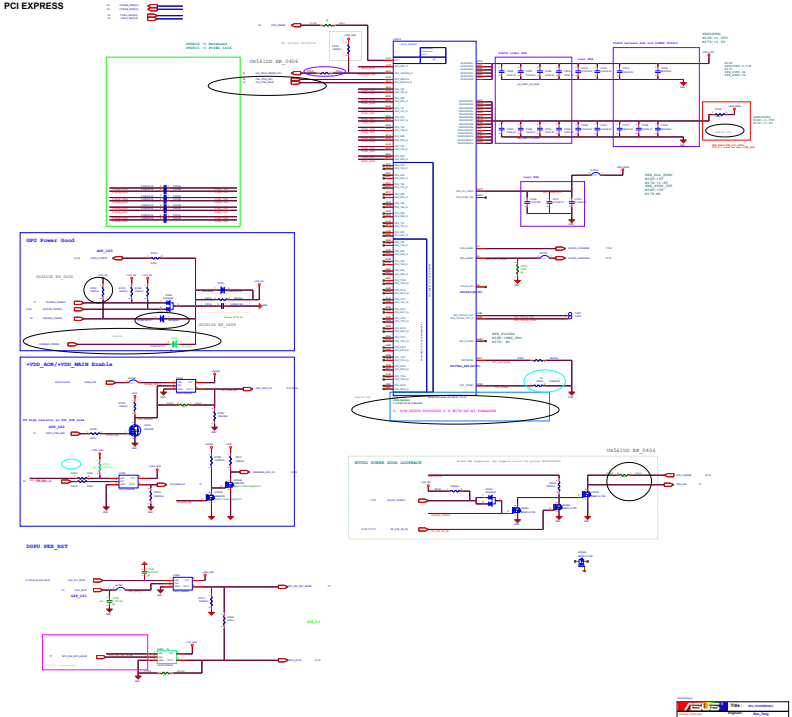




Revised	PG
Table	08033-00016800
Star	08033-00160800

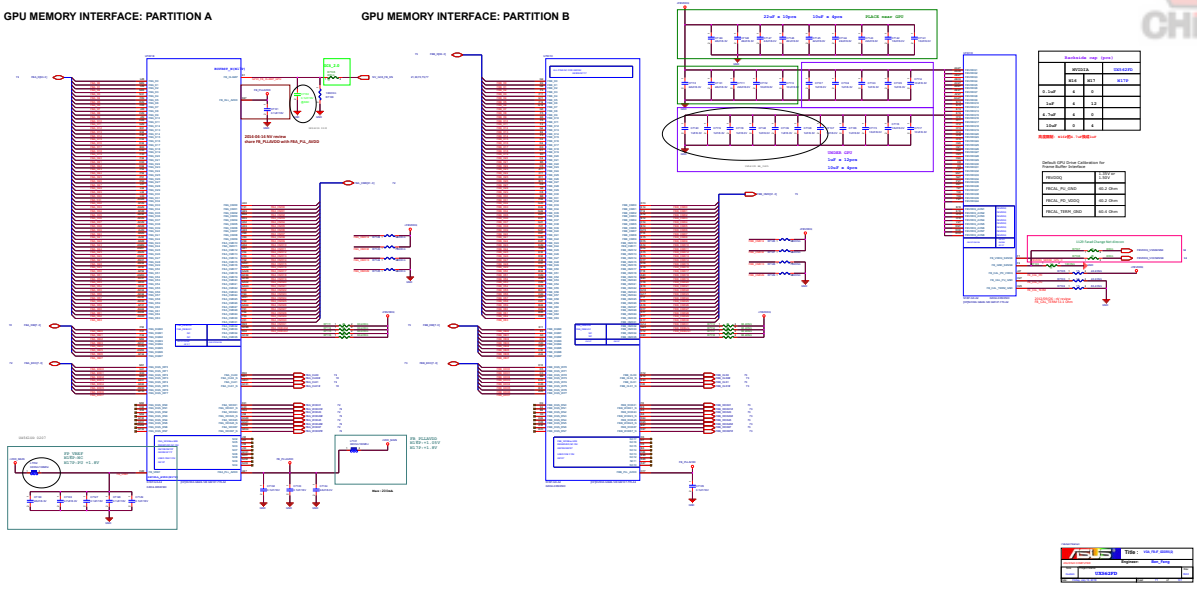


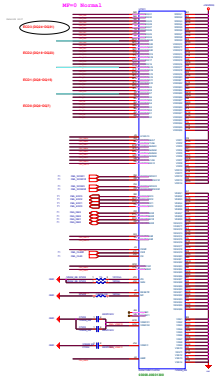
ASUSTeK COMPUTER INC.			
/ISUS	T3000ZPD		
Title :			
Size: B	Date:	Sheet of	Engineer: Ryan_Chang


PCI EXPRESS
GPU Power Good
+VDD_ACM/+VDD_MAIN Enable
DGPU PEX_RST
PEX_RST_GPU#
PEX_RST_DGPU#
+VDD_ACM_EN
+VDD_MAIN_EN
GPU_GD
DGPU_PWR_GD
PEX_RST_GPU#
PEX_RST_DGPU#
+VDD_ACM_EN
+VDD_MAIN_EN
GPU_GD
DGPU_PWR_GD

GPU MEMORY INTERFACE: PARTITION A

GPU MEMORY INTERFACE: PARTITION B



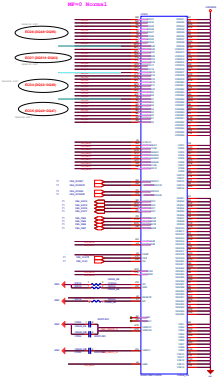


FBA Partition Memory (1 of 2)

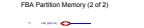
GDDS MODE SELECTION

UG1 G2G256 VSUM 128Mb x 32 (512MB)
Ver1 P/N: G2GS-2G512U32 G2GS2G32AZ1AG1A1G2RTLAC1G (1.2Gb), Sheep Ver2 (+1.25V)
Ver2 P/N: G2GS-2G512U32 Micron/ES2564G32BAG5-BLF (1.2Gb), Sheep Ver2 (+1.25V)

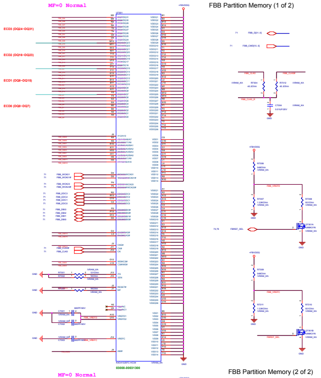
UG1 G2G256 VSUM 256Mb x 32 (1024MB)
Ver1 P/N: G2GS-4G1024U32 MC1G2G4A7P2 (2256MB)RLRF 4B (2.4Gb), Sheep Ver2 (+1.25V)
Ver2 P/N: G2GS-4G1024U32 SAMG2G4G1A1G2G3GFB-YG2C (2.4Gb), Sheep Ver2 (+1.25V)



FBA Partition Memory (2 of 2)



FBB Partition Memory (1 of 2)

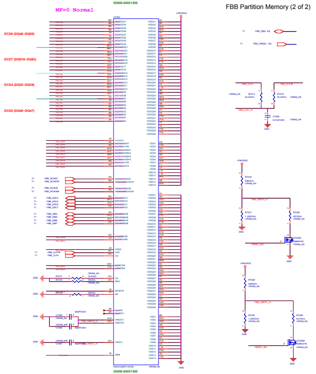


USE GDDR5 VRAM 128Mb x 32 (512MB)
1st: P/N: 03008-00030200 SAMSUNG/K4G41325FC-HC03 (C-die), Strap: 0x3 (+1.35V)
2nd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)

USE GDDR5 VRAM 256Mb x 32 (1024MB)
1st: P/N: 03008-00050300 MICRON/MT51J256M32HF-60:A (A-die) ,Strap: 0x9 (+1.35V)
2nd: P/N: 03008-00050100 SAMSUNG/K4G80325FB-HC03 (B-die), Strap: 0x8 (+1.35V)

	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm

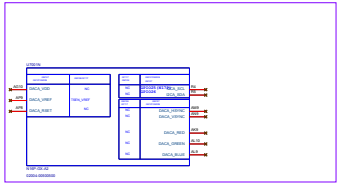
FBB Partition Memory (2 of 2)



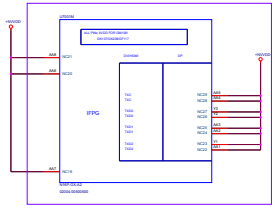
<Variant Name>

ASUSTeK COMPUTER	Title :	VGA VRAM CH_B	
	Engineer:	Ben_Fang	
Size: Custom	Project Name: UX562FD		Rev: R2.0
Date: Friday, July 13, 2018	Sheet: 73	of 101	

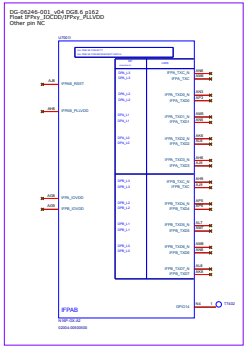
CRT DAC_A



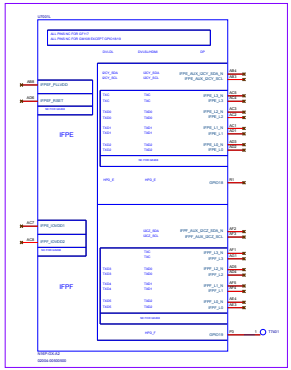
LVDS IFPG



LVDS IFPA/B



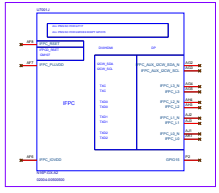
LVDS IFPE/F



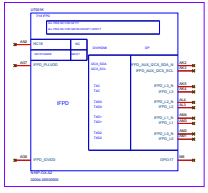
Title :	VGA CRTLVDS(I)	
Engineer:	Ben_Fang	
Size: C	Project Name: UX562FD	Rev: 0.1
Date: Friday, July 14, 2017	Sheet 15 of 57	

DG-06246-001_v02 p157 DG8.6
DPF not used
3FPxy_3DCDD//3FPxy_PLLVDD 10K PD
Other pin NC

DP(link C)



DVI(link D)



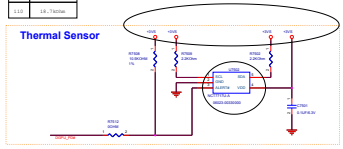
DG-07158-001_v05_secured Table 12-2.

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	OUT		HDVIO3_PWM_VID
1	OUT		SCH_FN_EN
2	OUT		GPU_EVENT# /WAKE*
3	OUT		EDP_PWM
4	OUT		LVDS_MAIN_EE
5	OUT		PWM_LCE
6	IN		HVVDD_FB1
7	OUT		LCD_EL_PWM
8	IN		MEM_VDD_CTL
9	I/O		THERM_ALERT
10	OUT		MEM_VREF_CTL
11	OUT		LCD_VDD
12	IN		PWM_LEVEL
13	OUT		LCD_BLEN
14	IN		HPD_IFPA
15	IN		HPD_IFPB
16	IN		EDP_PEX_RST_N#H#
17	IN		HPP_IFPC
18	IN		HPD_IFPE
19	IN		SD VID1CH/HTERXD3
20			HVVDD2_FB2
21	OUT		UNUSED
VBAT	I/O	40 gh	OVERT

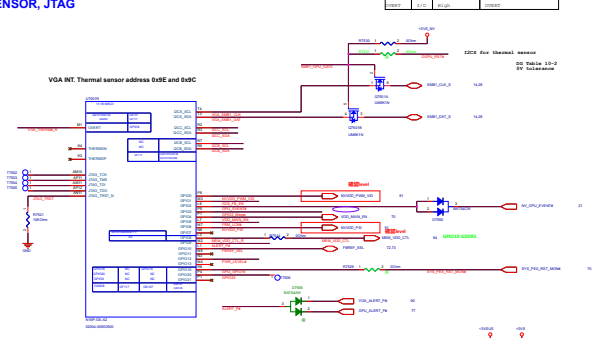
Temp.	Resistor
55	2kOhm
60	5.5kOhm
100	12.1kOhm
125	14kOhm
150	18.7kOhm

Thermal Sensor



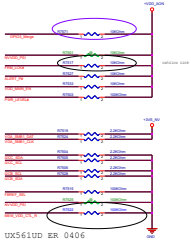
GPIO, TEMP SENSOR, JTAG

VGA INT. Thermal sensor address 0x9E and 0x9C

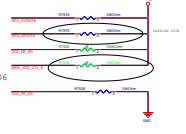


I2C5 for thermal sensor

DG Table 10-2
5V tolerance

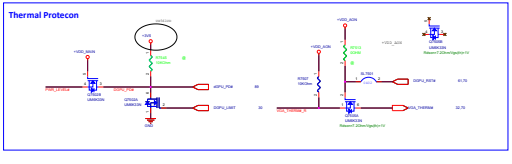


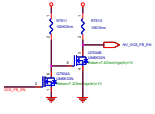
UX561UD ER_0406



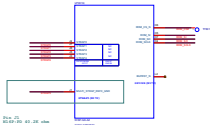
UX561UD ER_0406

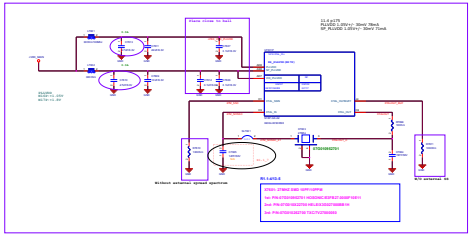
Thermal Protecon



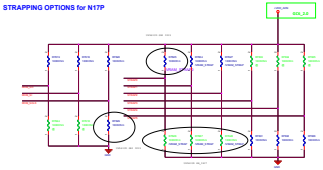


Title :	VGA_GPIO/VDP(I)		
Engineer:	Ben_Feng		
Size: Custom	Project Name: UX562FD		Rev: 0.01
Date: Friday, July 13, 2018	Sheet 157	of 170	





STRAPPING OPTIONS for N17P



N17P Strap use 100Kohm

VRAM Source	STRAP0	STRAP1	STRAP2	RAMCFG Setting	
2GB Samsung K4G80325FB-HC28	L	L	L	0x0	2GB(4x 16 VRAM) * 2 pcs (K4G 80 325 FB-HC28, K4G 80 325 FB-HC25)
2GB Micron MT61K256M32JE-14:A	L	L	H	0x1	
2GB Samsung K4G80325FB-HC25	H	H	L	0x6	2GB(4x 16 VRAM) * 2 pcs (K4G 80 325 FB-HC25)
2GB Micron MT61K256M32JE-12:A or 2GB Hynix H5GC4H24AJR-R0C	L	L	M	0x8	

	STRAP0	STRAP1	STRAP2	VGA_ALT_ADDR	MFGS_SEL	PCIE_CFG	VGA_DEVICE
	L	L	L	0	0	0	0
	L	L	H	0	0	0	1

N17P SCAL_EXPOSED Strap

Pass Index	SCAL_D3	SCAL_D1	SCAL_SCAN	SCAL_EXPOSED	SCAL_EXPOSED	SCAL_EXPOSED	SCAL_EXPOSED
1	H	H	H	DISABLE	DISABLE	DISABLE	DISABLE
2	H	H	M	DISABLE	DISABLE	DISABLE	DISABLE

STRAPPING OPTIONS for N16P

DD-07138-001_v05_secured.p 197
Table 15-1, GB5B-128 Multi-level Node Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SCAL_EXPOSED	SCAL_EXPOSED	SCAL_EXPOSED	SCAL_EXPOSED
ROM_CS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Tristate and pulled up to VIO_SUPPLY and pulled down to GND. Pull with factory pull up.			
STRAP1	Keep fast print for pull up to VIO_SUPPLY and pull down to GND. Do not Stuff.			
STRAP2				
STRAP3				

Table 15-2.

	PU	PD
1 GB/Color	1GB	1GB
2 GB/Color	2GB	2GB
3 GB/Color	3GB	3GB
4 GB/Color	4GB	4GB
6 GB/Color	6GB	6GB
8 GB/Color	8GB	8GB
12 GB/Color	12GB	12GB
16 GB/Color	16GB	16GB

RAM ID	RAM Size
0x0000	1GB/Color
0x0001	2GB/Color

Change N16S & N16N VRAM Vendor

USE GDDR5 VRAM 128Bx 4 32 (512MB)

Samsung x4 top 2ch Samsung/K4G41325FC-HC03 -> pn11=0xee, 20Mohm +1, 33V

Micron x4 top 2ch Micron/MT40A512M32JY-083:A -> pn11=0xee, 24.9Kohm +1, 33V

USE GDDR5 VRAM 256Bx 8 32 (1024MB)

Micron x8 top 2ch MT52L512M32D2PF-107:A -> pn11=0x, 100ohm +1, 33V

Samsung x8 top 2ch K4G80325FC-HC03 -> pn11=0x 4.99Kohm +1, 33V

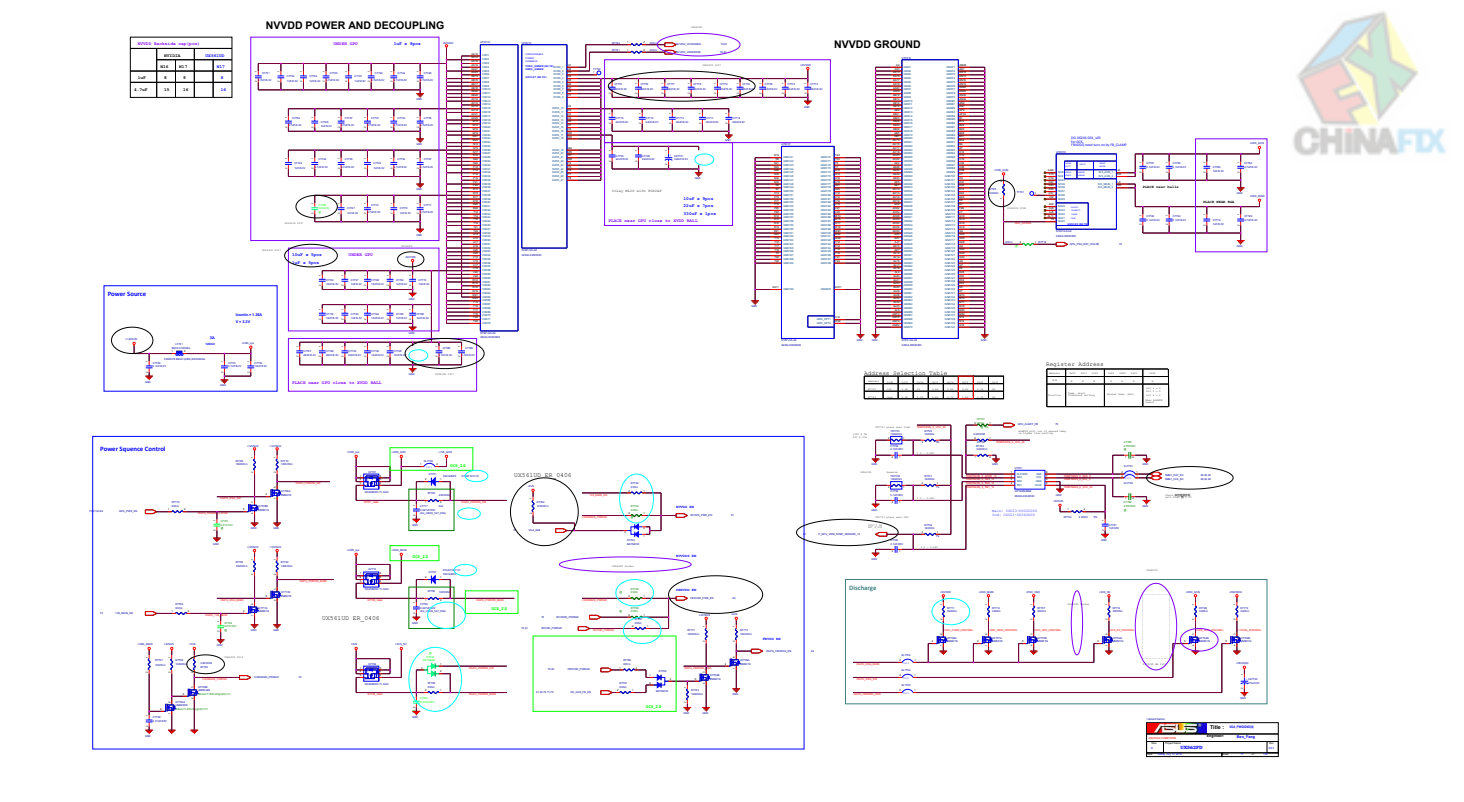
Table 3. N17P-GO/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDDQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Data Code Alert	qual. Plan	Status
8 Gb	256mx32	1.35V and 1.5V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	A-die	0x2	7 Gbps	N/A	Full	Port production candidate
4 Gb	128mx32	1.35V and 1.5V	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.35V	Micron	EDW4032BABG-70-R	A-die	0x5	7 Gbps	N/A	Full	Port production candidate

Notes:
1. For N17P-Gx, the maximum allowable memory case temperature is 95 °C.
2. N17P-Gx runs MCLK up to 3000 MHz when FBVDDQ = 1.35V. GPU is required to run MCLK > 3000 MHz.

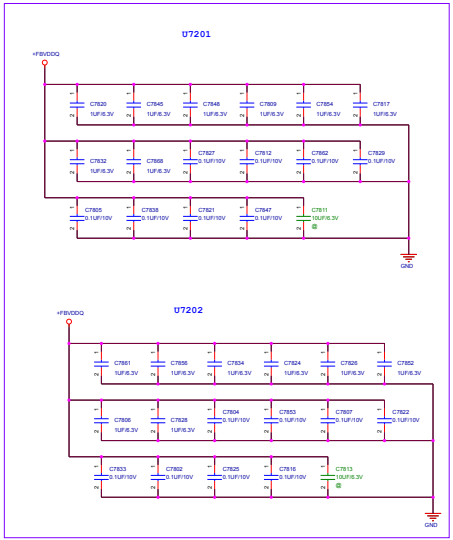
Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

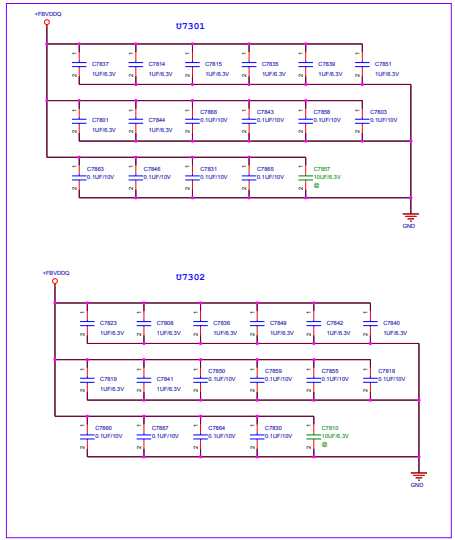
Strap Pins			Function Selected by This Strapping			
STRAP0	STRAP1	STRAP2	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1


NVVDD POWER AND DECOUPLING
NVVDD GROUND
Power Source
Power Squence Control
Discharge
Address Selection Table
Register Address
UX5610D_ER_0404
UX5610D_ER_0404
Title : MB-TM020002
Engineer : Shen_Feng
UX5610FD

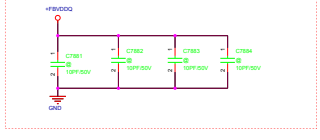
Location is close to DRAM for clamshell mode

0.1uF X8
1uF X 8



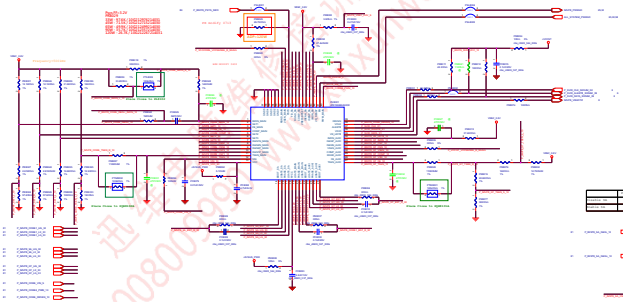


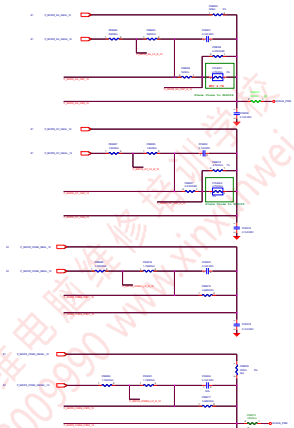
R0.1_16

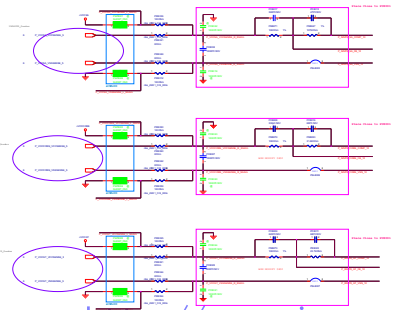


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : VRAM CAP	
	Engineer: Mario_Jhu	
Size: B	Project Name: UX562FD	Rev: R2.0
Date: Friday, July 13, 2018	Sheet 76 of 101	

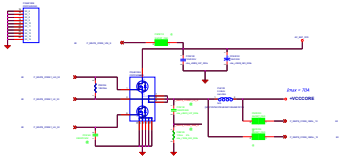


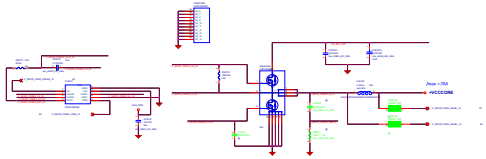




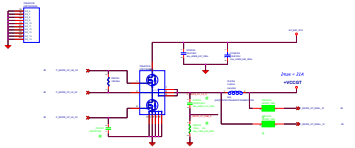
Wishky LAKE IMVP8 Power (2)[For CPU]

+VCCCORE

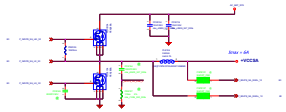


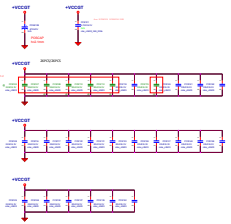


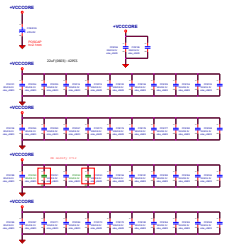
+VCCGT

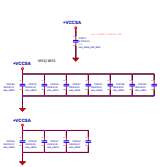


+VCCSA

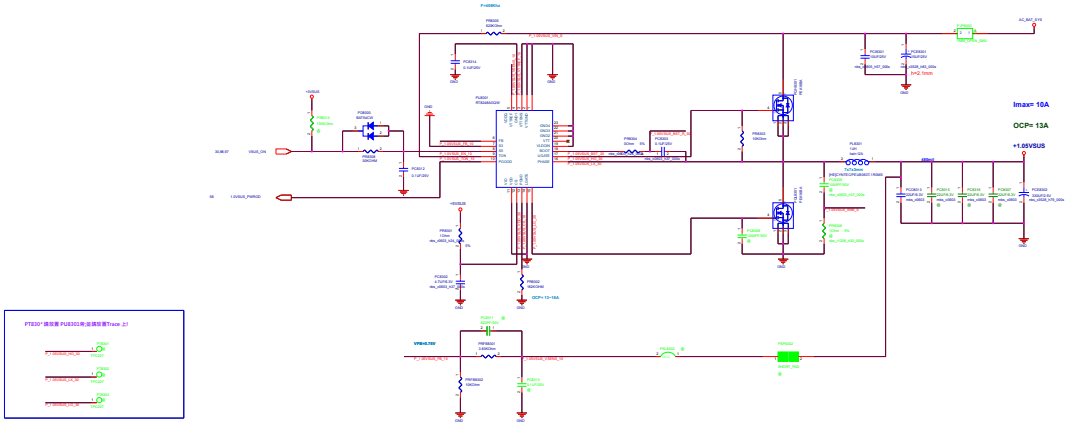






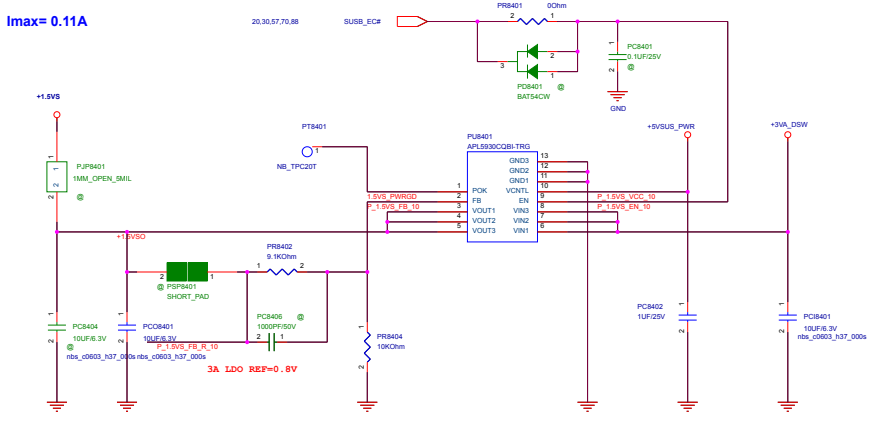


+1.05VSUS [For PCH]



ASUS	Project Name: UX582FD		Rev: 10.0
Title :	PW_+1.05VSUS/+1.8VSUS		
Size: A3	Dept.: MB Power team	Engineer:	EASON
Date: Friday, July 13, 2018		Sheet 35 of 102	

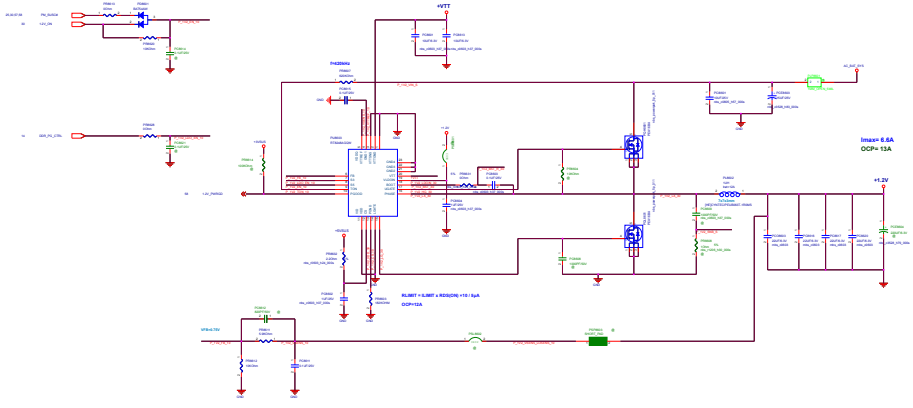
+1.5VS [For Audio]



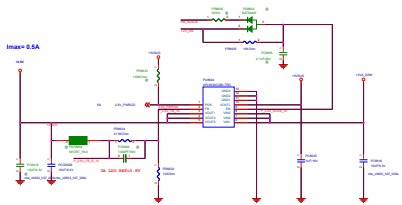
<Variant Name>

ASUS	Project Name: UX562FD	Rev: R2.0
Title : +1.5VS		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EASON
Date: Friday, July 13, 2018	Sheet 84 of 102	

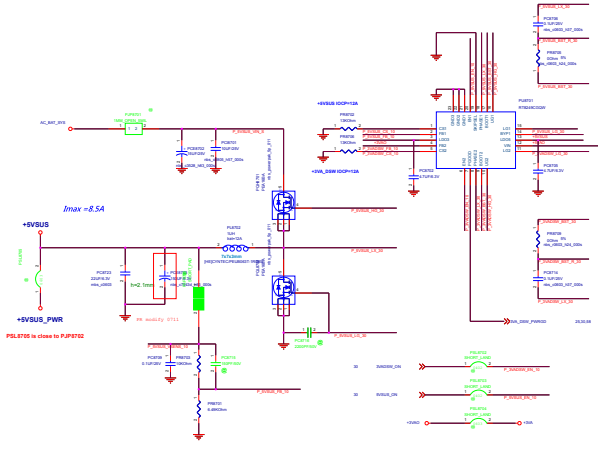
+1.2V / +VTT / +2.5V[For Memory]

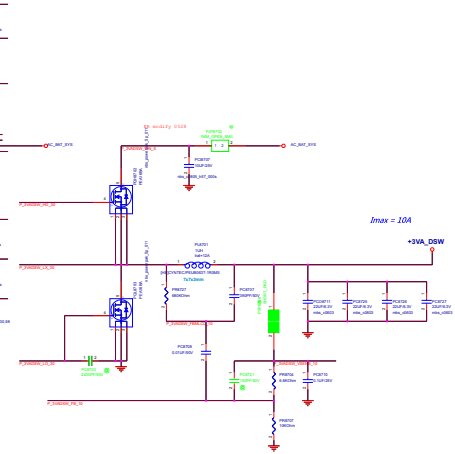


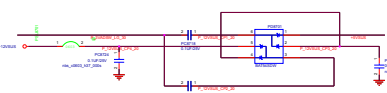
+2.5V



ASUSTeK Computer Inc.		Project Name: UX362FD	Rev: 0.1
TITLE :	PM_+1.2V/+VTT/+2.5V		
Size:	Dept.:	Engineer:	
Date: Friday, July 19, 2019		Sheet	of







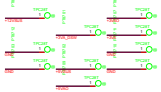
提 check 壓前線路 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (5MV/PB)

	S0	S3	S4	S5	S0i1	S0i3	S0 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.05V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	1	-	0	-	0

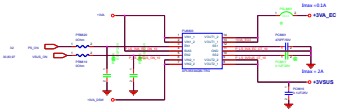
Battery Mode (8MV/PB)

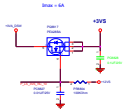
	S0	S3	S4	S5	S0i1	S0i3	S0 with USB Charger+
PS_ON	1	-	-	-	1	0	1
3VADSW_ON	1	-	-	-	1	0	1
5VSUS_ON	1	-	-	-	0	0	0
5VSUS_ON	1	-	-	-	1	0	1
1.05V_ON	1	-	-	-	0	0	0
SUSC_EC#	1	-	-	-	0	0	0
SUSB_EC#	1	-	-	-	0	0	0

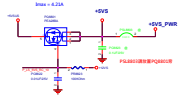


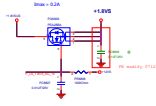
ASUS	Project Name: UX562FD		Rev: 1G.0
Title :	PAC +3VA_DSW/+5VSUS		
Size: Custom	Dept.: ASUSTEK	Engineer: Eason	
Date: Friday, July 13, 2018	Sheet: 67	of: 105	

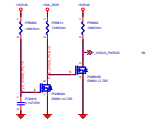
Load Switch

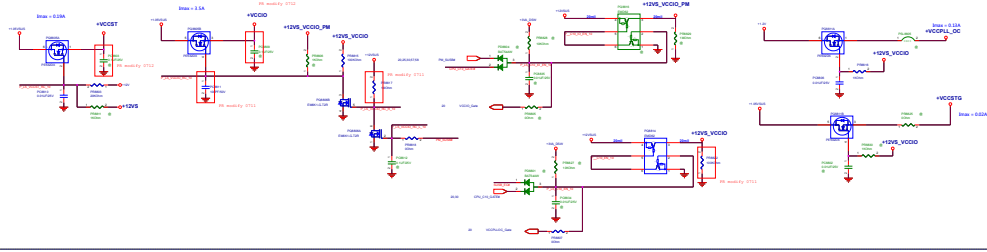




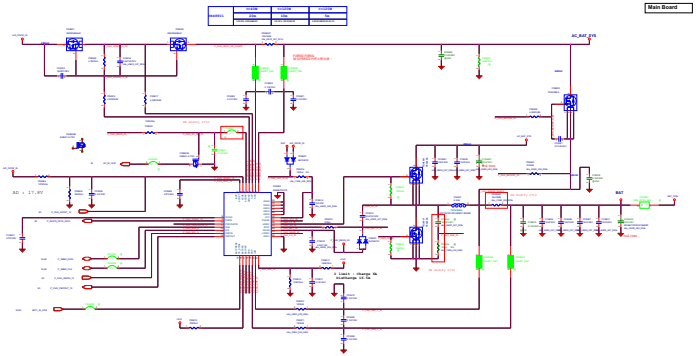


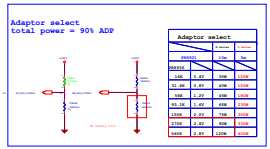




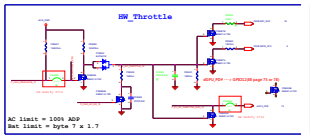


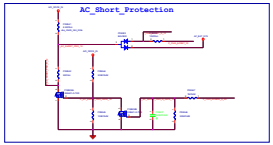
Title = PM_LOAD_SWITCH			
Size:	Project Name:	Rev:	
Date:	Dept.:	Engineer:	
File:		Sheet	of

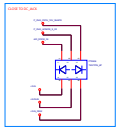




Adaptor select			
PROTO		EVT	
DVT/PVT		MP	
3.6A	1.4V	5A	1.42V
51.4A	1.8V	45W	1.57V
5A	1.2V	6W	1.65V
65.1A	1.4V	65W	1.83V
135A	2.2V	75W	1.92V
271A	2.4V	90W	1.97V
360A	2.8V	120W	1.97V





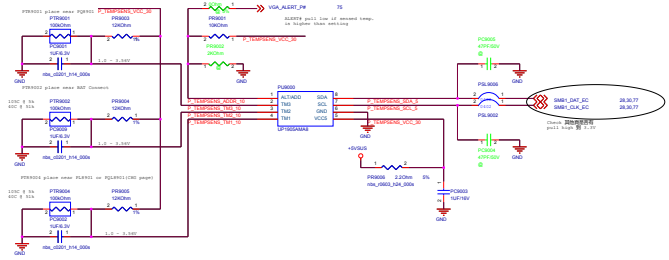


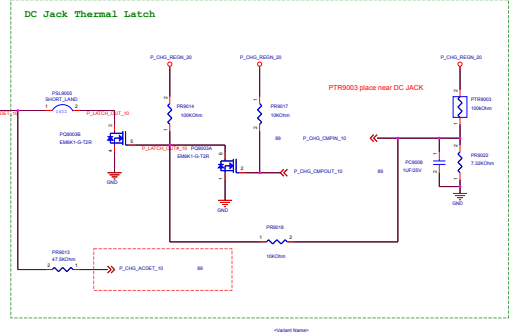
Address Selection Table

Address	0x98	0x9A	0x9C	0x9E	0xA2	0xA4	0xA6
PR9001	10K	1.5K	2K	3.4K	3.9K	5.1K	6K
PR9002	Open	8.2K	9.1K	9.8K	11.7K	13.3K	15K

Register Address

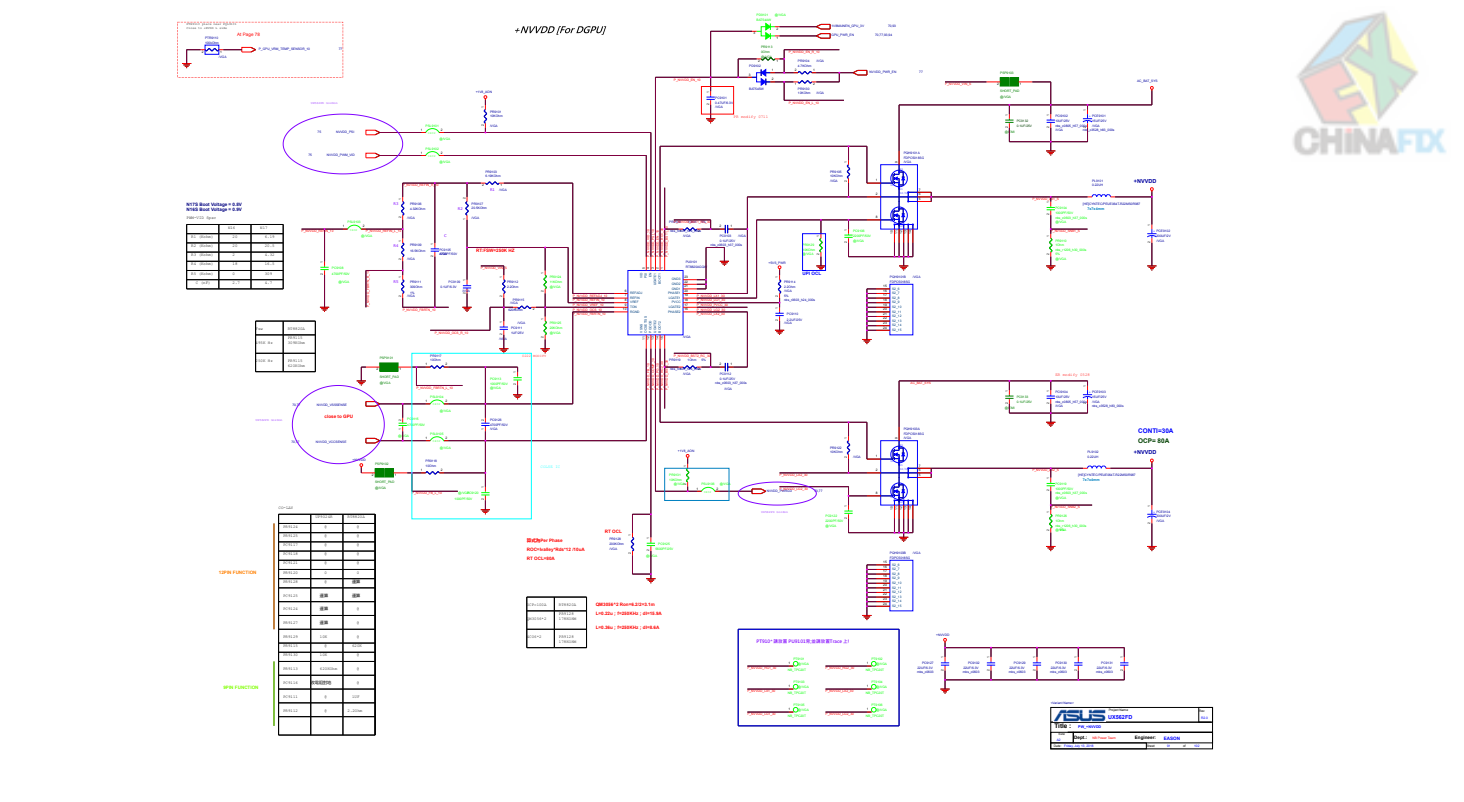
Address	0x01	0x02	0x03	0x04	0x05	0x06
R/W	R	R	R	R	R	R
Function	Temp. alert threshold setting		Second temp. data			bit 6 = 0 bit 5 = 0 bit 0 = 0 Whose ALERT# asserts

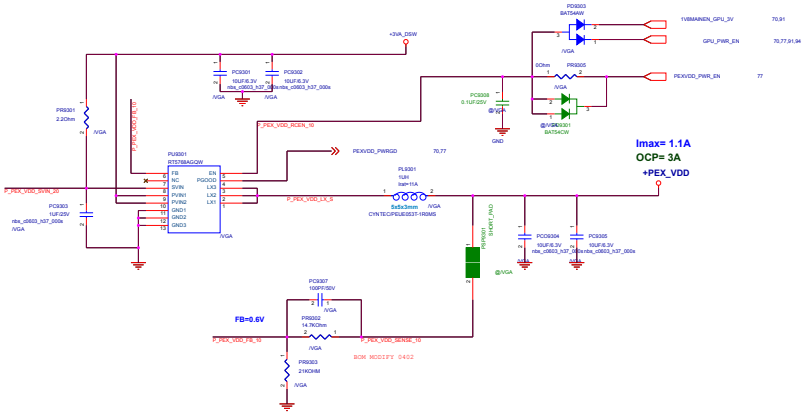




<Variant Name>

ASUS	Project Name: UX562FD		Rev: R2.0
Title : PW_PROTECTION			
Size: A3	Dept.: ASUS	Engineer: SS	
Date: Friday, July 13, 2018	Sheet: 89	of: 102	


+NVVDD [For DGPU]
At Page 79
close to GPU
NVTS Boot Voltage = 0.8V
NVMS Boot Voltage = 0.8V
RT OCL
CONTI=38A
OCP= 80A
+NVVDD
12PIN FUNCTION
9PIN FUNCTION



<Variant Name>

ASUS	Project Name: UX562FD	Rev: R2.0
Title : PW_+1.8V_AON		
Size: A3	Dept.: NB Power Team	Engineer: EASON
Date: Friday, January 13, 2017	Sheet: 83 of 102	

+FBVDDQ [For VRAM]

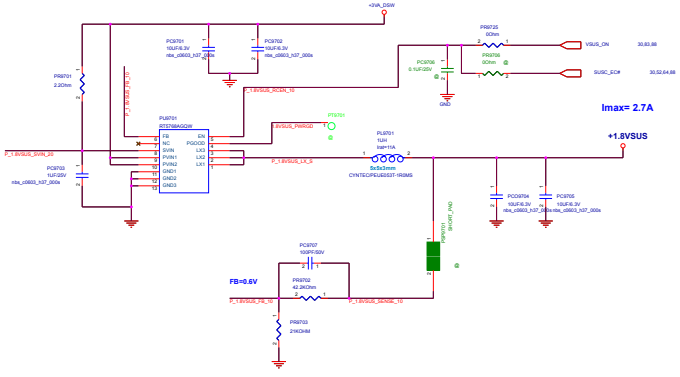
DVS Setting			
	BIT7 &5h Bycle 2 Volume		BIT8 &5h (BIT8 &5h Samecmp)
Voltage	1.35V	Voltage	1.35V
05h313	1030hm	05h313	1030hm
05h314	35.7KOhm	05h314	51.4KOhm
05h315	54.9KOhm	05h315	68.9KOhm

Imax= 20A
OCP= 30A
+FBVDDQ

FSW=300K HZ

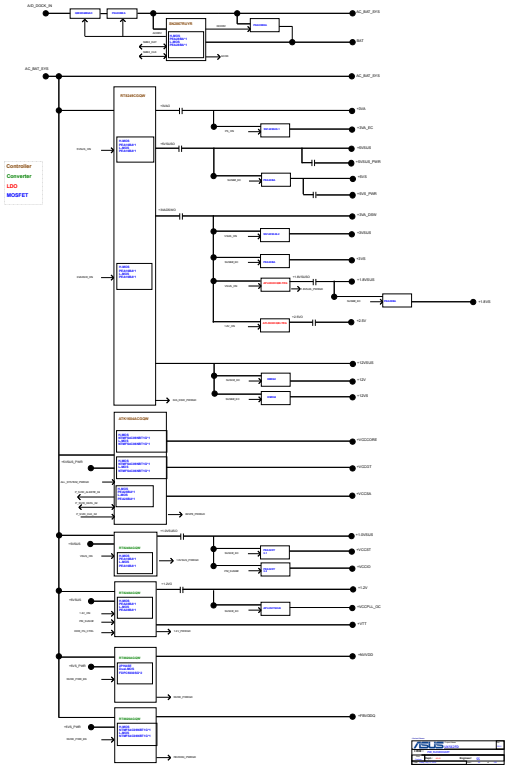
PT910* 建議量 PU9101電源建議量Trace 上下

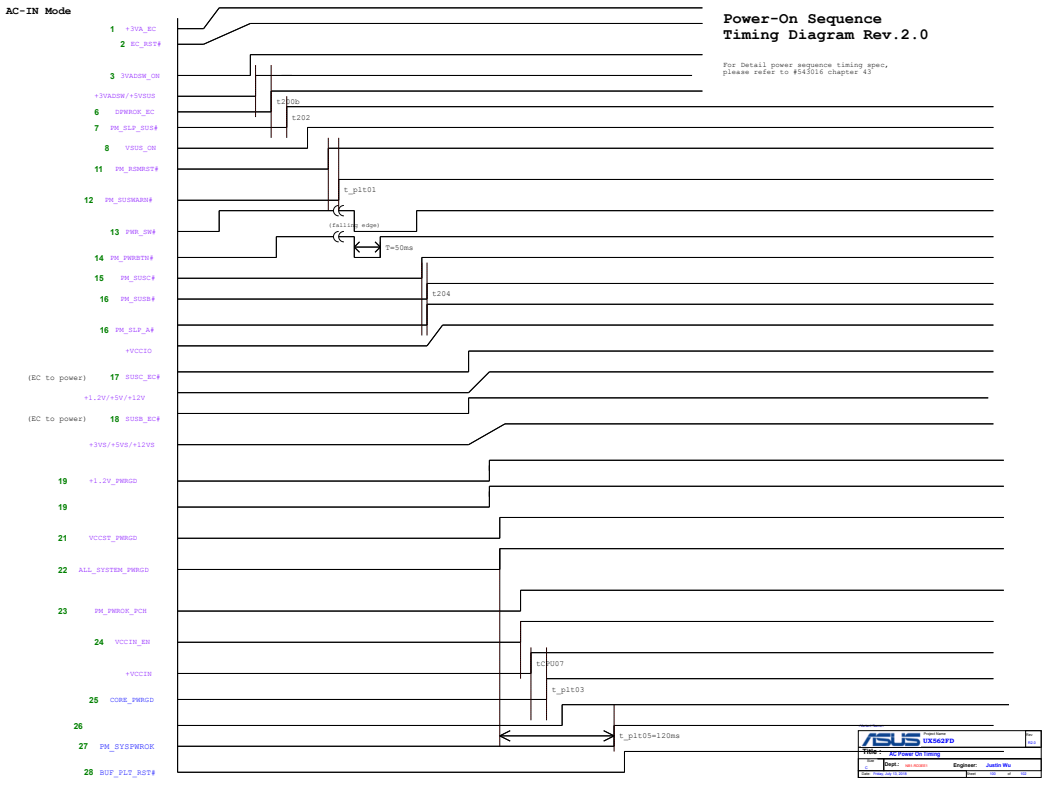
+1.8VSUS [For GPU]



<Variant Name>

ASUS	Project Name: UX562FD	Rev: 0.2.0
Title : PW_+1.8V_AON		
Size: A3	Dept.: NB Power Team	Engineer: EASON
Date: Friday, January 13, 2017	Sheet 67 of 102	


Controller
Converter
LDO
MOSFET
AC_BAT_SYS
+5VALW
+3VALW
+1.8VALW
+1.2V
+0.6V
+CPU_CORE
+VCCGT
+VCCSA
+VCCIO
+VCCPLL_OC
+DDRVDD
+PCH_1.05V


AC-IN Mode
Power-On Sequence
Timing Diagram Rev.2.0
For Detail power sequence timing spec,
please refer to #543016 chapter 43
1 +3VA_EC
2 EC_RST#
3 3VADSW_ON
+3VADSW/+5VSUS
6 DPWROK_EC
7 PM_SLP_SUS#
8 VSUS_ON
11 PM_RSMRST#
12 PM_SUSWARN#
13 PWR_SW#
14 PM_PWRBTN#
15 PM_SUSC#
16 PM_SUSB#
16 PM_SLP_A#
+VCCIO
(EC to power) 17 SUSC_EC#
+1.2V/+5V/+12V
(EC to power) 18 SUSB_EC#
+3VS/+5VS/+12VS
19 +1.2V_PWRGD
19
21 VCCST_PWRGD
22 ALL_SYSTEM_PWRGD
23 PM_PWROK_PCH
24 VCCIN_EN
+VCCIN
25 CORE_PWRGD
26
27 PM_SYSPWROK
28 BUF_PLT_RST#
t200b
t202
t_plt01
(falling edge)
T=50ms
t204
tCPU07
t_plt03
t_plt05=120ms
ASUS
UX562FD
Title: AC Power On Timing
Dept: MS ROBO
Engineer: Justin Wu
Date: Friday, July 13, 2018
Sheet 1 of 1

AC-IN Mode

Power On Sequence Diagram Rev.2.0