NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

ALPHARD

2018.12.27

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			
FILE NAME			
PCB P/N	60.xxxxx.xxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
MAIN BOARD

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 1 of 139

TABLE OF CONTENTS

SMALL BOARD1&2

SMALL BOARD3

FOR 17 SMALL BOARD1&2

GPU PAGE 71-116 FROM PAGE 72

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF THE CONTENT

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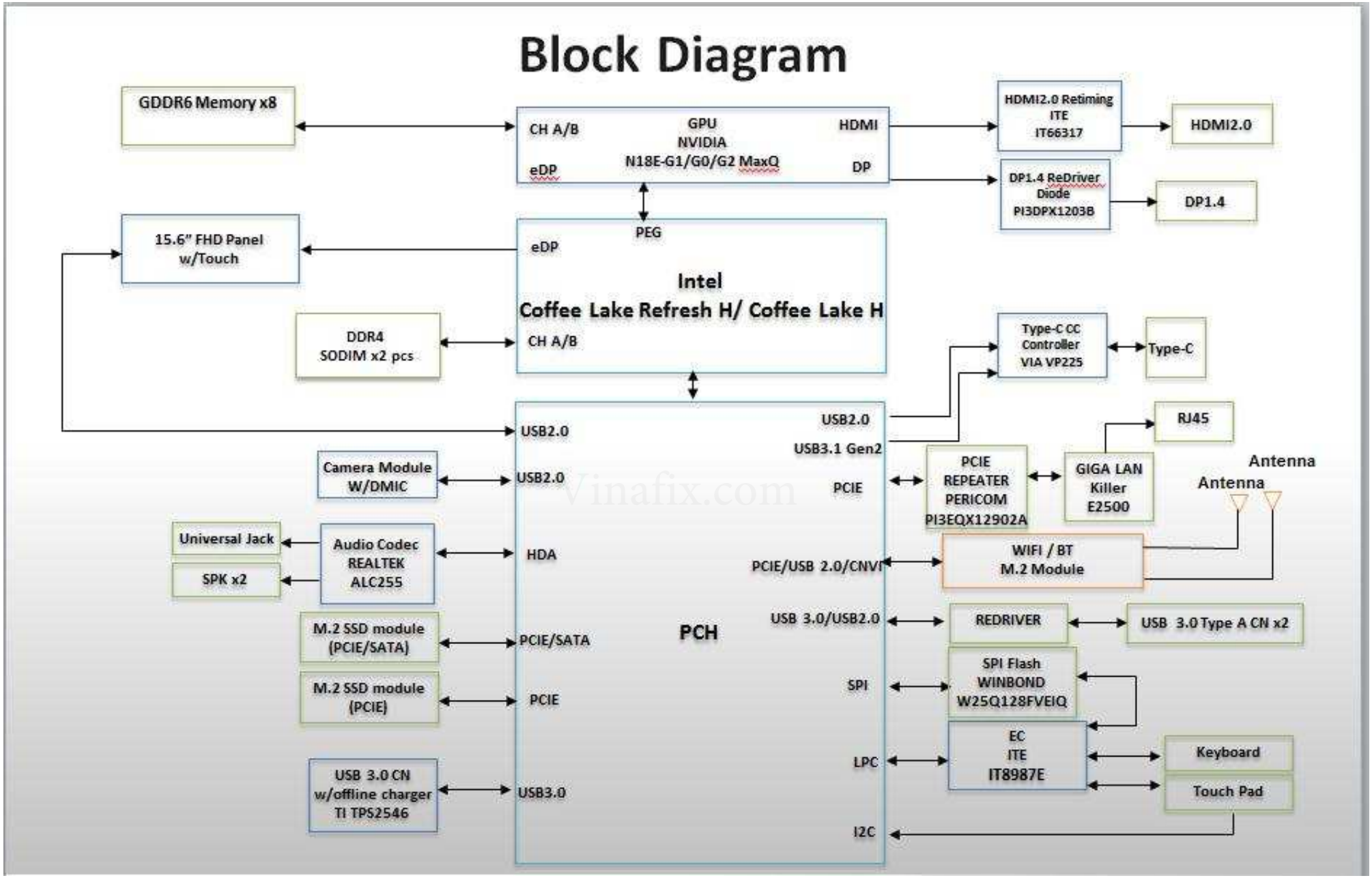
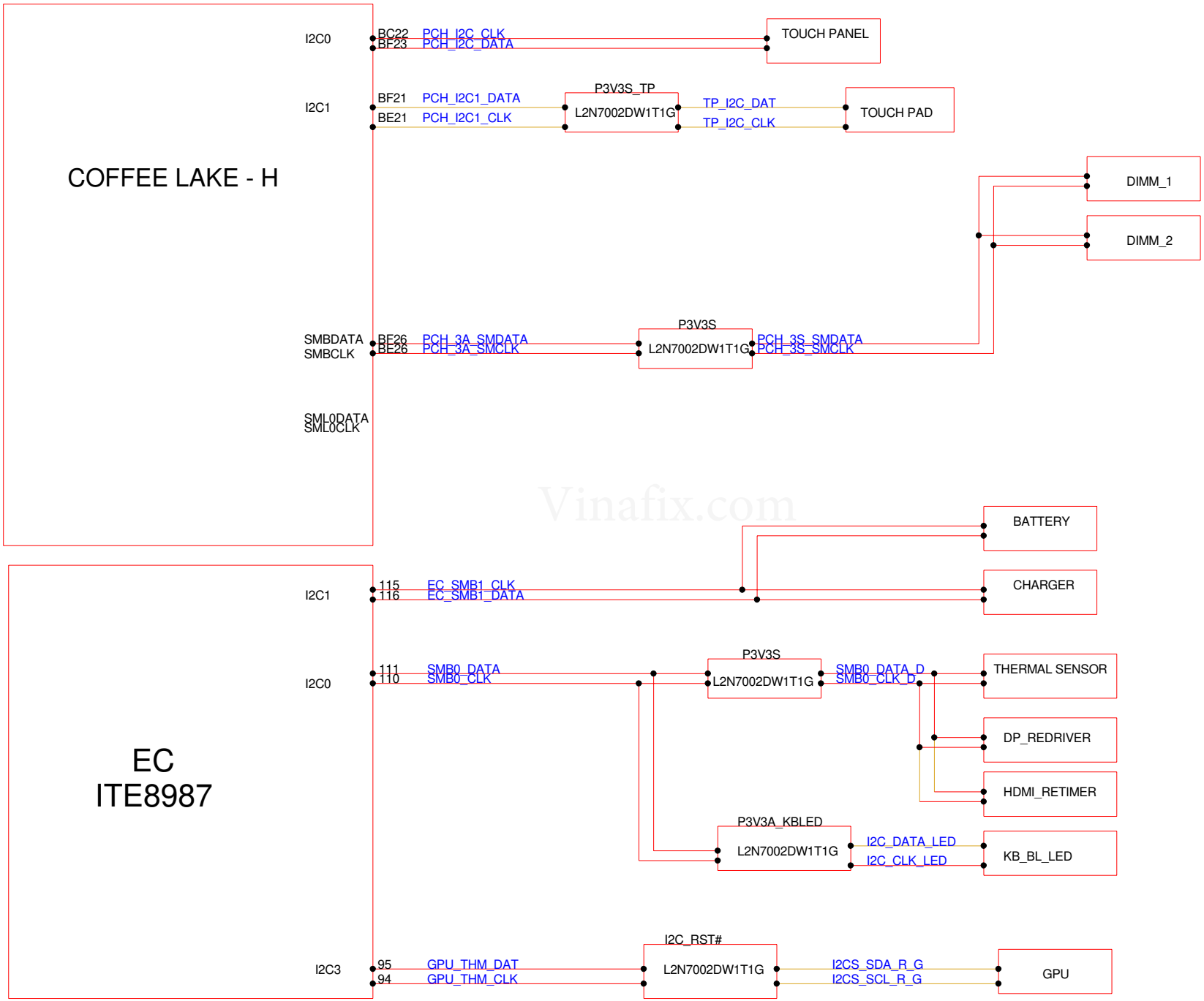
PCB P/N	60xxxxxxxxx	PCB VER	XXX	SHEET 2 of 139			



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 3 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



INVENTEC

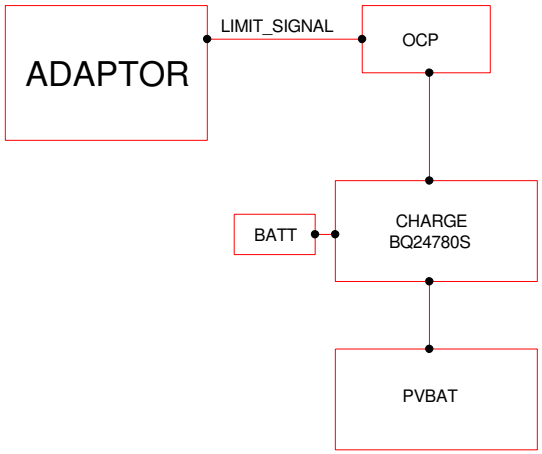
TITLE: MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 4 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

POWER BLOCK



IN/EN		OUT
PVBAT, EN_5V	SY8288CRAC	P5V0DS
PVBAT, EN_5V0	SY8284CRAC	P5V0
PVBAT, EN_3V	NB680AGD	P3V3DS
PVBAT, EN_VDDQ, EN_VTT	NB685AGQ	P1V2, P0V6S
PVBAT, EN_1V05V	SY8288CRAC	P1V05A
PVBAT, EN_VCCIO	NB681GD	PVCCIO
PVBAT, EN_PVCORE	NCP81215MNTXG	PVCORE
PVBAT, VRACPU_DRVON	NCP81151MNTBG	PVCCGT
PVBAT, VRACPU_DRVON	NCP81253MNTBG	PVCCSA

IN/EN		OUT
P5V0DS, EN_2V5	RT8097ALGE	P2V5
P3V3DS, EN_1V8	SY8088AAC	P1V8A
P3V3DS, P3V3A_5A_PWEN, CORE_PWEN	APL3523A	P3V3A, P3V3S
P5V0DS, CORE_PWEN, P1V8A, CORE_PWEN	APL3523A	P5V0S, P1V8S
P1V2, VCCPLL_OC_EN	PM514BA	VCCPLL_OC
P1V05A, RESUME_PWEN, CORE_PWEN	APL3523A	PVCCSTG, PVCCST

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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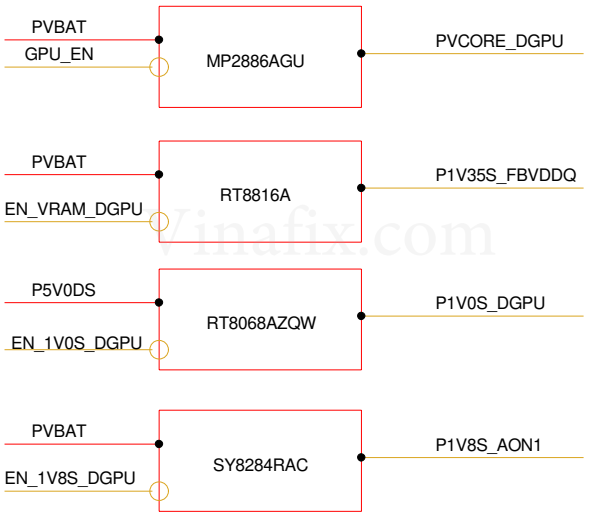
GPU POWER BLOCK

IN/EN OUT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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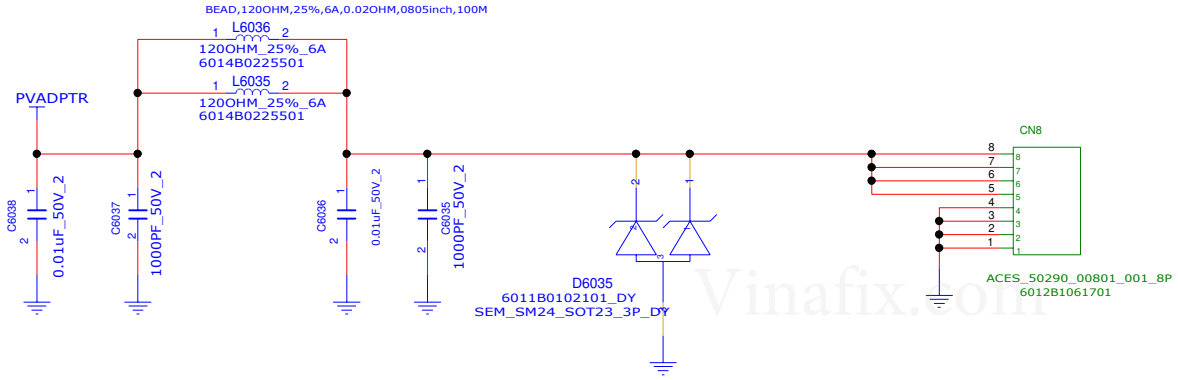

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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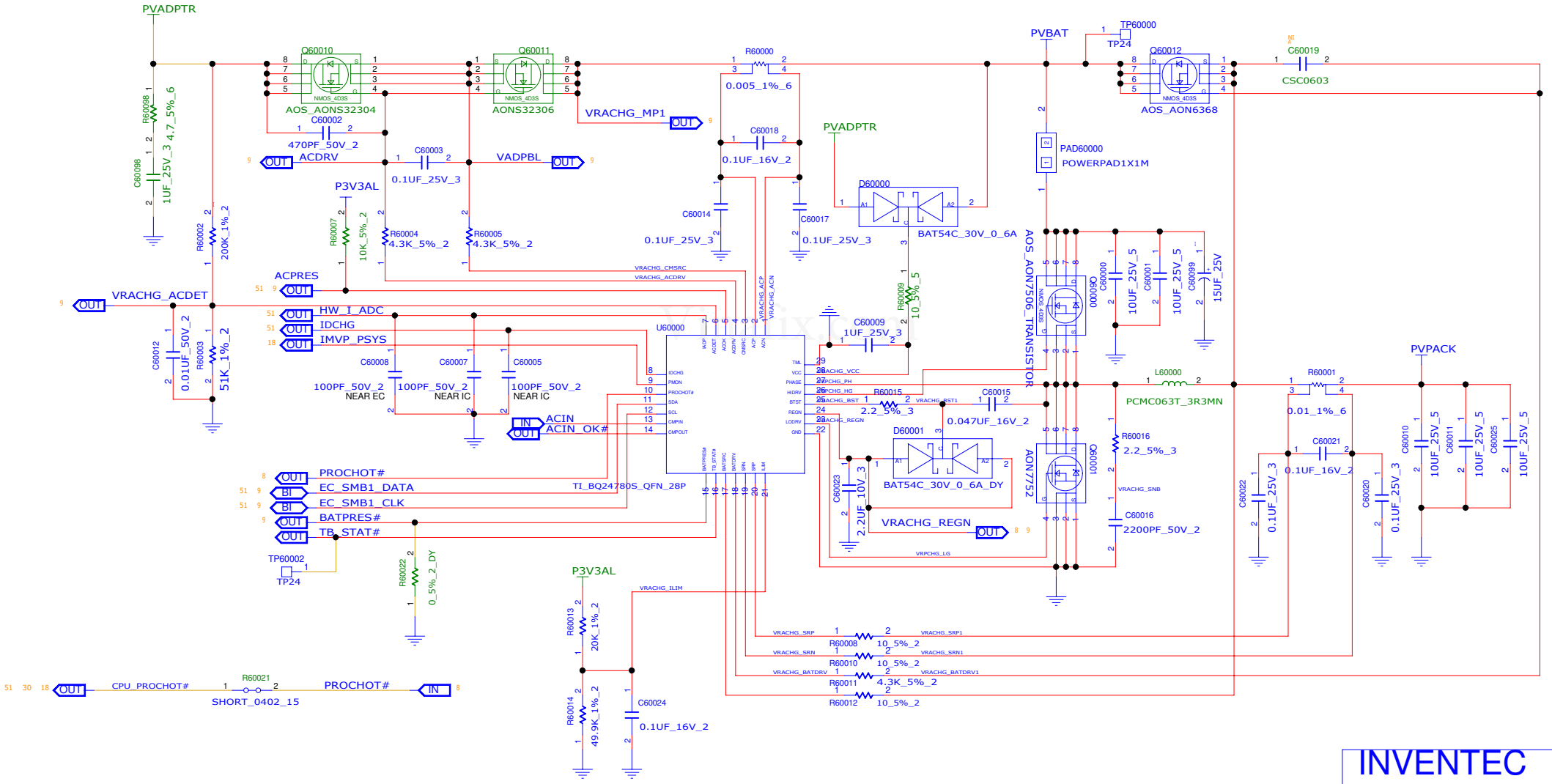


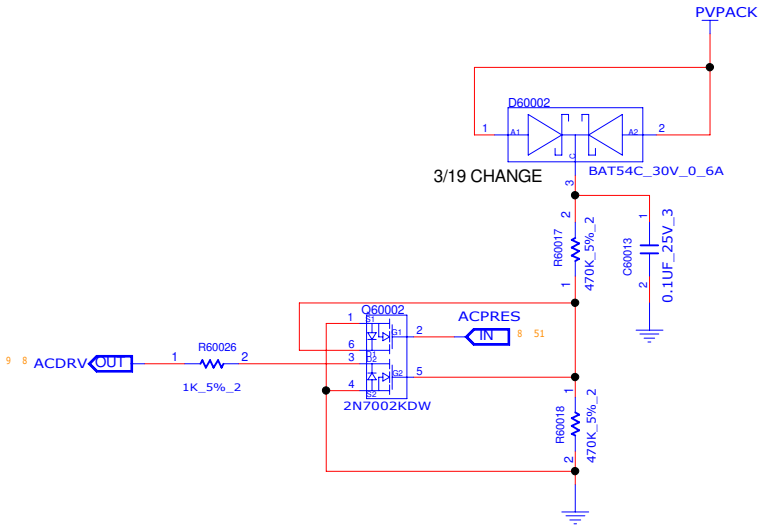
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 8 of 139			

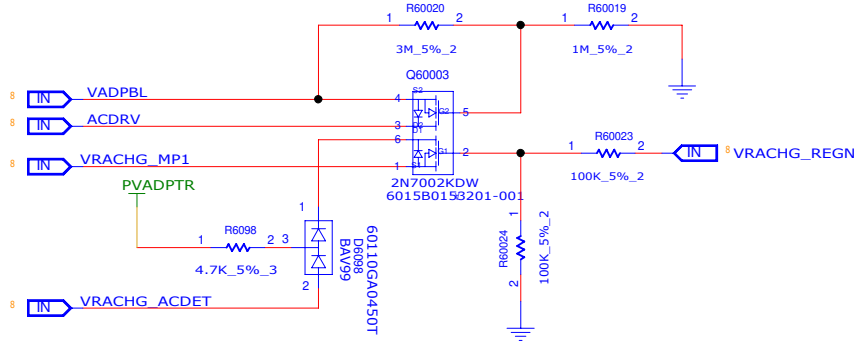
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

FOR CHARGER

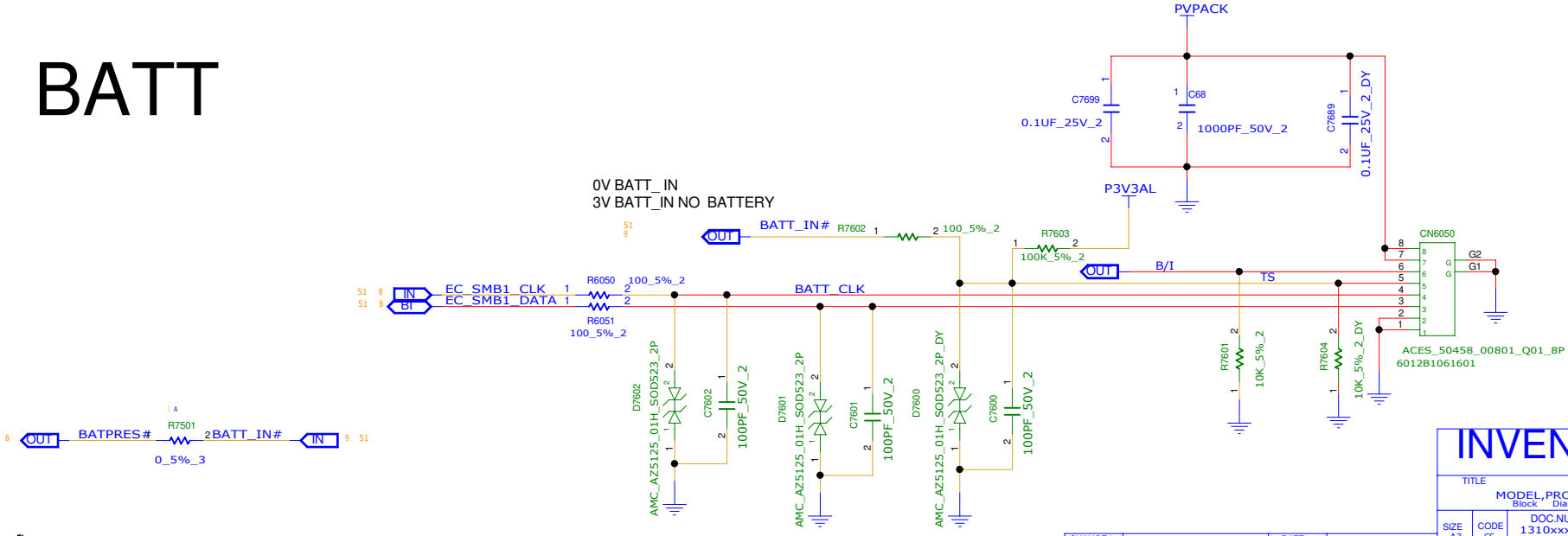
SCP



ARP



BATT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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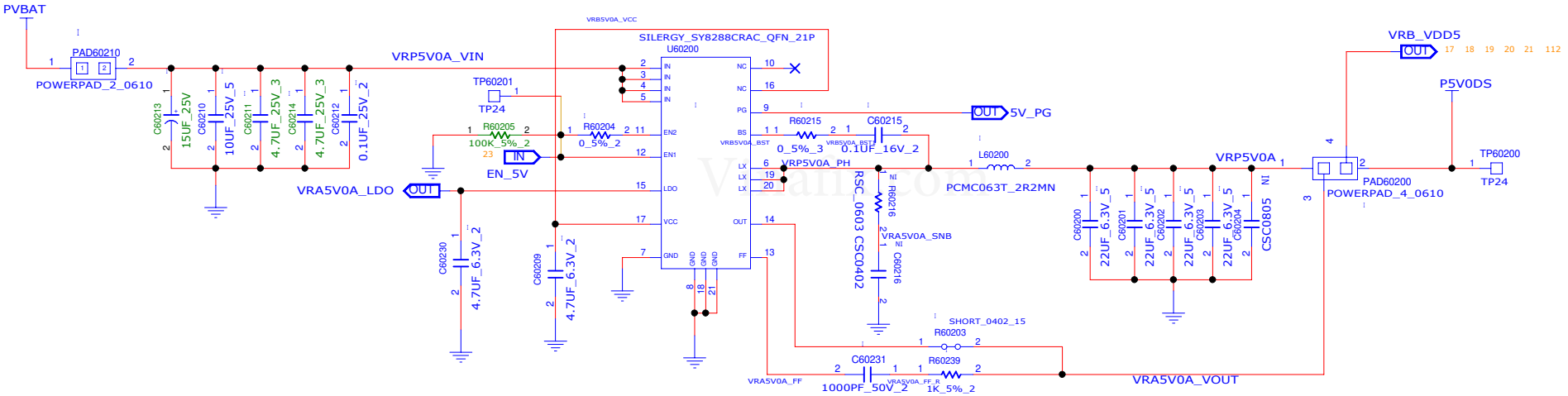
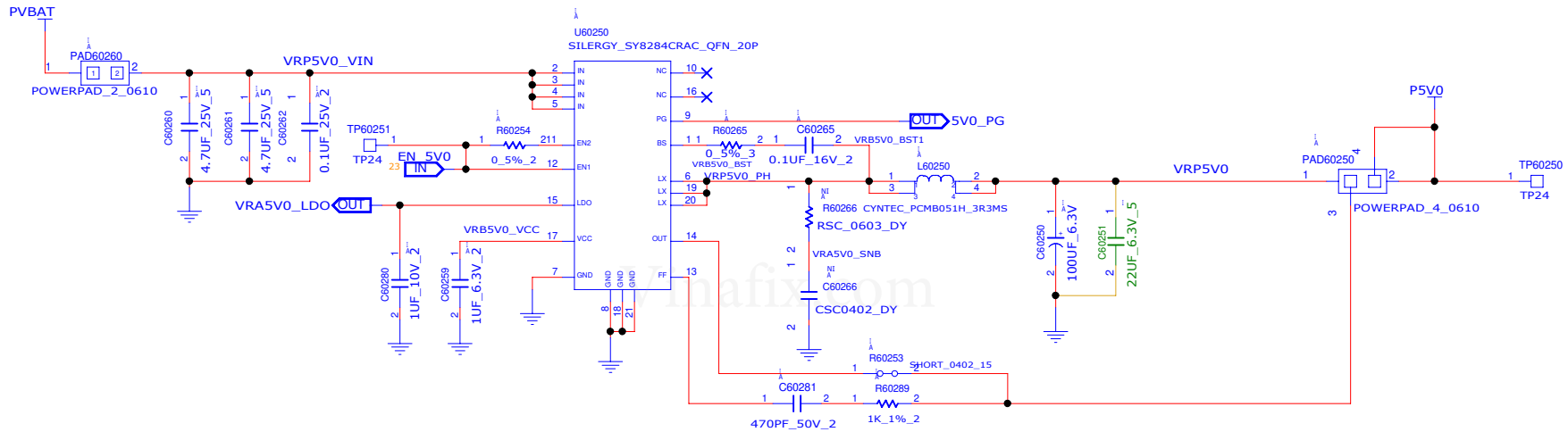


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P5V0DS		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 10 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE: MODEL_PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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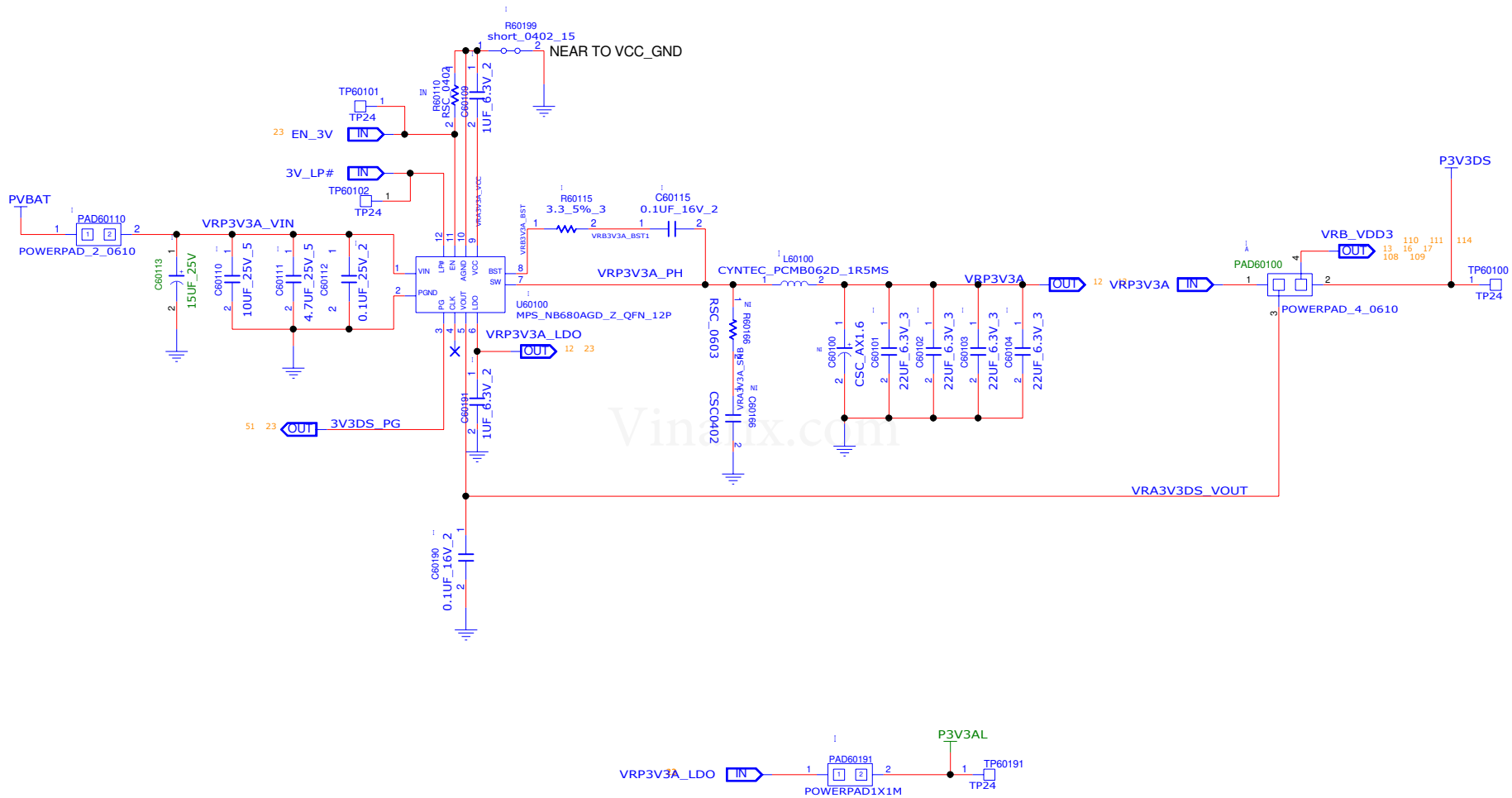
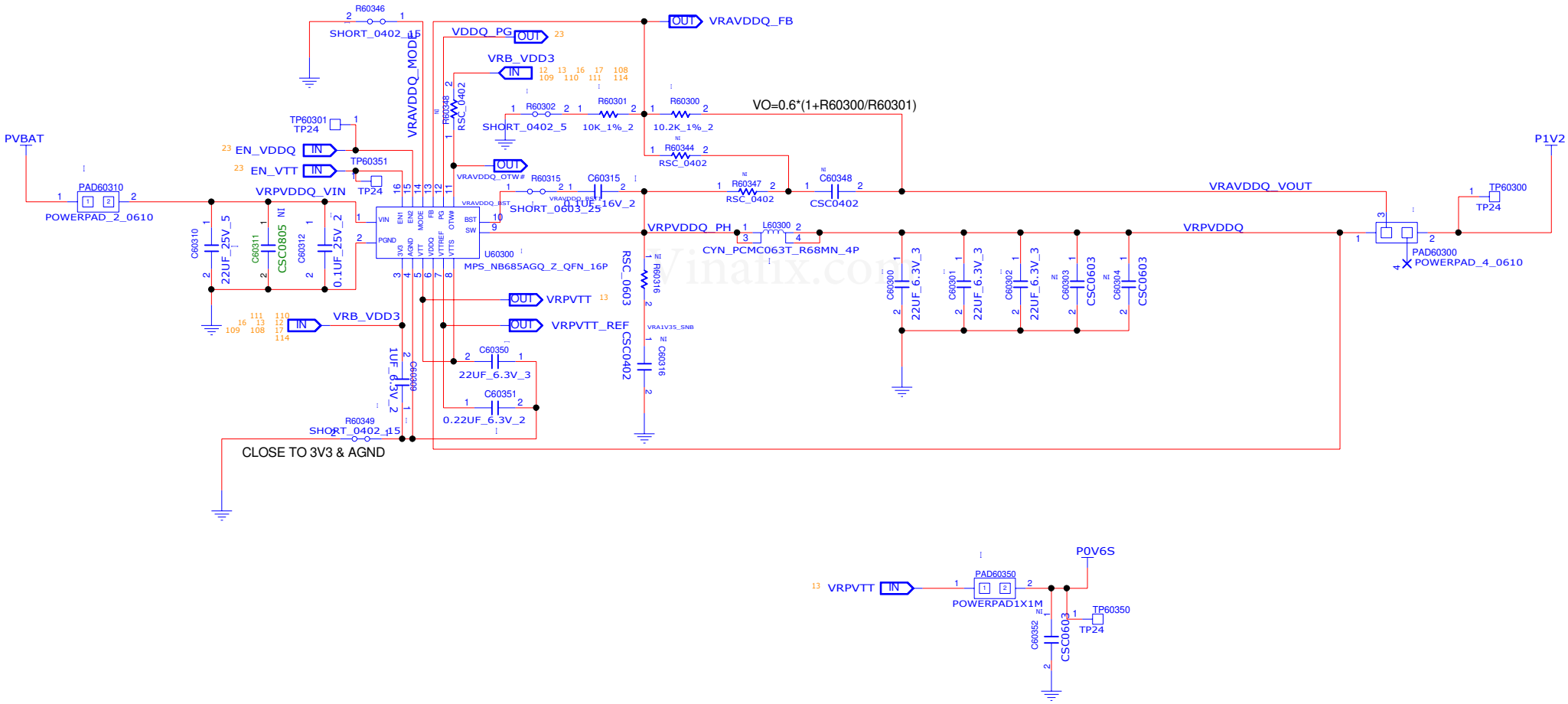


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P3V3DS_NB680A
SIZE	A3
CODE	CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	12 of 139
CHANGE by	XXX
PCB P/N	60xxxxxxxxxx
DATE	21-OCT-2002
PCB VER	XXX

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
VDDQ

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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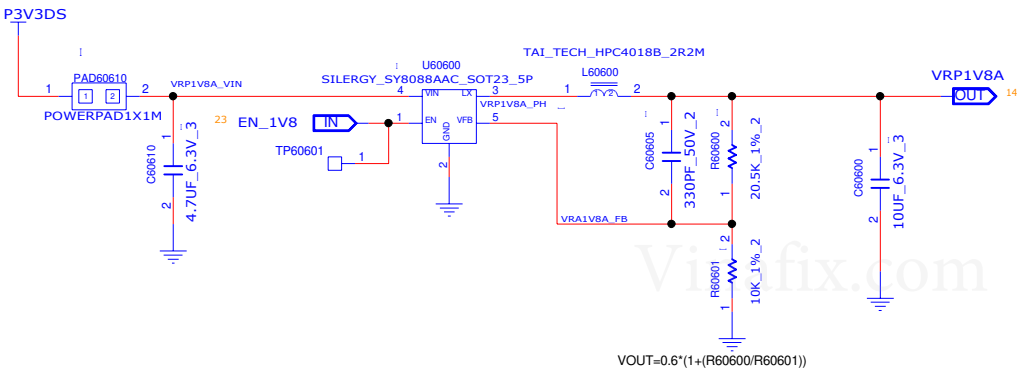

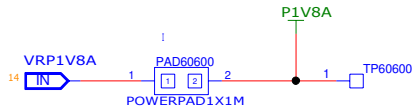

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
P1V8DS

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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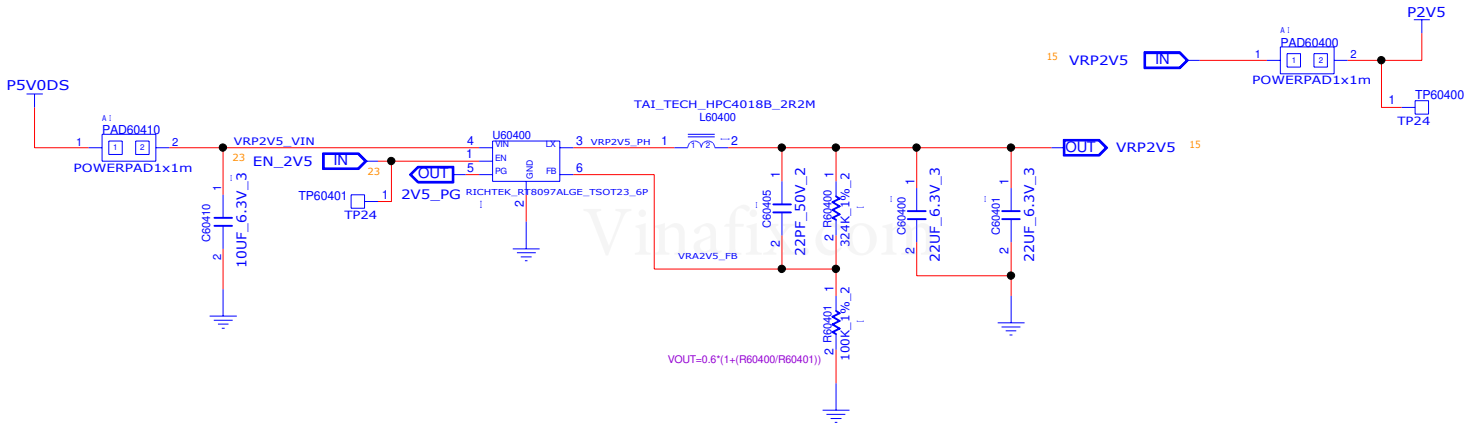

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P2V5

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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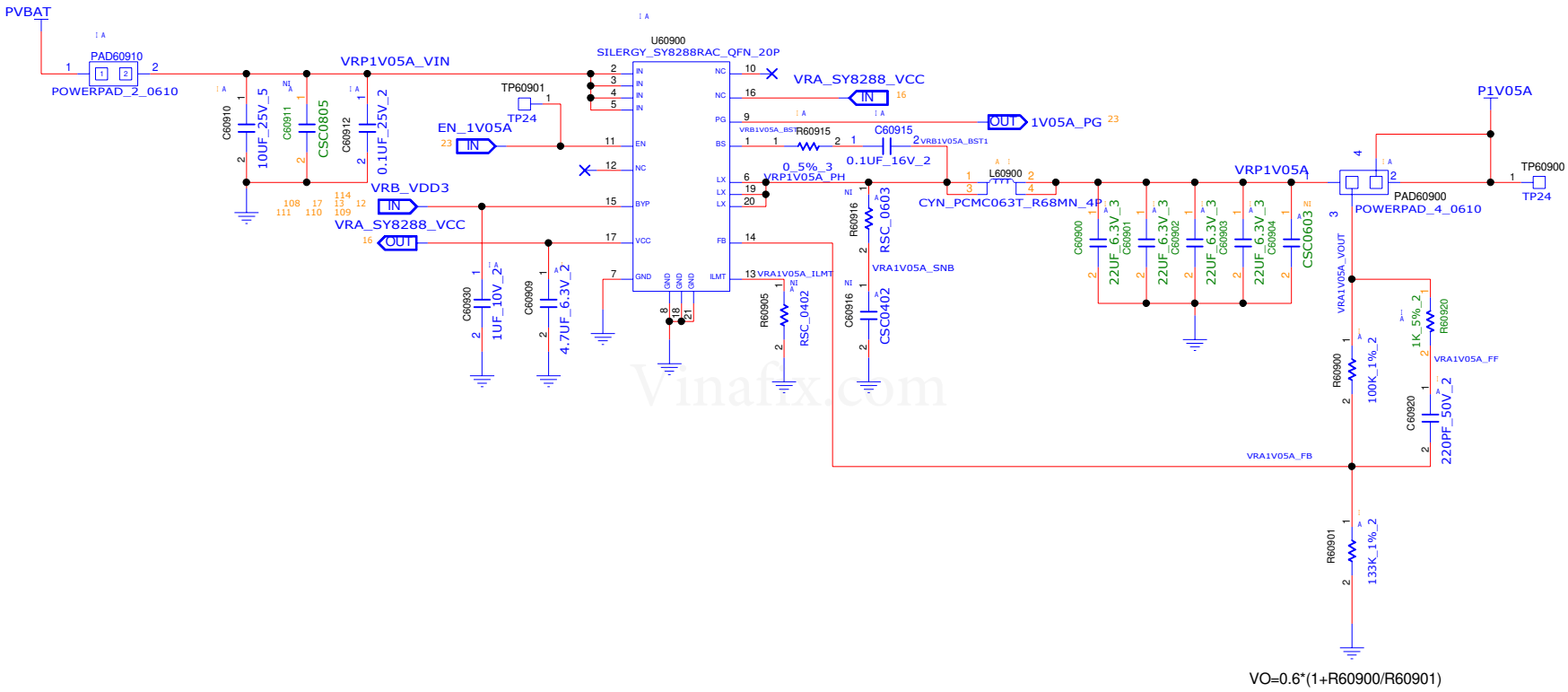

VO=0.6*(1+R60900/R60901)

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P1V0A

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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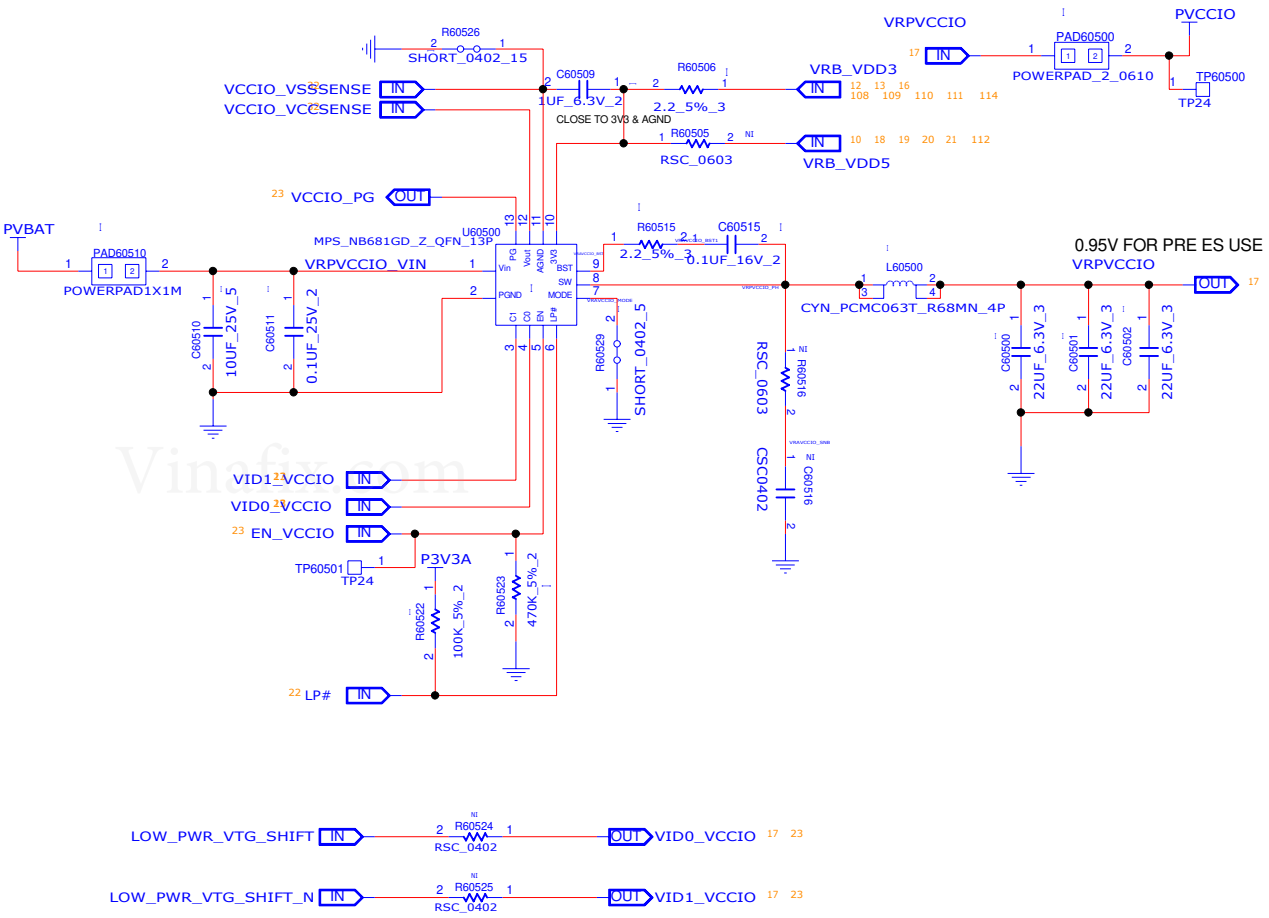
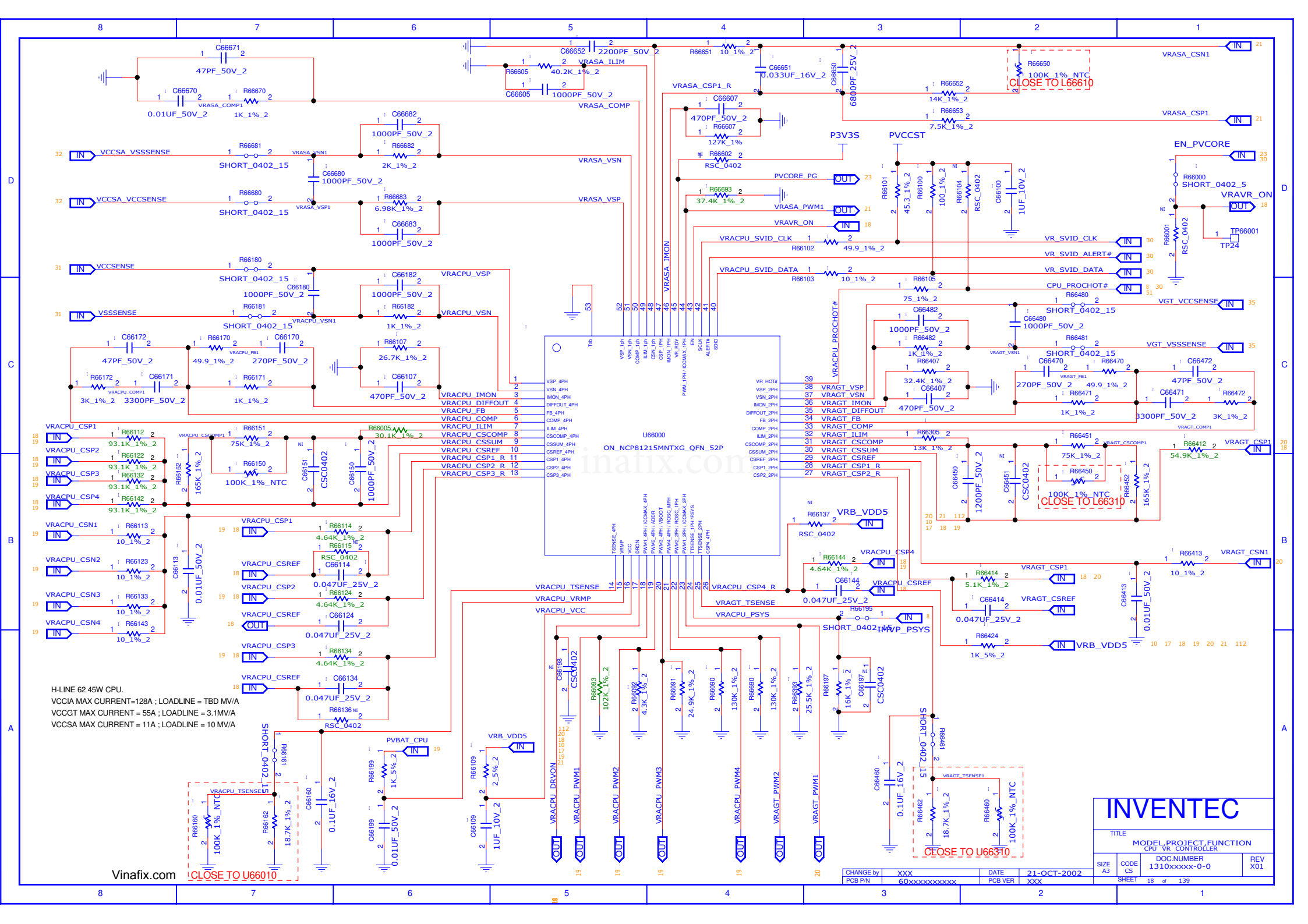
MODE	VR Rail	Resistor to GND (1% accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230 K
M3	EDRAM/V1.0A/EOPIO	100 K
M4	Others	150 K

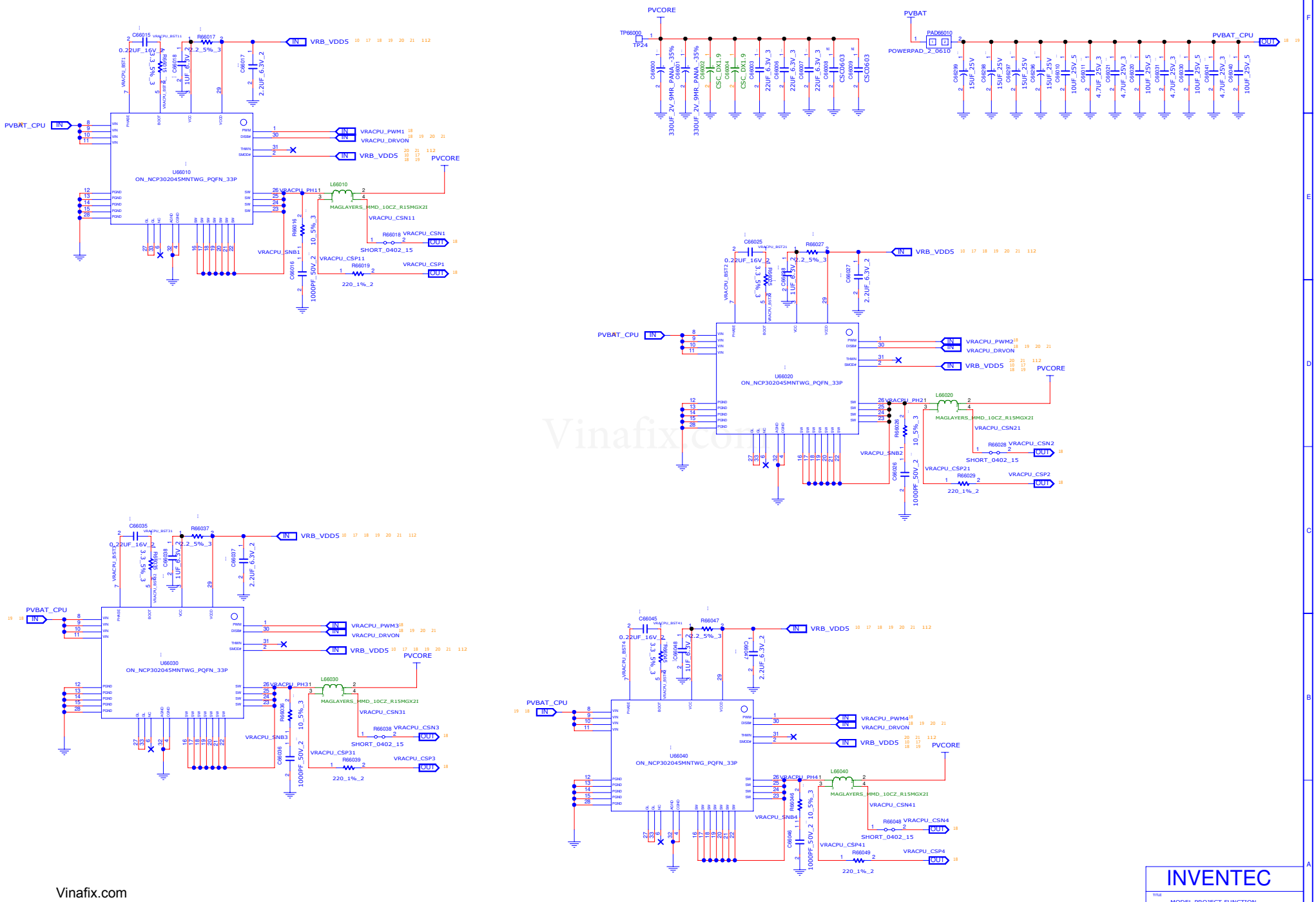
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

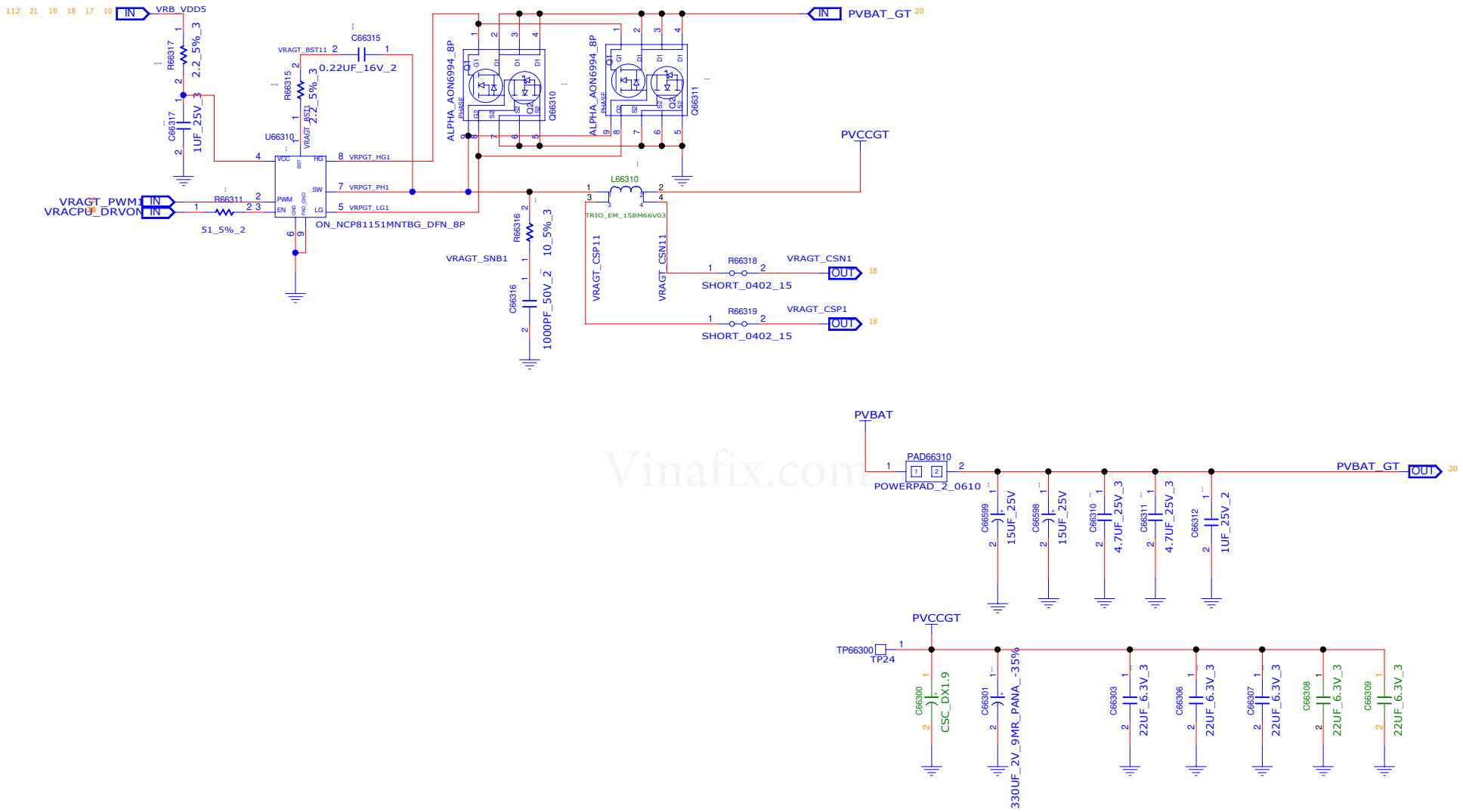


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PVCCIO		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 17 of 139	
PCB P/N 60xxxxxxxxx	PCB VER XXX		


U66000
ON_NCP81215MNTXG_QFN_52P
H-LINE 62 45W CPU.
VCCIA MAX CURRENT=128A ; LOADLINE = TBD MV/A
VCCGT MAX CURRENT = 55A ; LOADLINE = 3.1MV/A
VCCSA MAX CURRENT = 11A ; LOADLINE = 10 MV/A
CLOSE TO L66610
CLOSE TO L66310
CLOSE TO U66310
CLOSE TO U66010
Vinafix.com
INVENTEC
MODEL,PROJECT,FUNCTION
CPU VR CONTROLLER
DOC.NUMBER
1310xxxxx-0-0
REV X01
SIZE A3
CODE CS
SHEET 18 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX


PVCORE
PVBAT
PVBAT_CPU
VRB_VDD5
VRACPU_PWM1
VRACPU_DRVON
VRACPU_PWM2
VRACPU_PWM3
VRACPU_PWM4
U66010
U66020
U66030
U66040
ON_NCP302045MNTWG_PQFN_33P
MAGLAYERS_MMD_10CZ_R15MGX2I
SHORT_0402_15
VRACPU_CSN1
VRACPU_CSN2
VRACPU_CSN3
VRACPU_CSN4
VRACPU_CSP1
VRACPU_CSP2
VRACPU_CSP3
VRACPU_CSP4
Vinafix.com
INVENTEC
MODEL,PROJECT,FUNCTION
PVCORE



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PVCCGT		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX
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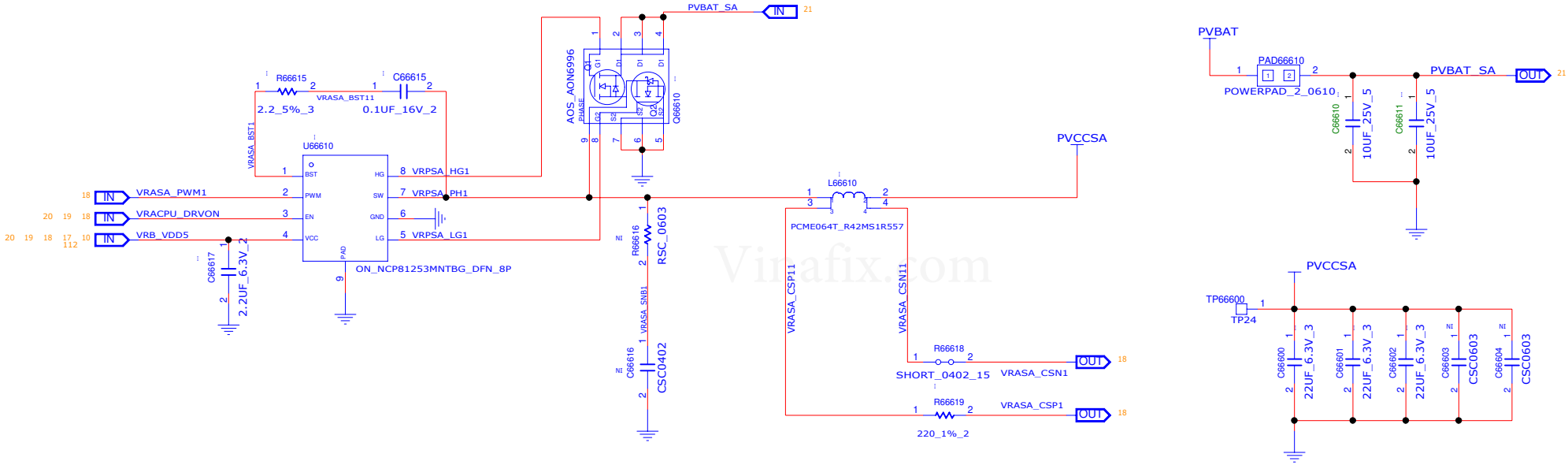

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCSA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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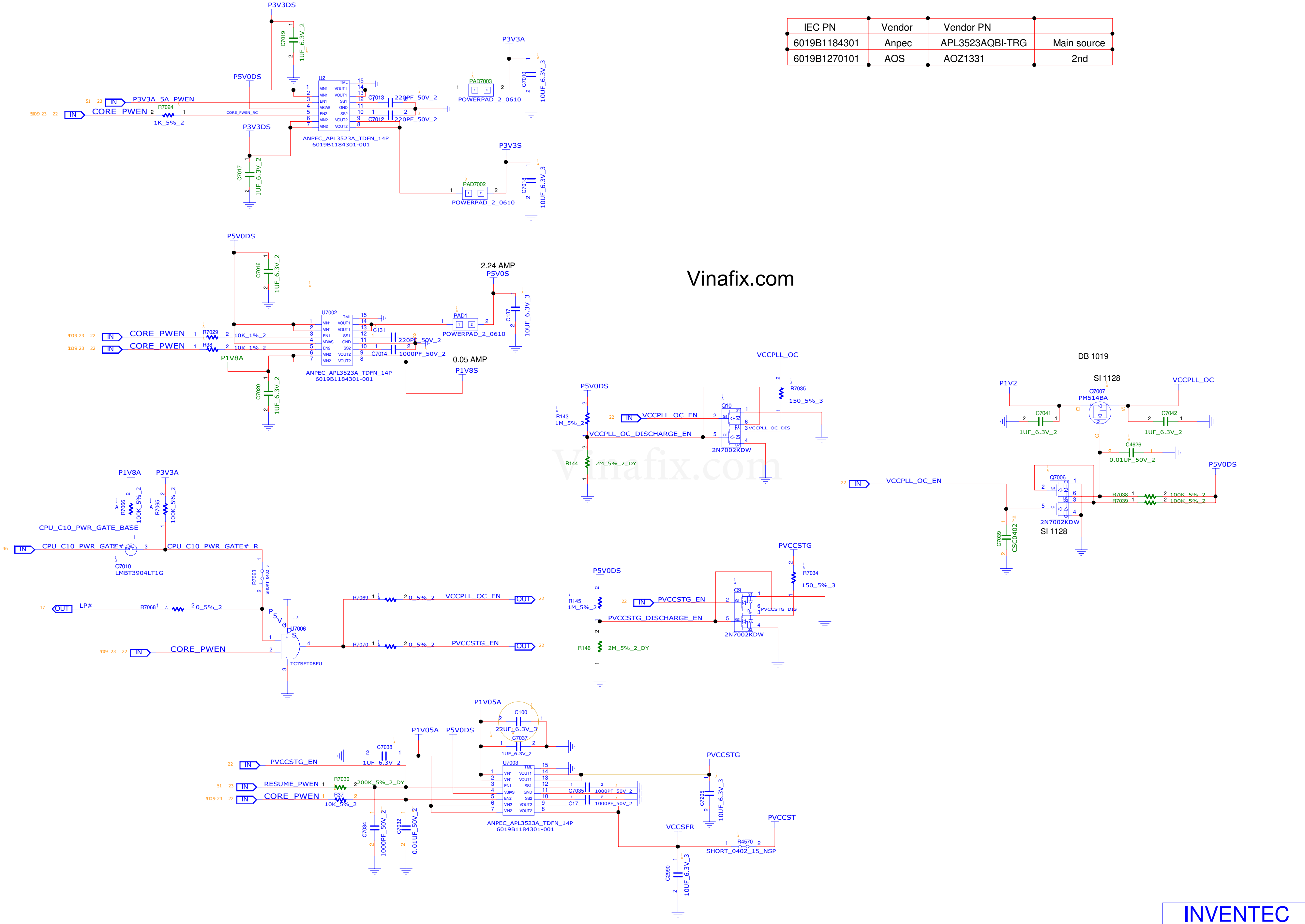
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

IEC PN	Vendor	Vendor PN	
6019B1184301	Anpec	APL3523AQBI-TRG	Main source
6019B1270101	AOS	AOZ1331	2nd



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Vinafix.com

INVENTEC

TITLE MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

CHANGE by	XXX	DATE		SIZE	CODE	DOC.NUMBER	REV
PCB P/N	60xxxxxxxx	PCB VER		C	CS	1310xxxxx-0-0	X01
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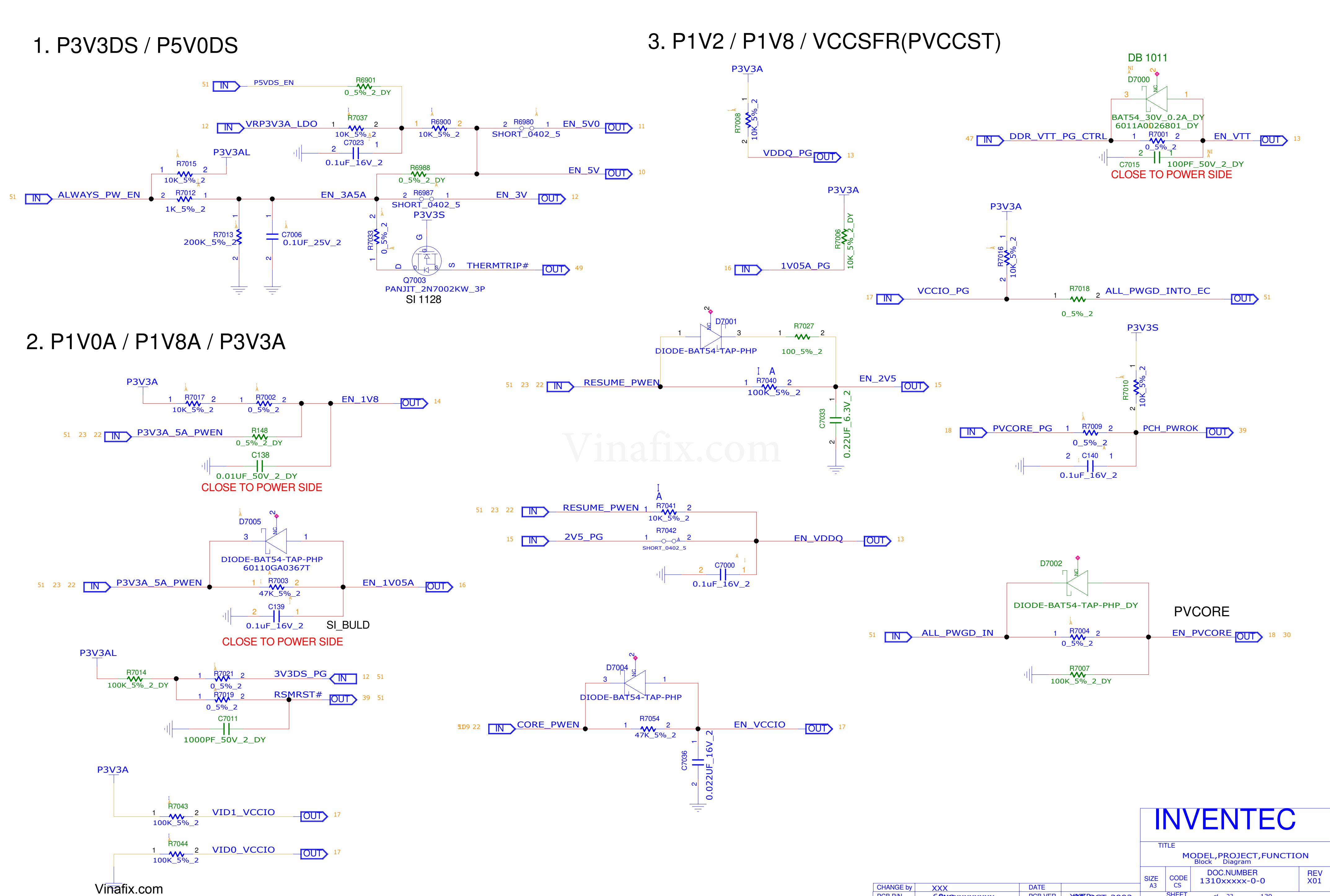


1. P3V3DS / P5V0DS
P5VDS_EN
R6901 0_5%_2_DY
VRP3V3A_LDO
R7037 10K_5%_2
R6900 10K_5%_2
R6980 SHORT_0402_5
EN_5V0
C7023 0.1uF_16V_2
P3V3AL
R7015 10K_5%_2
R6988 0_5%_2_DY
EN_5V
ALWAYS_PW_EN
R7012 1K_5%_2
EN_3A5A
R6987 SHORT_0402_5
EN_3V
P3V3S
R7013 200K_5%_2
C7006 0.1UF_25V_2
R7033 0_5%_2
THERMTRIP#
Q7003 PANJIT_2N7002KW_3P
SI 1128
2. P1V0A / P1V8A / P3V3A
P3V3A
R7017 10K_5%_2
R7002 0_5%_2
EN_1V8
P3V3A_5A_PWEN
R148 0_5%_2_DY
C138 0.01UF_50V_2_DY
CLOSE TO POWER SIDE
D7005
DIODE-BAT54-TAP-PHP 60110GA0367T
P3V3A_5A_PWEN
R7003 47K_5%_2
EN_1V05A
C139 0.1uF_16V_2
SI_BULD
CLOSE TO POWER SIDE
P3V3AL
R7014 100K_5%_2_DY
R7021 0_5%_2
3V3DS_PG
R7019 0_5%_2
RSMRST#
C7011 1000PF_50V_2_DY
P3V3A
R7043 100K_5%_2
VID1_VCCIO
R7044 100K_5%_2
VID0_VCCIO
Vinafix.com
3. P1V2 / P1V8 / VCCSFR(PVCCST)
P3V3A
R7008 10K_5%_2
VDDQ_PG
P3V3A
R7006 10K_5%_2_DY
1V05A_PG
D7001 DIODE-BAT54-TAP-PHP
R7027 100_5%_2
RESUME_PWEN
R7040 100K_5%_2
EN_2V5
C7033 0.22UF_6.3V_2
RESUME_PWEN
R7041 10K_5%_2
2V5_PG
R7042 SHORT_0402_5
EN_VDDQ
C7000 0.1uF_16V_2
D7004 DIODE-BAT54-TAP-PHP
CORE_PWEN
R7054 47K_5%_2
EN_VCCIO
C7036 0.022UF_16V_2
DB 1011
D7000
BAT54_30V_0.2A_DY 6011A0026801_DY
DDR_VTT_PG_CTRL
R7001 0_5%_2
EN_VTT
C7015 100PF_50V_2_DY
CLOSE TO POWER SIDE
P3V3A
R7016 10K_5%_2
VCCIO_PG
R7018 0_5%_2
ALL_PWGD_INTO_EC
P3V3S
R7010 10K_5%_2
PVCORE_PG
R7009 0_5%_2
PCH_PWROK
C140 0.1uF_16V_2
D7002 DIODE-BAT54-TAP-PHP_DY
PVCORE
ALL_PWGD_IN
R7004 0_5%_2
EN_PVCORE
R7007 100K_5%_2_DY

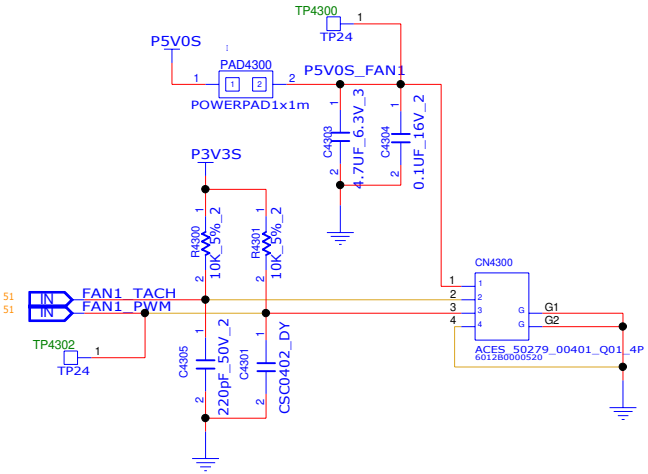
INVENTEC

TITLE MODEL,PROJECT,FUNCTION Block Diagram

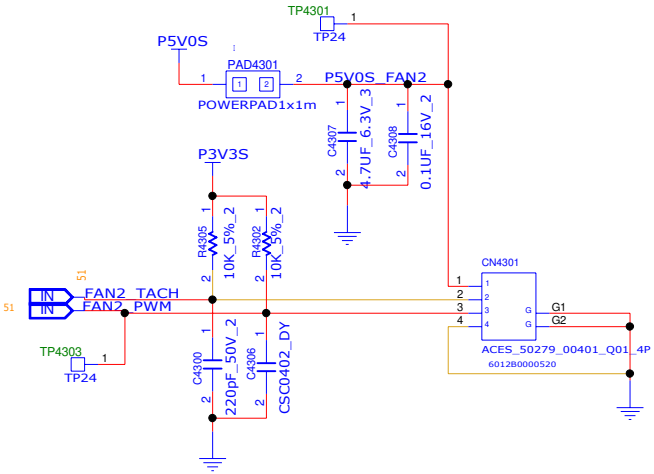
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE XX-OCT-2002
PCB P/N 6050xxxxxxxx PCB VER

REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
FAN & THERMAL

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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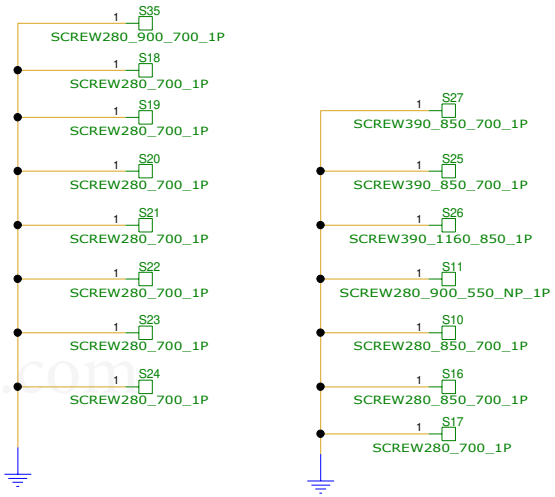
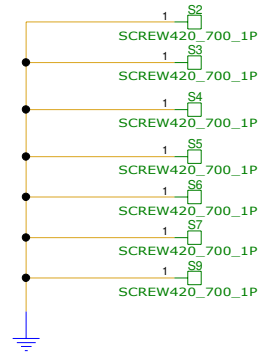
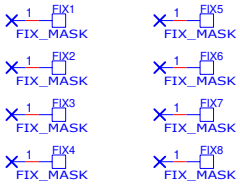
REFERENCE 0~49(PCB SCREW)



PCB





CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
XDP & ME CONN.

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 25 of 139

INTEL_J43242_BGA_1440P

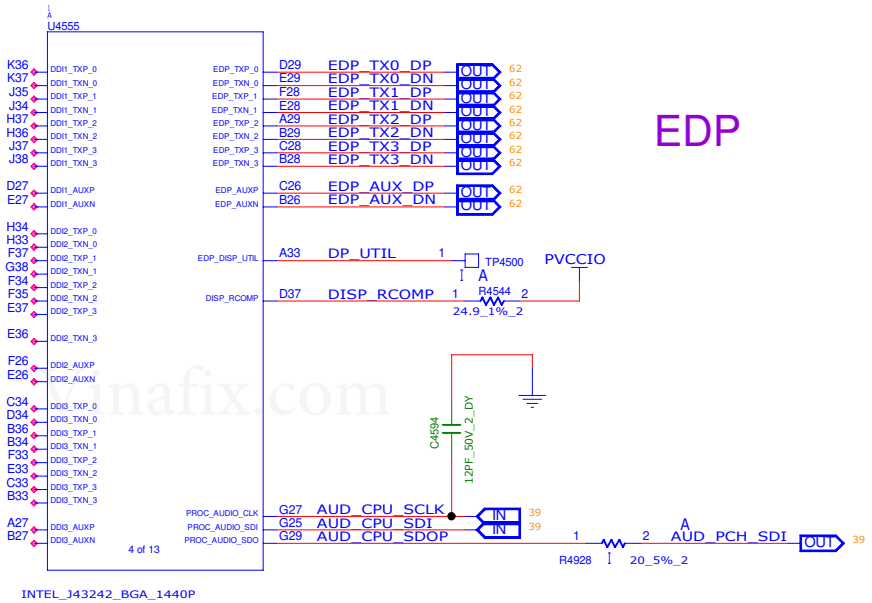
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE1_H-PEG,HDMI

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 26 of 139

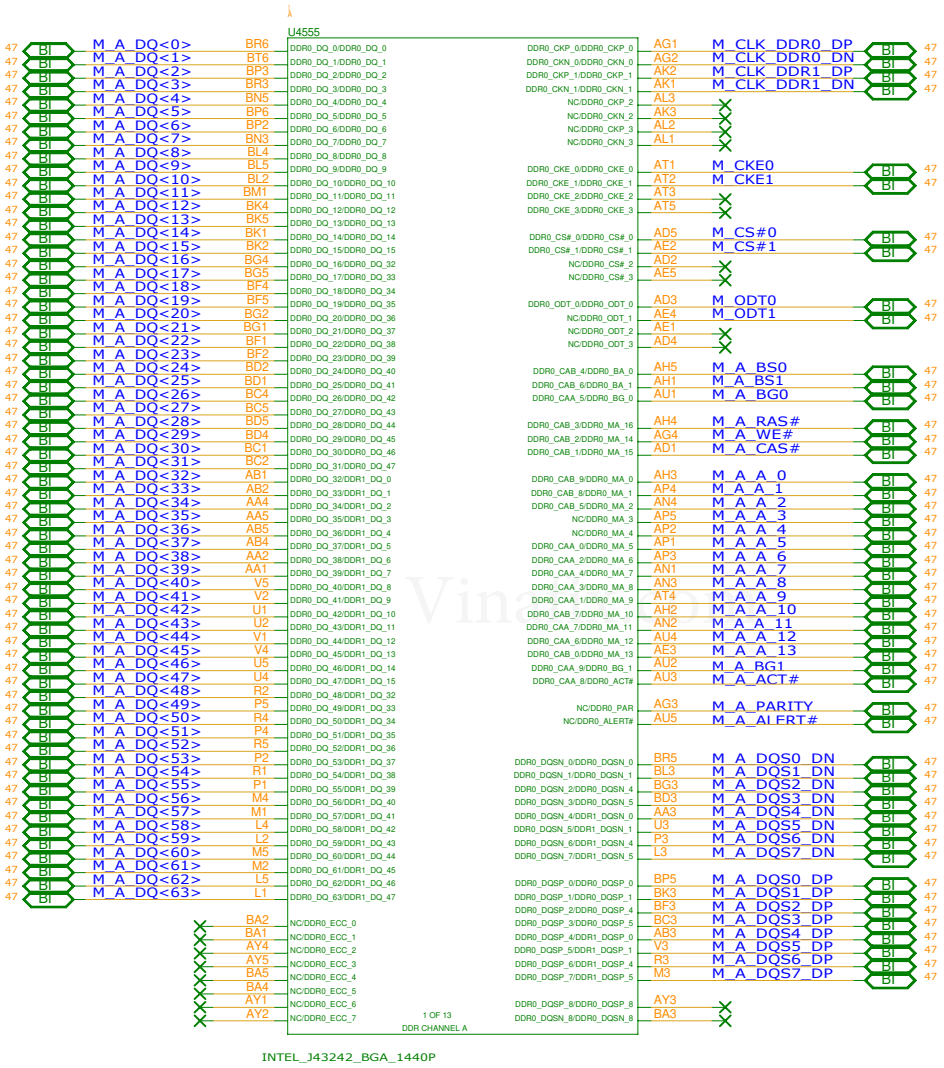
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SKYLAKE2_H-DDI,EDP		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 27 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



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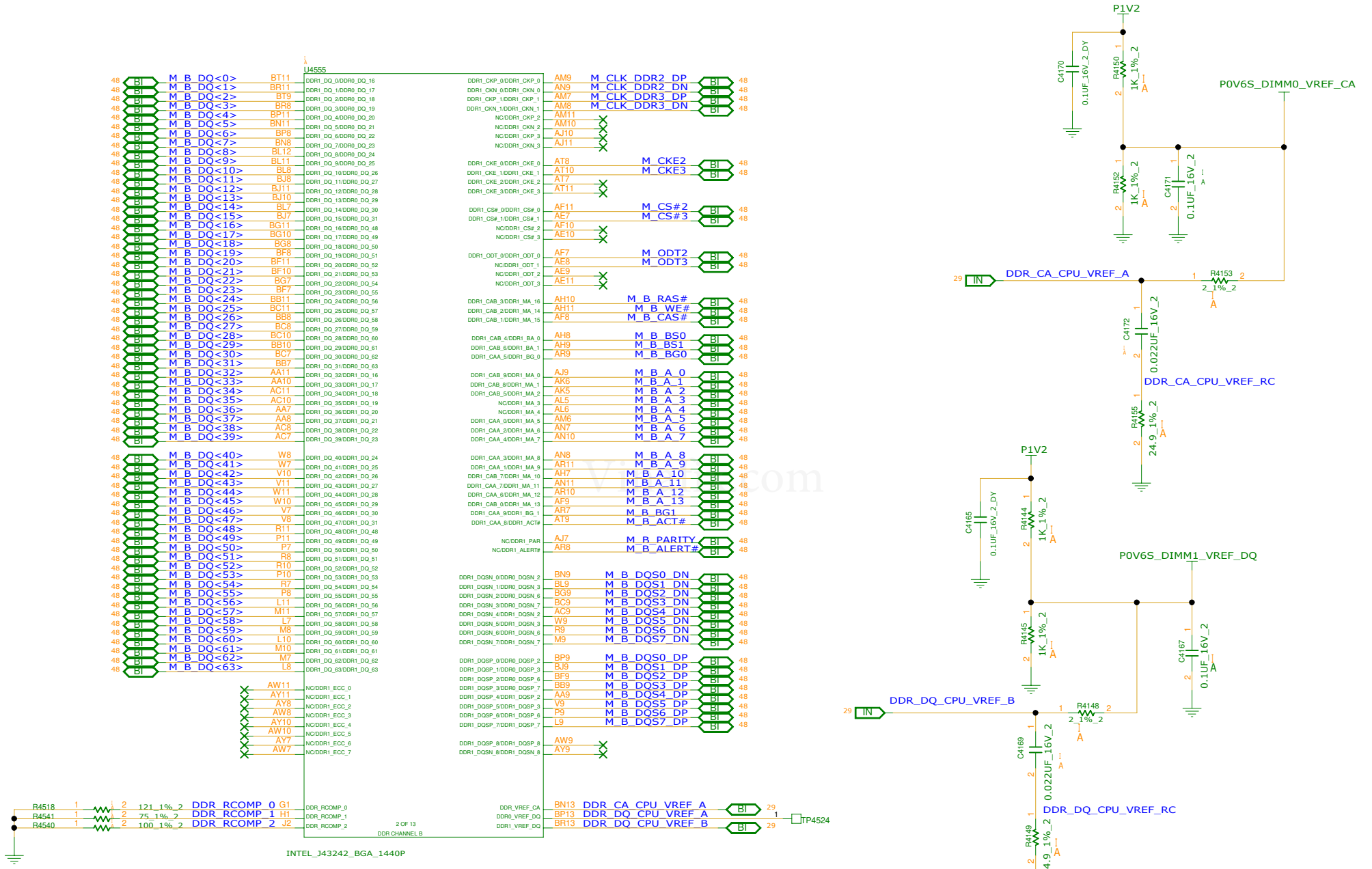
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE_H-DDR-1

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 28 of 139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M_CLK_DDR2_DN
M_CLK_DDR3_DP
M_CLK_DDR3_DN
M_CKE2
M_CKE3
M_CS#2
M_CS#3
M_ODT2
M_ODT3
M_B_RAS#
M_B_WE#
M_B_CAS#
M_B_BS0
M_B_BS1
M_B_BG0
M_B_A_0
M_B_A_1
M_B_A_2
M_B_A_3
M_B_A_4
M_B_A_5
M_B_A_6
M_B_A_7
M_B_A_8
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M_B_BG1
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M_B_PARITY
M_B_ALERT#
M_B_DQS0_DN
M_B_DQS1_DN
M_B_DQS2_DN
M_B_DQS3_DN
M_B_DQS4_DN
M_B_DQS5_DN
M_B_DQS6_DN
M_B_DQS7_DN
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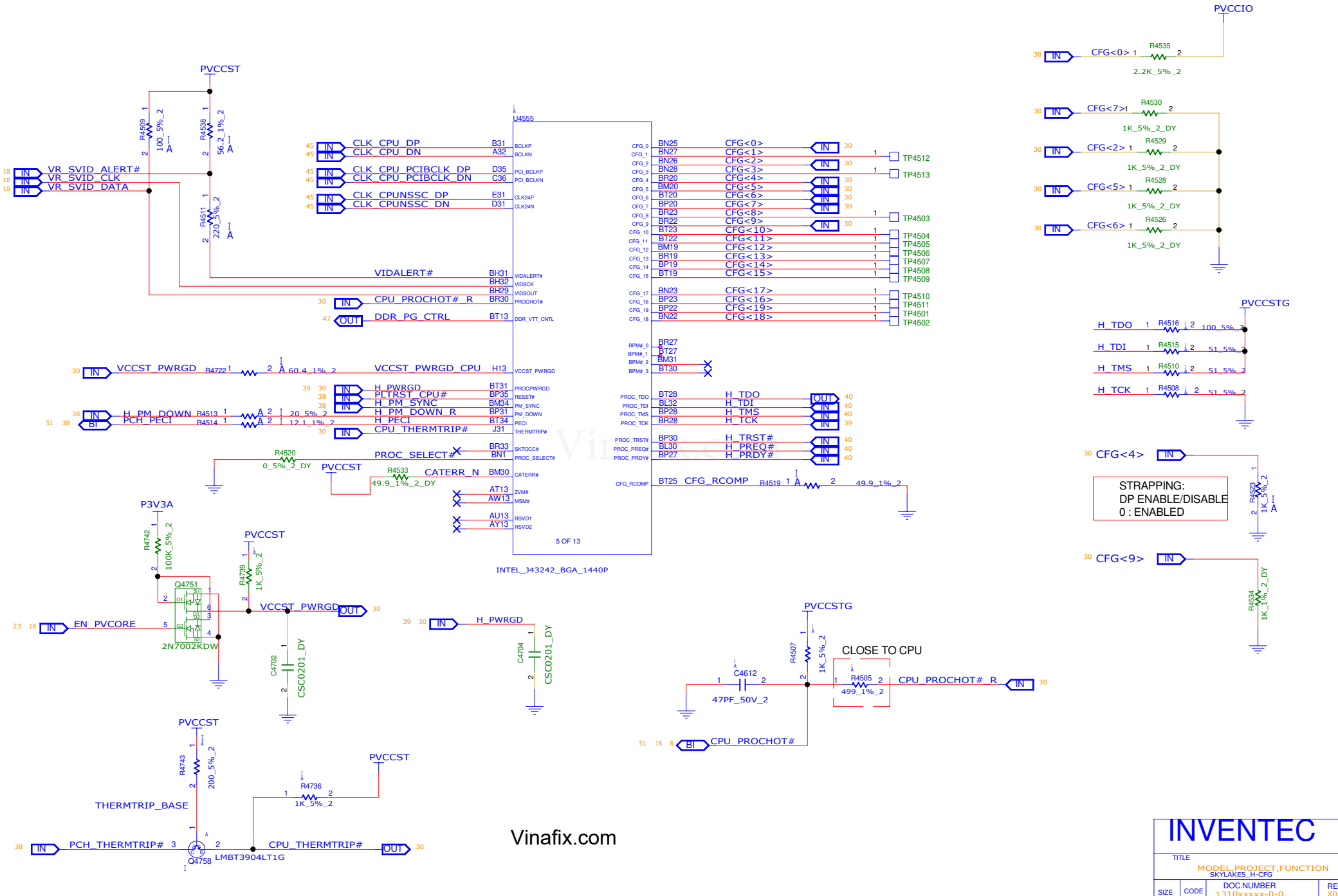
M_B_DQS1_DP
M_B_DQS2_DP
M_B_DQS3_DP
M_B_DQS4_DP
M_B_DQS5_DP
M_B_DQS6_DP
M_B_DQS7_DP
DDR_RCOMP_0
DDR_RCOMP_1
DDR_RCOMP_2
DDR_CA_CPU_VREF_A
DDR_DQ_CPU_VREF_A
DDR_DQ_CPU_VREF_B
TP4524
2 OF 13
DDR CHANNEL B
INTEL_J43242_BGA_1440P
P1V2
P0V6S_DIMM0_VREF_CA
DDR_CA_CPU_VREF_RC
P0V6S_DIMM1_VREF_DQ
DDR_DQ_CPU_VREF_RC
INVENTEC
MODEL,PROJECT,FUNCTION
SKYLAKE4_H-DDR-2
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SHEET 29 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX


PVCCST
PVCCIO
PVCCSTG
U4555
INTEL_J43242_BGA_1440P
5 OF 13
VR_SVID_ALERT#
VR_SVID_CLK
VR_SVID_DATA
CLK_CPU_DP
CLK_CPU_DN
CLK_CPU_PCIBCLK_DP
CLK_CPU_PCIBCLK_DN
CLK_CPUNSSC_DP
CLK_CPUNSSC_DN
VIDALERT#
CPU_PROCHOT#_R
DDR_PG_CTRL
VCCST_PWRGD
VCCST_PWRGD_CPU
H_PWRGD
PLTRST_CPU#
H_PM_SYNC
H_PM_DOWN_R
H_PECI
CPU_THERMTRIP#
PROC_SELECT#
CATERR_N
H_PM_DOWN
PCH_PECI
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H_TDI
H_TMS
H_TCK
H_TRST#
H_PREQ#
H_PRDY#
CFG_RCOMP
P3V3A
Q4751
2N7002KDW
EN_PVCORE
Q4758
LMBT3904LT1G
THERMTRIP_BASE
PCH_THERMTRIP#
CPU_THERMTRIP#
CPU_PROCHOT#
CLOSE TO CPU
STRAPPING:
DP ENABLE/DISABLE
0 : ENABLED
TP4512
TP4513
TP4503
TP4504
TP4505
TP4506
TP4507
TP4508
TP4509
TP4510
TP4511
TP4501
TP4502
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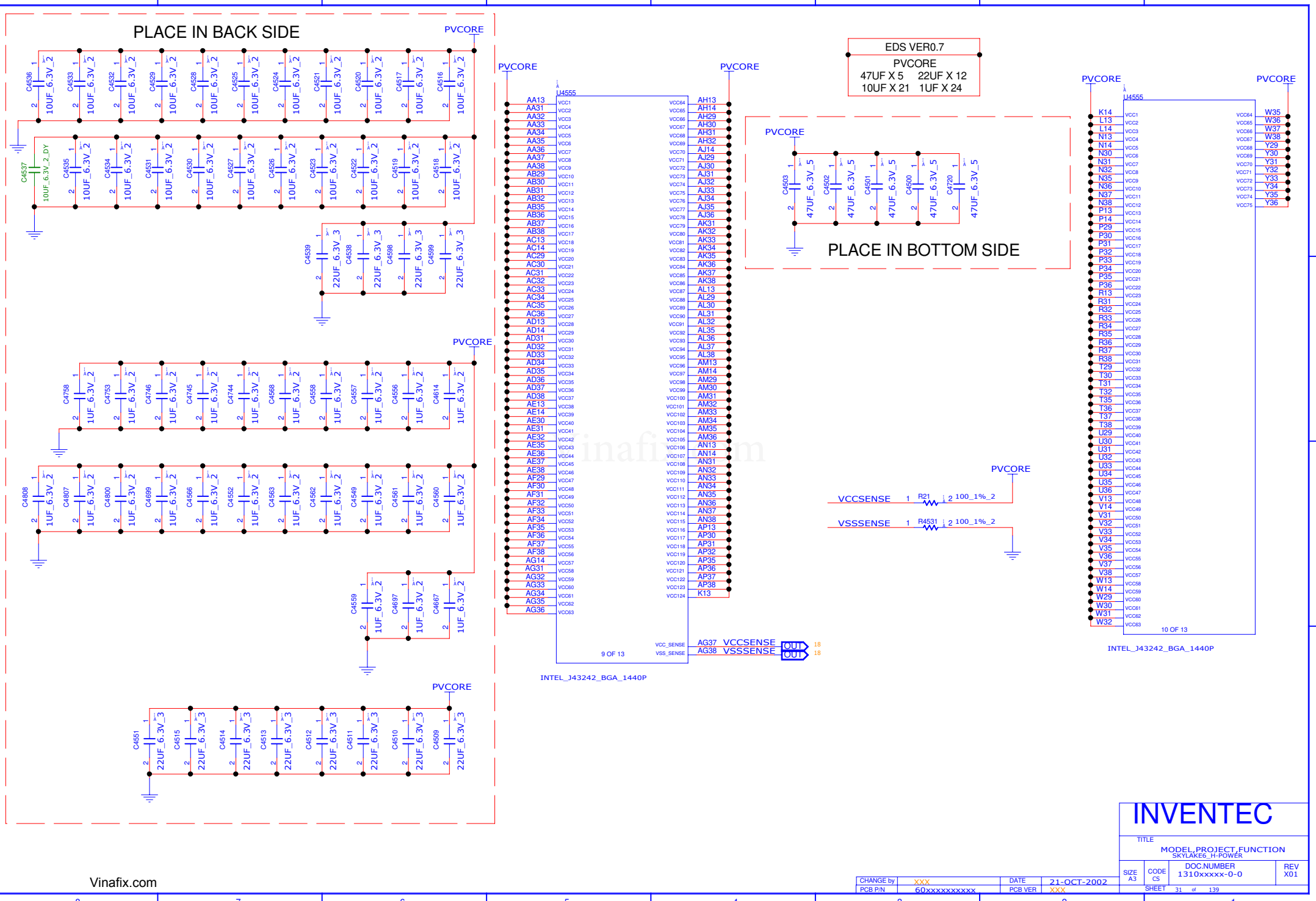
INVENTEC
MODEL,PROJECT,FUNCTION
SKYLAKE5_H-CFG
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
SHEET
30 of 139
CHANGE by
XXX
DATE
21-OCT-2002
PCB P/N
60xxxxxxxxxx
PCB VER
XXX



CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE6_H-POWER

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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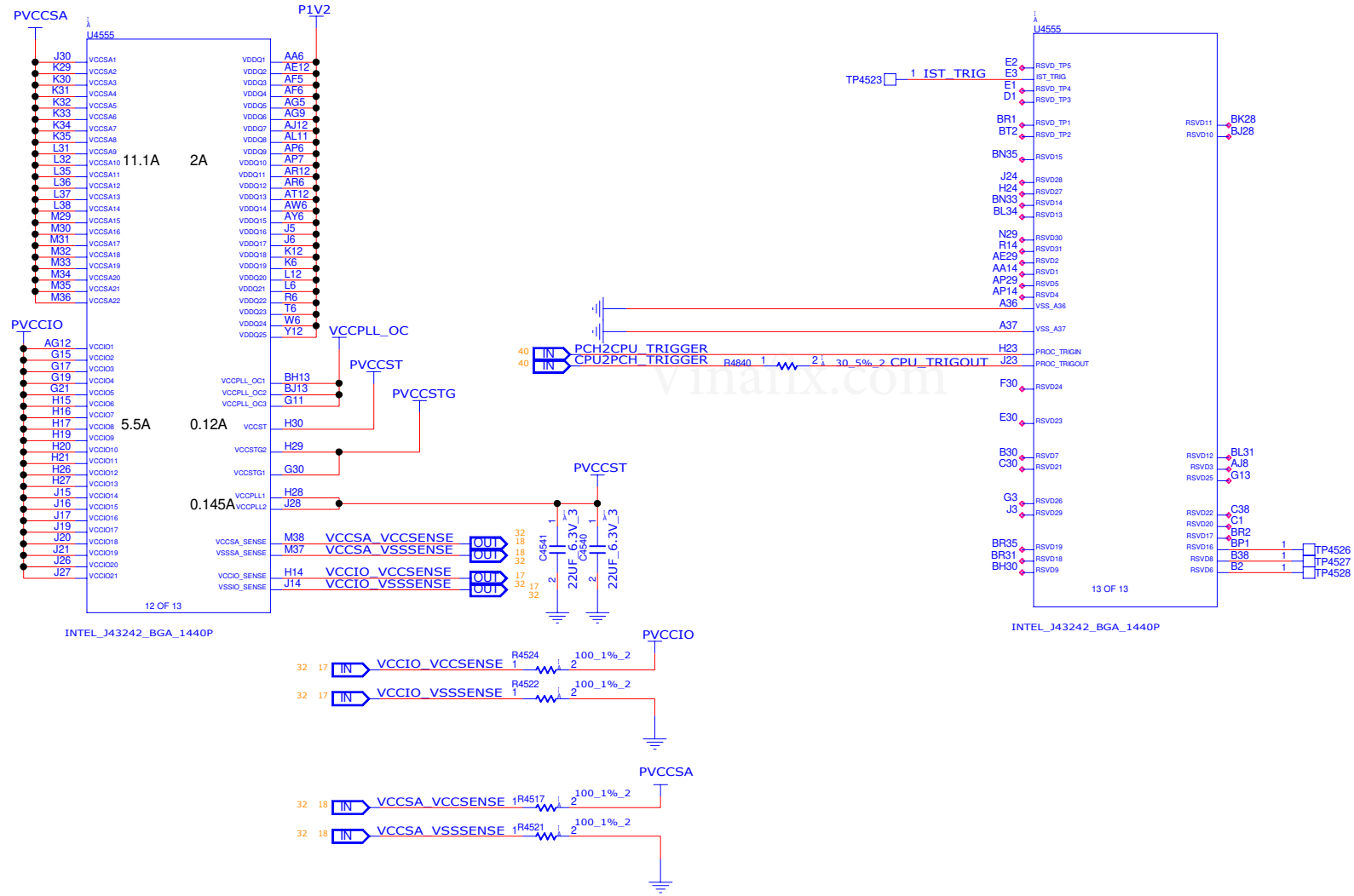

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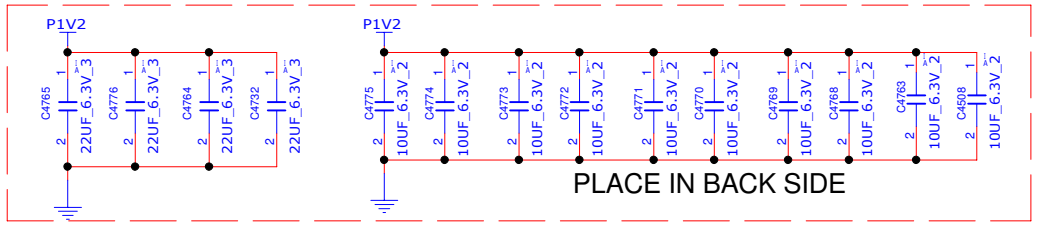
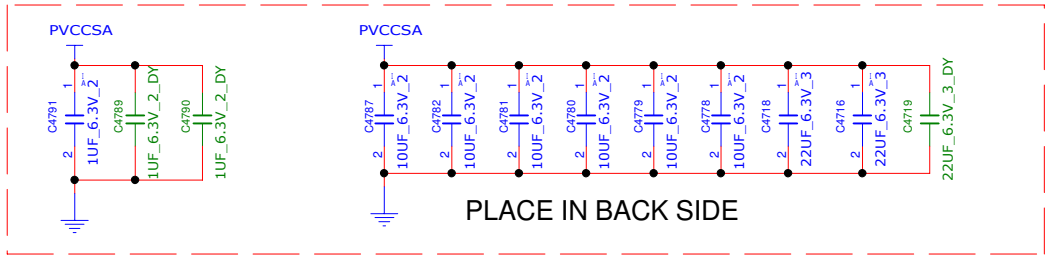
INVENTEC

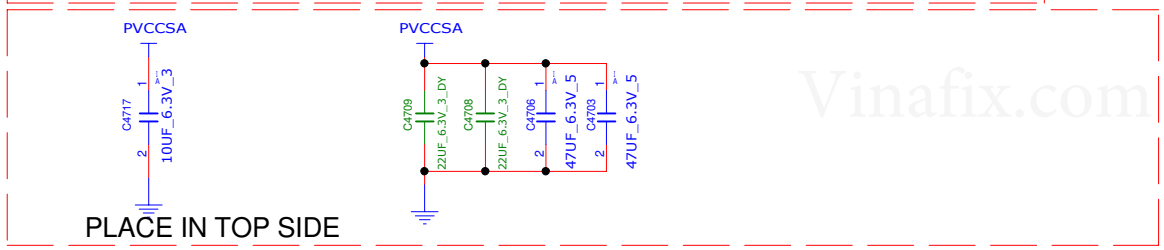
TITLE	MODEL,PROJECT,FUNCTION SKYLAKE7_H-POWER		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 32 of 139			

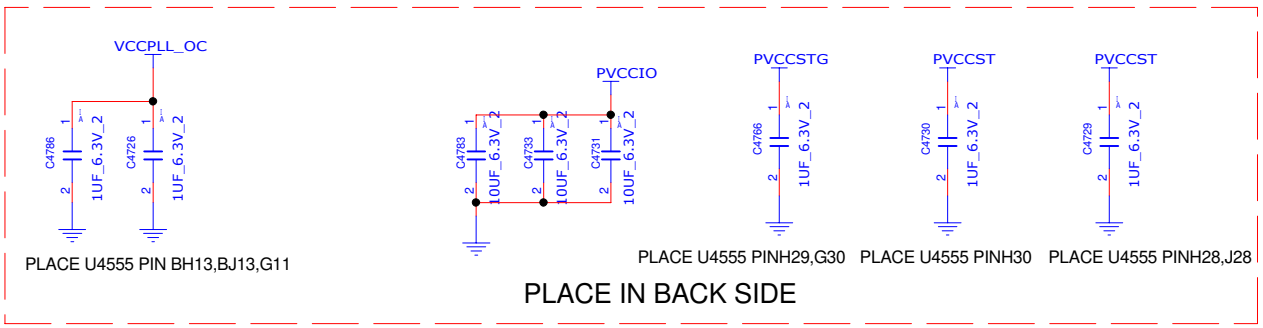
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX





EDS VER0.7
P1V2 10UF X 11 22UF X 4
PVCCSA 47UF X 2 22UF X 2 10UF X 7 1UF X 1





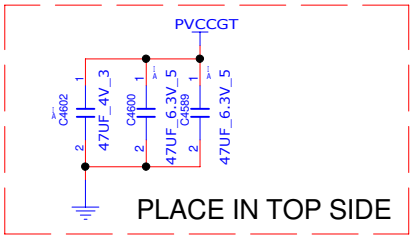
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION SKYLAKE8_H-DECOUPLING			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 33 of 139			

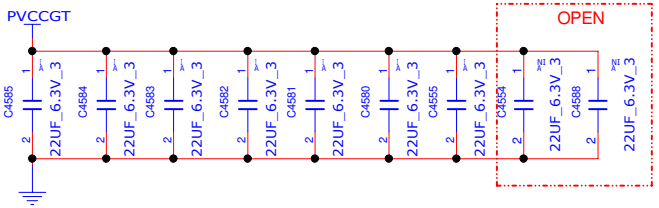
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

EDS VER0.7

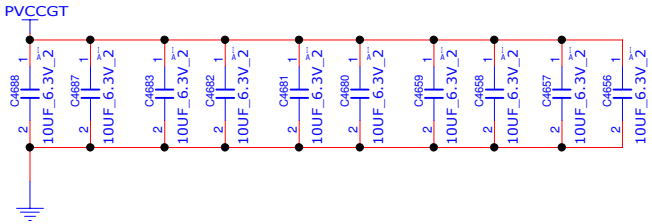
PVCCGT
47UF X 3 22UF X 7
10UF X 10 1UF X 12

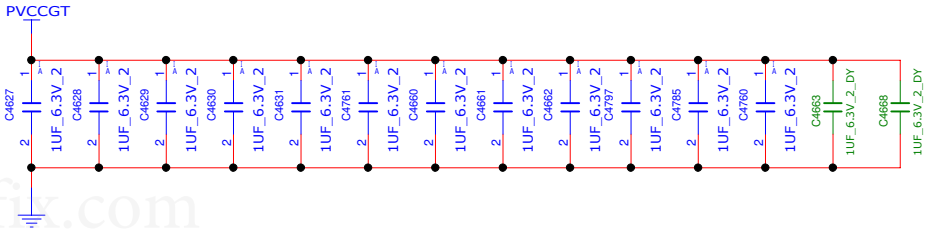


PLACE IN TOP SIDE

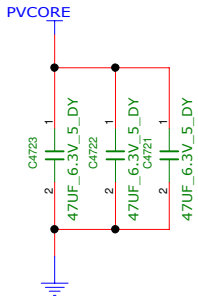


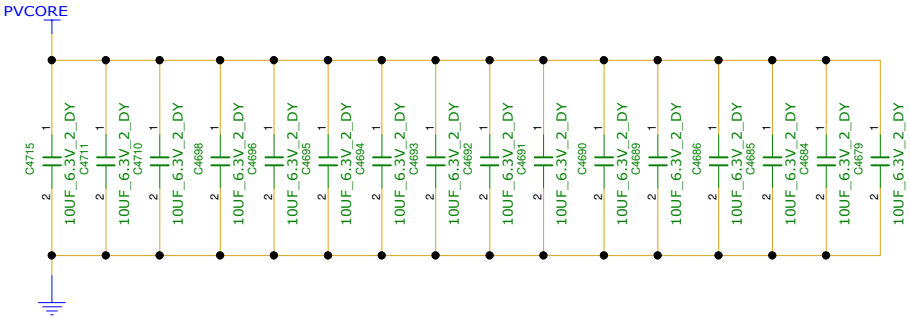
PLACE IN BACK SIDE

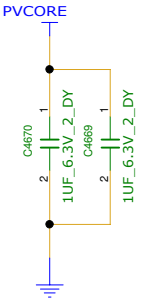




H82 CPU







INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE9_H-GT DECOUPLING

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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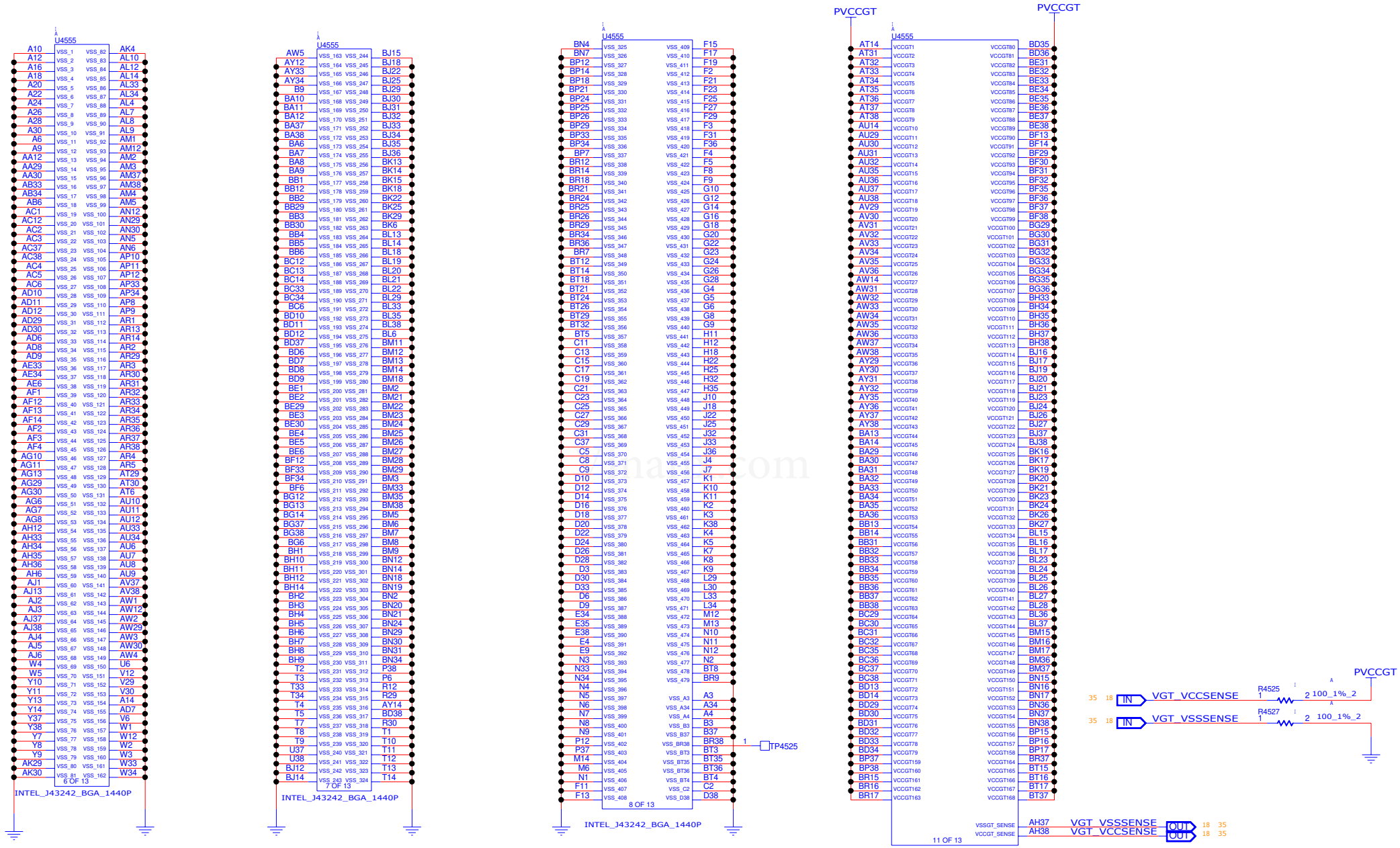
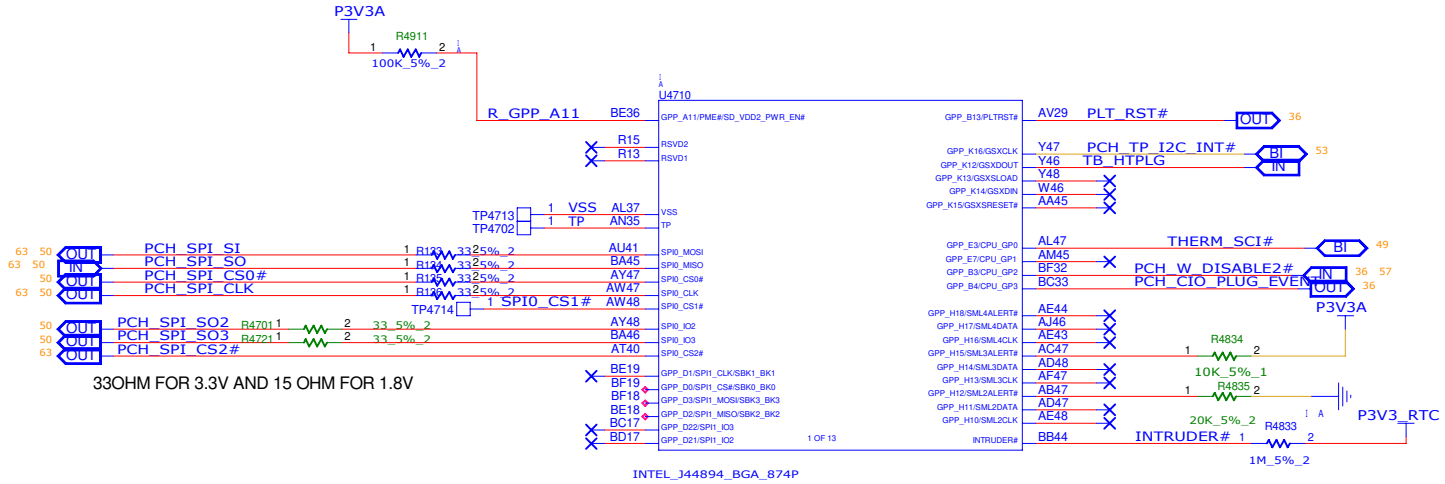
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

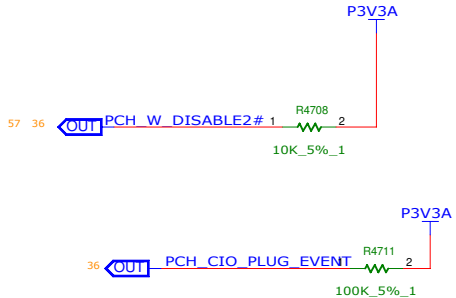


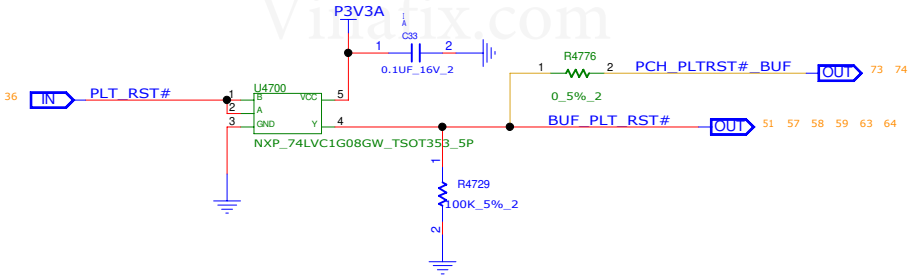
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SKYLAKE10_H-GND
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	35 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX







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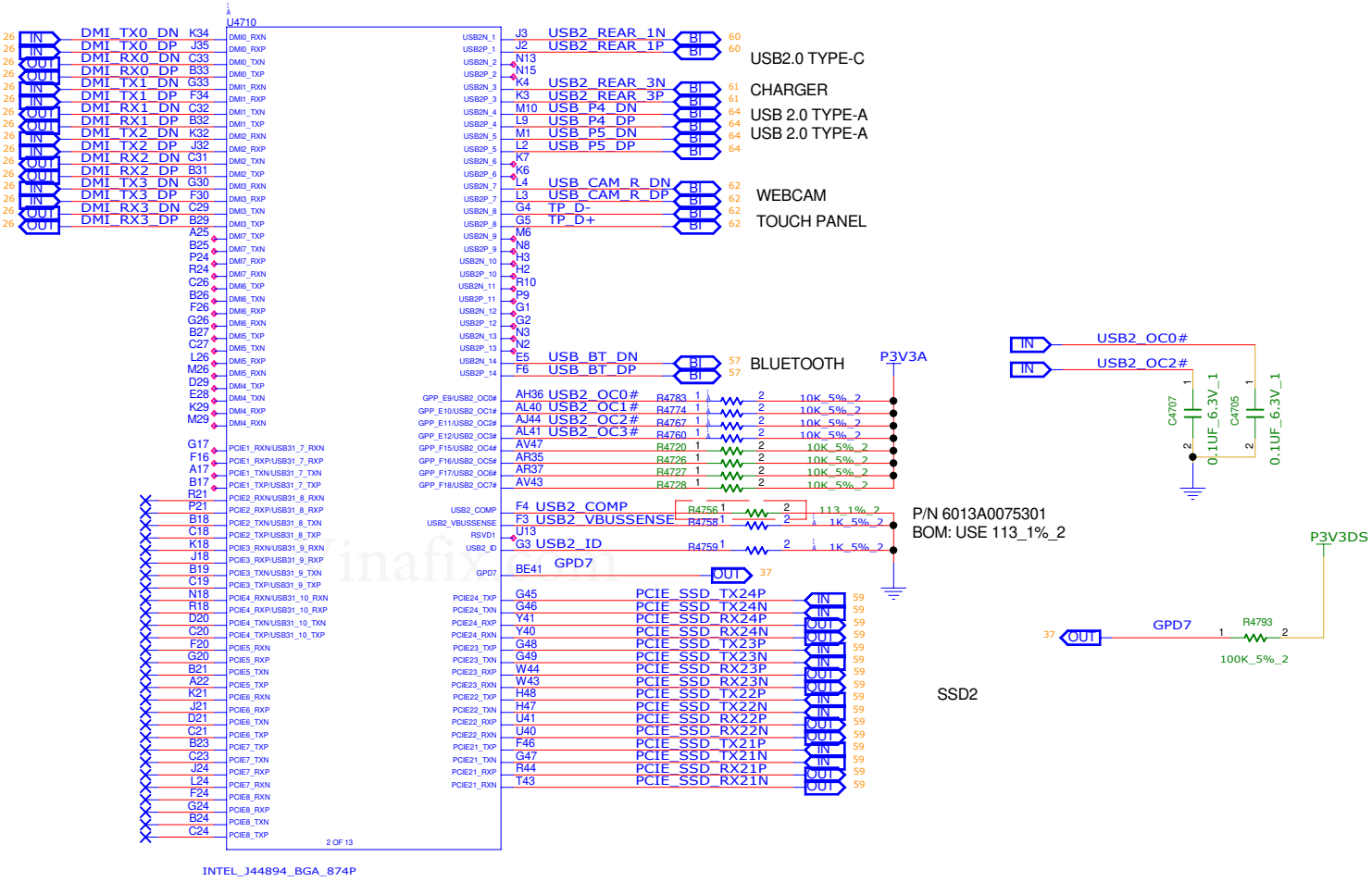
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-SPI,GPP

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 36 of 139



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-DMI,USB2,USB3

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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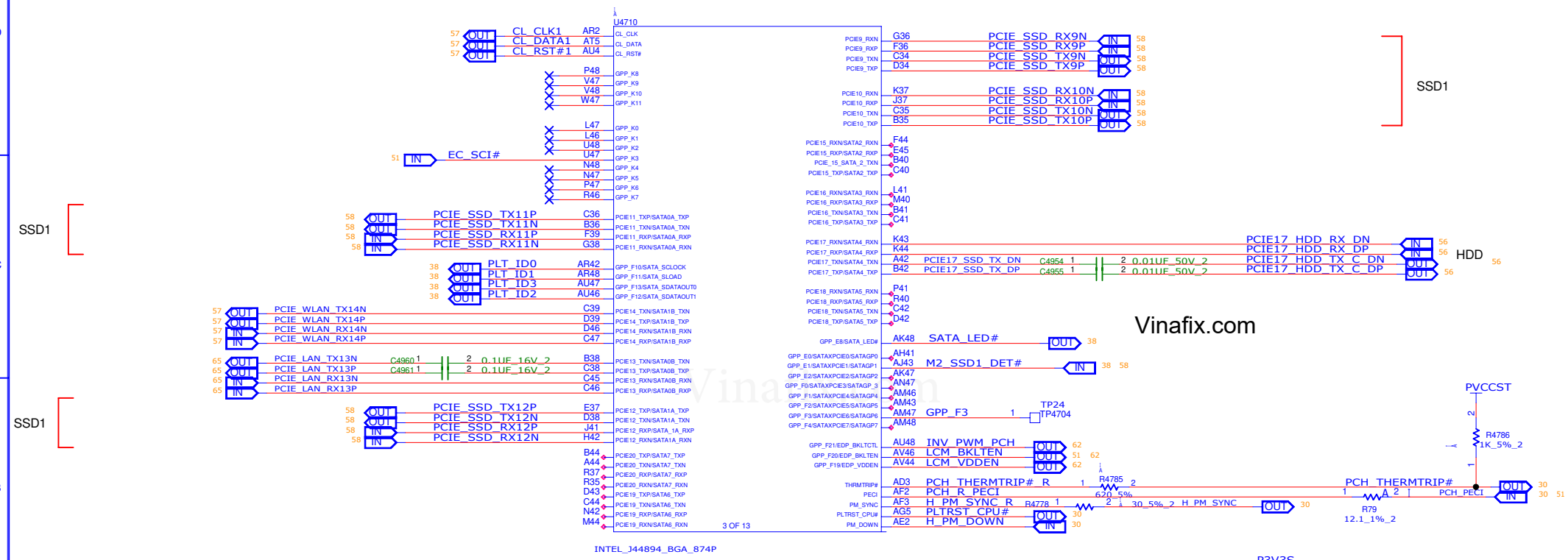

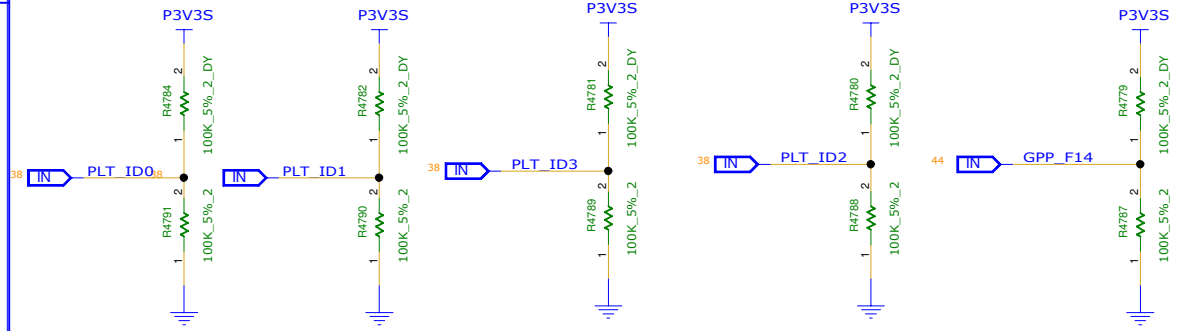

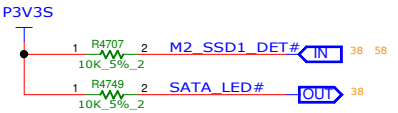

	PLT_ID0	PLT_ID1	GPU
GPU	0	0	N18E-G2
	0	1	N18E-G1
	1	0	N18E-G0

	PLT_ID2	PLT_ID3	Size
VRAM	0	0	8G
	0	1	6G

	GPP_F14	Panel
GPU	0	15"
	1	17"

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-CLINK,FAN,PCIE/SATA,HOST

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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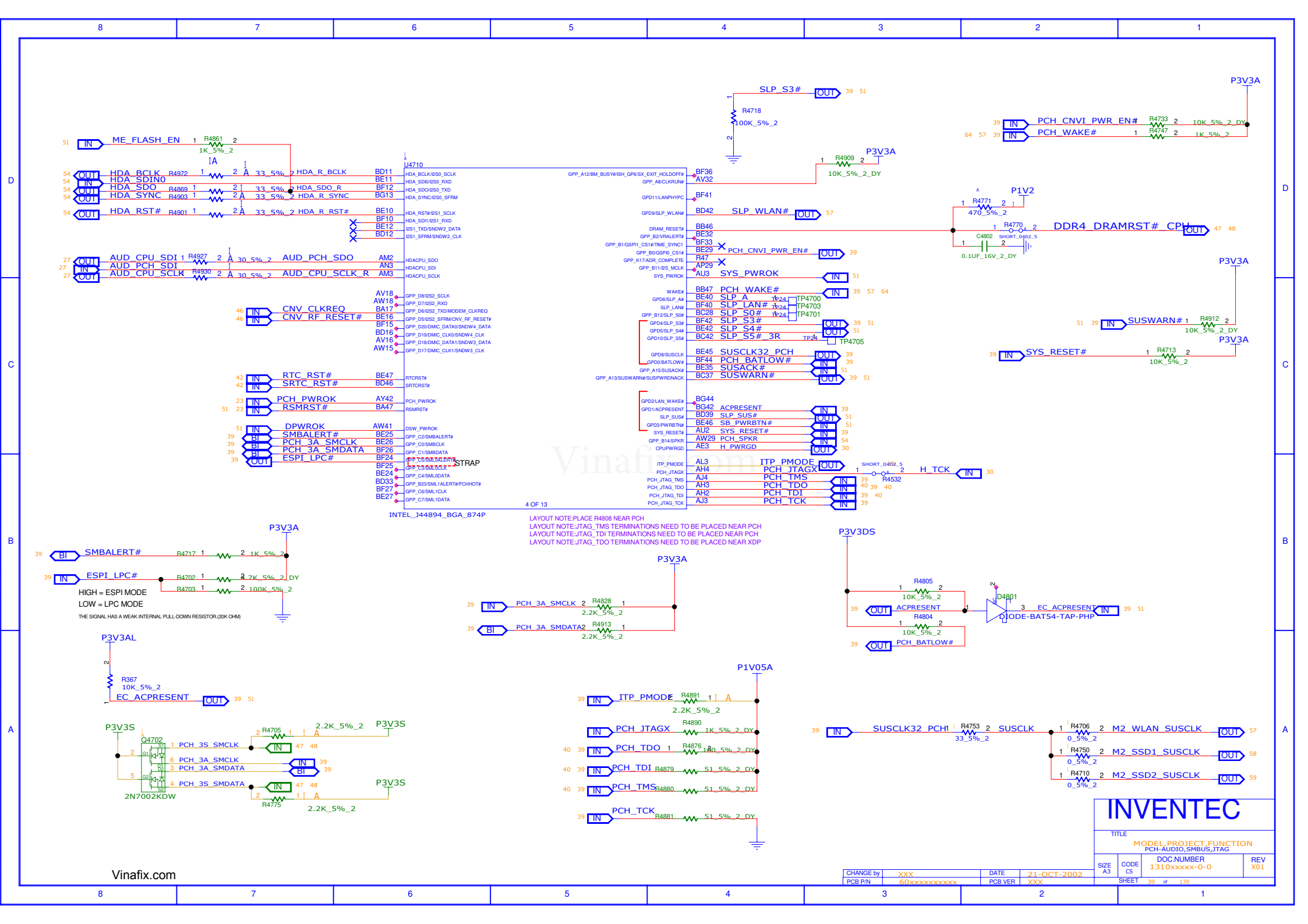
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX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HDA_SDIN0
HDA_SDO
HDA_SYNC
HDA_RST#
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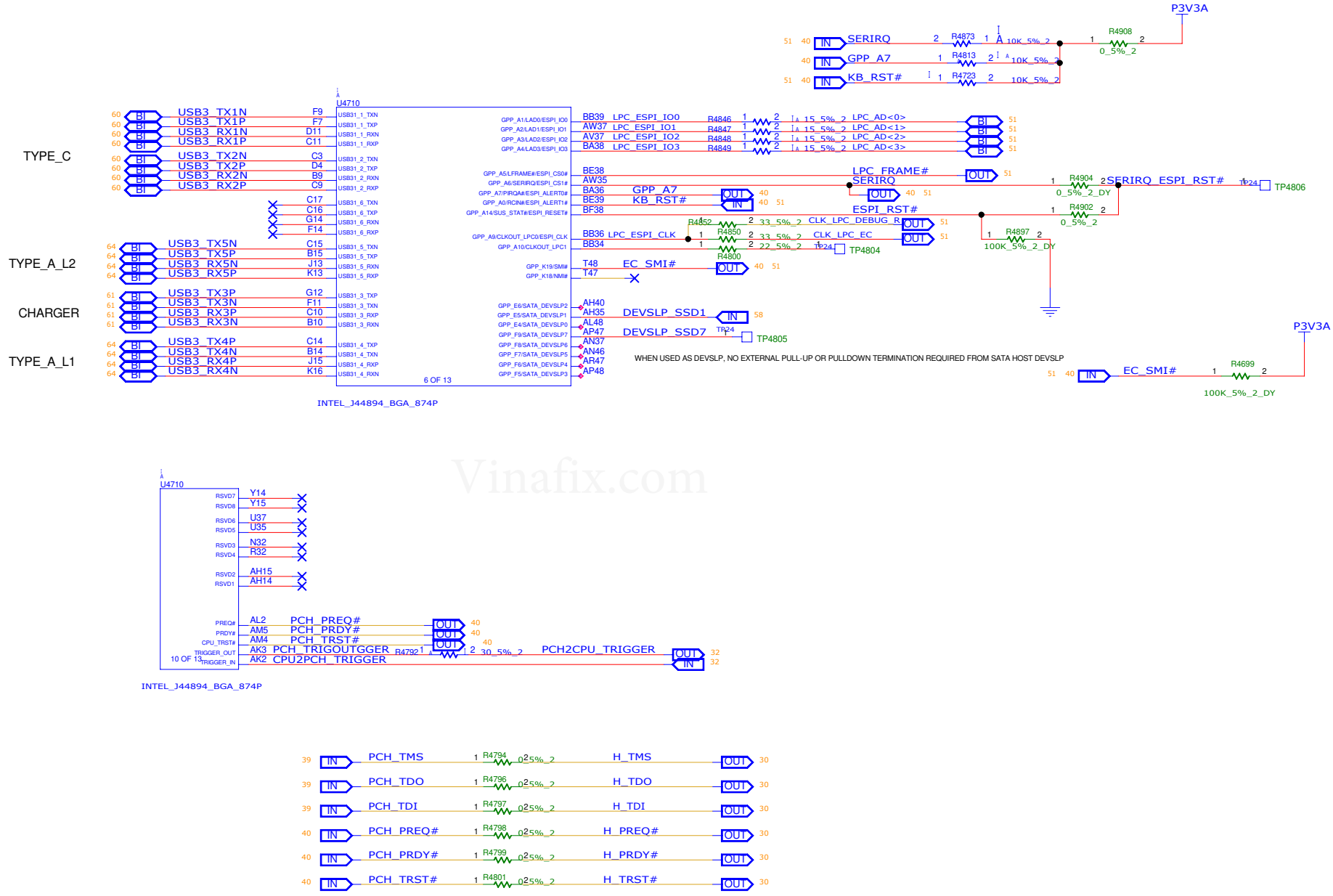
AUD_PCH_SDI
AUD_CPU_SCLK
AUD_PCH_SDO
AUD_CPU_SCLK_R
CNV_CLKREQ
CNV_RF_RESET#
RTC_RST#
SRTC_RST#
PCH_PWROK
RSMRST#
DPWROK
SMBALERT#
PCH_3A_SMCLK
PCH_3A_SMDATA
ESPI_LPC#
STRAP
U4710
INTEL_J44894_BGA_874P
4 OF 13
SLP_S3#
SLP_WLAN#
PCH_CNVI_PWR_EN#
SYS_PWROK
PCH_WAKE#
SLP_A
SLP_LAN#
SLP_S0#
SLP_S3#
SLP_S4#
SLP_S5#_3R
SUSCLK32_PCH
PCH_BATLOW#
SUSWARN#
ACPRESENT
SLP_SUS#
SB_PWRBTN#
SYS_RESET#
PCH_SPKR
H_PWRGD
ITP_PMODE
PCH_JTAGX
PCH_TMS
PCH_TDO
PCH_TDI
PCH_TCK
H_TCK
DDR4_DRAMRST#_CPU
SYS_RESET#
P3V3A
P1V2
P3V3DS
P3V3AL
P3V3S
P1V05A
HIGH = ESPI MODE
LOW = LPC MODE
THE SIGNAL HAS A WEAK INTERNAL PULL-DOWN RESISTOR.(20K OHM)
LAYOUT NOTE:PLACE R4808 NEAR PCH
LAYOUT NOTE:JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE:JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE:JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
2N7002KDW
D4801
DIODE-BAT54-TAP-PHP
M2_WLAN_SUSCLK
M2_SSD1_SUSCLK
M2_SSD2_SUSCLK
INVENTEC
MODEL,PROJECT,FUNCTION
PCH-AUDIO,SMBUS,JTAG
DOC.NUMBER
1310xxxxx-0-0
REV
X01
CHANGE by
XXX
DATE
21-OCT-2002
PCB P/N
60xxxxxxxxxx
PCB VER
XXX
SHEET
39 of 139
Vinafix.com



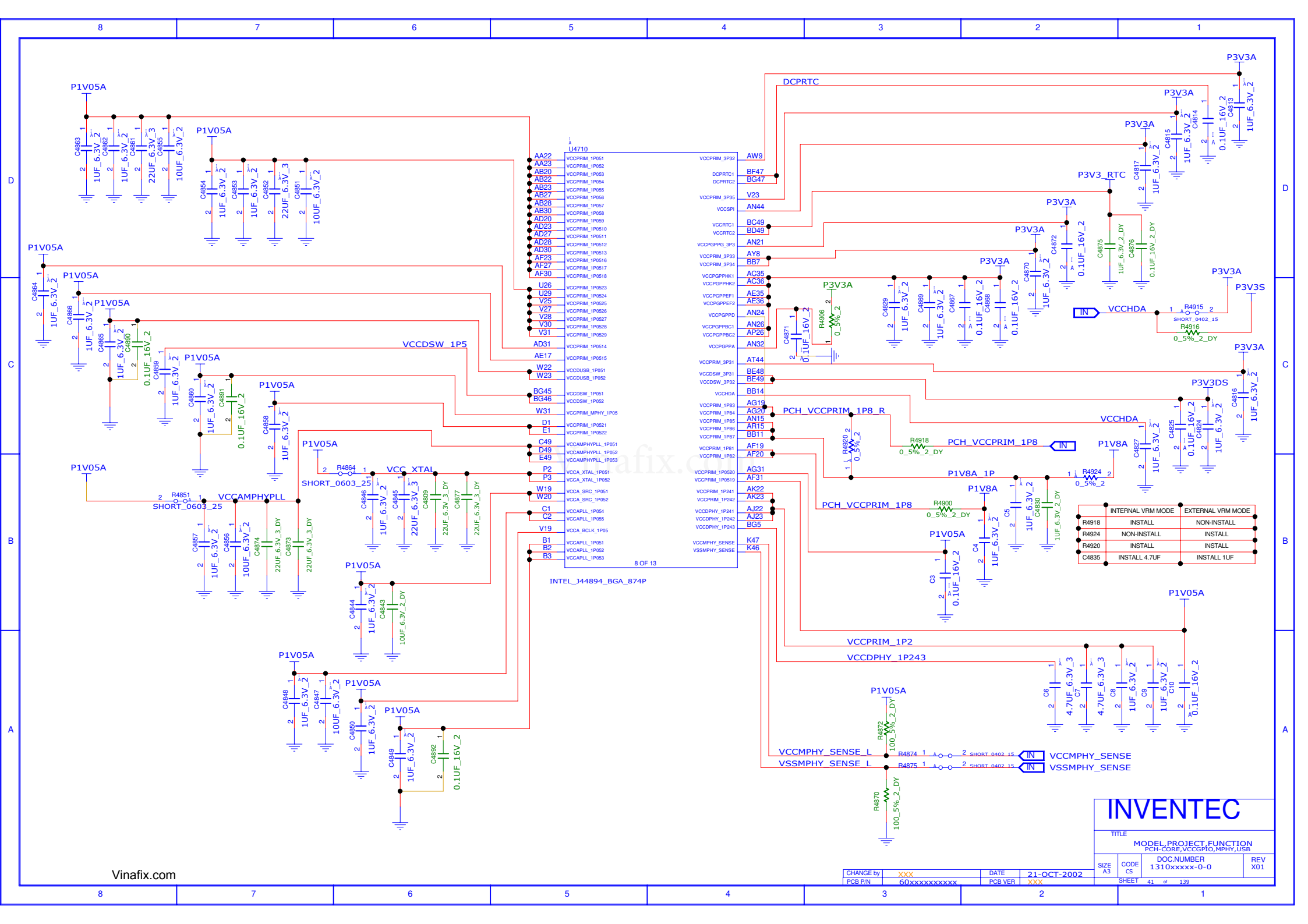
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

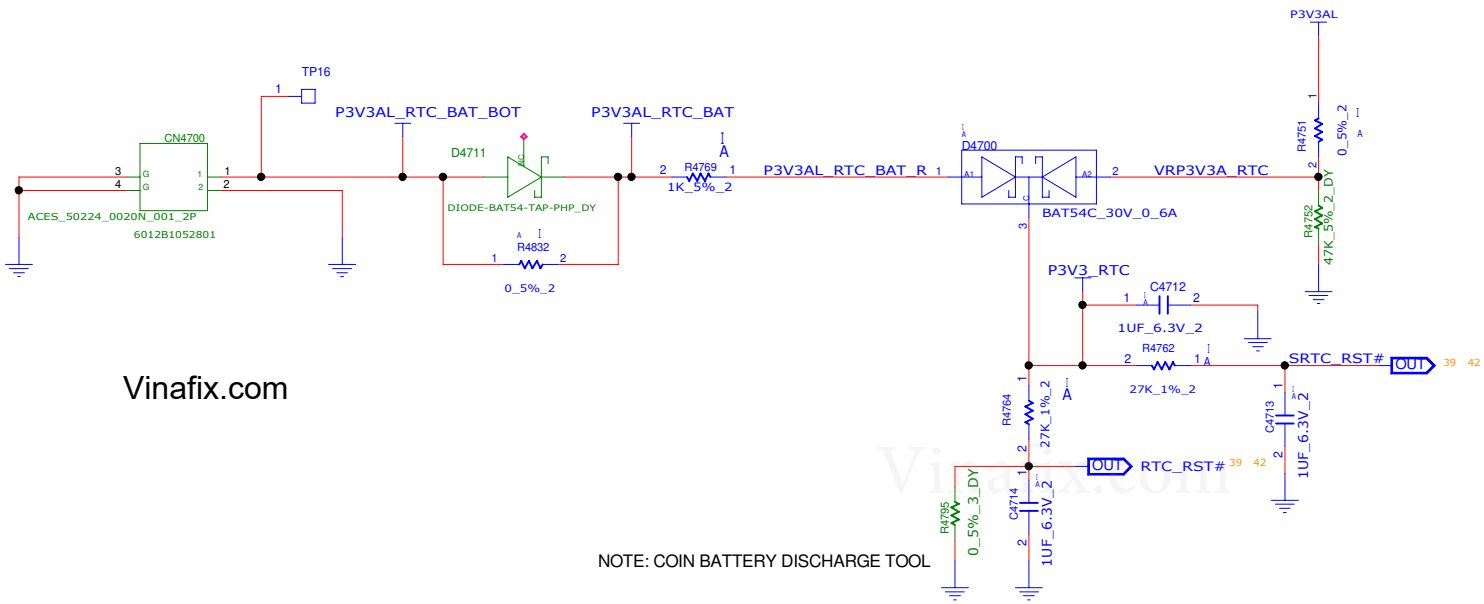
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-LPC/ESPI,USB,SATA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 40 of 139

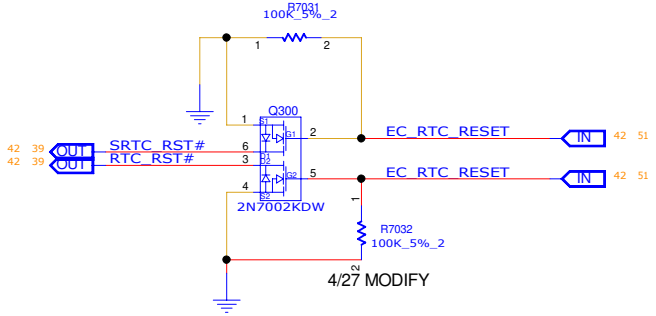

U4710
INTEL_J44894_BGA_874P
8 OF 13
P1V05A
P3V3A
P3V3_RTC
P3V3S
P3V3DS
P1V8A
P1V8A_1P
DCPRTC
VCCDSW_1P5
VCC_XTAL
VCCAMPHYPLL
PCH_VCCPRIM_1P8_R
PCH_VCCPRIM_1P8
VCCHDA
VCCPRIM_1P2
VCCDPHY_1P243
VCCMPHY_SENSE_L
VSSMPHY_SENSE_L
VCCMPHY_SENSE
VSSMPHY_SENSE
SHORT_0603_25
INTERNAL VRM MODE
EXTERNAL VRM MODE
R4918 INSTALL NON-INSTALL
R4924 NON-INSTALL INSTALL
R4920 INSTALL INSTALL
C4835 INSTALL 4.7UF INSTALL 1UF
INVENTEC
MODEL,PROJECT,FUNCTION
PCH-CORE,VCCGPIO,MPHY,USB
DOC.NUMBER 1310xxxxx-0-0
REV X01
SIZE A3
CODE CS
SHEET 41 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX
Vinafix.com



Vinafix.com

NOTE: COIN BATTERY DISCHARGE TOOL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R4710	INSTAL	UNINSTAL
R4709	UNINSTAL	INSTAL



Vinafix.com

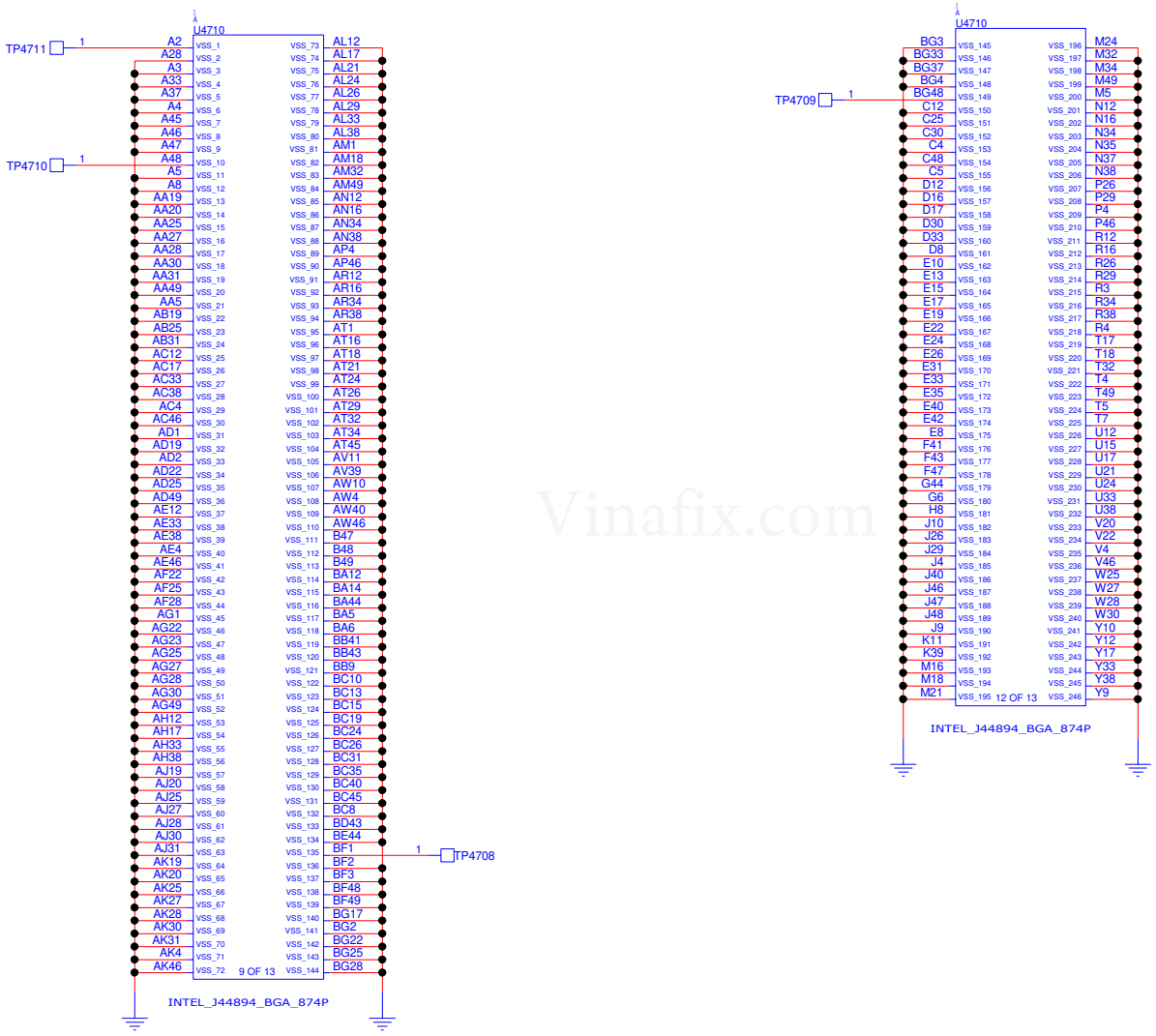
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 42 of 139



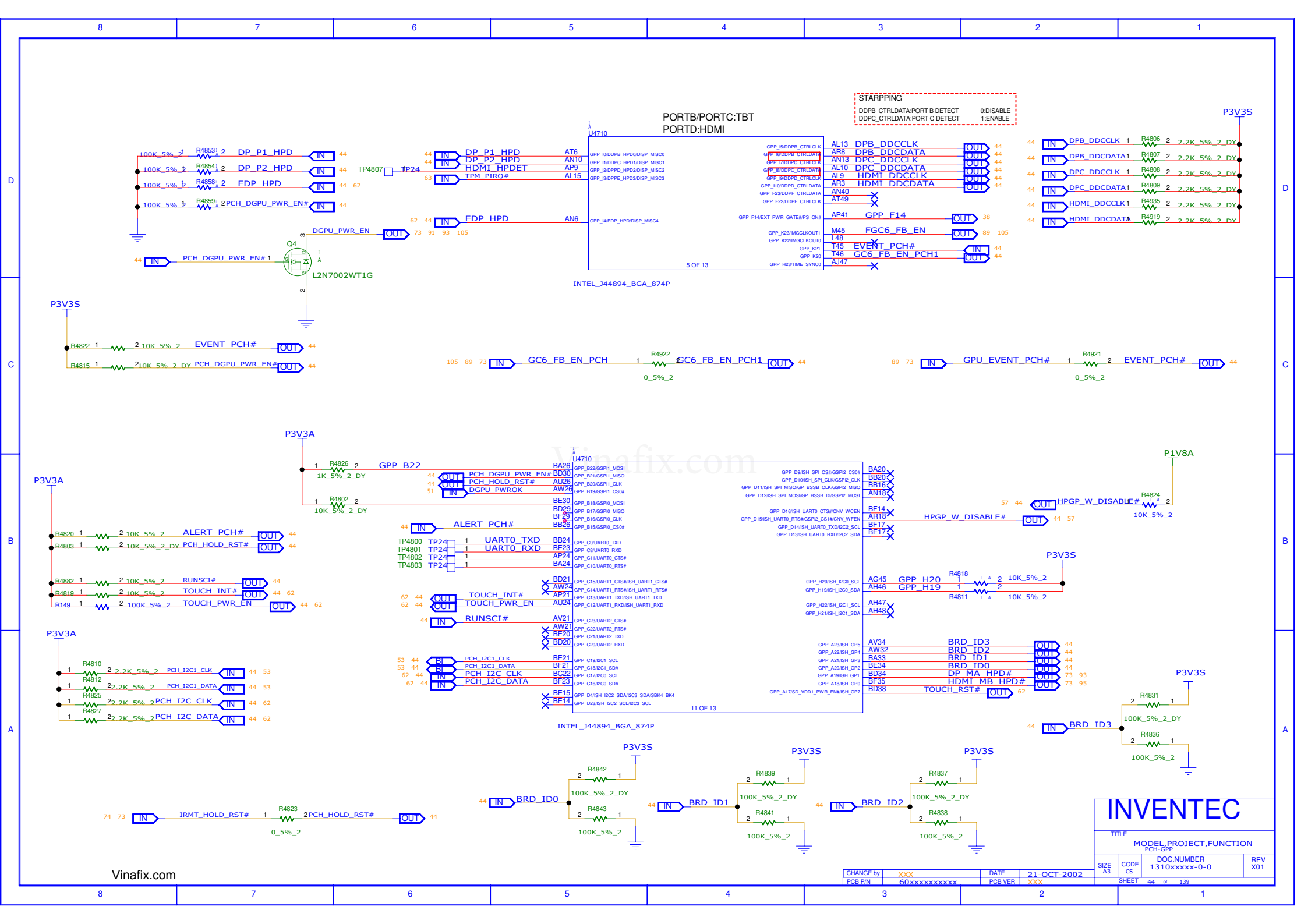
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-GND

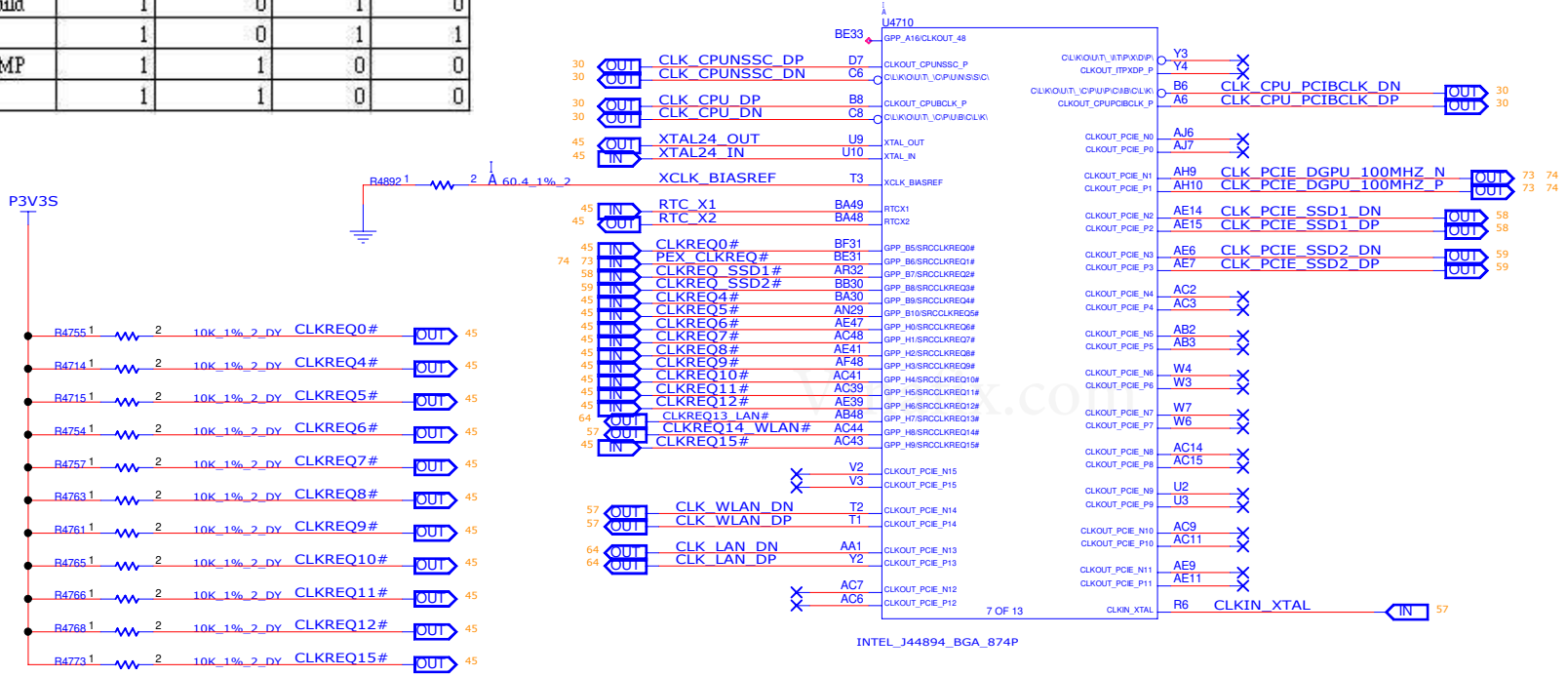
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

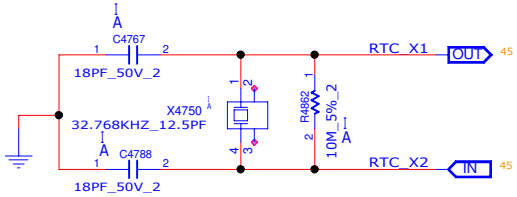
SHEET 43 of 139

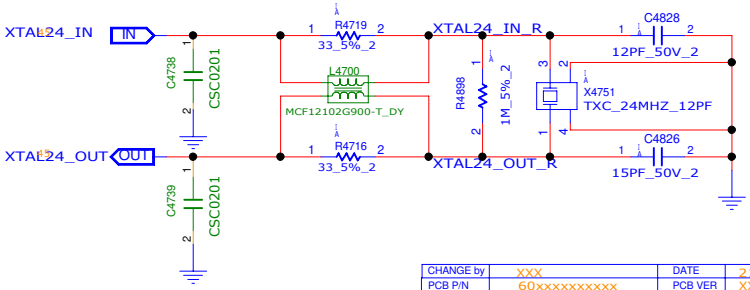

STARPPING
DDPB_CTRLDATA:PORT B DETECT 0:DISABLE
DDPC_CTRLDATA:PORT C DETECT 1:ENABLE
PORTB/PORTC:TBT
PORTD:HDMI
U4710
INTEL_J44894_BGA_874P
5 OF 13
11 OF 13
Q4
L2N7002WT1G
P3V3S
P3V3A
P1V8A
DP_P1_HPD
DP_P2_HPD
EDP_HPD
PCH_DGPU_PWR_EN#
DGPU_PWR_EN
TP4807
TP24
TPM_PIRQ#
HDMI_HPDET
DPB_DDCCLK
DPB_DDCDATA
DPC_DDCCLK
DPC_DDCDATA
HDMI_DDCCLK
HDMI_DDCDATA
GPP_F14
FGC6_FB_EN
EVENT_PCH#
GC6_FB_EN_PCH
GC6_FB_EN_PCH1
GPU_EVENT_PCH#
GPP_B22
PCH_DGPU_PWR_EN#
PCH_HOLD_RST#
DGPU_PWROK
ALERT_PCH#
UART0_TXD
UART0_RXD
TOUCH_INT#
TOUCH_PWR_EN
RUNSCI#
PCH_I2C1_CLK
PCH_I2C1_DATA
PCH_I2C_CLK
PCH_I2C_DATA
HPGP_W_DISABLE#
GPP_H20
GPP_H19
BRD_ID3
BRD_ID2
BRD_ID1
BRD_ID0
DP_MA_HPD#
HDMI_MB_HPD#
TOUCH_RST#
IRMT_HOLD_RST#
PCH_HOLD_RST#
RUNSCI#
ALERT_PCH#
TOUCH_INT#
TOUCH_PWR_EN
EVENT_PCH#
PCH_DGPU_PWR_EN#
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
PCH-GPP
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 44 of 139
CHANGE by XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx
PCB VER XXX
Vinafix.com

	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	0	1
D build	1	0	1	0
	1	0	1	1
Pre-MP	1	1	0	0
MP	1	1	0	0

1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs



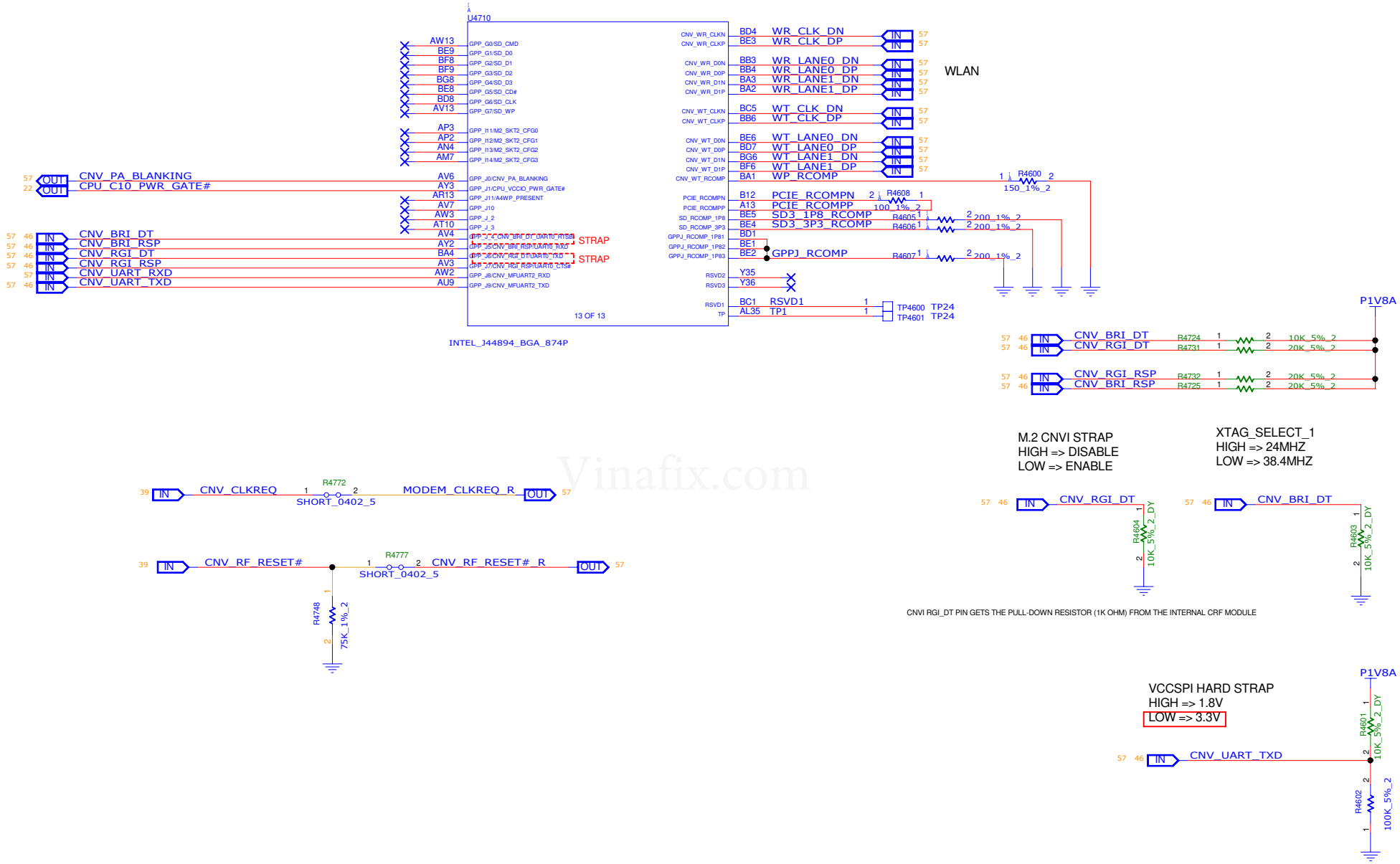


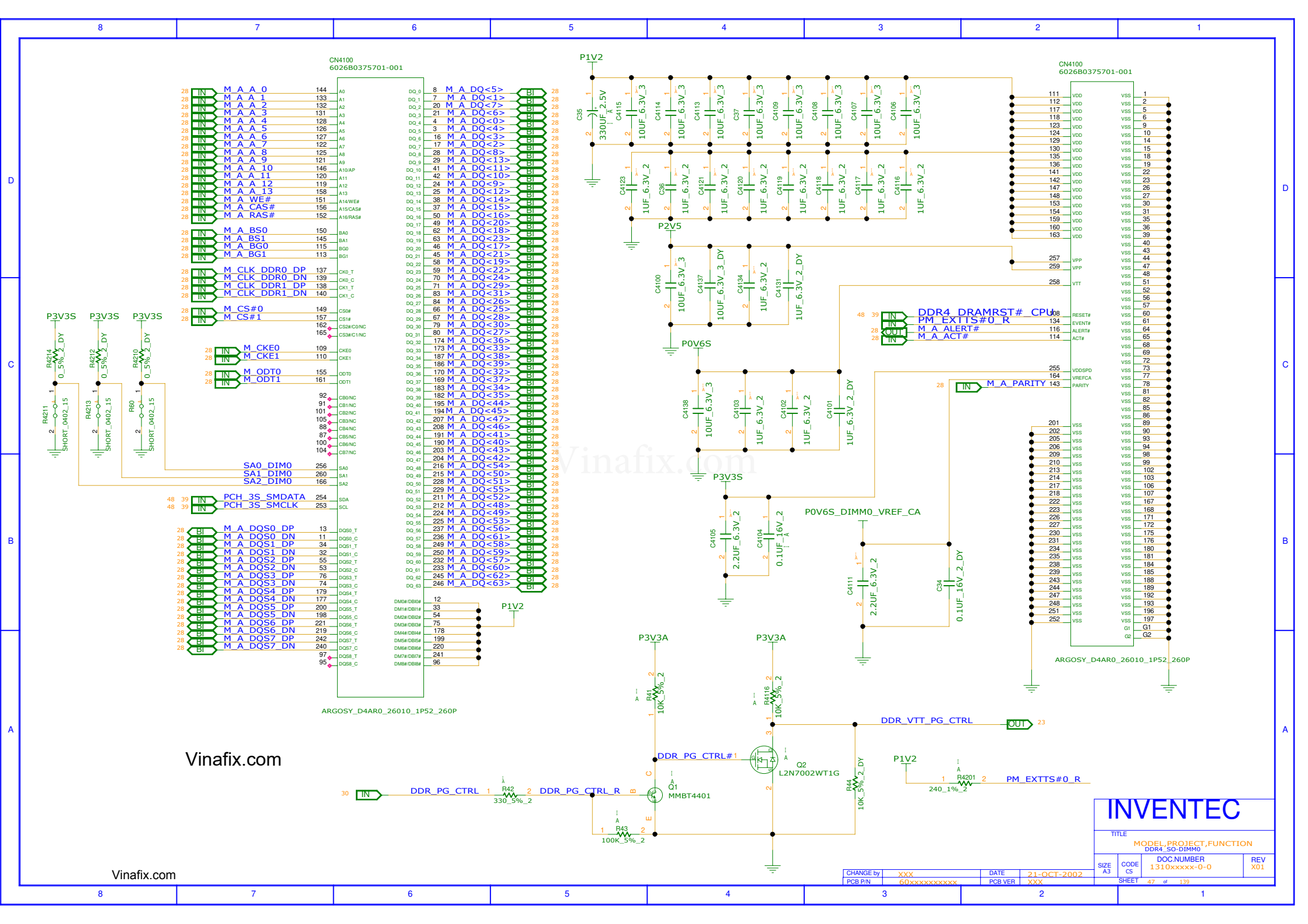


INVENTEC

TITLE: MODEL,PROJECT,FUNCTION PCH-GPP,CLKOUT			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 45 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX


U4710
INTEL_J44894_BGA_874P
13 OF 13
WLAN
CNV_PA_BLANKING
CPU_C10_PWR_GATE#
CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
CNV_UART_RXD
CNV_UART_TXD
STRAP
STRAP
WR_CLK_DN
WR_CLK_DP
WR_LANE0_DN
WR_LANE0_DP
WR_LANE1_DN
WR_LANE1_DP
WT_CLK_DN
WT_CLK_DP
WT_LANE0_DN
WT_LANE0_DP
WT_LANE1_DN
WT_LANE1_DP
WP_RCOMP
PCIE_RCOMPN
PCIE_RCOMPP
SD3_1P8_RCOMP
SD3_3P3_RCOMP
GPPJ_RCOMP
RSVD1
TP1
TP24
P1V8A
M.2 CNVI STRAP
HIGH => DISABLE
LOW => ENABLE
XTAG_SELECT_1
HIGH => 24MHZ
LOW => 38.4MHZ
CNV_CLKREQ
MODEM_CLKREQ_R
SHORT_0402_5
CNV_RF_RESET#
CNV_RF_RESET#_R
CNVI RGI_DT PIN GETS THE PULL-DOWN RESISTOR (1K OHM) FROM THE INTERNAL CRF MODULE
VCCSPI HARD STRAP
HIGH => 1.8V
LOW => 3.3V
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SHEET 46 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX


CN4100
6026B0375701-001
M_A_A_0
M_A_A_1
M_A_A_2
M_A_A_3
M_A_A_4
M_A_A_5
M_A_A_6
M_A_A_7
M_A_A_8
M_A_A_9
M_A_A_10
M_A_A_11
M_A_A_12
M_A_A_13
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_BS0
M_A_BS1
M_A_BG0
M_A_BG1
M_CLK_DDR0_DP
M_CLK_DDR0_DN
M_CLK_DDR1_DP
M_CLK_DDR1_DN
M_CS#0
M_CS#1
M_CKE0
M_CKE1
M_ODT0
M_ODT1
SA0_DIM0
SA1_DIM0
SA2_DIM0
PCH_3S_SMDATA
PCH_3S_SMCLK
M_A_DQS0_DP
M_A_DQS0_DN
M_A_DQS1_DP
M_A_DQS1_DN
M_A_DQS2_DP
M_A_DQS2_DN
M_A_DQS3_DP
M_A_DQS3_DN
M_A_DQS4_DP
M_A_DQS4_DN
M_A_DQS5_DP
M_A_DQS5_DN
M_A_DQS6_DP
M_A_DQS6_DN
M_A_DQS7_DP
M_A_DQS7_DN
M_A_DQ<0>
M_A_DQ<1>
M_A_DQ<2>
M_A_DQ<3>
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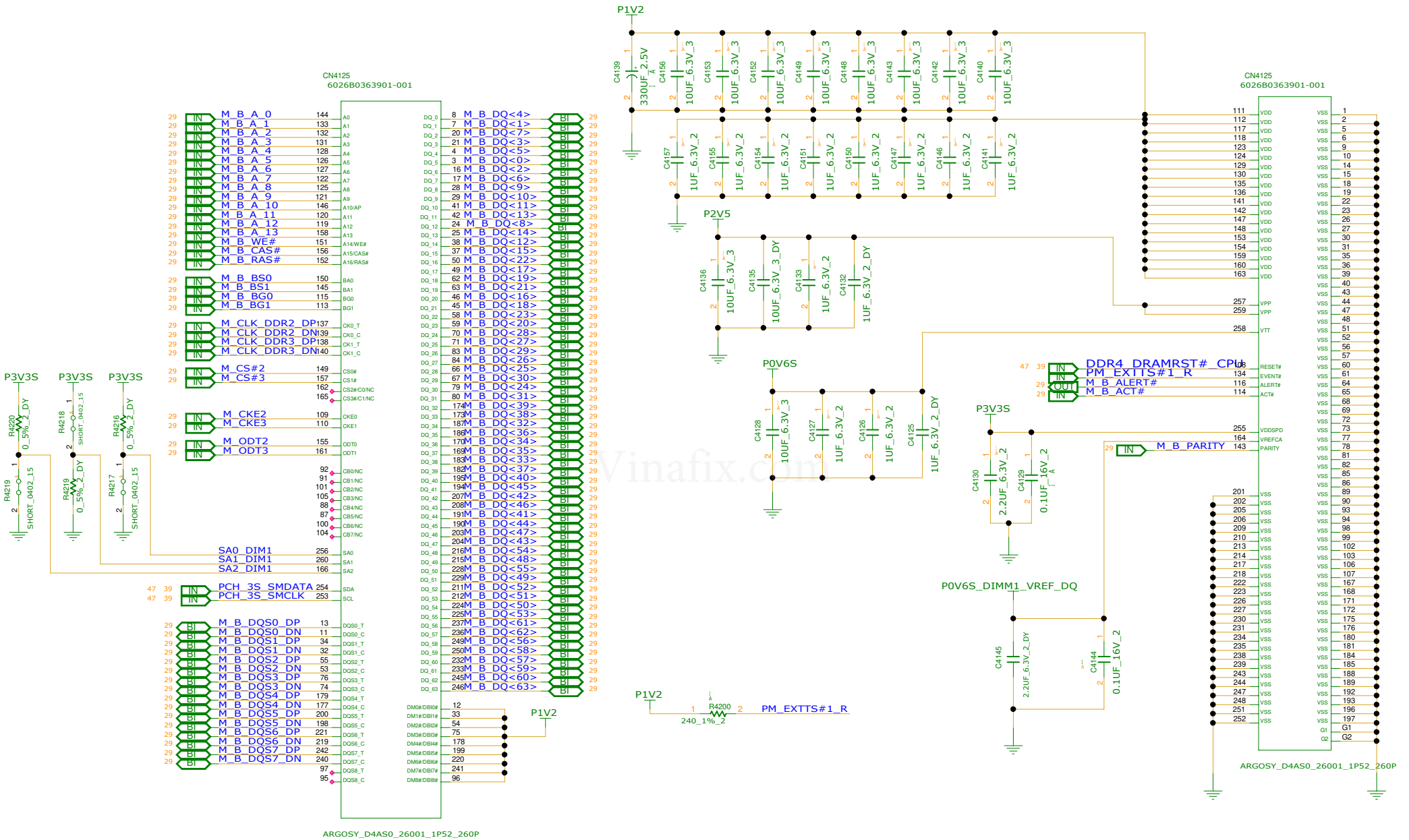
M_A_DQ<59>
M_A_DQ<60>
M_A_DQ<61>
M_A_DQ<62>
M_A_DQ<63>
ARGOSY_D4AR0_26010_1P52_260P
P3V3S
P1V2
P2V5
P0V6S
P3V3A
DDR4_DRAMRST#_CPU
PM_EXTTS#0_R
M_A_ALERT#
M_A_ACT#
M_A_PARITY
P0V6S_DIMM0_VREF_CA
DDR_VTT_PG_CTRL
DDR_PG_CTRL#
DDR_PG_CTRL
DDR_PG_CTRL_R
Q1
MMBT4401
Q2
L2N7002WT1G
ARGOSY_D4AR0_26010_1P52_260P
INVENTEC
MODEL,PROJECT,FUNCTION
DDR4_SO-DIMM0
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SHEET 47 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX
Vinafix.com

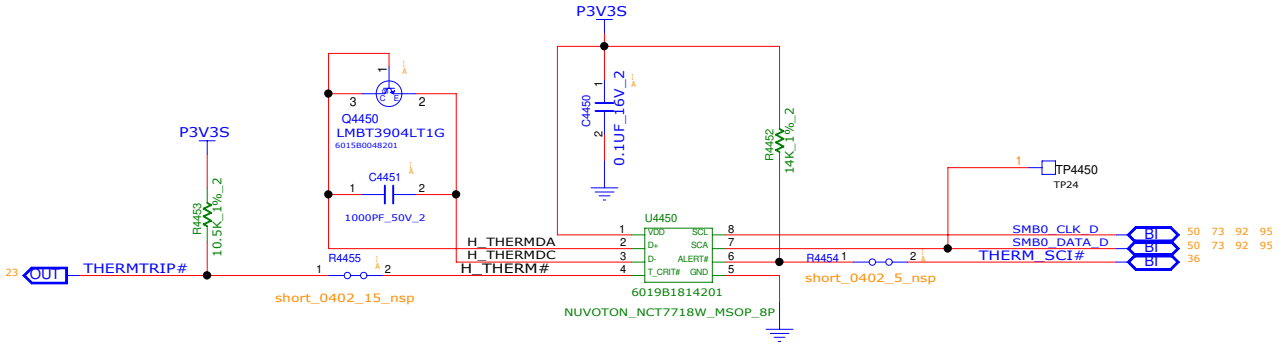


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION DDR4,SO-DIMM1		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	
SHEET 48 of 139			

REFERENCE NUMBER:4450~4499

THERM SENSOR



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

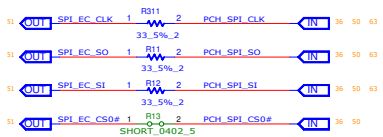
INVENTEC

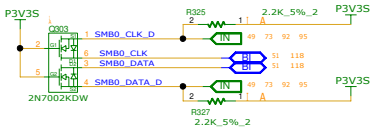
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

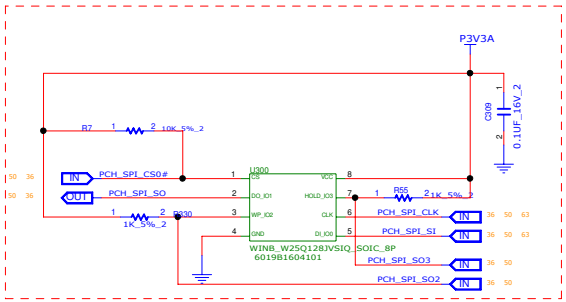
SHEET 49 of 139

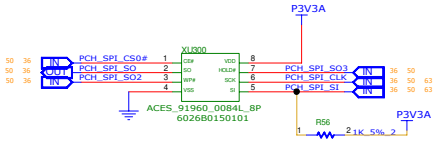
REFERENCE 300~389(KBC)





THERMAL SENSOR
HDMI
DP





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R390 FOR INTEL DEBUG

CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60Xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01
SHEET	50	of	139

EC

Location 300 ~ 389

2013EE1B

Ver.05_20120824

	VCC(1.8V OR 3.3V)	VSTBY_FSPI(1.8V OR 3.3V)
IT8987E_CX	PIN13 : LPCCLK/GPM4(3) PIN10 : LAD0/GPM0(3) PIN9 : LAD1/GPM1(3) PIN8 : LAD2/GPM2(3) PIN7 : LAD3/GPM3(3) PIN6 : LFRAME#/GPM5(3)	PIN5 : SERIRQ/GPM6(3) PIN105 : FSCK/GPG7 PIN101 : FSCE#/GPG3 PIN102 : FMOSI/GPG4 PIN103 : FMISO/GPG5

Platform	Intel	AMD
R319,R318	10KΩ	NA

Platform	Intel	AMD
R315	330Ω	0Ω

Intel DS3 function support

C314 For Intel platform

U1

ITE_IT8987E_CX_LQFP_128P_HP

6019B1650401

Vinafix.com

INVENTEC

MODEL,PROJECT,FUNCTION

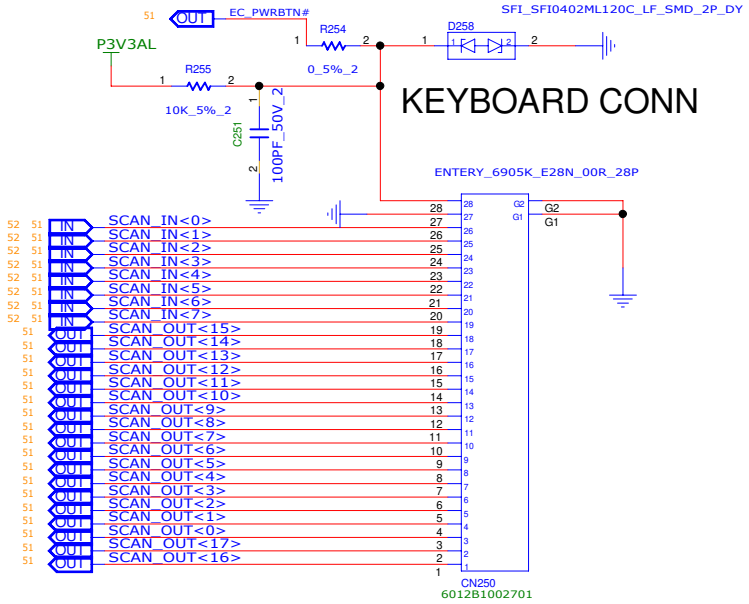
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SHEET 51 of 139

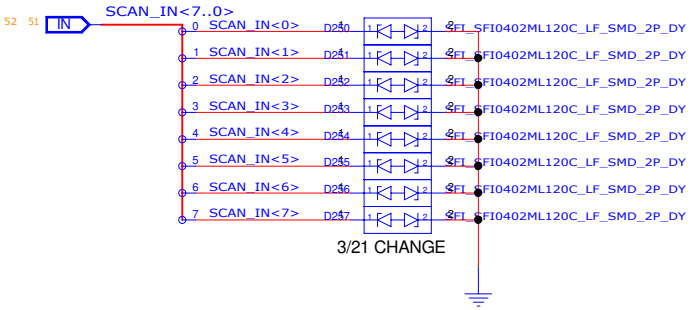
REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



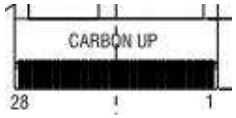
KEYBOARD CONN

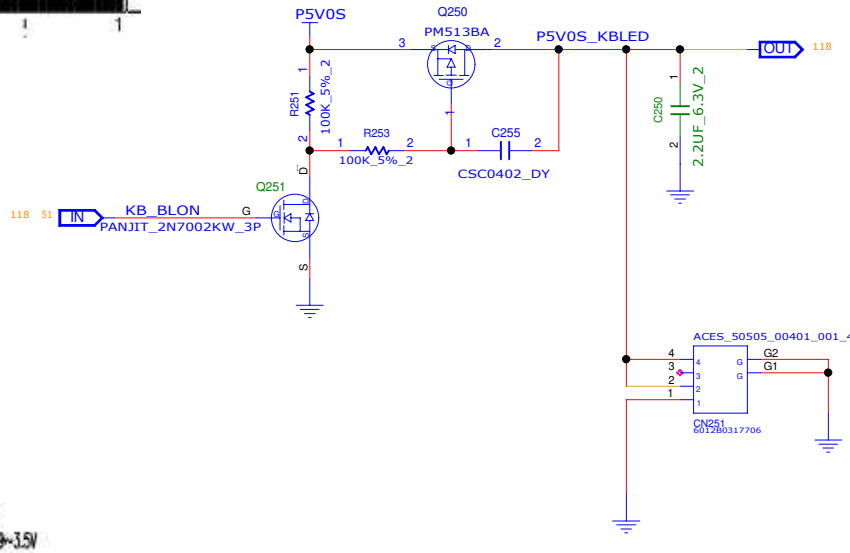
NEE TO CHANGE 6012B1002701
5/2 REVERSE

	14"
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



3/21 CHANGE





KEYBOARD LED CONN

VCC : +5V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

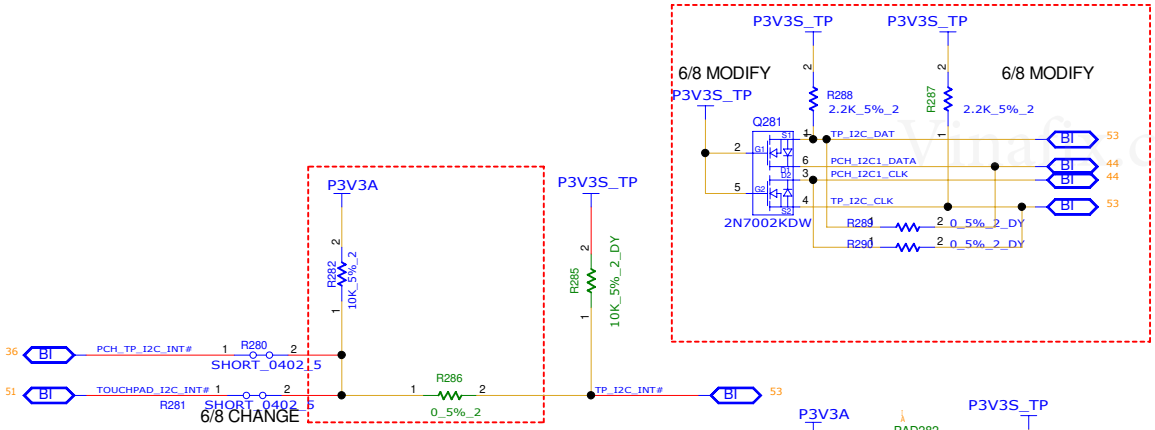
INVENTEC

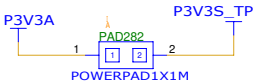
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

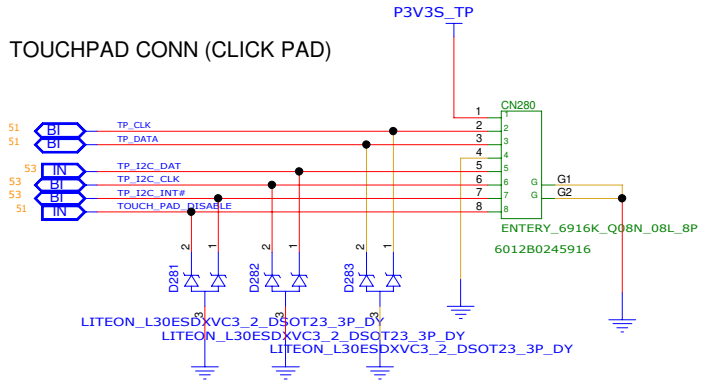
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 52 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX





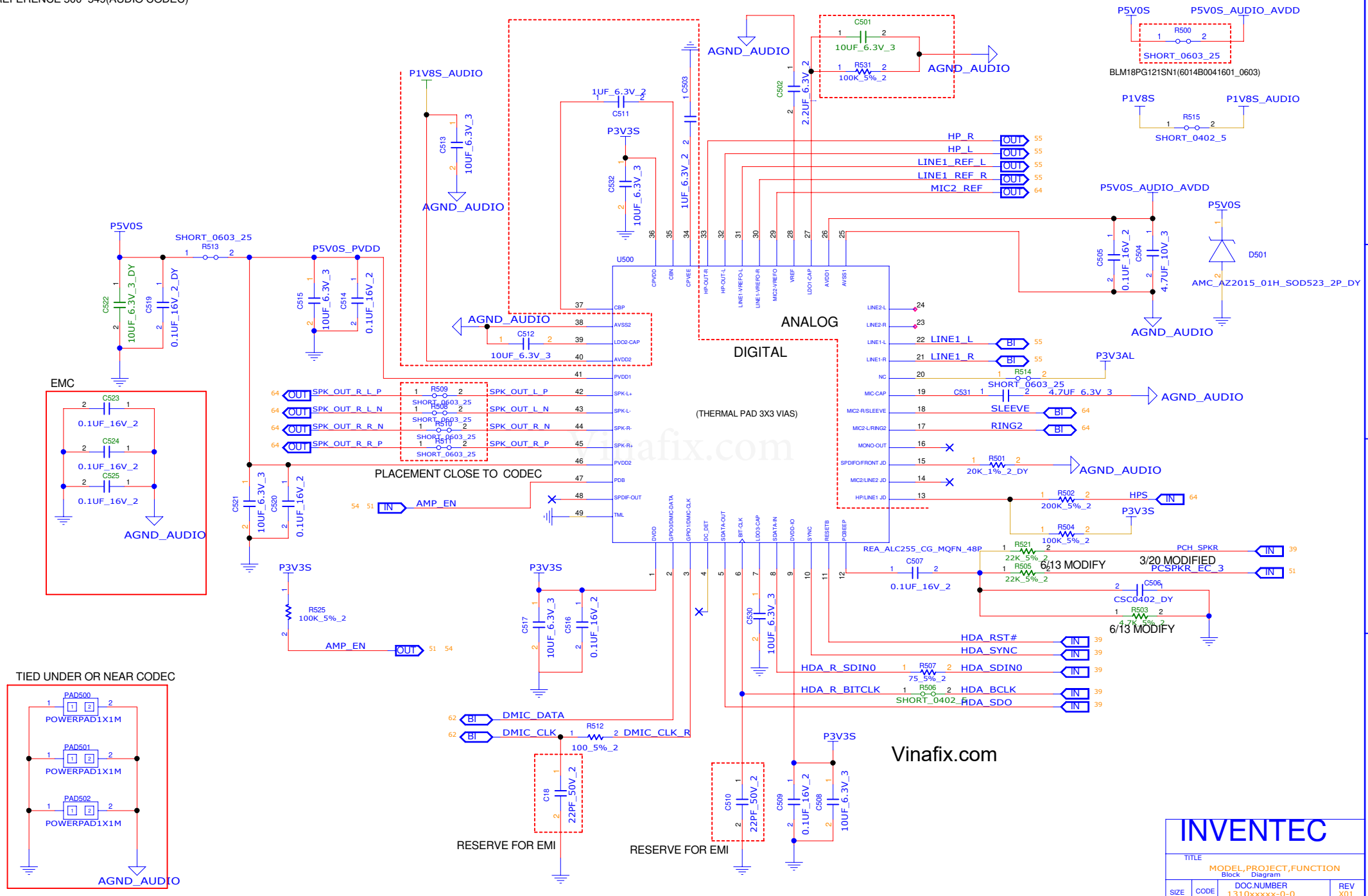


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 53 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

REFERENCE 500~549(AUDIO CODEC)



CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

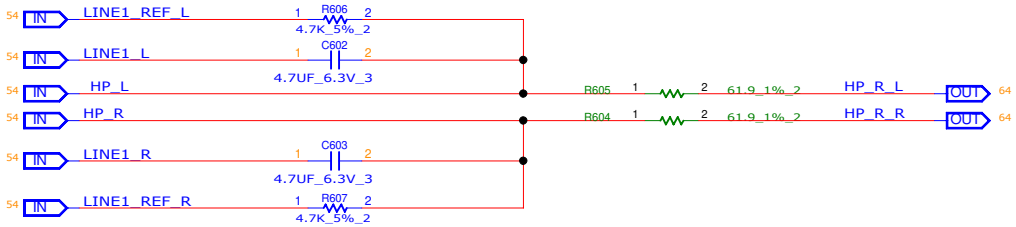
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 54 of 139

REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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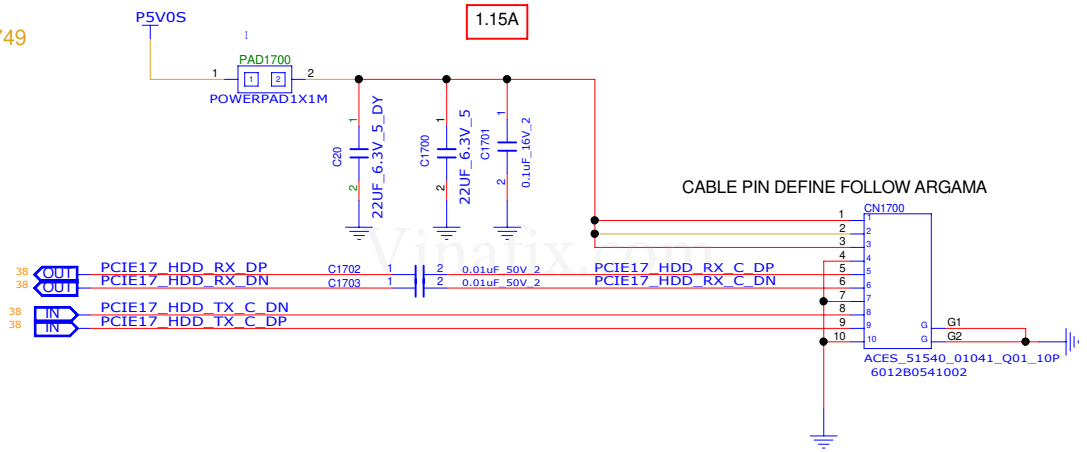
SATA HDD CABLE CONN on MB

SATA HDD
Location 1700 ~ 1749



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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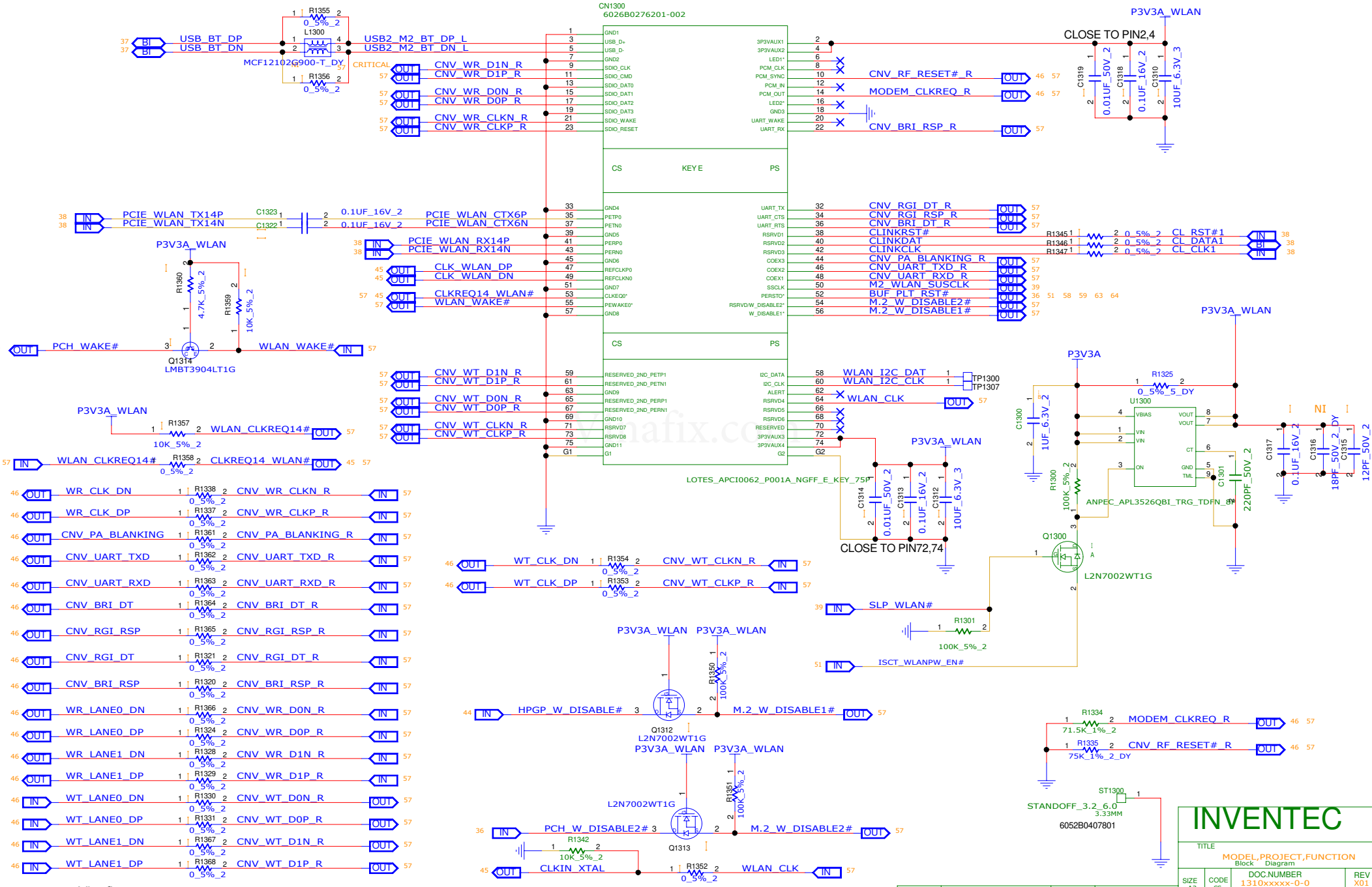
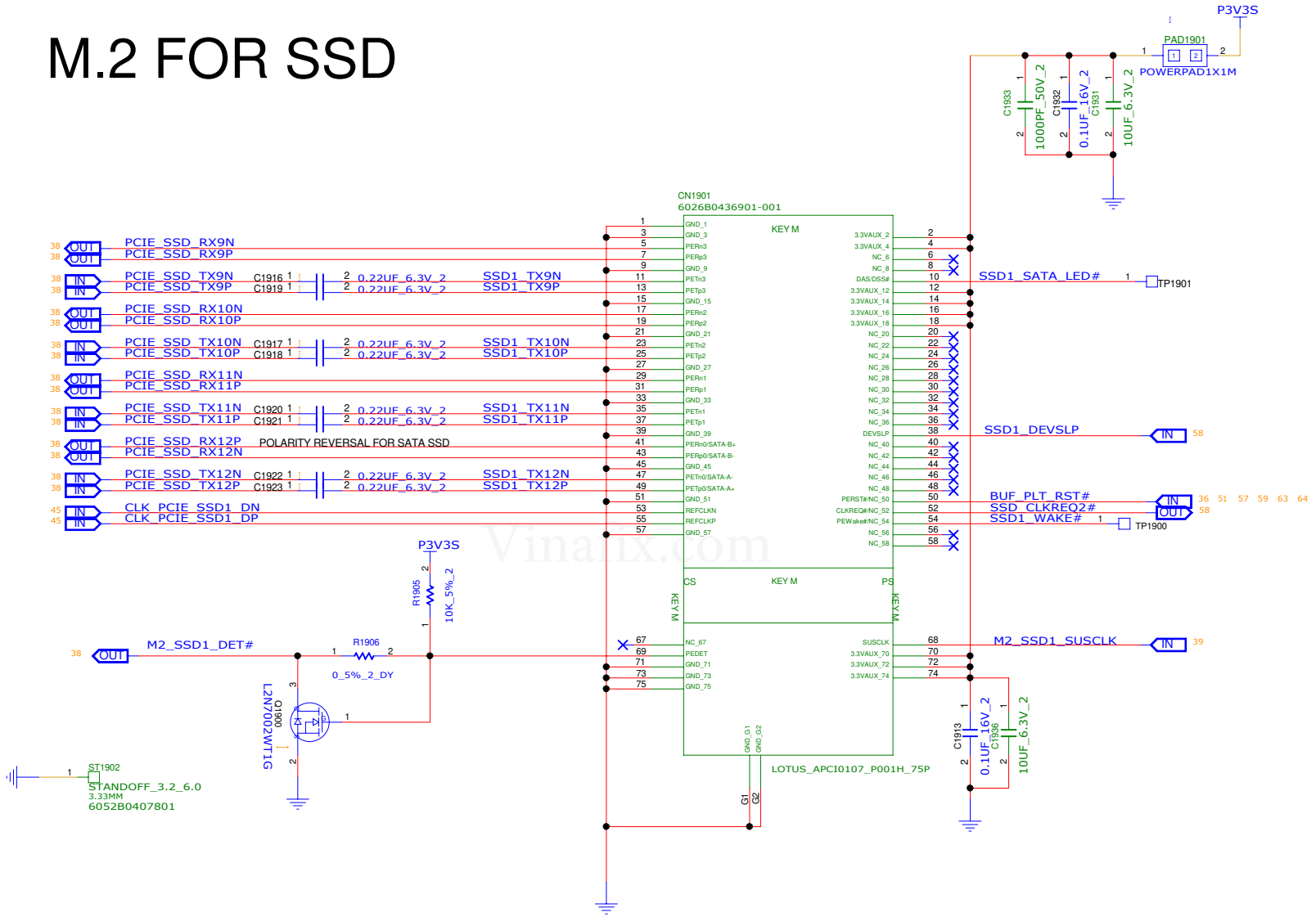
M.2 FOR WLAN/BT



M.2 FOR SSD



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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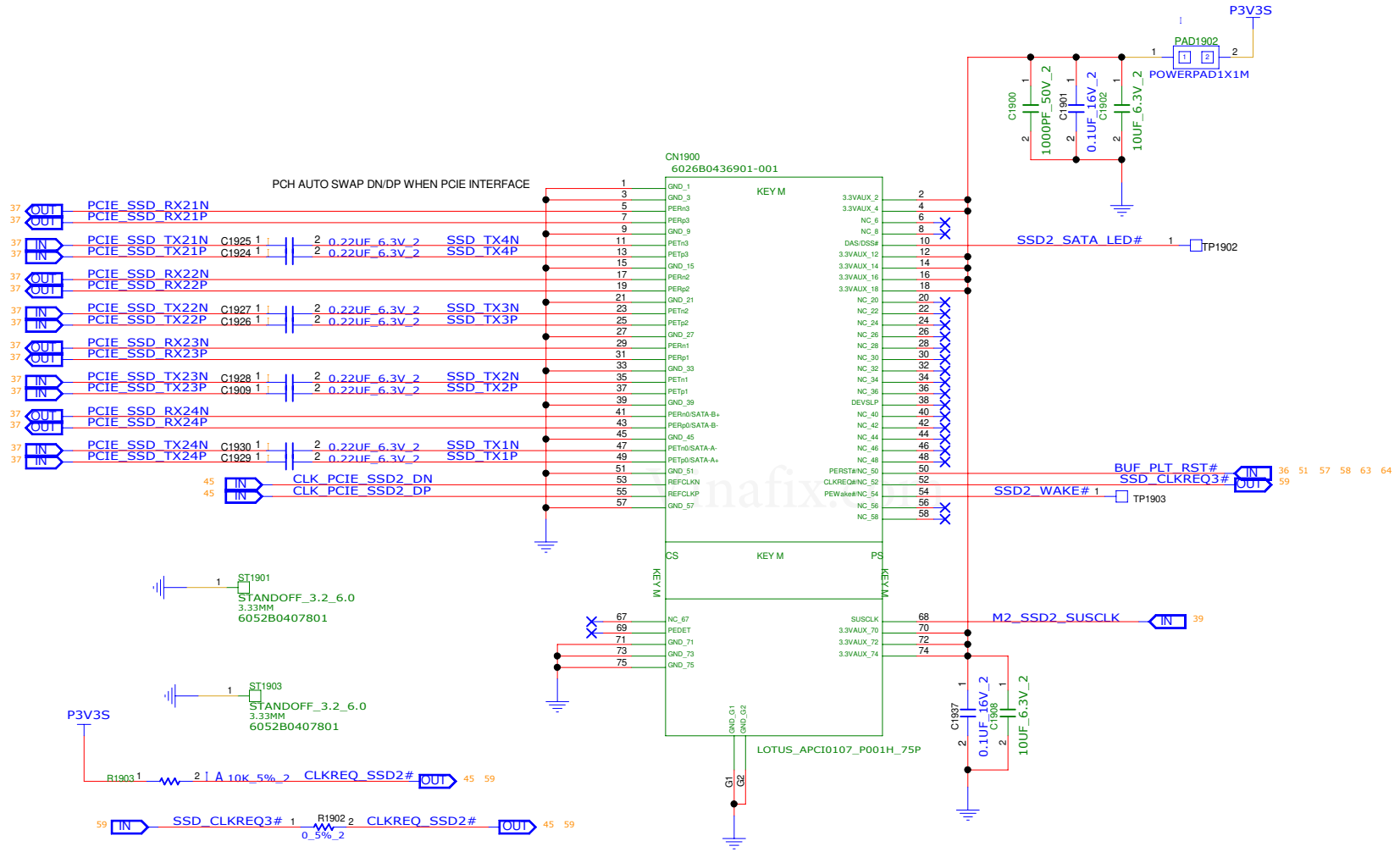
NGFF SSD2(PCIE/SATA 2X)



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

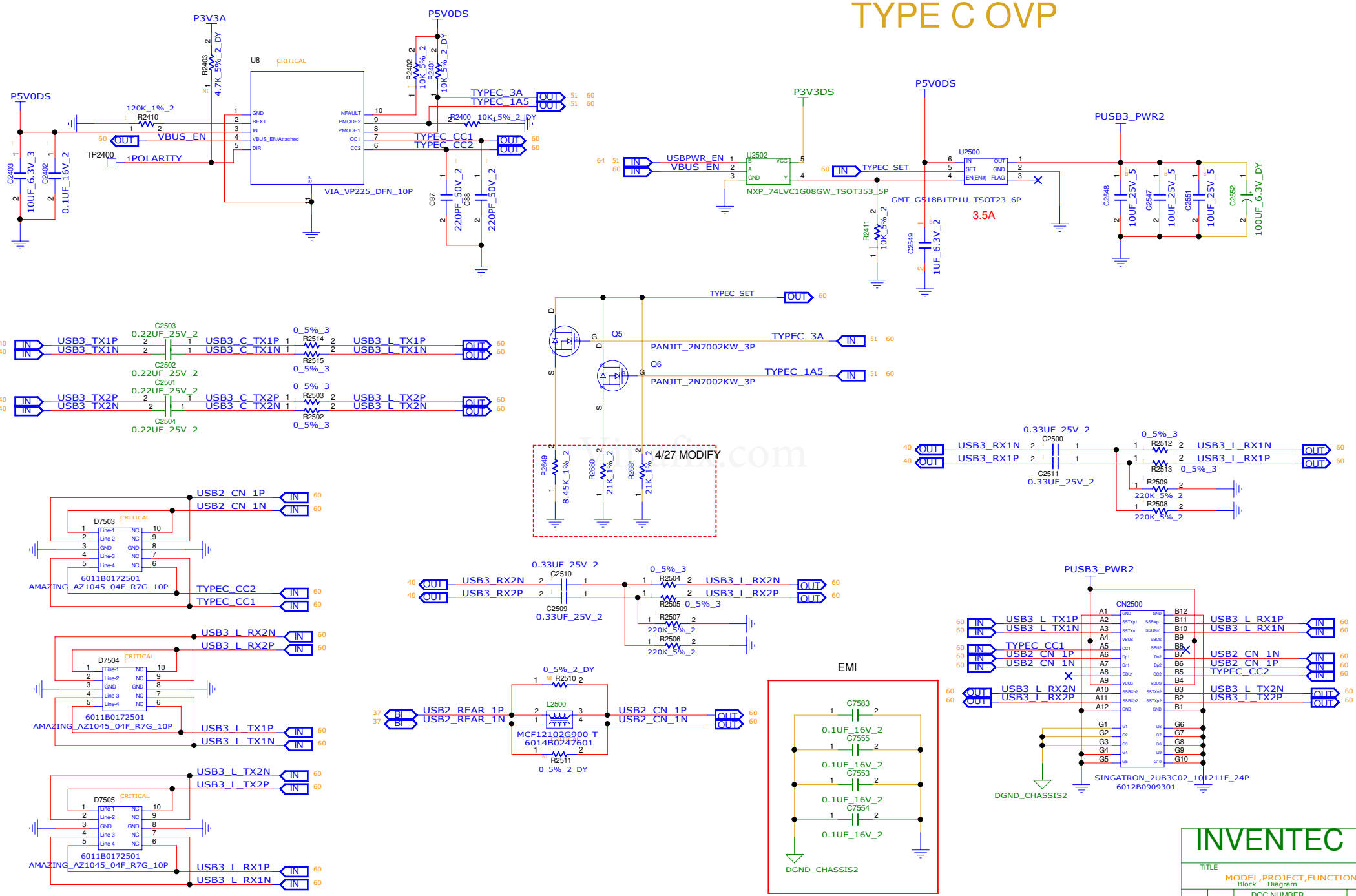
REFERENCE NUMBER:1950~1999

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SATA HDD CONN.		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 59 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TYPE C OVP



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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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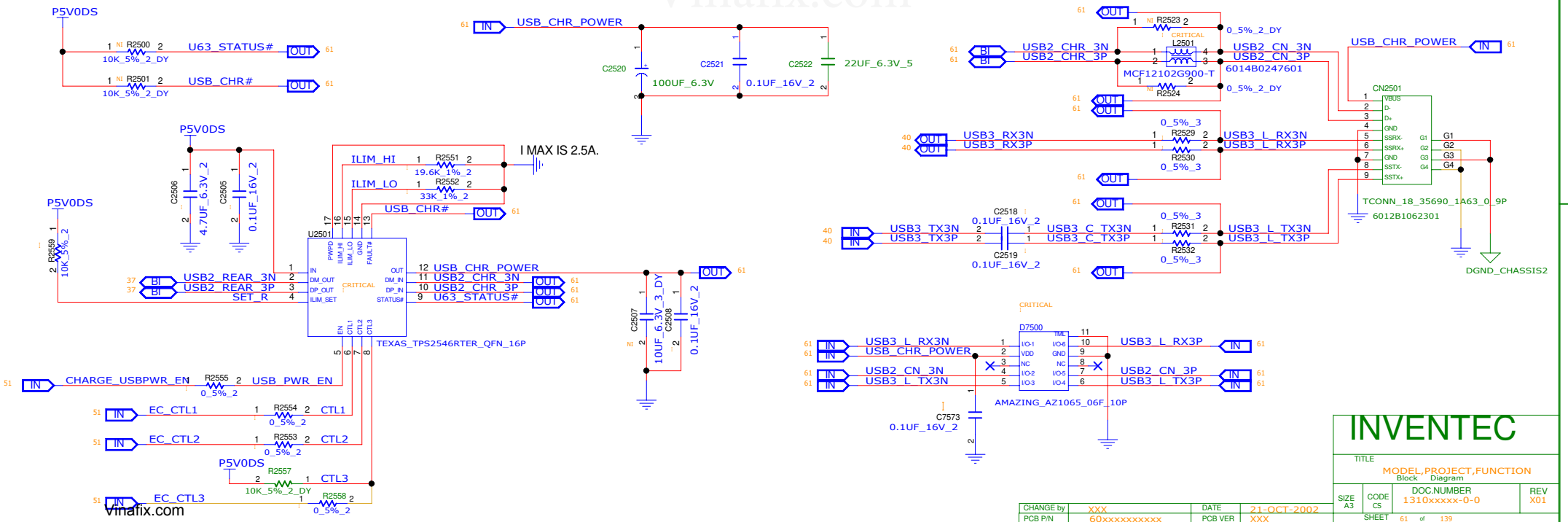
USB CHARGER

USB Faster Charger in S4/S5	USB Charger controller : TI2546	Ctrl-Pin (CTL1/CTL2/CTL3/ILIM_SEL)	Mode	ILIM	Note
Enable	S0	1/1/1/1	CDP	ILIM=2510mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
Disable	S0	1/1/1/1	CDP	ILIM=1525mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/0/0	Turn off switch	ILIM=1525mA	No support charger



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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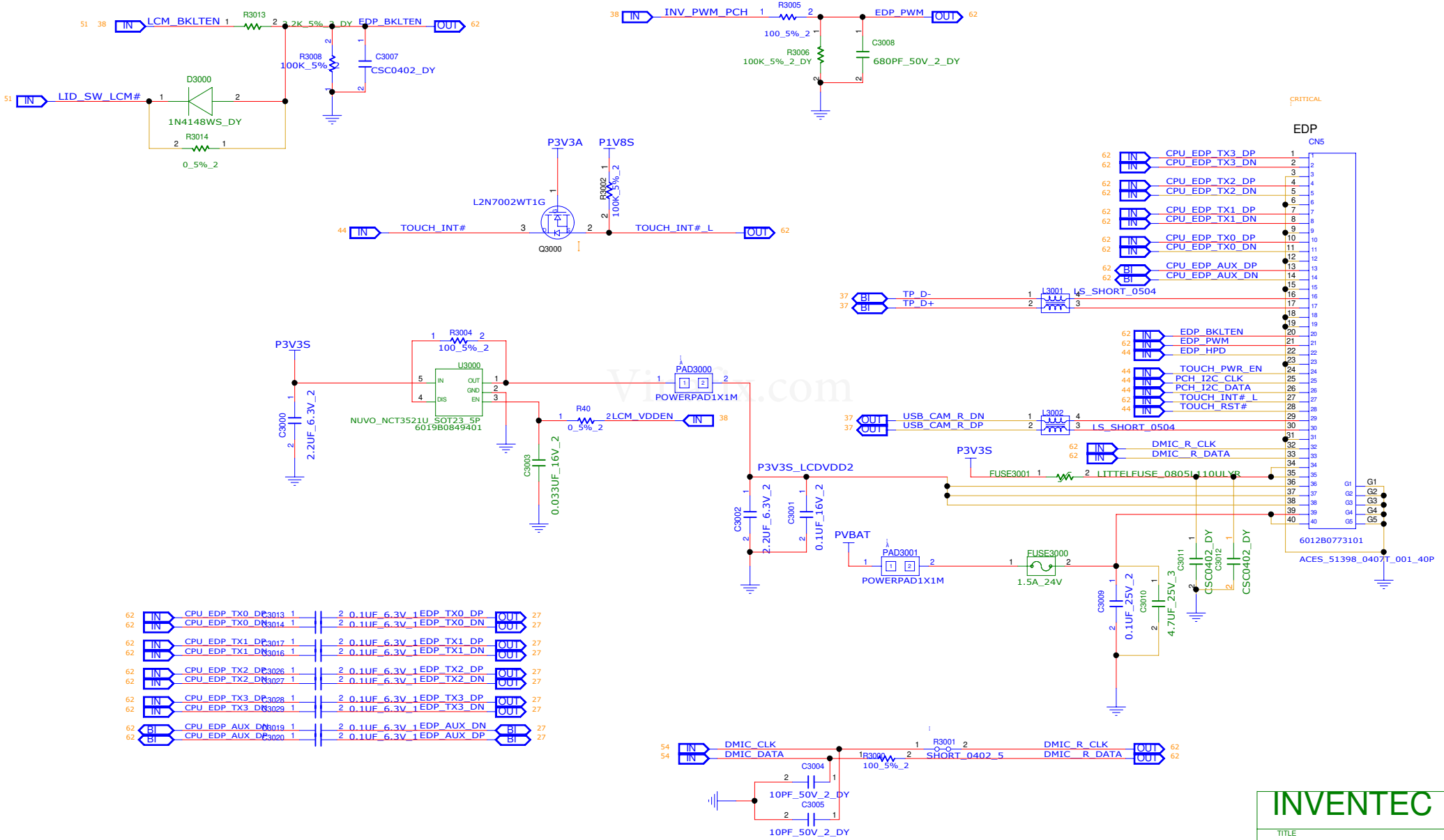
REFFERENCE 3000~3049(LCM)

EDP CONN



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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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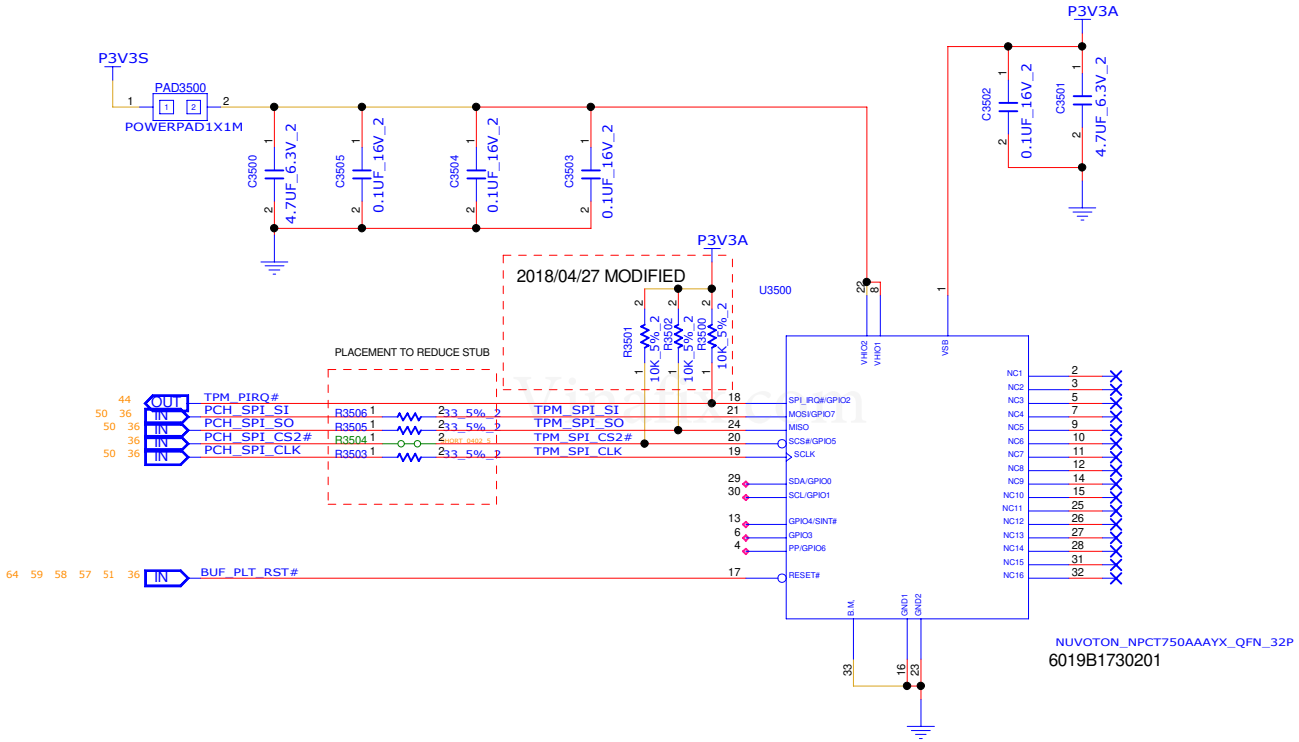
TPM DO NOT INSTALL



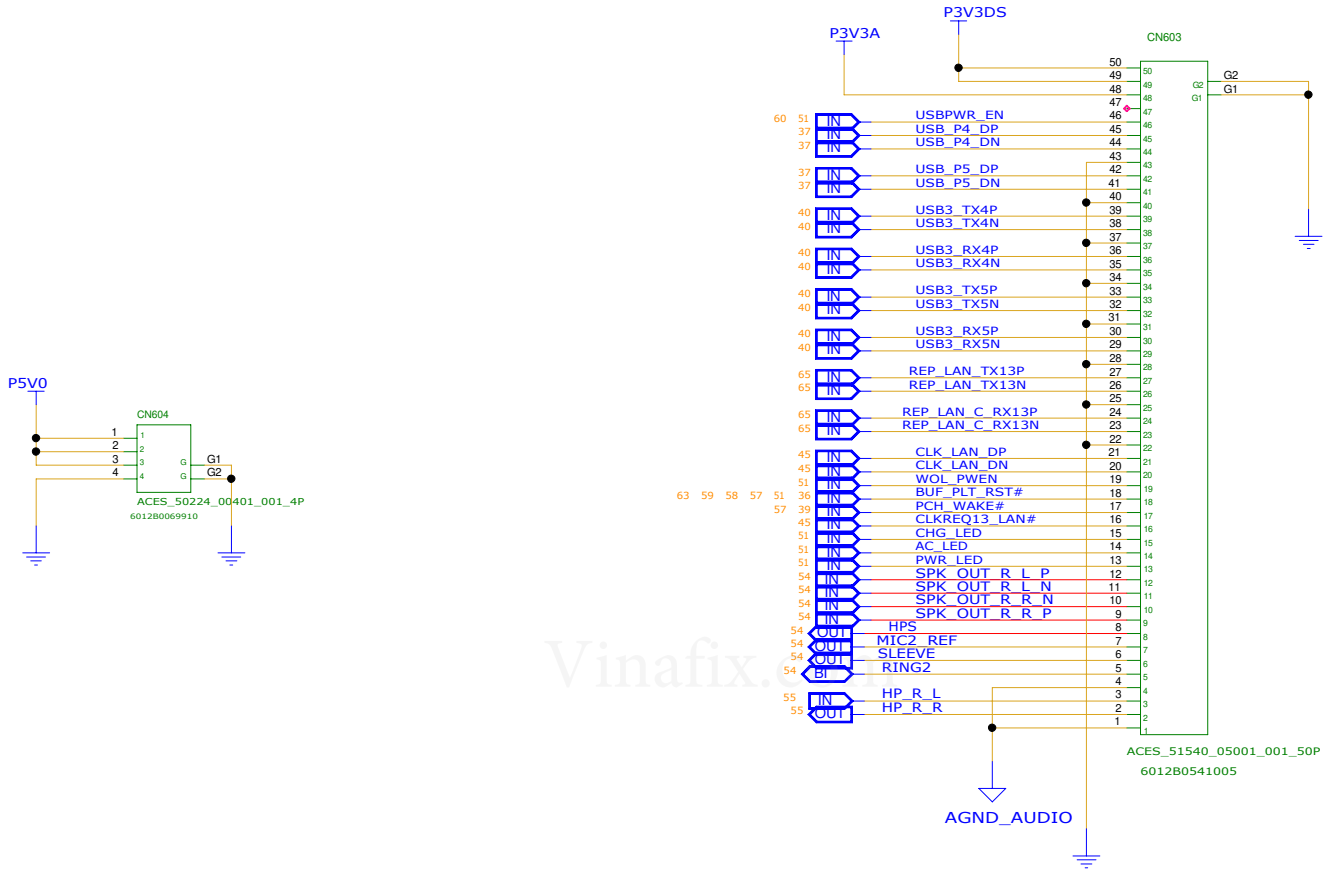
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 63 of 139



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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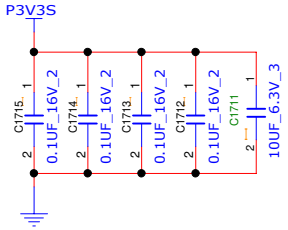
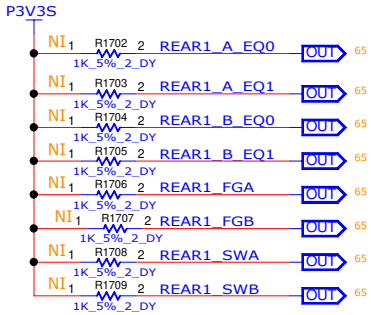
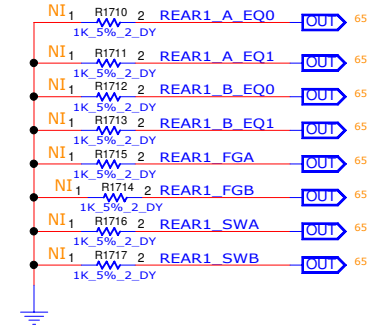
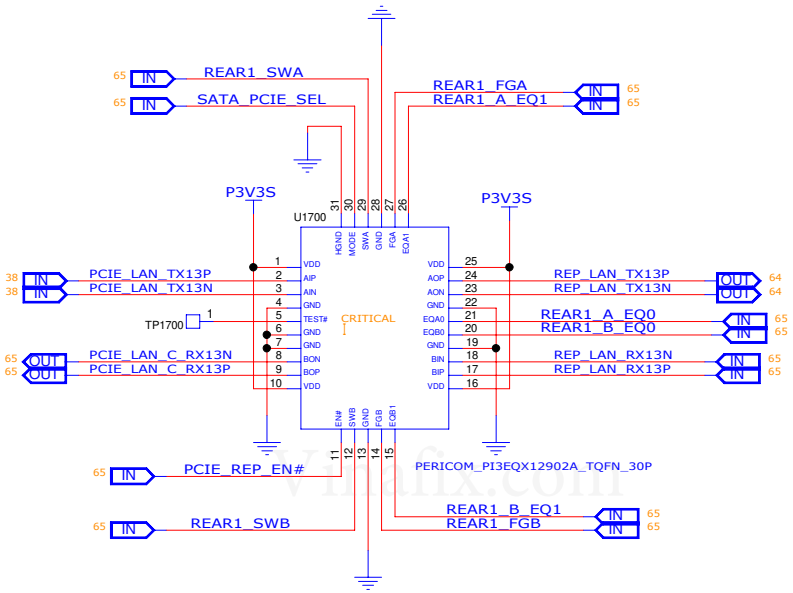
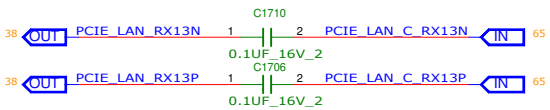
PCIE REPEATER

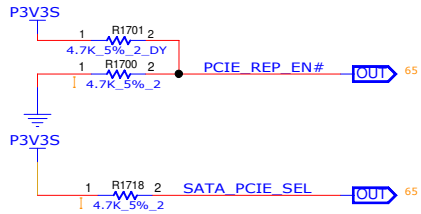


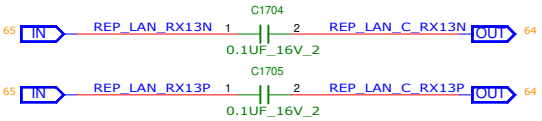












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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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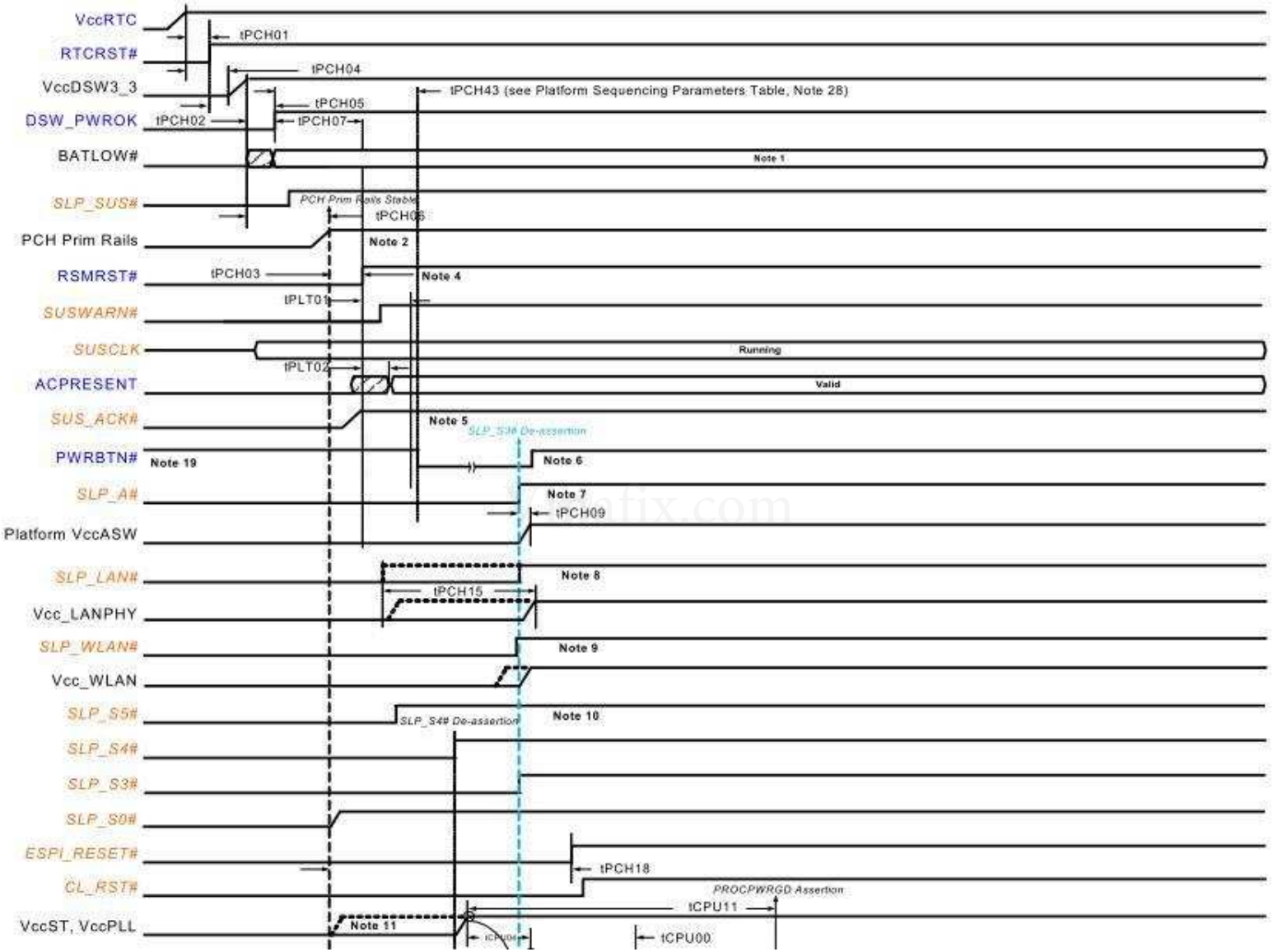
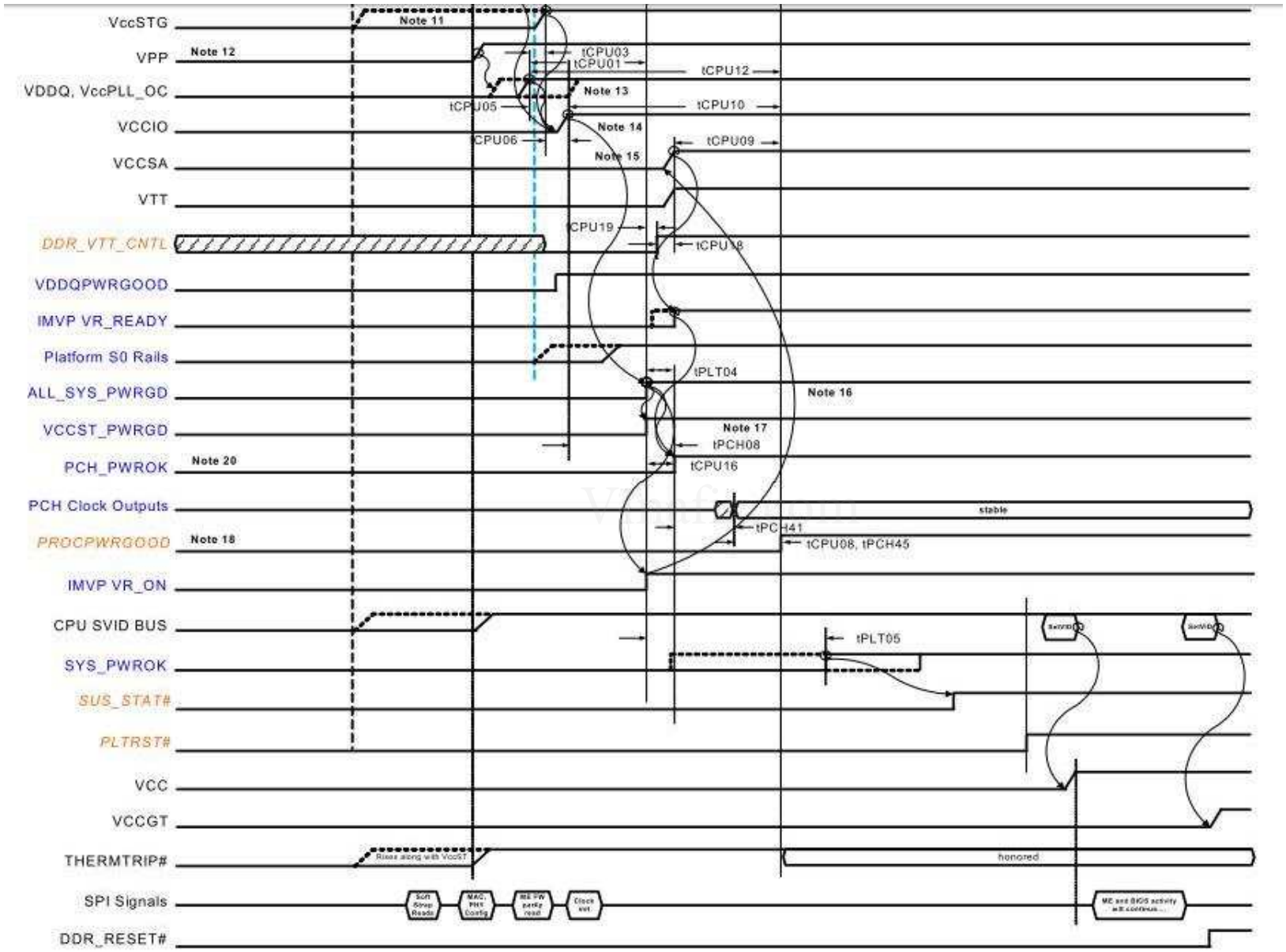


INVENTEC

TITLE: MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 66 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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07e30a1209261000d00169fd1b0036e2

CHANGE by	XXX	DATE	21-OCT-2002
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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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INVENTEC

TITLE
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N18E-G0
N18E-G1
N18E-G2 MAX-Q

8GB DDR5 256M X 16 X 2 X6

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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PCA CODE NAME： N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001
G1 : 6019B1849201
G2 MAXQ:6019B1849301

PCB VERSION：X01
BOARD SIZE:

SCH P/N:
PCB P/N:
PCA P/N:

SHEET	CONTENT	SHEET	CONTENT
71	TITLE	101	GPU 1V8_AON DECOUPLING
72	INDEX	102	GPU NVDD DECOUPLING
73	VGA CONNECTION WITH MAINBOARD	103	GPU FBVDD DECOUPLING
74	GPU PCI-E GEN3 X 16	104	GPU GND
75	GPU MEMORY PARTITION A	105	GPU POWER SEQUENCE
76	GPU MEMORY PARTITION B	106	GPU POWER DISCHARGE
77	GPU MEMORY PARTITION C	107	GPU 1V8_MAIN
78	GPU MEMORY PARTITION D	108	GPU_NVVDD/NVVDDS (MP2886A)
79	GPU MEMORY FBA PARTITION 31-0	109	PVCORE_DGPU (MP86941_1-2P)
80	GPU MEMORY FBA PARTITION 63-32	110	PVCORE_DGPU (MP86941_3-4P)
81	GPU MEMORY FBB PARTITION 31-0	111	PVCORE_DGPU (MP86941_5-6P)
82	GPU MEMORY FBB PARTITION 63-32	112	P1V35S_DGPU (RT8816A_2P)
83	GPU MEMORY FBC PARTITION 31-0	113	P1V0S_DGPU (RT8068A)
84	GPU MEMORY FBC PARTITION 63-32	114	P1V8S_DGPU (RT8068A)
85	GPU MEMORY FBD PARTITION 31-0	115	NOTES
86	GPU MEMORY FBD PARTITION 63-32	116	HISTORY
87	GPU 27 MHZ XTAL	117	
88	GPU VBIOS, STRAPS	118	
89	GPU GPIOS	119	
90	GPU IFP_AB	120	
91	GPU DP IFP_CD	121	
92	GPU DP REDRIVER PI3DPX1203ZHEX	122	
93	GPU DP CONNECTOR	123	
94	GPU HDMI IFP_EF	124	
95	GPU HDMI RETIMER IT66317	125	
96	GPU HDMI CONNECTOR	126	
97	GPU NVHS	127	
98	OVR-M	128	
99	GPU NVDD	129	
100	GPU FBVDD	130	

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL
NI: NON-INSTALL
DY: NON-INSTALL
MP: PRODUCTION
PROTO: PRE-PRODUCTION
CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14
6019B1847601

MICRON MT61K256M32JE-14:A
6019B1847701

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CONNECTION TO MAINBOARD

CLK_PCIE_DGPU_100MHZ_P
CLK_PCIE_DGPU_100MHZ_N
PCIE_DGPU_RX15P
PCIE_DGPU_RX15N
PCIE_DGPU_TX15P
PCIE_DGPU_TX15N
PCIE_DGPU_RX14P
PCIE_DGPU_RX14N
PCIE_DGPU_TX14P
PCIE_DGPU_TX14N
PCIE_DGPU_RX13P
PCIE_DGPU_RX13N
PCIE_DGPU_TX13P
PCIE_DGPU_TX13N
PCIE_DGPU_RX12P
PCIE_DGPU_RX12N
PCIE_DGPU_TX12P
PCIE_DGPU_TX12N
PCIE_DGPU_RX11P
PCIE_DGPU_RX11N
PCIE_DGPU_TX11P
PCIE_DGPU_TX11N
PCIE_DGPU_RX10P
PCIE_DGPU_RX10N
PCIE_DGPU_TX10P
PCIE_DGPU_TX10N
PCIE_DGPU_RX9P
PCIE_DGPU_RX9N
PCIE_DGPU_TX9P
PCIE_DGPU_TX9N
PCIE_DGPU_RX8P
PCIE_DGPU_RX8N
PCIE_DGPU_TX8P
PCIE_DGPU_TX8N
PCIE_DGPU_RX7P
PCIE_DGPU_RX7N
PCIE_DGPU_TX7P
PCIE_DGPU_TX7N
PCIE_DGPU_RX6P
PCIE_DGPU_RX6N
PCIE_DGPU_TX6P
PCIE_DGPU_TX6N
PCIE_DGPU_RX5P
PCIE_DGPU_RX5N
PCIE_DGPU_TX5P
PCIE_DGPU_TX5N
PCIE_DGPU_RX4P
PCIE_DGPU_RX4N
PCIE_DGPU_TX4P
PCIE_DGPU_TX4N
PCIE_DGPU_RX3P
PCIE_DGPU_RX3N
PCIE_DGPU_TX3P
PCIE_DGPU_TX3N
PCIE_DGPU_RX2P
PCIE_DGPU_RX2N
PCIE_DGPU_TX2P
PCIE_DGPU_TX2N
PCIE_DGPU_RX1P
PCIE_DGPU_RX1N
PCIE_DGPU_TX1P
PCIE_DGPU_TX1N
PCIE_DGPU_RX0P
PCIE_DGPU_RX0N
PCIE_DGPU_TX0P
PCIE_DGPU_TX0N

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DGPU_PWR_EN

GPU PWR ENABLE COME FROM PCH/EC
MAKE SURE 10K P3V3S PULL UP

PCH_PLTRST#_BUF

PCH PLATFORM RESET#
MAKE SURE 100K PULL TO GND

IRMT_HOLD_RST#

PCH HOLD RESET#
MAKE SURE 100K PULL TO GND

TO PCH

GPU_EVENT_PCH#

PCH INFORM GPU WILL EXIT GC6 MODS

DGPU_PWRLEVEL

15.3.2 PWR_LEVEL* (GPIO12)

The POWER_LEVEL input signal triggers an immediate GPU hardware slow-down, followed by the driver capping the GPU power state to the appropriate limit. There are two events that can trigger this signal assertion: AC to battery power transition or total system power overdraw event.

PEX_CLKREQ#

PCIE CLK REQUESTD#

ALL_POWER_GOOD

GPU ALL S RAIL GOOD
MAKE SURE 10K P3V3S PULL UP

DP_MA_HPD#

DP HPD TO MAINBOARD
MAKE SURE 10K P3V3S PULL UP

SMB0_DATA_D
SMB0_CLK_D

DP REDRIVER I2C CONNECT TO MOBARD
MAINBOARD NEED TO PULL UP

HDMI_MB_HPD#

HDMI HPD TO MB

SMB0_DATA_D
SMB0_CLK_D

HDMI RETIMER I2C TO MB
MAINBOARD NEED TO PULL UP

GPU_OVERT_EC#

3.3V LEVEL
OVER TEMPERATURE TO PCH OR EC

GC6_FB_EN_PCH

3.3V LEVEL
GC6 ENABLE SIGNAL TO PCH OR EC

EC

EC_SMBDATA0
EC_SMBCLK0

GPU I2C, COMMUNCATED WITH EC
THIS SIGNAL REQUIRE AN EXTERNAL PULL UP

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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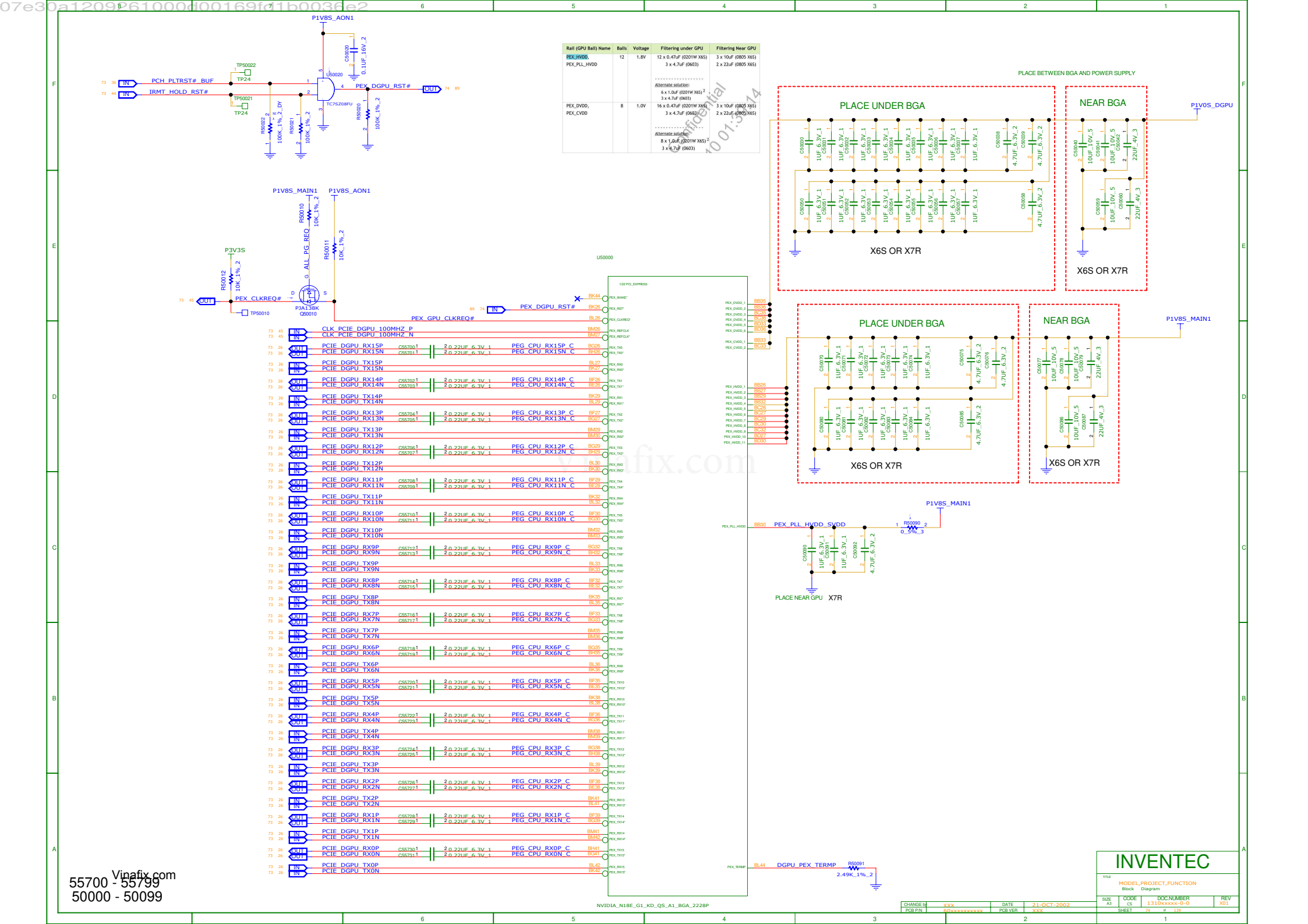
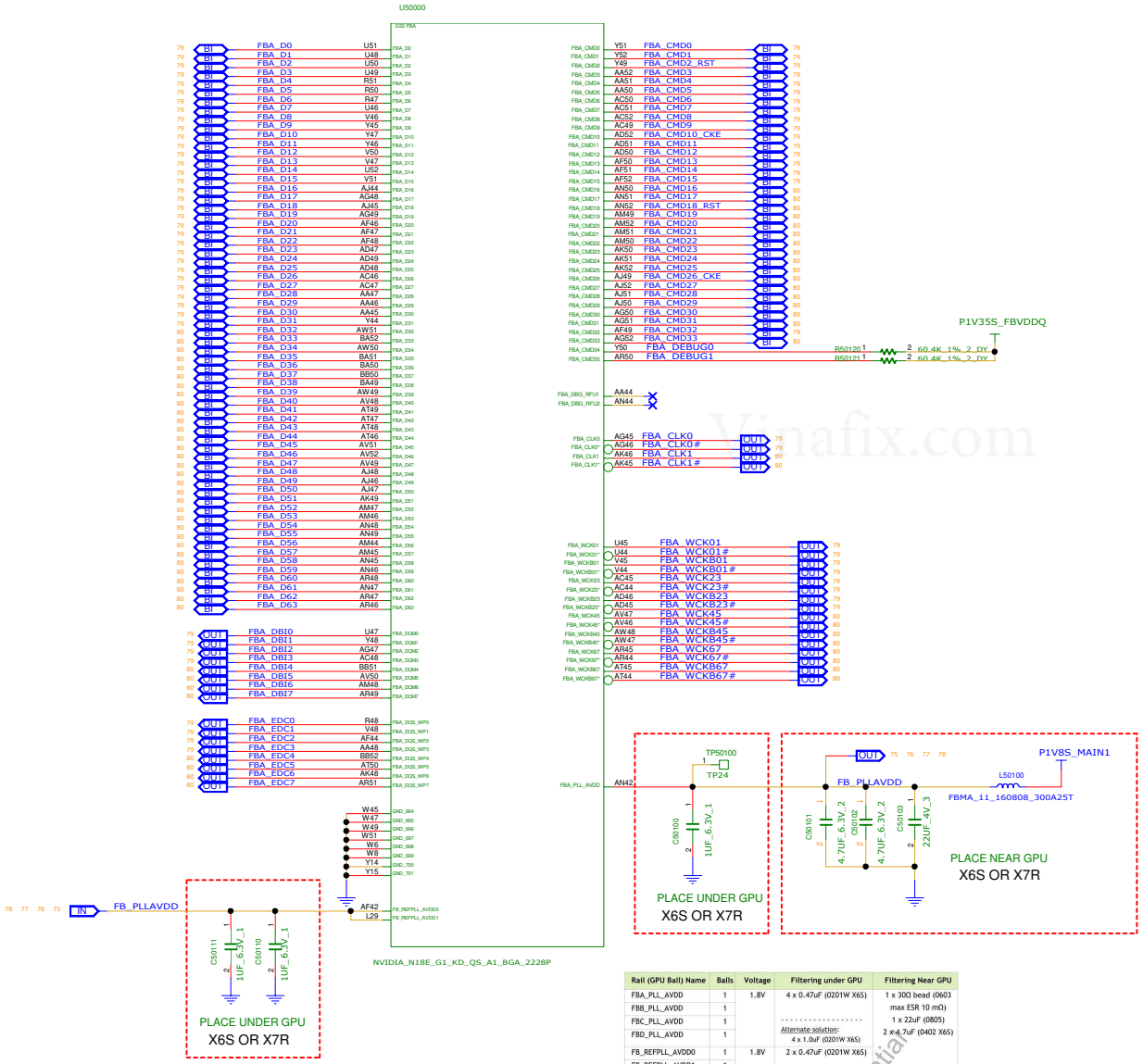


Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD, PEX_PLL_HVDD	12	1.8V	12 x 0.47uF (0201W X6S) 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
			Alternate solution: 6 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	
PEX_DVDD, PEX_CVDD	8	1.0V	16 x 0.47uF (0201W X6S) 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
			Alternate solution: 8 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	

GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1			
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1			
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	

50100 - 50199

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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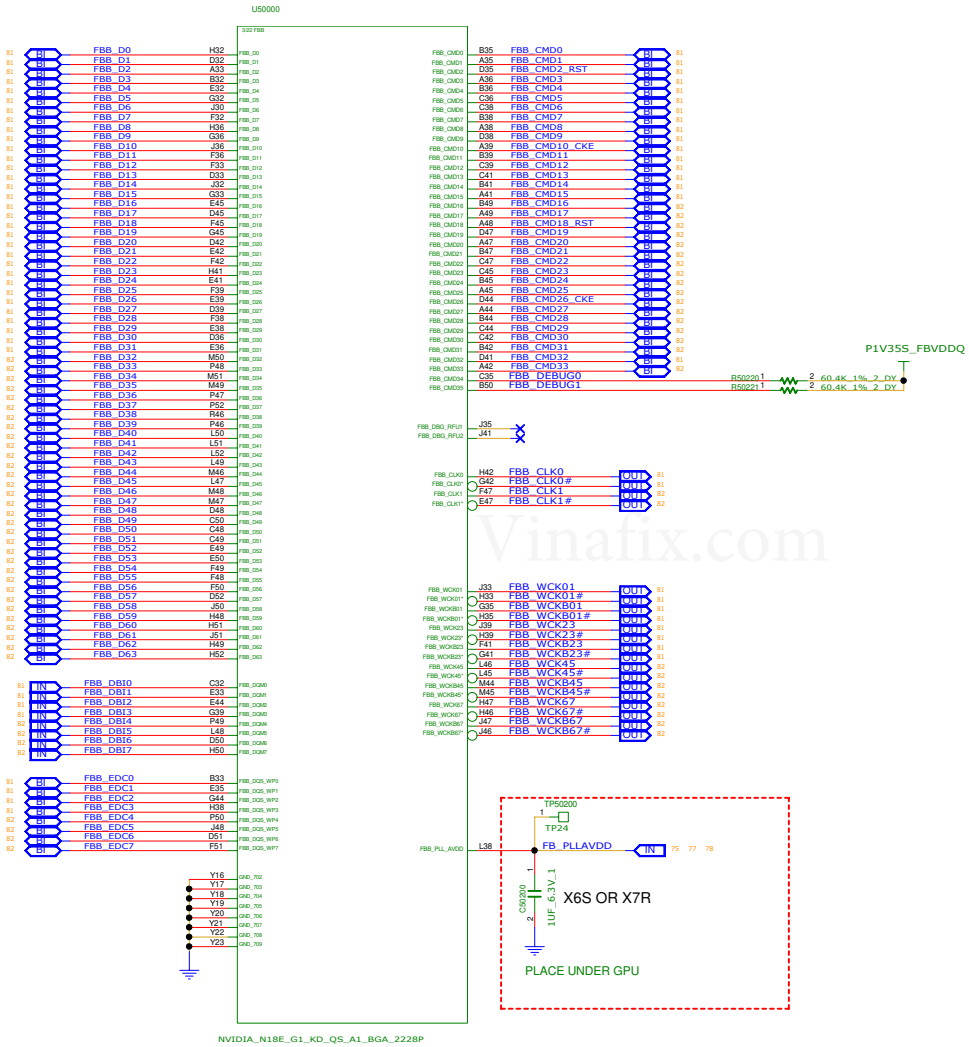
GPU FRAME BUFFER B



50200 - 50299

INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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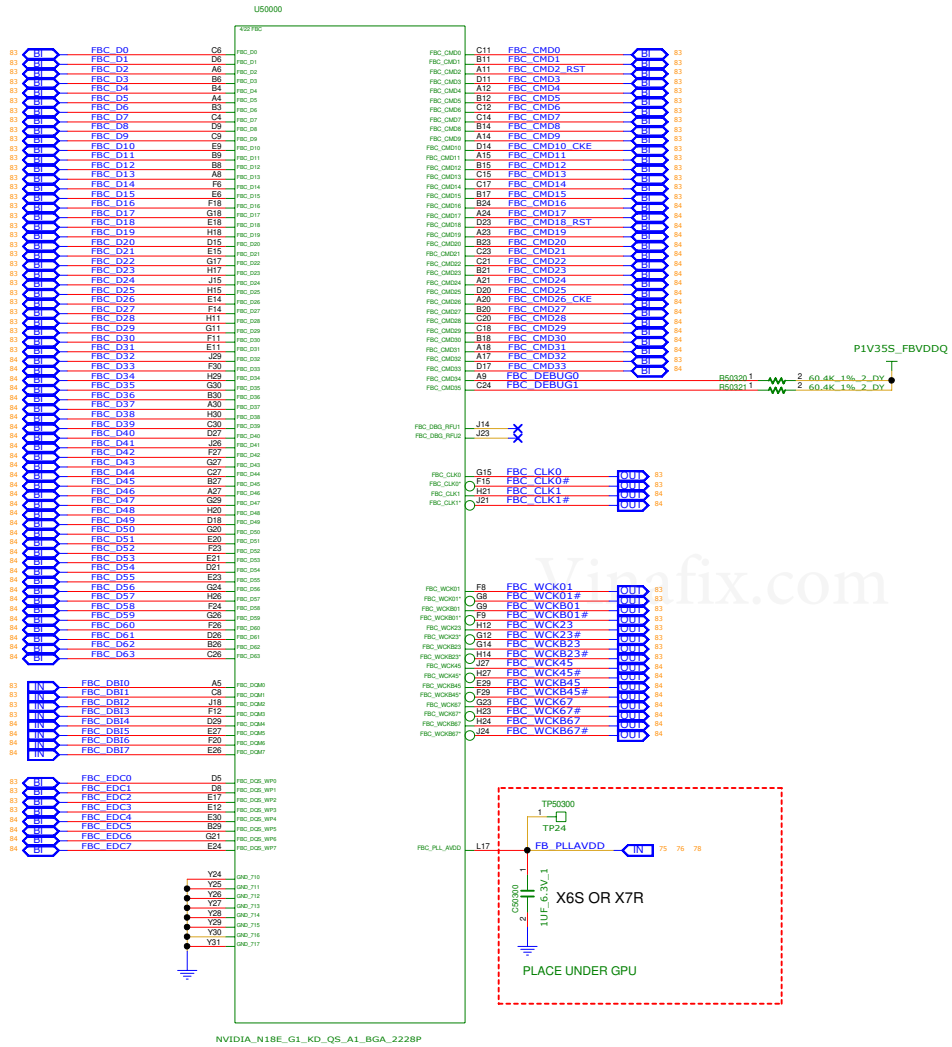
GPU FRAME BUFFER C



50300 - 50399

CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-D-D	X01

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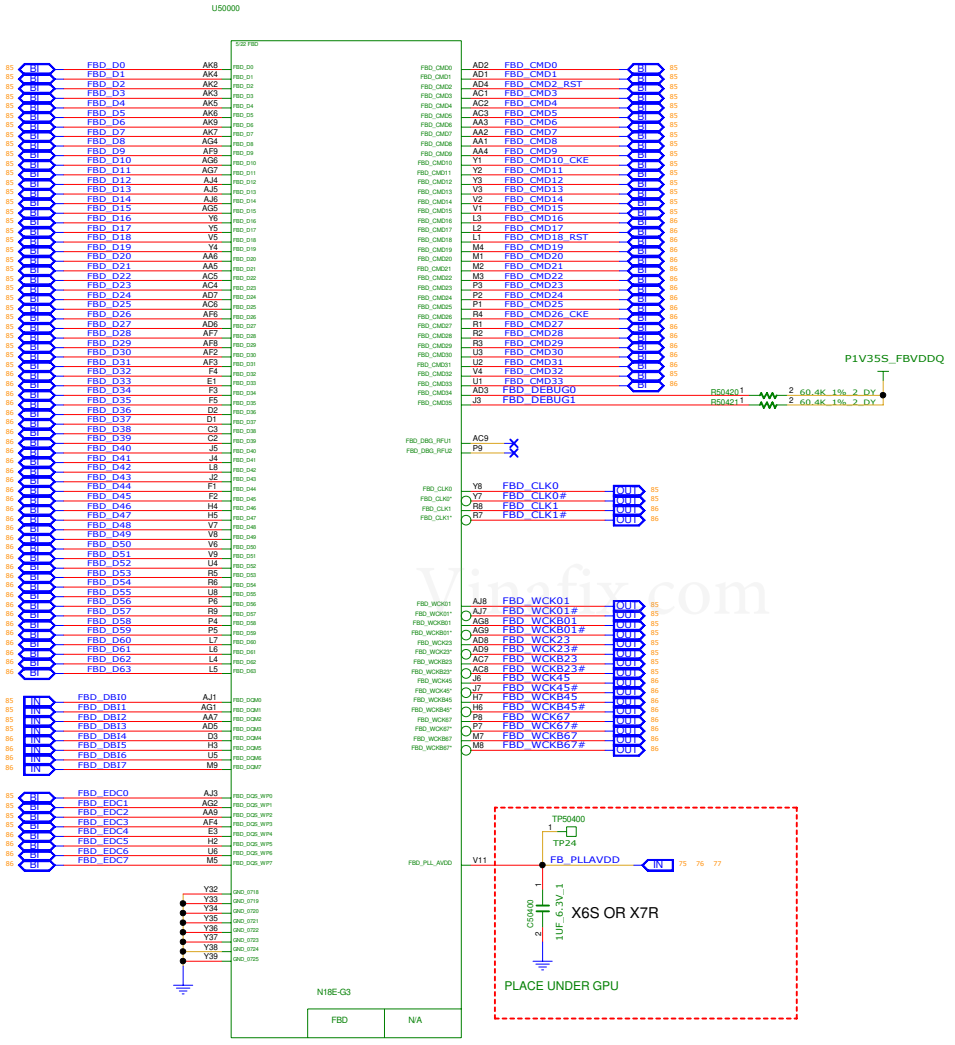
GPU FRAME BUFFER D



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SIZE	CODE	DOC NUMBER	REV
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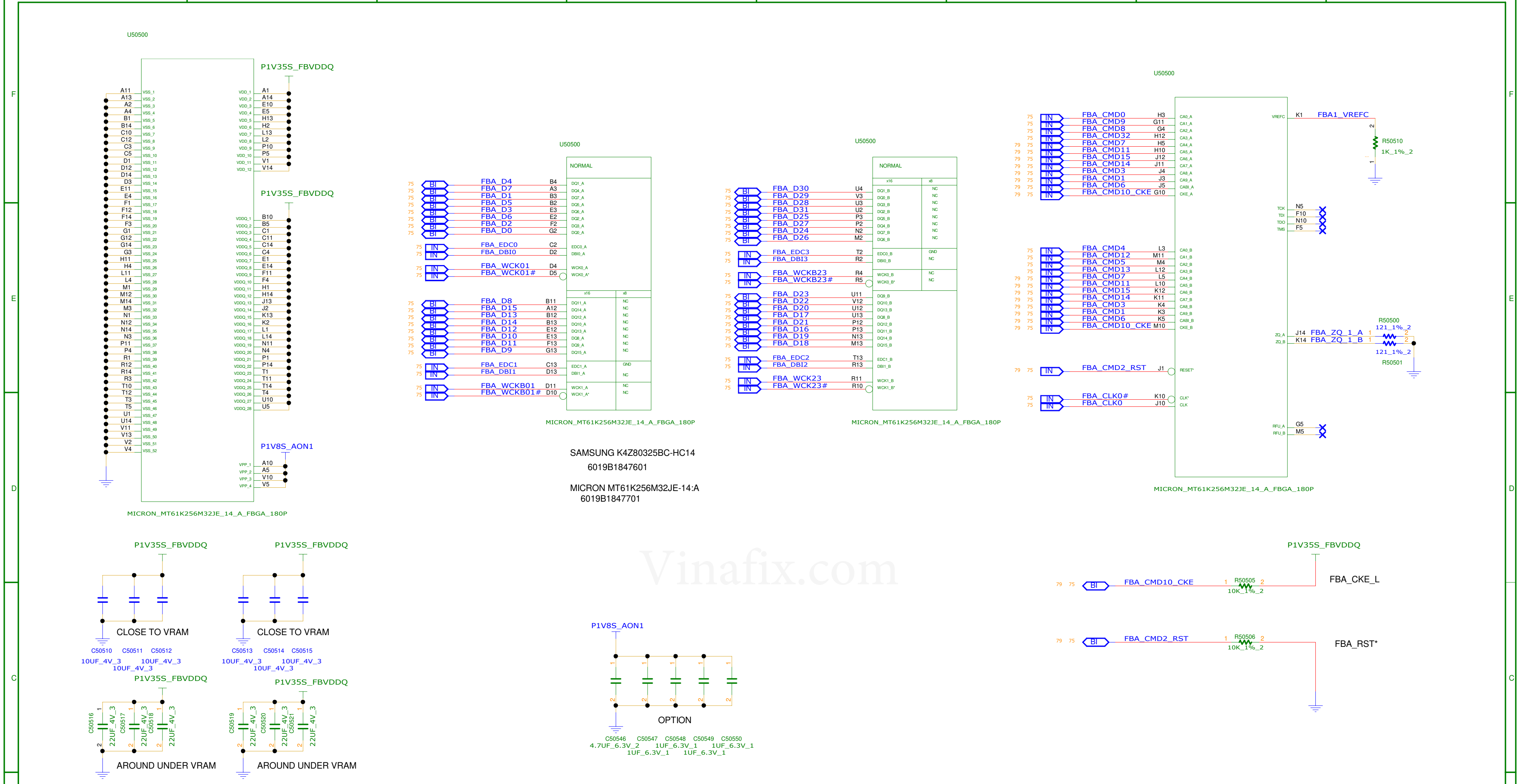

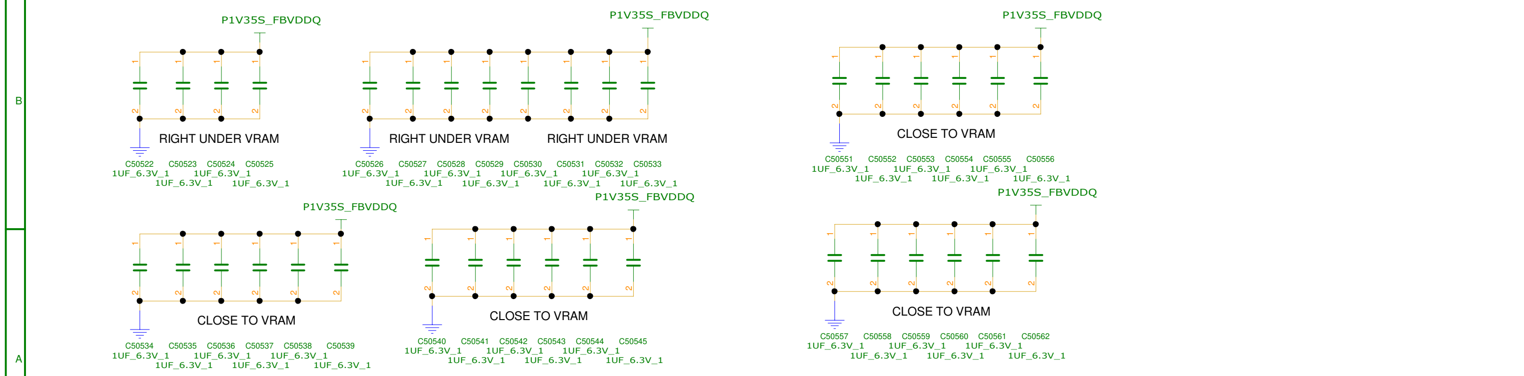

Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF NOTE 2	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Around DRAM
22 uF	X6S [0603]	6	
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

NOTE 1: NVIDIA reference designs use and recommend 0201 or 0201W capacitors where needed. PCB design teams should ensure that component placement equipment can support the smaller package size.

NOTE 2: Alternatively, instead of using 36 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 18 capacitors of value 1.0 uF (X6S, 0201W).

NOTE 3: Alternatively, instead of using 4 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 4 capacitors of value 1.0 uF (X6S, 0201W), one per VPP ball.

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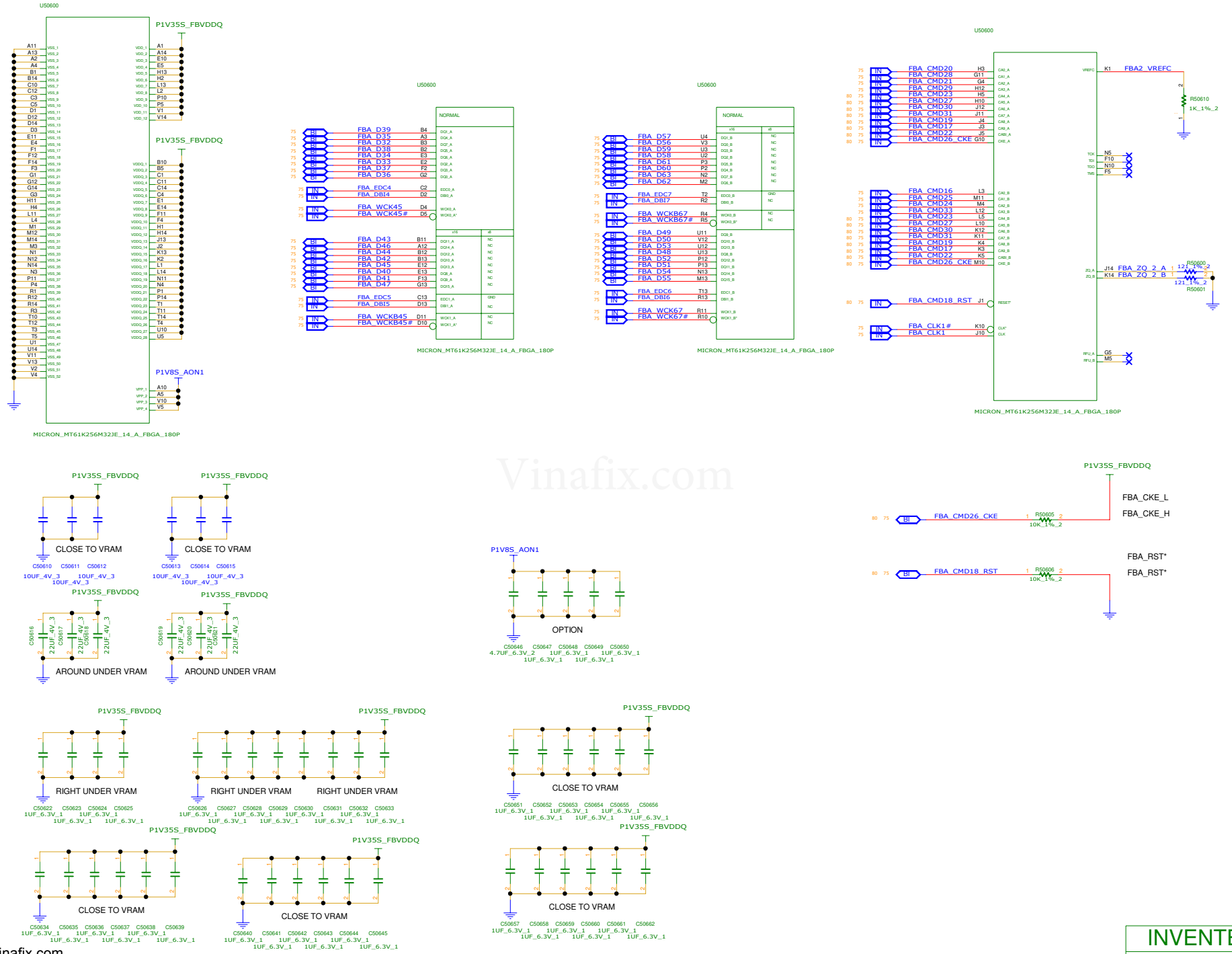
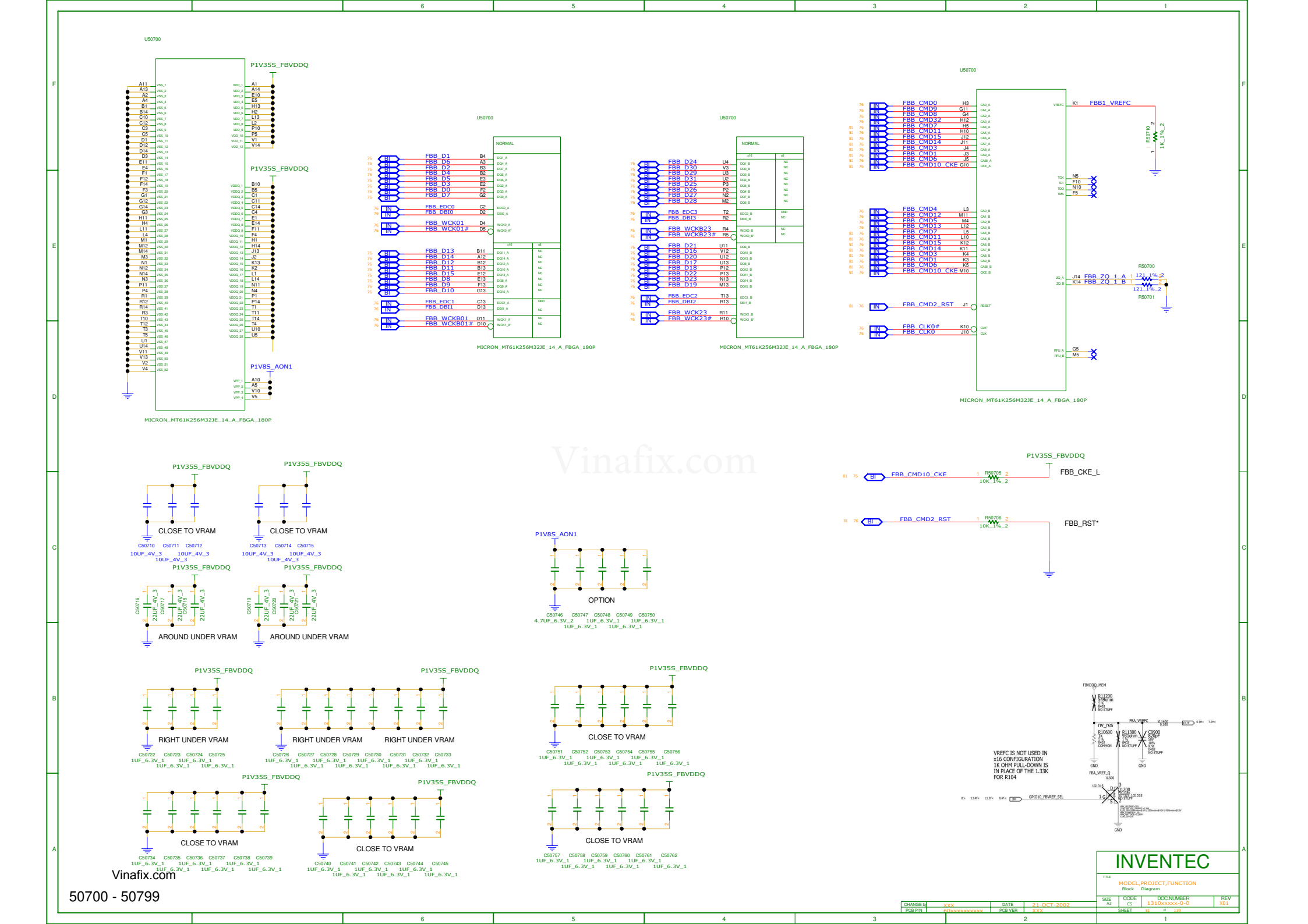
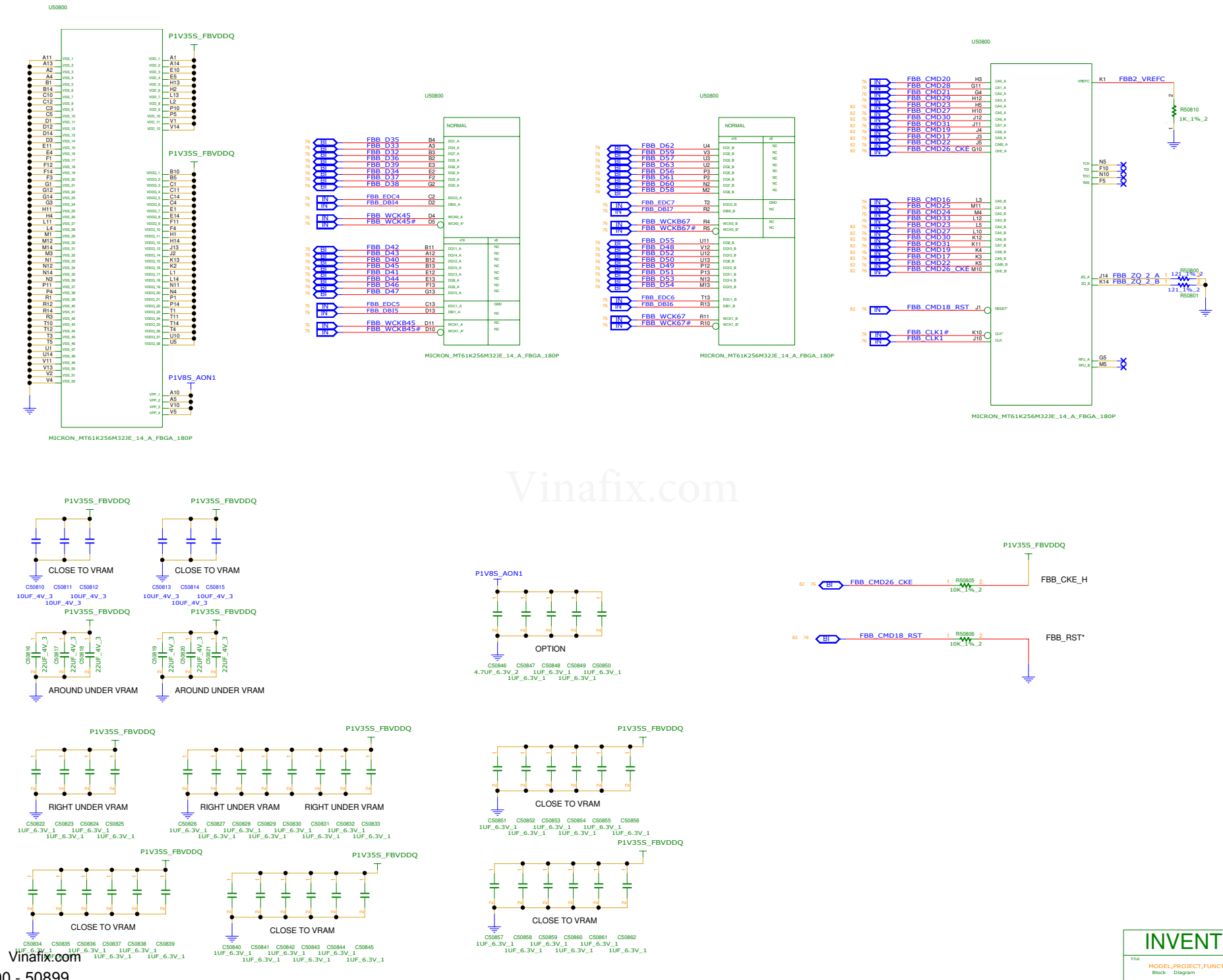


50600 - 50699



50700 - 50799



50800 - 50899

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Block Diagram

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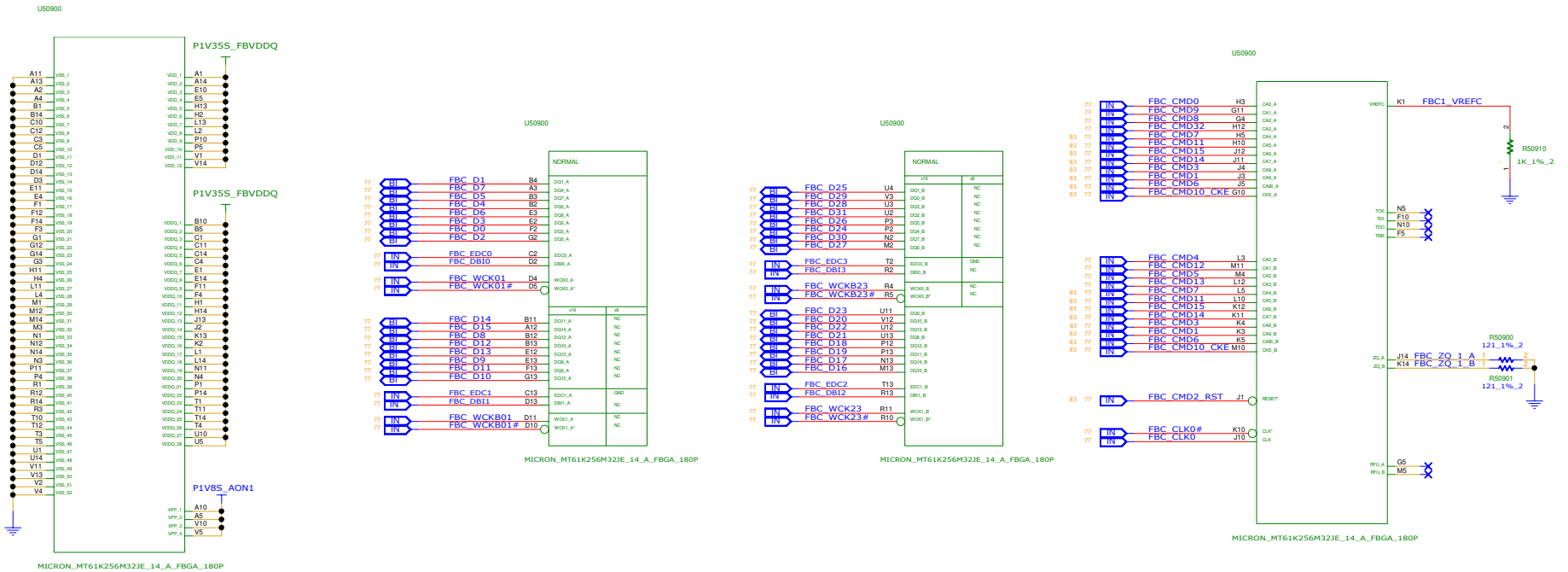
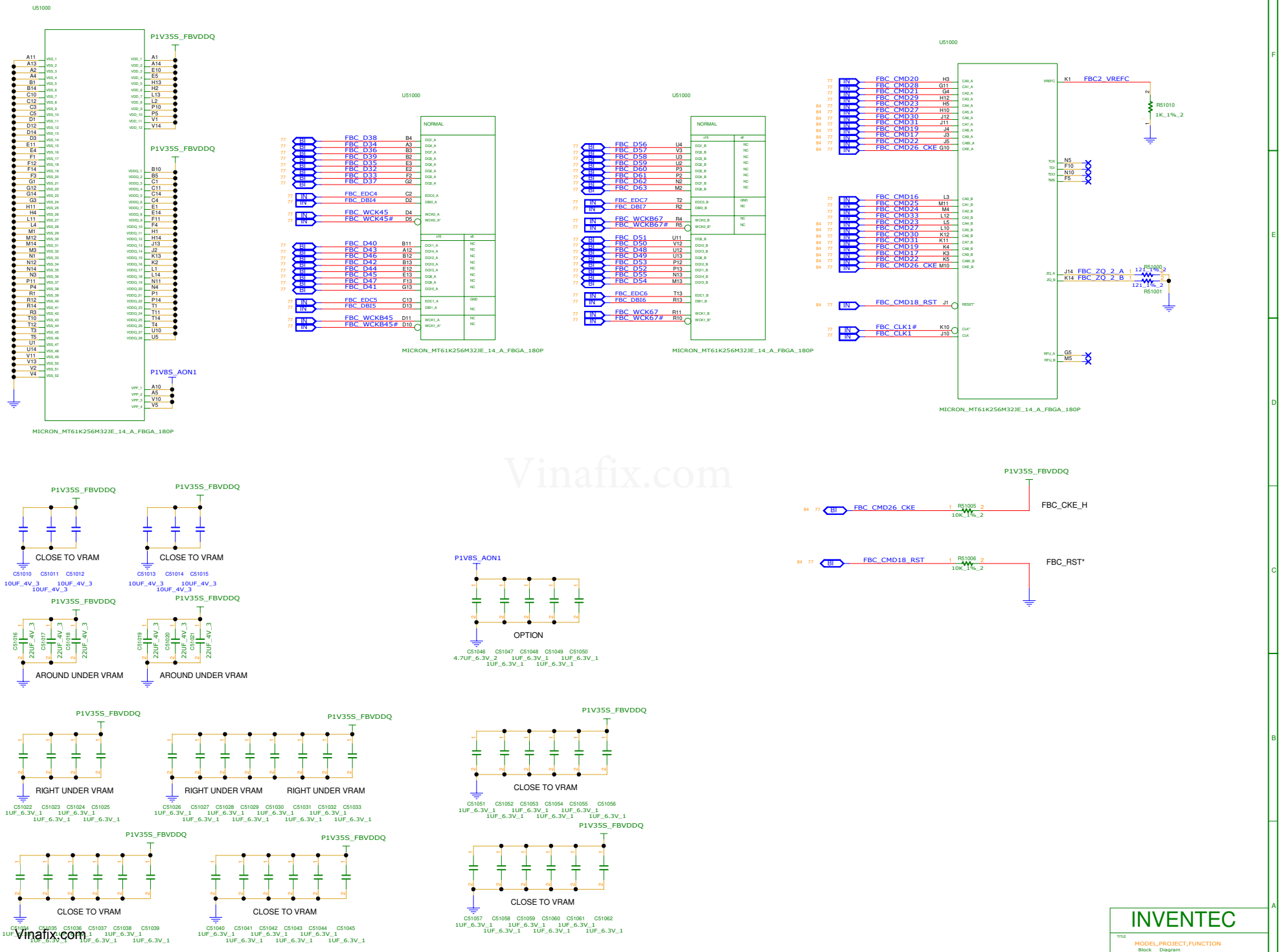


50900 - 50999


U51000
P1V35S_FBVDDQ
P1V8S_AON1
MICRON_MT61K256M32JE_14_A_FBGA_180P
FBC_D38
FBC_D34
FBC_D36
FBC_D39
FBC_D35
FBC_D32
FBC_D33
FBC_D37
FBC_EDC4
FBC_DBI4
FBC_WCK45
FBC_WCK45#
FBC_D40
FBC_D43
FBC_D46
FBC_D42
FBC_D44
FBC_D45
FBC_D47
FBC_D41
FBC_EDC5
FBC_DBI5
FBC_WCKB45
FBC_WCKB45#
FBC_D56
FBC_D57
FBC_D58
FBC_D59
FBC_D60
FBC_D61
FBC_D62
FBC_D63
FBC_EDC7
FBC_DBI7
FBC_WCKB67
FBC_WCKB67#
FBC_D51
FBC_D50
FBC_D48
FBC_D49
FBC_D53
FBC_D52
FBC_D55
FBC_D54
FBC_EDC6
FBC_DBI6
FBC_WCK67
FBC_WCK67#
FBC_CMD20
FBC_CMD28
FBC_CMD21
FBC_CMD29
FBC_CMD23
FBC_CMD27
FBC_CMD30
FBC_CMD31
FBC_CMD19
FBC_CMD17
FBC_CMD22
FBC_CMD26_CKE
FBC_CMD16
FBC_CMD25
FBC_CMD24
FBC_CMD33
FBC_CMD23
FBC_CMD27
FBC_CMD30
FBC_CMD31
FBC_CMD19
FBC_CMD17
FBC_CMD22
FBC_CMD26_CKE
FBC_CMD18_RST
FBC_CLK1#
FBC_CLK1
FBC2_VREFC
R51010
1K_1%_2
R51000
121_1%_2
R51001
FBC_ZQ_2_A
FBC_ZQ_2_B
CLOSE TO VRAM
AROUND UNDER VRAM
RIGHT UNDER VRAM
OPTION
FBC_CKE_H
FBC_RST*
INVENTEC
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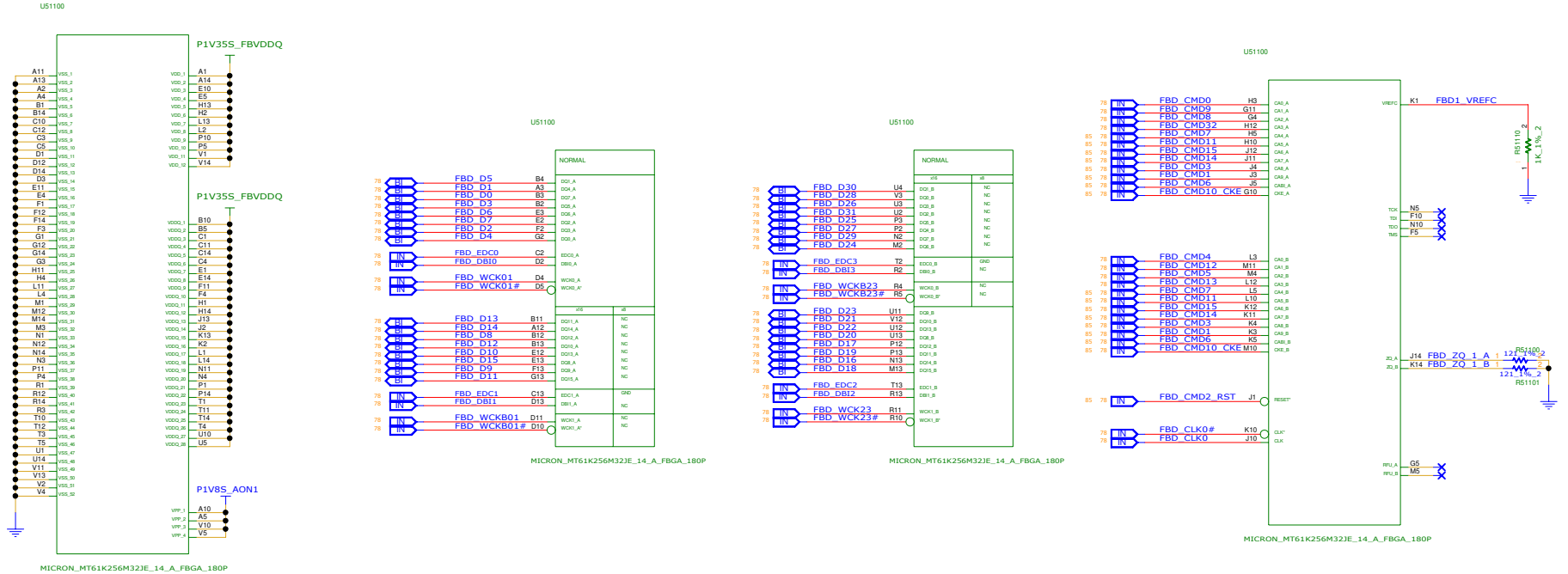
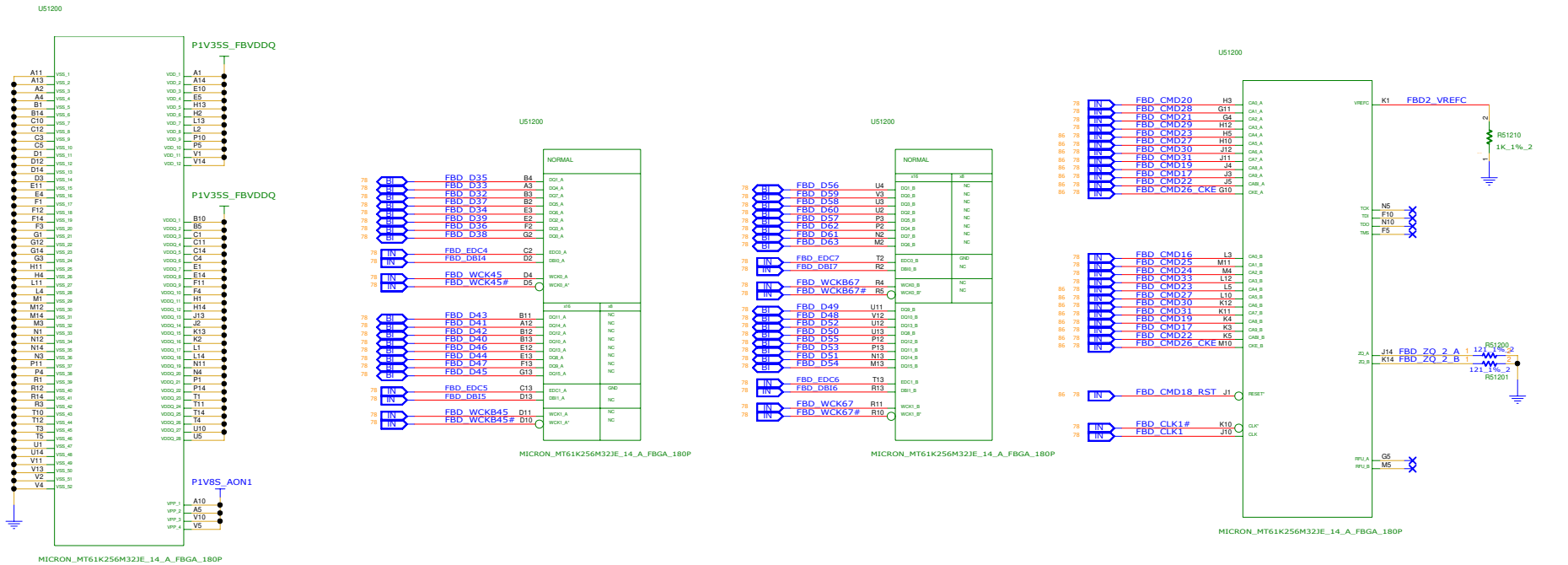
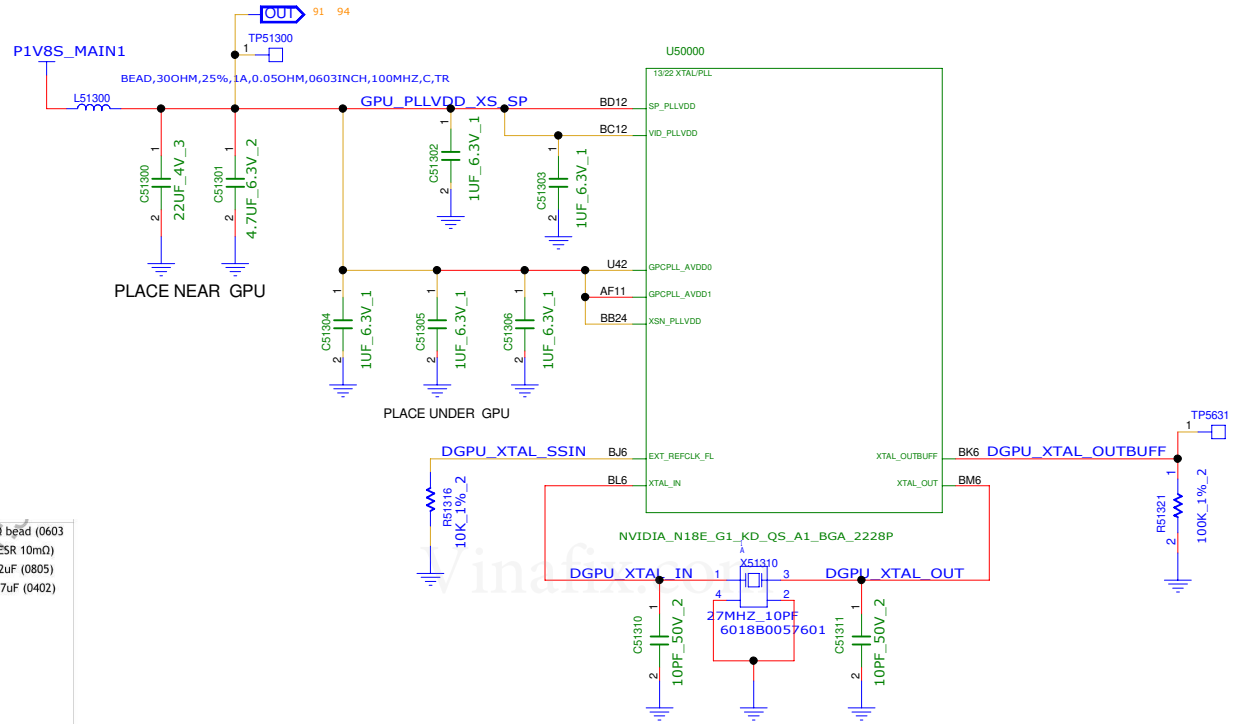


51100 - 51199



51200 - 51299

27 MHZ XTAL



CL=2*10-(5+3)=12

$CL\_trim = 2 \times CLoad - (Cstray + Ci)$

Where:

- C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
- C_{stray} is ~ 3pF (Stray capacitance of XTAL pads and any significant trace routing)
- C_i is pin capacitance (5 pF)

Typical CL_trim = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10mΩ) 1 x 22uF (0805) 1 x 4.7uF (0402)
IFPCD_PLLVDD	1			
IFPEF_PLLVDD	1		Alternate solution: 3 x 1.0uF (0201W X6S)	
GPCPLL_AVDDx XSN_PLLVDD	3		3 x 0.47uF (0201W X6S) Alternate solution: 3 x 1.0uF (0201W X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	

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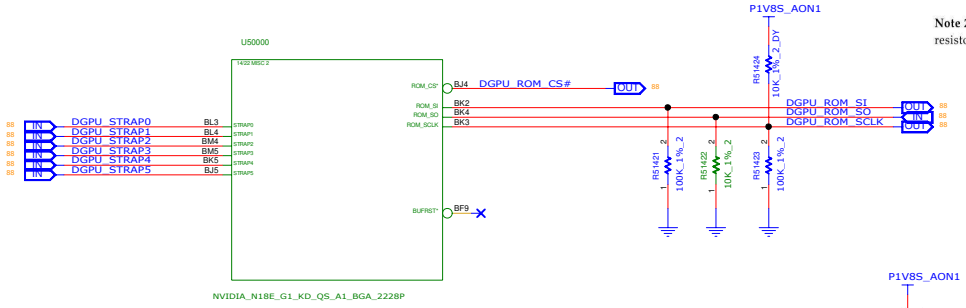
GPU VBIOS, EXTERNAL STRAPS

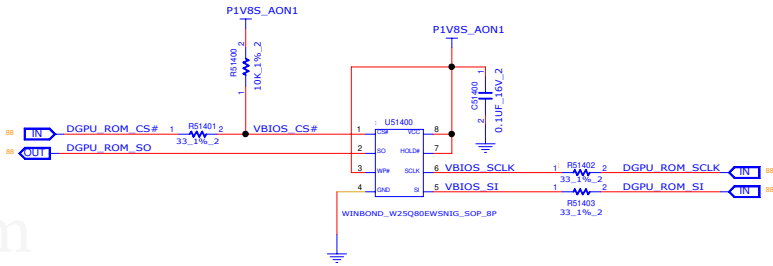
Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.





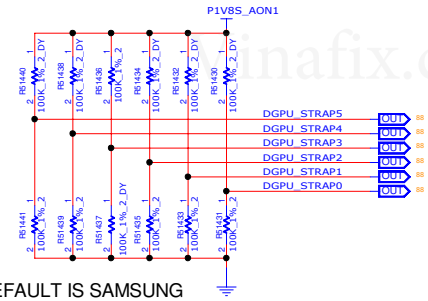


Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	M	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1
H	L	M				
H	M	L				
H	M	H				
H	H	M				
L	M	M				
M	L	M				
M	M	L				
M	M	H				
M	H	M				
H	M	M				
M	M	M				

Reserved

DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14
6019B1847601
STRAP 0X0=000
SAMSUNG:R51431 STUFF
R51430 NOT STUFF

MICRON MT61K256M32JE-14:A
6019B1847701
STRAP 0X1=001
MICRON :R51430 STUFF
R51431 NOT STUFF

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[1]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

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GPU GPIO

Table 7-1 Thermal Specifications

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
Thermal Resistance (Junction to Case, R_{JC})	0.014	0.017	0.017	TBD	°C/W
Thermal Resistance (Junction to PCB Board, R_{JB})	0.64	0.96	0.96	TBD	°C/W
GPU Shutdown Temperature (OVERT) [1]	99	99	99	TBD	°C
GPU Slowdown Temperature (THERM_ALERT) [2]	94	94	94	TBD	°C

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
GPU Maximum Operating Temperature [3]	89	89	89	TBD	°C
GPU Target Temperature	87 (Default) 75 (Min)	87 (Default) 75 (Min)	87 (Default) 75 (Min)	TBD	°C

Notes:
1. OVERT results in an 87.5% (±8) hardware clock slowdown.
2. THERM_ALERT results in a 50% (±2) hardware clock slowdown.
3. The GPU maximum operating temperature is the maximum GPU temperature at which the GPU is guaranteed to operate at the target performance (base clocks) under the total board power level.

OVERT#
3.3V LEVEL

3.3V LEVEL OVERHEAT TO EC

EC

HPD PULL UP

GPIO PULL UP

GPIO PULL DOWN

GC6_FB_EN
LEVEL SHIFTER

1.8V LEVEL

3.3V LEVEL

GC6_FB_EN
LEVEL SHIFTER

1.8V LEVEL

3.3V LEVEL

NVIDIA_N18E_G1_KD_QS_A1_BGA_2228P

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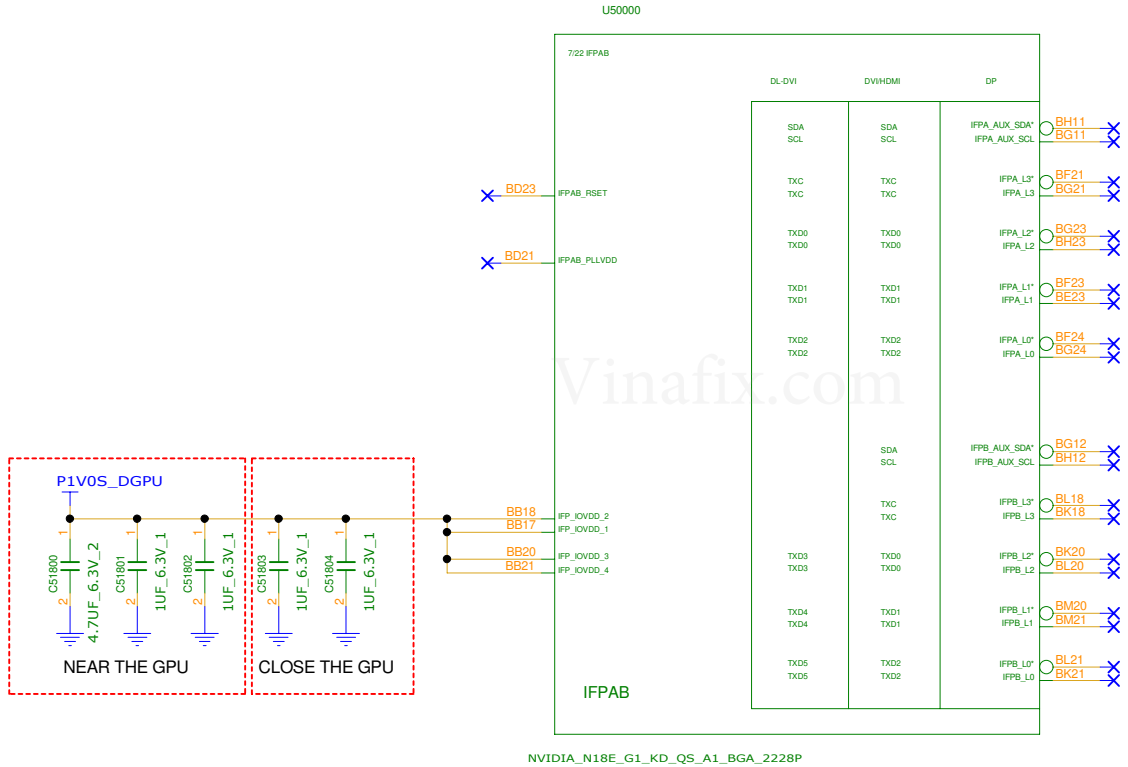

51800 - 51899

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A3	CS	1310xxxxx-0-0	X01

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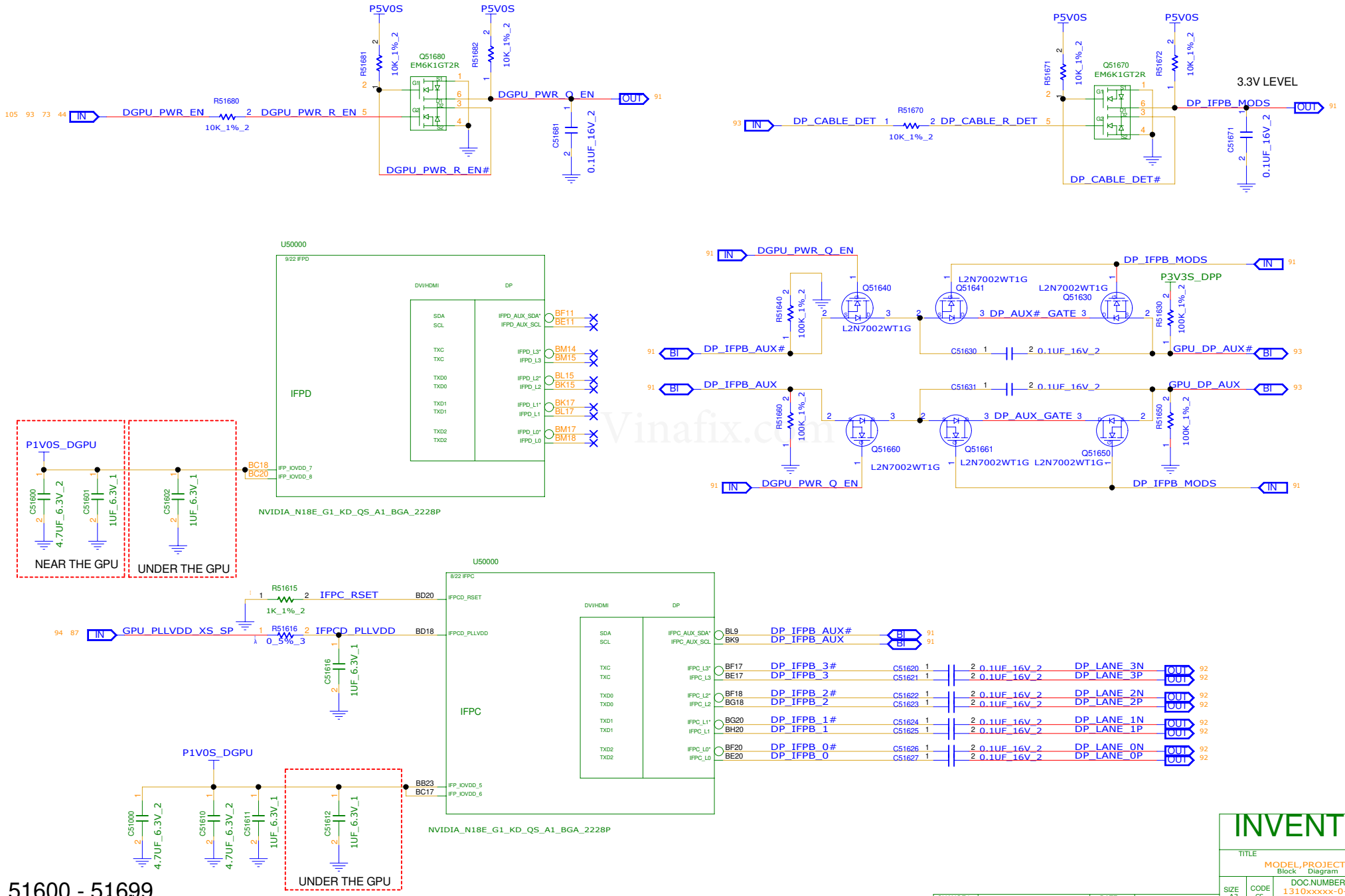

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
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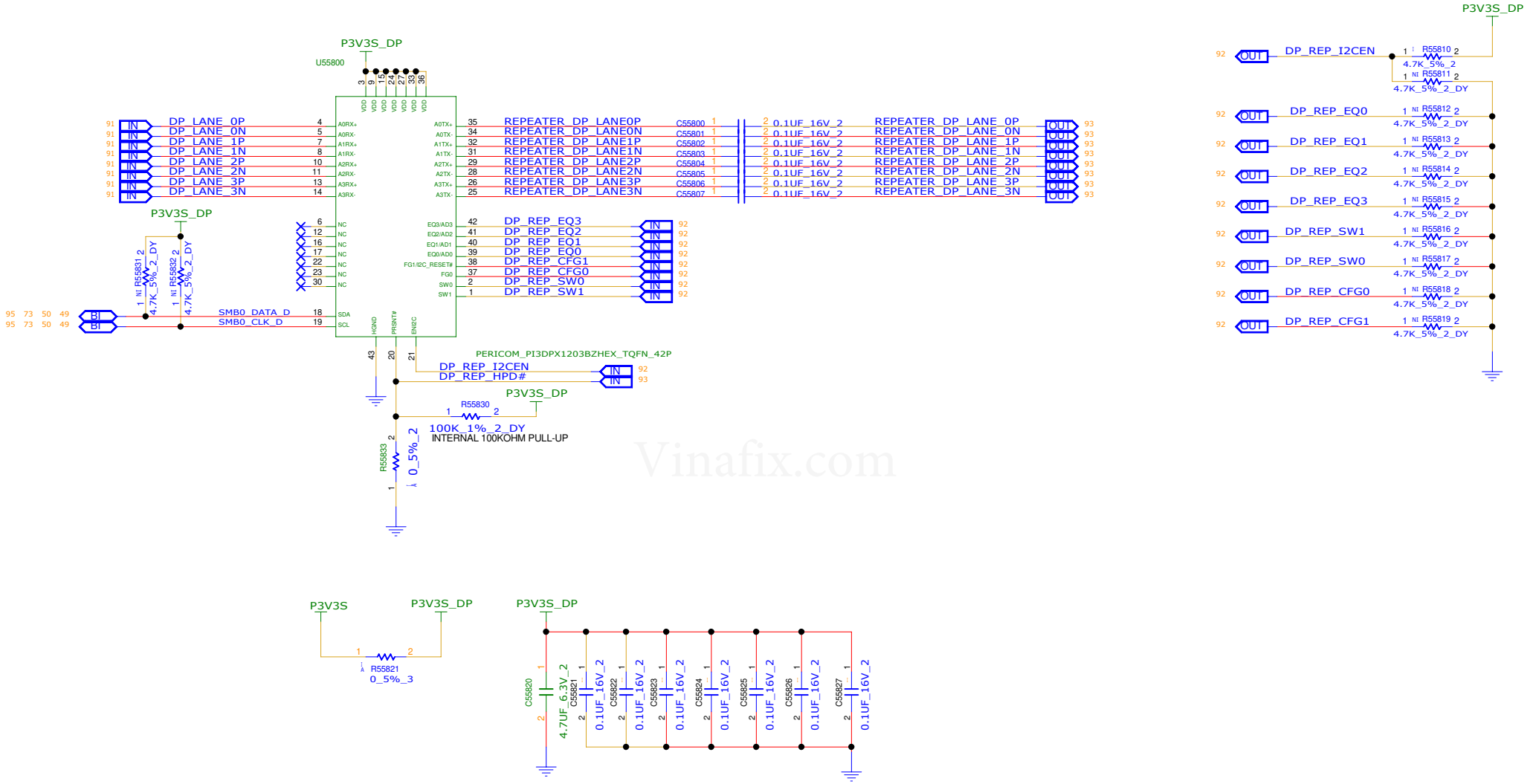
DP REDRIVER



55800 - 55999 56000 - 56199

CHANGE by	XXX	DATE	21-OCT-2002
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INVENTEC

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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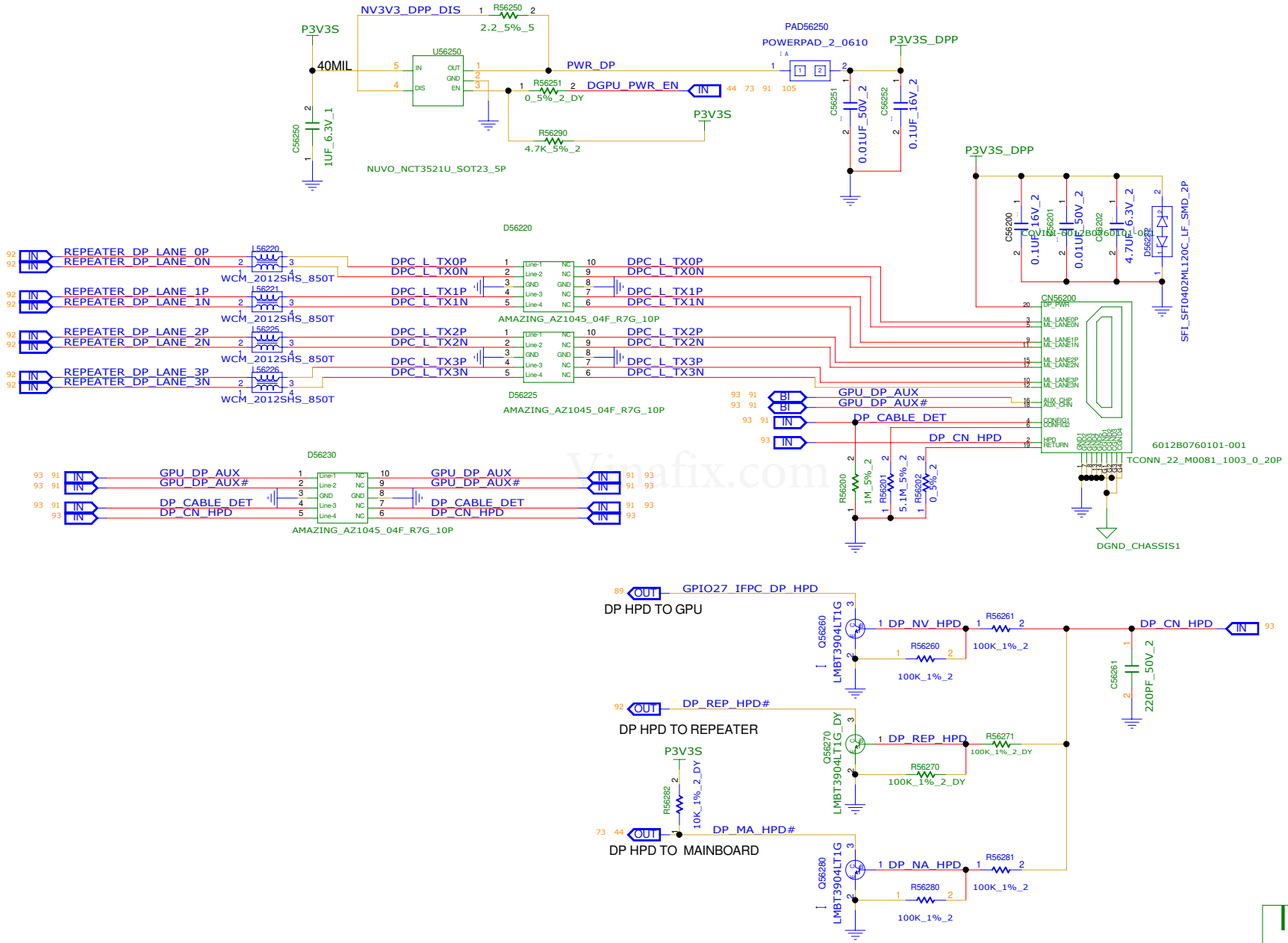

INVENTEC

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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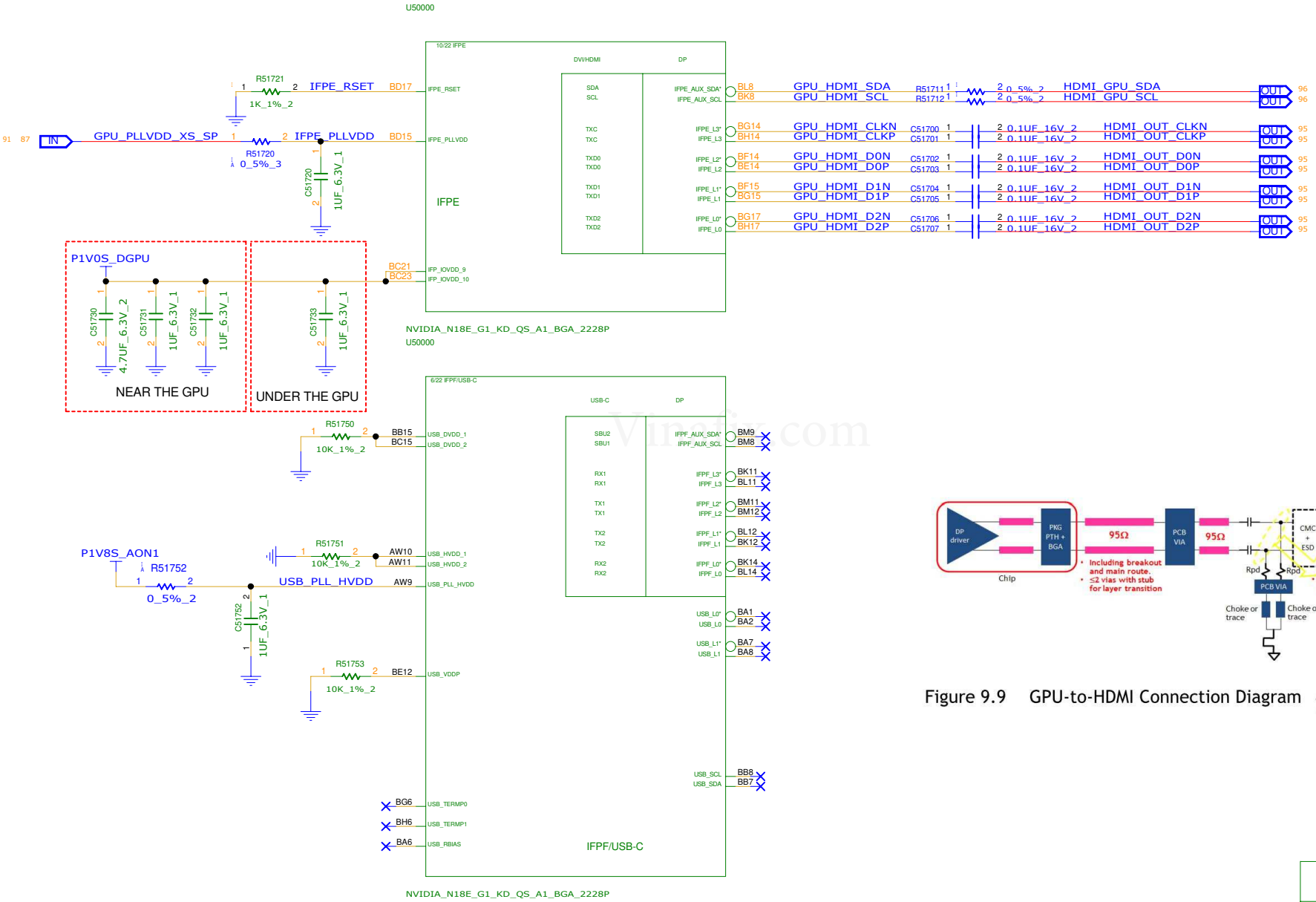

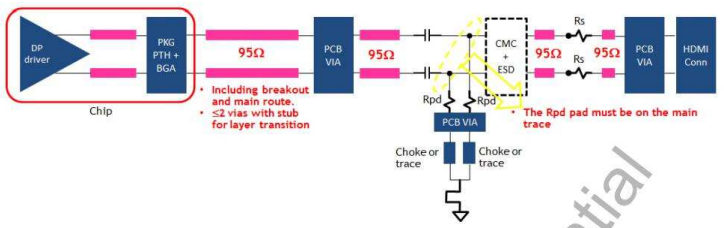

Figure 9.9 GPU-to-HDMI Connection Diagram

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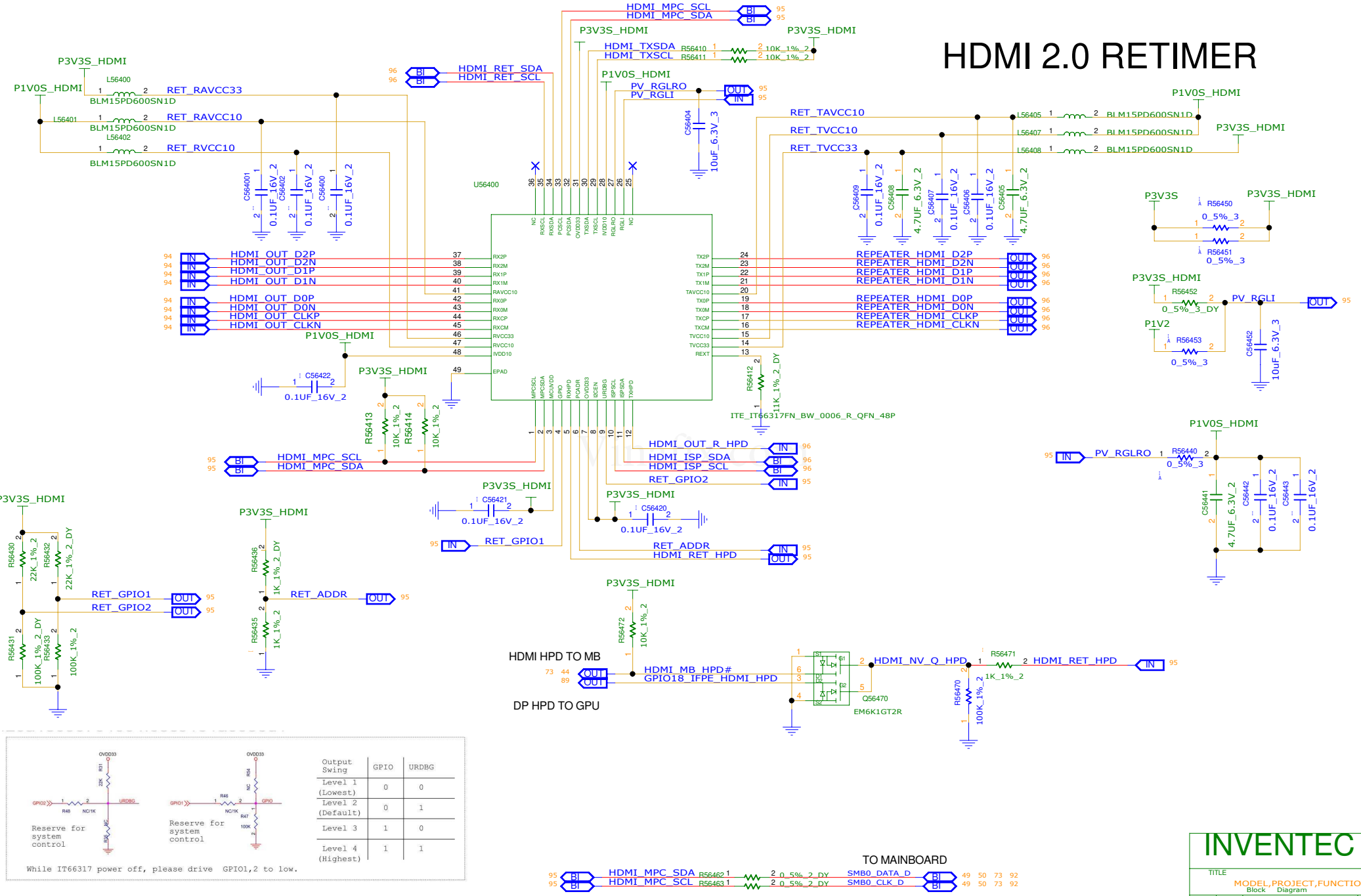
HDMI 2.0 RETIMER



Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

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A3	CS	1310xxxxx-0-0	X01

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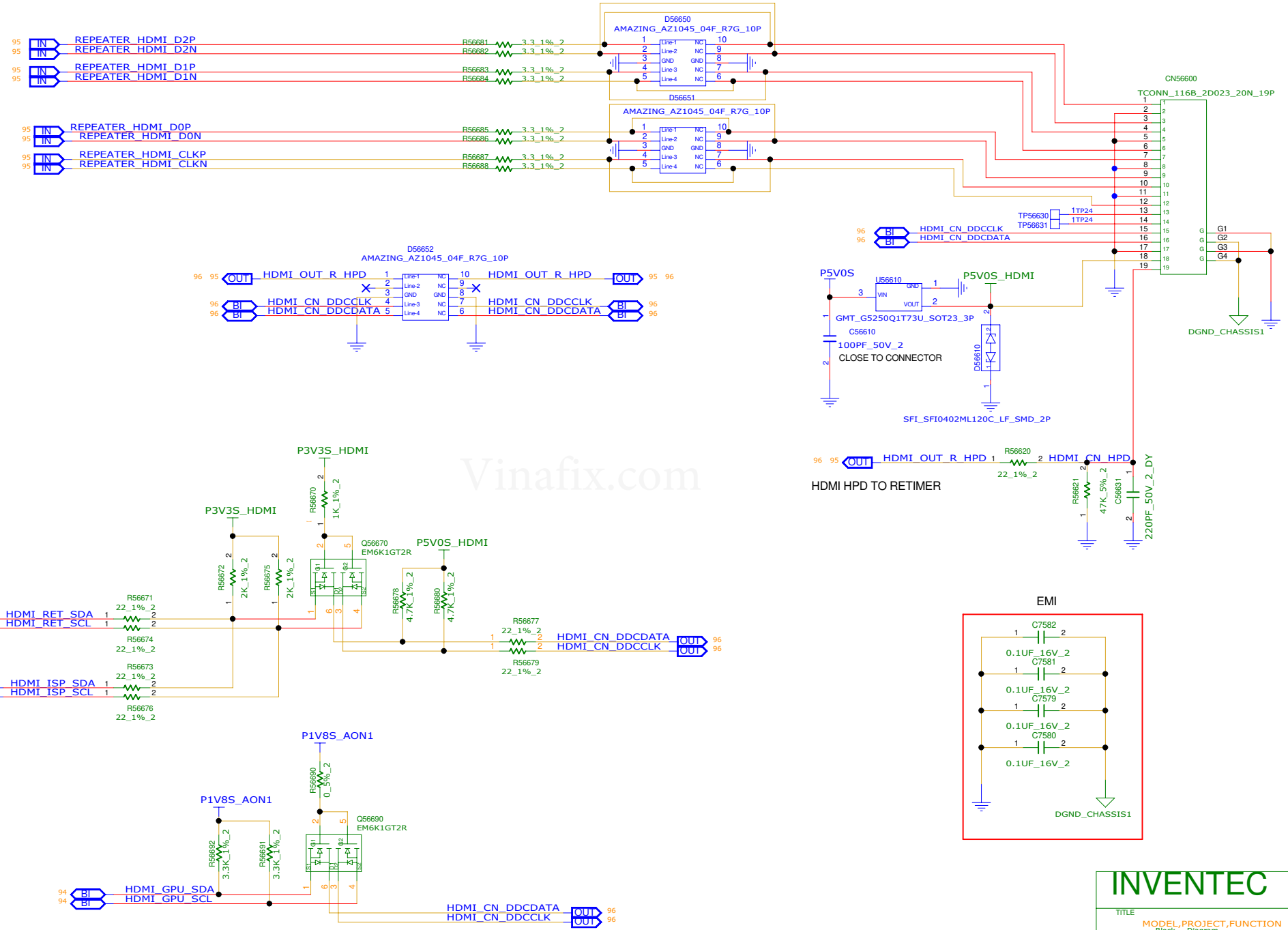
56400 - 56599



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TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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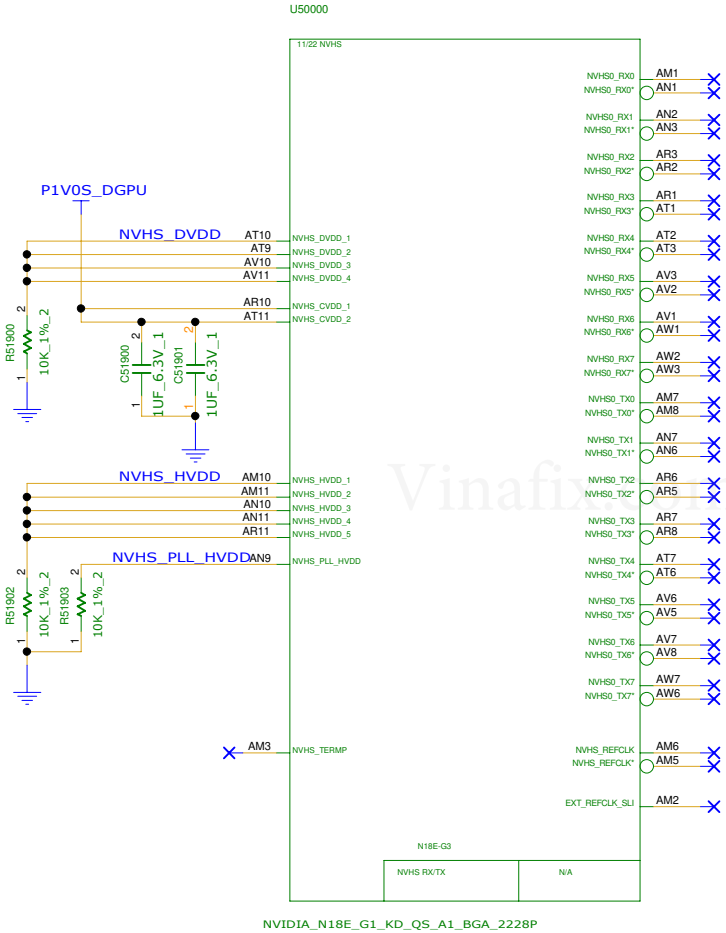

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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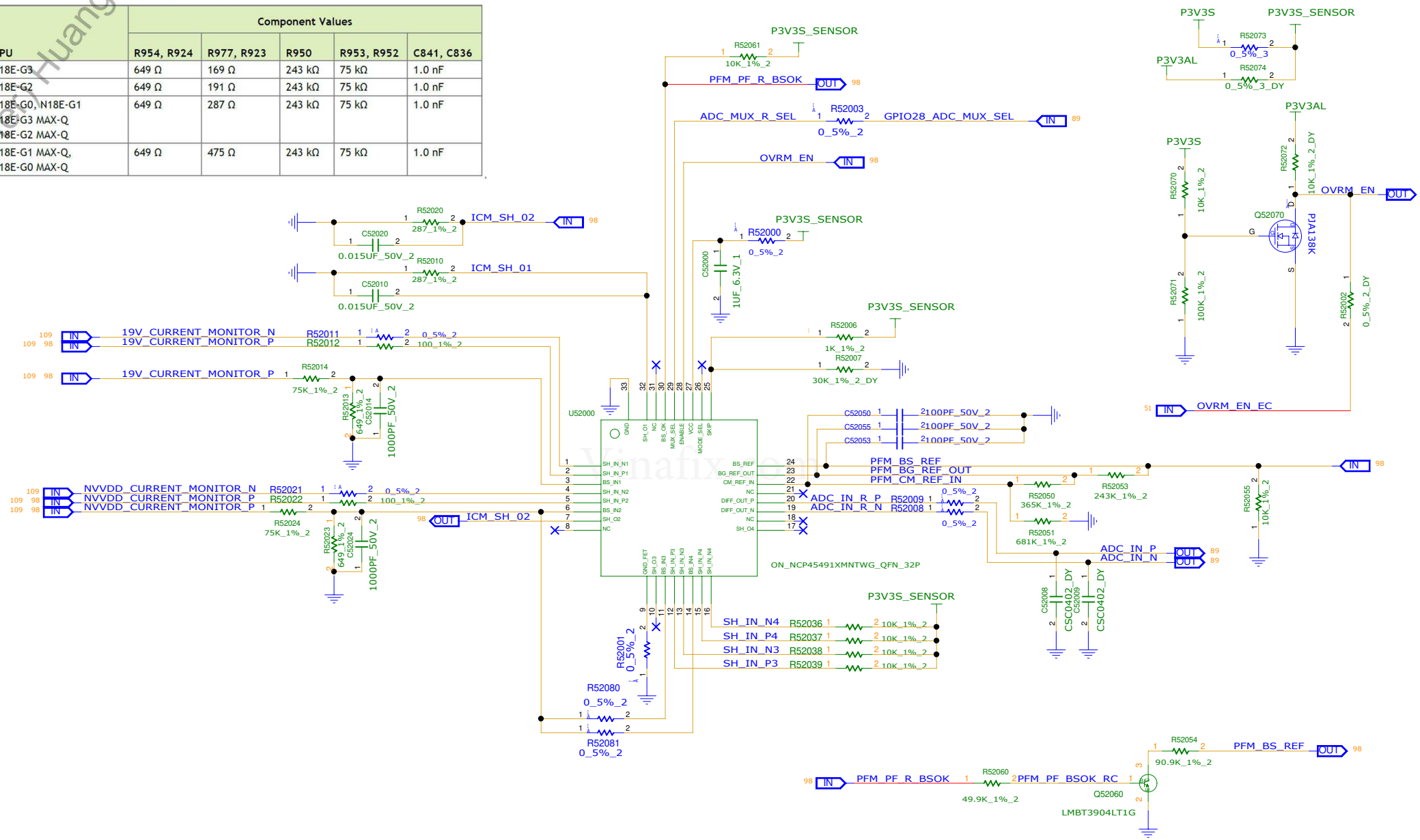
Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G2	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G0, N18E-G1 N18E-G3 MAX-Q N18E-G2 MAX-Q	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G1 MAX-Q, N18E-G0 MAX-Q	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF



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A3	CS	1310xxxxx-0-0	X01

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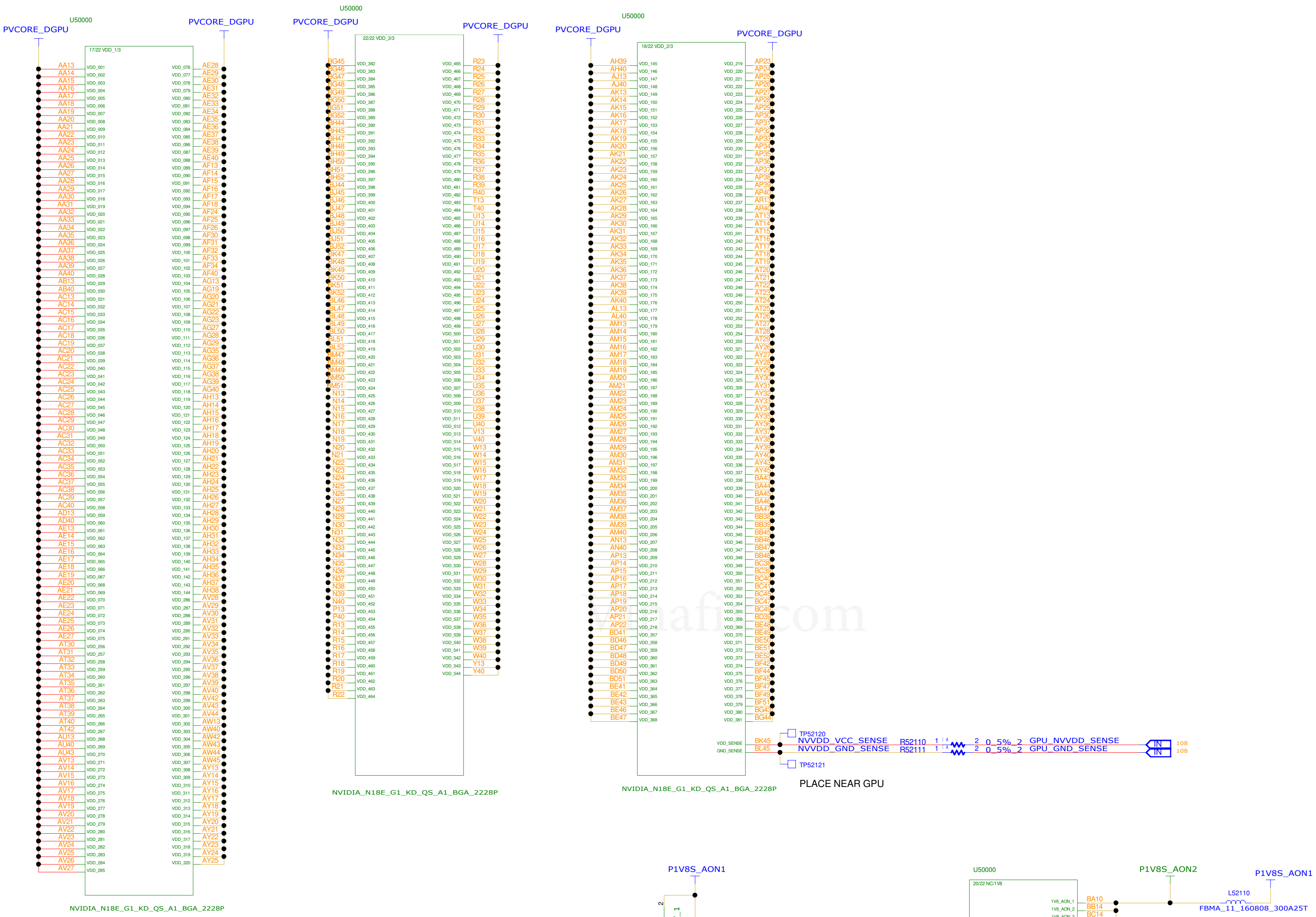


The required subcircuit is shown in detail in Figure 15.6.

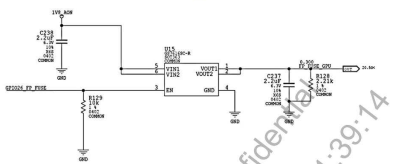
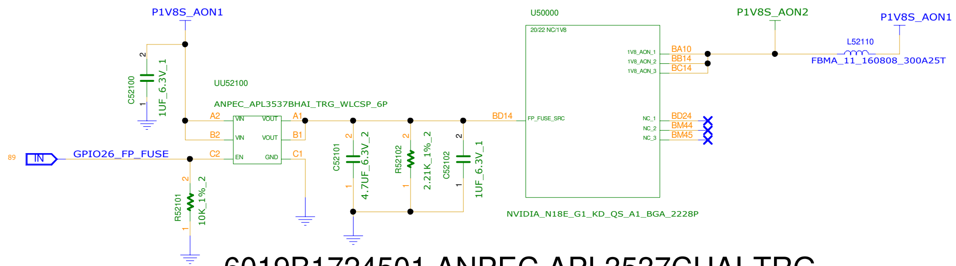


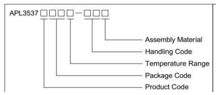
Figure 15.6 Subcircuit Schematic

In Figure 15.6, the component labeled “U15” is an active switch; devices equivalent to the GS7616SC-R are acceptable as long as they meet the following requirements:

- The active switch must be capable of driving 100mA or more.
- The timing delay from GPIO26_FP_FUSE assertion to FP_FUSE_GPU (active switch output) must be 100msec or less.
- There must be no glitch during power up or GC6/GC-OFF entry or exit.
- The FP_FUSE_GPU (output) trace width must be 0.25 mm (10 mil) or greater.

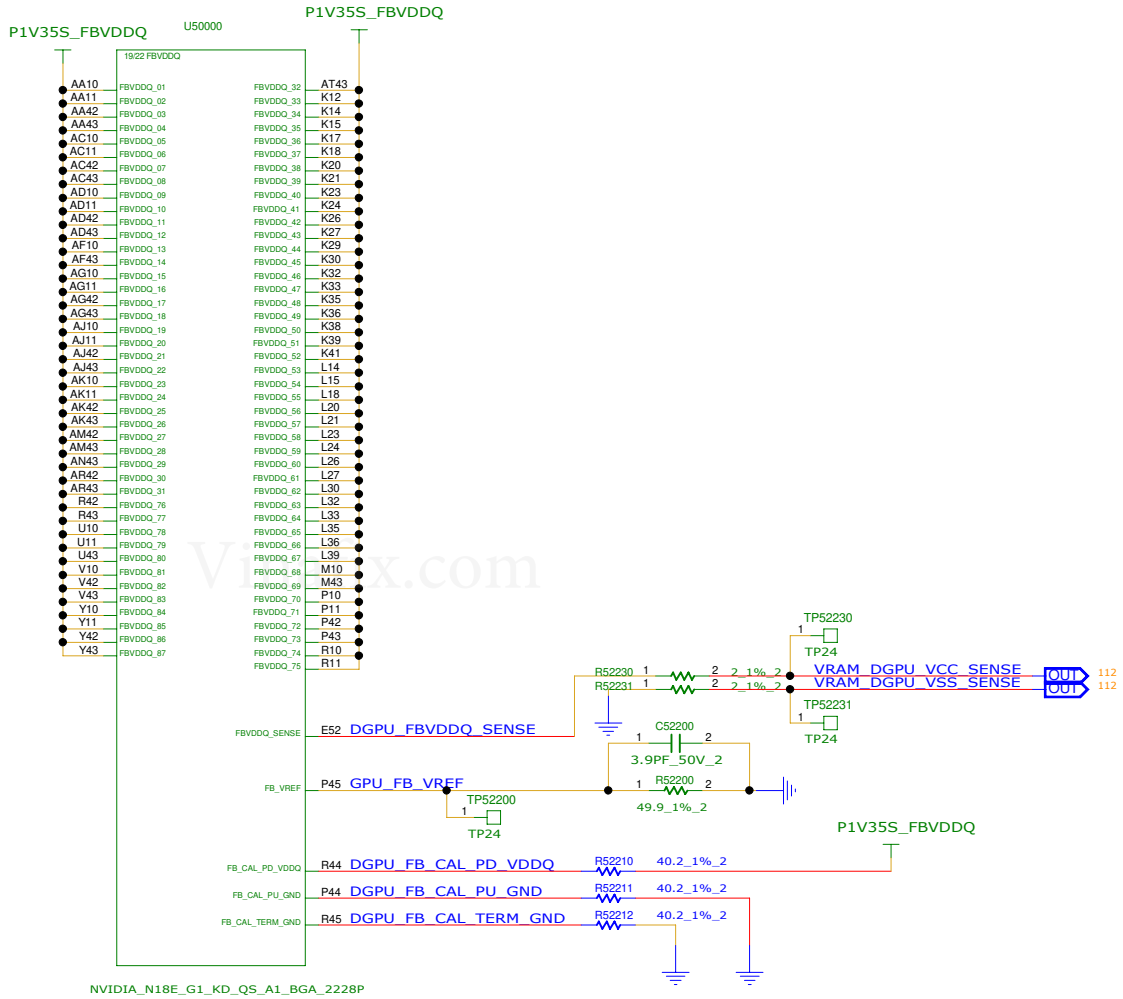


6019B1724501 ANPEC APL3537CHAI-TRG



Product Code
A : Turn On Delay 111μs B : Turn On Delay 800μs
Package Code
HA : WLCSP0.9x1.4-6
Operating Junction Temperature
I : -40 to 85 ℃
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

52100 - 52199



55600 - 55699

52200 - 52299

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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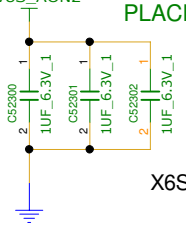
GPU 1V8_AON DECOUPLING

P1V8S_AON2

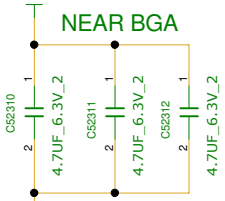
PLACE UNDER BGA



X6S OR X7R

P1V8S_AON2

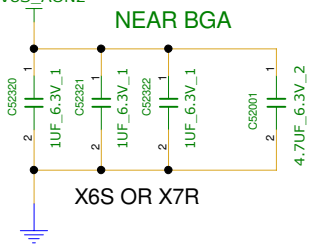
NEAR BGA



X6S OR X7R

P1V8S_AON2

NEAR BGA



X6S OR X7R

1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S) 3 x 1uF (0402 X6S) 3 x 4.7uF (0603 X6S) Alternate solution: 3 x 1.0uF (0201W X6S)

52300 - 52399

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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A3	CS	1310xxxxx-0-0	X01

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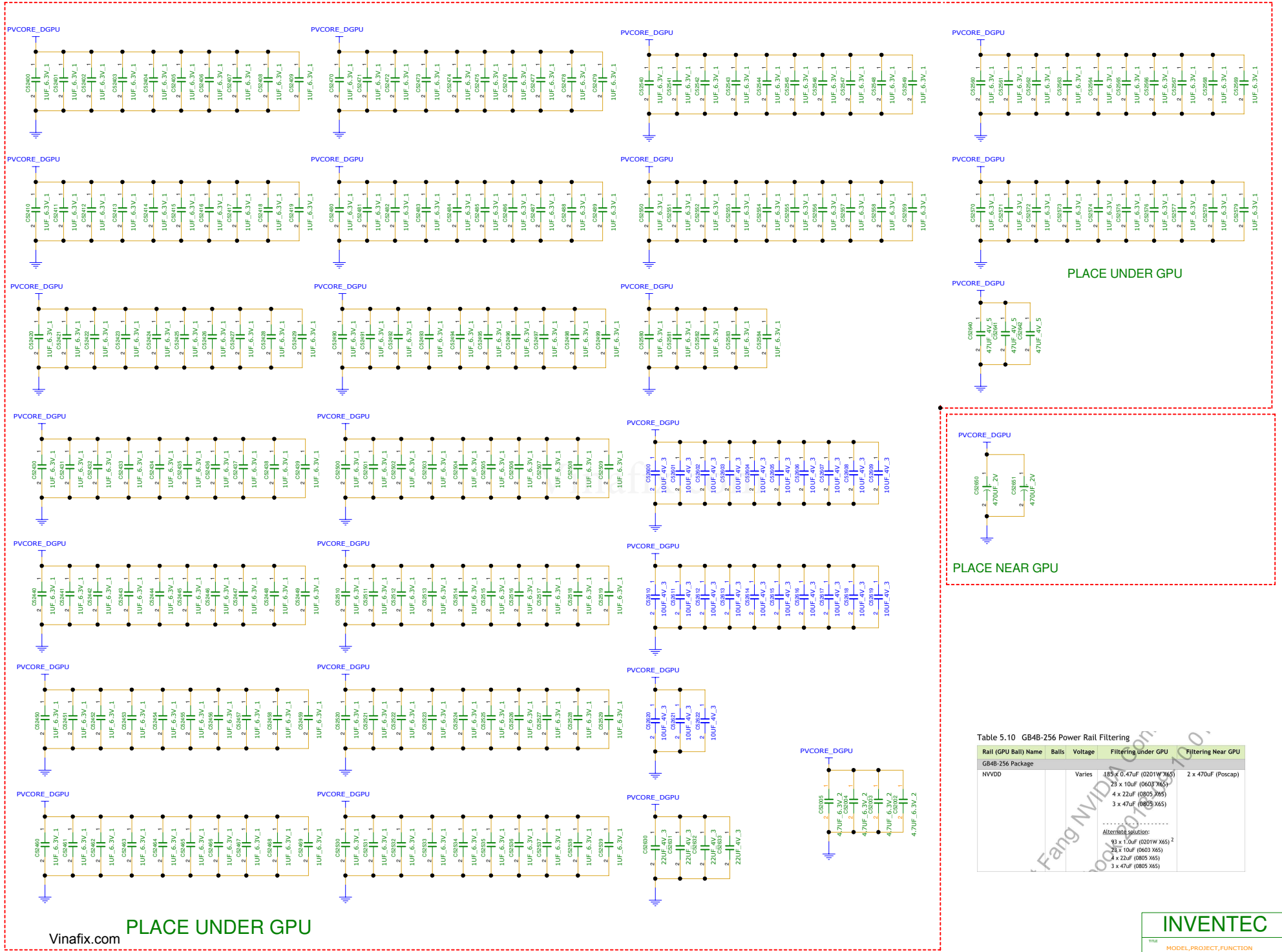

Table 5.10 GB4B-256 Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 x 0.47uF (0201W X6S) 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S) --- Alternate solution: 93 x 1.0uF (0201W X6S) [2] 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S)	2 x 470uF (Poscap)

52400 - 52999

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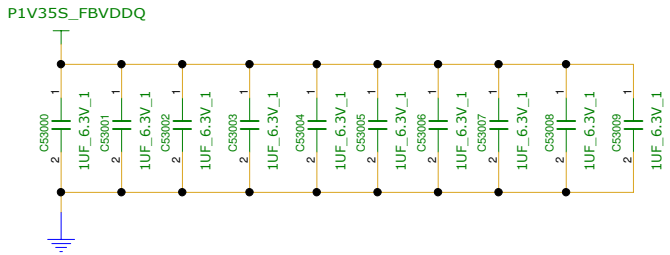
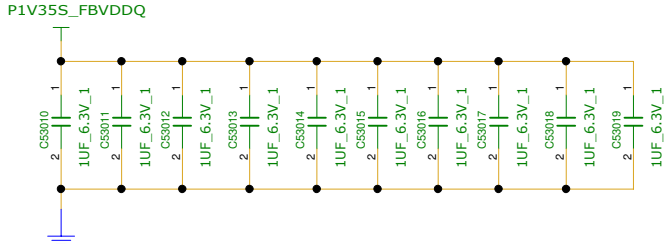
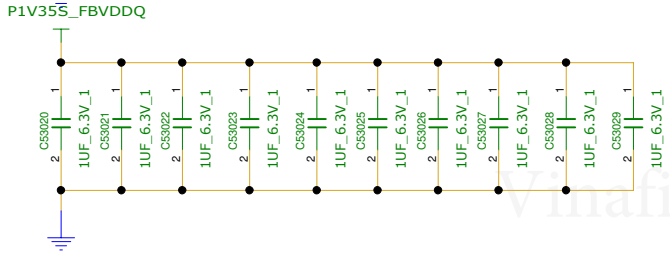
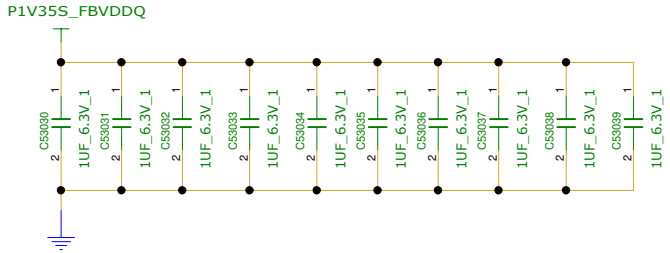
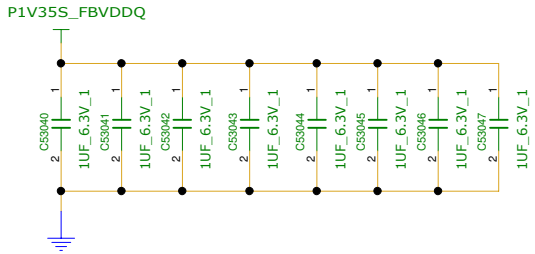


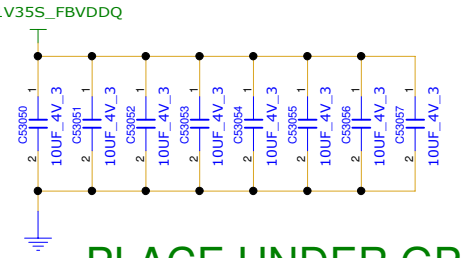




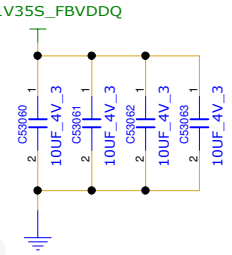




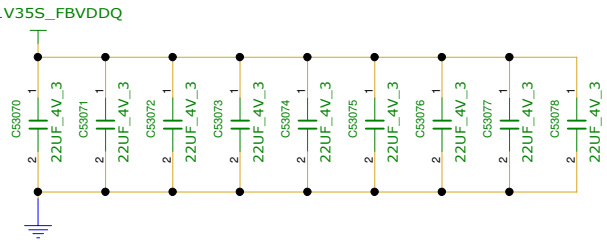
PLACE UNDER GPU



PLACE UNDER GPU



PLACE NEAR GPU



FBVDDQ (GPU side)[1]	1.25V 1.35V	48 x 0.47uF (0201W X6S) 8 x 10uF (0603 X6S) - - - - - - - - - - - - - - - - - Alternate solution: 24 x 1.0uF (0201W X6S)[2] 8 x 10uF (0603 X6S)	4 x 10uF (0603 X6S) 9 x 22uF (0603 X6S)

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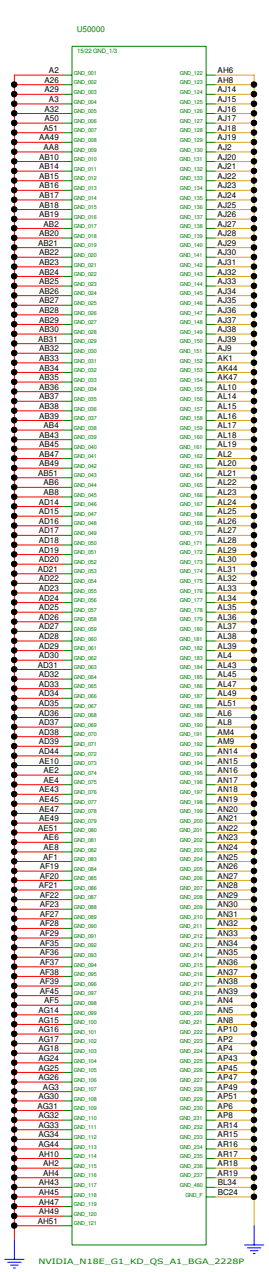
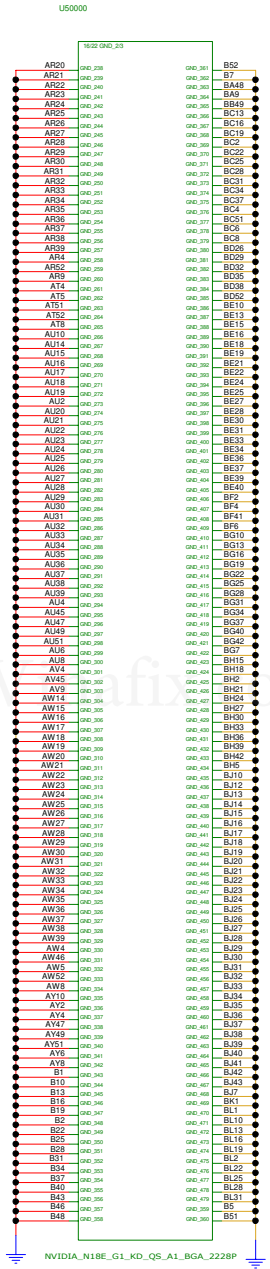
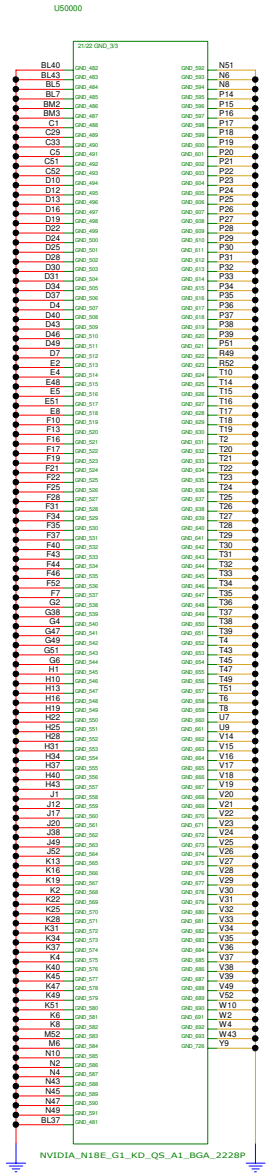
GND







53300 - 53499

INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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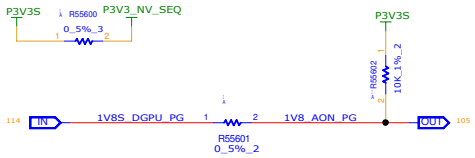
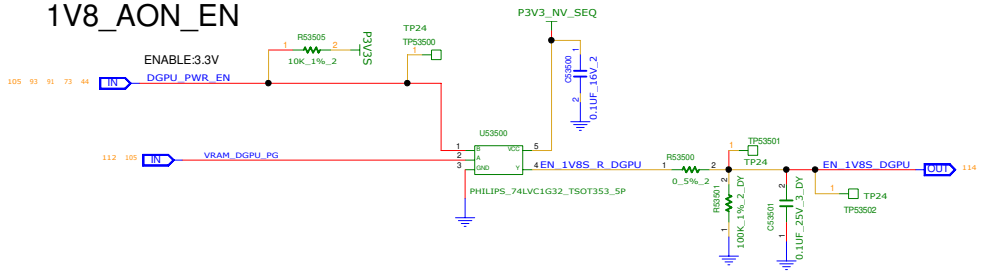
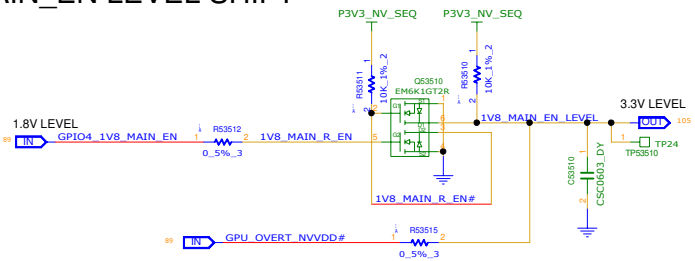


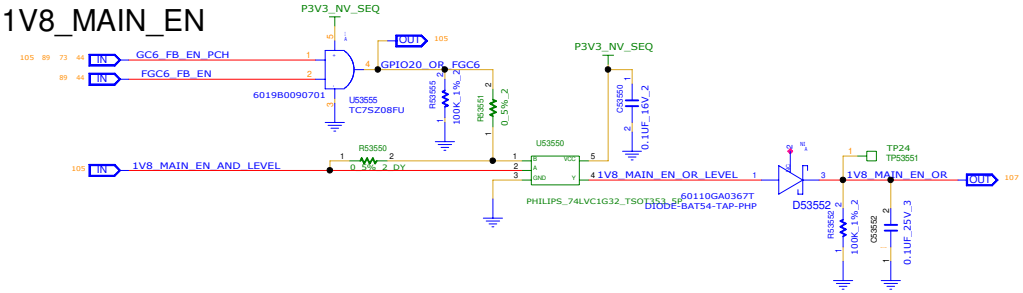
1V8_AON_EN



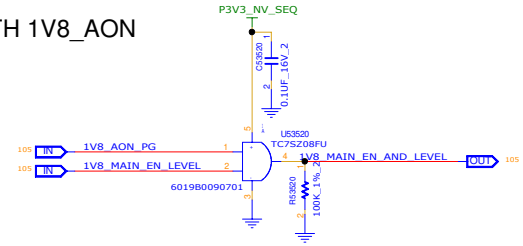
1V8_MAIN_EN LEVEL SHIFT



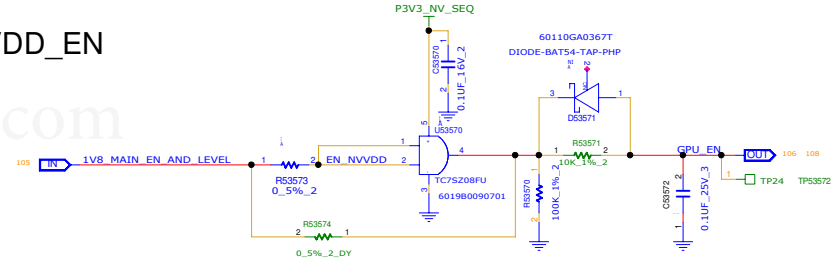
1V8_MAIN_EN



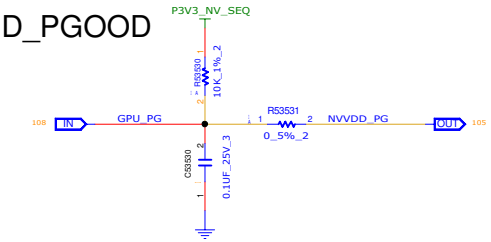
1V8_MAIN_EN AND WITH 1V8_AON



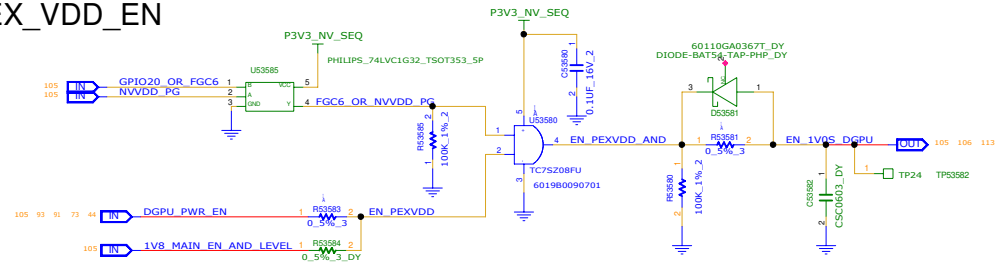
NVVDD_EN



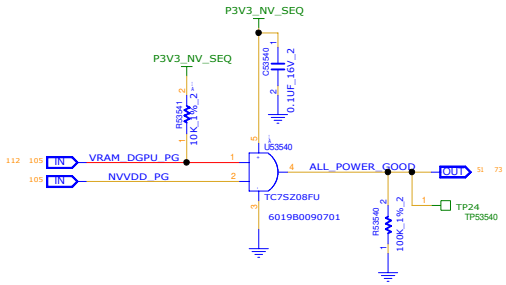
NVVDD_PGOOD



PEX_VDD_EN

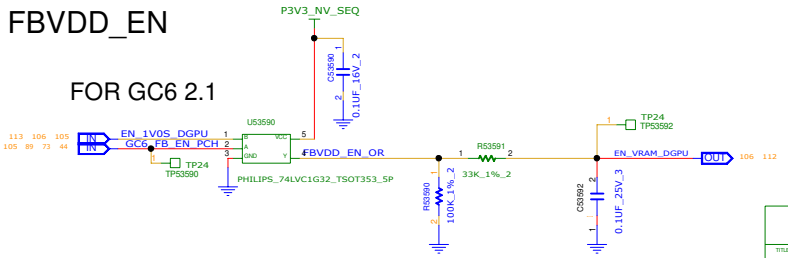


ALL POWER GOOD



FBVDD_EN

FOR GC6 2.1



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INVENTEC

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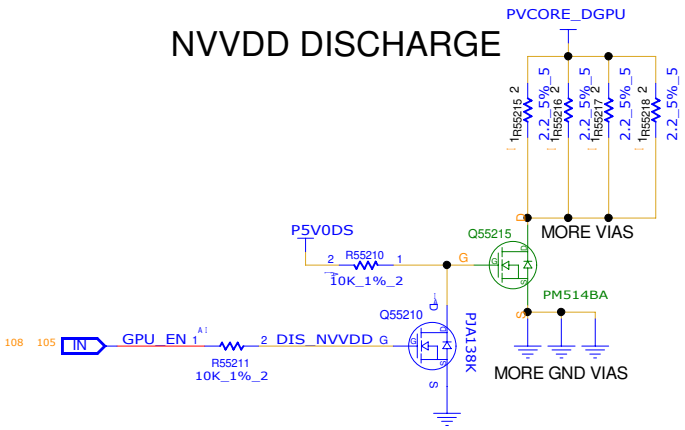
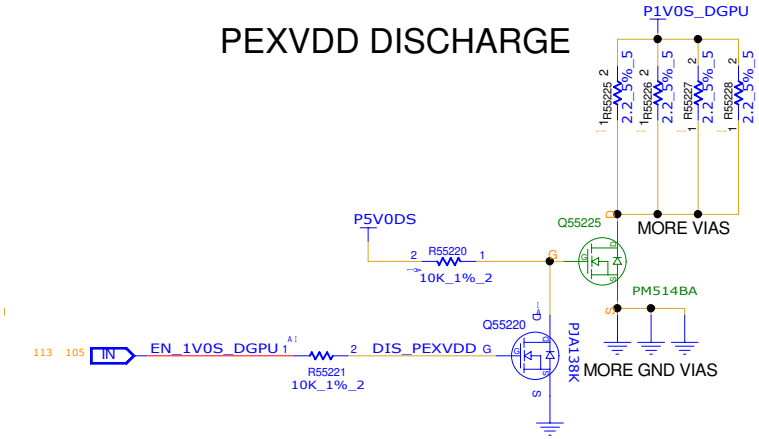
DISCHARGE CIRCUIT

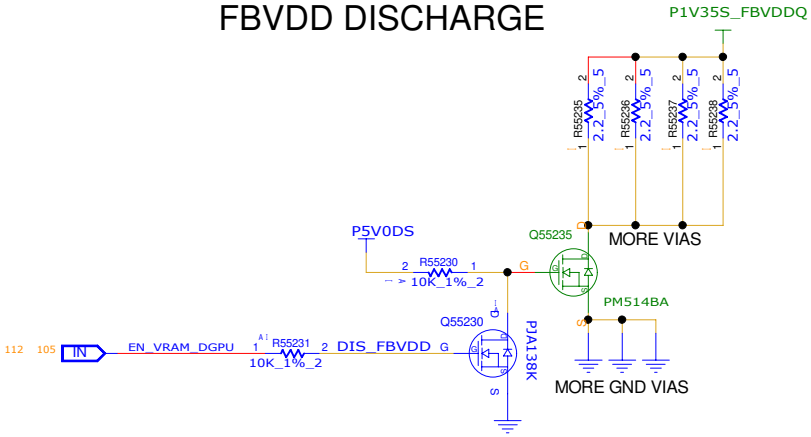
NVVDD DISCHARGE



PEXVDD DISCHARGE



FBVDD DISCHARGE



55200 - 55299

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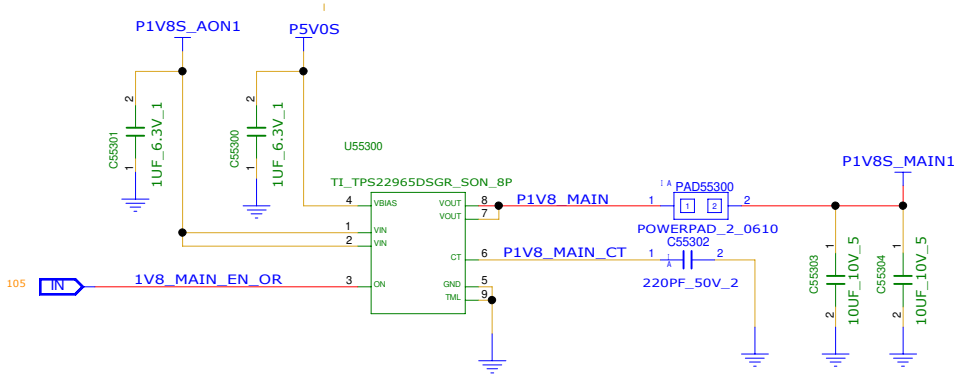
1V8_MAIN



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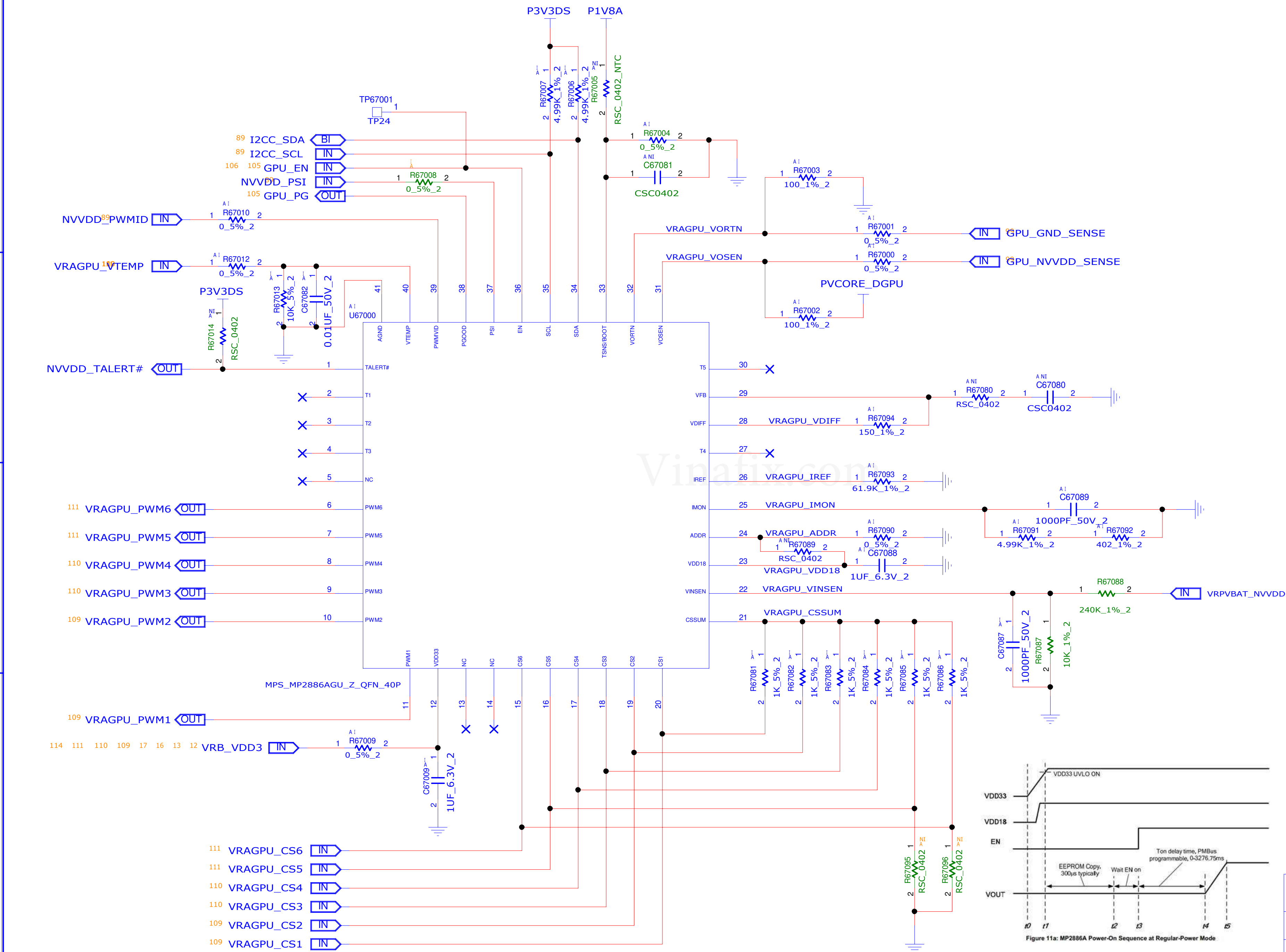
P3V3DS
P1V8A
TP67001
TP24
I2CC_SDA
I2CC_SCL
GPU_EN
NVVDD_PSI
GPU_PG
NVVDD_PWMID
VRAGPU_VTEMP
NVVDD_TALERT#
R67007 4.99K_1%_2
R67006 4.99K_1%_2
R67005 RSC_0402_NTC
R67004 0_5%_2
C67081 CSC0402
R67008 0_5%_2
R67010 0_5%_2
R67012 0_5%_2
R67013 10K_5%_2
C67082 0.01UF_50V_2
R67014 RSC_0402
U67000
MPS_MP2886AGU_Z_QFN_40P
AGND VTEMP PWMVID PGOOD PSI EN SCL SDA TSNS/BOOT VORTN VOSEN
TALERT# T1 T2 T3 NC PWM6 PWM5 PWM4 PWM3 PWM2
PWM1 VDD33 NC NC CS6 CS5 CS4 CS3 CS2 CS1
T5 VFB VDIFF T4 IREF IMON ADDR VDD18 VINSEN CSSUM
R67003 100_1%_2
VRAGPU_VORTN
VRAGPU_VOSEN
R67001 0_5%_2
R67000 0_5%_2
GPU_GND_SENSE
GPU_NVVDD_SENSE
PVCORE_DGPU
R67002 100_1%_2
R67080 RSC_0402
C67080 CSC0402
VRAGPU_VDIFF
R67094 150_1%_2
VRAGPU_IREF
R67093 61.9K_1%_2
VRAGPU_IMON
C67089 1000PF_50V_2
R67091 4.99K_1%_2
R67092 402_1%_2
VRAGPU_ADDR
R67090 0_5%_2
R67089 RSC_0402
C67088 1UF_6.3V_2
VRAGPU_VDD18
VRAGPU_VINSEN
R67088 240K_1%_2
VRPBAT_NVVDD
VRAGPU_CSSUM
C67087 1000PF_50V_2
R67087 10K_1%_2
R67081 R67082 R67083 R67084 R67085 R67086 1K_5%_2
VRAGPU_PWM6
VRAGPU_PWM5
VRAGPU_PWM4
VRAGPU_PWM3
VRAGPU_PWM2
VRAGPU_PWM1
VRB_VDD3
R67009 0_5%_2
C67009 1UF_6.3V_2
VRAGPU_CS6
VRAGPU_CS5
VRAGPU_CS4
VRAGPU_CS3
VRAGPU_CS2
VRAGPU_CS1
R67095 RSC_0402
R67096 RSC_0402
VDD33 UVLO ON
VDD33
VDD18
EN
VOUT
EEPROM Copy, 300μs typically
Wait EN on
Turn delay time, PMBus programmable, 0-3276.75ms
t0 t1 t2 t3 t4 t5
Figure 11a: MP2886A Power-On Sequence at Regular-Power Mode

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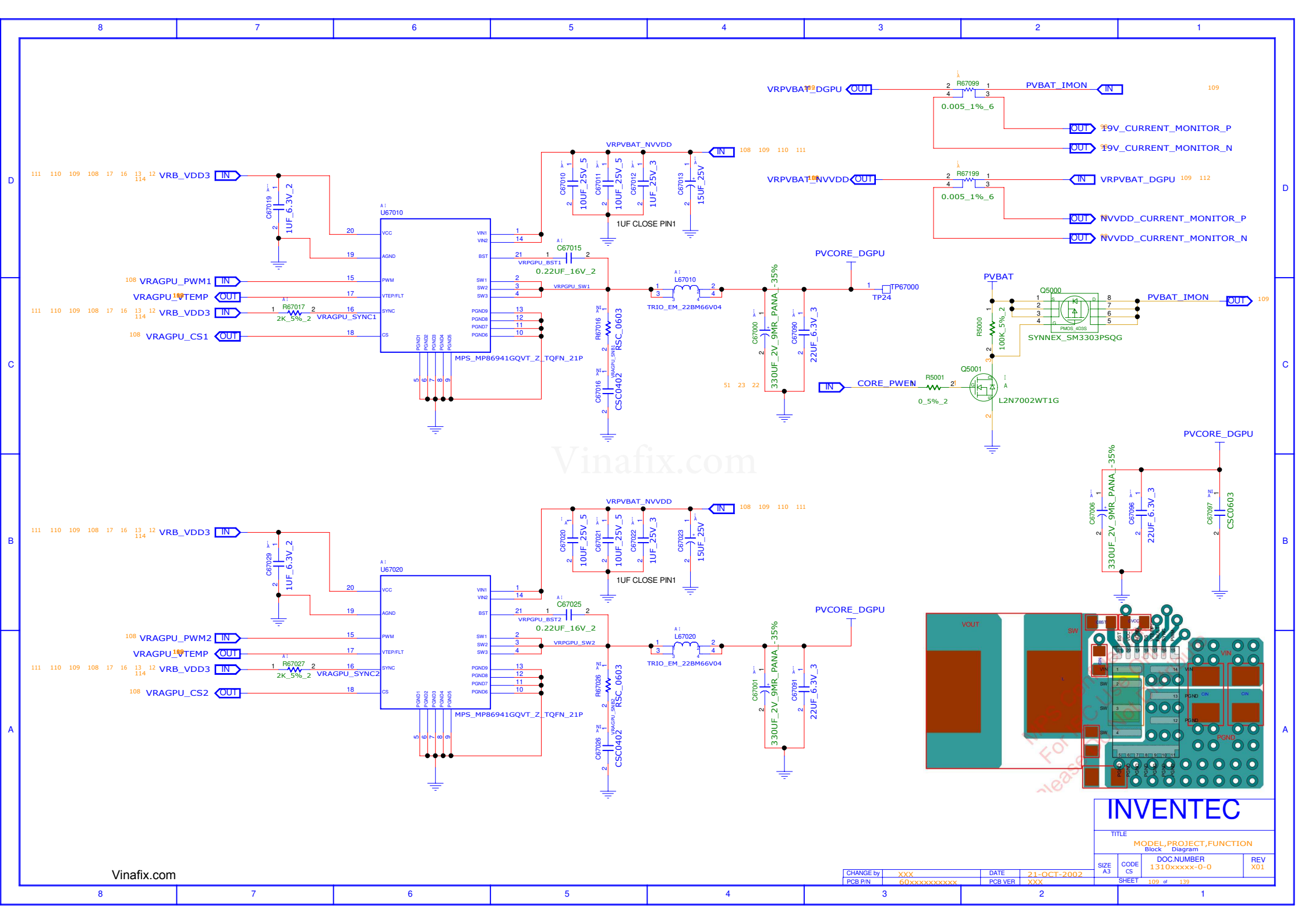
VRPVBAT_DGPU
R67099
PVBAT_IMON
0.005_1%_6
19V_CURRENT_MONITOR_P
19V_CURRENT_MONITOR_N
VRPVBAT_NVVDD
R67199
NVVDD_CURRENT_MONITOR_P
NVVDD_CURRENT_MONITOR_N
VRB_VDD3
U67010
MPS_MP86941GQVT_Z_TQFN_21P
VRAGPU_PWM1
VRAGPU_VTEMP
VRAGPU_SYNC1
VRAGPU_CS1
R67017
2K_5%_2
C67019
1UF_6.3V_2
C67015
0.22UF_16V_2
VRPGPU_BST1
VRPGPU_SW1
1UF CLOSE PIN1
C67010
C67011
C67012
C67013
L67010
TRIO_EM_22BM66V04
R67016
C67016
C67000
C67090
330UF_2V_9MR_PANA_35%
22UF_6.3V_3
PVCORE_DGPU
TP67000
TP24
PVBAT
Q5000
SYNNEX_SM3303PSQG
R5000
100K_5%_2
Q5001
L2N7002WT1G
R5001
0_5%_2
CORE_PWEN
U67020
VRAGPU_PWM2
VRAGPU_VTEMP
VRAGPU_SYNC2
VRAGPU_CS2
R67027
2K_5%_2
C67029
C67025
0.22UF_16V_2
VRPGPU_BST2
VRPGPU_SW2
C67020
C67021
C67022
C67023
L67020
R67026
C67026
C67001
C67091
C67006
C67096
C67097
VCOUT
SW
VIN
PGND
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60xxxxxxxxxx
PCB VER
XXX
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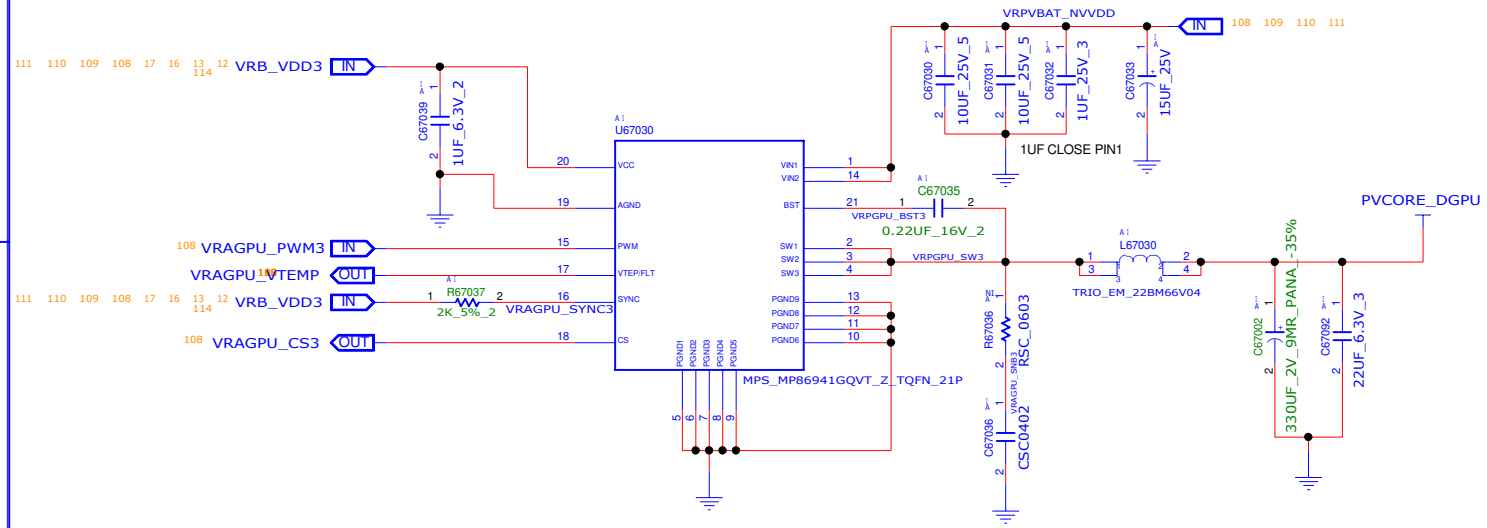

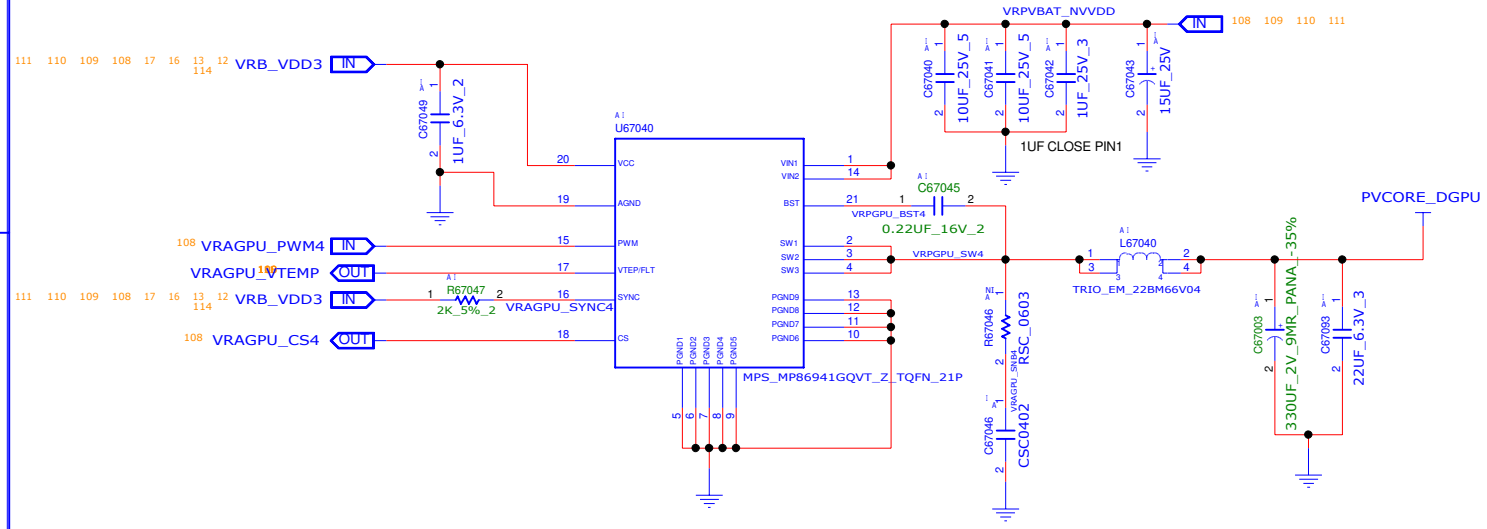

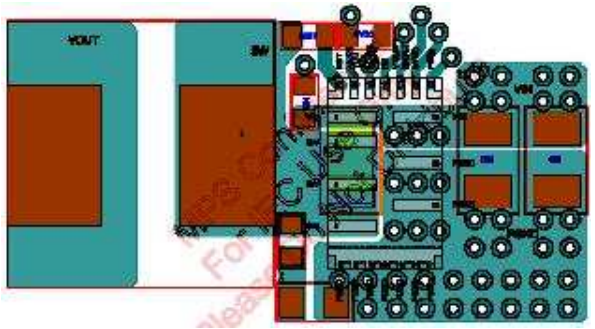

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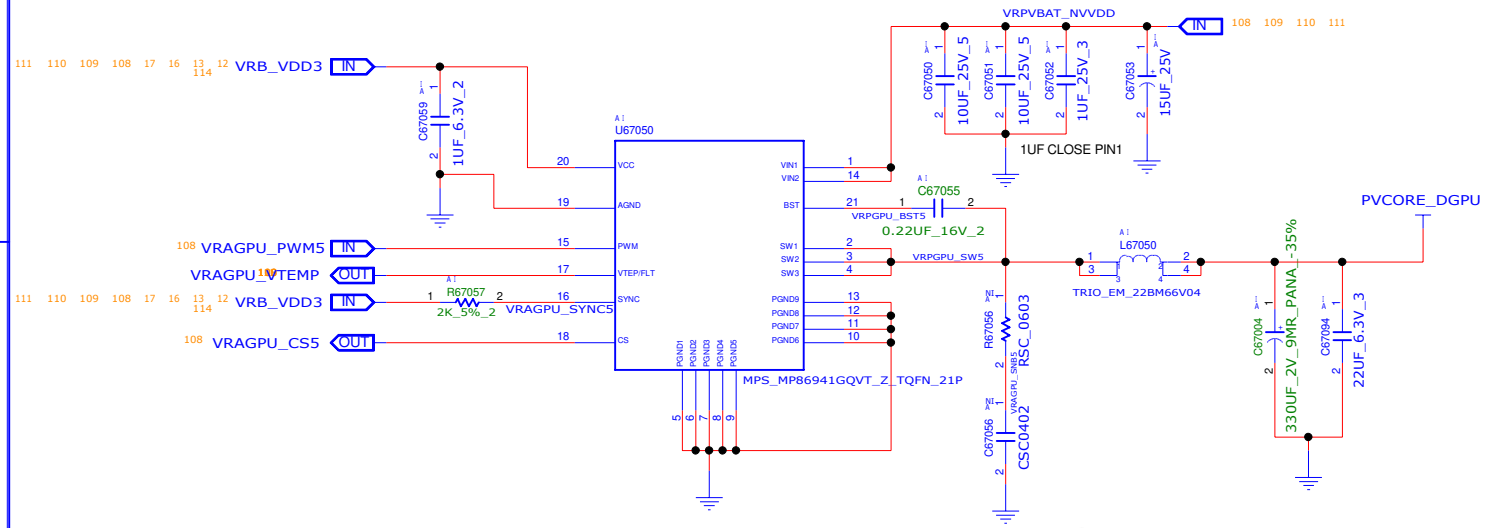
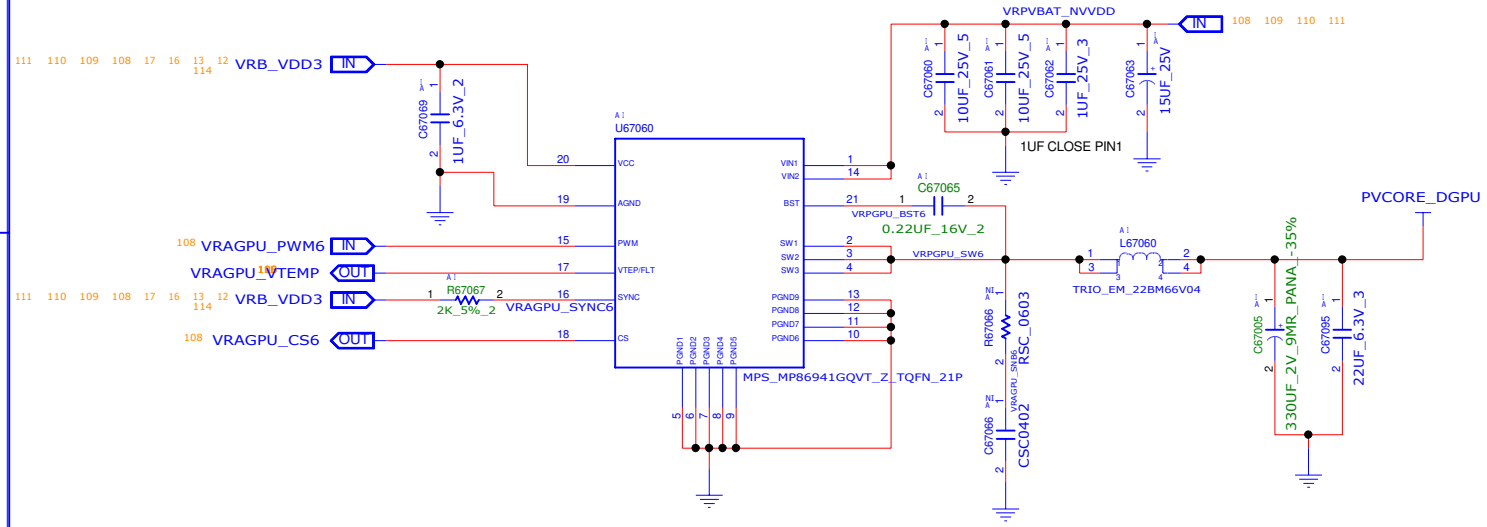
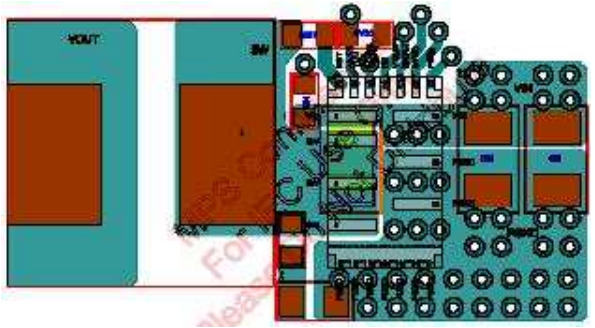
PCB P/N	60xxxxxxxxx	PCB VER	XXX		







INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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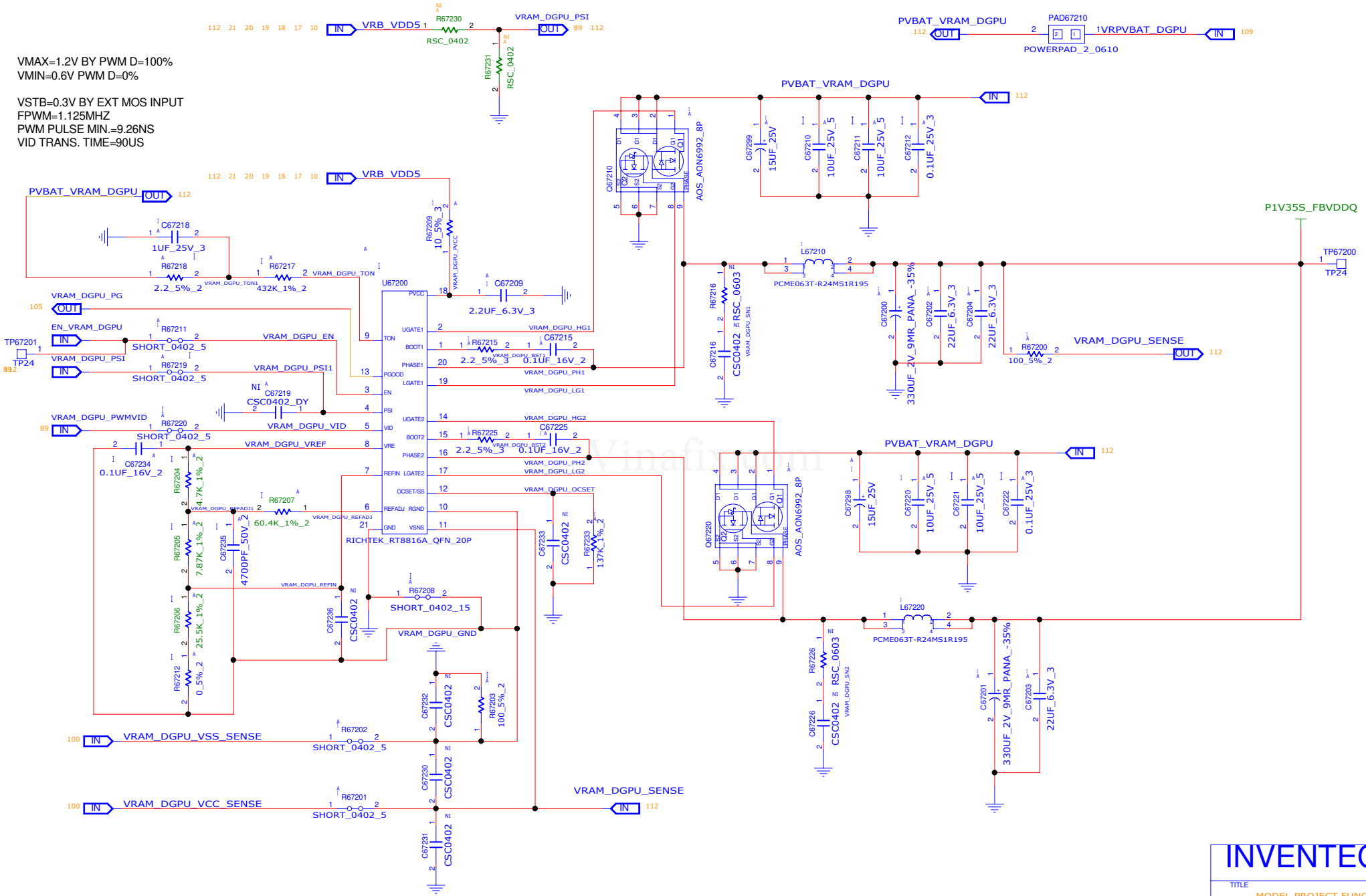
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VMIN=0.6V PWM D=0%
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=90US
VRB_VDD5
R67230
RSC_0402
VRAM_DGPU_PSI
R67231
PVBAT_VRAM_DGPU
PAD67210
1VRPVBAT_DGPU
POWERPAD_2_0610
AOS_AON6992_8P
C67299
15UF_25V
C67210
10UF_25V_5
C67211
C67212
0.1UF_25V_3
C67218
1UF_25V_3
R67218
2.2_5%_2
R67217
432K_1%_2
VRAM_DGPU_TON
U67200
R67209
10_5%_2
C67209
2.2UF_6.3V_3
VRAM_DGPU_PG
EN_VRAM_DGPU
R67211
SHORT_0402_5
VRAM_DGPU_EN
TP67201
TP24
R67219
VRAM_DGPU_PSI1
C67219
CSC0402_DY
VRAM_DGPU_PWMVID
R67220
VRAM_DGPU_VID
C67234
0.1UF_16V_2
VRAM_DGPU_VREF
R67204
4.7K_1%_2
R67207
60.4K_1%_2
R67205
7.87K_1%_2
C67235
4700PF_50V_2
R67206
25.5K_1%_2
R67212
0_5%_2
RICHTEK_RT8816A_QFN_20P
R67208
SHORT_0402_15
VRAM_DGPU_GND
C67236
CSC0402
C67232
R67203
100_5%_2
R67202
VRAM_DGPU_VSS_SENSE
C67230
R67201
VRAM_DGPU_VCC_SENSE
C67231
VRAM_DGPU_SENSE
C67233
R67233
137K_1%_2
L67210
PCME063T-R24MS1R195
R67216
RSC_0603
CSC0402
C67216
330UF_2V_9MR_PANA_-35%
C67202
22UF_6.3V_3
C67204
R67200
100_5%_2
P1V35S_FBVDDQ
TP67200
TP24
C67298
C67220
C67221
C67222
L67220
R67226
C67226
C67201
C67203
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
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1310xxxxx-0-0
REV
X01
SIZE
A3
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XXX
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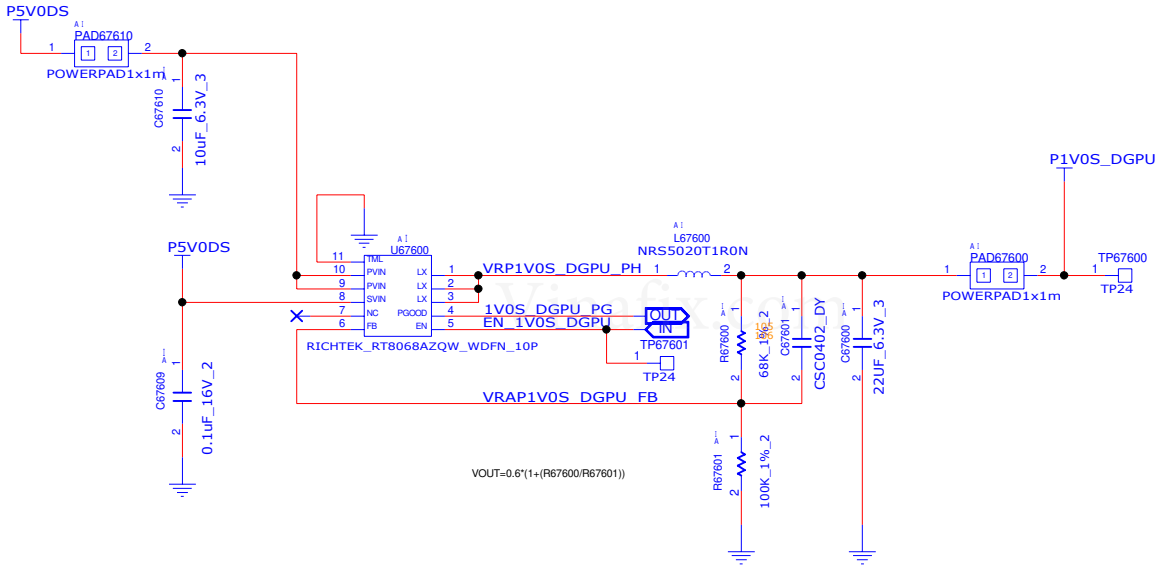

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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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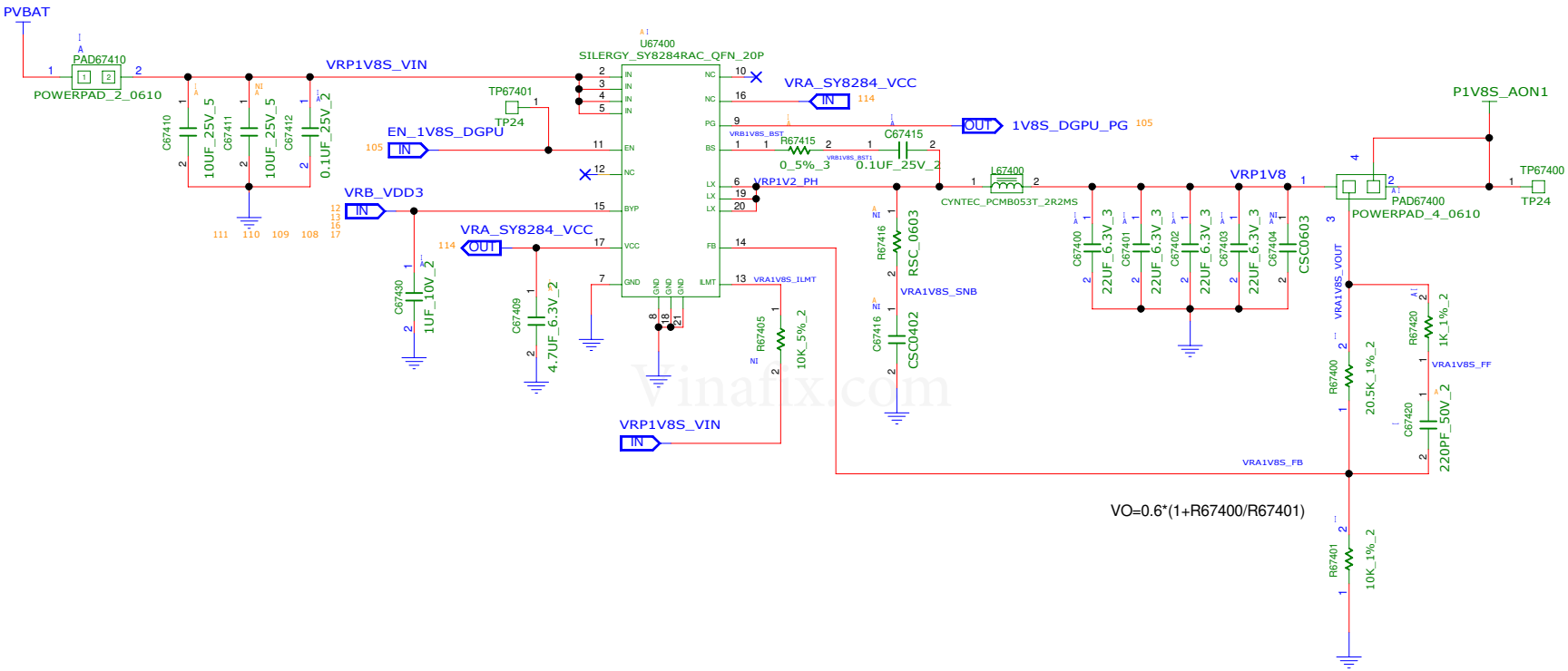

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms)[2] (A)	Input EDPp (5ms)[2] (A)	Input EDPc (1sec)[1] (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$Input\ EDPc\ Current\ (A) = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$Input\ EDPp\ (A) at\ V_{new} = Input\ EDPp(A)\ at\ 19Vx\ \frac{19\text{V}}{V_{new}(\text{V})}$$

Table 12. Output EDP-Continuous

Product	TGP (W)	NVVDD — (A)	FB TOTAL[5] 1.35V[3, 4] (A)	1.0V Total[1] 1.0V[3] (A)	1.8V Total[2] 1.8V[3] (A)
N18E-G3	150	144	46	1.6	2.3
	160	152			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Table 14. Output EDP-Peak

Product	TGP (W)	NVVDD - (A)	FB TOTAL[4] 1.35V[2, 3] (A)	1.0V Total[1] 1.0V[2] (A)	1.8V Total[2] 1.8V[5] (A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

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HISTORY

SCHEMATIC MODIFY HISTORY

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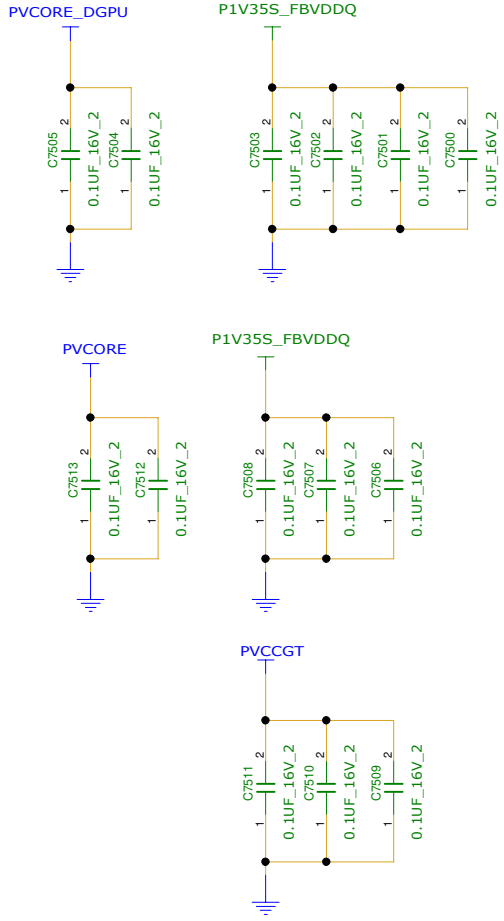
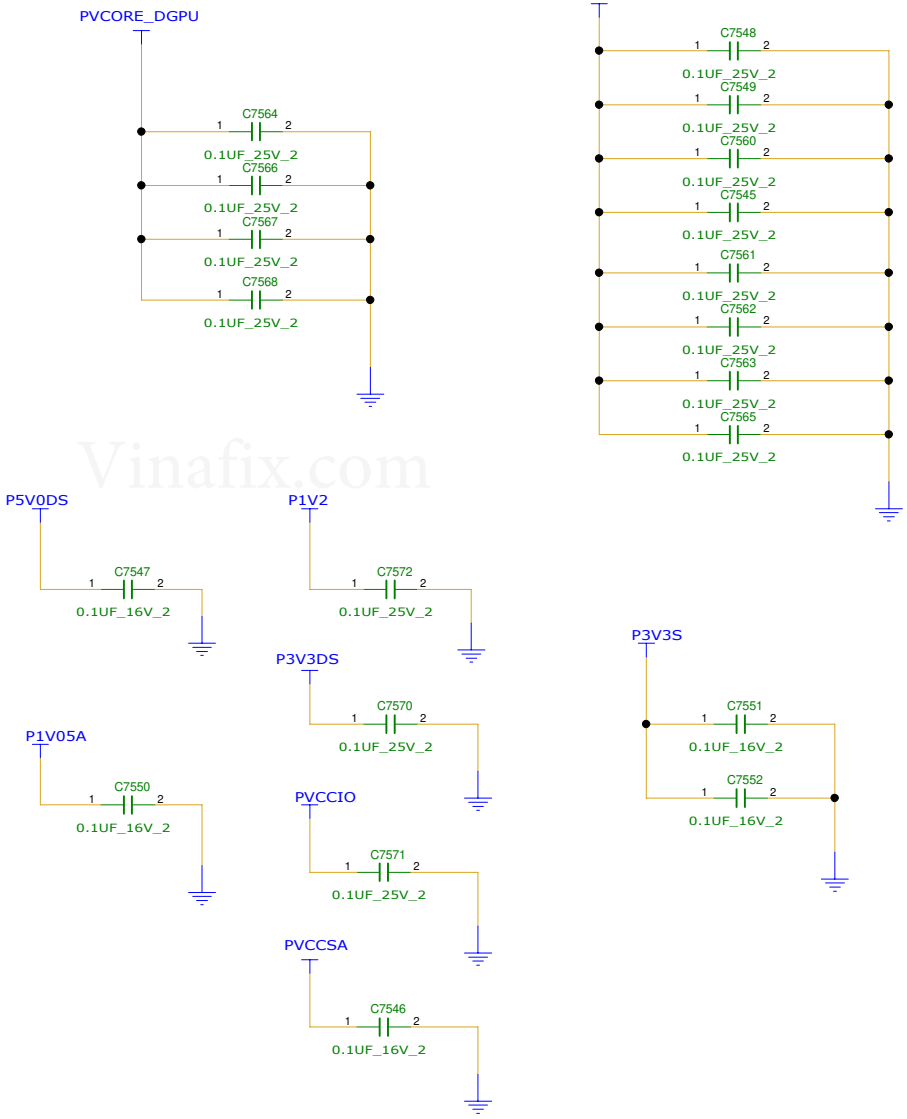
EMI





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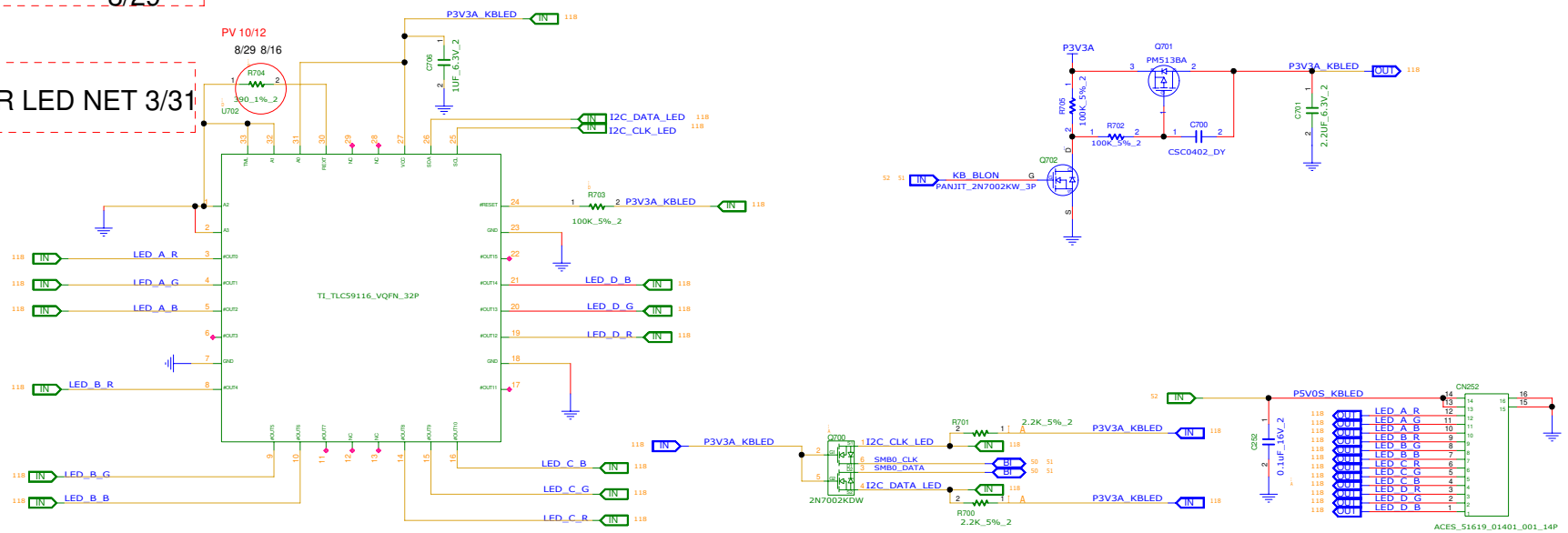
ADJUST LED RES 8/16
8/29

RE-ORDER LED NET 3/31



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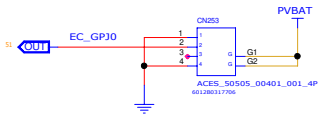

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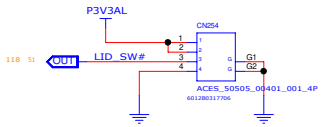

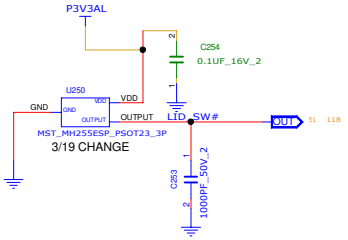

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INVENTEC

MODEL,PROJECT,FUNCTION
RING LED

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-D-D	X01

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TURBO# BOARD

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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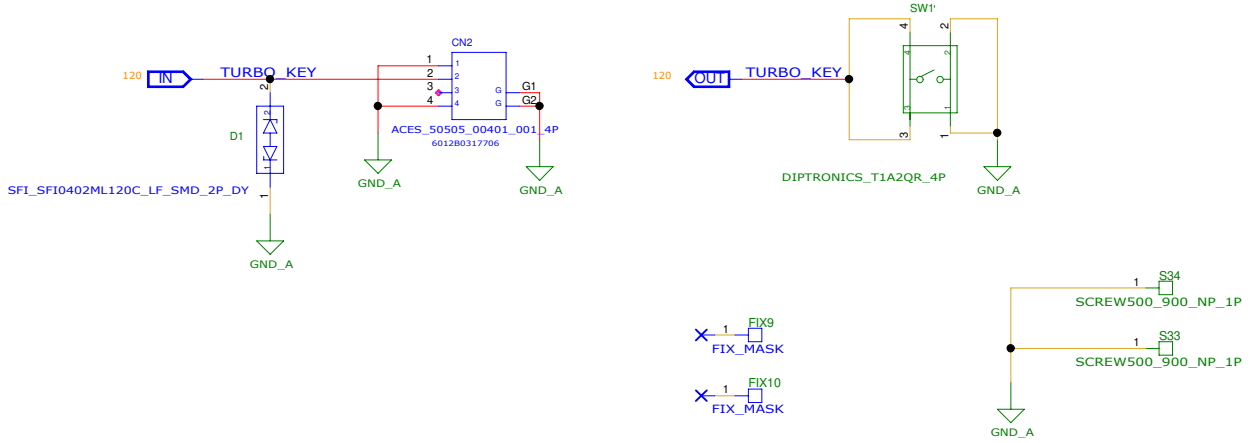
TURBO#



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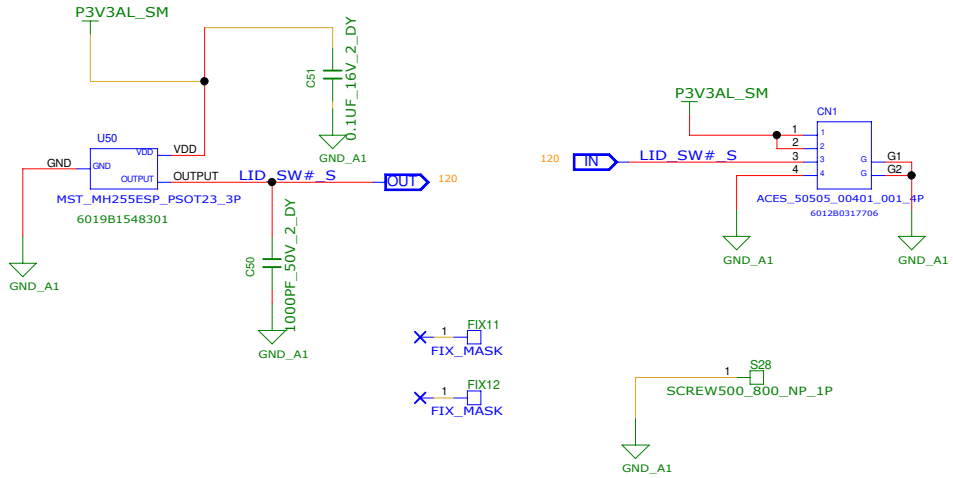

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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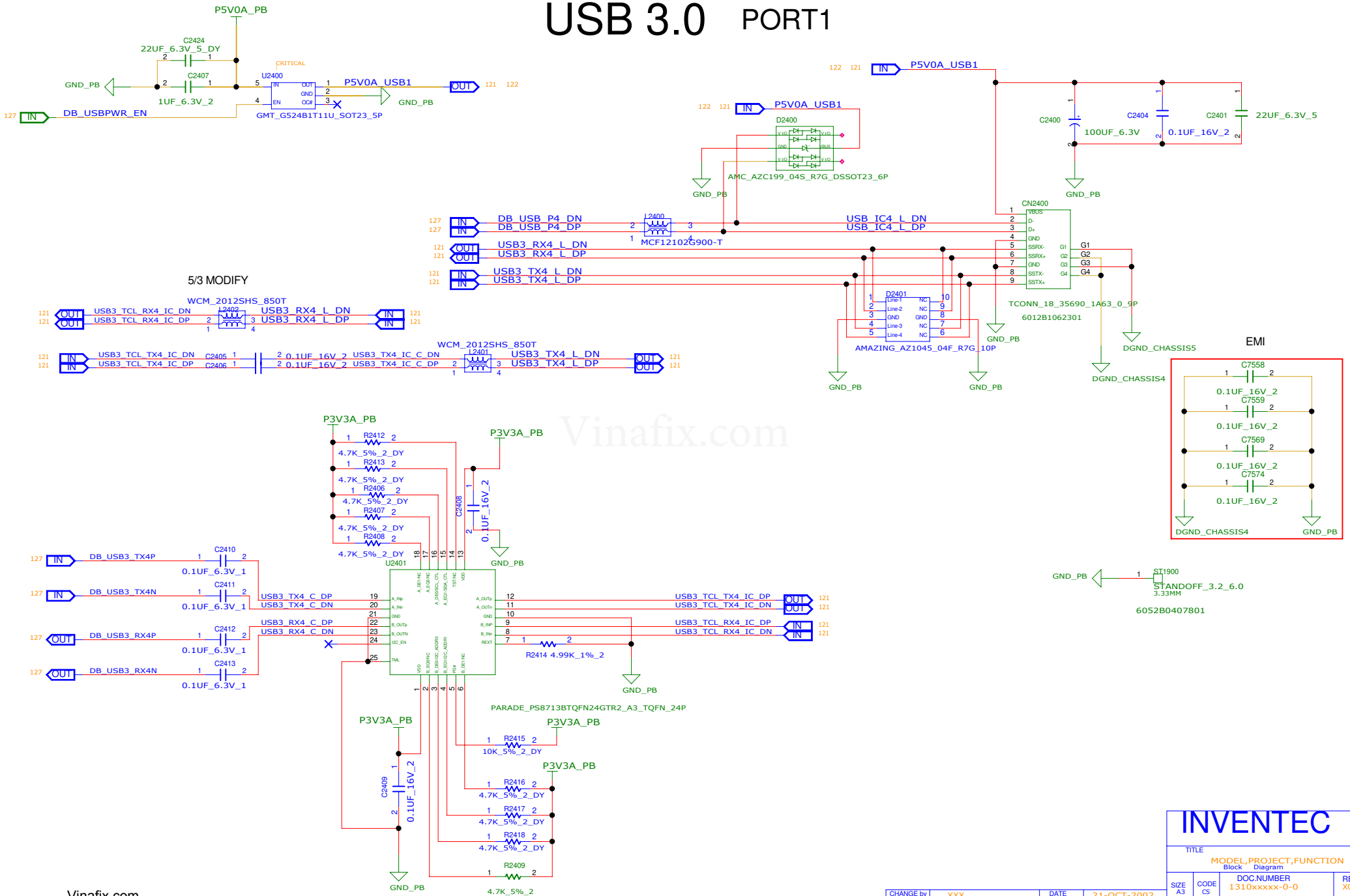
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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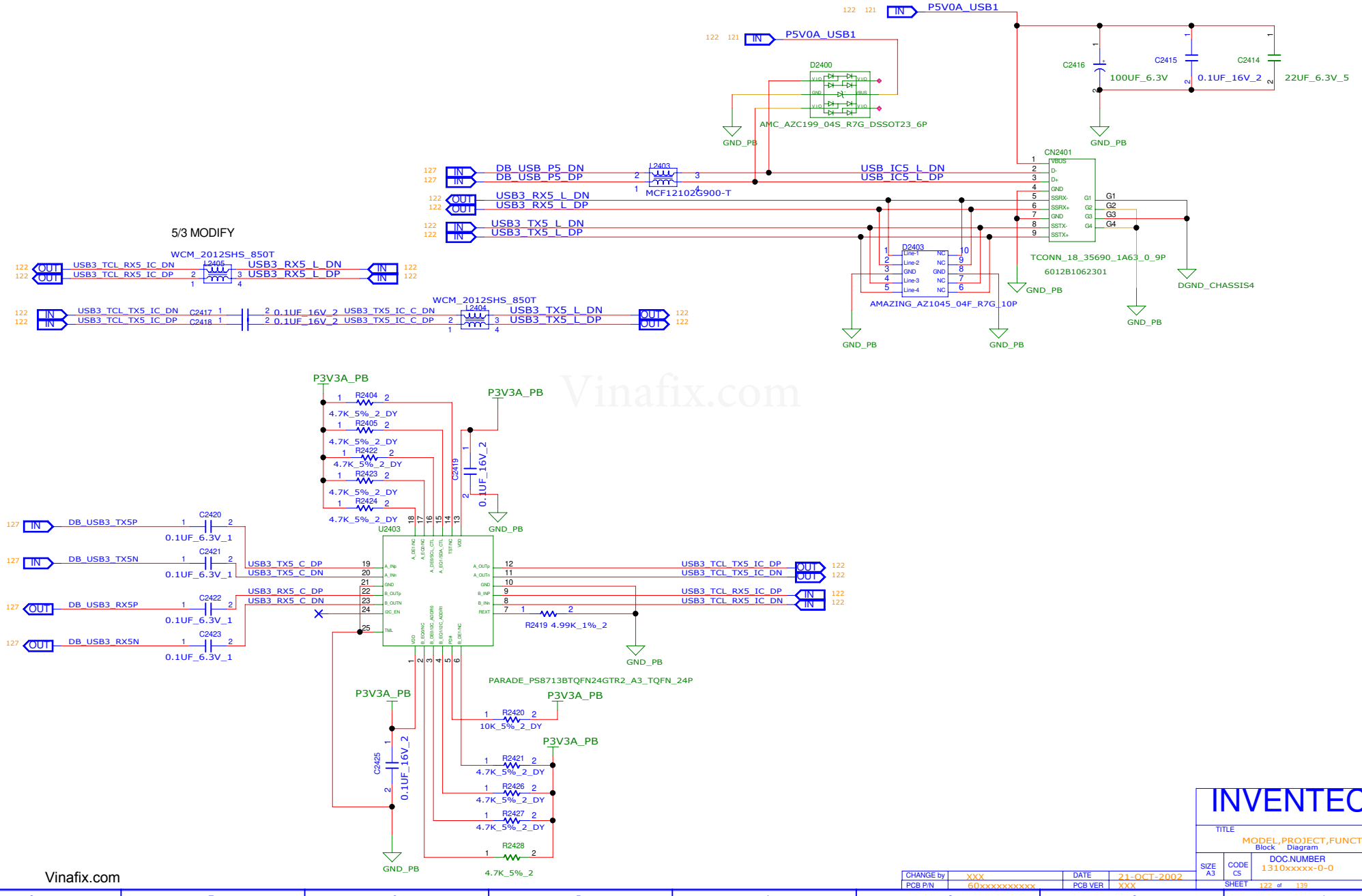
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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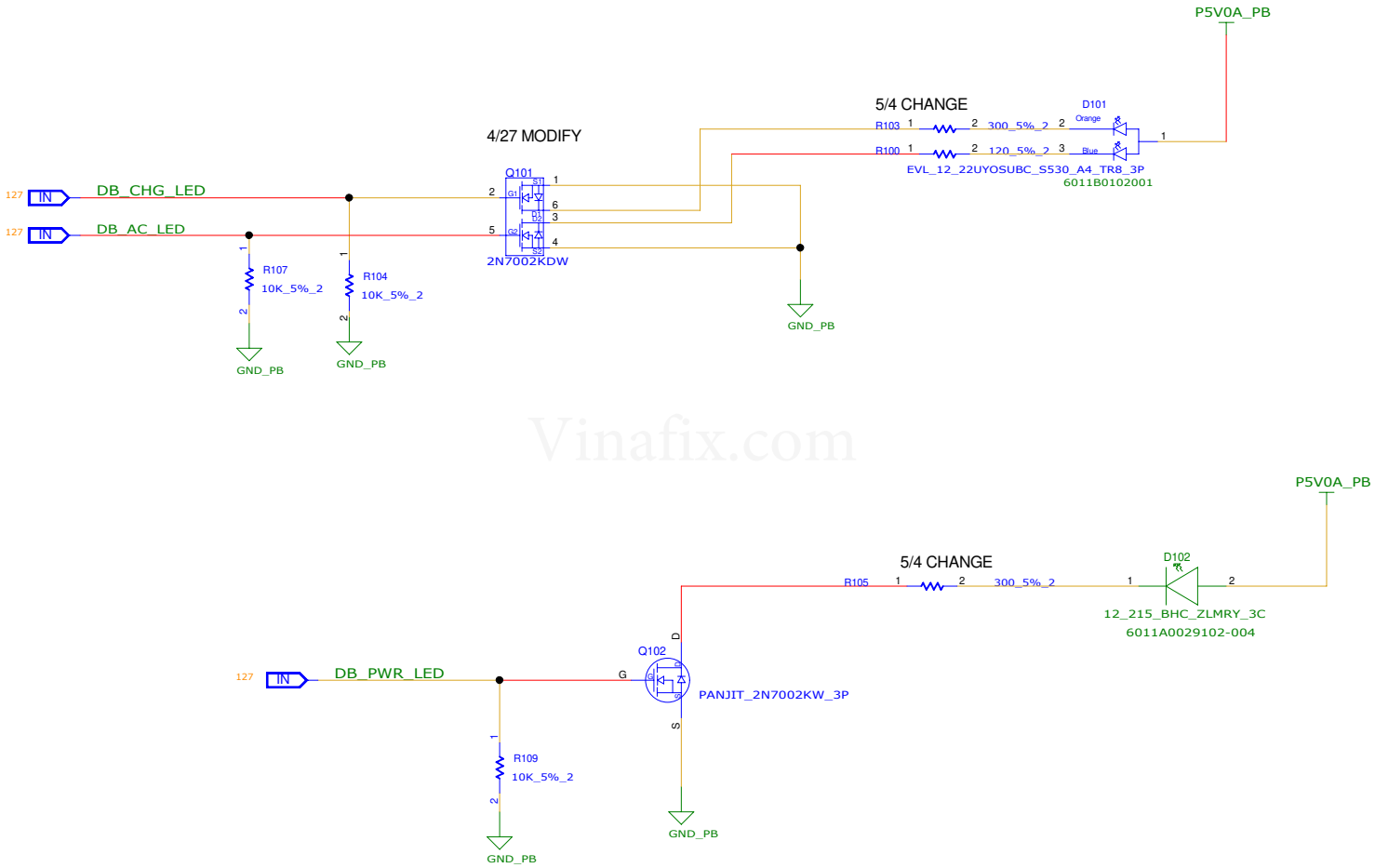

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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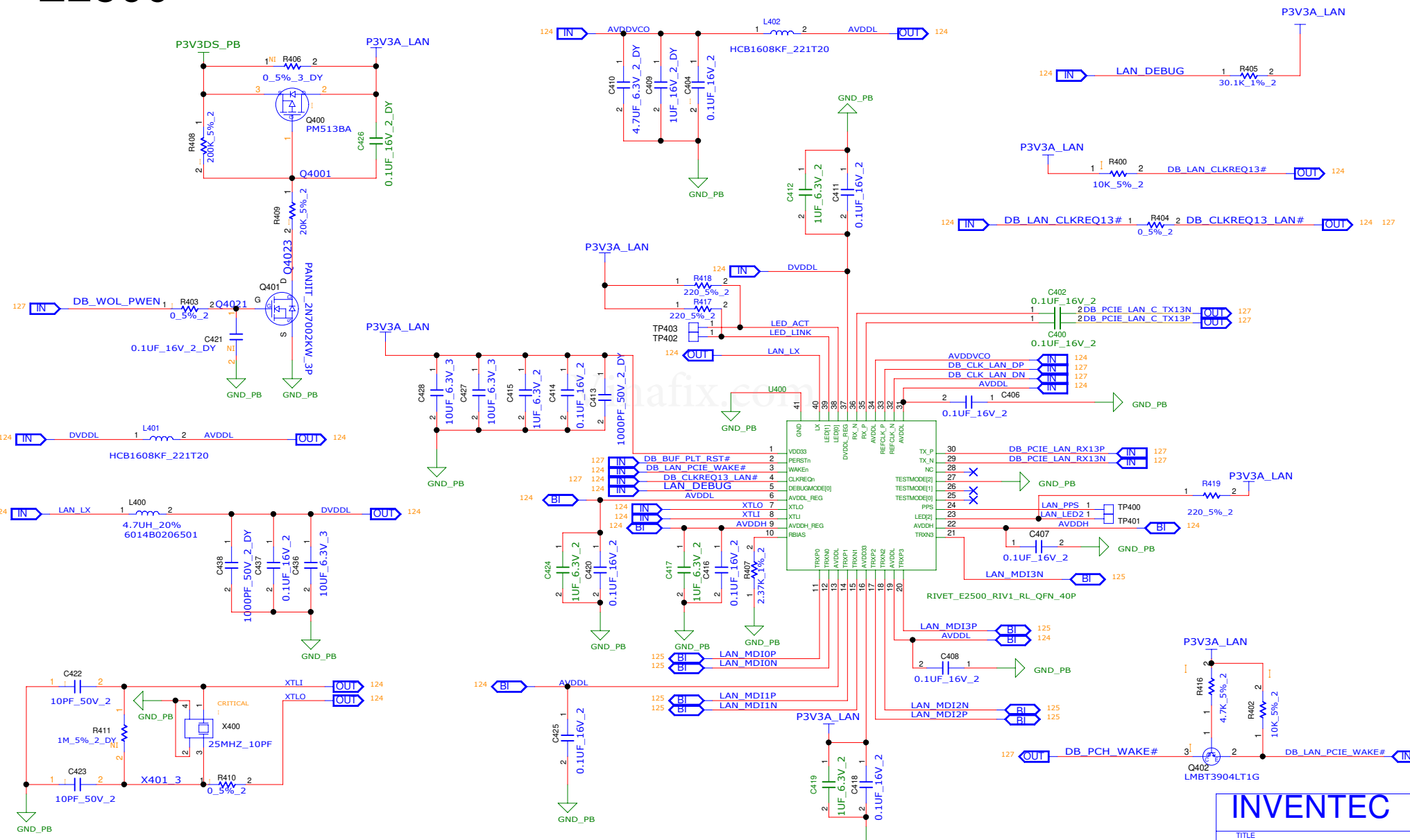
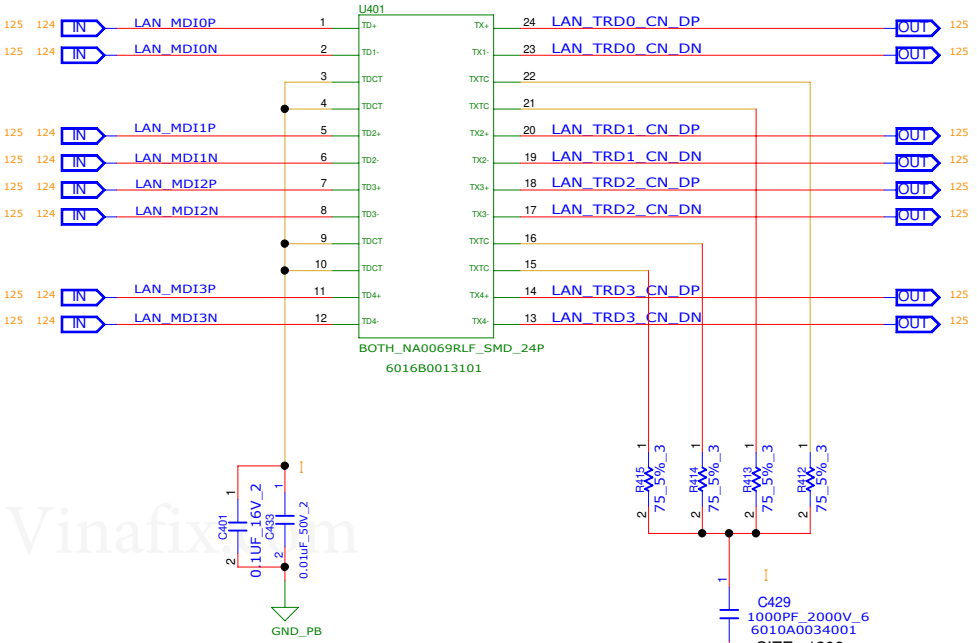
LAN (CONTROLLER)
E2500



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION USB/DP DE-MUX		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 124 of 139	
PCB P/N 60xxxxxxxxx	PCB VER XXX		

TRANSFORMER



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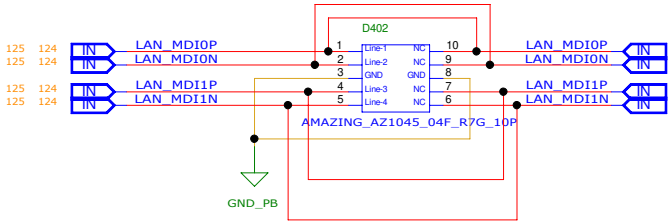
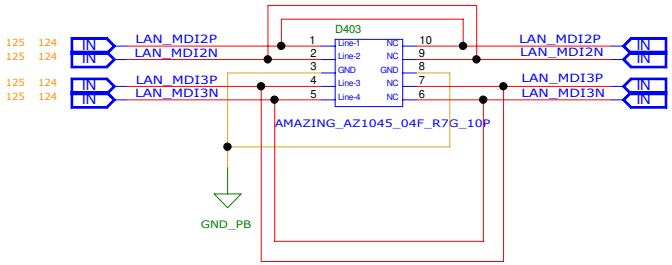
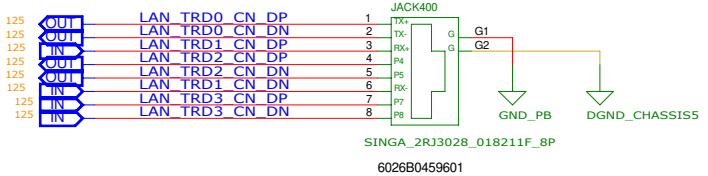
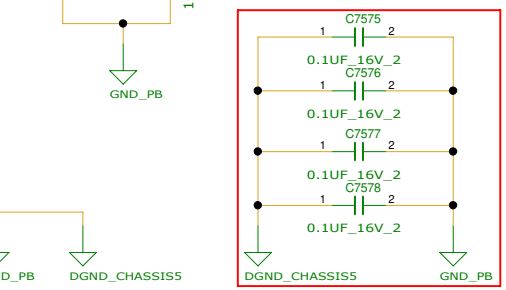




RJ-45





INVENTEC

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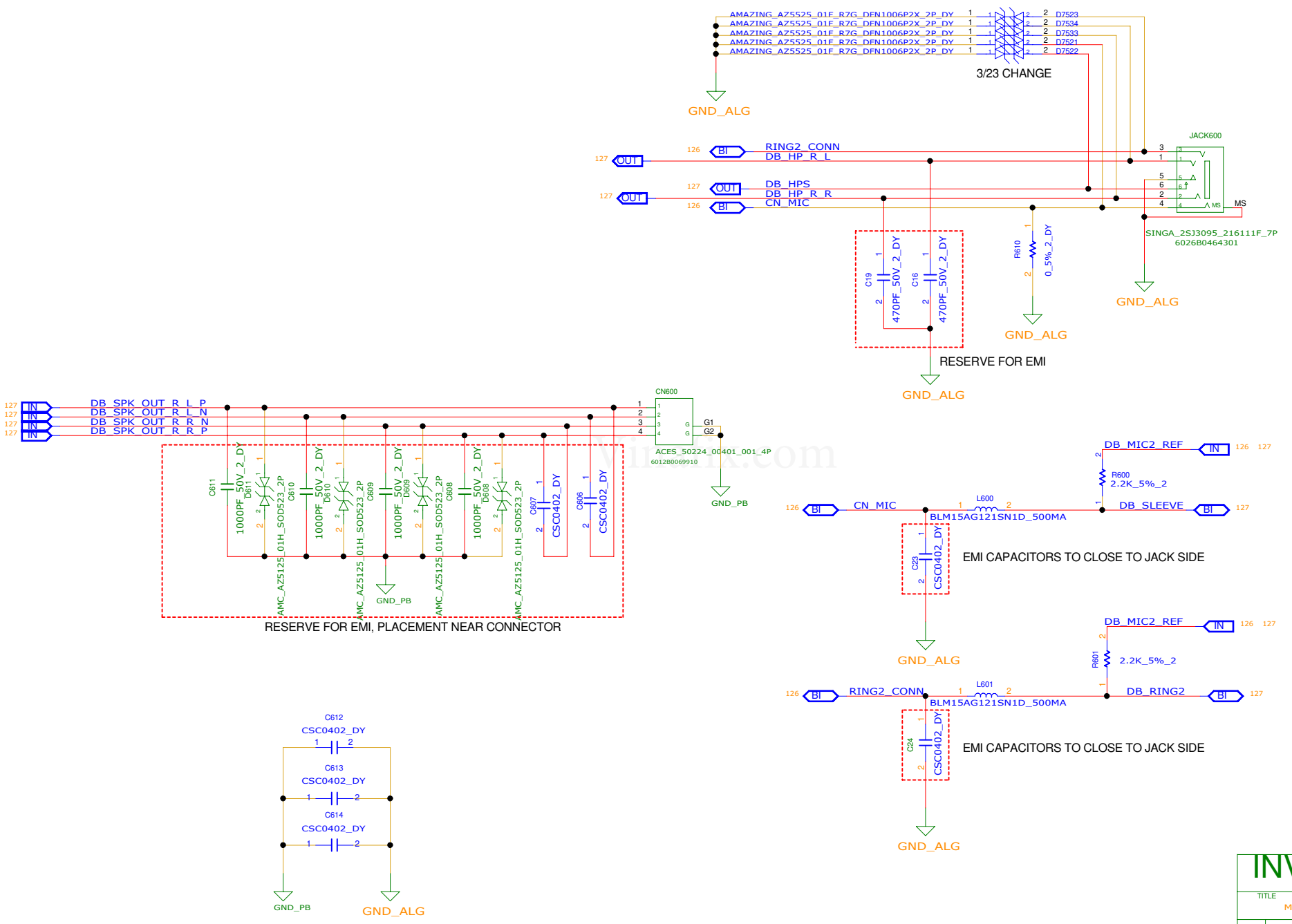

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TITLE: MODEL,PROJECT,FUNCTION
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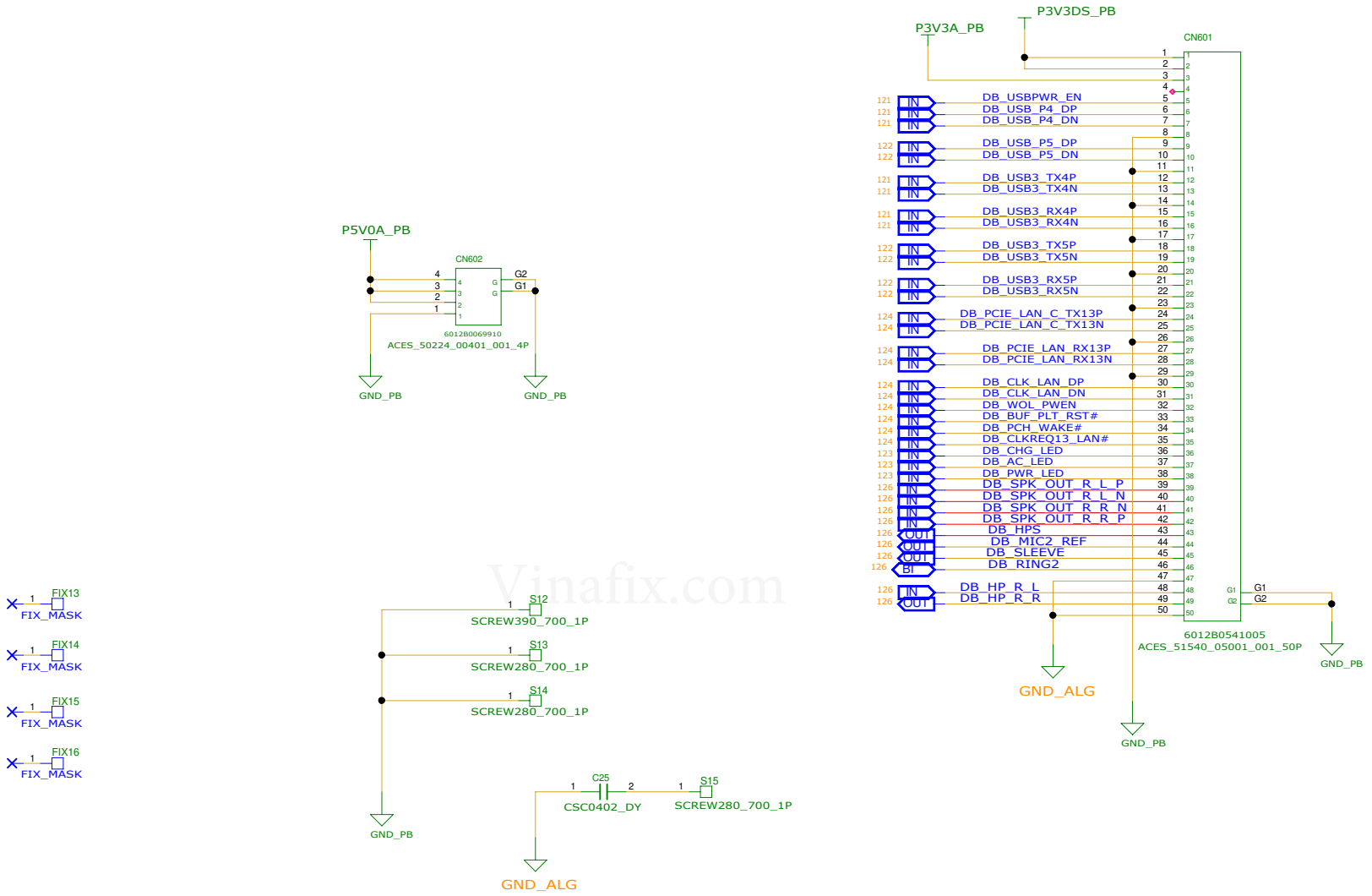

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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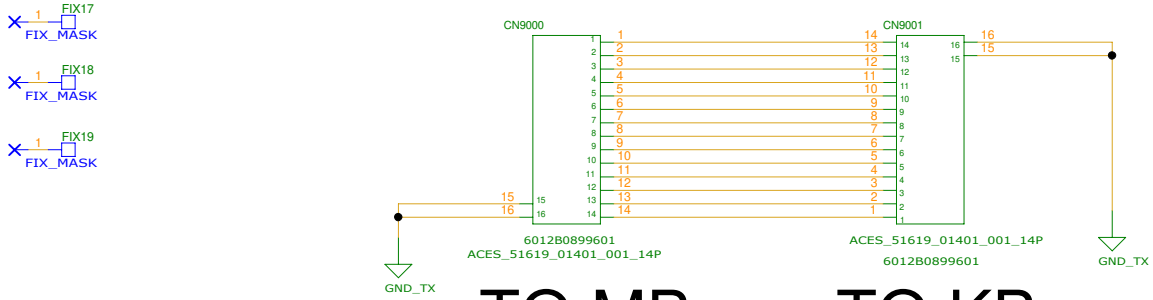
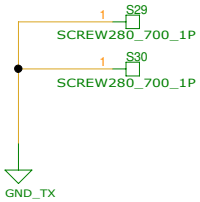
6050A3090601





CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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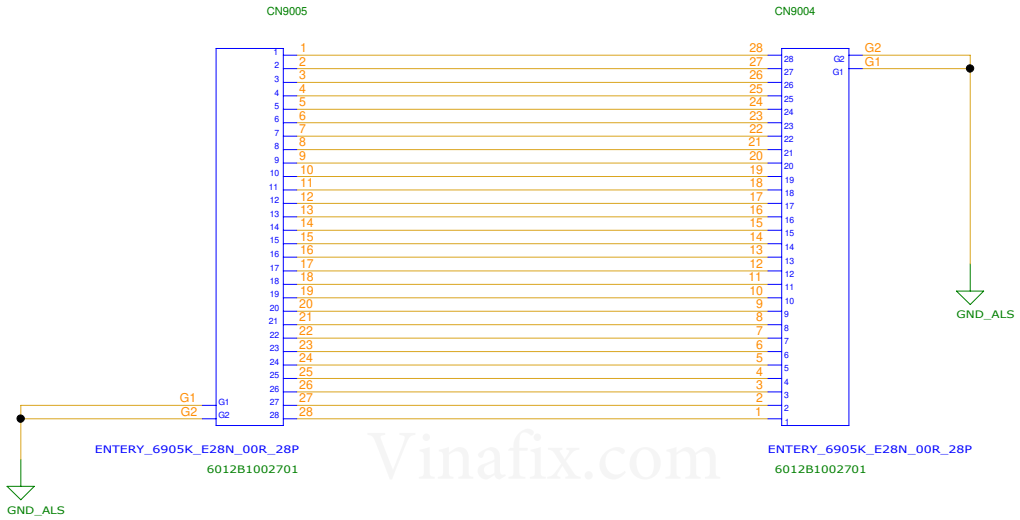

TO MB

TO KB

CHANGE by	XXX	DATE	21-OCT-2002
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TITLE: MODEL,PROJECT,FUNCTION
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FOR 15 AUDIO BOARD

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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A3	CS	1310xxxxx-0-0	X01

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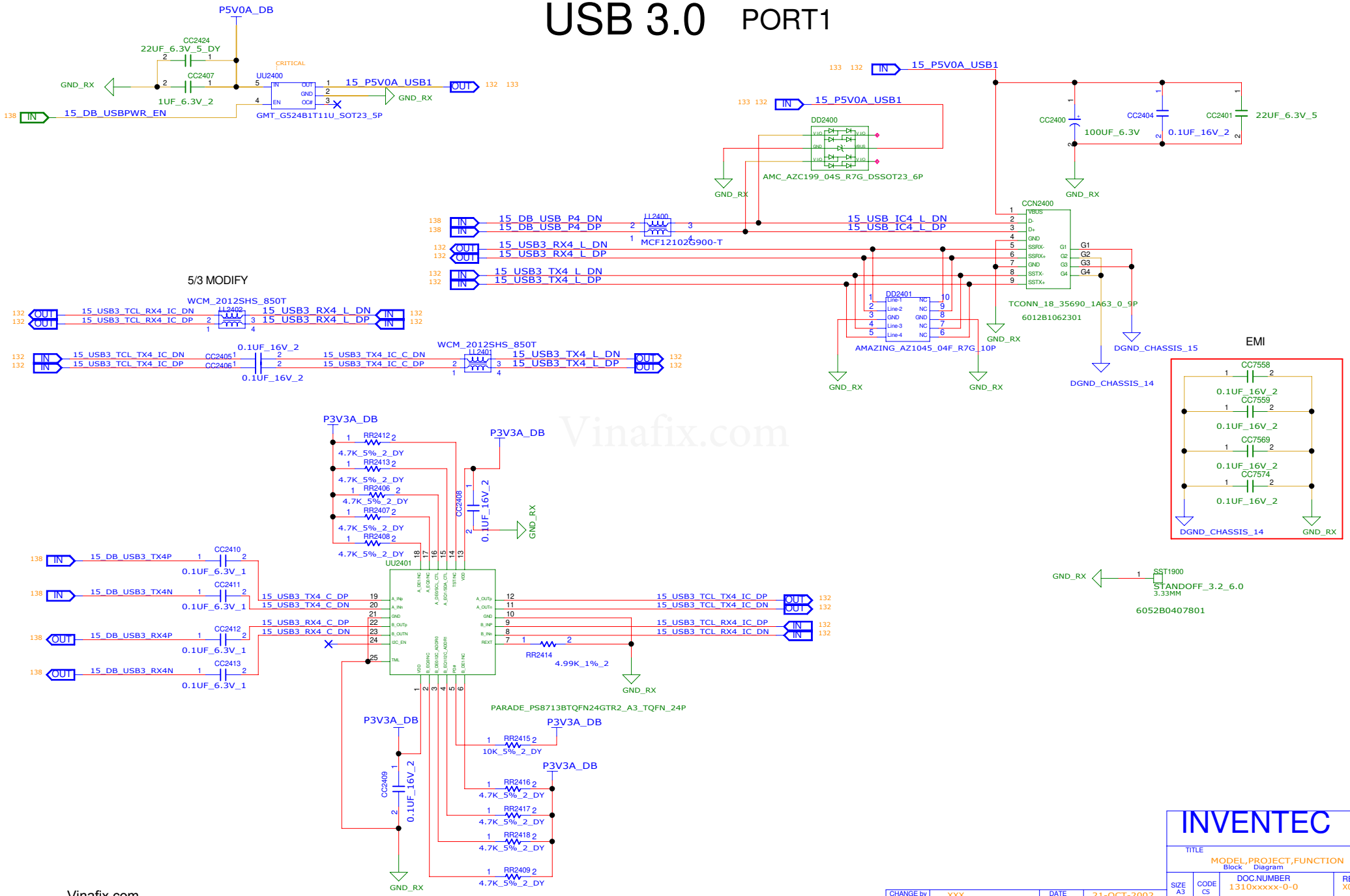
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



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TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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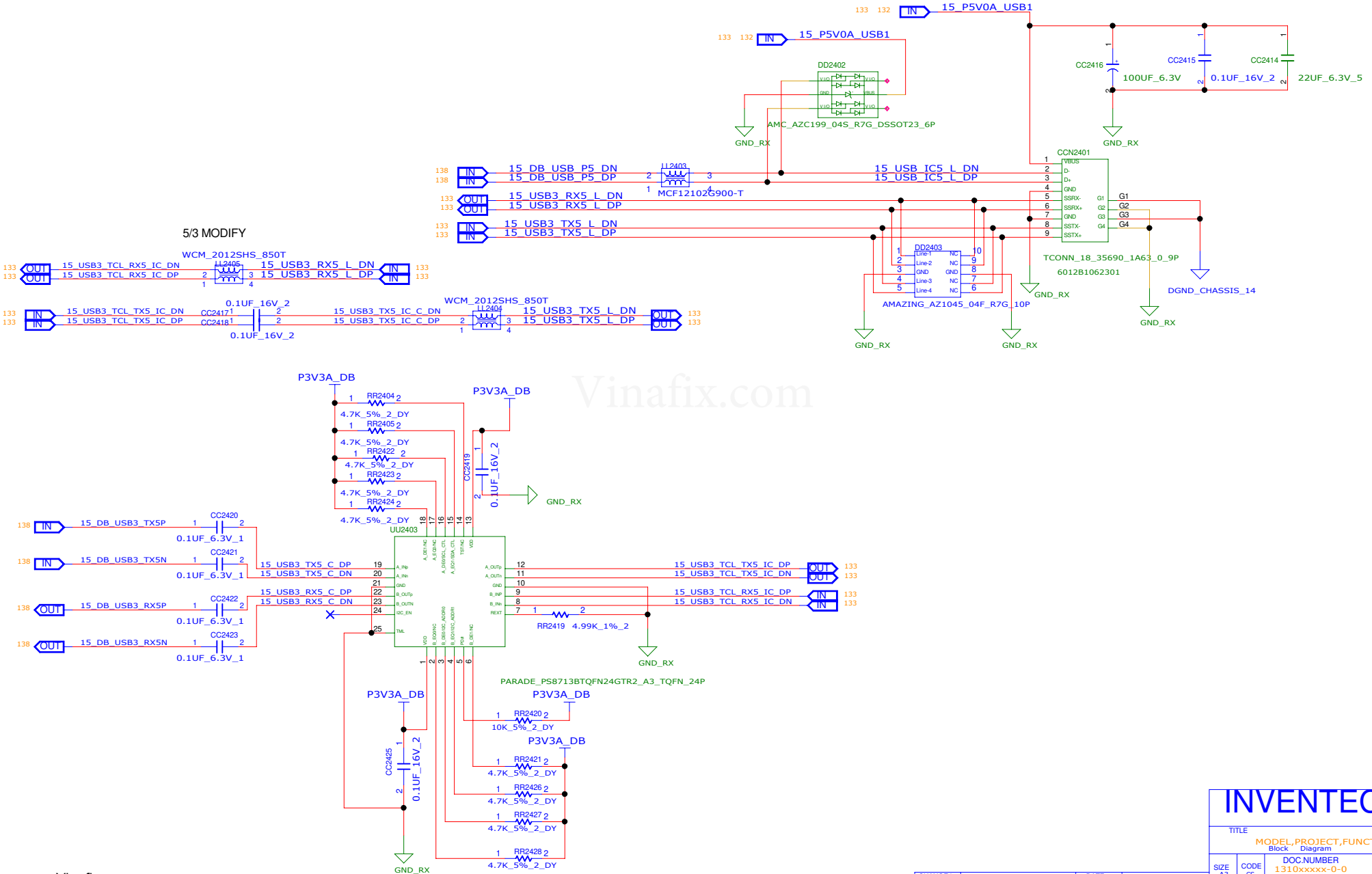
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



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TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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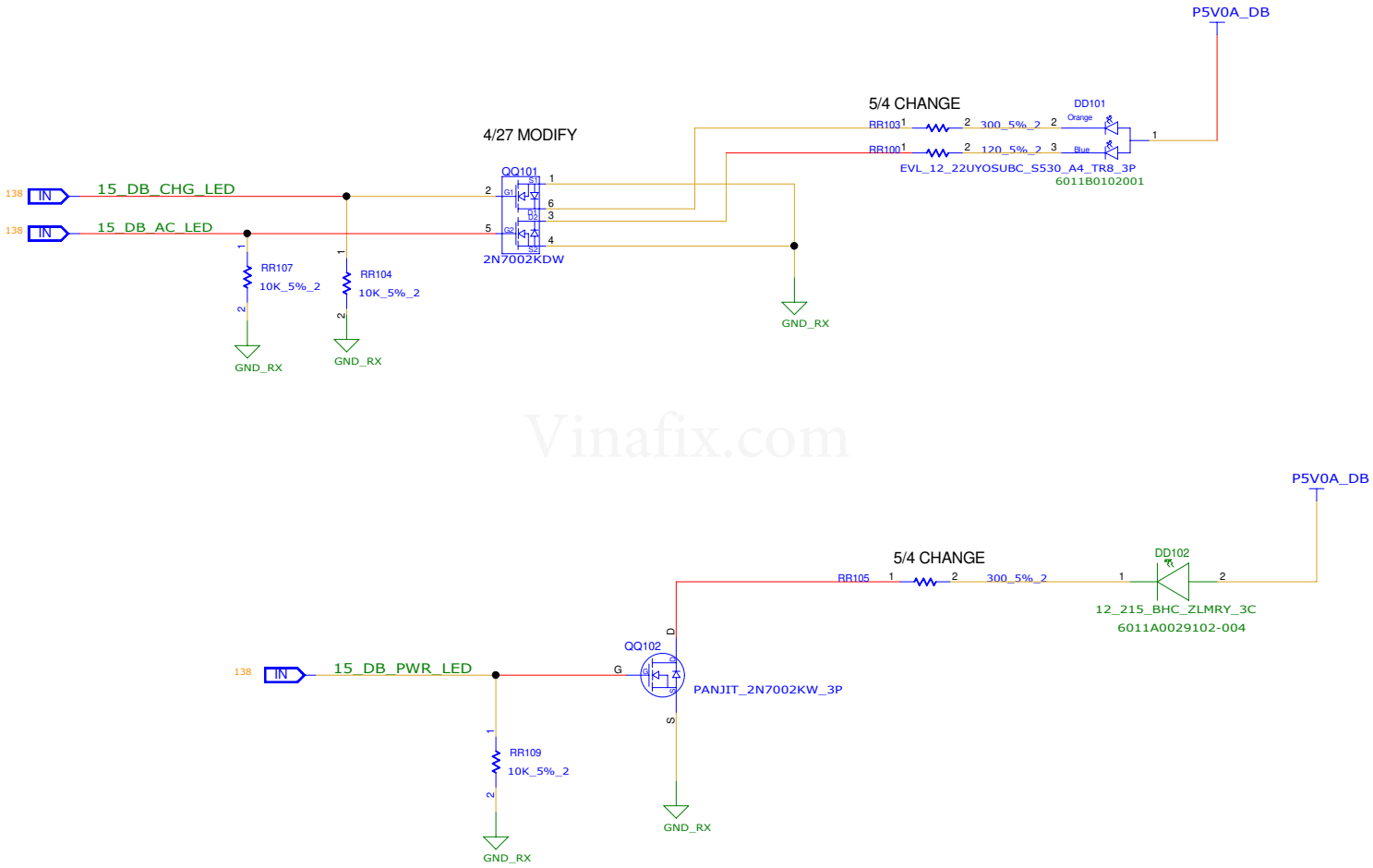

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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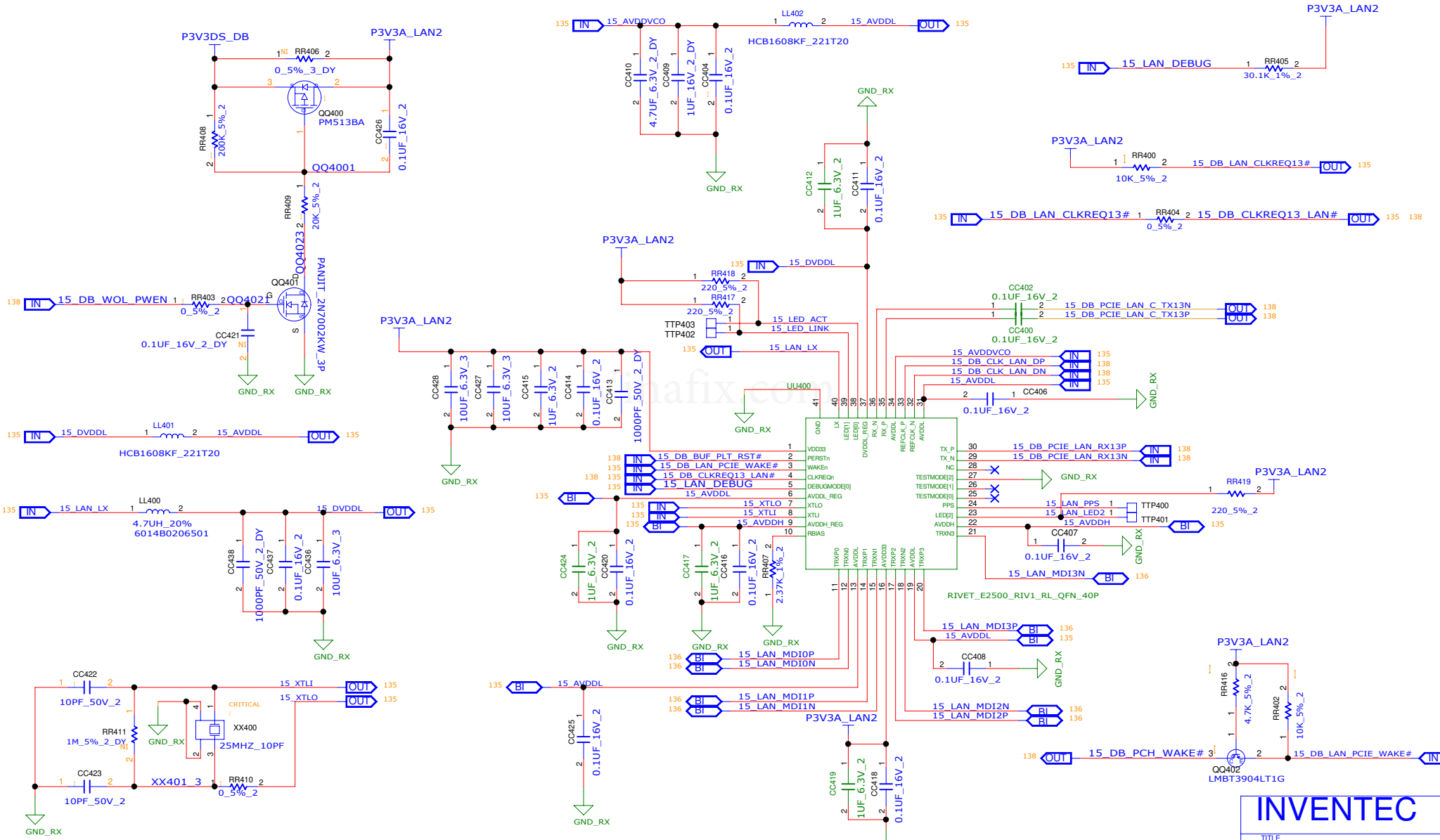
LAN (CONTROLLER)
E2500



Vinafix.com

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
USB/DP DE-MUX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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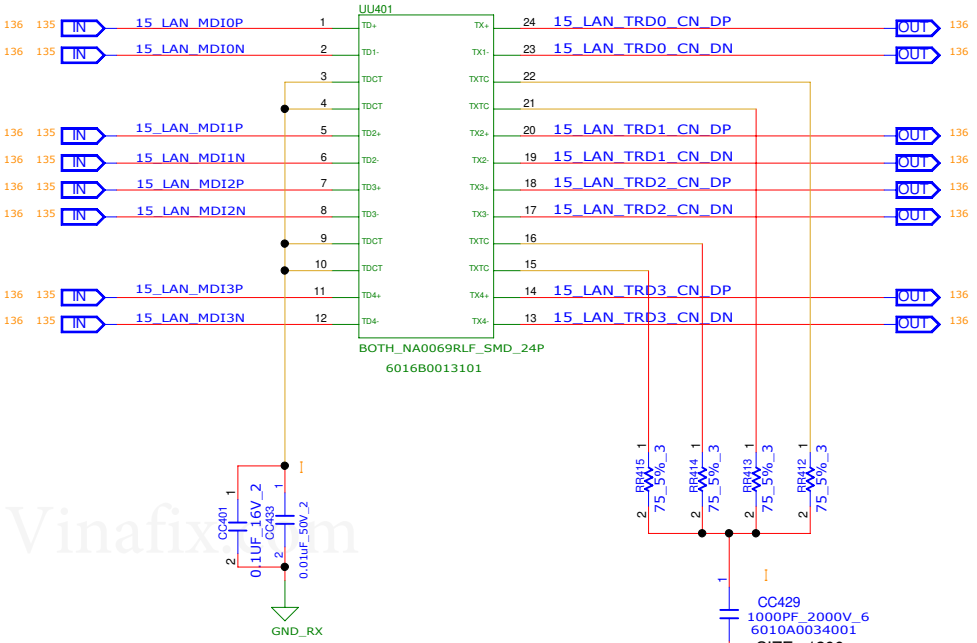
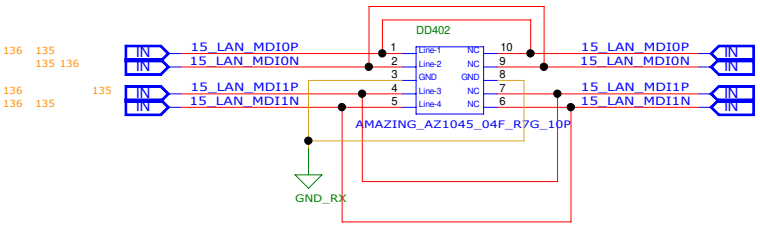
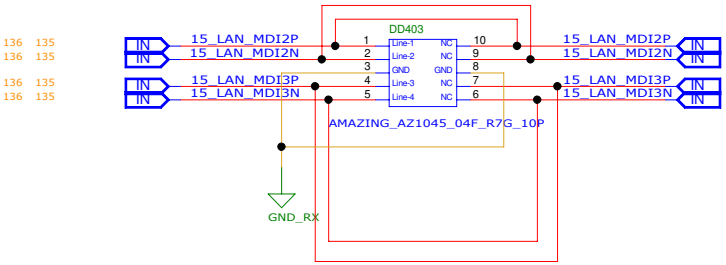
TRANSFORMER

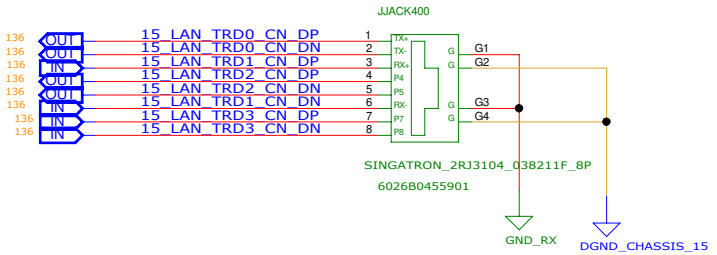


ESD

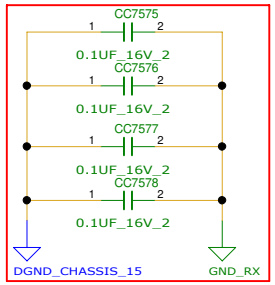




RJ-45



EMI



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
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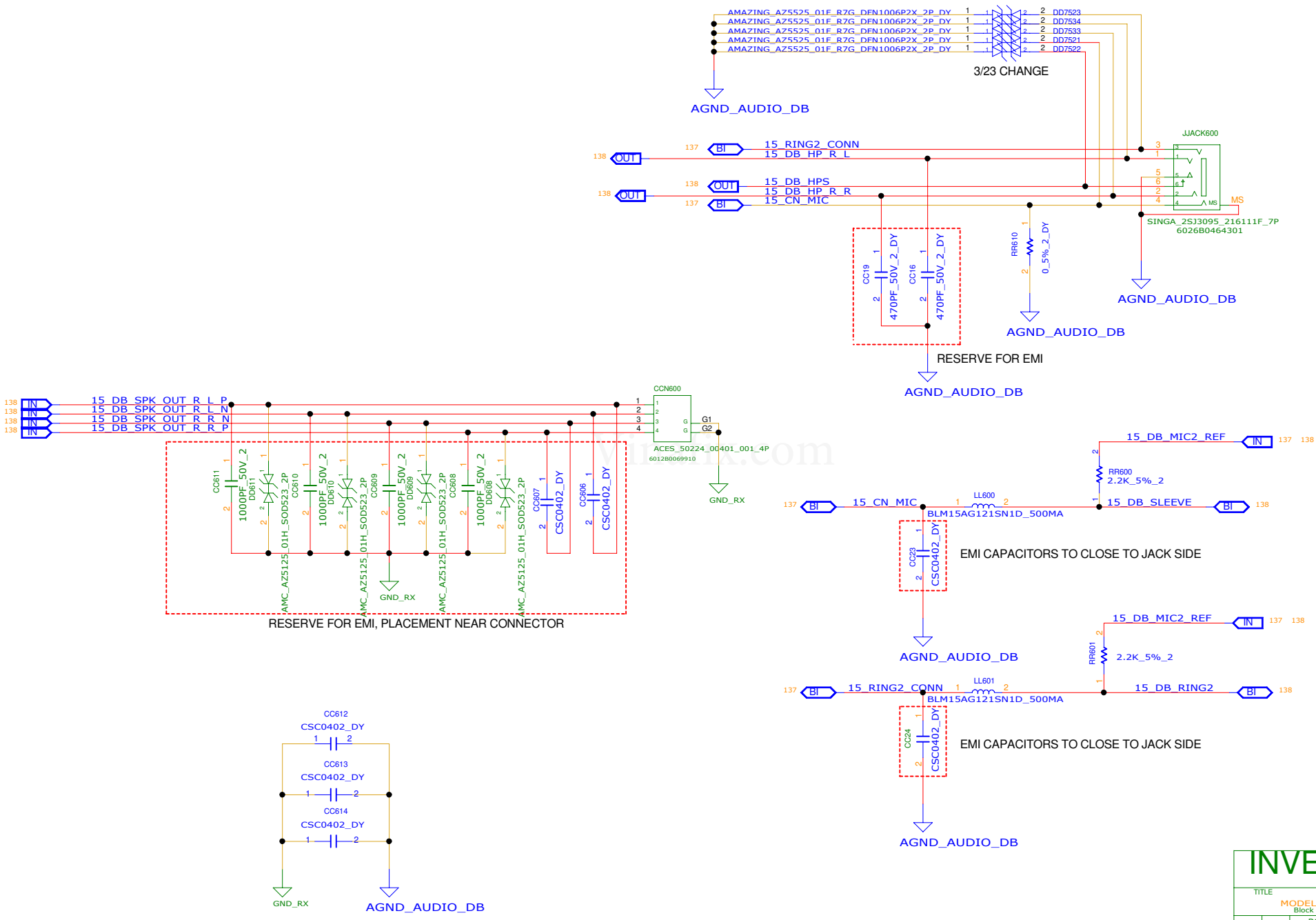

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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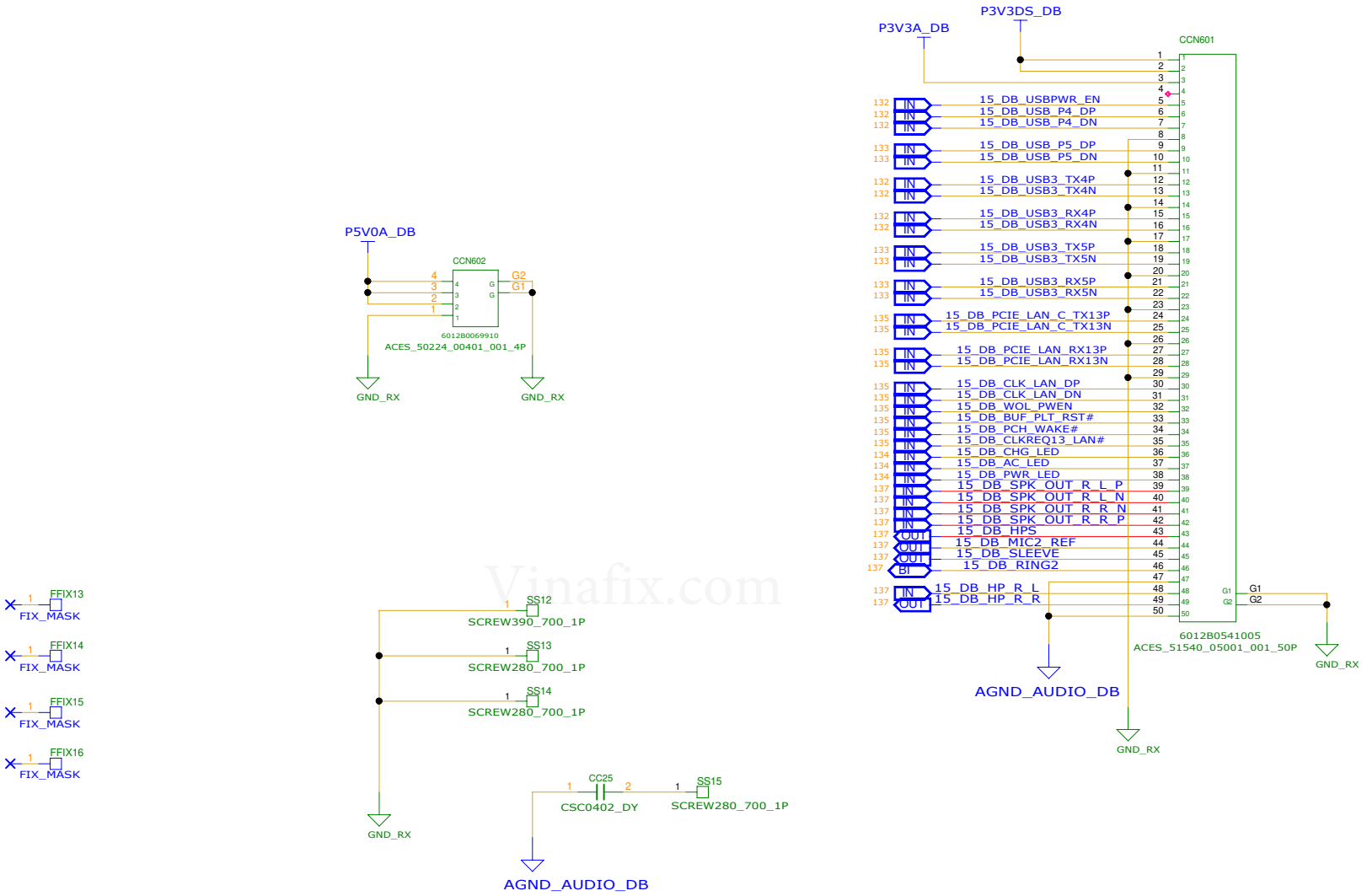

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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TITLE
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Block Diagram

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